



# B1L103S, U9-ch0, adc0

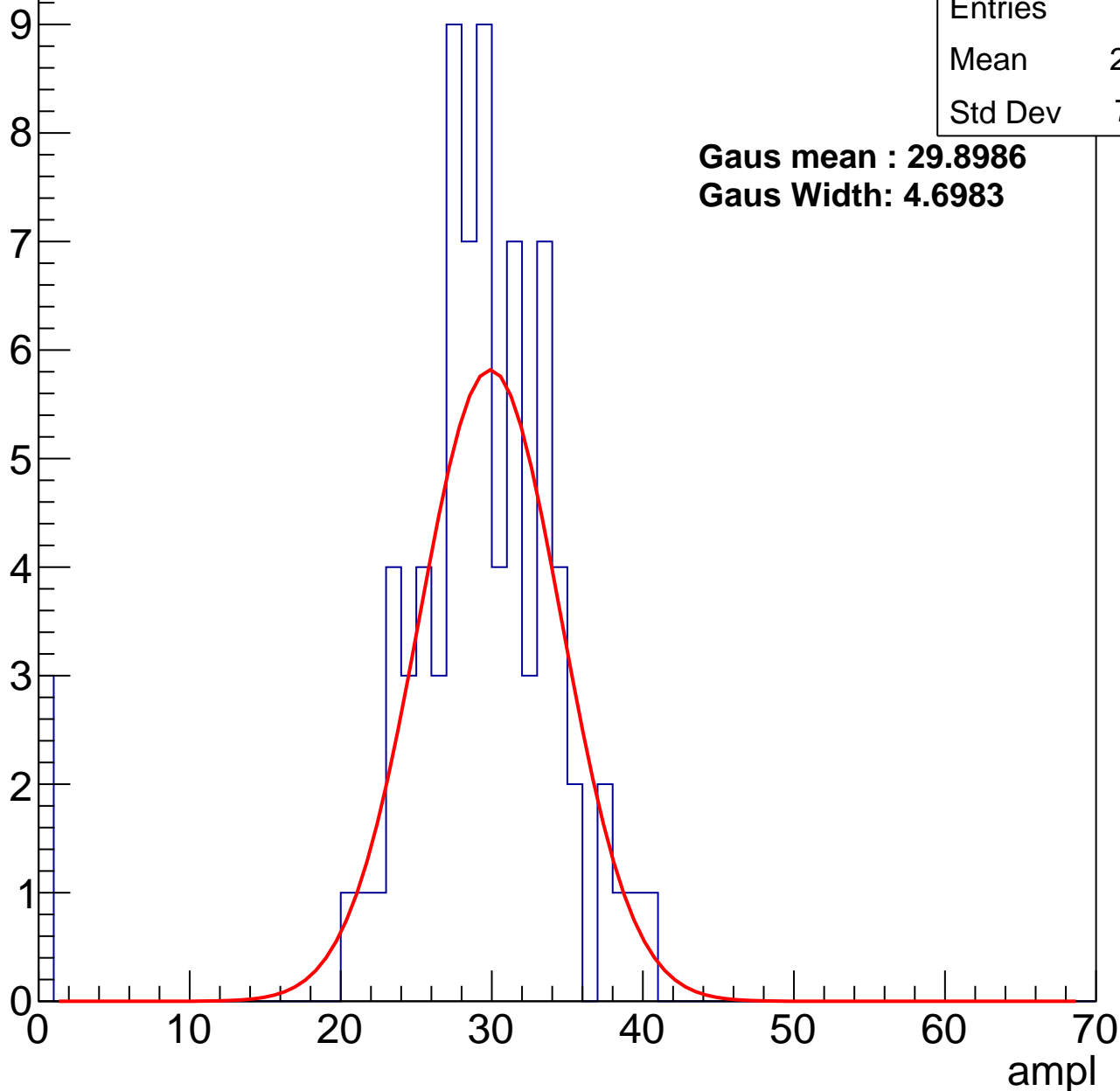
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	77
Mean	28.13
Std Dev	7.011

**Gaus mean : 29.8986**

**Gaus Width: 4.6983**



# B1L103S, U9-ch0, adc1

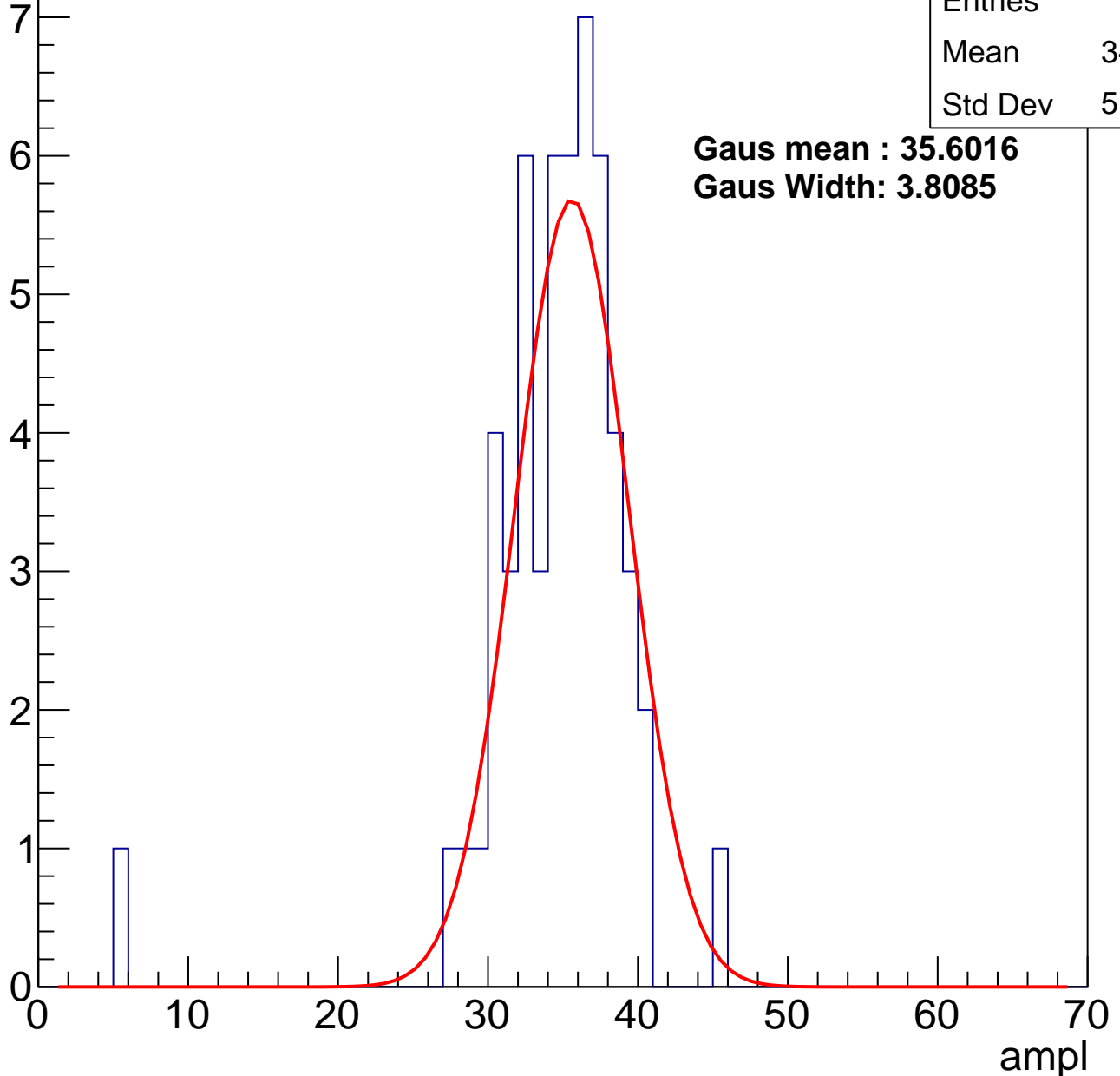
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	55
Mean	34.09
Std Dev	5.202

**Gaus mean : 35.6016**

**Gaus Width: 3.8085**



# B1L103S, U9-ch0, adc2

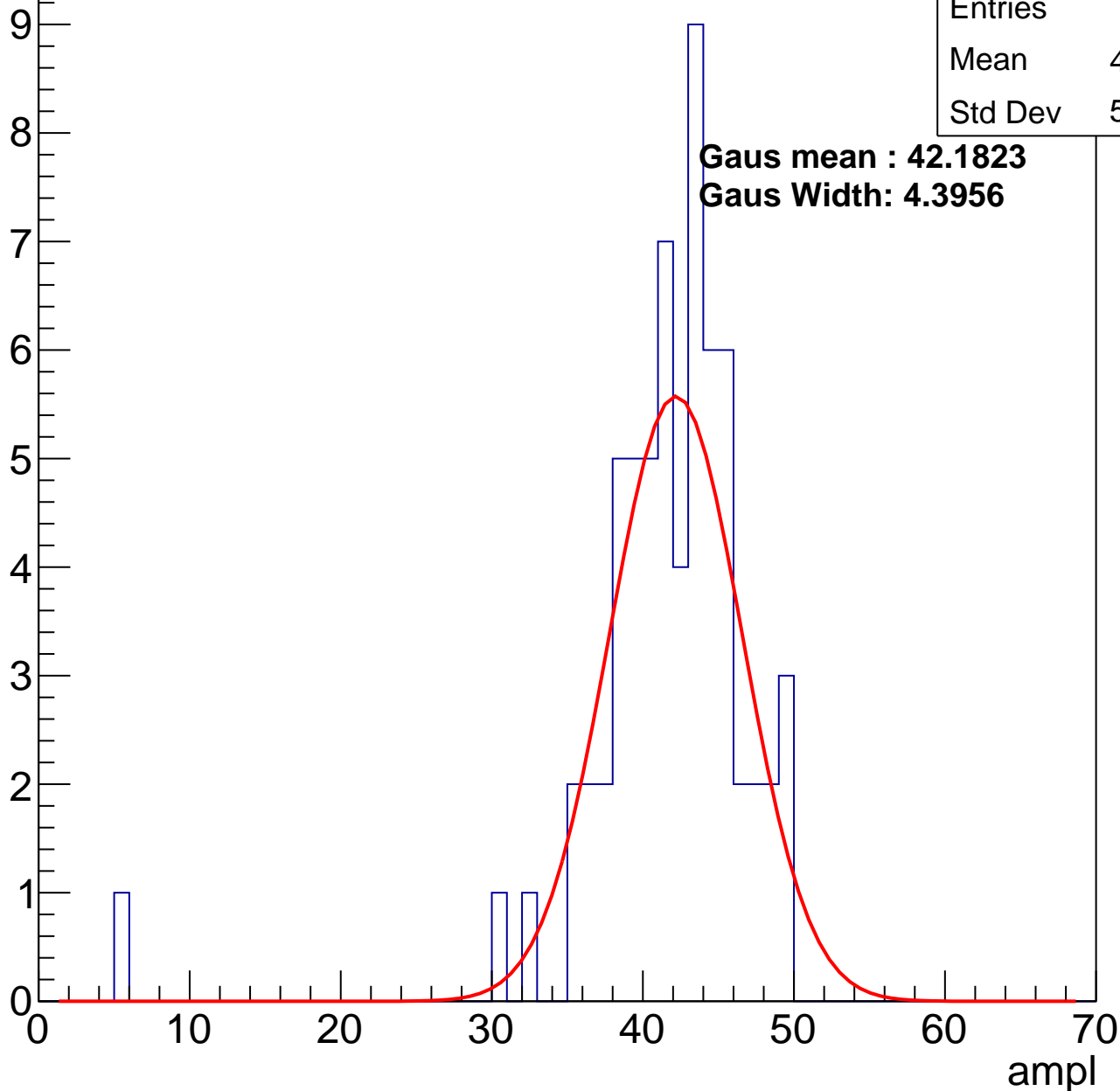
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	41.12
Std Dev	5.978

**Gaus mean : 42.1823**

**Gaus Width: 4.3956**

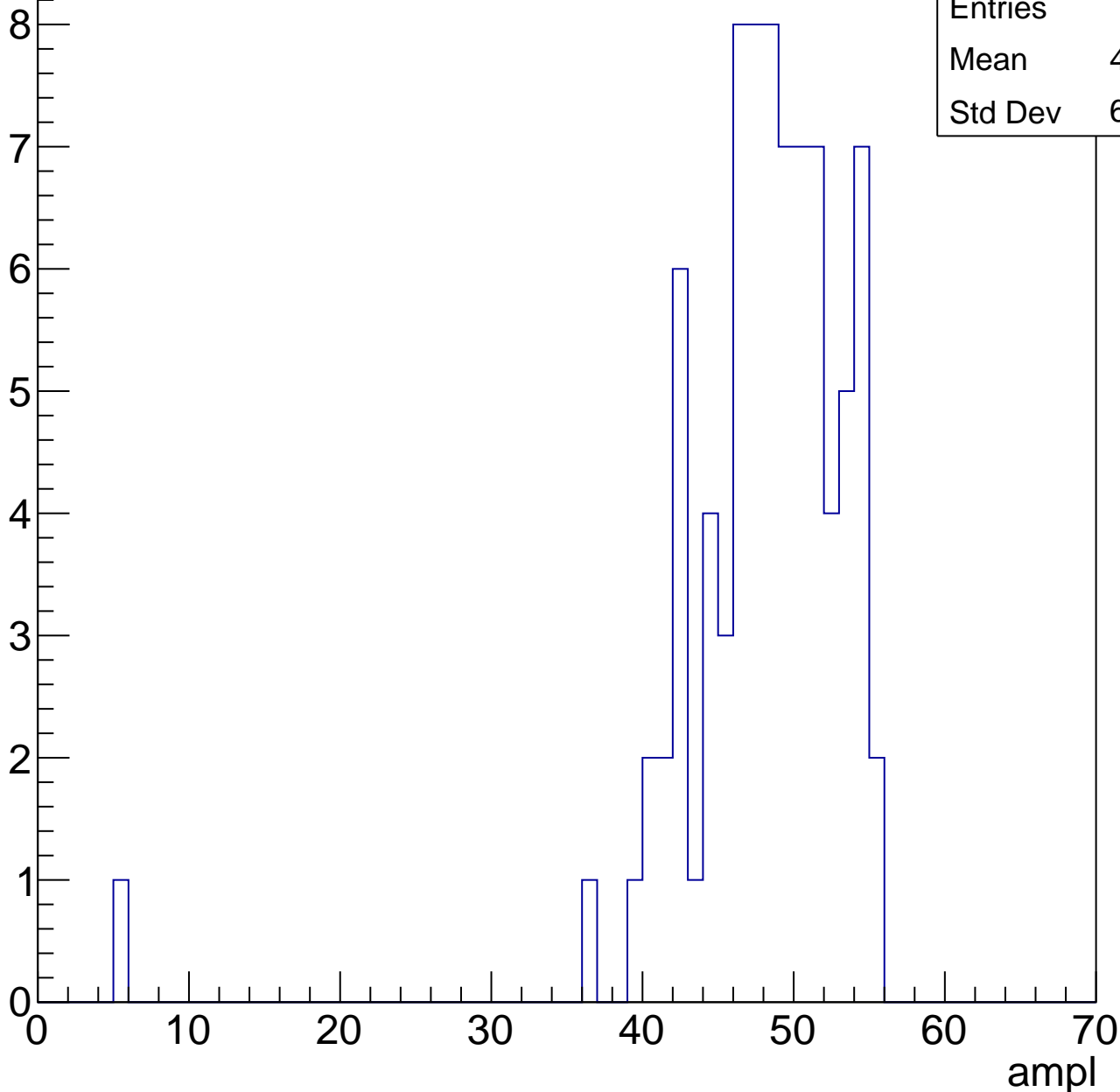


# B1L103S, U9-ch0, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	84
Mean	47.46
Std Dev	6.253

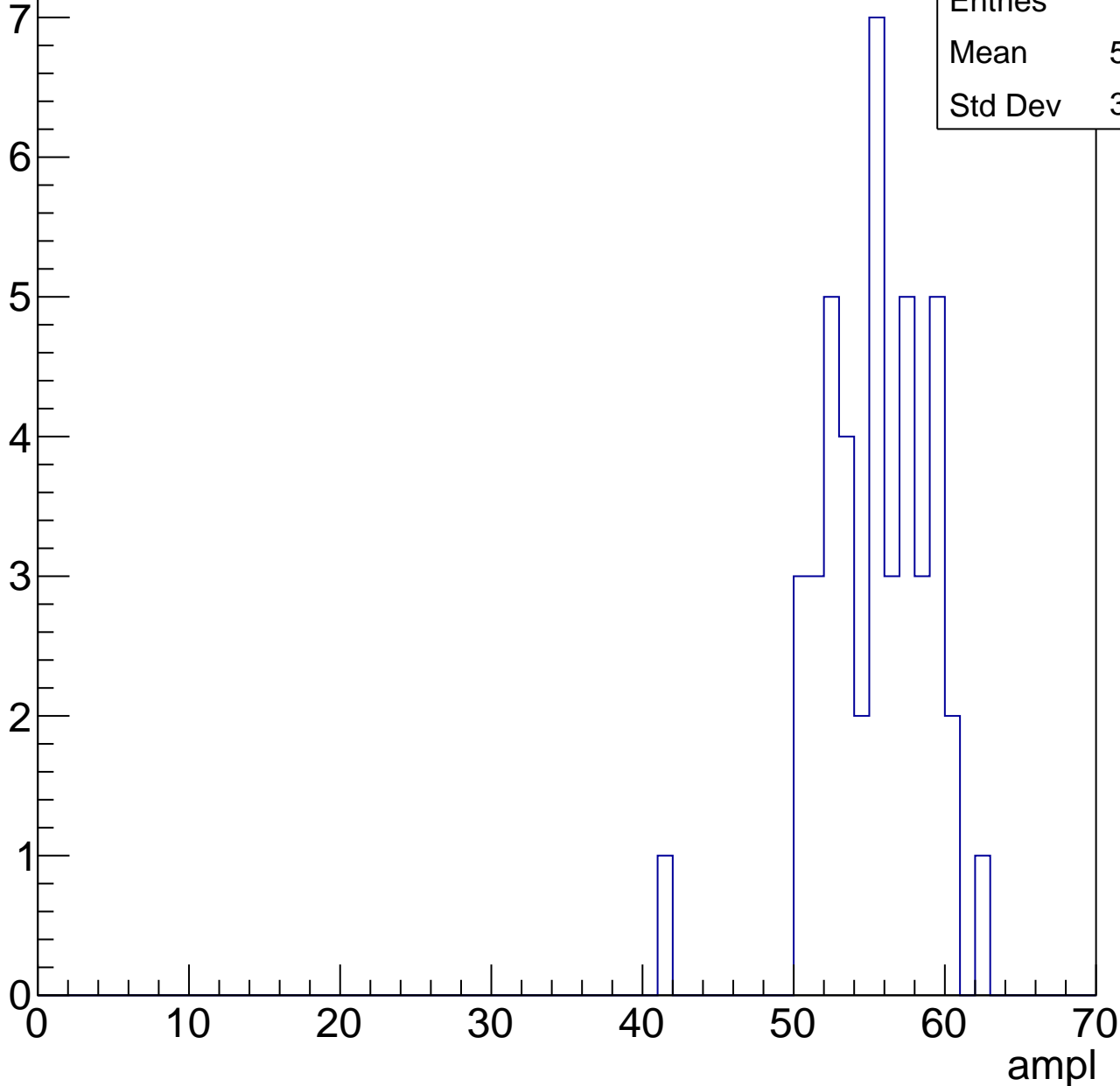


# B1L103S, U9-ch0, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	44
Mean	54.84
Std Dev	3.723

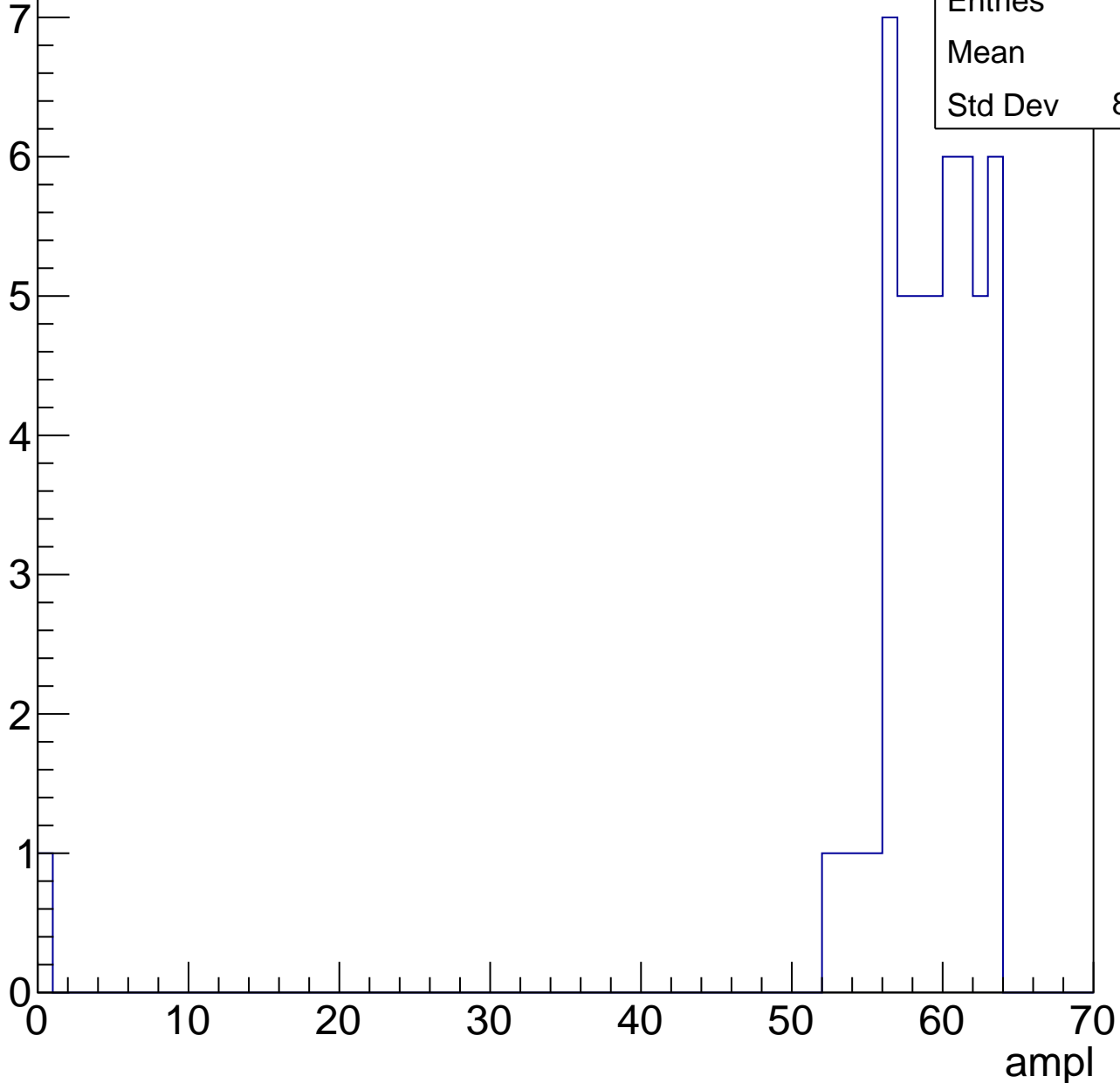


# B1L103S, U9-ch0, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

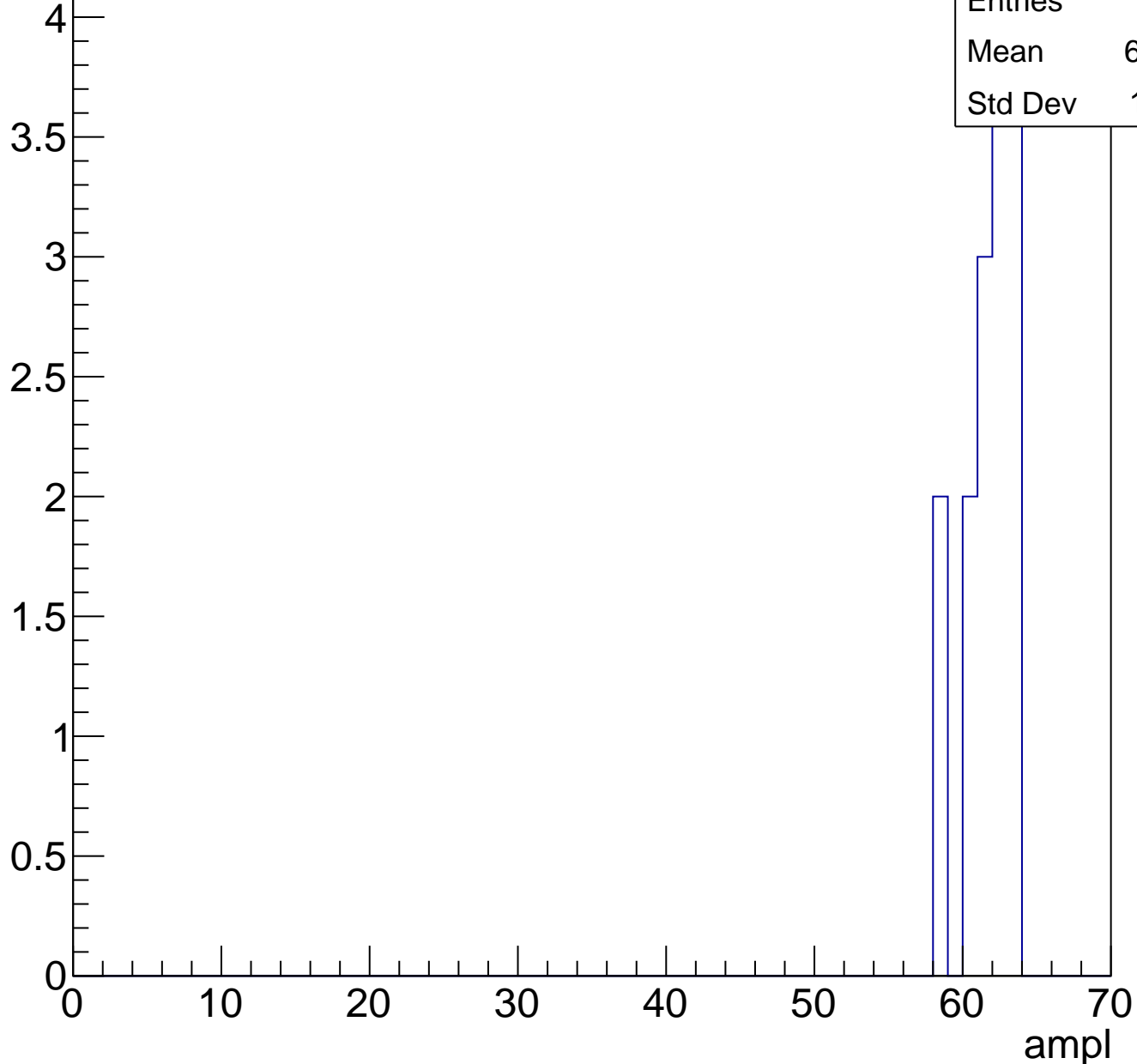
Entries	50
Mean	57.8
Std Dev	8.711



# B1L103S, U9-ch0, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

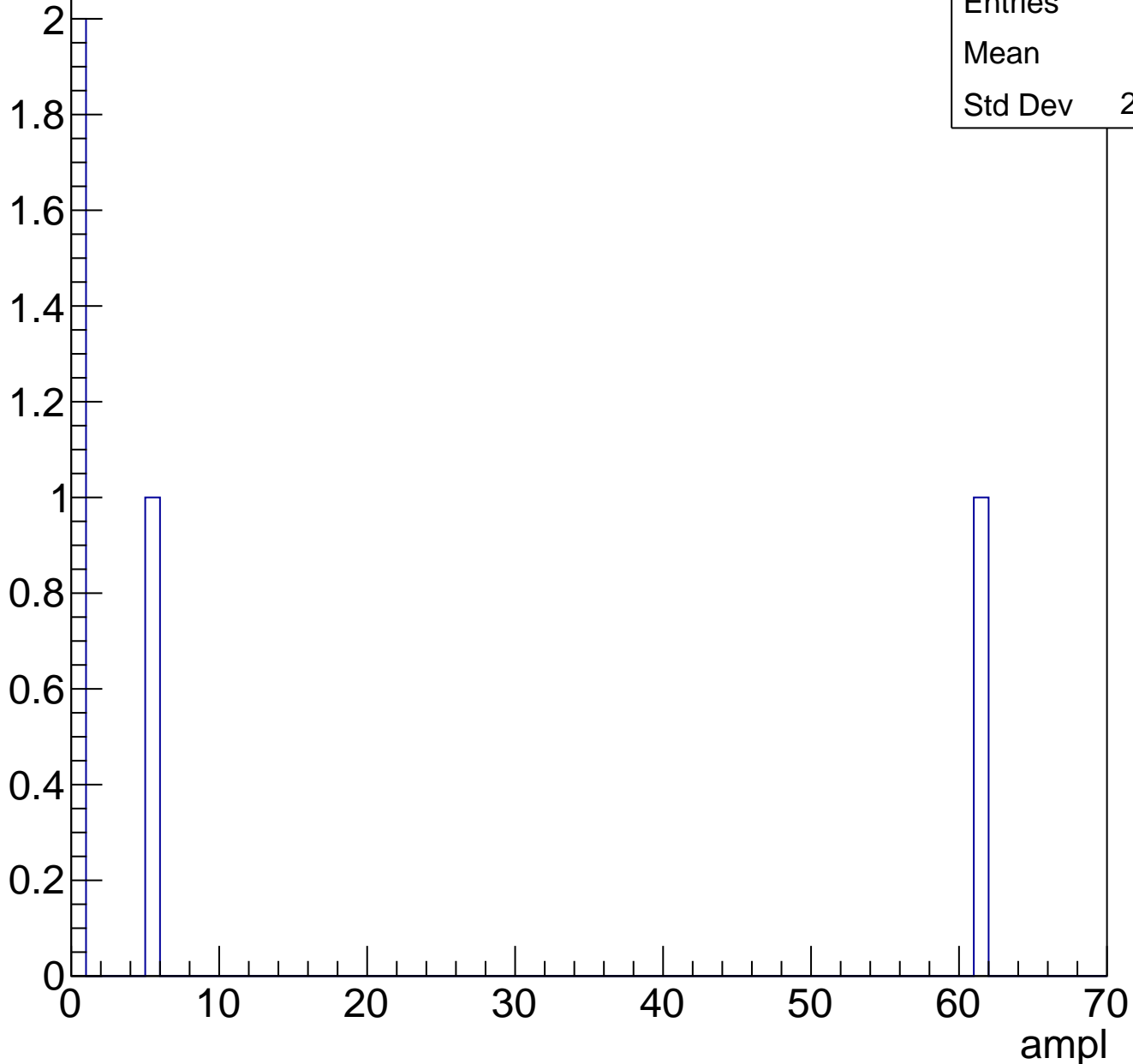




# B1L103S, U9-ch0, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	4
Mean	16.5
Std Dev	25.77

# B1L103S, U9-ch1, adc0

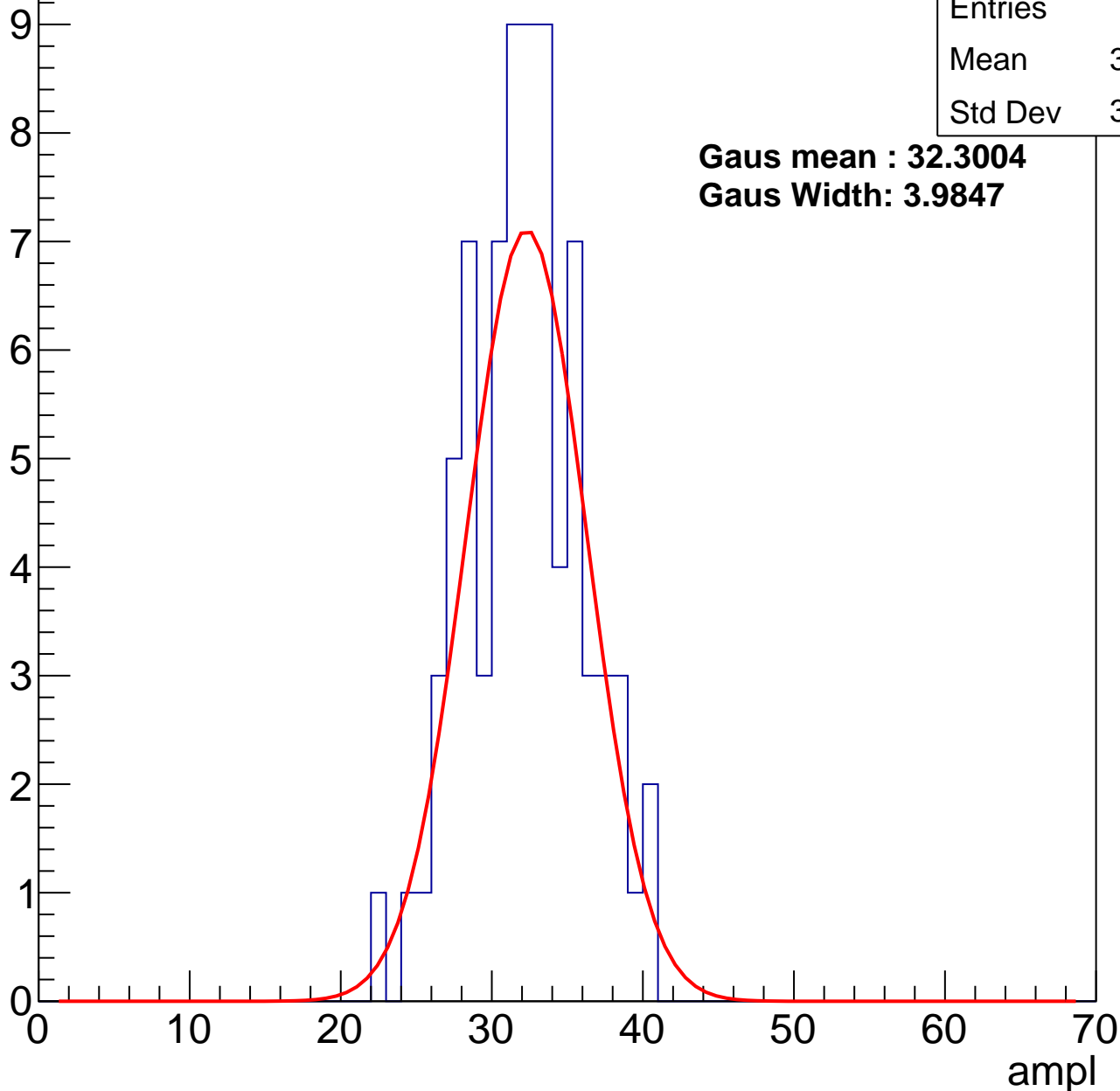
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	78
Mean	31.72
Std Dev	3.775

**Gaus mean : 32.3004**

**Gaus Width: 3.9847**



# B1L103S, U9-ch1, adc1

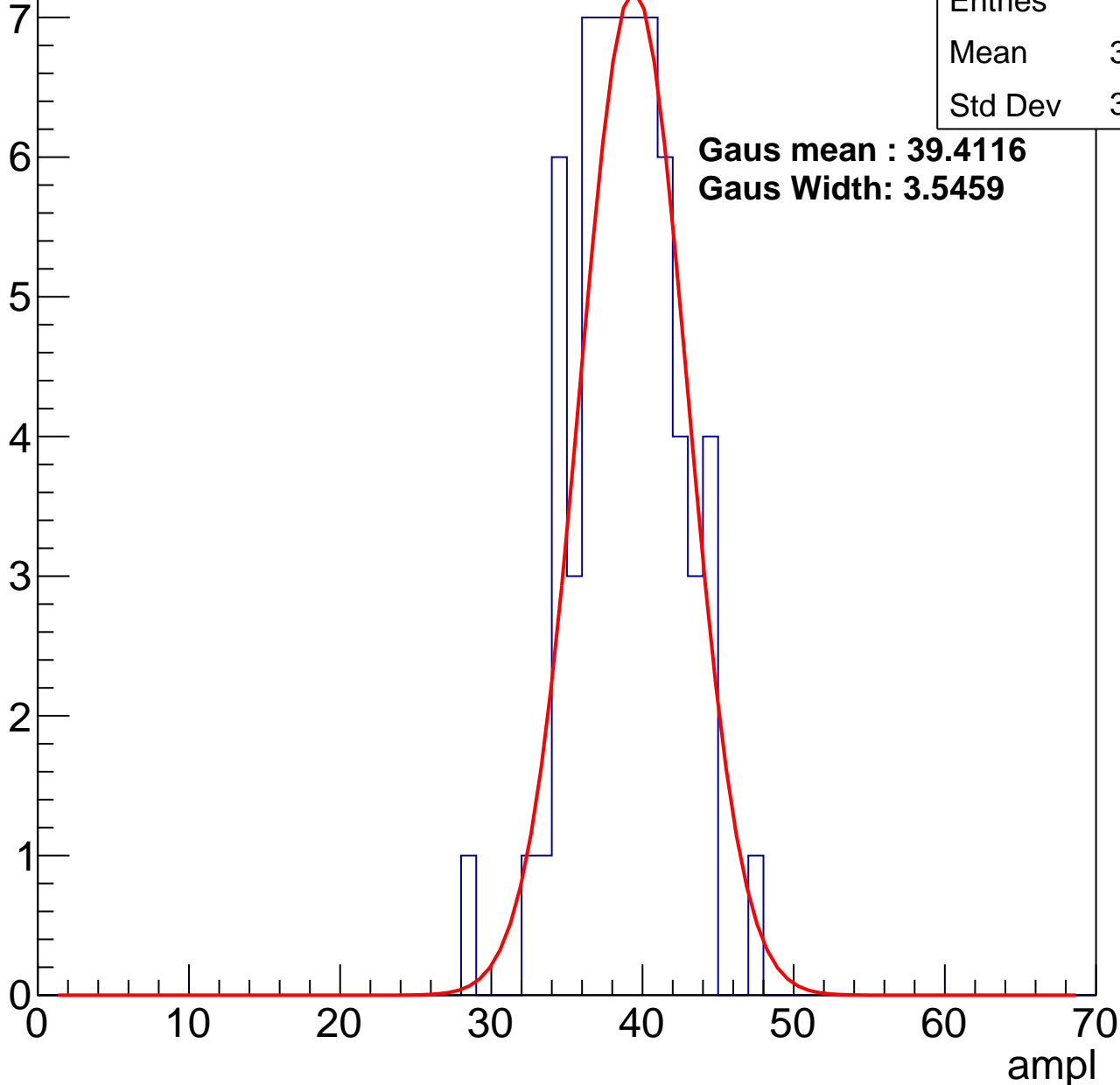
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	38.43
Std Dev	3.419

**Gaus mean : 39.4116**

**Gaus Width: 3.5459**



# B1L103S, U9-ch1, adc2

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	63
Mean	44.97
Std Dev	2.708

**Gaus mean : 45.4858**

**Gaus Width: 2.8568**

Entry

10

8

6

4

2

0

0

10

20

30

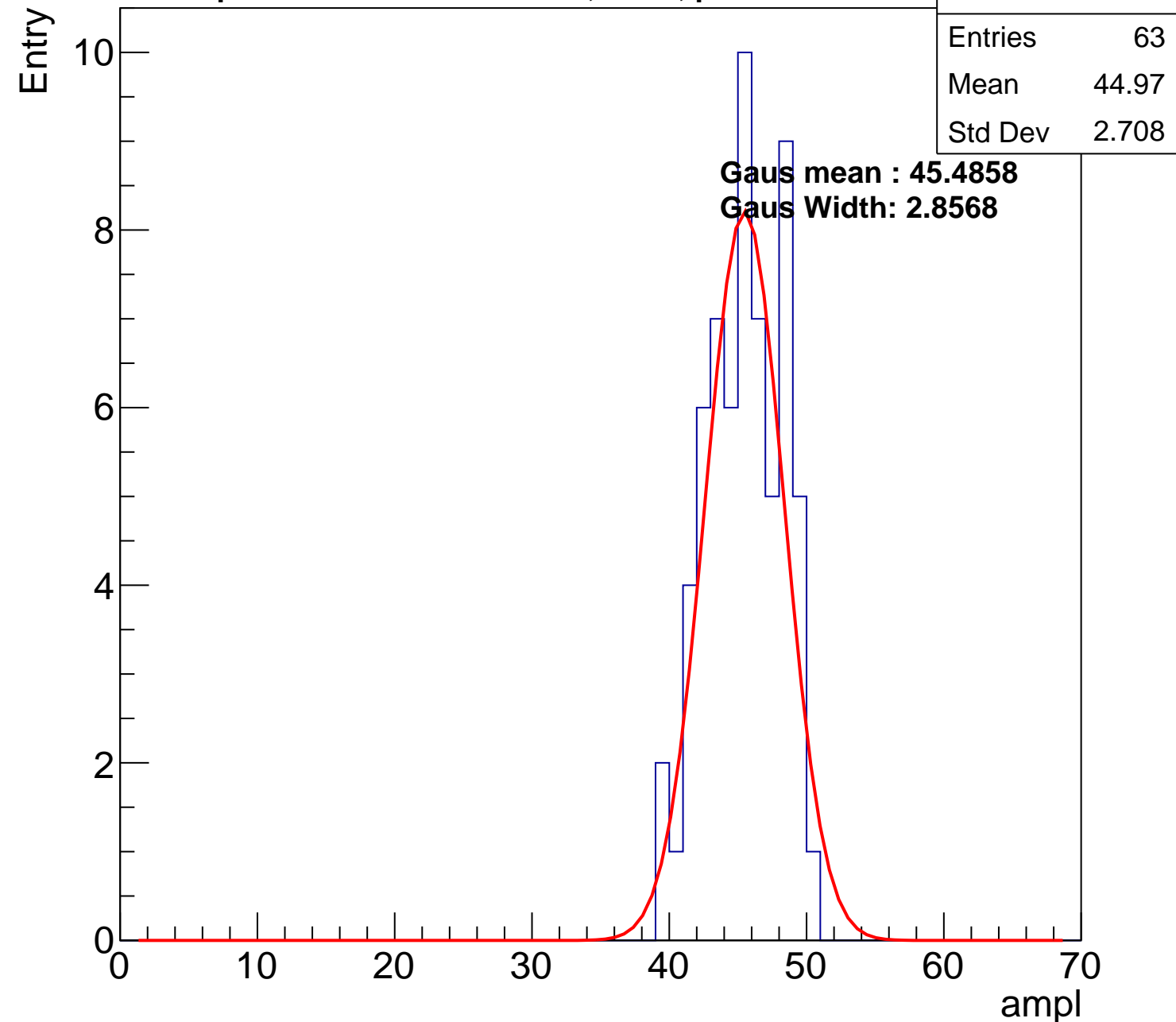
40

50

60

70

ampl

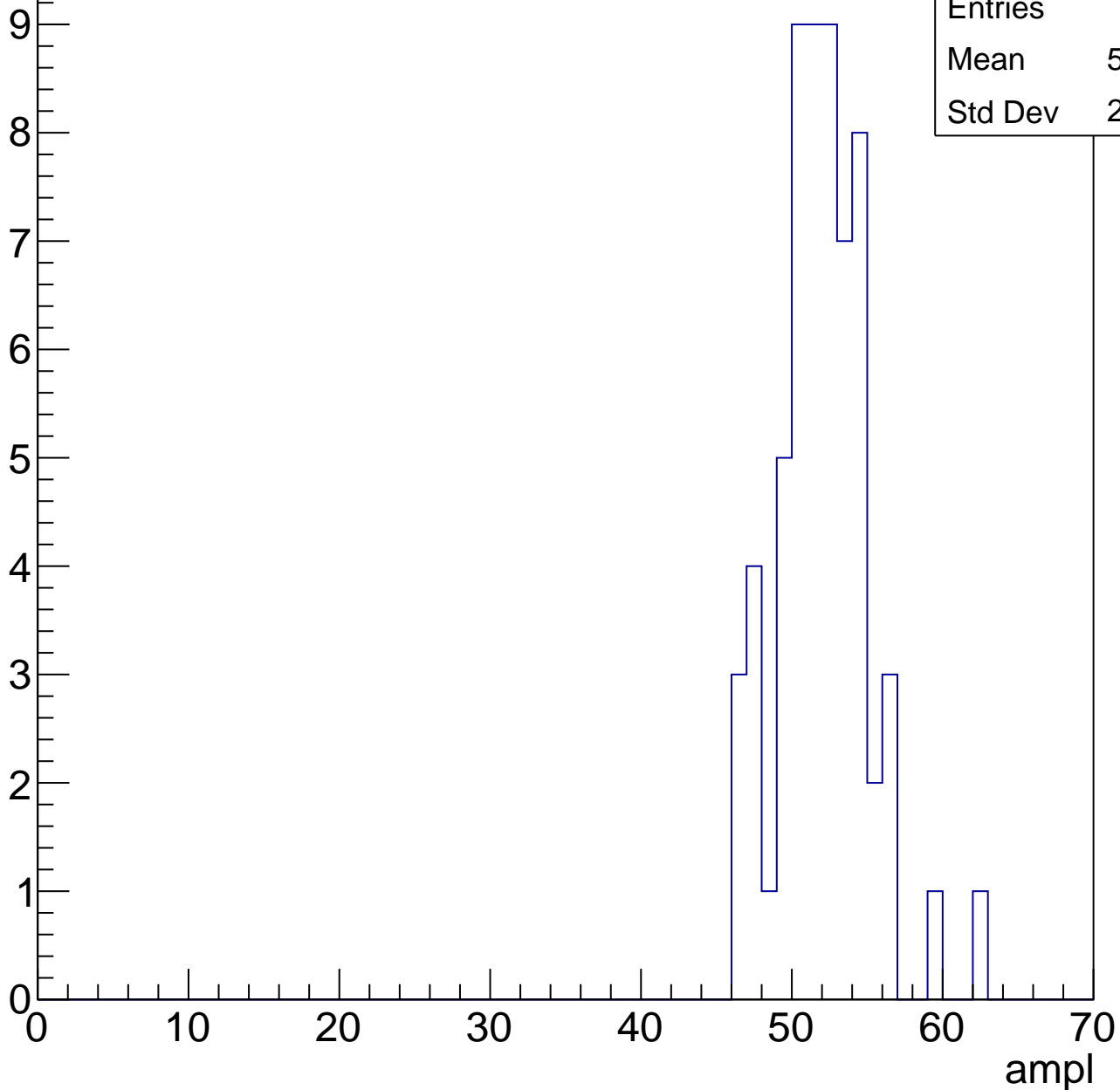


# B1L103S, U9-ch1, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

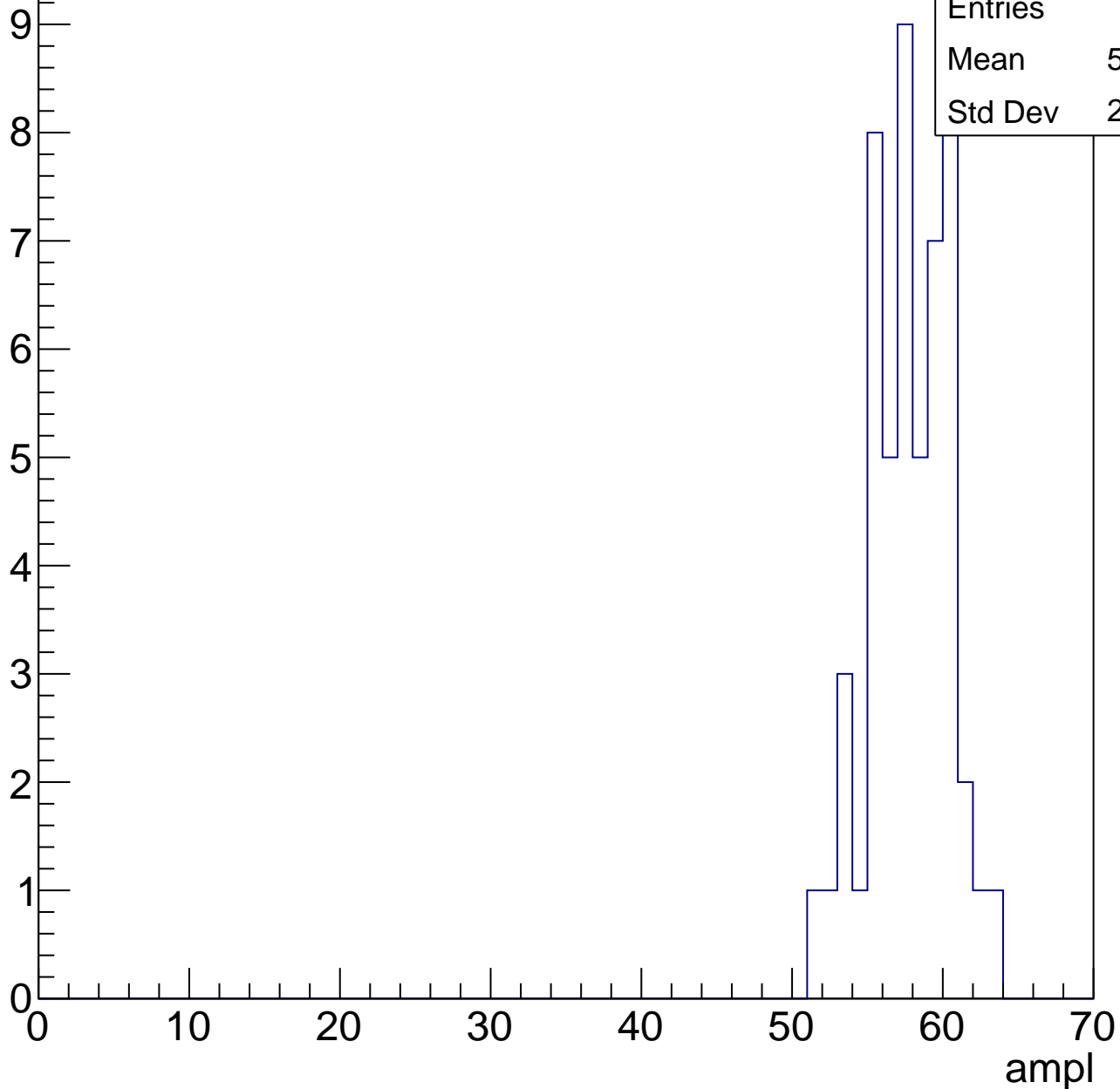
Entries	62
Mean	51.58
Std Dev	2.998



# B1L103S, U9-ch1, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

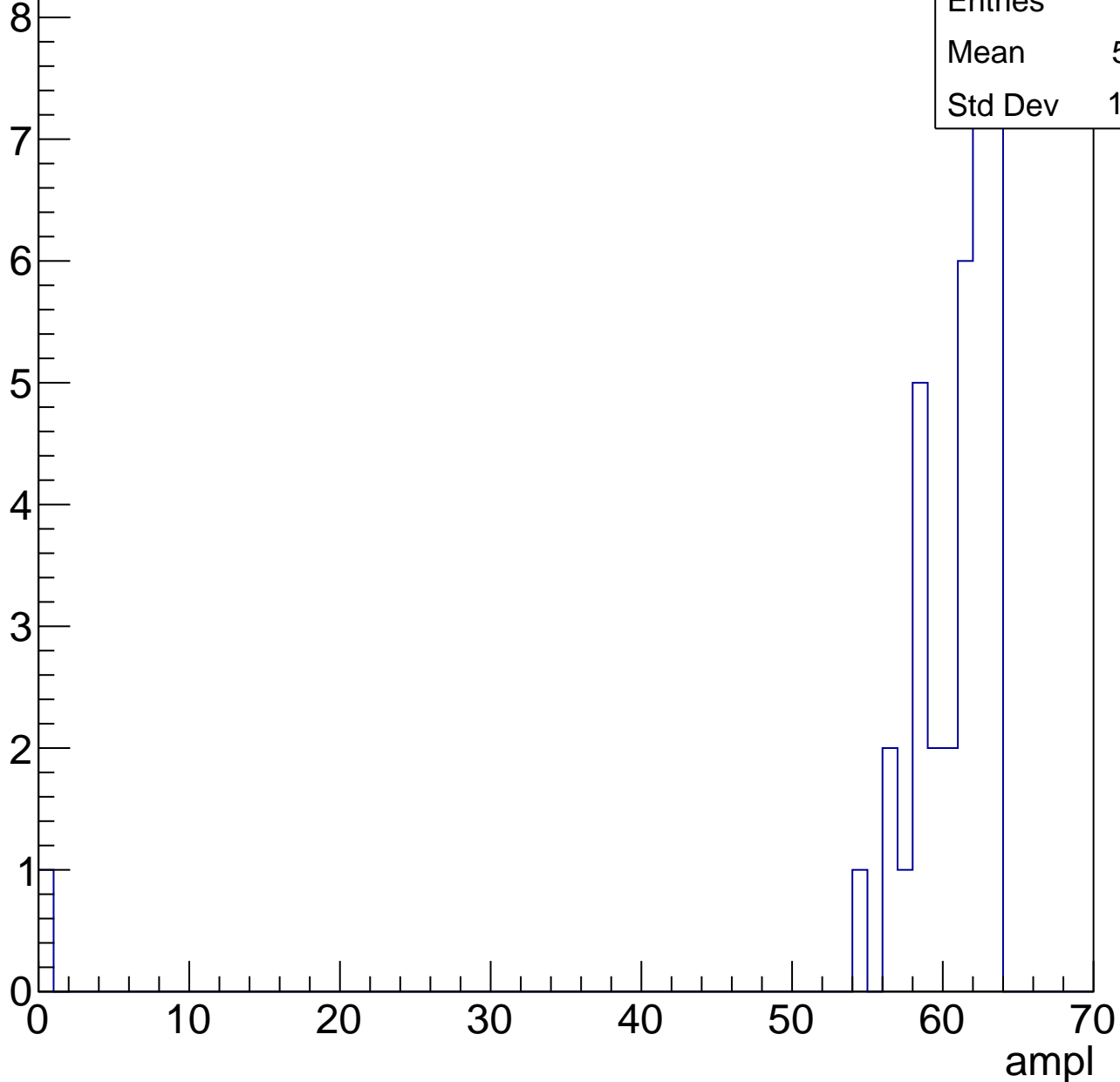


# B1L103S, U9-ch1, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	36
Mean	58.81
Std Dev	10.22



# B1L103S, U9-ch1, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	3
Mean	61.67
Std Dev	0.9428



# B1L103S, U9-ch1, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U9-ch2, adc0

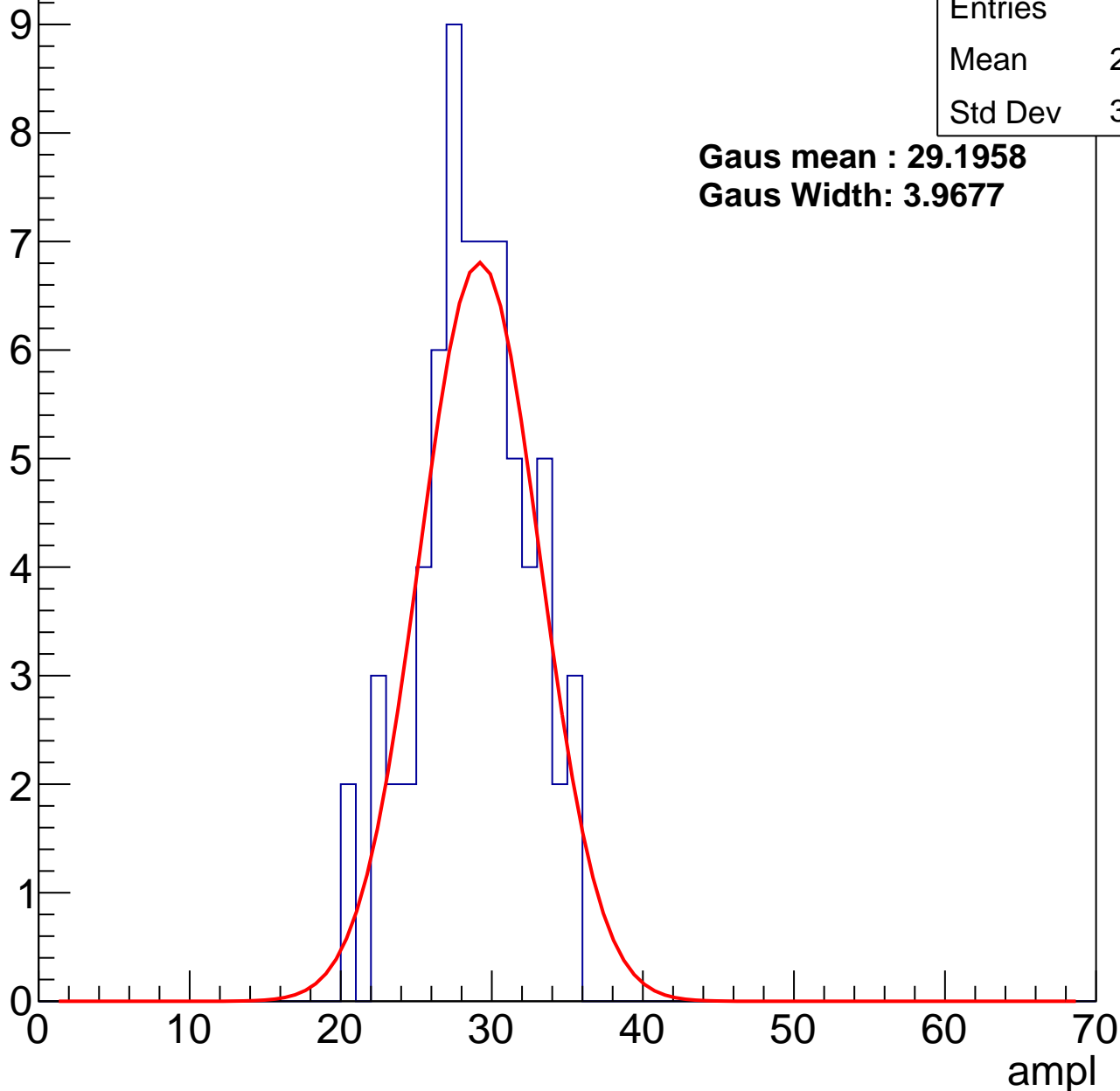
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	68
Mean	28.37
Std Dev	3.568

**Gaus mean : 29.1958**

**Gaus Width: 3.9677**



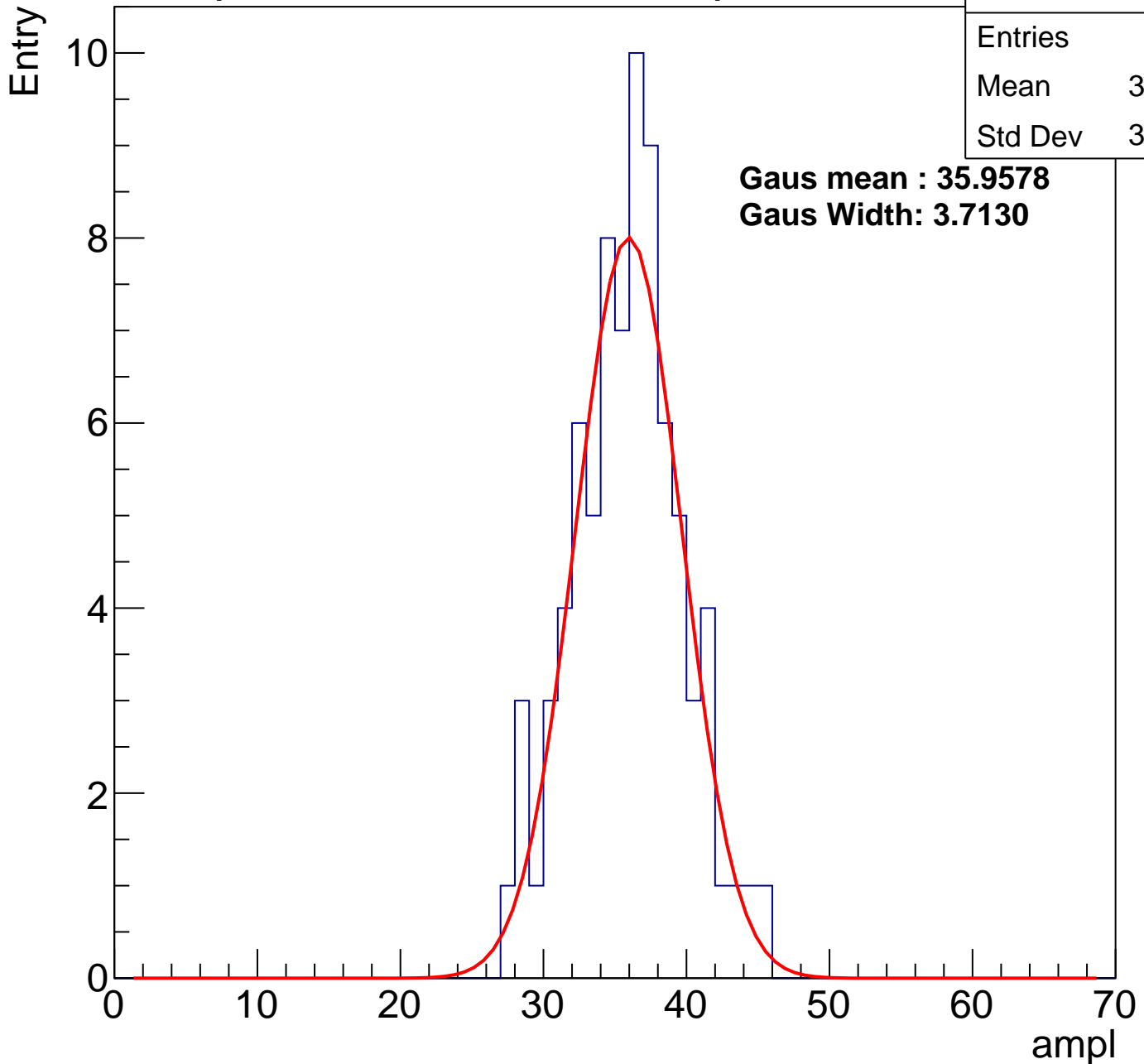
# B1L103S, U9-ch2, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	79
Mean	35.47
Std Dev	3.805

**Gaus mean : 35.9578**

**Gaus Width: 3.7130**



# B1L103S, U9-ch2, adc2

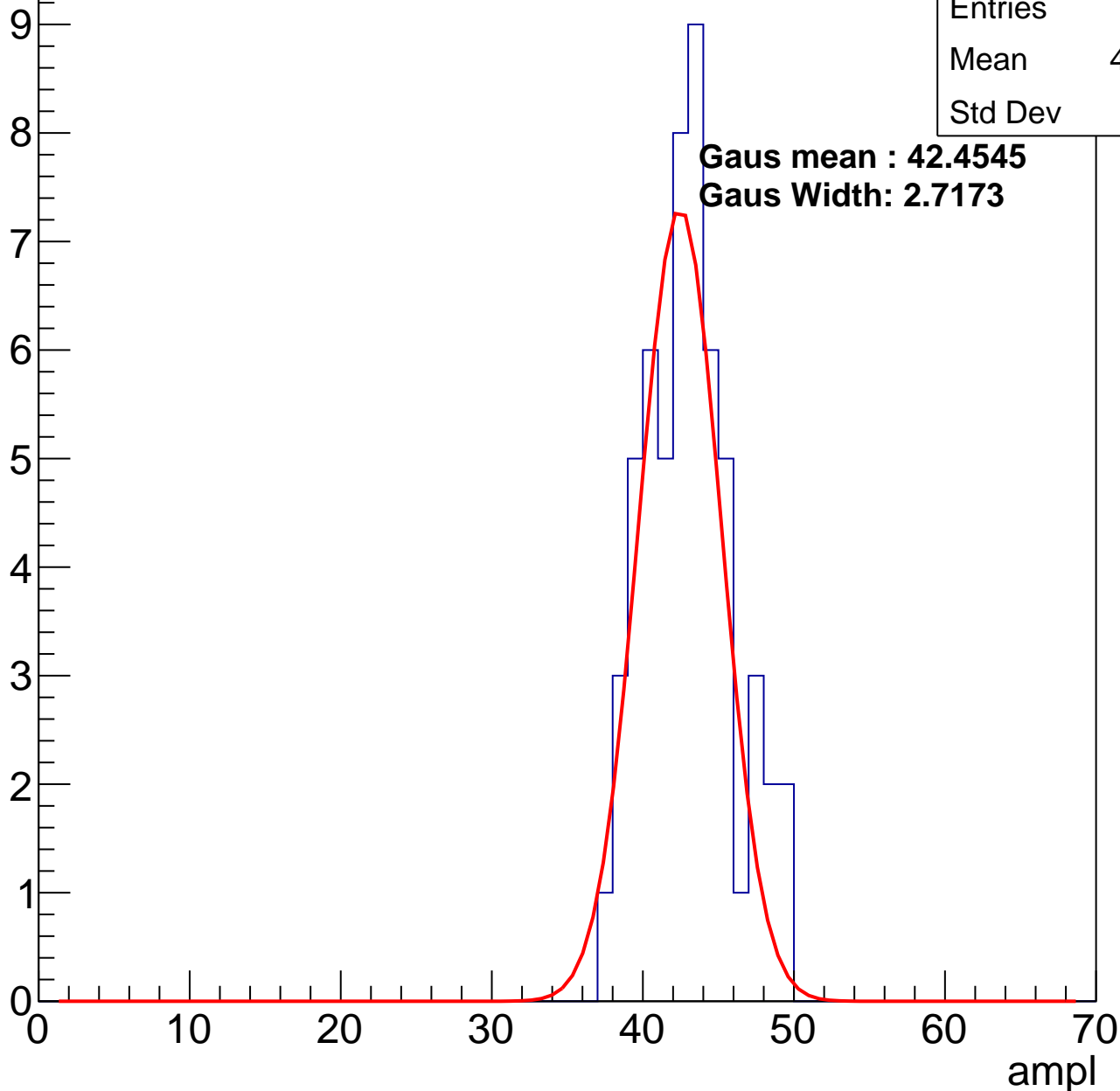
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	56
Mean	42.57
Std Dev	2.89

**Gaus mean : 42.4545**

**Gaus Width: 2.7173**

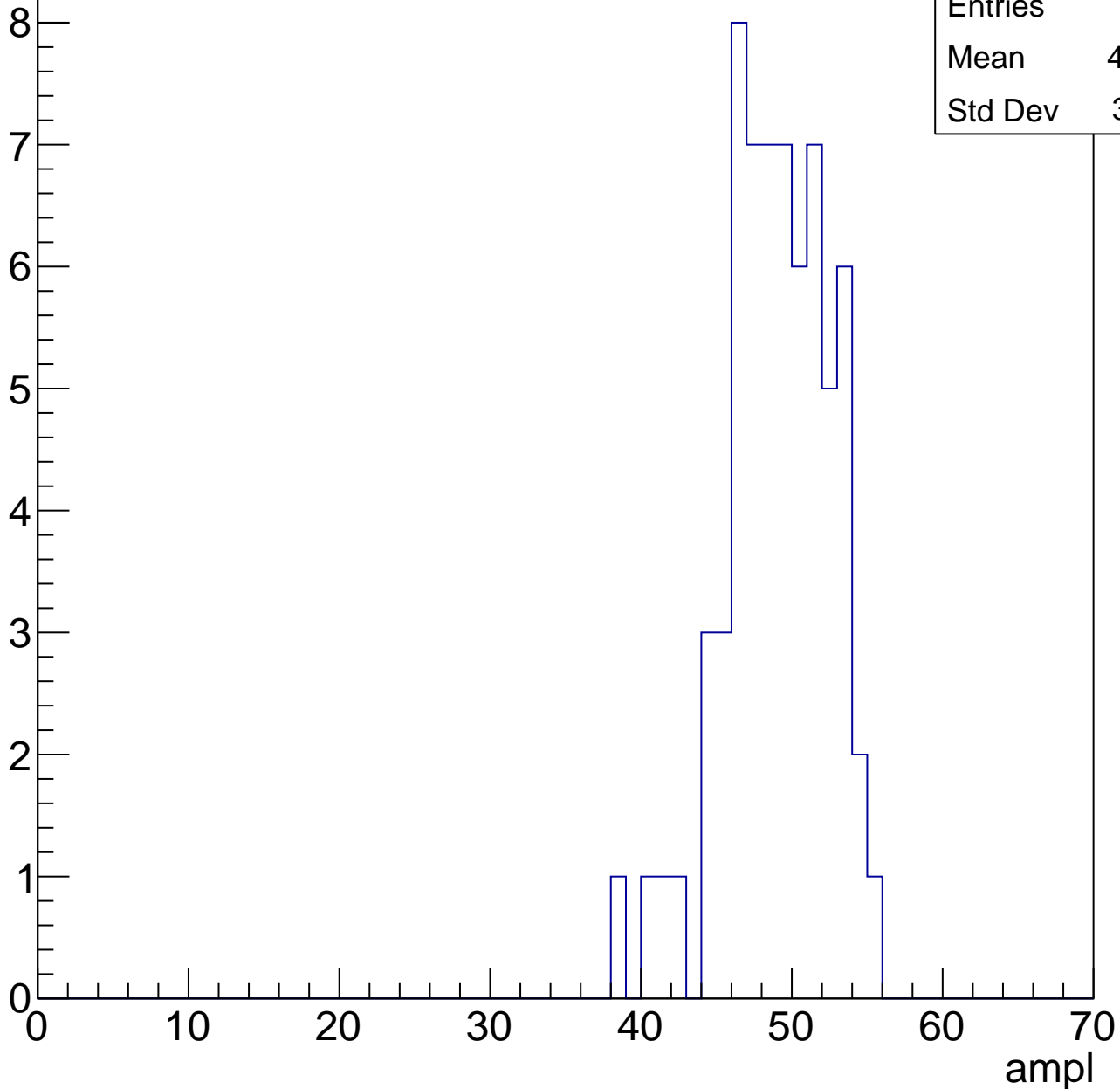


# B1L103S, U9-ch2, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	48.52
Std Dev	3.461

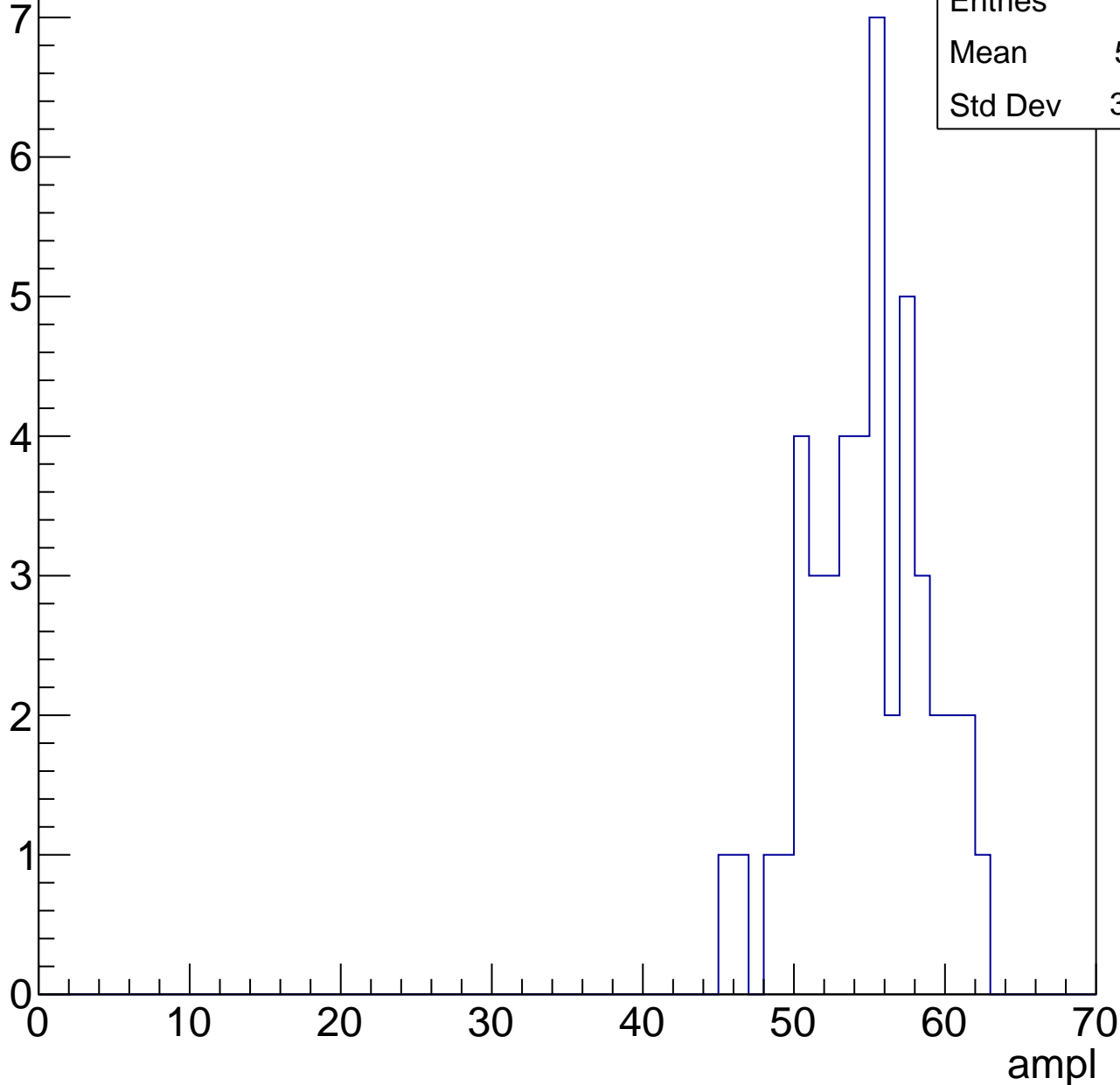


# B1L103S, U9-ch2, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	46
Mean	54.41
Std Dev	3.893

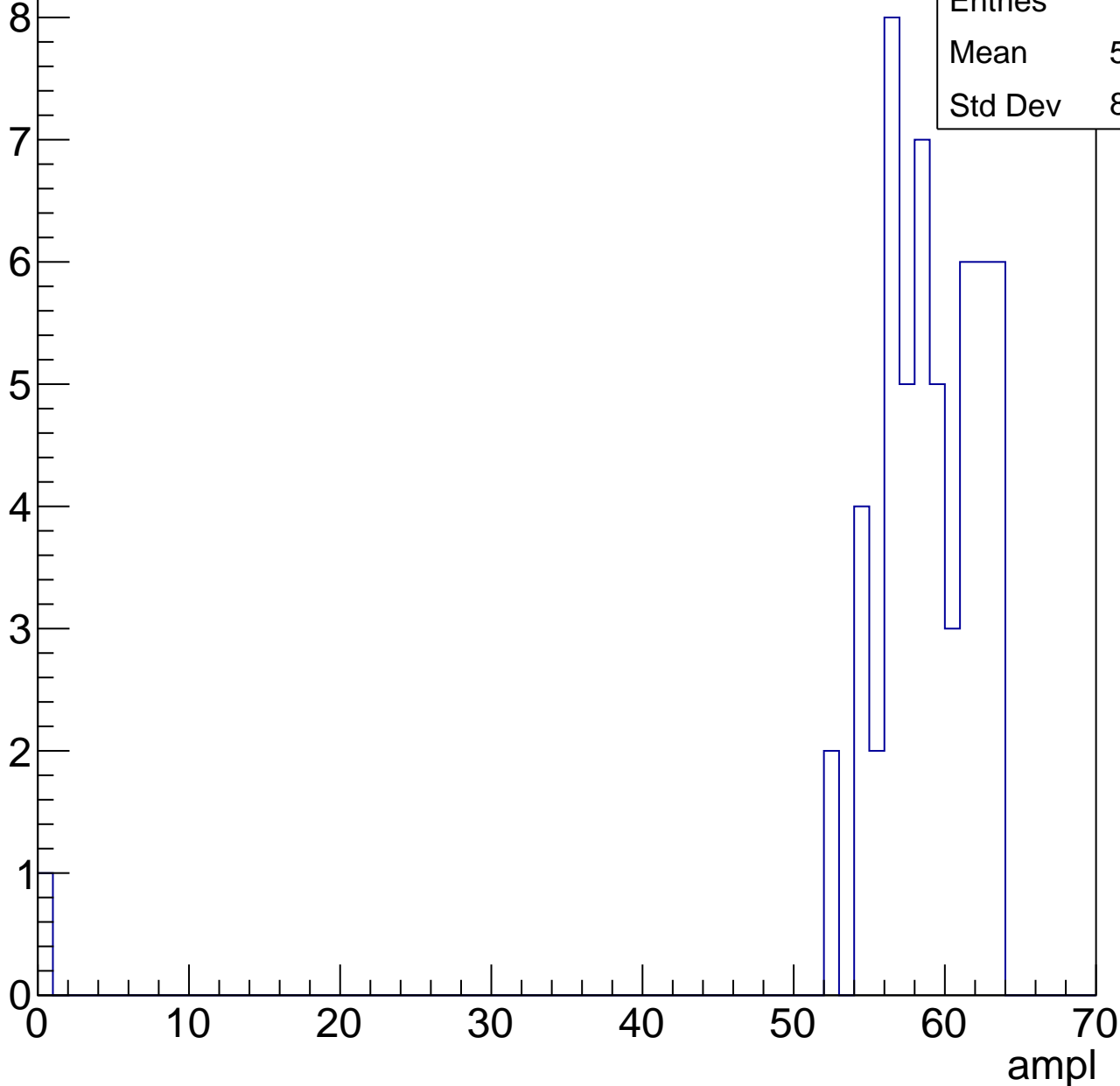


# B1L103S, U9-ch2, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

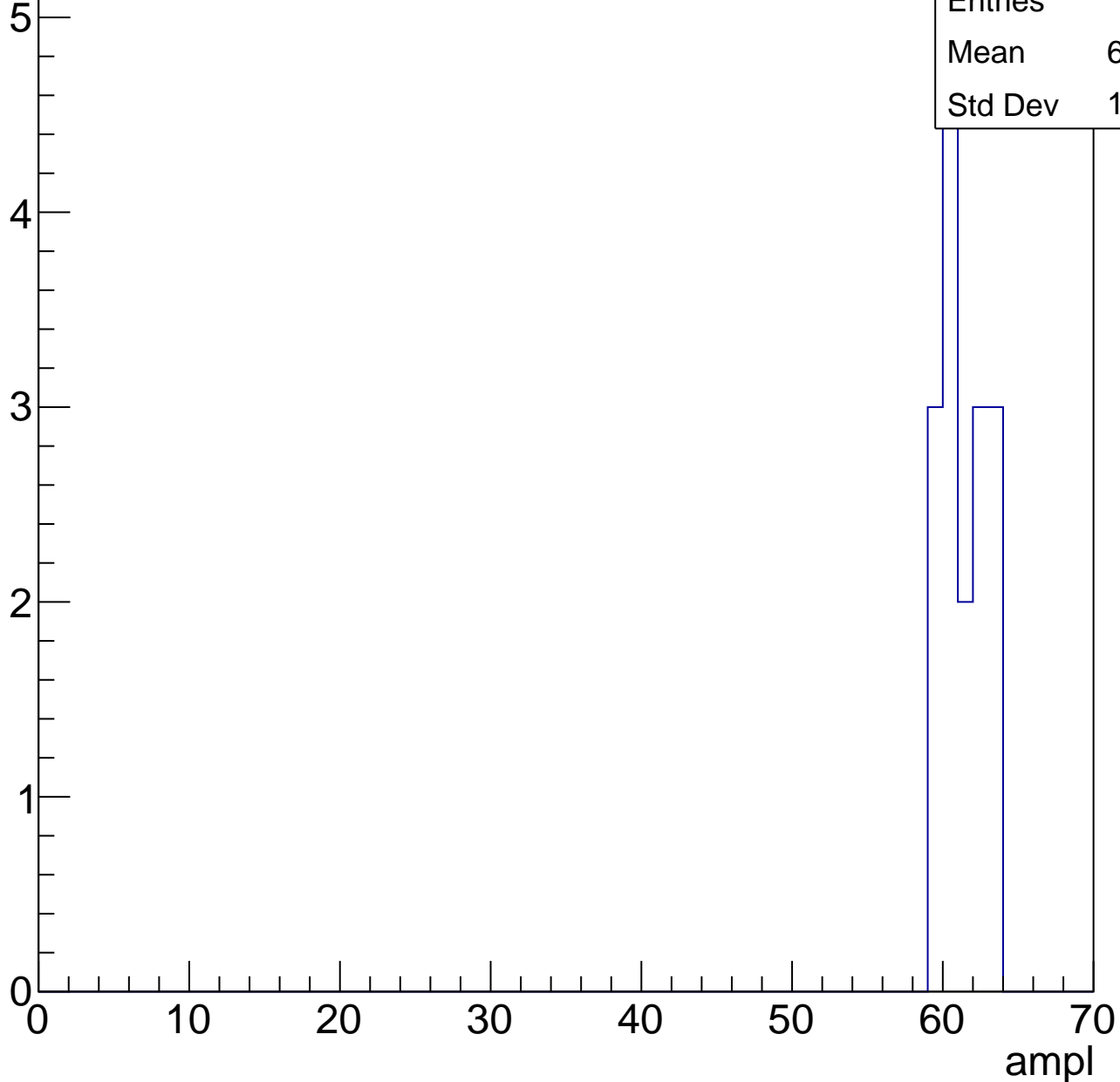
Entries	55
Mean	57.45
Std Dev	8.373



# B1L103S, U9-ch2, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	16
Mean	60.88
Std Dev	1.409



# B1L103S, U9-ch2, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

1  
0.8  
0.6  
0.4  
0.2  
0

Entries	2
Mean	40.5
Std Dev	22.5

ampl

# B1L103S, U9-ch3, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	68
Mean	30.65
Std Dev	3.373

**Gaus mean : 31.2688**

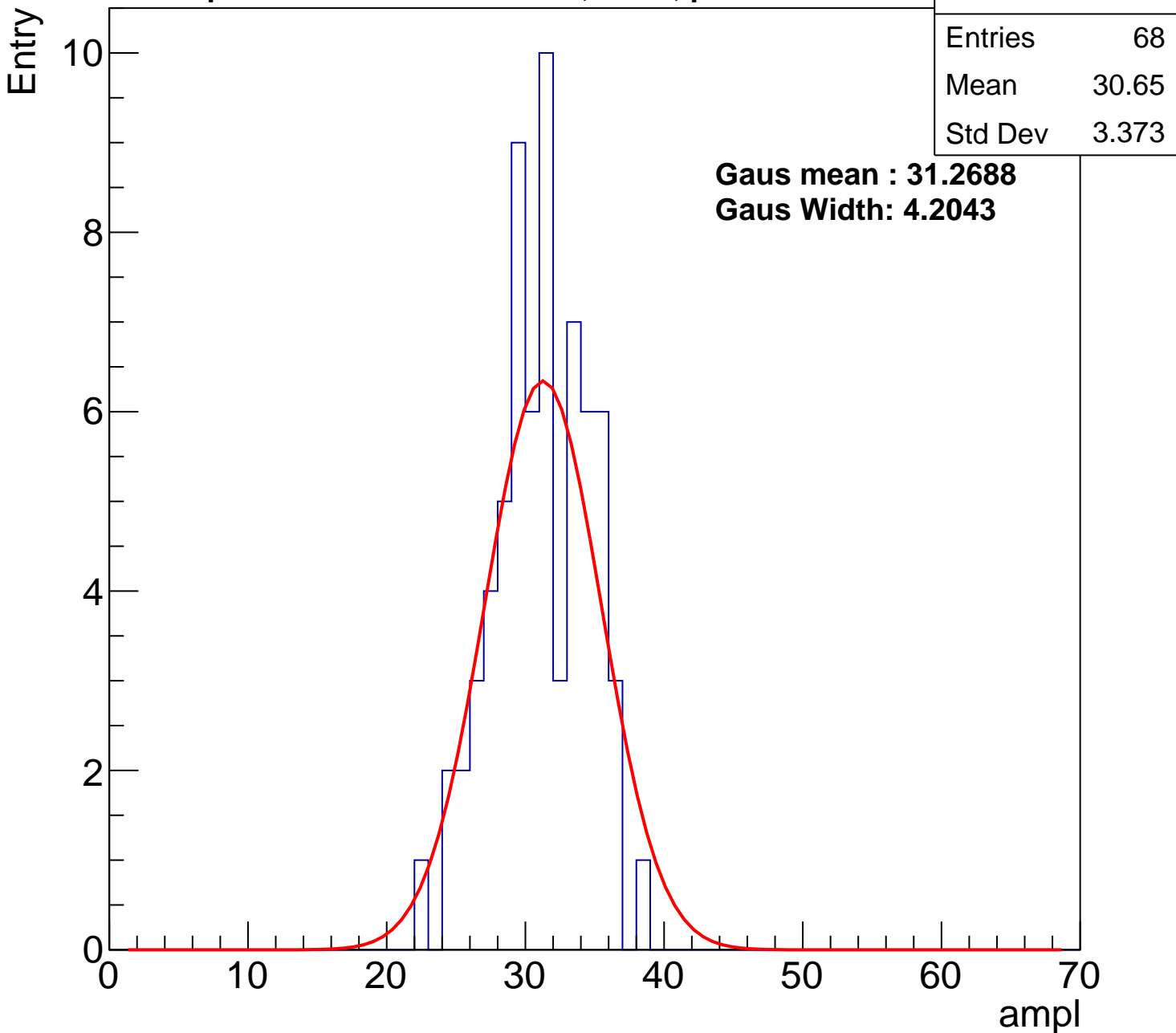
**Gaus Width: 4.2043**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U9-ch3, adc1

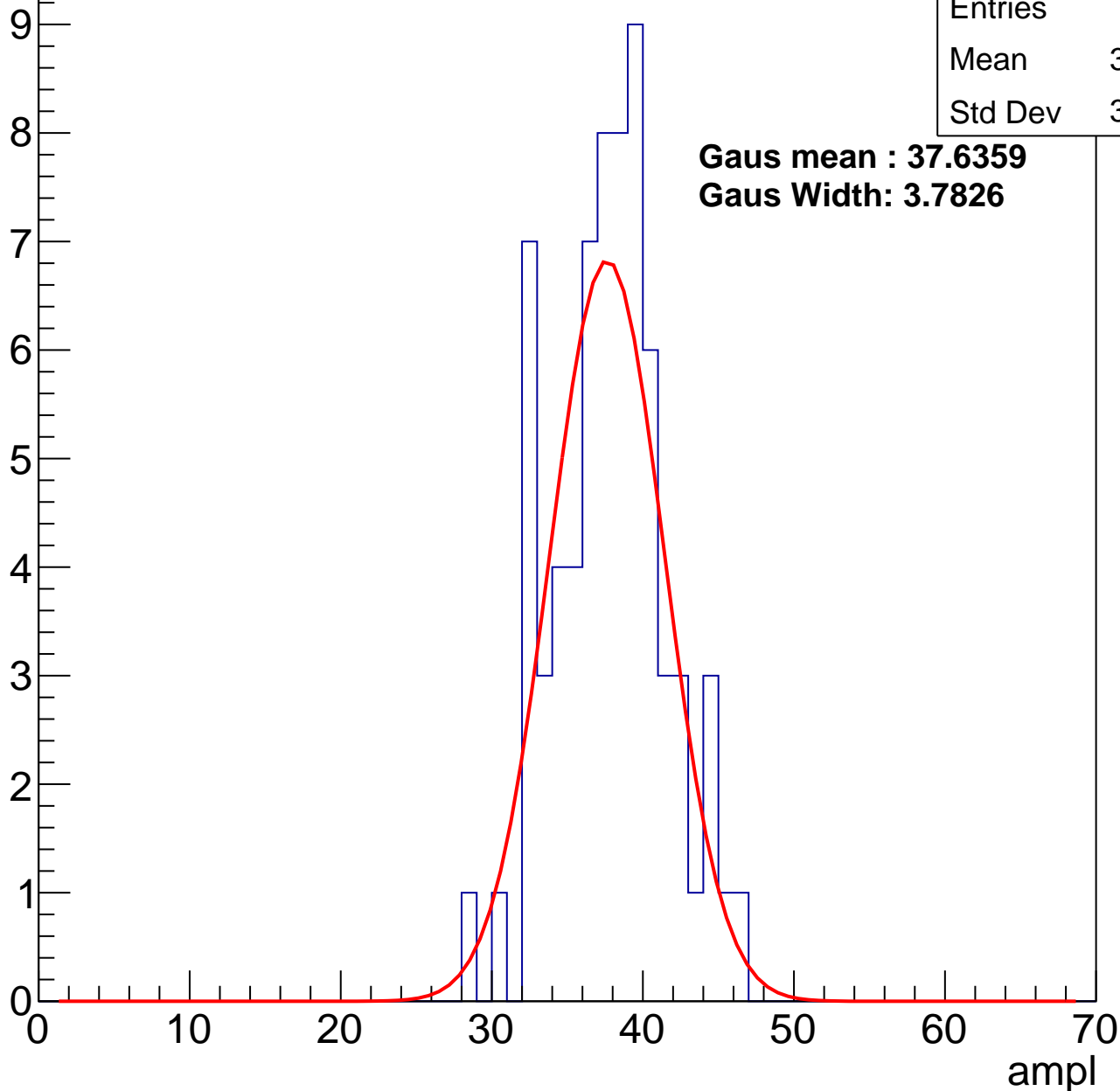
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	70
Mean	37.36
Std Dev	3.688

**Gaus mean : 37.6359**

**Gaus Width: 3.7826**



# B1L103S, U9-ch3, adc2

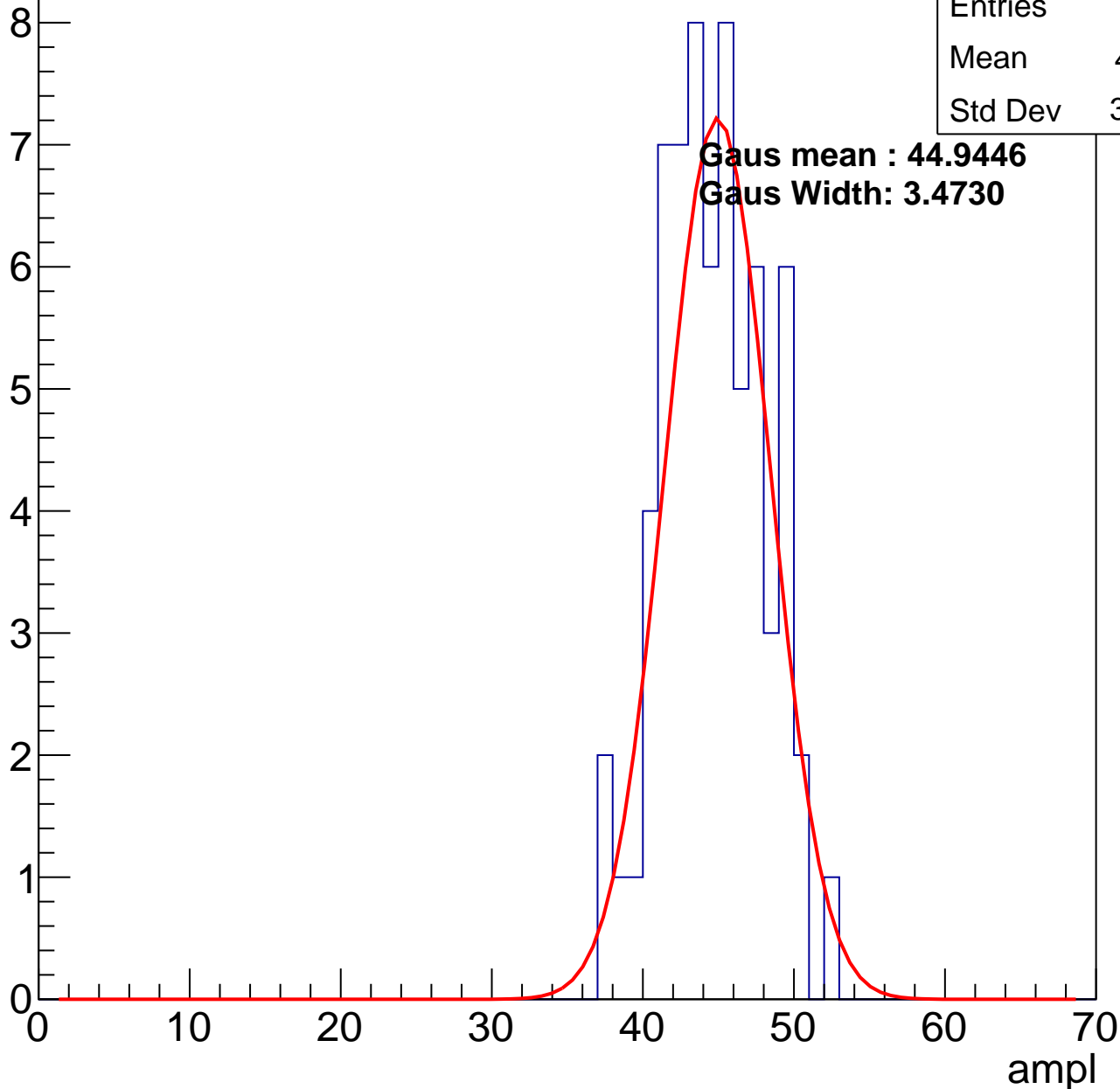
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	44.21
Std Dev	3.312

**Gaus mean : 44.9446**

**Gaus Width: 3.4730**

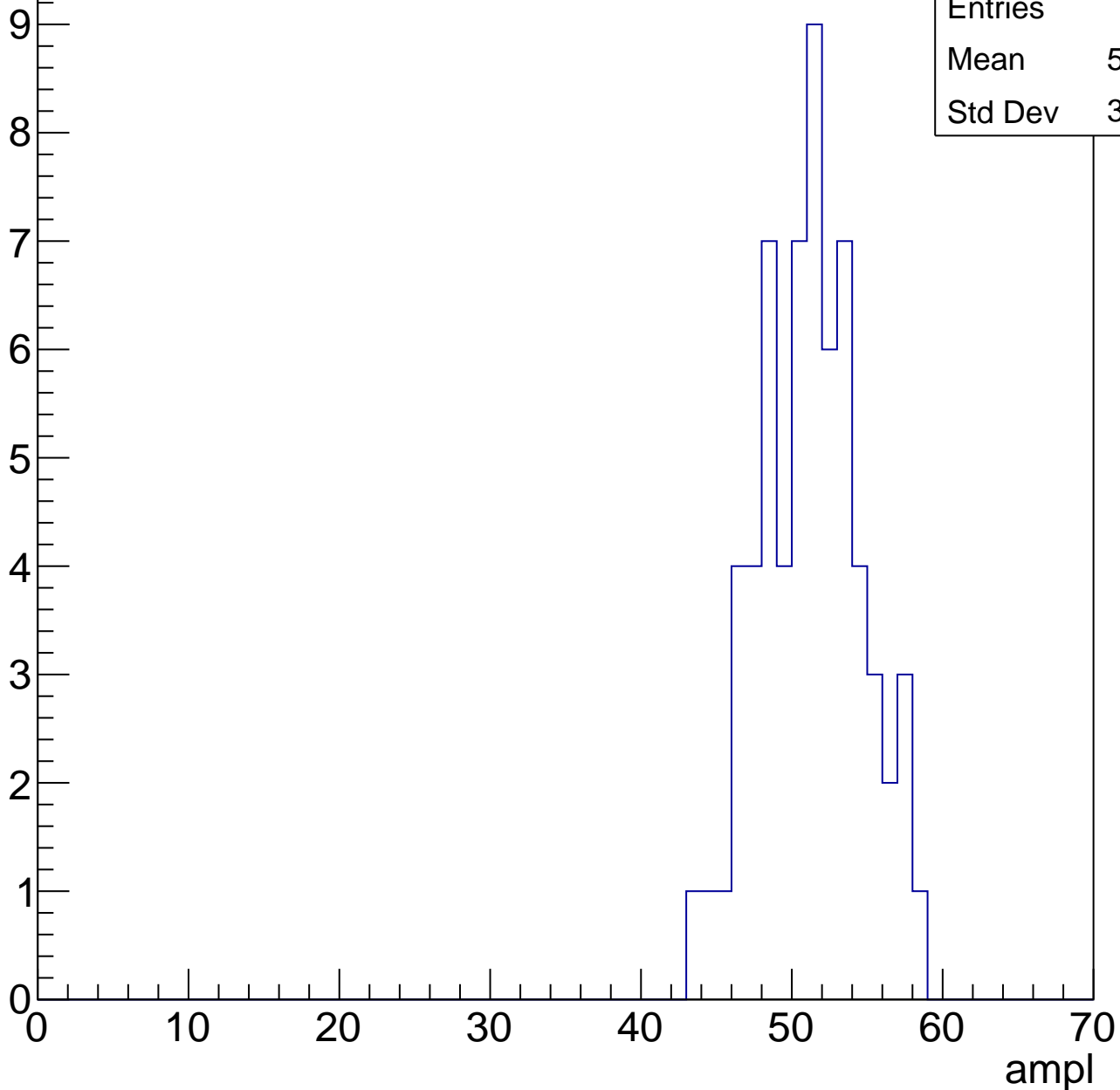


# B1L103S, U9-ch3, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

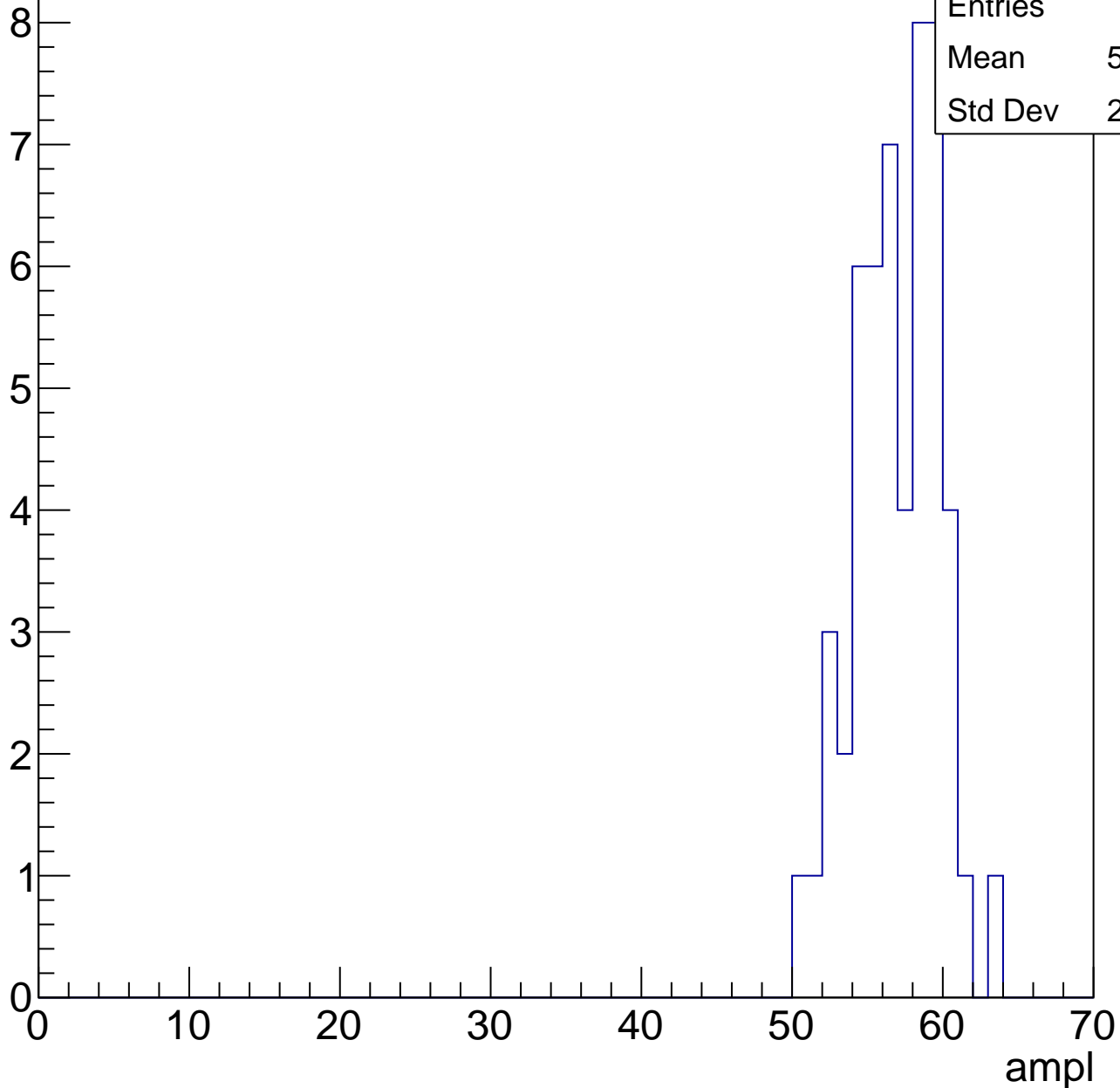
Entries	64
Mean	50.78
Std Dev	3.356



# B1L103S, U9-ch3, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

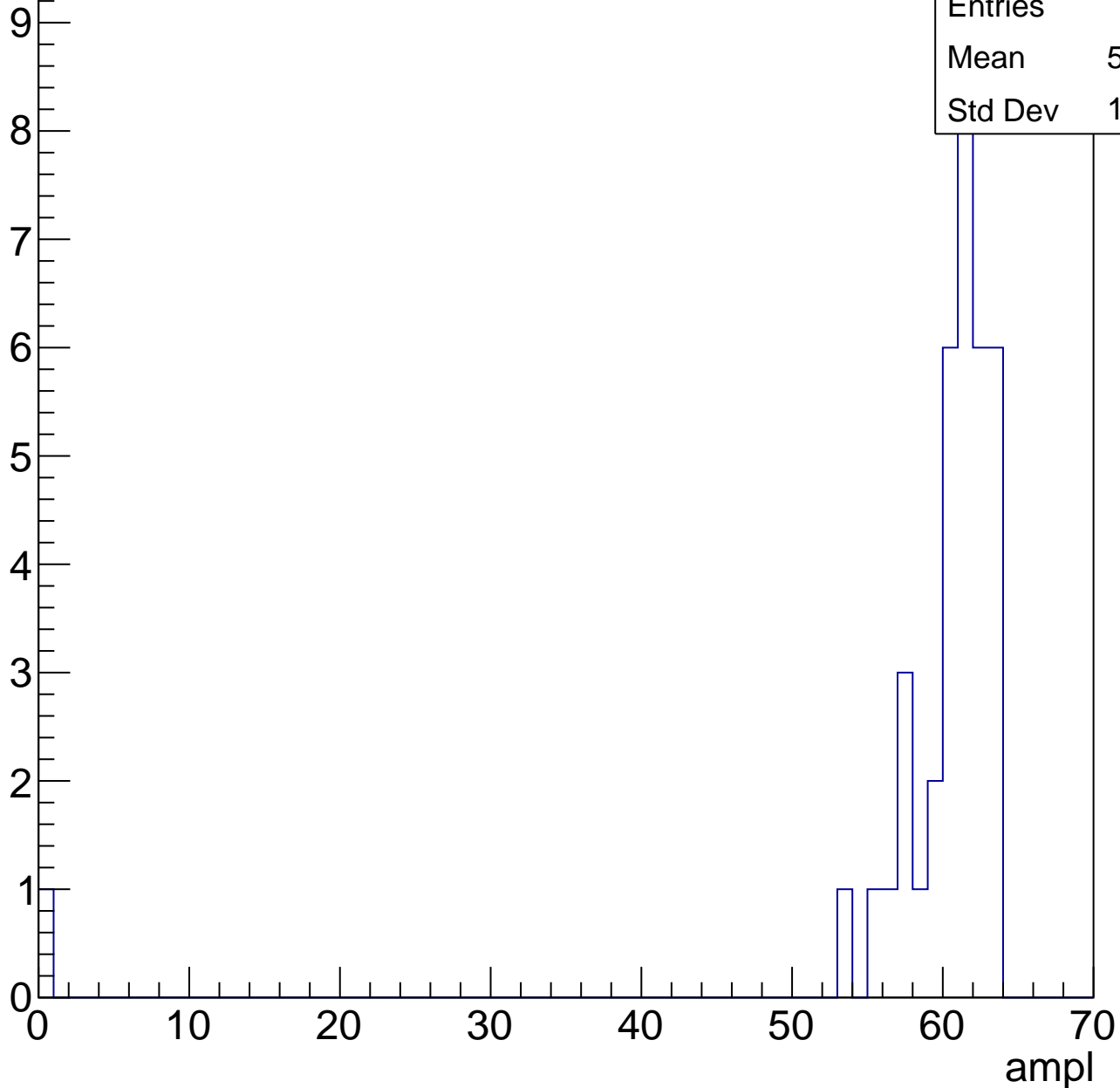


Entries	52
Mean	56.48
Std Dev	2.742

# B1L103S, U9-ch3, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

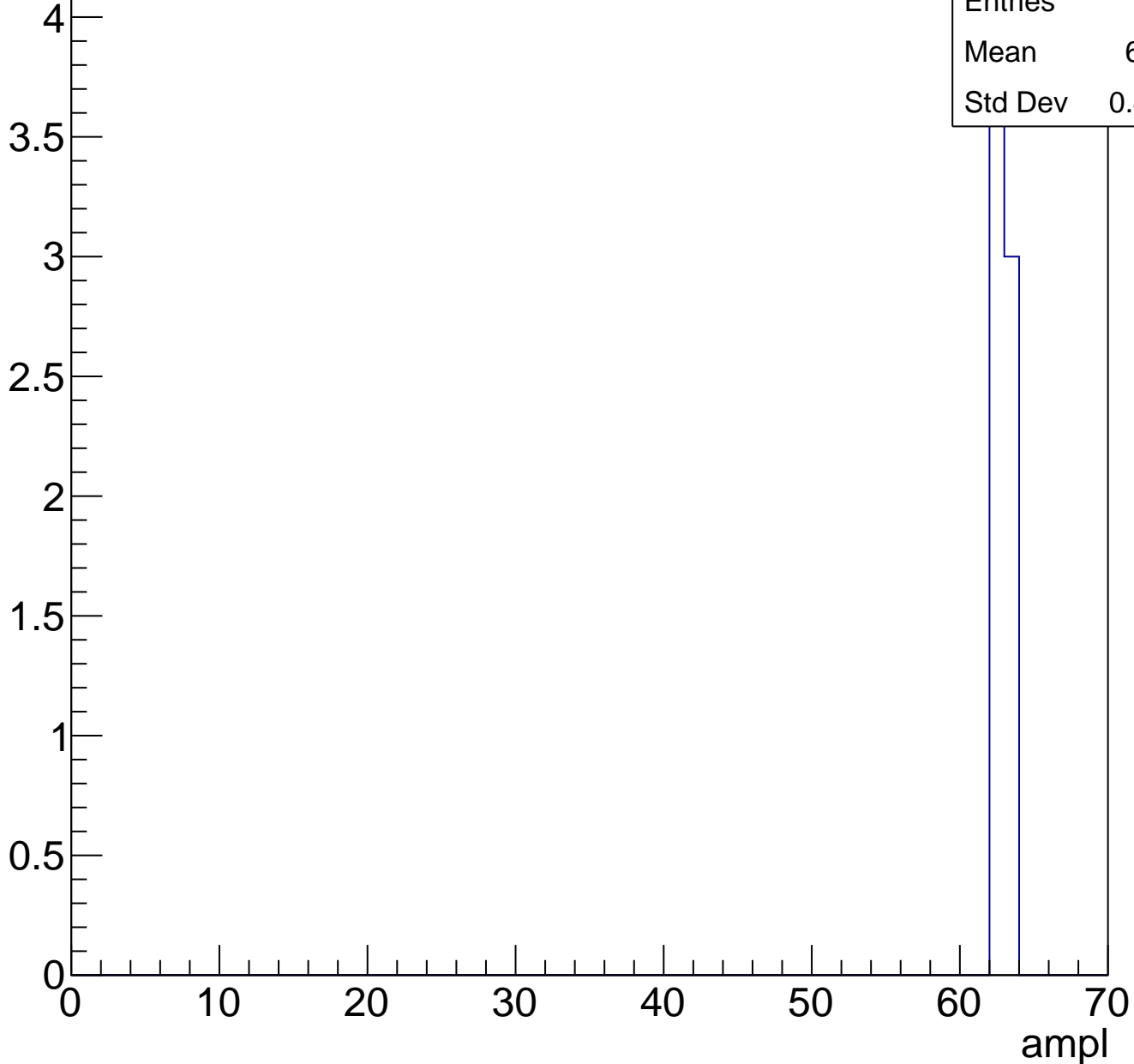
Entry



# B1L103S, U9-ch3, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U9-ch3, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U9-ch4, adc0

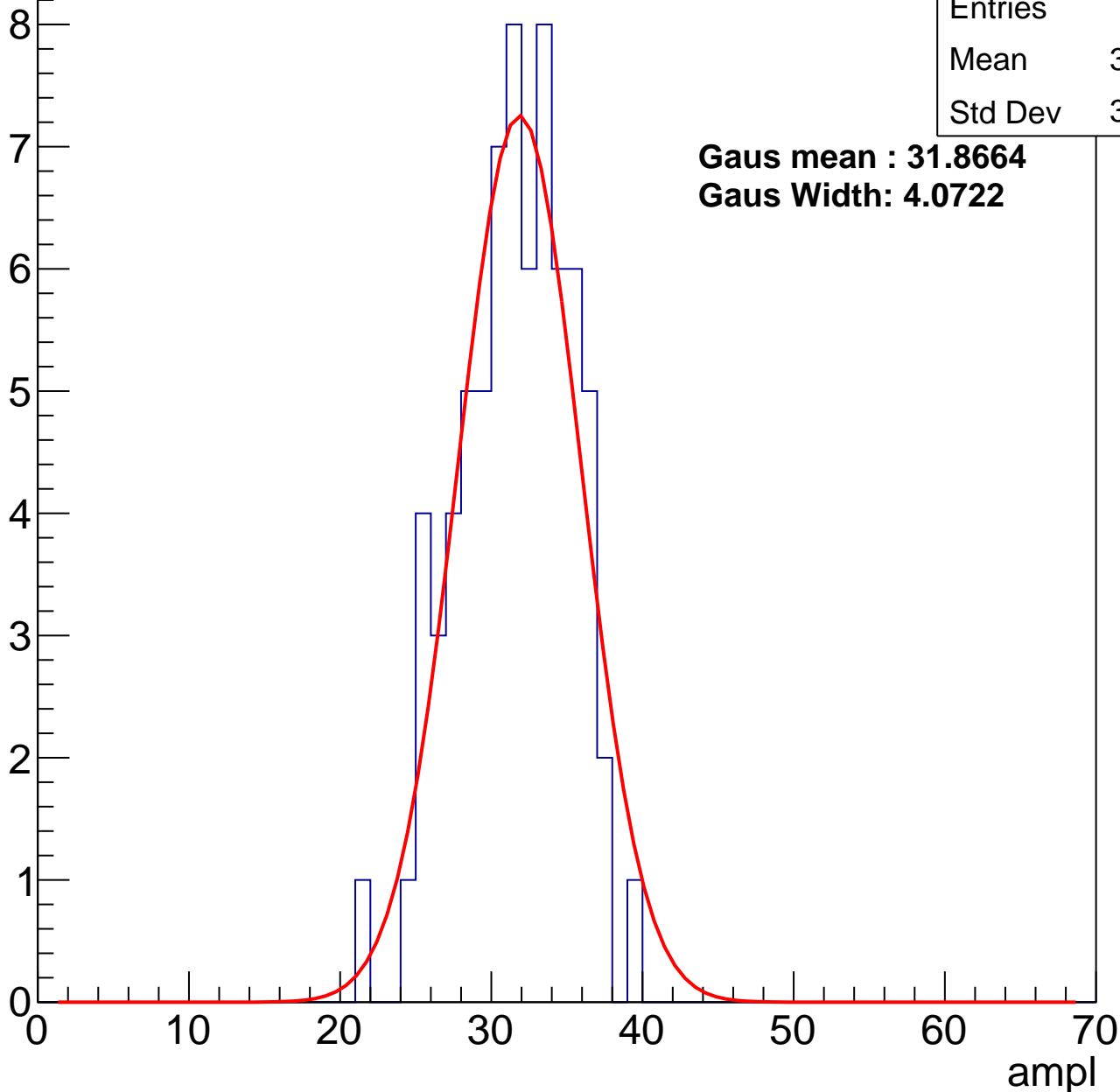
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	72
Mean	31.07
Std Dev	3.637

**Gaus mean : 31.8664**

**Gaus Width: 4.0722**



# B1L103S, U9-ch4, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	67
Mean	37.22
Std Dev	5.698

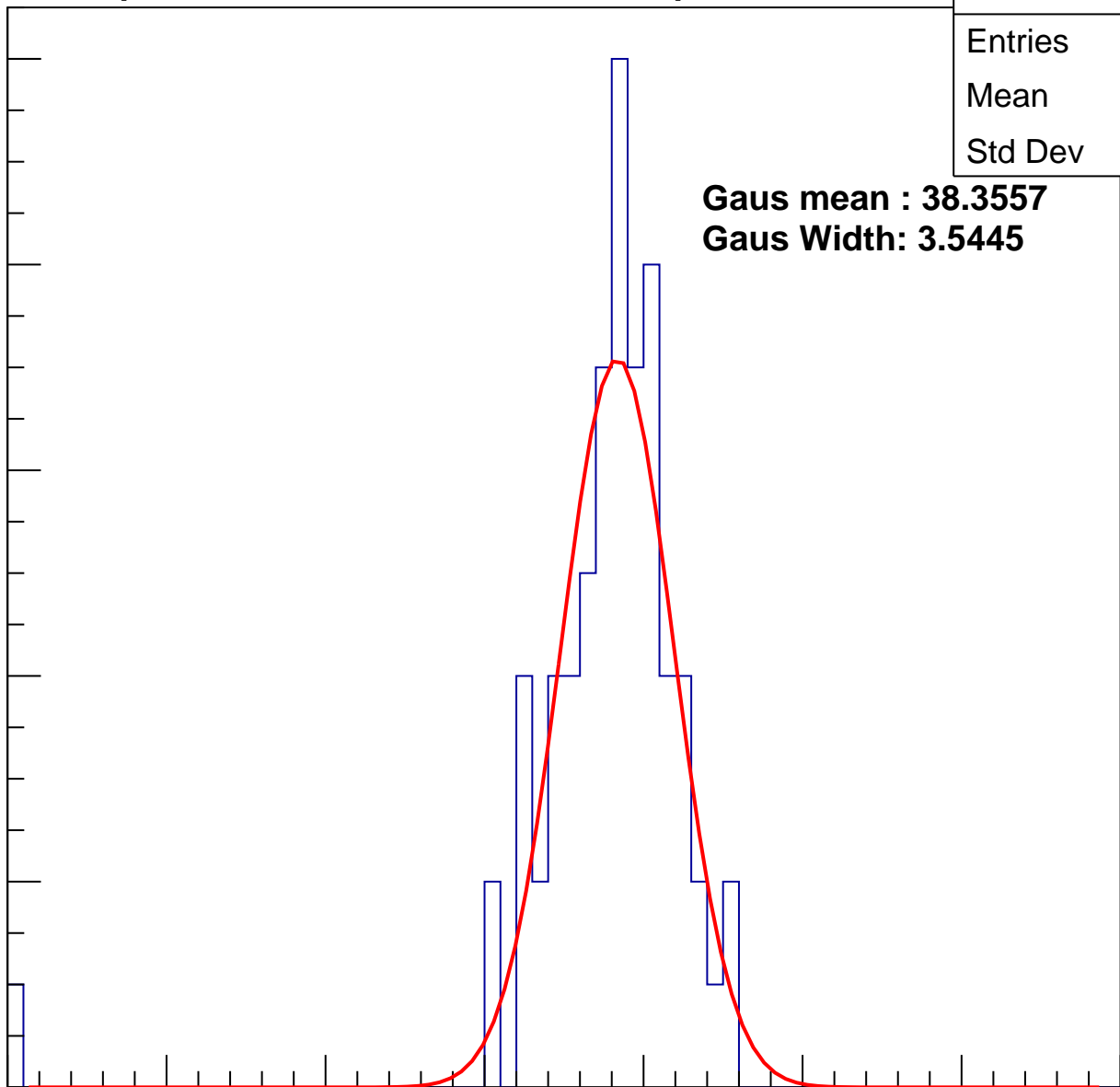
**Gaus mean : 38.3557**  
**Gaus Width: 3.5445**

Entry

10  
8  
6  
4  
2  
0

ampl

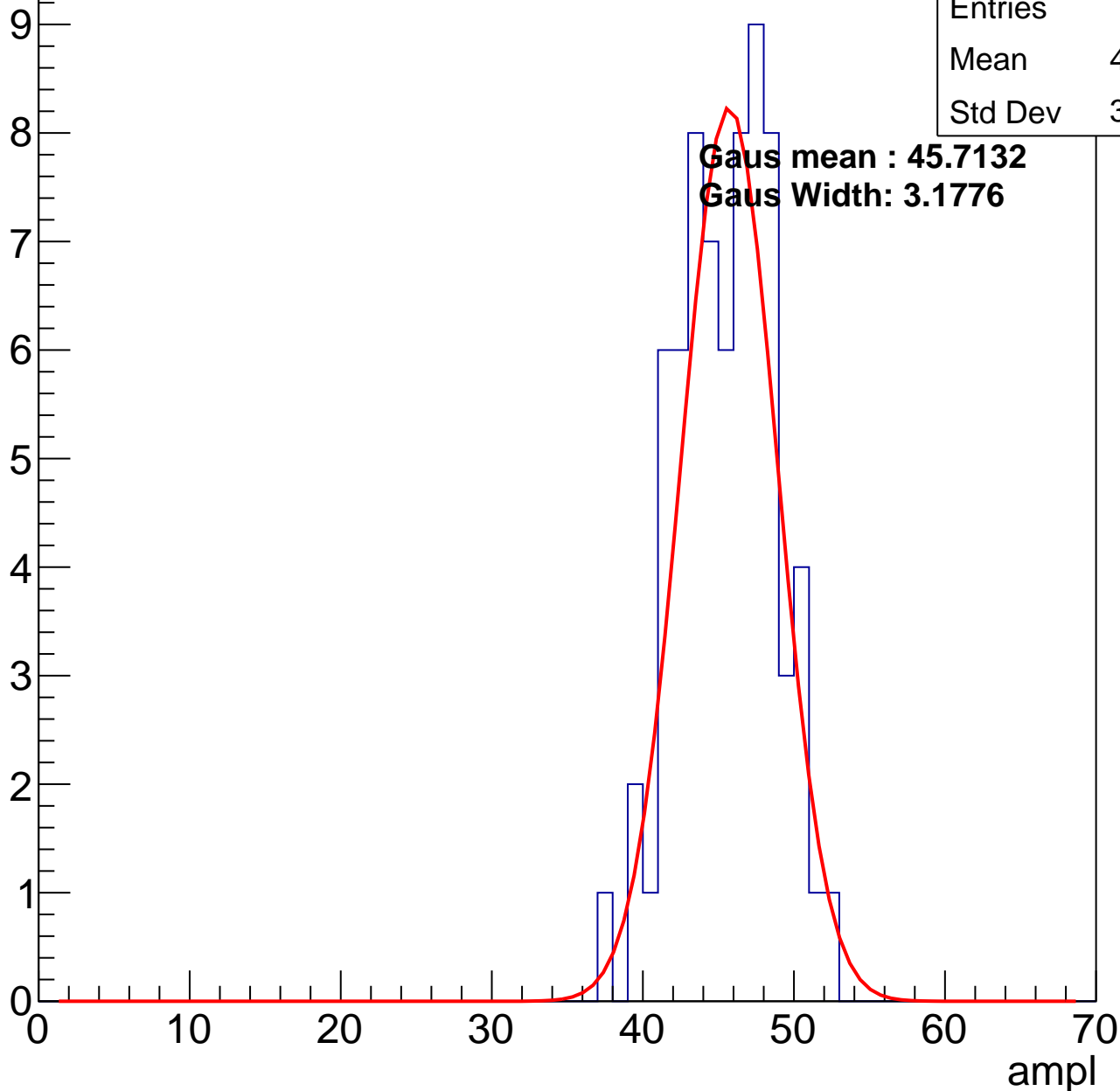
0 10 20 30 40 50 60 70



# B1L103S, U9-ch4, adc2

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

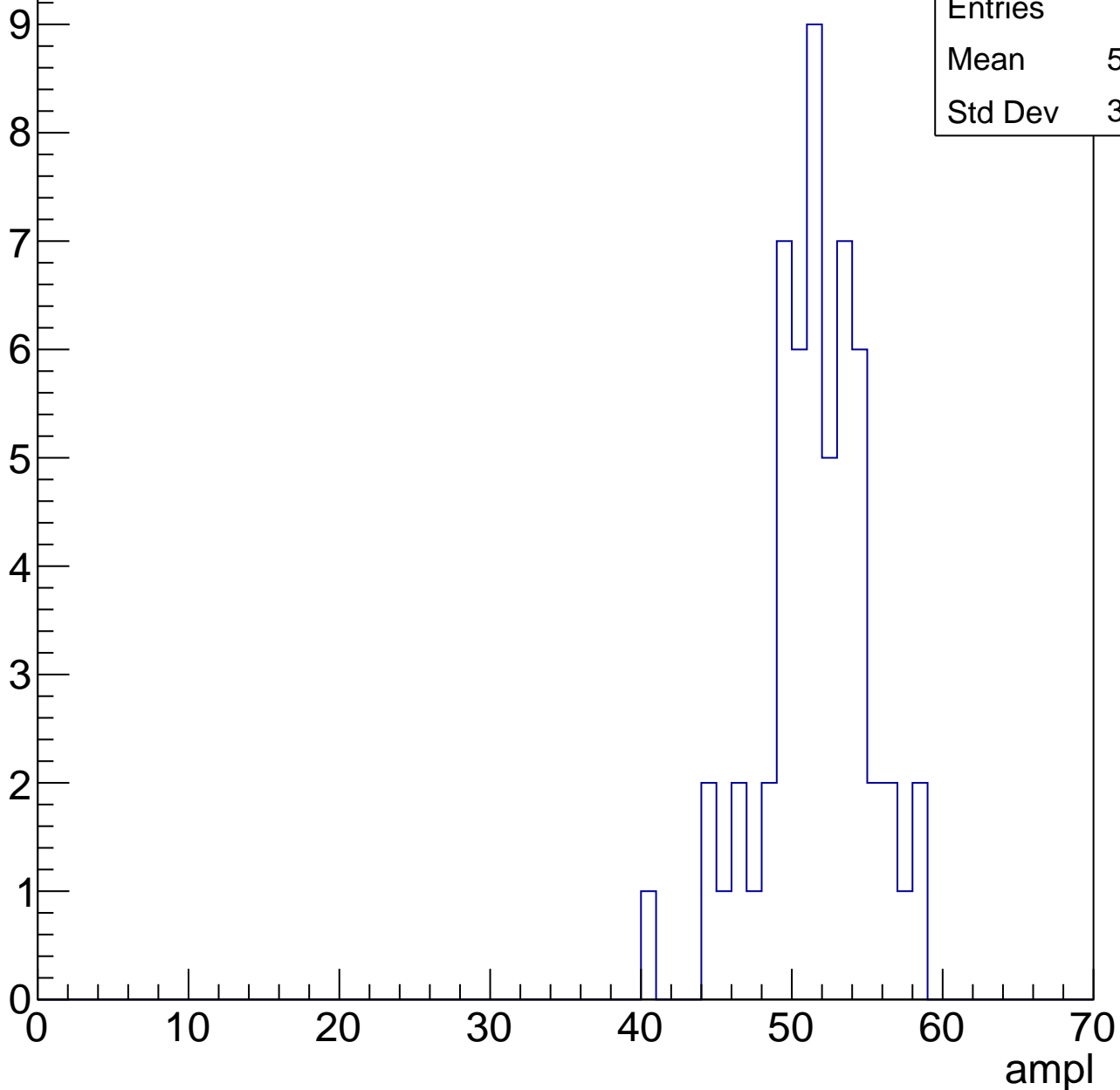


# B1L103S, U9-ch4, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	56
Mean	51.07
Std Dev	3.474



# B1L103S, U9-ch4, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	72
Mean	56.56
Std Dev	7.422

Entry

10

8

6

4

2

0

0

10

20

30

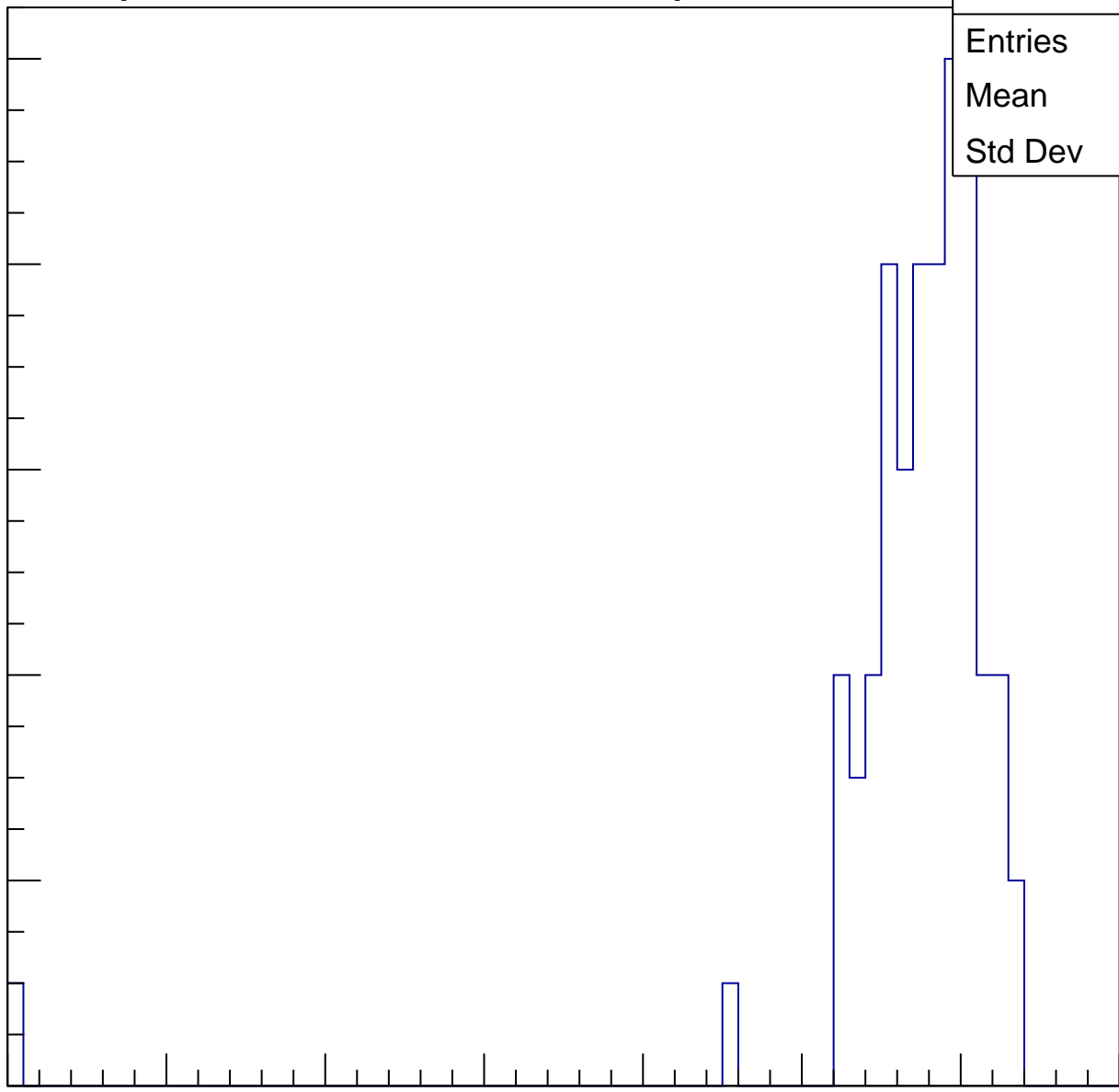
40

50

60

70

ampl

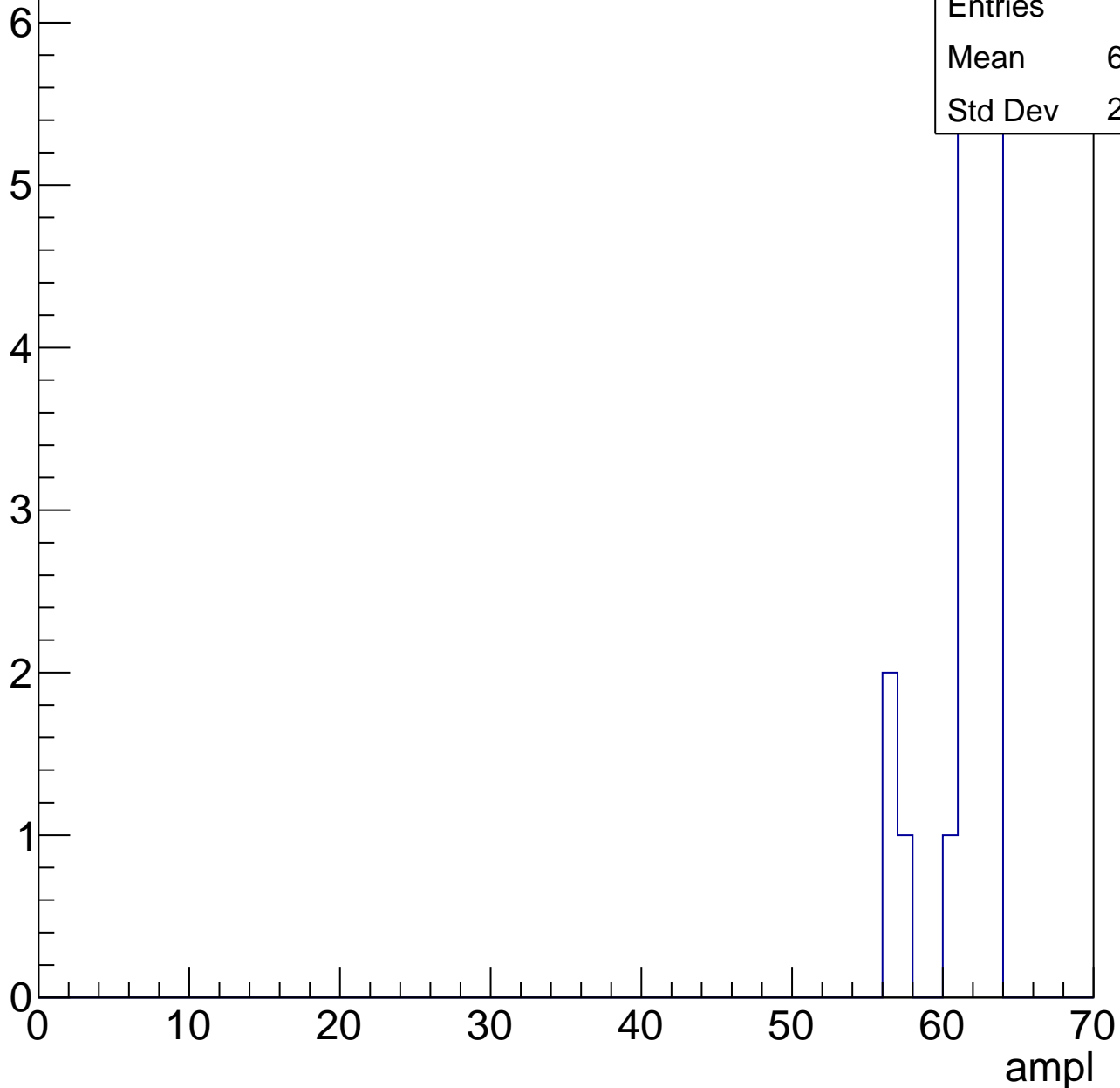


# B1L103S, U9-ch4, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	22
Mean	61.14
Std Dev	2.095



# B1L103S, U9-ch4, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	2
Mean	63
Std Dev	0

ampl



# B1L103S, U9-ch4, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U9-ch5, adc0

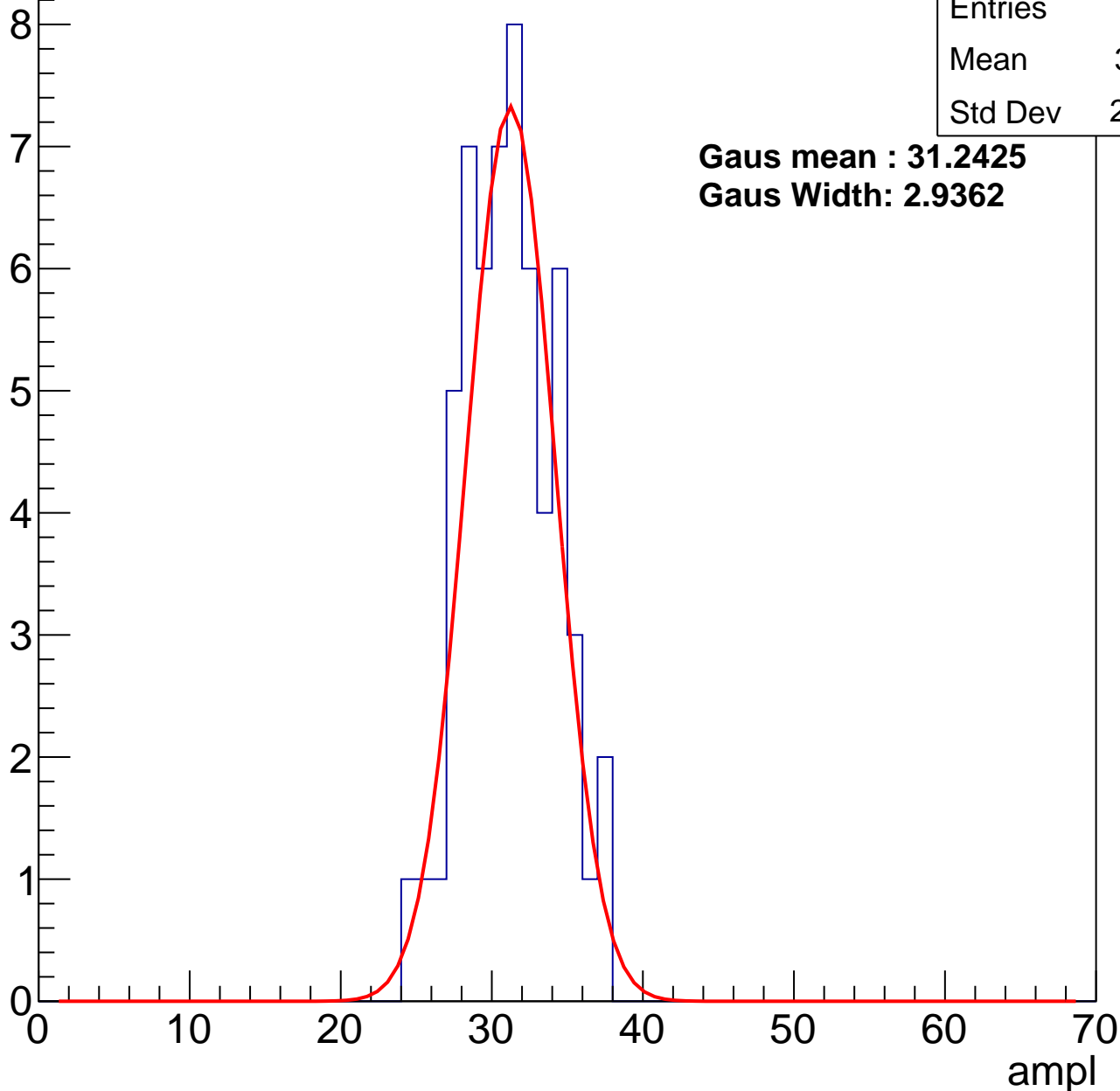
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	58
Mean	30.71
Std Dev	2.936

**Gaus mean : 31.2425**

**Gaus Width: 2.9362**



# B1L103S, U9-ch5, adc1

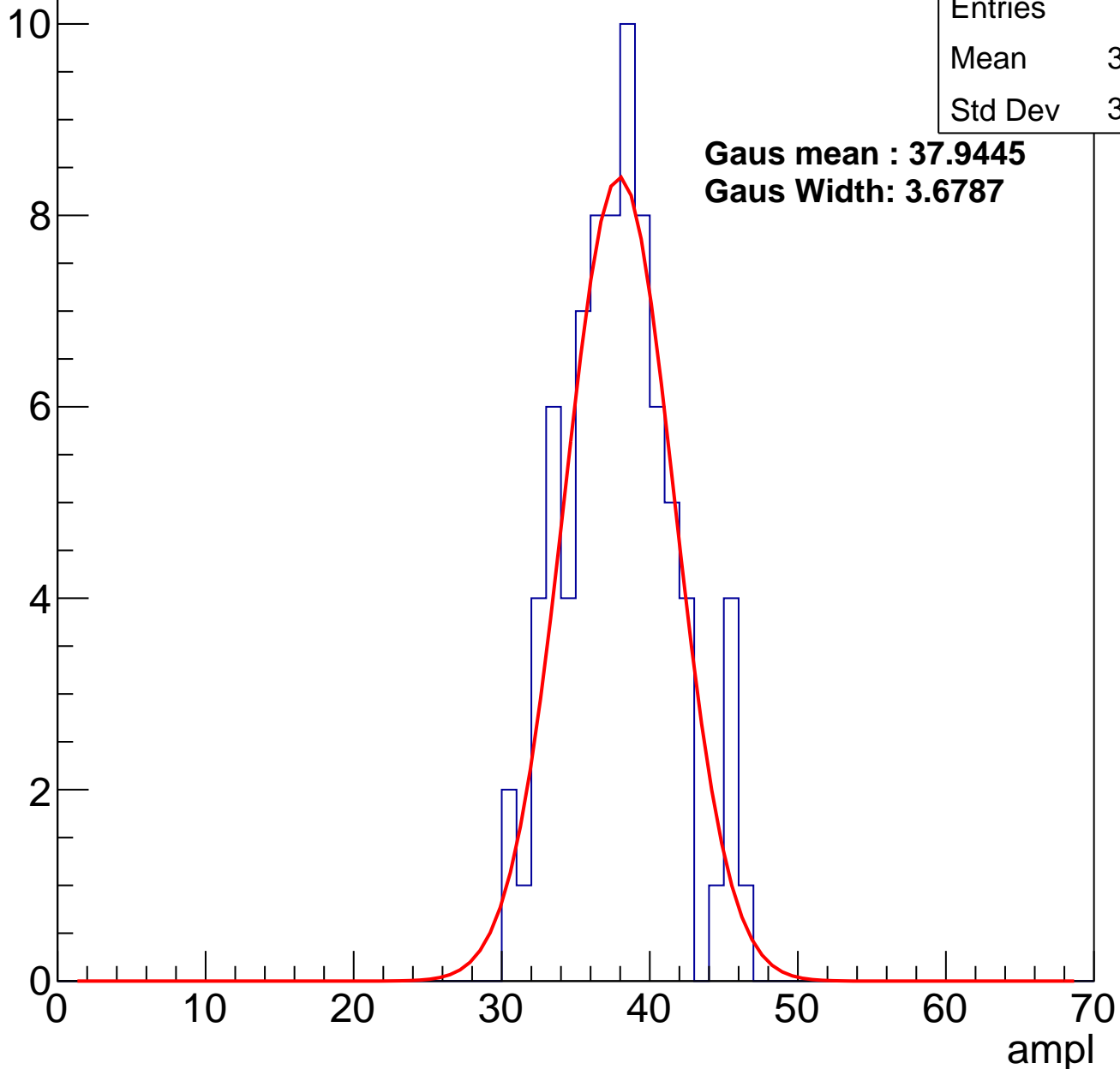
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	79
Mean	37.43
Std Dev	3.645

**Gaus mean : 37.9445**

**Gaus Width: 3.6787**

Entry



# B1L103S, U9-ch5, adc2

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	61
Mean	44.66
Std Dev	3.506

**Gaus mean : 45.3203**

**Gaus Width: 4.9601**

Entry

10

8

6

4

2

0

0

10

20

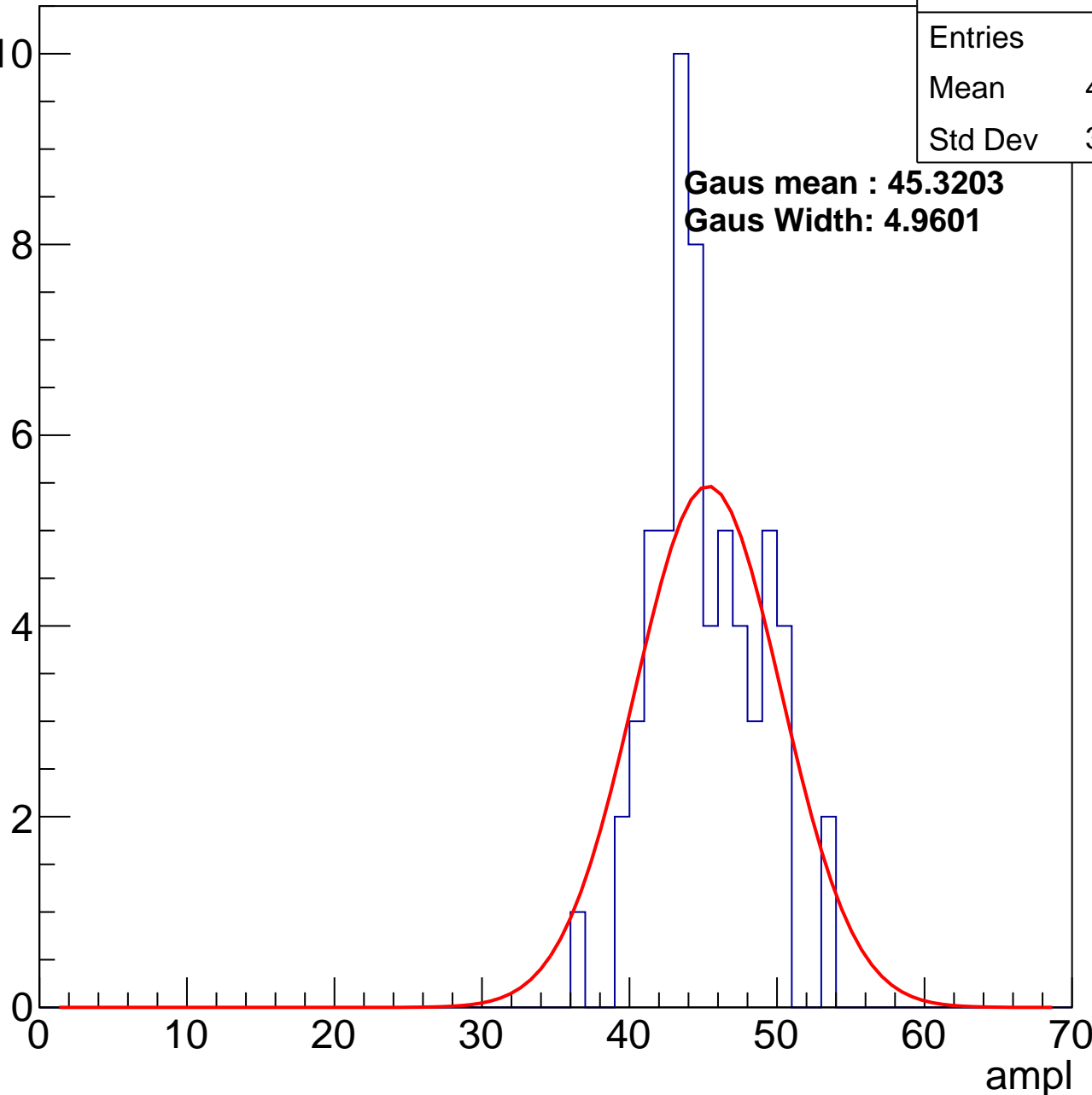
30

40

50

60

ampl

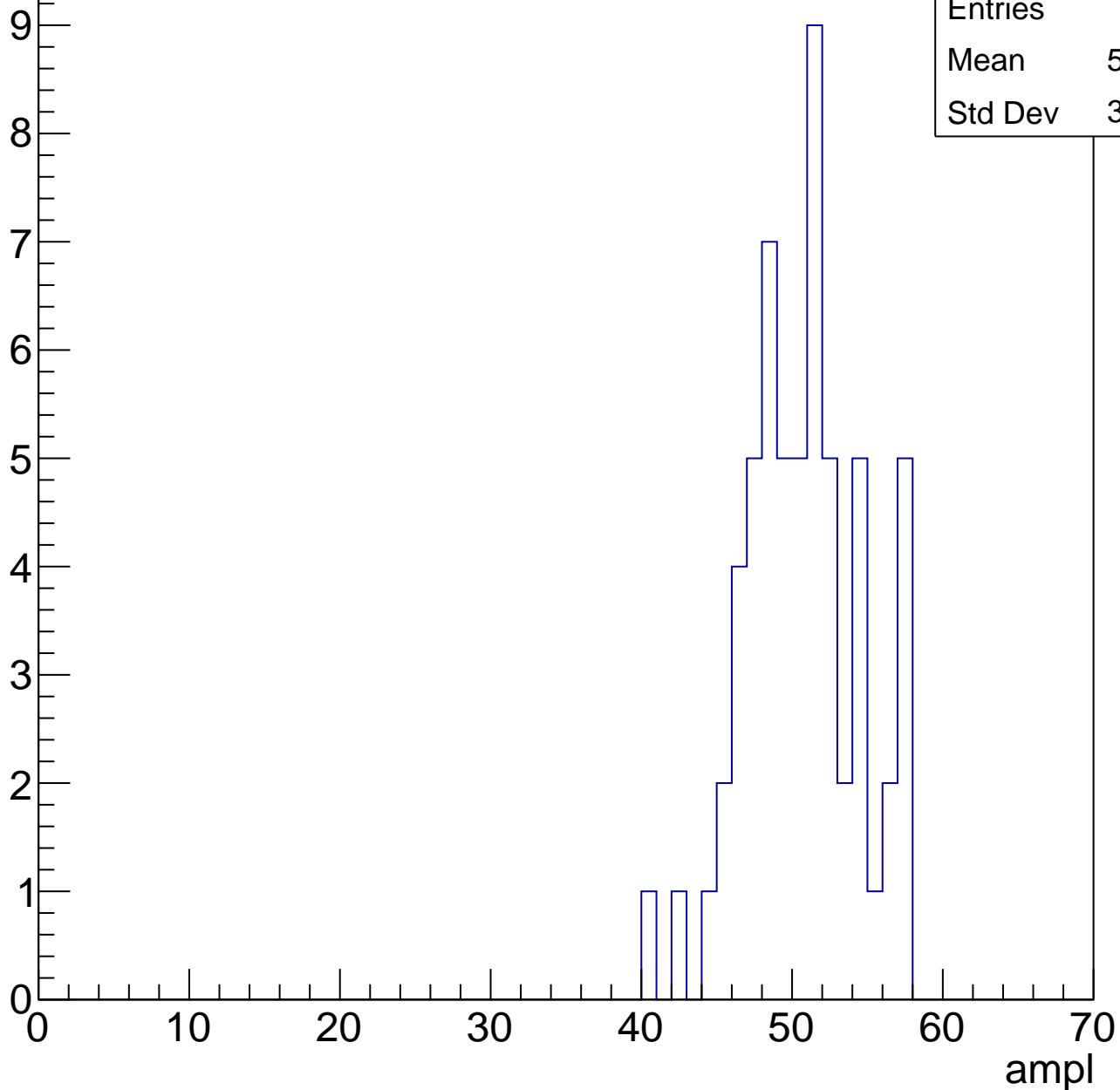


# B1L103S, U9-ch5, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

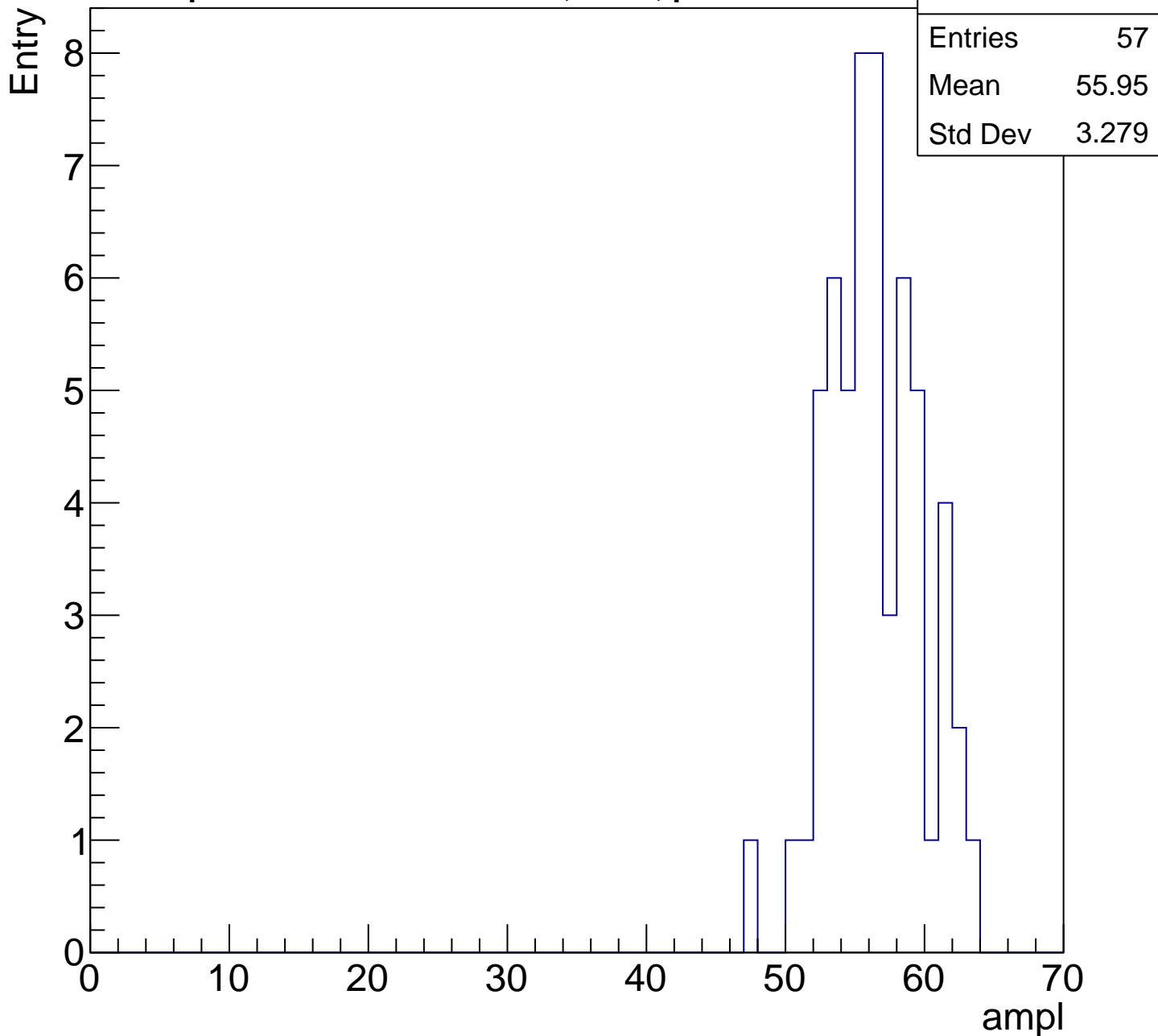
Entry

Entries	60
Mean	50.22
Std Dev	3.782



# B1L103S, U9-ch5, adc4

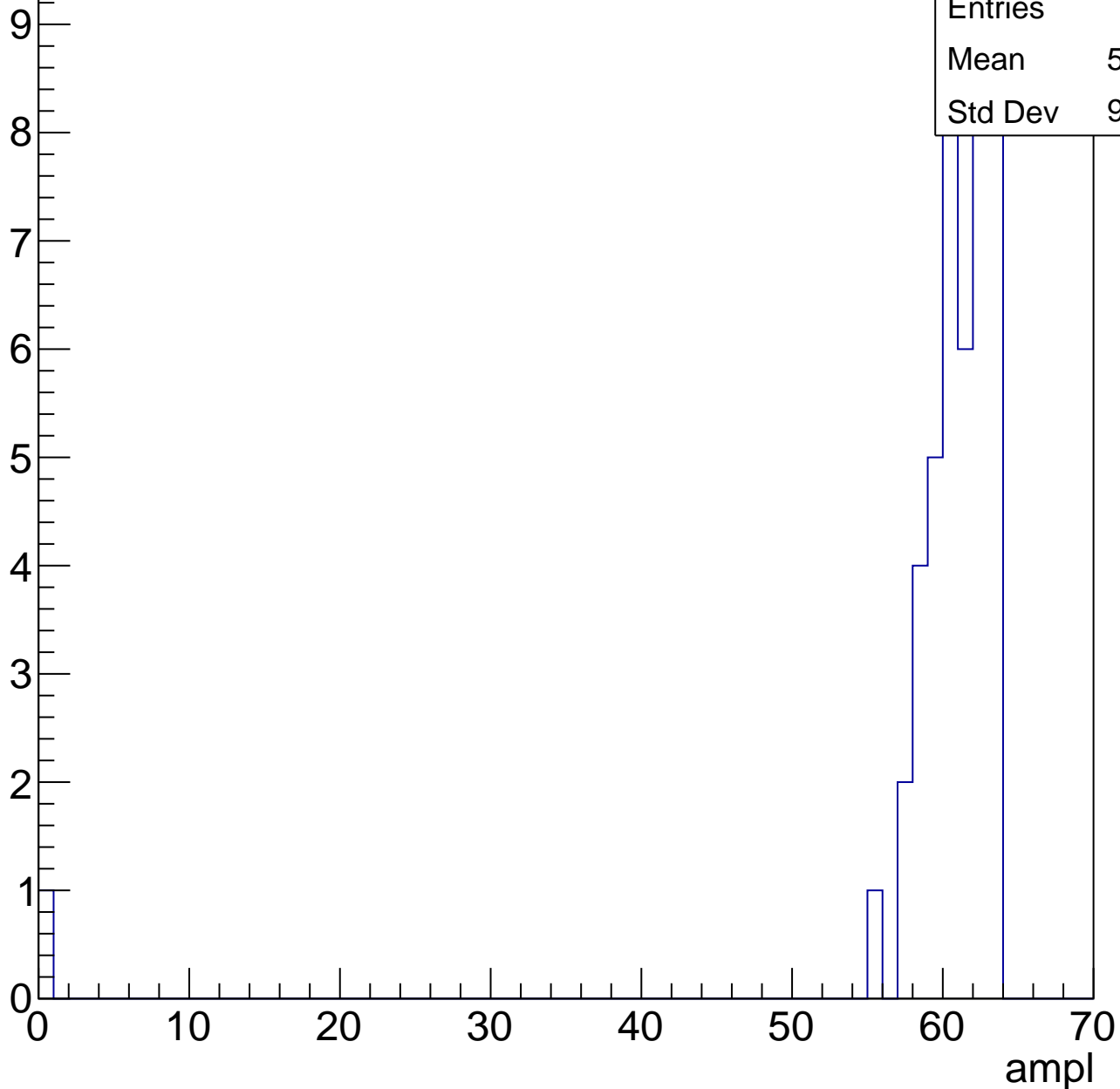
calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U9-ch5, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U9-ch5, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0



# B1L103S, U9-ch5, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

1  
0.8  
0.6  
0.4  
0.2  
0

Entries	1
Mean	23
Std Dev	0

ampl

# B1L103S, U9-ch6, adc0

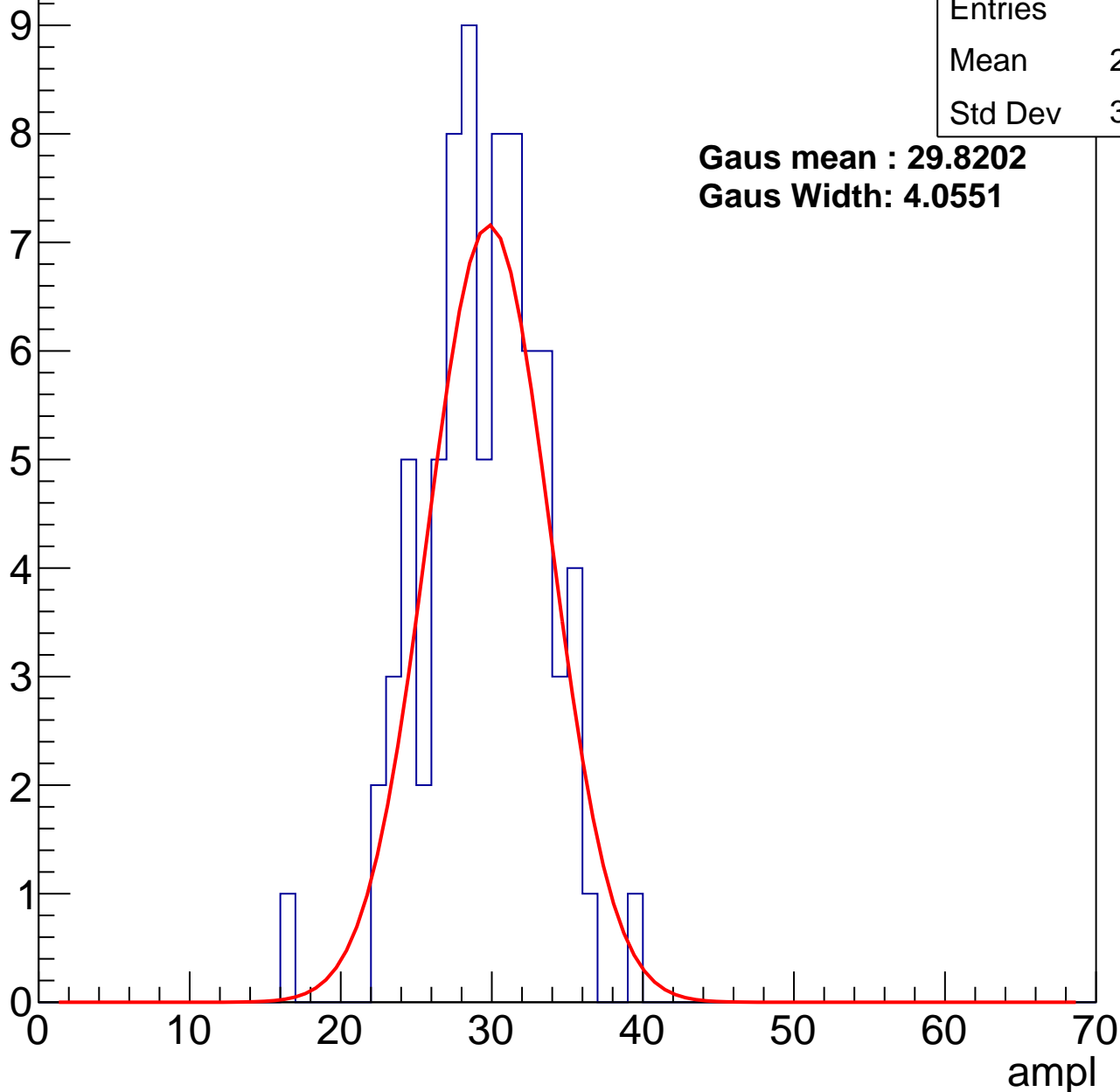
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	77
Mean	29.05
Std Dev	3.908

**Gaus mean : 29.8202**

**Gaus Width: 4.0551**



# B1L103S, U9-ch6, adc1

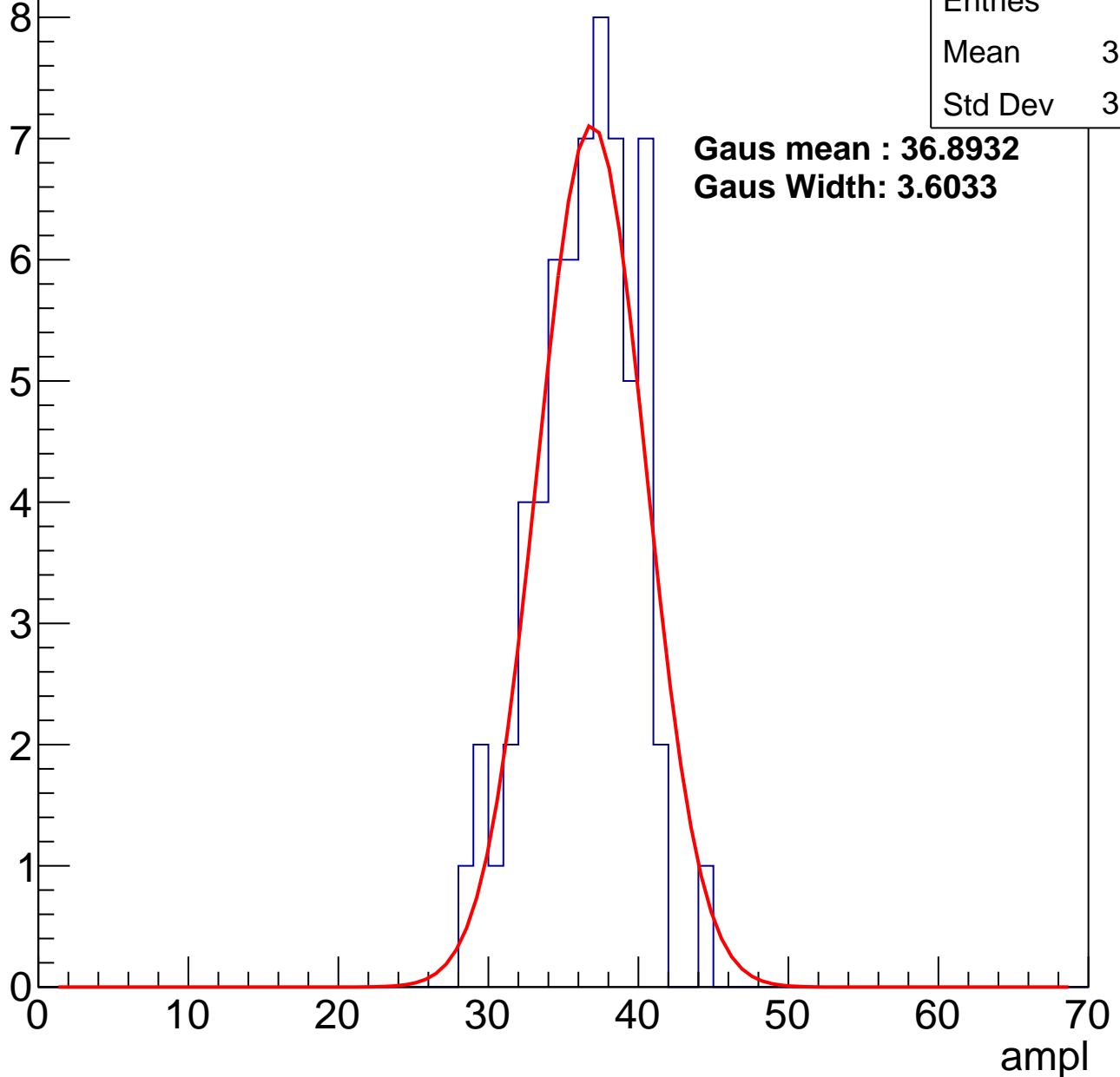
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	35.98
Std Dev	3.297

**Gaus mean : 36.8932**

**Gaus Width: 3.6033**



# B1L103S, U9-ch6, adc2

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	77
Mean	43.48
Std Dev	3.581

**Gaus mean : 43.8818**

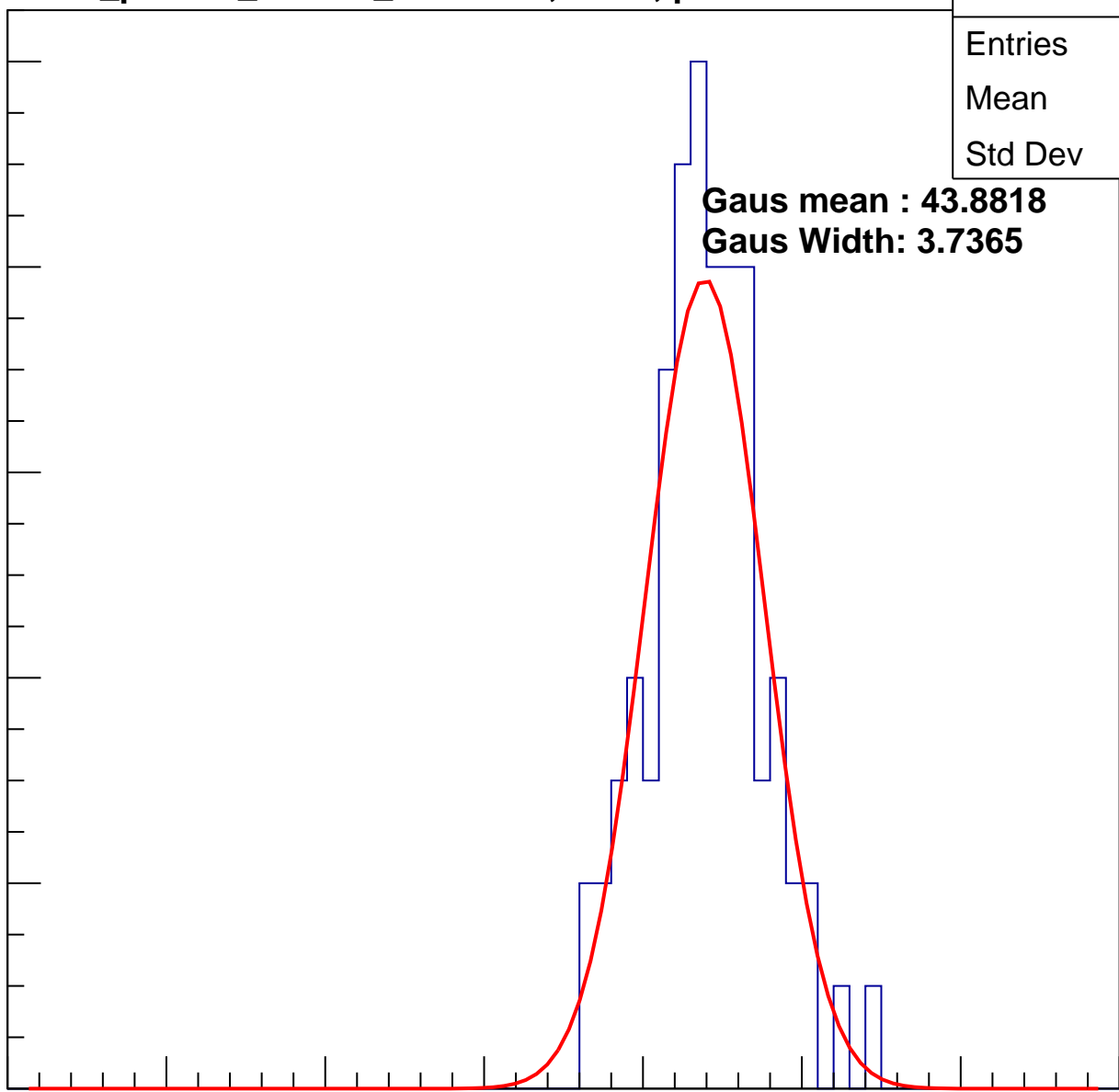
**Gaus Width: 3.7365**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

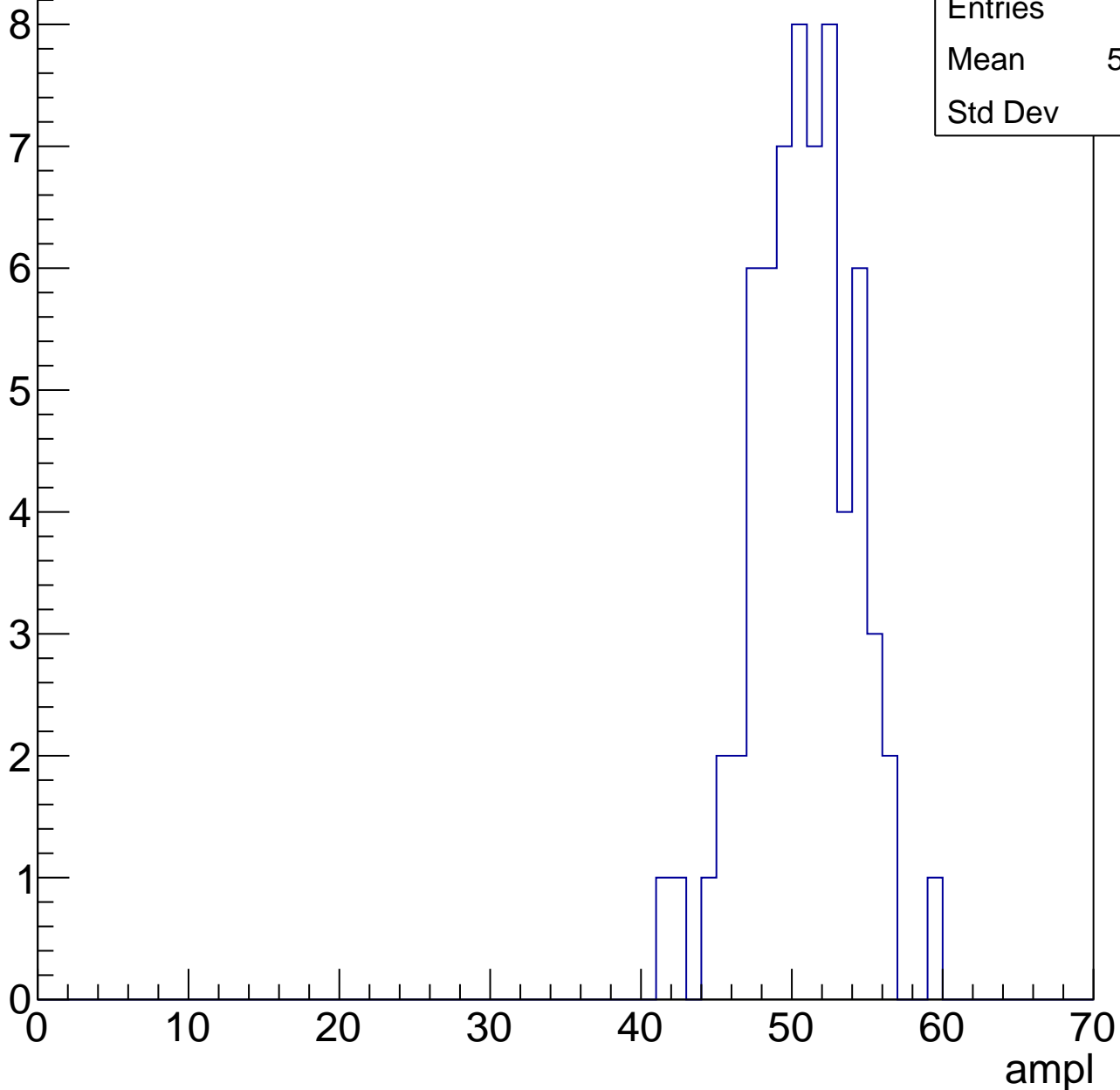


# B1L103S, U9-ch6, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	50.26
Std Dev	3.38

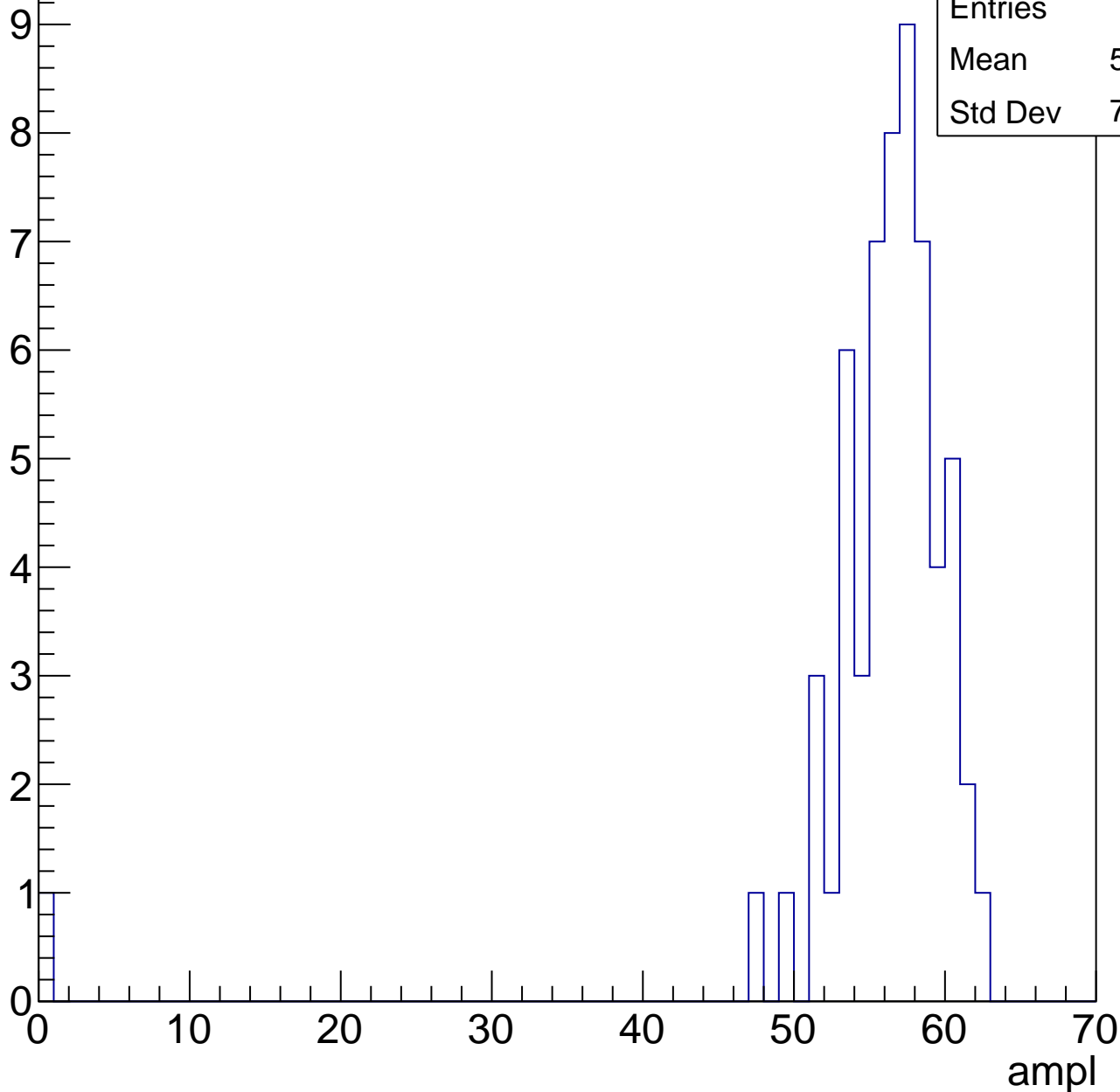


# B1L103S, U9-ch6, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

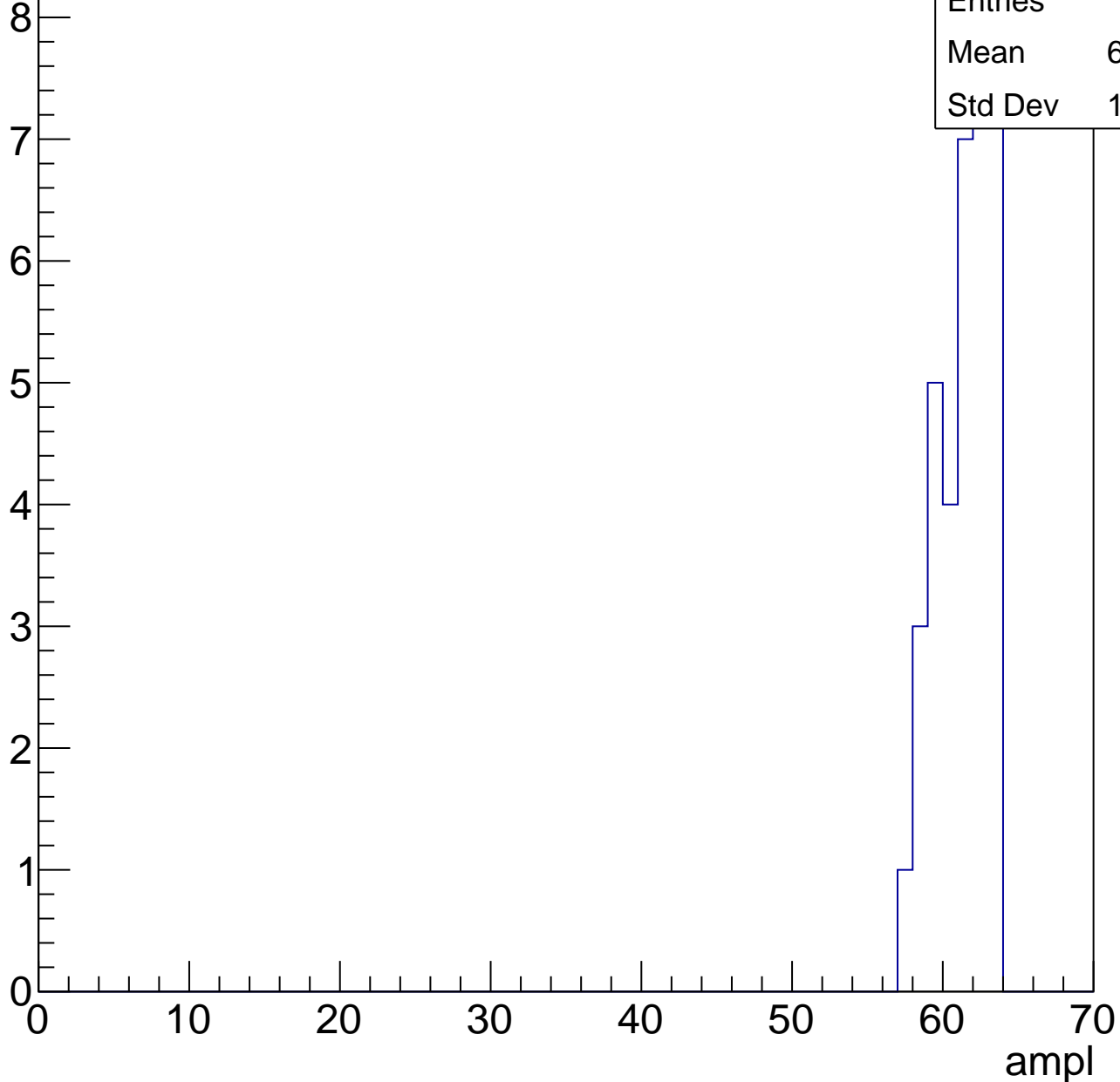
Entries	59
Mean	55.14
Std Dev	7.838



# B1L103S, U9-ch6, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	36
Mean	60.92
Std Dev	1.722

# B1L103S, U9-ch6, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	4
Mean	62.25
Std Dev	0.8292

ampl

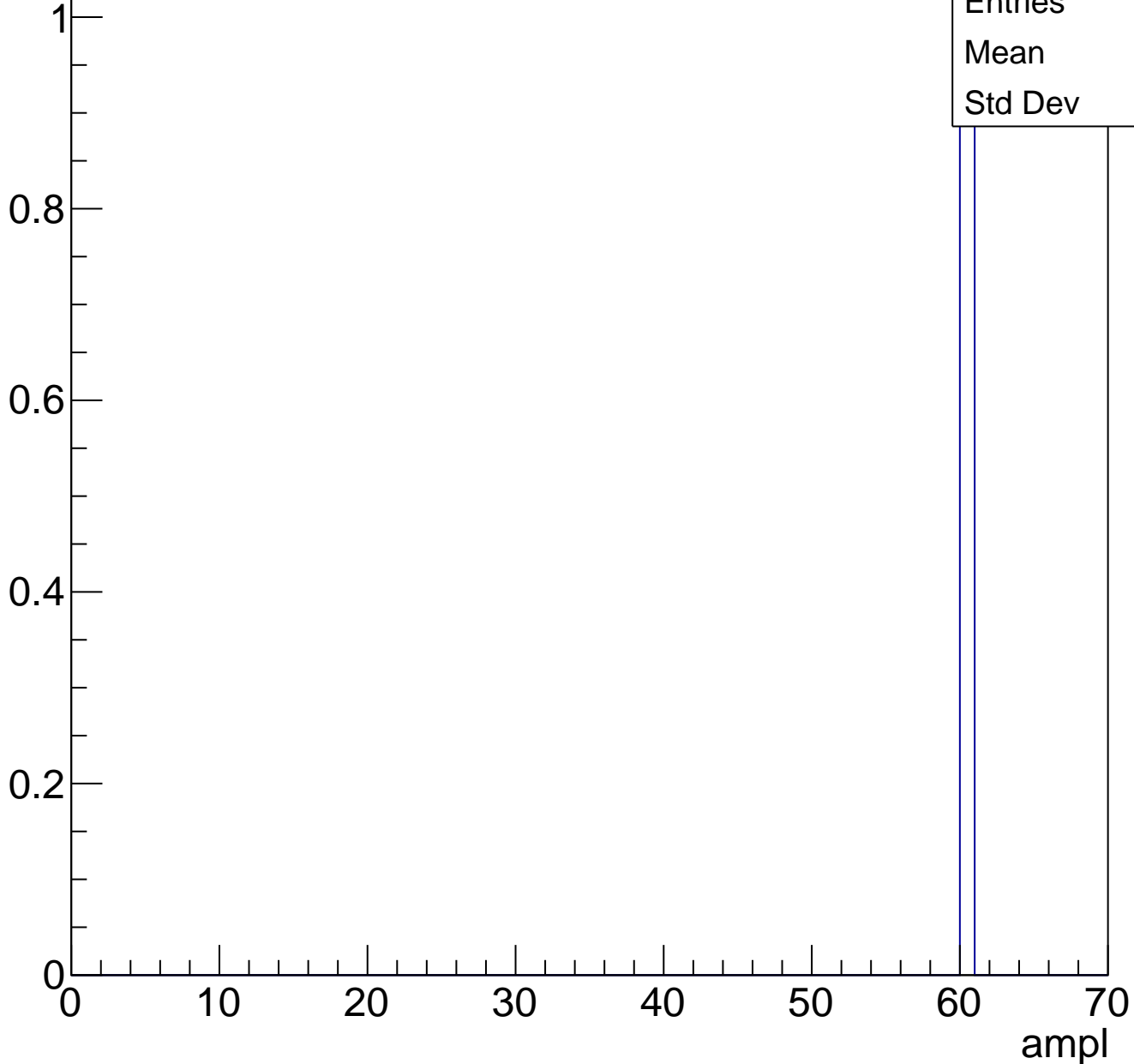
0 10 20 30 40 50 60 70



# B1L103S, U9-ch6, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U9-ch7, adc0

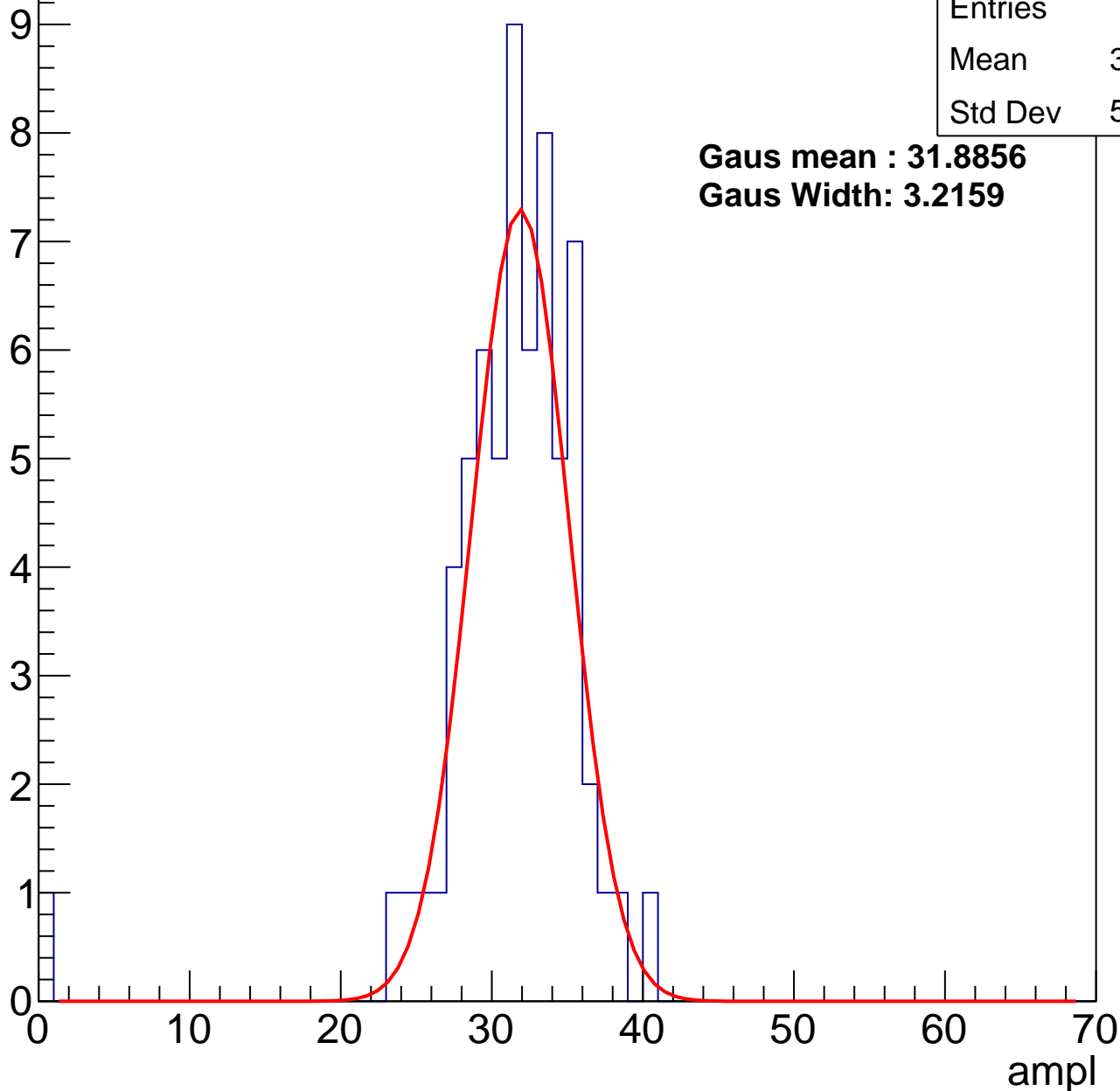
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	30.88
Std Dev	5.088

**Gaus mean : 31.8856**

**Gaus Width: 3.2159**



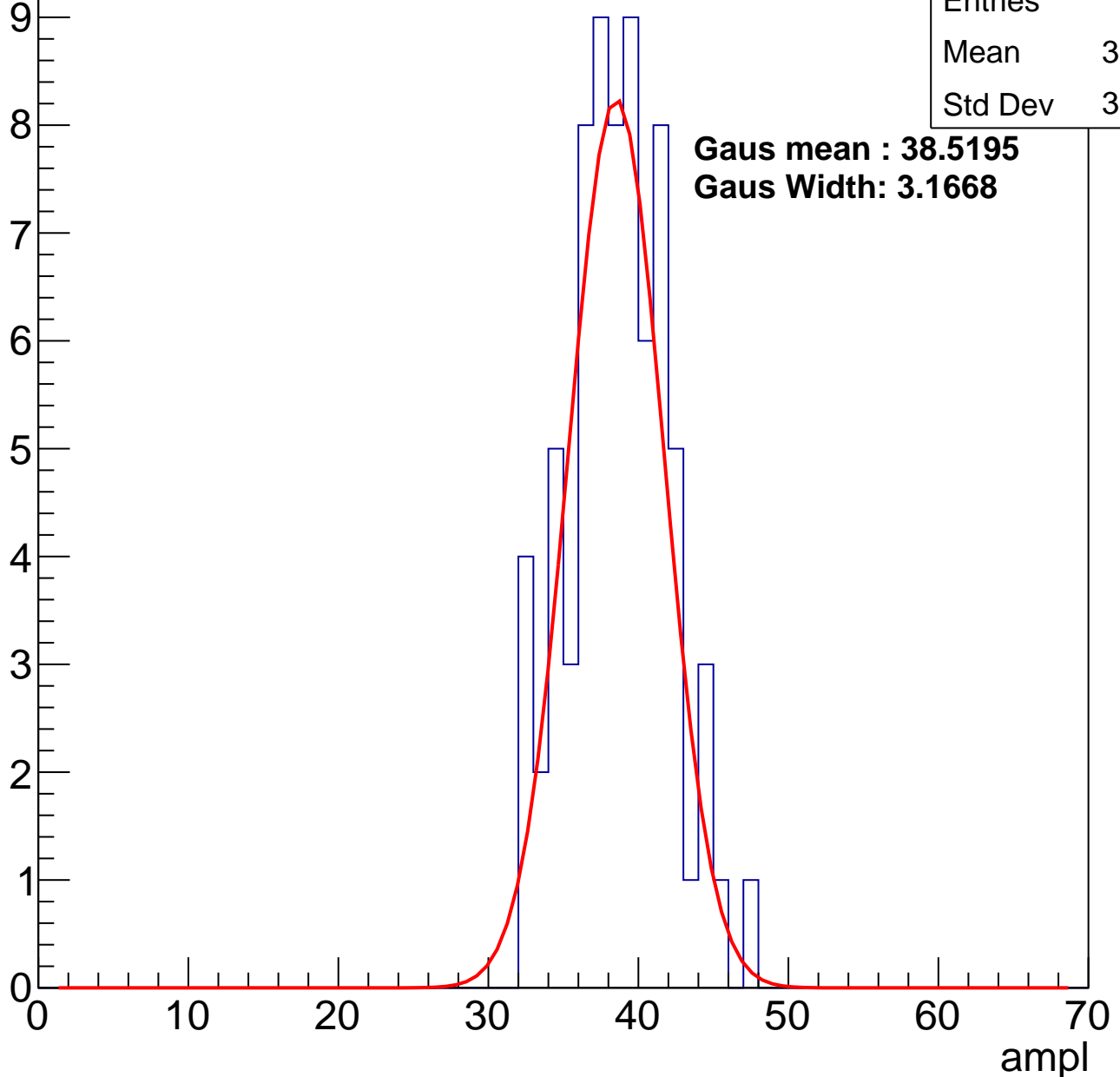
# B1L103S, U9-ch7, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	73
Mean	38.22
Std Dev	3.282

**Gaus mean : 38.5195**  
**Gaus Width: 3.1668**



# B1L103S, U9-ch7, adc2

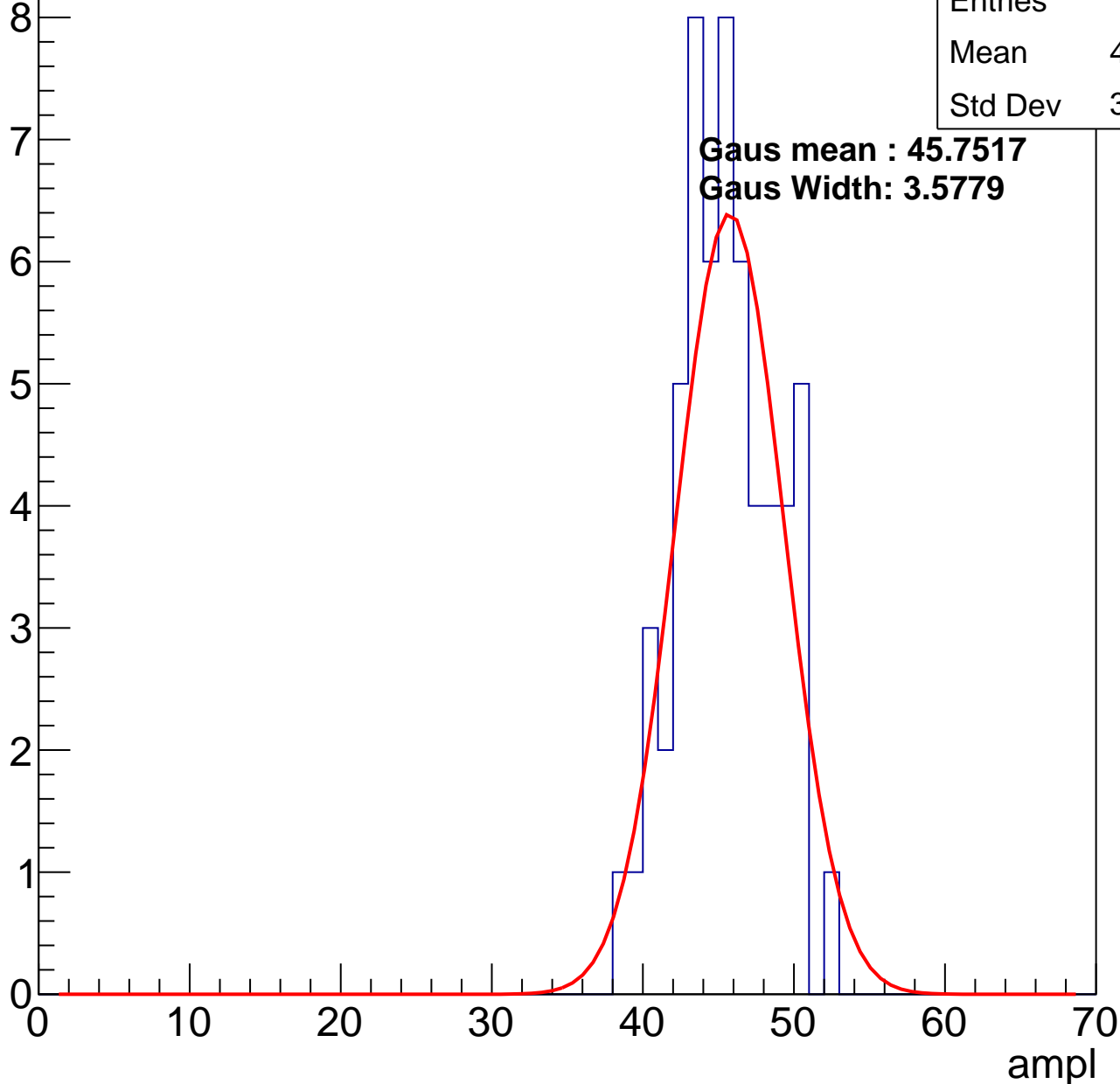
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	58
Mean	45.02
Std Dev	3.138

**Gaus mean : 45.7517**

**Gaus Width: 3.5779**

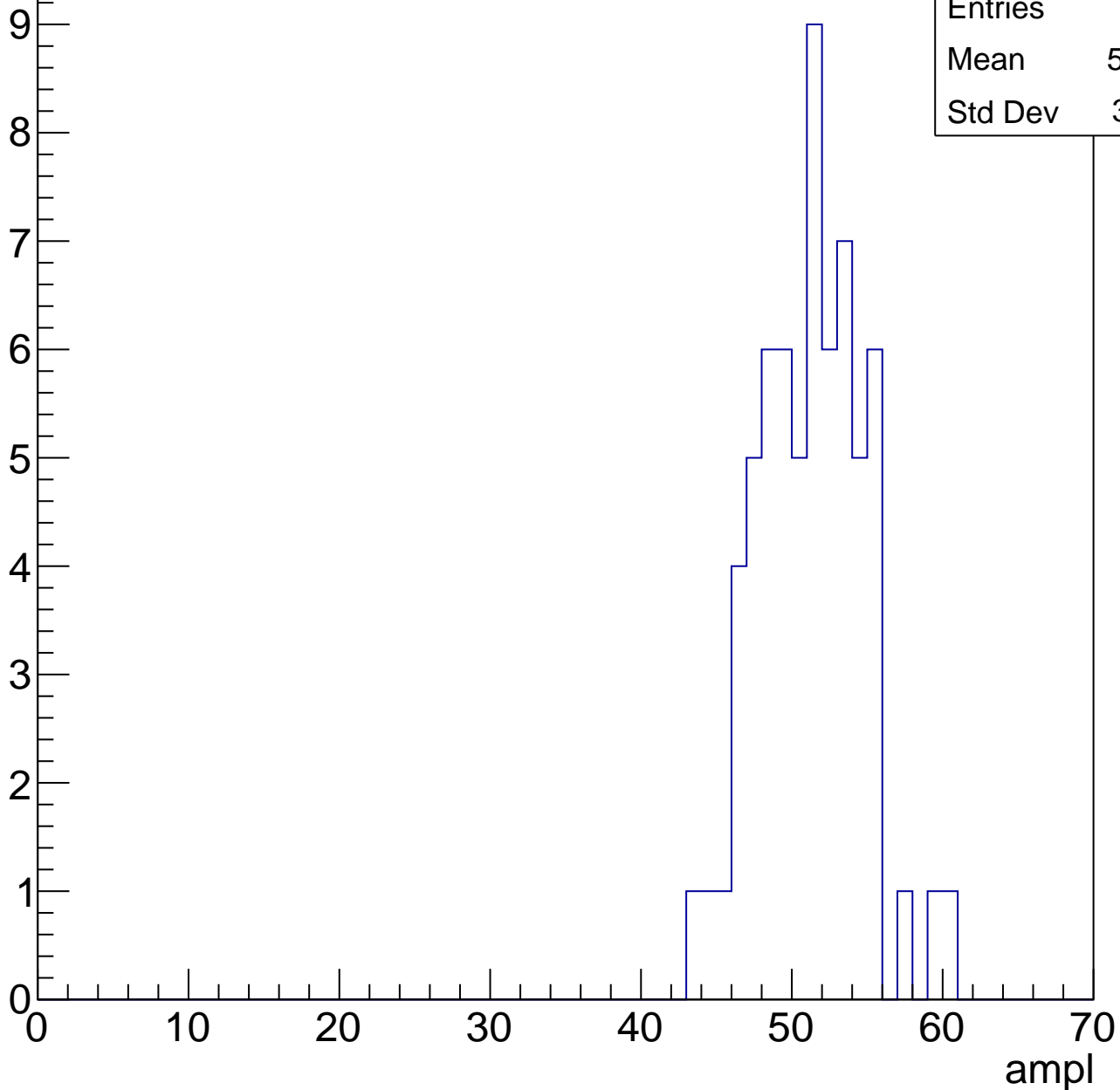


# B1L103S, U9-ch7, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	50.78
Std Dev	3.431

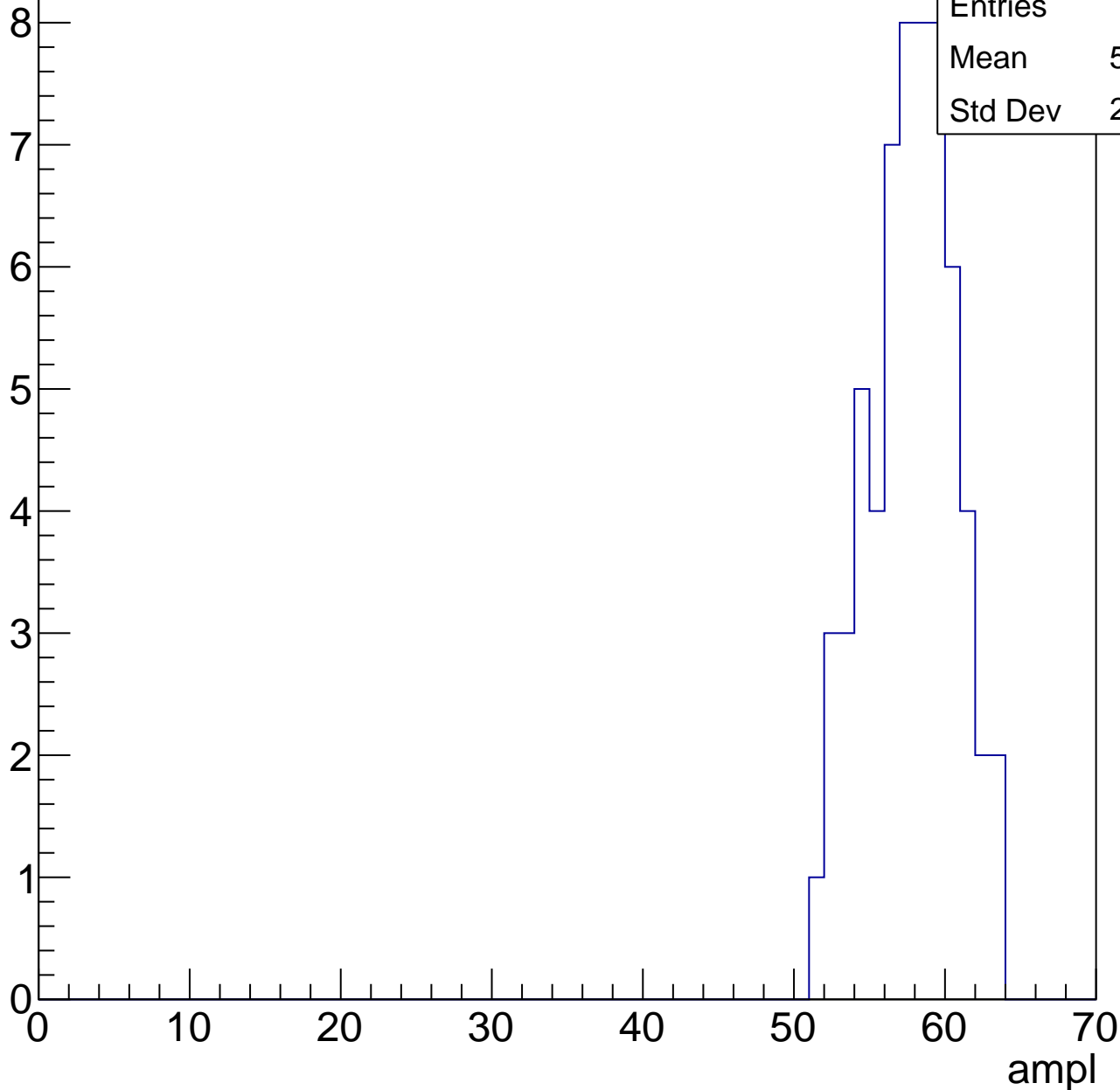


# B1L103S, U9-ch7, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	61
Mean	57.28
Std Dev	2.869

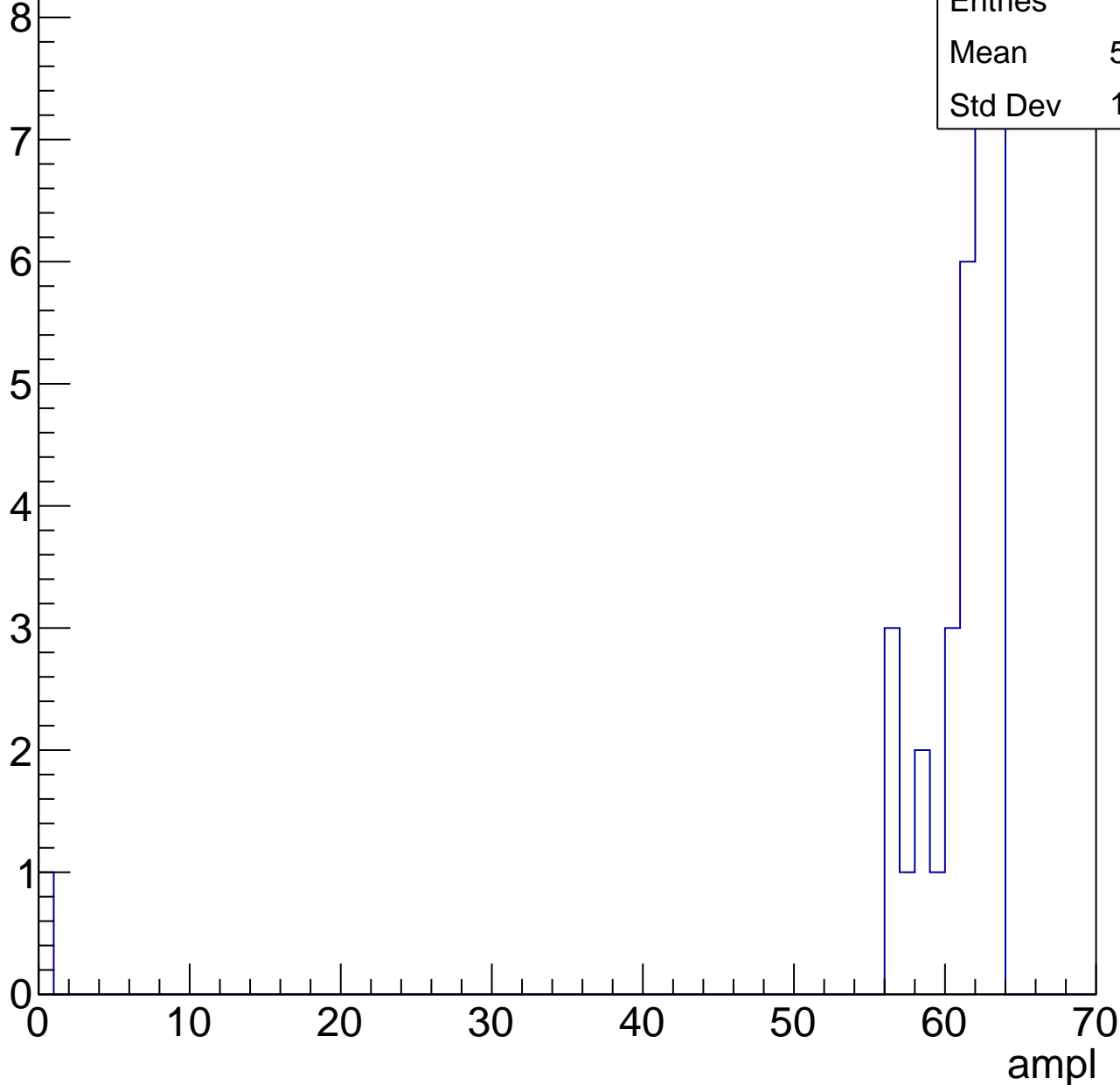


# B1L103S, U9-ch7, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	33
Mean	58.97
Std Dev	10.65



# B1L103S, U9-ch7, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0



# B1L103S, U9-ch7, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U9-ch8, adc0

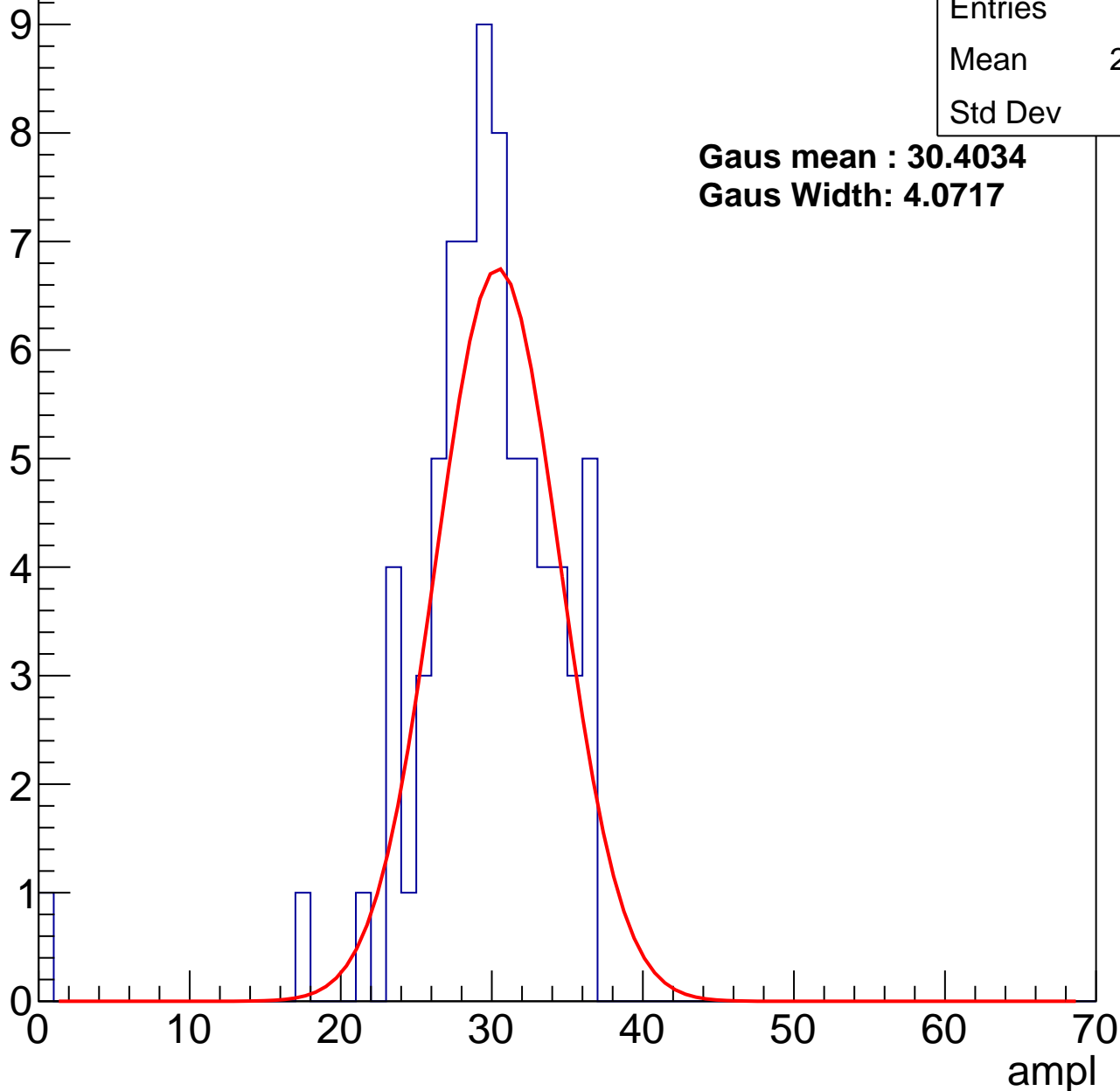
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	73
Mean	28.95
Std Dev	5.15

**Gaus mean : 30.4034**

**Gaus Width: 4.0717**



# B1L103S, U9-ch8, adc1

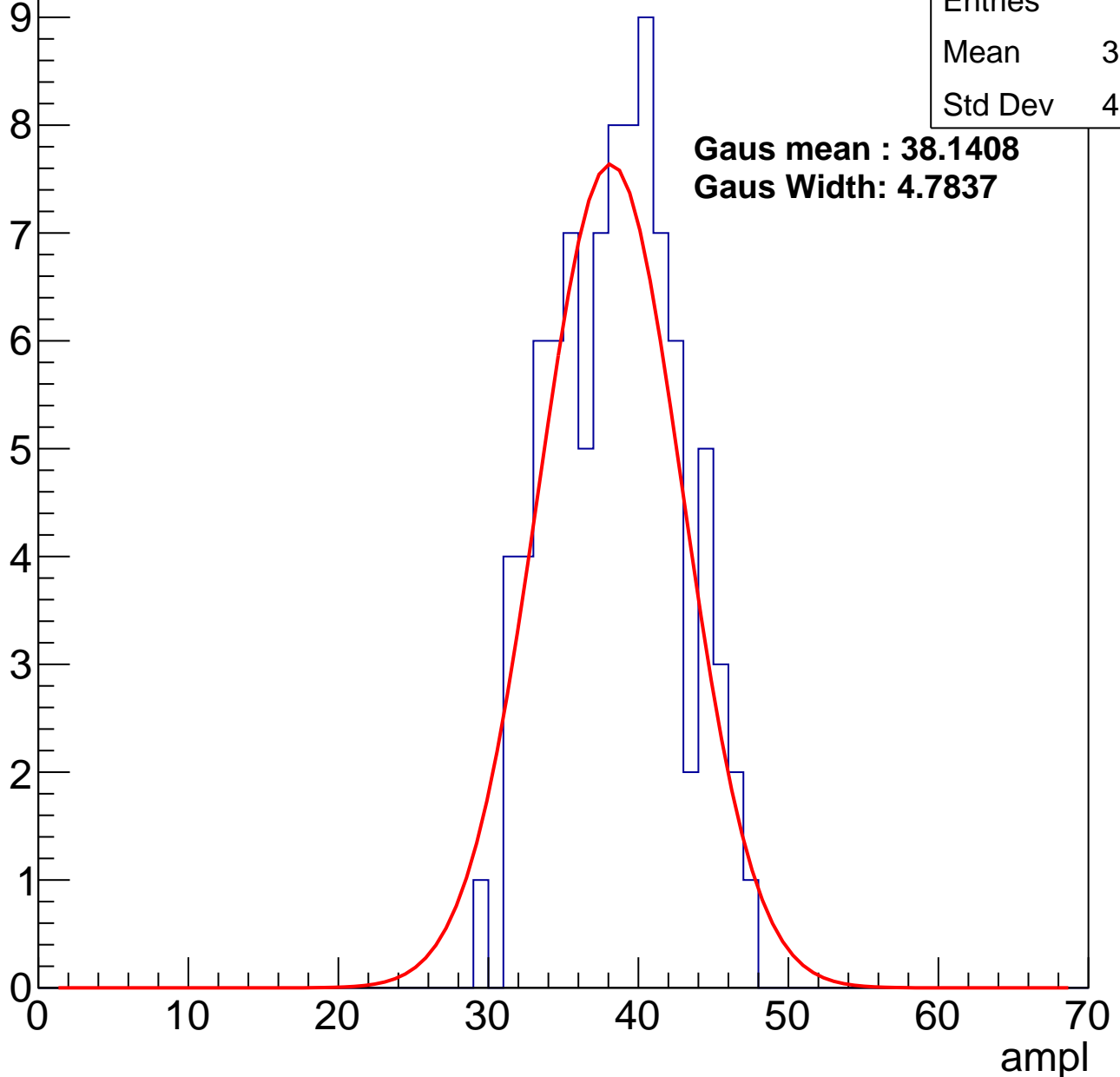
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	91
Mean	38.04
Std Dev	4.122

**Gaus mean : 38.1408**

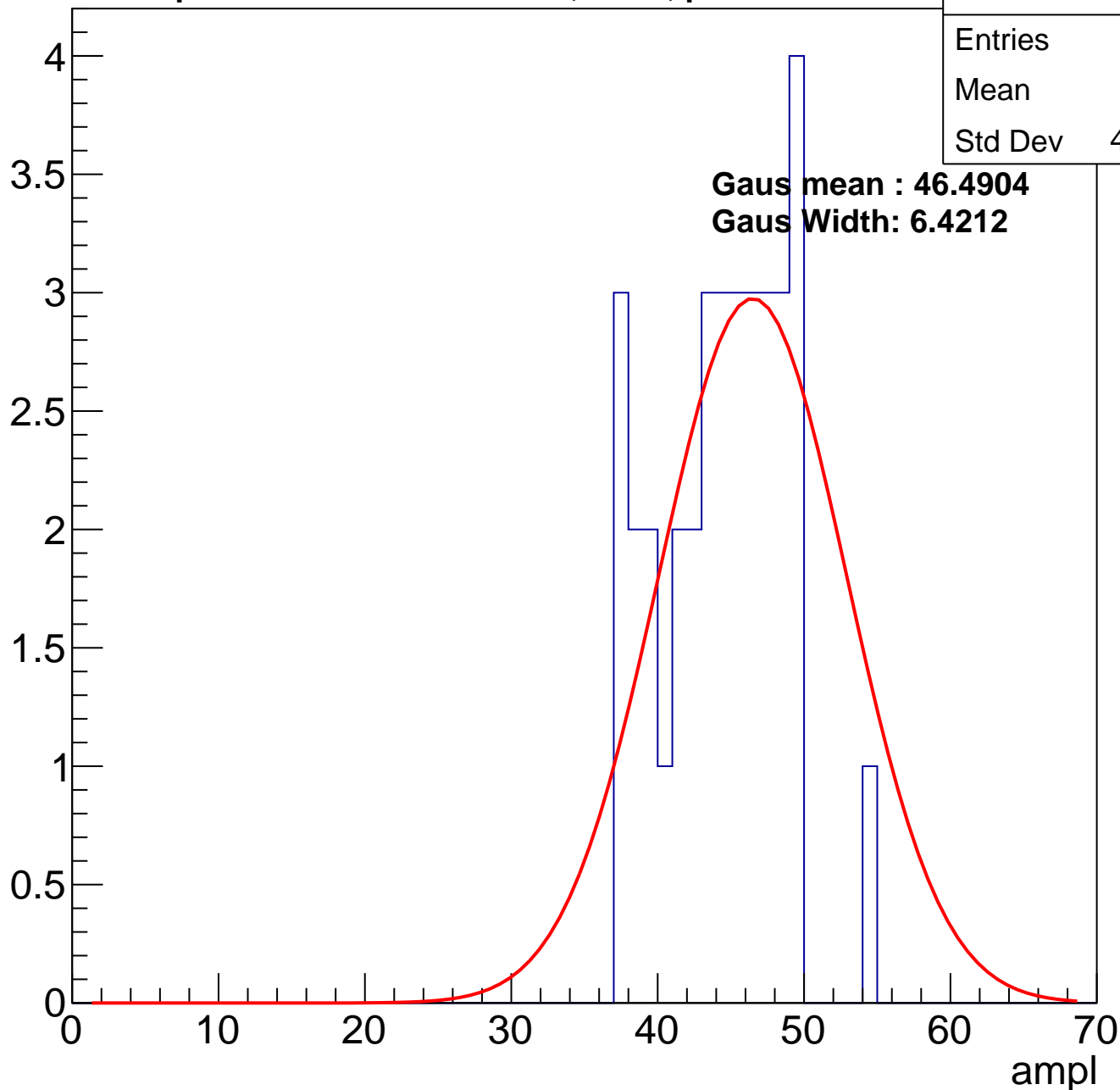
**Gaus Width: 4.7837**



# B1L103S, U9-ch8, adc2

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



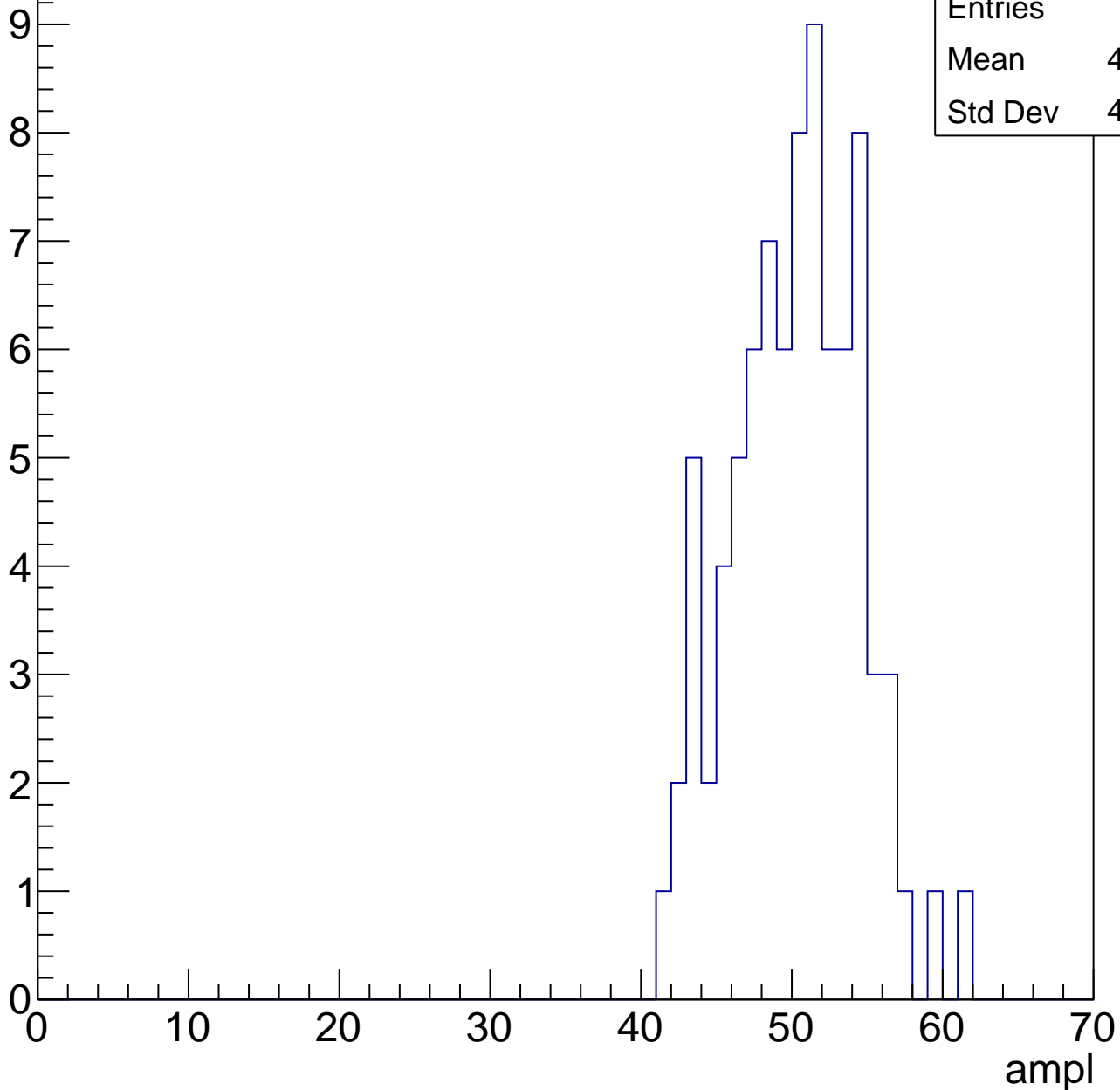
Entries	35
Mean	44
Std Dev	4.154

# B1L103S, U9-ch8, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

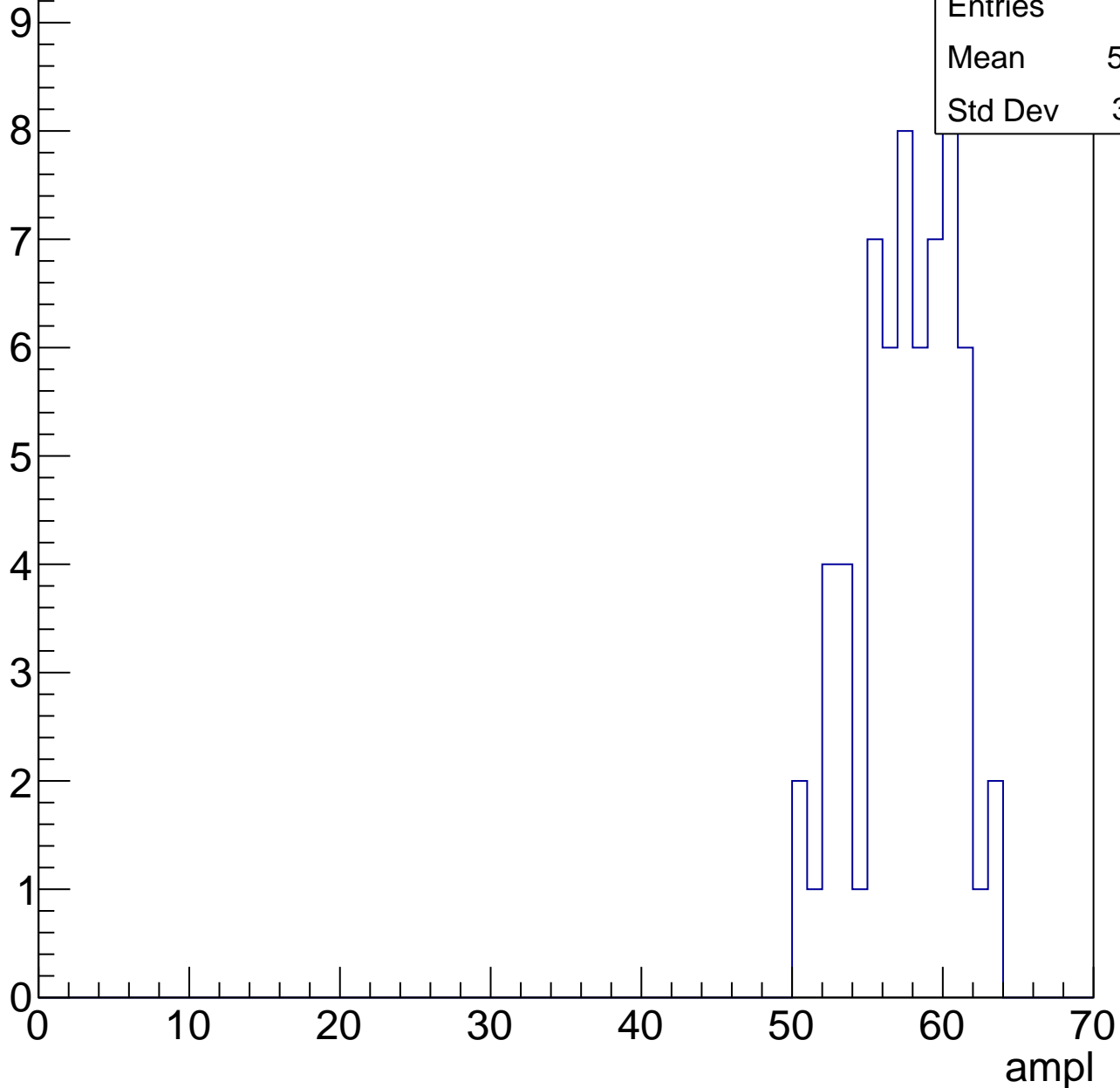
Entries	84
Mean	49.77
Std Dev	4.139



# B1L103S, U9-ch8, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



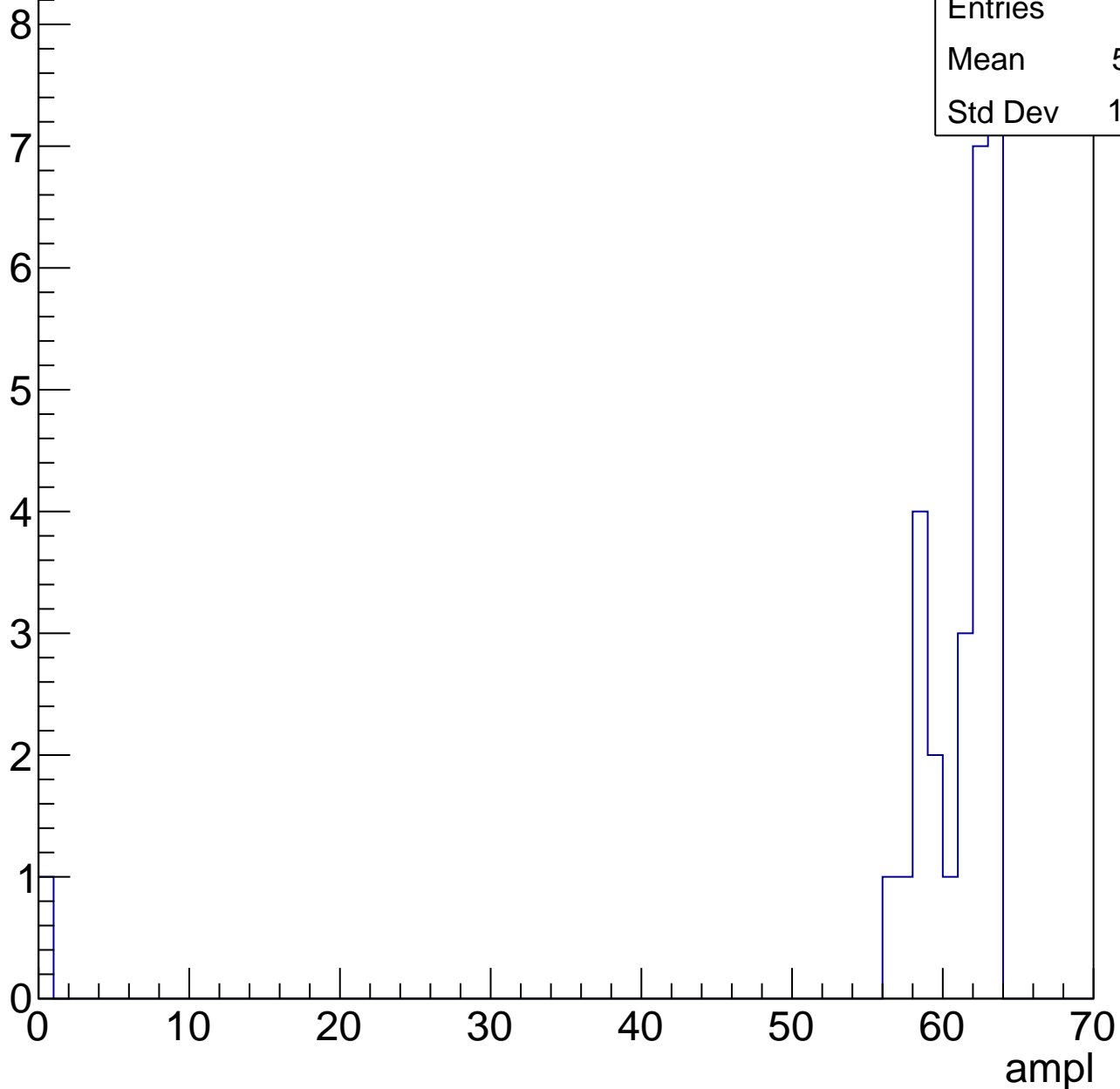
Entries	64
Mean	57.14
Std Dev	3.181

# B1L103S, U9-ch8, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	28
Mean	58.71
Std Dev	11.49



# B1L103S, U9-ch8, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	2
Mean	62
Std Dev	0

ampl



# B1L103S, U9-ch8, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L103S, U9-ch9, adc0

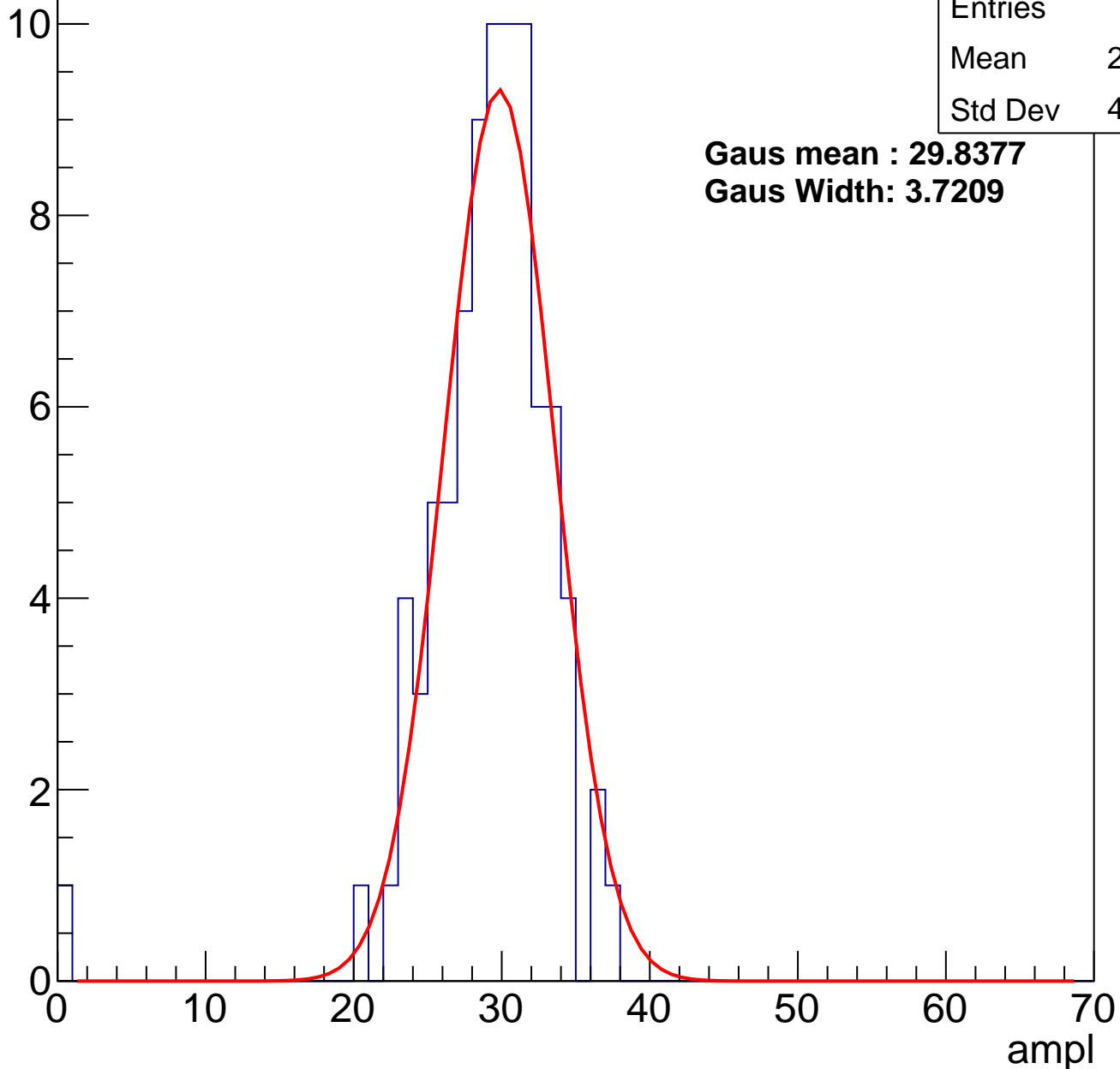
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	85
Mean	28.67
Std Dev	4.608

**Gaus mean : 29.8377**

**Gaus Width: 3.7209**

Entry



# B1L103S, U9-ch9, adc1

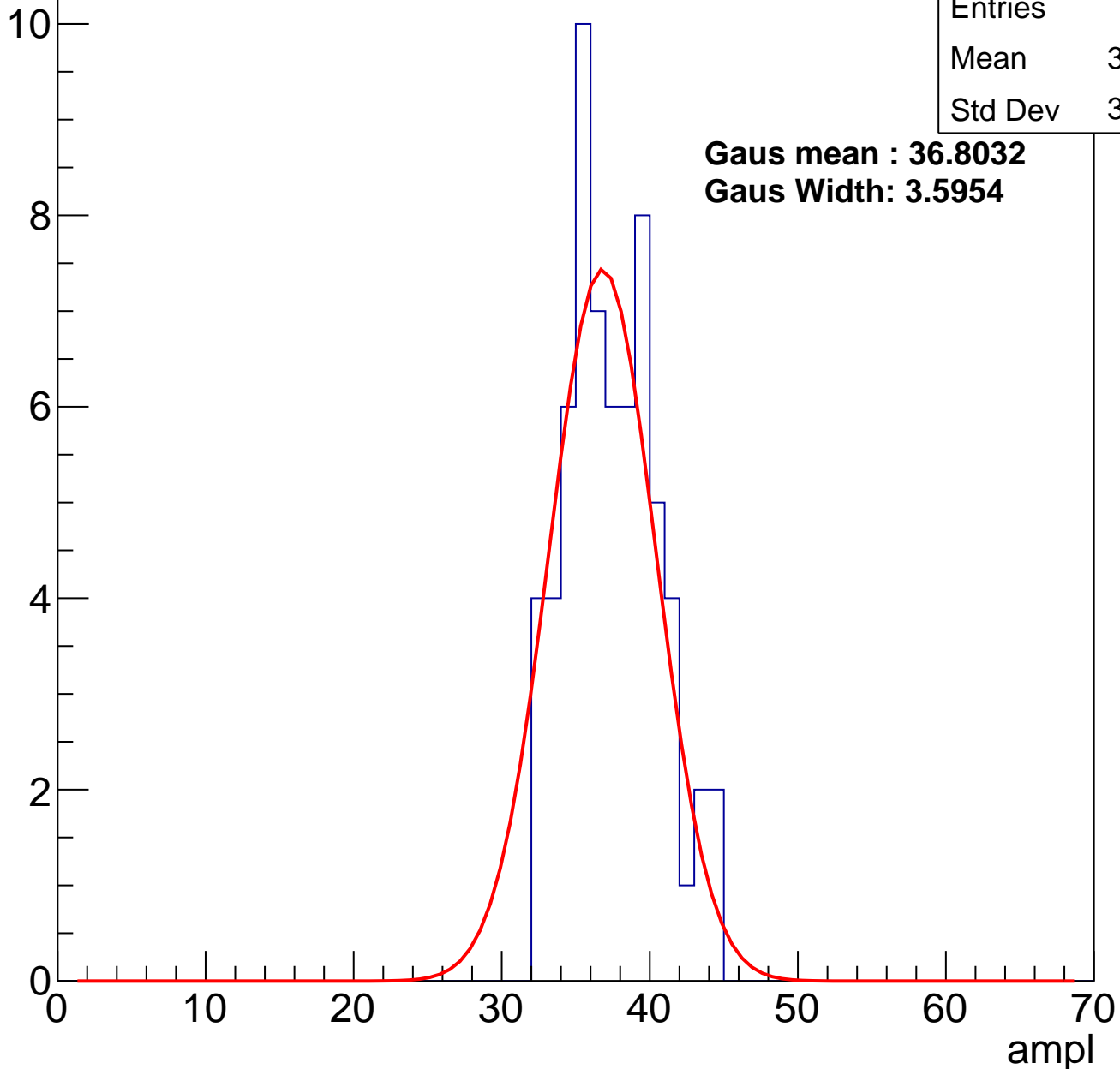
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	65
Mean	37.05
Std Dev	3.056

**Gaus mean : 36.8032**

**Gaus Width: 3.5954**

Entry



# B1L103S, U9-ch9, adc2

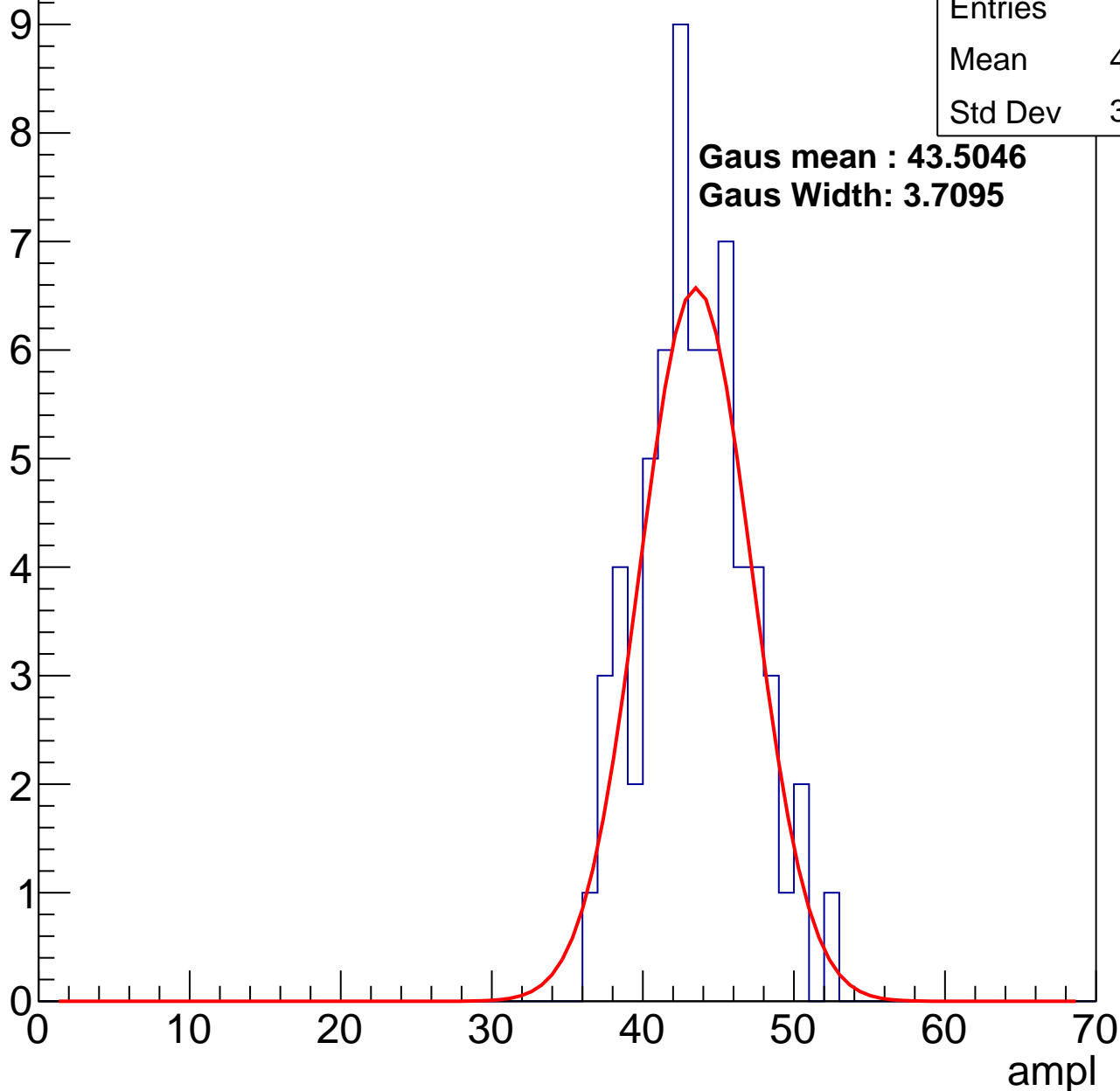
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	43.05
Std Dev	3.515

**Gaus mean : 43.5046**

**Gaus Width: 3.7095**

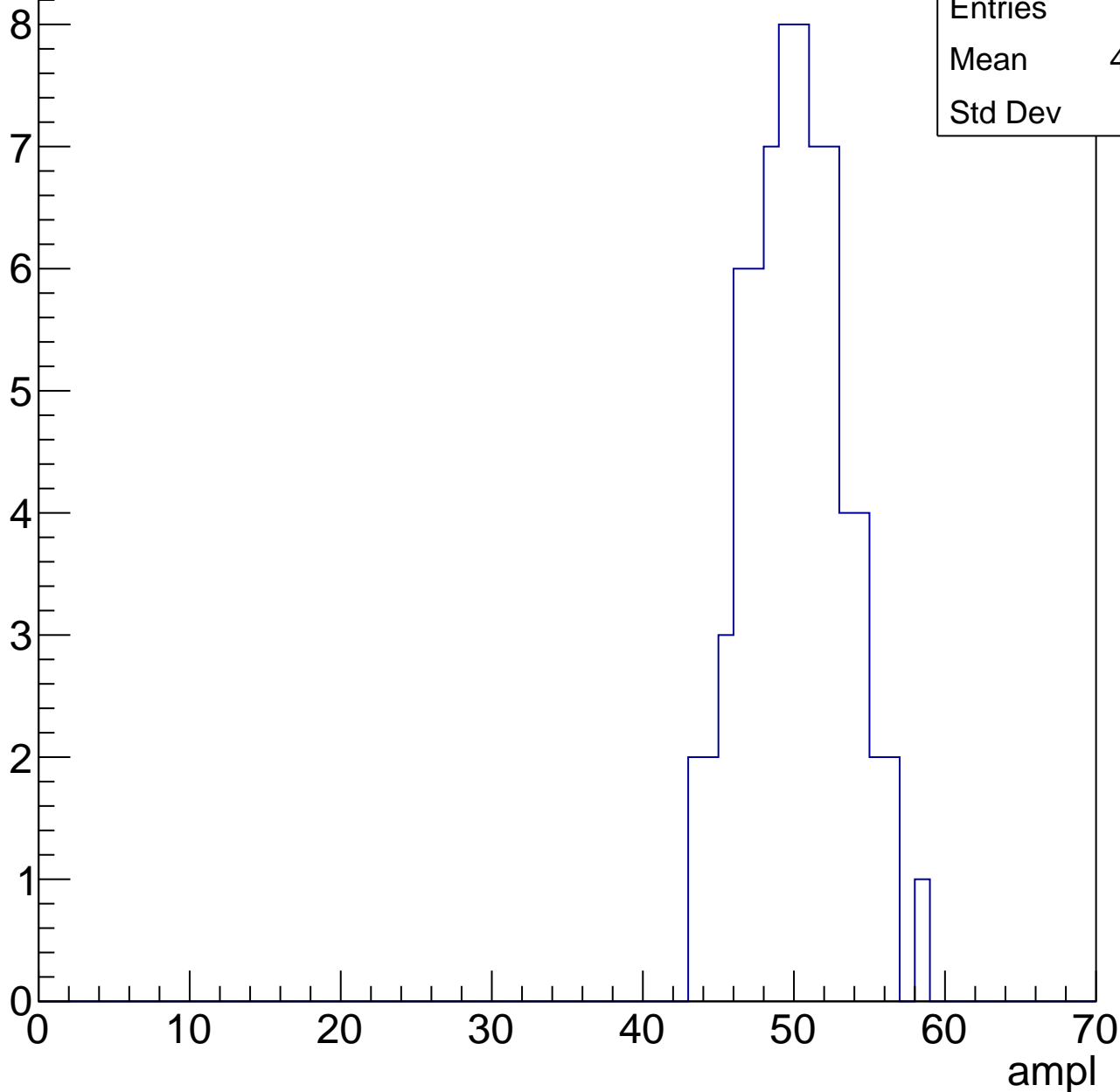


# B1L103S, U9-ch9, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	69
Mean	49.62
Std Dev	3.28

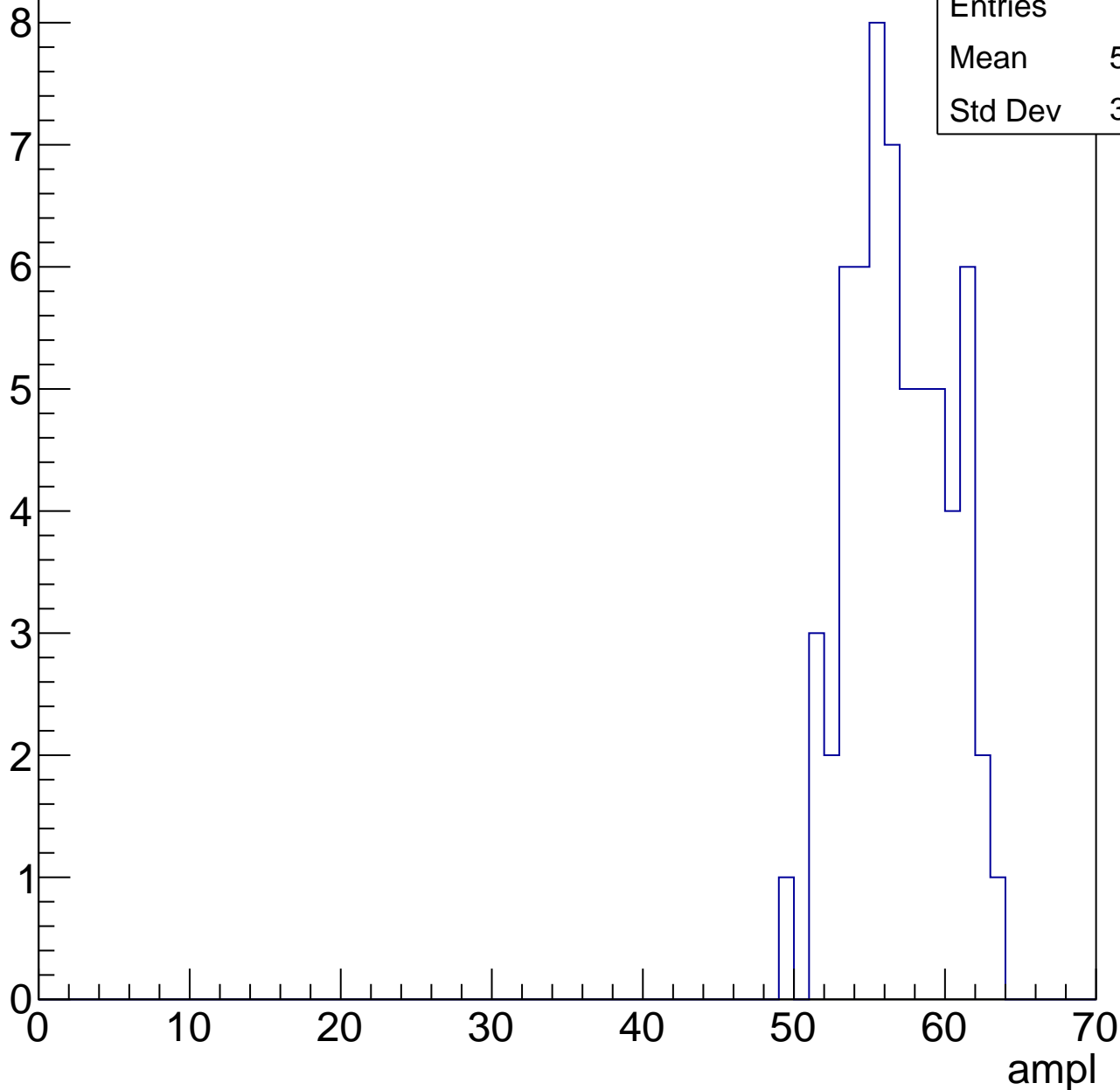


# B1L103S, U9-ch9, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	61
Mean	56.44
Std Dev	3.227

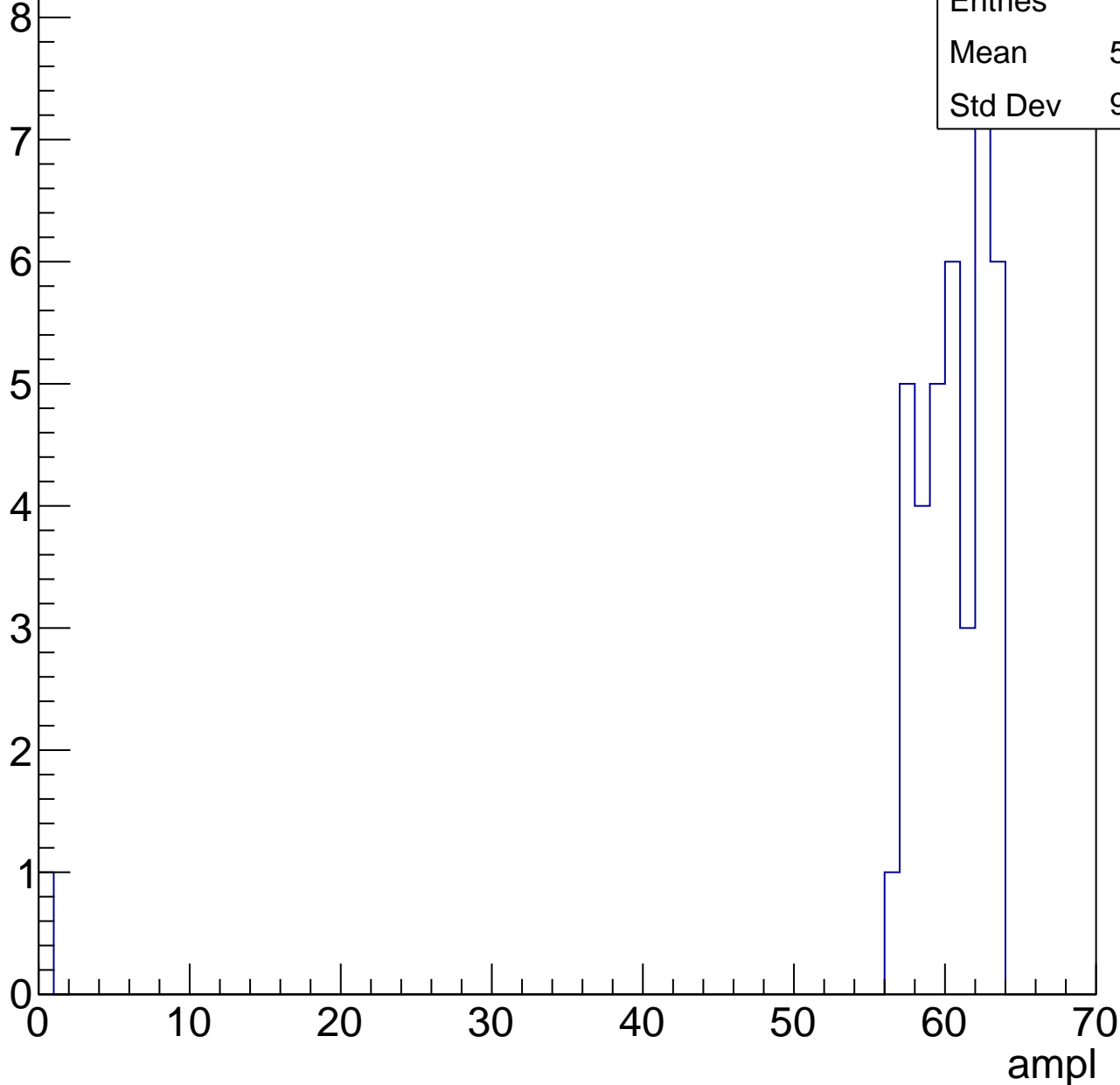


# B1L103S, U9-ch9, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	39
Mean	58.59
Std Dev	9.732



# B1L103S, U9-ch9, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U9-ch9, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U9-ch10, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	93
Mean	28.44
Std Dev	4.913

**Gaus mean : 29.2490**

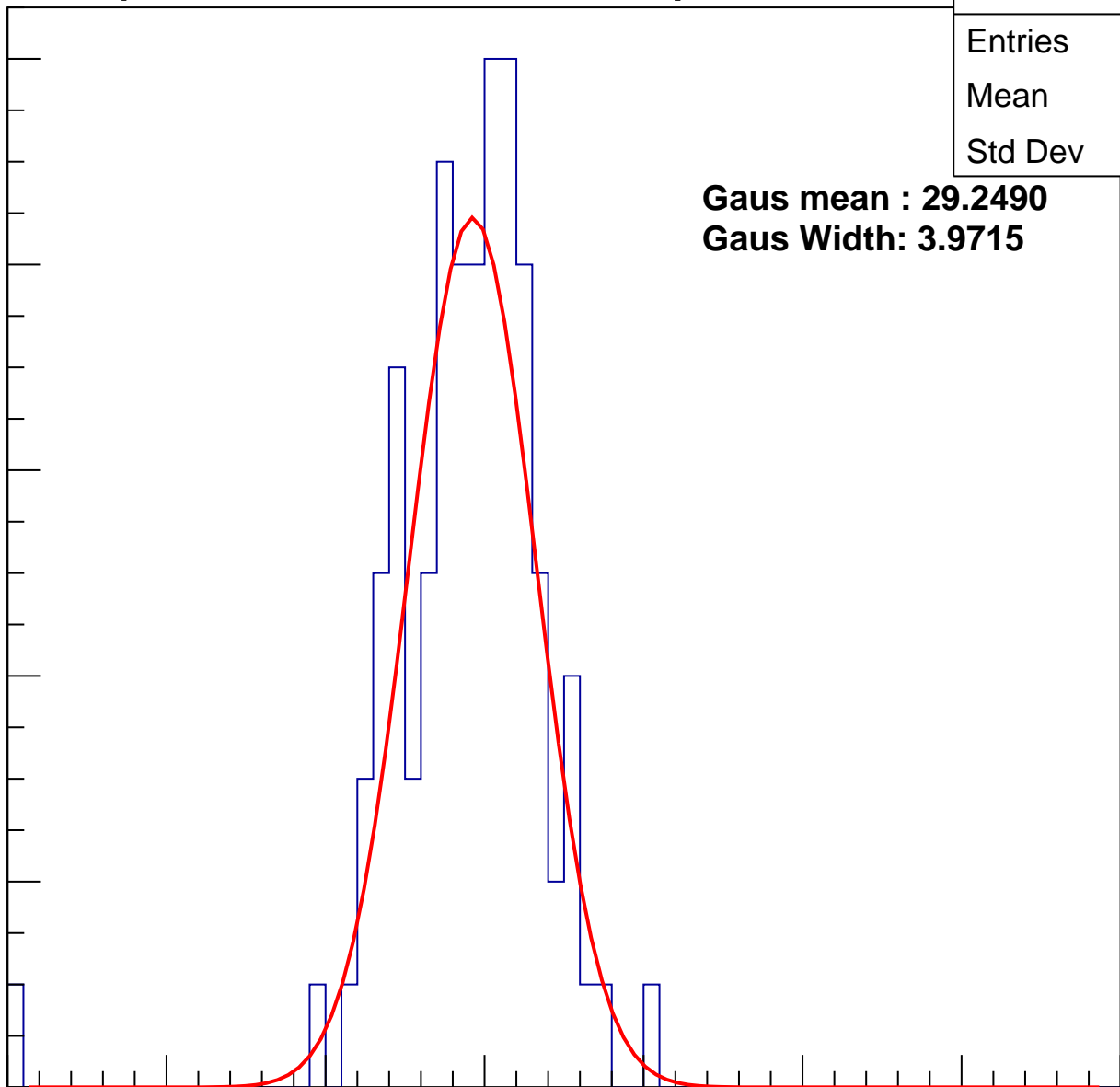
**Gaus Width: 3.9715**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U9-ch10, adc1

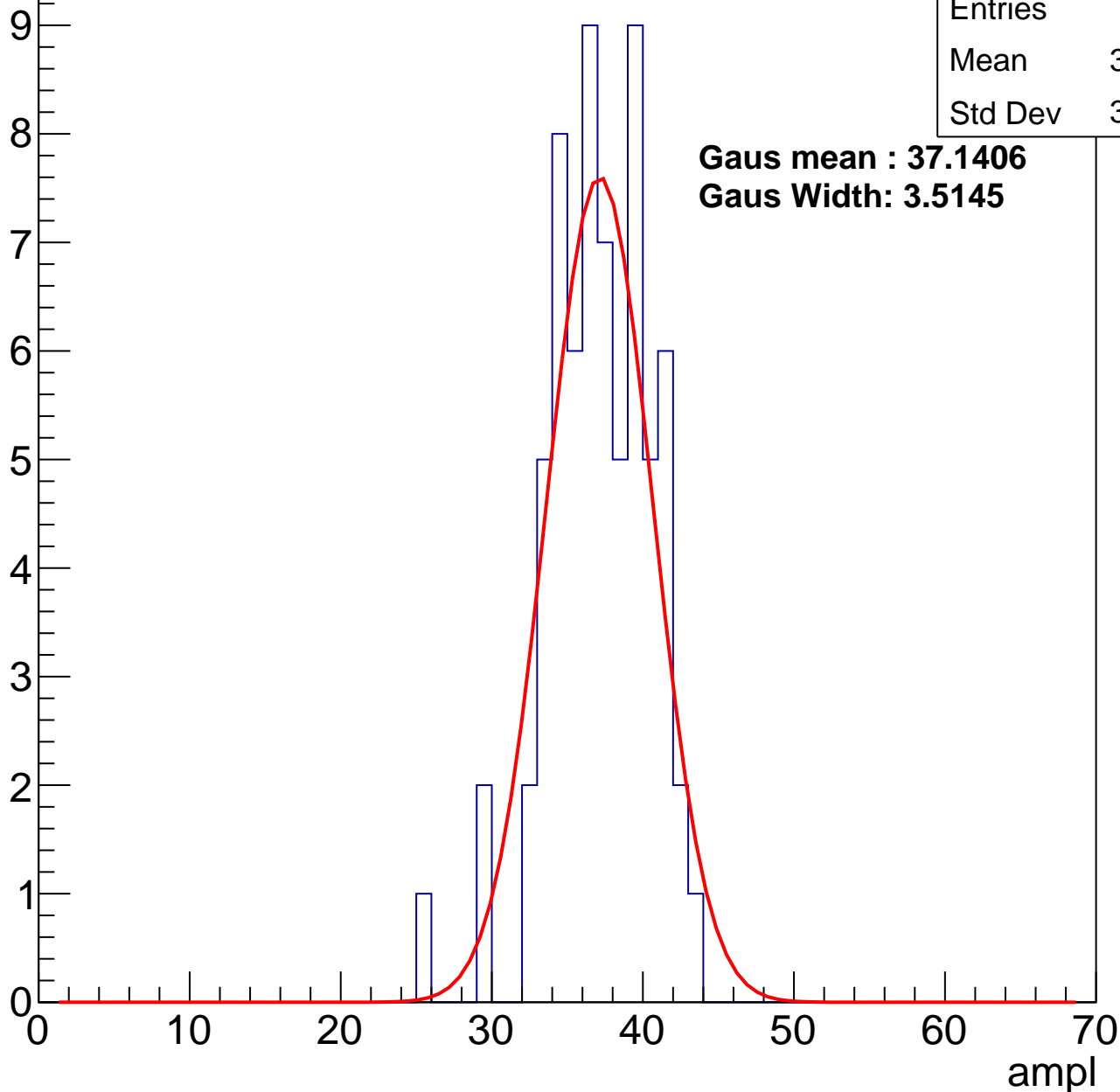
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	68
Mean	36.63
Std Dev	3.356

**Gaus mean : 37.1406**

**Gaus Width: 3.5145**



# B1L103S, U9-ch10, adc2

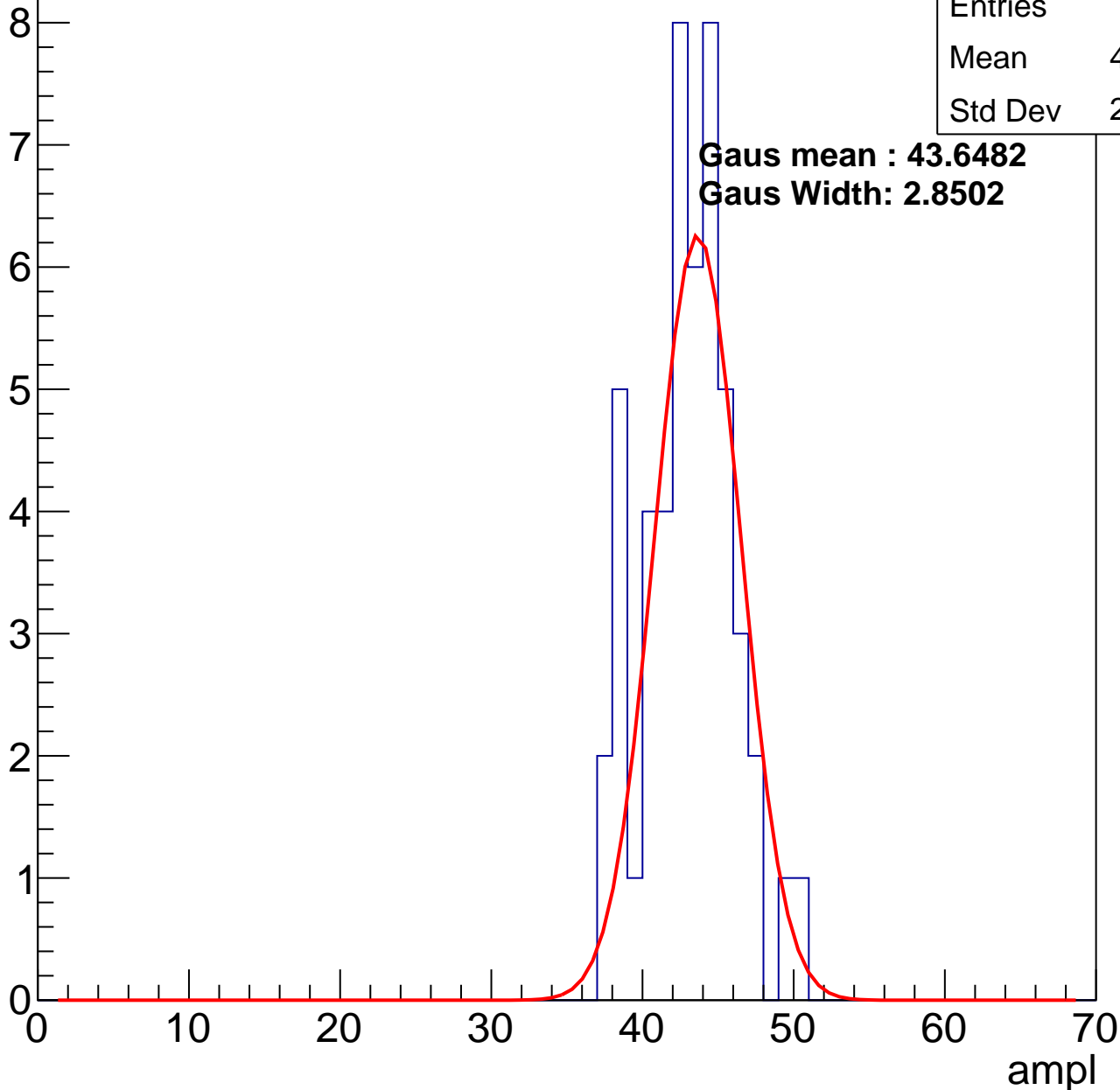
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	50
Mean	42.58
Std Dev	2.954

**Gaus mean : 43.6482**

**Gaus Width: 2.8502**

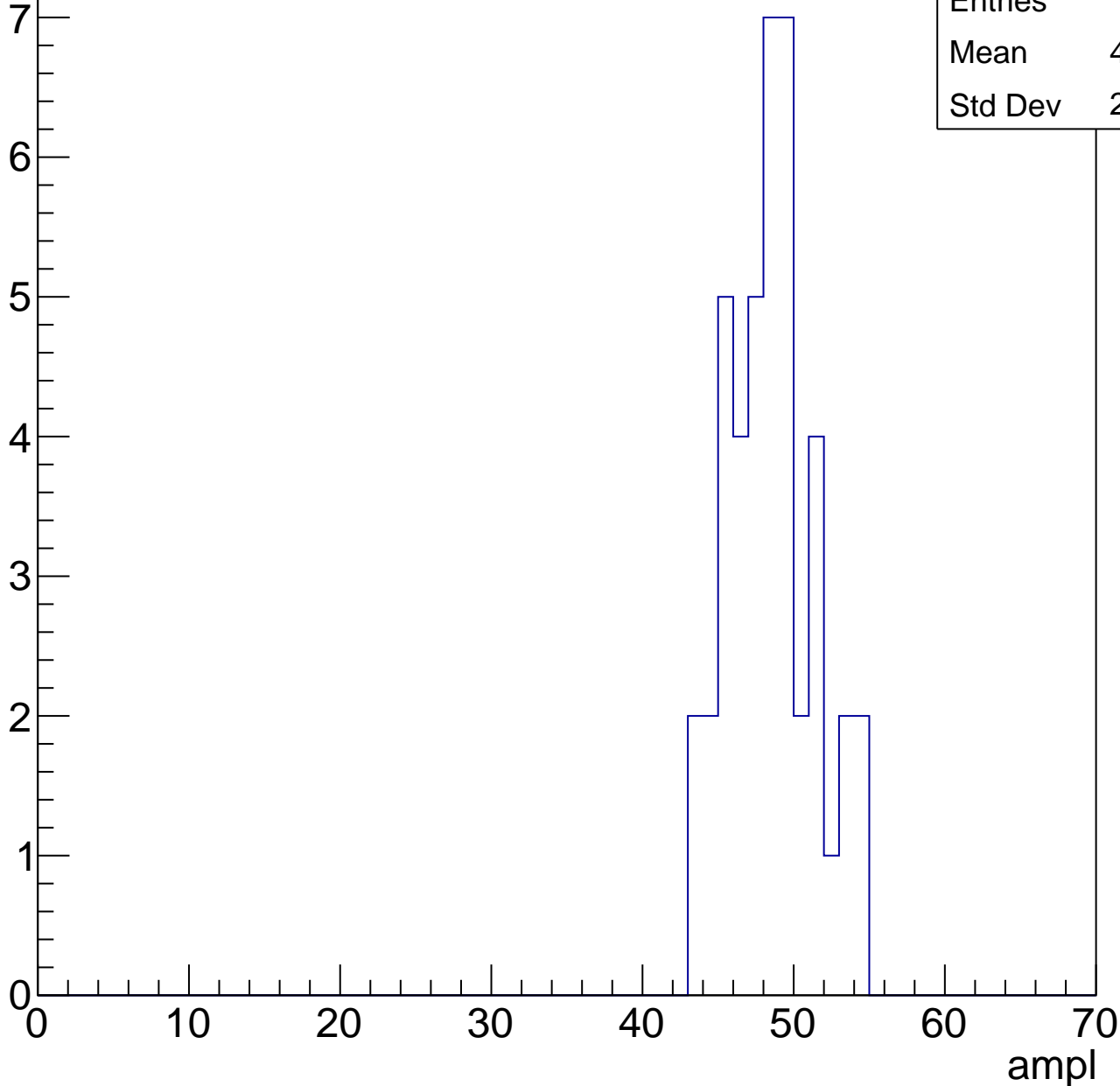


# B1L103S, U9-ch10, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	43
Mean	48.07
Std Dev	2.799

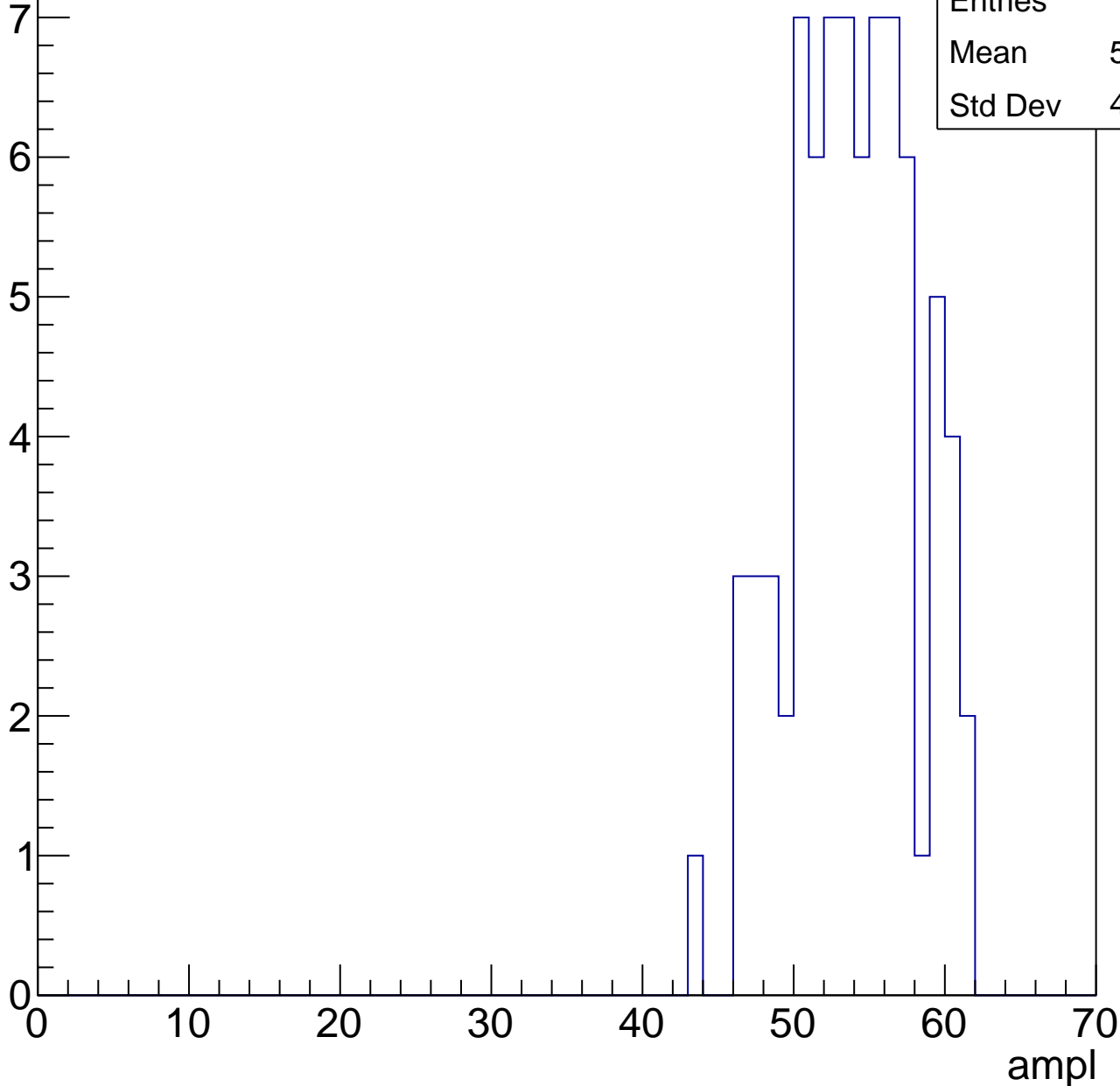


# B1L103S, U9-ch10, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	77
Mean	53.42
Std Dev	4.053



# B1L103S, U9-ch10, adc5

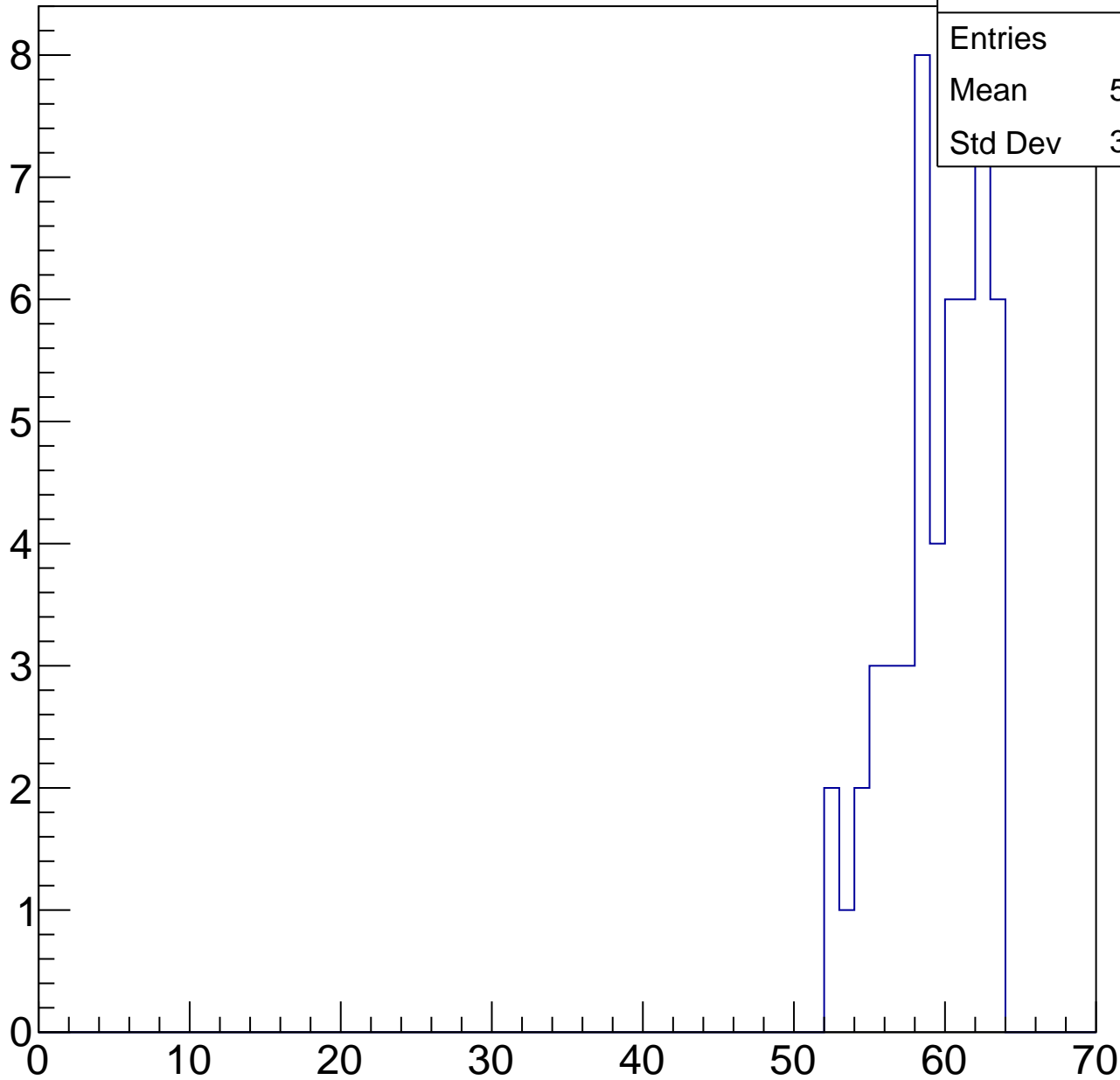
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	52
Mean	59.02
Std Dev	3.029

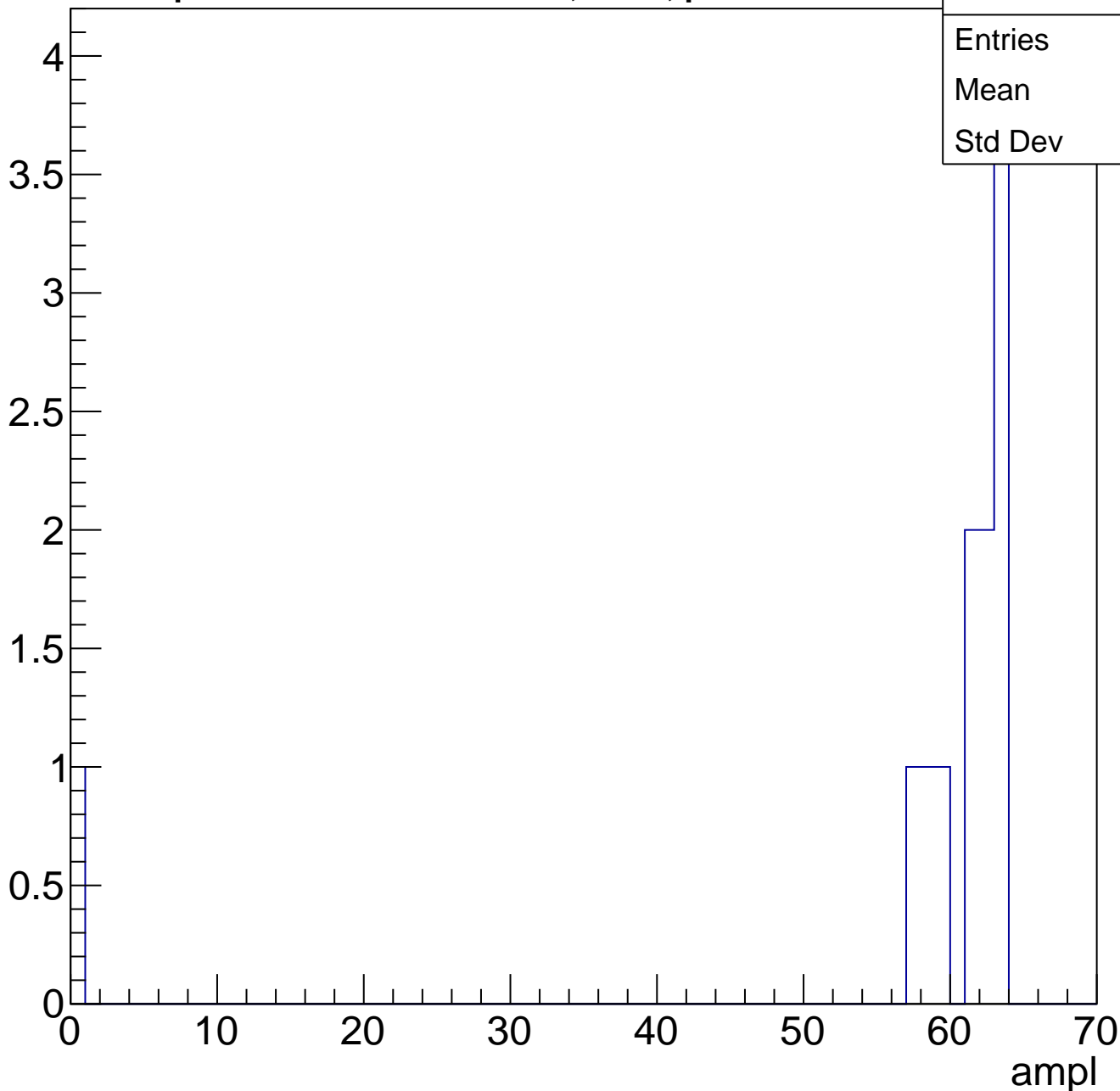
ampl



# B1L103S, U9-ch10, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U9-ch10, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	3
Mean	6.333
Std Dev	8.957

# B1L103S, U9-ch11, adc0

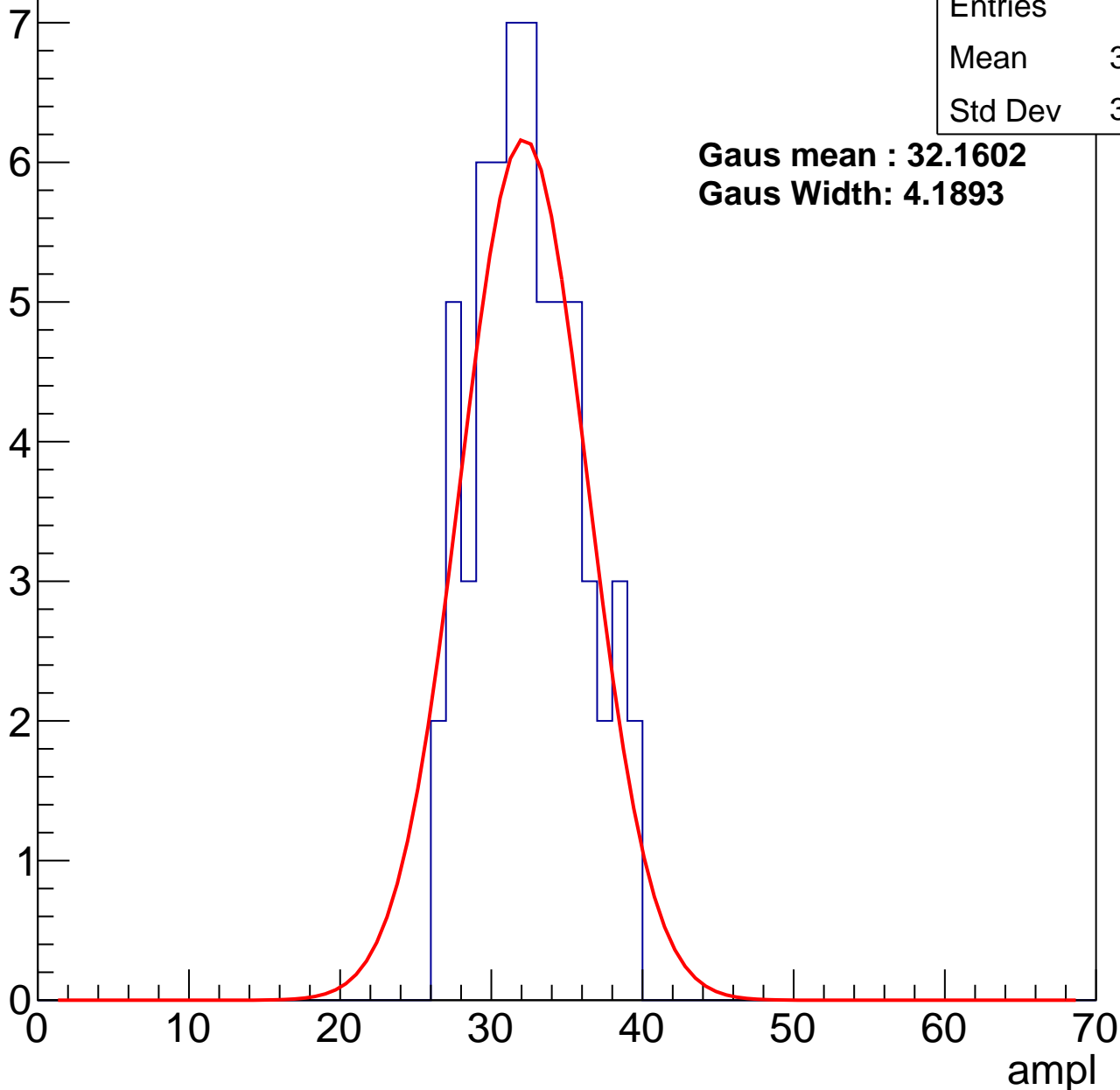
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	61
Mean	31.97
Std Dev	3.397

**Gaus mean : 32.1602**

**Gaus Width: 4.1893**



# B1L103S, U9-ch11, adc1

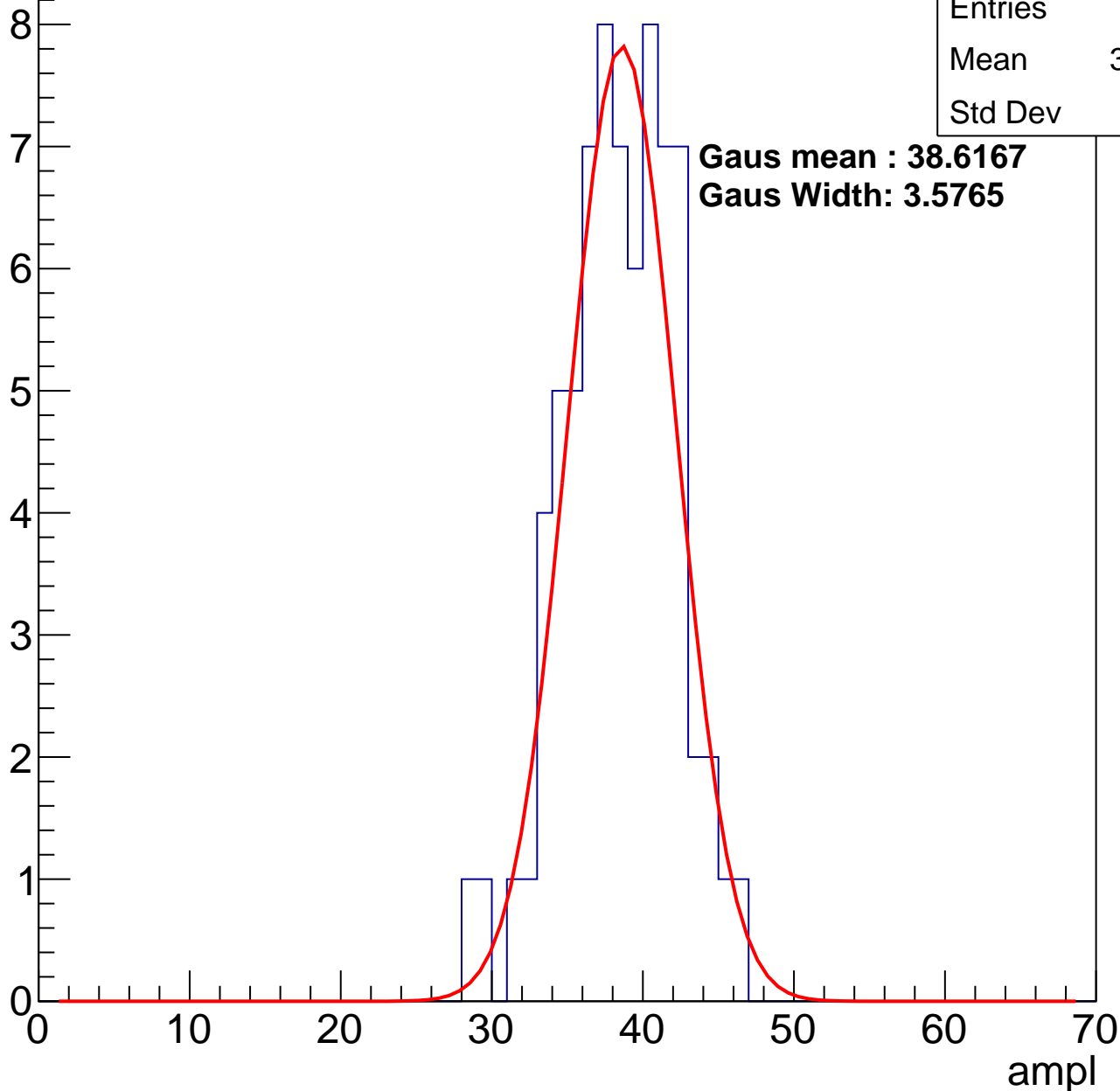
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	74
Mean	37.99
Std Dev	3.63

**Gaus mean : 38.6167**

**Gaus Width: 3.5765**



# B1L103S, U9-ch11, adc2

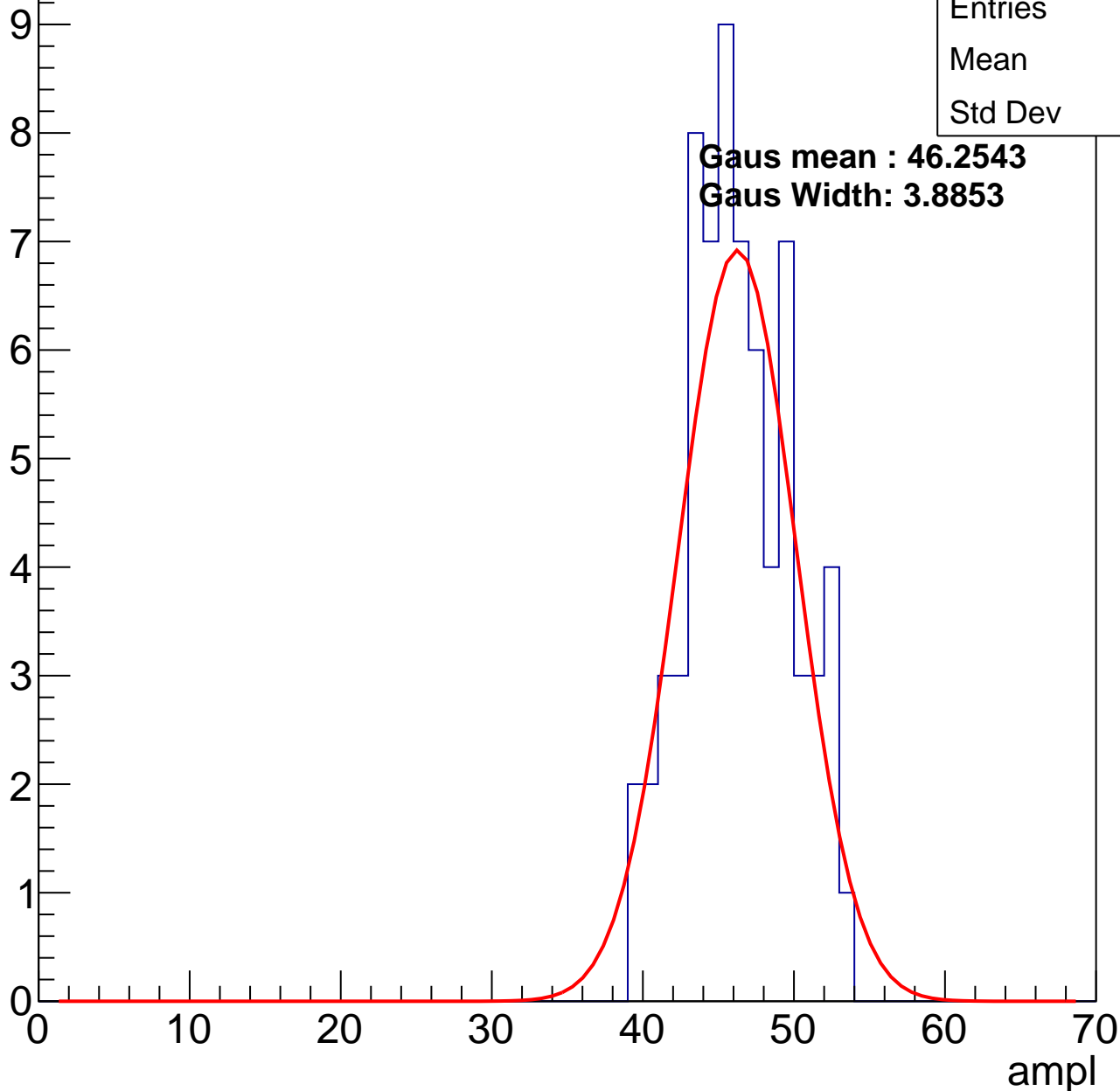
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	69
Mean	45.9
Std Dev	3.41

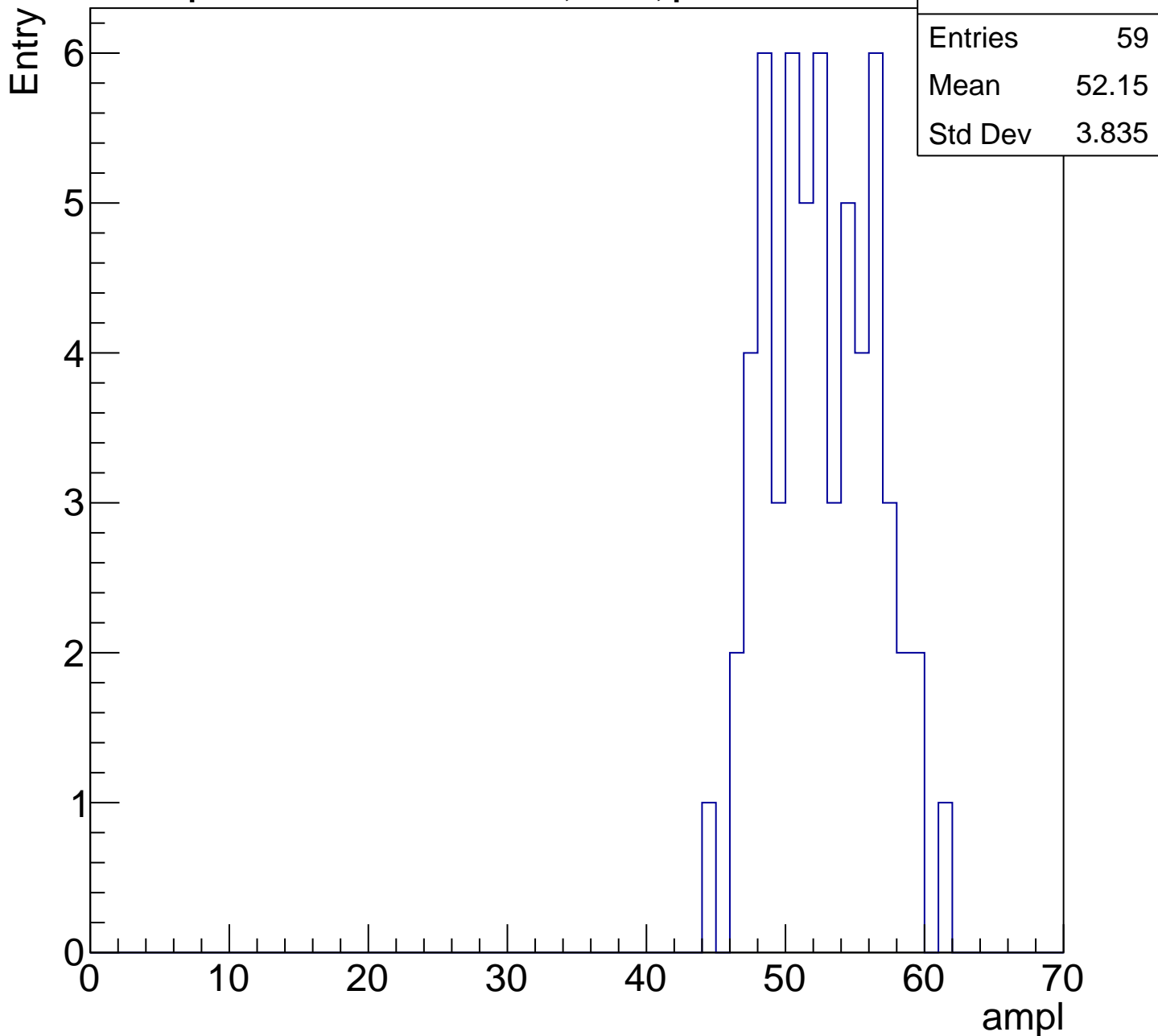
**Gaus mean : 46.2543**

**Gaus Width: 3.8853**



# B1L103S, U9-ch11, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

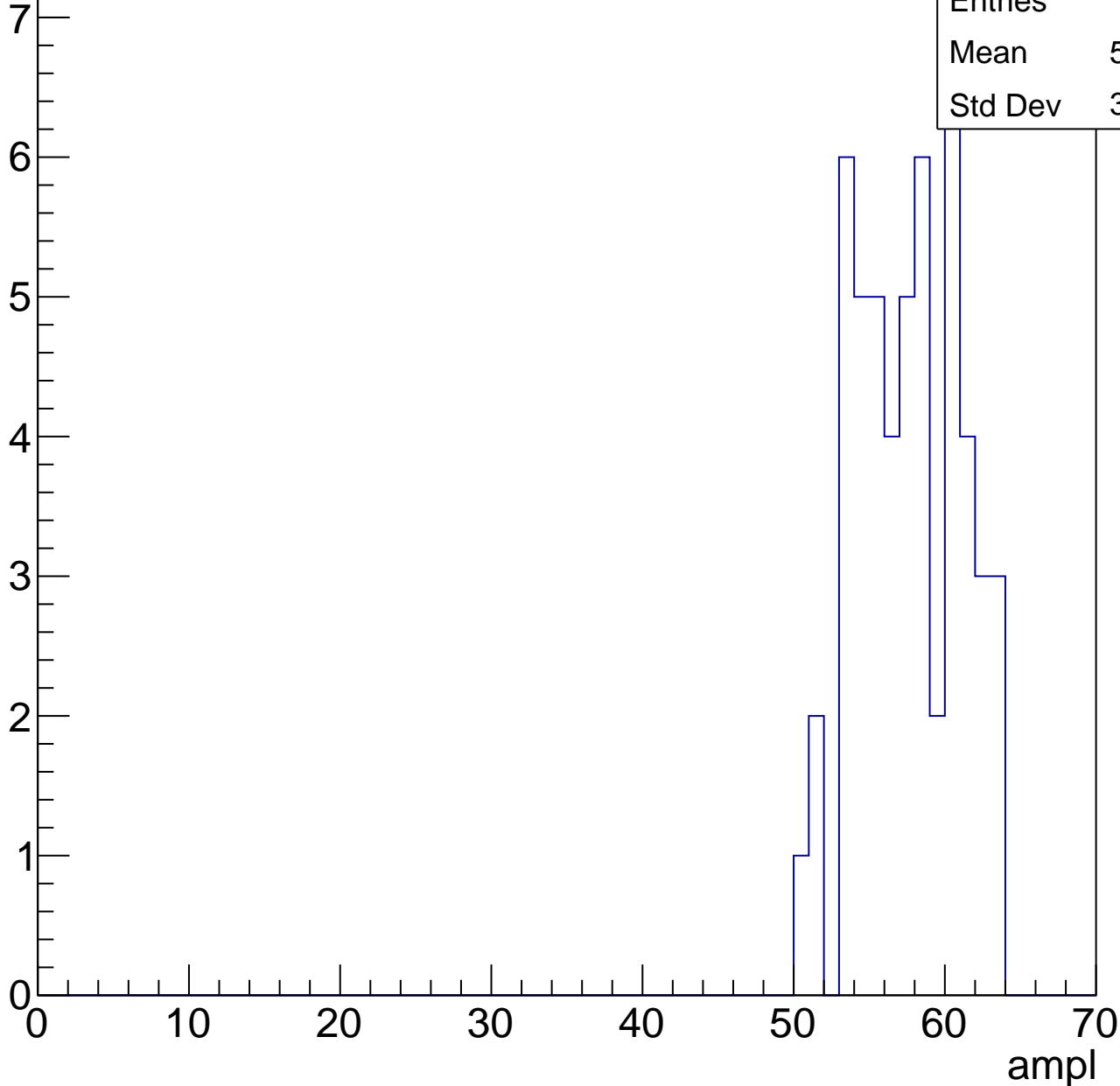


# B1L103S, U9-ch11, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	53
Mean	57.15
Std Dev	3.389

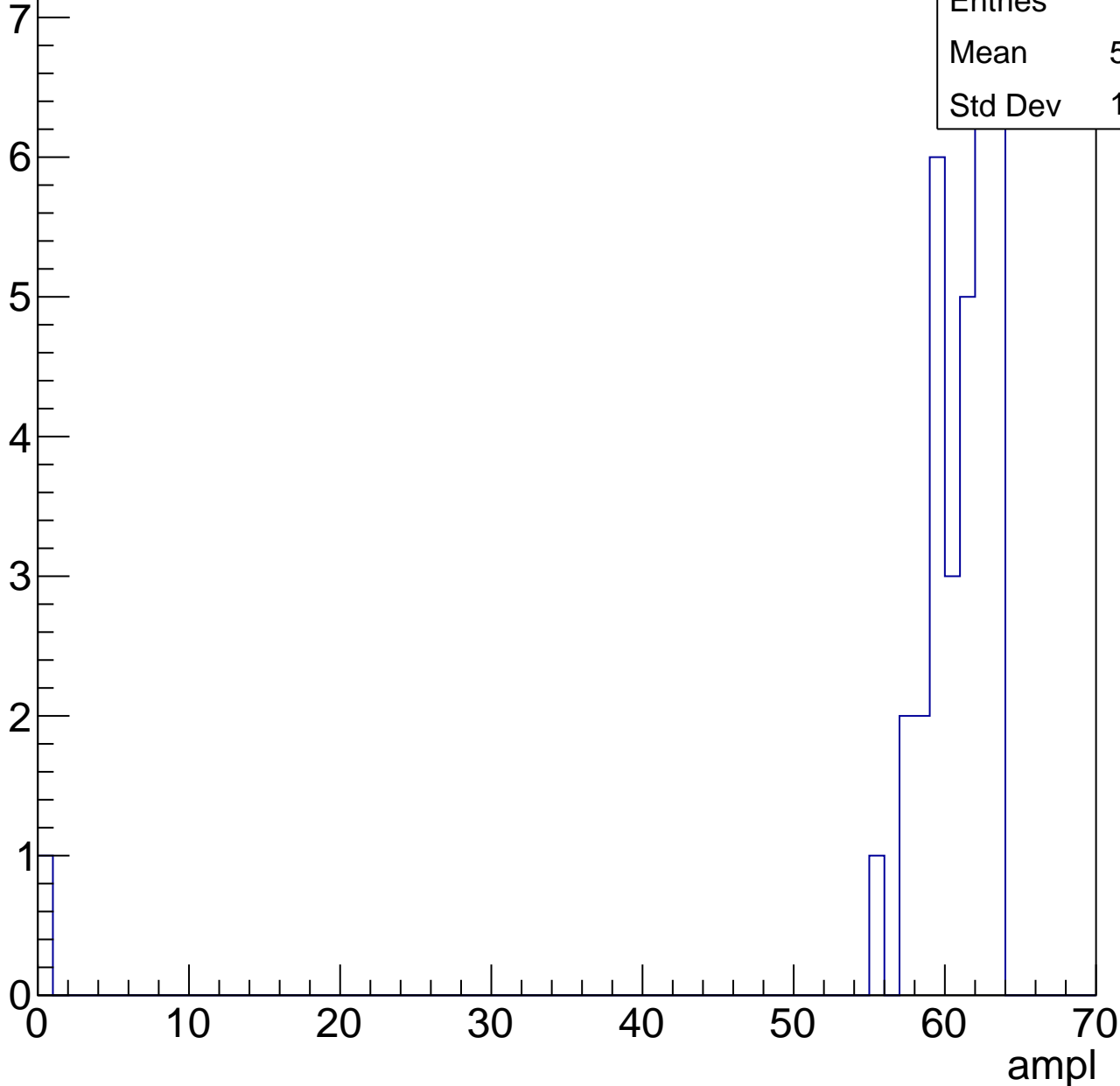


# B1L103S, U9-ch11, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	34
Mean	58.79
Std Dev	10.44



# B1L103S, U9-ch11, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



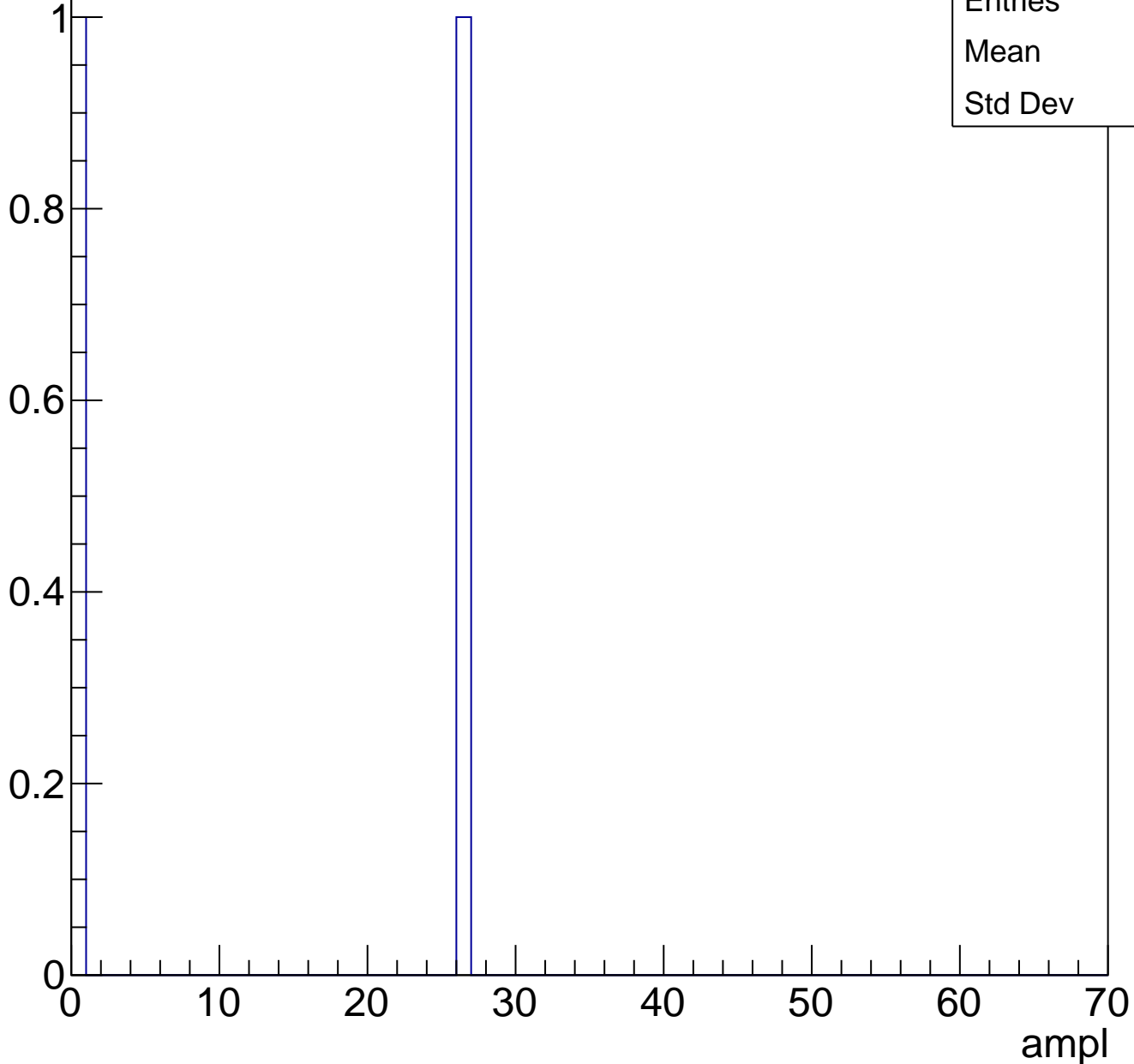
Entries	0
Mean	0
Std Dev	0



# B1L103S, U9-ch11, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	2
Mean	13
Std Dev	13

# B1L103S, U9-ch12, adc0

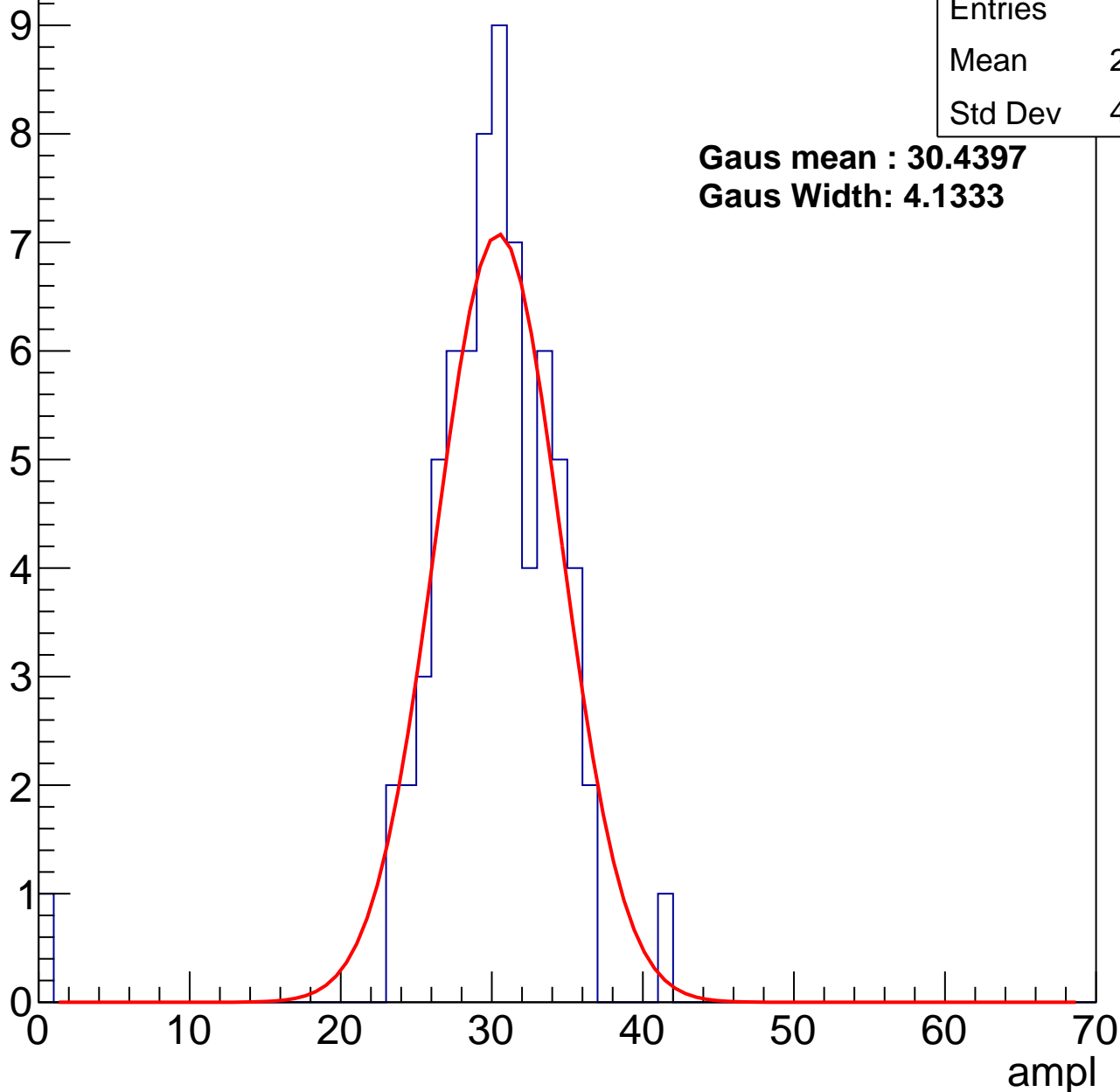
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	71
Mean	29.54
Std Dev	4.959

**Gaus mean : 30.4397**

**Gaus Width: 4.1333**



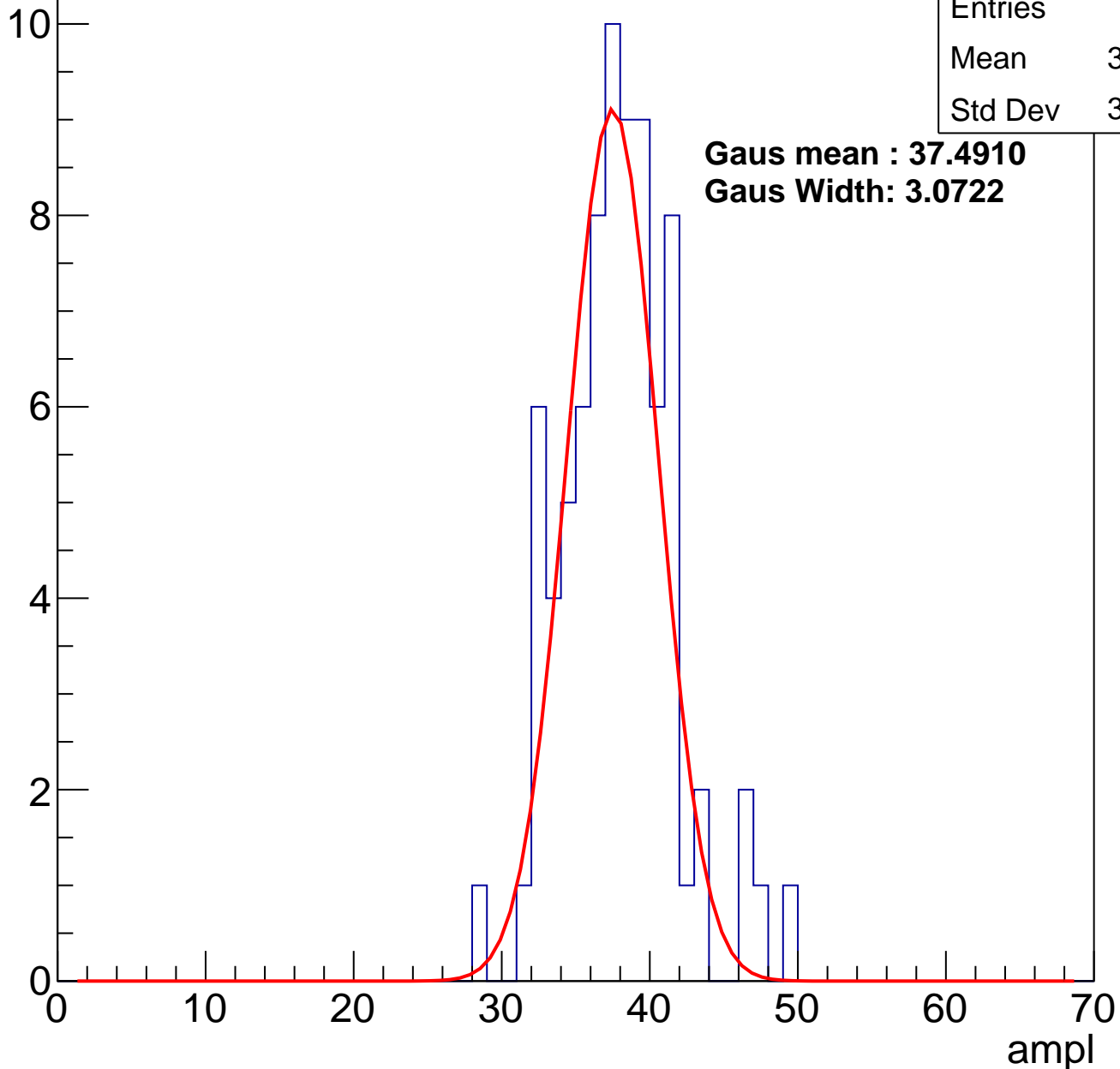
# B1L103S, U9-ch12, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	80
Mean	37.48
Std Dev	3.742

**Gaus mean : 37.4910**  
**Gaus Width: 3.0722**

Entry



# B1L103S, U9-ch12, adc2

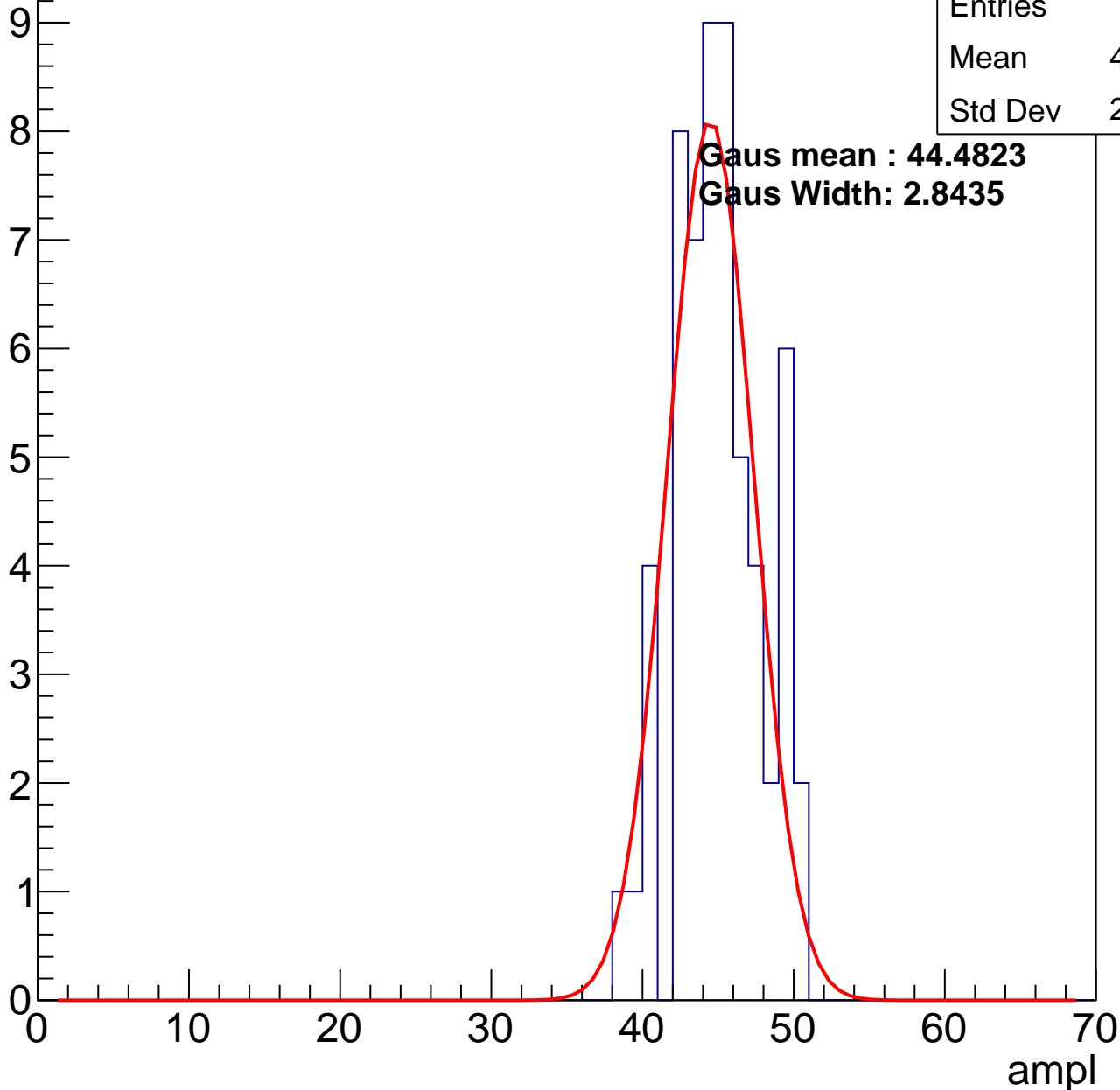
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	58
Mean	44.53
Std Dev	2.836

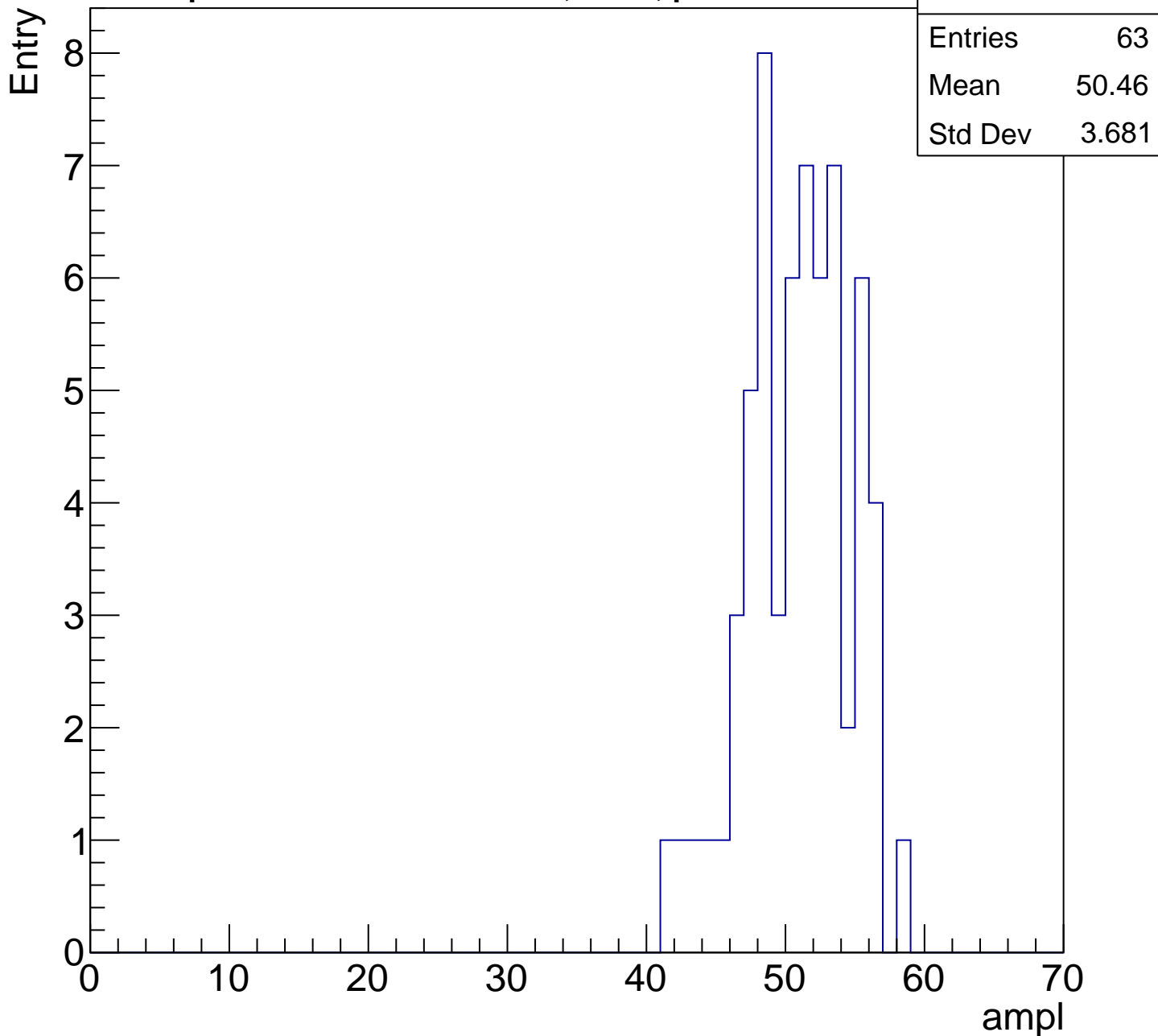
**Gaus mean : 44.4823**

**Gaus Width: 2.8435**



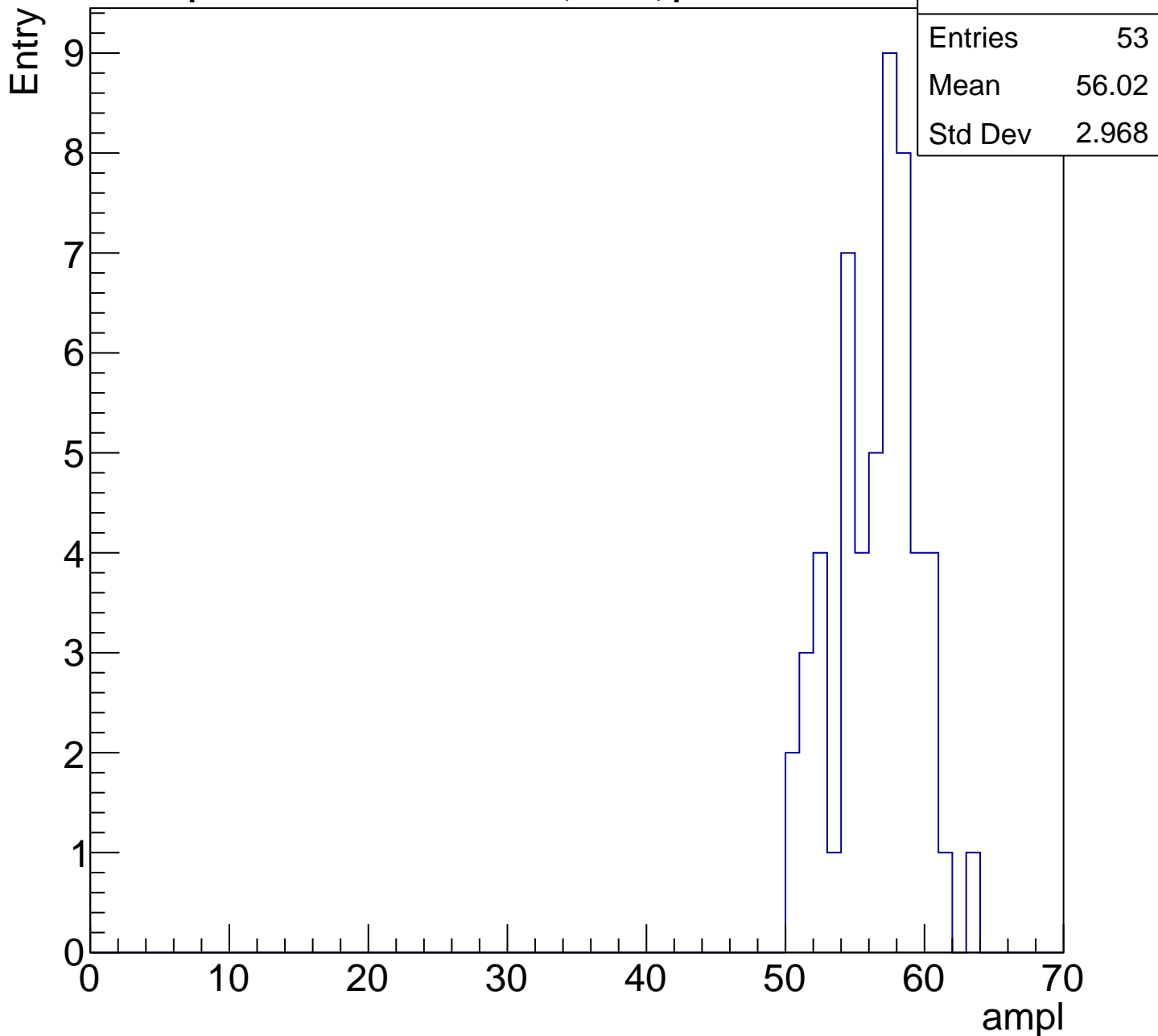
# B1L103S, U9-ch12, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U9-ch12, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

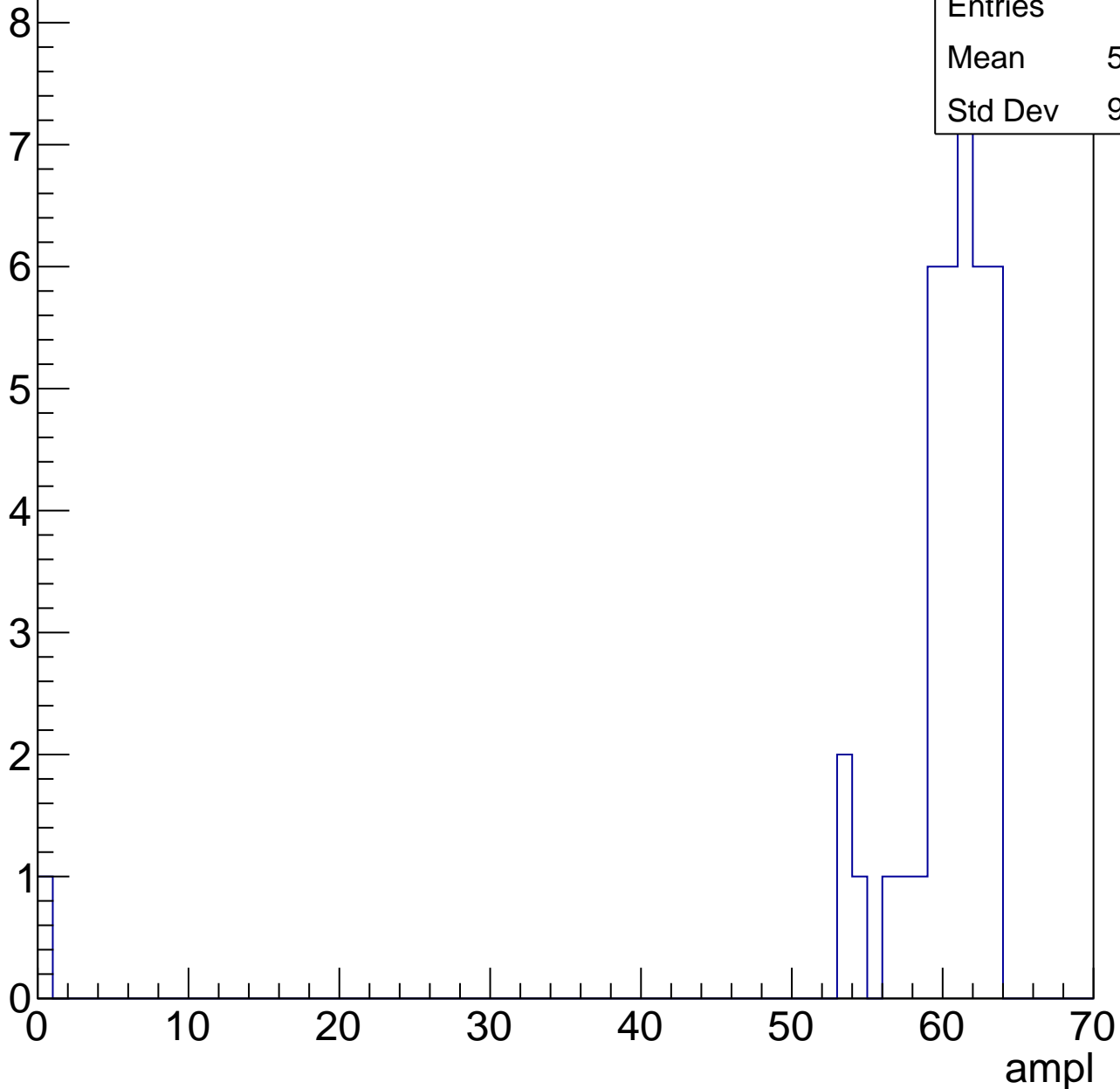


# B1L103S, U9-ch12, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

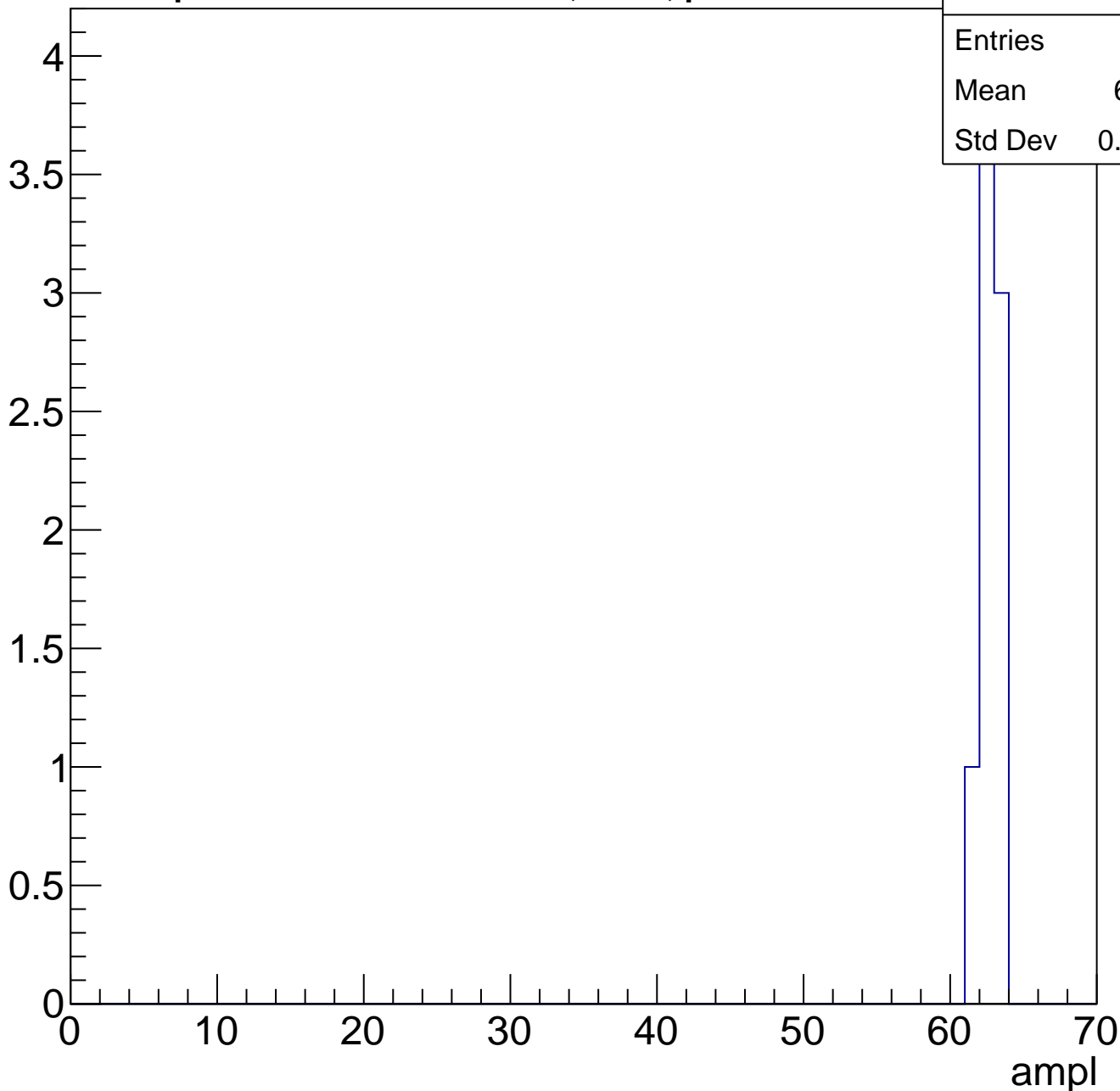
Entries	39
Mean	58.54
Std Dev	9.834



# B1L103S, U9-ch12, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U9-ch12, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

1  
0.8  
0.6  
0.4  
0.2  
0

Entries	1
Mean	23
Std Dev	0

ampl

# B1L103S, U9-ch13, adc0

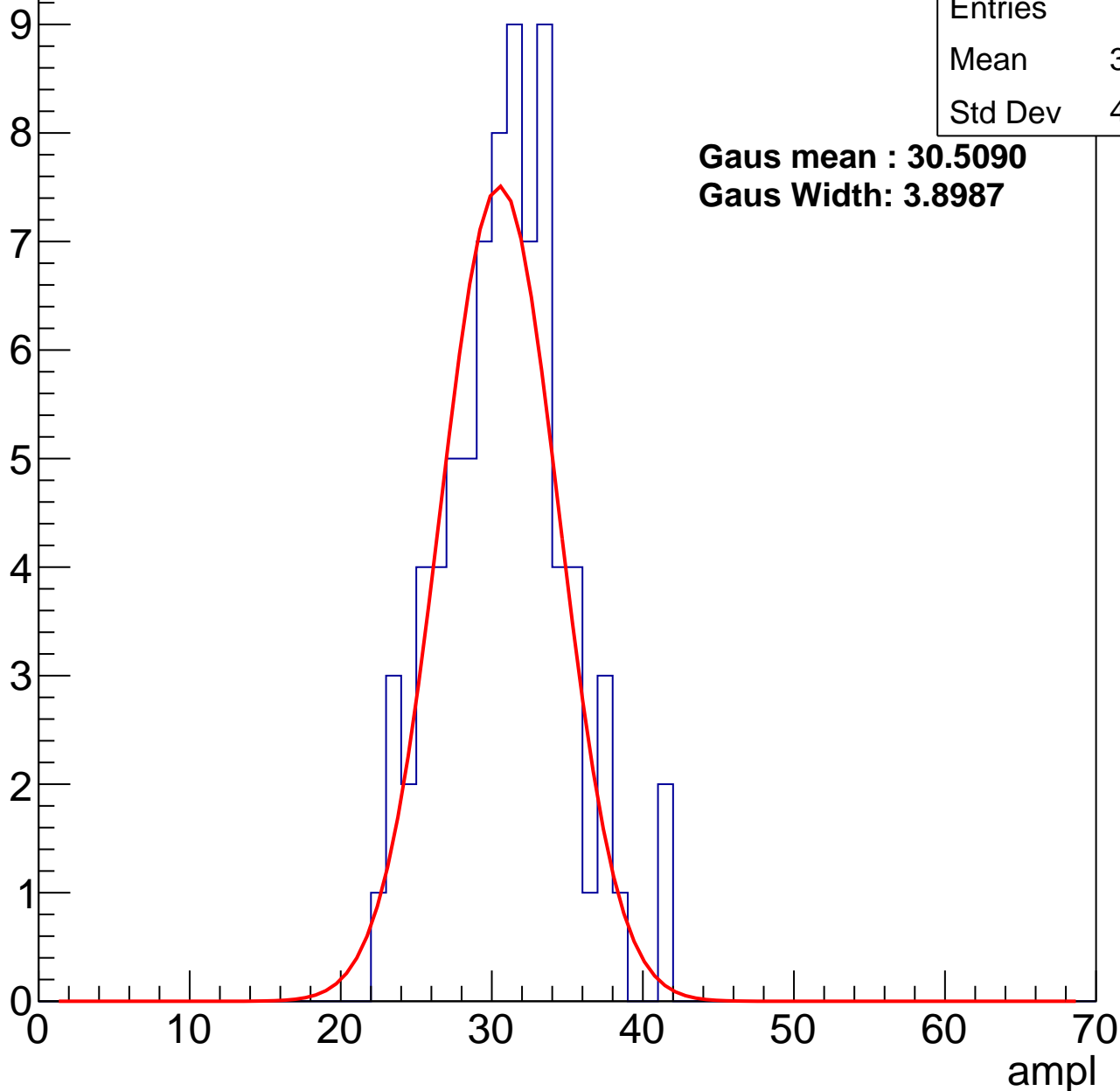
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	79
Mean	30.43
Std Dev	4.018

**Gaus mean : 30.5090**

**Gaus Width: 3.8987**



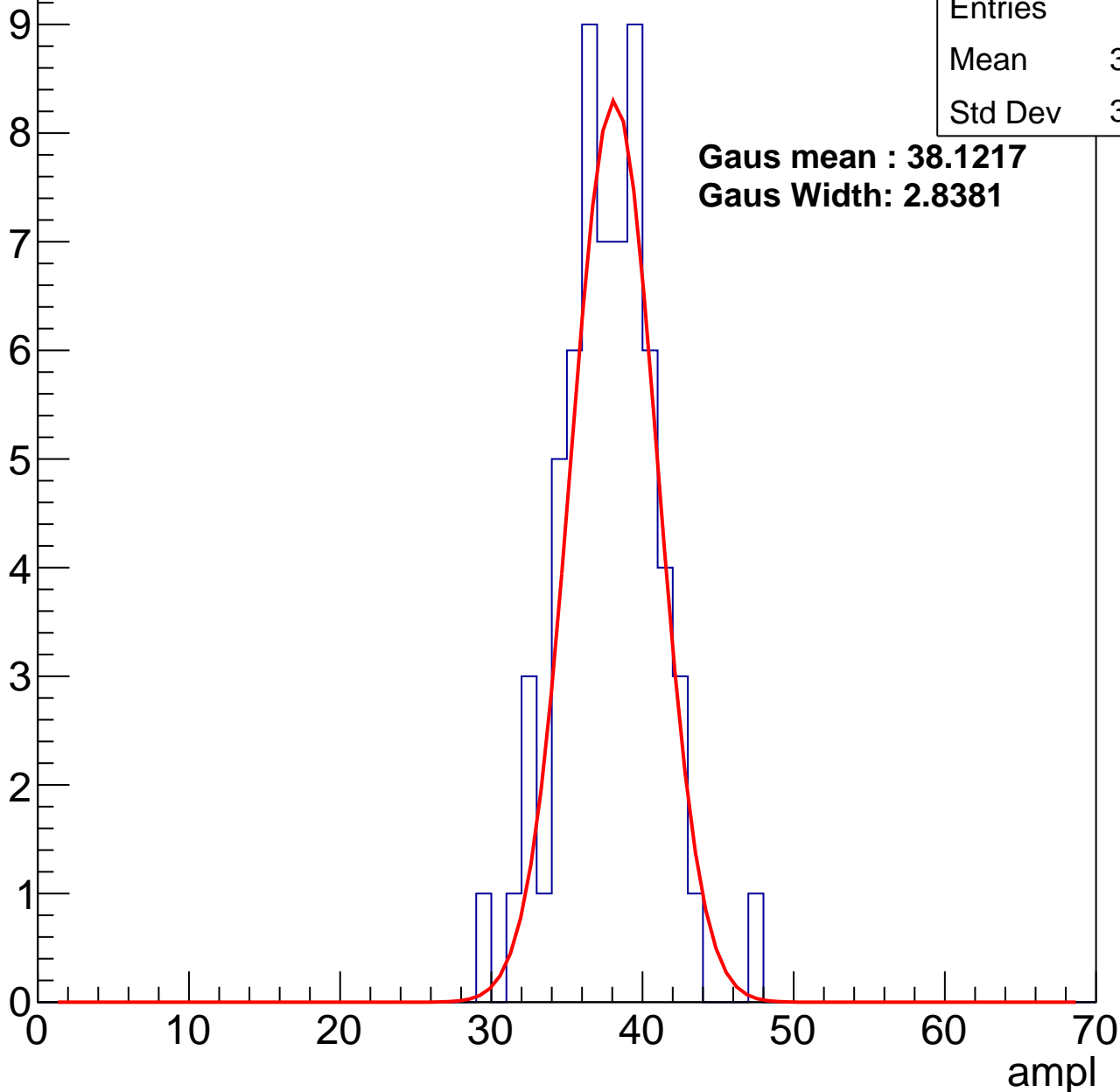
# B1L103S, U9-ch13, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	37.33
Std Dev	3.148

**Gaus mean : 38.1217**  
**Gaus Width: 2.8381**



# B1L103S, U9-ch13, adc2

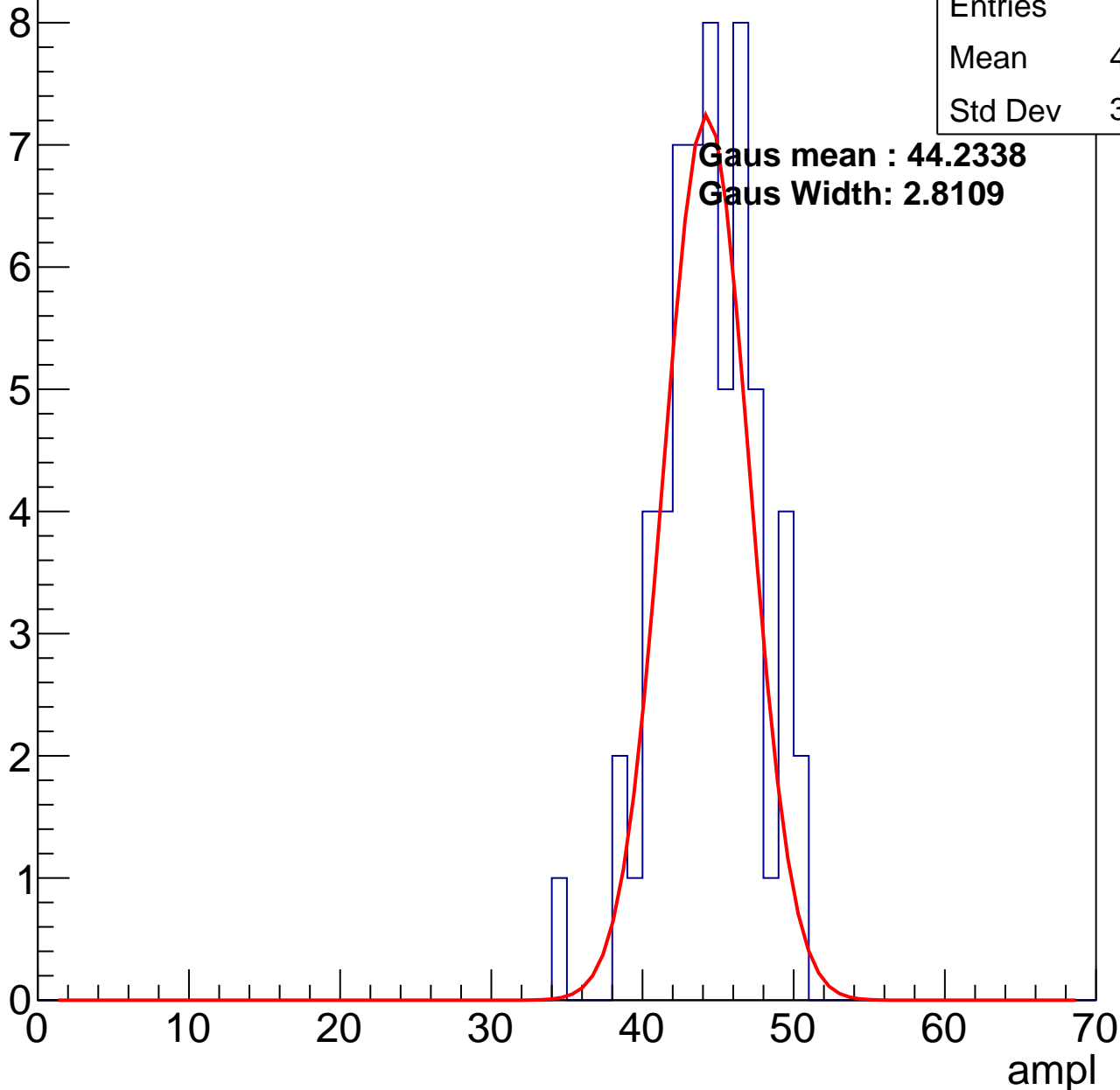
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	59
Mean	43.93
Std Dev	3.194

**Gaus mean : 44.2338**

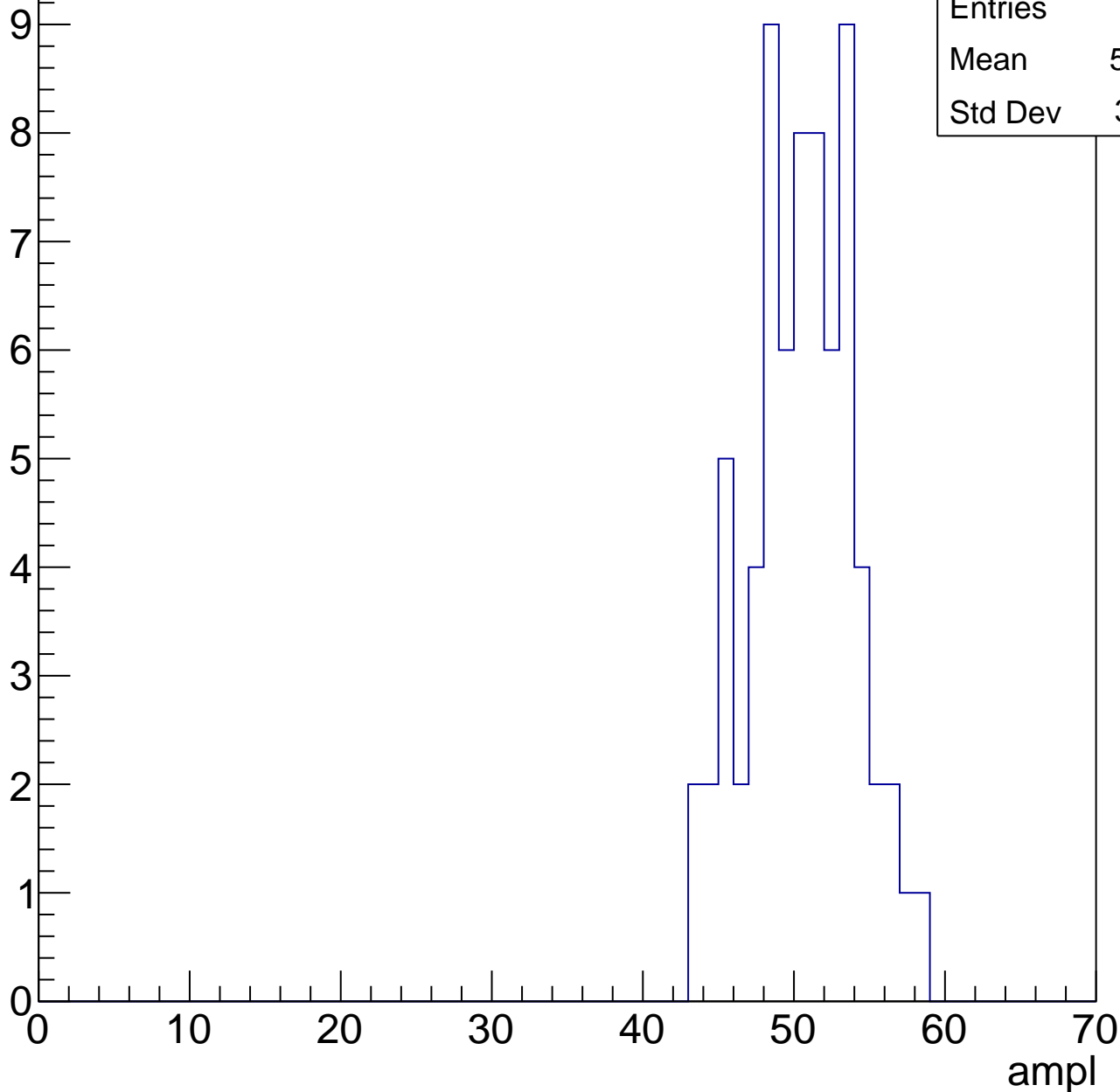
**Gaus Width: 2.8109**



# B1L103S, U9-ch13, adc3

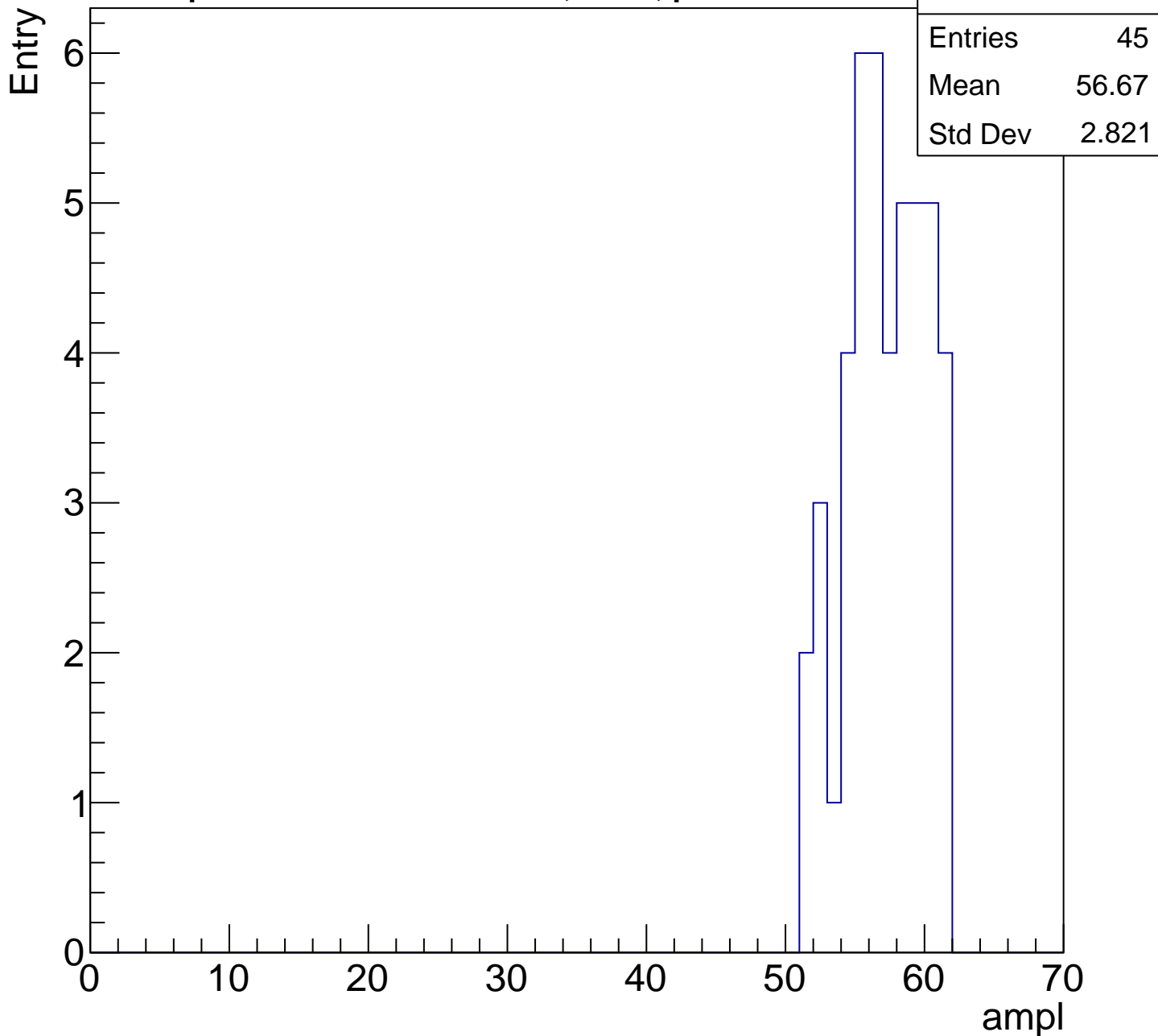
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U9-ch13, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

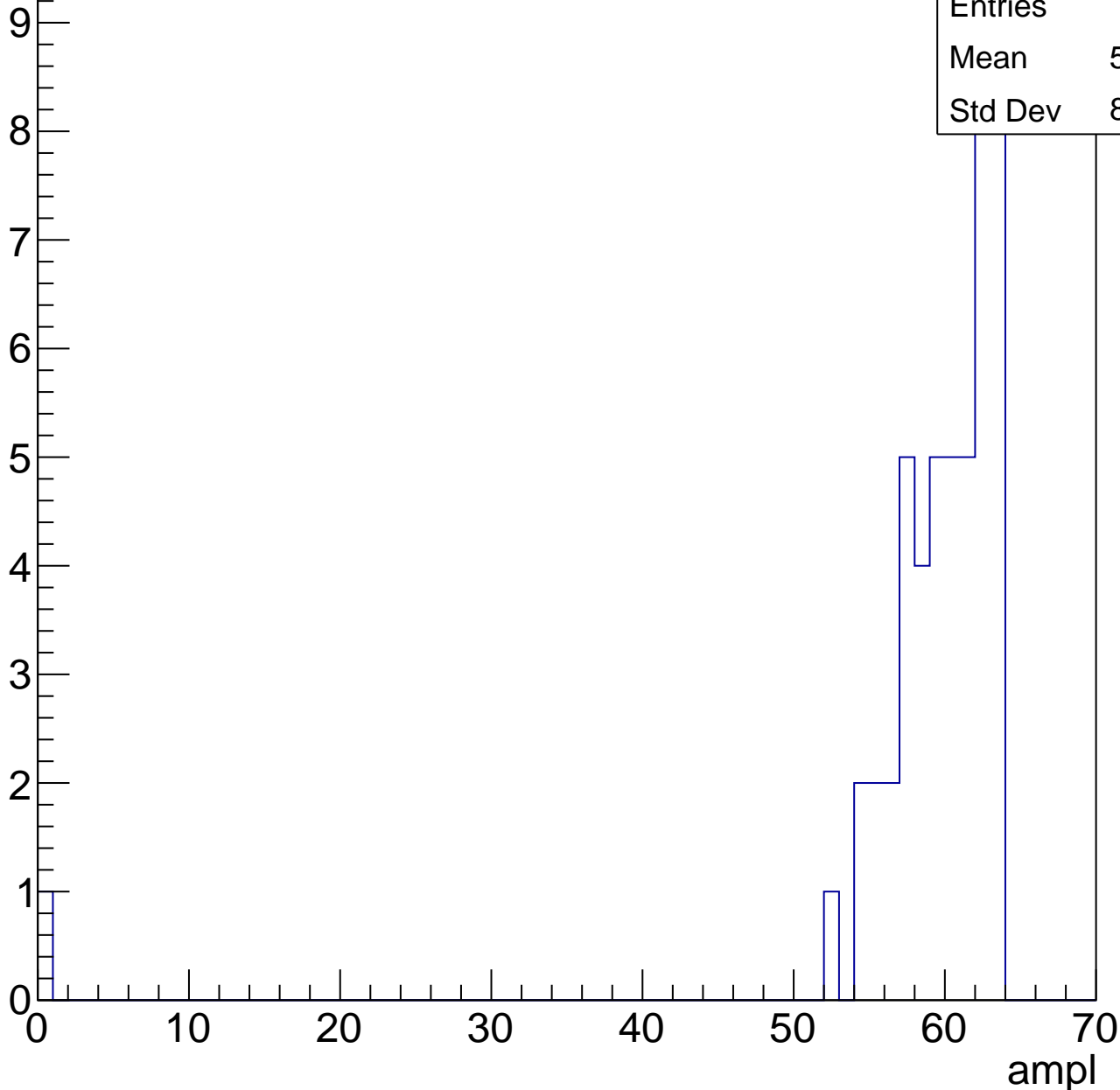


# B1L103S, U9-ch13, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	49
Mean	58.39
Std Dev	8.887



# B1L103S, U9-ch13, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

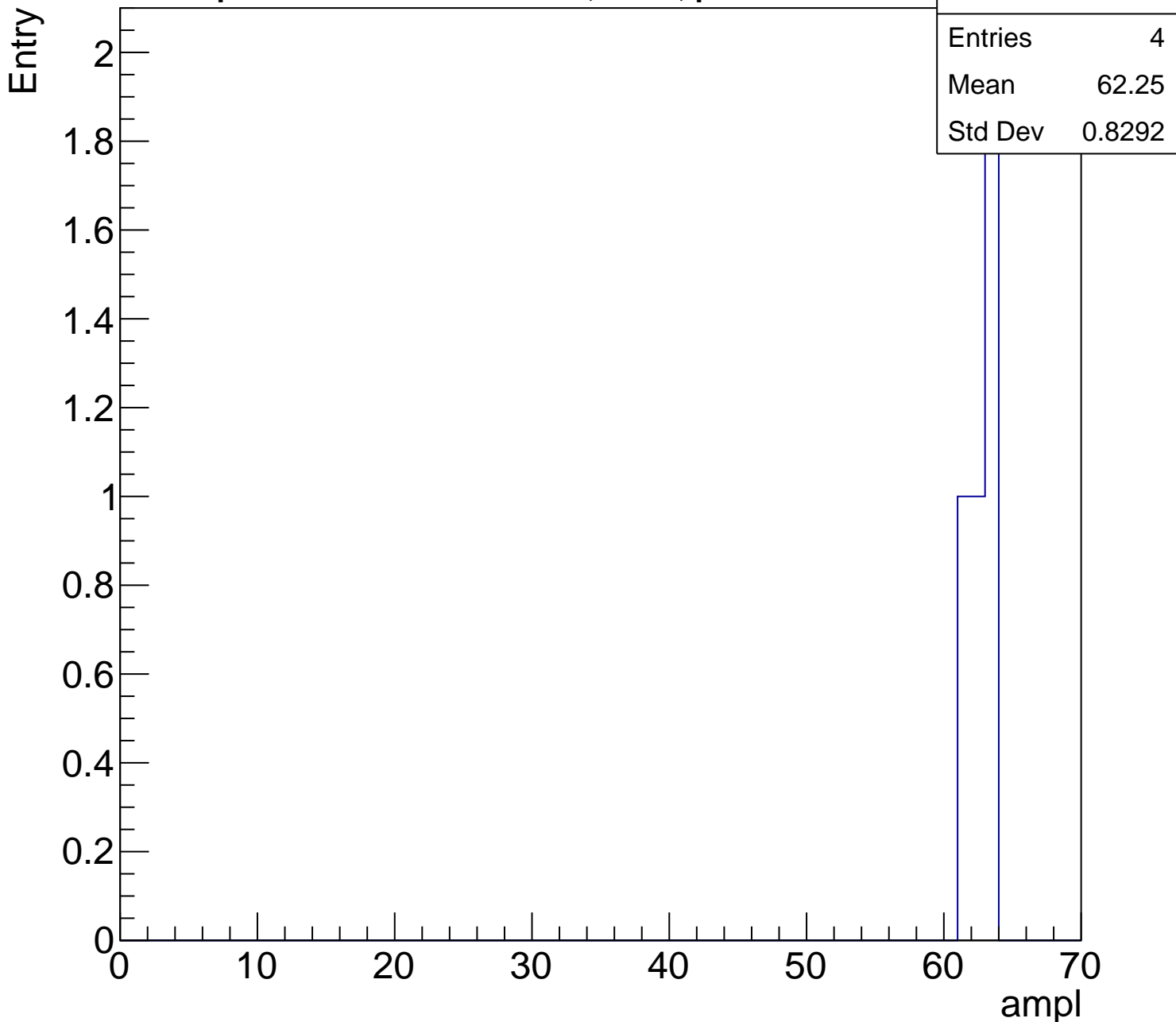
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	4
Mean	62.25
Std Dev	0.8292

0 10 20 30 40 50 60 70

ampl





# B1L103S, U9-ch13, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U9-ch14, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	60
Mean	29.67
Std Dev	3.491

**Gaus mean : 30.6681**

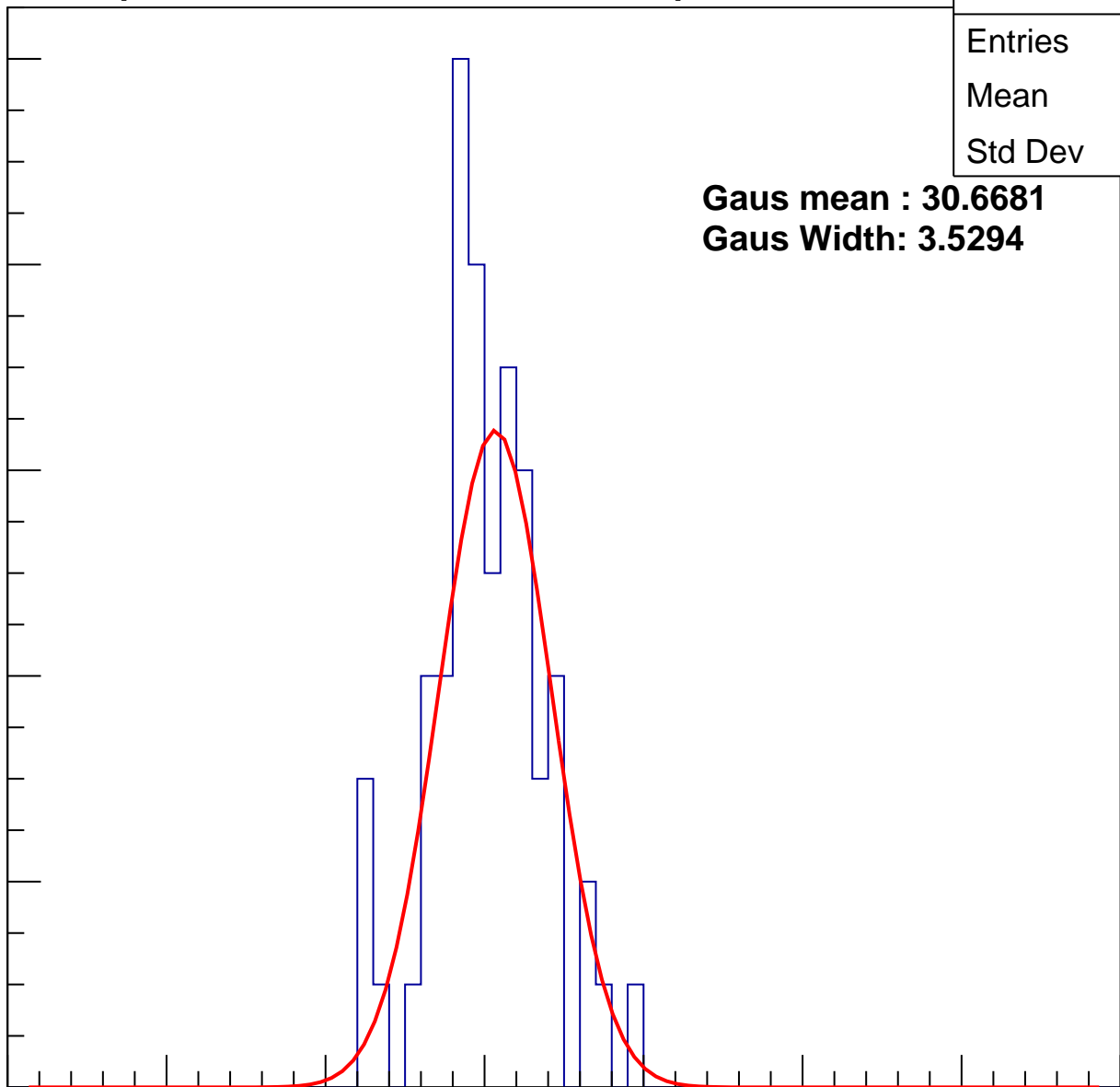
**Gaus Width: 3.5294**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U9-ch14, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	74
Mean	36.45
Std Dev	3.511

**Gaus mean : 37.0542**

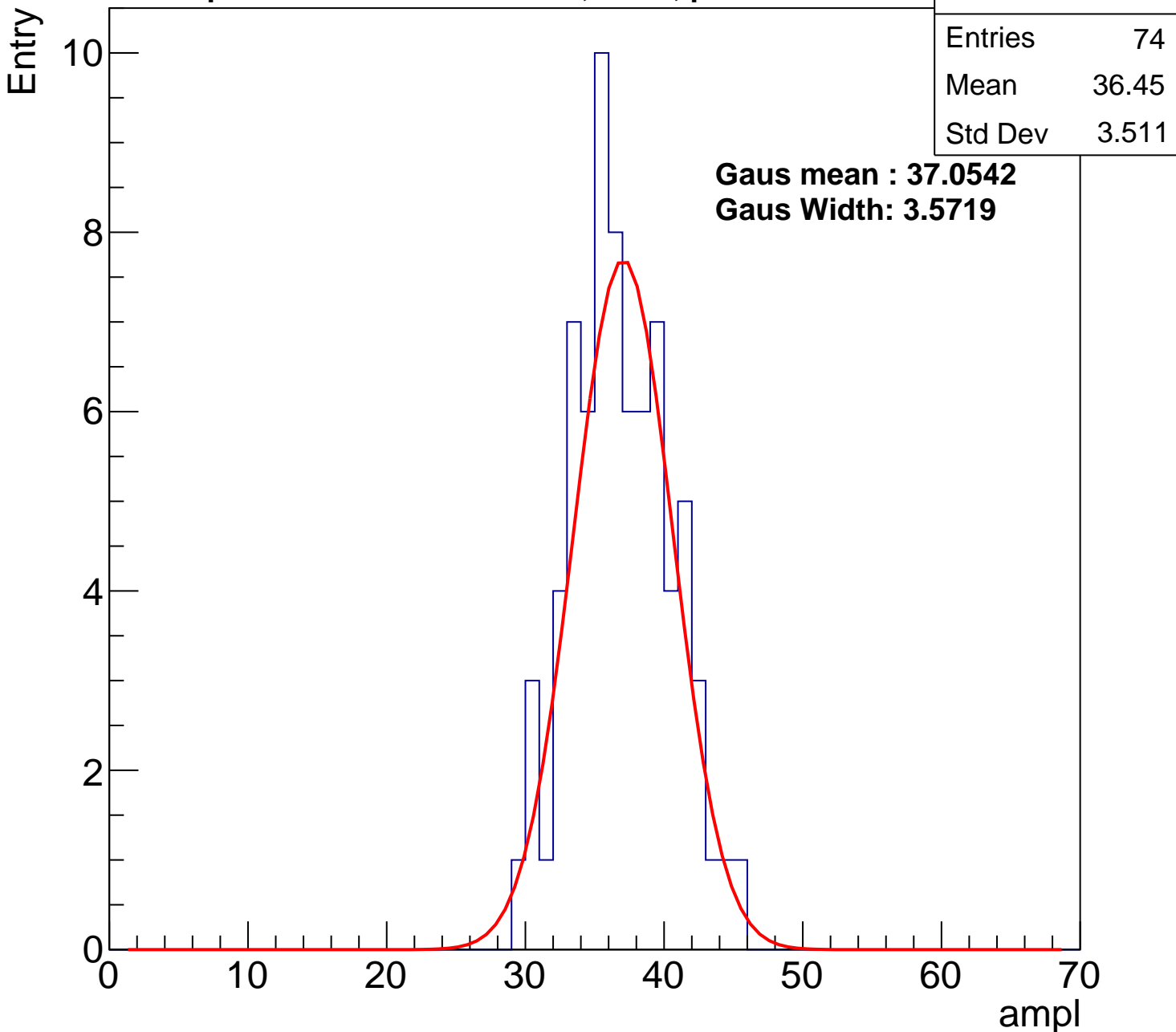
**Gaus Width: 3.5719**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B1L103S, U9-ch14, adc2

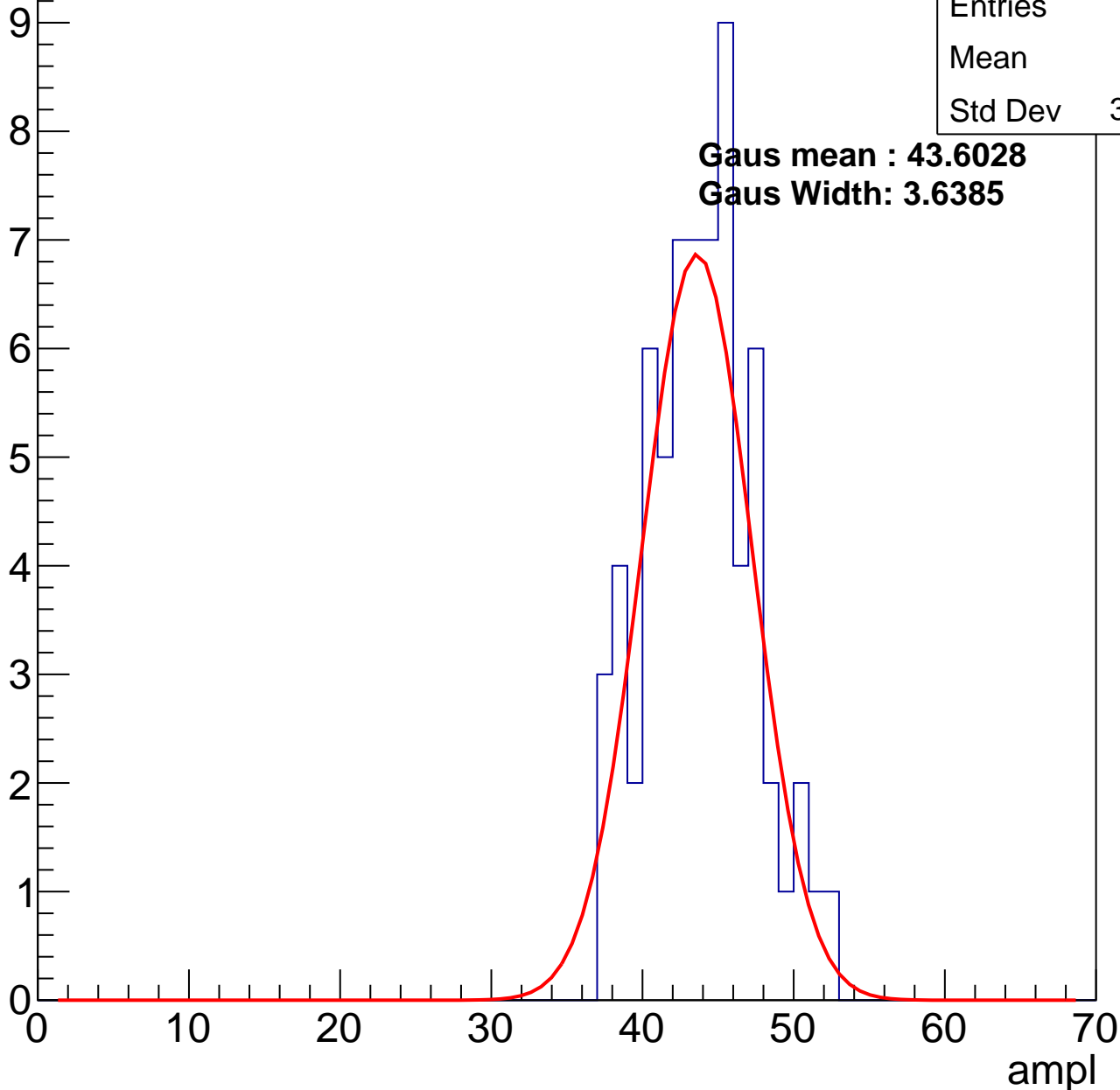
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	43.4
Std Dev	3.486

**Gaus mean : 43.6028**

**Gaus Width: 3.6385**

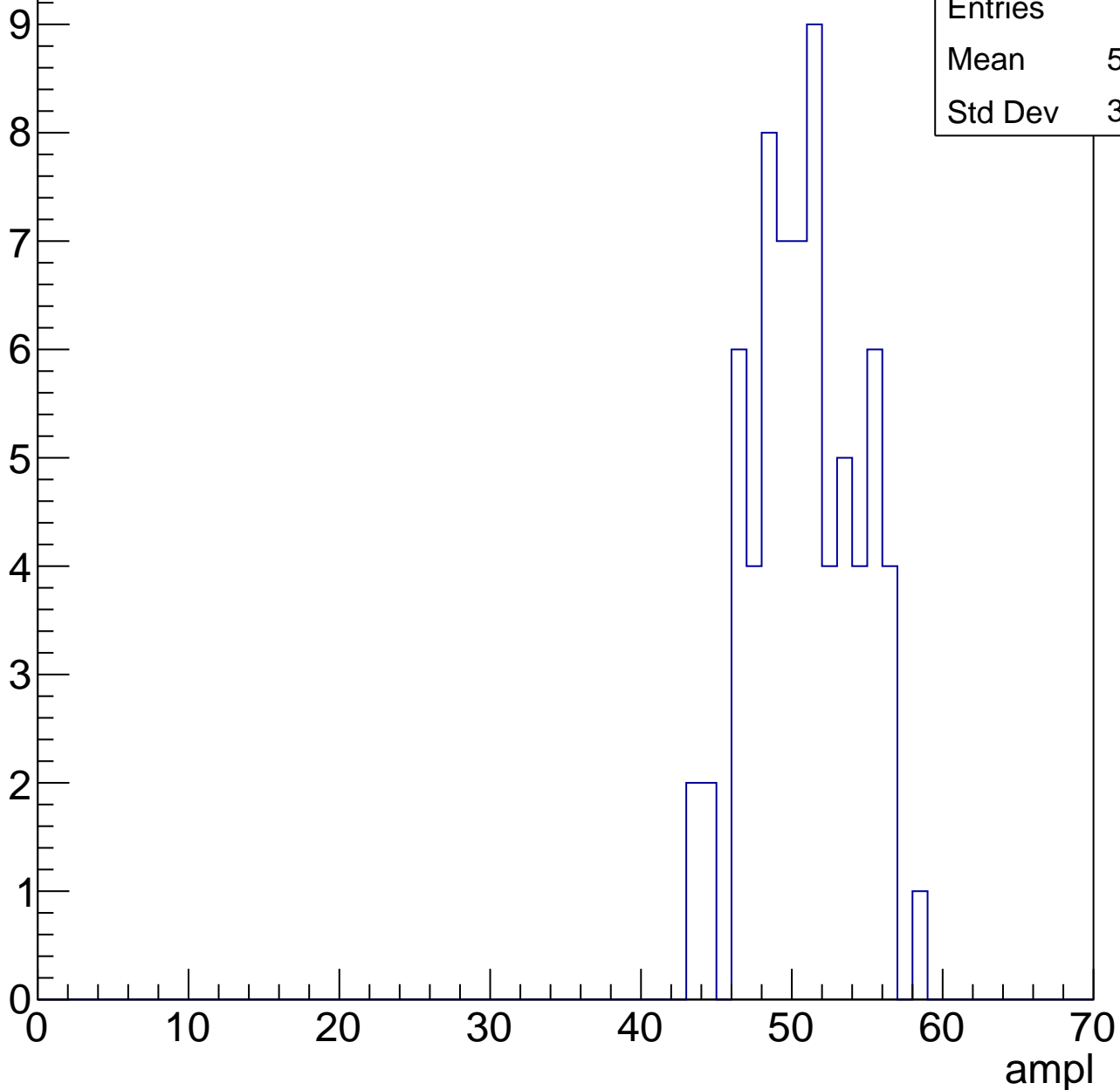


# B1L103S, U9-ch14, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

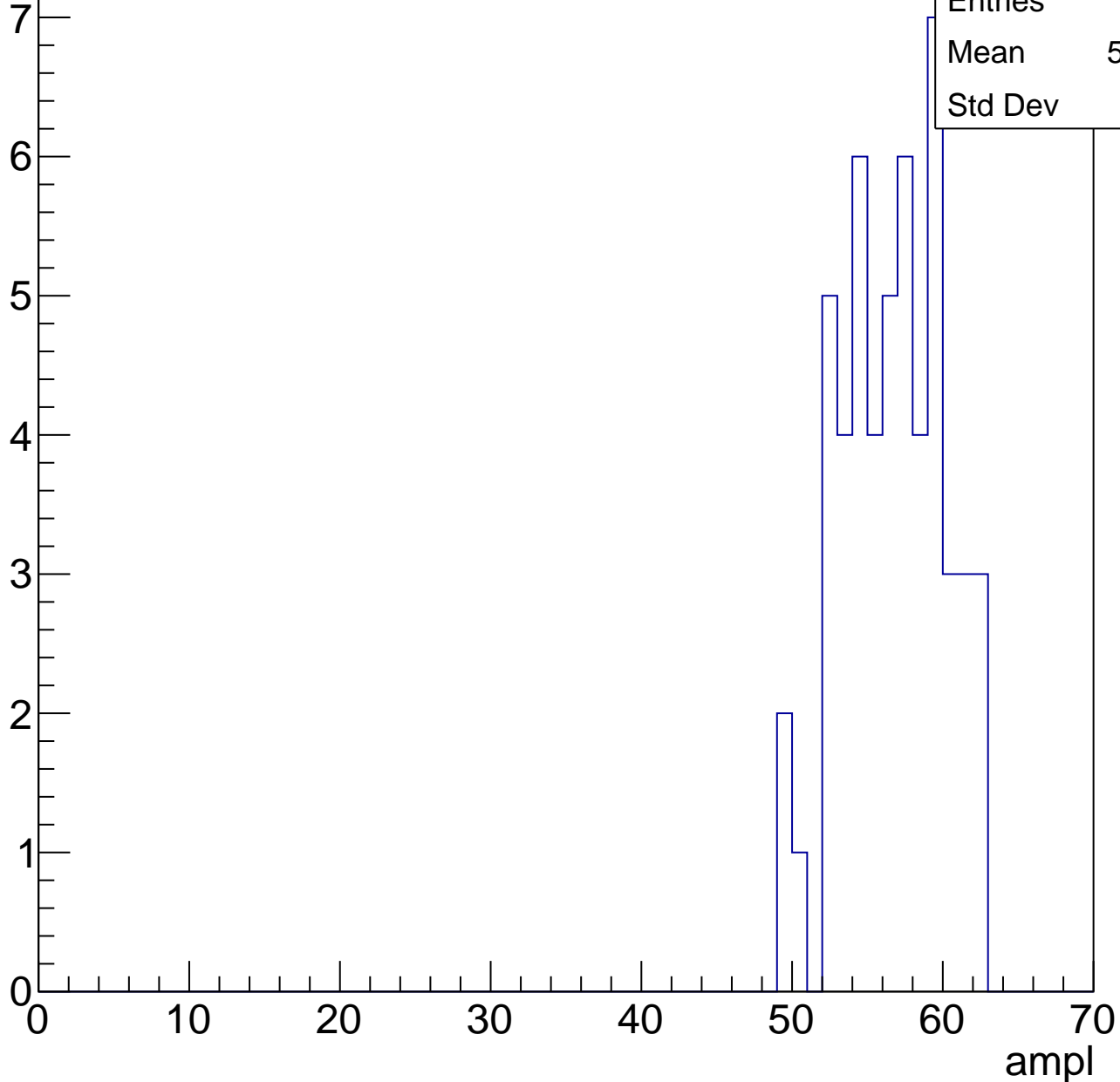
Entries	69
Mean	50.36
Std Dev	3.456



# B1L103S, U9-ch14, adc4

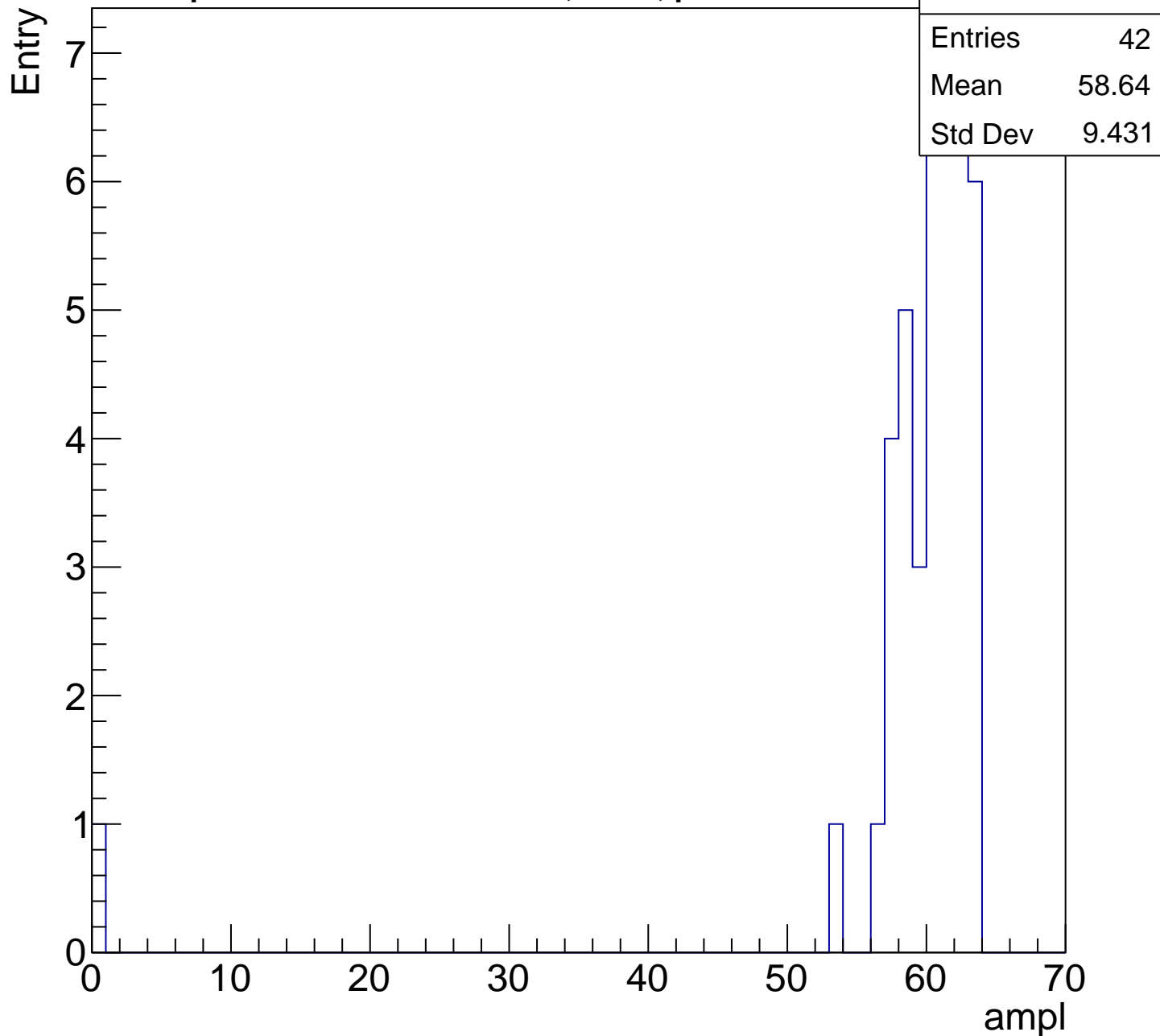
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U9-ch14, adc5

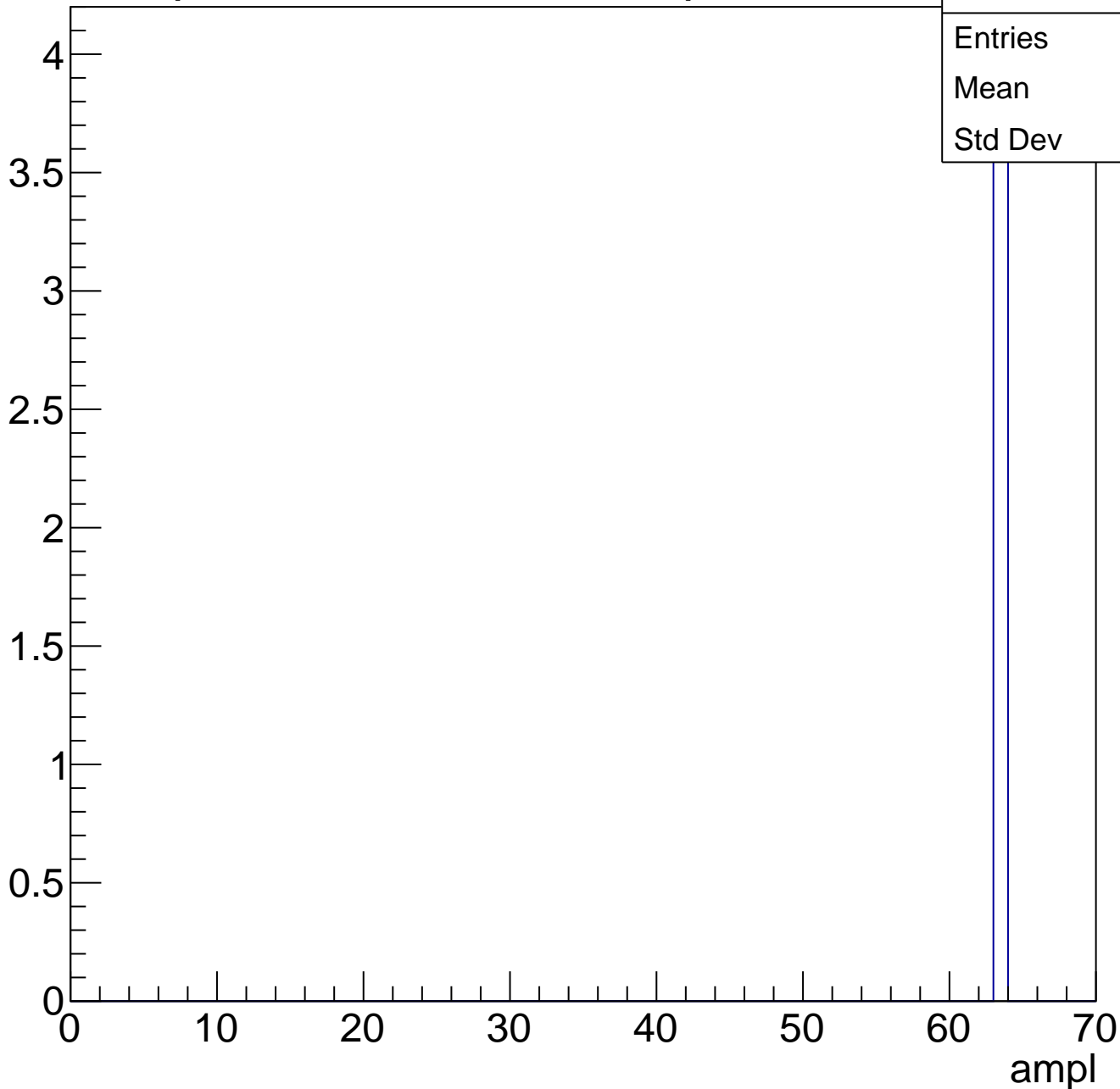
calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U9-ch14, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

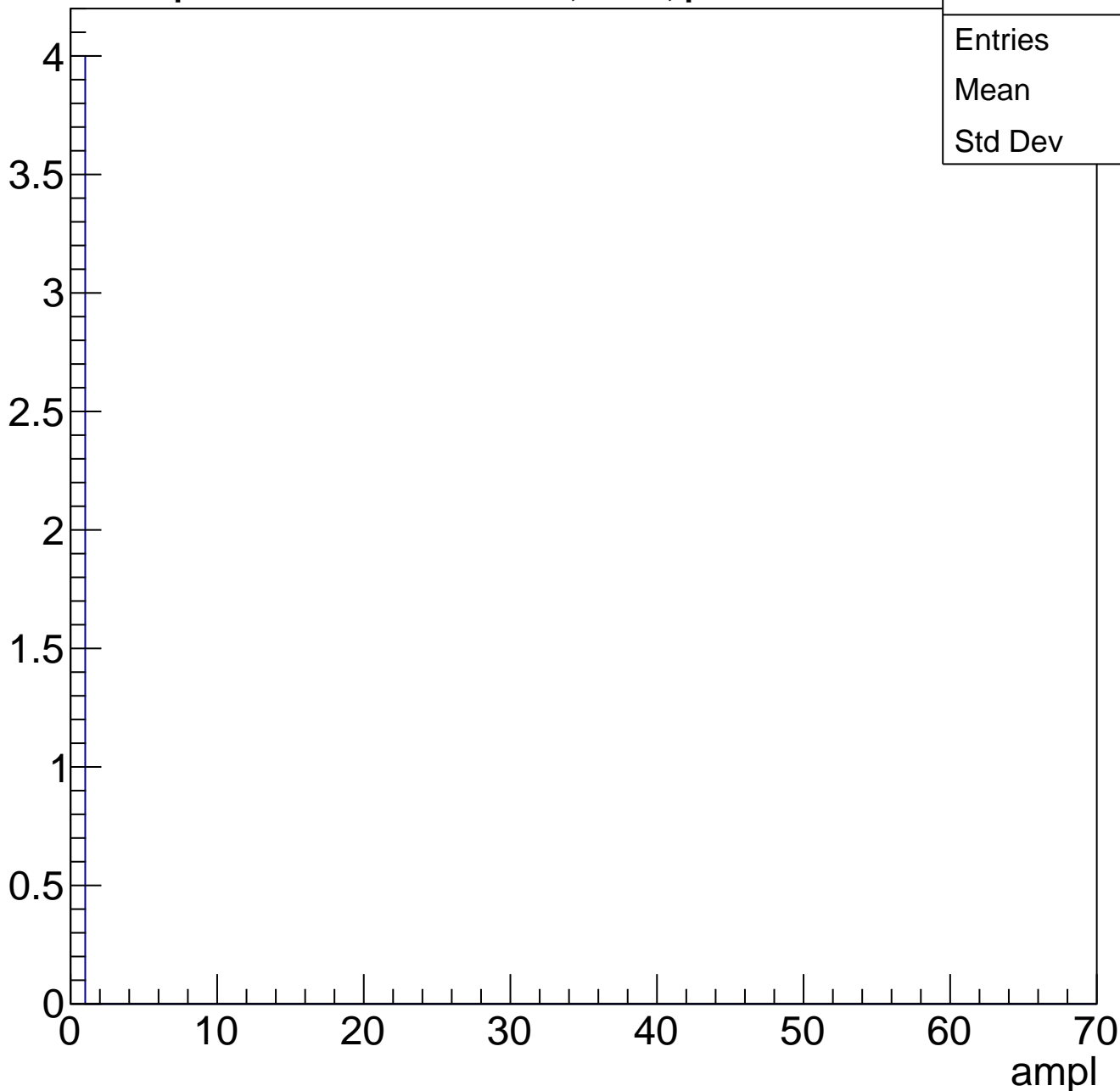




# B1L103S, U9-ch14, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	4
Mean	0
Std Dev	0

# B1L103S, U9-ch15, adc0

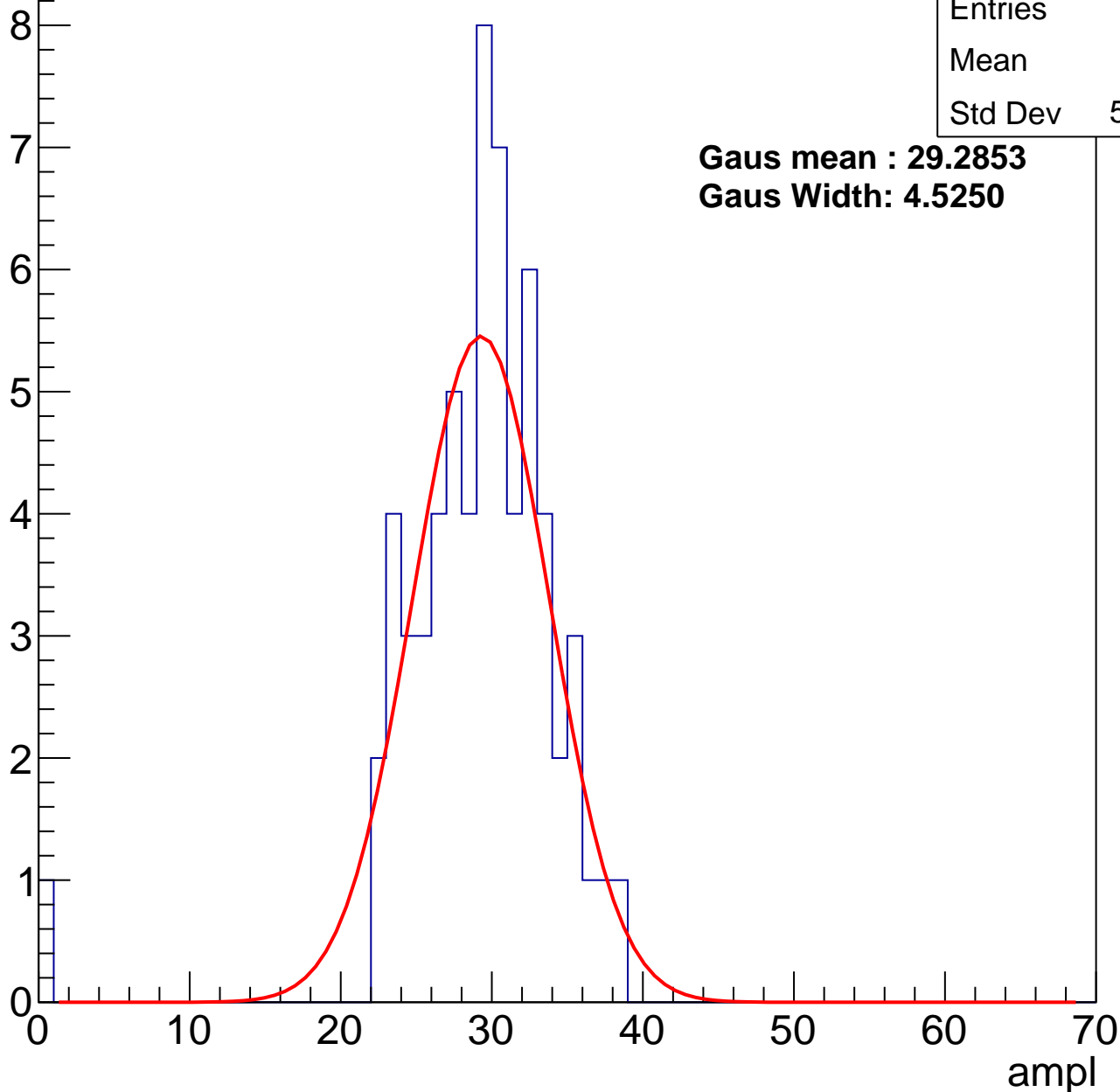
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	28.7
Std Dev	5.275

**Gaus mean : 29.2853**

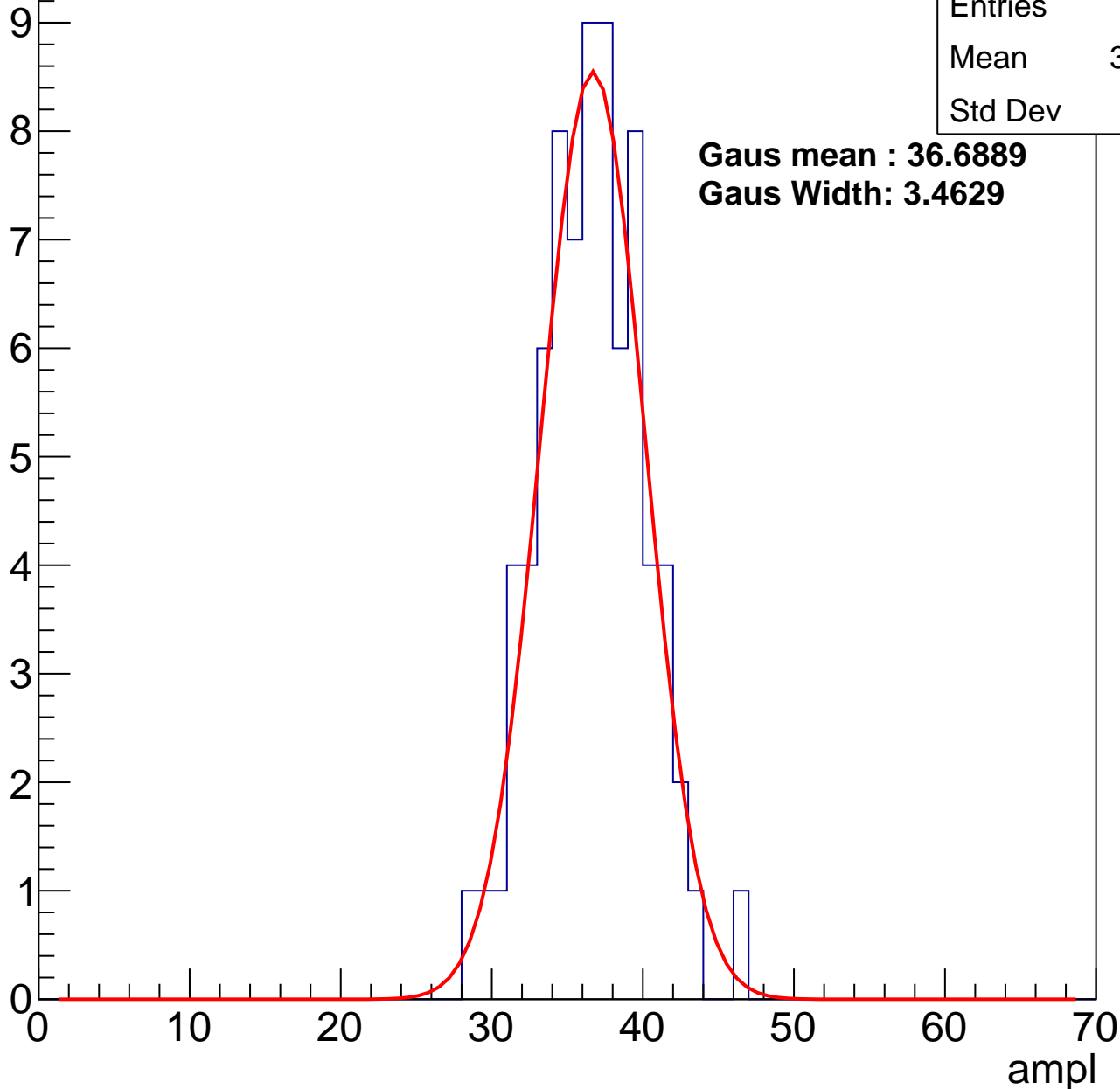
**Gaus Width: 4.5250**



# B1L103S, U9-ch15, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U9-ch15, adc2

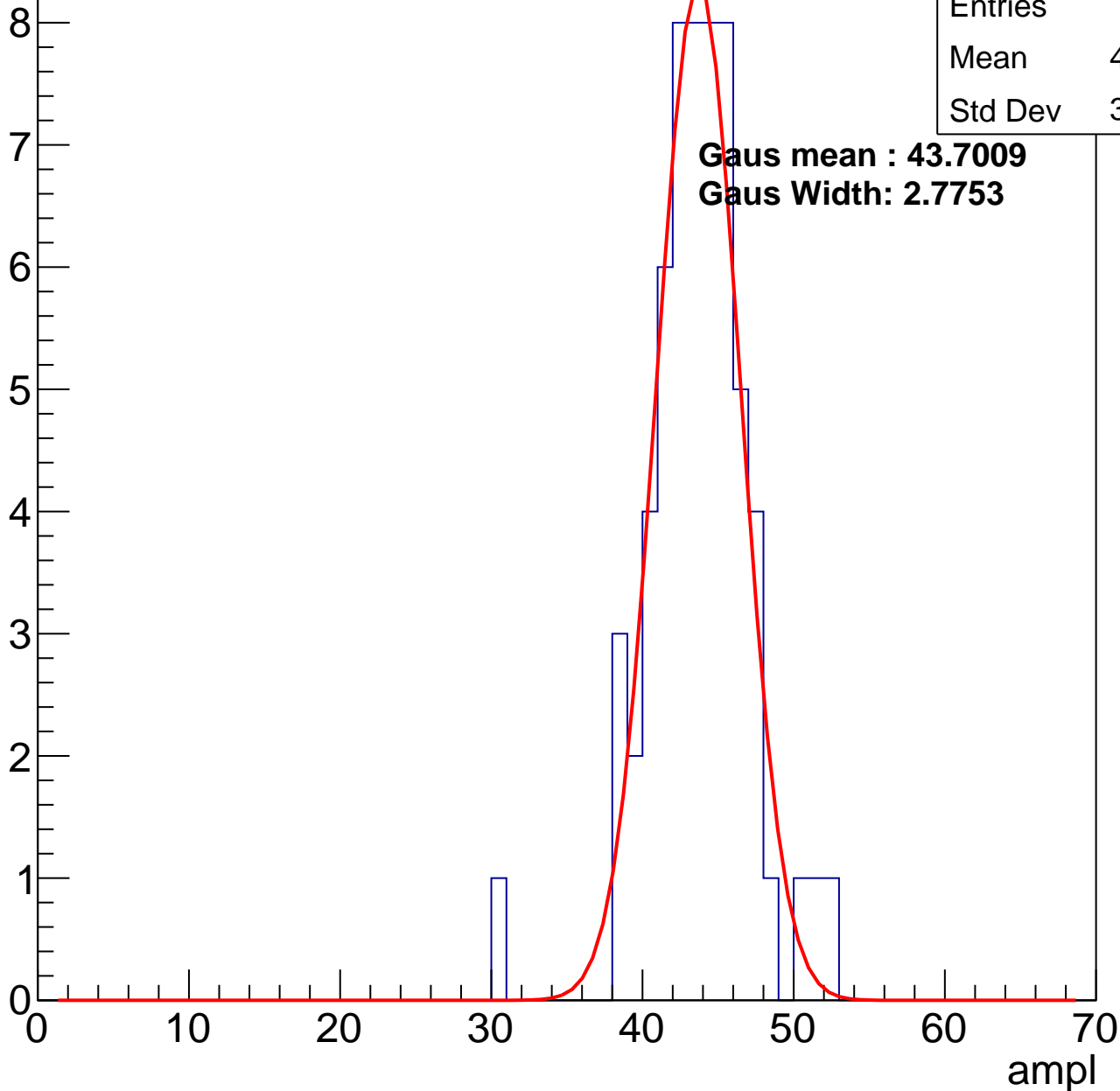
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	61
Mean	43.26
Std Dev	3.406

**Gaus mean : 43.7009**

**Gaus Width: 2.7753**

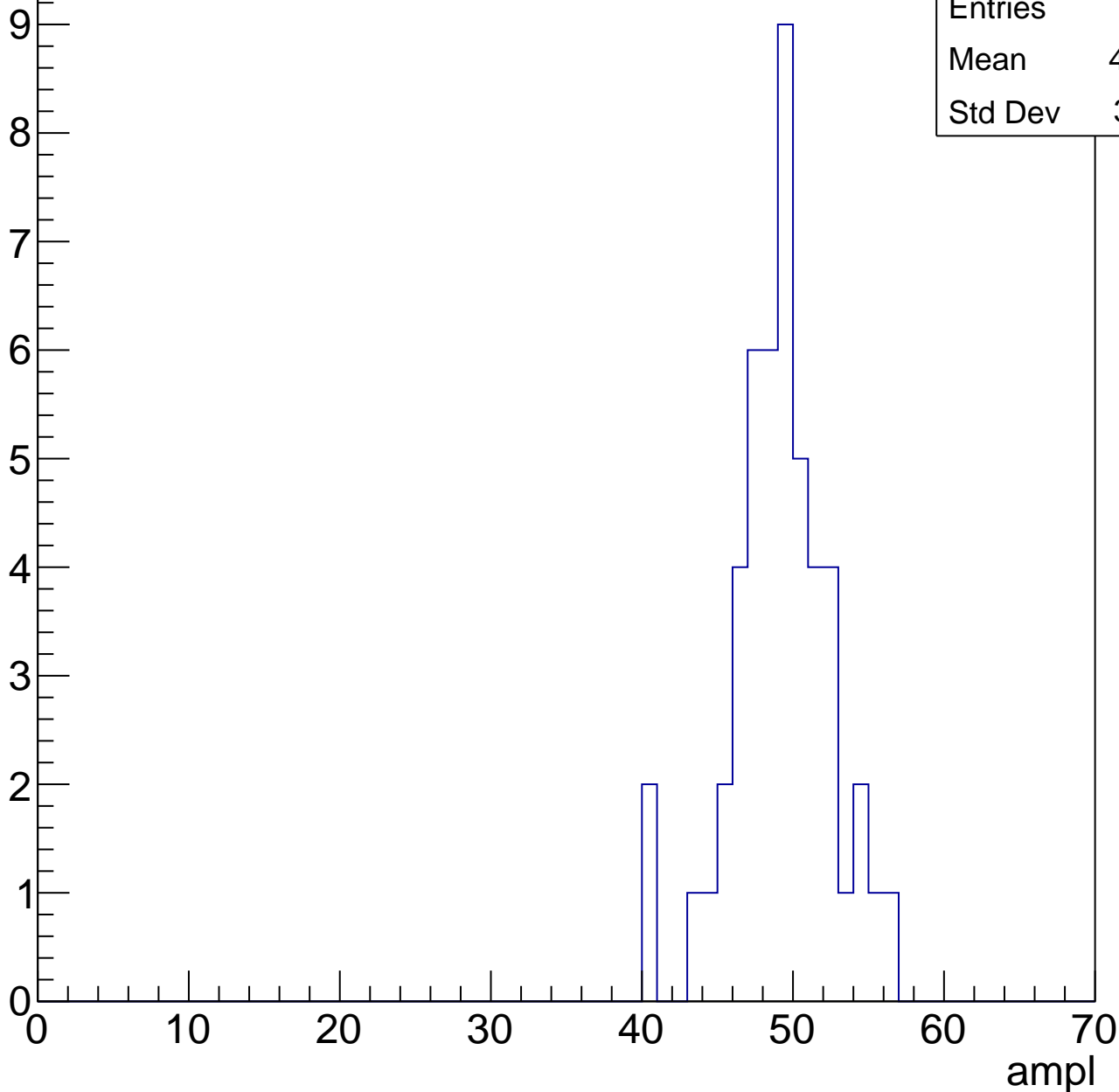


# B1L103S, U9-ch15, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	49
Mean	48.69
Std Dev	3.271

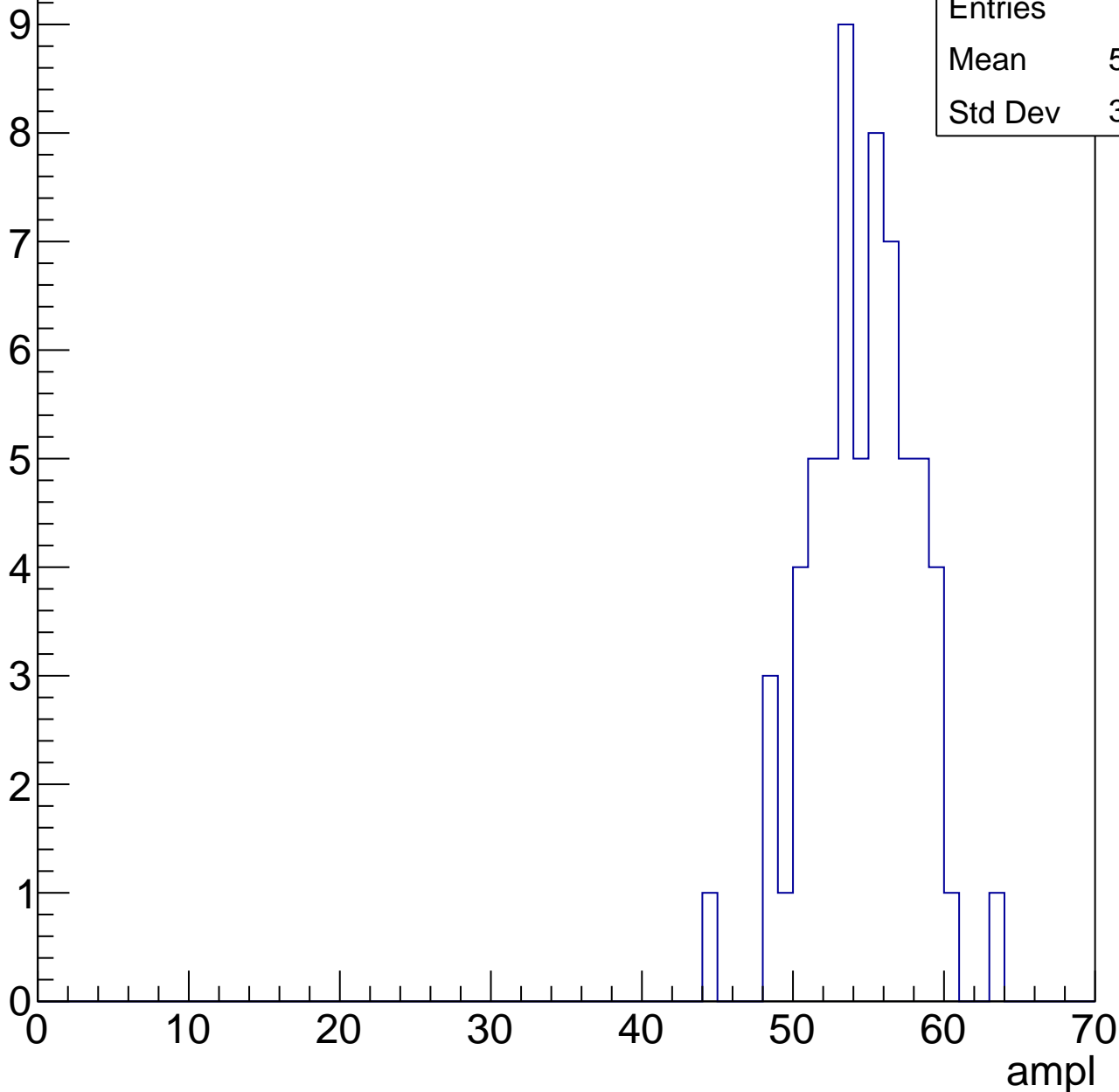


# B1L103S, U9-ch15, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	54.14
Std Dev	3.418

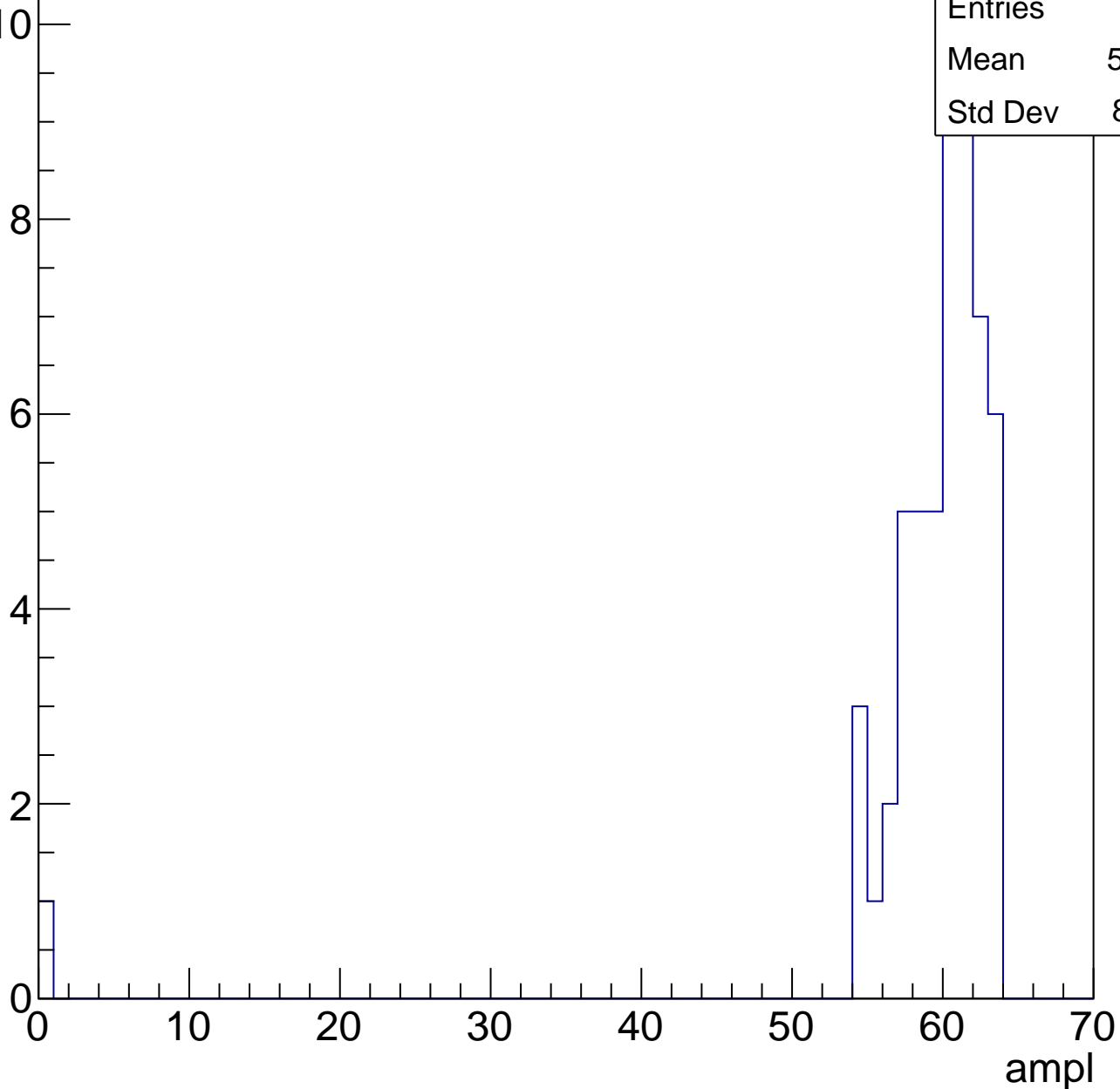


# B1L103S, U9-ch15, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	54
Mean	58.54
Std Dev	8.401



# B1L103S, U9-ch15, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U9-ch15, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U9-ch16, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	77
Mean	29.64
Std Dev	3.449

**Gaus mean : 29.4927**

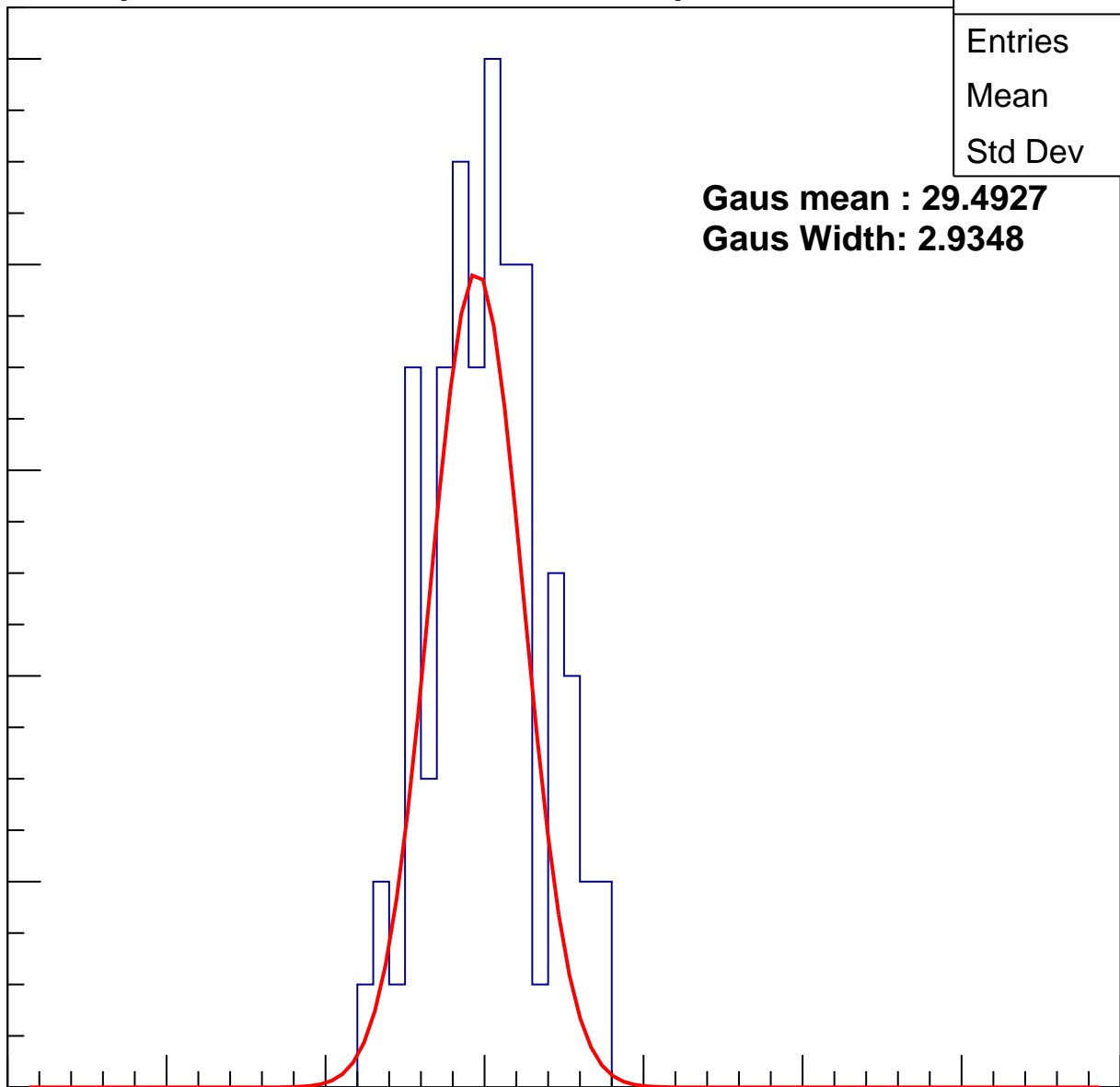
**Gaus Width: 2.9348**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U9-ch16, adc1

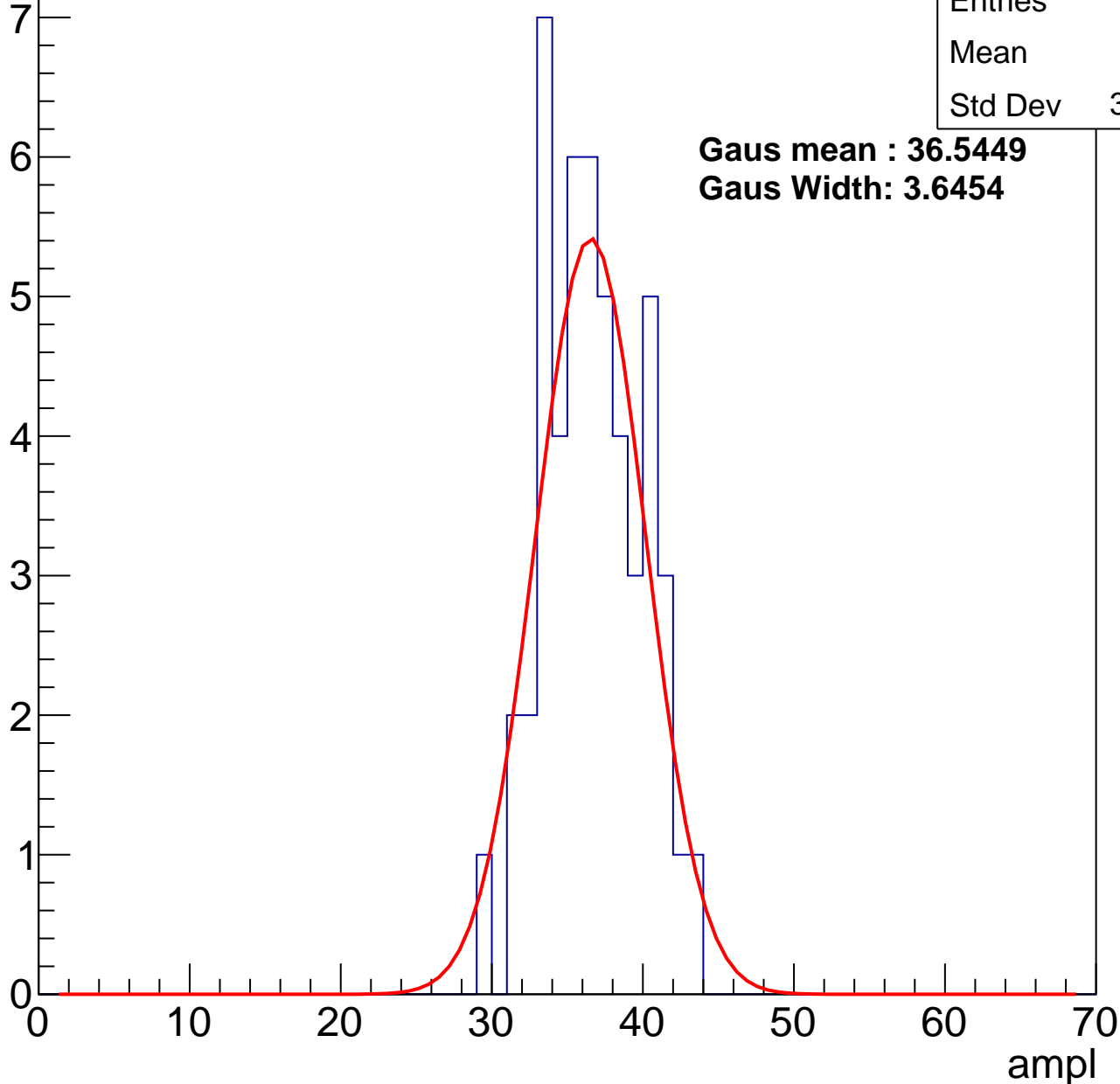
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	50
Mean	36.2
Std Dev	3.169

**Gaus mean : 36.5449**

**Gaus Width: 3.6454**



# B1L103S, U9-ch16, adc2

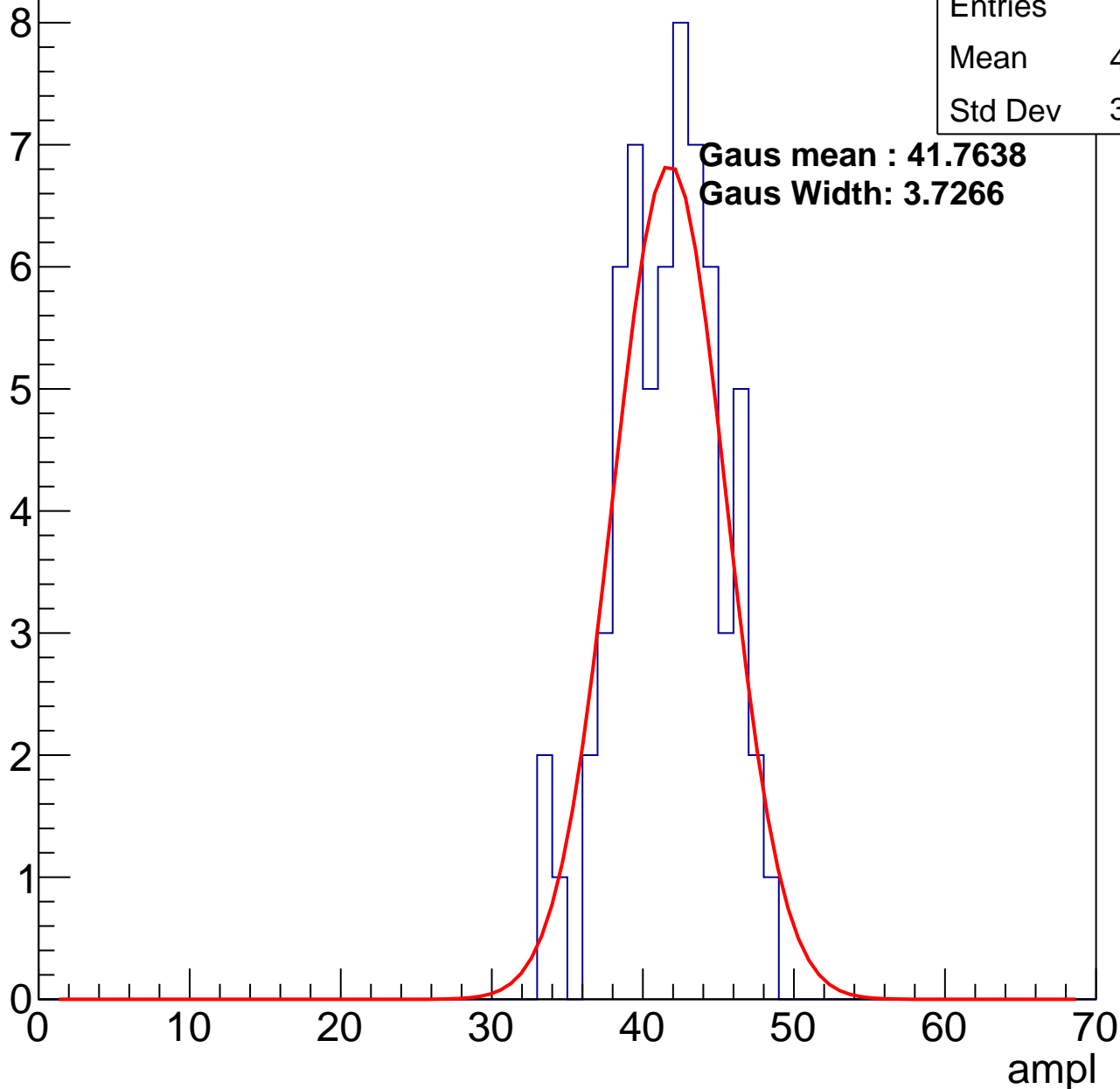
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	41.22
Std Dev	3.407

**Gaus mean : 41.7638**

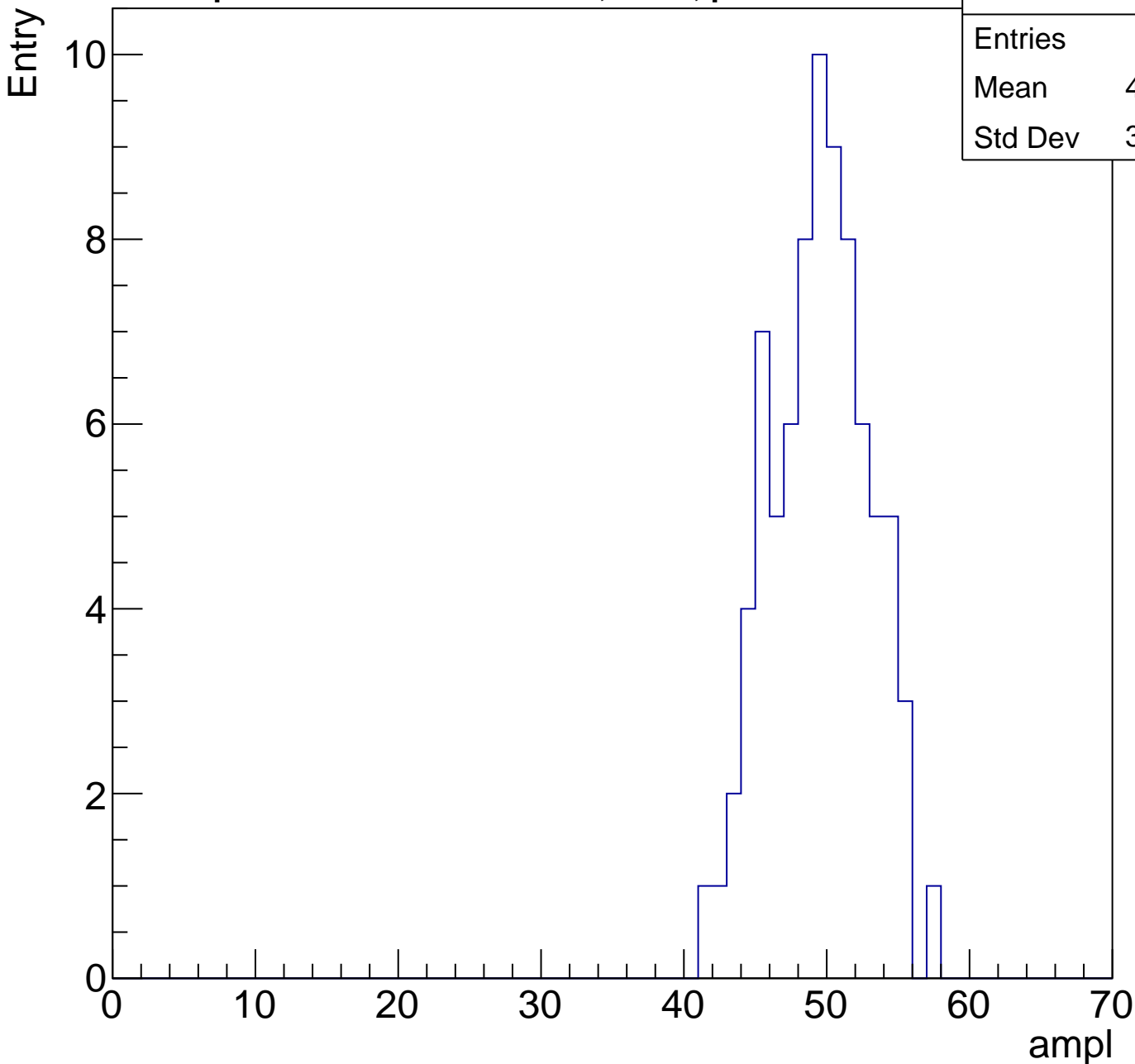
**Gaus Width: 3.7266**



# B1L103S, U9-ch16, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	81
Mean	49.05
Std Dev	3.417

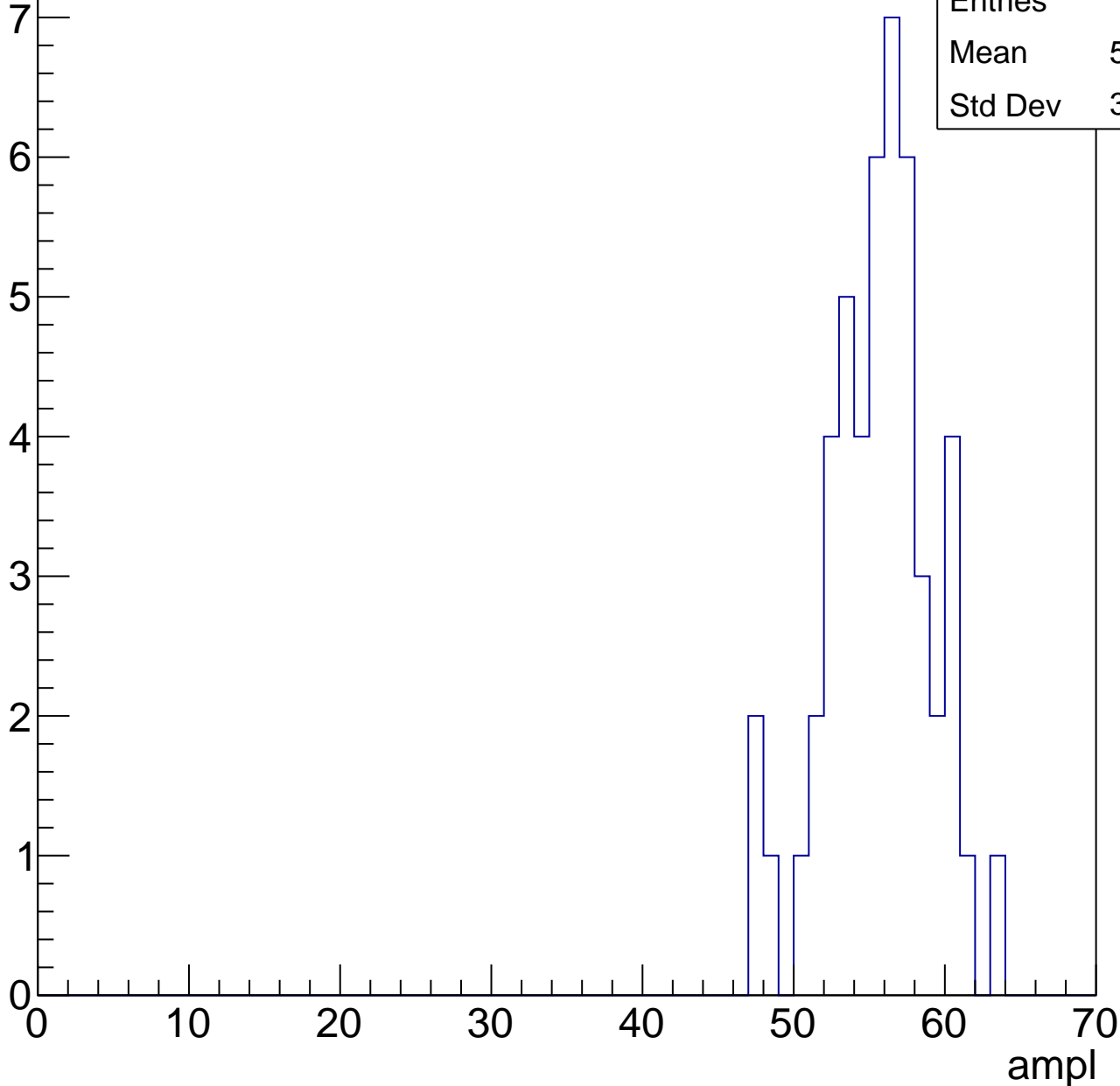


# B1L103S, U9-ch16, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	49
Mean	55.16
Std Dev	3.448



# B1L103S, U9-ch16, adc5

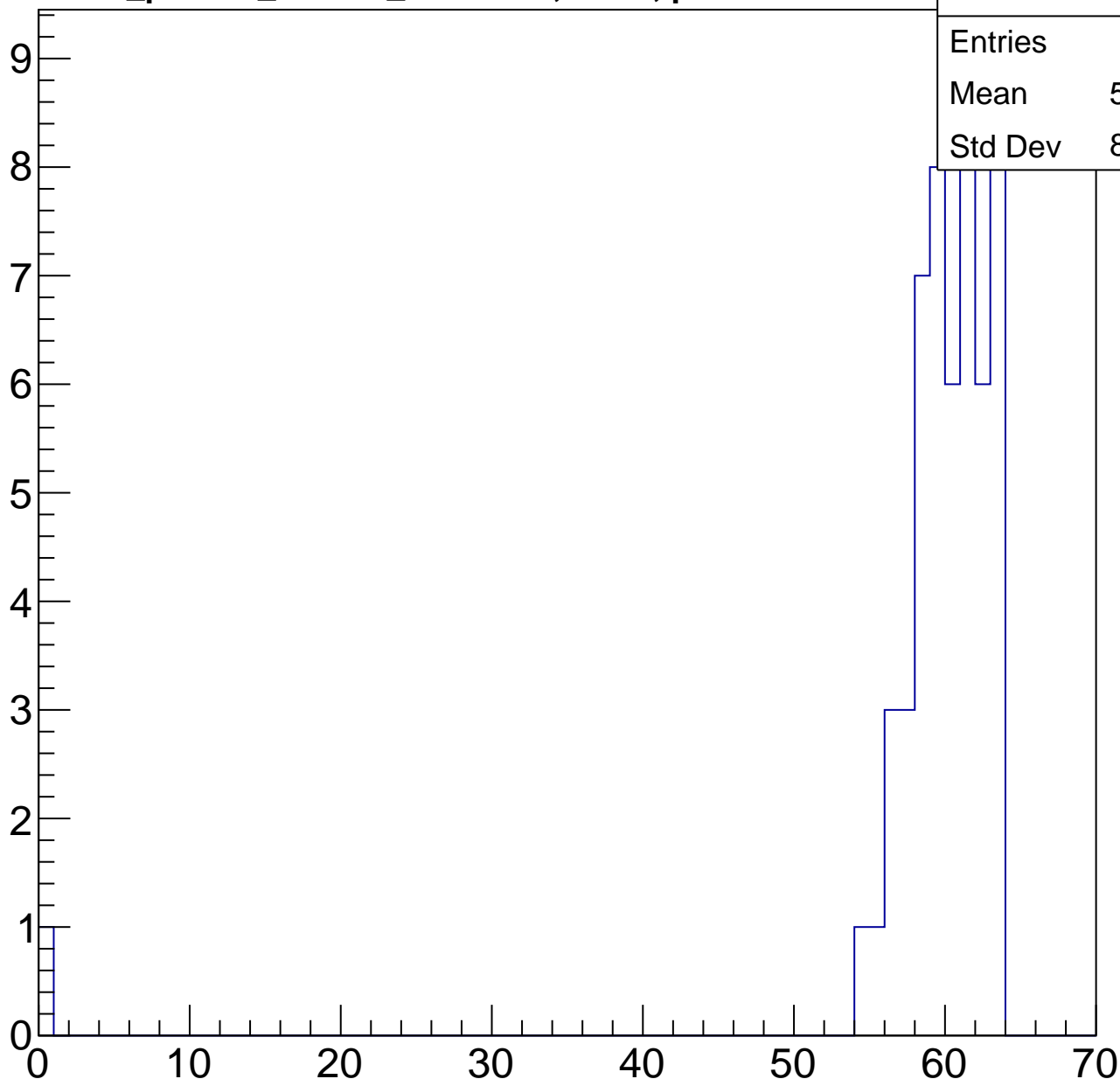
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	53
Mean	58.74
Std Dev	8.468

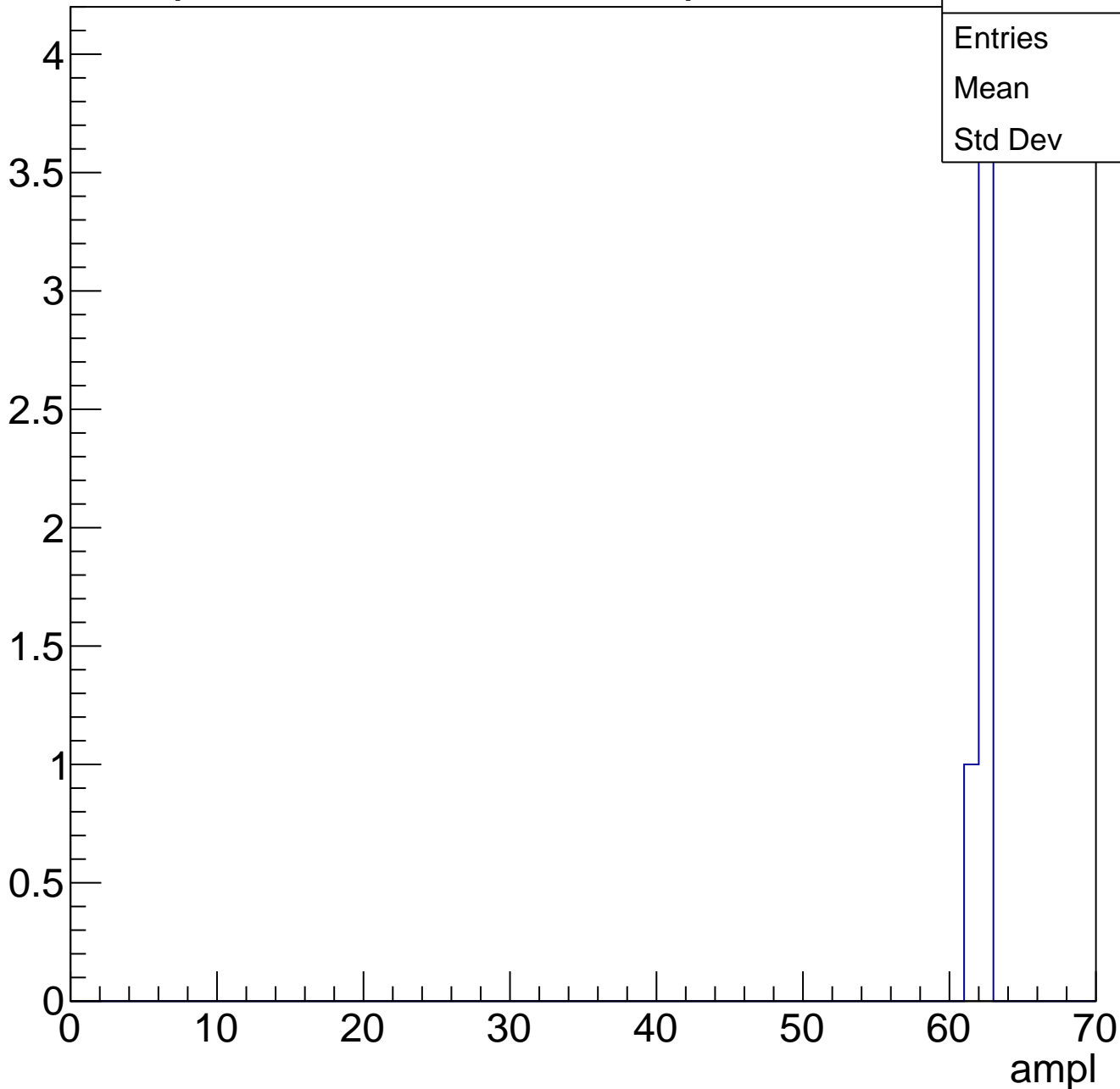
ampl



# B1L103S, U9-ch16, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U9-ch16, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L103S, U9-ch17, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	98
Mean	29.38
Std Dev	4.937

**Gaus mean : 29.9658**

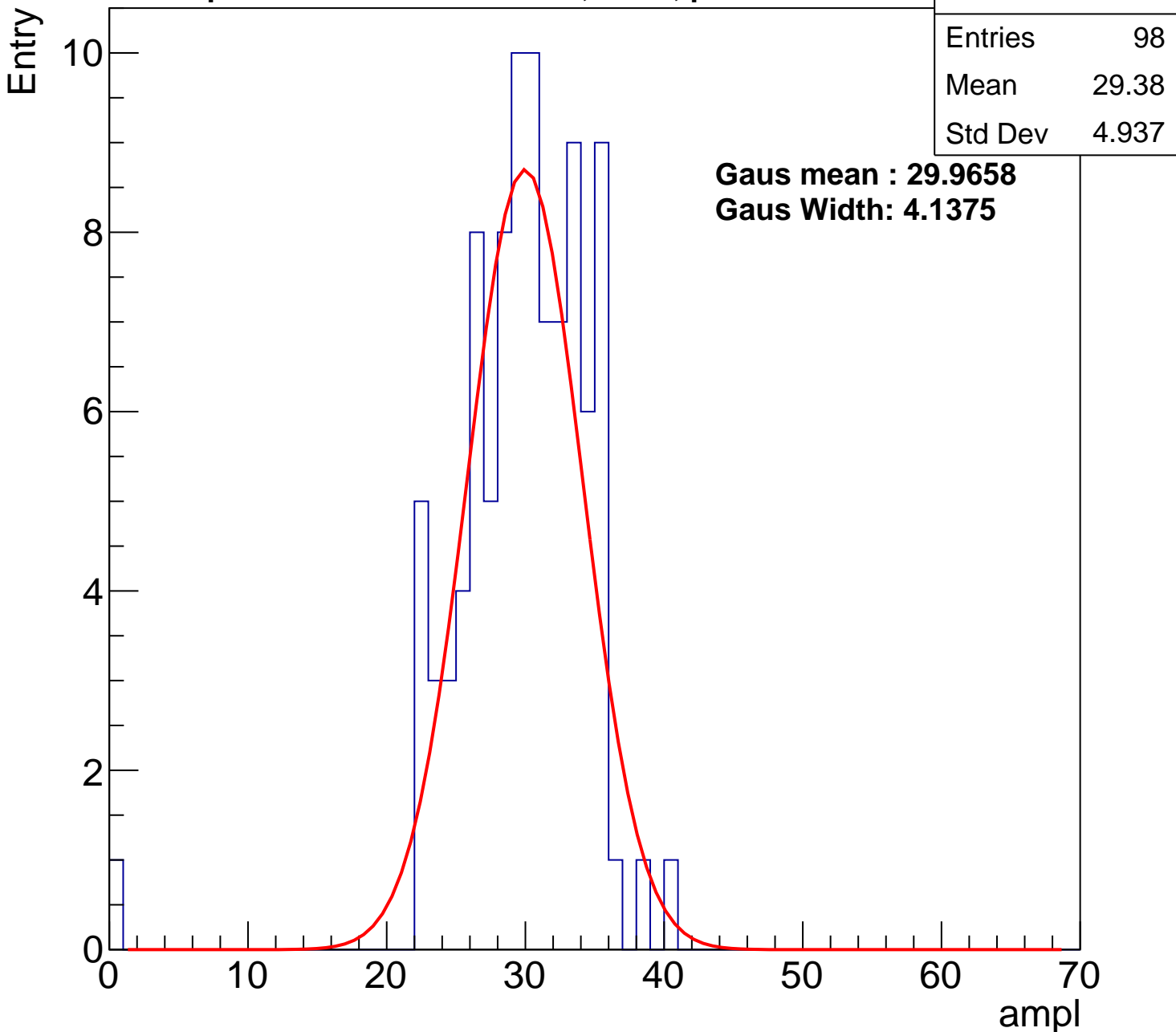
**Gaus Width: 4.1375**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U9-ch17, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	60
Mean	37.65
Std Dev	3.265

**Gaus mean : 38.8496**

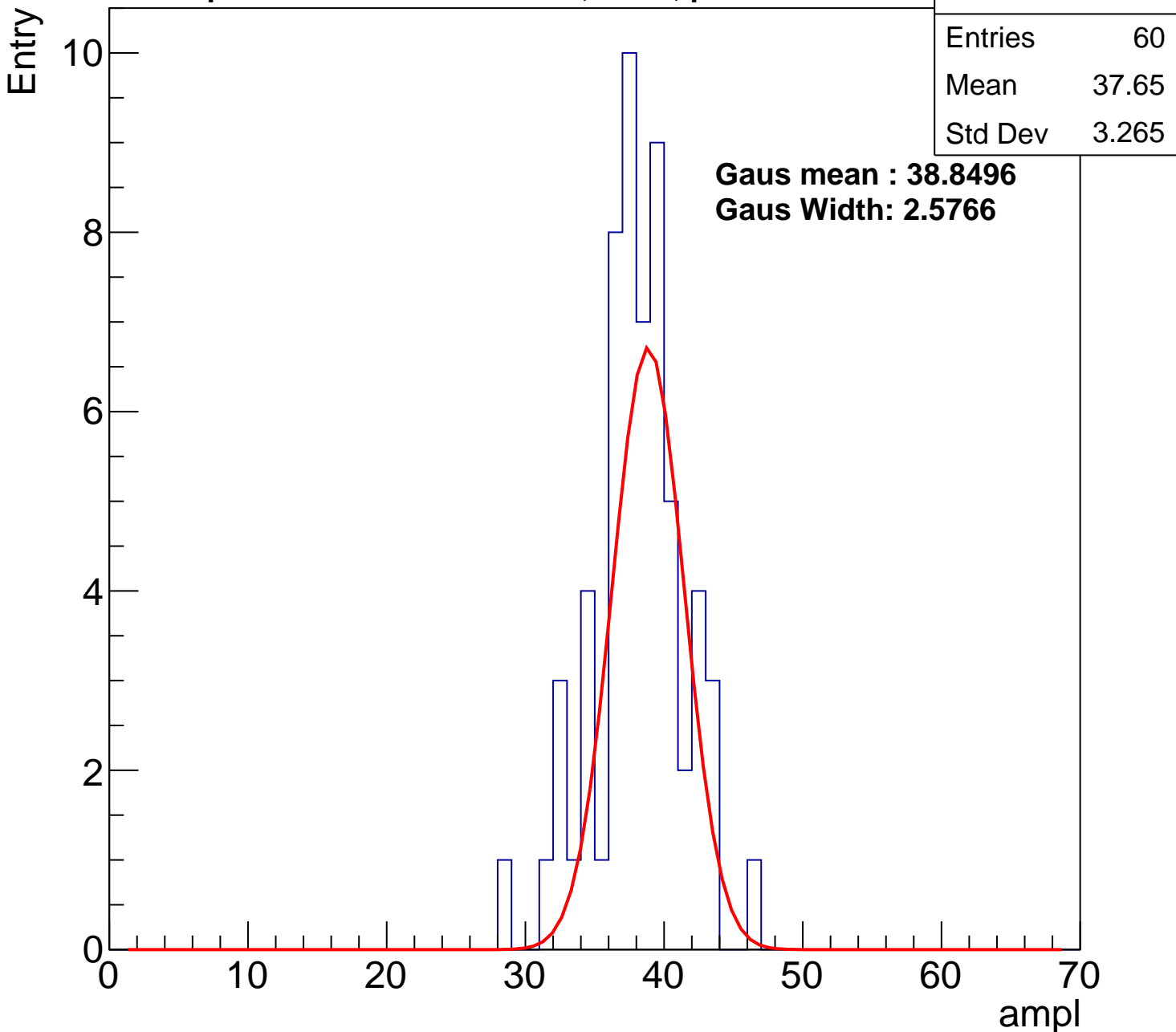
**Gaus Width: 2.5766**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B1L103S, U9-ch17, adc2

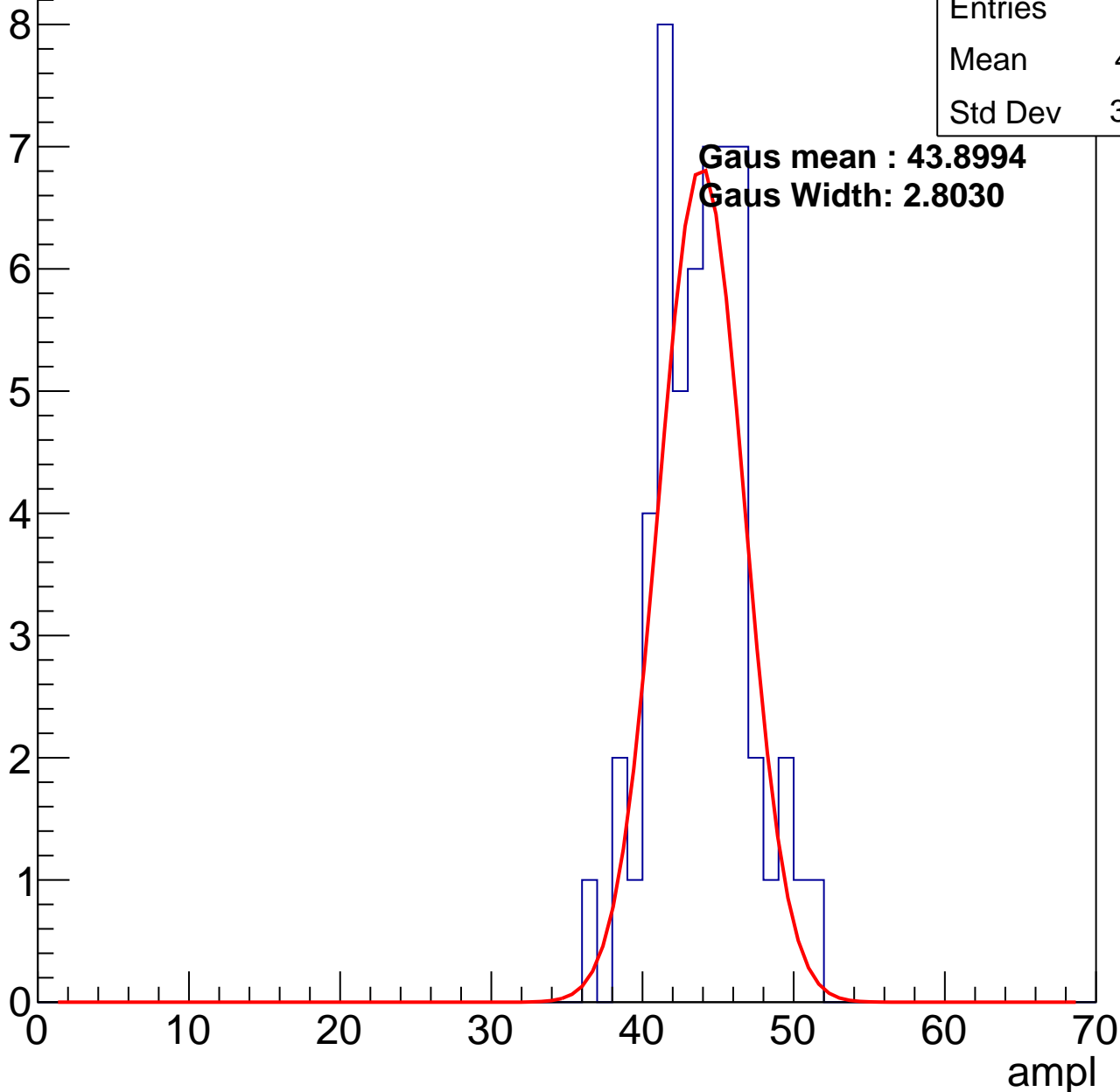
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	55
Mean	43.51
Std Dev	3.056

**Gaus mean : 43.8994**

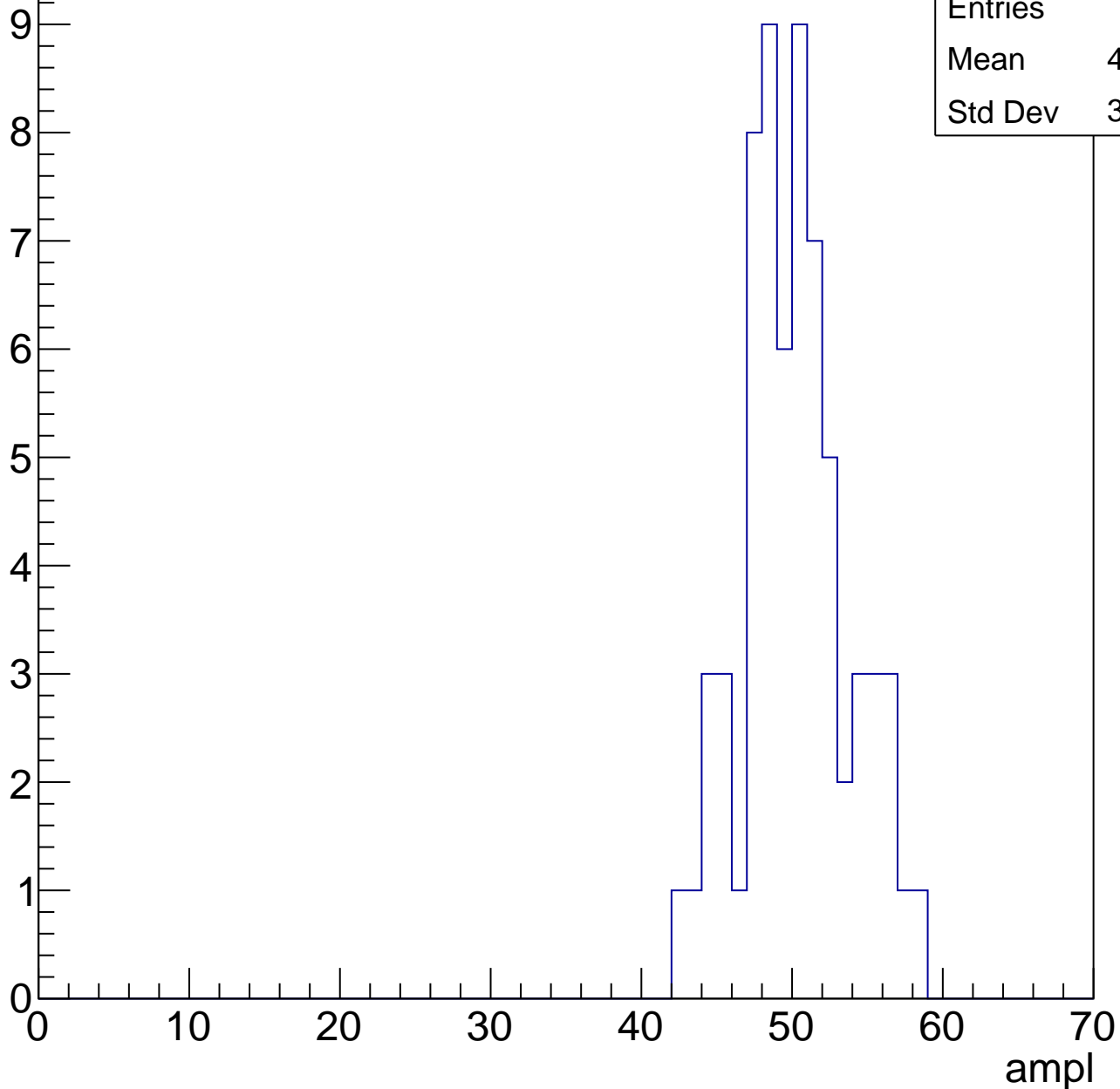
**Gaus Width: 2.8030**



# B1L103S, U9-ch17, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

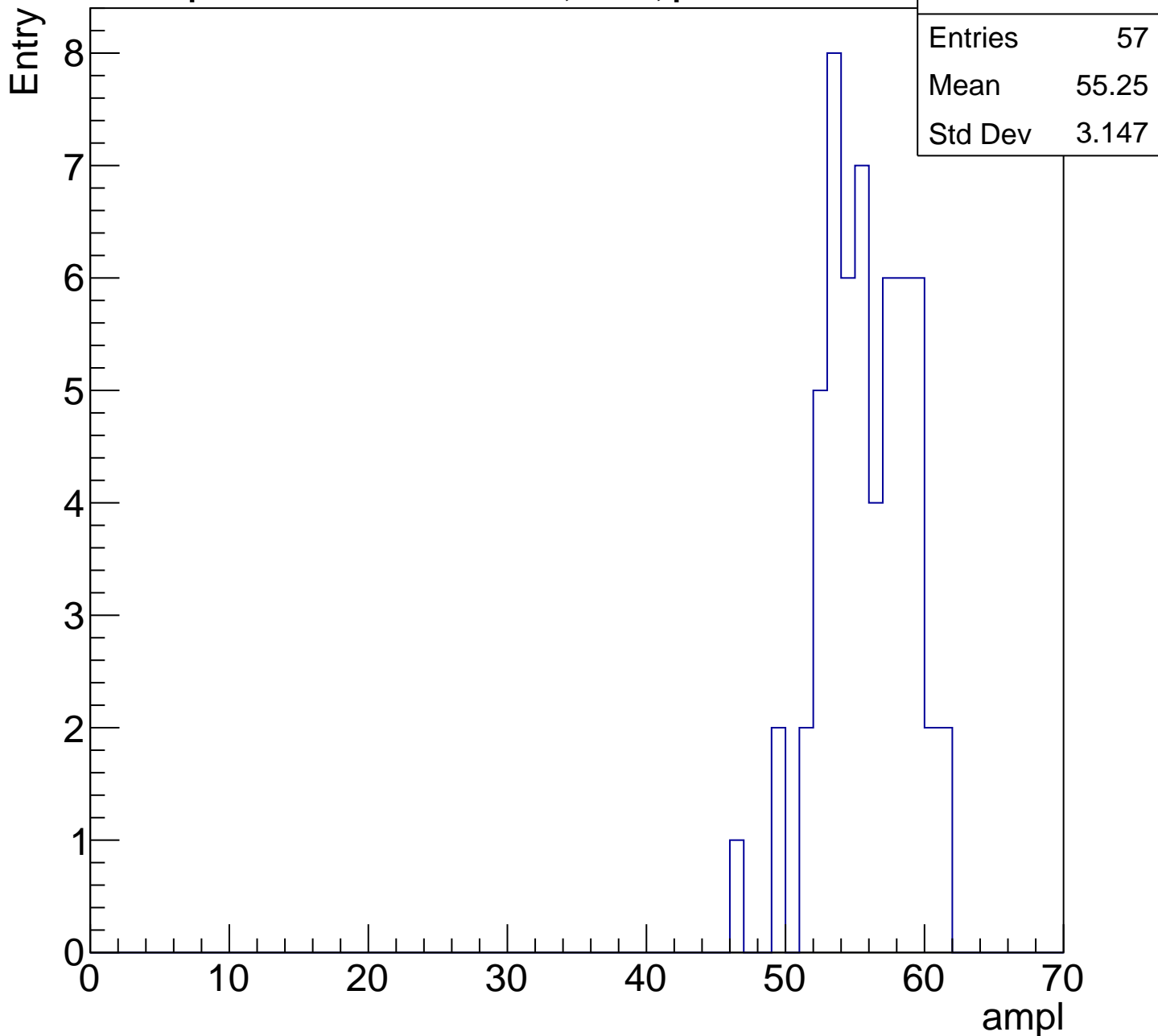
Entry



Entries	66
Mean	49.74
Std Dev	3.505

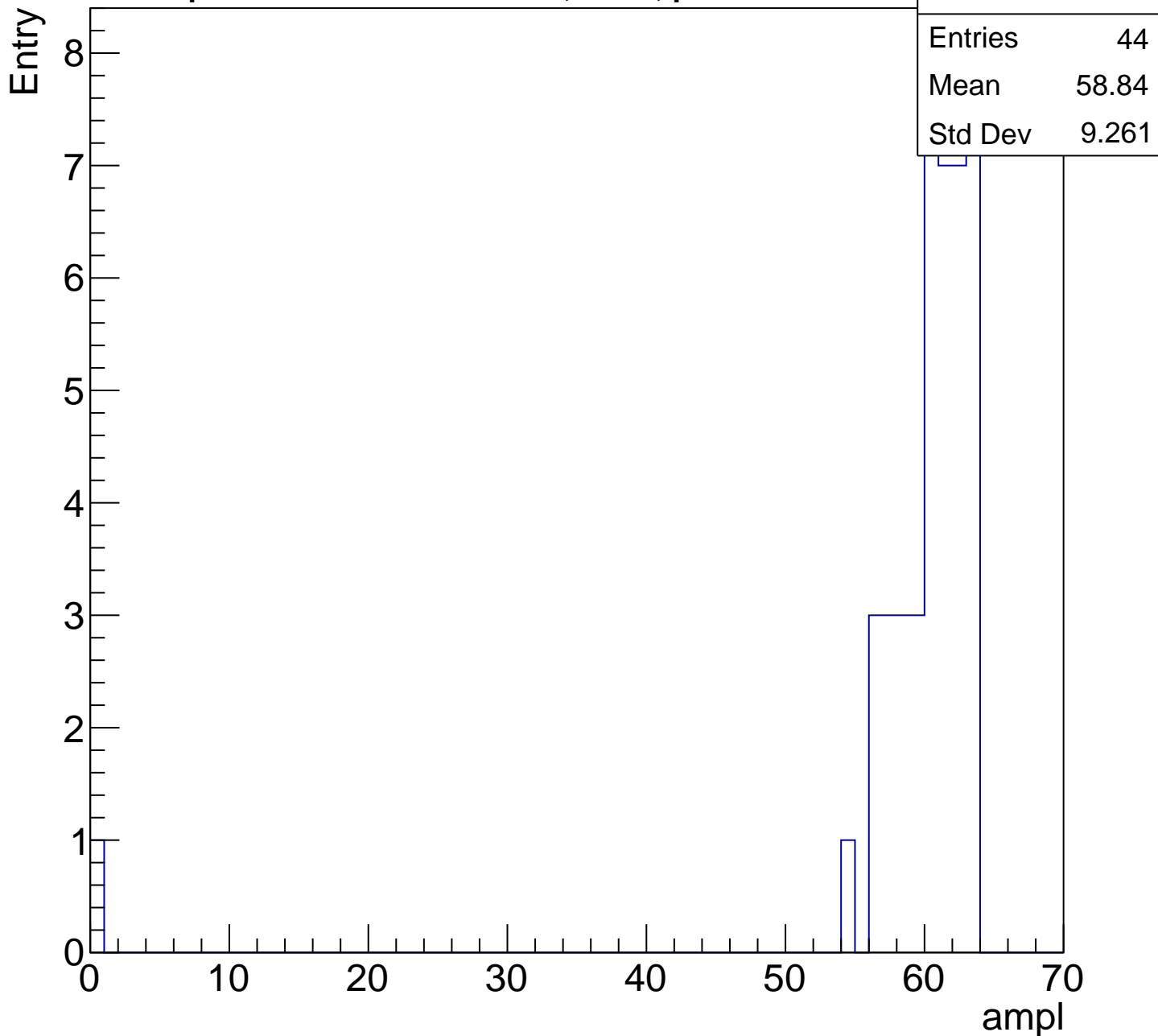
# B1L103S, U9-ch17, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U9-ch17, adc5

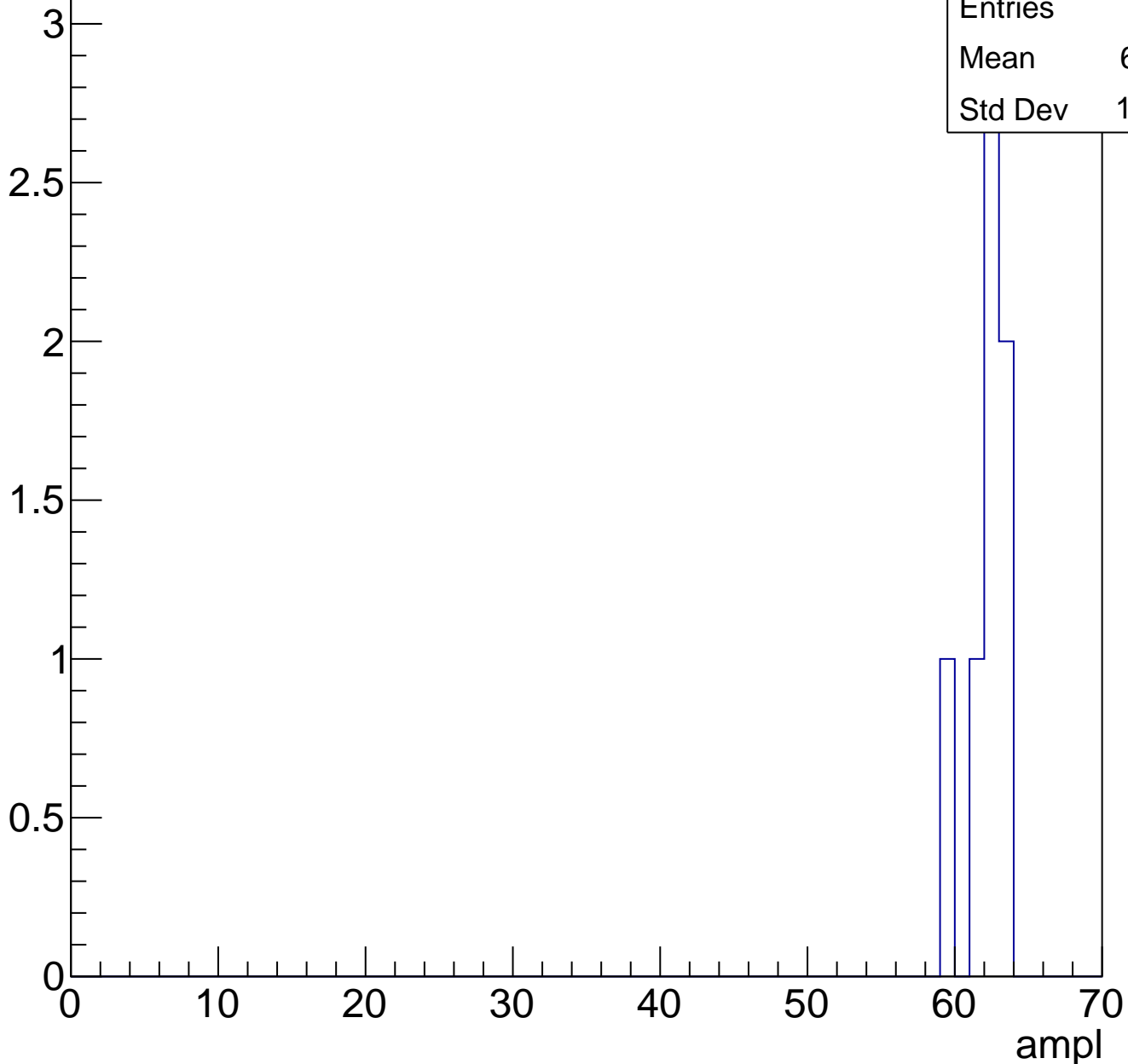
calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U9-ch17, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	7
Mean	61.71
Std Dev	1.278



# B1L103S, U9-ch17, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L103S, U9-ch18, adc0

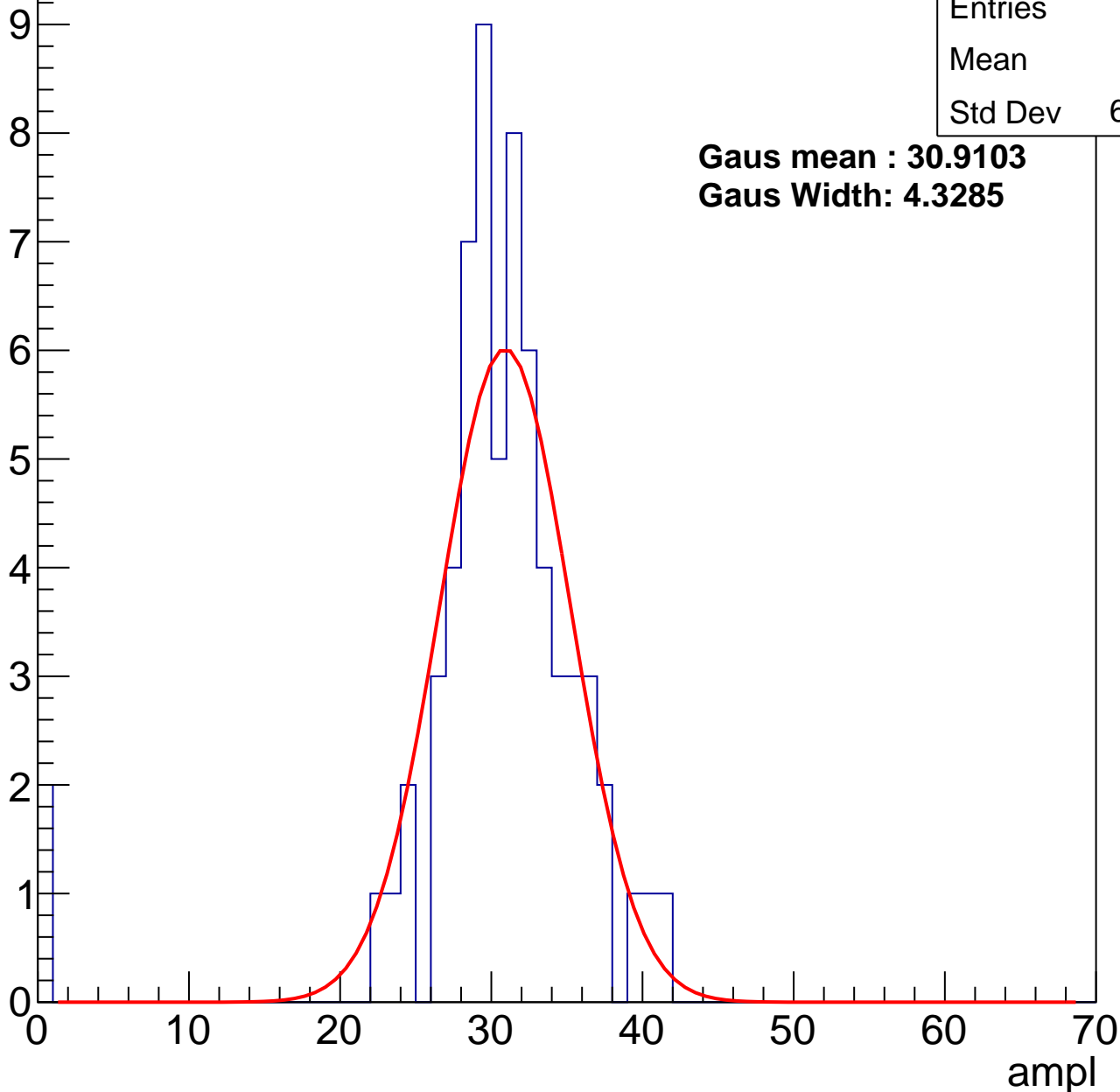
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	29.8
Std Dev	6.516

**Gaus mean : 30.9103**

**Gaus Width: 4.3285**



# B1L103S, U9-ch18, adc1

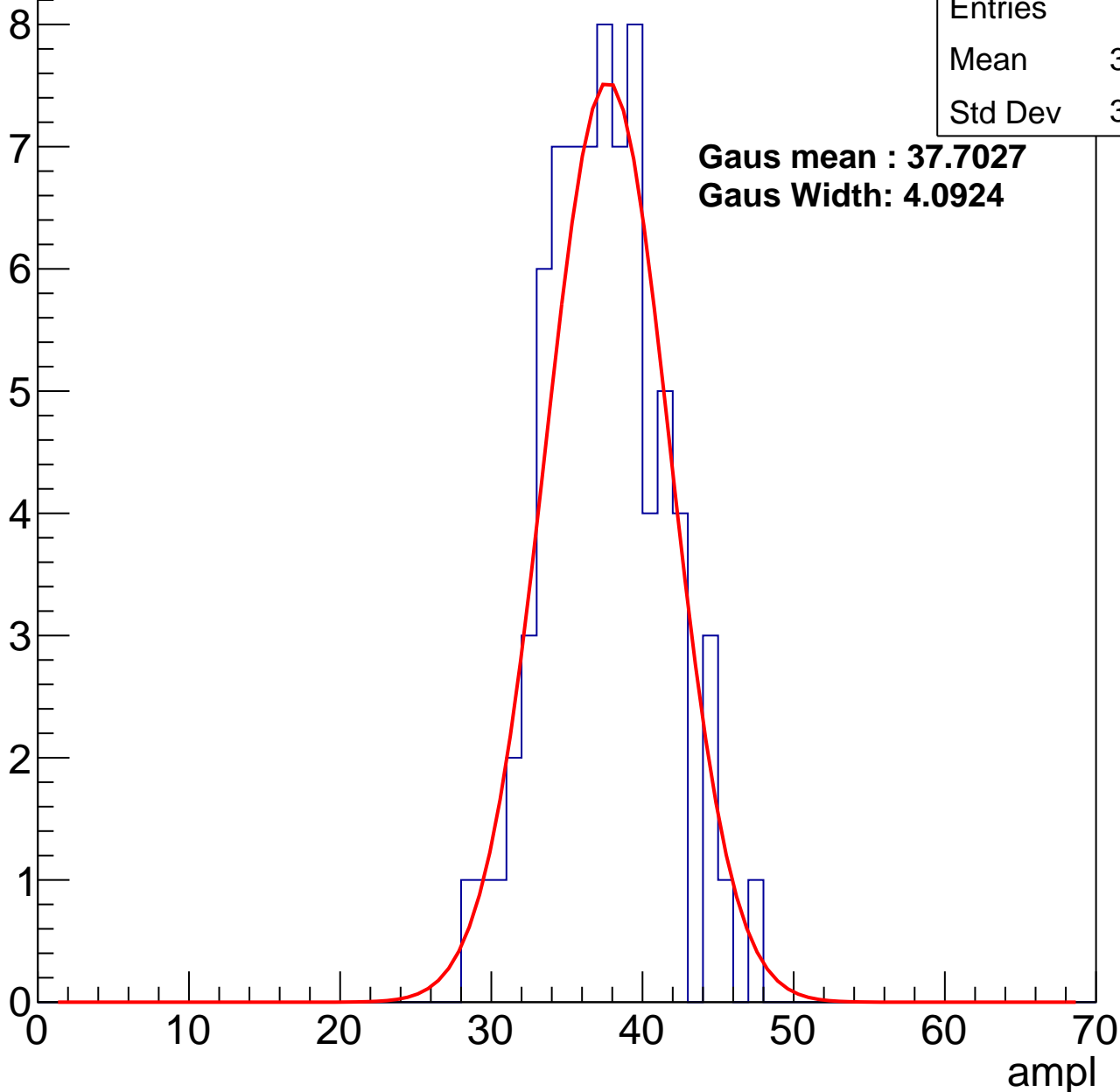
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	76
Mean	36.96
Std Dev	3.806

**Gaus mean : 37.7027**

**Gaus Width: 4.0924**



# B1L103S, U9-ch18, adc2

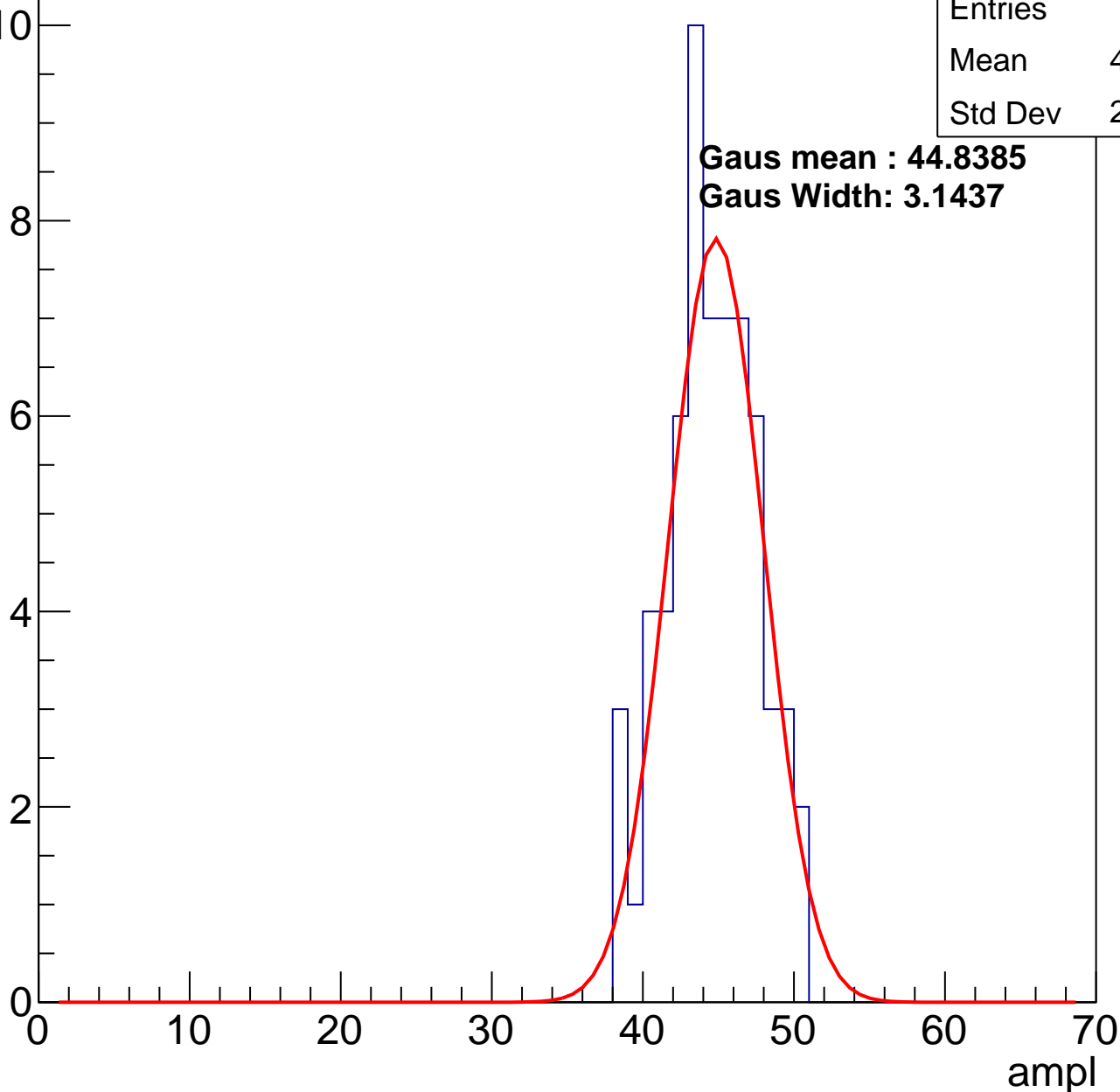
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	44.08
Std Dev	2.956

**Gaus mean : 44.8385**

**Gaus Width: 3.1437**

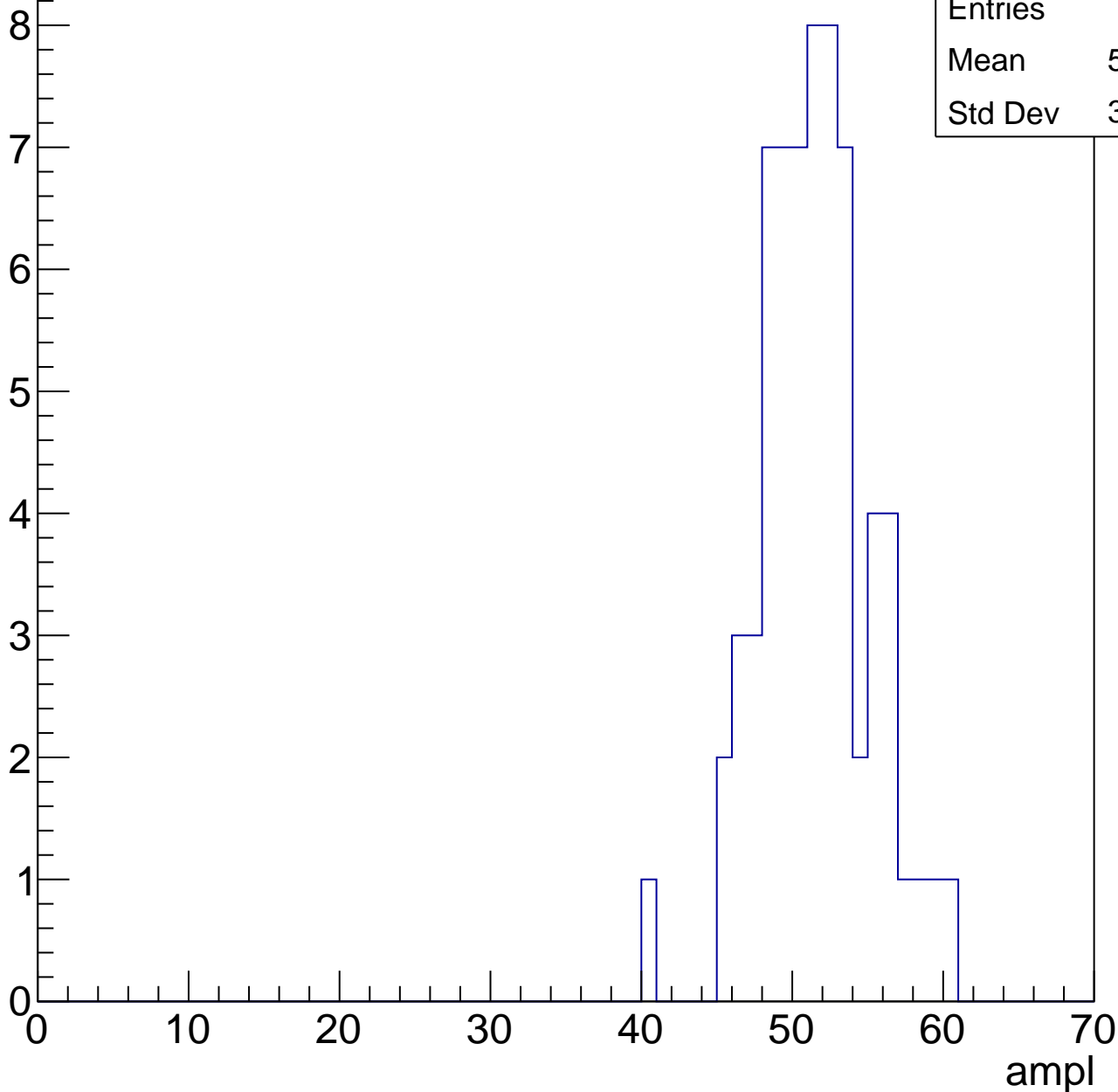


# B1L103S, U9-ch18, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

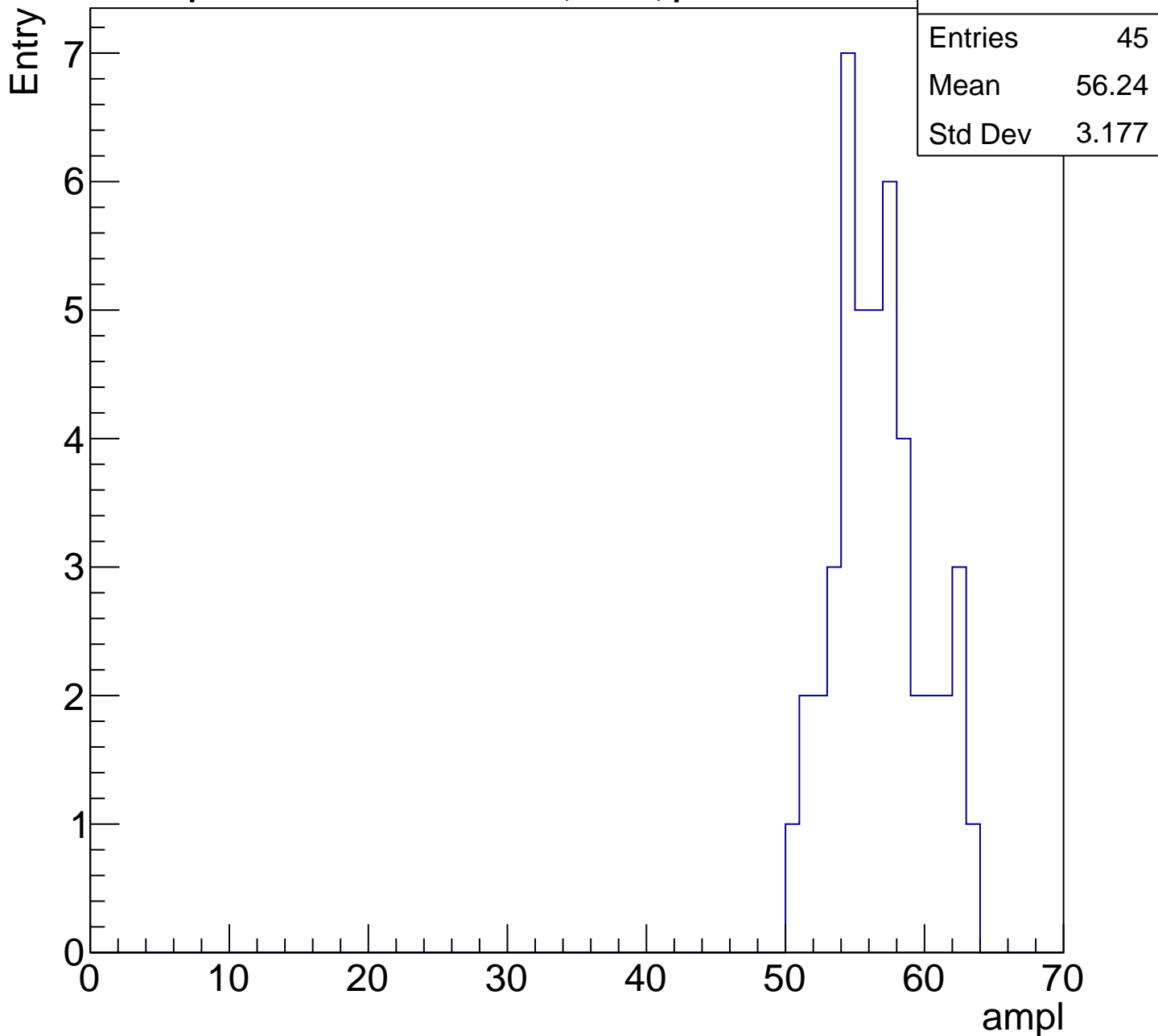
Entry

Entries	67
Mean	51.03
Std Dev	3.587



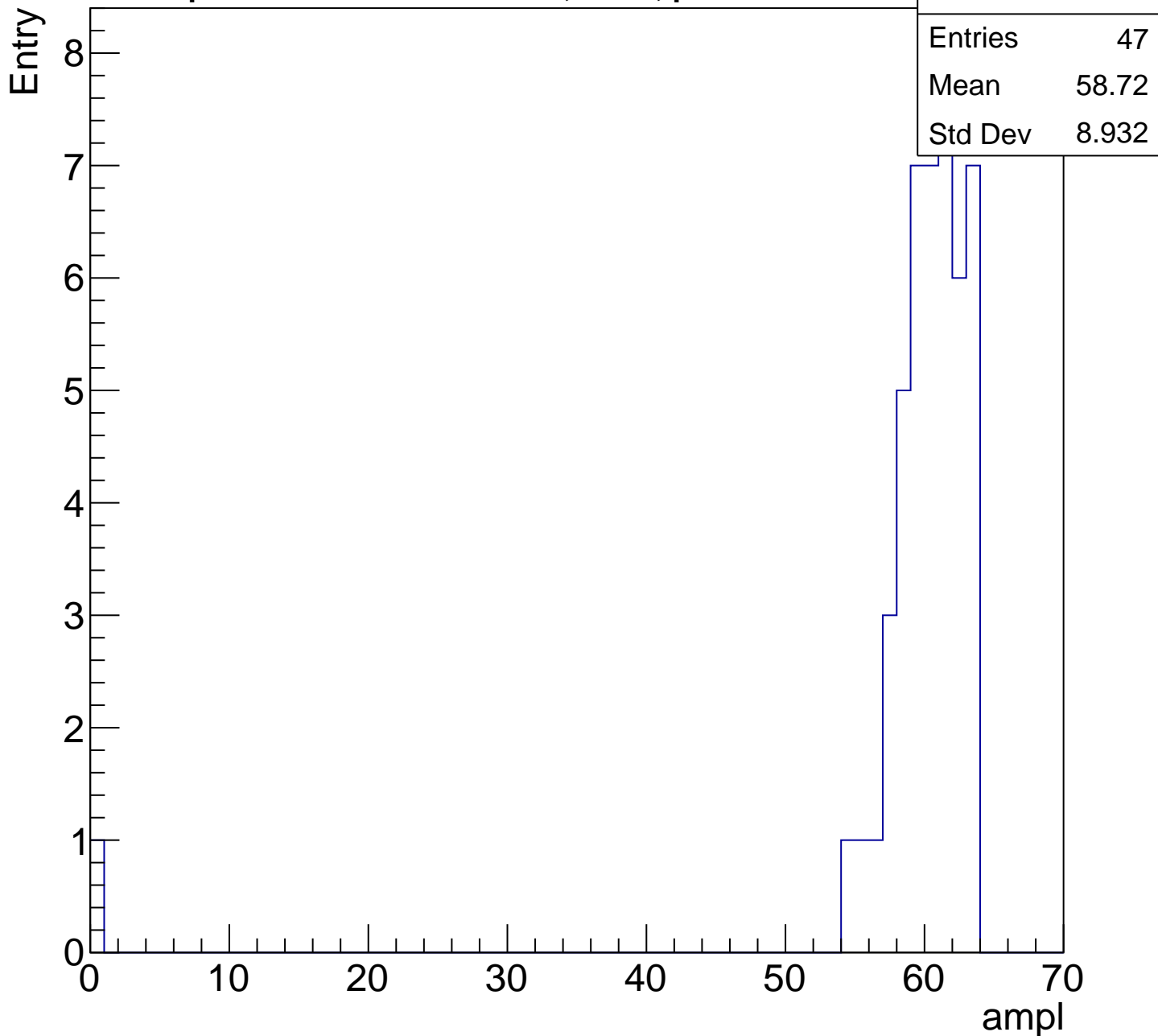
# B1L103S, U9-ch18, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U9-ch18, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U9-ch18, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U9-ch18, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U9-ch19, adc0

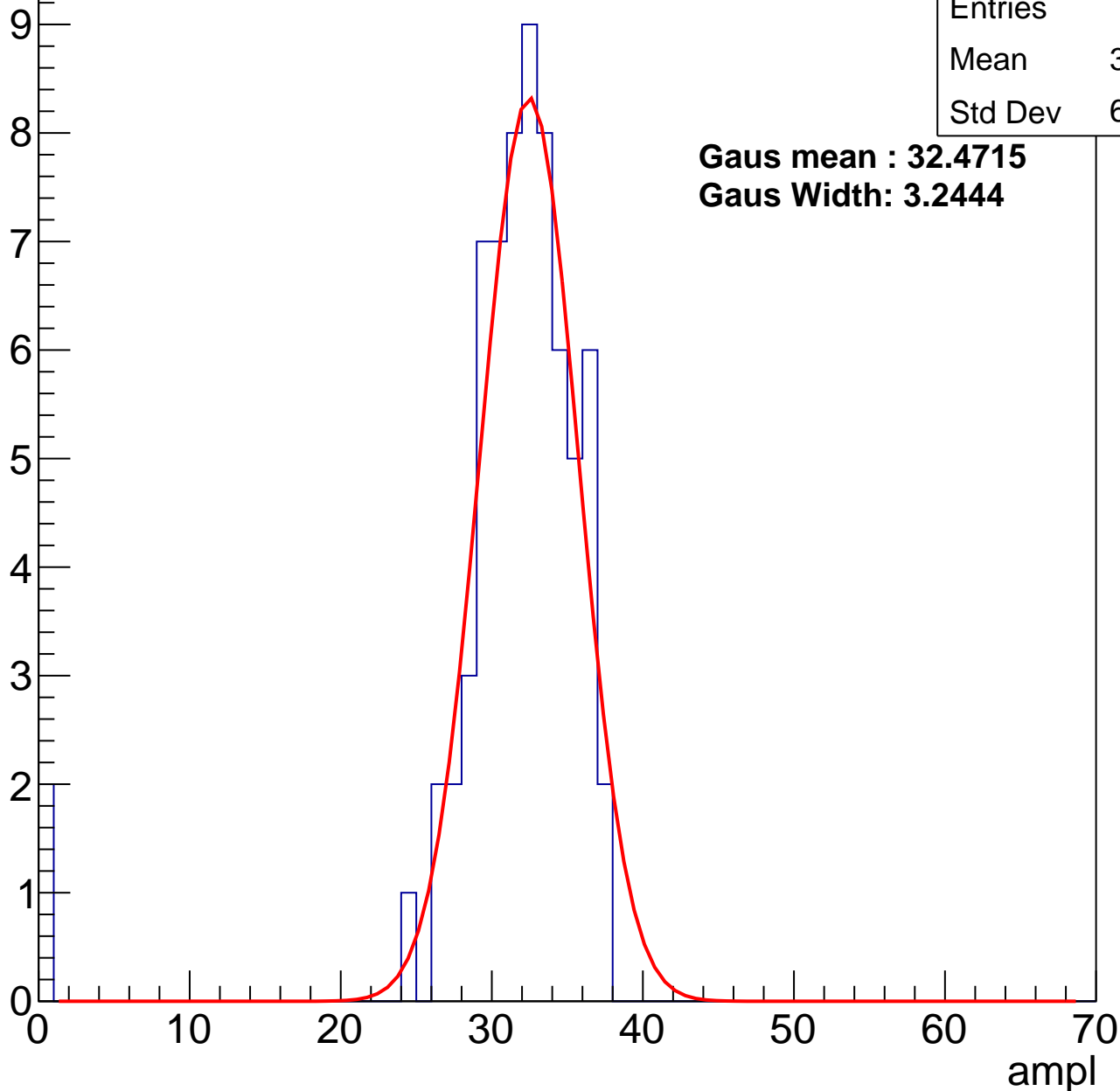
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	68
Mean	30.82
Std Dev	6.075

**Gaus mean : 32.4715**

**Gaus Width: 3.2444**



# B1L103S, U9-ch19, adc1

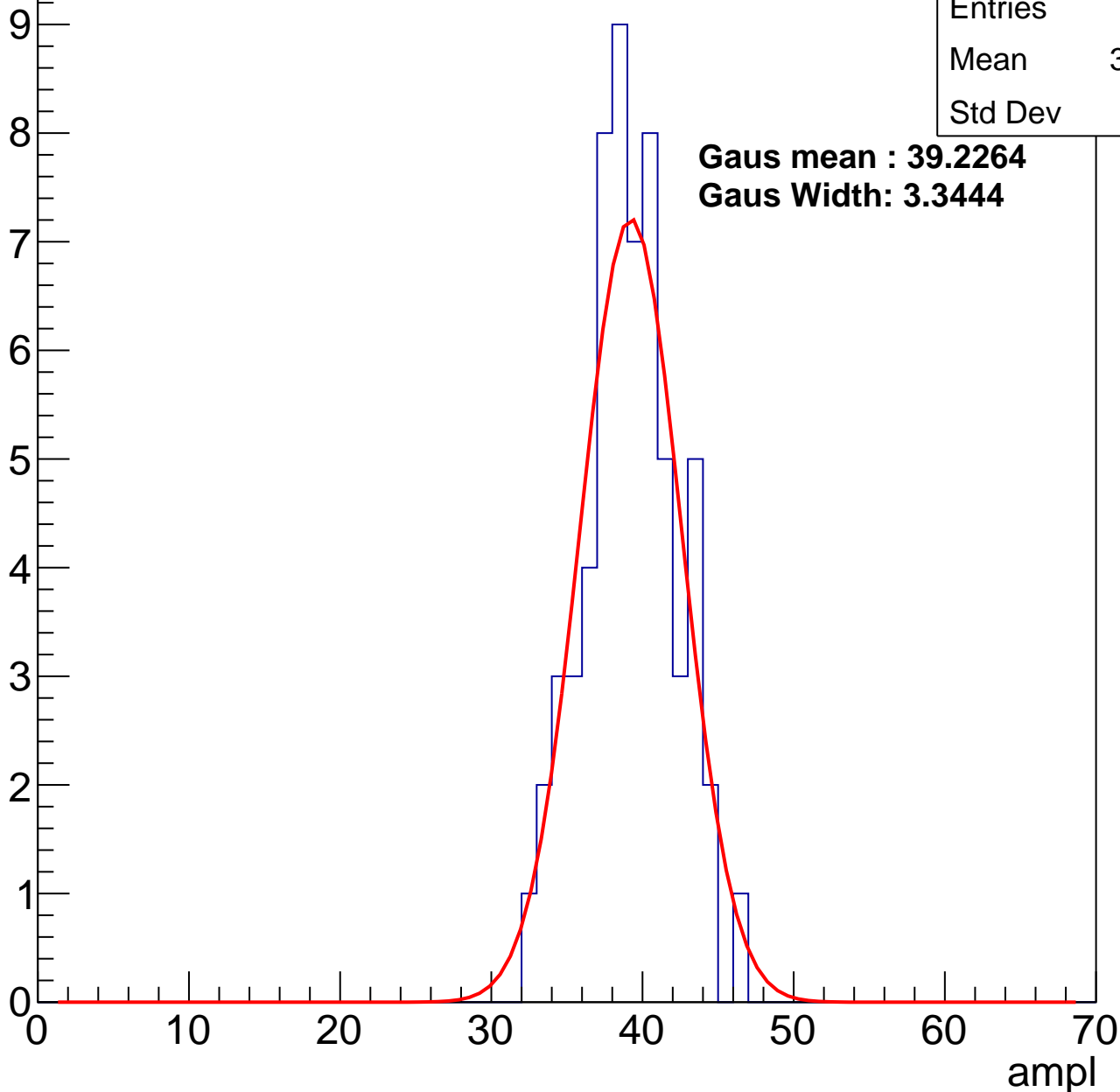
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	61
Mean	38.69
Std Dev	3

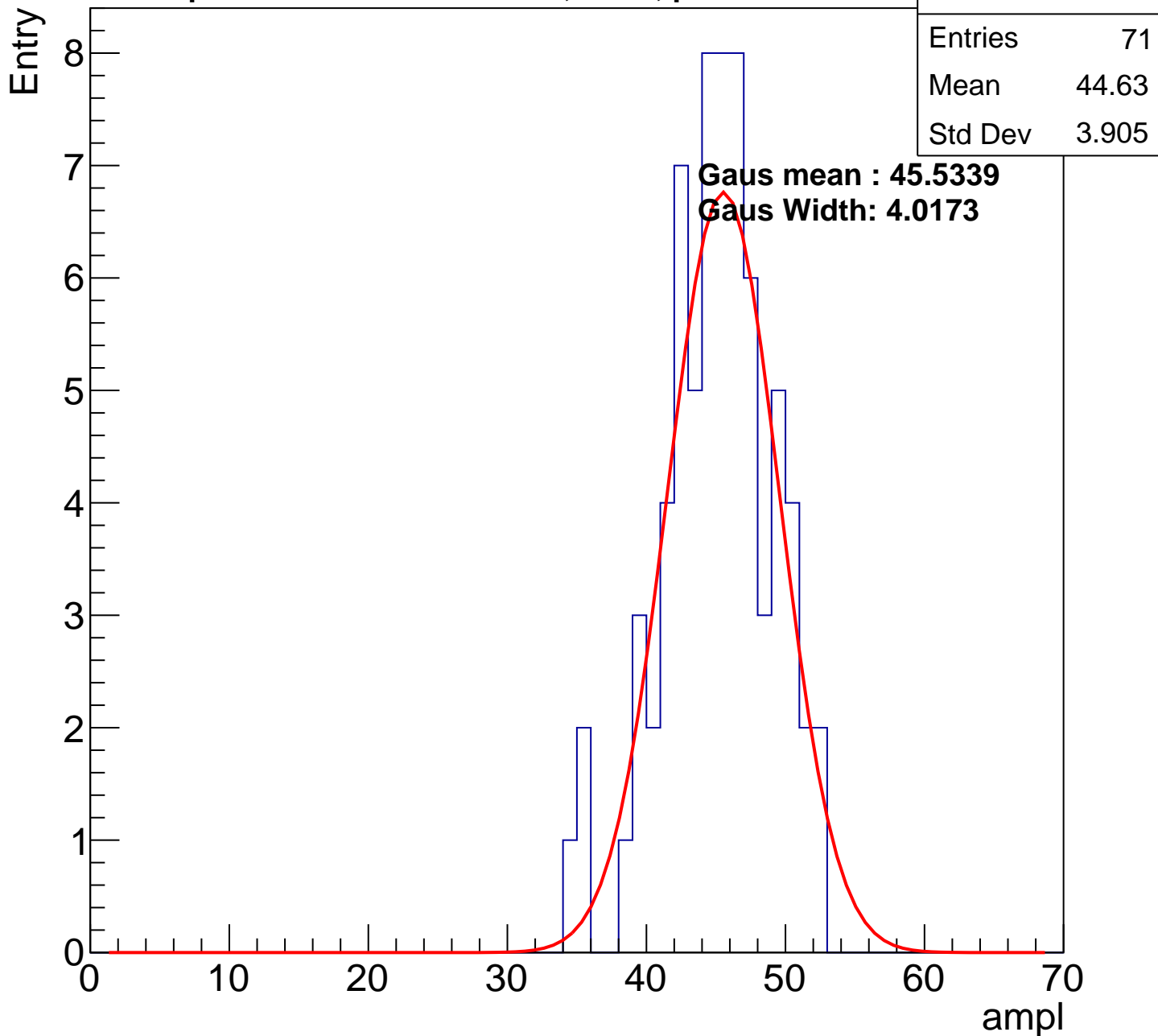
**Gaus mean : 39.2264**

**Gaus Width: 3.3444**



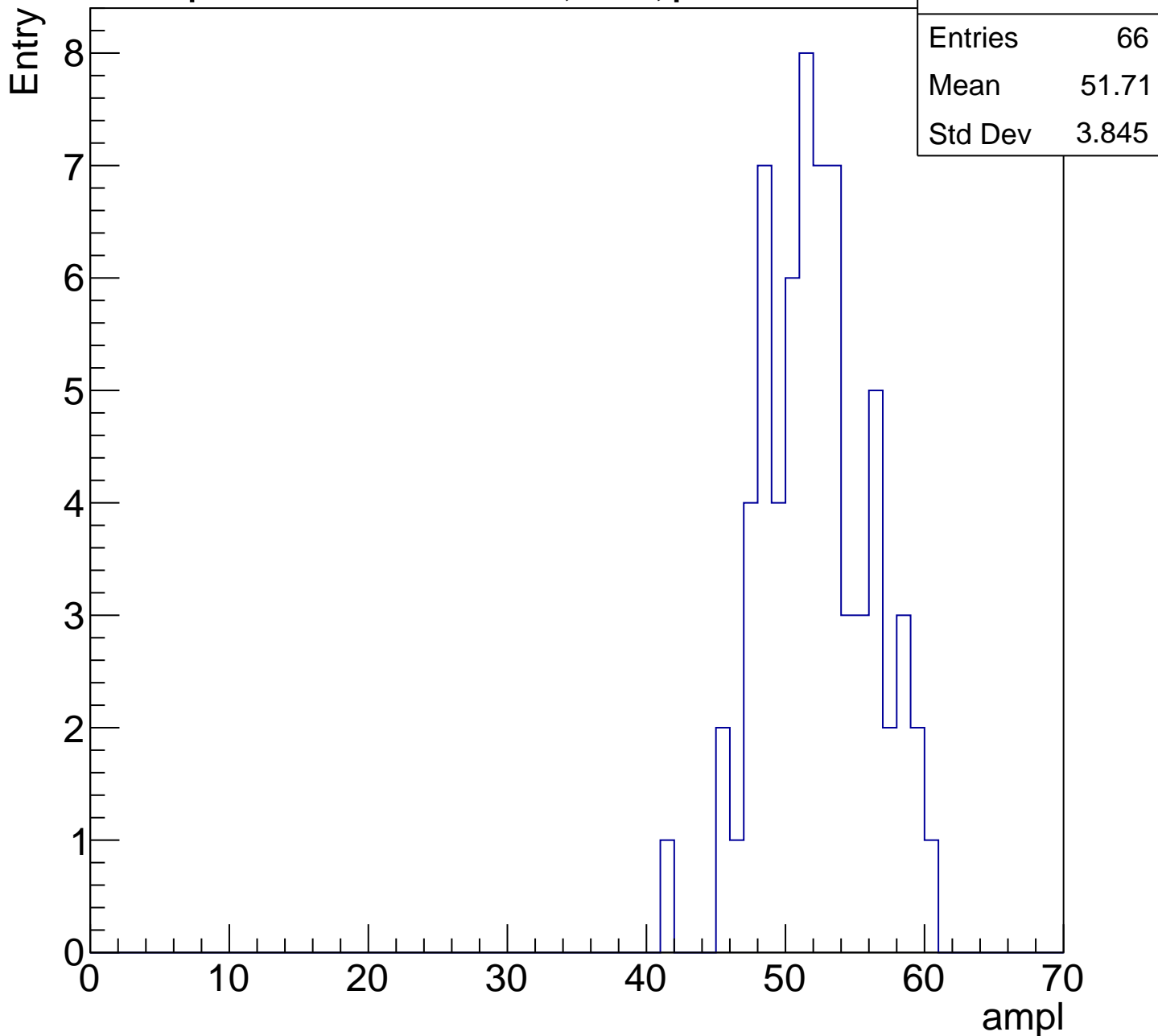
# B1L103S, U9-ch19, adc2

calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U9-ch19, adc3

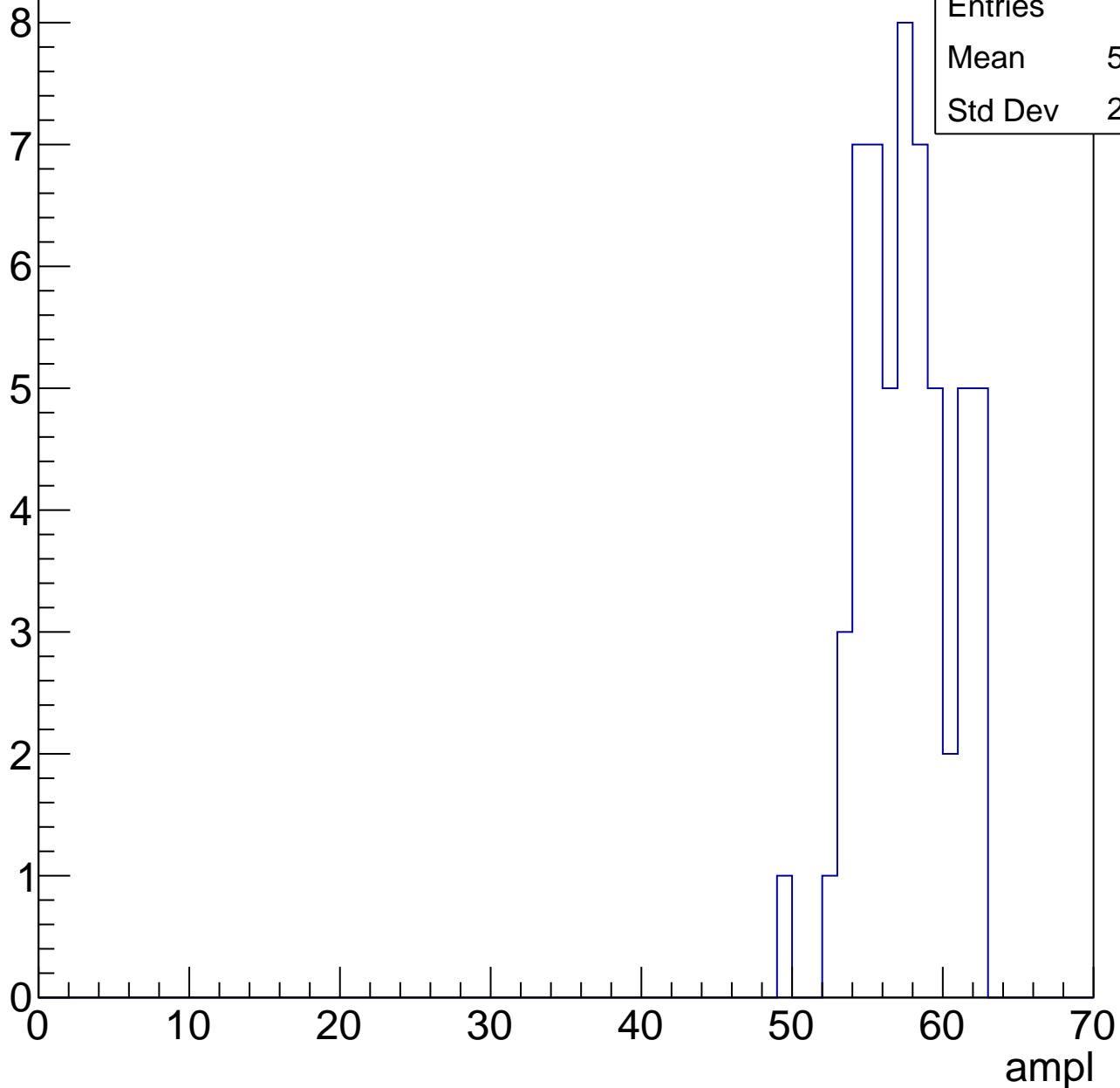
calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U9-ch19, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	56
Mean	57.05
Std Dev	2.936

# B1L103S, U9-ch19, adc5

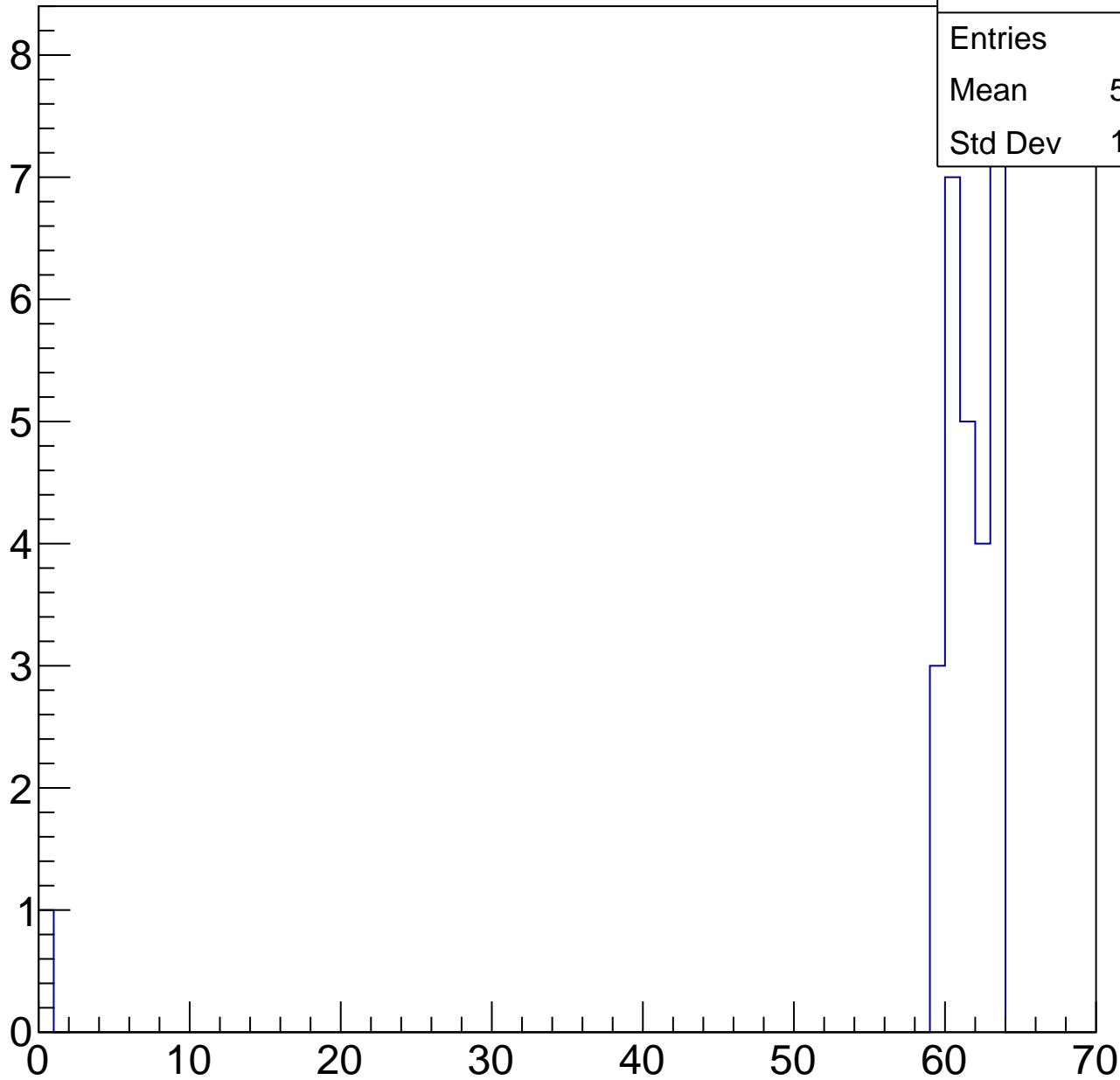
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	28
Mean	59.07
Std Dev	11.45

ampl



# B1L103S, U9-ch19, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U9-ch19, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U9-ch20, adc0

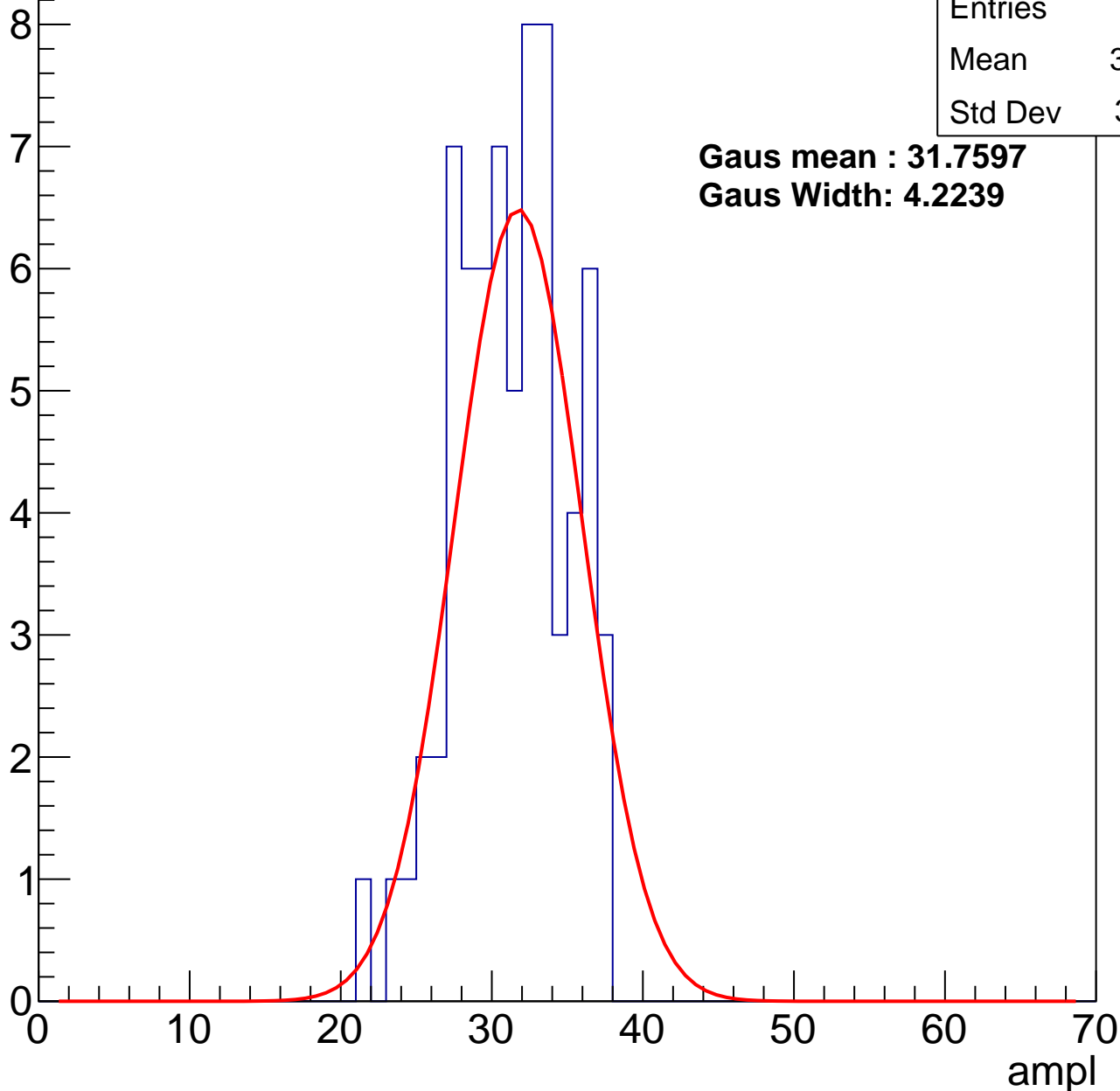
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	70
Mean	30.79
Std Dev	3.621

**Gaus mean : 31.7597**

**Gaus Width: 4.2239**



# B1L103S, U9-ch20, adc1

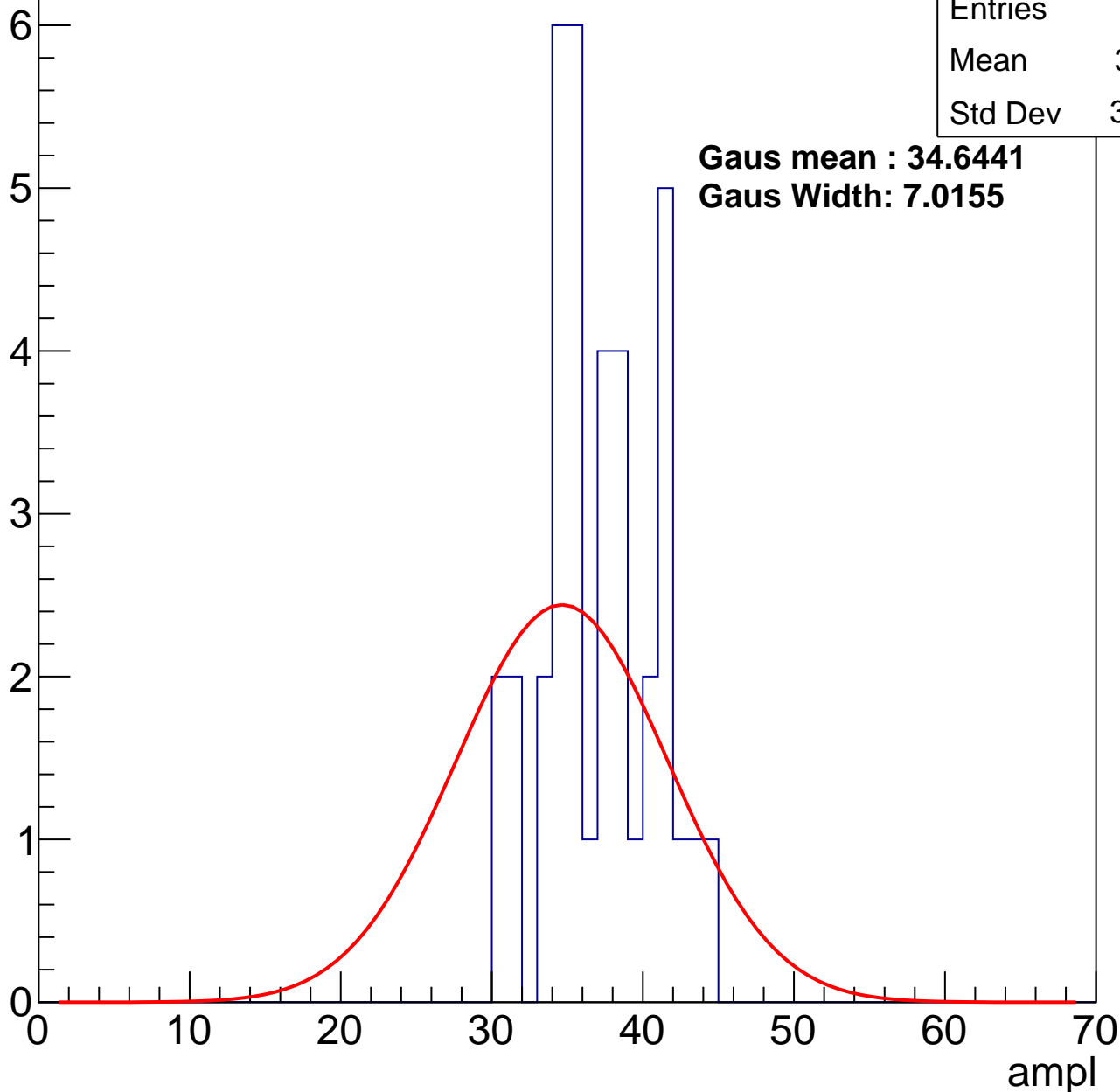
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	38
Mean	36.61
Std Dev	3.595

**Gaus mean : 34.6441**

**Gaus Width: 7.0155**



# B1L103S, U9-ch20, adc2

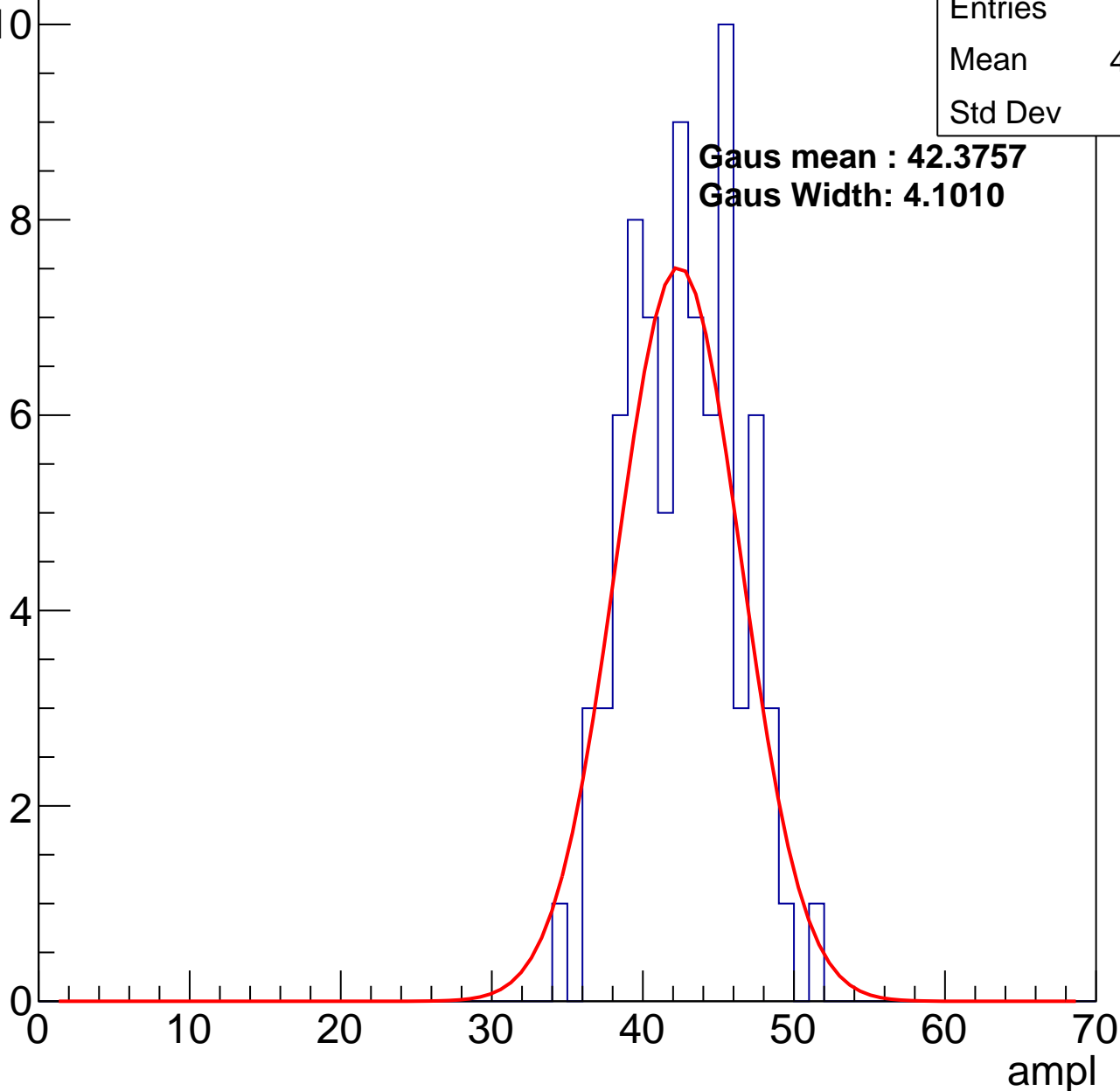
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	79
Mean	42.22
Std Dev	3.56

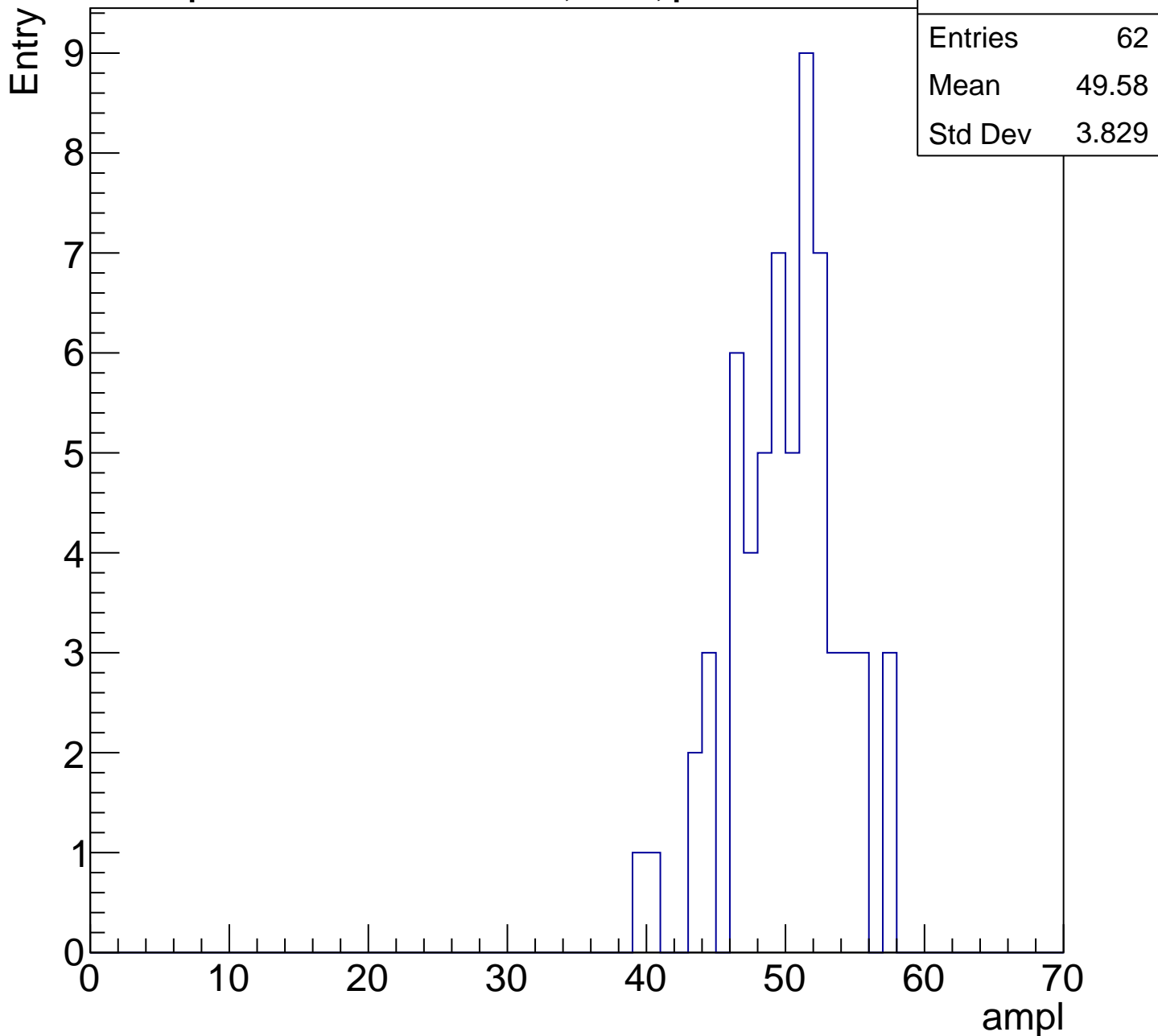
**Gaus mean : 42.3757**

**Gaus Width: 4.1010**



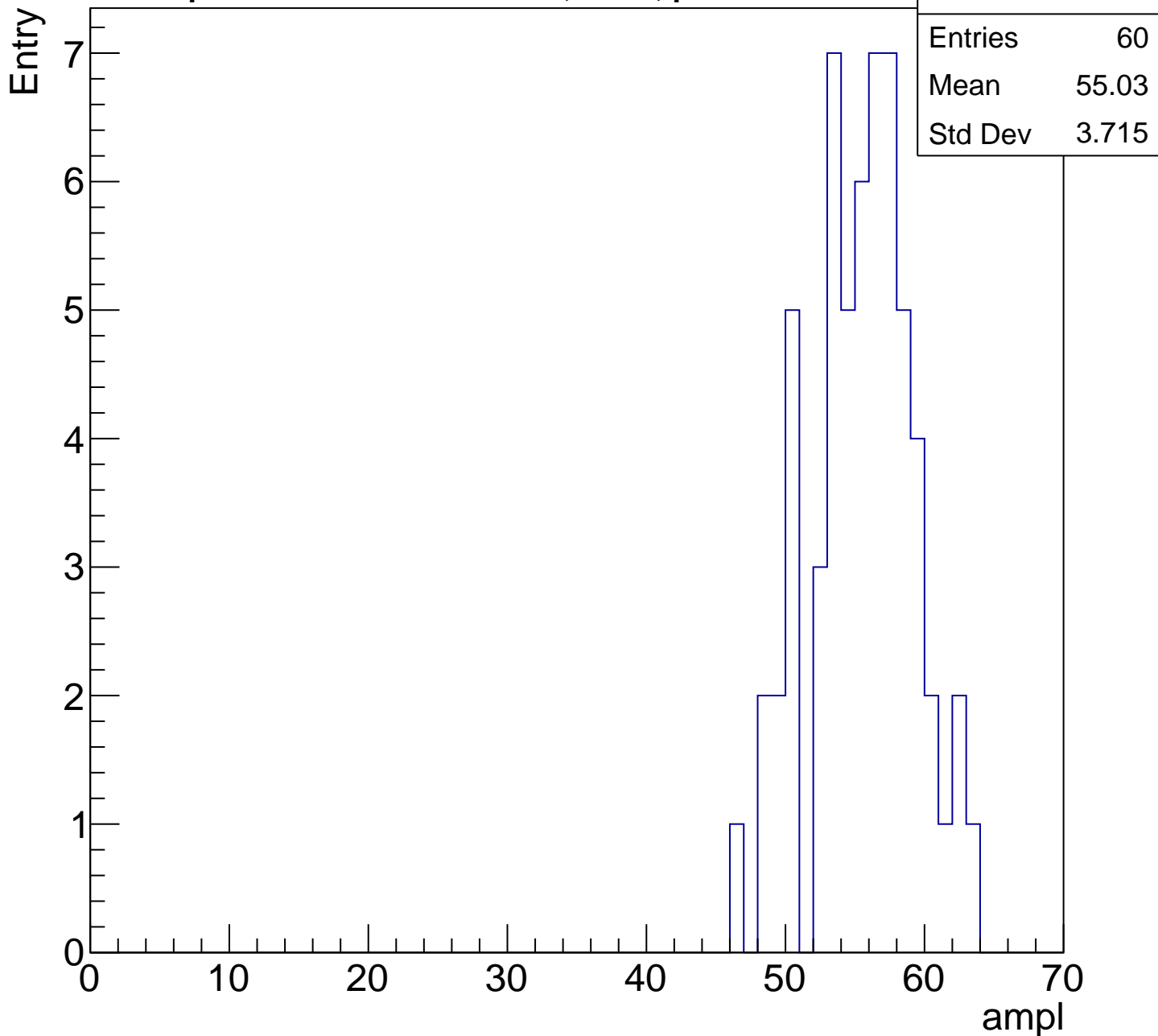
# B1L103S, U9-ch20, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U9-ch20, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

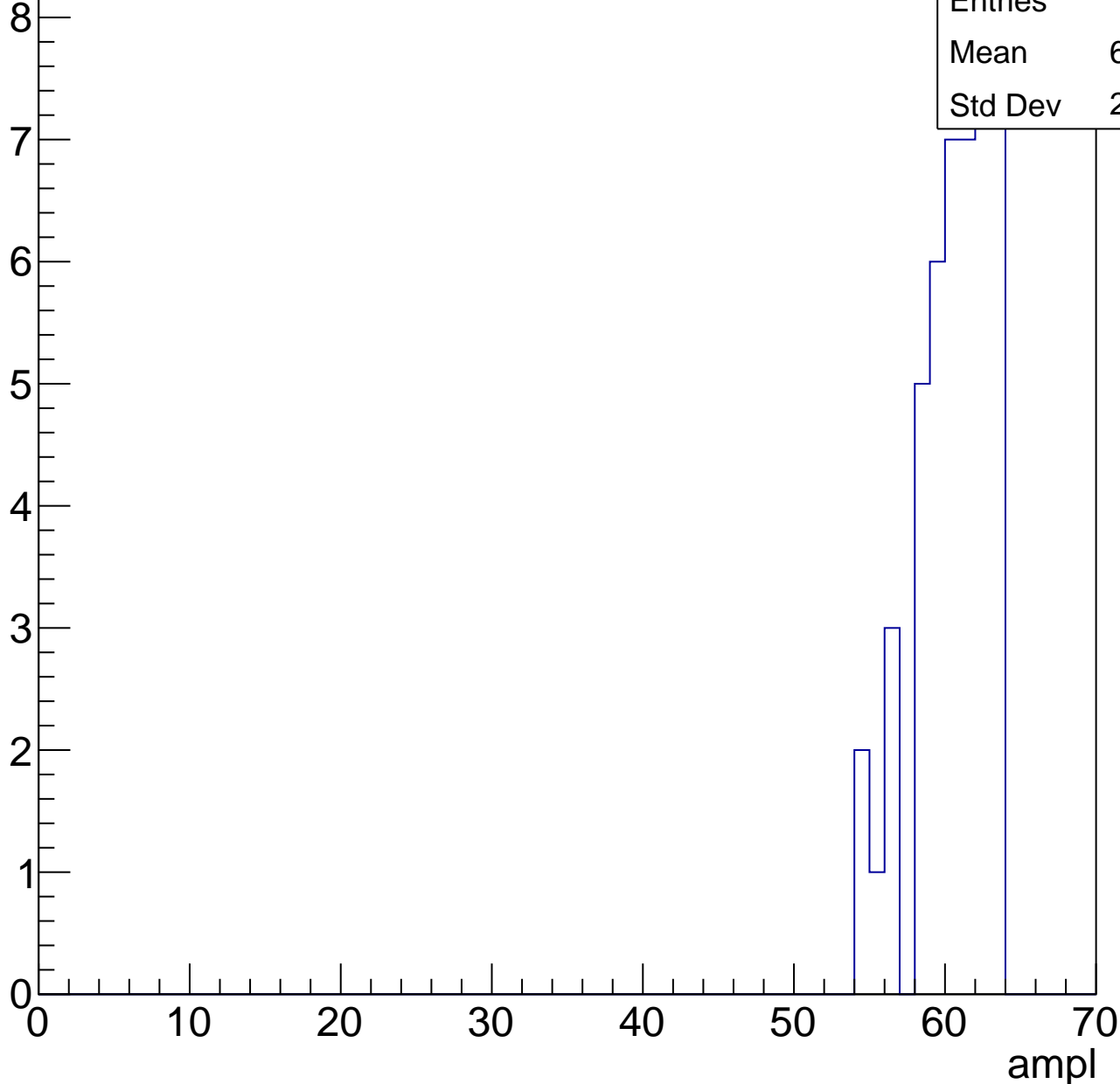


# B1L103S, U9-ch20, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	47
Mean	60.04
Std Dev	2.449



# B1L103S, U9-ch20, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

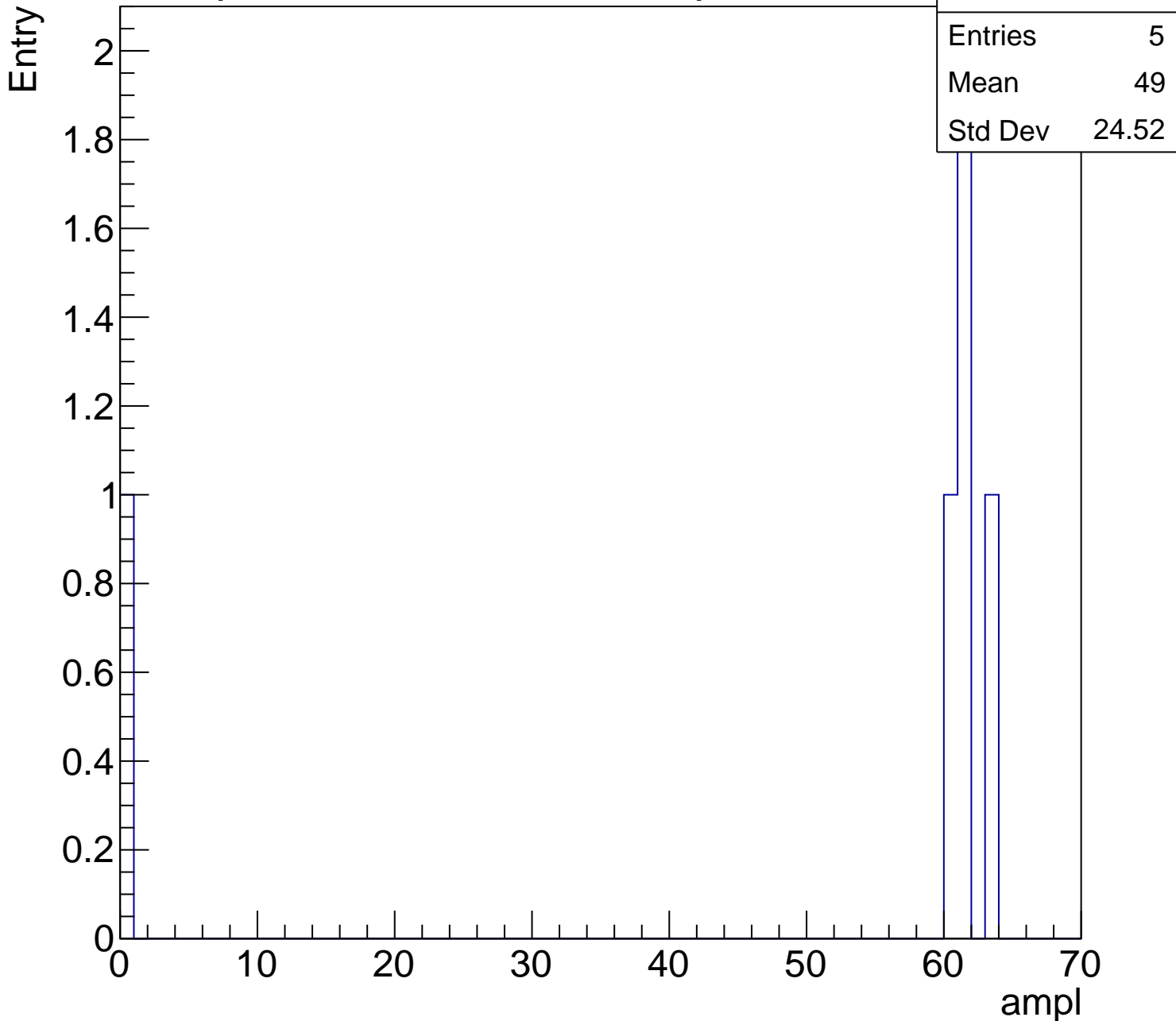
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	5
Mean	49
Std Dev	24.52

0 10 20 30 40 50 60 70

ampl





# B1L103S, U9-ch20, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L103S, U9-ch21, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	75
Mean	31.2
Std Dev	3.633

**Gaus mean : 31.4619**

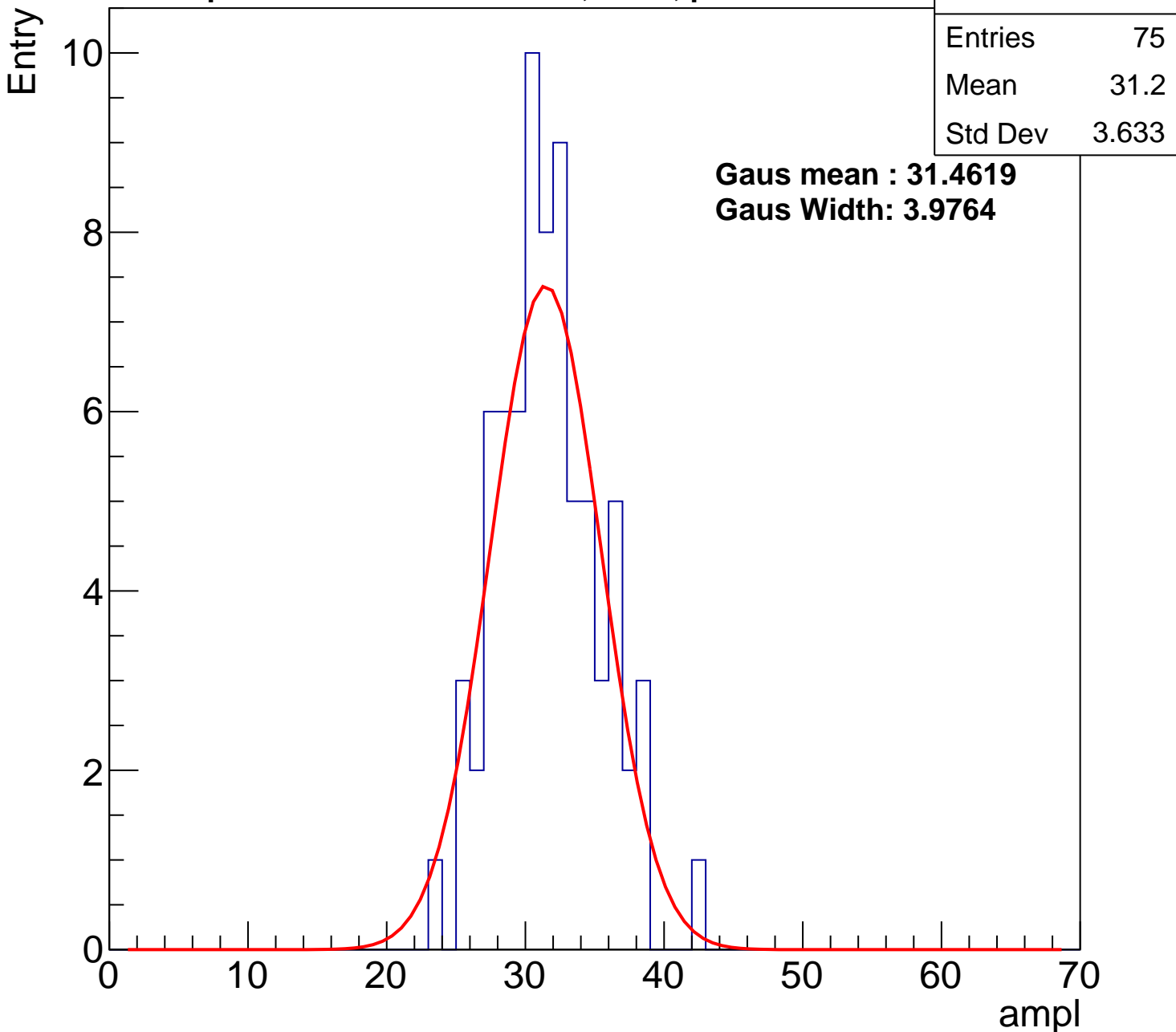
**Gaus Width: 3.9764**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U9-ch21, adc1

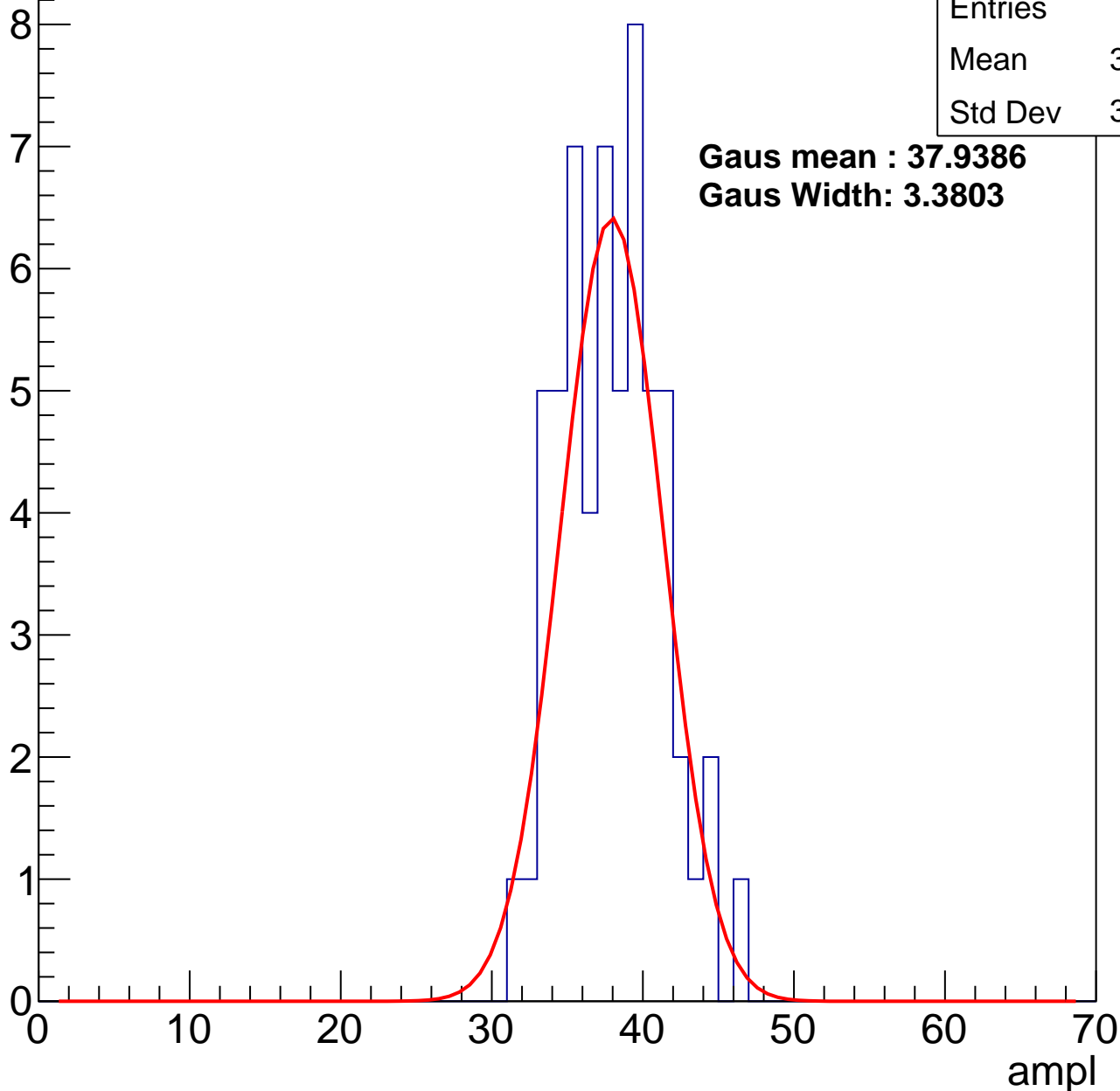
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	59
Mean	37.53
Std Dev	3.264

**Gaus mean : 37.9386**

**Gaus Width: 3.3803**



# B1L103S, U9-ch21, adc2

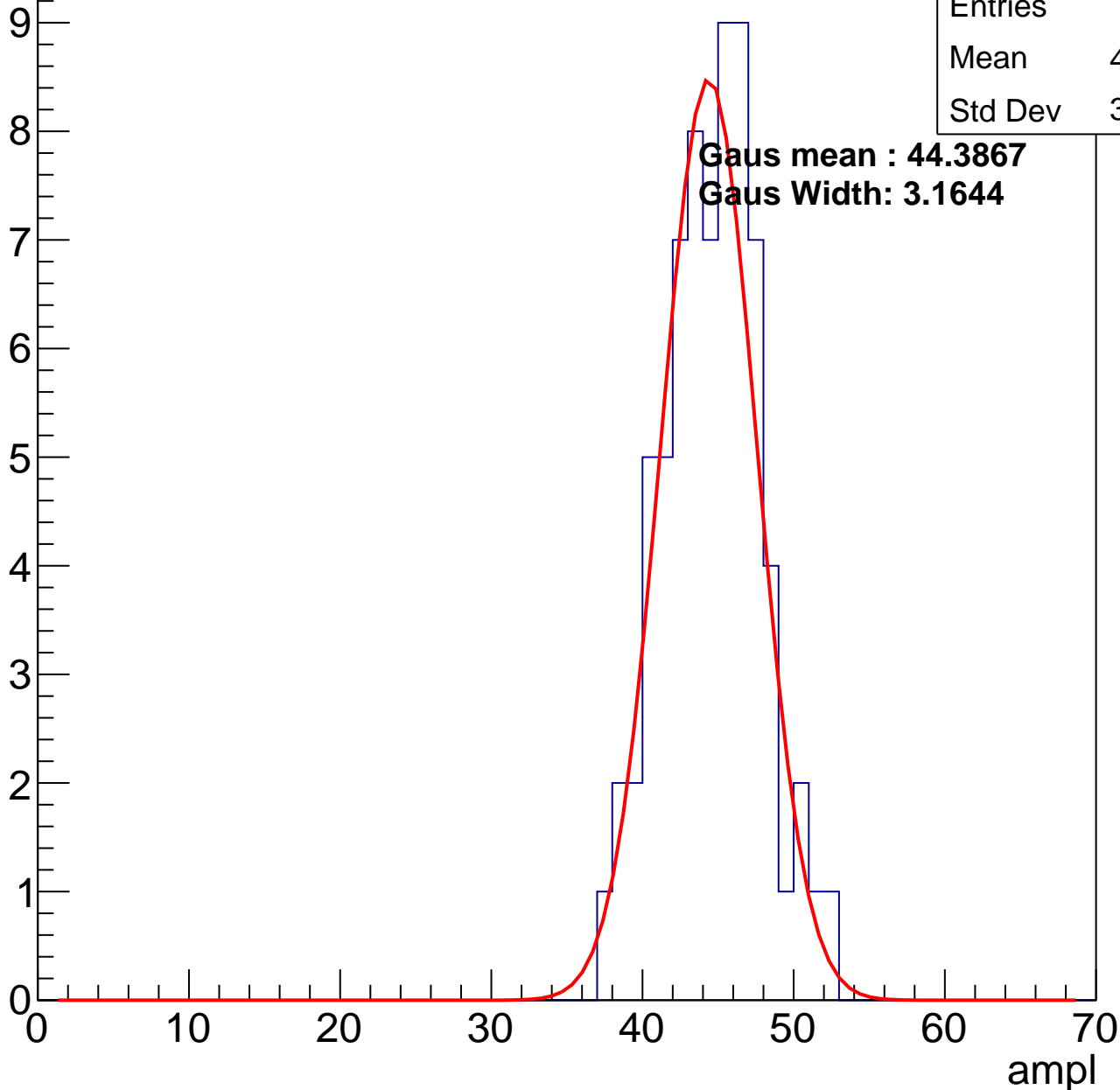
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	71
Mean	44.14
Std Dev	3.168

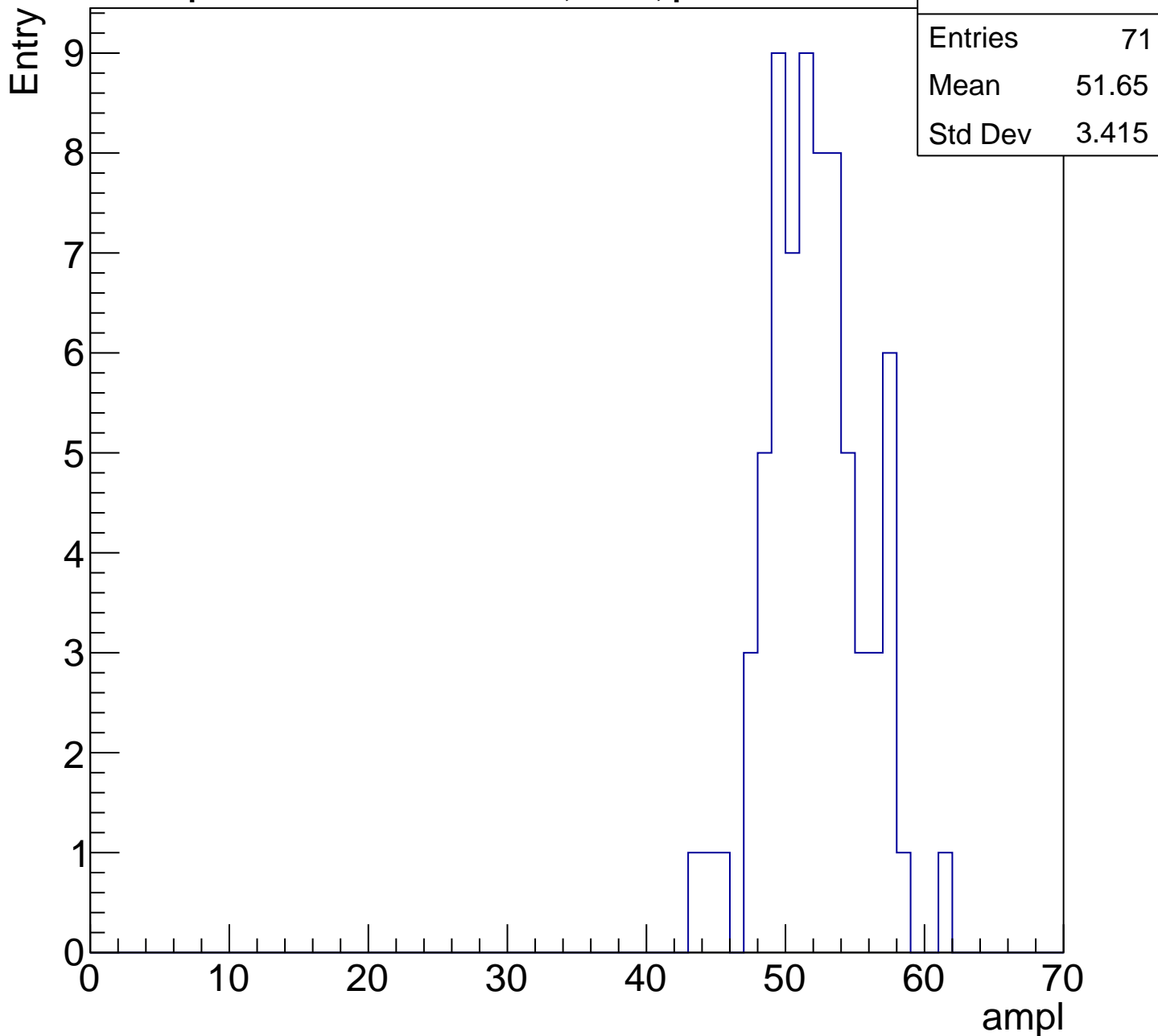
**Gaus mean : 44.3867**

**Gaus Width: 3.1644**



# B1L103S, U9-ch21, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

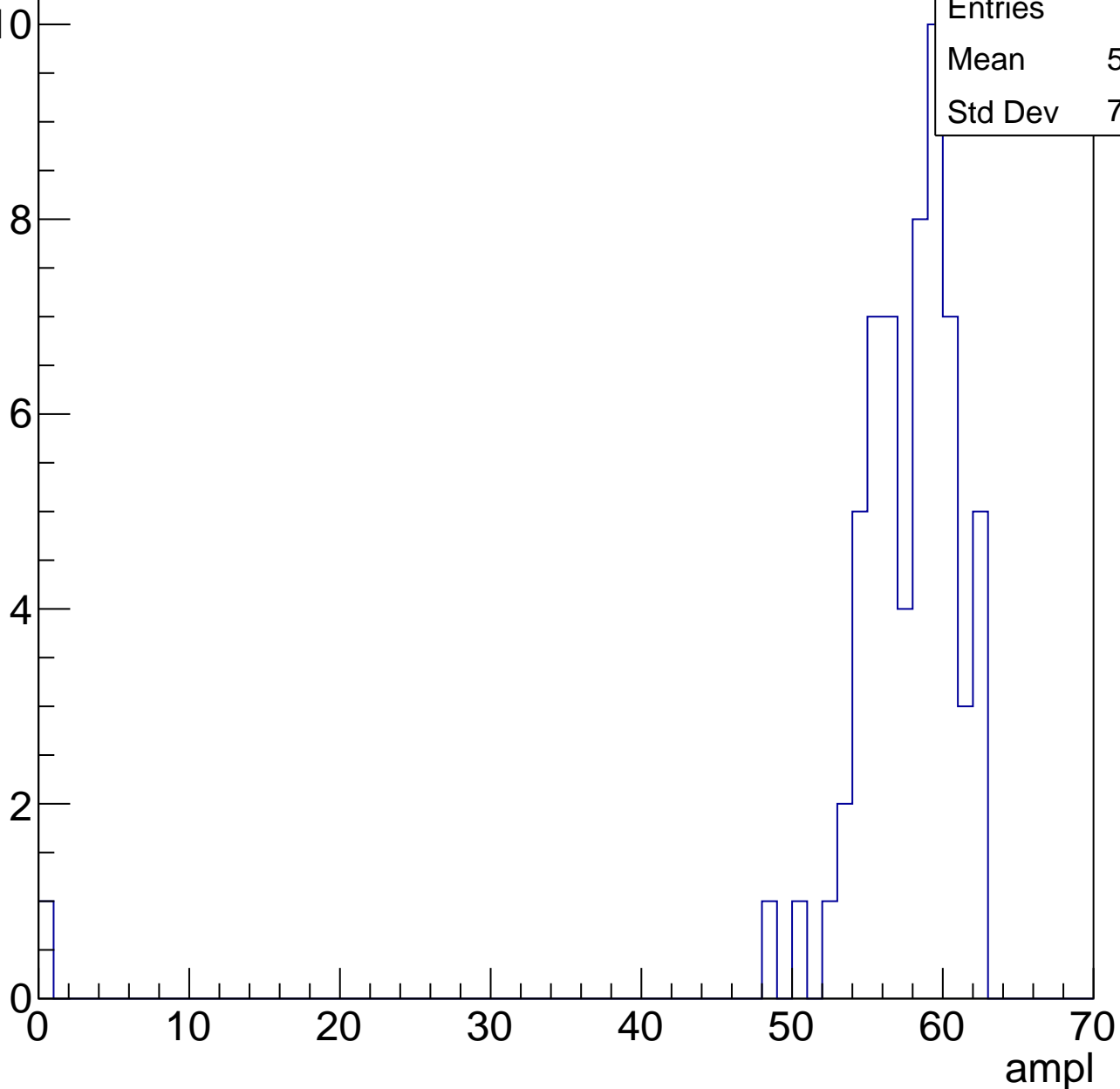


# B1L103S, U9-ch21, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	56.42
Std Dev	7.807



# B1L103S, U9-ch21, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

10

8

6

4

2

0

0

10

20

30

40

50

60

ampl

Entries	25
Mean	61.76
Std Dev	1.305

0

2

4

6

8

10

# B1L103S, U9-ch21, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0



# B1L103S, U9-ch21, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L103S, U9-ch22, adc0

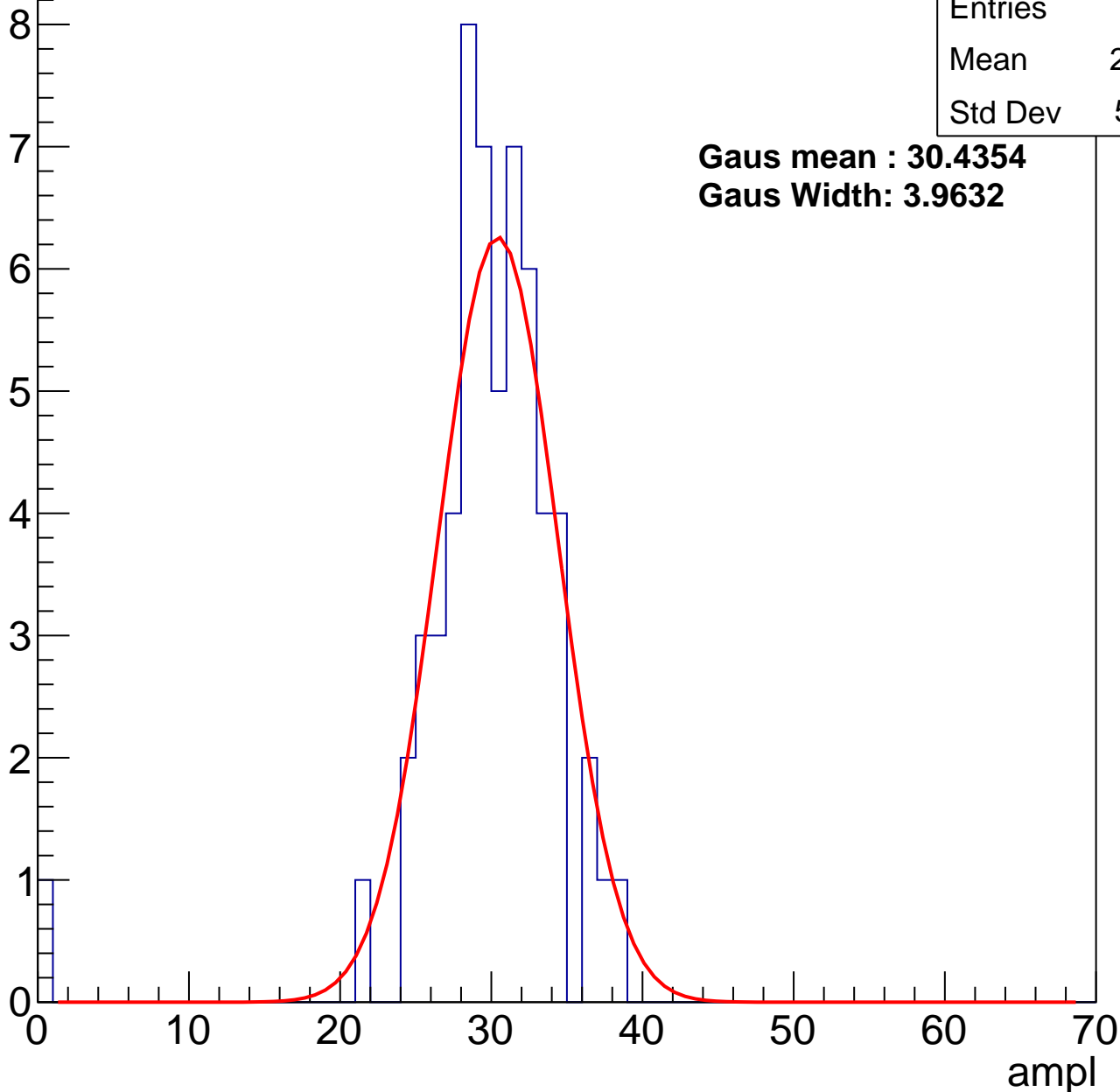
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	59
Mean	29.34
Std Dev	5.111

**Gaus mean : 30.4354**

**Gaus Width: 3.9632**



# B1L103S, U9-ch22, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	79
Mean	35.41
Std Dev	4.077

**Gaus mean : 36.0282**

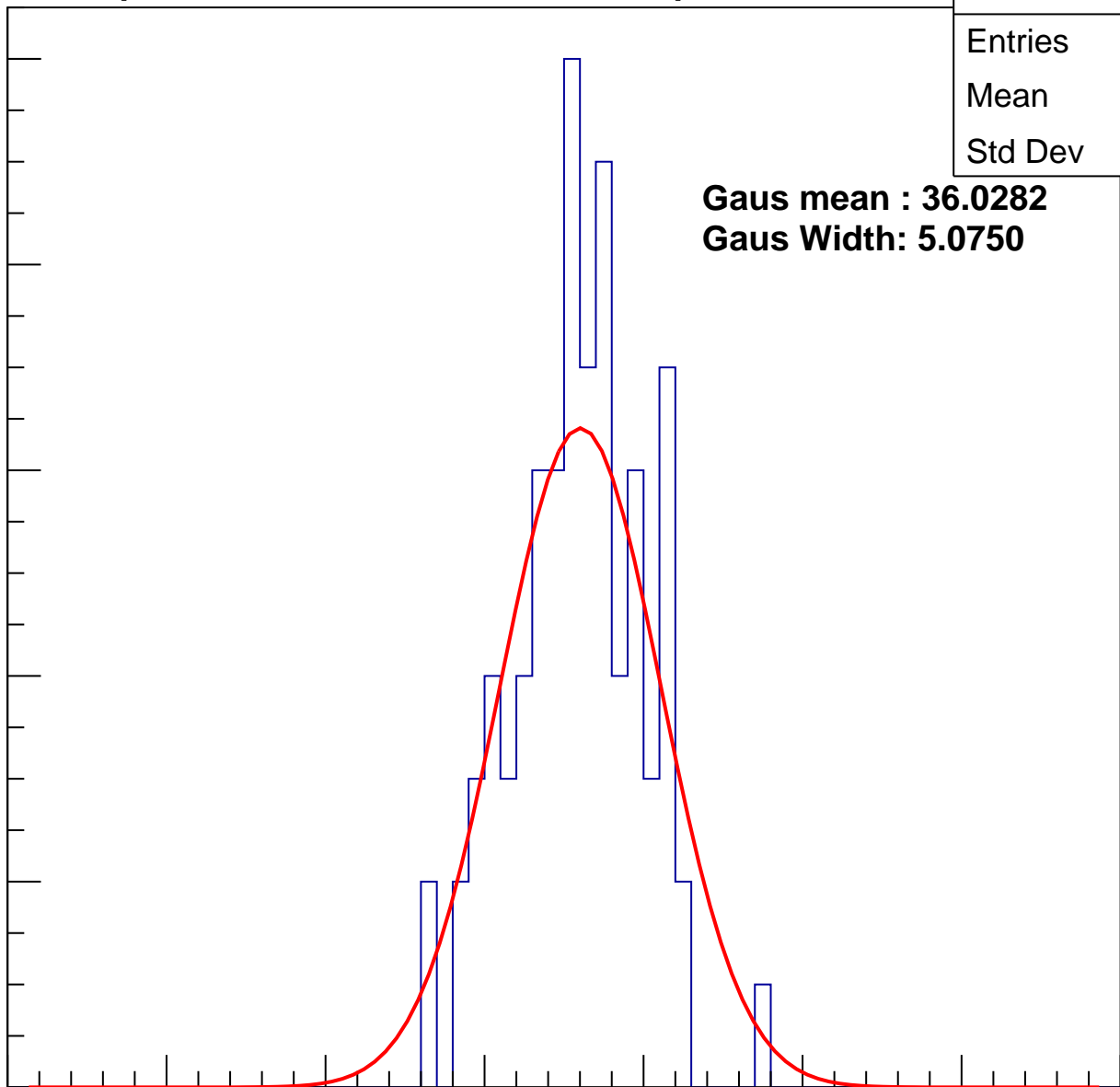
**Gaus Width: 5.0750**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U9-ch22, adc2

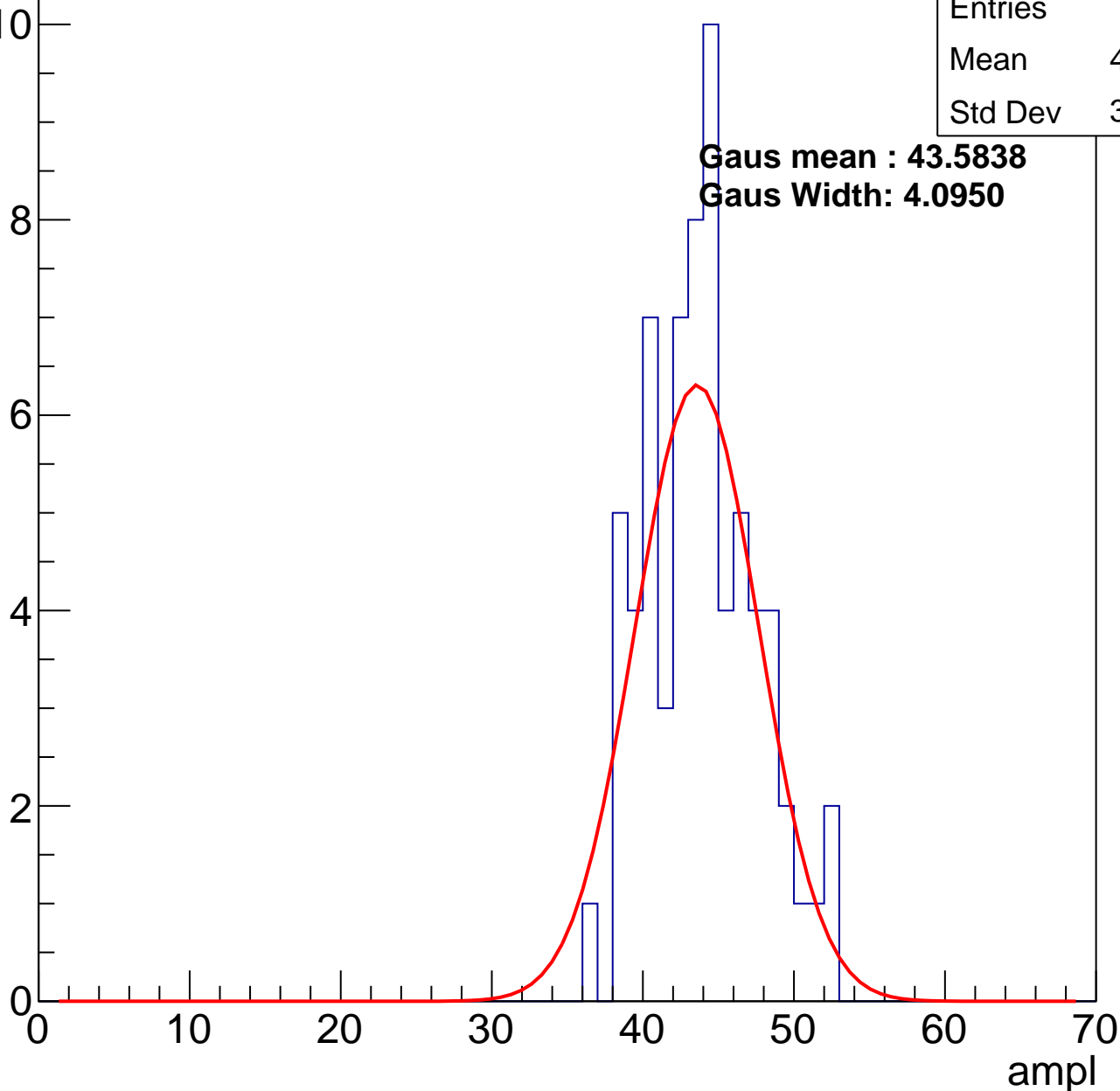
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	68
Mean	43.47
Std Dev	3.612

**Gaus mean : 43.5838**

**Gaus Width: 4.0950**

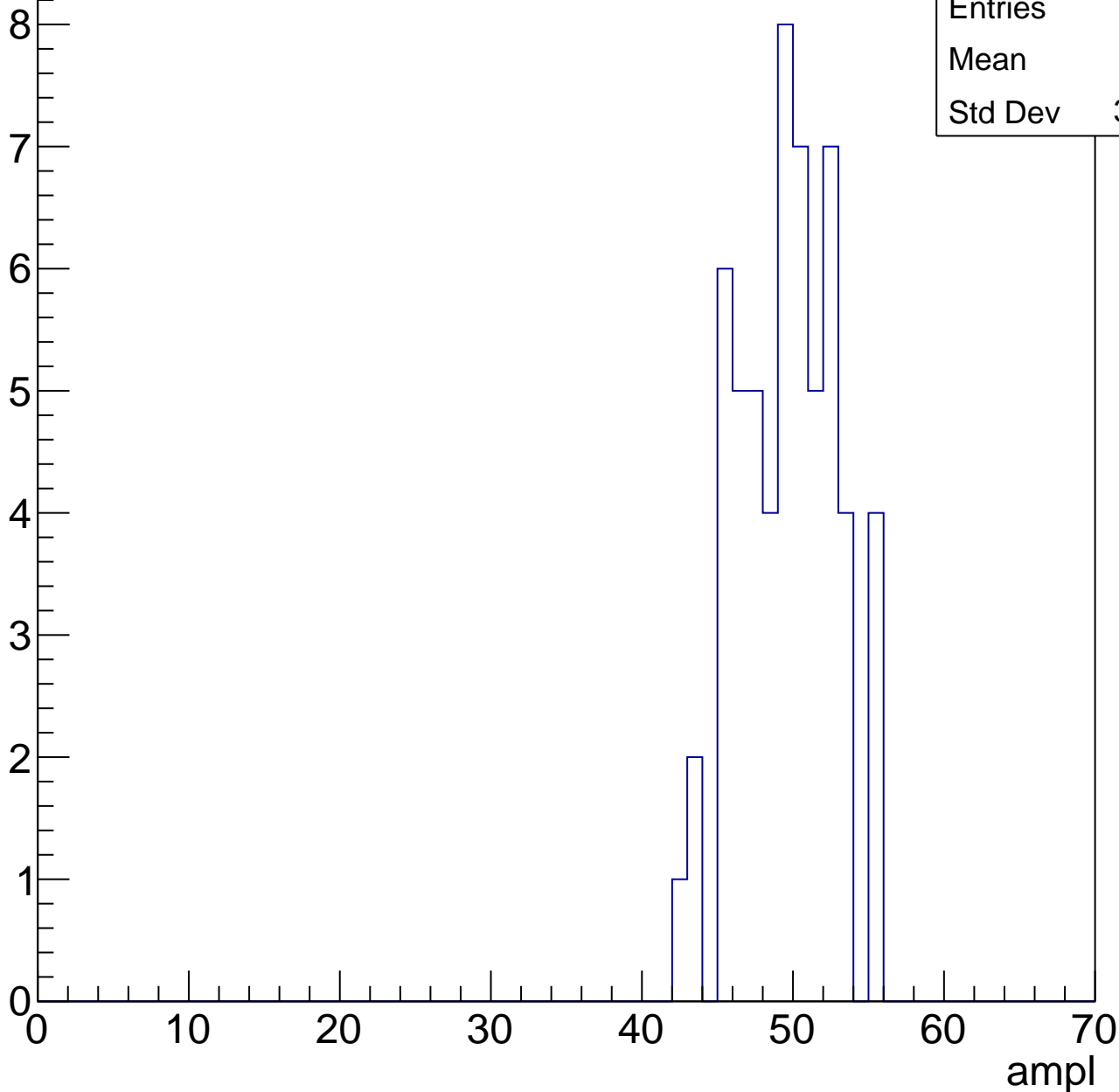


# B1L103S, U9-ch22, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

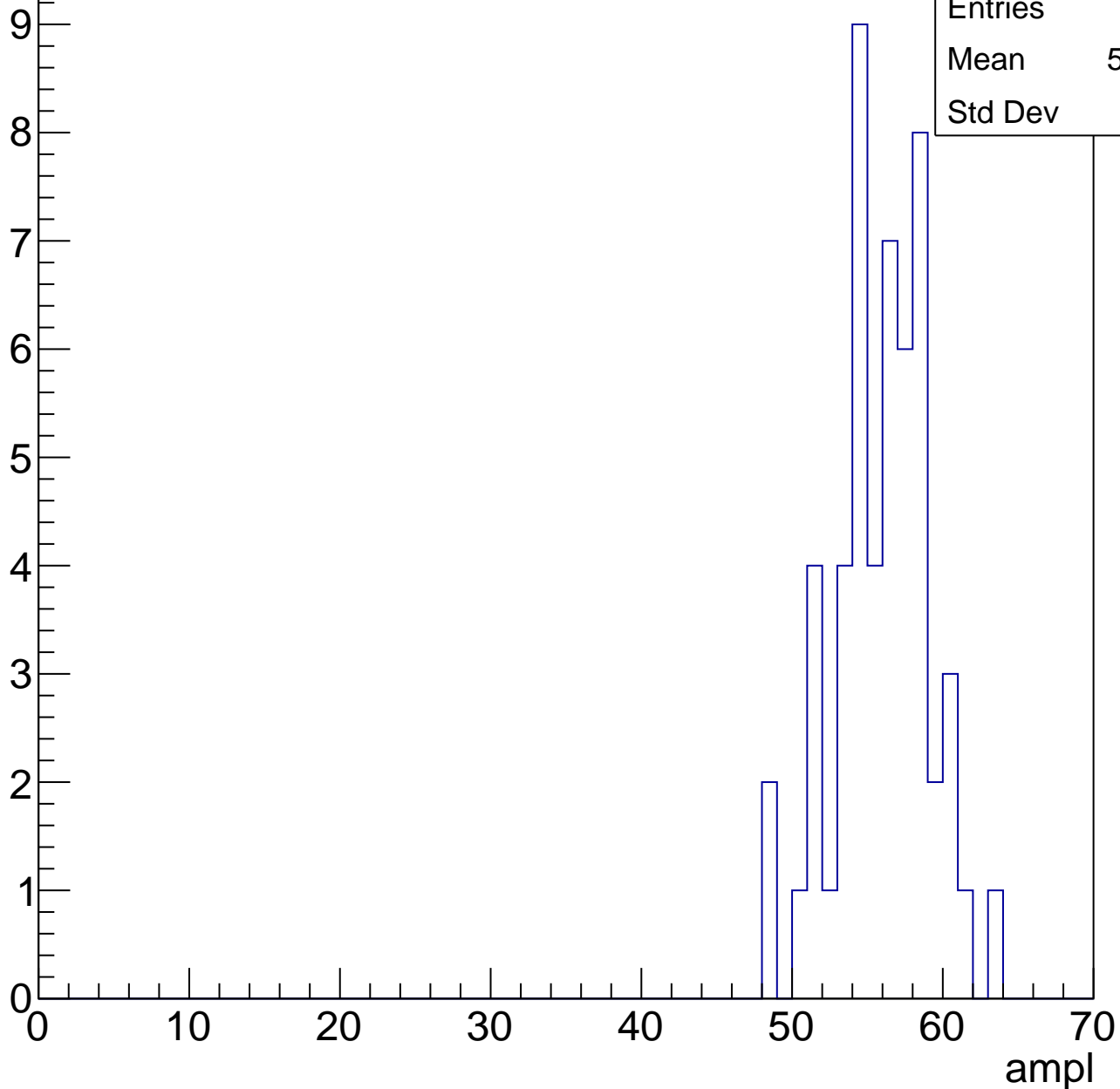
Entries	58
Mean	49.1
Std Dev	3.171



# B1L103S, U9-ch22, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



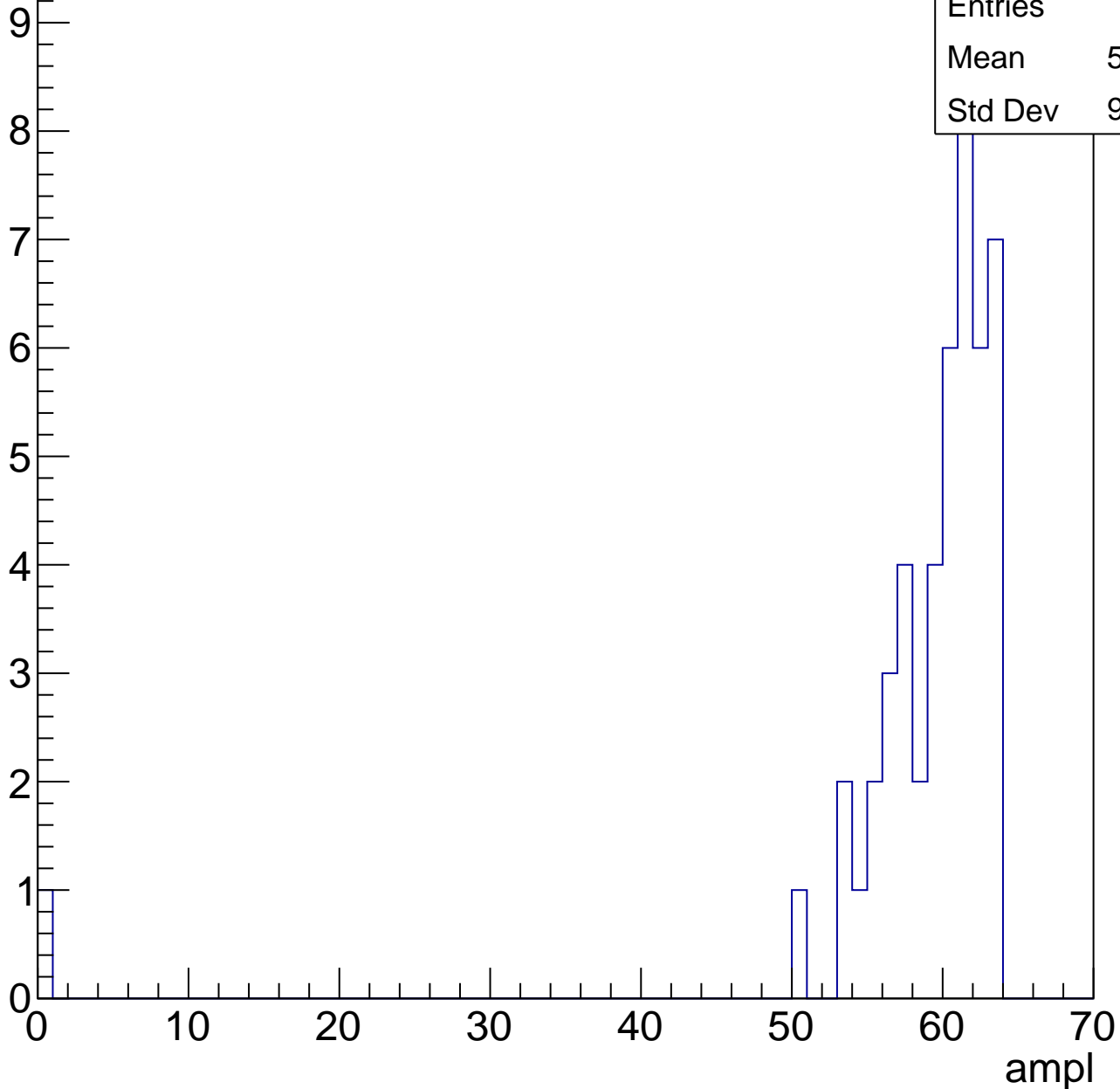
Entries	53
Mean	55.47
Std Dev	3.13

# B1L103S, U9-ch22, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

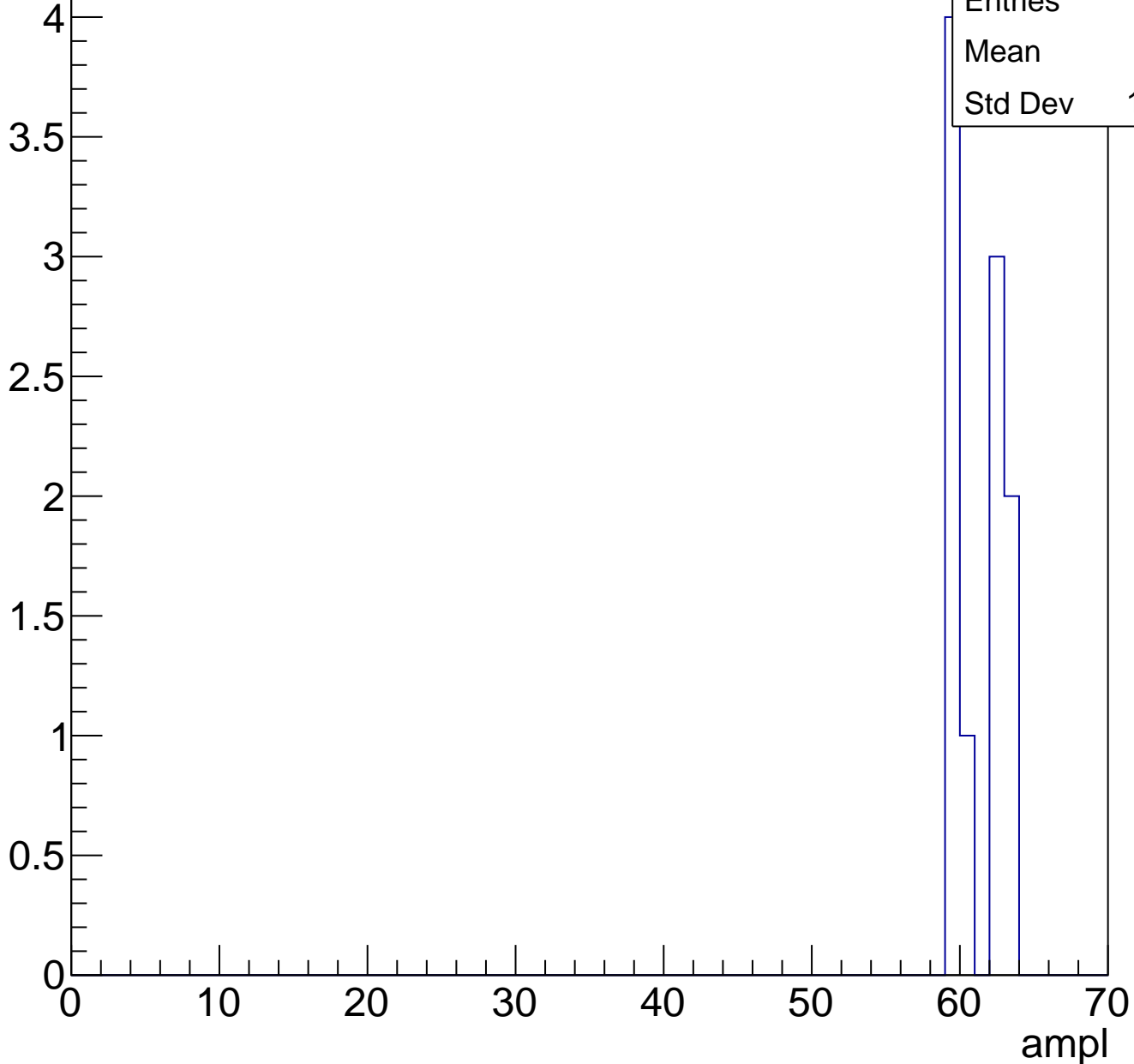
Entries	48
Mean	58.12
Std Dev	9.022



# B1L103S, U9-ch22, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	10
Mean	60.8
Std Dev	1.661



# B1L103S, U9-ch22, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

1

0.8

0.6

0.4

0.2

0

0

10

20

30

40

50

60

70

ampl

Entries

1

Mean

62

Std Dev

0

# B1L103S, U9-ch23, adc0

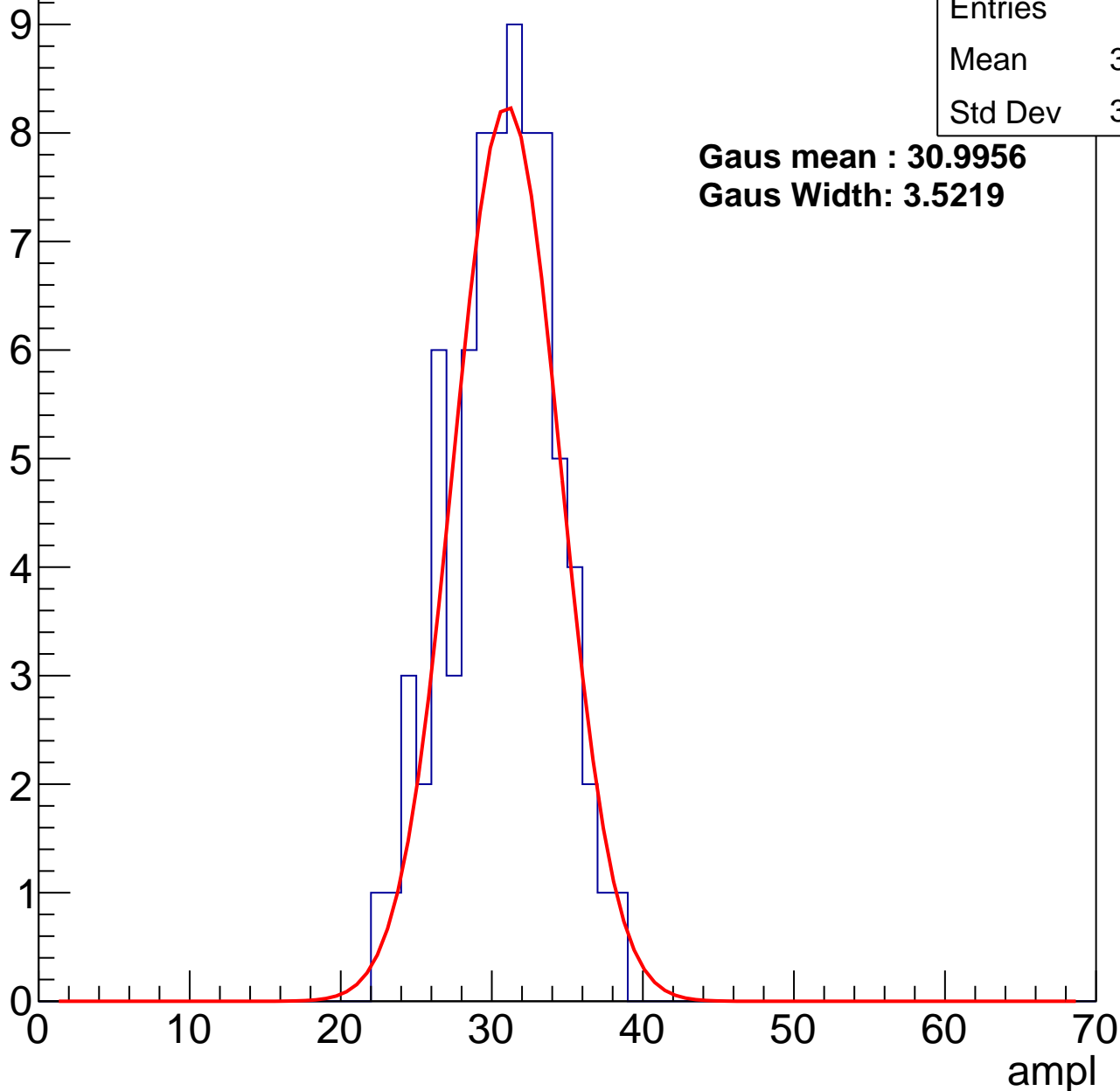
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	76
Mean	30.26
Std Dev	3.439

**Gaus mean : 30.9956**

**Gaus Width: 3.5219**



# B1L103S, U9-ch23, adc1

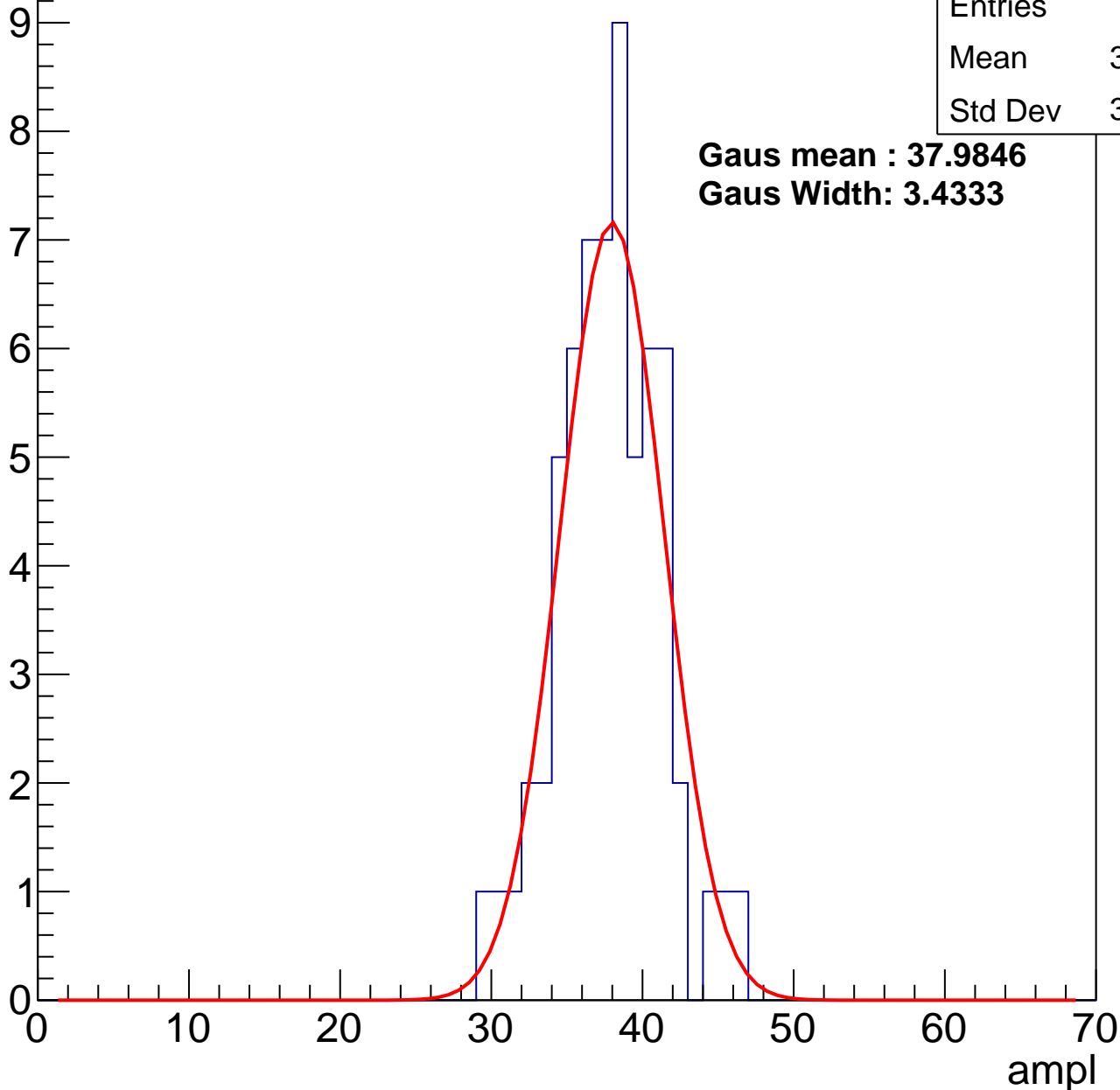
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	37.35
Std Dev	3.386

**Gaus mean : 37.9846**

**Gaus Width: 3.4333**



# B1L103S, U9-ch23, adc2

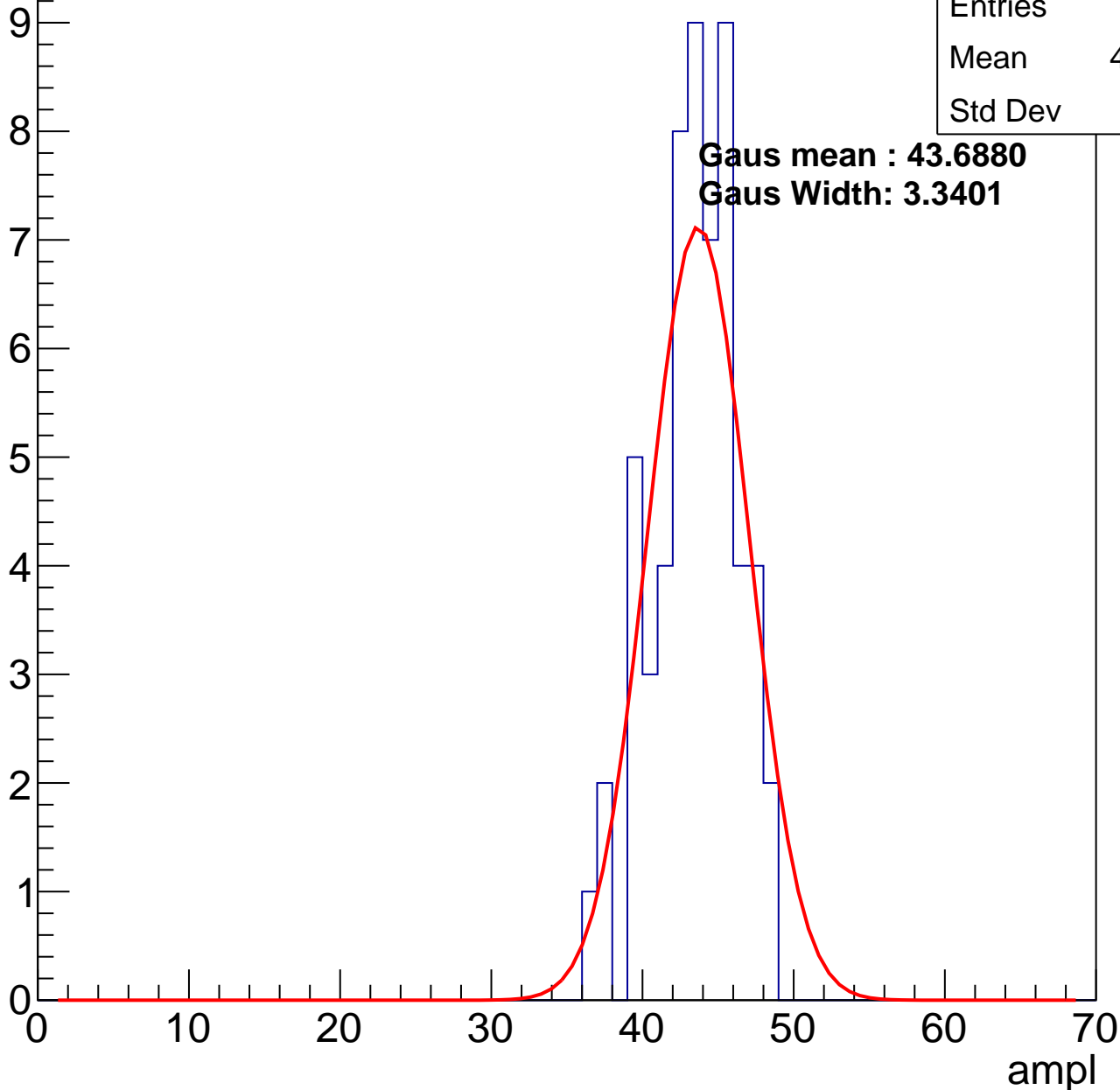
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	58
Mean	42.98
Std Dev	2.77

**Gaus mean : 43.6880**

**Gaus Width: 3.3401**



# B1L103S, U9-ch23, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

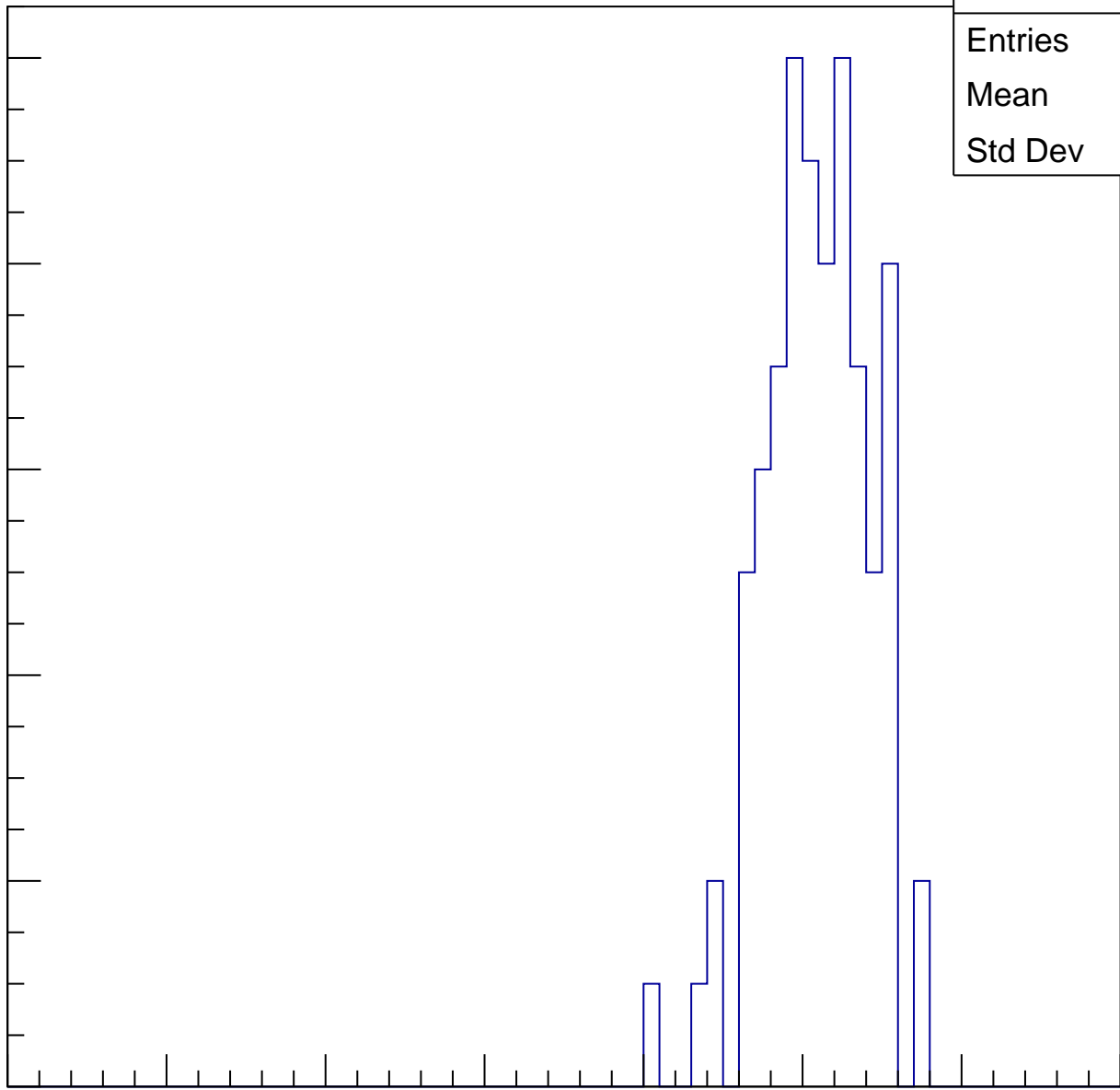
Entries	81
Mean	50.4
Std Dev	3.276

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

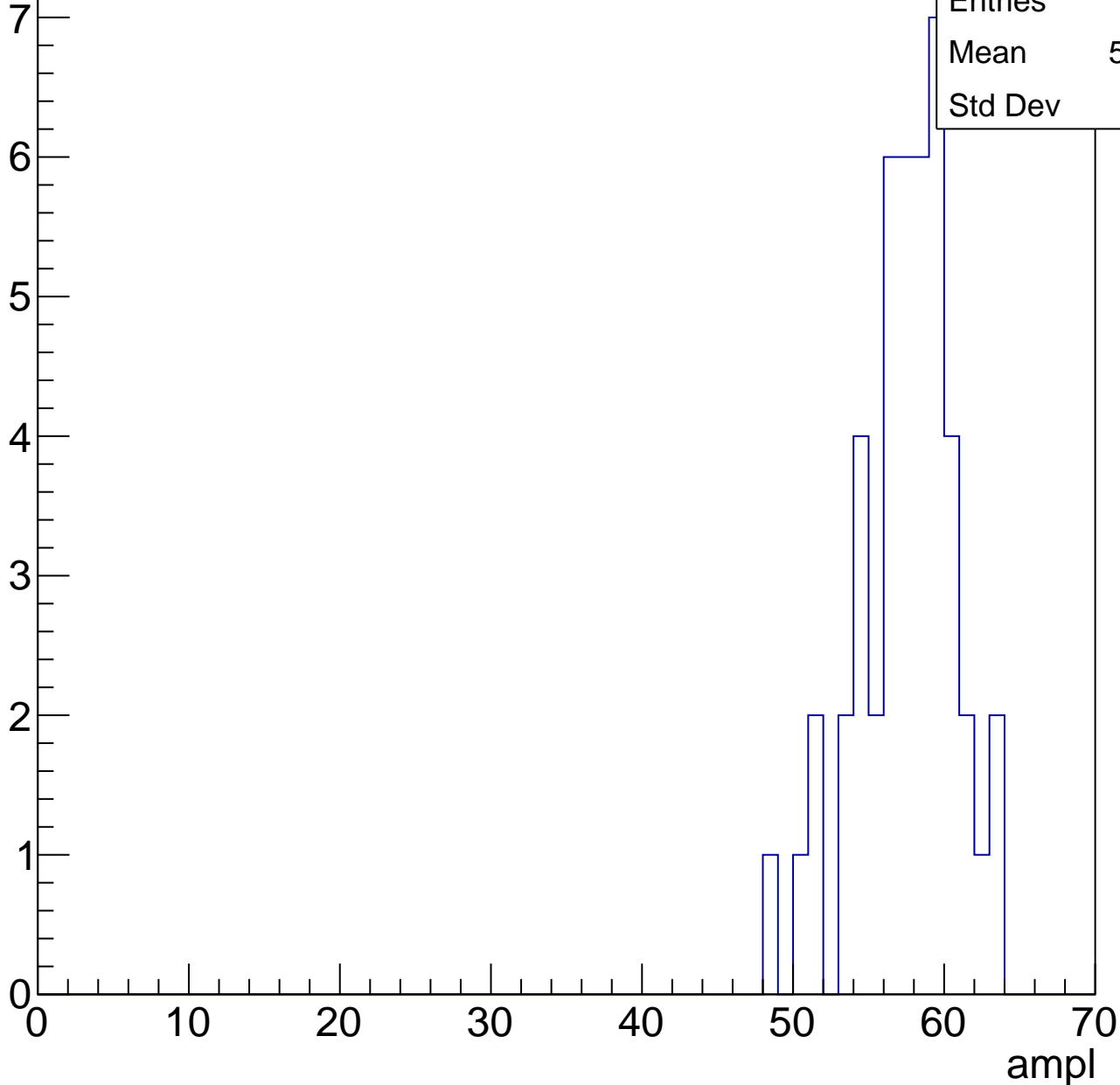


# B1L103S, U9-ch23, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	46
Mean	56.98
Std Dev	3.24

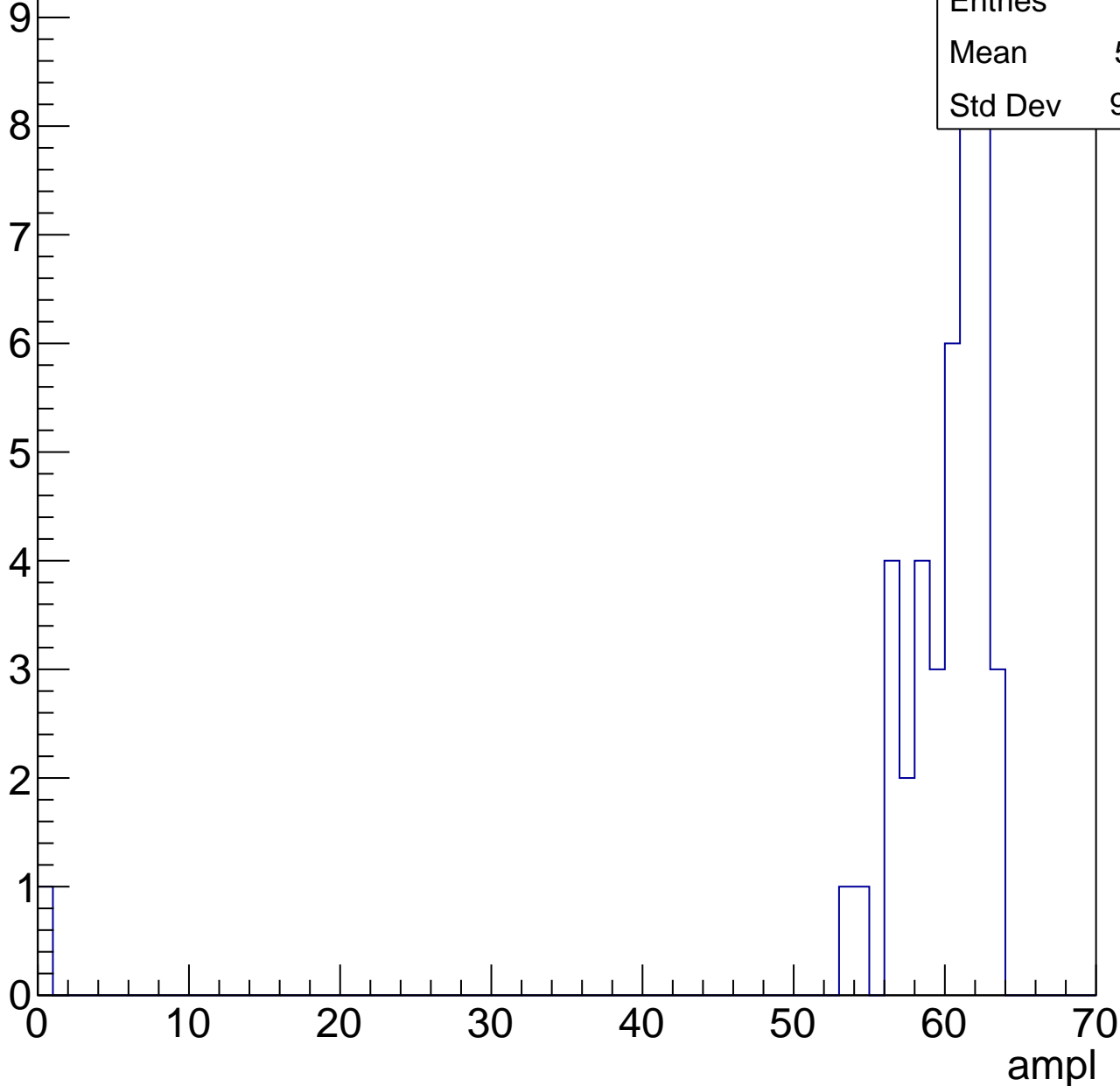


# B1L103S, U9-ch23, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

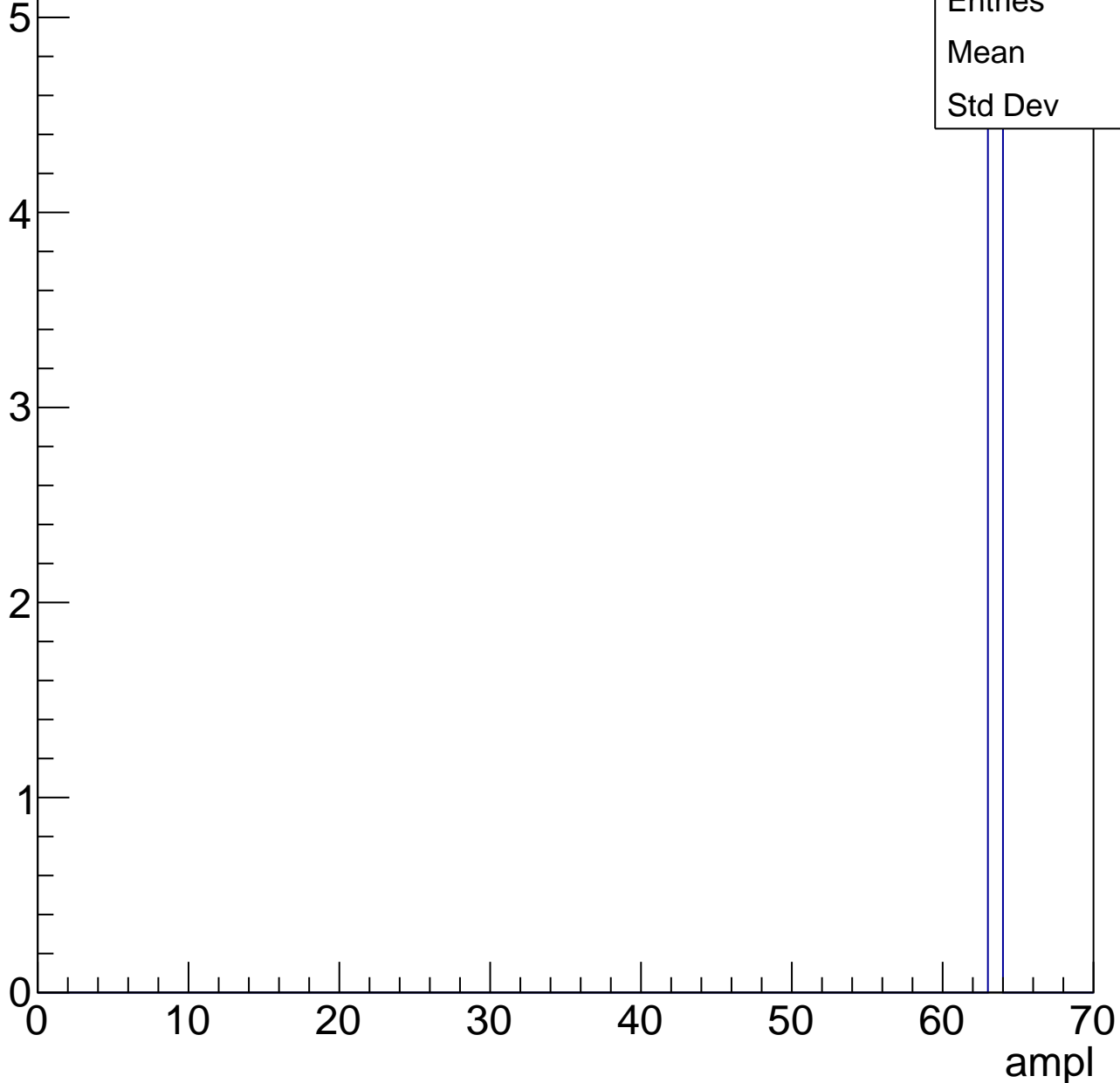
Entries	42
Mean	58.31
Std Dev	9.433



# B1L103S, U9-ch23, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U9-ch23, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U9-ch24, adc0

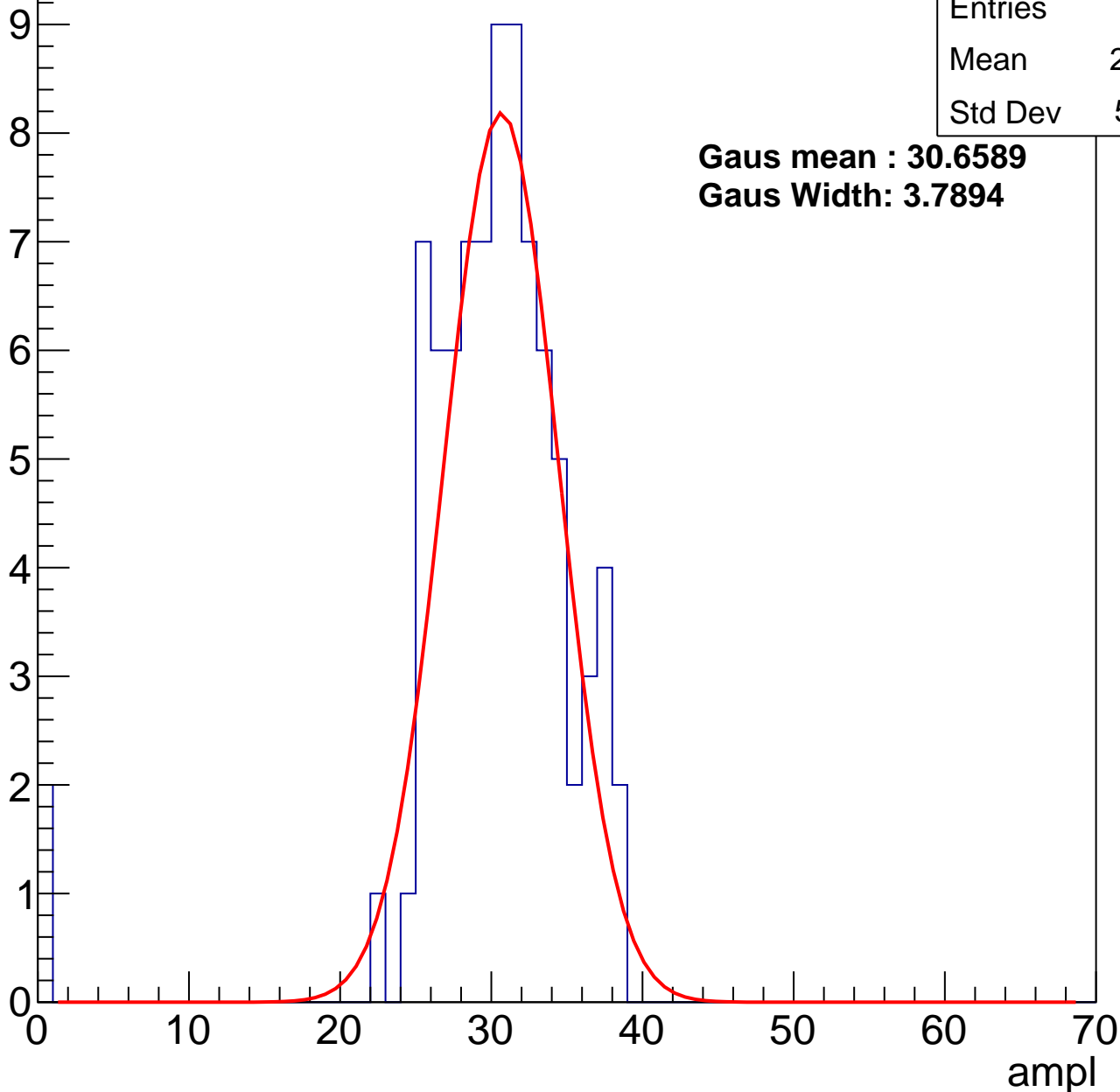
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	84
Mean	29.54
Std Dev	5.871

**Gaus mean : 30.6589**

**Gaus Width: 3.7894**



# B1L103S, U9-ch24, adc1

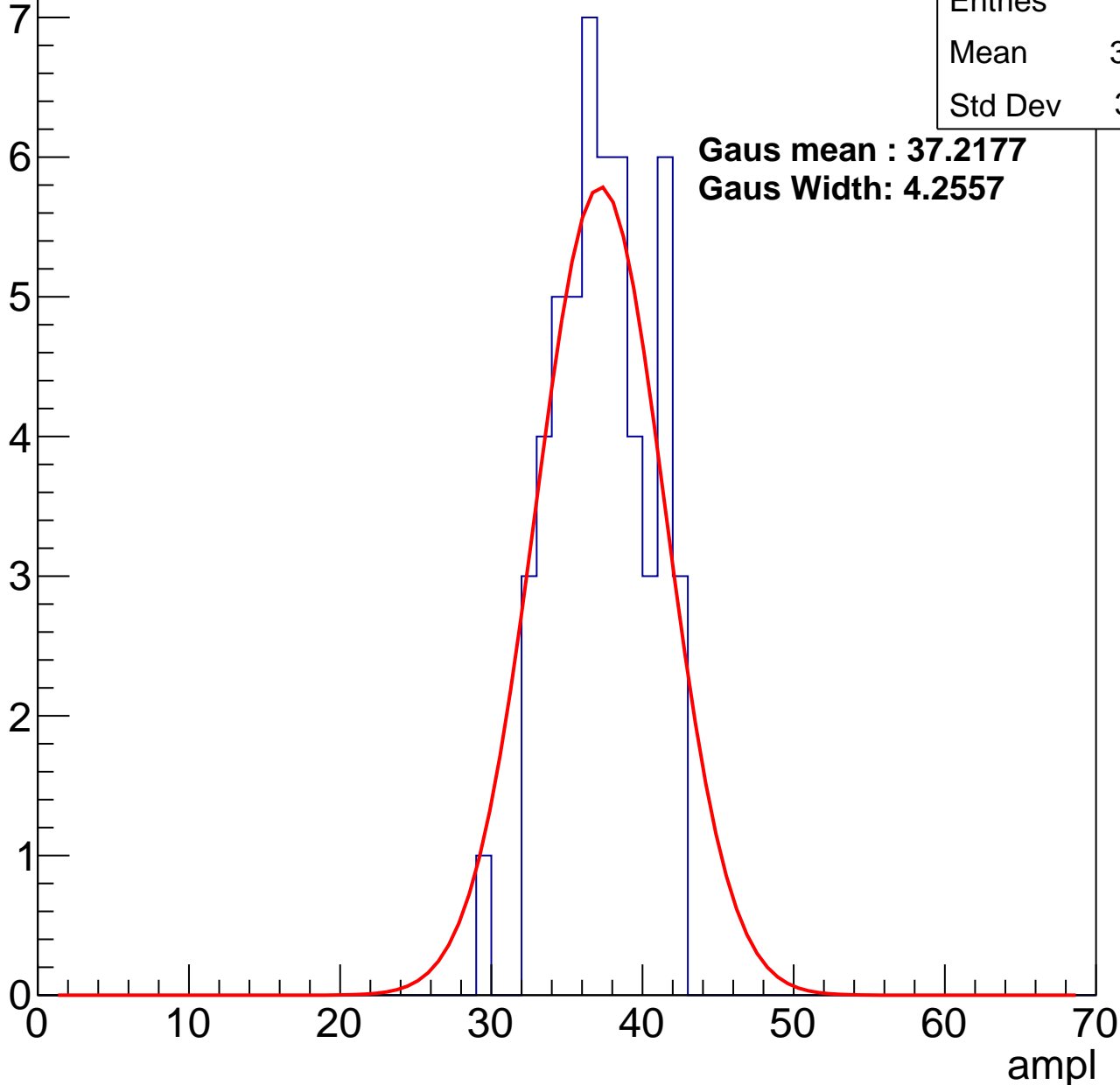
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	53
Mean	36.83
Std Dev	3.051

**Gaus mean : 37.2177**

**Gaus Width: 4.2557**



# B1L103S, U9-ch24, adc2

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	64
Mean	42.89
Std Dev	3.405

**Gaus mean : 43.9718**

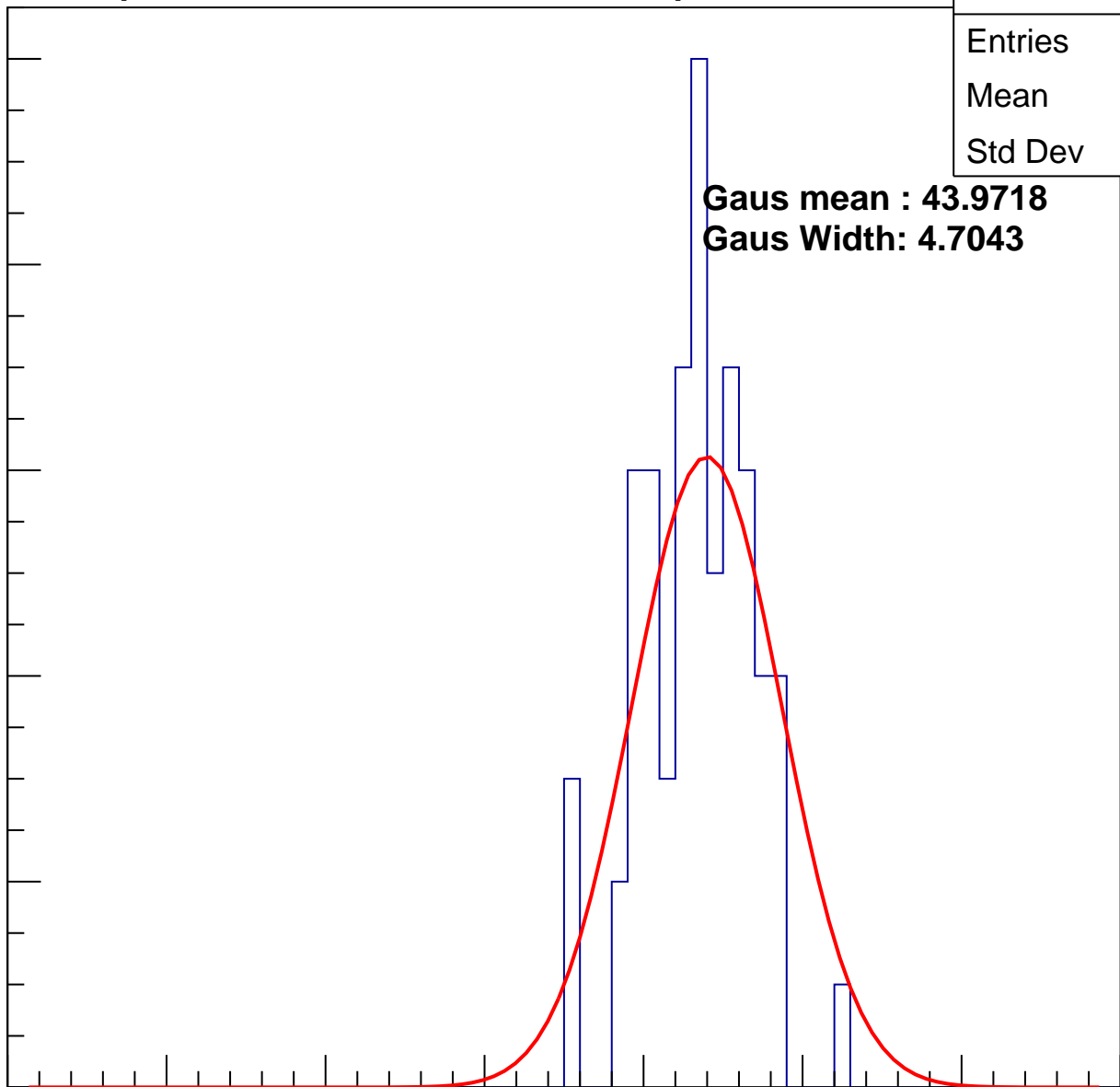
**Gaus Width: 4.7043**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

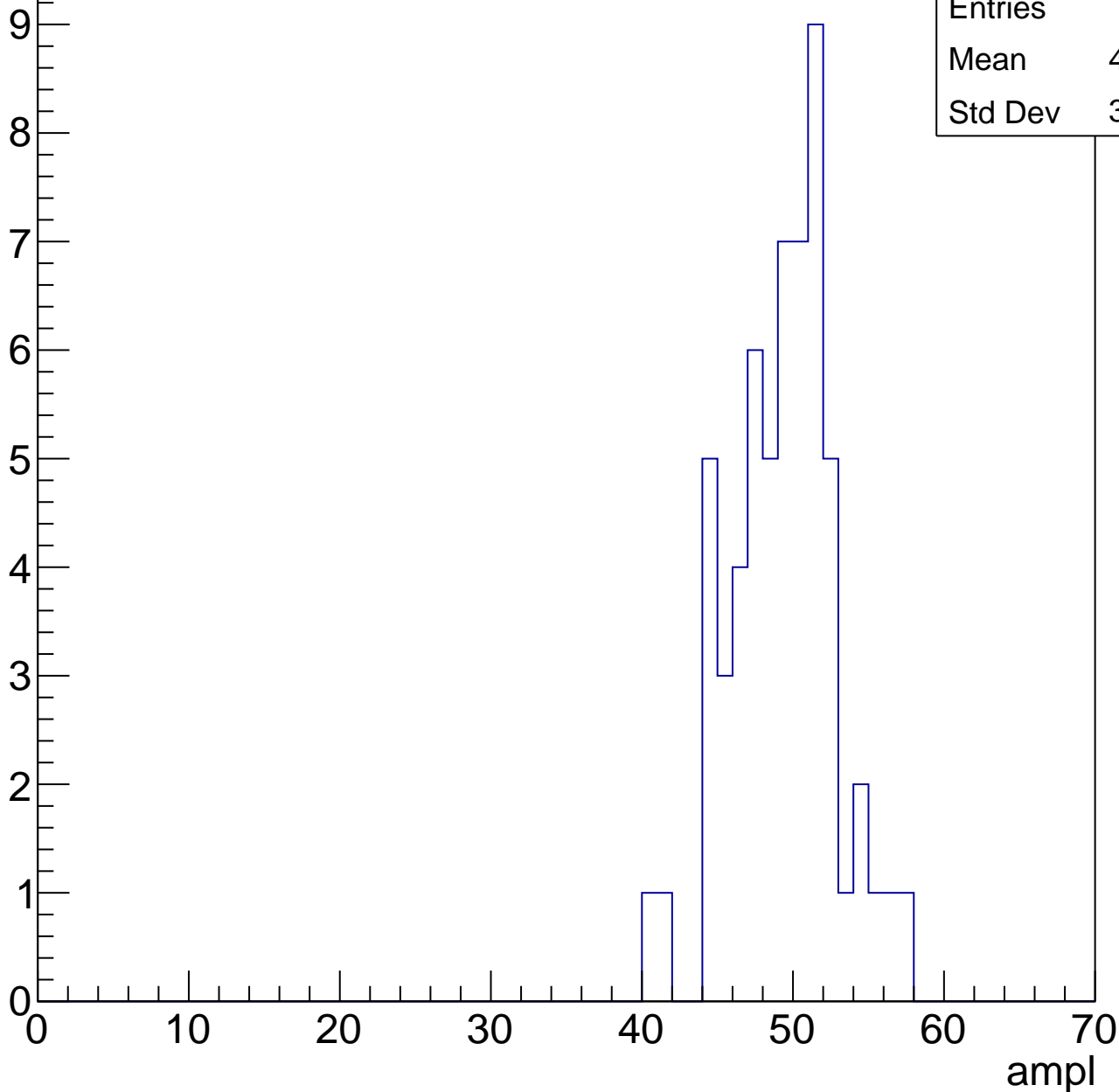


# B1L103S, U9-ch24, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	59
Mean	48.86
Std Dev	3.407

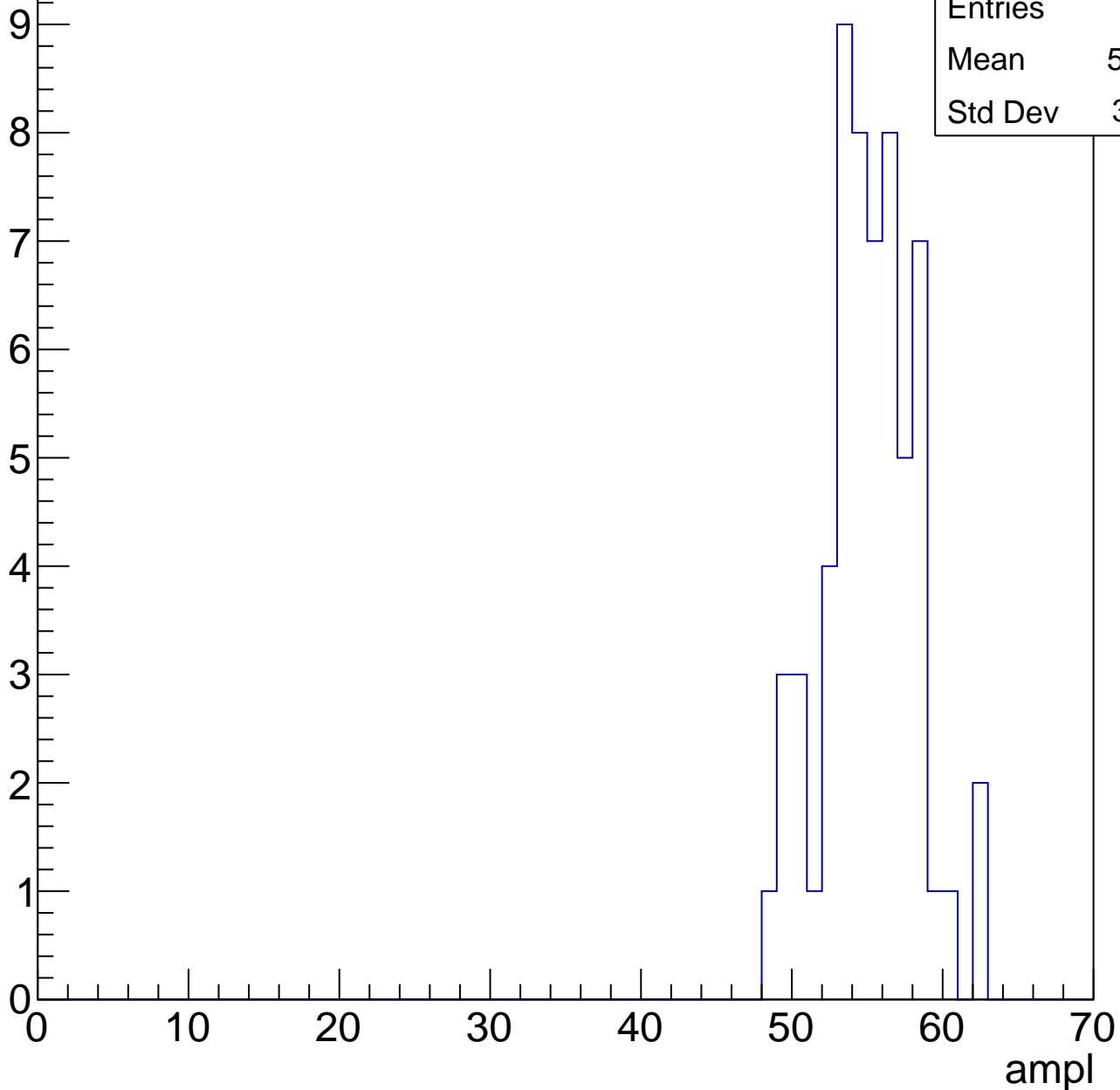


# B1L103S, U9-ch24, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

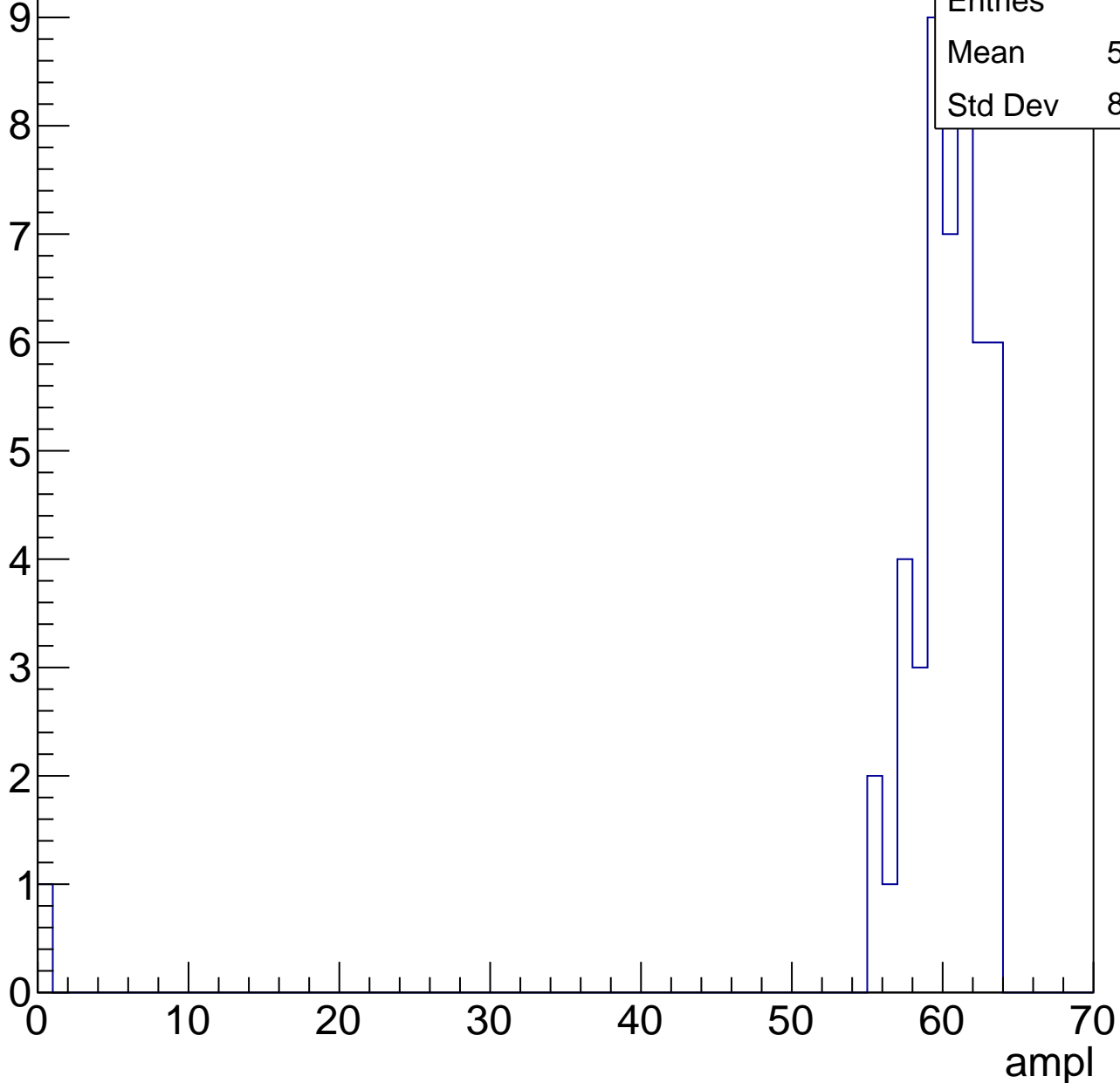
Entries	60
Mean	54.67
Std Dev	3.031



# B1L103S, U9-ch24, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U9-ch24, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

3

2.5

2

1.5

1

0.5

0

0

10

20

30

40

50

60

70

ampl

Entries

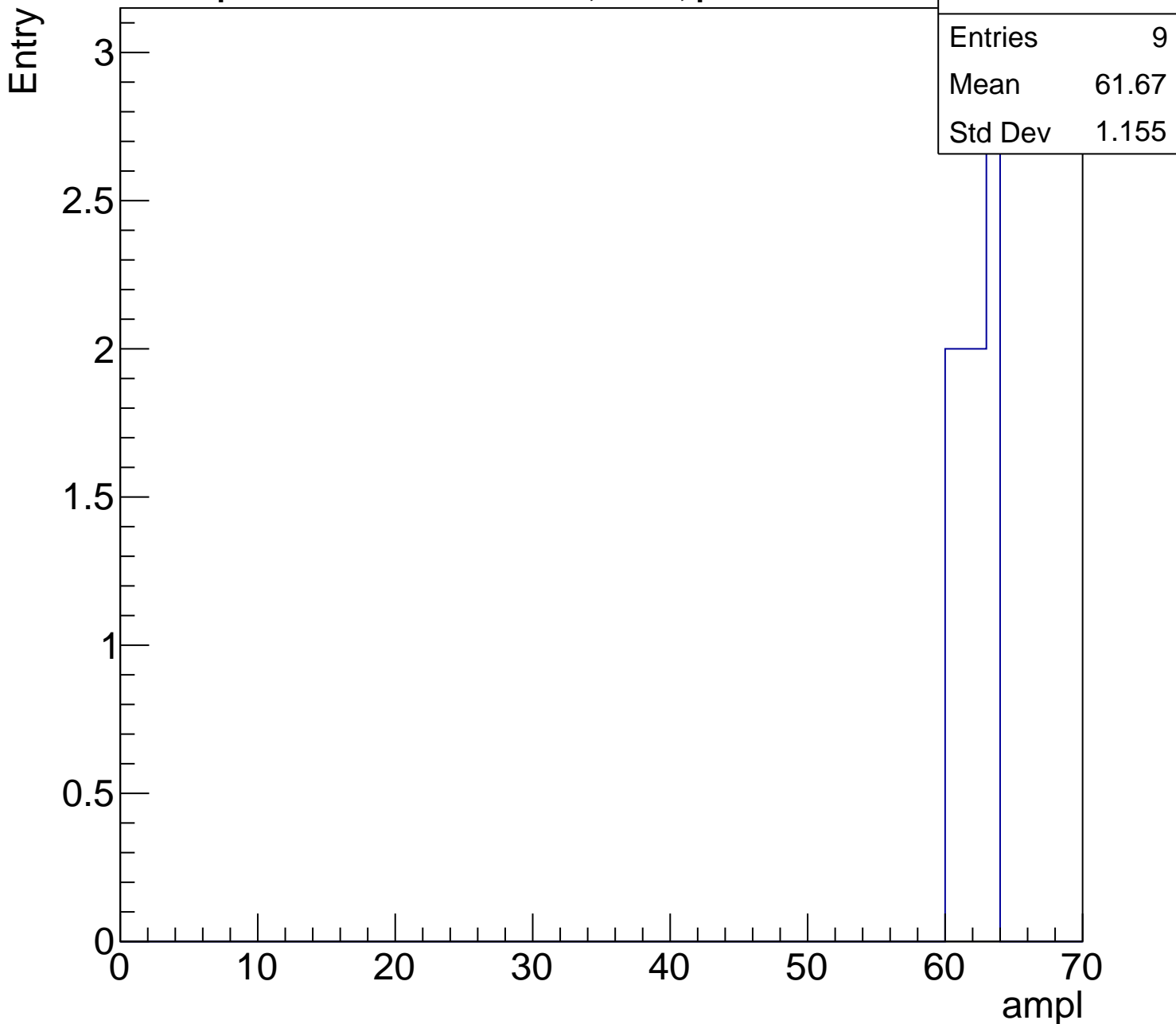
9

Mean

61.67

Std Dev

1.155





# B1L103S, U9-ch24, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U9-ch25, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	77
Mean	29.61
Std Dev	5.981

**Gaus mean : 29.7769**

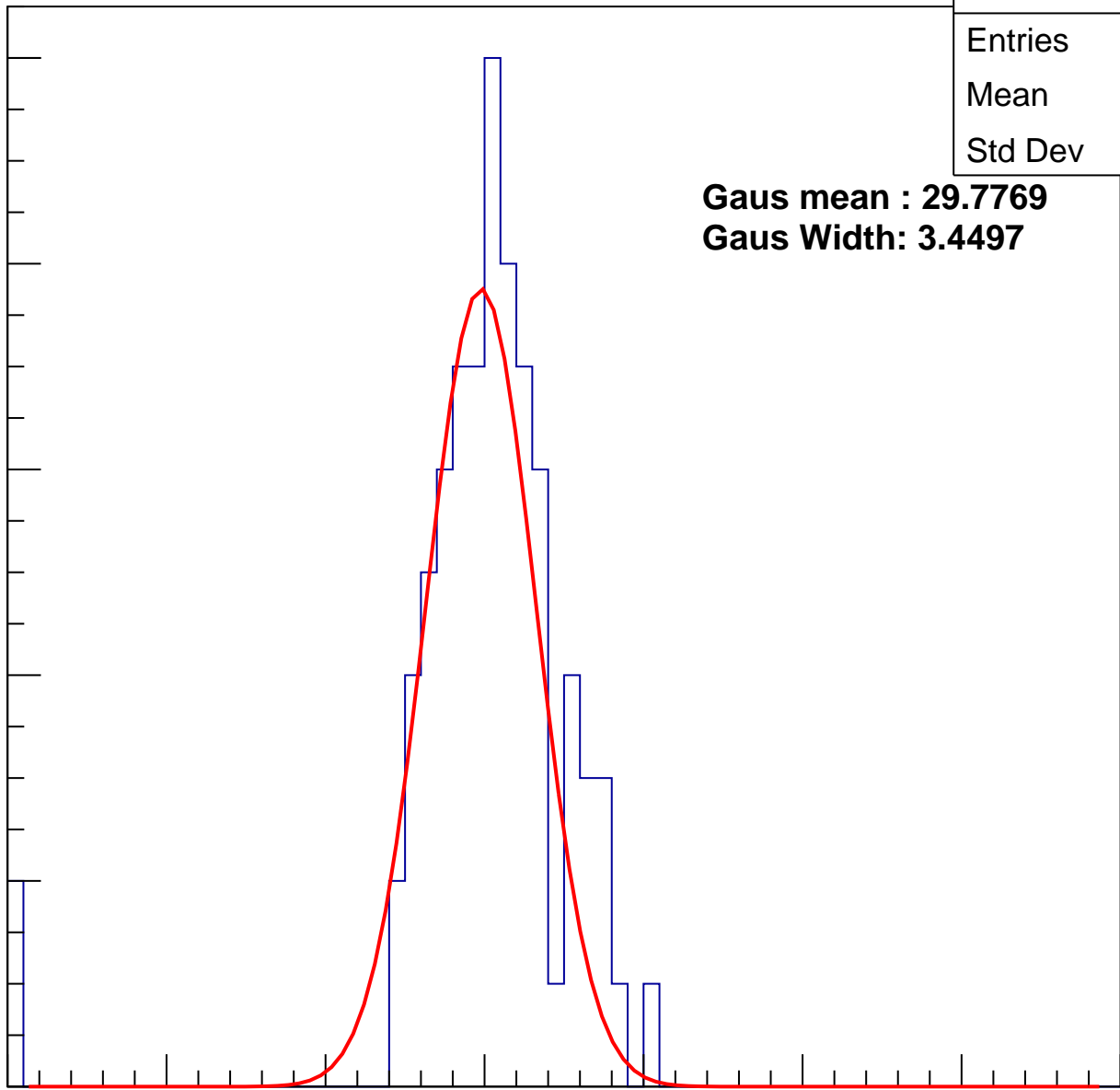
**Gaus Width: 3.4497**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U9-ch25, adc1

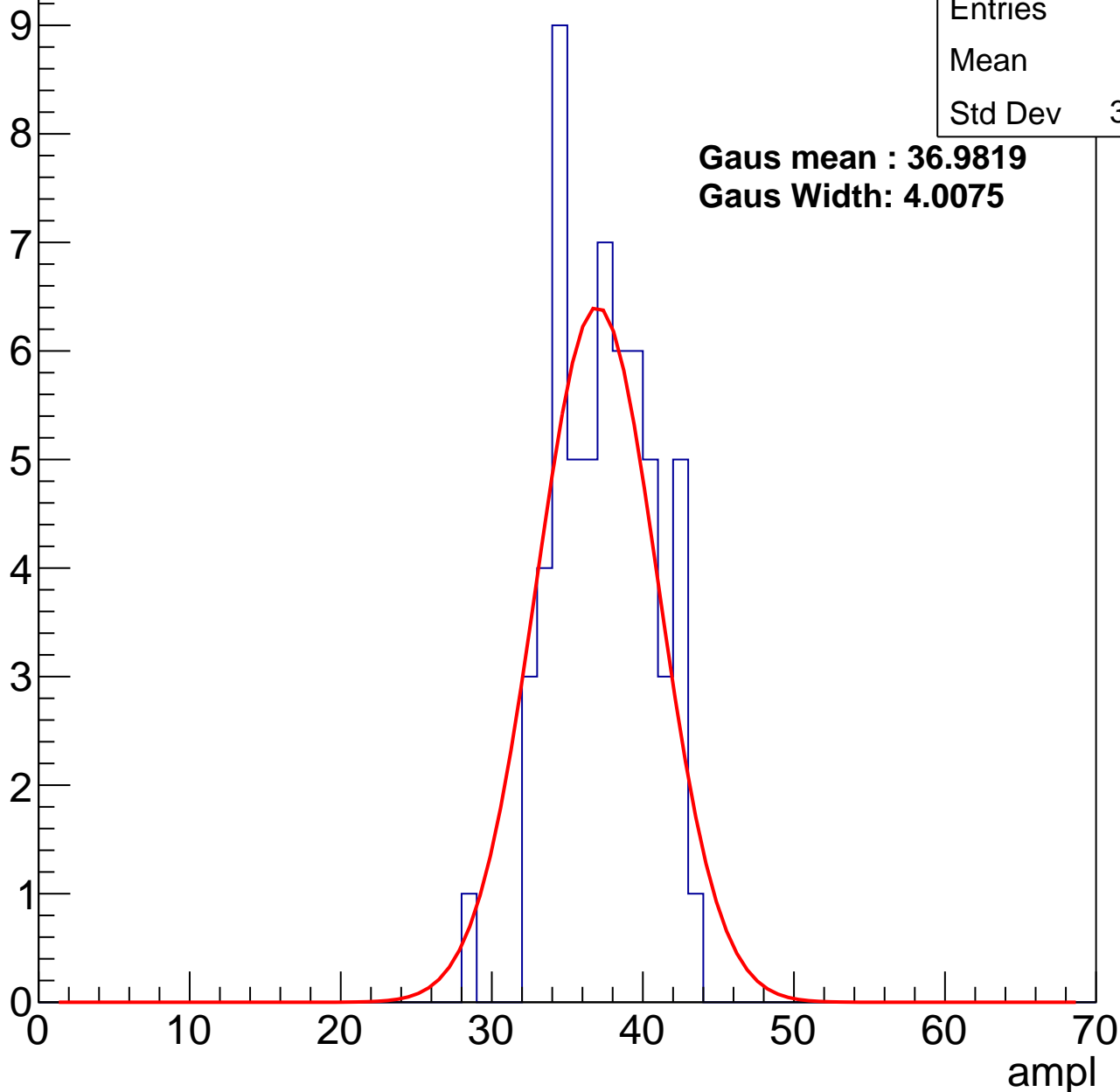
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	60
Mean	36.9
Std Dev	3.187

**Gaus mean : 36.9819**

**Gaus Width: 4.0075**



# B1L103S, U9-ch25, adc2

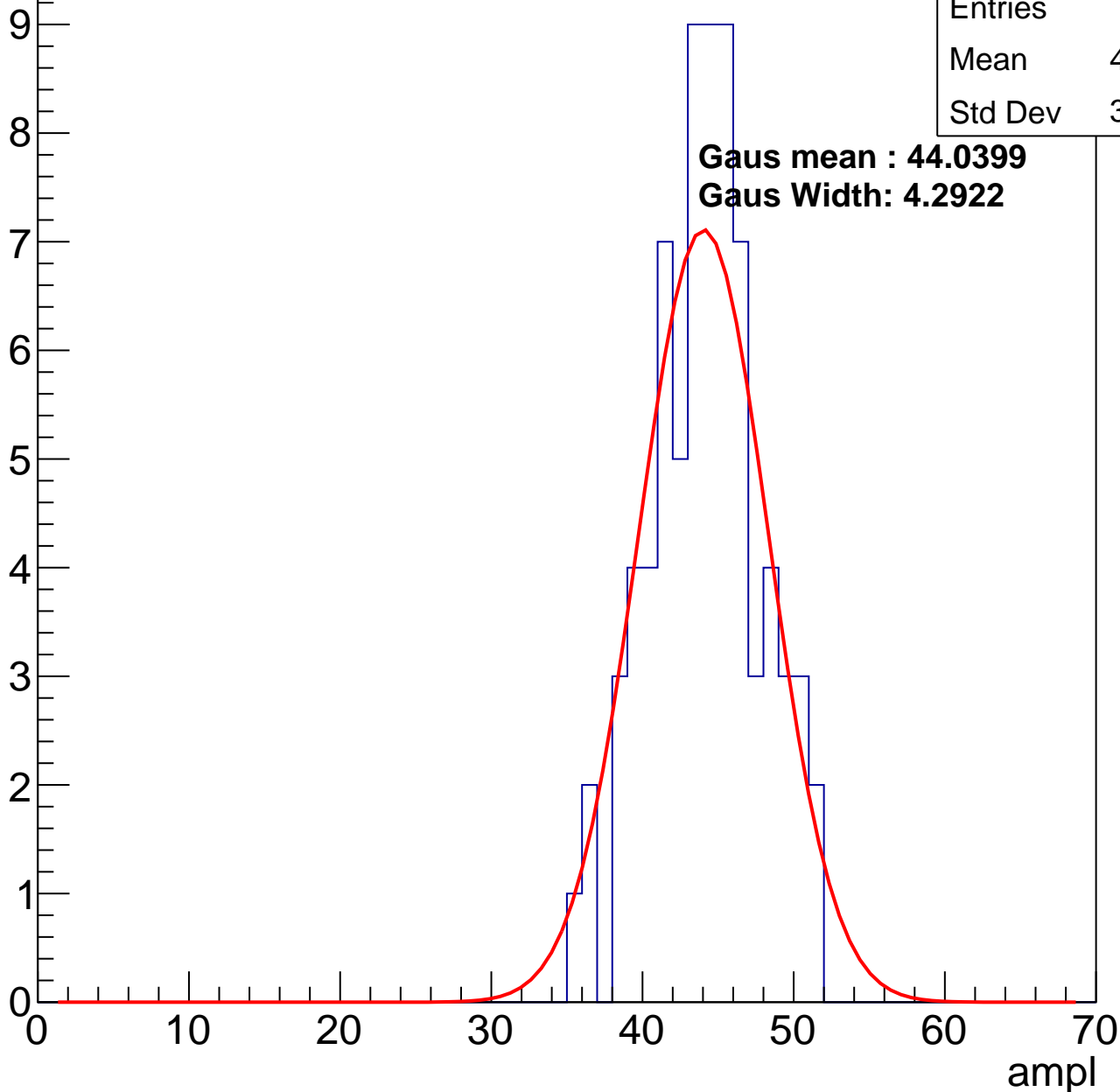
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	75
Mean	43.68
Std Dev	3.604

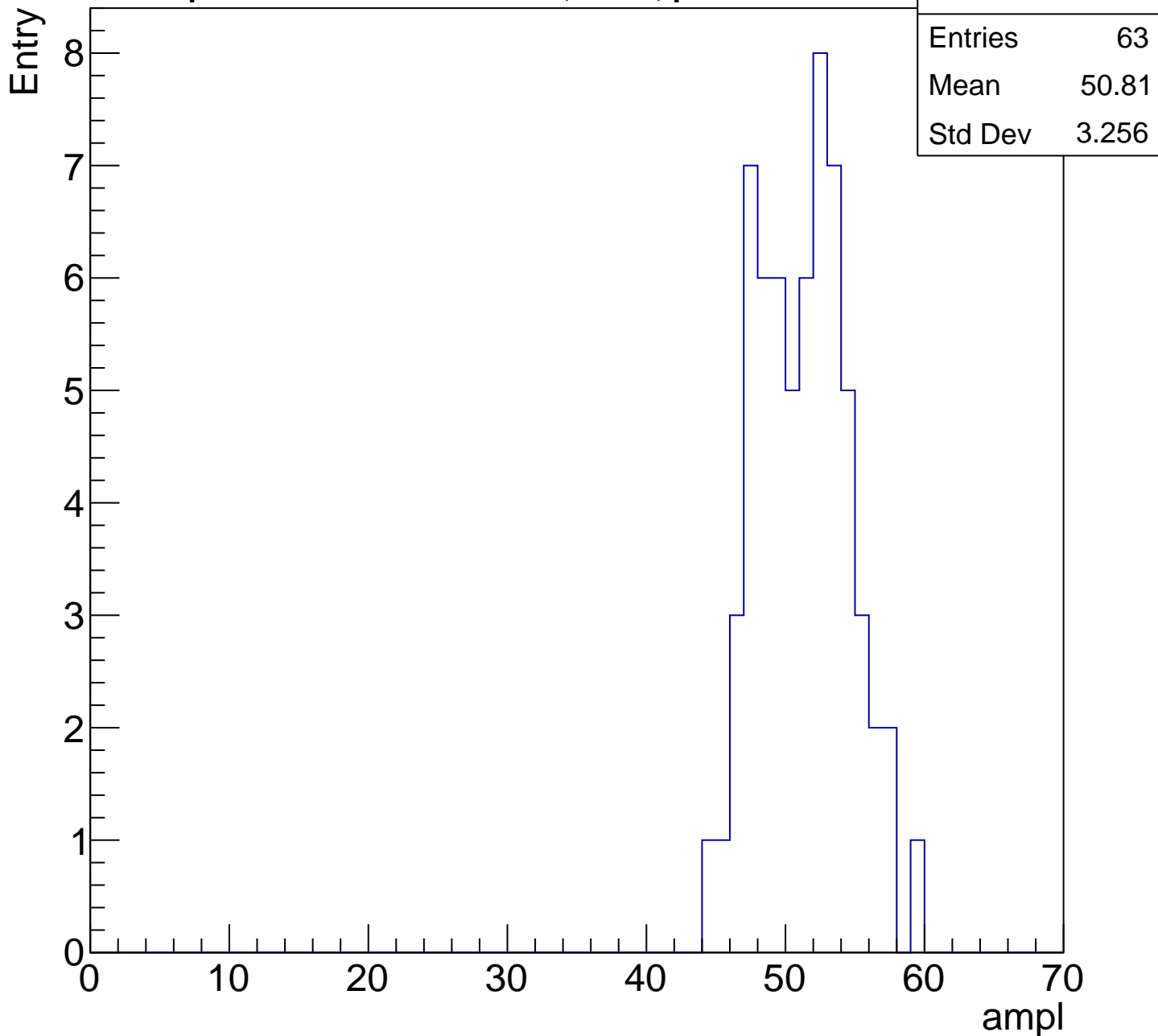
**Gaus mean : 44.0399**

**Gaus Width: 4.2922**



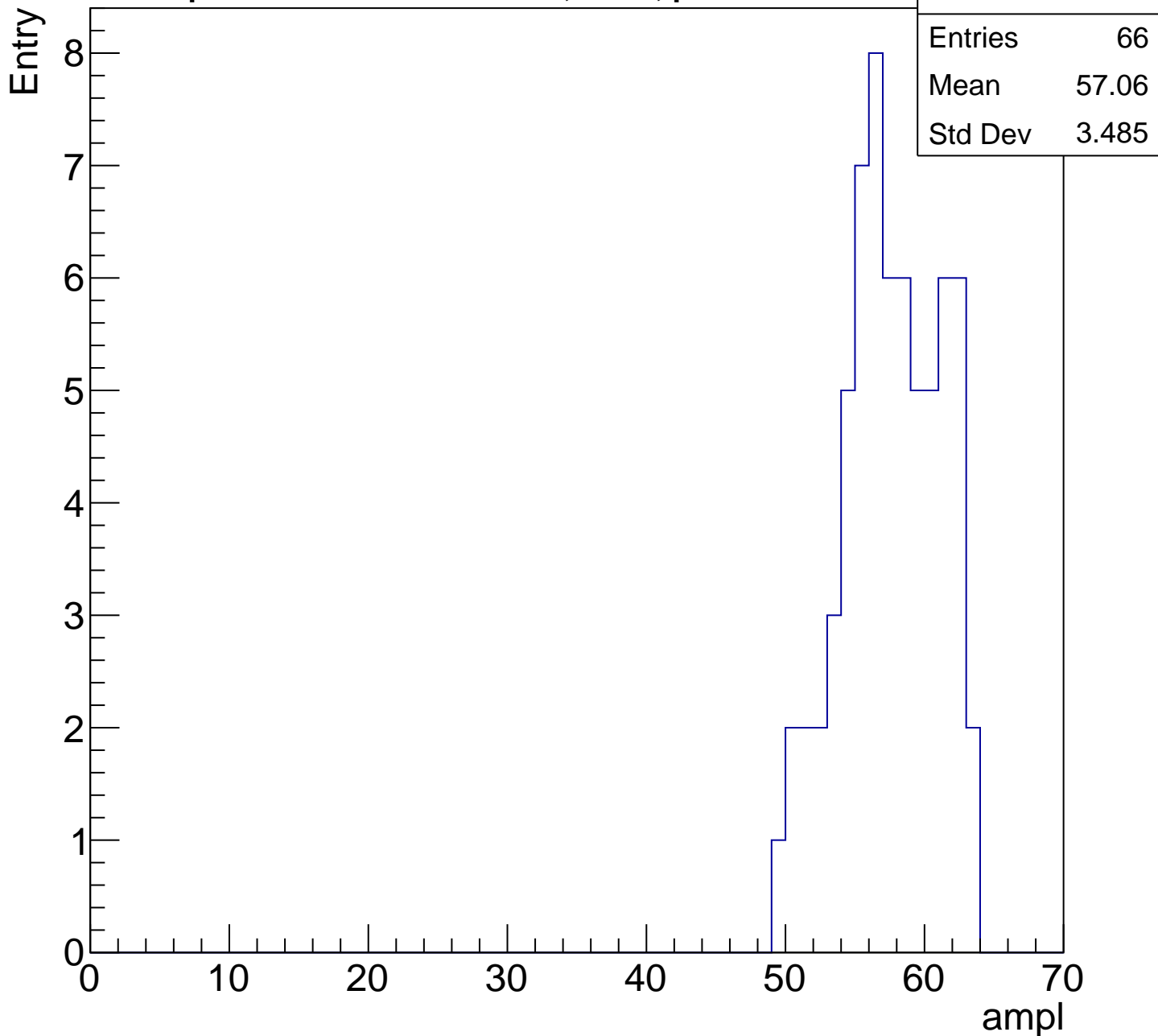
# B1L103S, U9-ch25, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U9-ch25, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

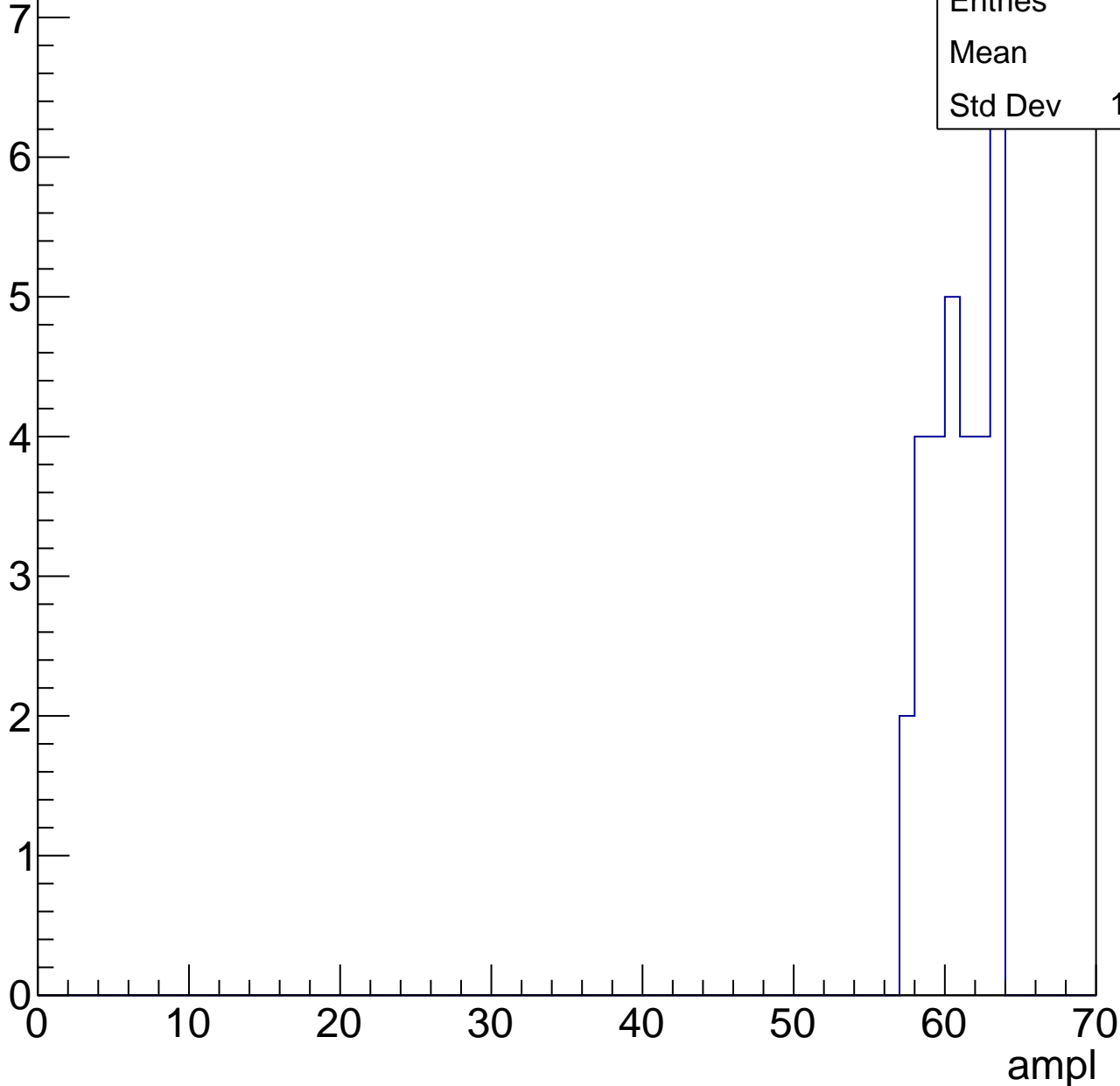


# B1L103S, U9-ch25, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	30
Mean	60.5
Std Dev	1.945



# B1L103S, U9-ch25, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U9-ch25, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U9-ch26, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	106
Mean	28.78
Std Dev	5.632

**Gaus mean : 30.3084**

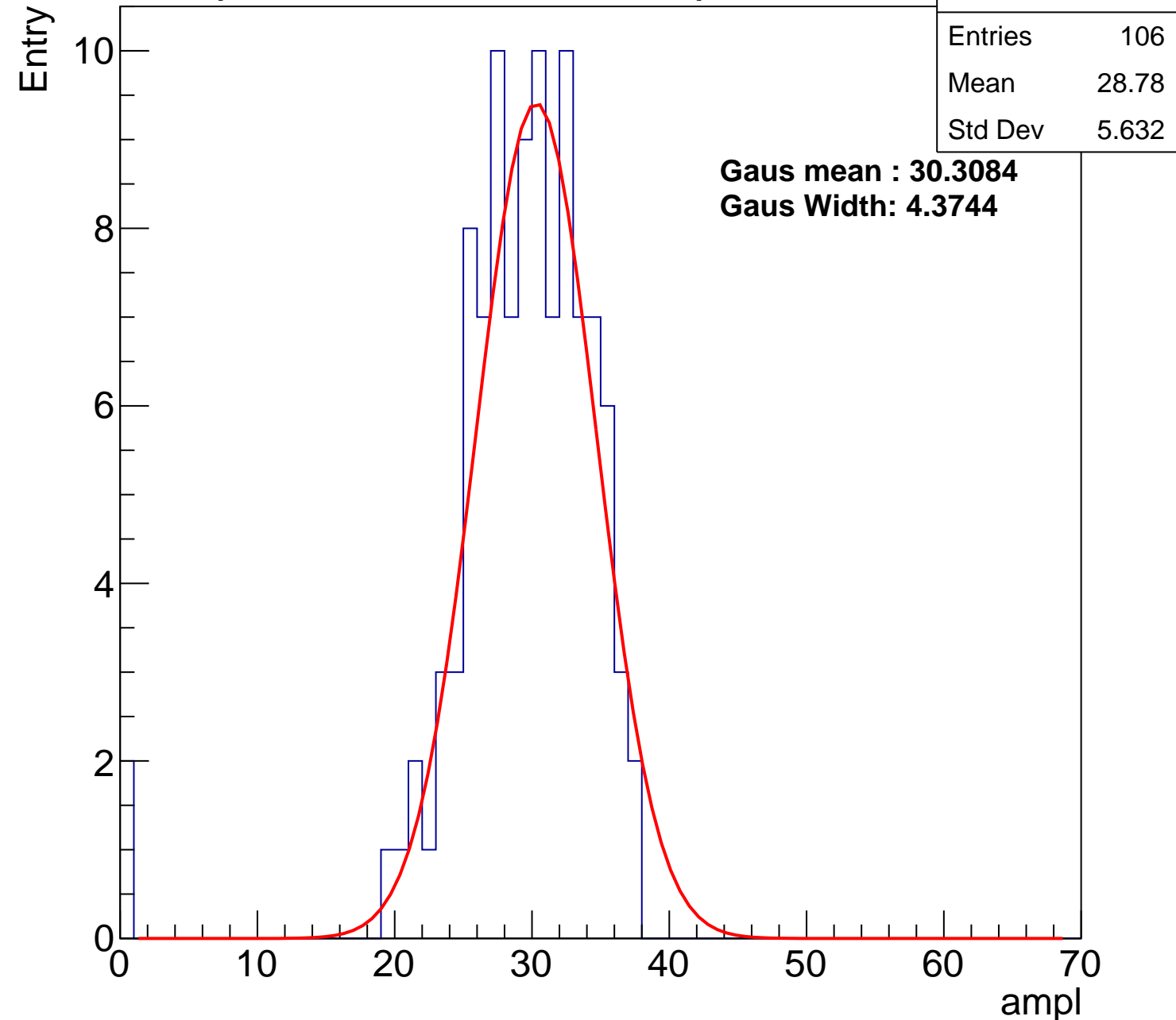
**Gaus Width: 4.3744**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U9-ch26, adc1

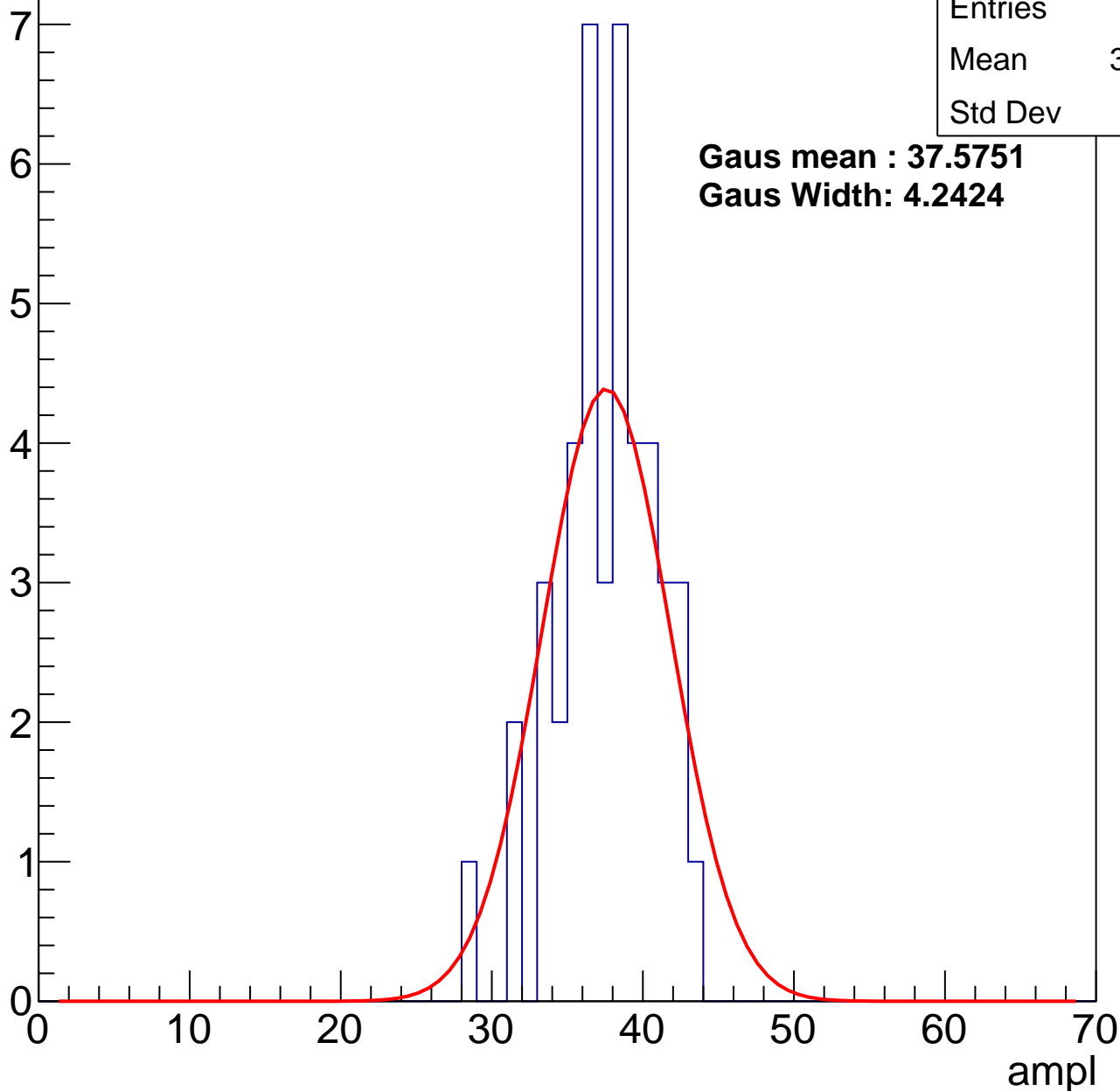
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	44
Mean	37.14
Std Dev	3.23

**Gaus mean : 37.5751**

**Gaus Width: 4.2424**



# B1L103S, U9-ch26, adc2

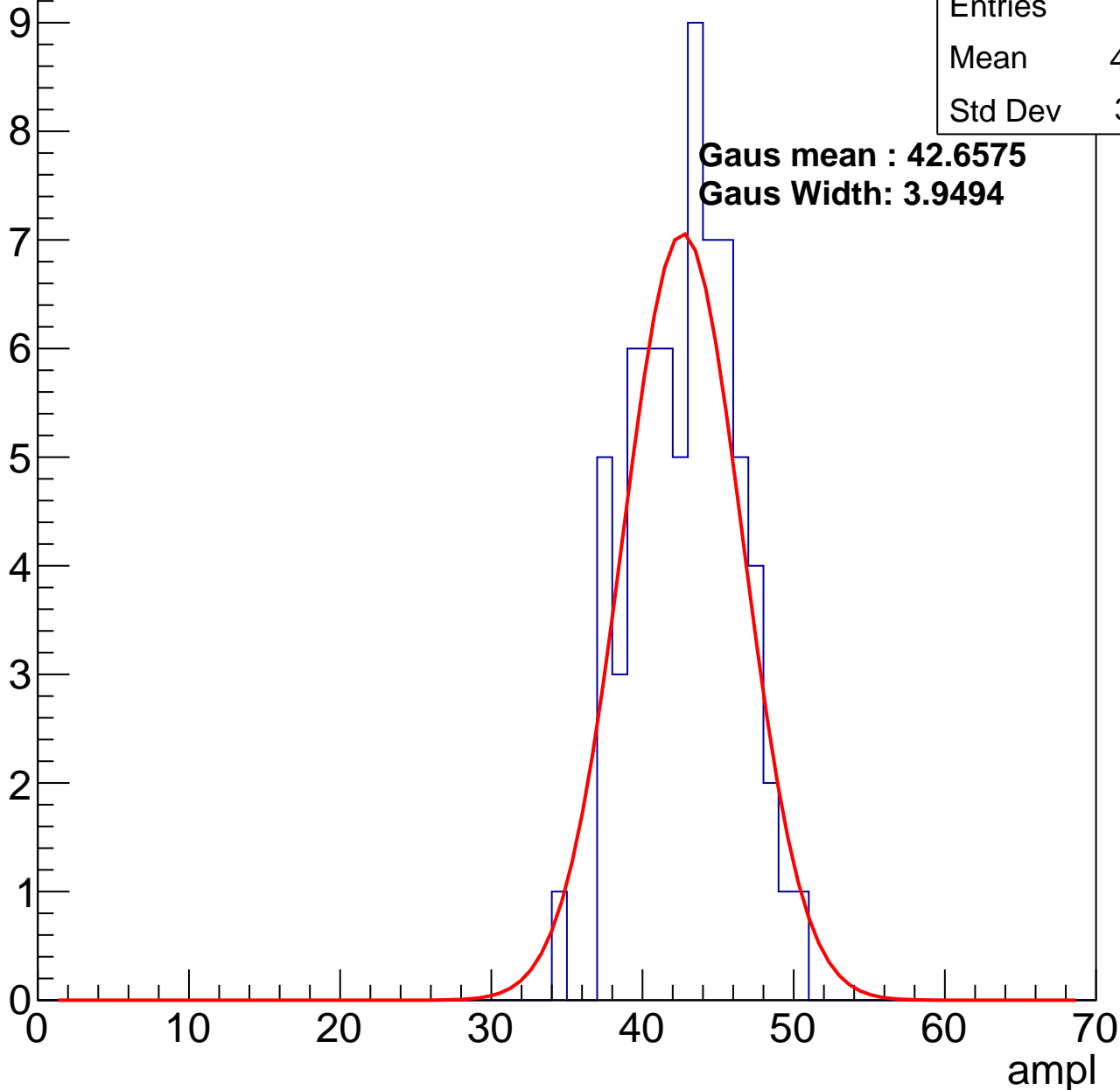
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	68
Mean	42.44
Std Dev	3.371

**Gaus mean : 42.6575**

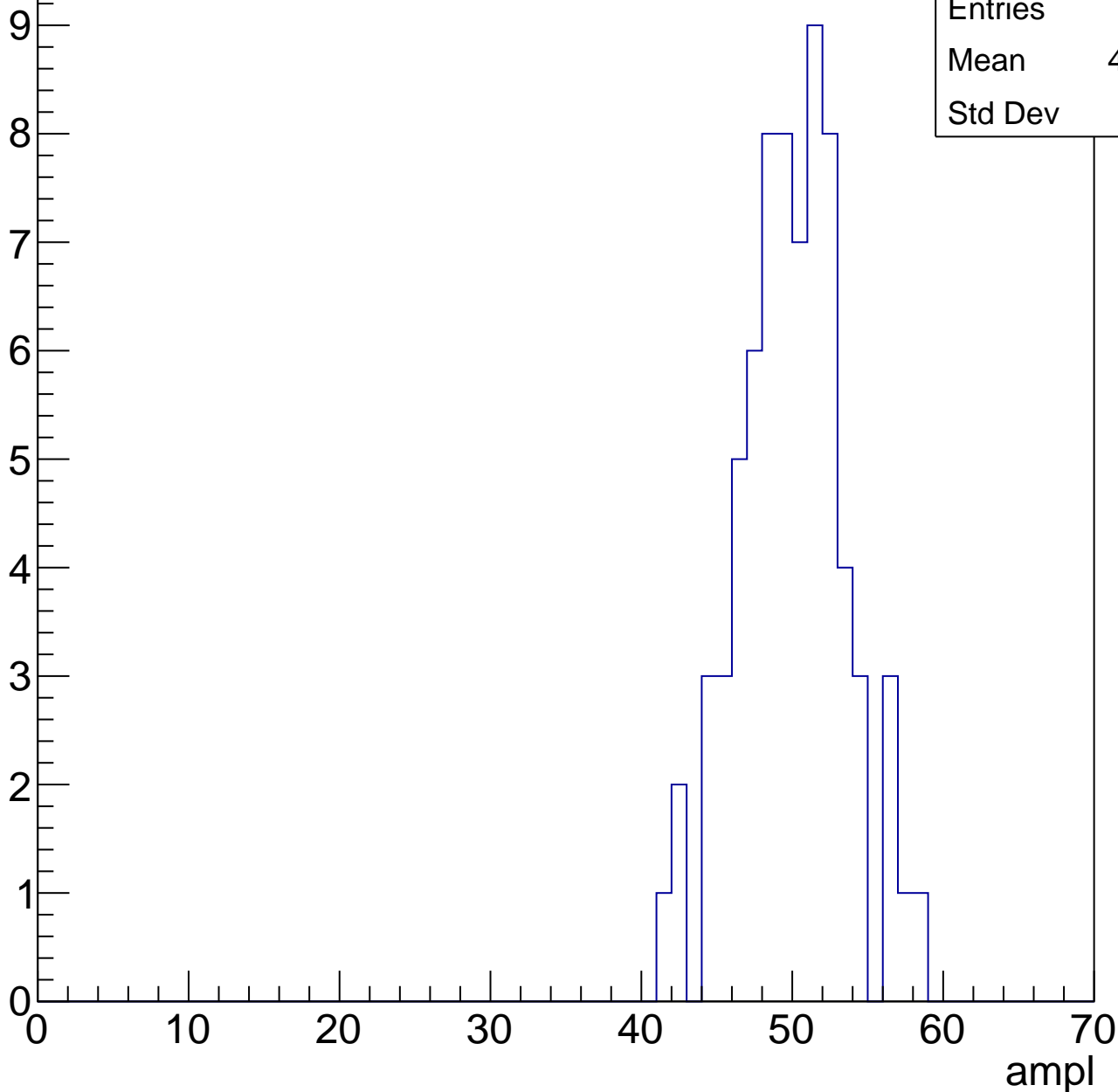
**Gaus Width: 3.9494**



# B1L103S, U9-ch26, adc3

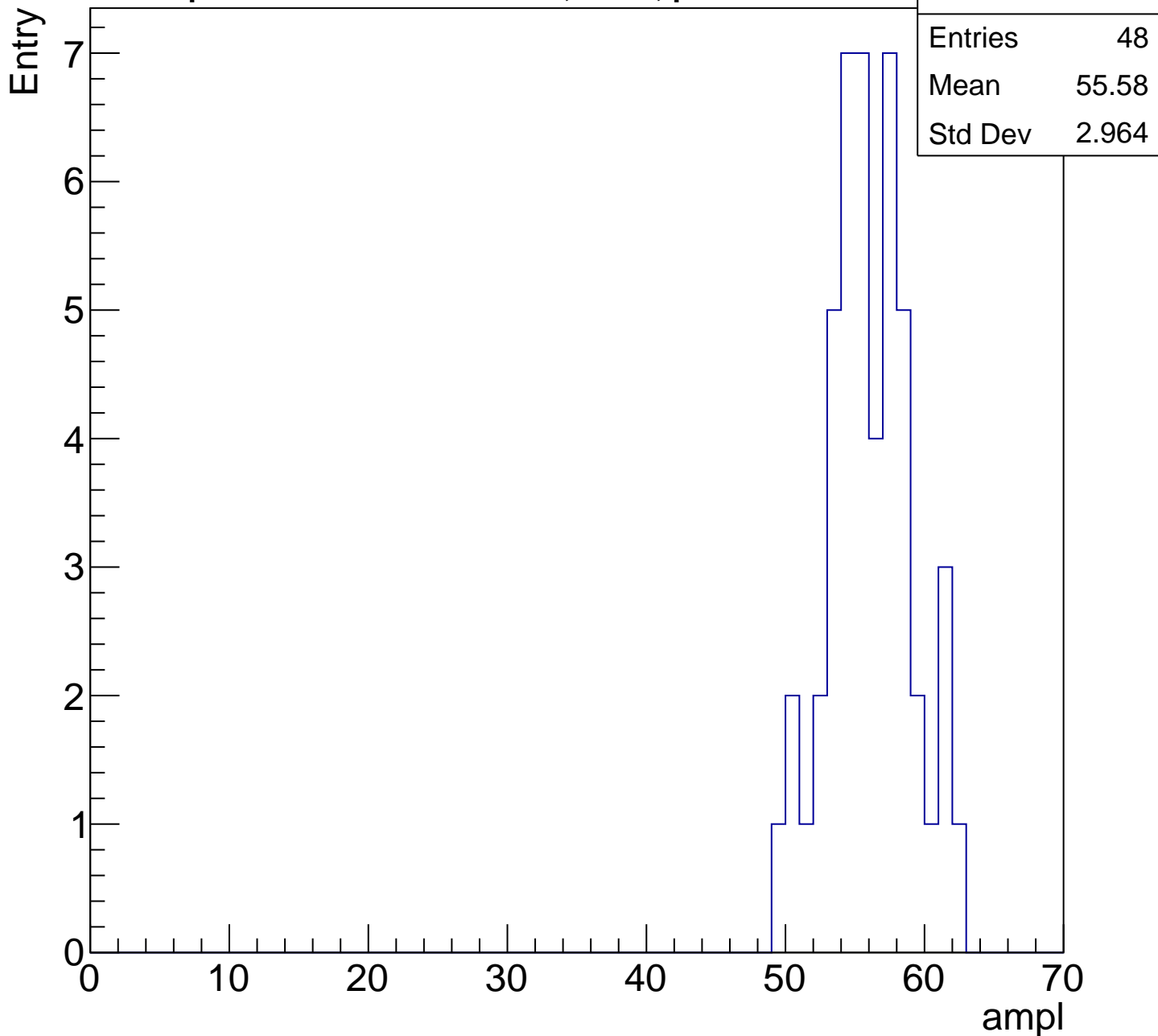
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U9-ch26, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U9-ch26, adc5

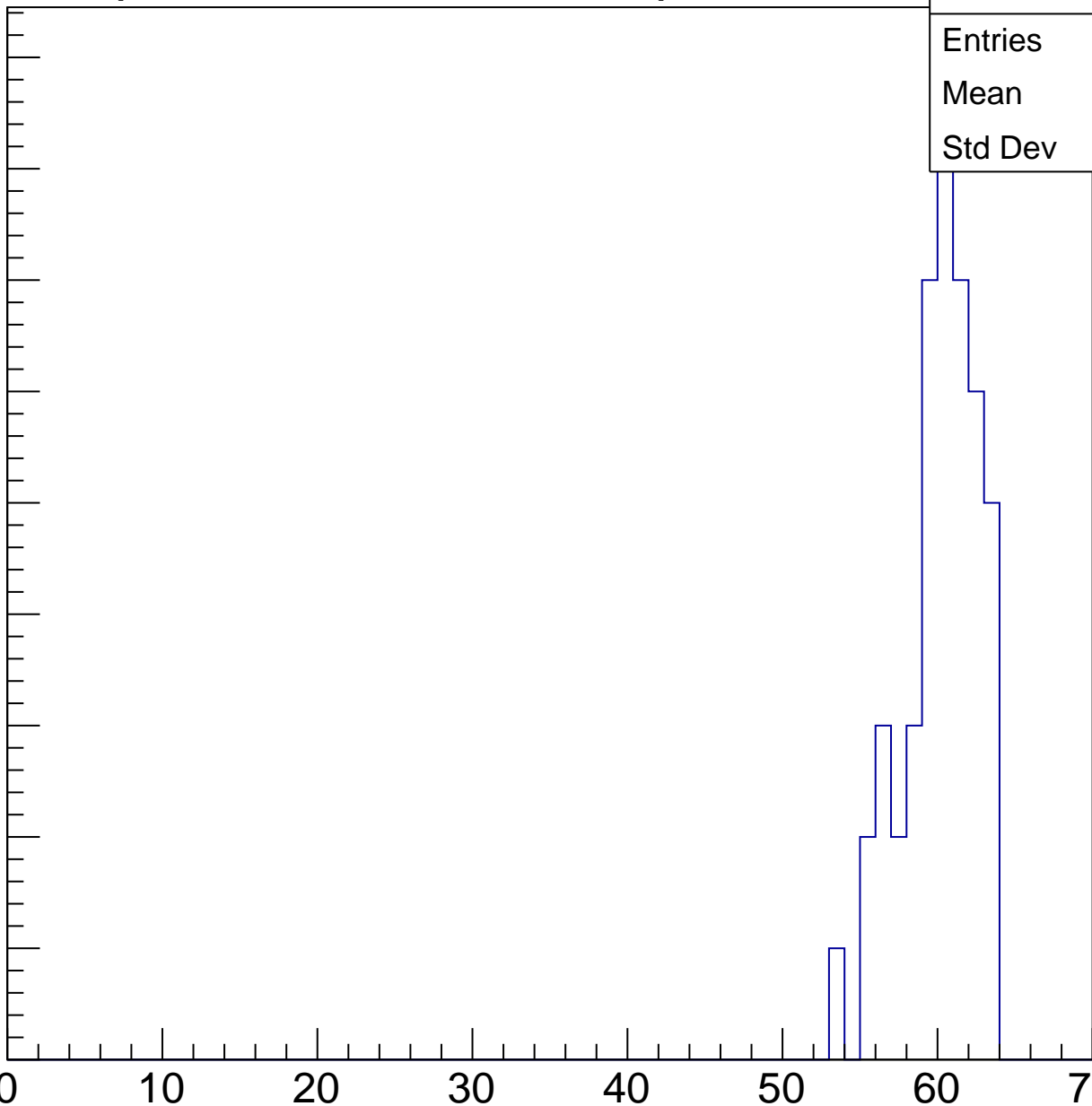
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	45
Mean	59.69
Std Dev	2.383

ampl

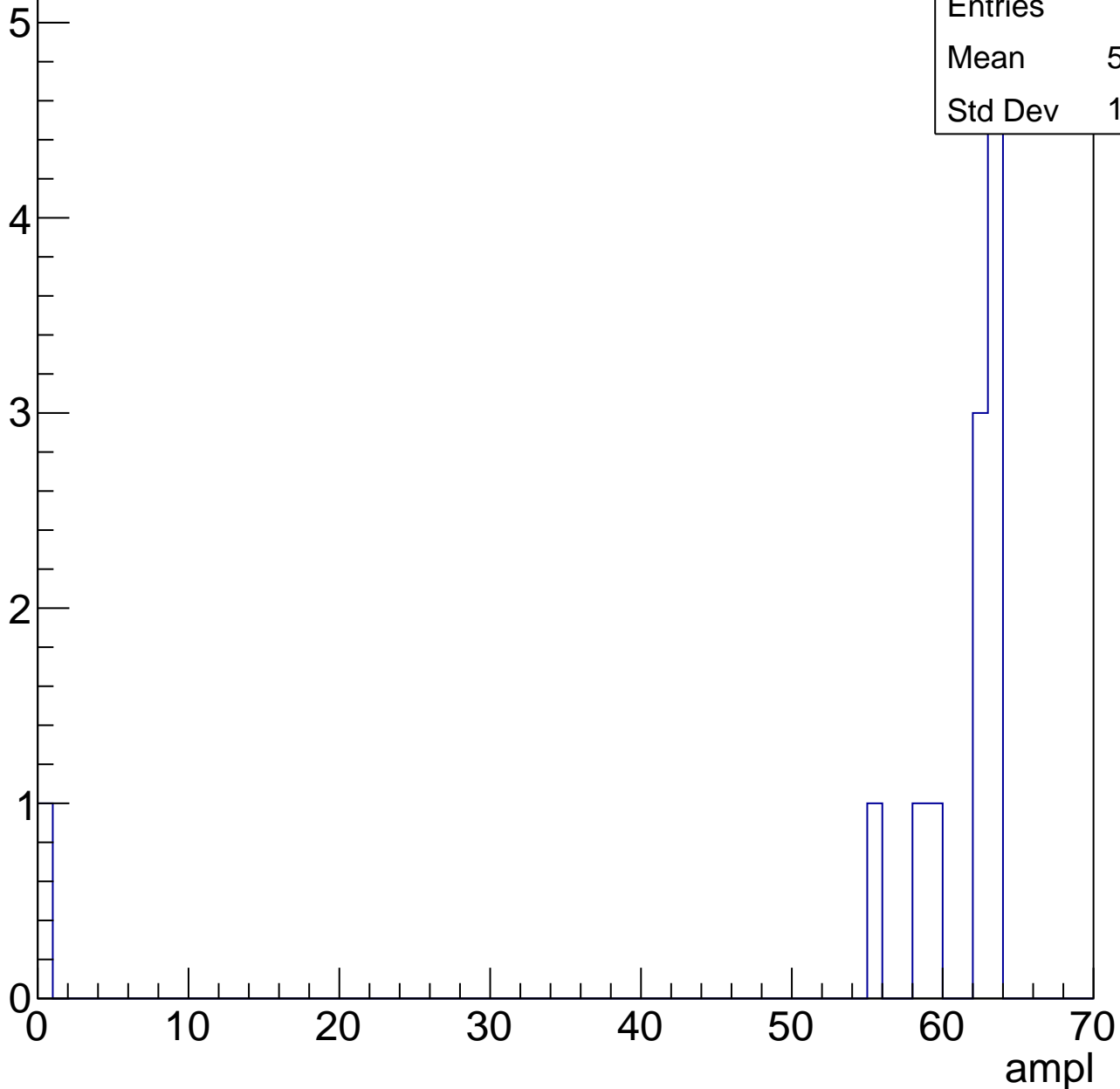


# B1L103S, U9-ch26, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	12
Mean	56.08
Std Dev	17.09

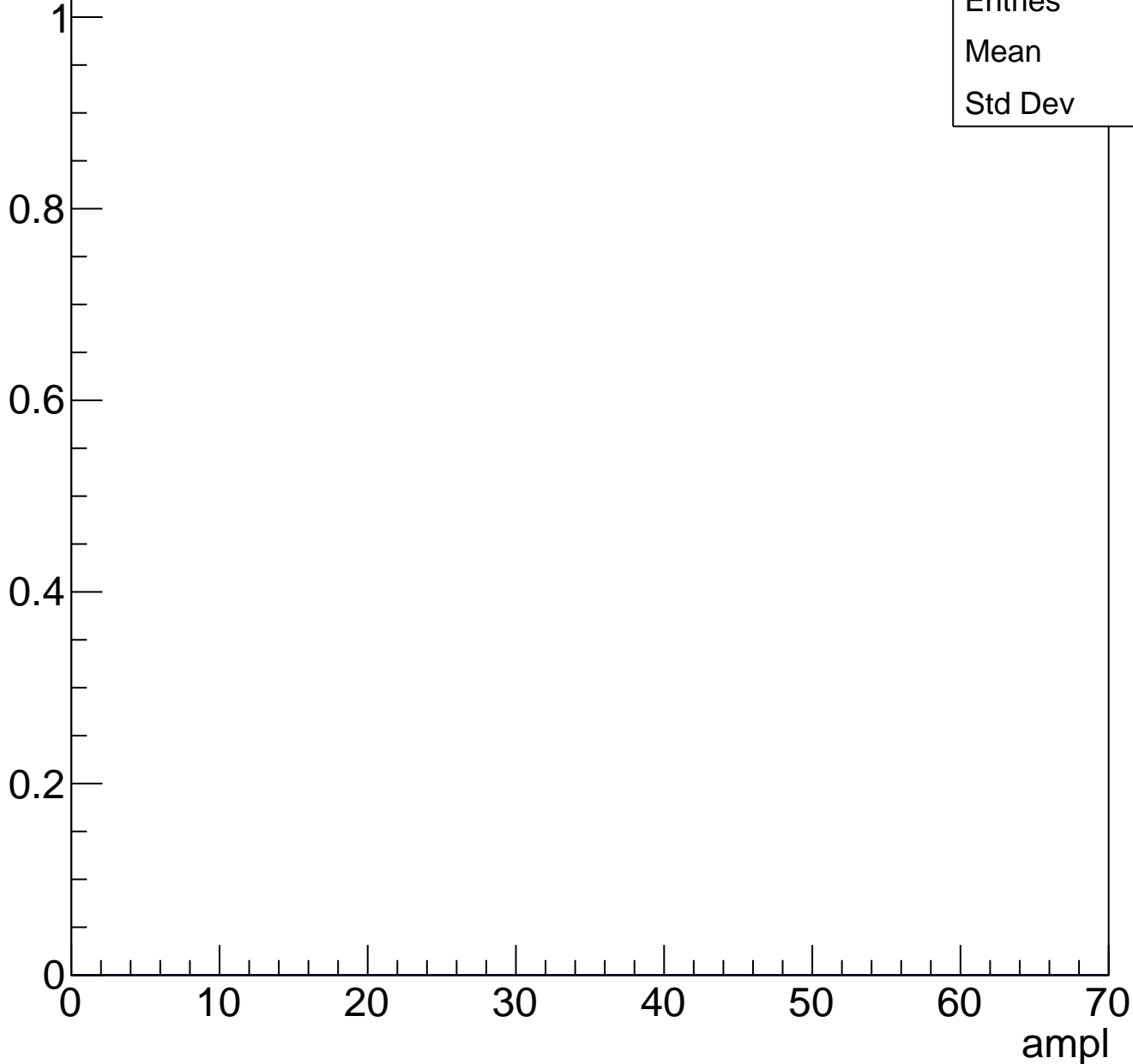




# B1L103S, U9-ch26, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U9-ch27, adc0

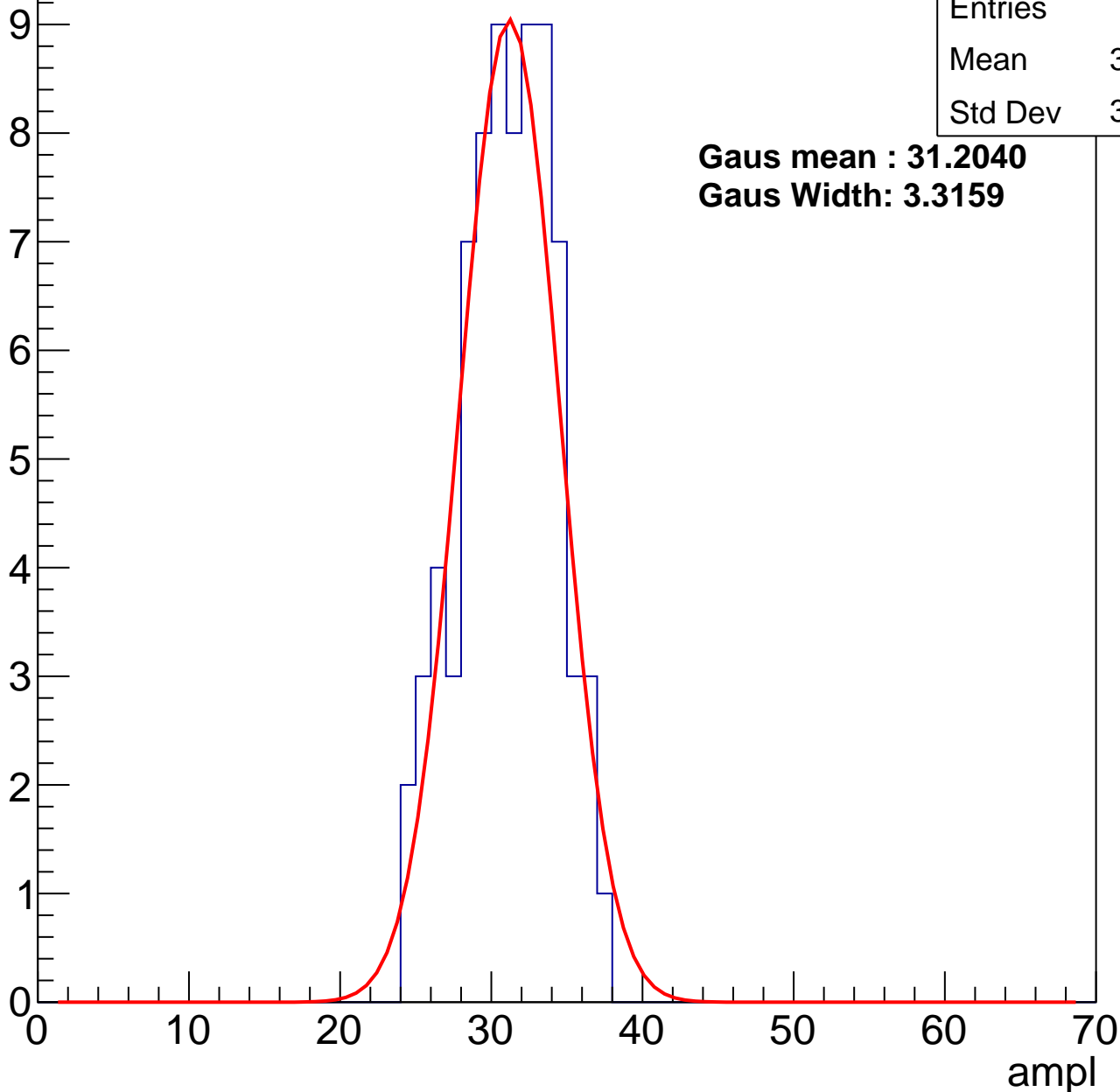
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	76
Mean	30.62
Std Dev	3.065

**Gaus mean : 31.2040**

**Gaus Width: 3.3159**



# B1L103S, U9-ch27, adc1

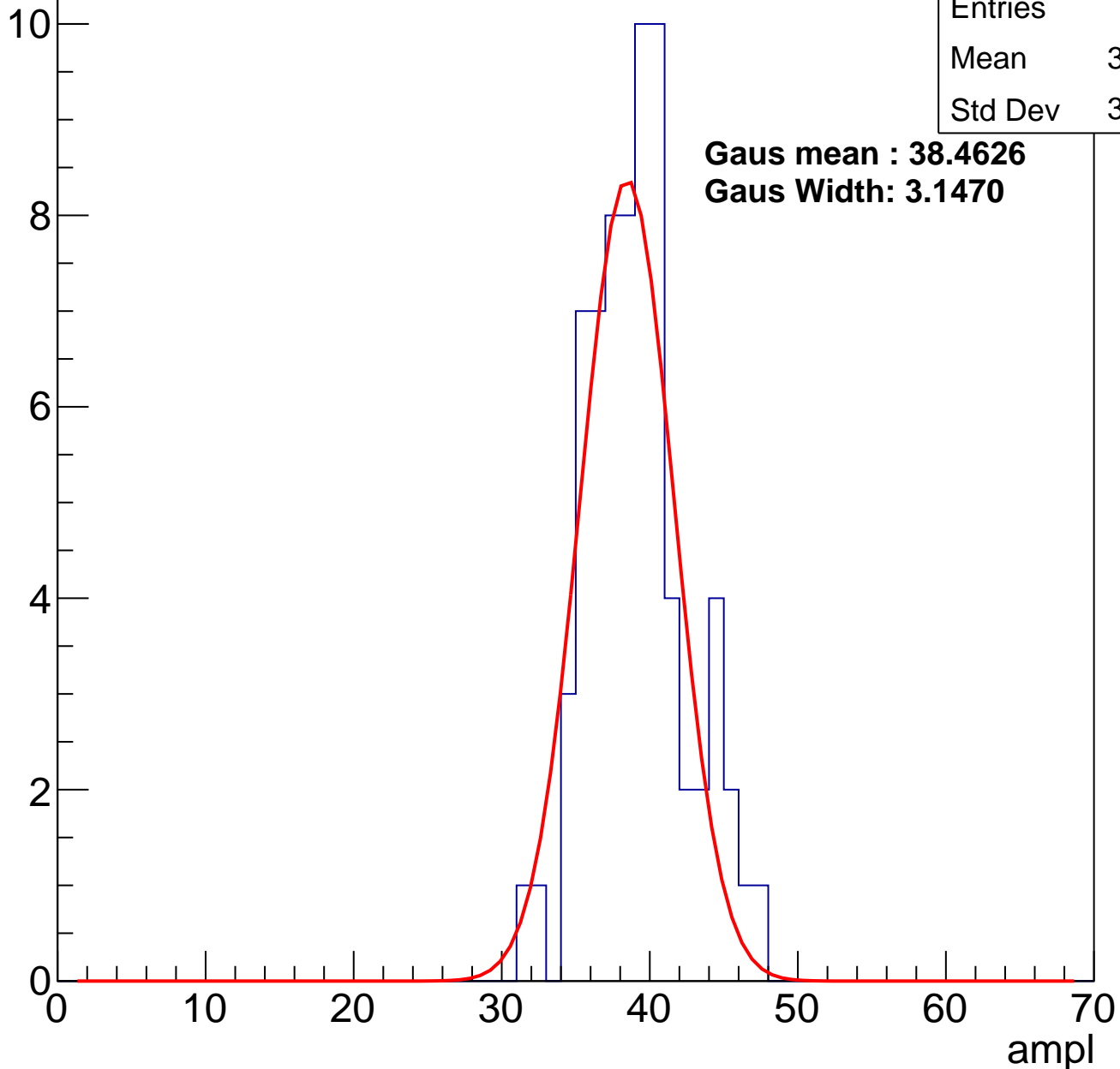
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	71
Mean	38.66
Std Dev	3.263

**Gaus mean : 38.4626**

**Gaus Width: 3.1470**

Entry



# B1L103S, U9-ch27, adc2

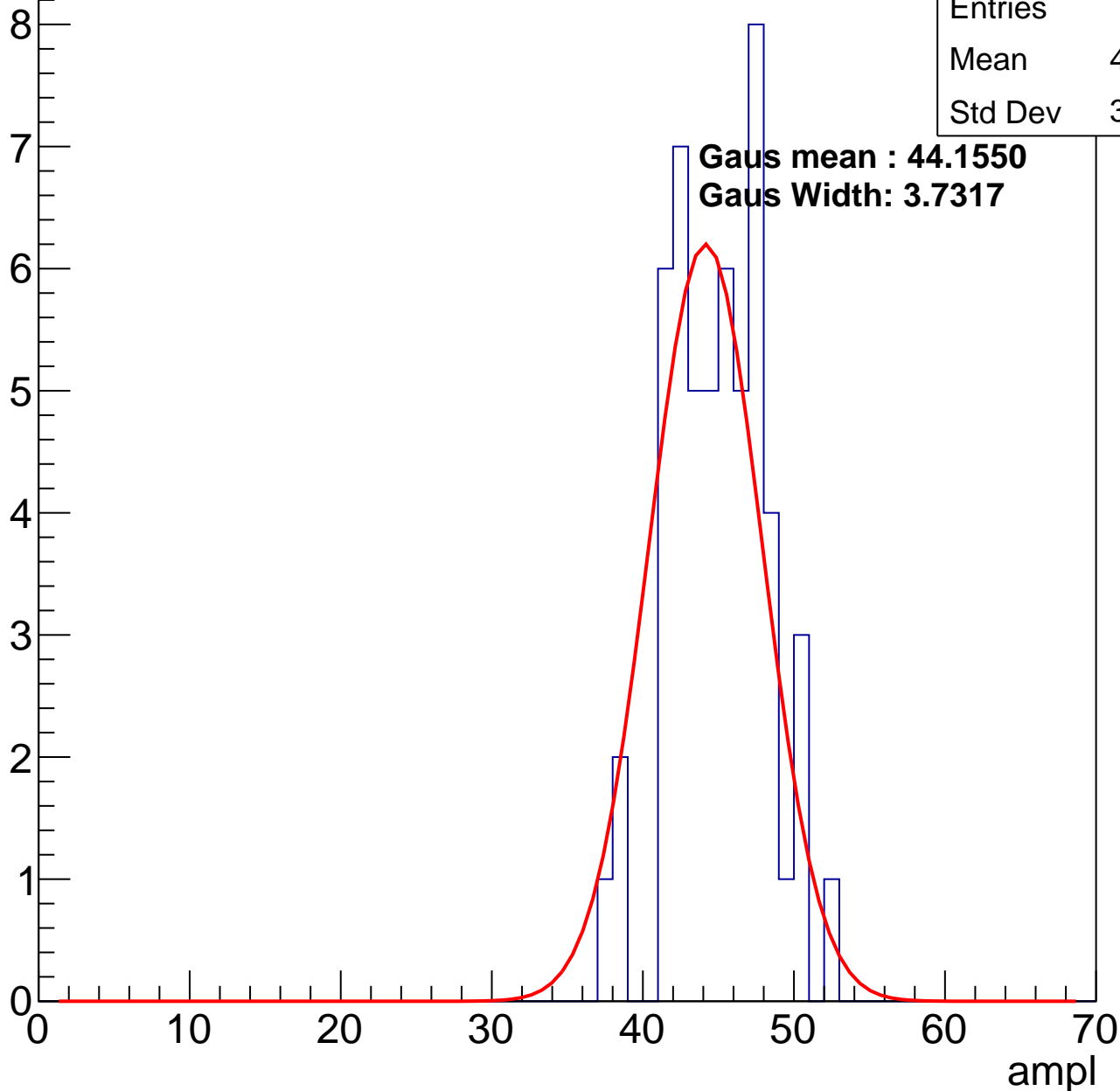
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	54
Mean	44.57
Std Dev	3.189

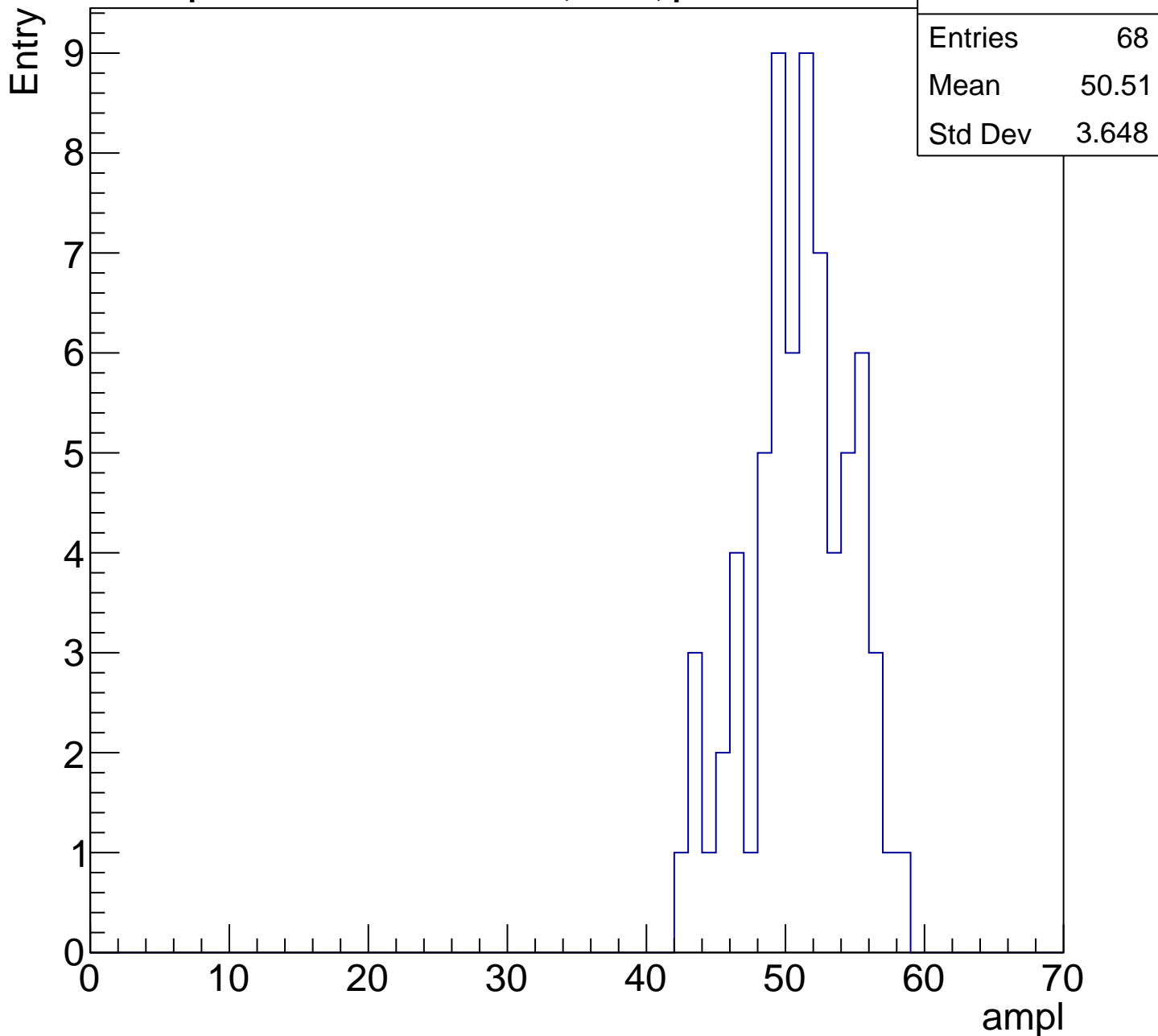
**Gaus mean : 44.1550**

**Gaus Width: 3.7317**



# B1L103S, U9-ch27, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

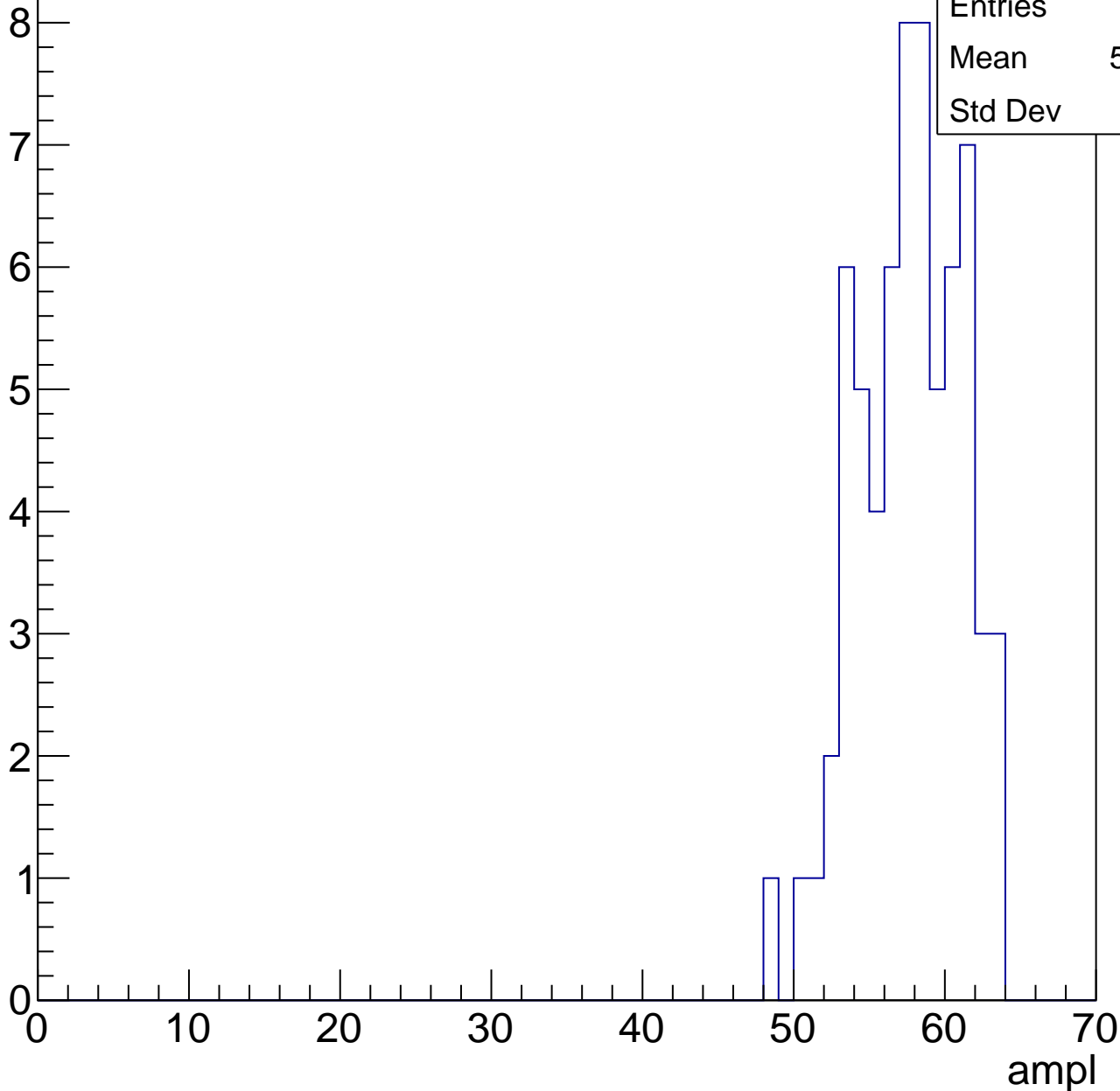


# B1L103S, U9-ch27, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	57.18
Std Dev	3.38

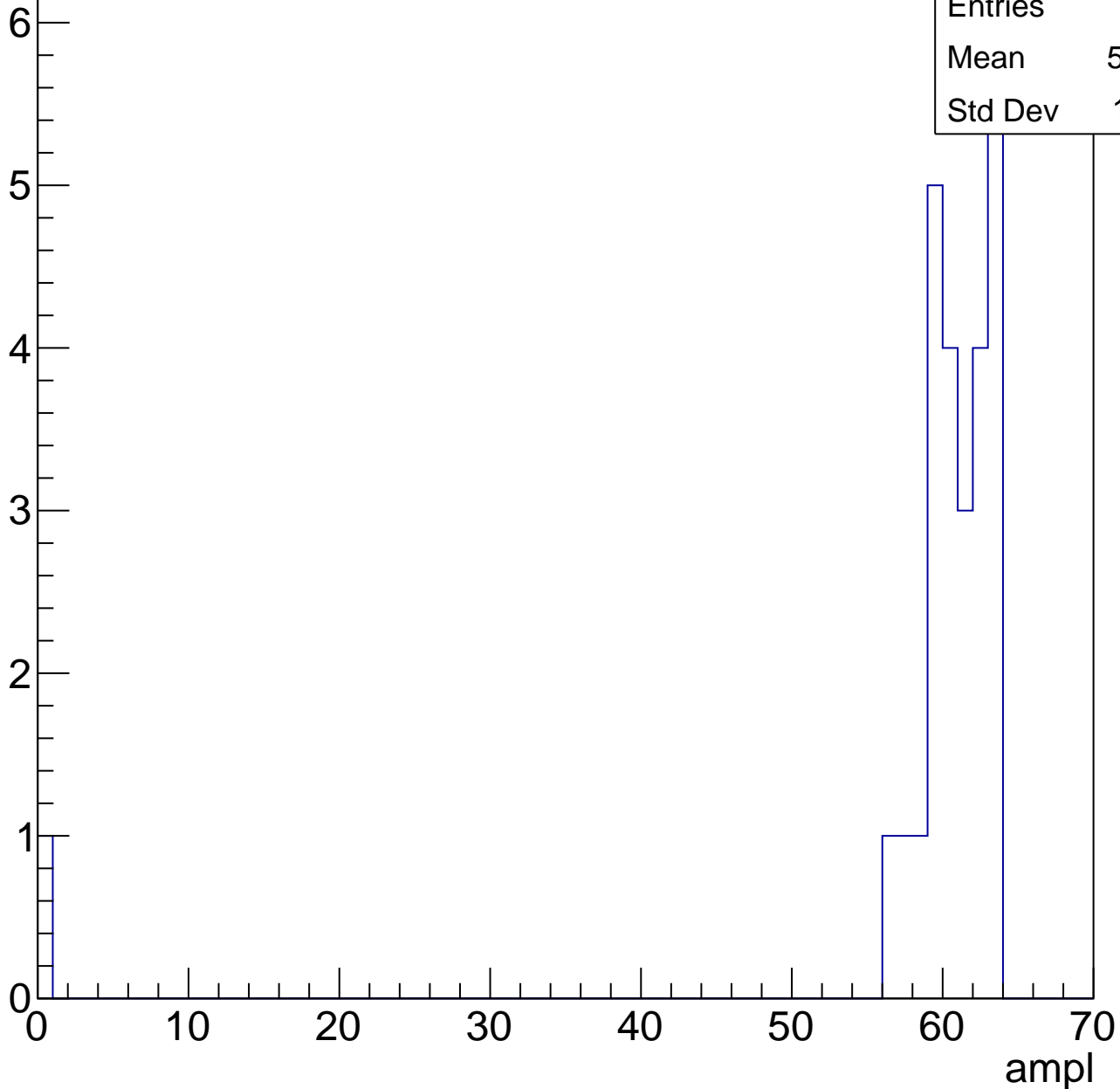


# B1L103S, U9-ch27, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

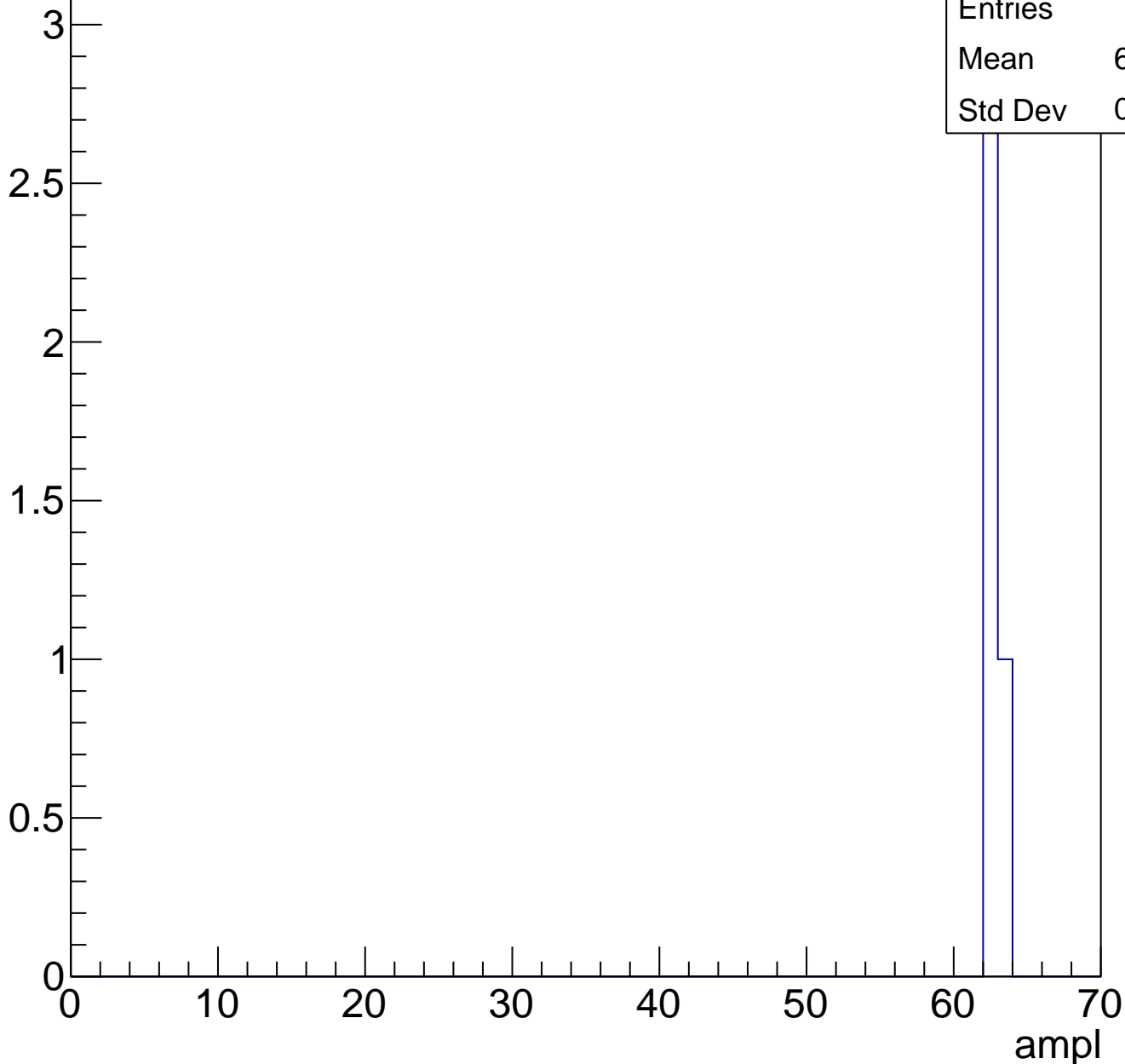
Entries	26
Mean	58.27
Std Dev	11.81



# B1L103S, U9-ch27, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U9-ch27, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

1  
0.8  
0.6  
0.4  
0.2  
0

Entries	1
Mean	23
Std Dev	0

ampl

# B1L103S, U9-ch28, adc0

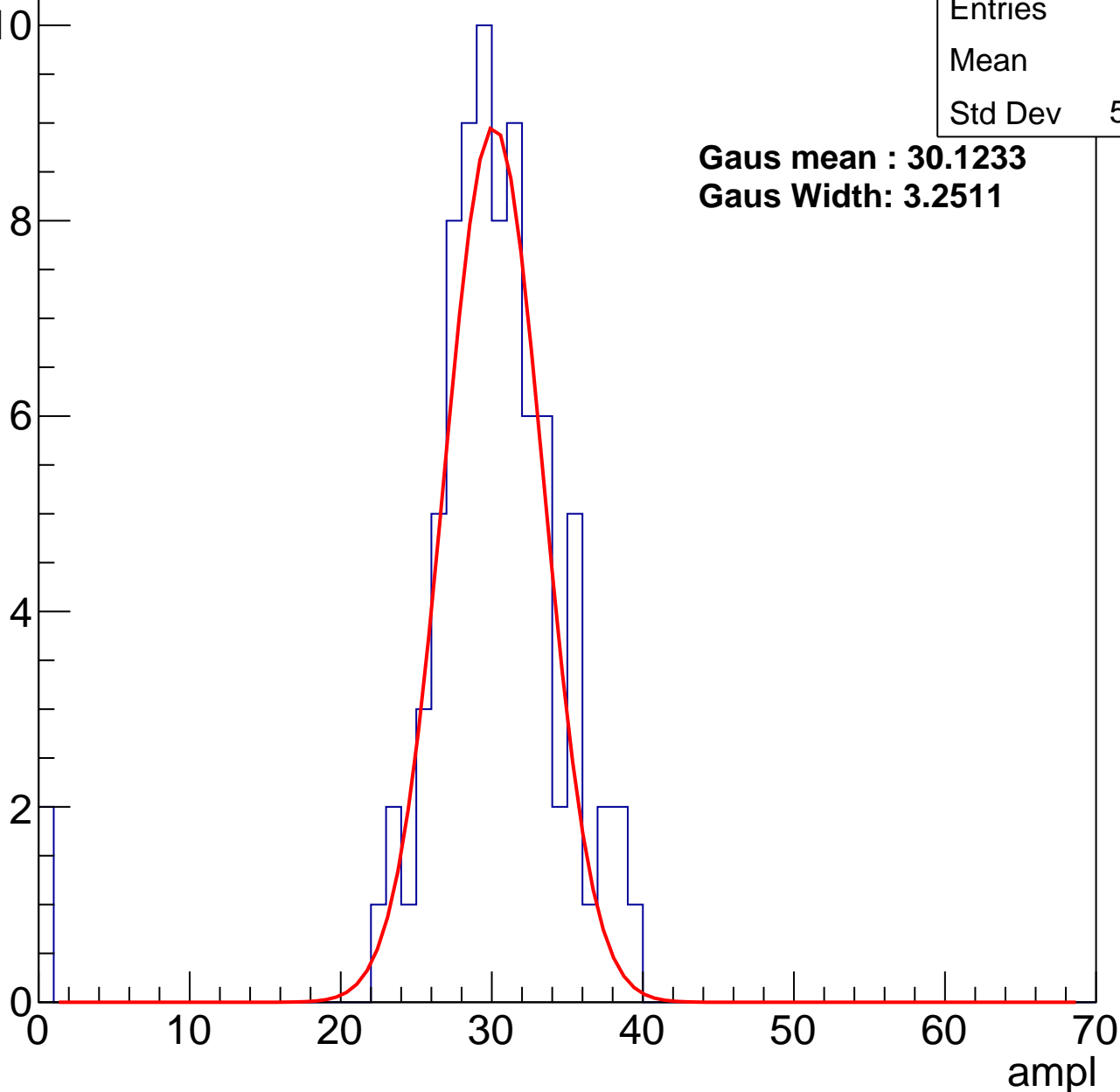
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	83
Mean	29.3
Std Dev	5.826

**Gaus mean : 30.1233**

**Gaus Width: 3.2511**



# B1L103S, U9-ch28, adc1

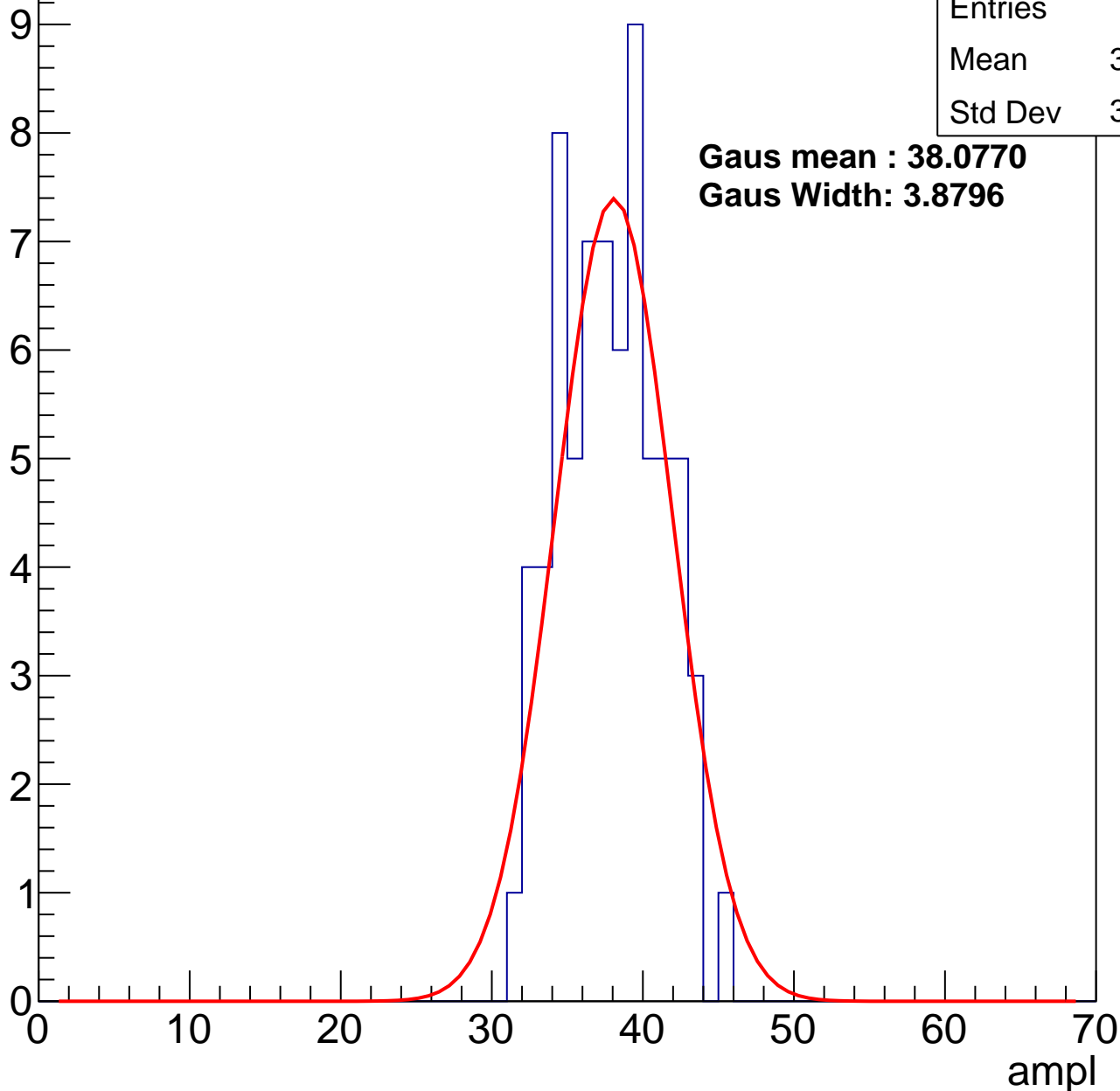
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	70
Mean	37.39
Std Dev	3.279

**Gaus mean : 38.0770**

**Gaus Width: 3.8796**



# B1L103S, U9-ch28, adc2

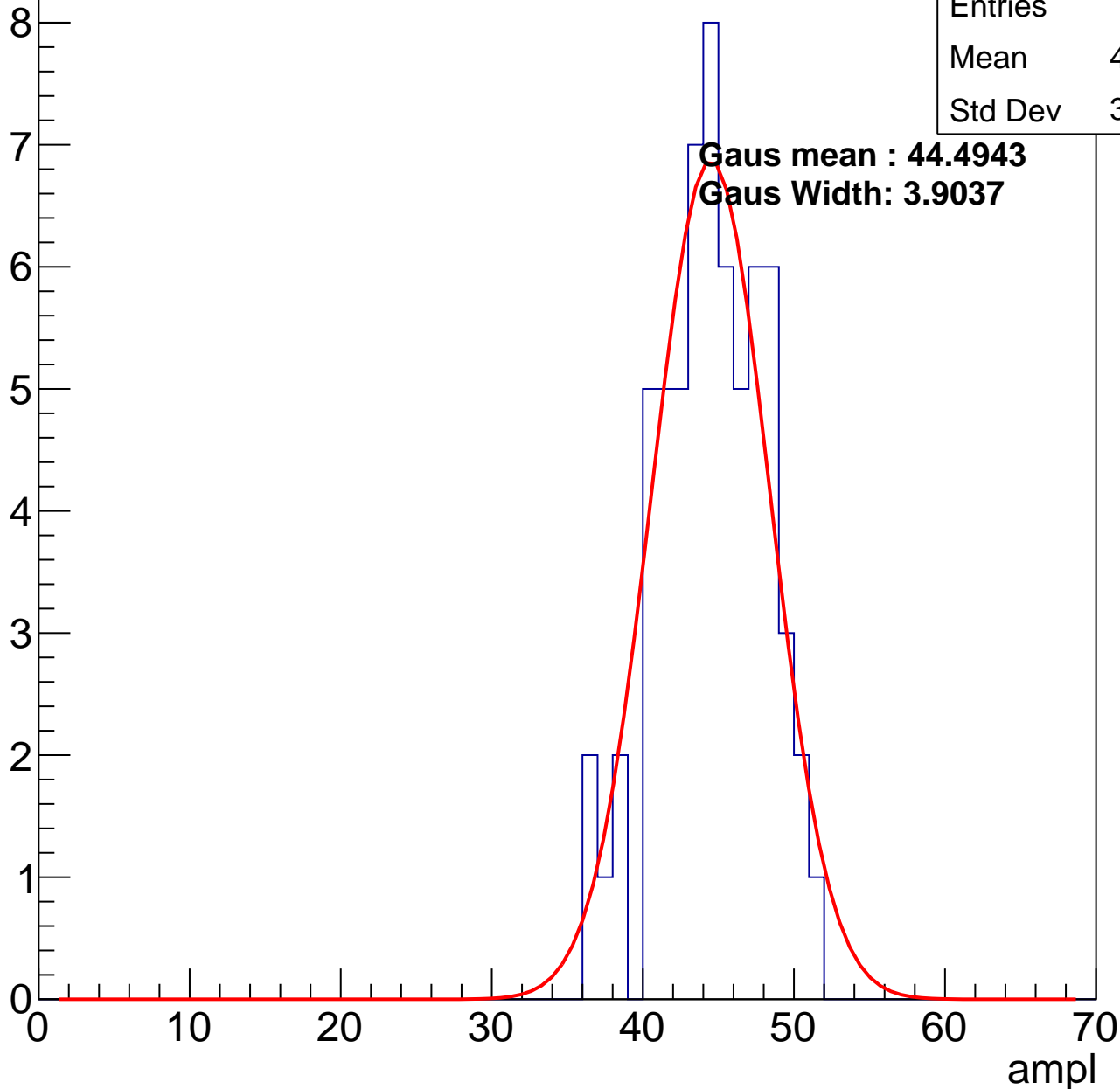
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	44.08
Std Dev	3.474

**Gaus mean : 44.4943**

**Gaus Width: 3.9037**

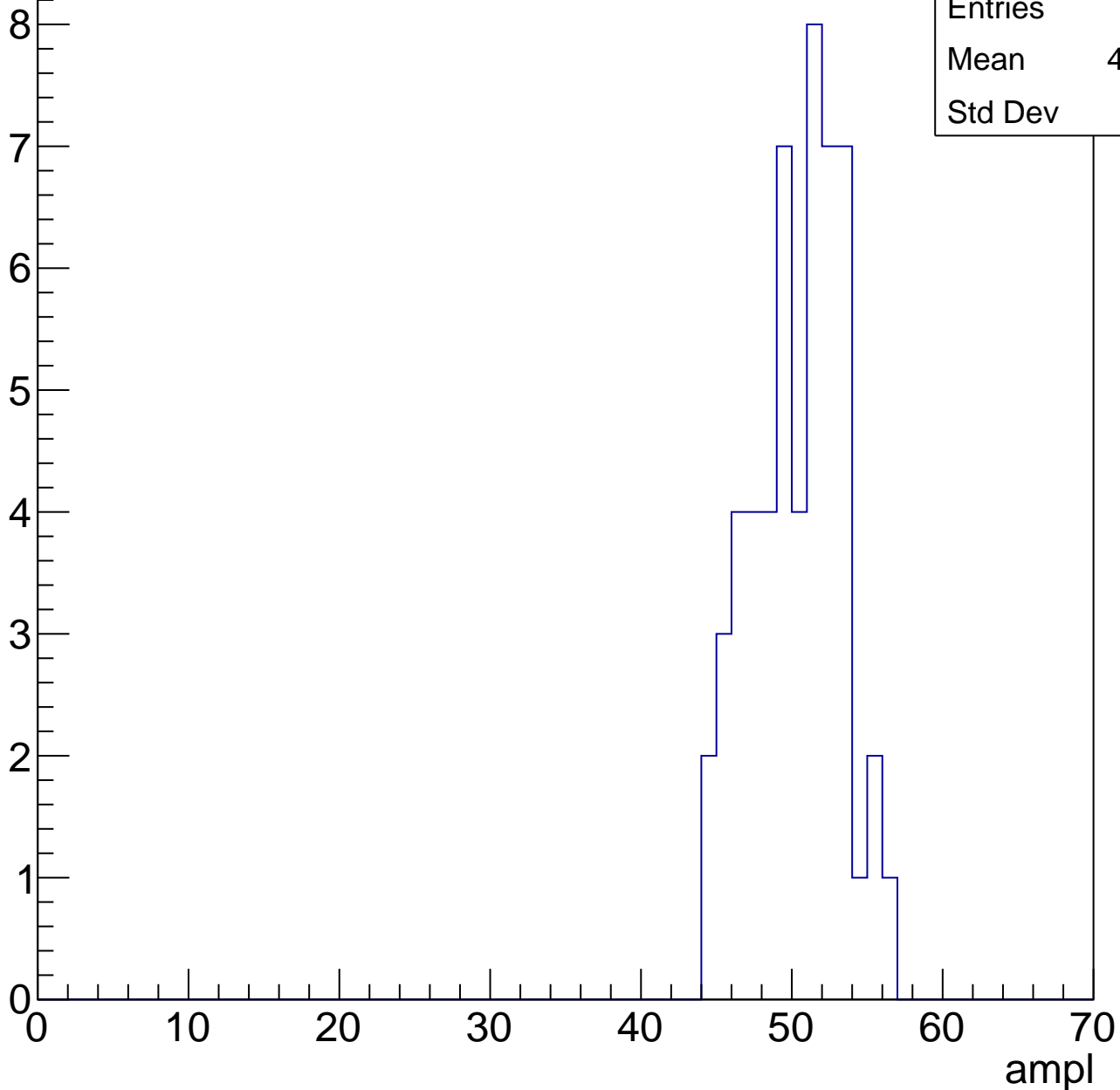


# B1L103S, U9-ch28, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

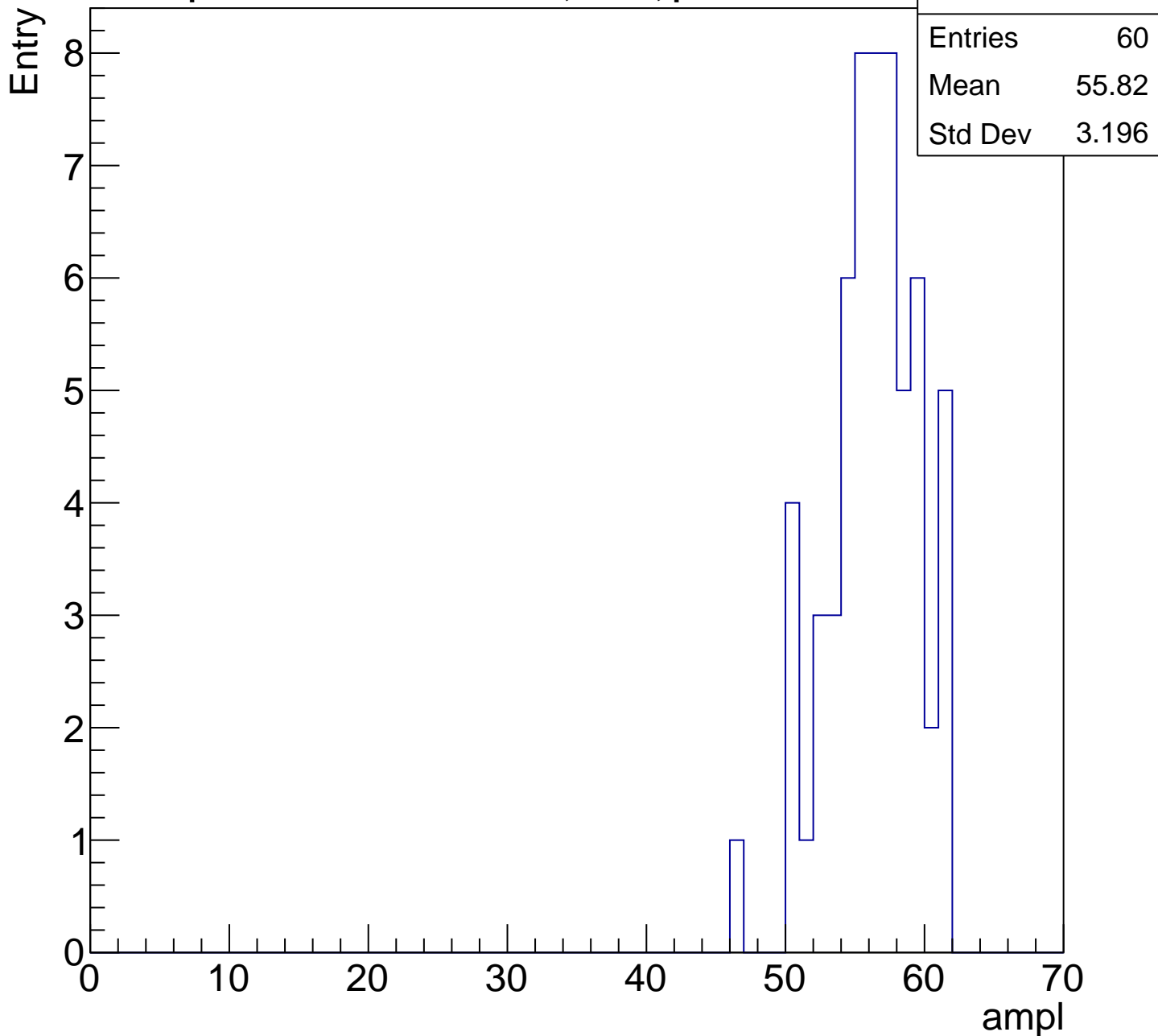
Entry

Entries	54
Mean	49.87
Std Dev	2.95



# B1L103S, U9-ch28, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

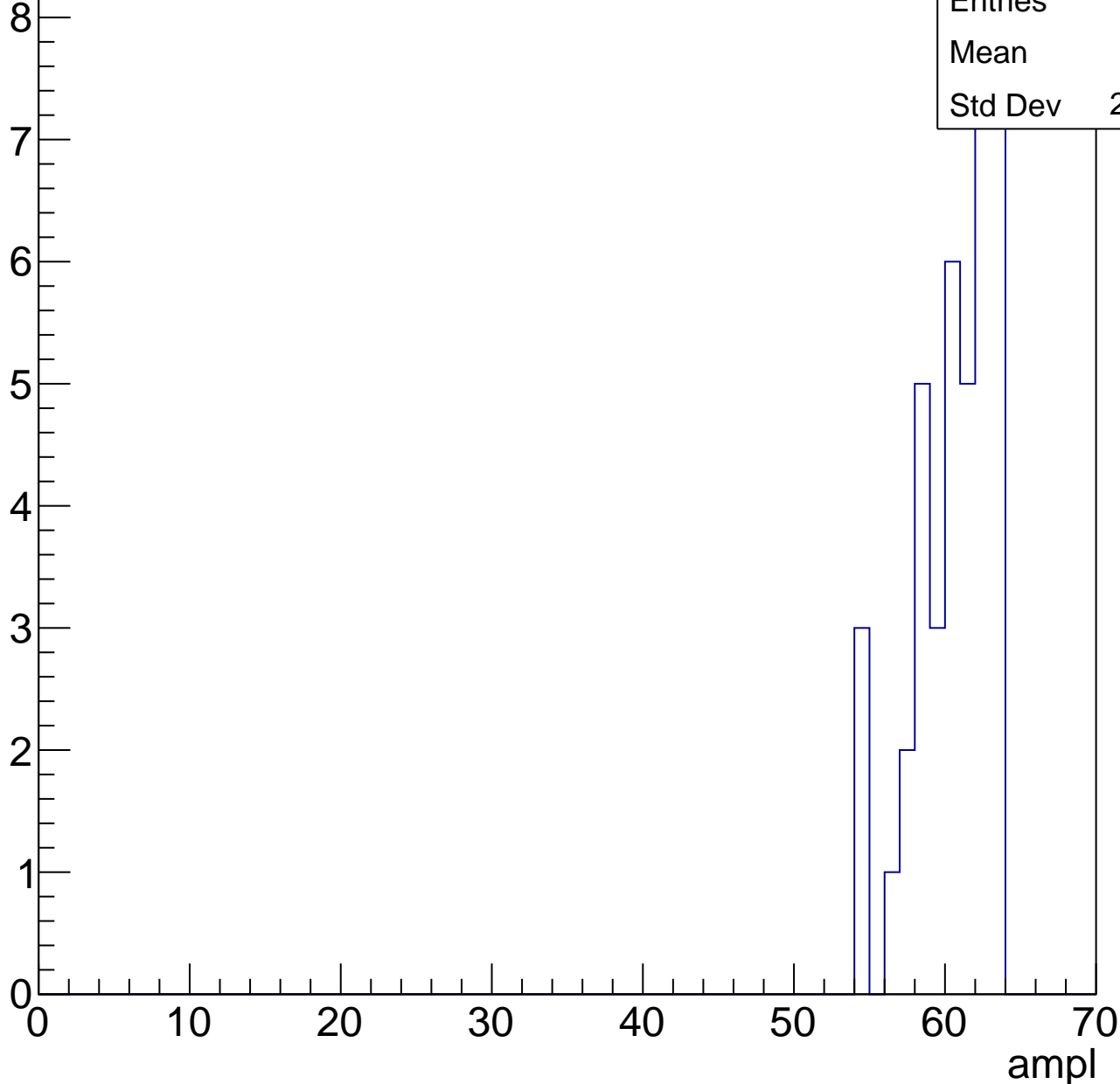


# B1L103S, U9-ch28, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	41
Mean	60.1
Std Dev	2.583



# B1L103S, U9-ch28, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

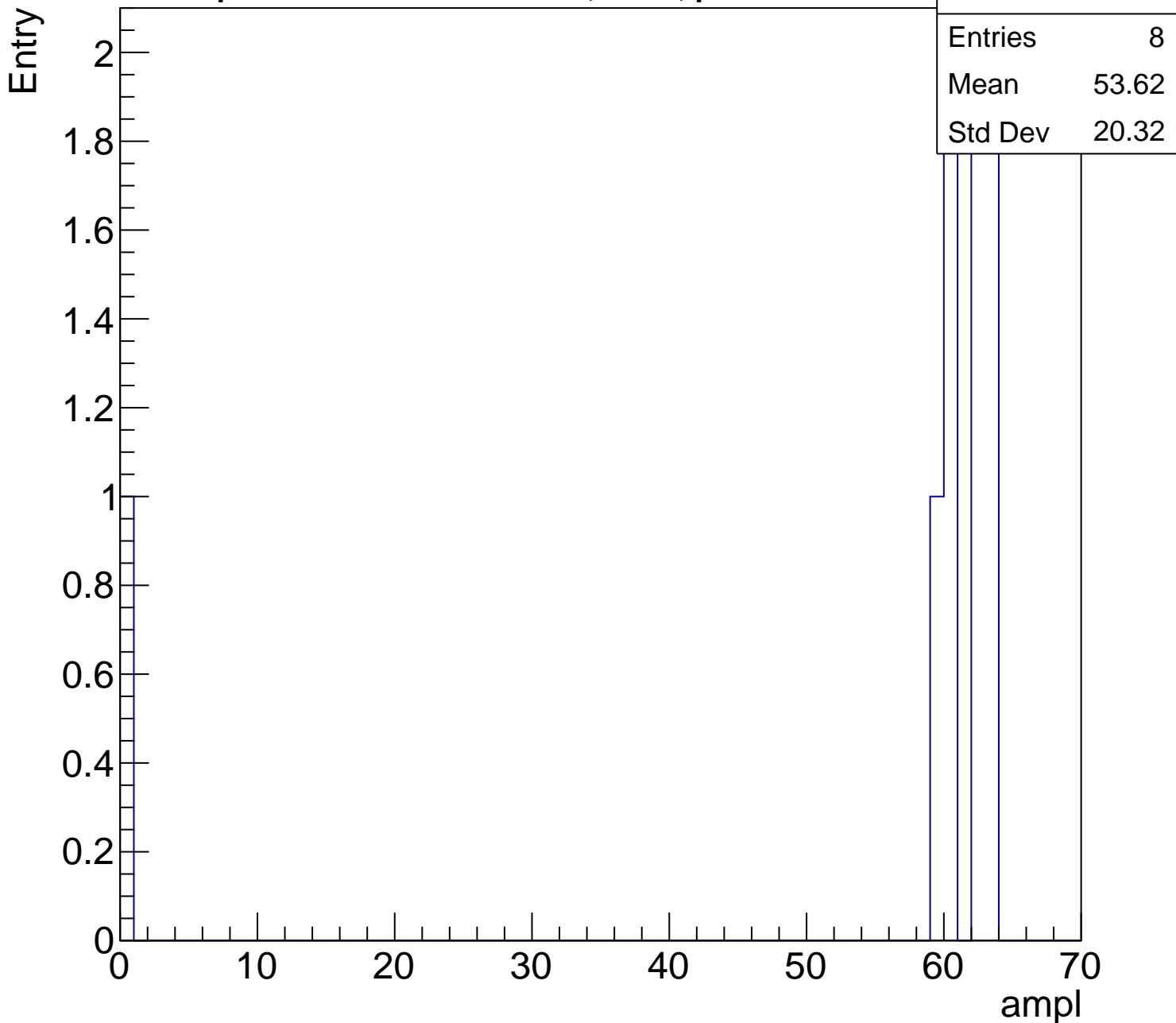
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	8
Mean	53.62
Std Dev	20.32

0 10 20 30 40 50 60 70

ampl





# B1L103S, U9-ch28, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U9-ch29, adc0

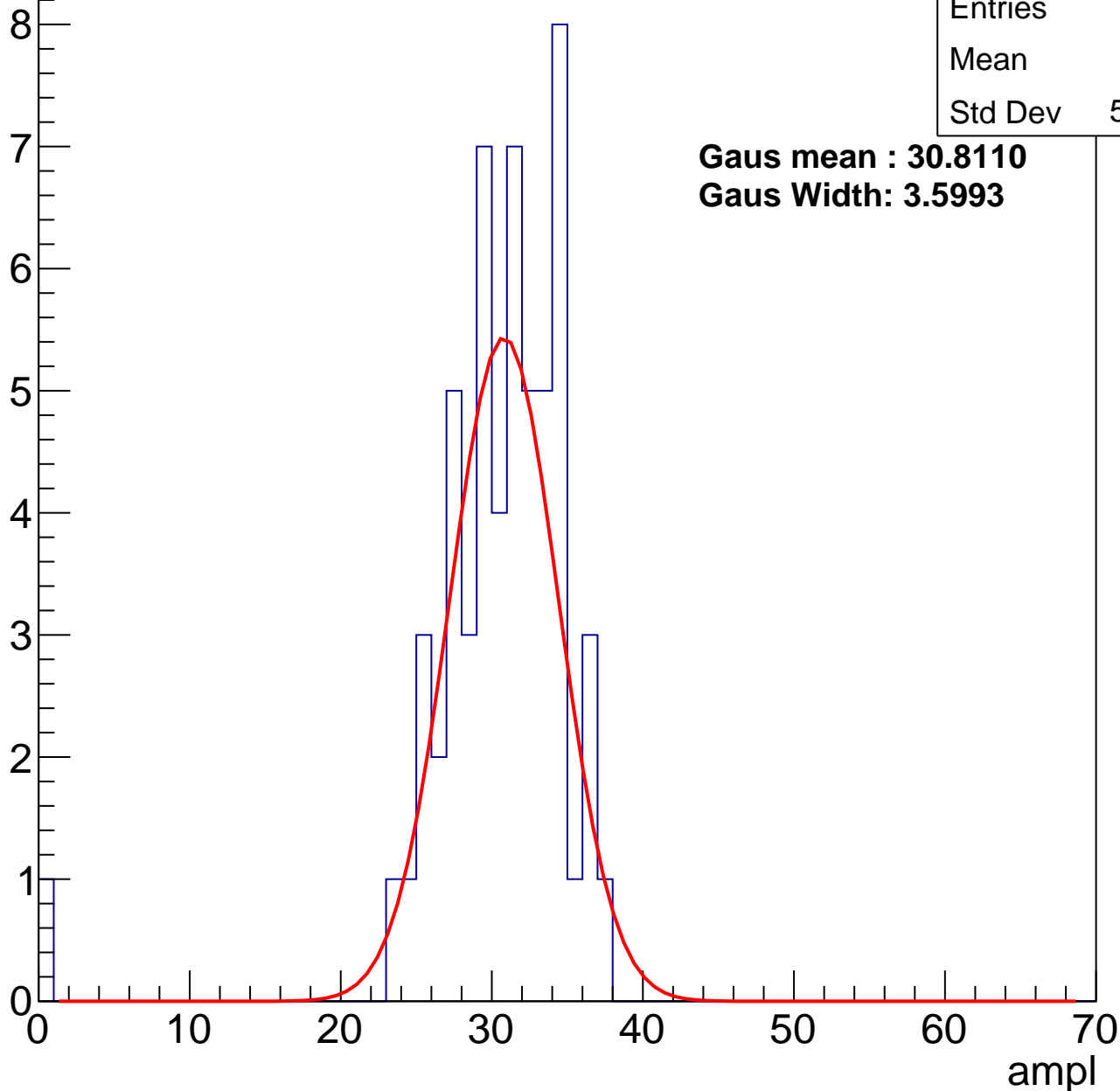
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	57
Mean	30
Std Dev	5.194

**Gaus mean : 30.8110**

**Gaus Width: 3.5993**



# B1L103S, U9-ch29, adc1

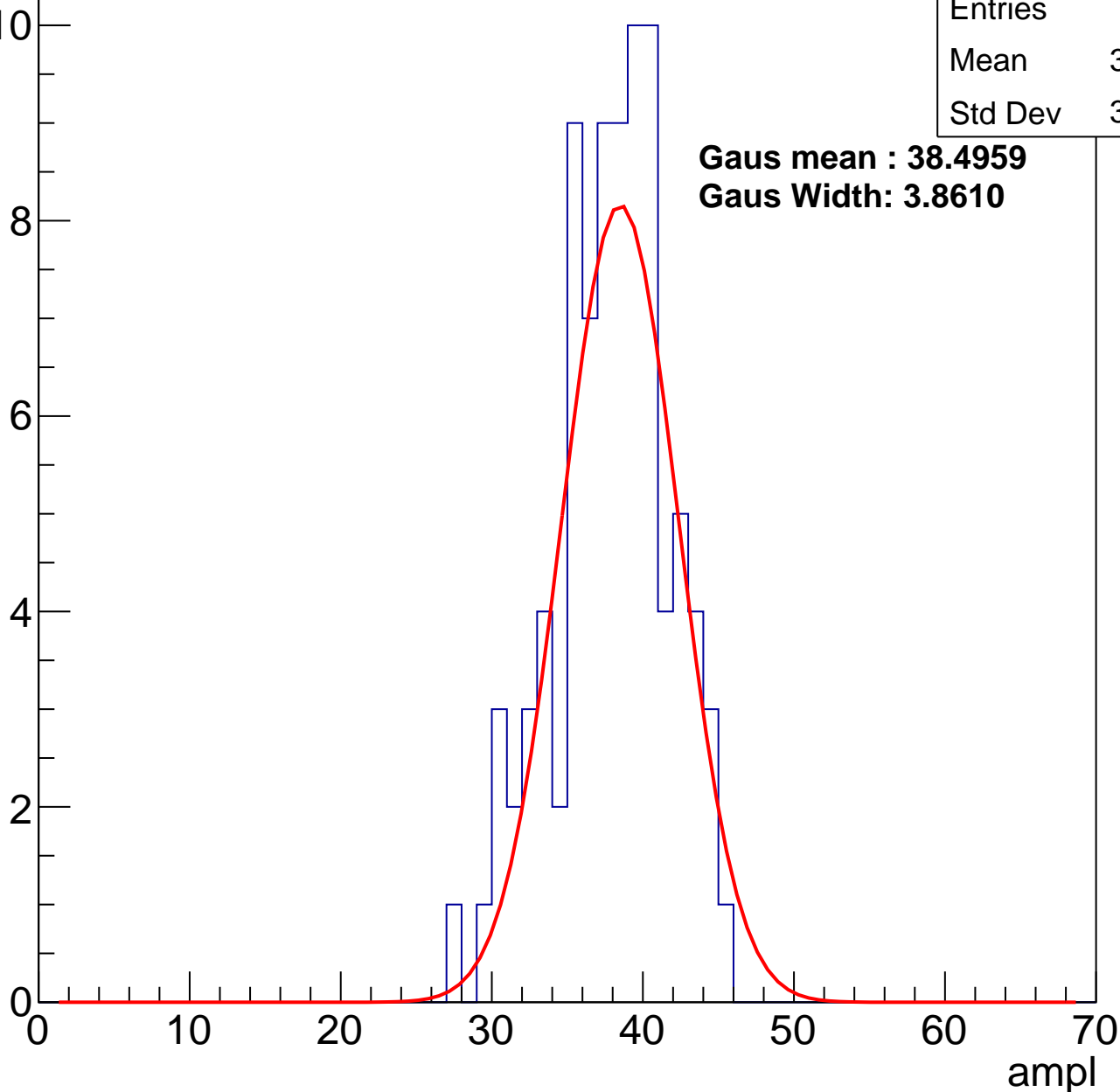
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	87
Mean	37.46
Std Dev	3.787

**Gaus mean : 38.4959**

**Gaus Width: 3.8610**



# B1L103S, U9-ch29, adc2

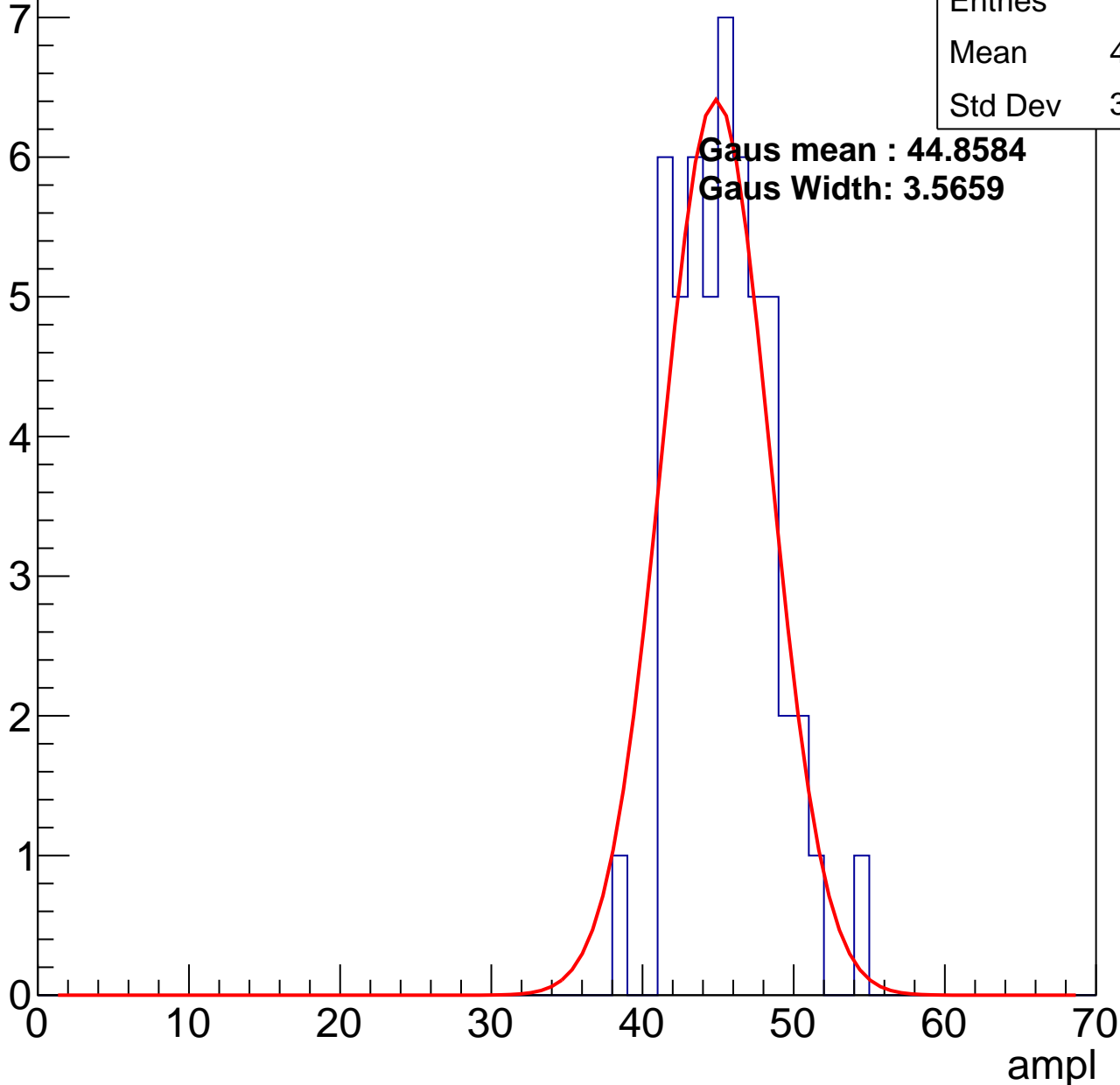
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	52
Mean	45.02
Std Dev	3.067

**Gaus mean : 44.8584**

**Gaus Width: 3.5659**

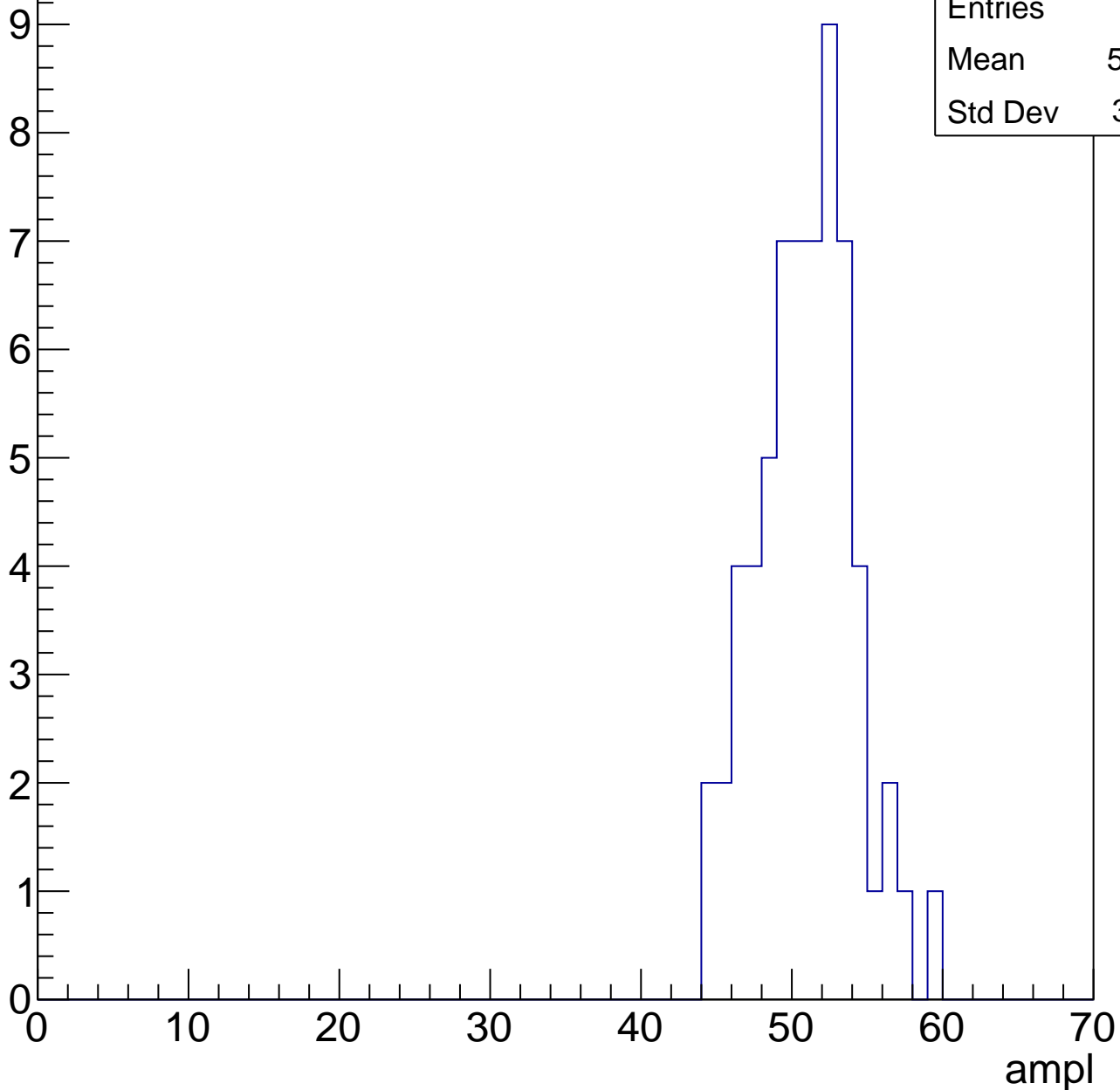


# B1L103S, U9-ch29, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	50.44
Std Dev	3.171

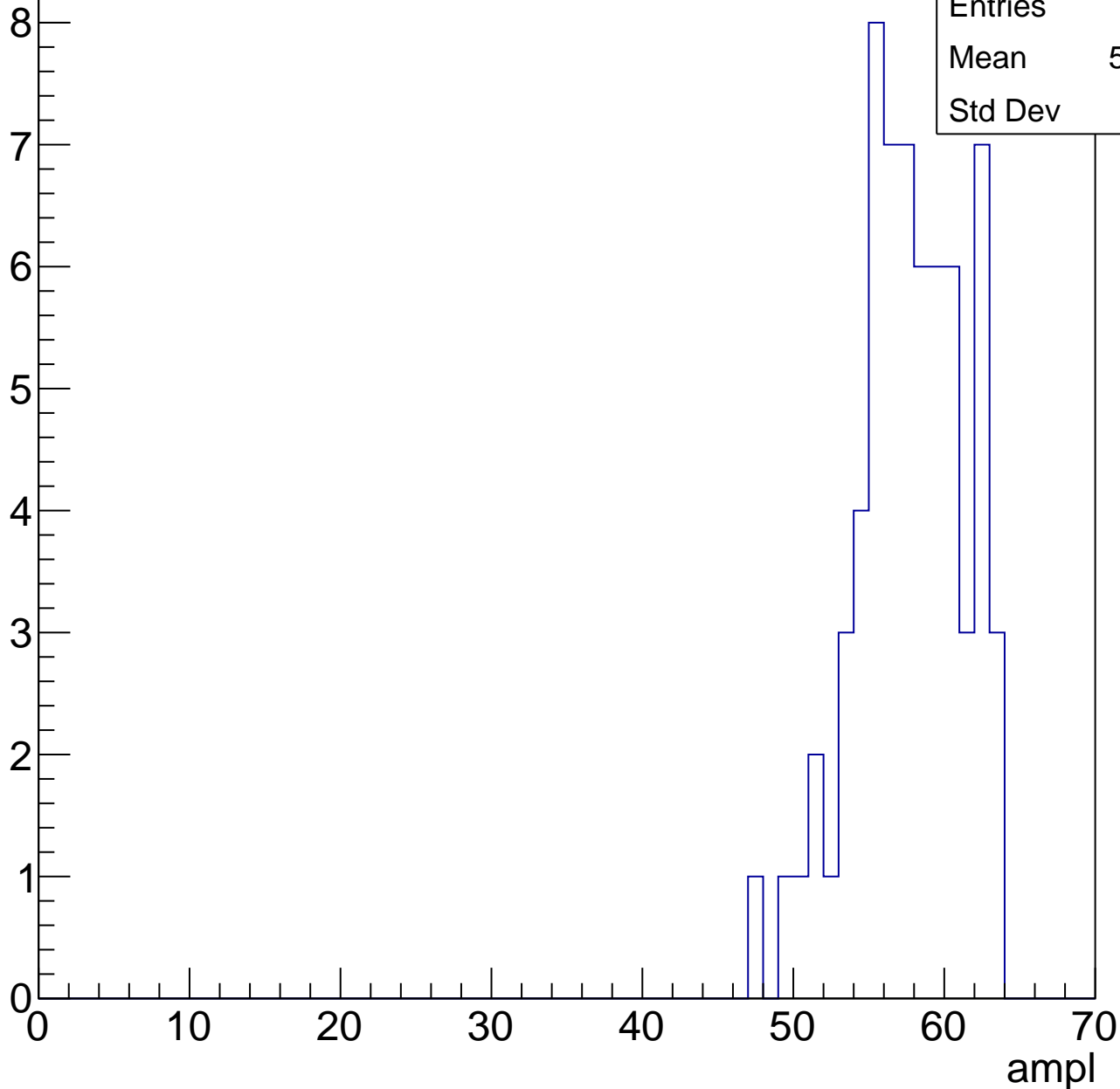


# B1L103S, U9-ch29, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	57.18
Std Dev	3.58

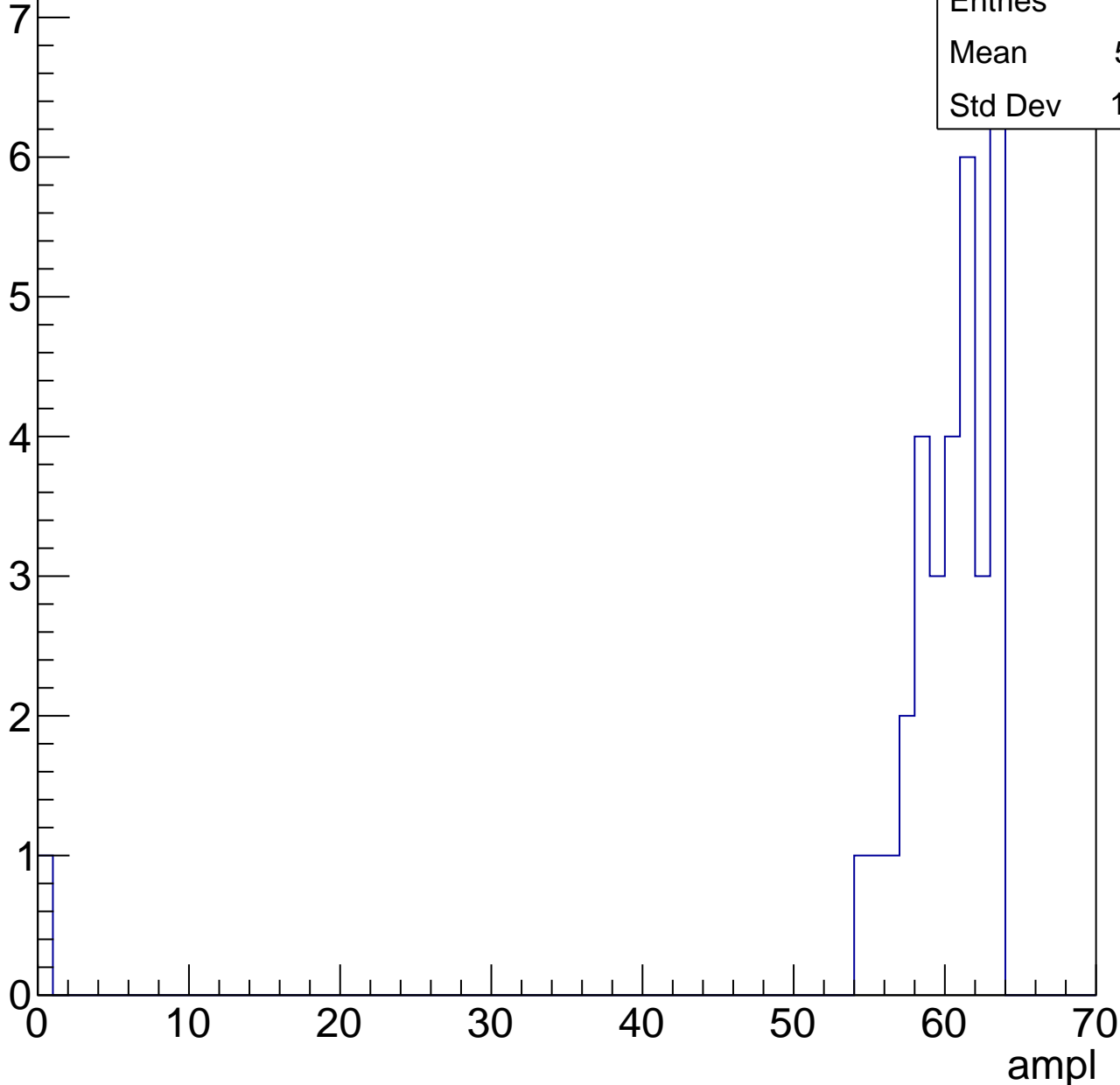


# B1L103S, U9-ch29, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

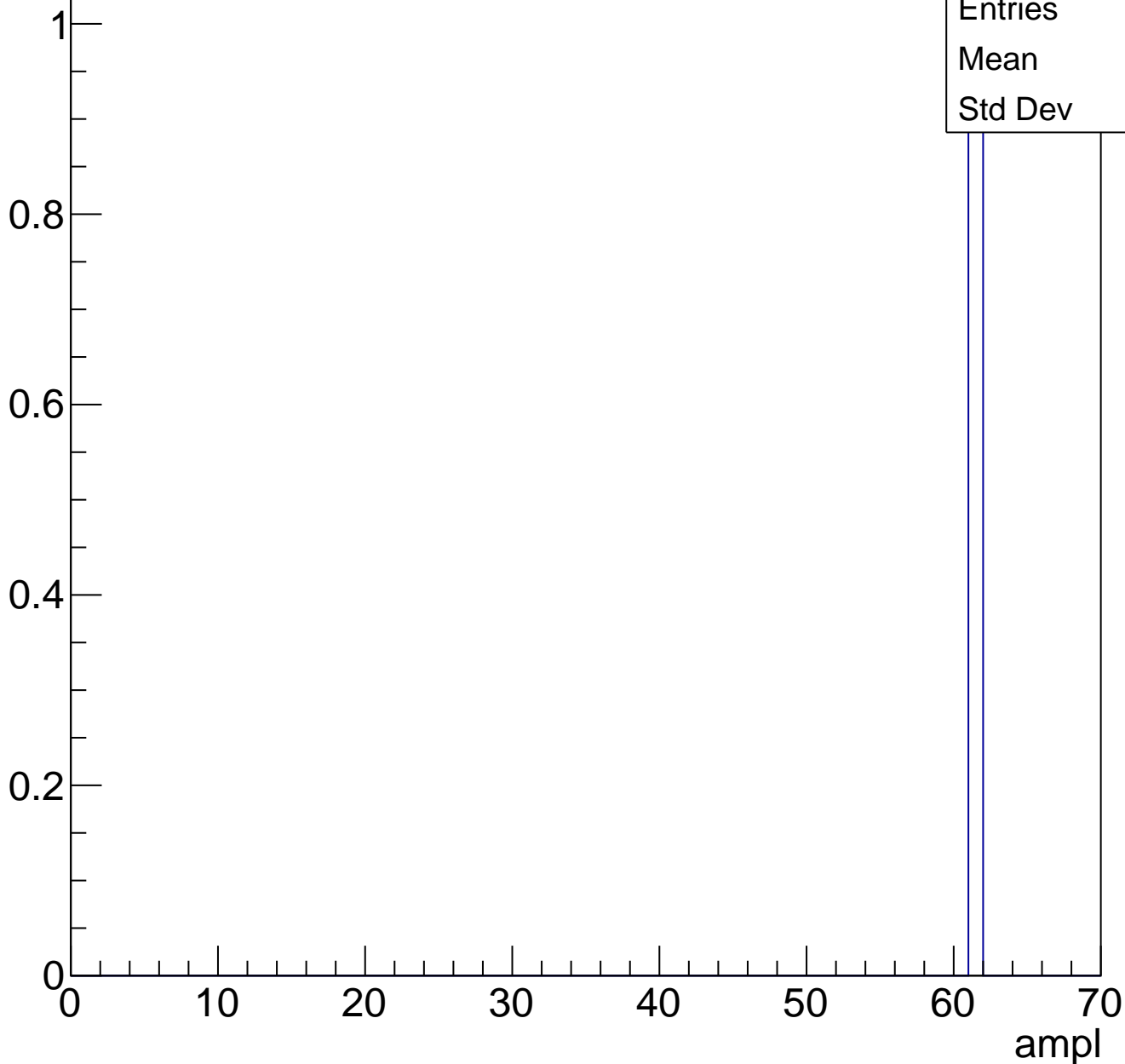
Entries	33
Mean	58.21
Std Dev	10.57



# B1L103S, U9-ch29, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U9-ch29, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L103S, U9-ch30, adc0

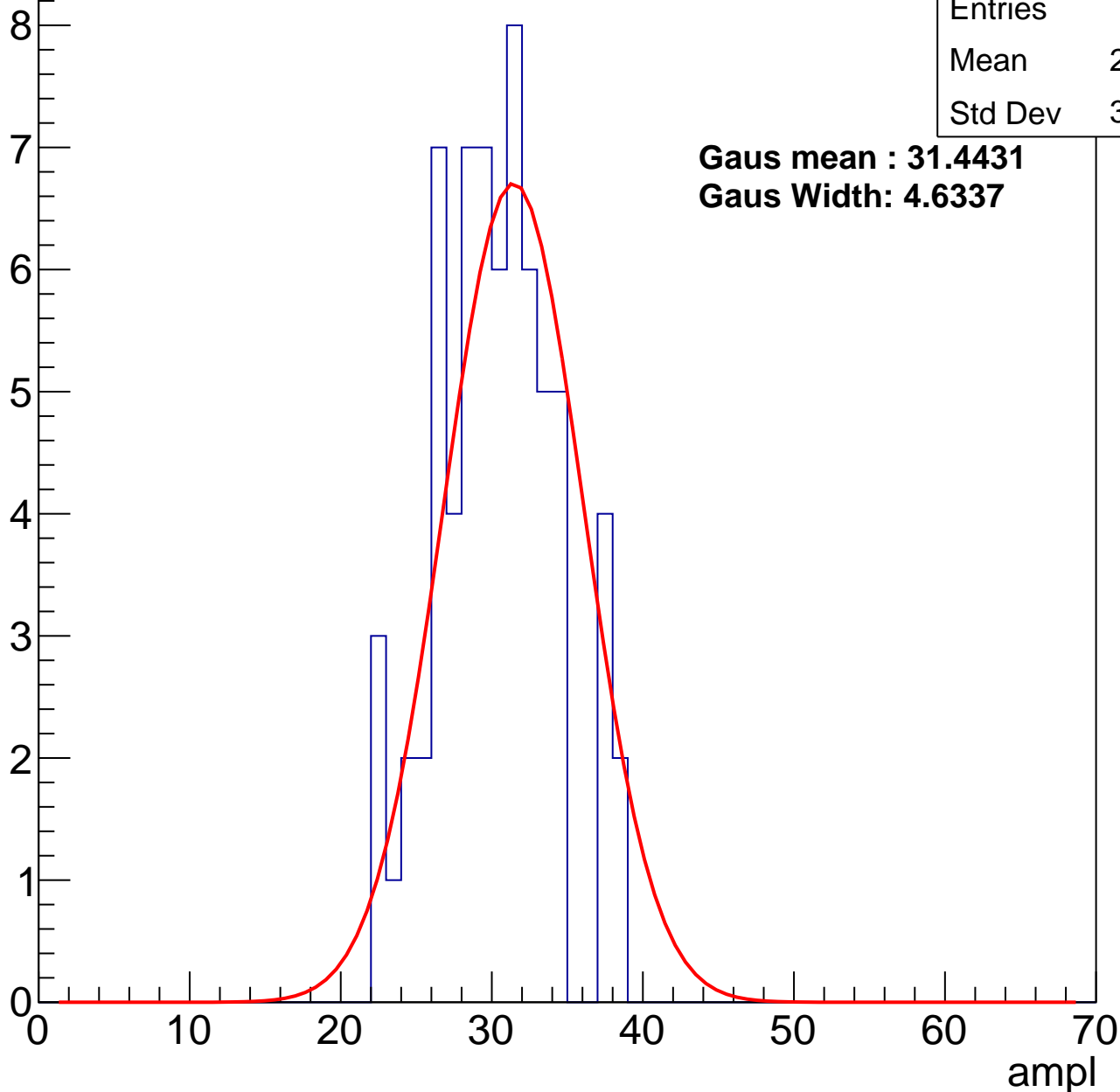
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	69
Mean	29.78
Std Dev	3.852

**Gaus mean : 31.4431**

**Gaus Width: 4.6337**



# B1L103S, U9-ch30, adc1

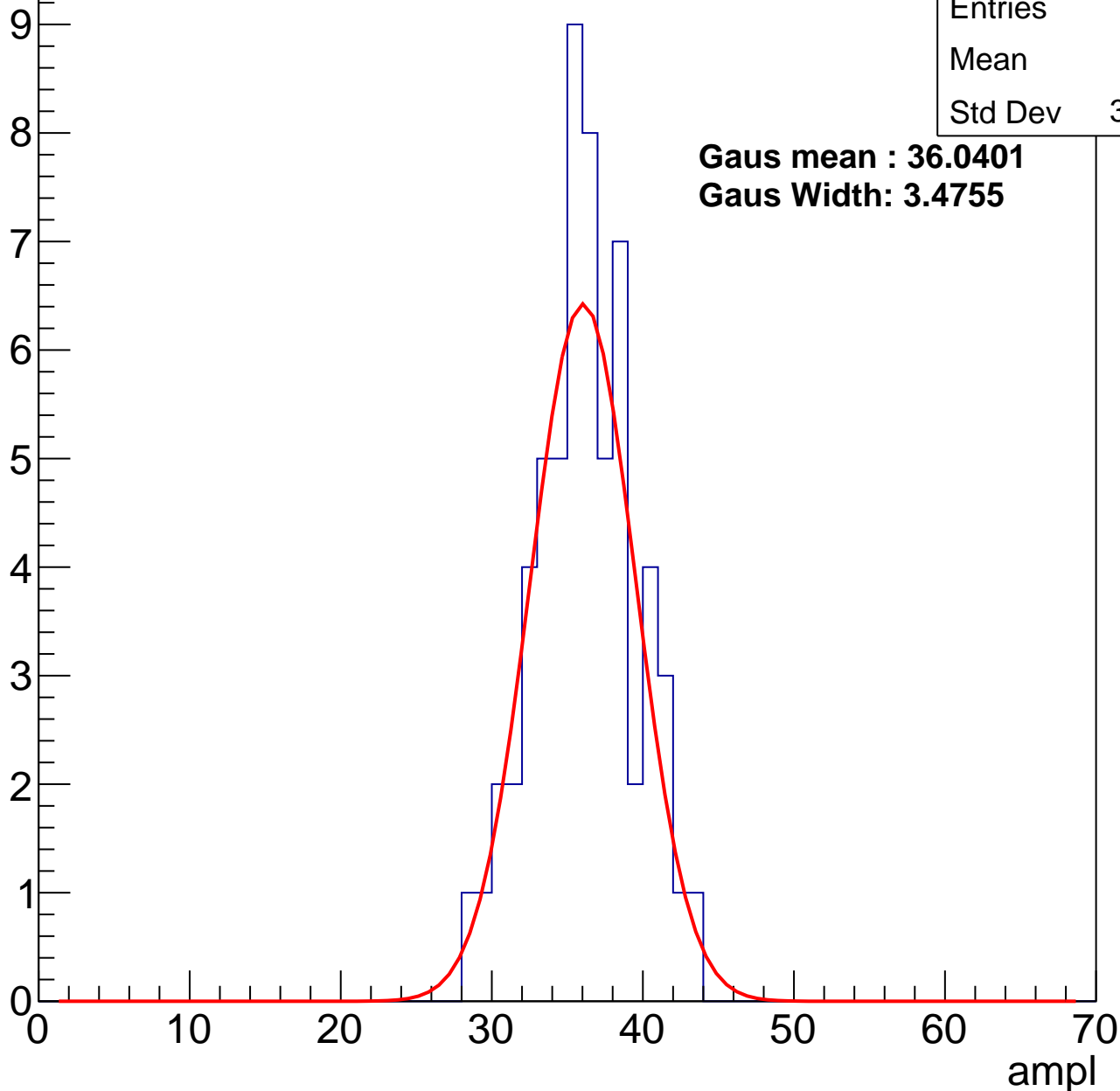
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	60
Mean	35.7
Std Dev	3.273

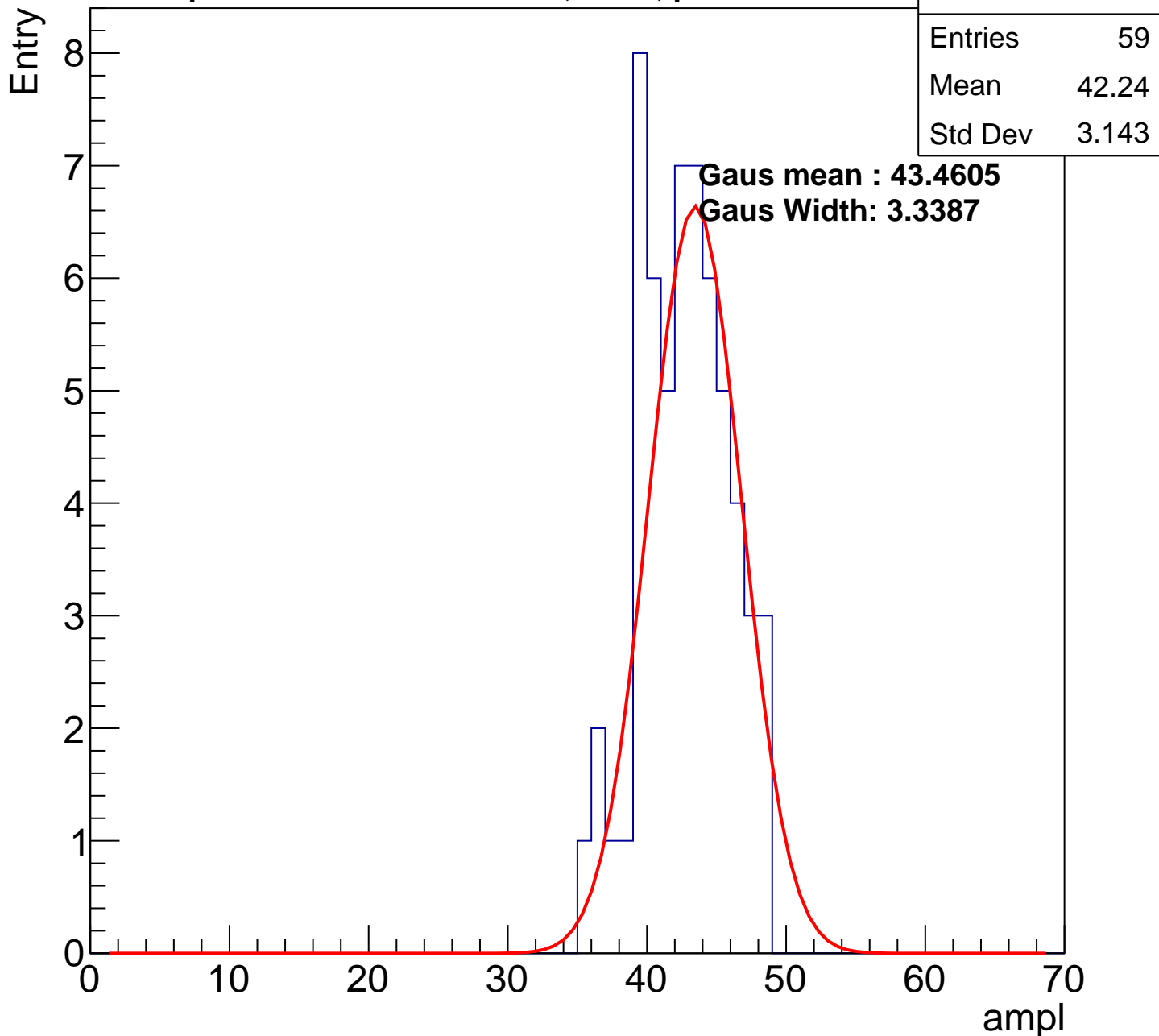
**Gaus mean : 36.0401**

**Gaus Width: 3.4755**



# B1L103S, U9-ch30, adc2

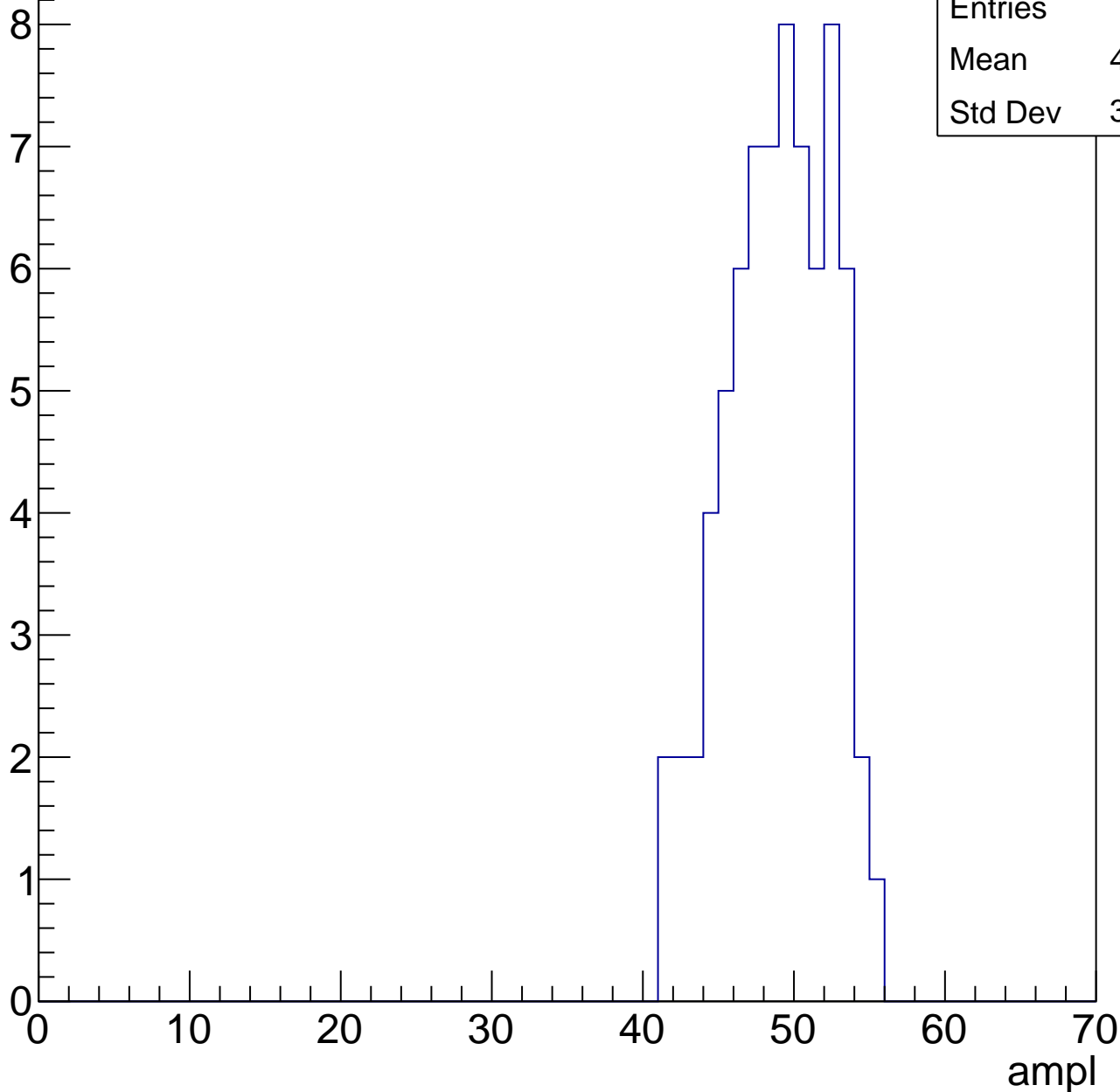
calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U9-ch30, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

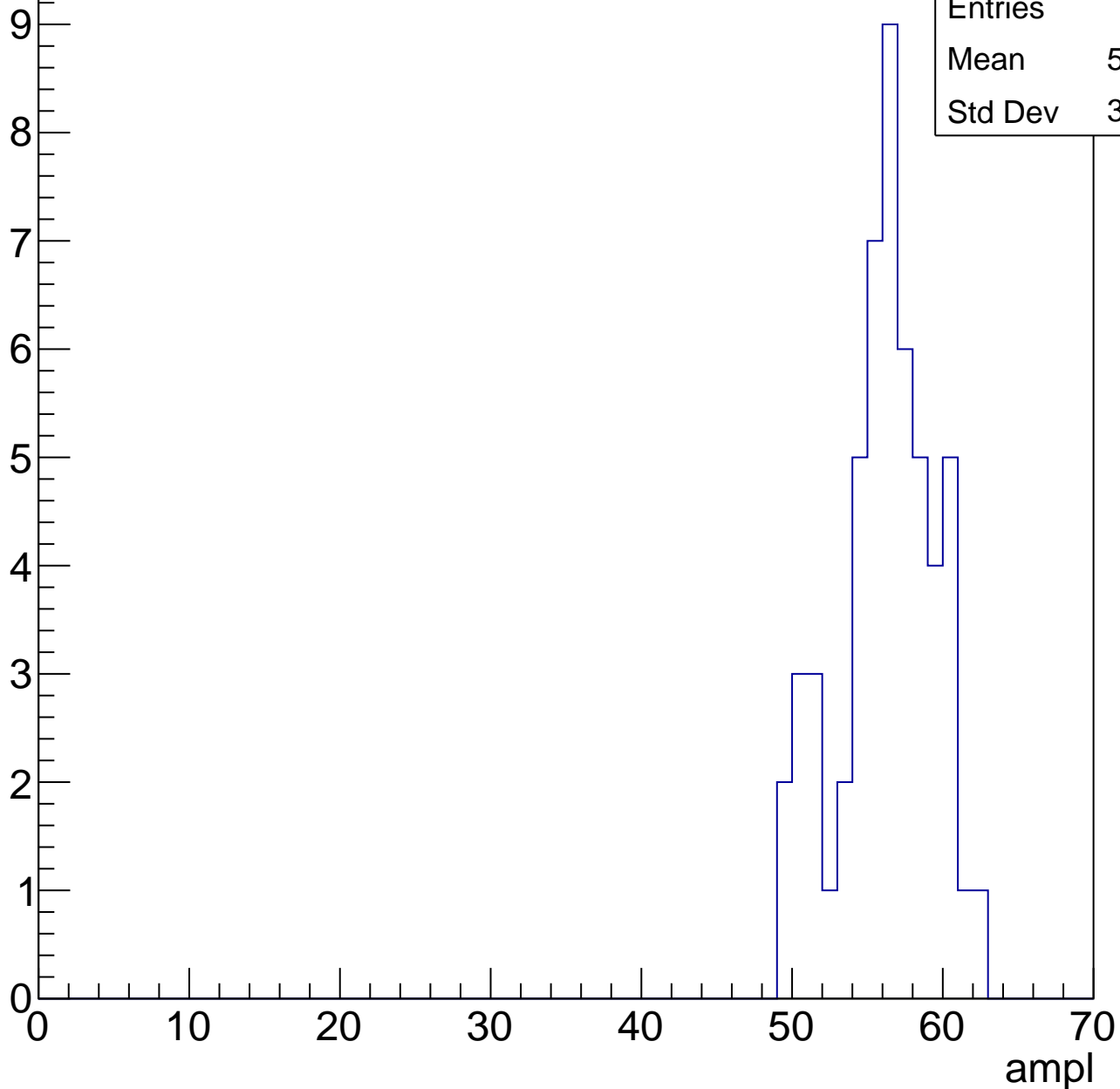


Entries	73
Mean	48.48
Std Dev	3.376

# B1L103S, U9-ch30, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

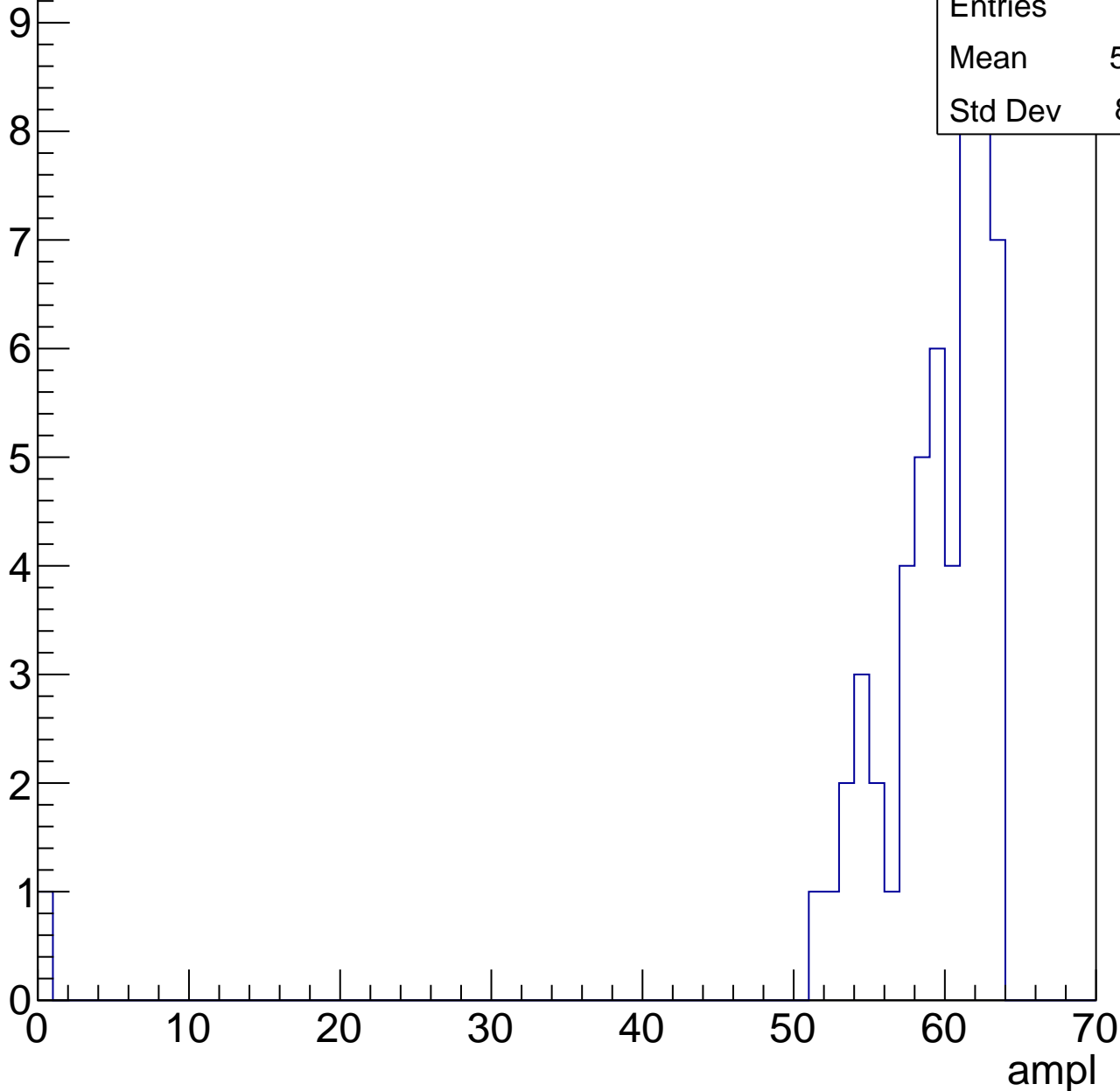


# B1L103S, U9-ch30, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	54
Mean	58.07
Std Dev	8.591



# B1L103S, U9-ch30, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U9-ch30, adc7

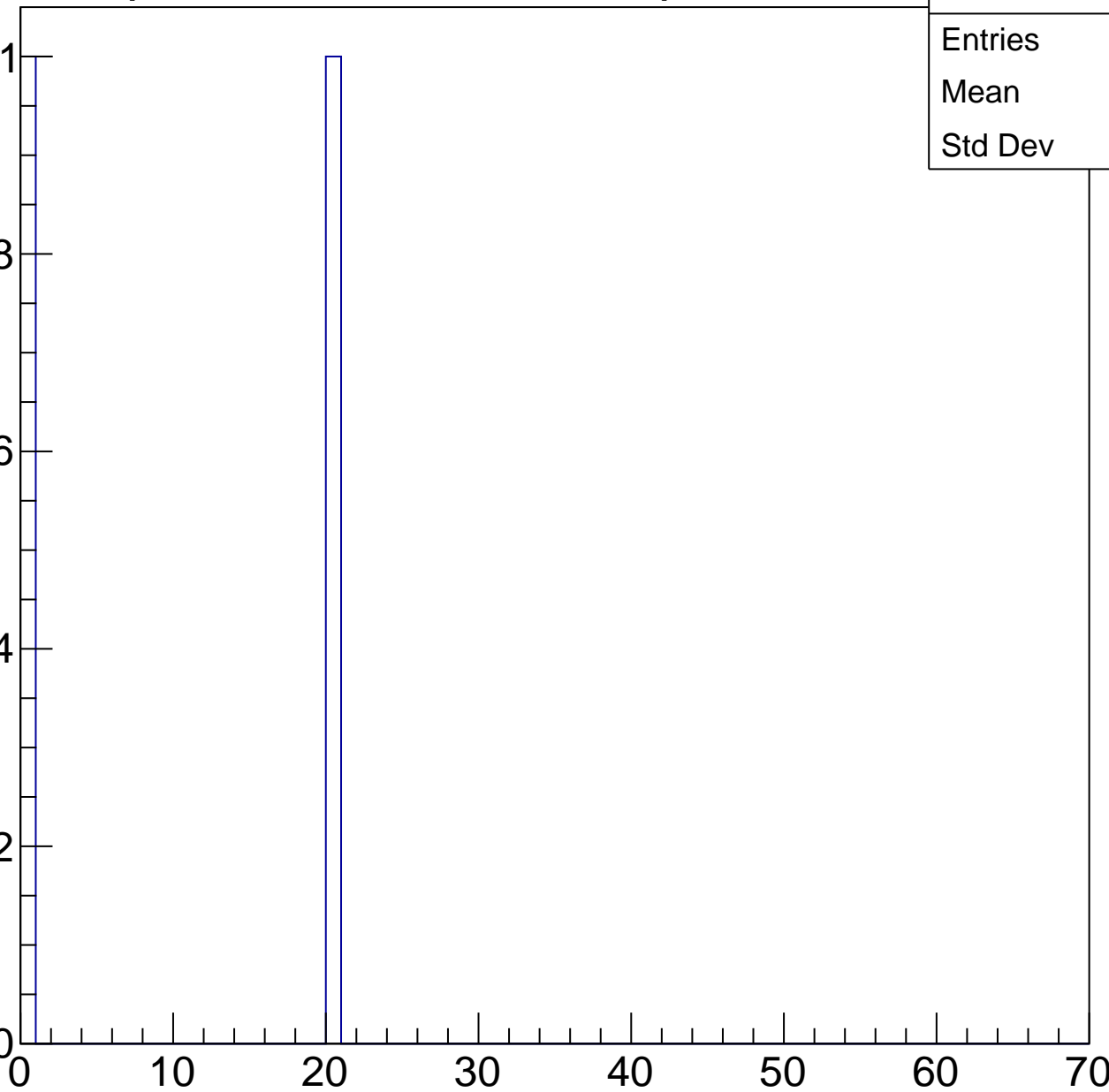
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

1  
0.8  
0.6  
0.4  
0.2  
0

Entries	2
Mean	10
Std Dev	10

ampl



# B1L103S, U9-ch31, adc0

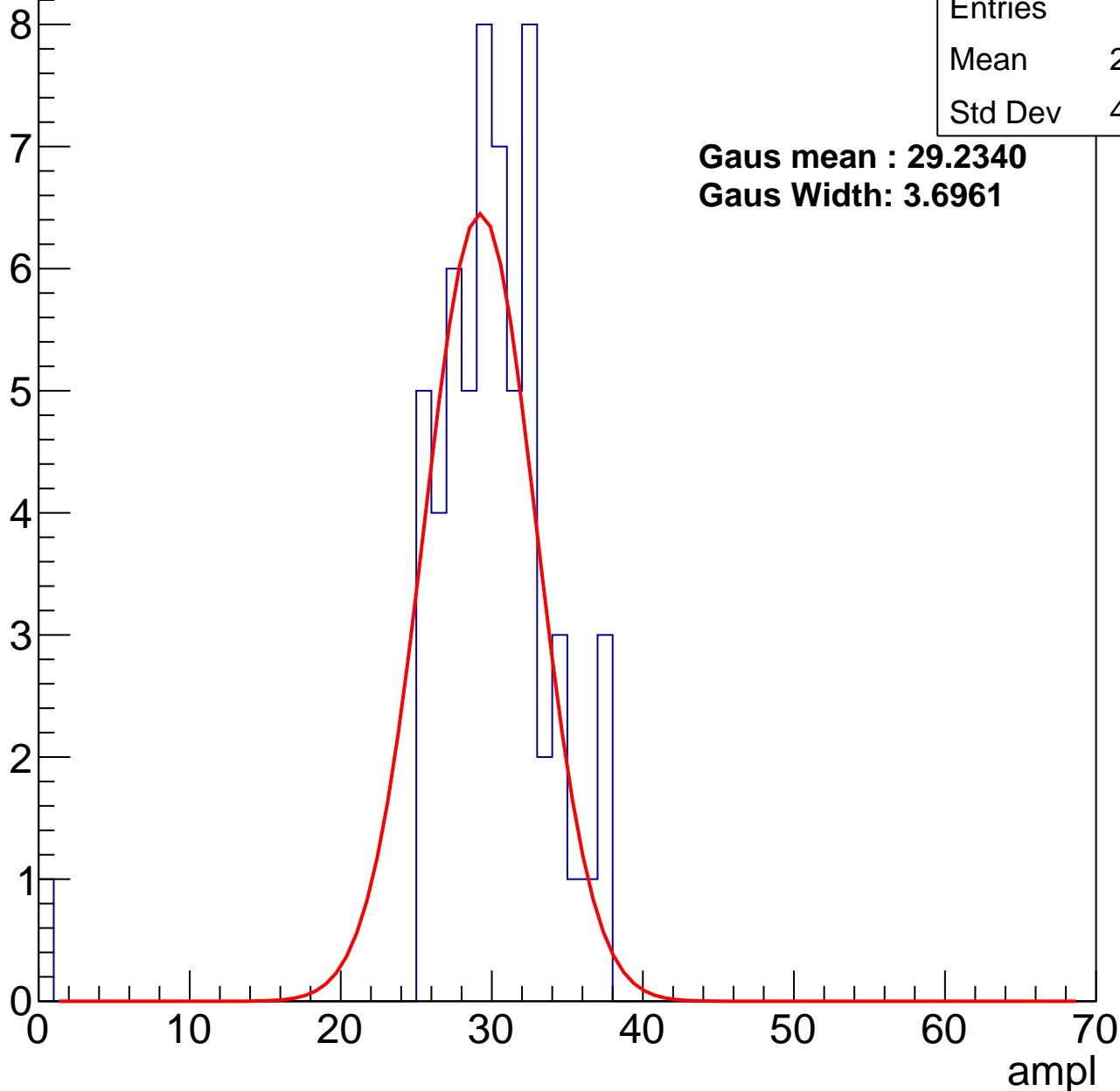
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	59
Mean	29.39
Std Dev	4.975

**Gaus mean : 29.2340**

**Gaus Width: 3.6961**



# B1L103S, U9-ch31, adc1

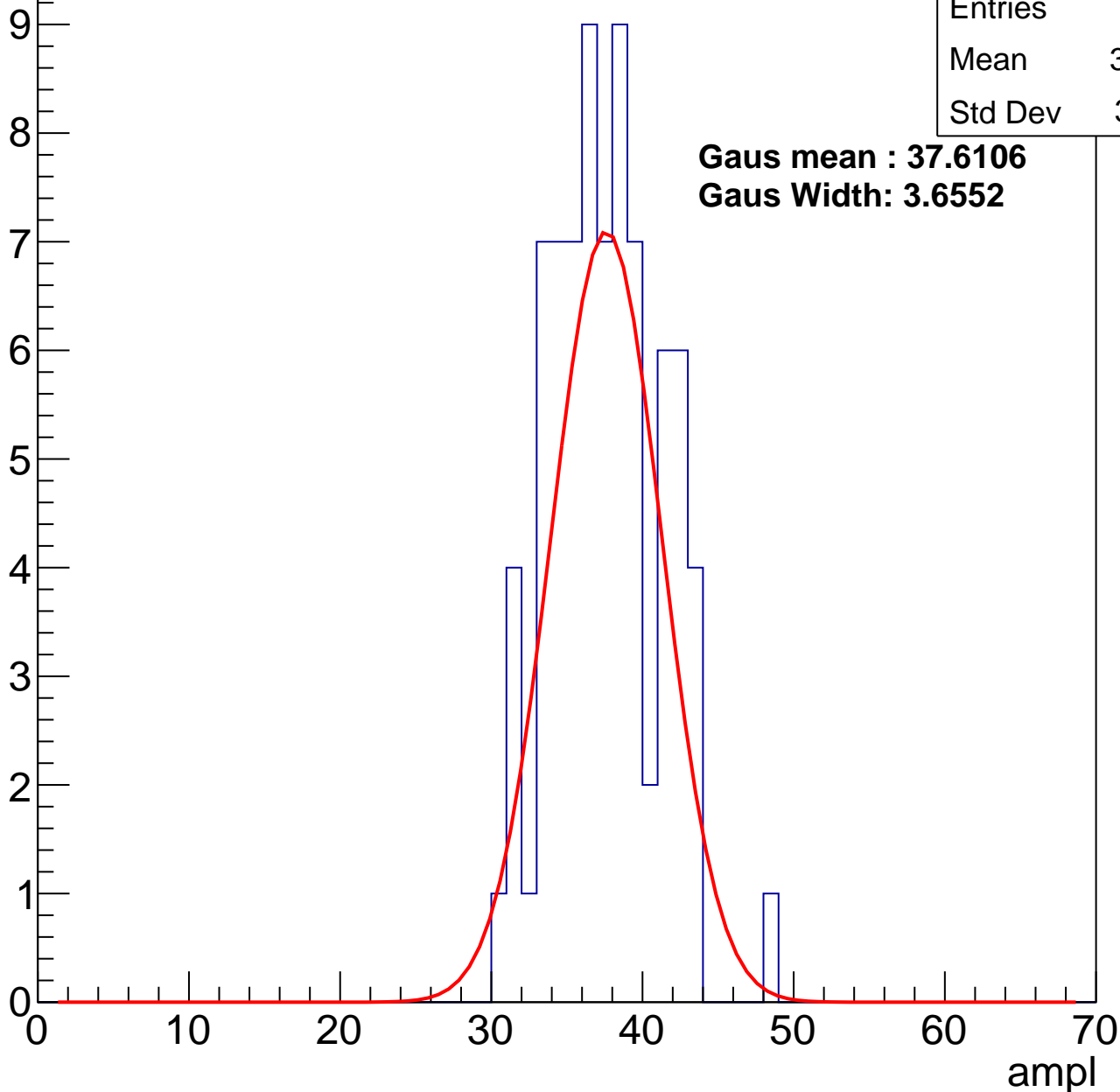
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	78
Mean	37.13
Std Dev	3.571

**Gaus mean : 37.6106**

**Gaus Width: 3.6552**



# B1L103S, U9-ch31, adc2

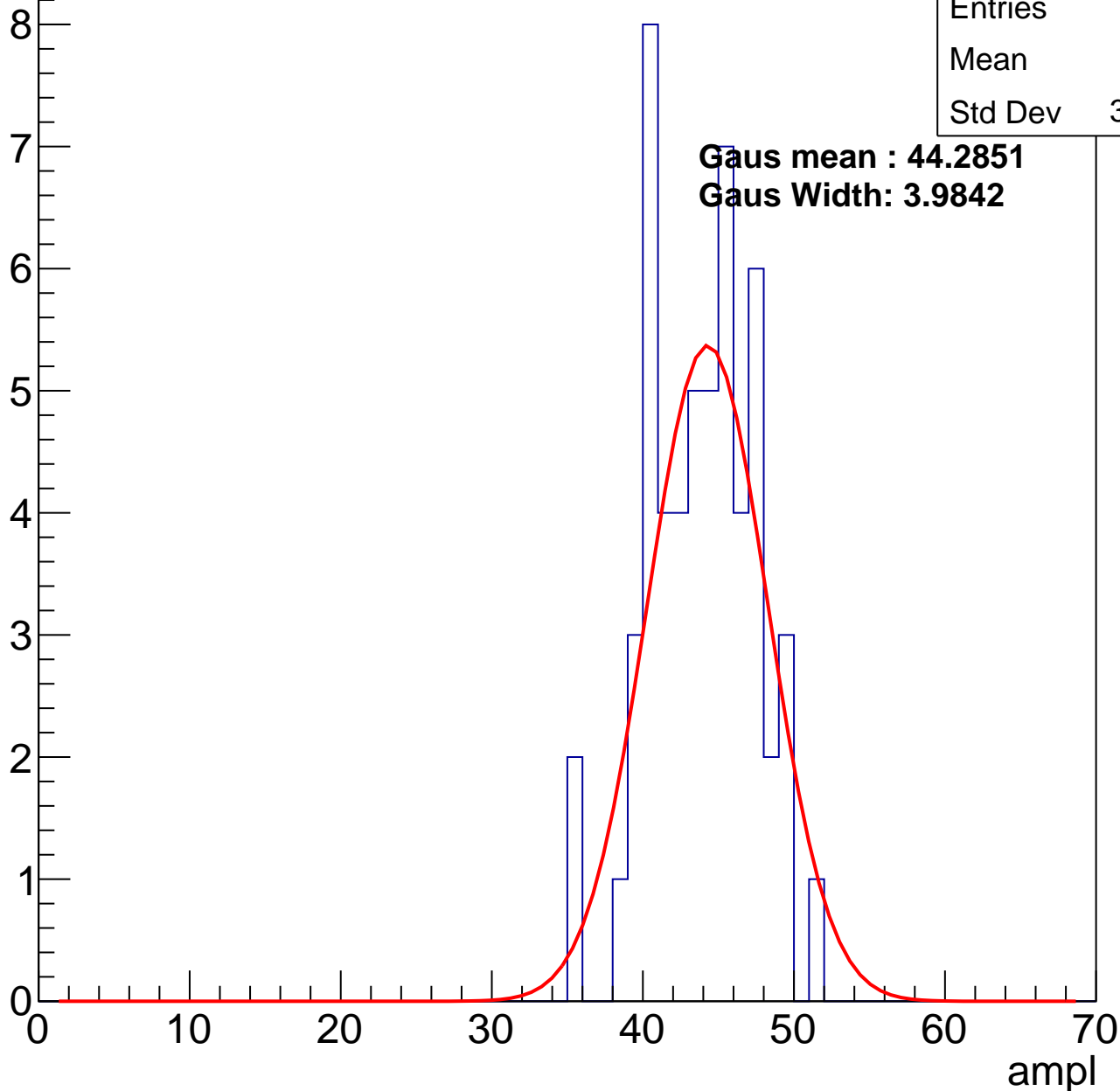
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	55
Mean	43.4
Std Dev	3.493

**Gaus mean : 44.2851**

**Gaus Width: 3.9842**

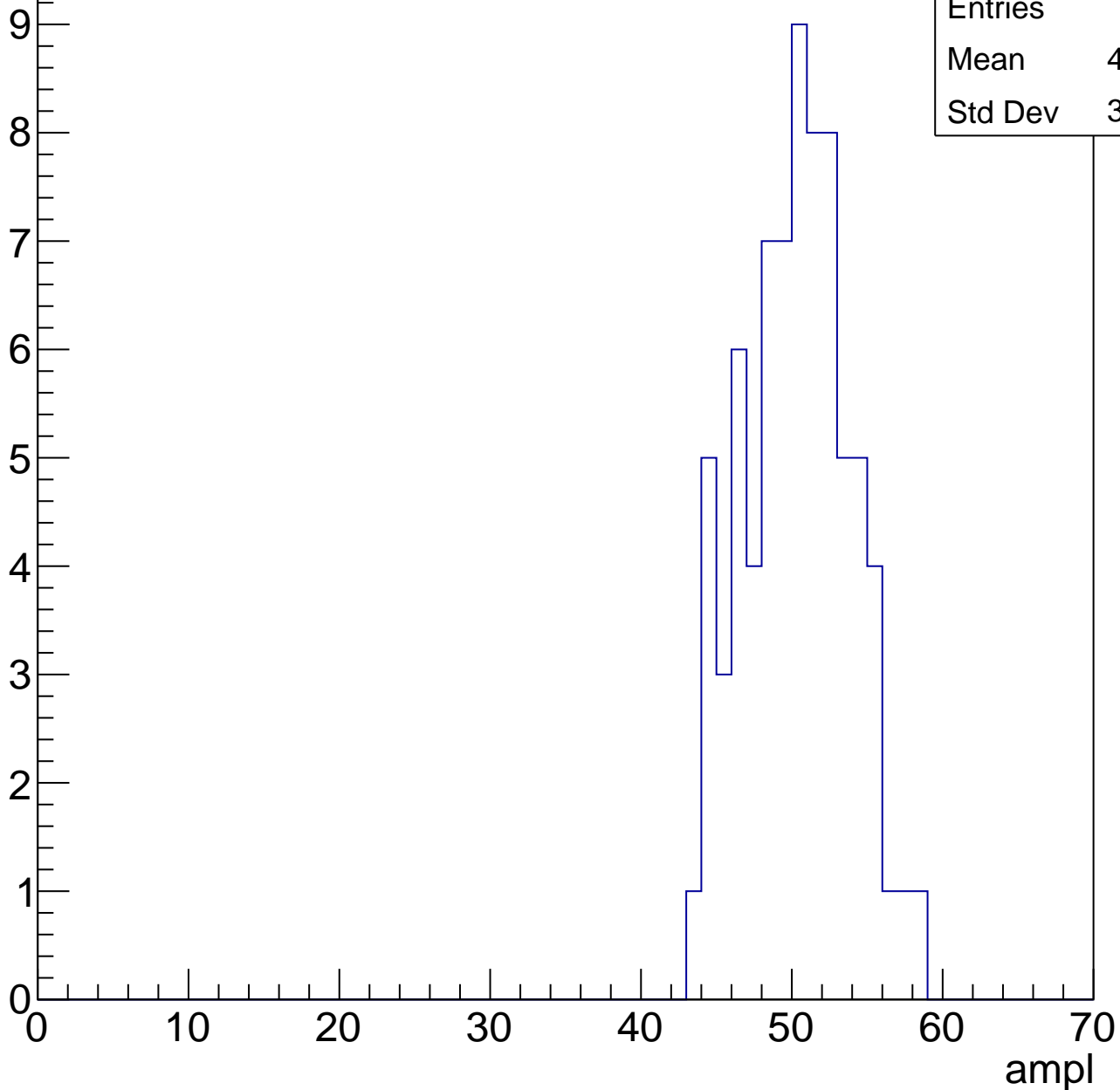


# B1L103S, U9-ch31, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

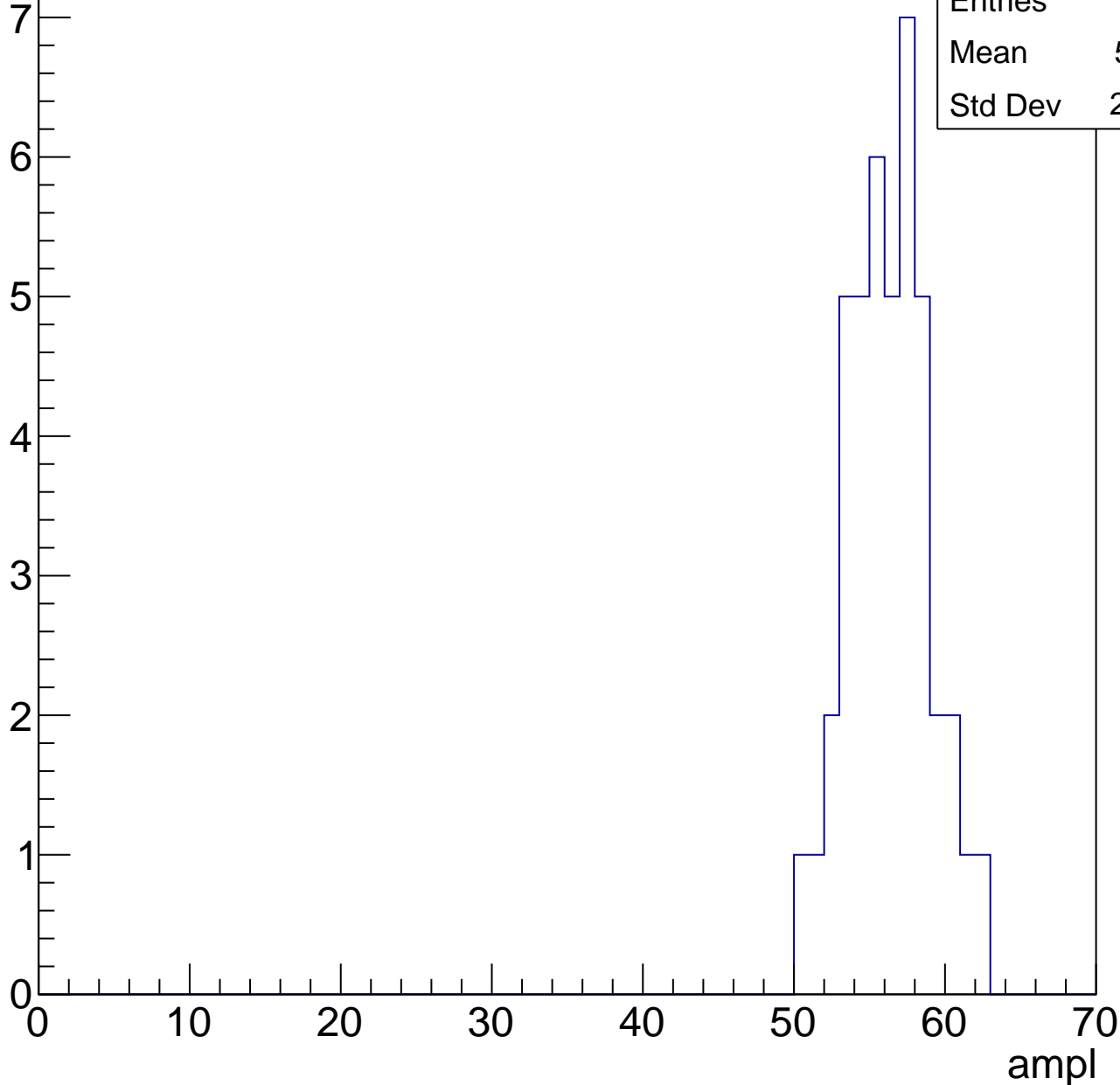
Entries	75
Mean	49.88
Std Dev	3.433



# B1L103S, U9-ch31, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

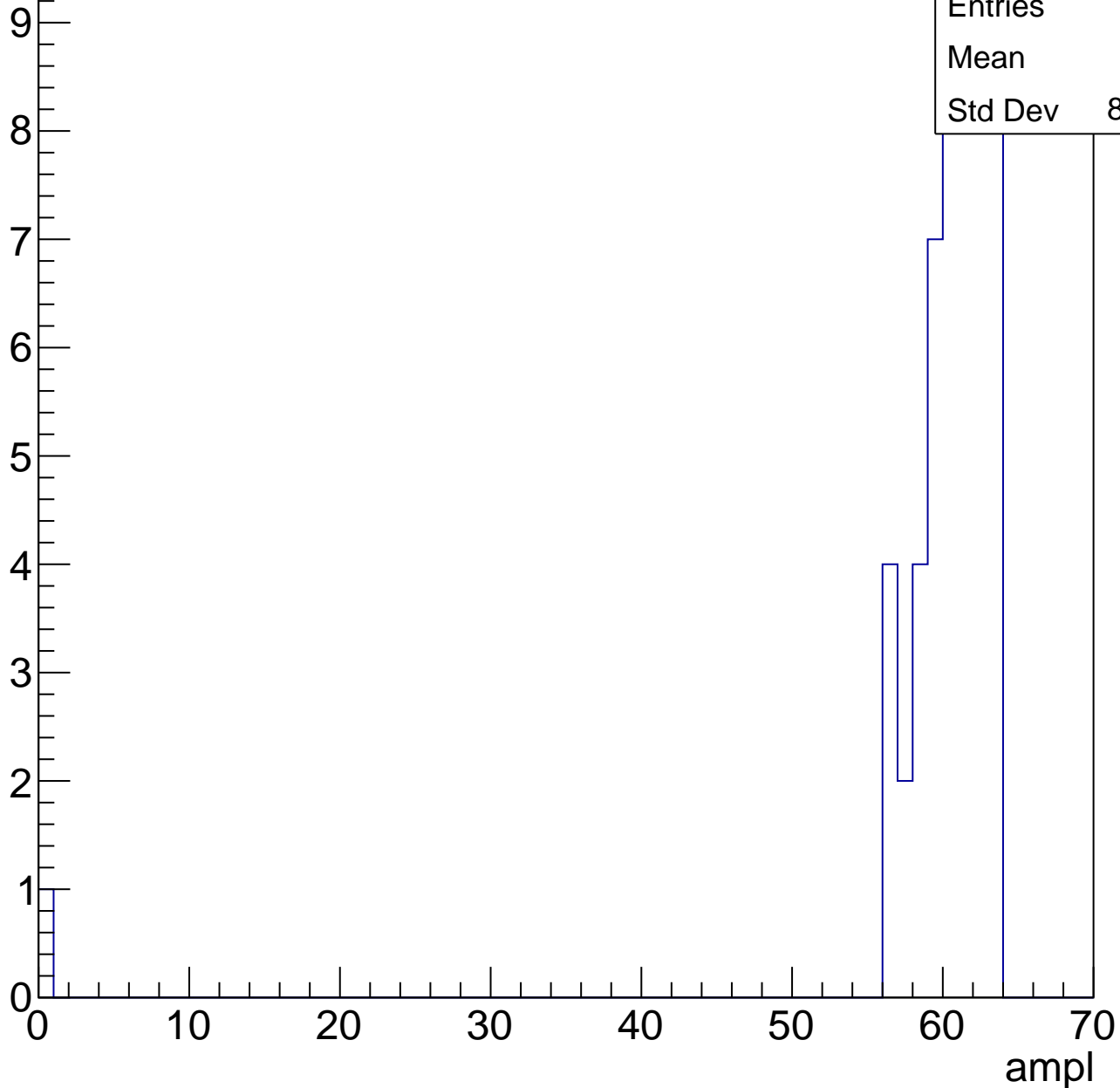
Entry



# B1L103S, U9-ch31, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

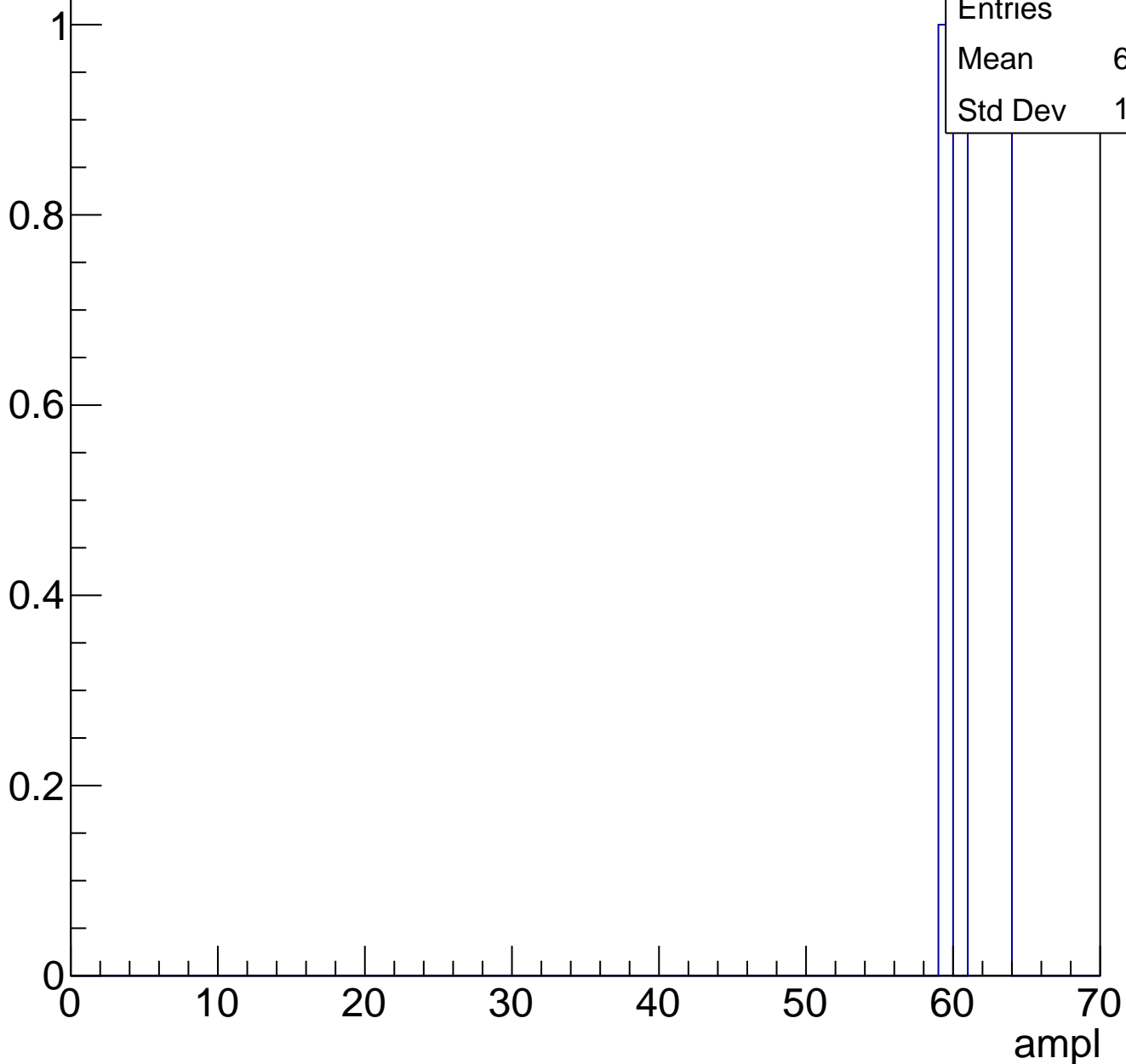


Entries	51
Mean	59.1
Std Dev	8.614

# B1L103S, U9-ch31, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

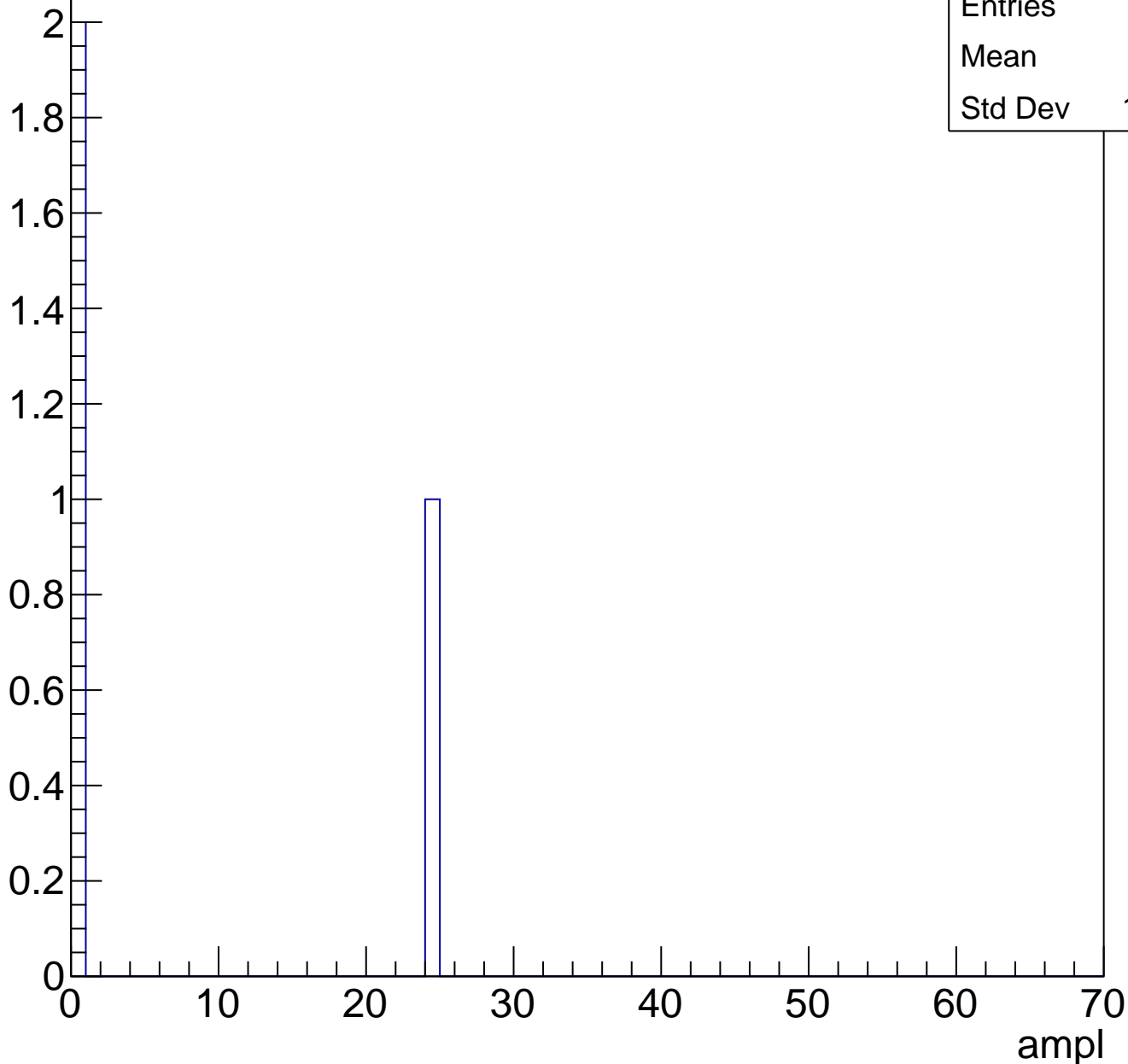




# B1L103S, U9-ch31, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U9-ch32, adc0

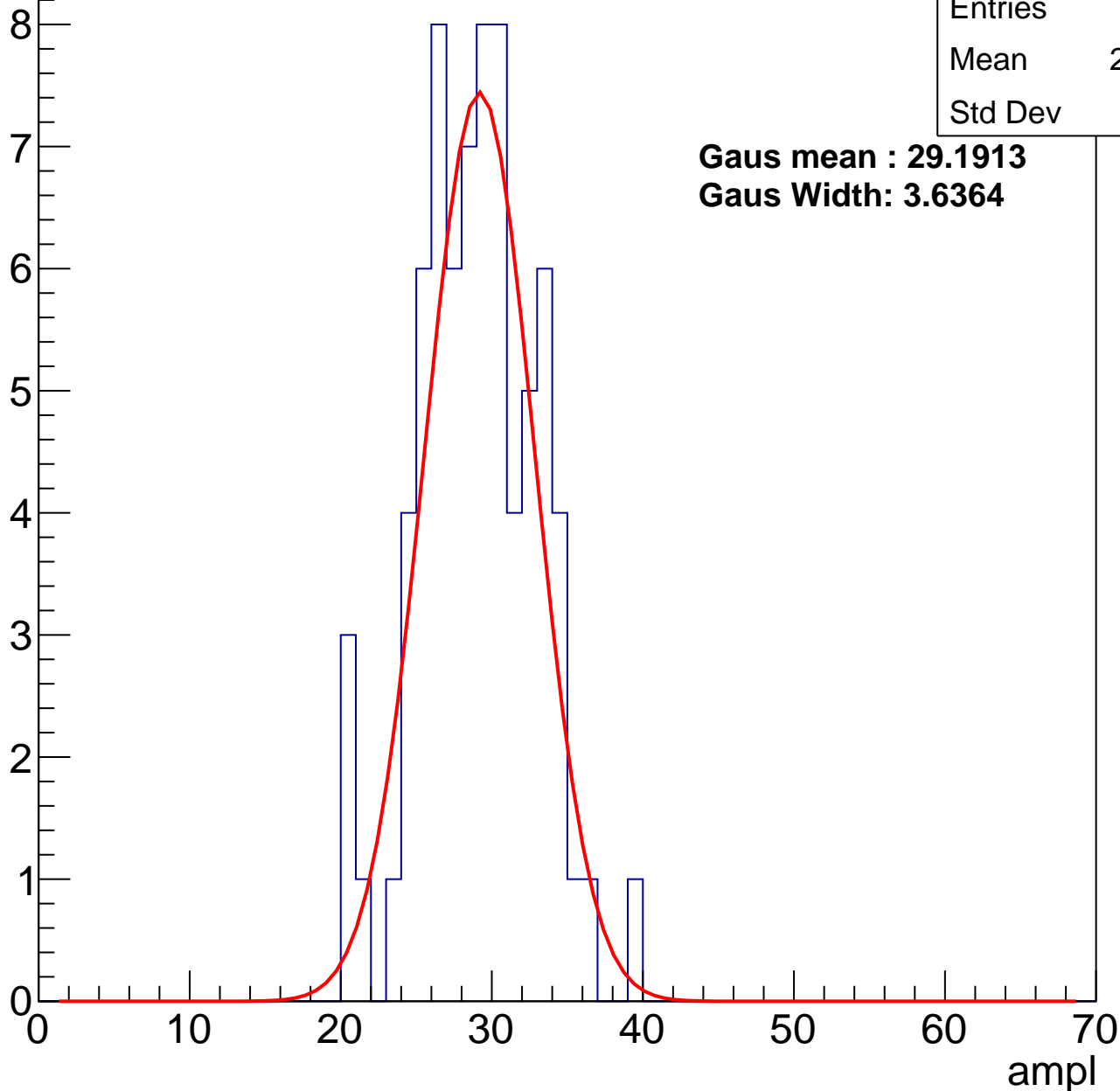
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	74
Mean	28.59
Std Dev	3.82

**Gaus mean : 29.1913**

**Gaus Width: 3.6364**



# B1L103S, U9-ch32, adc1

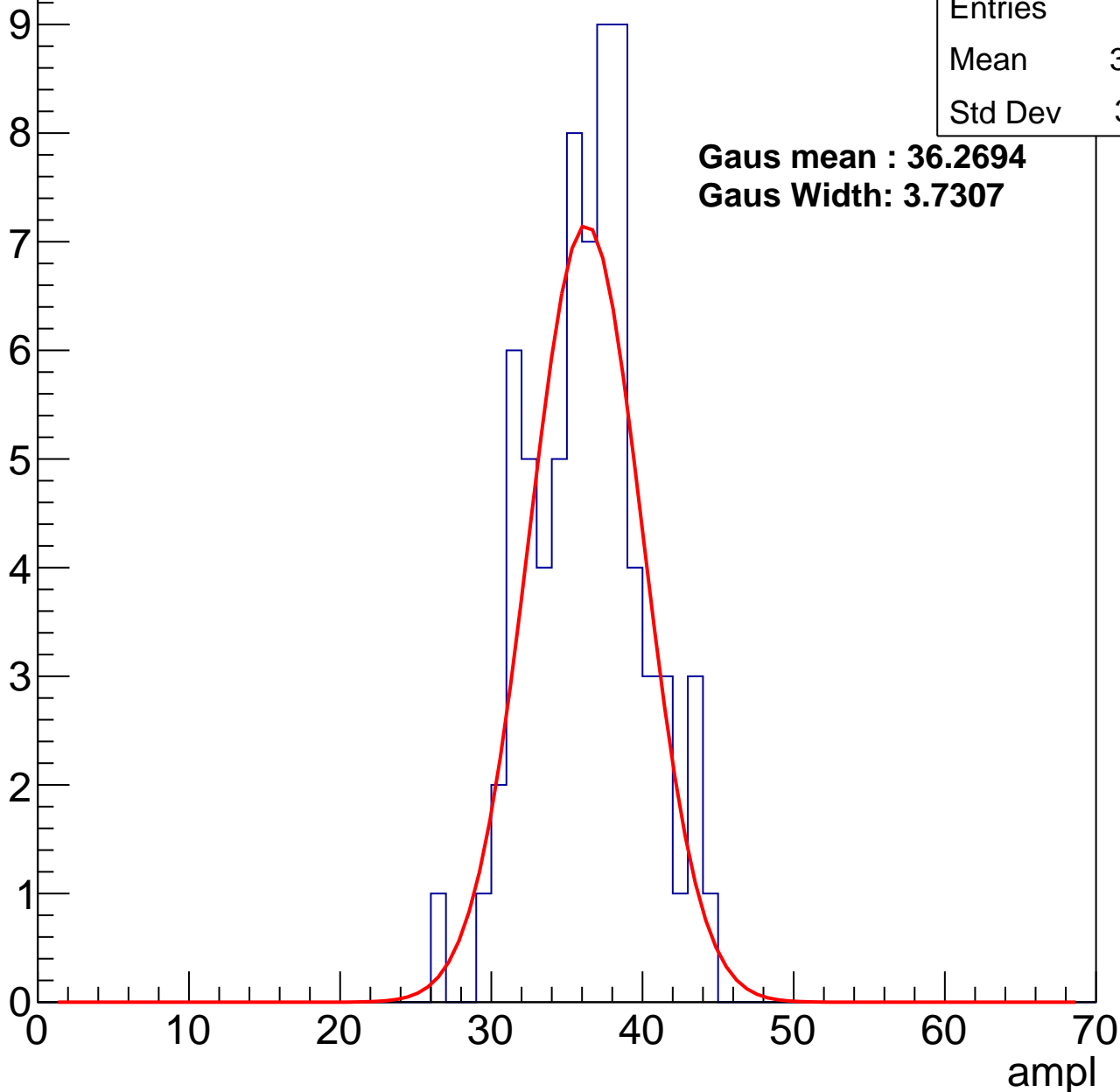
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	72
Mean	35.89
Std Dev	3.661

**Gaus mean : 36.2694**

**Gaus Width: 3.7307**



# B1L103S, U9-ch32, adc2

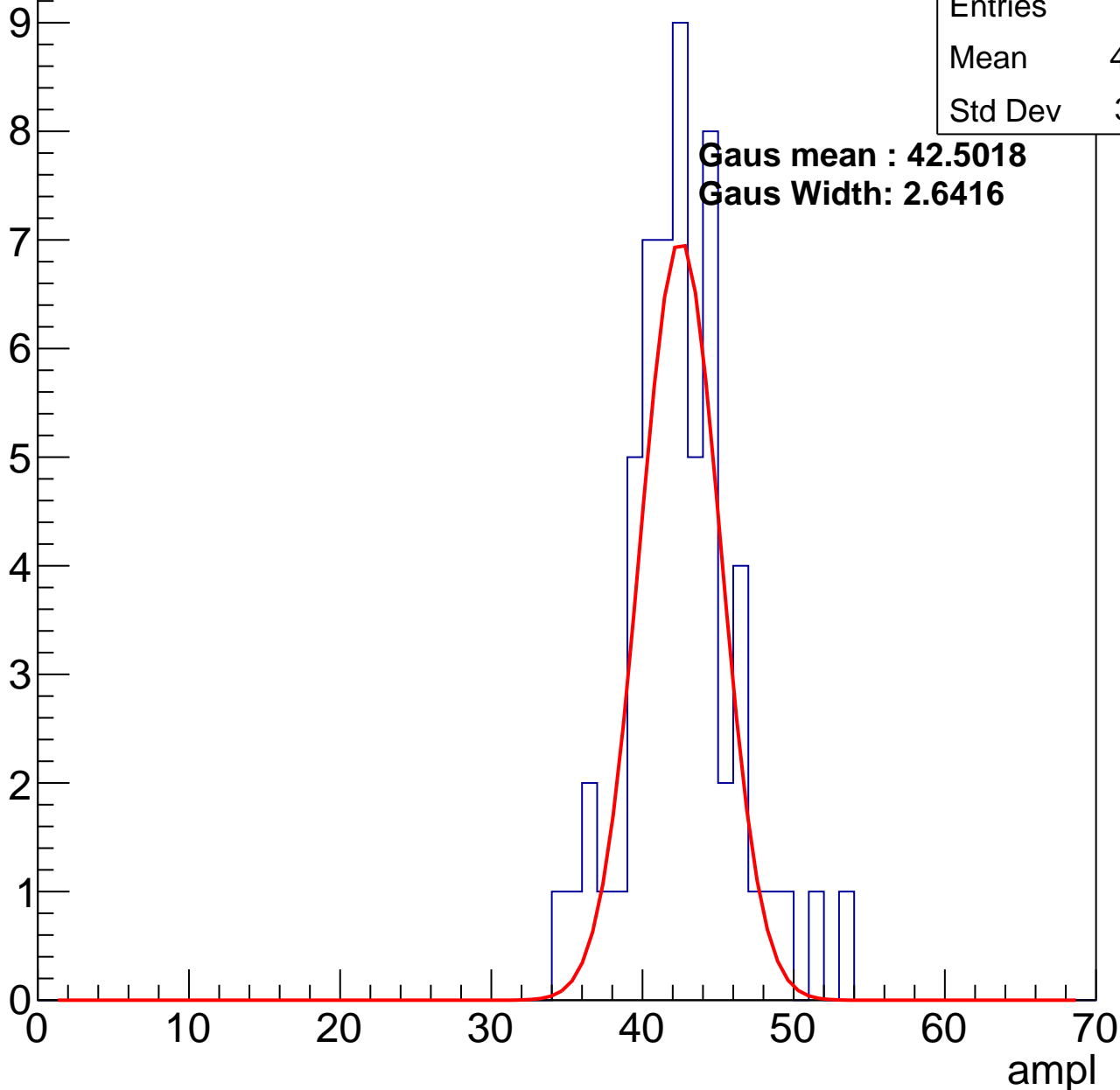
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	58
Mean	42.16
Std Dev	3.561

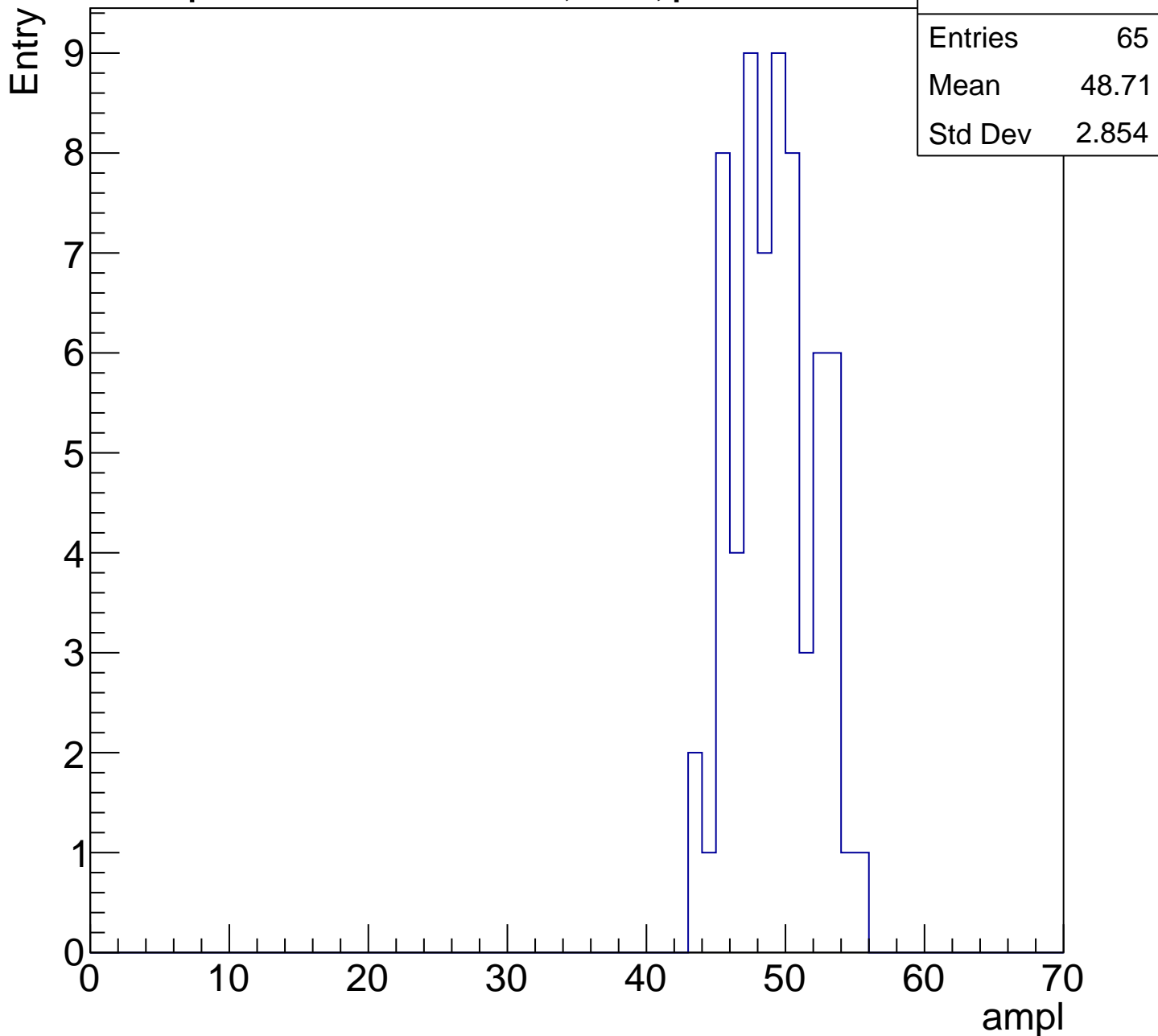
**Gaus mean : 42.5018**

**Gaus Width: 2.6416**



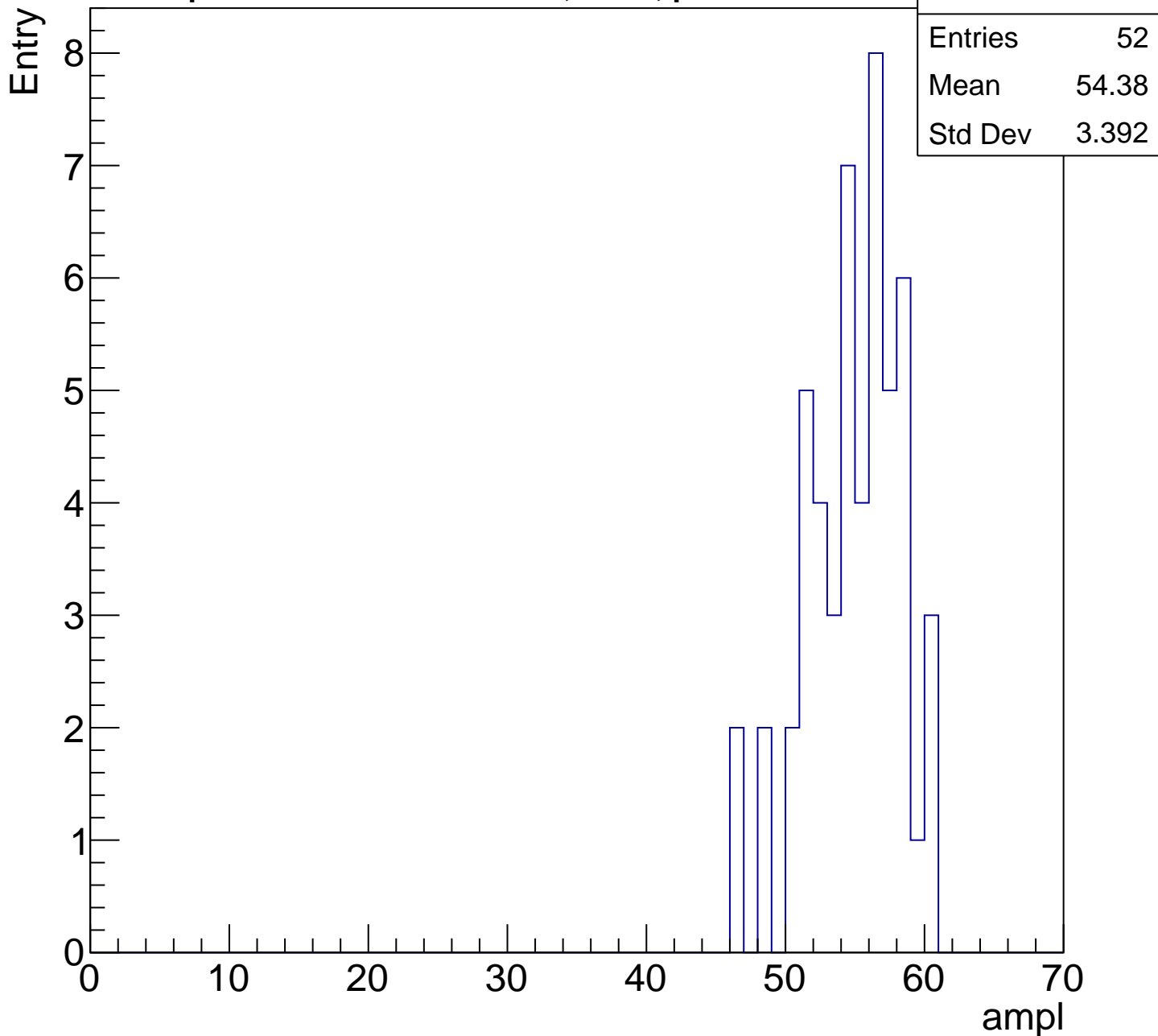
# B1L103S, U9-ch32, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U9-ch32, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U9-ch32, adc5

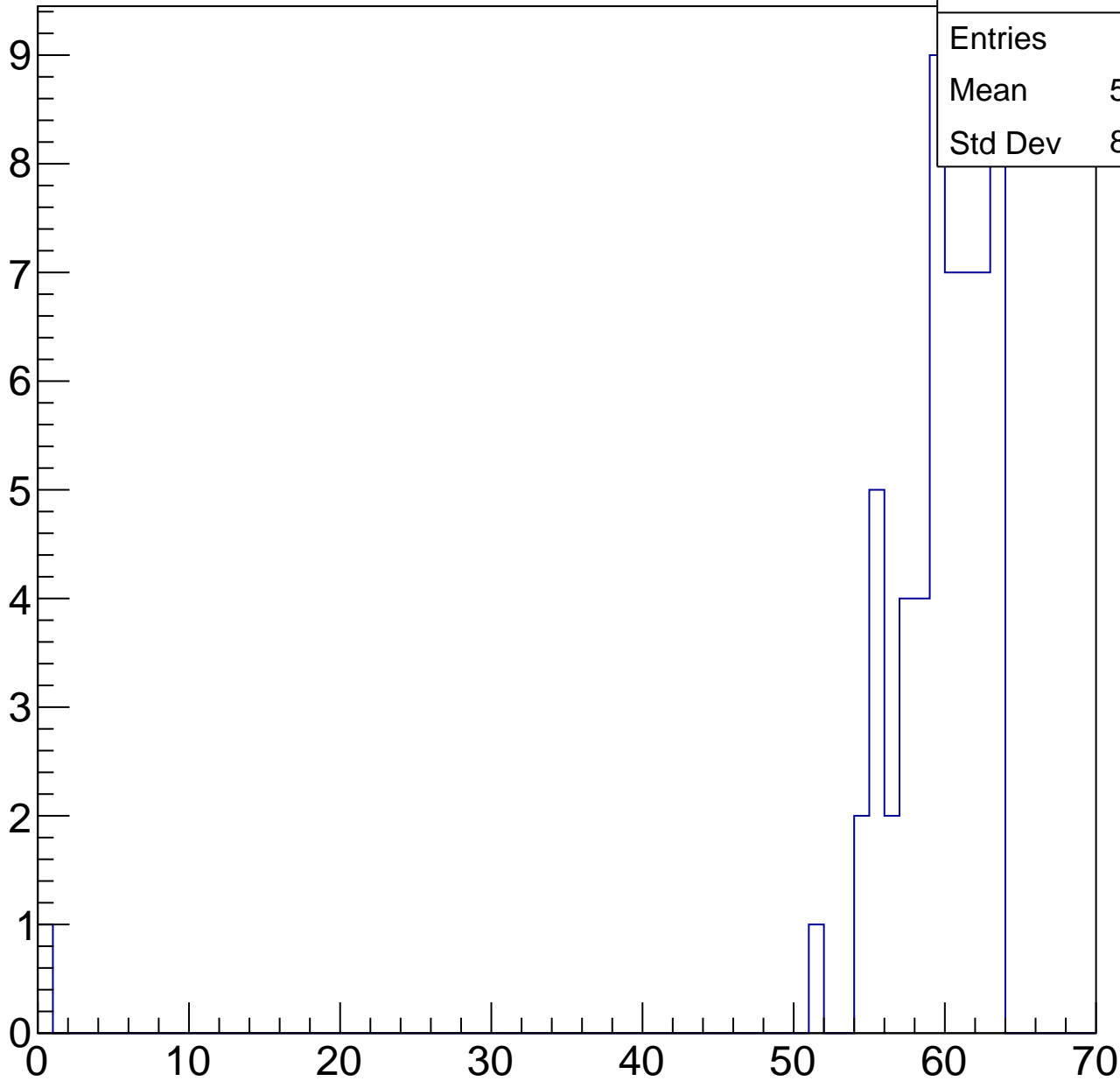
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	57
Mean	58.28
Std Dev	8.282

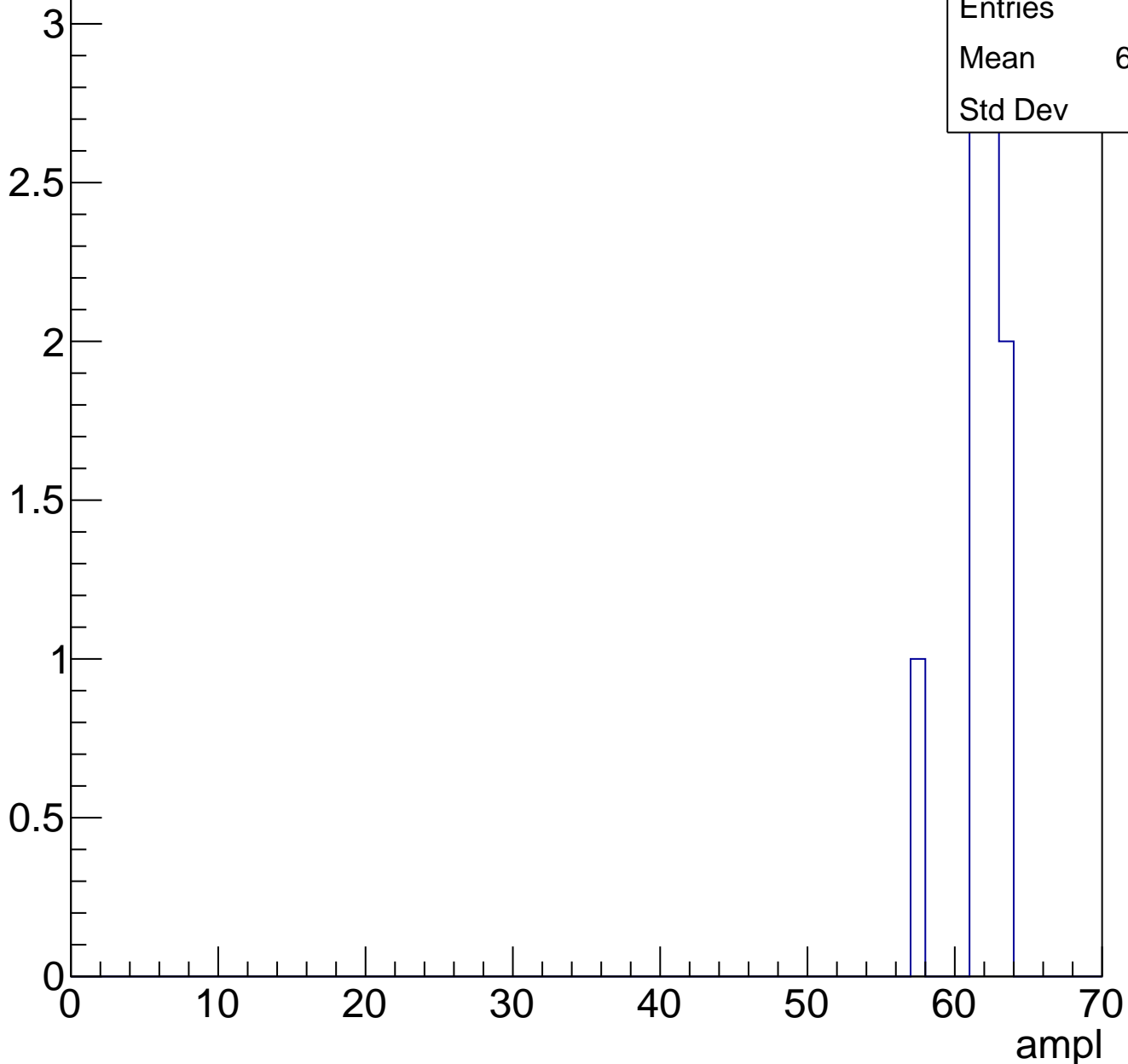
ampl



# B1L103S, U9-ch32, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U9-ch32, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U9-ch33, adc0

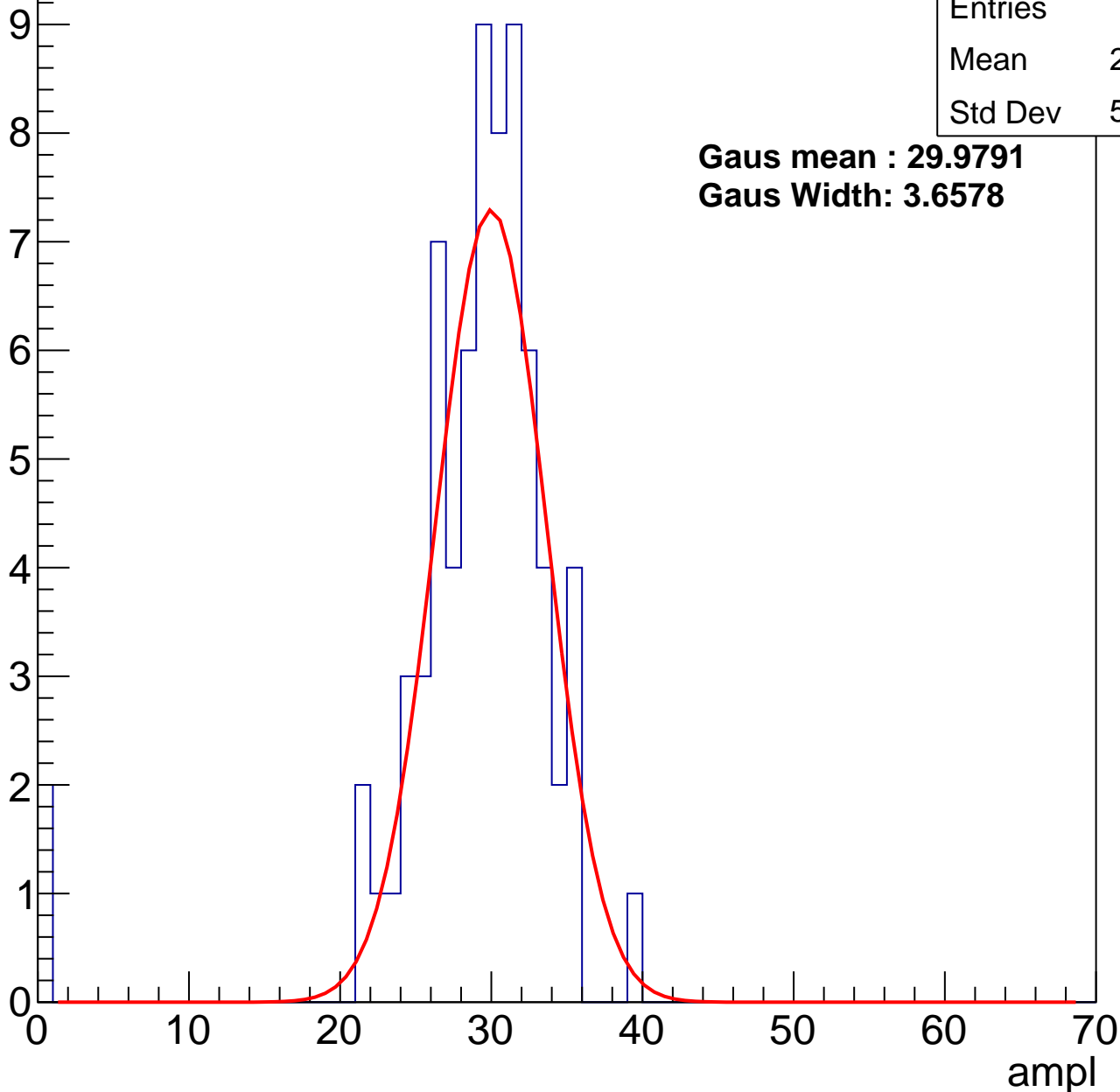
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	72
Mean	28.38
Std Dev	5.929

**Gaus mean : 29.9791**

**Gaus Width: 3.6578**



# B1L103S, U9-ch33, adc1

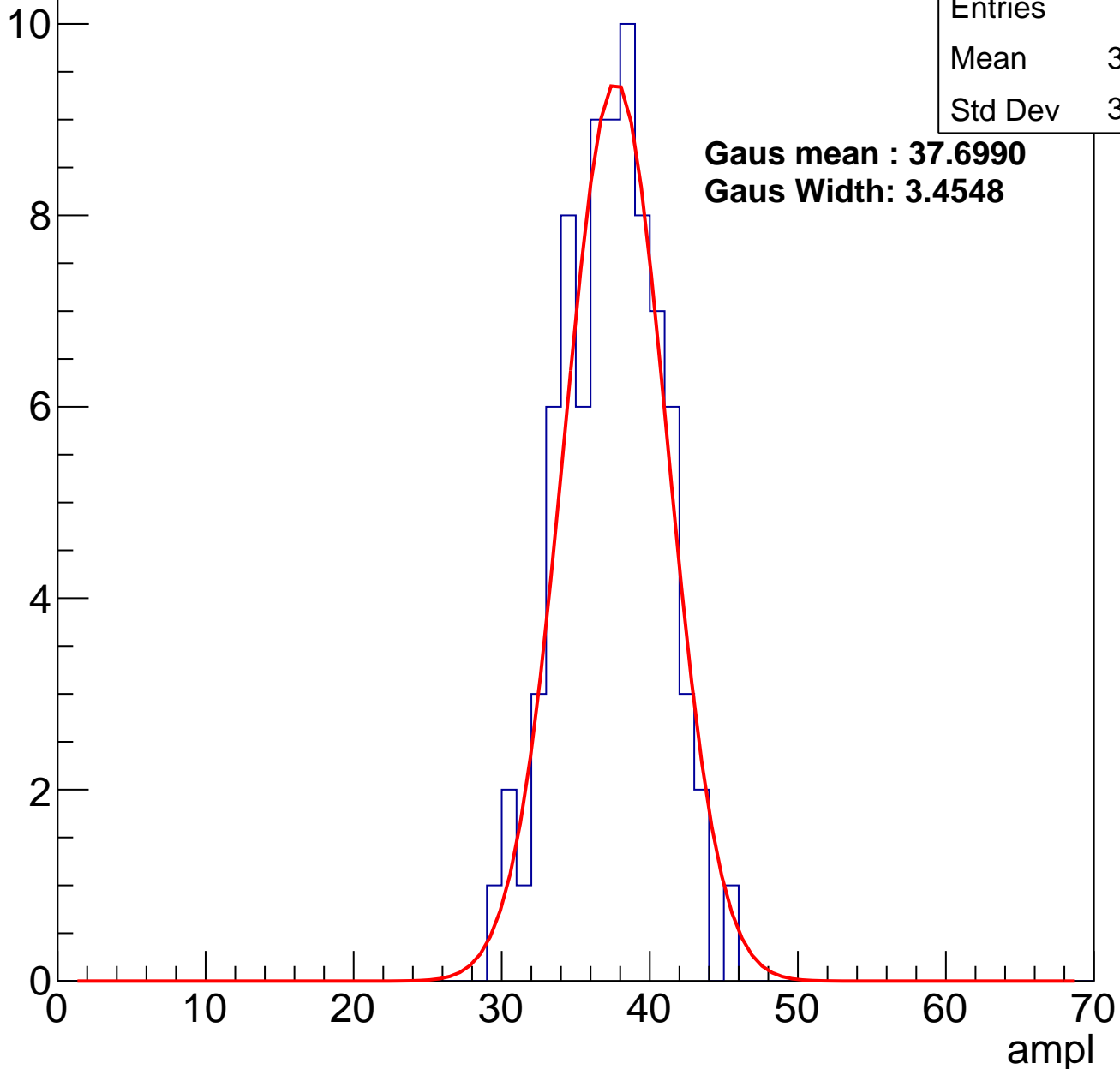
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	82
Mean	36.93
Std Dev	3.286

**Gaus mean : 37.6990**

**Gaus Width: 3.4548**

Entry



# B1L103S, U9-ch33, adc2

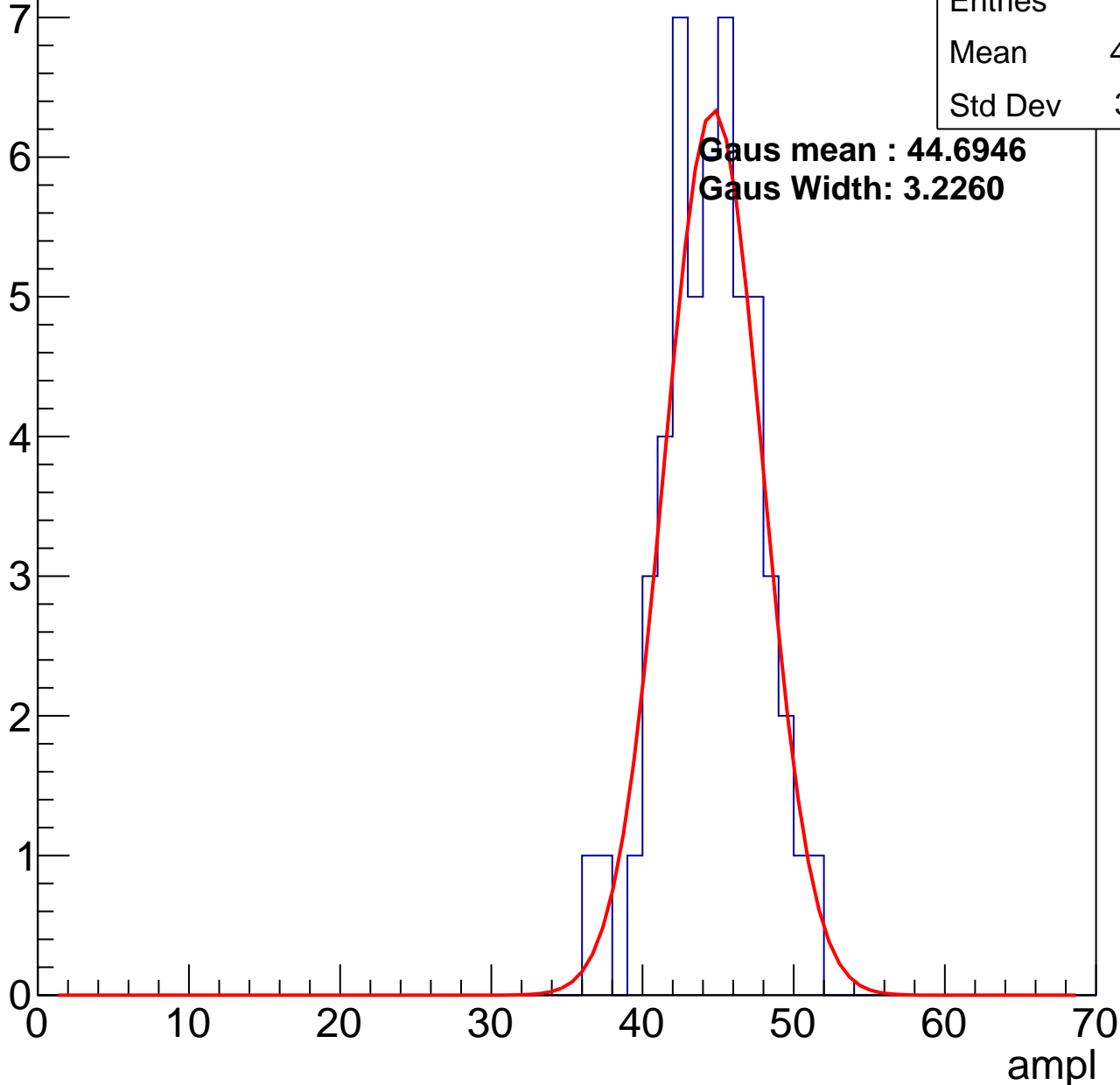
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	52
Mean	44.08
Std Dev	3.131

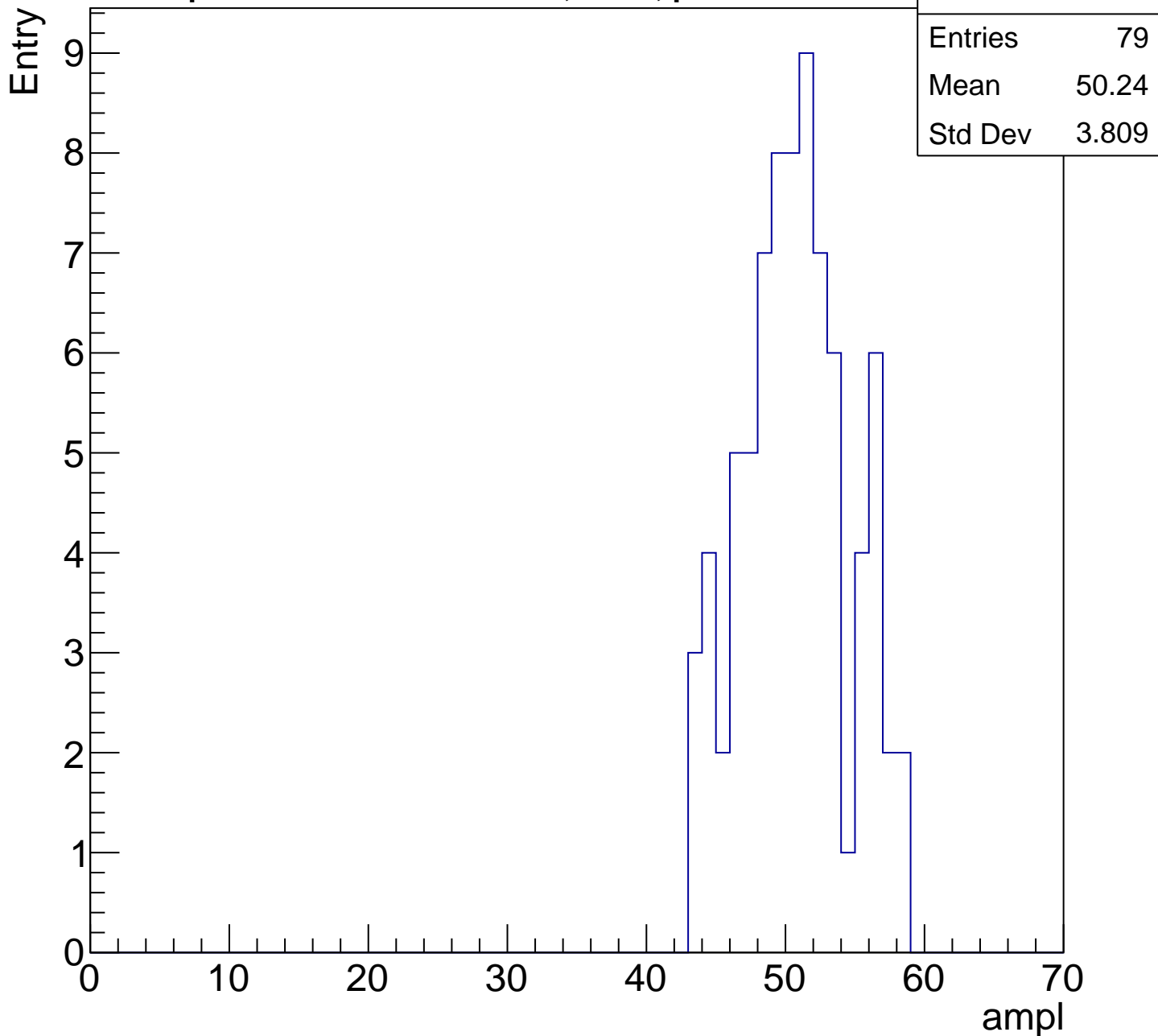
**Gaus mean : 44.6946**

**Gaus Width: 3.2260**



# B1L103S, U9-ch33, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

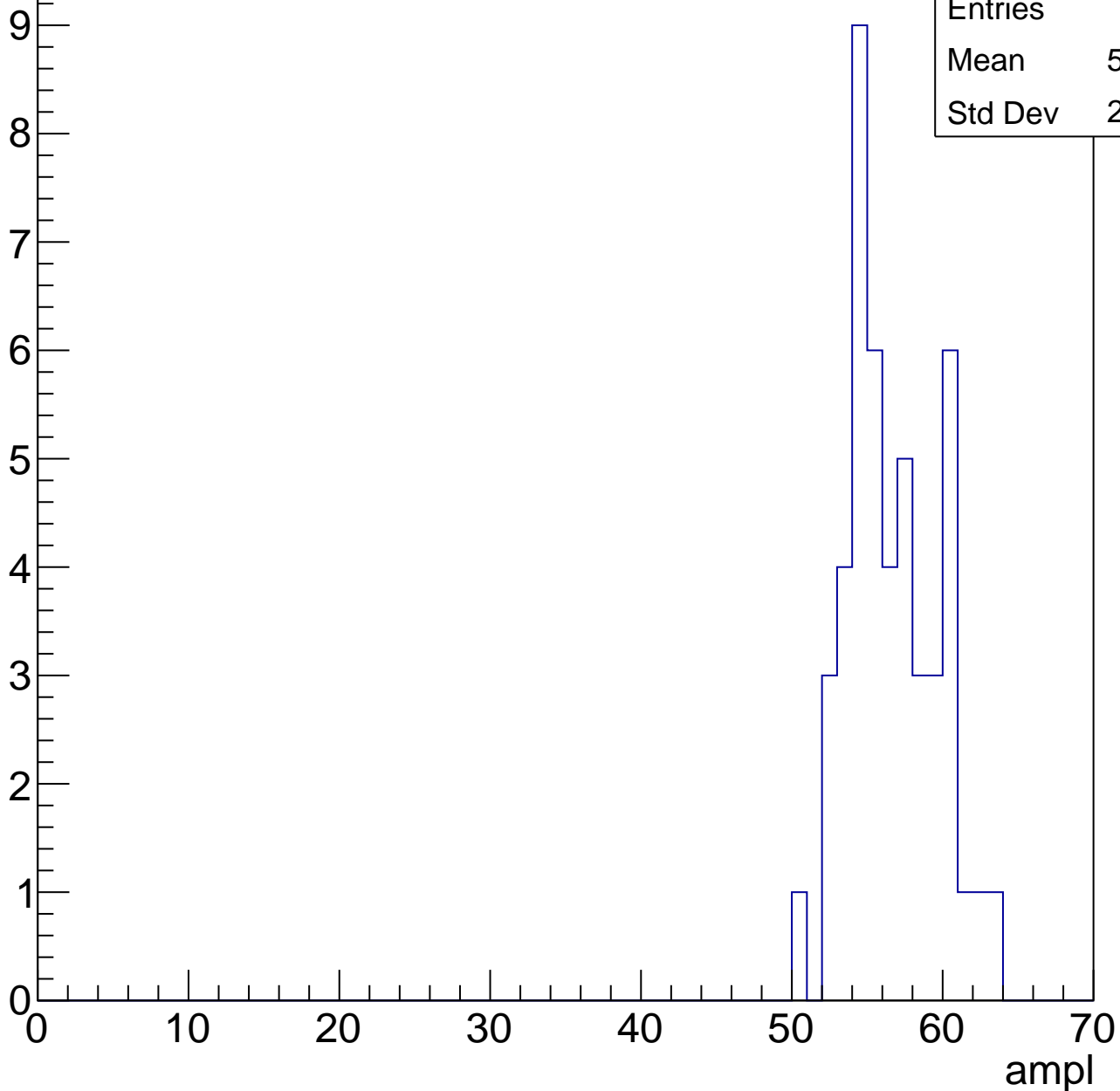


# B1L103S, U9-ch33, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

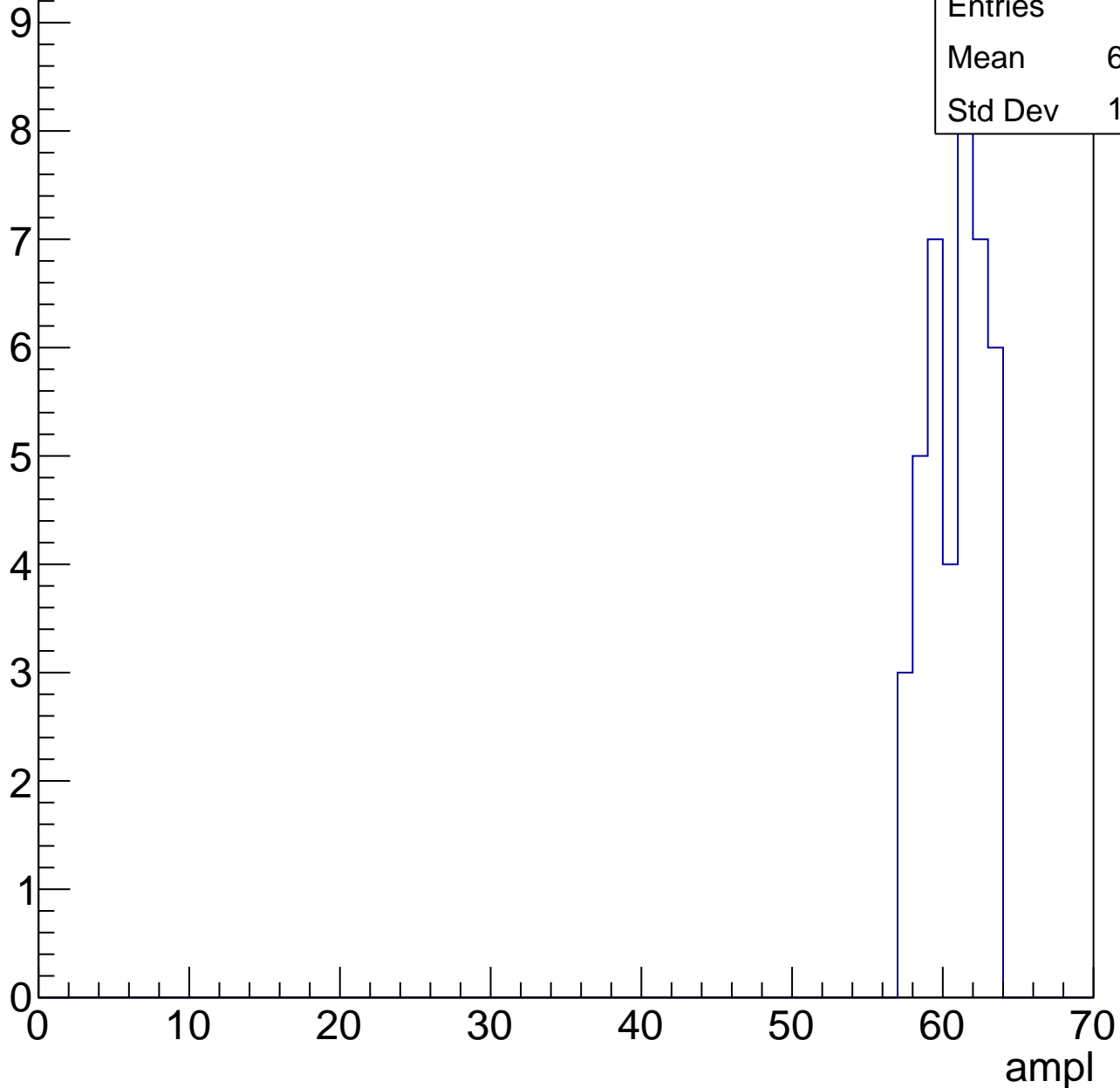
Entries	47
Mean	56.17
Std Dev	2.956



# B1L103S, U9-ch33, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

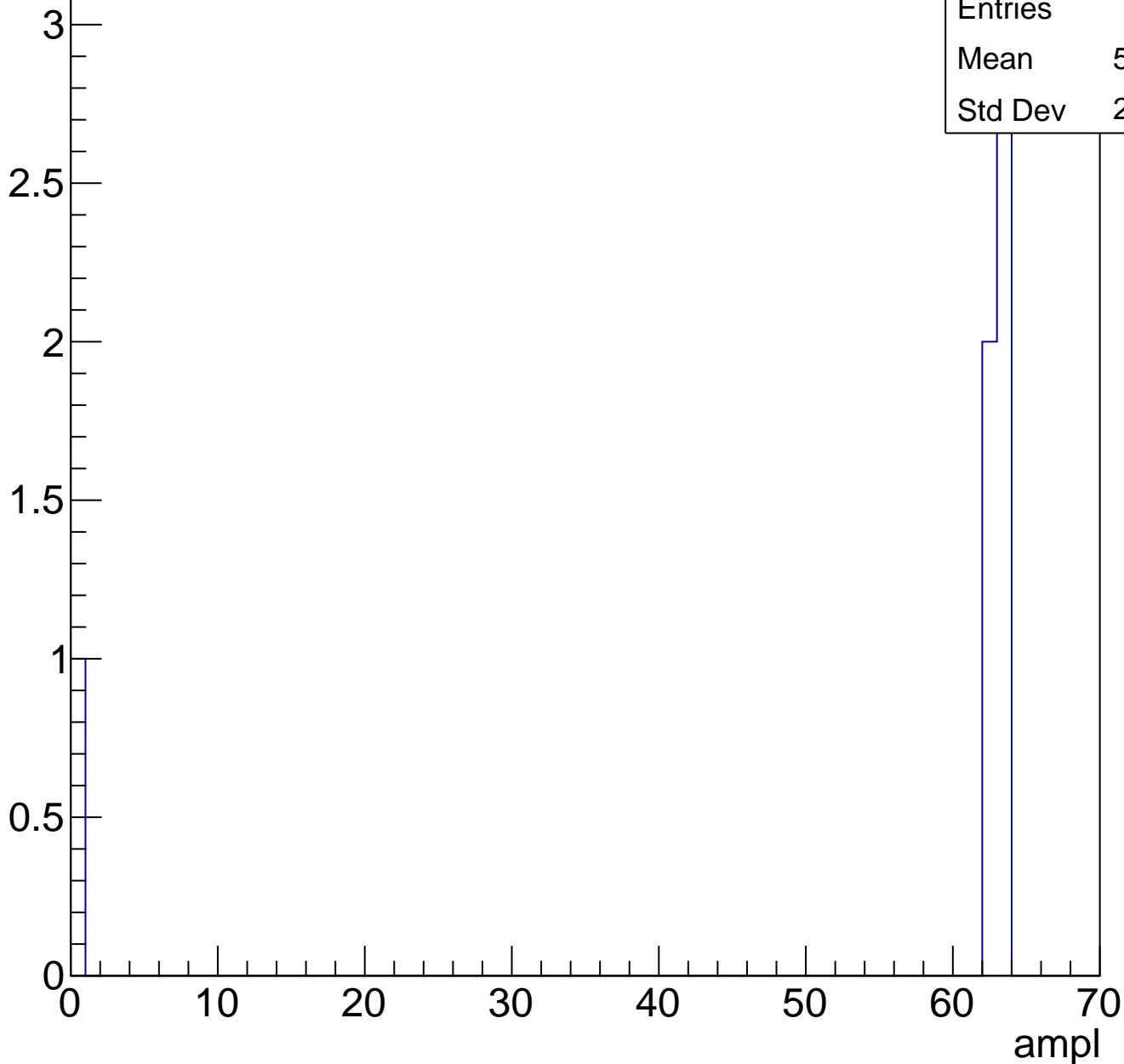
Entry



# B1L103S, U9-ch33, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U9-ch33, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U9-ch34, adc0

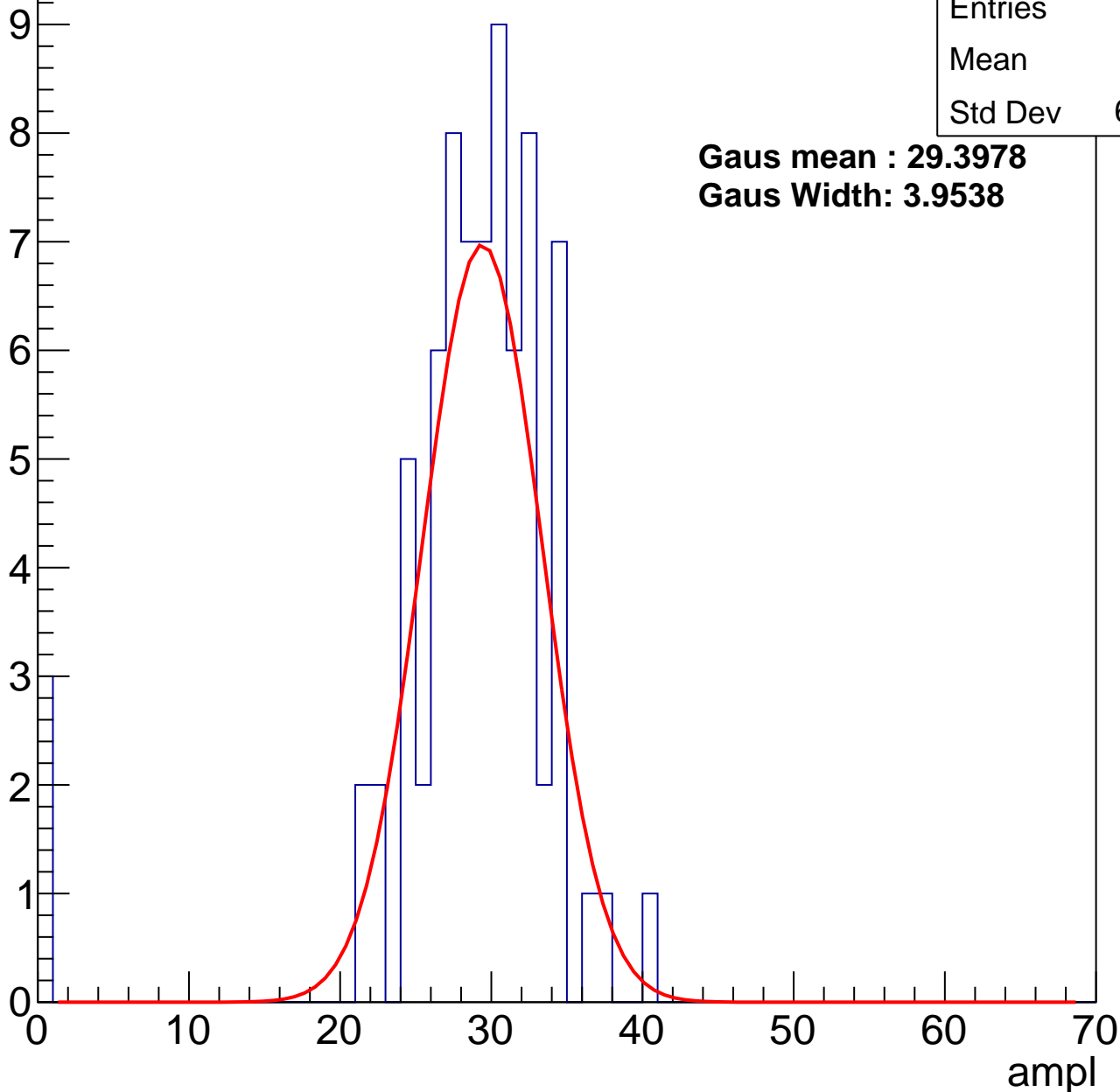
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	77
Mean	28
Std Dev	6.711

**Gaus mean : 29.3978**

**Gaus Width: 3.9538**



# B1L103S, U9-ch34, adc1

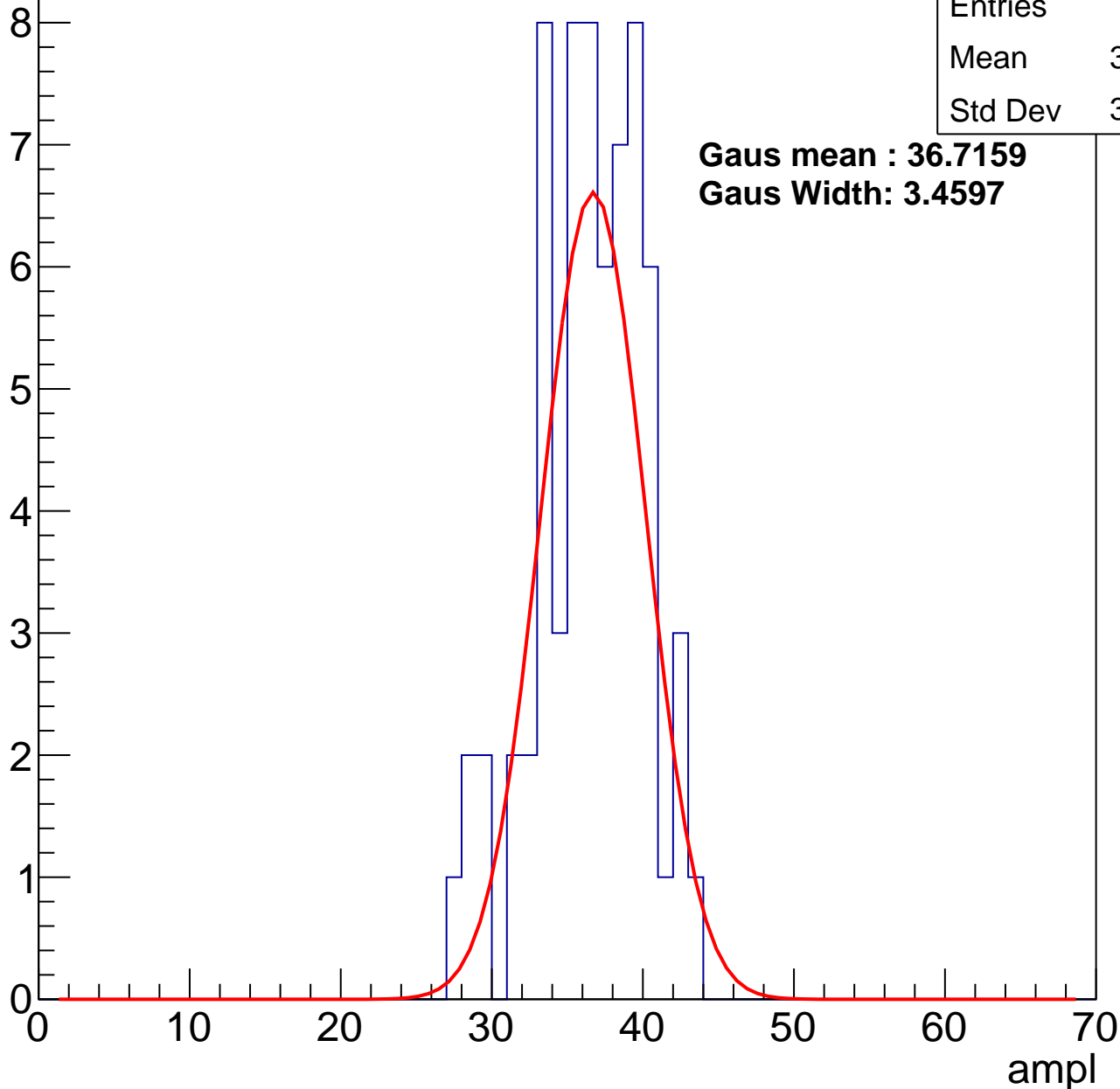
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	68
Mean	36.04
Std Dev	3.566

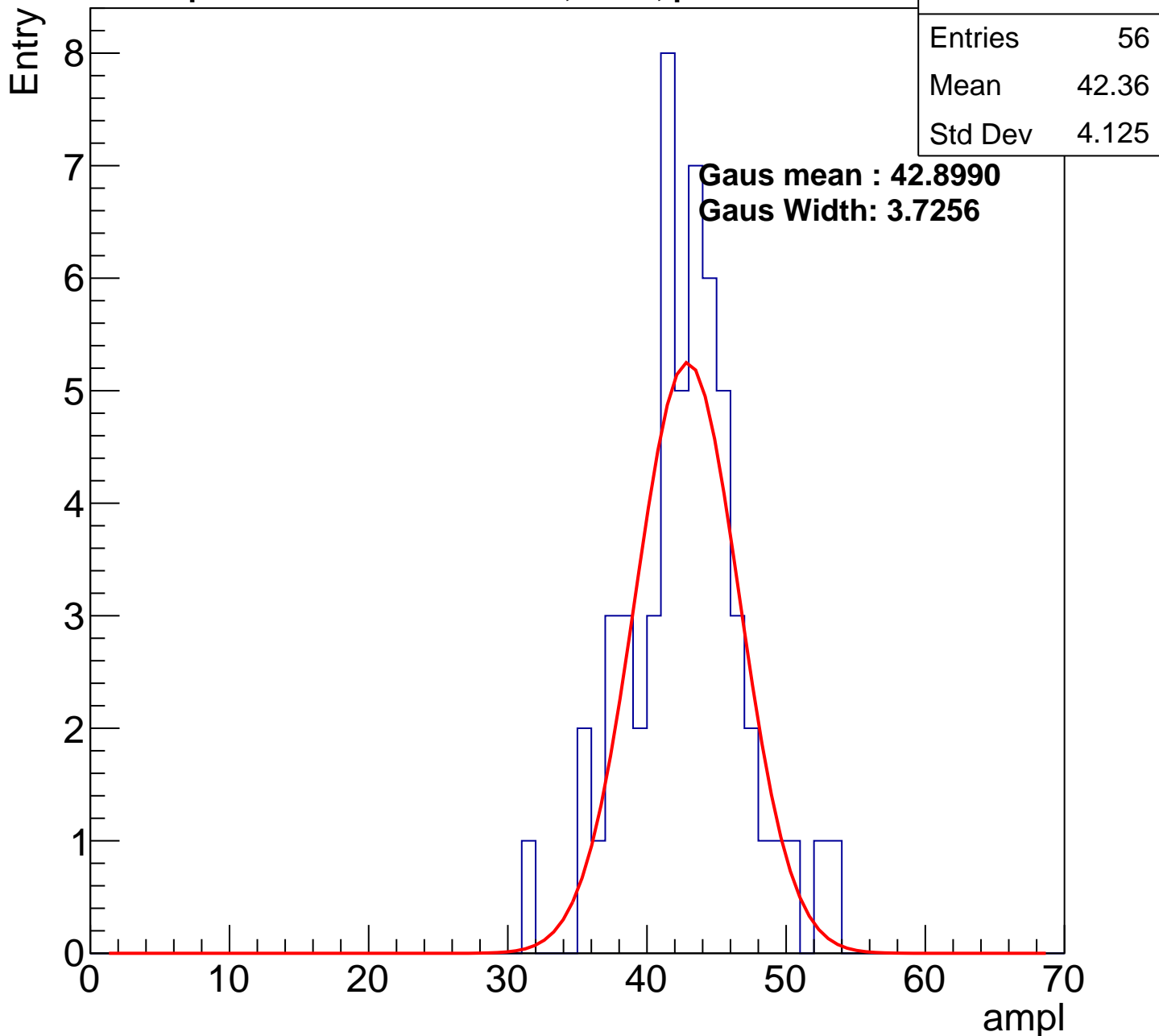
**Gaus mean : 36.7159**

**Gaus Width: 3.4597**



# B1L103S, U9-ch34, adc2

calib\_packv5\_042523\_0143.root, FC#7, port C2

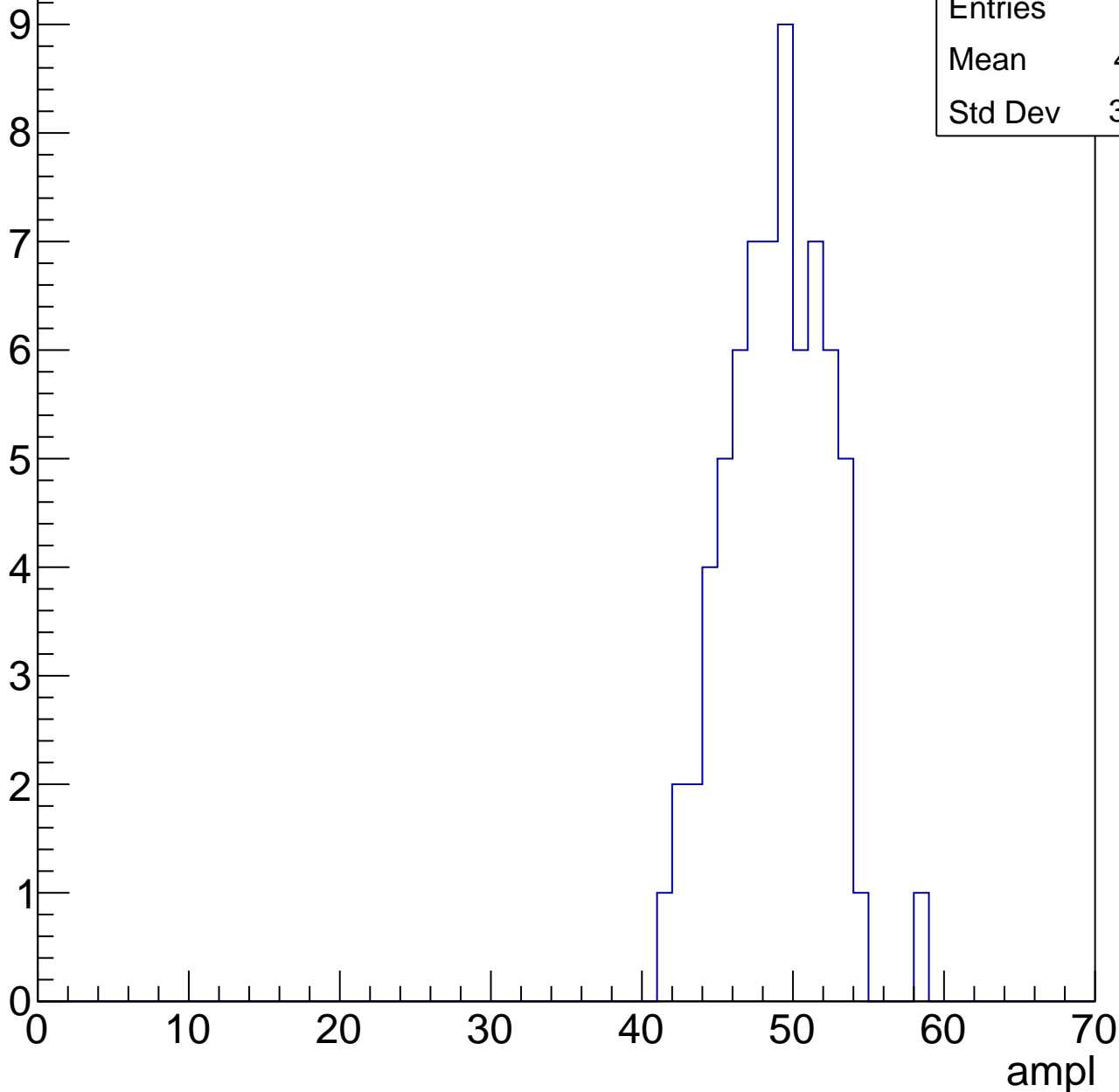


# B1L103S, U9-ch34, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	69
Mean	48.41
Std Dev	3.303

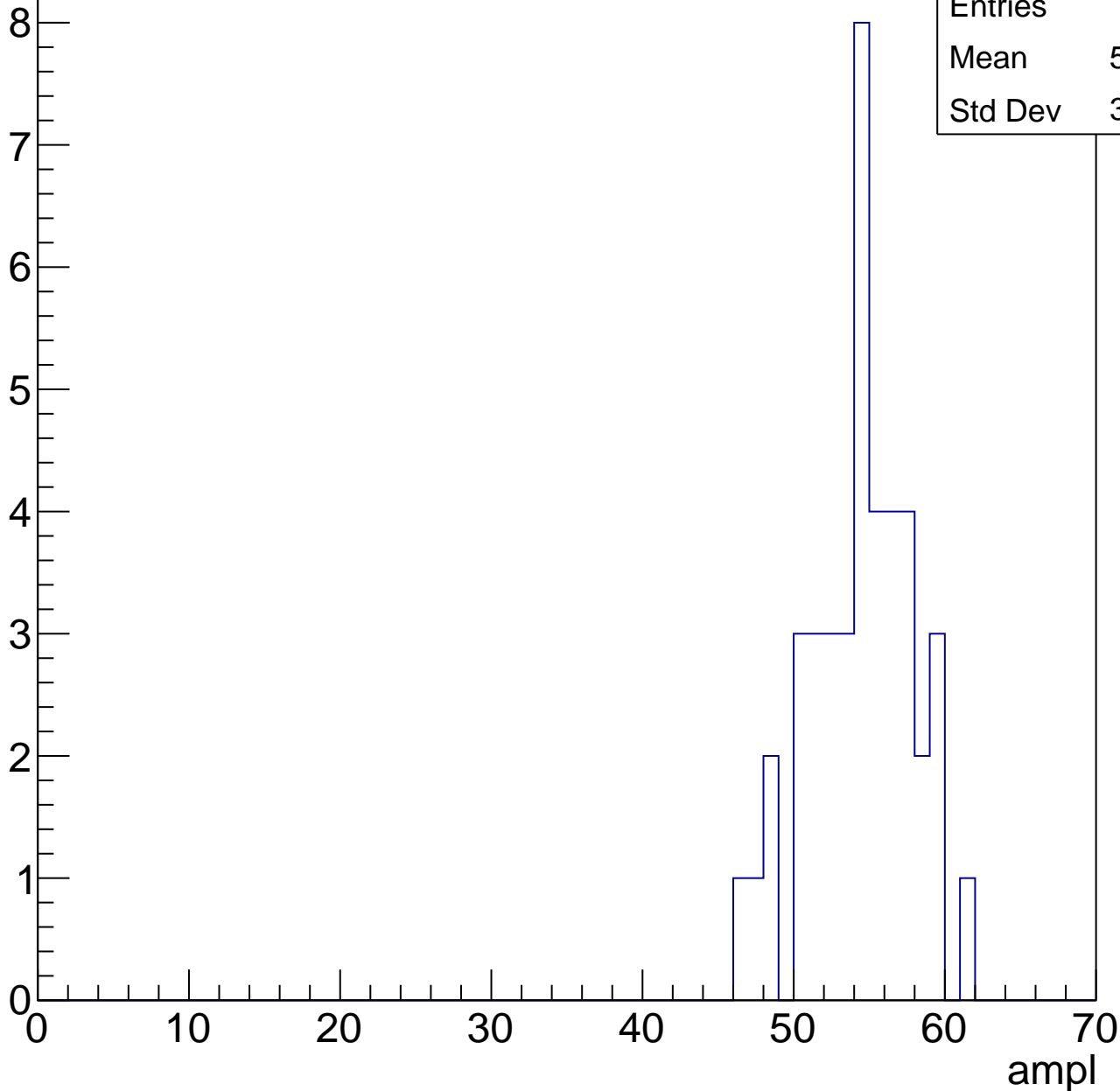


# B1L103S, U9-ch34, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	42
Mean	53.93
Std Dev	3.404



# B1L103S, U9-ch34, adc5

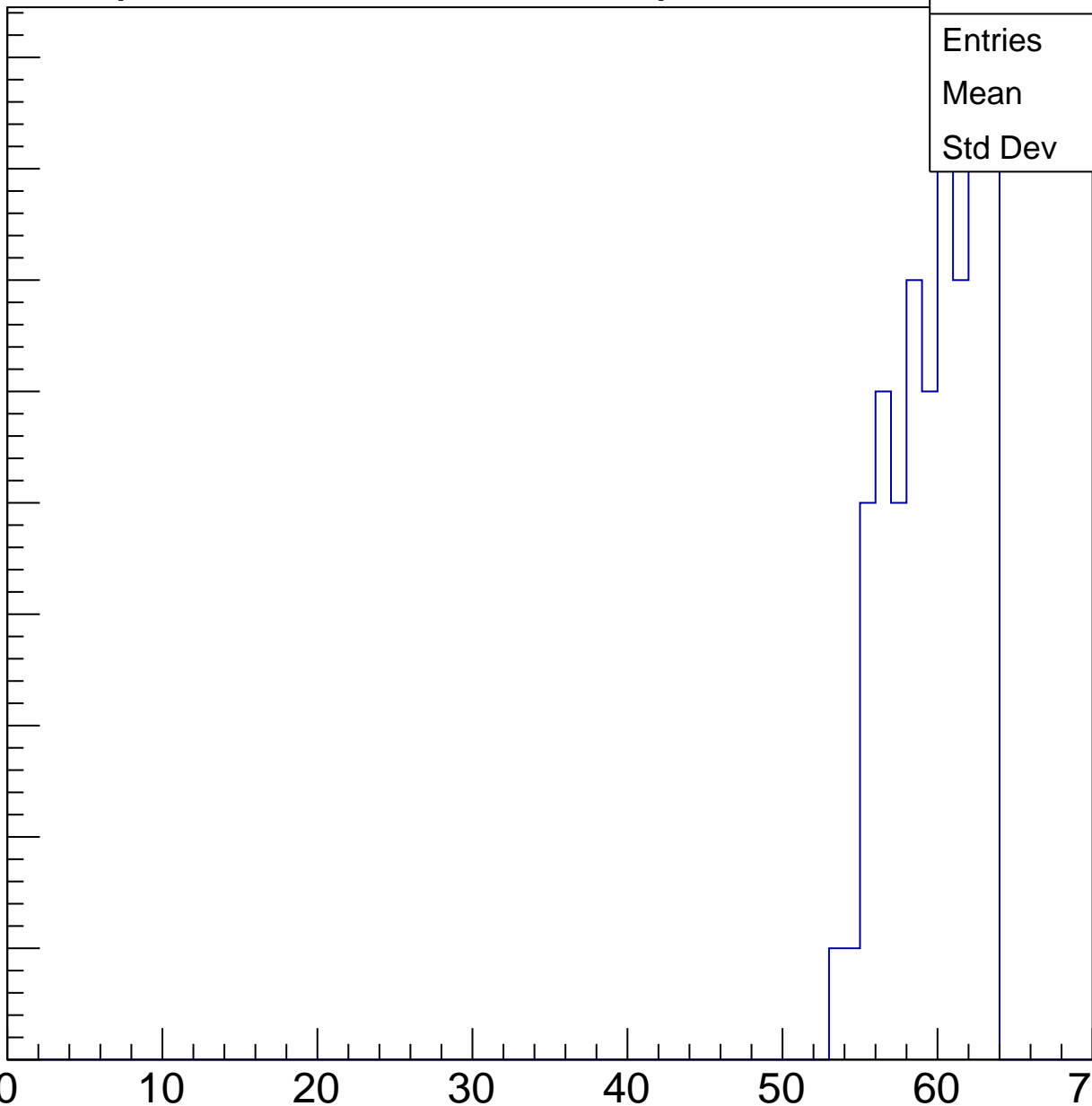
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	63
Mean	59.24
Std Dev	2.712

ampl



# B1L103S, U9-ch34, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

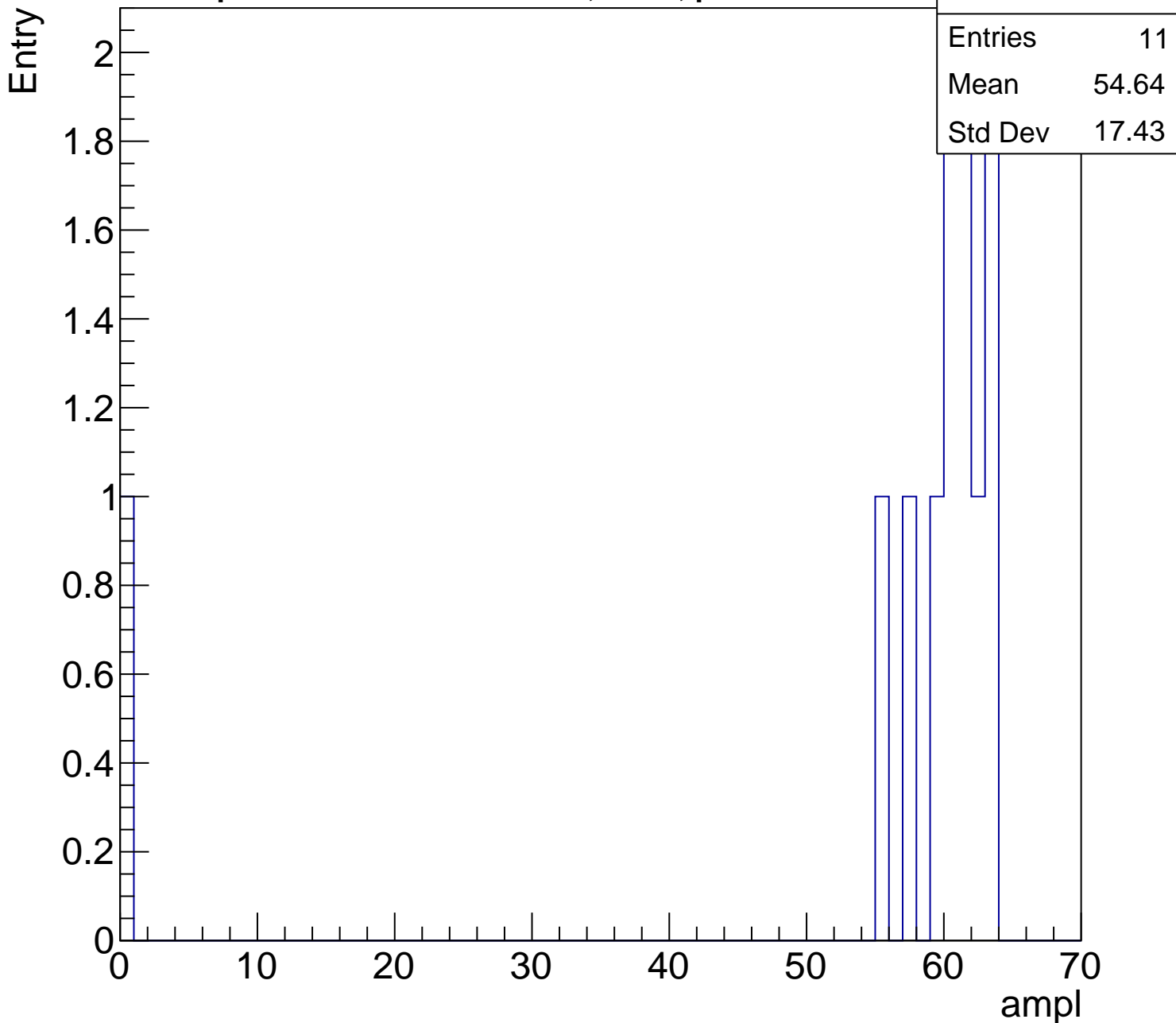
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	11
Mean	54.64
Std Dev	17.43

0 10 20 30 40 50 60 70

ampl





# B1L103S, U9-ch34, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U9-ch35, adc0

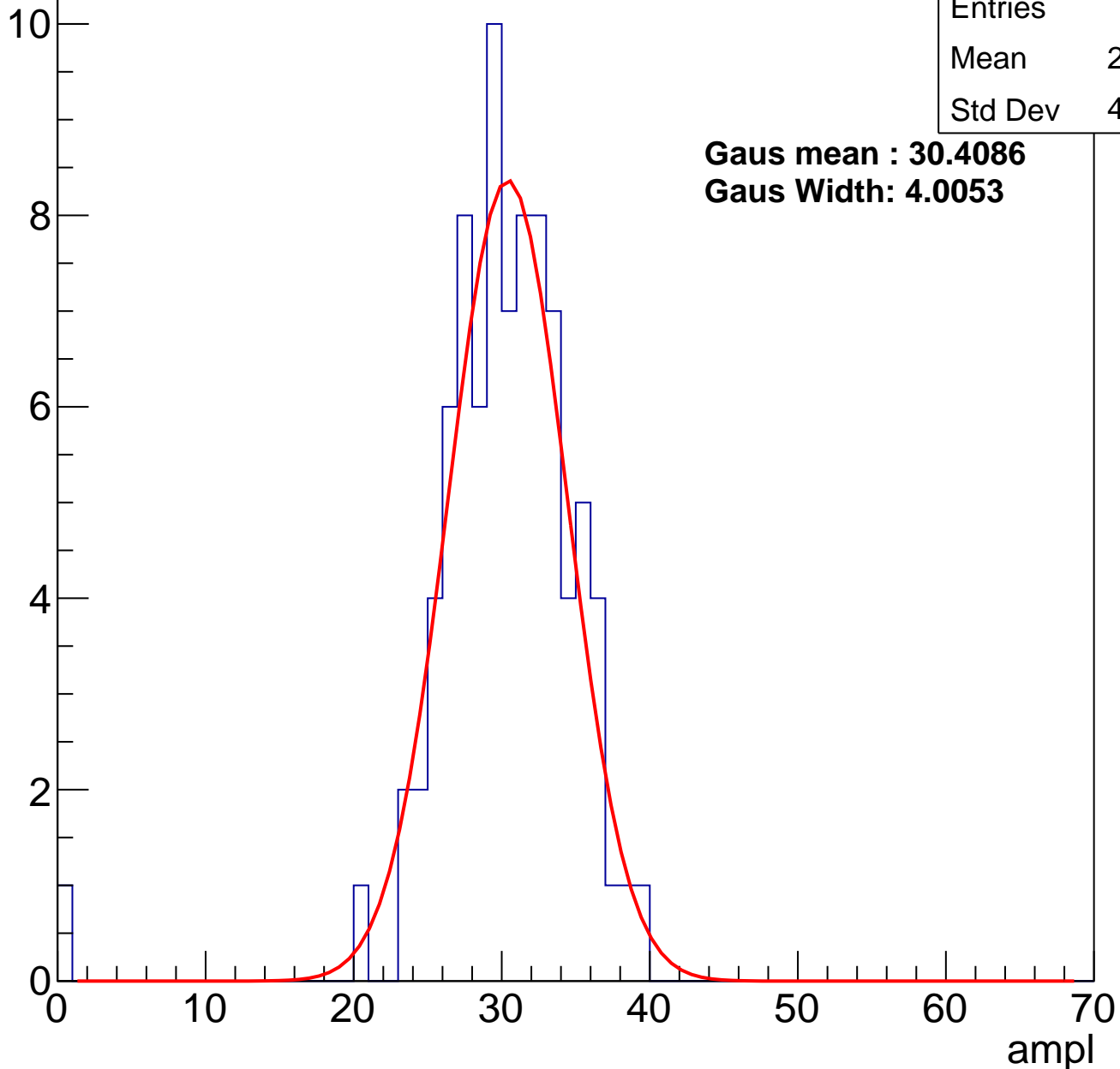
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	86
Mean	29.74
Std Dev	4.937

**Gaus mean : 30.4086**

**Gaus Width: 4.0053**

Entry



# B1L103S, U9-ch35, adc1

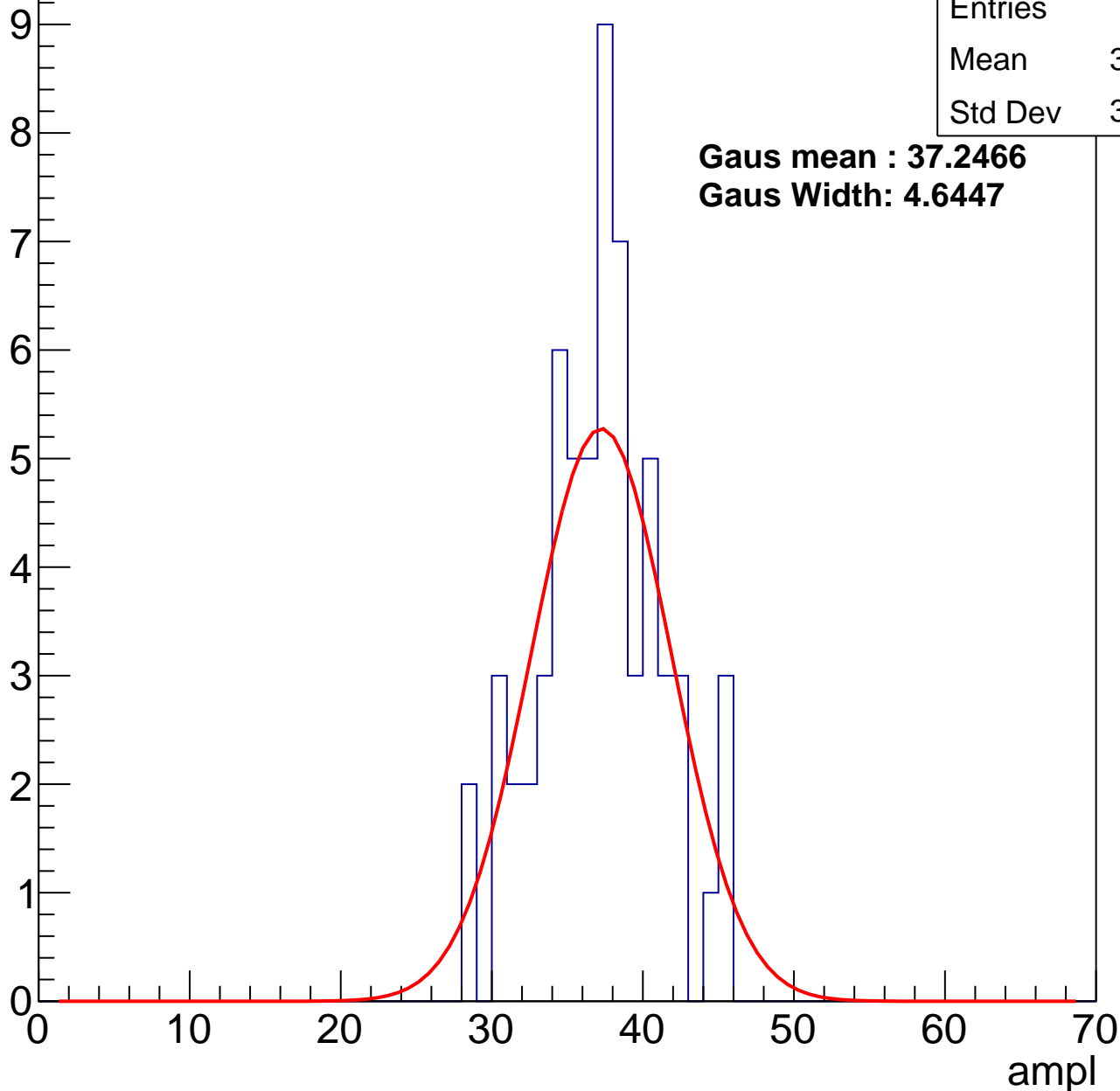
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	36.68
Std Dev	3.975

**Gaus mean : 37.2466**

**Gaus Width: 4.6447**



# B1L103S, U9-ch35, adc2

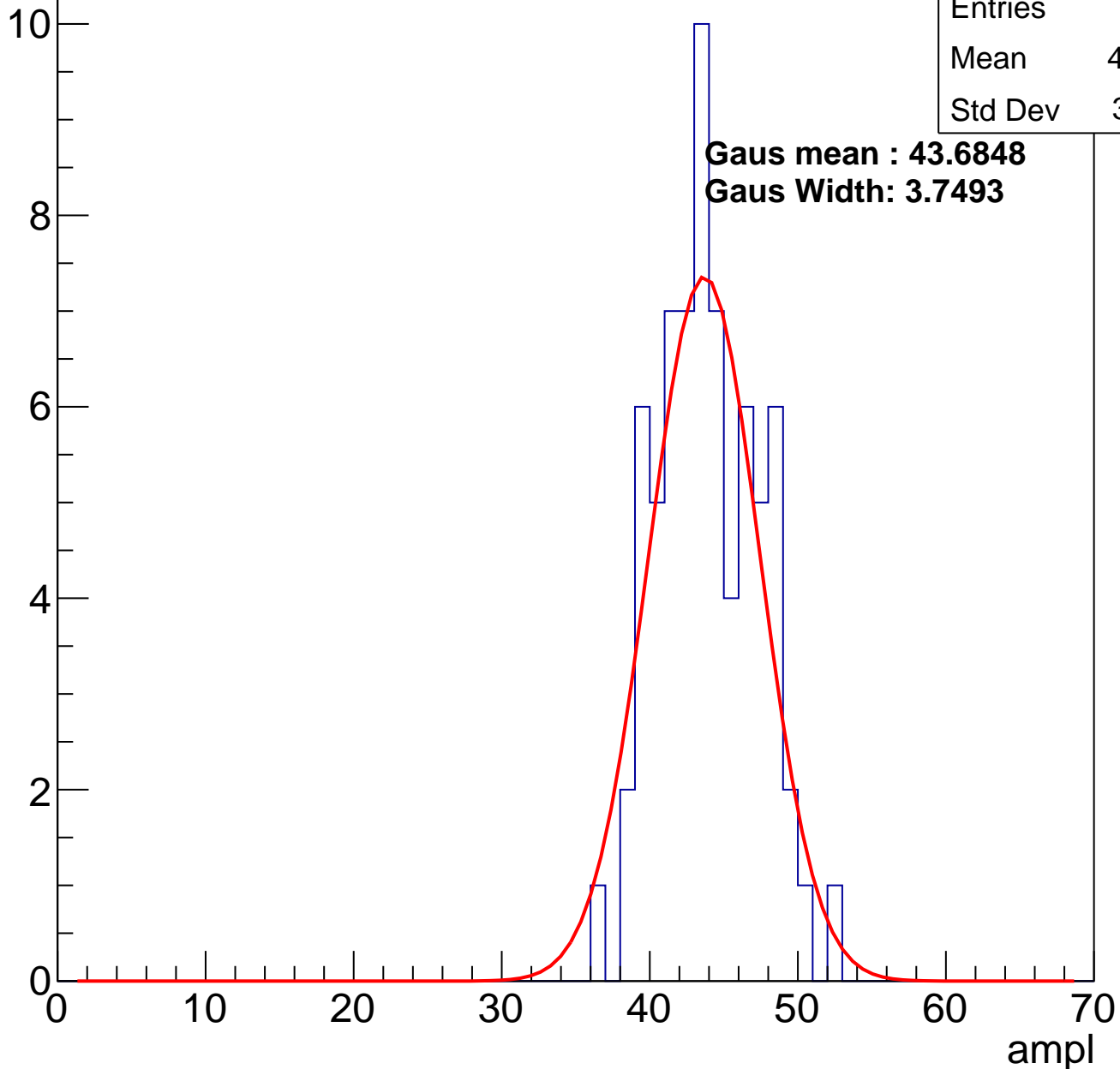
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	70
Mean	43.49
Std Dev	3.311

**Gaus mean : 43.6848**

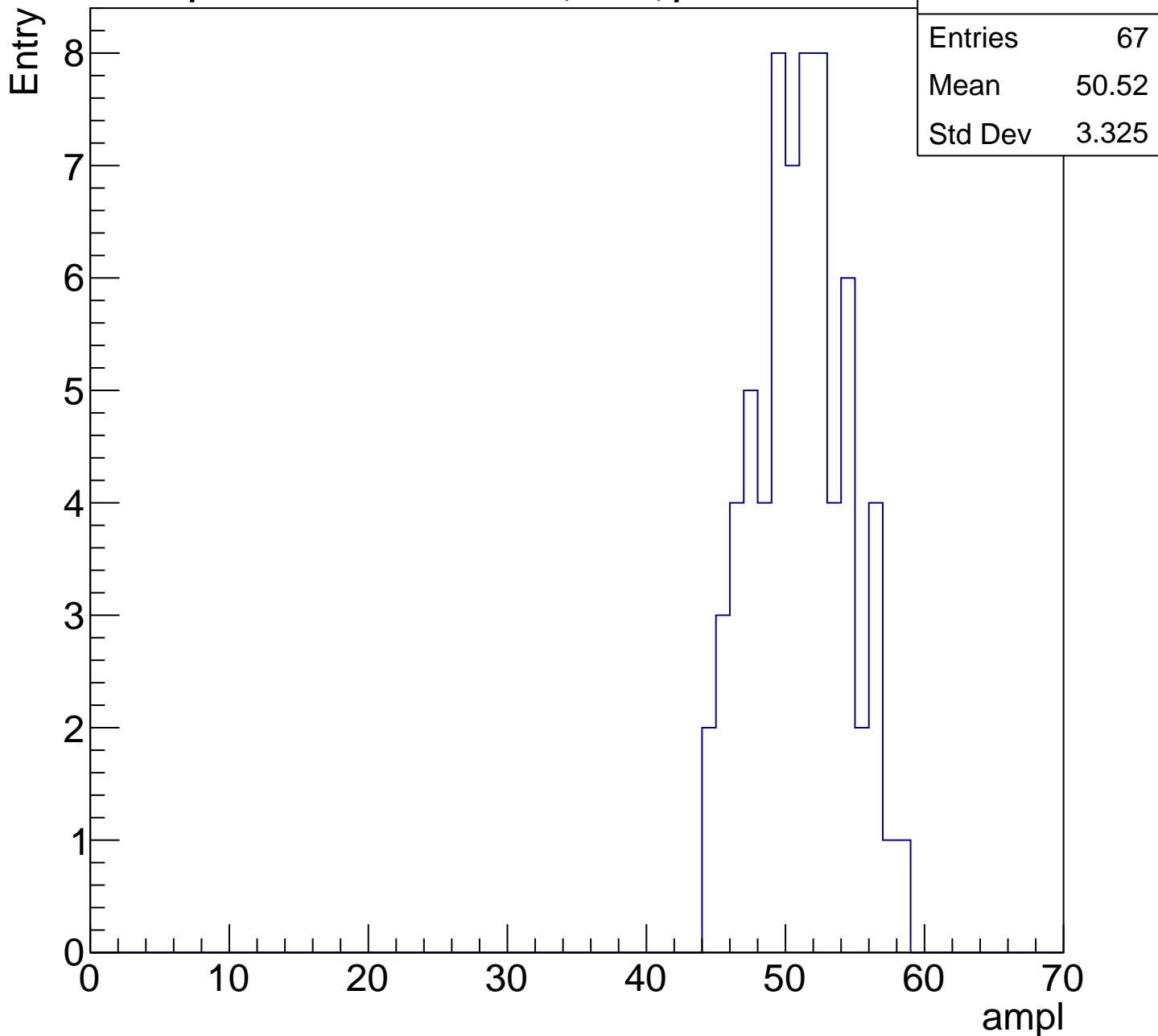
**Gaus Width: 3.7493**

Entry



# B1L103S, U9-ch35, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

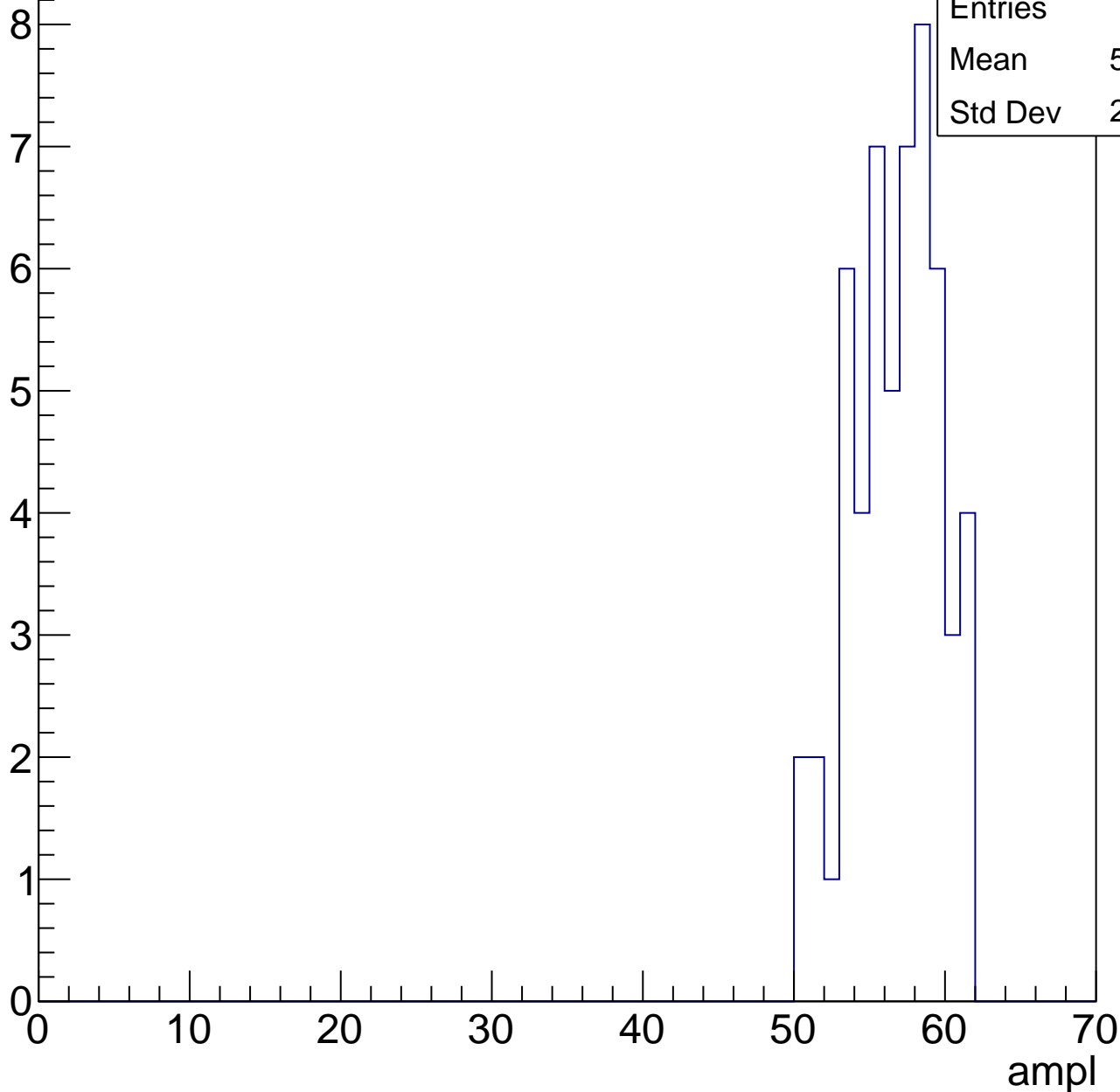


# B1L103S, U9-ch35, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	55
Mean	56.25
Std Dev	2.868



# B1L103S, U9-ch35, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	40
Mean	59.23
Std Dev	9.697

Entry

10

8

6

4

2

0

0

10

20

30

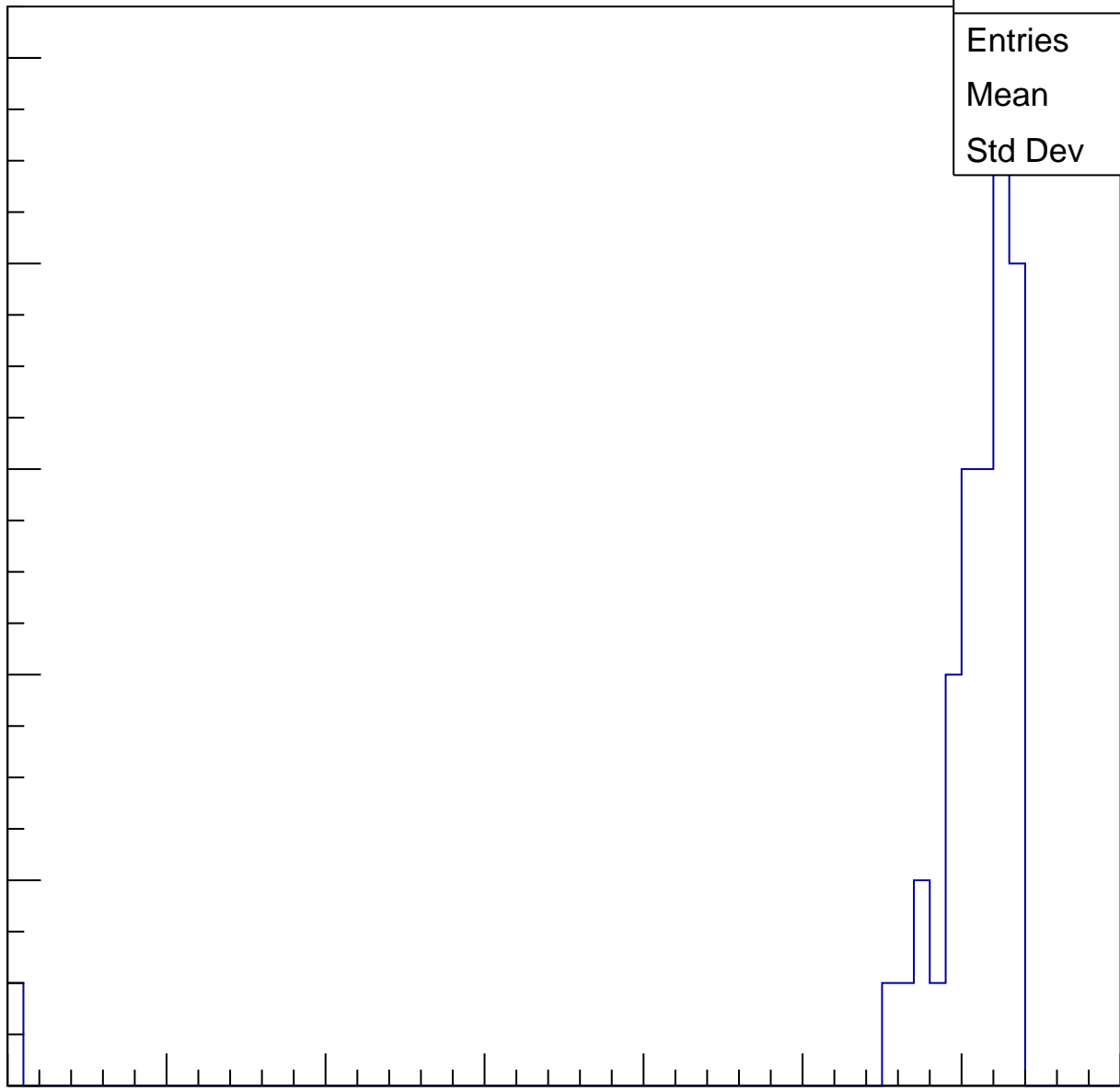
40

50

60

70

ampl



# B1L103S, U9-ch35, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U9-ch35, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L103S, U9-ch36, adc0

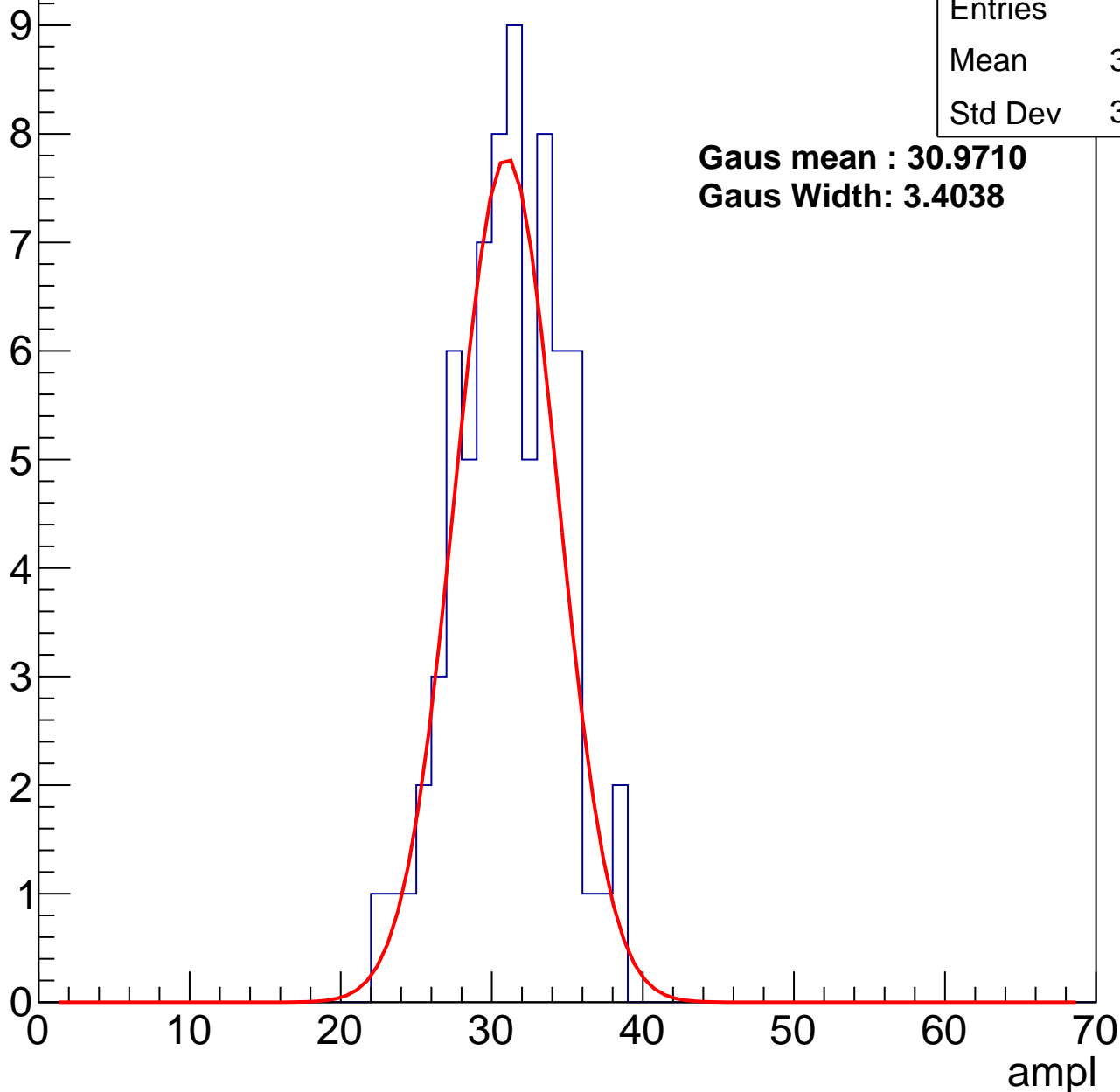
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	72
Mean	30.67
Std Dev	3.448

**Gaus mean : 30.9710**

**Gaus Width: 3.4038**



# B1L103S, U9-ch36, adc1

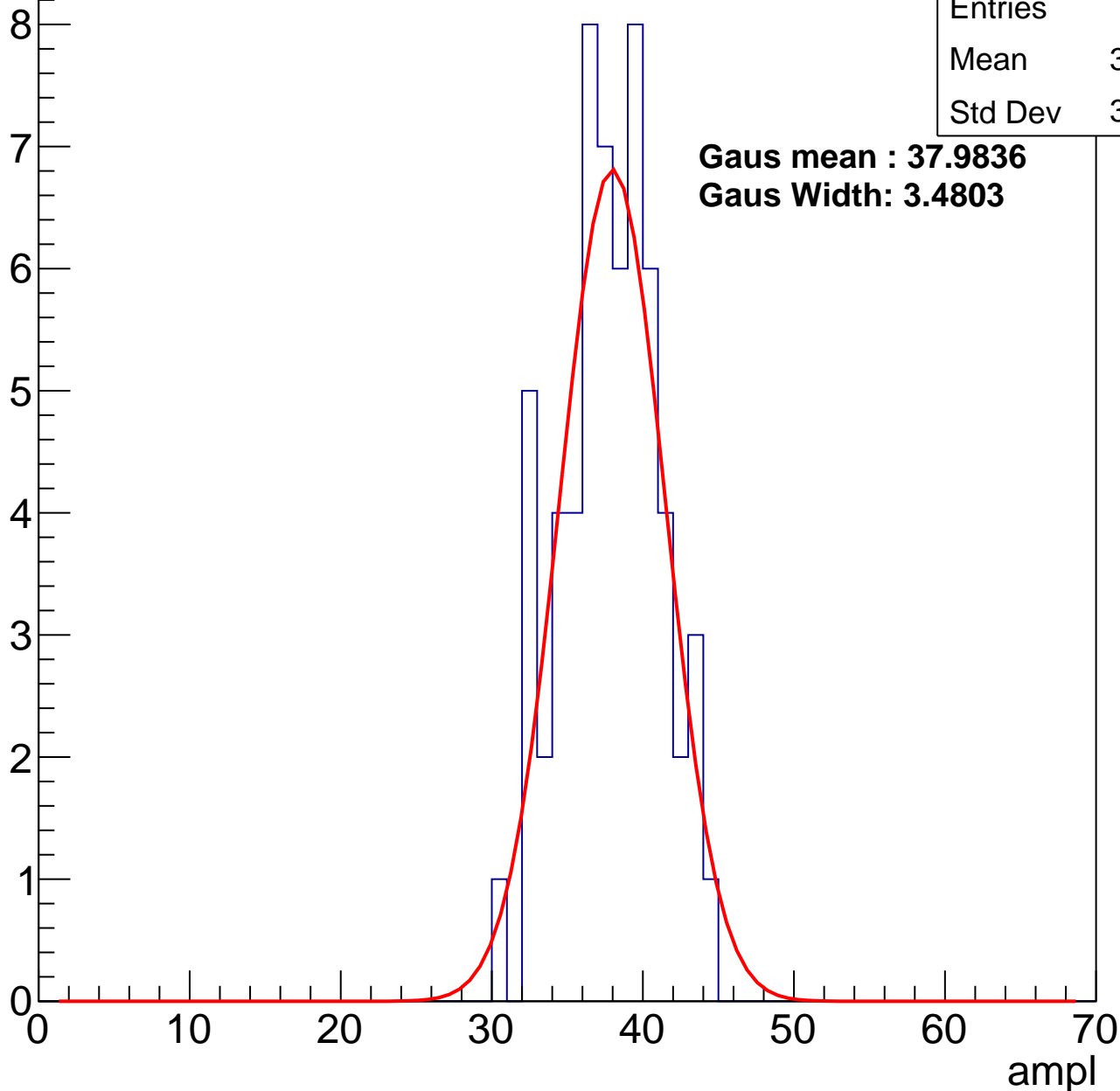
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	61
Mean	37.38
Std Dev	3.189

**Gaus mean : 37.9836**

**Gaus Width: 3.4803**



# B1L103S, U9-ch36, adc2

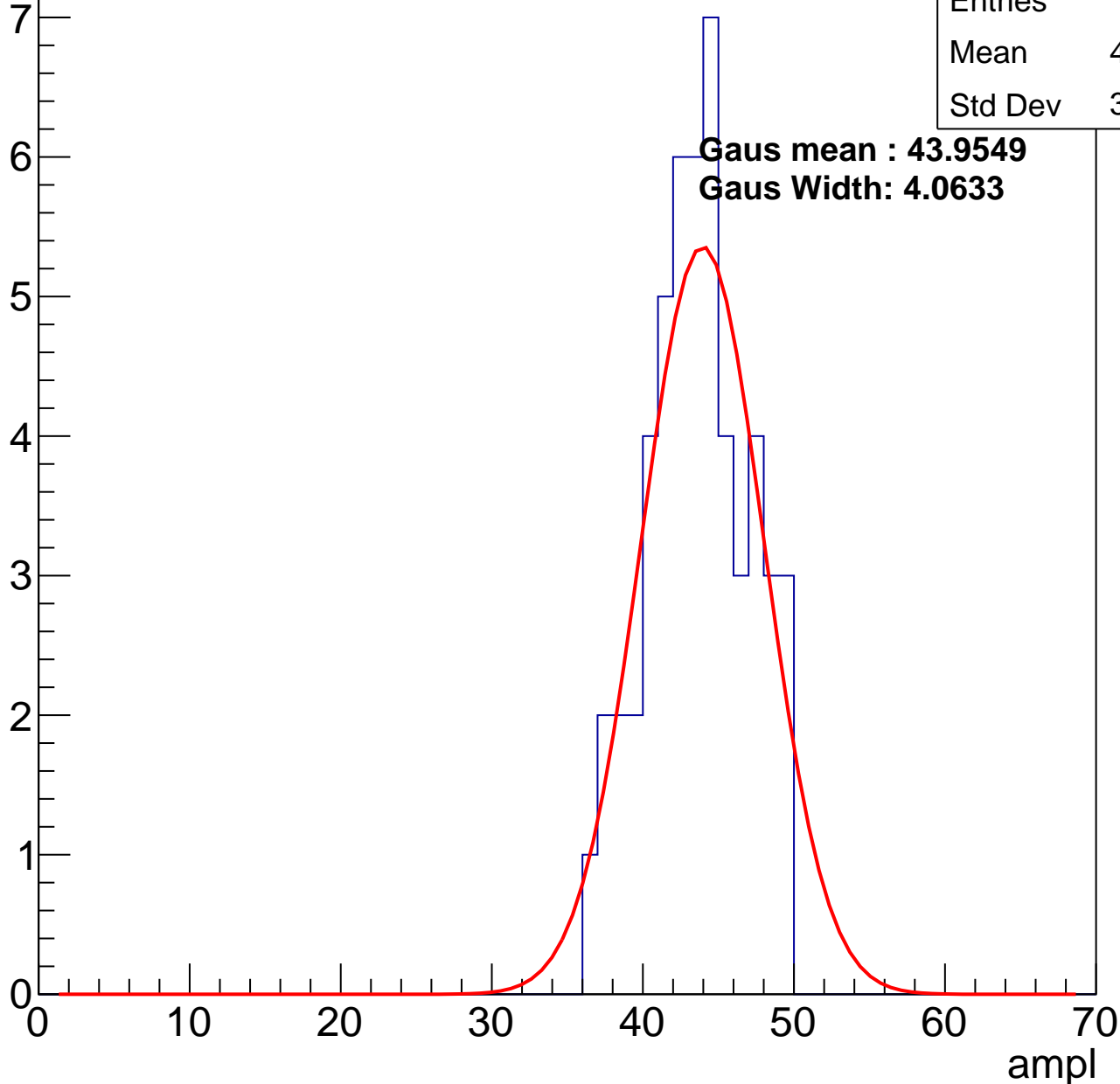
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	52
Mean	43.15
Std Dev	3.284

**Gaus mean : 43.9549**

**Gaus Width: 4.0633**

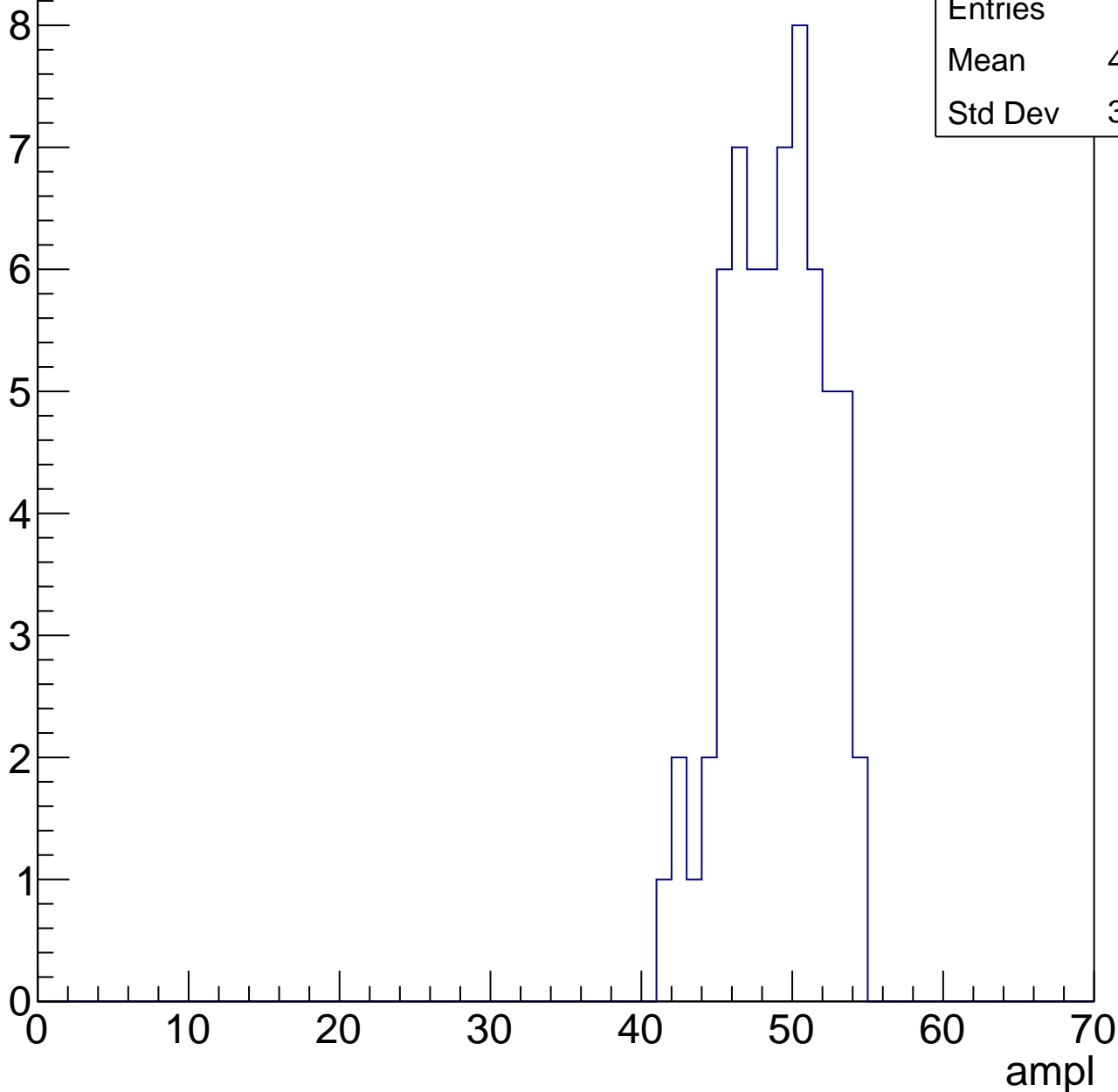


# B1L103S, U9-ch36, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	48.44
Std Dev	3.122

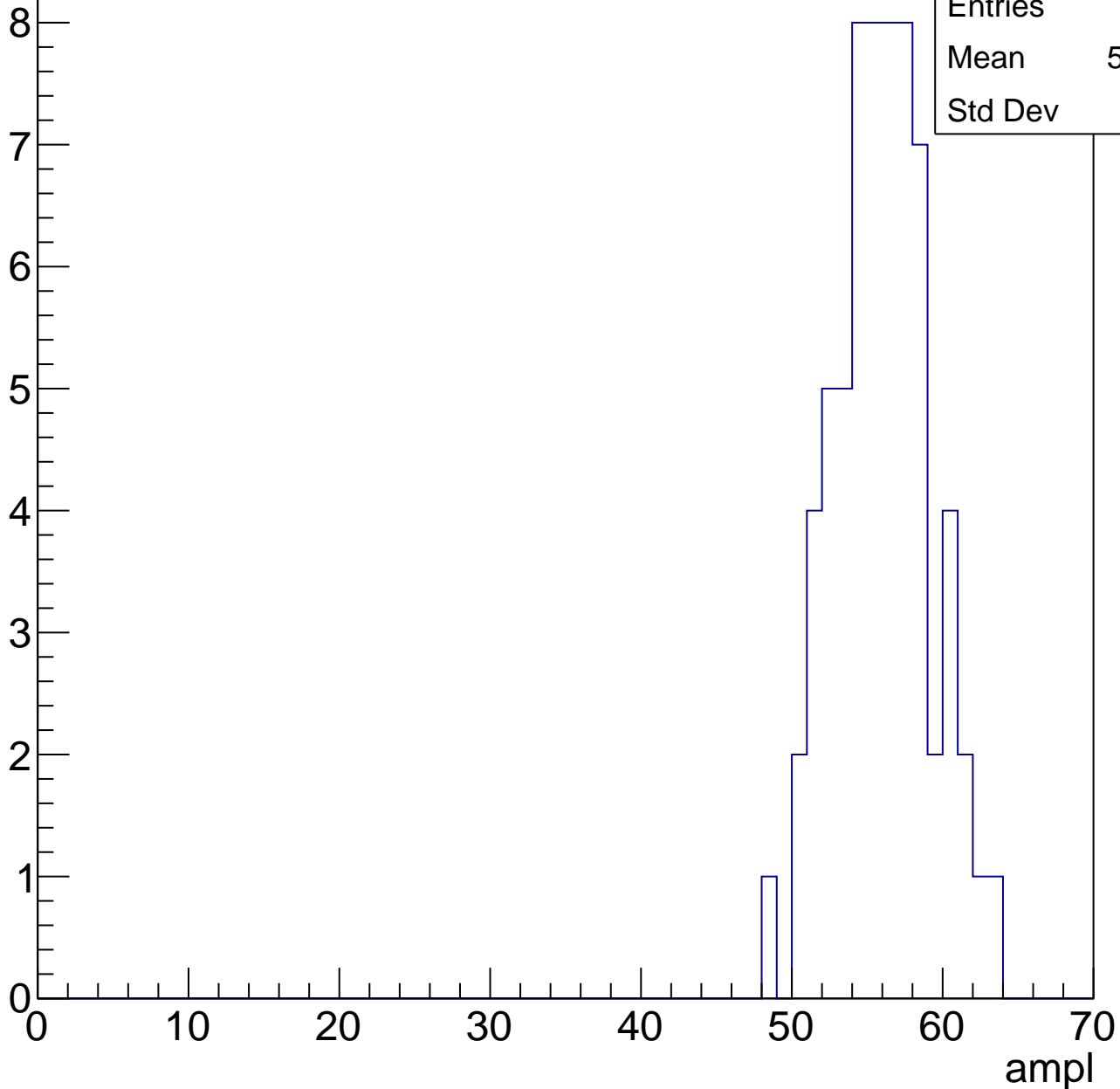


# B1L103S, U9-ch36, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	55.52
Std Dev	3.11



# B1L103S, U9-ch36, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	47
Mean	58.94
Std Dev	8.967

ampl

0 10 20 30 40 50 60 70

0

1

2

3

4

5

6

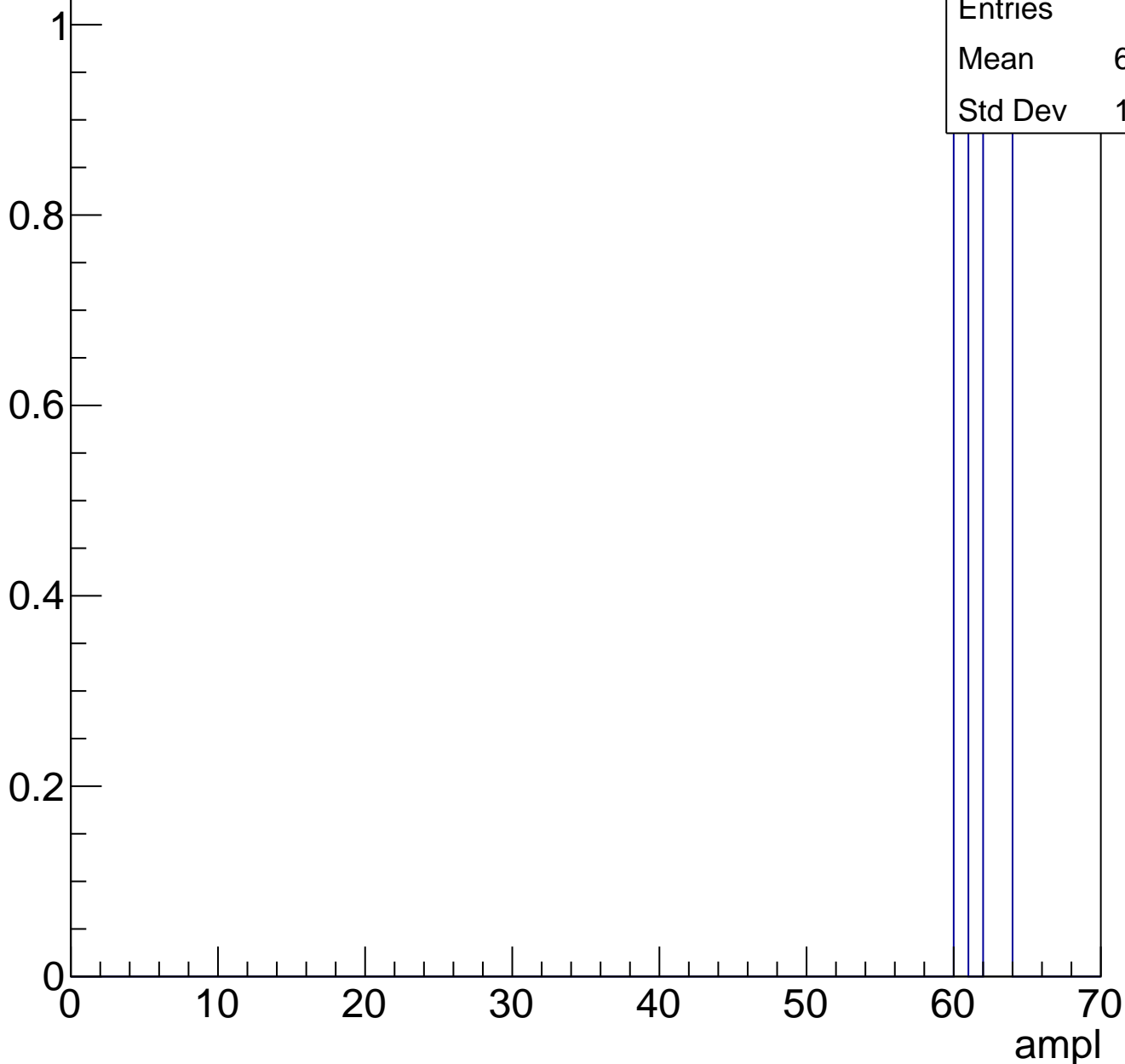
7

8

# B1L103S, U9-ch36, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

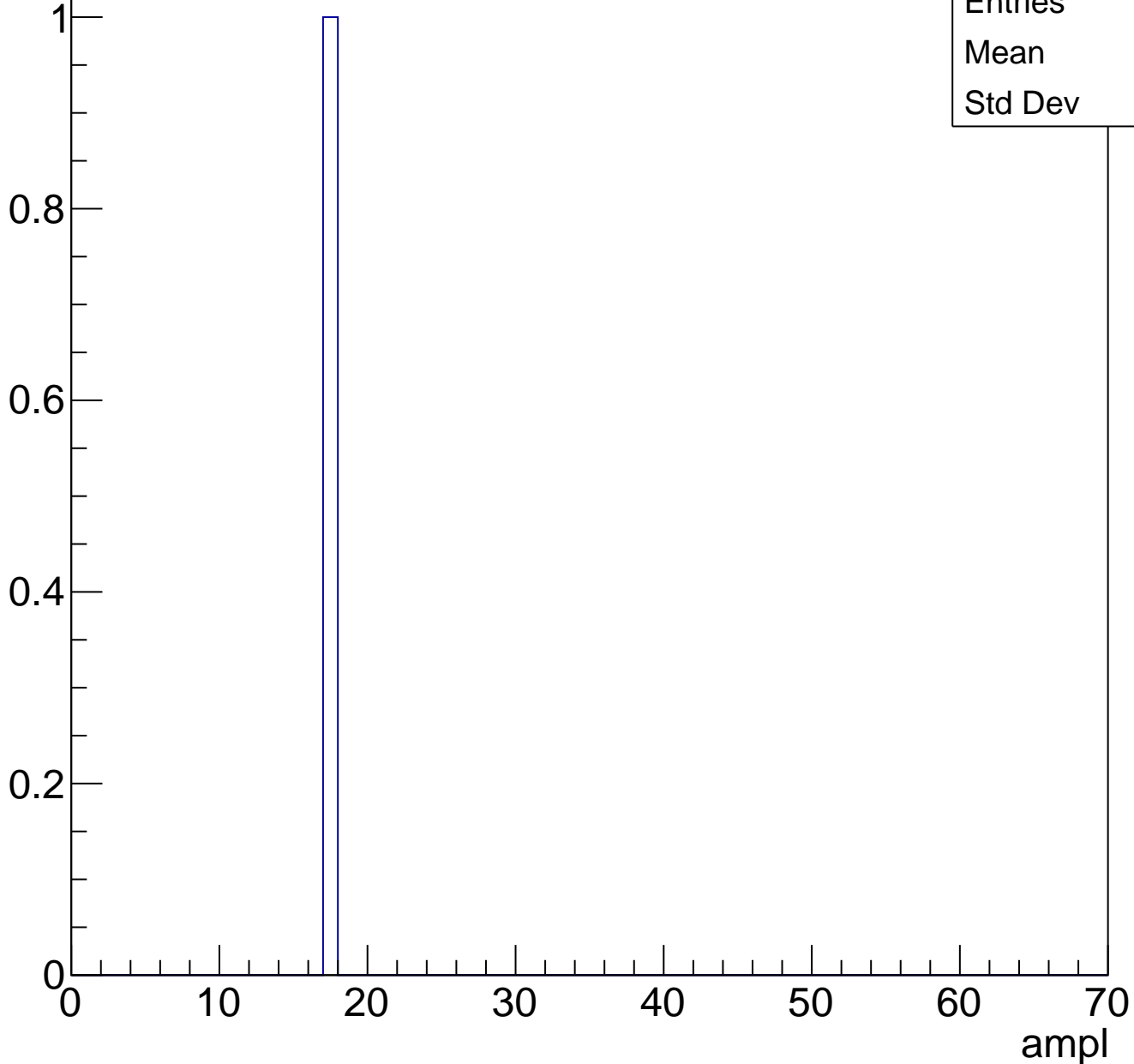




# B1L103S, U9-ch36, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U9-ch37, adc0

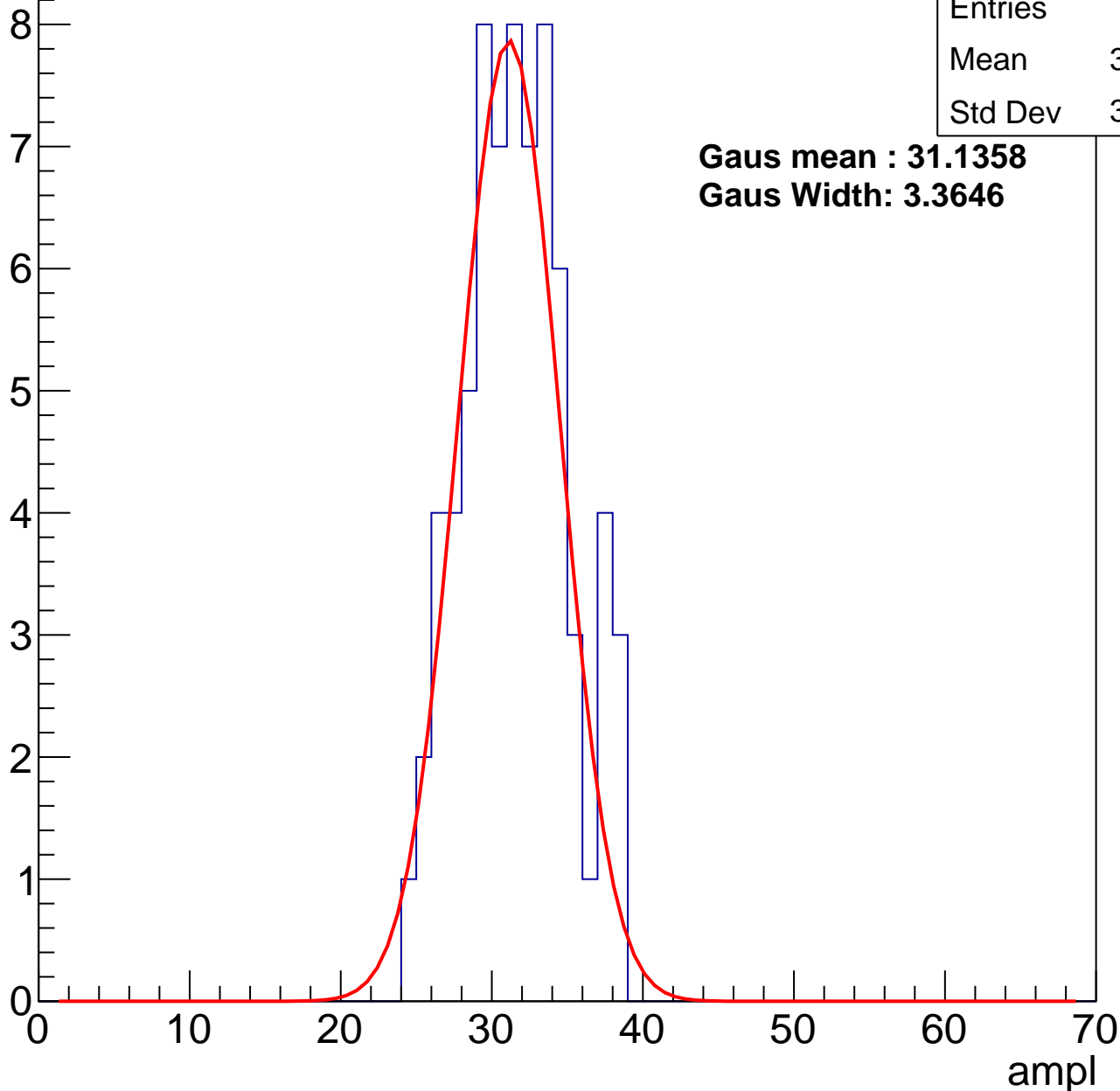
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	71
Mean	31.14
Std Dev	3.408

**Gaus mean : 31.1358**

**Gaus Width: 3.3646**



# B1L103S, U9-ch37, adc1

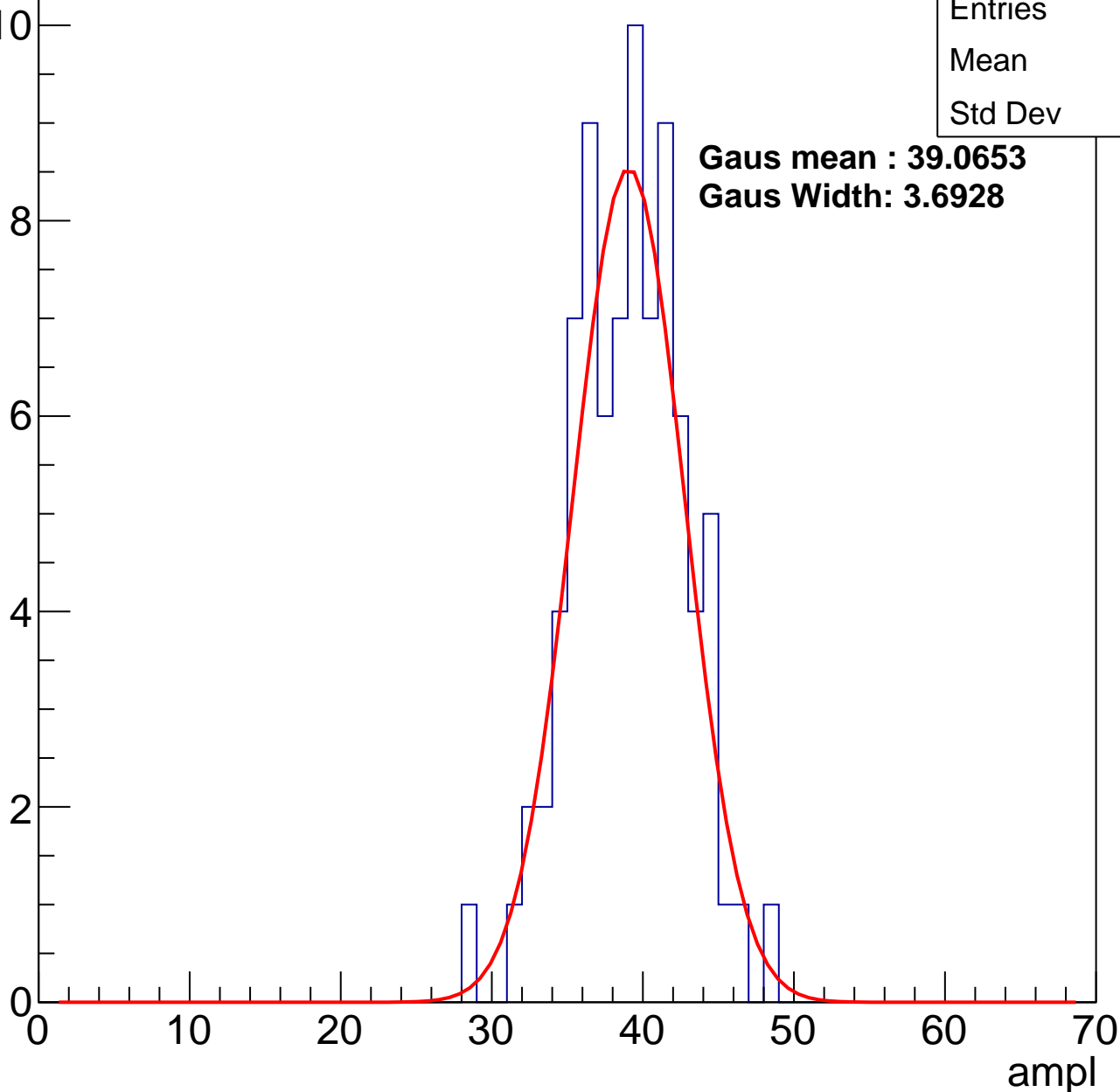
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	83
Mean	38.6
Std Dev	3.67

**Gaus mean : 39.0653**

**Gaus Width: 3.6928**



# B1L103S, U9-ch37, adc2

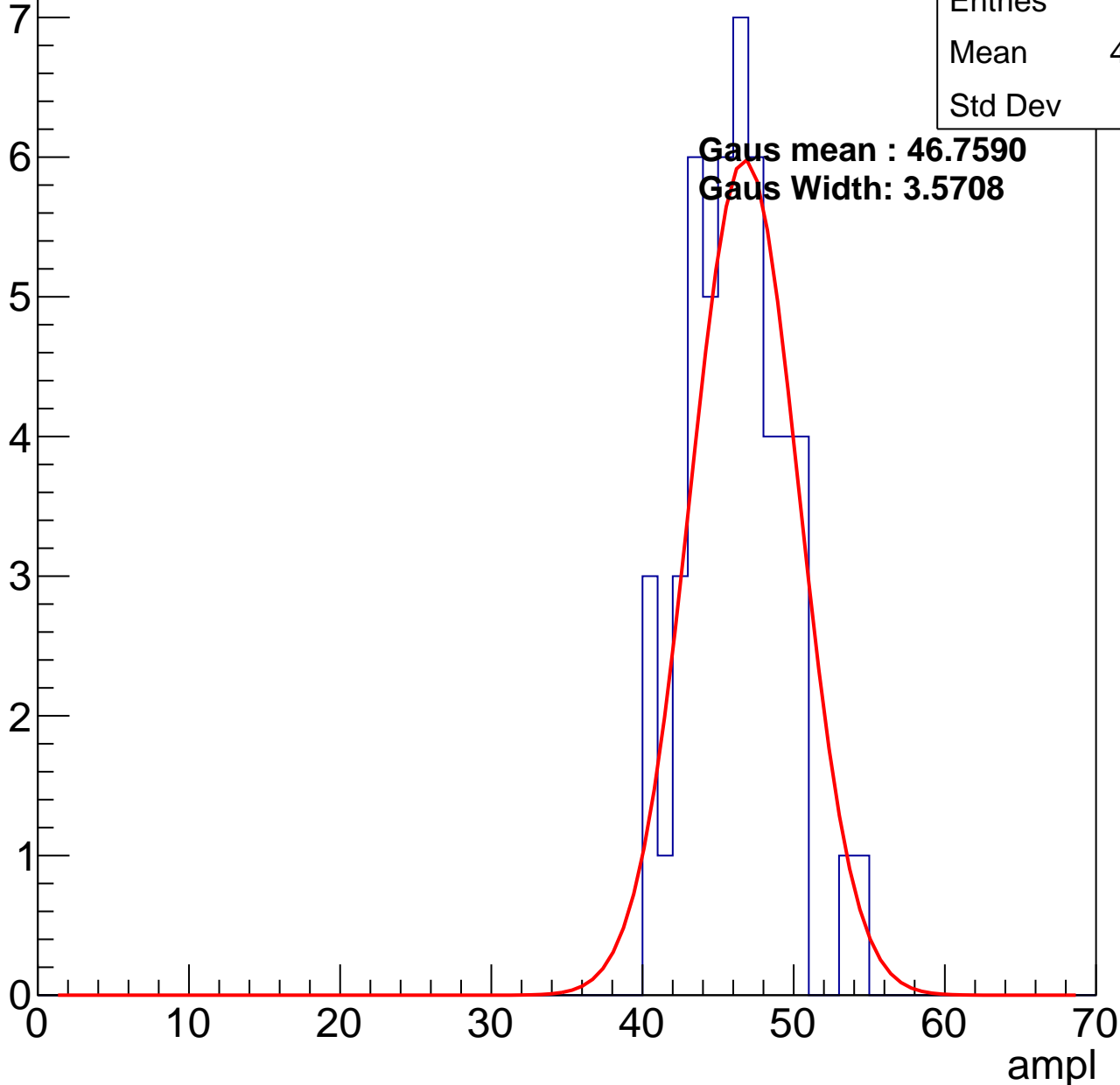
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	51
Mean	45.76
Std Dev	3.11

**Gaus mean : 46.7590**

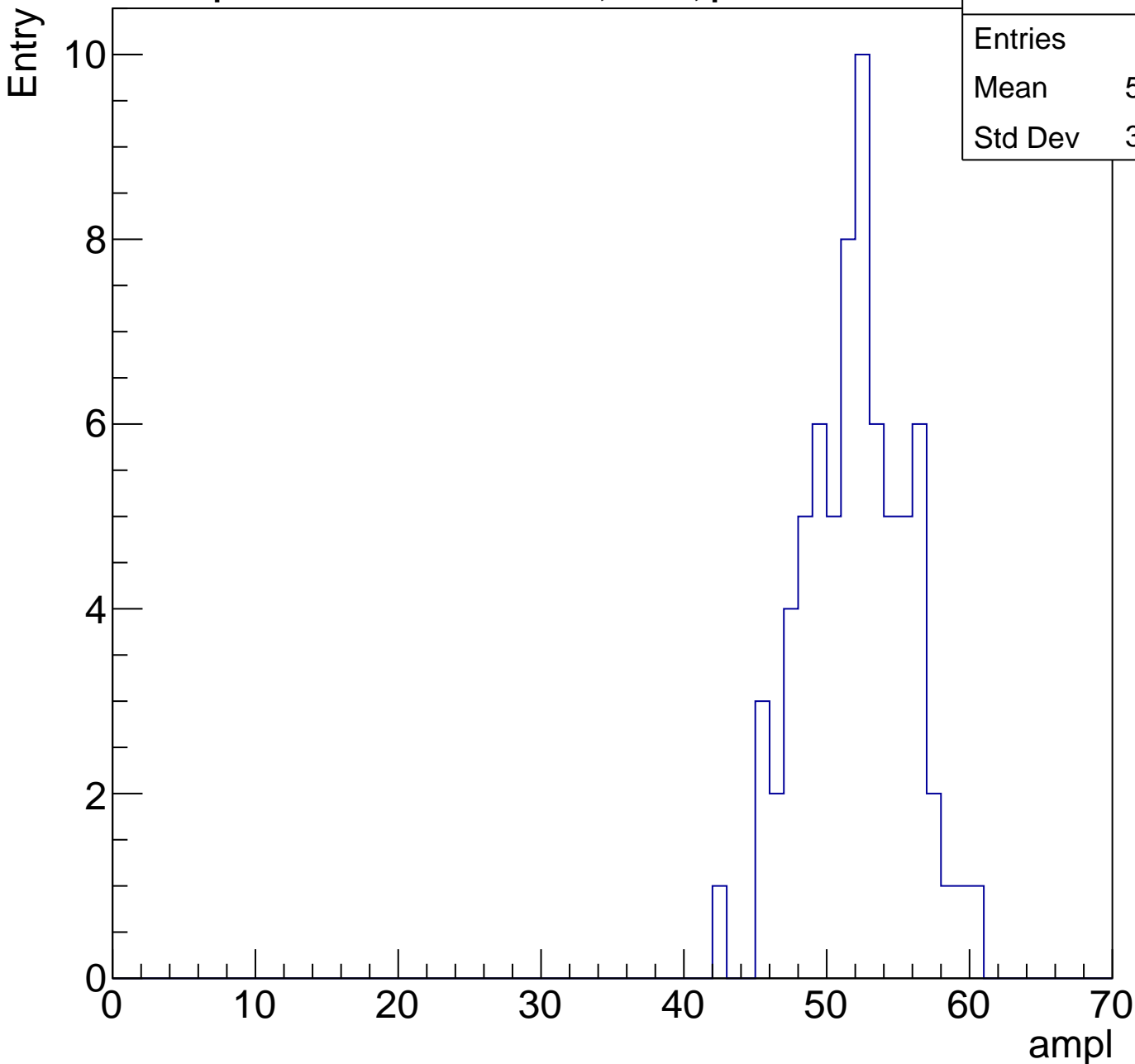
**Gaus Width: 3.5708**



# B1L103S, U9-ch37, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	71
Mean	51.54
Std Dev	3.622

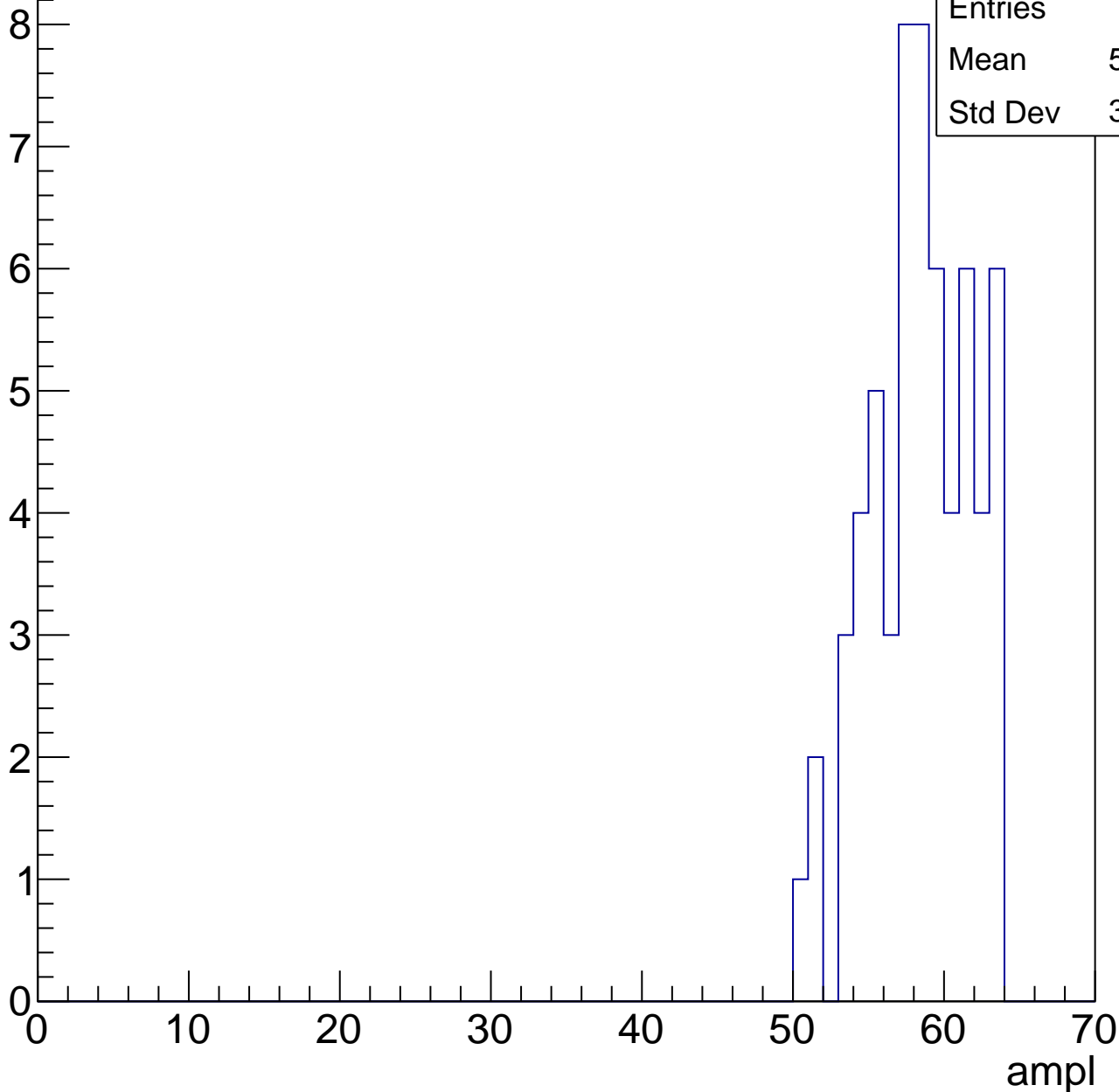


# B1L103S, U9-ch37, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	60
Mean	57.93
Std Dev	3.306

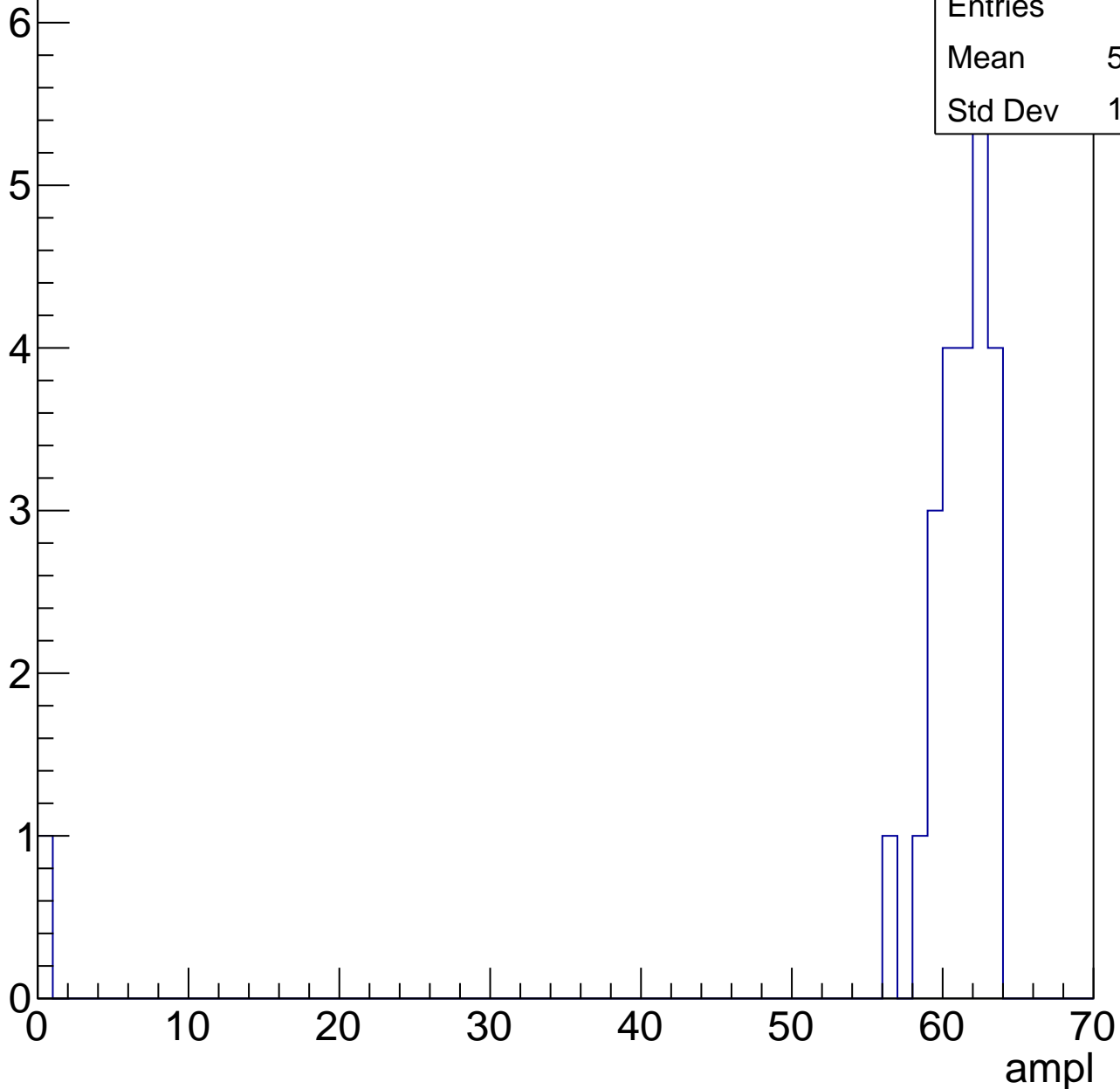


# B1L103S, U9-ch37, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	24
Mean	58.29
Std Dev	12.28



# B1L103S, U9-ch37, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U9-ch37, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	23
Std Dev	0

# B1L103S, U9-ch38, adc0

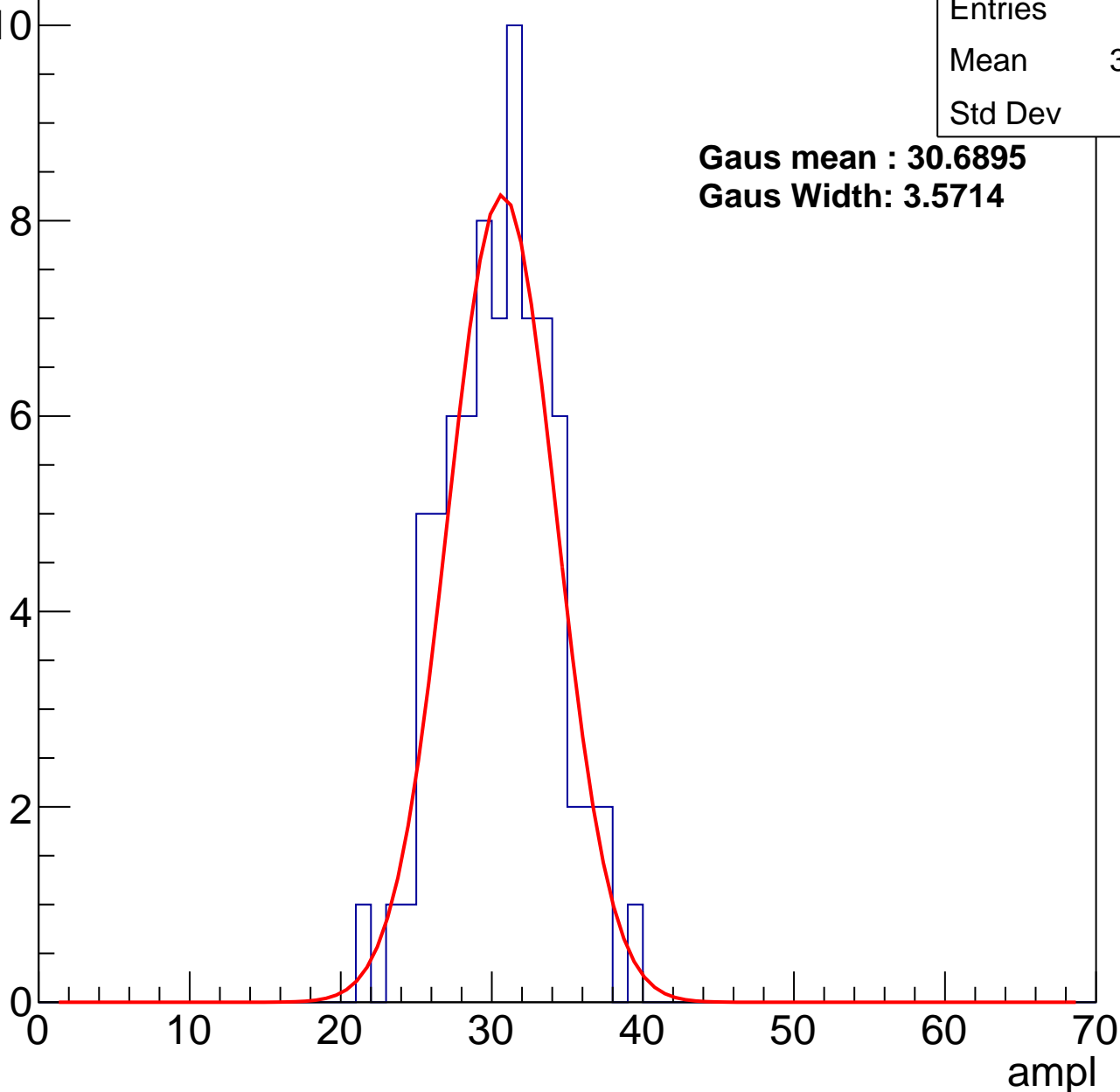
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	77
Mean	30.12
Std Dev	3.52

**Gaus mean : 30.6895**

**Gaus Width: 3.5714**



# B1L103S, U9-ch38, adc1

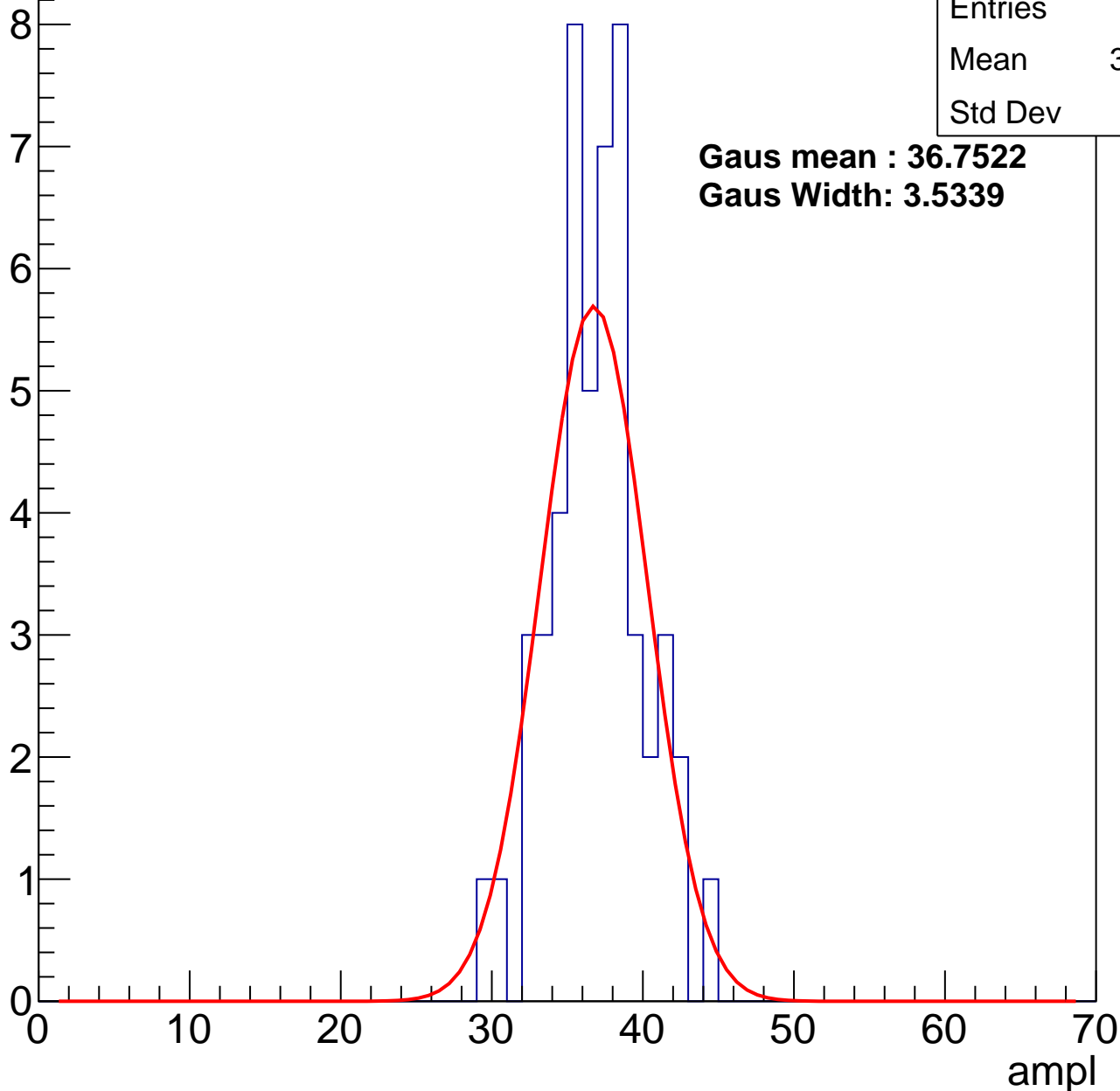
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	51
Mean	36.49
Std Dev	3.07

**Gaus mean : 36.7522**

**Gaus Width: 3.5339**



# B1L103S, U9-ch38, adc2

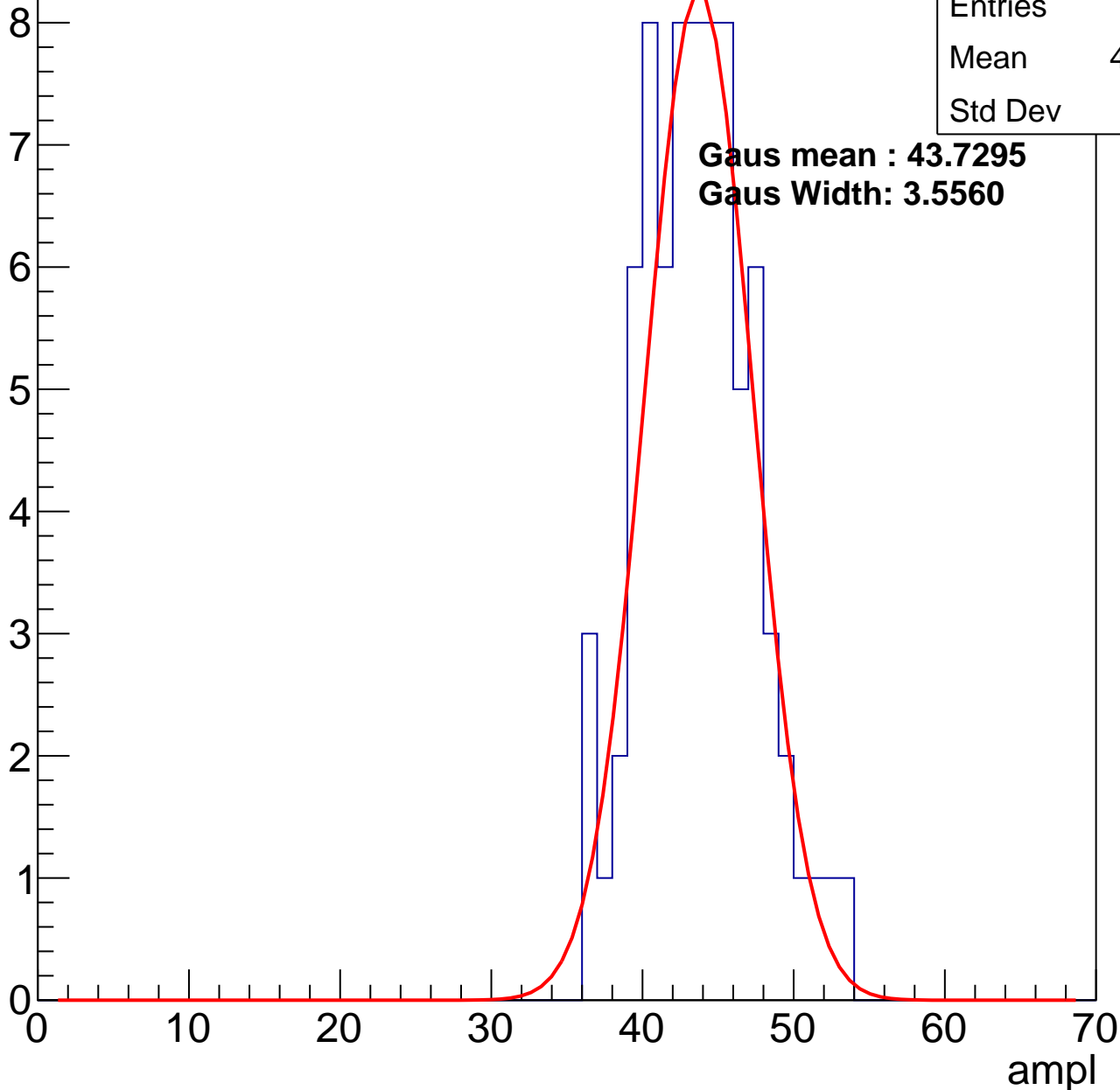
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	78
Mean	43.24
Std Dev	3.67

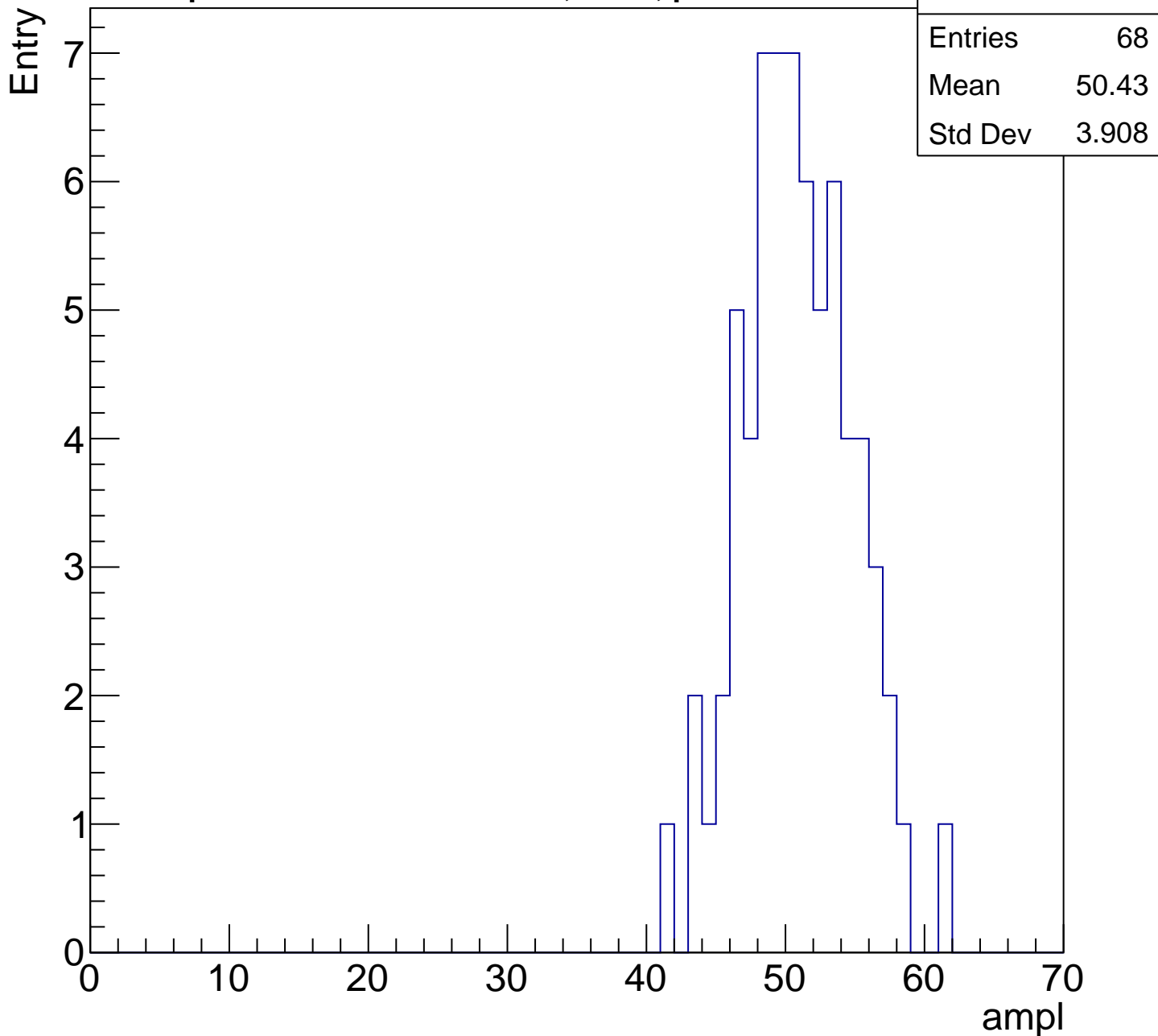
**Gaus mean : 43.7295**

**Gaus Width: 3.5560**



# B1L103S, U9-ch38, adc3

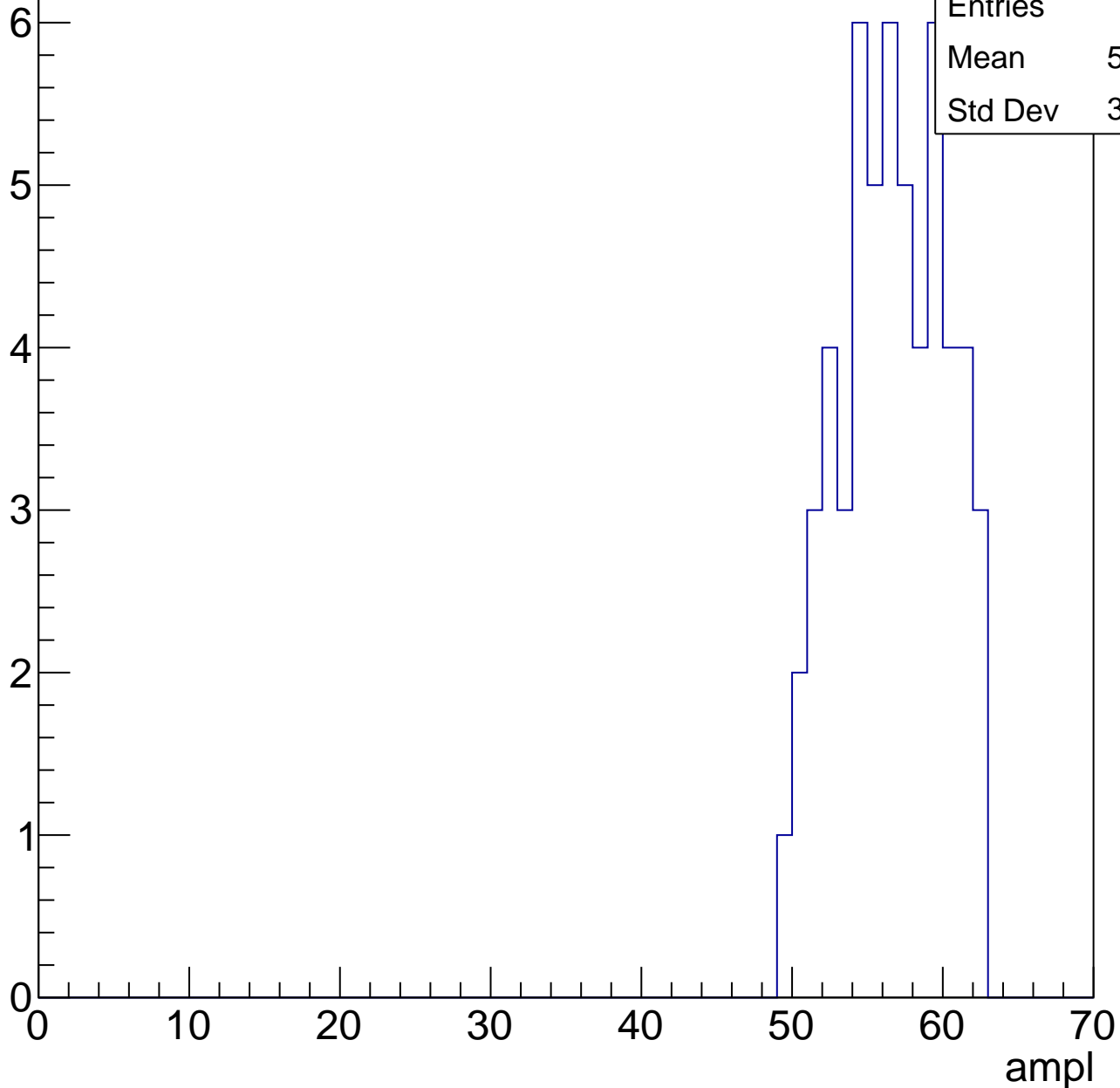
calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U9-ch38, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

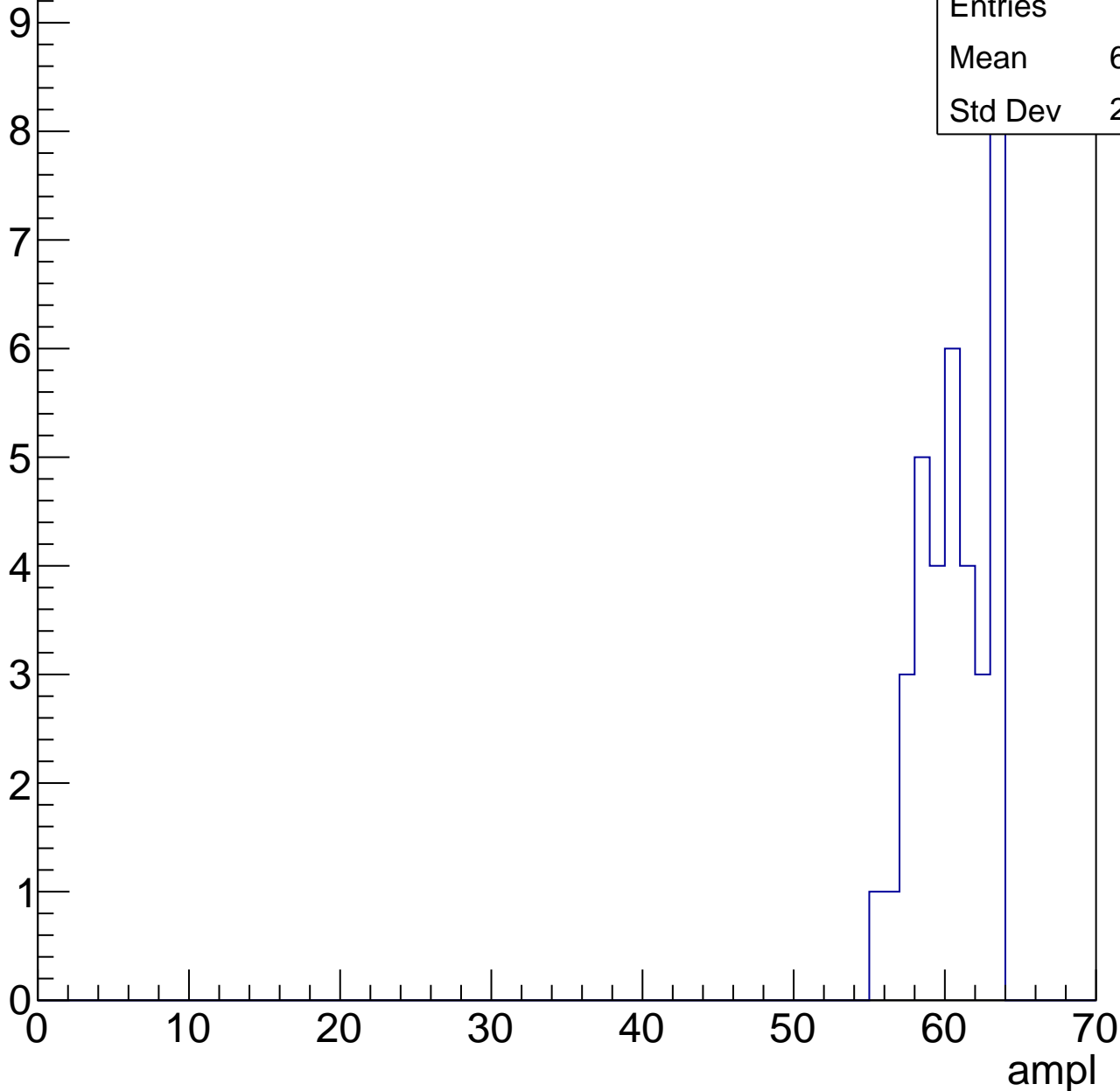


# B1L103S, U9-ch38, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

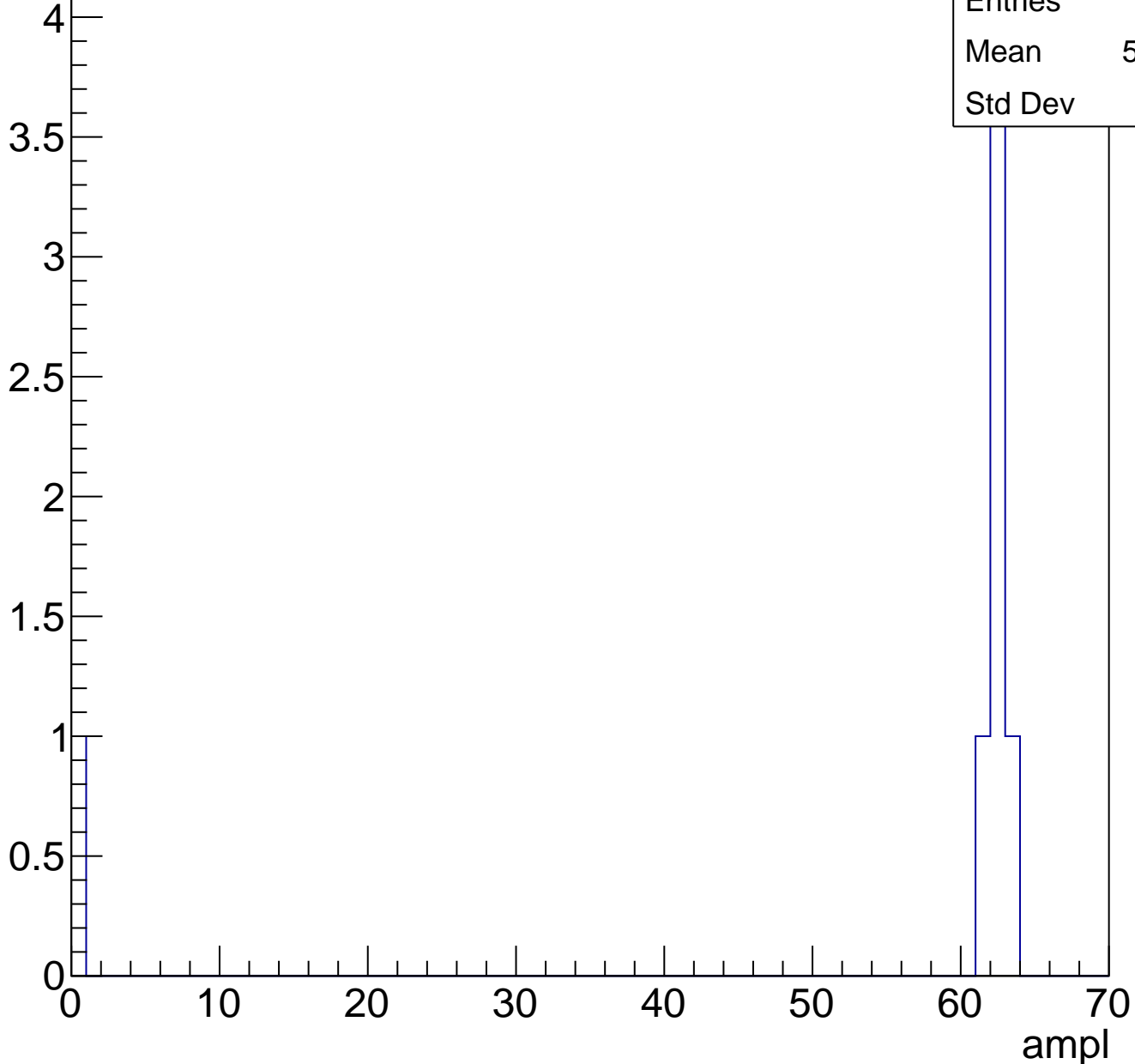
Entries	36
Mean	60.14
Std Dev	2.287



# B1L103S, U9-ch38, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U9-ch38, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U9-ch39, adc0

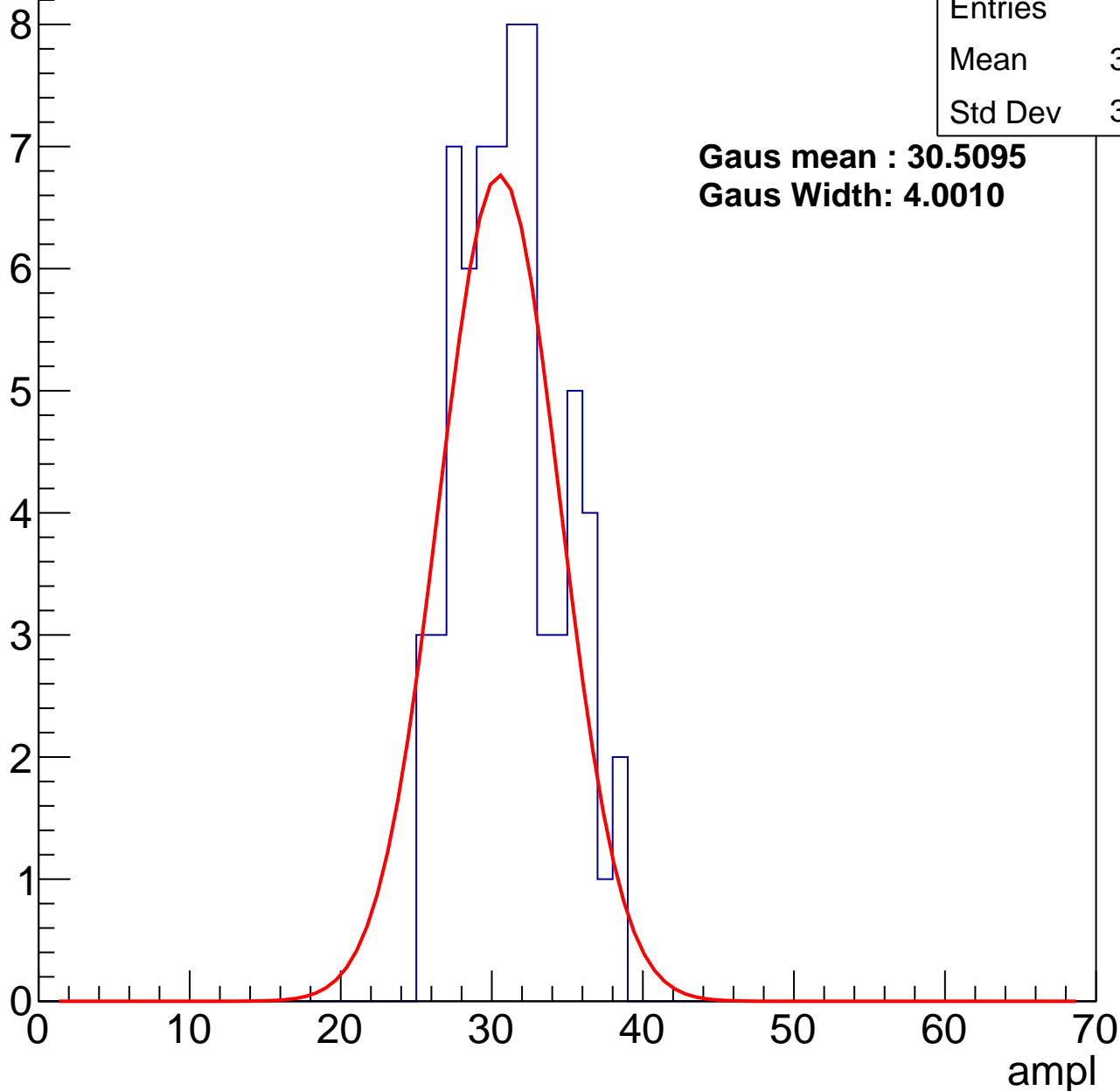
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	30.75
Std Dev	3.325

**Gaus mean : 30.5095**

**Gaus Width: 4.0010**



# B1L103S, U9-ch39, adc1

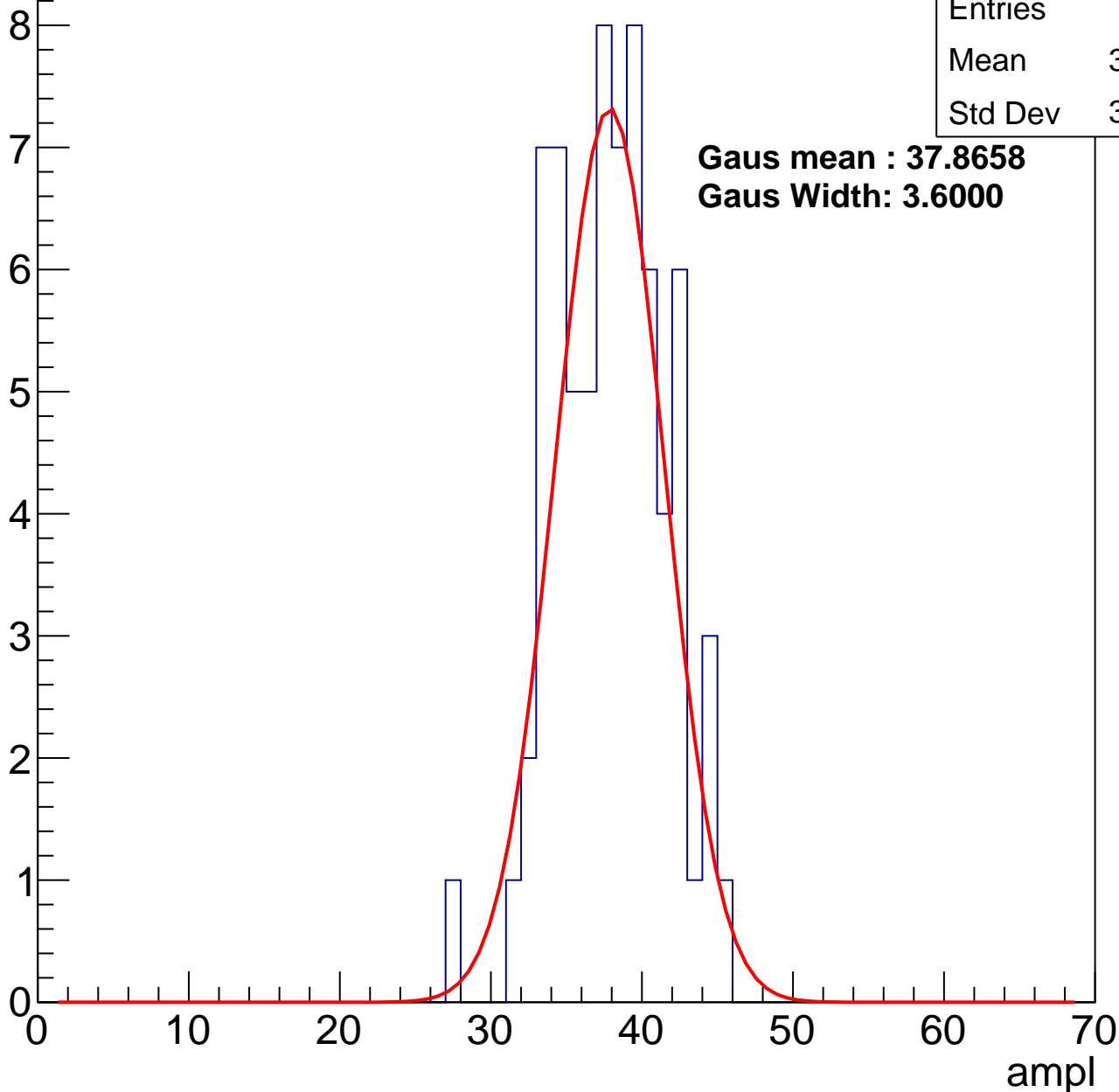
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	72
Mean	37.44
Std Dev	3.586

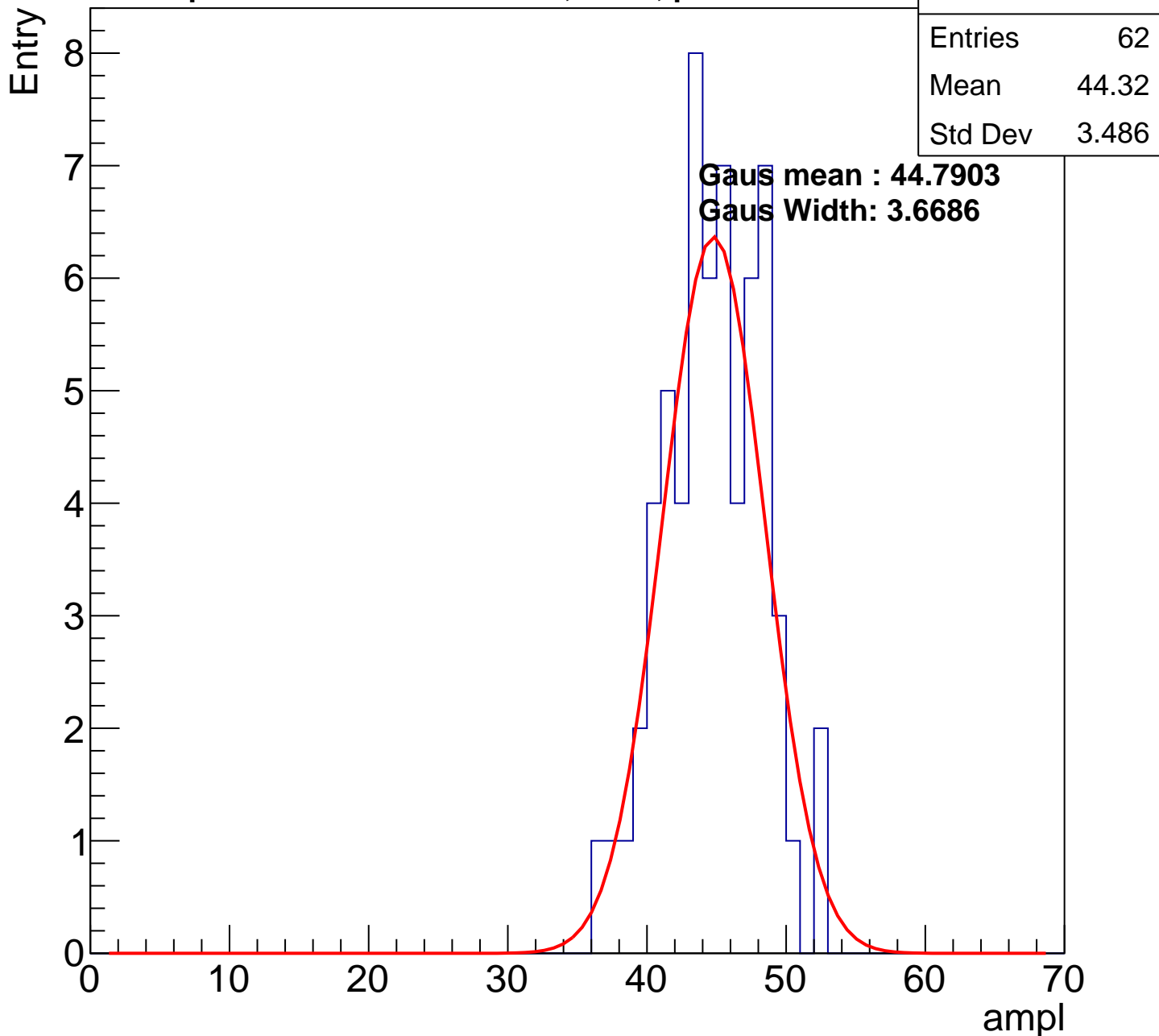
**Gaus mean : 37.8658**

**Gaus Width: 3.6000**



# B1L103S, U9-ch39, adc2

calib\_packv5\_042523\_0143.root, FC#7, port C2

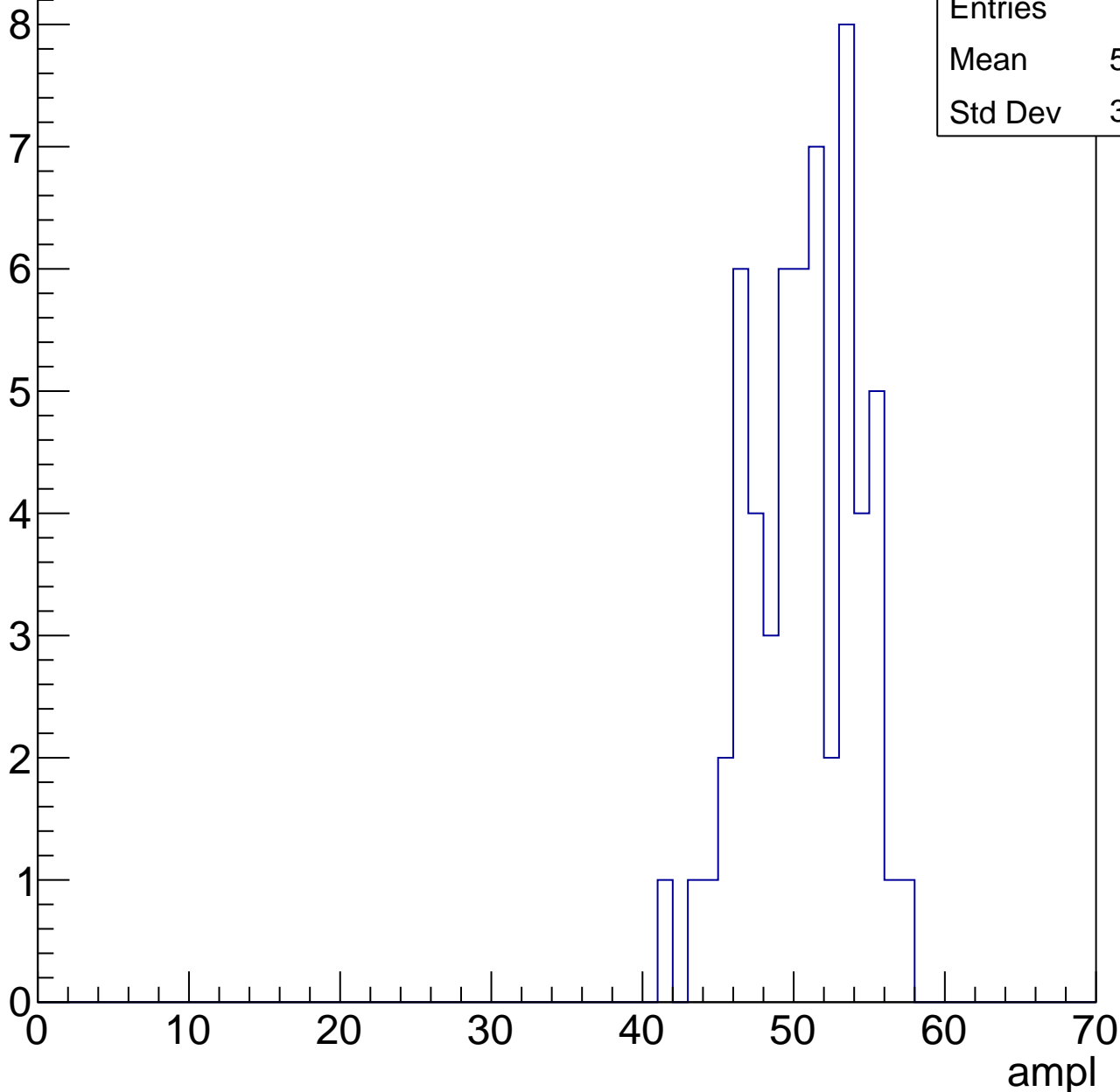


# B1L103S, U9-ch39, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	58
Mean	50.16
Std Dev	3.537

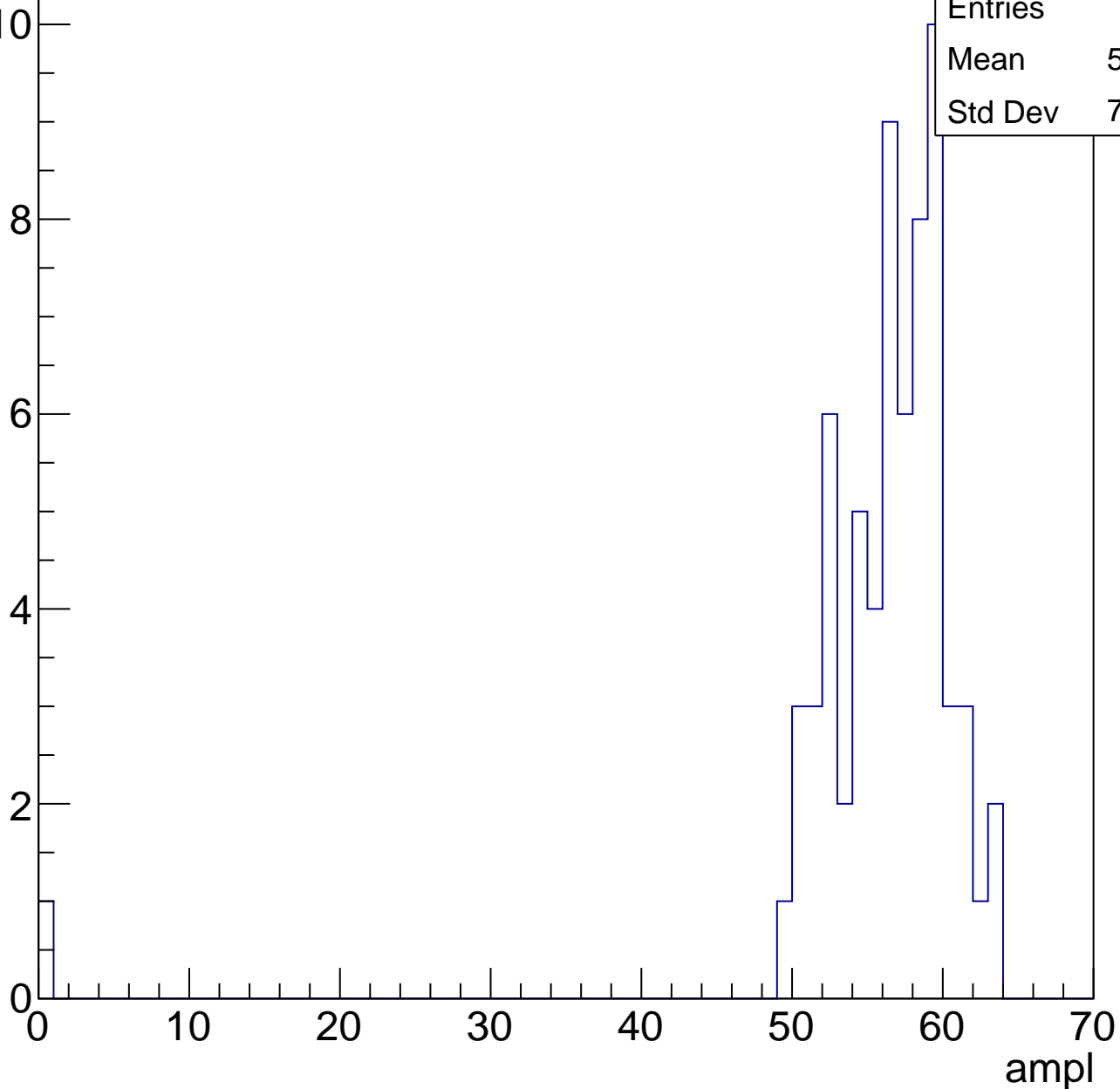


# B1L103S, U9-ch39, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	55.39
Std Dev	7.596

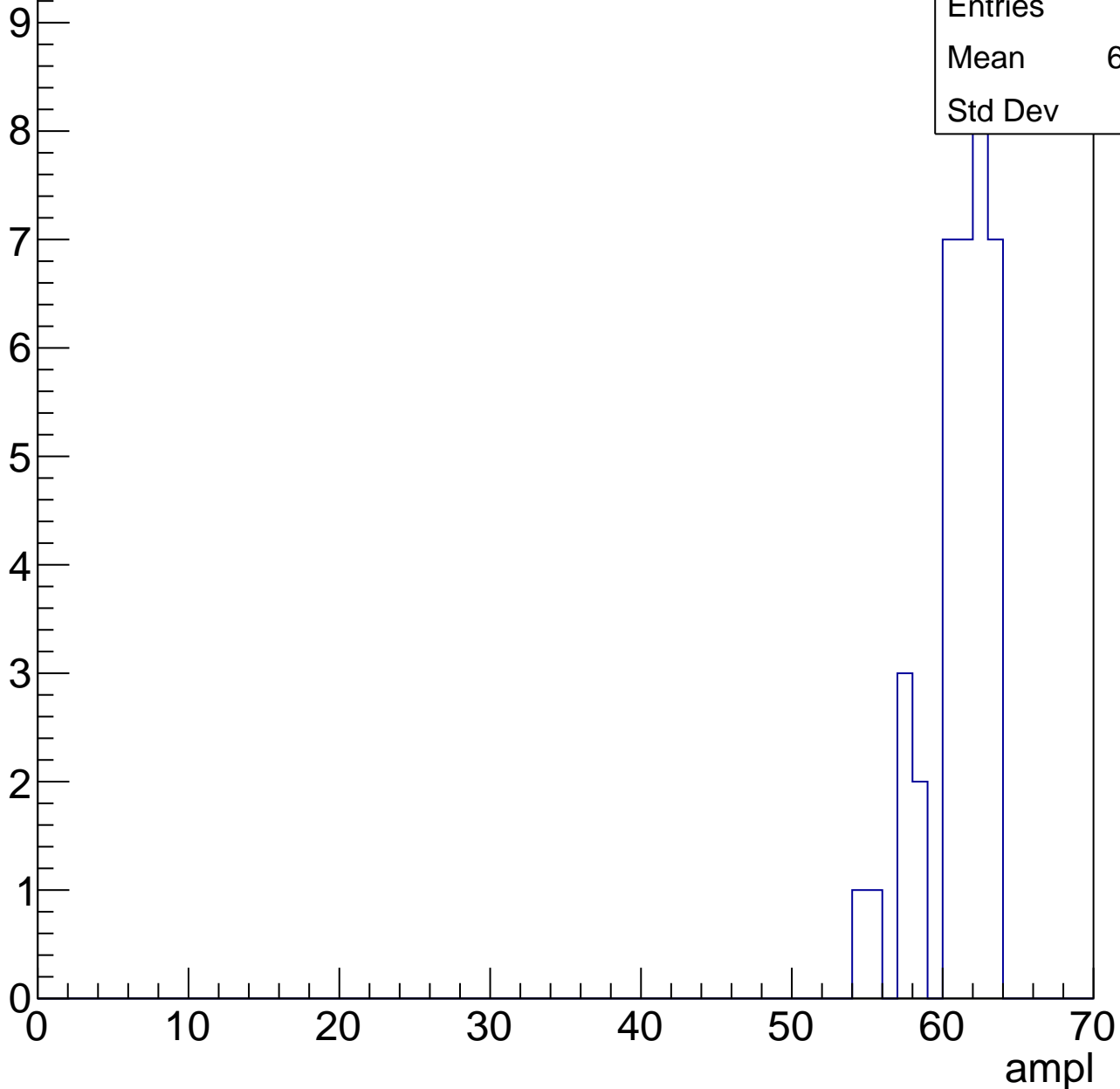


# B1L103S, U9-ch39, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	37
Mean	60.59
Std Dev	2.26



# B1L103S, U9-ch39, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U9-ch39, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U9-ch40, adc0

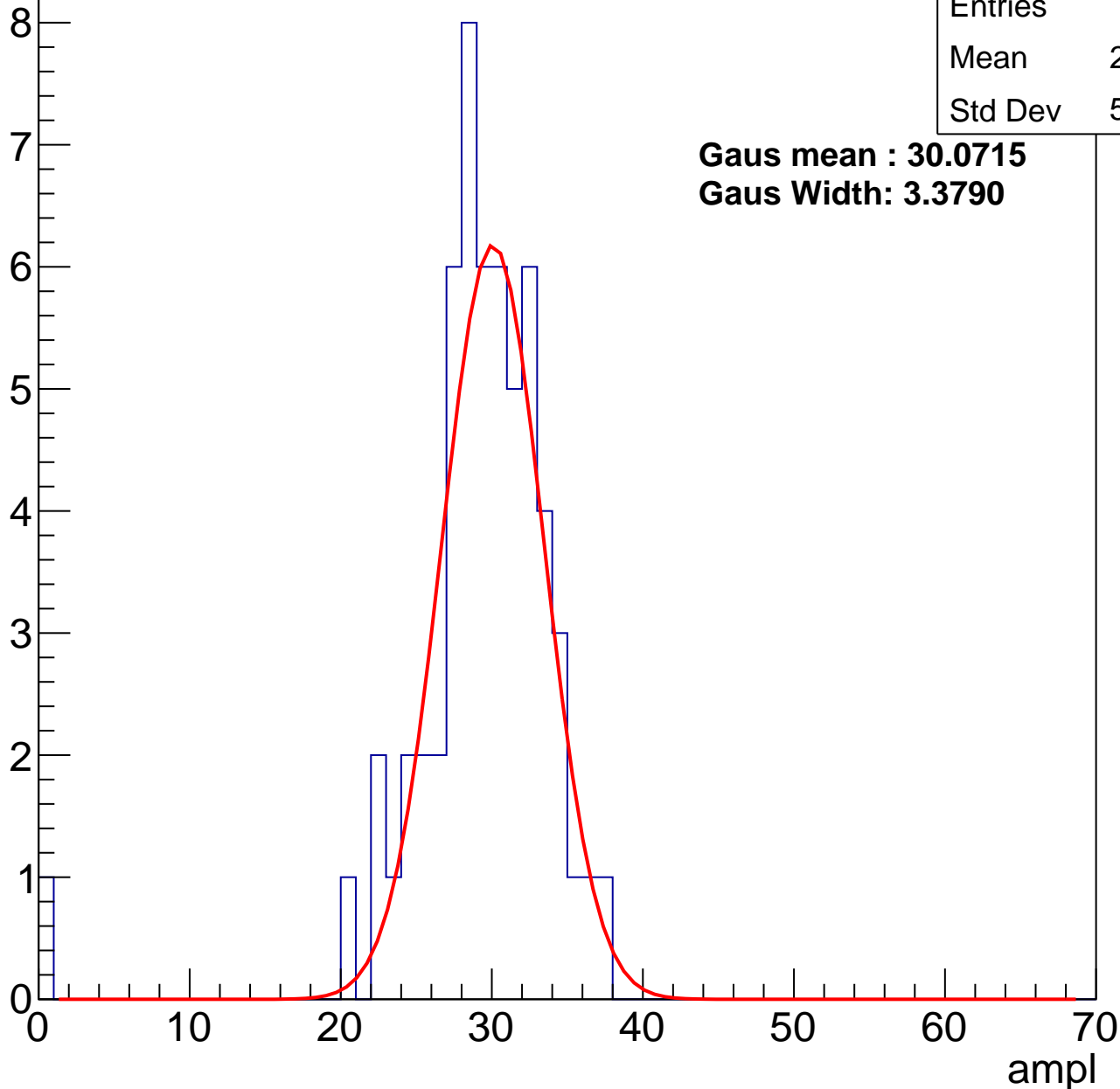
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	58
Mean	28.72
Std Dev	5.172

**Gaus mean : 30.0715**

**Gaus Width: 3.3790**



# B1L103S, U9-ch40, adc1

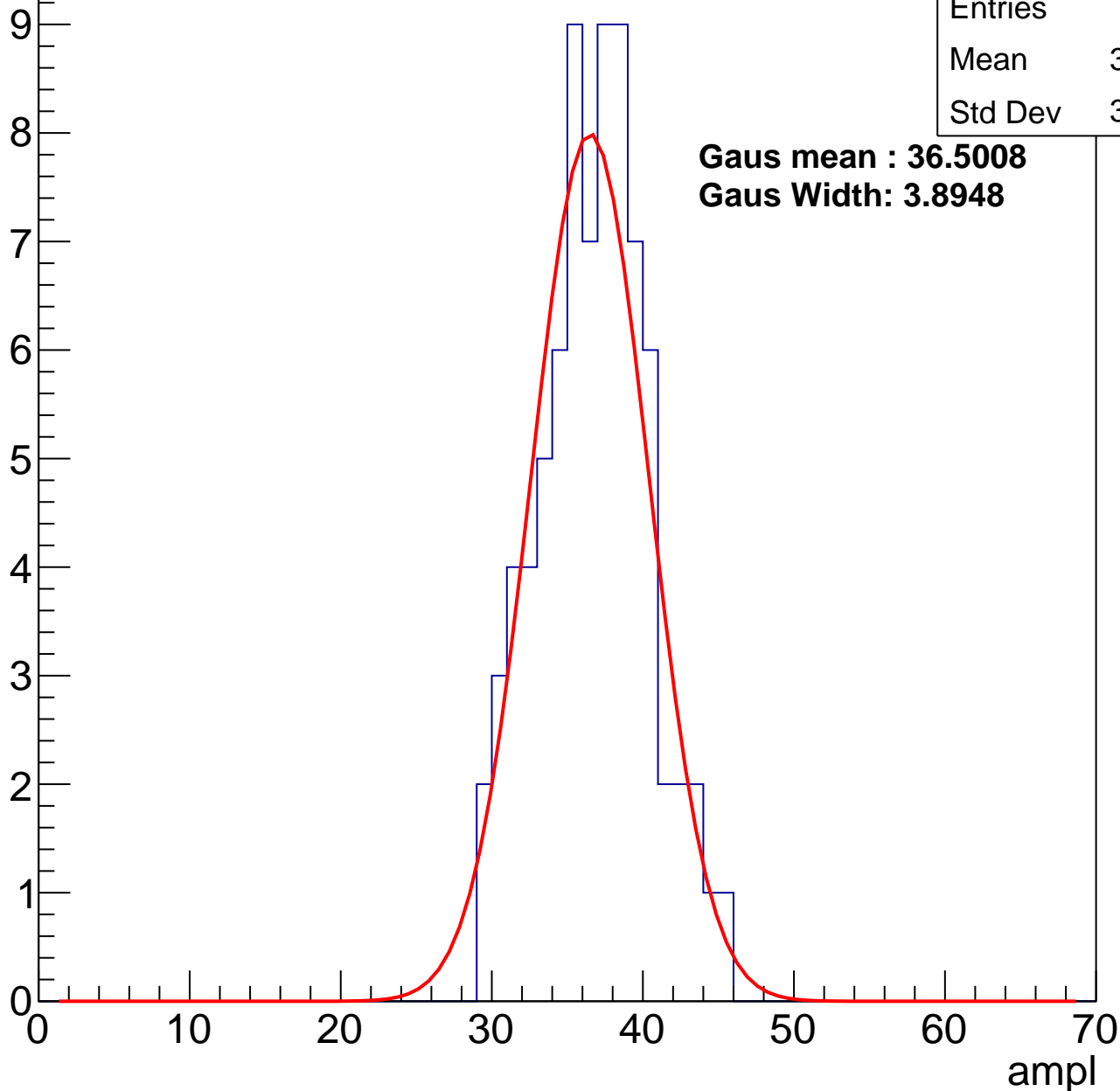
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	79
Mean	36.27
Std Dev	3.578

**Gaus mean : 36.5008**

**Gaus Width: 3.8948**



# B1L103S, U9-ch40, adc2

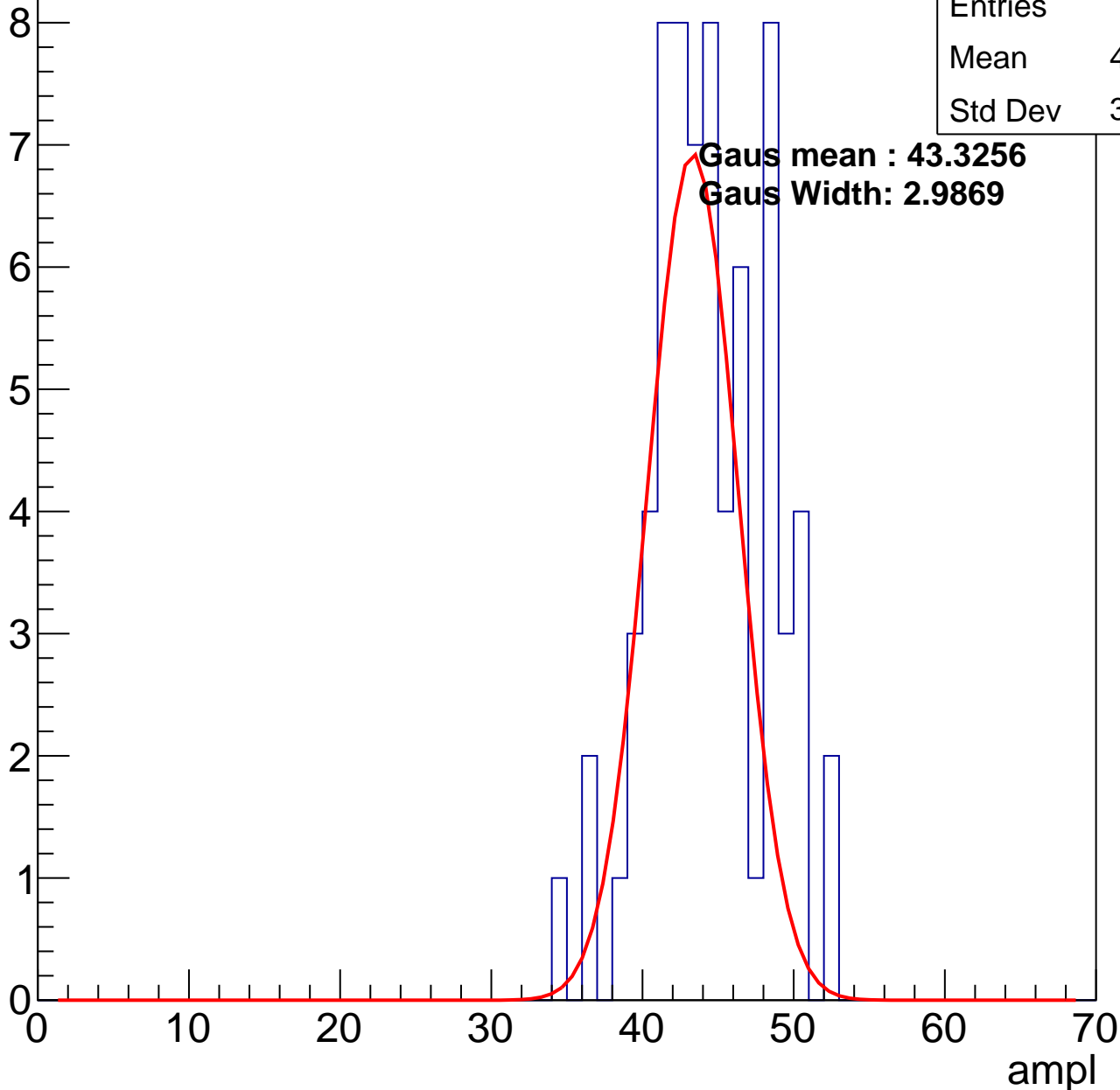
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	70
Mean	43.94
Std Dev	3.828

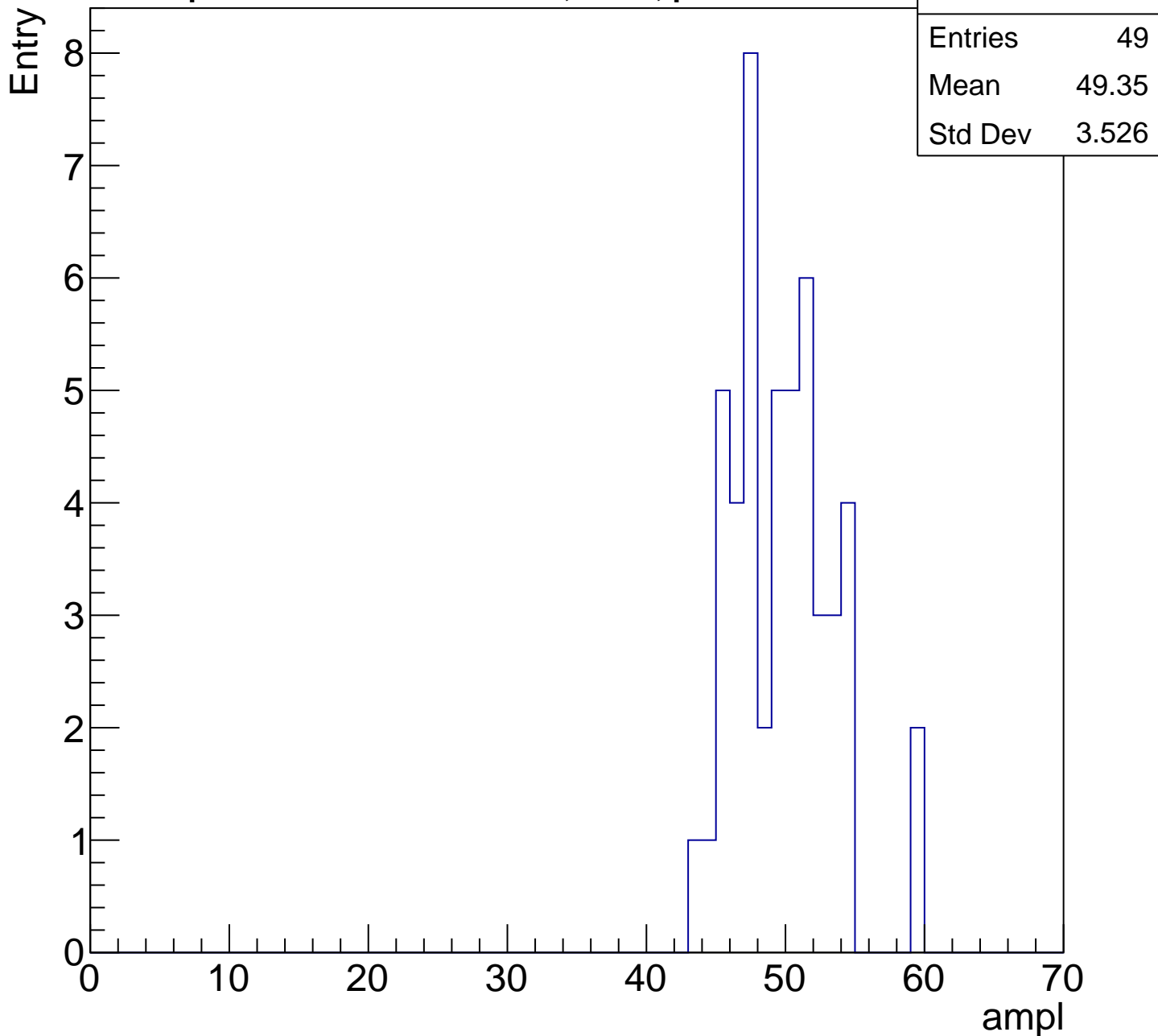
Gaus mean : 43.3256

Gaus Width: 2.9869



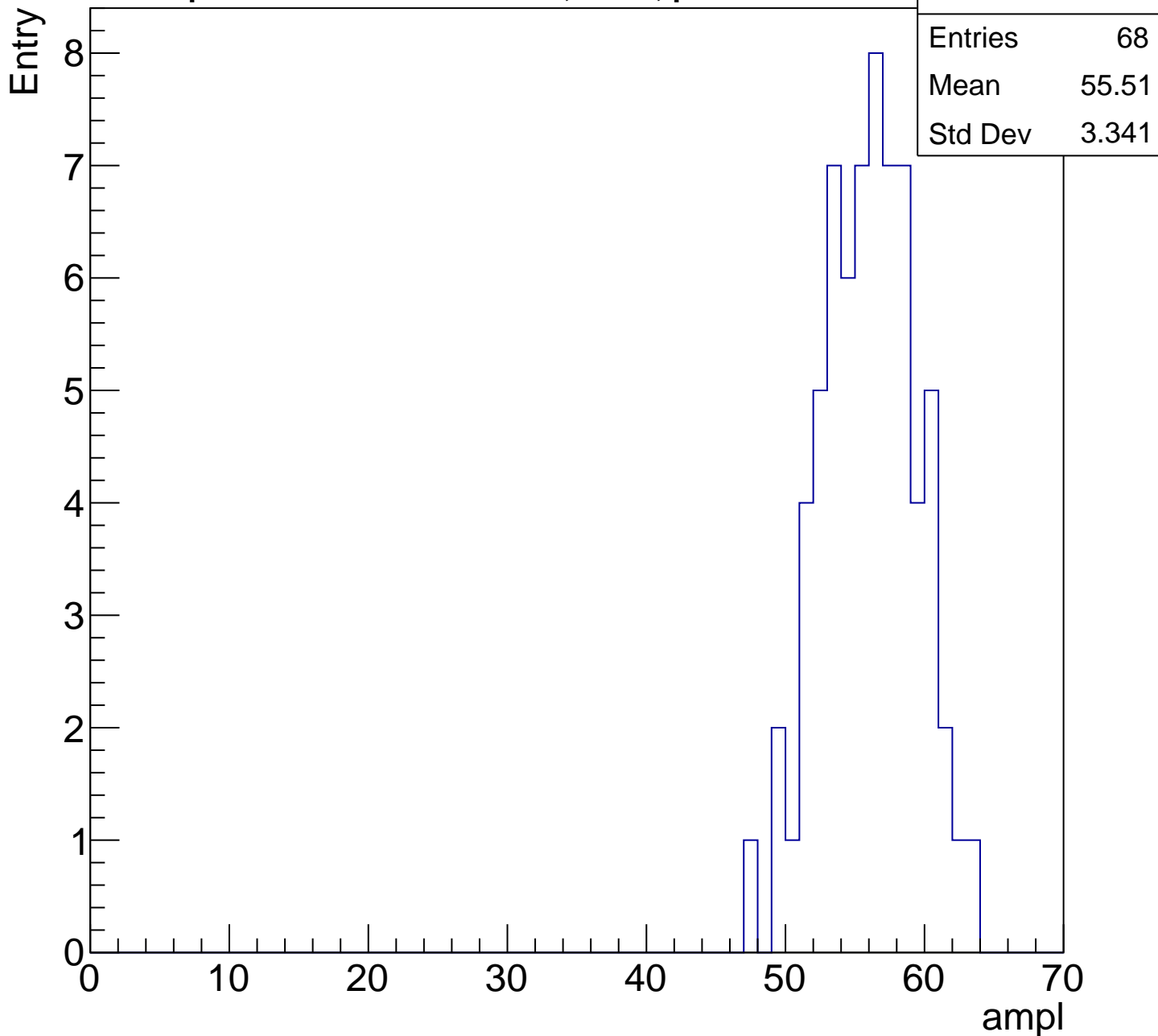
# B1L103S, U9-ch40, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U9-ch40, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

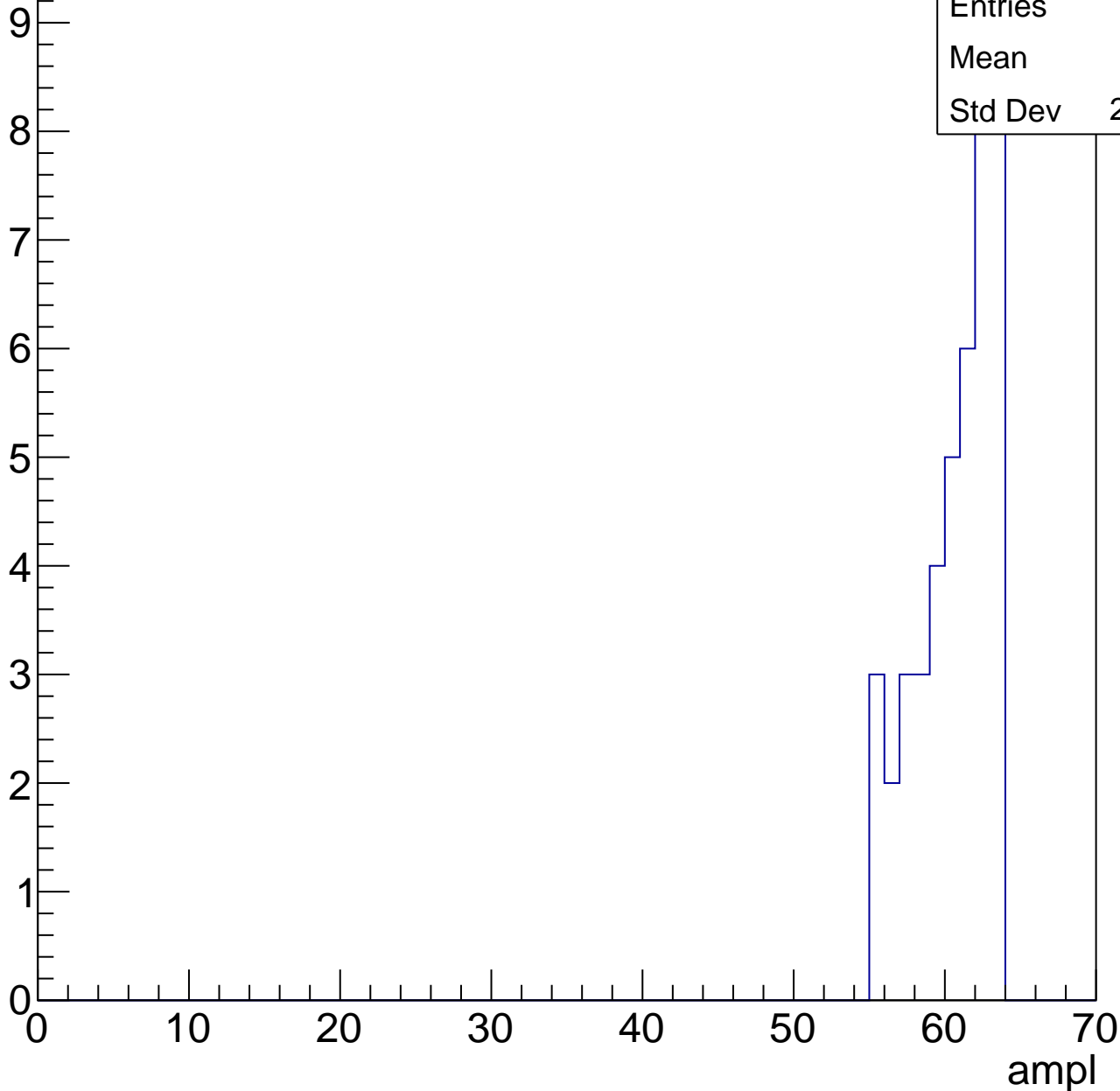


# B1L103S, U9-ch40, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

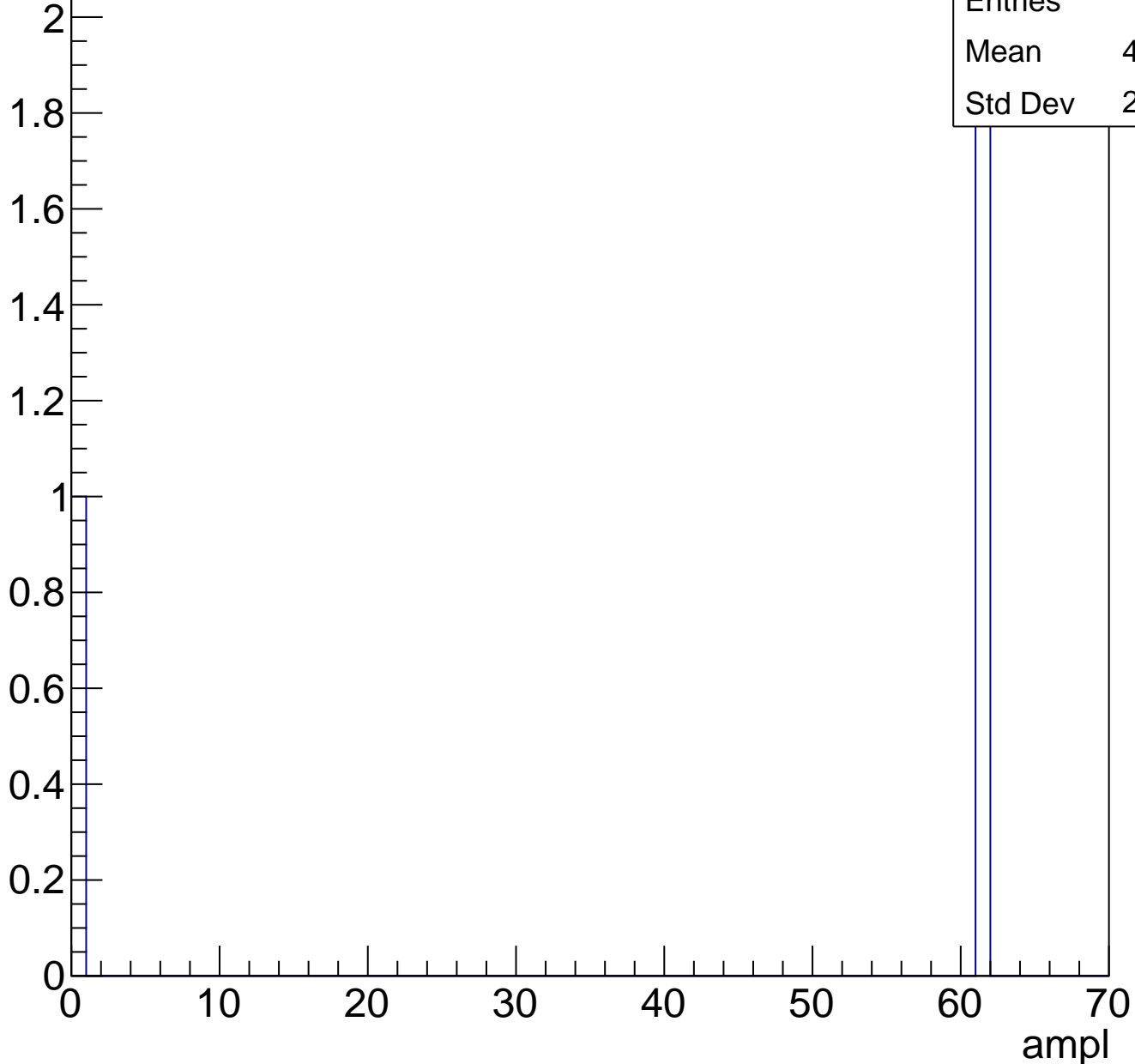
Entries	44
Mean	60.2
Std Dev	2.482



# B1L103S, U9-ch40, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U9-ch40, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L103S, U9-ch41, adc0

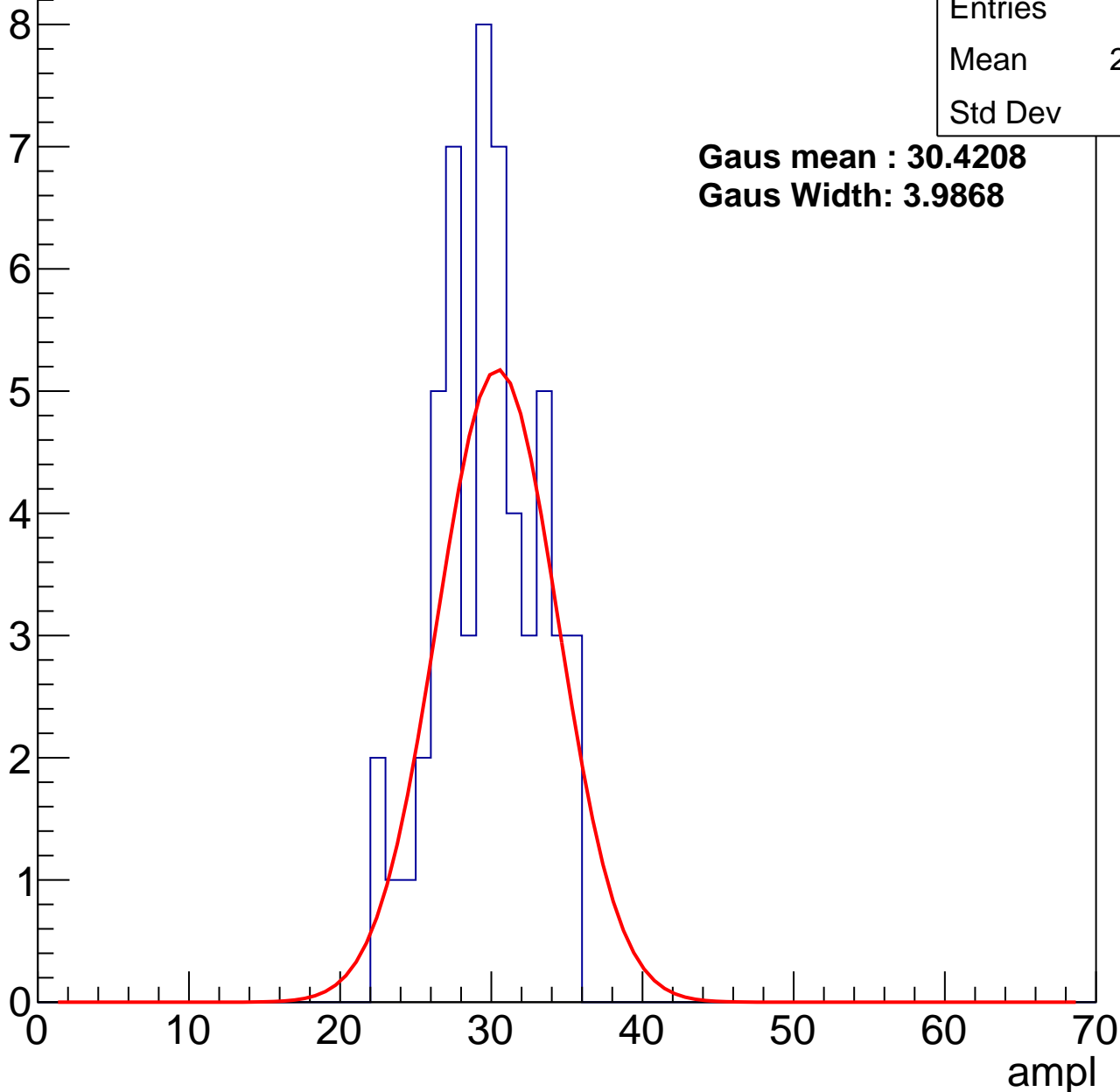
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	54
Mean	29.22
Std Dev	3.27

**Gaus mean : 30.4208**

**Gaus Width: 3.9868**



# B1L103S, U9-ch41, adc1

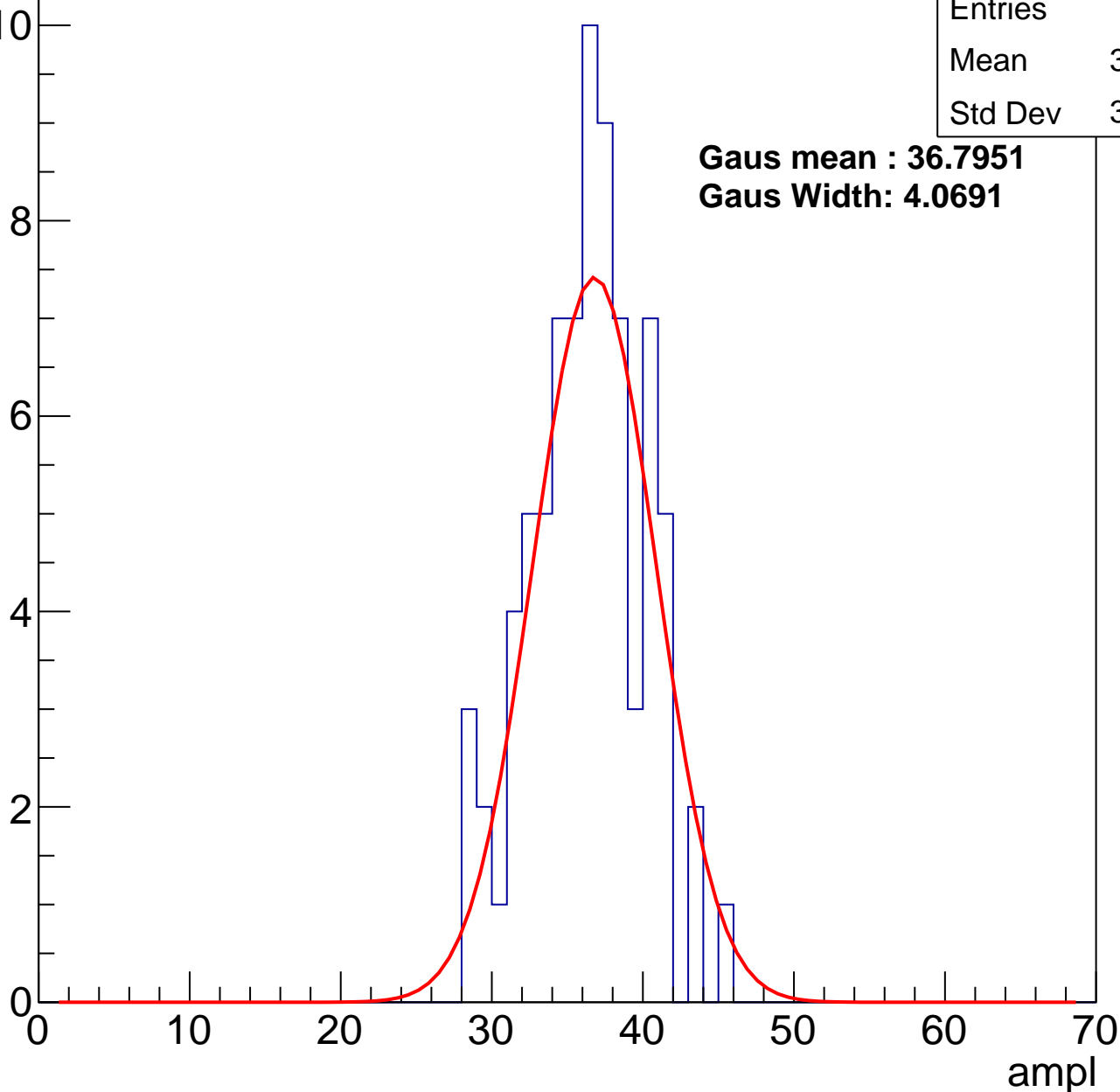
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	78
Mean	35.85
Std Dev	3.694

**Gaus mean : 36.7951**

**Gaus Width: 4.0691**



# B1L103S, U9-ch41, adc2

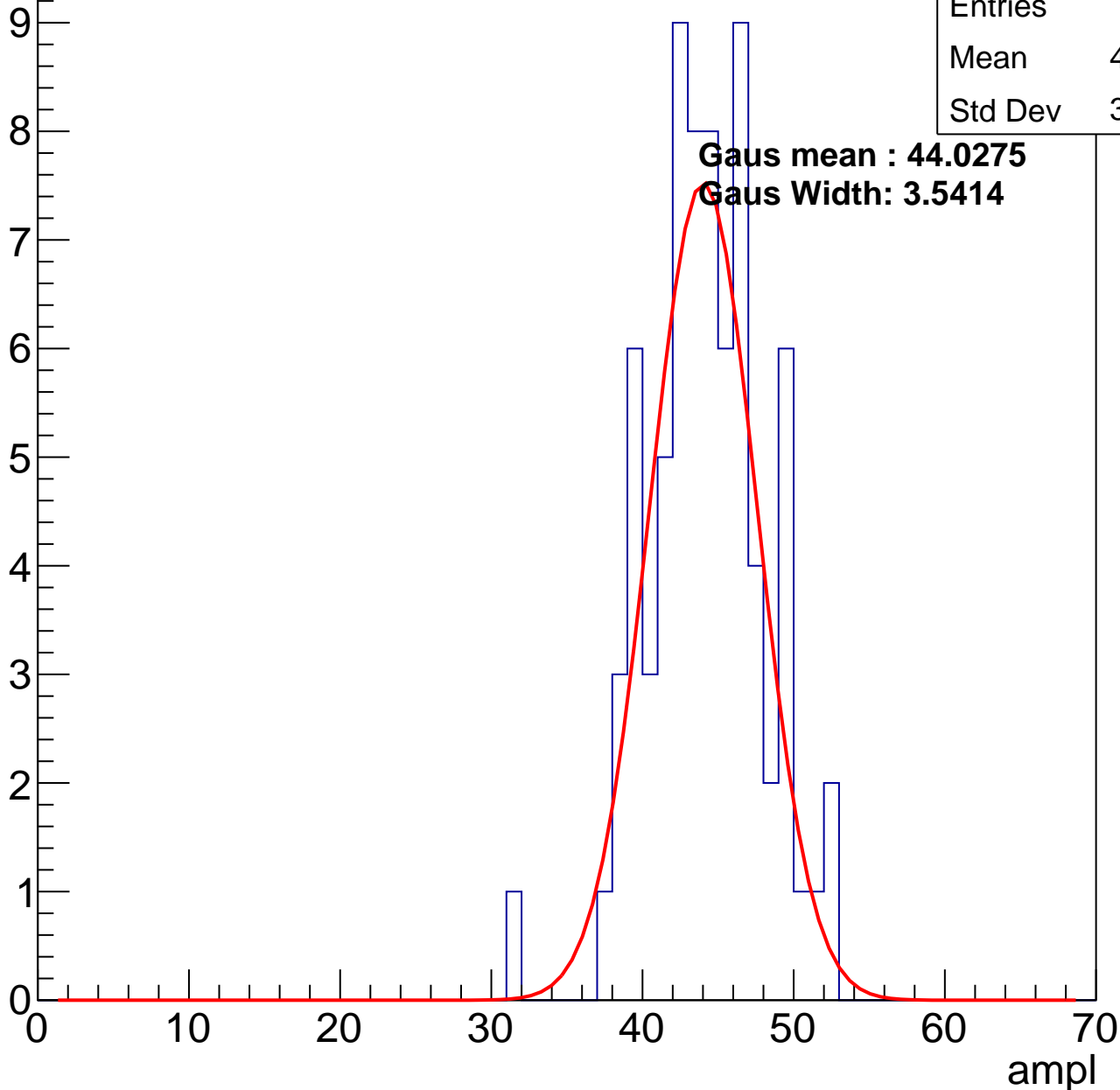
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	75
Mean	43.76
Std Dev	3.798

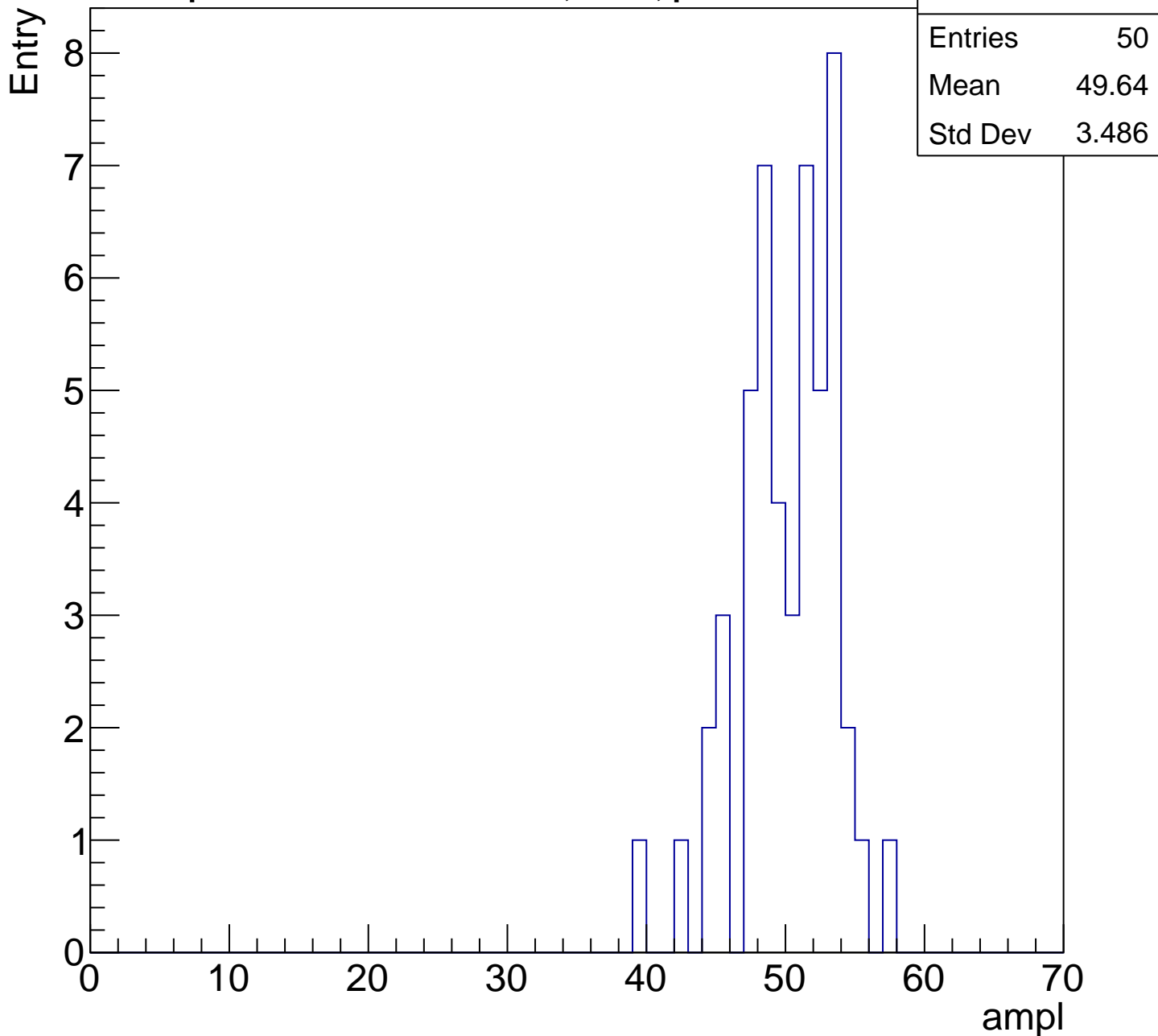
**Gaus mean : 44.0275**

**Gaus Width: 3.5414**



# B1L103S, U9-ch41, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

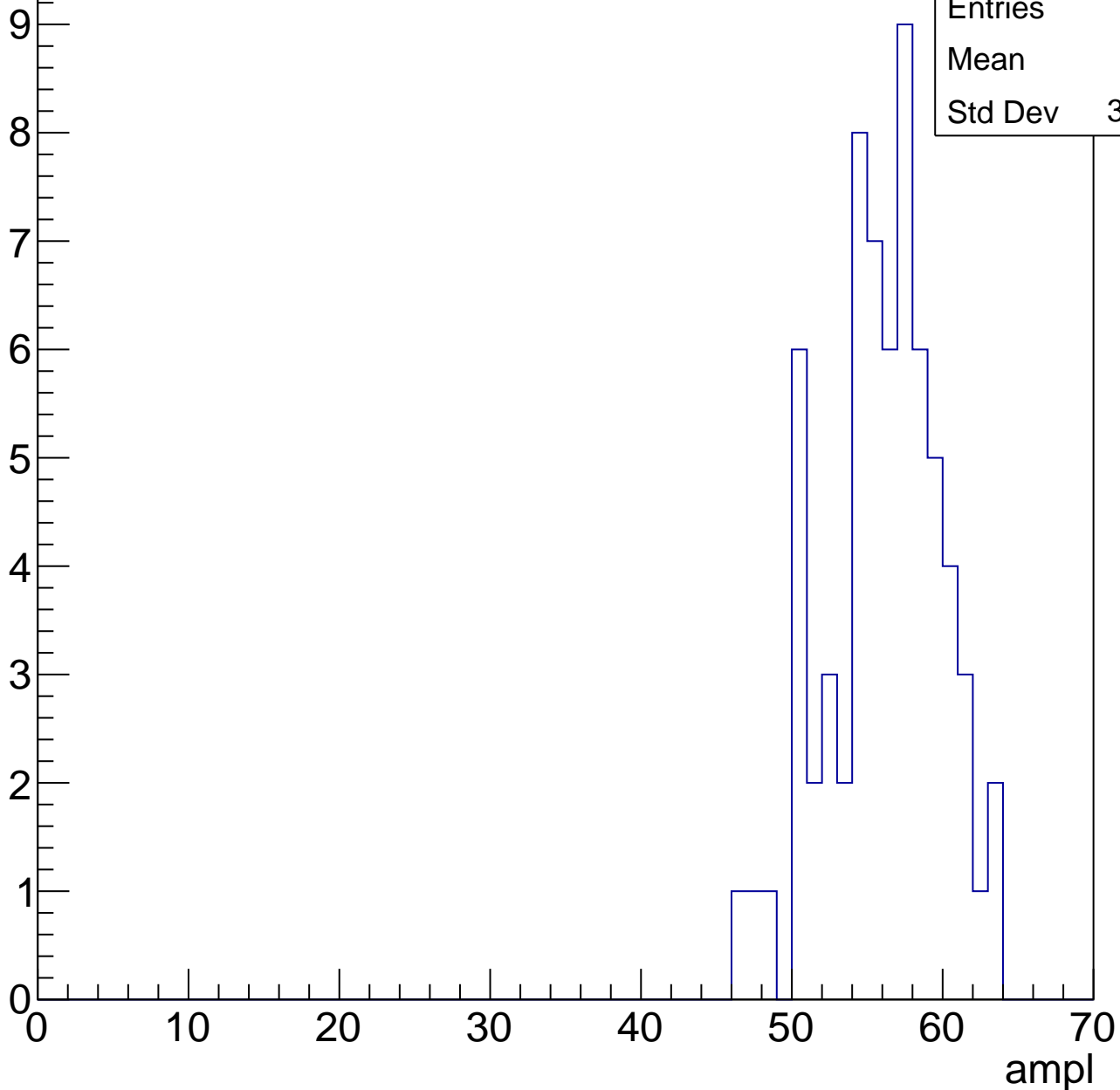


# B1L103S, U9-ch41, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

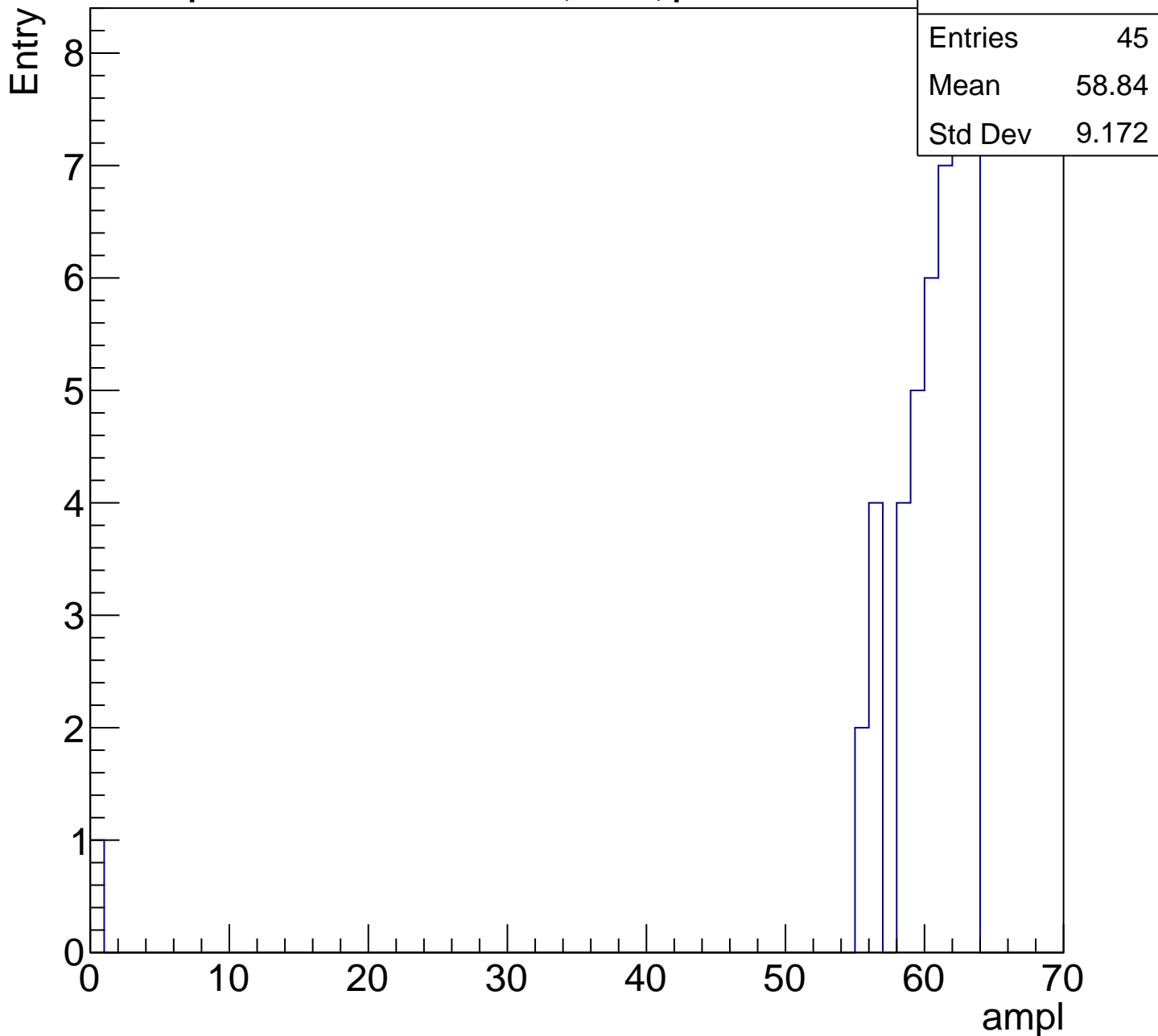
Entry

Entries	67
Mean	55.6
Std Dev	3.778



# B1L103S, U9-ch41, adc5

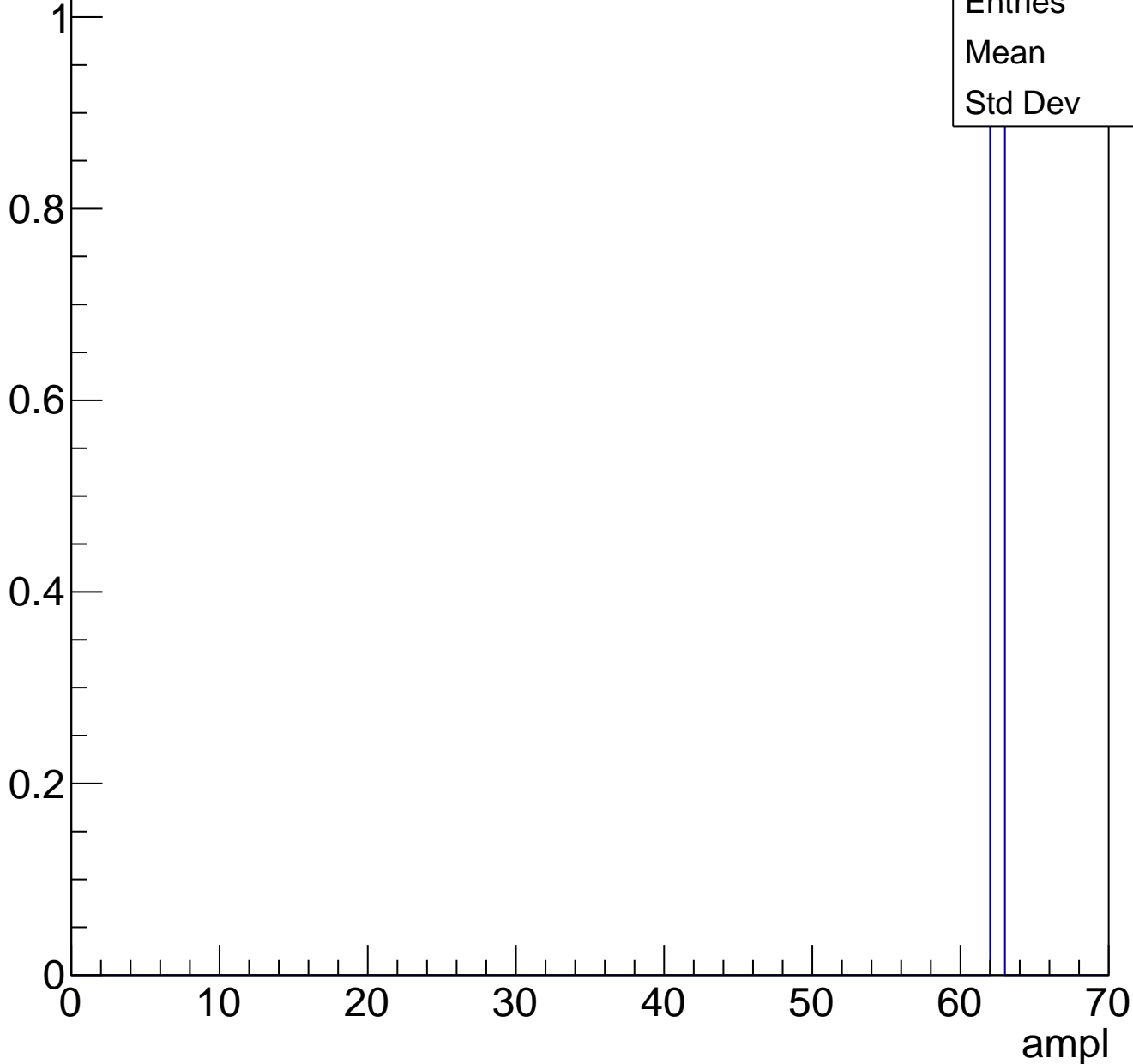
calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U9-ch41, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U9-ch41, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U9-ch42, adc0

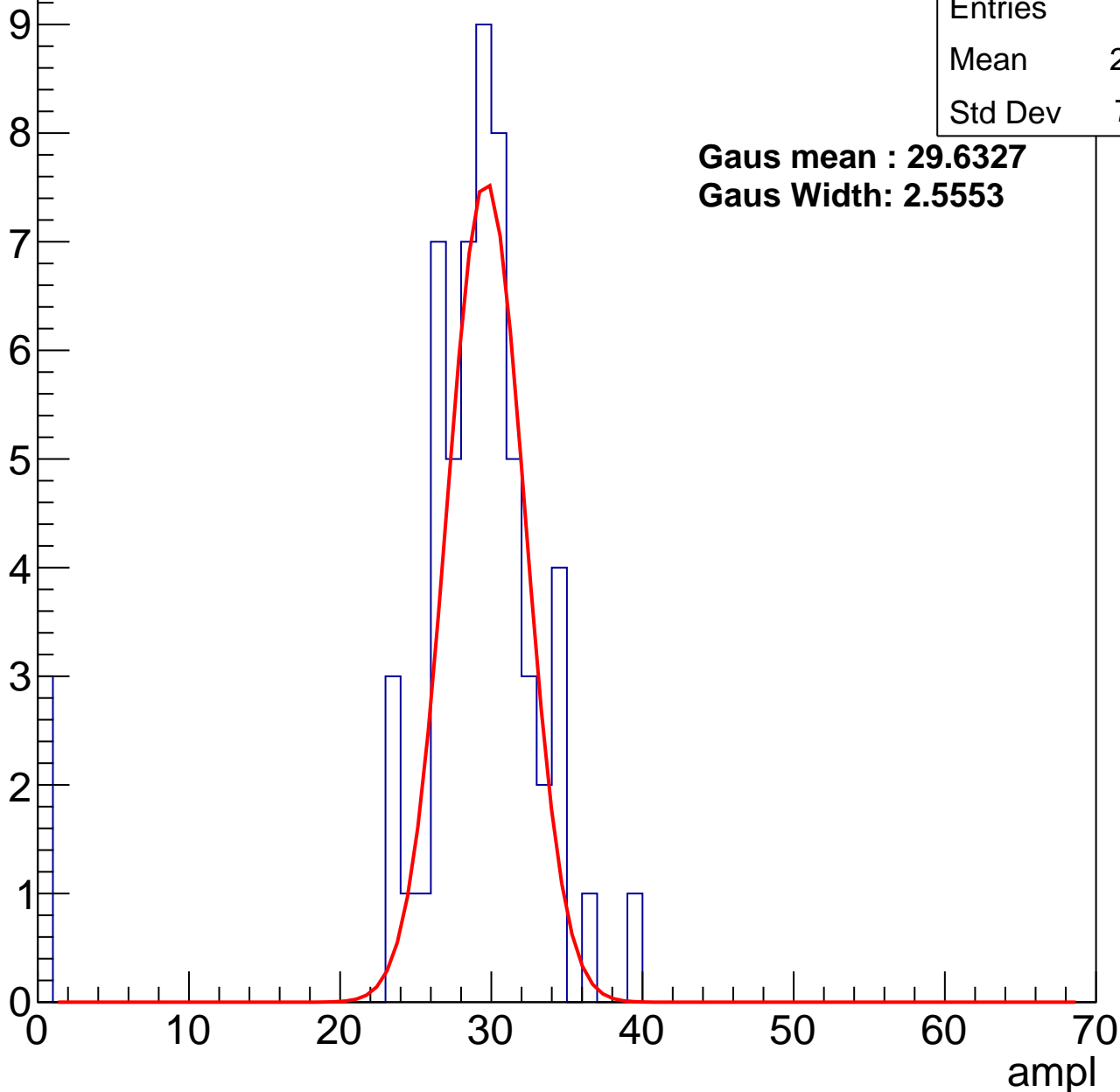
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	60
Mean	27.67
Std Dev	7.061

**Gaus mean : 29.6327**

**Gaus Width: 2.5553**



# B1L103S, U9-ch42, adc1

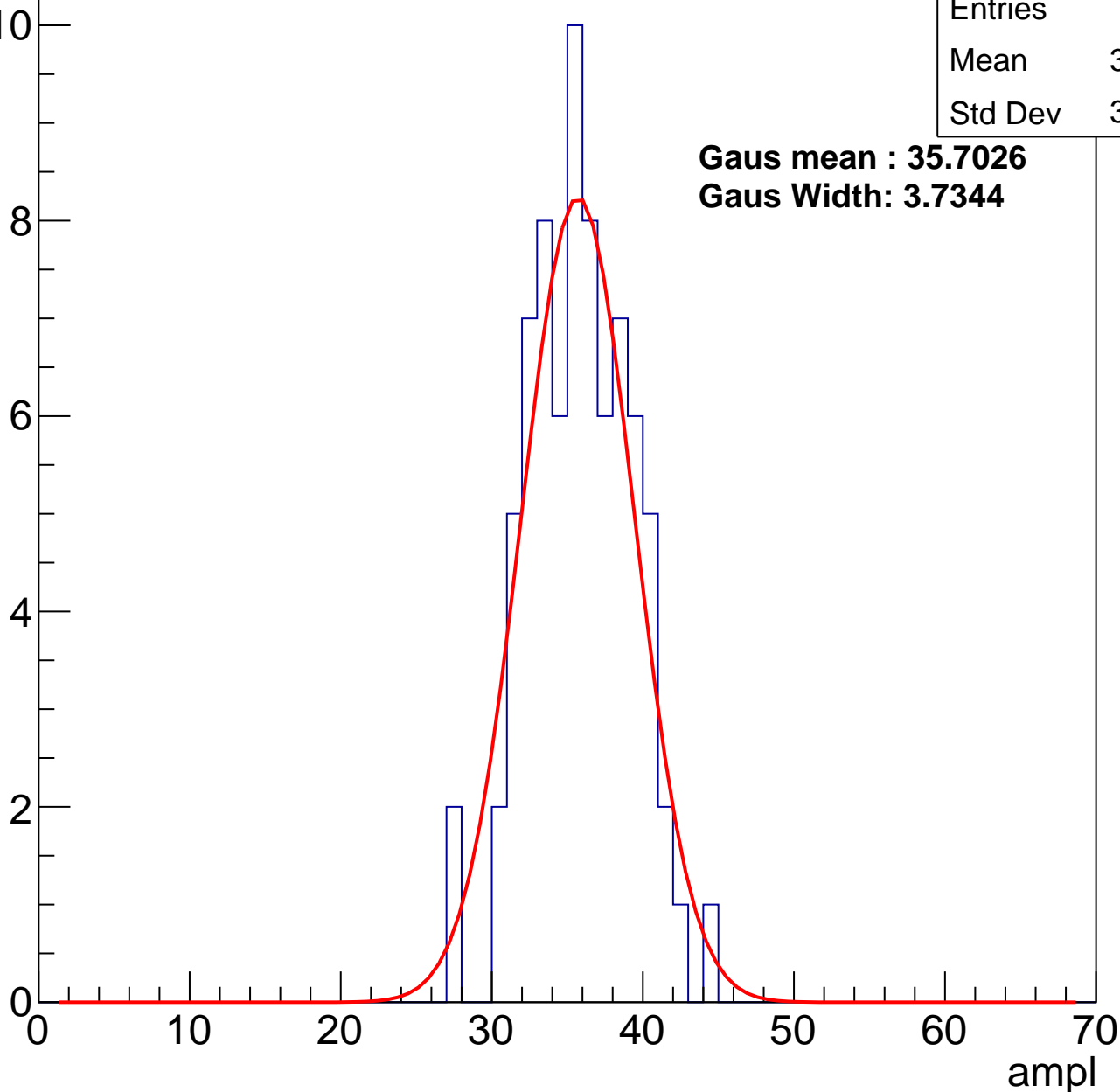
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	76
Mean	35.38
Std Dev	3.375

**Gaus mean : 35.7026**

**Gaus Width: 3.7344**



# B1L103S, U9-ch42, adc2

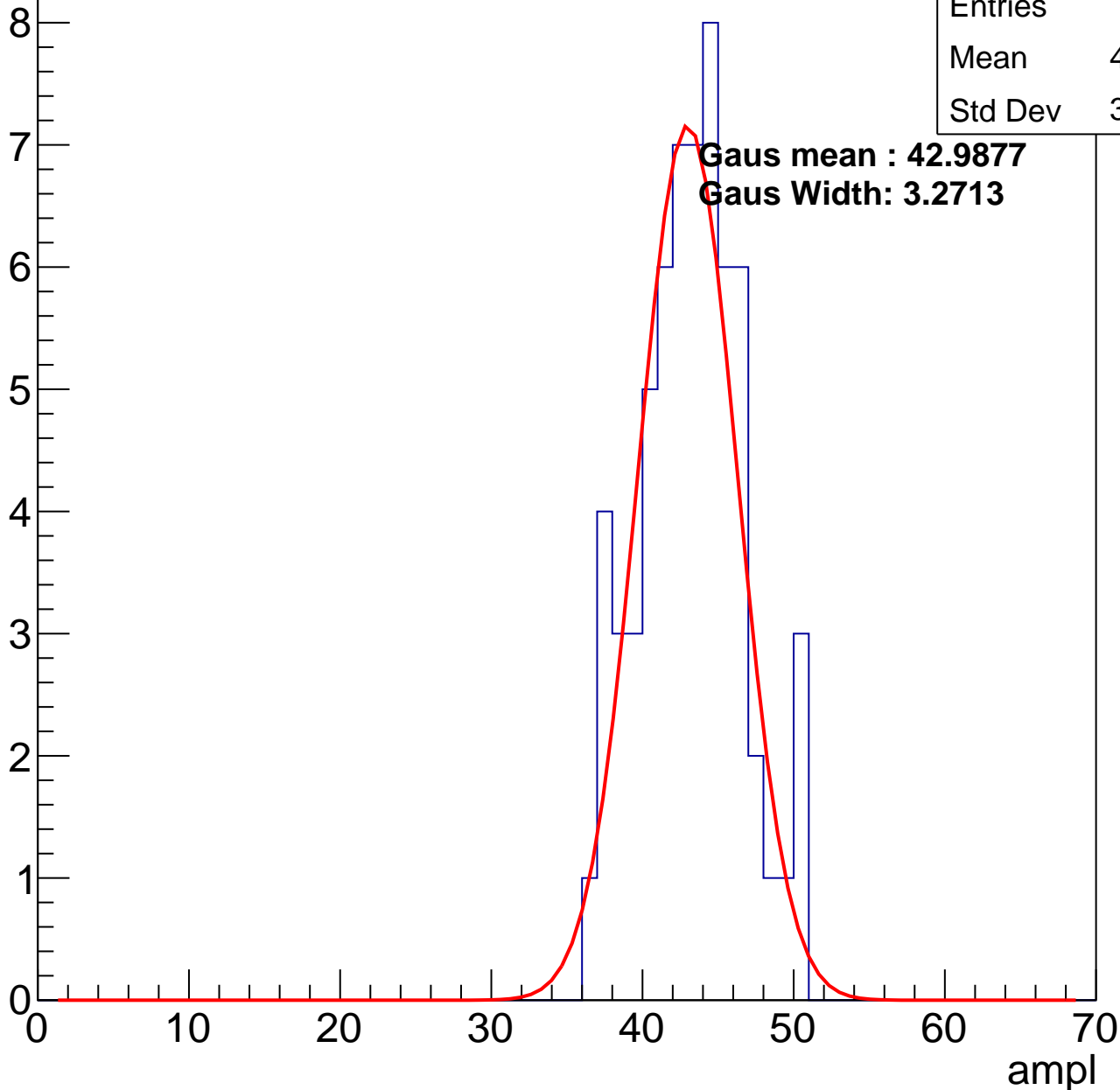
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	42.78
Std Dev	3.369

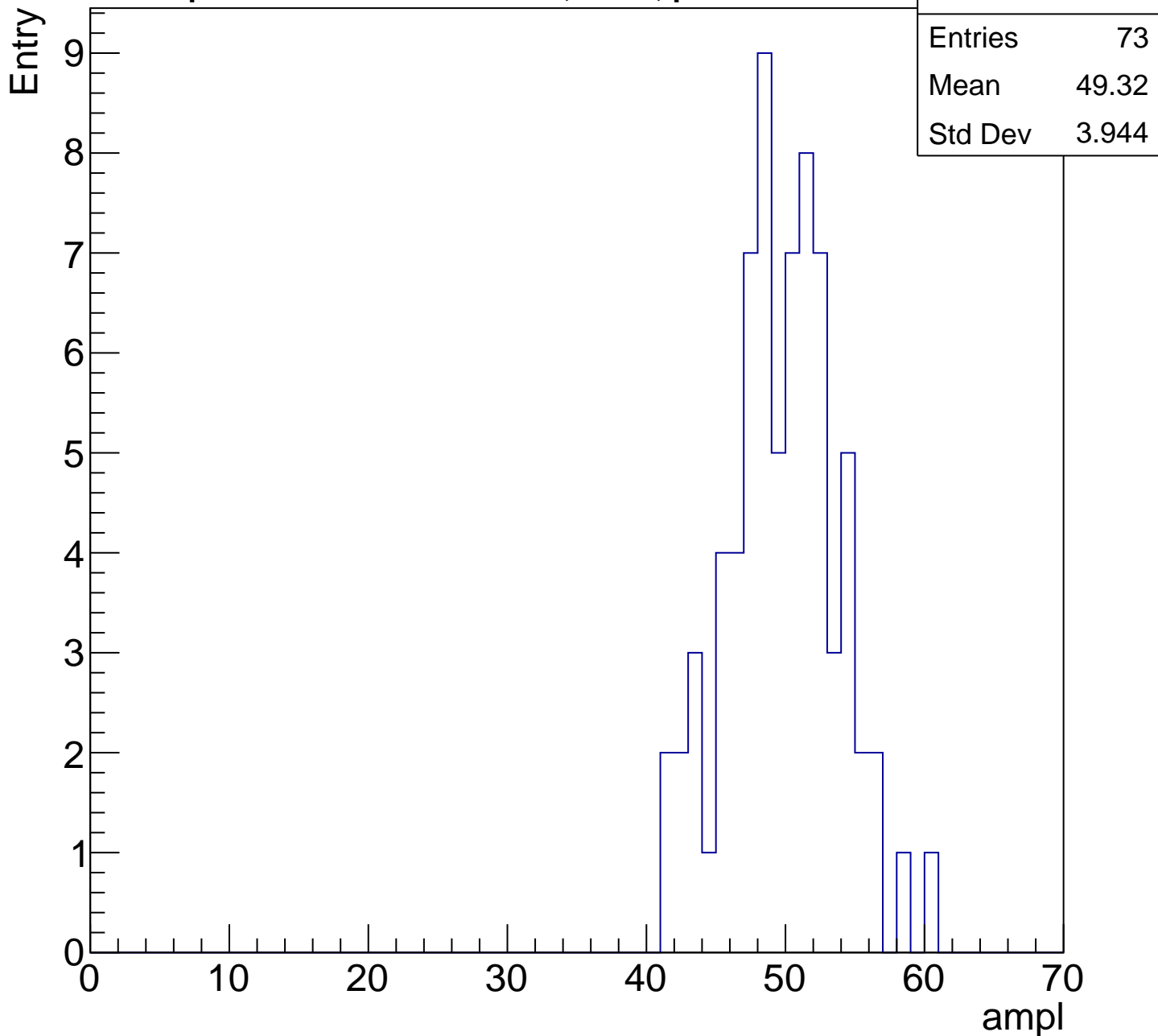
**Gaus mean : 42.9877**

**Gaus Width: 3.2713**



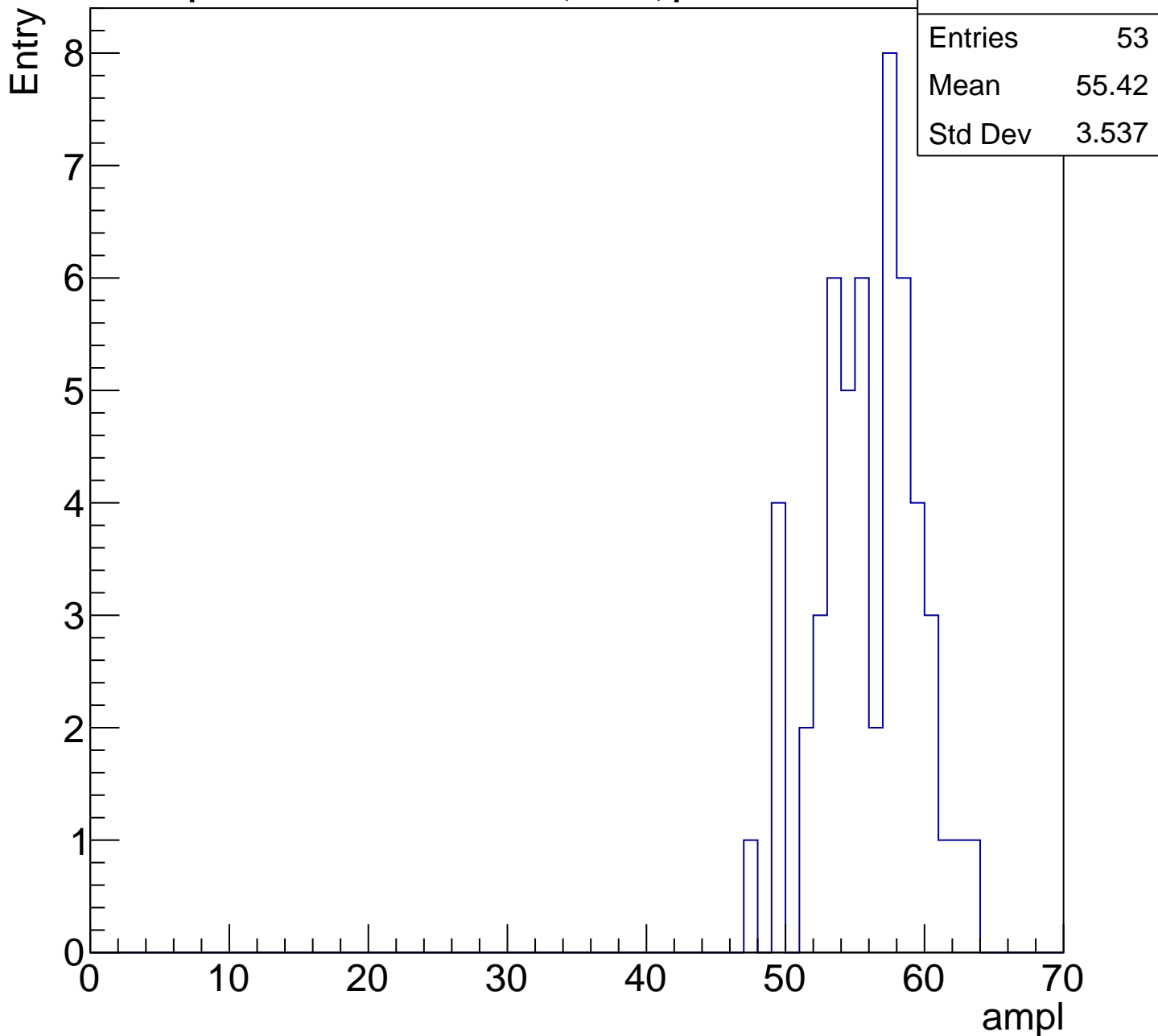
# B1L103S, U9-ch42, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U9-ch42, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

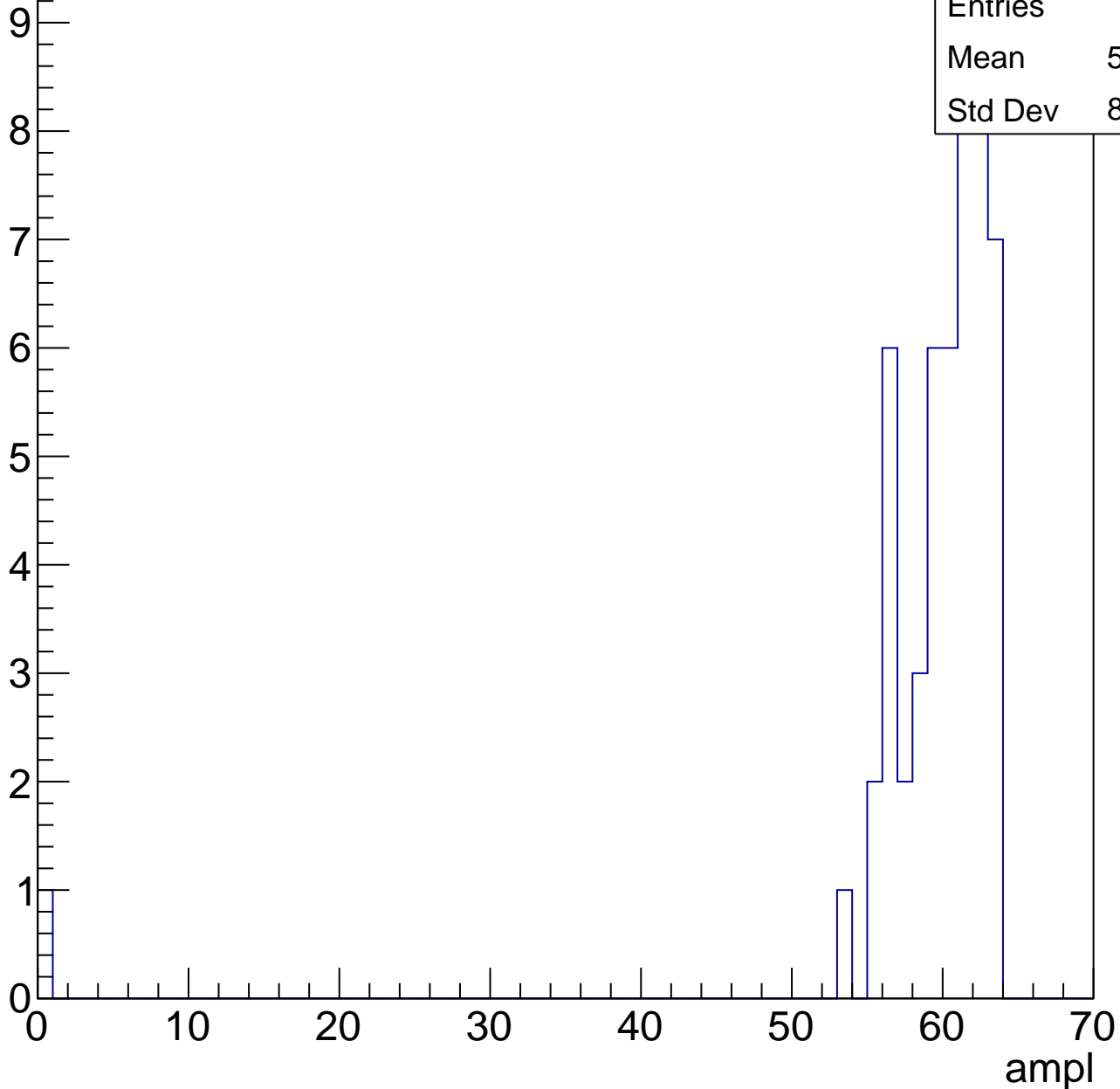


# B1L103S, U9-ch42, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	51
Mean	58.59
Std Dev	8.673



# B1L103S, U9-ch42, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U9-ch42, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	2
Mean	11
Std Dev	11

# B1L103S, U9-ch43, adc0

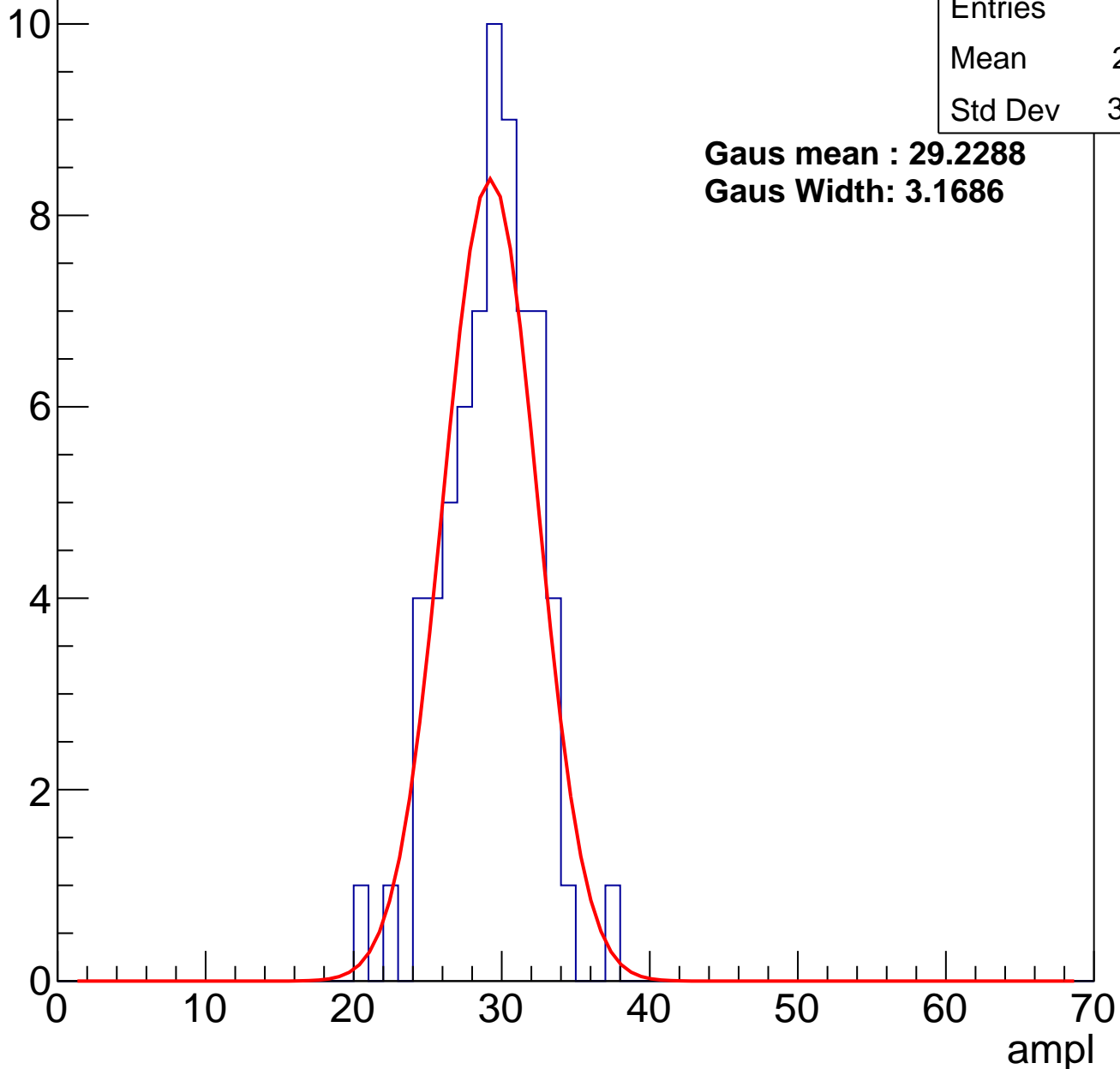
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	67
Mean	28.81
Std Dev	3.043

**Gaus mean : 29.2288**

**Gaus Width: 3.1686**

Entry



# B1L103S, U9-ch43, adc1

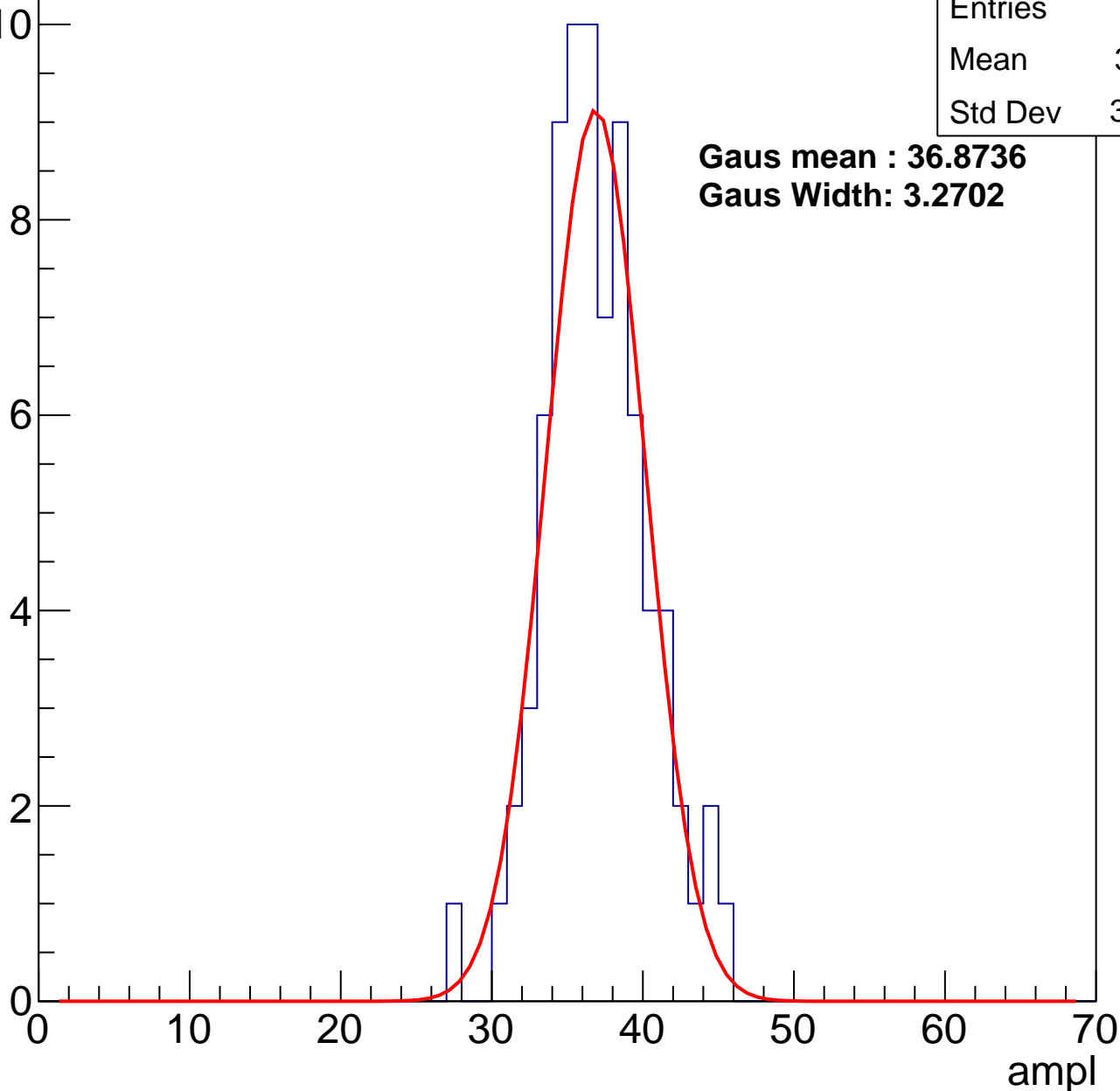
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	78
Mean	36.51
Std Dev	3.369

**Gaus mean : 36.8736**

**Gaus Width: 3.2702**



# B1L103S, U9-ch43, adc2

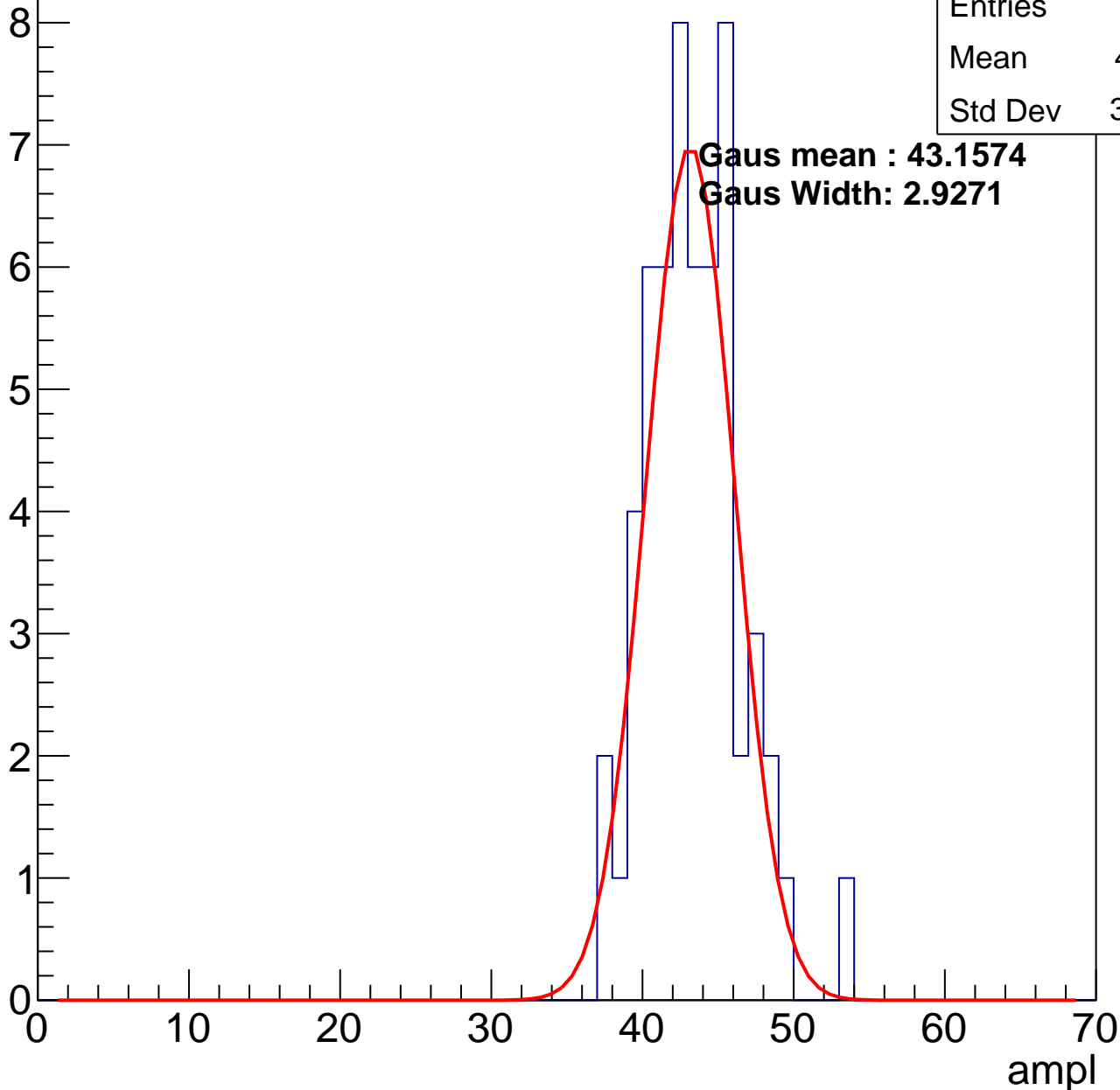
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	56
Mean	42.91
Std Dev	3.095

**Gaus mean : 43.1574**

**Gaus Width: 2.9271**



# B1L103S, U9-ch43, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

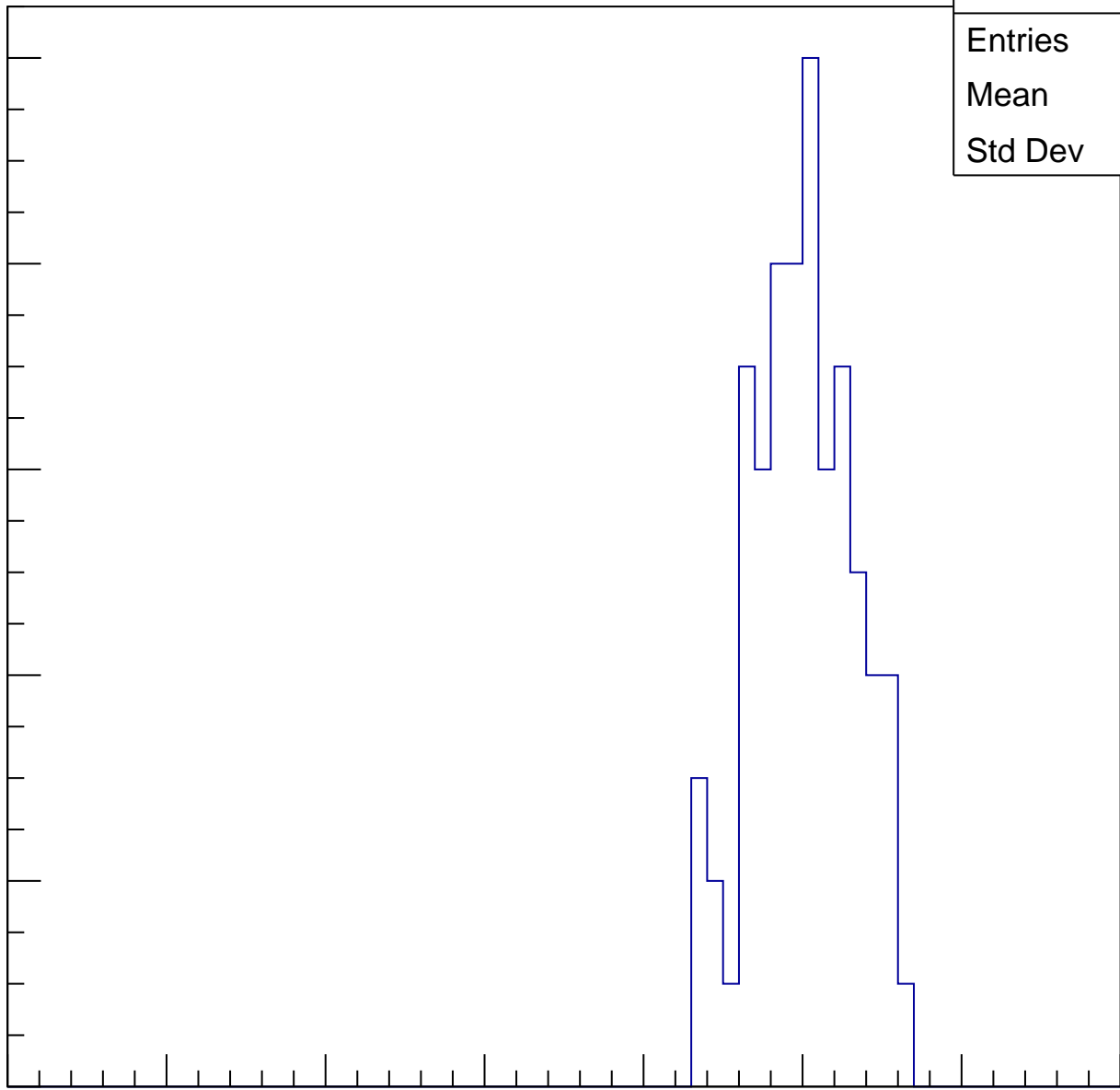
Entries	72
Mean	49.57
Std Dev	3.153

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

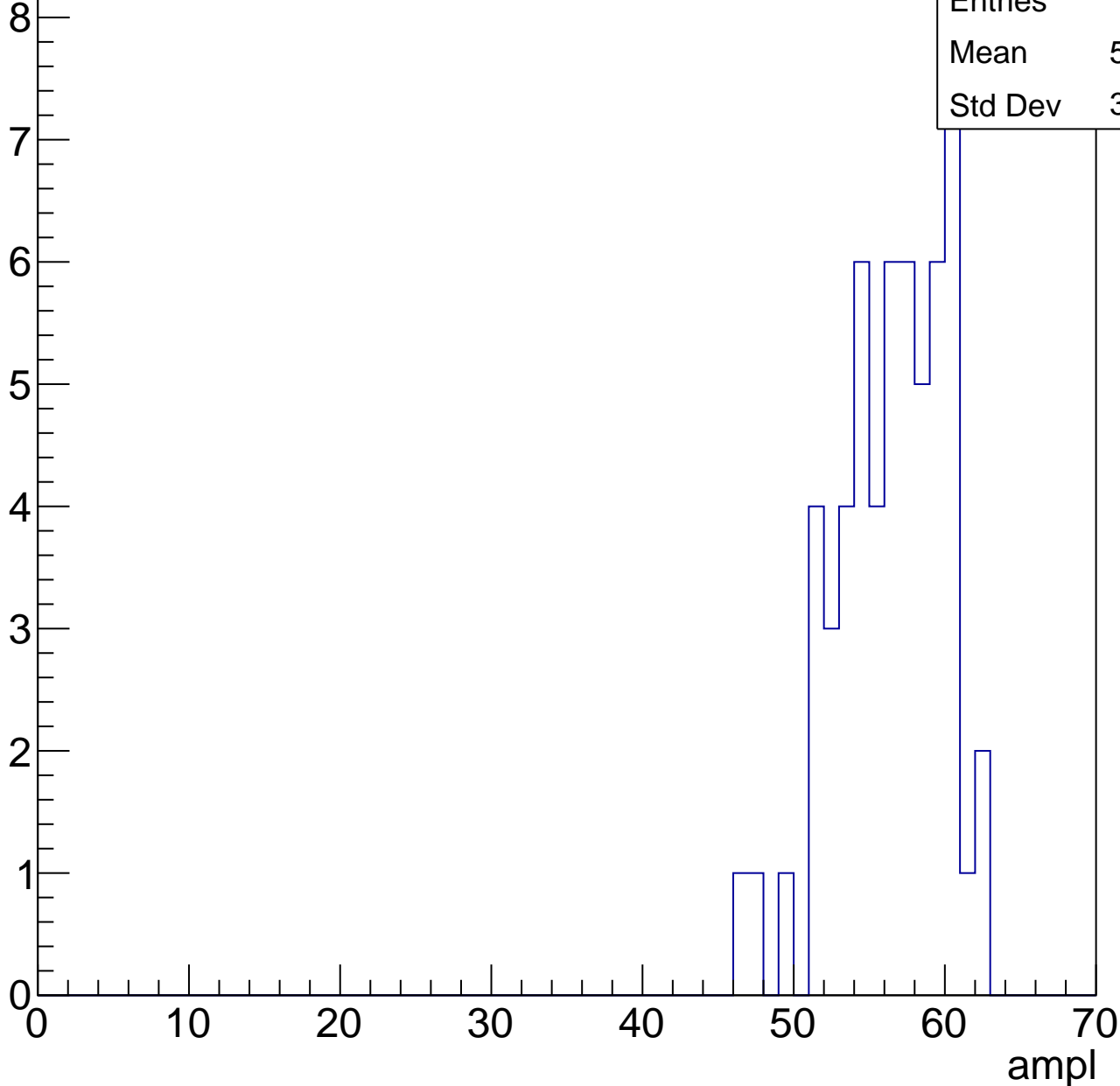


# B1L103S, U9-ch43, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	58
Mean	55.95
Std Dev	3.588

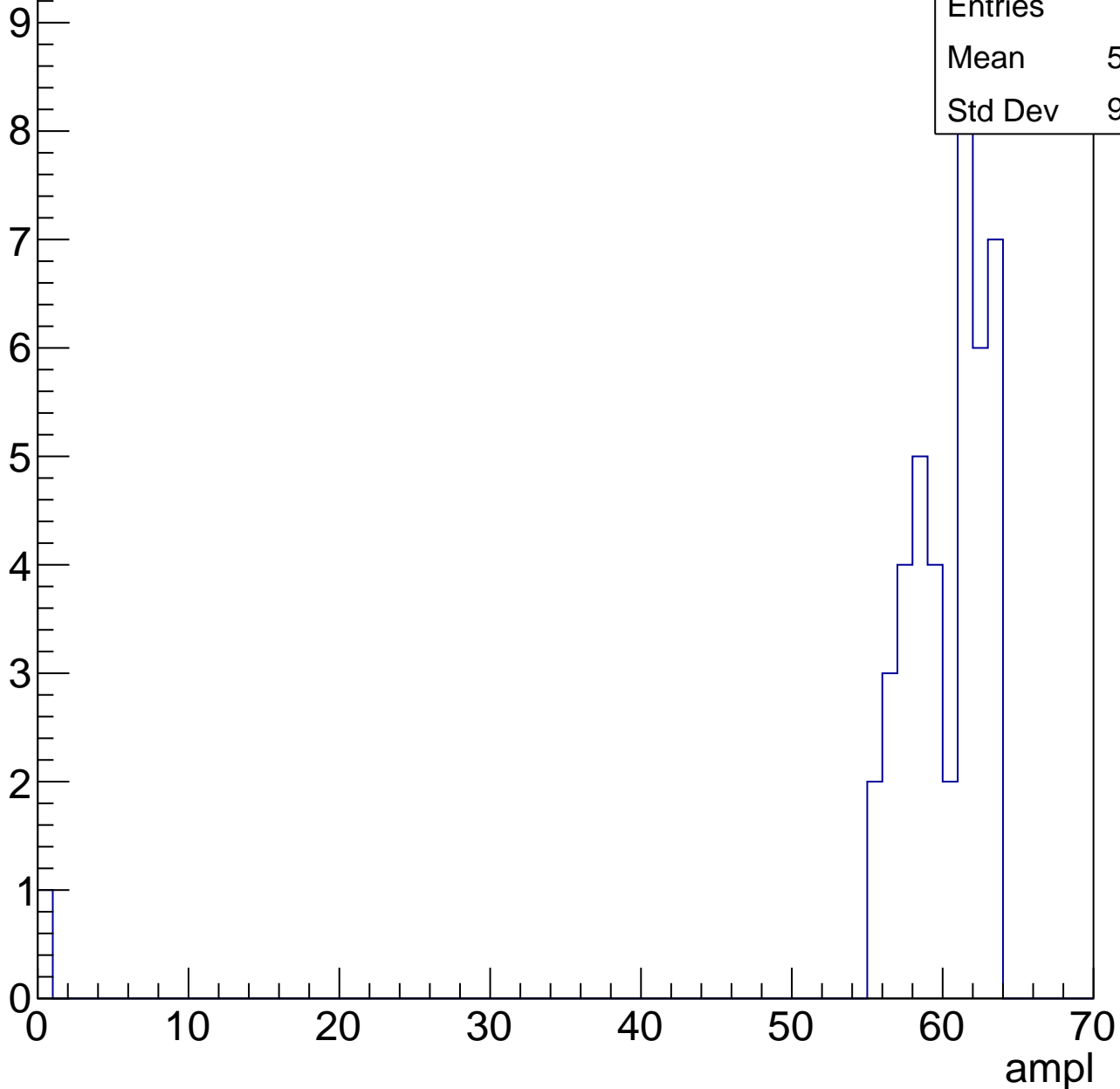


# B1L103S, U9-ch43, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	43
Mean	58.47
Std Dev	9.342



# B1L103S, U9-ch43, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U9-ch43, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

1  
0.8  
0.6  
0.4  
0.2  
0

Entries	1
Mean	18
Std Dev	0

ampl

# B1L103S, U9-ch44, adc0

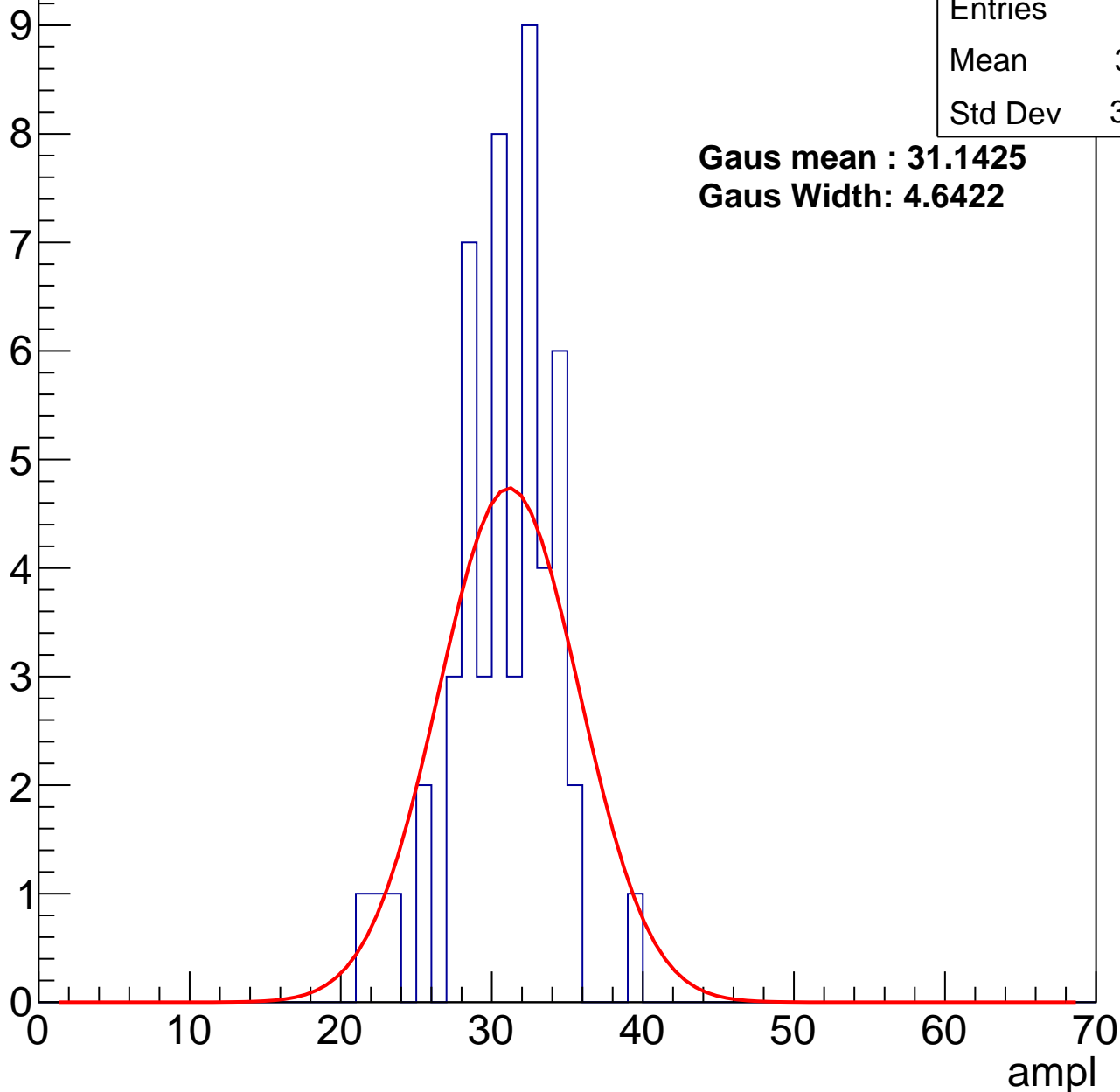
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	51
Mean	30.31
Std Dev	3.427

**Gaus mean : 31.1425**

**Gaus Width: 4.6422**



# B1L103S, U9-ch44, adc1

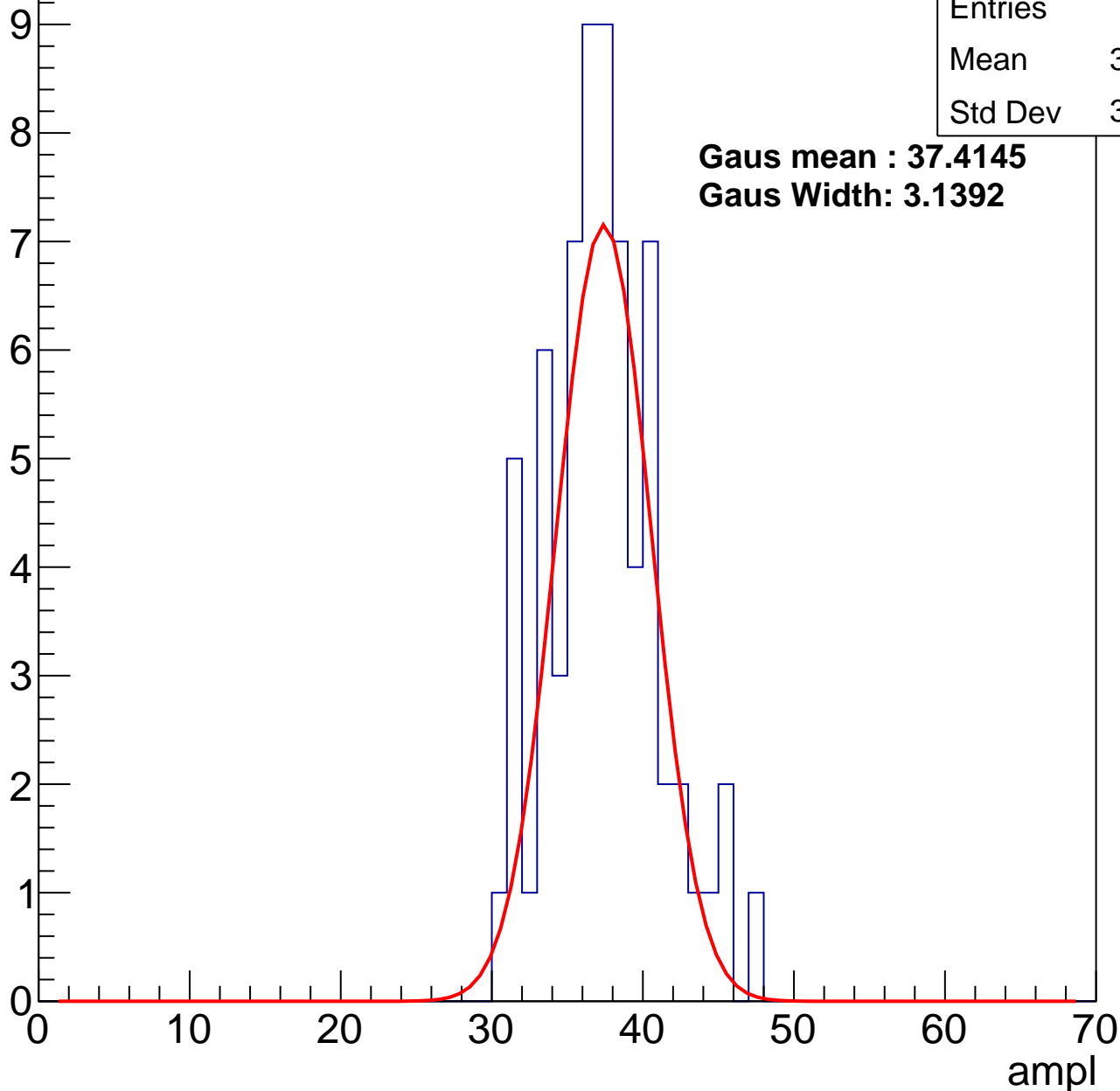
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	68
Mean	36.93
Std Dev	3.627

**Gaus mean : 37.4145**

**Gaus Width: 3.1392**



# B1L103S, U9-ch44, adc2

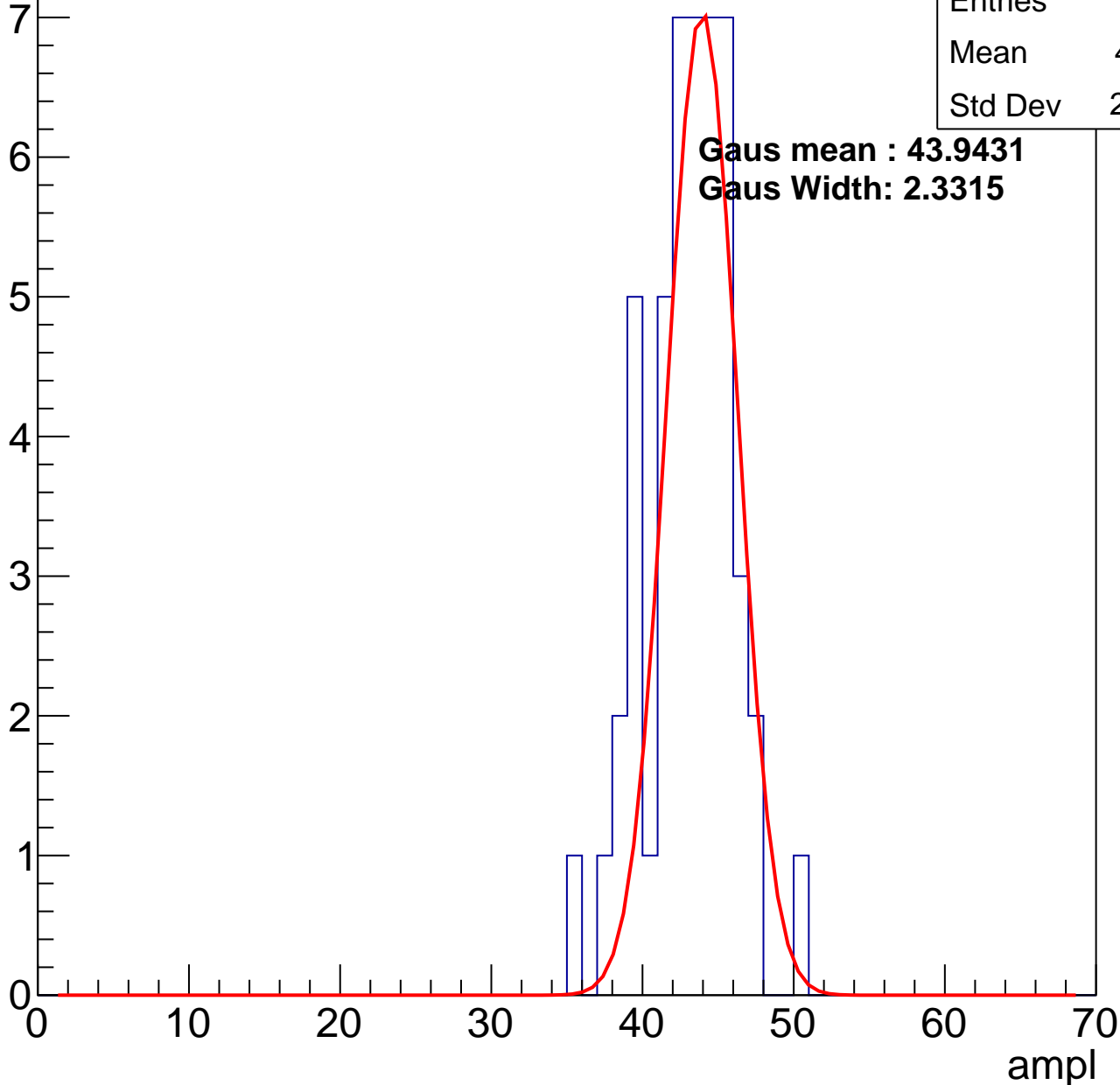
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	49
Mean	42.61
Std Dev	2.863

**Gaus mean : 43.9431**

**Gaus Width: 2.3315**

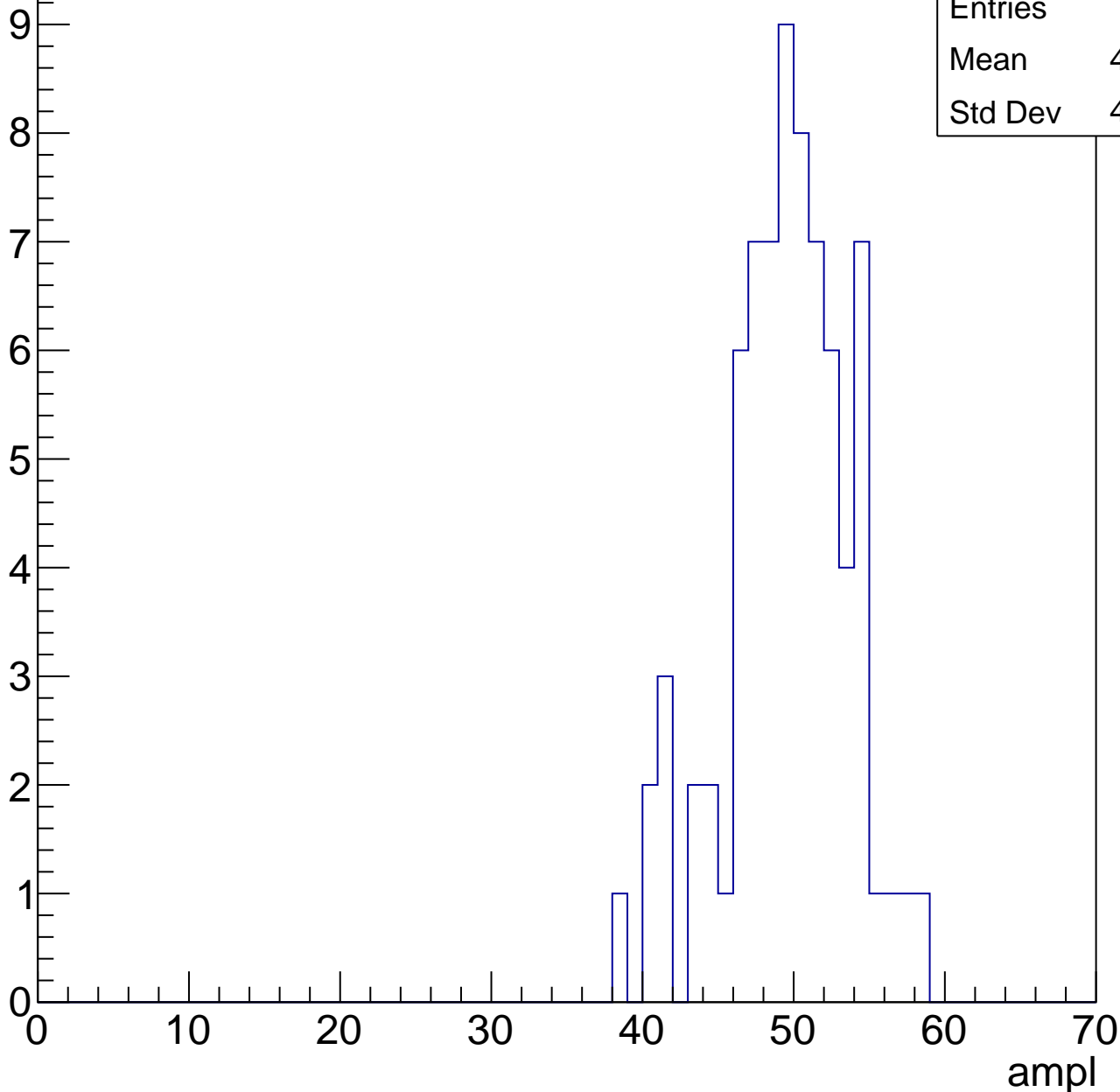


# B1L103S, U9-ch44, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

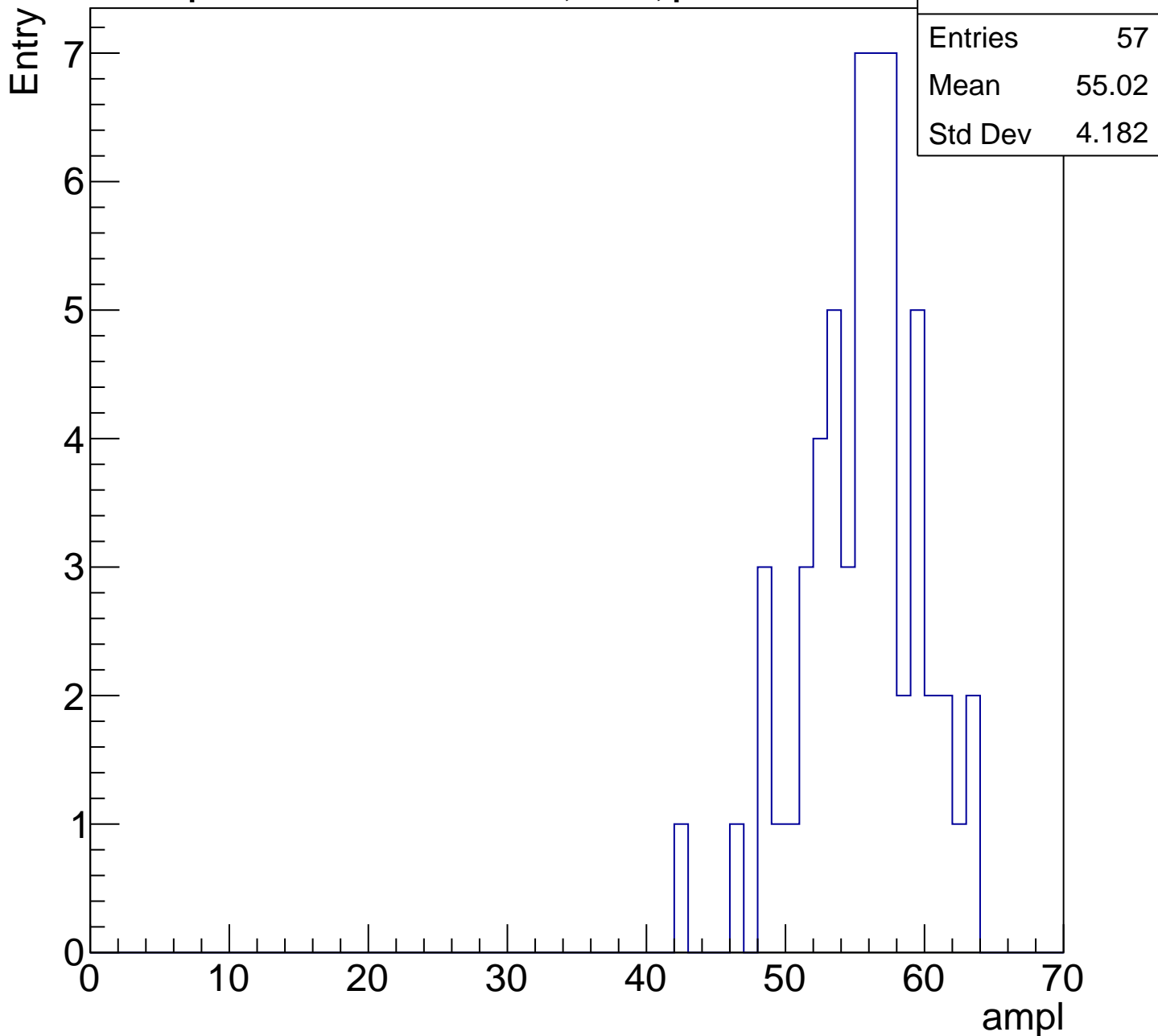
Entry

Entries	76
Mean	49.04
Std Dev	4.073



# B1L103S, U9-ch44, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

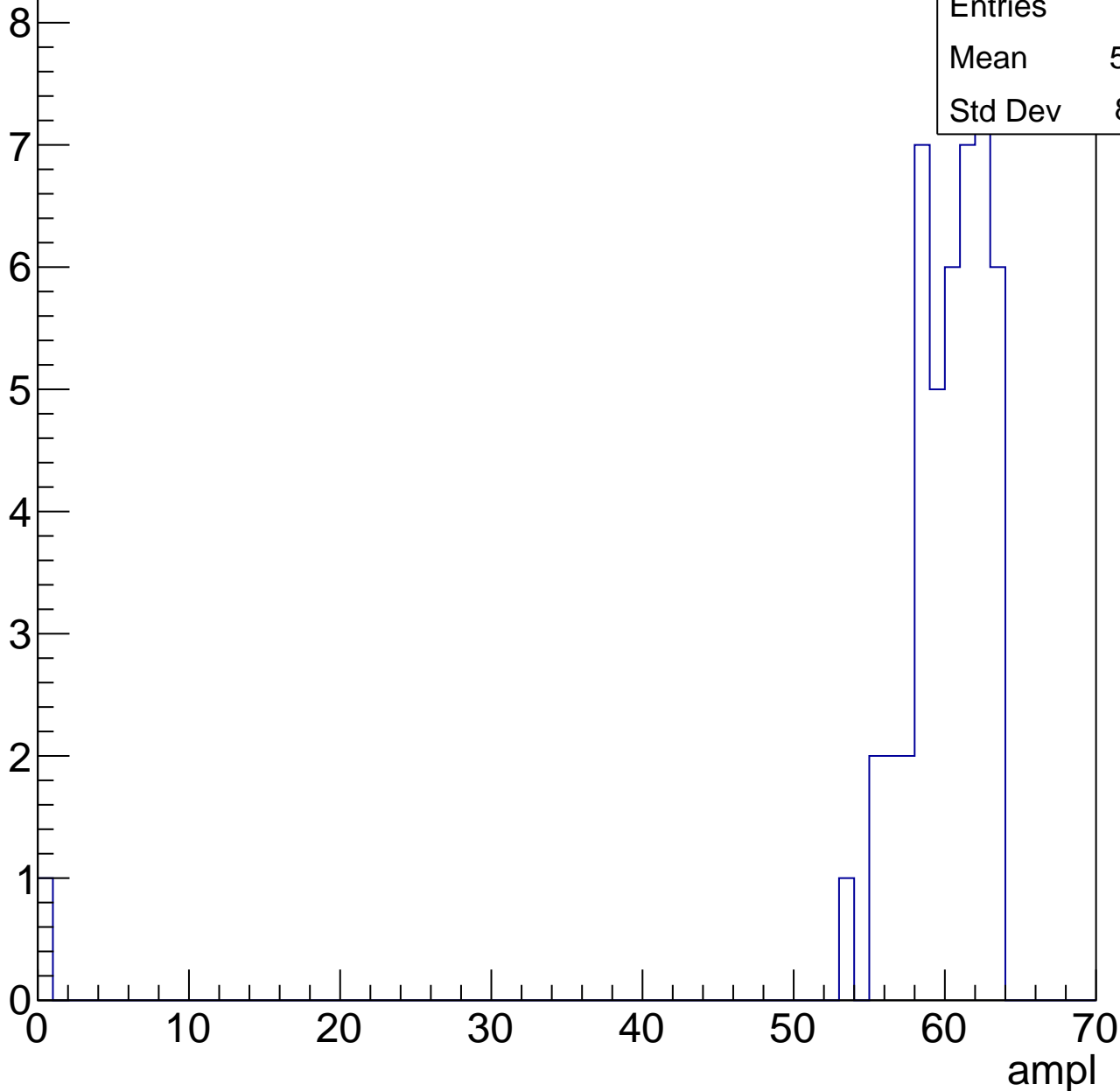


# B1L103S, U9-ch44, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	47
Mean	58.53
Std Dev	8.961



# B1L103S, U9-ch44, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	6
Mean	61.5
Std Dev	1.258

ampl



# B1L103S, U9-ch44, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L103S, U9-ch45, adc0

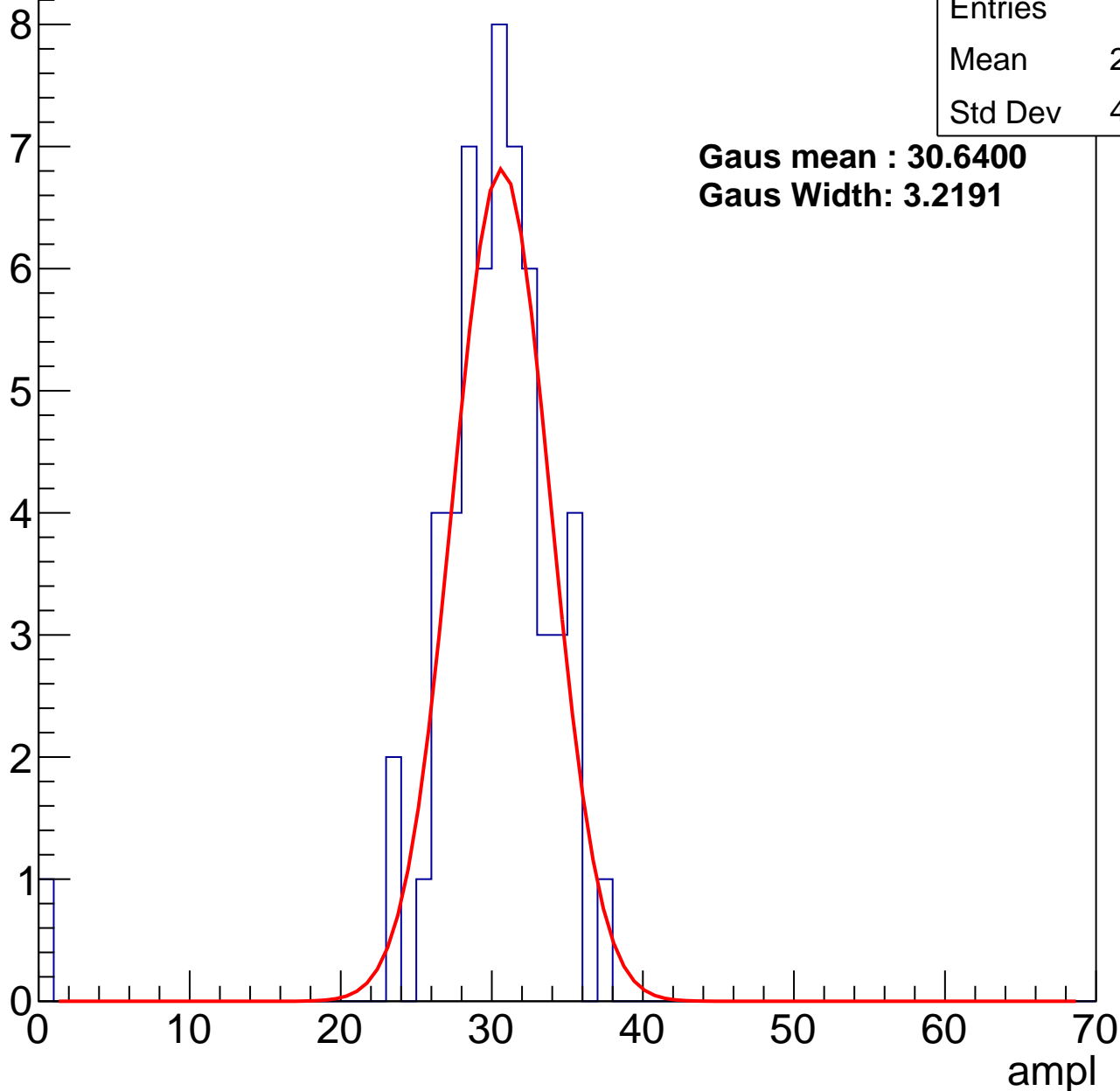
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	57
Mean	29.47
Std Dev	4.949

**Gaus mean : 30.6400**

**Gaus Width: 3.2191**



# B1L103S, U9-ch45, adc1

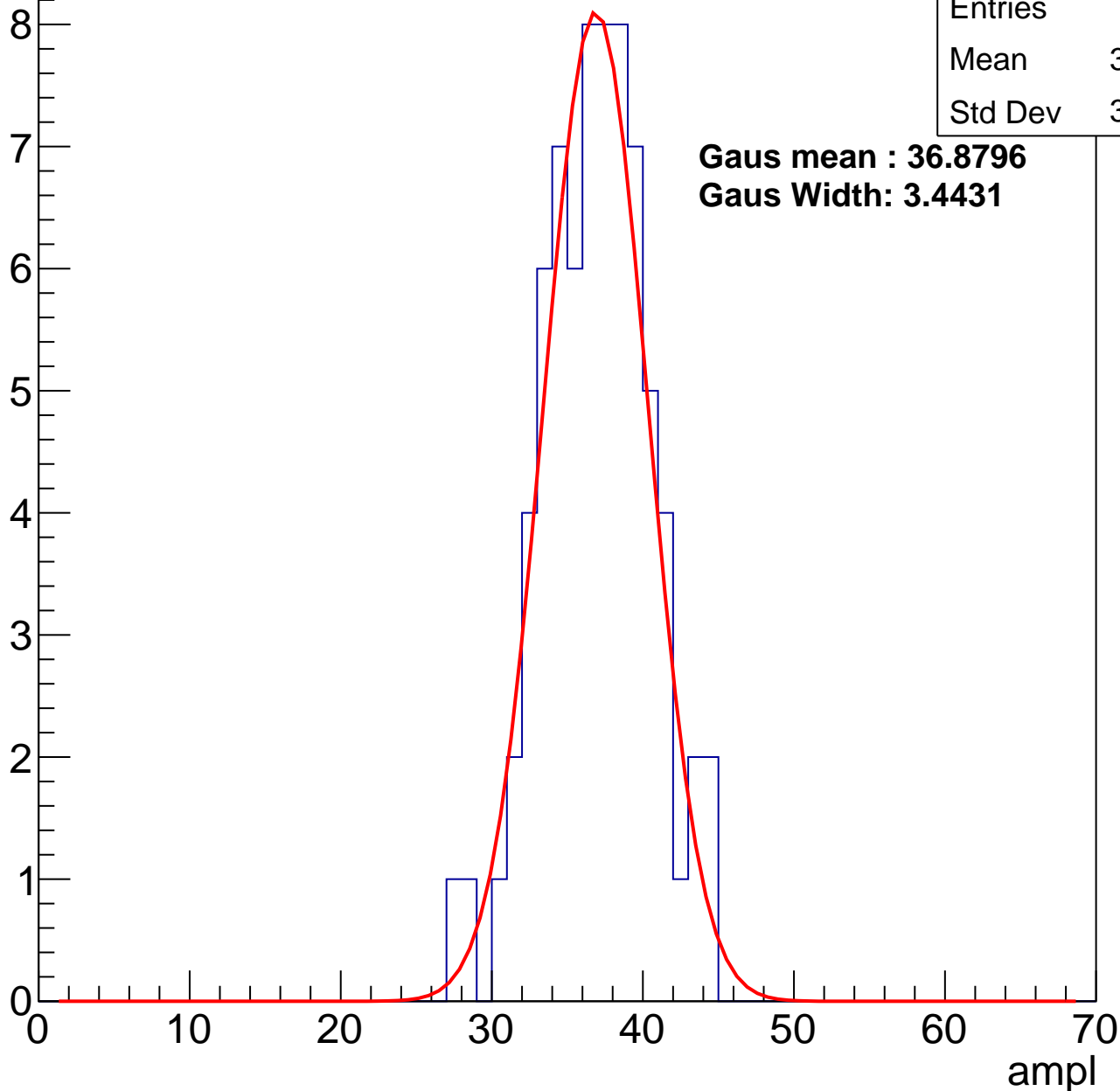
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	73
Mean	36.47
Std Dev	3.535

**Gaus mean : 36.8796**

**Gaus Width: 3.4431**



# B1L103S, U9-ch45, adc2

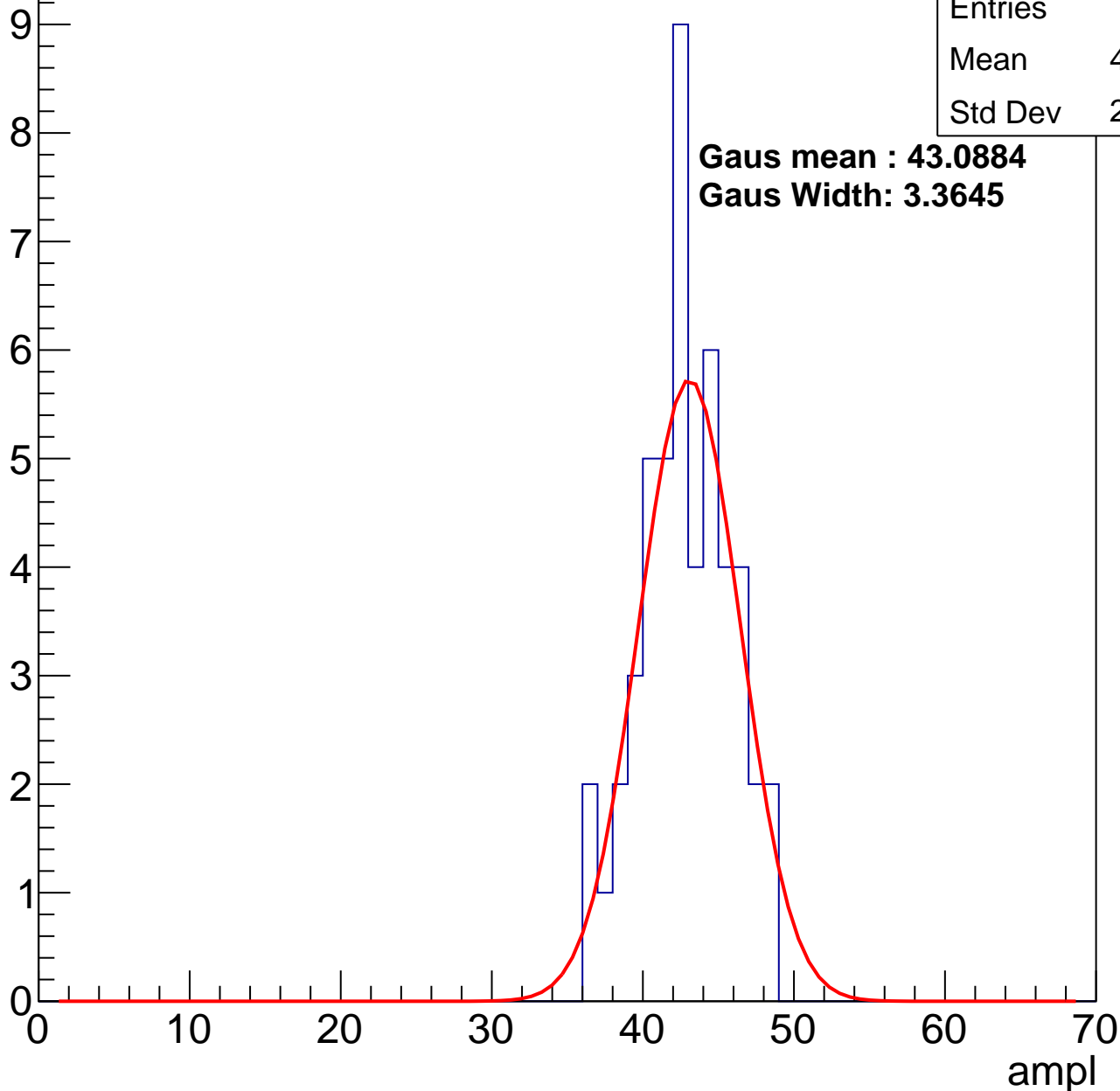
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	49
Mean	42.35
Std Dev	2.945

**Gaus mean : 43.0884**

**Gaus Width: 3.3645**



# B1L103S, U9-ch45, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

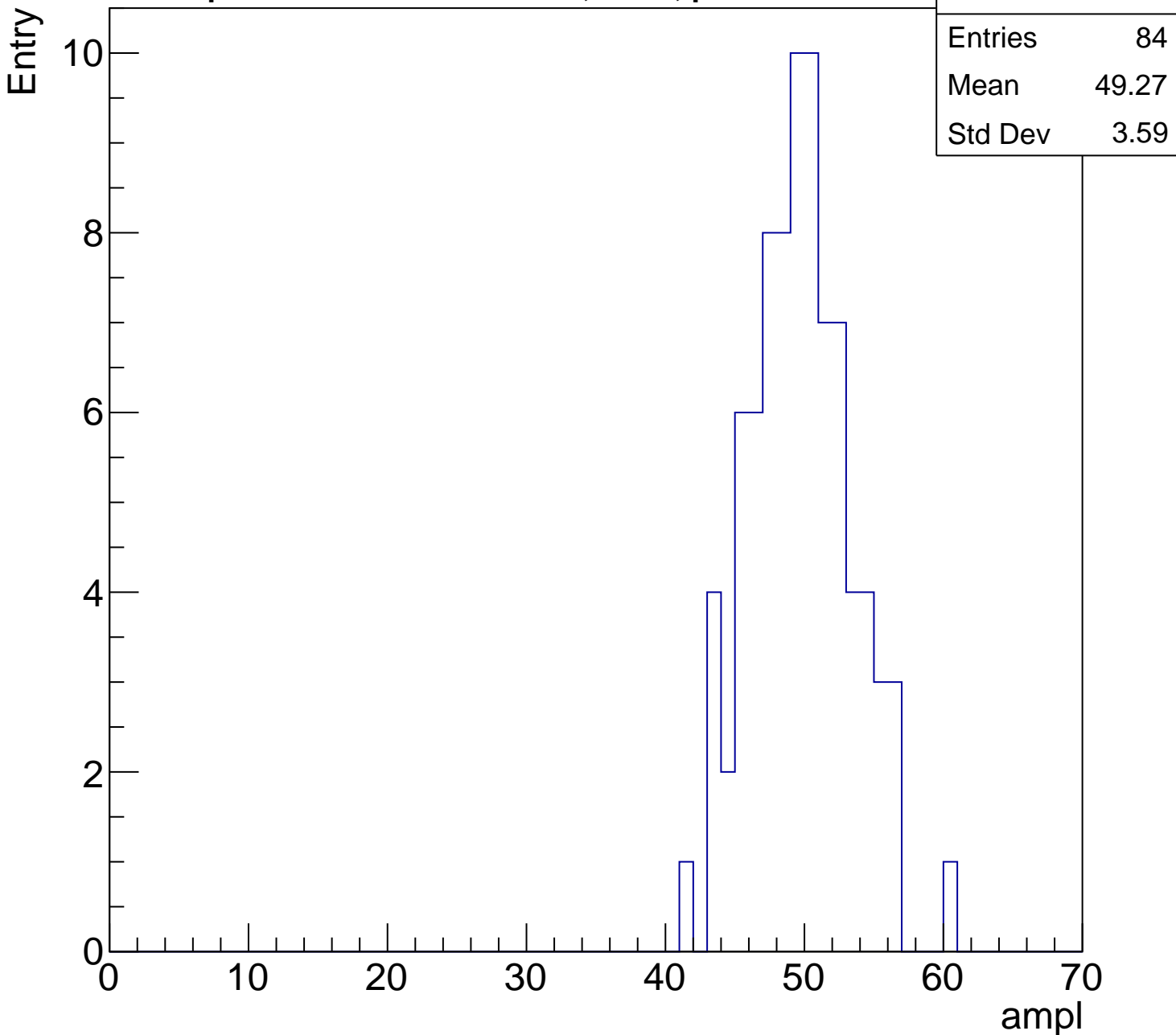
Entries	84
Mean	49.27
Std Dev	3.59

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

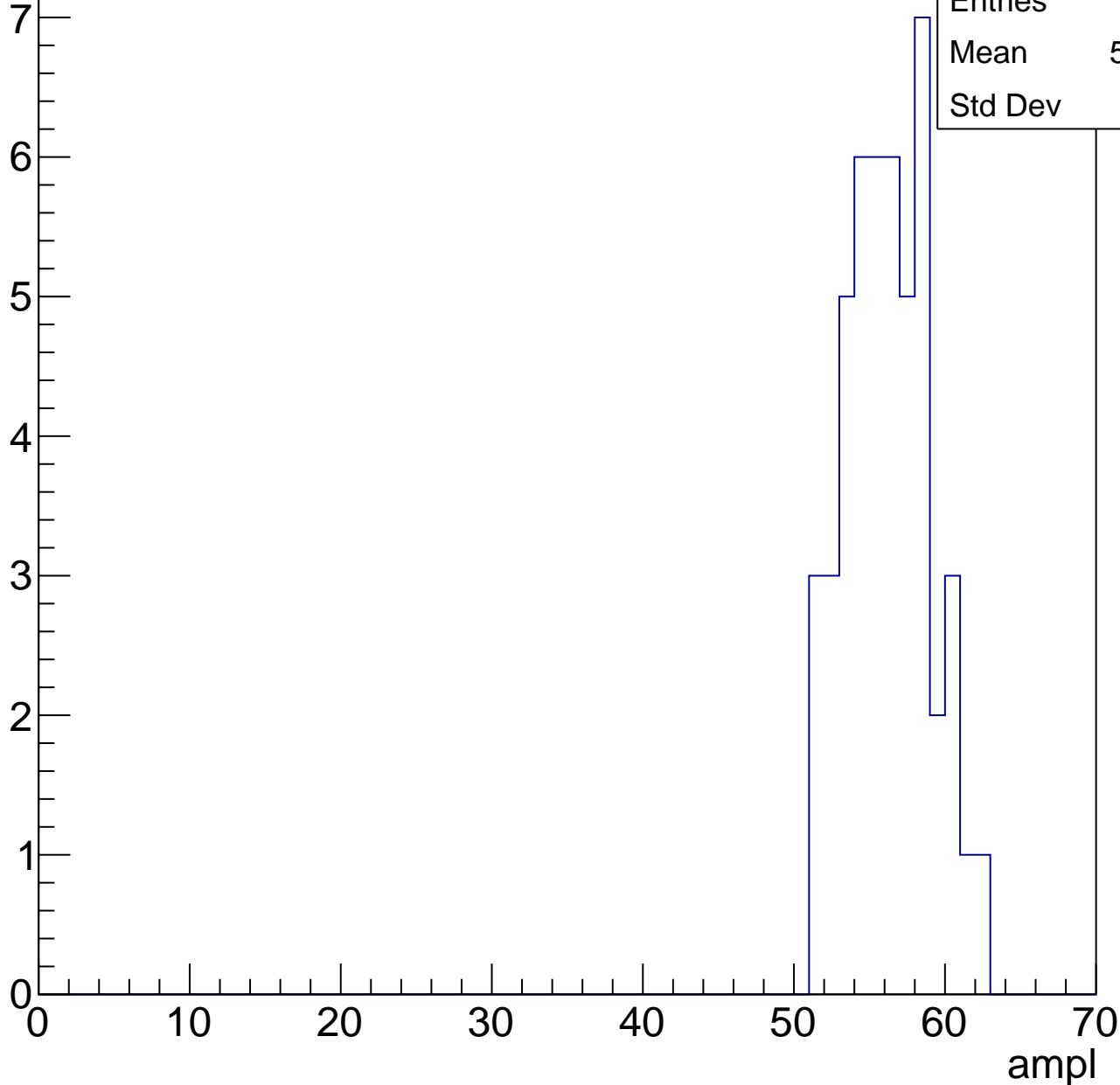
ampl



# B1L103S, U9-ch45, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U9-ch45, adc5

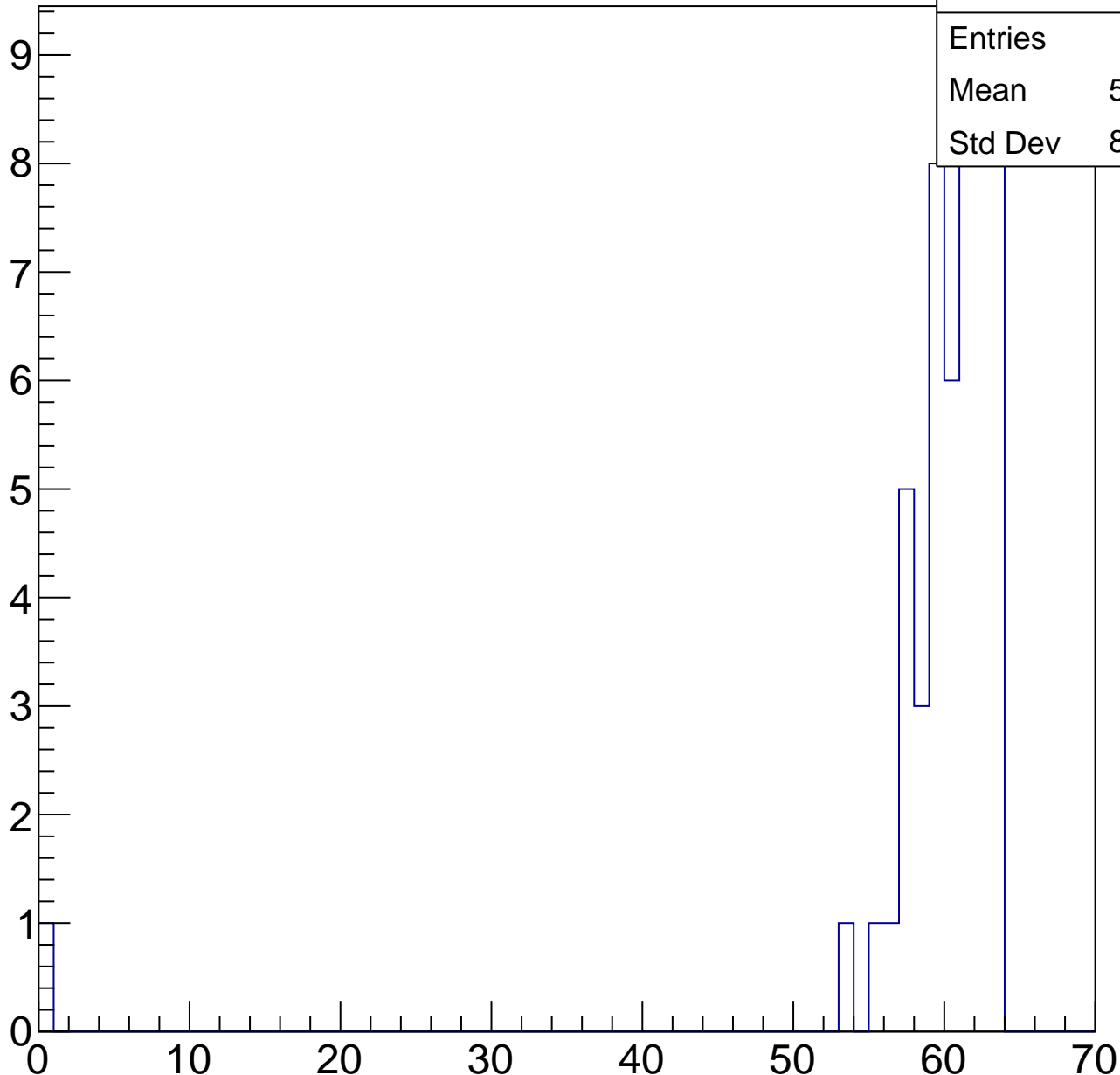
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	53
Mean	59.04
Std Dev	8.503

ampl



# B1L103S, U9-ch45, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U9-ch45, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L103S, U9-ch46, adc0

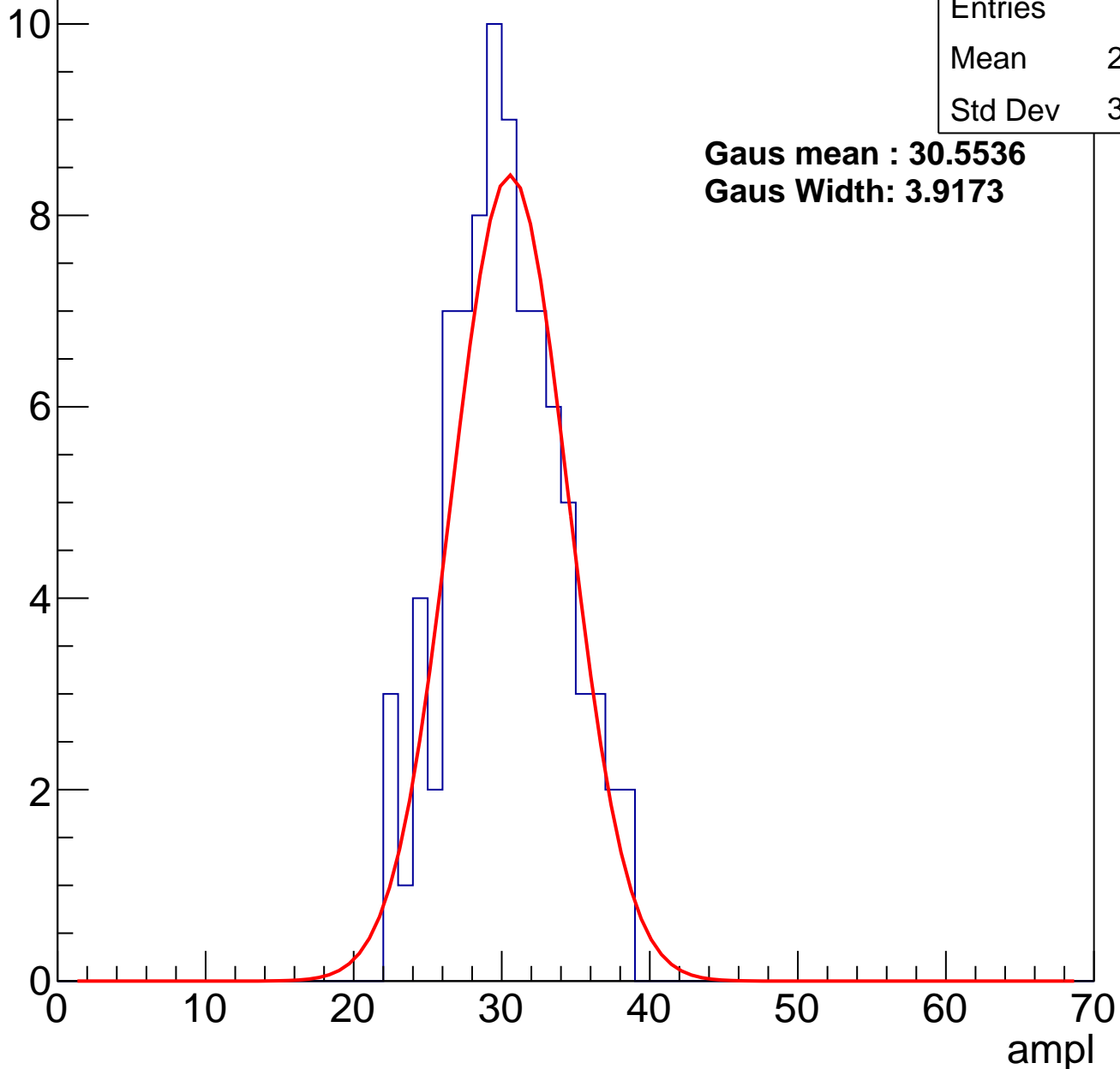
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	86
Mean	29.79
Std Dev	3.776

**Gaus mean : 30.5536**

**Gaus Width: 3.9173**

Entry



# B1L103S, U9-ch46, adc1

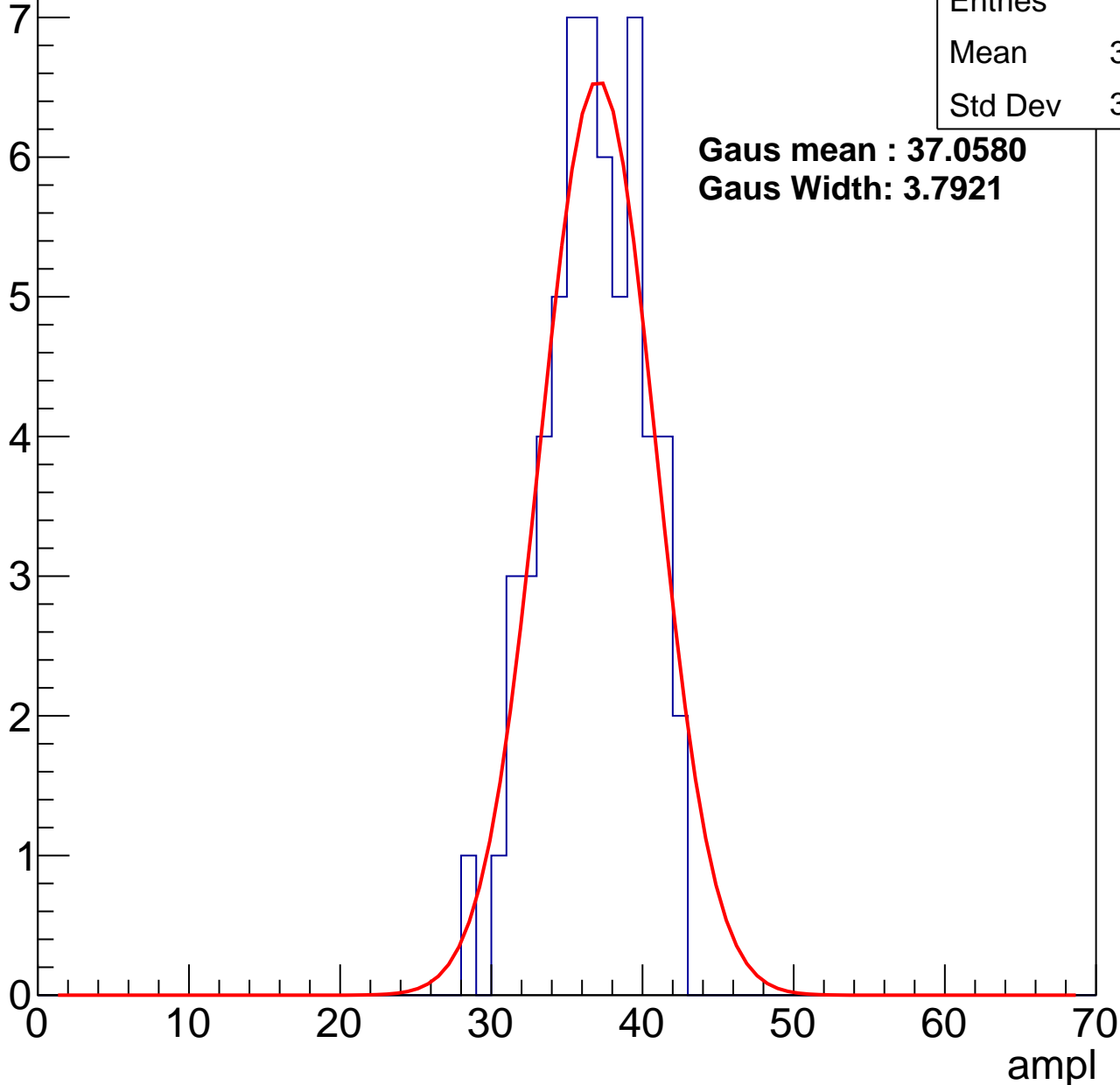
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	59
Mean	36.25
Std Dev	3.208

**Gaus mean : 37.0580**

**Gaus Width: 3.7921**



# B1L103S, U9-ch46, adc2

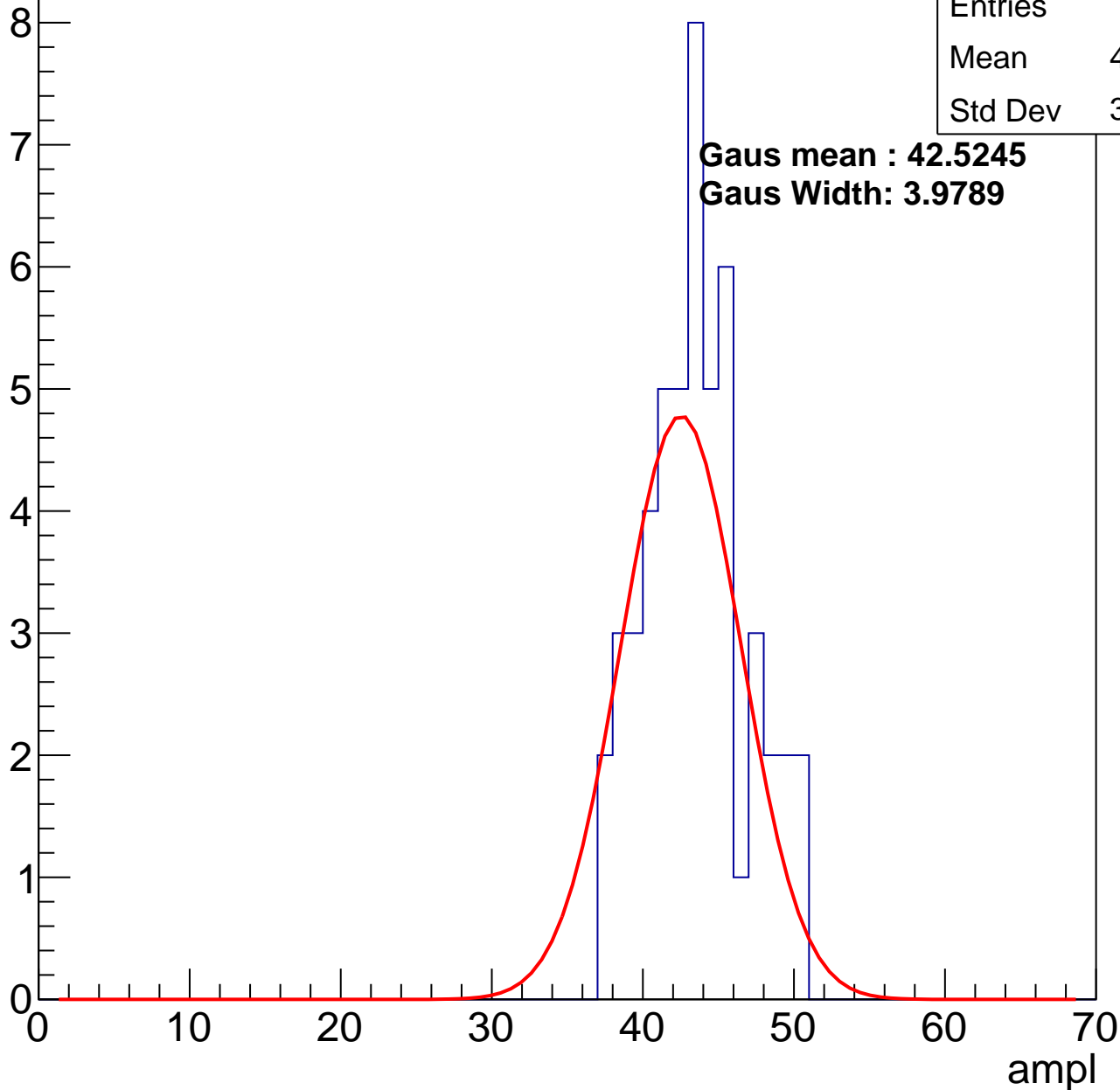
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	51
Mean	43.04
Std Dev	3.319

**Gaus mean : 42.5245**

**Gaus Width: 3.9789**

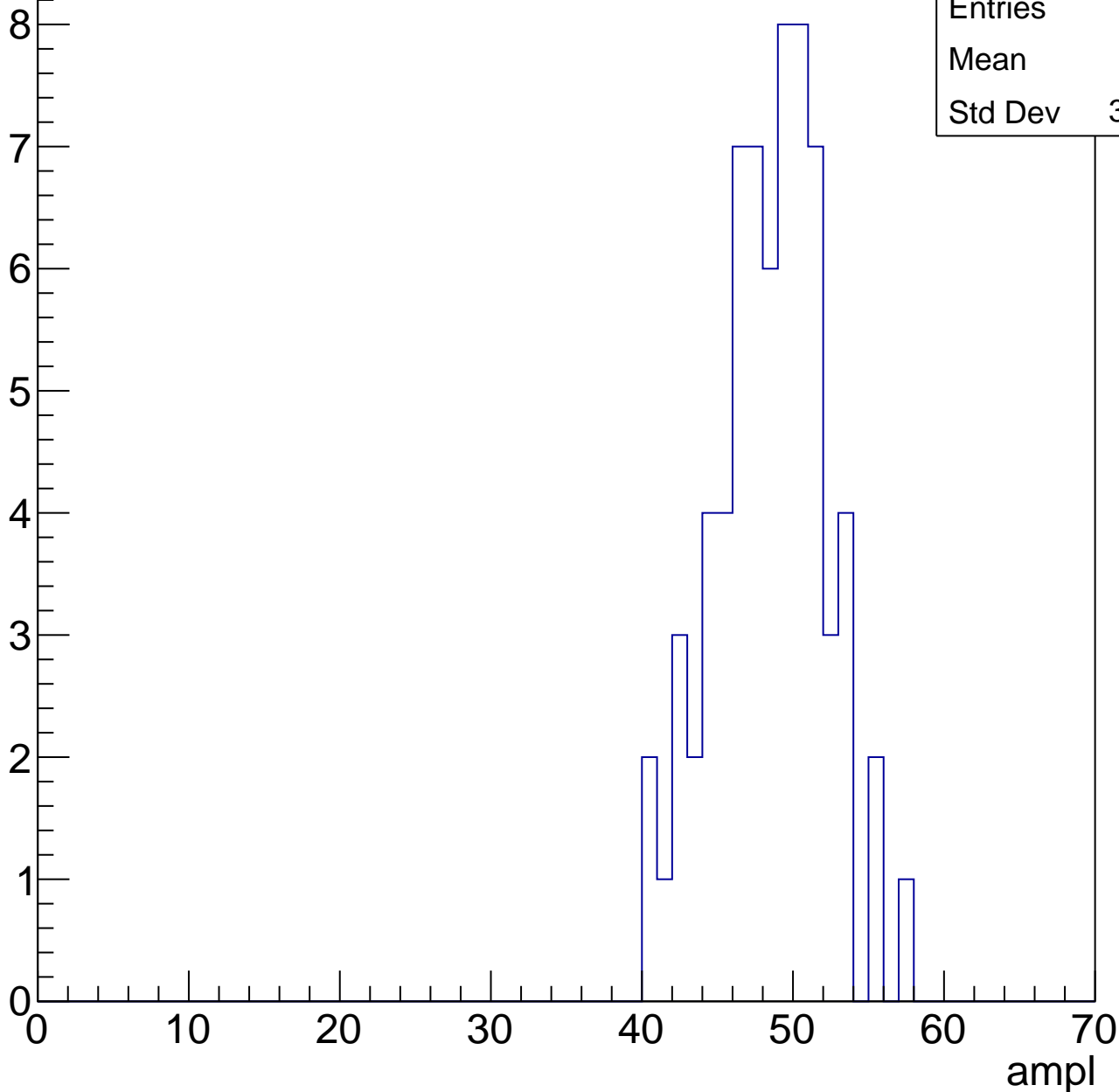


# B1L103S, U9-ch46, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	69
Mean	48
Std Dev	3.612

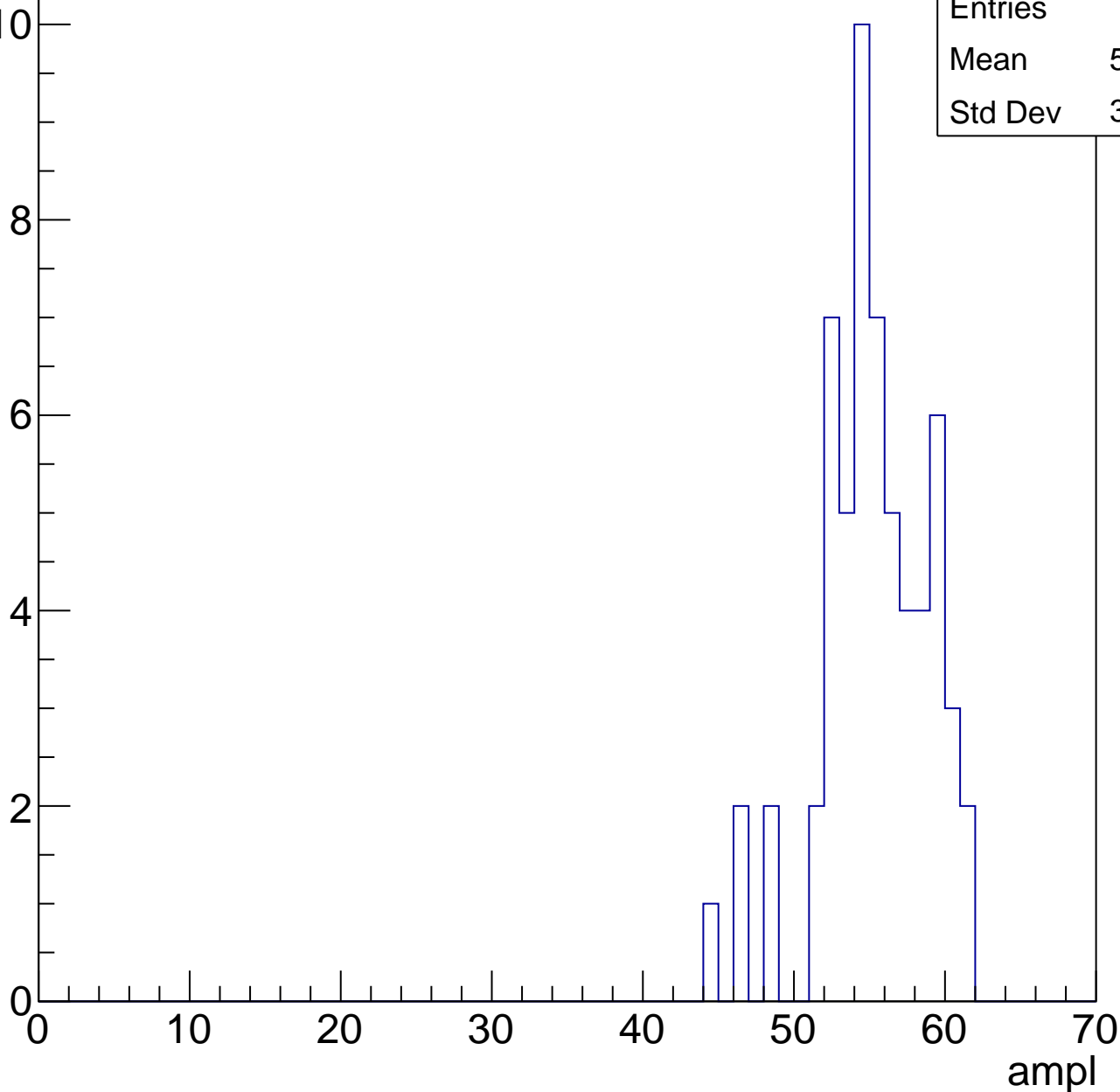


# B1L103S, U9-ch46, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	60
Mean	54.73
Std Dev	3.655

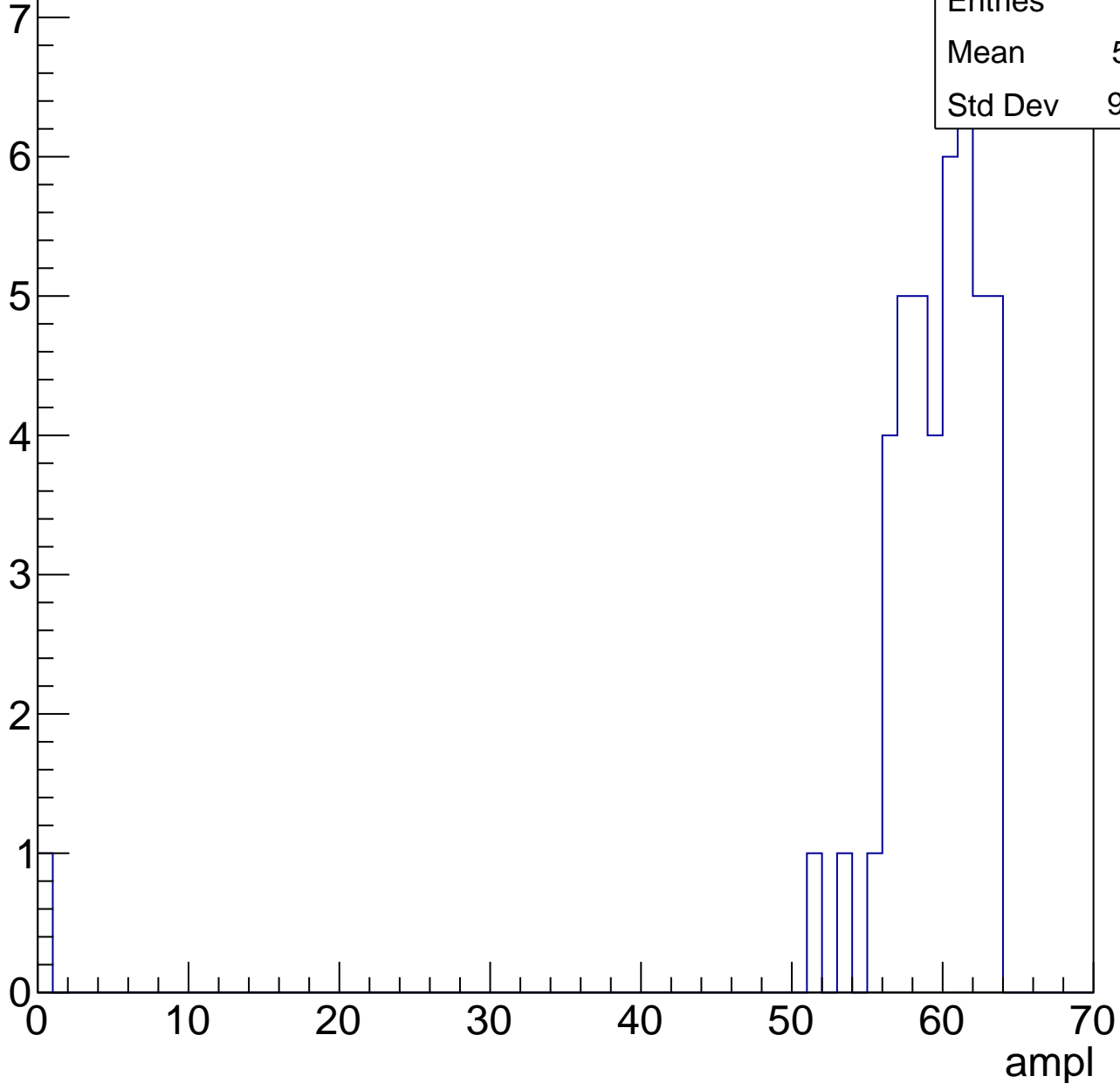


# B1L103S, U9-ch46, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	45
Mean	57.91
Std Dev	9.145

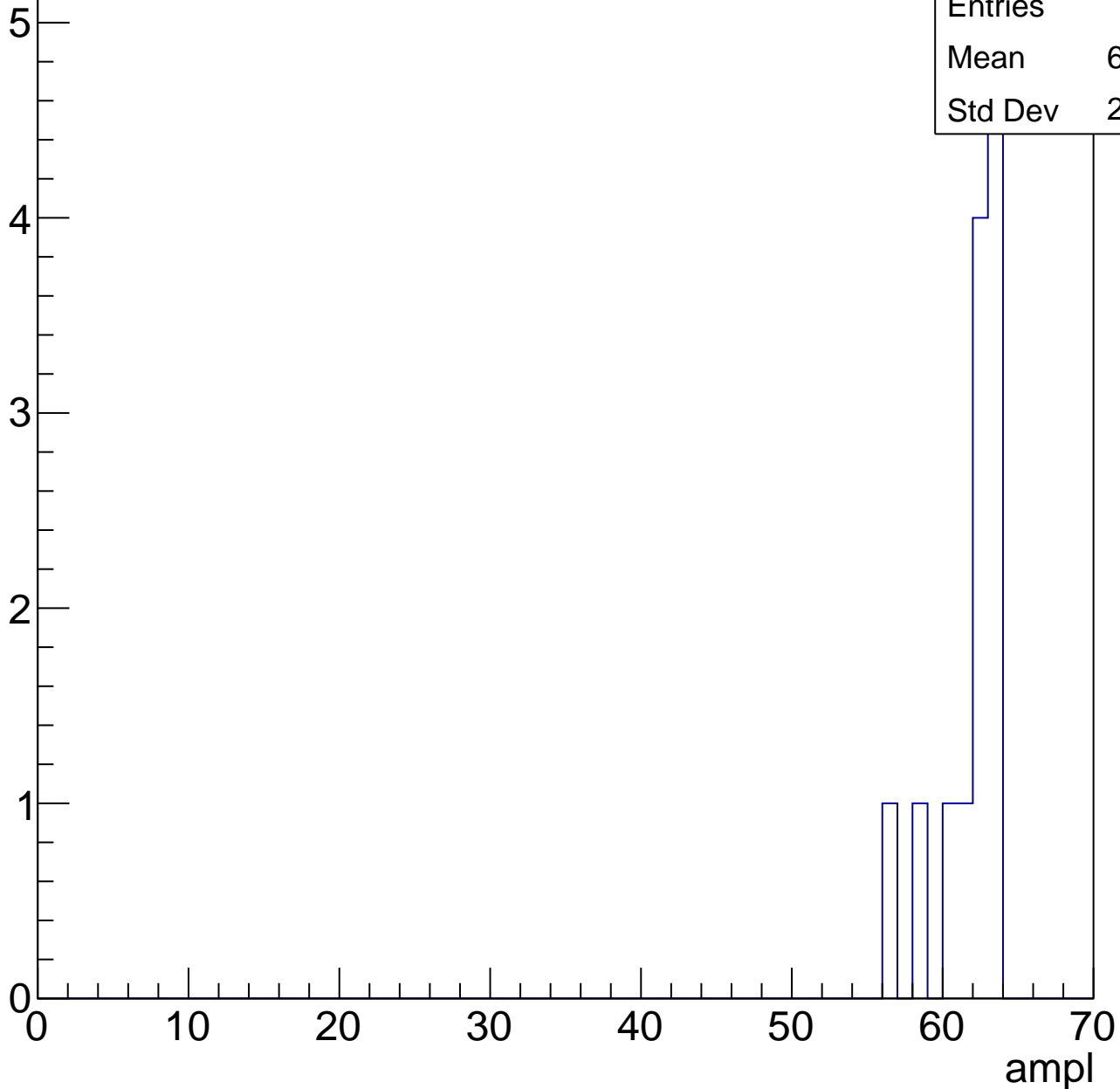


# B1L103S, U9-ch46, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	13
Mean	61.38
Std Dev	2.095

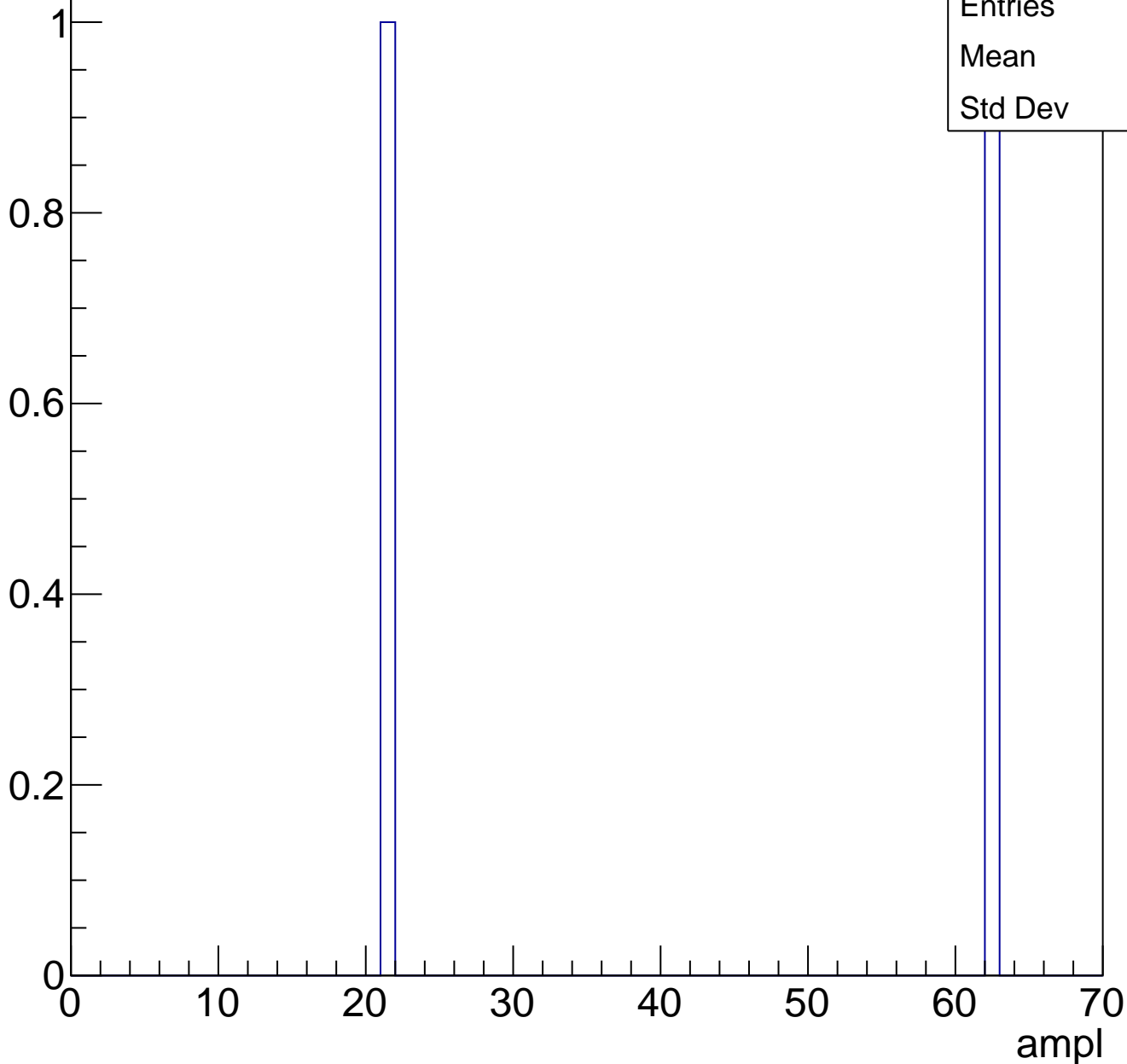




# B1L103S, U9-ch46, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U9-ch47, adc0

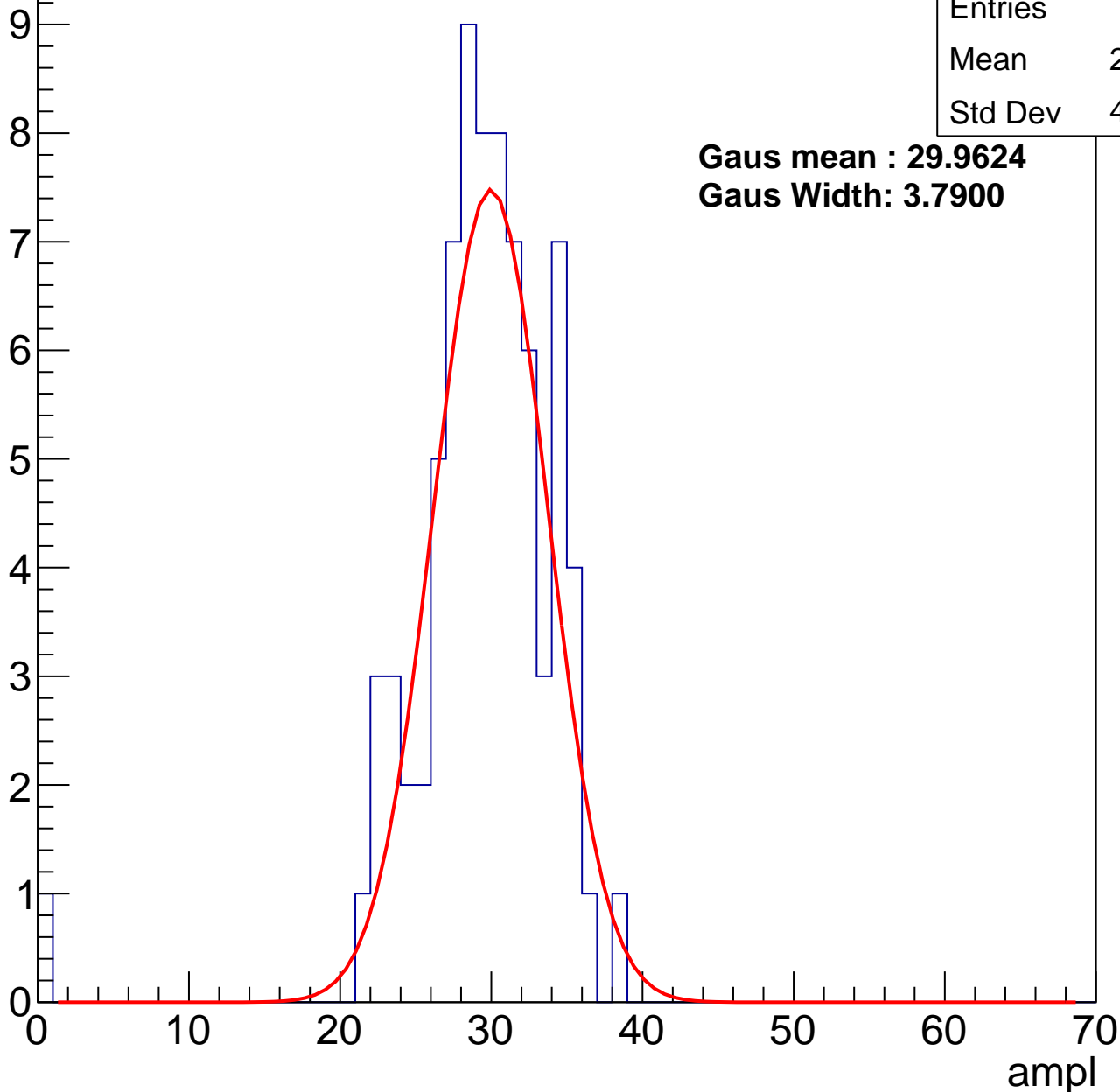
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	78
Mean	28.94
Std Dev	4.949

**Gaus mean : 29.9624**

**Gaus Width: 3.7900**



# B1L103S, U9-ch47, adc1

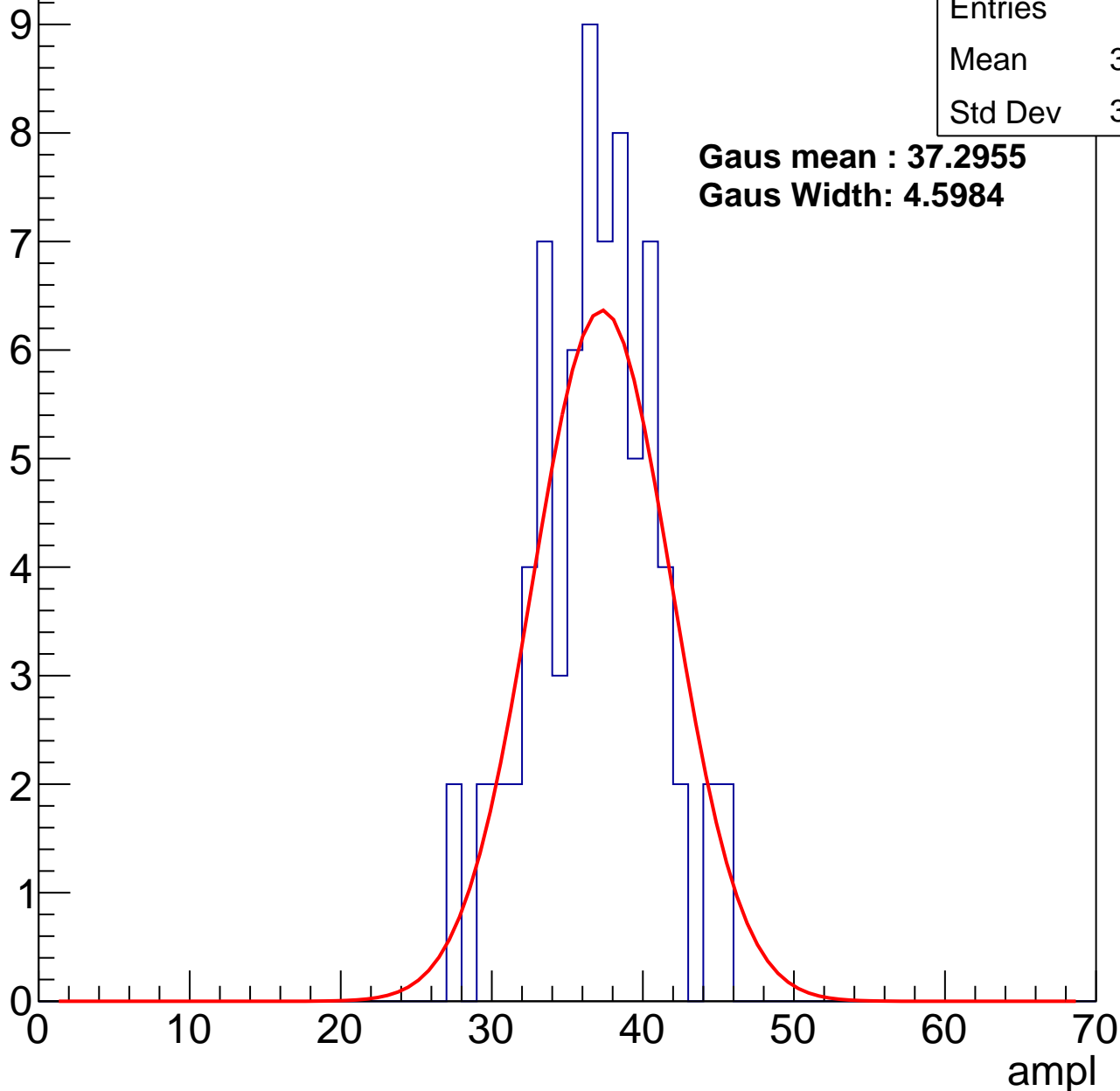
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	74
Mean	36.39
Std Dev	3.982

**Gaus mean : 37.2955**

**Gaus Width: 4.5984**



# B1L103S, U9-ch47, adc2

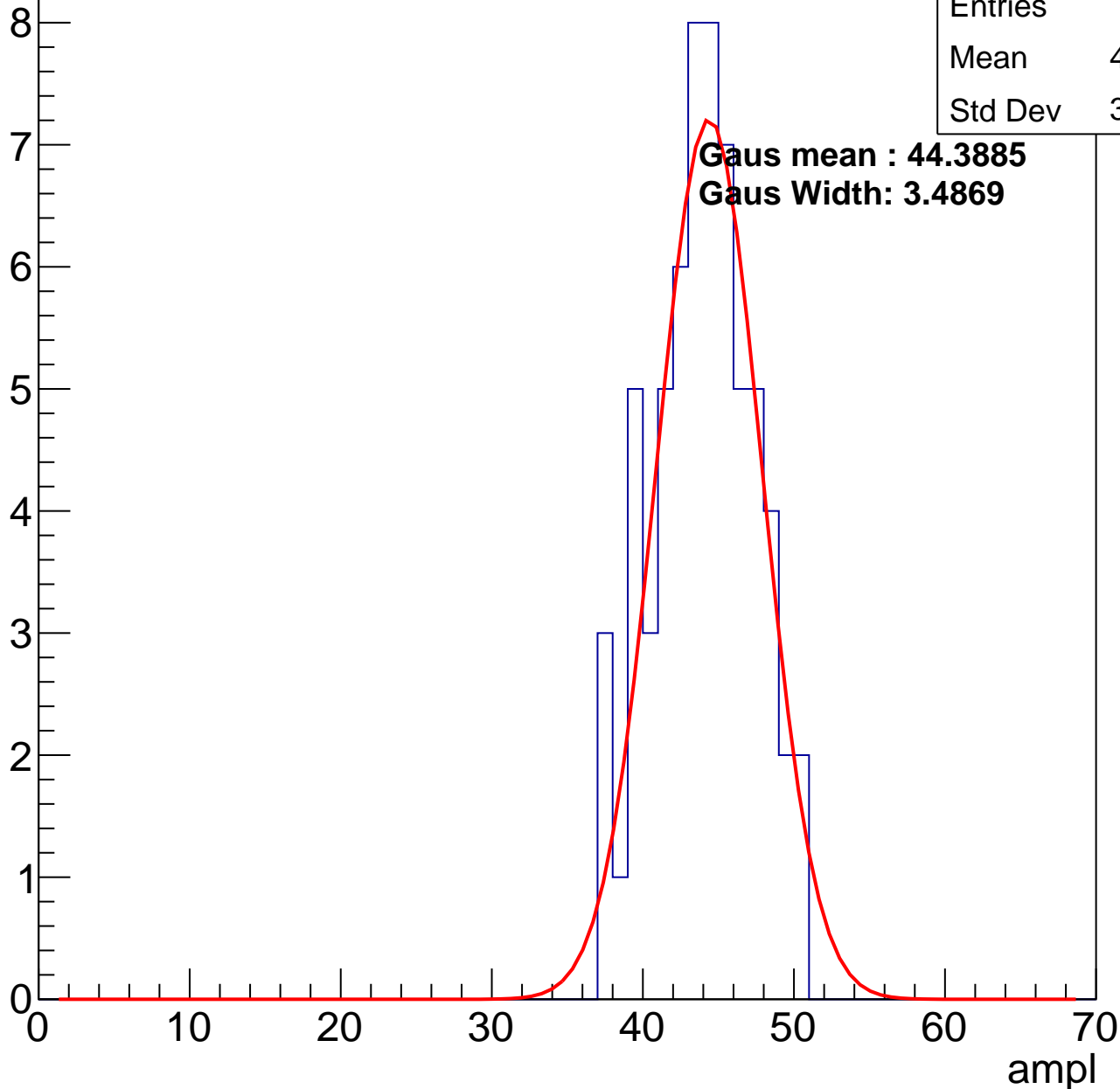
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	43.55
Std Dev	3.254

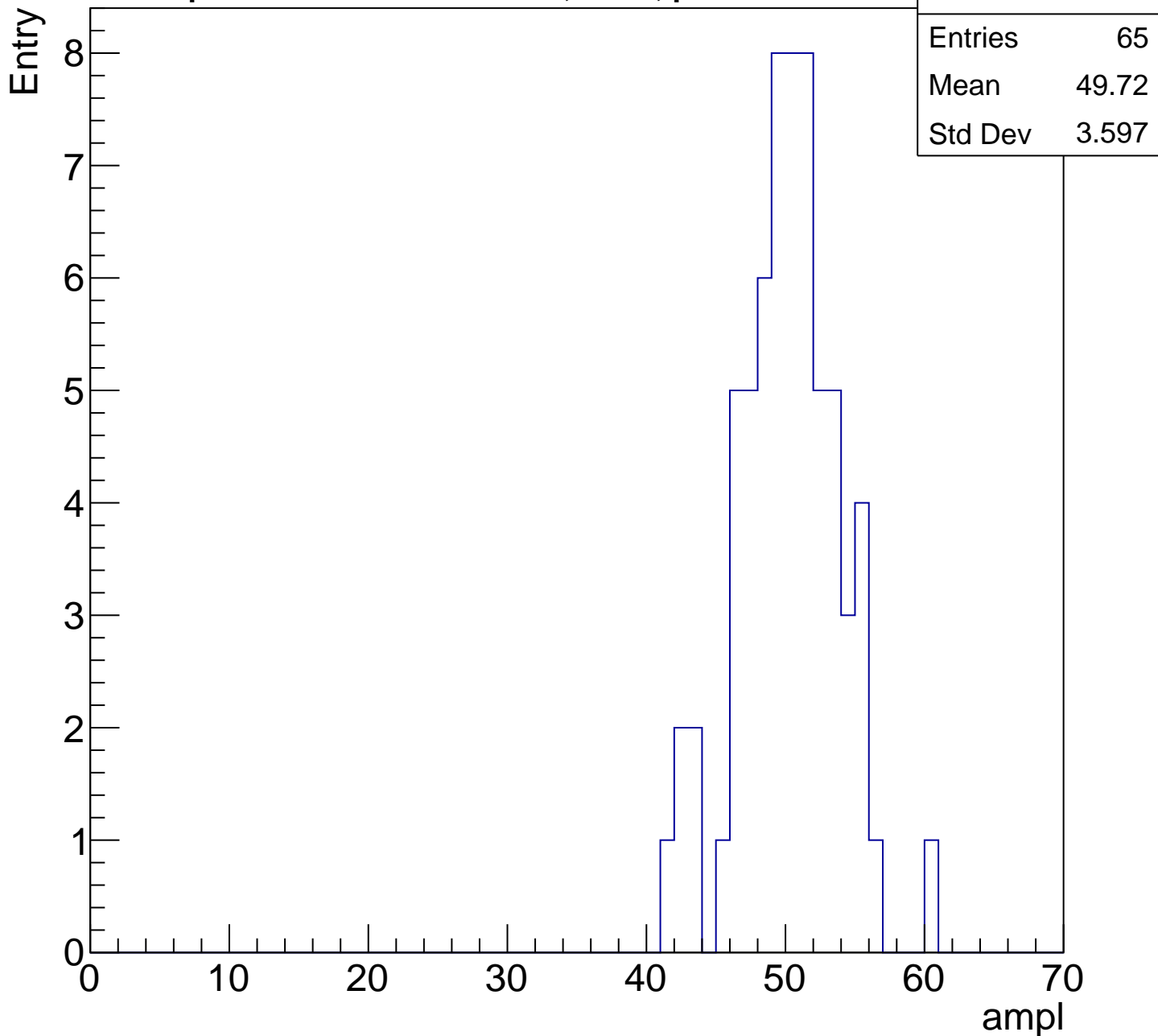
**Gaus mean : 44.3885**

**Gaus Width: 3.4869**



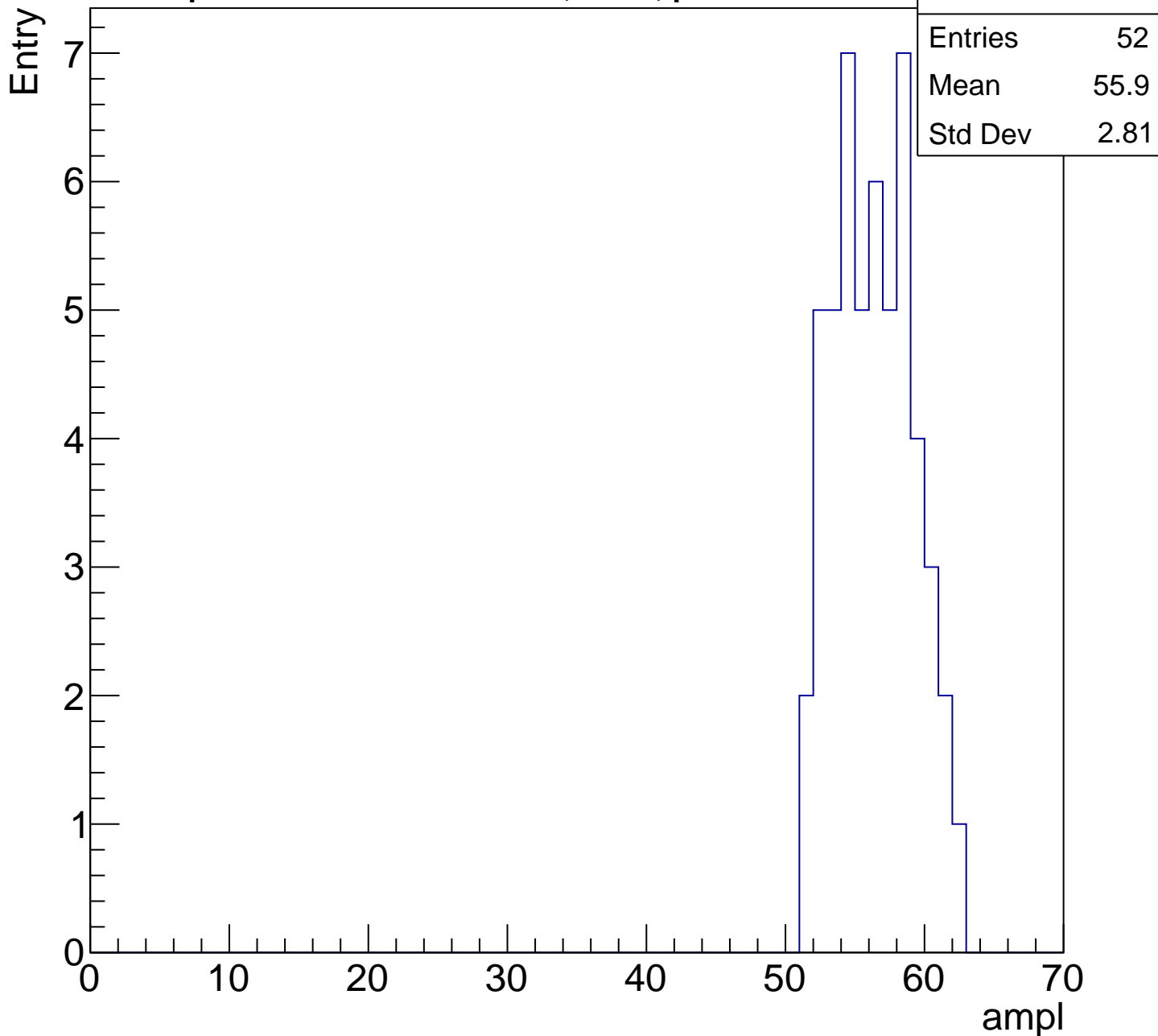
# B1L103S, U9-ch47, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U9-ch47, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

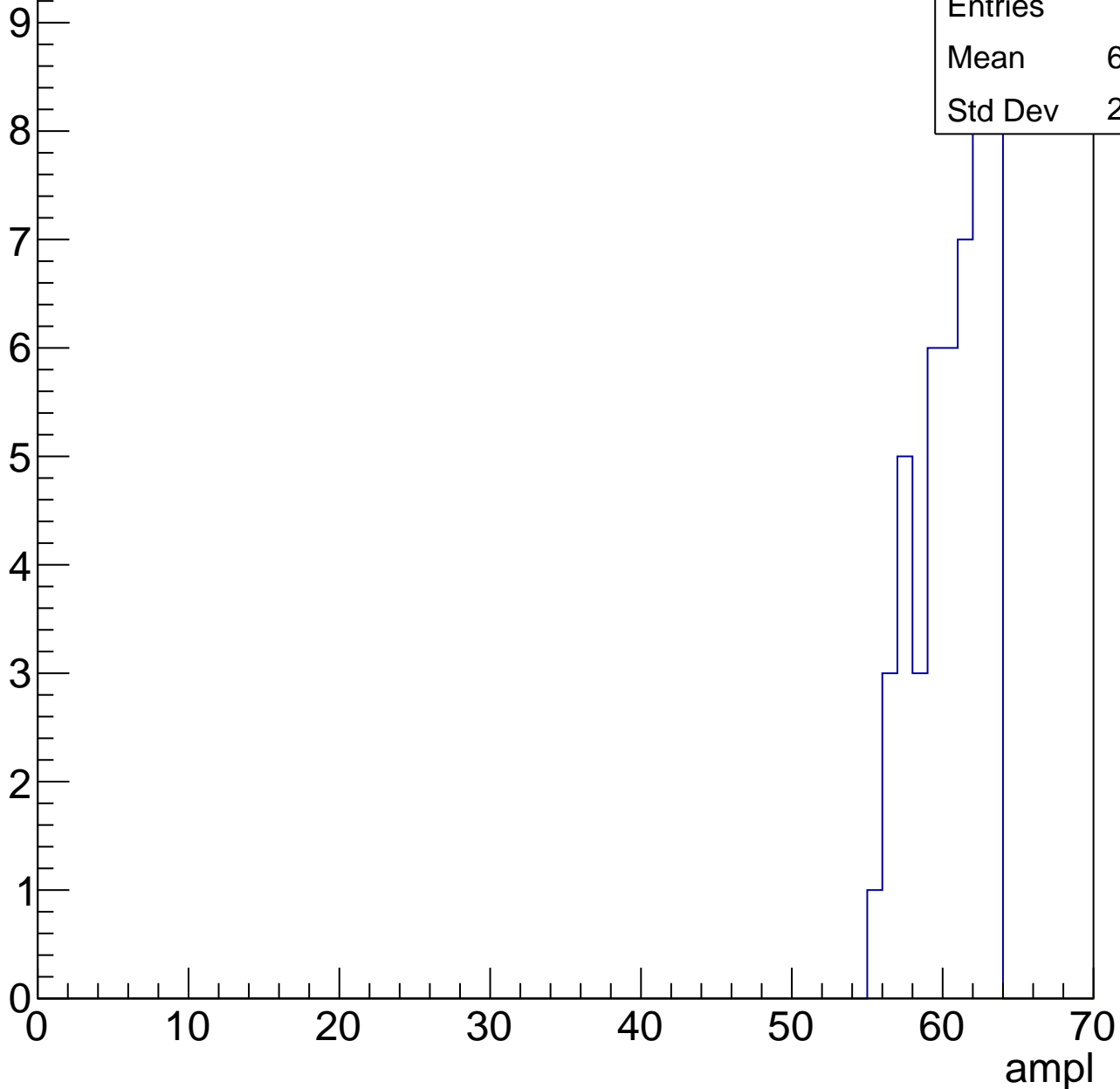


# B1L103S, U9-ch47, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	48
Mean	60.12
Std Dev	2.306



# B1L103S, U9-ch47, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U9-ch47, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U9-ch48, adc0

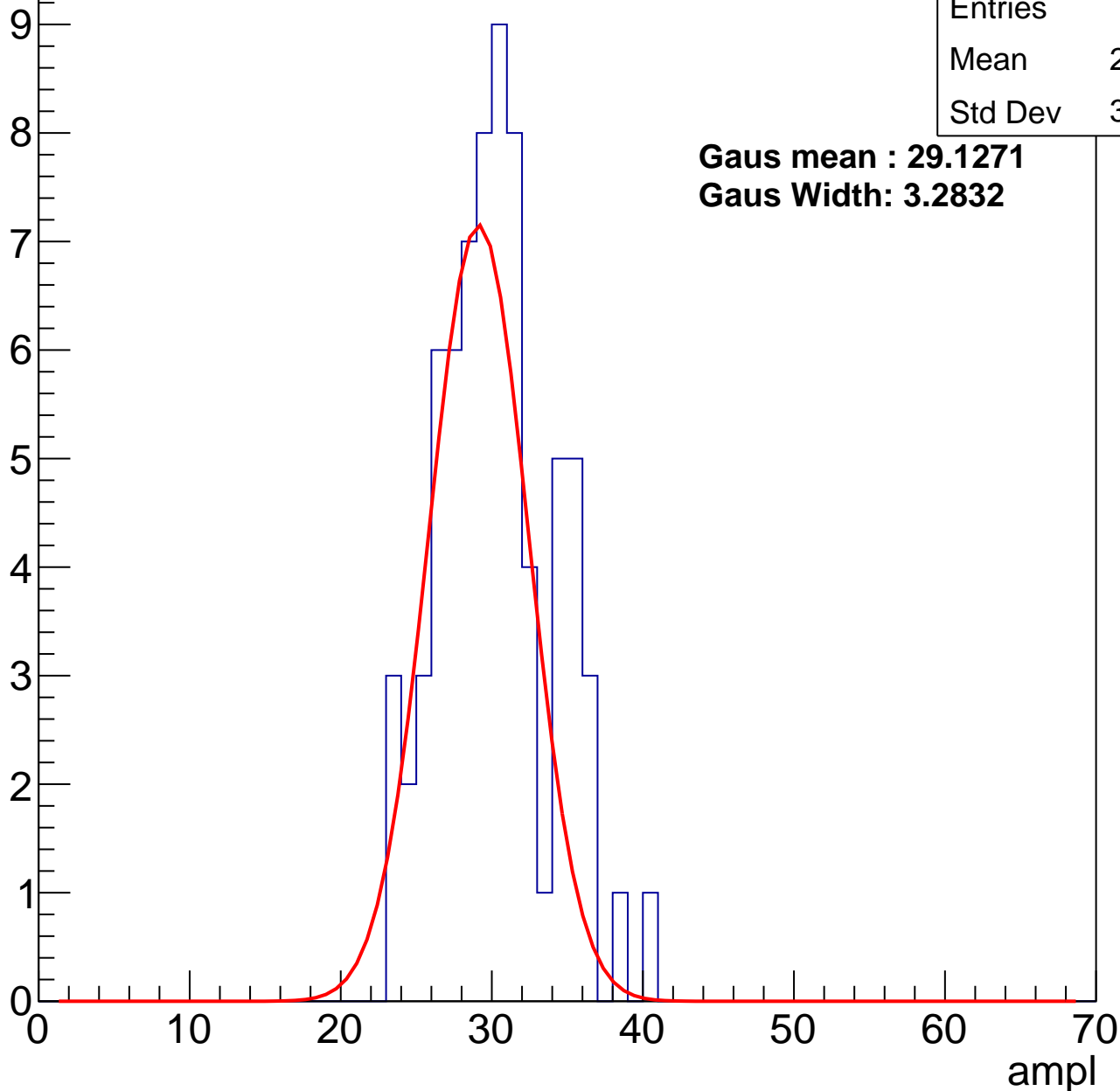
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	72
Mean	29.83
Std Dev	3.704

**Gaus mean : 29.1271**

**Gaus Width: 3.2832**



# B1L103S, U9-ch48, adc1

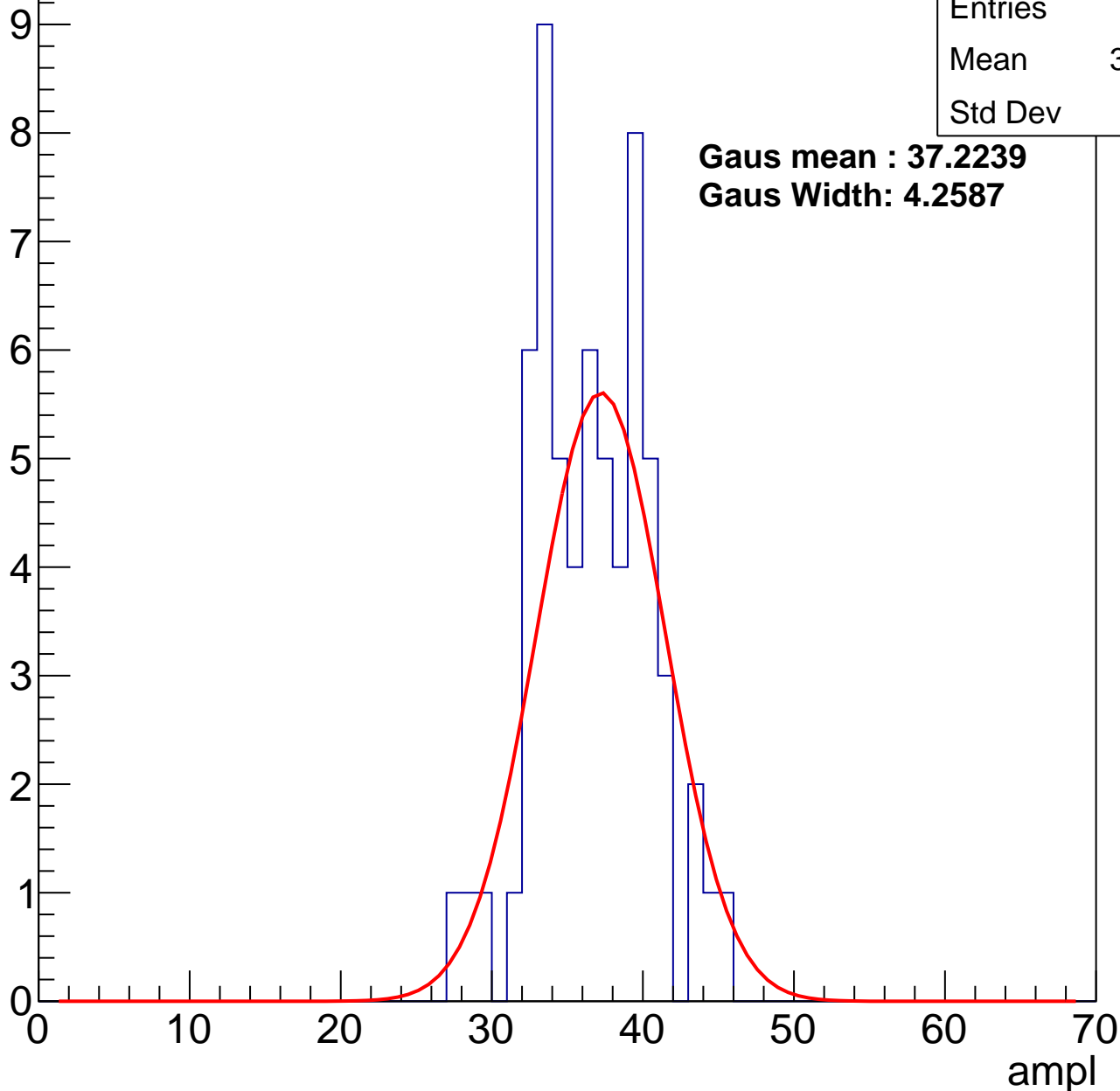
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	36.14
Std Dev	3.8

**Gaus mean : 37.2239**

**Gaus Width: 4.2587**



# B1L103S, U9-ch48, adc2

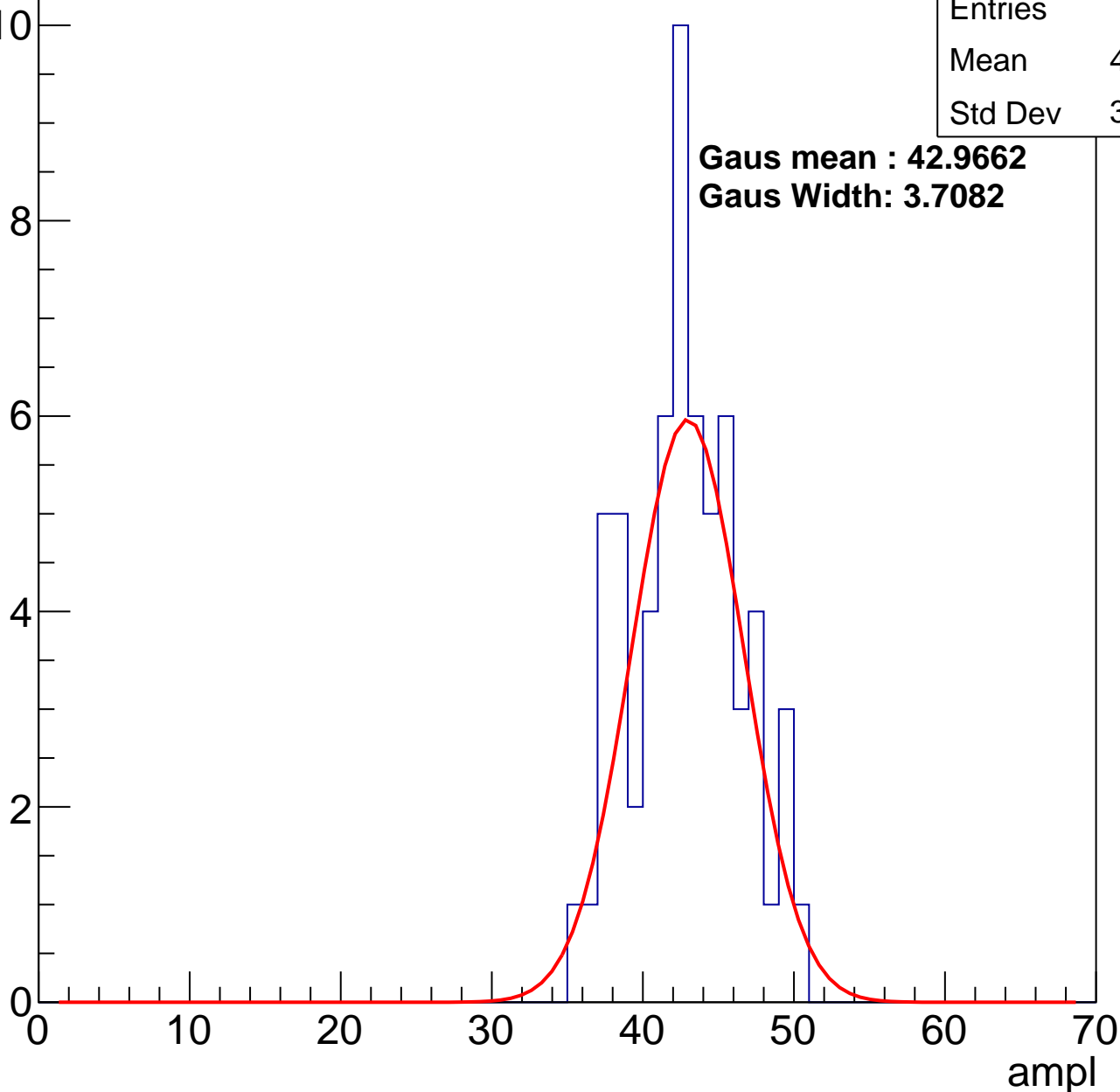
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	42.37
Std Dev	3.556

**Gaus mean : 42.9662**

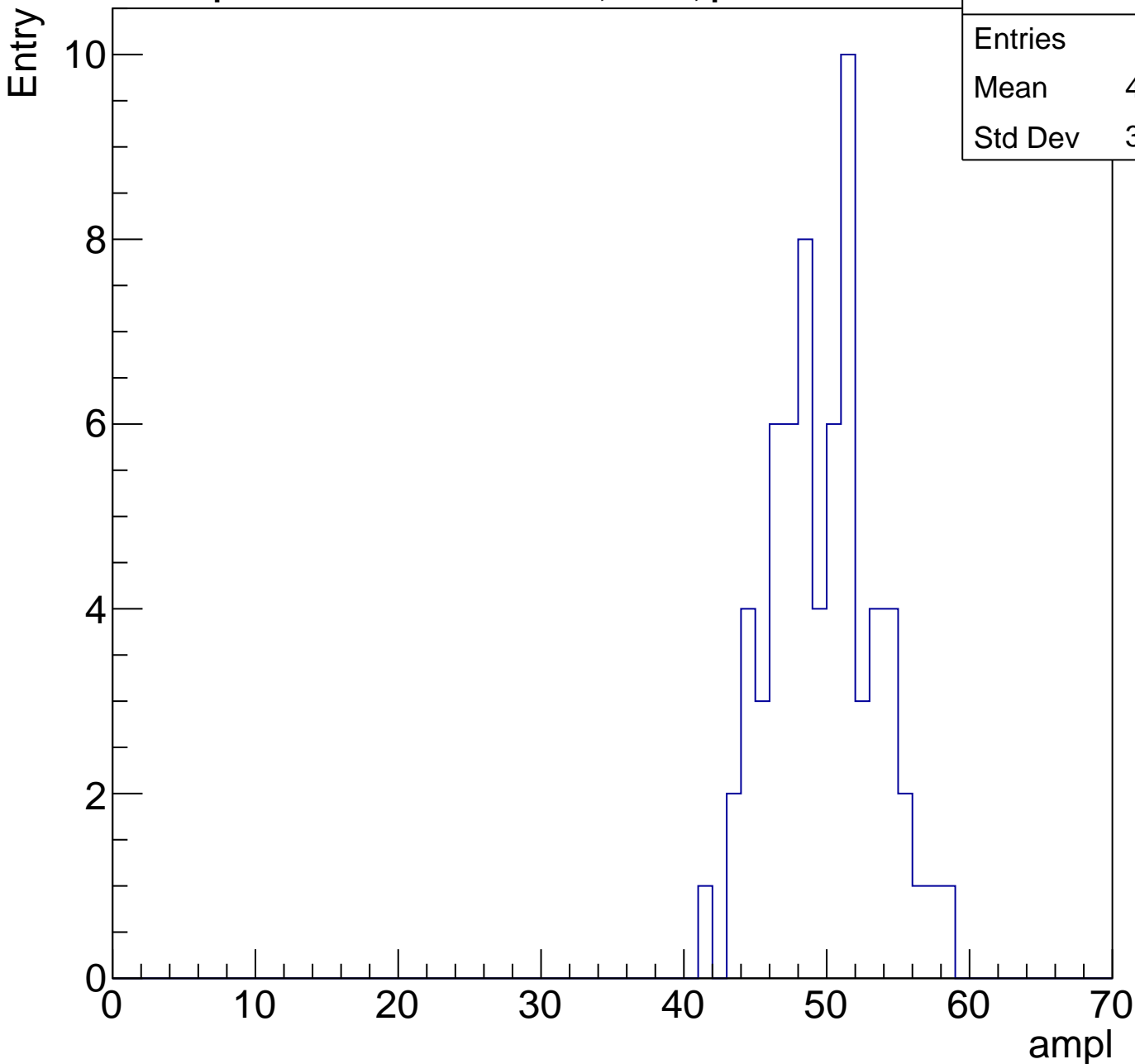
**Gaus Width: 3.7082**



# B1L103S, U9-ch48, adc3

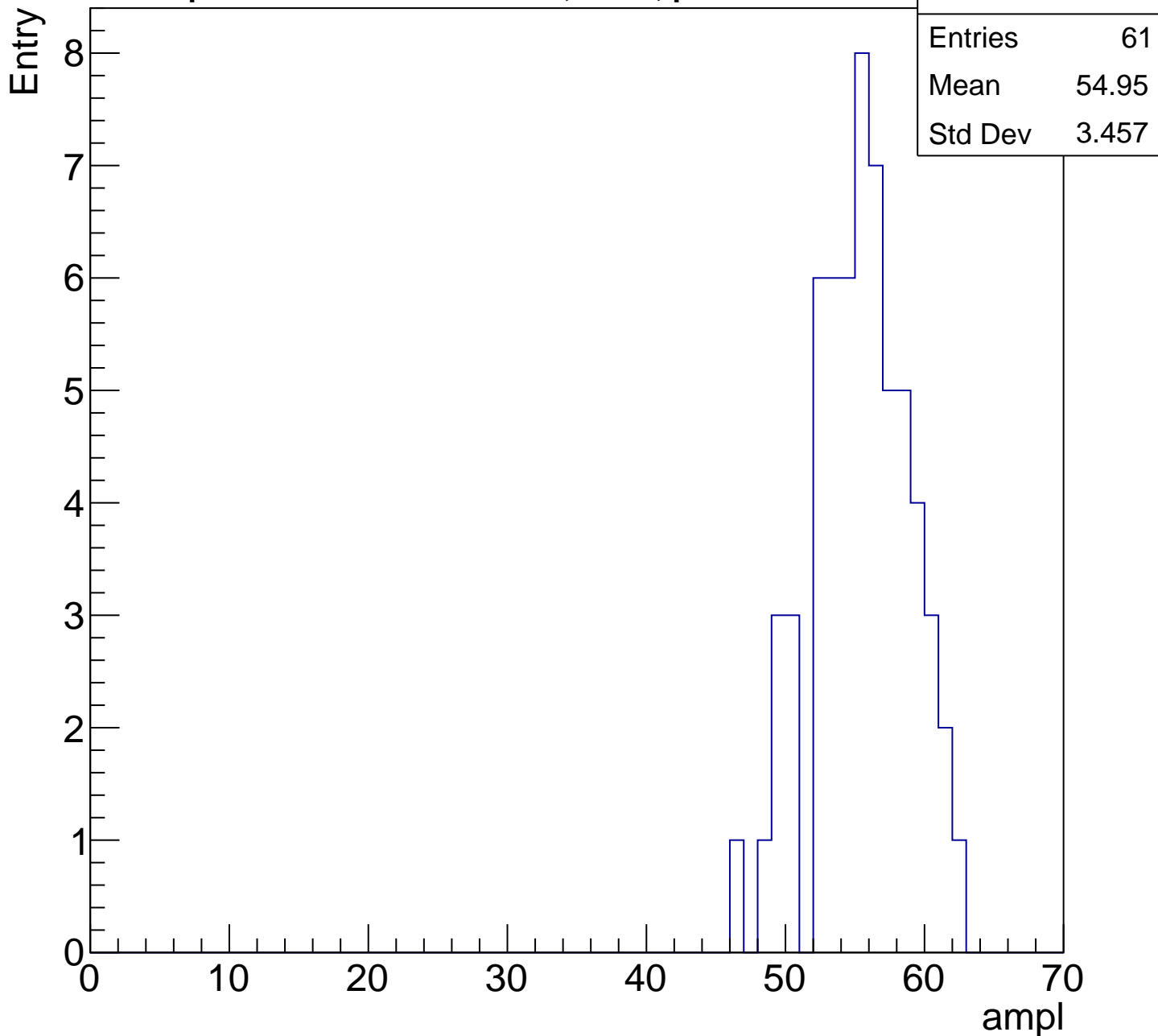
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	66
Mean	49.26
Std Dev	3.628



# B1L103S, U9-ch48, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

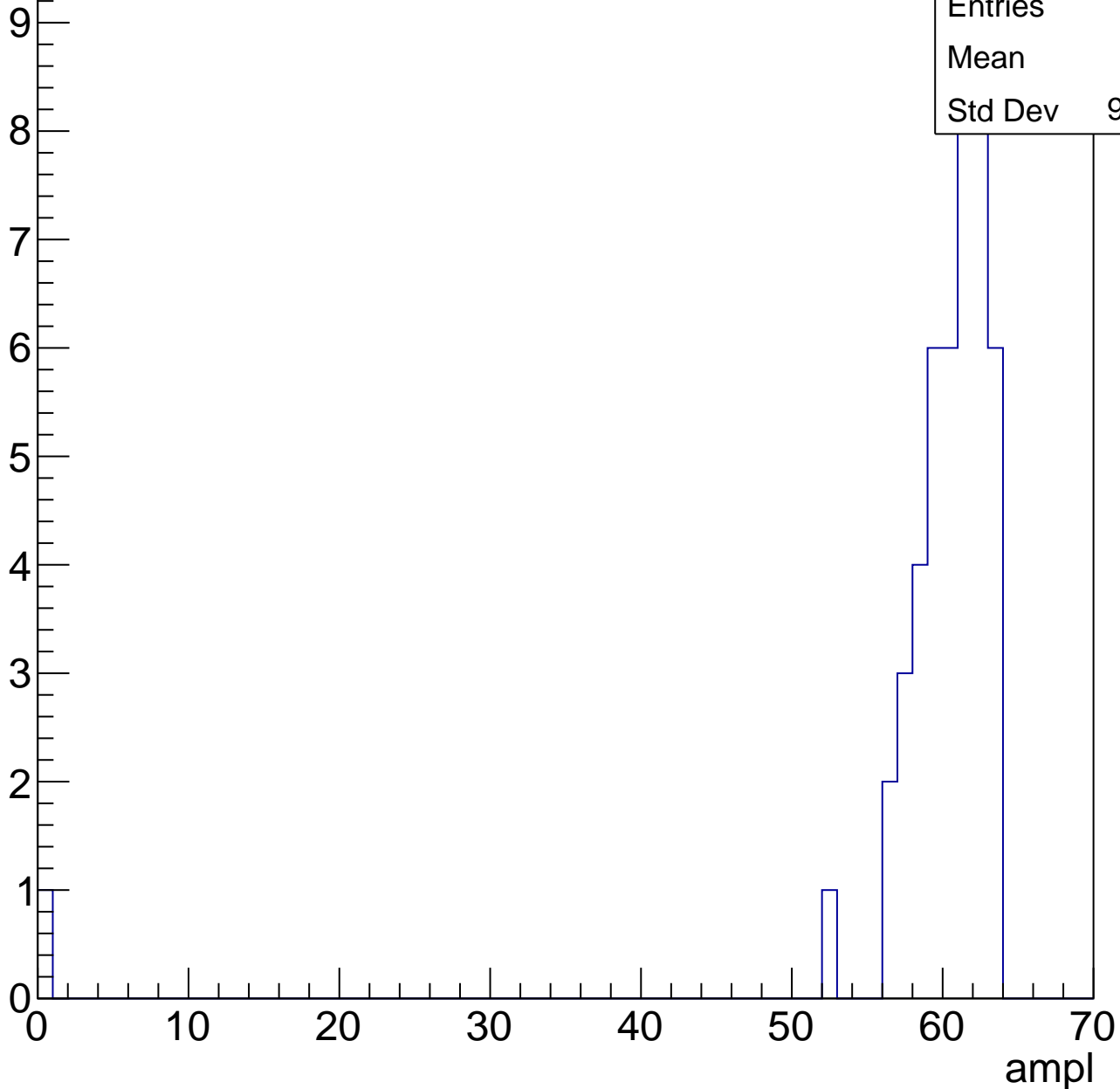


# B1L103S, U9-ch48, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

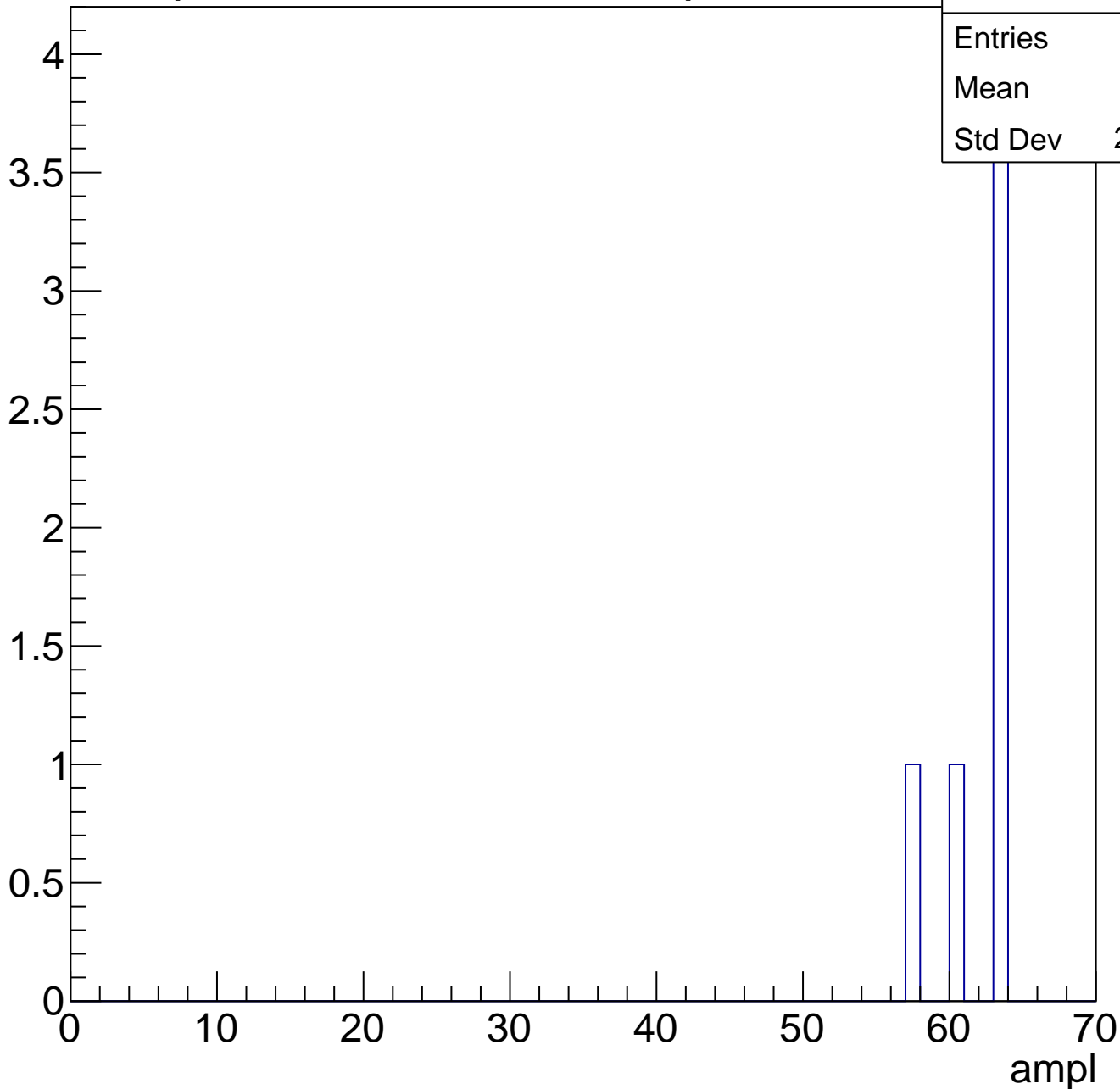
Entries	46
Mean	58.8
Std Dev	9.062



# B1L103S, U9-ch48, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U9-ch48, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	2
Mean	11.5
Std Dev	11.5

# B1L103S, U9-ch49, adc0

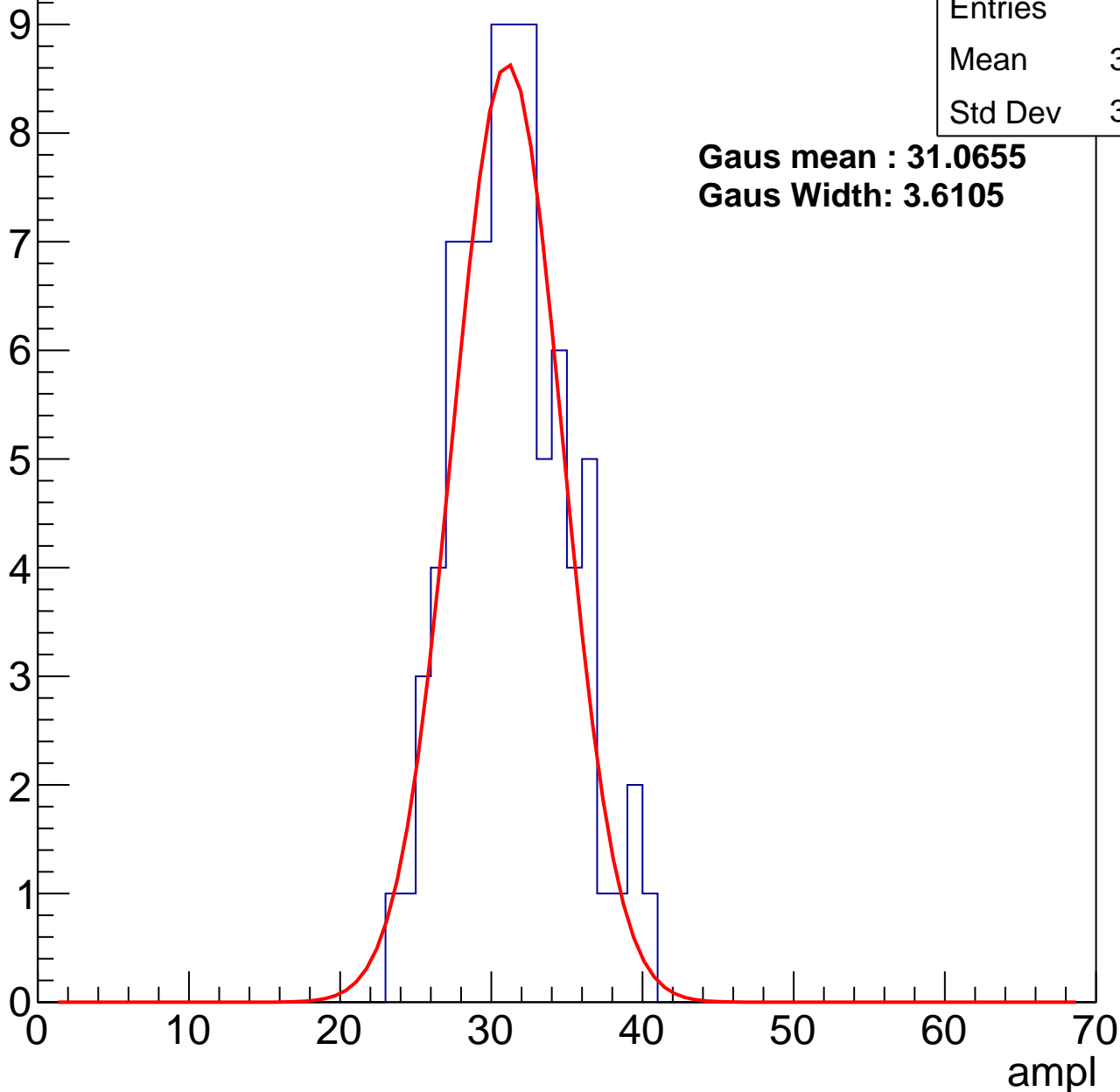
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	82
Mean	30.89
Std Dev	3.659

**Gaus mean : 31.0655**

**Gaus Width: 3.6105**



# B1L103S, U9-ch49, adc1

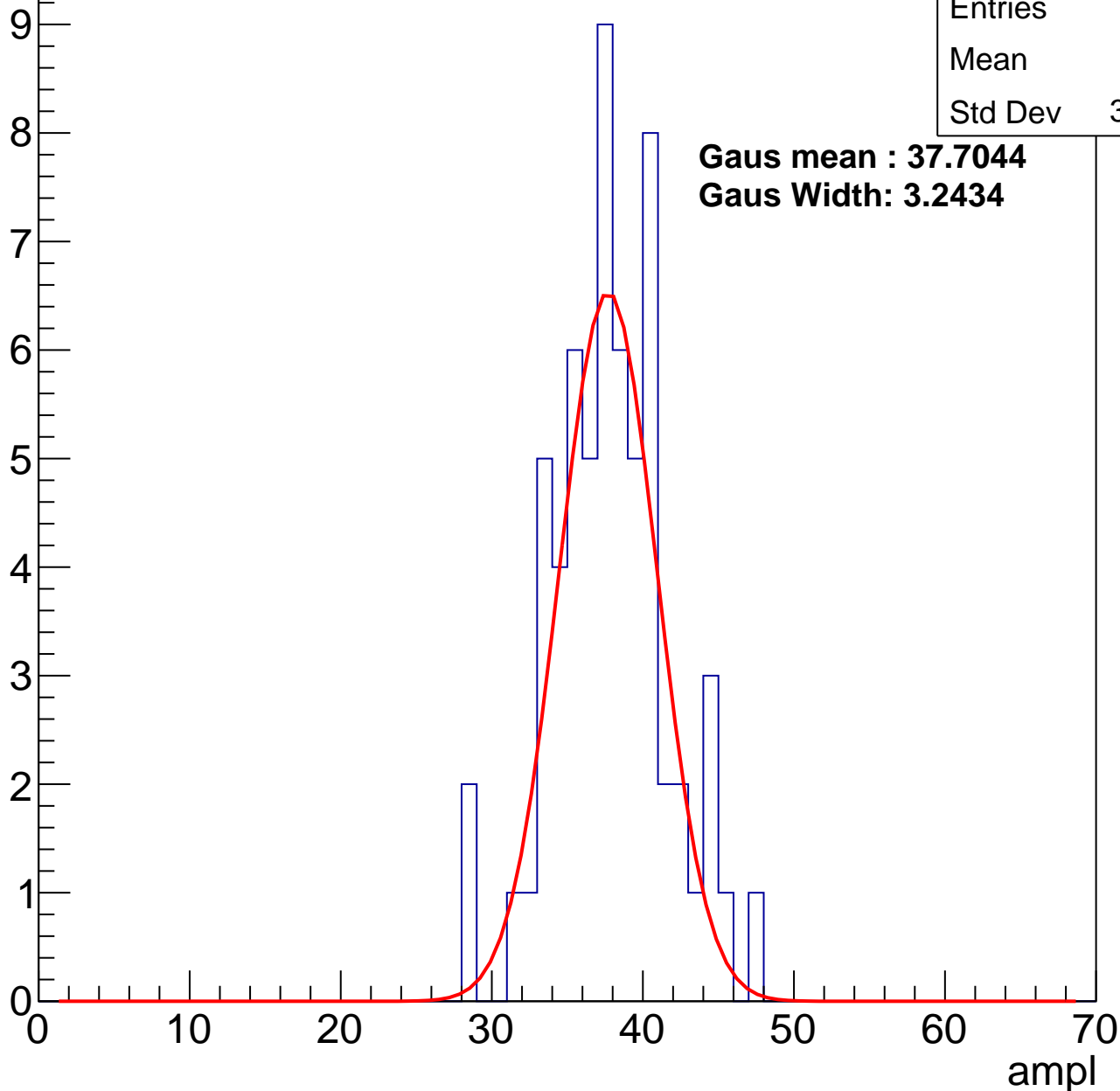
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	37.4
Std Dev	3.778

**Gaus mean : 37.7044**

**Gaus Width: 3.2434**



# B1L103S, U9-ch49, adc2

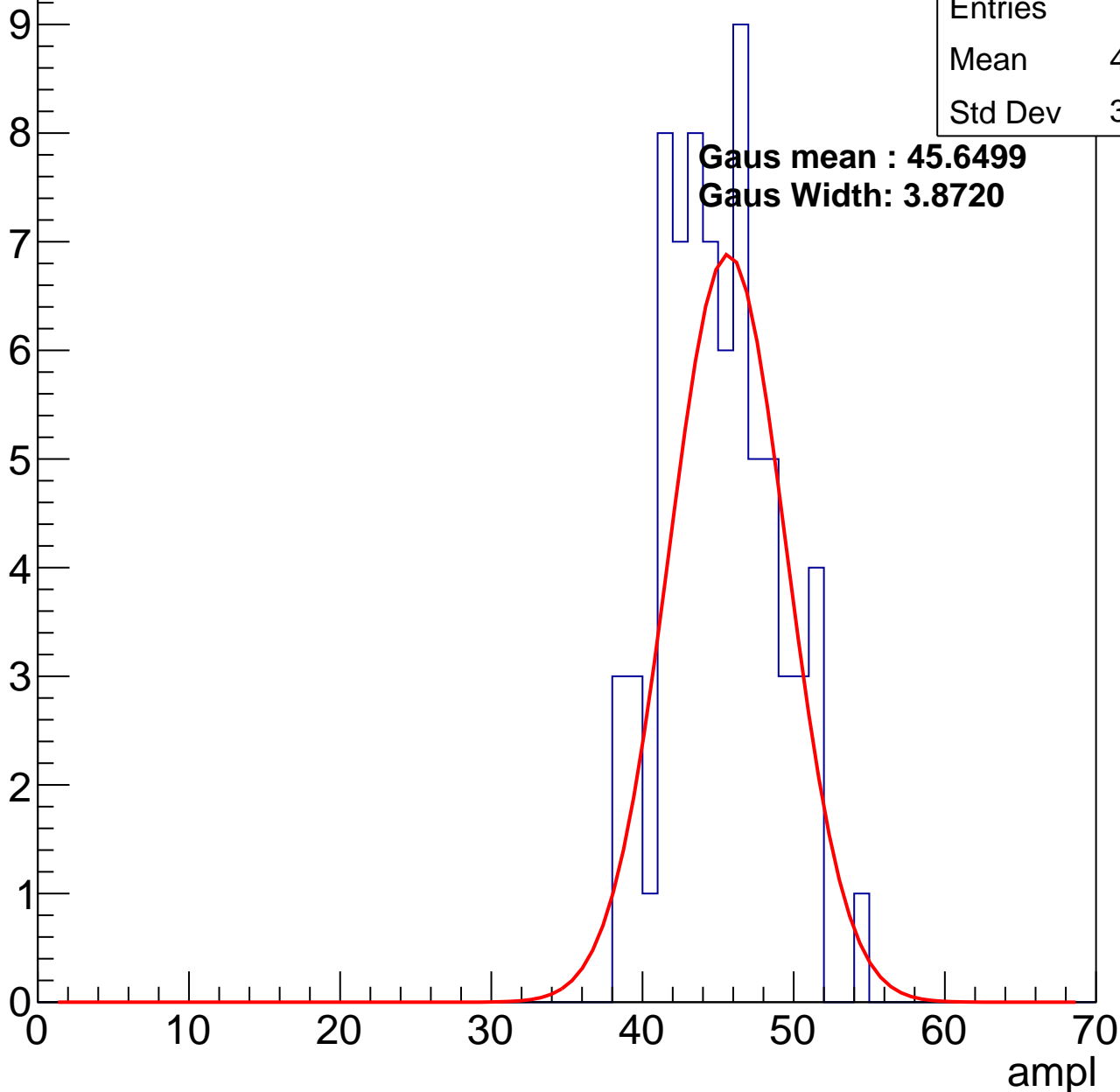
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	73
Mean	44.64
Std Dev	3.555

**Gaus mean : 45.6499**

**Gaus Width: 3.8720**

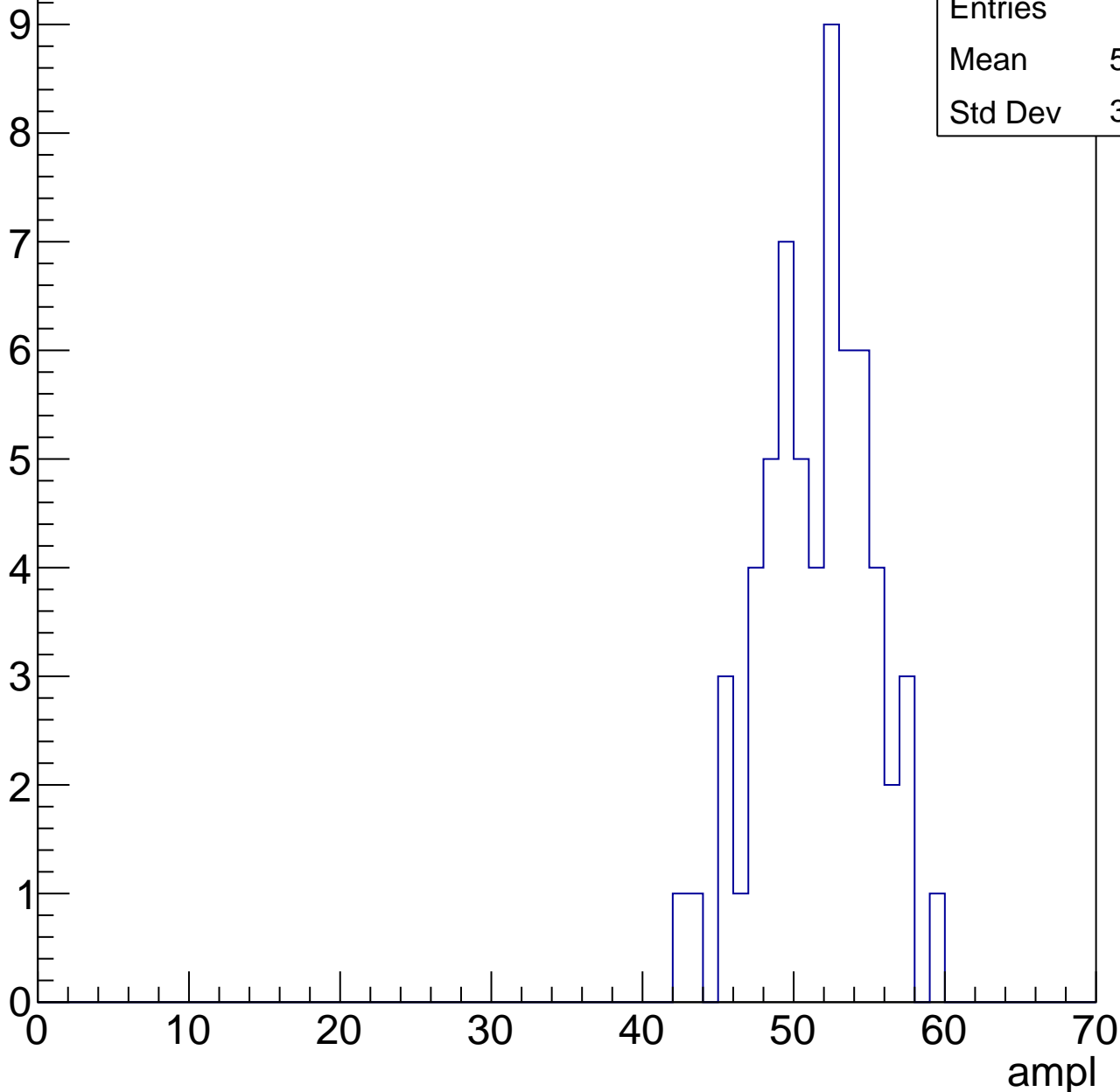


# B1L103S, U9-ch49, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

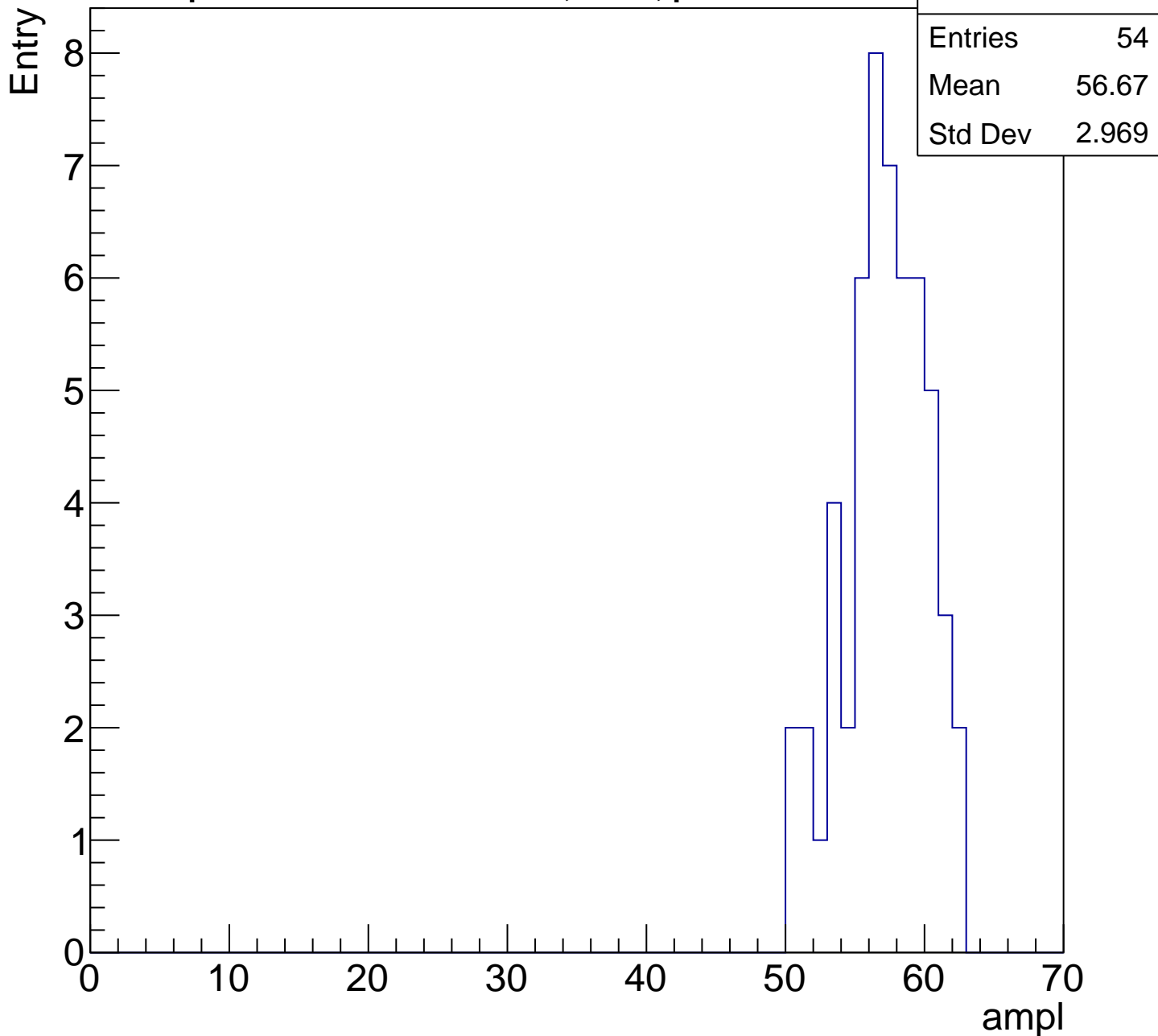
Entry

Entries	62
Mean	51.02
Std Dev	3.576



# B1L103S, U9-ch49, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

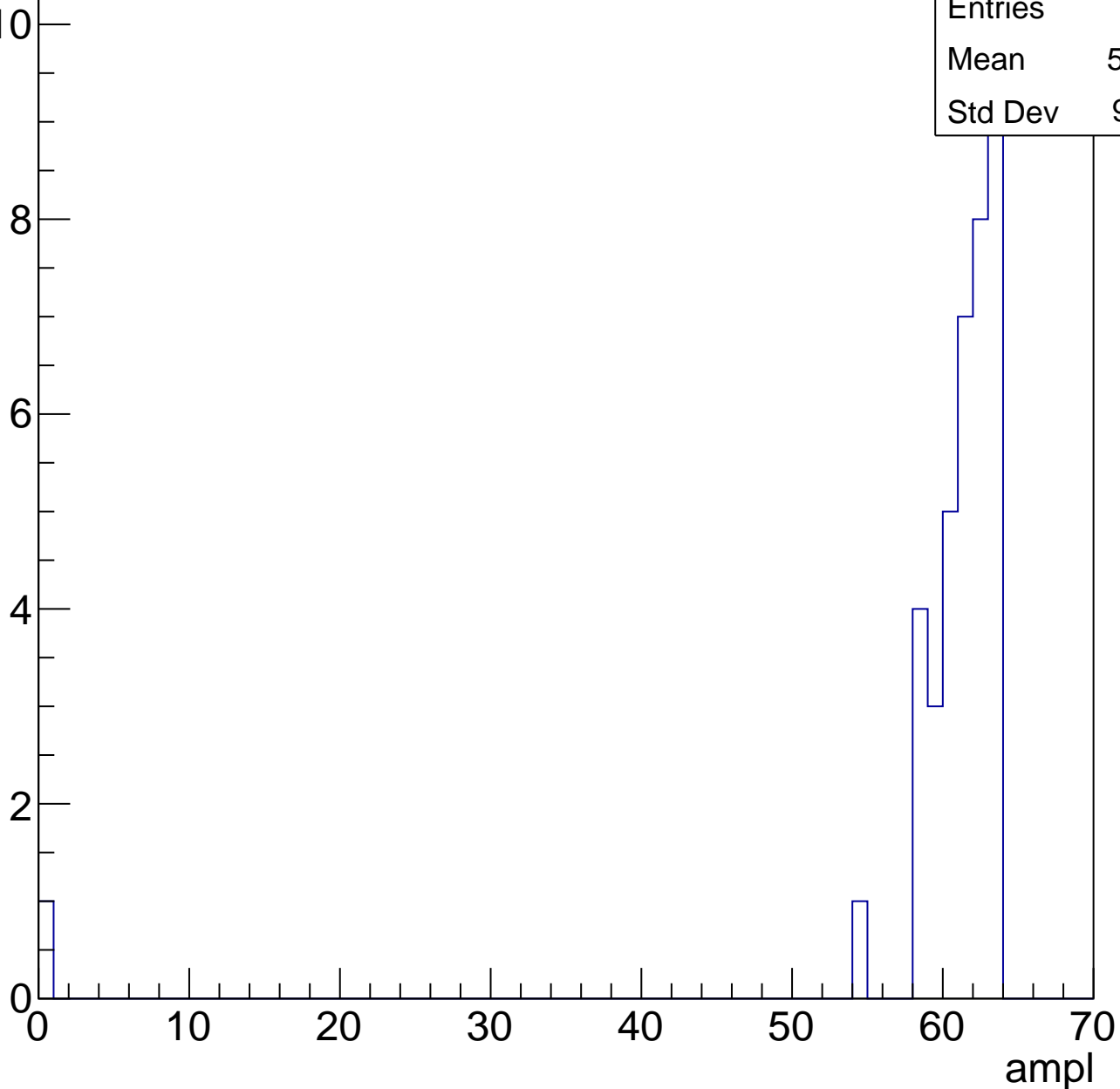


# B1L103S, U9-ch49, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	39
Mean	59.38
Std Dev	9.831



# B1L103S, U9-ch49, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0



# B1L103S, U9-ch49, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L103S, U9-ch50, adc0

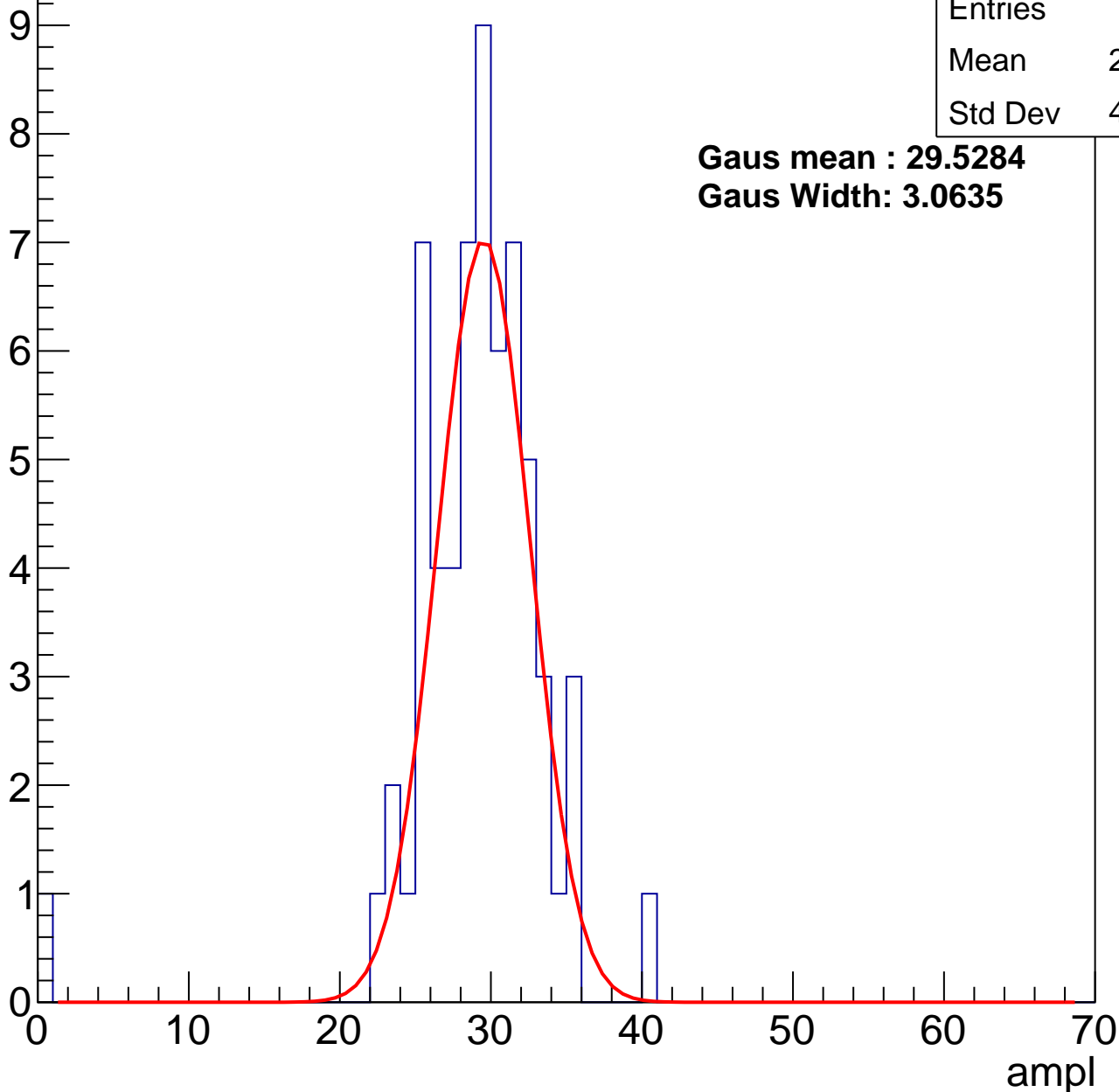
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	28.56
Std Dev	4.963

**Gaus mean : 29.5284**

**Gaus Width: 3.0635**



# B1L103S, U9-ch50, adc1

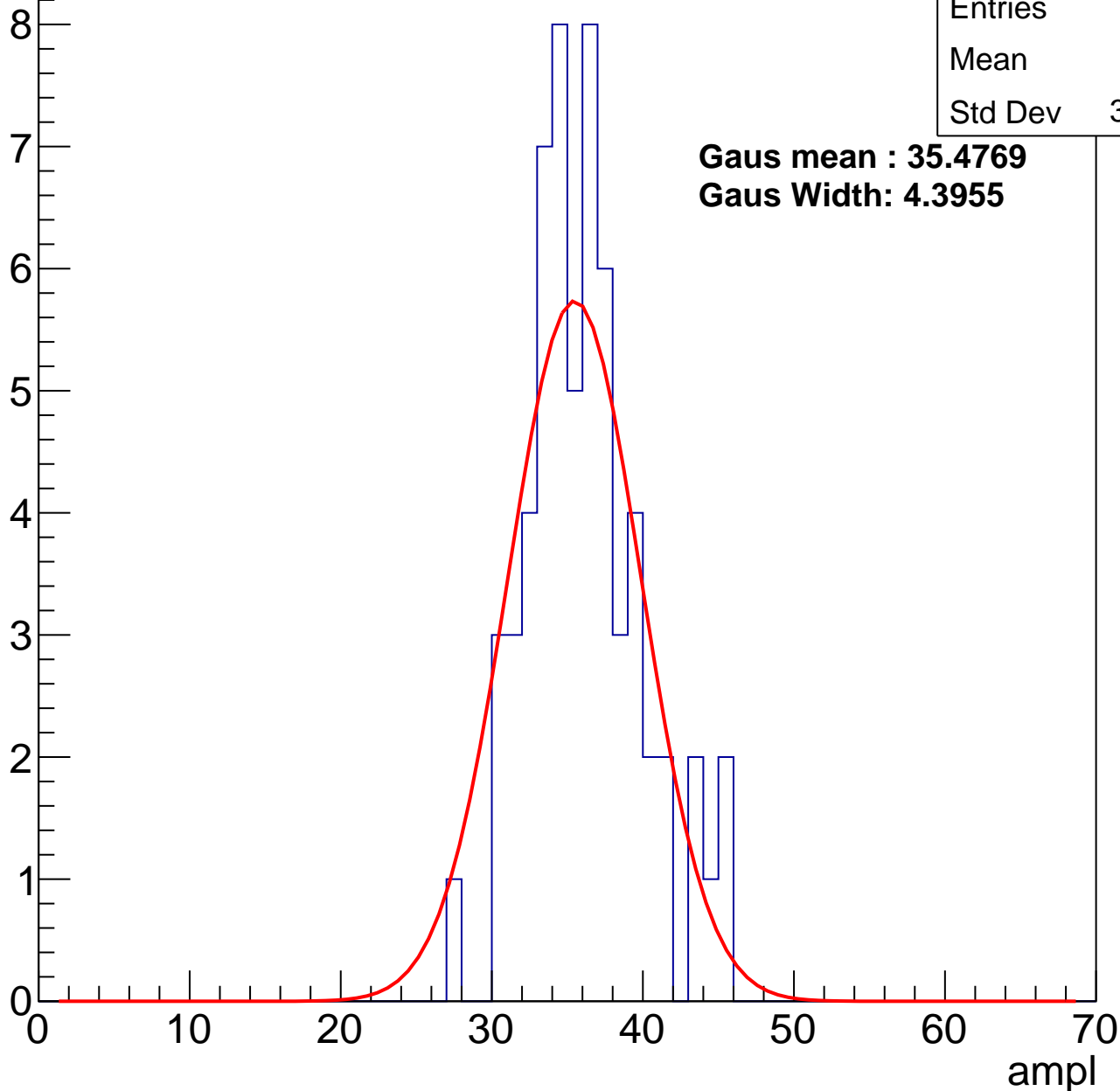
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	61
Mean	35.7
Std Dev	3.804

**Gaus mean : 35.4769**

**Gaus Width: 4.3955**



# B1L103S, U9-ch50, adc2

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	71
Mean	41.86
Std Dev	3.948

**Gaus mean : 42.1442**

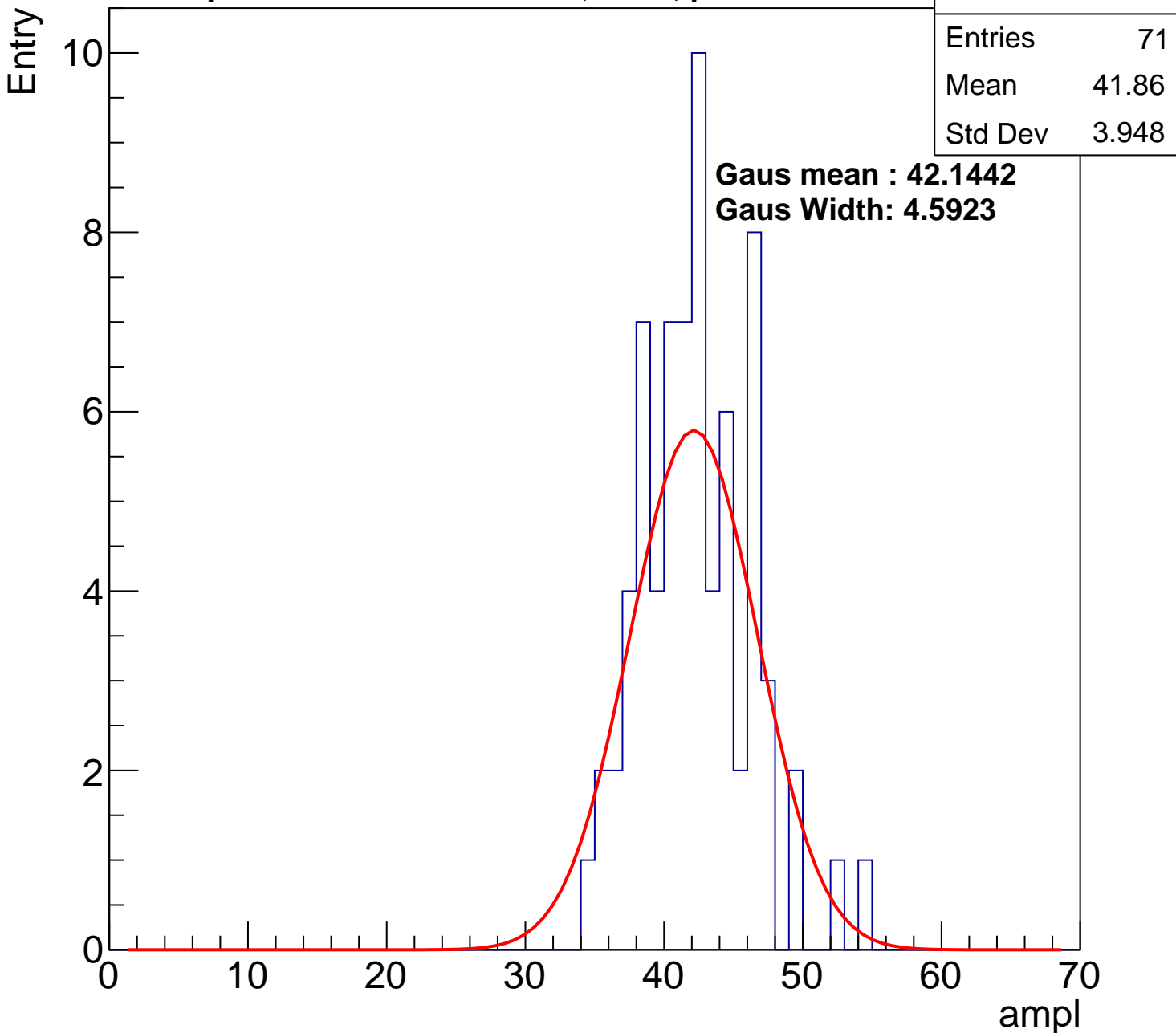
**Gaus Width: 4.5923**

Entry

10  
8  
6  
4  
2  
0

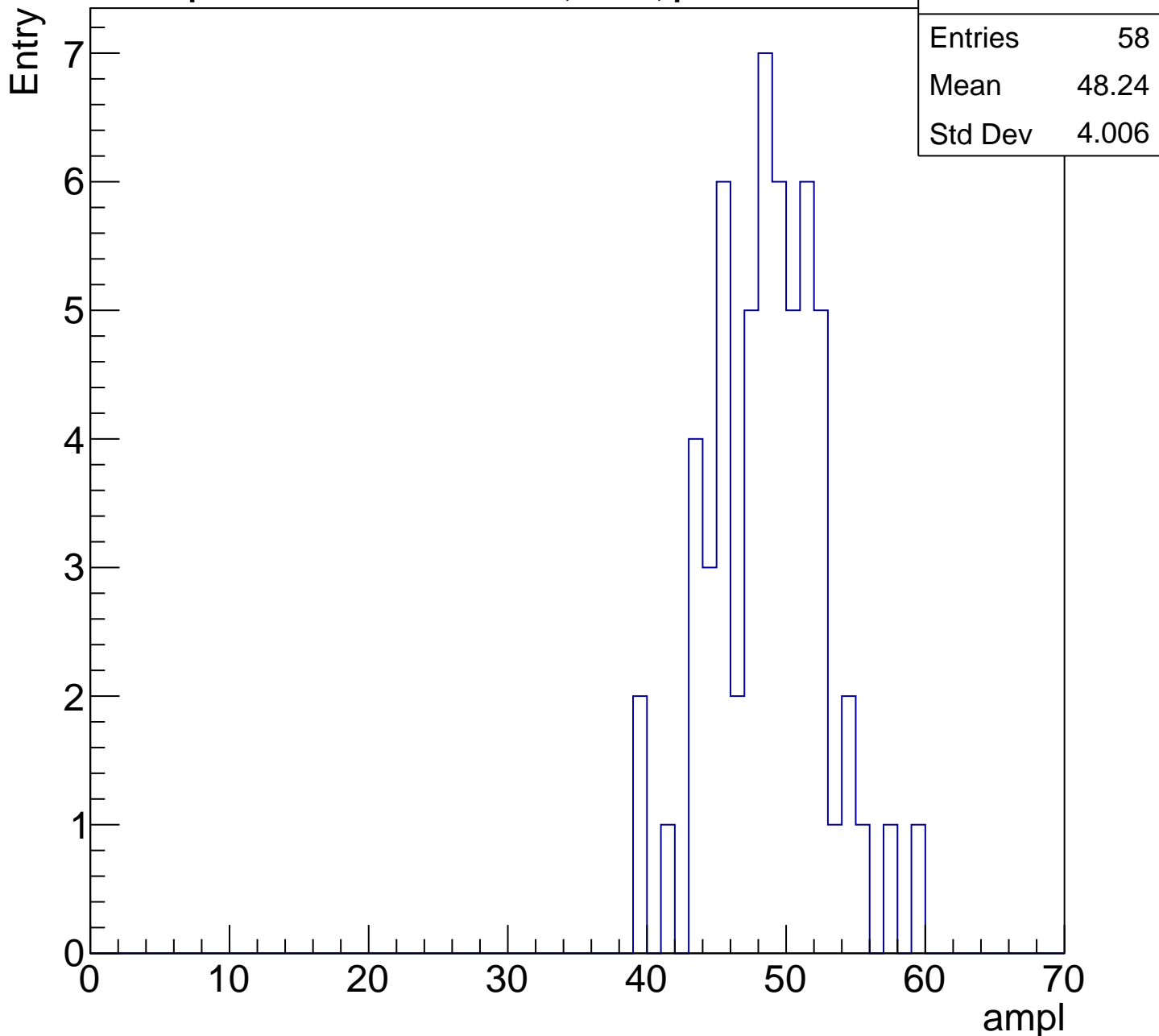
ampl

0 10 20 30 40 50 60 70



# B1L103S, U9-ch50, adc3

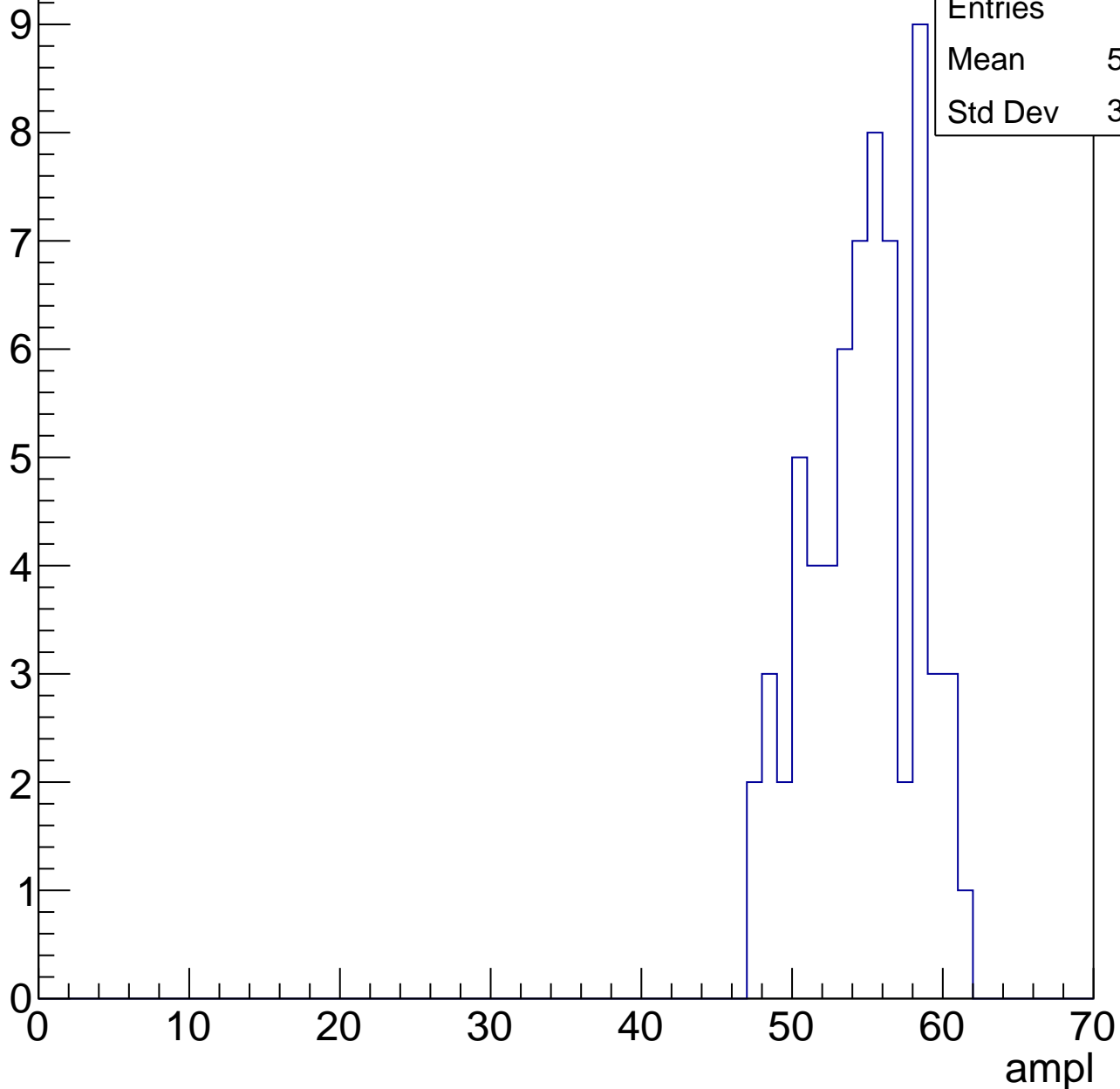
calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U9-ch50, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

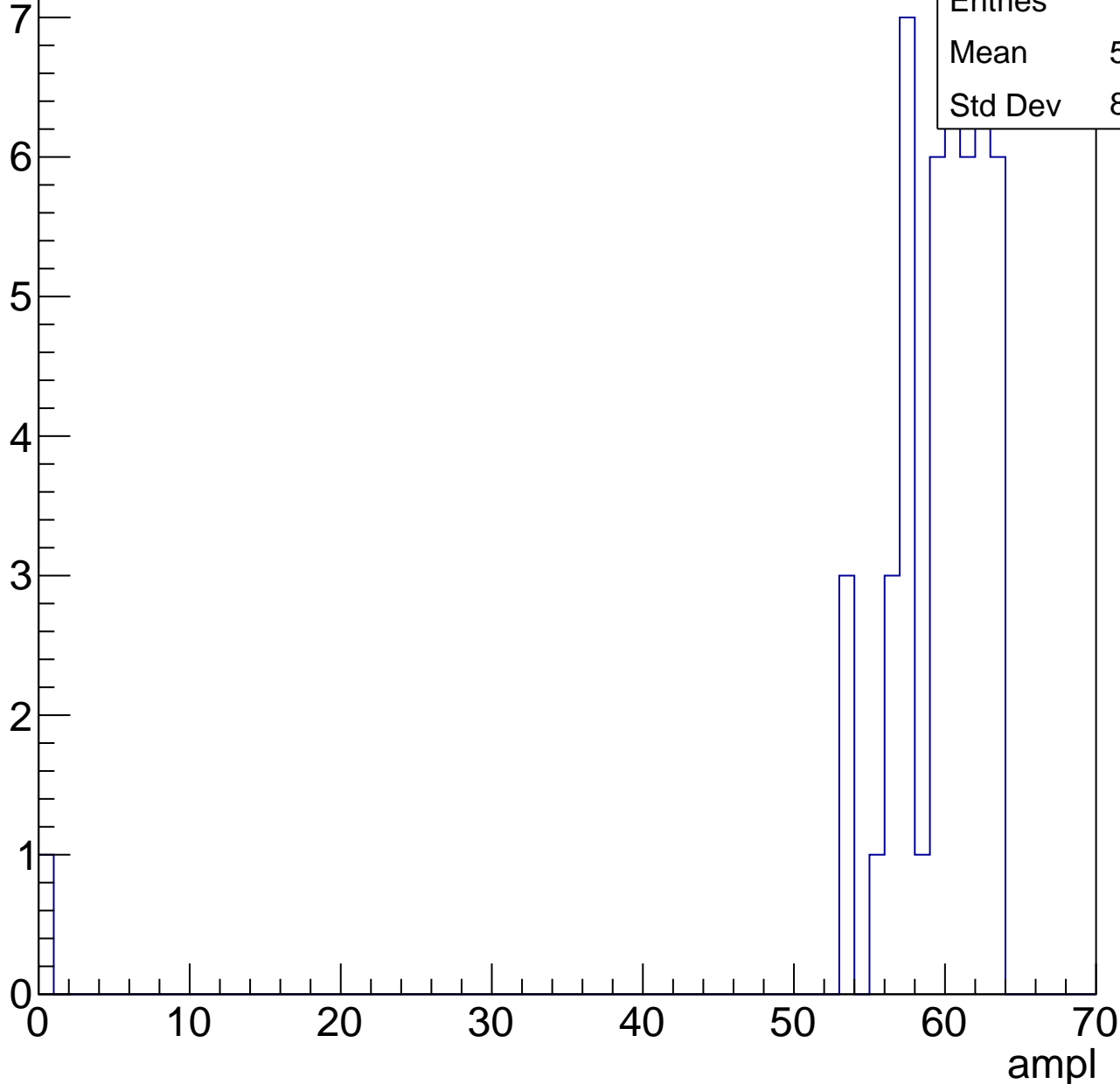
Entry



# B1L103S, U9-ch50, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

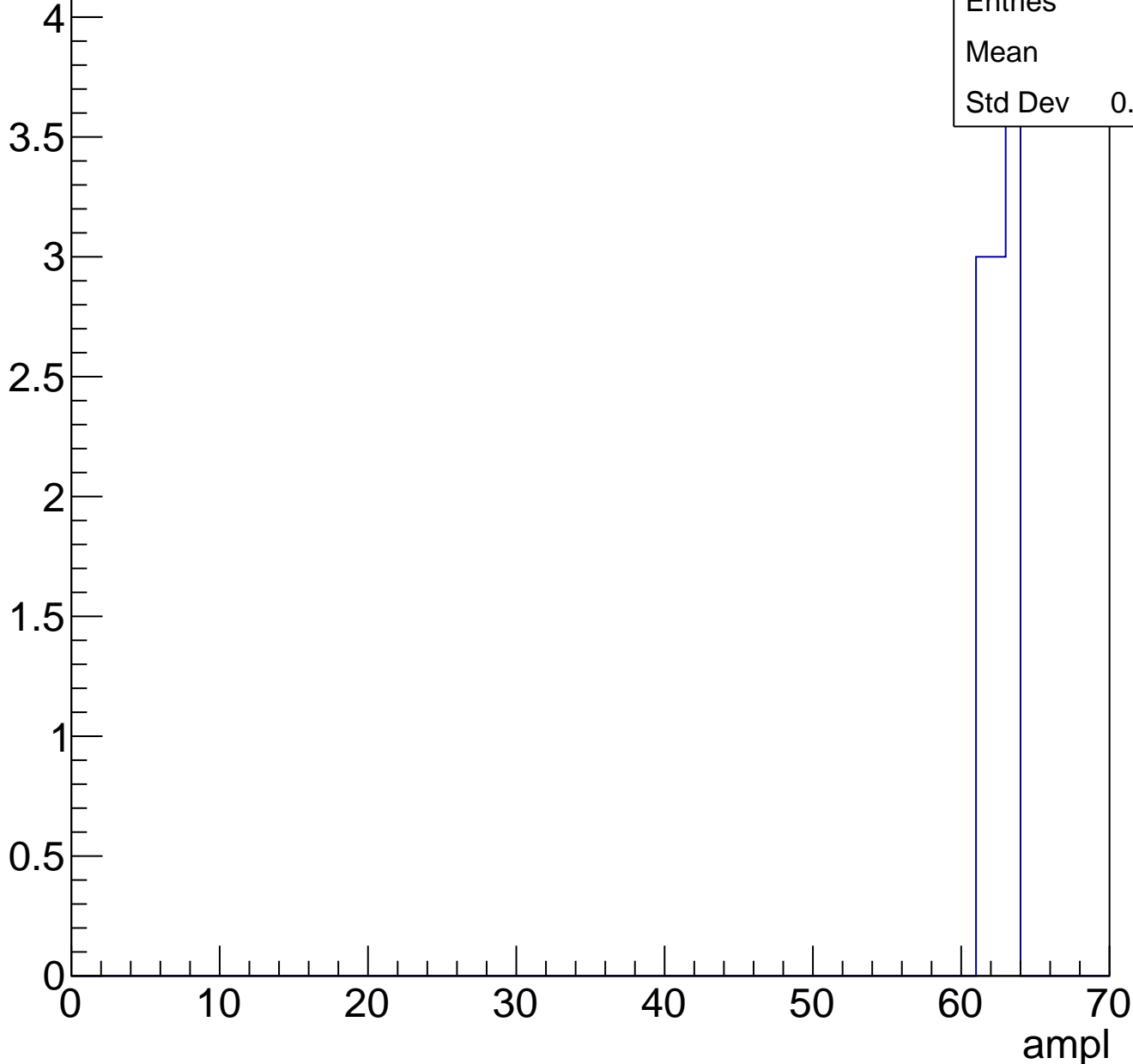
Entry



# B1L103S, U9-ch50, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

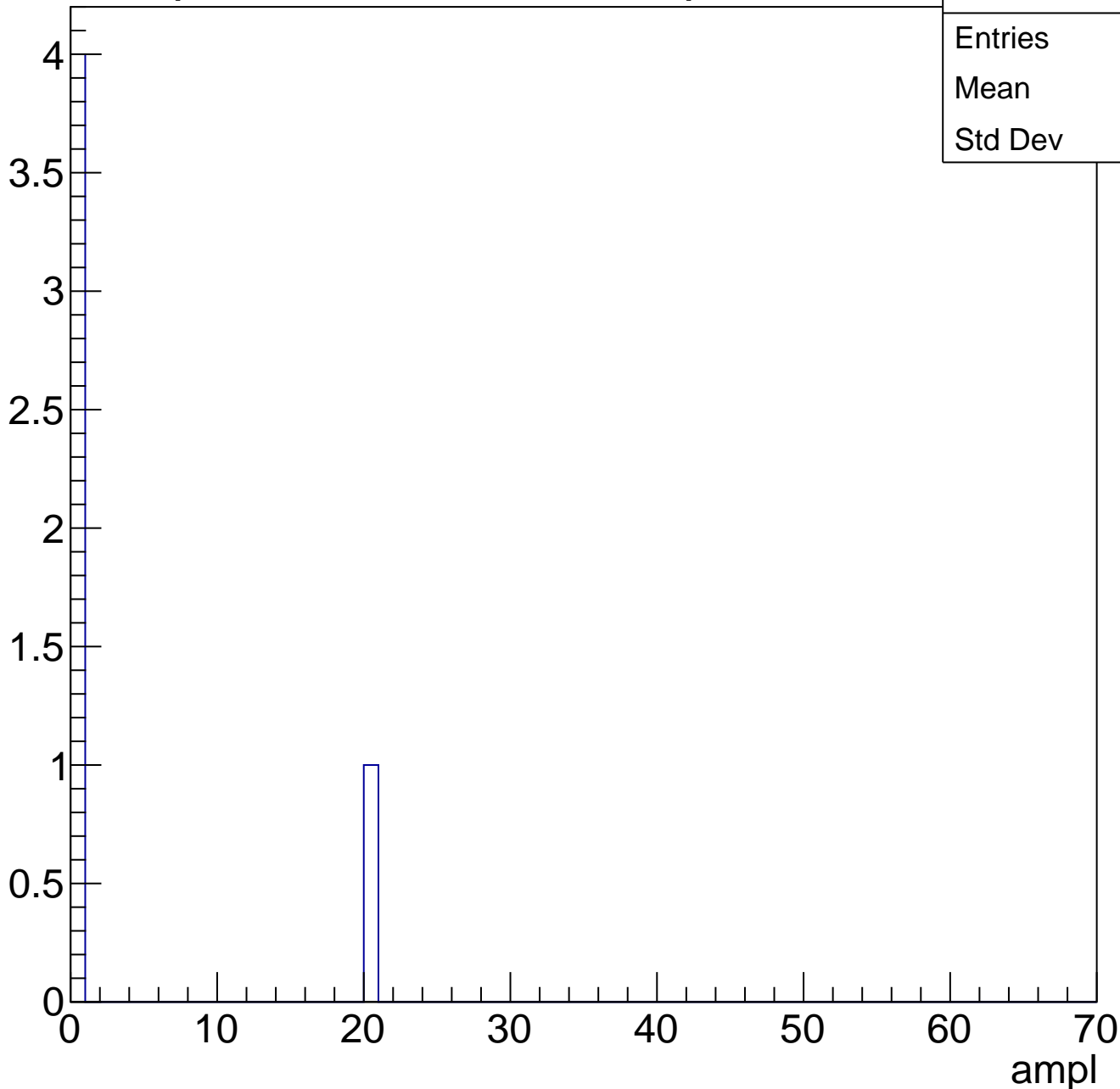




# B1L103S, U9-ch50, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	5
Mean	4
Std Dev	8

# B1L103S, U9-ch51, adc0

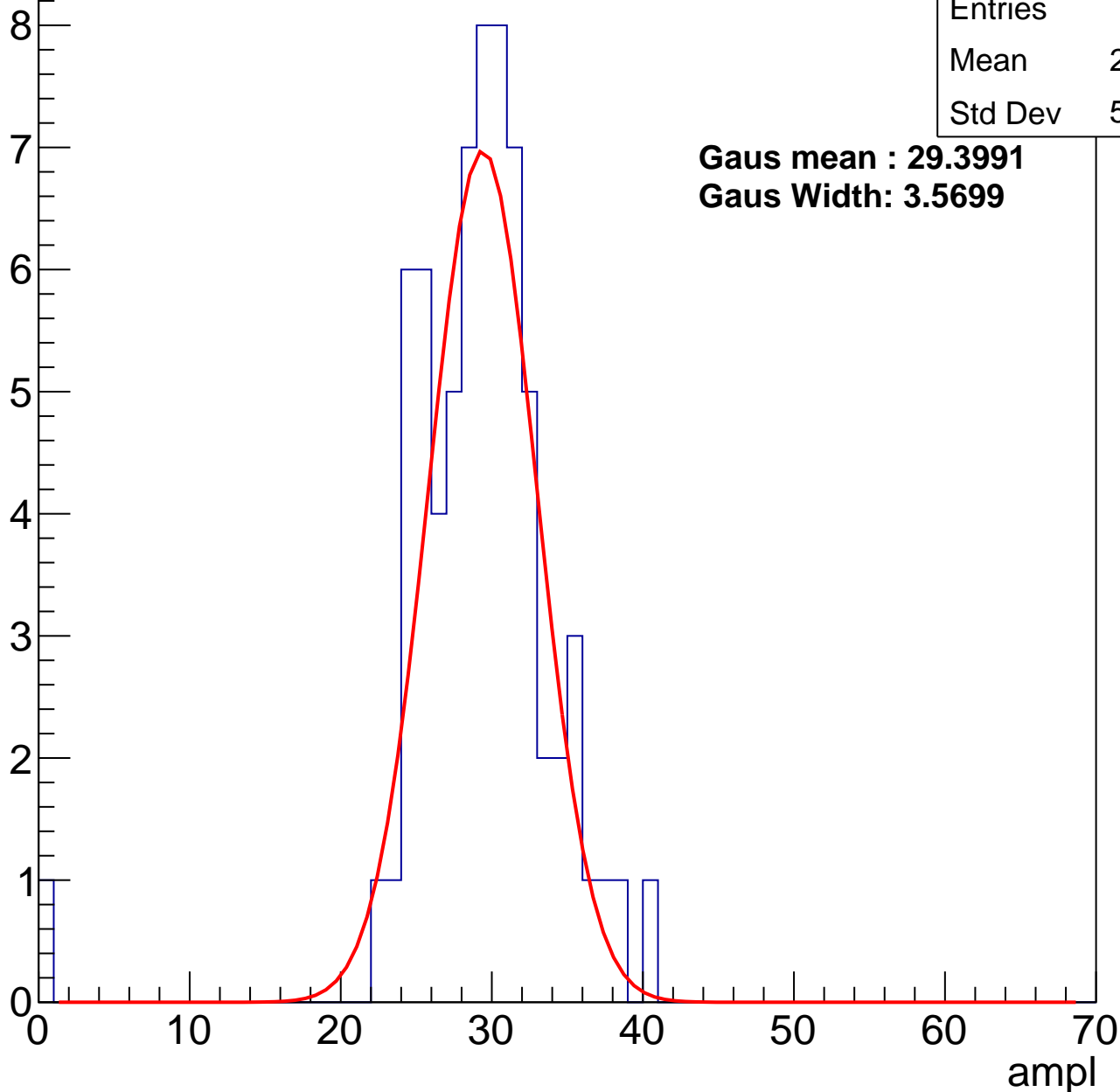
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	70
Mean	28.76
Std Dev	5.095

**Gaus mean : 29.3991**

**Gaus Width: 3.5699**



# B1L103S, U9-ch51, adc1

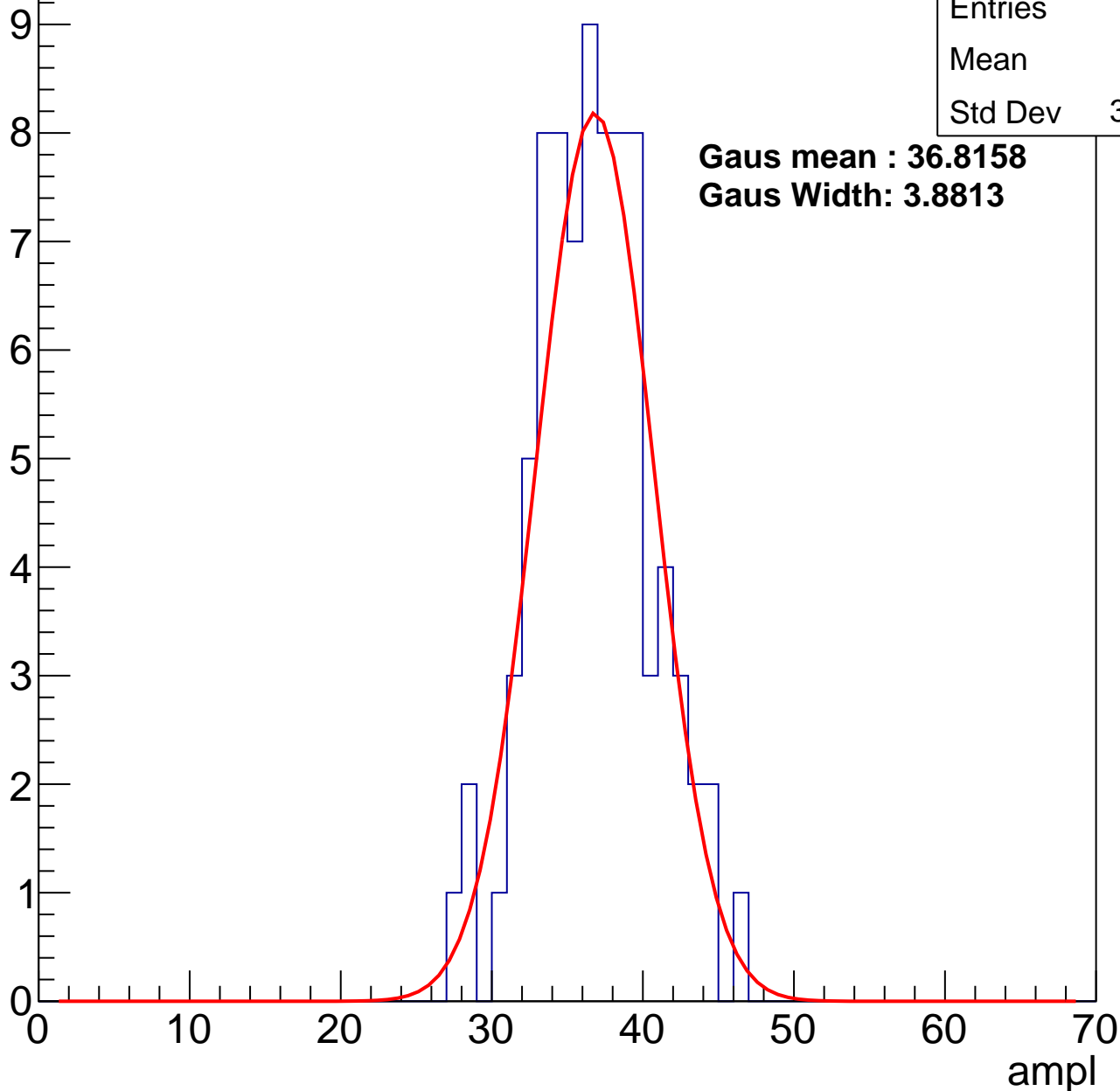
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	83
Mean	36.3
Std Dev	3.798

**Gaus mean : 36.8158**

**Gaus Width: 3.8813**

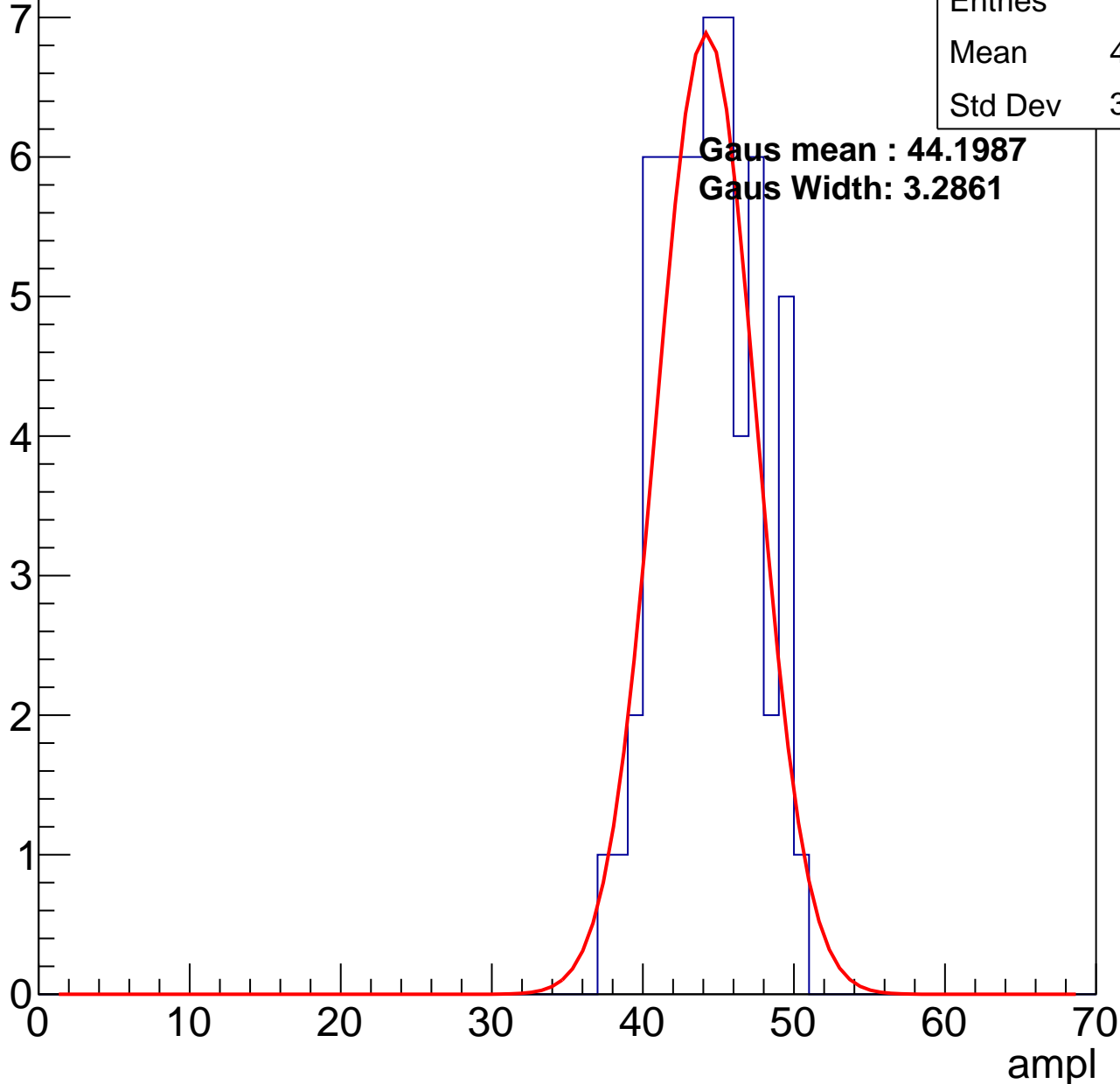


# B1L103S, U9-ch51, adc2

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	60
Mean	43.82
Std Dev	3.117

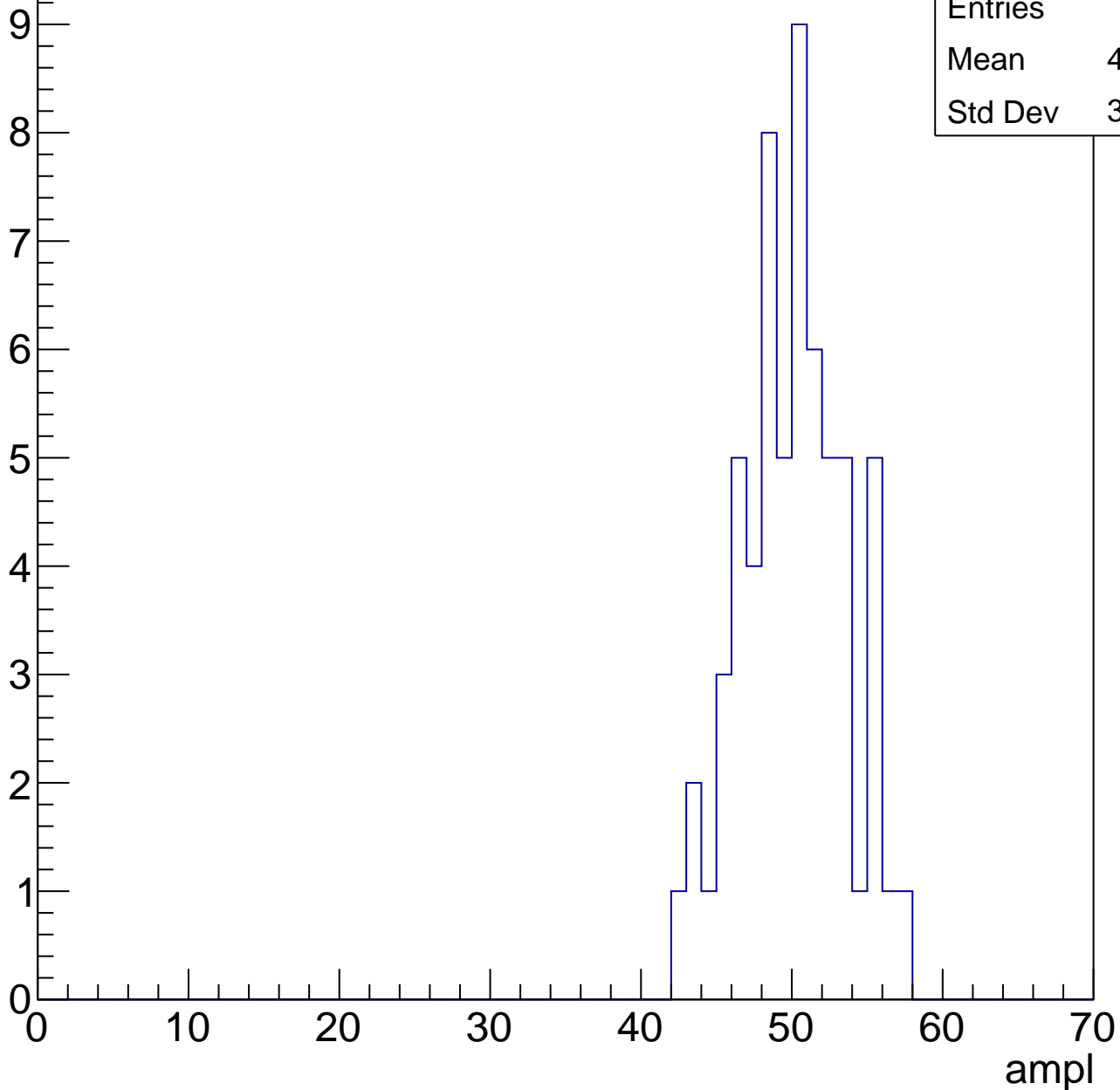


# B1L103S, U9-ch51, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	49.63
Std Dev	3.395



# B1L103S, U9-ch51, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

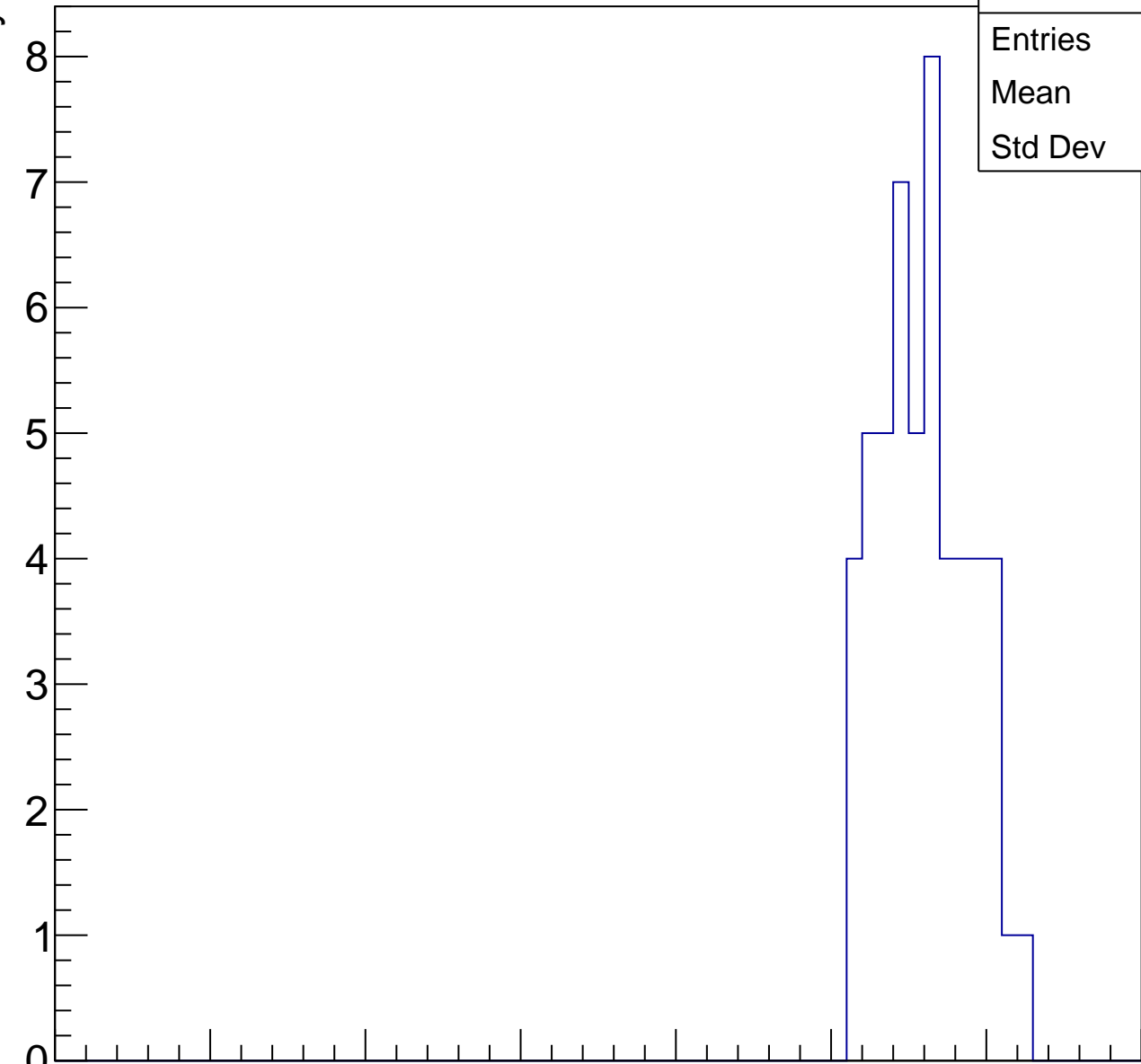
Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	52
Mean	55.56
Std Dev	2.872

ampl

0 10 20 30 40 50 60 70

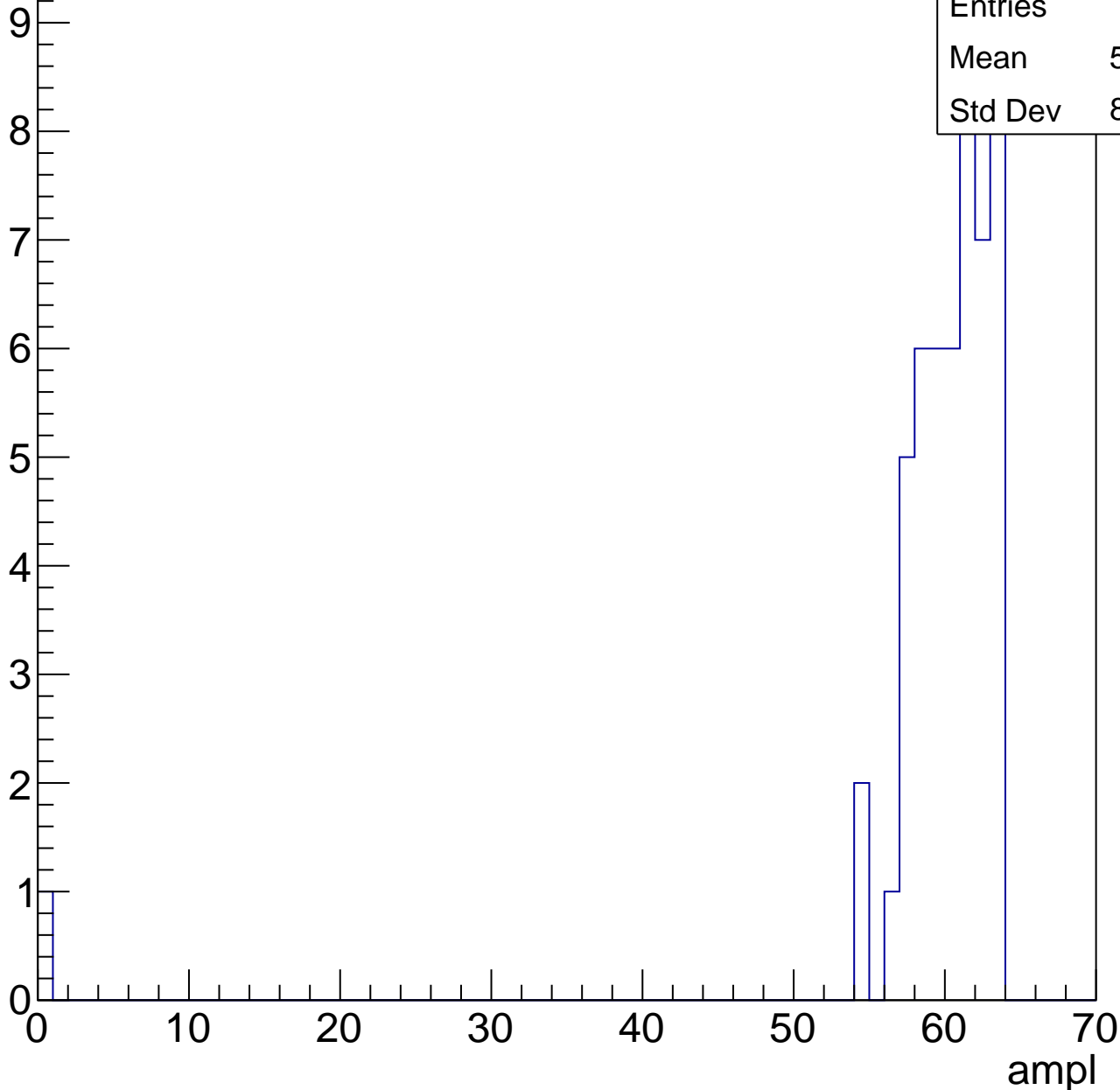


# B1L103S, U9-ch51, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	51
Mean	58.82
Std Dev	8.643



# B1L103S, U9-ch51, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	4
Mean	62
Std Dev	0.7071

ampl

0 10 20 30 40 50 60 70



# B1L103S, U9-ch51, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U9-ch52, adc0

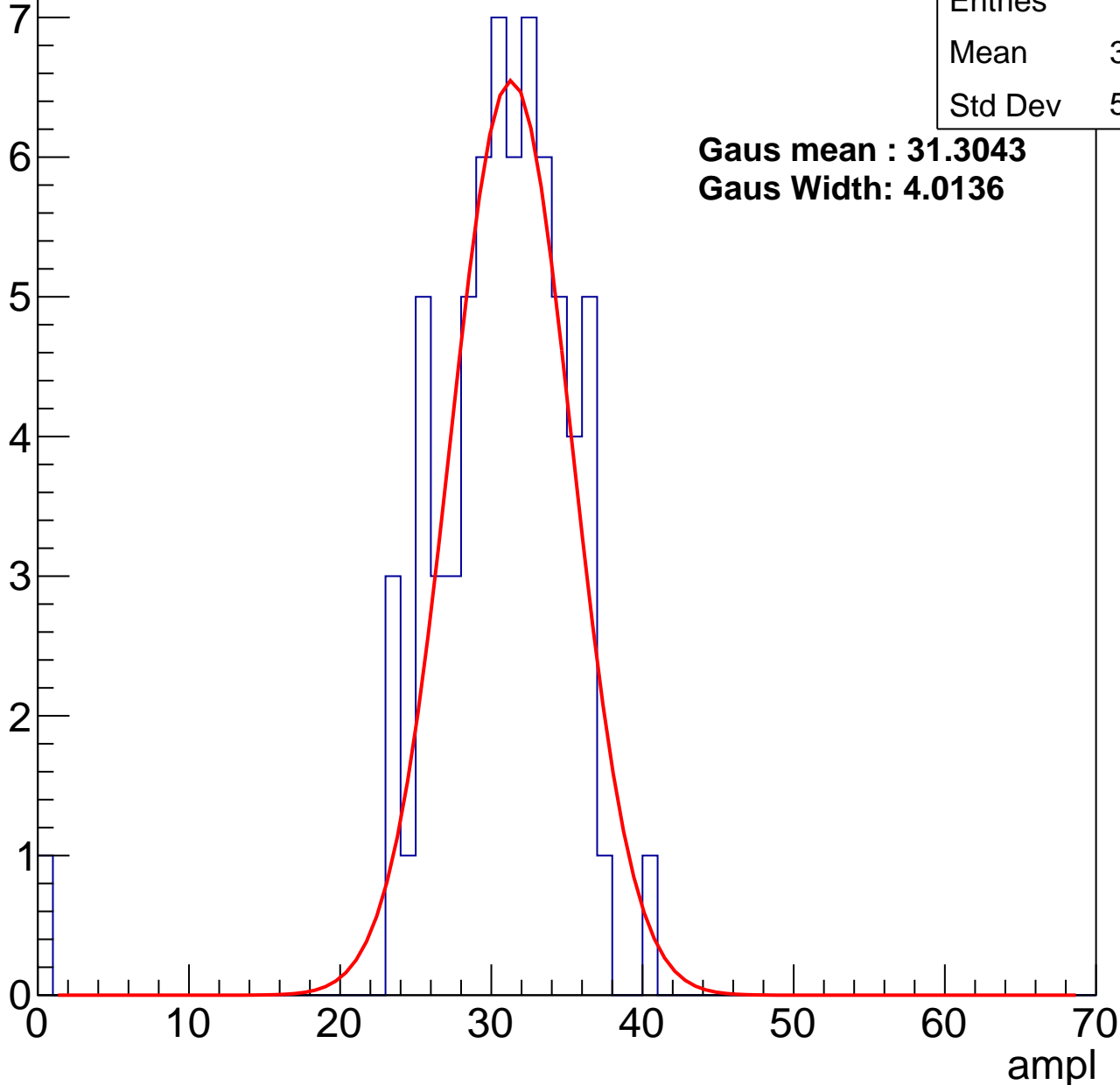
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	69
Mean	30.09
Std Dev	5.255

**Gaus mean : 31.3043**

**Gaus Width: 4.0136**



# B1L103S, U9-ch52, adc1

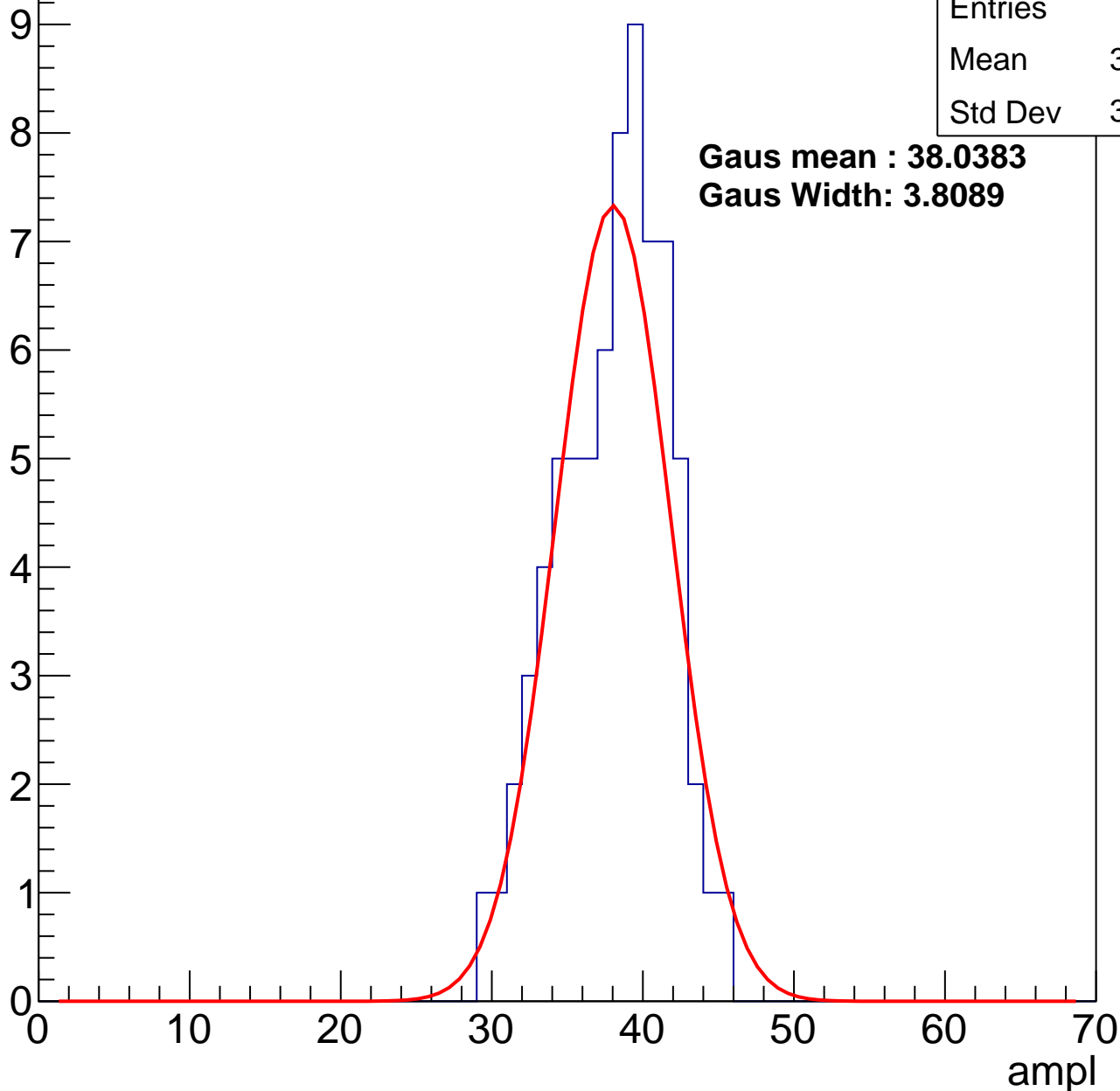
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	72
Mean	37.54
Std Dev	3.539

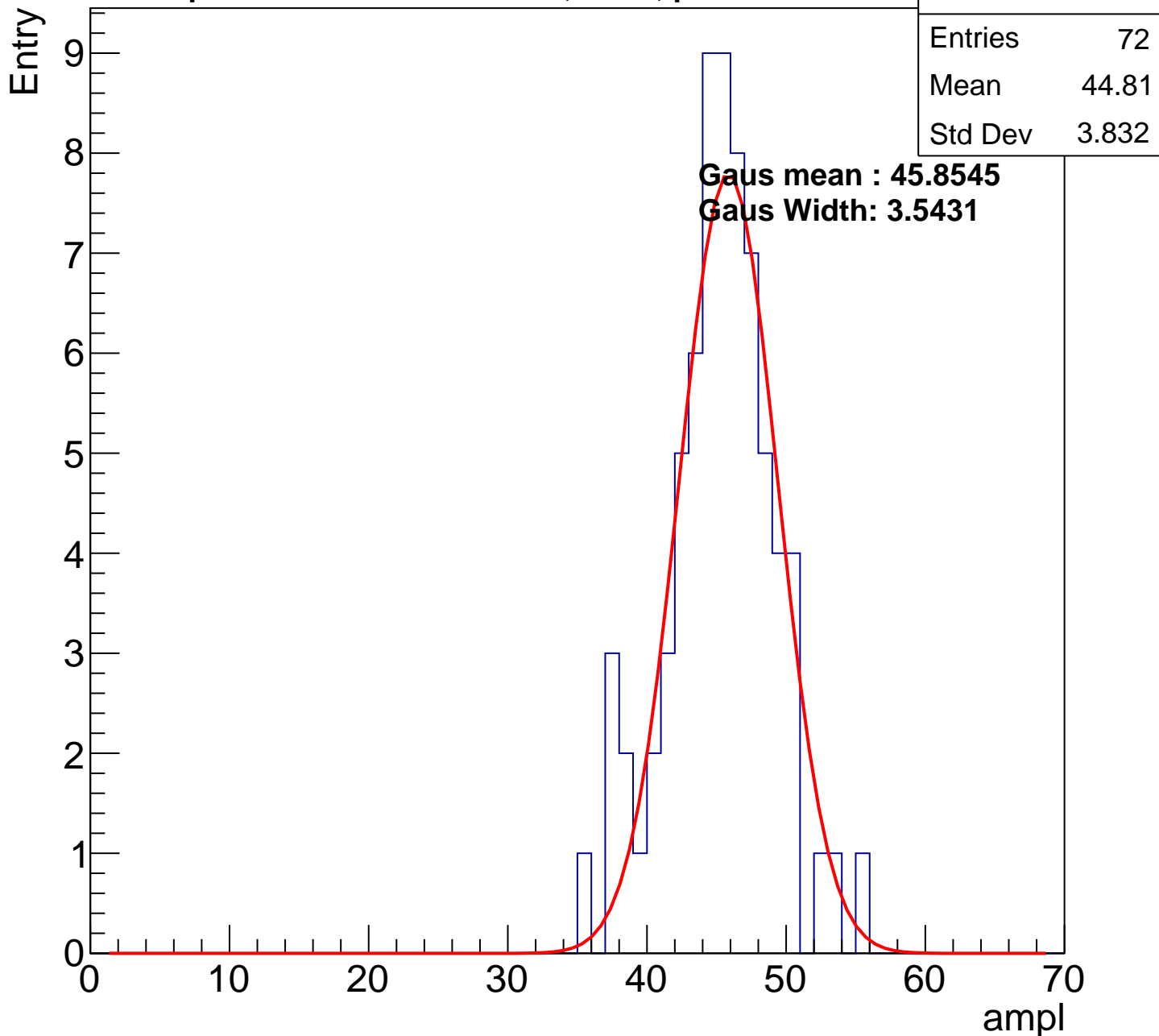
**Gaus mean : 38.0383**

**Gaus Width: 3.8089**



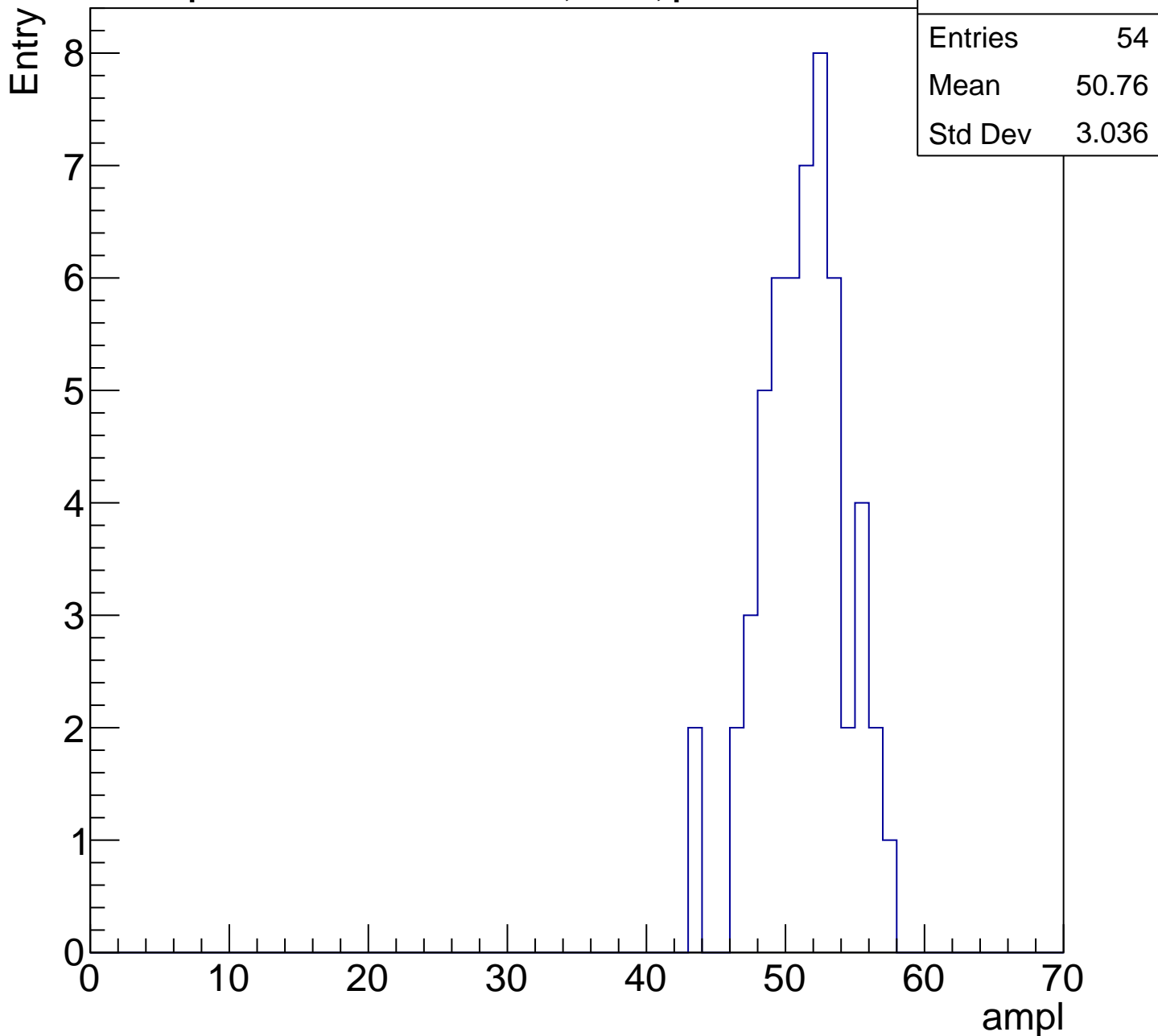
# B1L103S, U9-ch52, adc2

calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U9-ch52, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

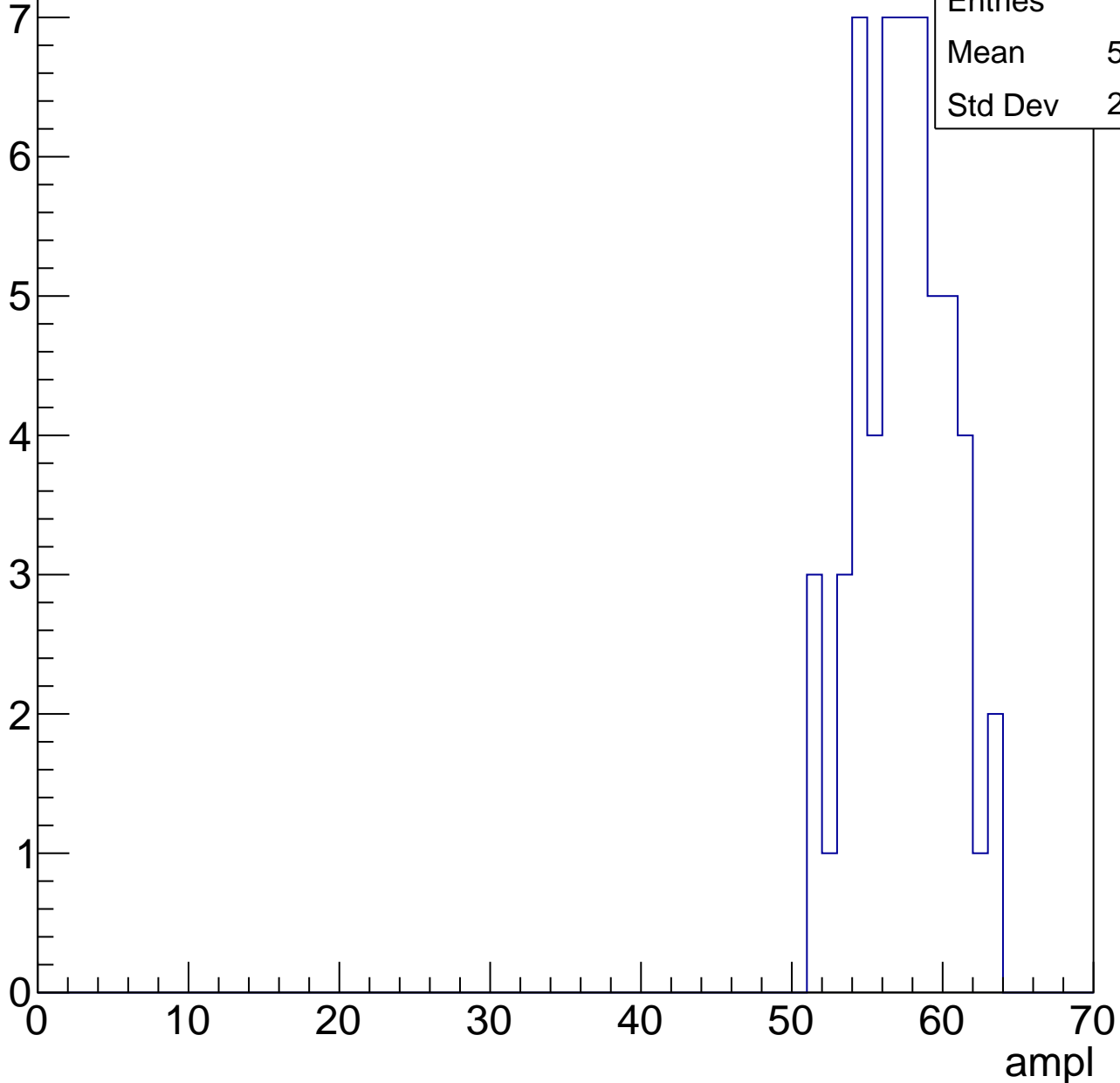


# B1L103S, U9-ch52, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

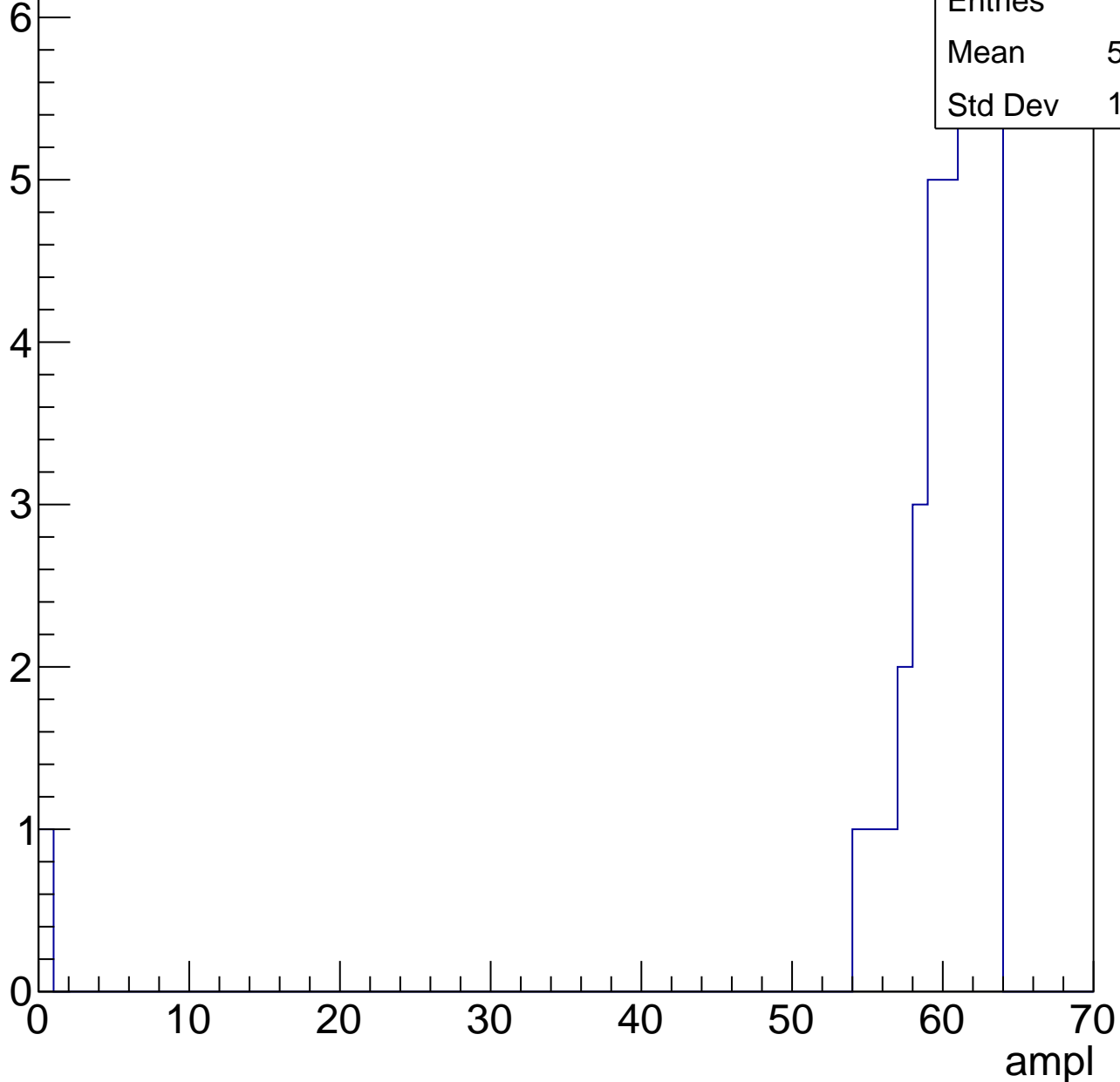
Entries	56
Mean	56.89
Std Dev	2.986



# B1L103S, U9-ch52, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U9-ch52, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U9-ch52, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U9-ch53, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	85
Mean	32.16
Std Dev	3.952

**Gaus mean : 32.4913**

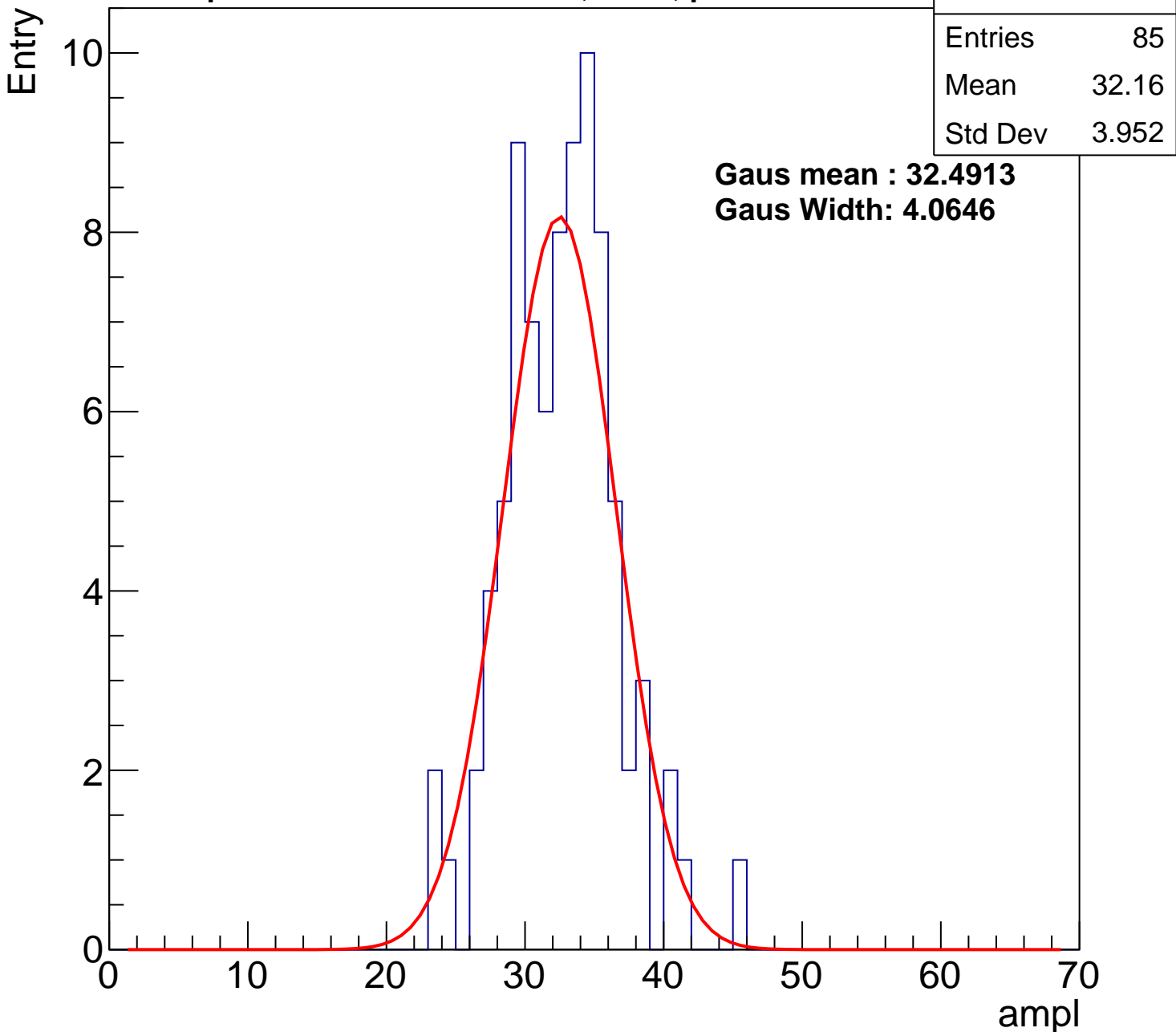
**Gaus Width: 4.0646**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U9-ch53, adc1

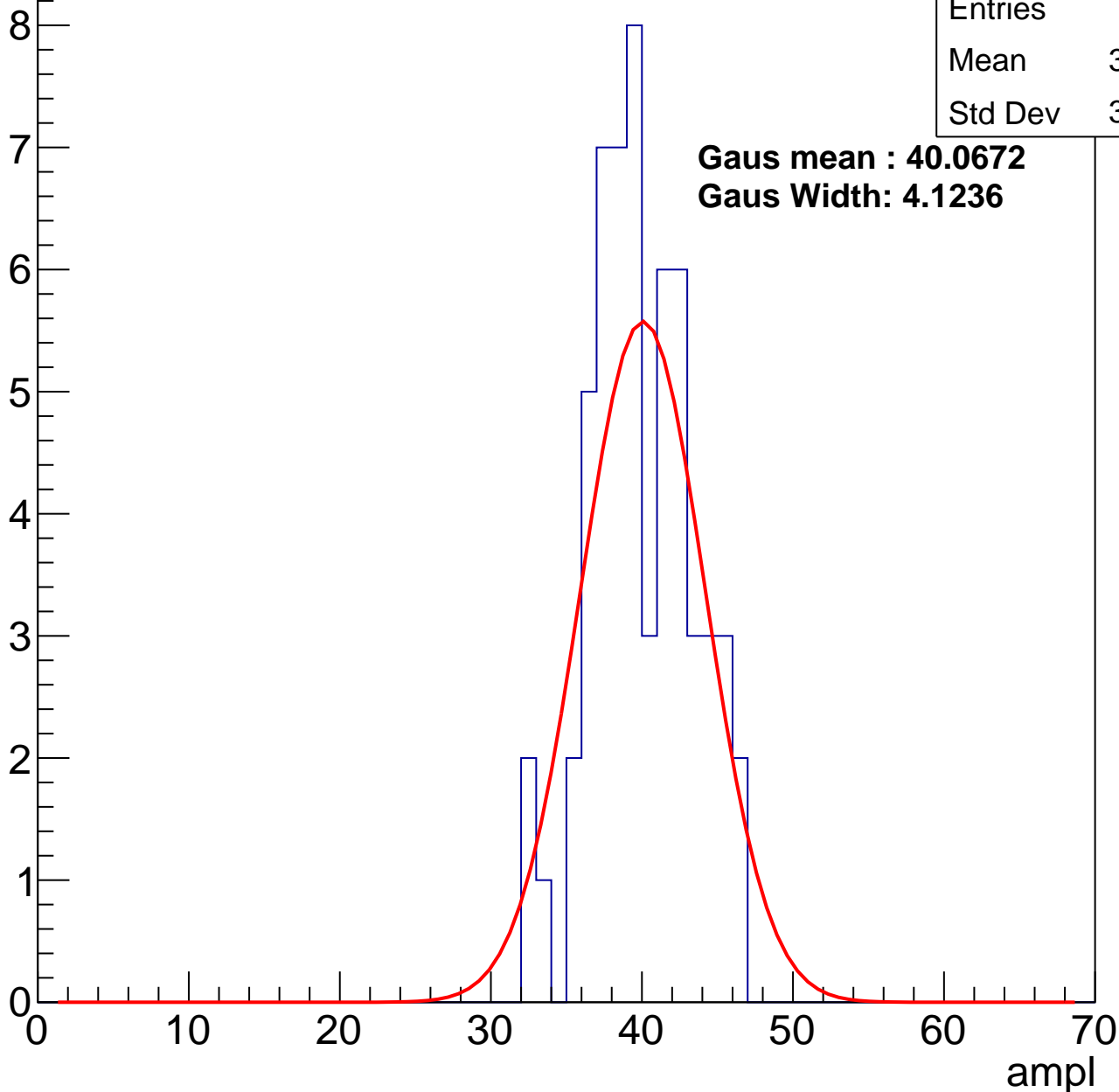
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	58
Mean	39.48
Std Dev	3.328

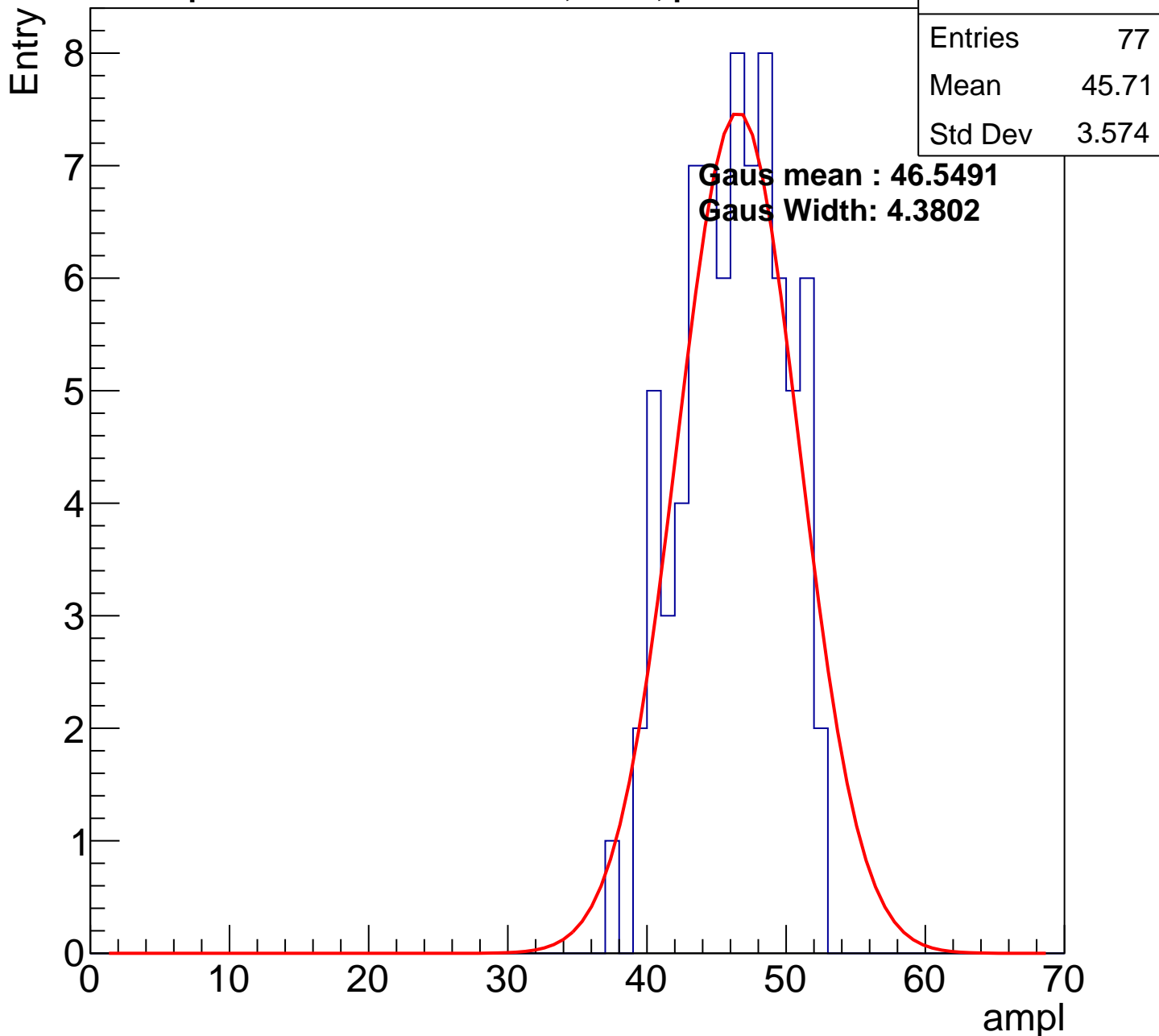
**Gaus mean : 40.0672**

**Gaus Width: 4.1236**



# B1L103S, U9-ch53, adc2

calib\_packv5\_042523\_0143.root, FC#7, port C2

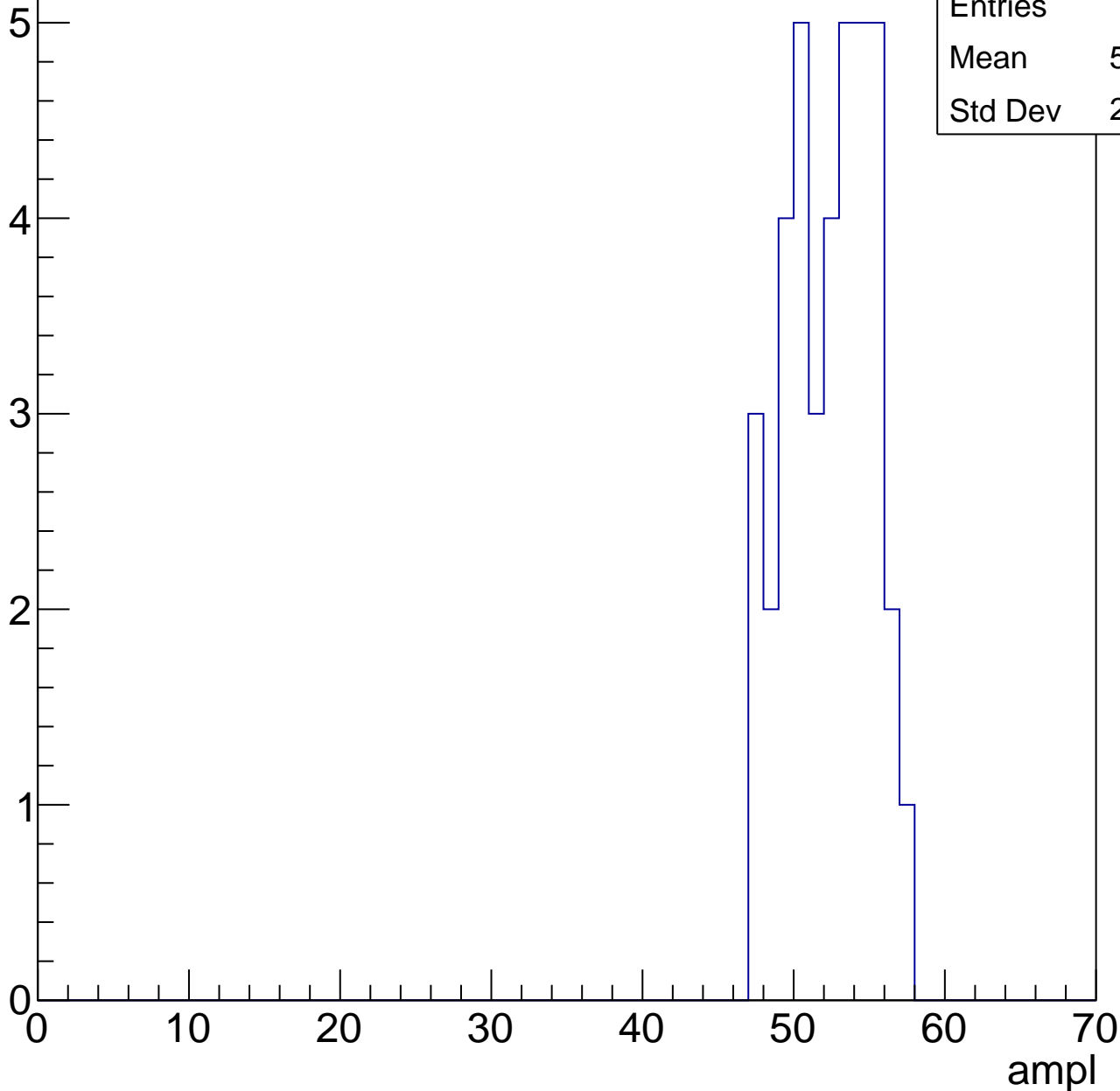


# B1L103S, U9-ch53, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	39
Mean	51.87
Std Dev	2.738

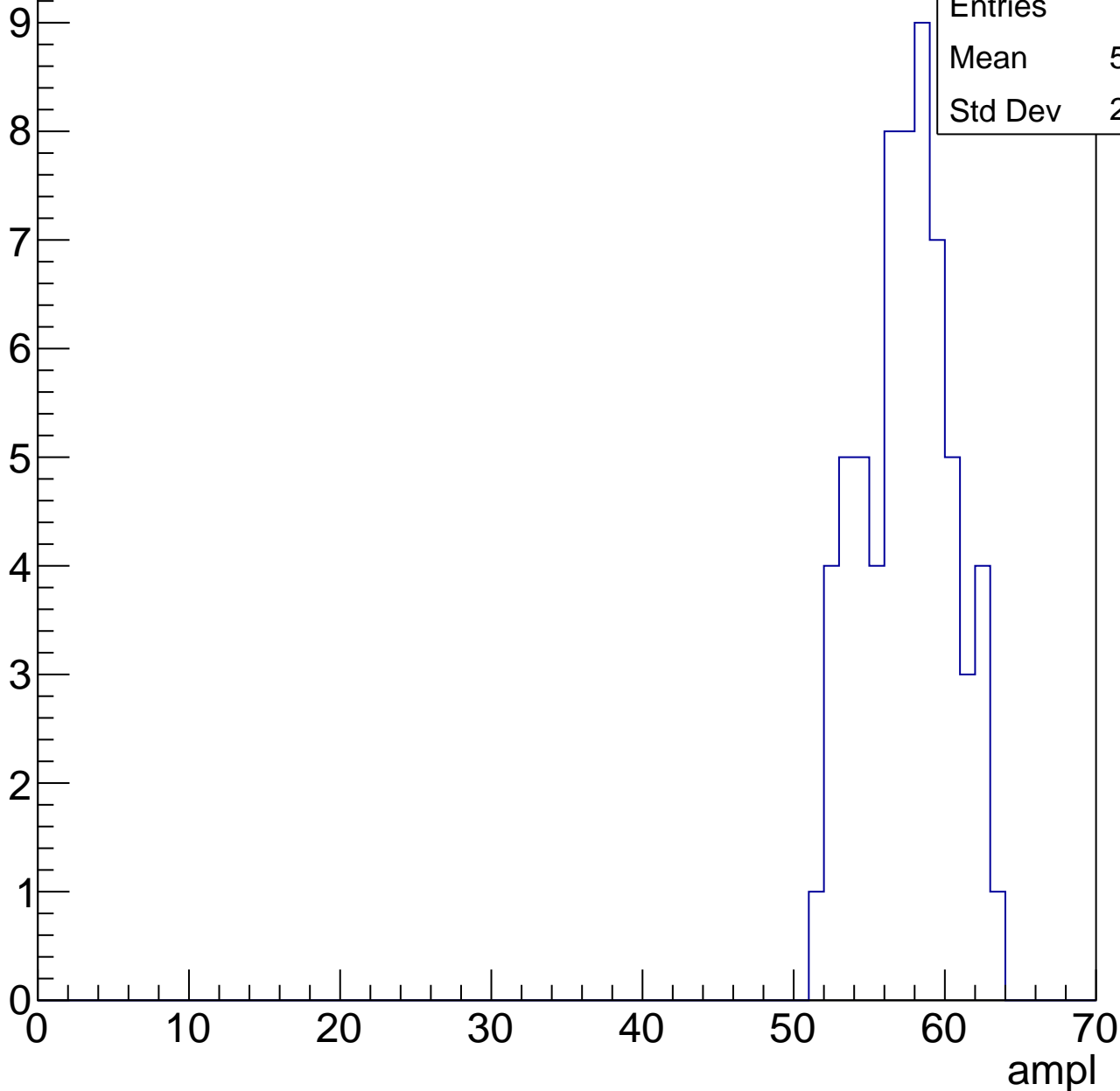


# B1L103S, U9-ch53, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	56.98
Std Dev	2.934

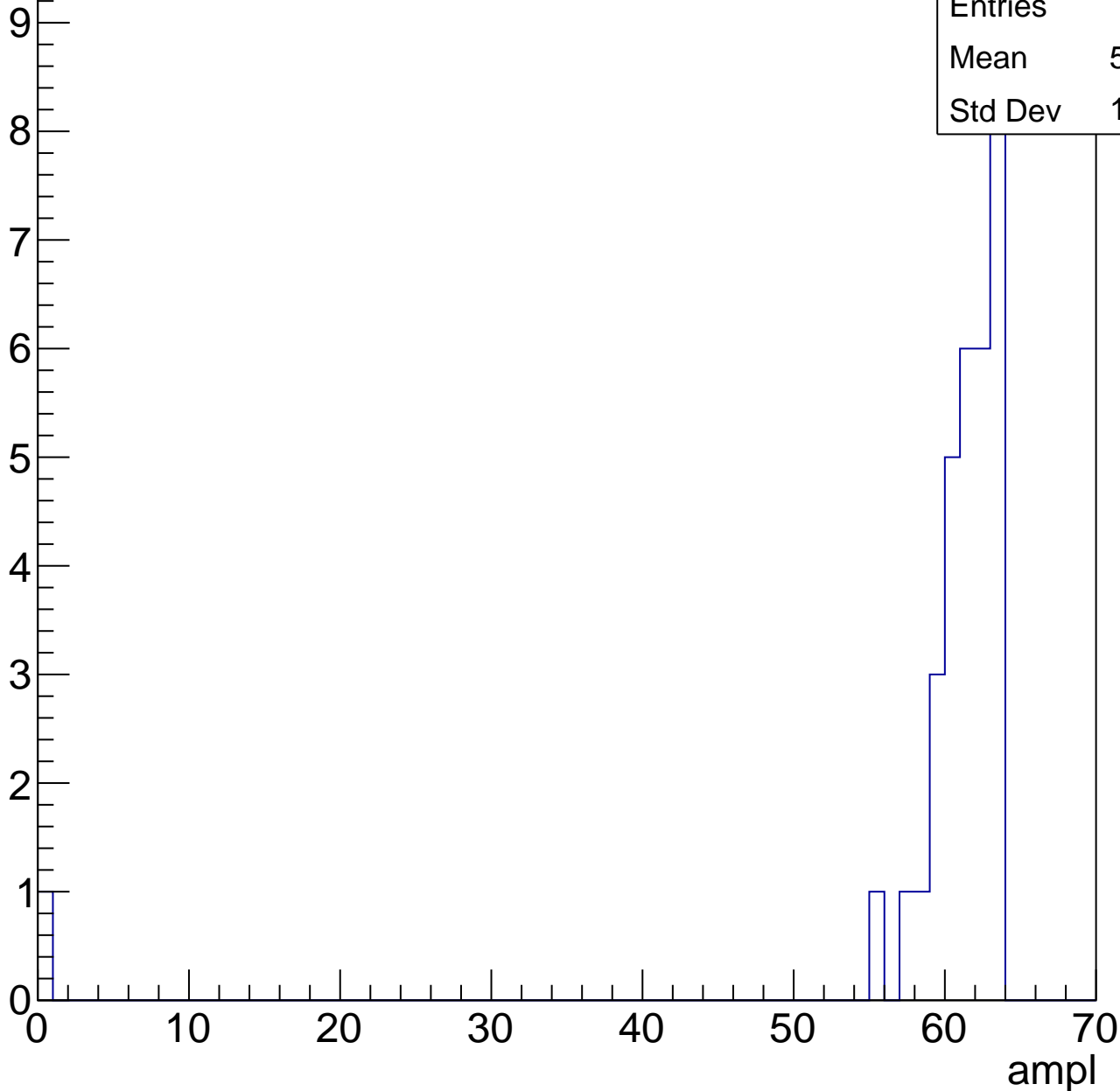


# B1L103S, U9-ch53, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	33
Mean	59.15
Std Dev	10.63



# B1L103S, U9-ch53, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	61
Std Dev	0



# B1L103S, U9-ch53, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L103S, U9-ch54, adc0

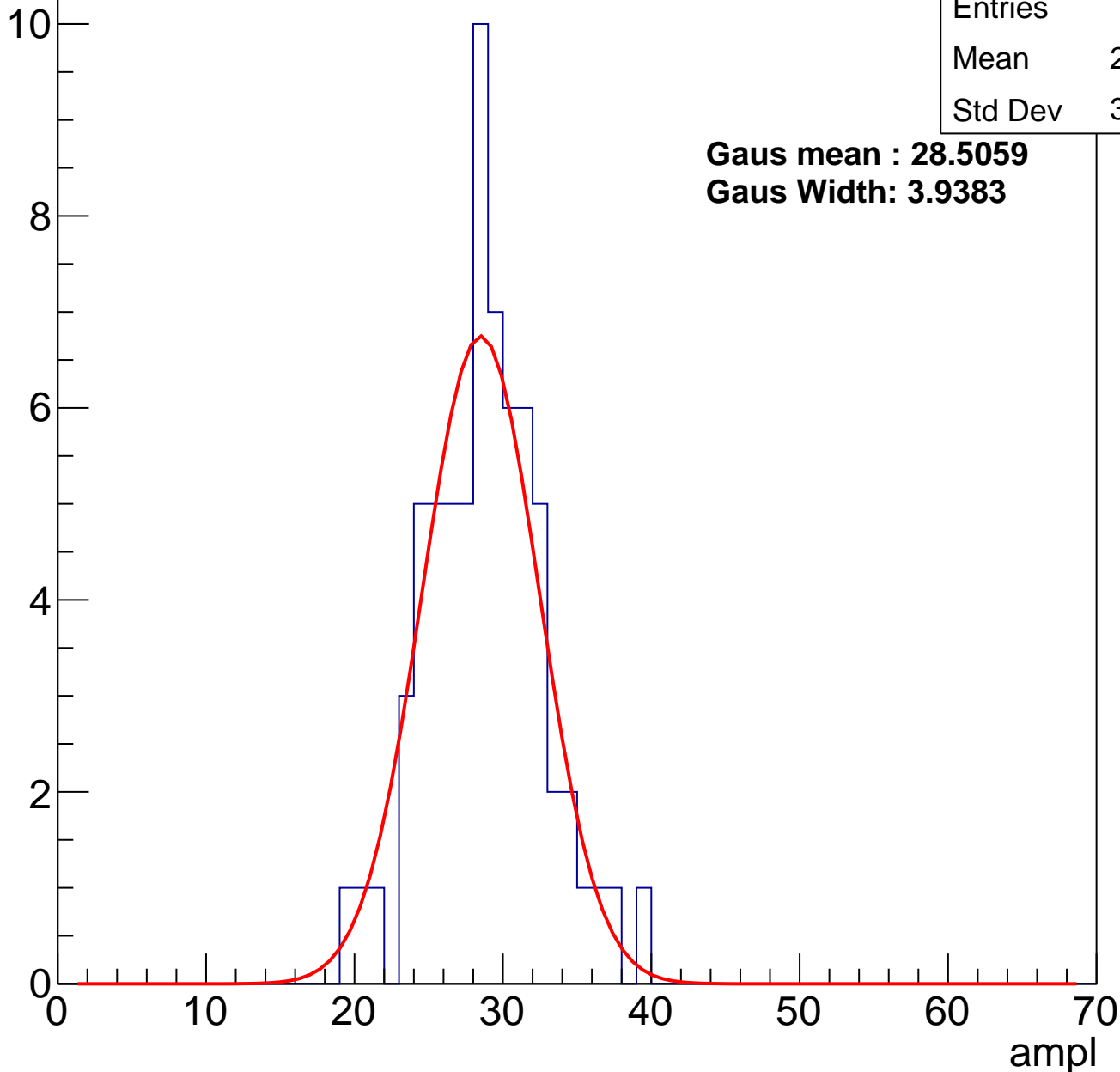
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	68
Mean	28.37
Std Dev	3.857

**Gaus mean : 28.5059**

**Gaus Width: 3.9383**

Entry



# B1L103S, U9-ch54, adc1

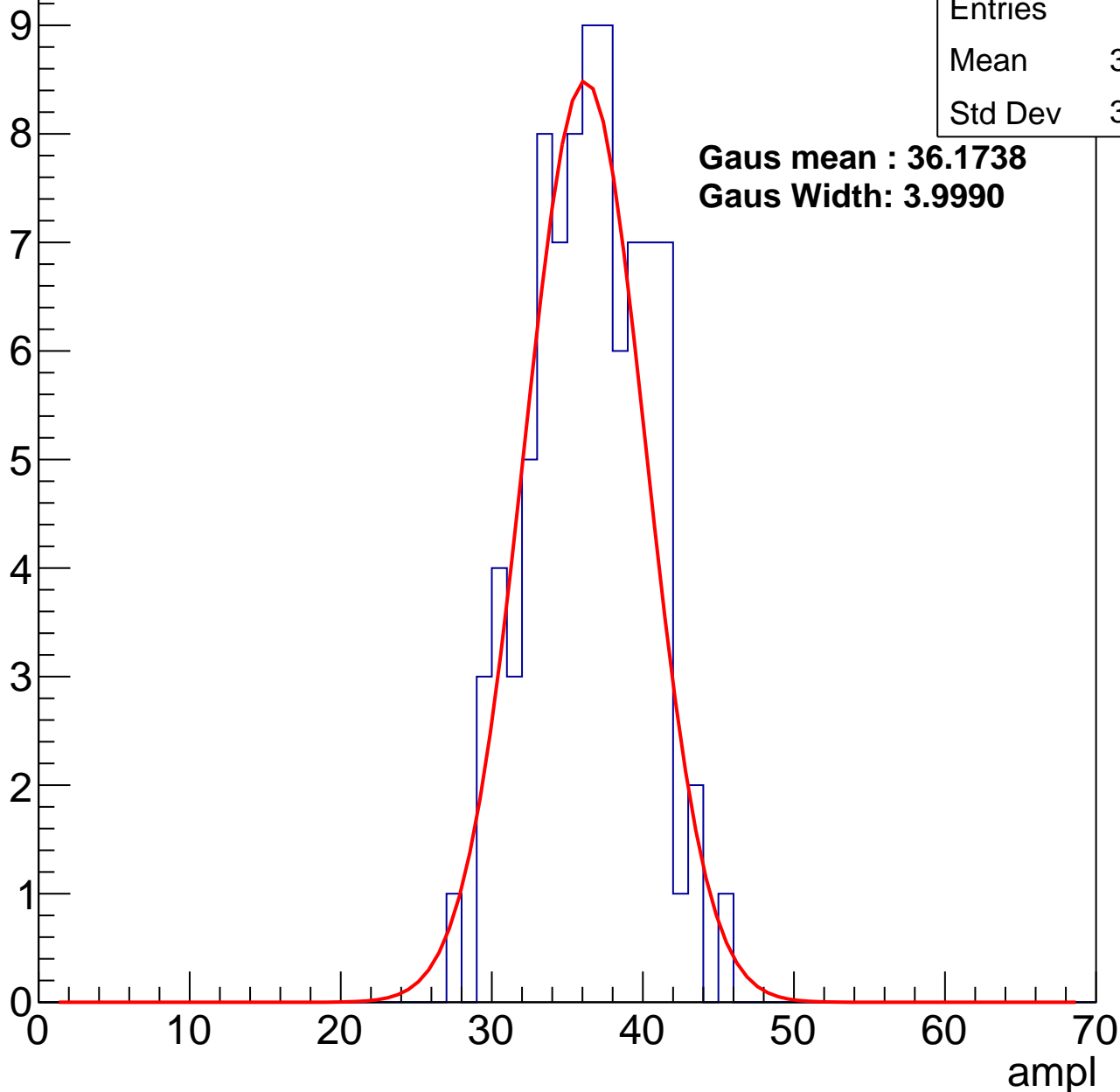
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	88
Mean	35.99
Std Dev	3.743

**Gaus mean : 36.1738**

**Gaus Width: 3.9990**



# B1L103S, U9-ch54, adc2

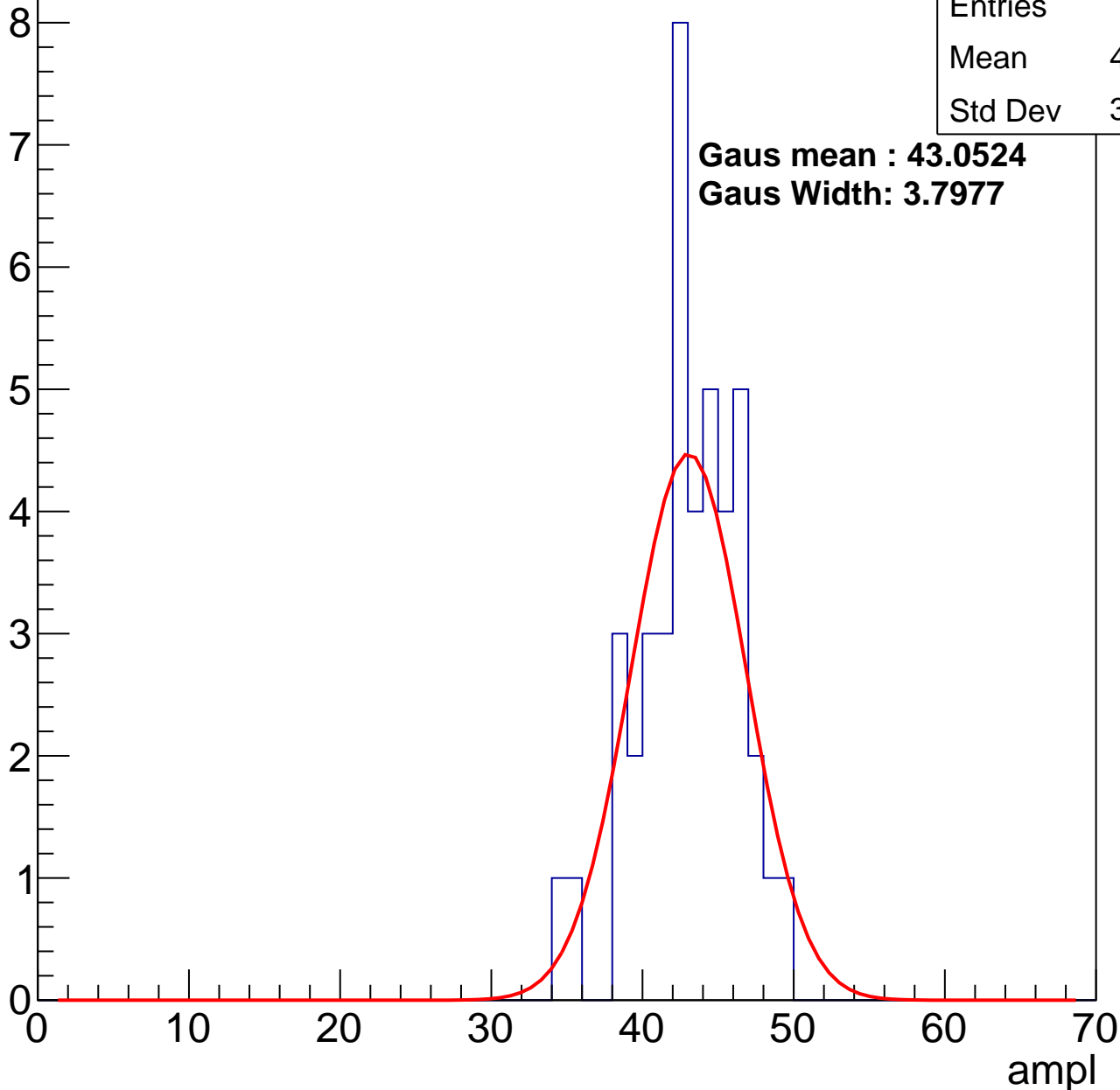
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	43
Mean	42.63
Std Dev	3.242

**Gaus mean : 43.0524**

**Gaus Width: 3.7977**

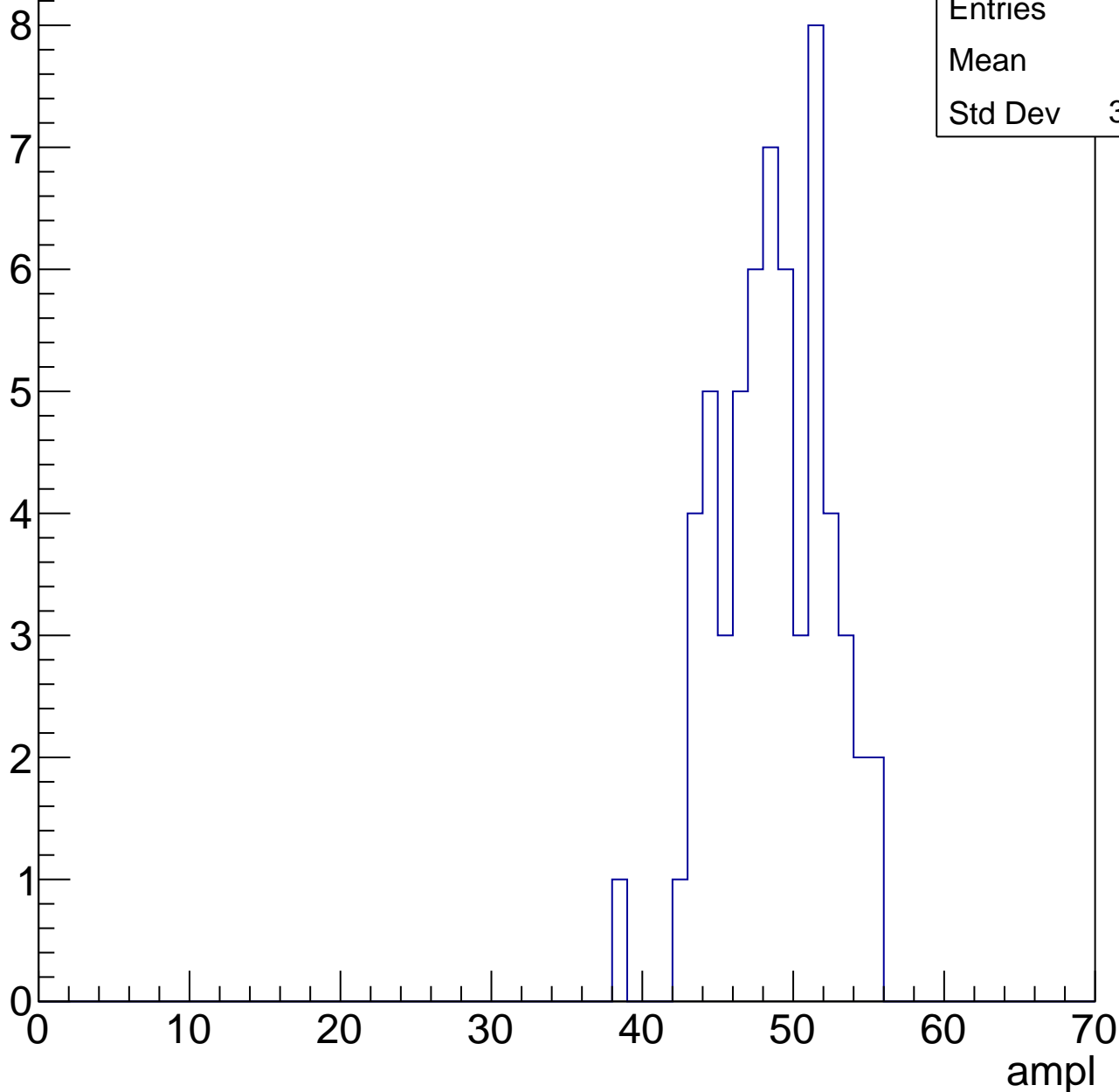


# B1L103S, U9-ch54, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

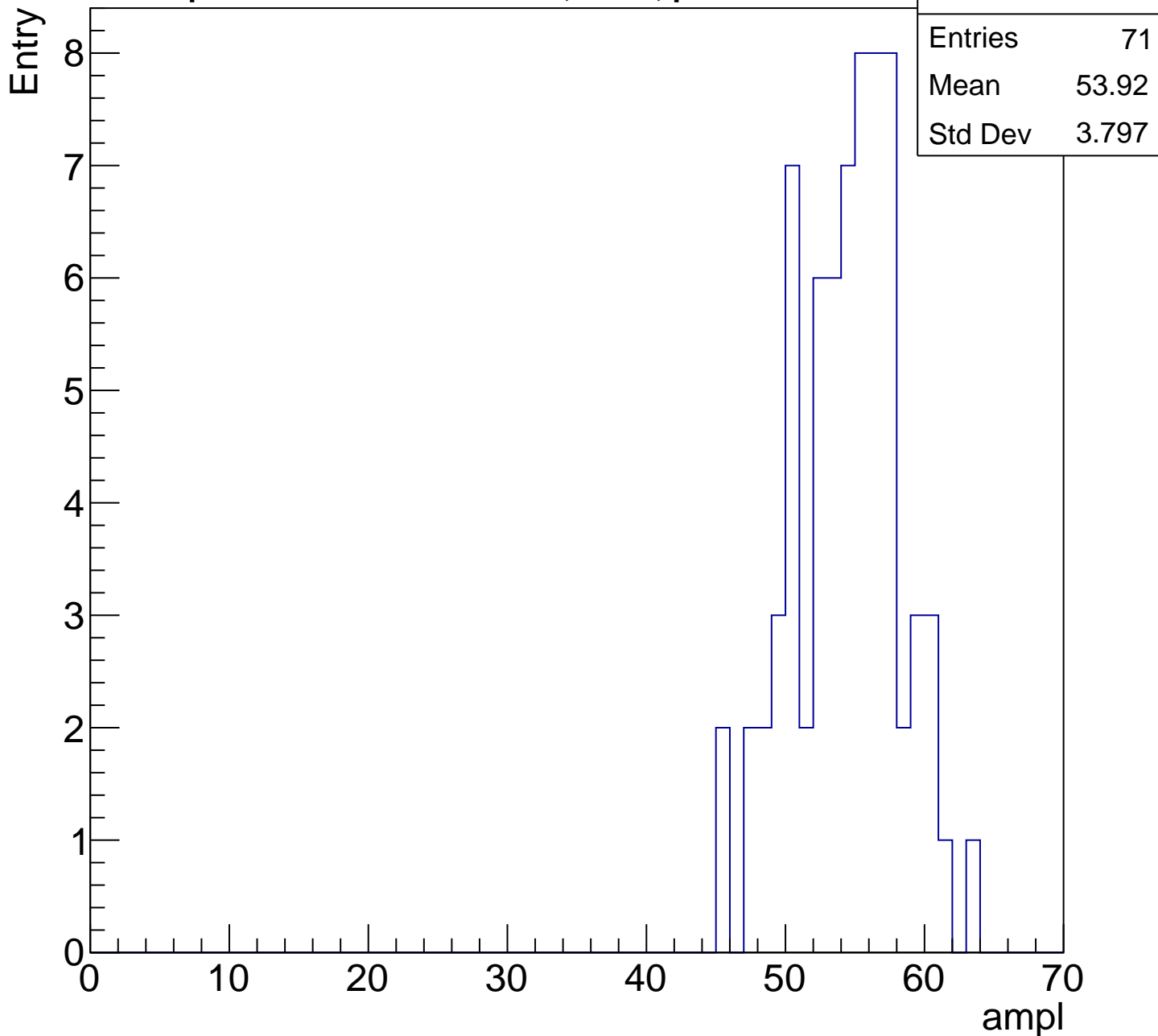
Entry

Entries	60
Mean	48.2
Std Dev	3.572



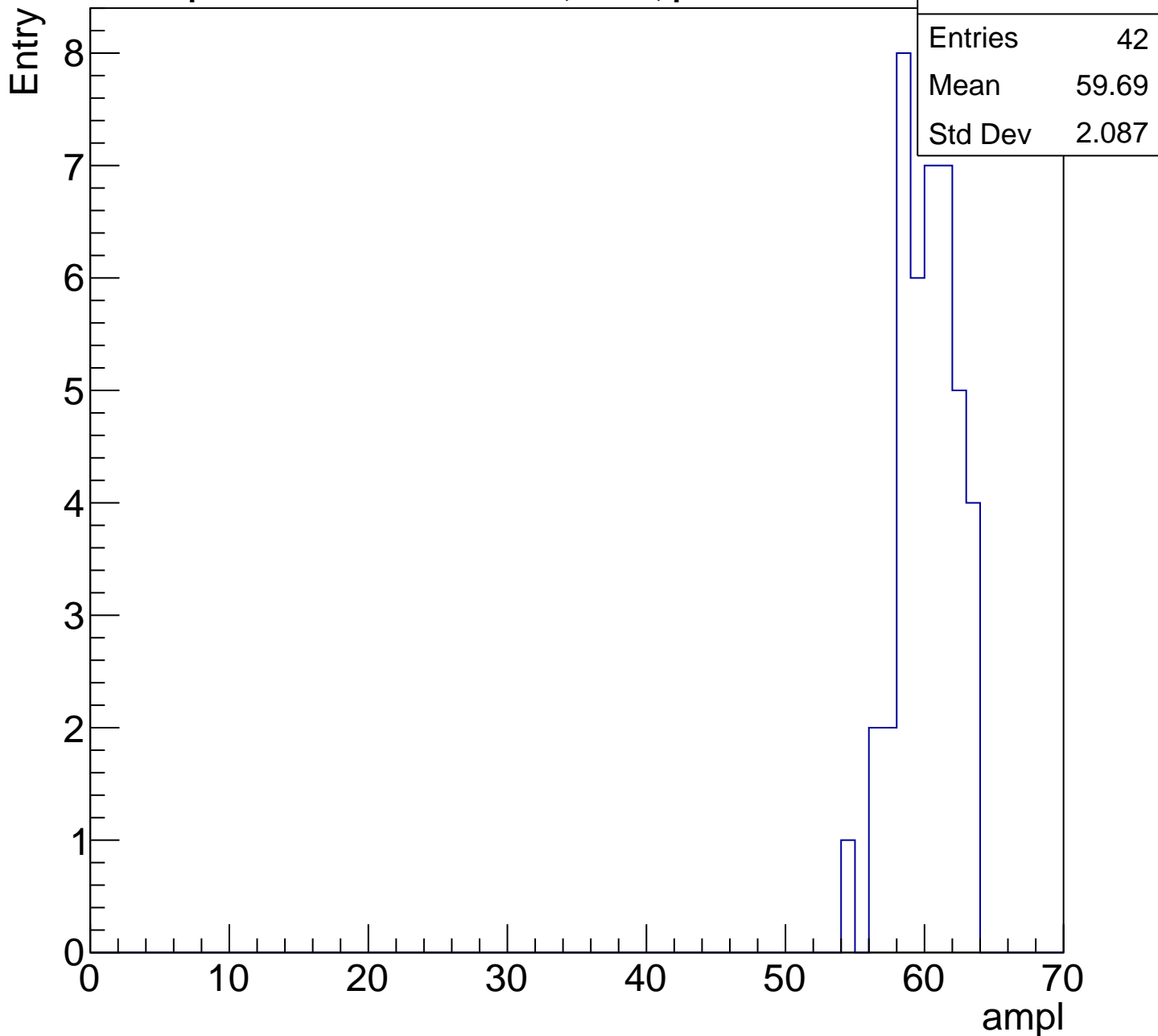
# B1L103S, U9-ch54, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U9-ch54, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

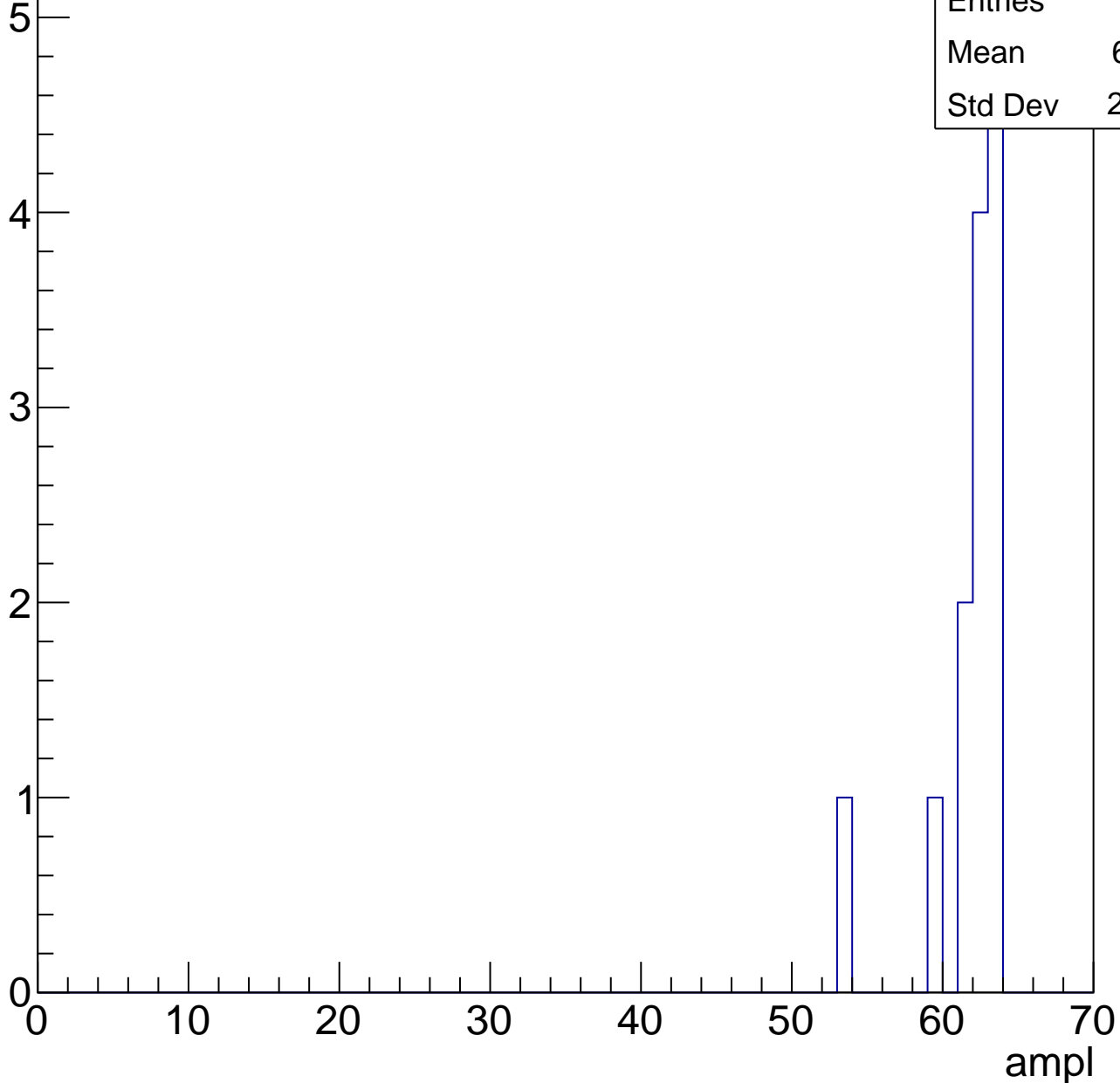


# B1L103S, U9-ch54, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	13
Mean	61.31
Std Dev	2.642





# B1L103S, U9-ch54, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U9-ch55, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	80
Mean	29.16
Std Dev	4.963

**Gaus mean : 30.0248**

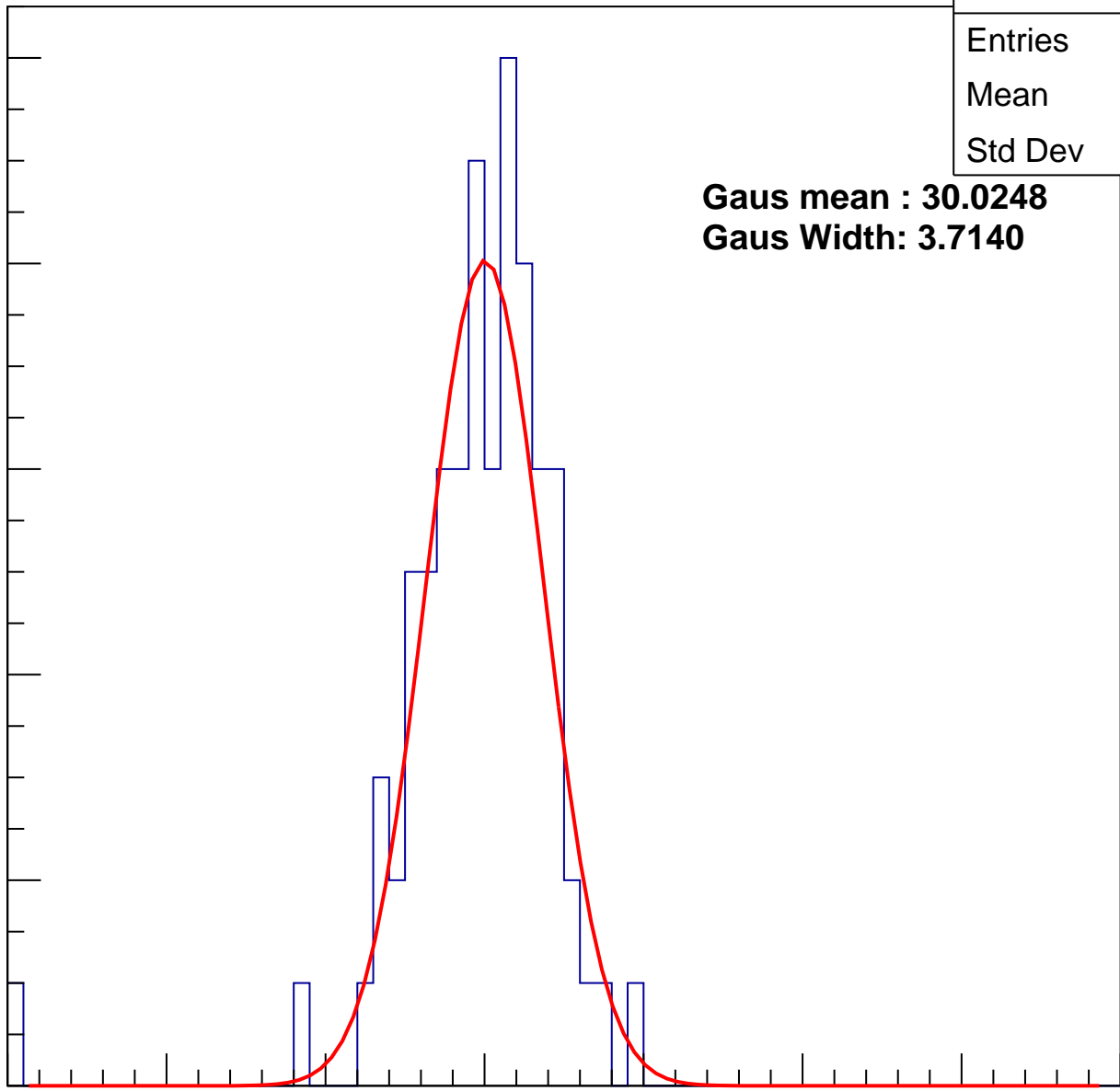
**Gaus Width: 3.7140**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U9-ch55, adc1

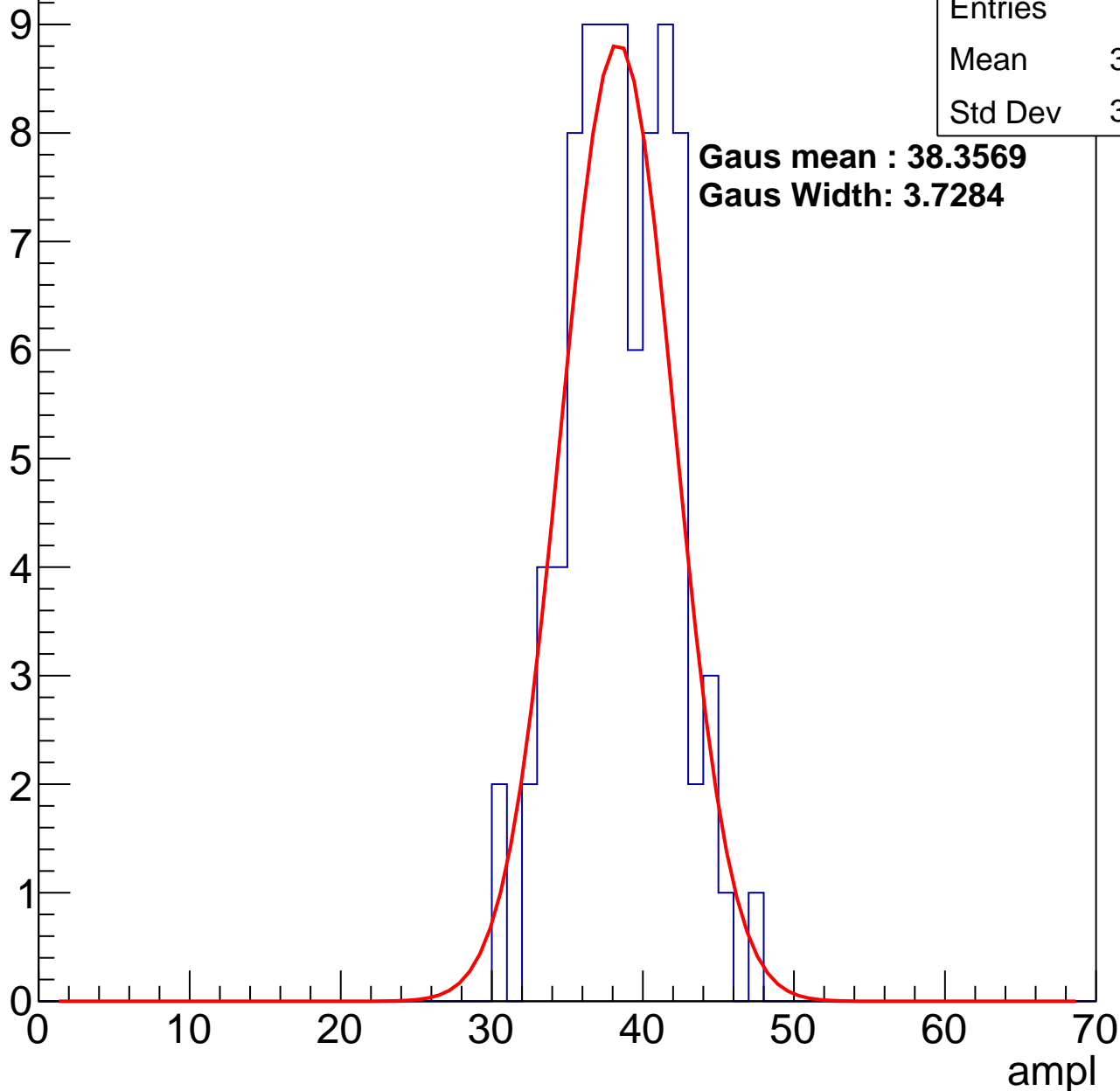
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	85
Mean	38.12
Std Dev	3.455

**Gaus mean : 38.3569**

**Gaus Width: 3.7284**



# B1L103S, U9-ch55, adc2

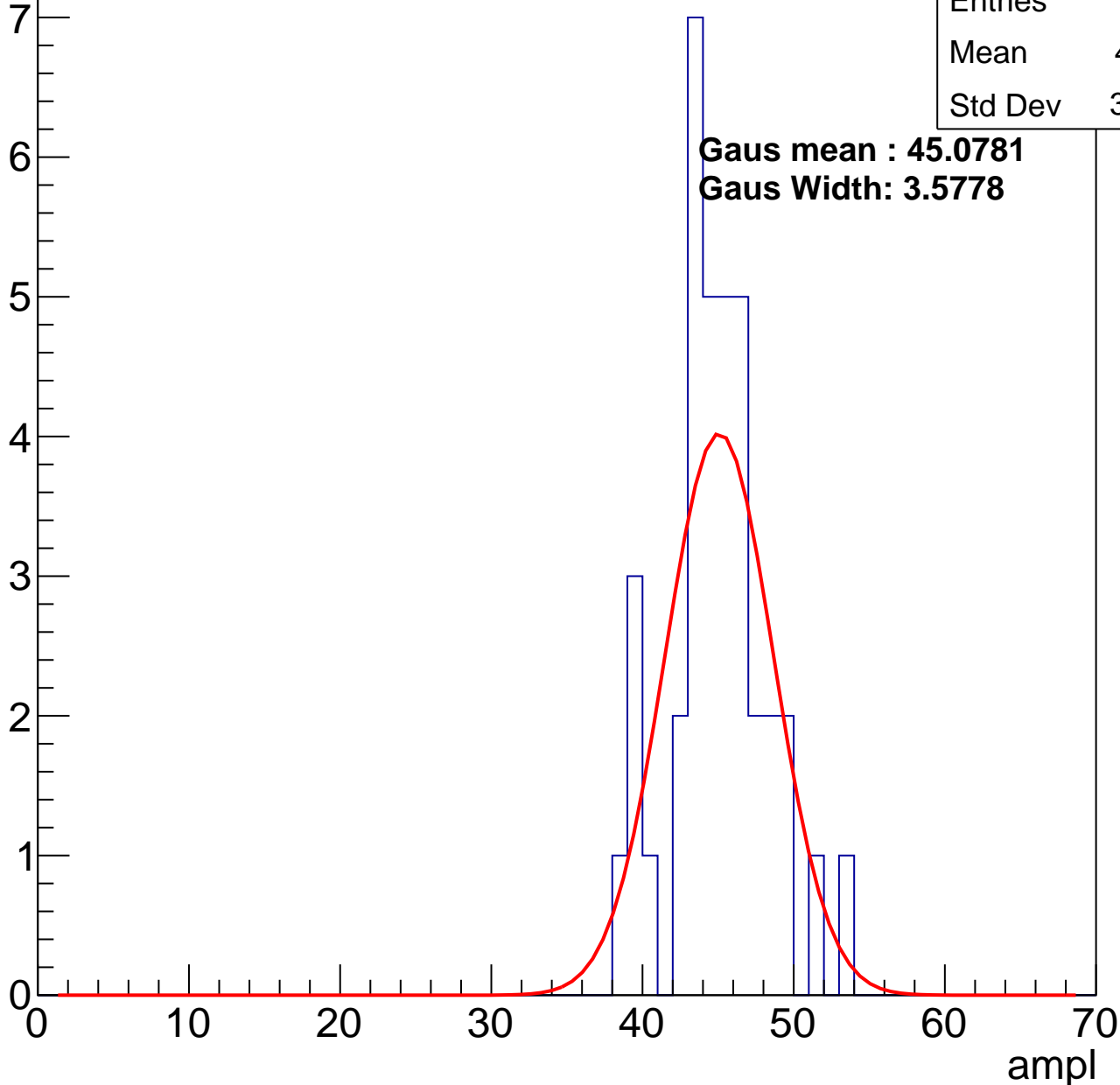
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	37
Mean	44.51
Std Dev	3.235

**Gaus mean : 45.0781**

**Gaus Width: 3.5778**

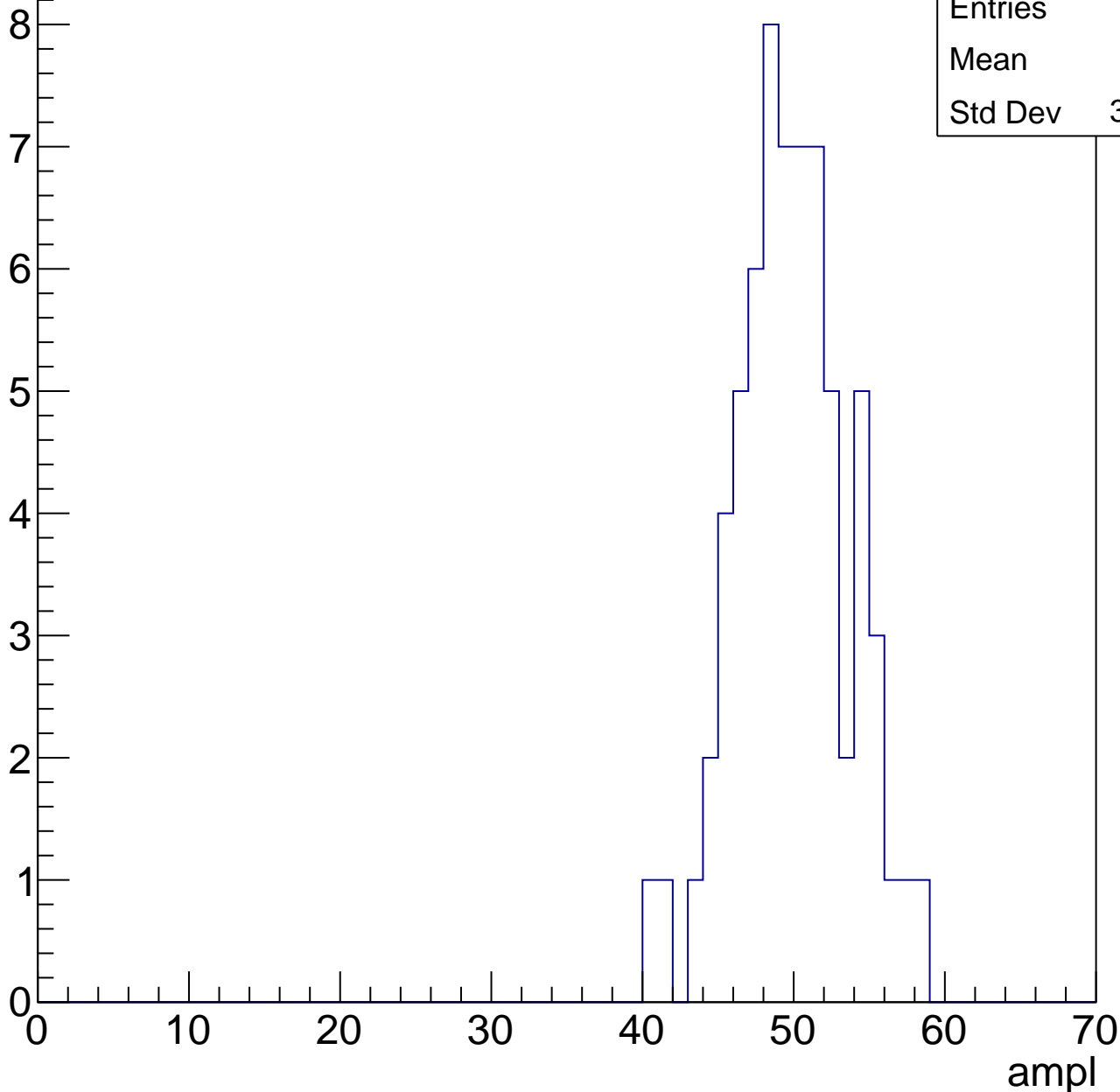


# B1L103S, U9-ch55, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

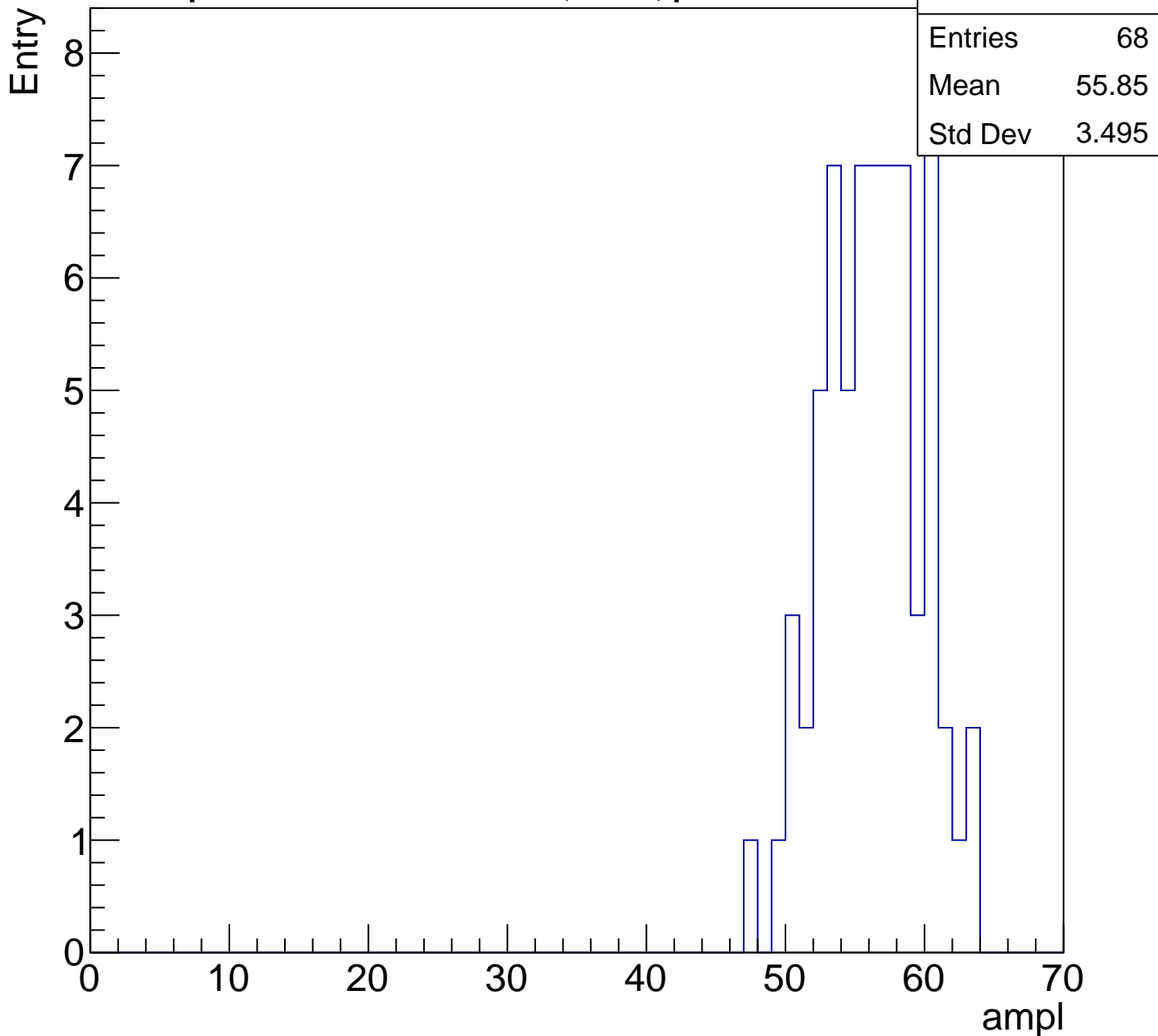
Entry

Entries	67
Mean	49.4
Std Dev	3.665



# B1L103S, U9-ch55, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U9-ch55, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	41
Mean	59.15
Std Dev	9.565

ampl

0 10 20 30 40 50 60 70

0

1

2

3

4

5

6

7

8

9

# B1L103S, U9-ch55, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0



# B1L103S, U9-ch55, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U9-ch56, adc0

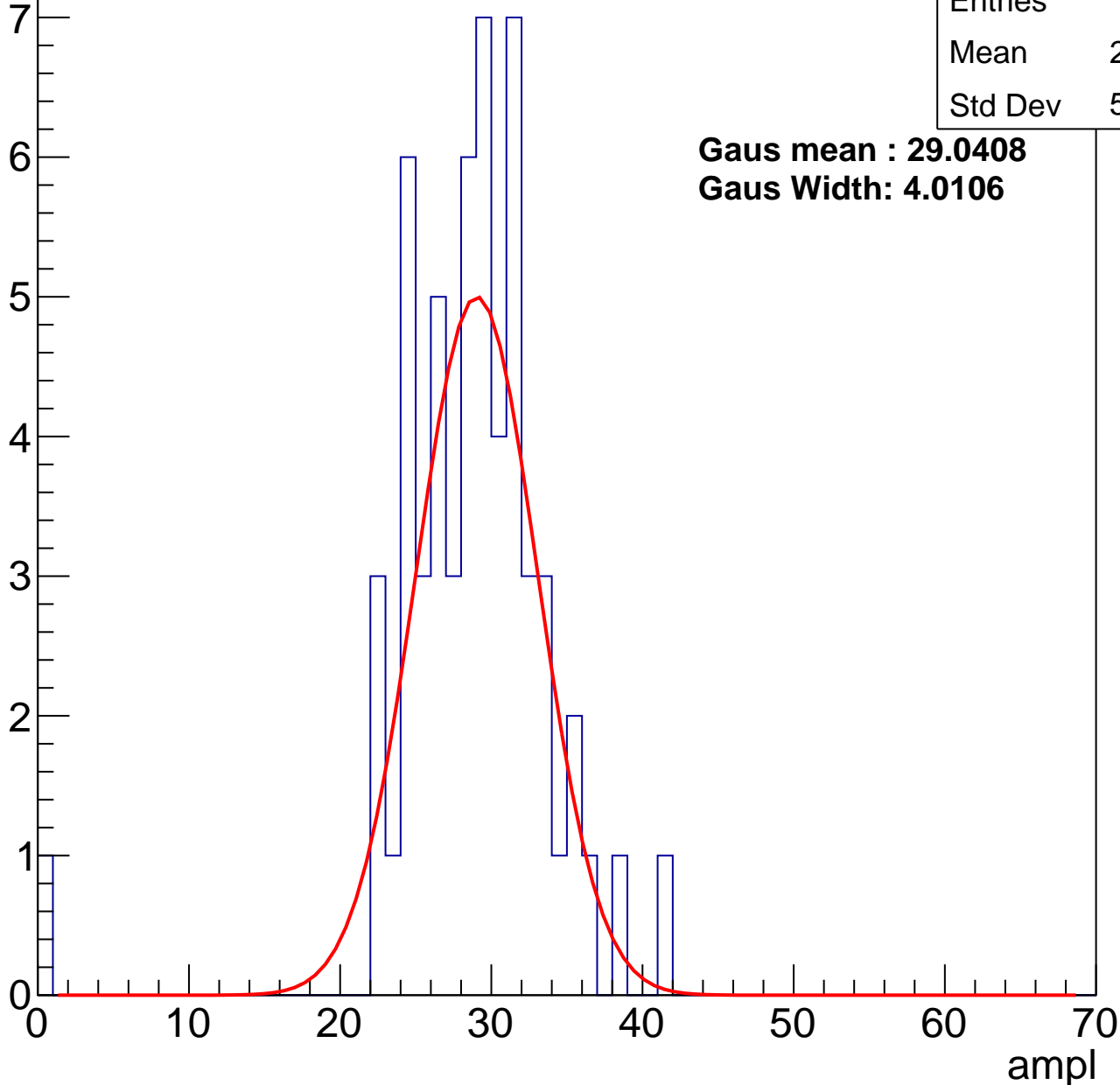
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	58
Mean	28.29
Std Dev	5.468

**Gaus mean : 29.0408**

**Gaus Width: 4.0106**



# B1L103S, U9-ch56, adc1

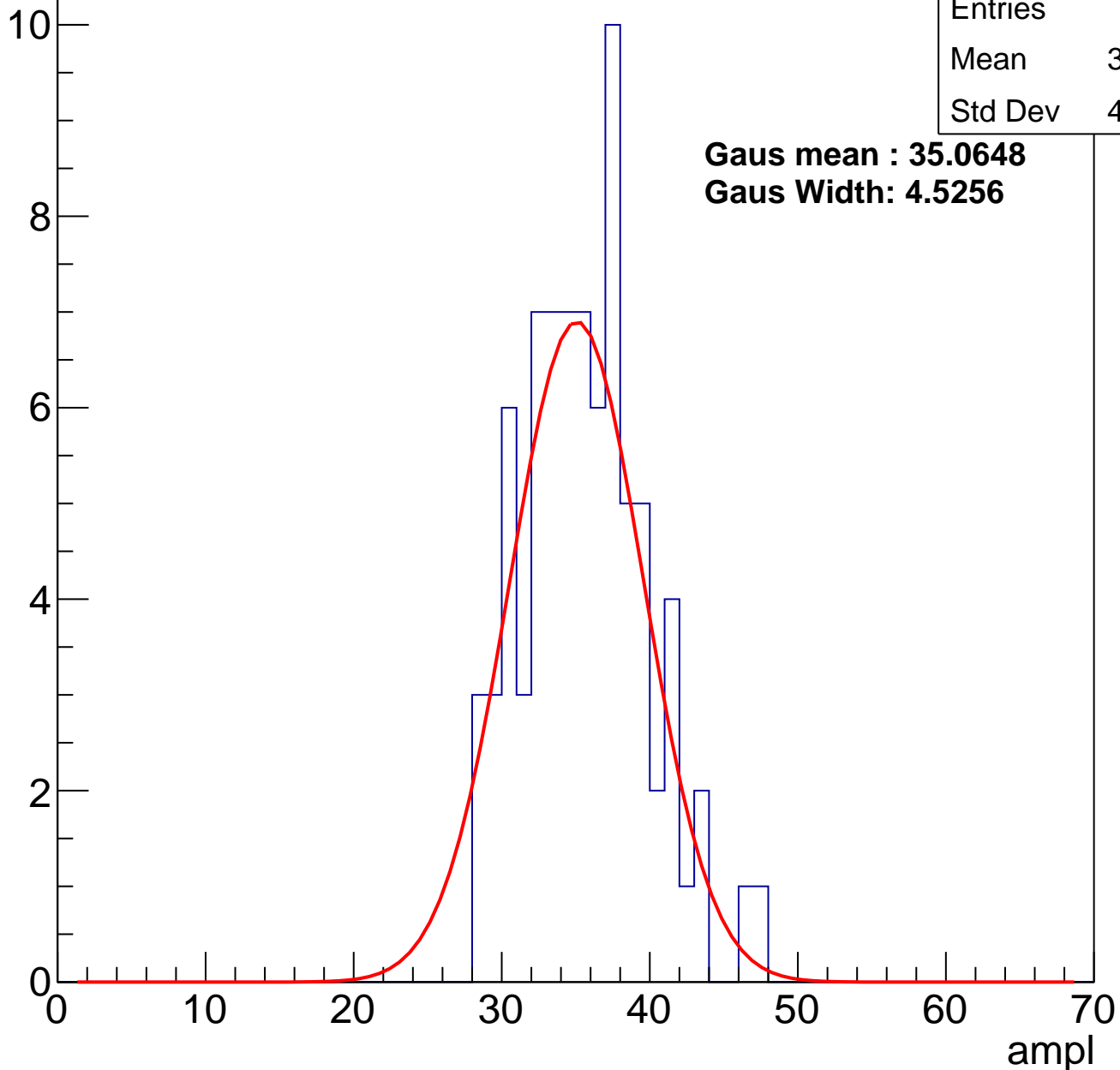
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	80
Mean	35.23
Std Dev	4.114

**Gaus mean : 35.0648**

**Gaus Width: 4.5256**

Entry



# B1L103S, U9-ch56, adc2

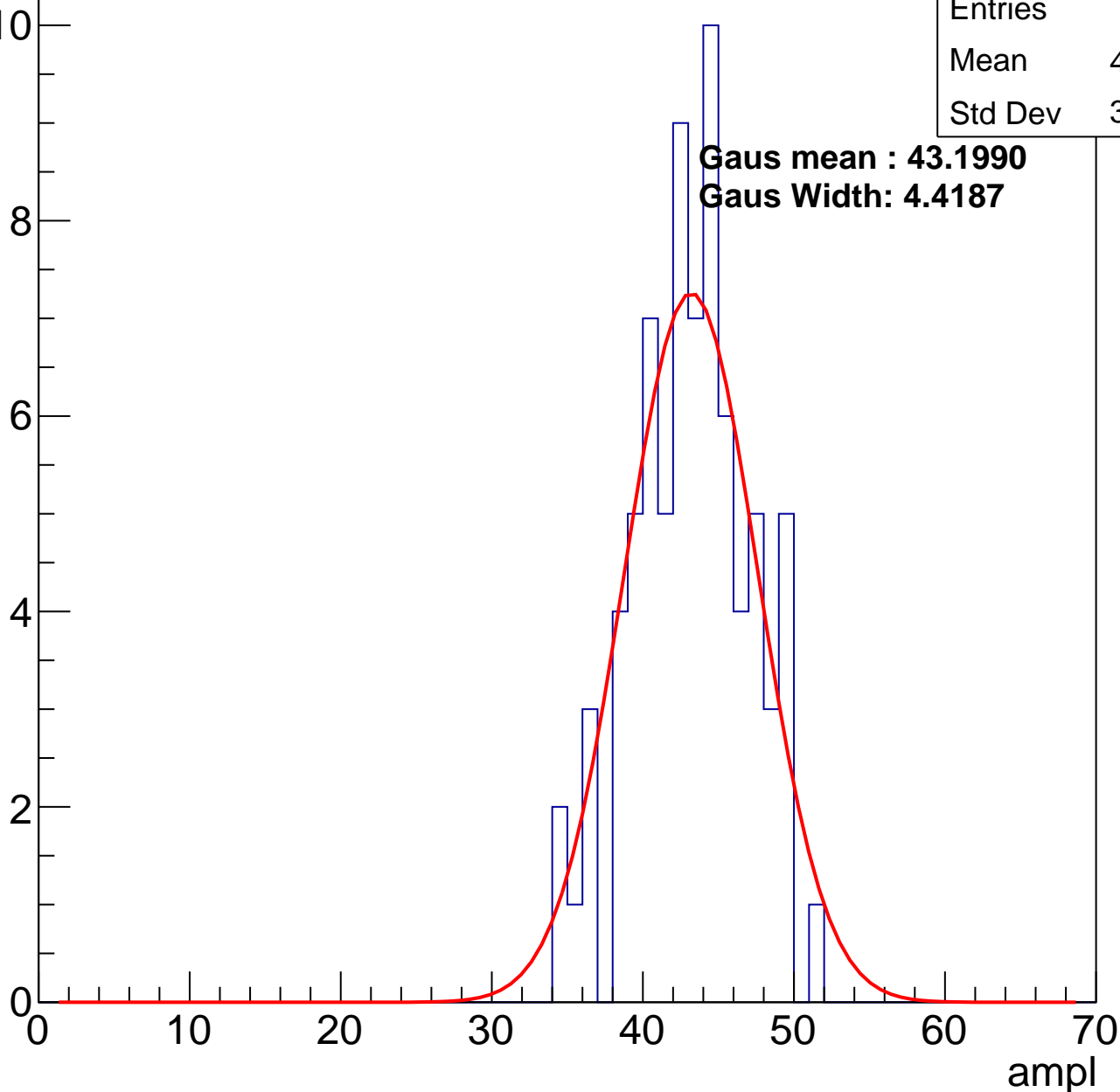
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	77
Mean	42.74
Std Dev	3.795

**Gaus mean : 43.1990**

**Gaus Width: 4.4187**

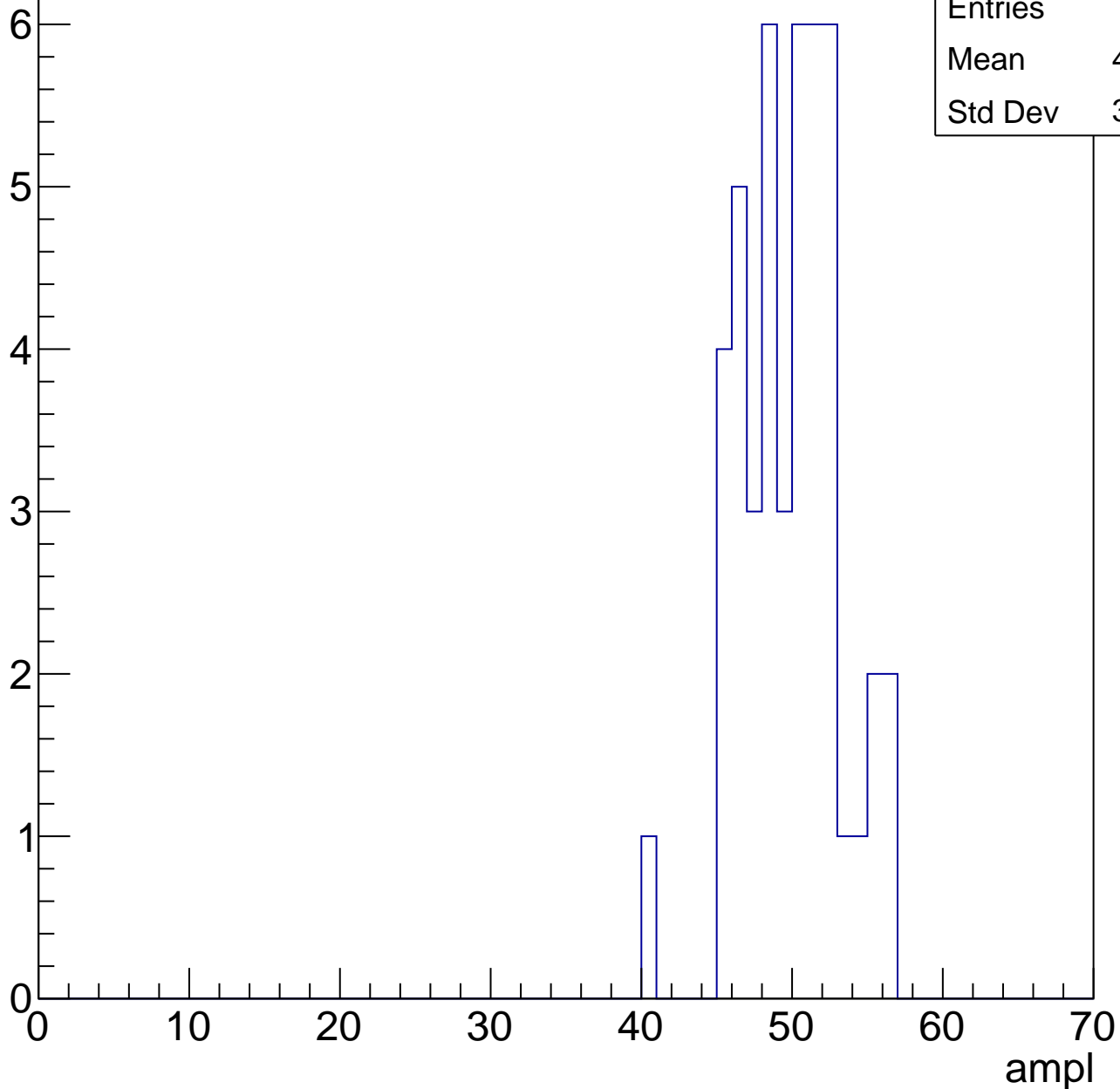


# B1L103S, U9-ch56, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	46
Mean	49.41
Std Dev	3.281

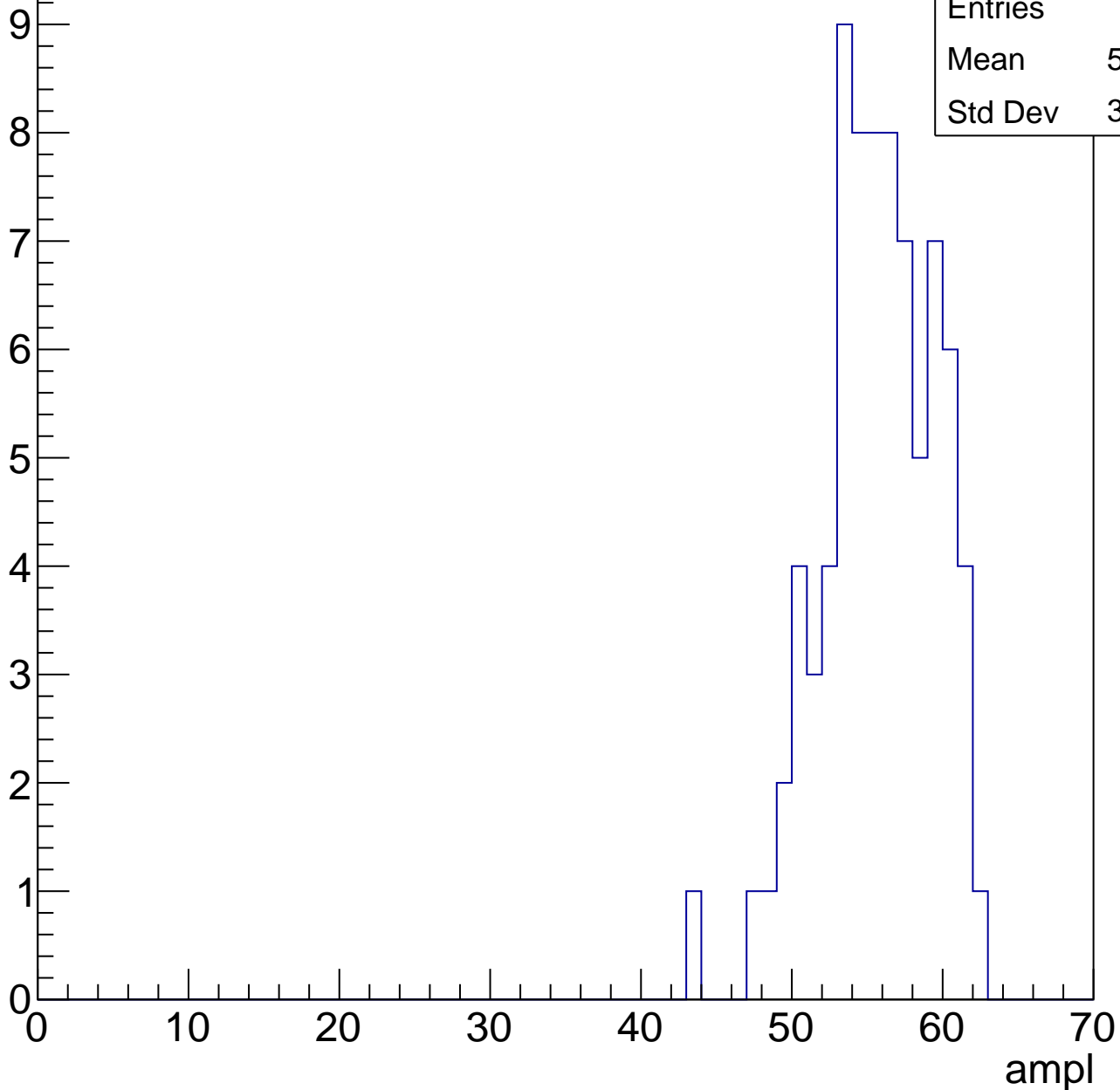


# B1L103S, U9-ch56, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	79
Mean	55.22
Std Dev	3.713

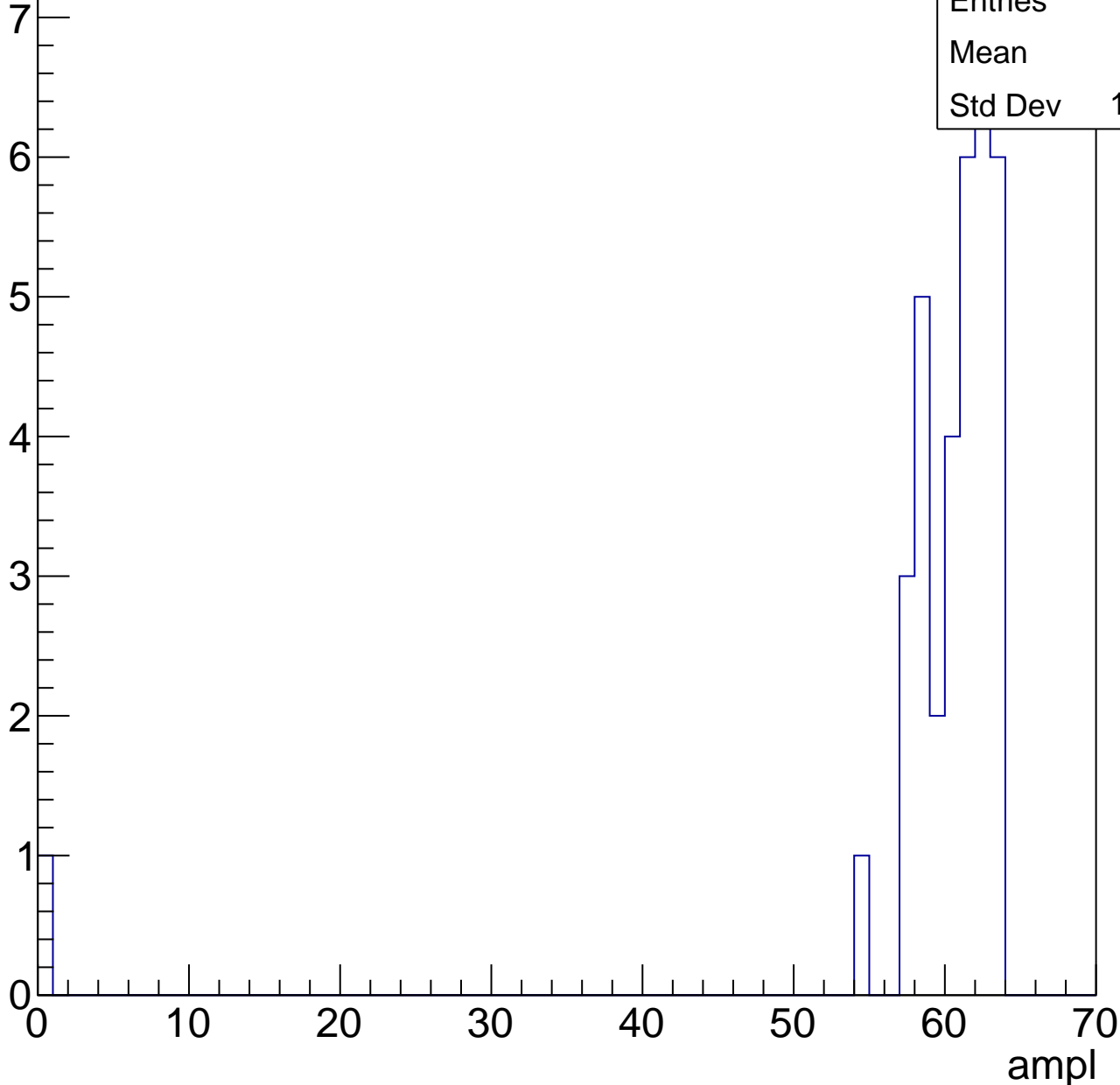


# B1L103S, U9-ch56, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

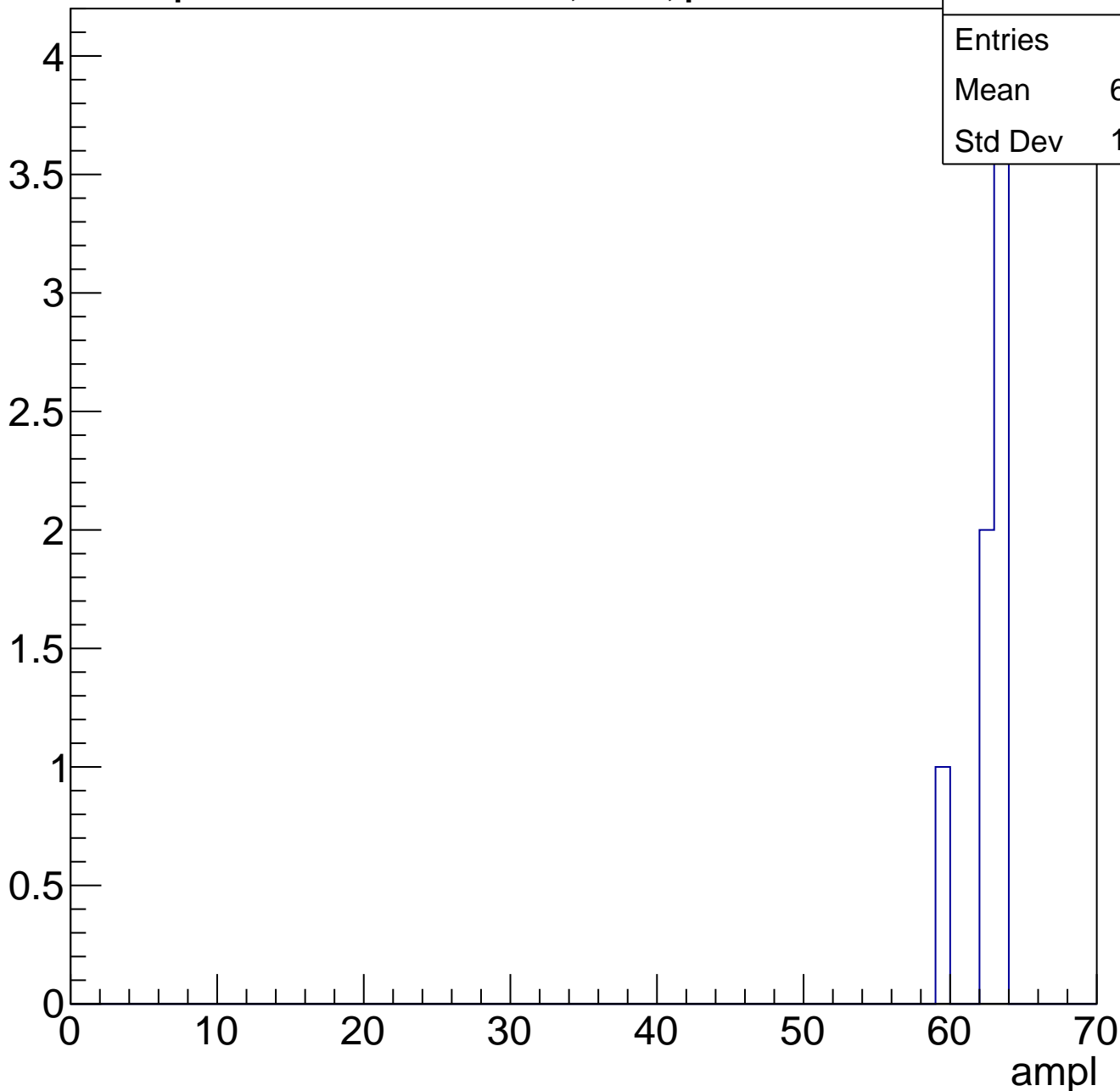
Entries	35
Mean	58.6
Std Dev	10.29



# B1L103S, U9-ch56, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

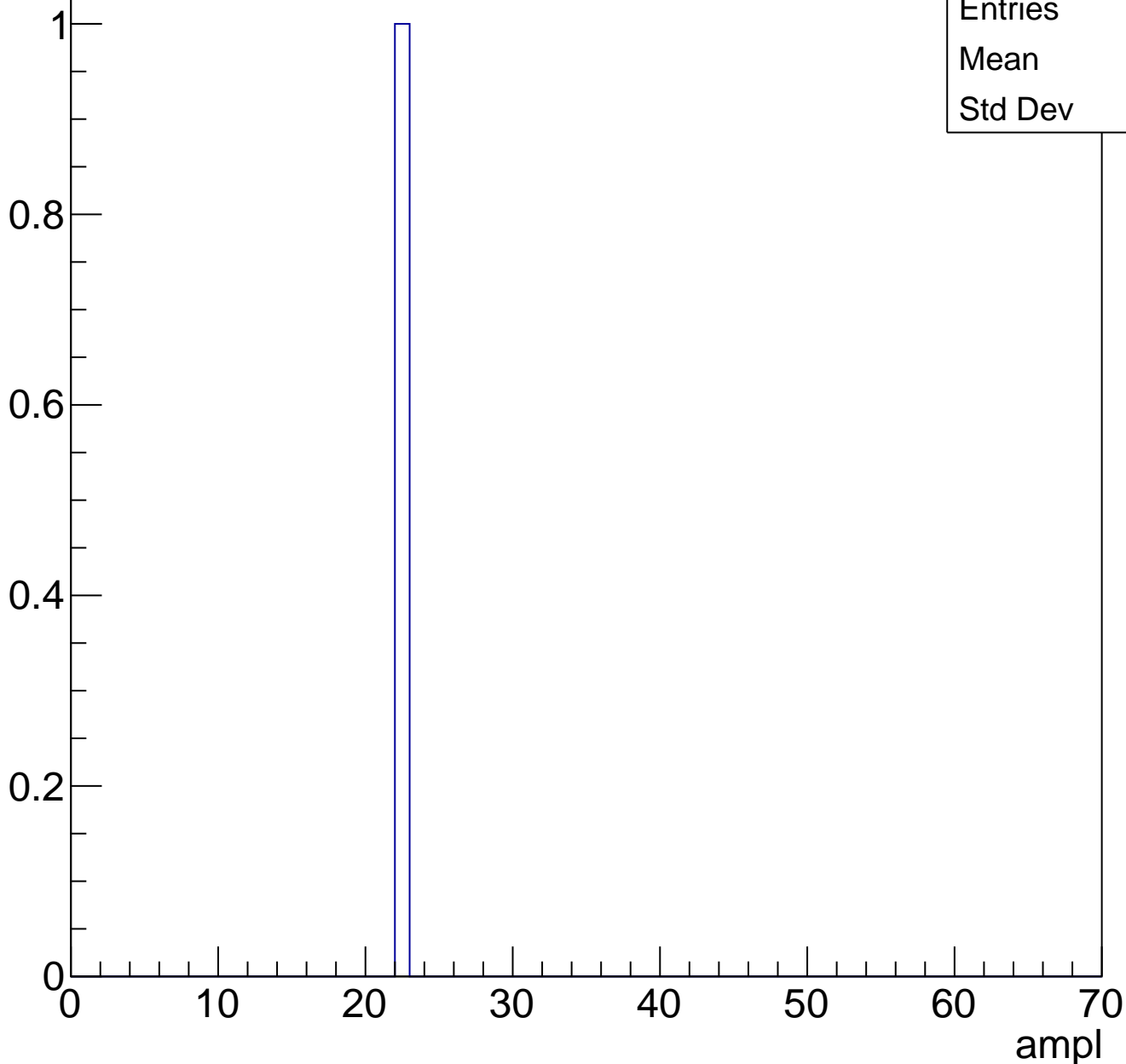




# B1L103S, U9-ch56, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U9-ch57, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	61
Mean	29.95
Std Dev	3.144

**Gaus mean : 30.4078**

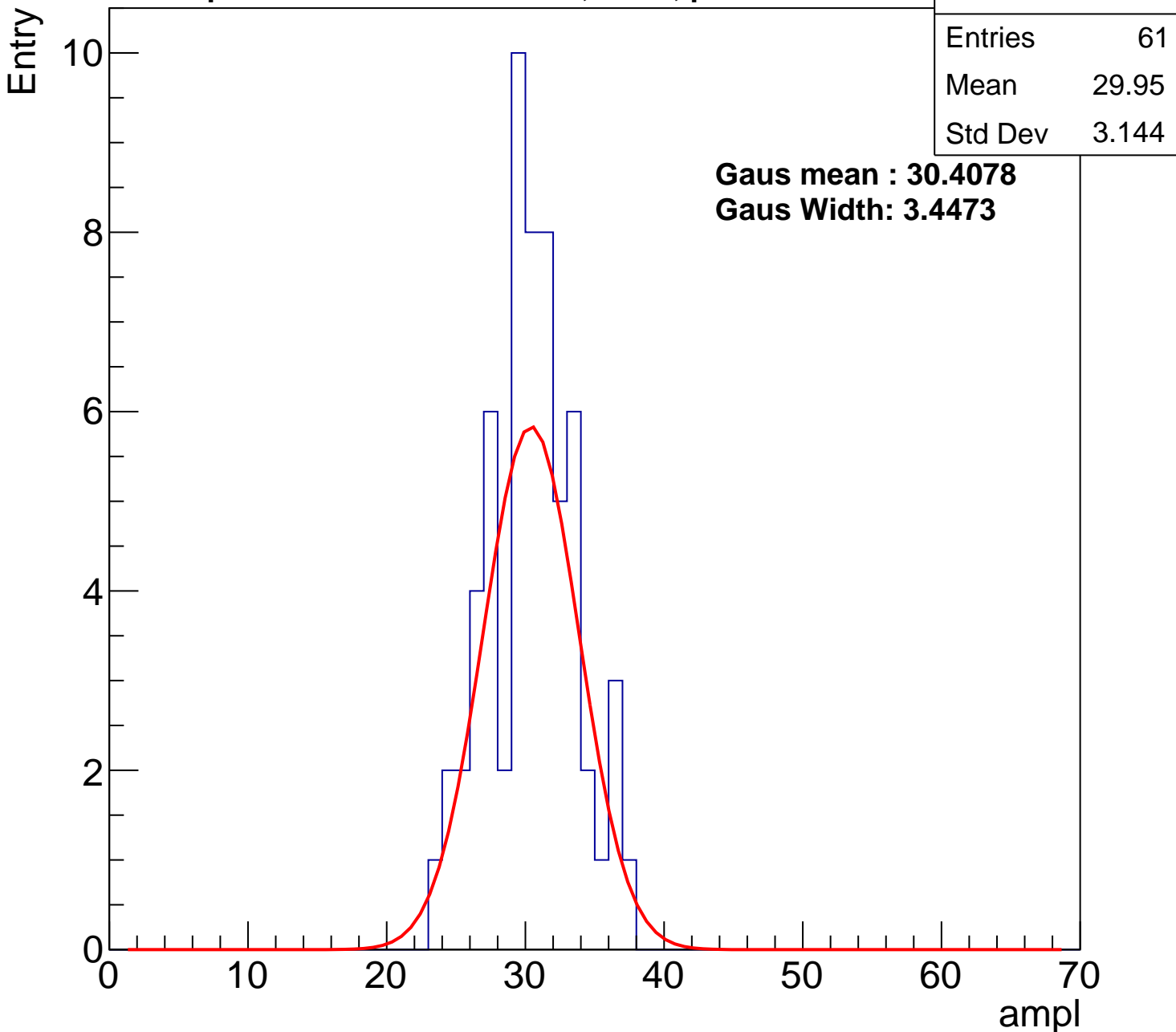
**Gaus Width: 3.4473**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U9-ch57, adc1

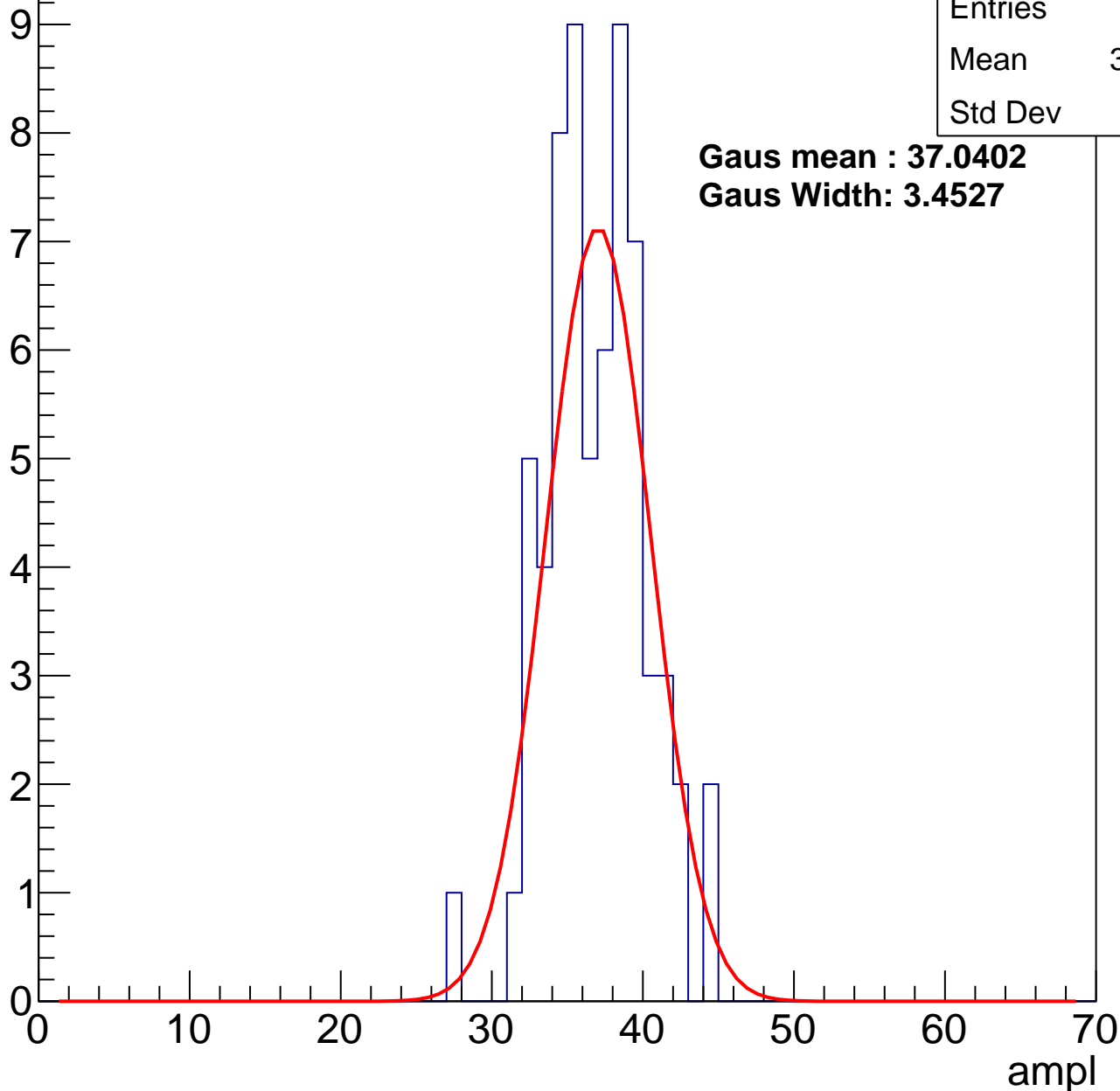
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	36.45
Std Dev	3.23

**Gaus mean : 37.0402**

**Gaus Width: 3.4527**



# B1L103S, U9-ch57, adc2

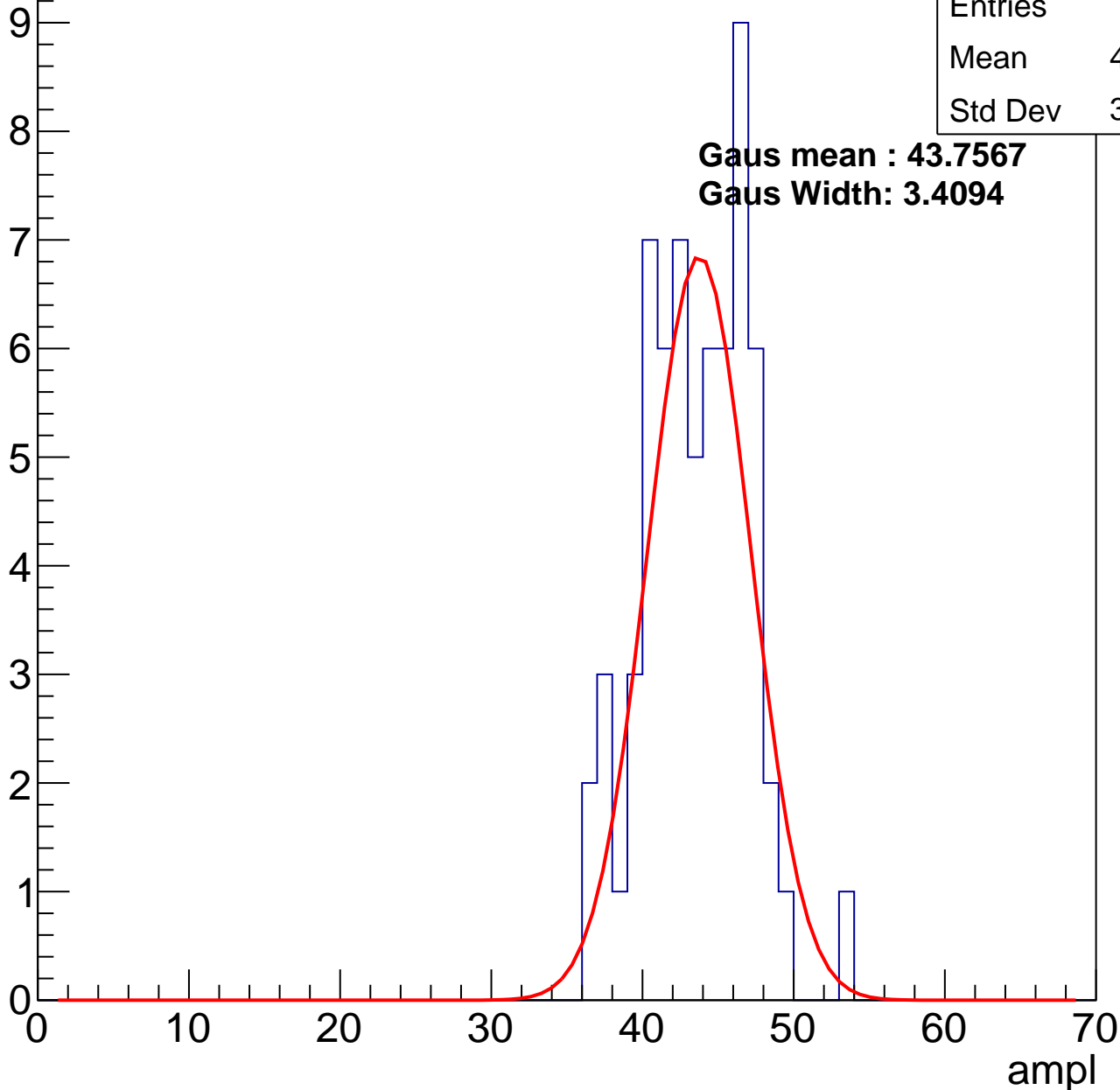
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	43.09
Std Dev	3.432

**Gaus mean : 43.7567**

**Gaus Width: 3.4094**



# B1L103S, U9-ch57, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

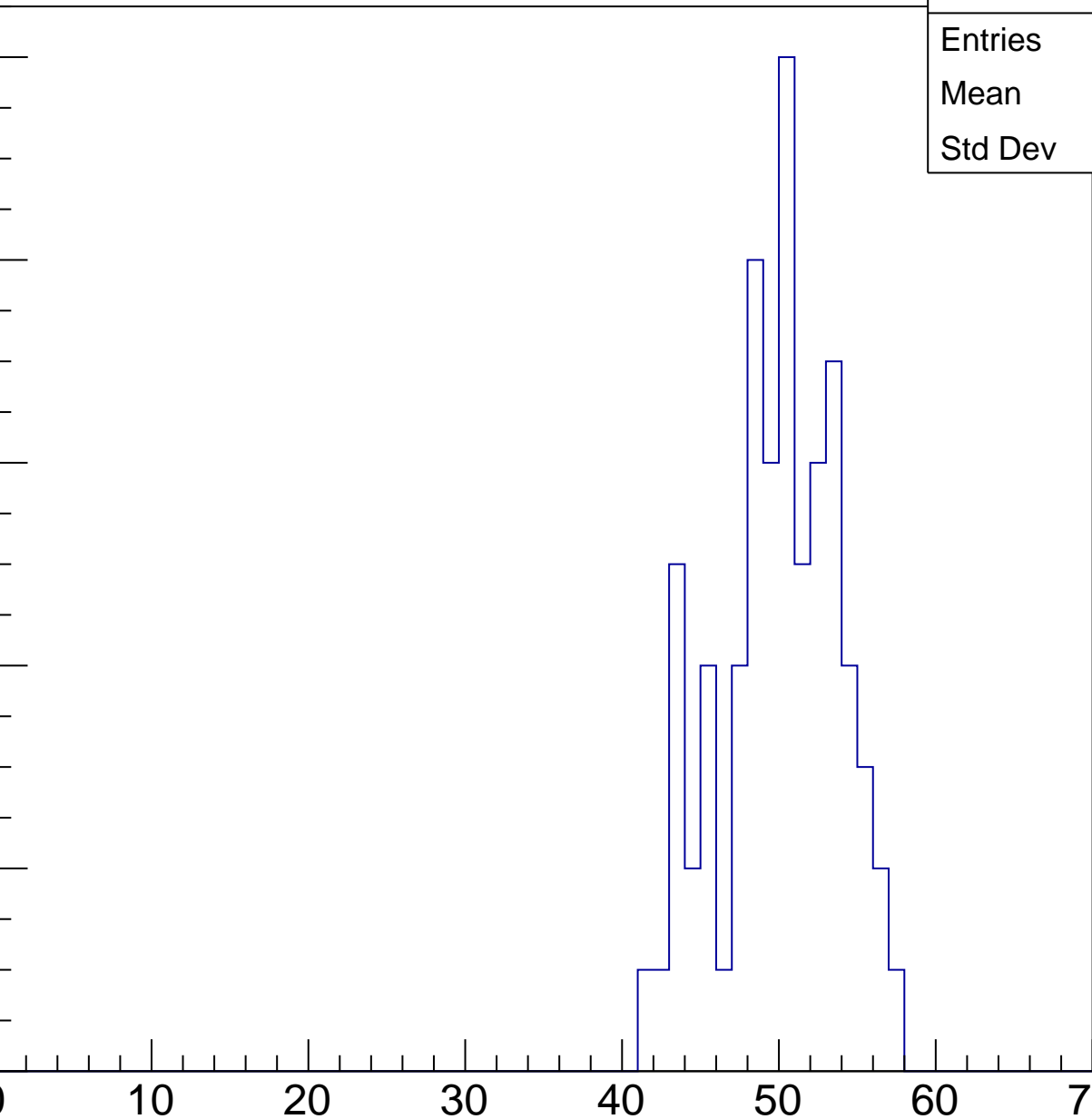
Entries	70
Mean	49.51
Std Dev	3.756

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

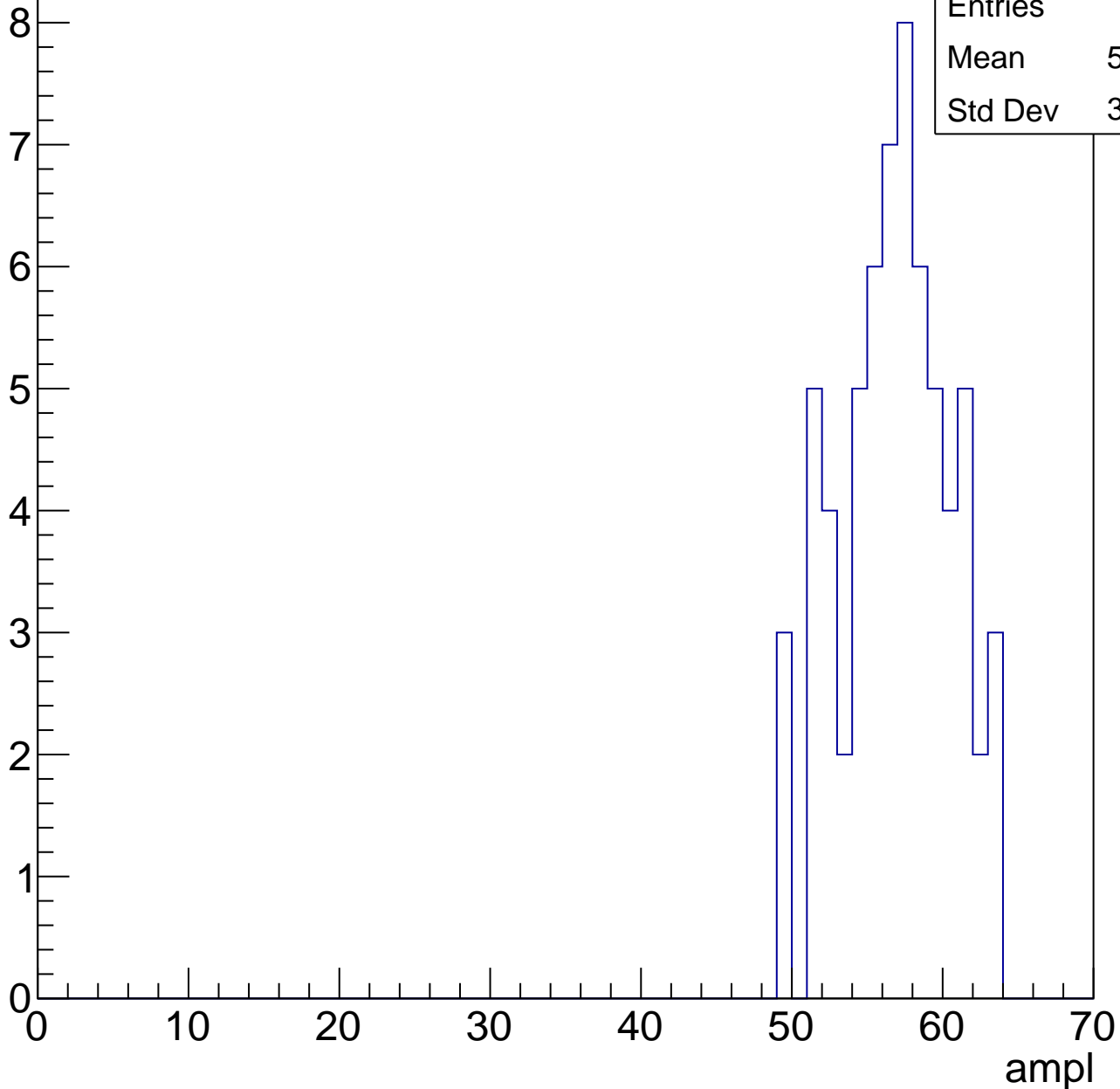


# B1L103S, U9-ch57, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	56.38
Std Dev	3.628



# B1L103S, U9-ch57, adc5

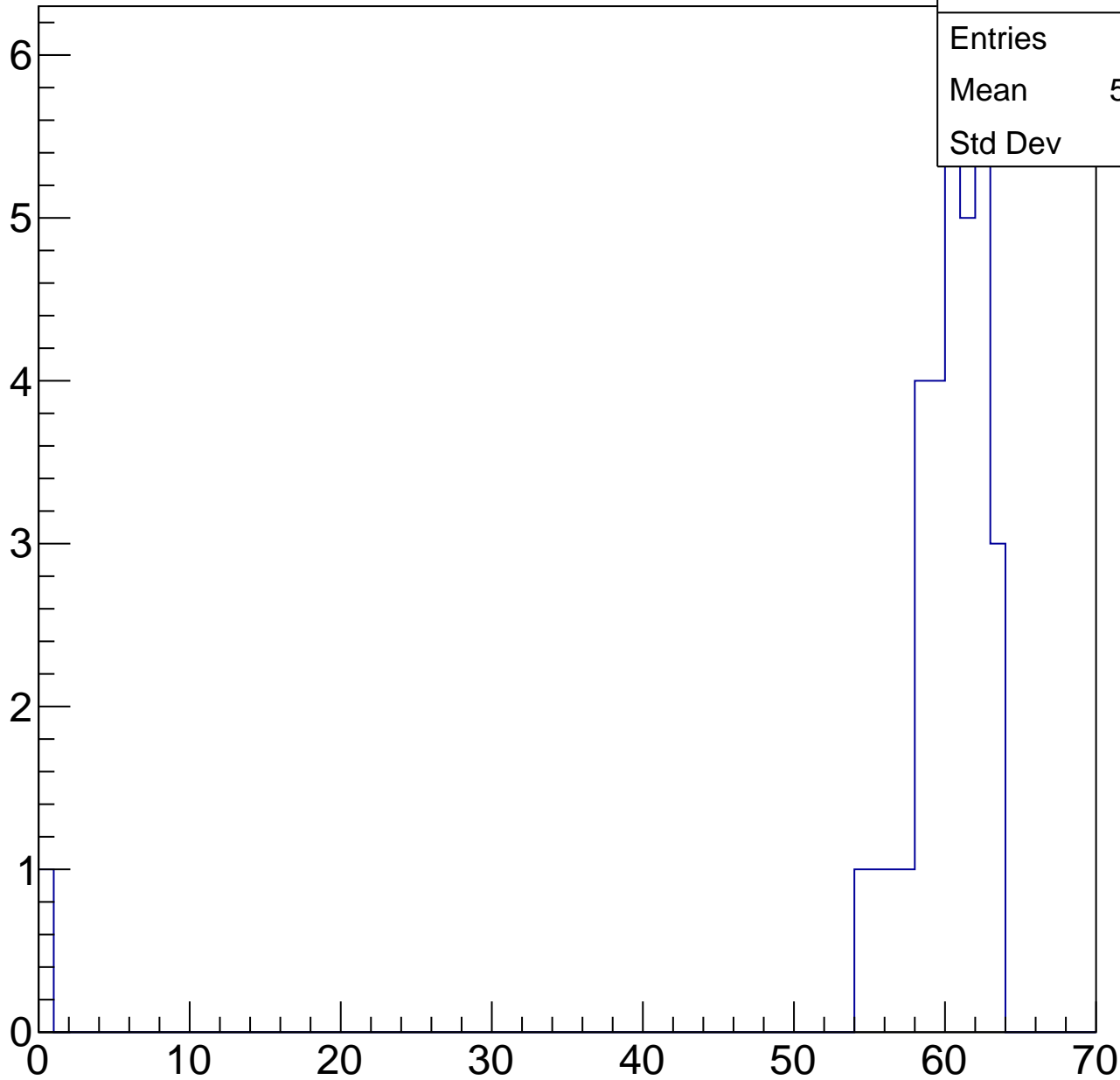
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

6  
5  
4  
3  
2  
1  
0

Entries	33
Mean	58.06
Std Dev	10.5

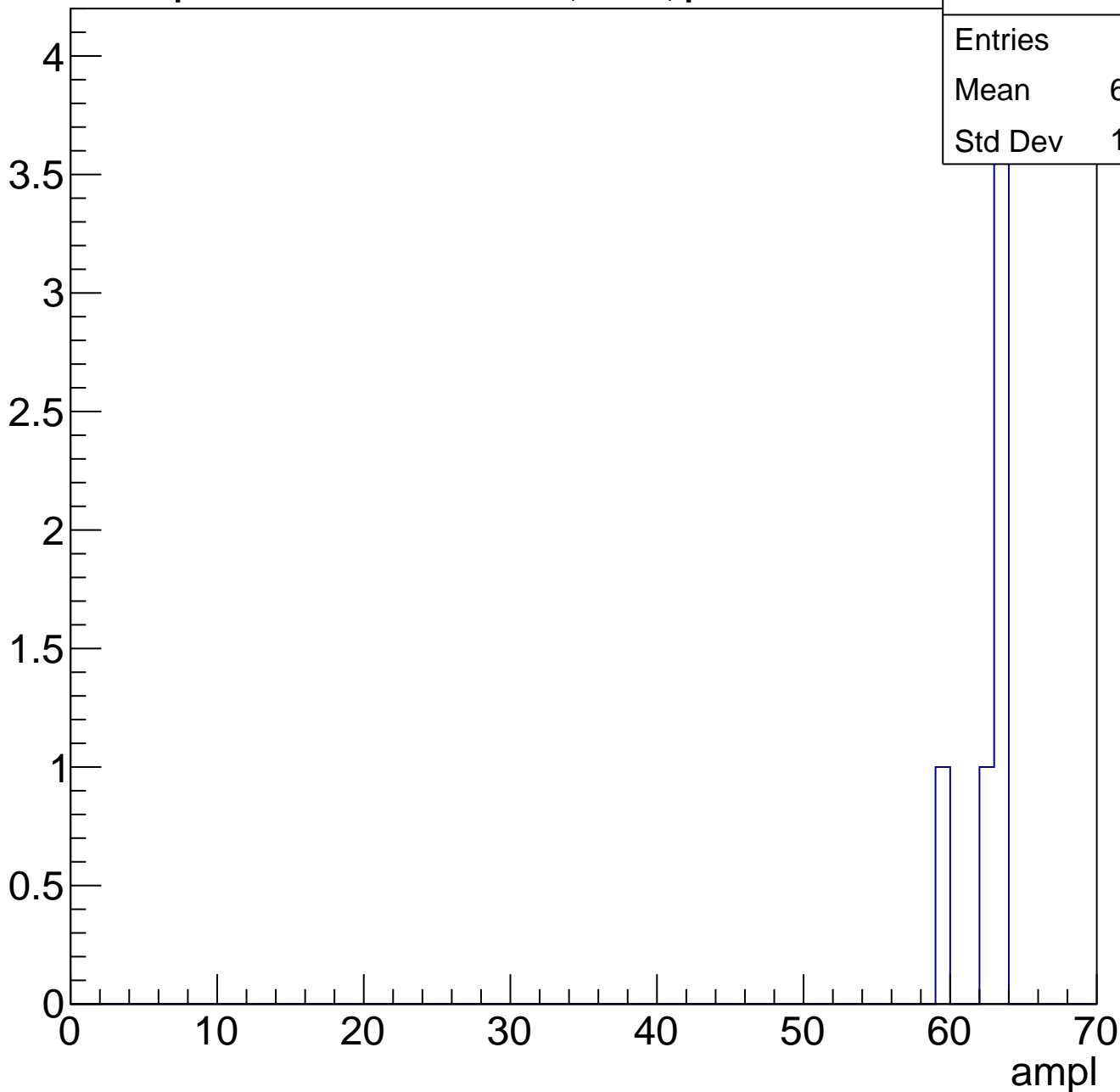
ampl



# B1L103S, U9-ch57, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



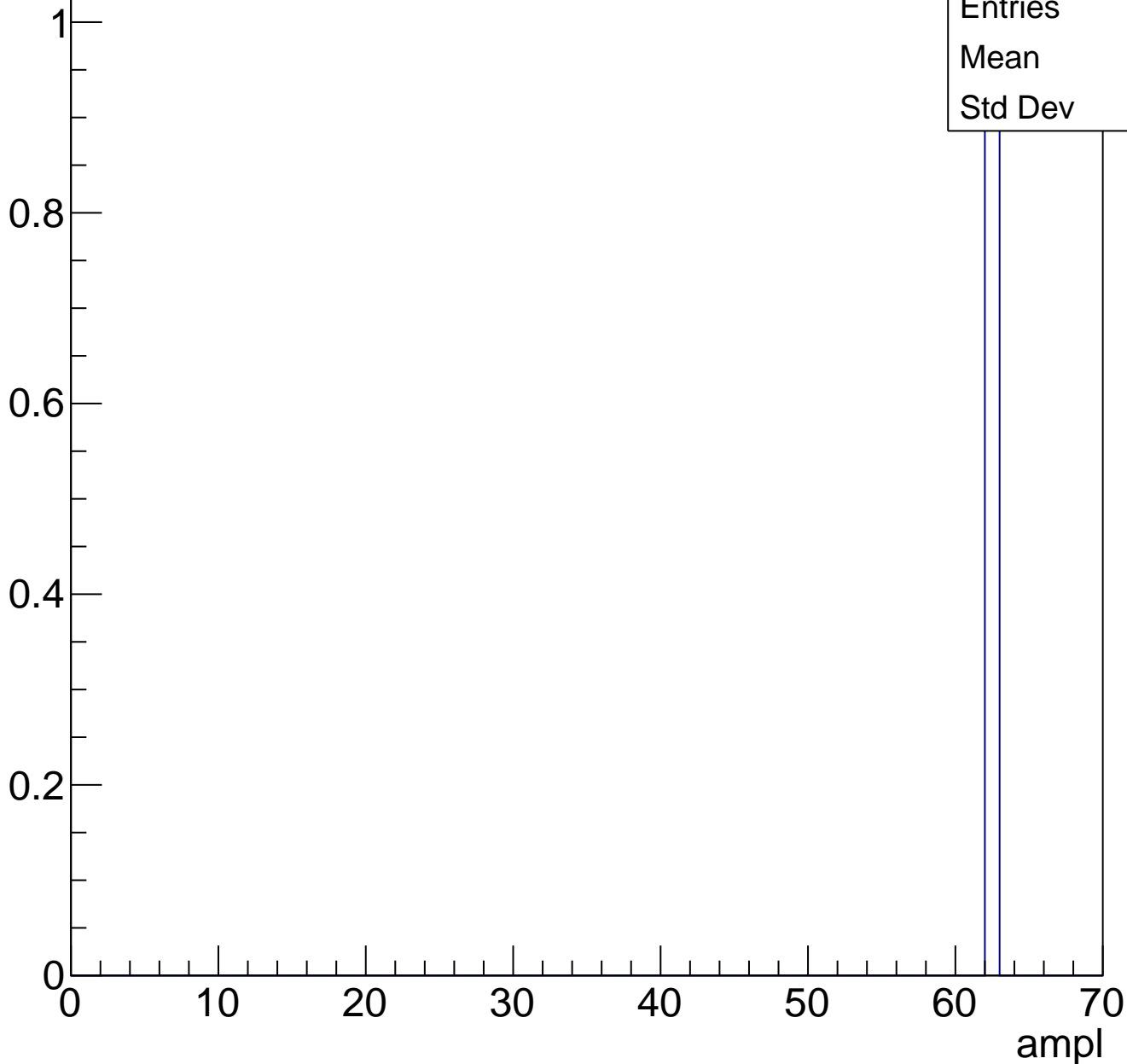
Entries	6
Mean	62.17
Std Dev	1.462



# B1L103S, U9-ch57, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U9-ch58, adc0

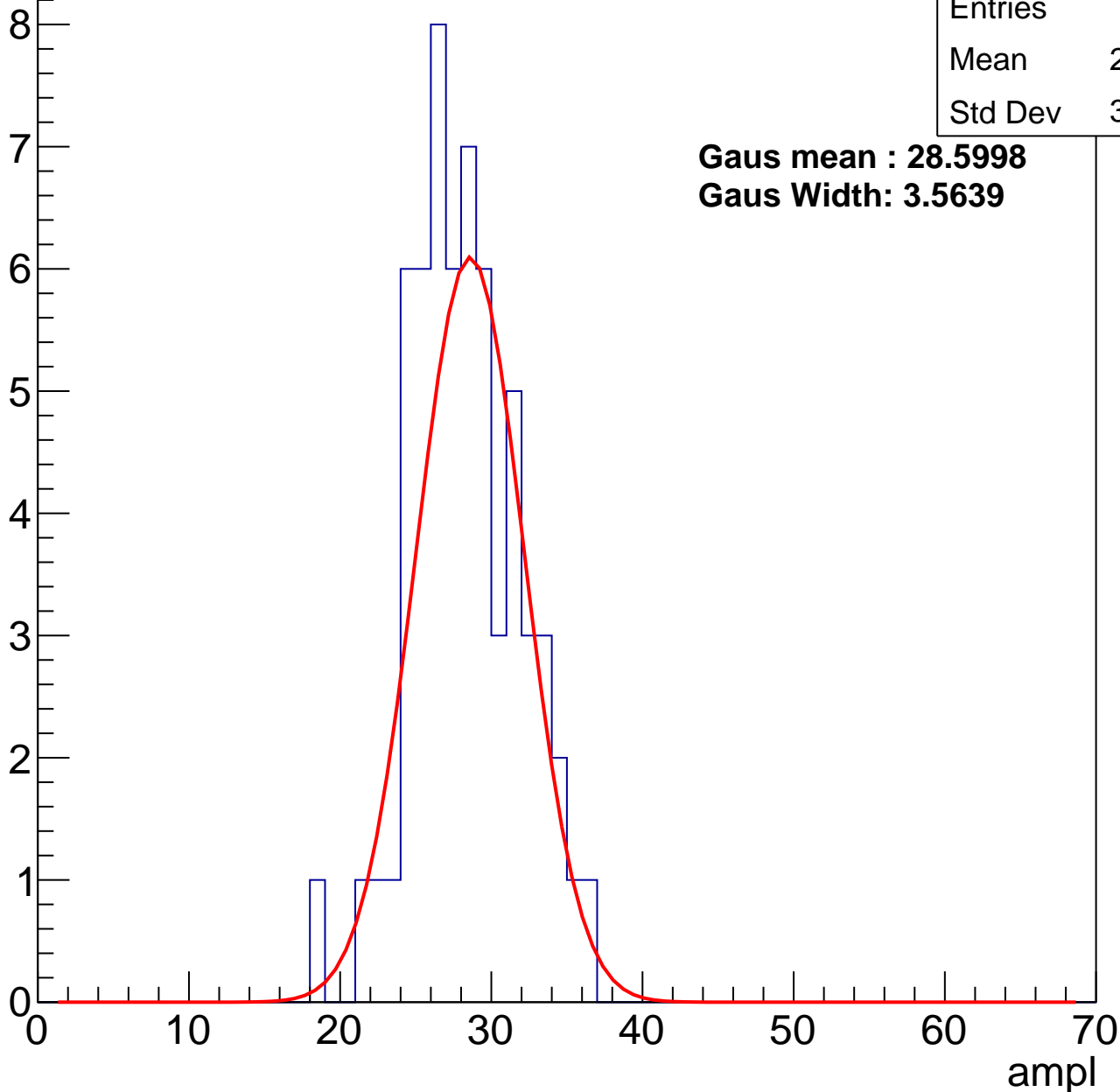
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	61
Mean	27.82
Std Dev	3.546

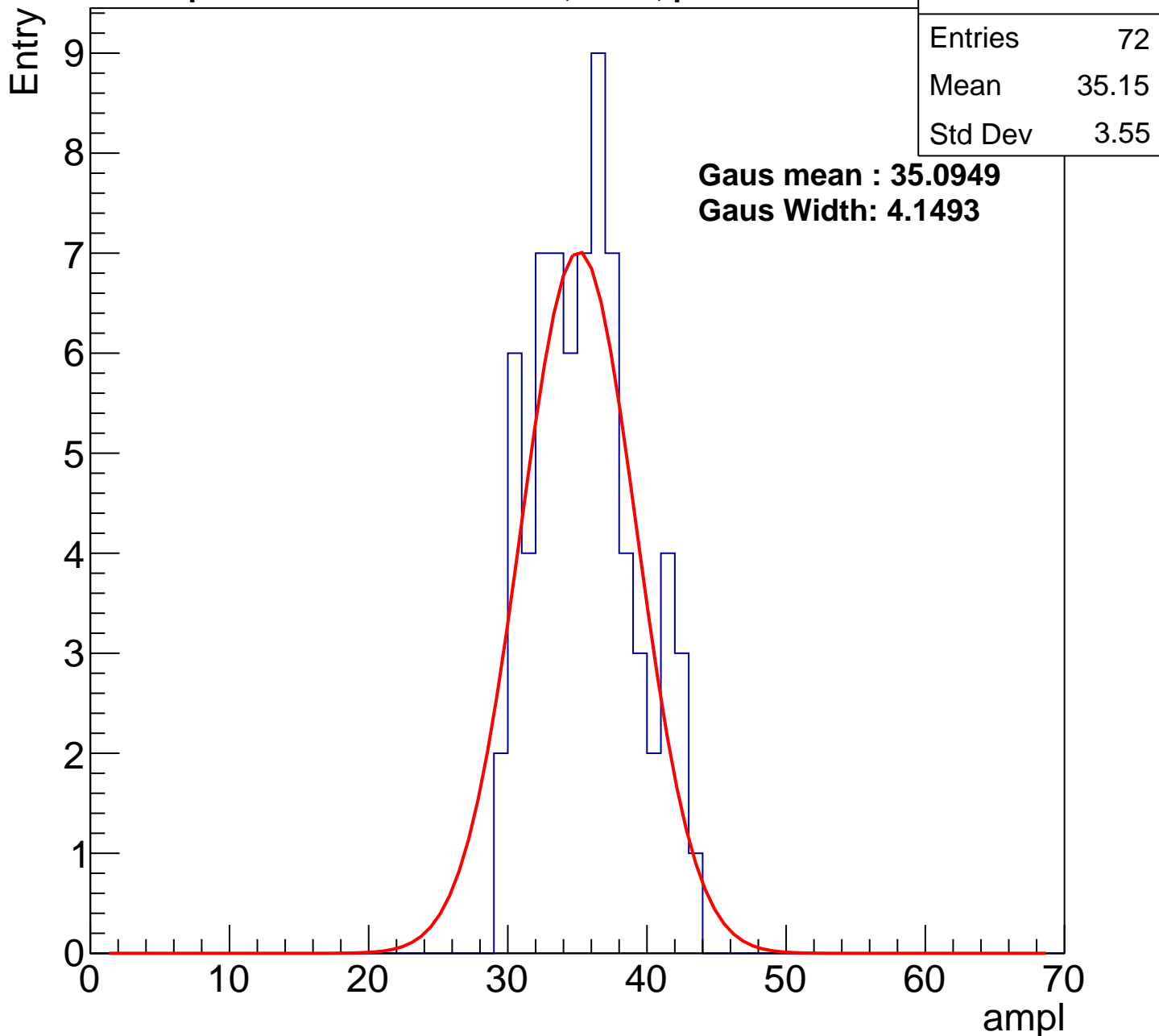
**Gaus mean : 28.5998**

**Gaus Width: 3.5639**



# B1L103S, U9-ch58, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U9-ch58, adc2

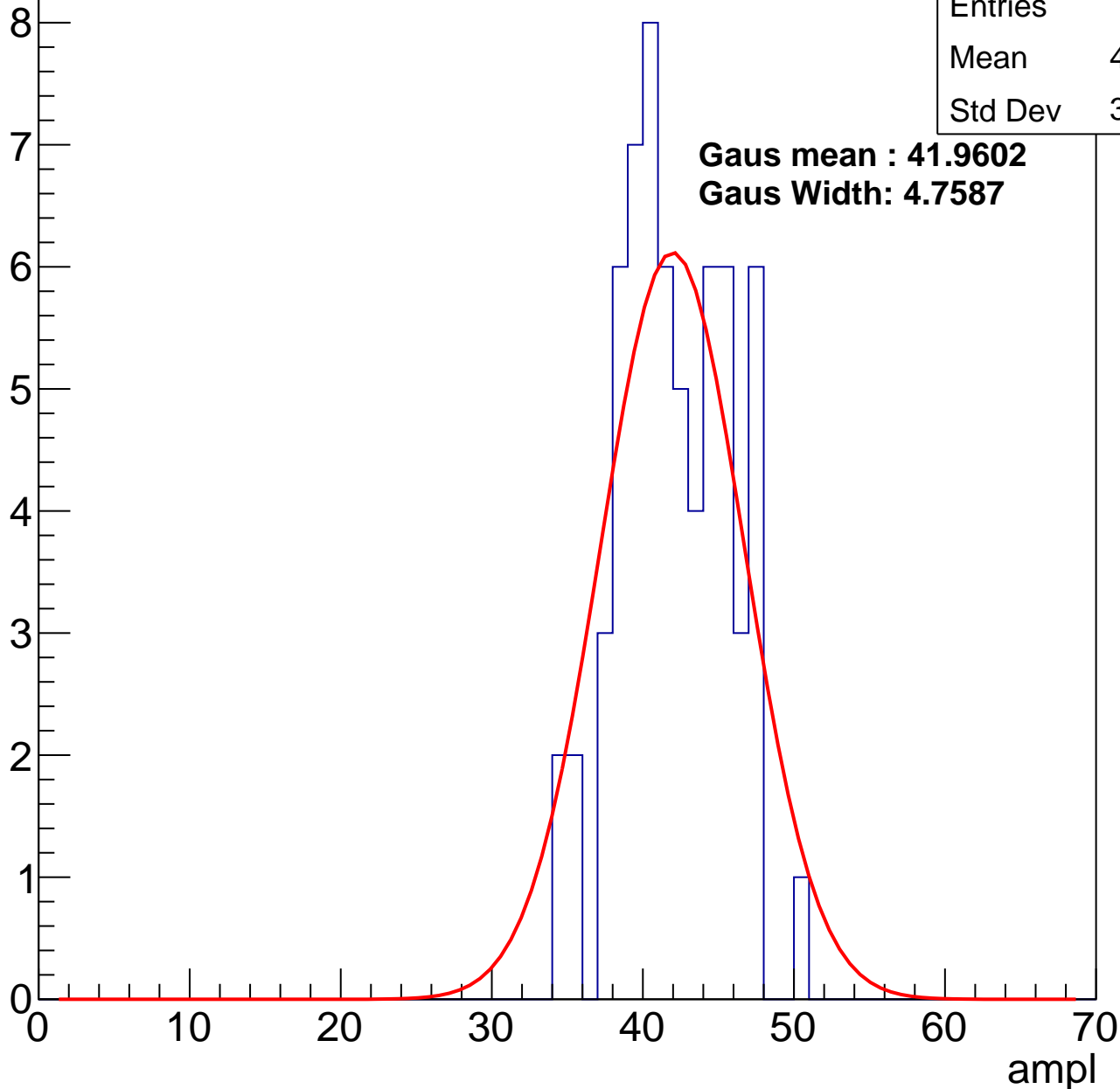
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	41.57
Std Dev	3.573

**Gaus mean : 41.9602**

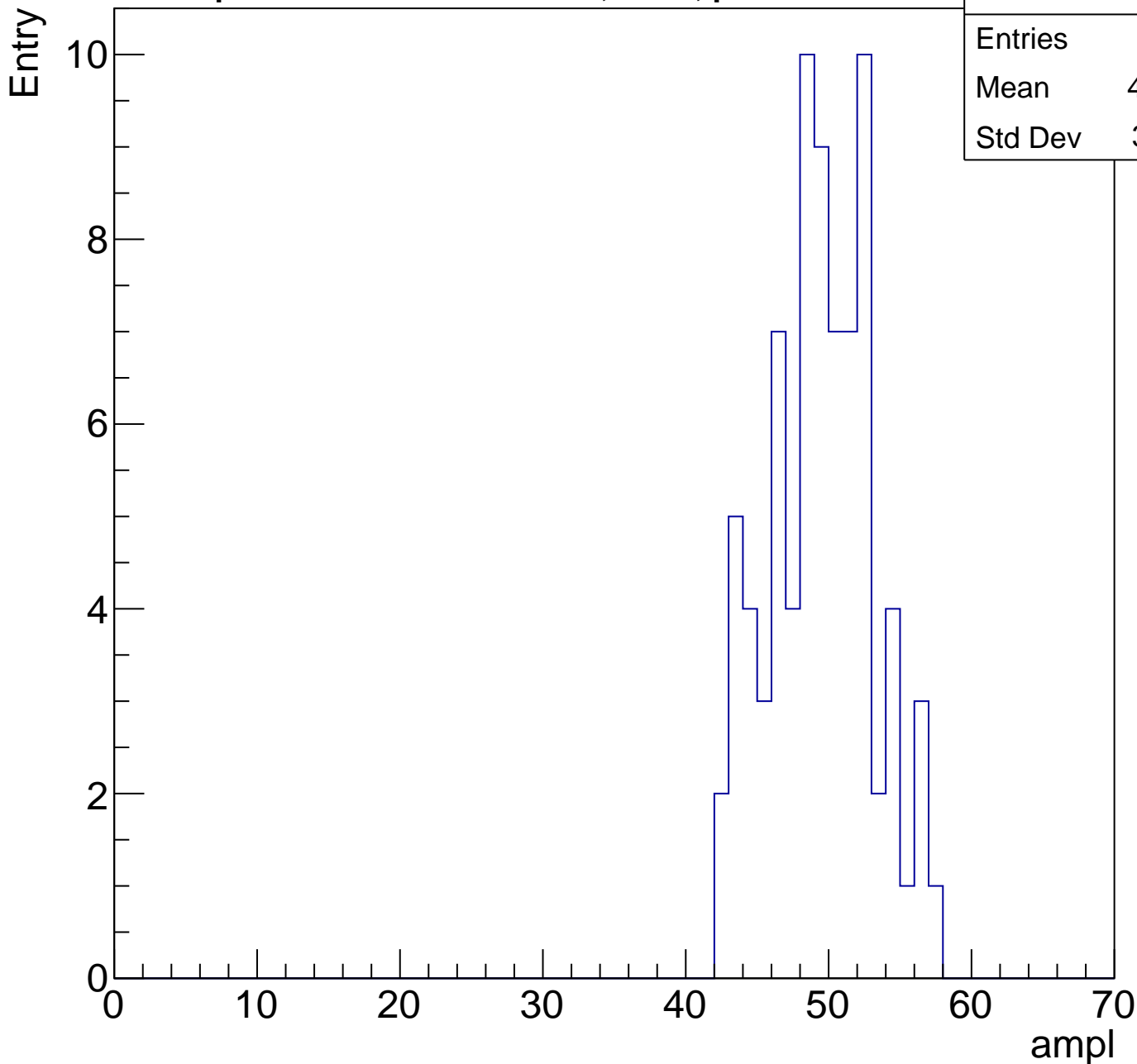
**Gaus Width: 4.7587**



# B1L103S, U9-ch58, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	79
Mean	48.99
Std Dev	3.591

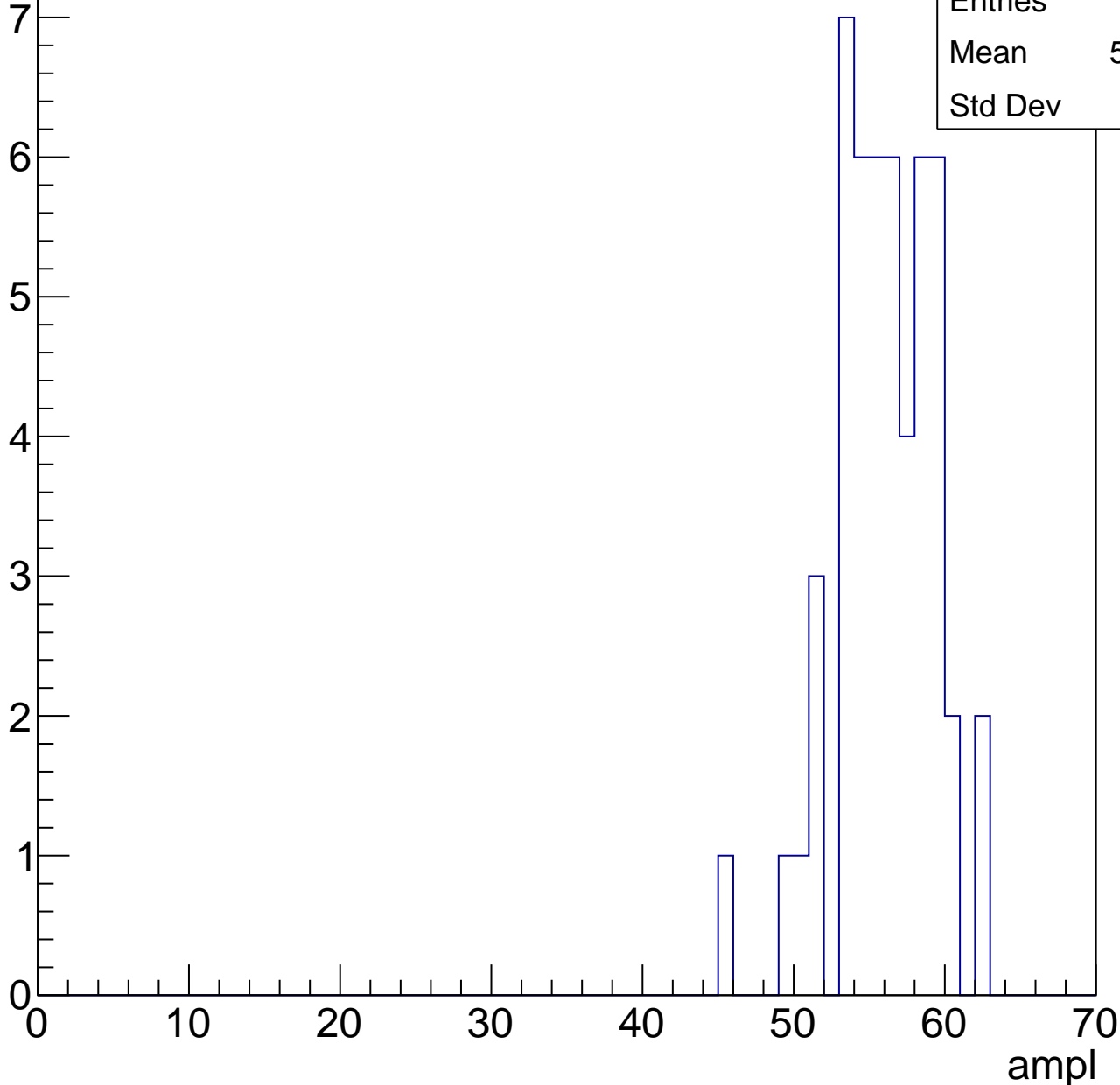


# B1L103S, U9-ch58, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	51
Mean	55.53
Std Dev	3.28

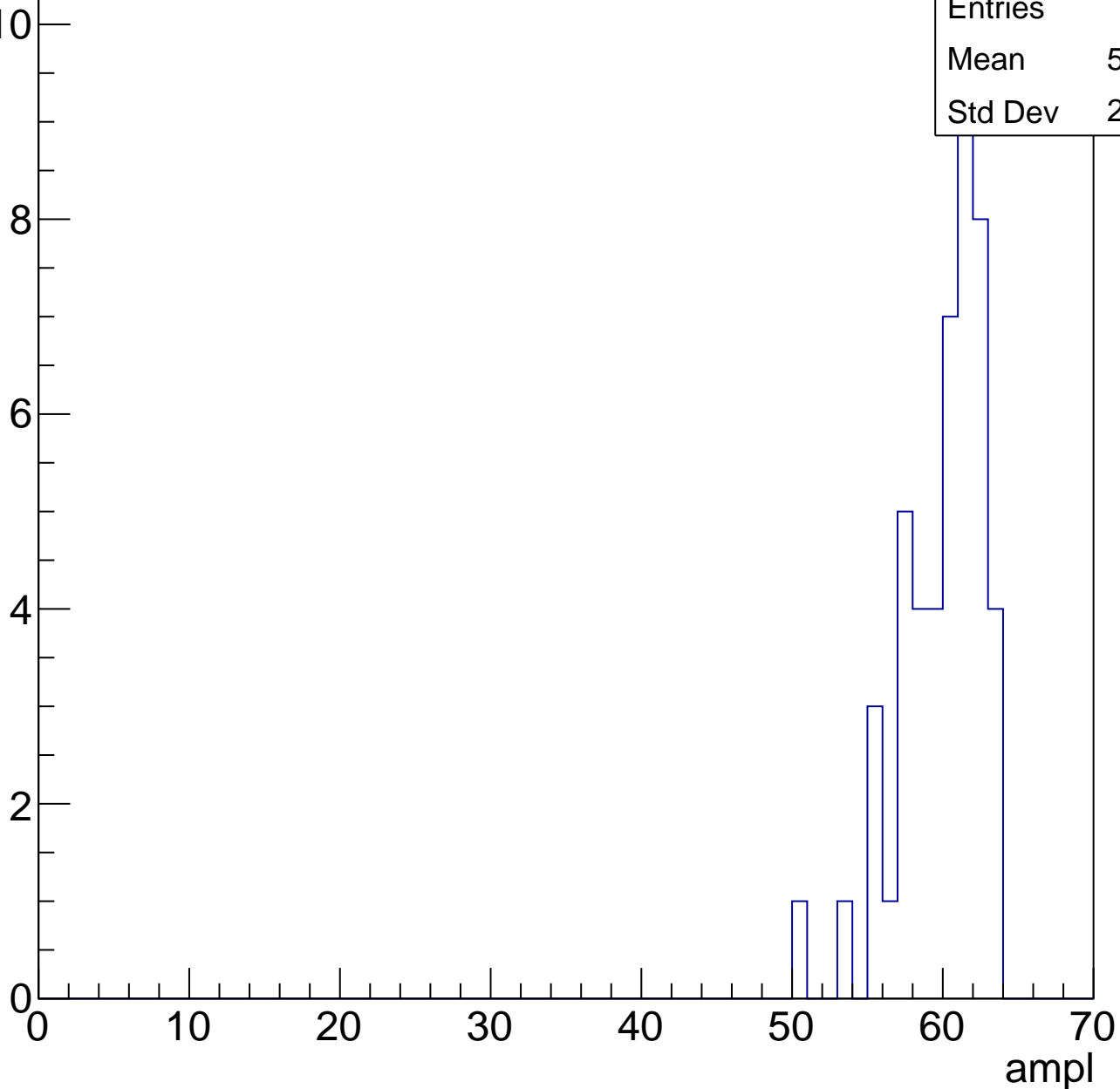


# B1L103S, U9-ch58, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	48
Mean	59.48
Std Dev	2.776

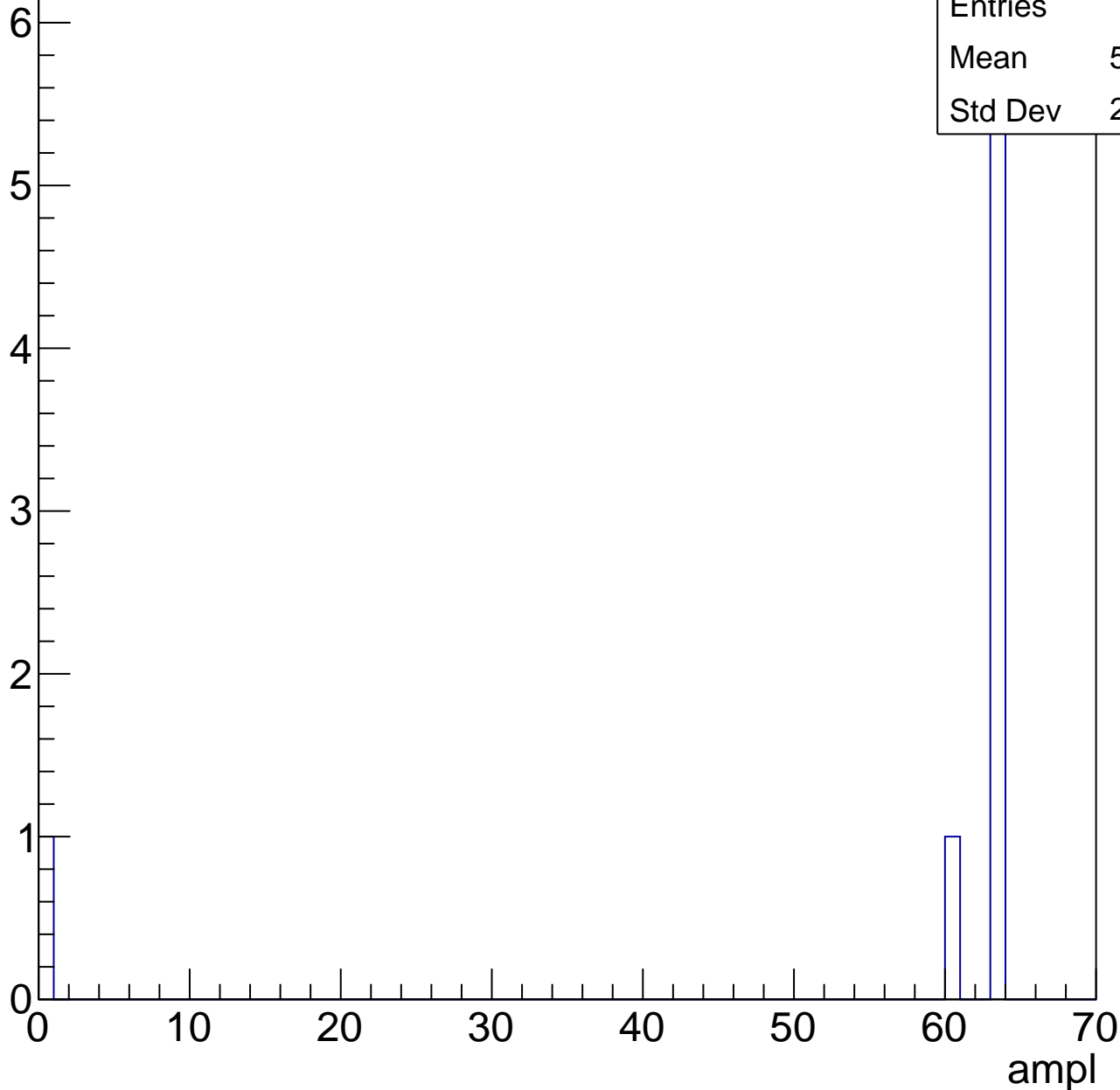


# B1L103S, U9-ch58, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	8
Mean	54.75
Std Dev	20.72





# B1L103S, U9-ch58, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L103S, U9-ch59, adc0

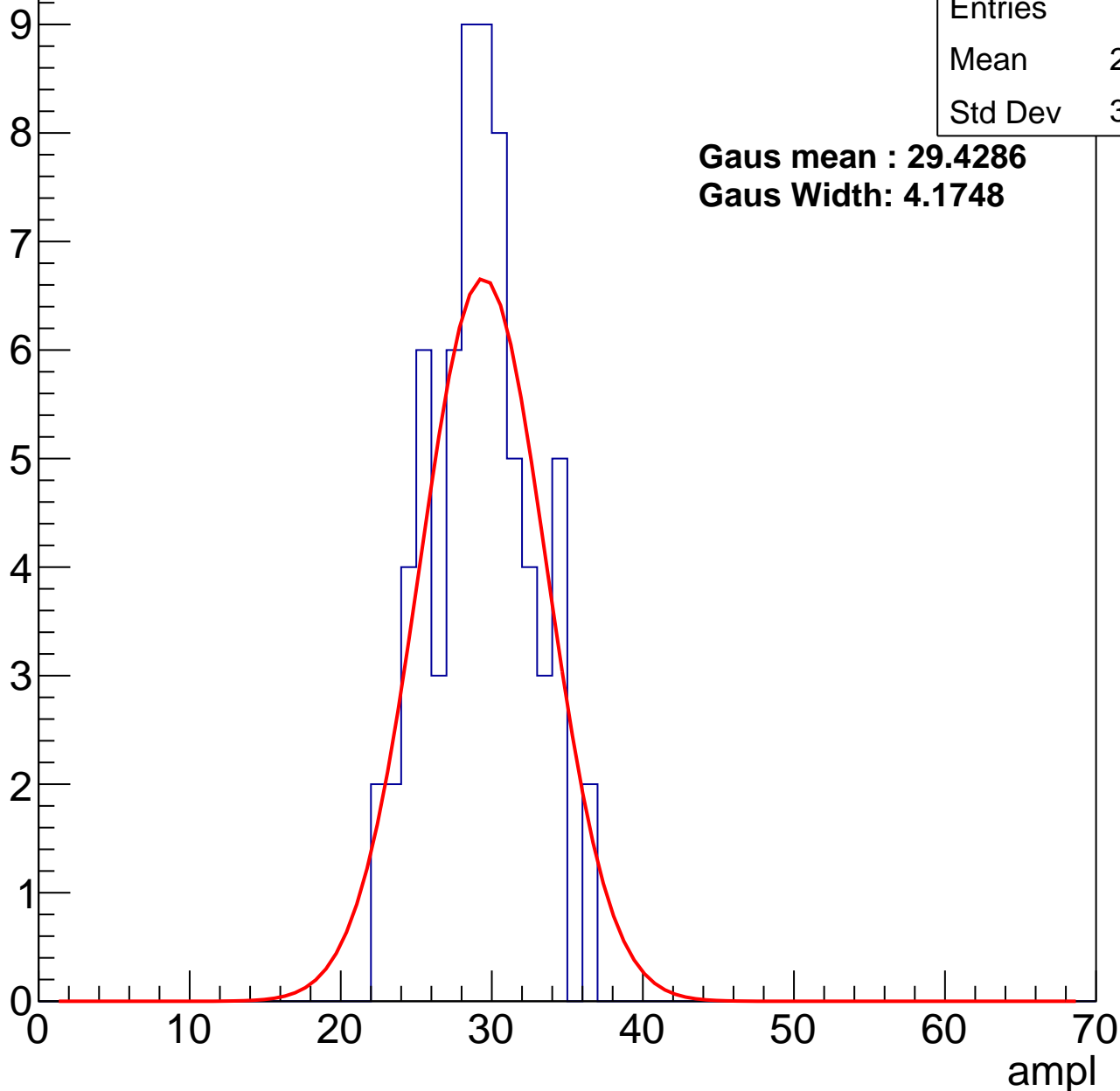
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	68
Mean	28.72
Std Dev	3.334

**Gaus mean : 29.4286**

**Gaus Width: 4.1748**



# B1L103S, U9-ch59, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	83
Mean	36.67
Std Dev	3.758

**Gaus mean : 36.6448**

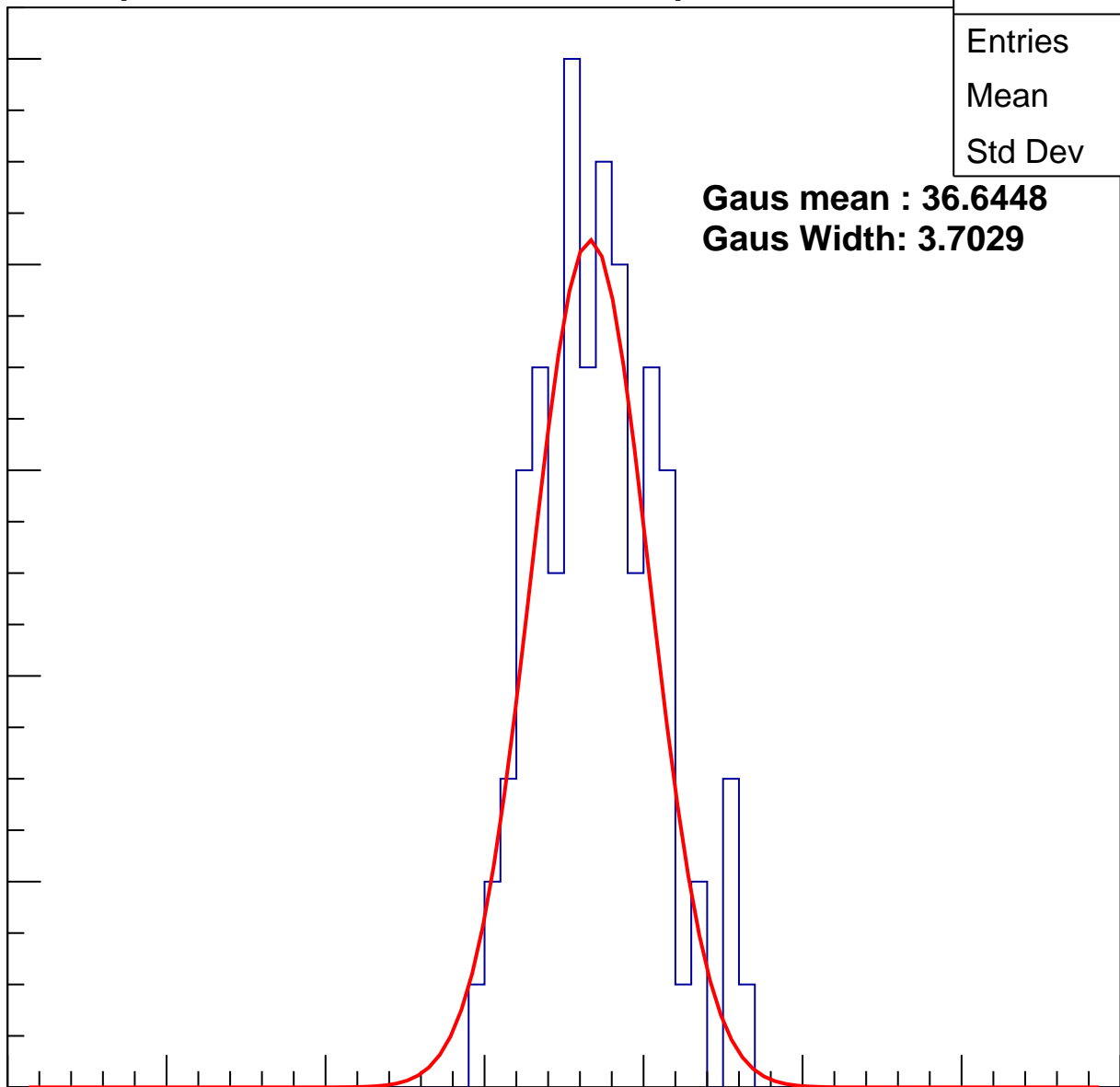
**Gaus Width: 3.7029**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B1L103S, U9-ch59, adc2

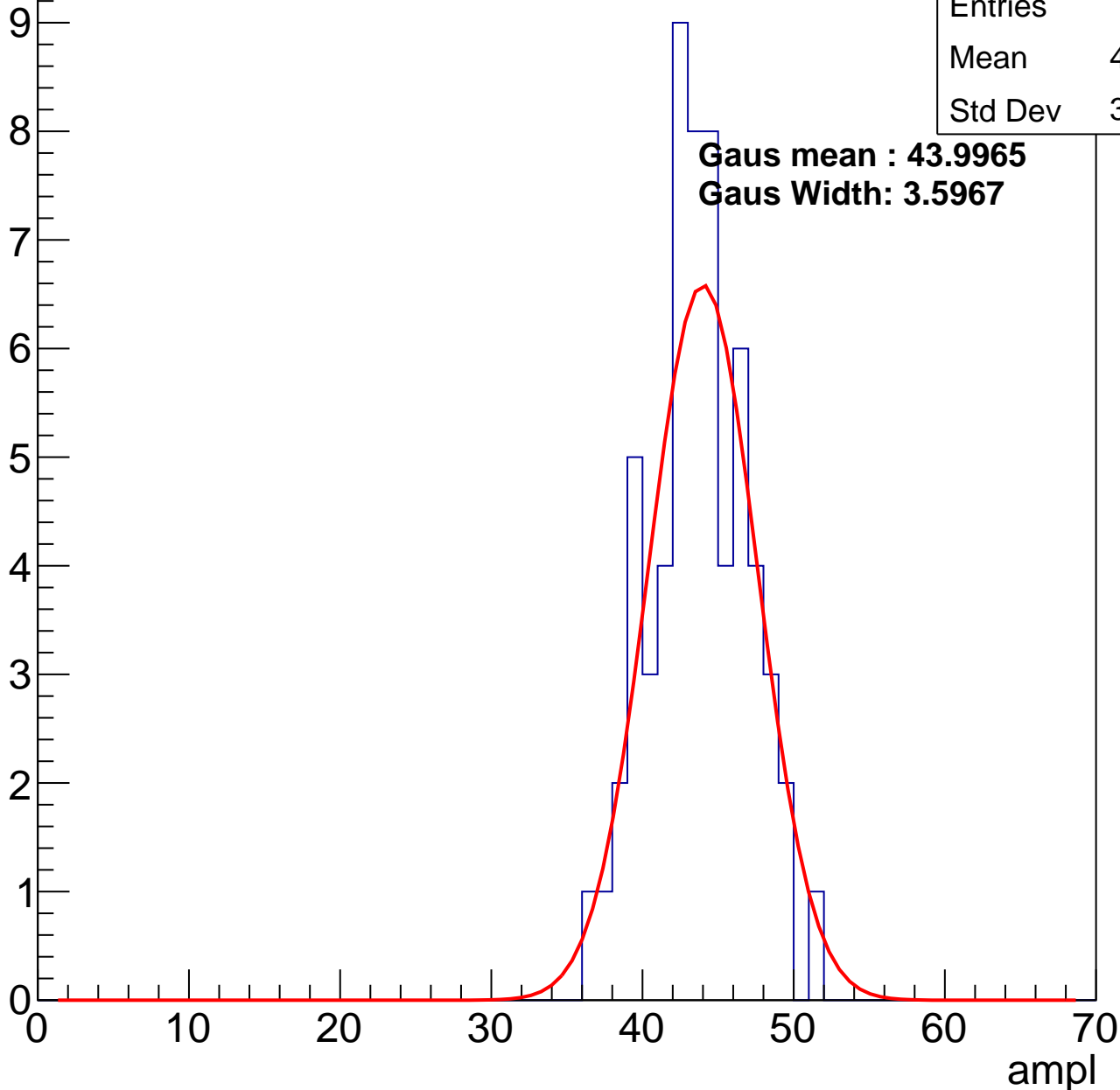
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	61
Mean	43.26
Std Dev	3.177

**Gaus mean : 43.9965**

**Gaus Width: 3.5967**

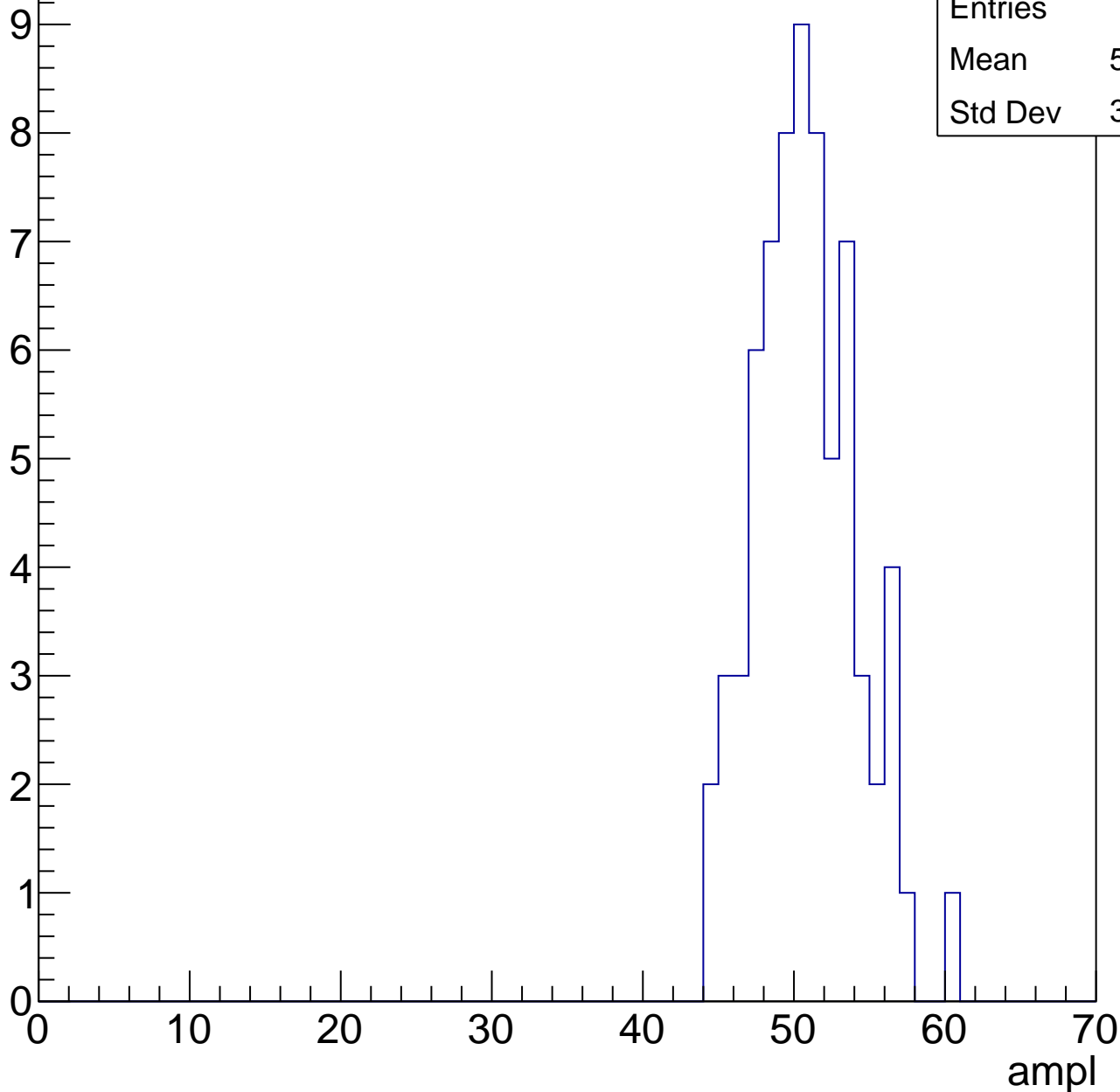


# B1L103S, U9-ch59, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	69
Mean	50.33
Std Dev	3.317

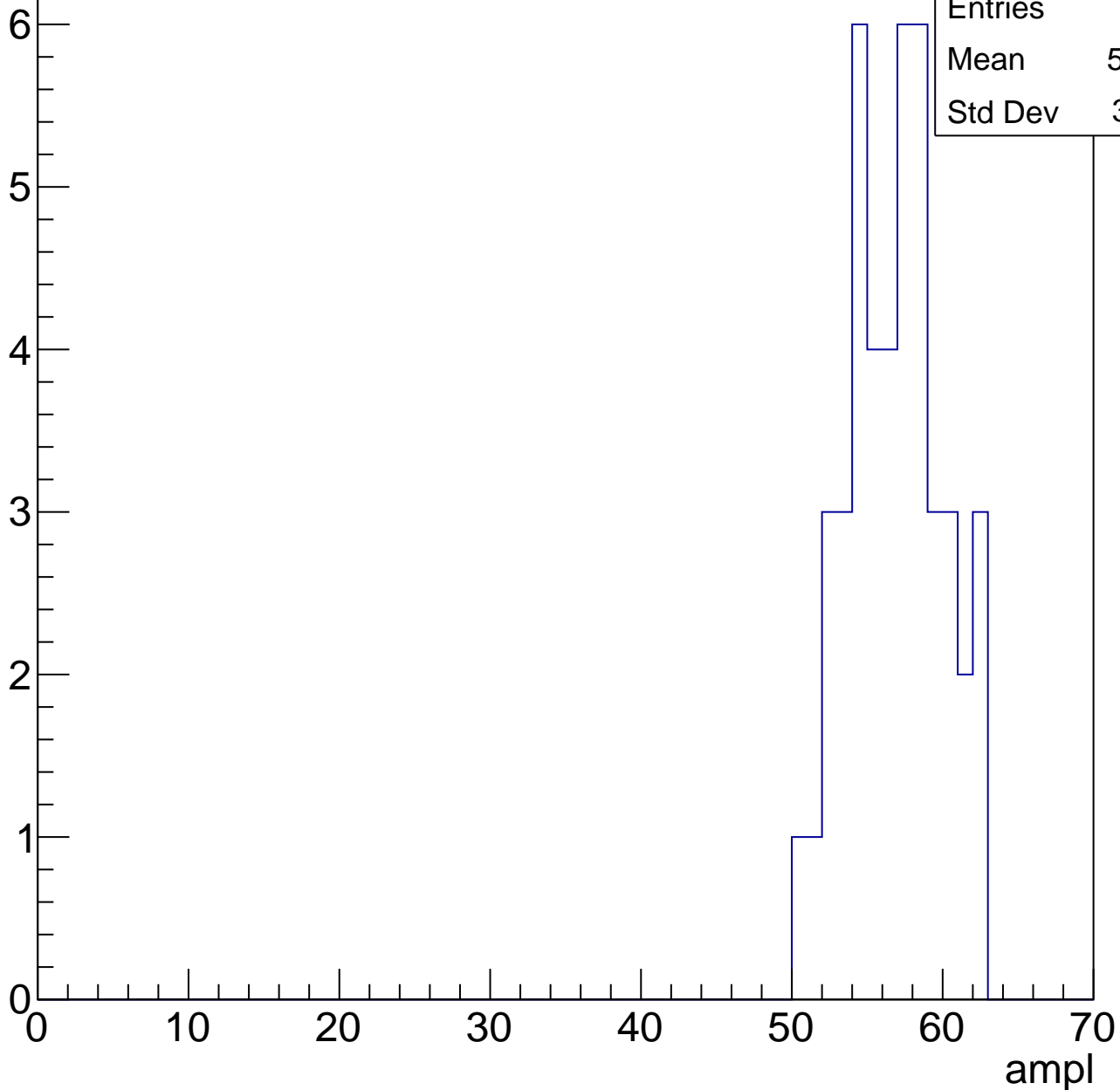


# B1L103S, U9-ch59, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	45
Mean	56.42
Std Dev	3.051

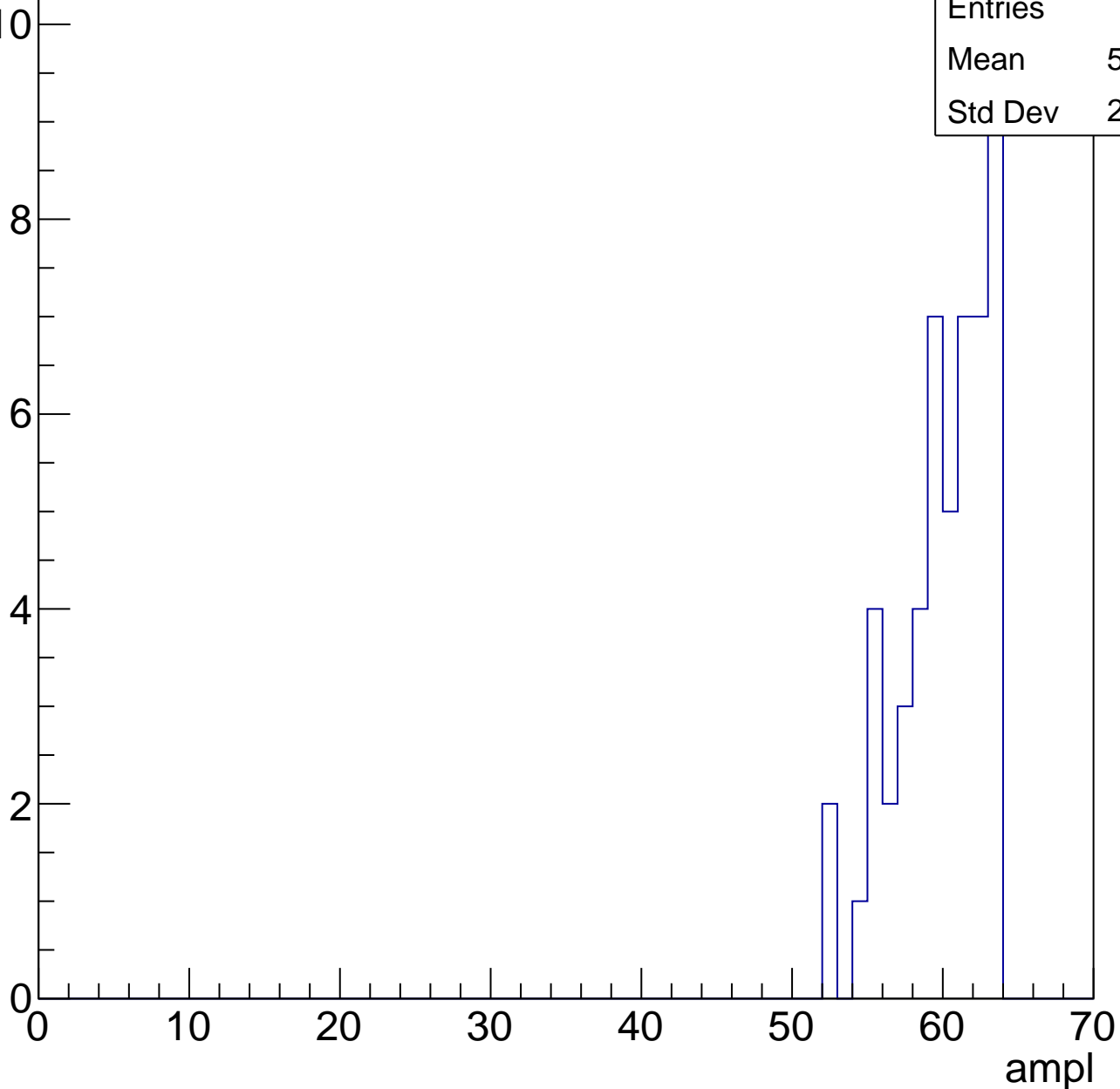


# B1L103S, U9-ch59, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

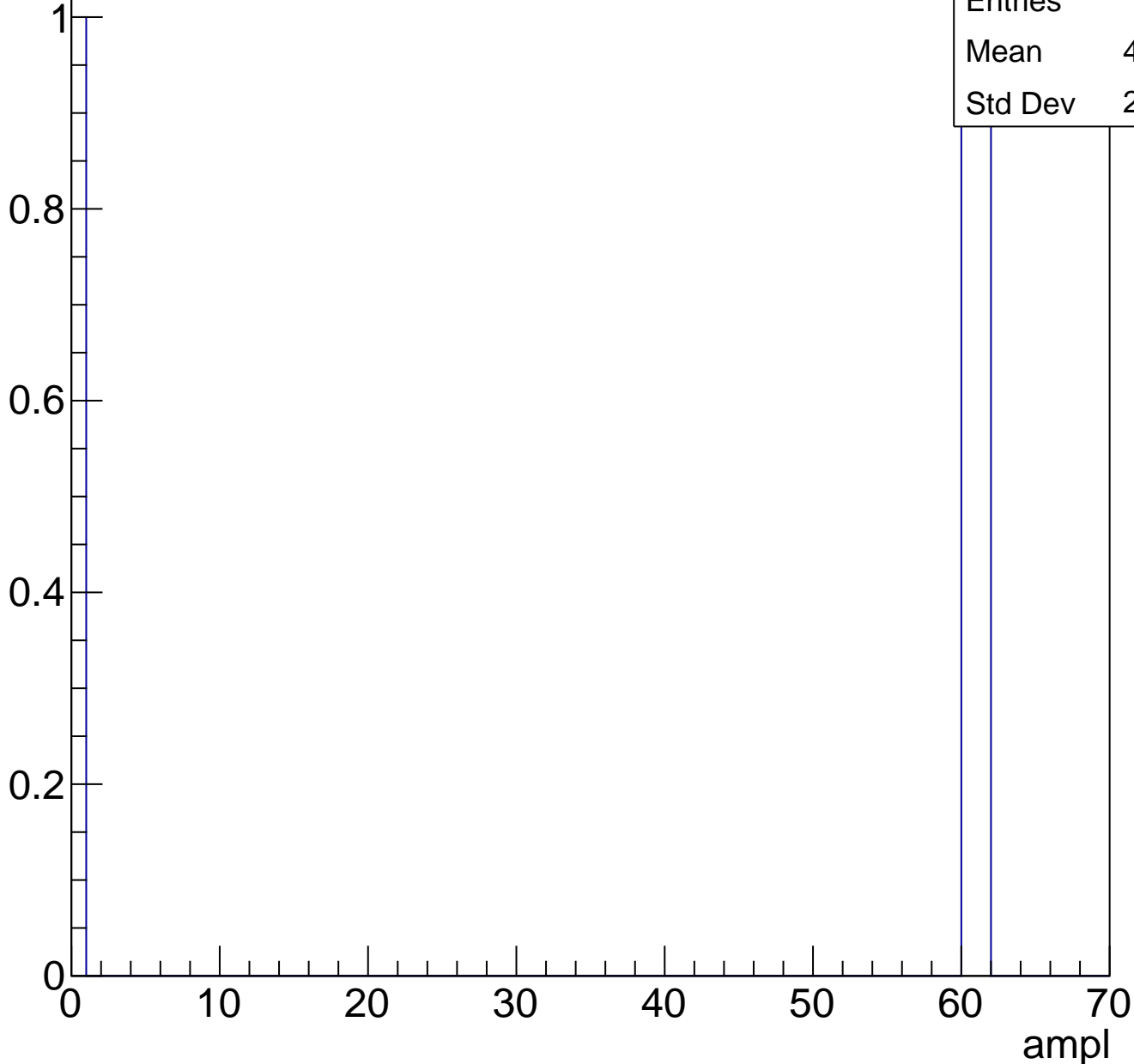
Entries	52
Mean	59.56
Std Dev	2.977



# B1L103S, U9-ch59, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U9-ch59, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U9-ch60, adc0

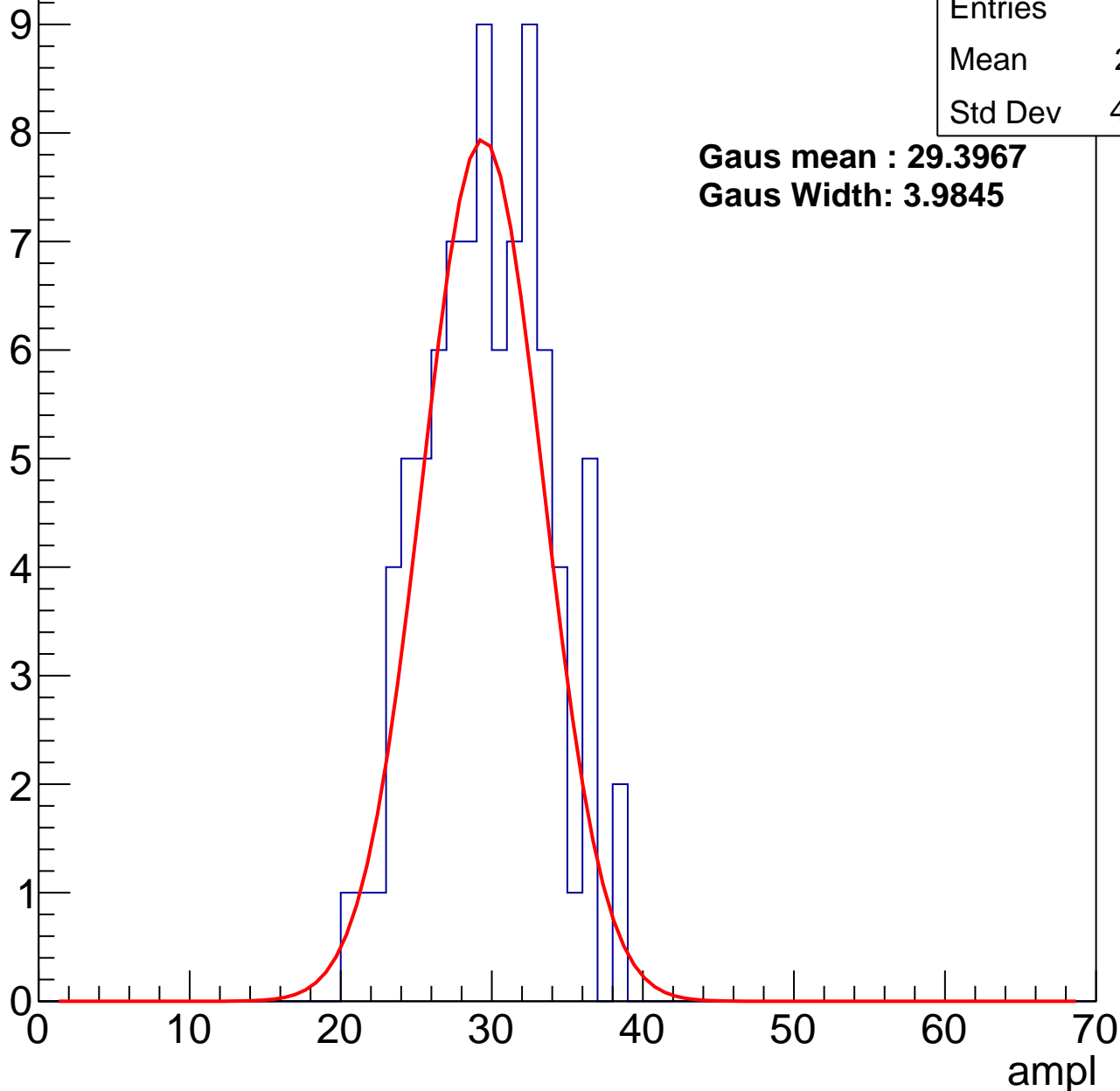
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	86
Mean	29.21
Std Dev	4.009

**Gaus mean : 29.3967**

**Gaus Width: 3.9845**



# B1L103S, U9-ch60, adc1

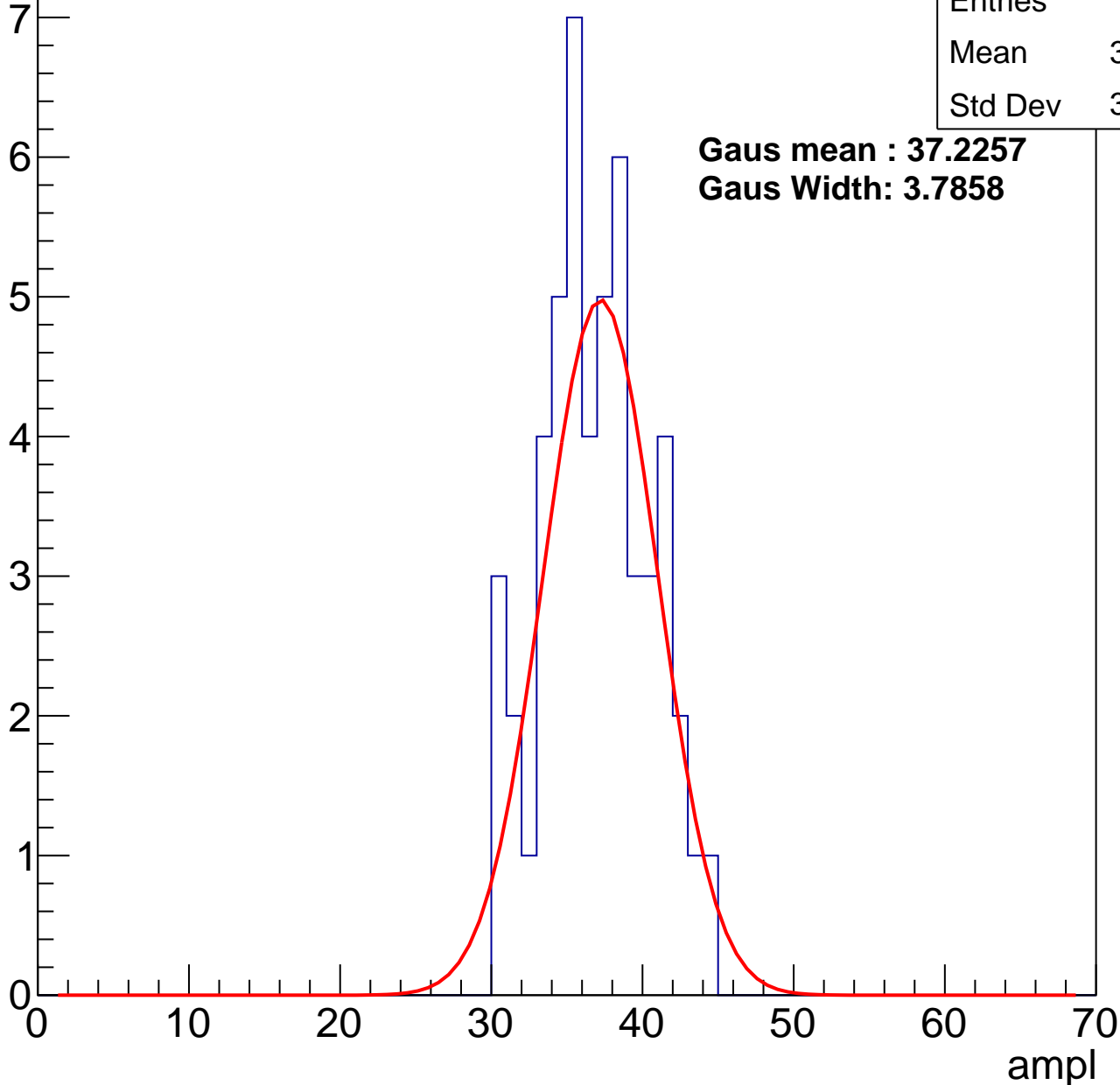
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	51
Mean	36.47
Std Dev	3.472

**Gaus mean : 37.2257**

**Gaus Width: 3.7858**



# B1L103S, U9-ch60, adc2

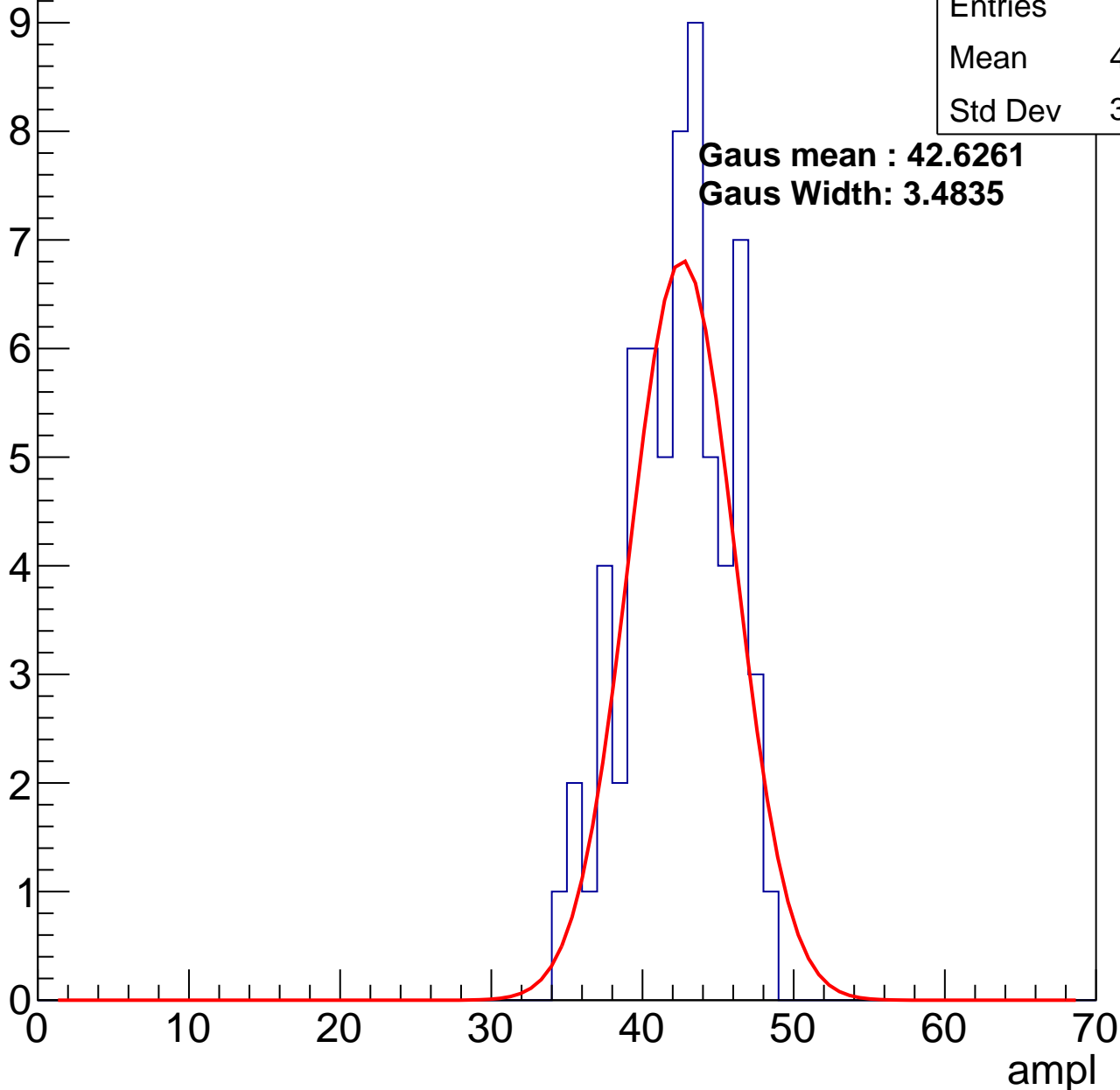
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	41.83
Std Dev	3.305

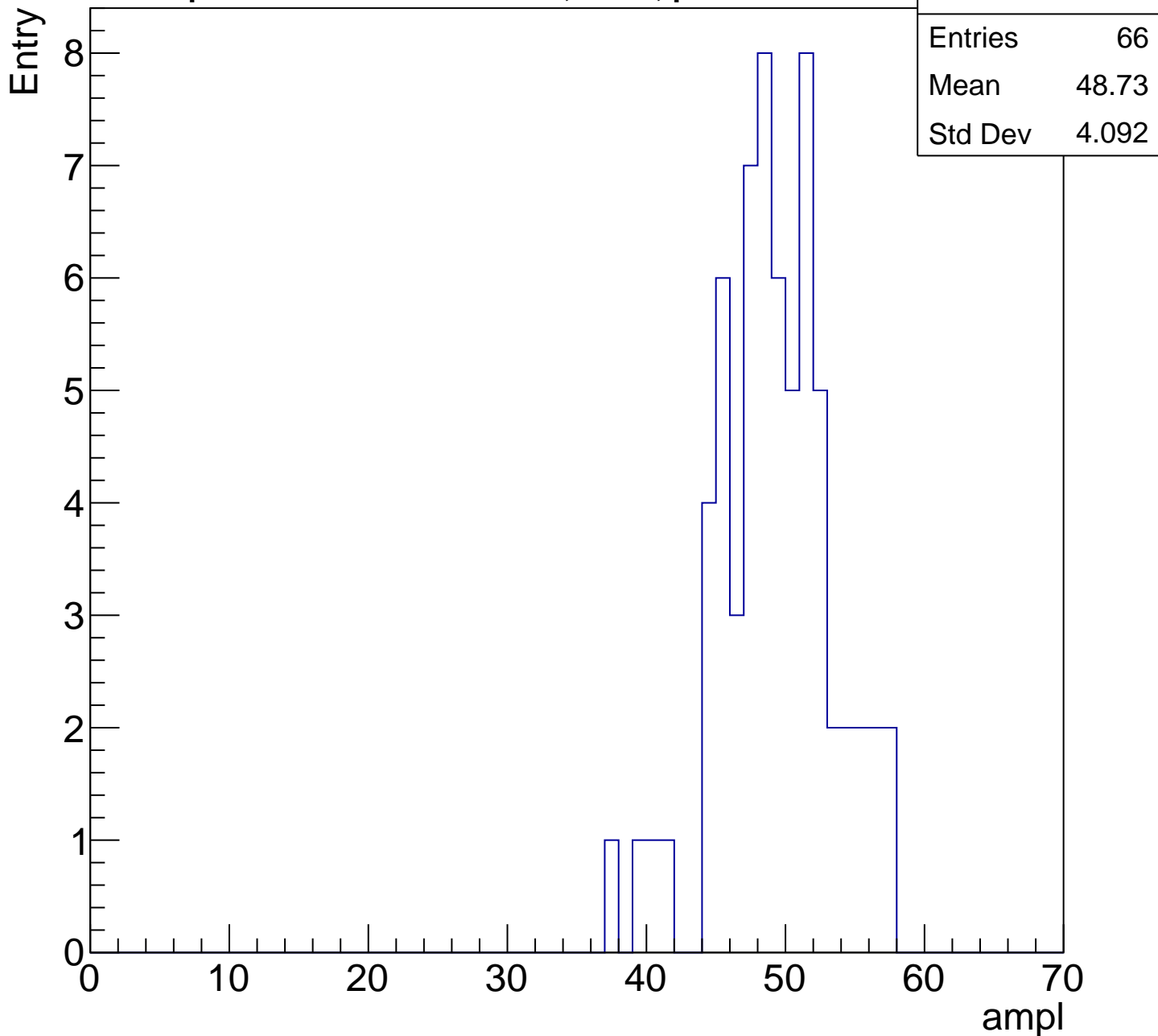
**Gaus mean : 42.6261**

**Gaus Width: 3.4835**



# B1L103S, U9-ch60, adc3

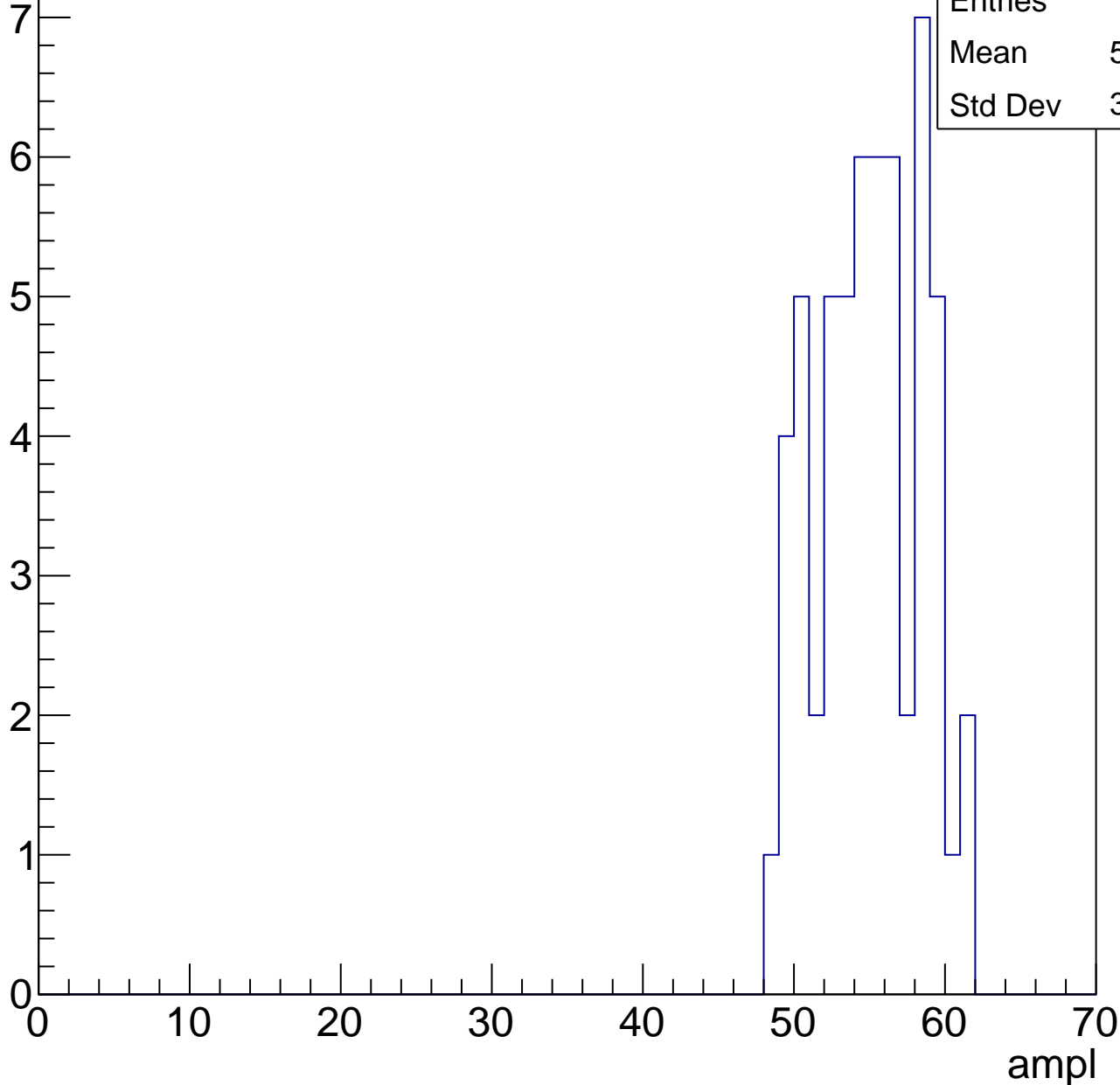
calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U9-ch60, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

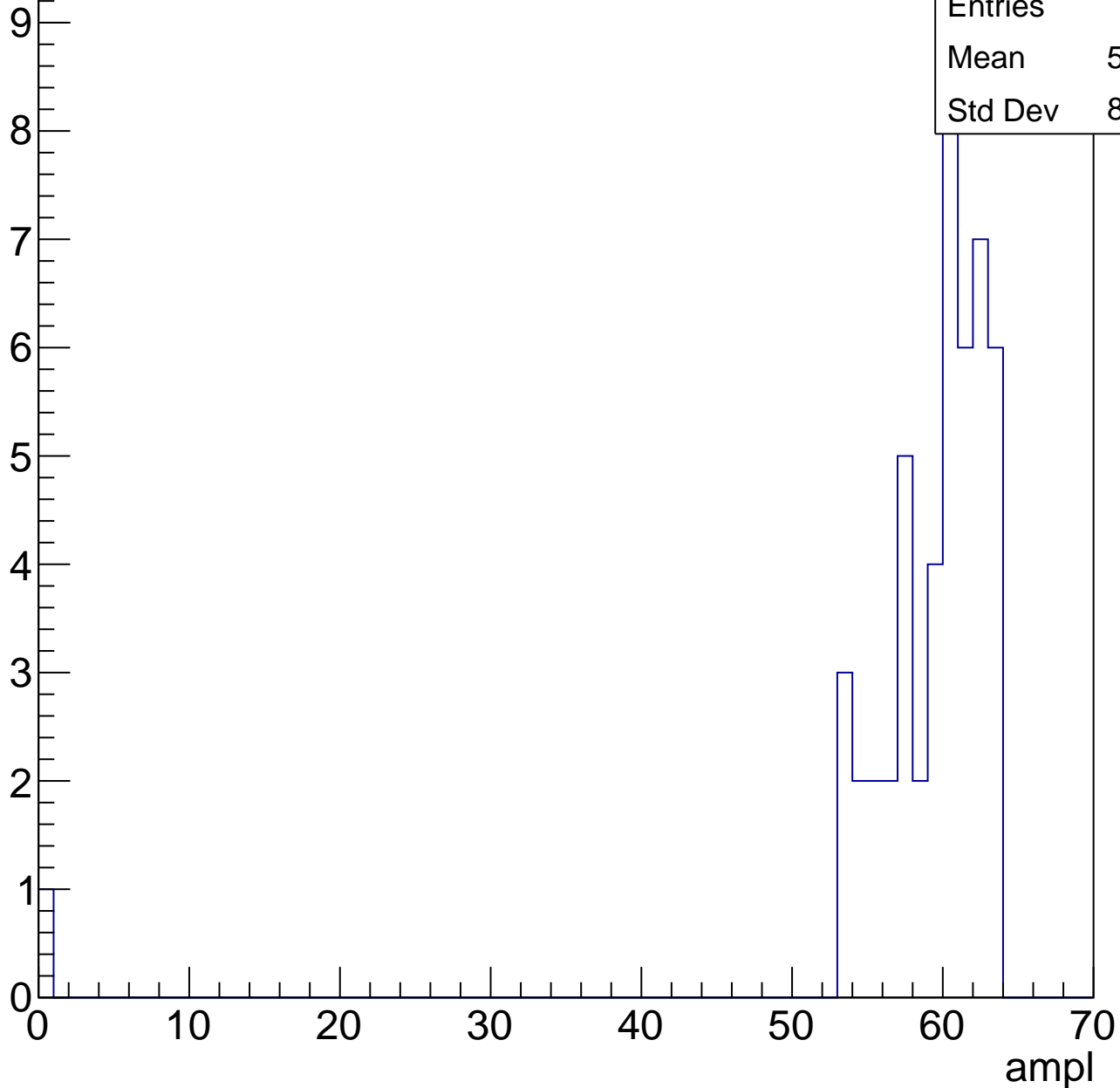


Entries	57
Mean	54.53
Std Dev	3.408

# B1L103S, U9-ch60, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

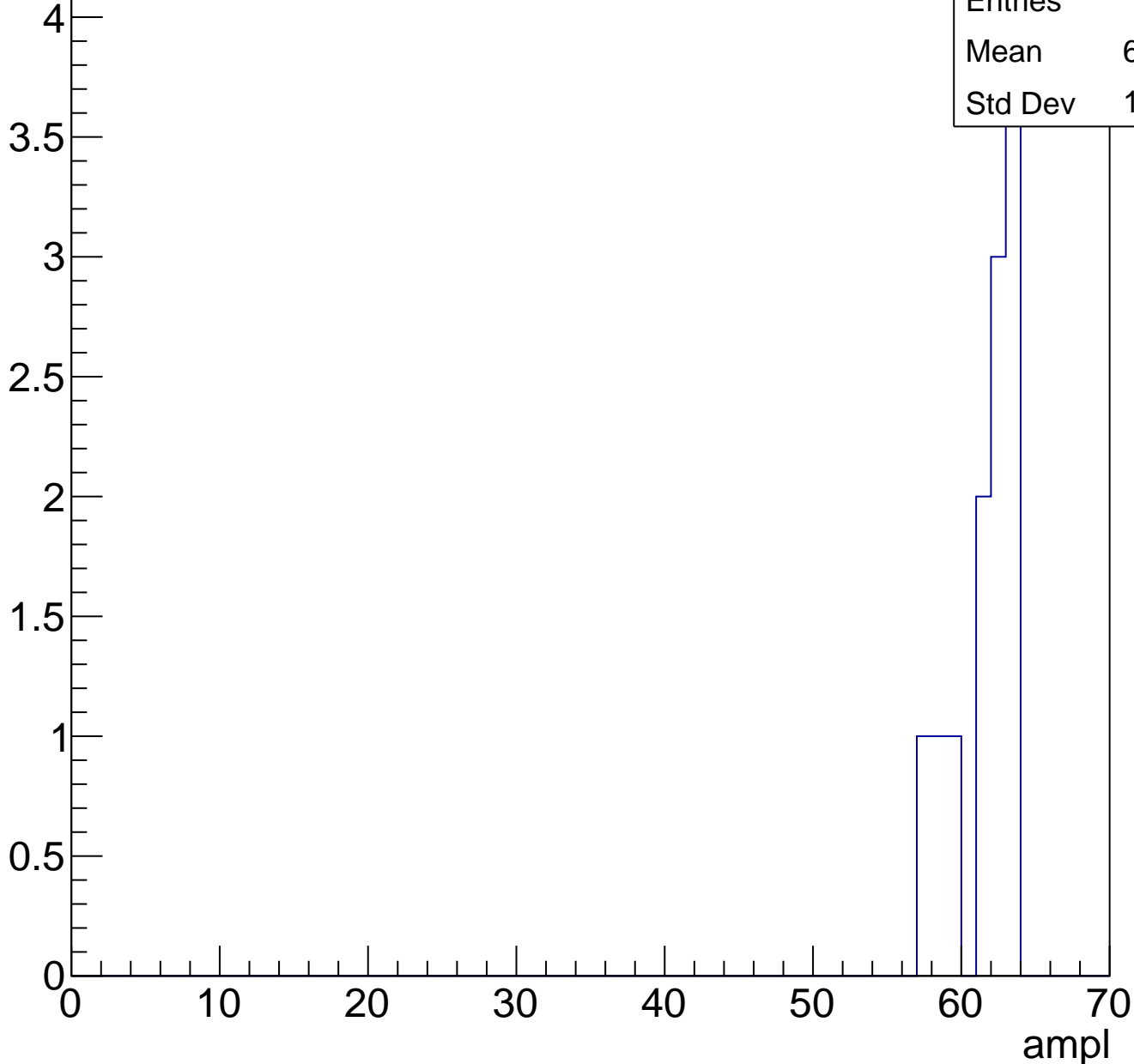
Entry



# B1L103S, U9-ch60, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

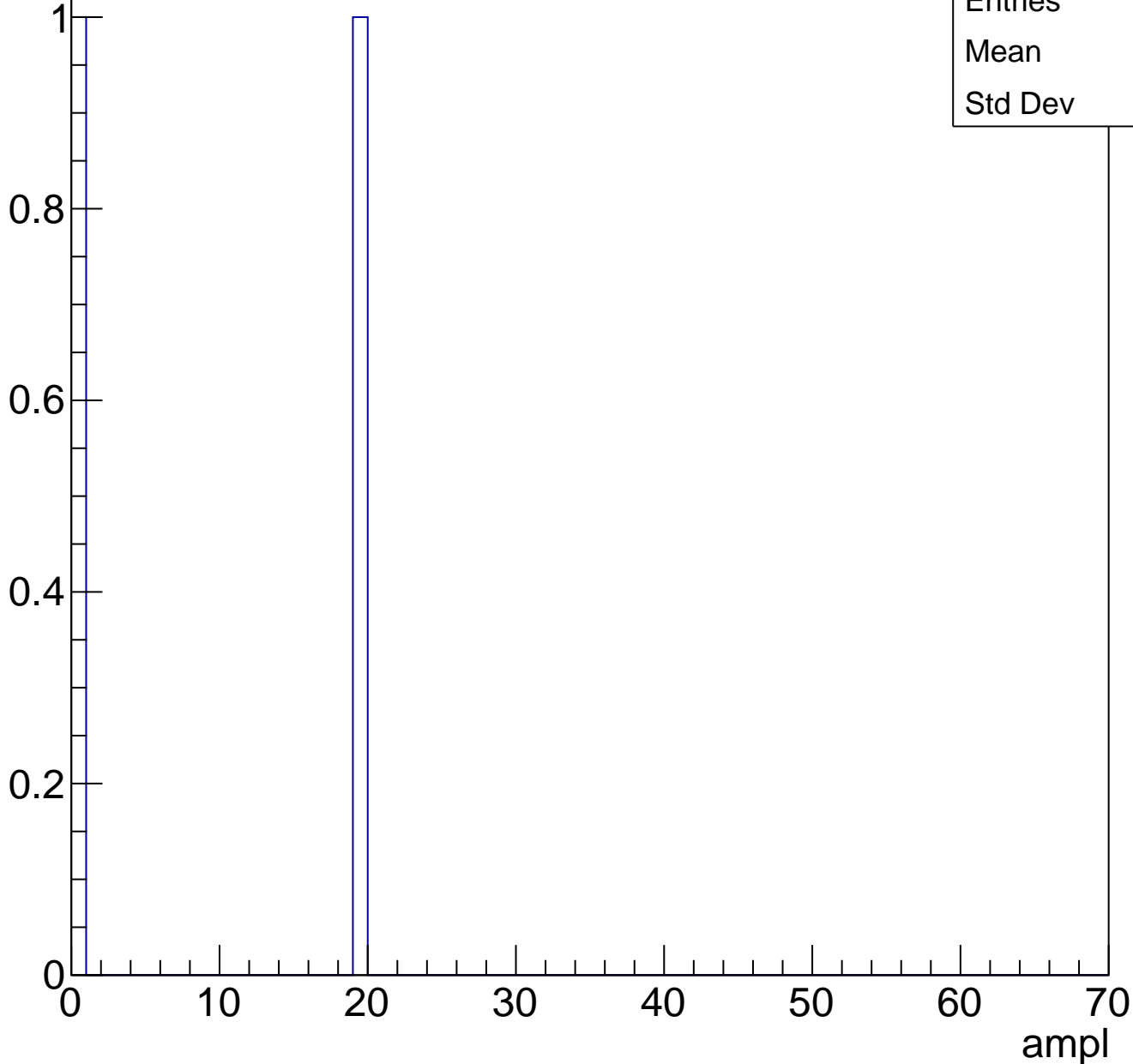




# B1L103S, U9-ch60, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U9-ch61, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	75
Mean	29.47
Std Dev	6.03

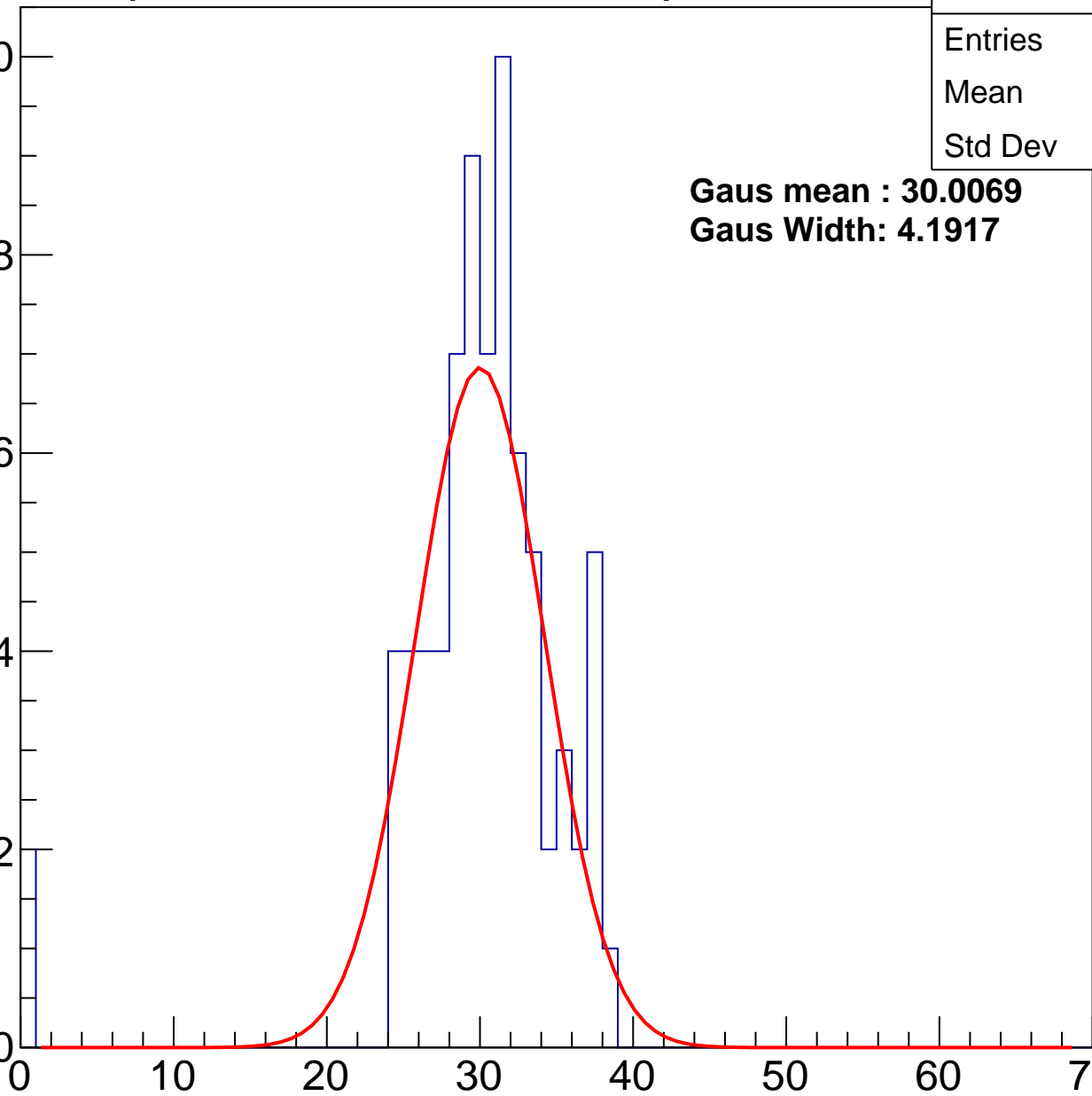
**Gaus mean : 30.0069**

**Gaus Width: 4.1917**

Entry

10  
8  
6  
4  
2  
0

ampl



# B1L103S, U9-ch61, adc1

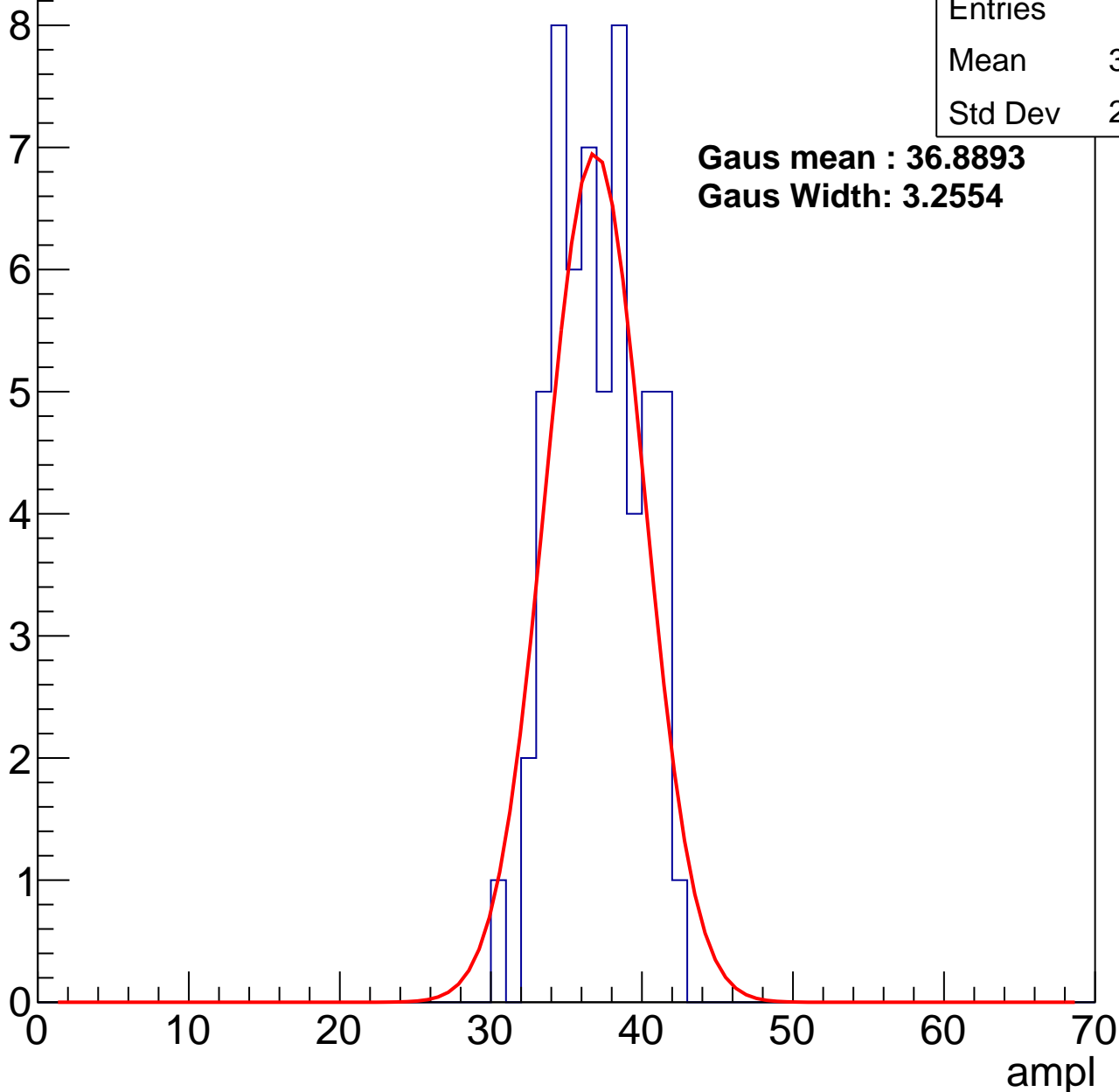
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	57
Mean	36.58
Std Dev	2.797

**Gaus mean : 36.8893**

**Gaus Width: 3.2554**



# B1L103S, U9-ch61, adc2

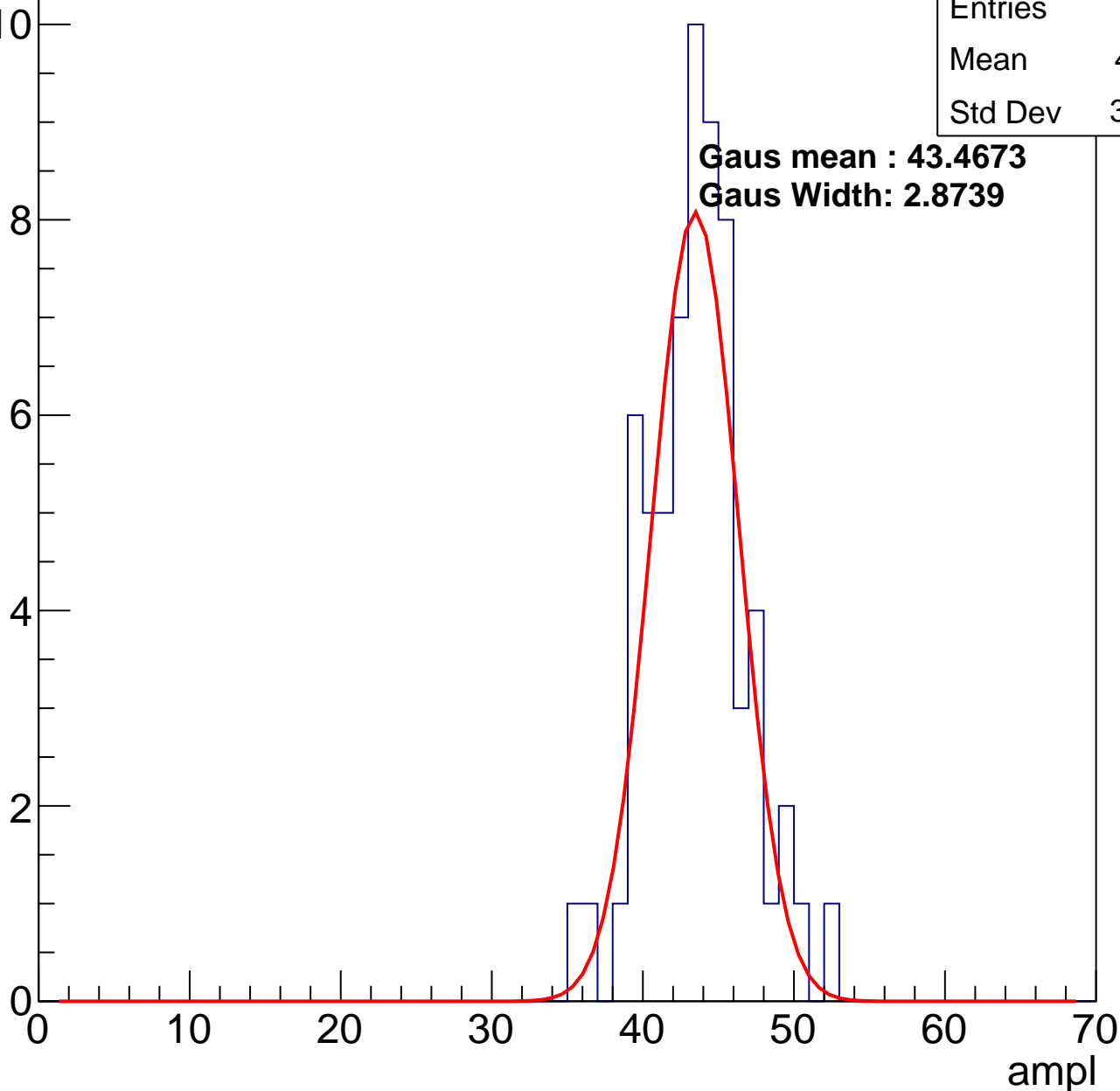
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	43.11
Std Dev	3.197

**Gaus mean : 43.4673**

**Gaus Width: 2.8739**



# B1L103S, U9-ch61, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	68
Mean	49.4
Std Dev	2.966

Entry

10

8

6

4

2

0

0

10

20

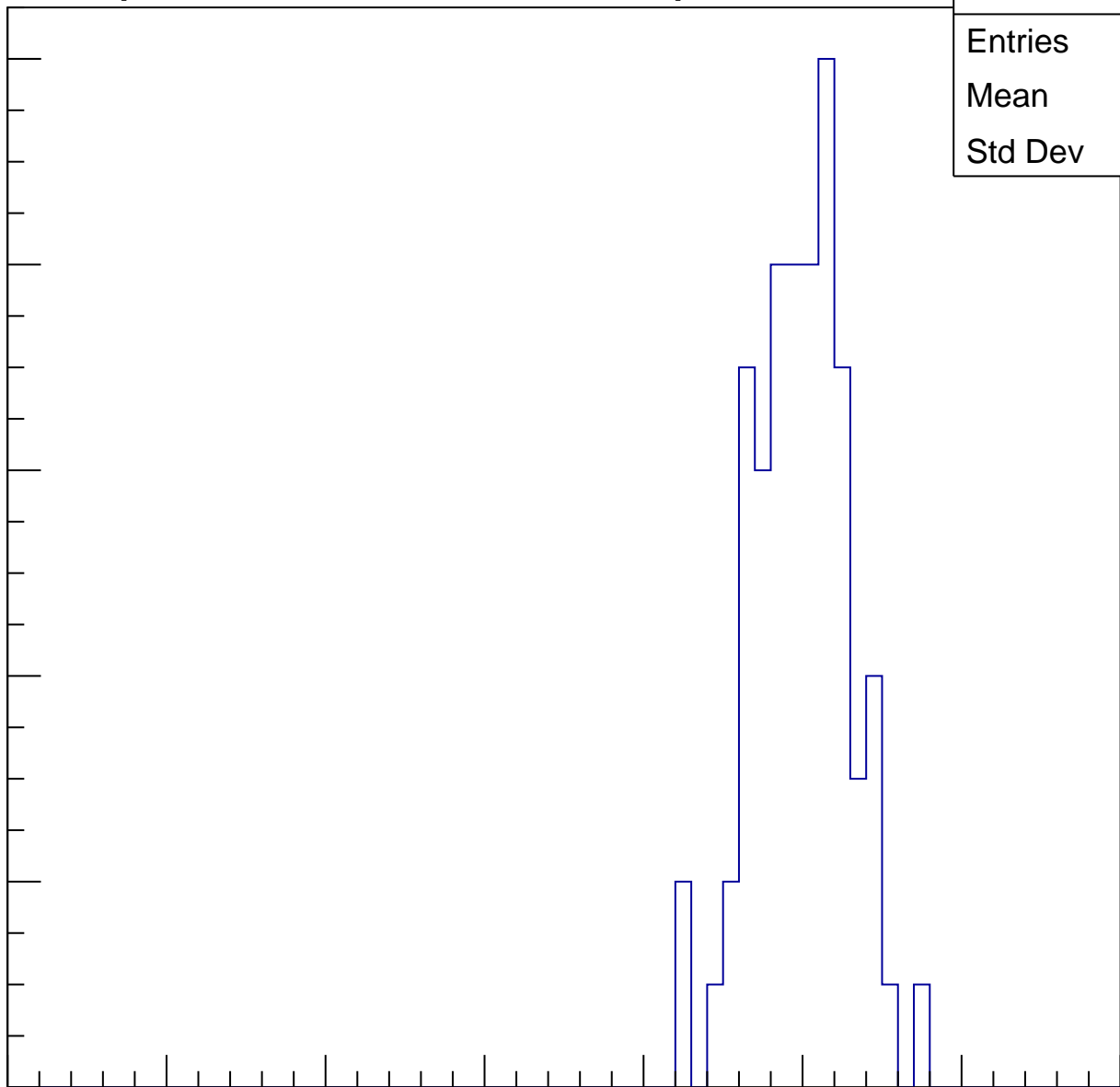
30

40

50

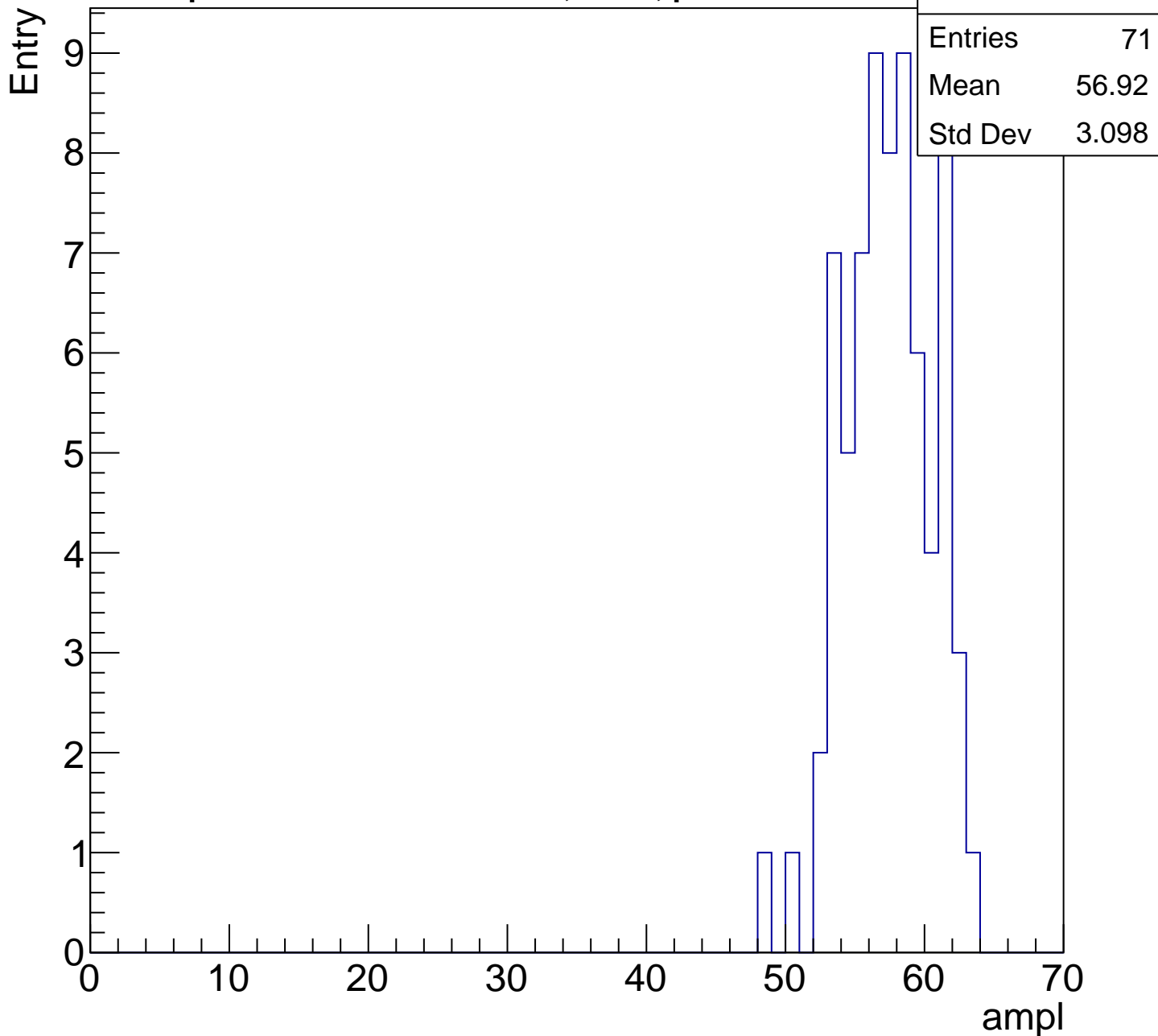
60

ampl



# B1L103S, U9-ch61, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

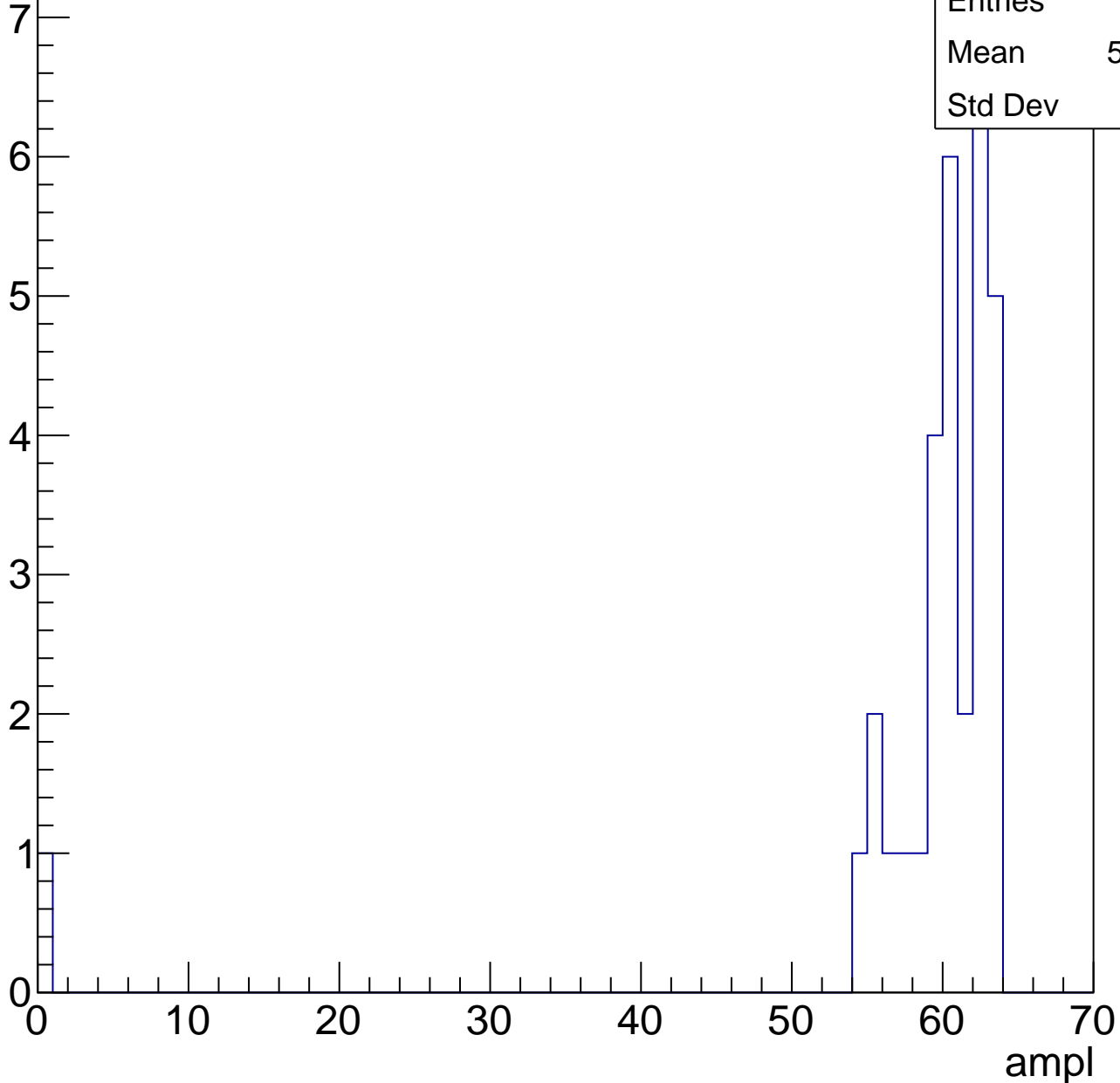


# B1L103S, U9-ch61, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

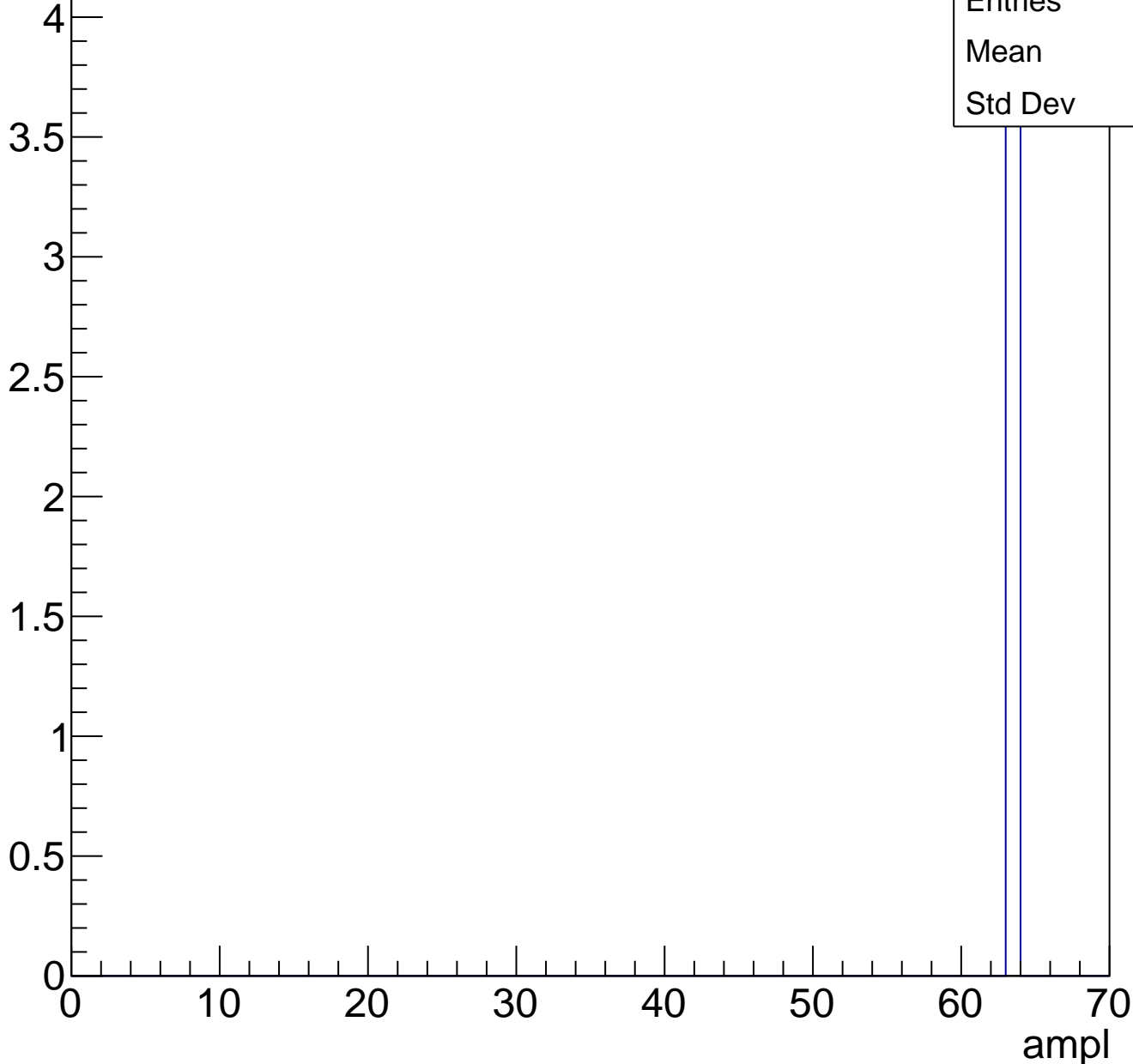
Entries	31
Mean	58.13
Std Dev	10.9



# B1L103S, U9-ch61, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U9-ch61, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U9-ch62, adc0

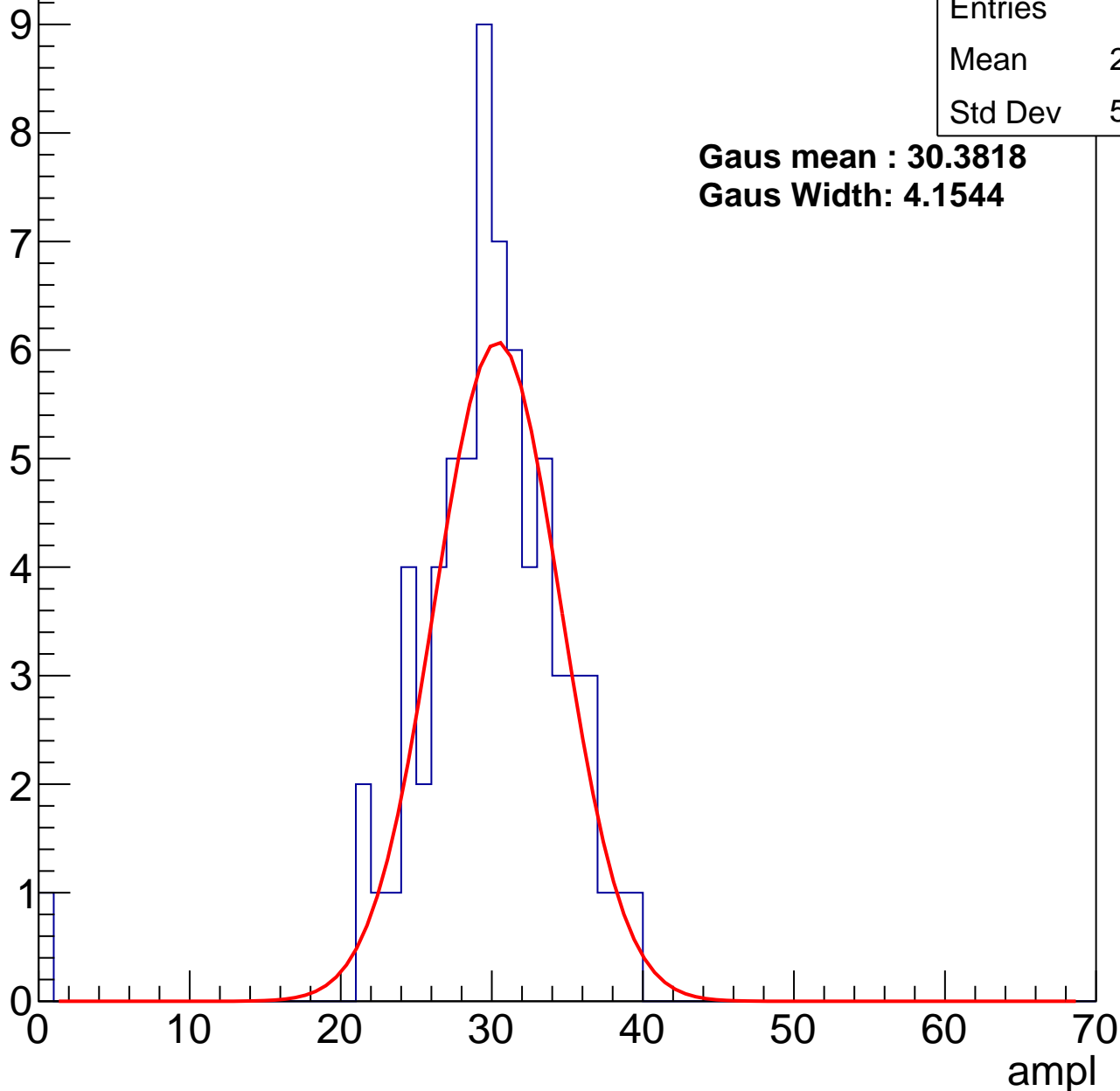
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	68
Mean	29.28
Std Dev	5.374

**Gaus mean : 30.3818**

**Gaus Width: 4.1544**



# B1L103S, U9-ch62, adc1

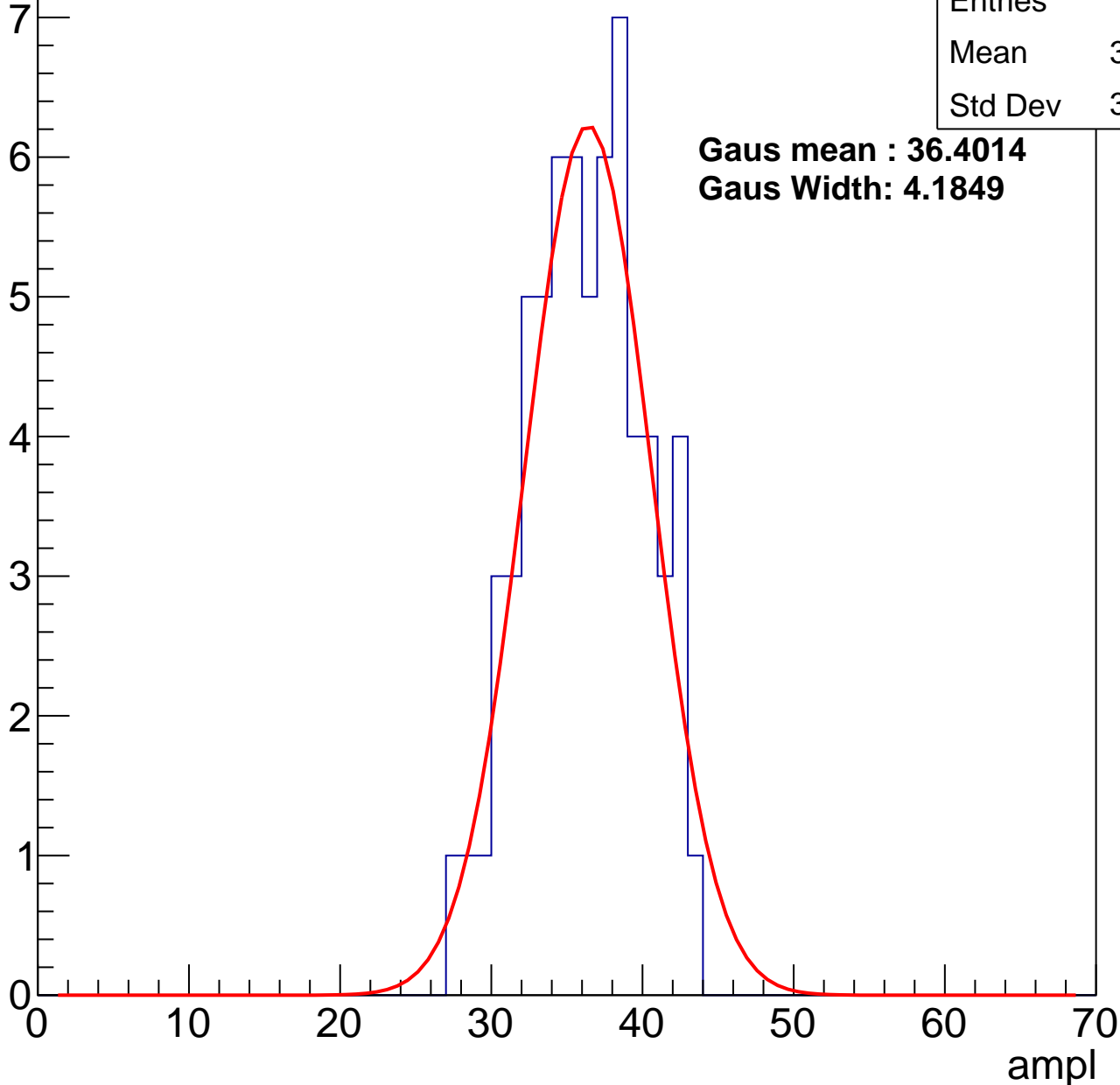
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	35.75
Std Dev	3.783

**Gaus mean : 36.4014**

**Gaus Width: 4.1849**



# B1L103S, U9-ch62, adc2

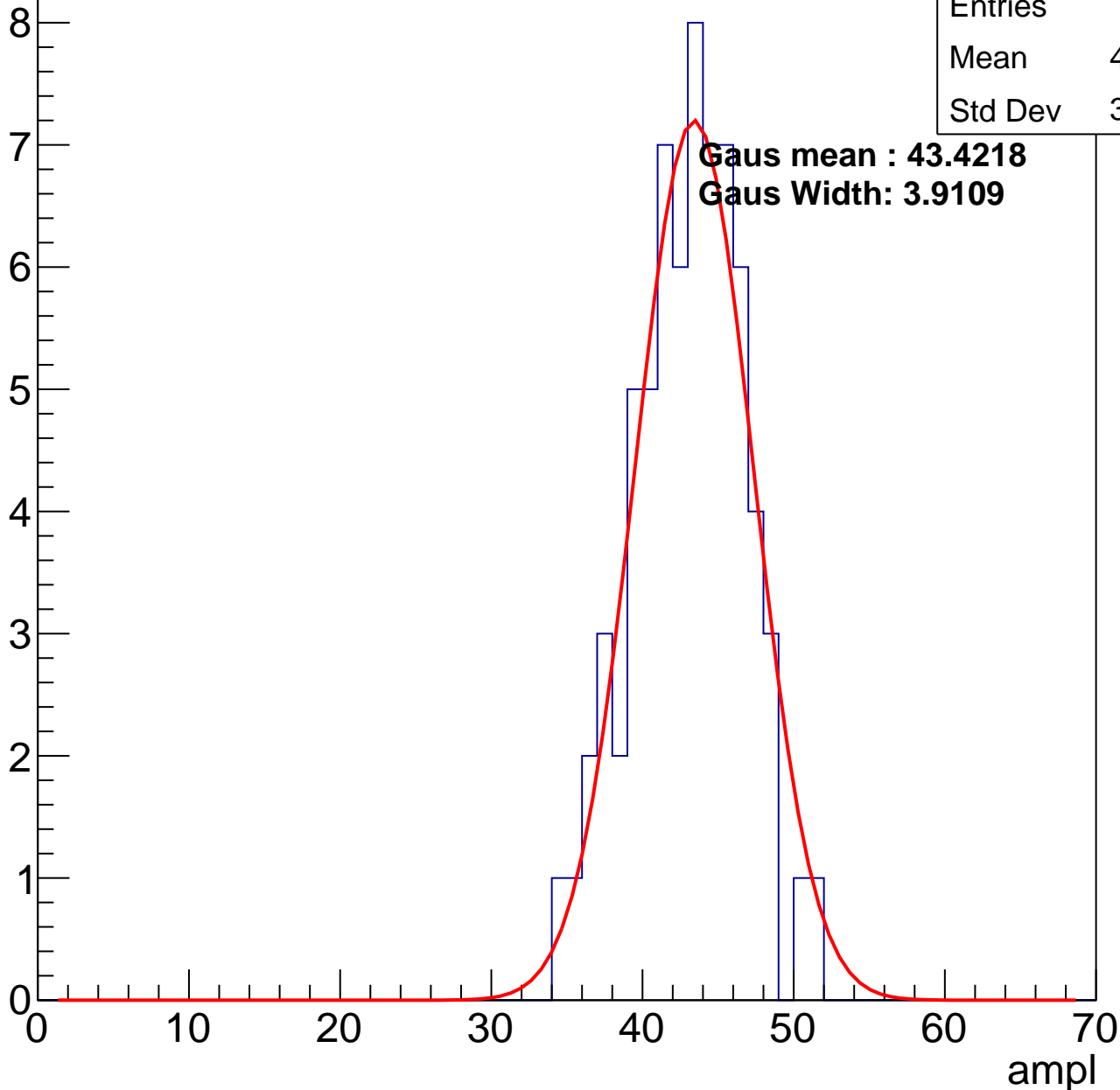
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	69
Mean	42.58
Std Dev	3.589

**Gaus mean : 43.4218**

**Gaus Width: 3.9109**

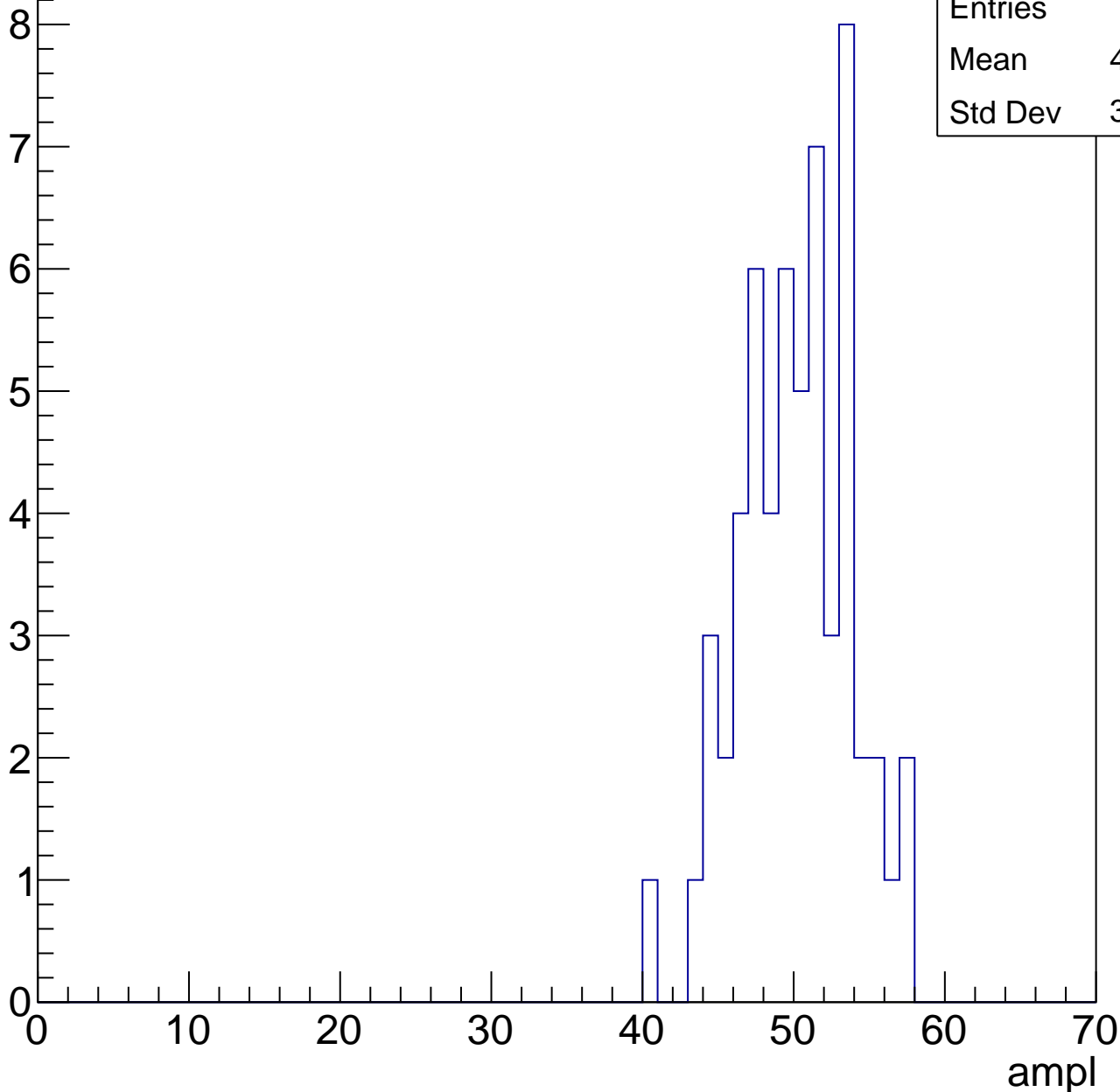


# B1L103S, U9-ch62, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

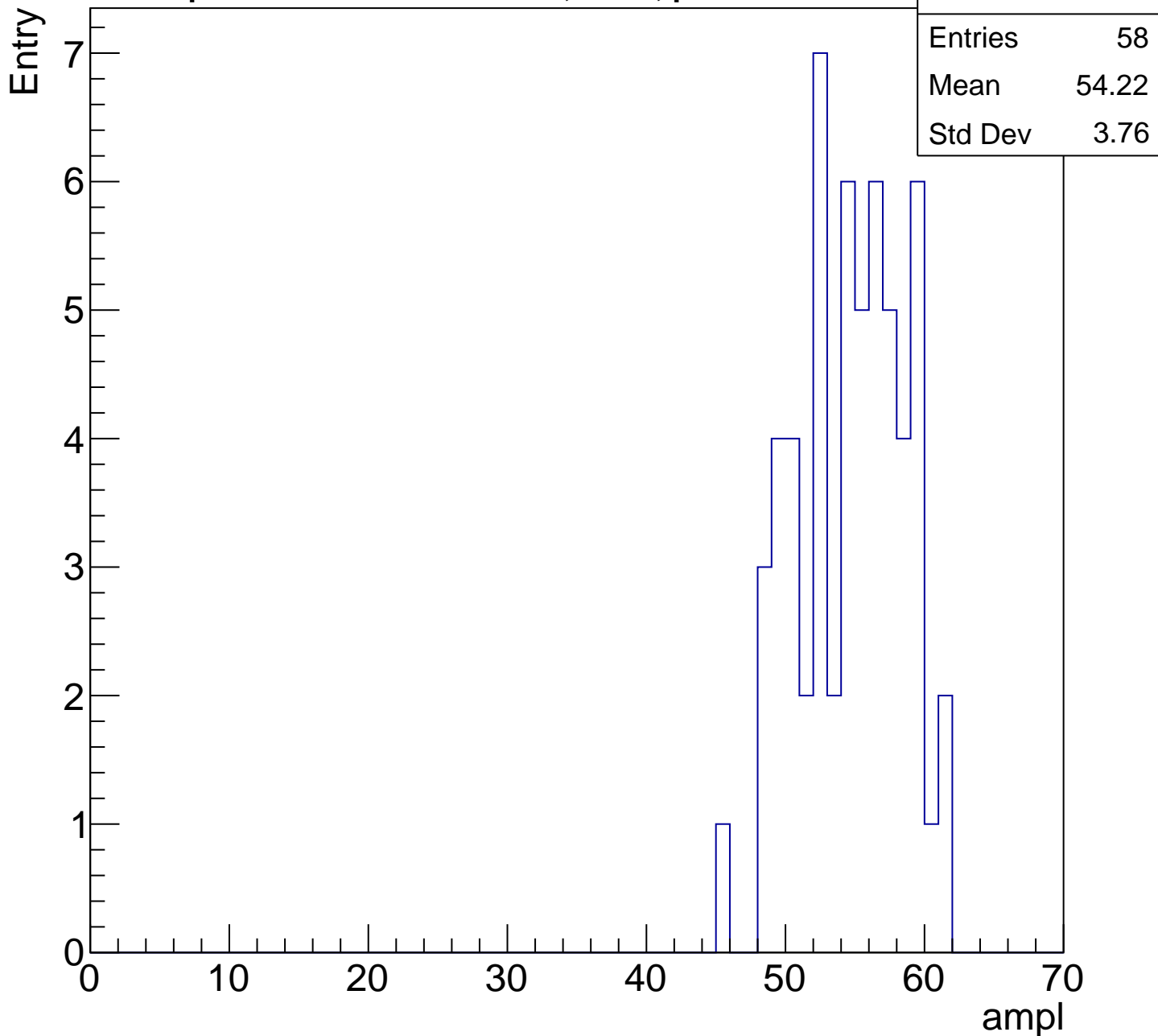
Entry

Entries	57
Mean	49.68
Std Dev	3.623



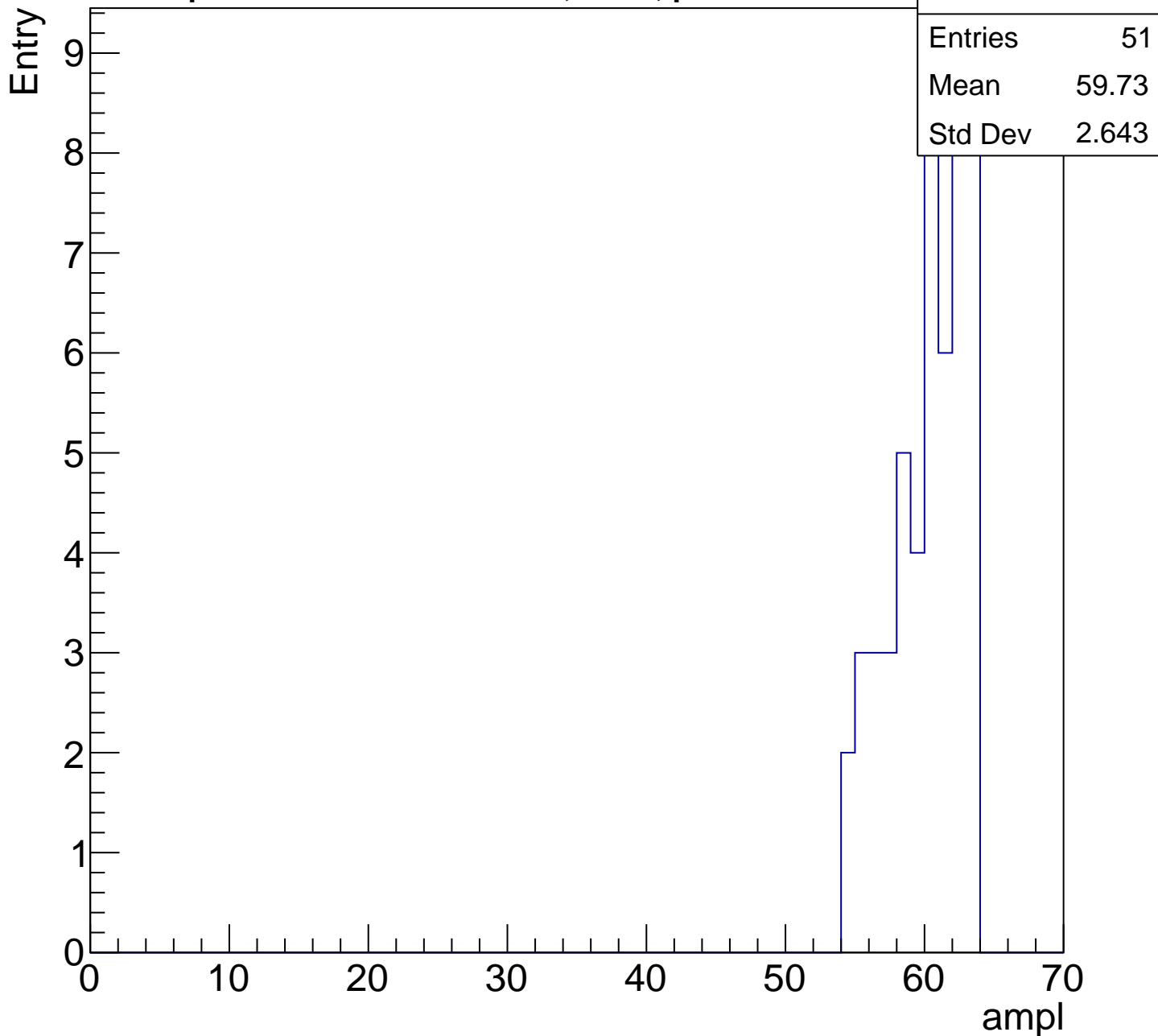
# B1L103S, U9-ch62, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U9-ch62, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U9-ch62, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

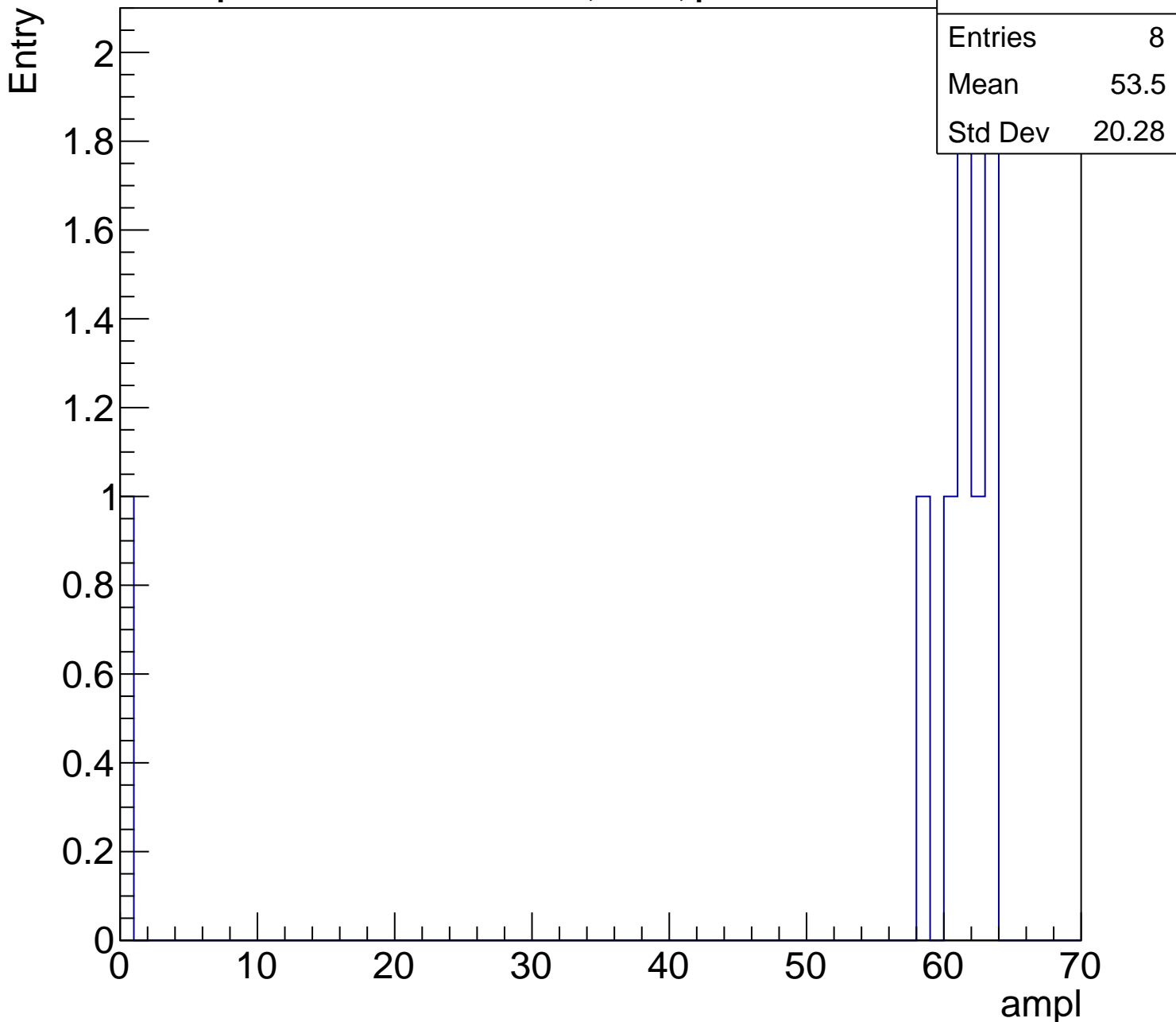
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	8
Mean	53.5
Std Dev	20.28

0 10 20 30 40 50 60 70

ampl





# B1L103S, U9-ch62, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U9-ch63, adc0

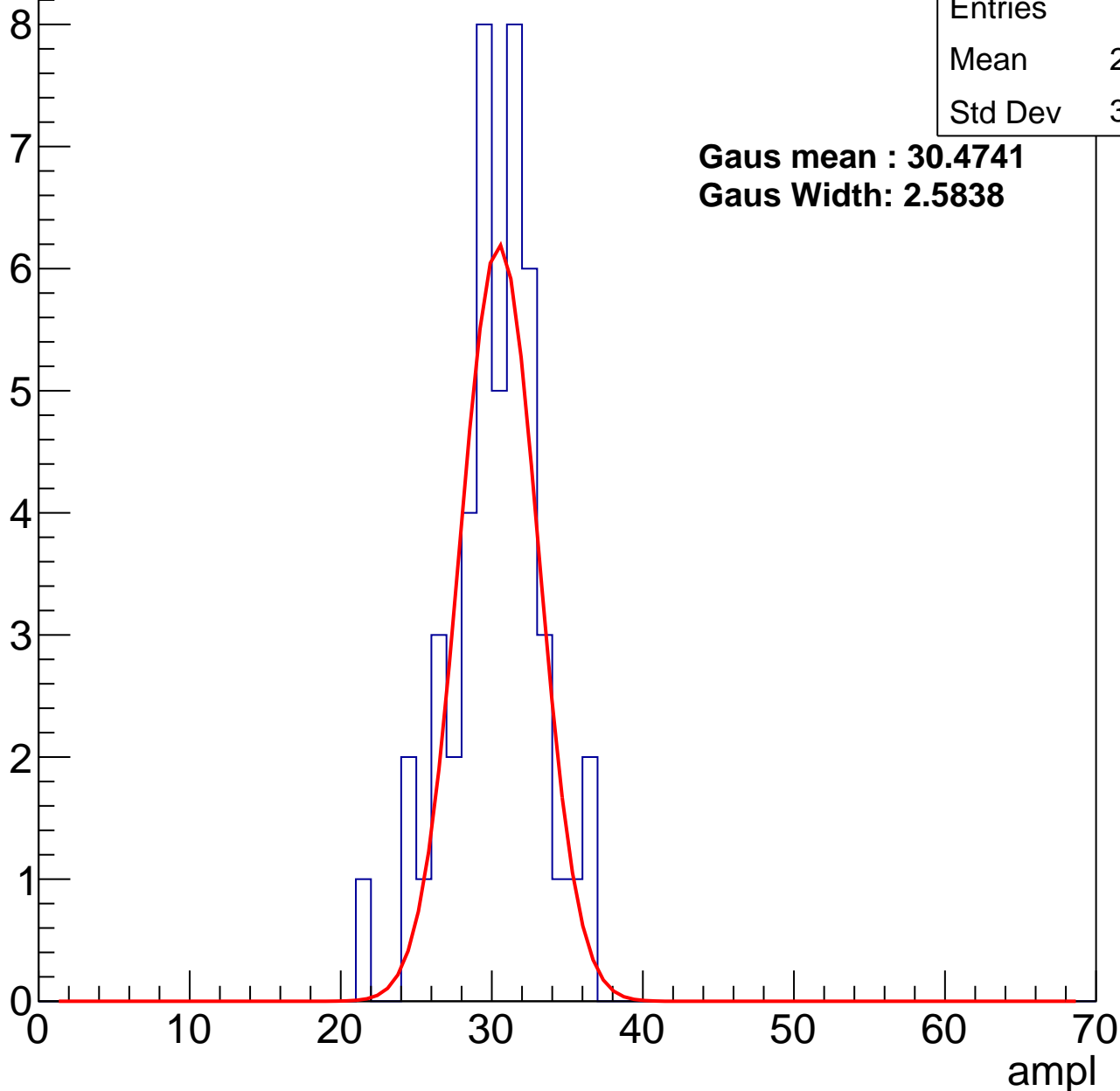
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	47
Mean	29.79
Std Dev	3.052

**Gaus mean : 30.4741**

**Gaus Width: 2.5838**



# B1L103S, U9-ch63, adc1

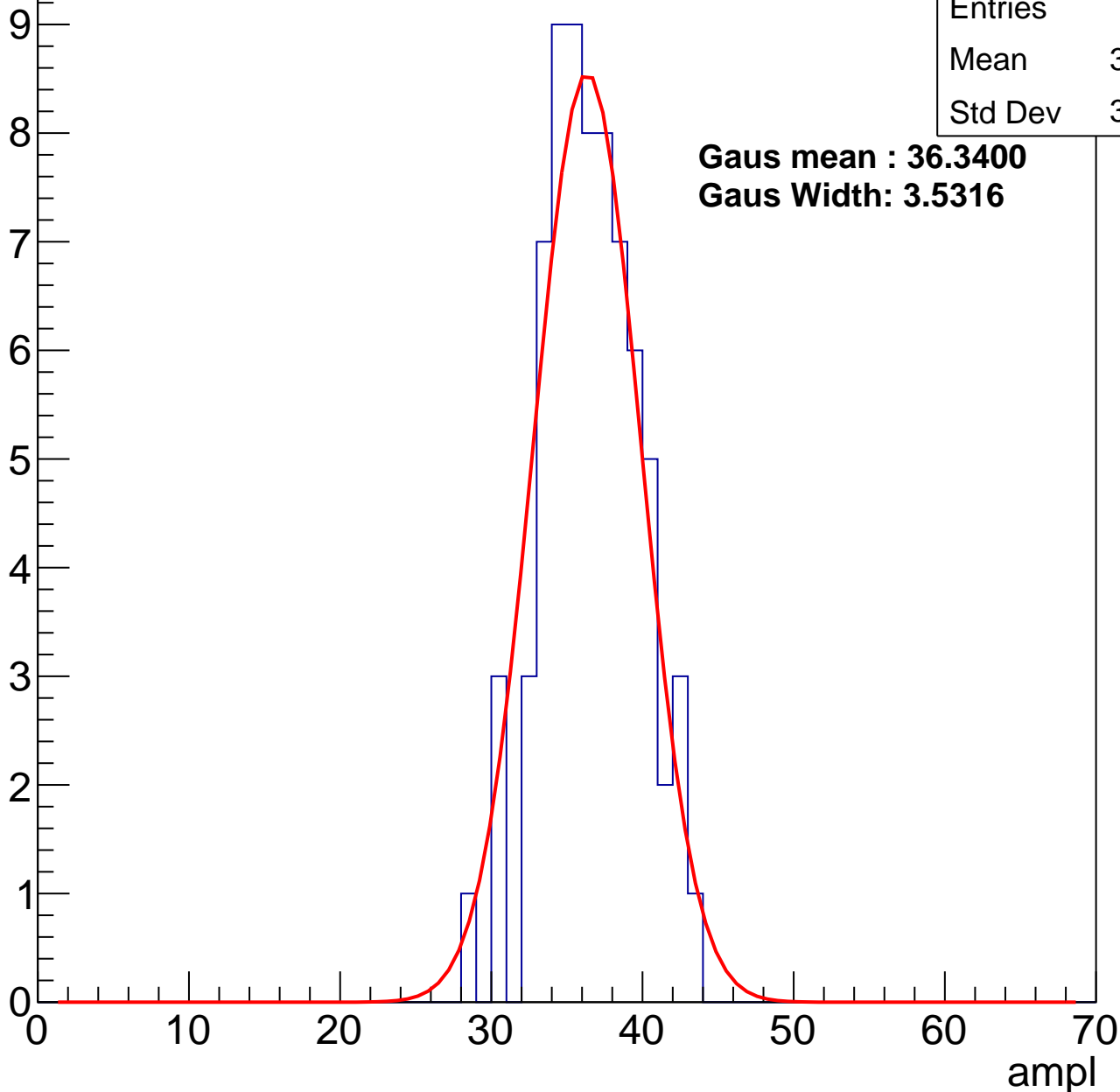
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	72
Mean	36.12
Std Dev	3.127

**Gaus mean : 36.3400**

**Gaus Width: 3.5316**



# B1L103S, U9-ch63, adc2

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	72
Mean	43.38
Std Dev	3.372

**Gaus mean : 42.9652**

**Gaus Width: 2.8875**

10

8

6

4

2

0

0

10

20

30

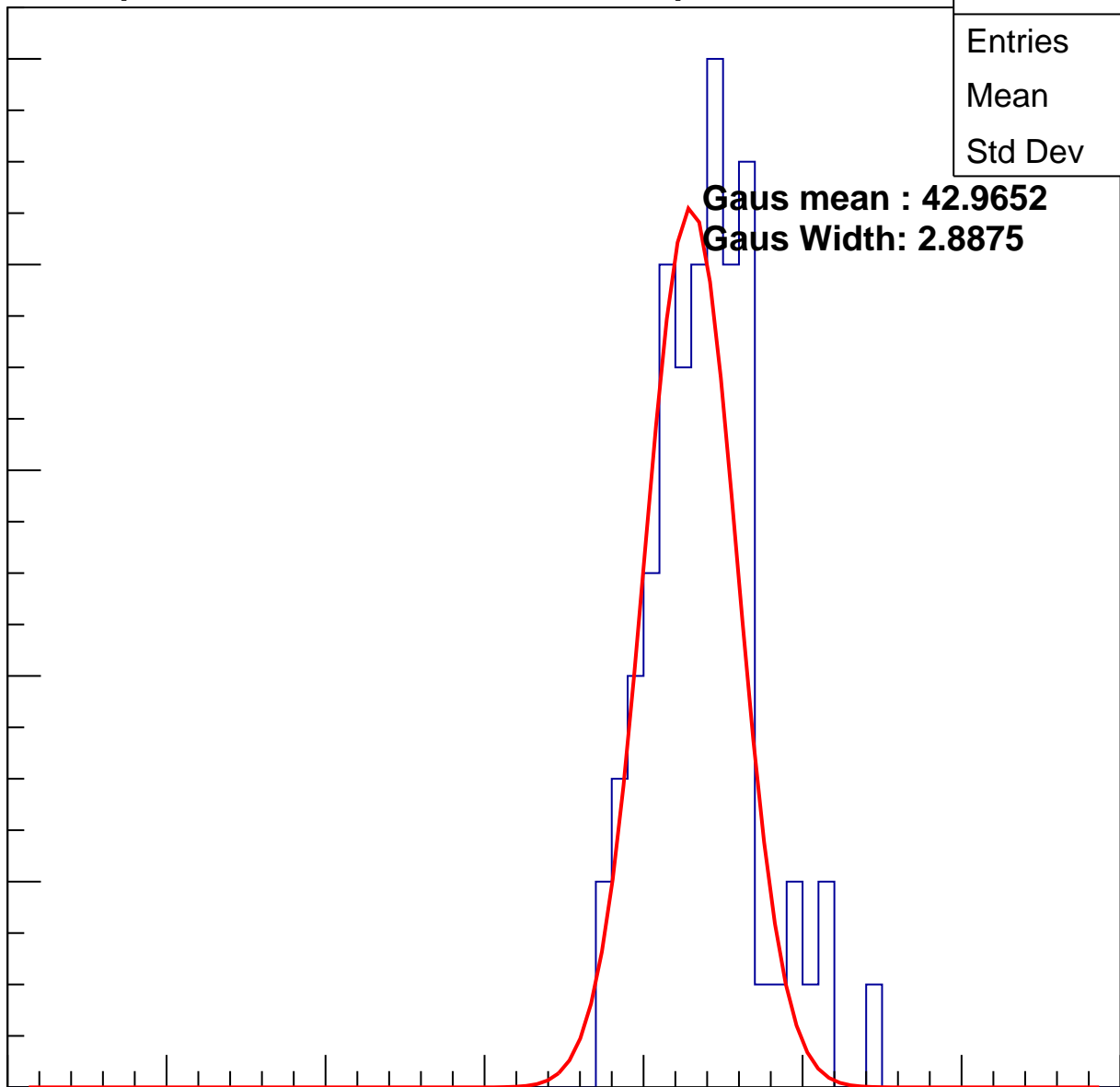
40

50

60

70

ampl

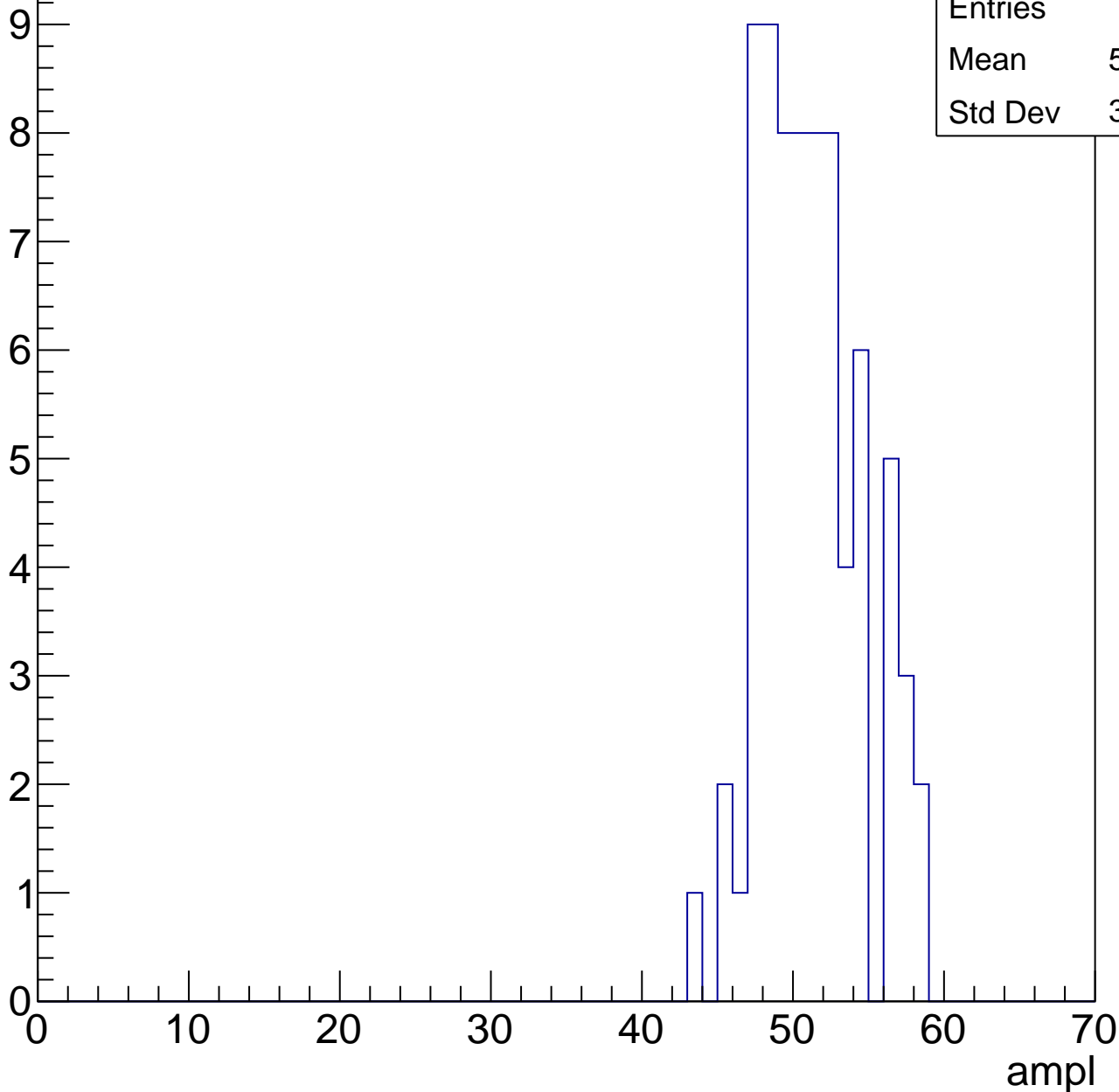


# B1L103S, U9-ch63, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

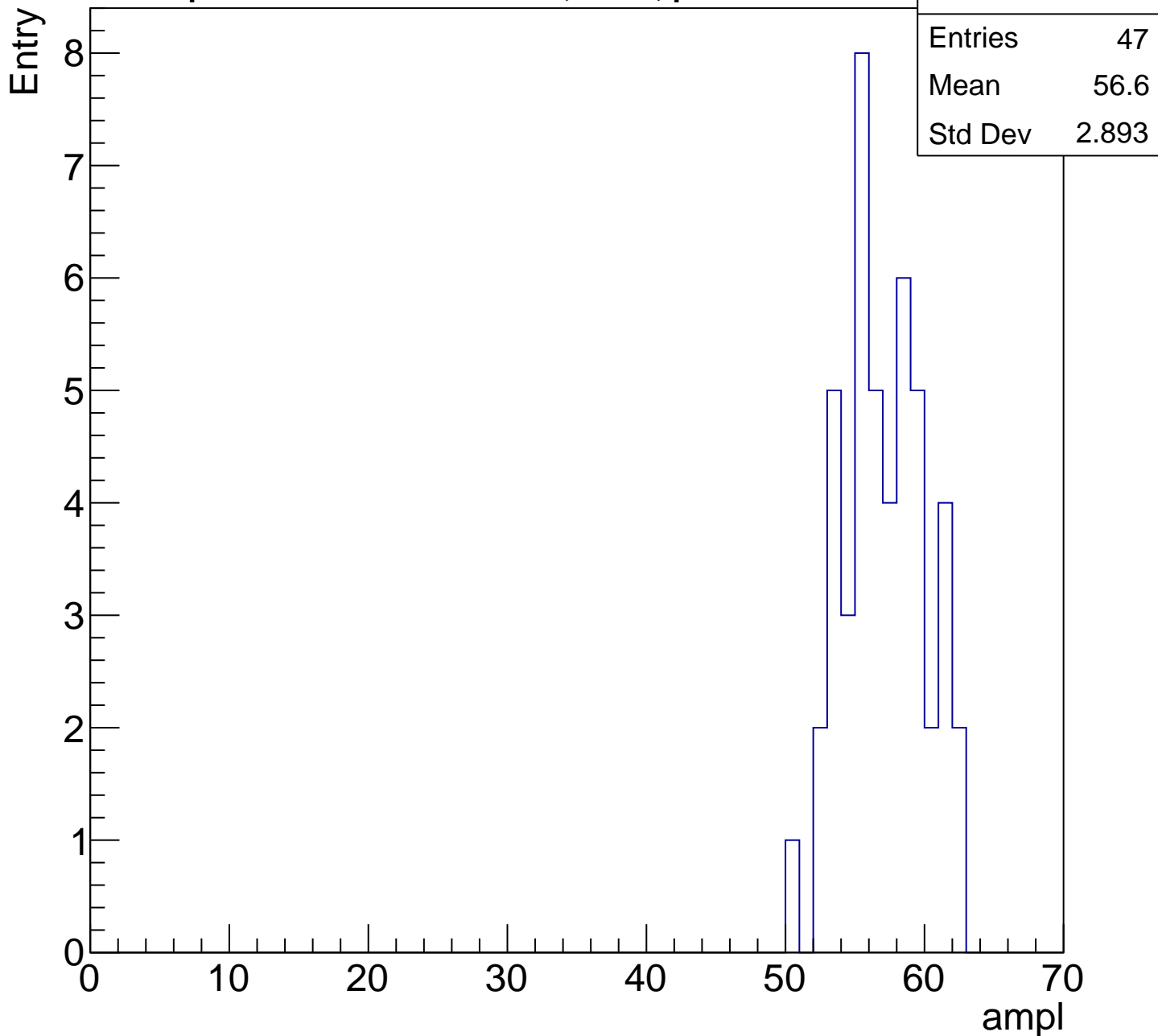
Entry

Entries	74
Mean	50.72
Std Dev	3.347



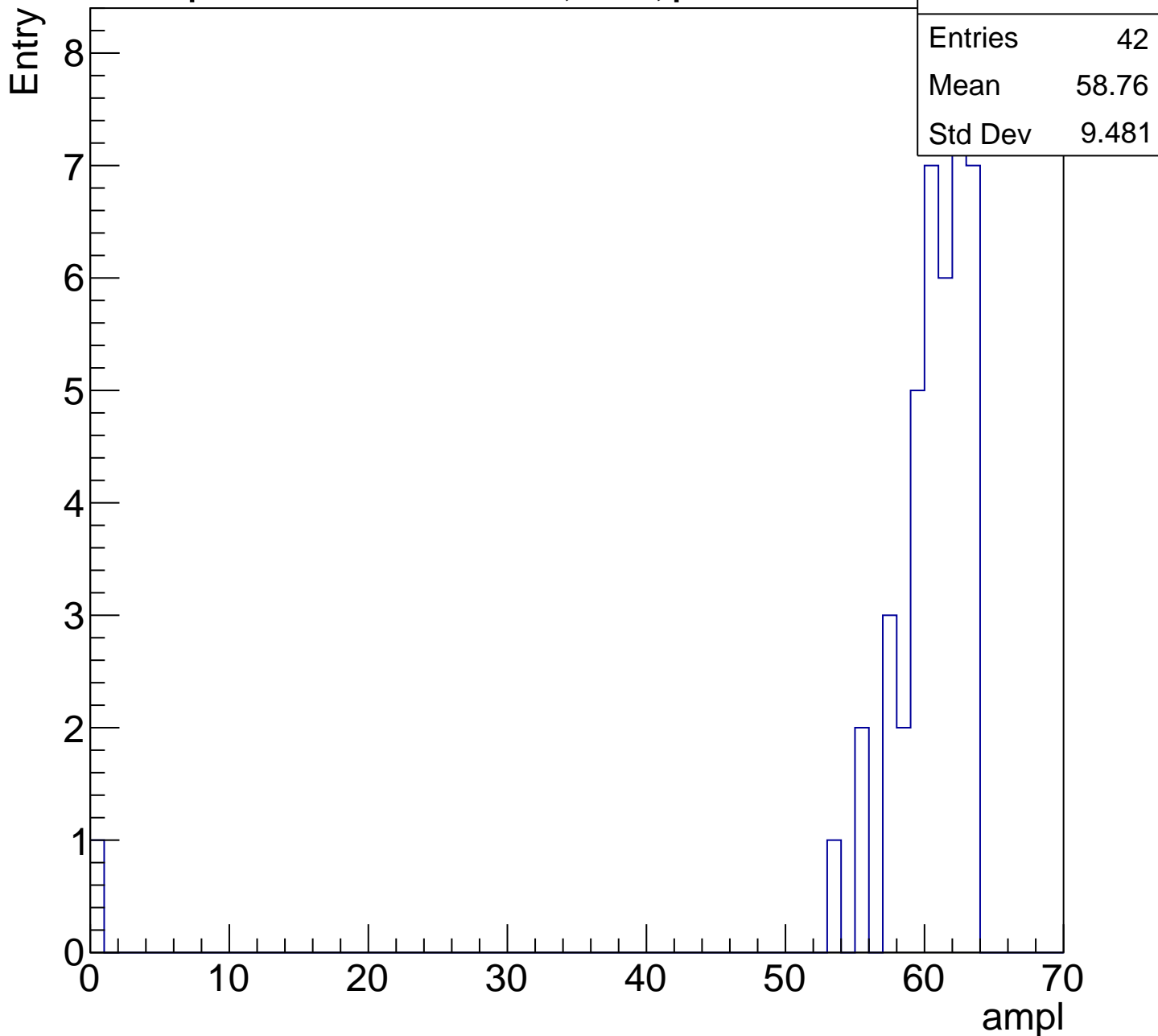
# B1L103S, U9-ch63, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U9-ch63, adc5

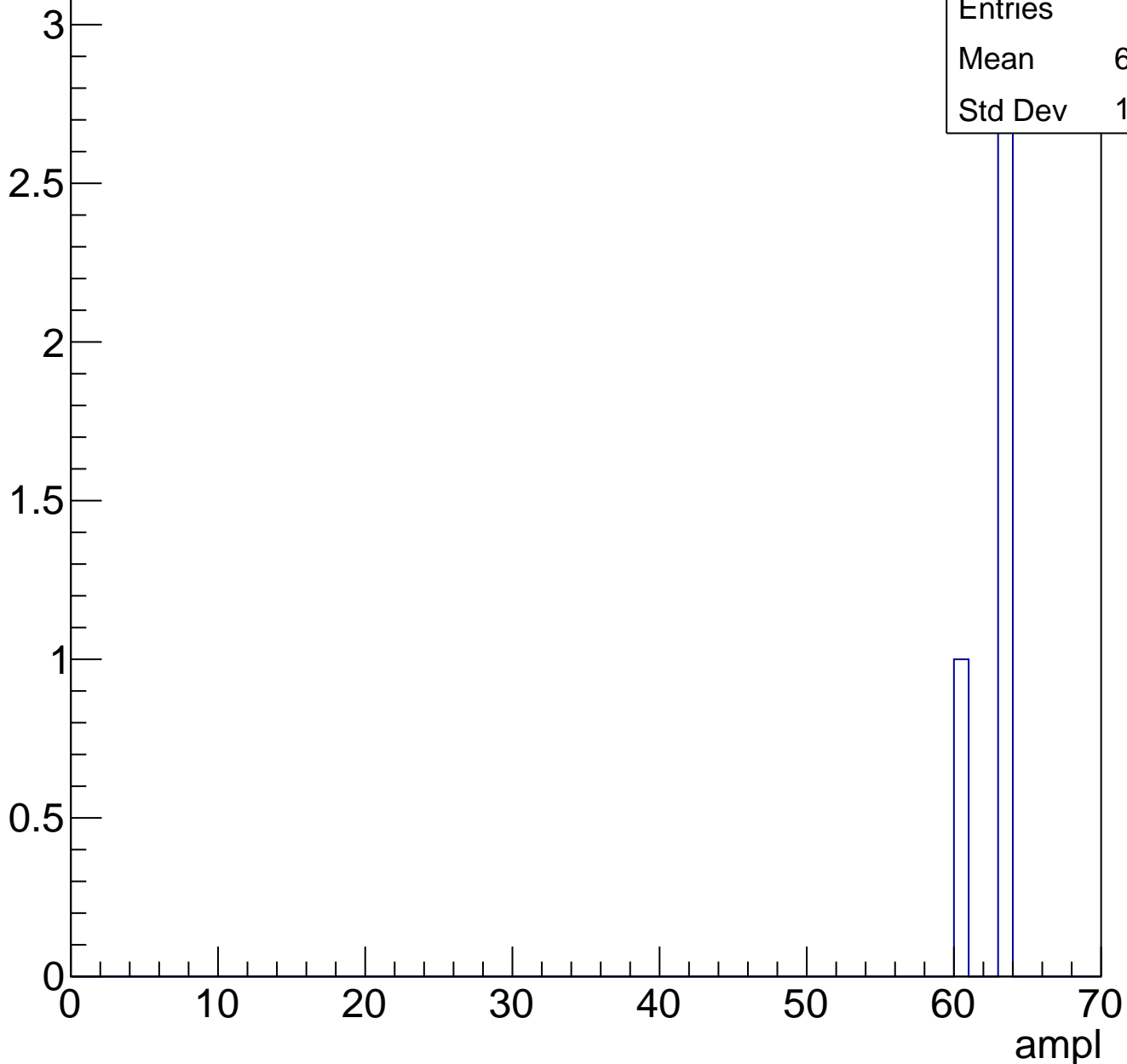
calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U9-ch63, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U9-ch63, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

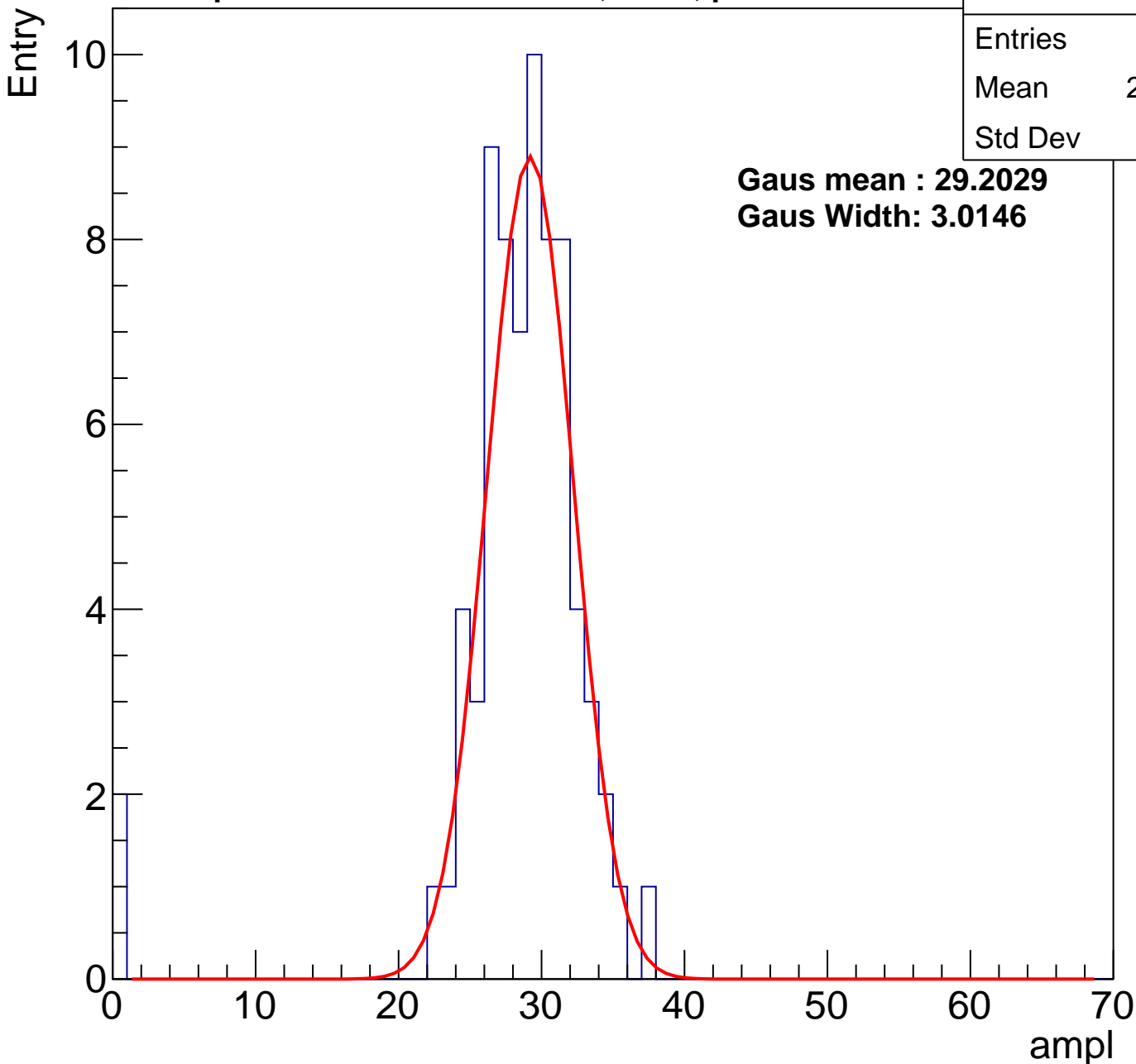
# B1L103S, U9-ch64, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	72
Mean	27.88
Std Dev	5.55

**Gaus mean : 29.2029**

**Gaus Width: 3.0146**



# B1L103S, U9-ch64, adc1

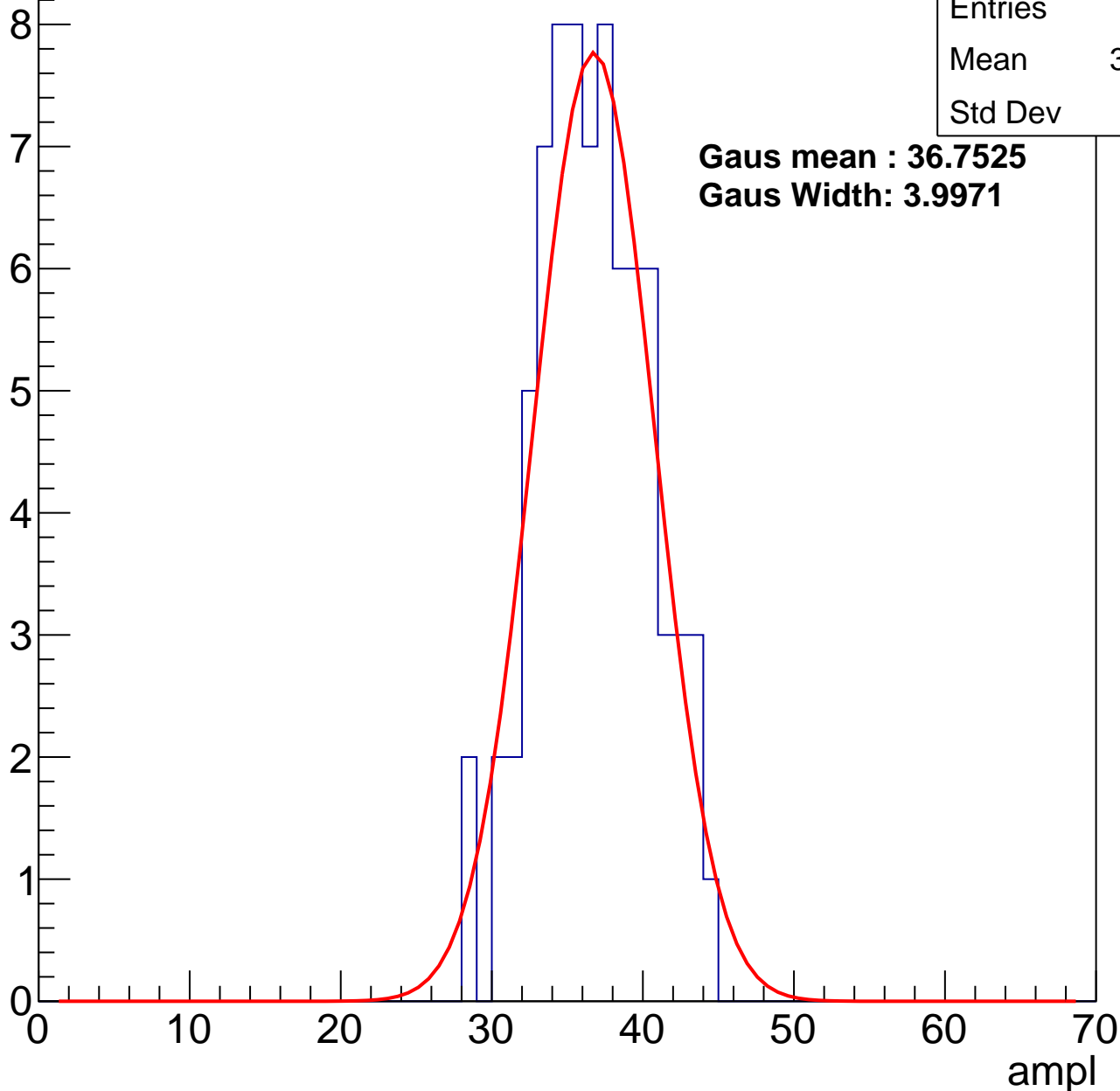
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	77
Mean	36.27
Std Dev	3.61

**Gaus mean : 36.7525**

**Gaus Width: 3.9971**

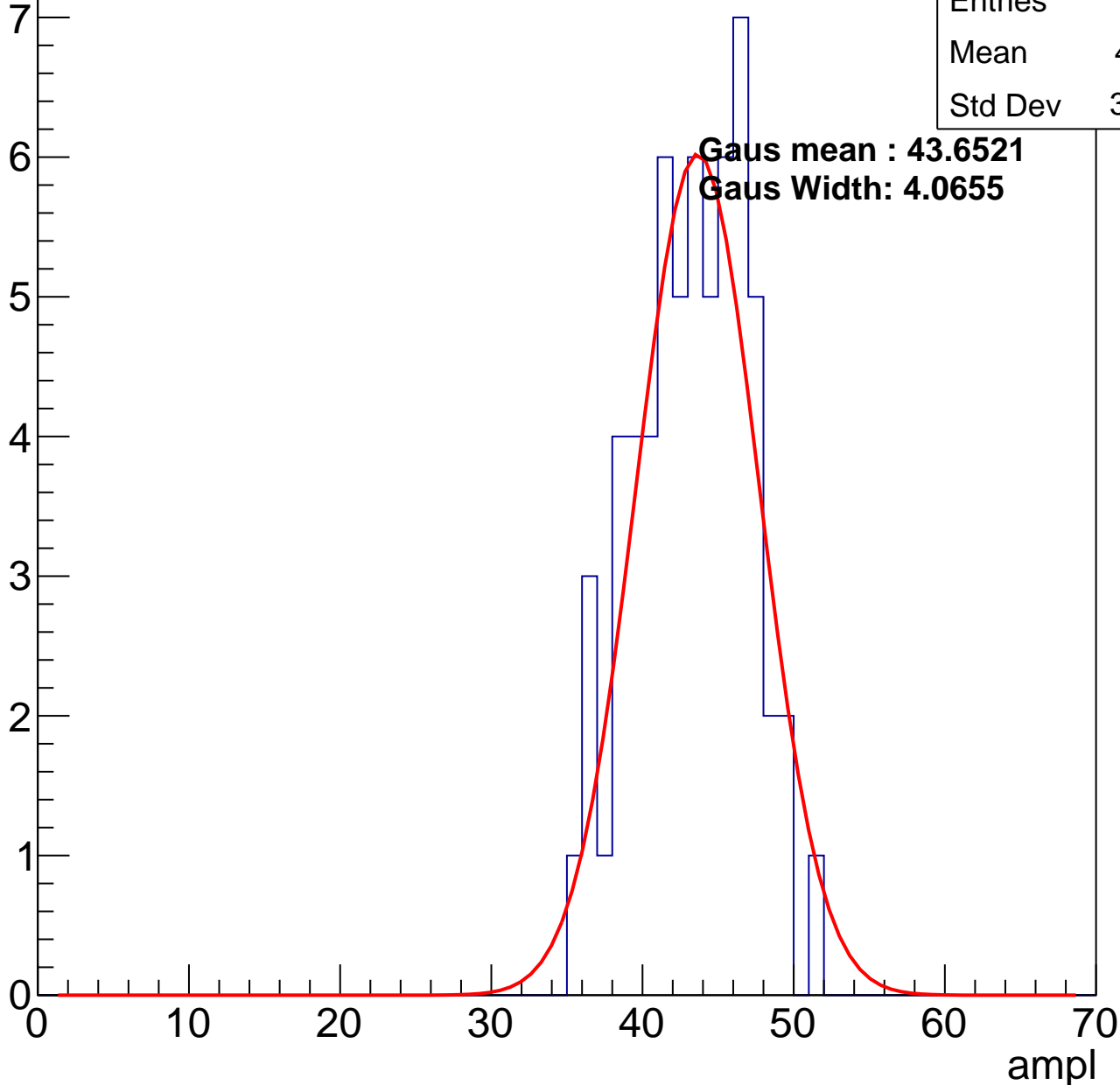


# B1L103S, U9-ch64, adc2

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	42.81
Std Dev	3.663

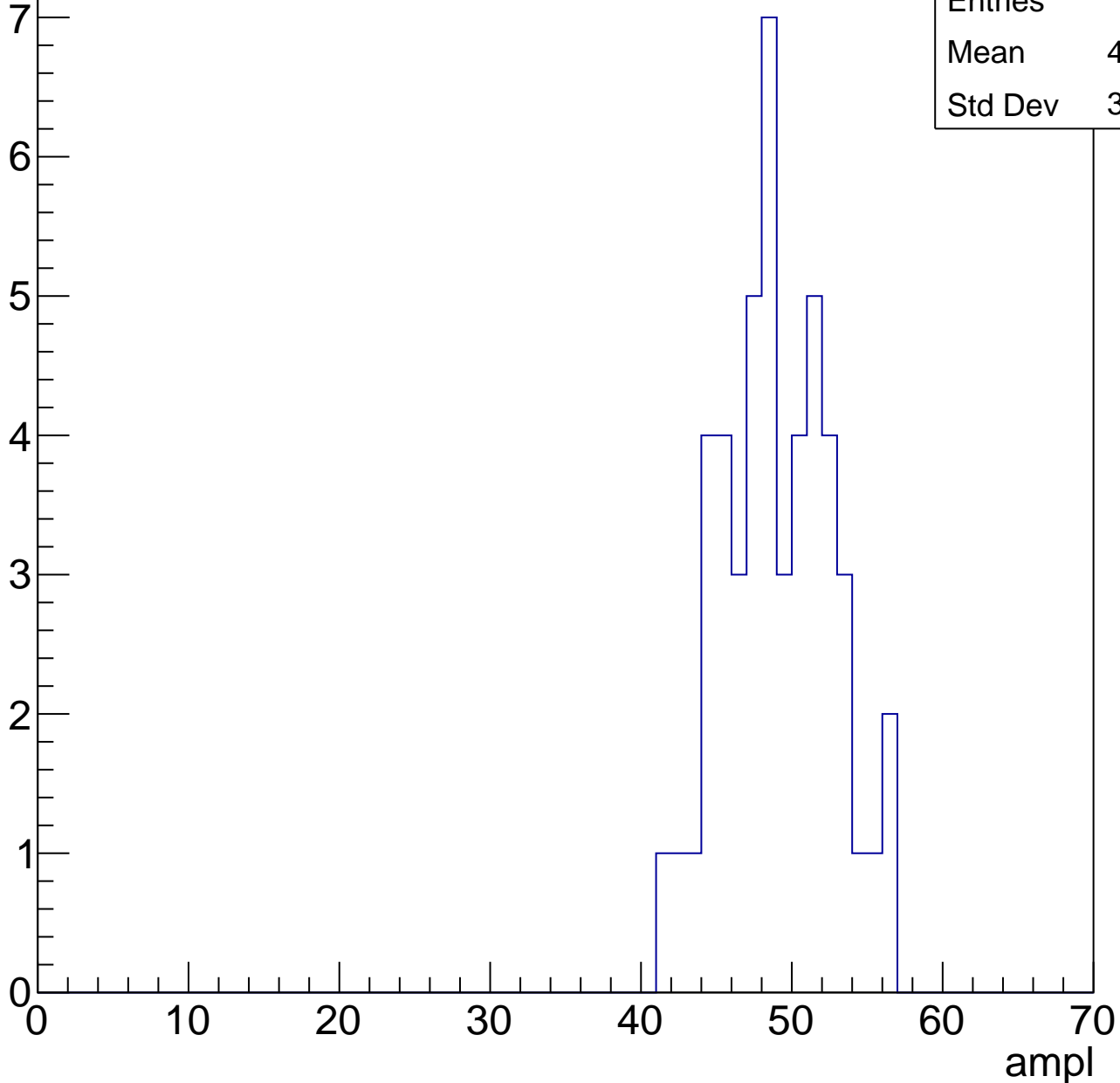


# B1L103S, U9-ch64, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	49
Mean	48.59
Std Dev	3.574

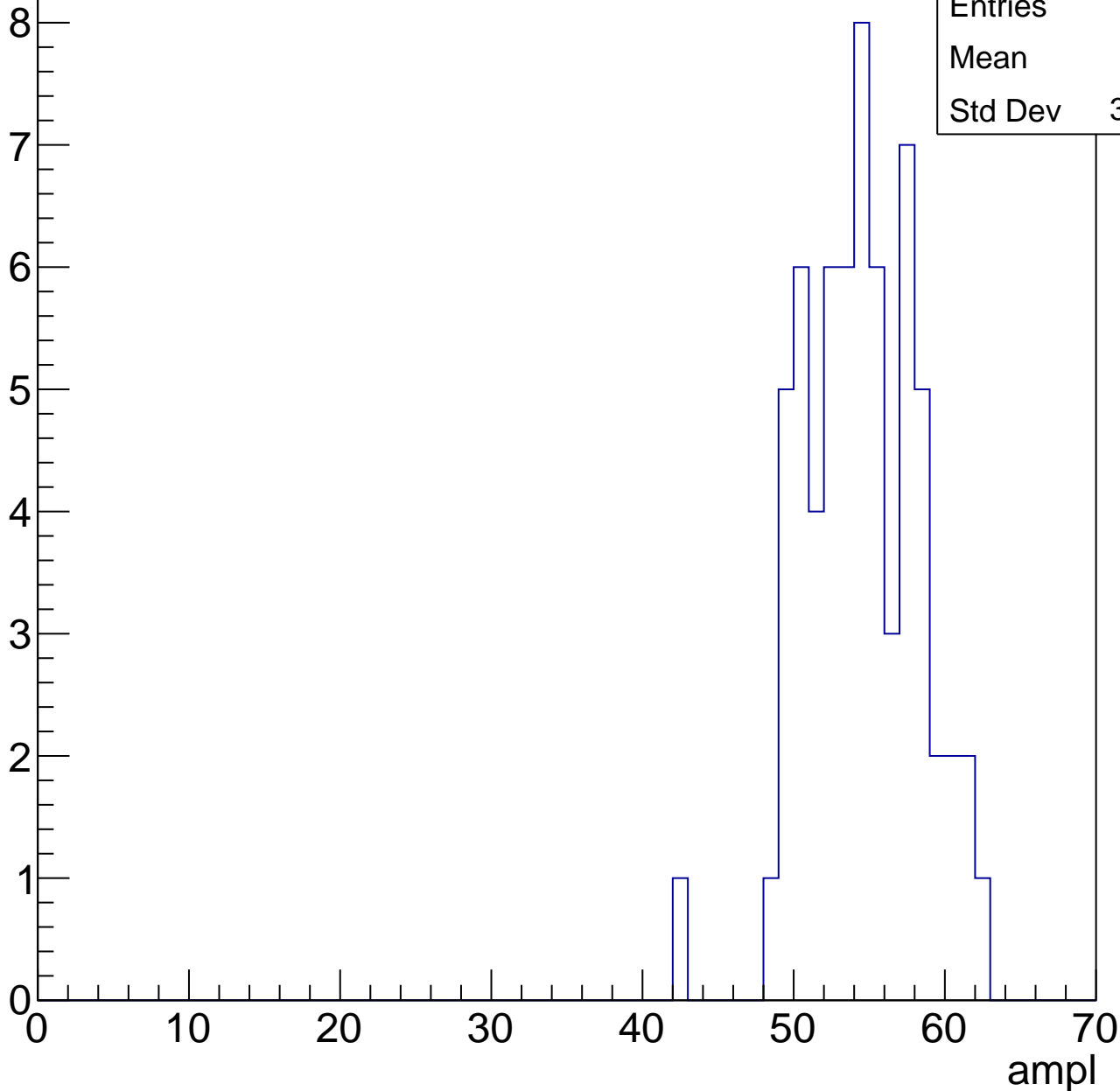


# B1L103S, U9-ch64, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

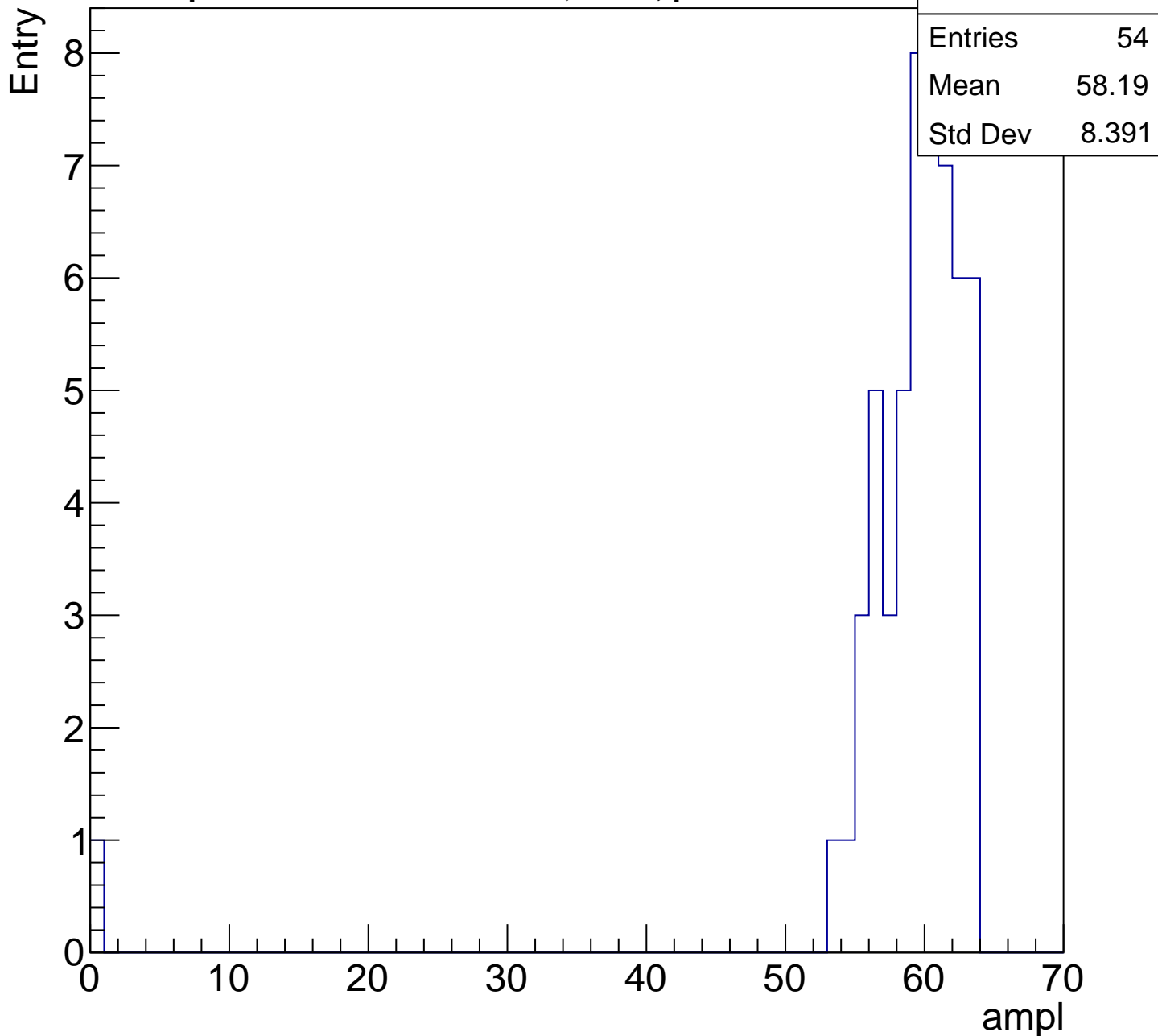
Entry

Entries	65
Mean	54
Std Dev	3.746



# B1L103S, U9-ch64, adc5

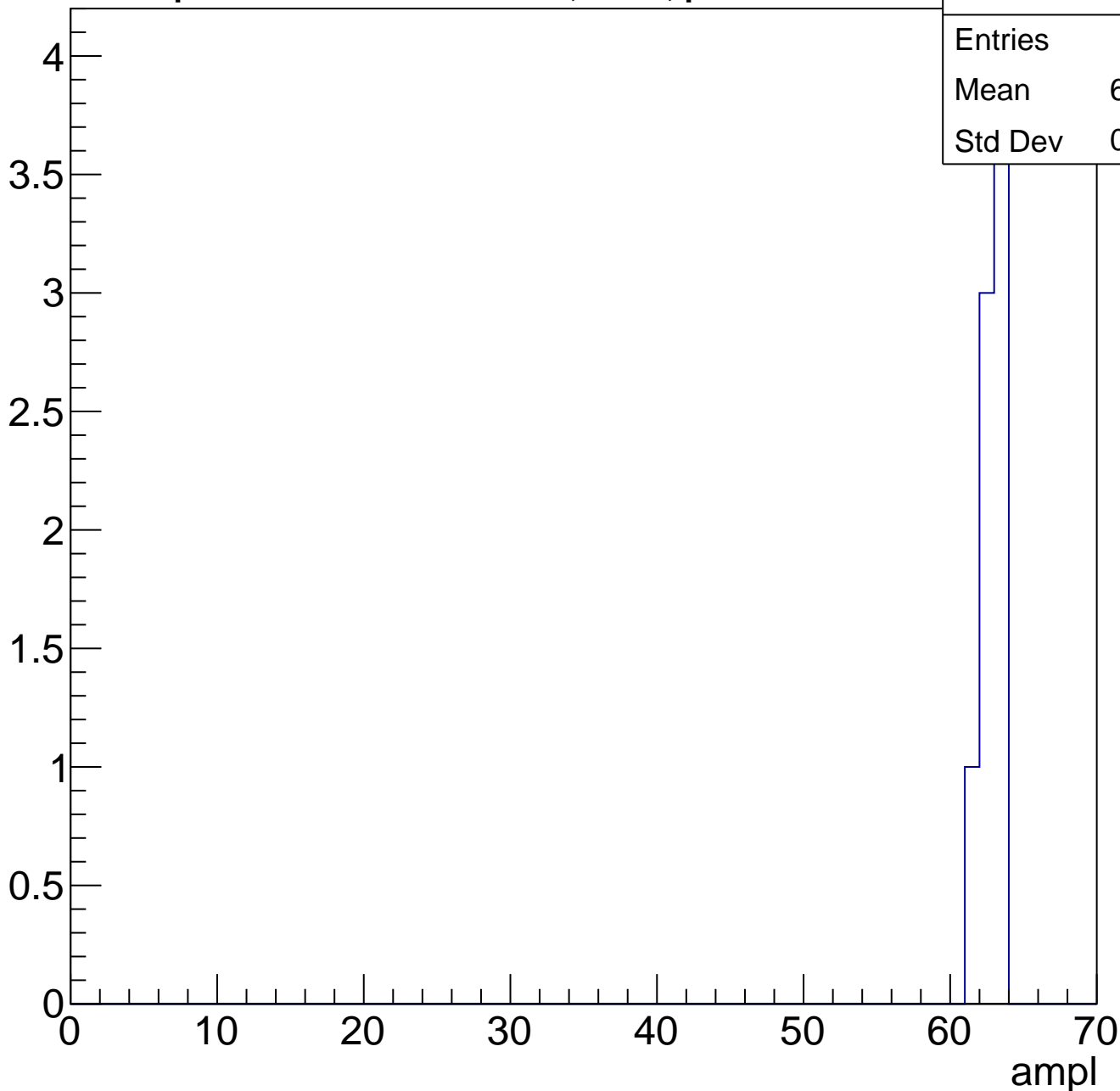
calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U9-ch64, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U9-ch64, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U9-ch65, adc0

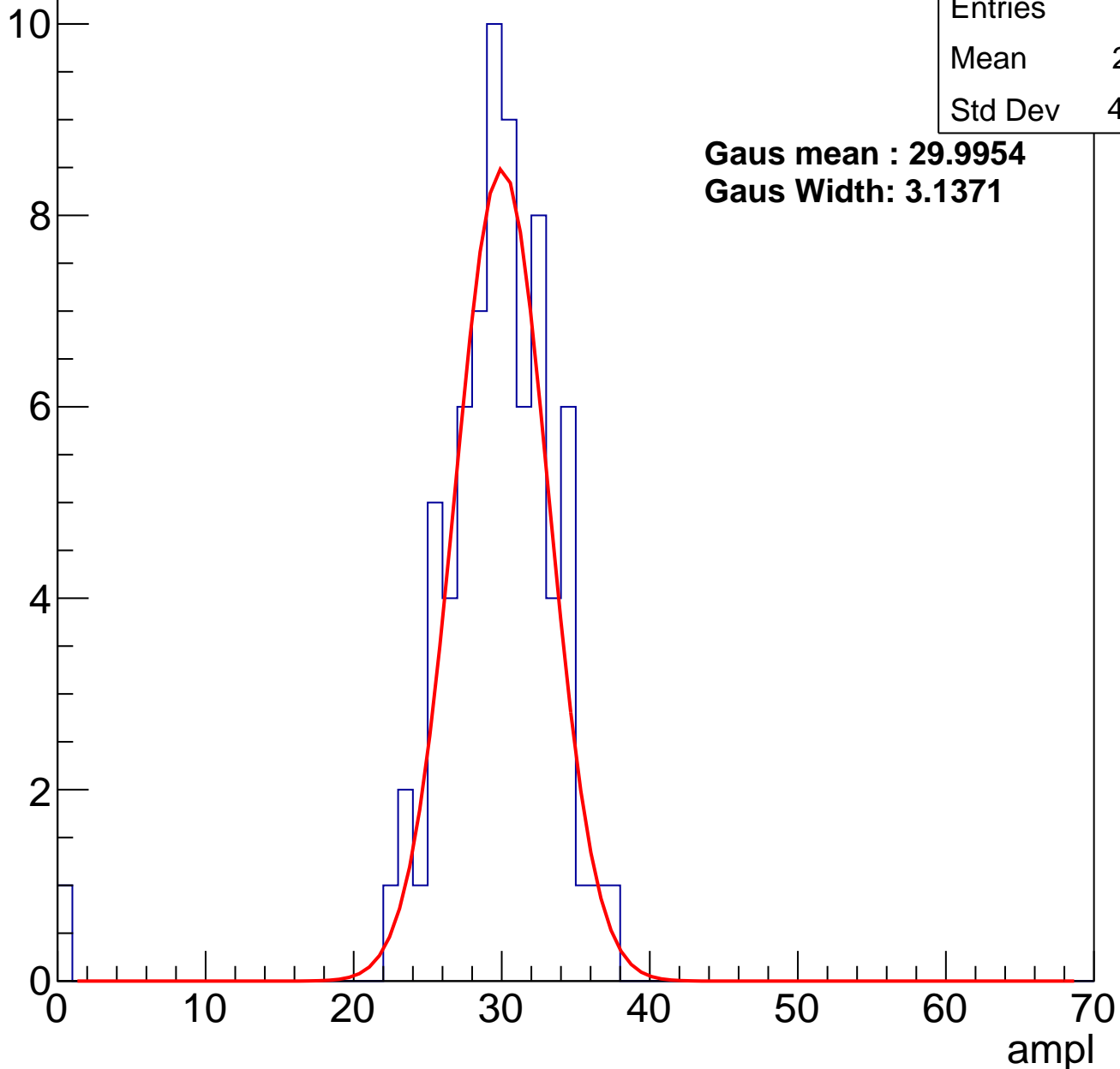
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	73
Mean	29.11
Std Dev	4.683

**Gaus mean : 29.9954**

**Gaus Width: 3.1371**

Entry



# B1L103S, U9-ch65, adc1

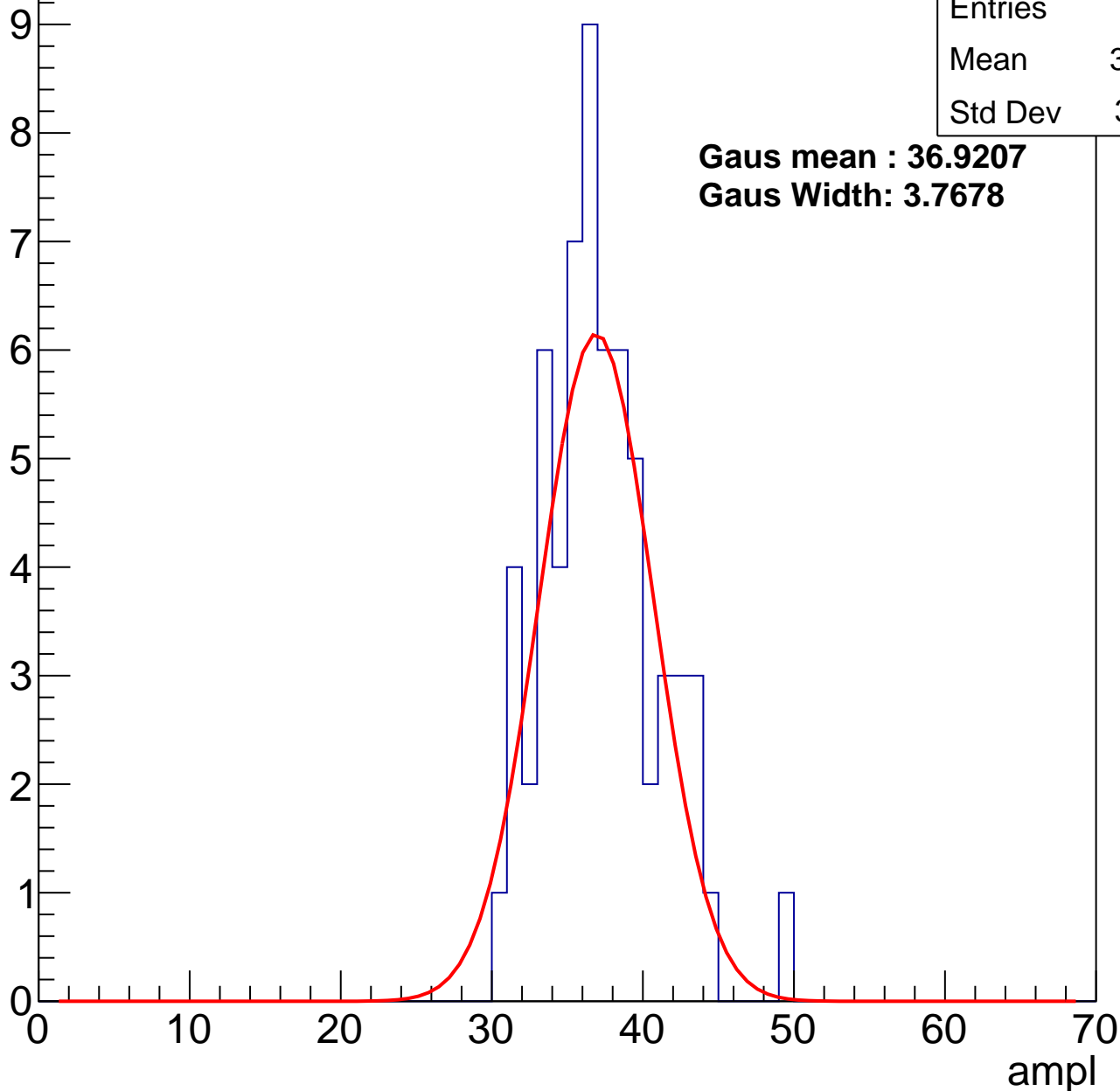
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	36.78
Std Dev	3.731

**Gaus mean : 36.9207**

**Gaus Width: 3.7678**



# B1L103S, U9-ch65, adc2

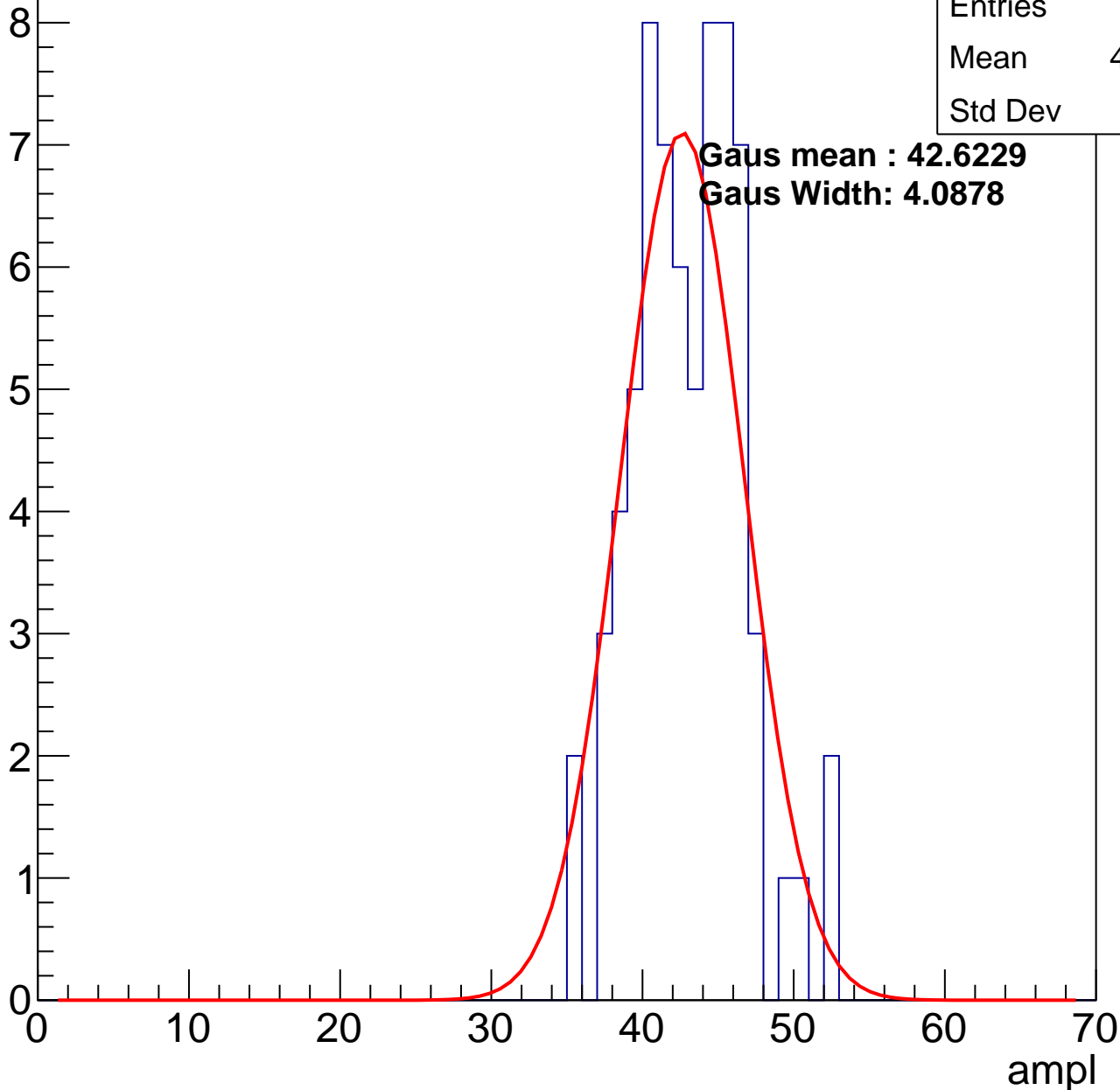
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	70
Mean	42.57
Std Dev	3.6

**Gaus mean : 42.6229**

**Gaus Width: 4.0878**

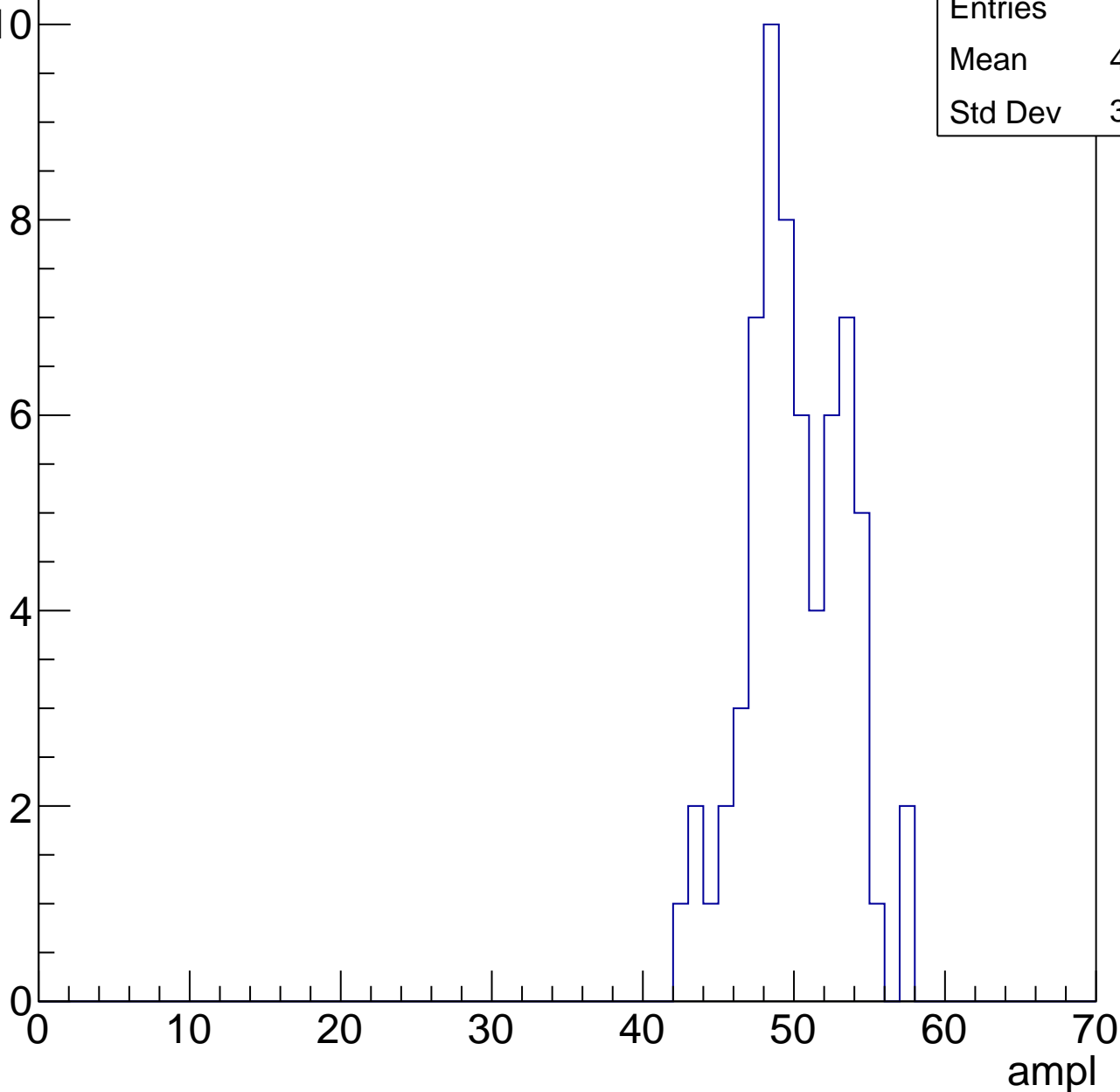


# B1L103S, U9-ch65, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

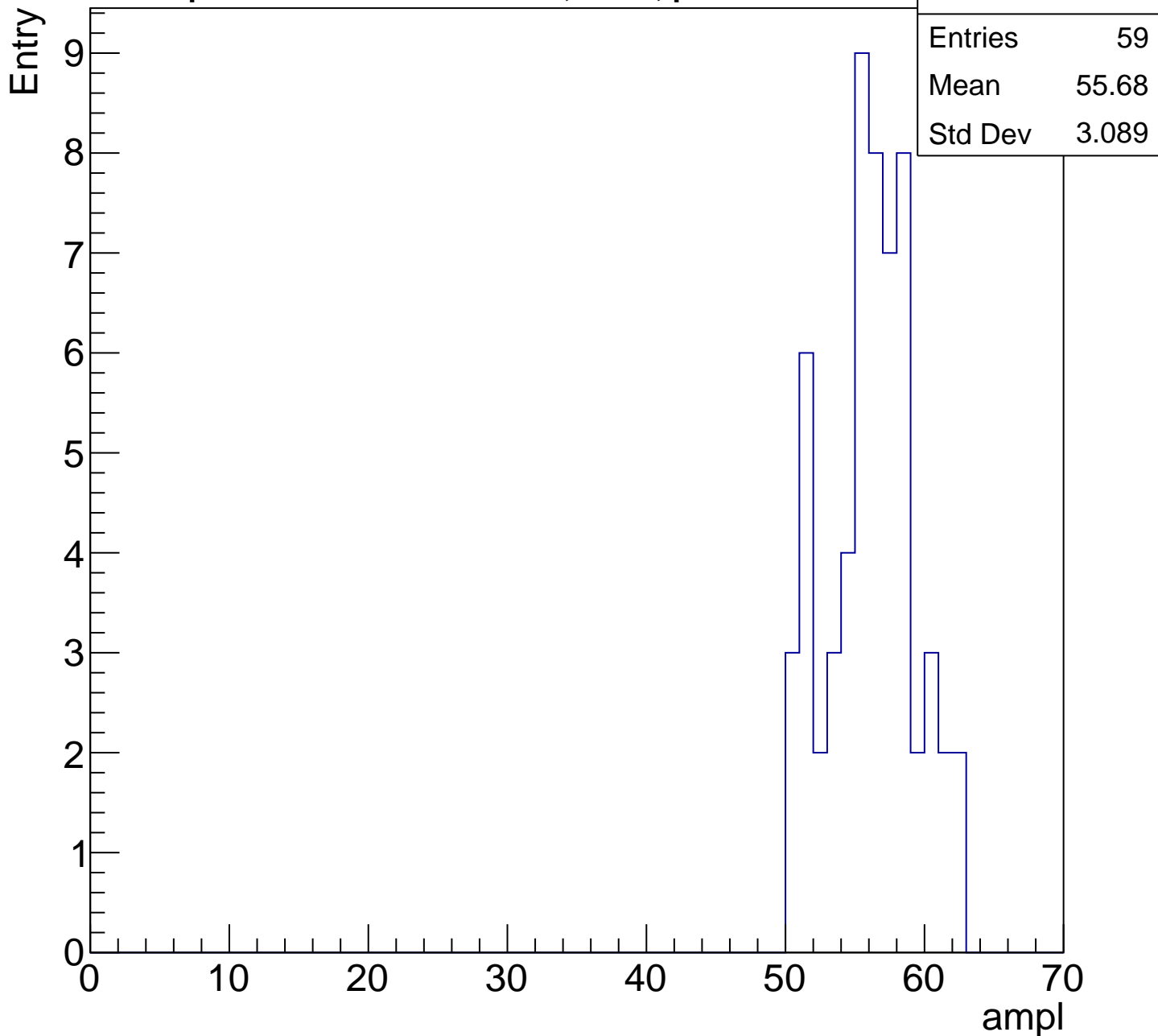
Entry

Entries	65
Mean	49.65
Std Dev	3.265



# B1L103S, U9-ch65, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U9-ch65, adc5

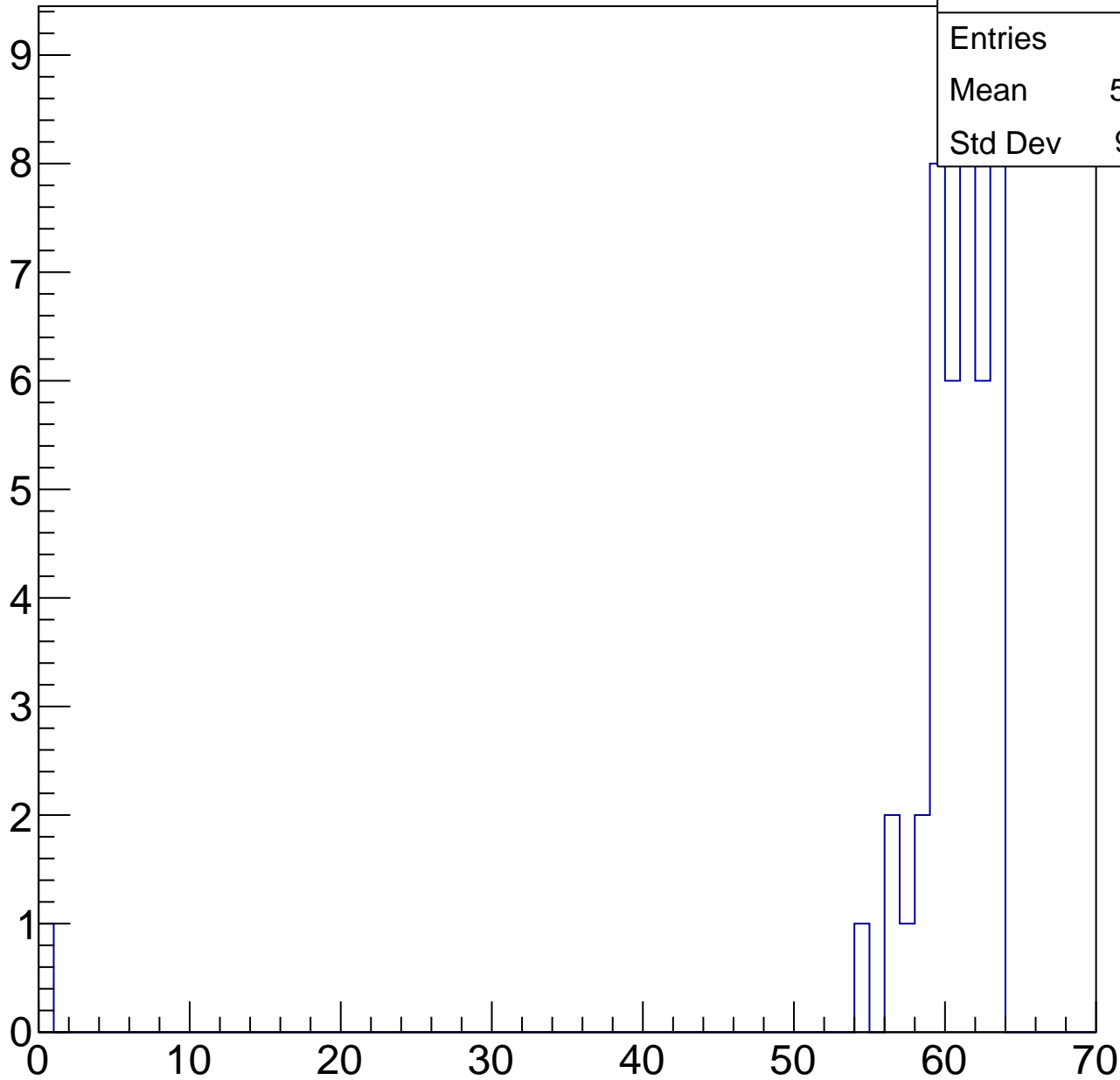
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	44
Mean	59.05
Std Dev	9.251

ampl



# B1L103S, U9-ch65, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

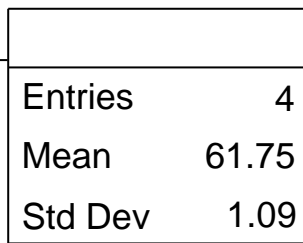
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	4
Mean	61.75
Std Dev	1.09

0 10 20 30 40 50 60 70

ampl





# B1L103S, U9-ch65, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	3
Mean	6.667
Std Dev	9.428

# B1L103S, U9-ch66, adc0

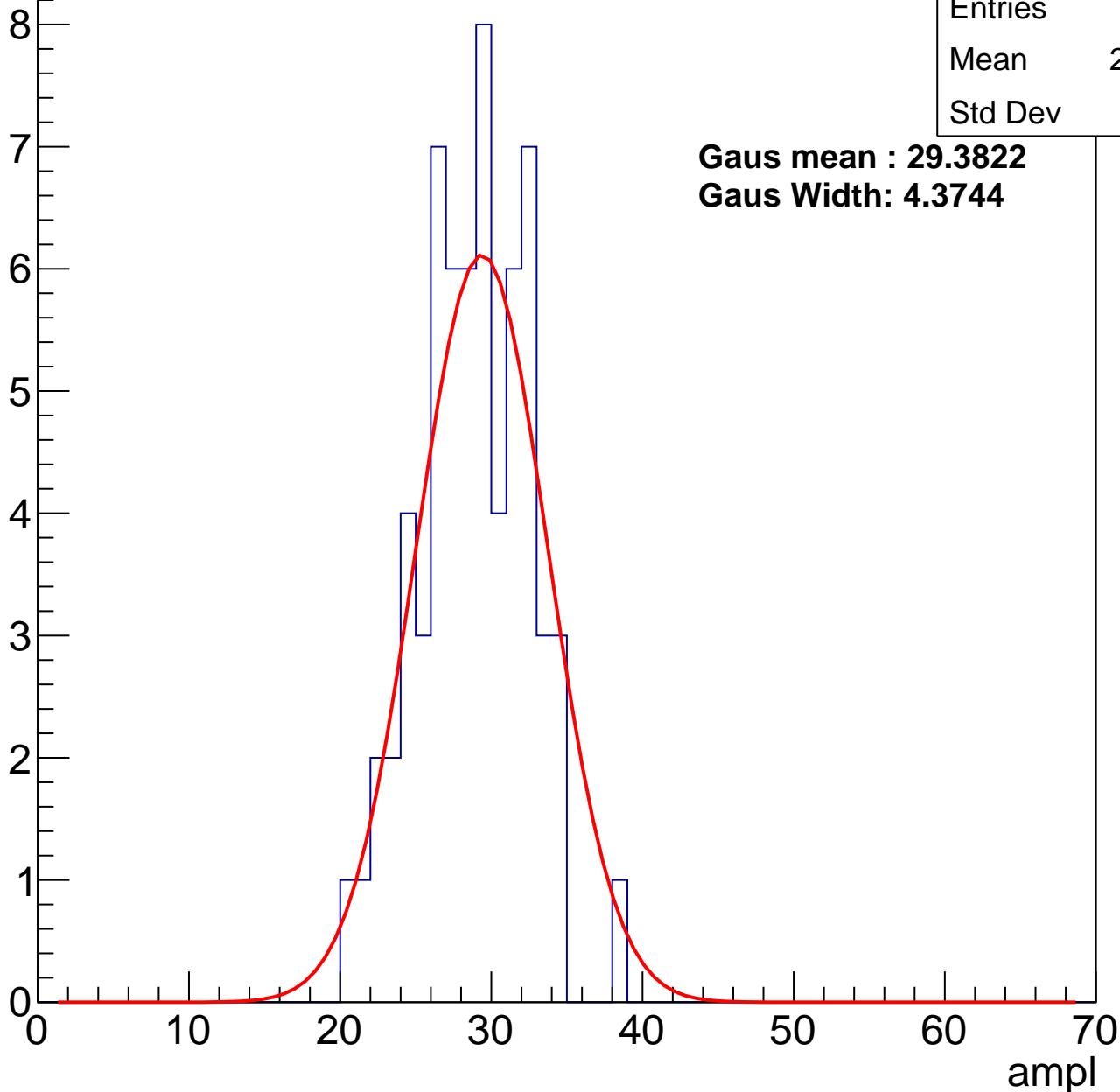
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	28.36
Std Dev	3.59

**Gaus mean : 29.3822**

**Gaus Width: 4.3744**



# B1L103S, U9-ch66, adc1

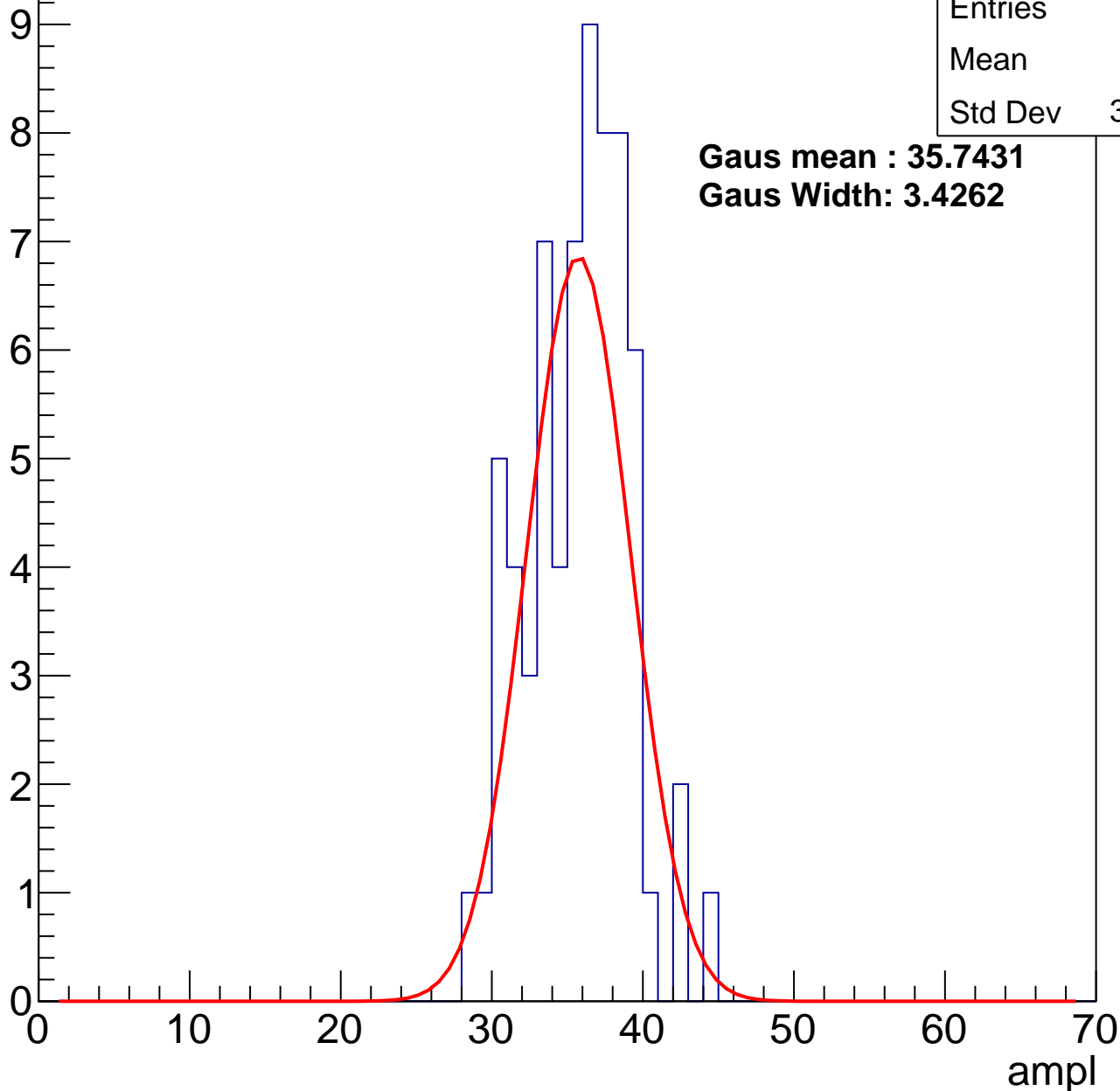
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	35.3
Std Dev	3.323

**Gaus mean : 35.7431**

**Gaus Width: 3.4262**



# B1L103S, U9-ch66, adc2

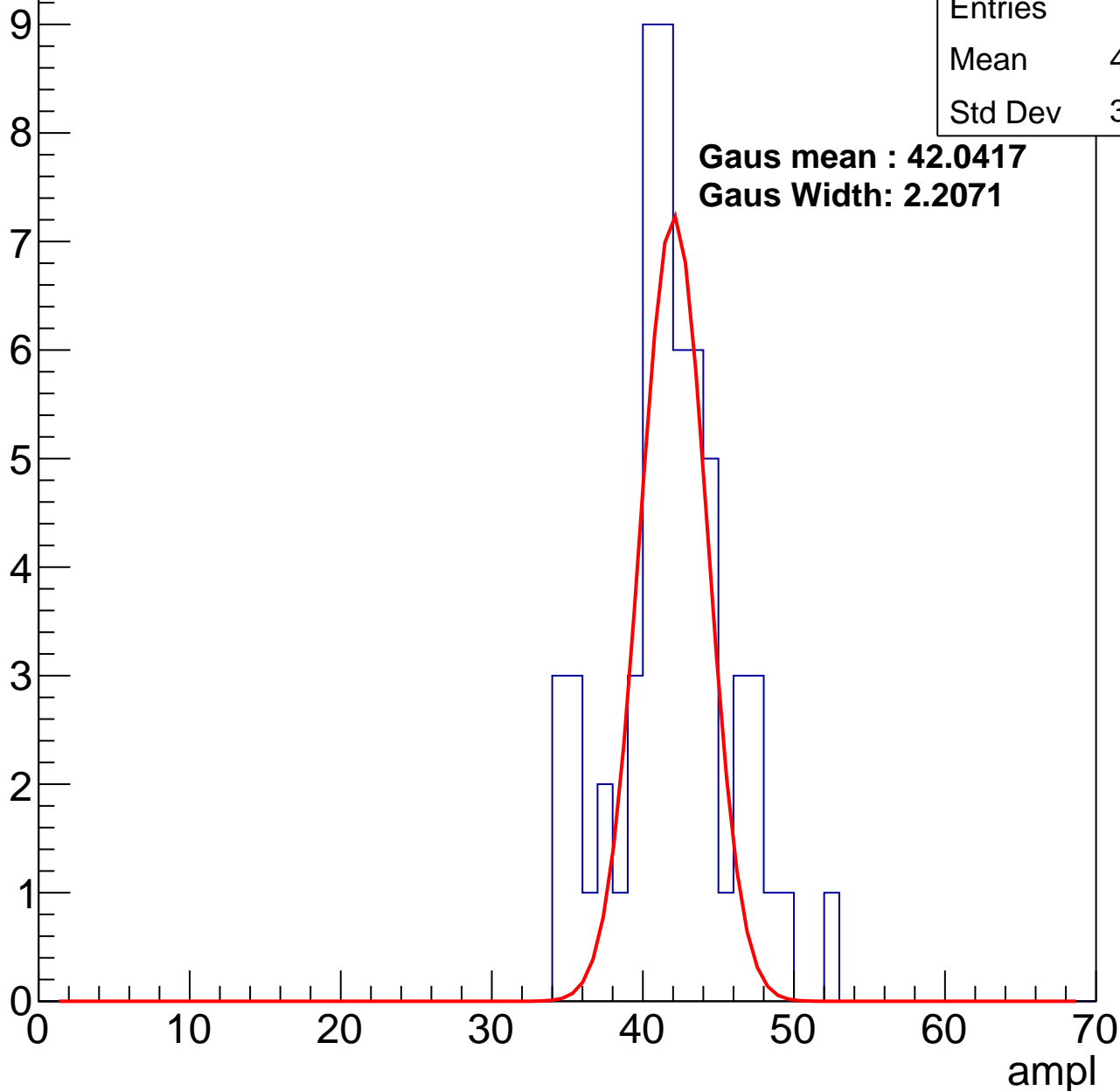
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	58
Mean	41.45
Std Dev	3.802

**Gaus mean : 42.0417**

**Gaus Width: 2.2071**

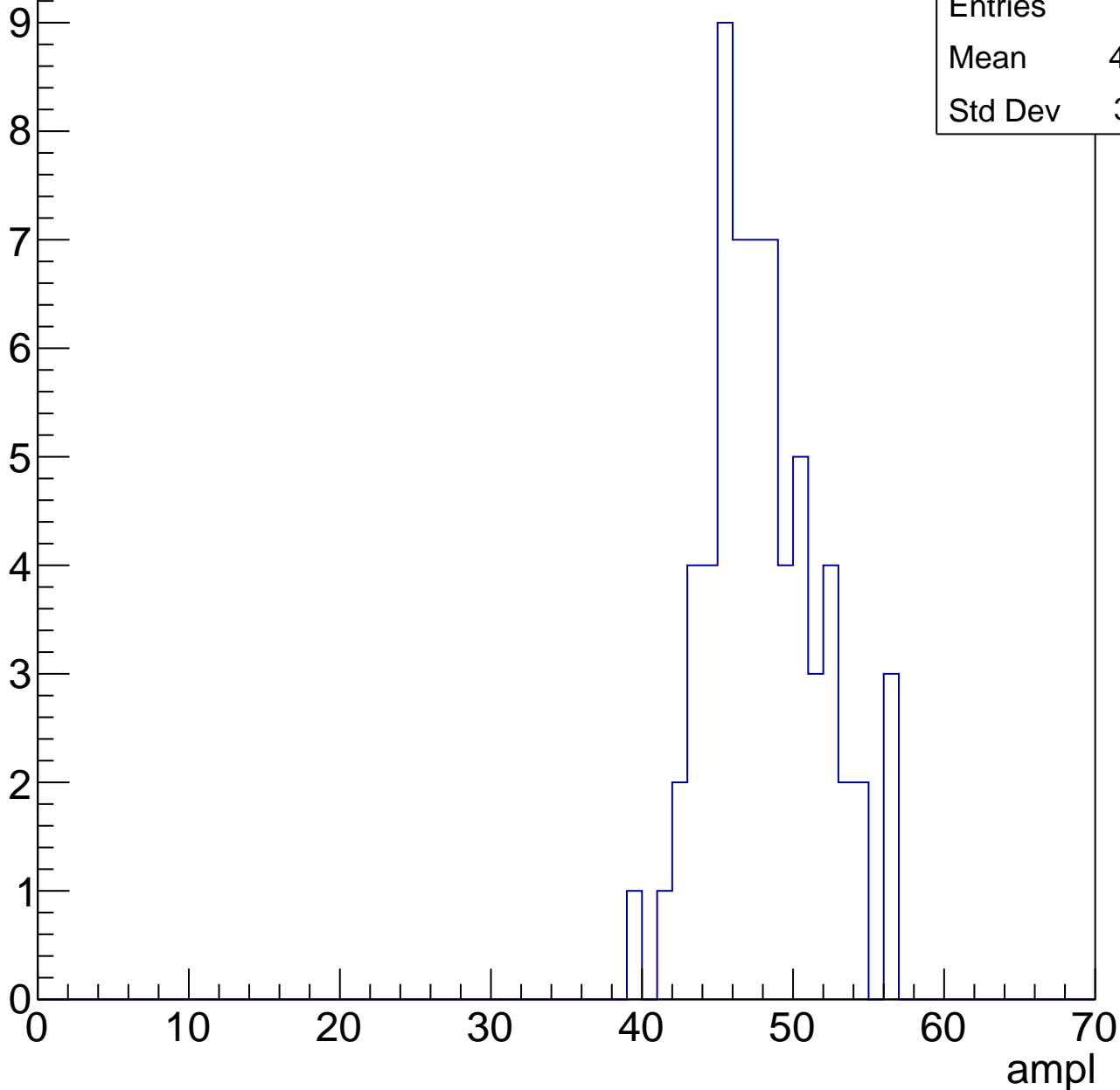


# B1L103S, U9-ch66, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

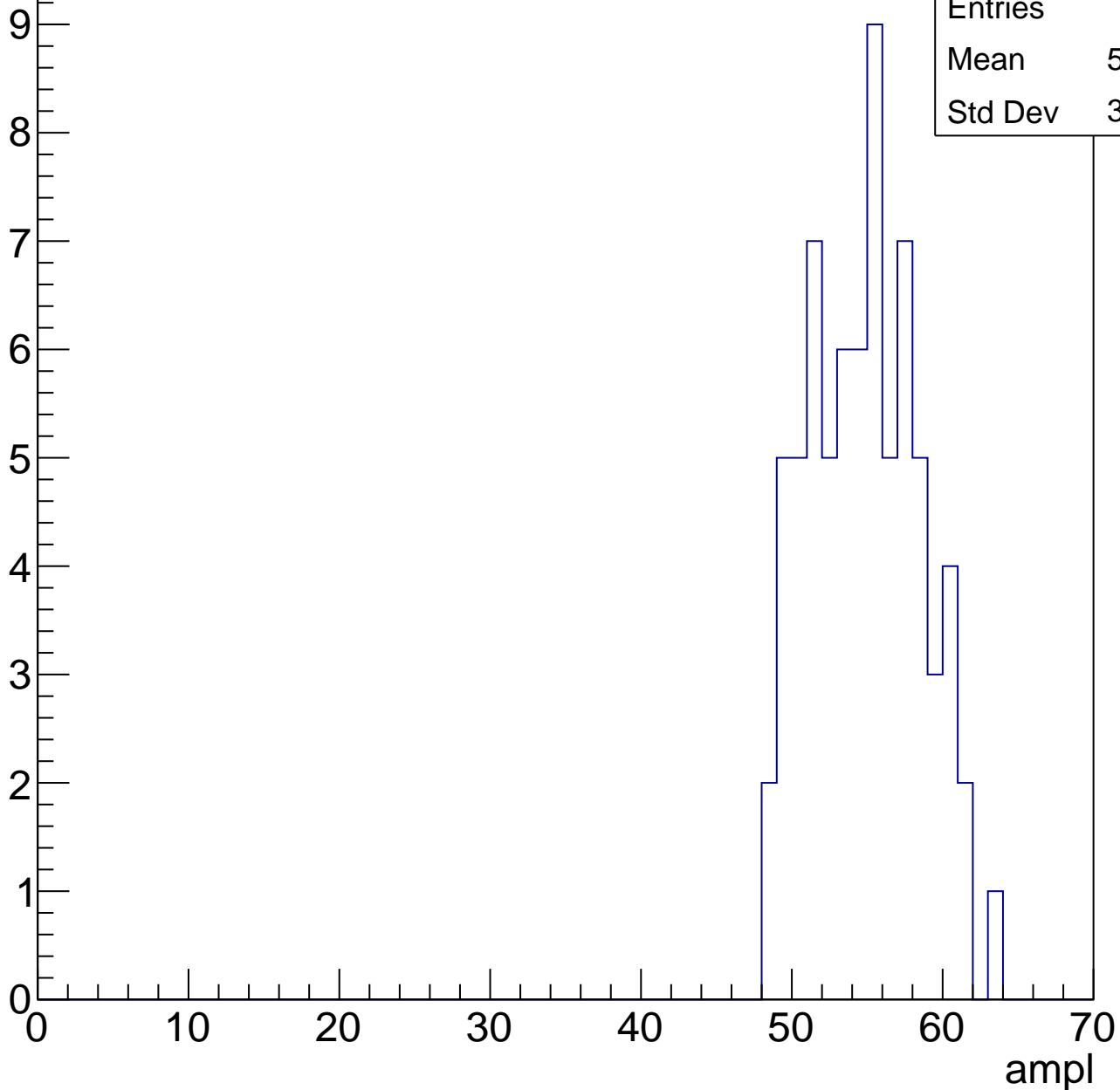
Entries	65
Mean	47.58
Std Dev	3.721



# B1L103S, U9-ch66, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

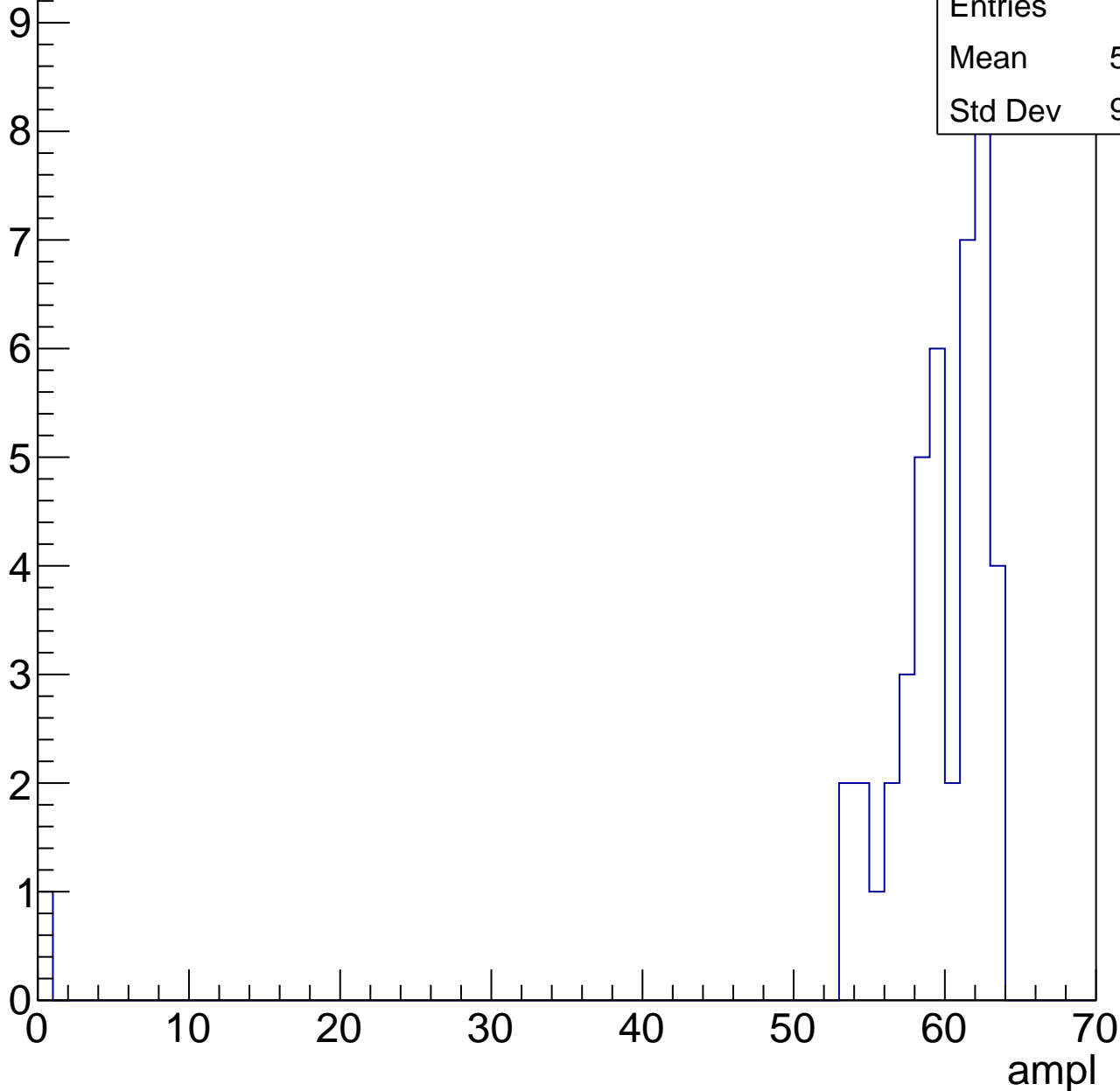


# B1L103S, U9-ch66, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	44
Mean	58.02
Std Dev	9.277

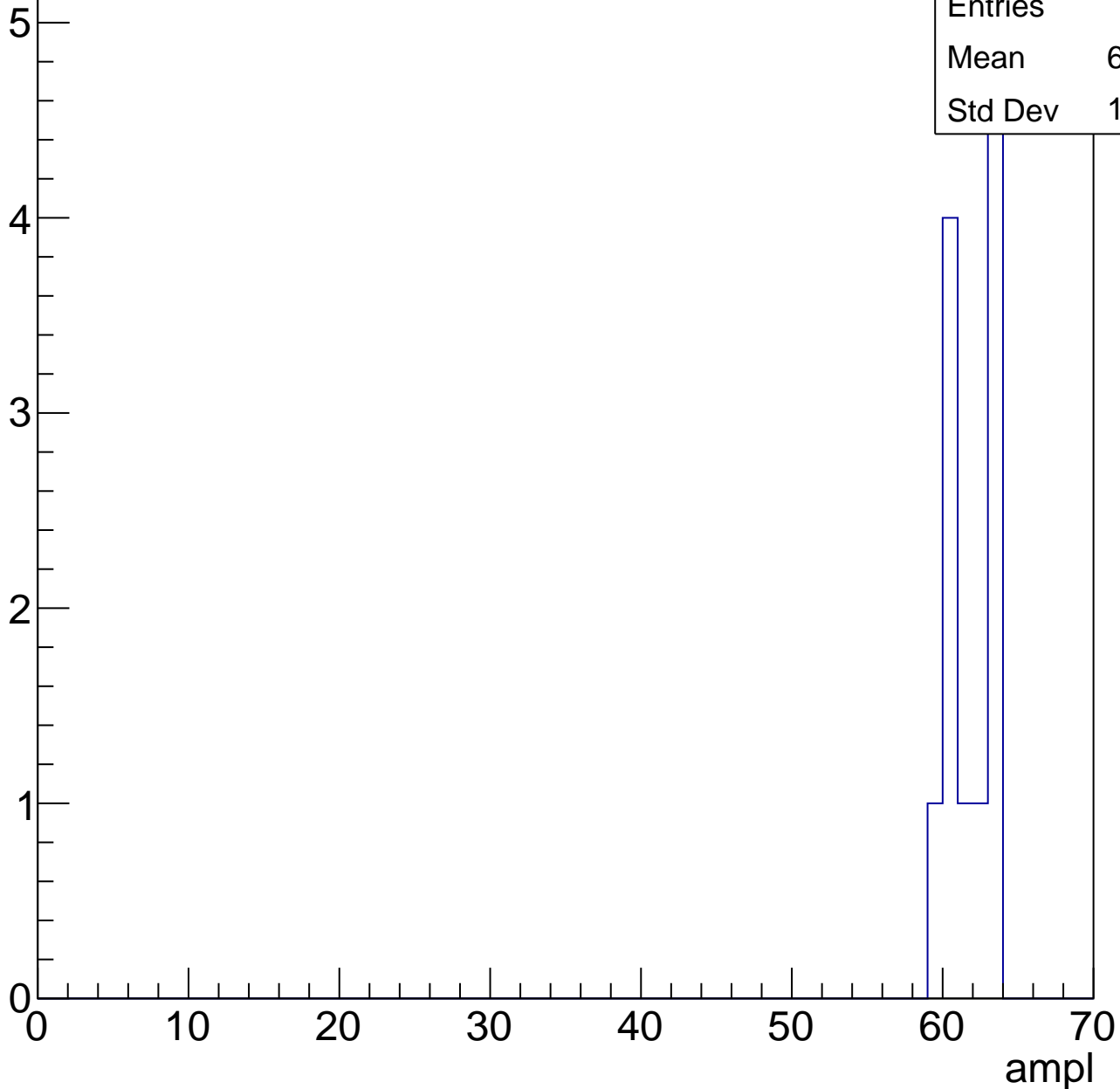


# B1L103S, U9-ch66, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	12
Mean	61.42
Std Dev	1.498





# B1L103S, U9-ch66, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U9-ch67, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

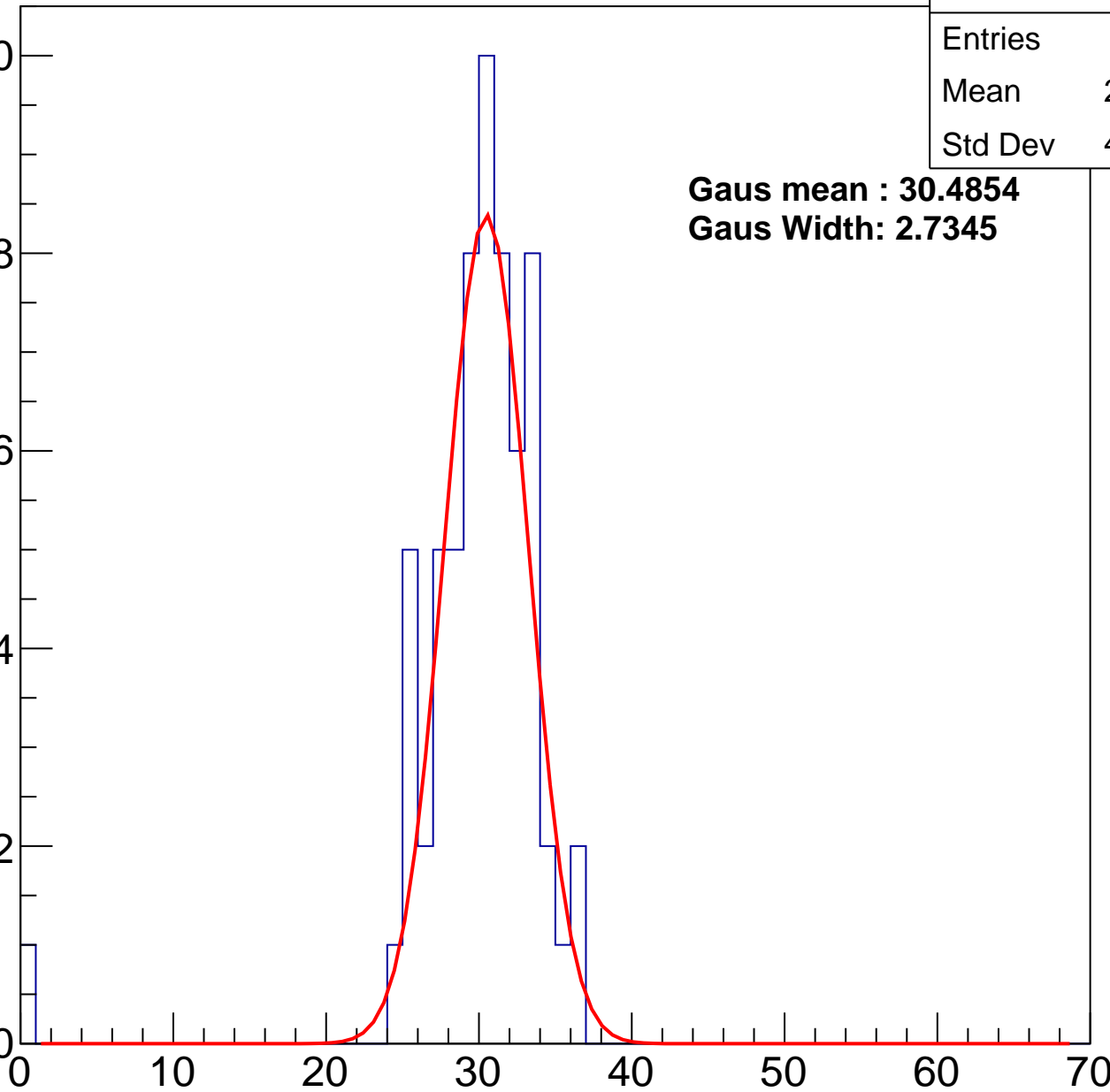
Entries	64
Mean	29.48
Std Dev	4.647

**Gaus mean : 30.4854**

**Gaus Width: 2.7345**

10  
8  
6  
4  
2  
0

ampl



# B1L103S, U9-ch67, adc1

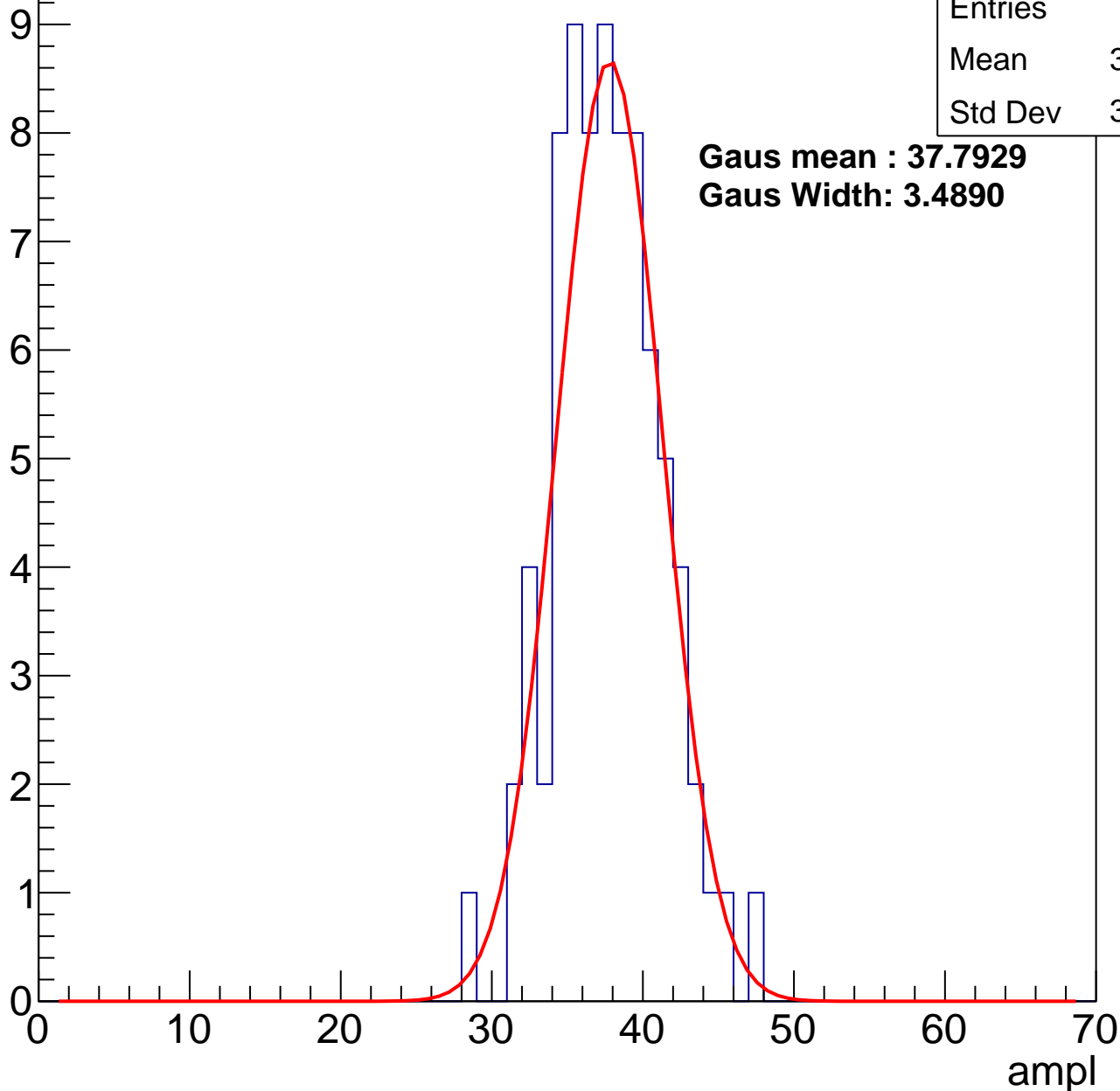
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	79
Mean	37.25
Std Dev	3.477

**Gaus mean : 37.7929**

**Gaus Width: 3.4890**



# B1L103S, U9-ch67, adc2

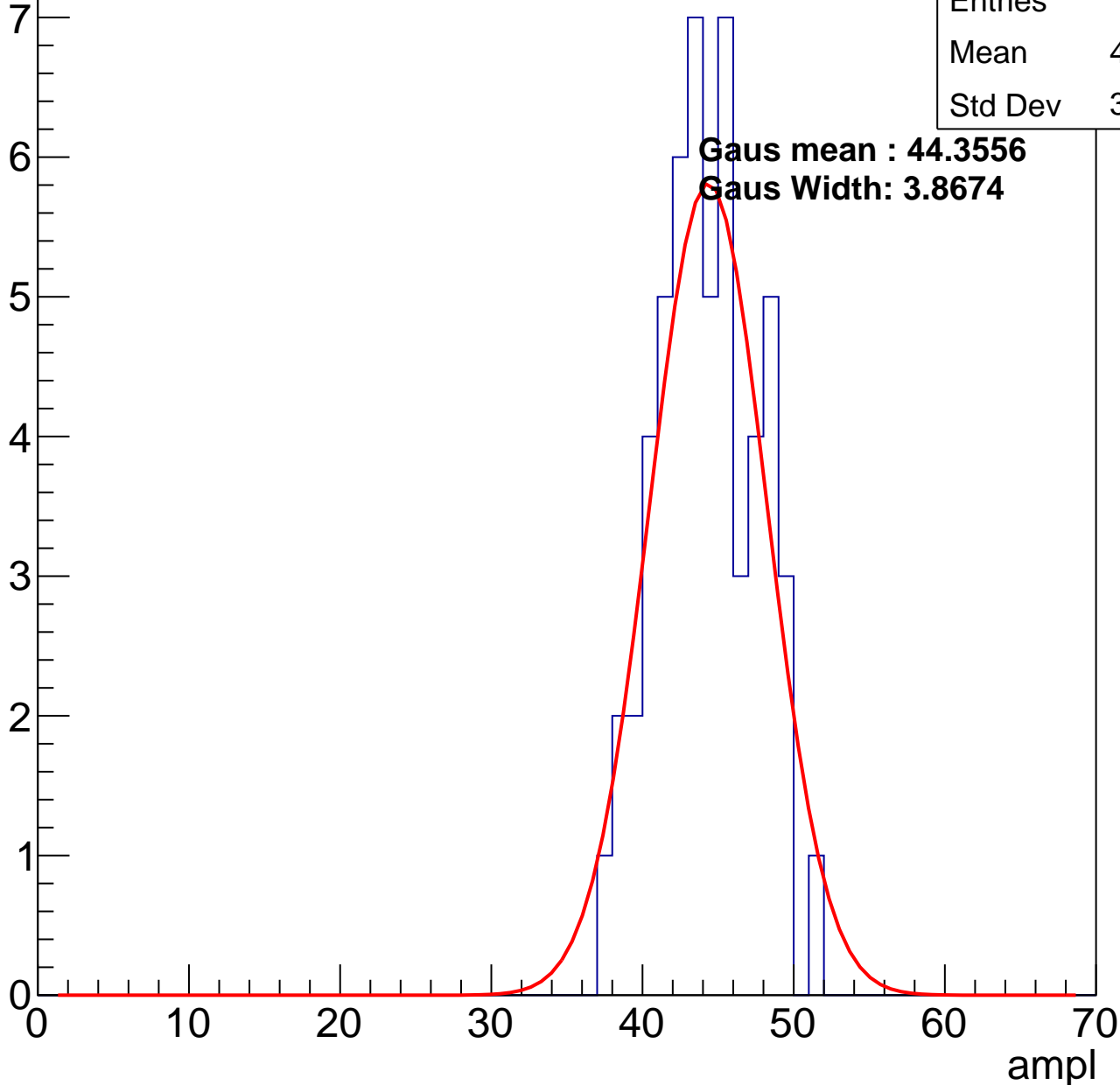
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	55
Mean	43.78
Std Dev	3.212

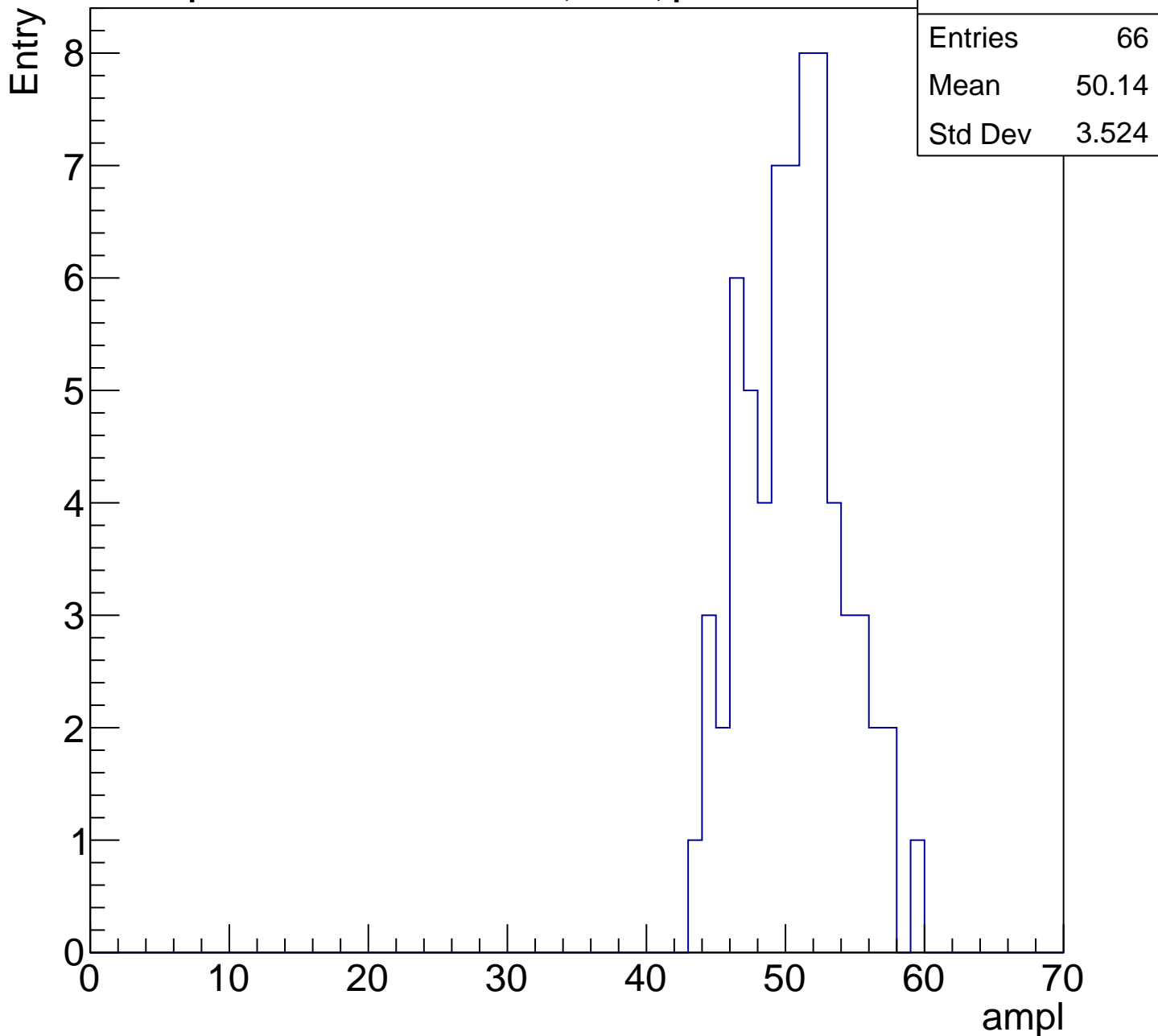
**Gaus mean : 44.3556**

**Gaus Width: 3.8674**



# B1L103S, U9-ch67, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

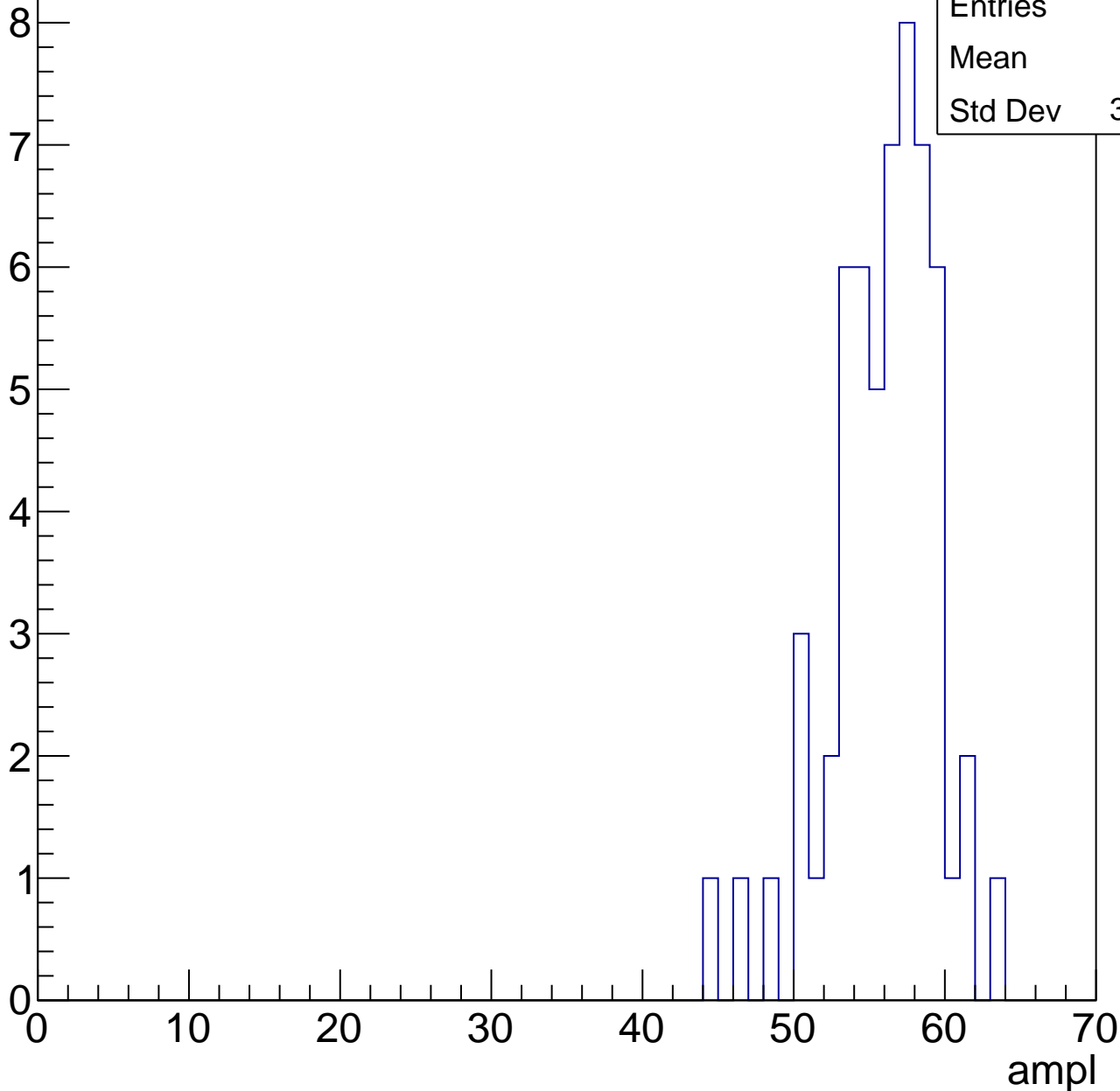


# B1L103S, U9-ch67, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	58
Mean	55.4
Std Dev	3.572

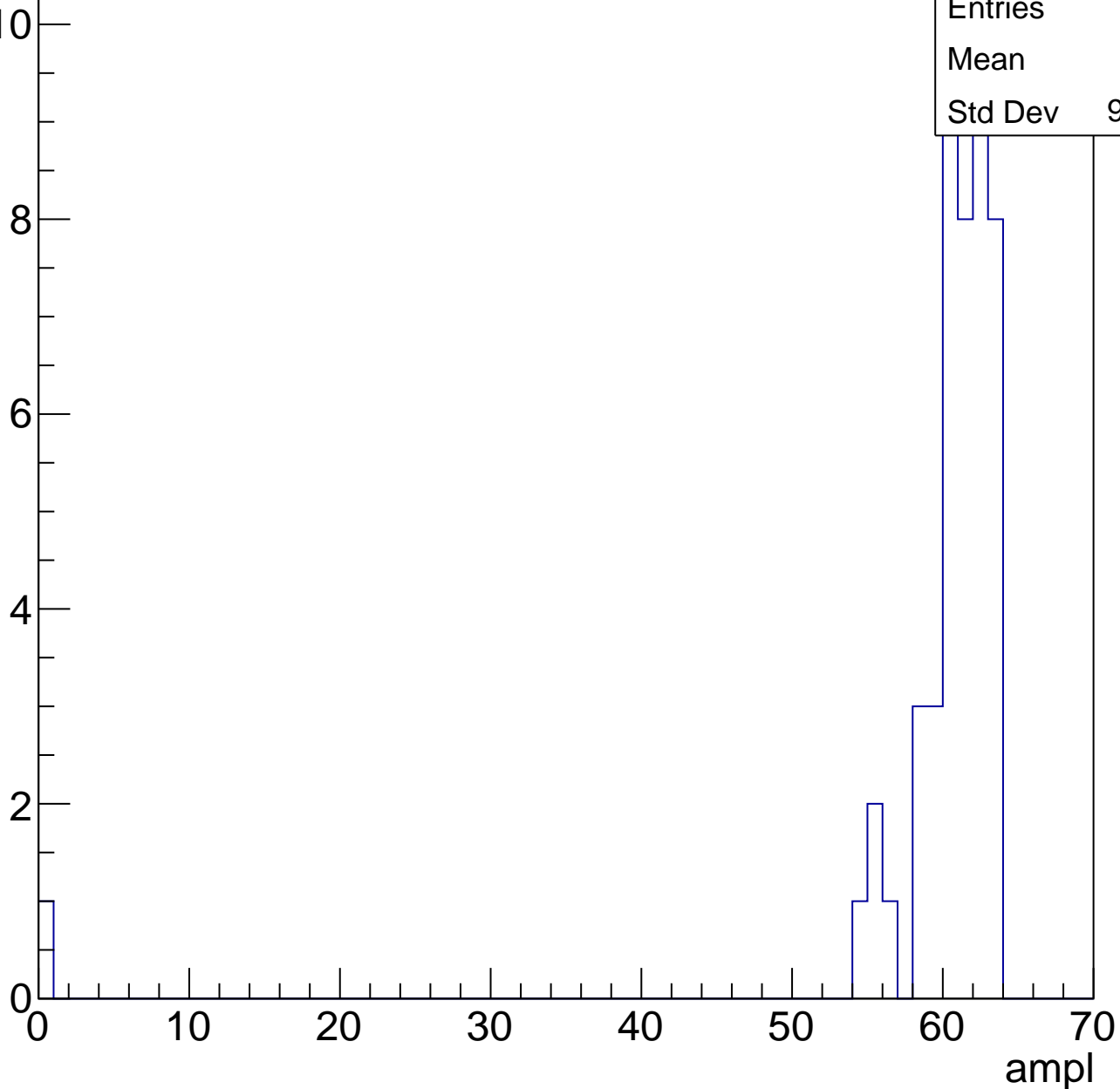


# B1L103S, U9-ch67, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	46
Mean	59.2
Std Dev	9.098



# B1L103S, U9-ch67, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



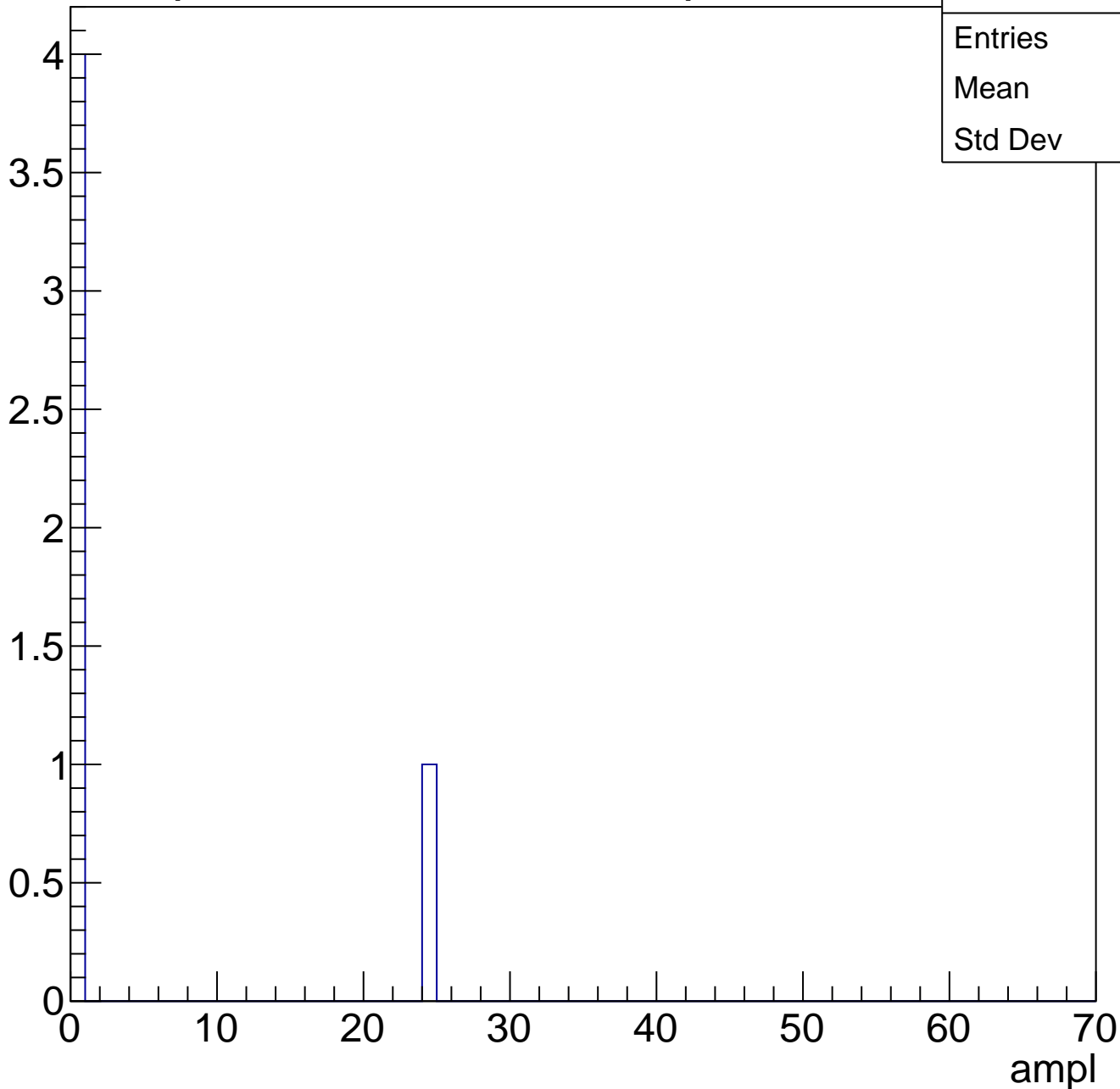
Entries	1
Mean	63
Std Dev	0



# B1L103S, U9-ch67, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U9-ch68, adc0

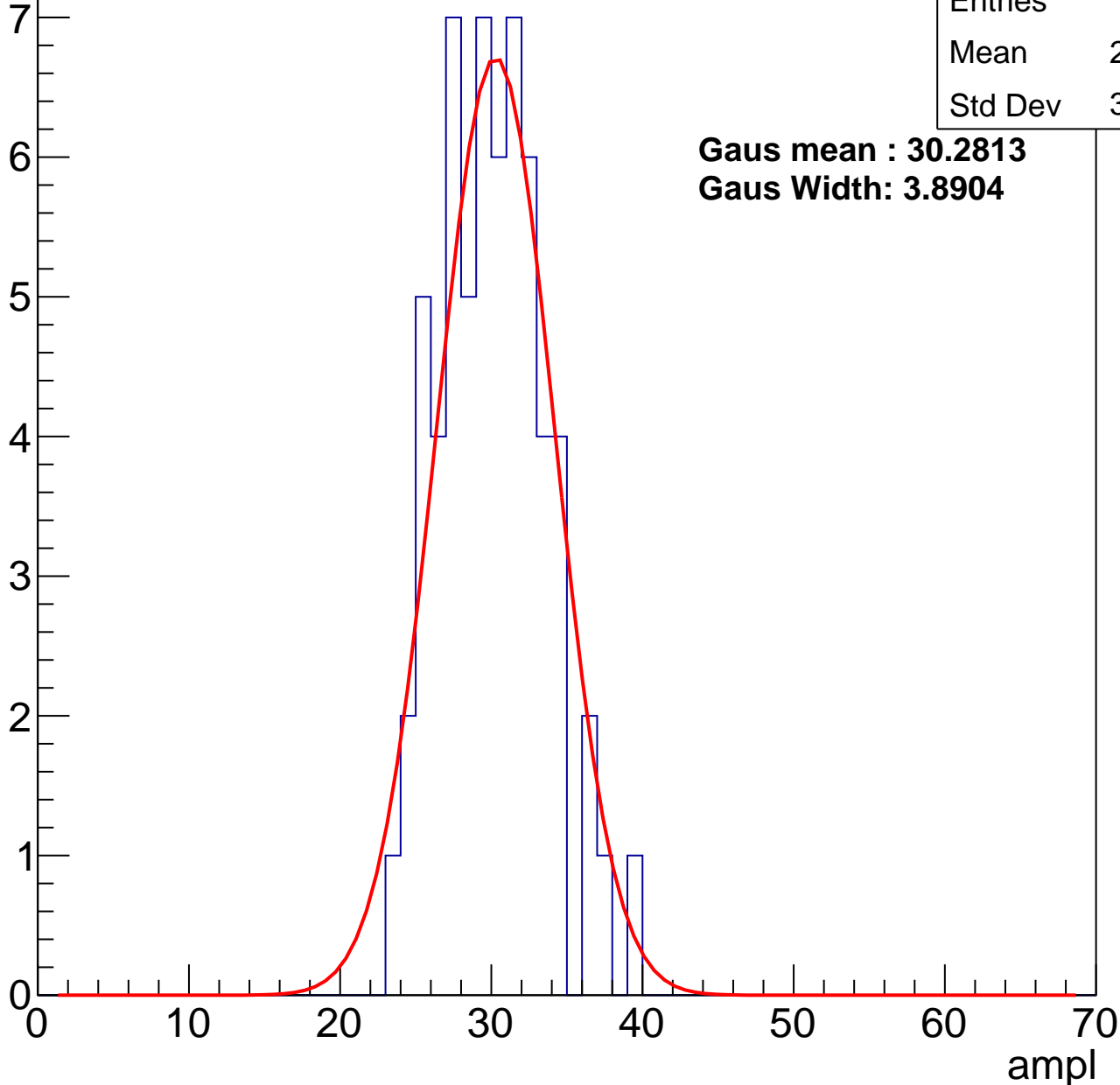
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	29.63
Std Dev	3.418

**Gaus mean : 30.2813**

**Gaus Width: 3.8904**



# B1L103S, U9-ch68, adc1

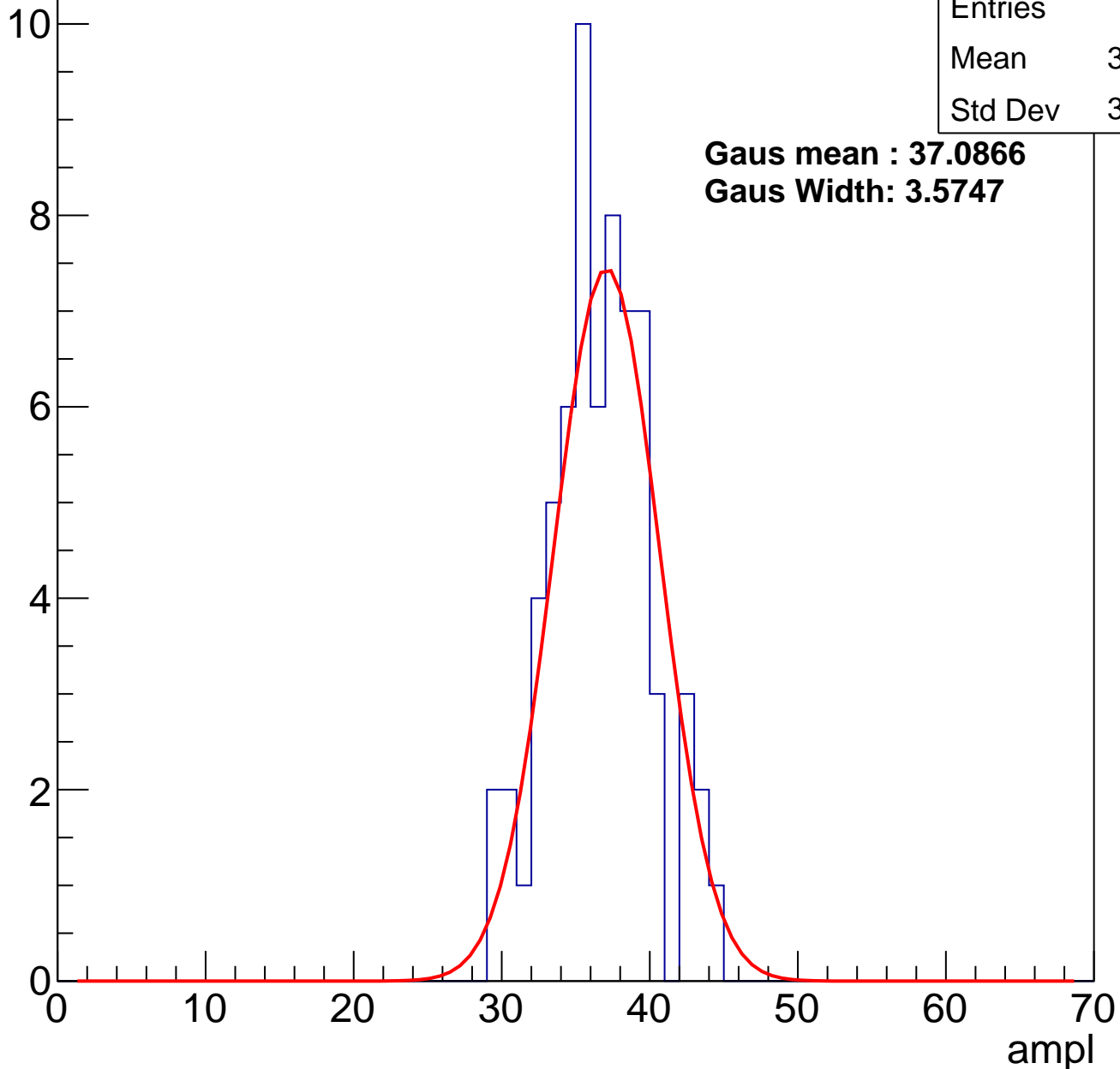
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	67
Mean	36.16
Std Dev	3.353

**Gaus mean : 37.0866**

**Gaus Width: 3.5747**

Entry



# B1L103S, U9-ch68, adc2

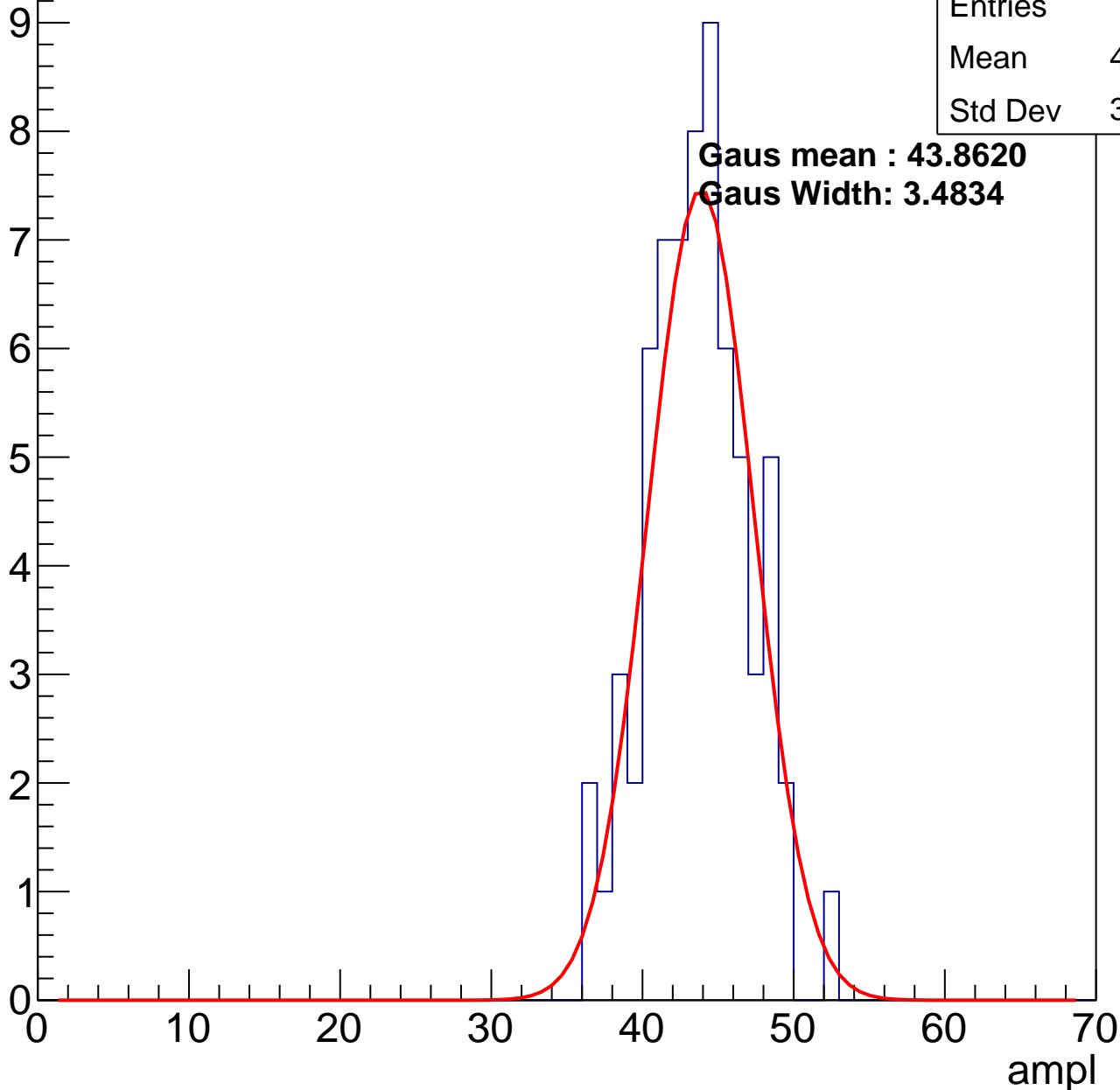
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	43.18
Std Dev	3.305

**Gaus mean : 43.8620**

**Gaus Width: 3.4834**

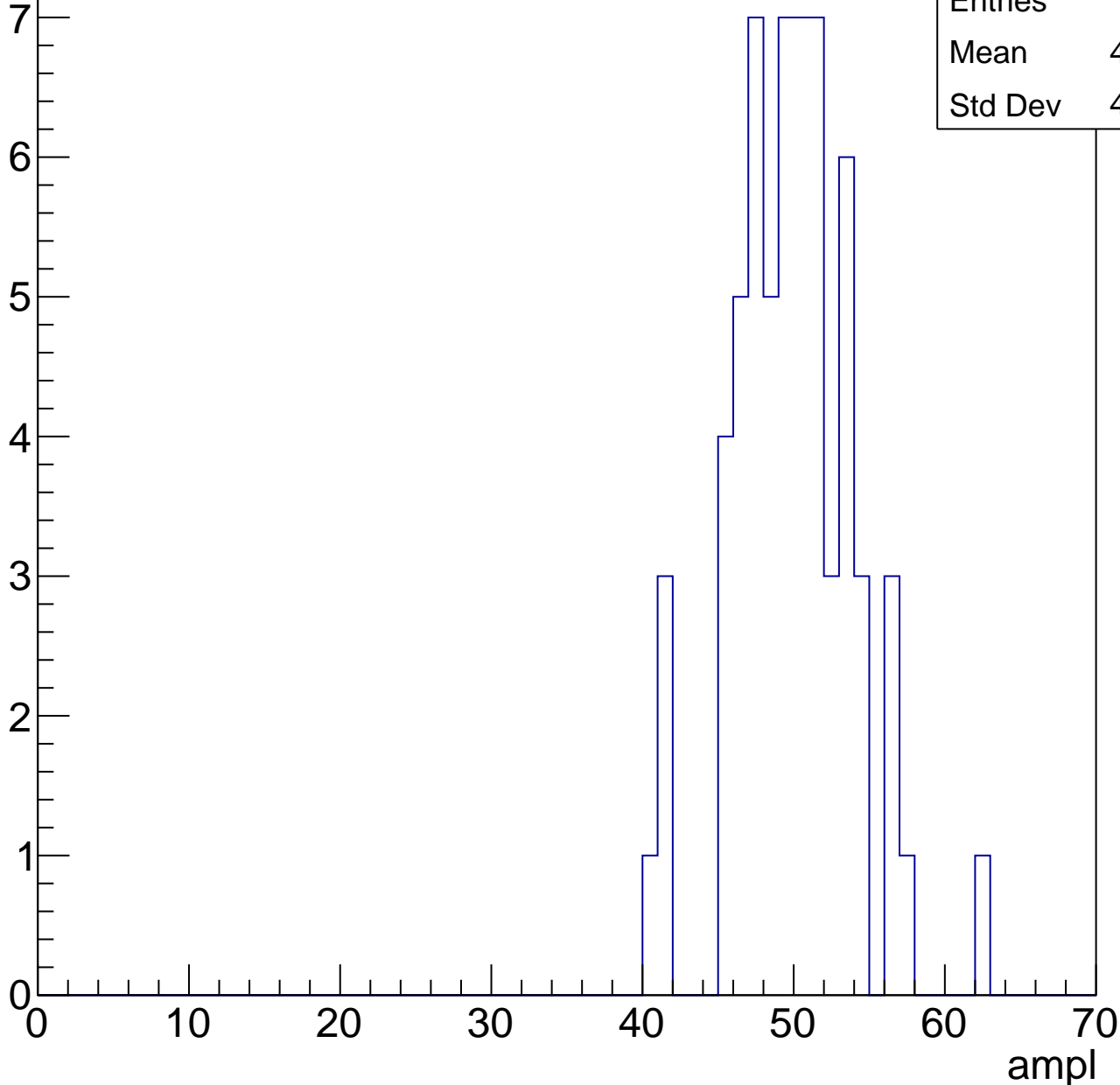


# B1L103S, U9-ch68, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

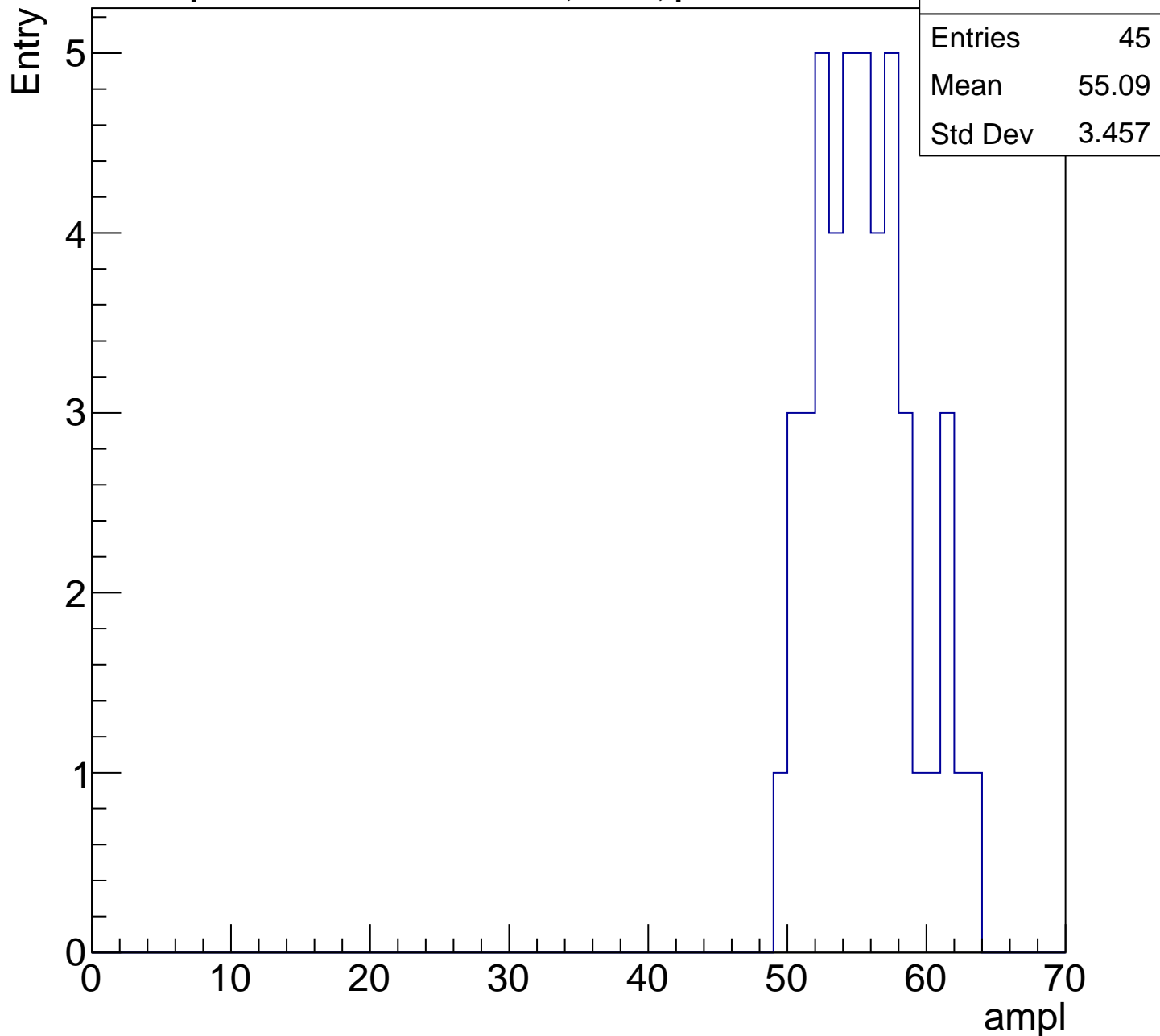
Entry

Entries	63
Mean	49.44
Std Dev	4.015



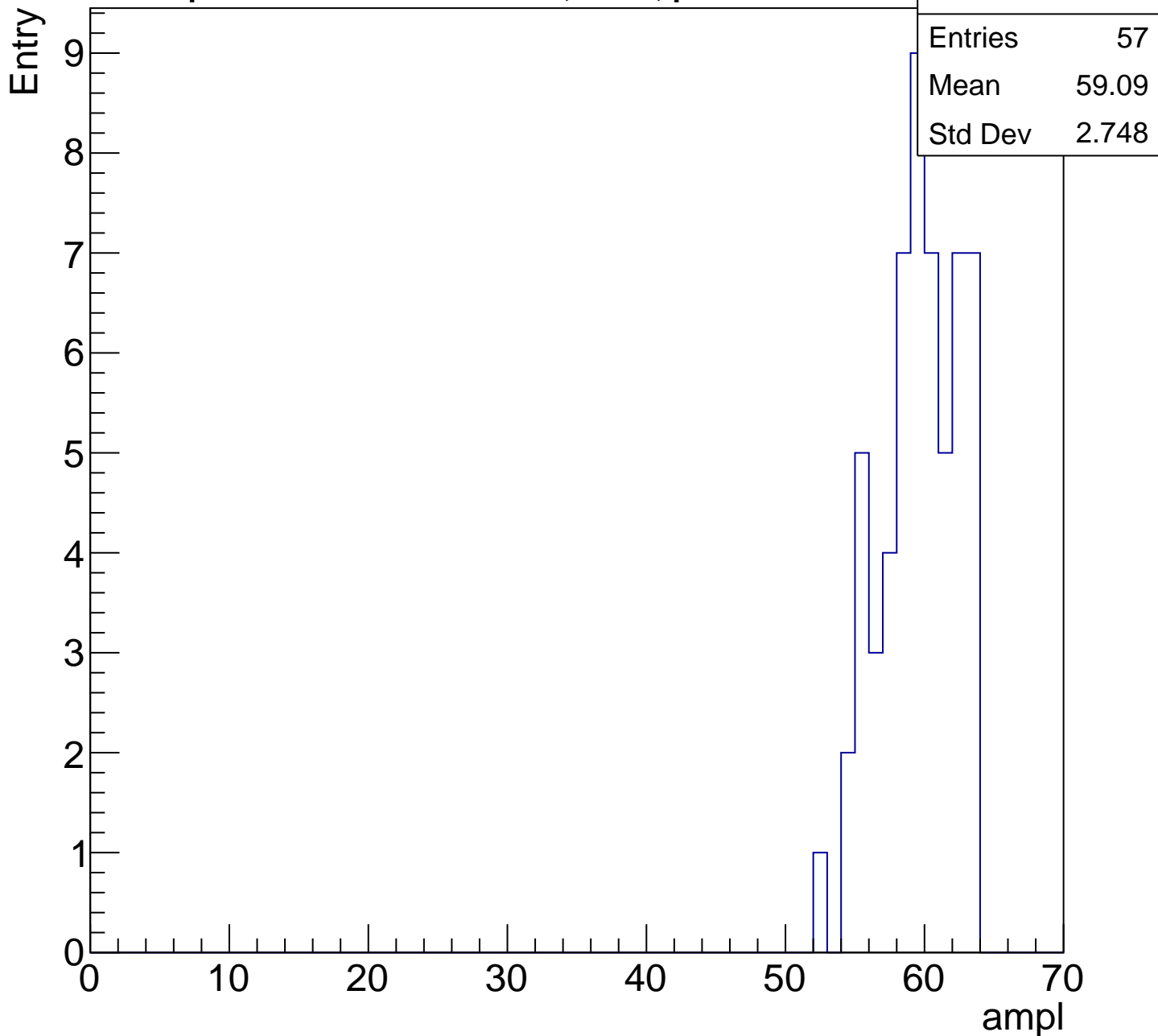
# B1L103S, U9-ch68, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U9-ch68, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U9-ch68, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

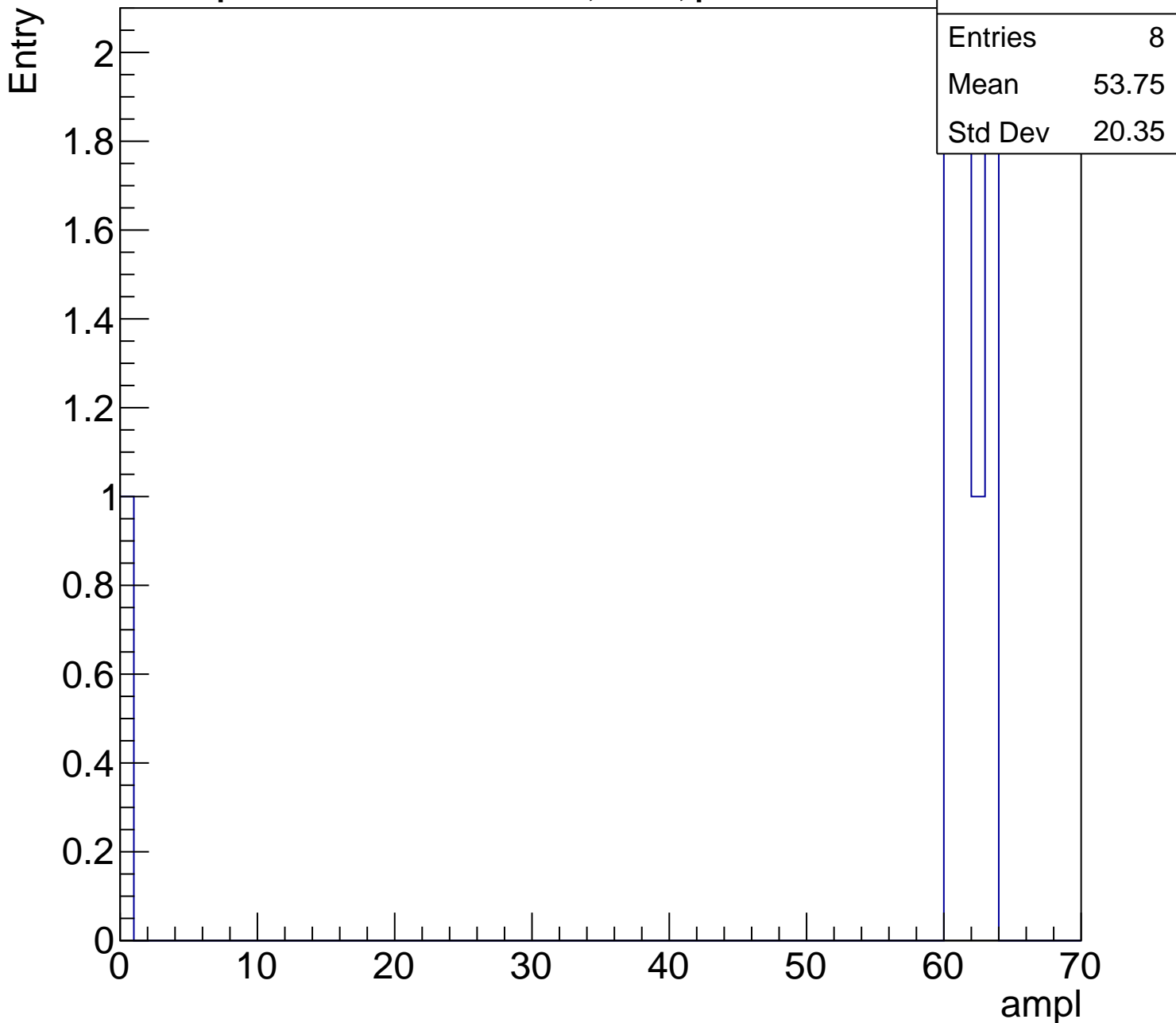
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	8
Mean	53.75
Std Dev	20.35

0 10 20 30 40 50 60 70

ampl





# B1L103S, U9-ch68, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

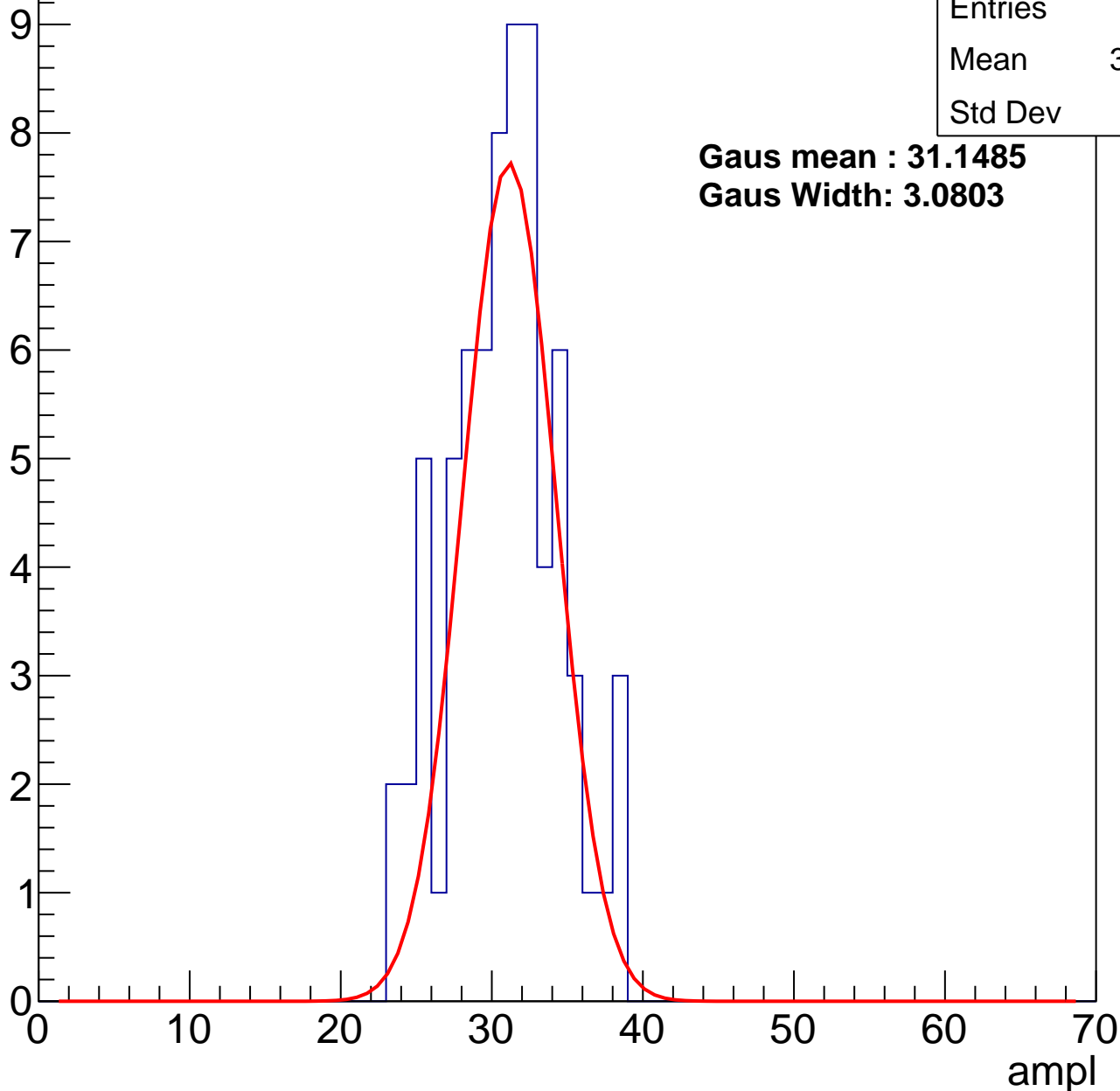
Entry



# B1L103S, U9-ch69, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U9-ch69, adc1

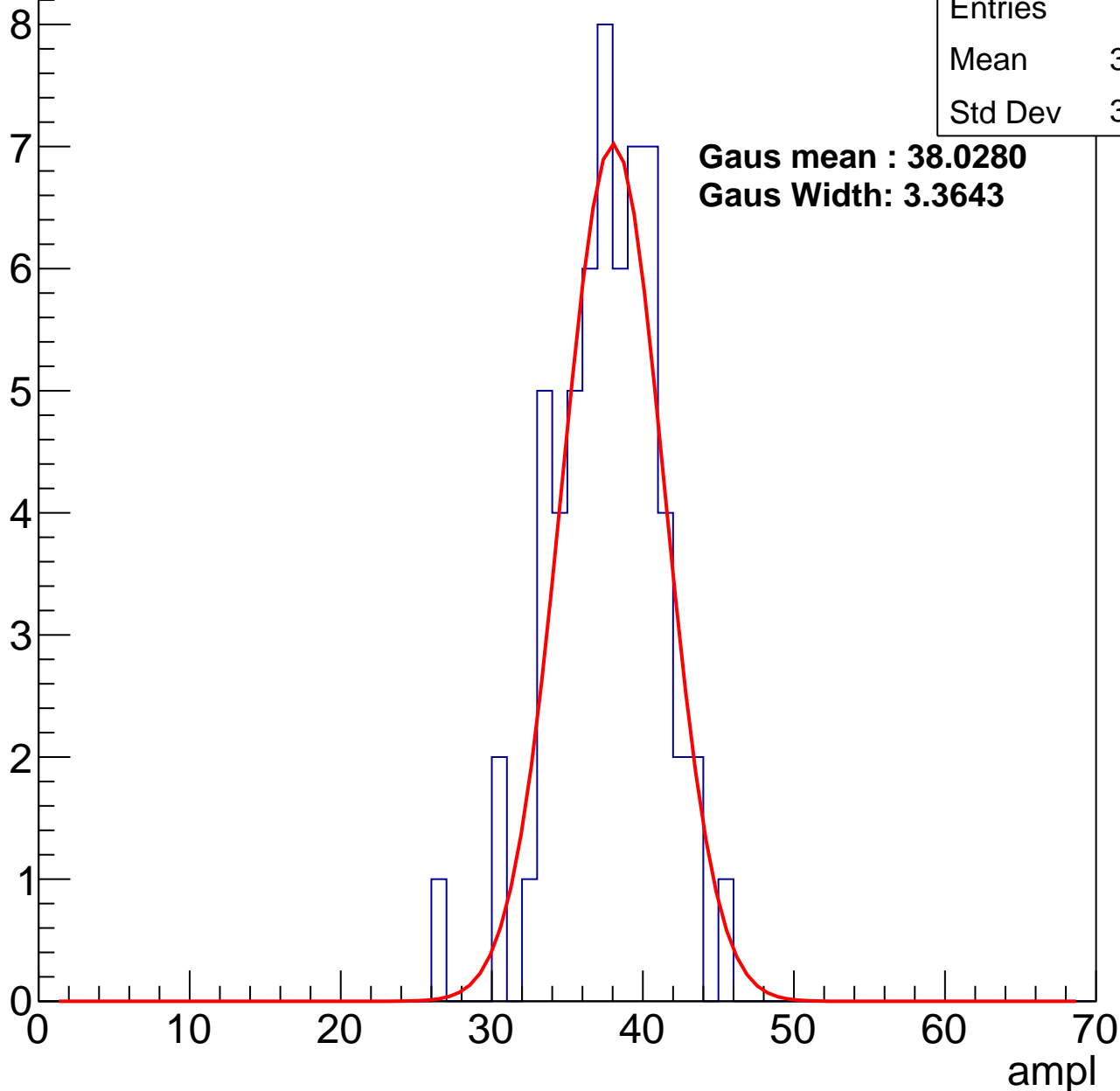
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	61
Mean	37.15
Std Dev	3.463

**Gaus mean : 38.0280**

**Gaus Width: 3.3643**



# B1L103S, U9-ch69, adc2

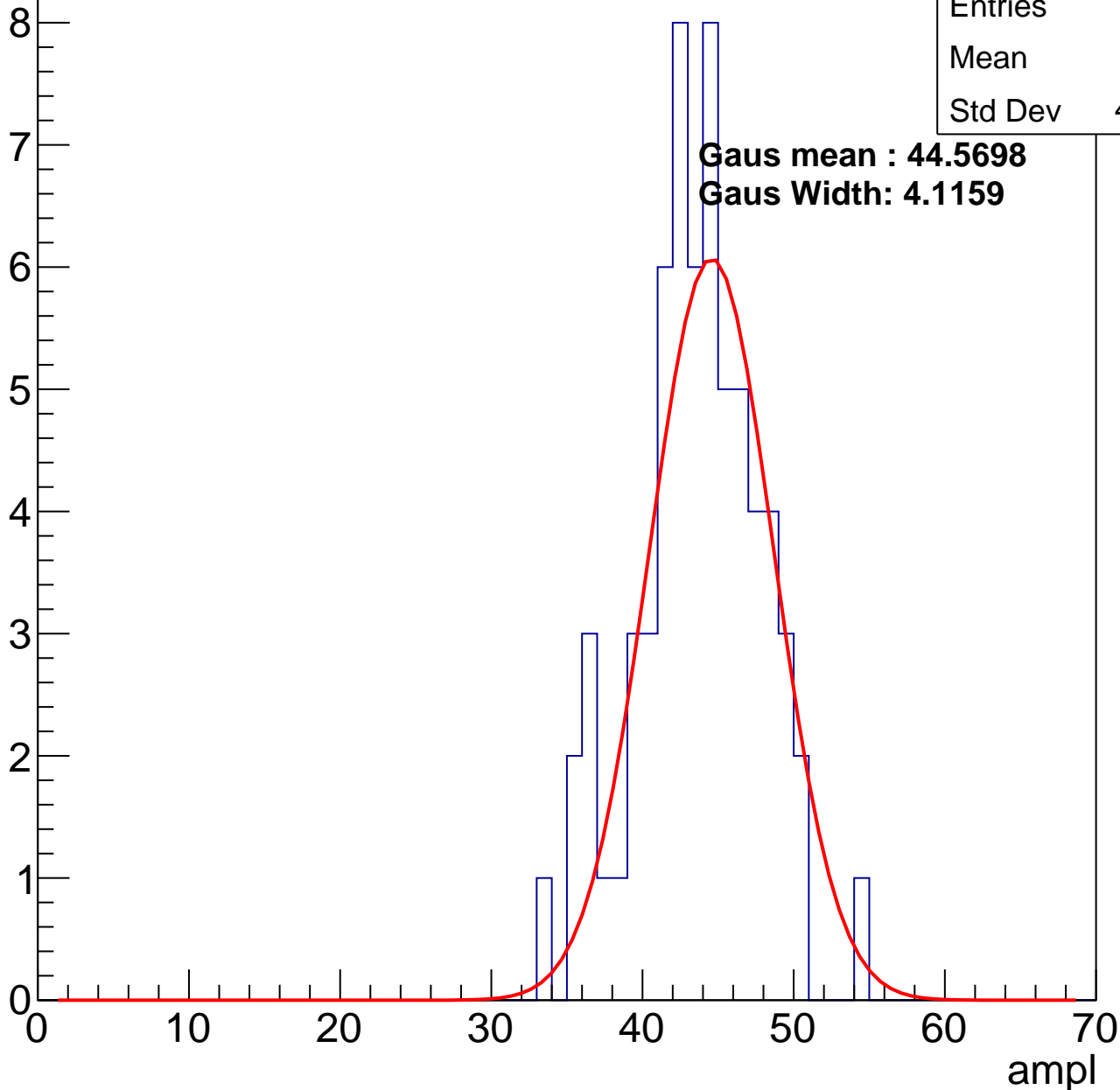
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	43.2
Std Dev	4.091

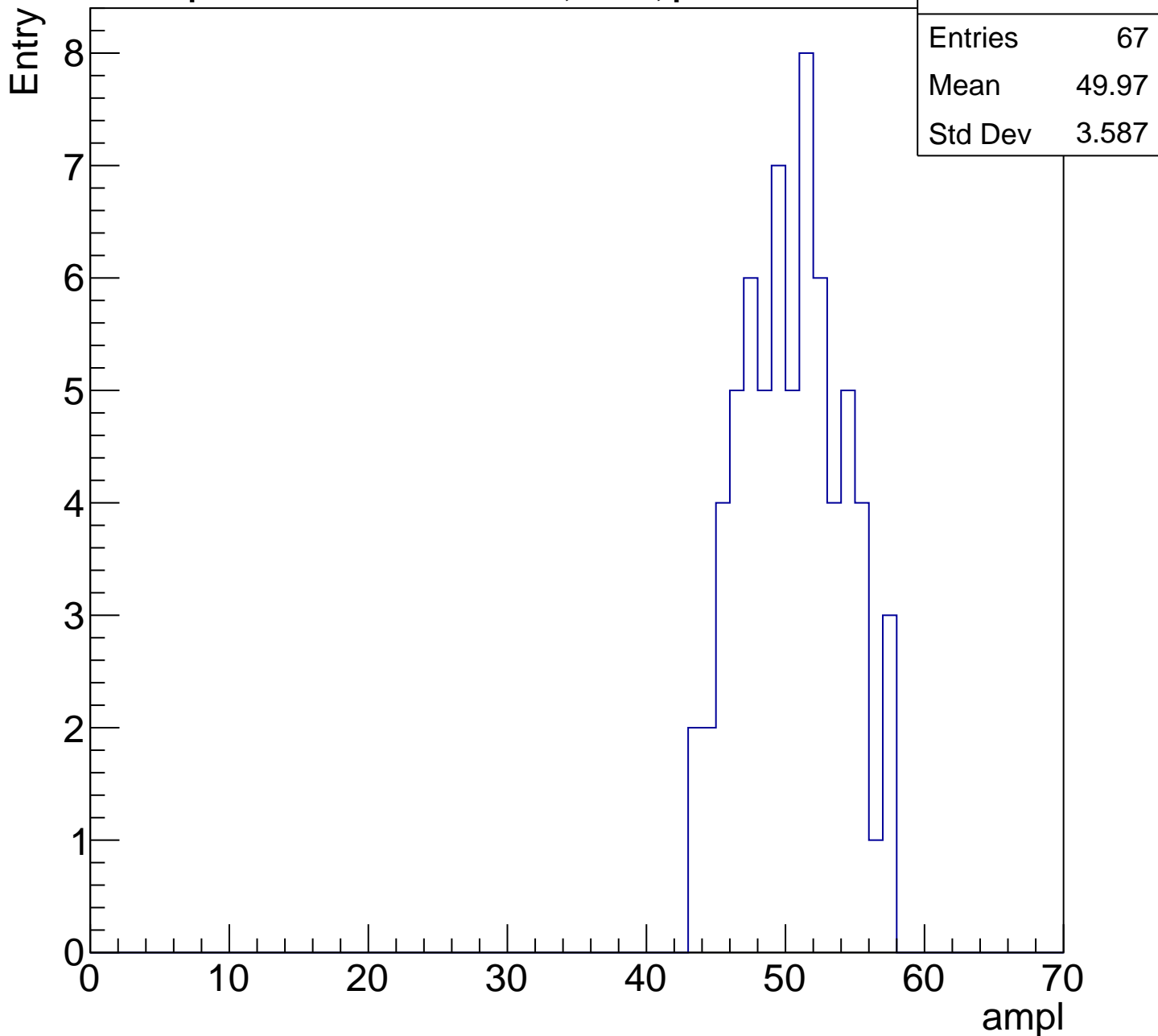
**Gaus mean : 44.5698**

**Gaus Width: 4.1159**



# B1L103S, U9-ch69, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

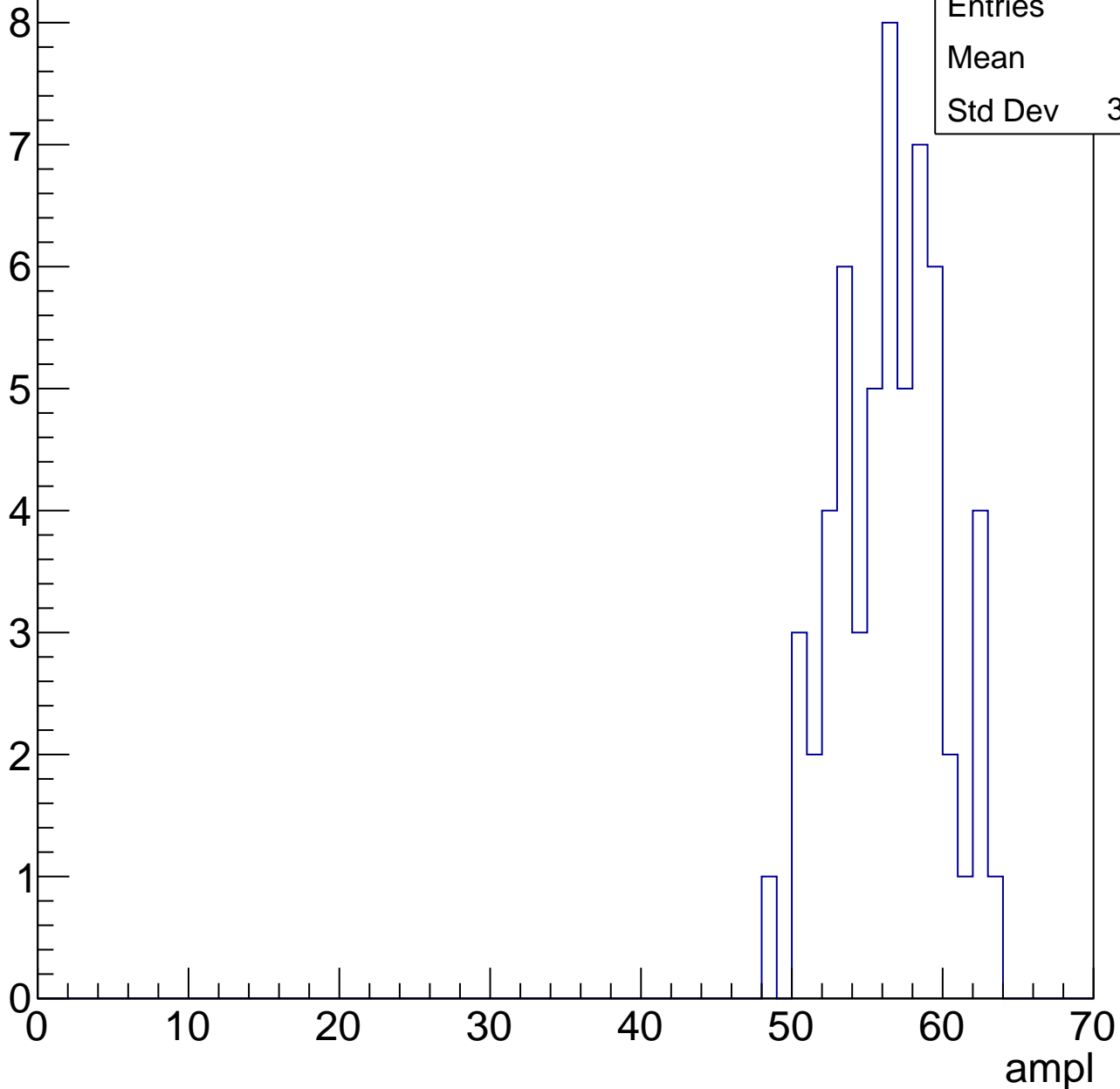


# B1L103S, U9-ch69, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	58
Mean	56
Std Dev	3.459

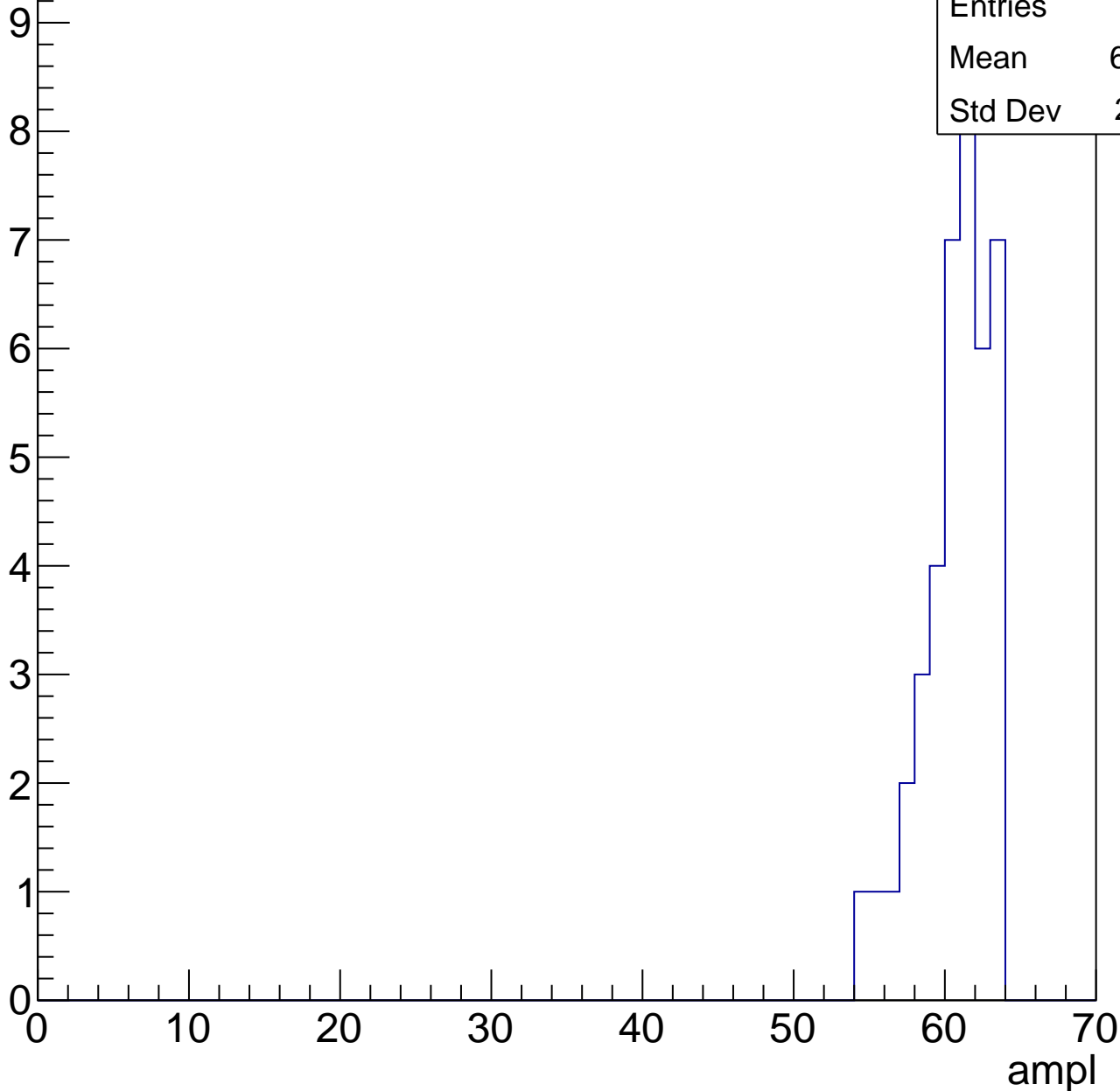


# B1L103S, U9-ch69, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

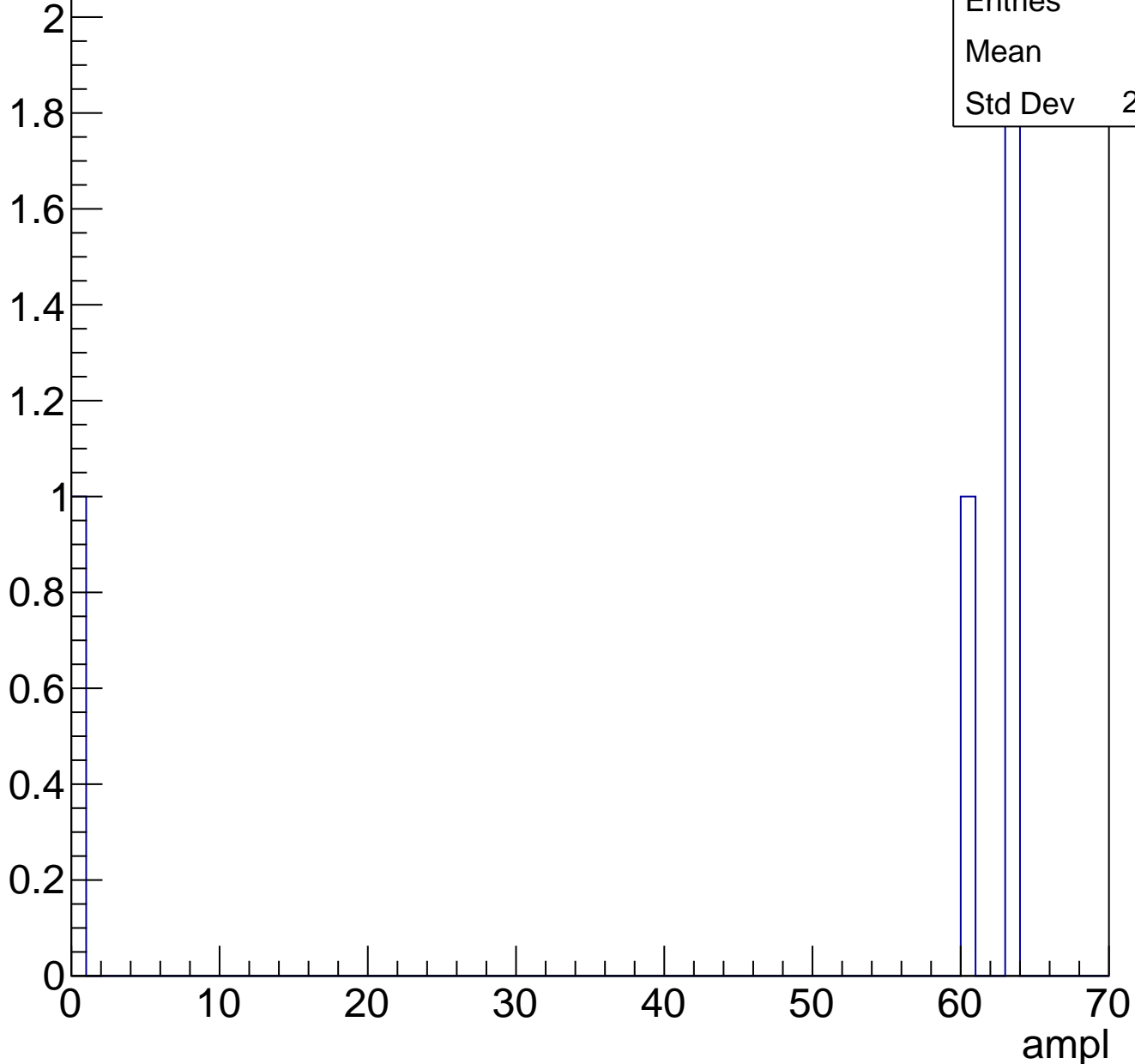
Entries	41
Mean	60.27
Std Dev	2.231



# B1L103S, U9-ch69, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U9-ch69, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U9-ch70, adc0

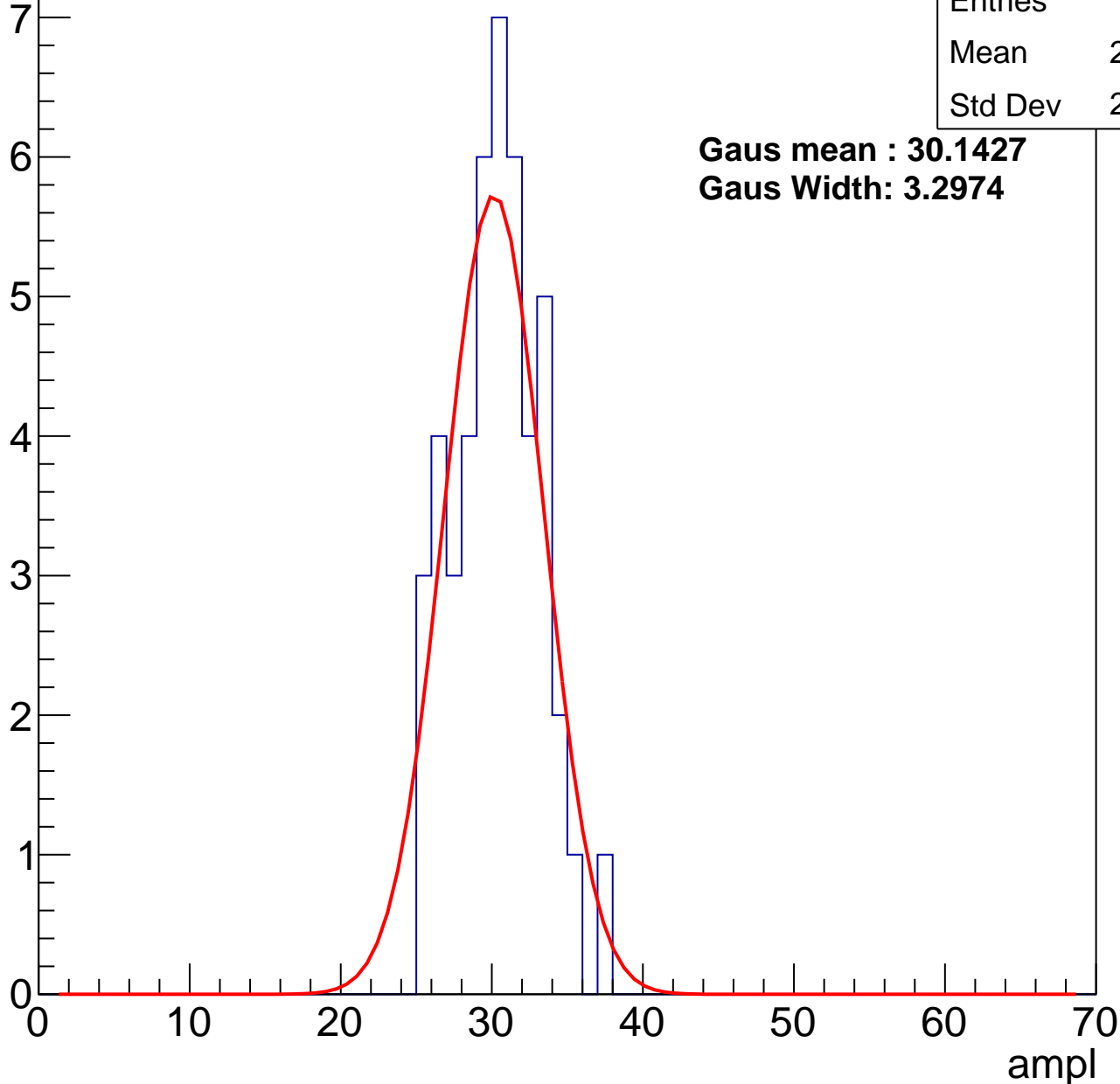
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	46
Mean	29.89
Std Dev	2.799

**Gaus mean : 30.1427**

**Gaus Width: 3.2974**



# B1L103S, U9-ch70, adc1

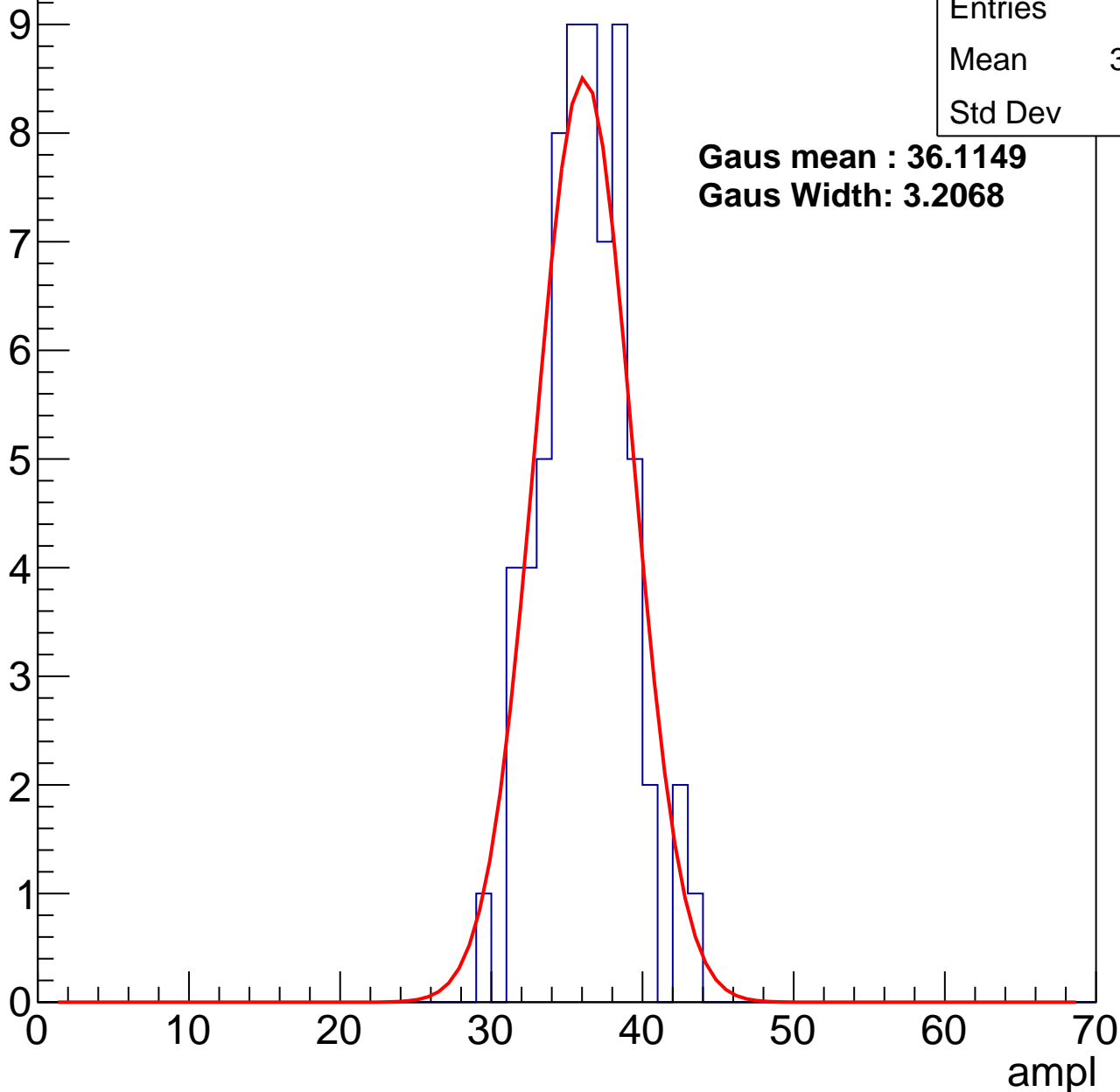
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	35.76
Std Dev	2.85

**Gaus mean : 36.1149**

**Gaus Width: 3.2068**



# B1L103S, U9-ch70, adc2

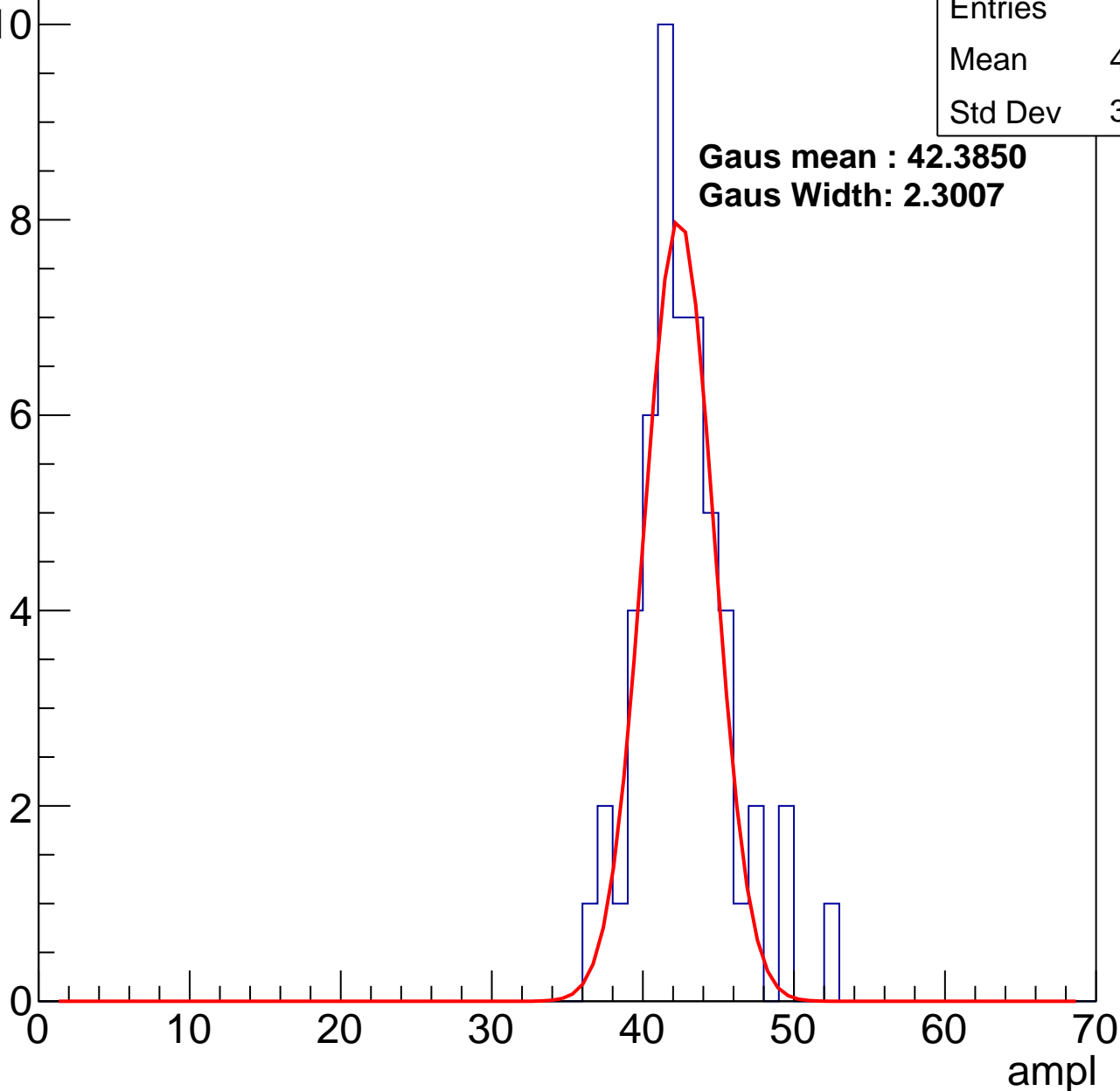
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	53
Mean	42.25
Std Dev	3.059

**Gaus mean : 42.3850**

**Gaus Width: 2.3007**

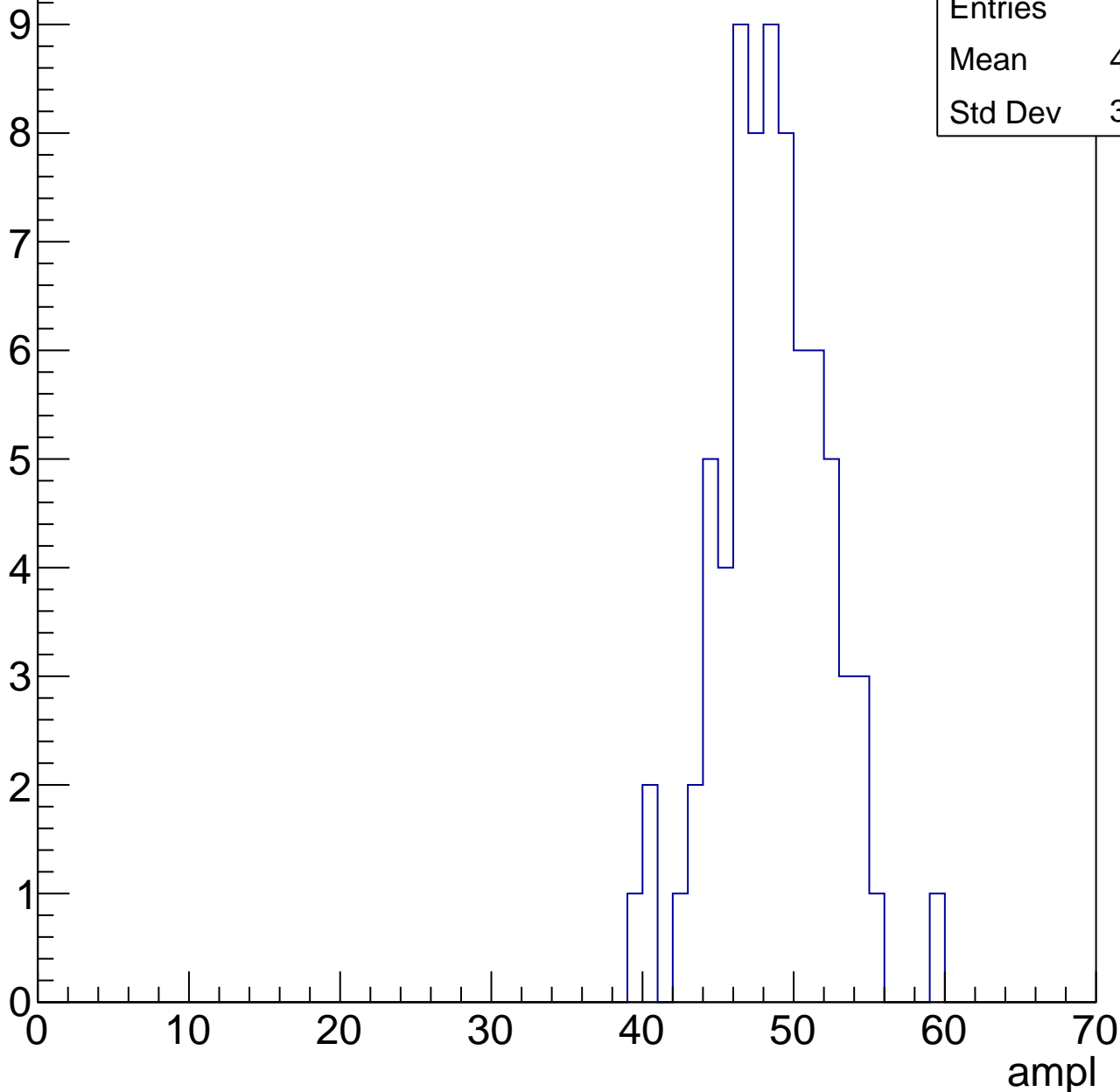


# B1L103S, U9-ch70, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	74
Mean	48.14
Std Dev	3.625



# B1L103S, U9-ch70, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	64
Mean	54.98
Std Dev	3.706

Entry

10

8

6

4

2

0

0

10

20

30

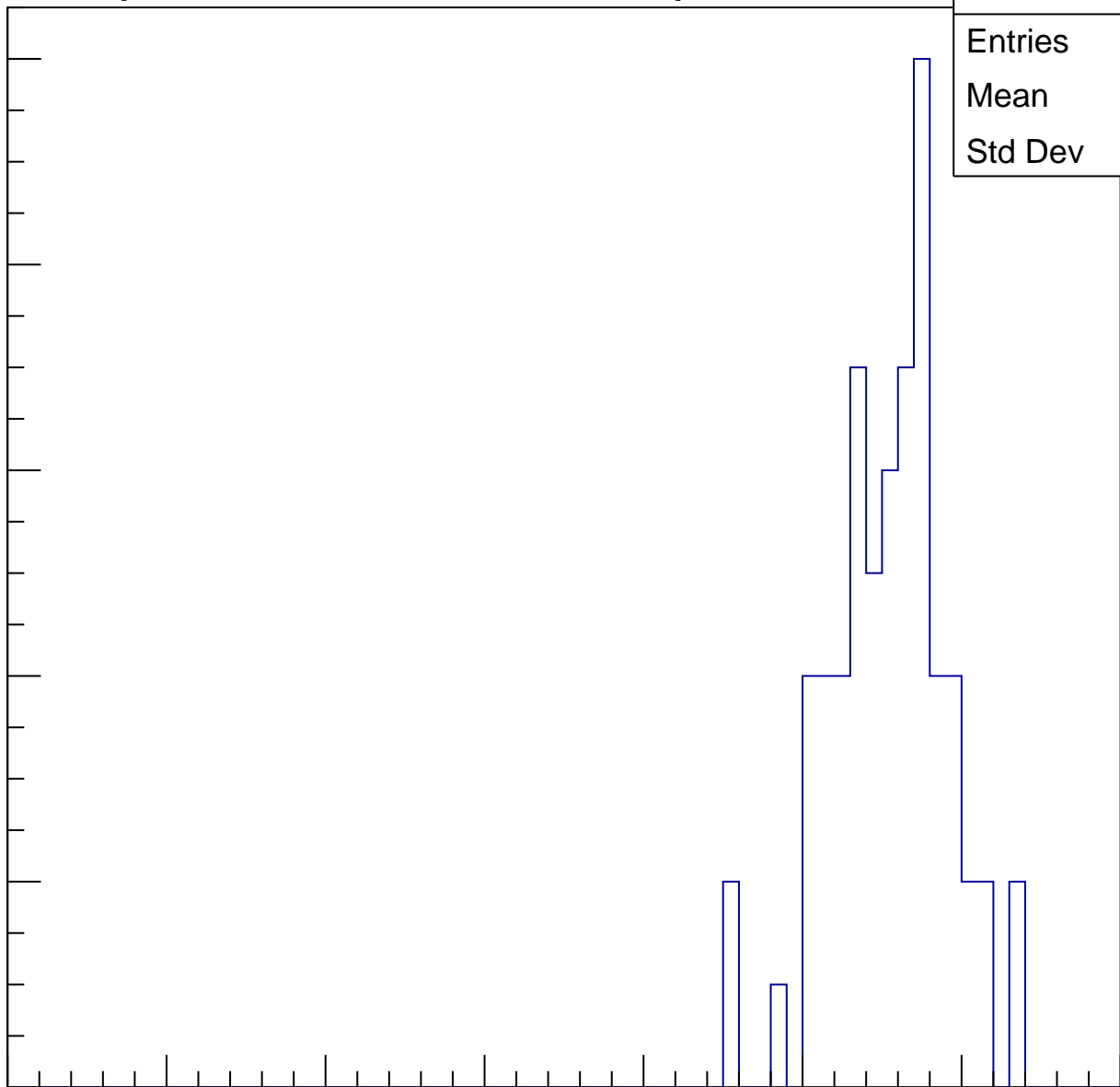
40

50

60

70

ampl

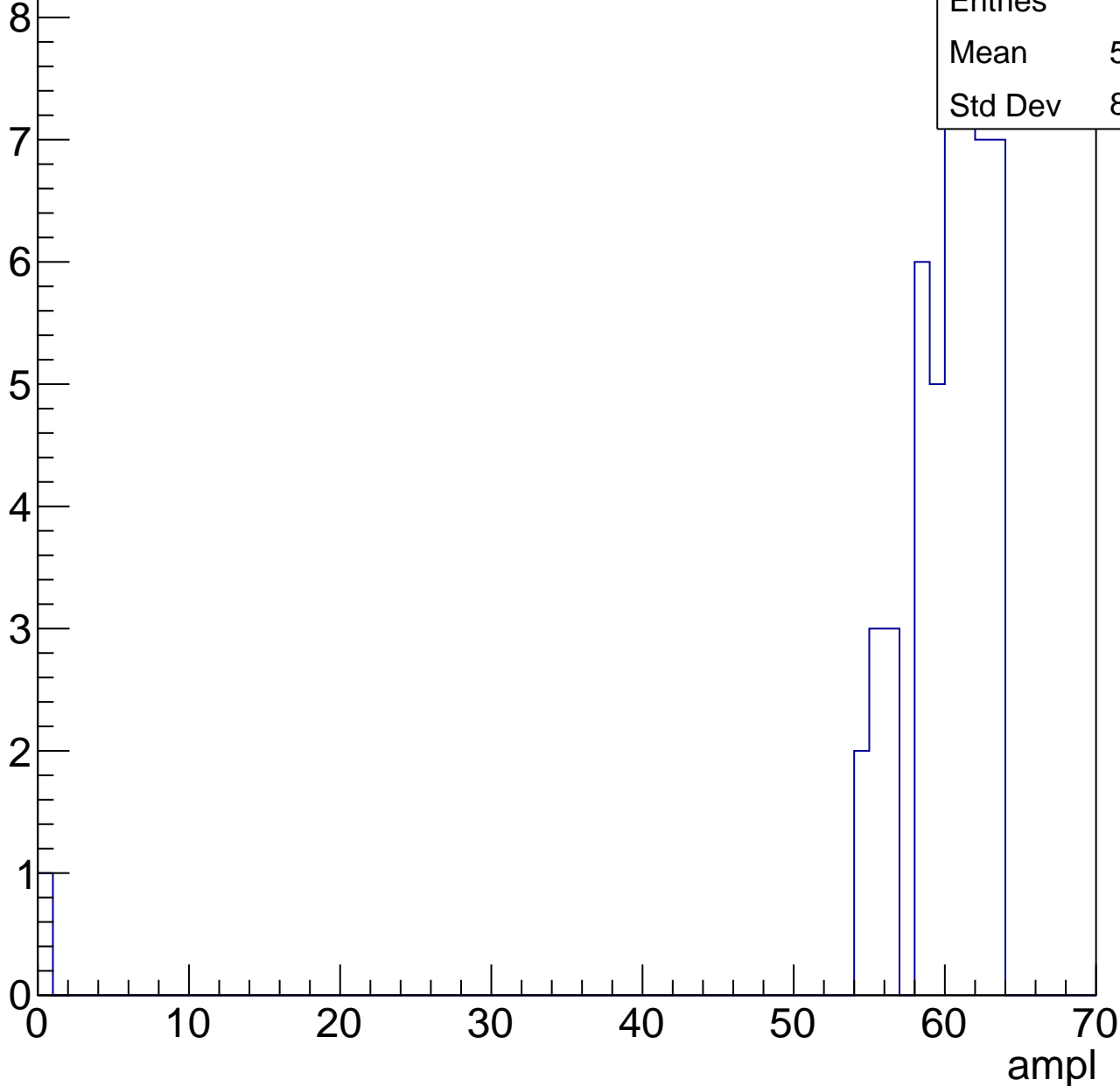


# B1L103S, U9-ch70, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

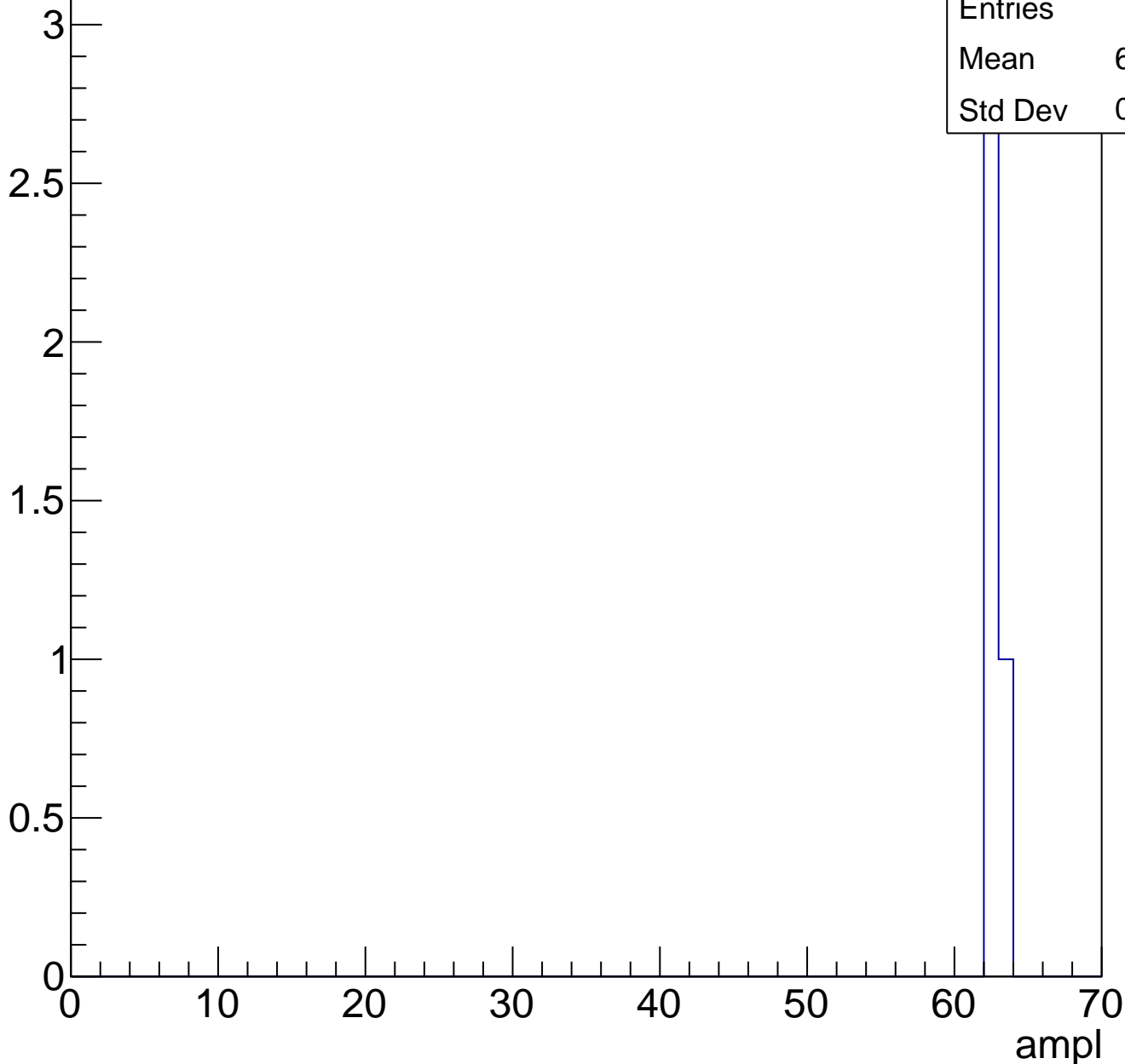
Entries	50
Mean	58.54
Std Dev	8.737



# B1L103S, U9-ch70, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U9-ch70, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U9-ch71, adc0

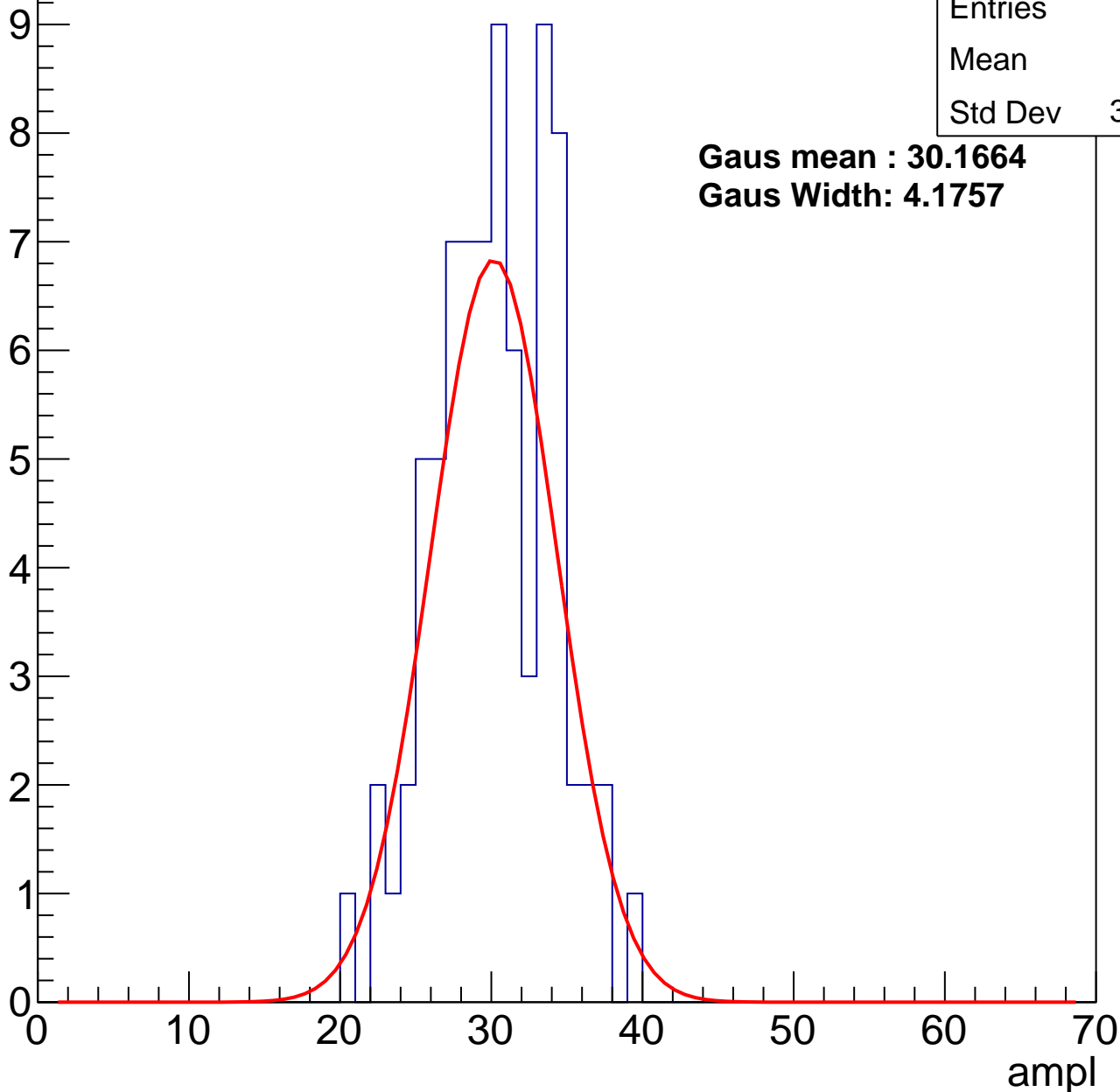
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	79
Mean	29.8
Std Dev	3.859

**Gaus mean : 30.1664**

**Gaus Width: 4.1757**



# B1L103S, U9-ch71, adc1

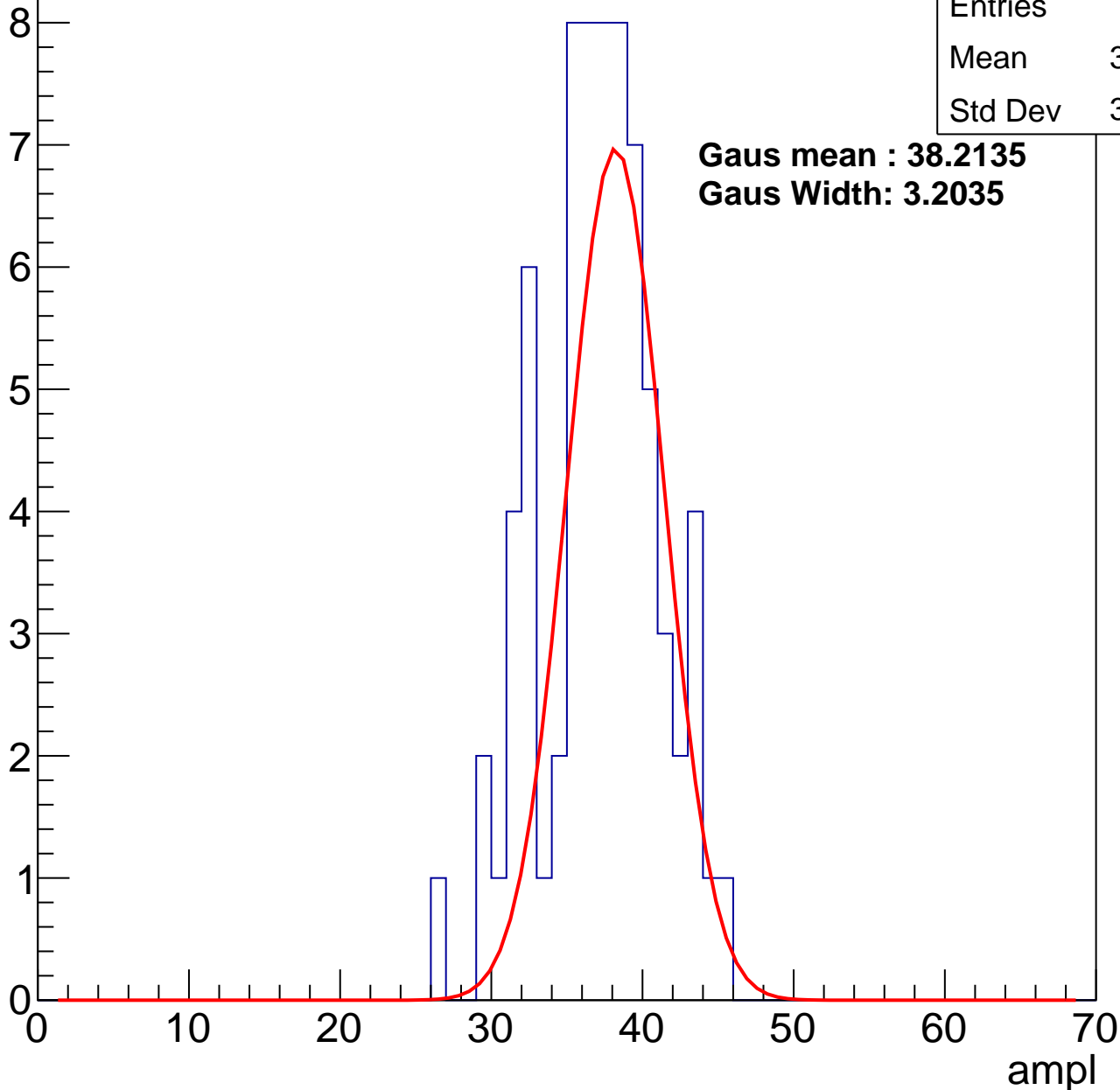
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	72
Mean	36.67
Std Dev	3.898

**Gaus mean : 38.2135**

**Gaus Width: 3.2035**



# B1L103S, U9-ch71, adc2

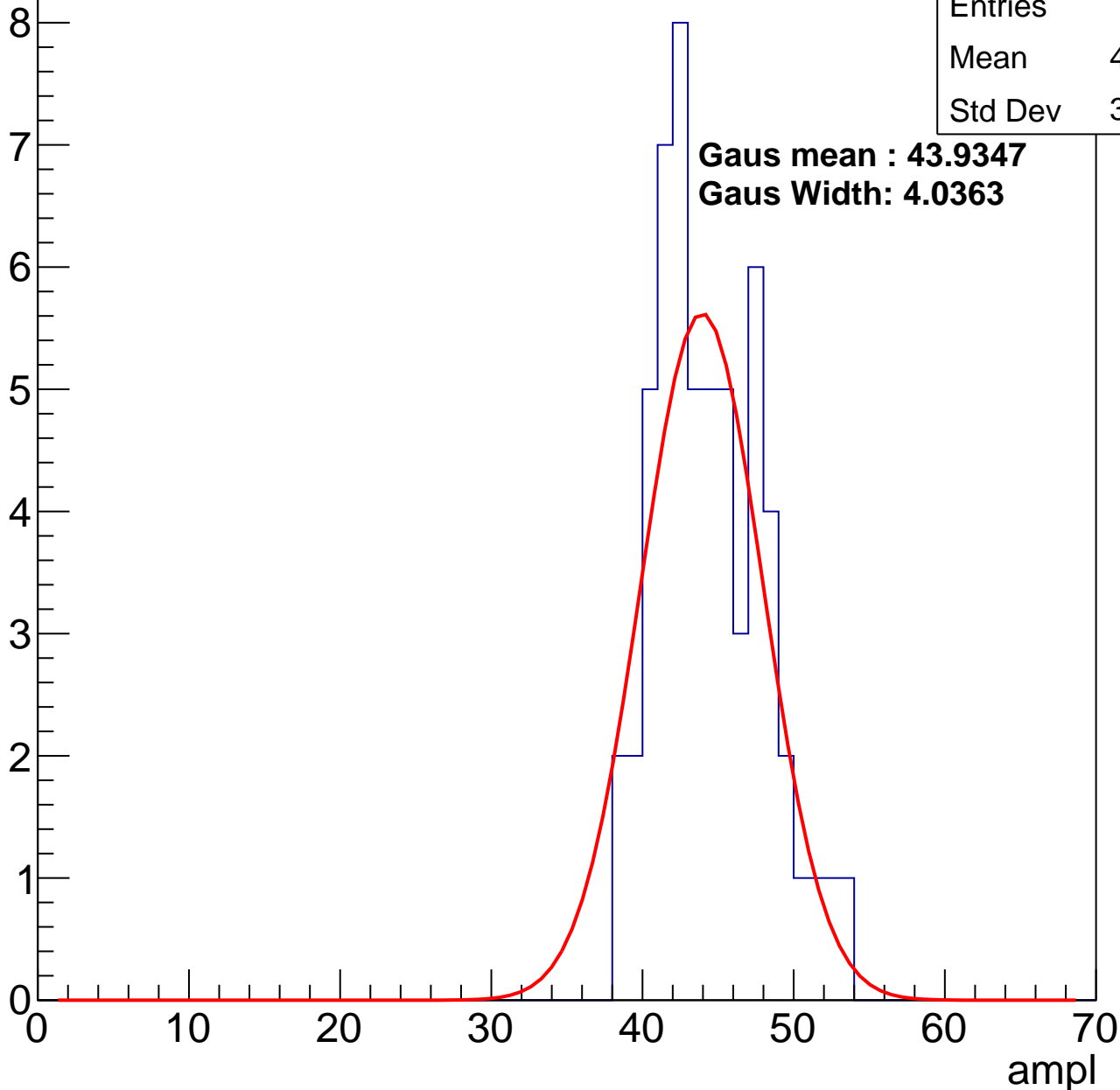
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	58
Mean	44.02
Std Dev	3.516

**Gaus mean : 43.9347**

**Gaus Width: 4.0363**

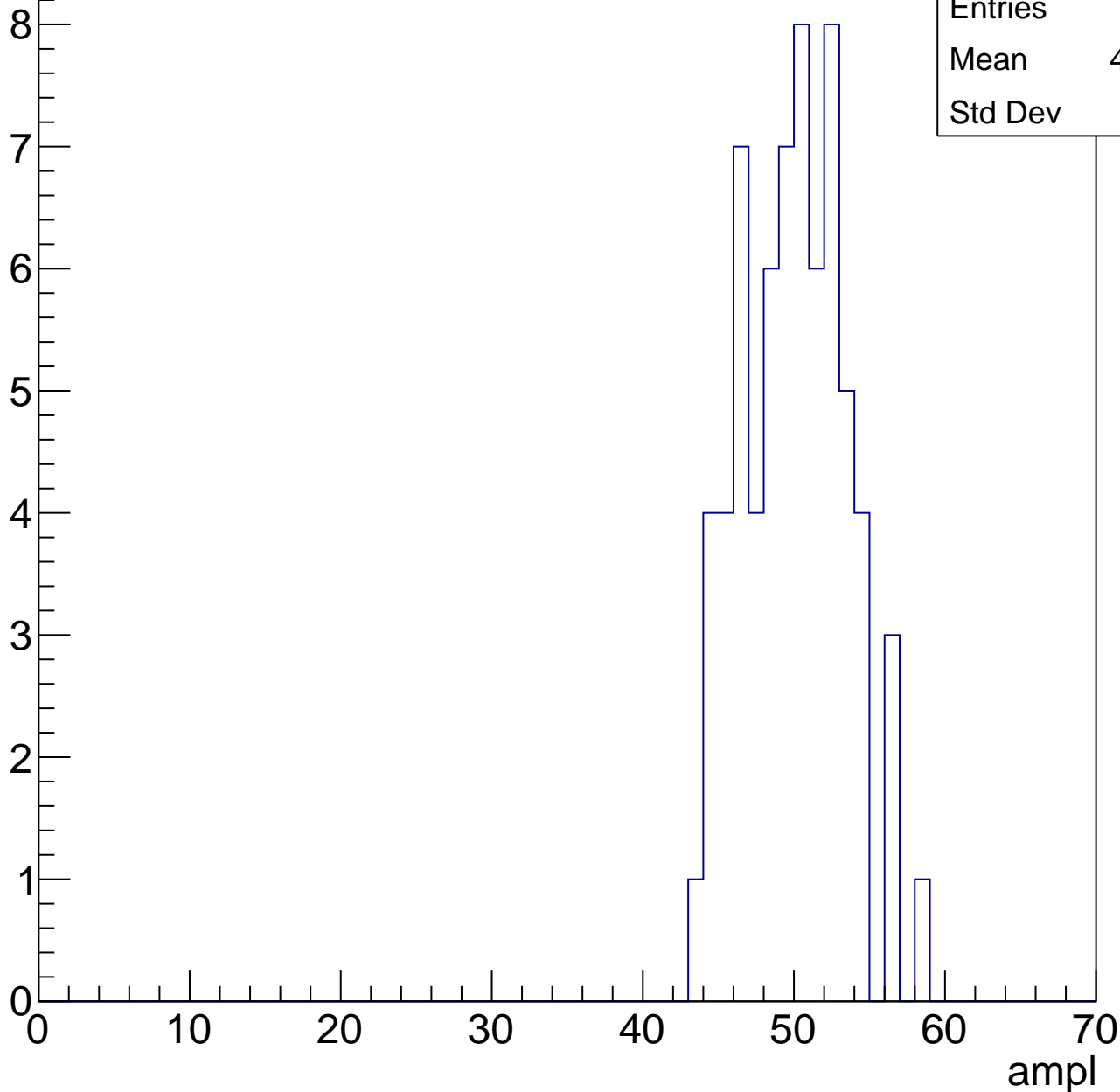


# B1L103S, U9-ch71, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	68
Mean	49.54
Std Dev	3.38

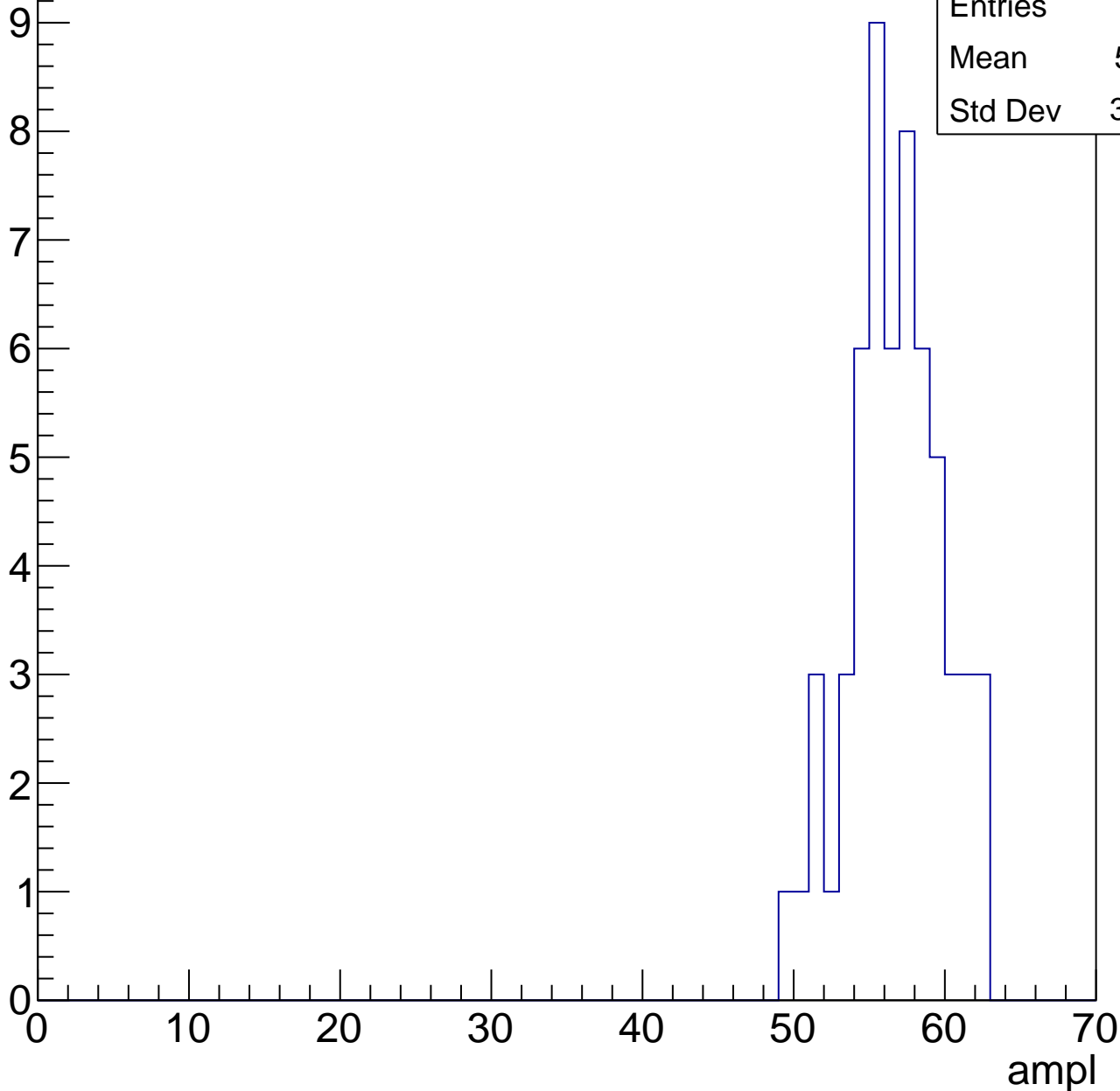


# B1L103S, U9-ch71, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	58
Mean	56.31
Std Dev	3.047

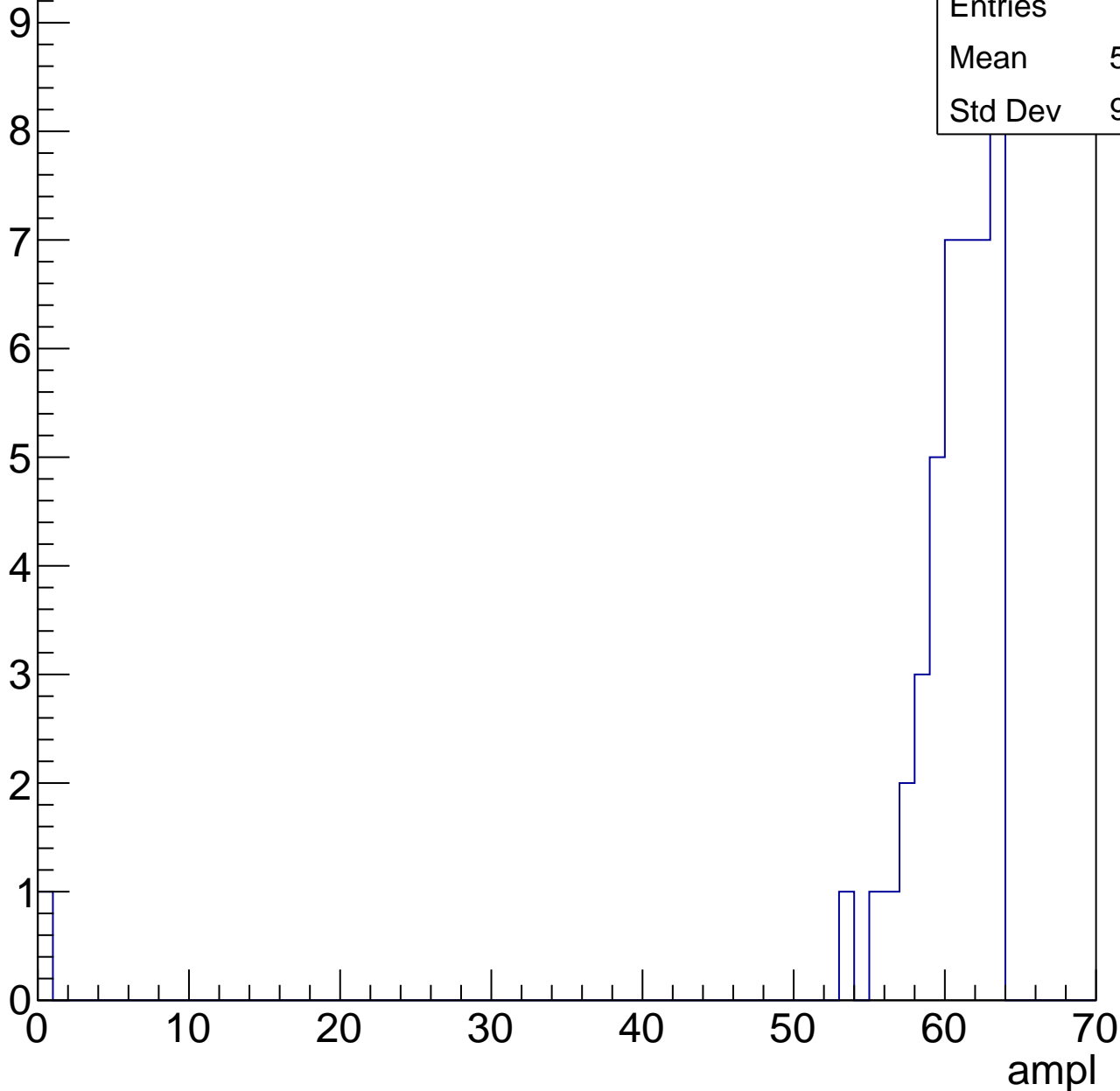


# B1L103S, U9-ch71, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	44
Mean	58.98
Std Dev	9.287



# B1L103S, U9-ch71, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U9-ch71, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U9-ch72, adc0

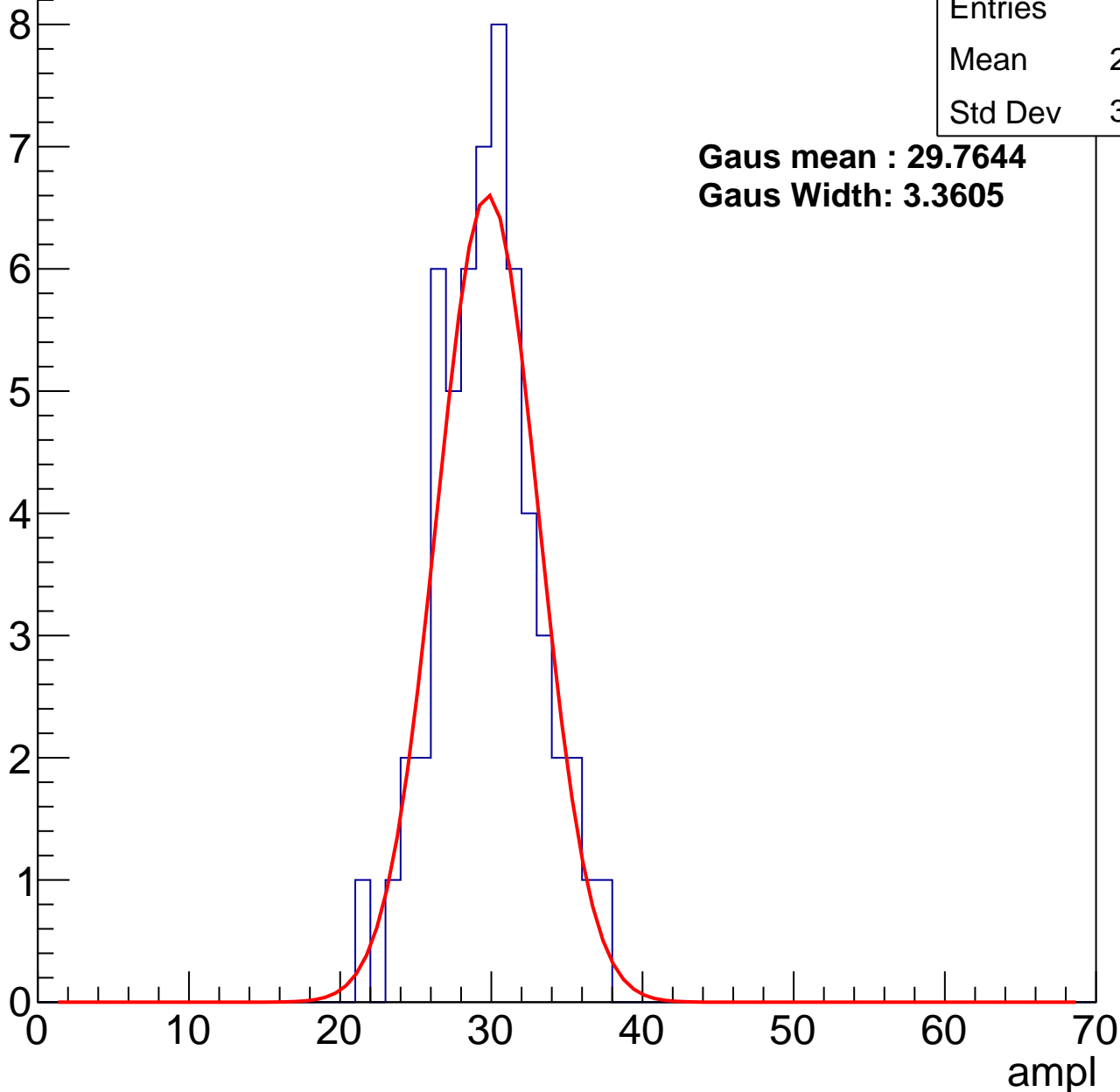
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	57
Mean	29.26
Std Dev	3.269

**Gaus mean : 29.7644**

**Gaus Width: 3.3605**



# B1L103S, U9-ch72, adc1

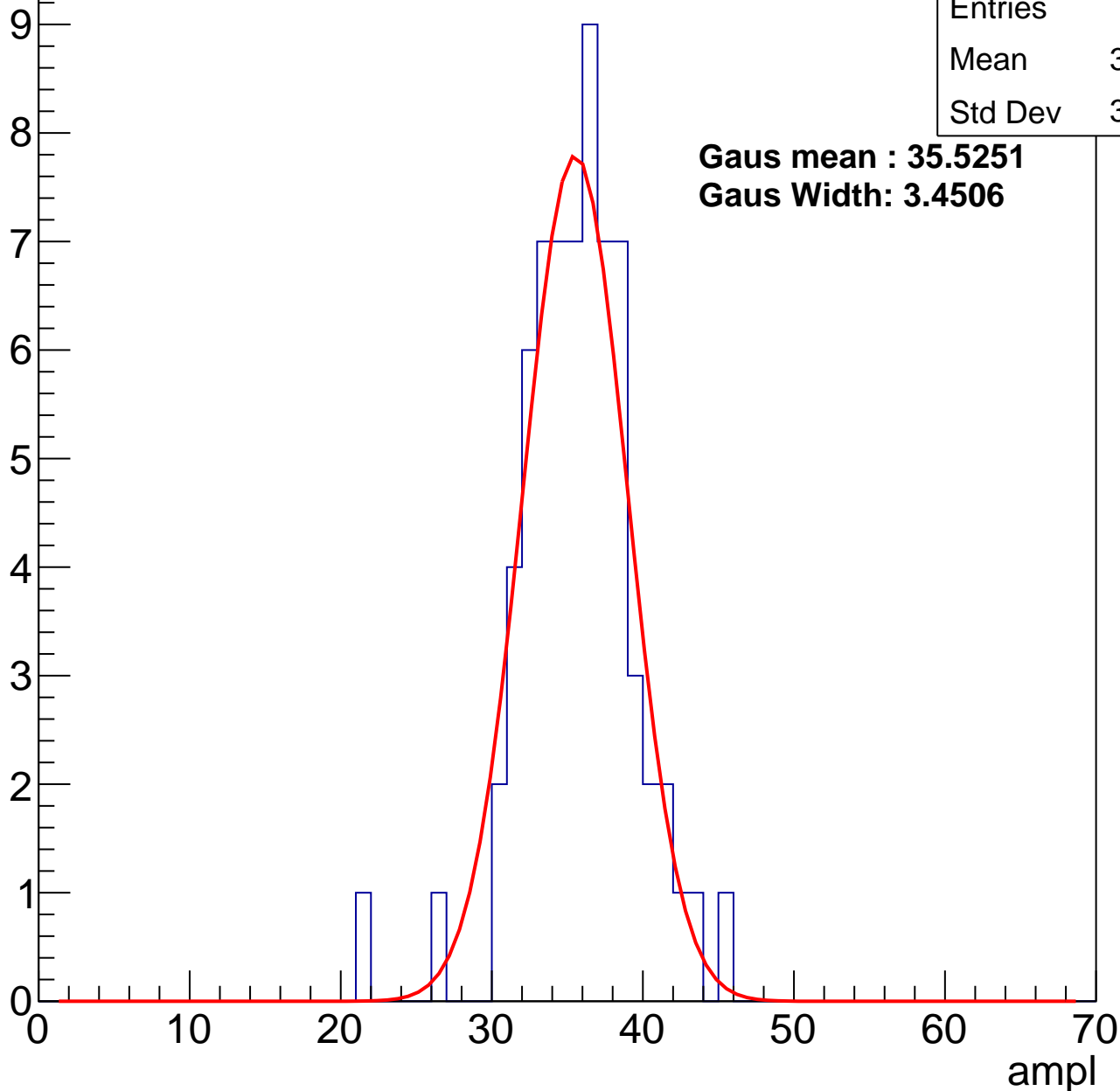
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	68
Mean	35.22
Std Dev	3.757

**Gaus mean : 35.5251**

**Gaus Width: 3.4506**



# B1L103S, U9-ch72, adc2

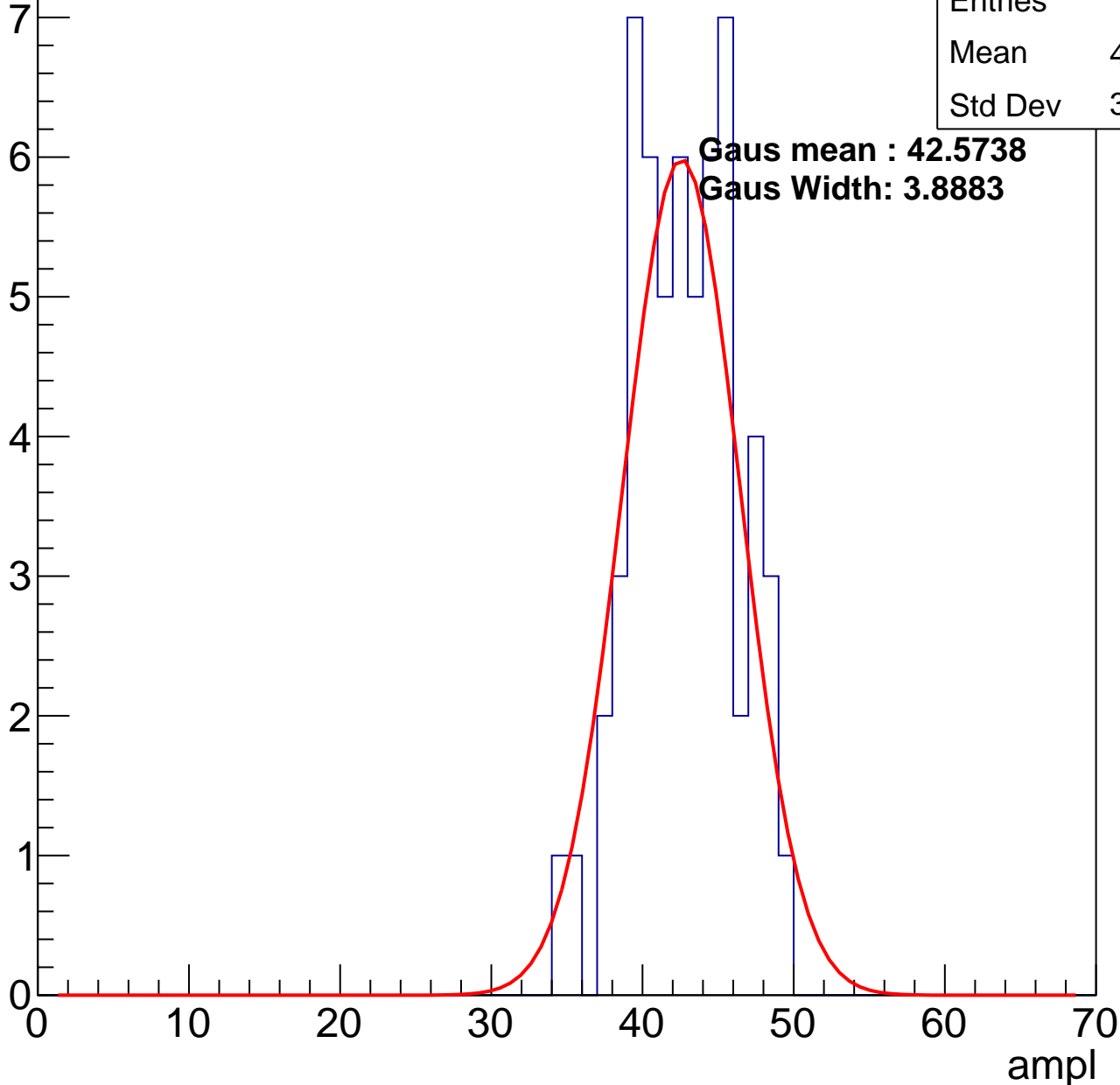
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	59
Mean	42.27
Std Dev	3.394

**Gaus mean : 42.5738**

**Gaus Width: 3.8883**

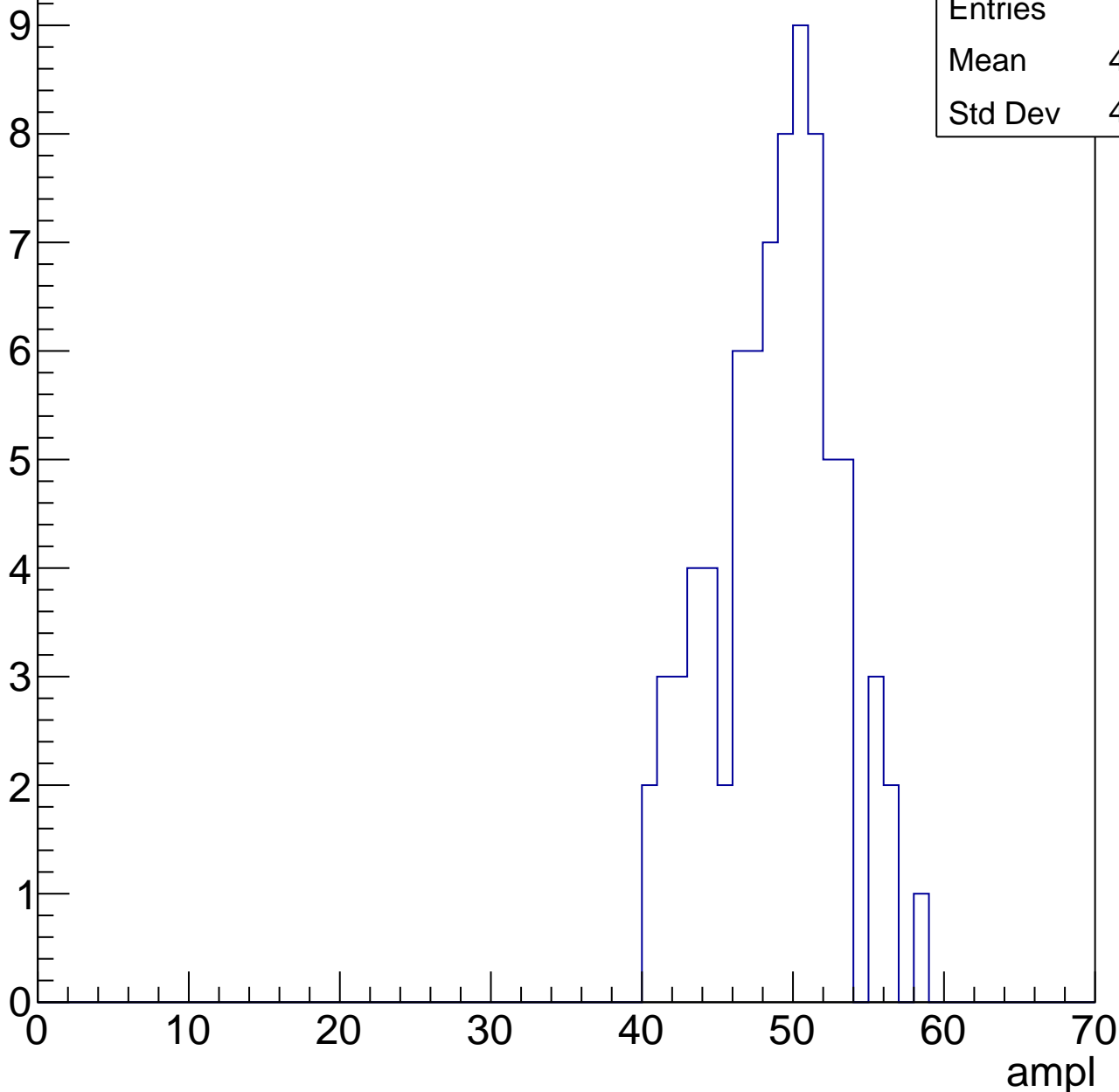


# B1L103S, U9-ch72, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	78
Mean	48.35
Std Dev	4.054

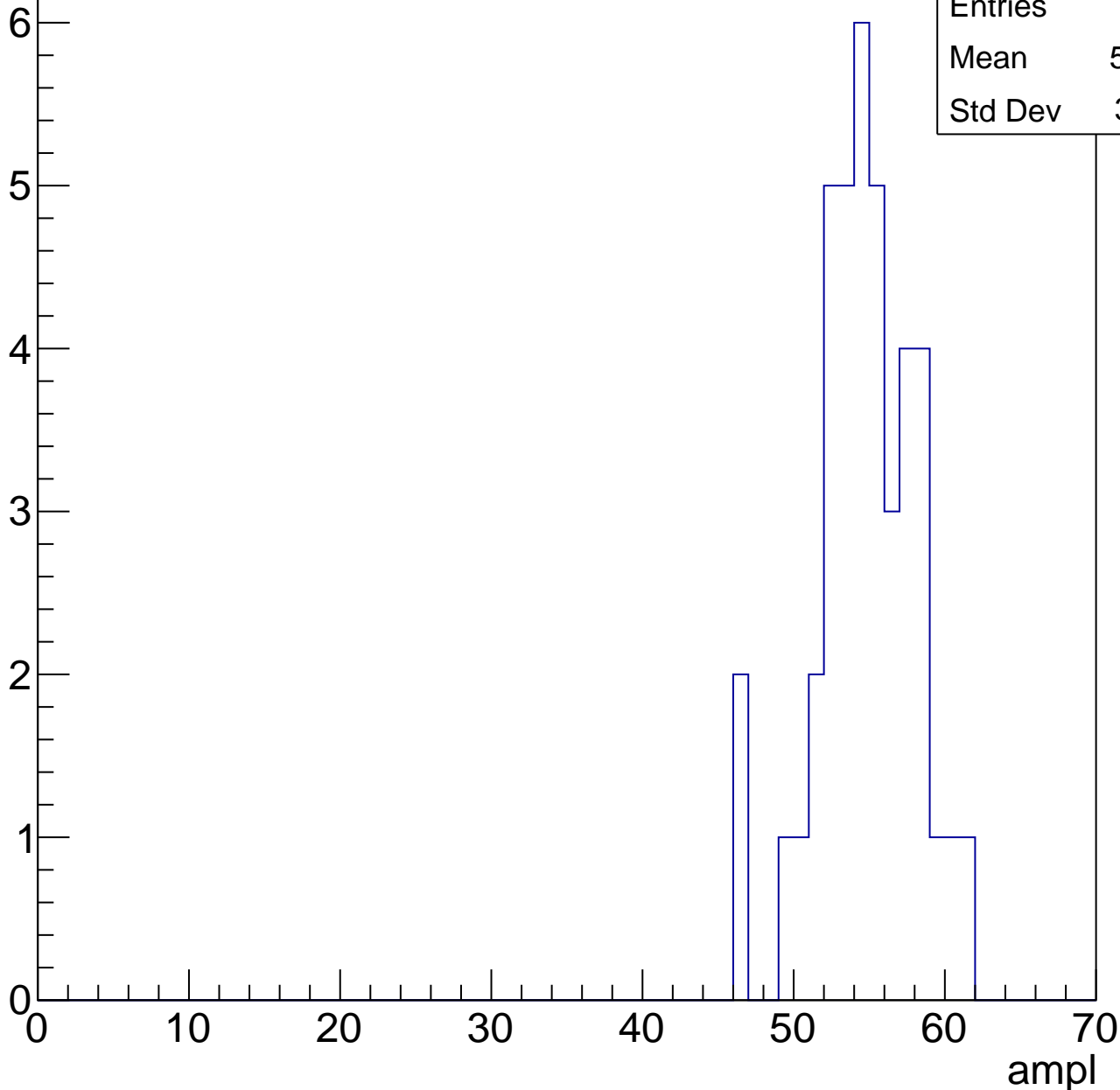


# B1L103S, U9-ch72, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

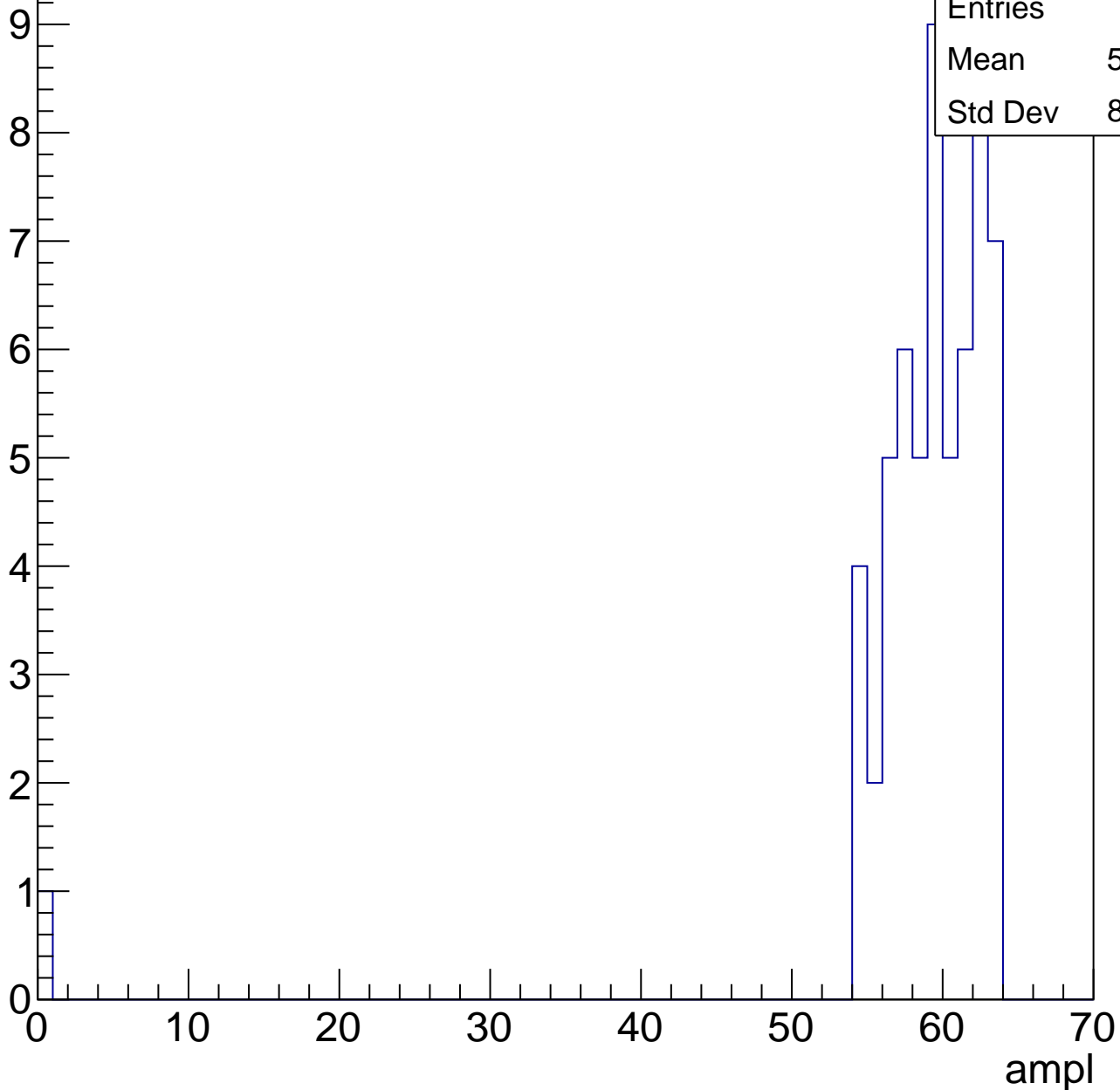
Entries	41
Mean	54.27
Std Dev	3.261



# B1L103S, U9-ch72, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U9-ch72, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

3  
2.5  
2  
1.5  
1  
0.5  
0

Entries	11
Mean	61.45
Std Dev	1.157

ampl

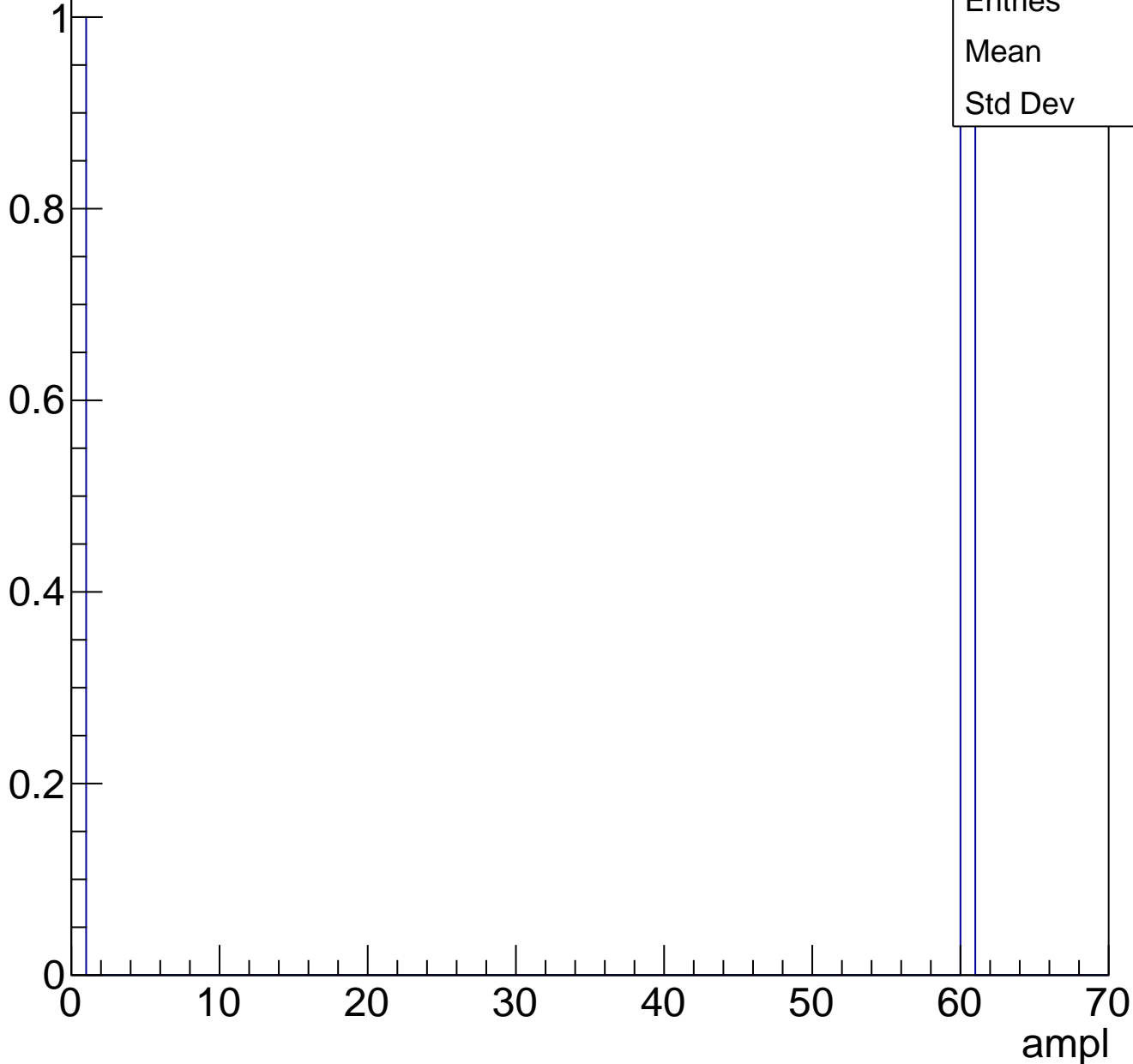
0 10 20 30 40 50 60 70



# B1L103S, U9-ch72, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U9-ch73, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	80
Mean	30.39
Std Dev	3.614

**Gaus mean : 30.4645**

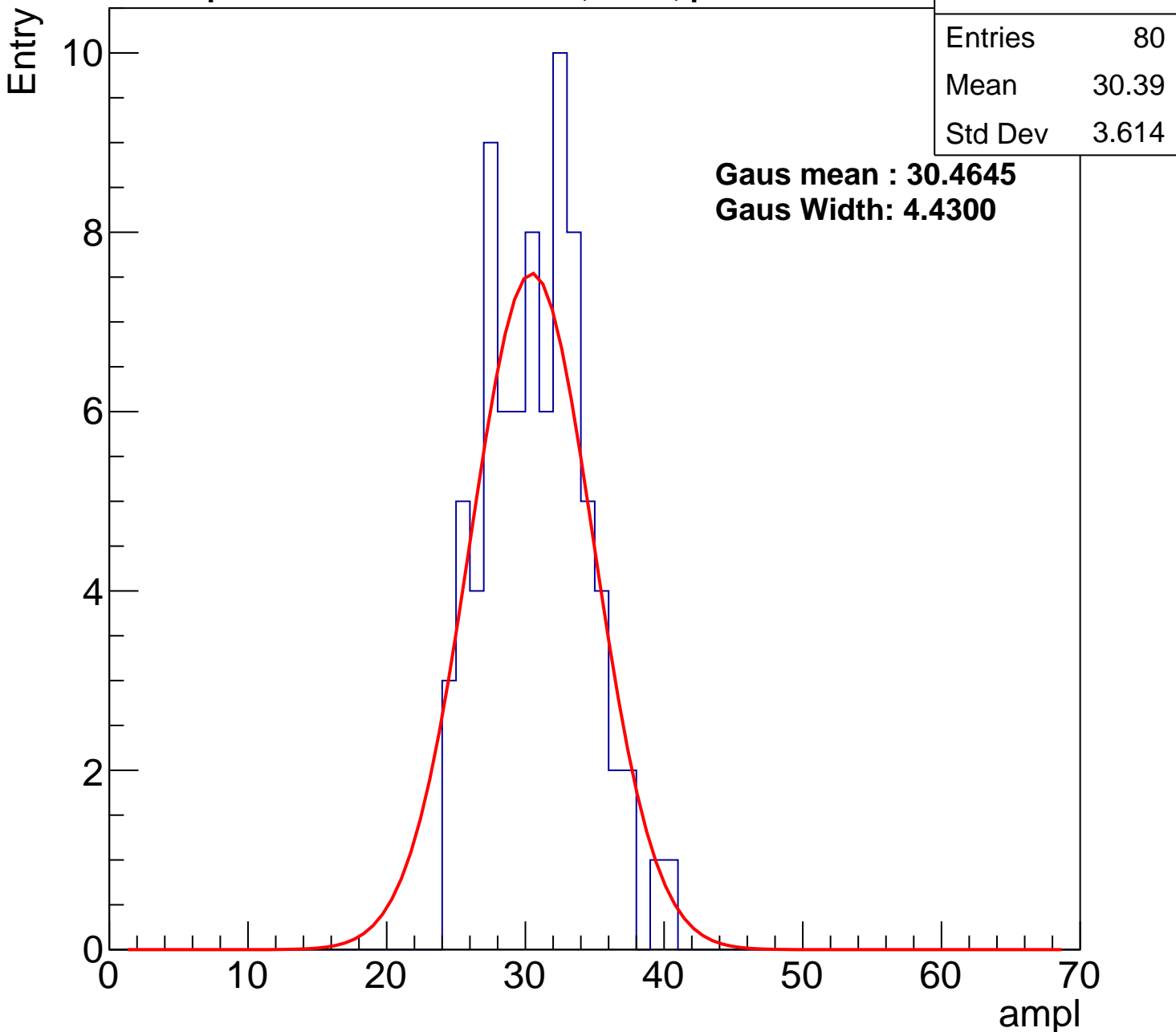
**Gaus Width: 4.4300**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U9-ch73, adc1

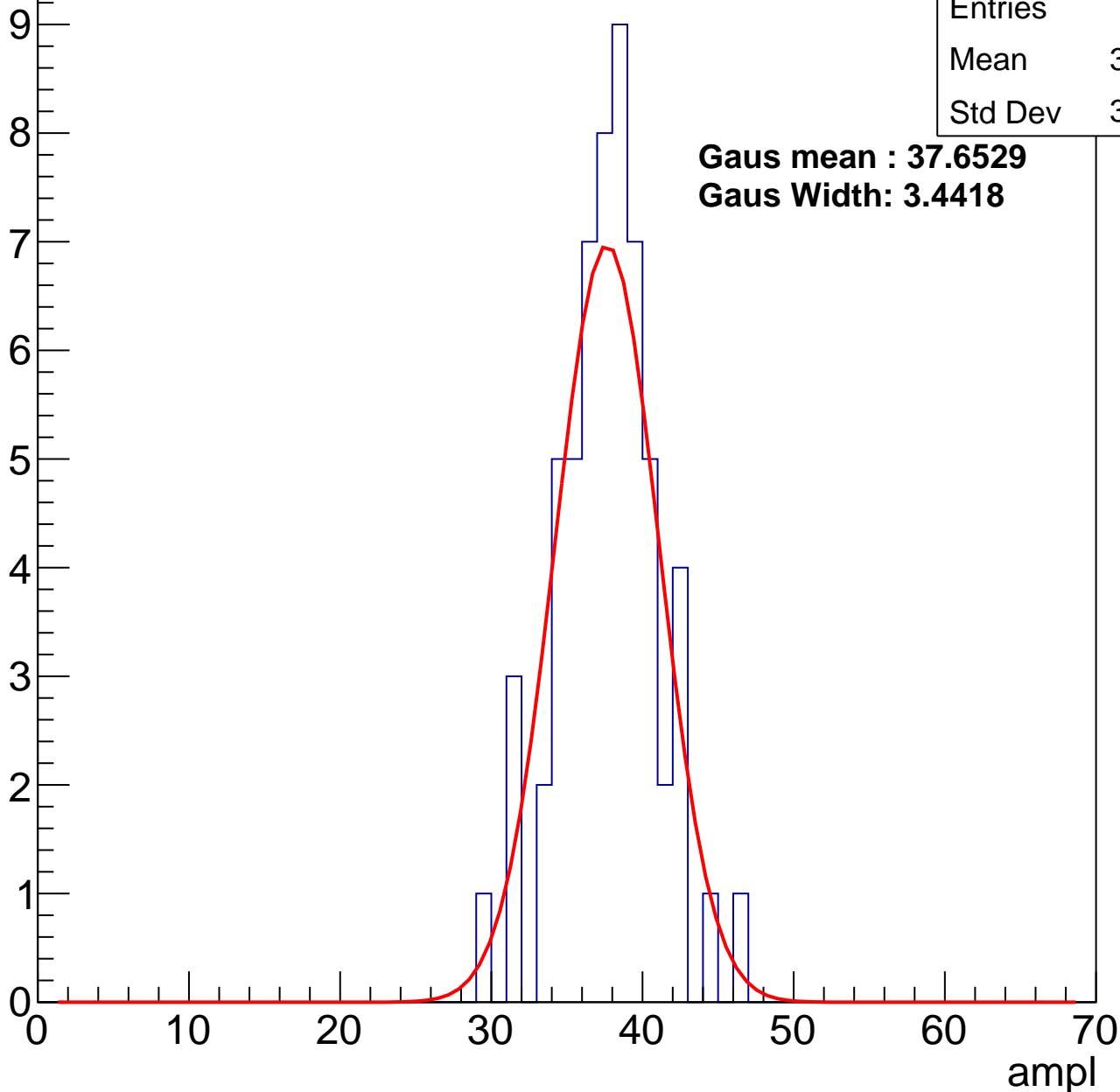
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	60
Mean	37.27
Std Dev	3.203

**Gaus mean : 37.6529**

**Gaus Width: 3.4418**



# B1L103S, U9-ch73, adc2

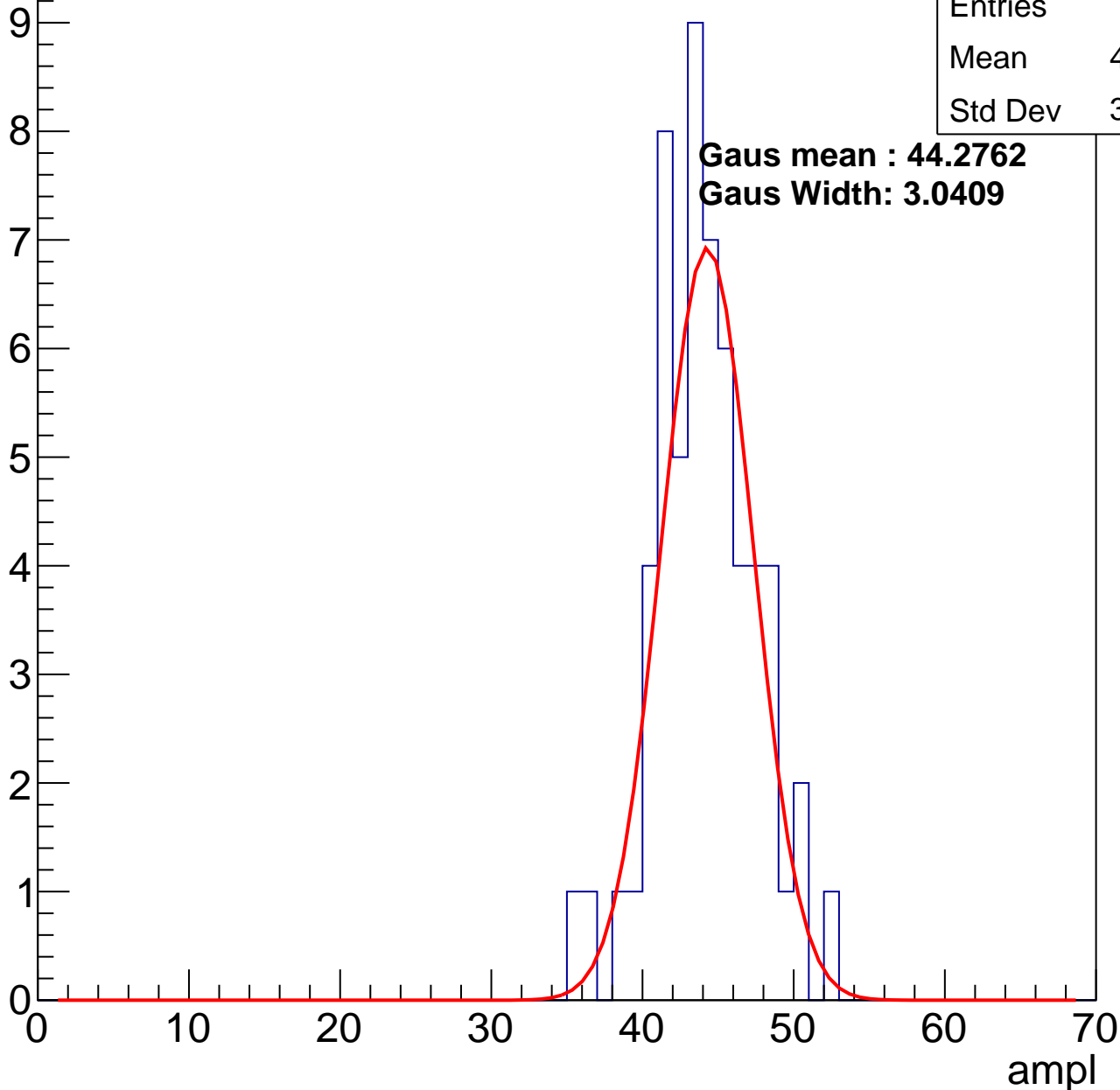
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	59
Mean	43.66
Std Dev	3.312

**Gaus mean : 44.2762**

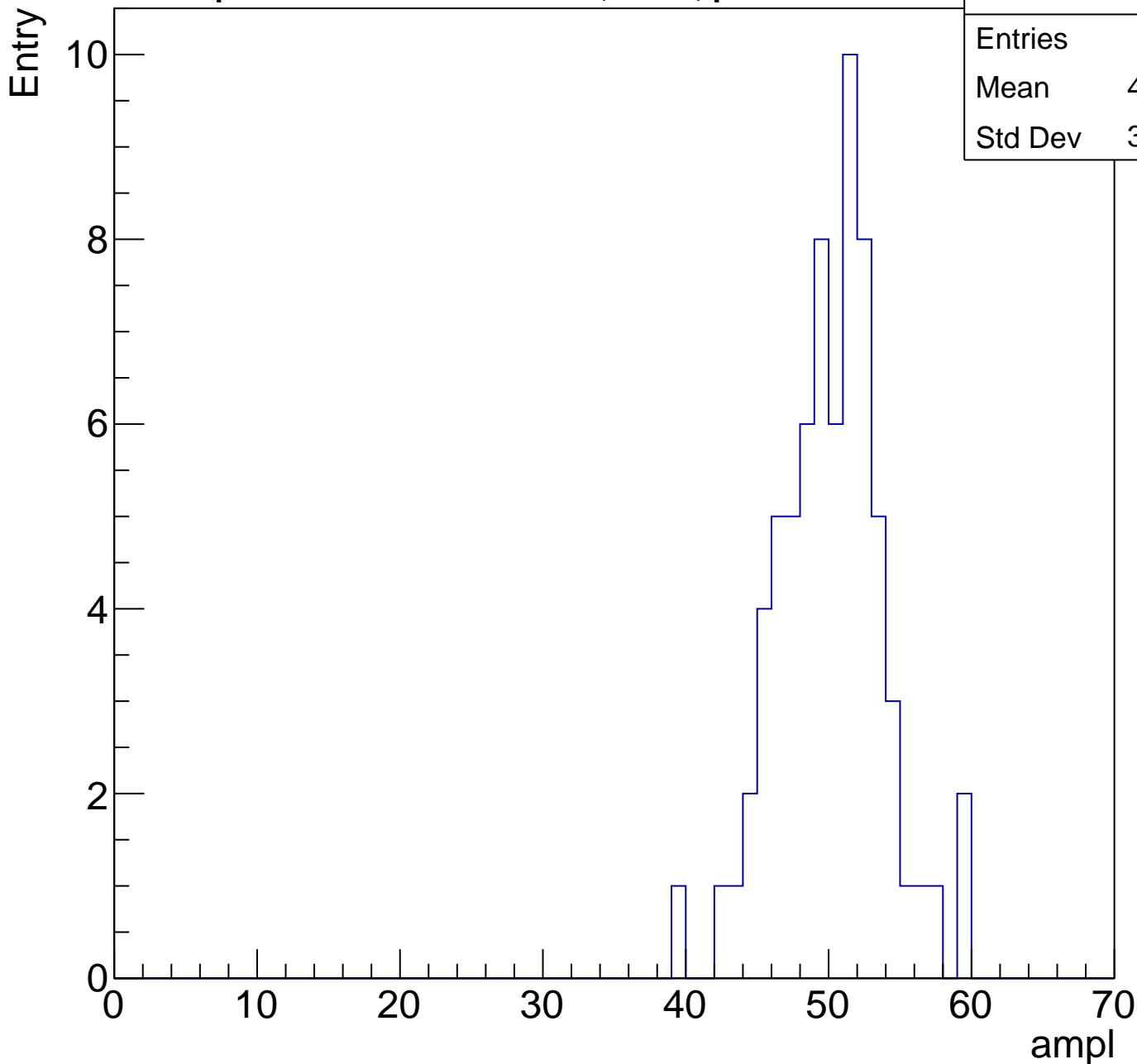
**Gaus Width: 3.0409**



# B1L103S, U9-ch73, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	70
Mean	49.66
Std Dev	3.707

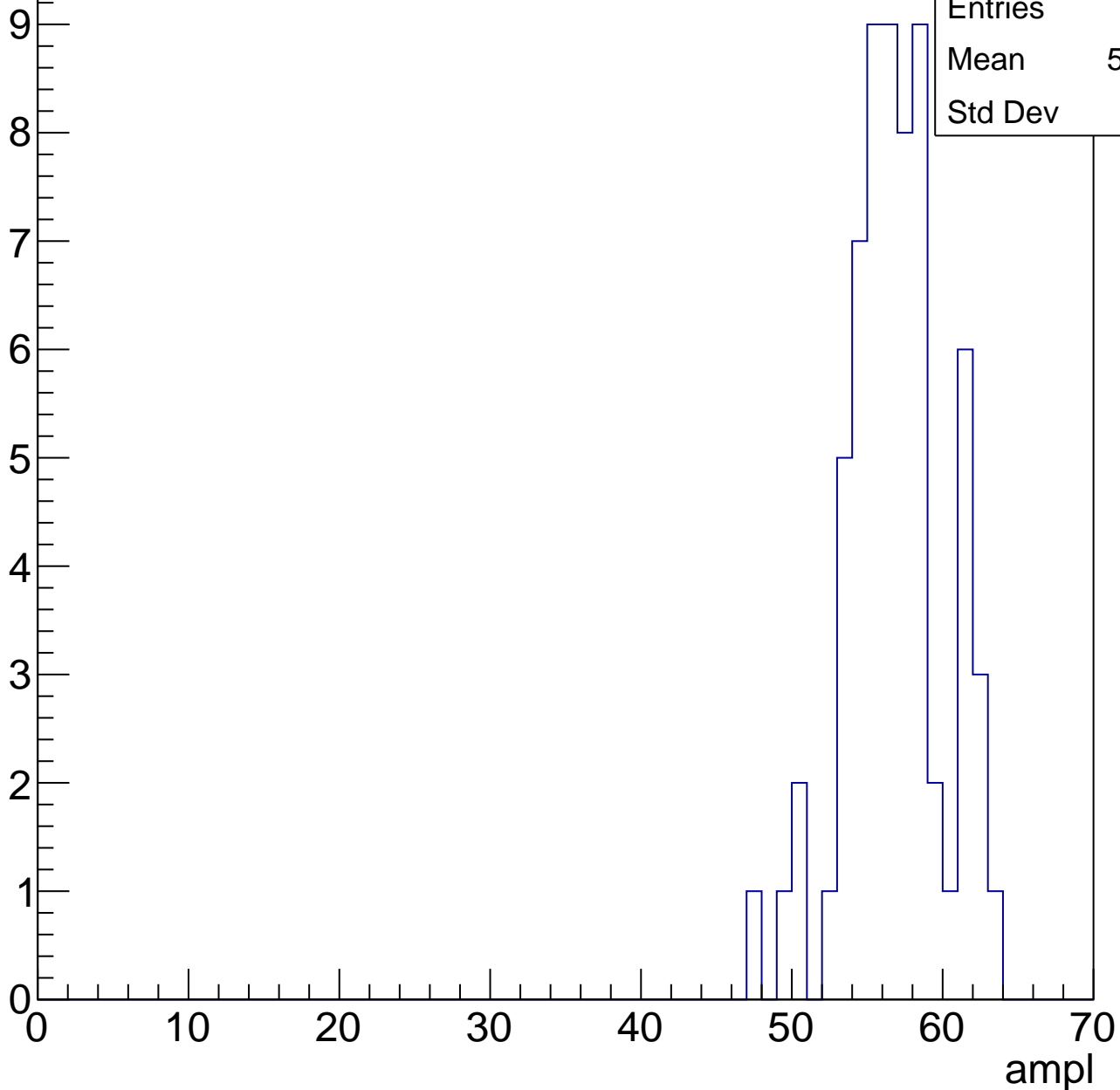


# B1L103S, U9-ch73, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

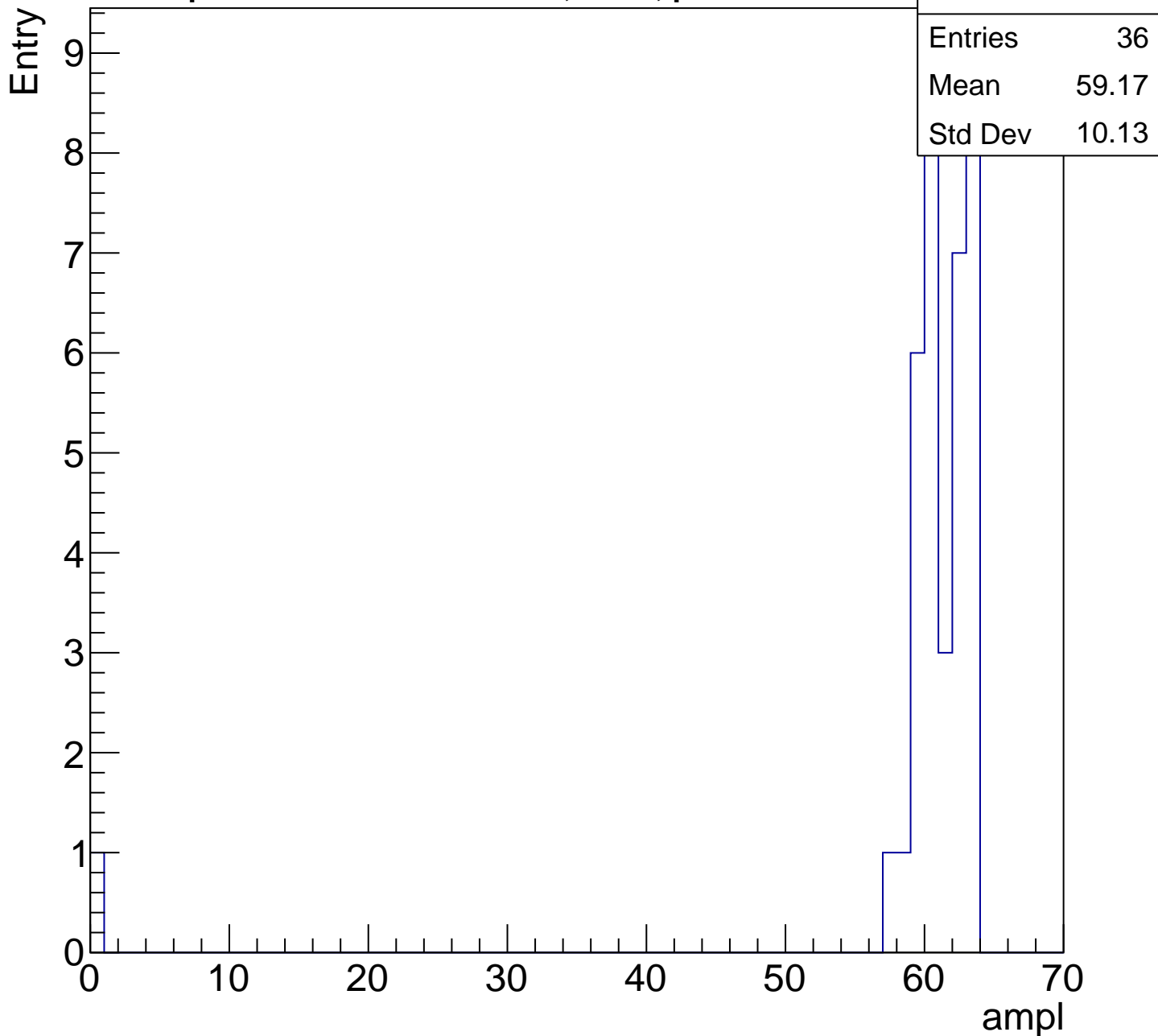
Entry

Entries	65
Mean	56.32
Std Dev	3.23



# B1L103S, U9-ch73, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U9-ch73, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U9-ch73, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	2
Mean	11.5
Std Dev	11.5

# B1L103S, U9-ch74, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	66
Mean	27.41
Std Dev	3.494

**Gaus mean : 28.0008**

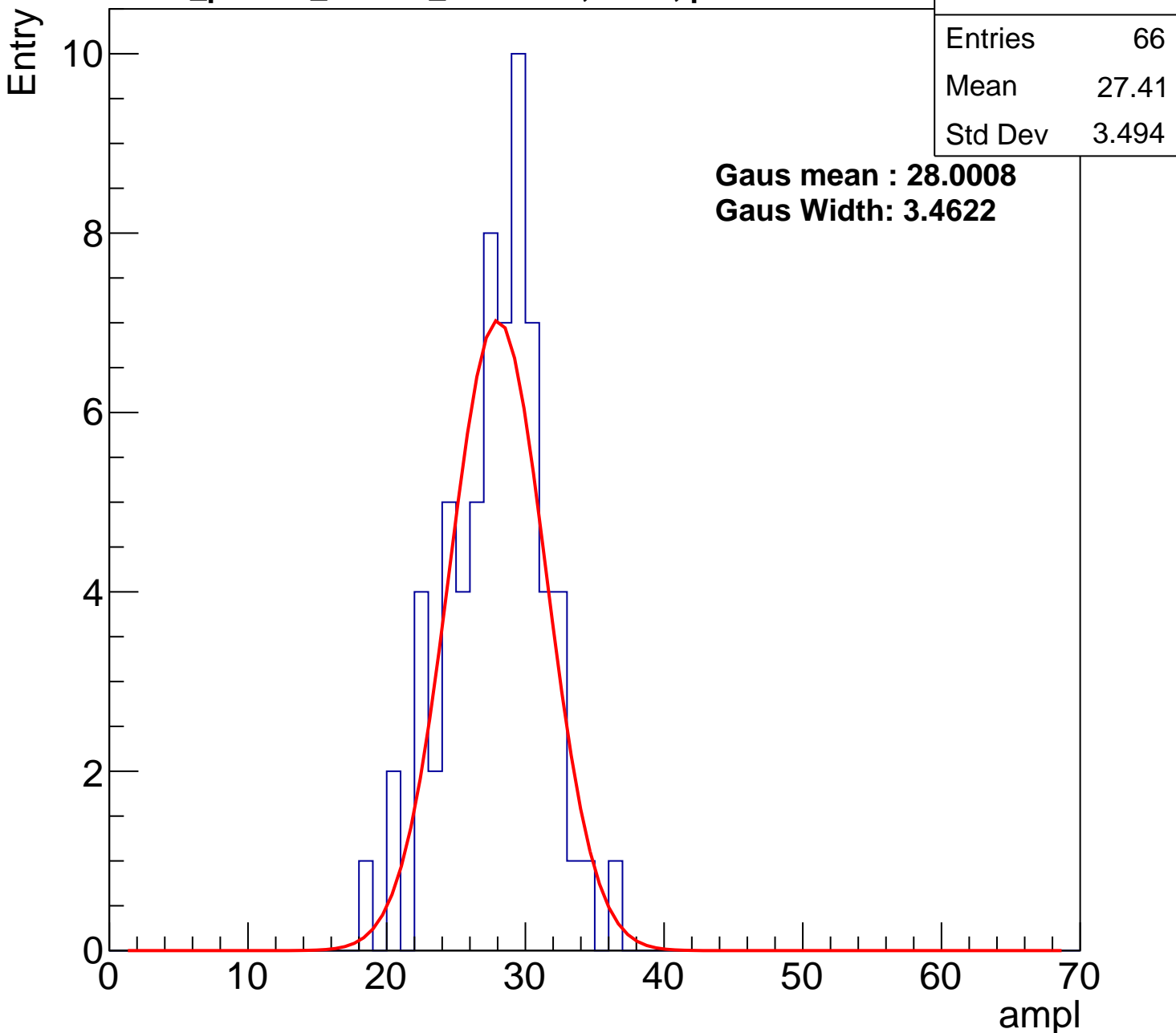
**Gaus Width: 3.4622**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U9-ch74, adc1

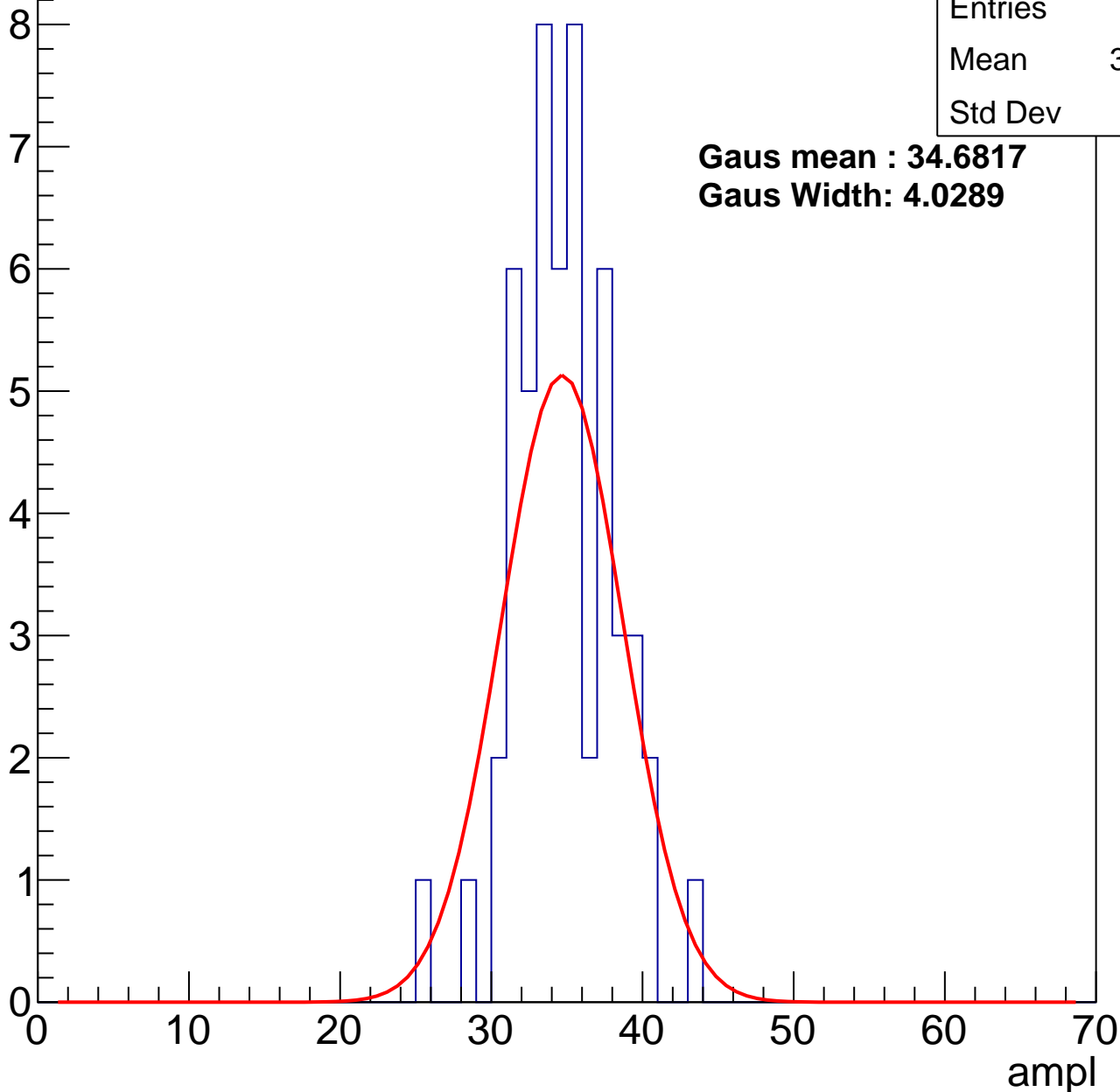
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	54
Mean	34.35
Std Dev	3.25

**Gaus mean : 34.6817**

**Gaus Width: 4.0289**



# B1L103S, U9-ch74, adc2

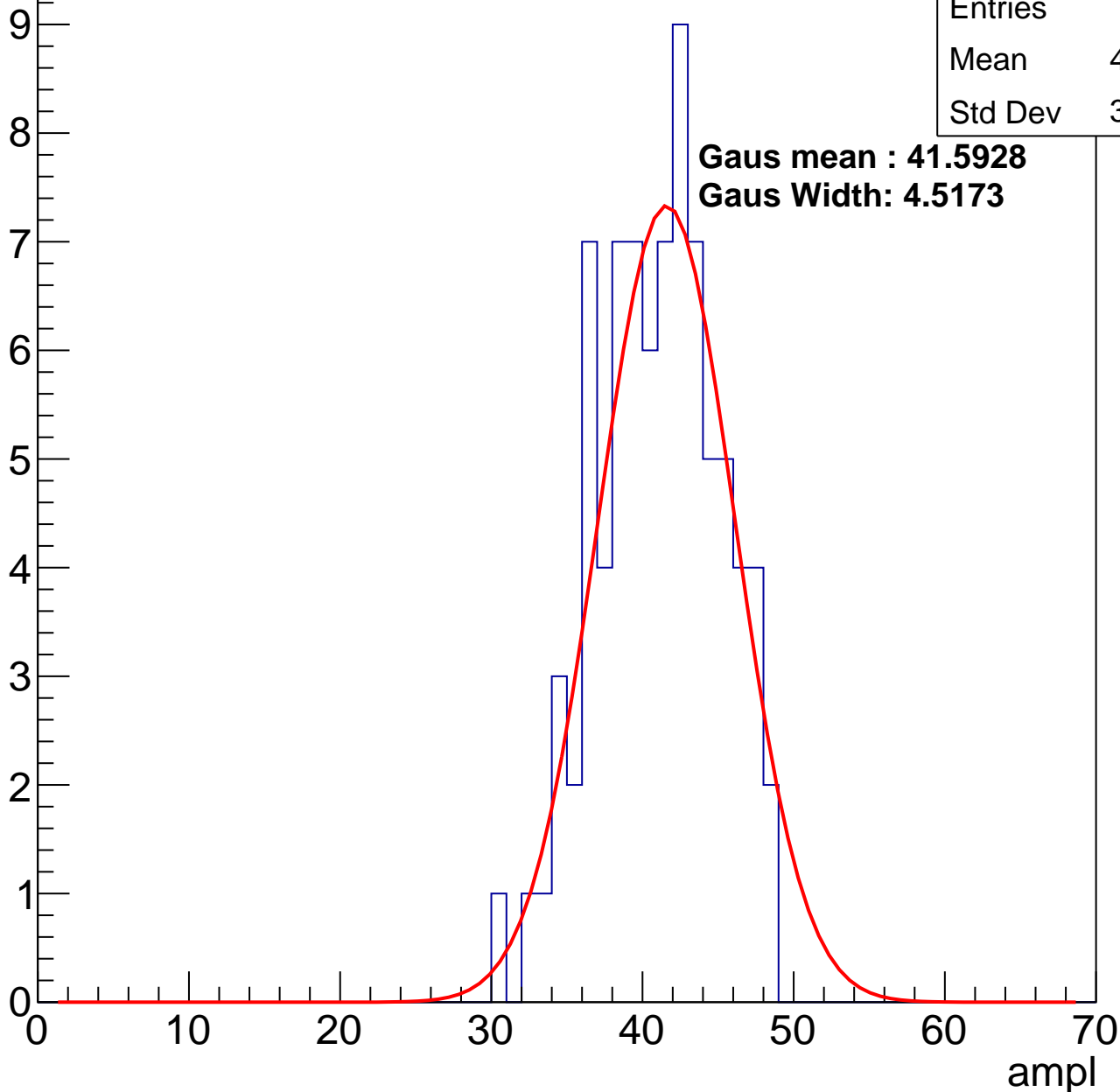
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	82
Mean	40.55
Std Dev	3.994

**Gaus mean : 41.5928**

**Gaus Width: 4.5173**

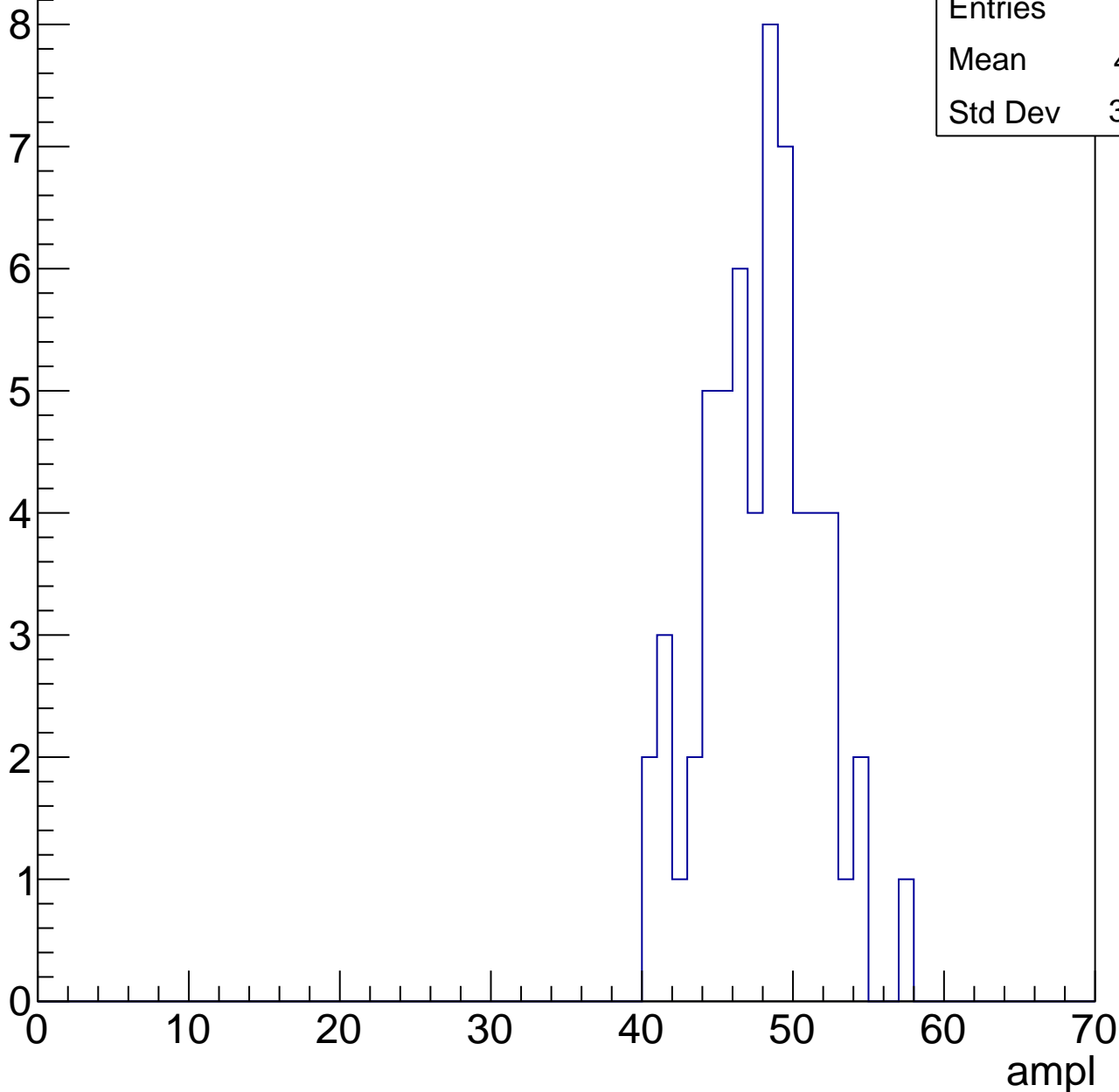


# B1L103S, U9-ch74, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	59
Mean	47.41
Std Dev	3.669

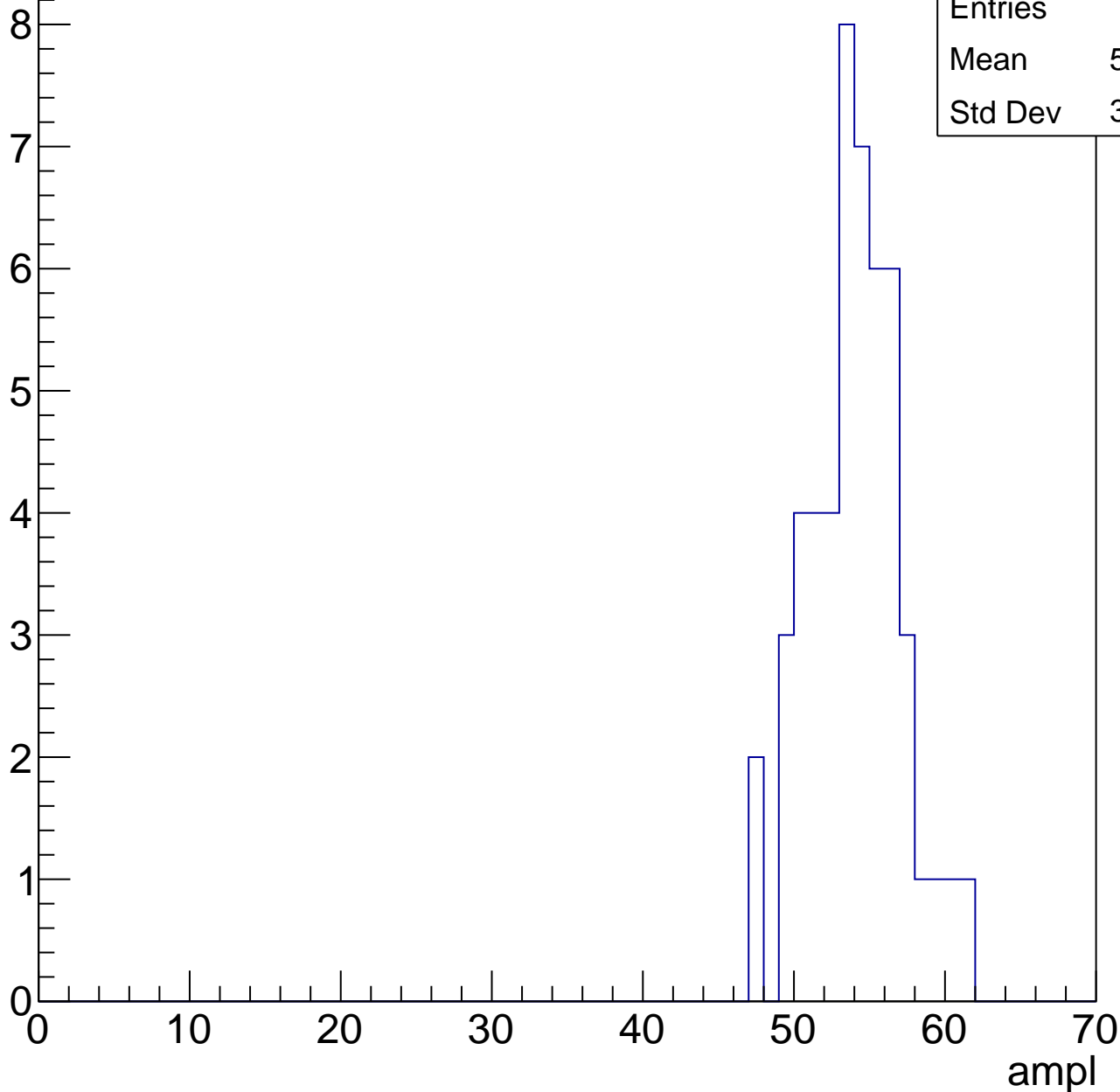


# B1L103S, U9-ch74, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	51
Mean	53.53
Std Dev	3.032

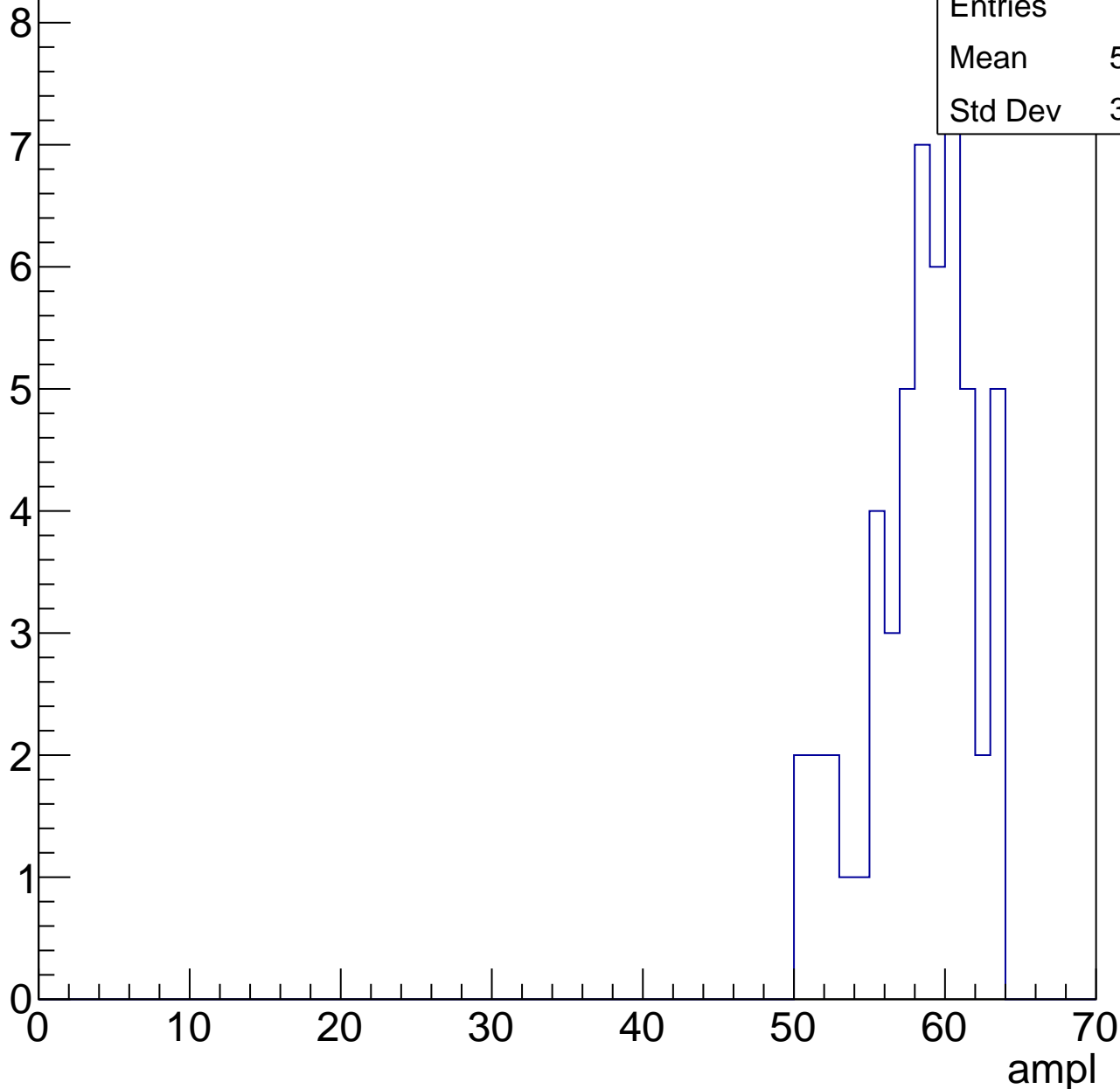


# B1L103S, U9-ch74, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	53
Mean	57.92
Std Dev	3.452

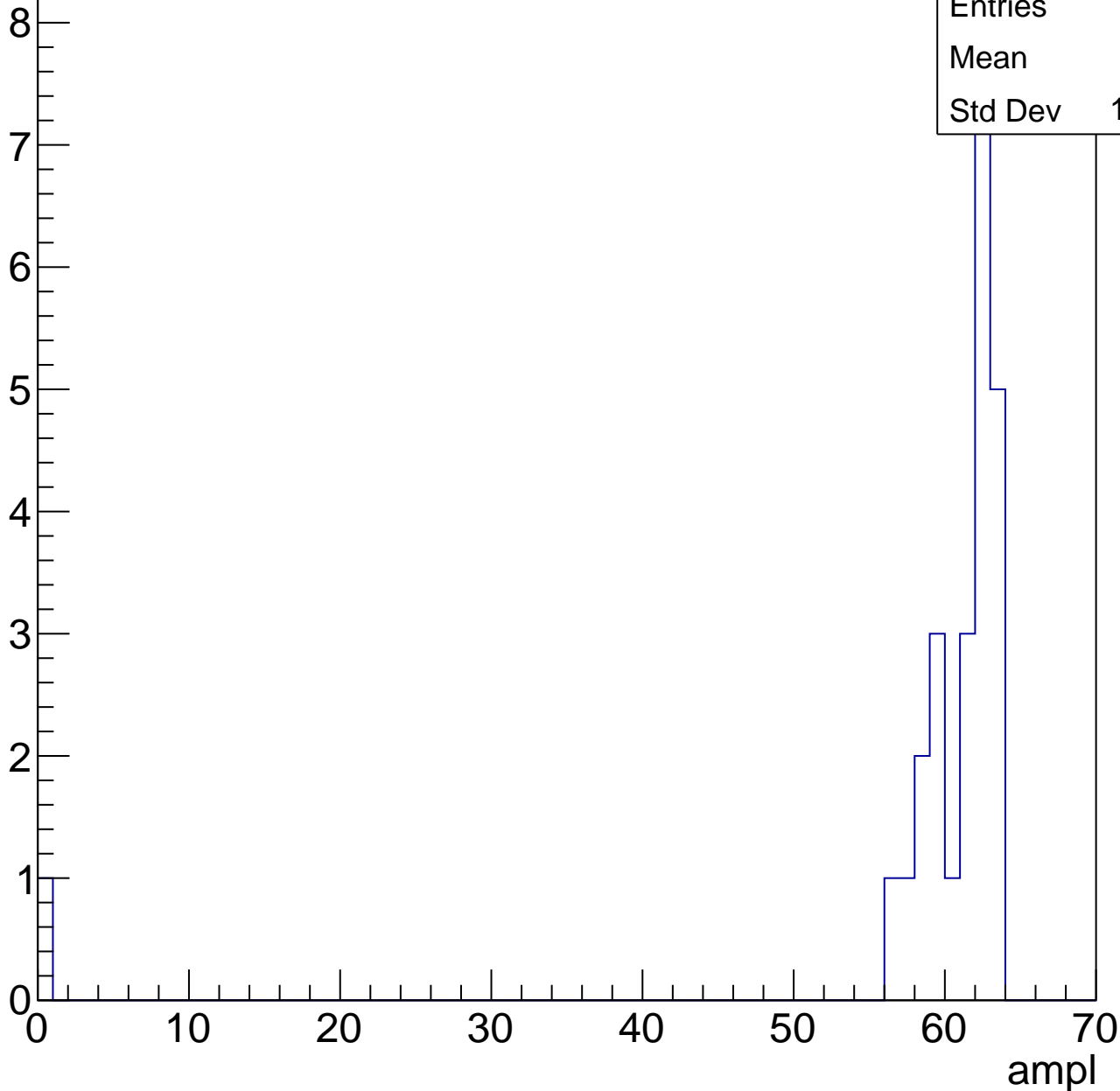


# B1L103S, U9-ch74, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	25
Mean	58.4
Std Dev	12.09

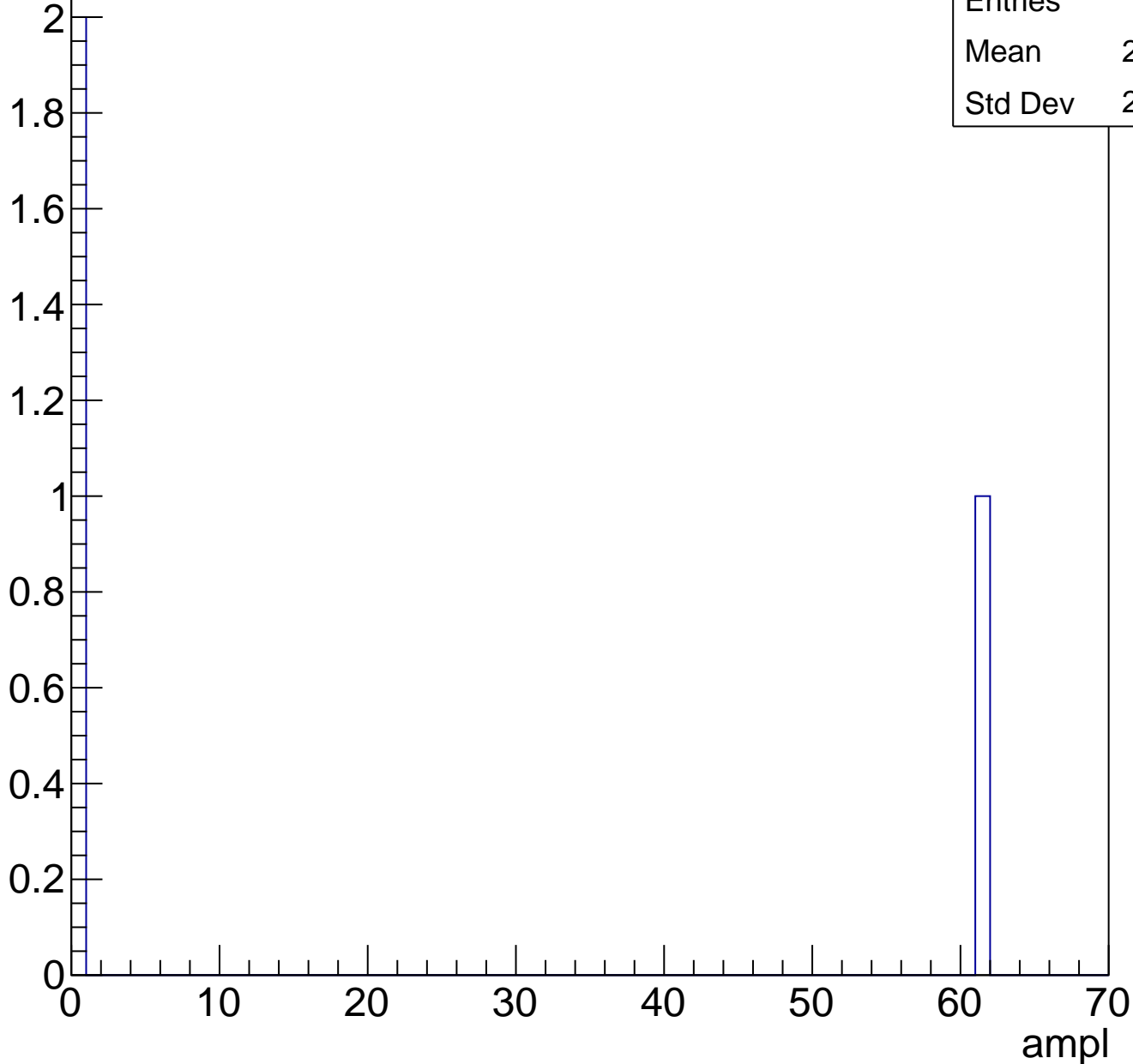




# B1L103S, U9-ch74, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



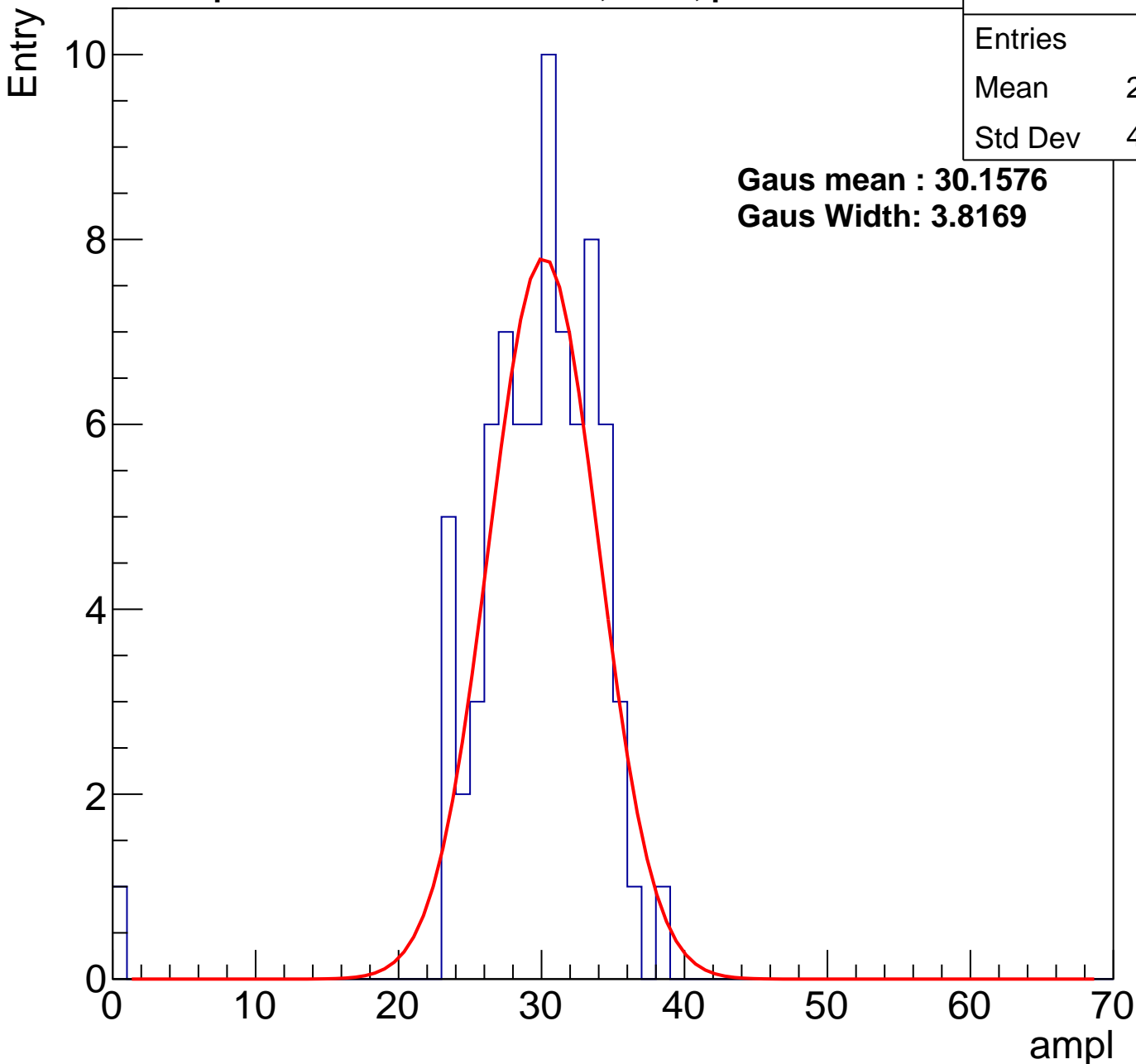
# B1L103S, U9-ch75, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	78
Mean	29.24
Std Dev	4.818

**Gaus mean : 30.1576**

**Gaus Width: 3.8169**



# B1L103S, U9-ch75, adc1

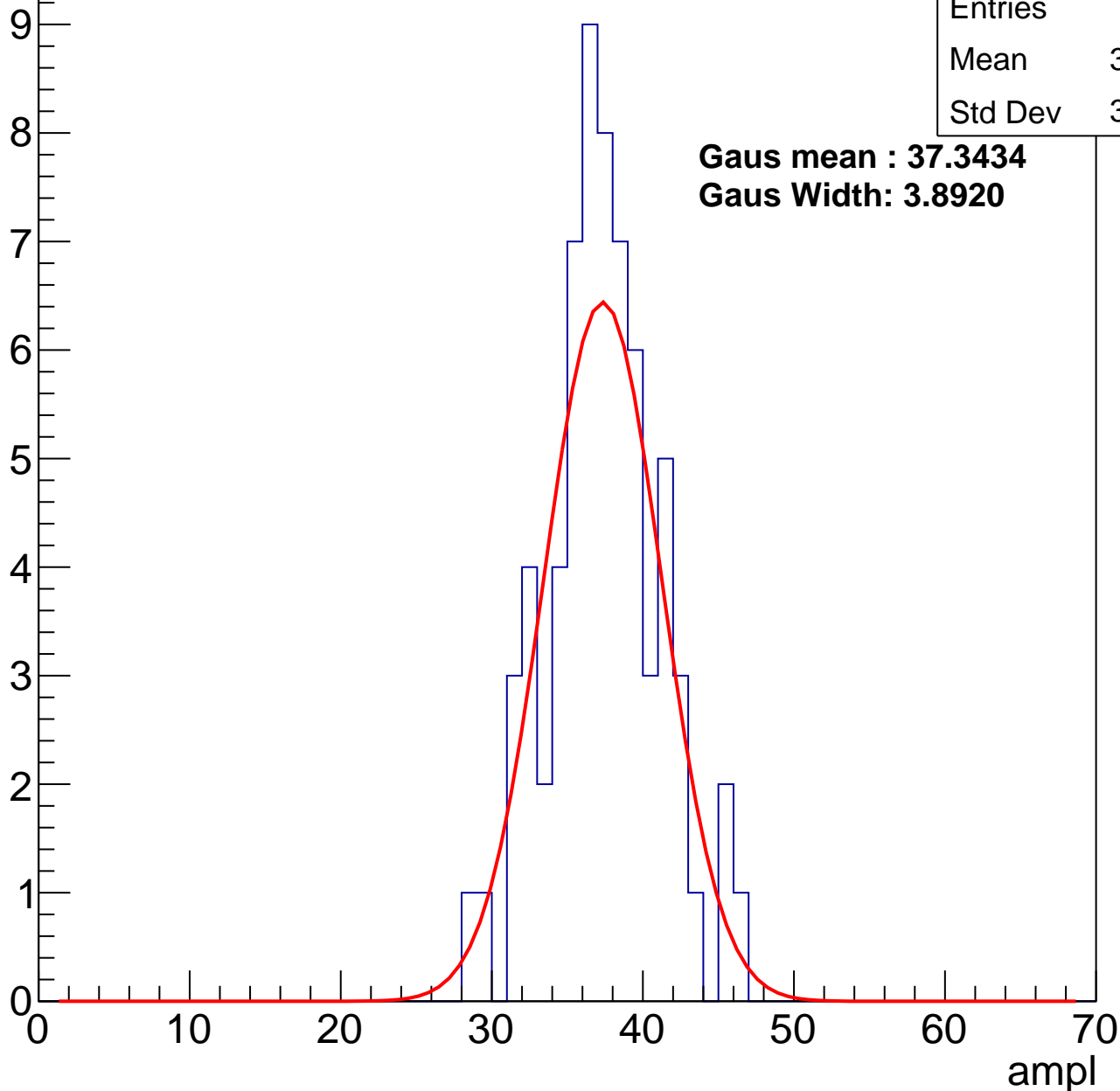
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	36.94
Std Dev	3.697

**Gaus mean : 37.3434**

**Gaus Width: 3.8920**



# B1L103S, U9-ch75, adc2

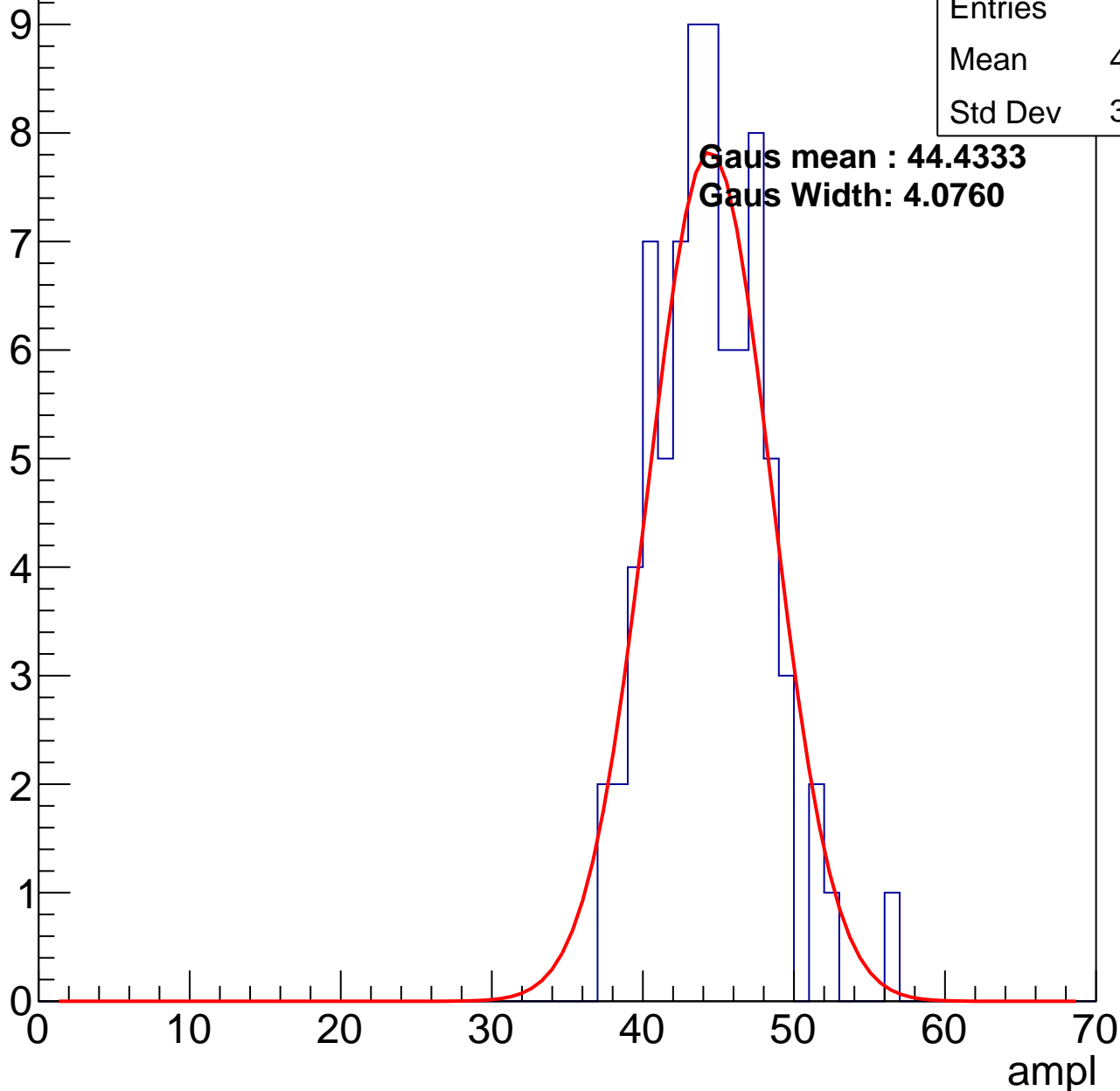
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	77
Mean	43.99
Std Dev	3.652

**Gaus mean : 44.4333**

**Gaus Width: 4.0760**

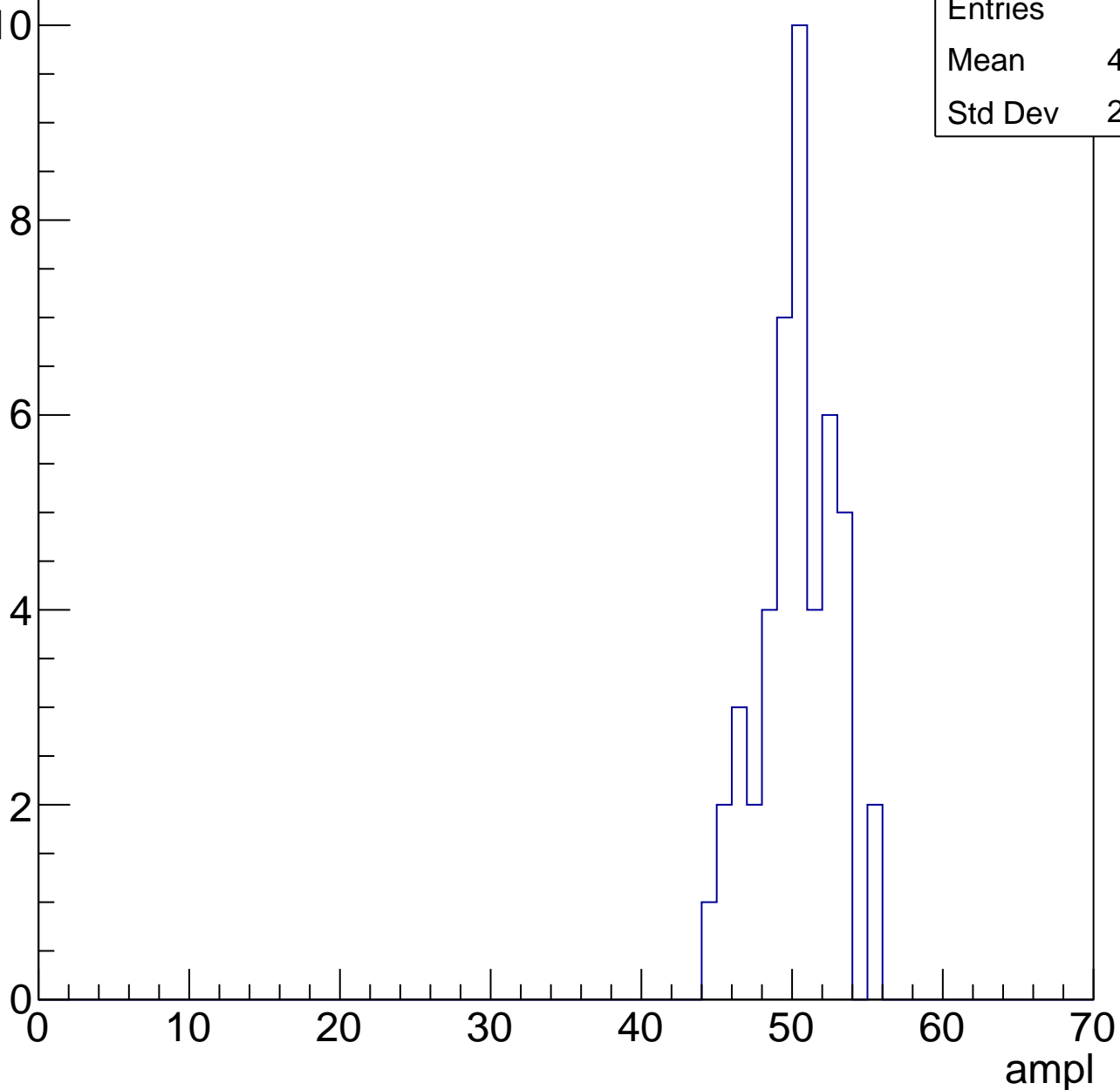


# B1L103S, U9-ch75, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	46
Mean	49.83
Std Dev	2.539

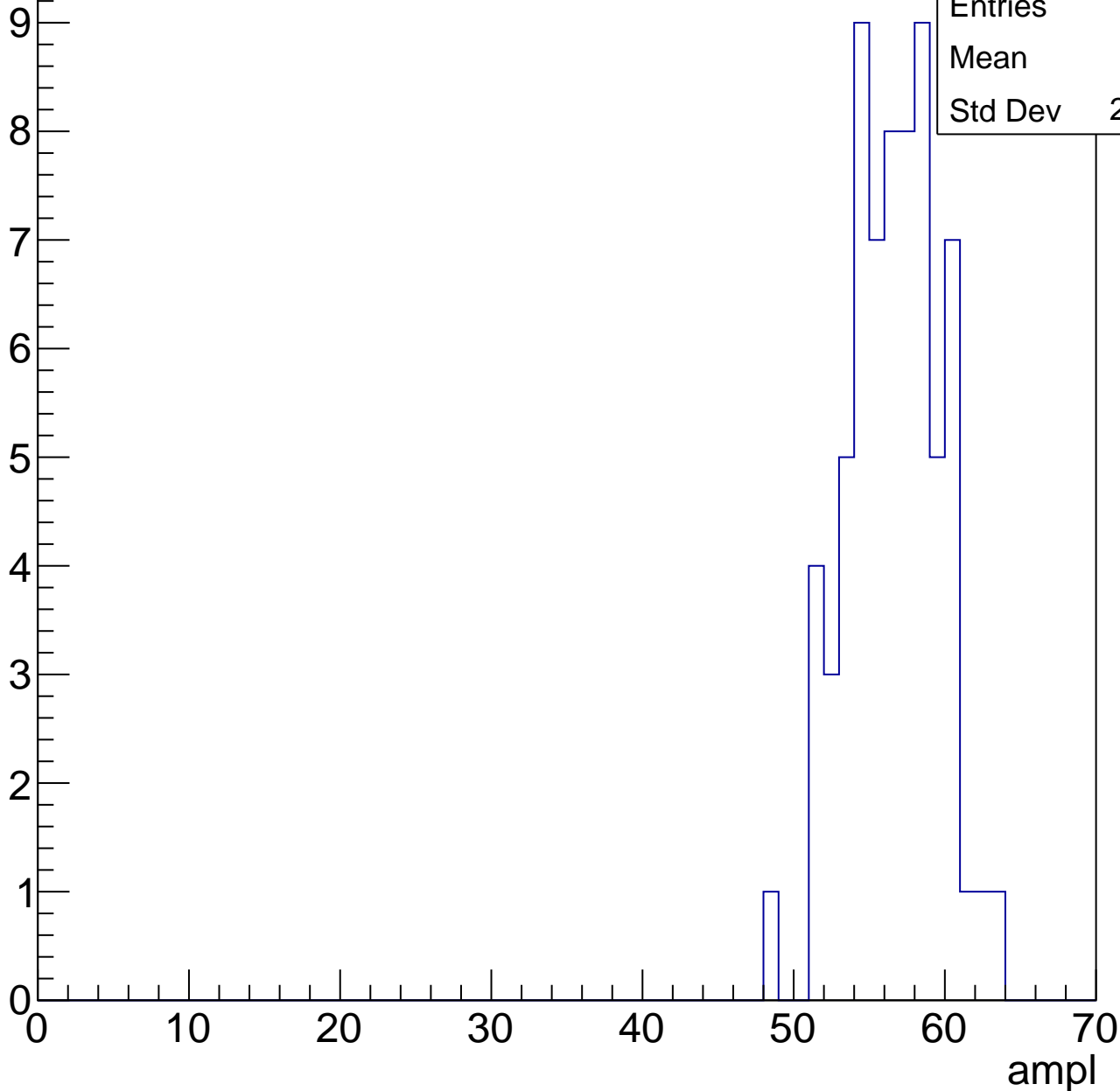


# B1L103S, U9-ch75, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	69
Mean	56.1
Std Dev	2.974

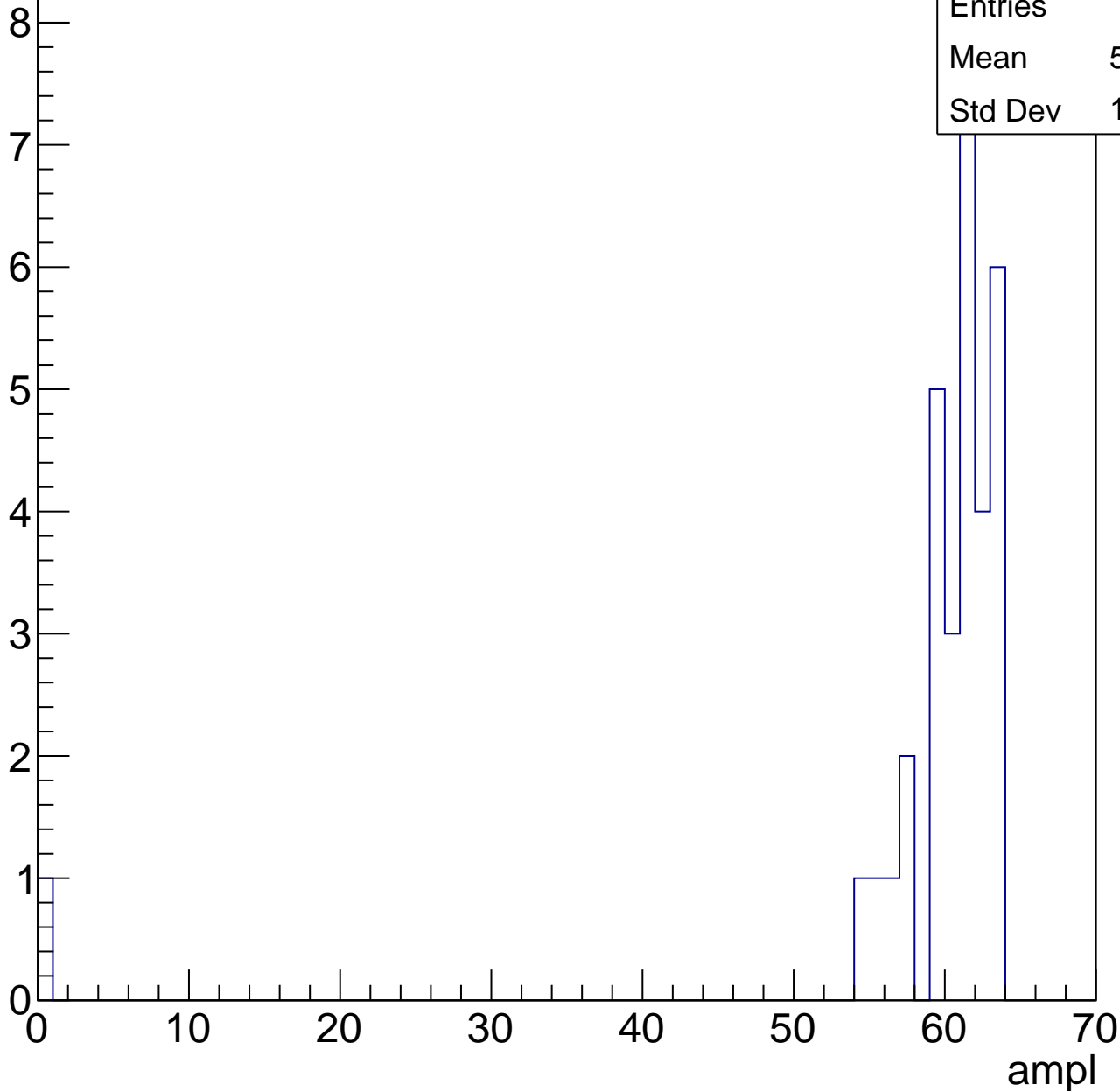


# B1L103S, U9-ch75, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	32
Mean	58.38
Std Dev	10.74

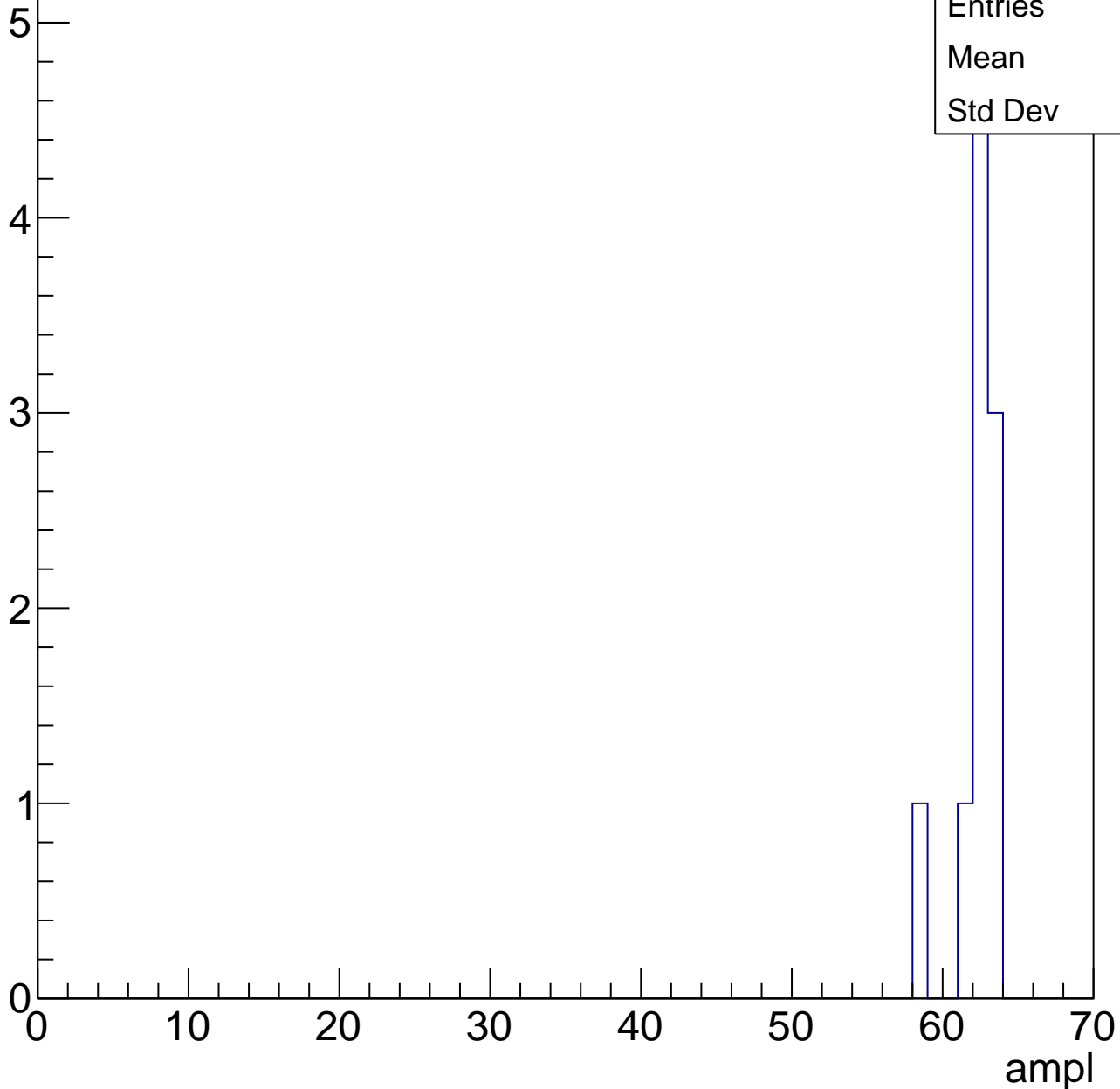


# B1L103S, U9-ch75, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	10
Mean	61.8
Std Dev	1.4





# B1L103S, U9-ch75, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U9-ch76, adc0

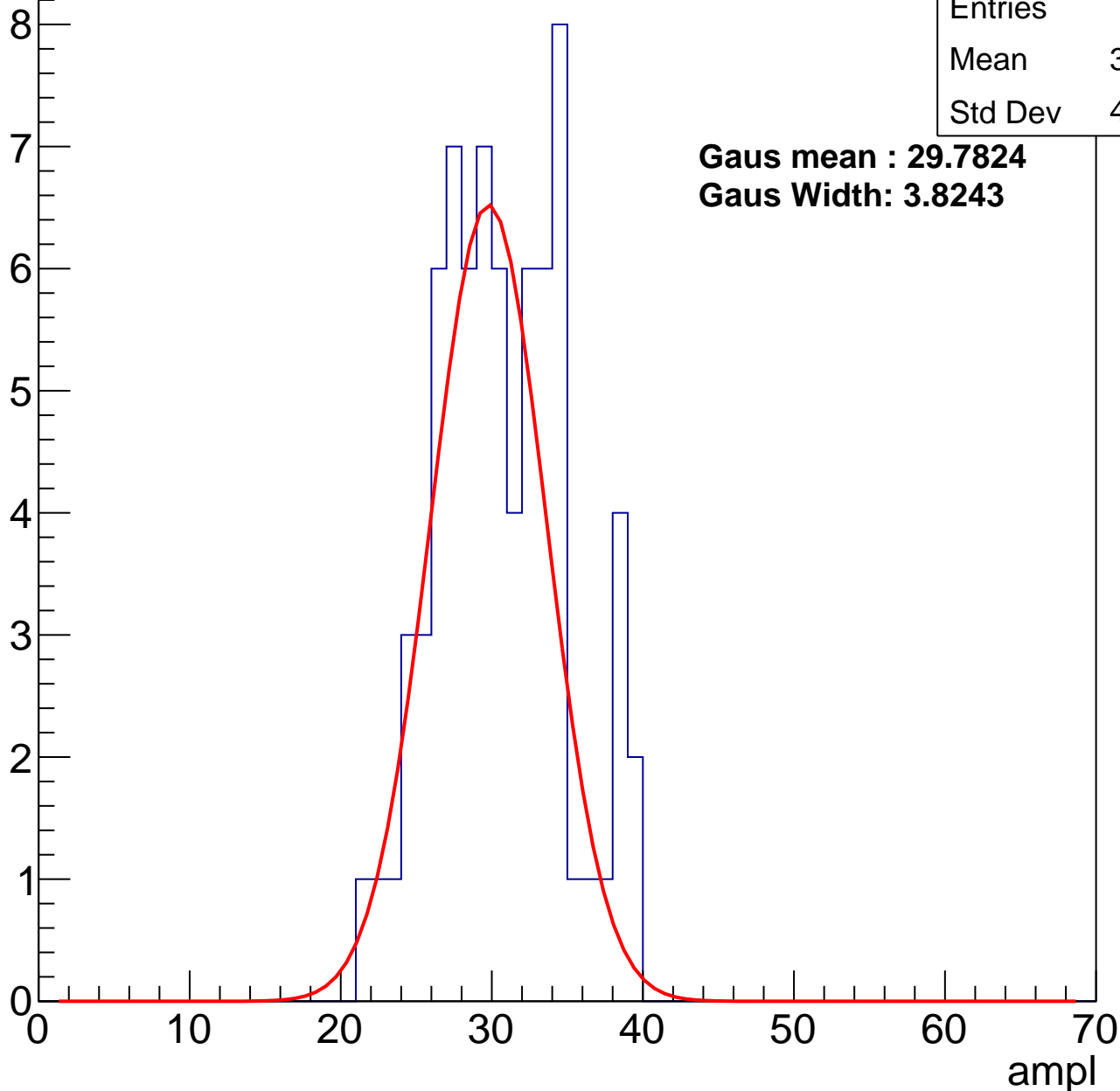
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	74
Mean	30.18
Std Dev	4.196

**Gaus mean : 29.7824**

**Gaus Width: 3.8243**



# B1L103S, U9-ch76, adc1

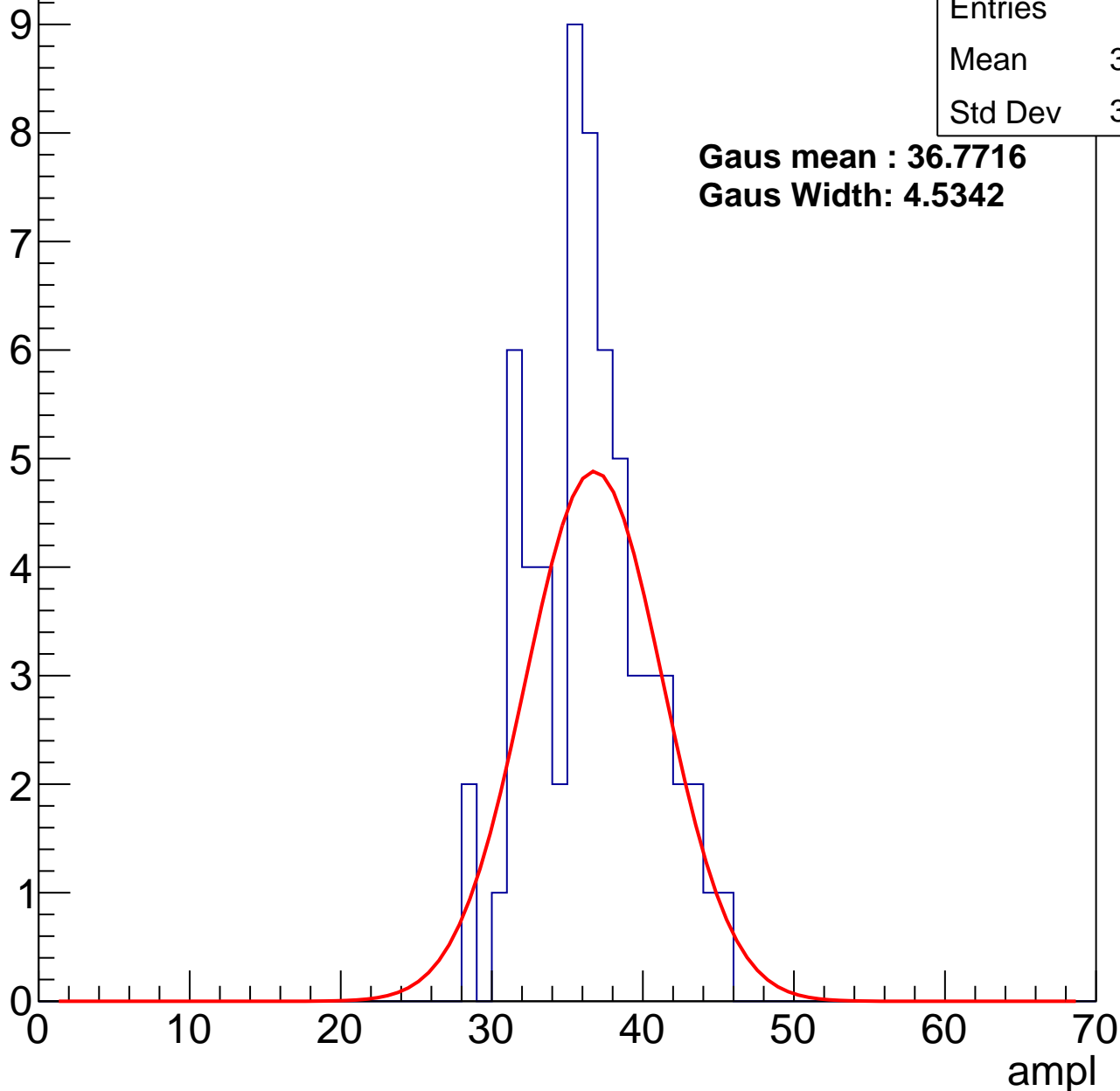
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	36.03
Std Dev	3.856

**Gaus mean : 36.7716**

**Gaus Width: 4.5342**



# B1L103S, U9-ch76, adc2

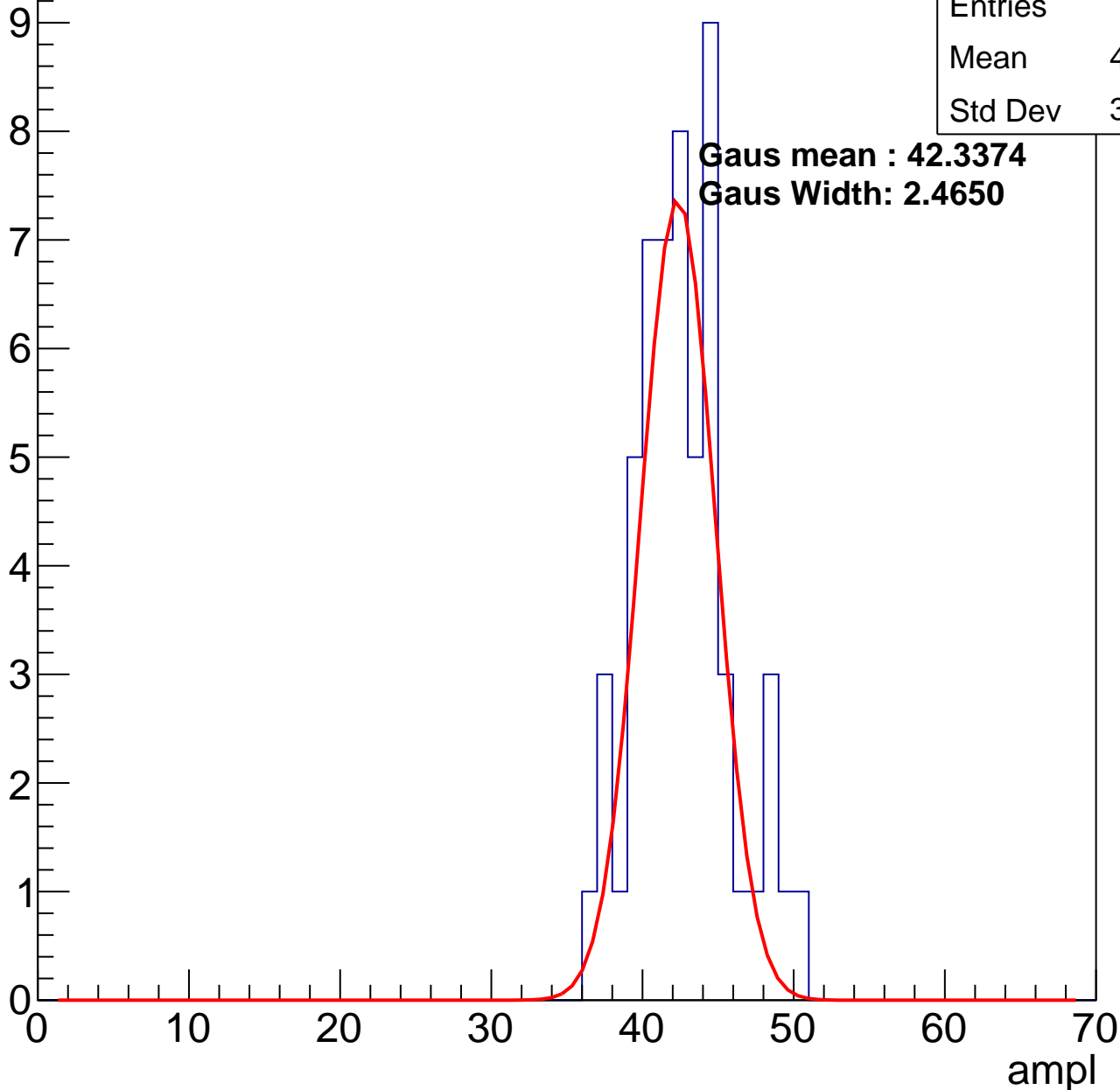
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	56
Mean	42.23
Std Dev	3.088

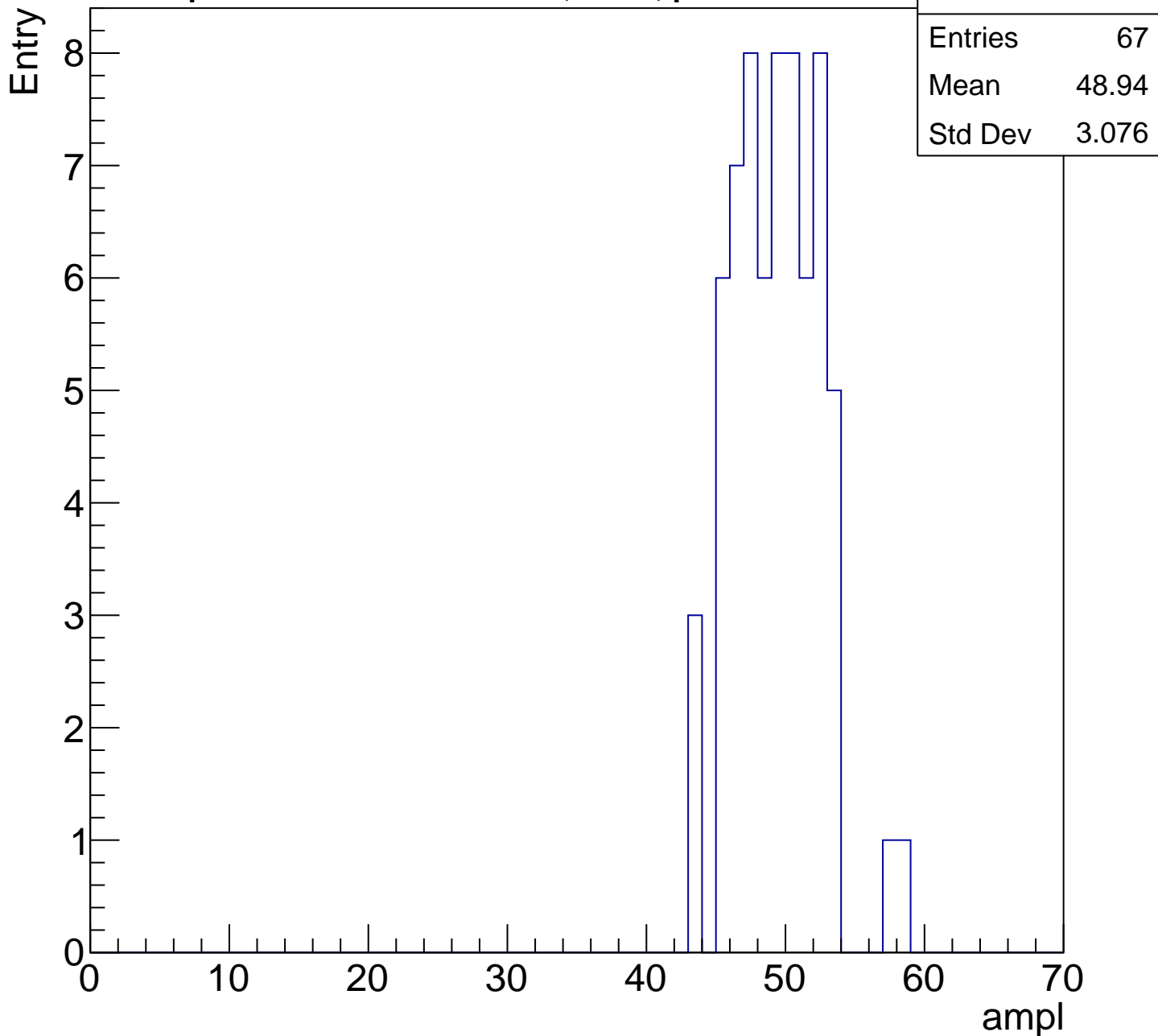
**Gaus mean : 42.3374**

**Gaus Width: 2.4650**



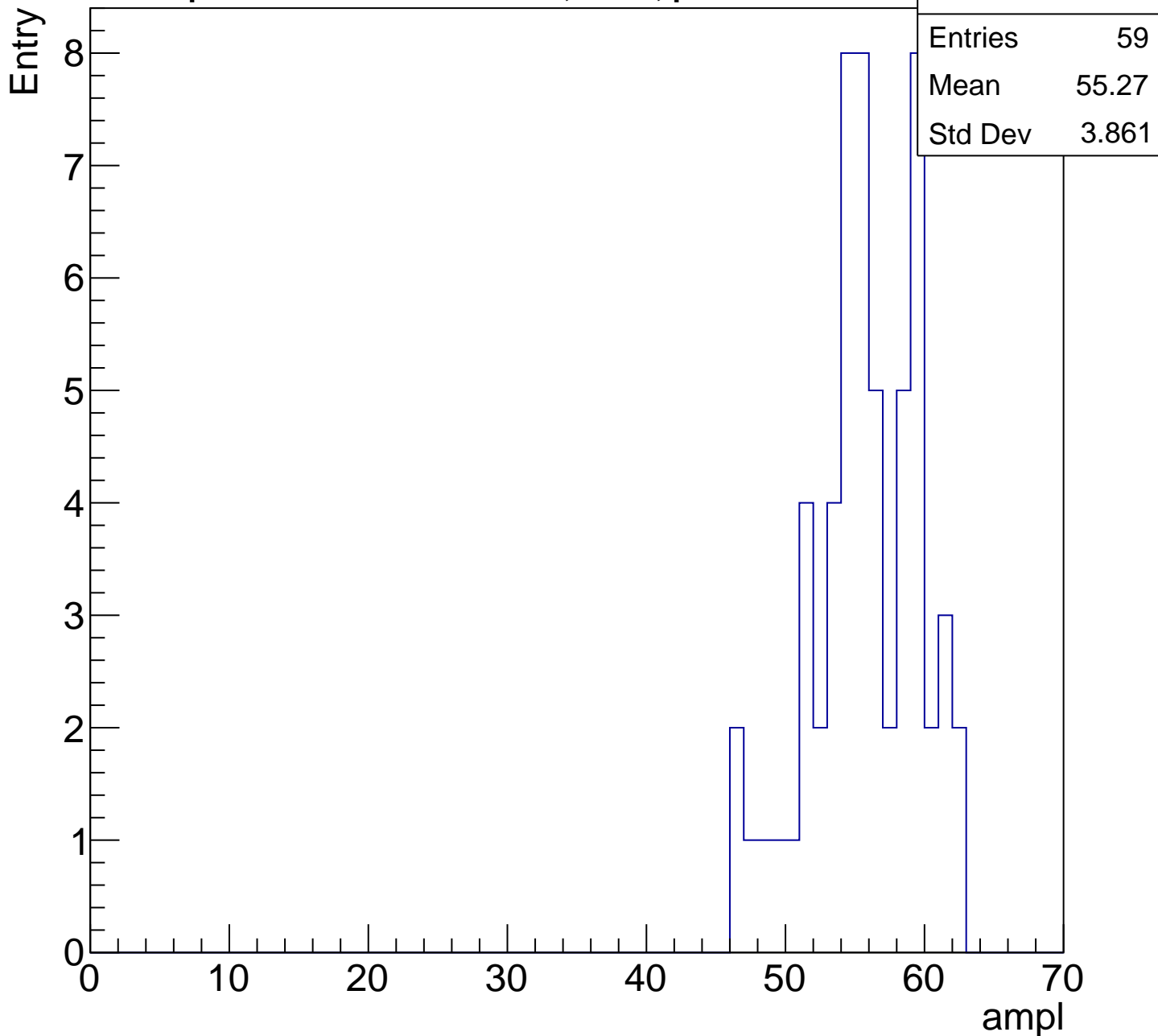
# B1L103S, U9-ch76, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U9-ch76, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

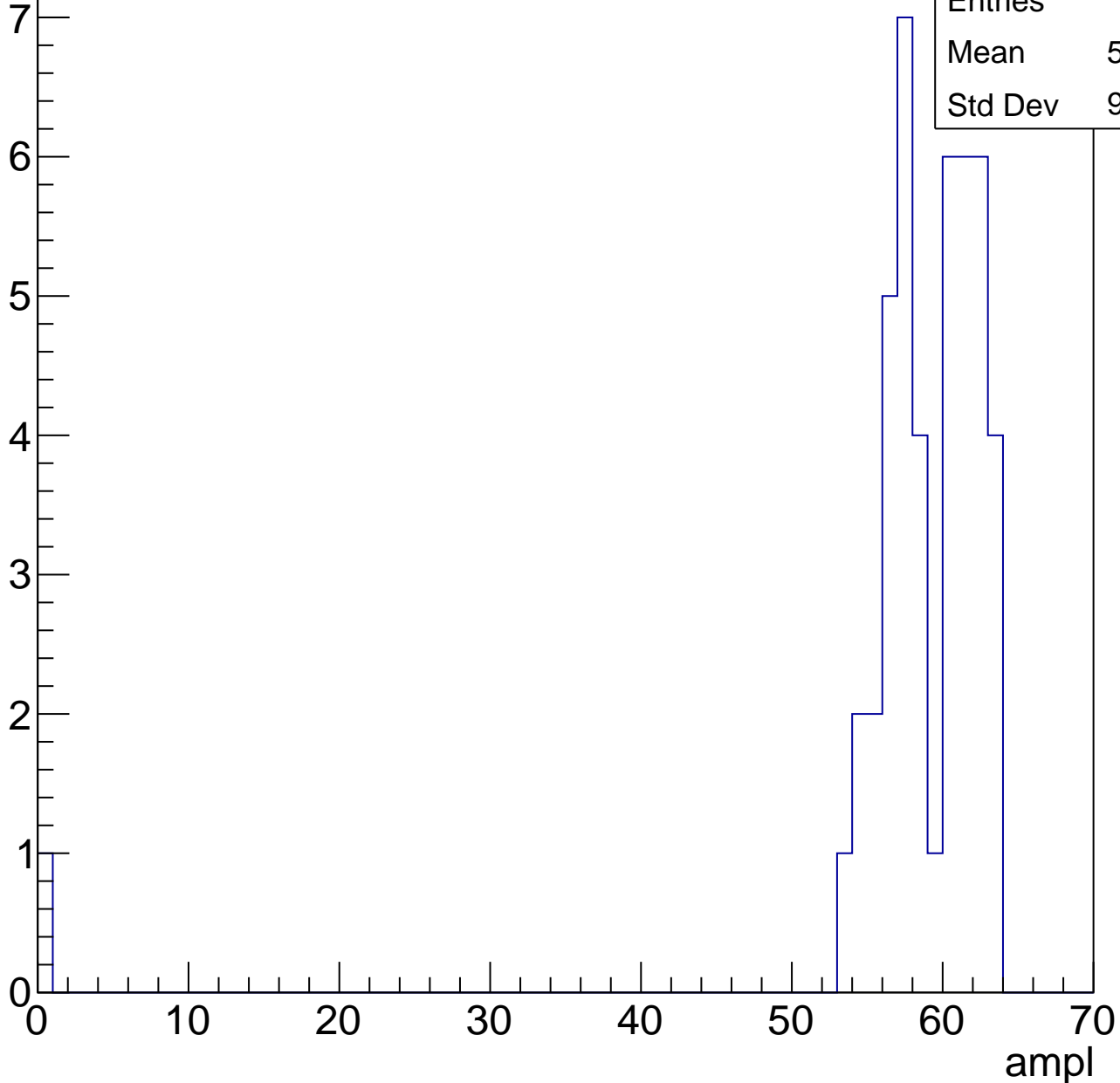


# B1L103S, U9-ch76, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	45
Mean	57.58
Std Dev	9.108

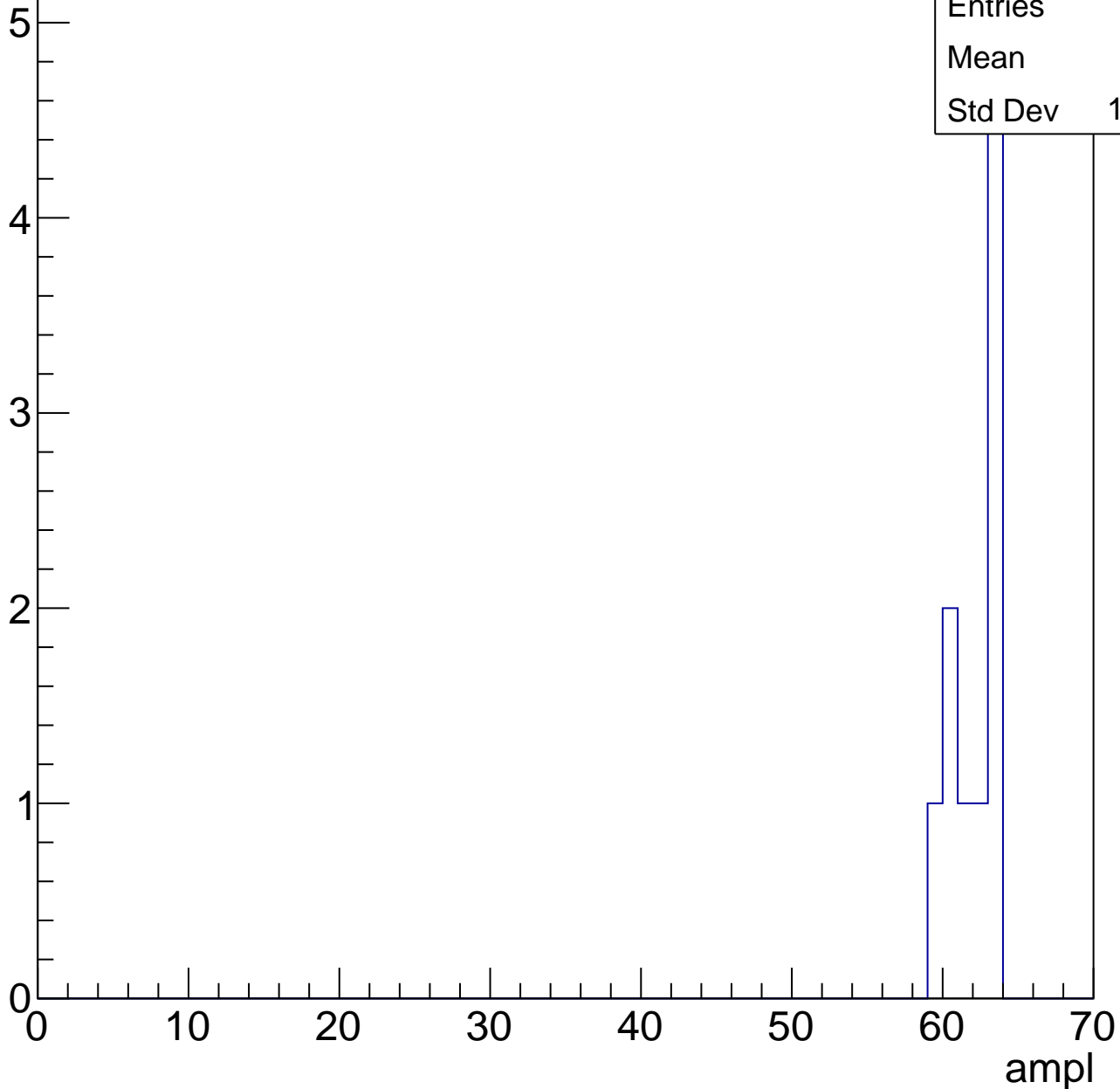


# B1L103S, U9-ch76, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	10
Mean	61.7
Std Dev	1.487

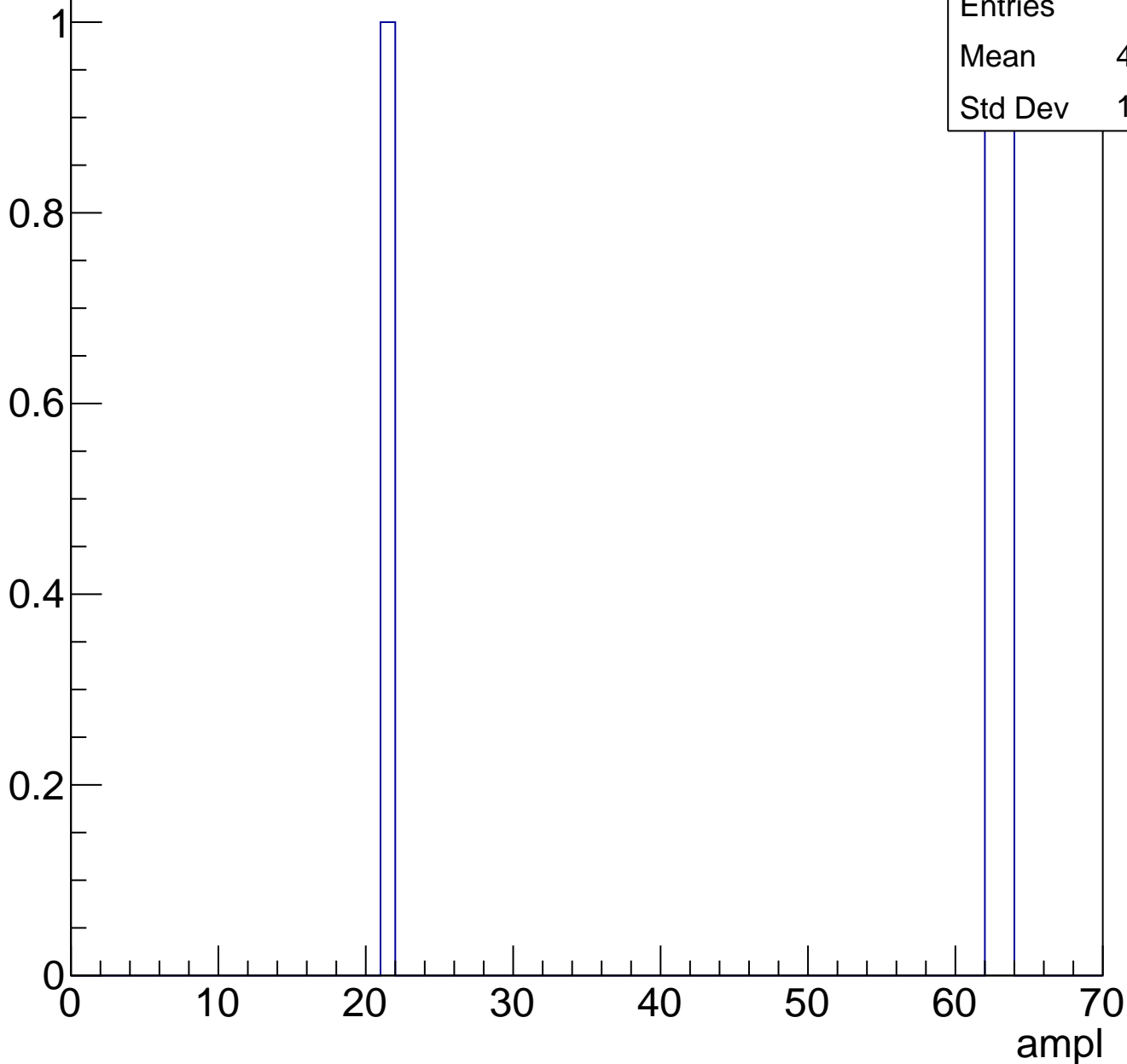




# B1L103S, U9-ch76, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U9-ch77, adc0

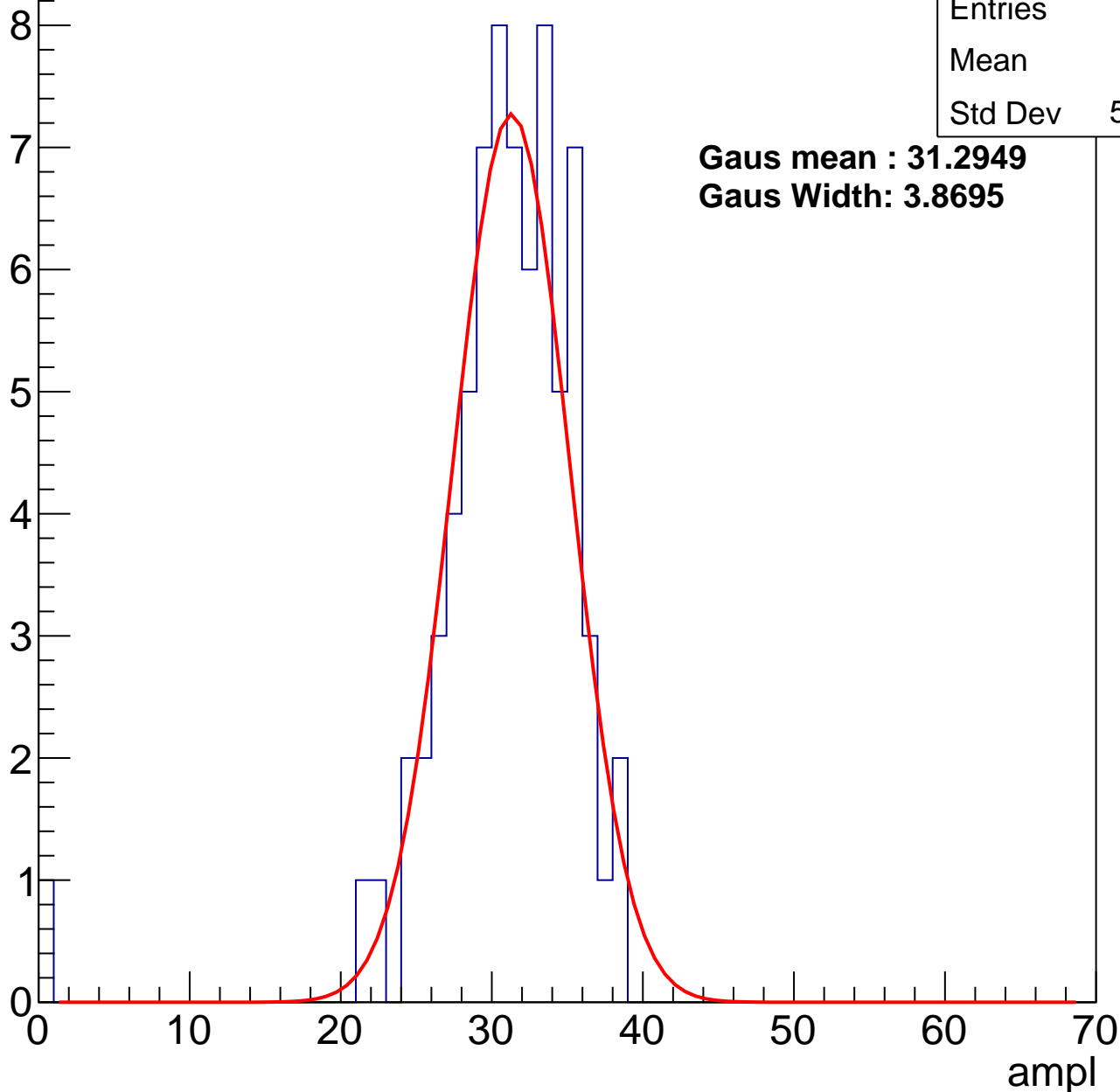
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	73
Mean	30.4
Std Dev	5.114

**Gaus mean : 31.2949**

**Gaus Width: 3.8695**



# B1L103S, U9-ch77, adc1

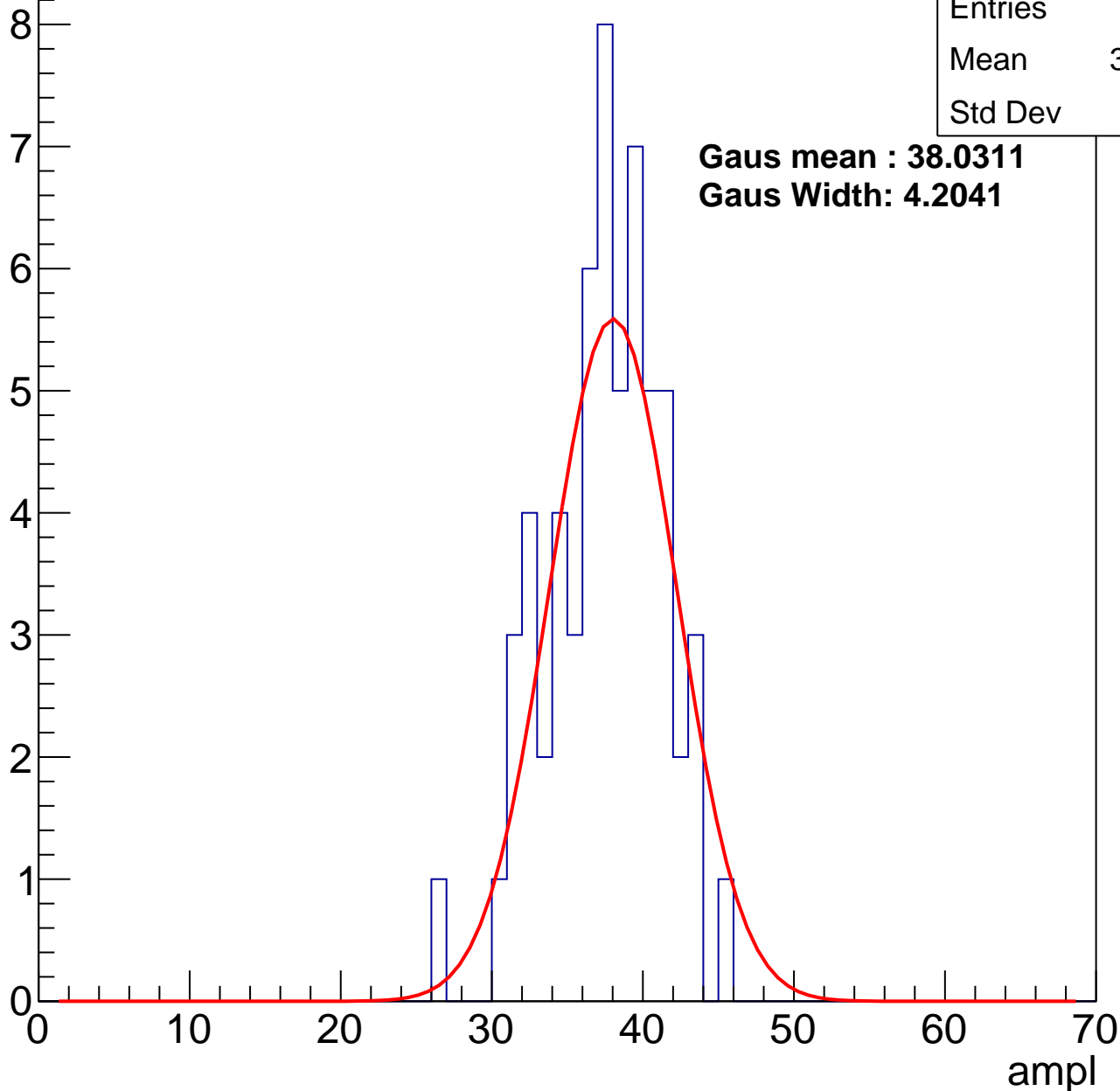
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	60
Mean	37.03
Std Dev	3.75

**Gaus mean : 38.0311**

**Gaus Width: 4.2041**



# B1L103S, U9-ch77, adc2

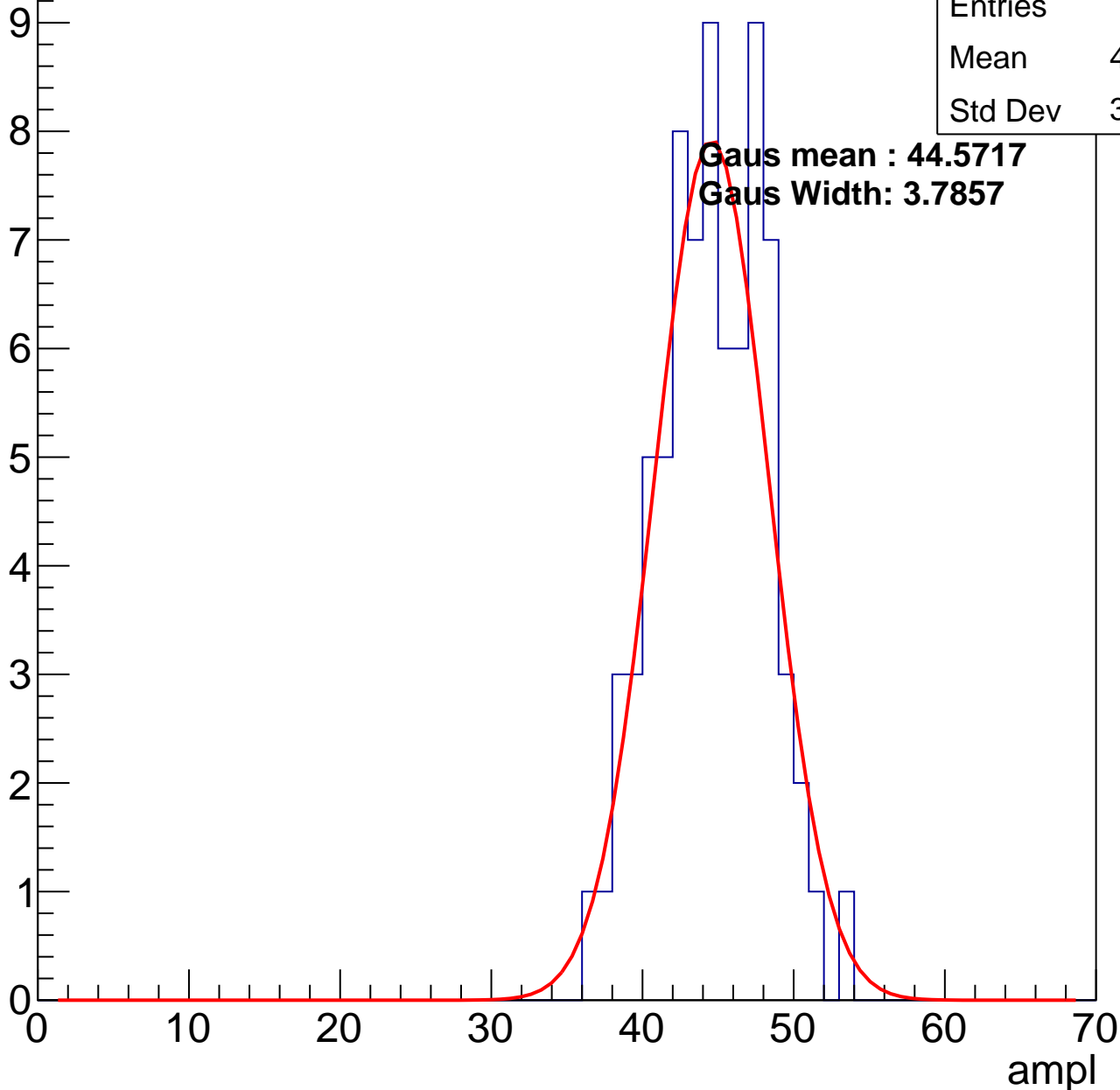
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	77
Mean	44.13
Std Dev	3.529

**Gaus mean : 44.5717**

**Gaus Width: 3.7857**

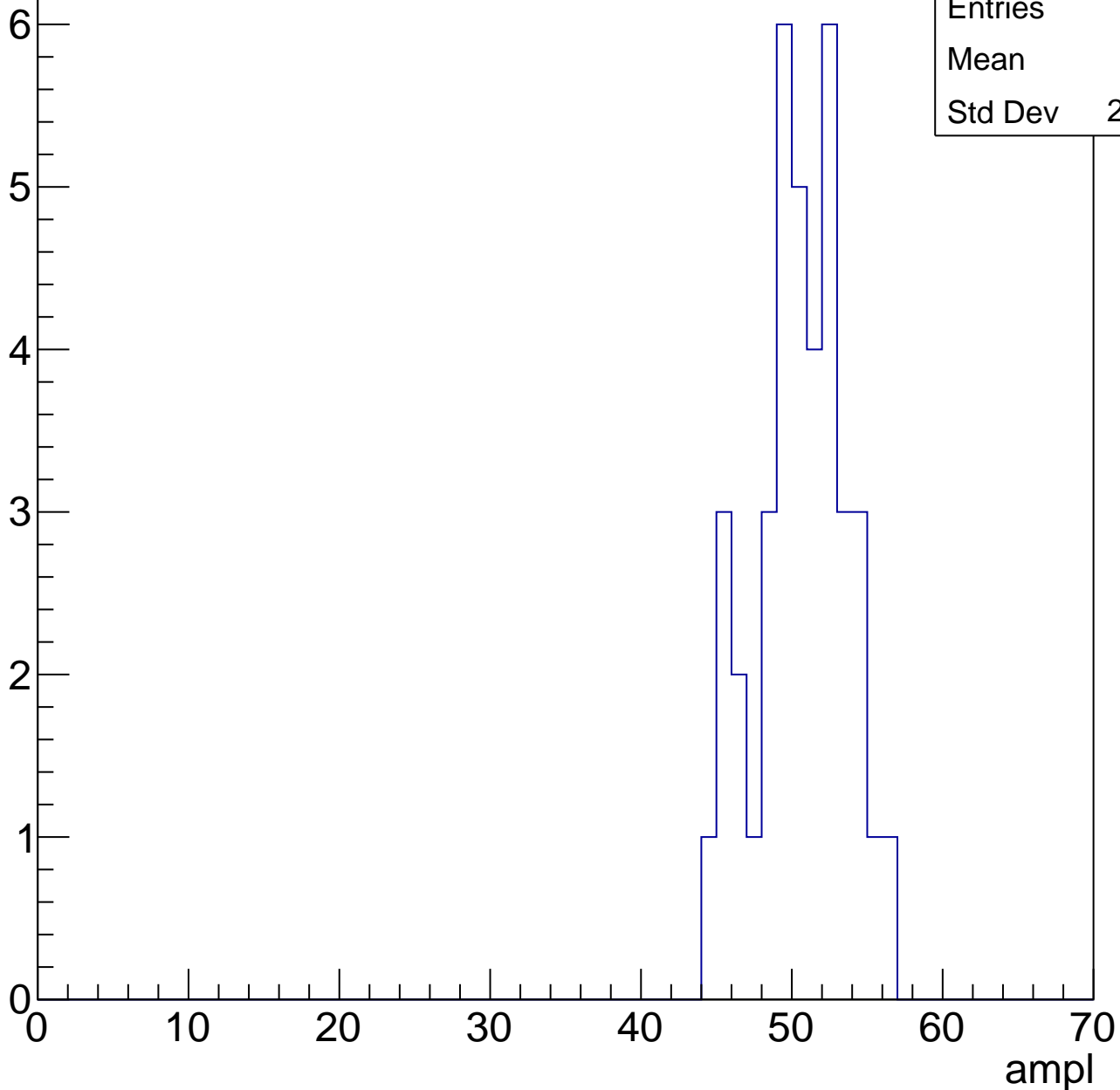


# B1L103S, U9-ch77, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	39
Mean	50.1
Std Dev	2.925



# B1L103S, U9-ch77, adc4

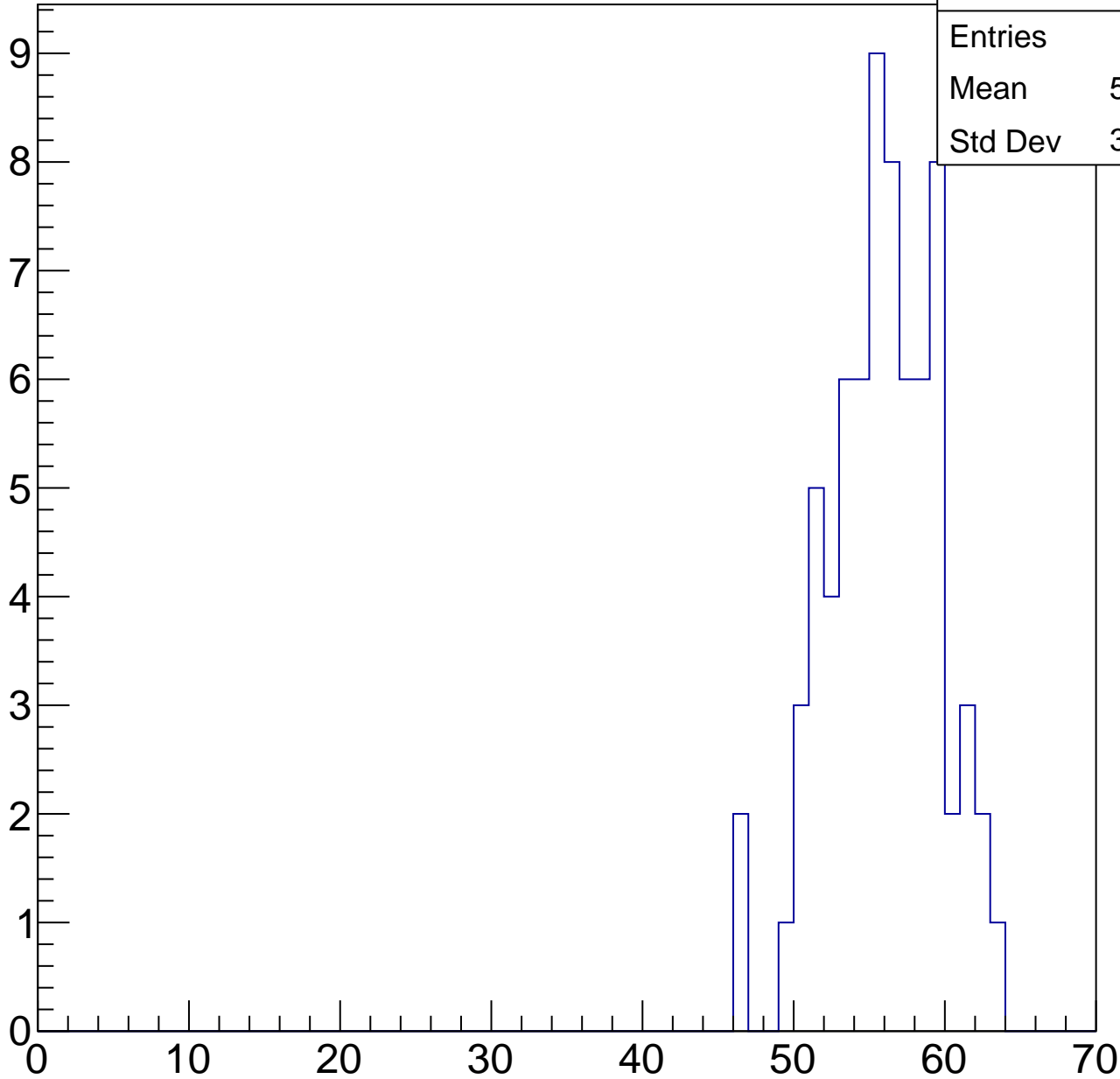
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	72
Mean	55.43
Std Dev	3.613

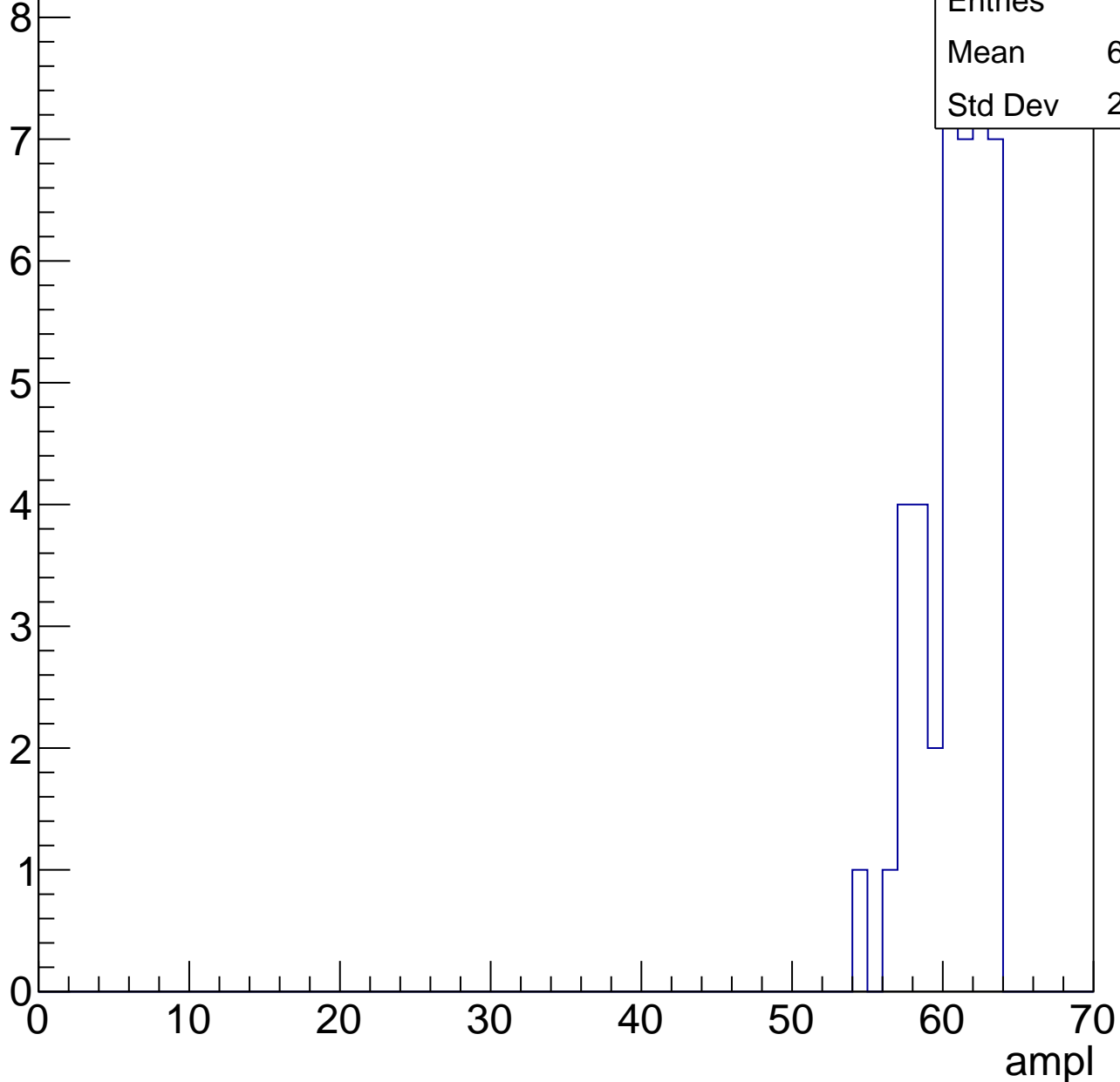
ampl



# B1L103S, U9-ch77, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	42
Mean	60.29
Std Dev	2.207

# B1L103S, U9-ch77, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U9-ch77, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L103S, U9-ch78, adc0

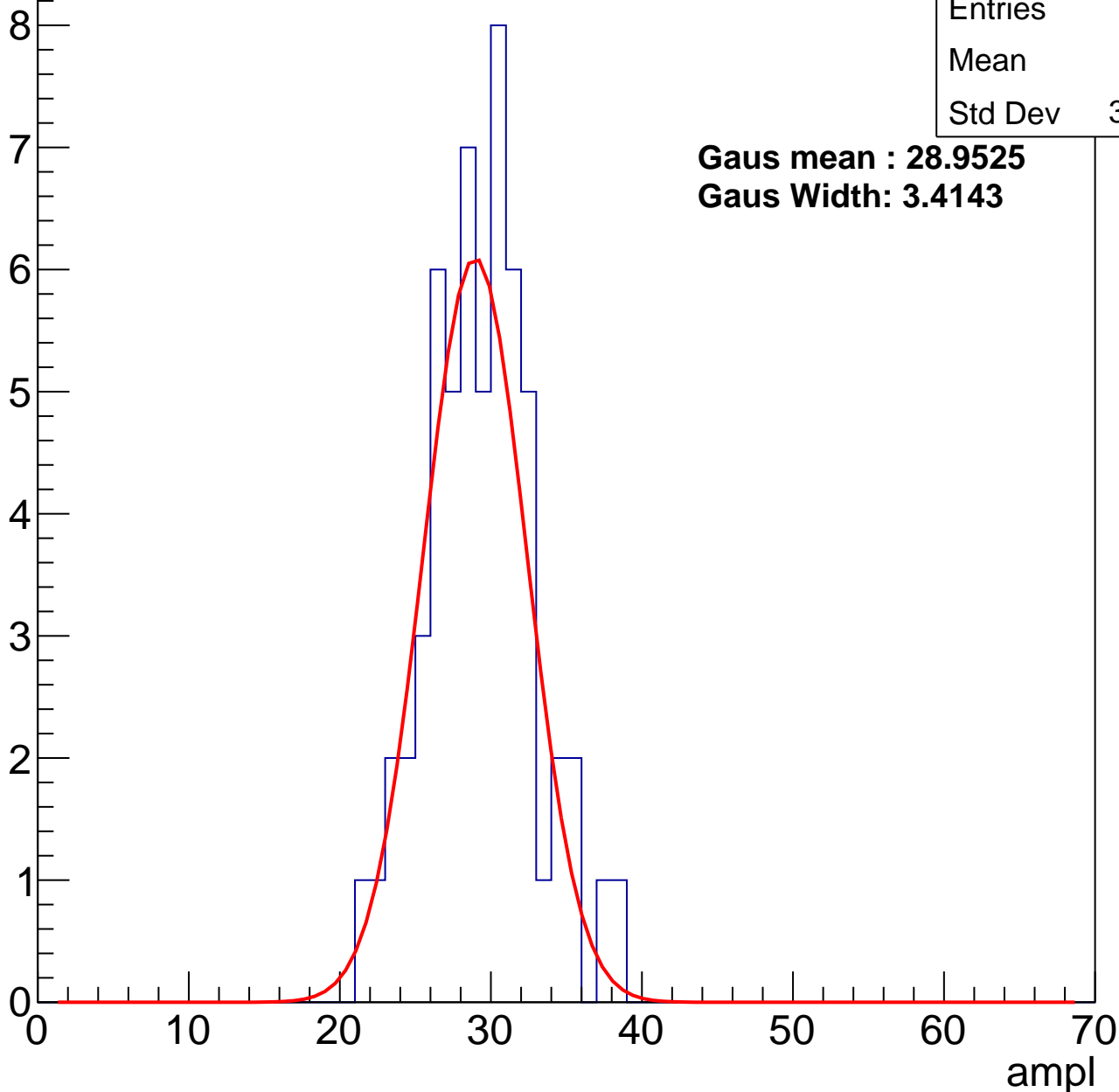
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	58
Mean	28.9
Std Dev	3.532

**Gaus mean : 28.9525**

**Gaus Width: 3.4143**



# B1L103S, U9-ch78, adc1

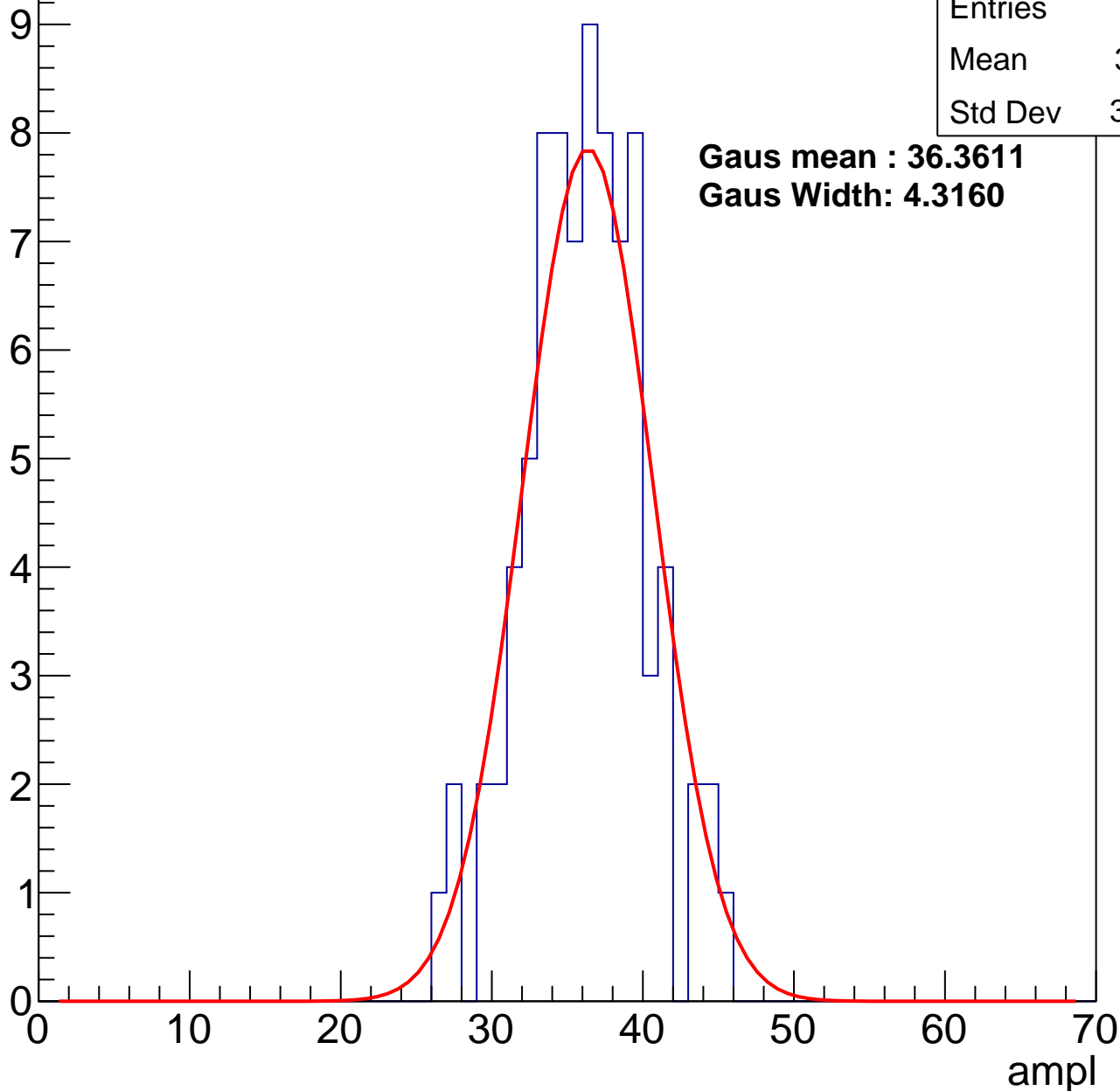
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	83
Mean	35.71
Std Dev	3.926

**Gaus mean : 36.3611**

**Gaus Width: 4.3160**



# B1L103S, U9-ch78, adc2

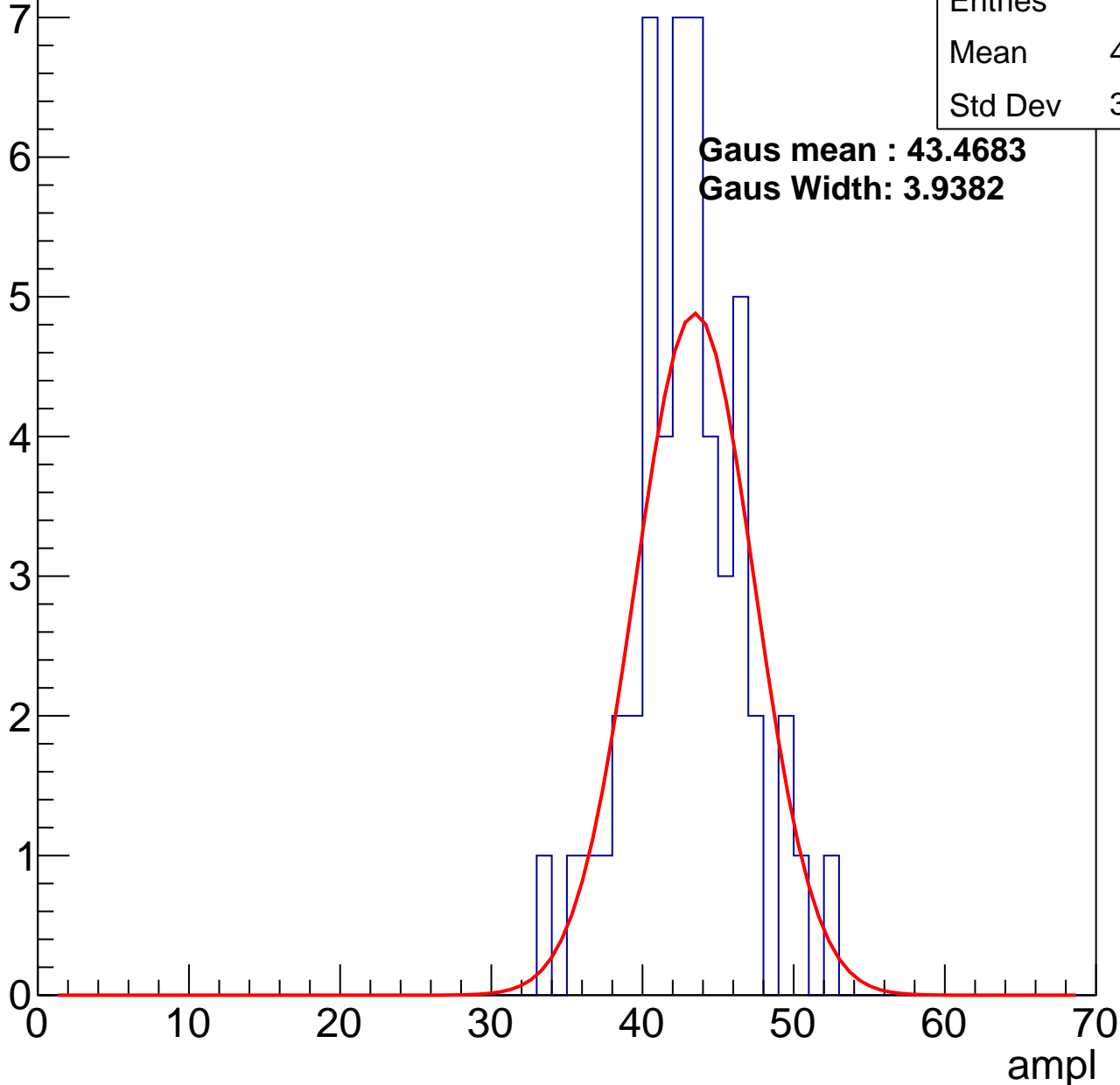
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	51
Mean	42.53
Std Dev	3.707

**Gaus mean : 43.4683**

**Gaus Width: 3.9382**

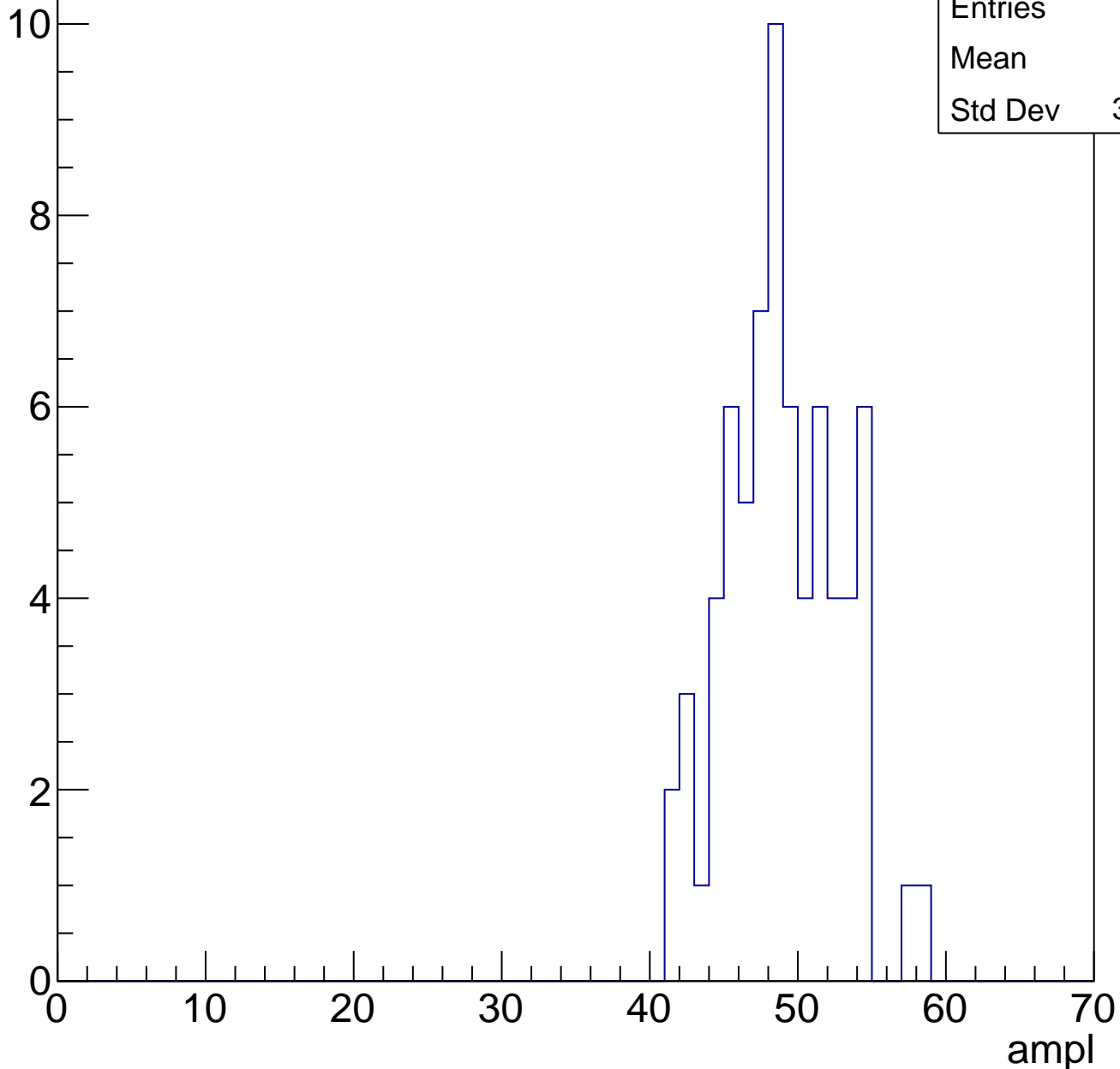


# B1L103S, U9-ch78, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	70
Mean	48.5
Std Dev	3.771

Entry

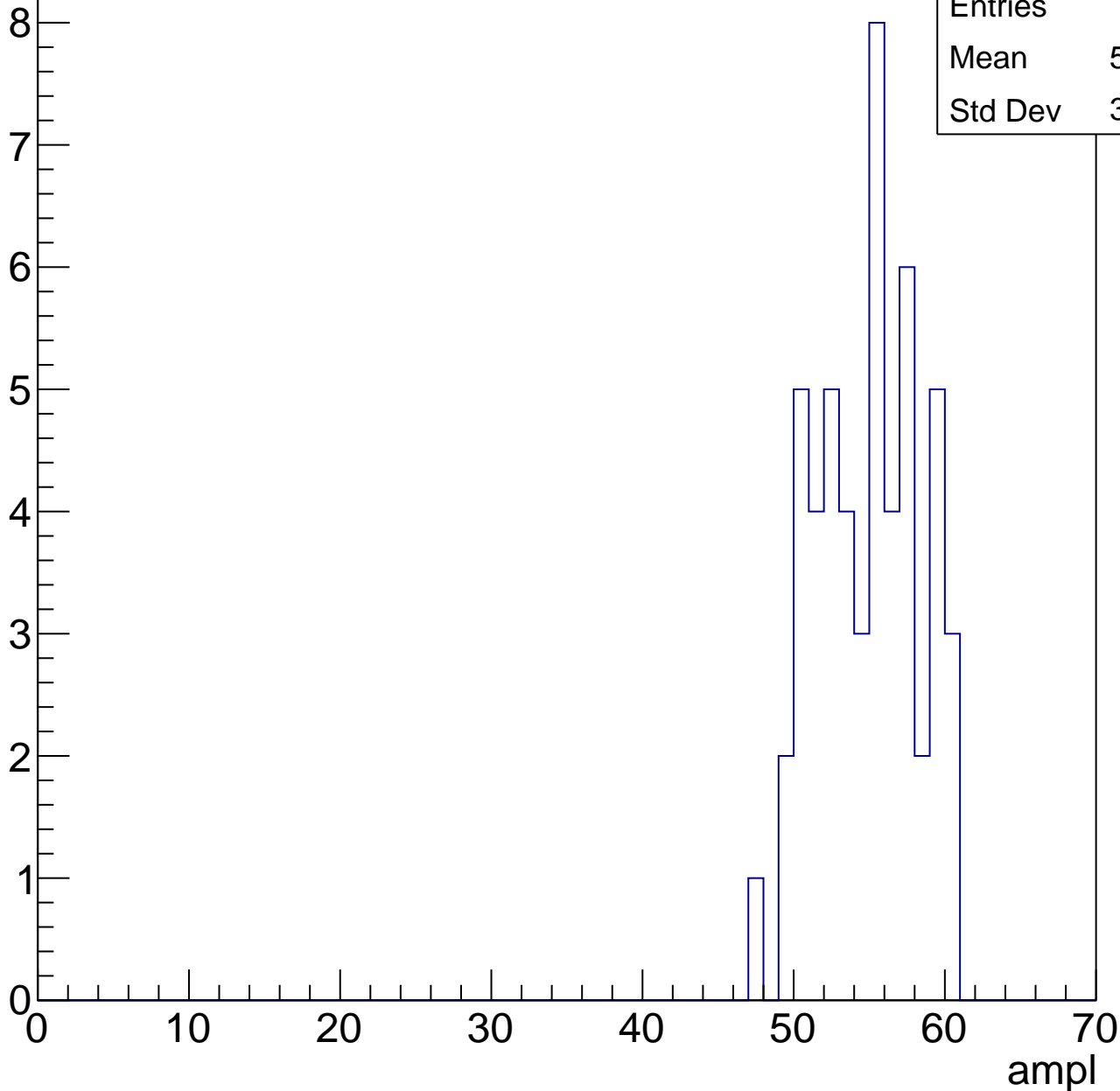


# B1L103S, U9-ch78, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	52
Mean	54.42
Std Dev	3.319

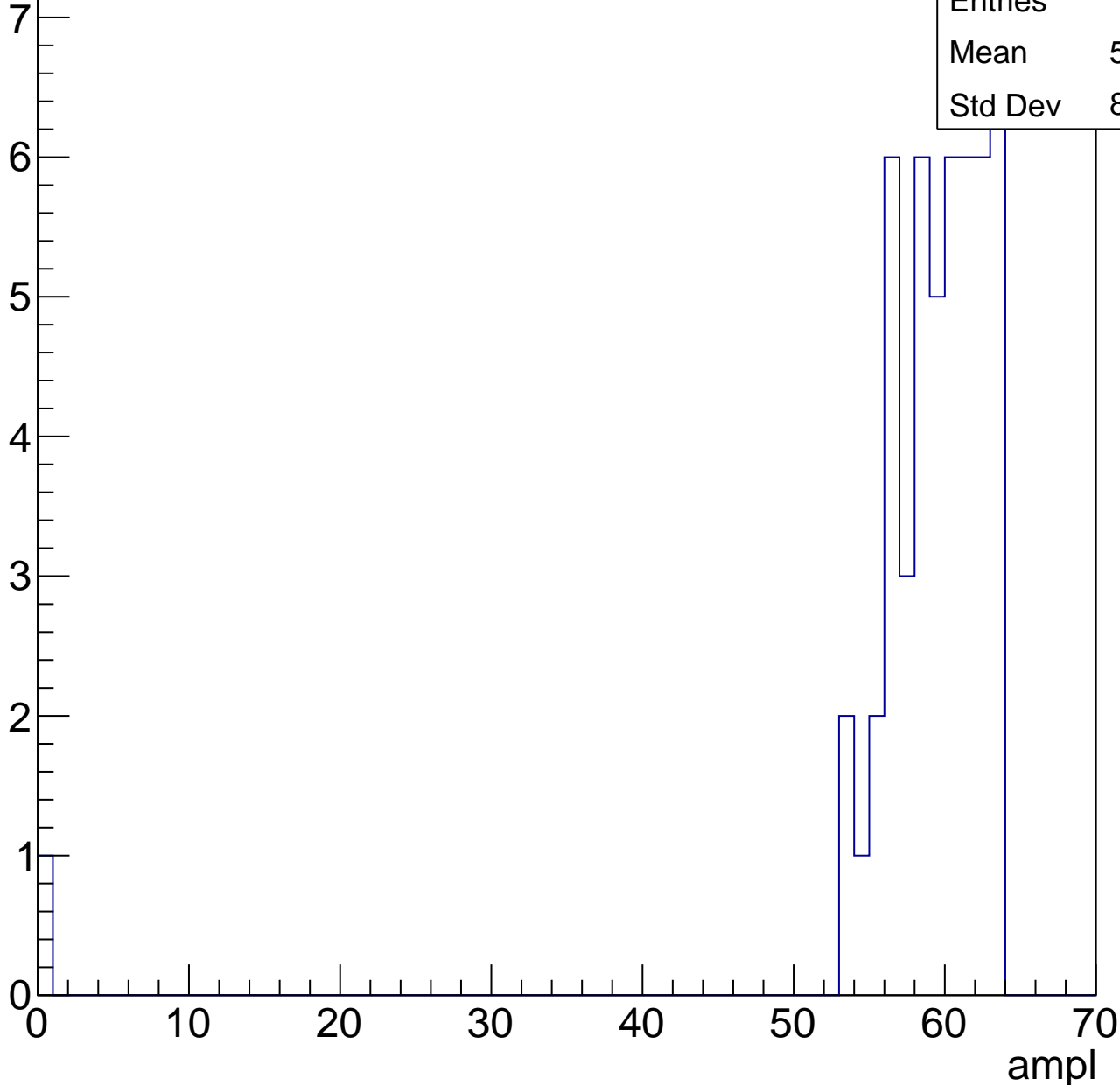


# B1L103S, U9-ch78, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

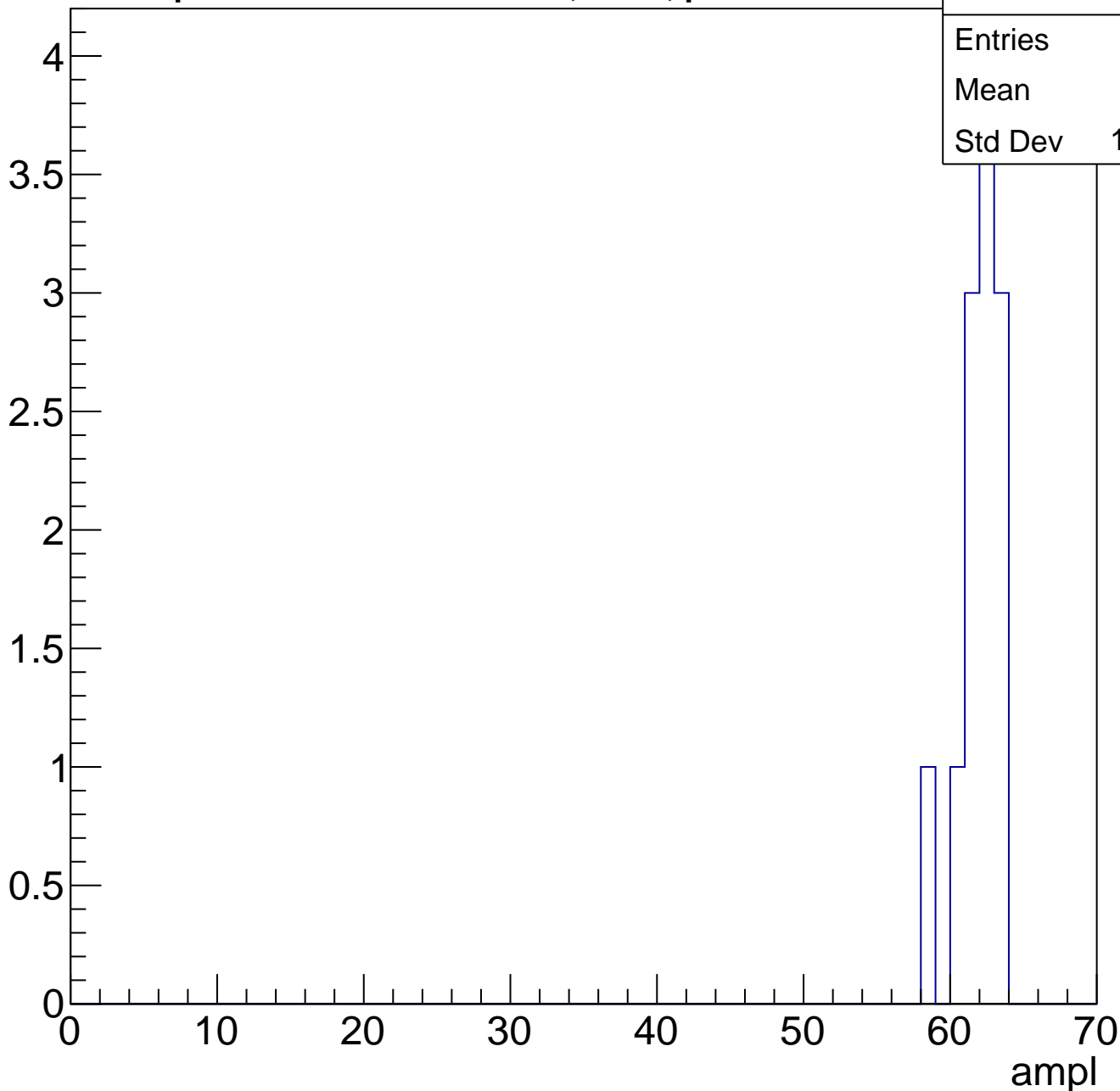
Entries	51
Mean	58.02
Std Dev	8.665



# B1L103S, U9-ch78, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	12
Mean	61.5
Std Dev	1.384



# B1L103S, U9-ch78, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U9-ch79, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	74
Mean	29.03
Std Dev	4.731

**Gaus mean : 30.5750**

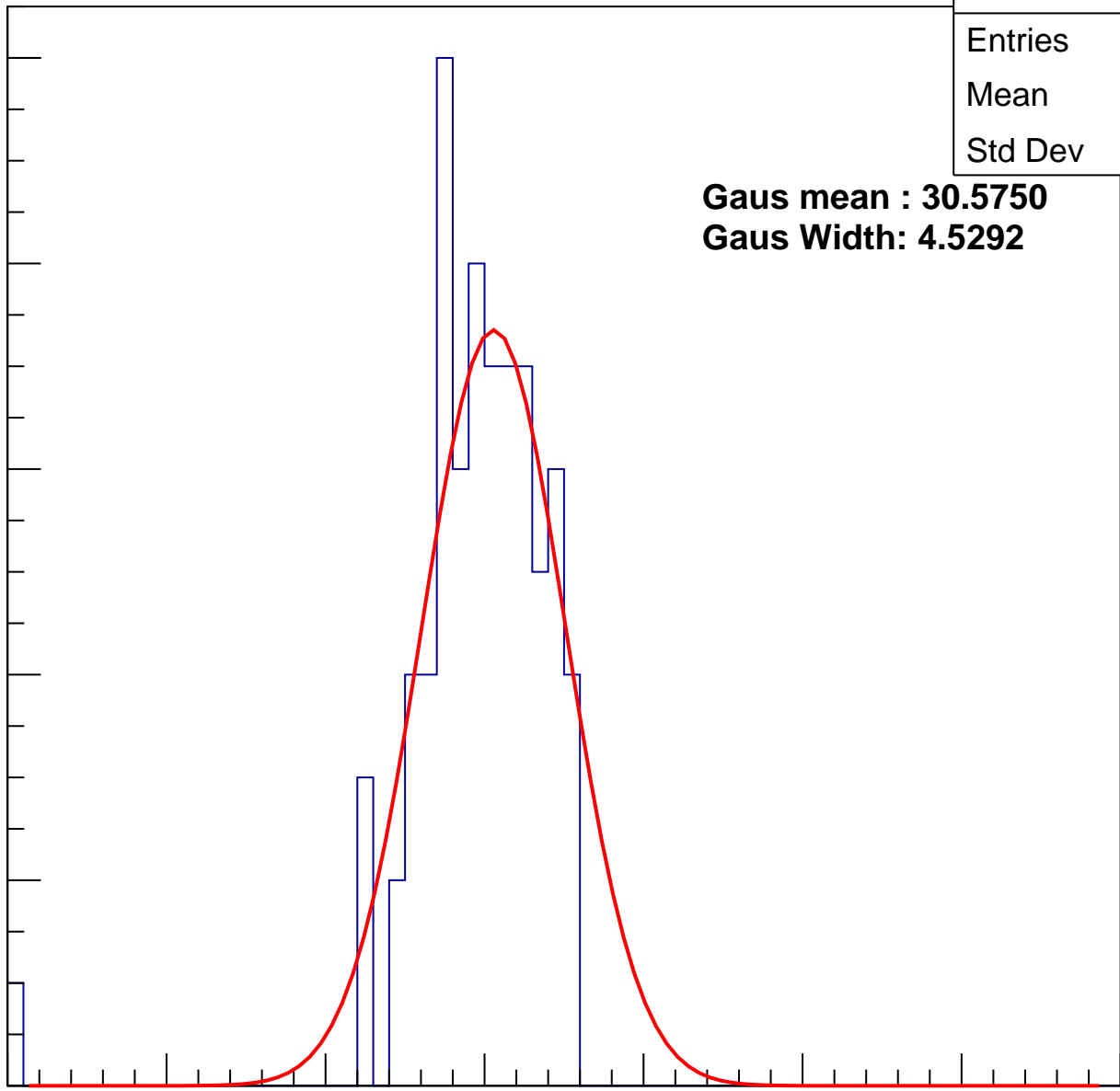
**Gaus Width: 4.5292**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U9-ch79, adc1

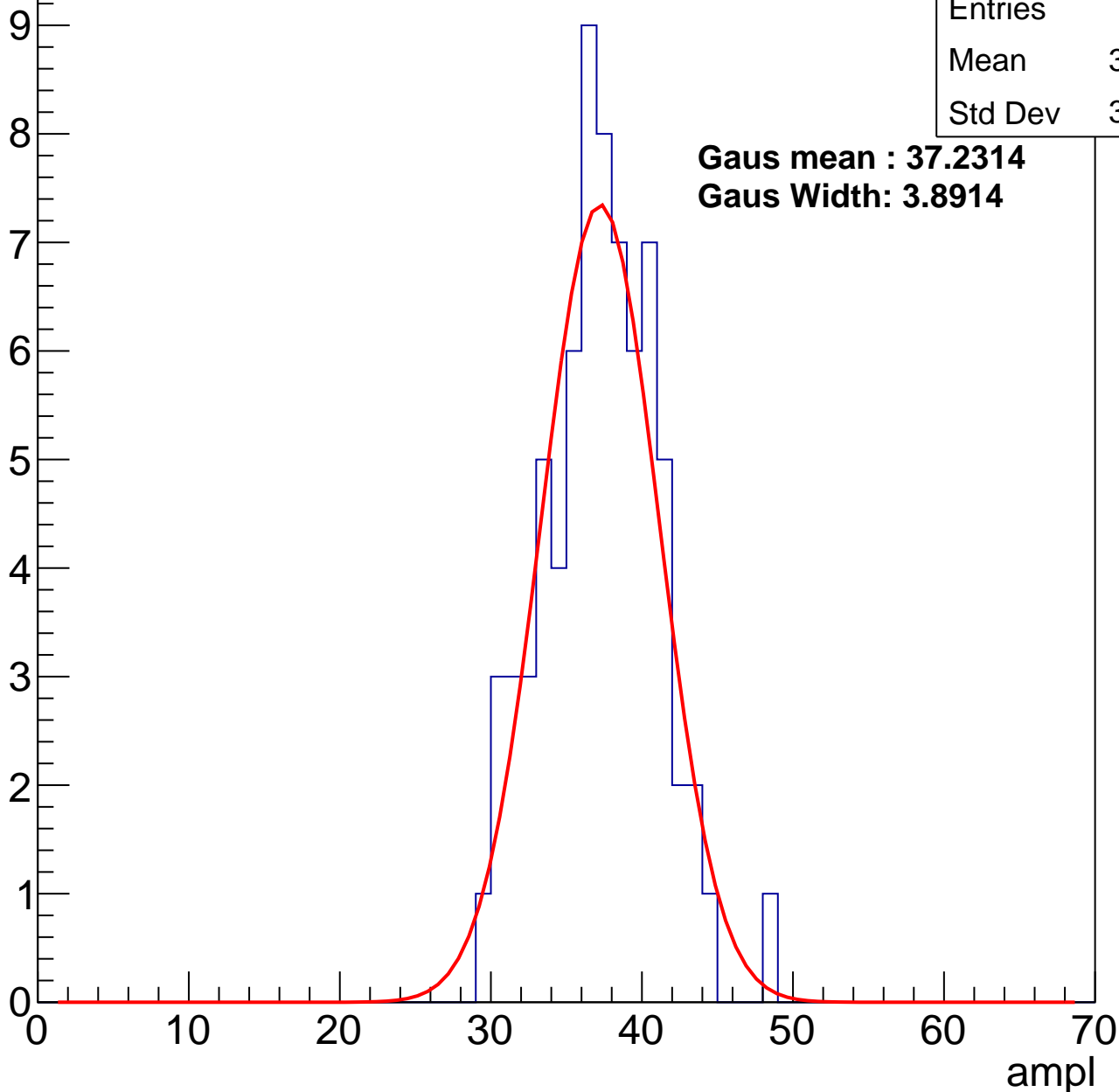
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	73
Mean	36.79
Std Dev	3.712

**Gaus mean : 37.2314**

**Gaus Width: 3.8914**



# B1L103S, U9-ch79, adc2

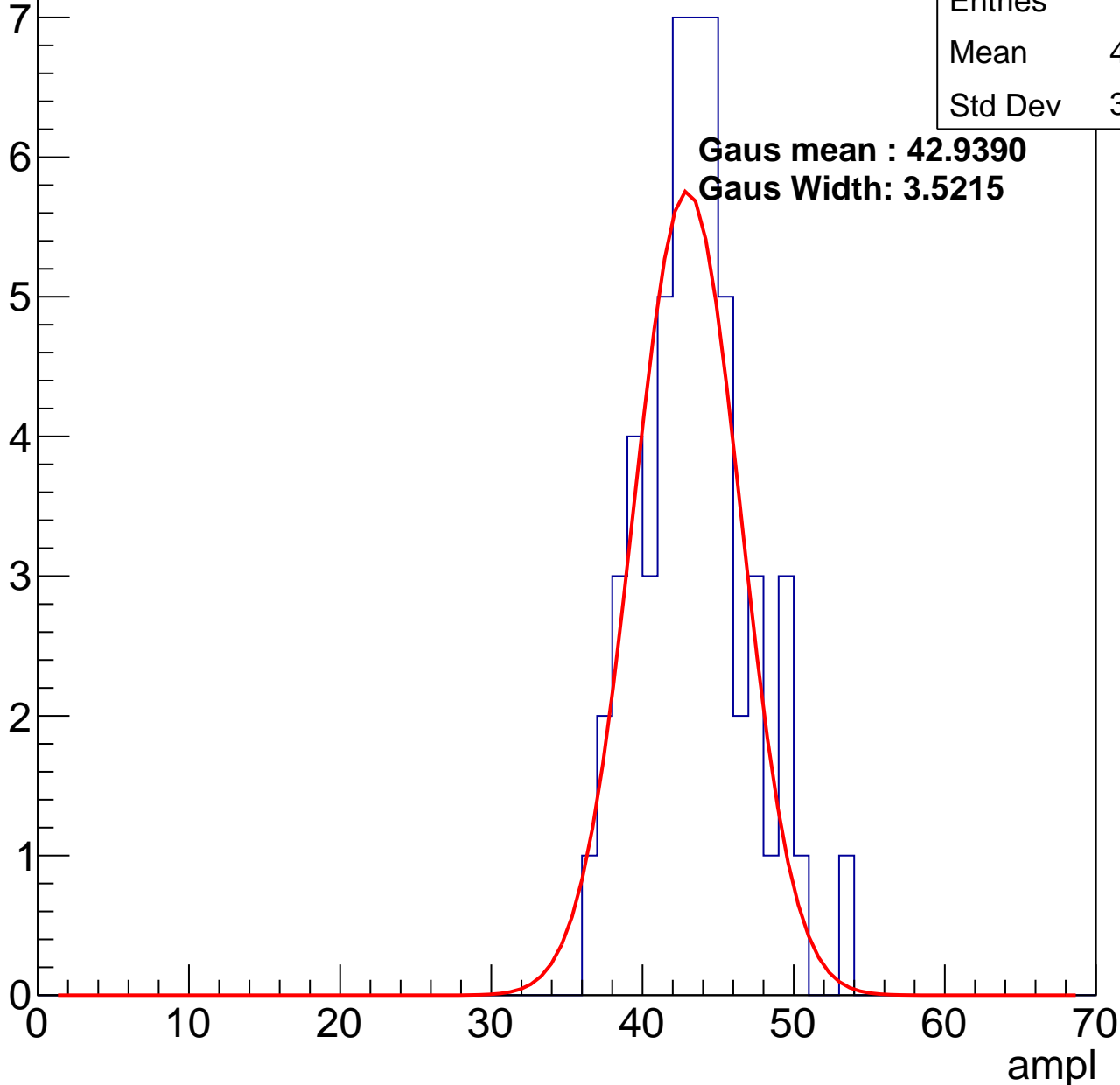
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	55
Mean	42.98
Std Dev	3.539

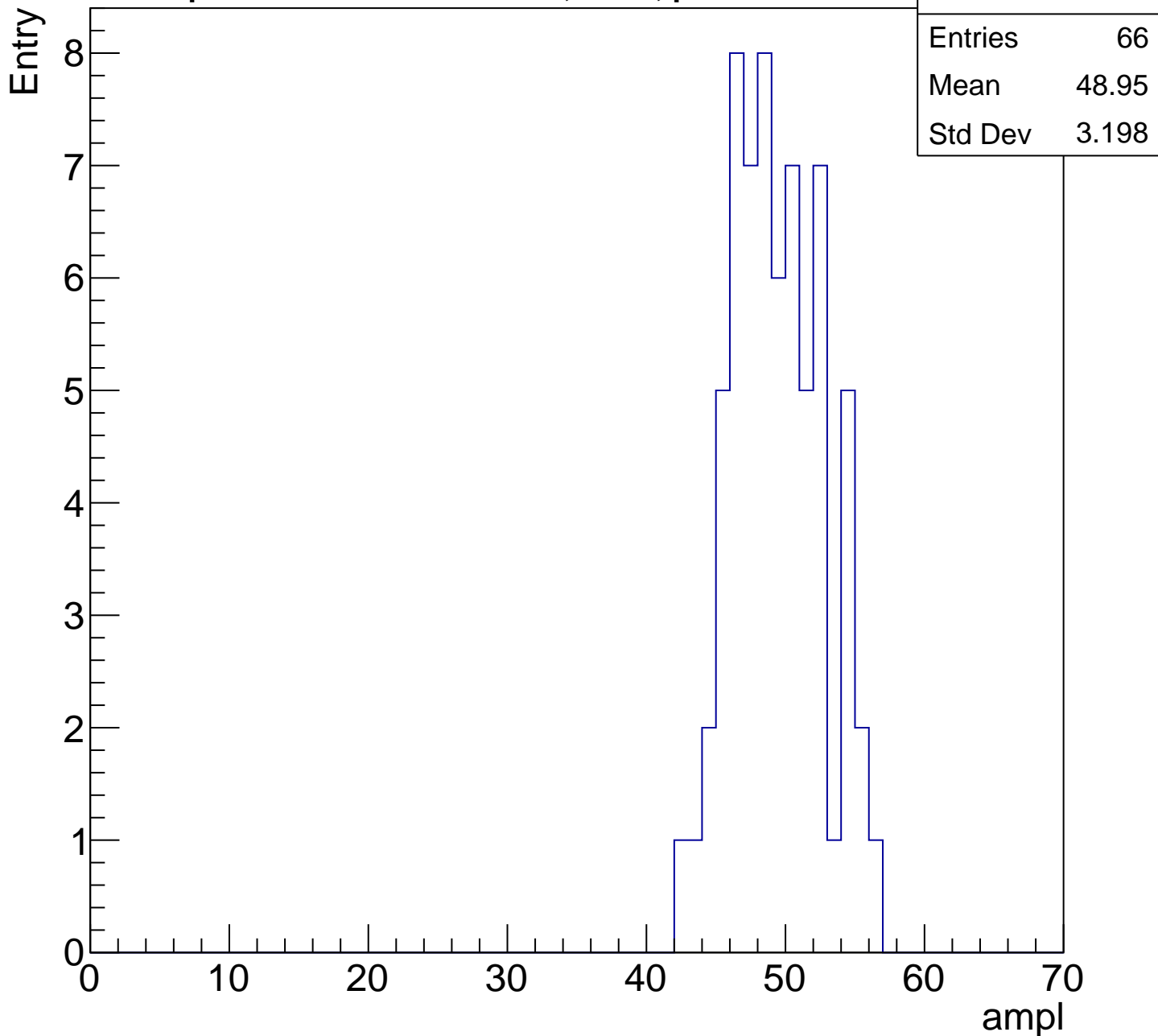
**Gaus mean : 42.9390**

**Gaus Width: 3.5215**



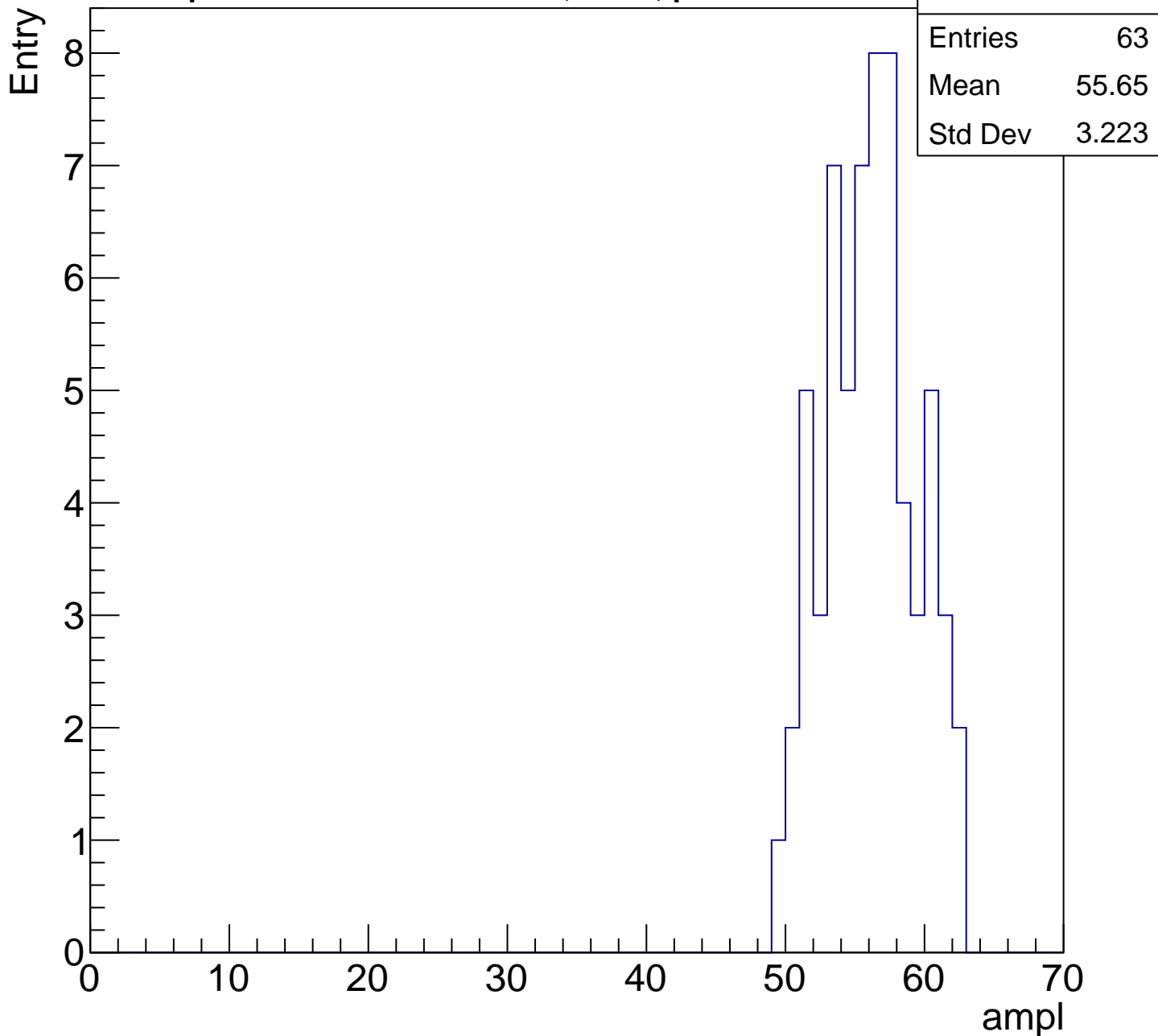
# B1L103S, U9-ch79, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U9-ch79, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

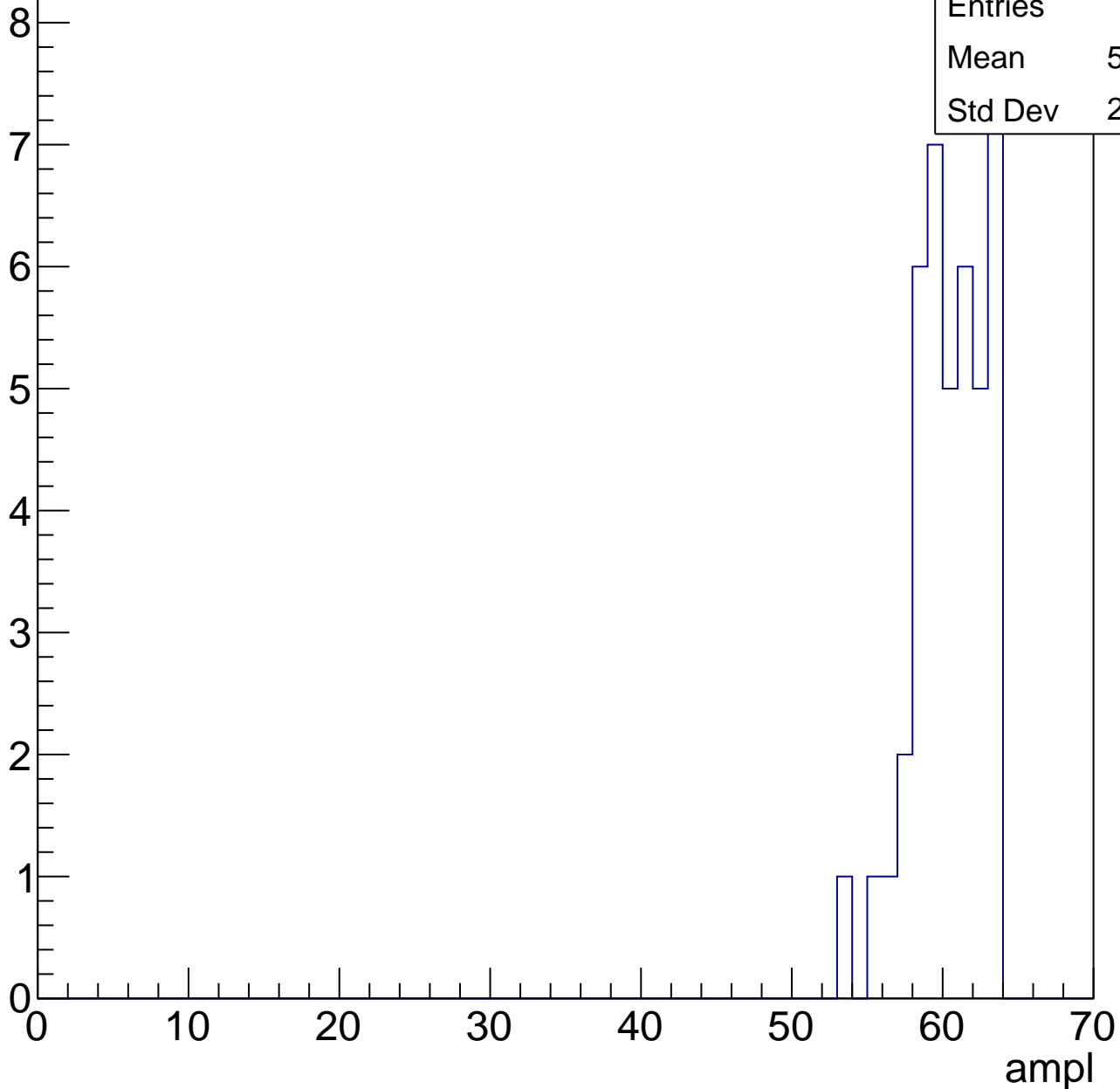


# B1L103S, U9-ch79, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

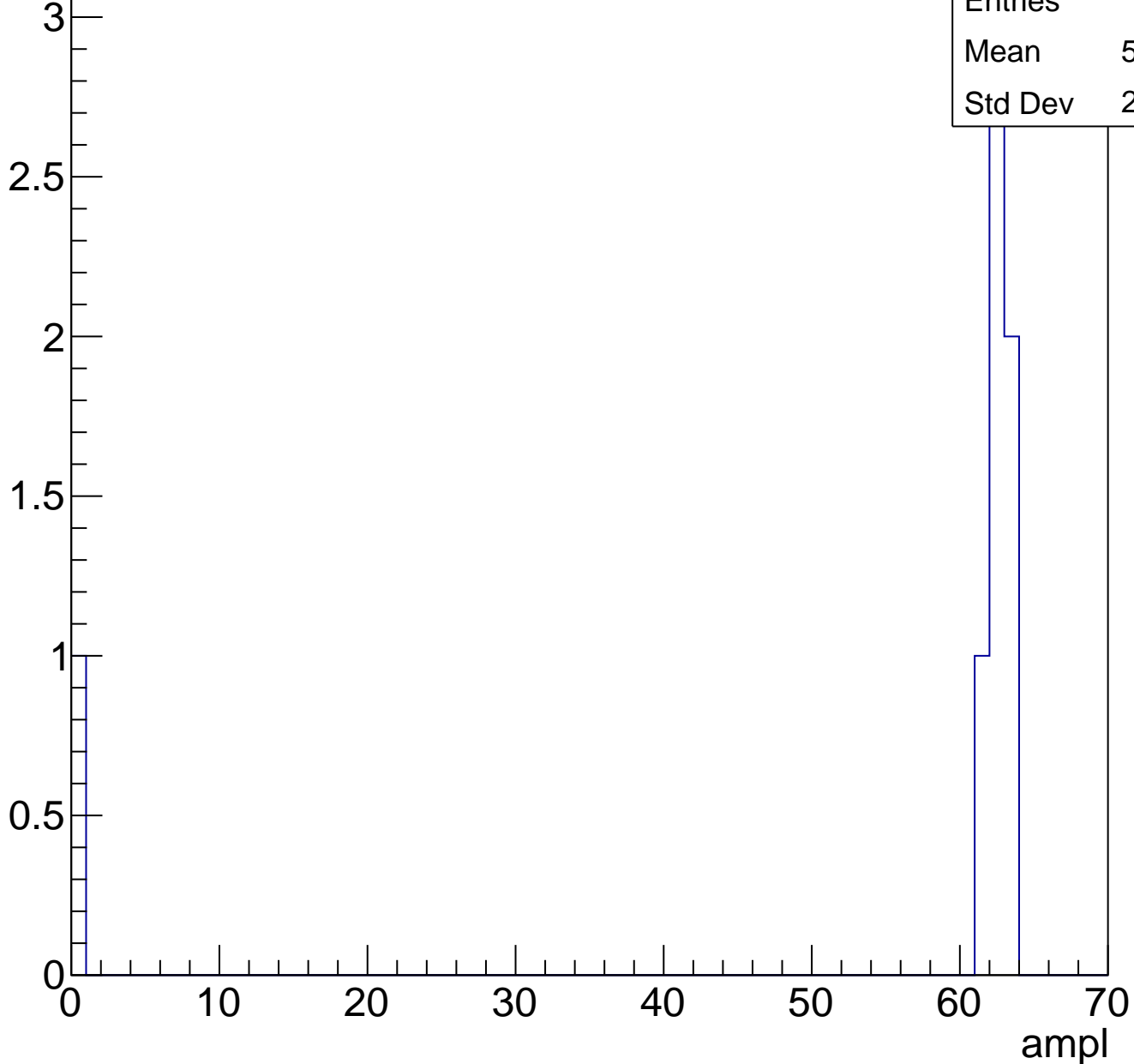
Entries	42
Mean	59.98
Std Dev	2.375



# B1L103S, U9-ch79, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U9-ch79, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U9-ch80, adc0

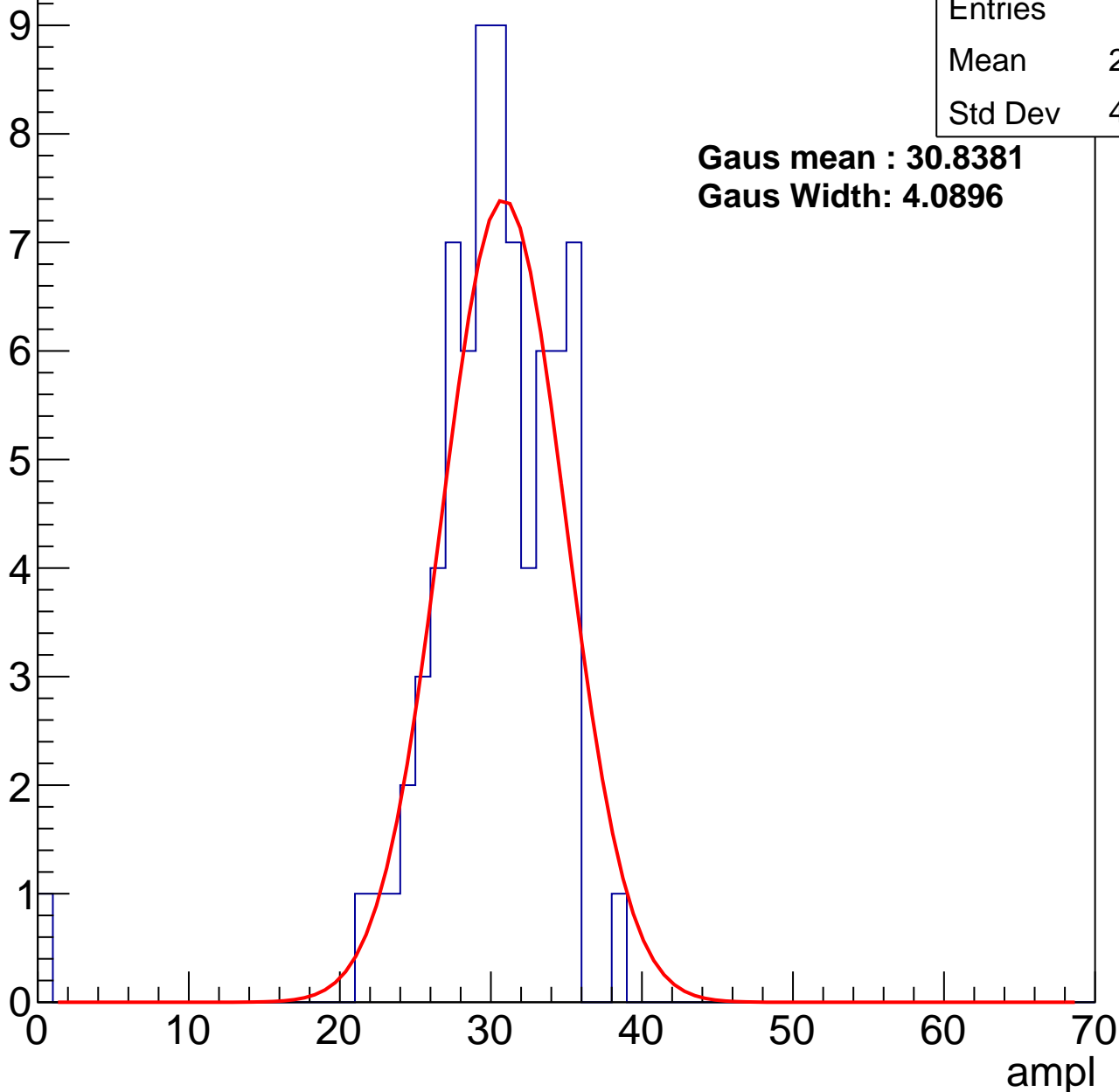
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	75
Mean	29.48
Std Dev	4.889

**Gaus mean : 30.8381**

**Gaus Width: 4.0896**



# B1L103S, U9-ch80, adc1

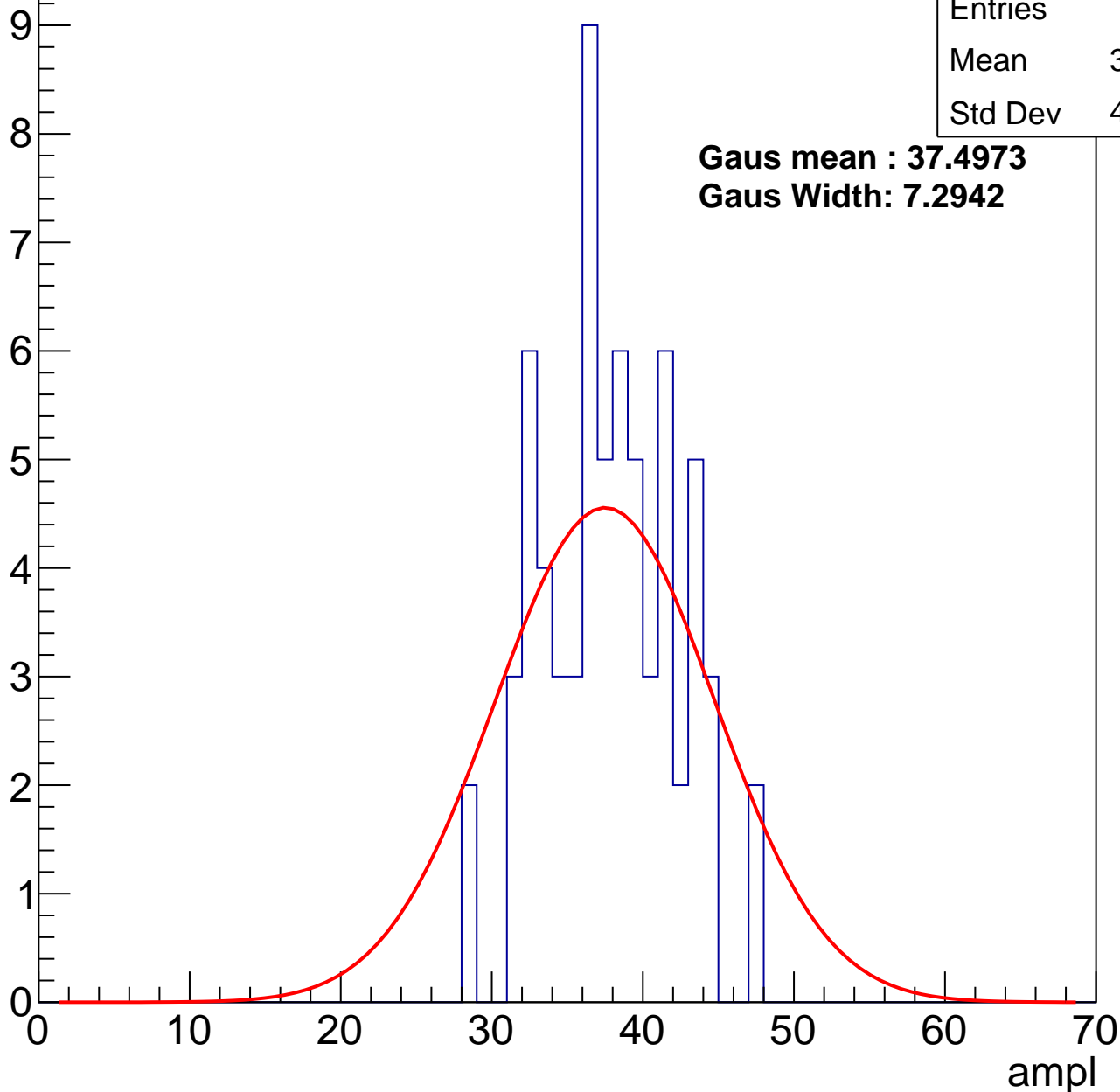
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	37.36
Std Dev	4.318

**Gaus mean : 37.4973**

**Gaus Width: 7.2942**



# B1L103S, U9-ch80, adc2

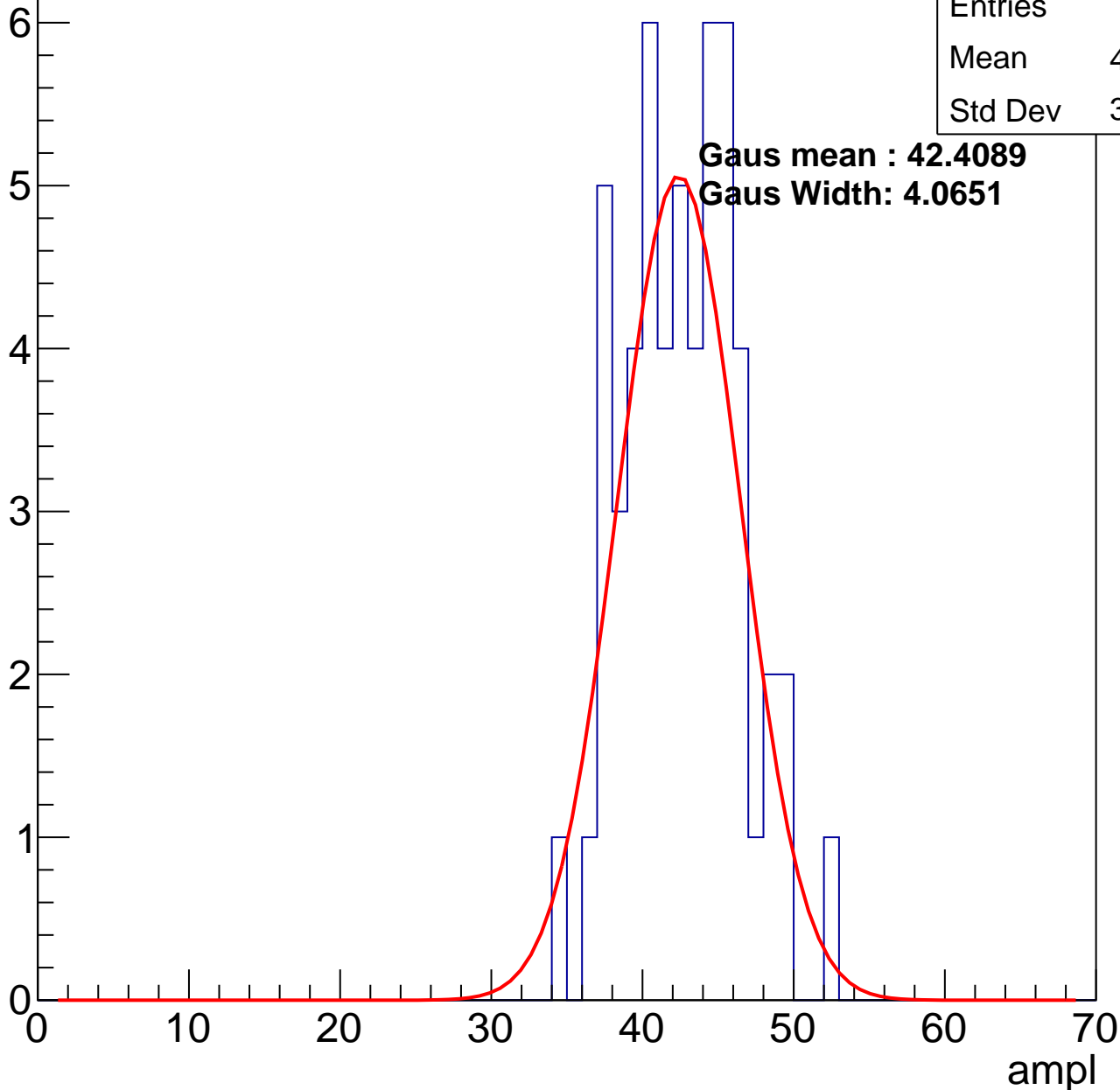
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	55
Mean	42.22
Std Dev	3.755

**Gaus mean : 42.4089**

**Gaus Width: 4.0651**

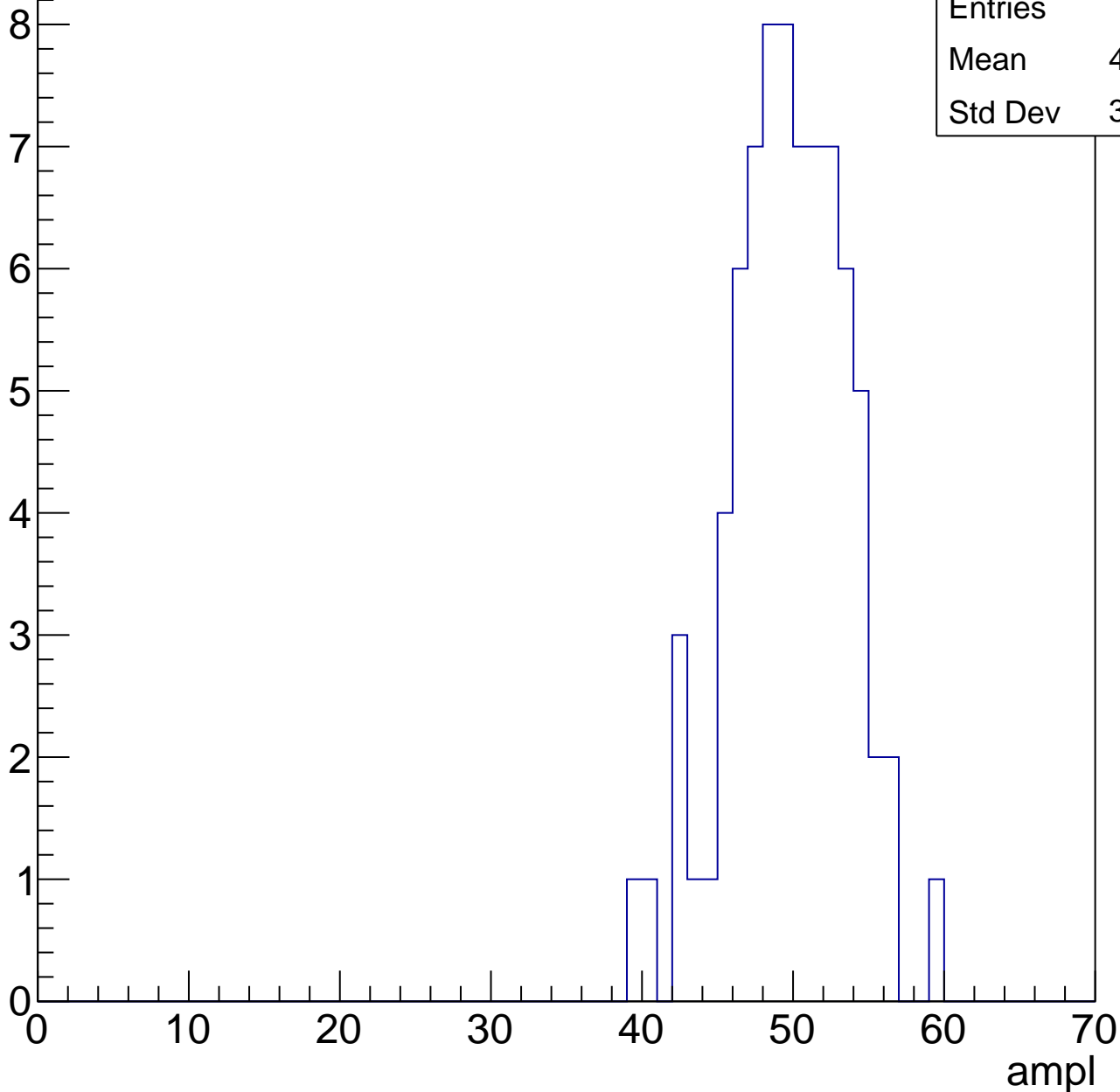


# B1L103S, U9-ch80, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

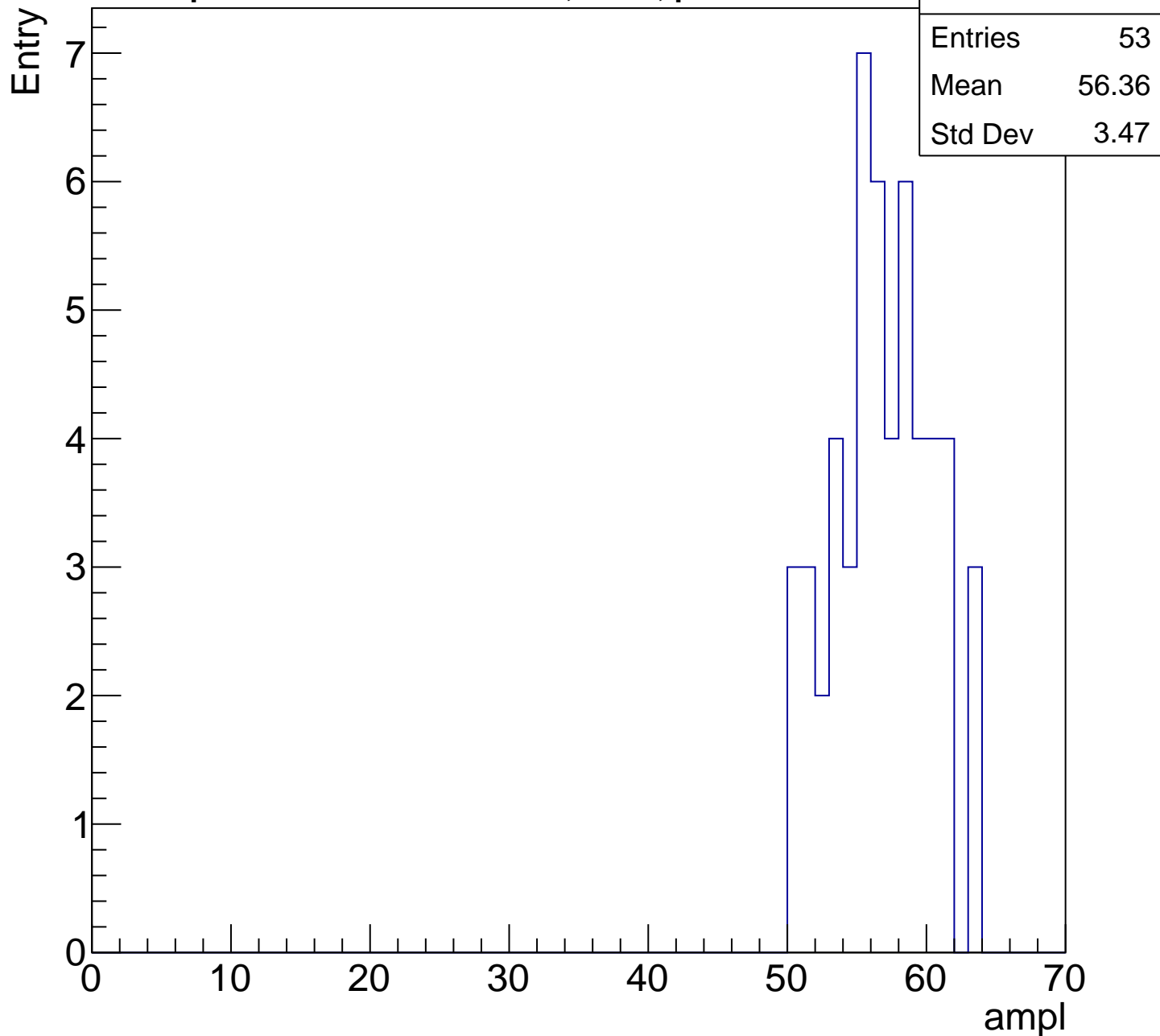
Entry

Entries	77
Mean	49.26
Std Dev	3.825



# B1L103S, U9-ch80, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

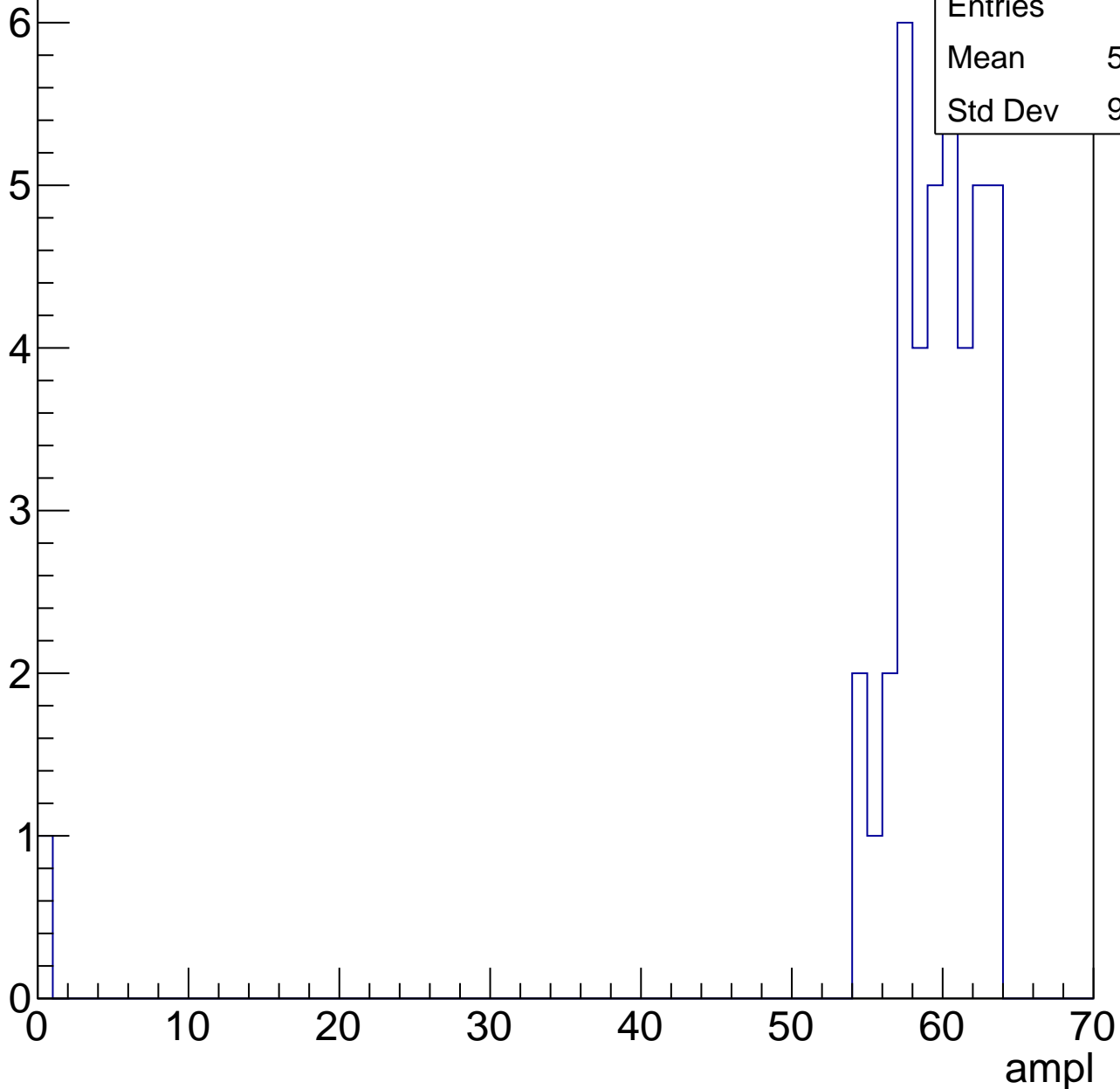


# B1L103S, U9-ch80, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	41
Mean	57.88
Std Dev	9.485

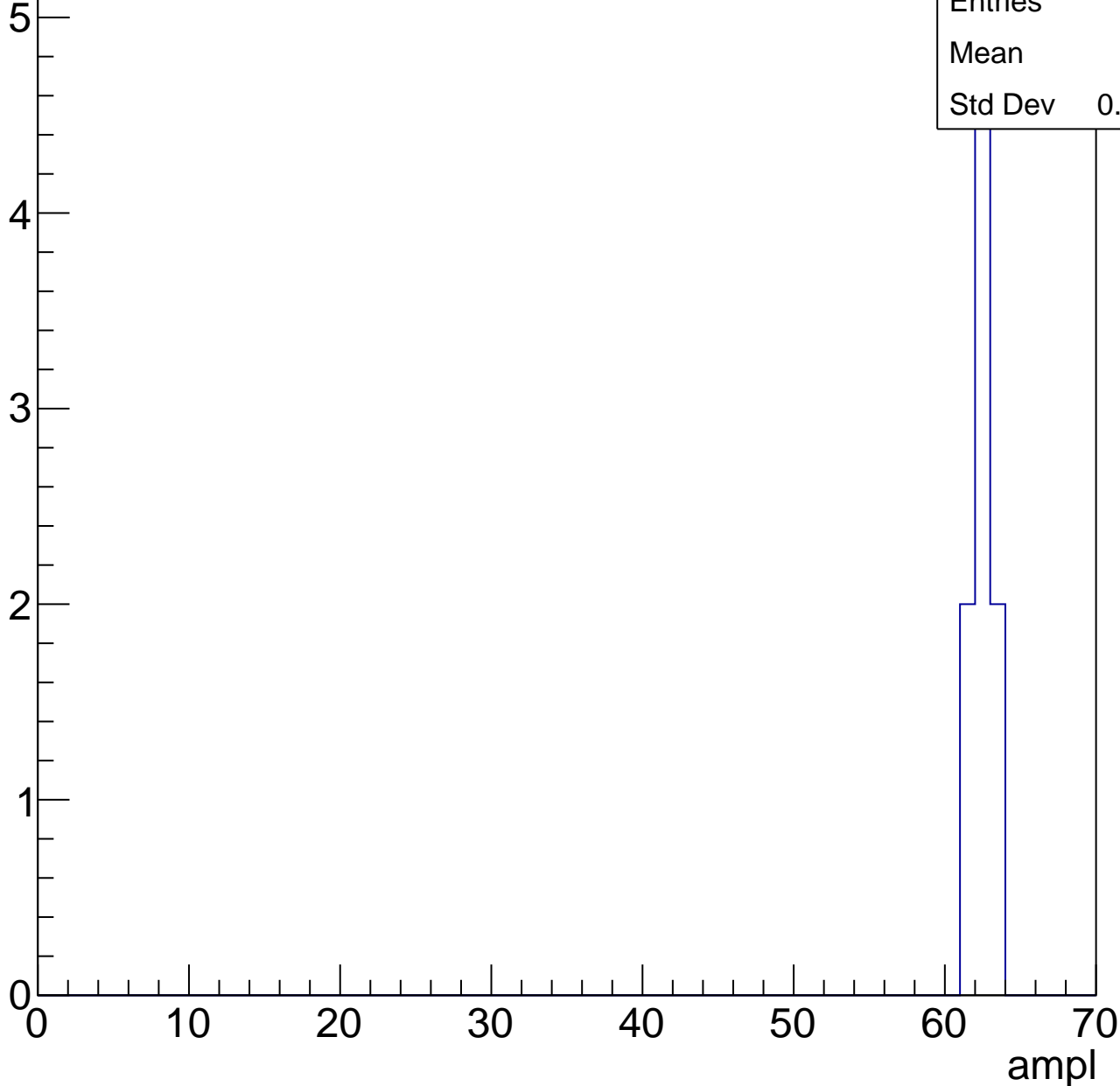


# B1L103S, U9-ch80, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	9
Mean	62
Std Dev	0.6667





# B1L103S, U9-ch80, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L103S, U9-ch81, adc0

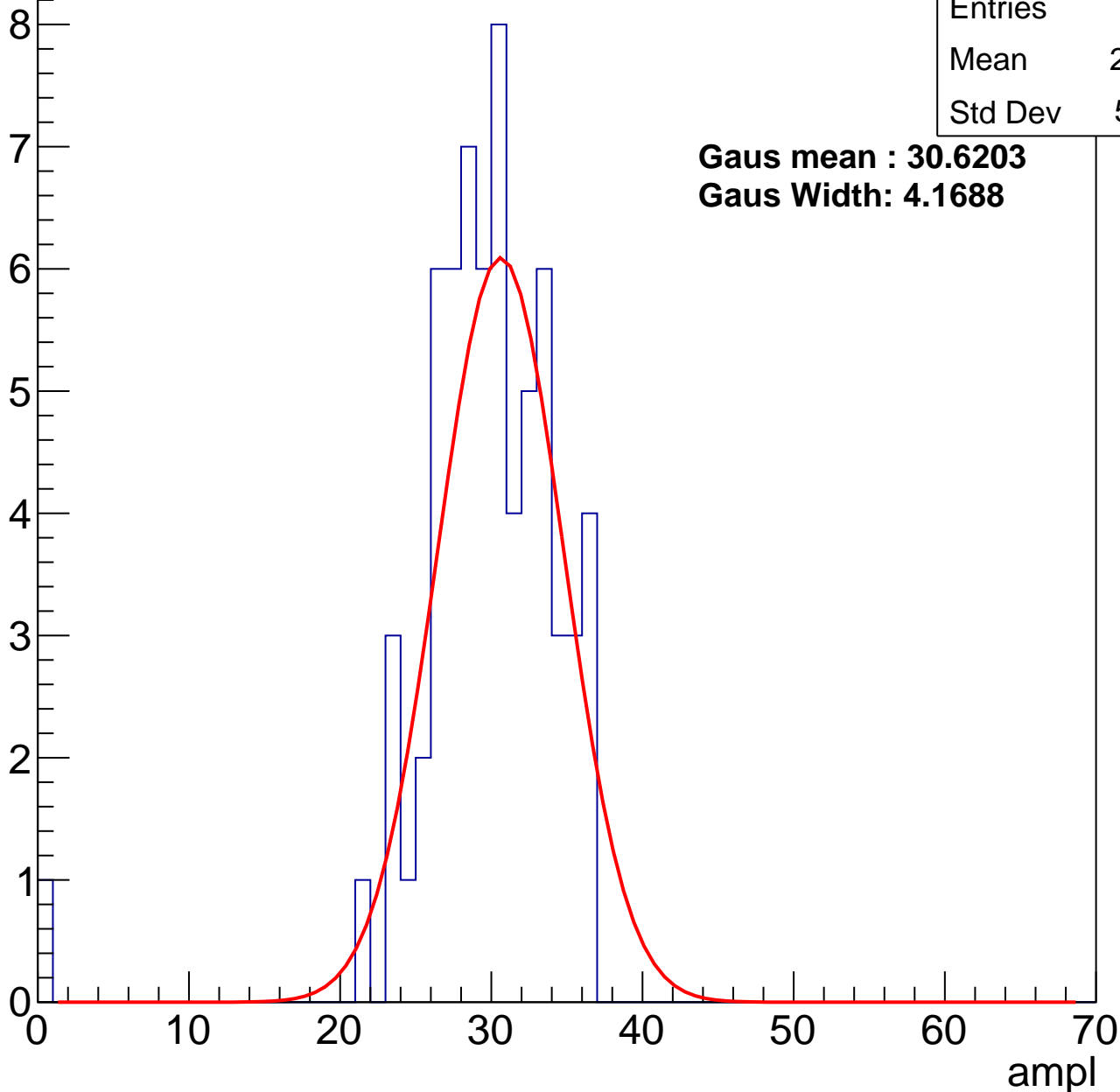
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	29.17
Std Dev	5.071

**Gaus mean : 30.6203**

**Gaus Width: 4.1688**



# B1L103S, U9-ch81, adc1

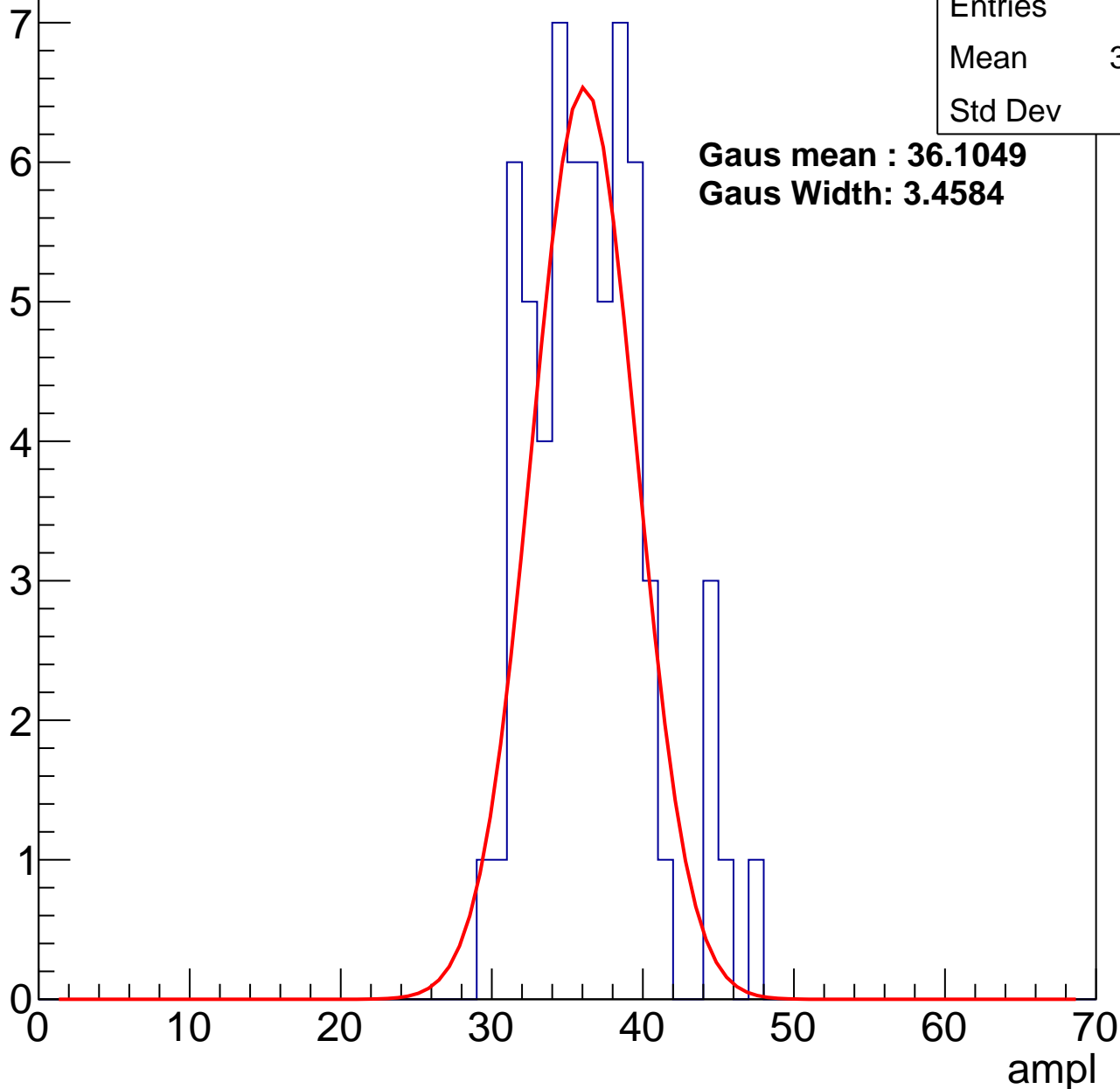
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	36.05
Std Dev	3.86

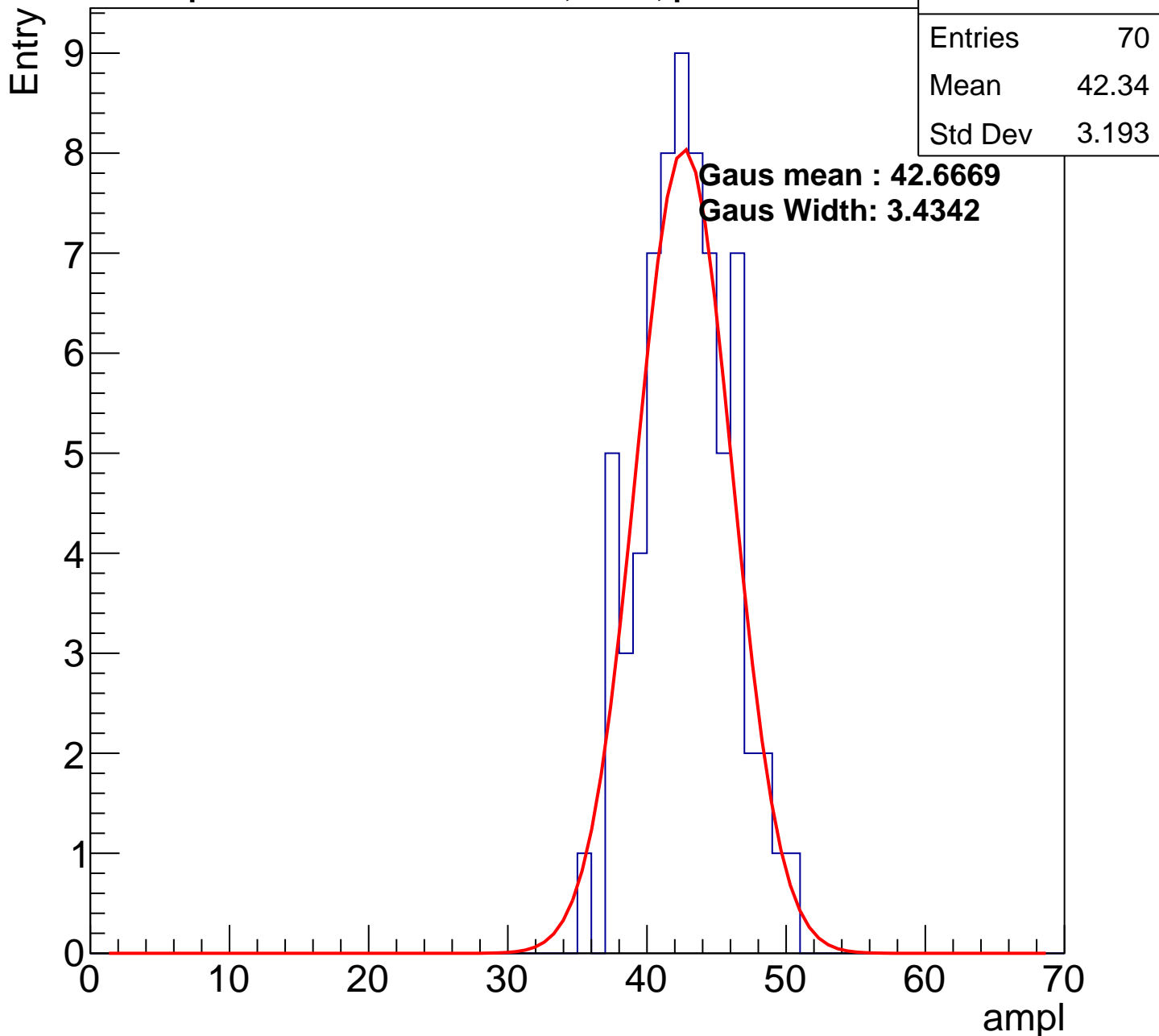
**Gaus mean : 36.1049**

**Gaus Width: 3.4584**



# B1L103S, U9-ch81, adc2

calib\_packv5\_042523\_0143.root, FC#7, port C2

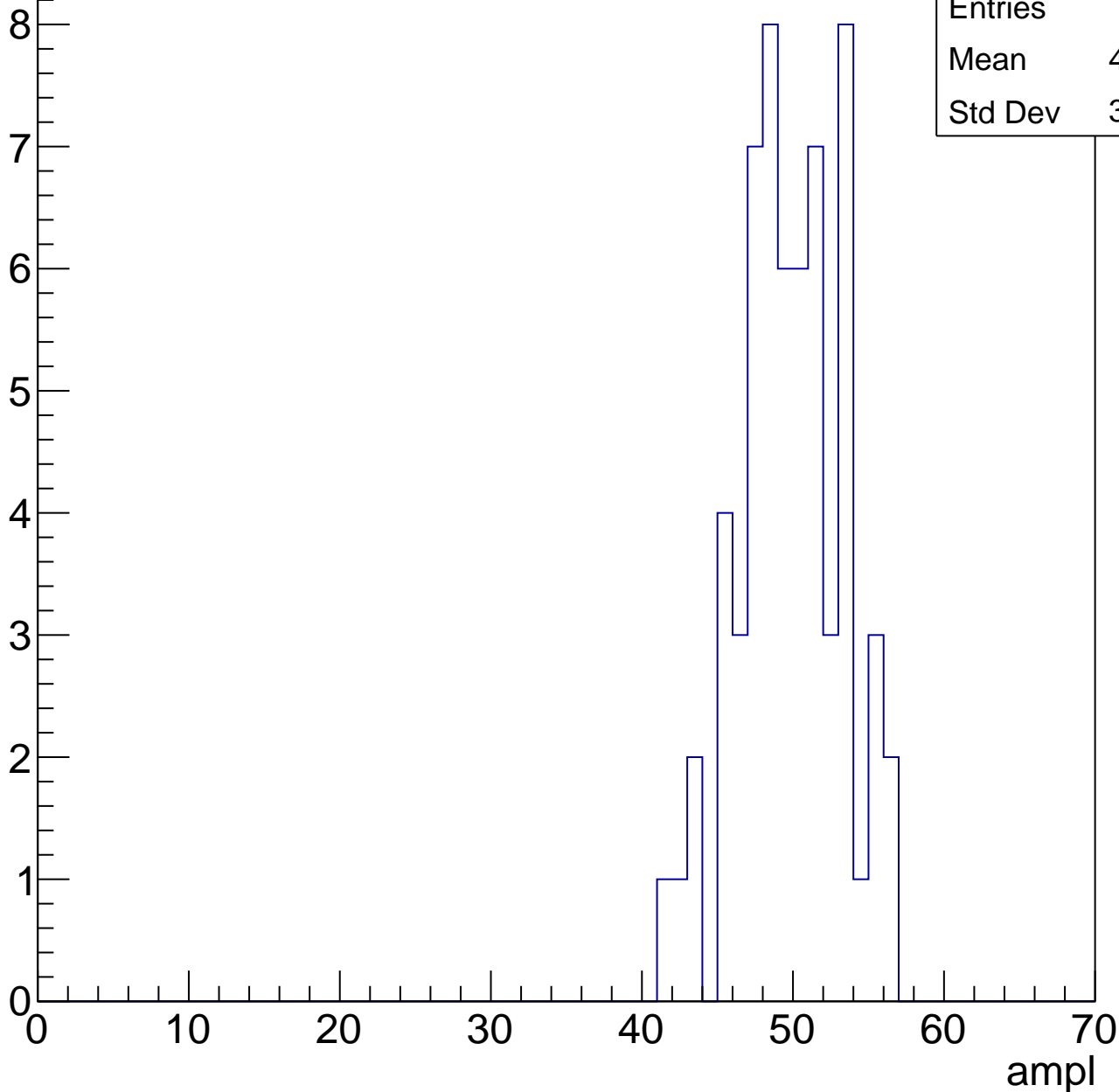


# B1L103S, U9-ch81, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	49.39
Std Dev	3.414

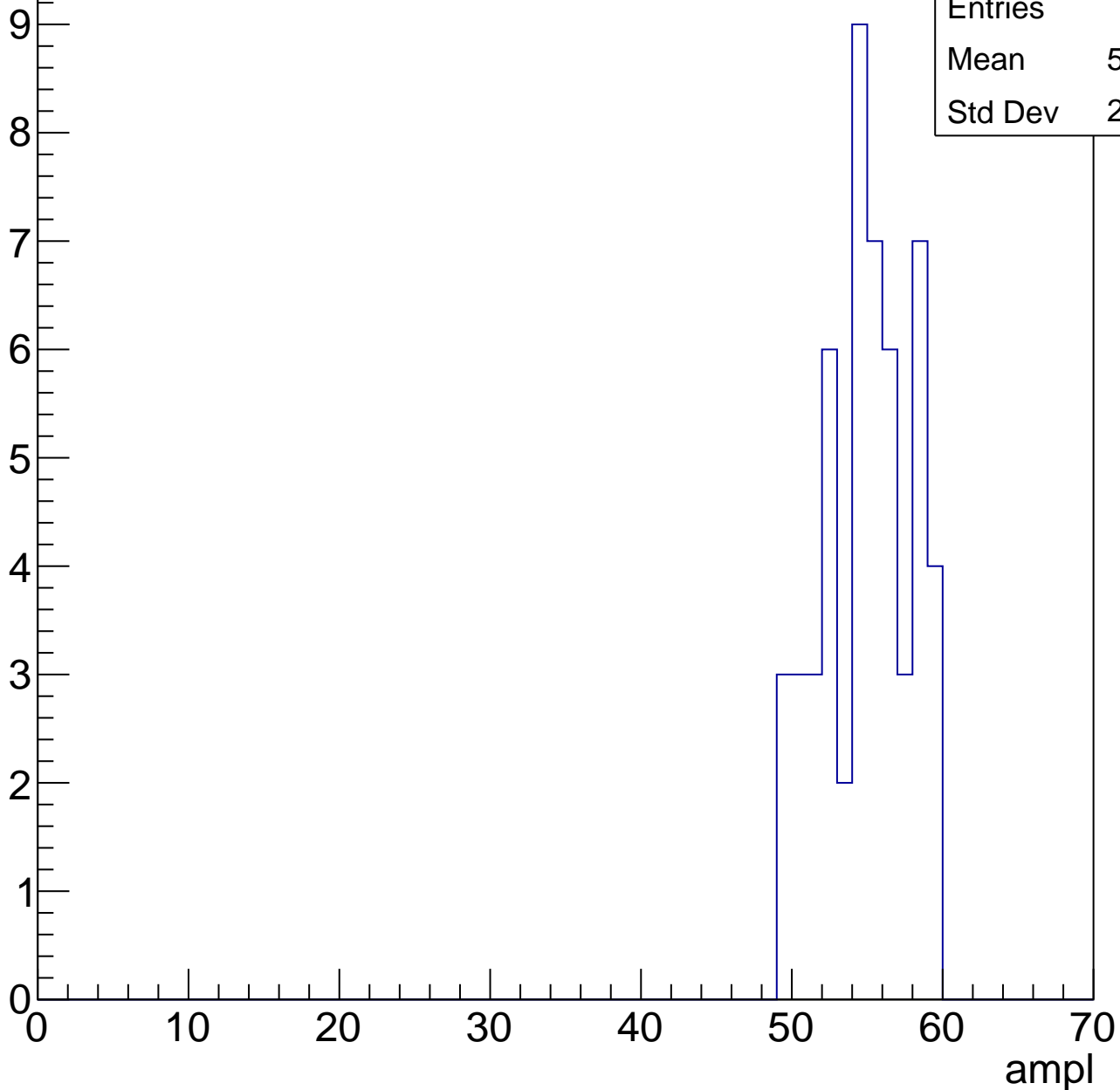


# B1L103S, U9-ch81, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	53
Mean	54.49
Std Dev	2.859

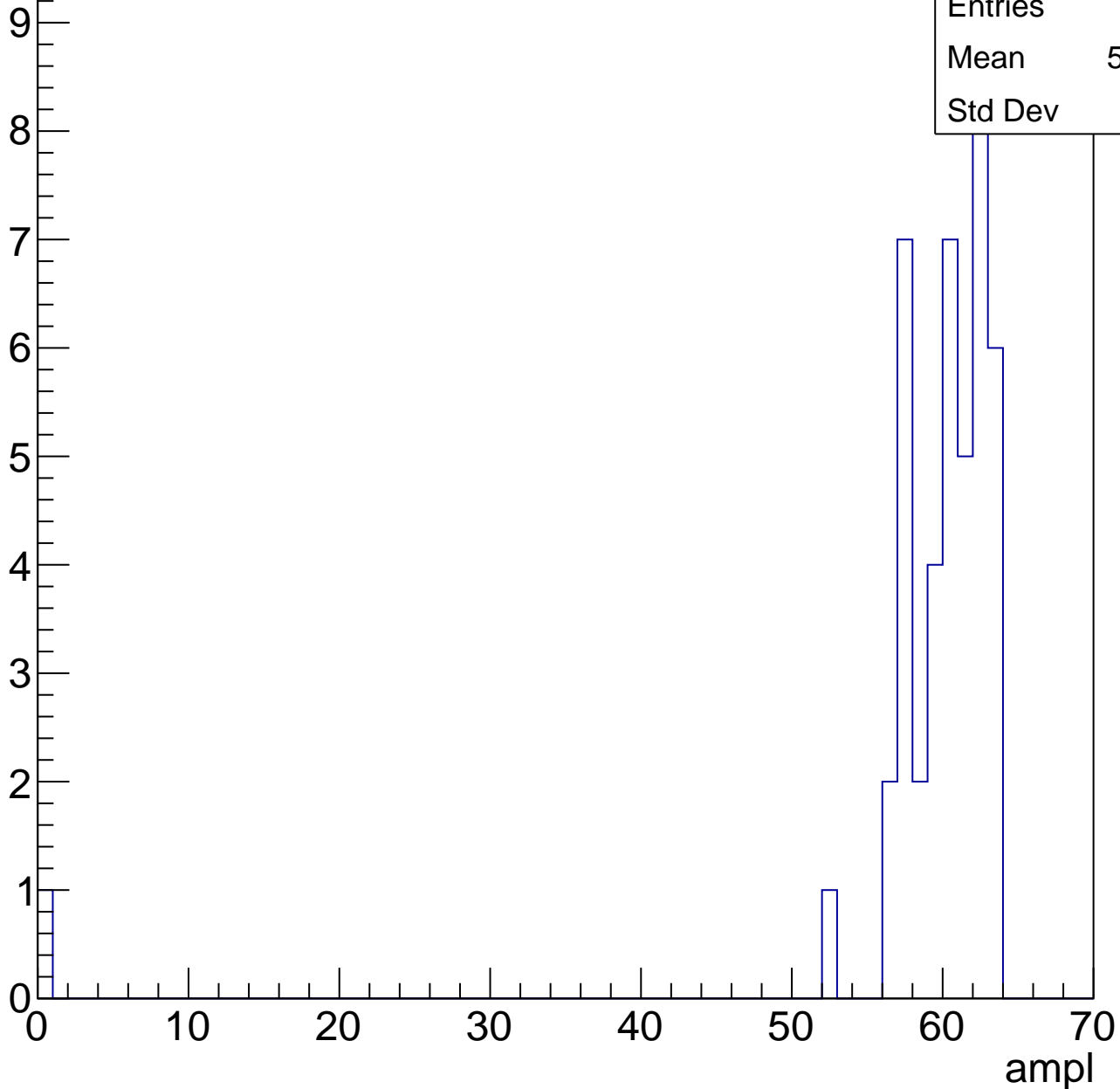


# B1L103S, U9-ch81, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	44
Mean	58.55
Std Dev	9.26

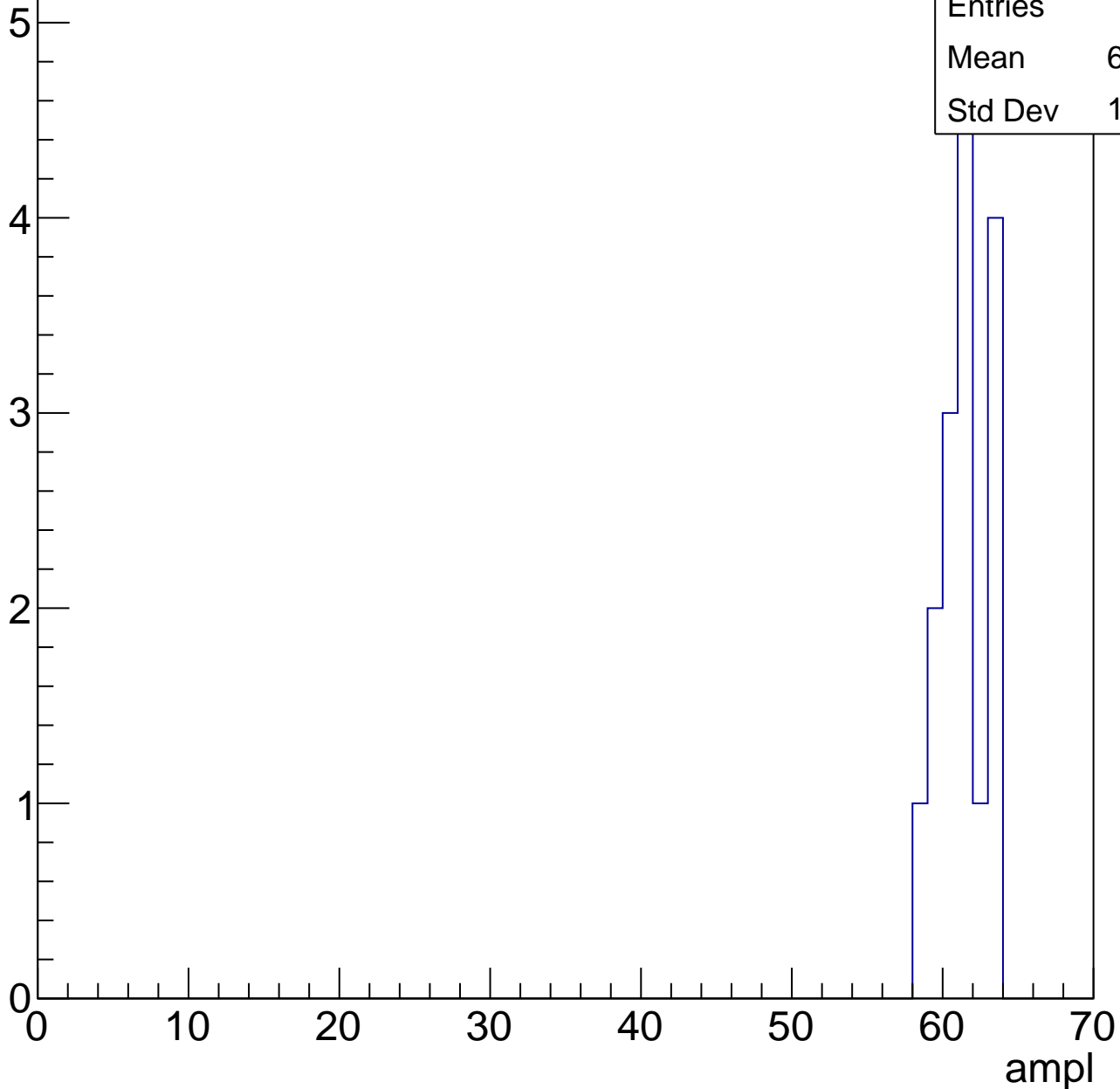


# B1L103S, U9-ch81, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	16
Mean	60.94
Std Dev	1.519





# B1L103S, U9-ch81, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U9-ch82, adc0

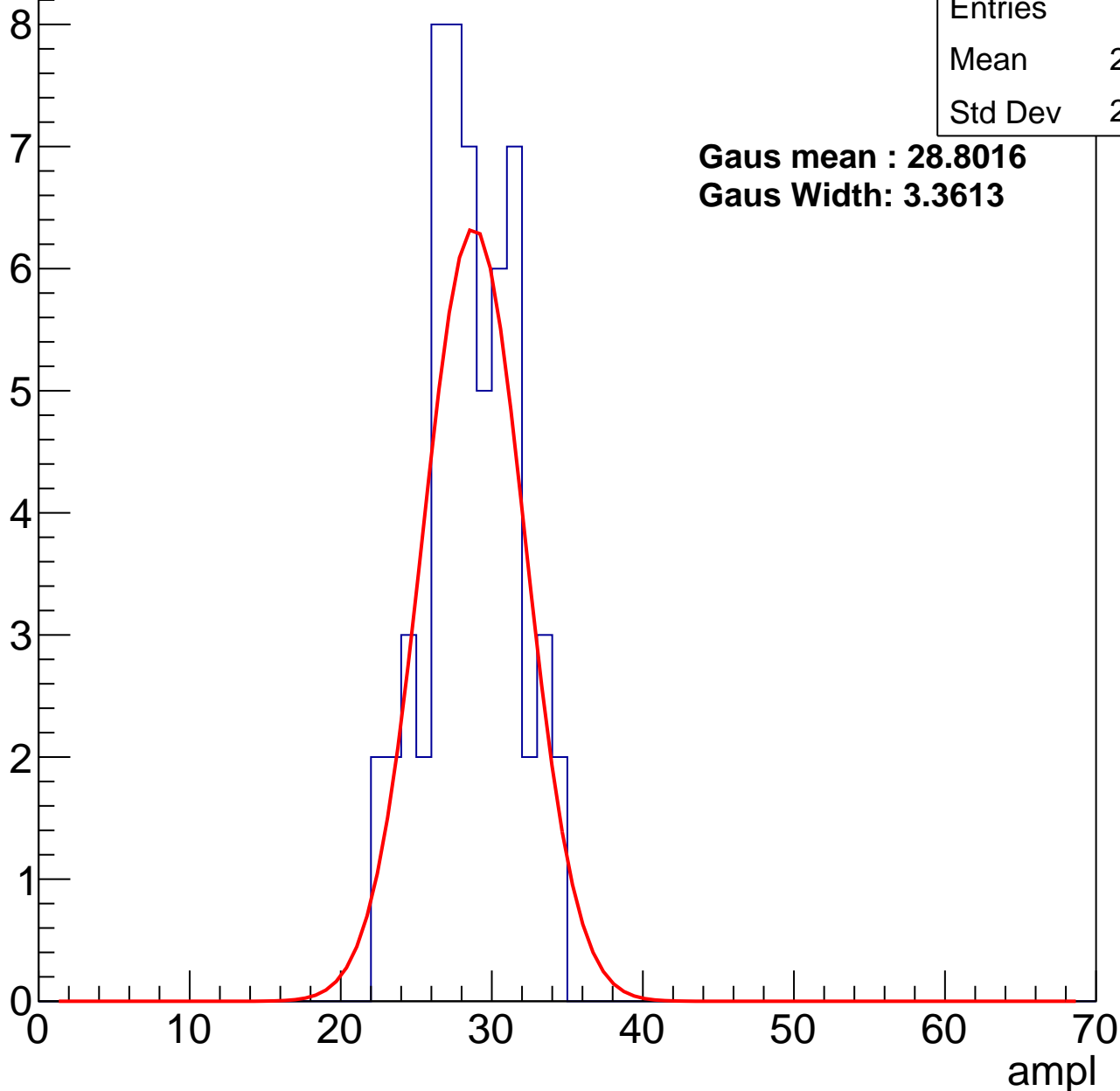
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	57
Mean	28.16
Std Dev	2.955

**Gaus mean : 28.8016**

**Gaus Width: 3.3613**



# B1L103S, U9-ch82, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	85
Mean	34.76
Std Dev	4.405

**Gaus mean : 35.2611**

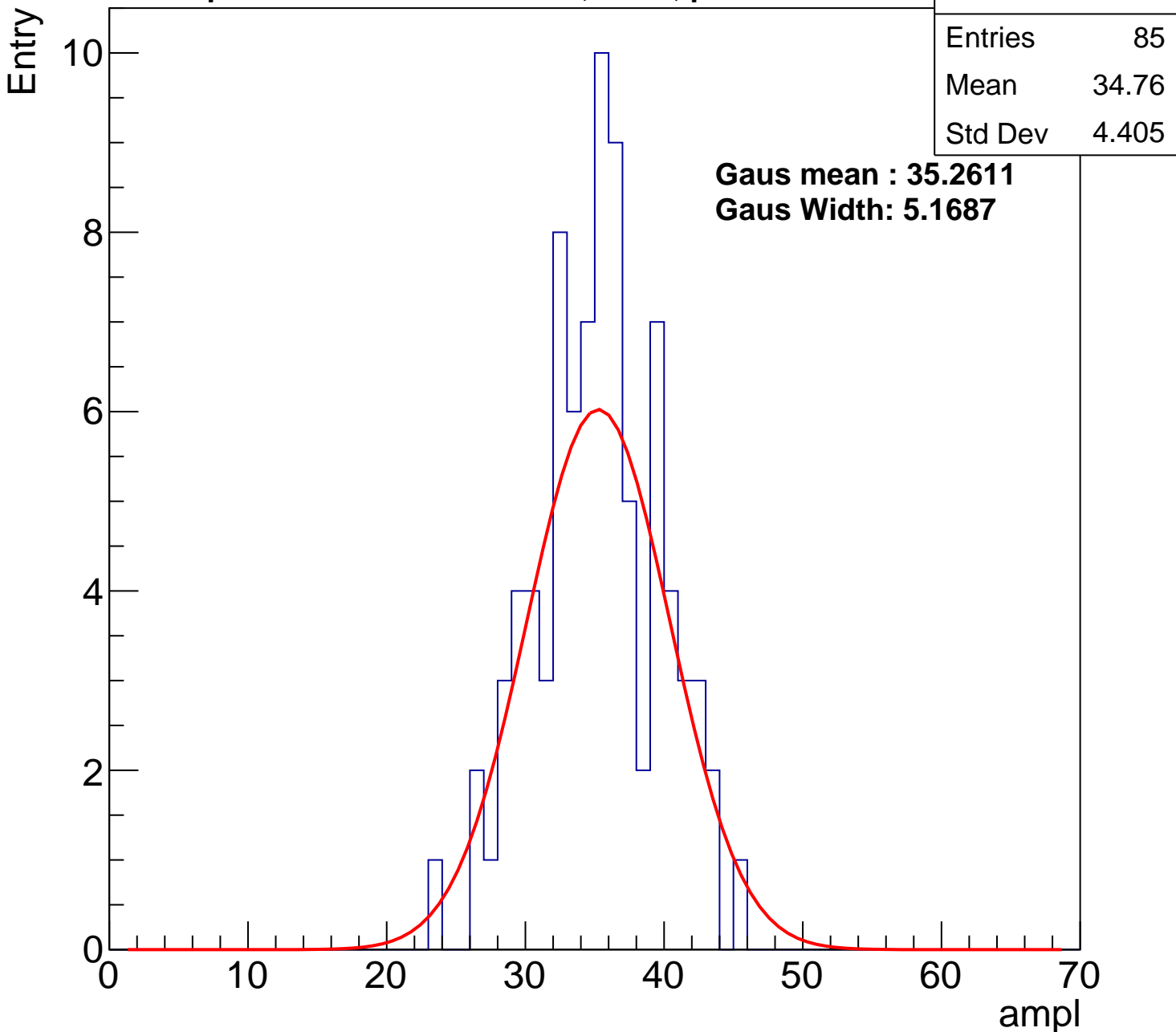
**Gaus Width: 5.1687**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U9-ch82, adc2

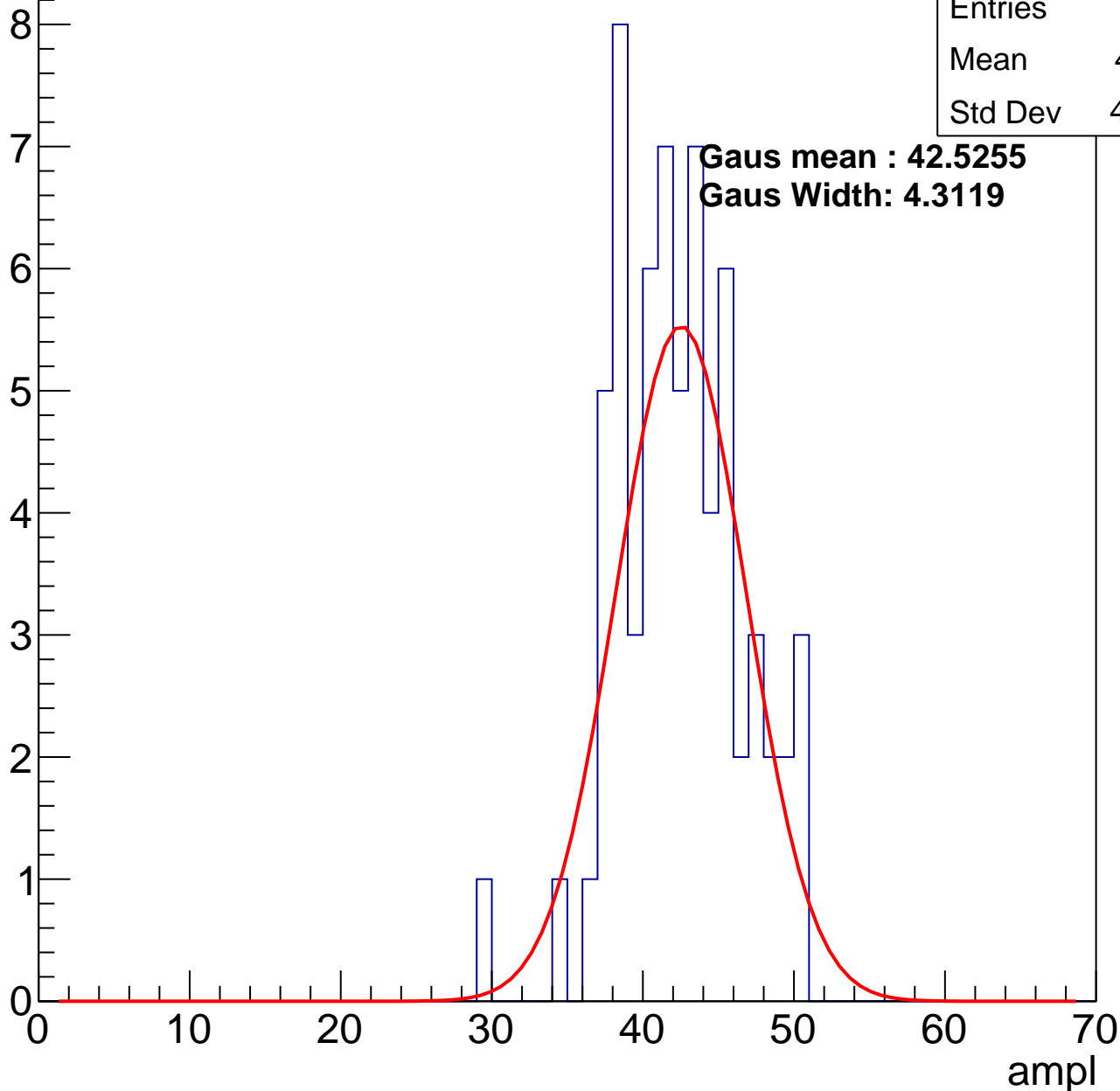
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	41.91
Std Dev	4.129

**Gaus mean : 42.5255**

**Gaus Width: 4.3119**



# B1L103S, U9-ch82, adc3

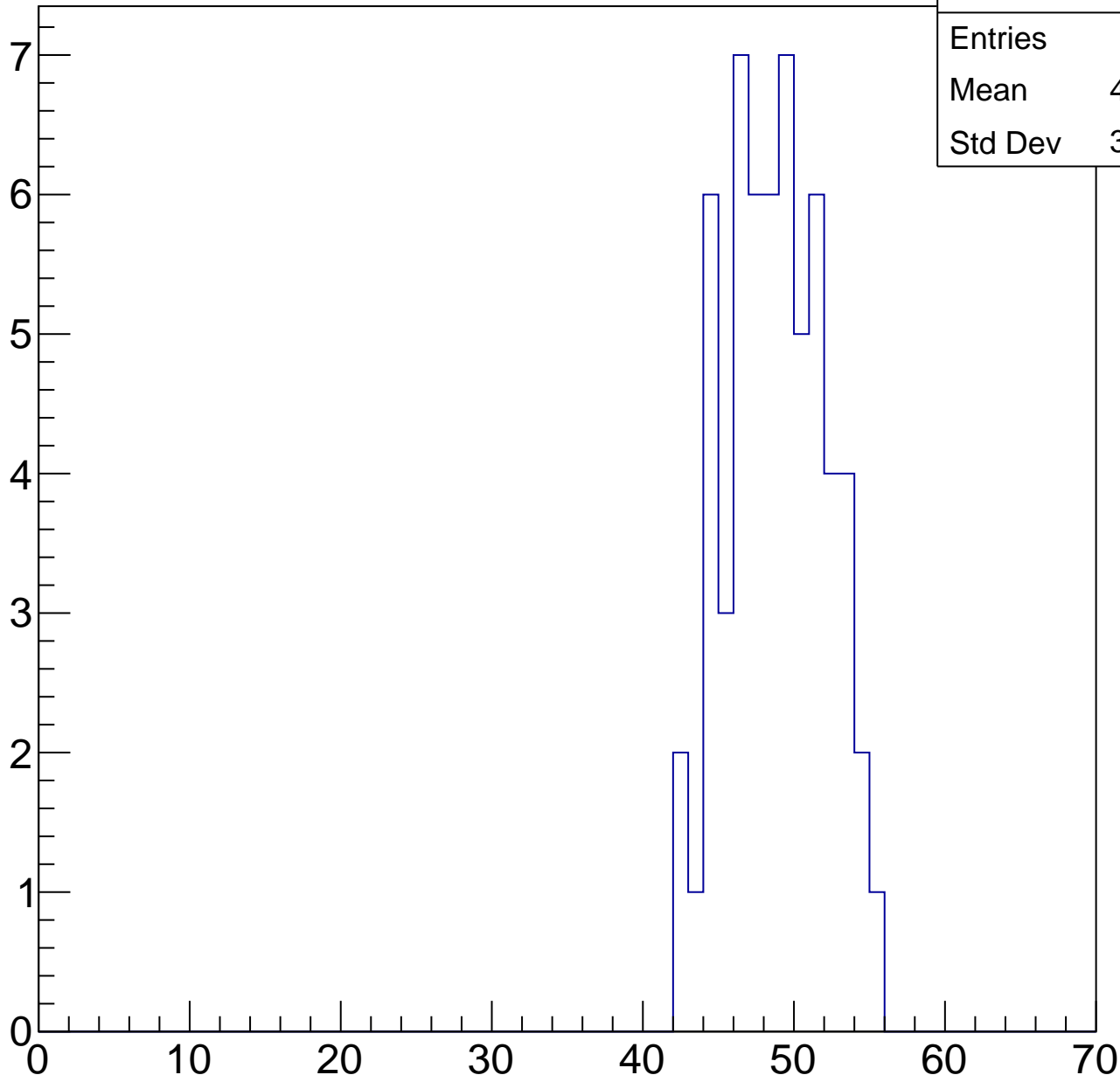
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

7  
6  
5  
4  
3  
2  
1  
0

Entries	60
Mean	48.33
Std Dev	3.197

ampl

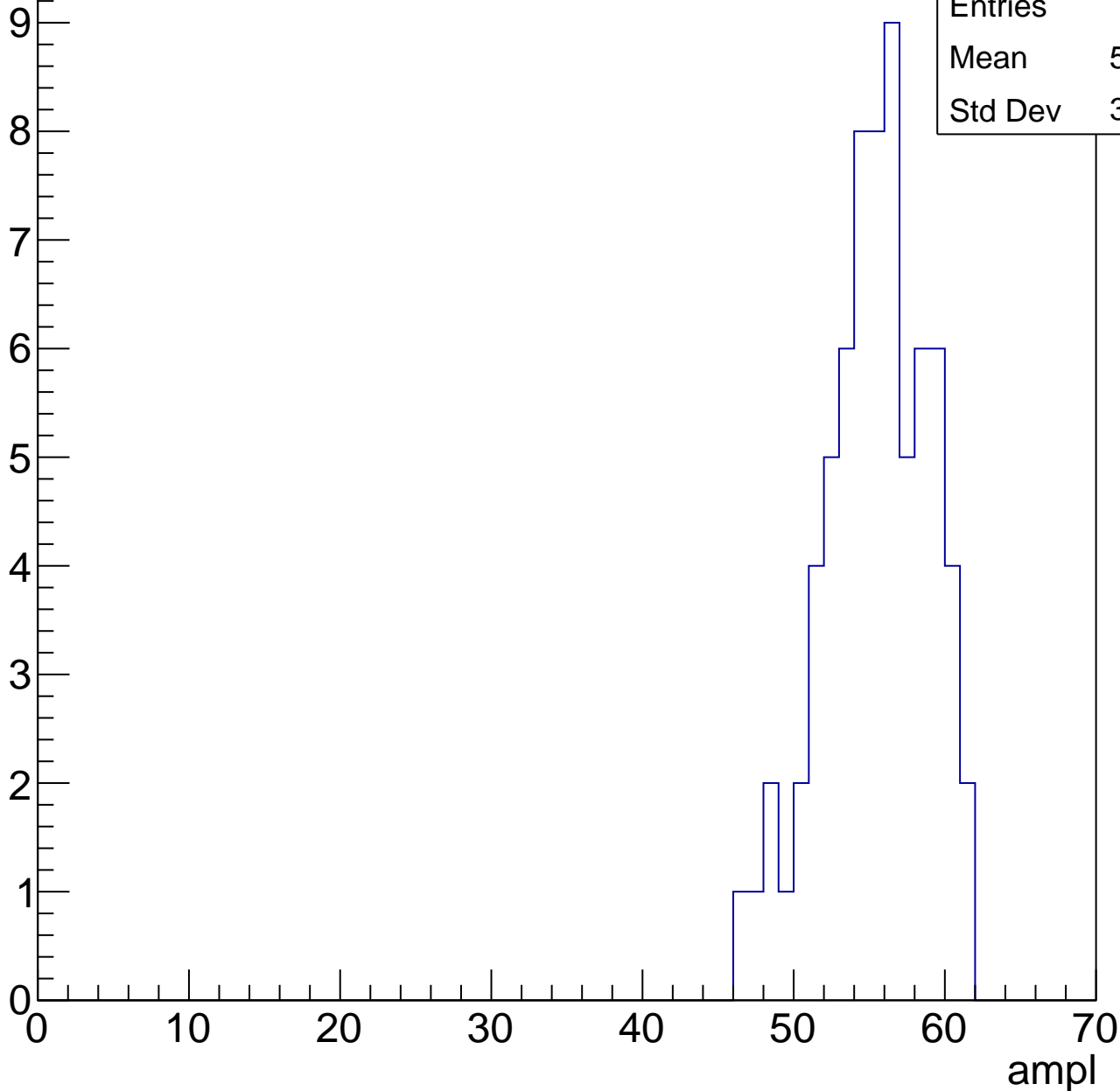


# B1L103S, U9-ch82, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	70
Mean	54.93
Std Dev	3.424

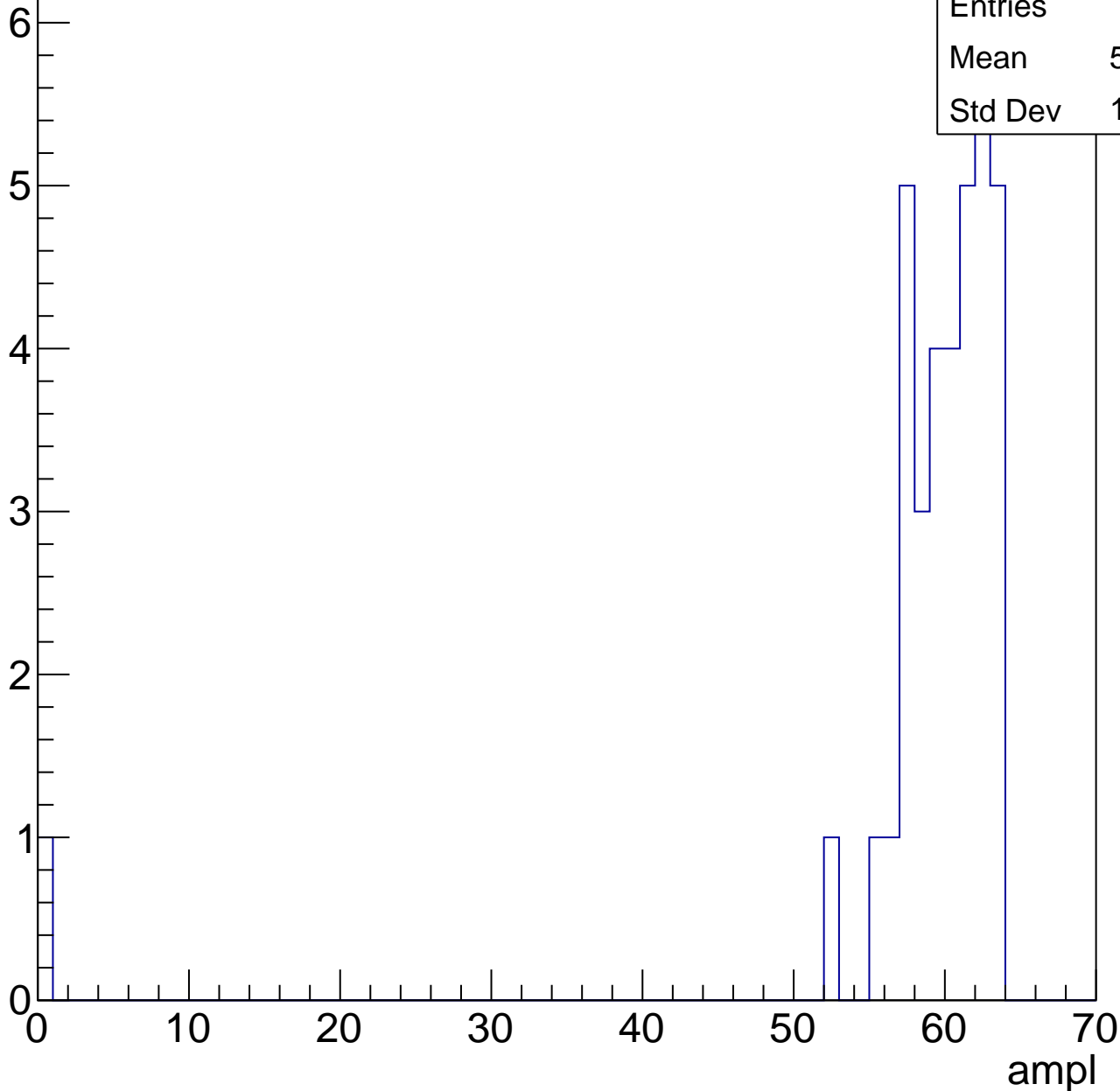


# B1L103S, U9-ch82, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

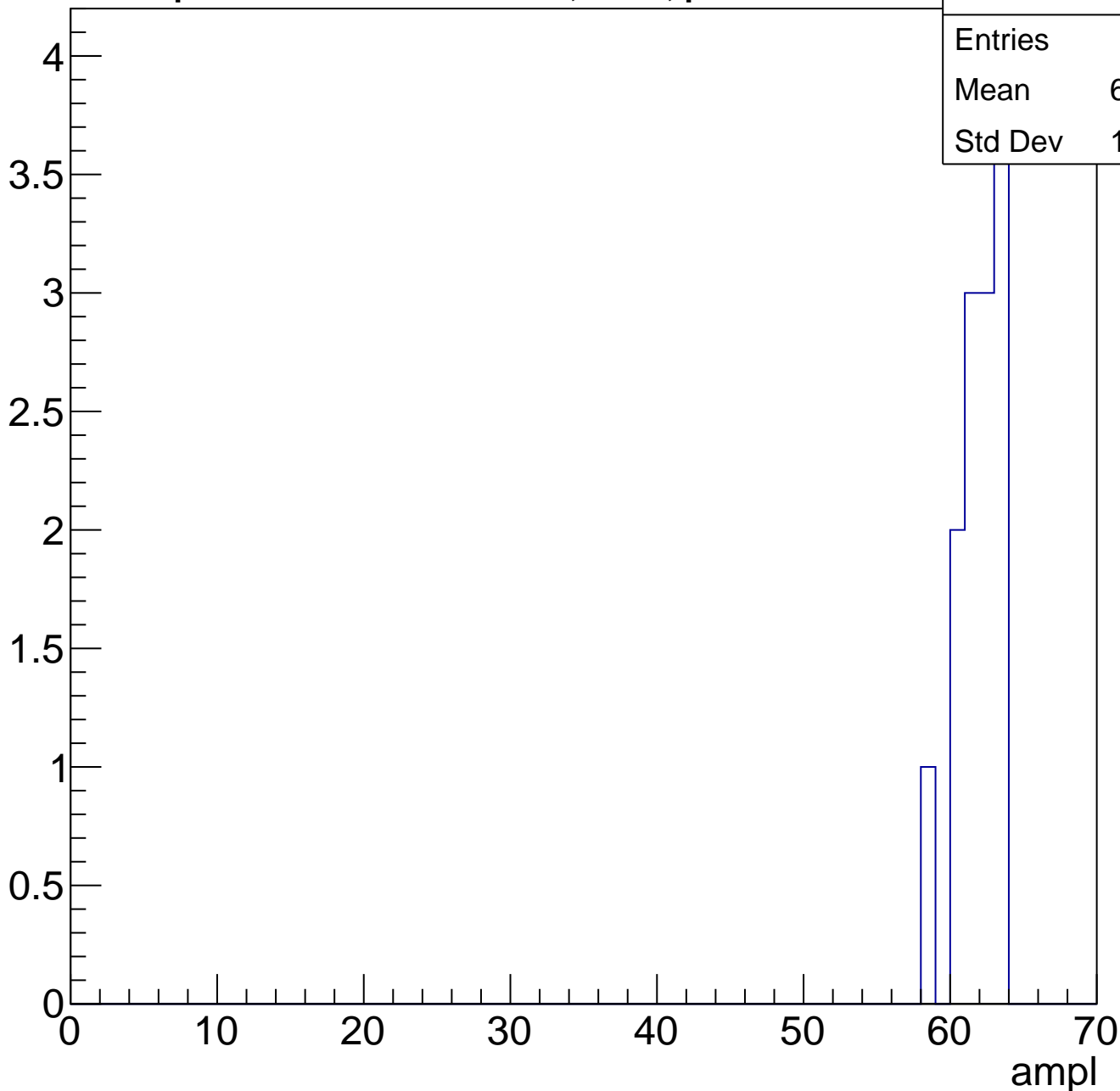
Entries	36
Mean	58.06
Std Dev	10.14



# B1L103S, U9-ch82, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U9-ch82, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U9-ch83, adc0

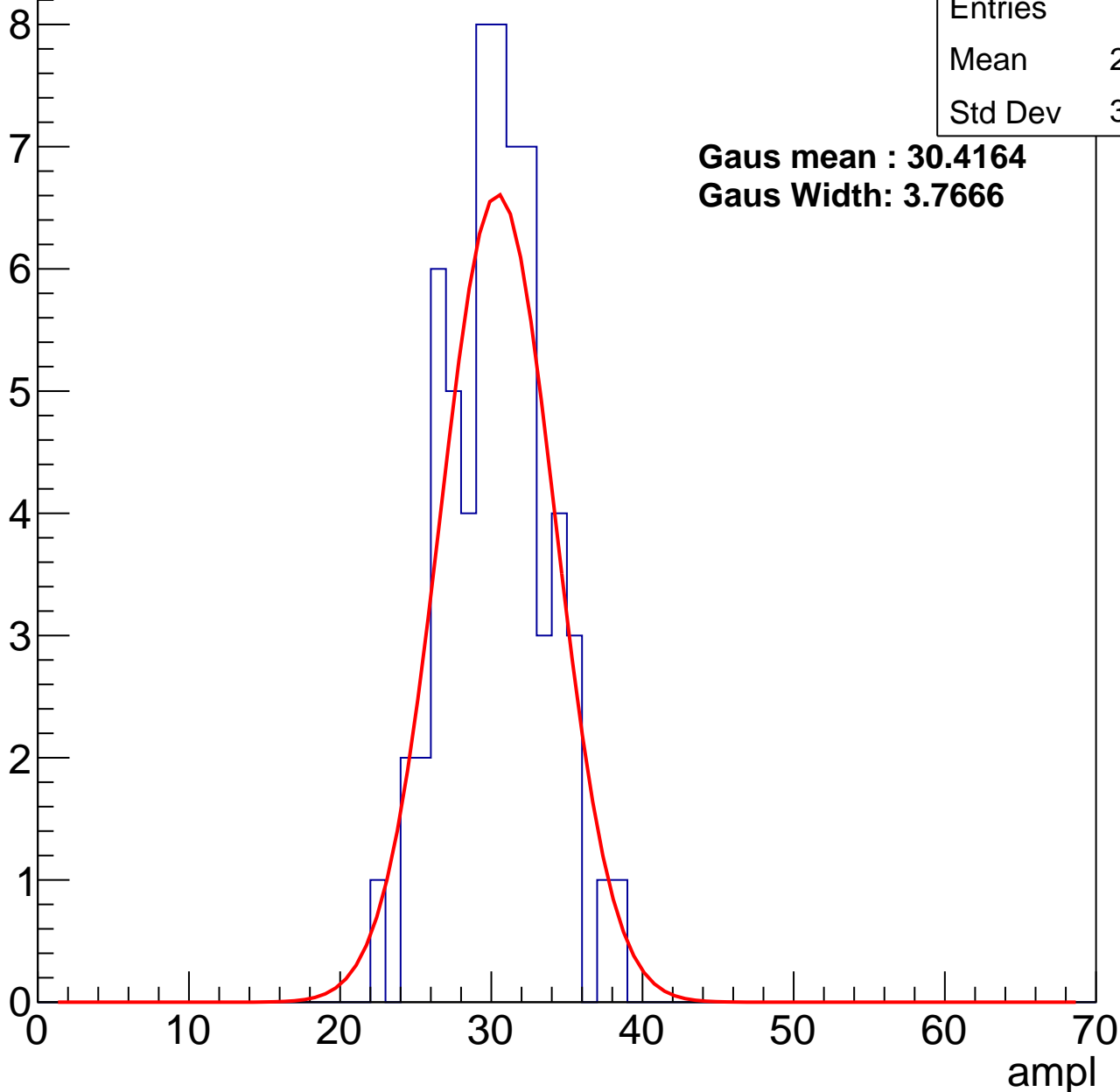
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	29.85
Std Dev	3.272

**Gaus mean : 30.4164**

**Gaus Width: 3.7666**



# B1L103S, U9-ch83, adc1

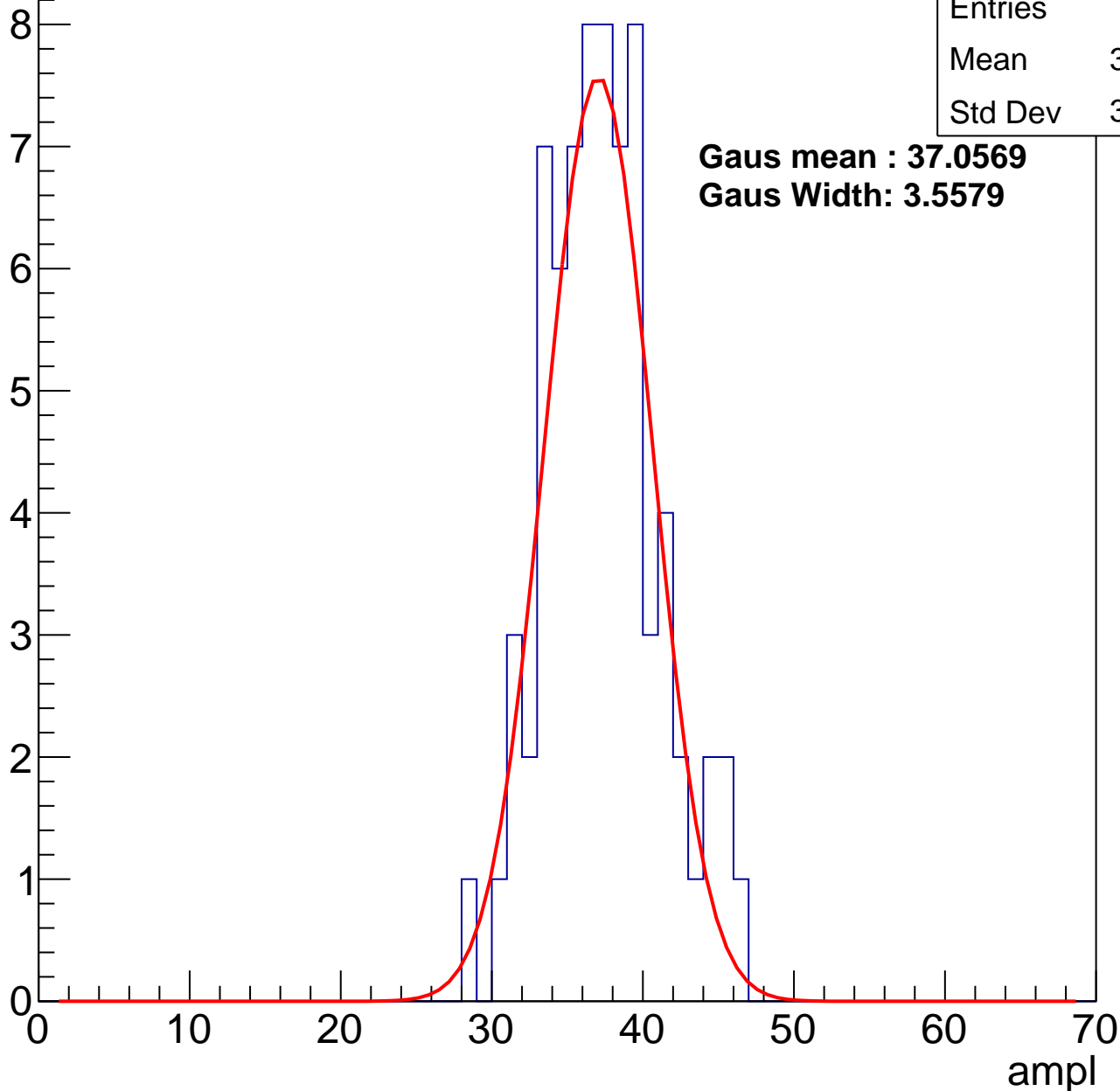
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	73
Mean	36.88
Std Dev	3.723

**Gaus mean : 37.0569**

**Gaus Width: 3.5579**

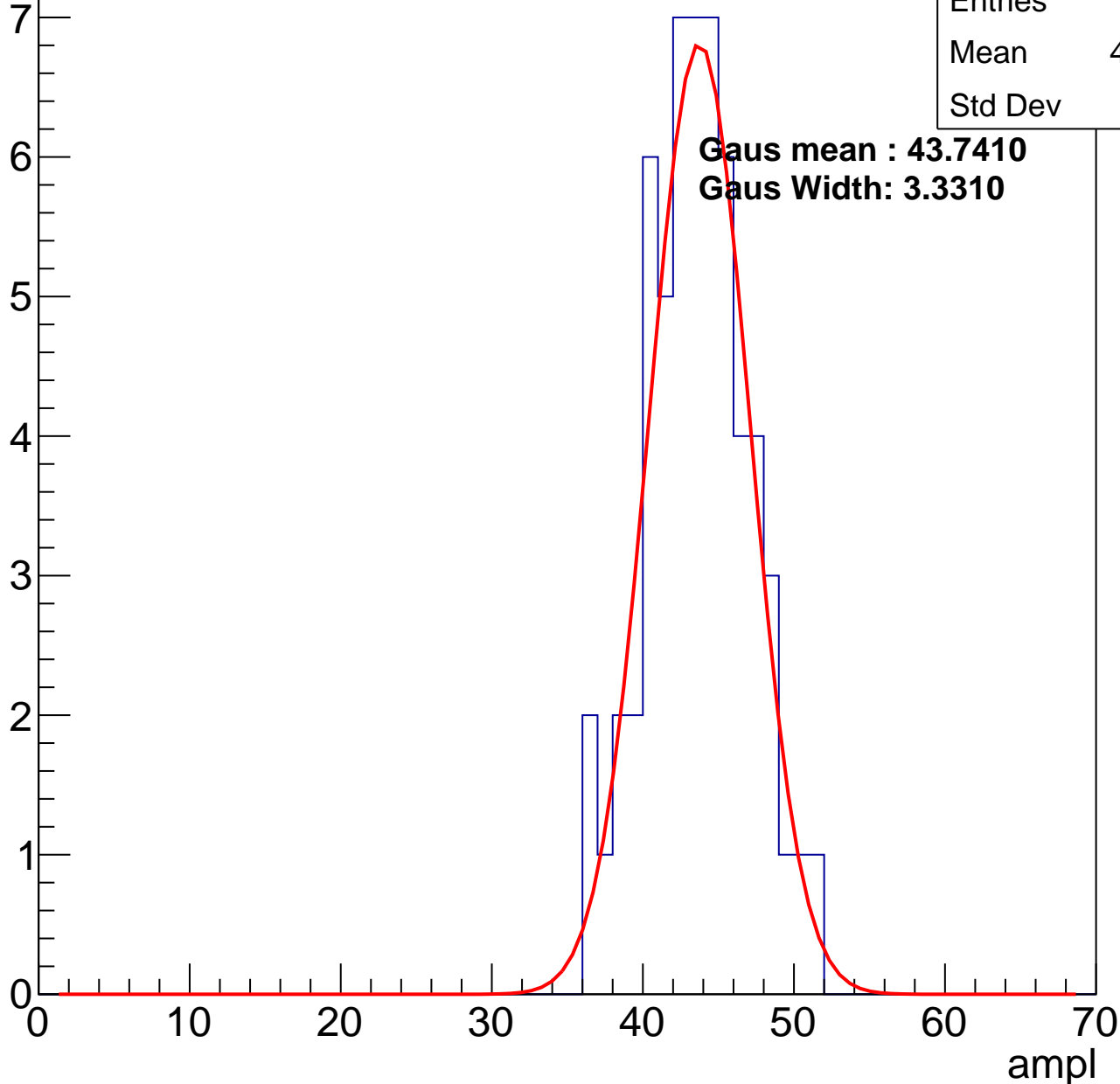


# B1L103S, U9-ch83, adc2

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	59
Mean	43.17
Std Dev	3.32

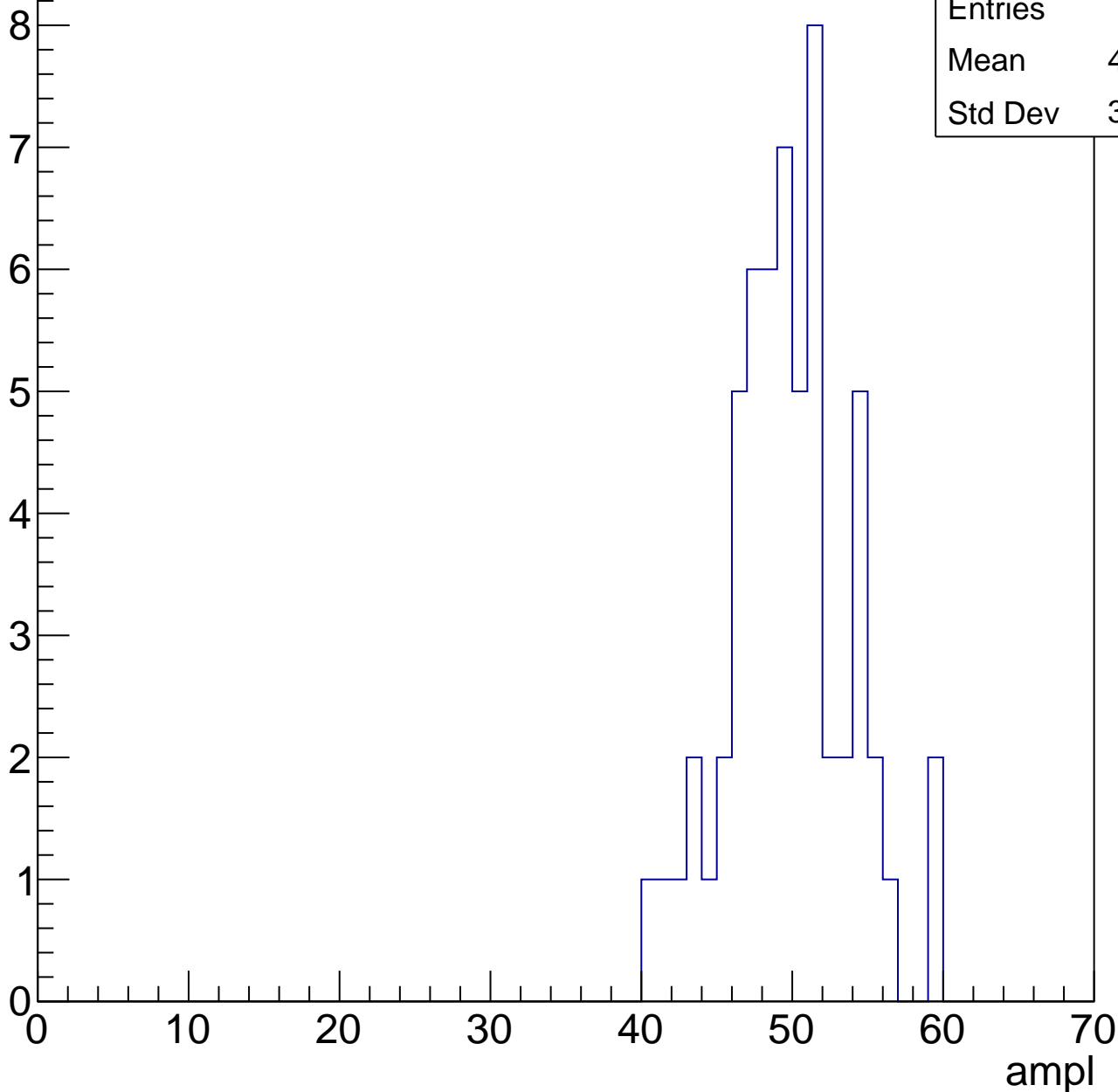


# B1L103S, U9-ch83, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

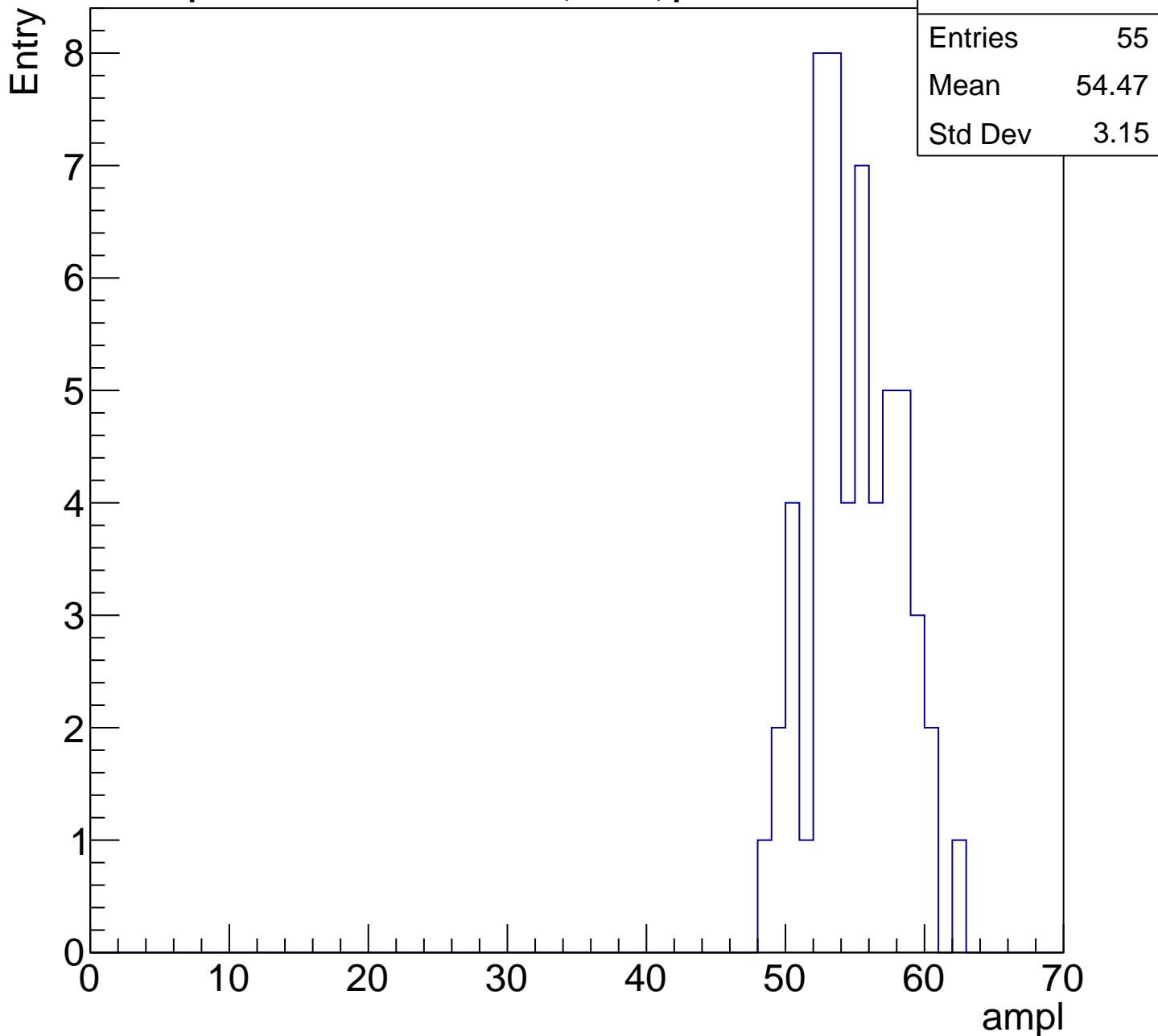
Entry

Entries	59
Mean	49.29
Std Dev	3.962



# B1L103S, U9-ch83, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

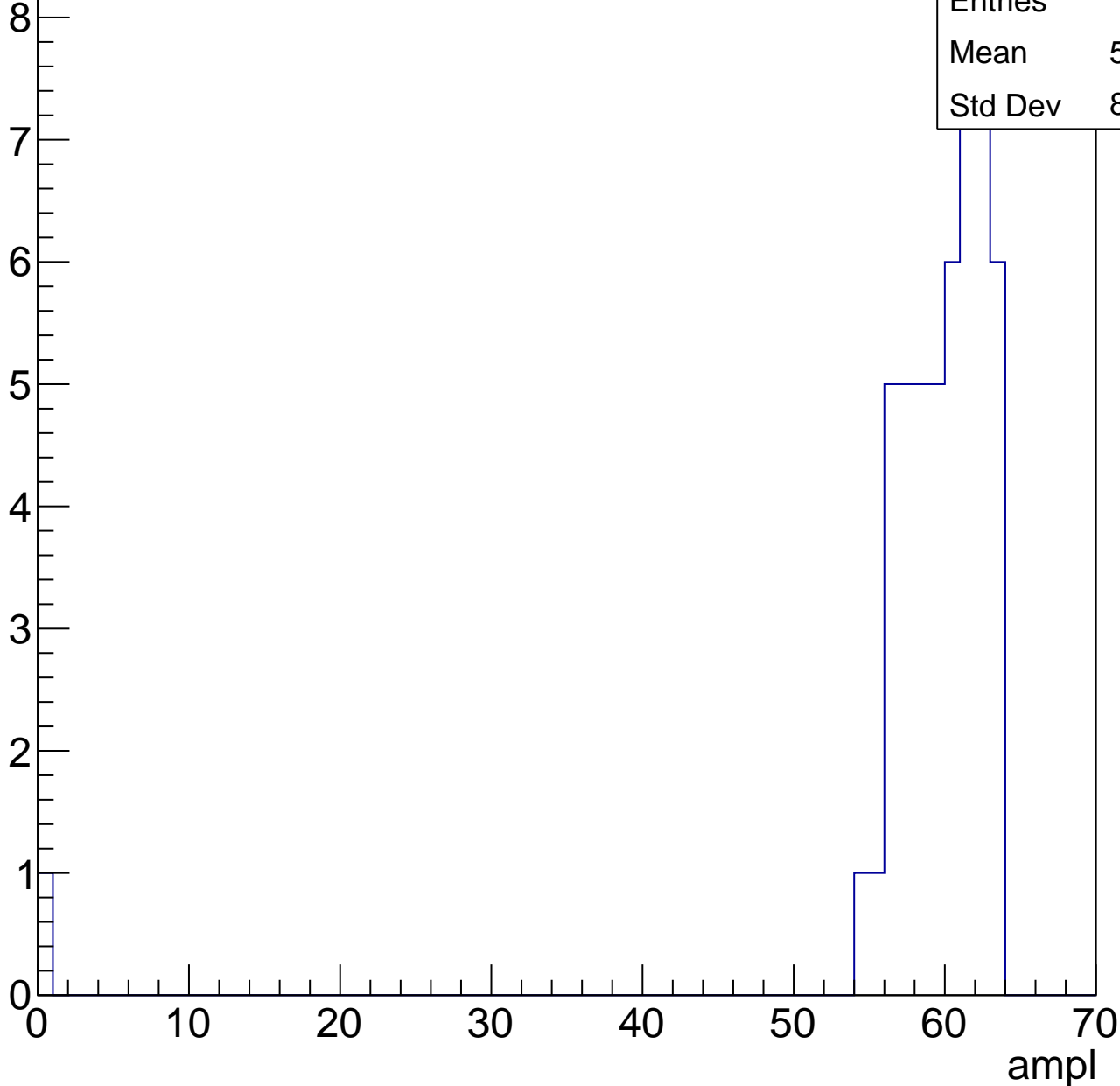


# B1L103S, U9-ch83, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

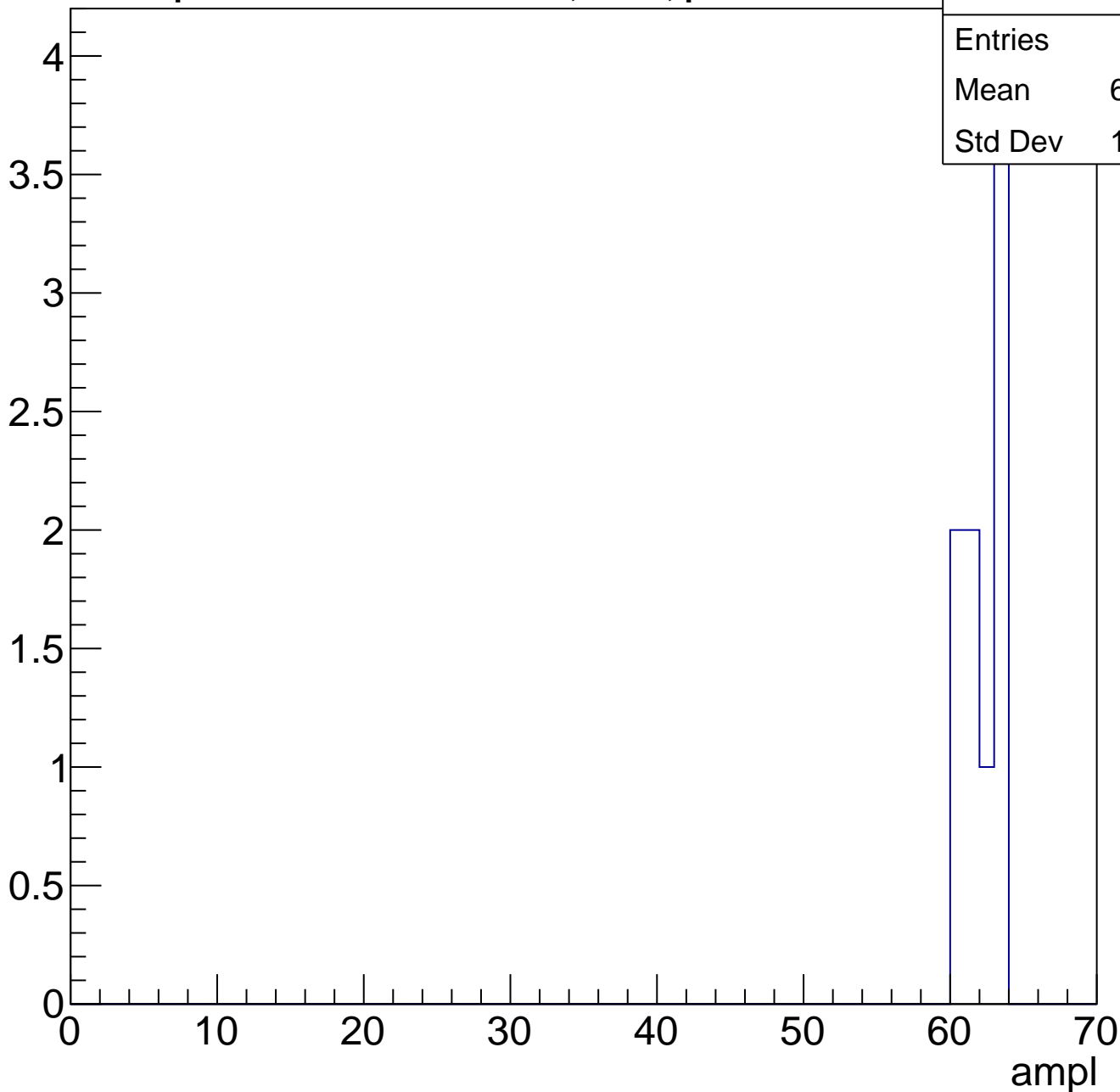
Entries	51
Mean	58.45
Std Dev	8.612



# B1L103S, U9-ch83, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U9-ch83, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U9-ch84, adc0

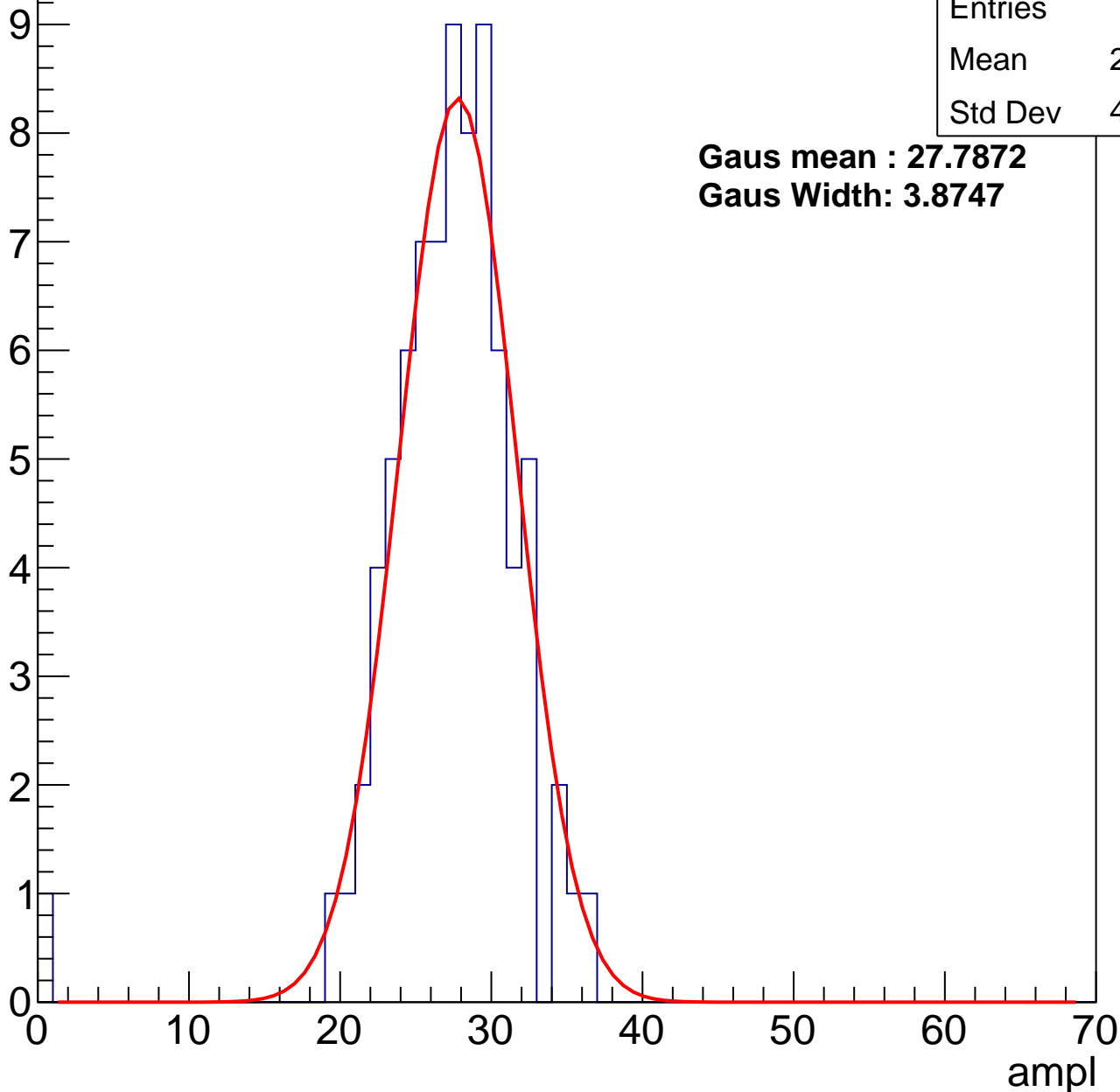
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	79
Mean	26.78
Std Dev	4.652

**Gaus mean : 27.7872**

**Gaus Width: 3.8747**



# B1L103S, U9-ch84, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	75
Mean	35
Std Dev	3.2

**Gaus mean : 35.0444**

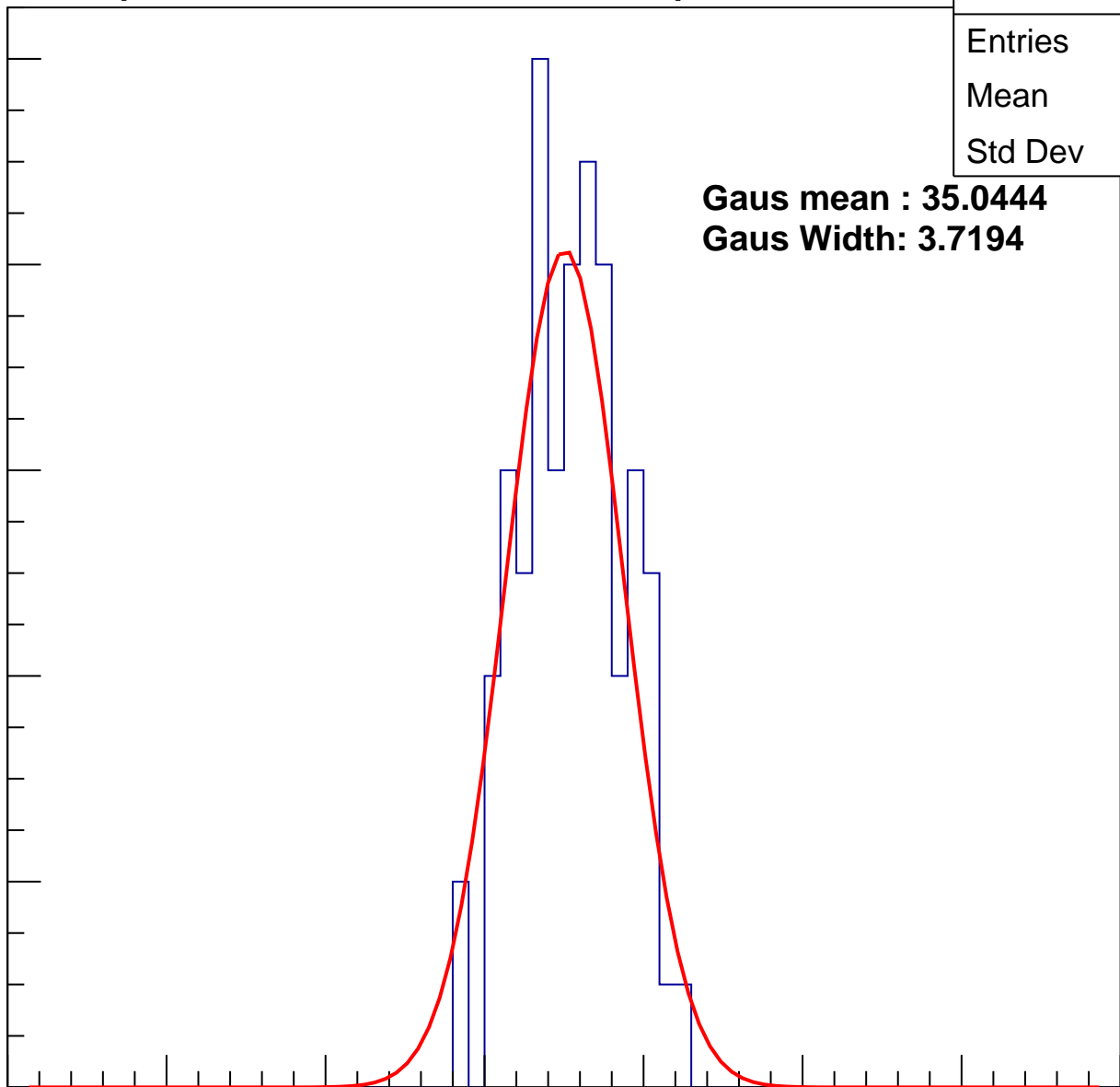
**Gaus Width: 3.7194**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U9-ch84, adc2

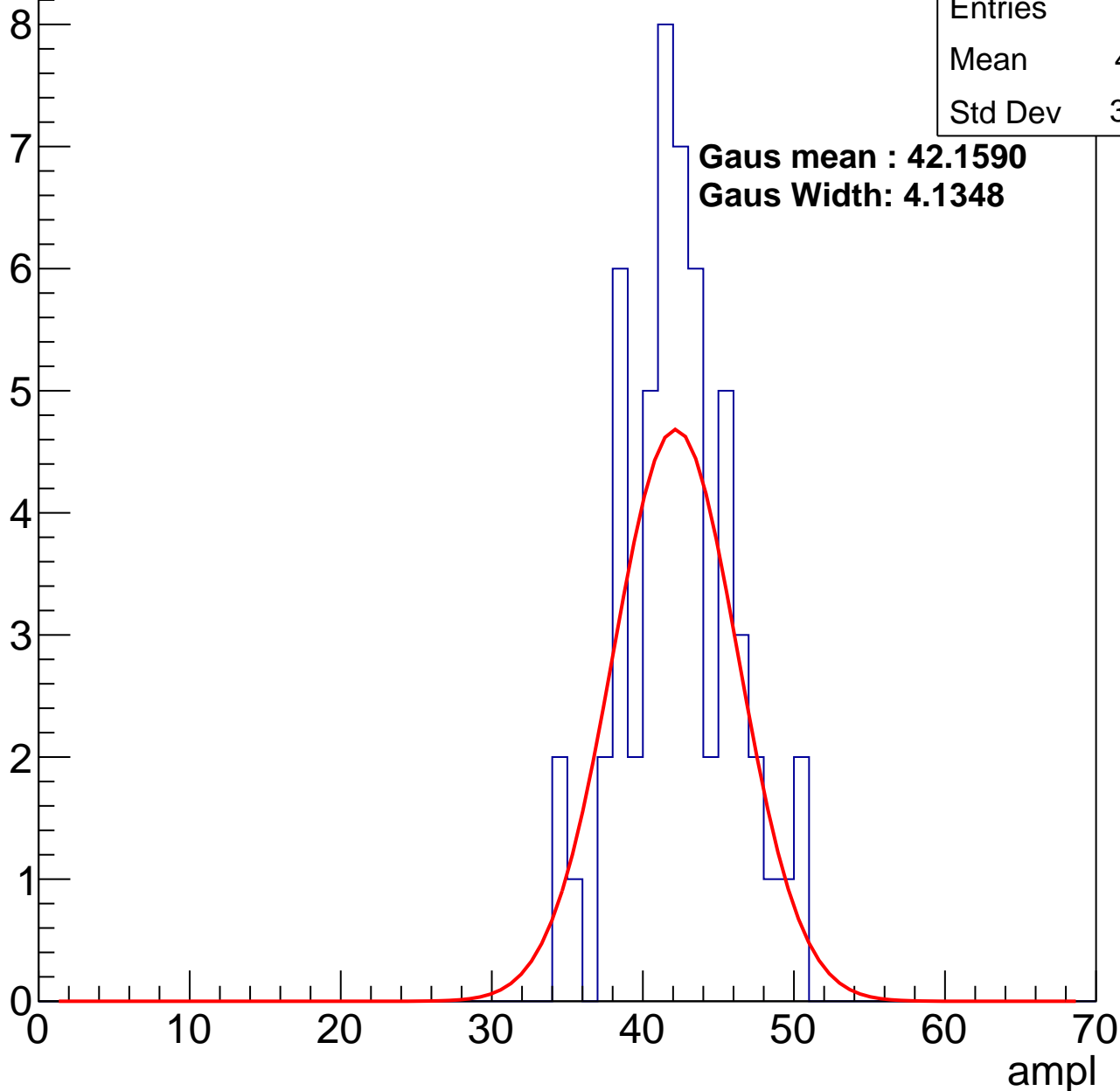
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	55
Mean	41.91
Std Dev	3.664

**Gaus mean : 42.1590**

**Gaus Width: 4.1348**

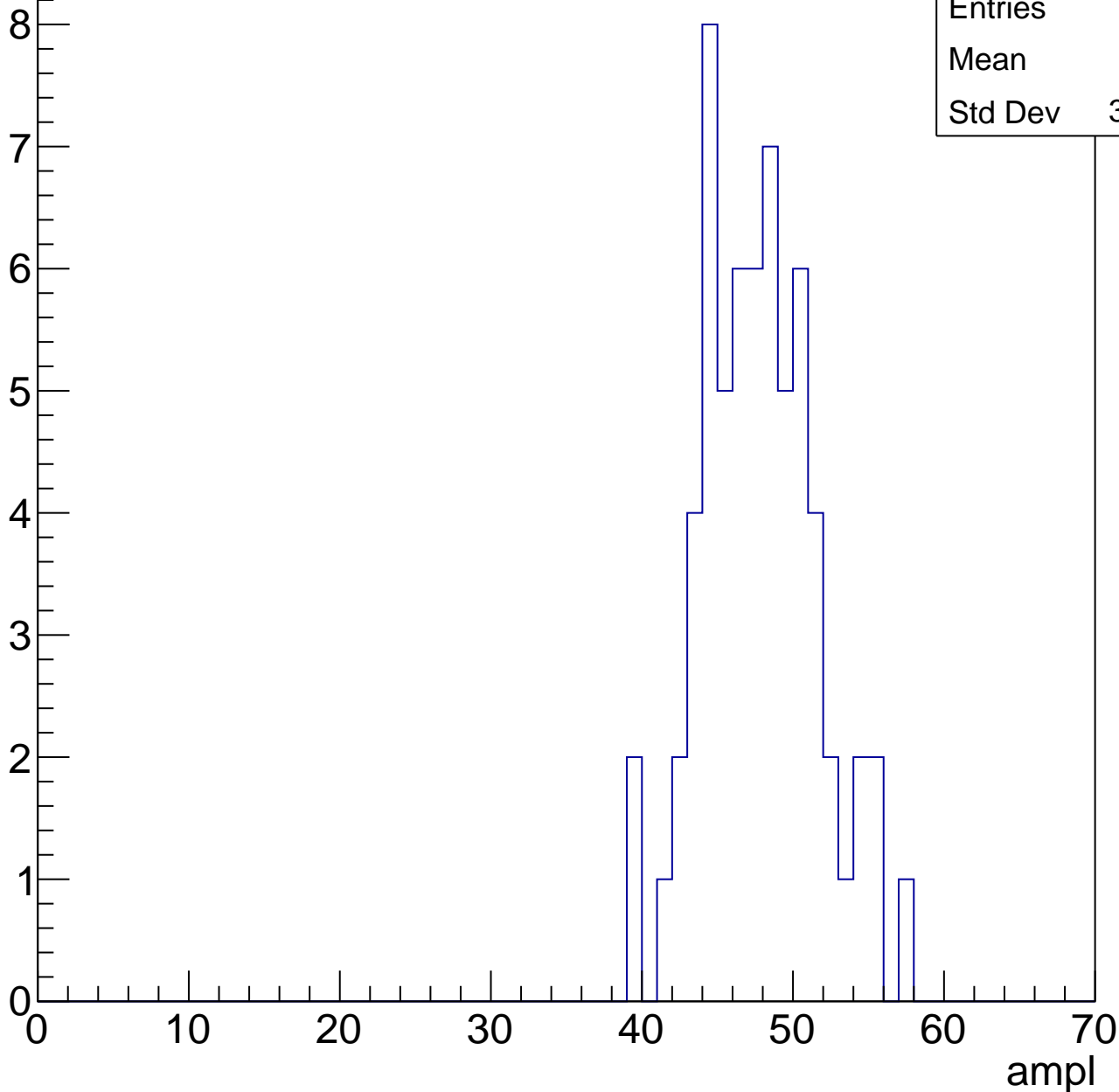


# B1L103S, U9-ch84, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

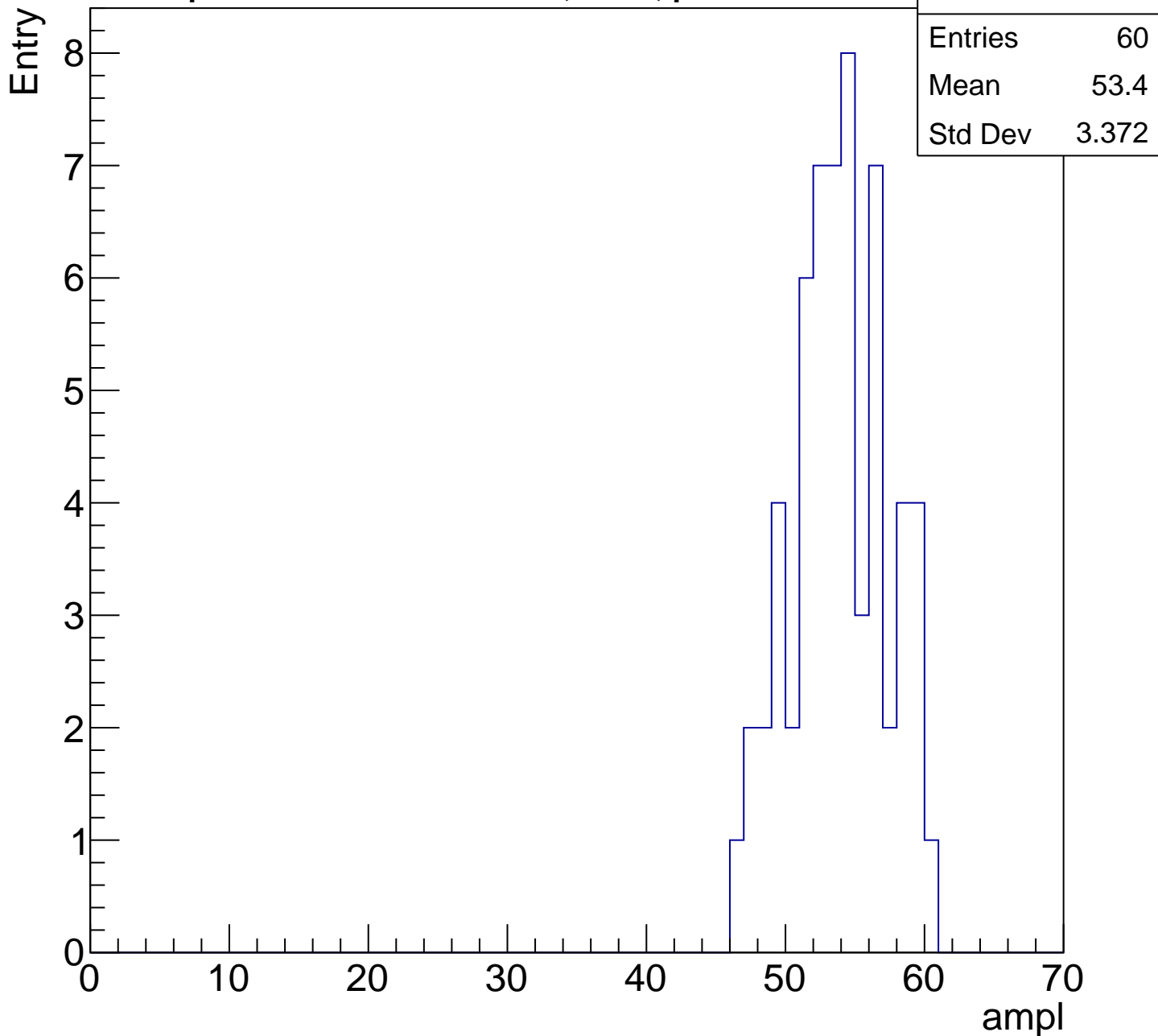
Entry

Entries	64
Mean	47.3
Std Dev	3.807



# B1L103S, U9-ch84, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U9-ch84, adc5

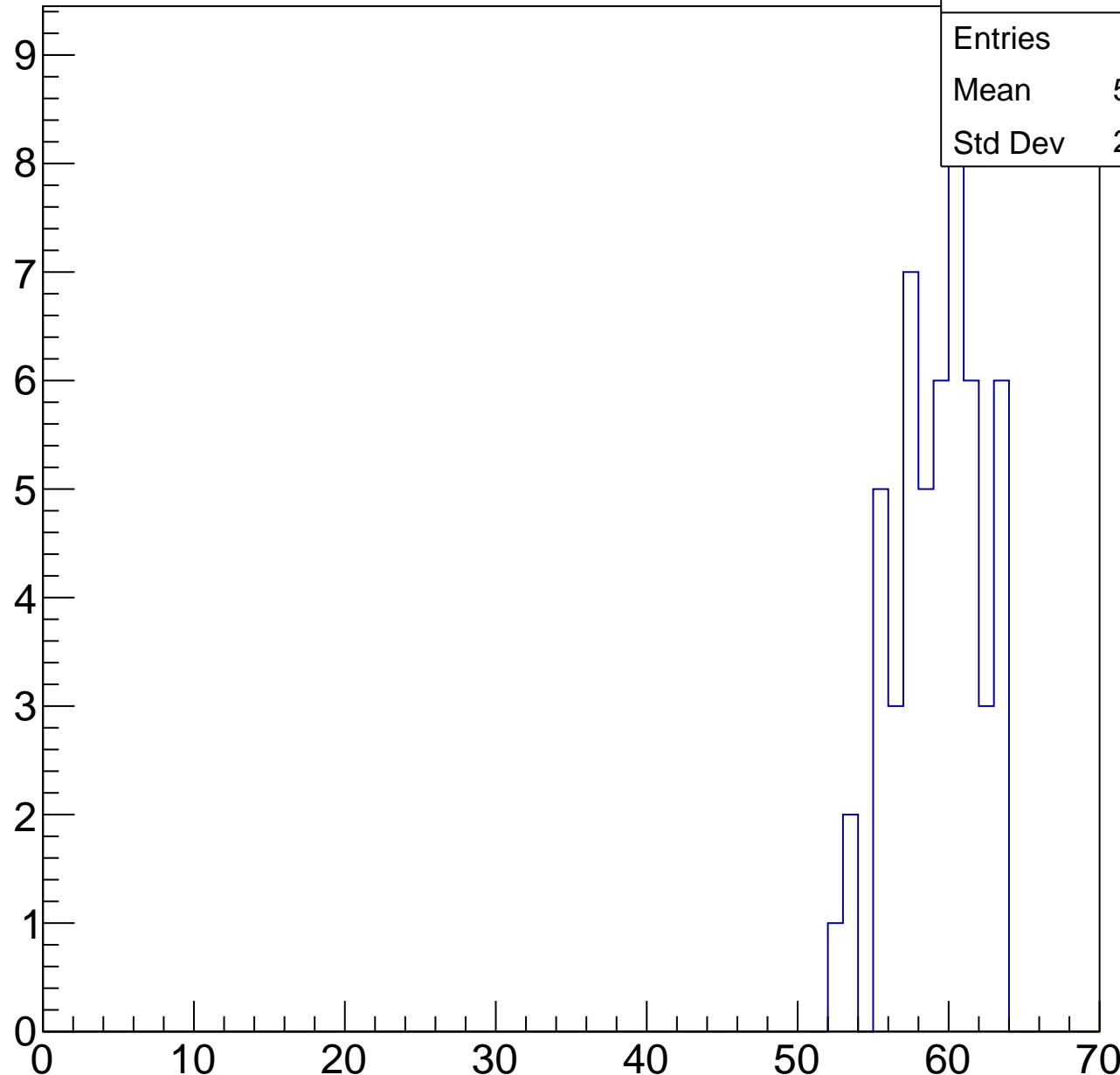
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	53
Mean	58.75
Std Dev	2.794

ampl

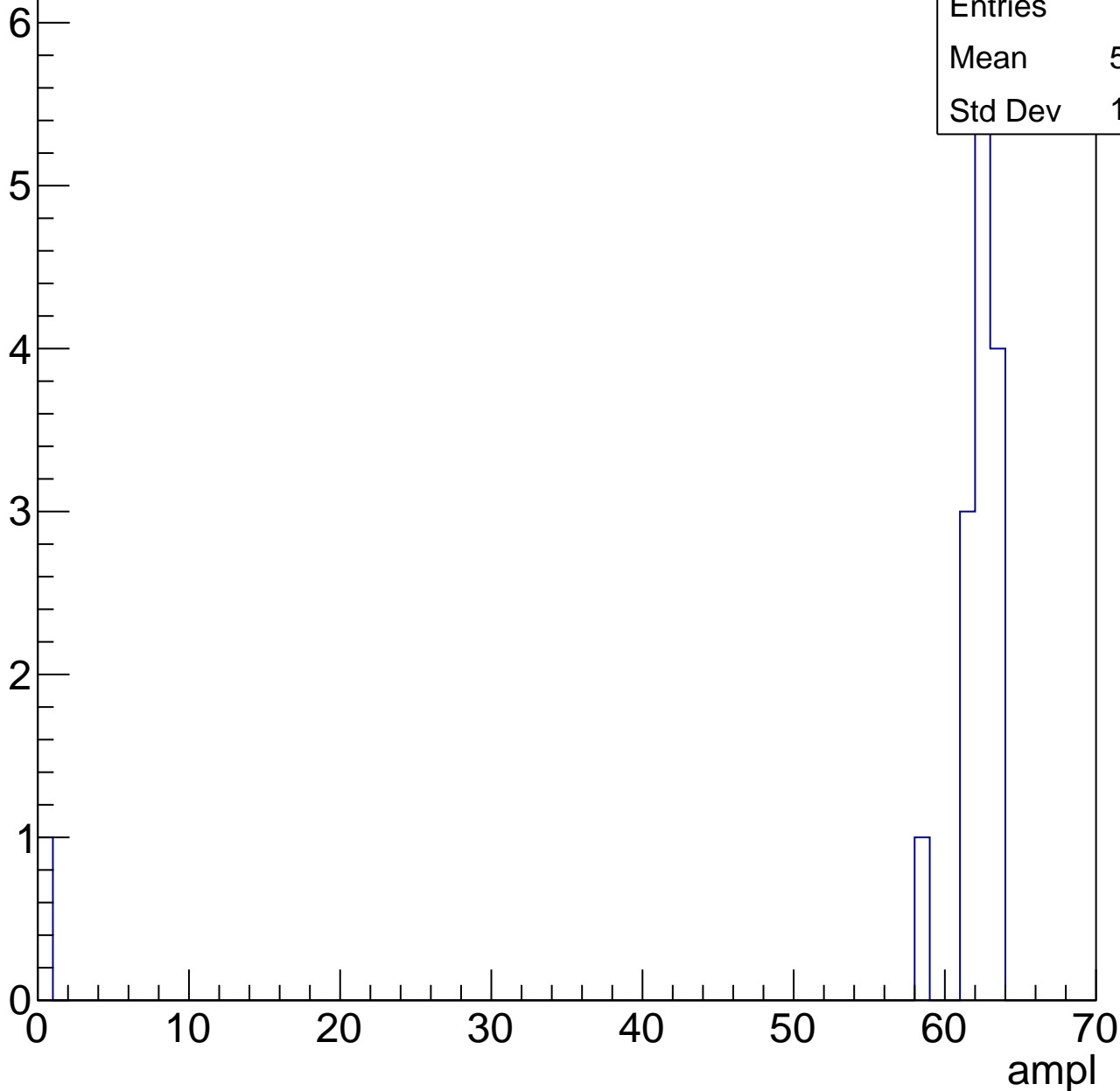


# B1L103S, U9-ch84, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	15
Mean	57.67
Std Dev	15.46





# B1L103S, U9-ch84, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

1

0.8

0.6

0.4

0.2

0

0

10

20

30

40

50

60

70

ampl

Entries

1

Mean

62

Std Dev

0

# B1L103S, U9-ch85, adc0

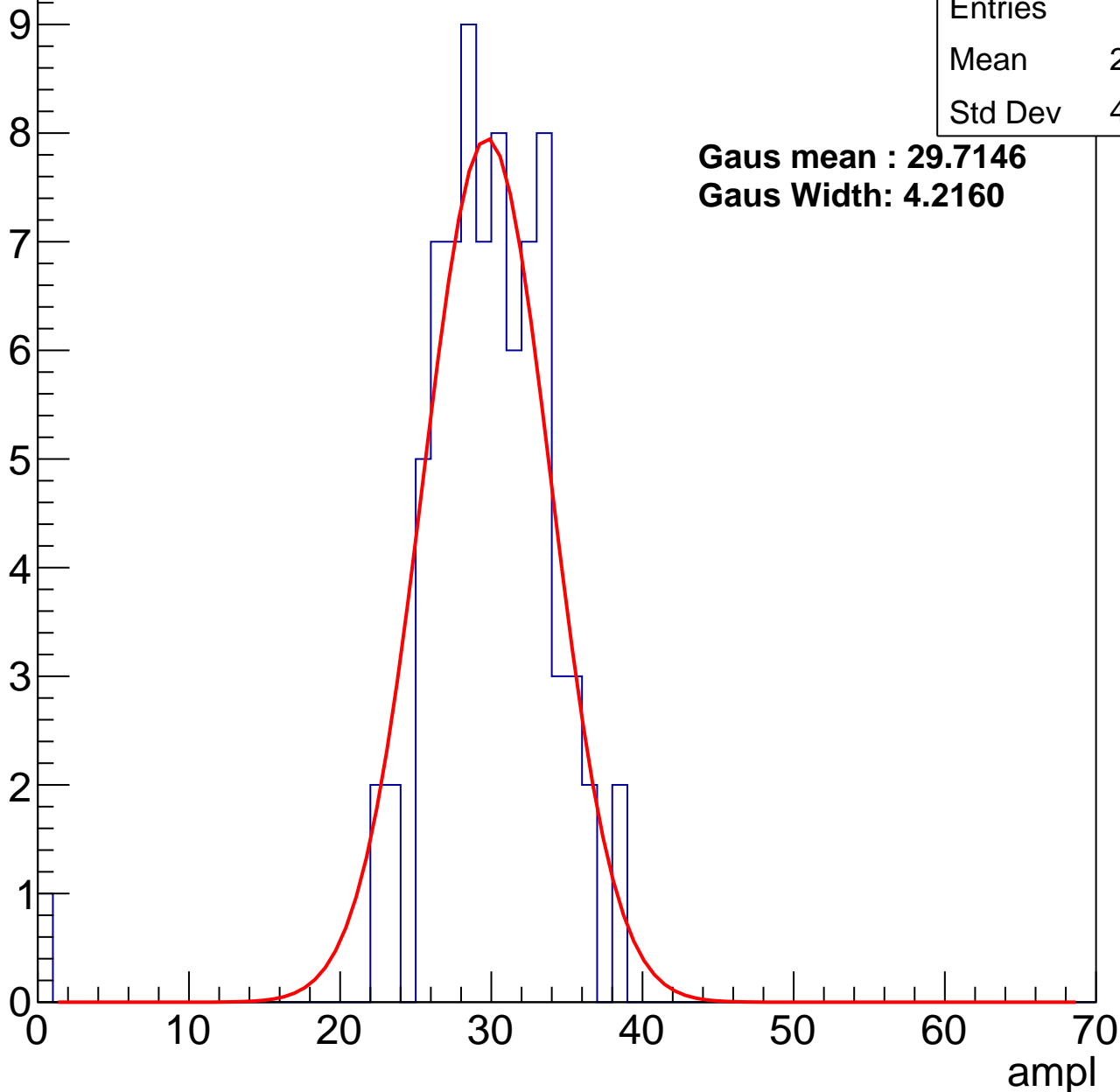
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	79
Mean	29.24
Std Dev	4.842

**Gaus mean : 29.7146**

**Gaus Width: 4.2160**



# B1L103S, U9-ch85, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	76
Mean	37.58
Std Dev	3.559

**Gaus mean : 38.2604**

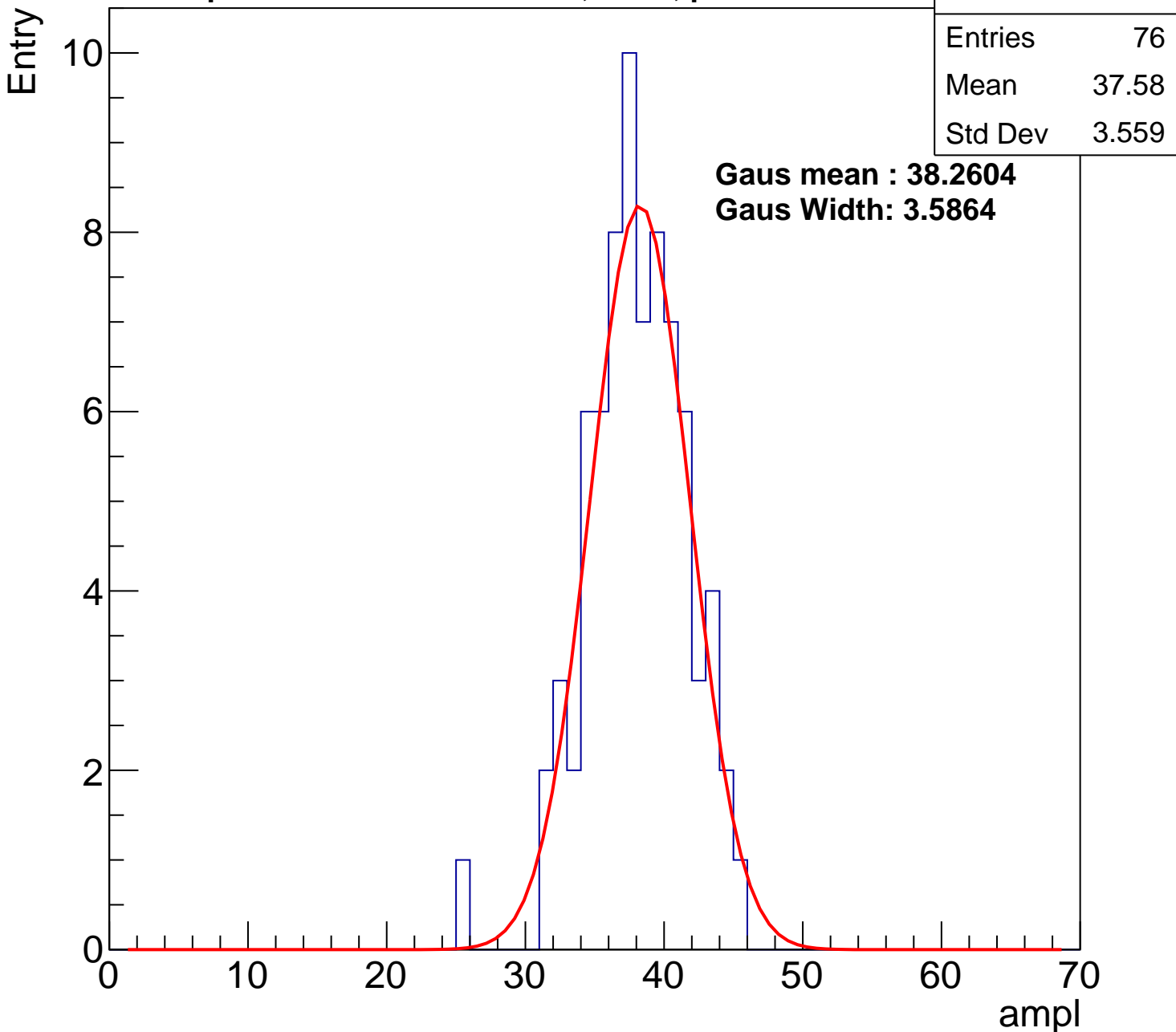
**Gaus Width: 3.5864**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U9-ch85, adc2

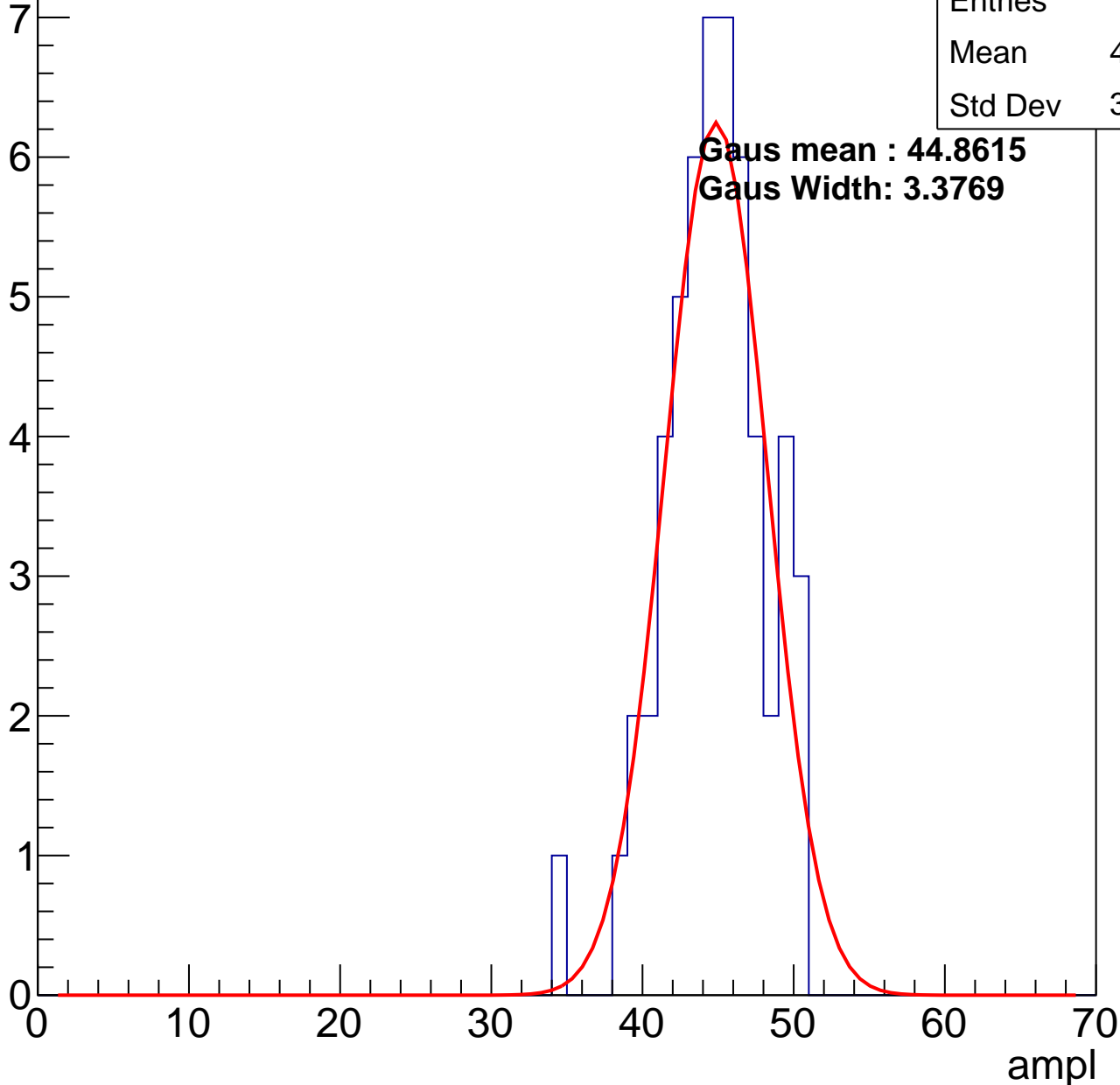
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	54
Mean	44.28
Std Dev	3.285

**Gaus mean : 44.8615**

**Gaus Width: 3.3769**

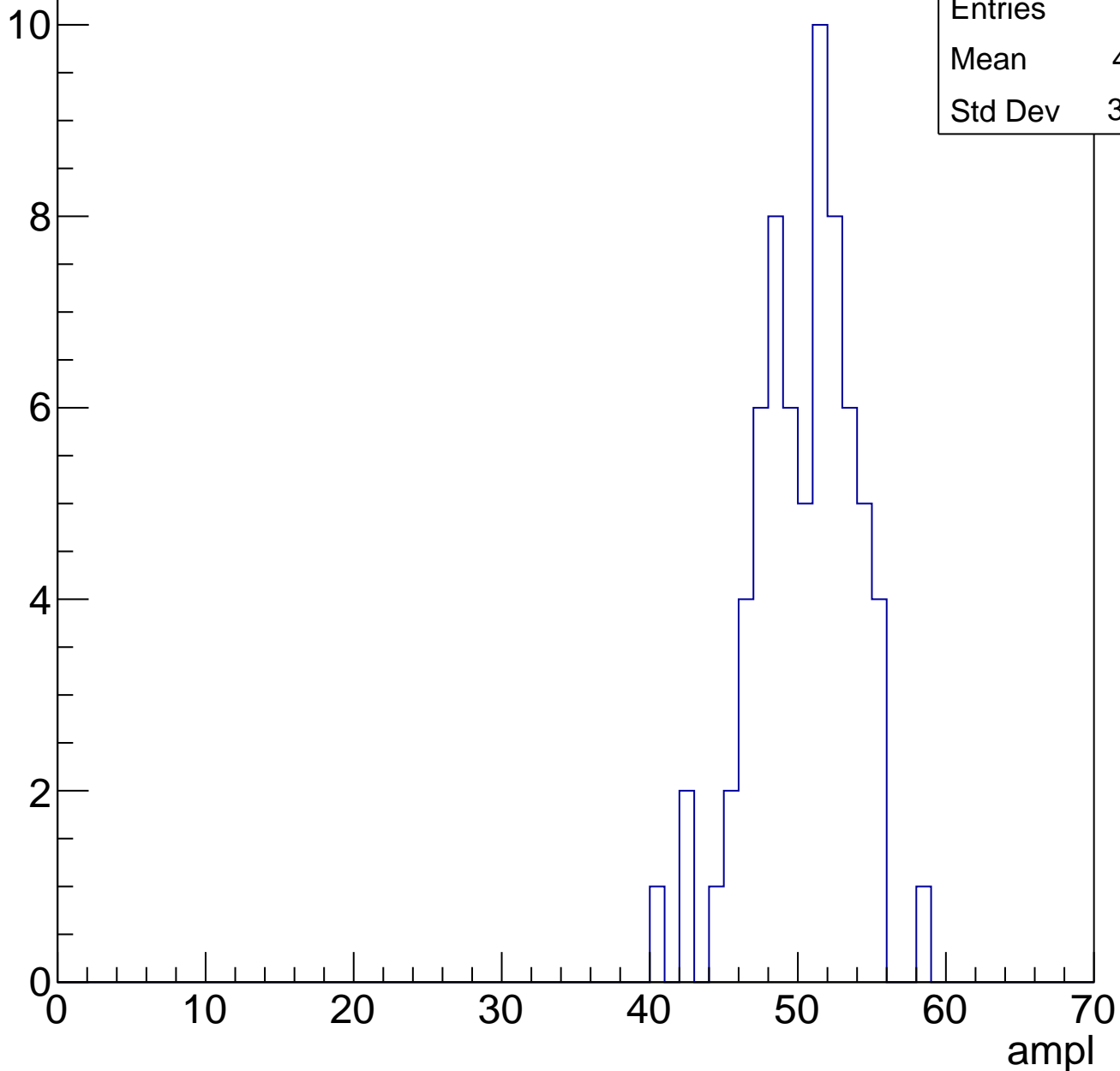


# B1L103S, U9-ch85, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

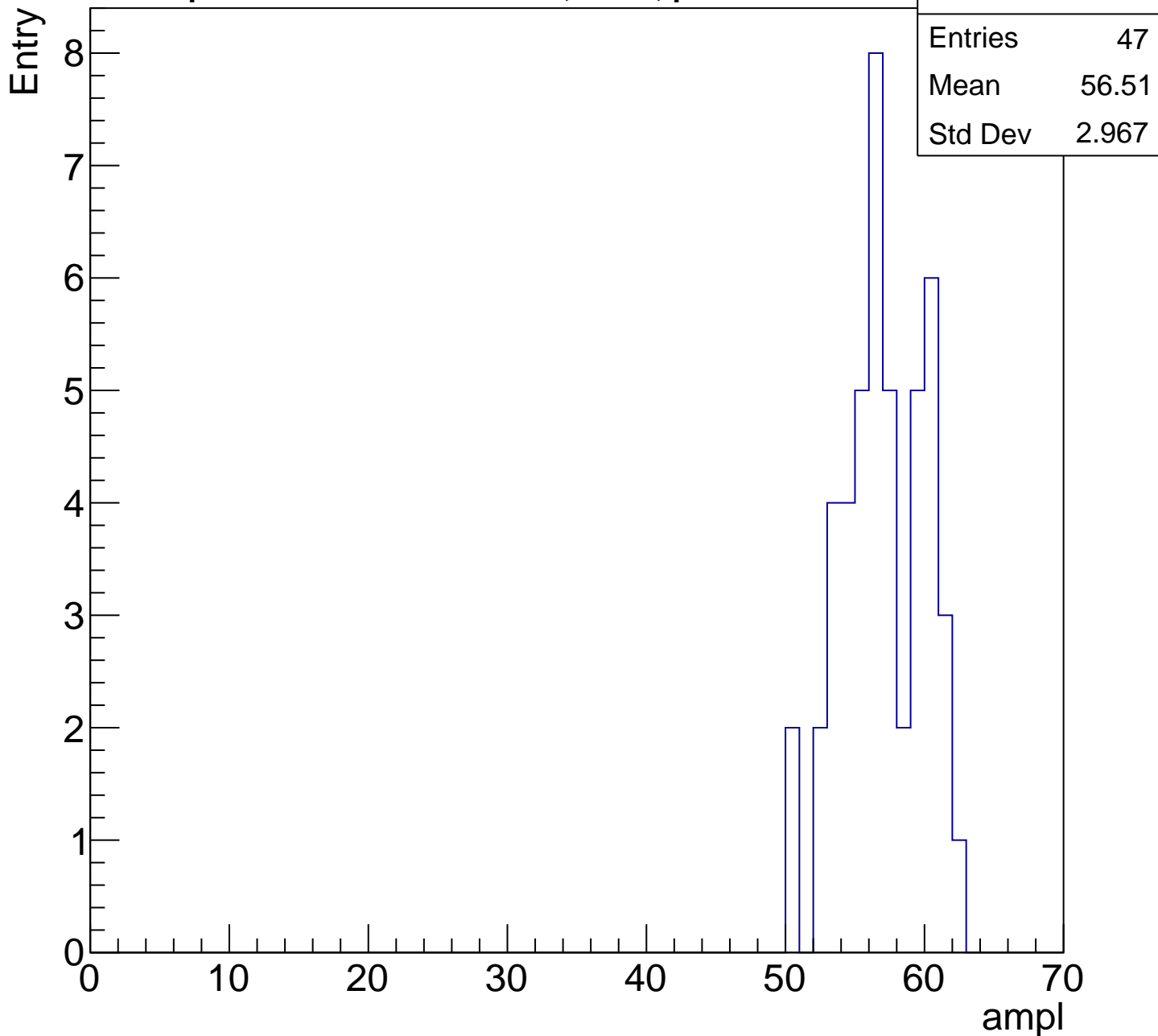
Entries	69
Mean	49.91
Std Dev	3.425

Entry



# B1L103S, U9-ch85, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

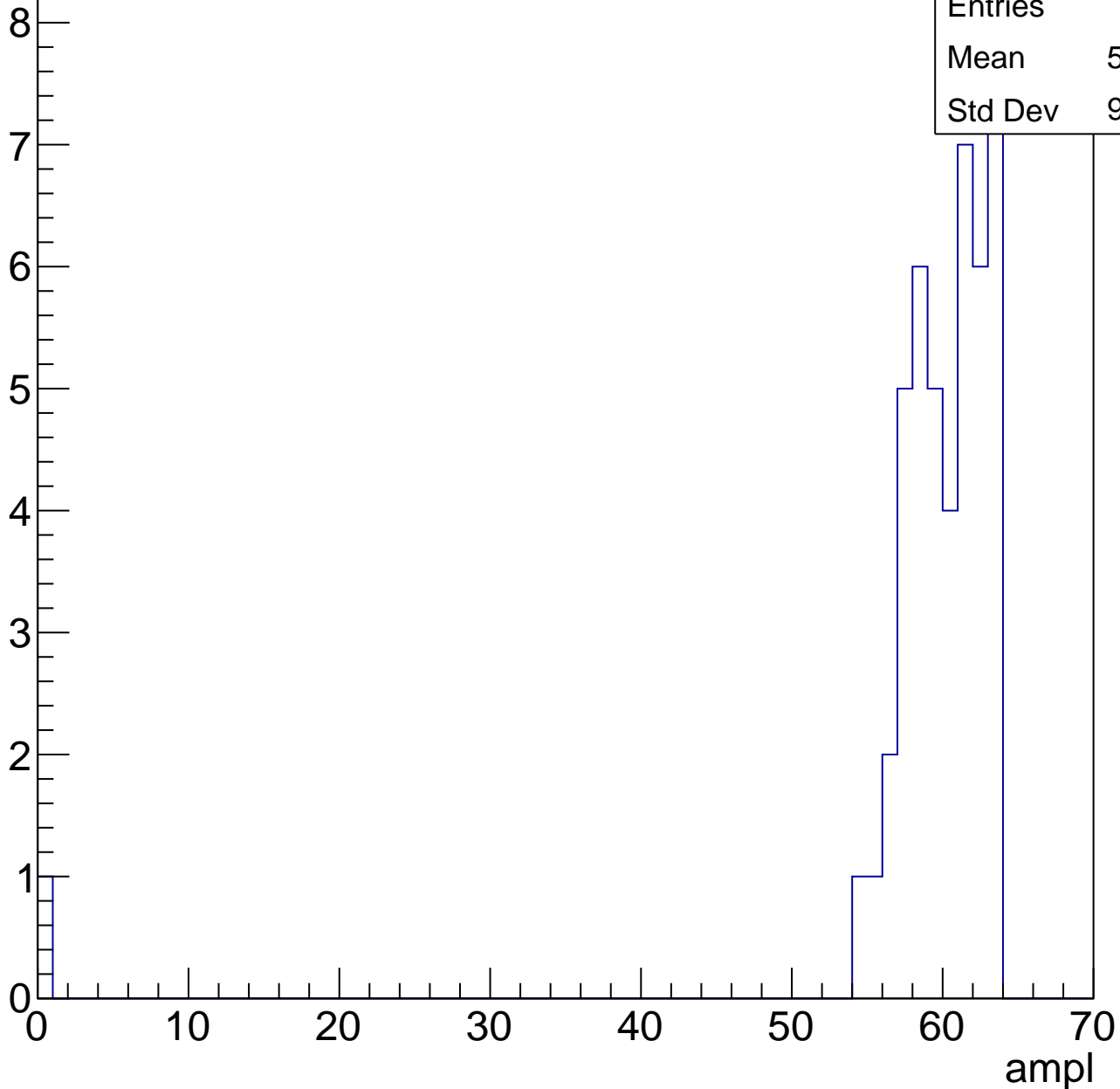


# B1L103S, U9-ch85, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

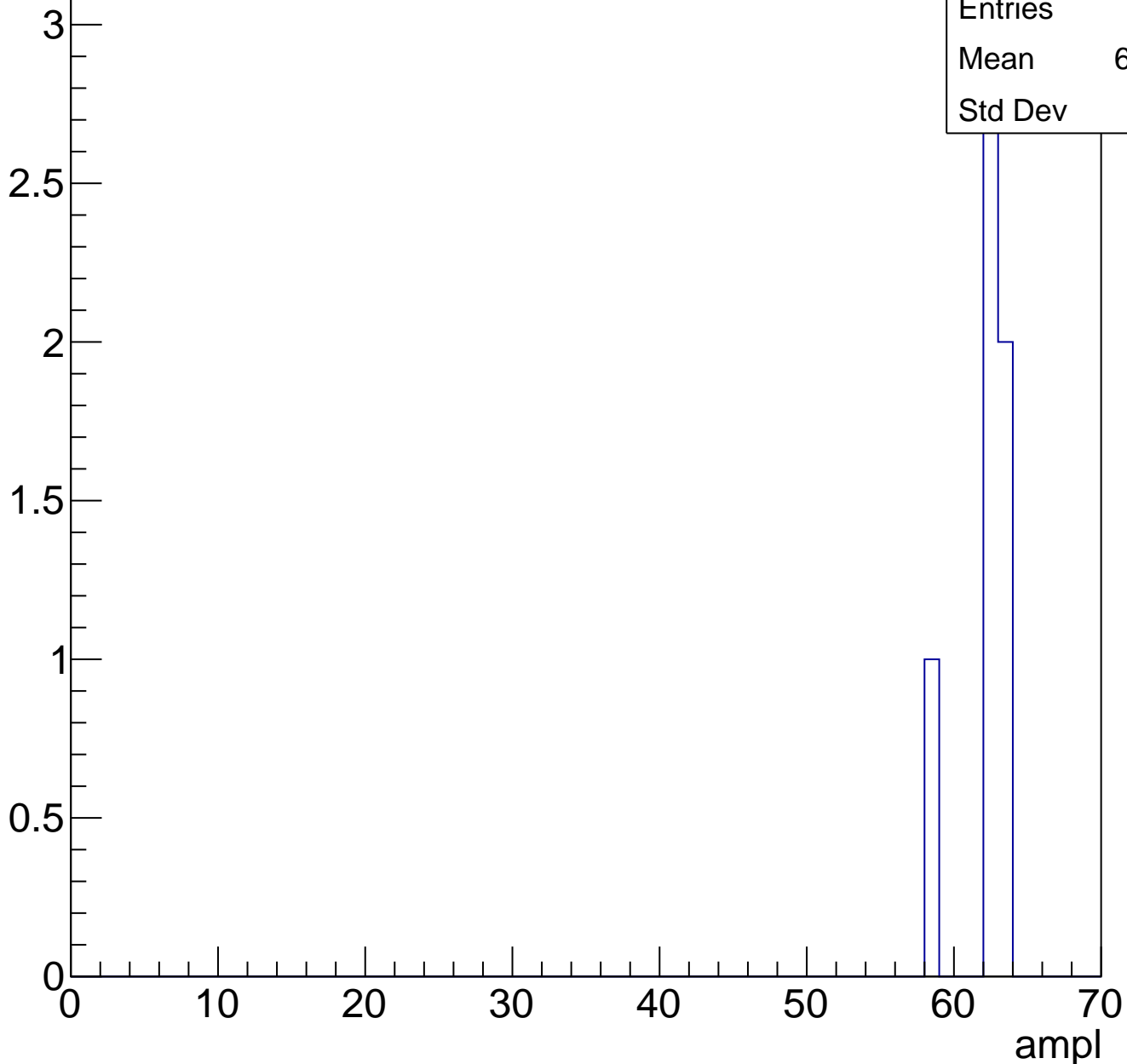
Entries	46
Mean	58.52
Std Dev	9.052



# B1L103S, U9-ch85, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U9-ch85, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U9-ch86, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	60
Mean	29.25
Std Dev	3.85

**Gaus mean : 28.9746**

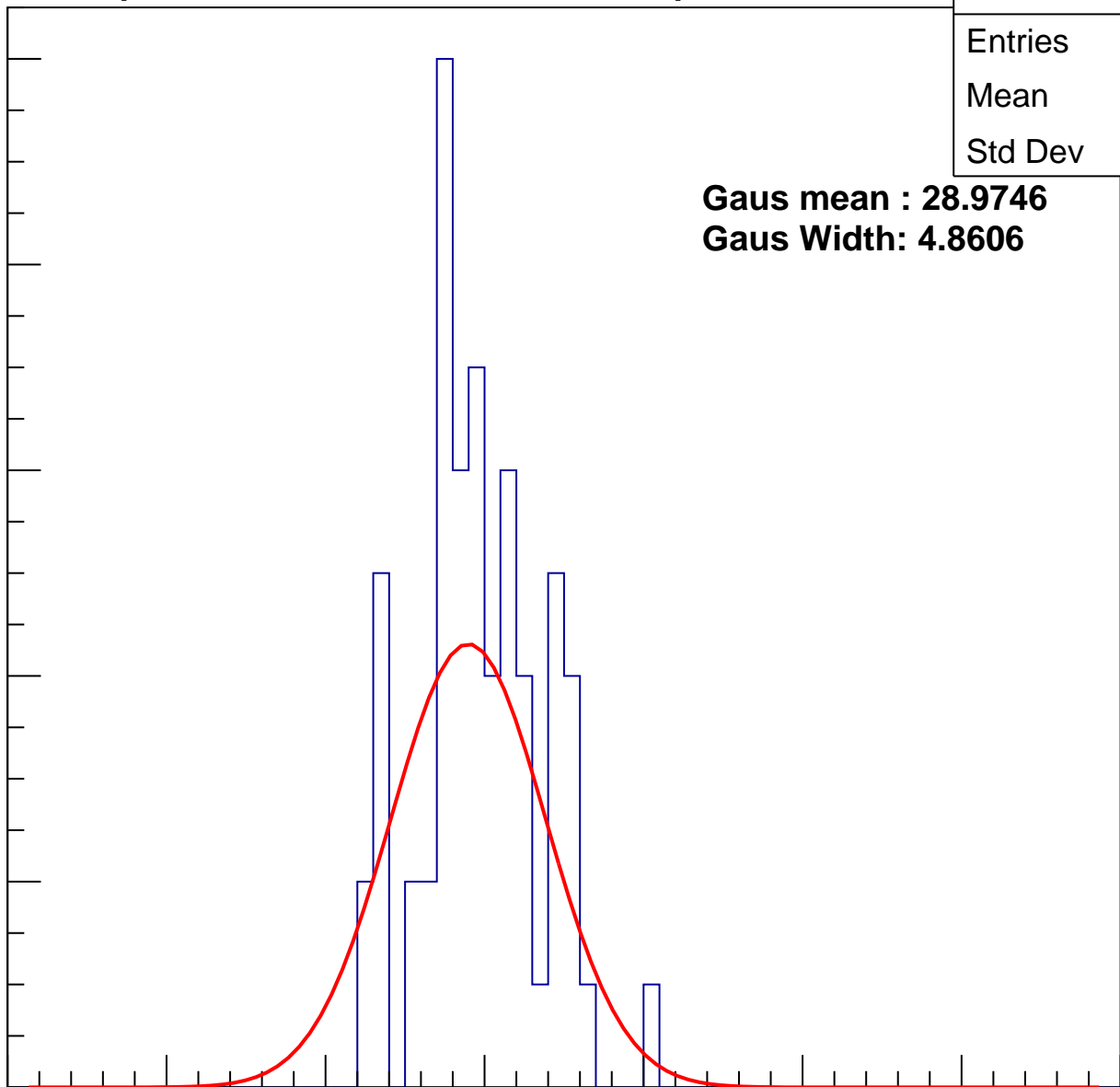
**Gaus Width: 4.8606**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U9-ch86, adc1

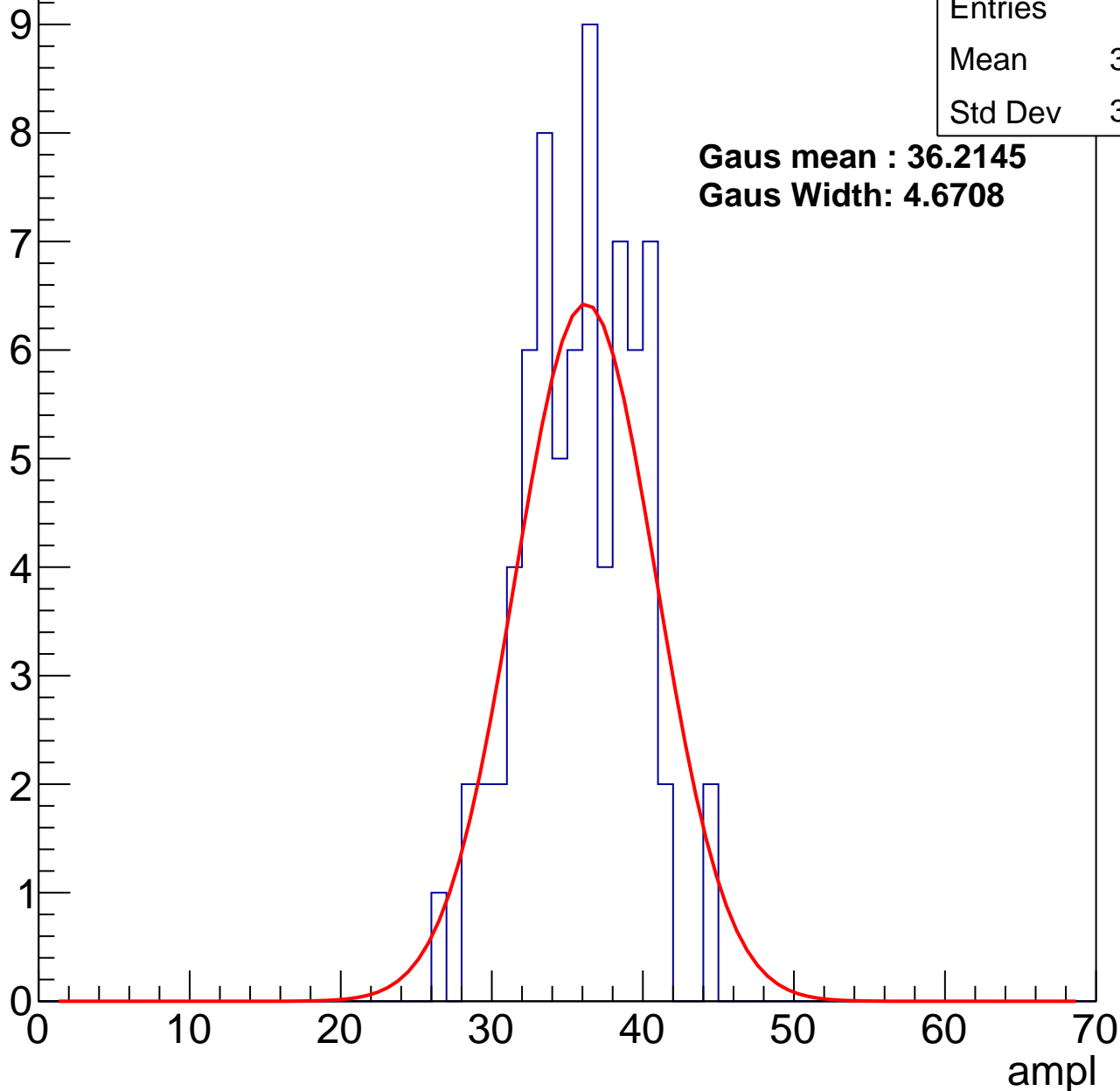
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	73
Mean	35.37
Std Dev	3.773

**Gaus mean : 36.2145**

**Gaus Width: 4.6708**



# B1L103S, U9-ch86, adc2

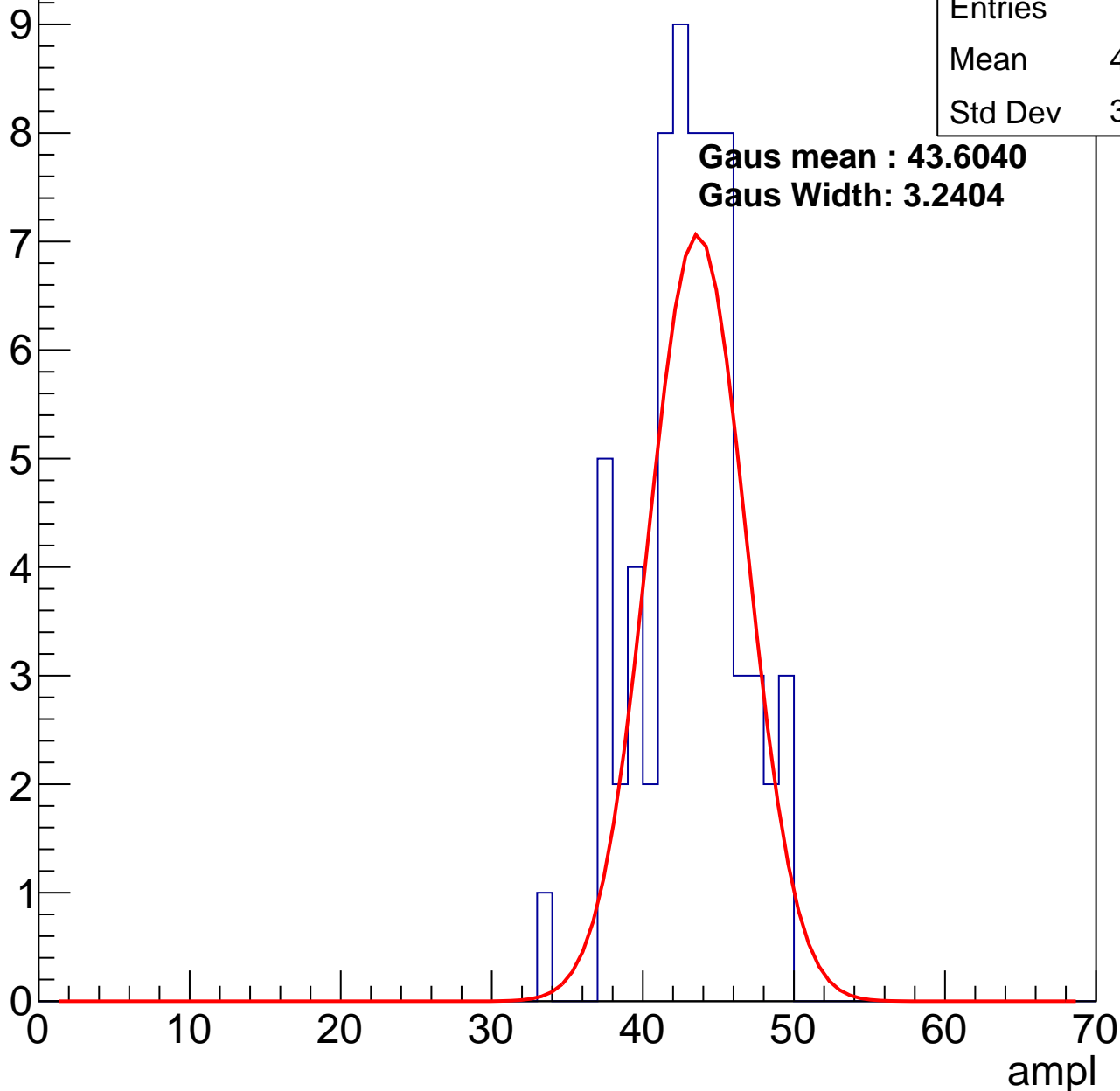
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	42.64
Std Dev	3.297

**Gaus mean : 43.6040**

**Gaus Width: 3.2404**



# B1L103S, U9-ch86, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

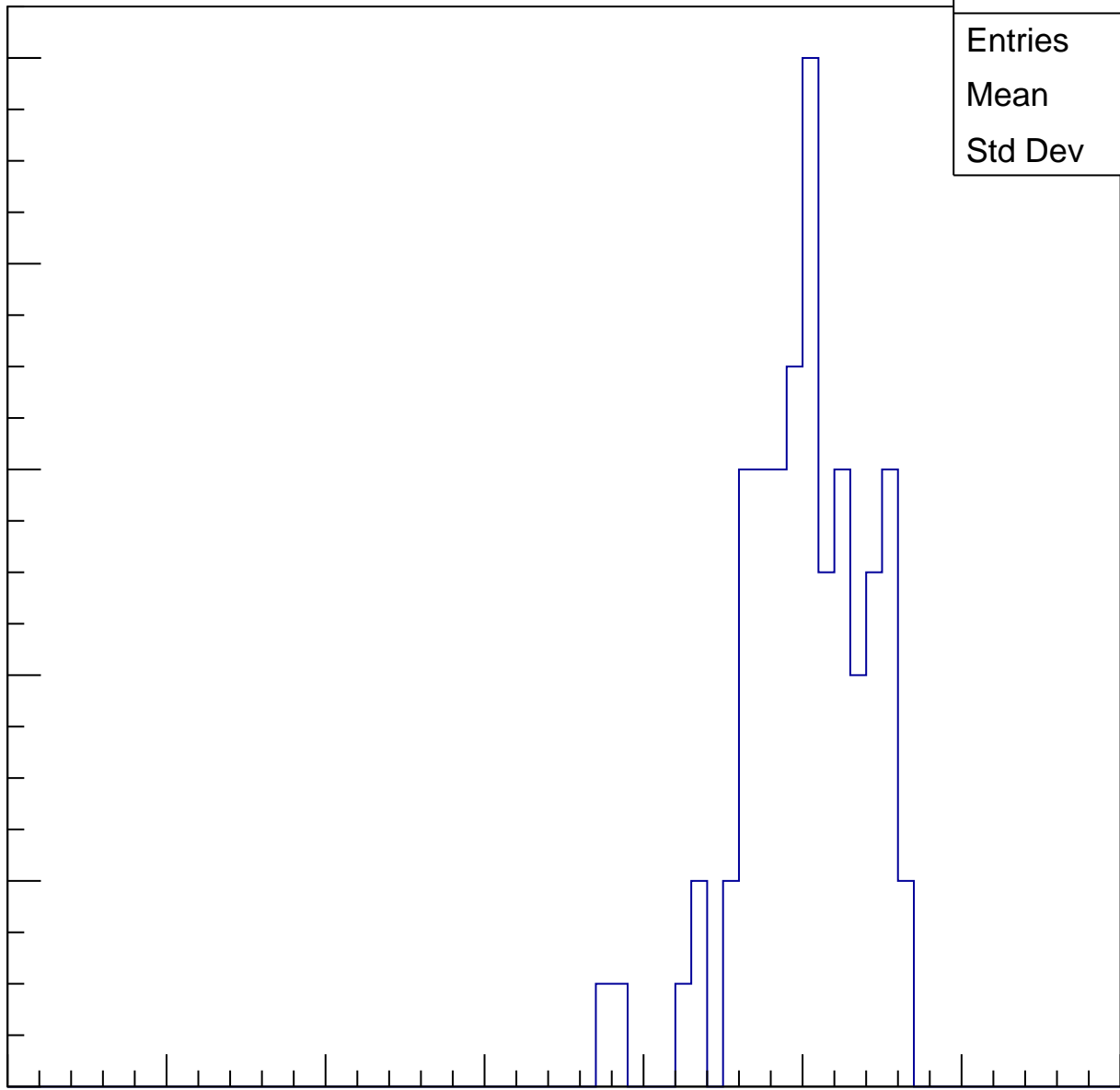
Entries	70
Mean	49.61
Std Dev	3.896

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

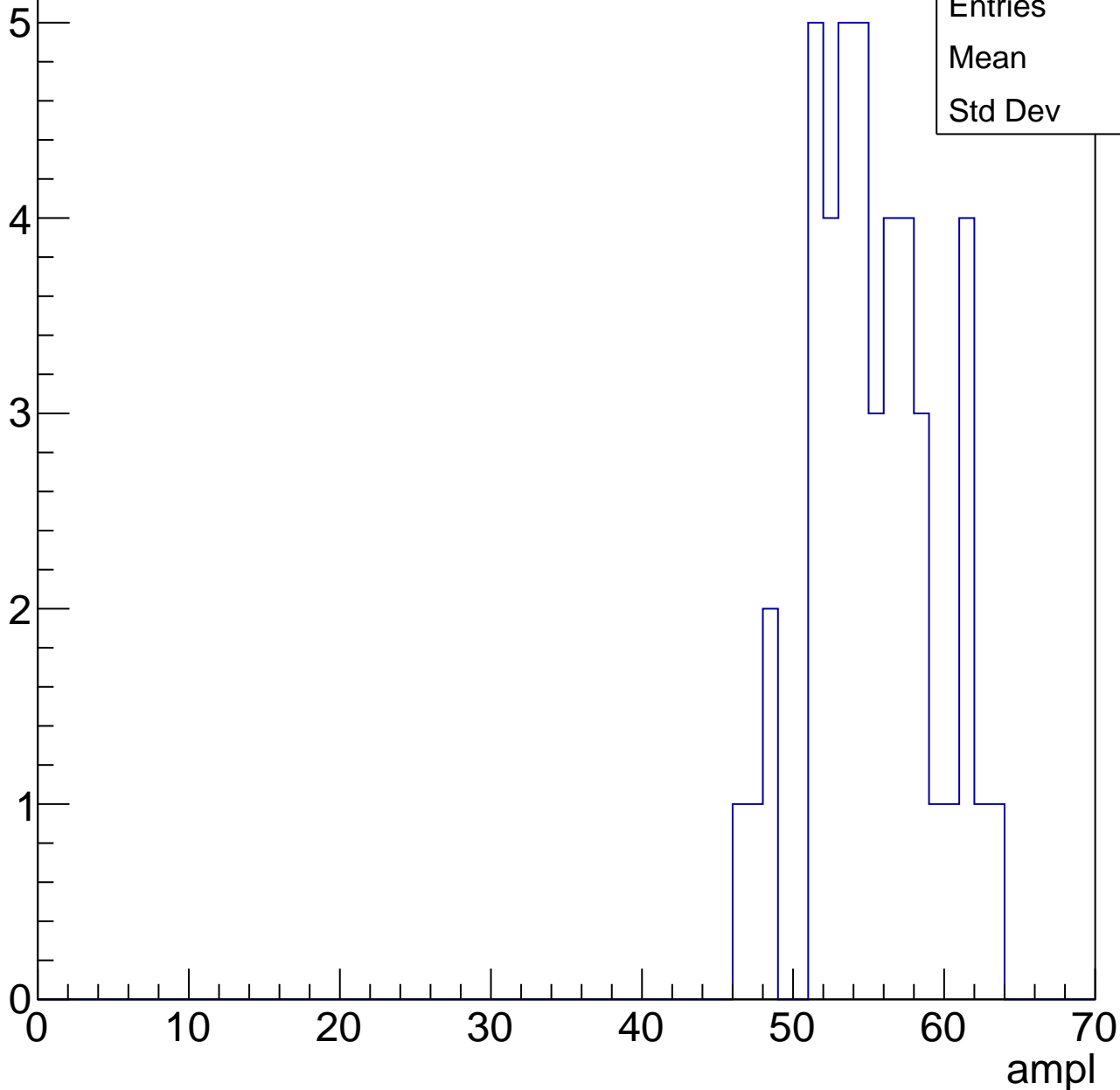


# B1L103S, U9-ch86, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

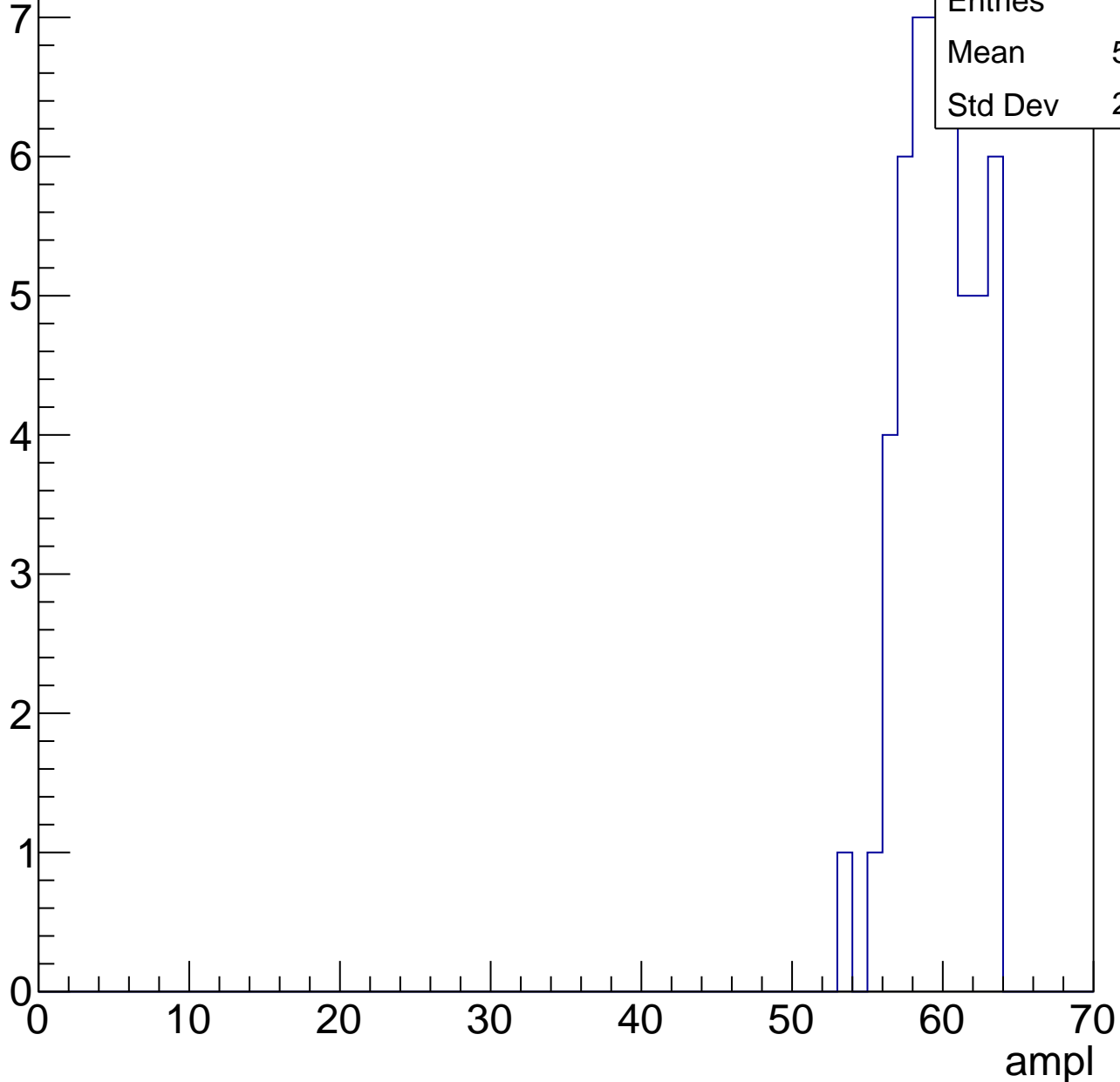
Entries	45
Mean	54.8
Std Dev	4.02



# B1L103S, U9-ch86, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

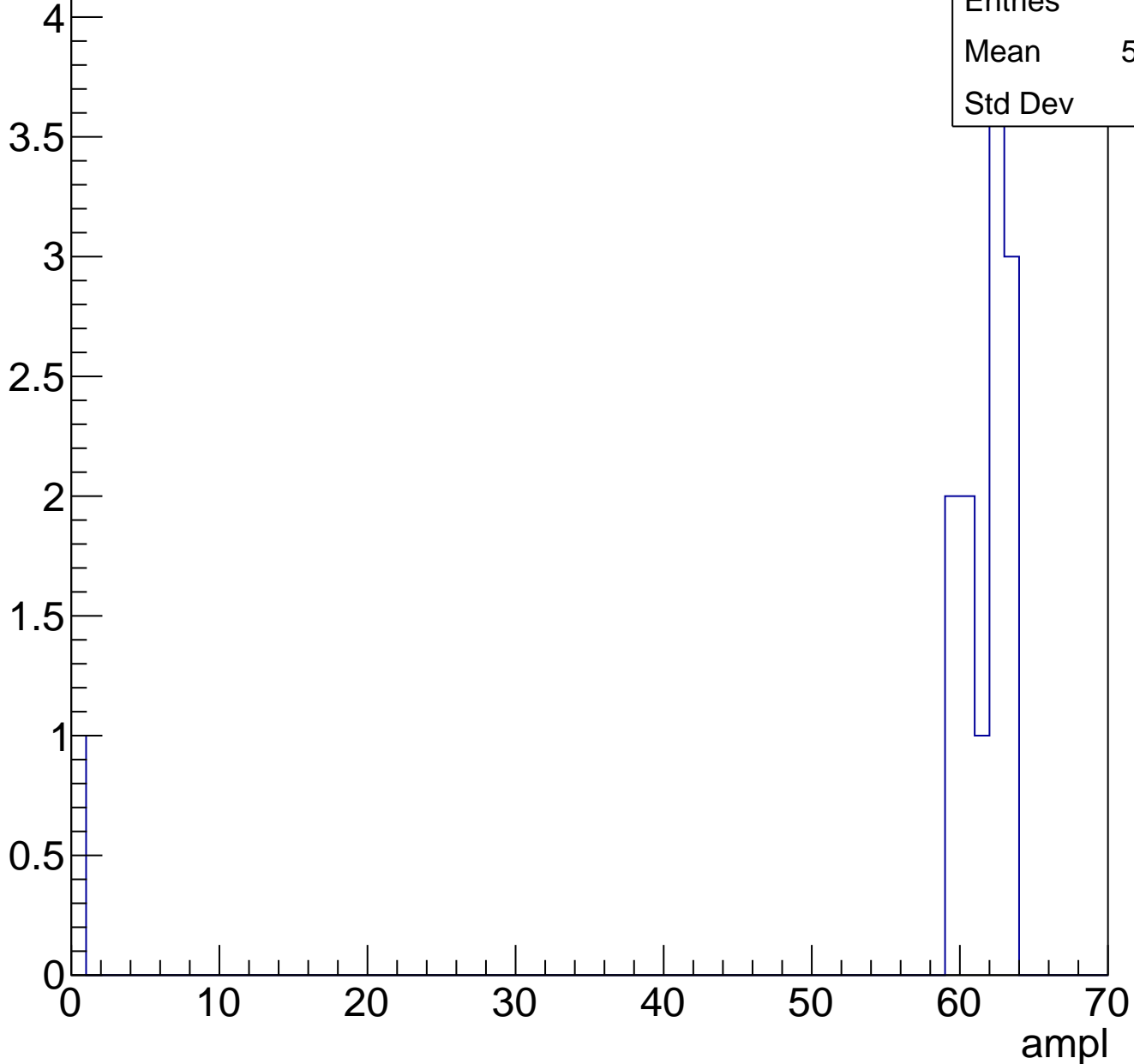


Entries	49
Mean	59.31
Std Dev	2.401

# B1L103S, U9-ch86, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U9-ch86, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U9-ch87, adc0

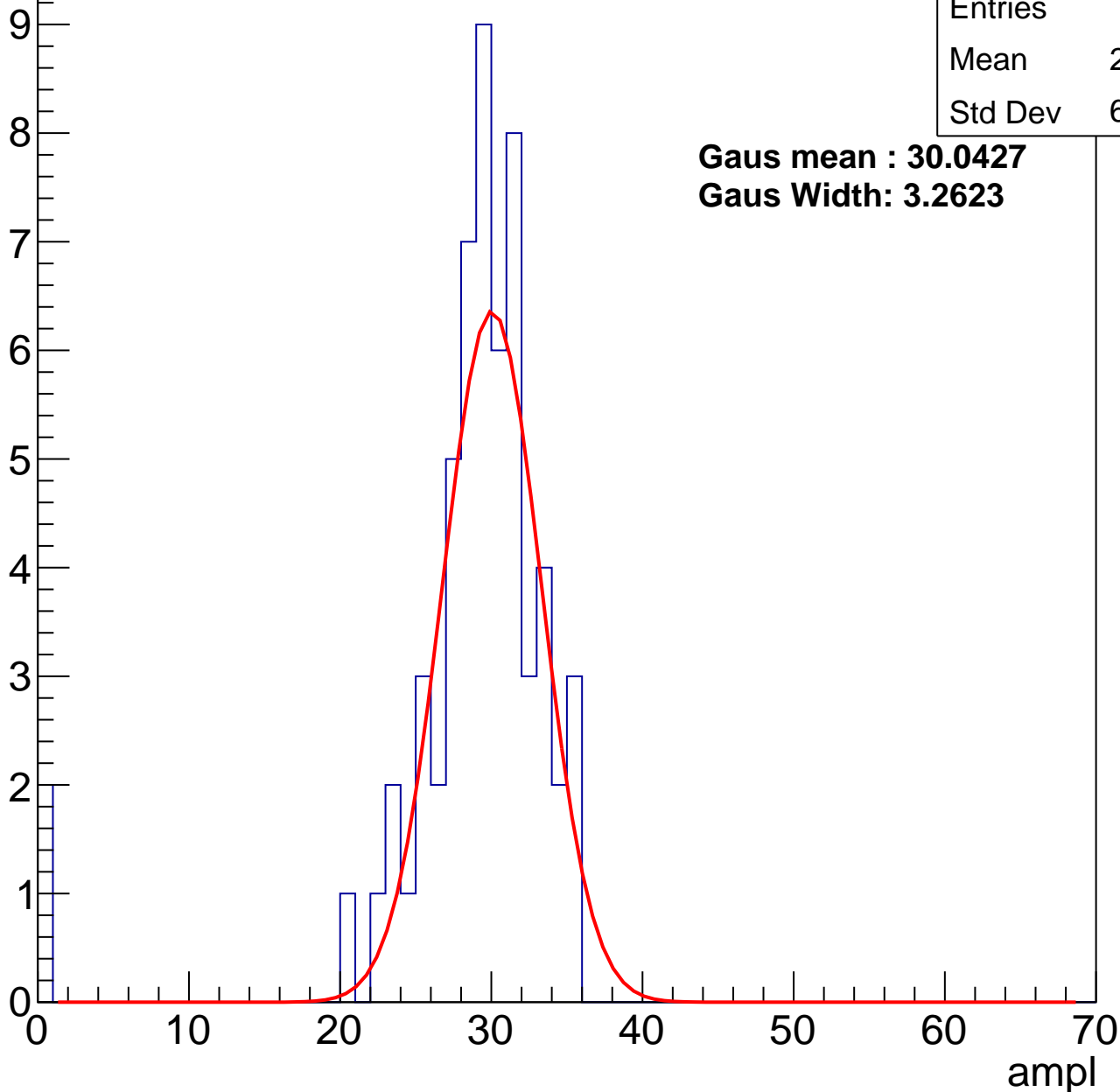
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	59
Mean	28.14
Std Dev	6.168

**Gaus mean : 30.0427**

**Gaus Width: 3.2623**



# B1L103S, U9-ch87, adc1

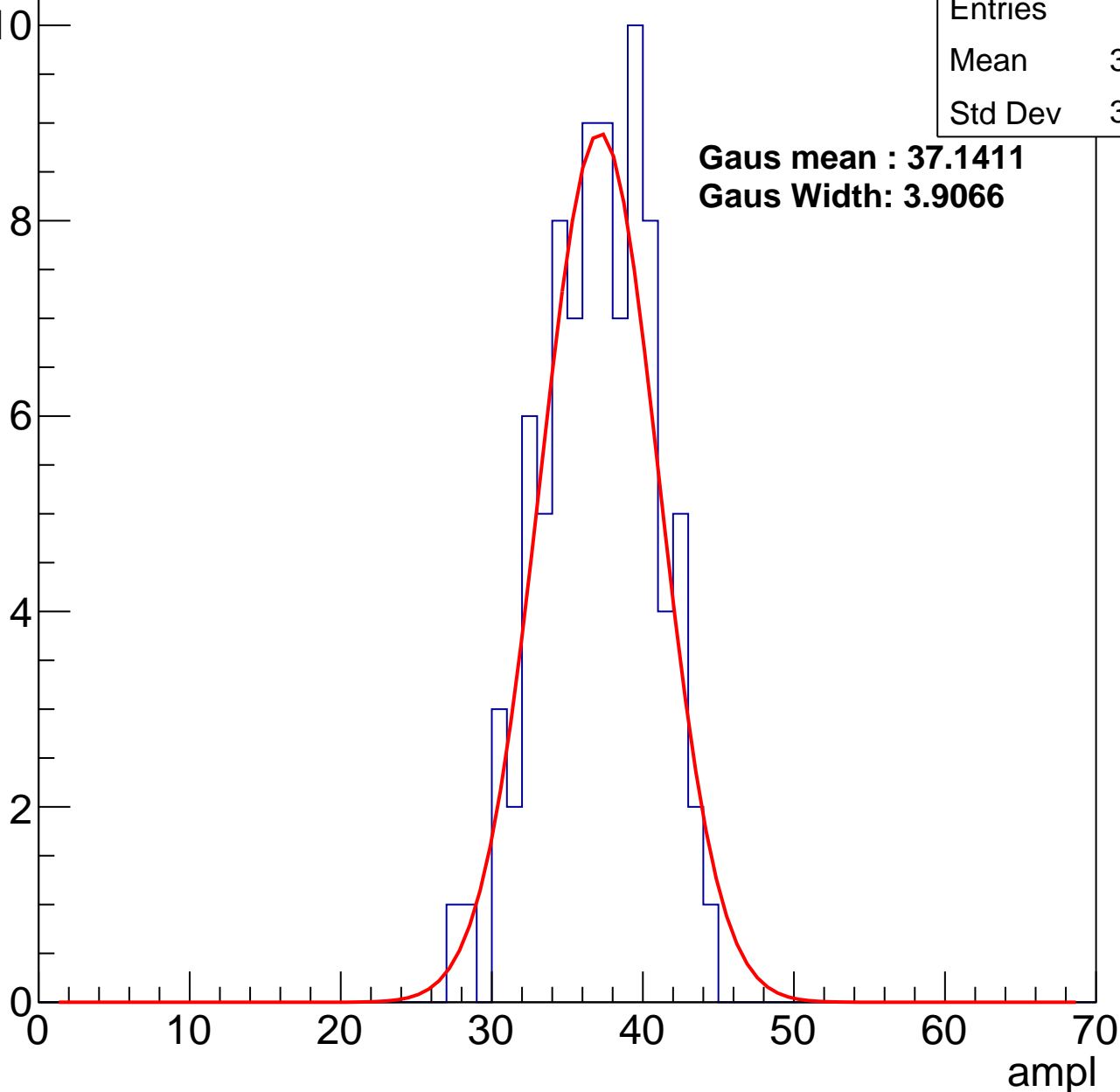
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	88
Mean	36.57
Std Dev	3.617

**Gaus mean : 37.1411**

**Gaus Width: 3.9066**



# B1L103S, U9-ch87, adc2

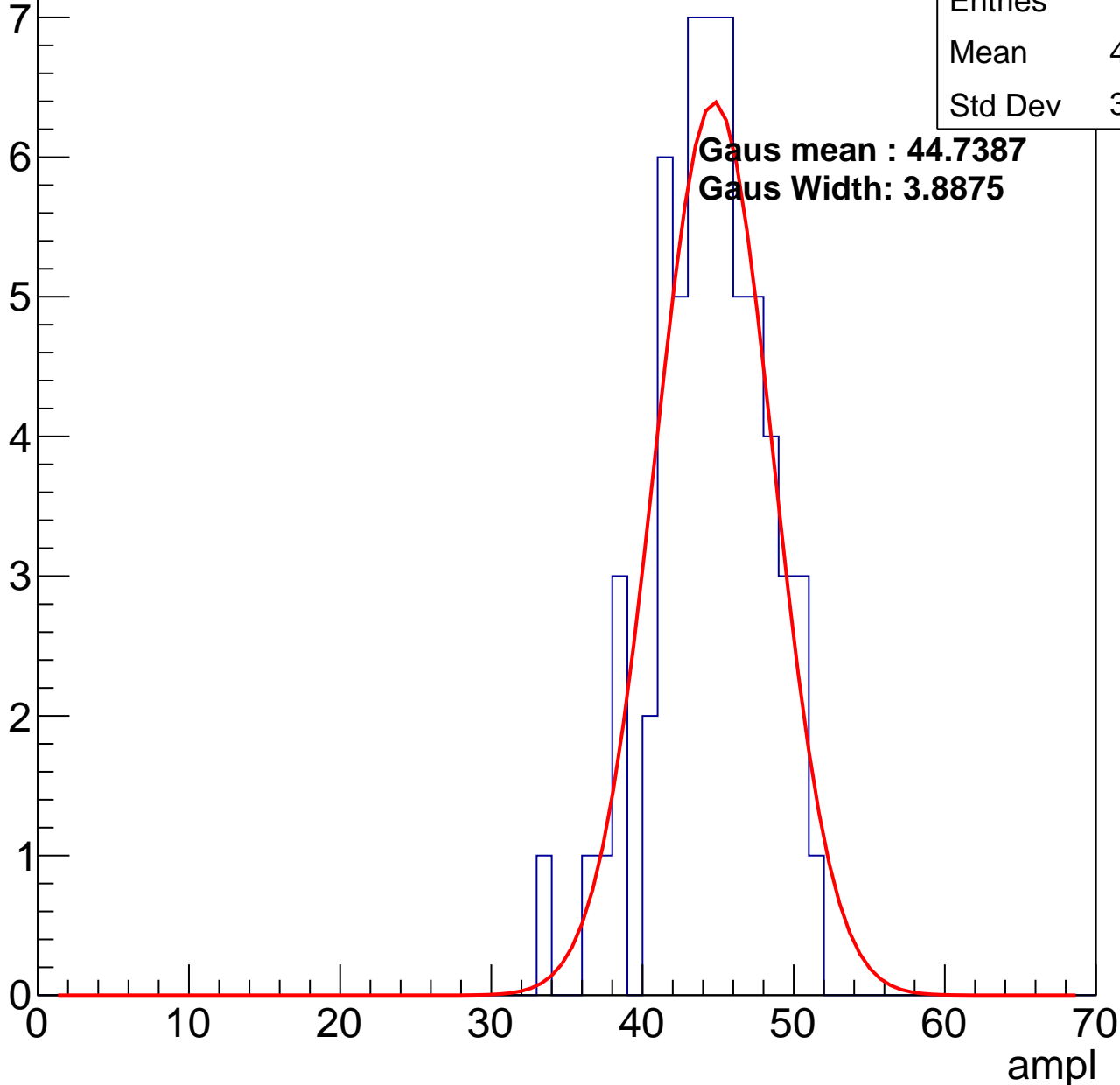
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	61
Mean	44.02
Std Dev	3.673

**Gaus mean : 44.7387**

**Gaus Width: 3.8875**

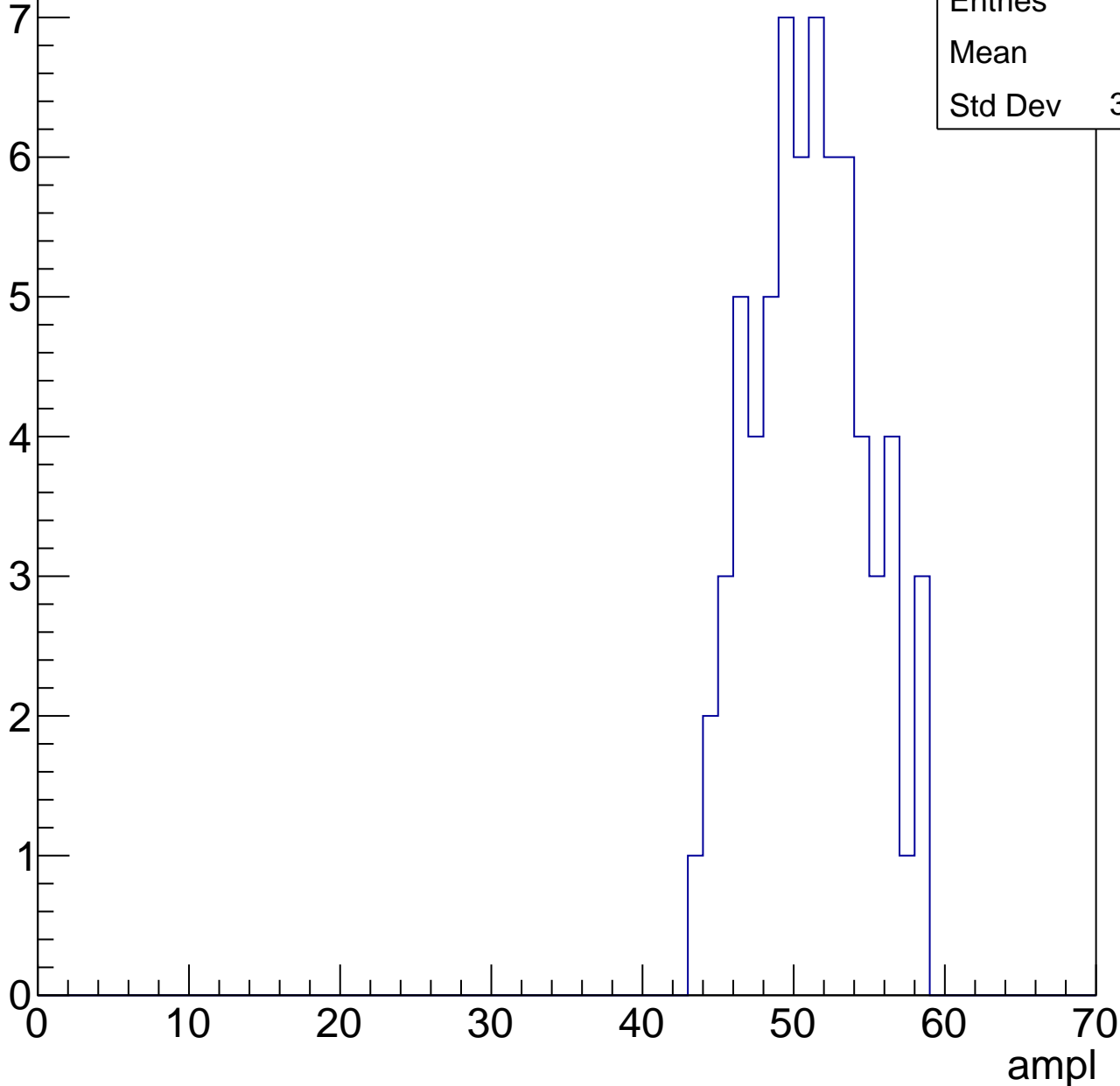


# B1L103S, U9-ch87, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	50.6
Std Dev	3.714

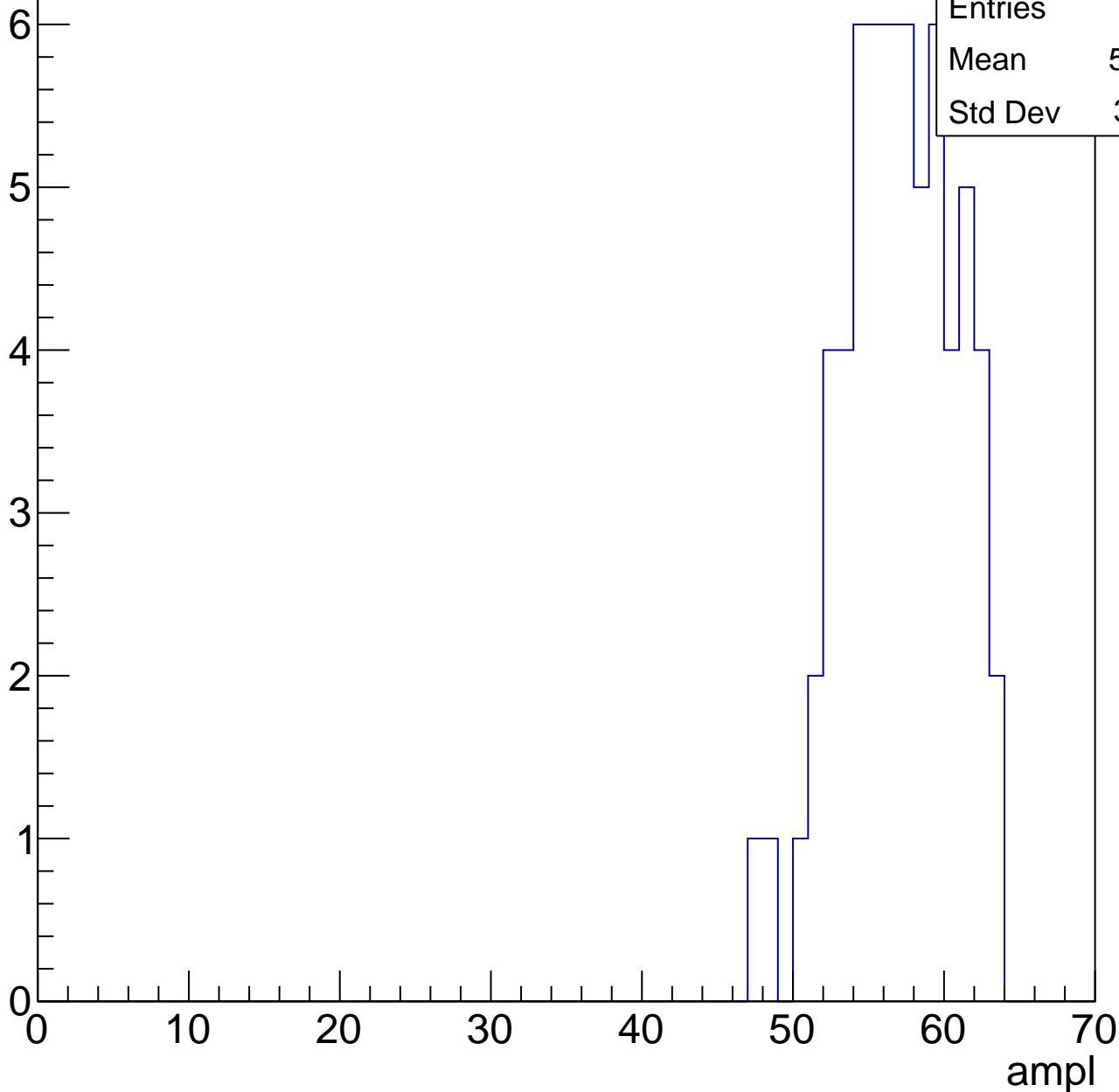


# B1L103S, U9-ch87, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	56.54
Std Dev	3.681

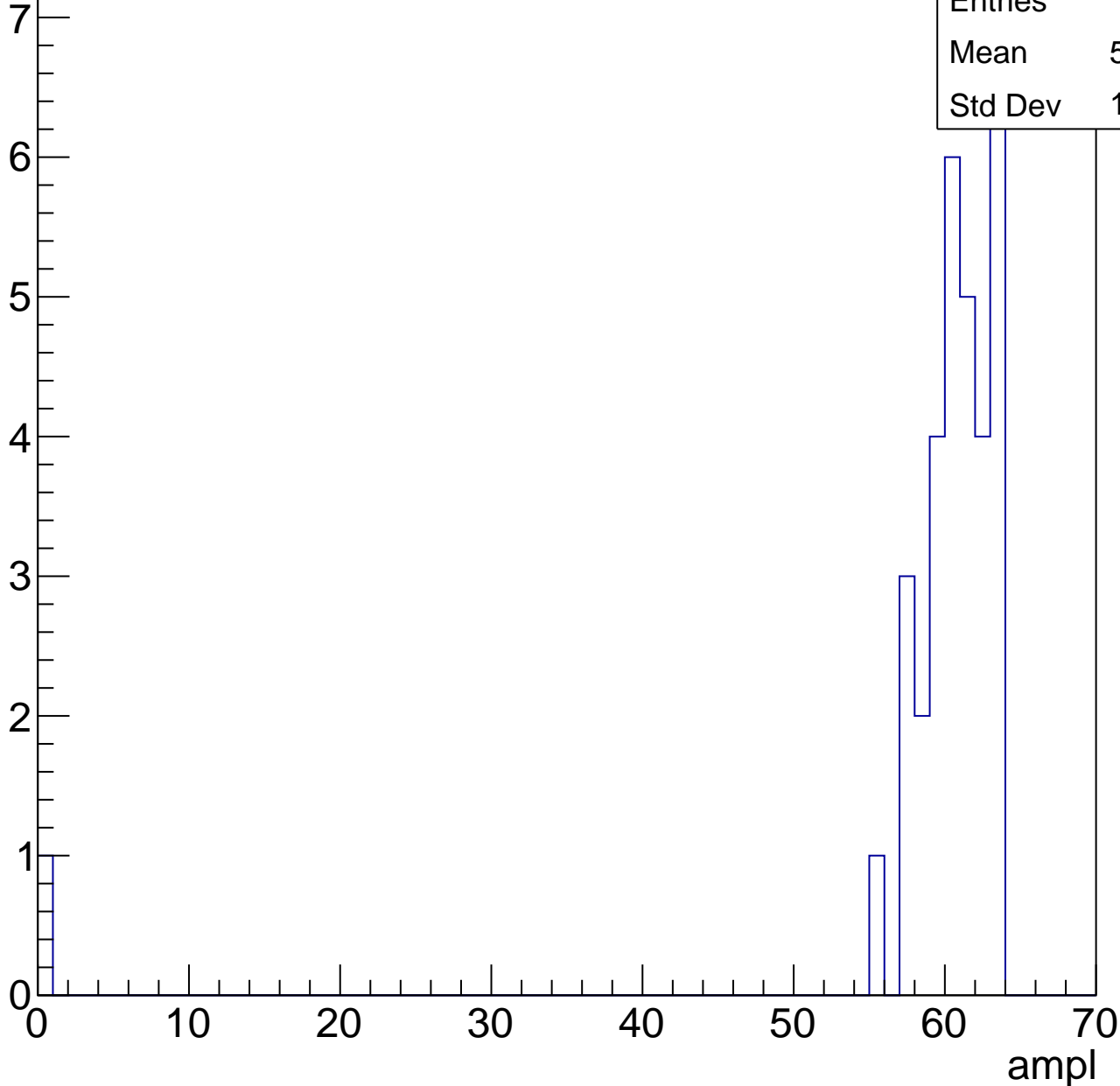


# B1L103S, U9-ch87, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	33
Mean	58.55
Std Dev	10.56



# B1L103S, U9-ch87, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	3
Mean	62.33
Std Dev	0.4714

ampl



# B1L103S, U9-ch87, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U9-ch88, adc0

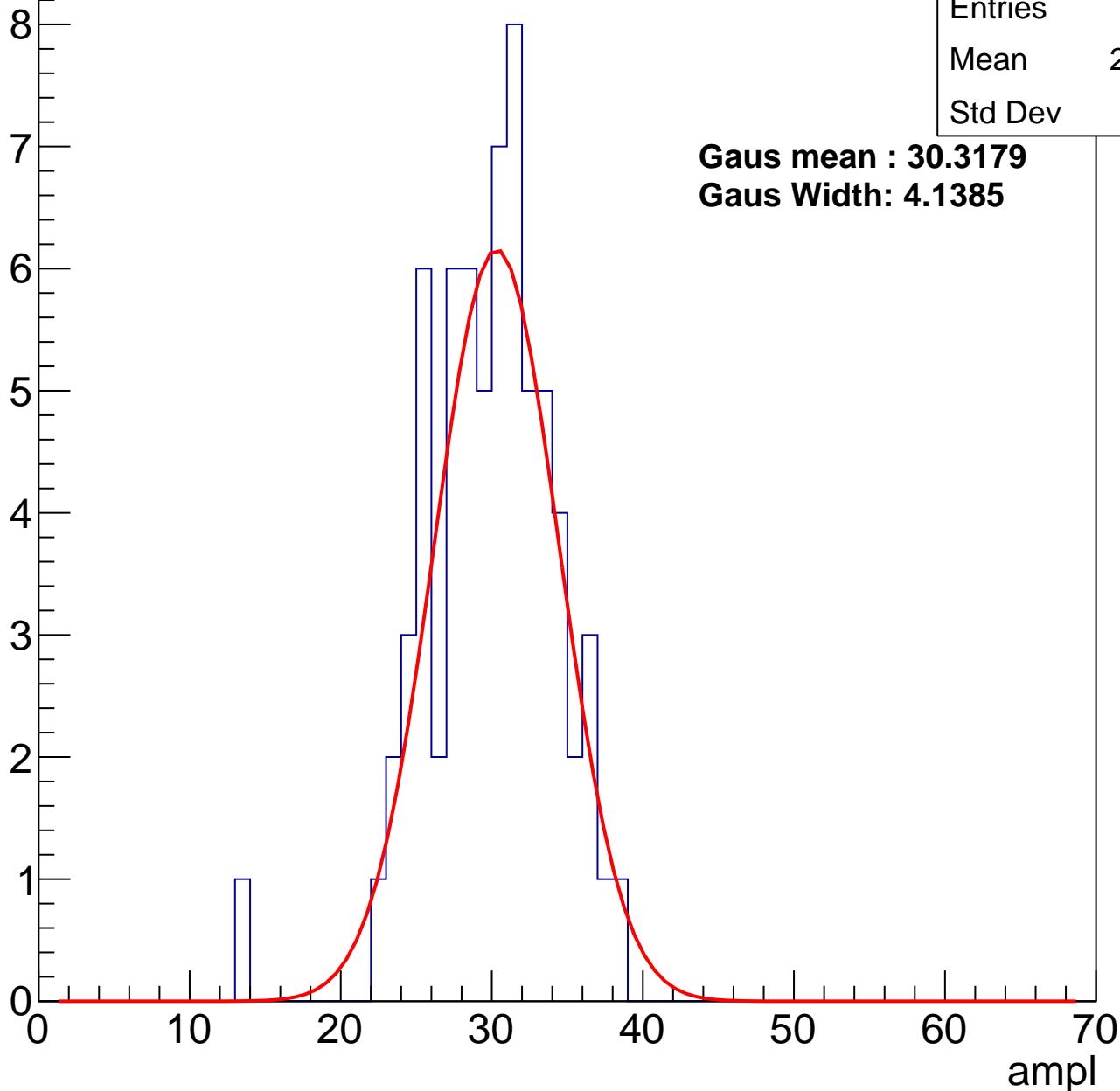
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	68
Mean	29.44
Std Dev	4.22

**Gaus mean : 30.3179**

**Gaus Width: 4.1385**



# B1L103S, U9-ch88, adc1

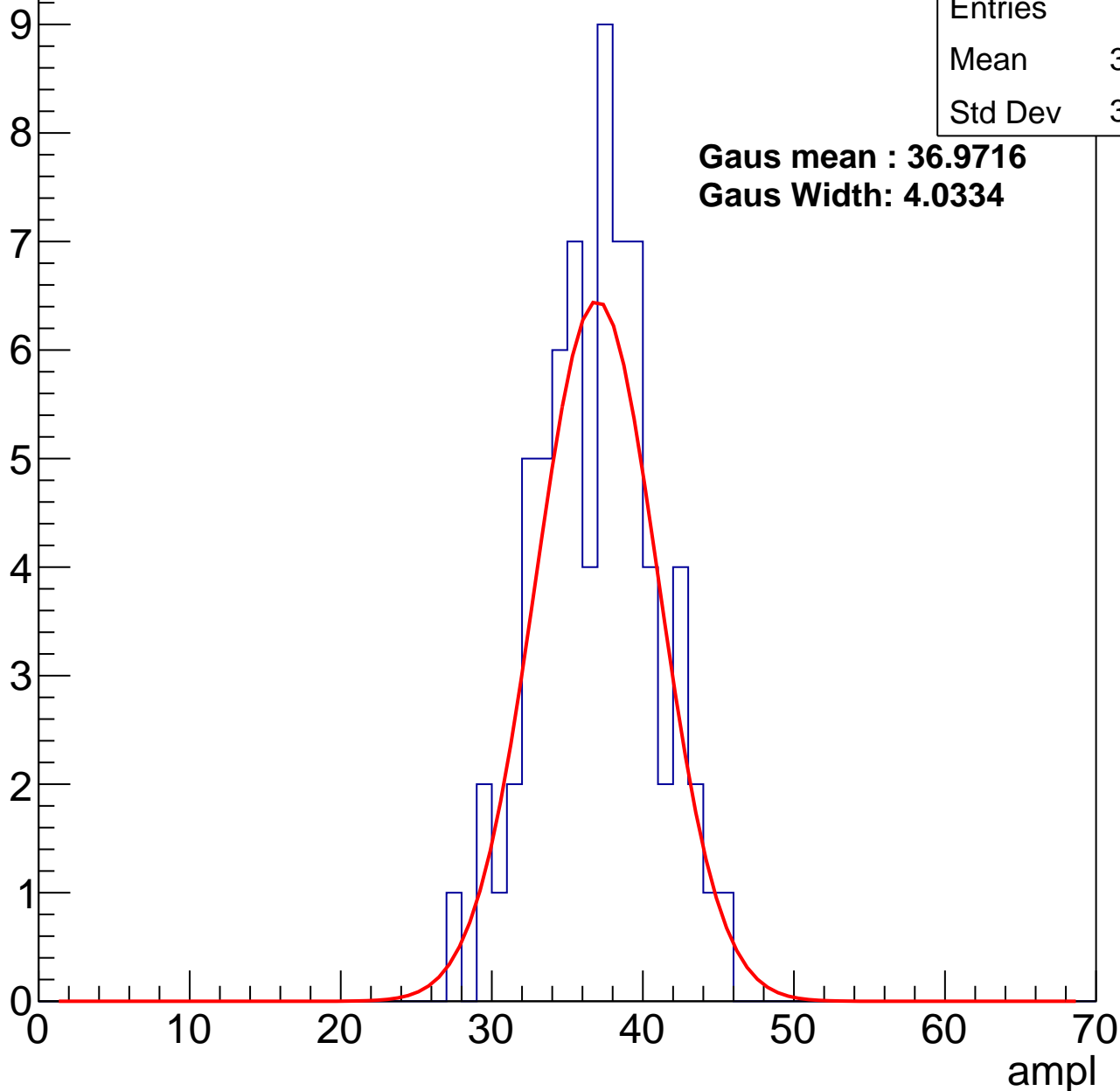
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	70
Mean	36.46
Std Dev	3.794

**Gaus mean : 36.9716**

**Gaus Width: 4.0334**

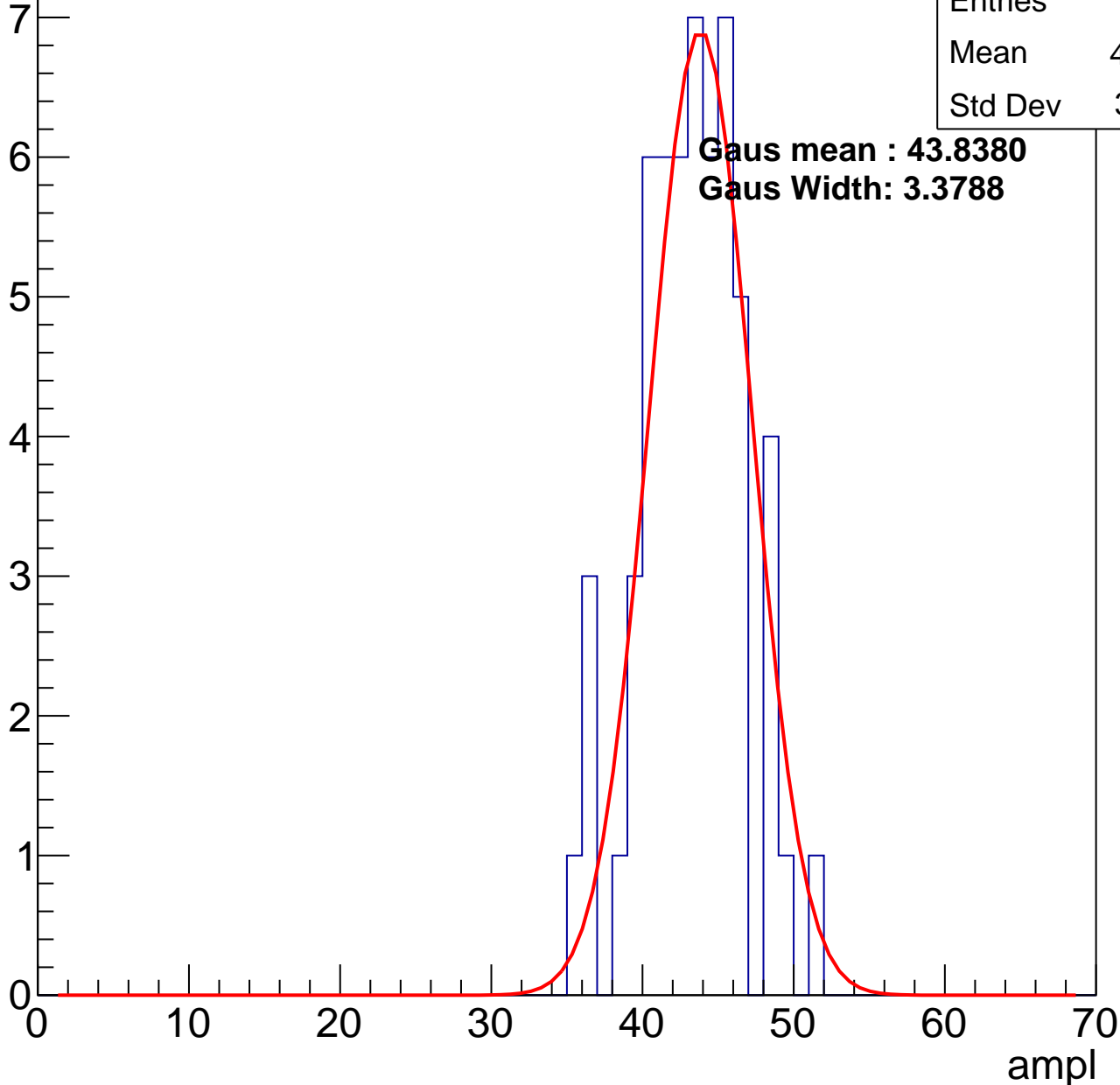


# B1L103S, U9-ch88, adc2

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	57
Mean	42.77
Std Dev	3.361

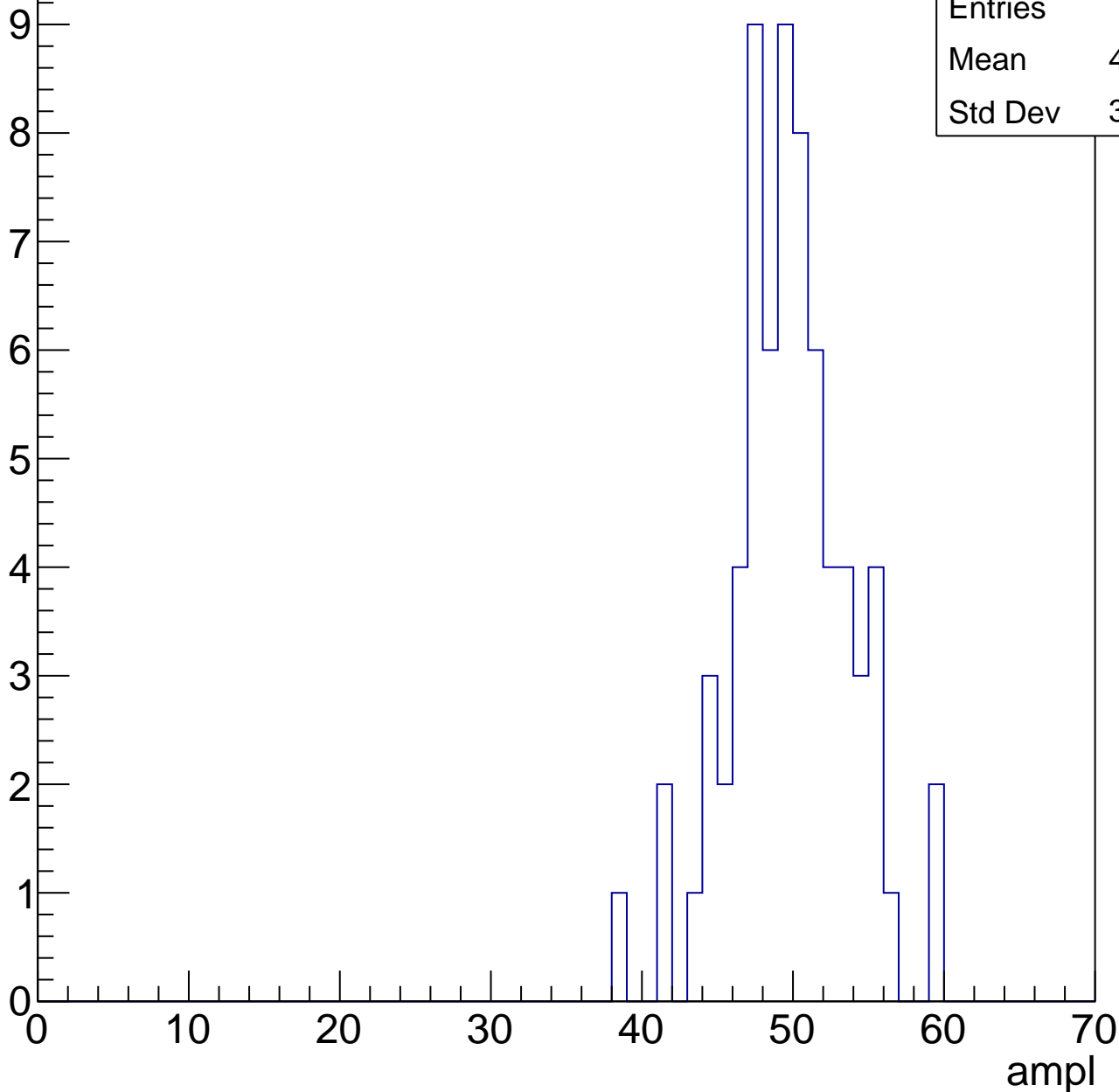


# B1L103S, U9-ch88, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

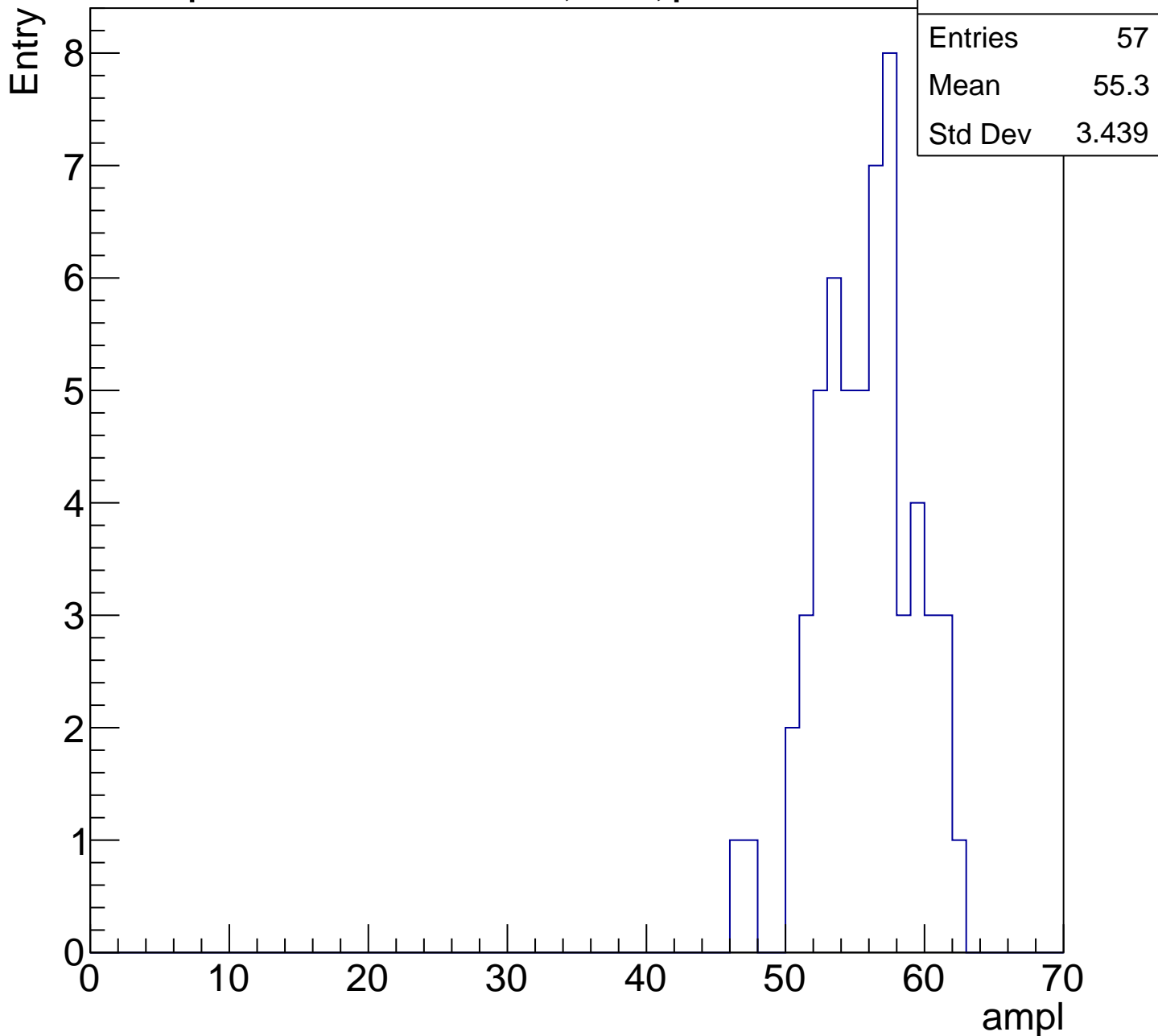
Entry

Entries	69
Mean	49.32
Std Dev	3.925



# B1L103S, U9-ch88, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

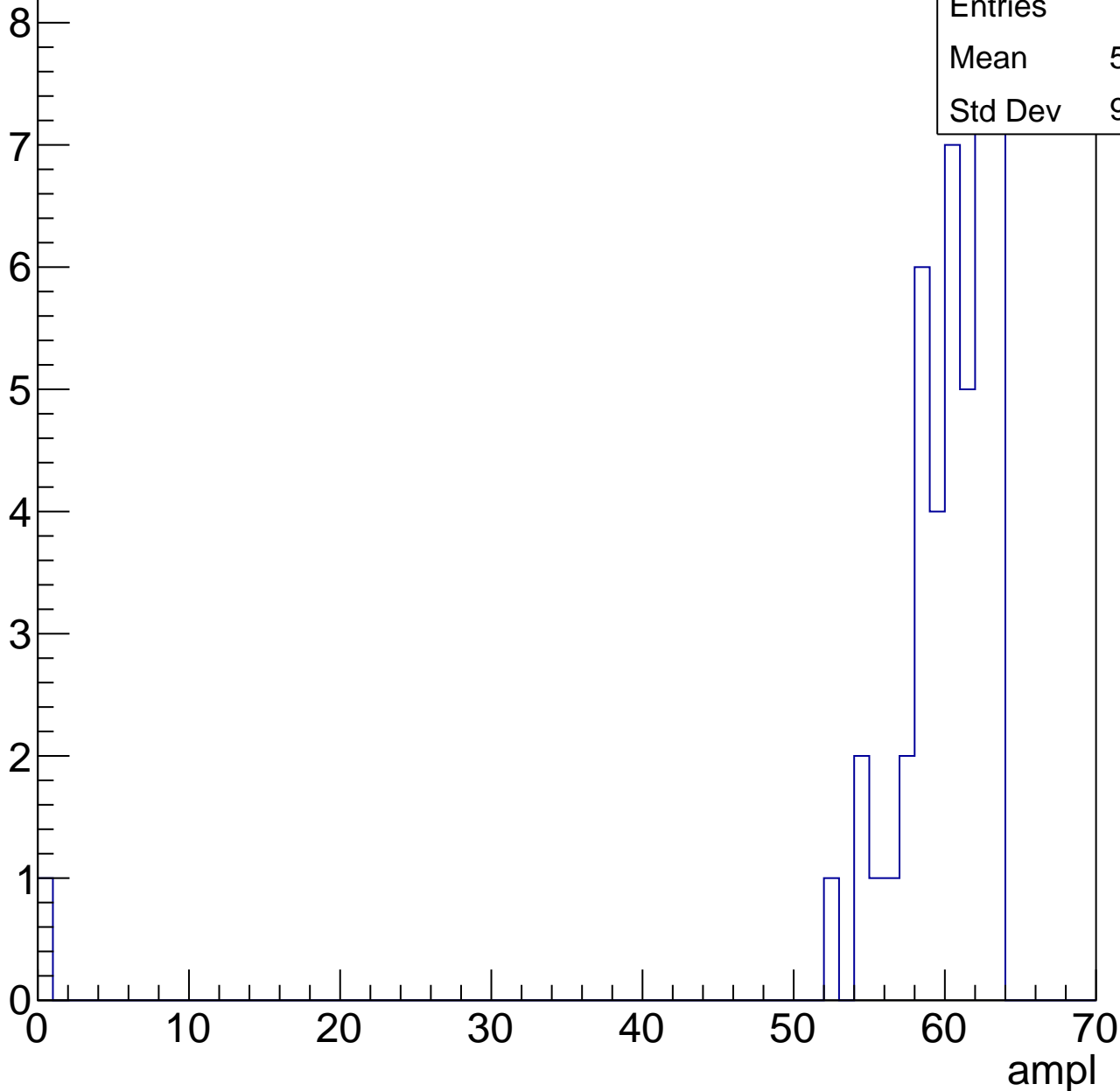


# B1L103S, U9-ch88, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	46
Mean	58.57
Std Dev	9.133



# B1L103S, U9-ch88, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

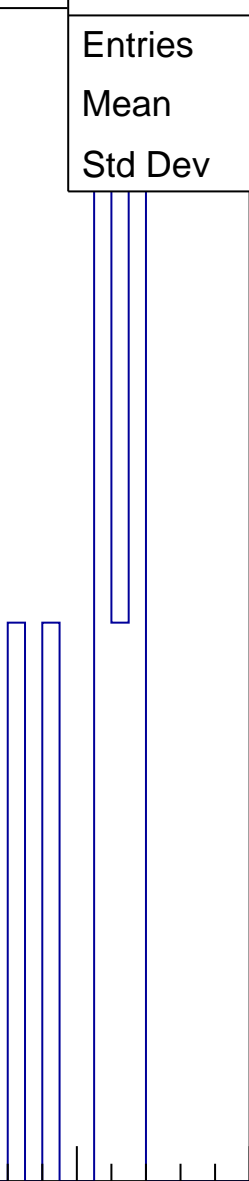
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	7
Mean	60.57
Std Dev	2.441

0 10 20 30 40 50 60 70

ampl





# B1L103S, U9-ch88, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U9-ch89, adc0

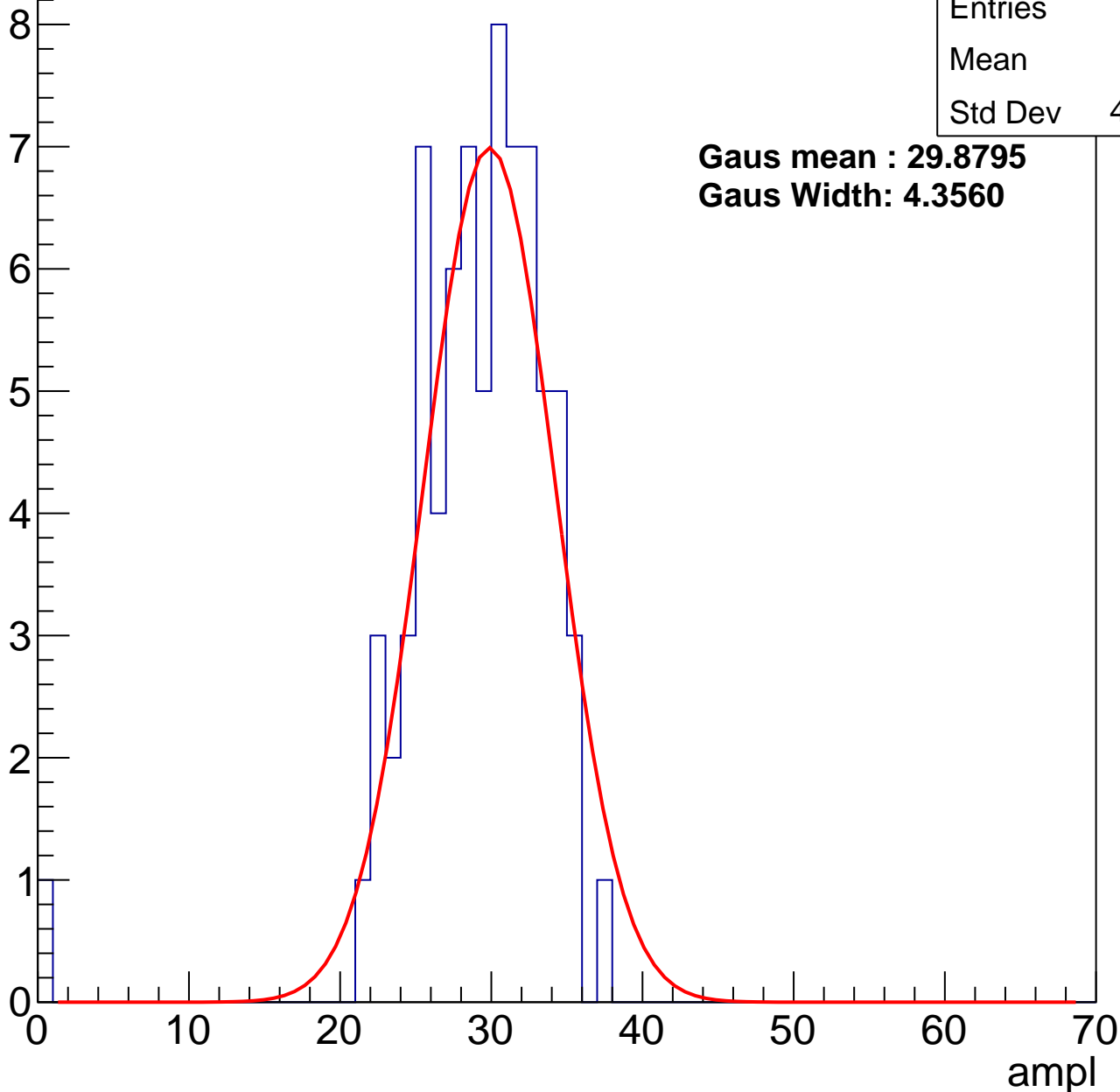
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	75
Mean	28.6
Std Dev	4.956

**Gaus mean : 29.8795**

**Gaus Width: 4.3560**



# B1L103S, U9-ch89, adc1

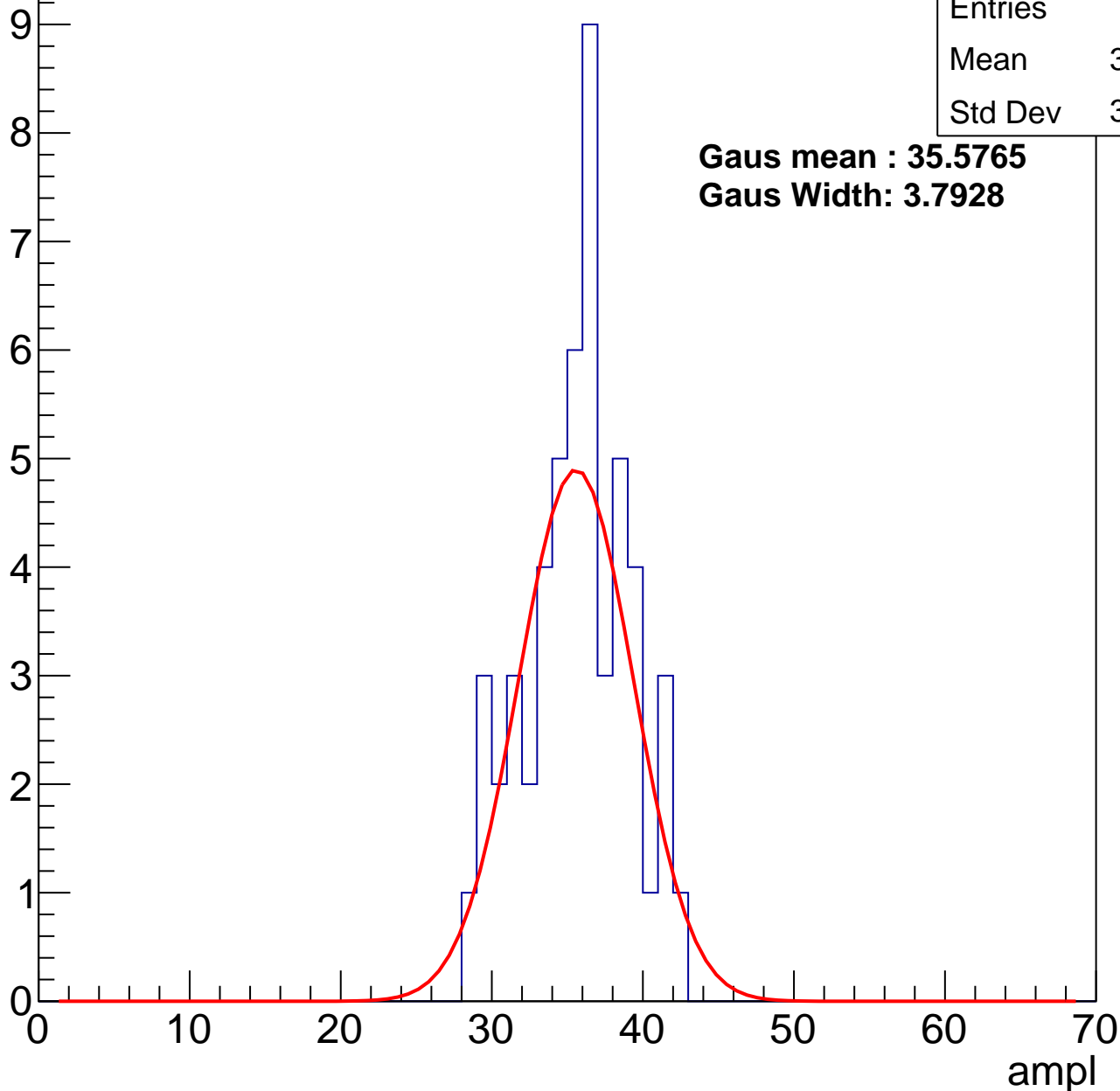
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	52
Mean	35.19
Std Dev	3.408

**Gaus mean : 35.5765**

**Gaus Width: 3.7928**



# B1L103S, U9-ch89, adc2

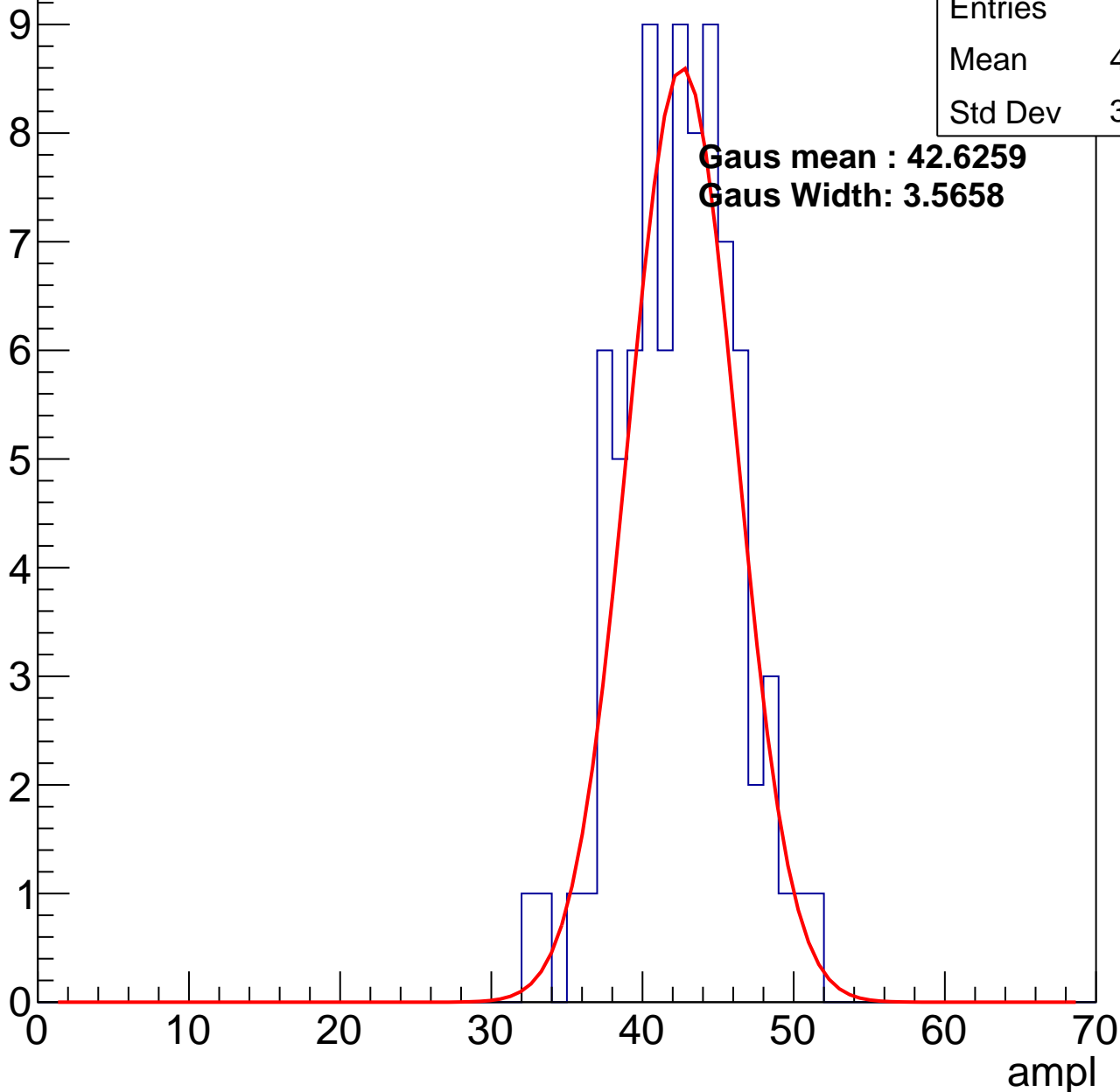
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	83
Mean	41.99
Std Dev	3.717

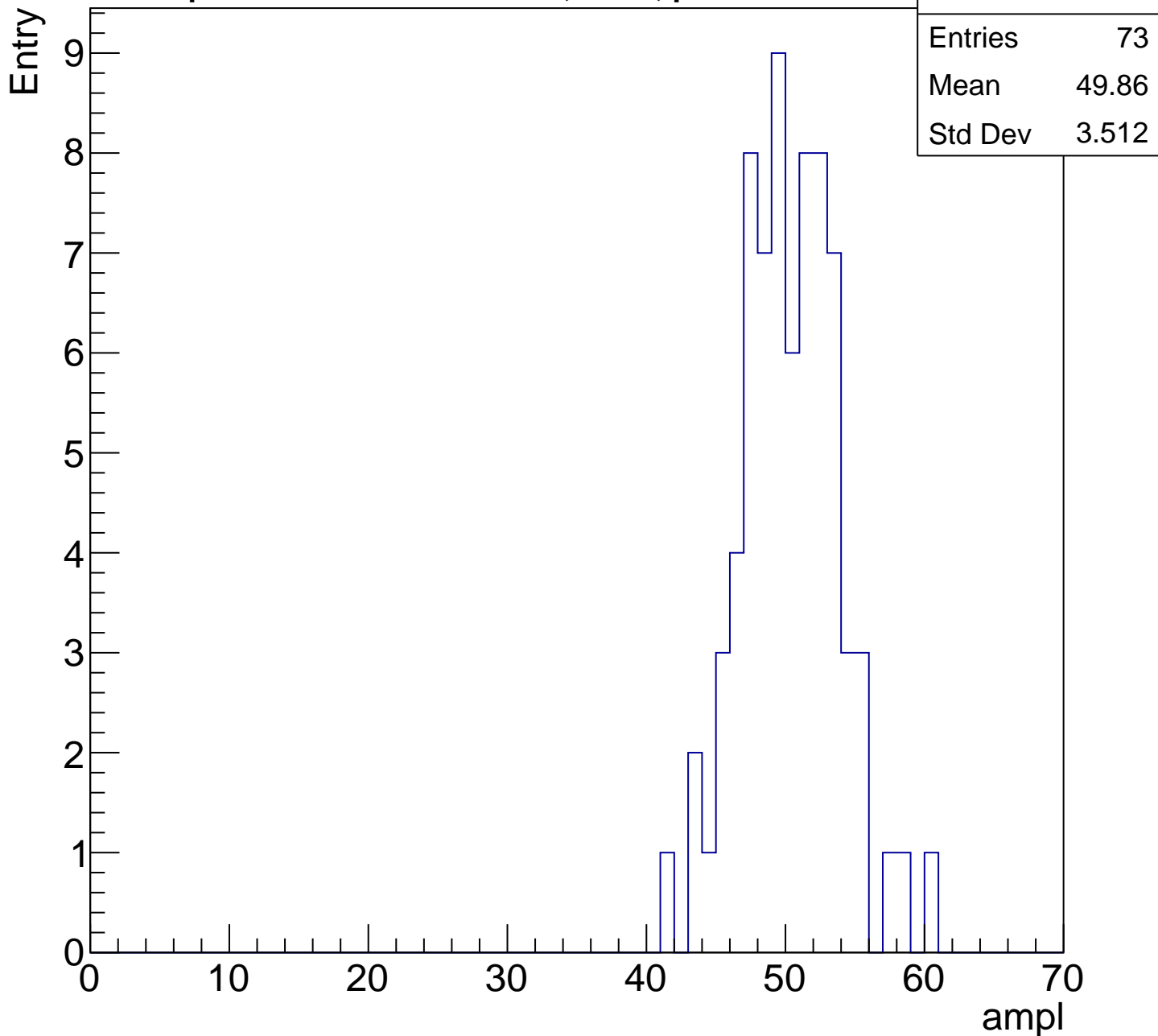
**Gaus mean : 42.6259**

**Gaus Width: 3.5658**



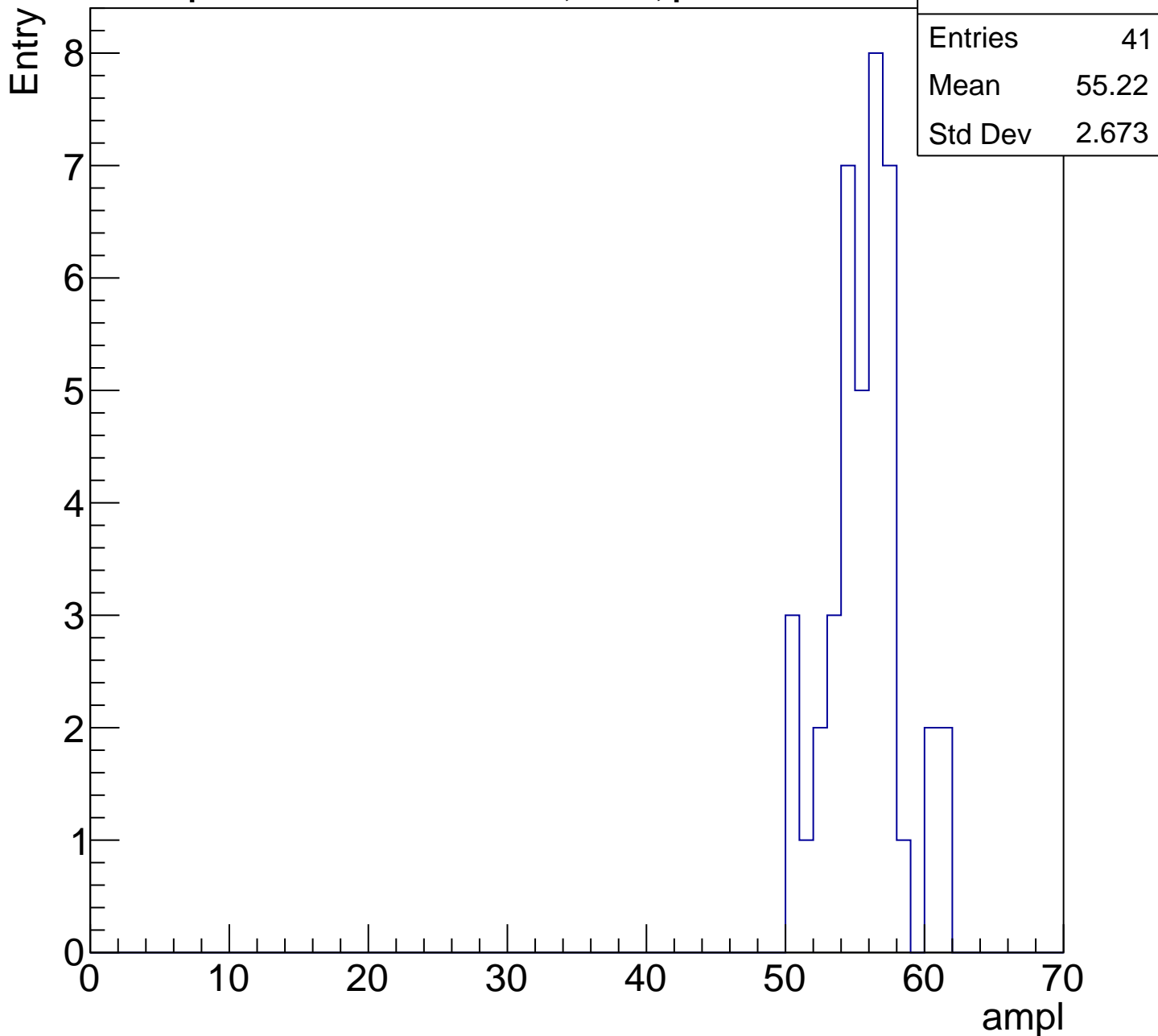
# B1L103S, U9-ch89, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U9-ch89, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

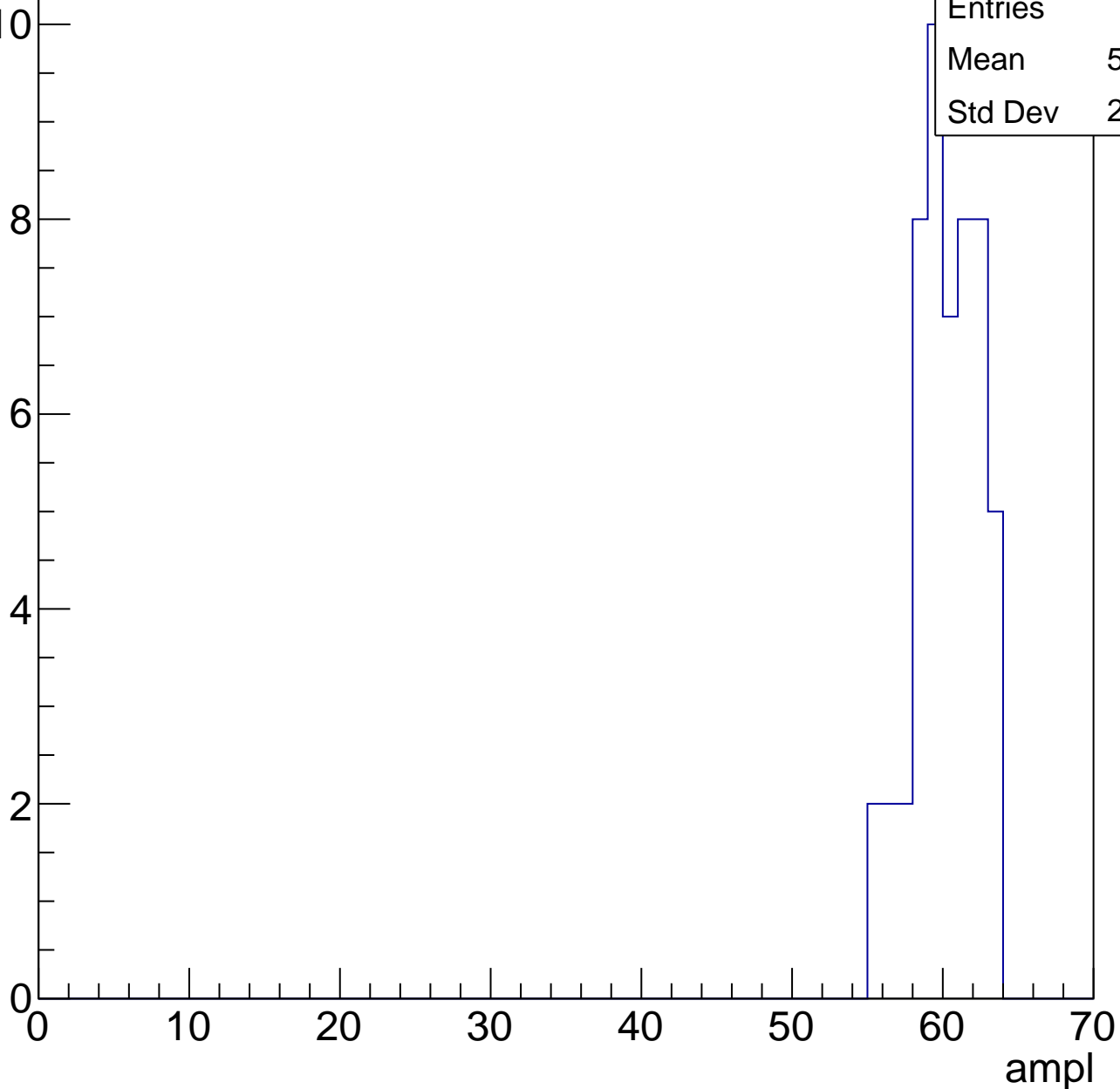


# B1L103S, U9-ch89, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	52
Mean	59.79
Std Dev	2.079

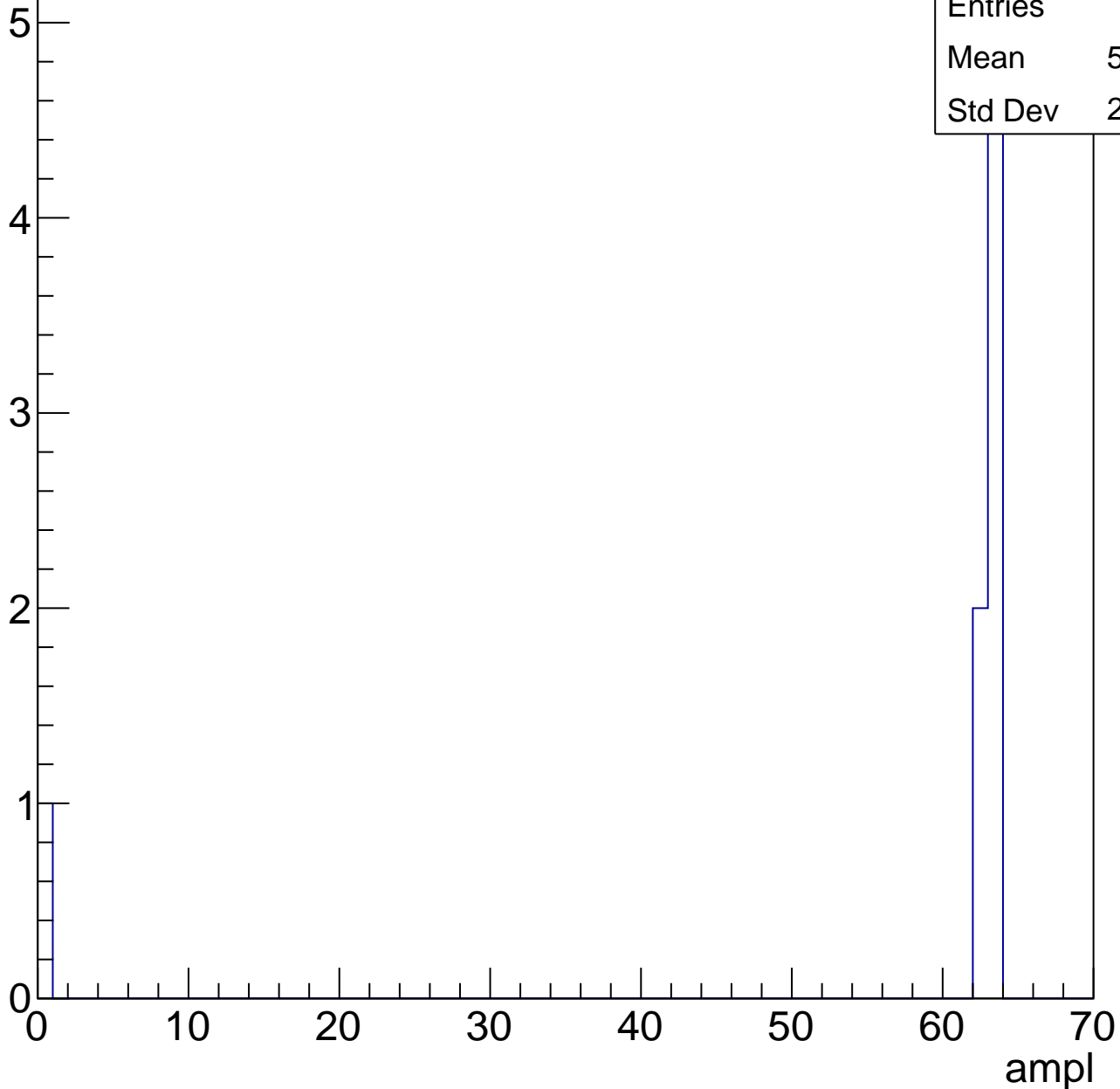


# B1L103S, U9-ch89, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	8
Mean	54.88
Std Dev	20.75





# B1L103S, U9-ch89, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U9-ch90, adc0

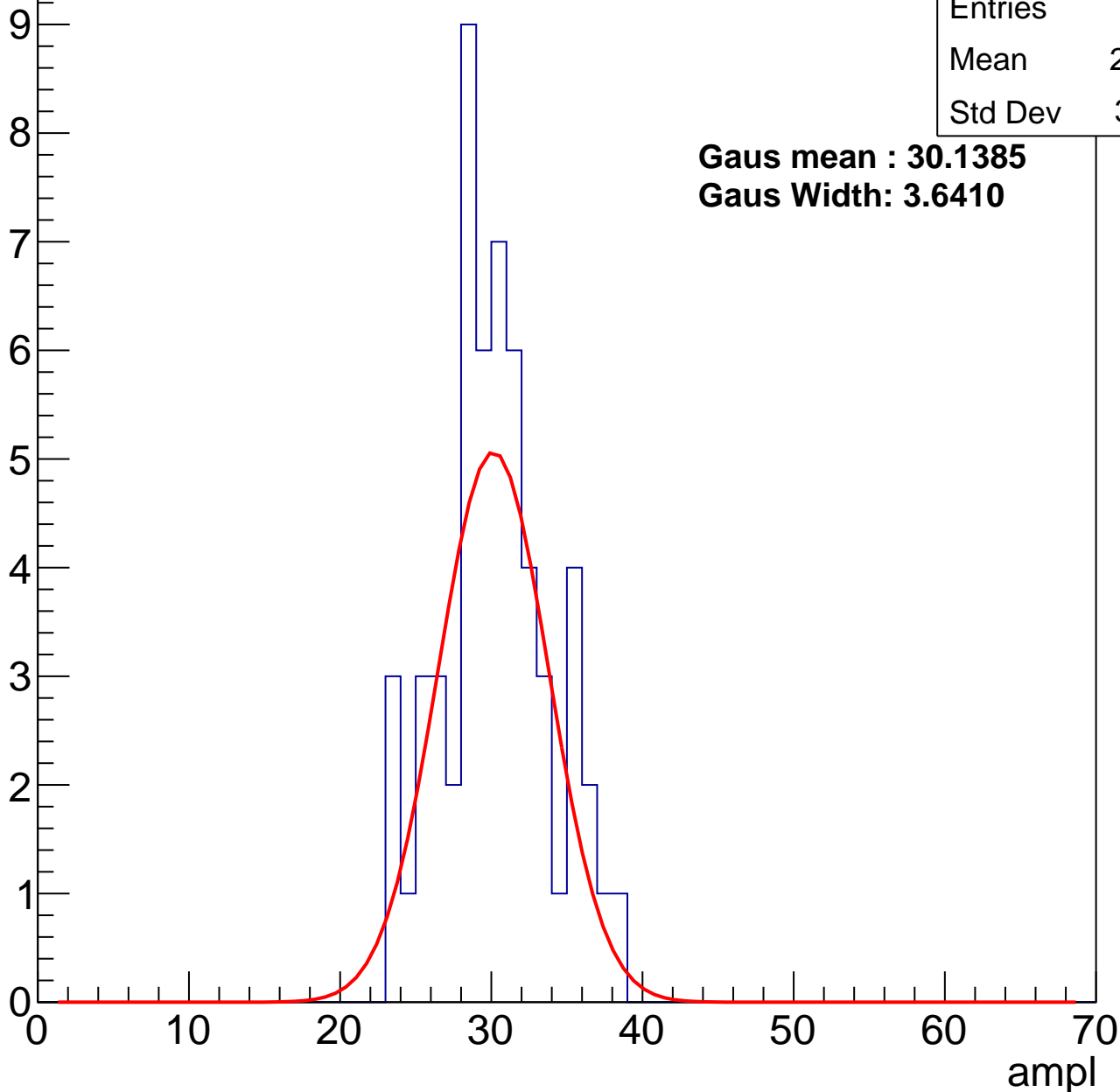
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	56
Mean	29.82
Std Dev	3.571

**Gaus mean : 30.1385**

**Gaus Width: 3.6410**



# B1L103S, U9-ch90, adc1

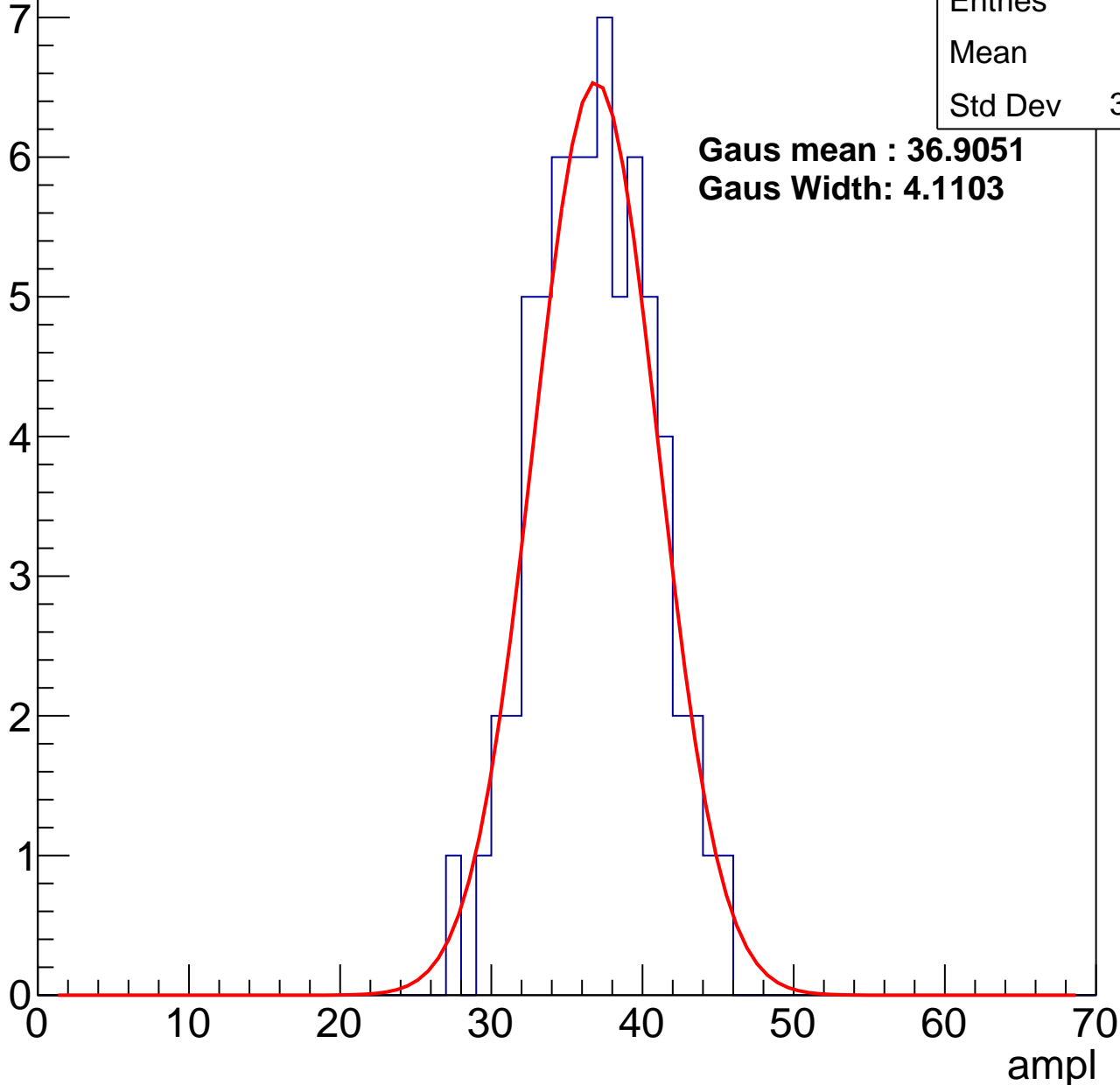
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	36.4
Std Dev	3.809

**Gaus mean : 36.9051**

**Gaus Width: 4.1103**



# B1L103S, U9-ch90, adc2

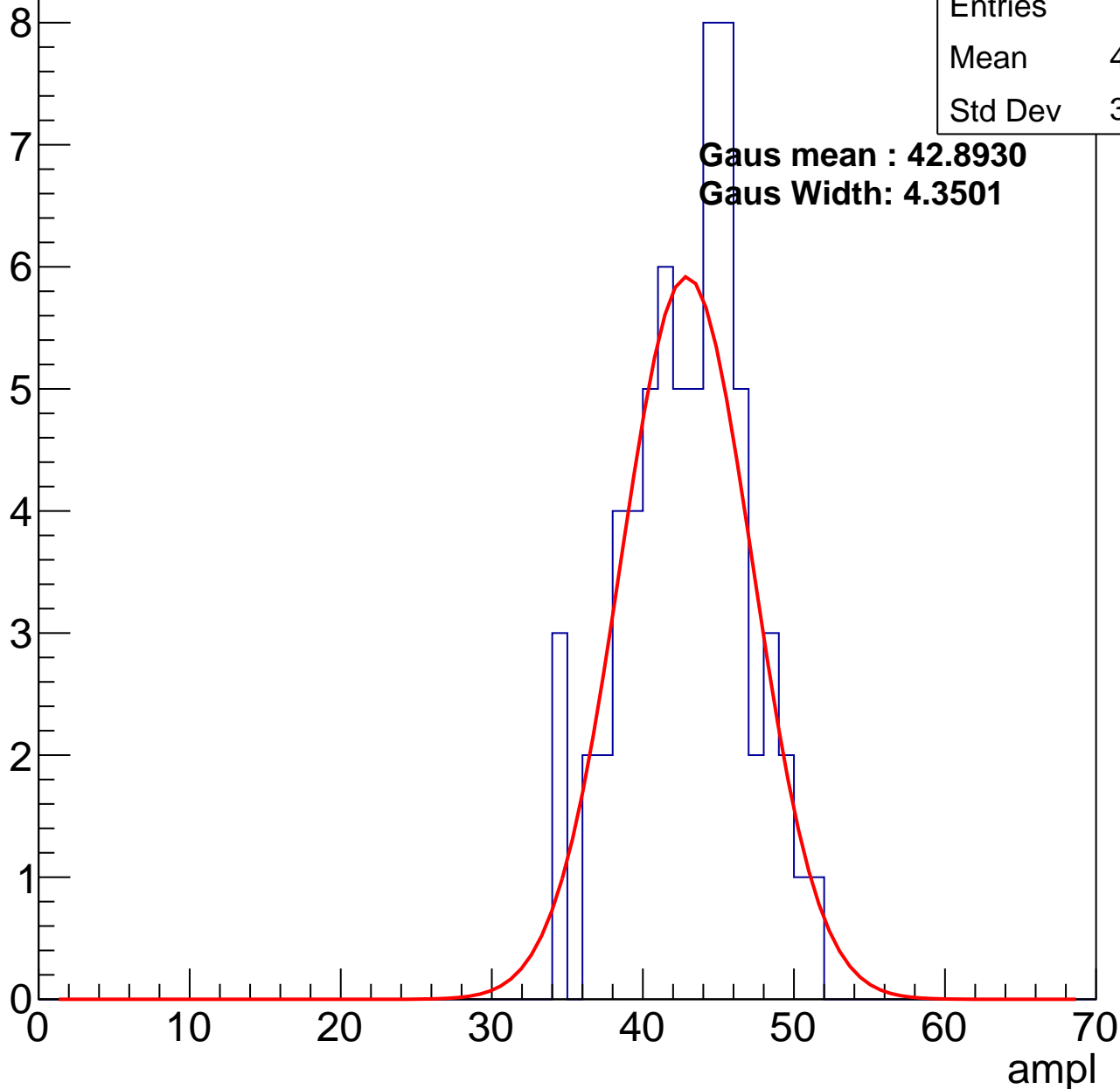
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	42.52
Std Dev	3.917

**Gaus mean : 42.8930**

**Gaus Width: 4.3501**

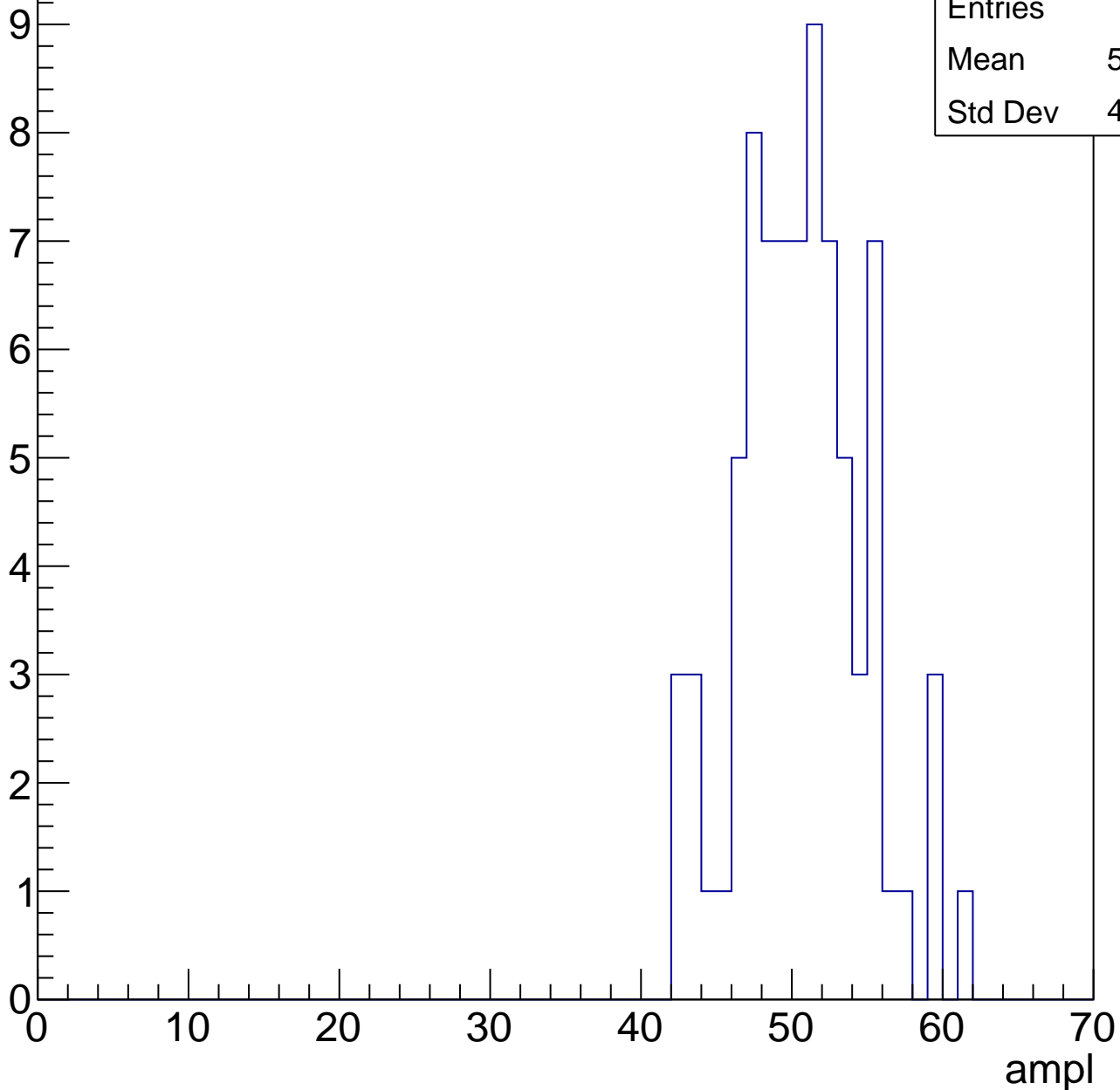


# B1L103S, U9-ch90, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

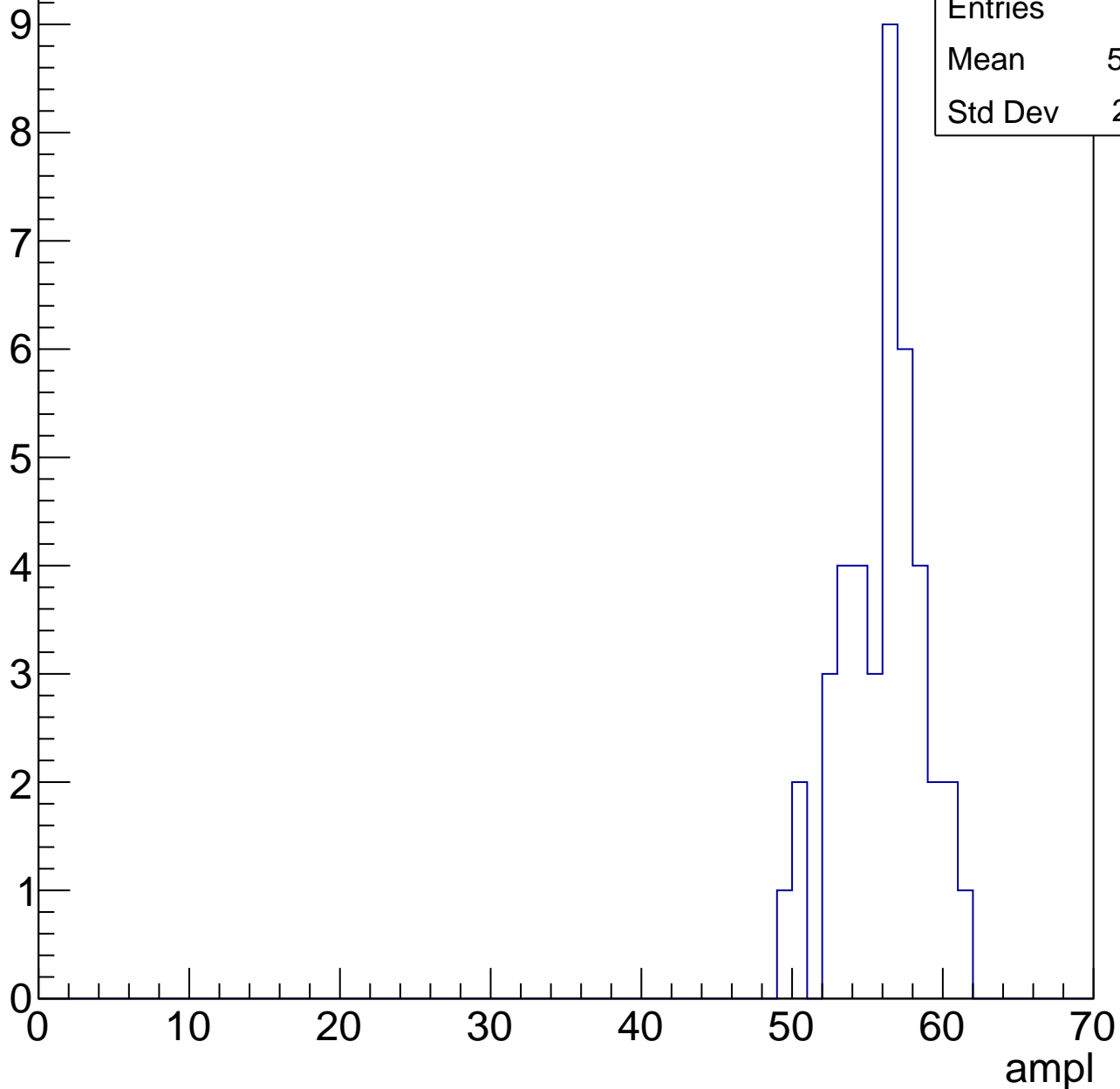
Entries	79
Mean	50.19
Std Dev	4.116



# B1L103S, U9-ch90, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U9-ch90, adc5

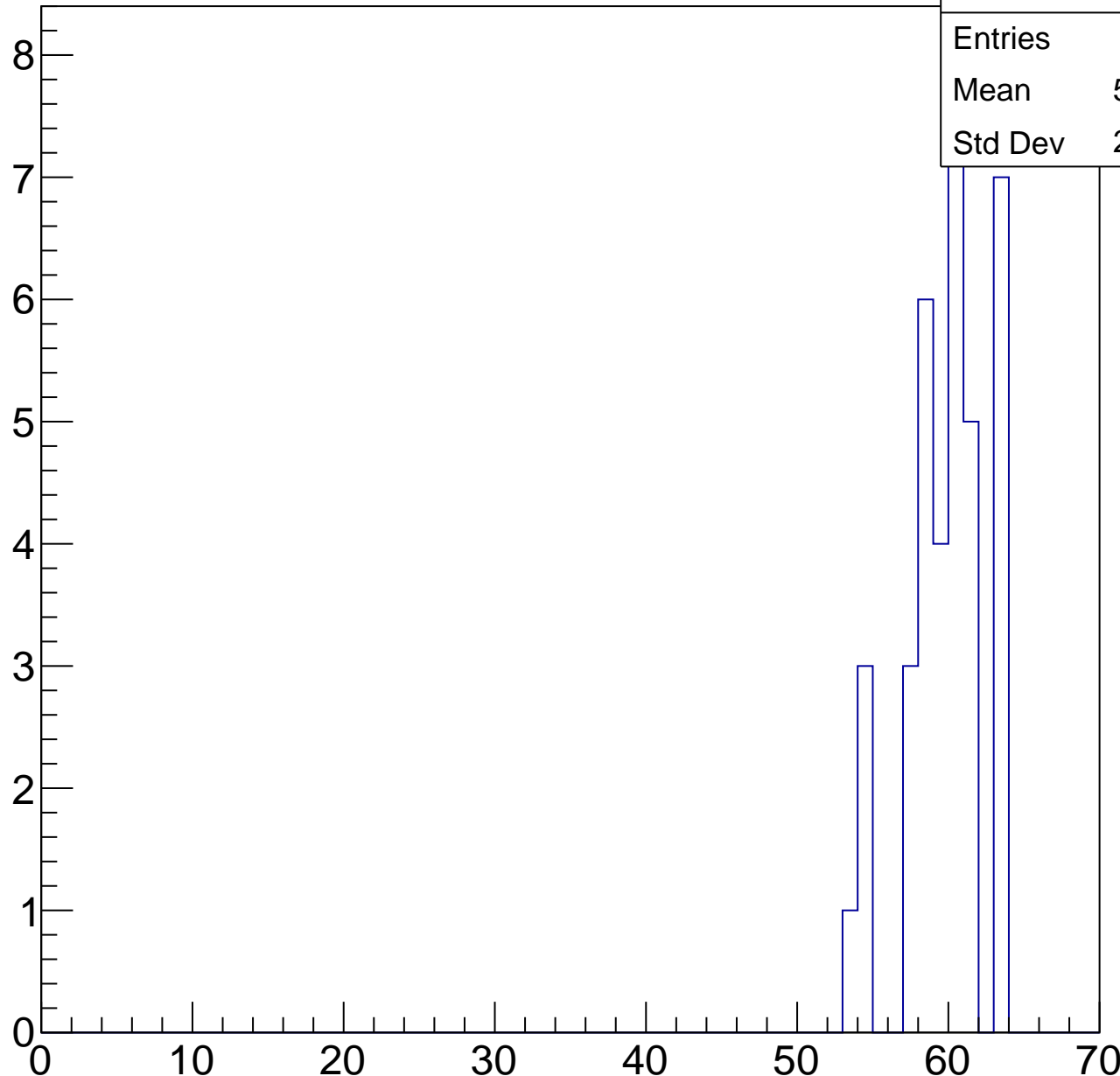
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	37
Mean	59.35
Std Dev	2.673

ampl

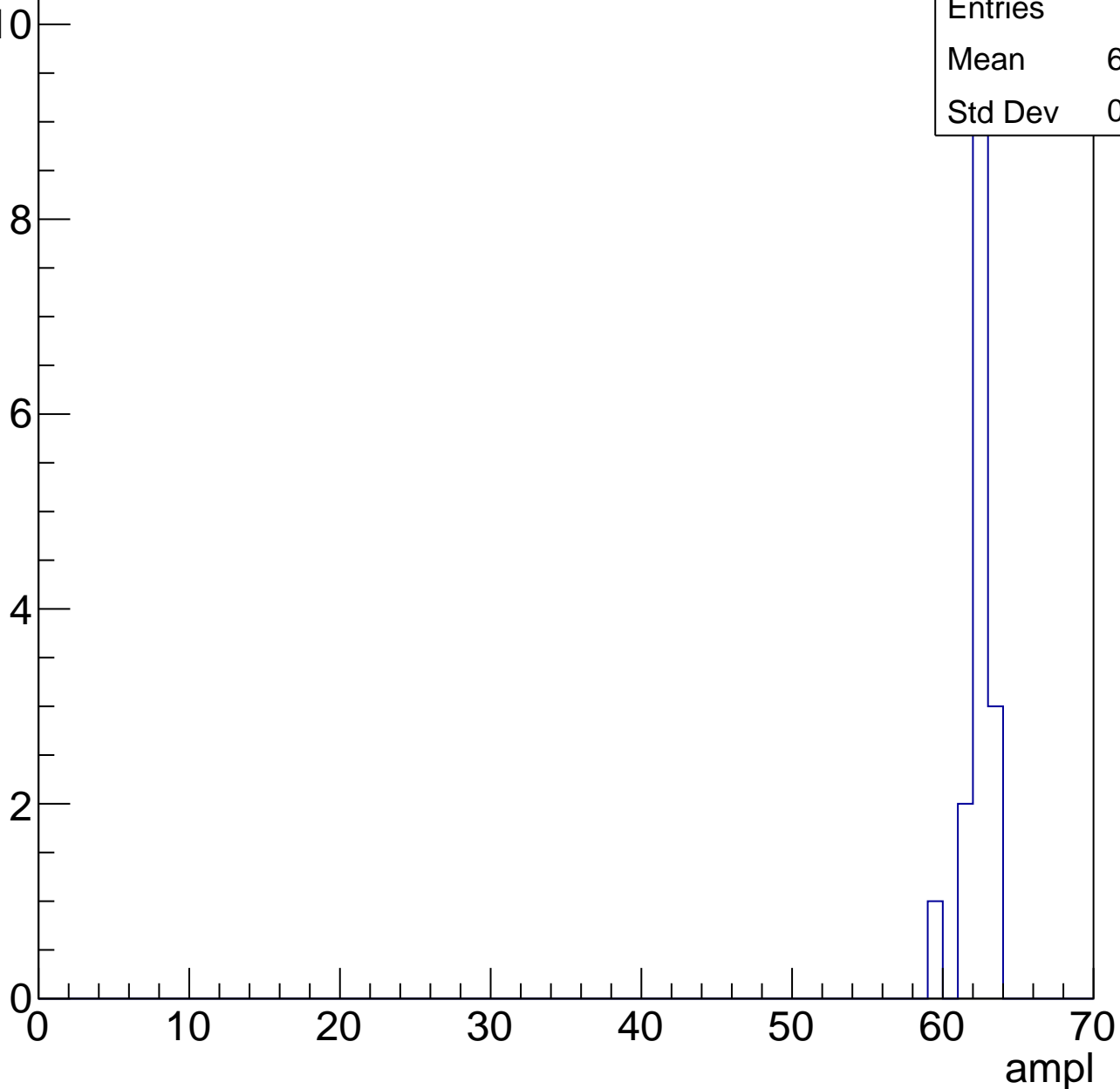


# B1L103S, U9-ch90, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	16
Mean	61.88
Std Dev	0.927

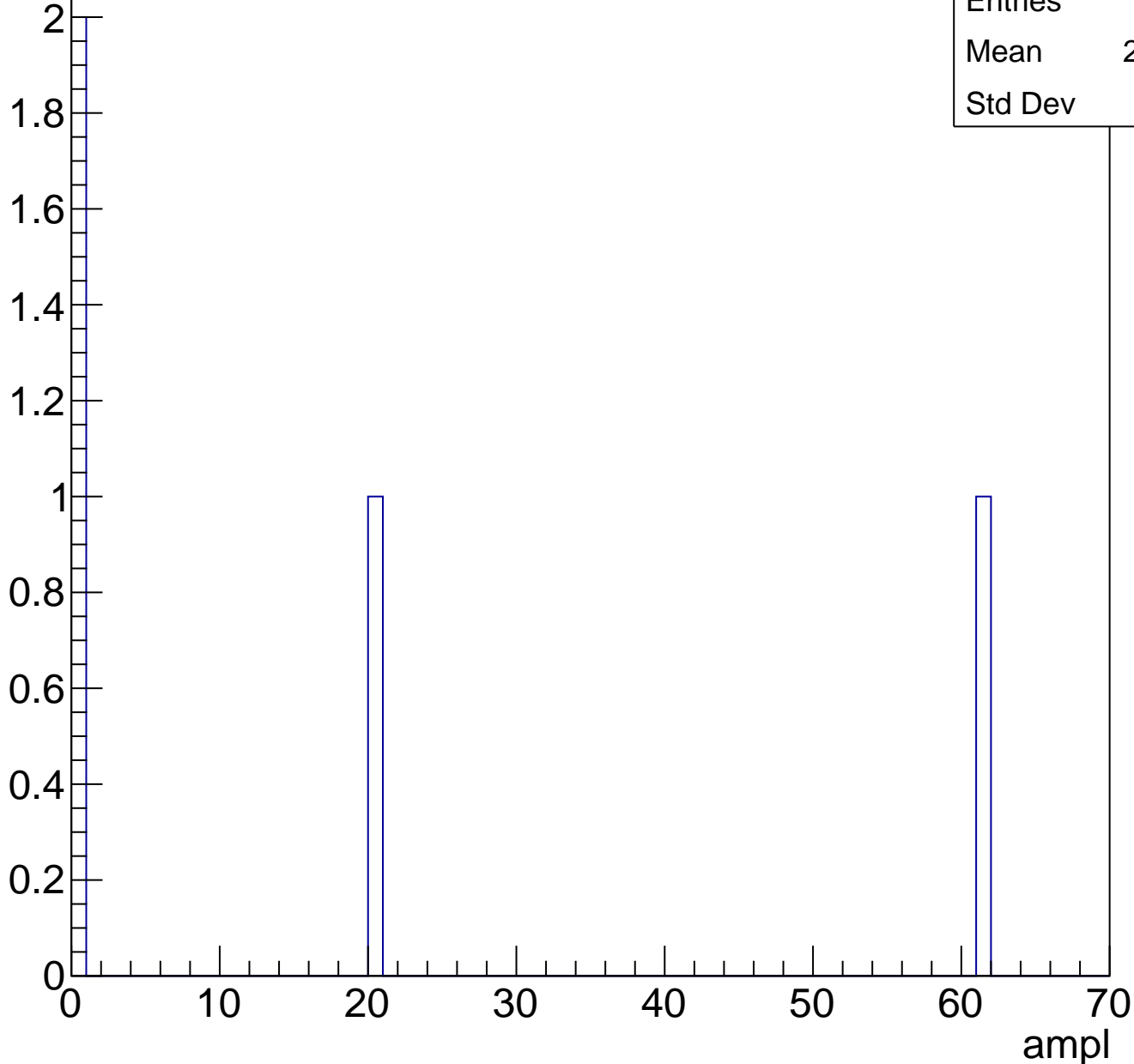




# B1L103S, U9-ch90, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	4
Mean	20.25
Std Dev	24.9

# B1L103S, U9-ch91, adc0

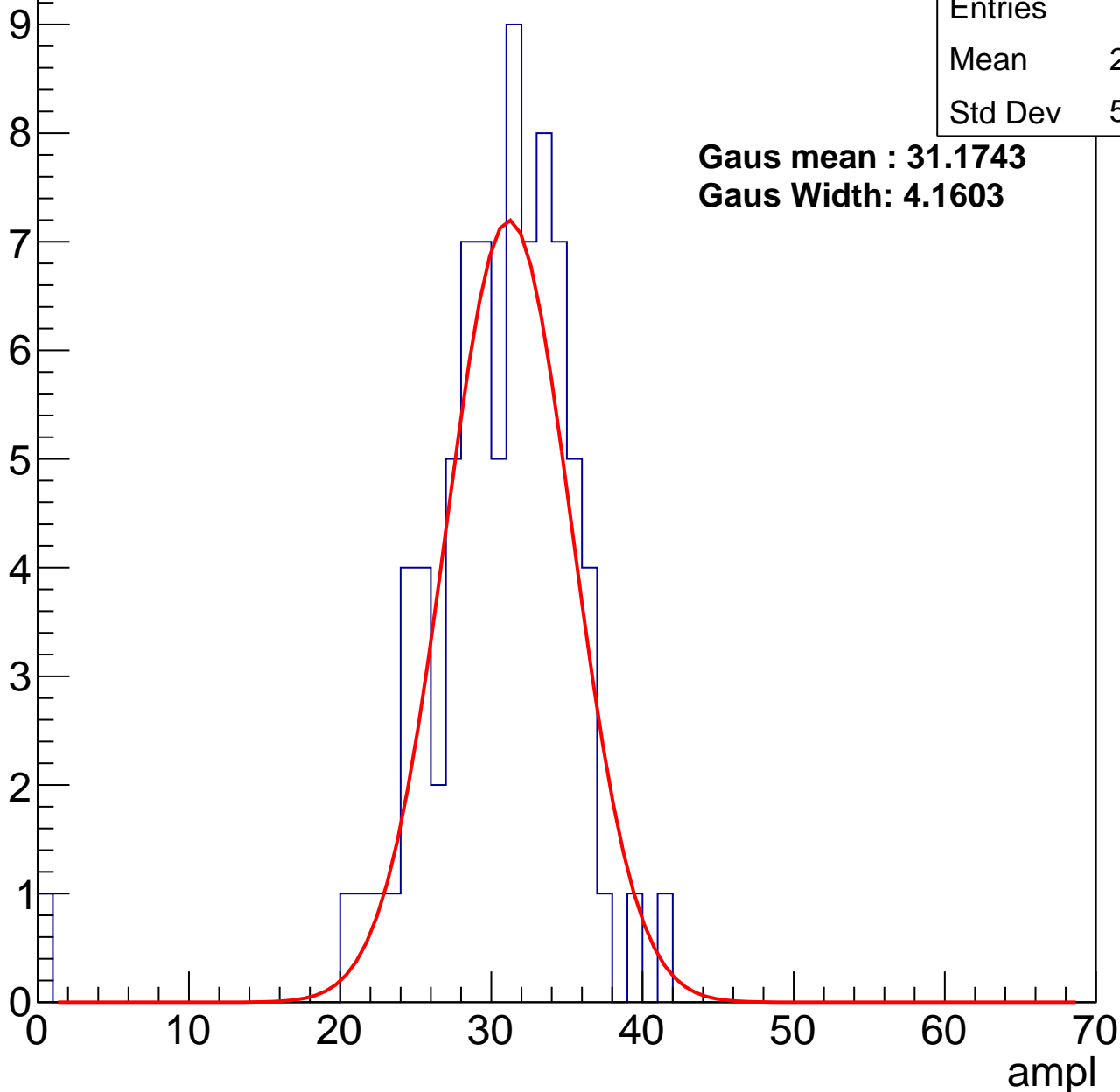
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	82
Mean	29.99
Std Dev	5.286

**Gaus mean : 31.1743**

**Gaus Width: 4.1603**



# B1L103S, U9-ch91, adc1

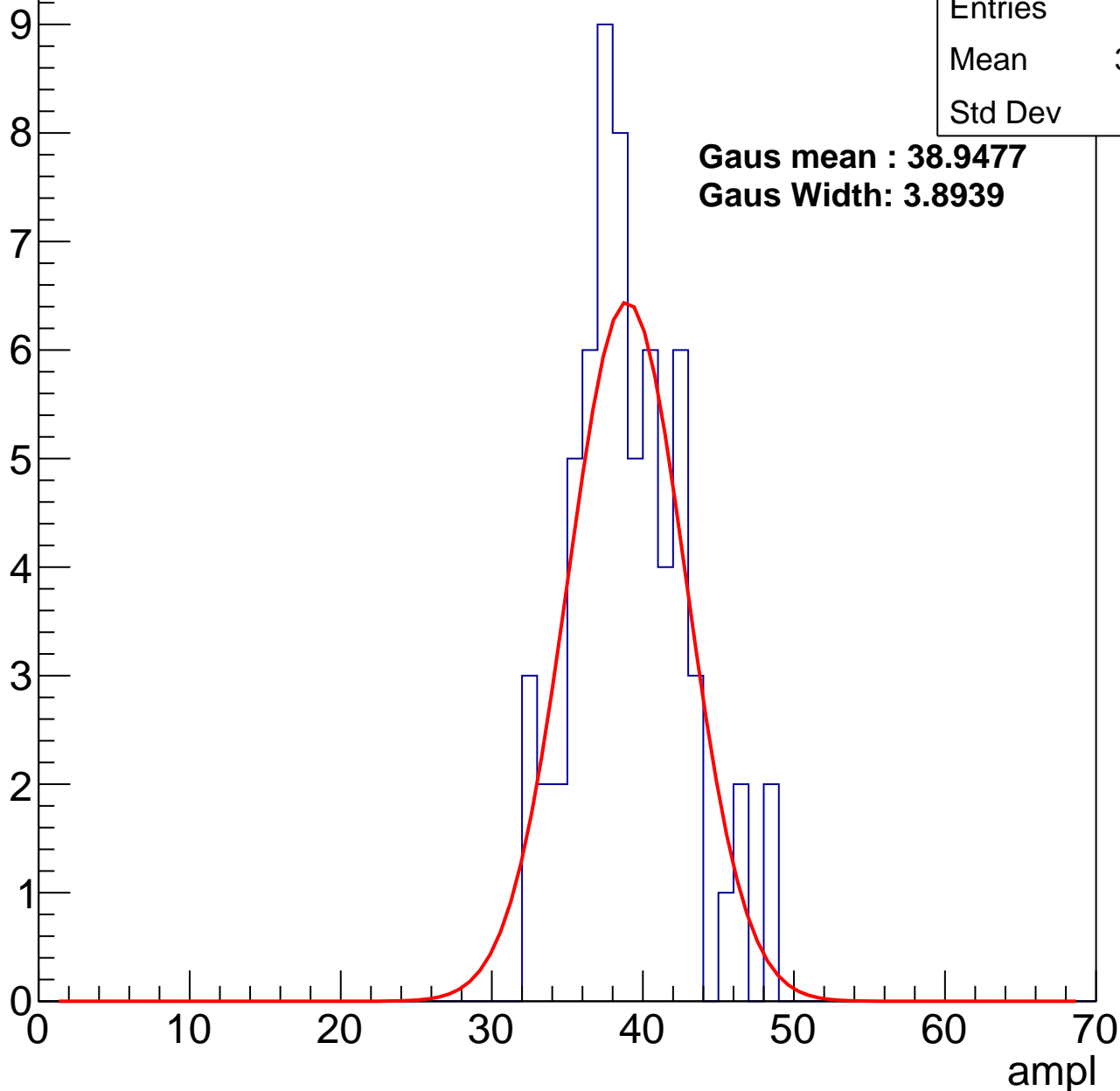
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	38.61
Std Dev	3.66

**Gaus mean : 38.9477**

**Gaus Width: 3.8939**



# B1L103S, U9-ch91, adc2

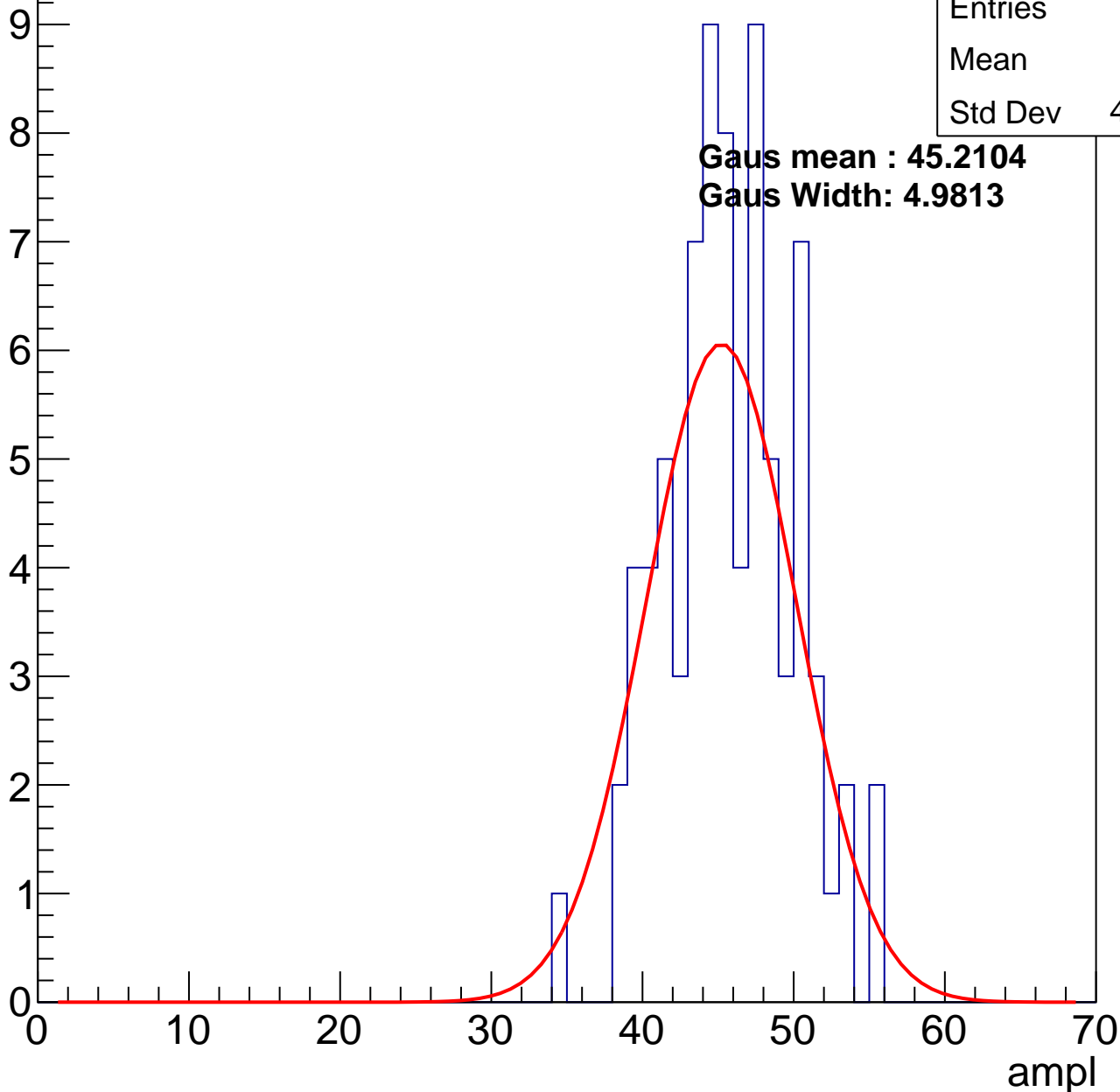
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	79
Mean	45.3
Std Dev	4.199

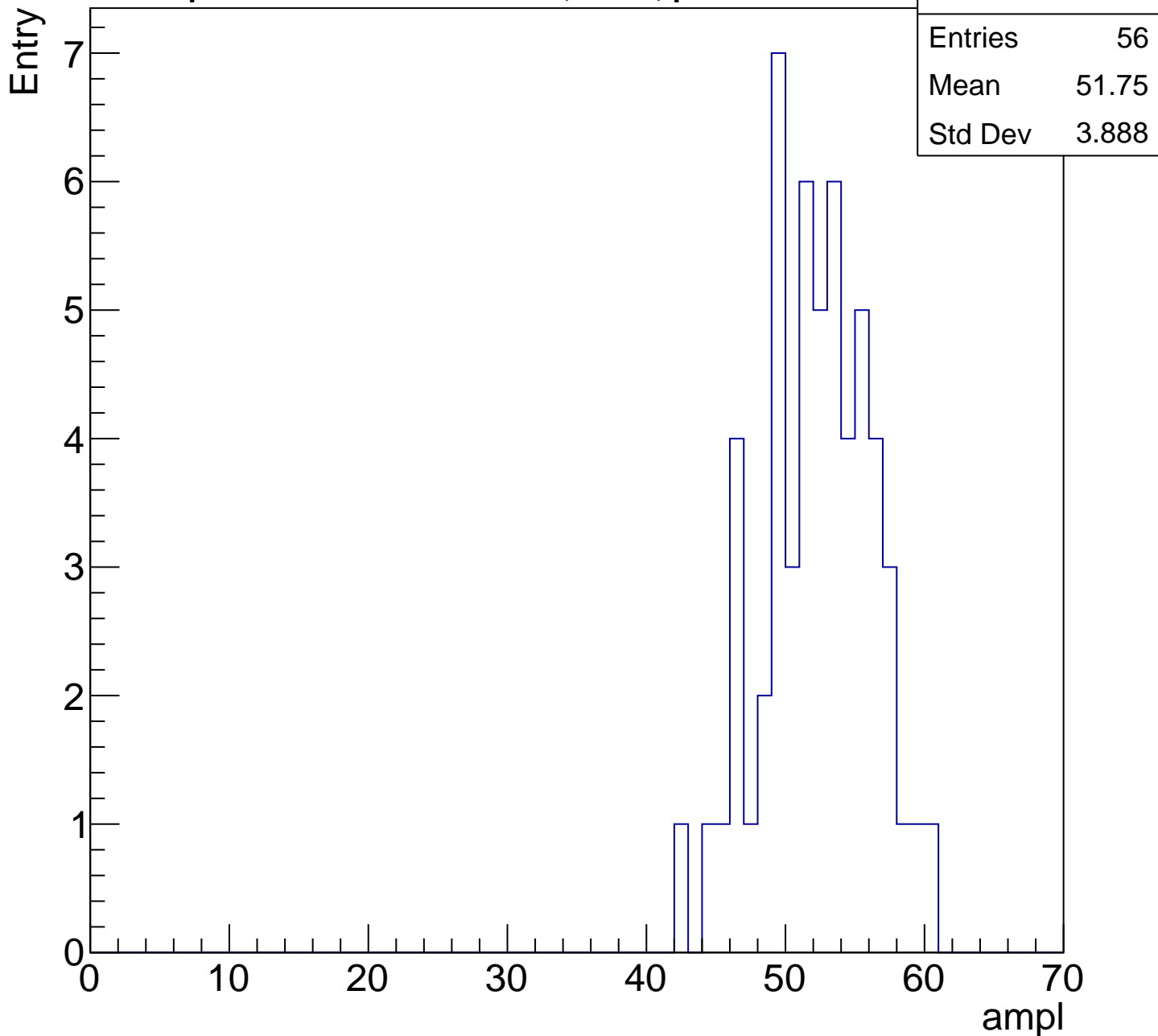
**Gaus mean : 45.2104**

**Gaus Width: 4.9813**



# B1L103S, U9-ch91, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

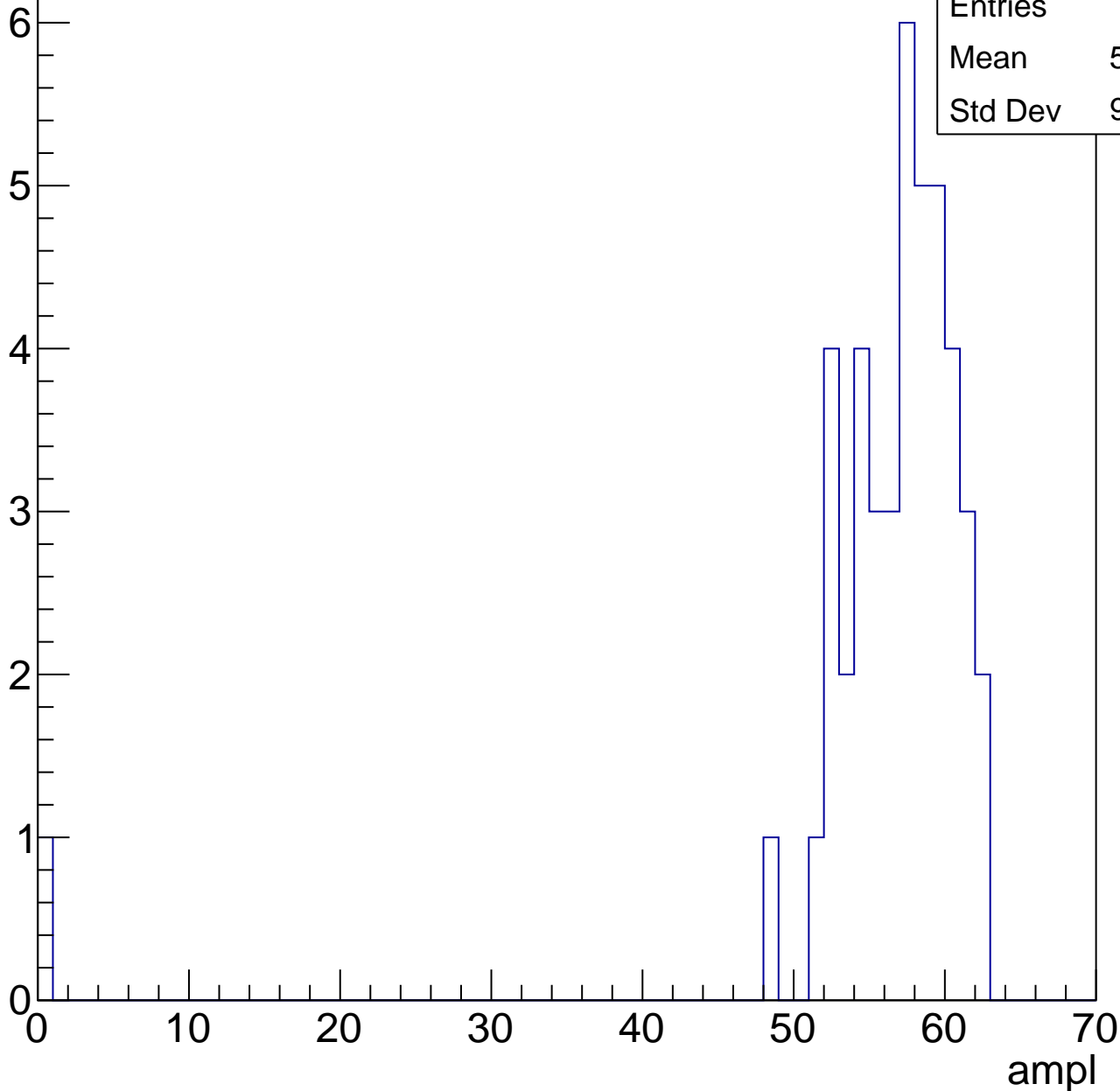


# B1L103S, U9-ch91, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	44
Mean	55.36
Std Dev	9.033

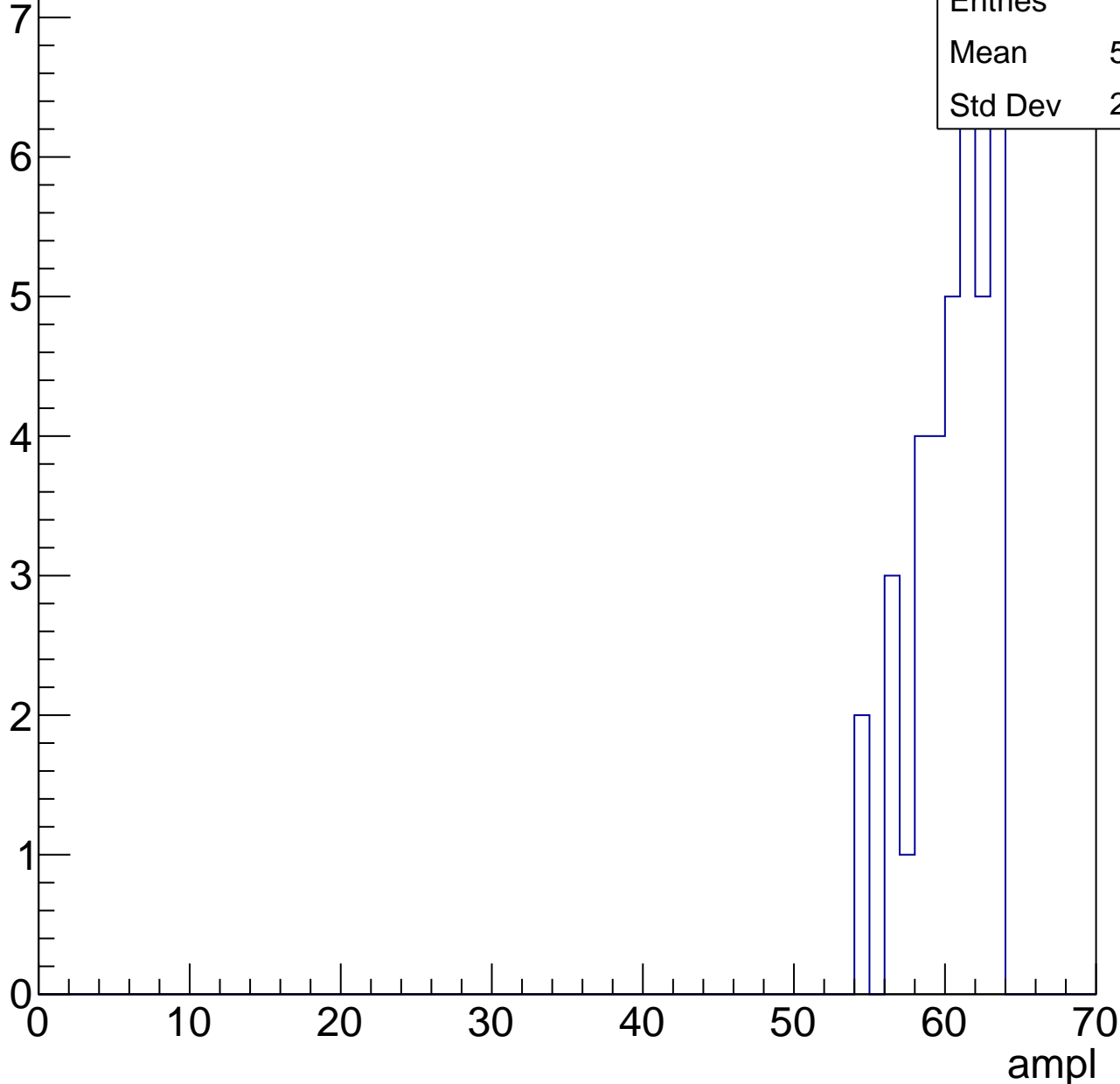


# B1L103S, U9-ch91, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	38
Mean	59.97
Std Dev	2.508



# B1L103S, U9-ch91, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U9-ch91, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U9-ch92, adc0

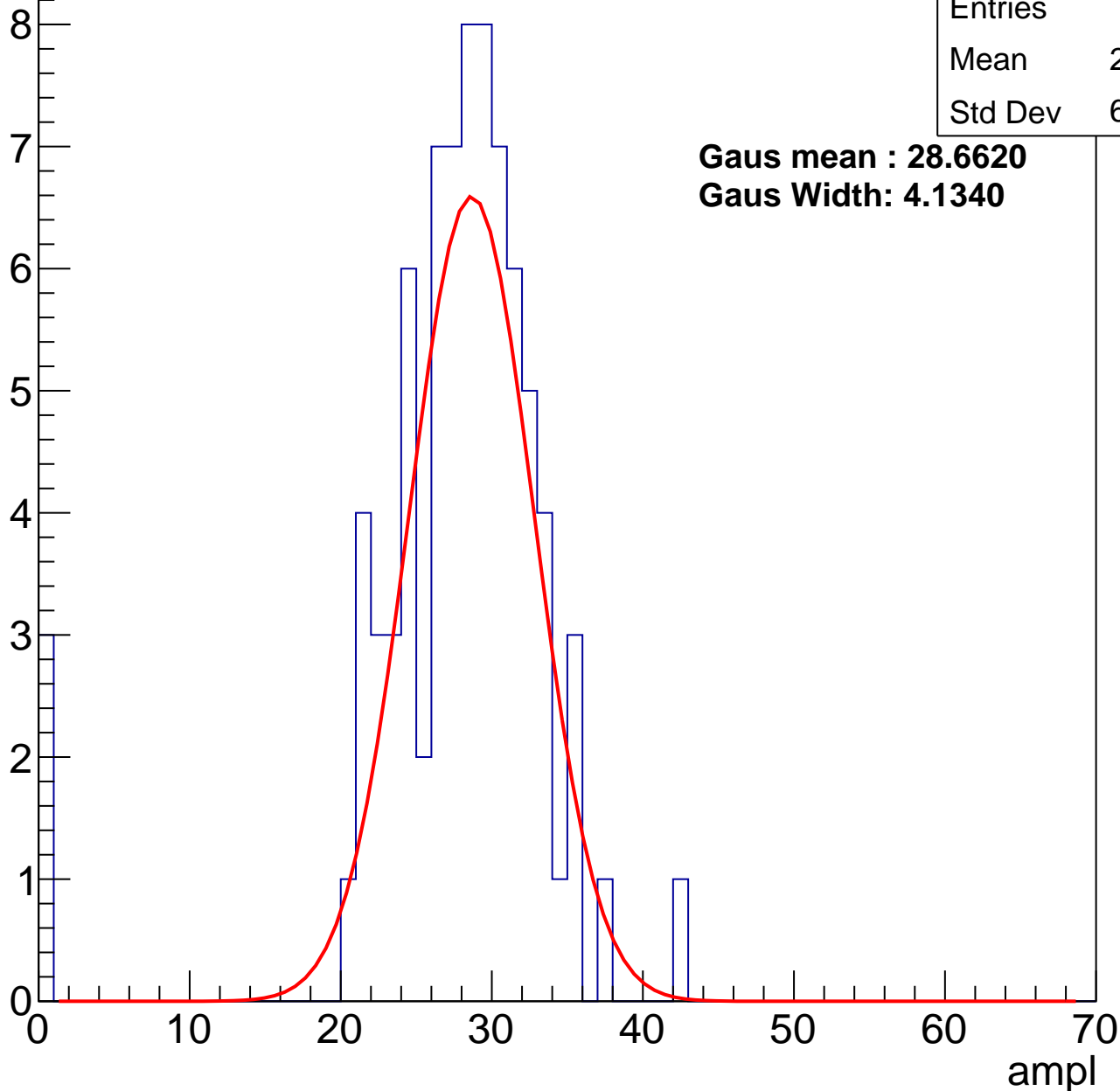
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	80
Mean	27.07
Std Dev	6.713

**Gaus mean : 28.6620**

**Gaus Width: 4.1340**



# B1L103S, U9-ch92, adc1

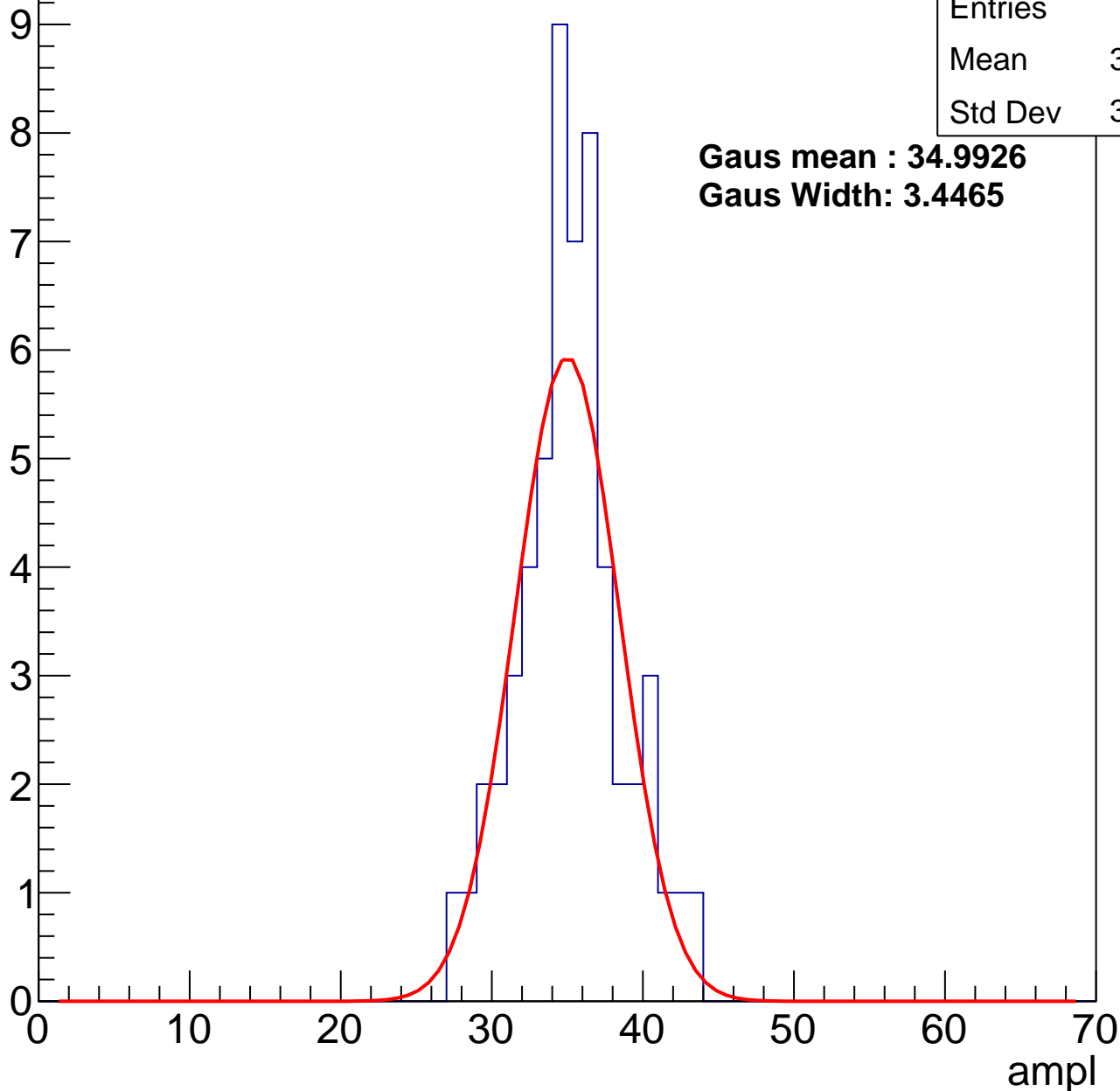
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	56
Mean	34.75
Std Dev	3.387

**Gaus mean : 34.9926**

**Gaus Width: 3.4465**



# B1L103S, U9-ch92, adc2

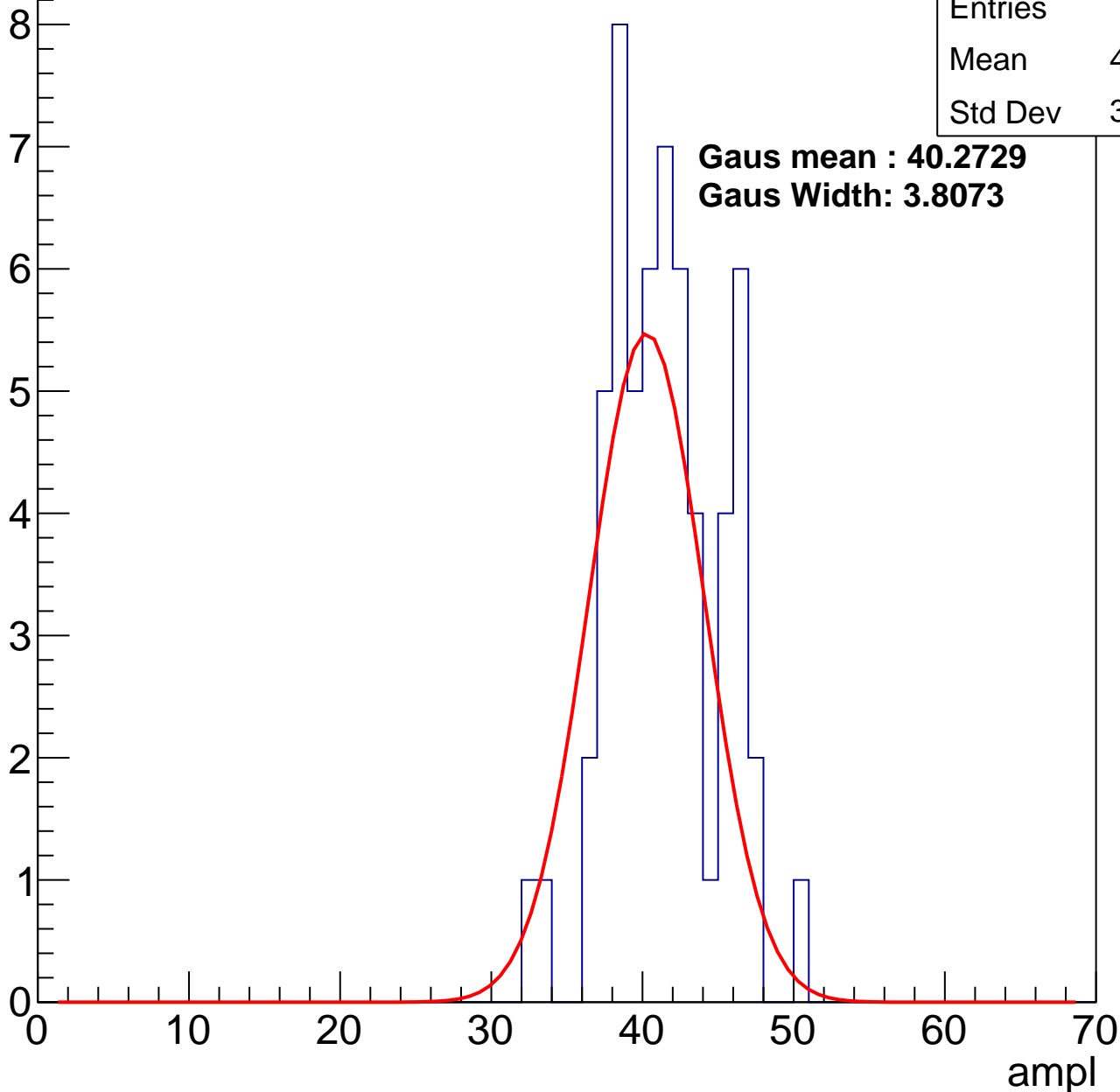
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	59
Mean	40.95
Std Dev	3.615

**Gaus mean : 40.2729**

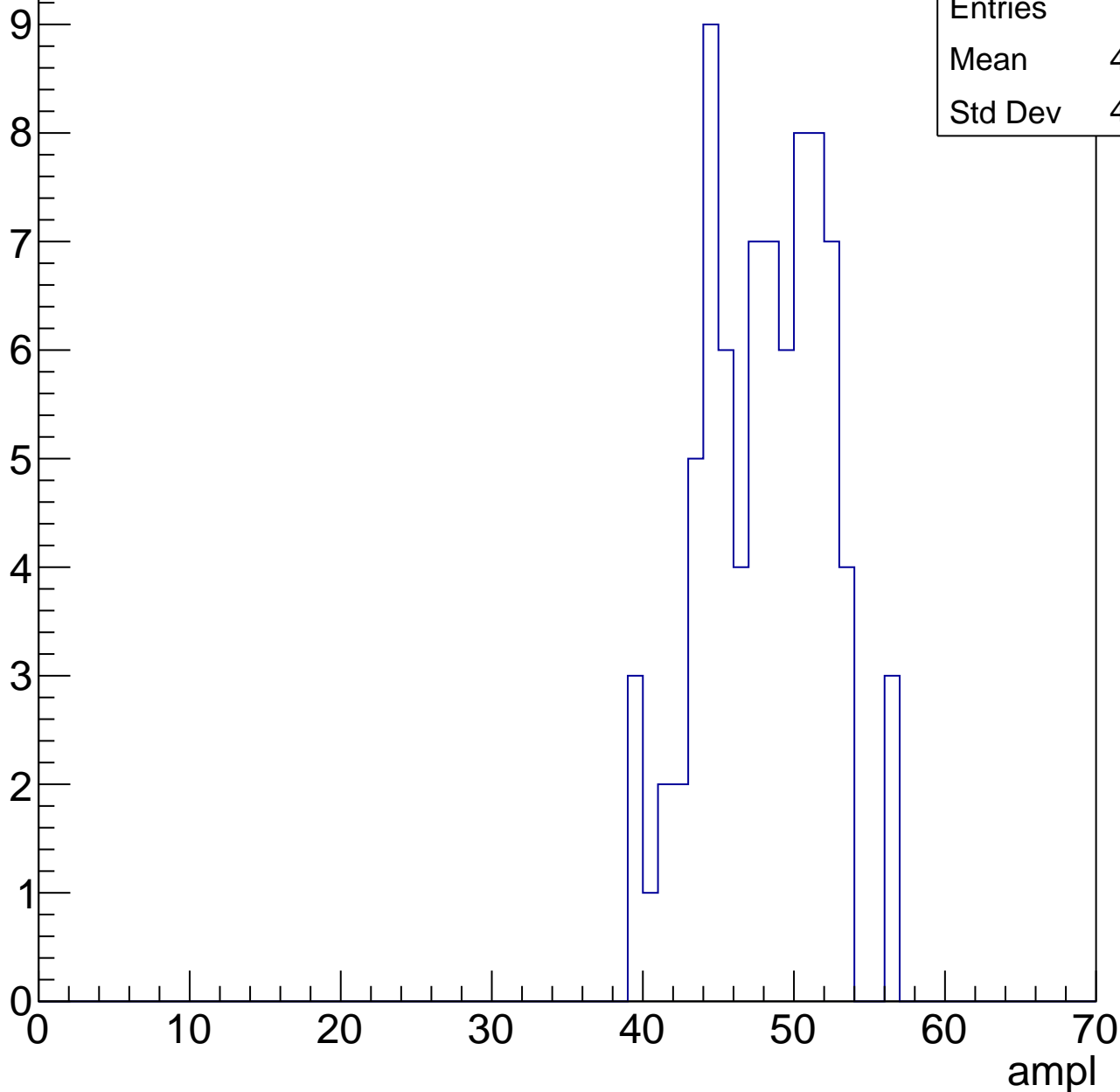
**Gaus Width: 3.8073**



# B1L103S, U9-ch92, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U9-ch92, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

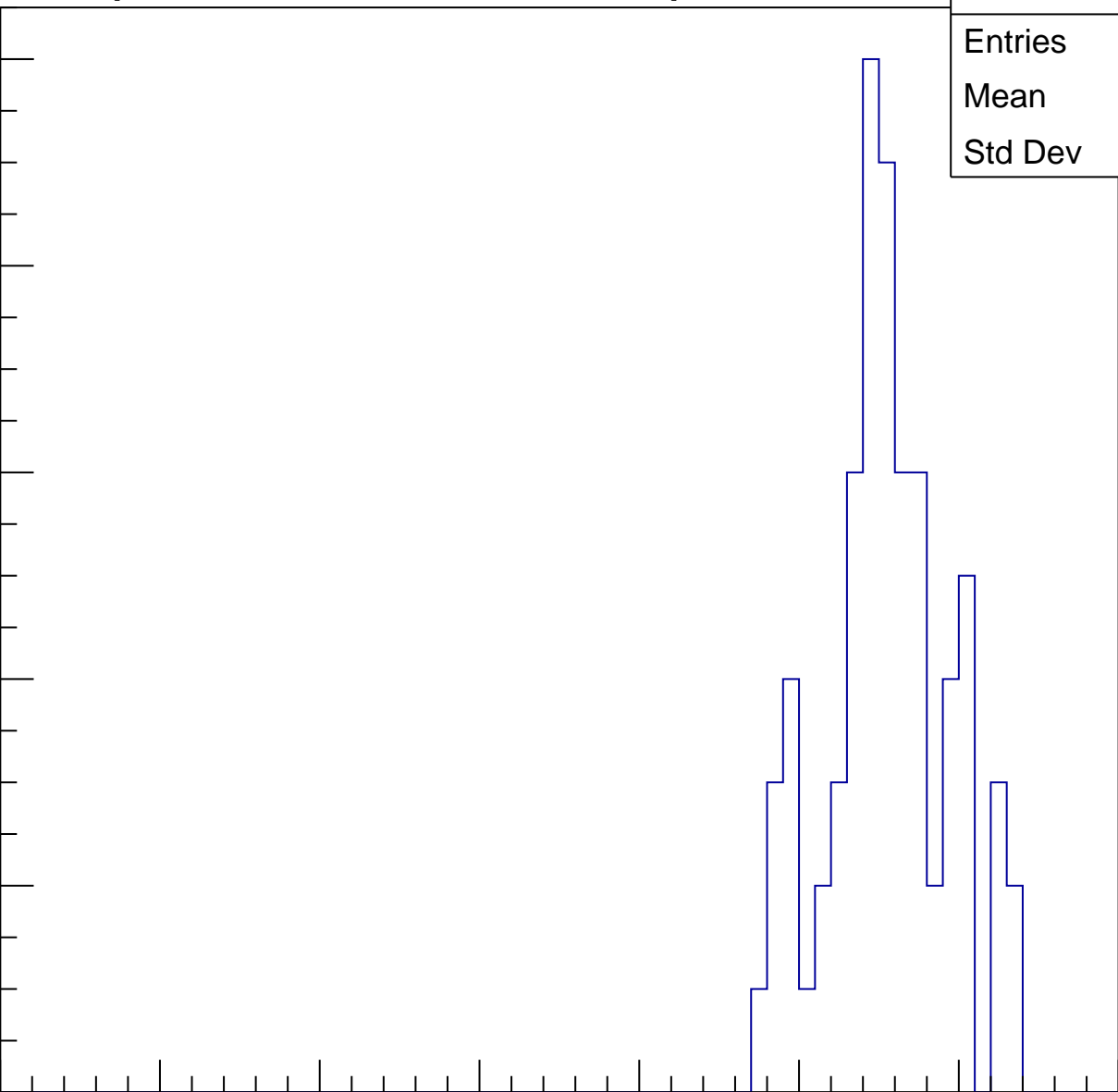
Entries	67
Mean	55.07
Std Dev	3.834

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B1L103S, U9-ch92, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

7

6

5

4

3

2

1

0

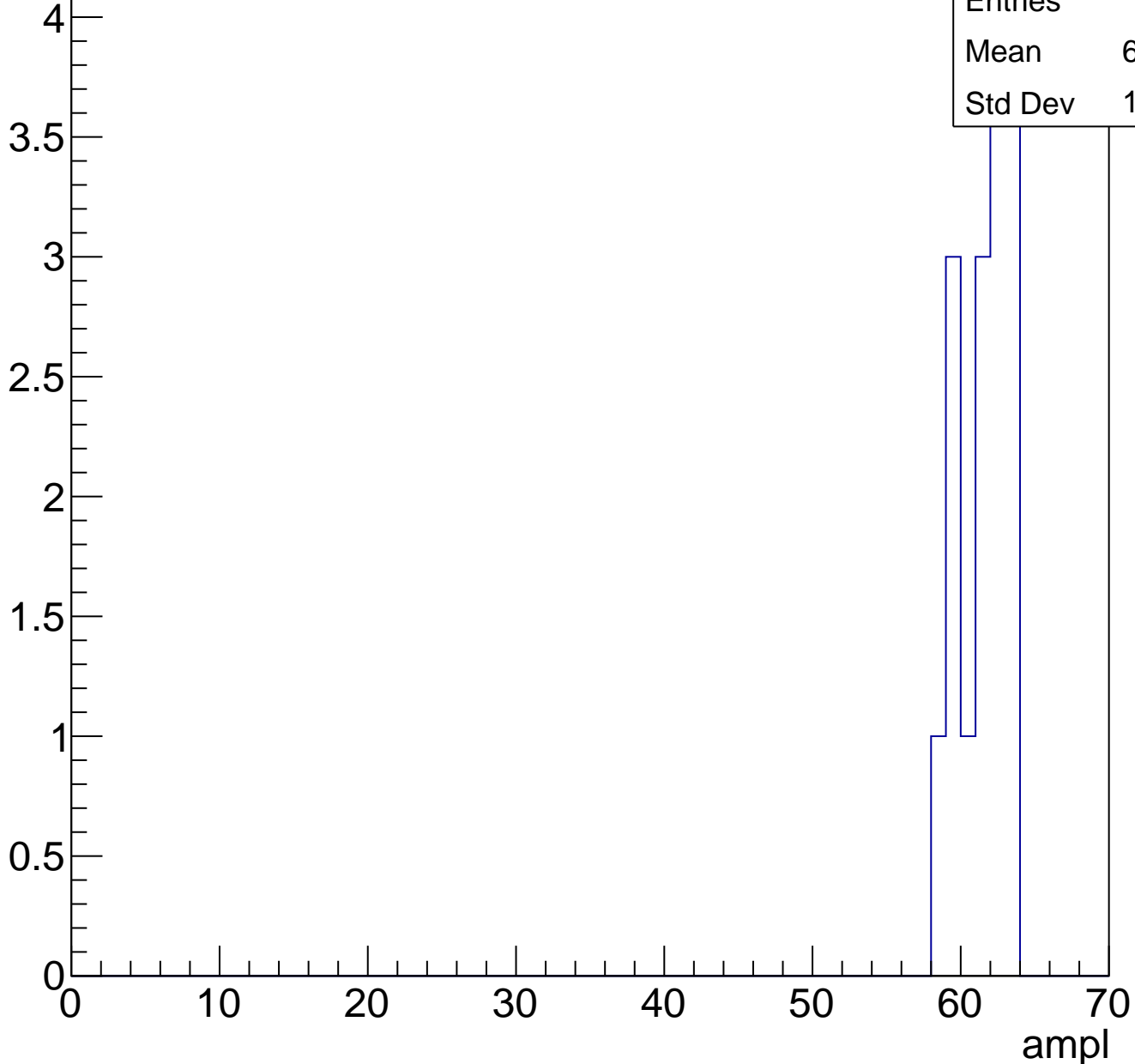
Entries	35
Mean	57.91
Std Dev	10.16

ampl

# B1L103S, U9-ch92, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U9-ch92, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L103S, U9-ch93, adc0

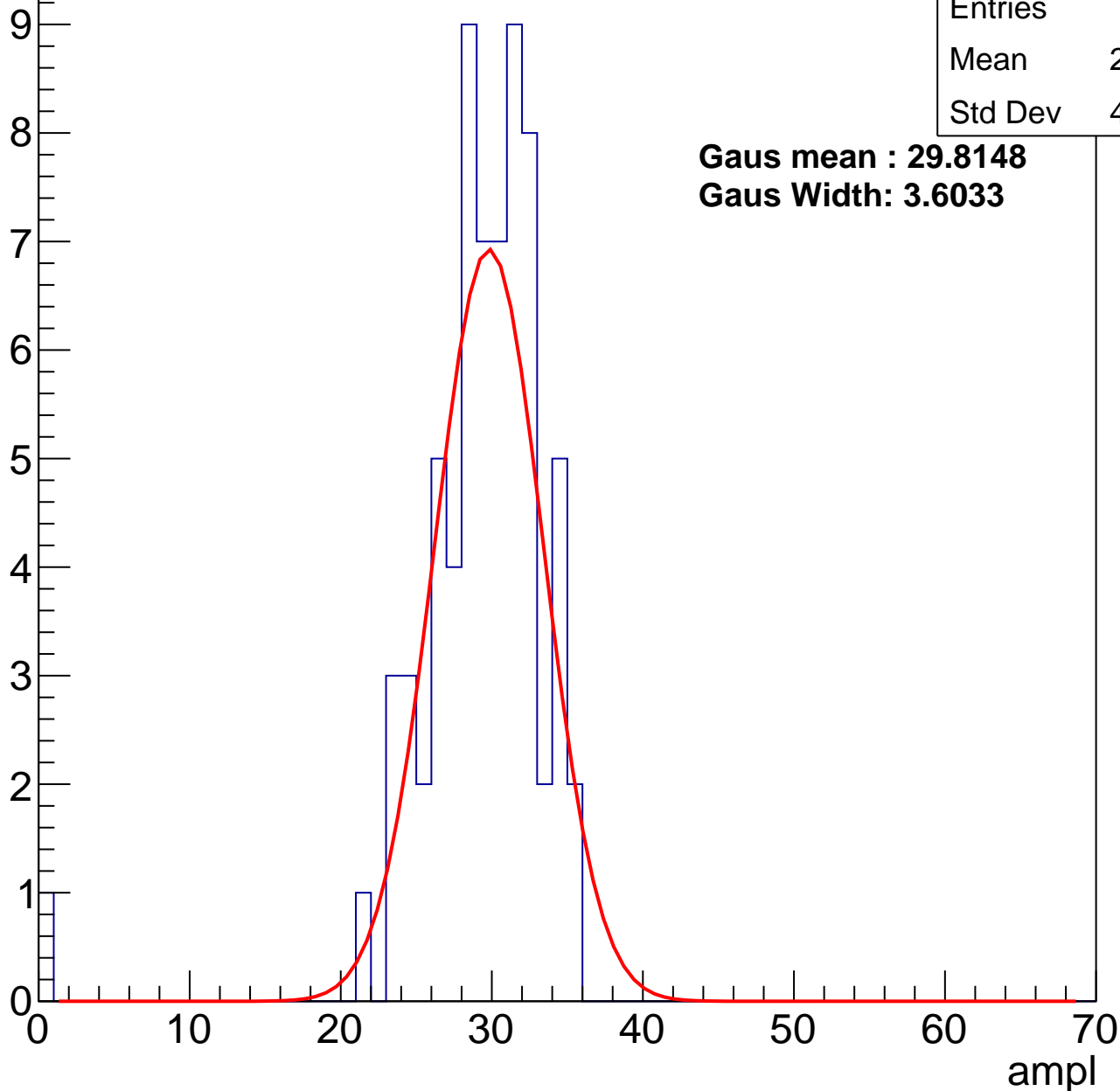
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	68
Mean	28.76
Std Dev	4.744

**Gaus mean : 29.8148**

**Gaus Width: 3.6033**



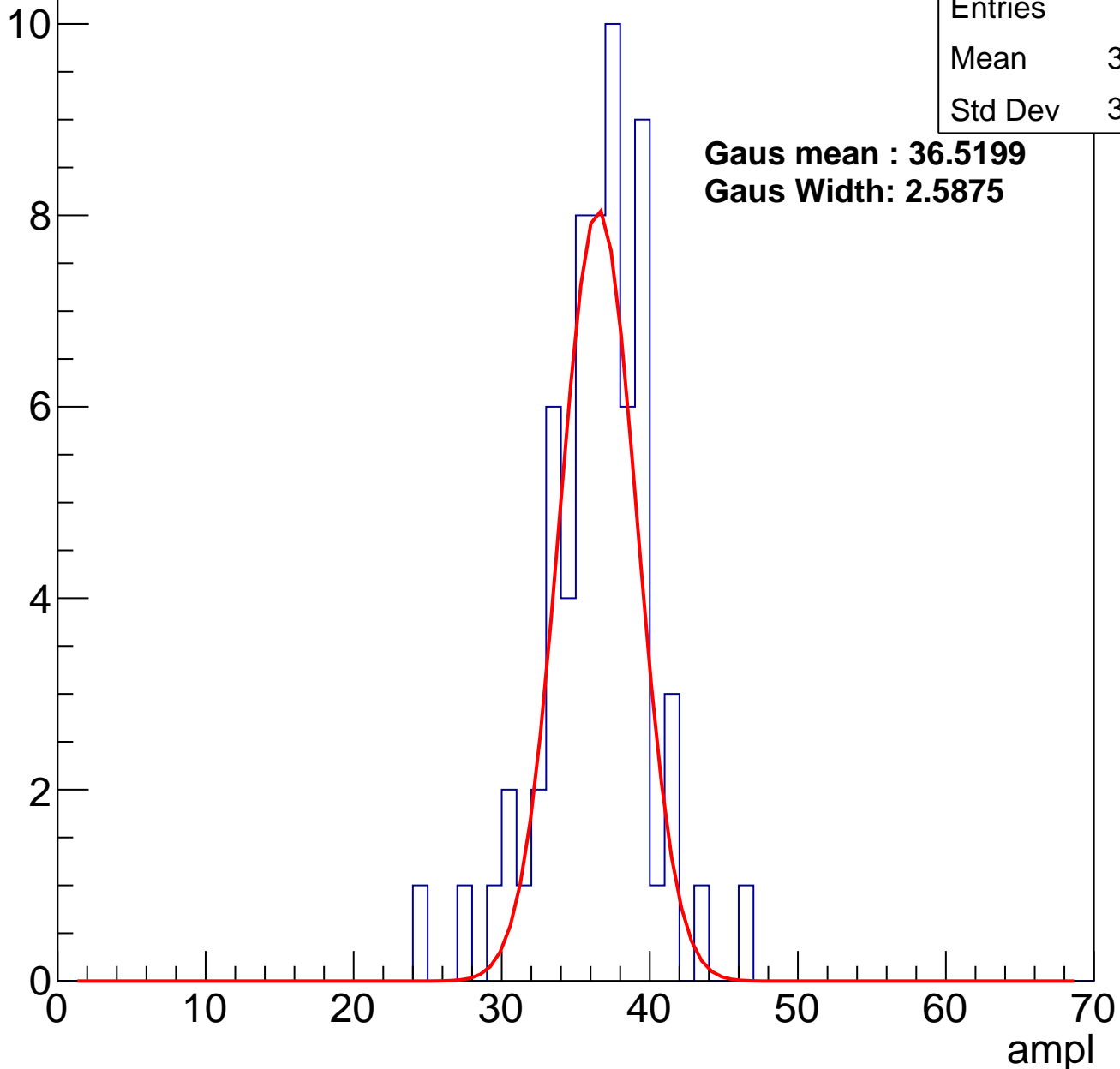
# B1L103S, U9-ch93, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	65
Mean	35.97
Std Dev	3.586

**Gaus mean : 36.5199**  
**Gaus Width: 2.5875**

Entry



# B1L103S, U9-ch93, adc2

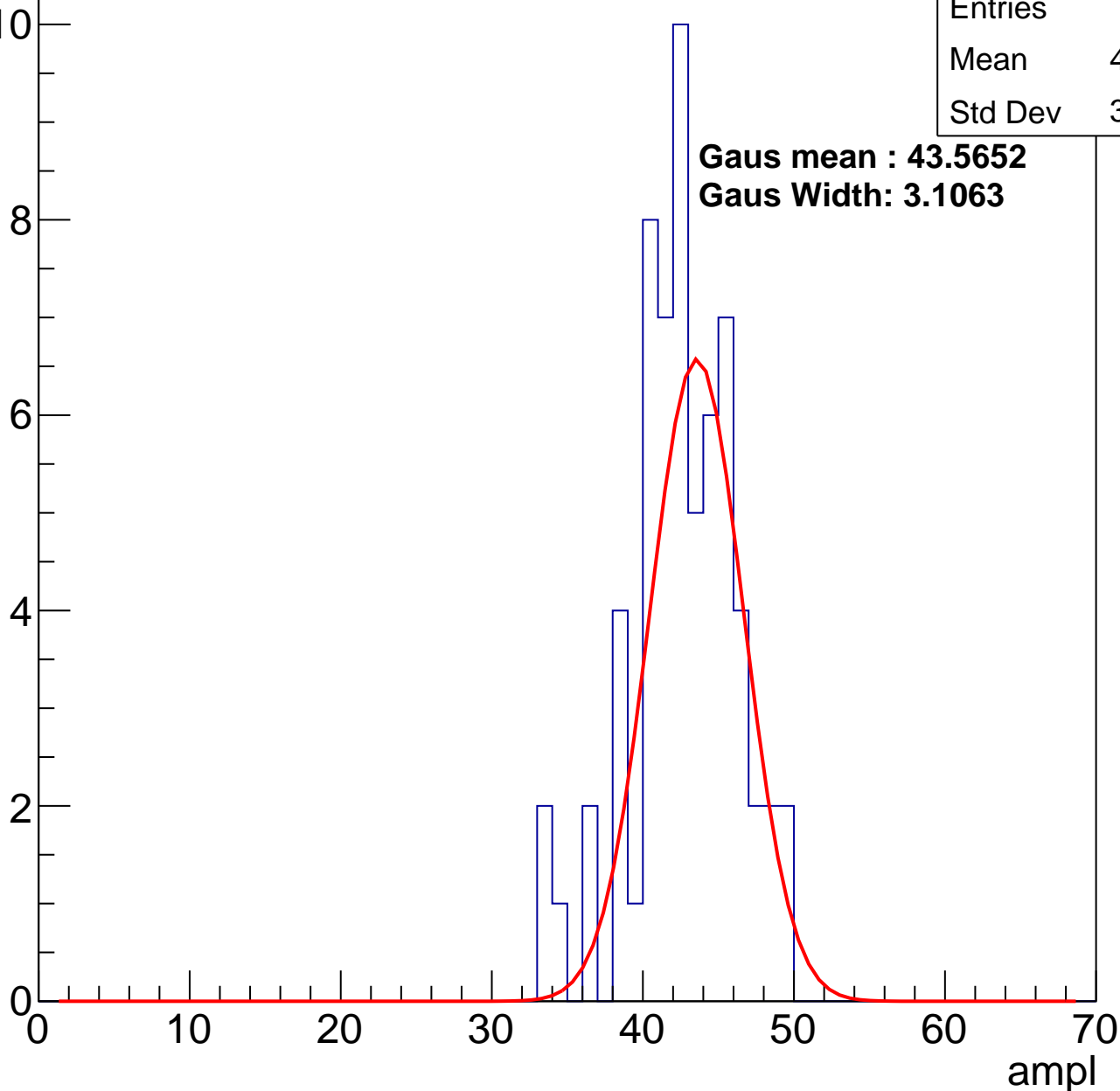
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	42.16
Std Dev	3.529

**Gaus mean : 43.5652**

**Gaus Width: 3.1063**

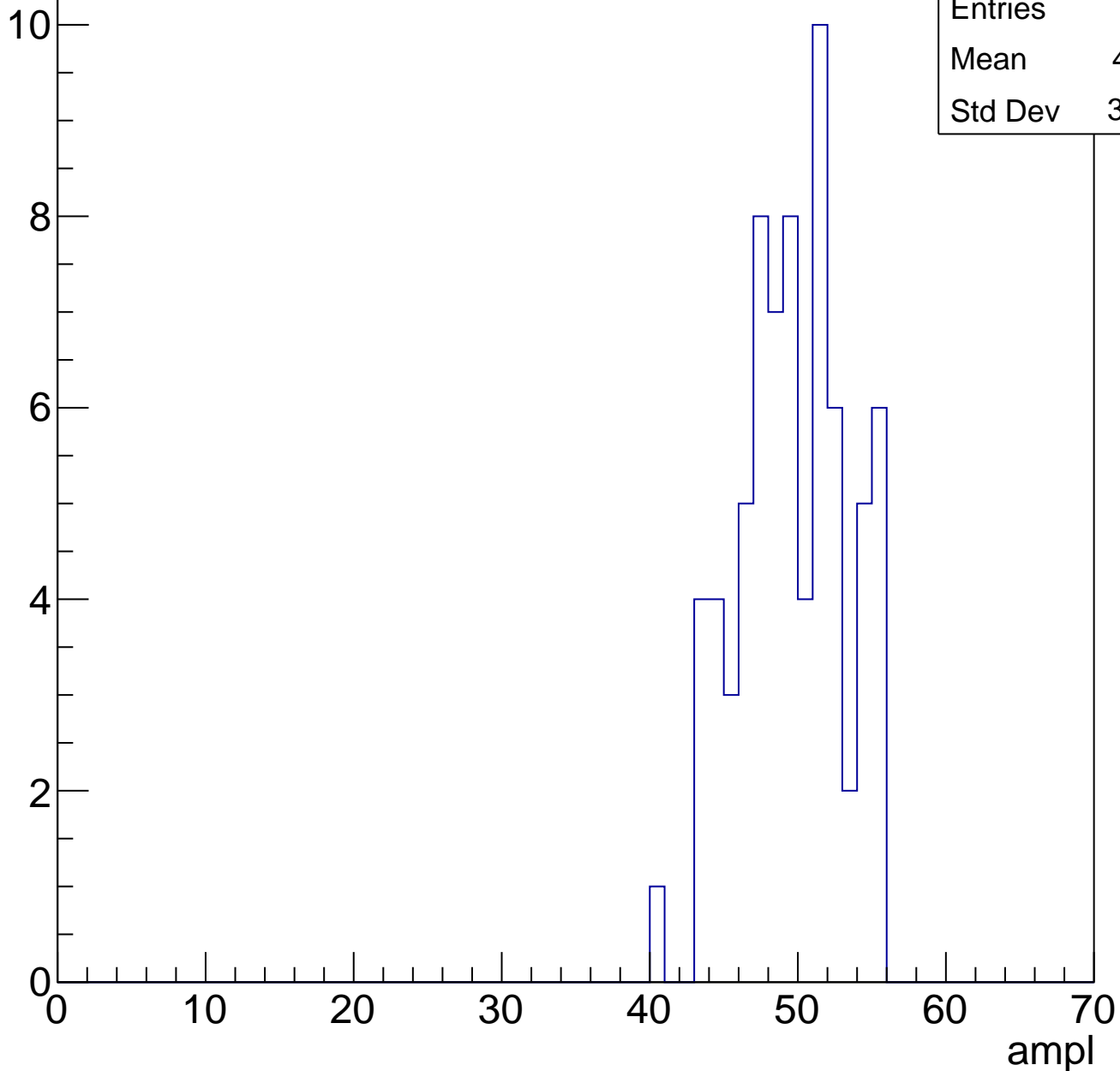


# B1L103S, U9-ch93, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

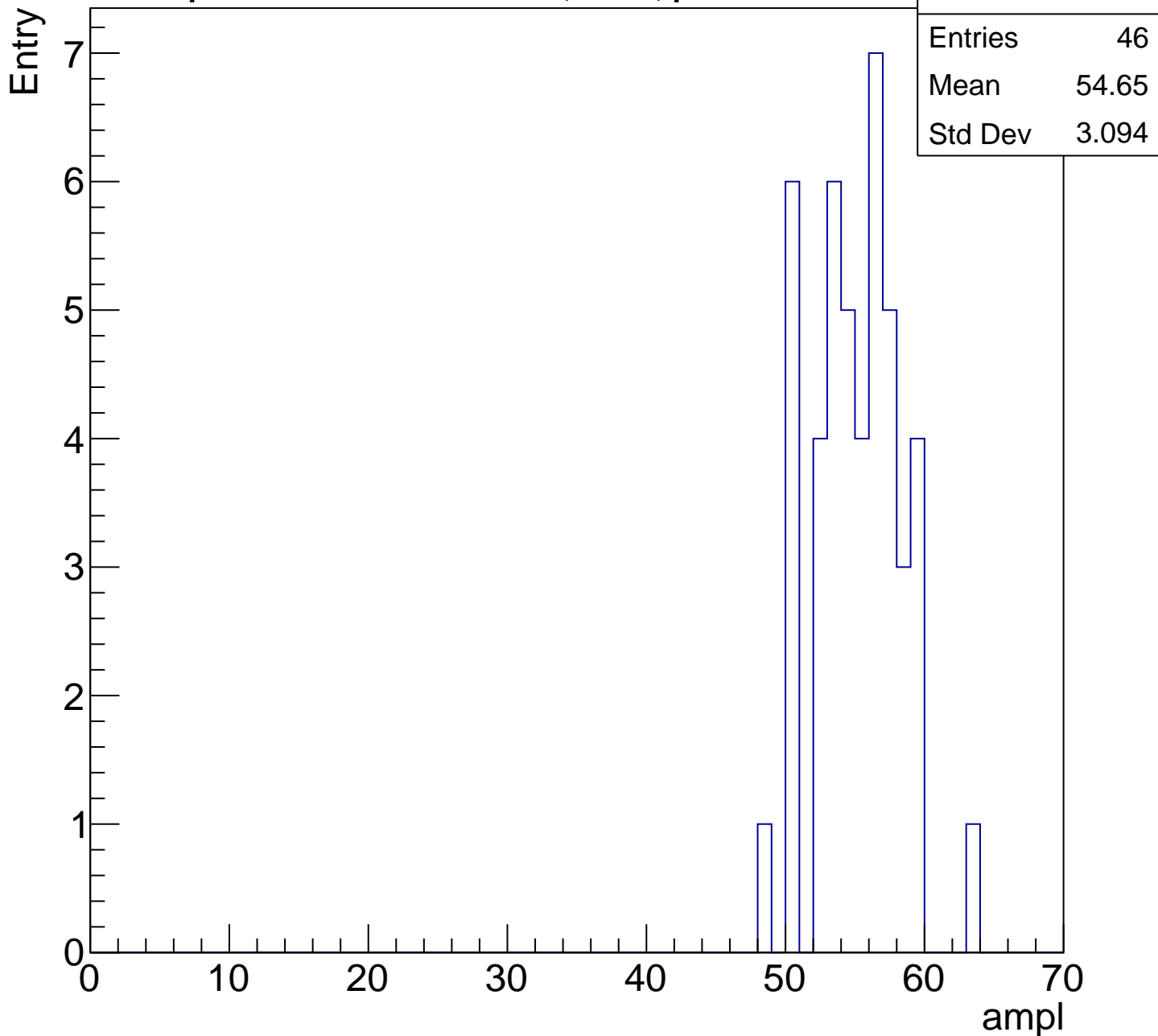
Entries	73
Mean	49.11
Std Dev	3.564

Entry



# B1L103S, U9-ch93, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

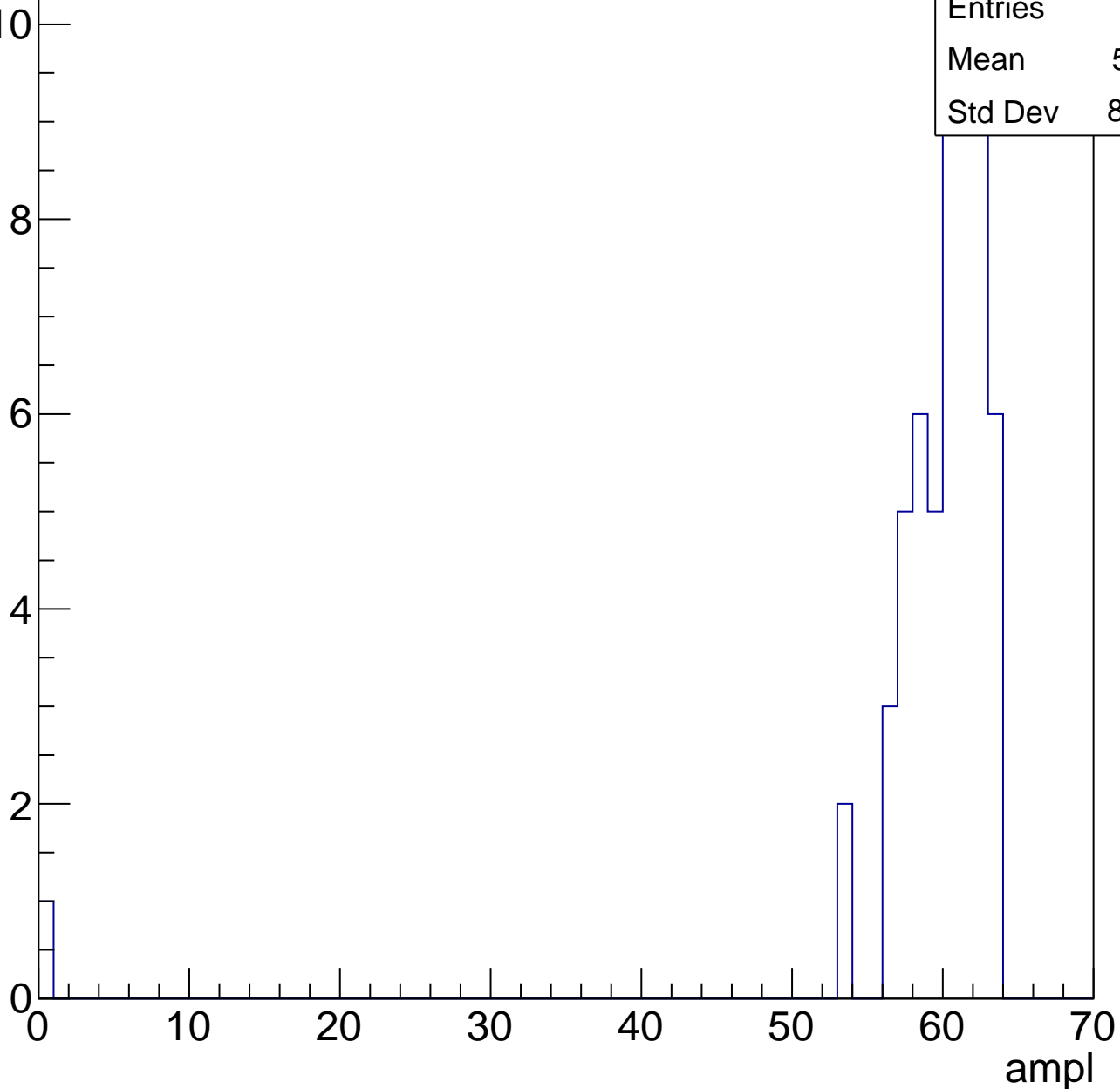


# B1L103S, U9-ch93, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

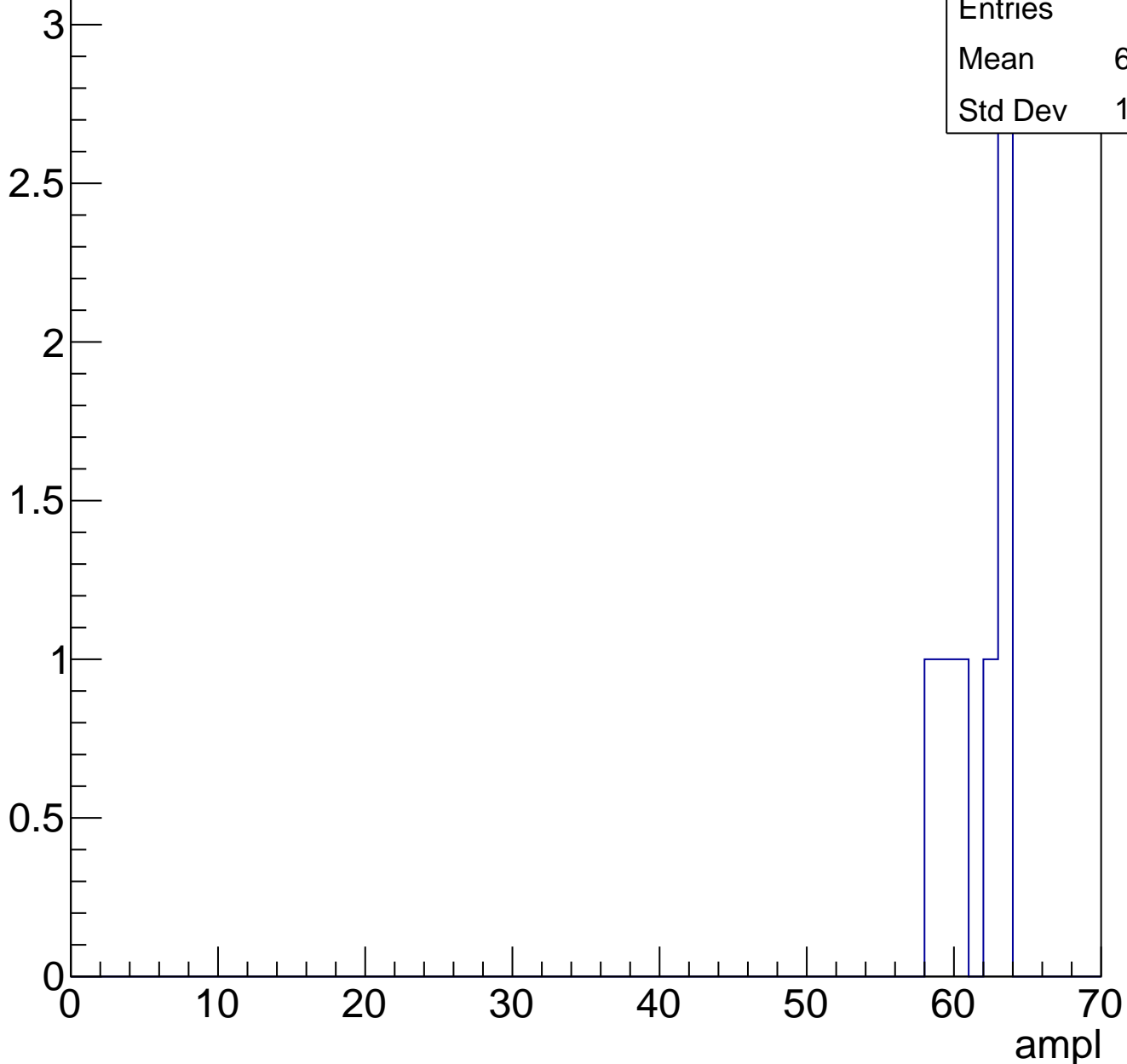
Entries	56
Mean	58.71
Std Dev	8.267



# B1L103S, U9-ch93, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U9-ch93, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U9-ch94, adc0

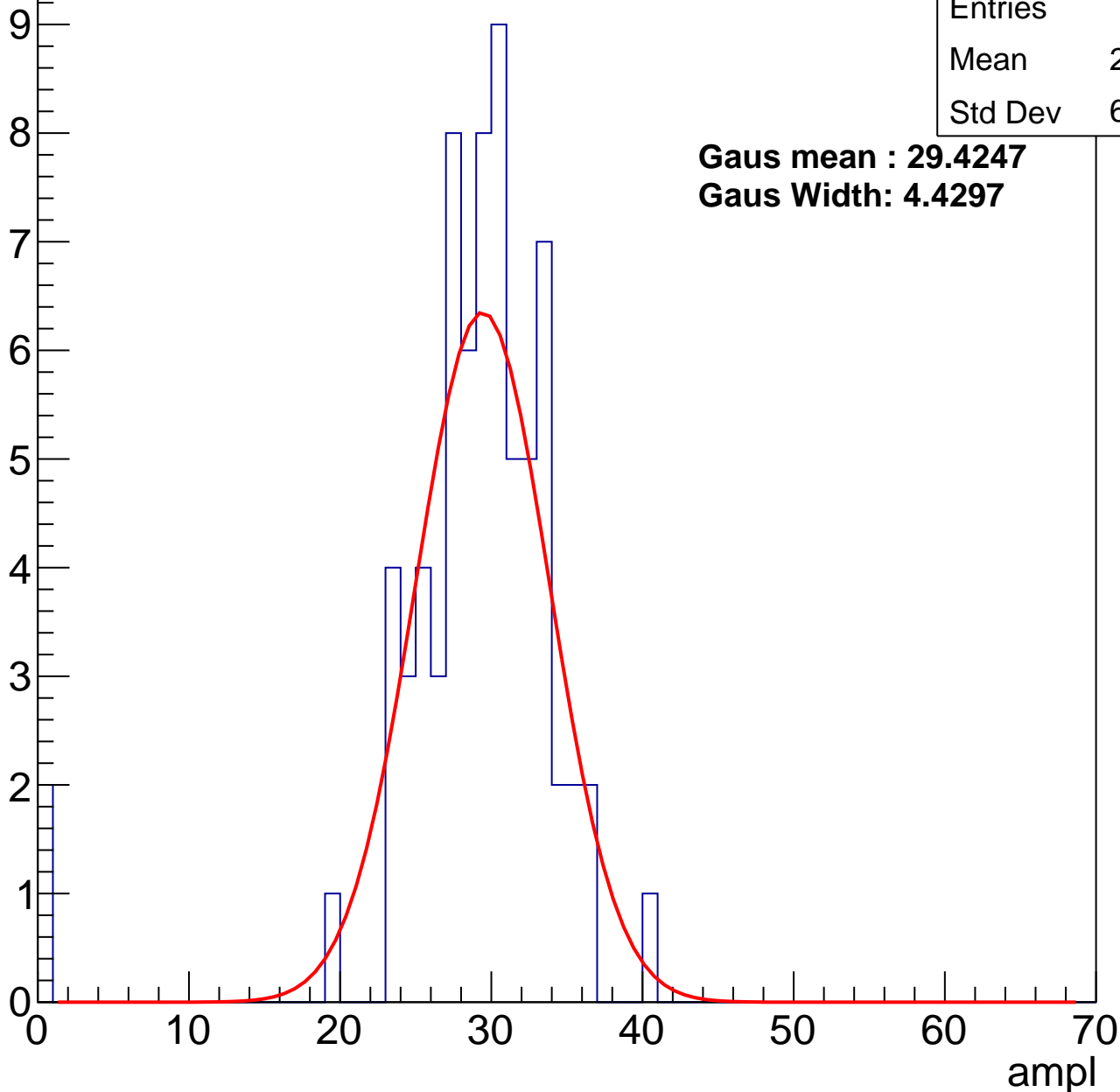
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	72
Mean	28.38
Std Dev	6.043

**Gaus mean : 29.4247**

**Gaus Width: 4.4297**



# B1L103S, U9-ch94, adc1

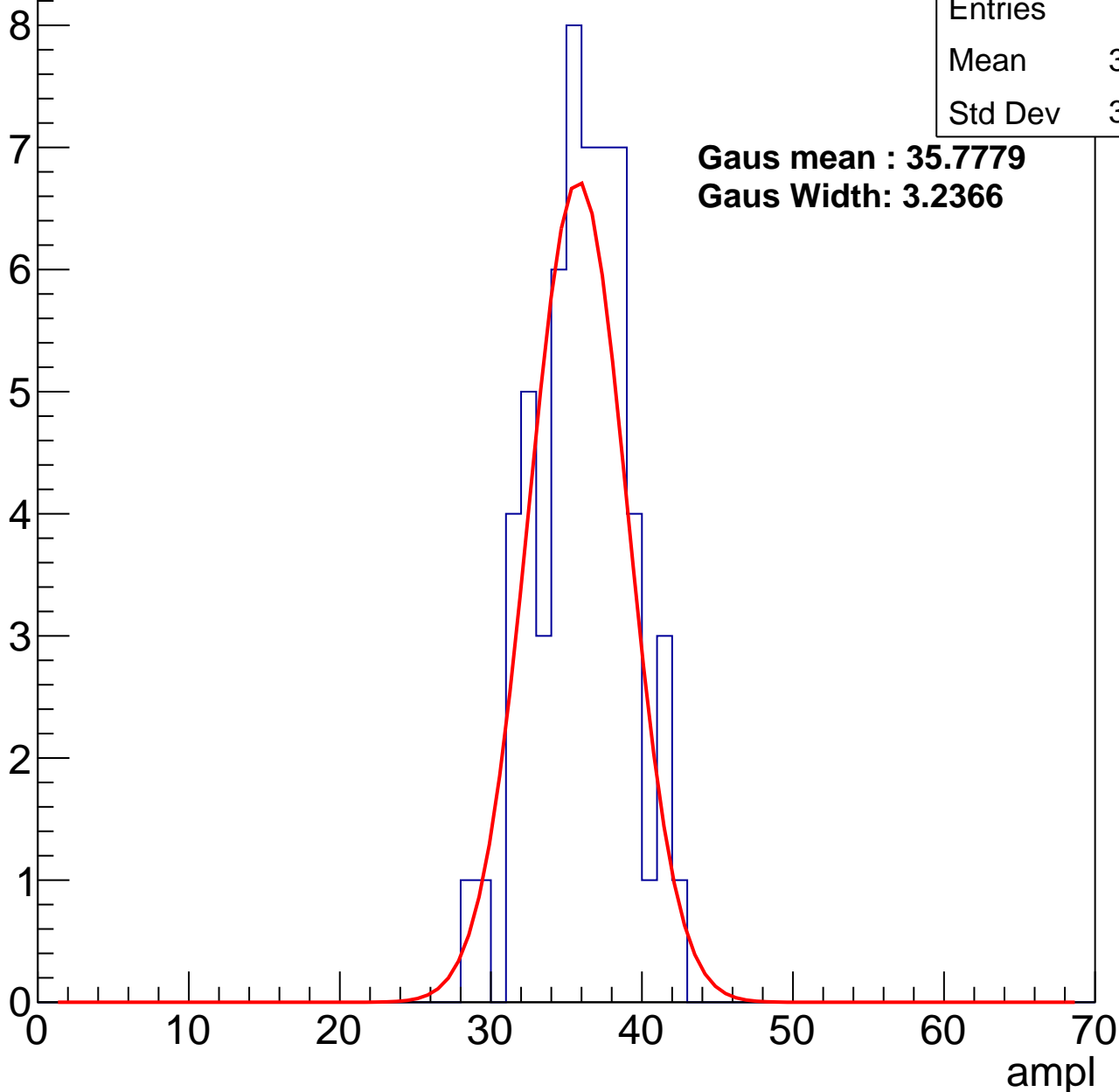
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	58
Mean	35.55
Std Dev	3.047

**Gaus mean : 35.7779**

**Gaus Width: 3.2366**



# B1L103S, U9-ch94, adc2

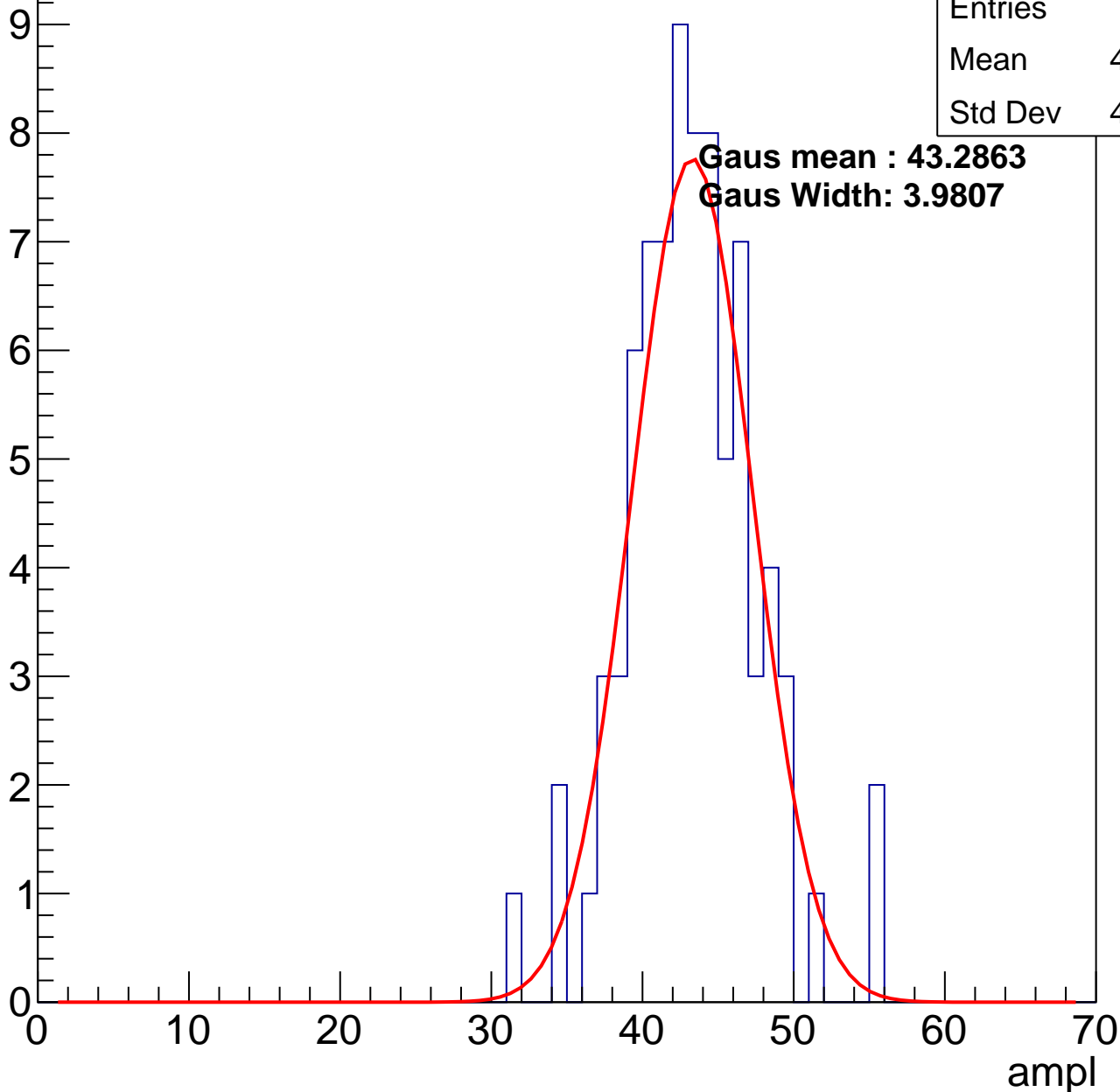
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	80
Mean	42.79
Std Dev	4.227

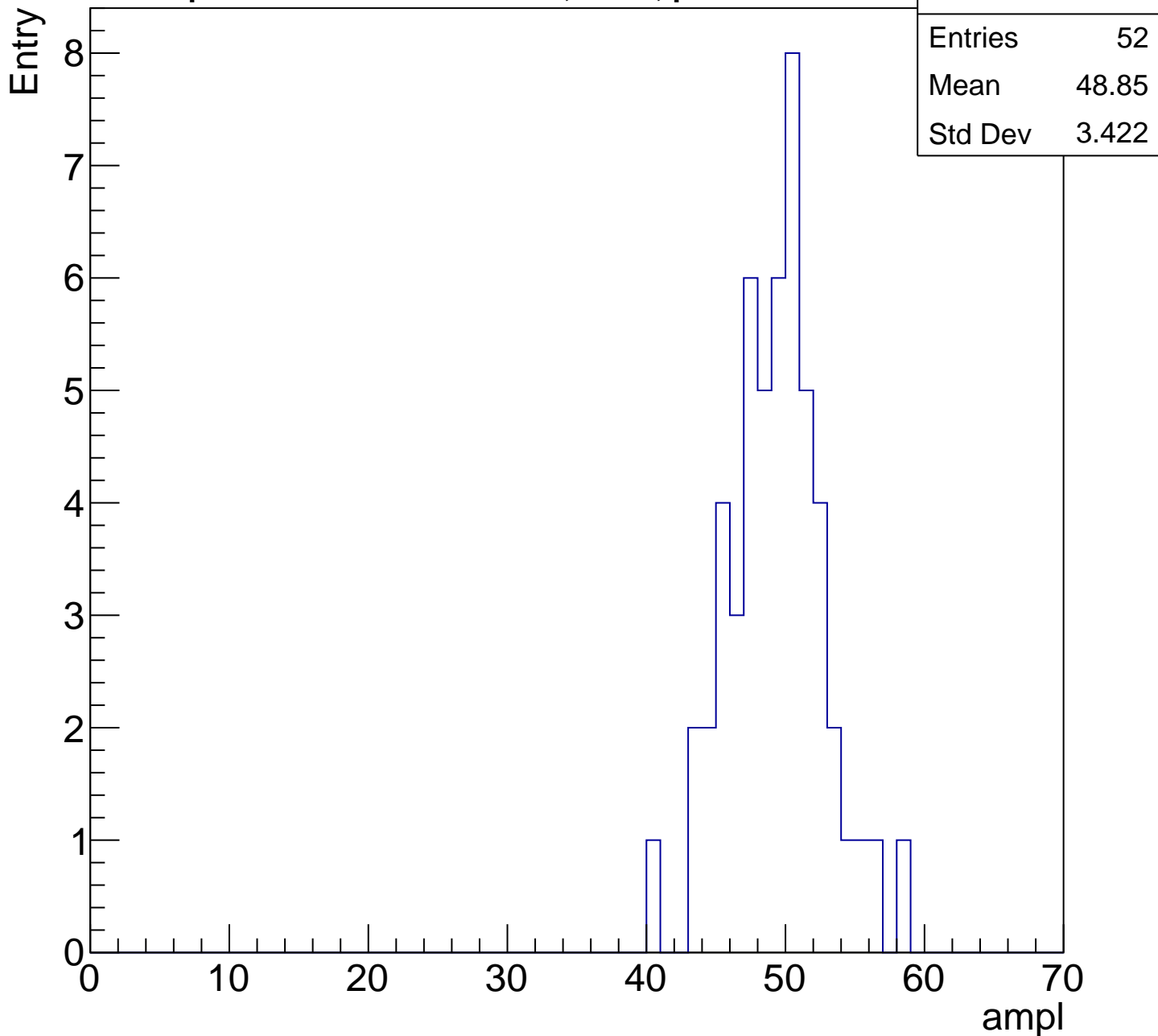
**Gaus mean : 43.2863**

**Gaus Width: 3.9807**



# B1L103S, U9-ch94, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

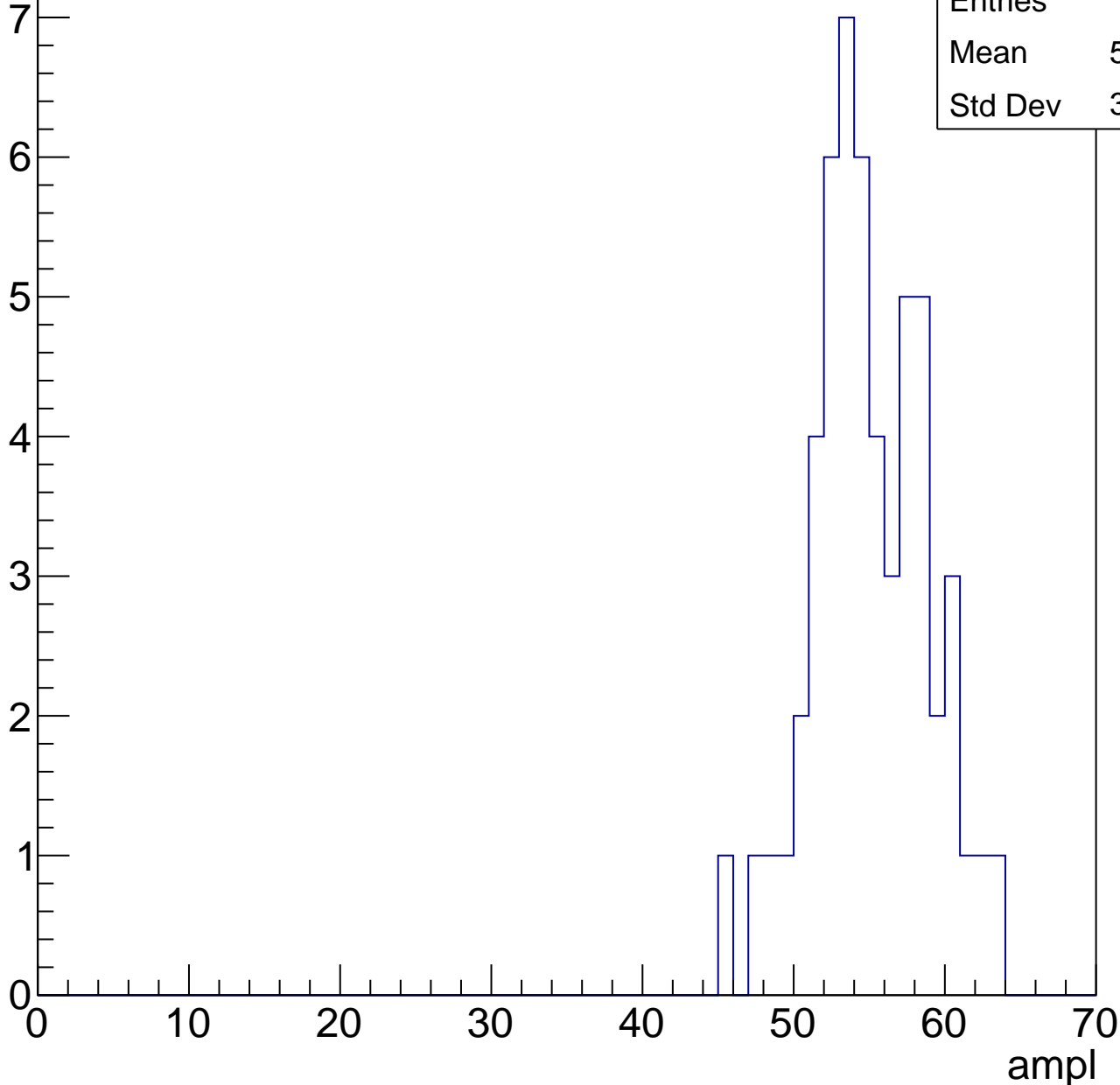


# B1L103S, U9-ch94, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	54
Mean	54.57
Std Dev	3.764

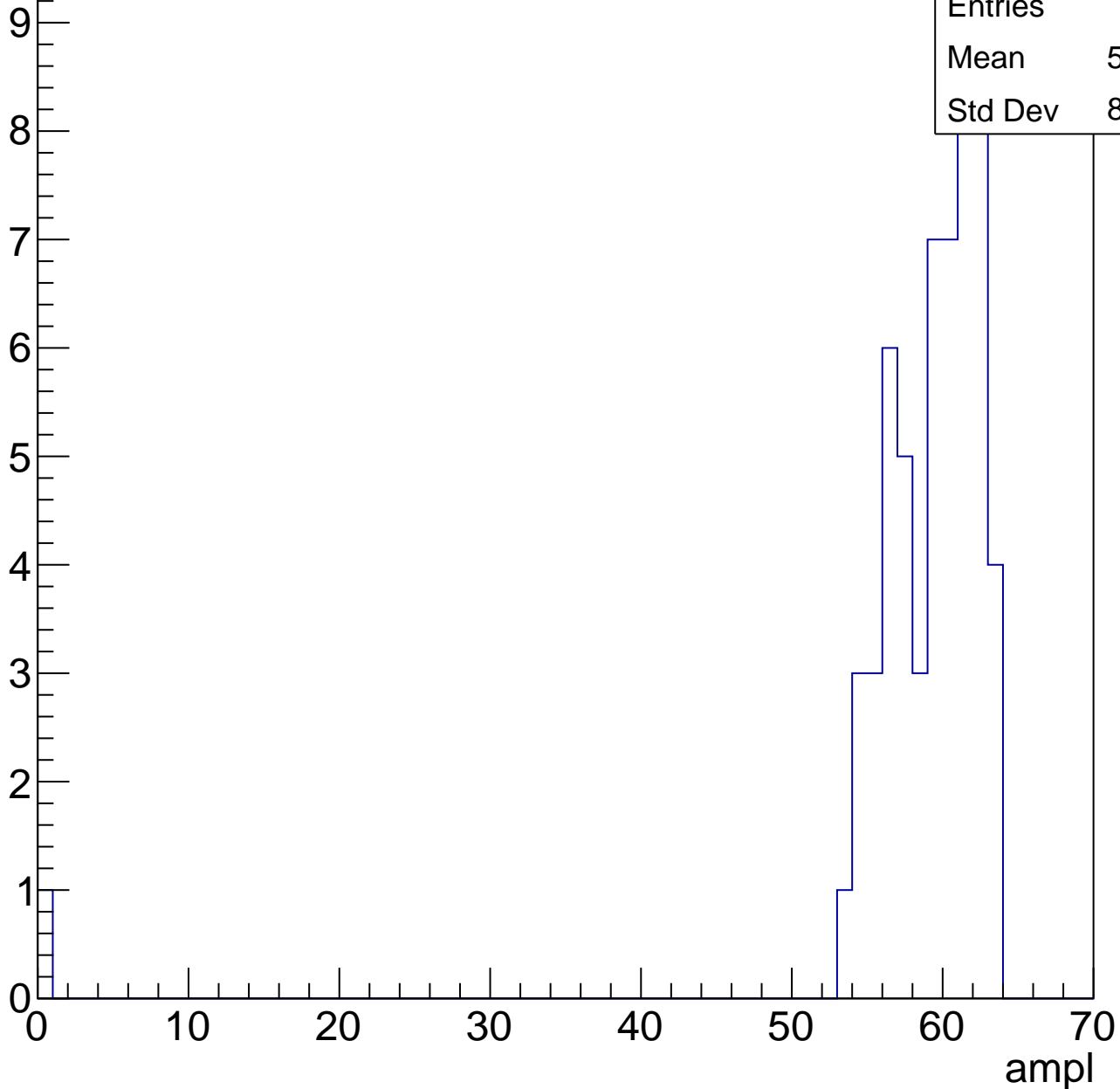


# B1L103S, U9-ch94, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	57
Mean	57.98
Std Dev	8.205

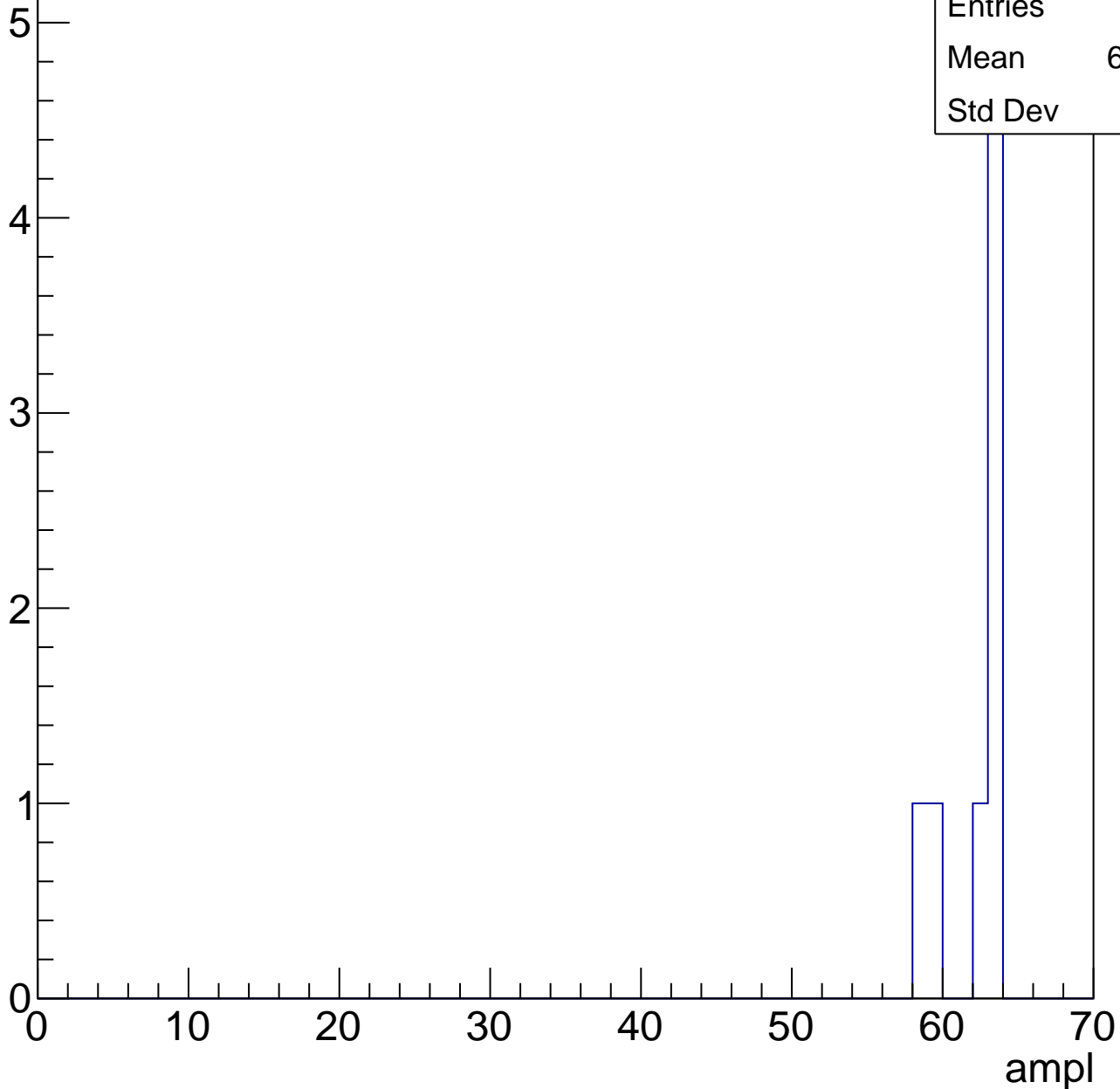


# B1L103S, U9-ch94, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	8
Mean	61.75
Std Dev	1.92





# B1L103S, U9-ch94, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U9-ch95, adc0

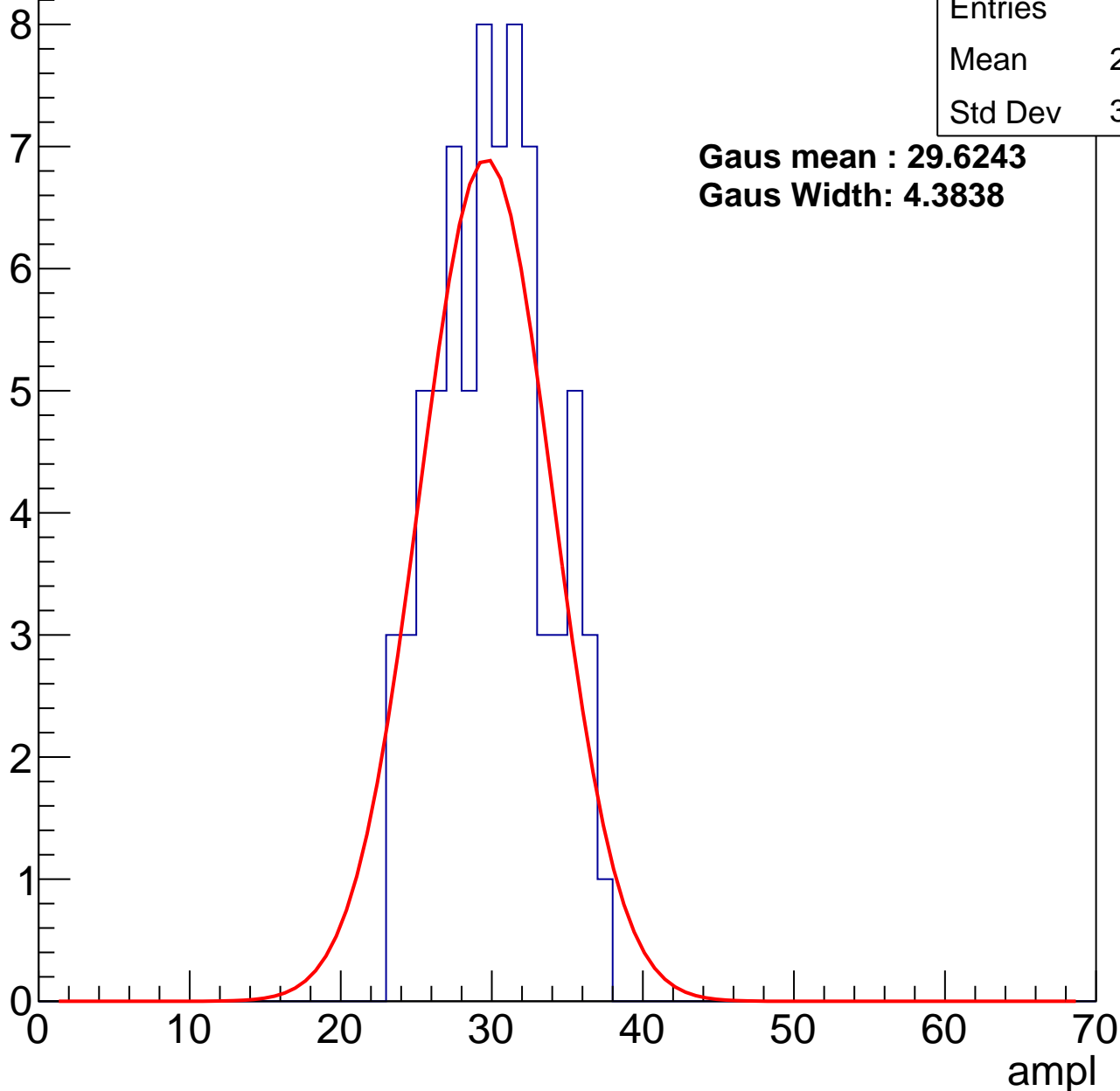
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	73
Mean	29.59
Std Dev	3.572

**Gaus mean : 29.6243**

**Gaus Width: 4.3838**



# B1L103S, U9-ch95, adc1

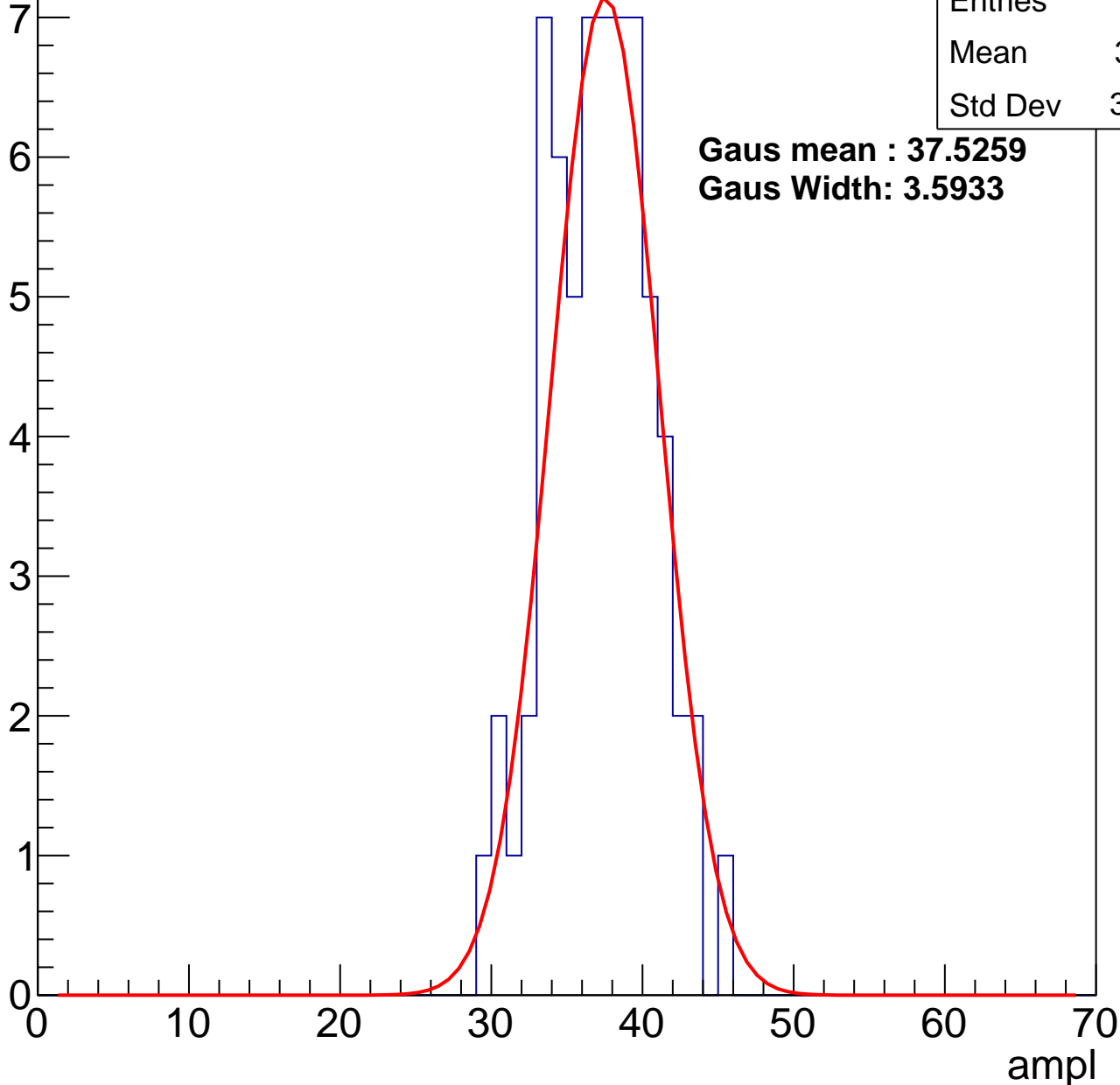
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	36.71
Std Dev	3.406

**Gaus mean : 37.5259**

**Gaus Width: 3.5933**



# B1L103S, U9-ch95, adc2

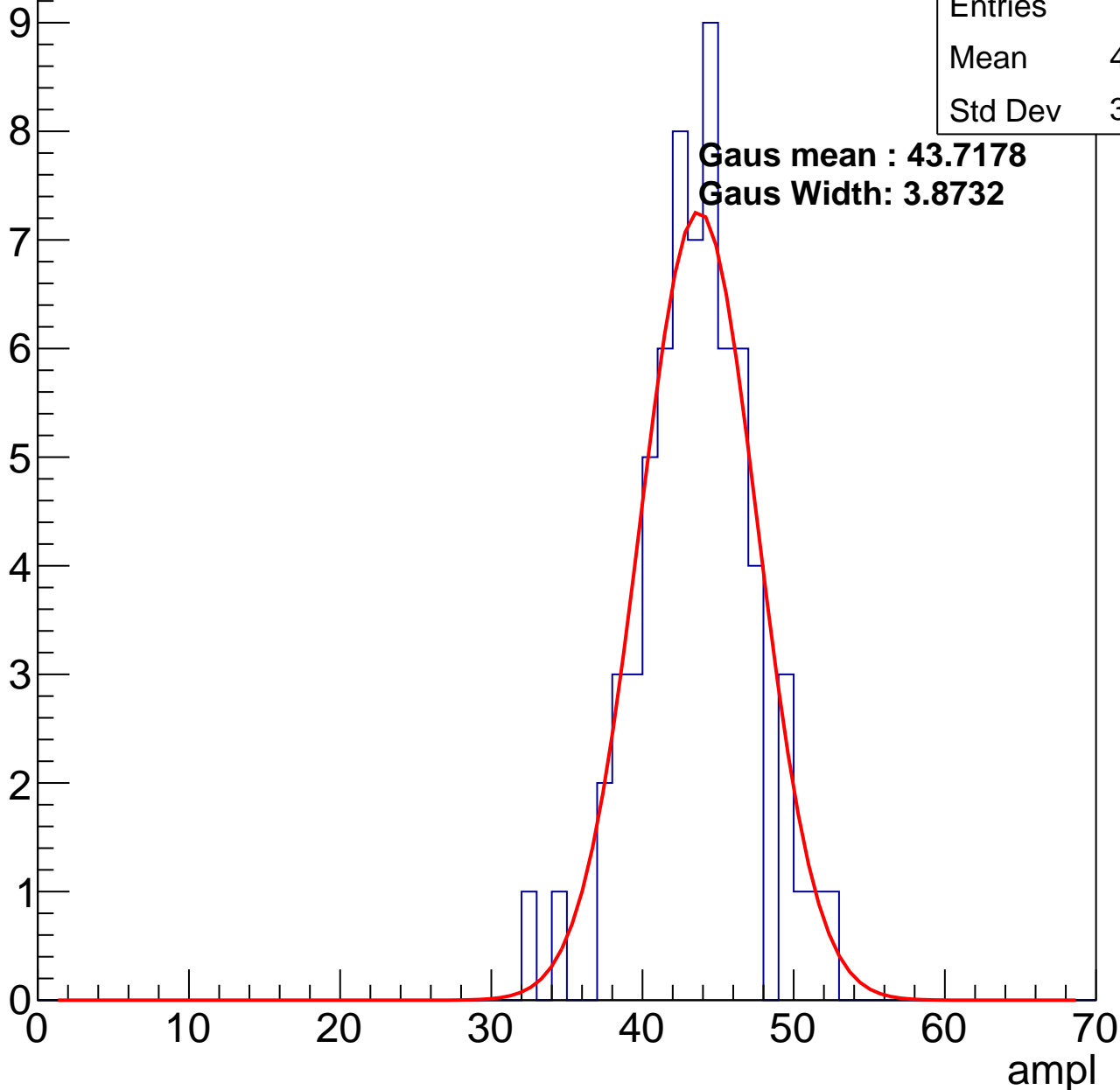
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	43.04
Std Dev	3.719

**Gaus mean : 43.7178**

**Gaus Width: 3.8732**

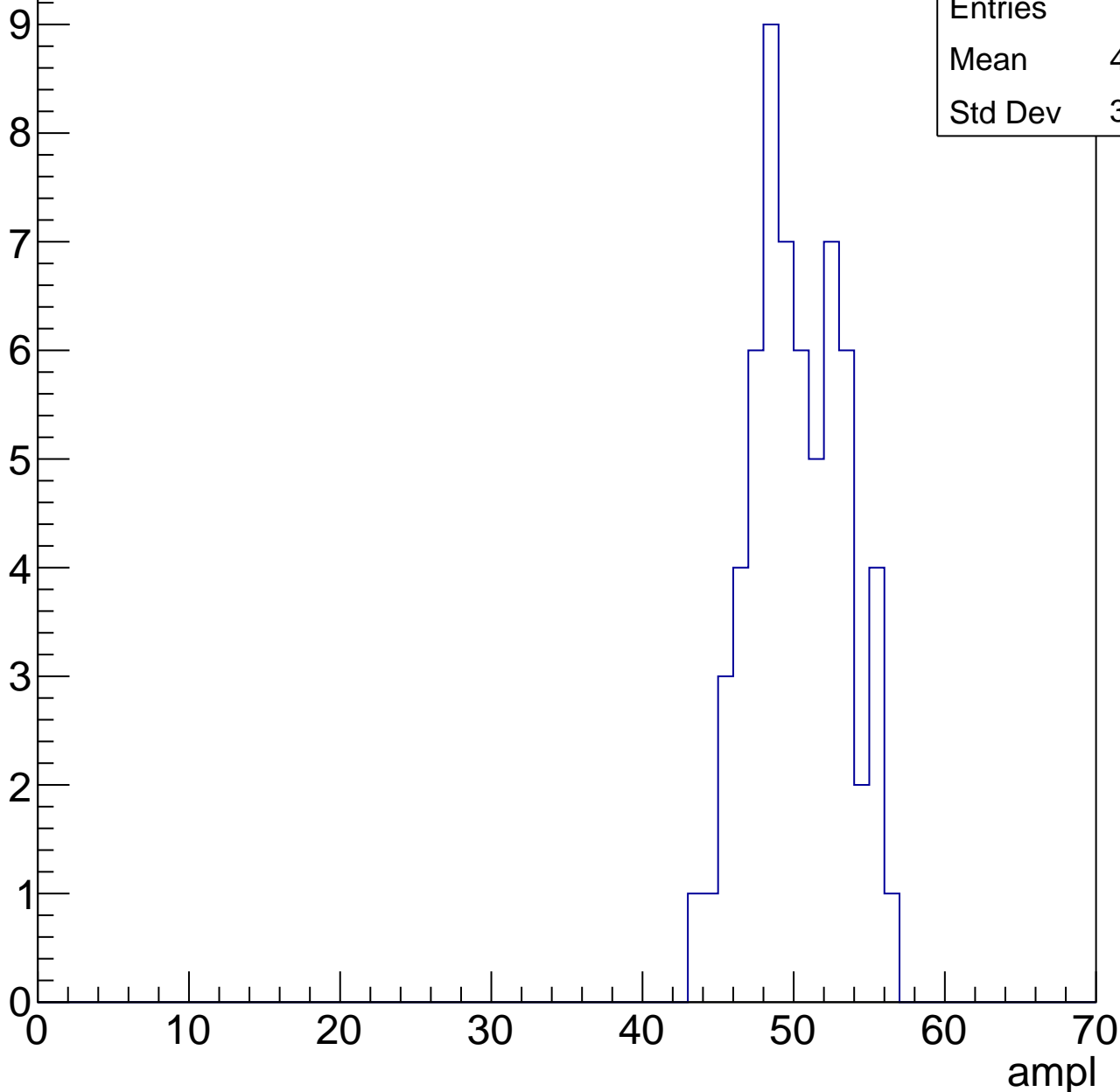


# B1L103S, U9-ch95, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	49.74
Std Dev	3.037

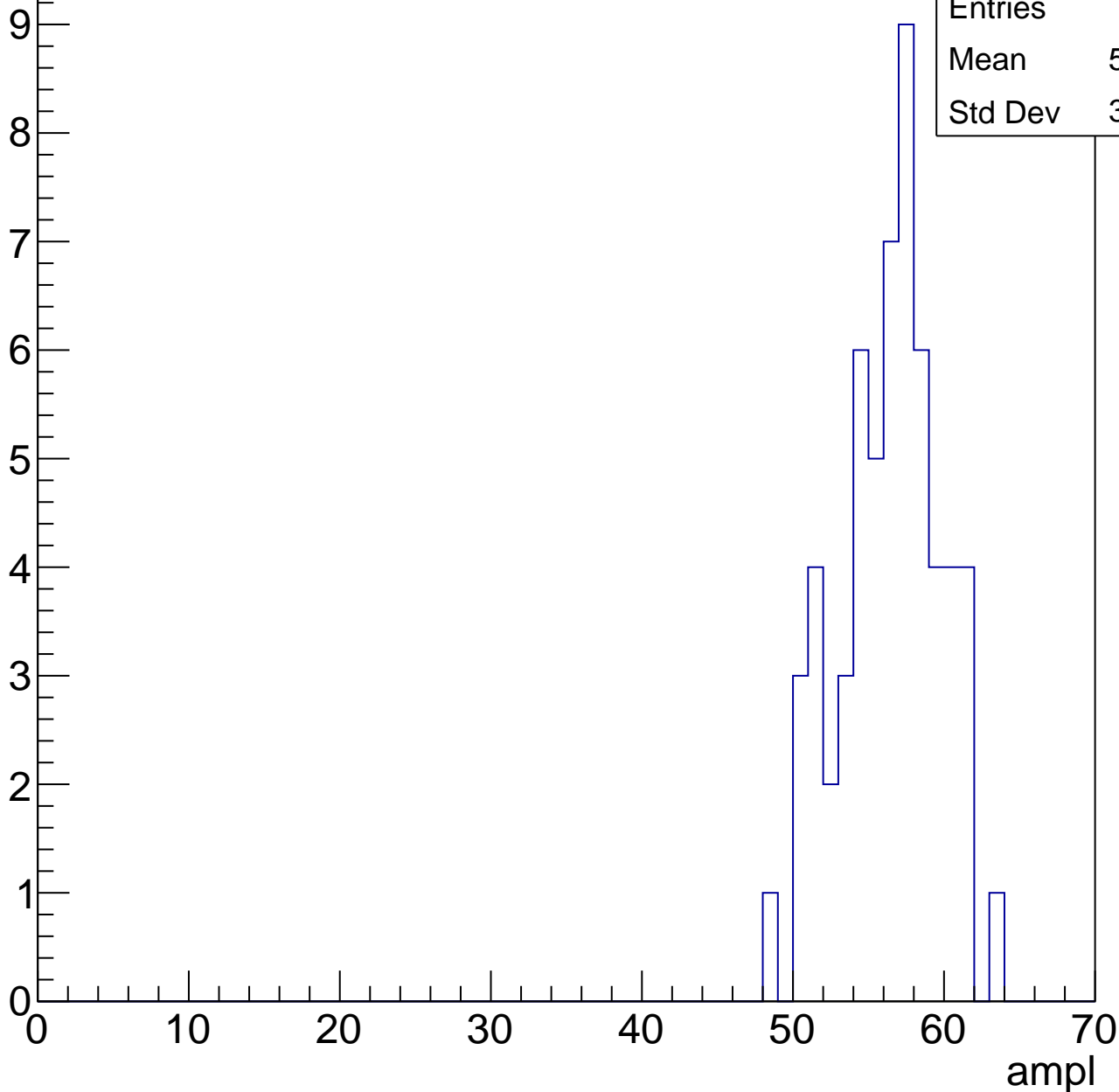


# B1L103S, U9-ch95, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	59
Mean	55.93
Std Dev	3.298

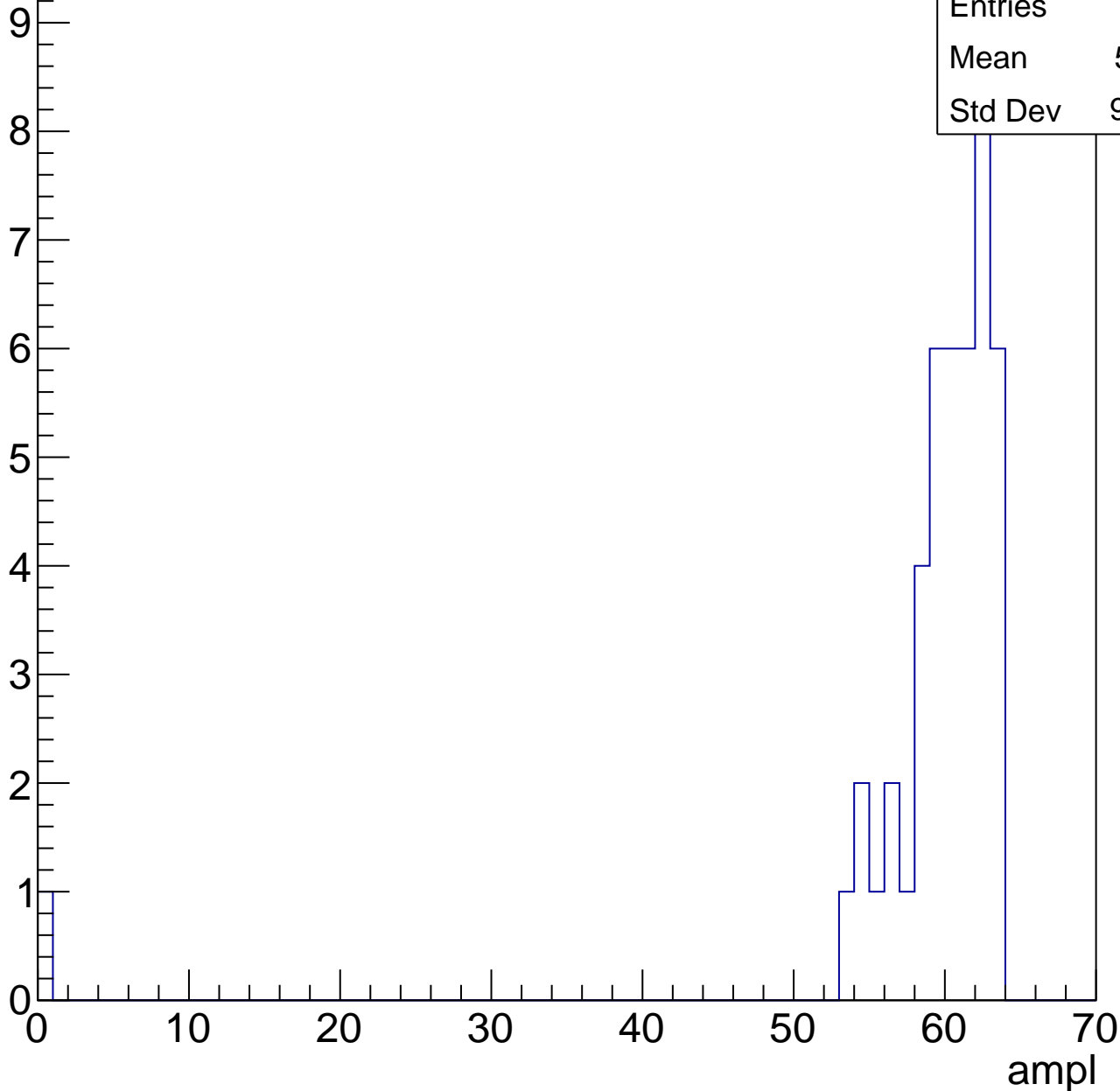


# B1L103S, U9-ch95, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	45
Mean	58.51
Std Dev	9.196



# B1L103S, U9-ch95, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



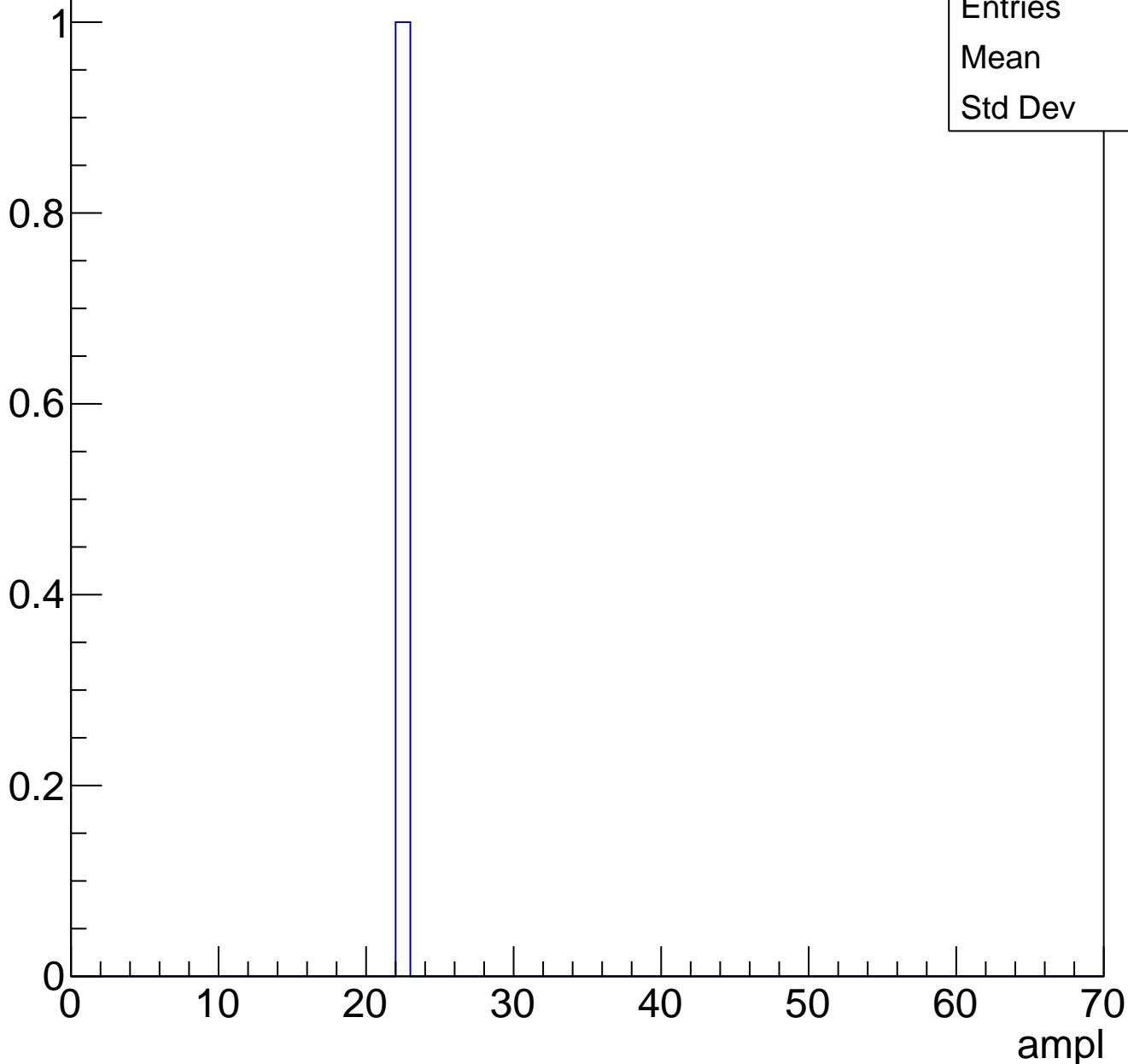
Entries	4
Mean	62.75
Std Dev	0.433



# B1L103S, U9-ch95, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



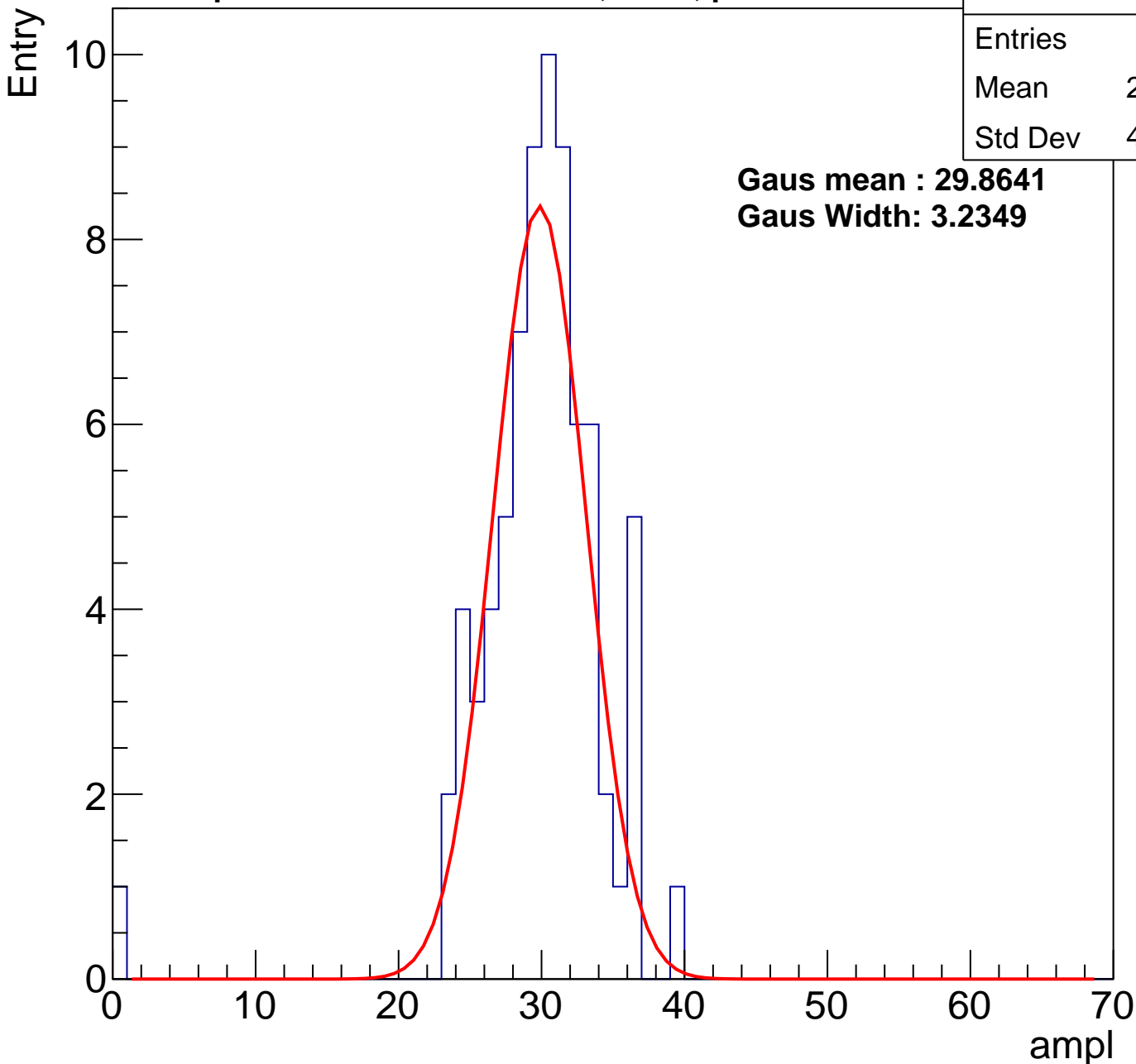
# B1L103S, U9-ch96, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	75
Mean	29.39
Std Dev	4.816

**Gaus mean : 29.8641**

**Gaus Width: 3.2349**



# B1L103S, U9-ch96, adc1

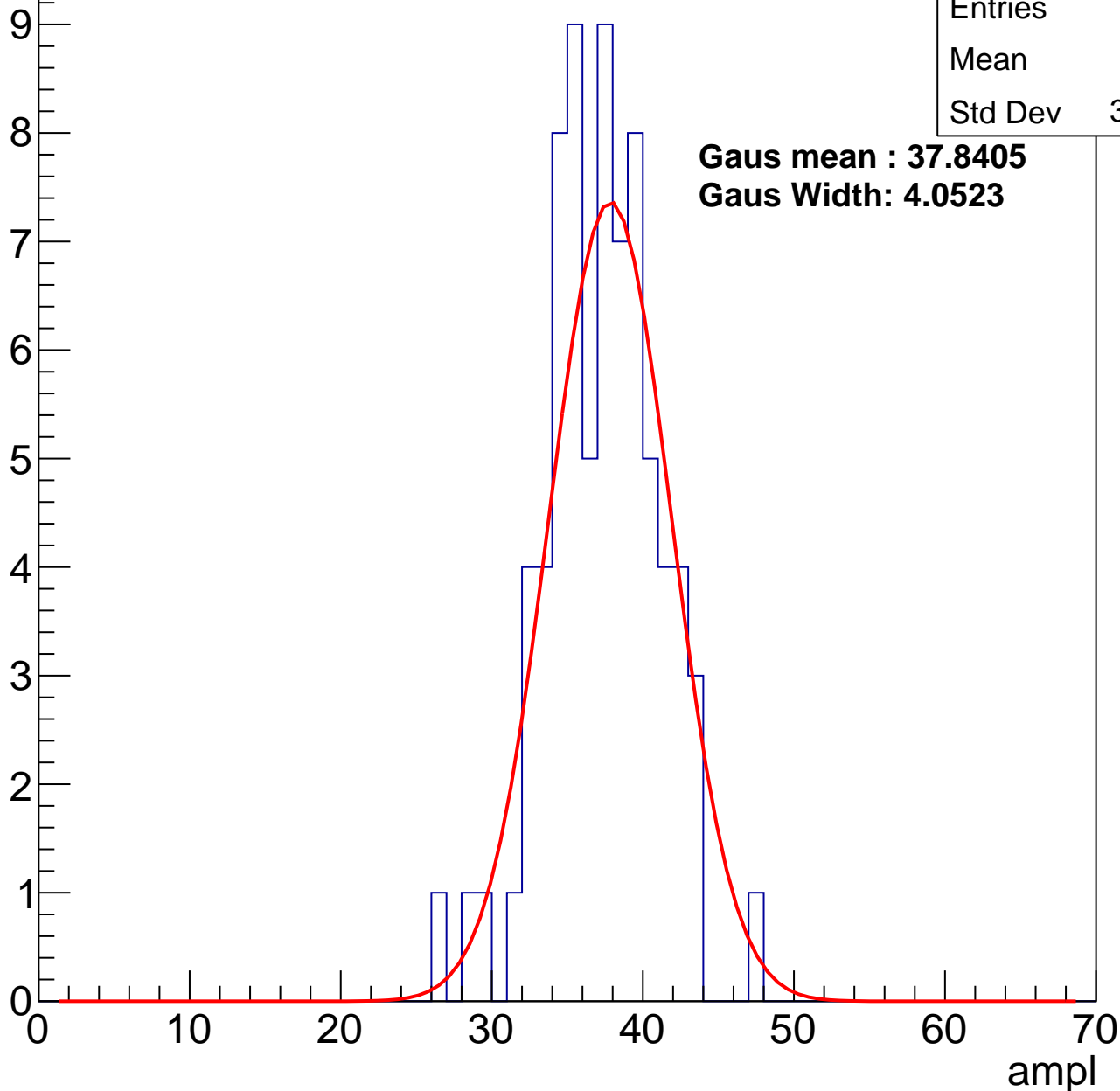
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	75
Mean	36.8
Std Dev	3.709

**Gaus mean : 37.8405**

**Gaus Width: 4.0523**



# B1L103S, U9-ch96, adc2

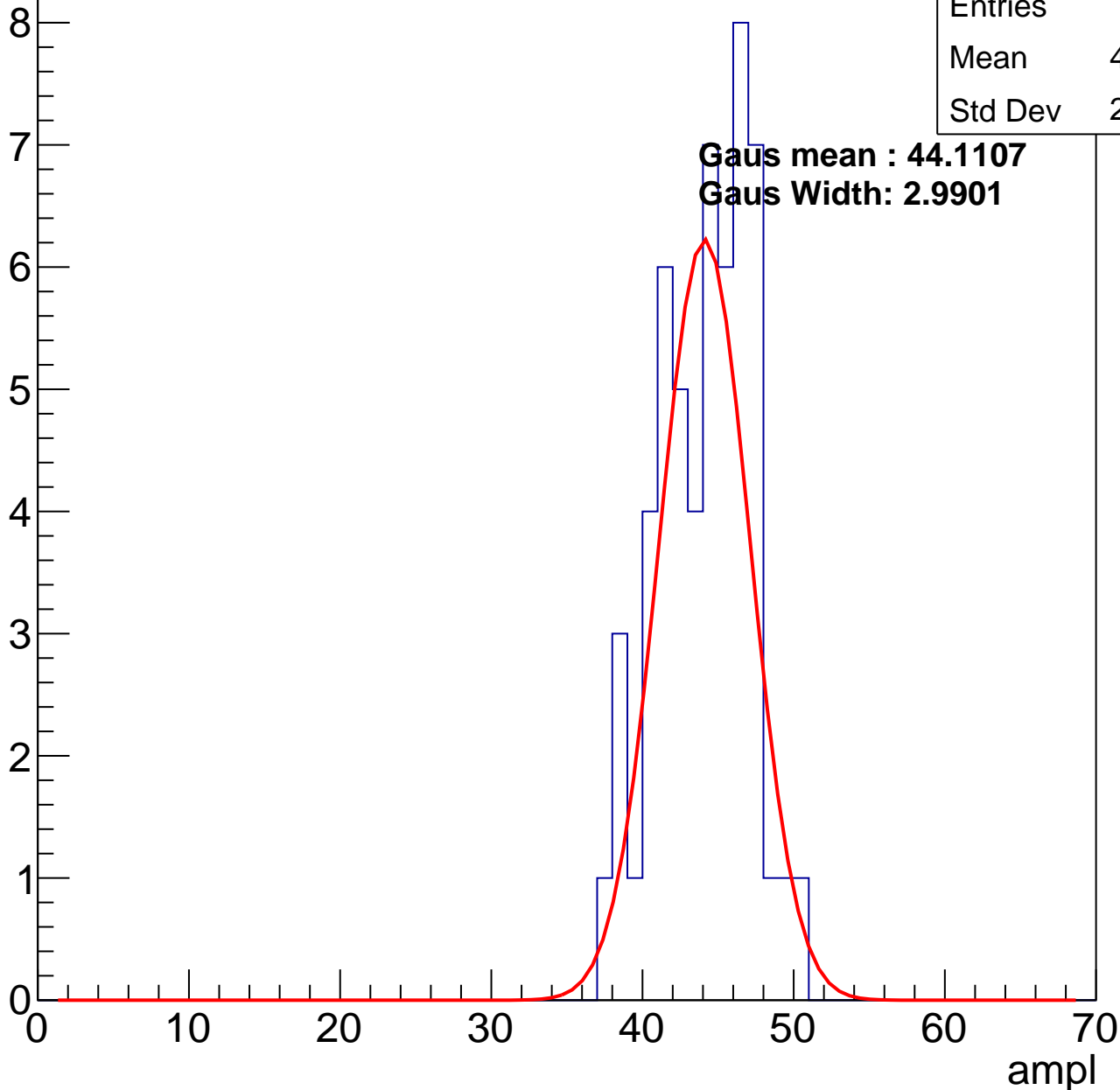
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	55
Mean	43.64
Std Dev	2.999

**Gaus mean : 44.1107**

**Gaus Width: 2.9901**

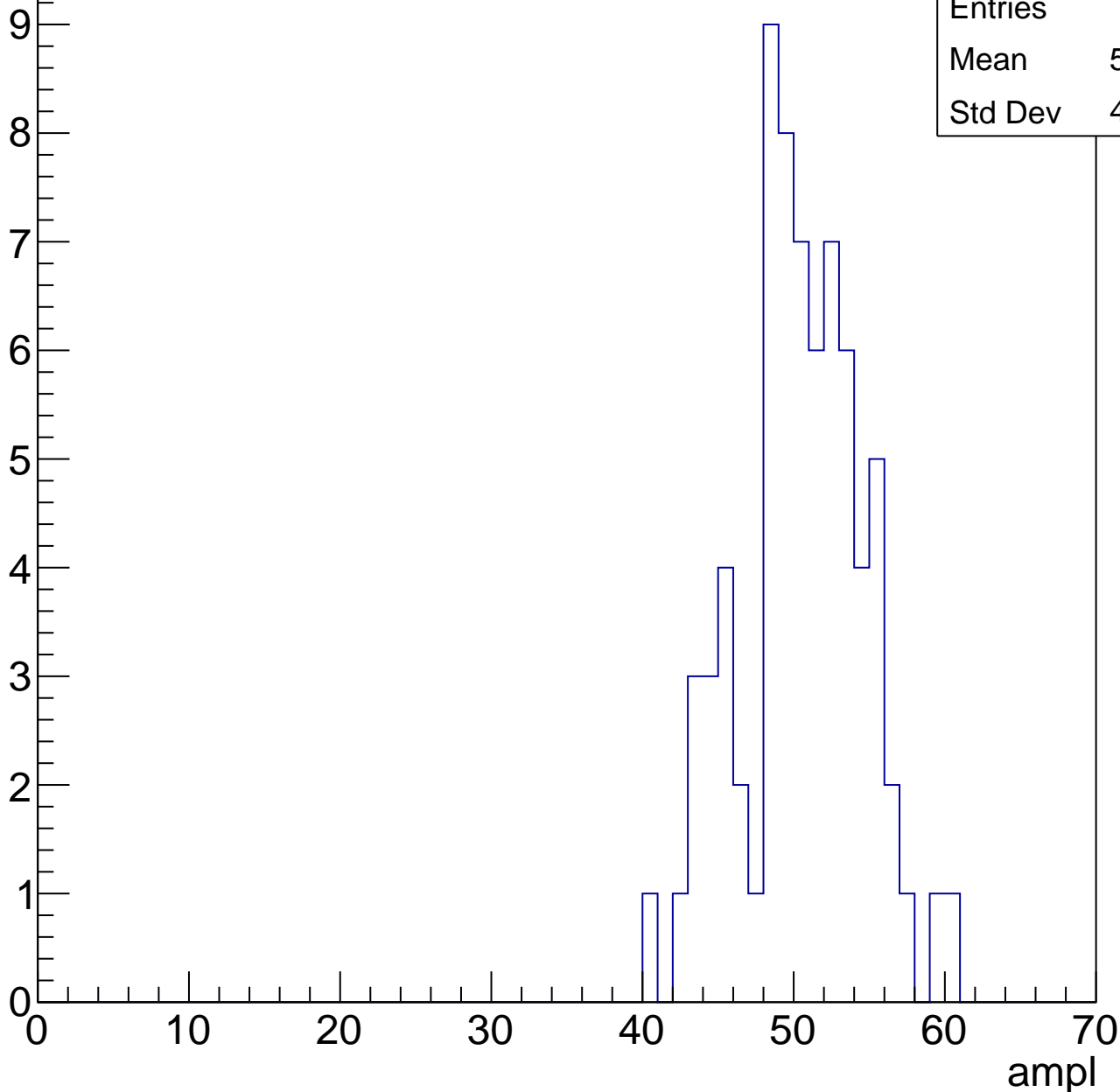


# B1L103S, U9-ch96, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	72
Mean	50.04
Std Dev	4.053

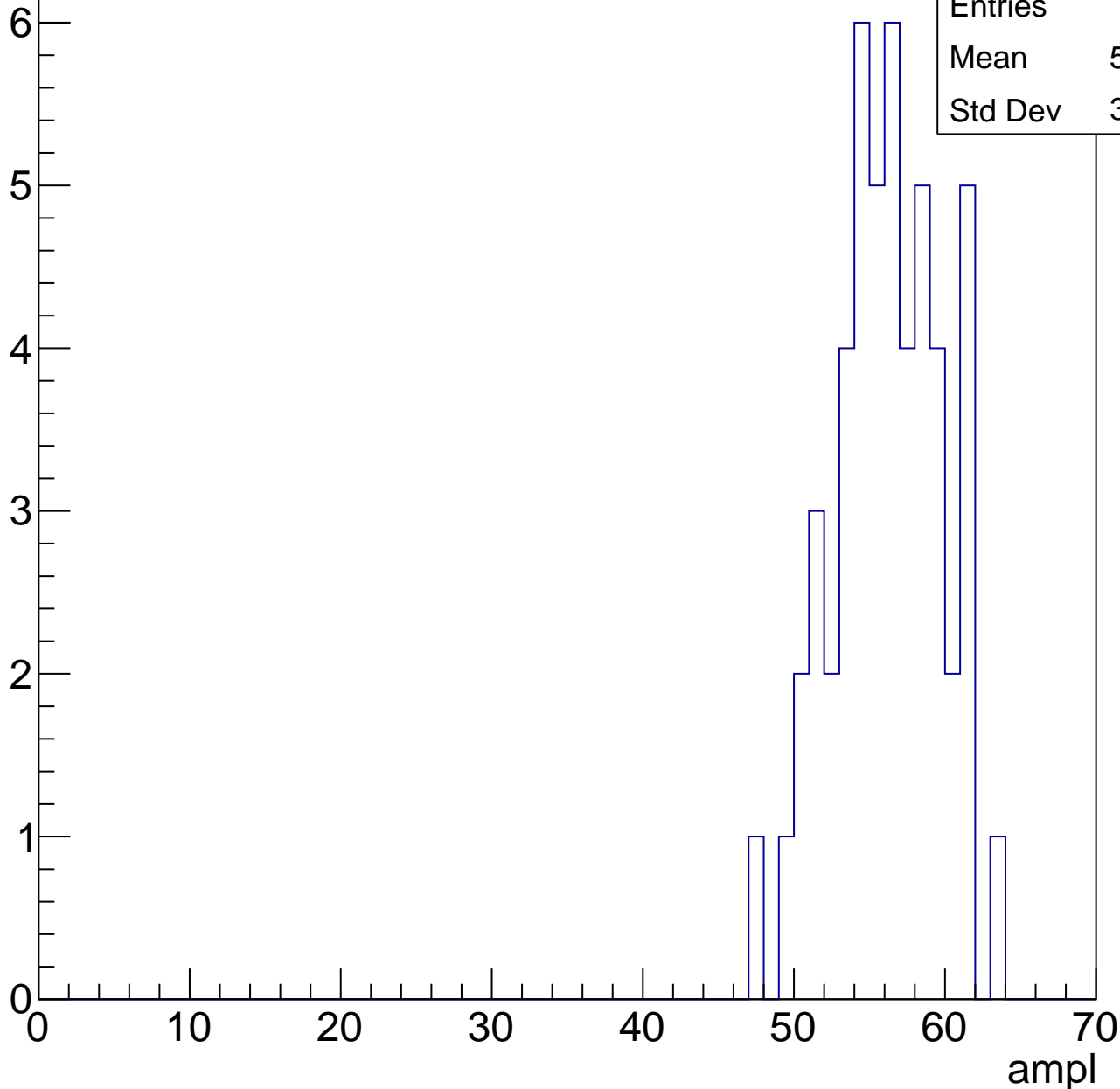


# B1L103S, U9-ch96, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	51
Mean	55.73
Std Dev	3.532

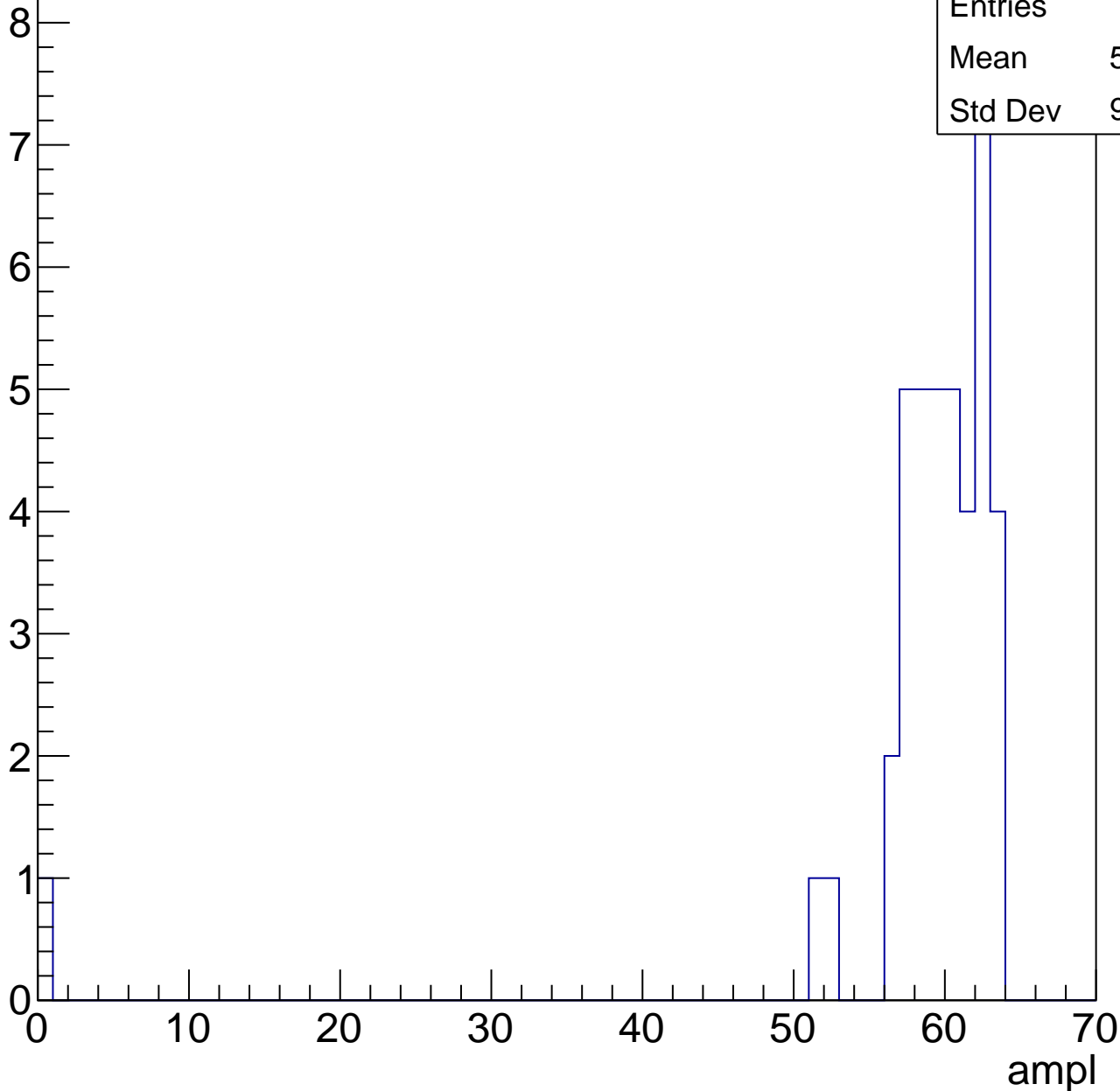


# B1L103S, U9-ch96, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

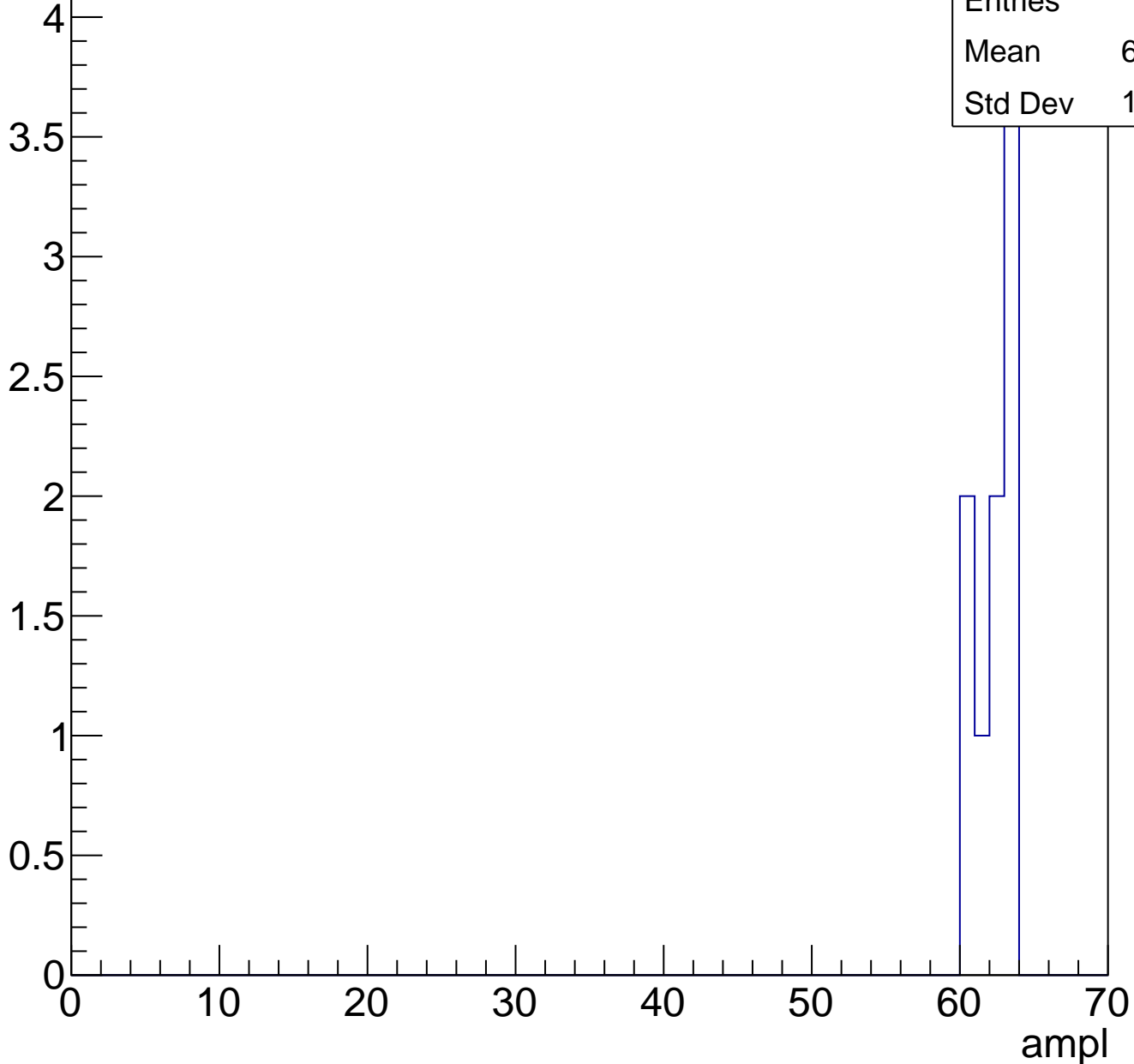
Entries	41
Mean	57.98
Std Dev	9.565



# B1L103S, U9-ch96, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

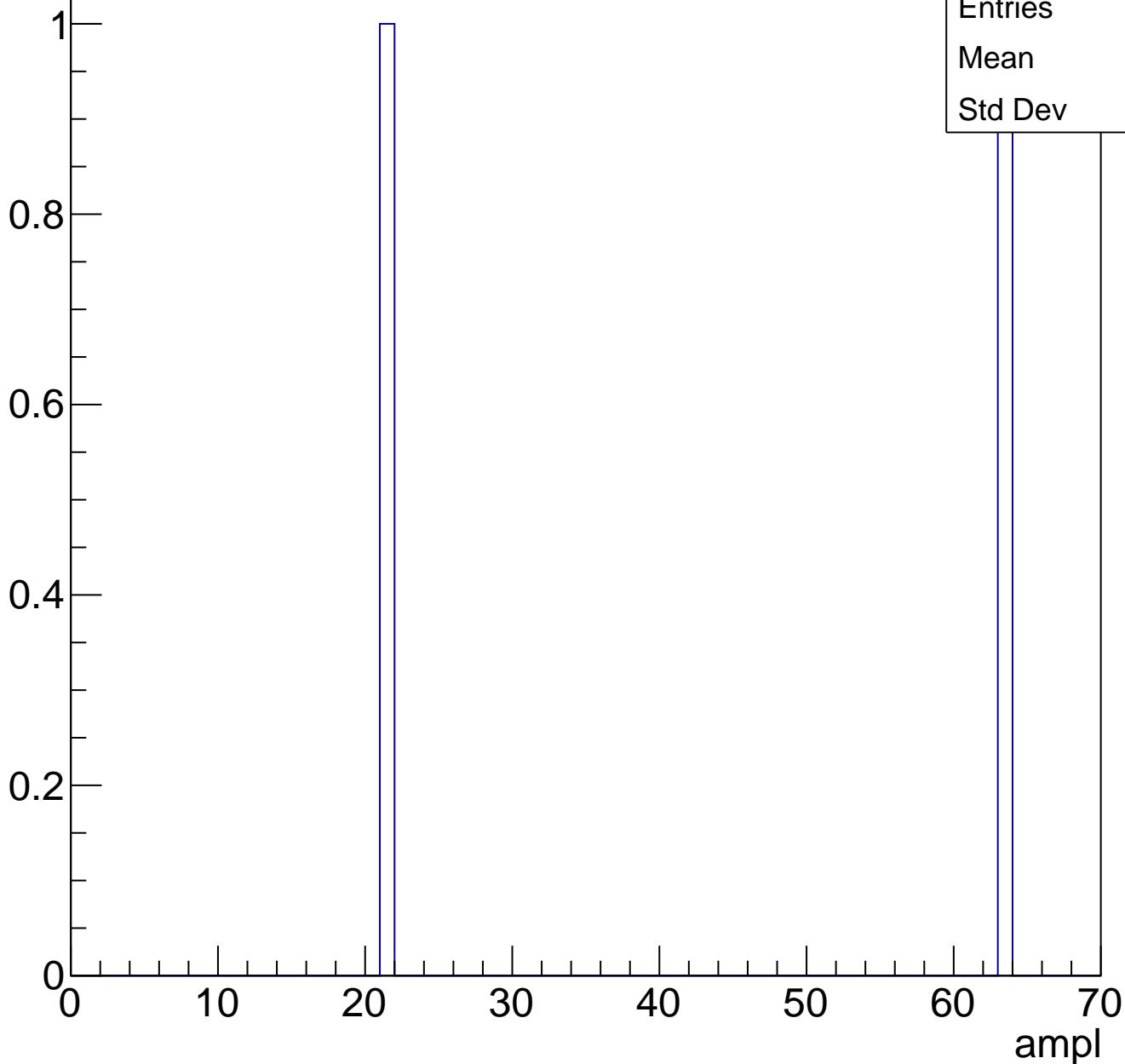




# B1L103S, U9-ch96, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U9-ch97, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	84
Mean	29.32
Std Dev	4.642

**Gaus mean : 30.1195**

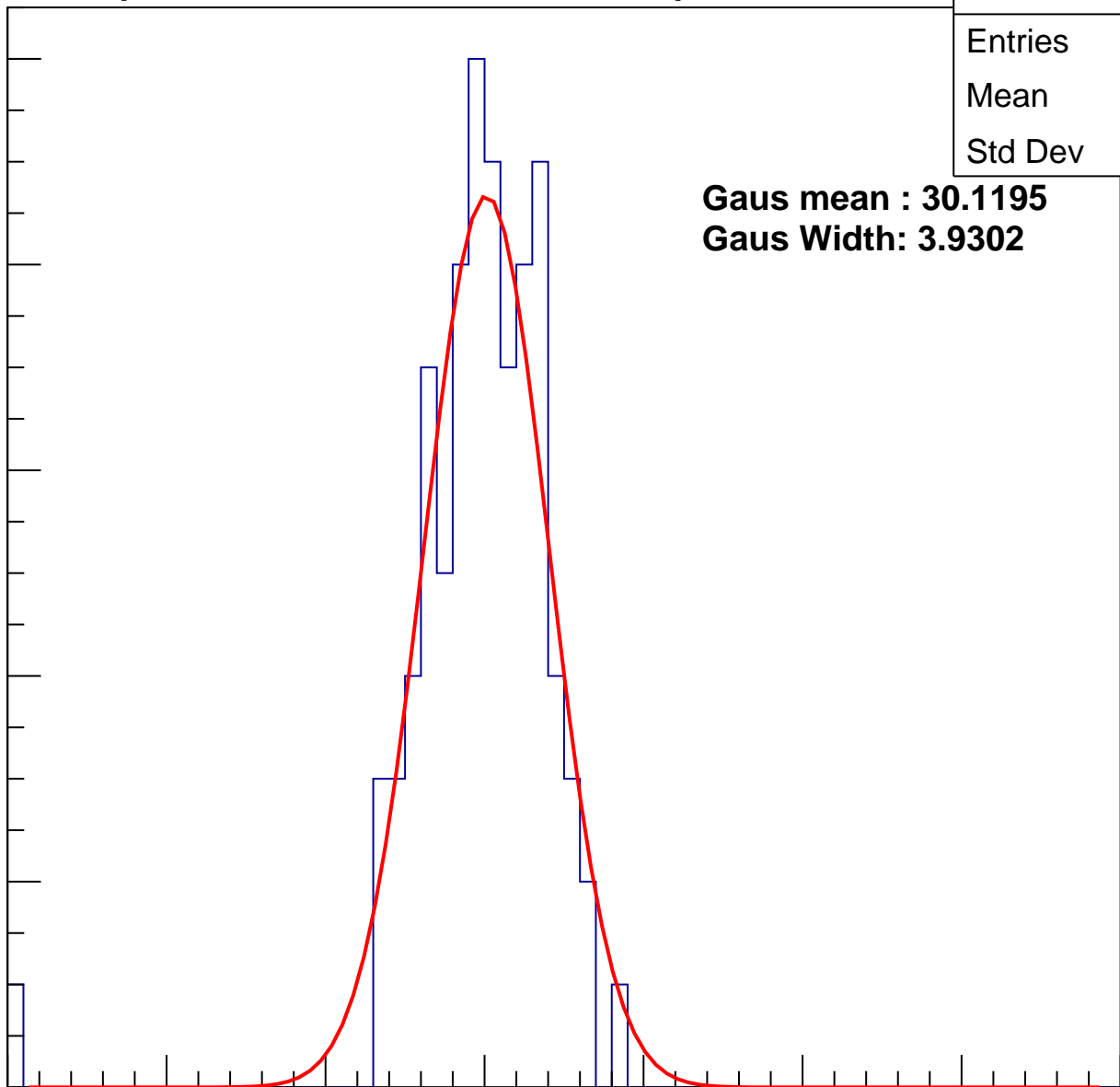
**Gaus Width: 3.9302**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U9-ch97, adc1

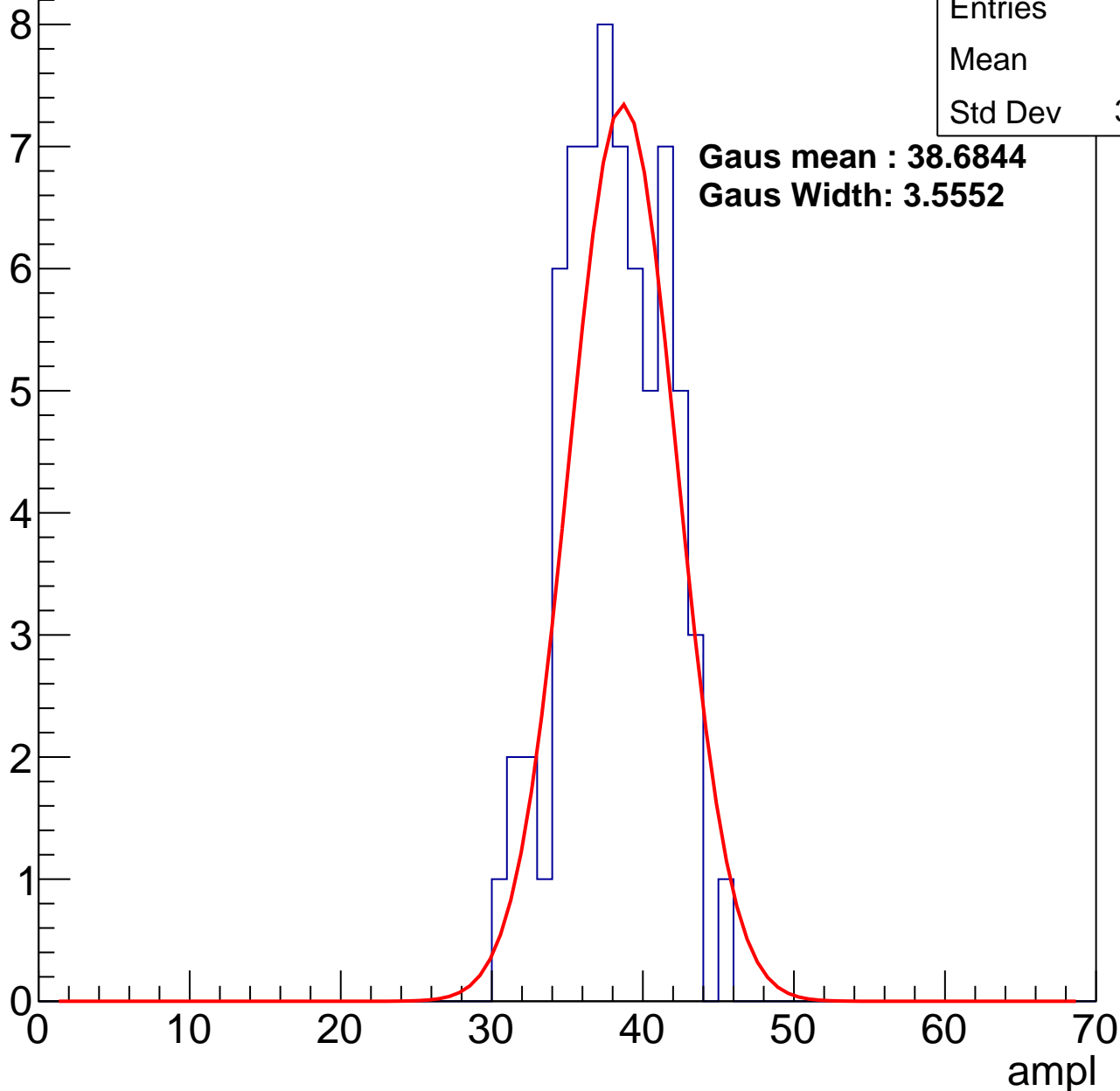
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	68
Mean	37.6
Std Dev	3.291

**Gaus mean : 38.6844**

**Gaus Width: 3.5552**



# B1L103S, U9-ch97, adc2

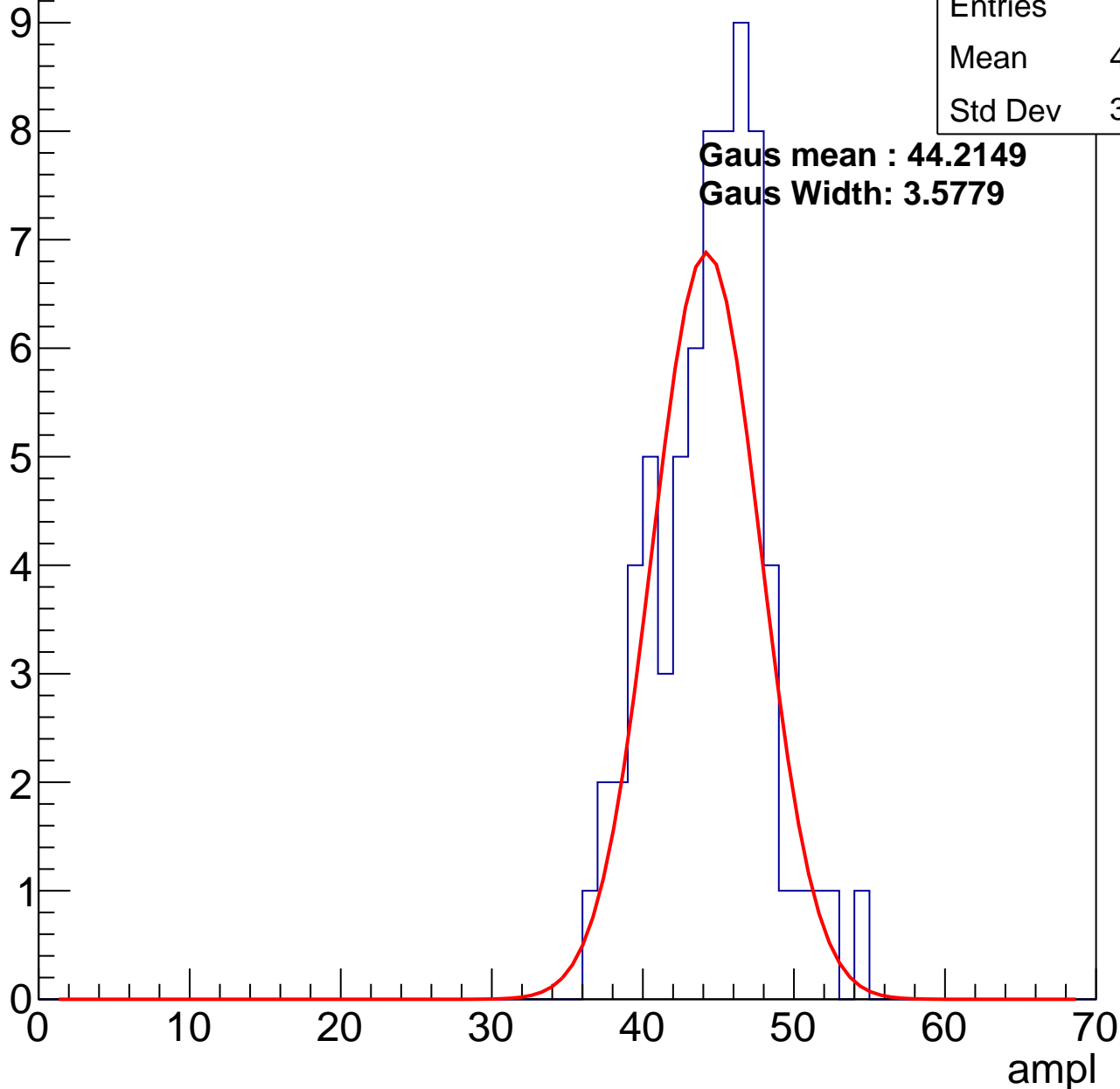
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	70
Mean	44.04
Std Dev	3.627

**Gaus mean : 44.2149**

**Gaus Width: 3.5779**

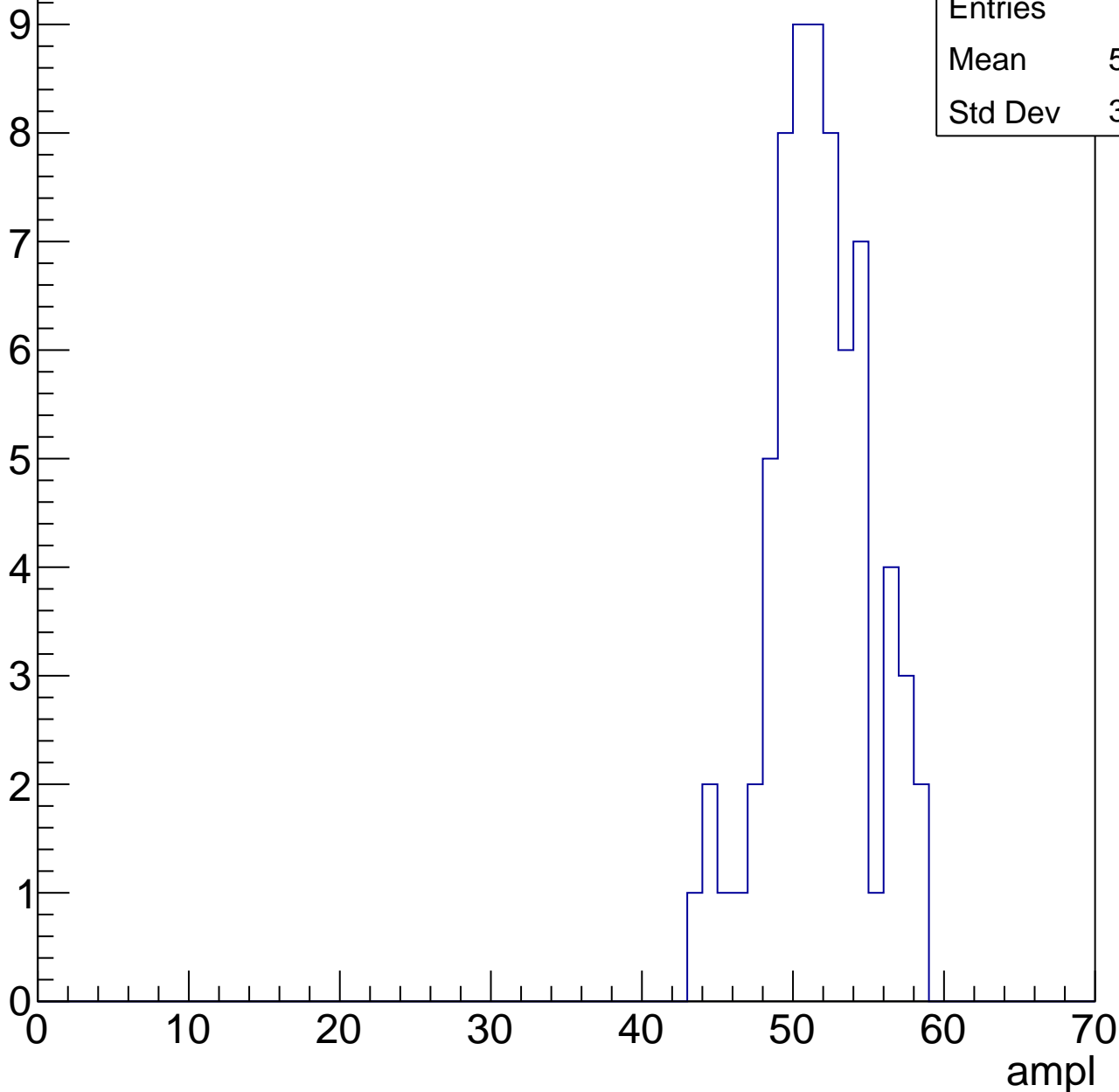


# B1L103S, U9-ch97, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

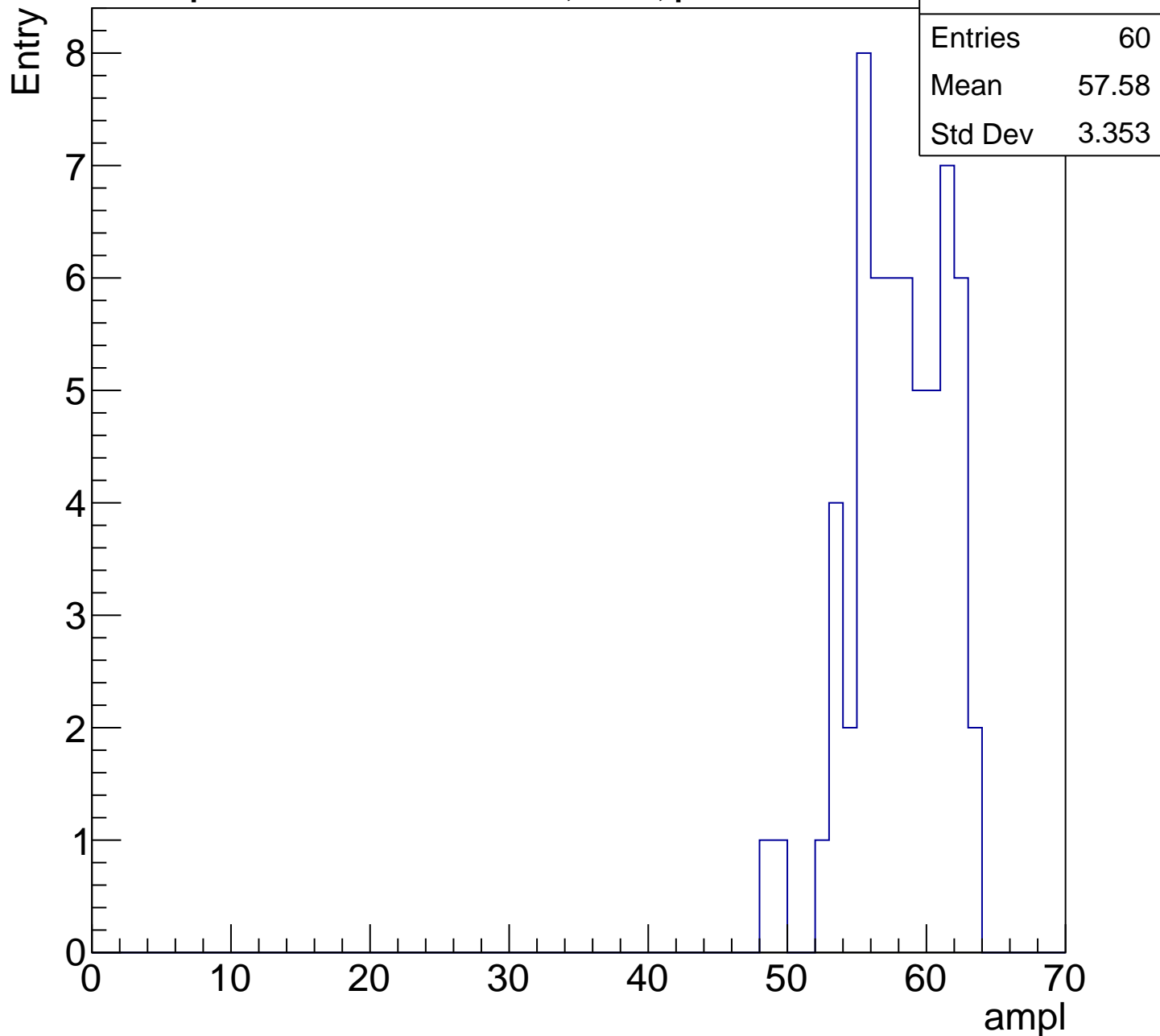
Entry

Entries	69
Mean	51.23
Std Dev	3.306



# B1L103S, U9-ch97, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

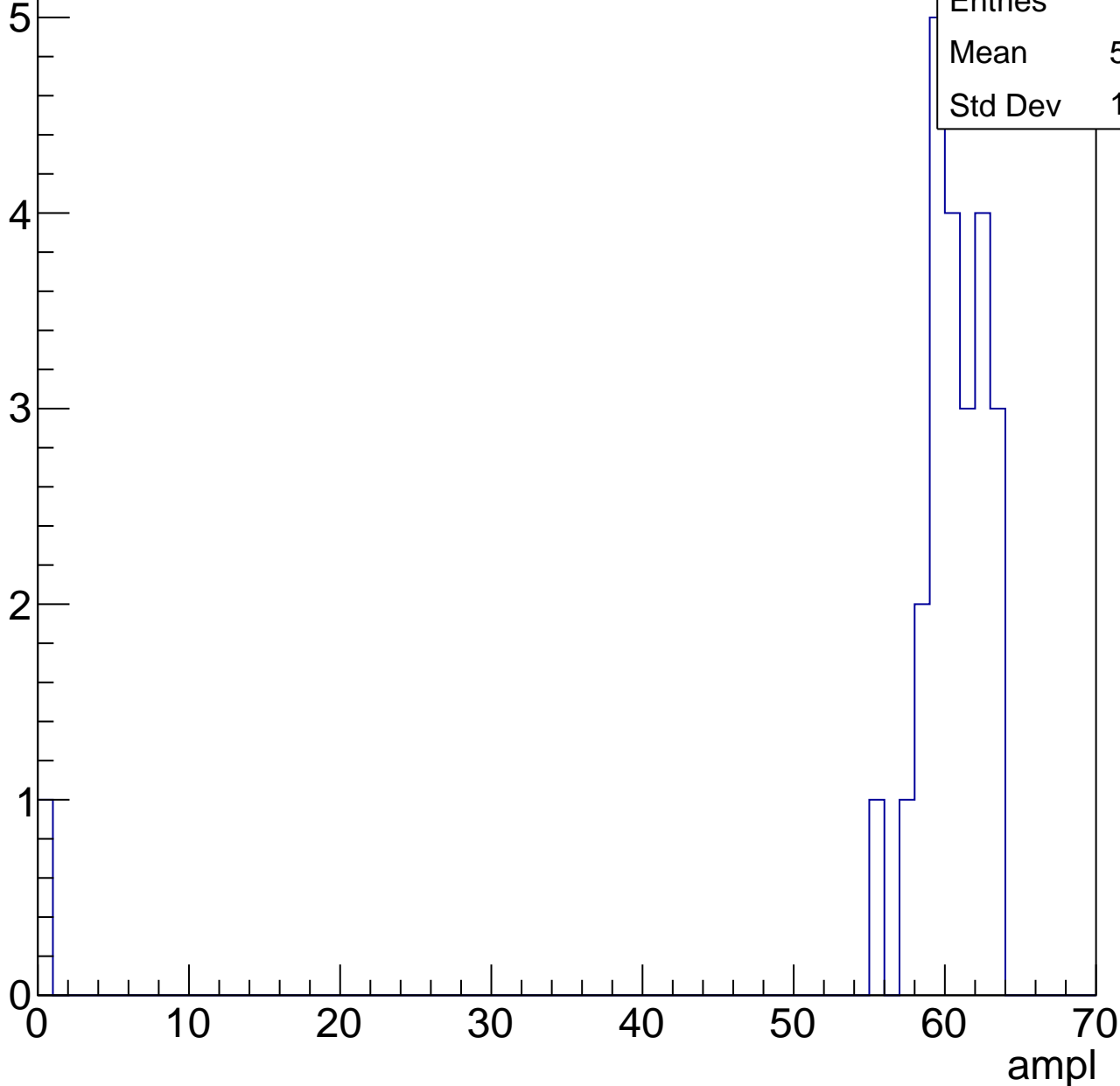


# B1L103S, U9-ch97, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	24
Mean	57.62
Std Dev	12.18

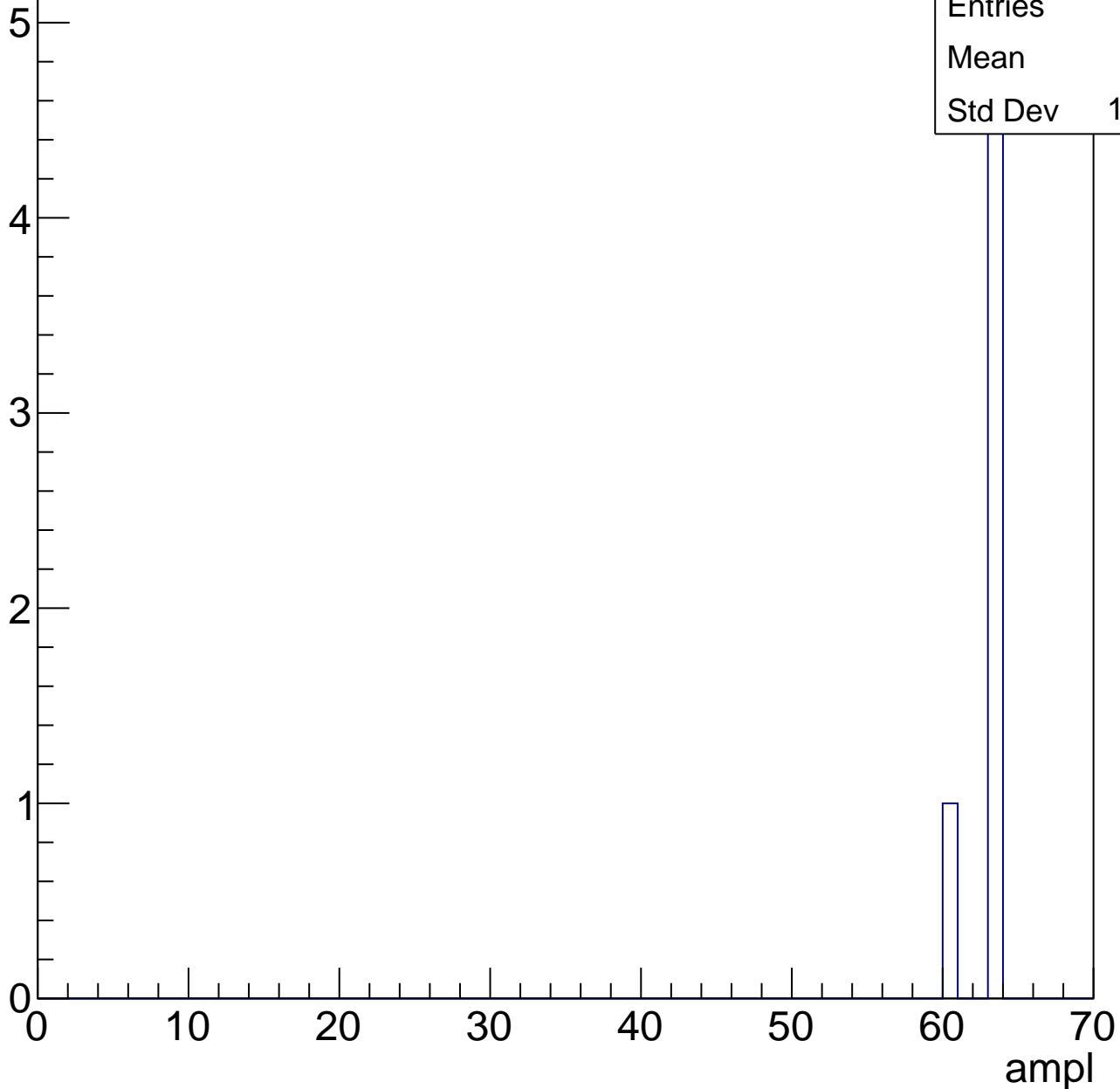


# B1L103S, U9-ch97, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	6
Mean	62.5
Std Dev	1.118





# B1L103S, U9-ch97, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U9-ch98, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	80
Mean	28.62
Std Dev	5.342

**Gaus mean : 29.7956**

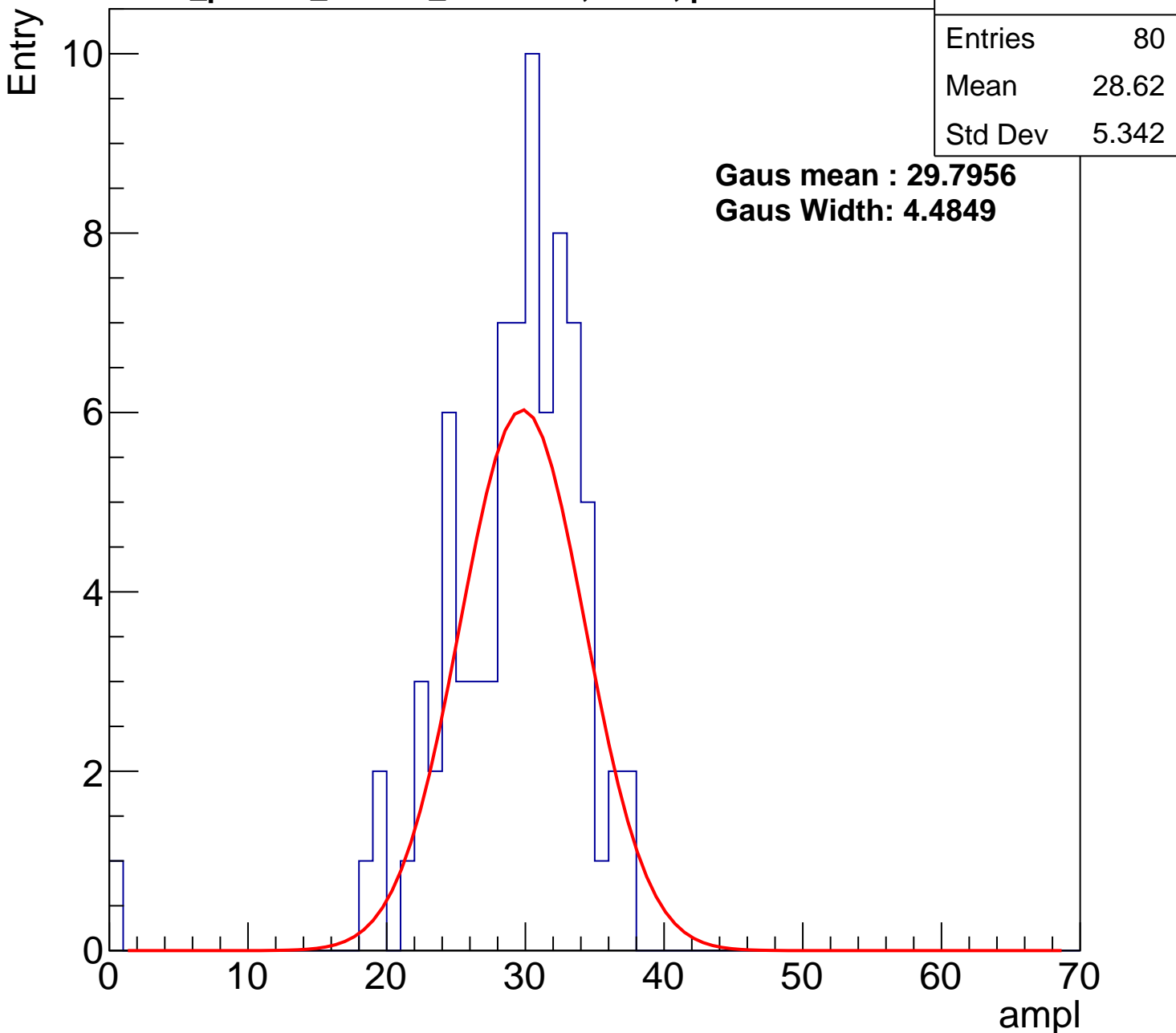
**Gaus Width: 4.4849**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U9-ch98, adc1

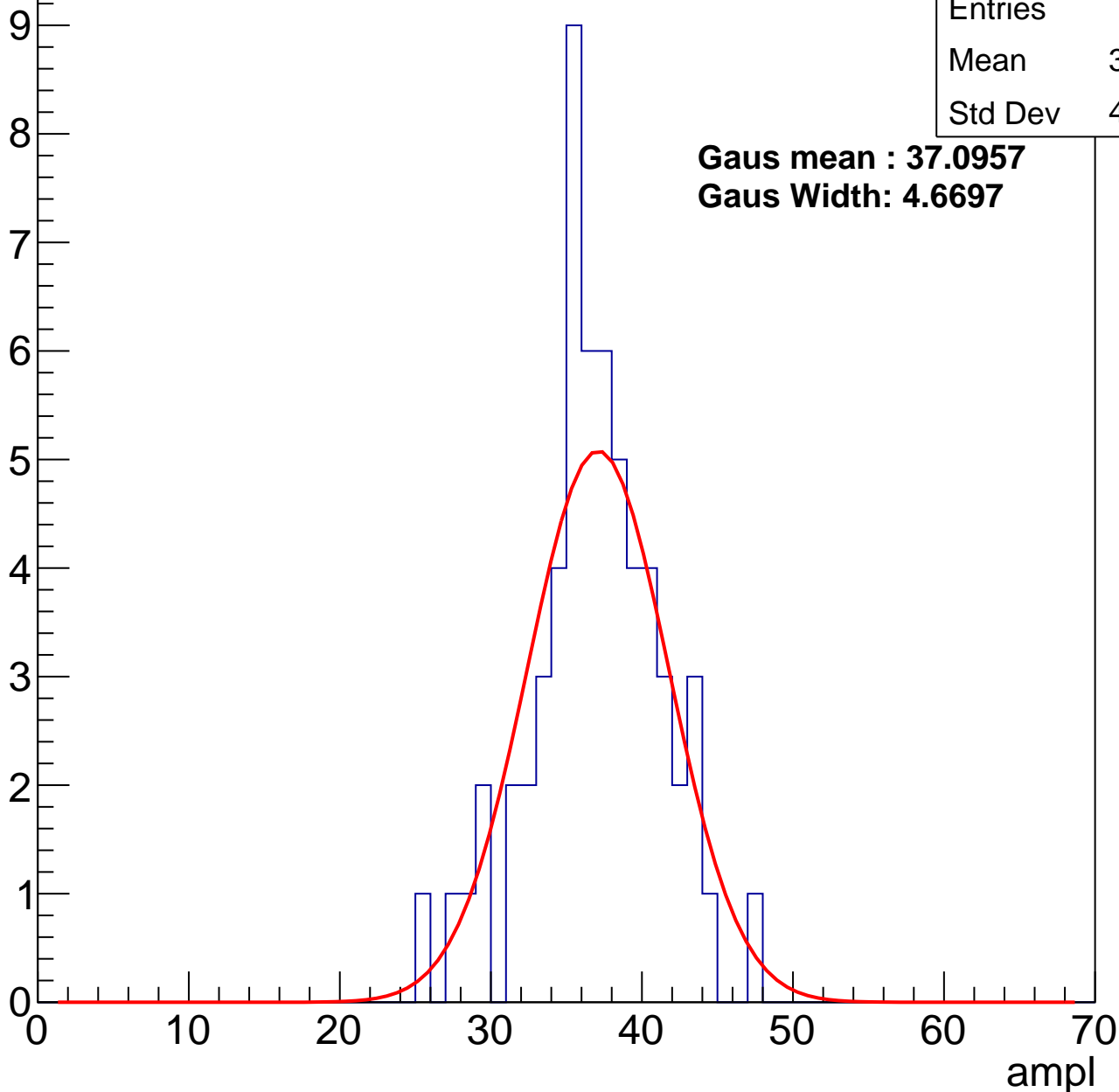
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	60
Mean	36.42
Std Dev	4.267

**Gaus mean : 37.0957**

**Gaus Width: 4.6697**



# B1L103S, U9-ch98, adc2

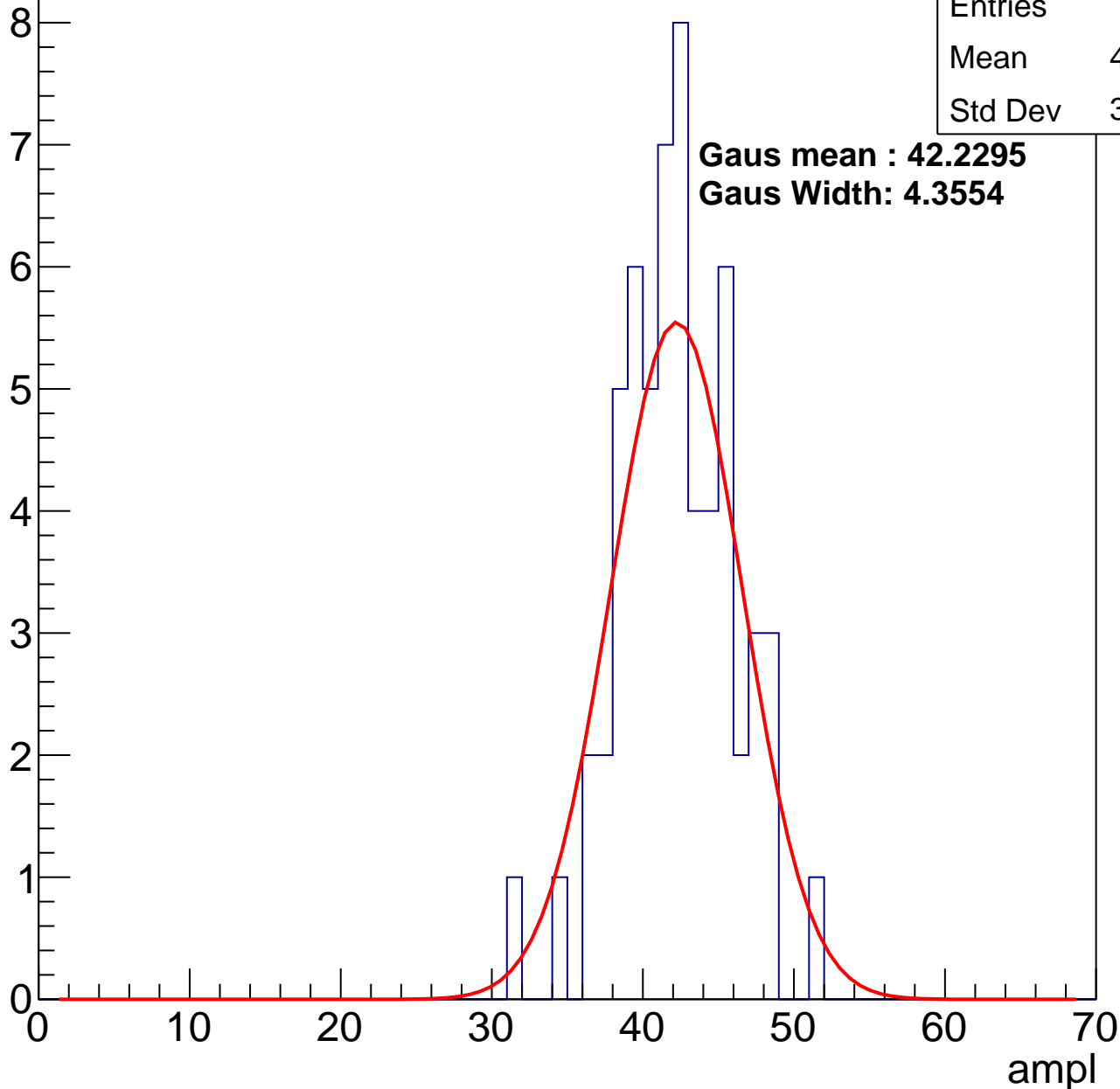
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	60
Mean	41.73
Std Dev	3.728

**Gaus mean : 42.2295**

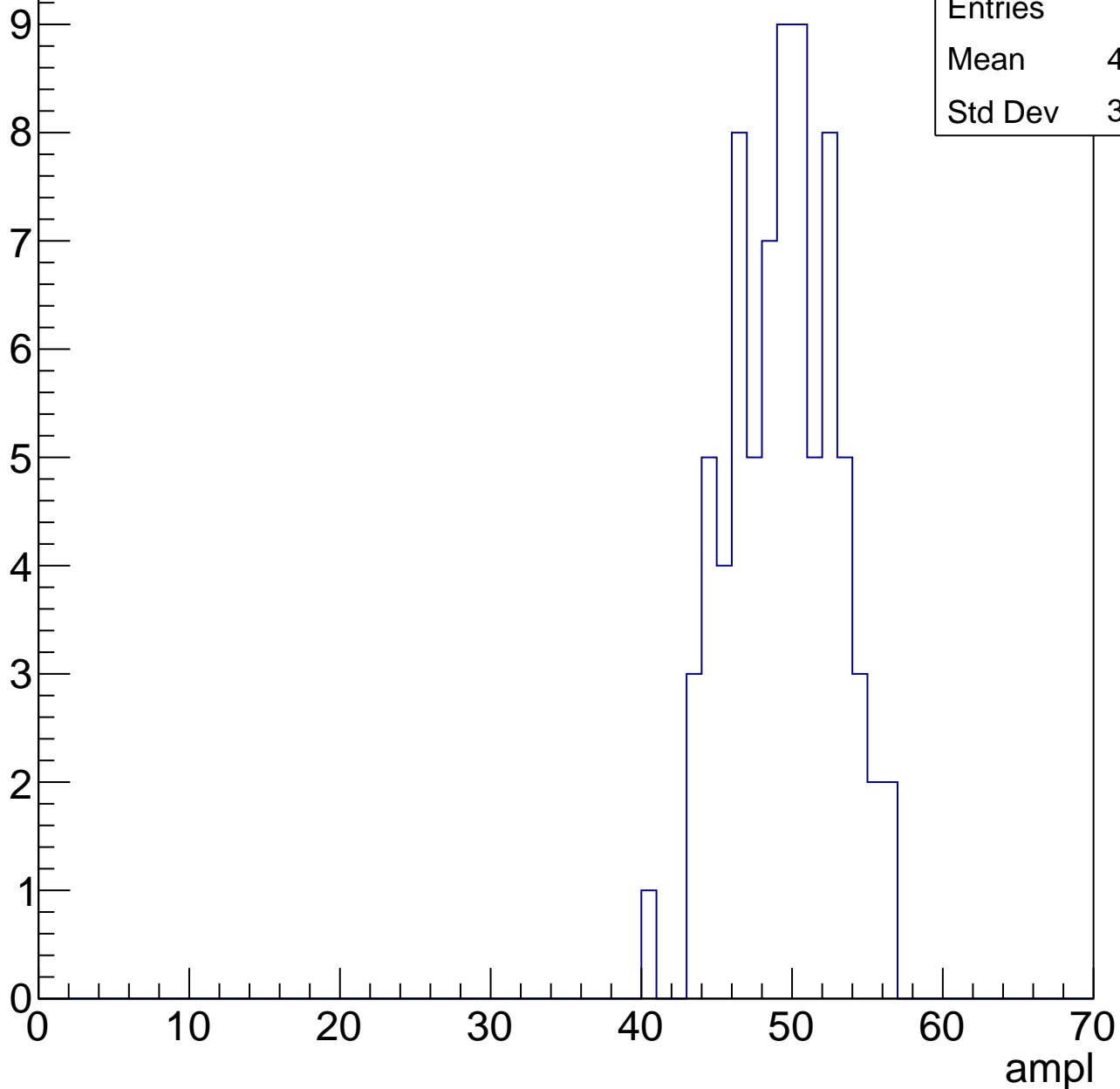
**Gaus Width: 4.3554**



# B1L103S, U9-ch98, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

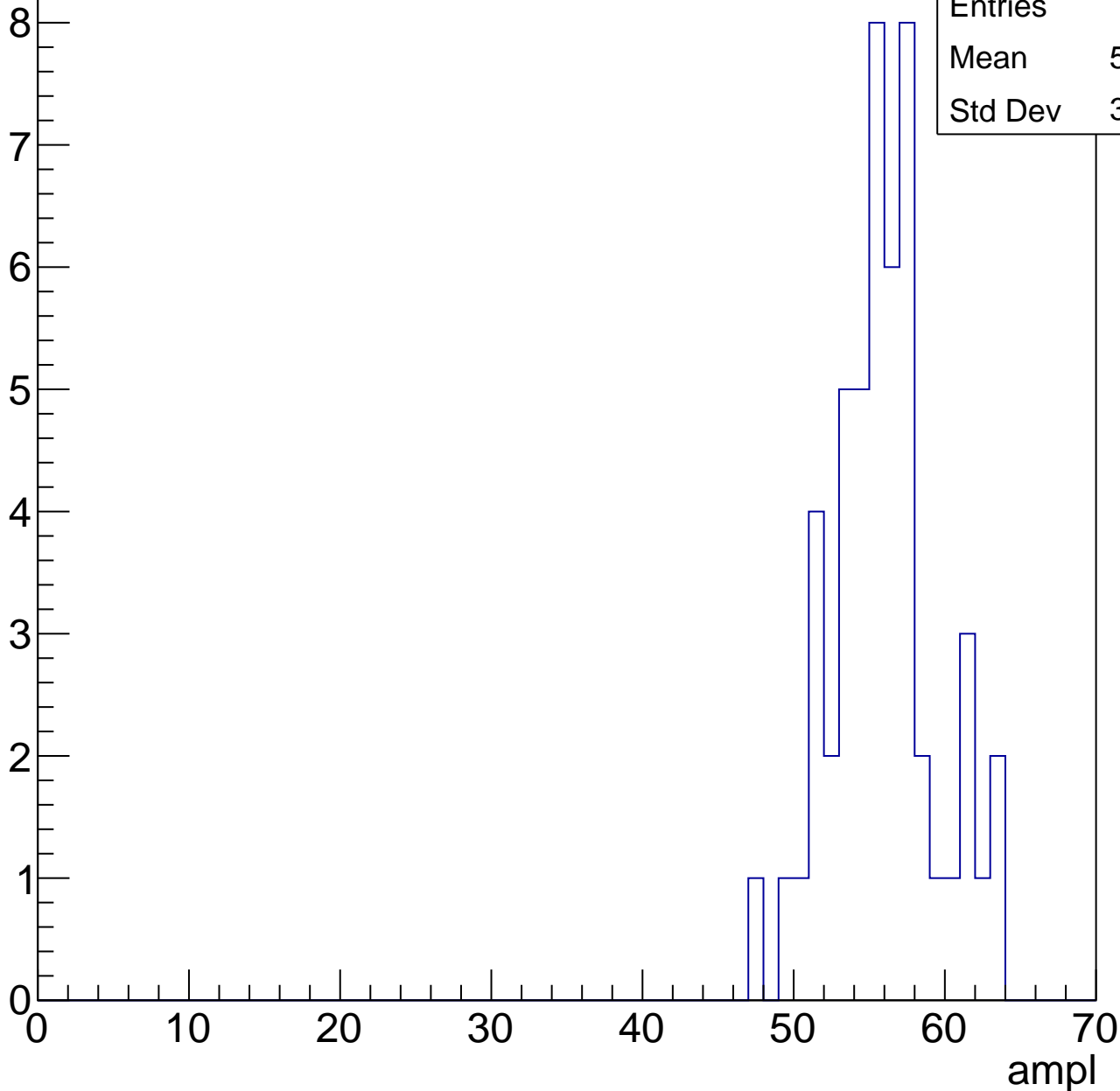


# B1L103S, U9-ch98, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

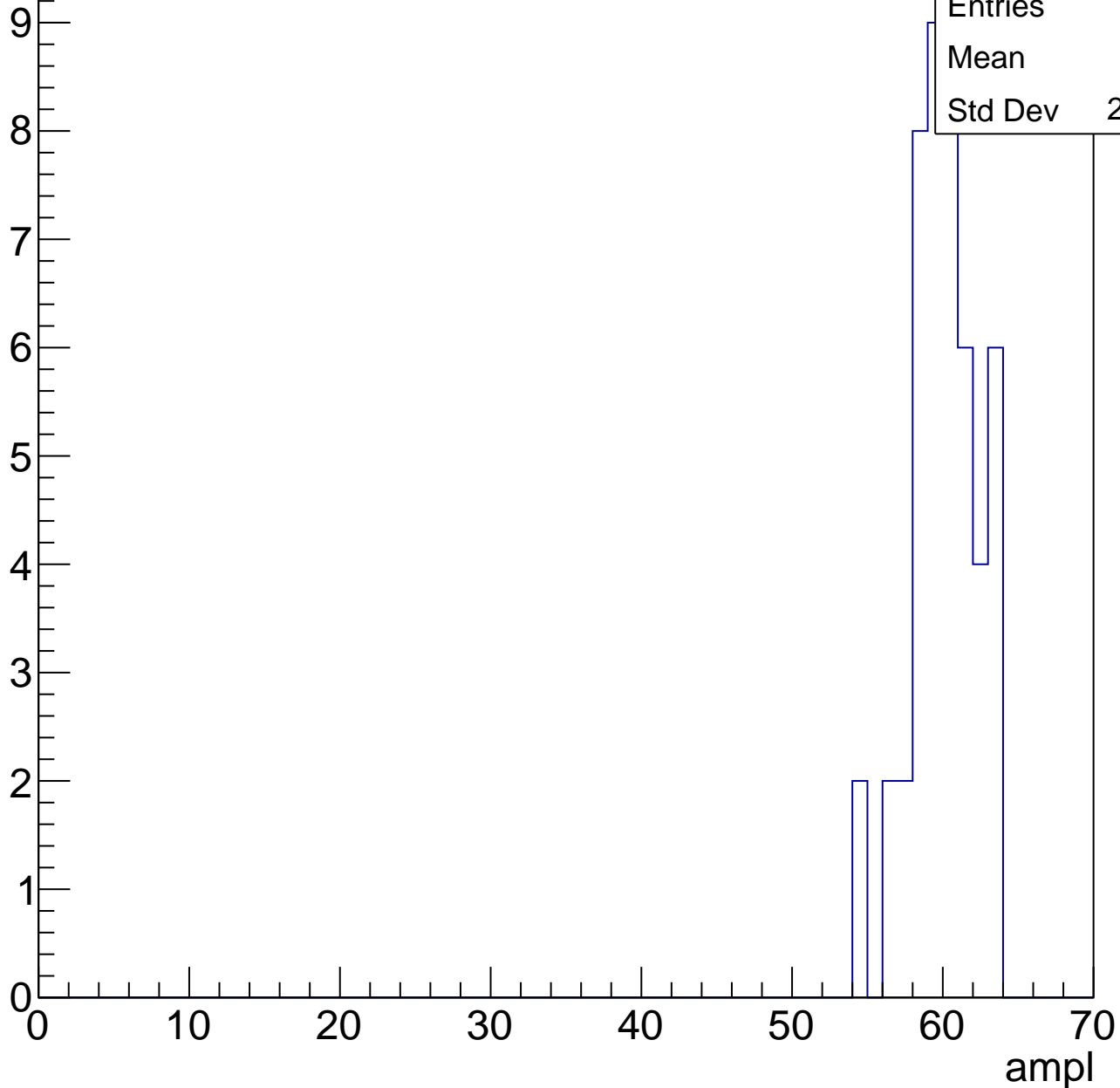
Entries	51
Mean	55.43
Std Dev	3.443



# B1L103S, U9-ch98, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

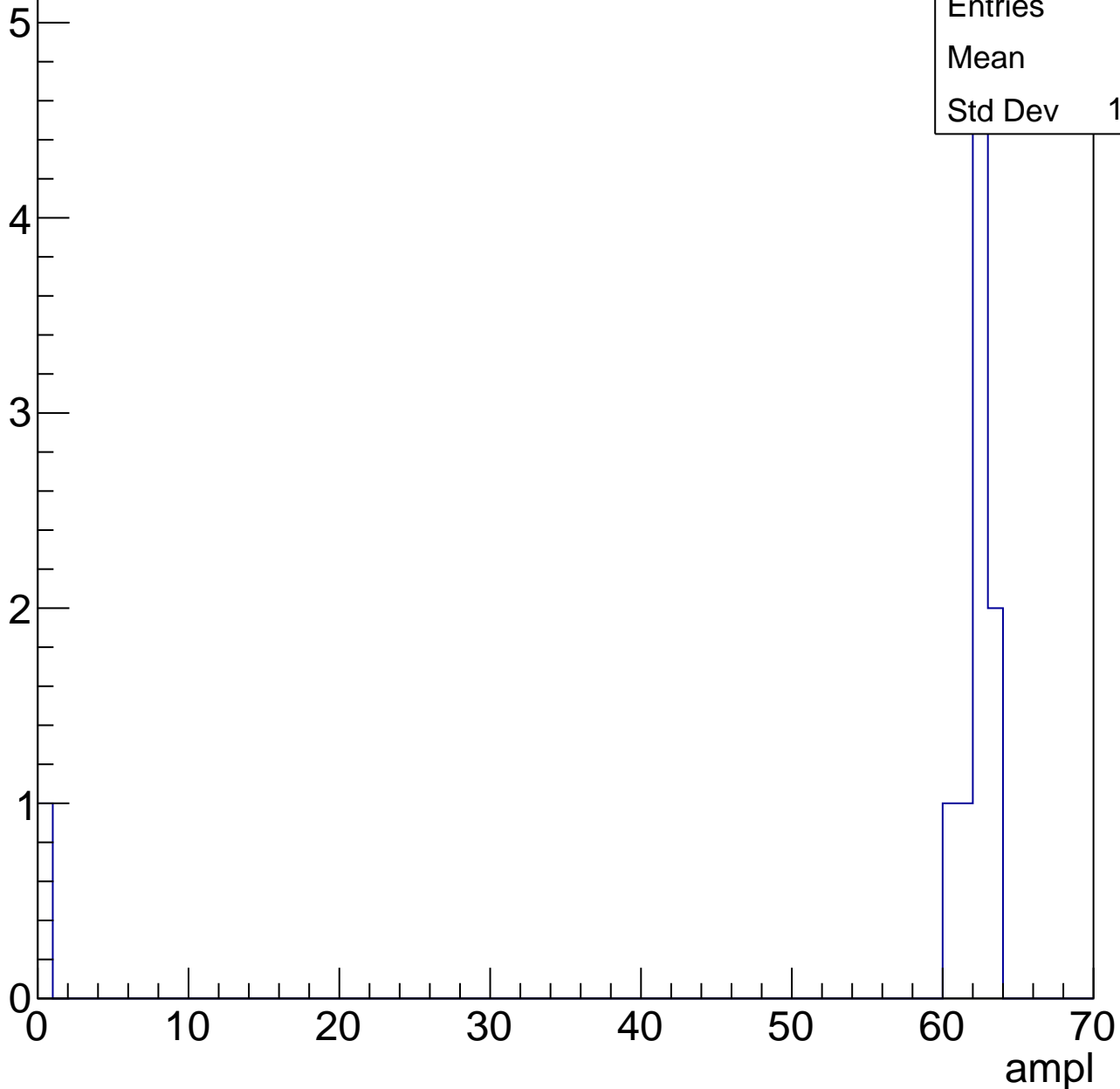


# B1L103S, U9-ch98, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	10
Mean	55.7
Std Dev	18.59





# B1L103S, U9-ch98, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U9-ch99, adc0

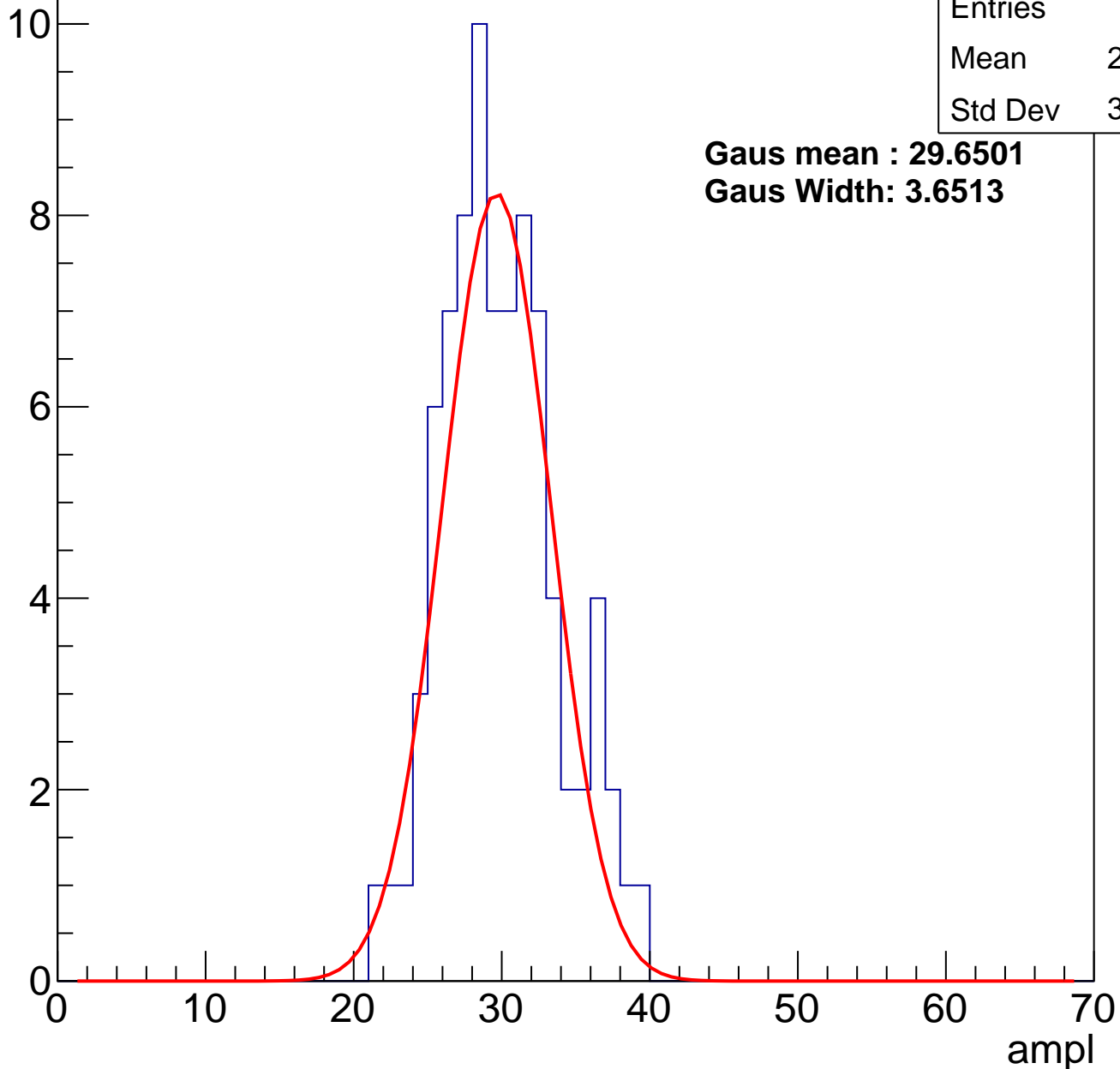
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	82
Mean	29.46
Std Dev	3.826

**Gaus mean : 29.6501**

**Gaus Width: 3.6513**

Entry



# B1L103S, U9-ch99, adc1

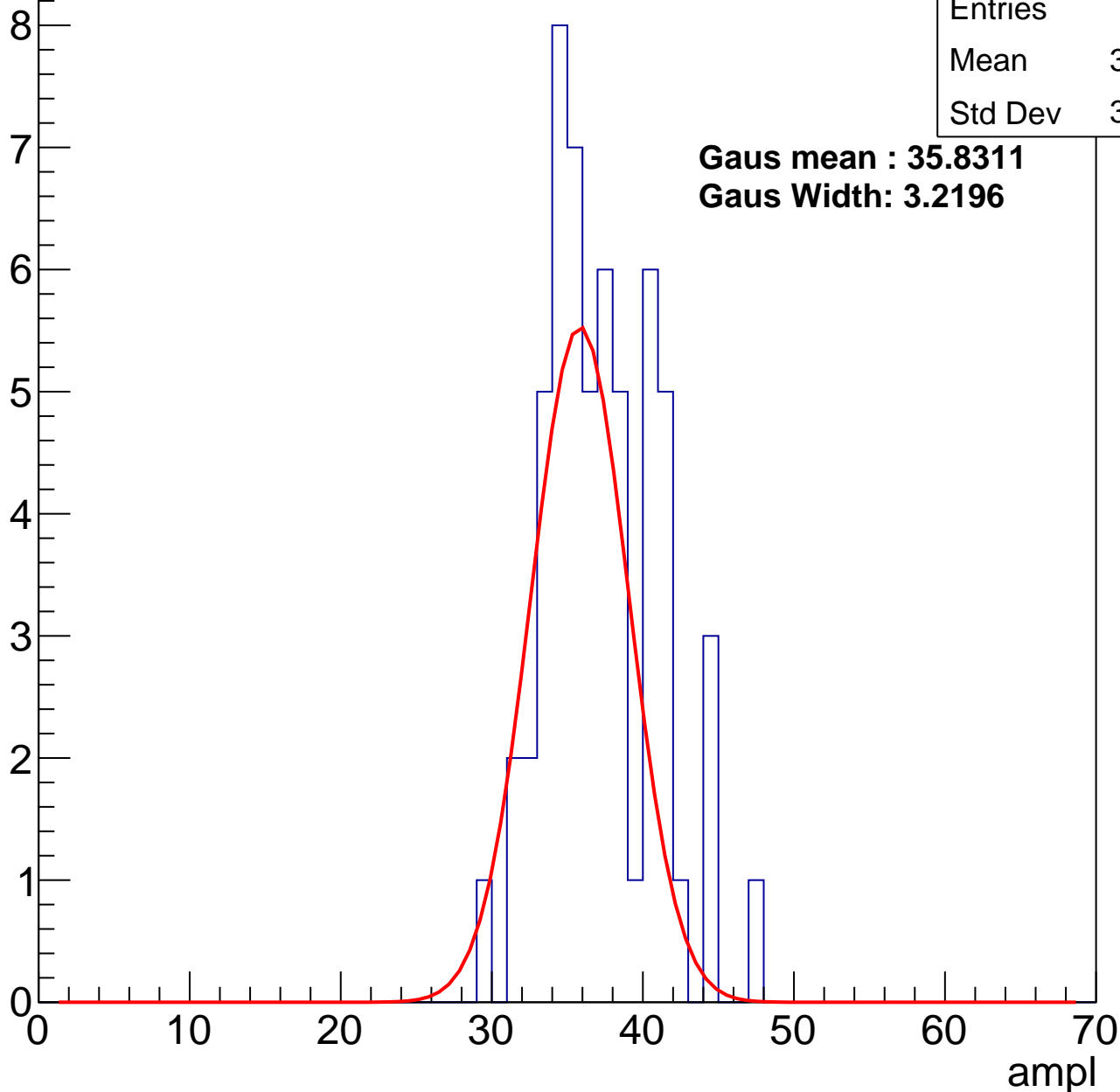
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	58
Mean	36.79
Std Dev	3.675

**Gaus mean : 35.8311**

**Gaus Width: 3.2196**



# B1L103S, U9-ch99, adc2

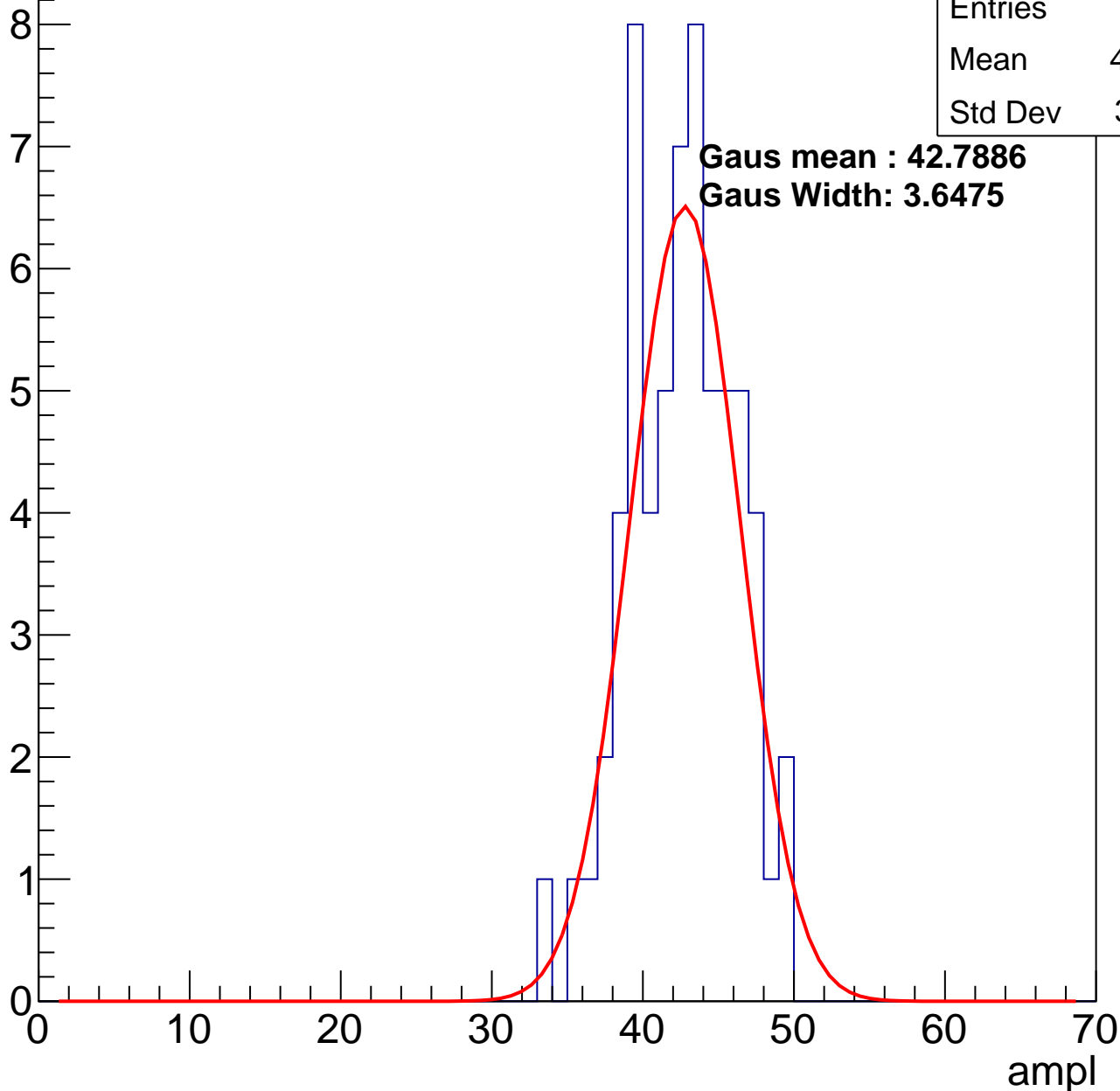
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	42.13
Std Dev	3.471

**Gaus mean : 42.7886**

**Gaus Width: 3.6475**

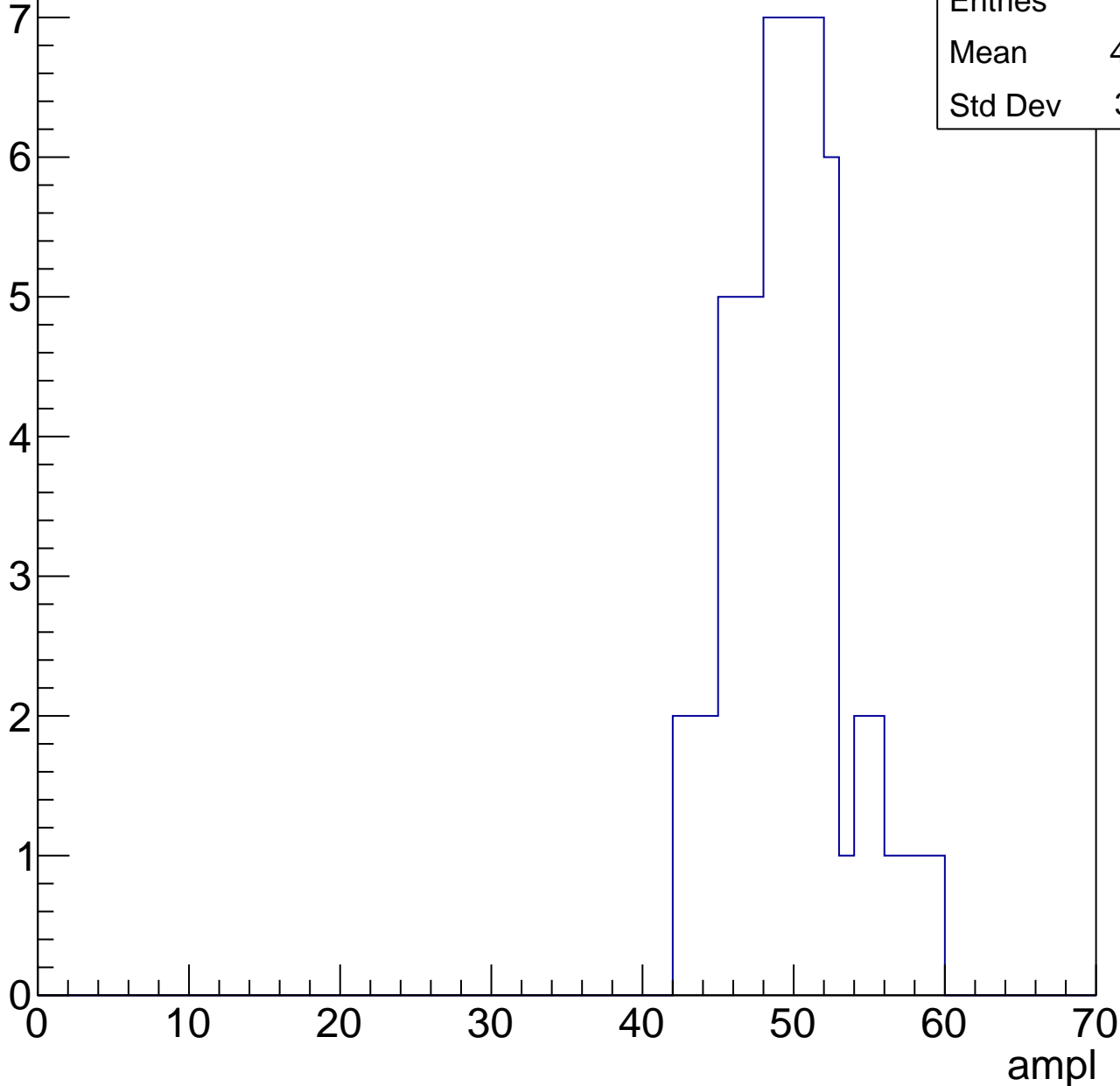


# B1L103S, U9-ch99, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	49.17
Std Dev	3.731

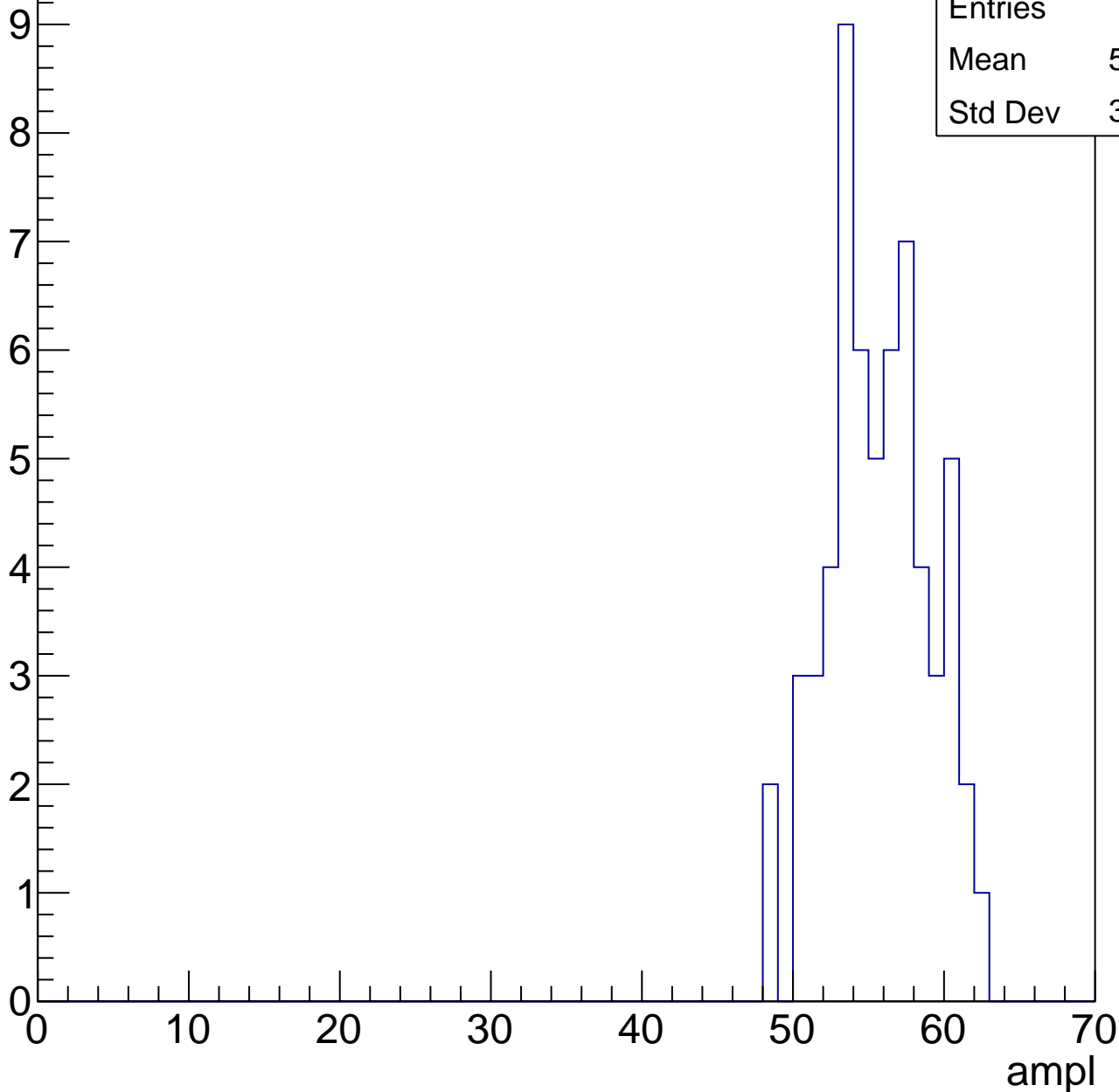


# B1L103S, U9-ch99, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	60
Mean	55.18
Std Dev	3.319



# B1L103S, U9-ch99, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

7

6

5

4

3

2

1

0

Entries

46

Mean

57.87

Std Dev

9.121

ampl

0

10

20

30

40

50

60

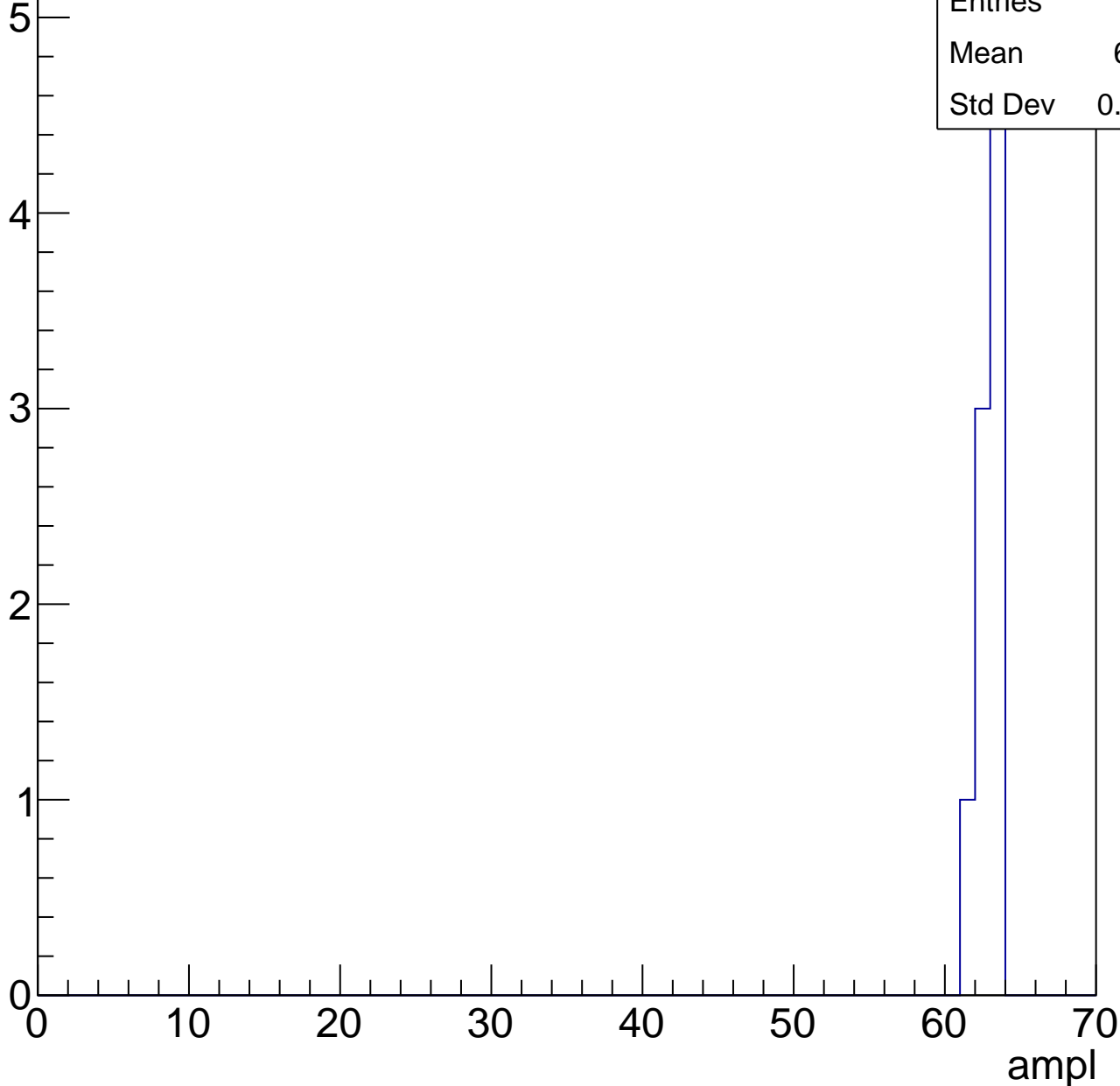
70

# B1L103S, U9-ch99, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	9
Mean	62.44
Std Dev	0.6849





# B1L103S, U9-ch99, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U9-ch100, adc0

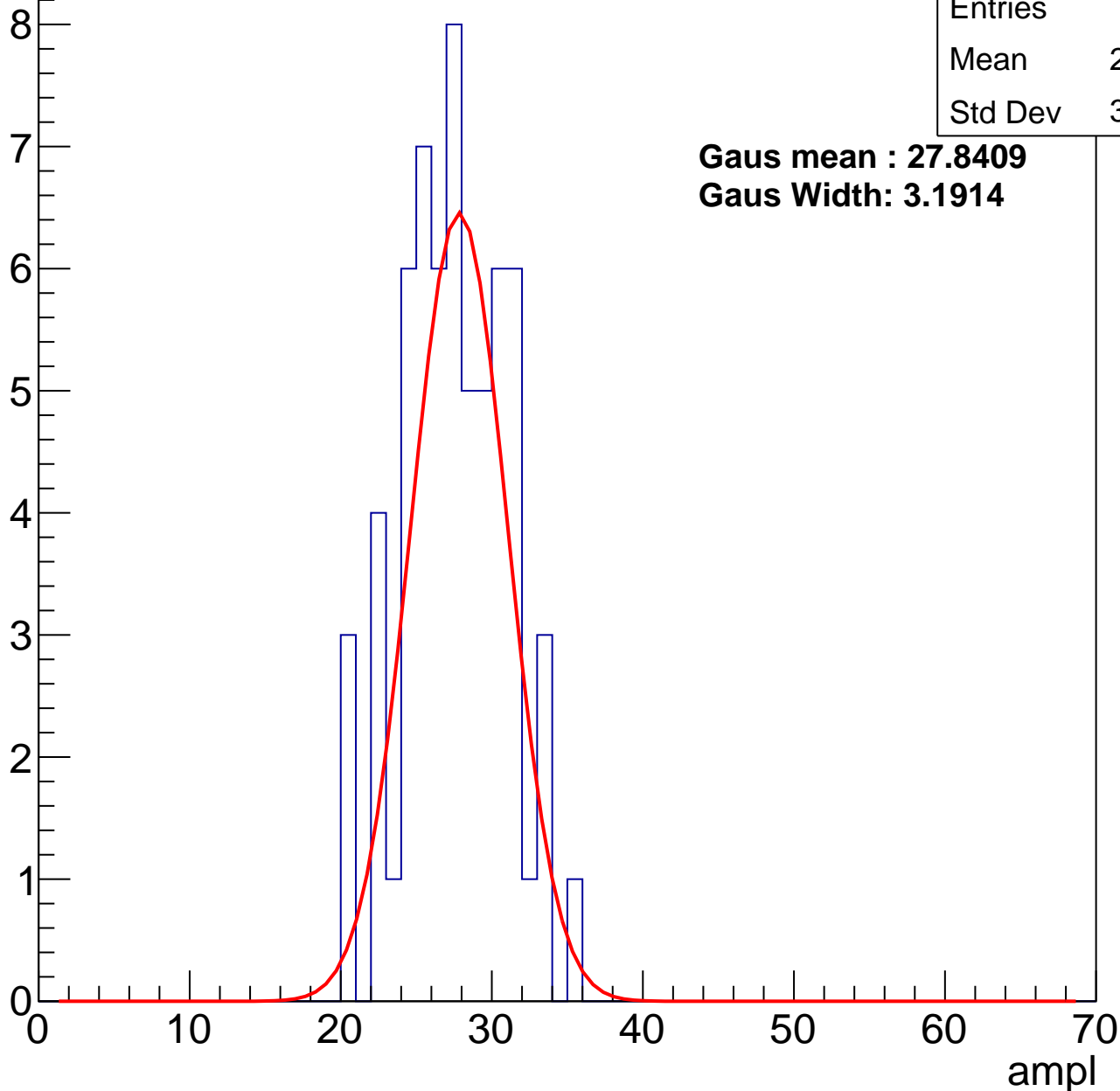
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	27.08
Std Dev	3.414

**Gaus mean : 27.8409**

**Gaus Width: 3.1914**



# B1L103S, U9-ch100, adc1

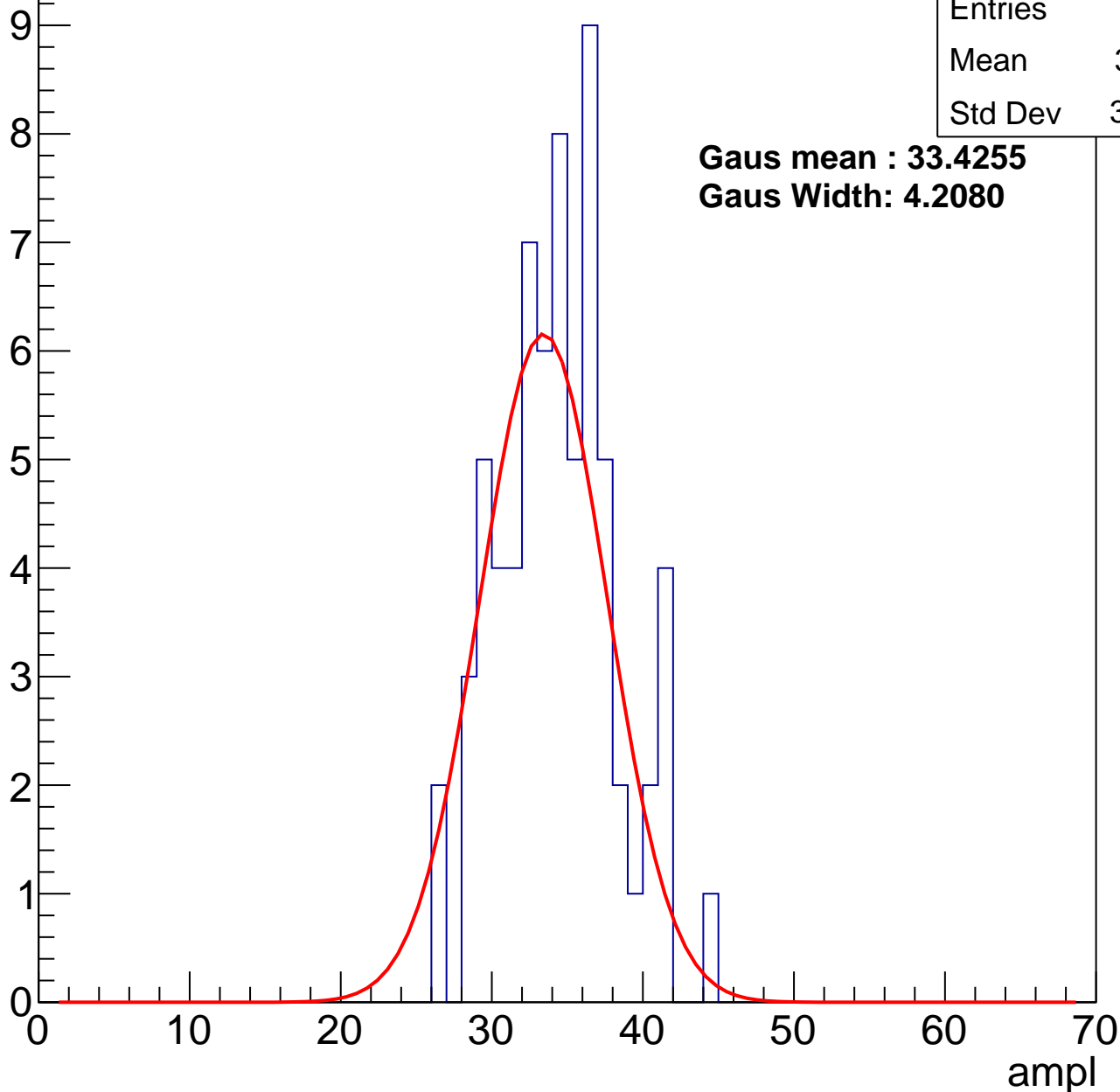
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	68
Mean	33.91
Std Dev	3.845

**Gaus mean : 33.4255**

**Gaus Width: 4.2080**



# B1L103S, U9-ch100, adc2

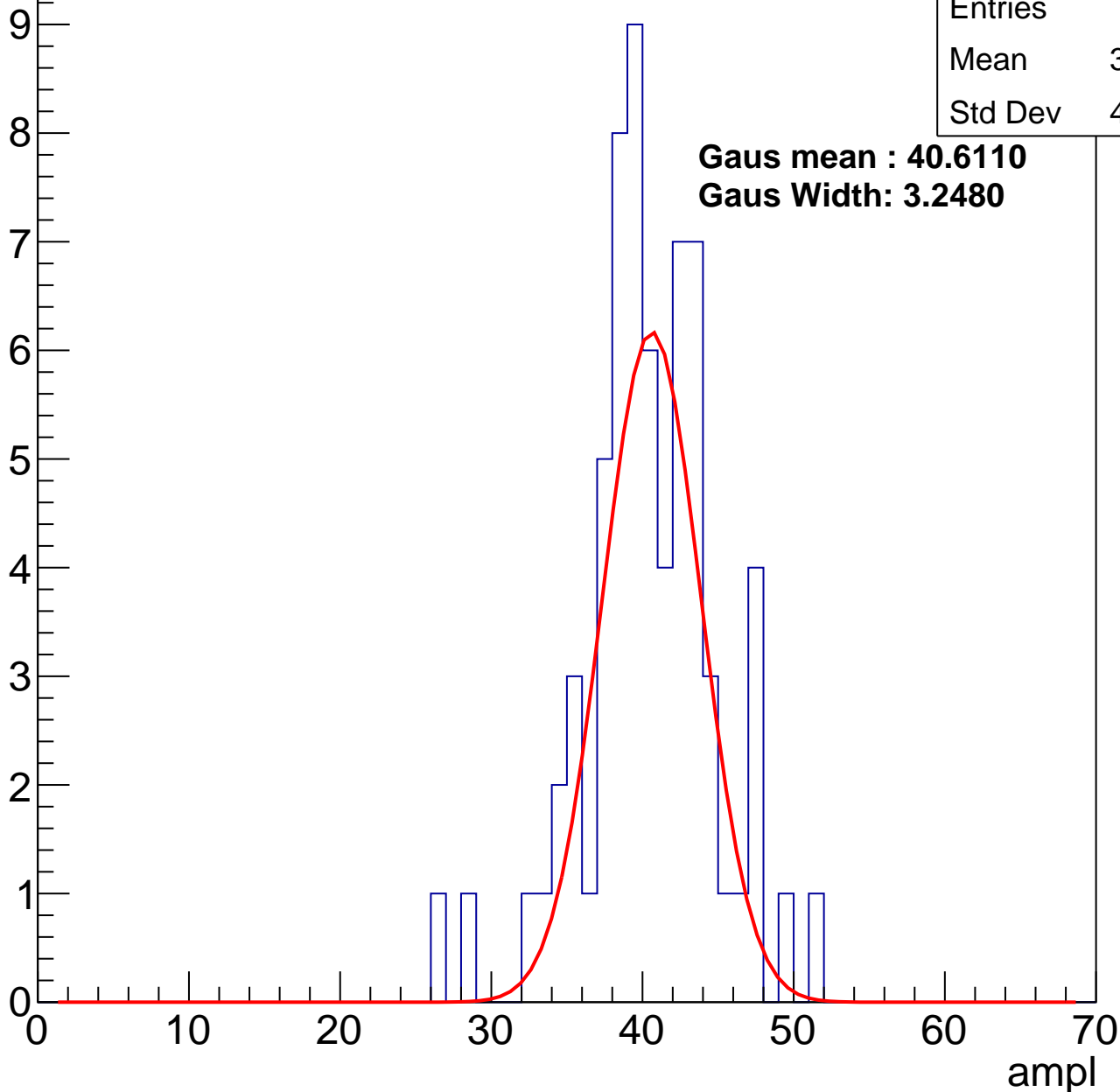
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	39.97
Std Dev	4.412

**Gaus mean : 40.6110**

**Gaus Width: 3.2480**

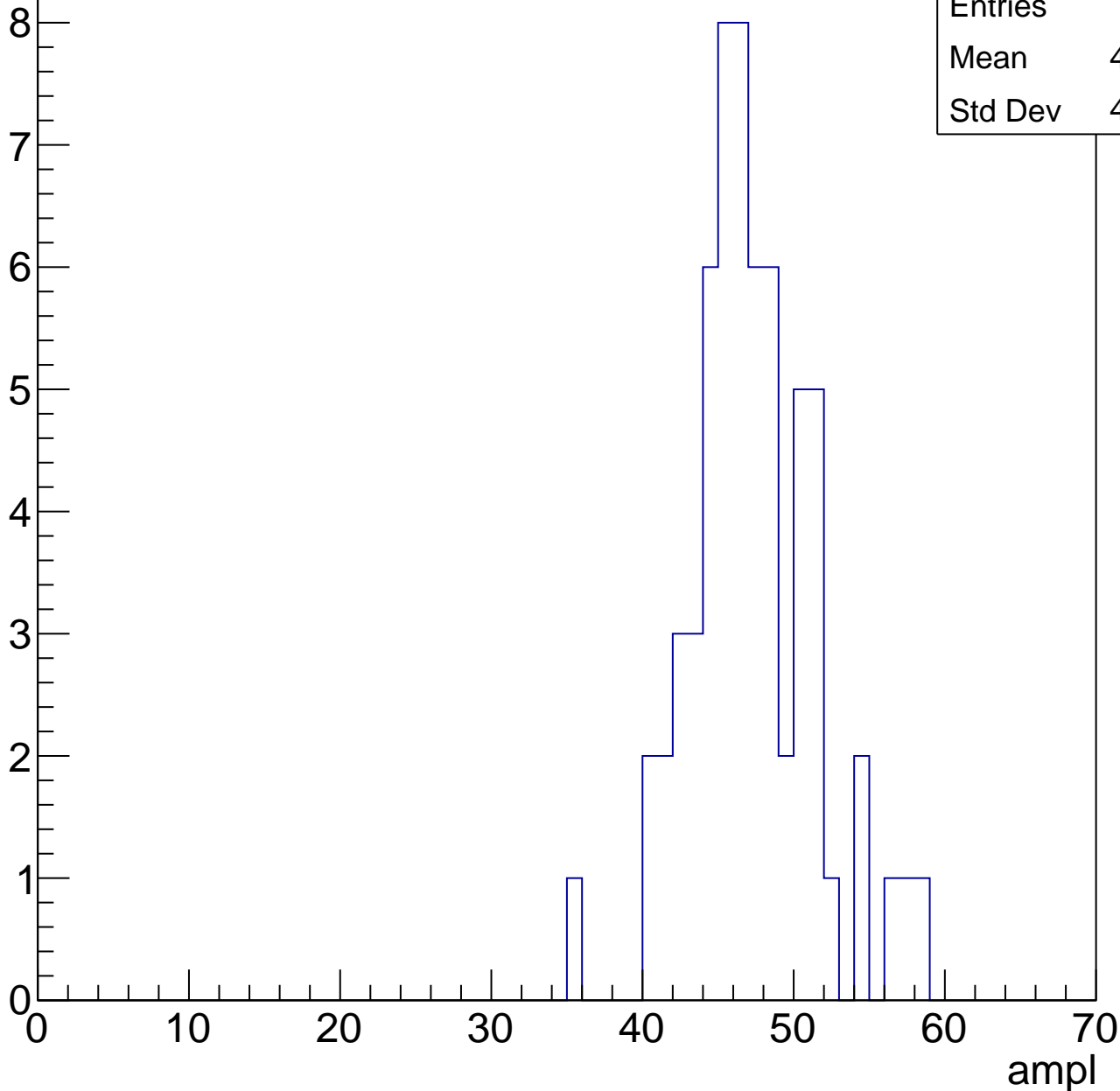


# B1L103S, U9-ch100, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	46.79
Std Dev	4.164

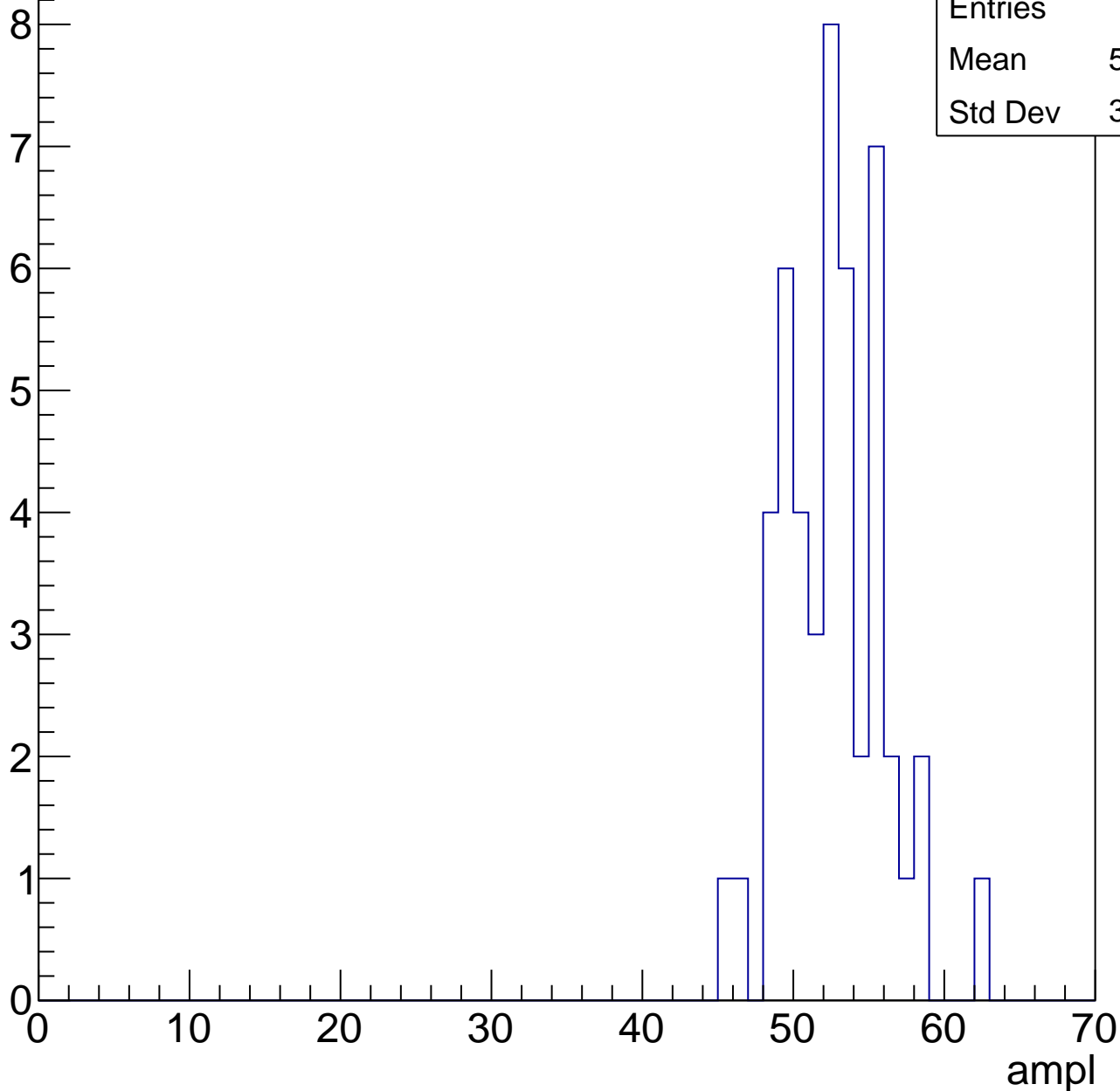


# B1L103S, U9-ch100, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	48
Mean	52.17
Std Dev	3.312

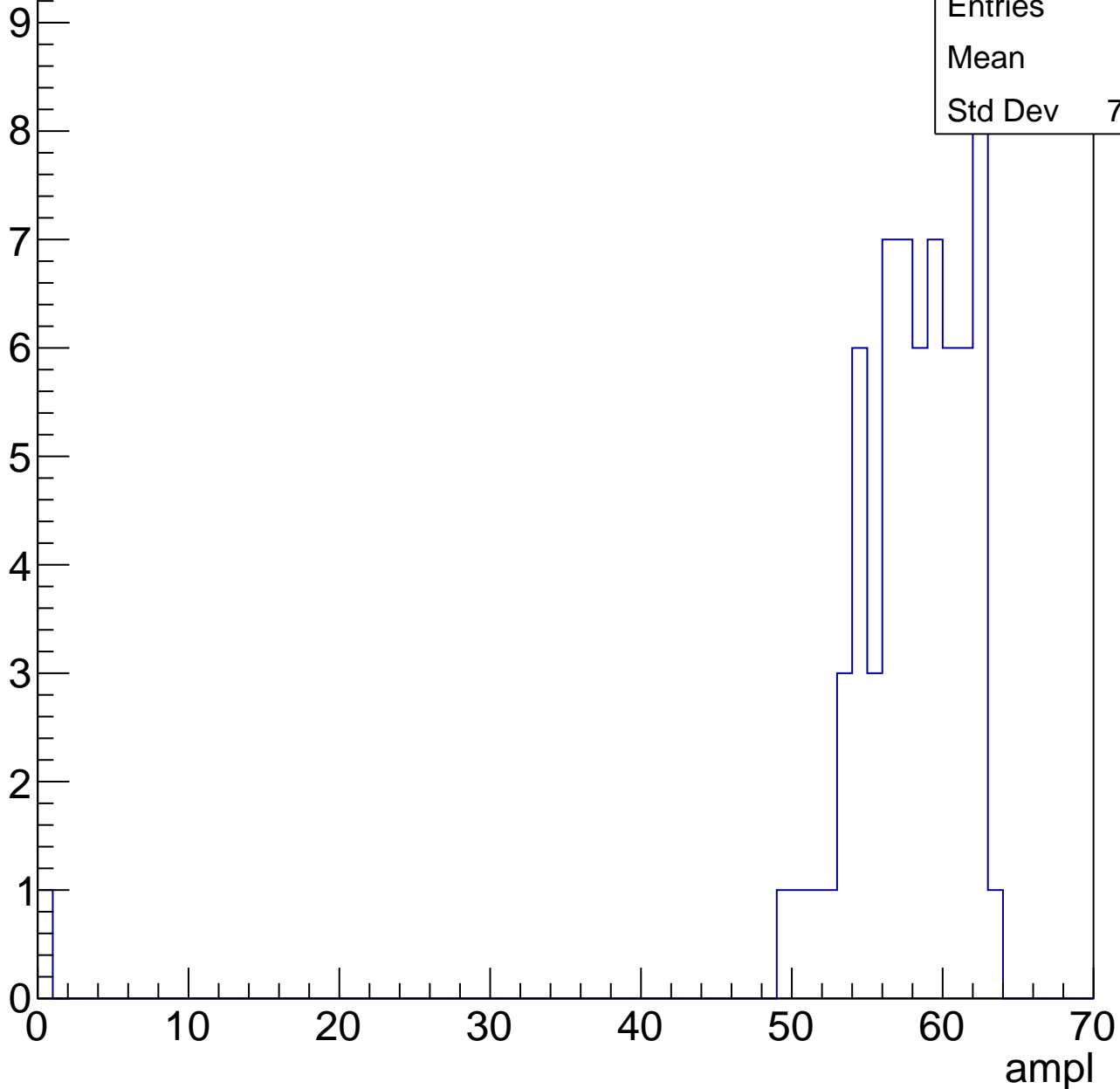


# B1L103S, U9-ch100, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	56.8
Std Dev	7.772

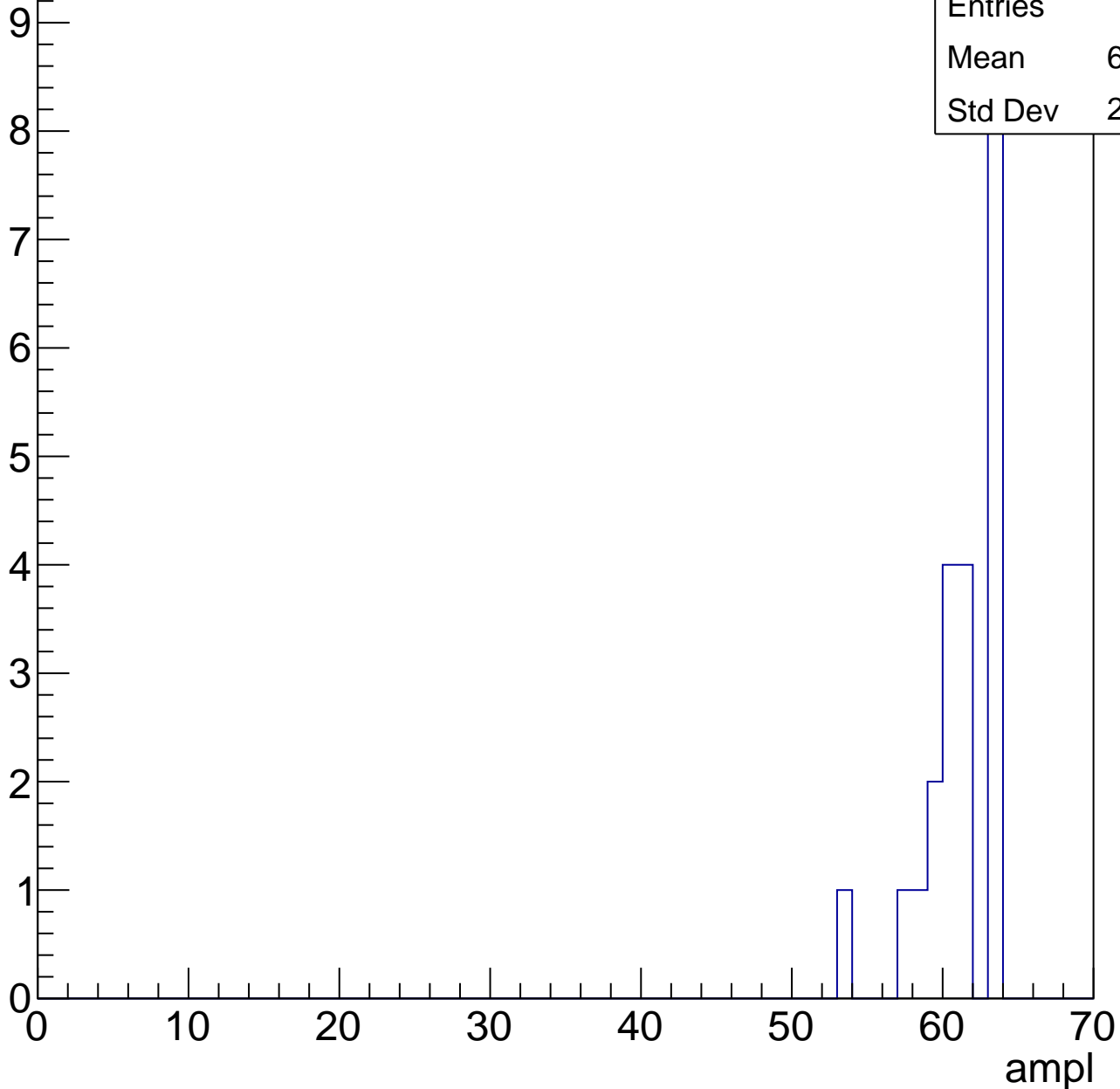


# B1L103S, U9-ch100, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	22
Mean	60.77
Std Dev	2.485

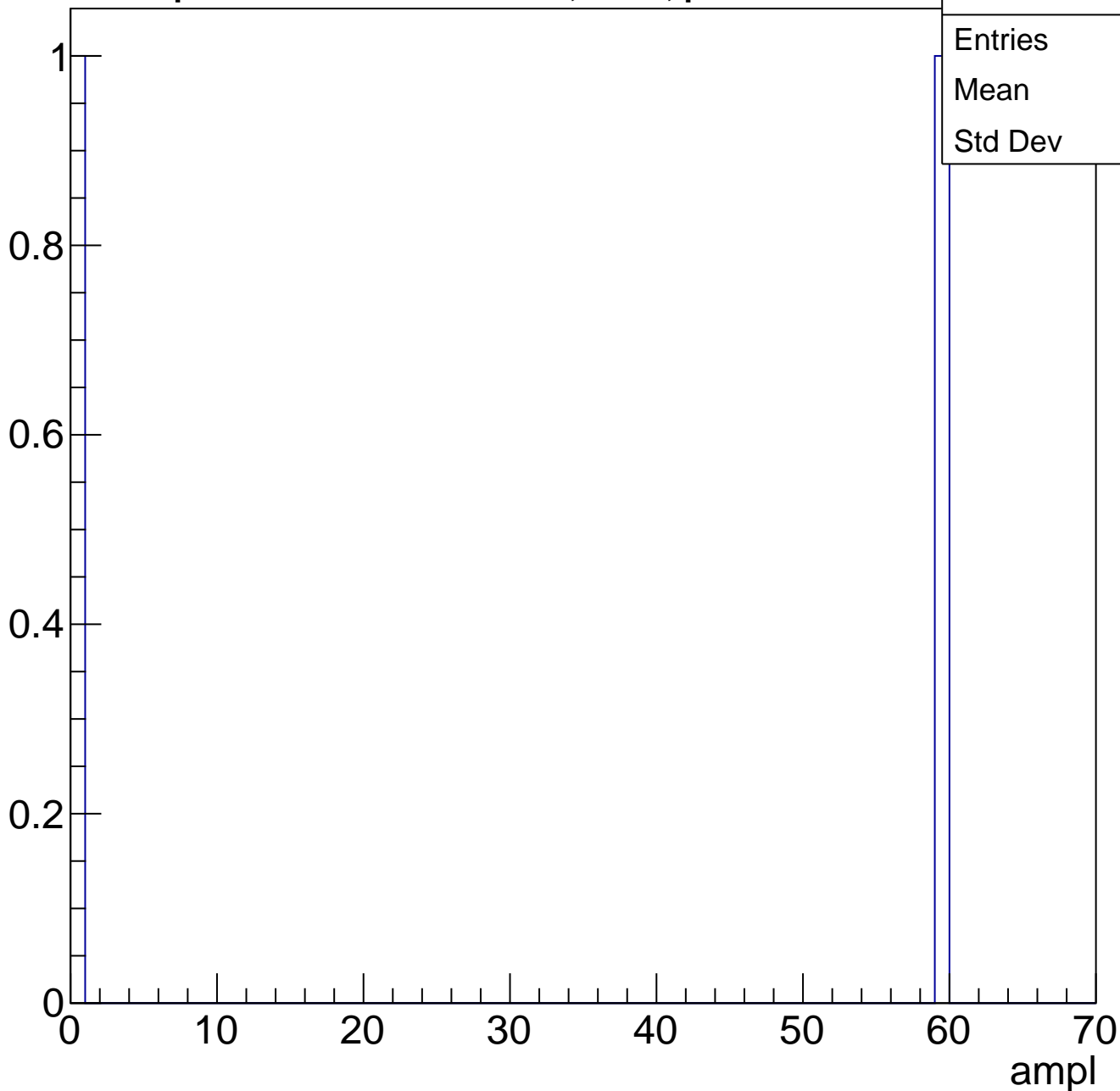




# B1L103S, U9-ch100, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U9-ch101, adc0

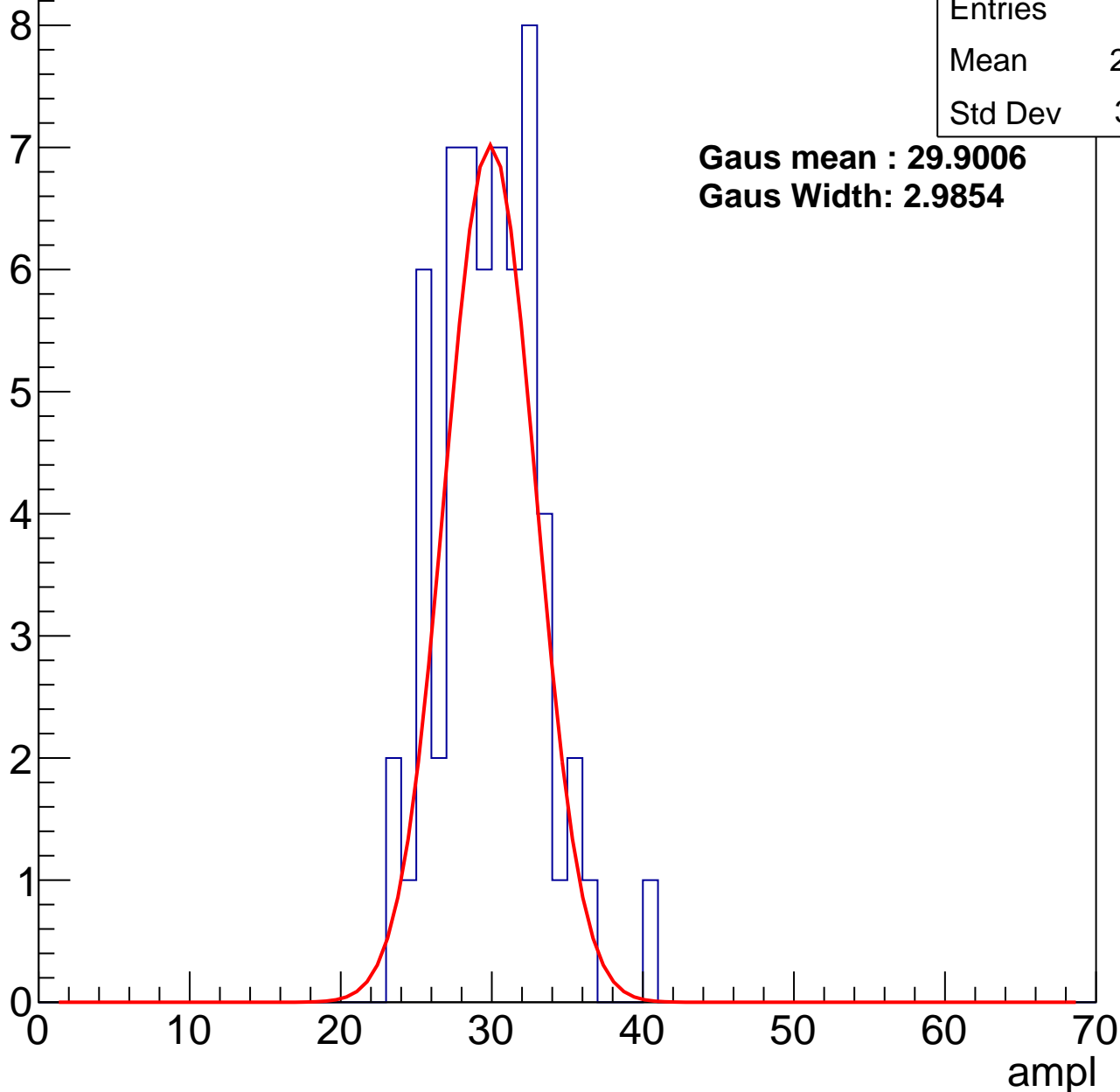
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	61
Mean	29.43
Std Dev	3.311

**Gaus mean : 29.9006**

**Gaus Width: 2.9854**



# B1L103S, U9-ch101, adc1

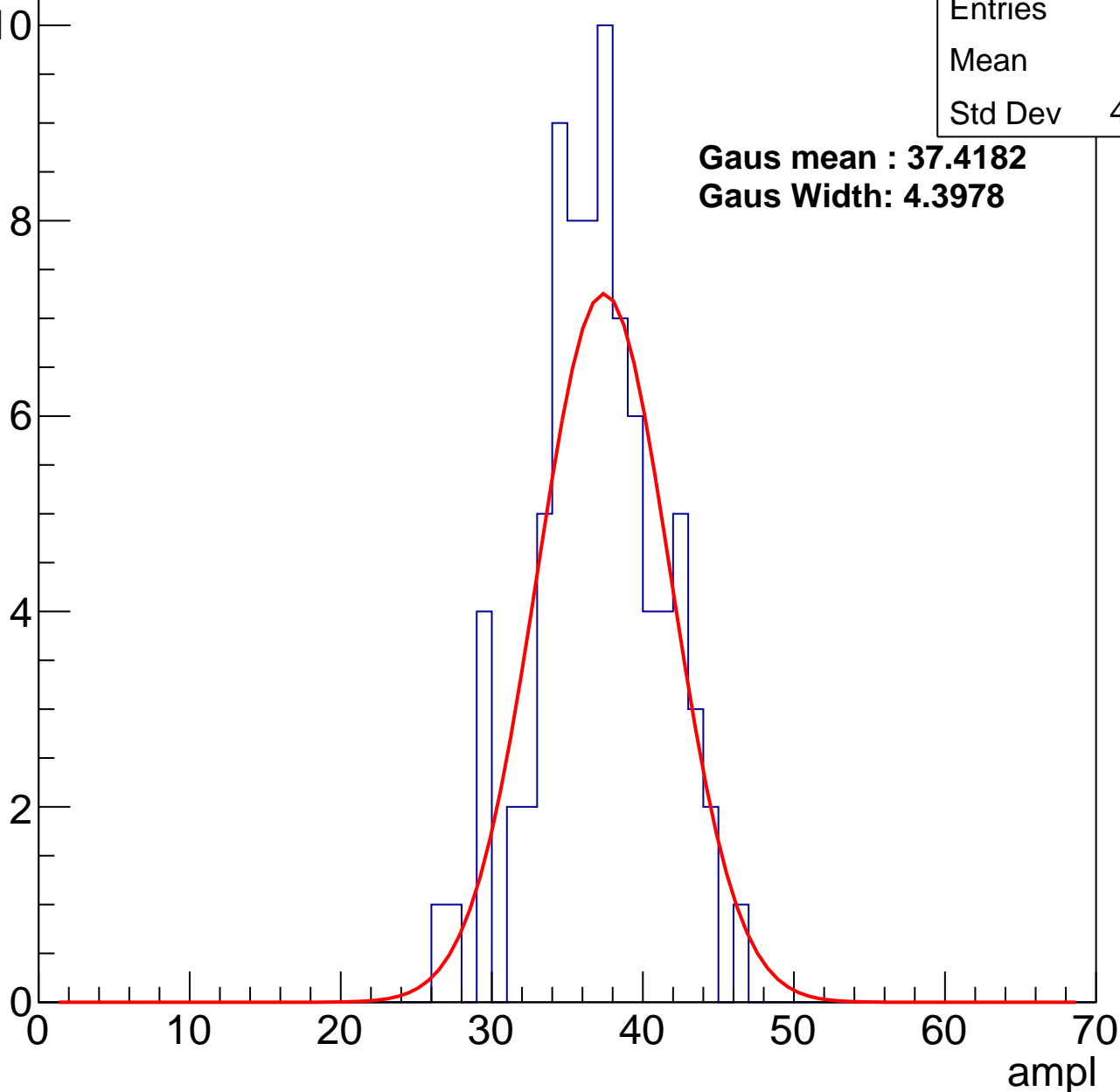
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	82
Mean	36.6
Std Dev	4.027

**Gaus mean : 37.4182**

**Gaus Width: 4.3978**



# B1L103S, U9-ch101, adc2

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	70
Mean	44.07
Std Dev	3.348

**Gaus mean : 44.2896**

**Gaus Width: 3.8918**

Entry

10  
8  
6  
4  
2  
0

ampl

0

10

20

30

40

50

60

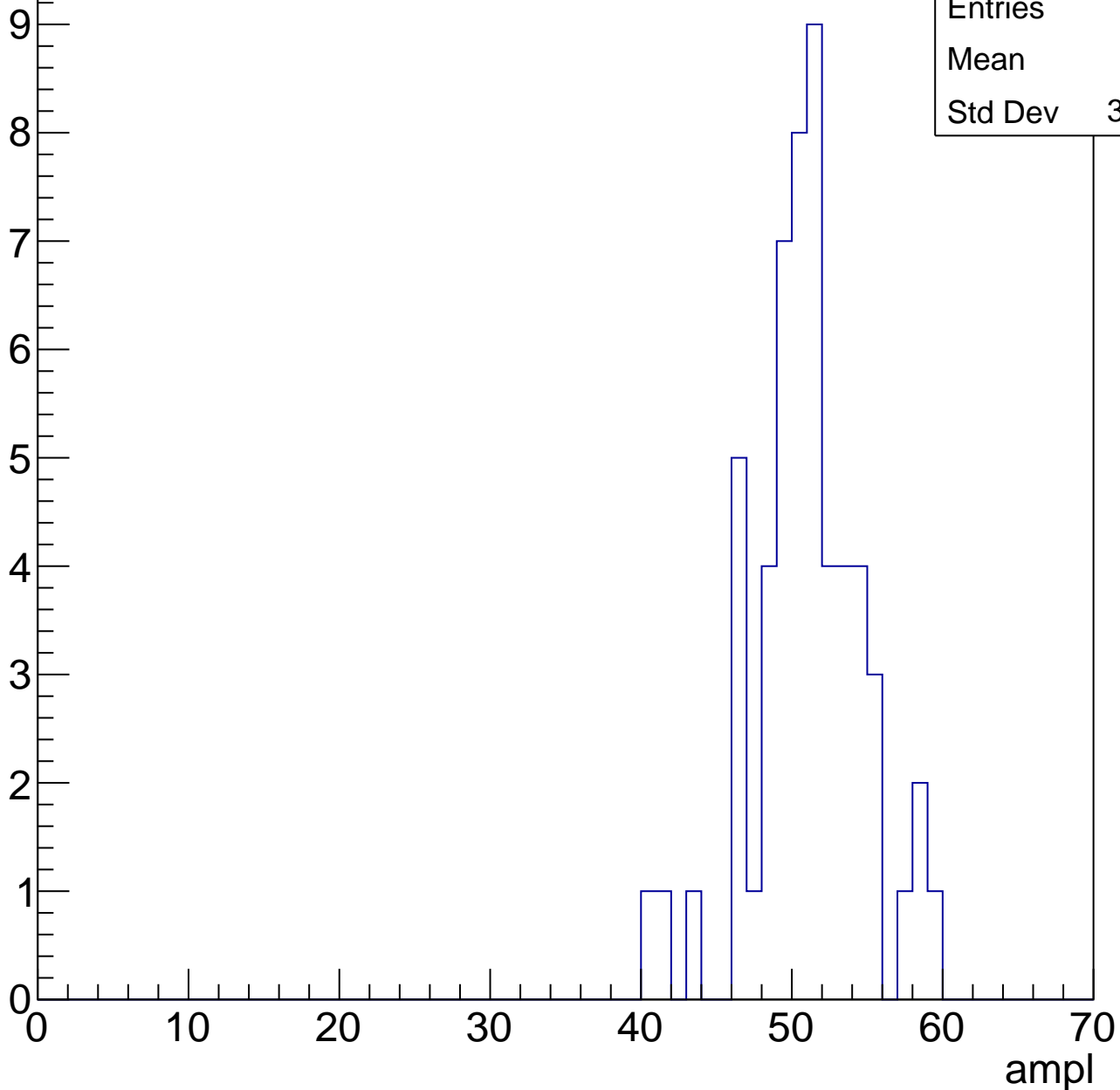
70

# B1L103S, U9-ch101, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

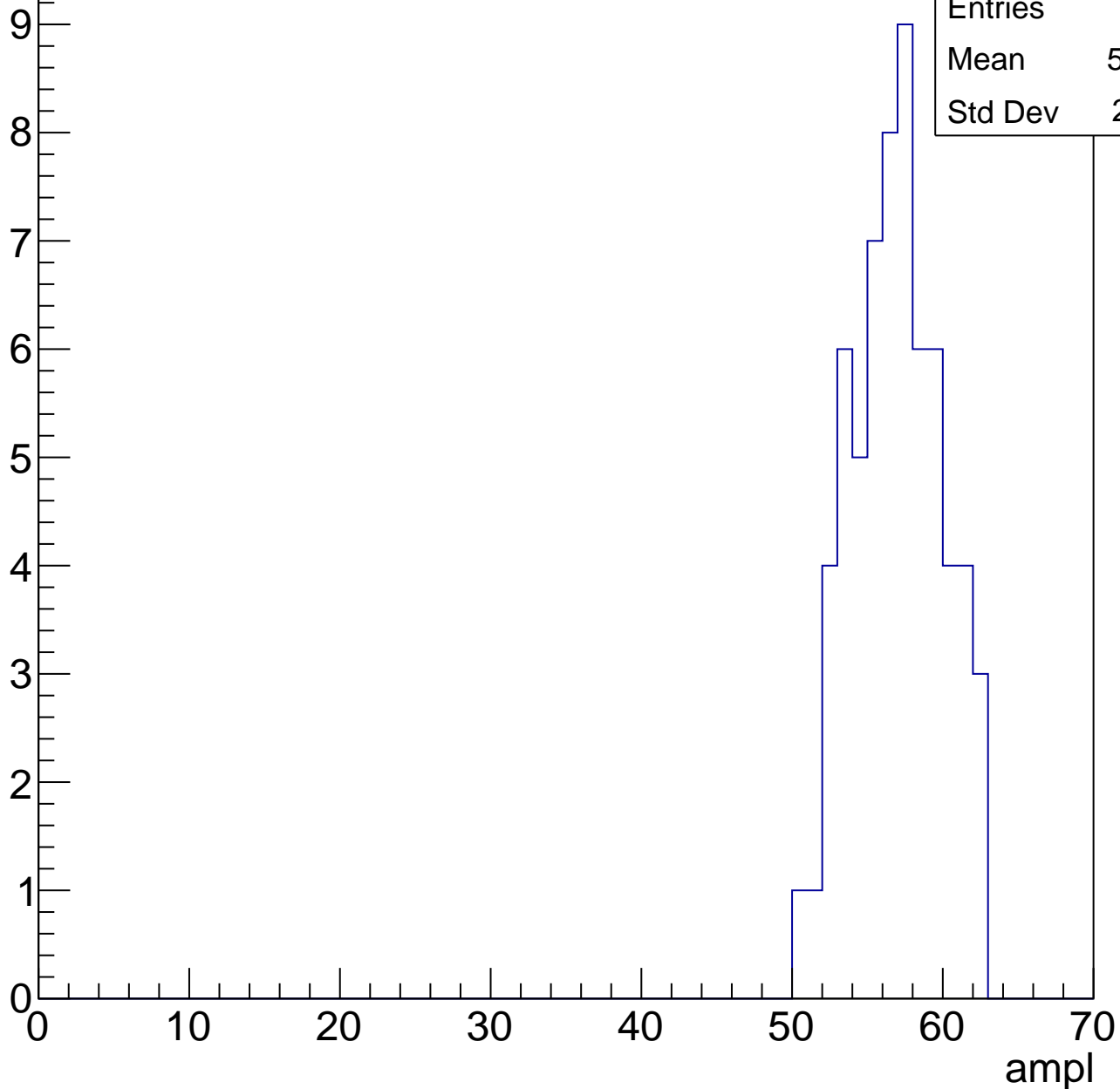
Entries	56
Mean	50.5
Std Dev	3.746



# B1L103S, U9-ch101, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

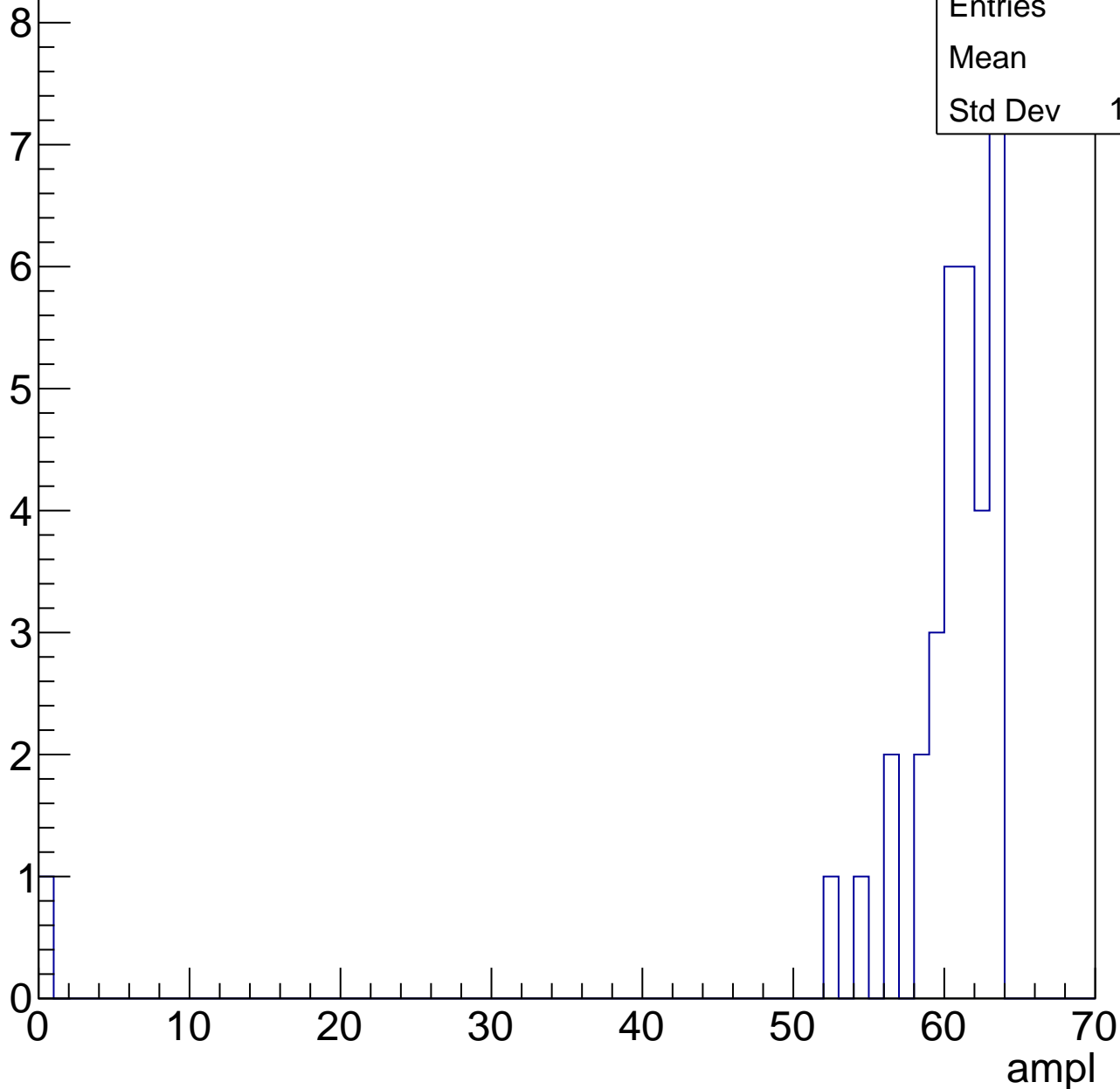


# B1L103S, U9-ch101, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	34
Mean	58.5
Std Dev	10.52



# B1L103S, U9-ch101, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U9-ch101, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U9-ch102, adc0

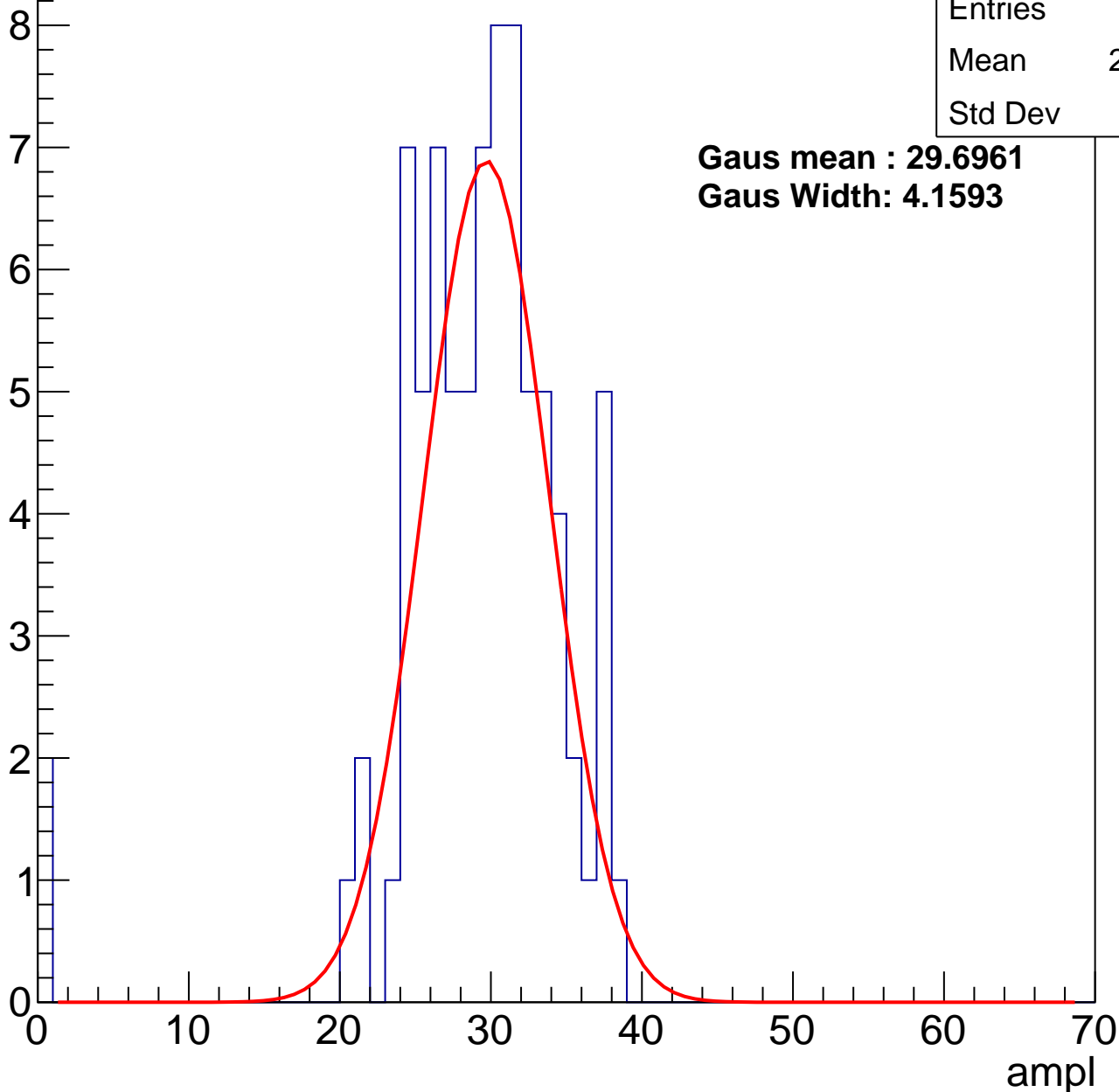
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	81
Mean	28.59
Std Dev	6.13

**Gaus mean : 29.6961**

**Gaus Width: 4.1593**



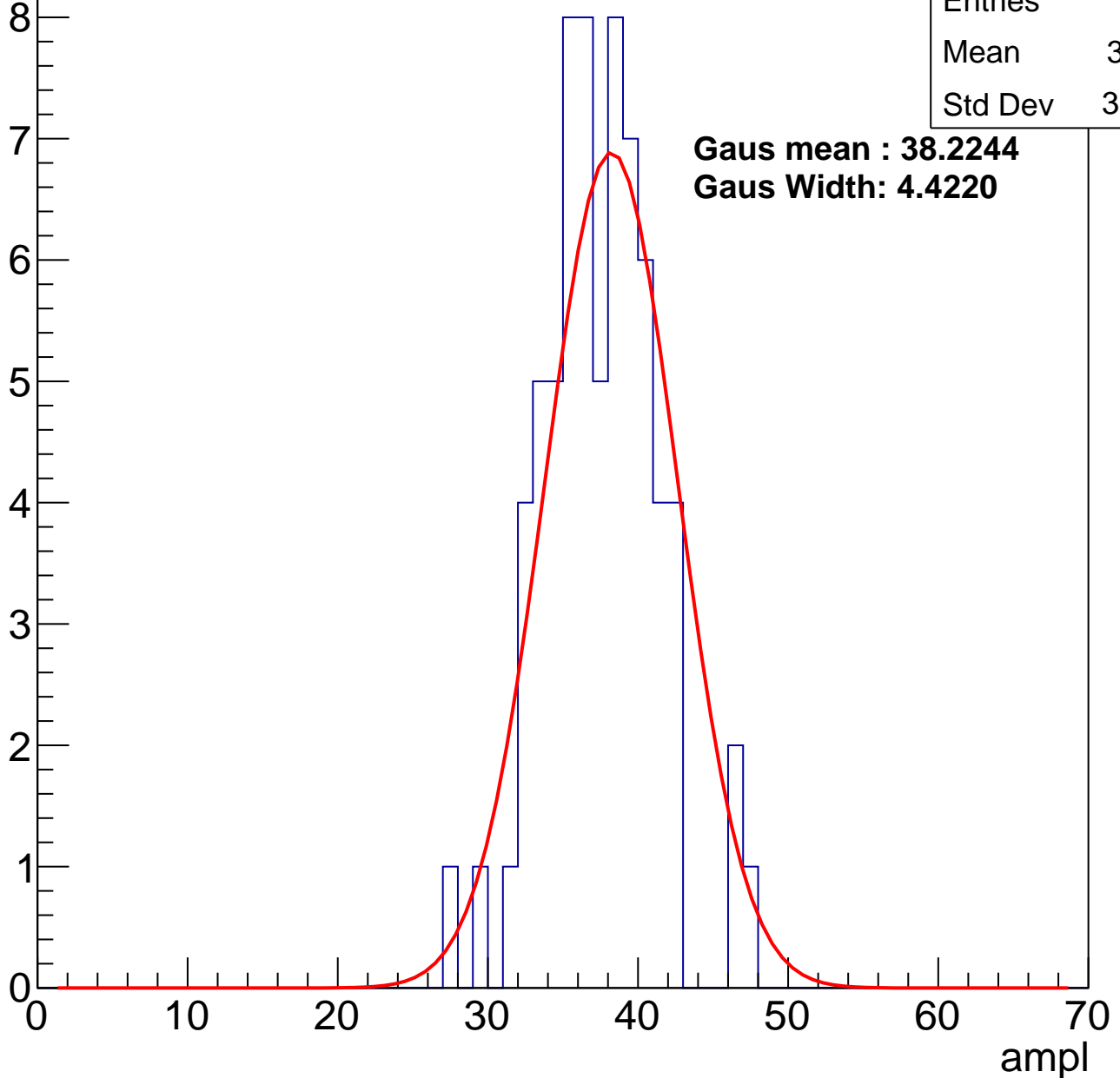
# B1L103S, U9-ch102, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	70
Mean	37.01
Std Dev	3.744

**Gaus mean : 38.2244**  
**Gaus Width: 4.4220**



# B1L103S, U9-ch102, adc2

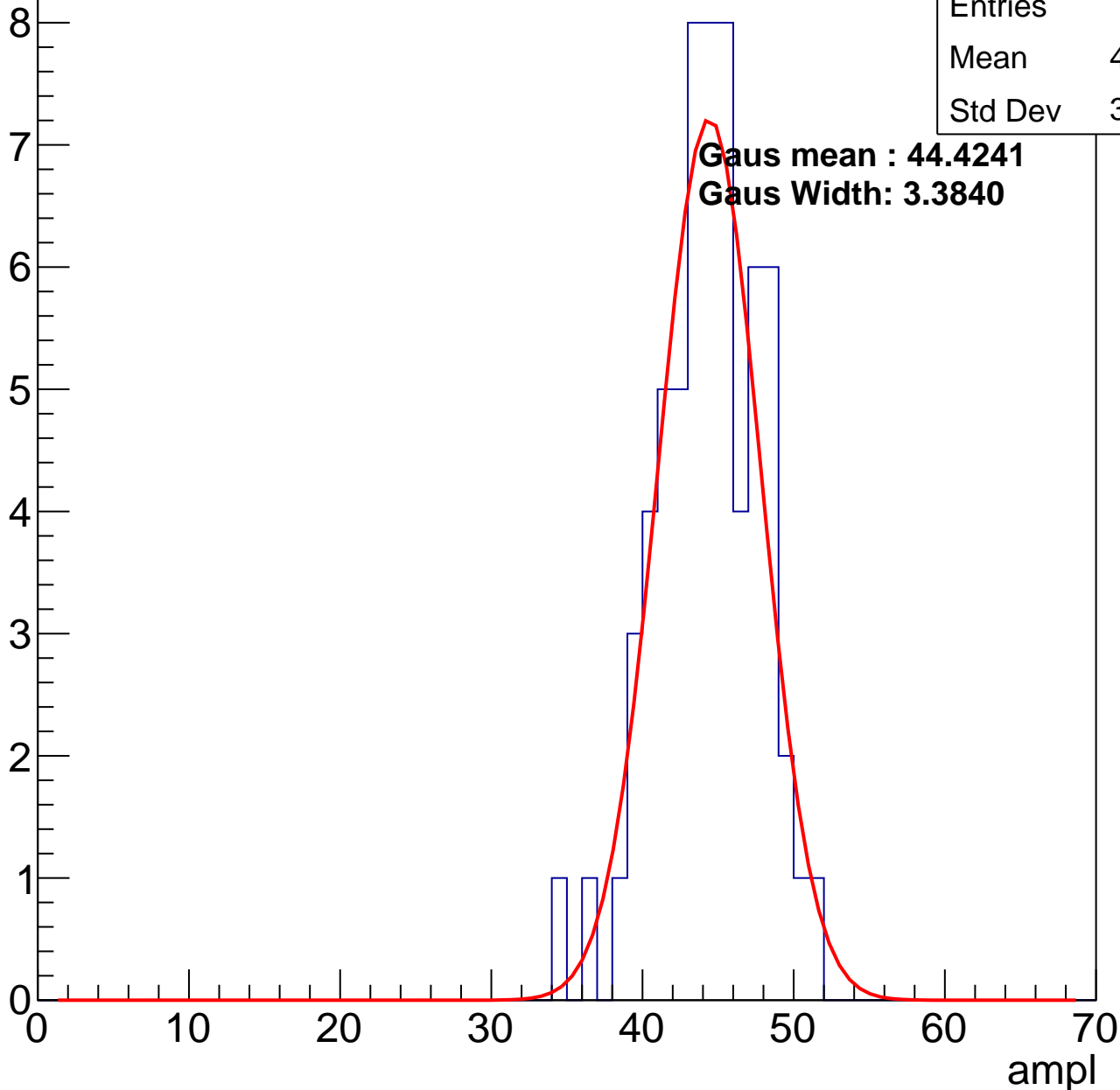
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	43.89
Std Dev	3.355

**Gaus mean : 44.4241**

**Gaus Width: 3.3840**

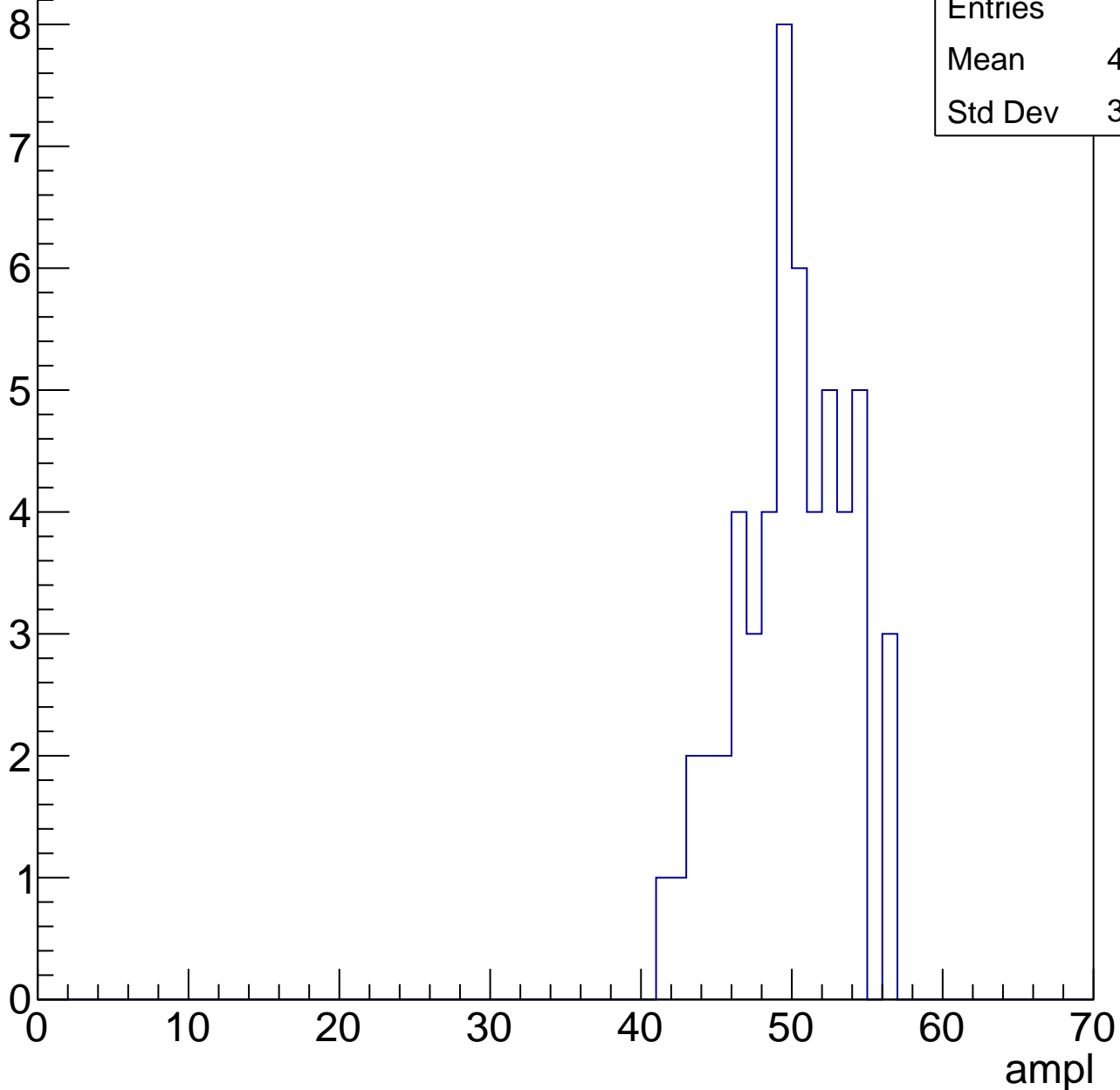


# B1L103S, U9-ch102, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	54
Mean	49.44
Std Dev	3.629

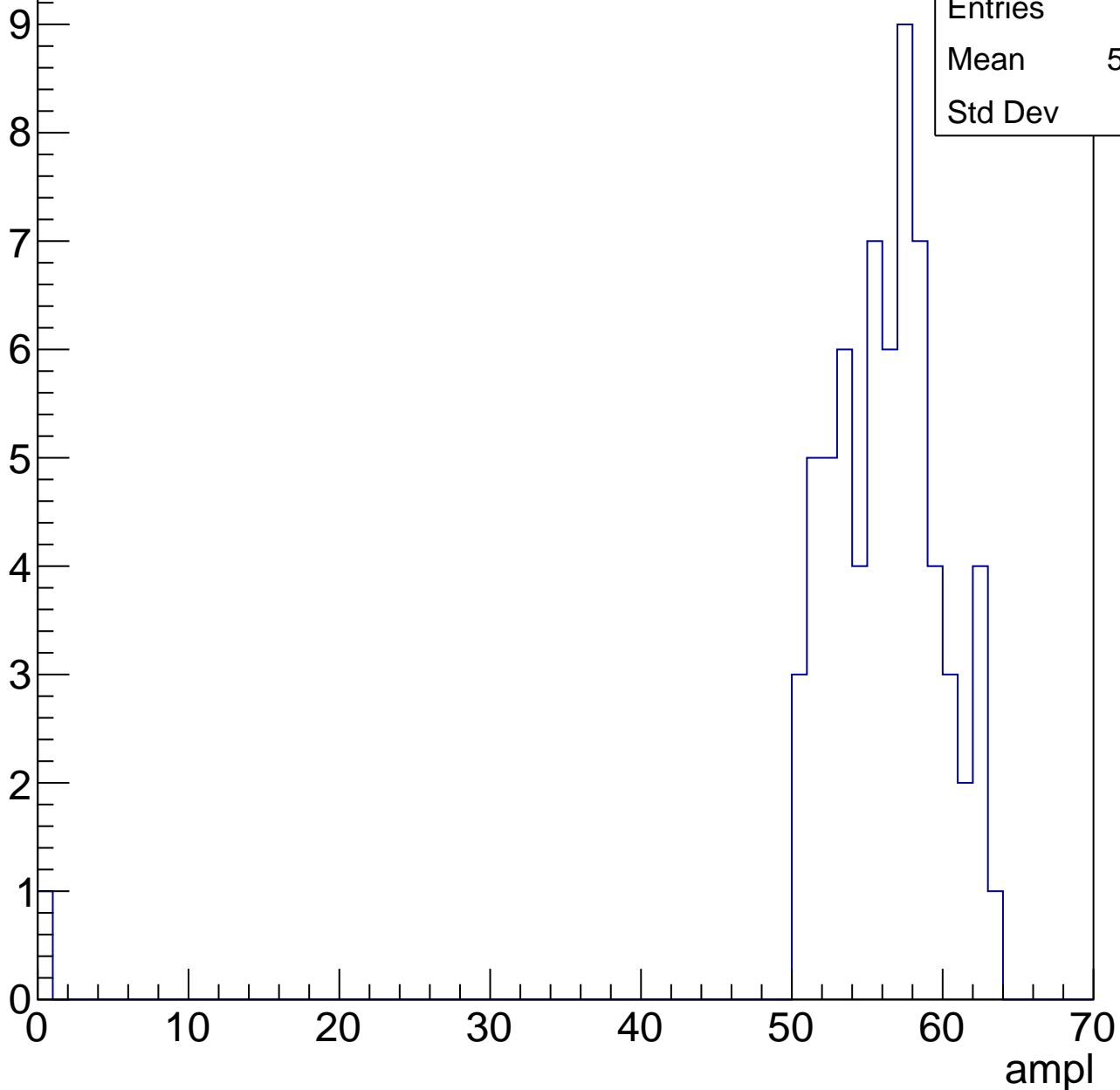


# B1L103S, U9-ch102, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	55.04
Std Dev	7.56



# B1L103S, U9-ch102, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

7

6

5

4

3

2

1

0

Entries	38
Mean	59.84
Std Dev	2.412

ampl

0

10

20

30

40

50

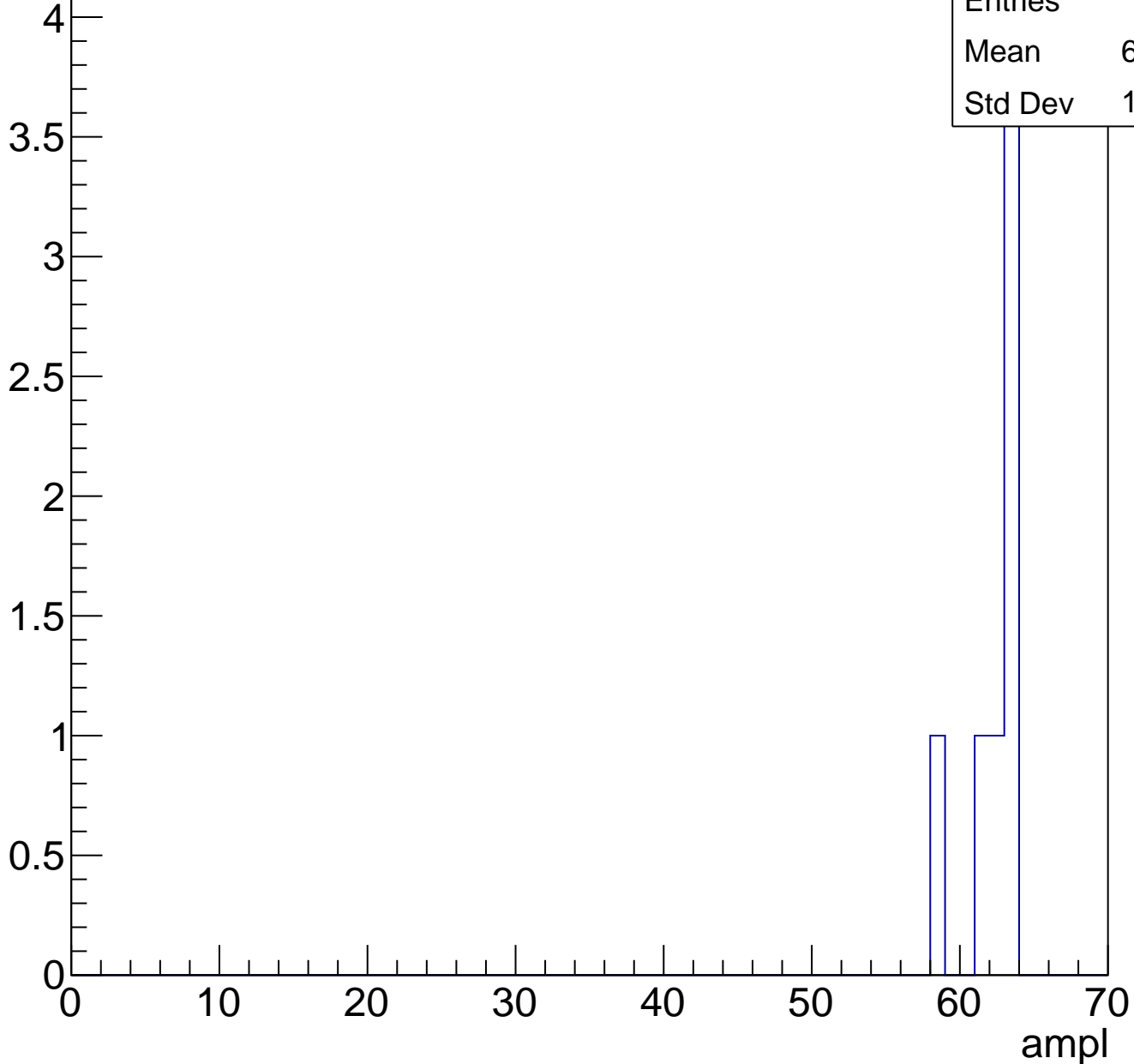
60

70

# B1L103S, U9-ch102, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U9-ch102, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U9-ch103, adc0

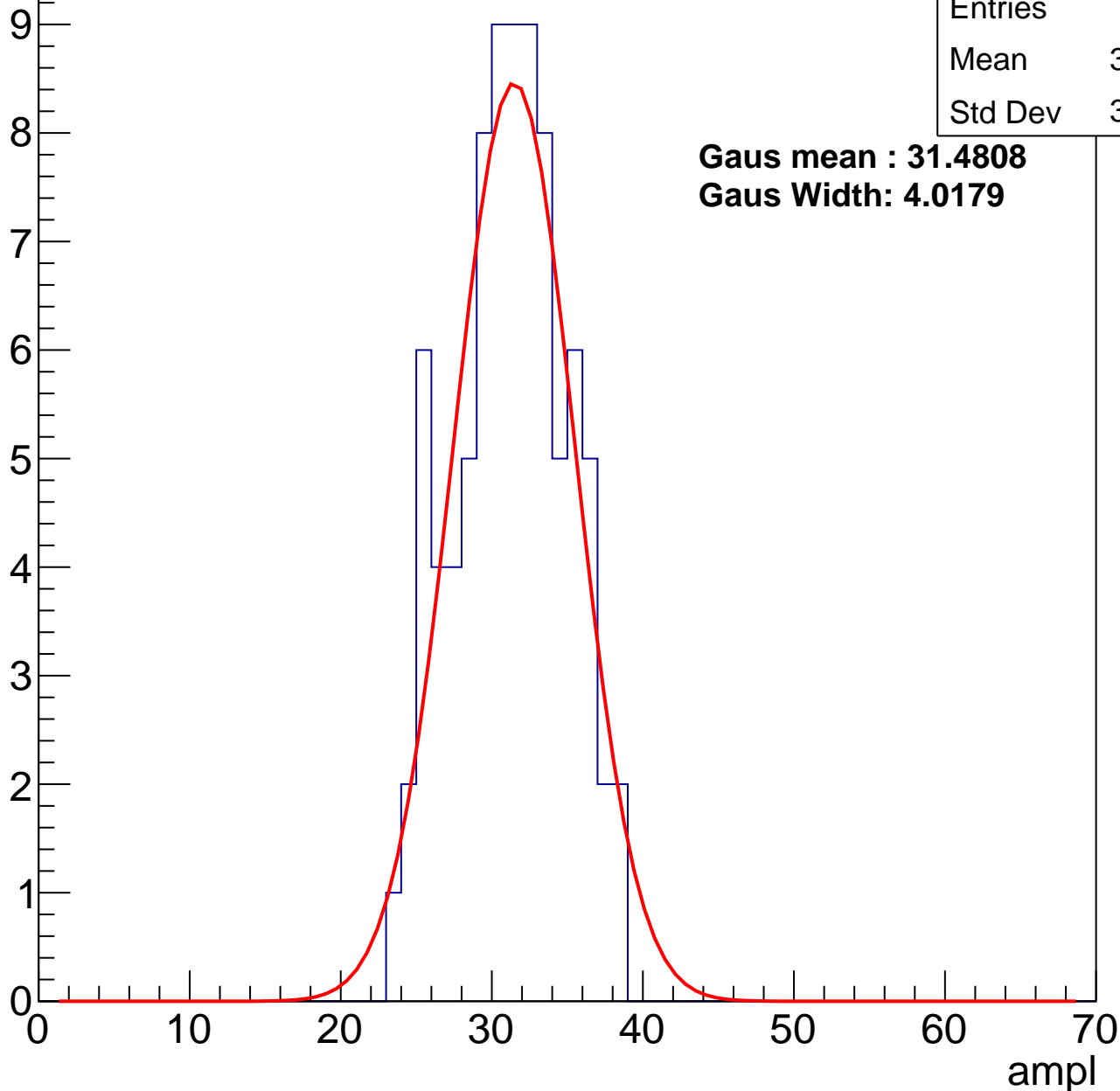
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	85
Mean	30.78
Std Dev	3.599

**Gaus mean : 31.4808**

**Gaus Width: 4.0179**



# B1L103S, U9-ch103, adc1

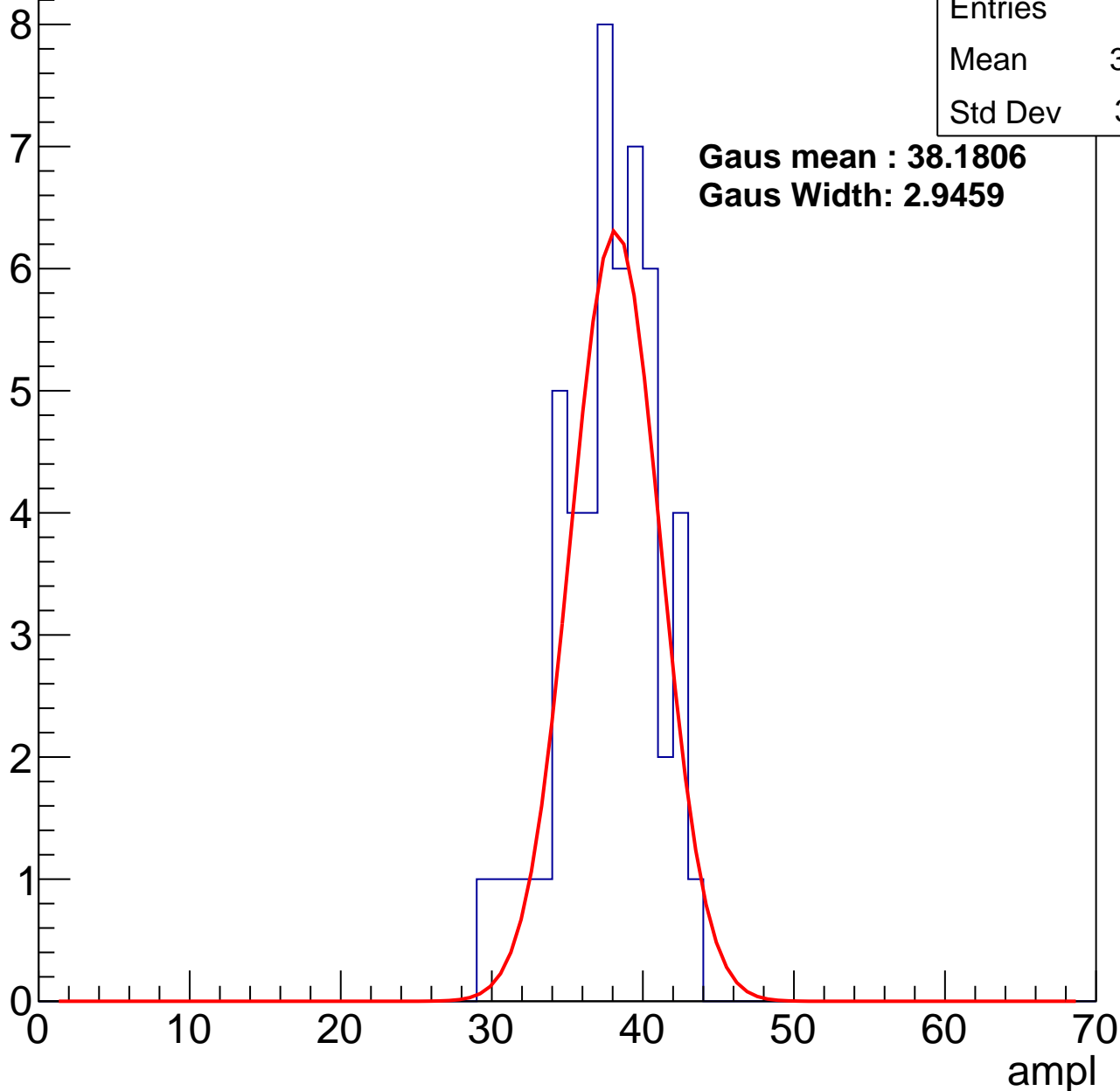
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	52
Mean	37.29
Std Dev	3.121

**Gaus mean : 38.1806**

**Gaus Width: 2.9459**



# B1L103S, U9-ch103, adc2

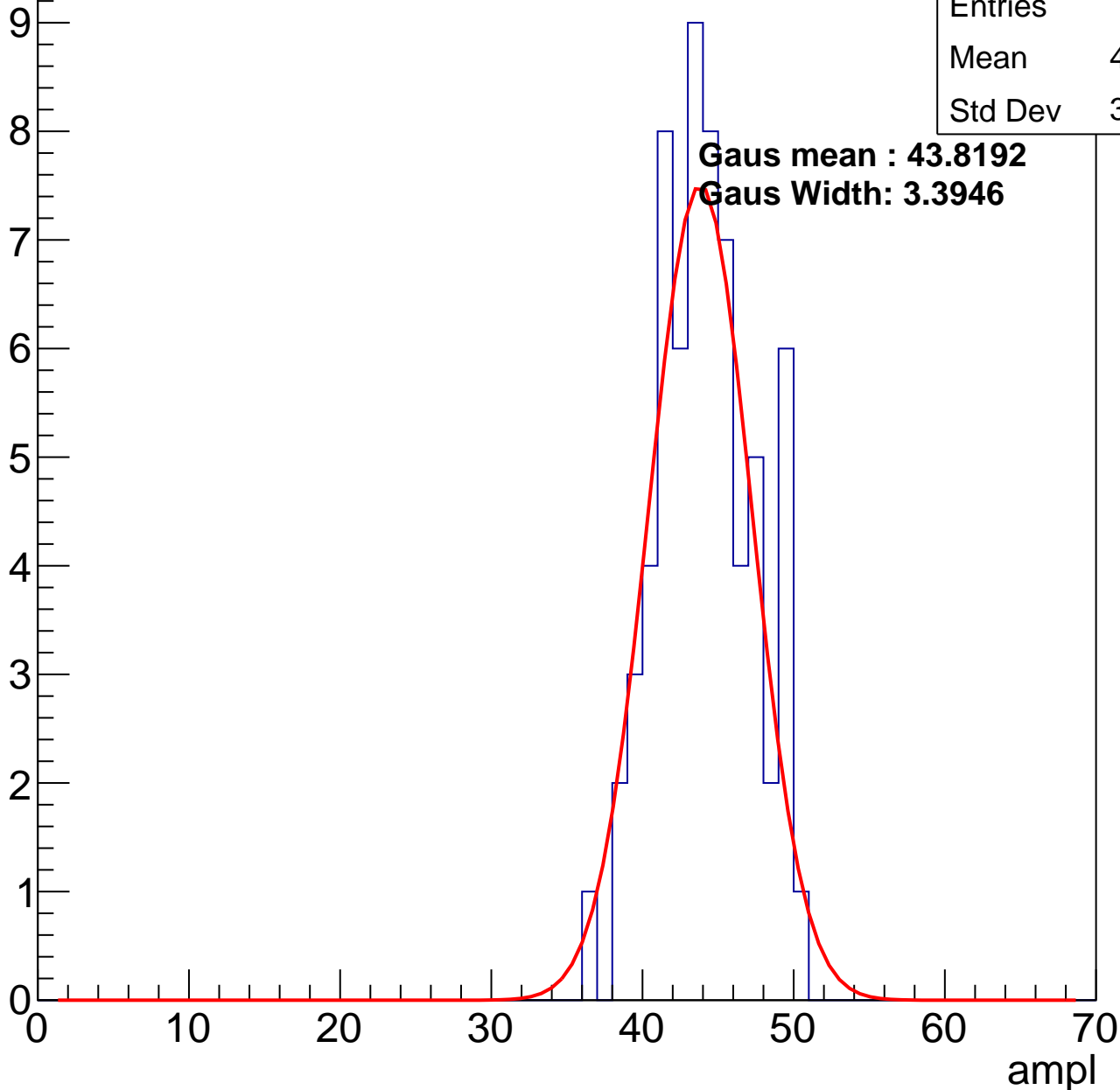
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	43.67
Std Dev	3.159

**Gaus mean : 43.8192**

**Gaus Width: 3.3946**

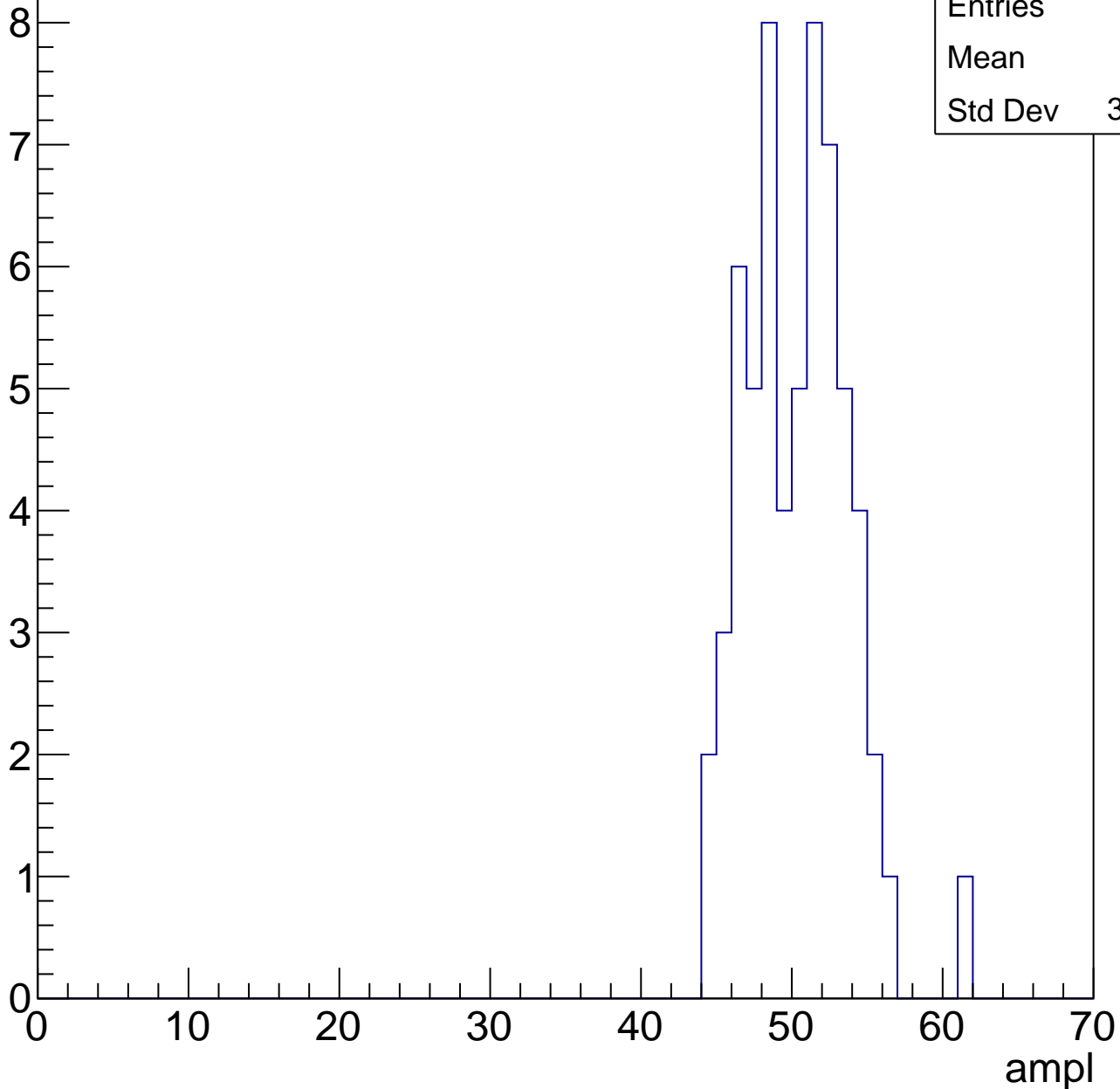


# B1L103S, U9-ch103, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	61
Mean	49.9
Std Dev	3.328

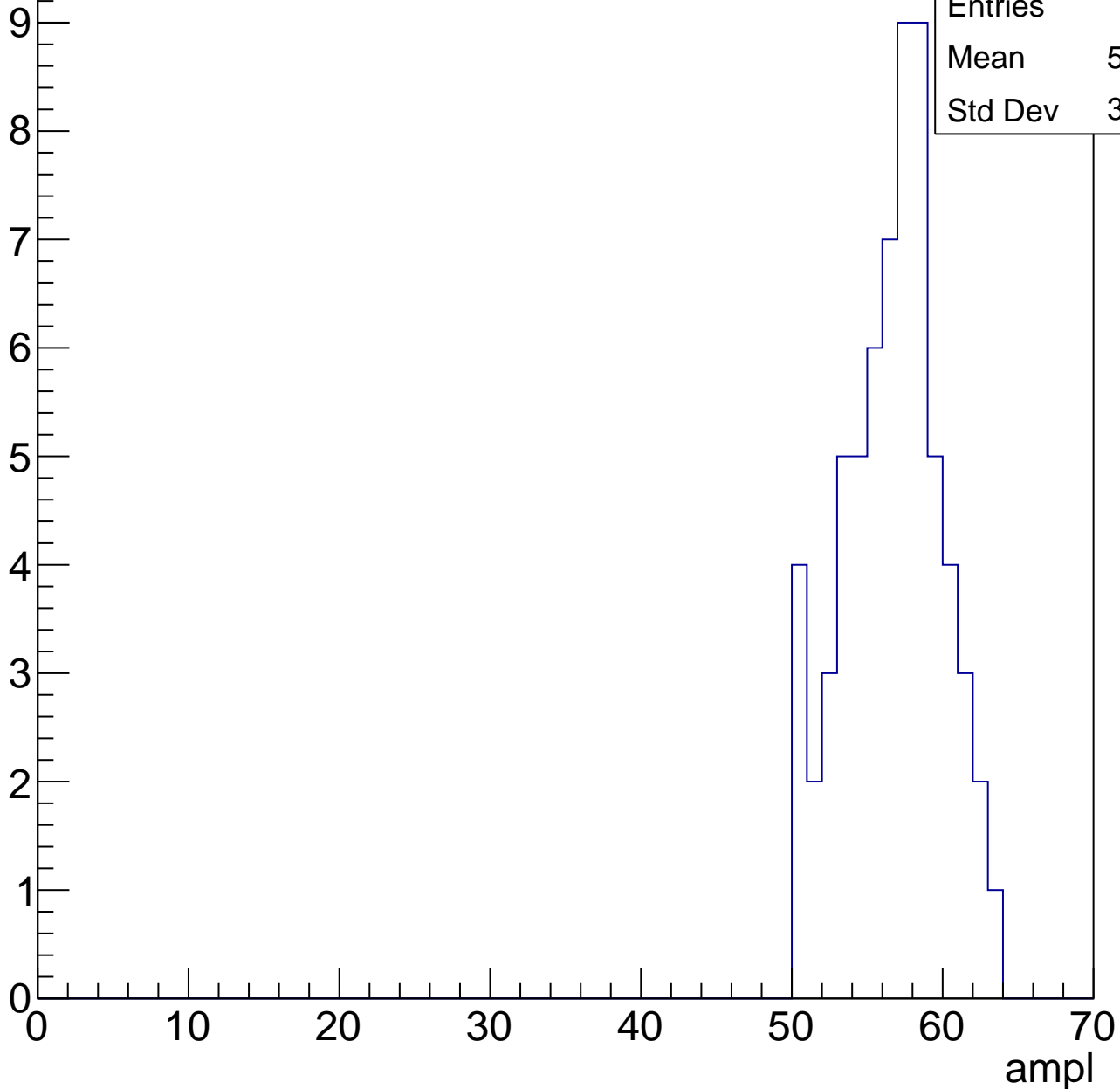


# B1L103S, U9-ch103, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	56.23
Std Dev	3.185

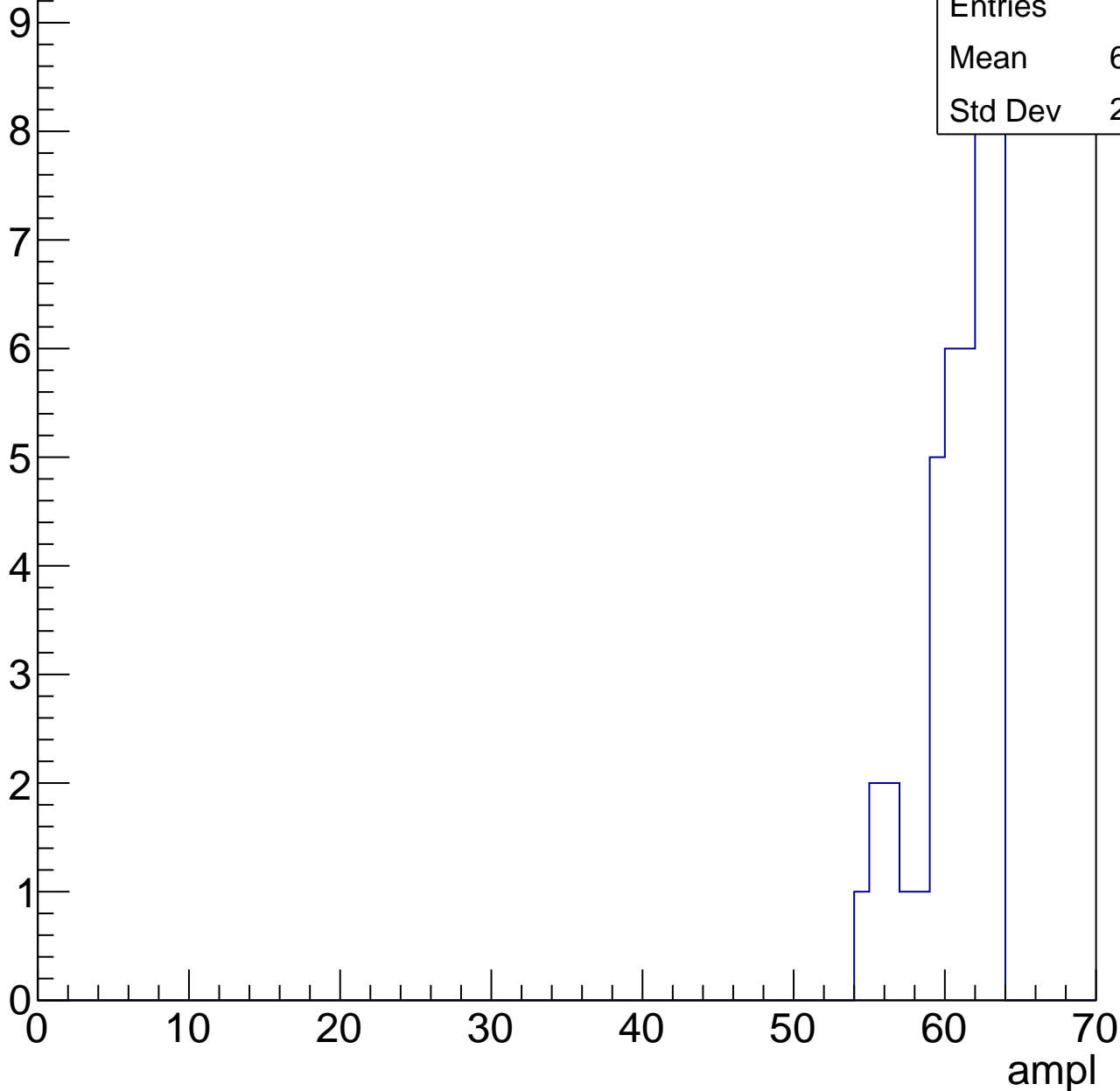


# B1L103S, U9-ch103, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	41
Mean	60.37
Std Dev	2.467



# B1L103S, U9-ch103, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U9-ch103, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	3
Mean	0
Std Dev	0

# B1L103S, U9-ch104, adc0

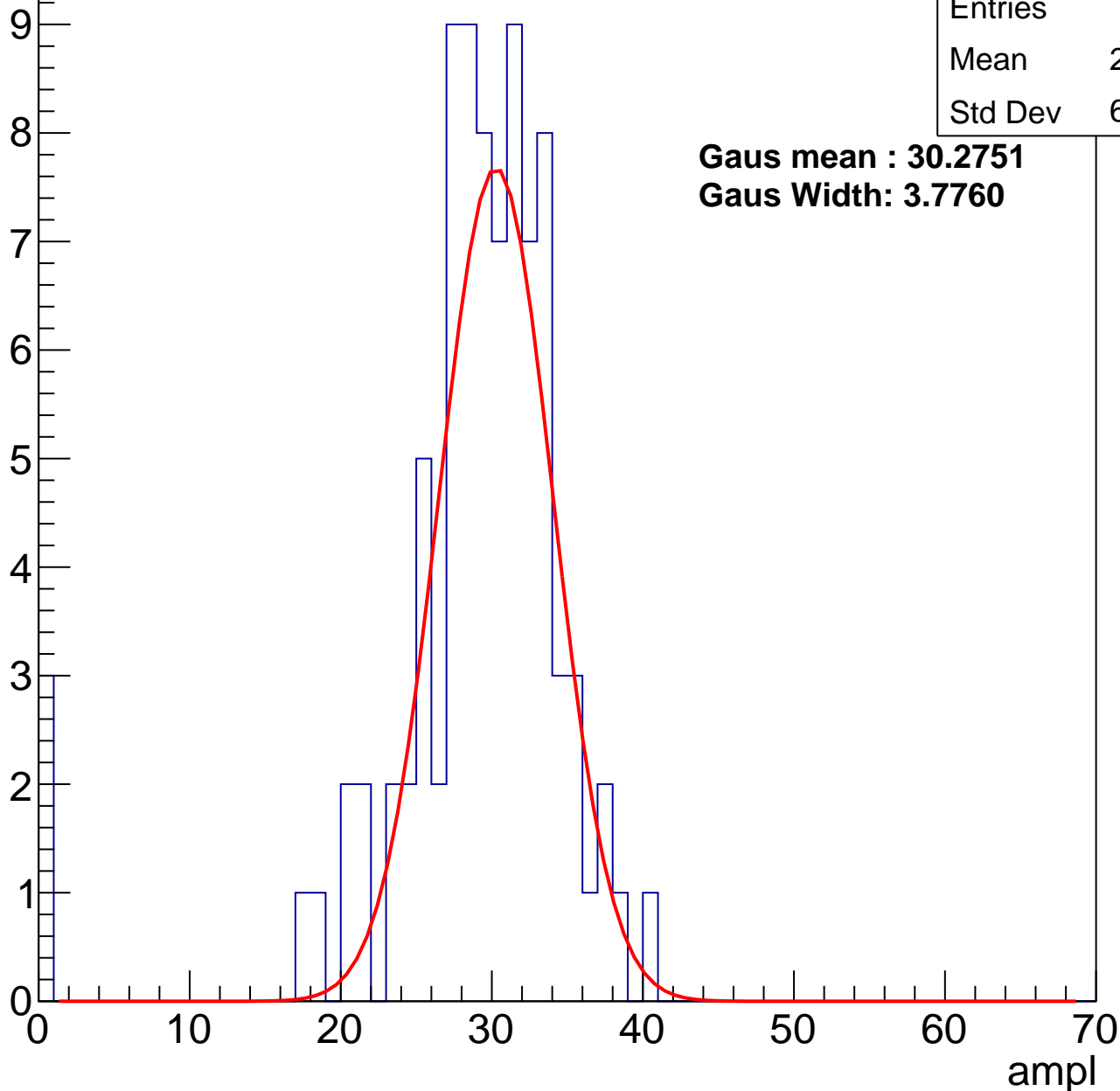
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	88
Mean	28.26
Std Dev	6.818

**Gaus mean : 30.2751**

**Gaus Width: 3.7760**



# B1L103S, U9-ch104, adc1

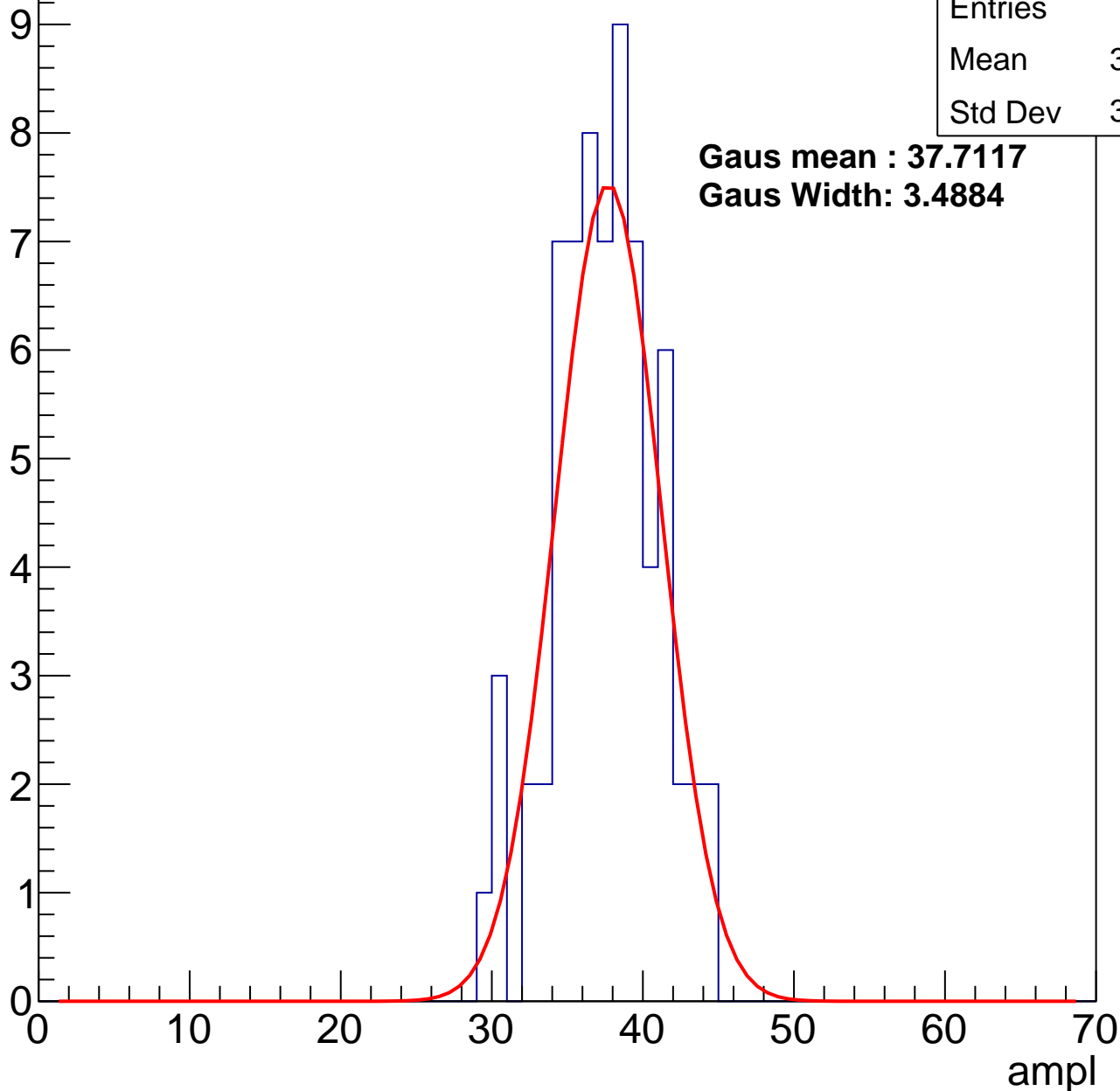
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	69
Mean	37.07
Std Dev	3.364

**Gaus mean : 37.7117**

**Gaus Width: 3.4884**



# B1L103S, U9-ch104, adc2

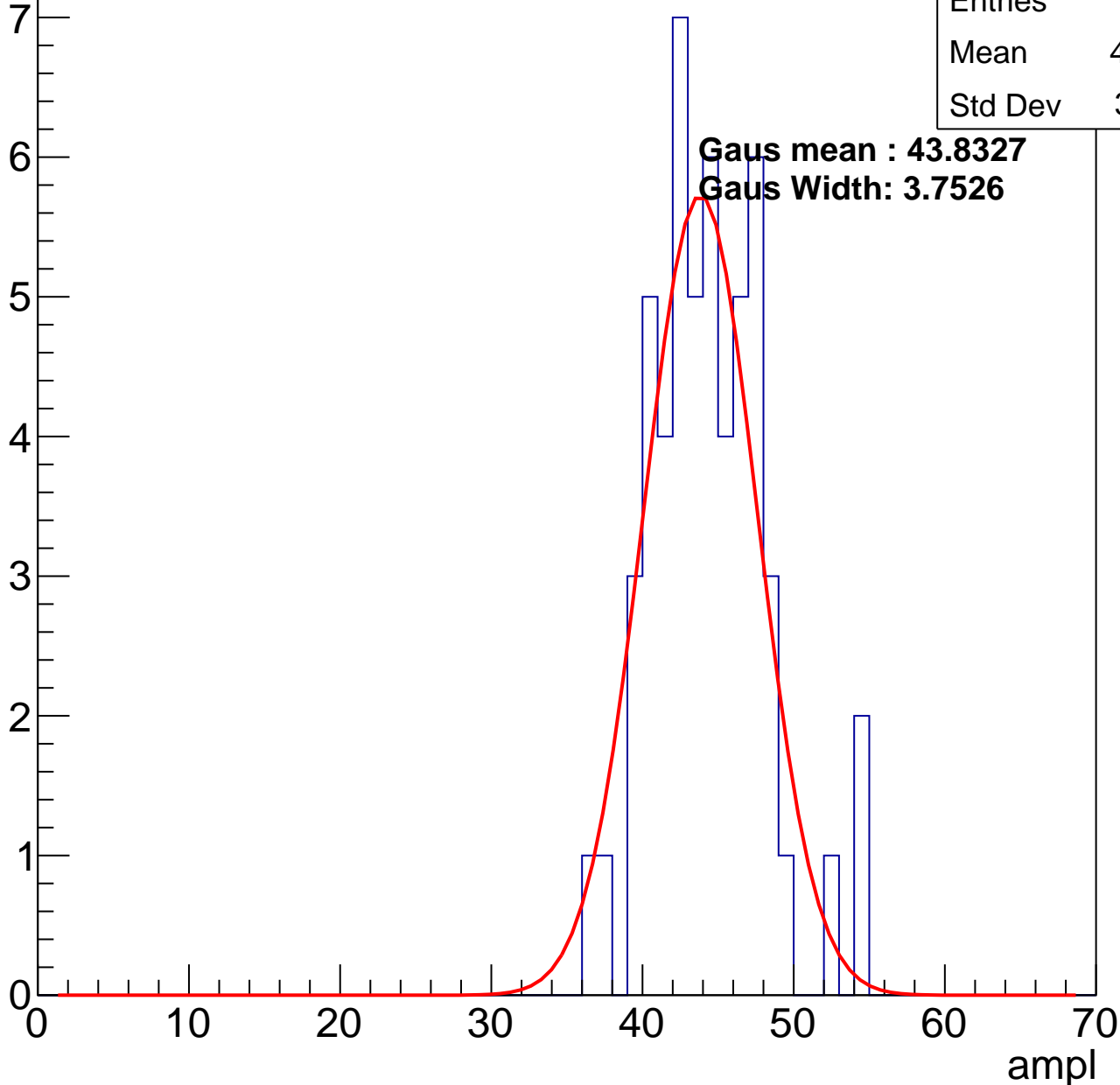
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	54
Mean	43.93
Std Dev	3.731

**Gaus mean : 43.8327**

**Gaus Width: 3.7526**

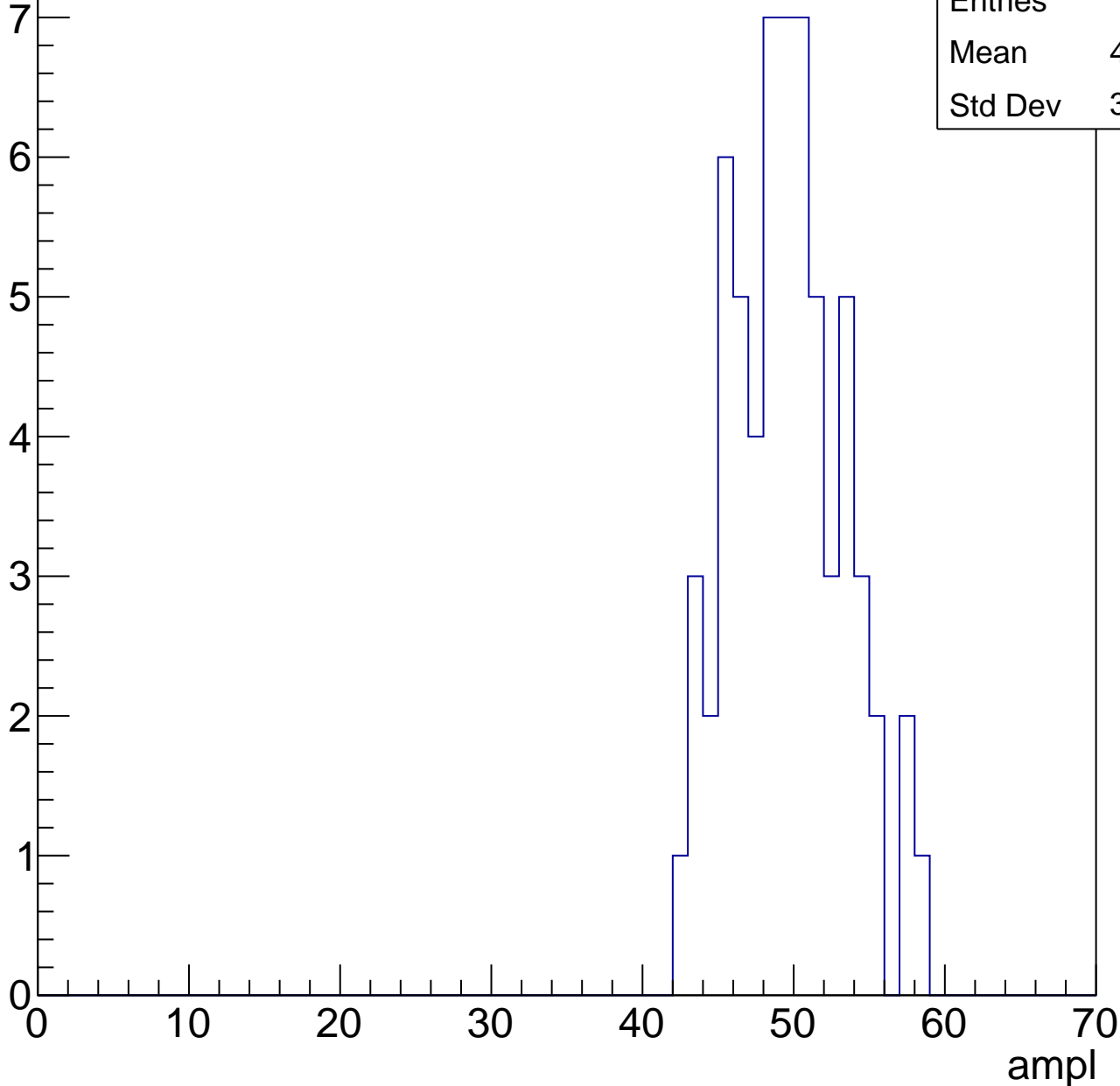


# B1L103S, U9-ch104, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	49.14
Std Dev	3.694

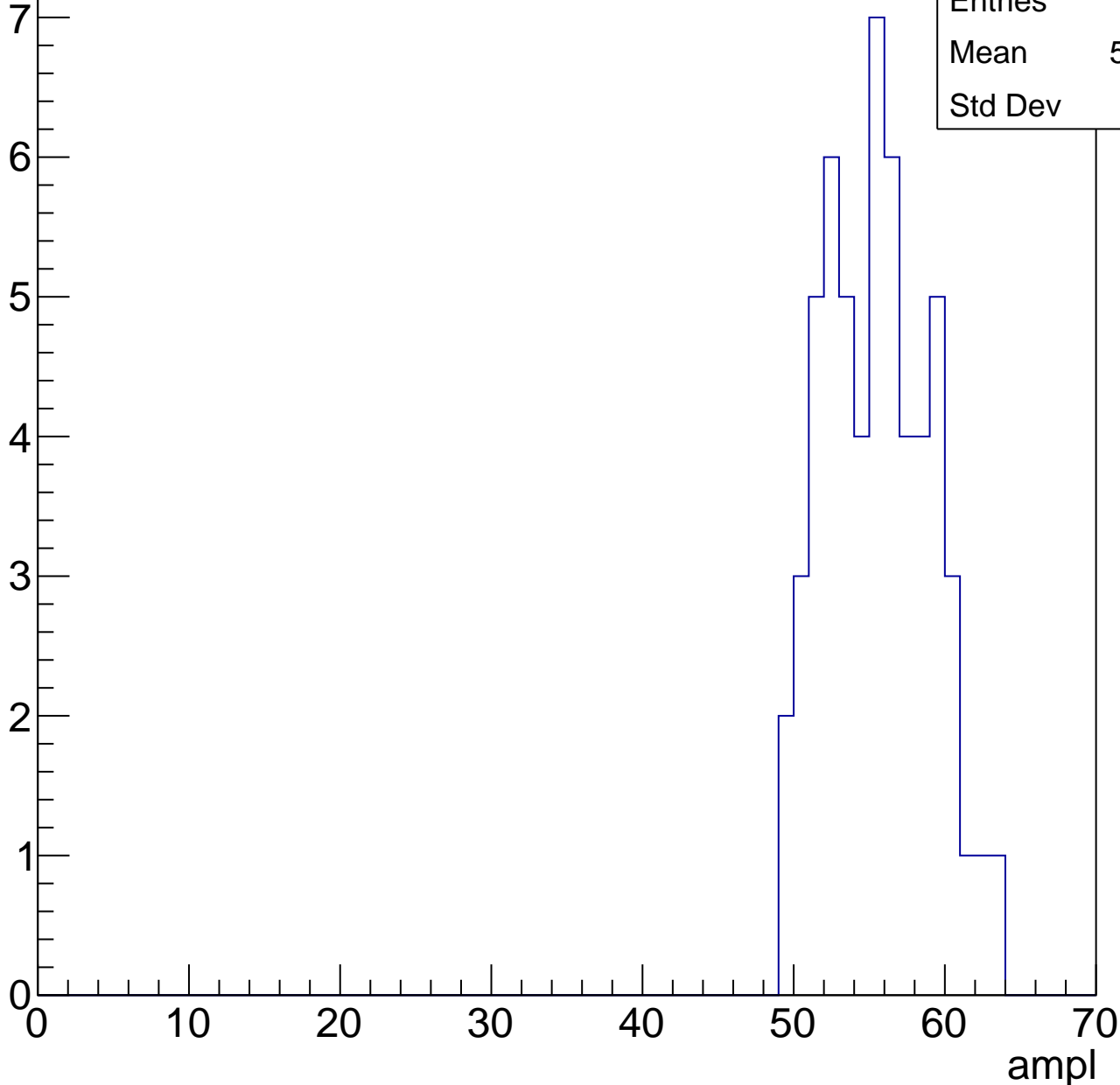


# B1L103S, U9-ch104, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	57
Mean	55.05
Std Dev	3.42

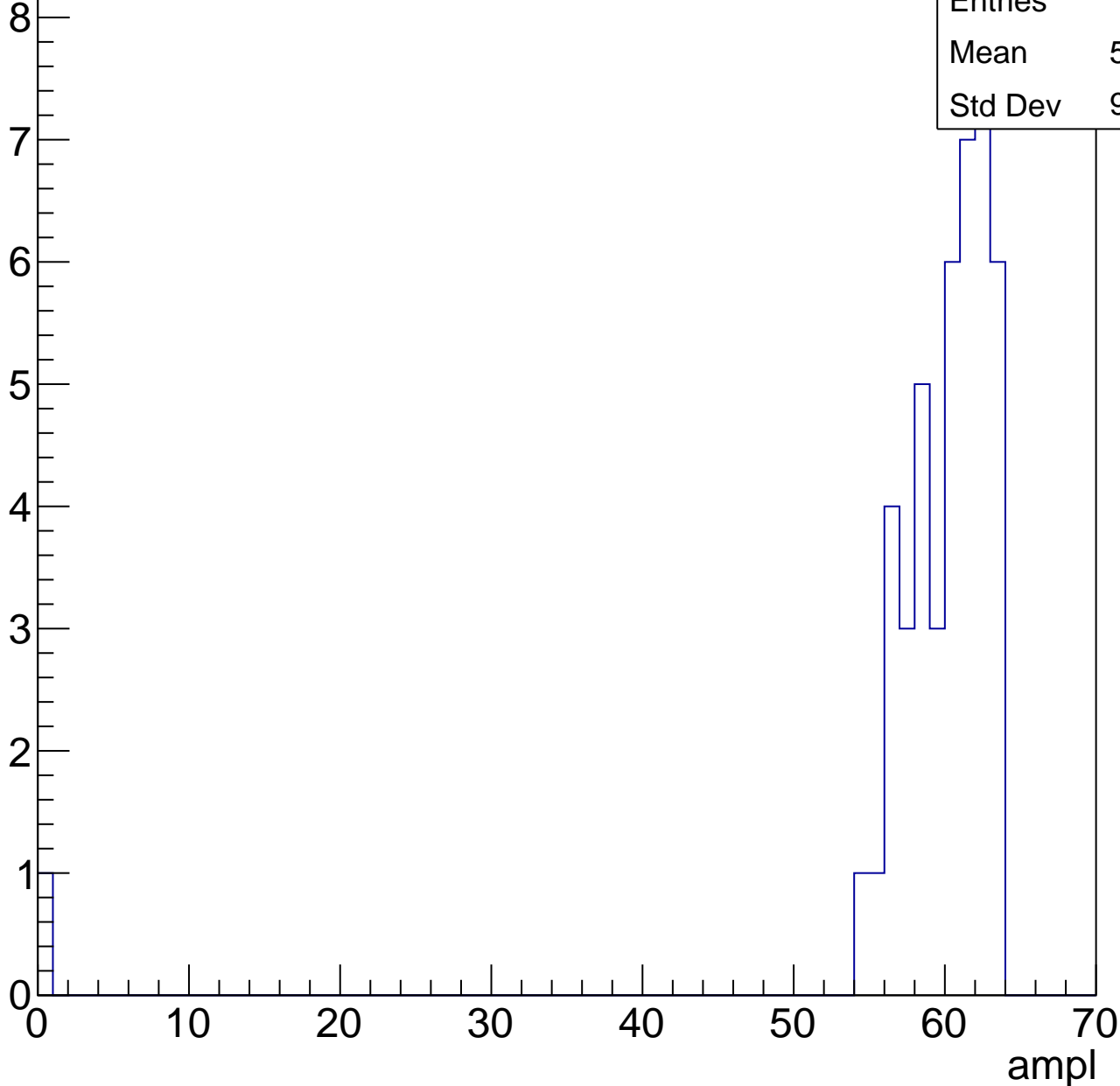


# B1L103S, U9-ch104, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

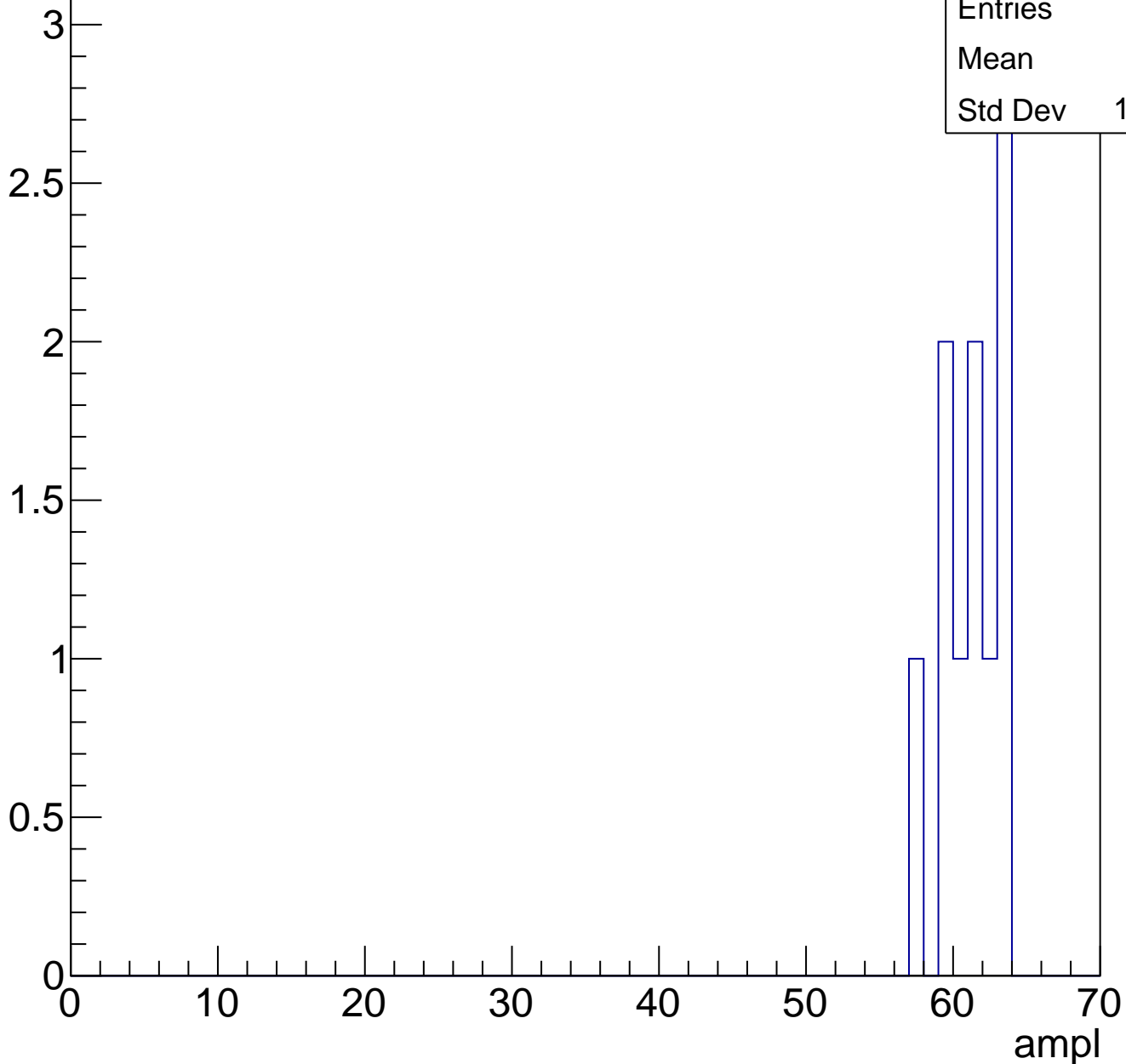
Entries	45
Mean	58.49
Std Dev	9.147



# B1L103S, U9-ch104, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	10
Mean	60.8
Std Dev	1.939



# B1L103S, U9-ch104, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U9-ch105, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	79
Mean	30.28
Std Dev	3.735

**Gaus mean : 29.9850**

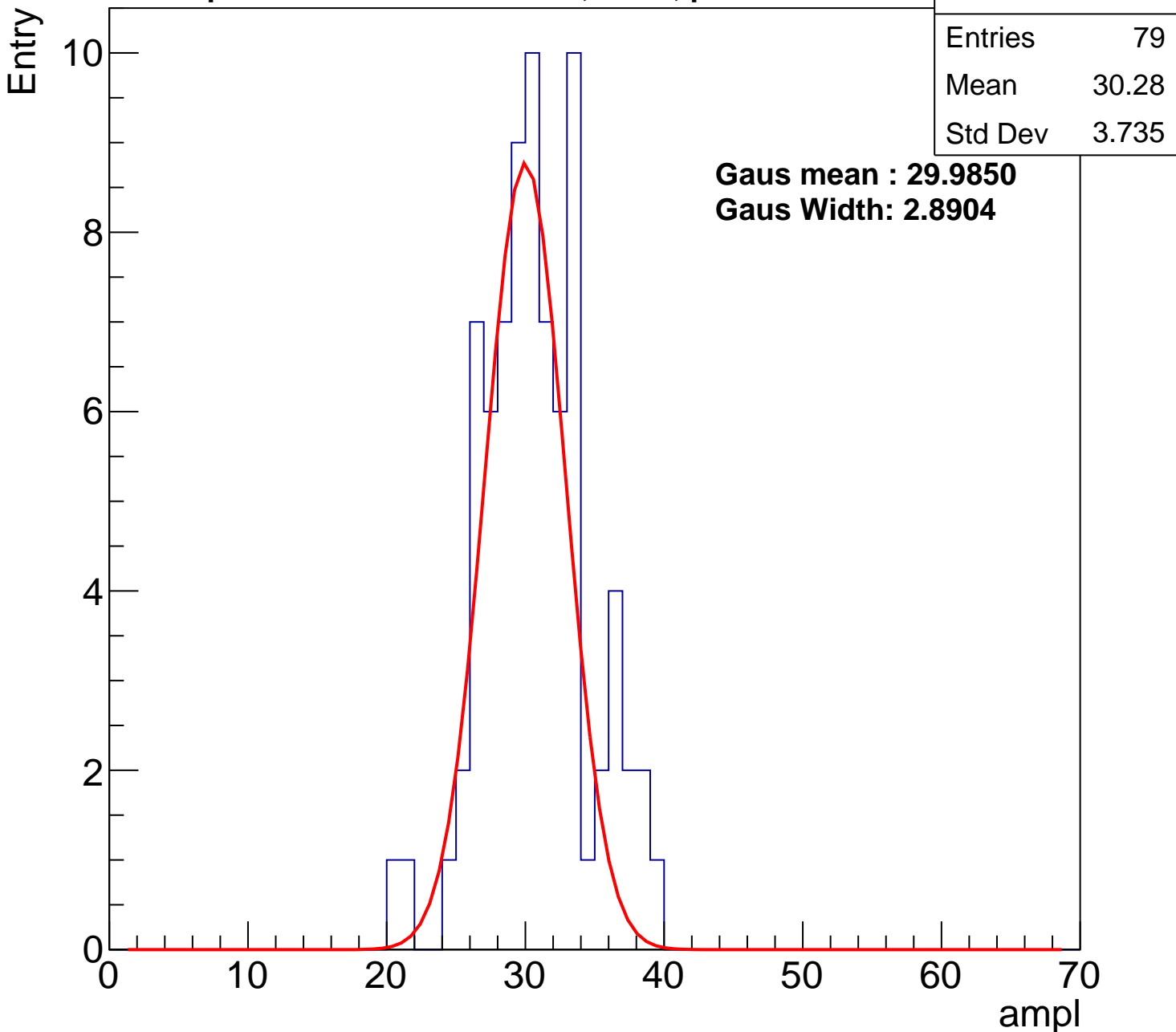
**Gaus Width: 2.8904**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B1L103S, U9-ch105, adc1

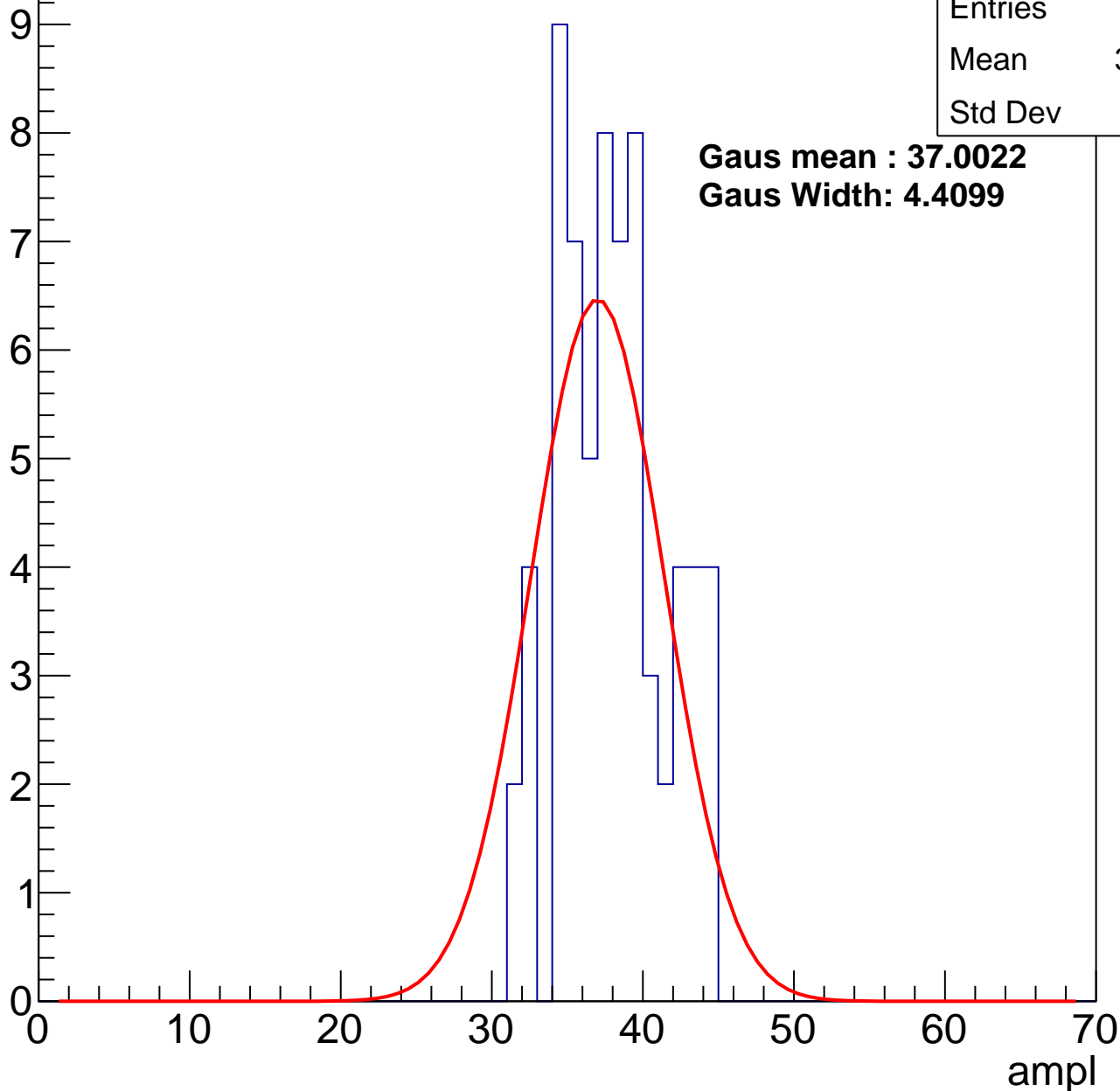
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	37.51
Std Dev	3.47

**Gaus mean : 37.0022**

**Gaus Width: 4.4099**



# B1L103S, U9-ch105, adc2

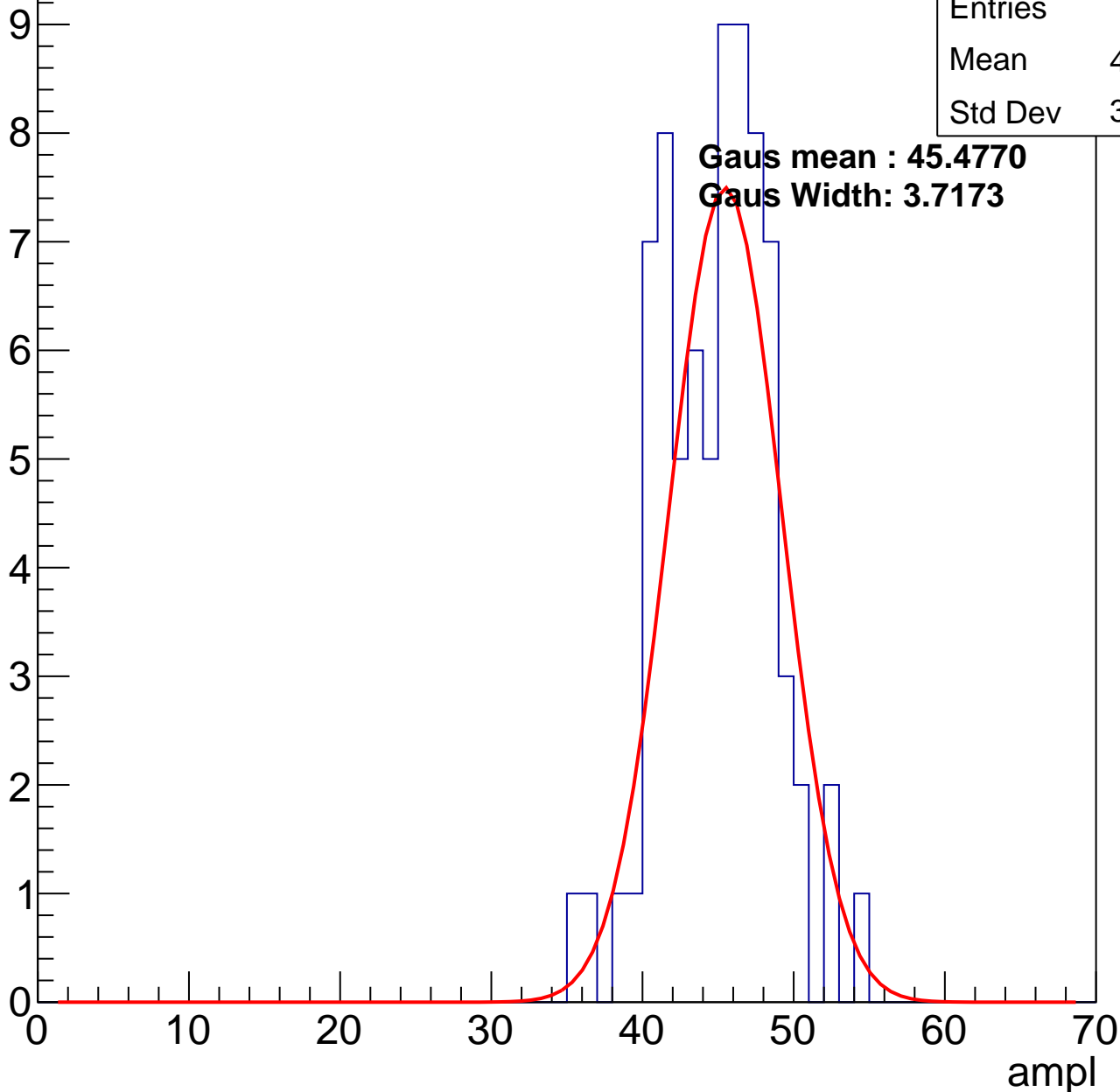
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	76
Mean	44.47
Std Dev	3.633

**Gaus mean : 45.4770**

**Gaus Width: 3.7173**

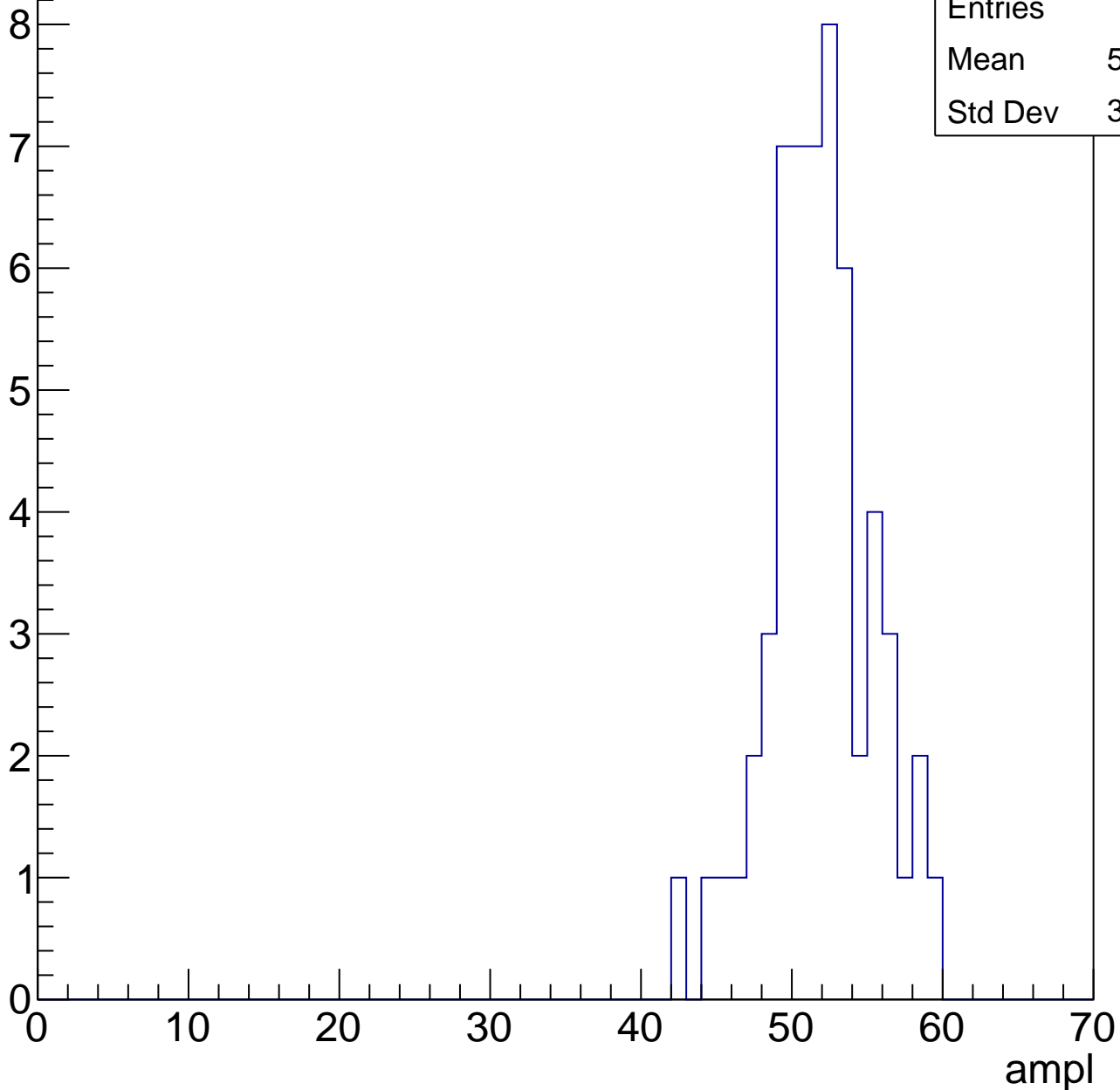


# B1L103S, U9-ch105, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	57
Mean	51.35
Std Dev	3.416

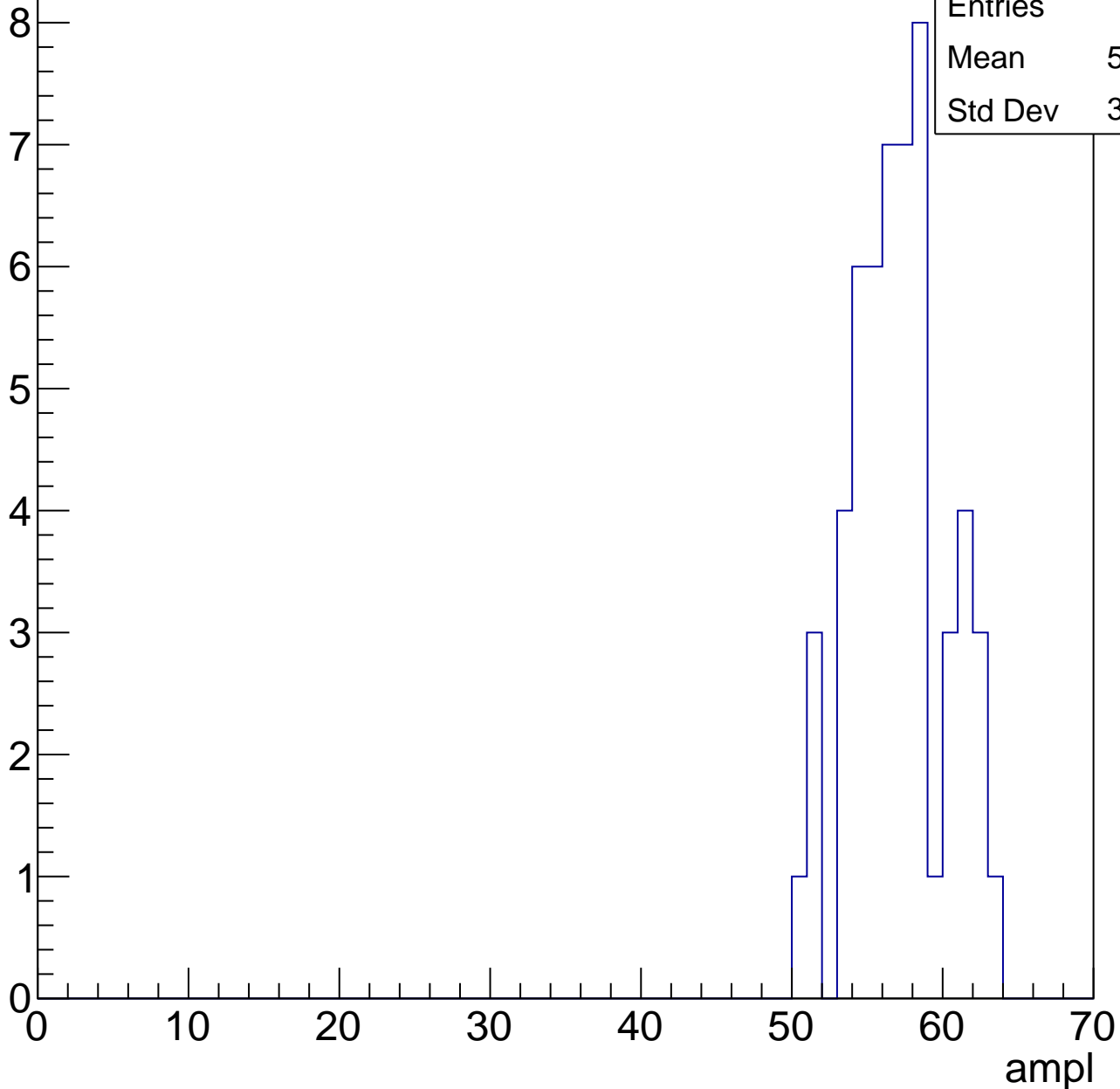


# B1L103S, U9-ch105, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	54
Mean	56.59
Std Dev	3.076

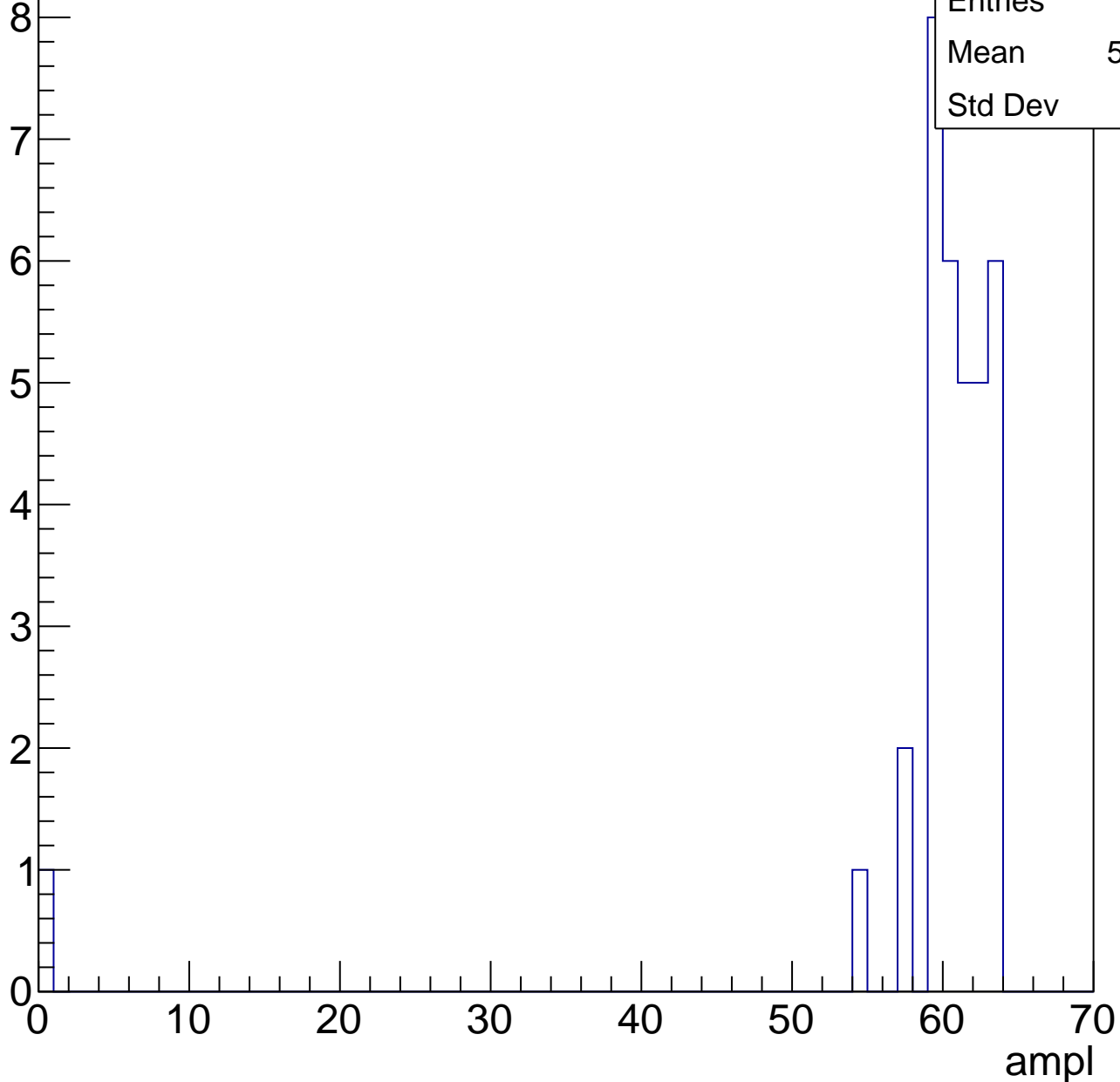


# B1L103S, U9-ch105, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	34
Mean	58.62
Std Dev	10.4



# B1L103S, U9-ch105, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	7
Mean	62
Std Dev	1.069



# B1L103S, U9-ch105, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U9-ch106, adc0

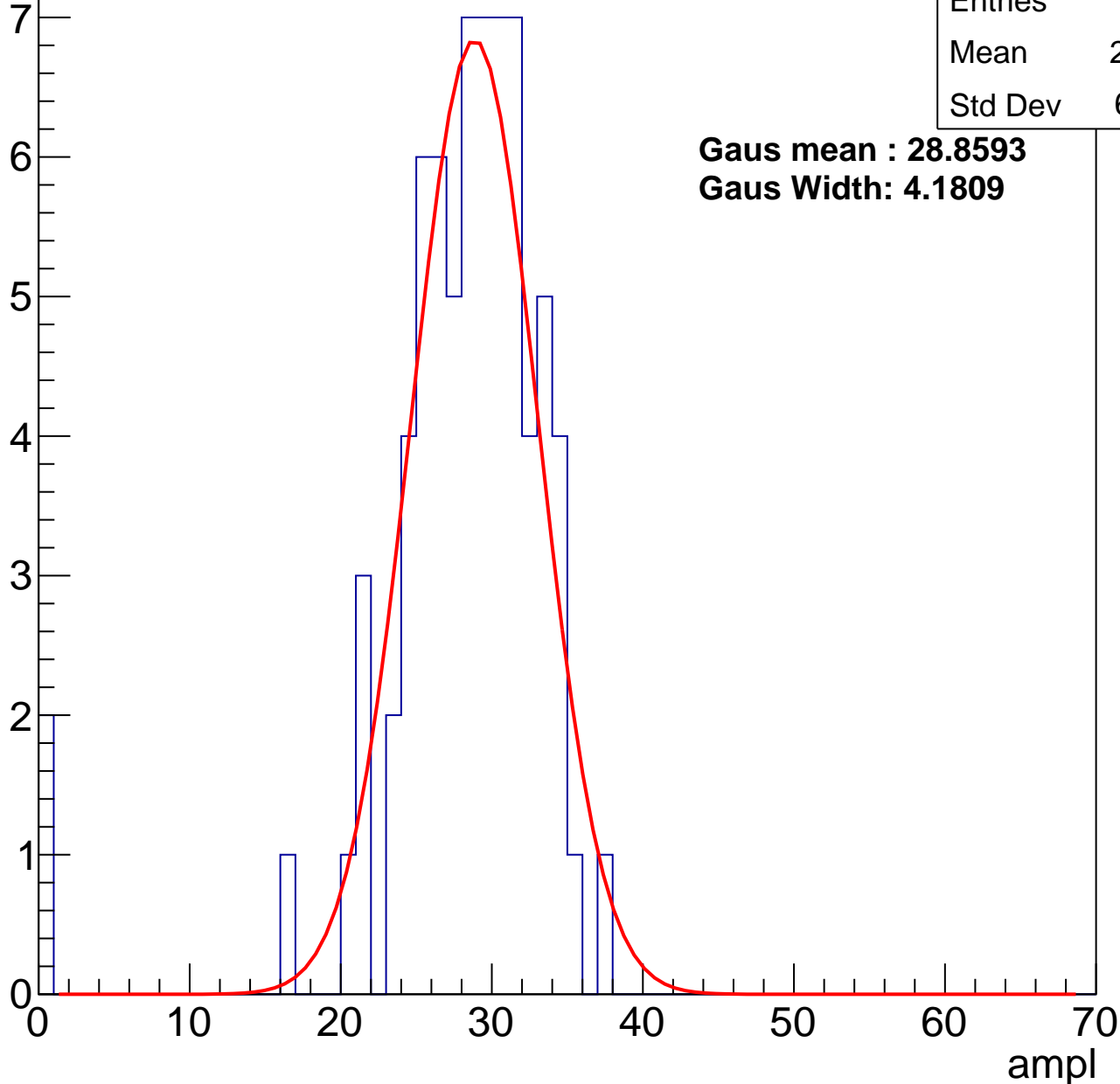
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	73
Mean	27.52
Std Dev	6.041

**Gaus mean : 28.8593**

**Gaus Width: 4.1809**



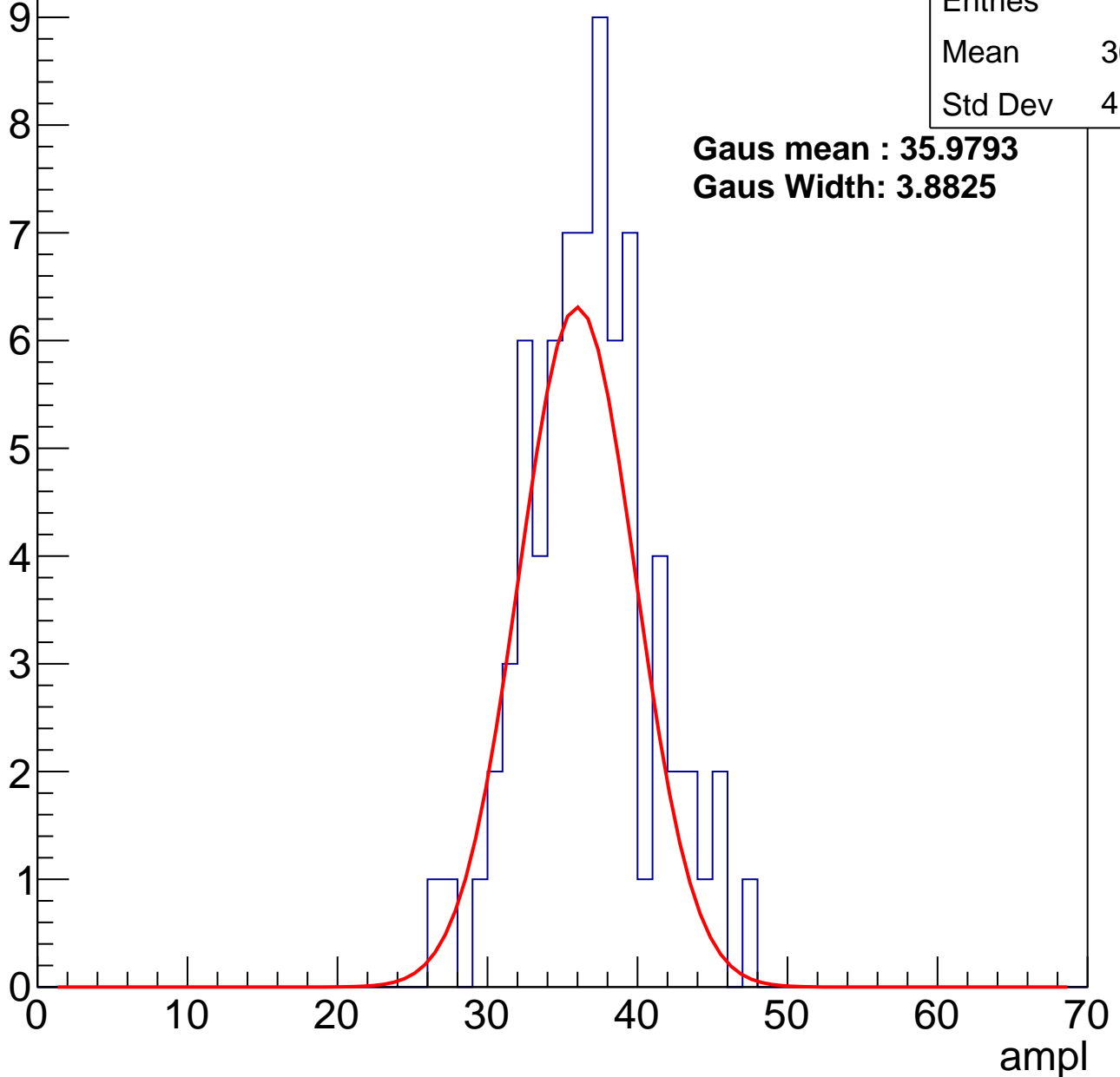
# B1L103S, U9-ch106, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	73
Mean	36.29
Std Dev	4.159

**Gaus mean : 35.9793**  
**Gaus Width: 3.8825**



# B1L103S, U9-ch106, adc2

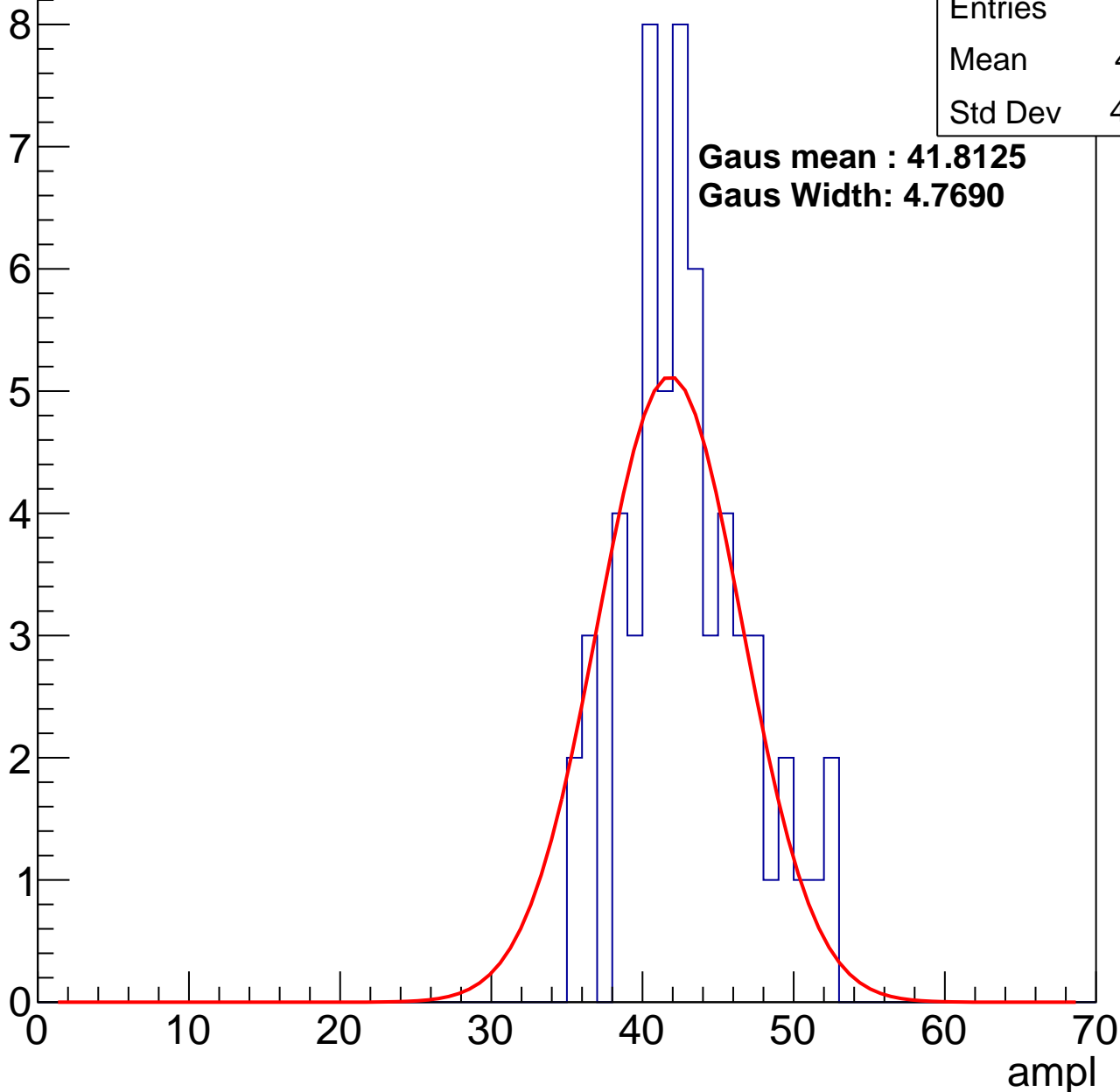
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	59
Mean	42.51
Std Dev	4.065

**Gaus mean : 41.8125**

**Gaus Width: 4.7690**

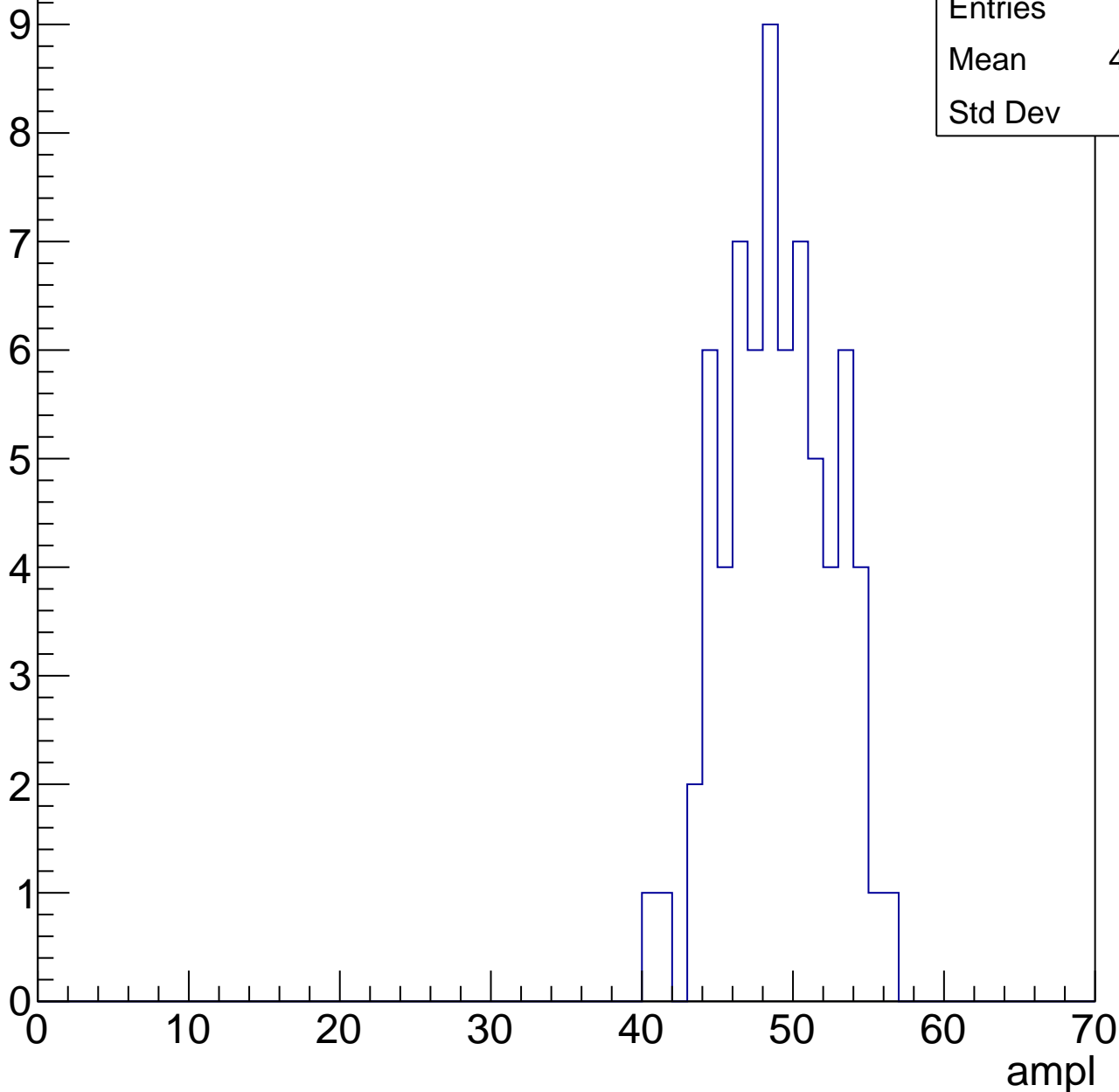


# B1L103S, U9-ch106, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

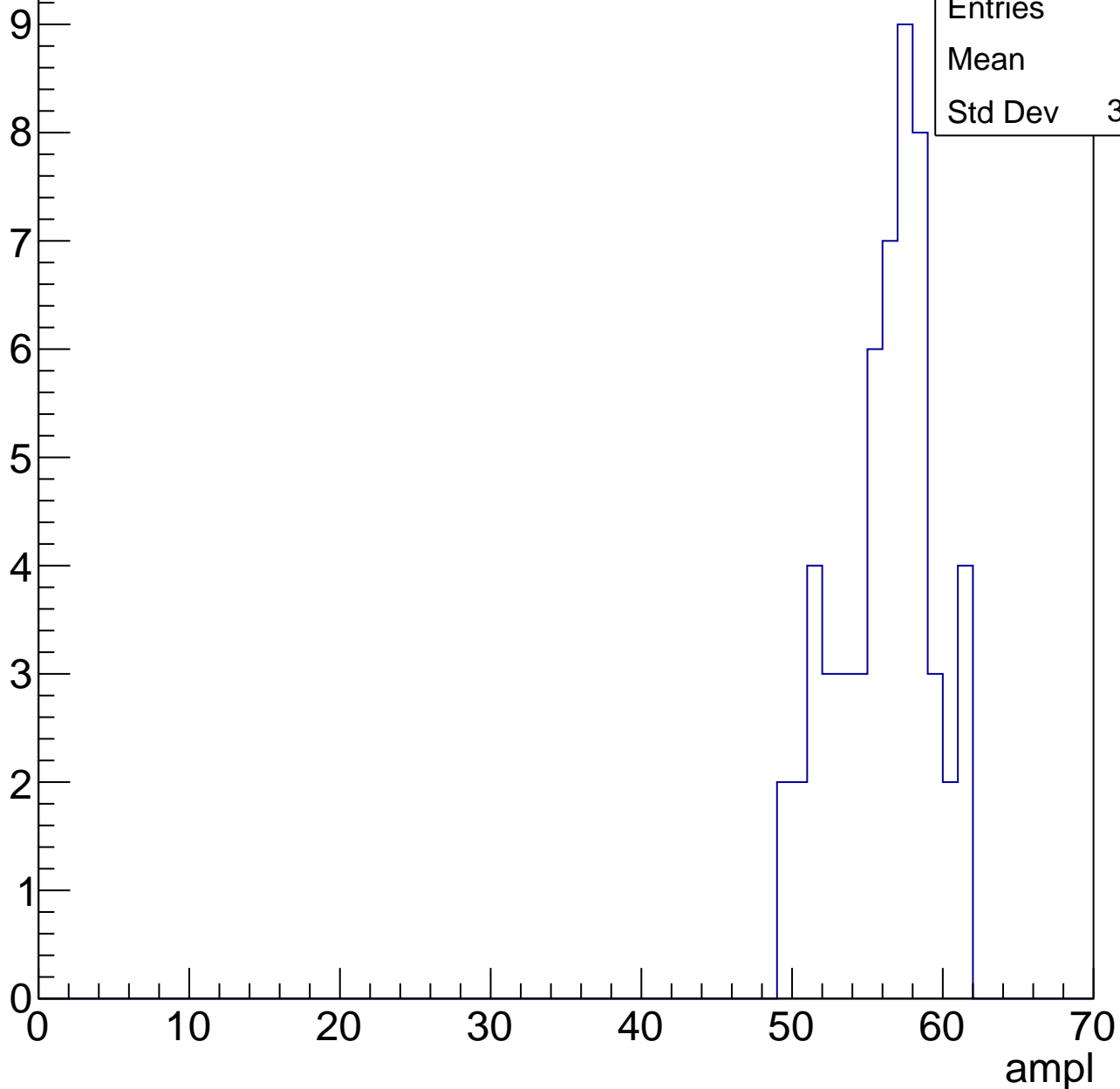
Entries	70
Mean	48.56
Std Dev	3.5



# B1L103S, U9-ch106, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



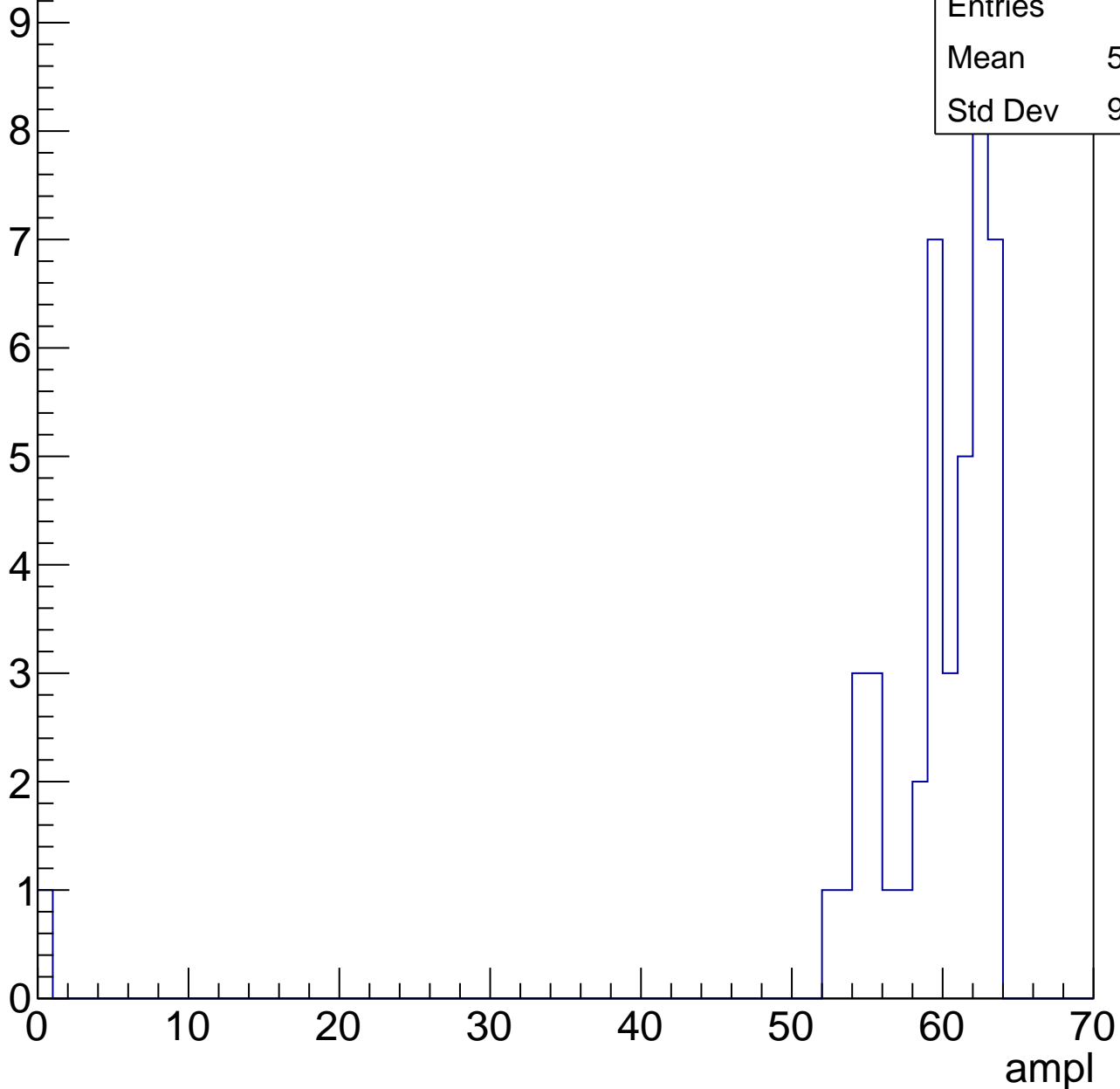
Entries	56
Mean	55.7
Std Dev	3.156

# B1L103S, U9-ch106, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

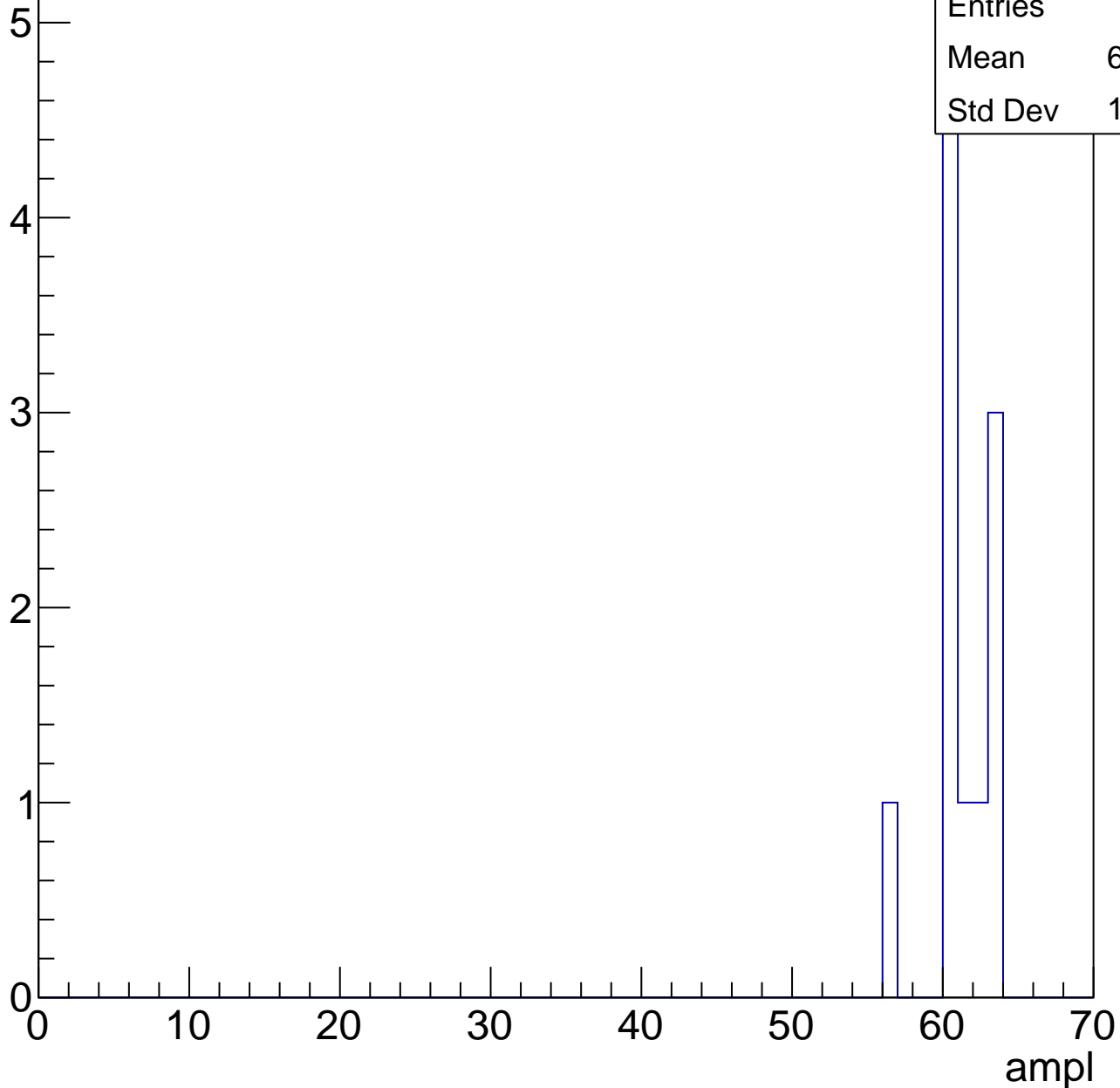
Entries	44
Mean	58.14
Std Dev	9.399



# B1L103S, U9-ch106, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U9-ch106, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U9-ch107, adc0

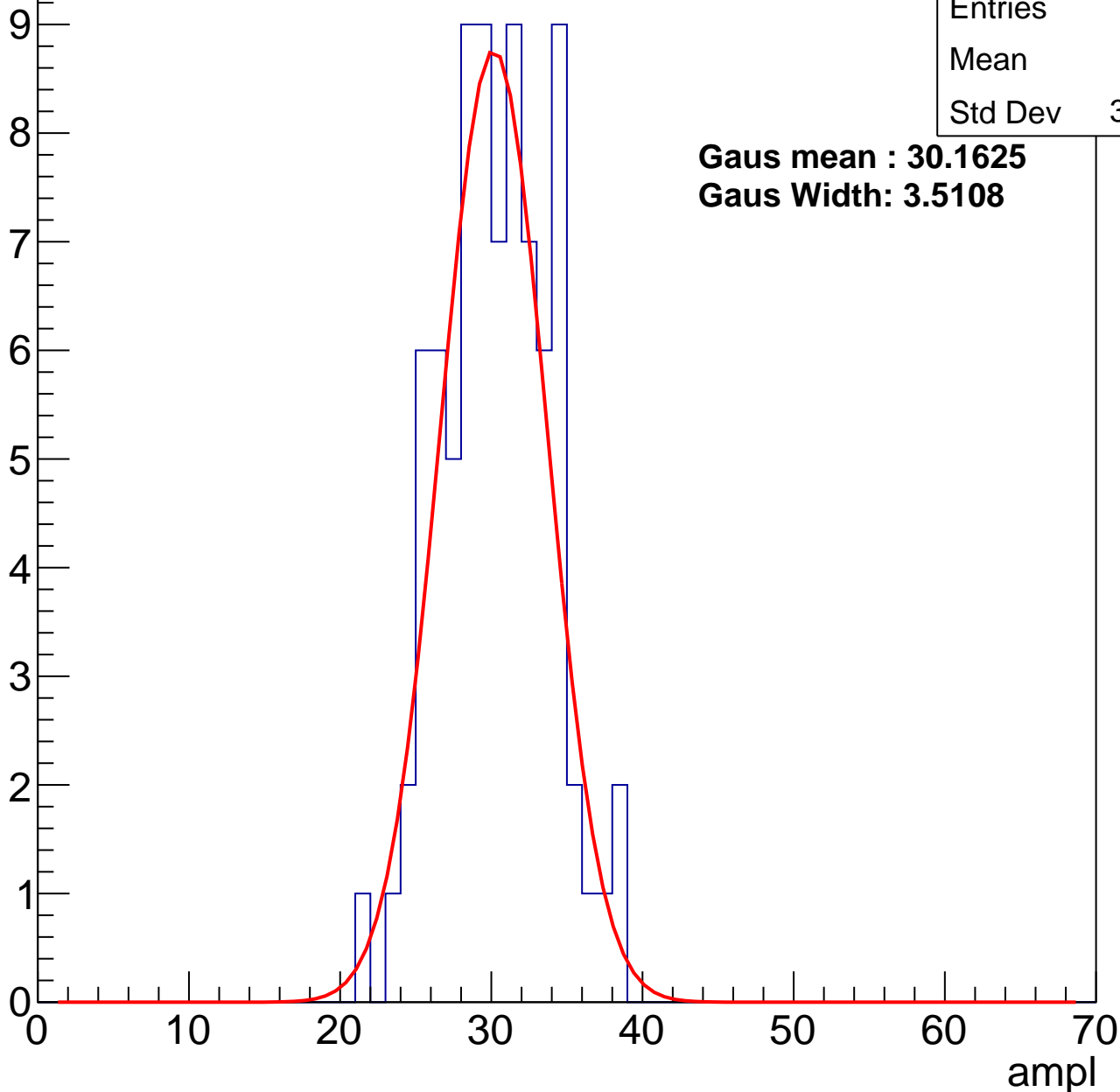
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	83
Mean	29.9
Std Dev	3.532

**Gaus mean : 30.1625**

**Gaus Width: 3.5108**



# B1L103S, U9-ch107, adc1

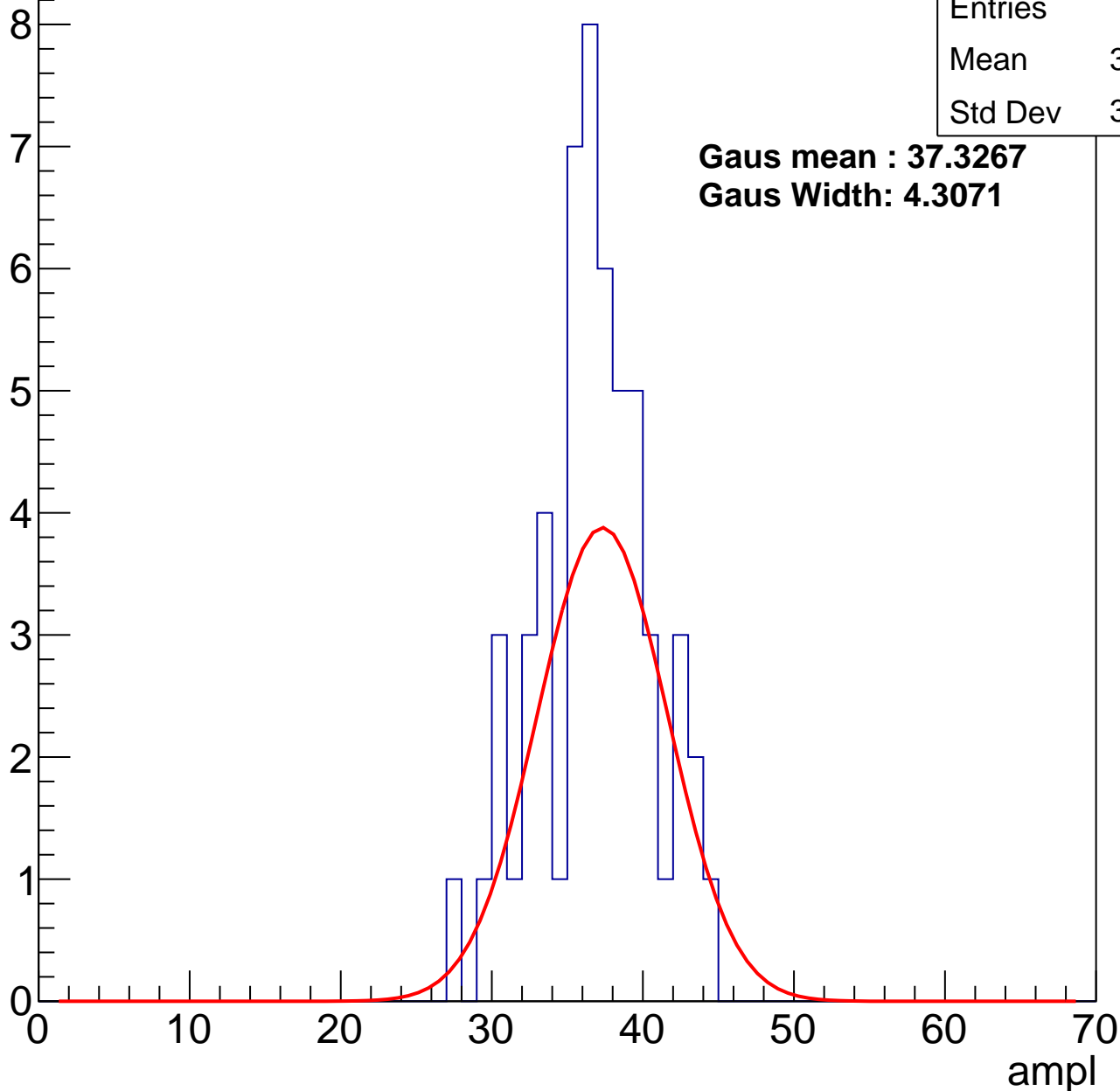
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	55
Mean	36.29
Std Dev	3.735

**Gaus mean : 37.3267**

**Gaus Width: 4.3071**



# B1L103S, U9-ch107, adc2

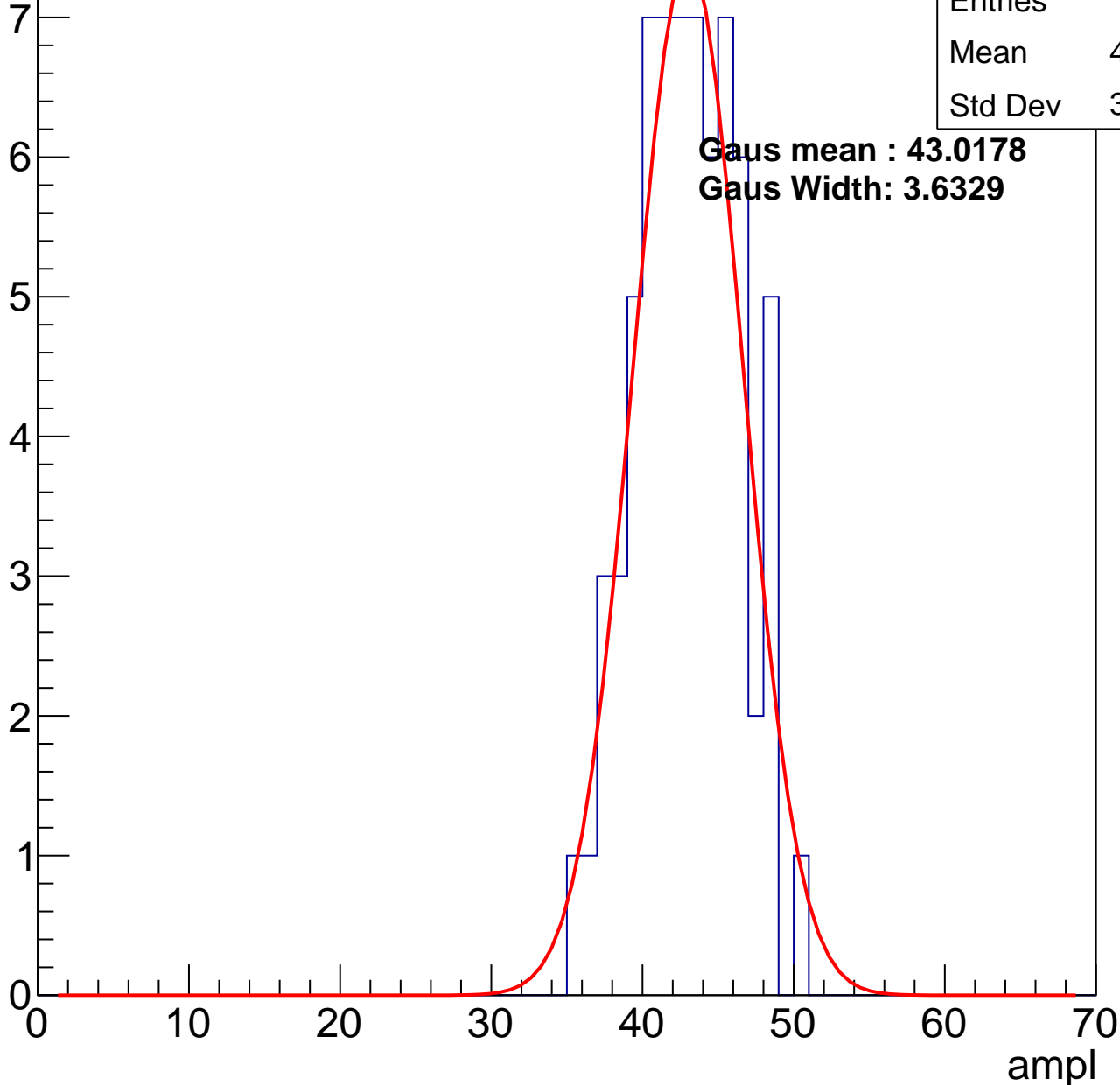
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	68
Mean	42.53
Std Dev	3.328

**Gaus mean : 43.0178**

**Gaus Width: 3.6329**

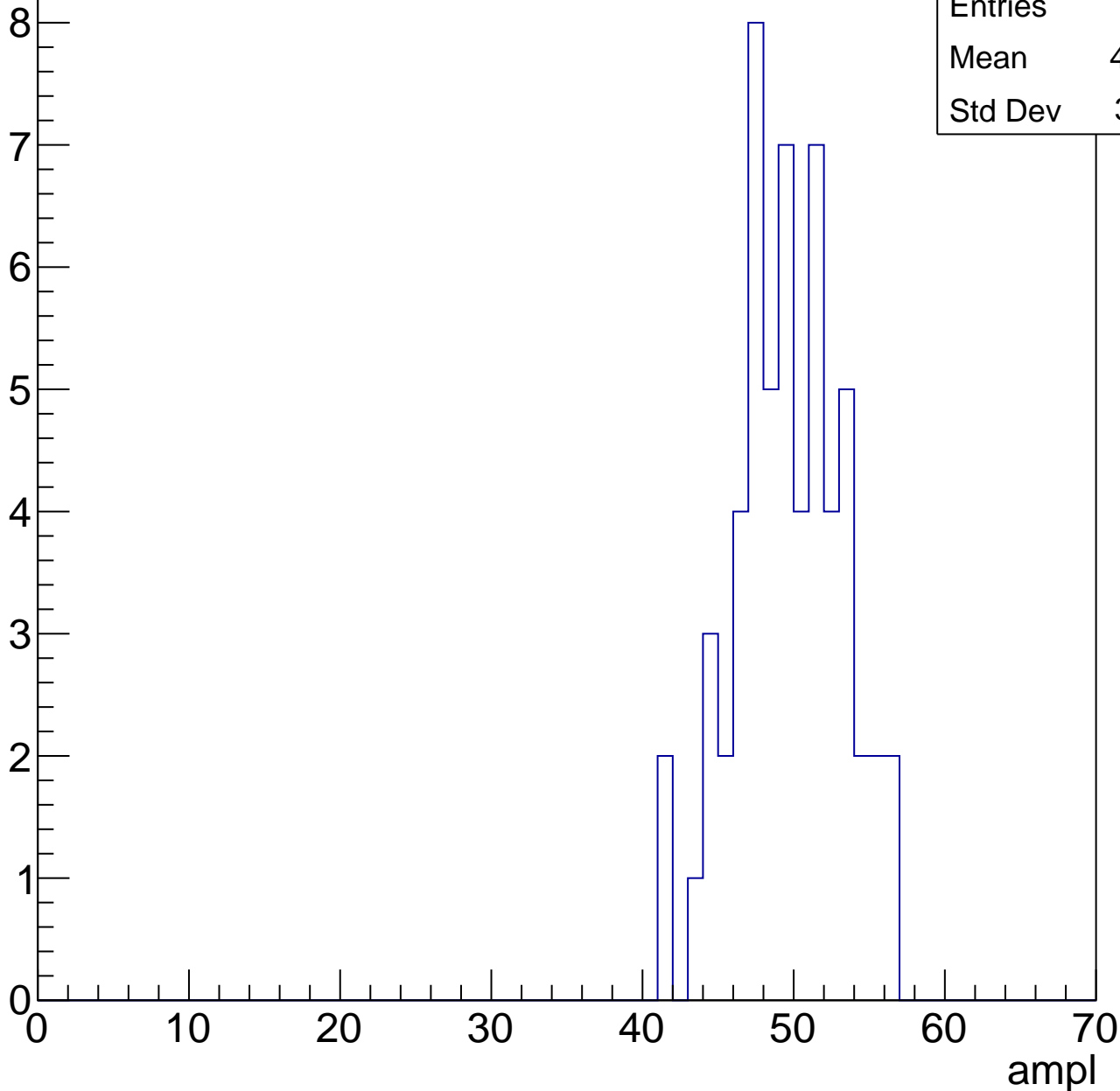


# B1L103S, U9-ch107, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	58
Mean	49.14
Std Dev	3.501

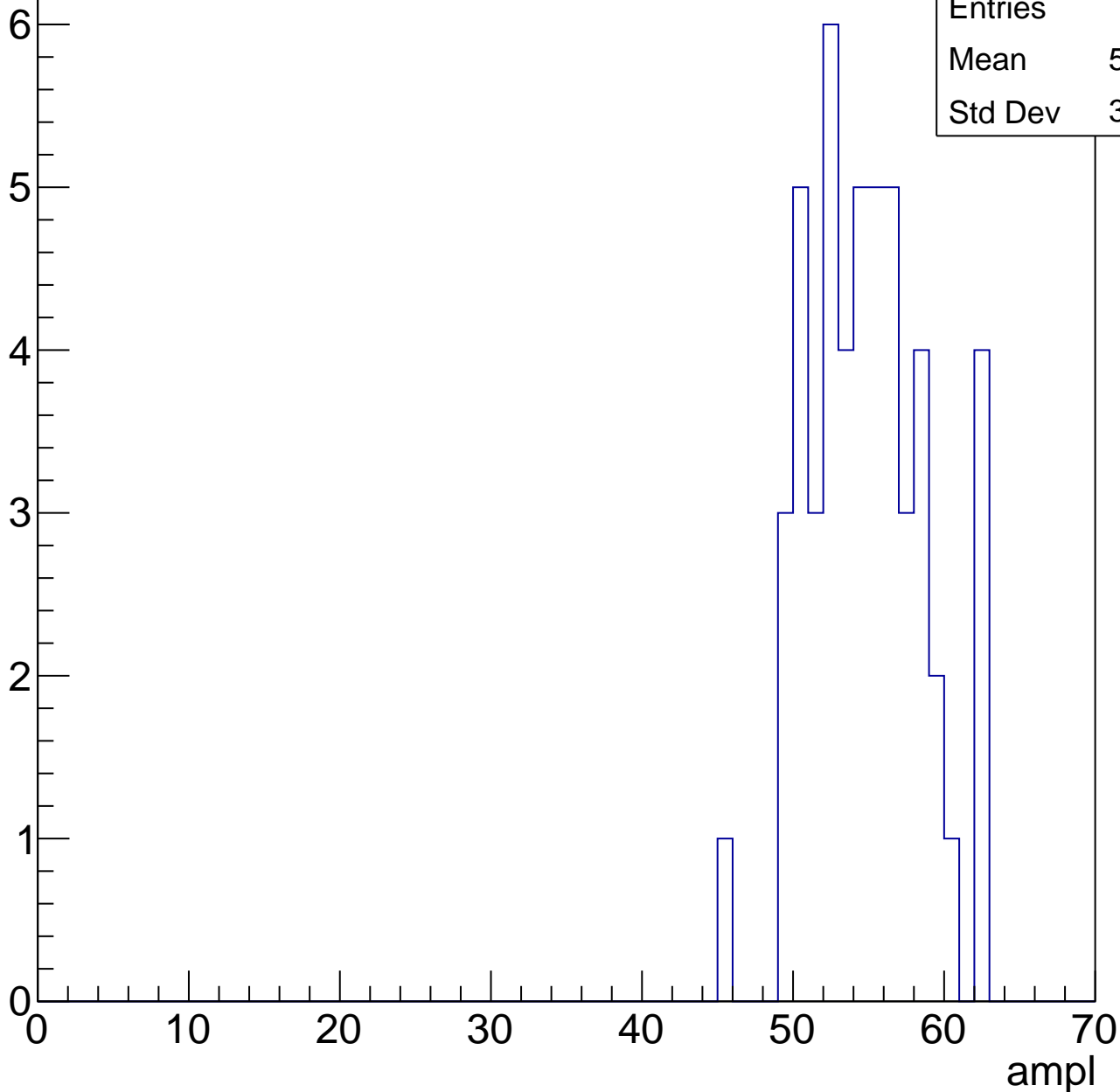


# B1L103S, U9-ch107, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	51
Mean	54.37
Std Dev	3.814



# B1L103S, U9-ch107, adc5

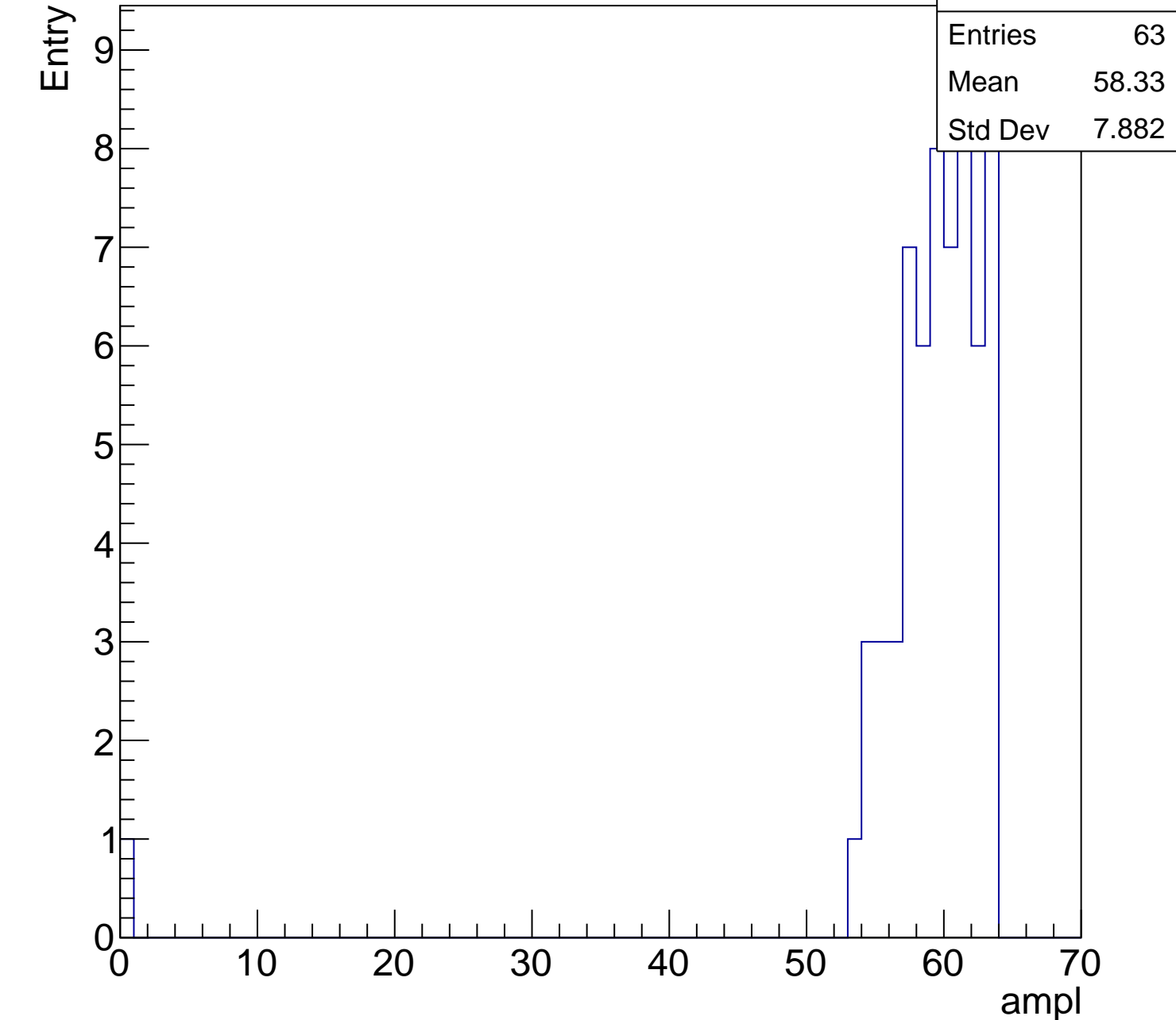
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	63
Mean	58.33
Std Dev	7.882

ampl



# B1L103S, U9-ch107, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	4
Mean	61
Std Dev	1.225

ampl

0 10 20 30 40 50 60 70



# B1L103S, U9-ch107, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U9-ch108, adc0

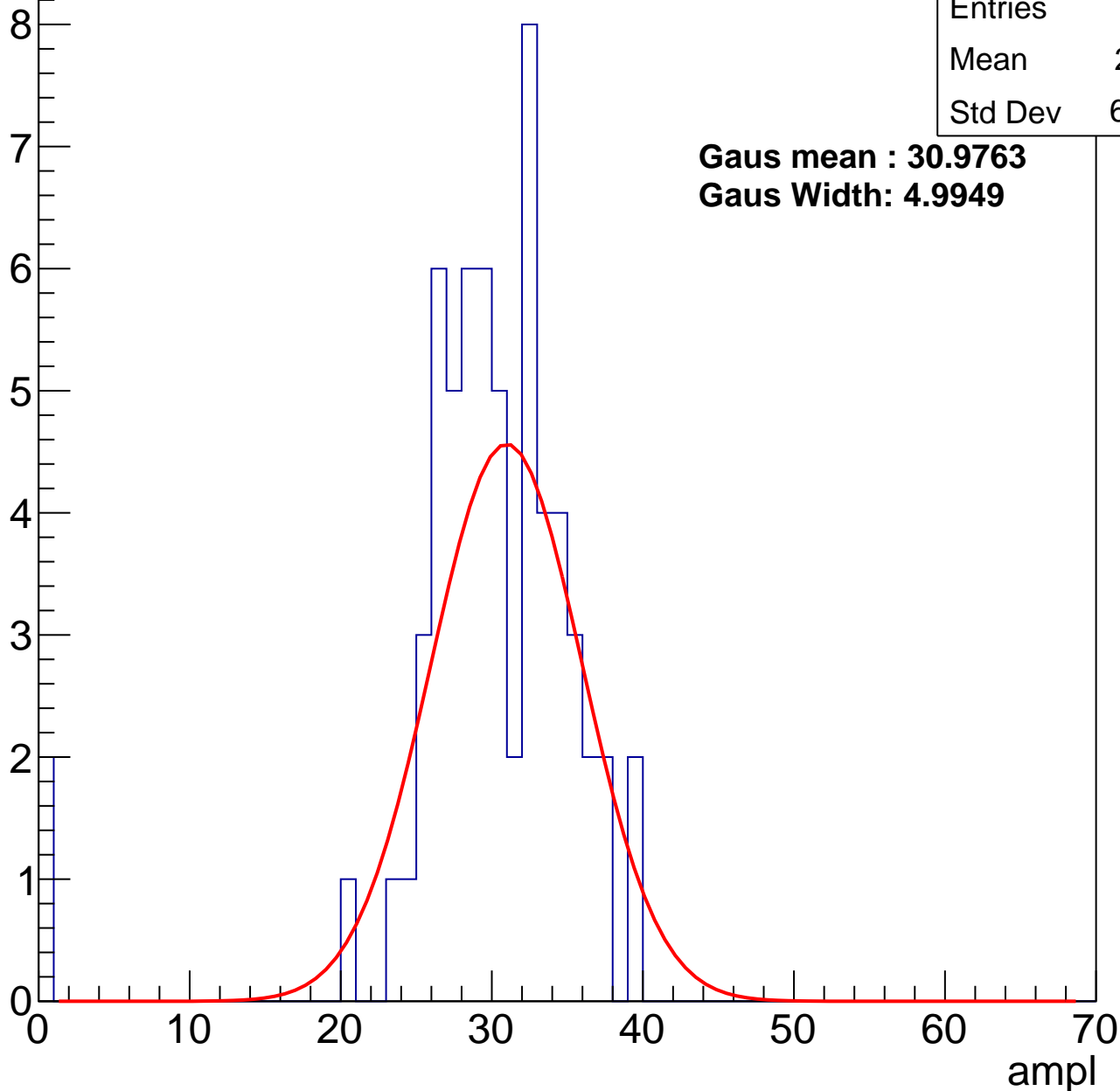
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	29.21
Std Dev	6.586

**Gaus mean : 30.9763**

**Gaus Width: 4.9949**



# B1L103S, U9-ch108, adc1

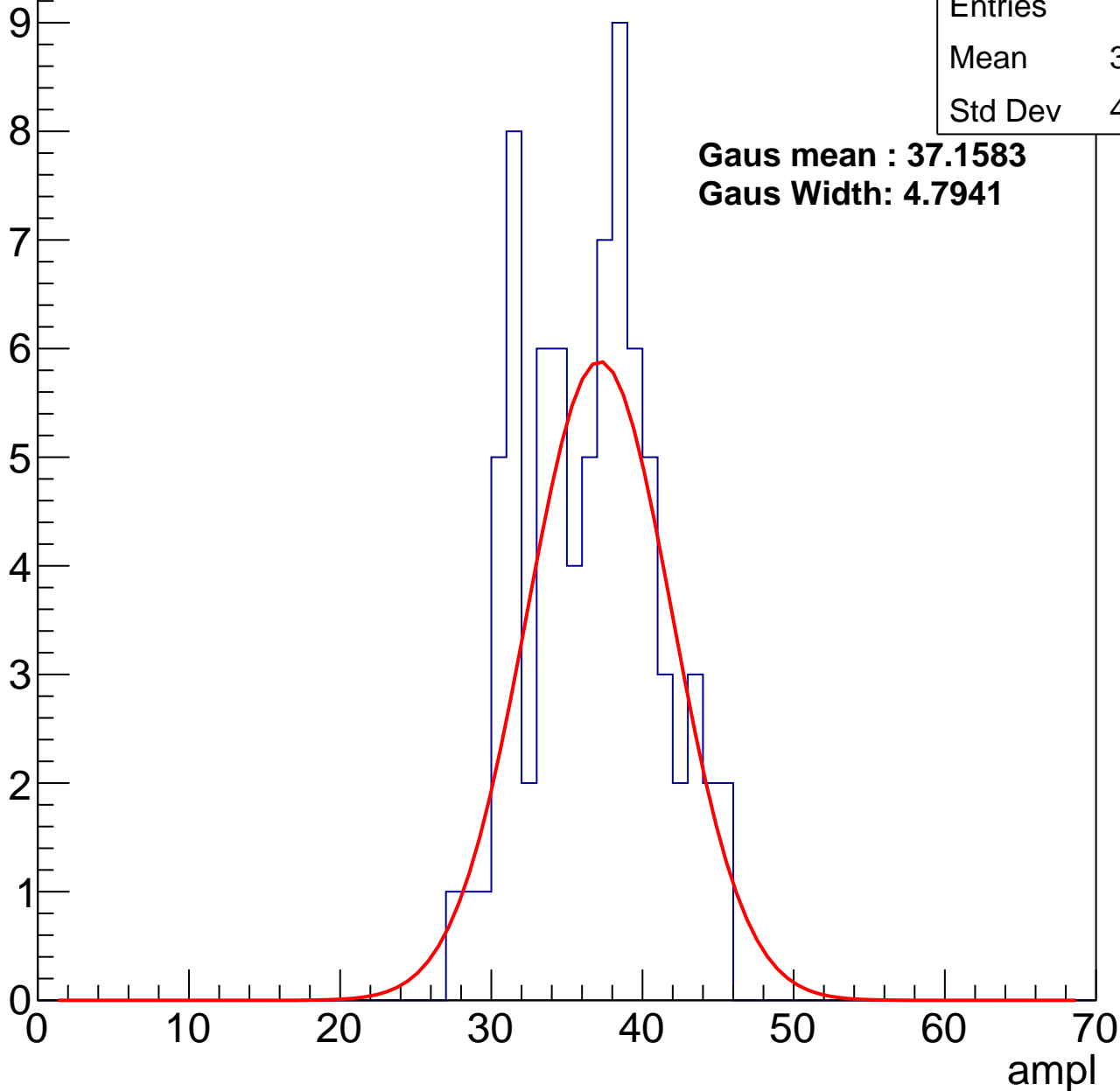
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	78
Mean	36.12
Std Dev	4.309

**Gaus mean : 37.1583**

**Gaus Width: 4.7941**



# B1L103S, U9-ch108, adc2

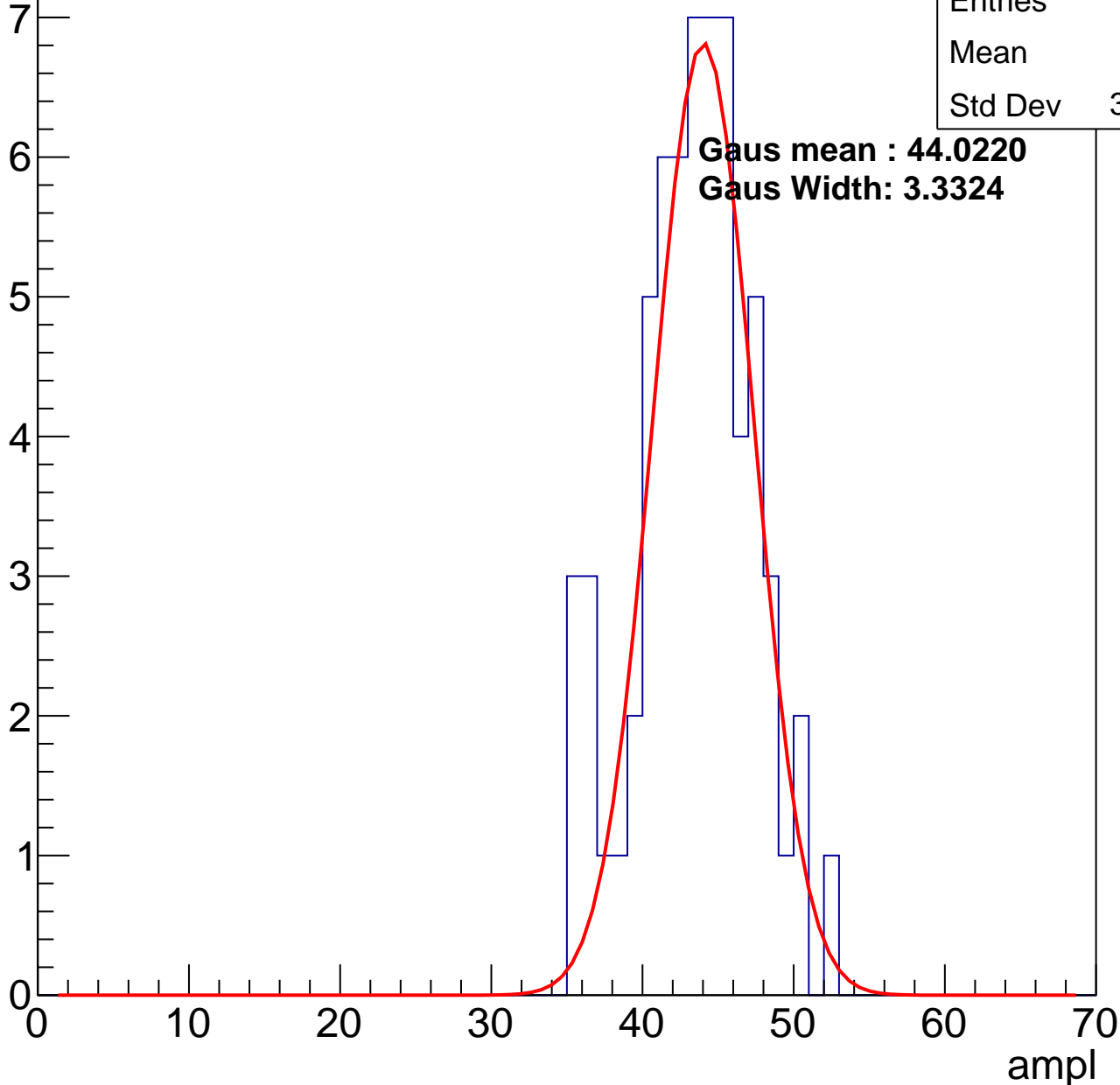
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	43
Std Dev	3.849

**Gaus mean : 44.0220**

**Gaus Width: 3.3324**

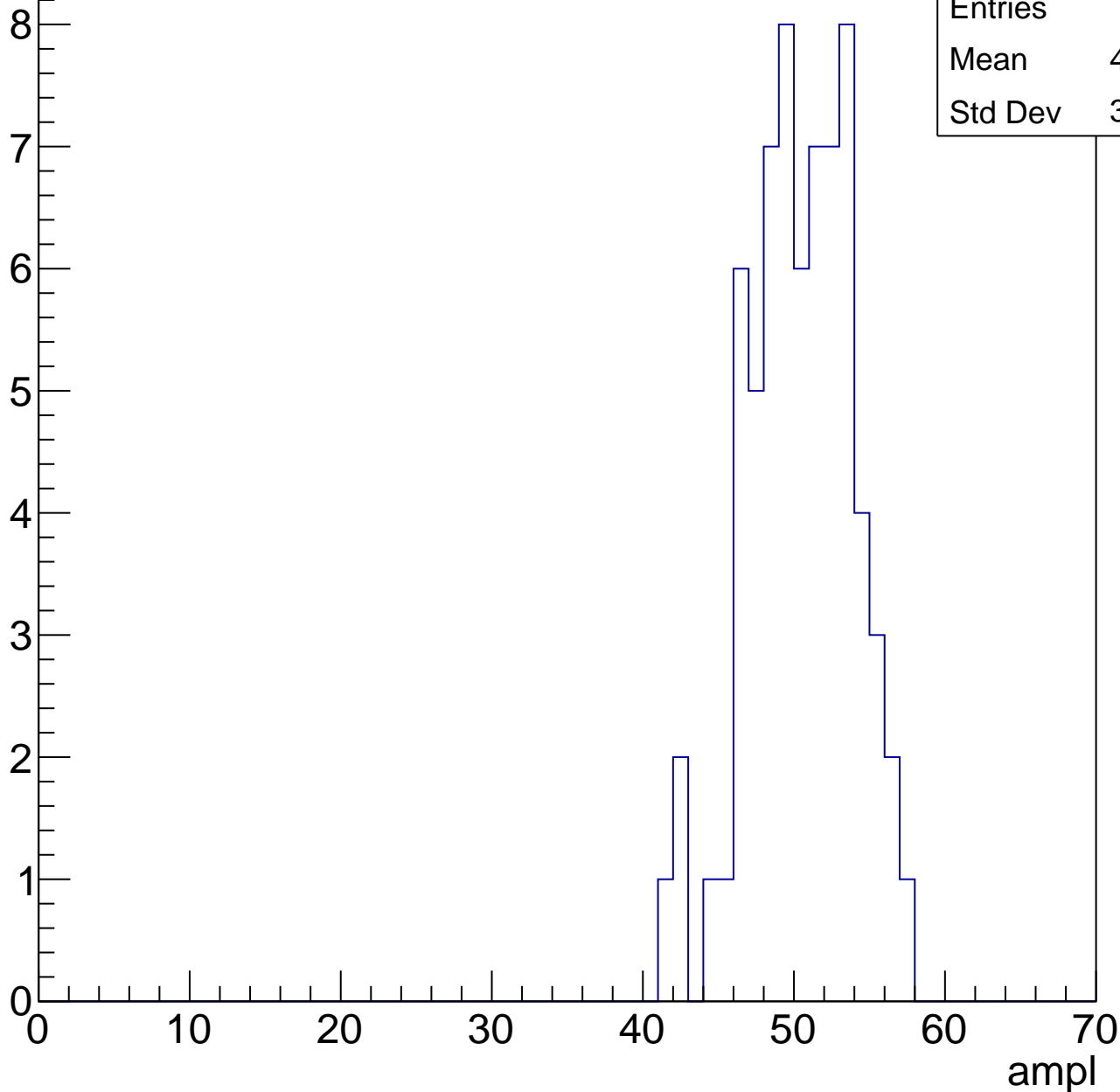


# B1L103S, U9-ch108, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	69
Mean	49.97
Std Dev	3.435



# B1L103S, U9-ch108, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	62
Mean	56.48
Std Dev	3.083

Entry

10

8

6

4

2

0

0

10

20

30

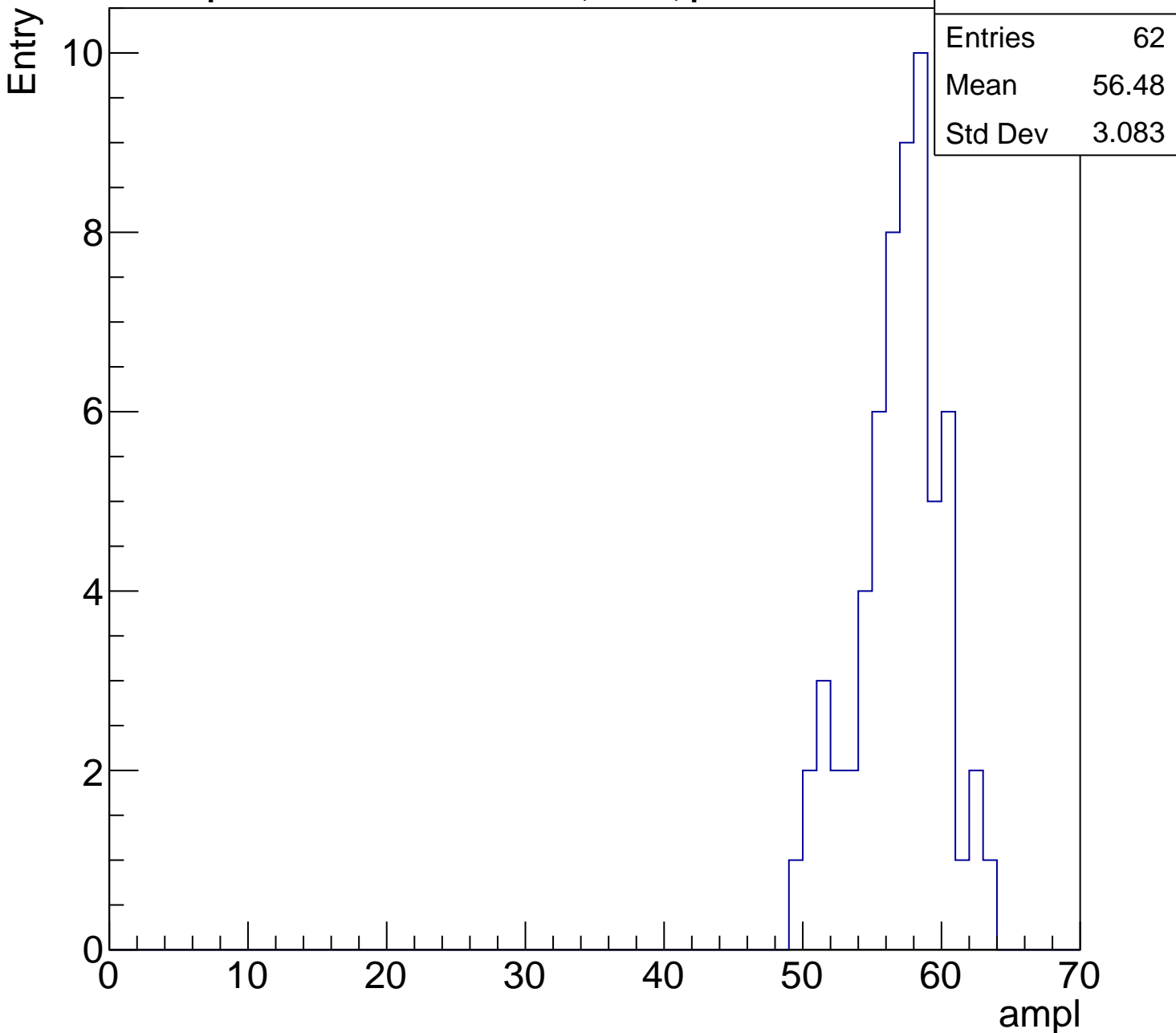
40

50

60

ampl

70

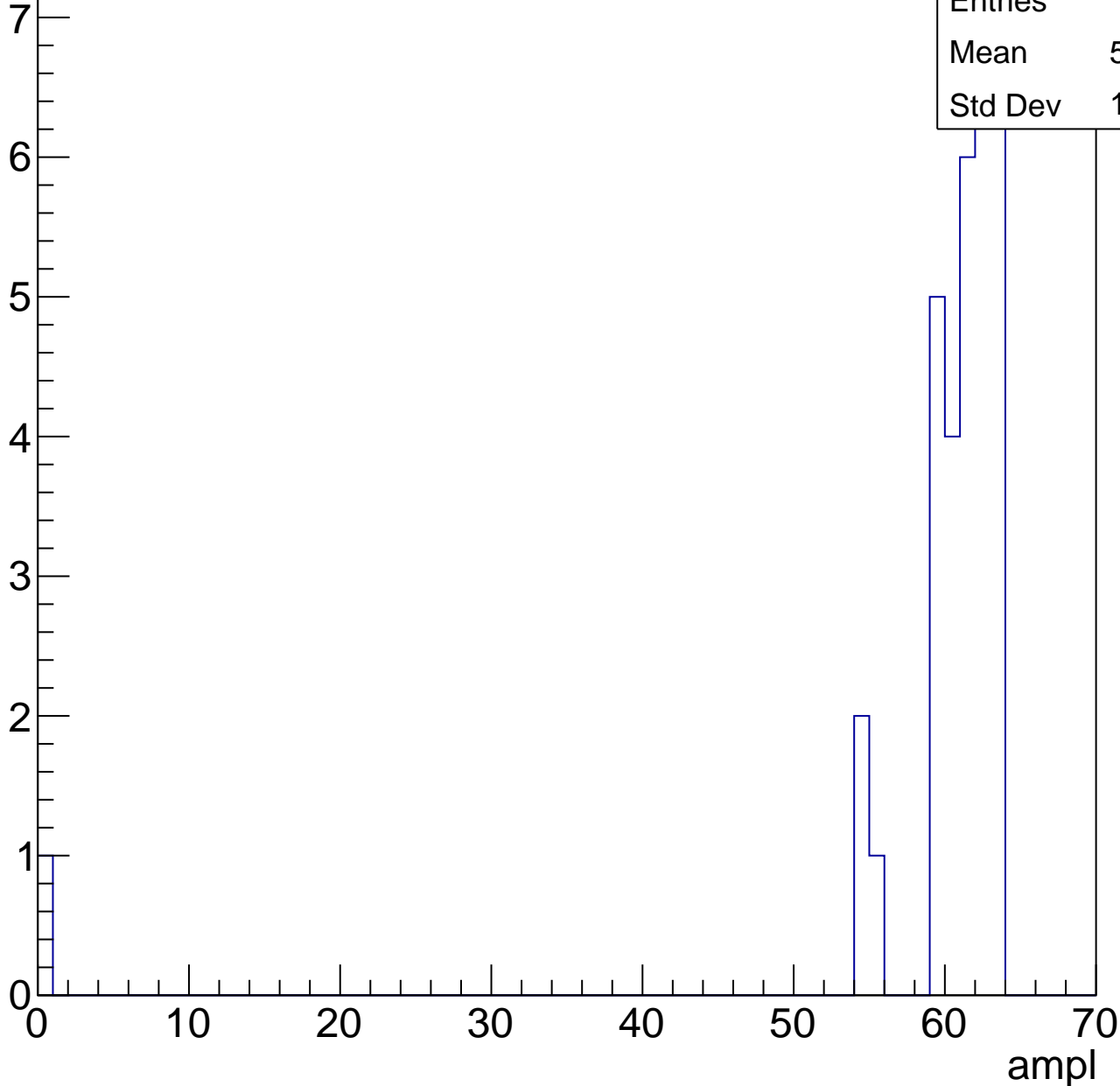


# B1L103S, U9-ch108, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

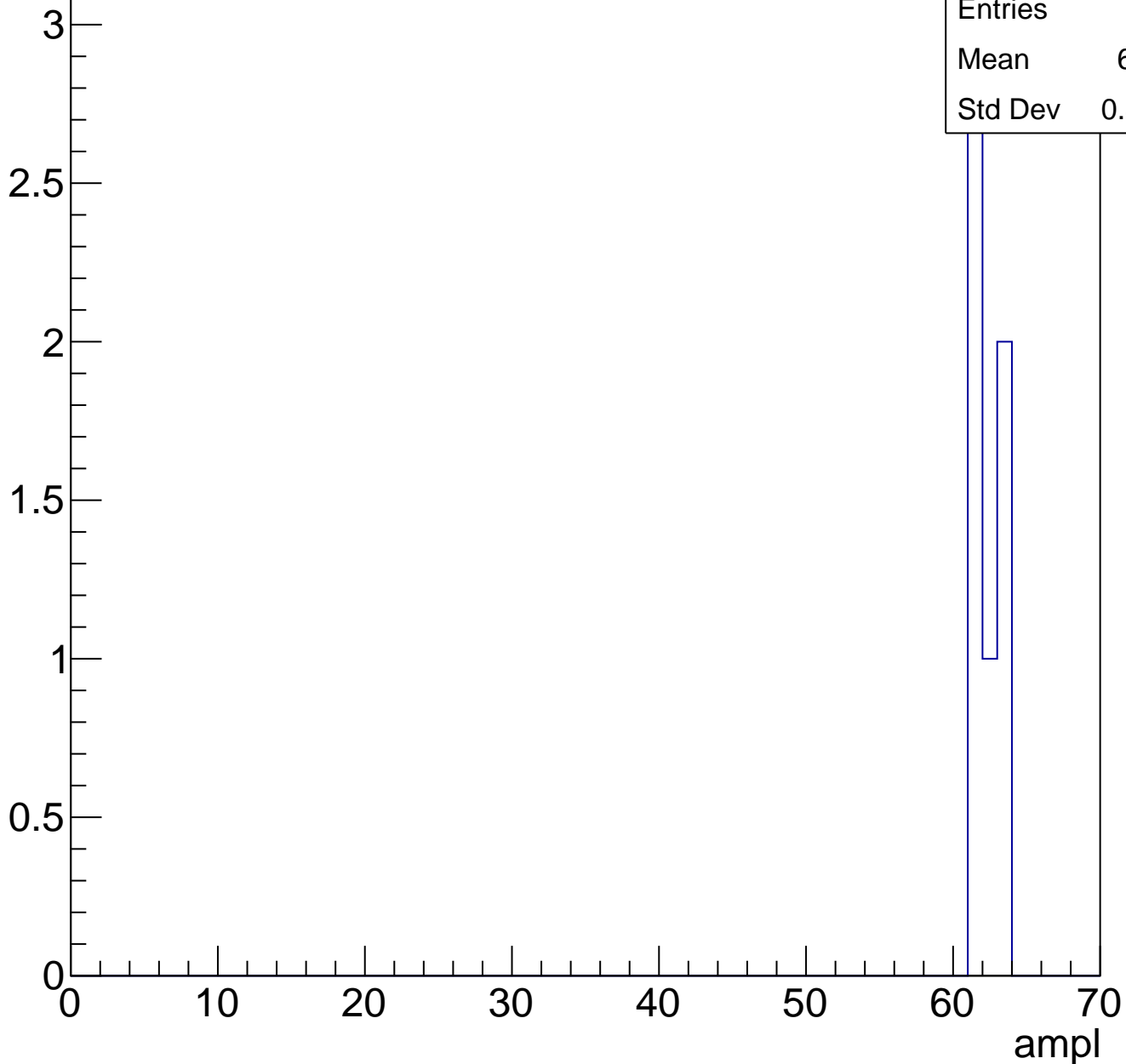
Entries	33
Mean	58.76
Std Dev	10.66



# B1L103S, U9-ch108, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U9-ch108, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U9-ch109, adc0

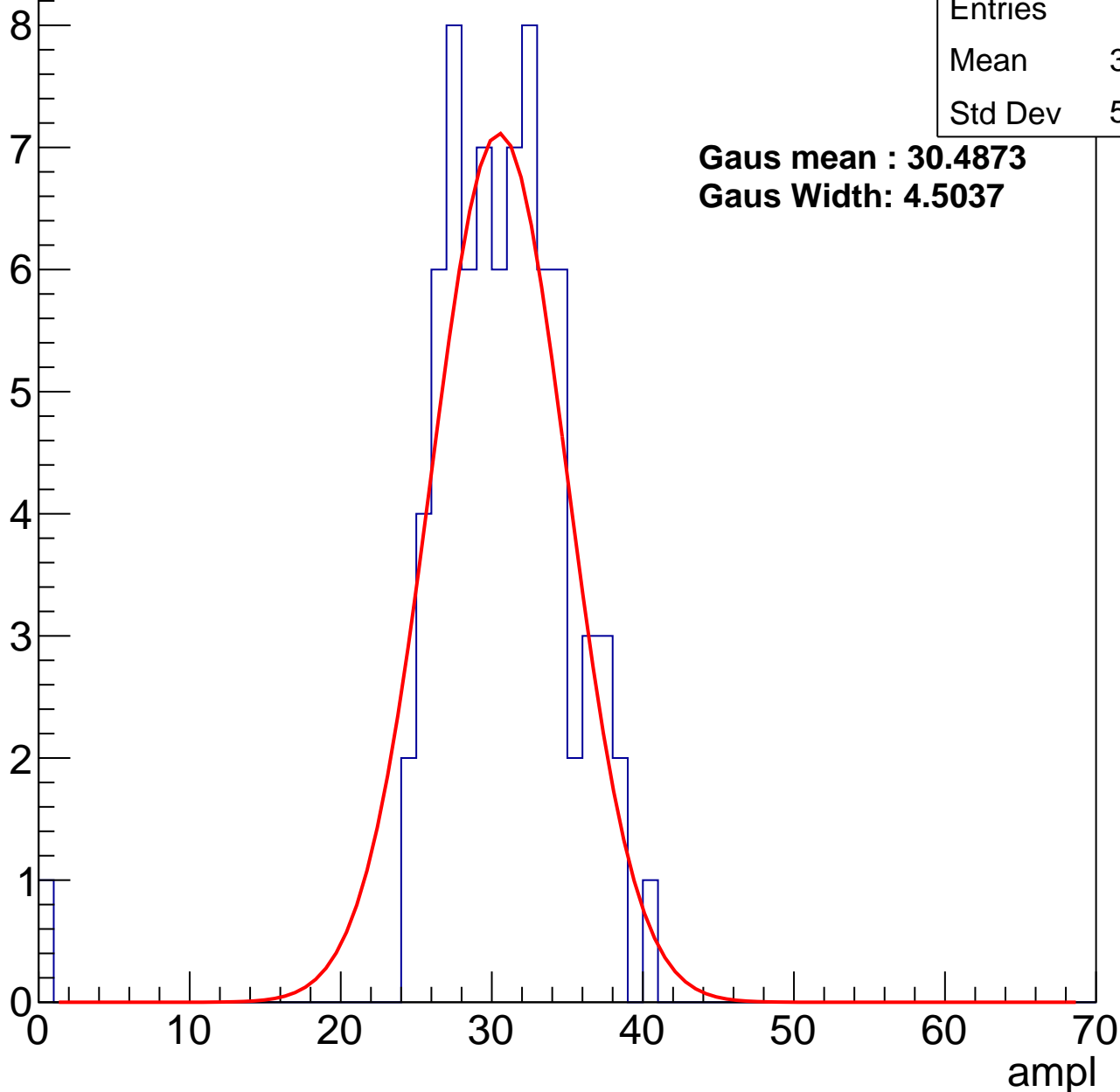
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	78
Mean	30.14
Std Dev	5.053

**Gaus mean : 30.4873**

**Gaus Width: 4.5037**



# B1L103S, U9-ch109, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	37.95
Std Dev	3.484

7

6

5

4

3

2

1

0

**Gaus mean : 38.3167**

**Gaus Width: 4.1403**

0

10

20

30

40

50

60

70

ampl

# B1L103S, U9-ch109, adc2

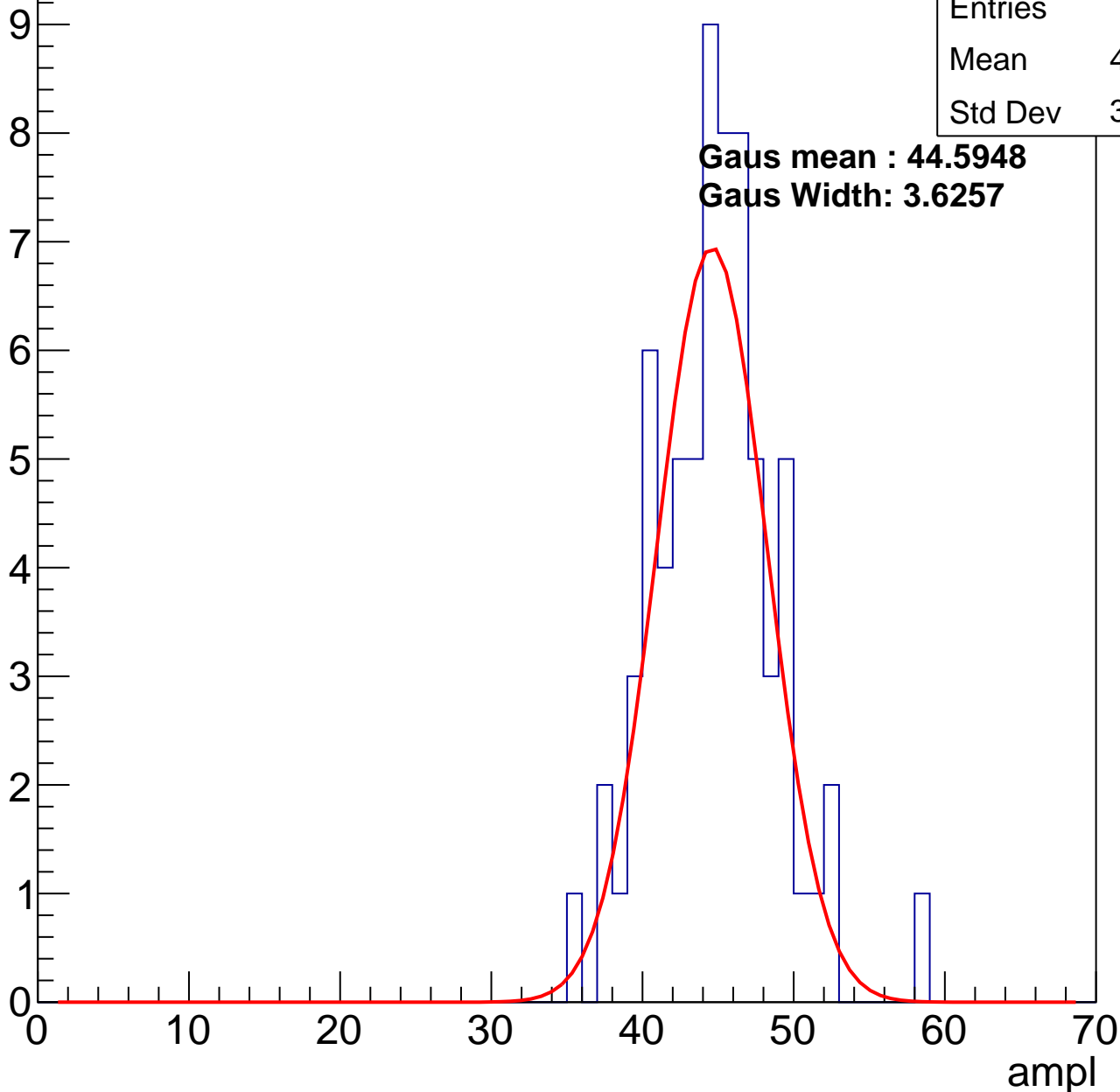
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	70
Mean	44.34
Std Dev	3.975

**Gaus mean : 44.5948**

**Gaus Width: 3.6257**

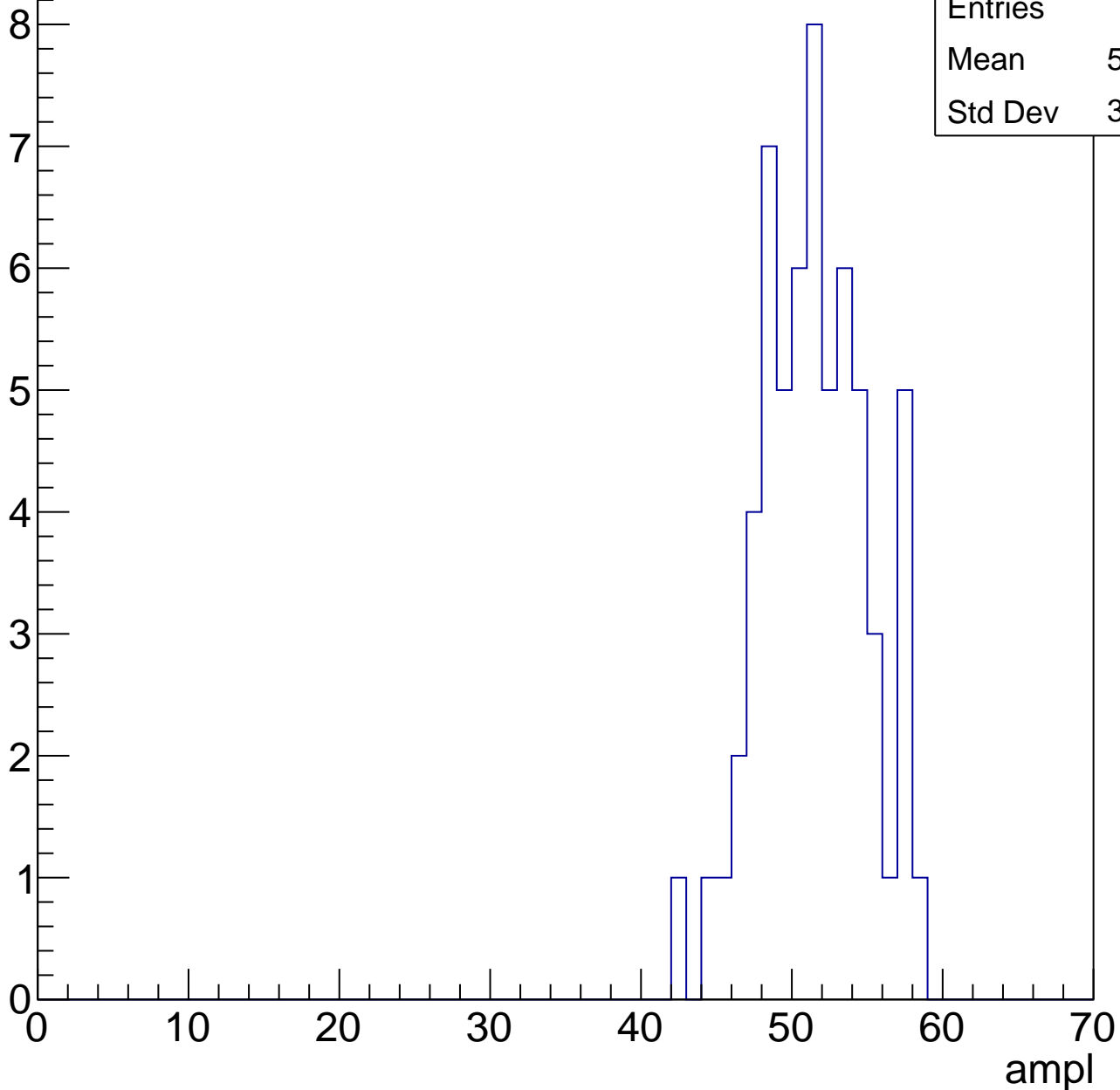


# B1L103S, U9-ch109, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	61
Mean	51.02
Std Dev	3.495

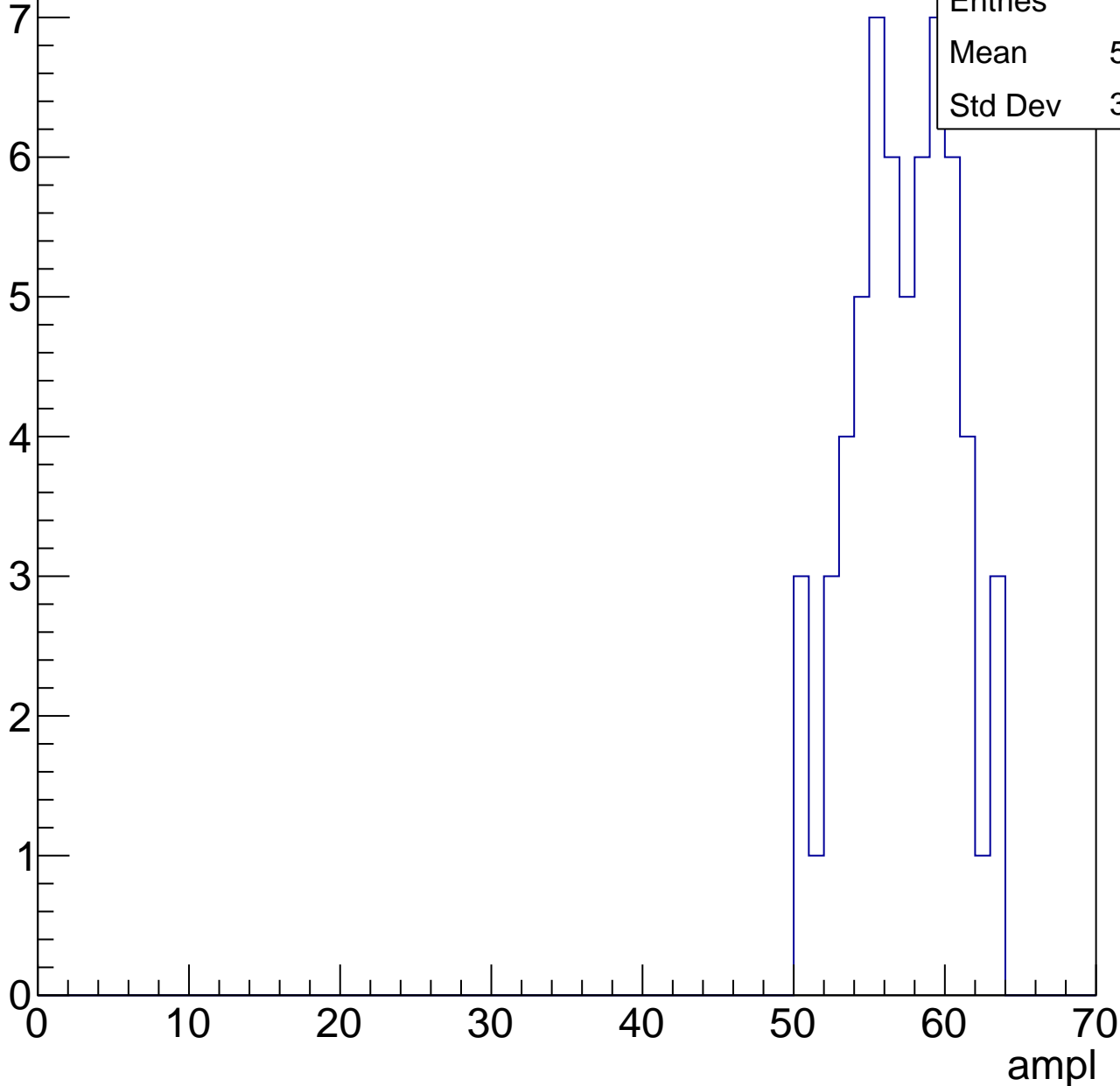


# B1L103S, U9-ch109, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	61
Mean	56.74
Std Dev	3.343

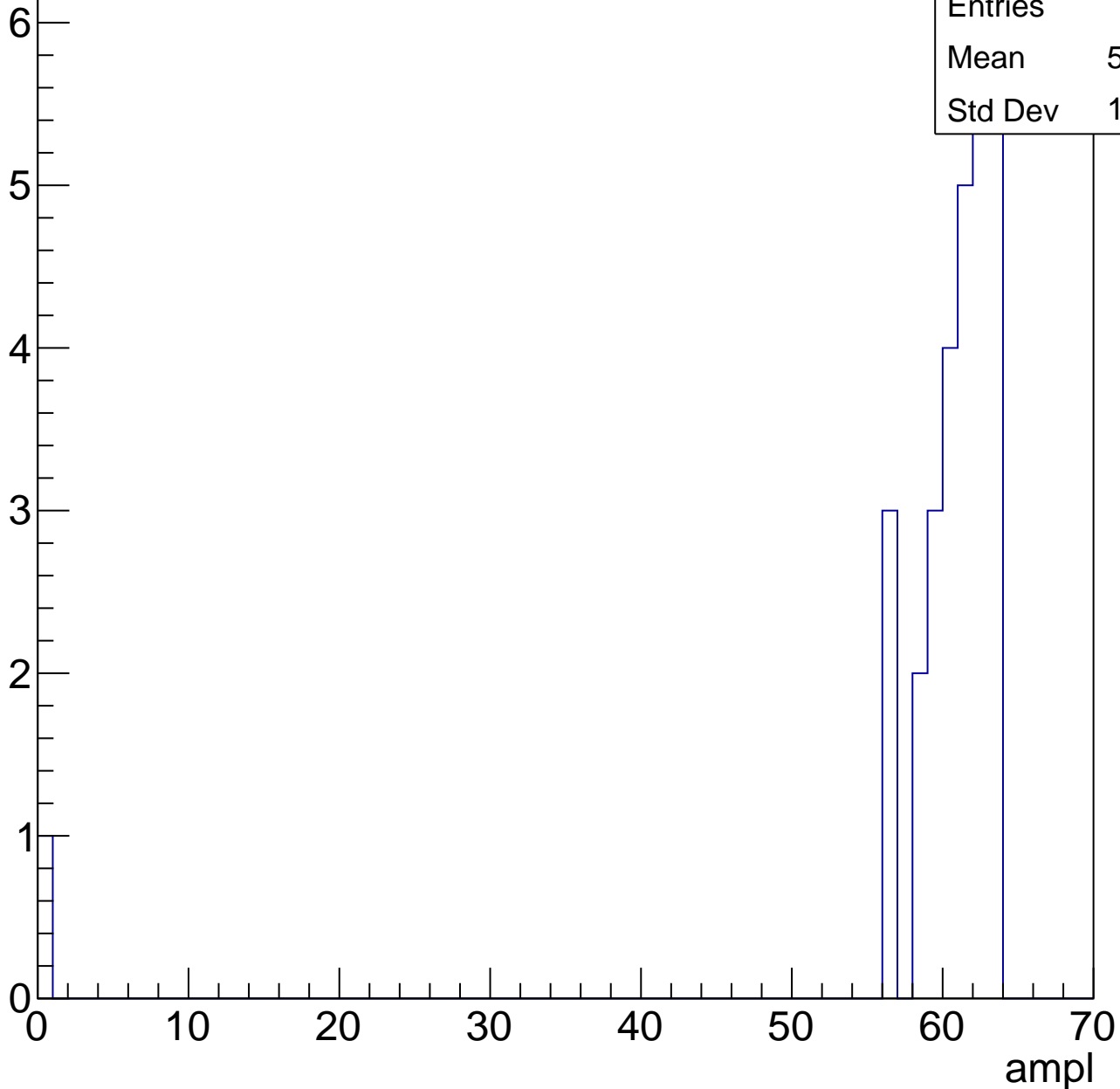


# B1L103S, U9-ch109, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	30
Mean	58.53
Std Dev	11.07



# B1L103S, U9-ch109, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U9-ch109, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U9-ch110, adc0

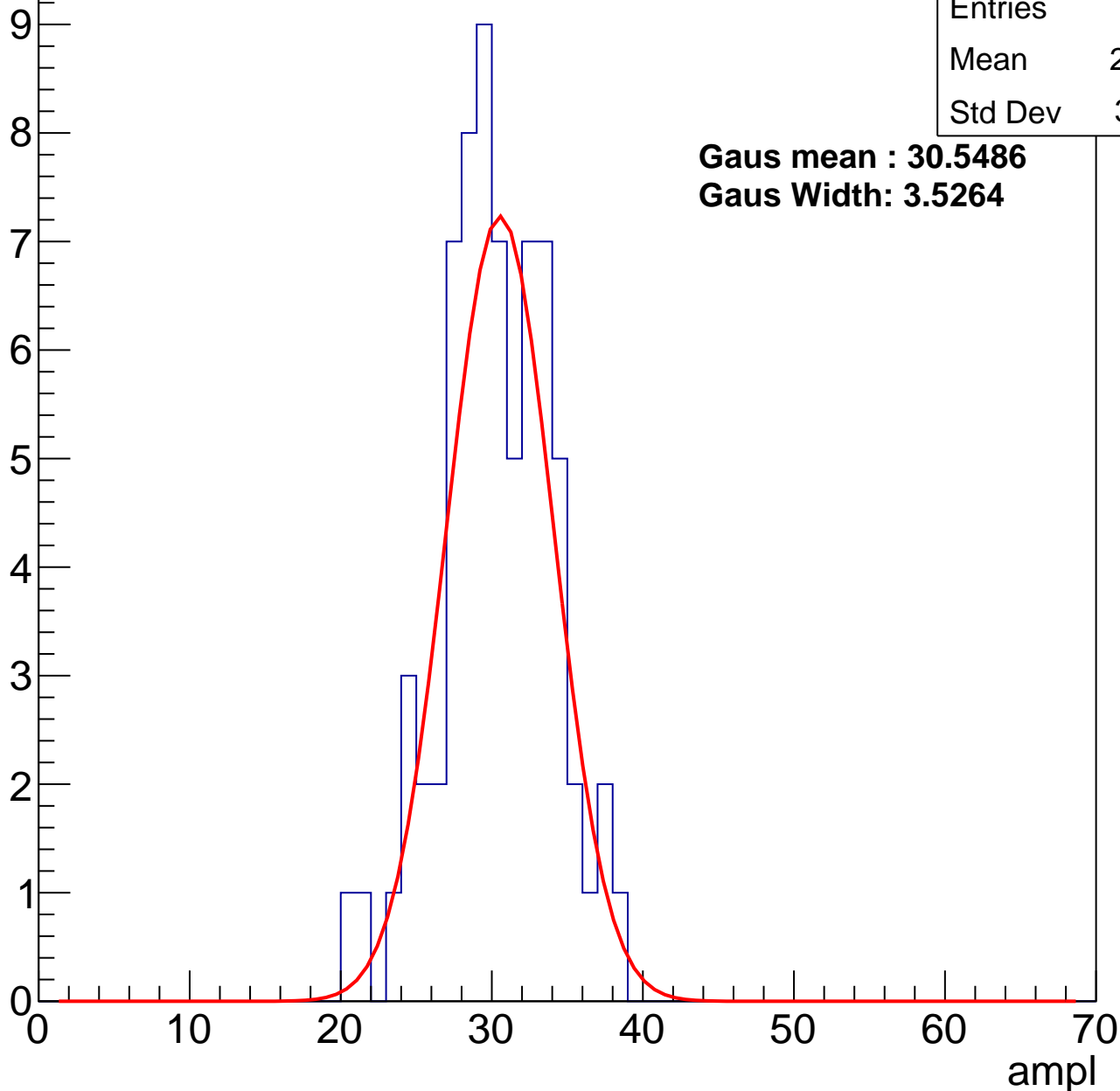
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	71
Mean	29.86
Std Dev	3.651

**Gaus mean : 30.5486**

**Gaus Width: 3.5264**



# B1L103S, U9-ch110, adc1

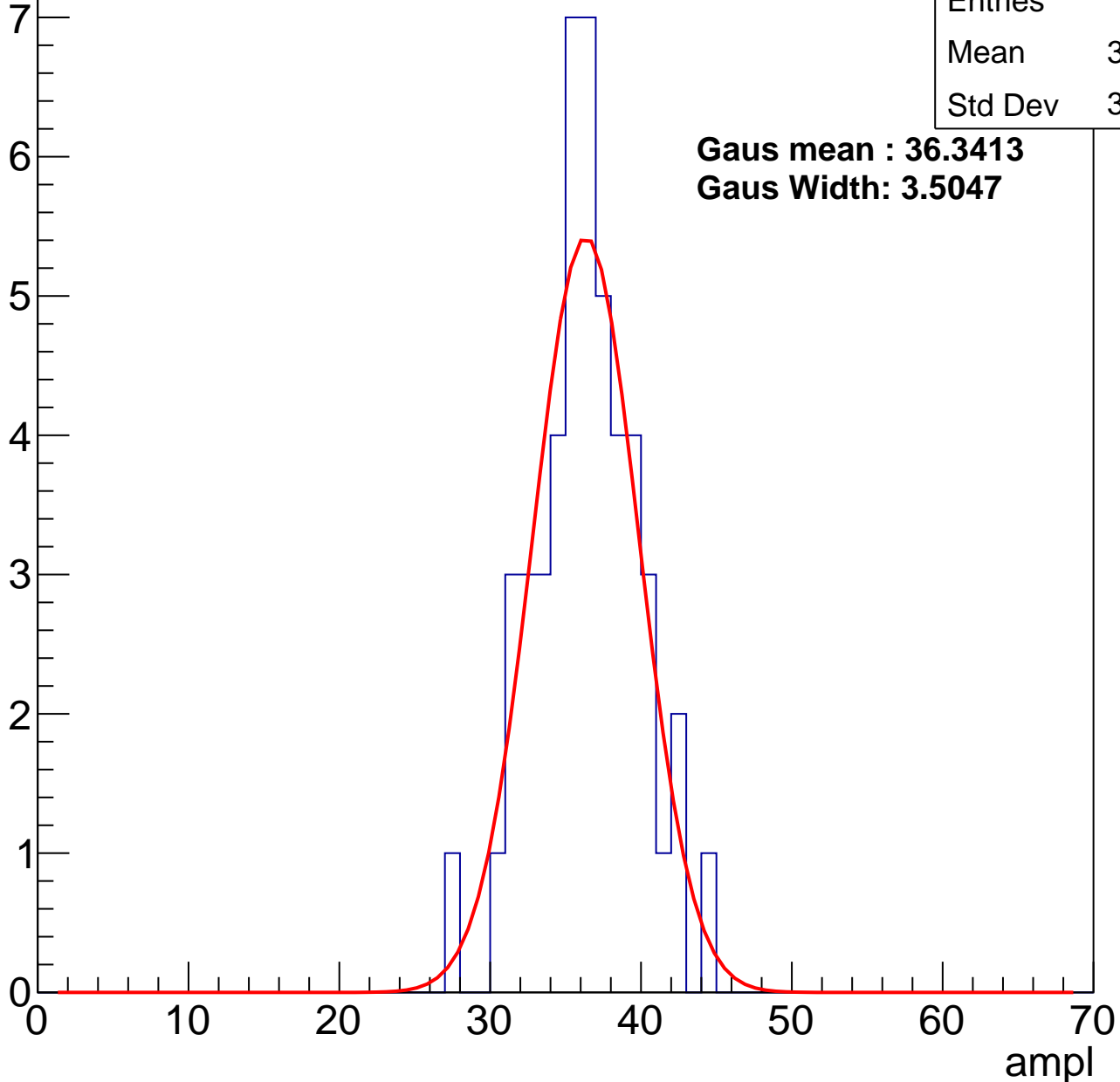
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	49
Mean	35.92
Std Dev	3.368

**Gaus mean : 36.3413**

**Gaus Width: 3.5047**



# B1L103S, U9-ch110, adc2

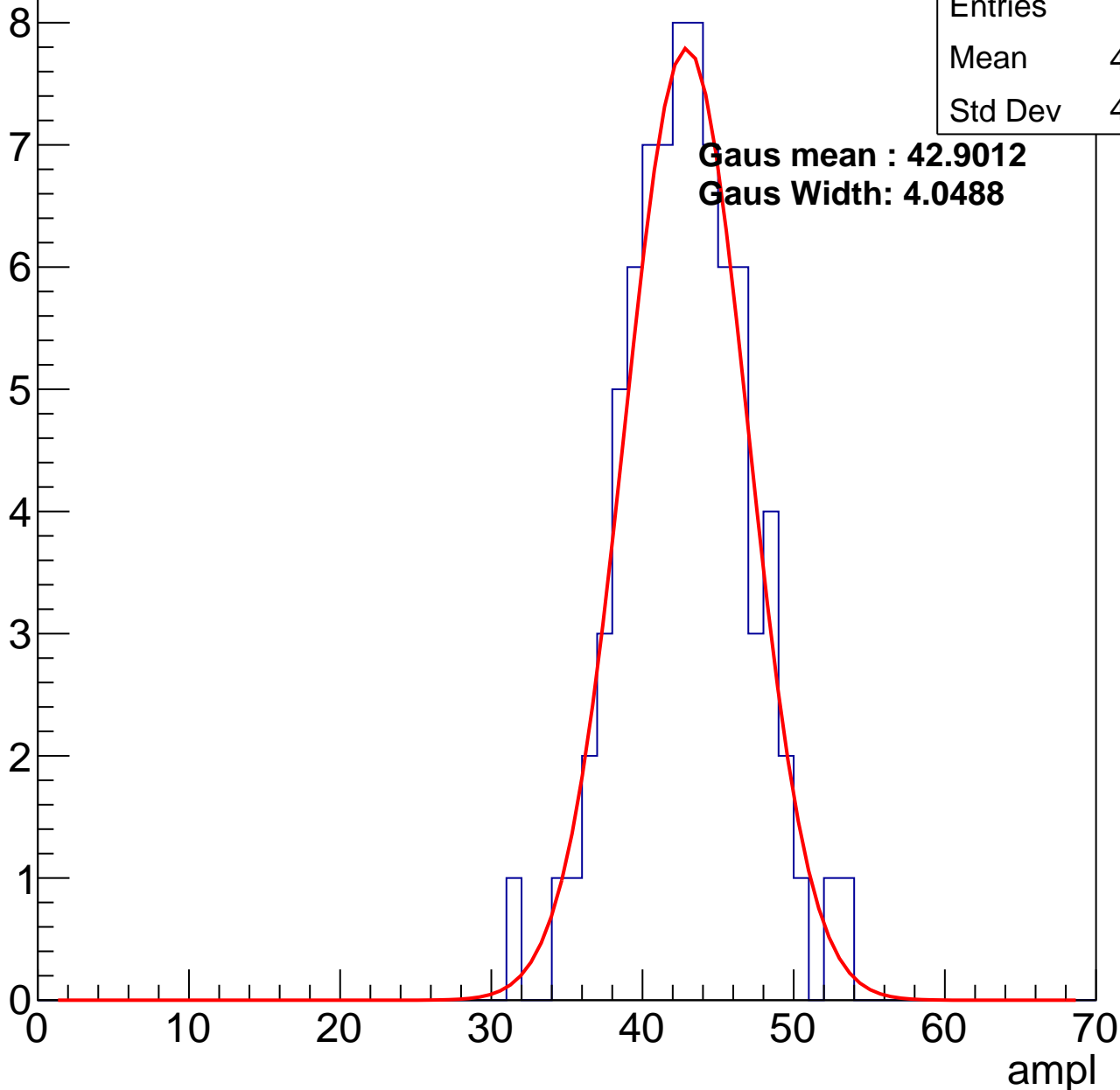
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	80
Mean	42.42
Std Dev	4.067

**Gaus mean : 42.9012**

**Gaus Width: 4.0488**

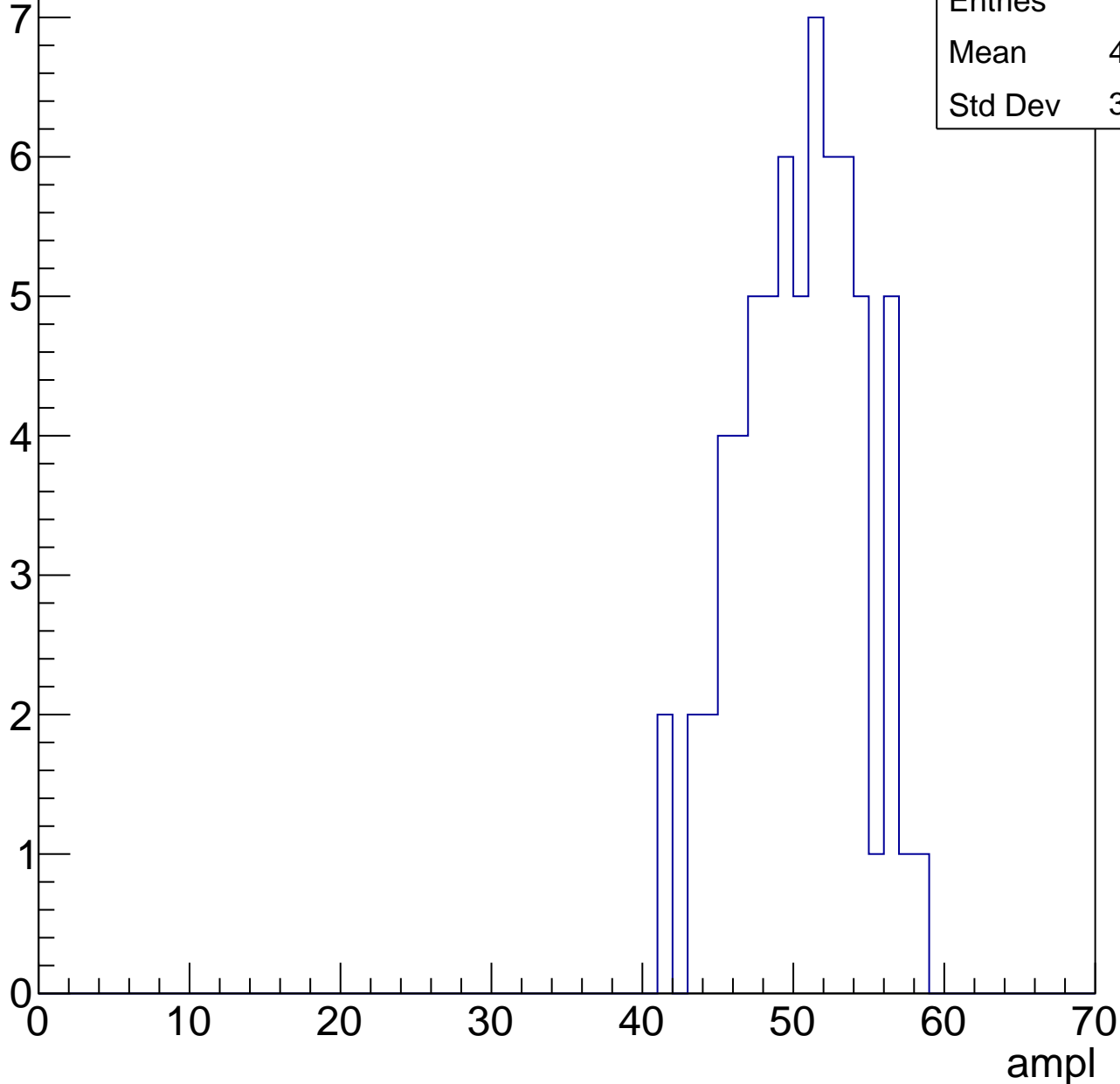


# B1L103S, U9-ch110, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	49.94
Std Dev	3.958

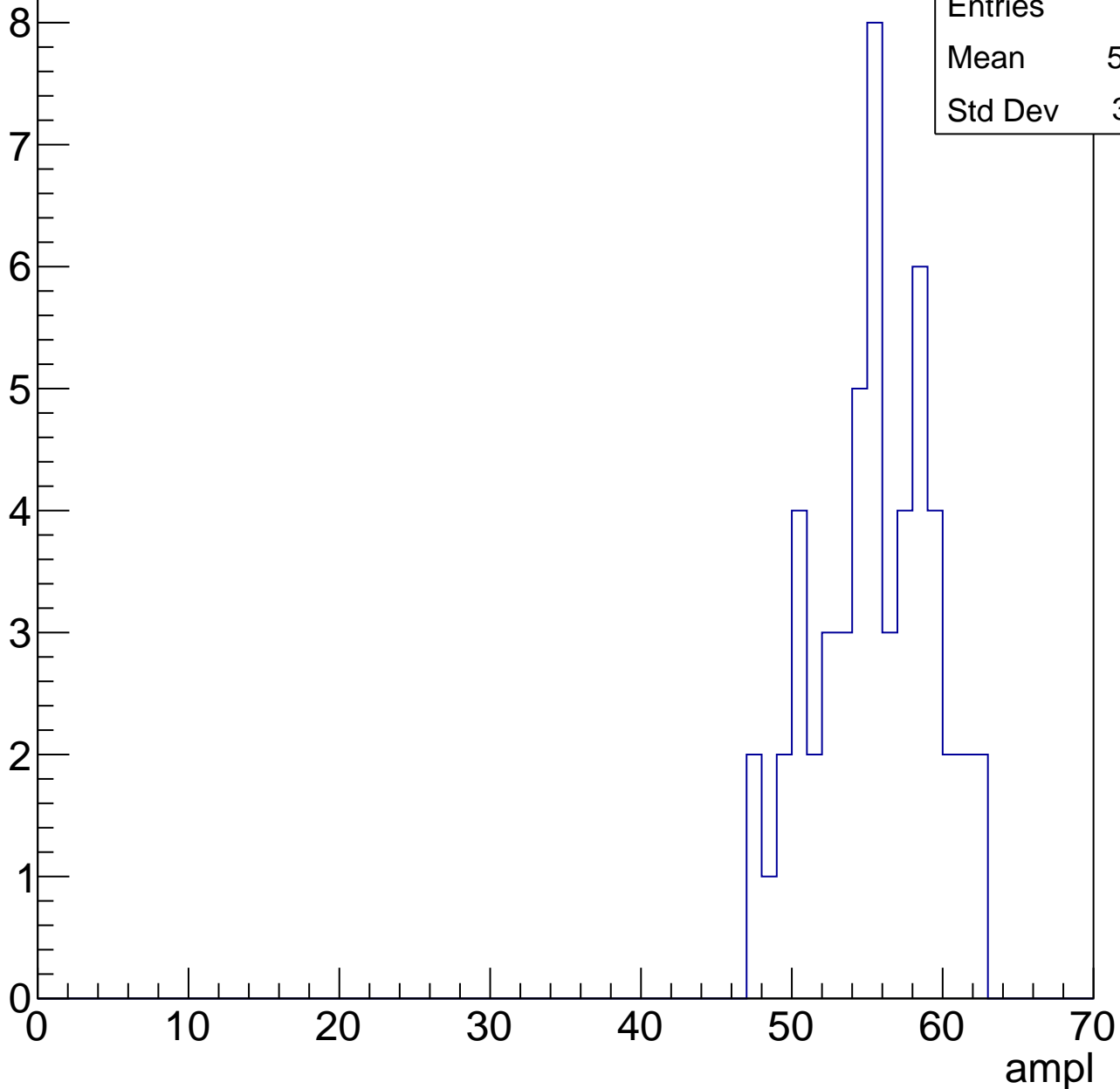


# B1L103S, U9-ch110, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	53
Mean	54.96
Std Dev	3.841

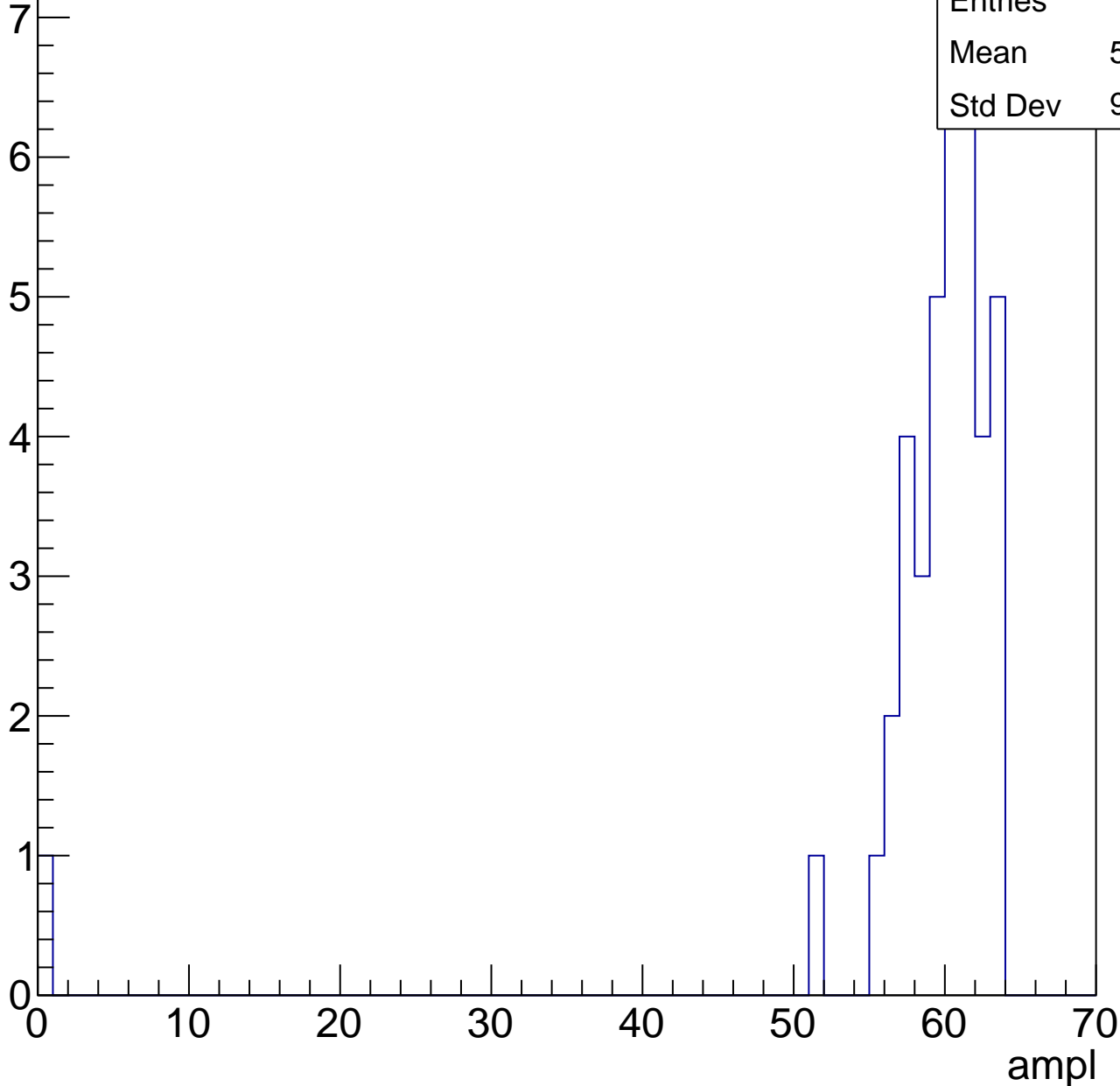


# B1L103S, U9-ch110, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	40
Mean	58.12
Std Dev	9.642

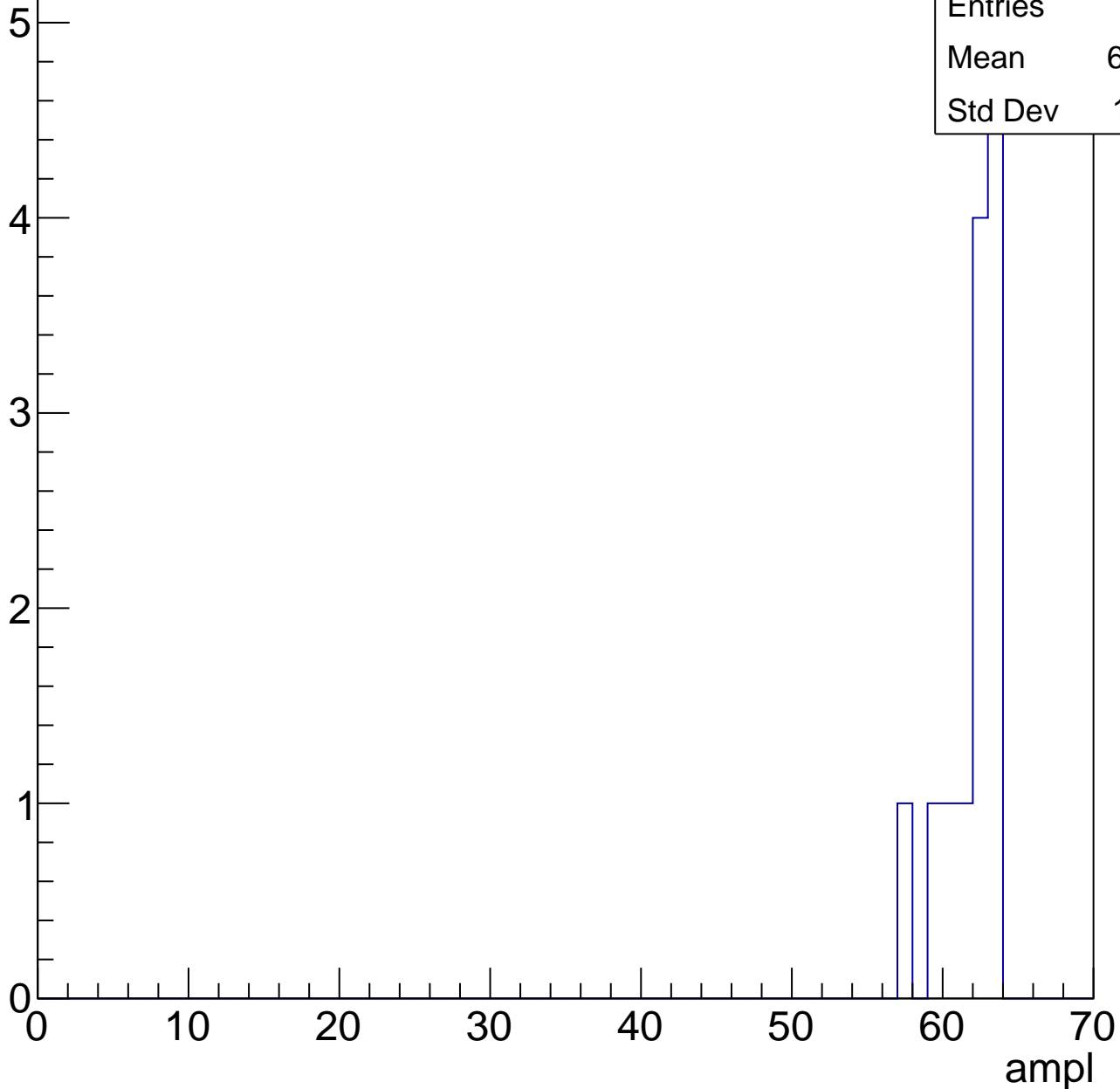


# B1L103S, U9-ch110, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	13
Mean	61.54
Std Dev	1.781





# B1L103S, U9-ch110, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	3
Mean	0
Std Dev	0

# B1L103S, U9-ch111, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	84
Mean	29.5
Std Dev	6.785

**Gaus mean : 30.8765**

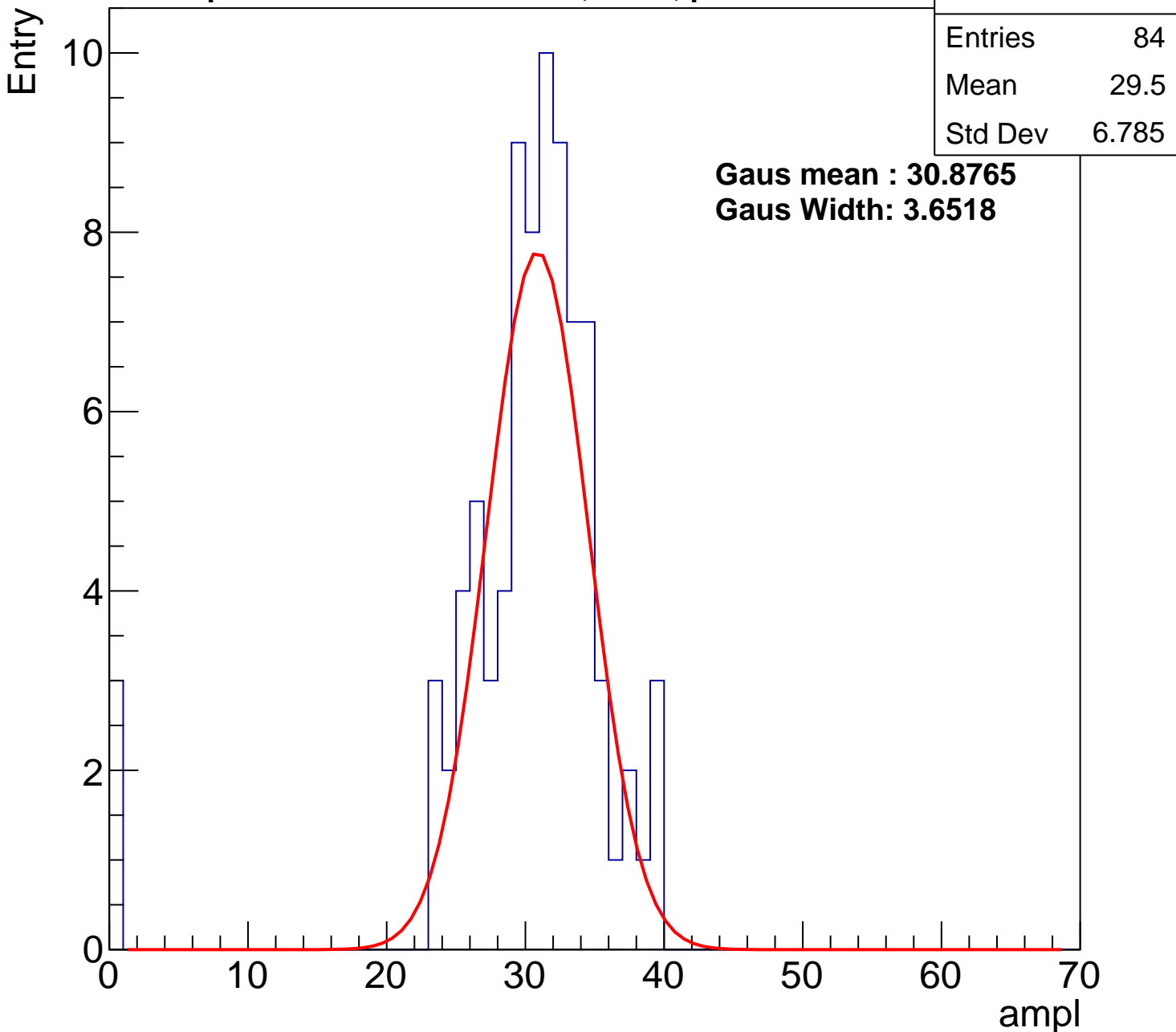
**Gaus Width: 3.6518**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U9-ch111, adc1

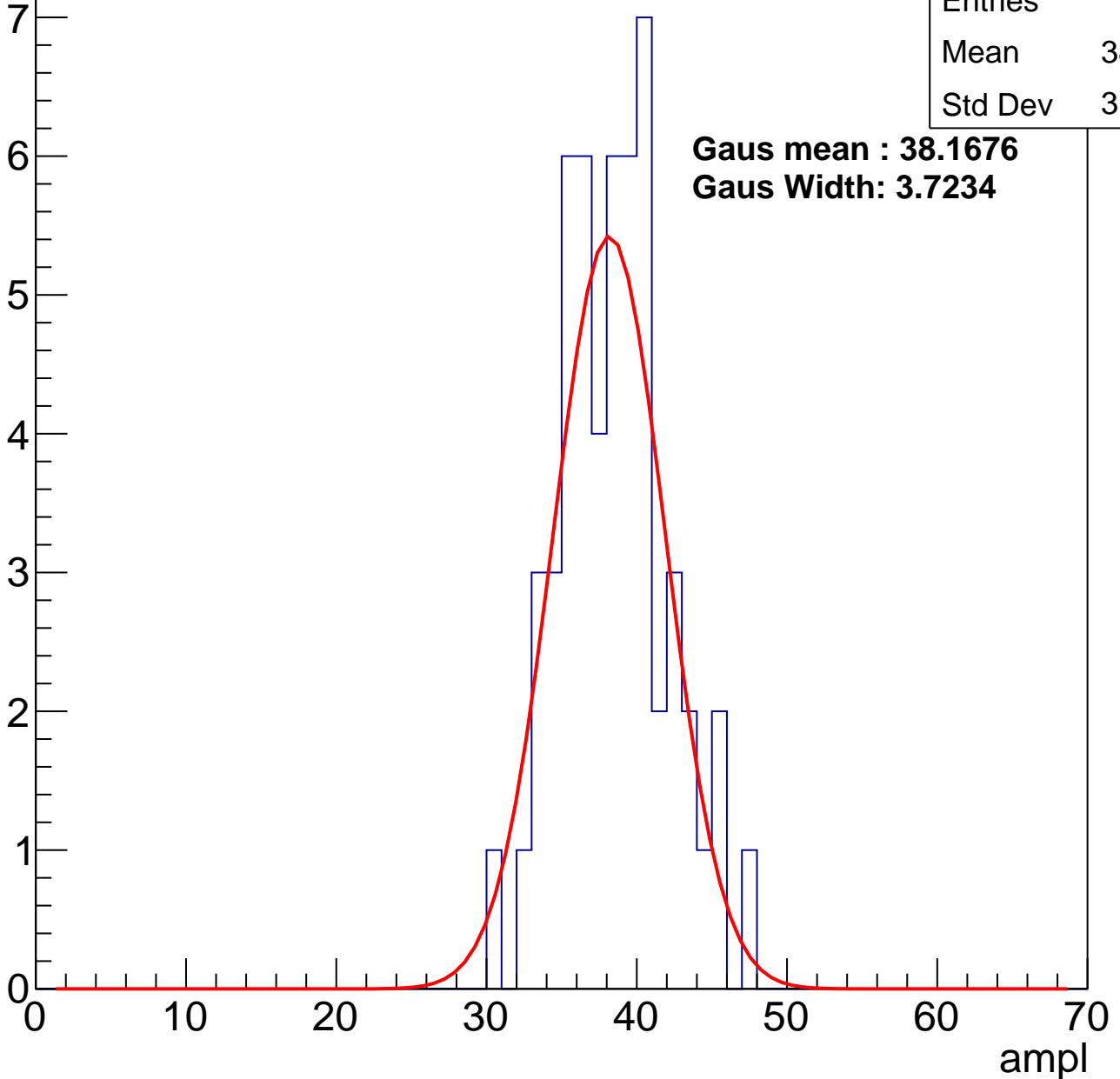
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	54
Mean	38.04
Std Dev	3.522

**Gaus mean : 38.1676**

**Gaus Width: 3.7234**



# B1L103S, U9-ch111, adc2

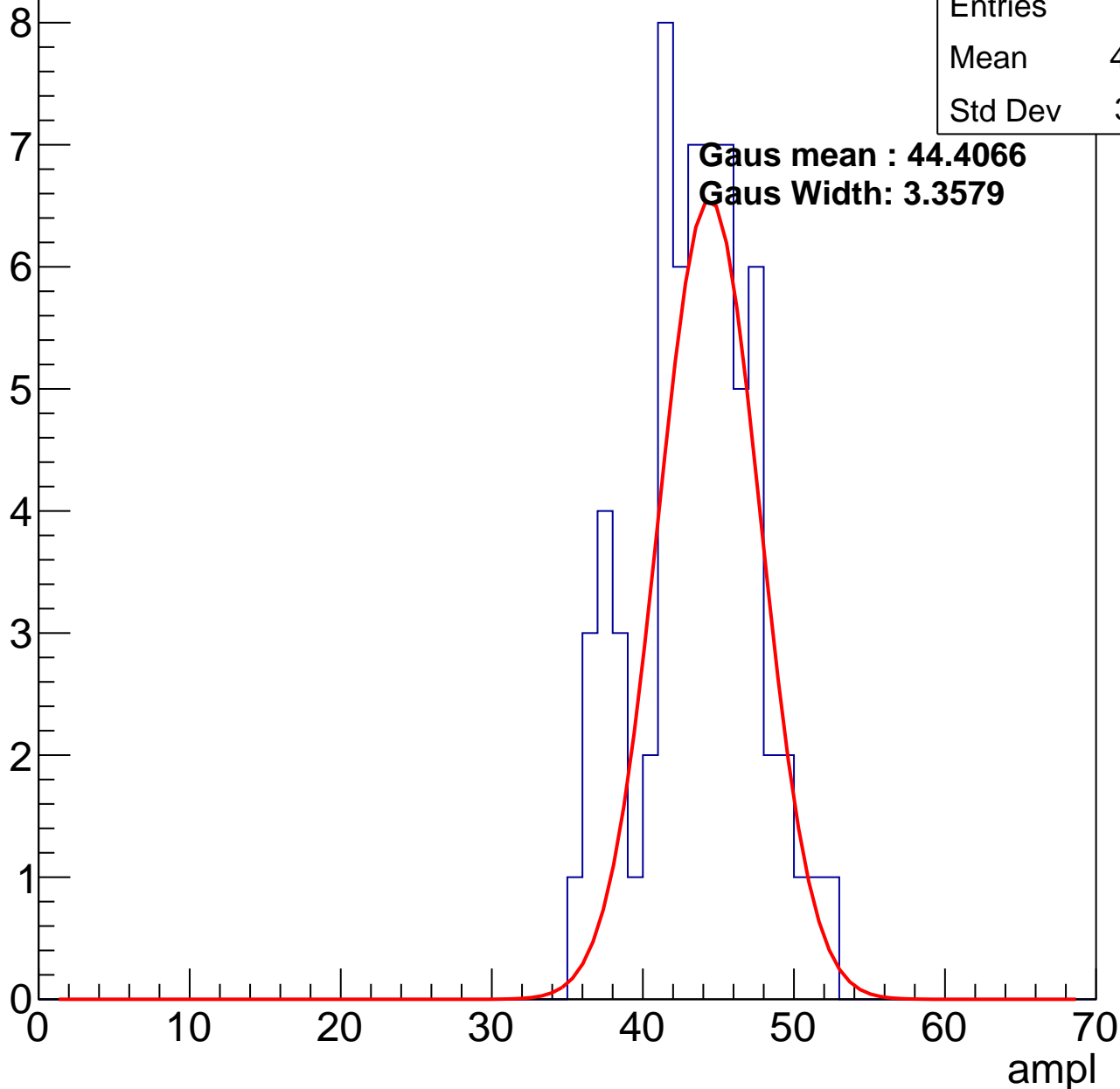
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	43.09
Std Dev	3.851

**Gaus mean : 44.4066**

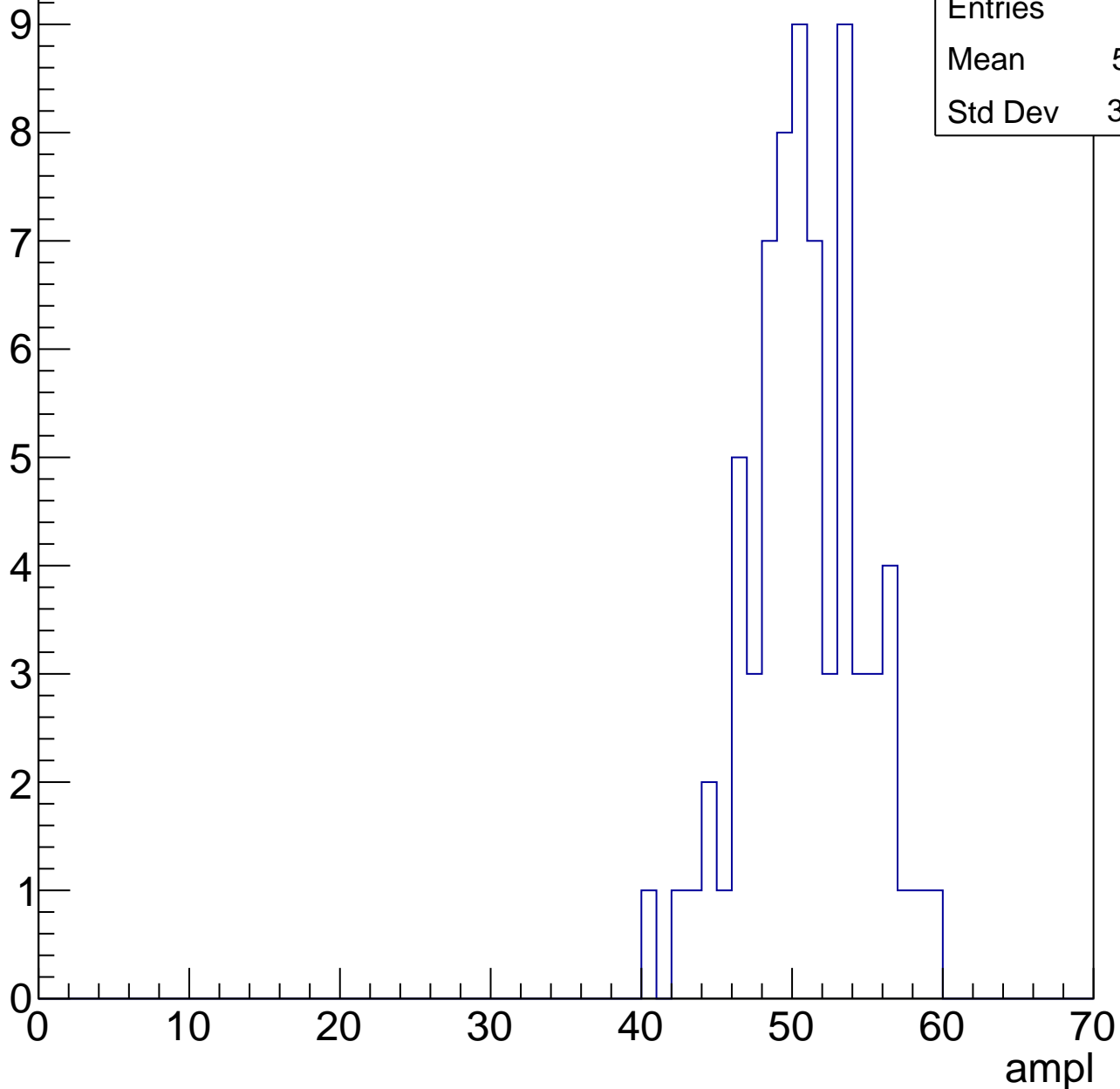
**Gaus Width: 3.3579**



# B1L103S, U9-ch111, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



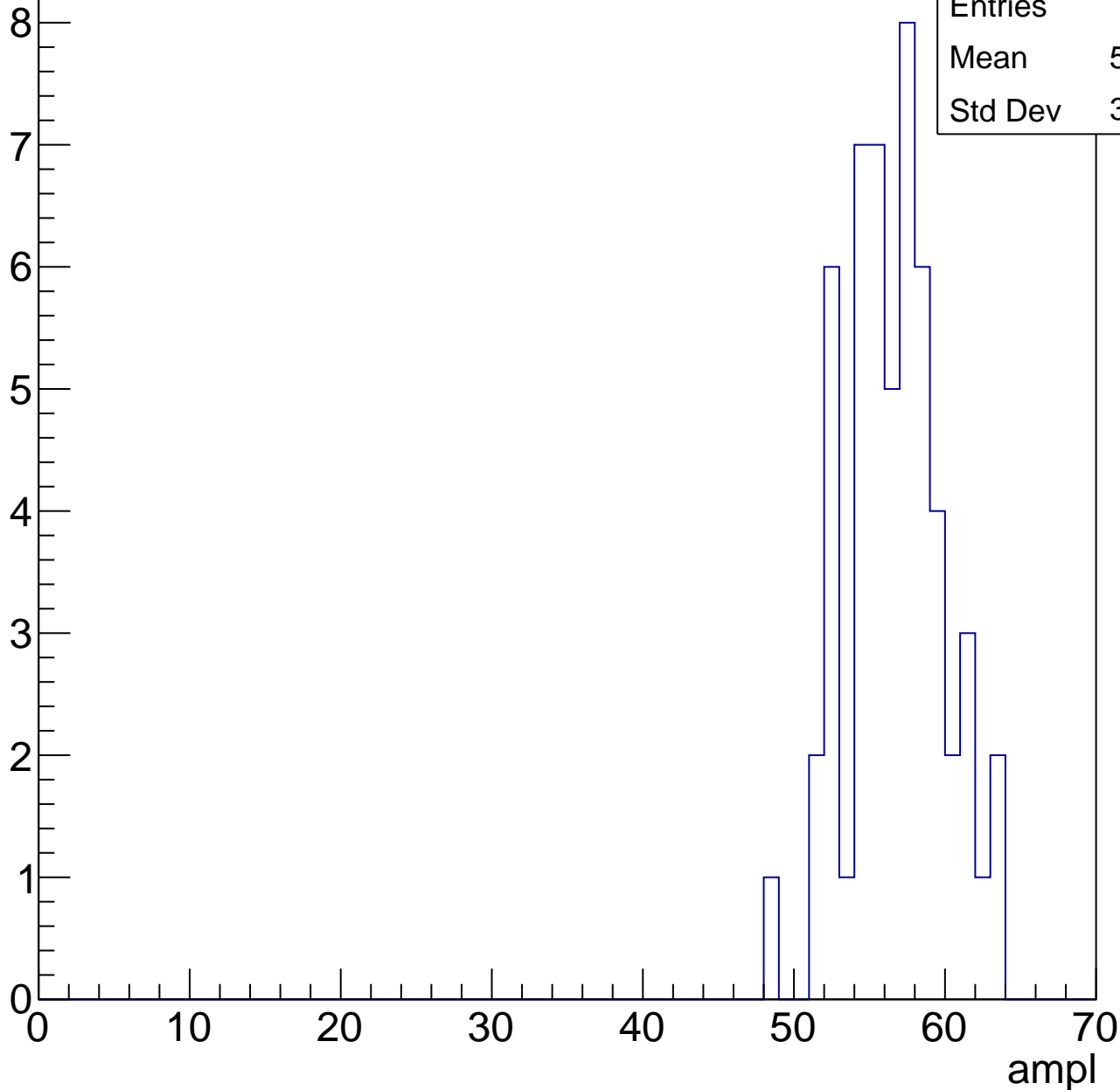
Entries	70
Mean	50.31
Std Dev	3.793

# B1L103S, U9-ch111, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

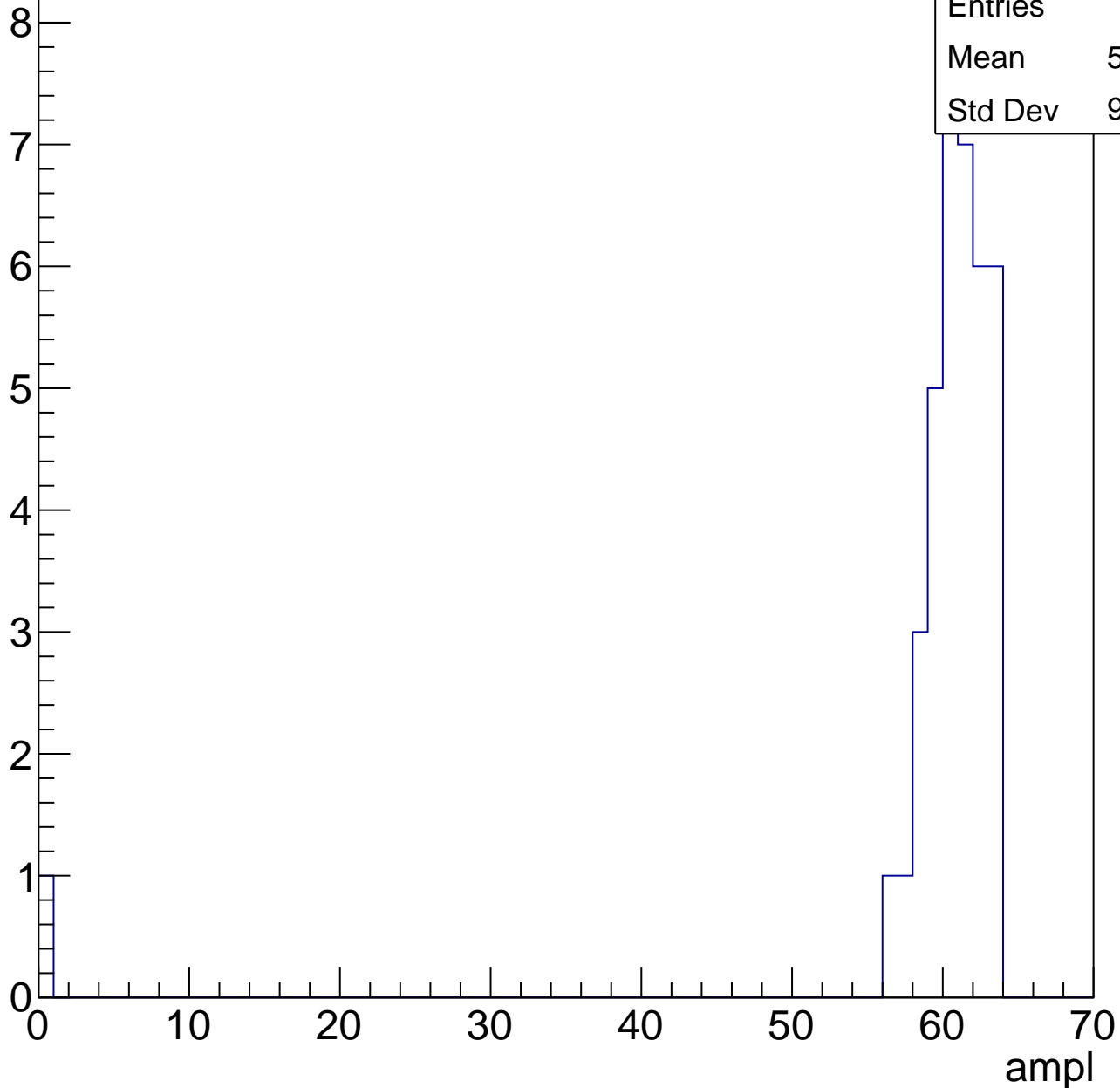
Entries	55
Mean	56.16
Std Dev	3.195



# B1L103S, U9-ch111, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U9-ch111, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U9-ch111, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U9-ch112, adc0

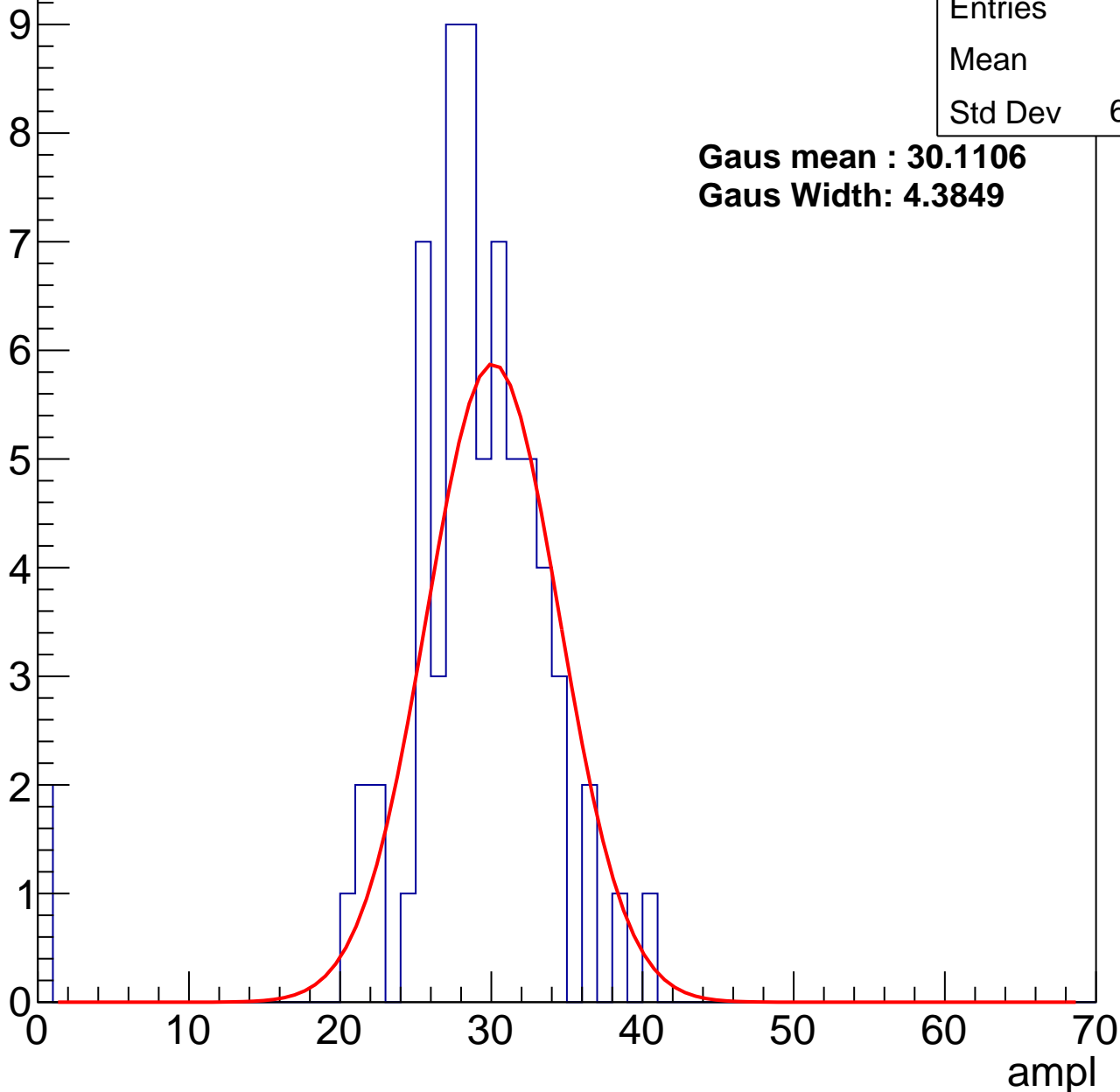
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	69
Mean	28
Std Dev	6.186

**Gaus mean : 30.1106**

**Gaus Width: 4.3849**



# B1L103S, U9-ch112, adc1

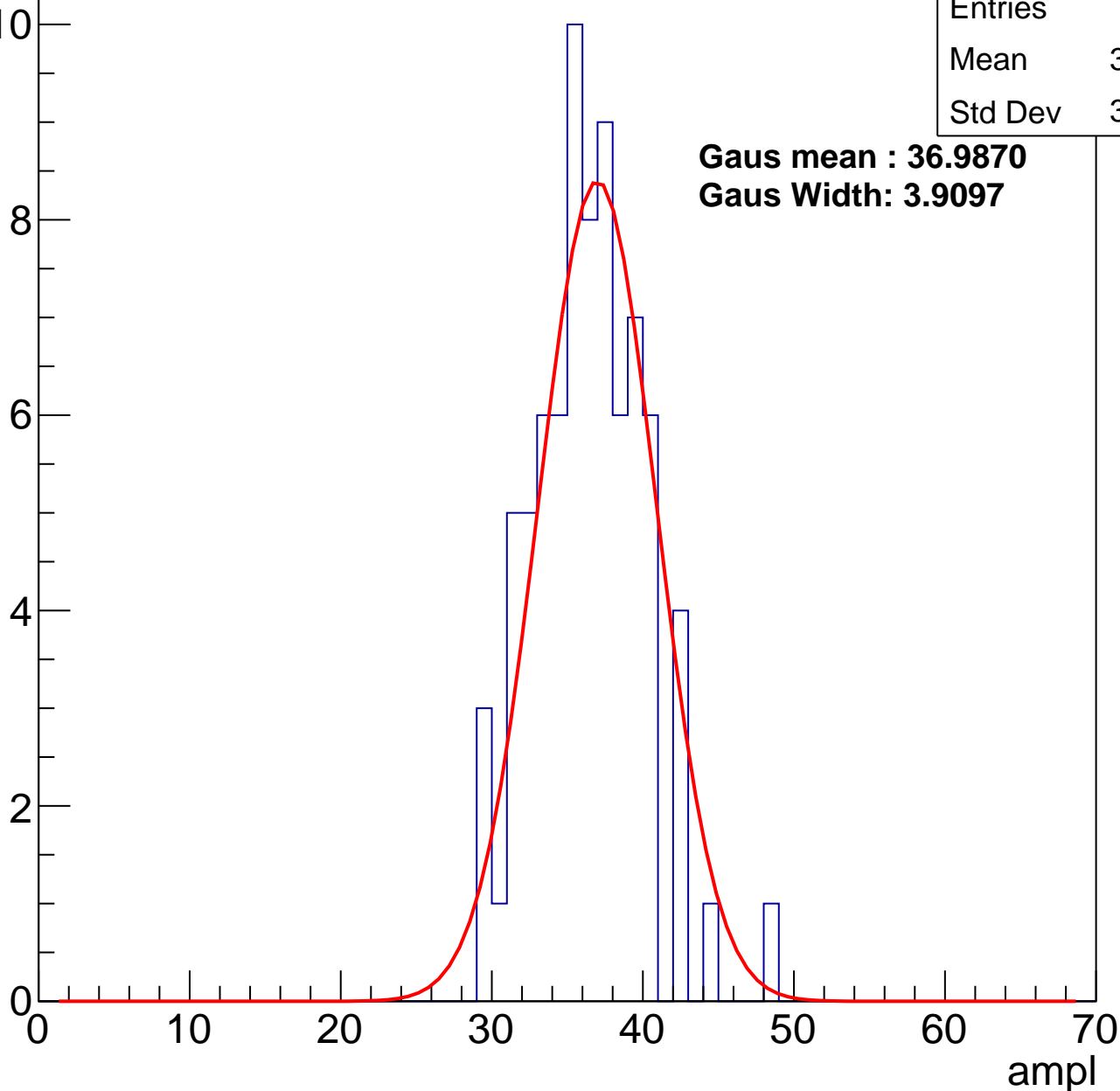
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	78
Mean	35.97
Std Dev	3.616

**Gaus mean : 36.9870**

**Gaus Width: 3.9097**



# B1L103S, U9-ch112, adc2

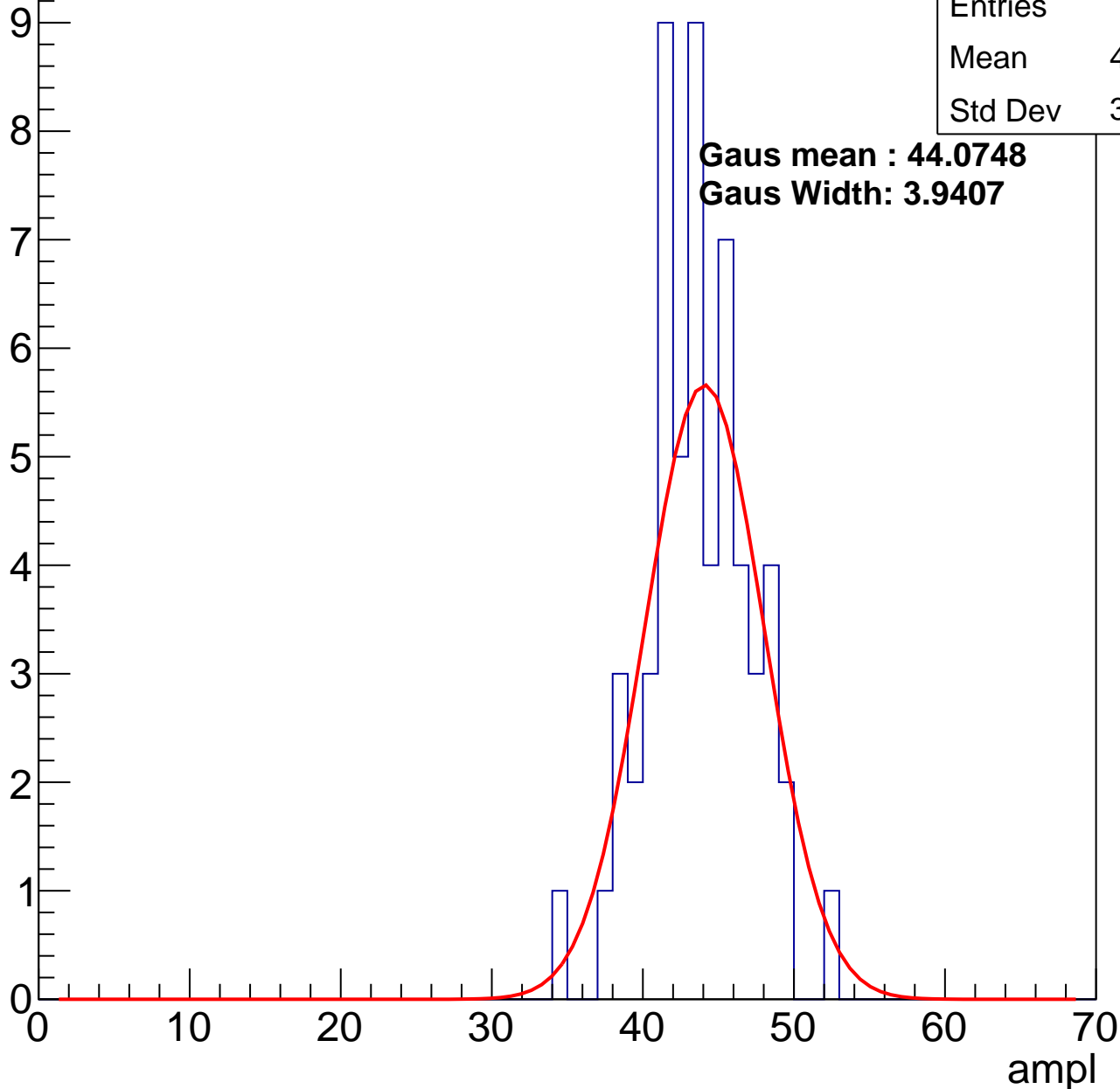
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	58
Mean	43.22
Std Dev	3.368

**Gaus mean : 44.0748**

**Gaus Width: 3.9407**

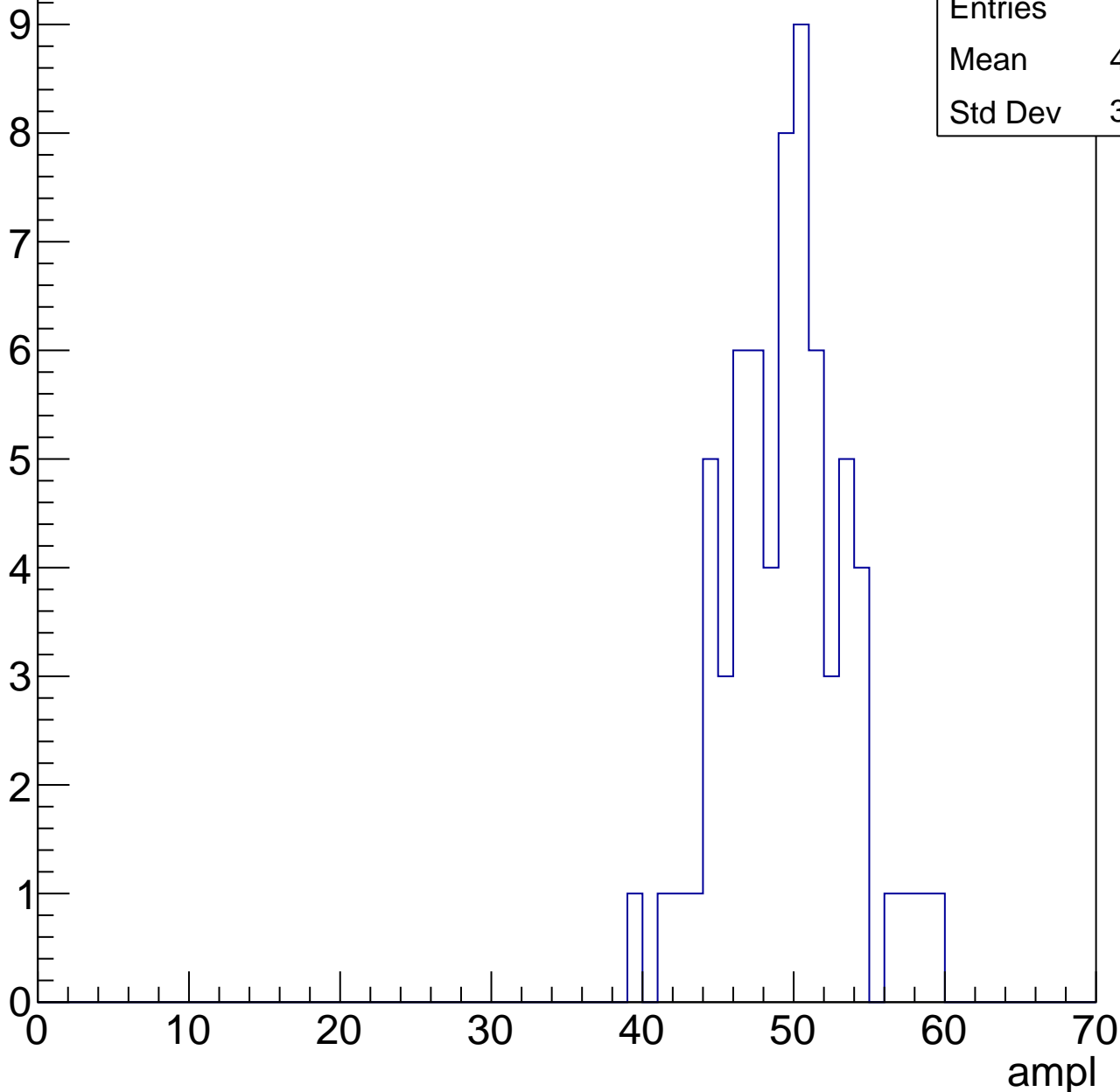


# B1L103S, U9-ch112, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	49.03
Std Dev	3.936

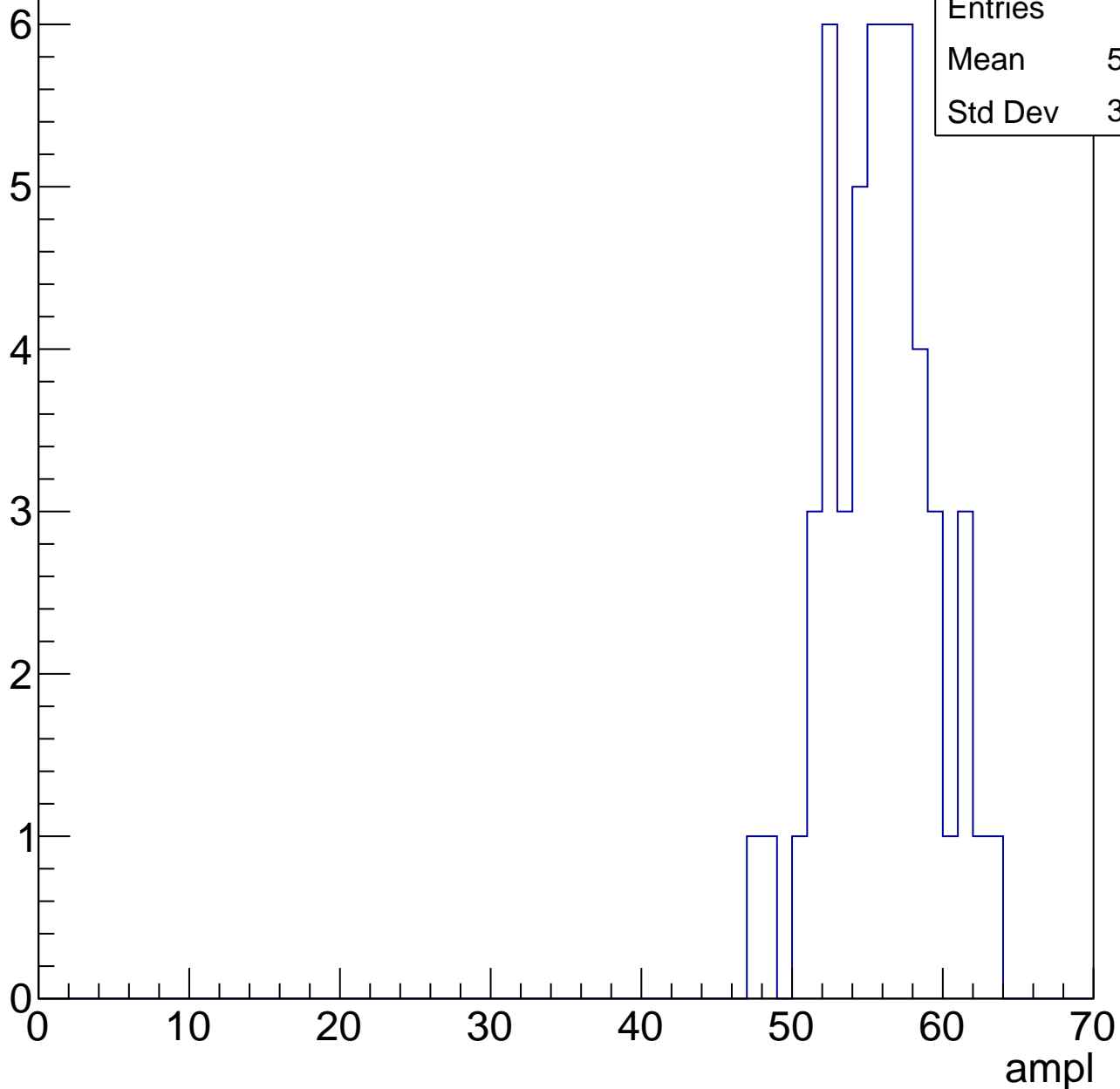


# B1L103S, U9-ch112, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	51
Mean	55.37
Std Dev	3.458

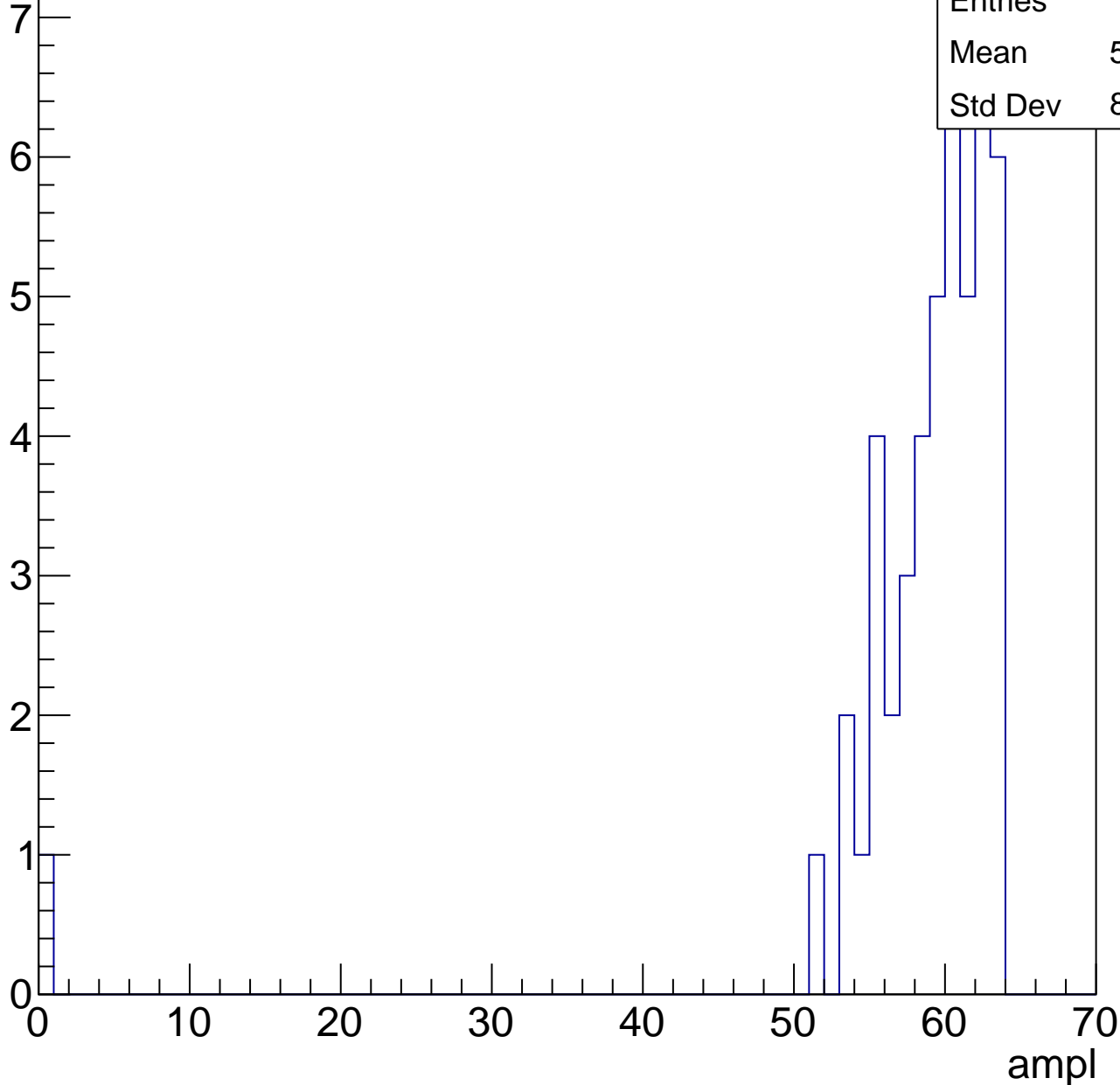


# B1L103S, U9-ch112, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

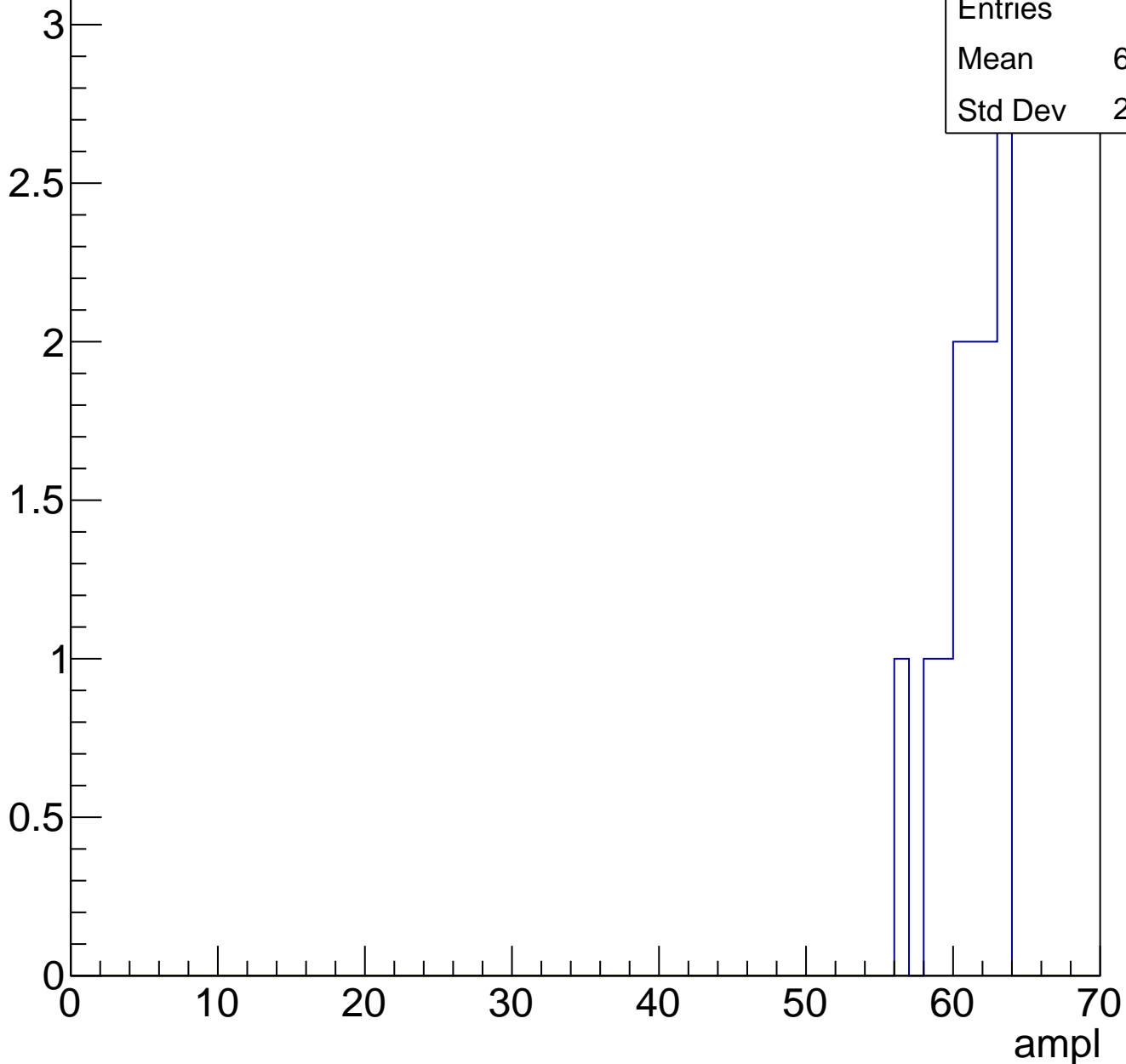
Entries	48
Mean	57.88
Std Dev	8.974



# B1L103S, U9-ch112, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U9-ch112, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U9-ch113, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	87
Mean	28.93
Std Dev	5.175

**Gaus mean : 29.6184**

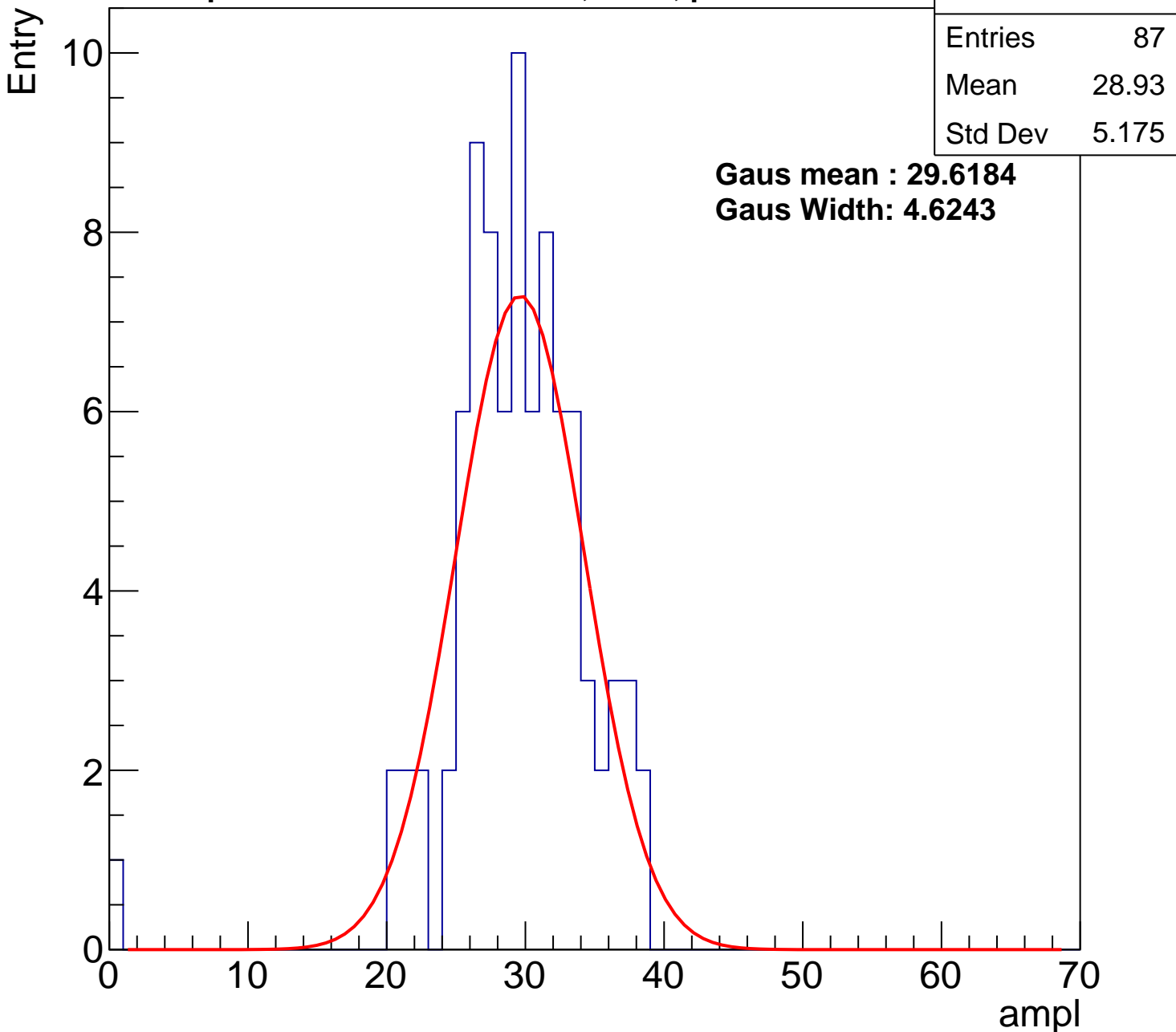
**Gaus Width: 4.6243**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U9-ch113, adc1

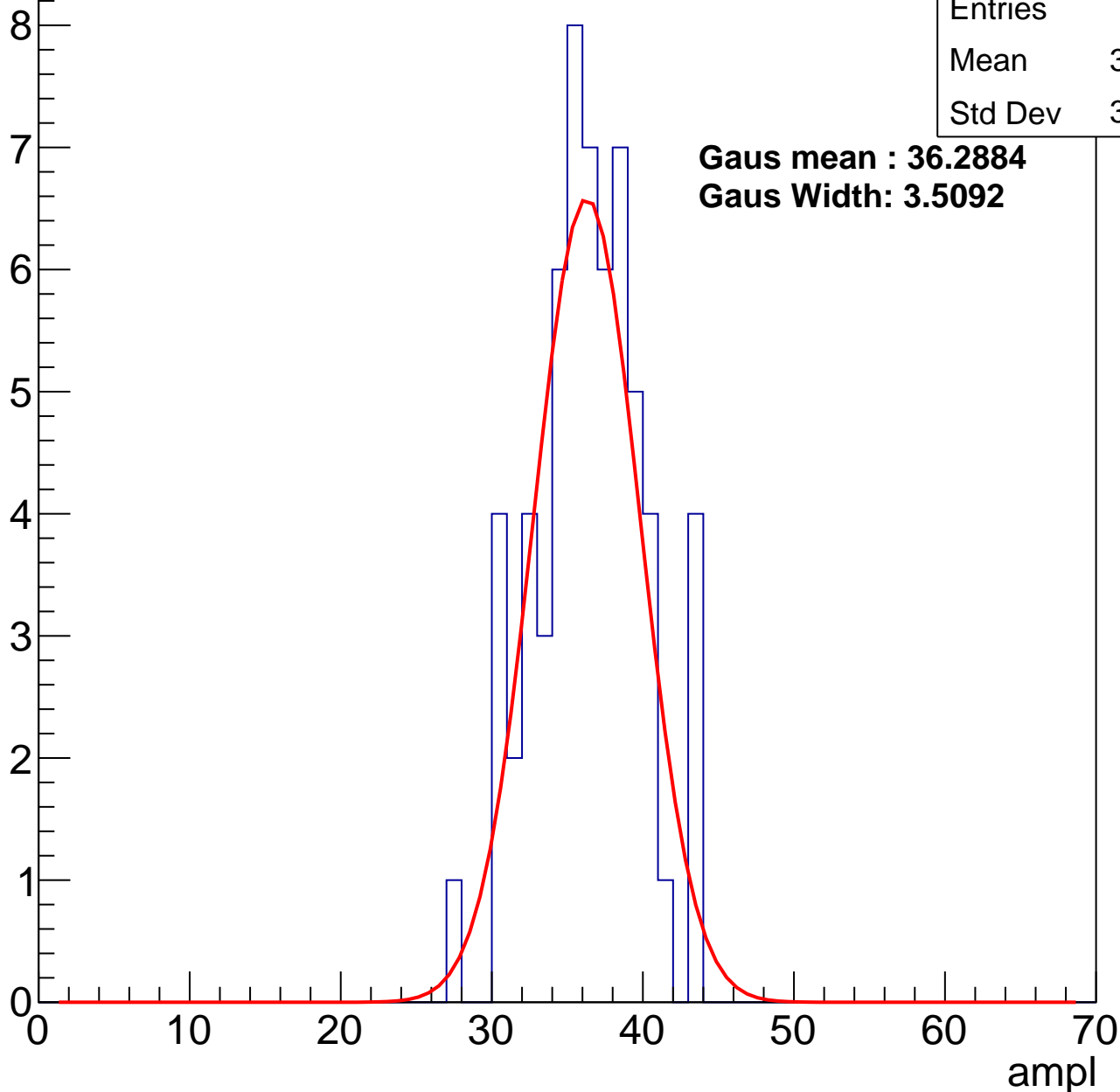
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	35.94
Std Dev	3.505

**Gaus mean : 36.2884**

**Gaus Width: 3.5092**



# B1L103S, U9-ch113, adc2

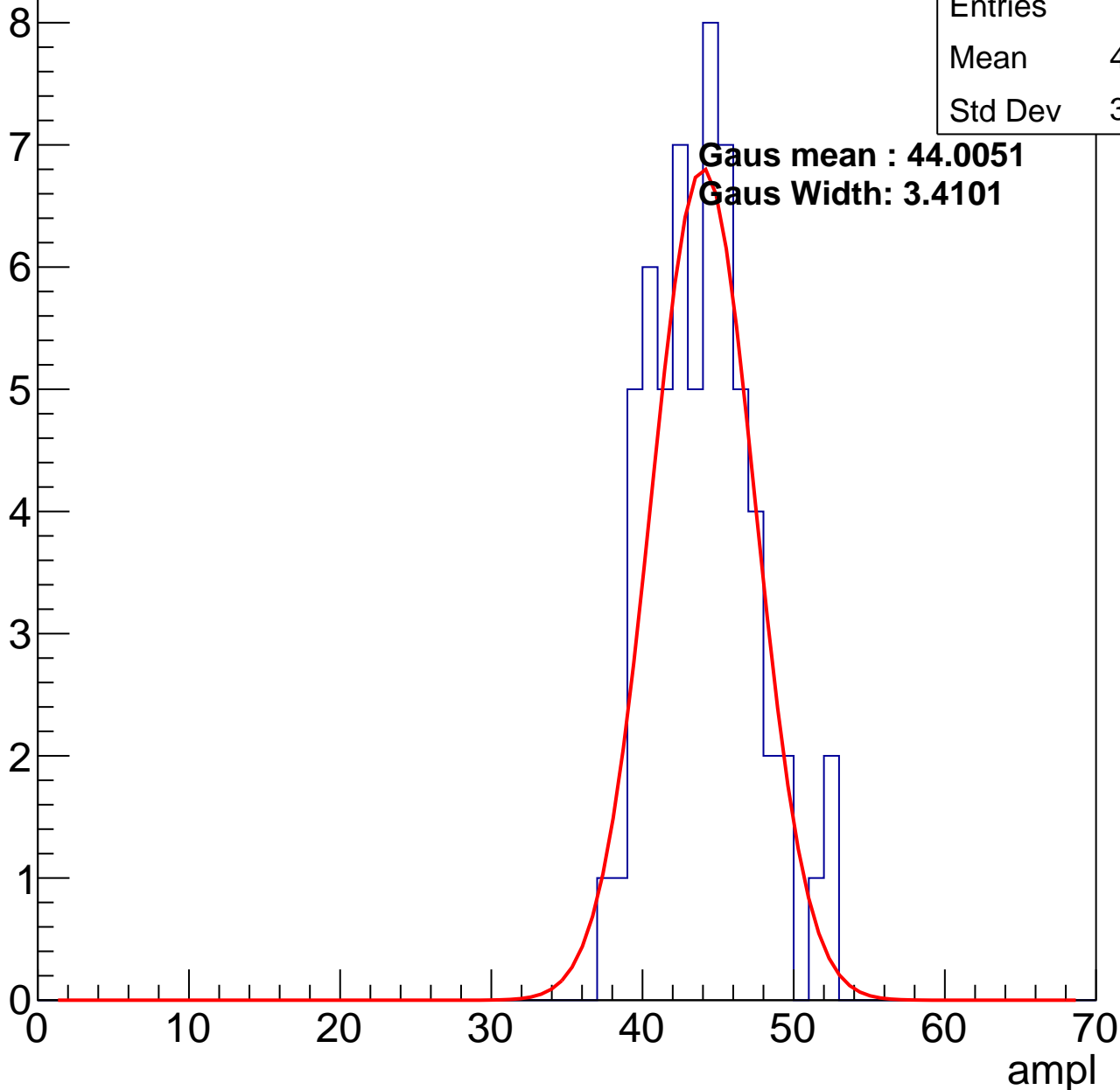
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	61
Mean	43.57
Std Dev	3.375

**Gaus mean : 44.0051**

**Gaus Width: 3.4101**

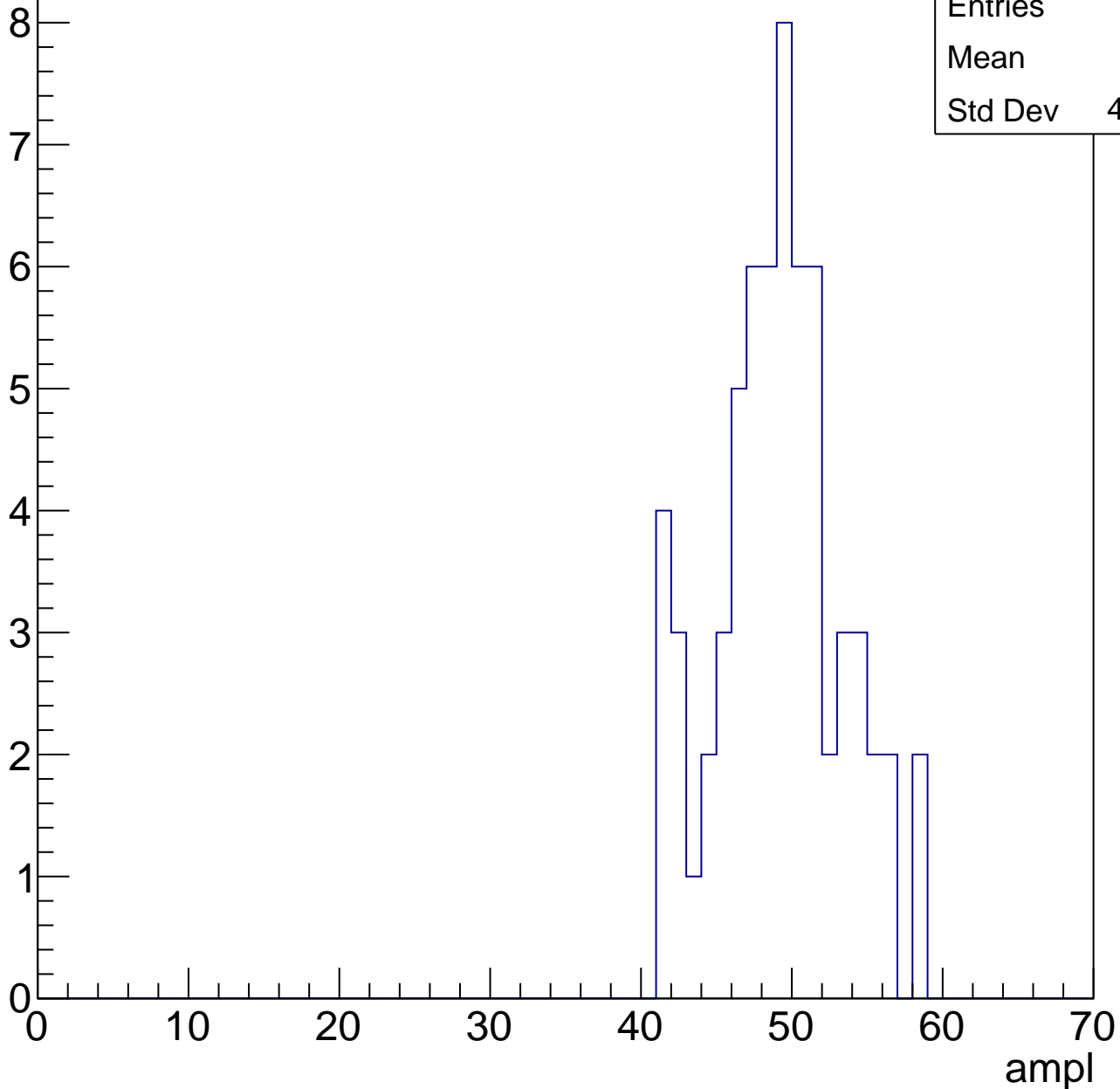


# B1L103S, U9-ch113, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	48.7
Std Dev	4.163

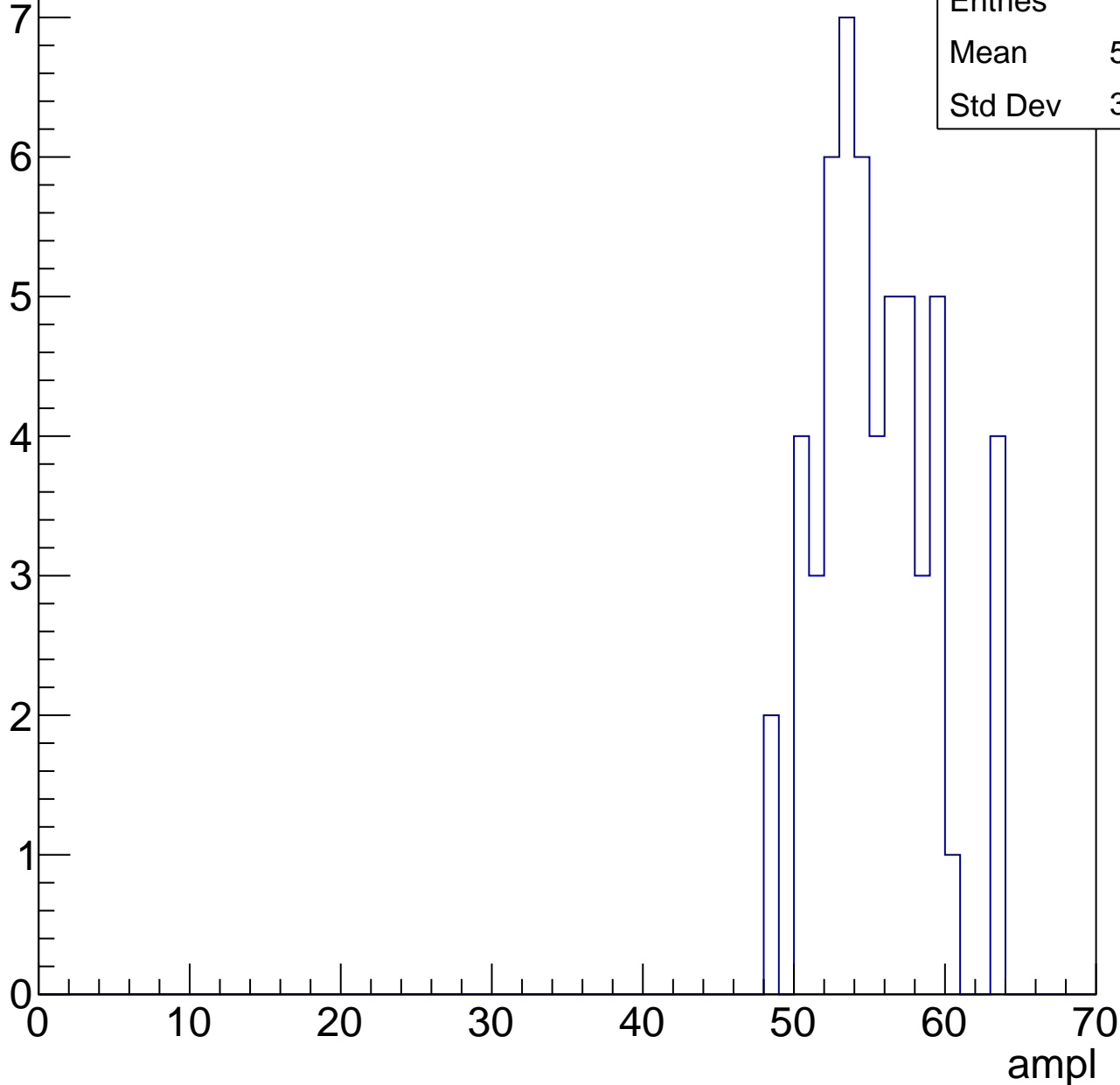


# B1L103S, U9-ch113, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

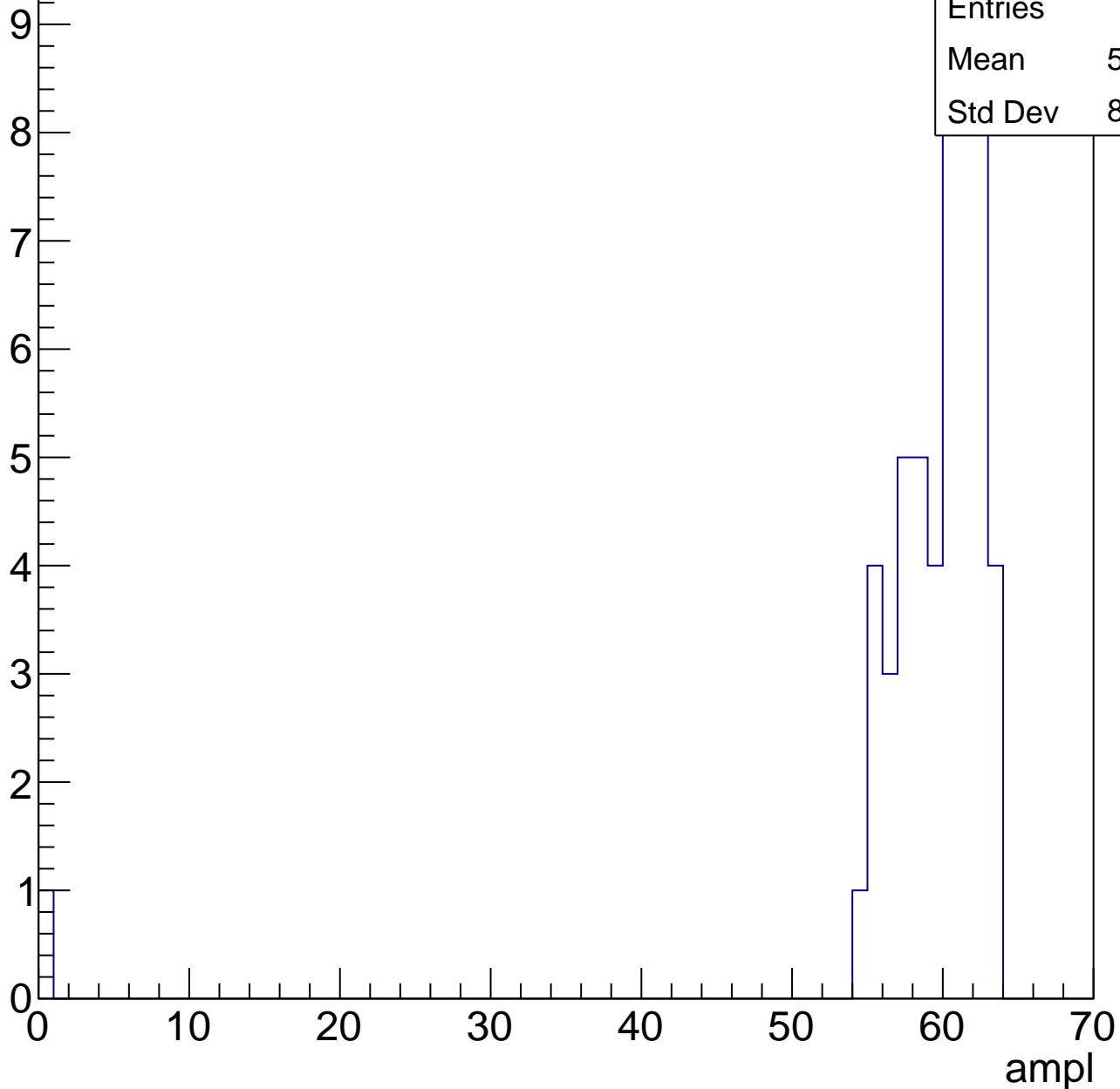
Entries	55
Mean	54.95
Std Dev	3.685



# B1L103S, U9-ch113, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

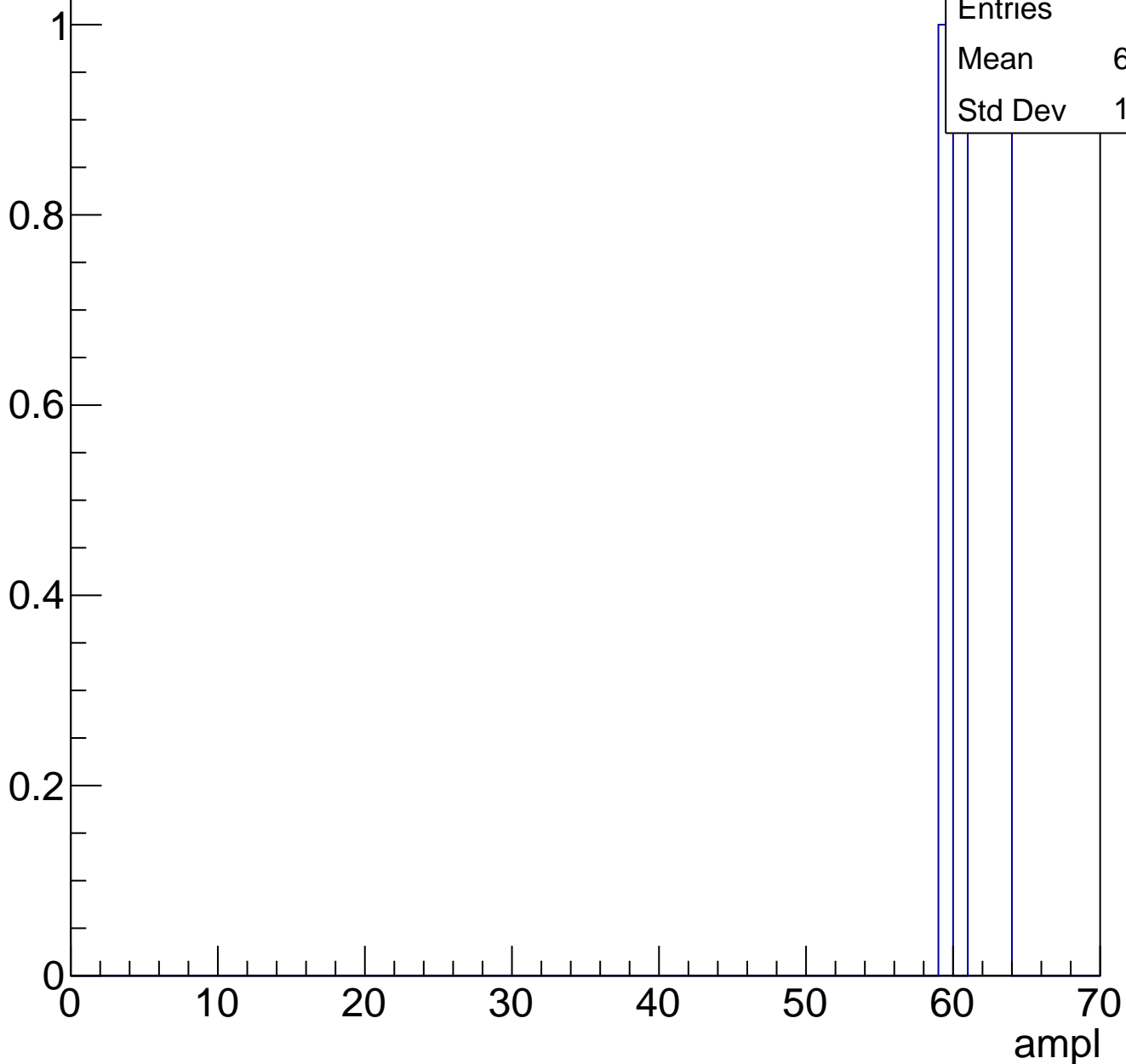
Entry



# B1L103S, U9-ch113, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U9-ch113, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U9-ch114, adc0

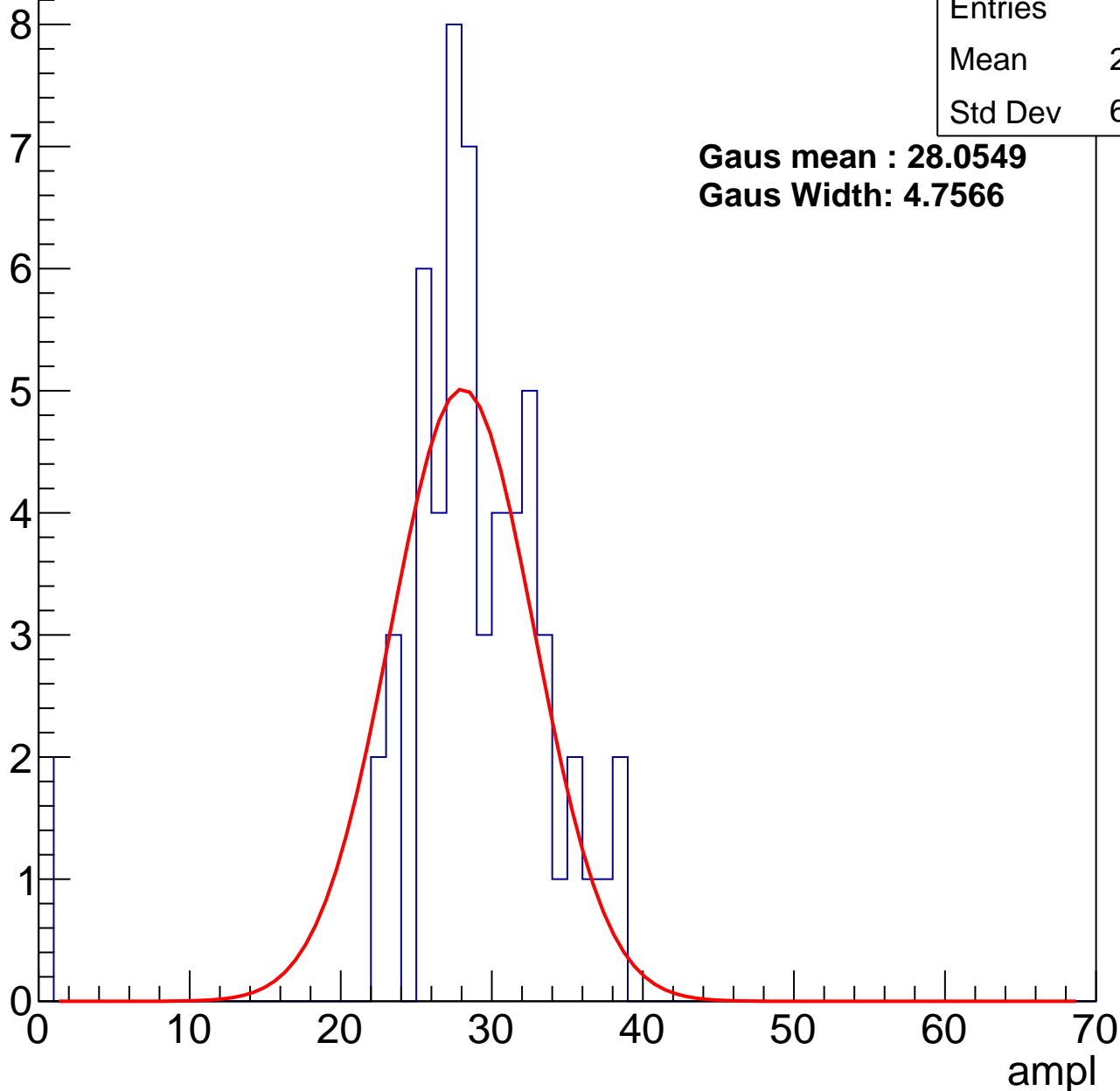
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	58
Mean	27.97
Std Dev	6.542

**Gaus mean : 28.0549**

**Gaus Width: 4.7566**



# B1L103S, U9-ch114, adc1

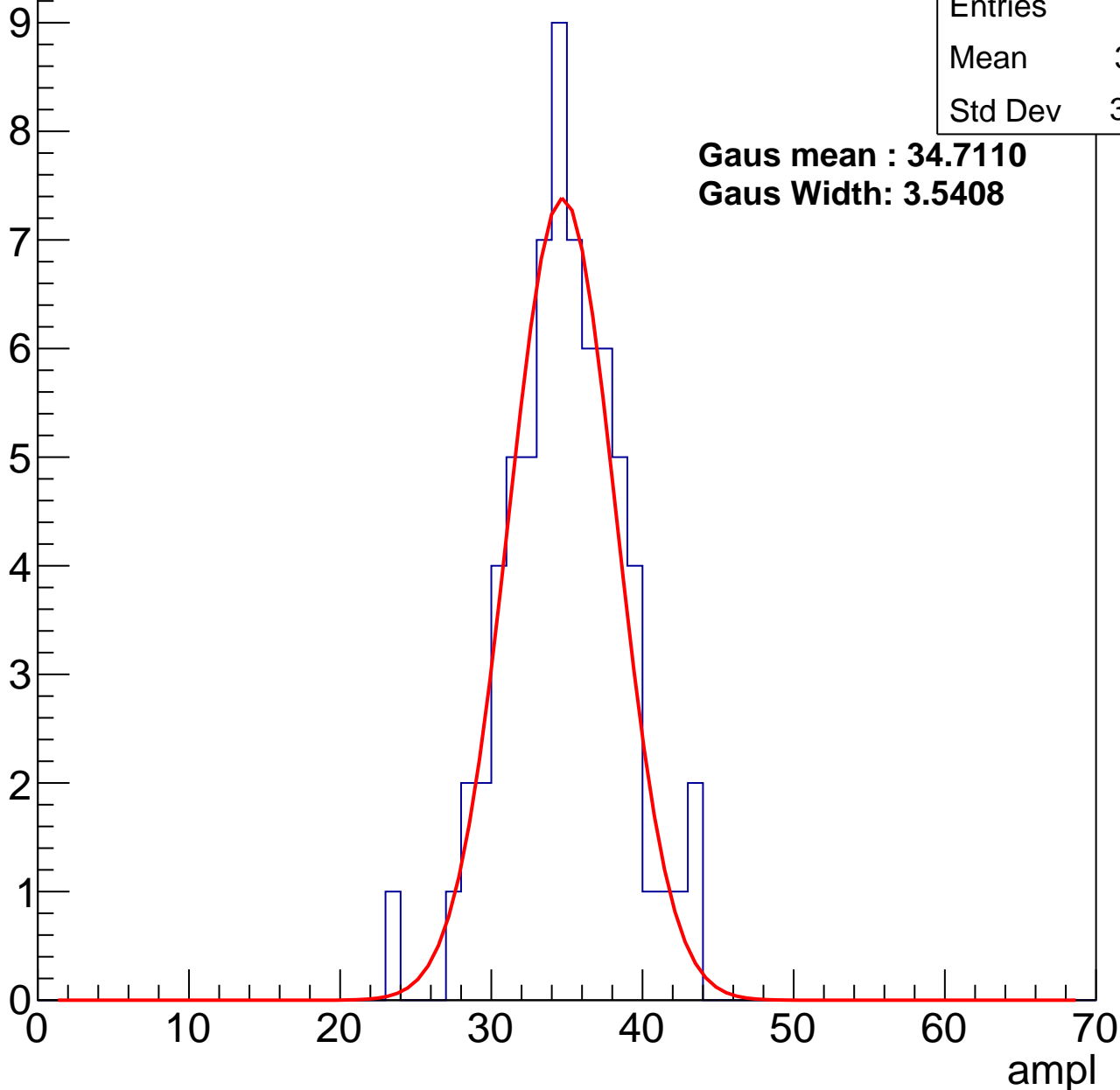
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	69
Mean	34.41
Std Dev	3.793

**Gaus mean : 34.7110**

**Gaus Width: 3.5408**



# B1L103S, U9-ch114, adc2

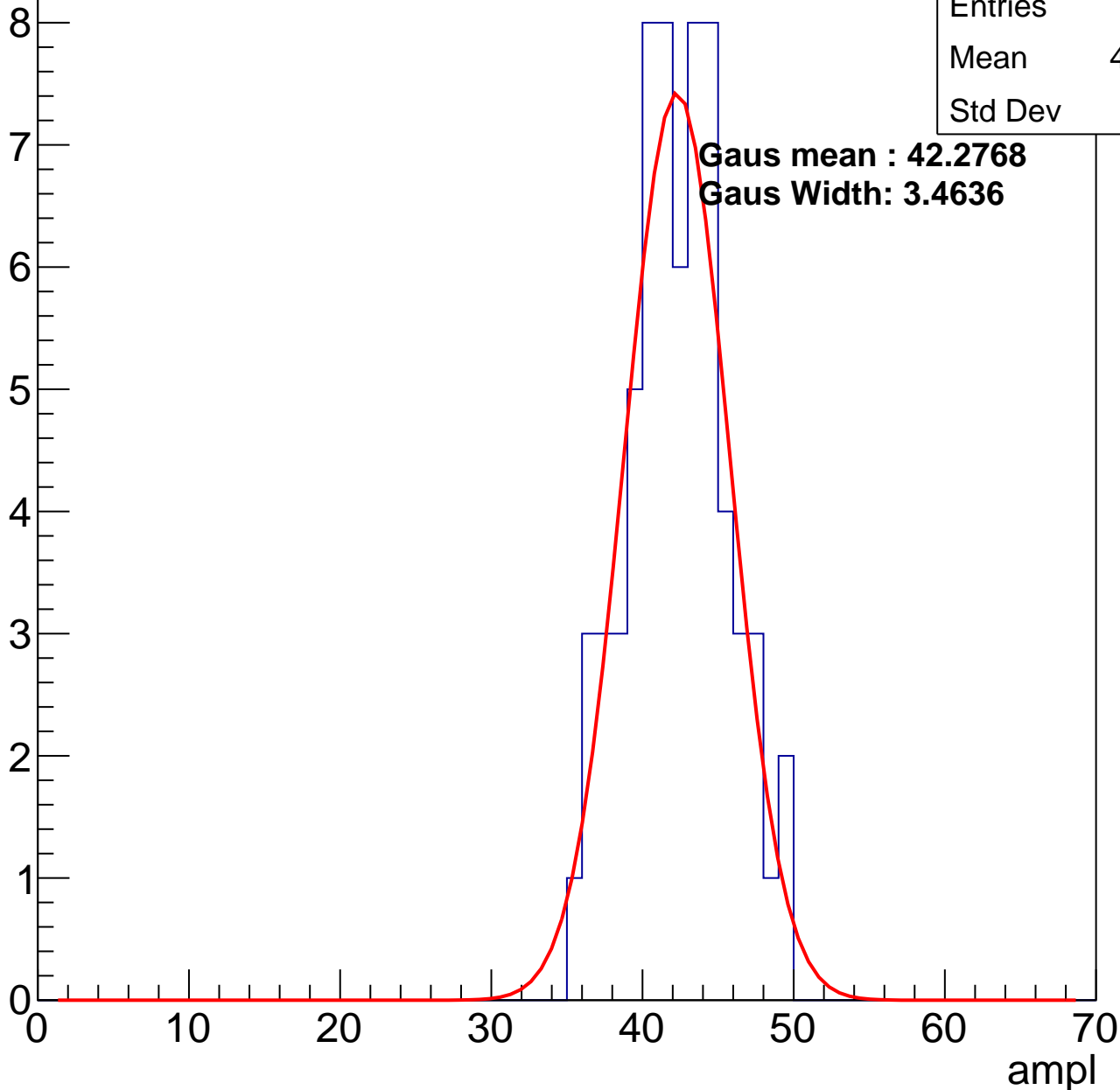
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	41.88
Std Dev	3.25

**Gaus mean : 42.2768**

**Gaus Width: 3.4636**

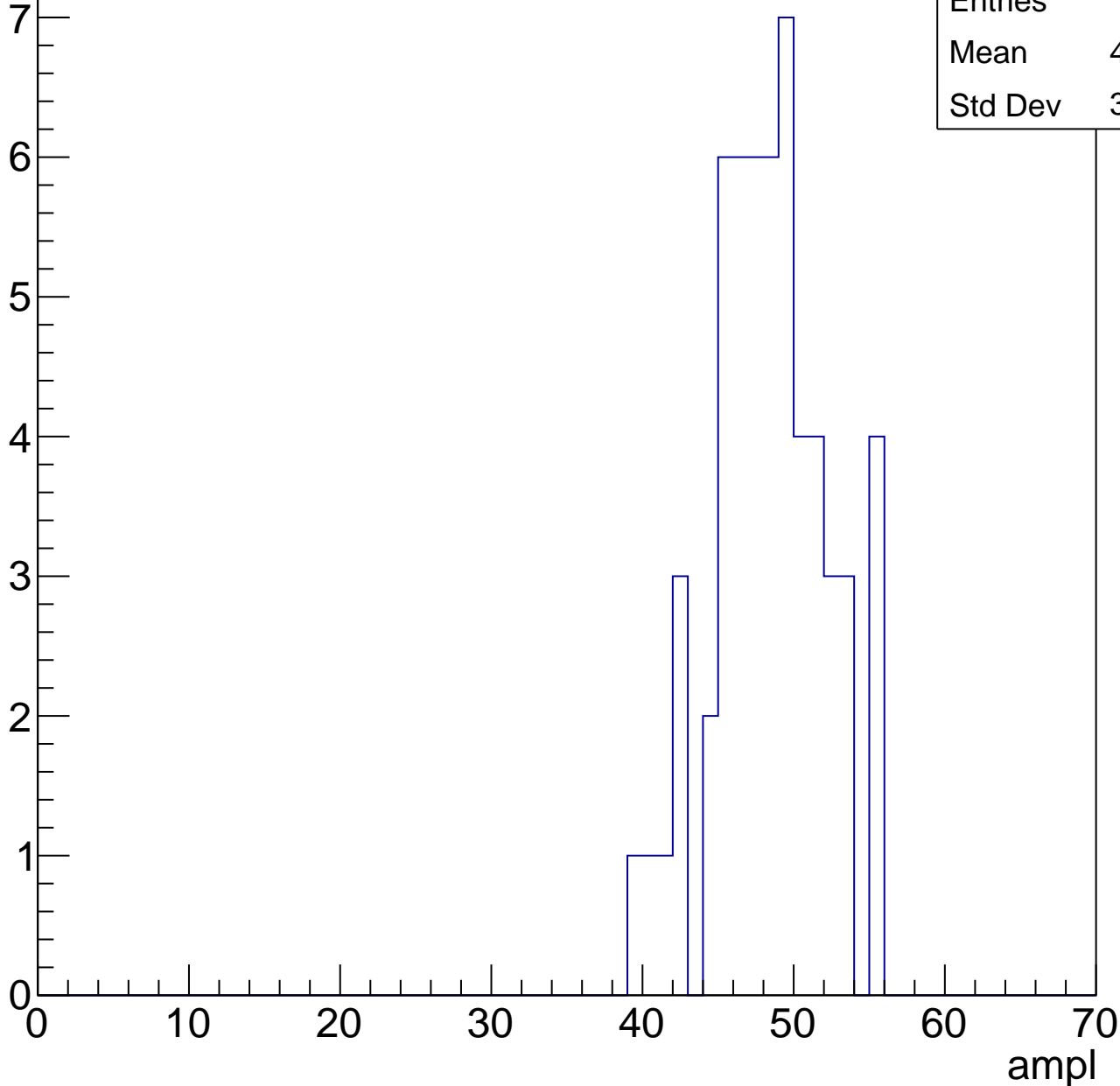


# B1L103S, U9-ch114, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	57
Mean	47.93
Std Dev	3.736



# B1L103S, U9-ch114, adc4

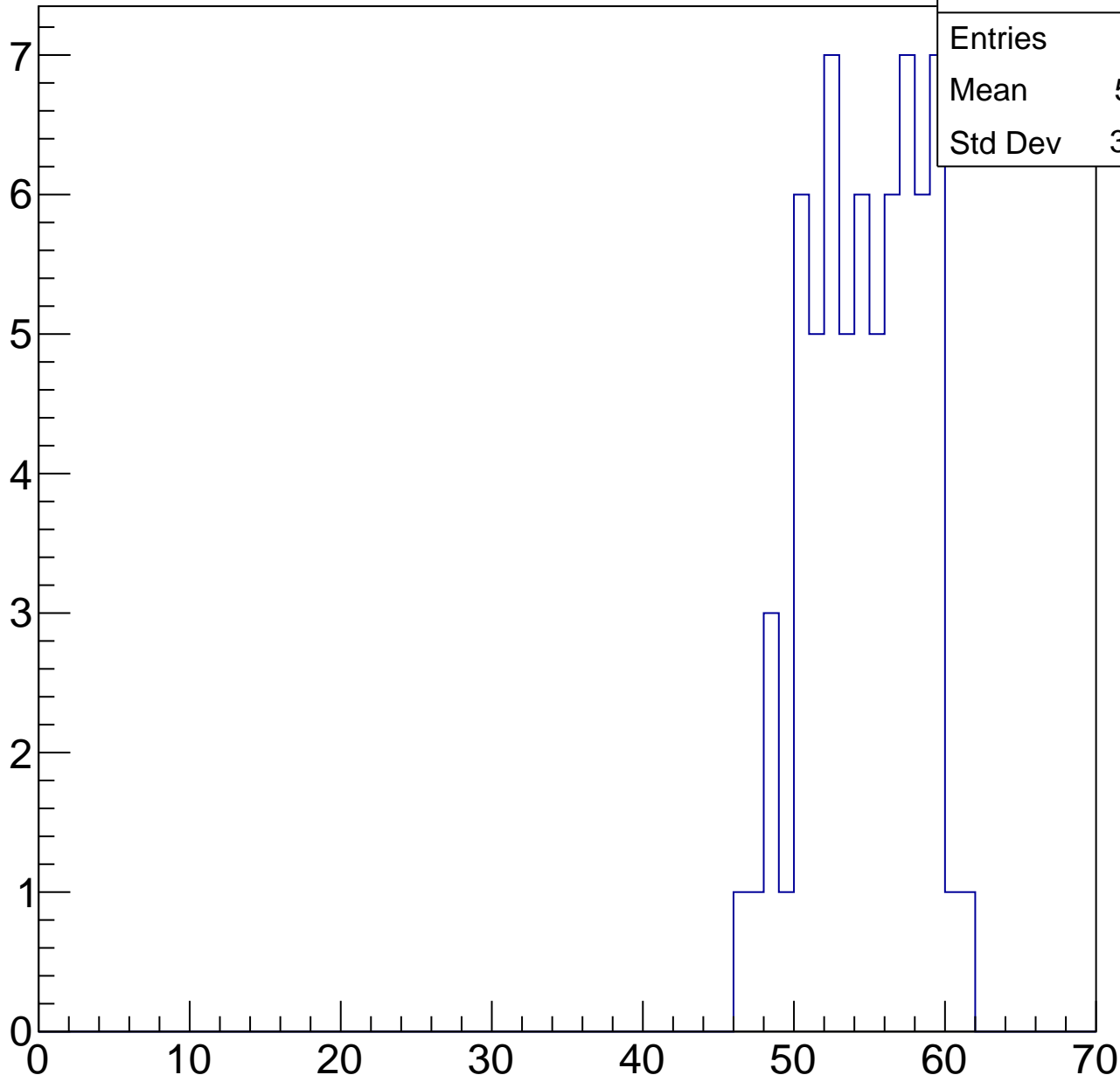
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

7  
6  
5  
4  
3  
2  
1  
0

Entries	68
Mean	54.21
Std Dev	3.567

ampl

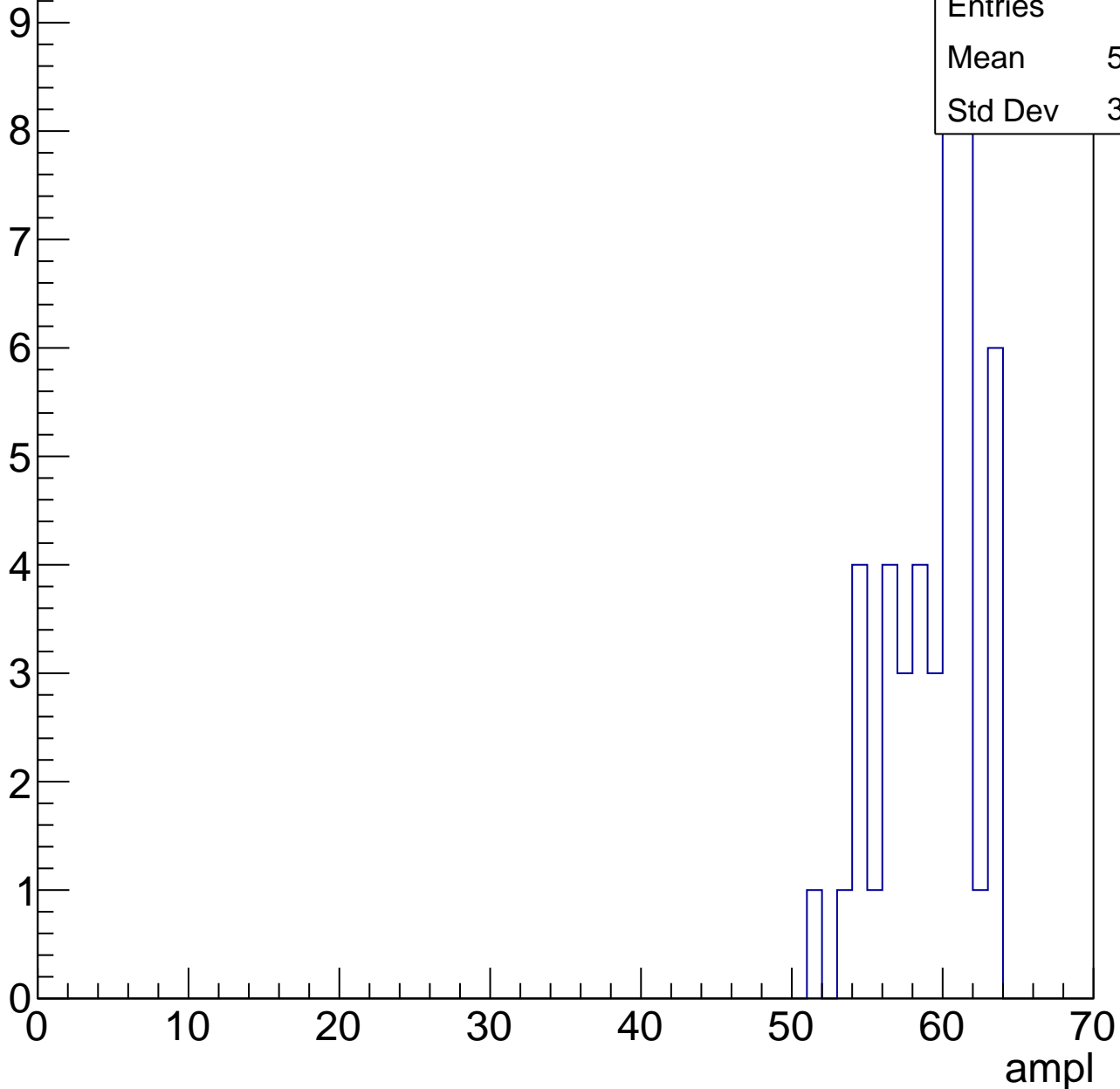


# B1L103S, U9-ch114, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	45
Mean	58.82
Std Dev	3.028

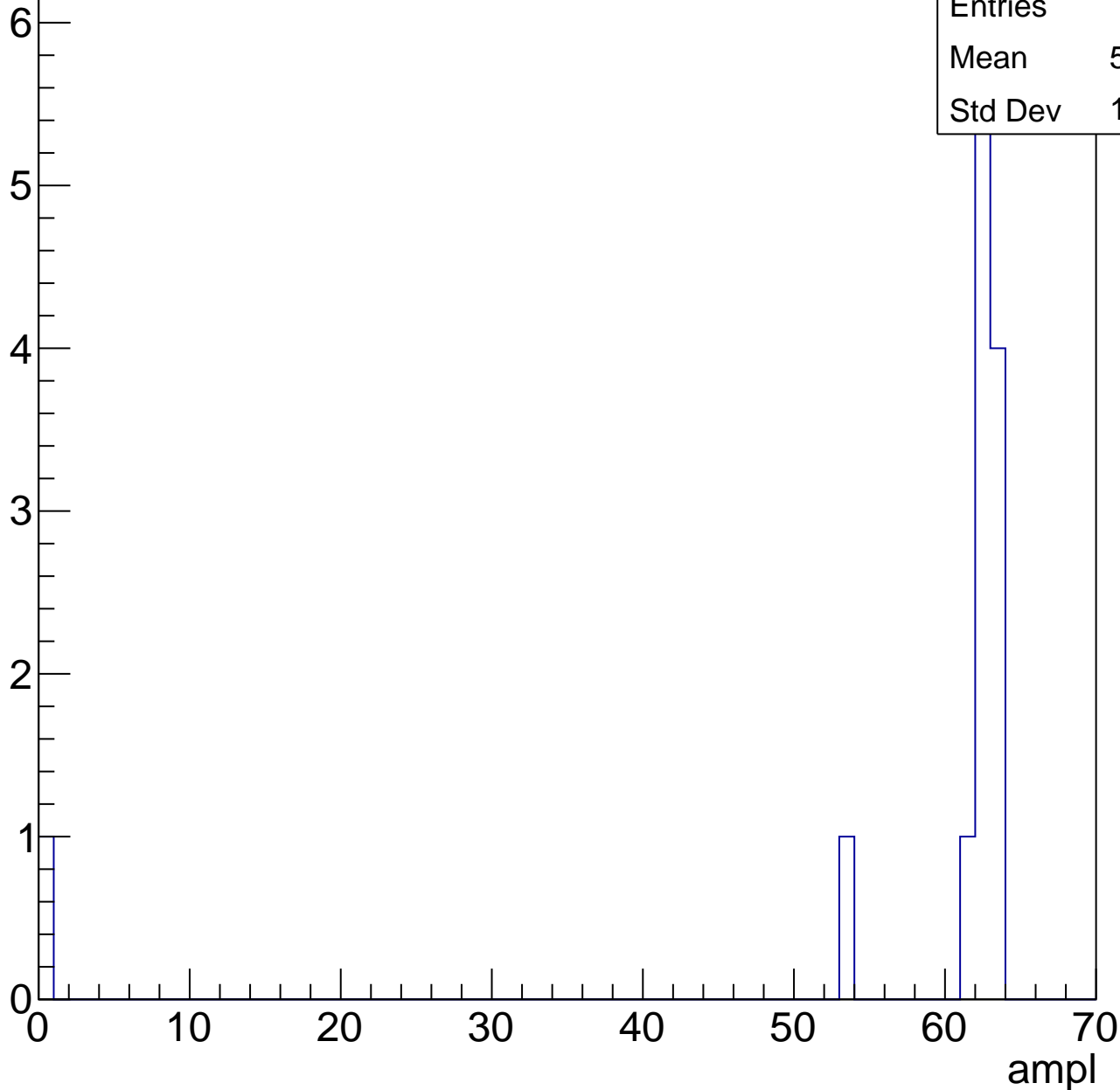


# B1L103S, U9-ch114, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	13
Mean	56.77
Std Dev	16.58

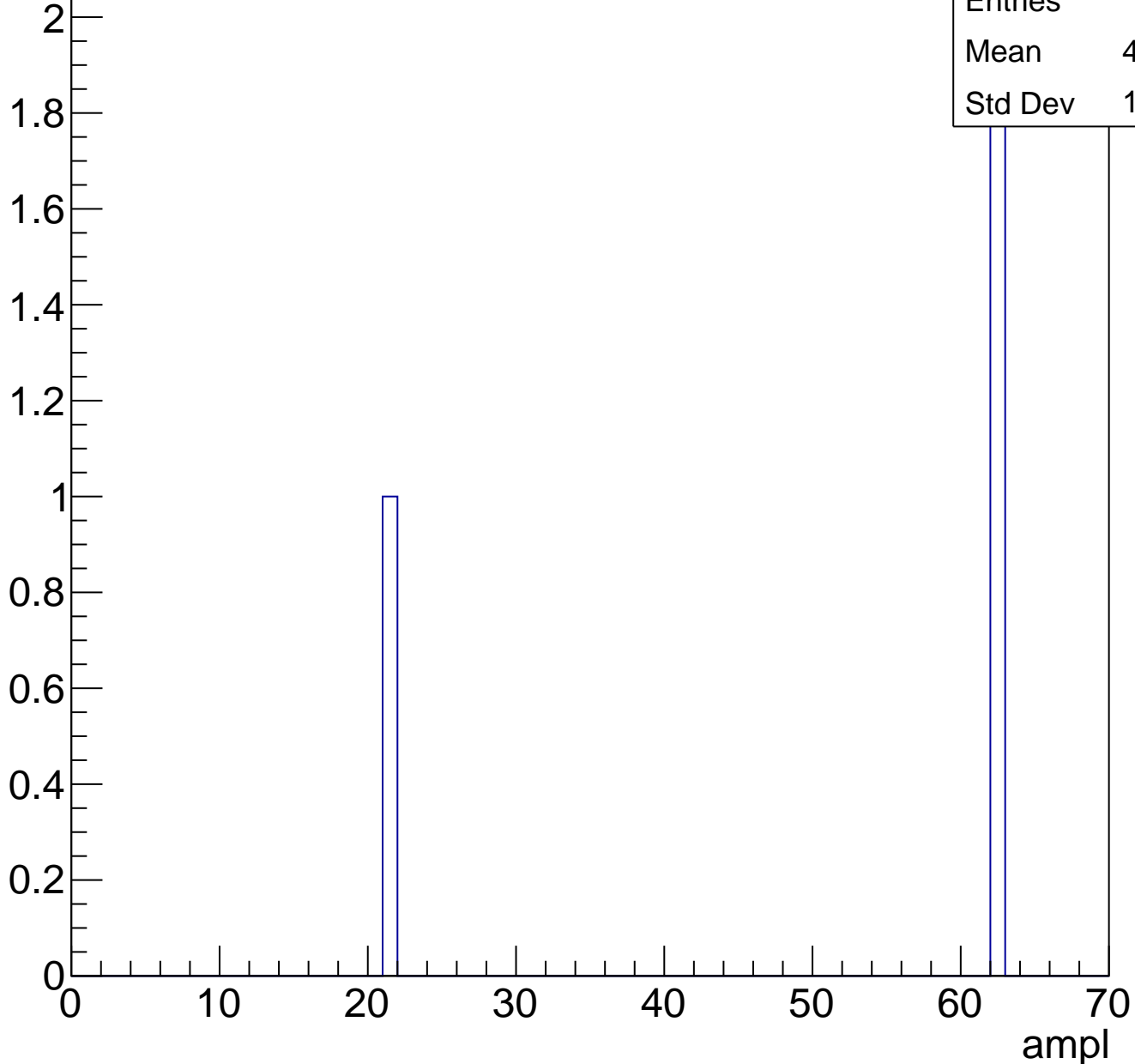




# B1L103S, U9-ch114, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	3
Mean	48.33
Std Dev	19.33

# B1L103S, U9-ch115, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	78
Mean	28.58
Std Dev	6.783

**Gaus mean : 29.9851**

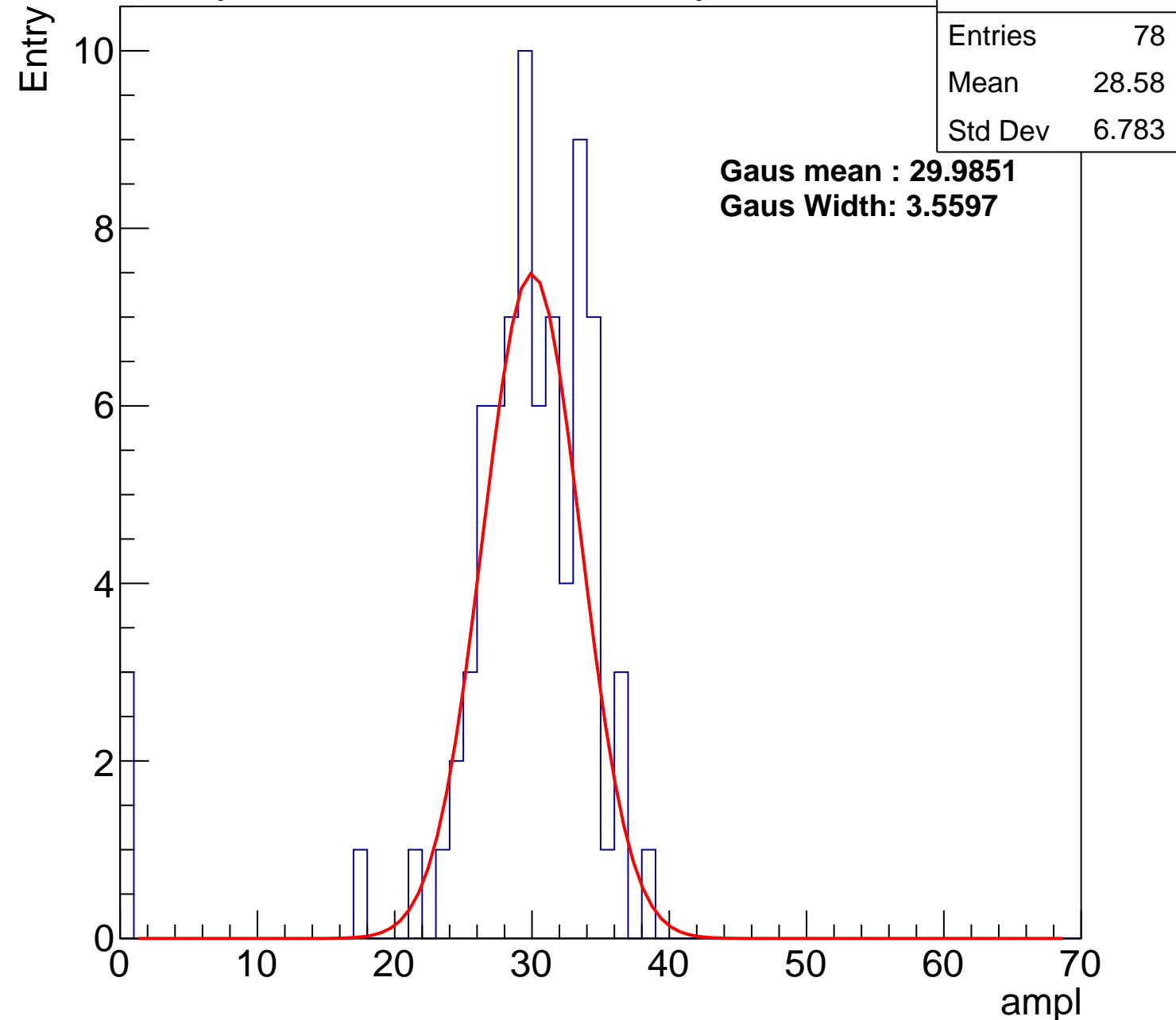
**Gaus Width: 3.5597**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U9-ch115, adc1

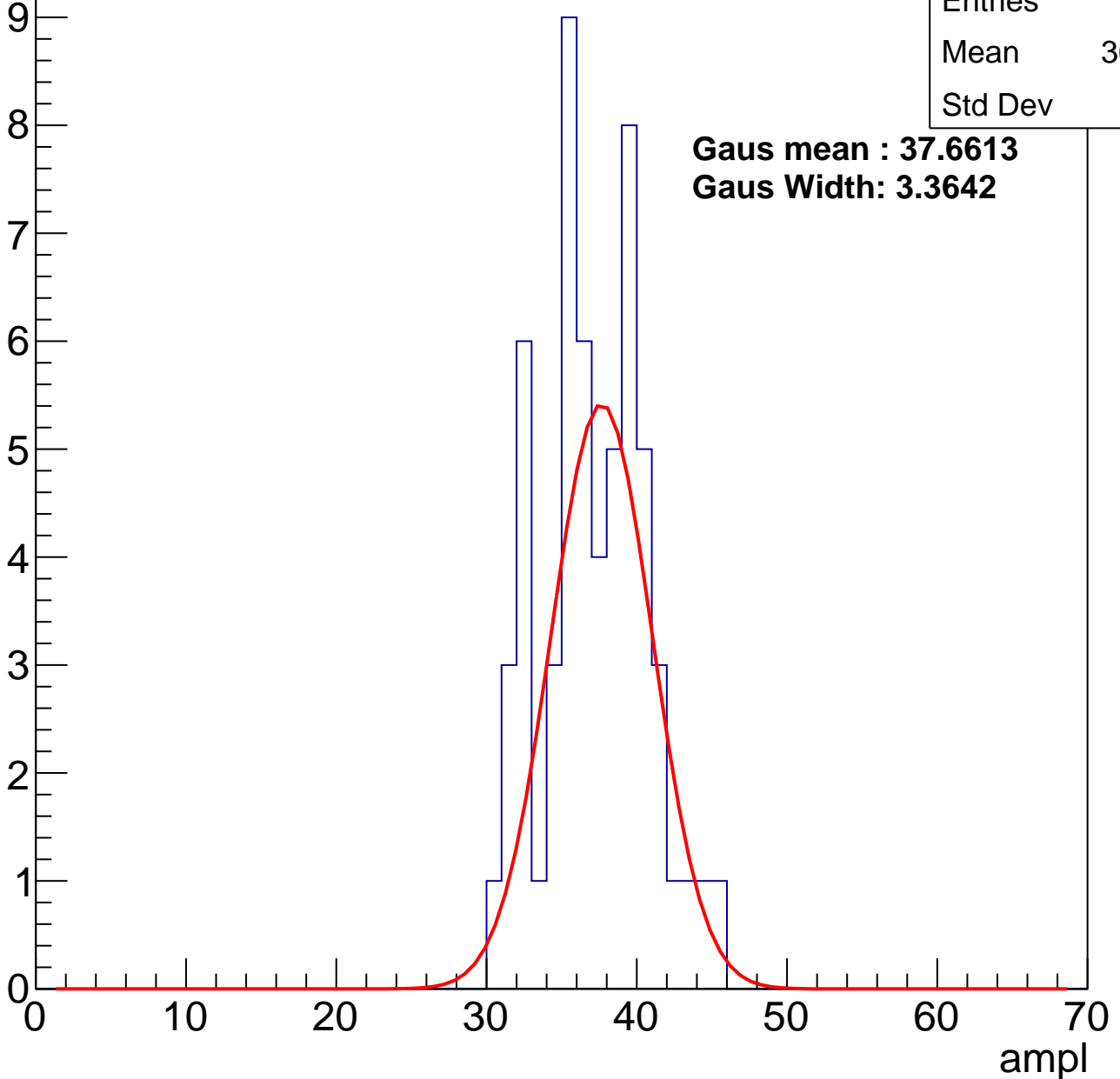
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	58
Mean	36.69
Std Dev	3.45

**Gaus mean : 37.6613**

**Gaus Width: 3.3642**



# B1L103S, U9-ch115, adc2

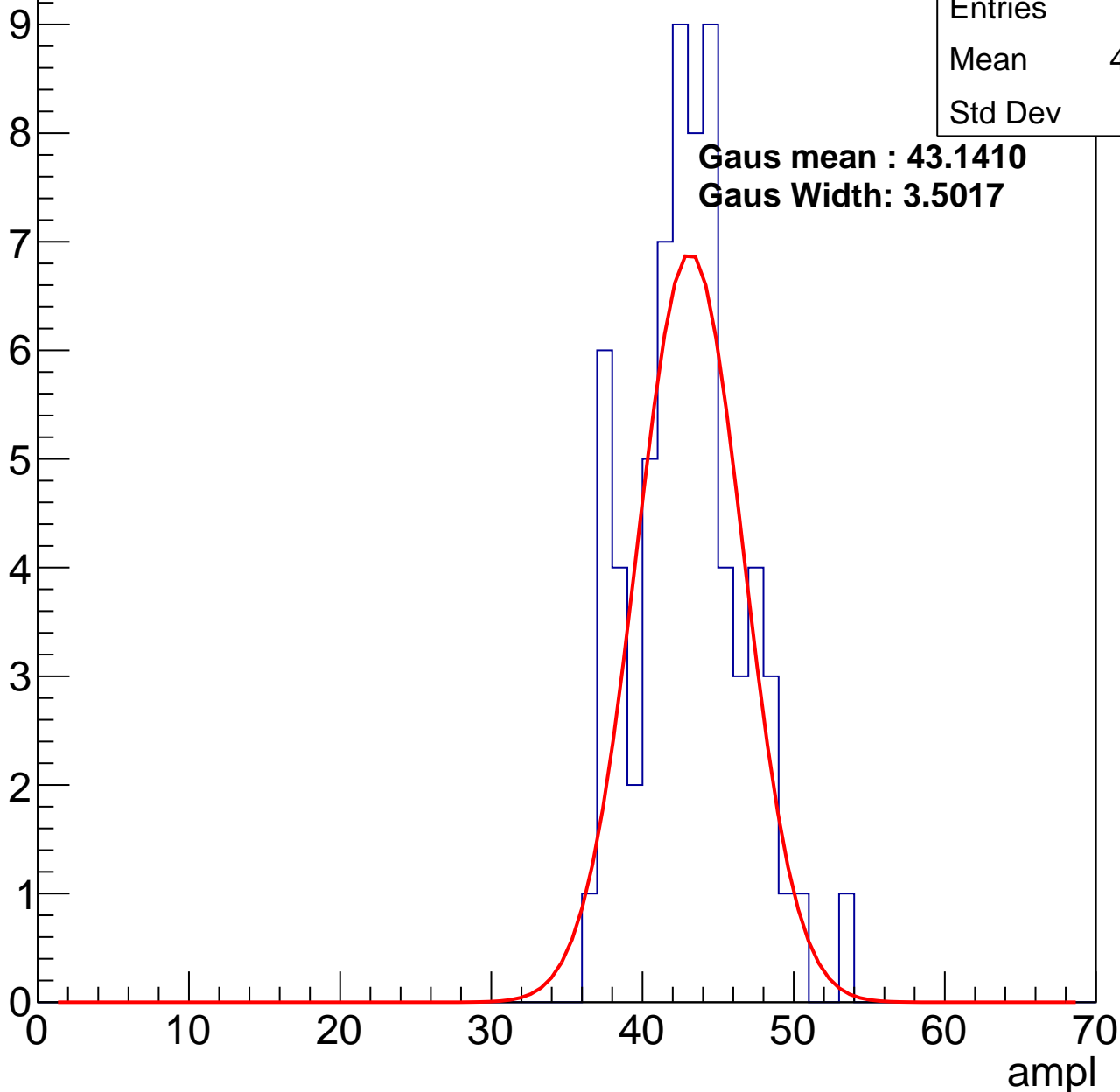
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	68
Mean	42.57
Std Dev	3.52

**Gaus mean : 43.1410**

**Gaus Width: 3.5017**

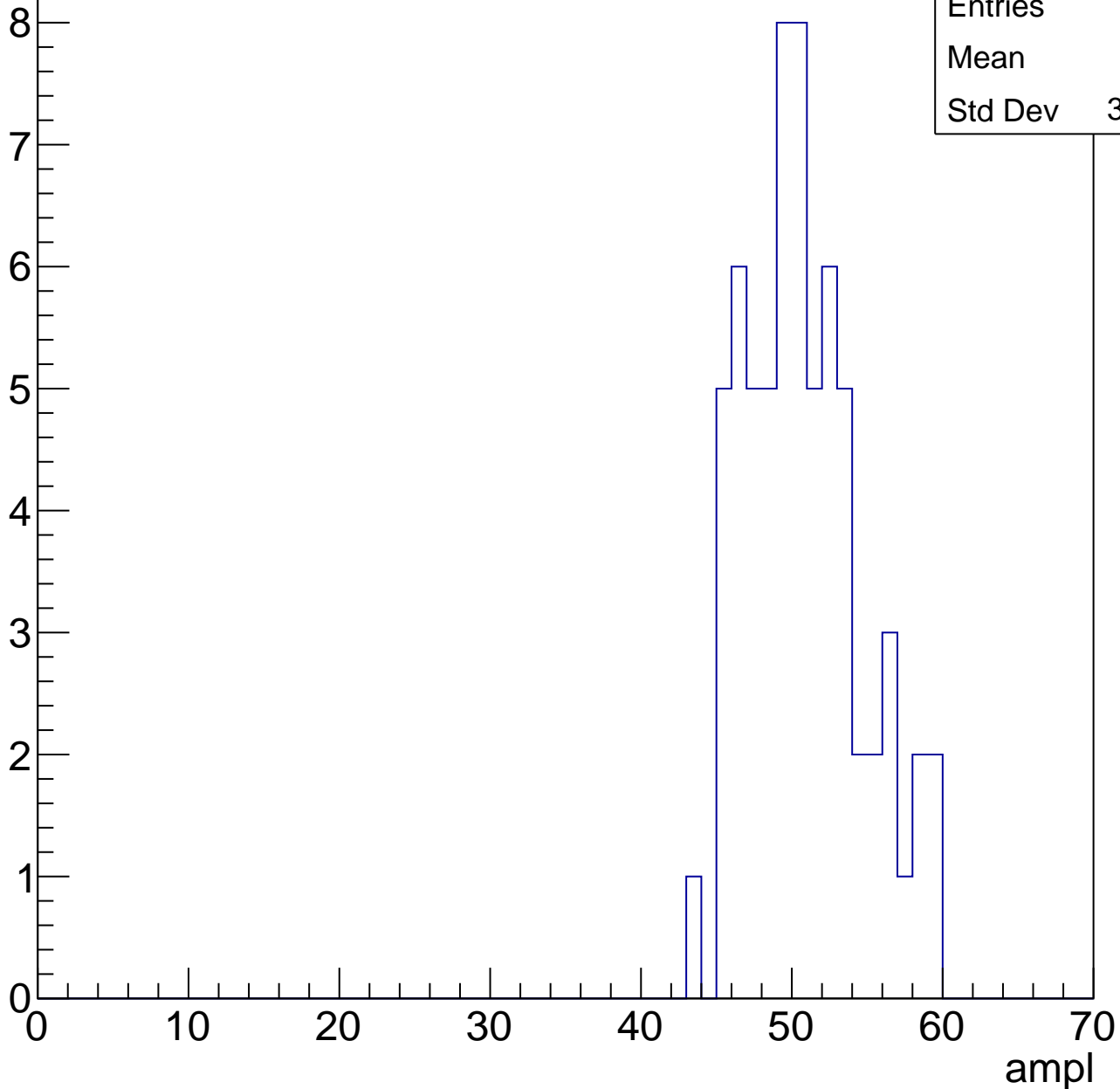


# B1L103S, U9-ch115, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	50.3
Std Dev	3.774

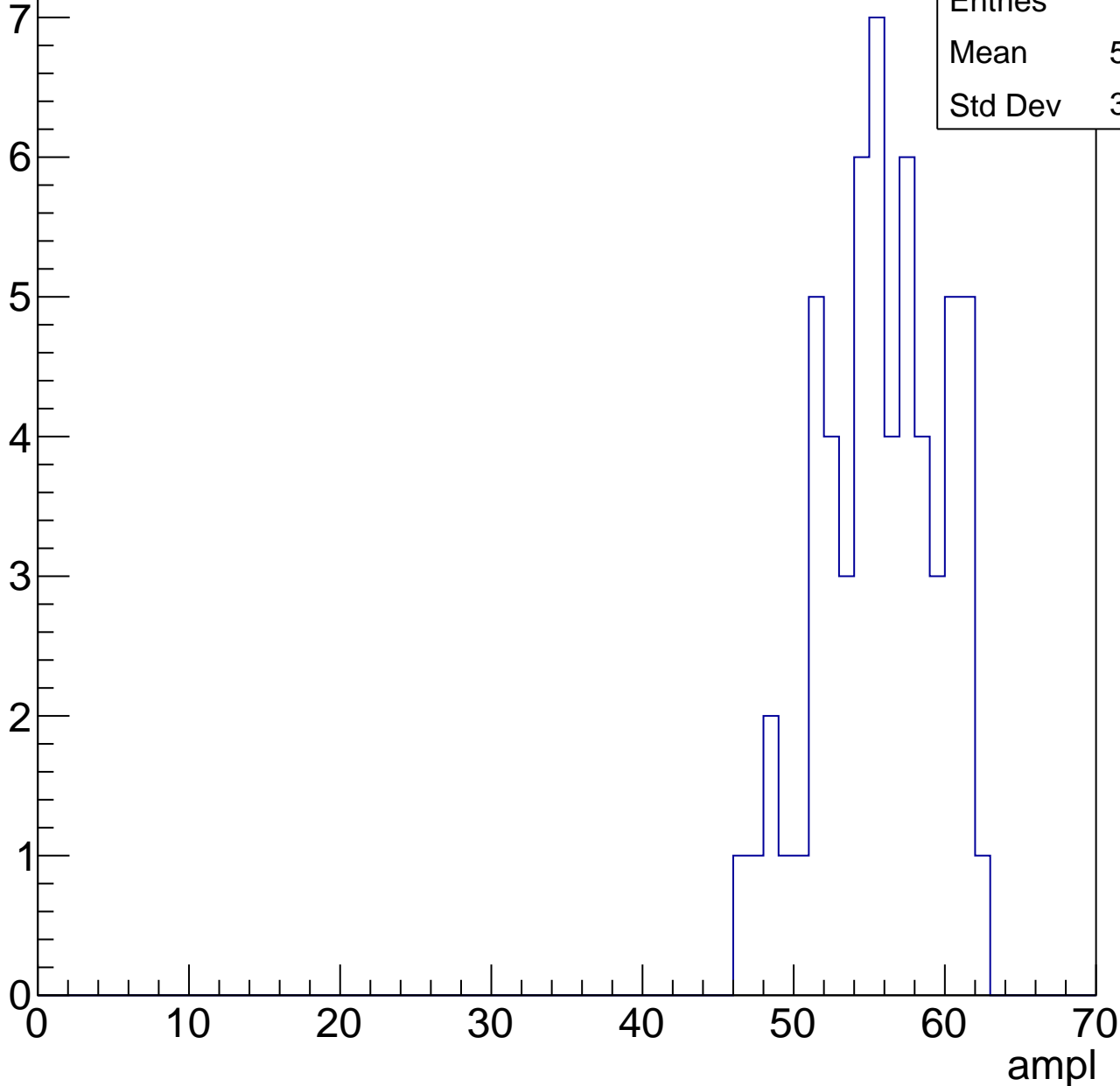


# B1L103S, U9-ch115, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	59
Mean	55.27
Std Dev	3.905

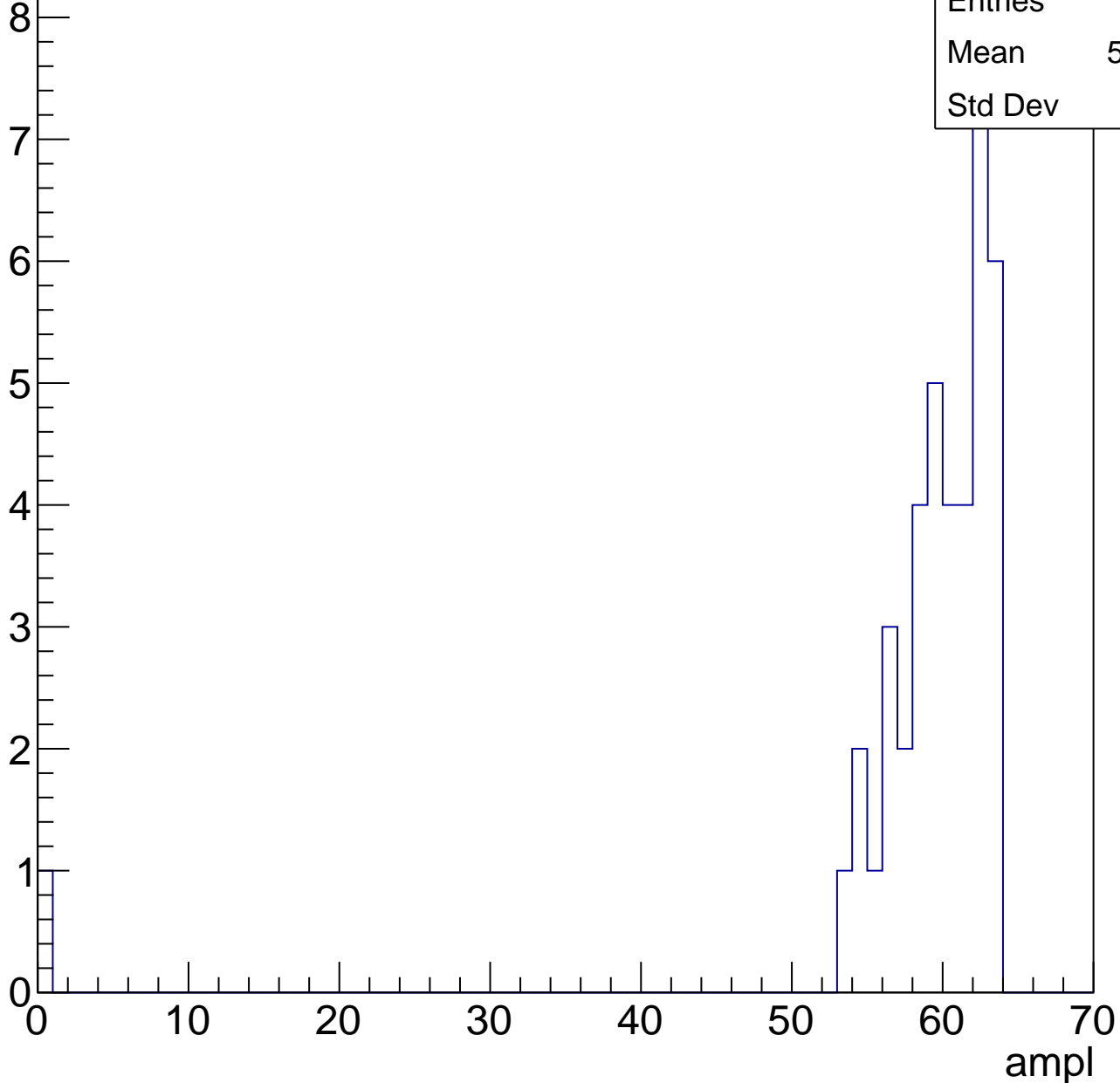


# B1L103S, U9-ch115, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

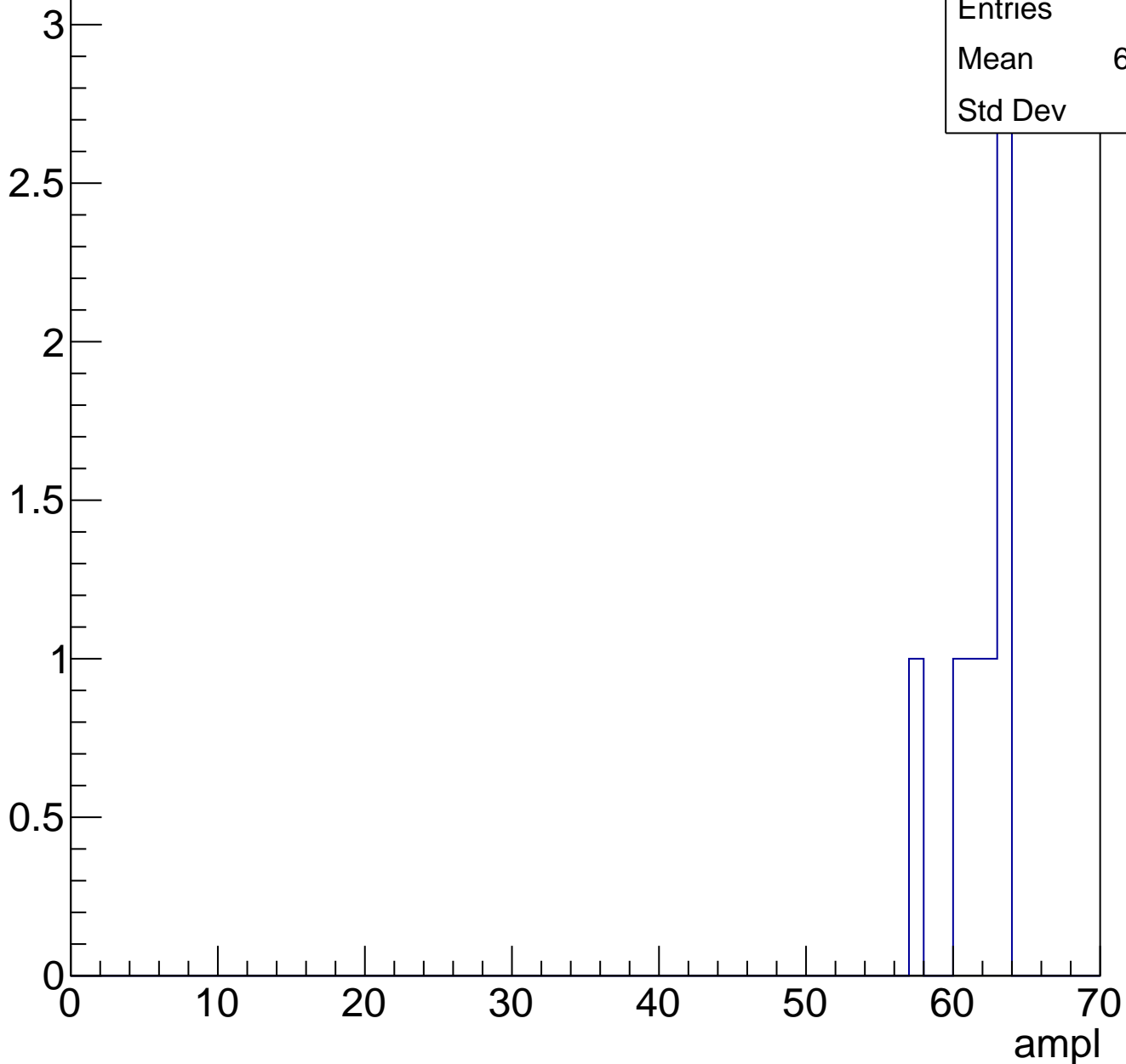
Entries	41
Mean	58.12
Std Dev	9.6



# B1L103S, U9-ch115, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



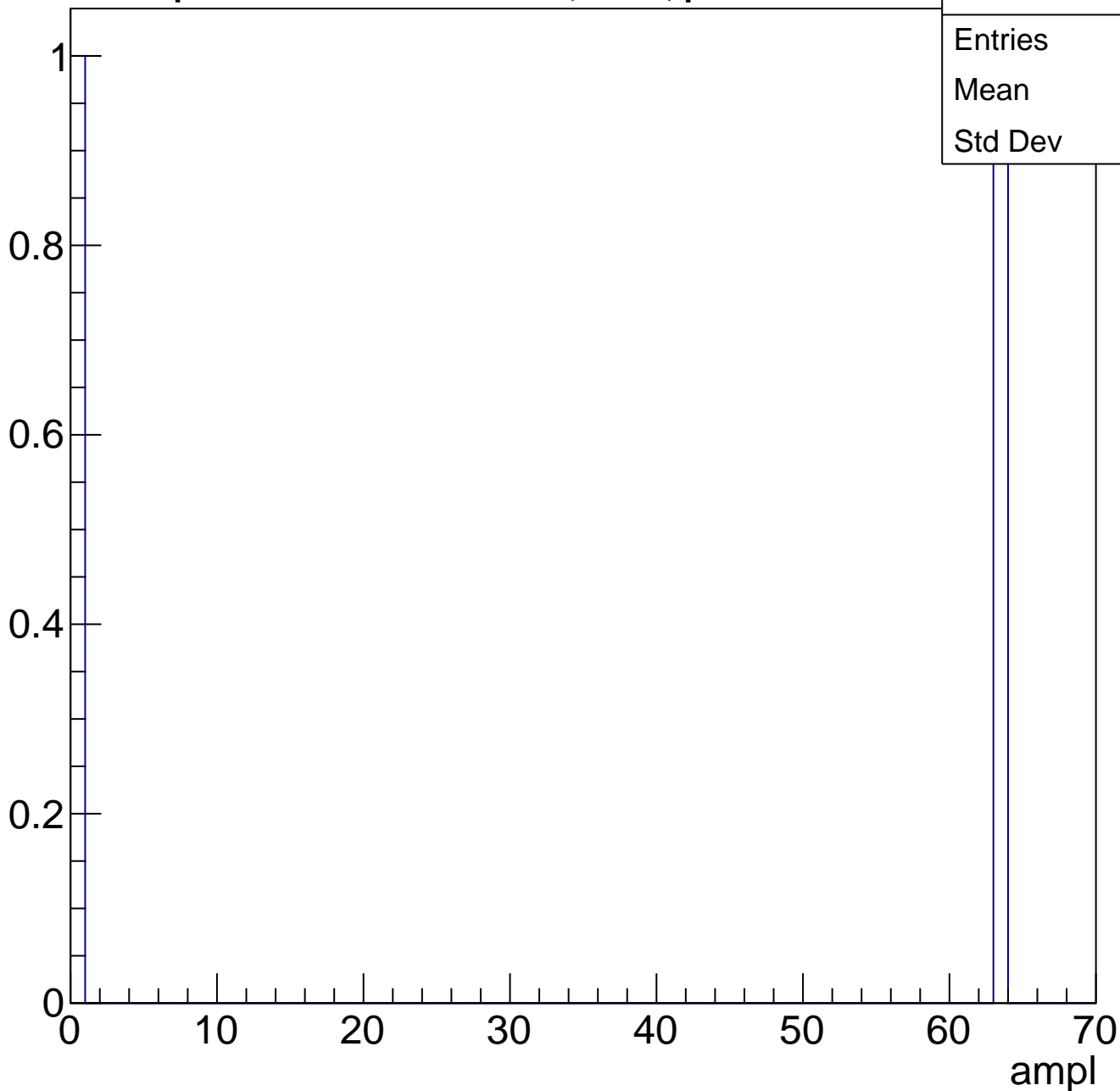
Entries	7
Mean	61.29
Std Dev	2.05



# B1L103S, U9-ch115, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U9-ch116, adc0

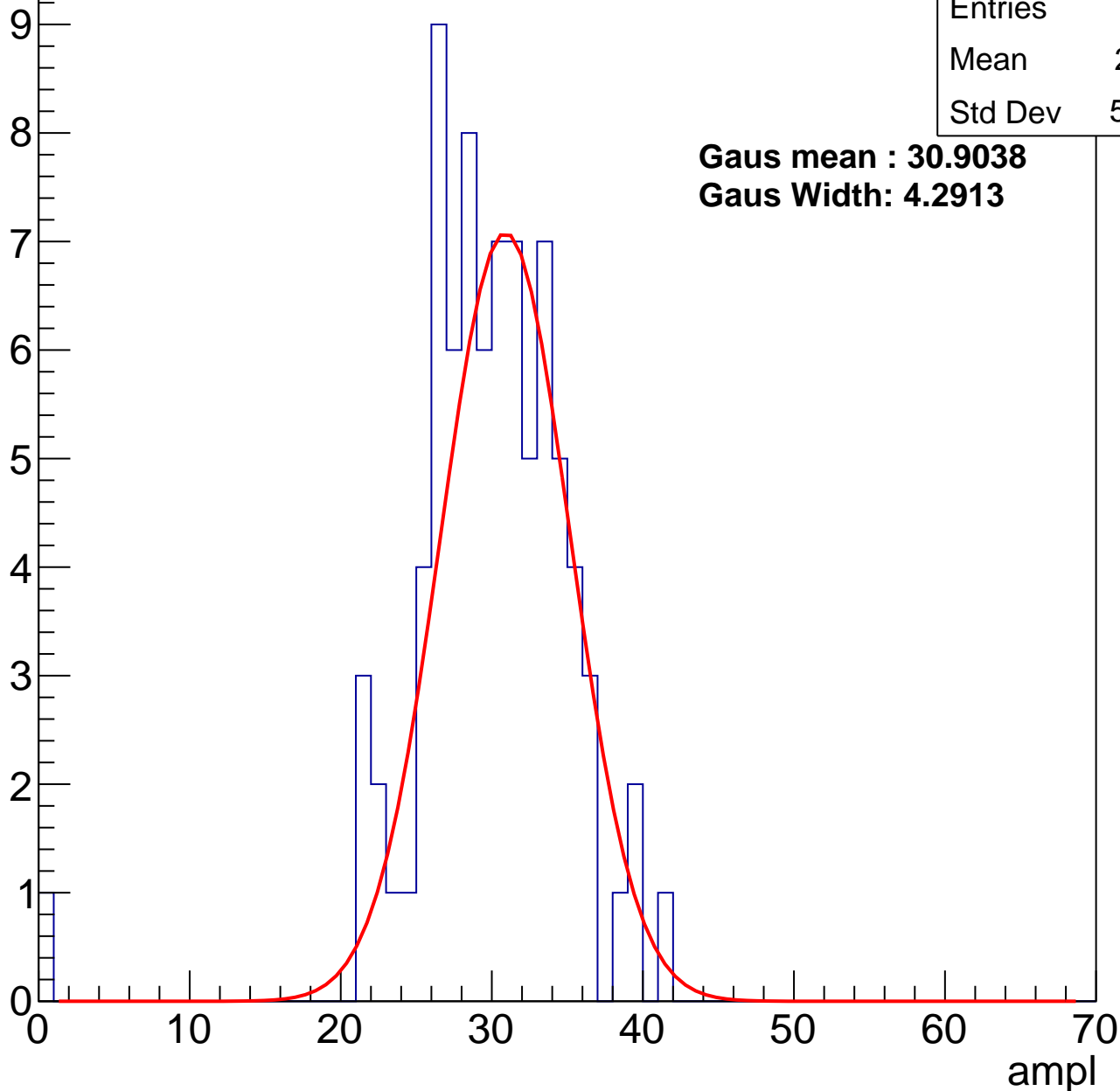
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	83
Mean	29.41
Std Dev	5.364

**Gaus mean : 30.9038**

**Gaus Width: 4.2913**



# B1L103S, U9-ch116, adc1

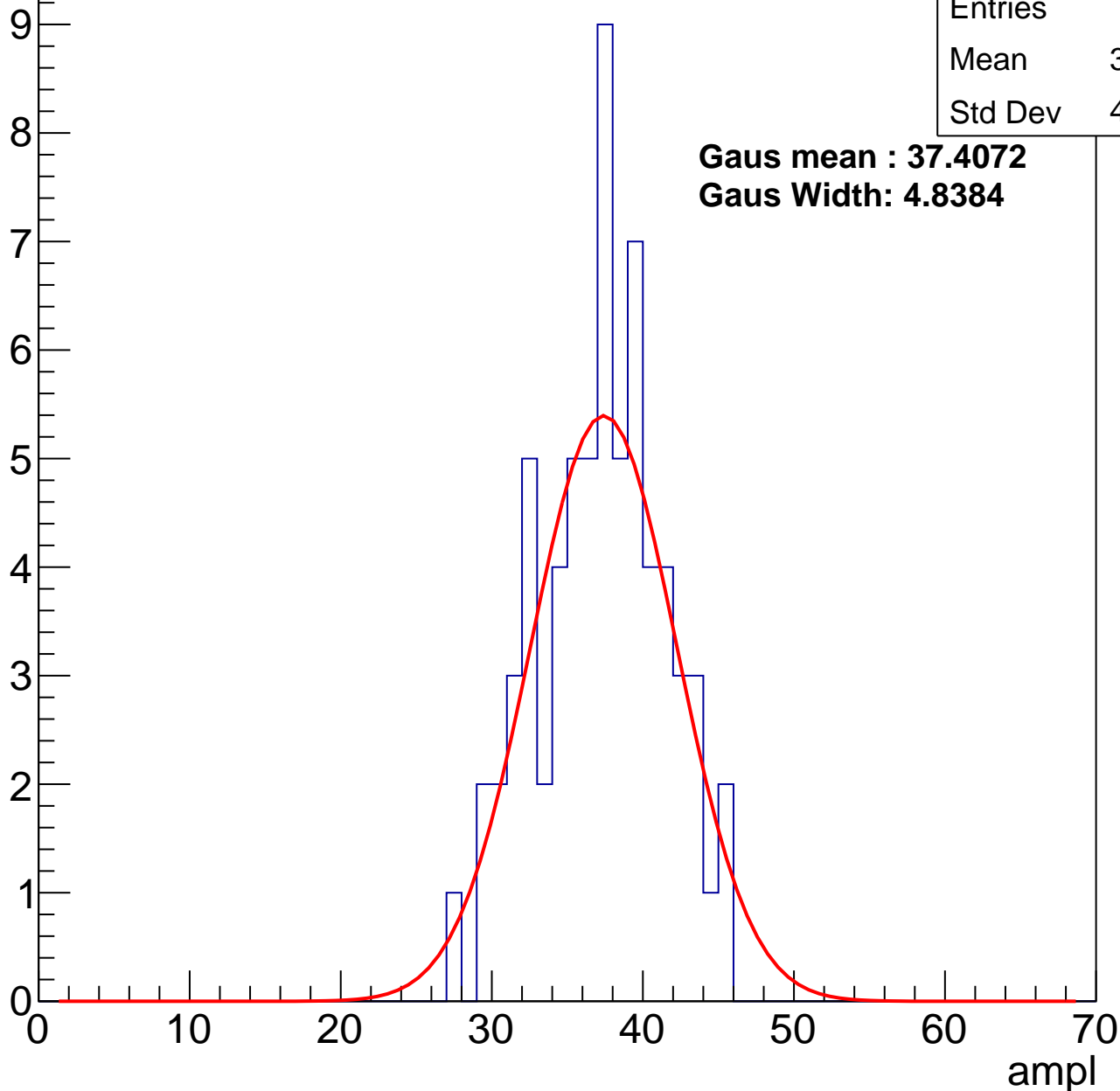
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	36.78
Std Dev	4.128

**Gaus mean : 37.4072**

**Gaus Width: 4.8384**



# B1L103S, U9-ch116, adc2

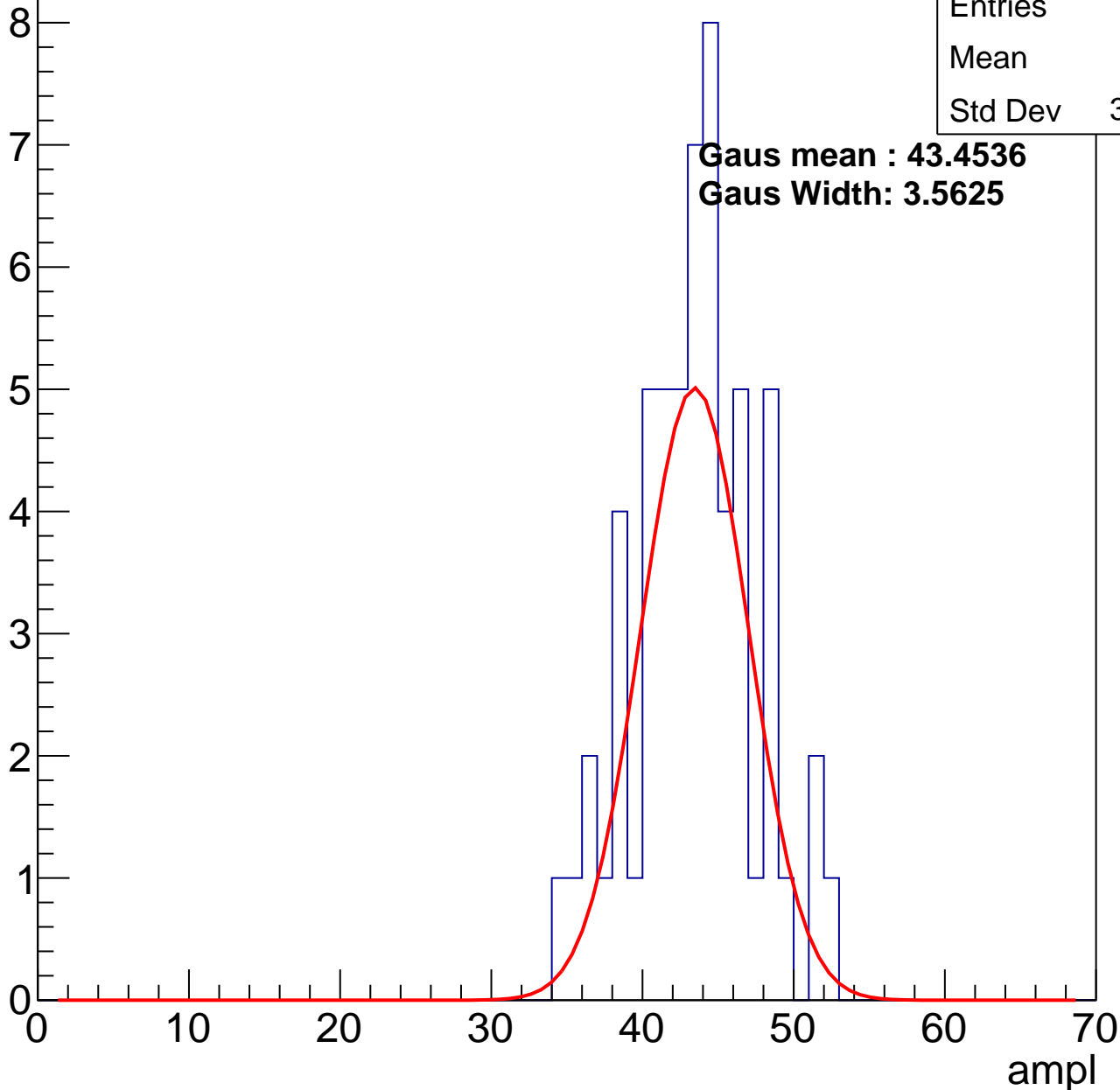
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	59
Mean	43
Std Dev	3.949

**Gaus mean : 43.4536**

**Gaus Width: 3.5625**

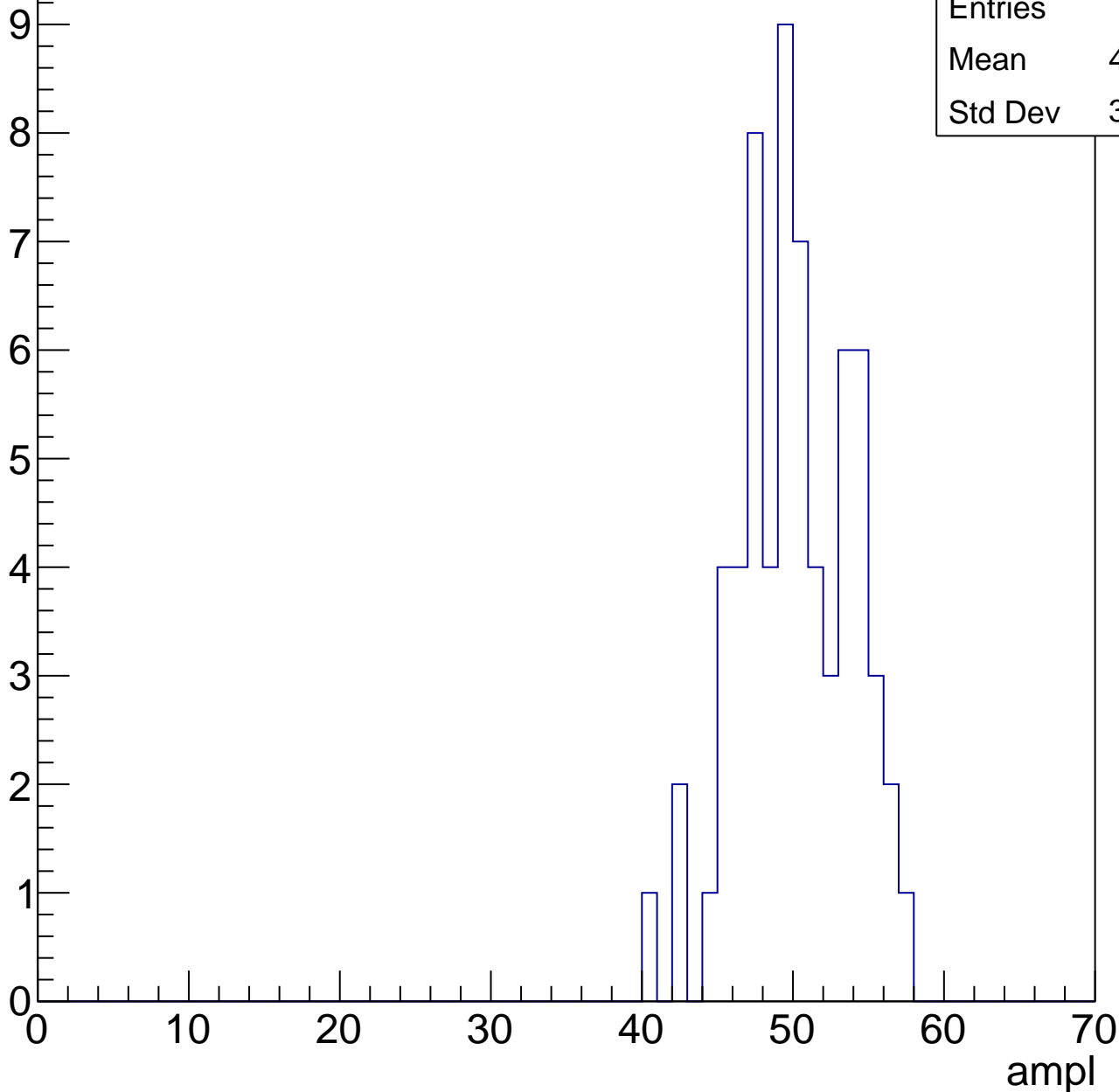


# B1L103S, U9-ch116, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	49.65
Std Dev	3.677

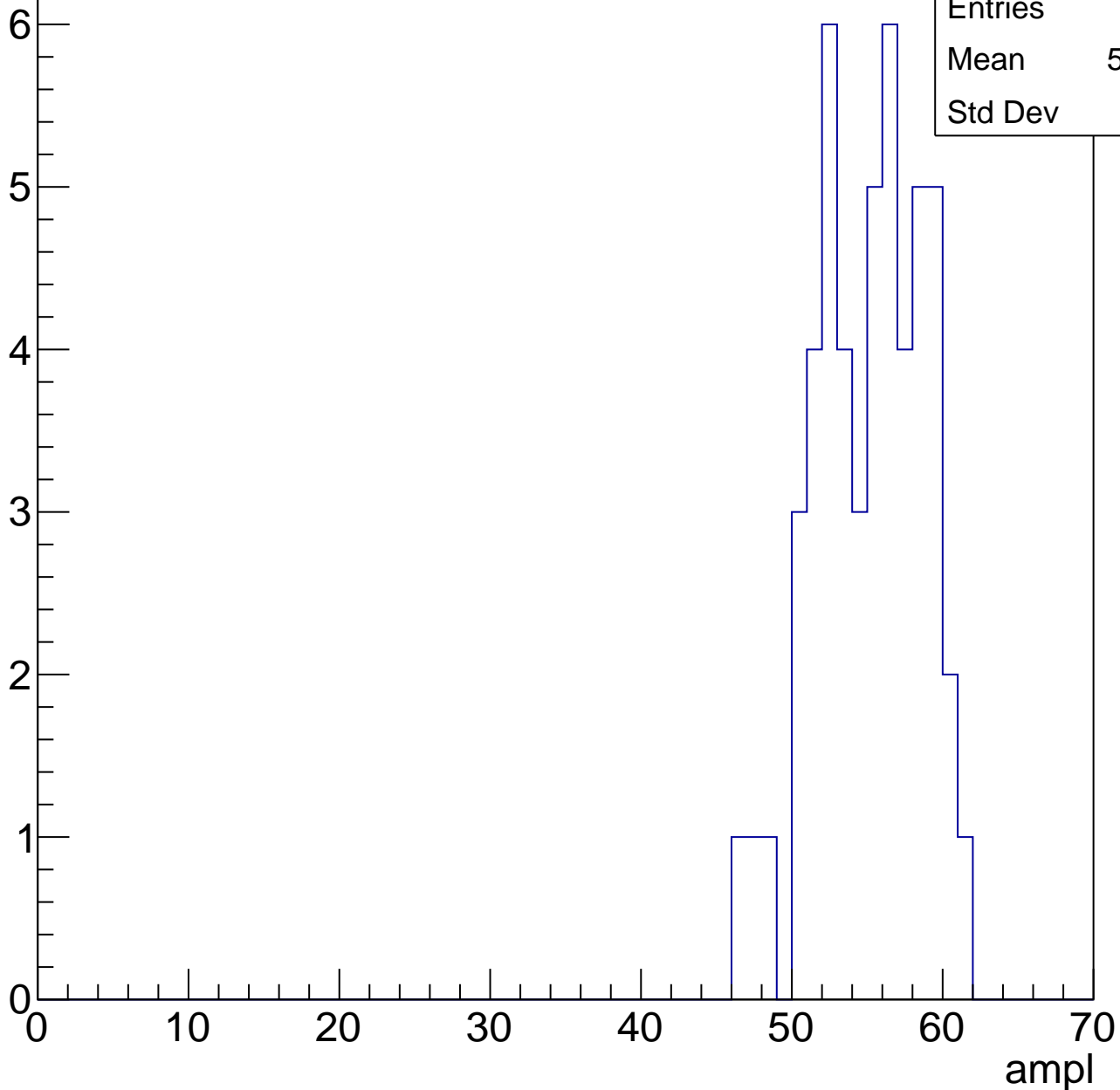


# B1L103S, U9-ch116, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	51
Mean	54.63
Std Dev	3.52



# B1L103S, U9-ch116, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	55
Mean	60.04
Std Dev	2.419

Entry

10

8

6

4

2

0

0

10

20

30

40

50

60

ampl

70

# B1L103S, U9-ch116, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U9-ch116, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U9-ch117, adc0

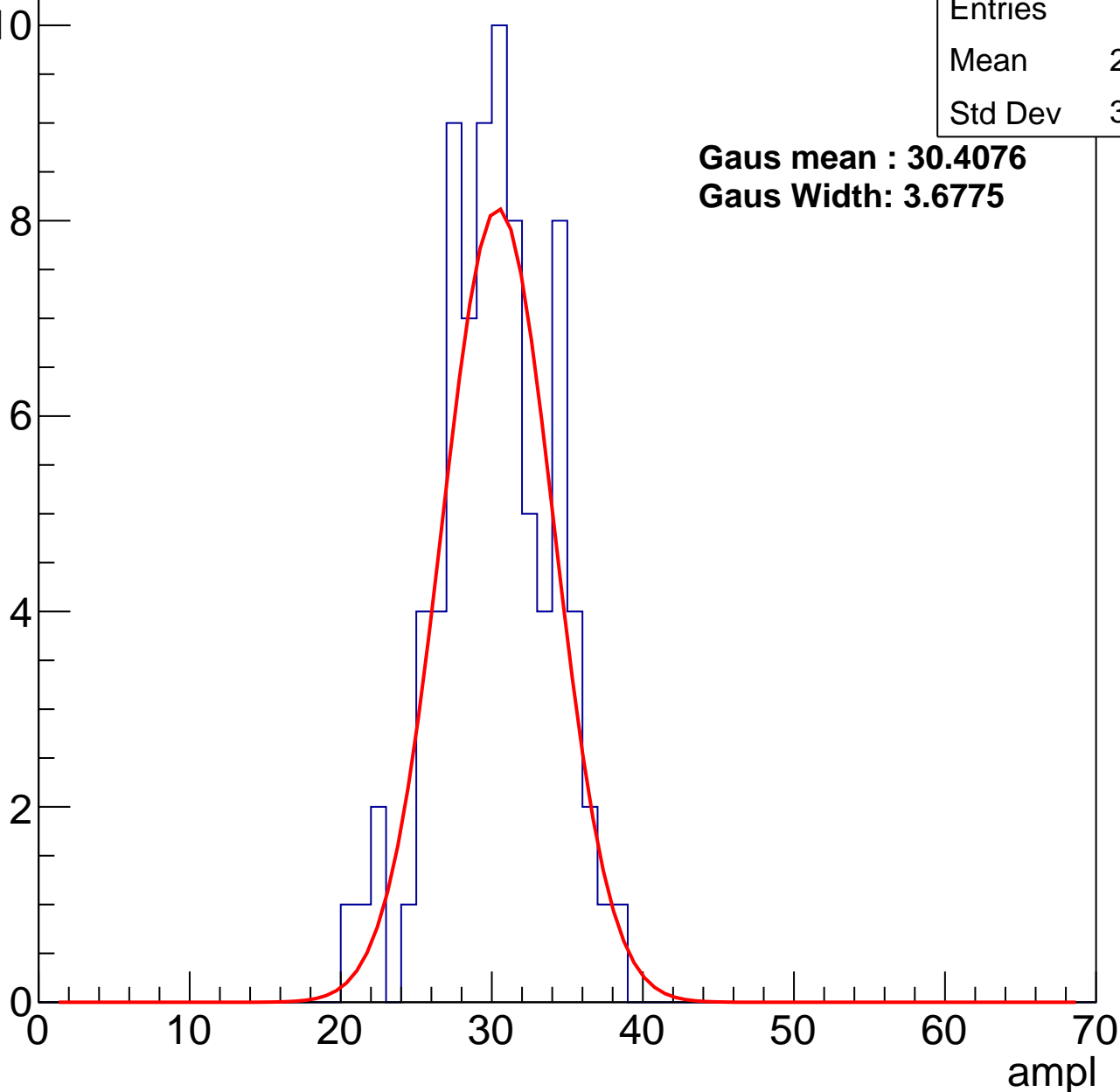
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	81
Mean	29.78
Std Dev	3.685

**Gaus mean : 30.4076**

**Gaus Width: 3.6775**



# B1L103S, U9-ch117, adc1

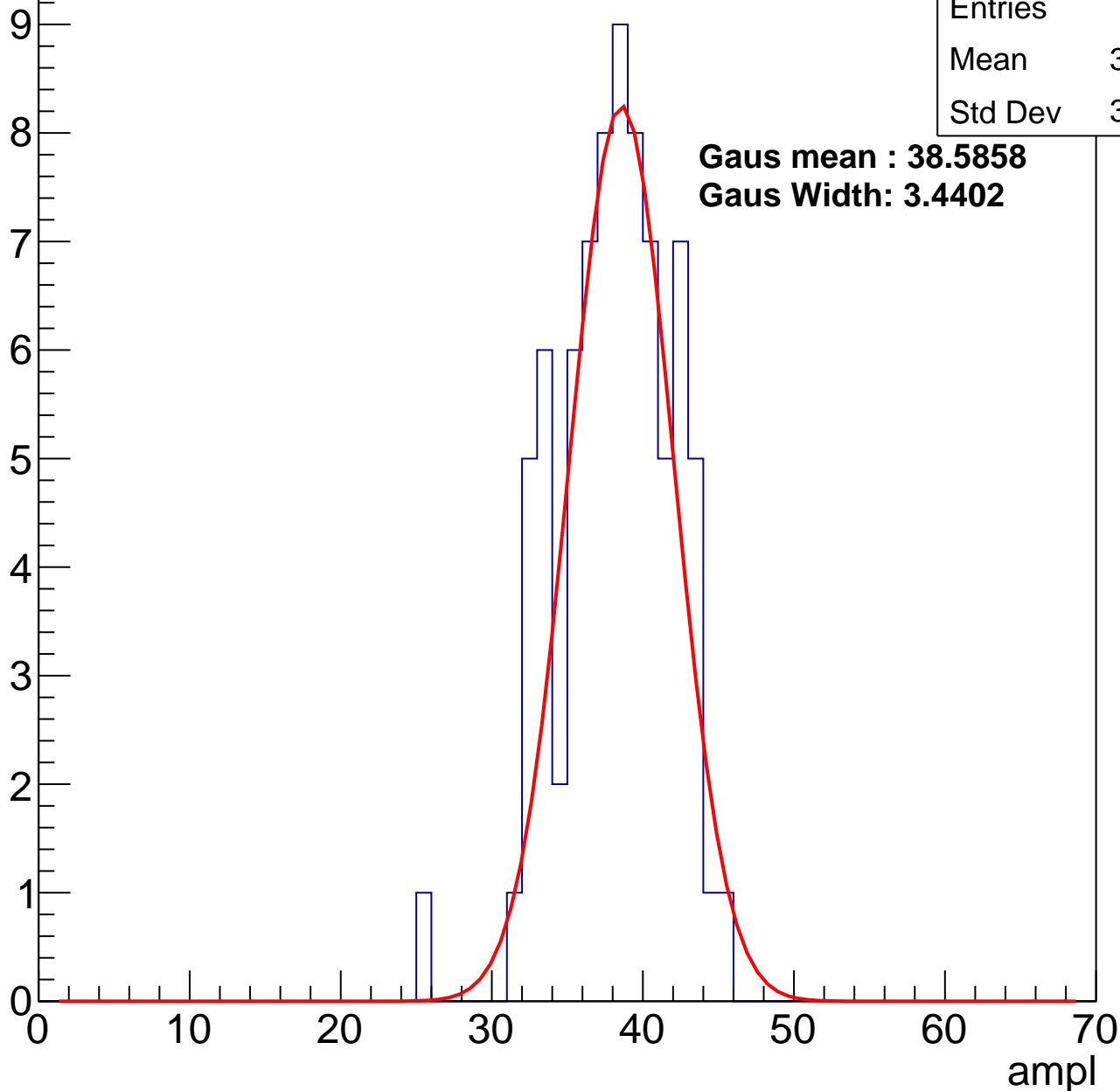
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	79
Mean	37.68
Std Dev	3.672

**Gaus mean : 38.5858**

**Gaus Width: 3.4402**



# B1L103S, U9-ch117, adc2

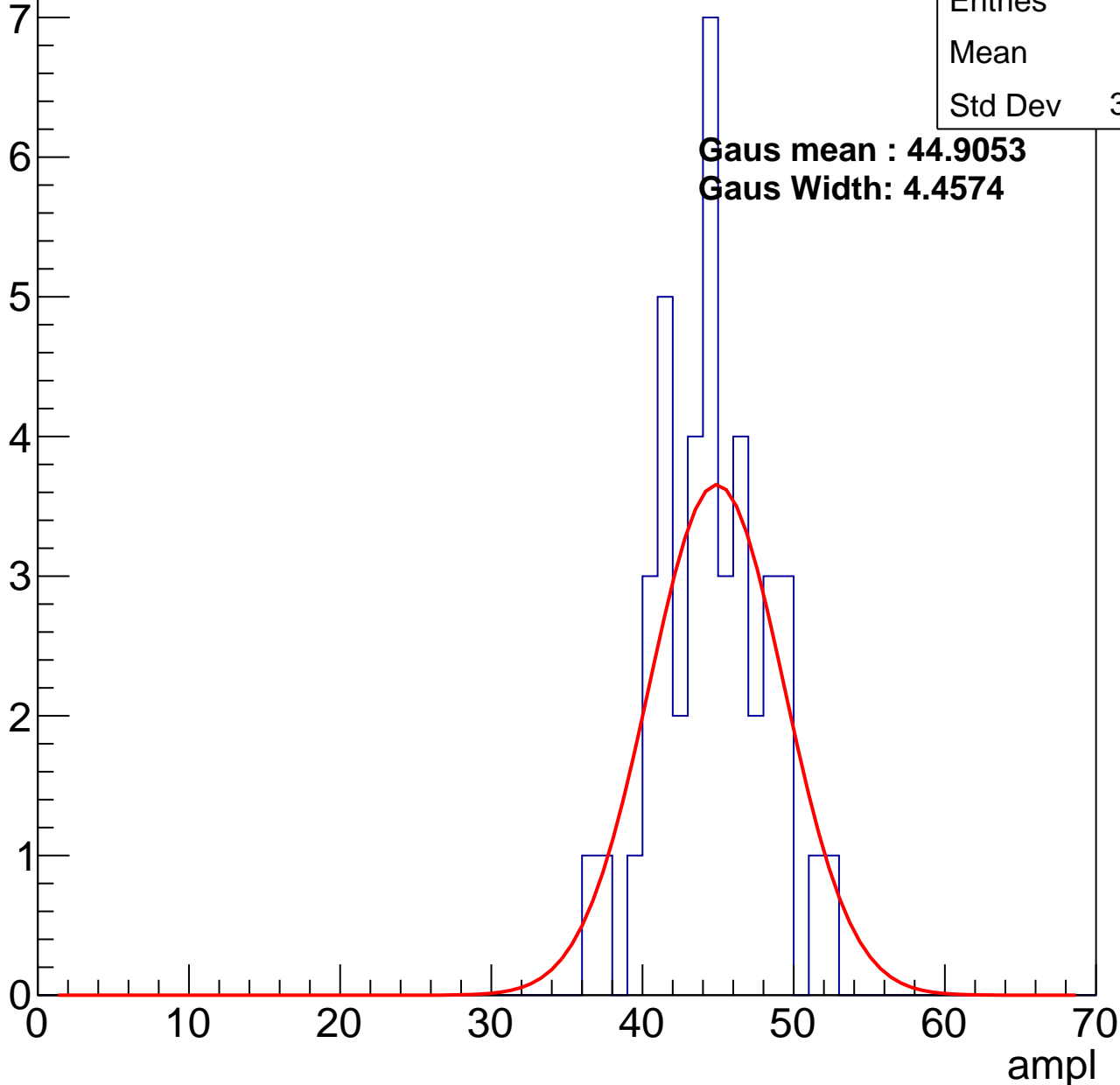
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	41
Mean	44.1
Std Dev	3.546

**Gaus mean : 44.9053**

**Gaus Width: 4.4574**

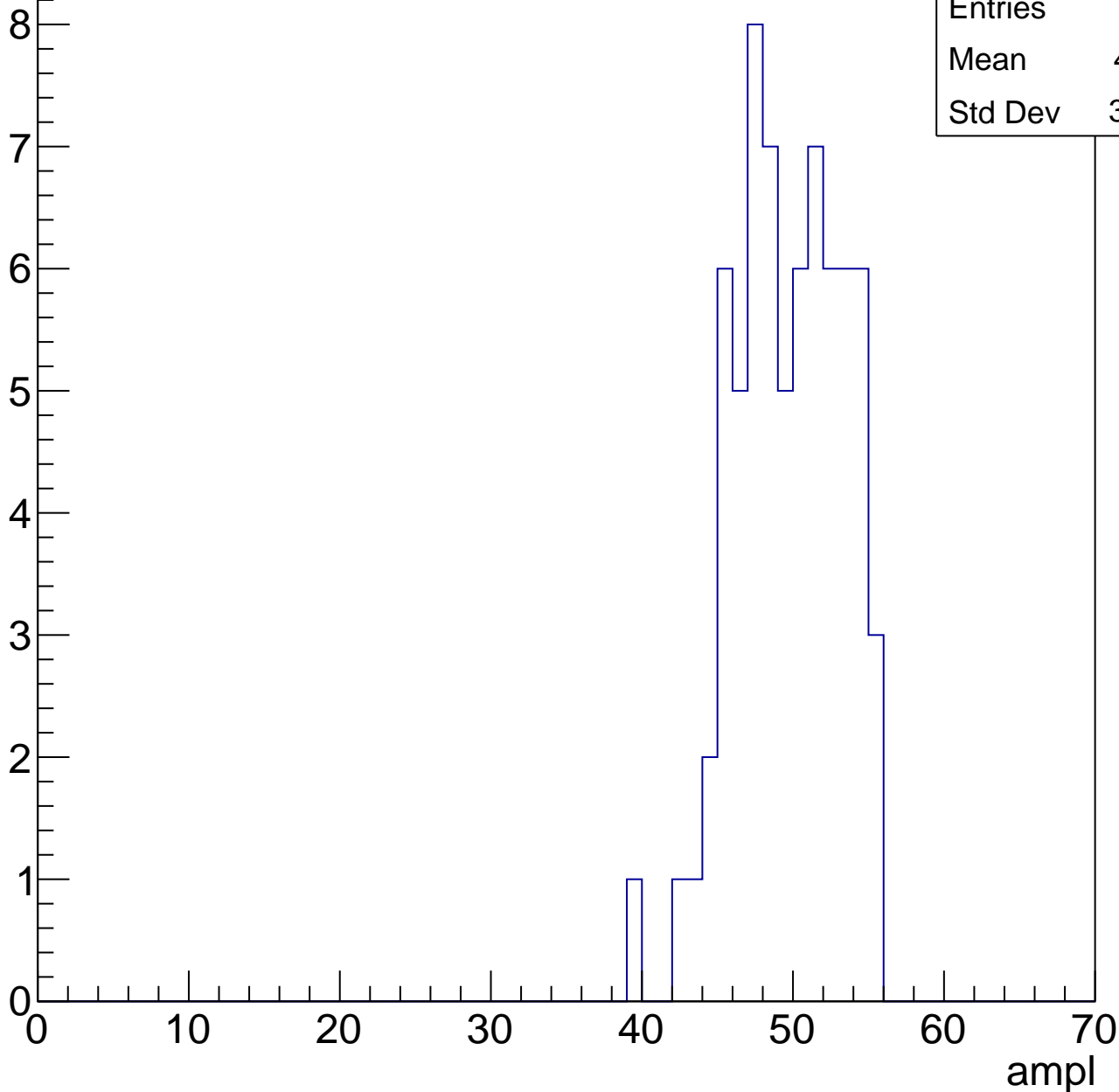


# B1L103S, U9-ch117, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

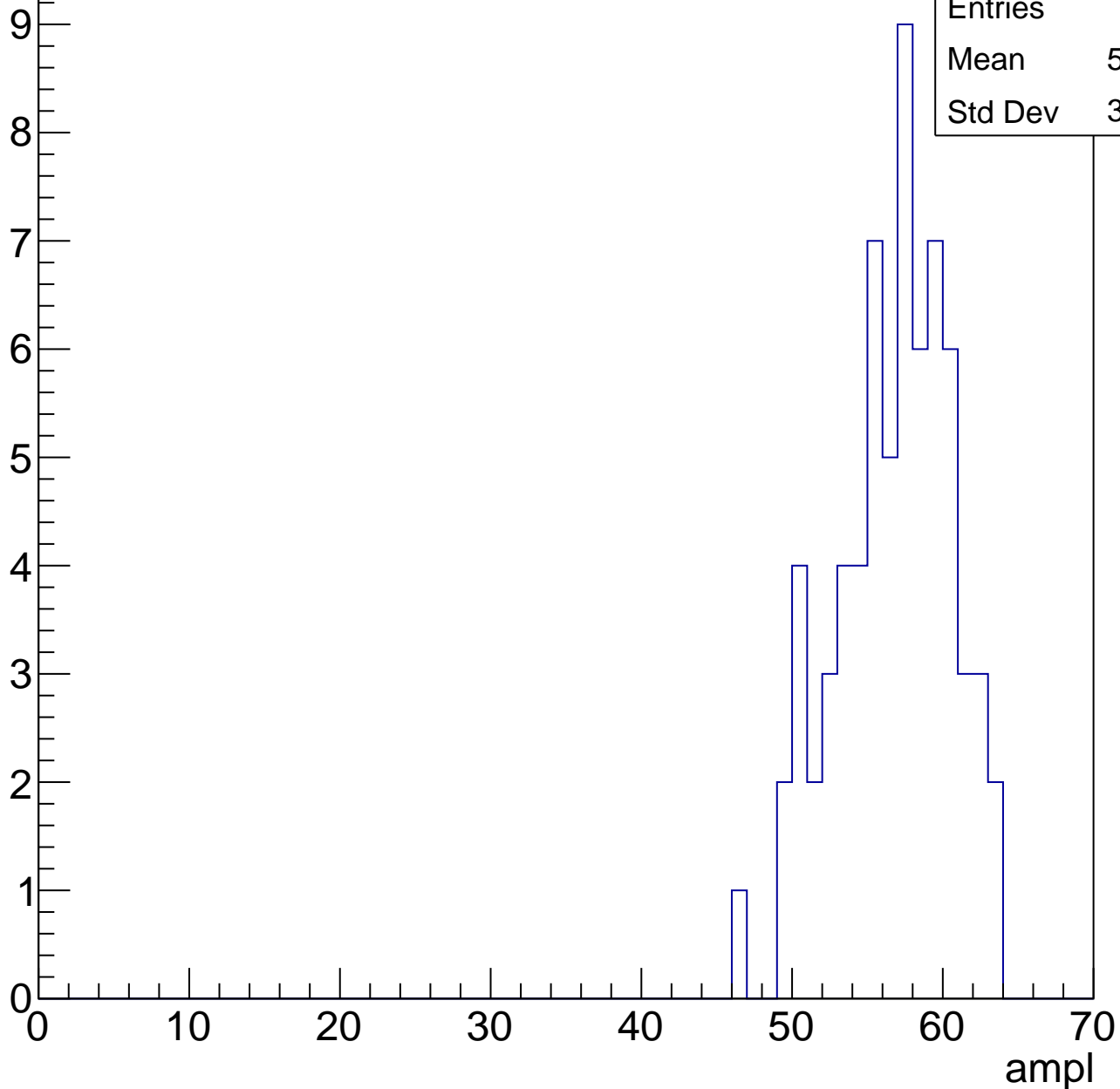
Entries	70
Mean	49.21
Std Dev	3.492



# B1L103S, U9-ch117, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



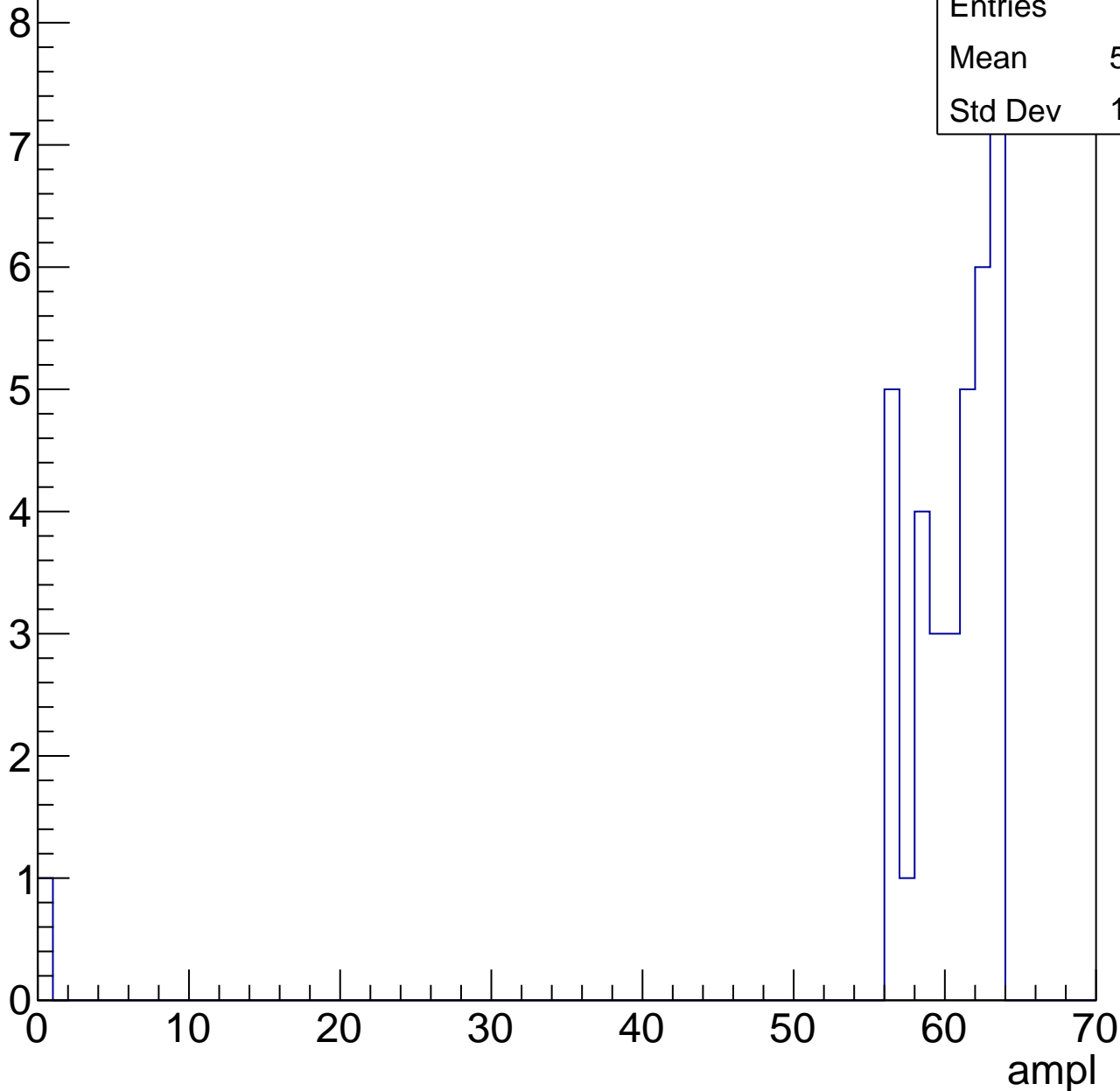
Entries	68
Mean	56.24
Std Dev	3.773

# B1L103S, U9-ch117, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

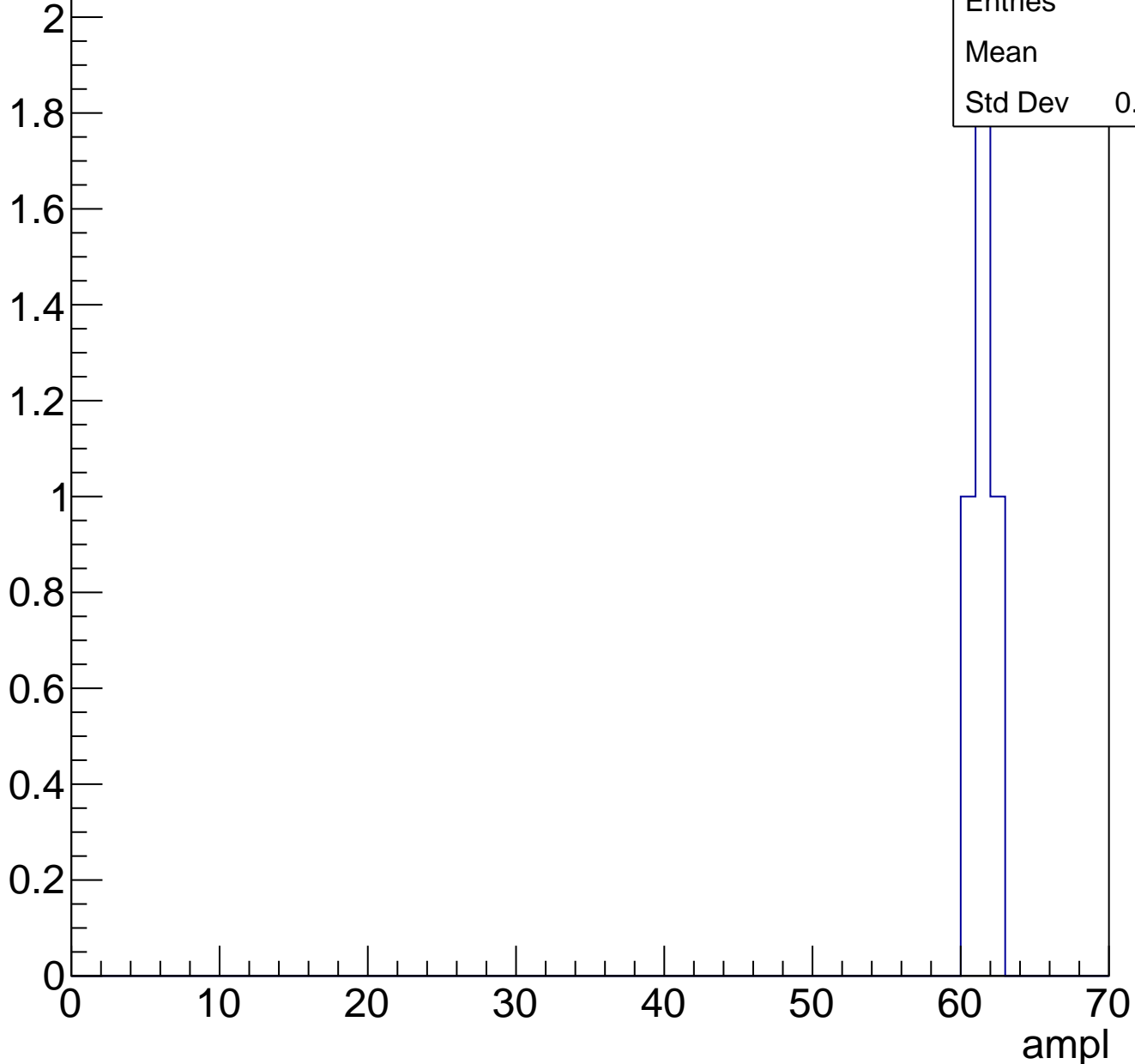
Entries	36
Mean	58.53
Std Dev	10.18



# B1L103S, U9-ch117, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	4
Mean	61
Std Dev	0.7071



# B1L103S, U9-ch117, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U9-ch118, adc0

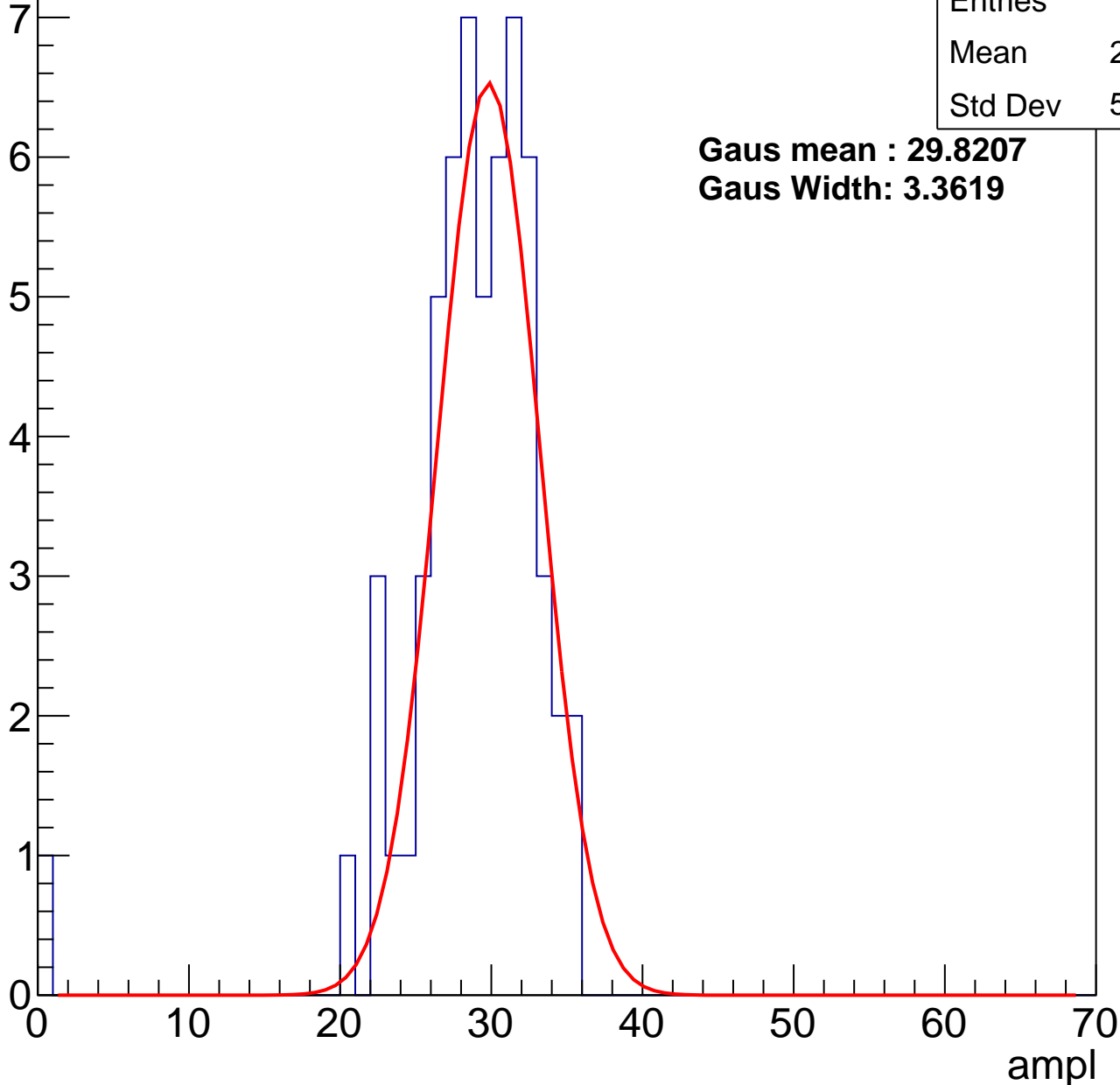
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	59
Mean	28.25
Std Dev	5.007

**Gaus mean : 29.8207**

**Gaus Width: 3.3619**



# B1L103S, U9-ch118, adc1

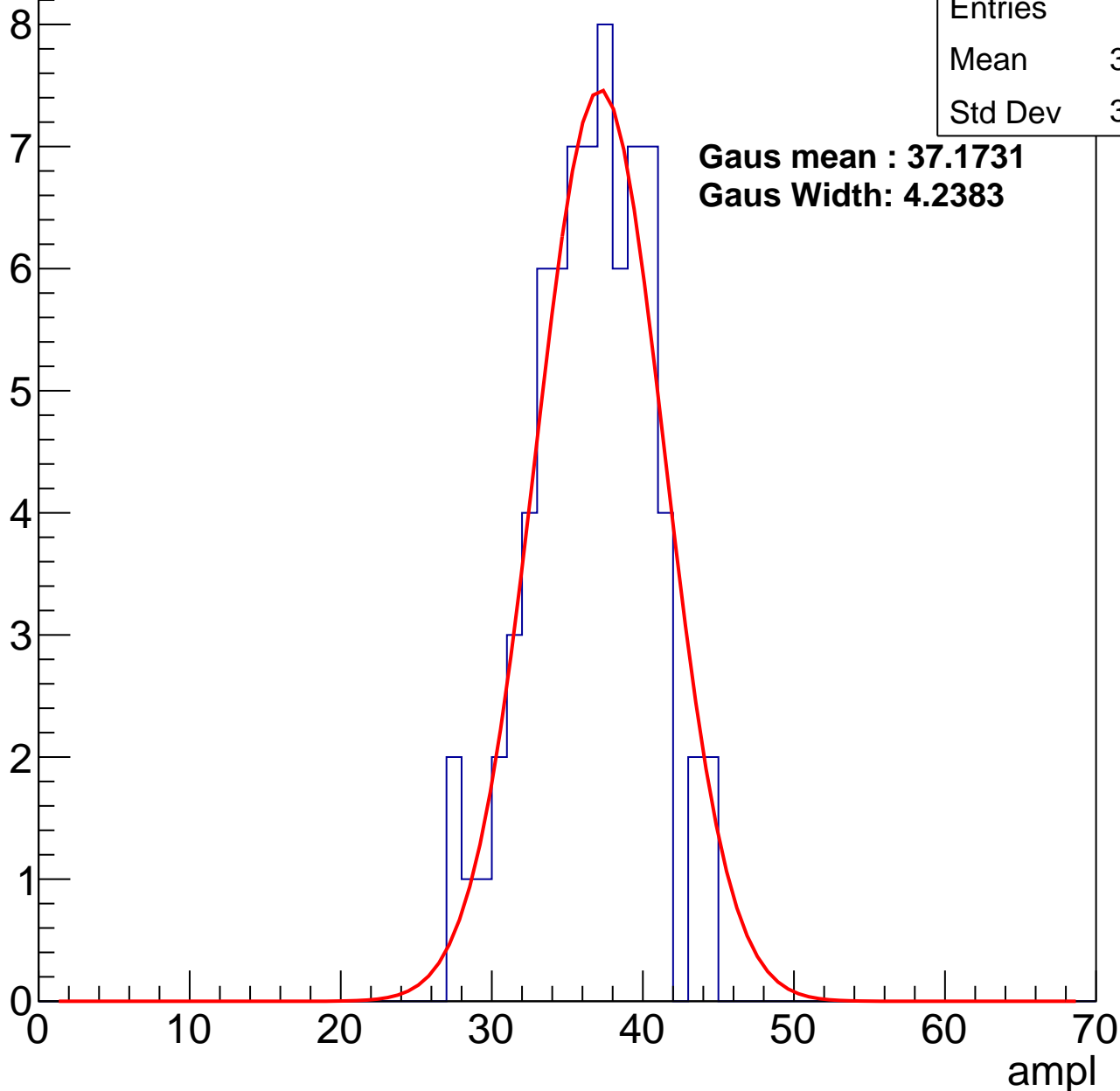
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	75
Mean	36.08
Std Dev	3.836

**Gaus mean : 37.1731**

**Gaus Width: 4.2383**



# B1L103S, U9-ch118, adc2

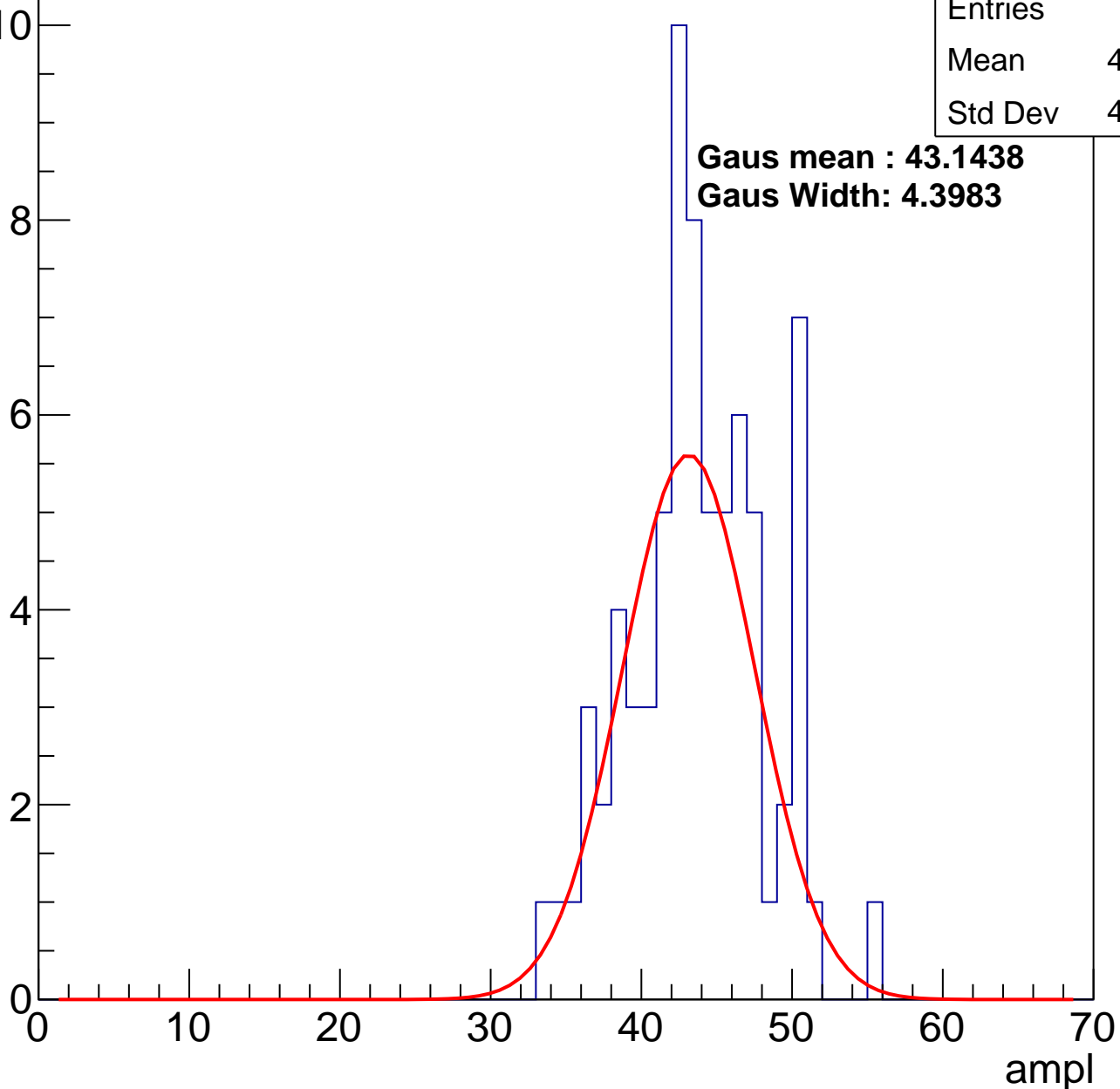
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	74
Mean	43.24
Std Dev	4.459

**Gaus mean : 43.1438**

**Gaus Width: 4.3983**

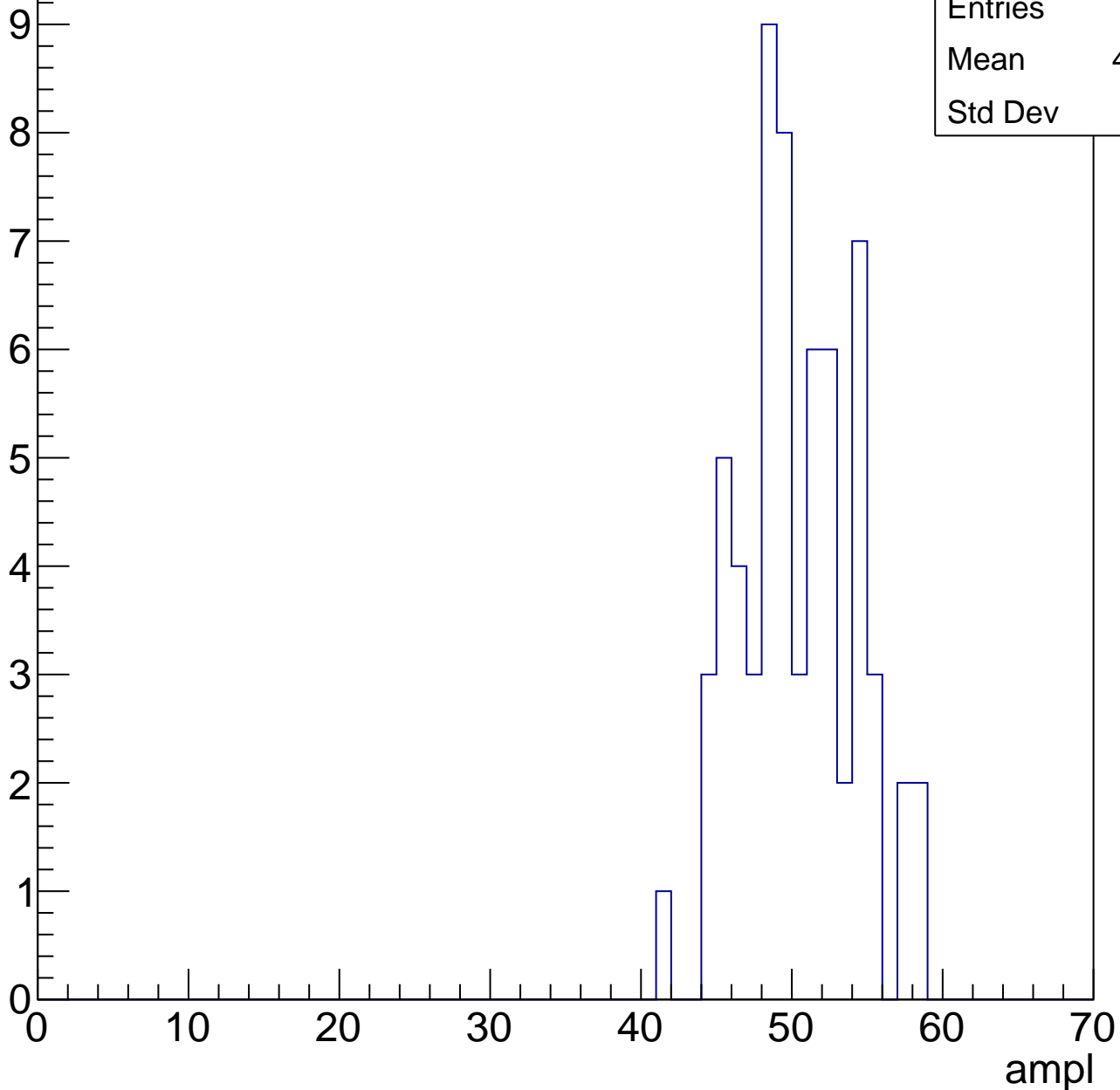


# B1L103S, U9-ch118, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	49.91
Std Dev	3.77

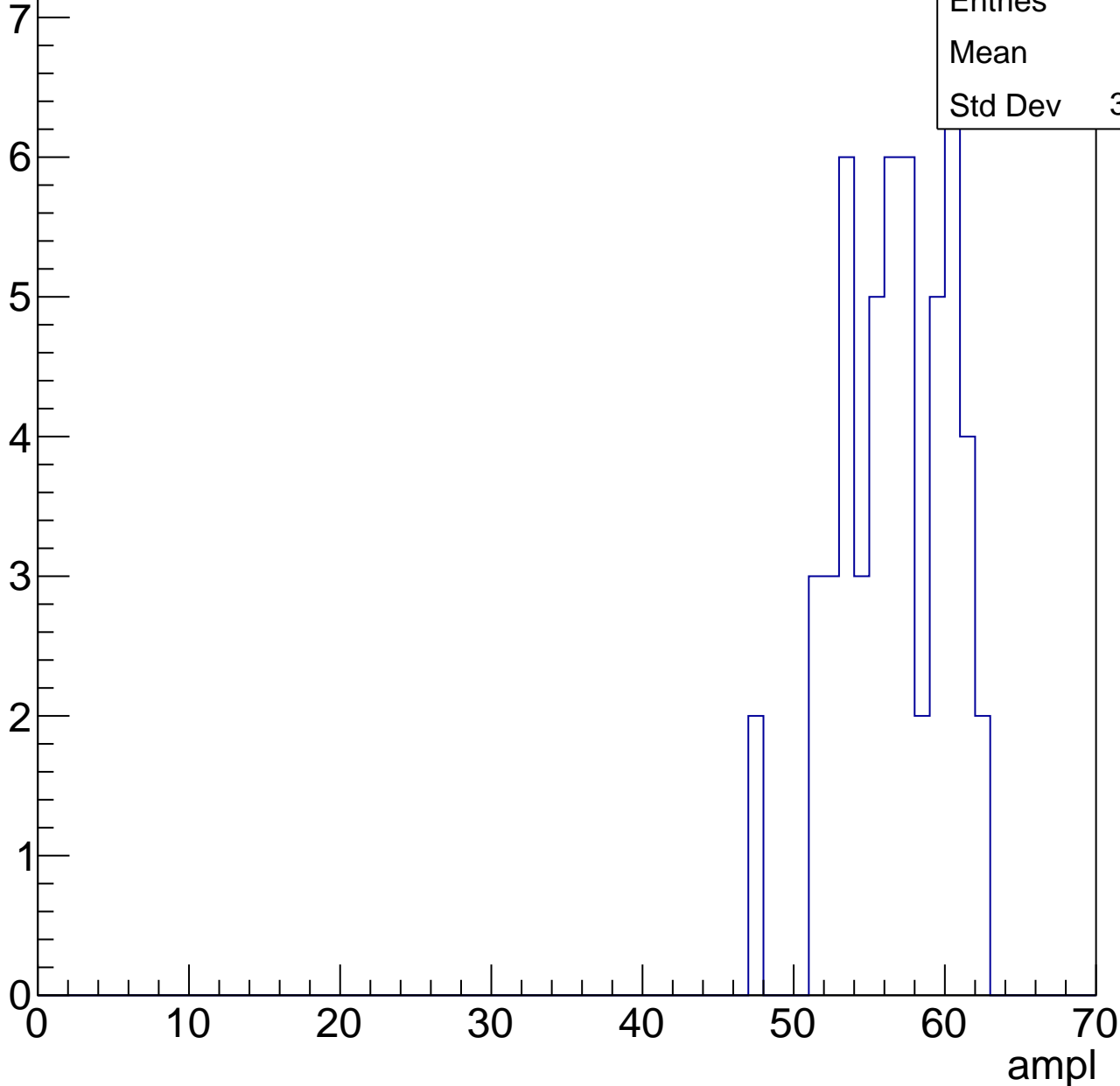


# B1L103S, U9-ch118, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	54
Mean	56.2
Std Dev	3.592

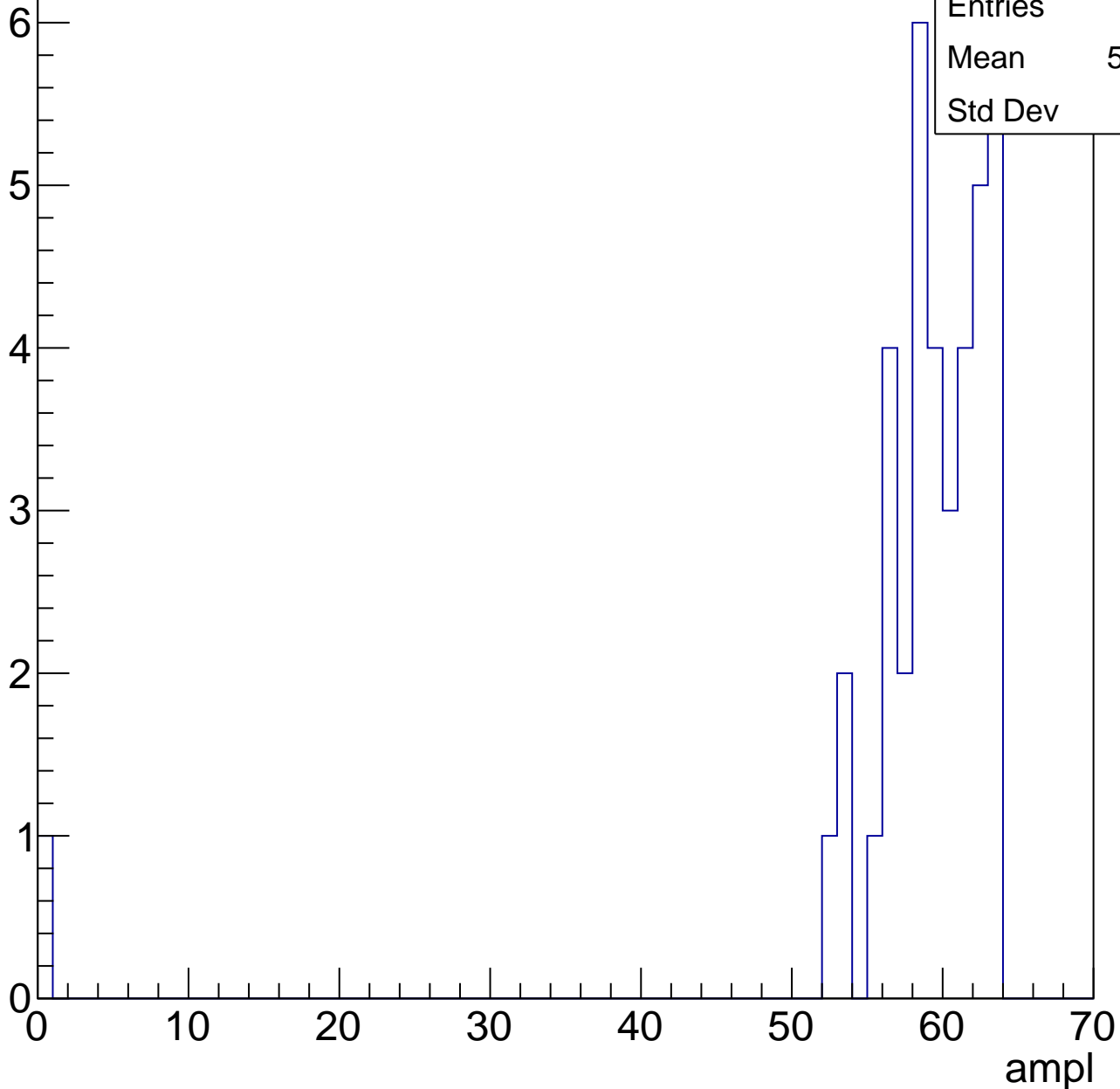


# B1L103S, U9-ch118, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

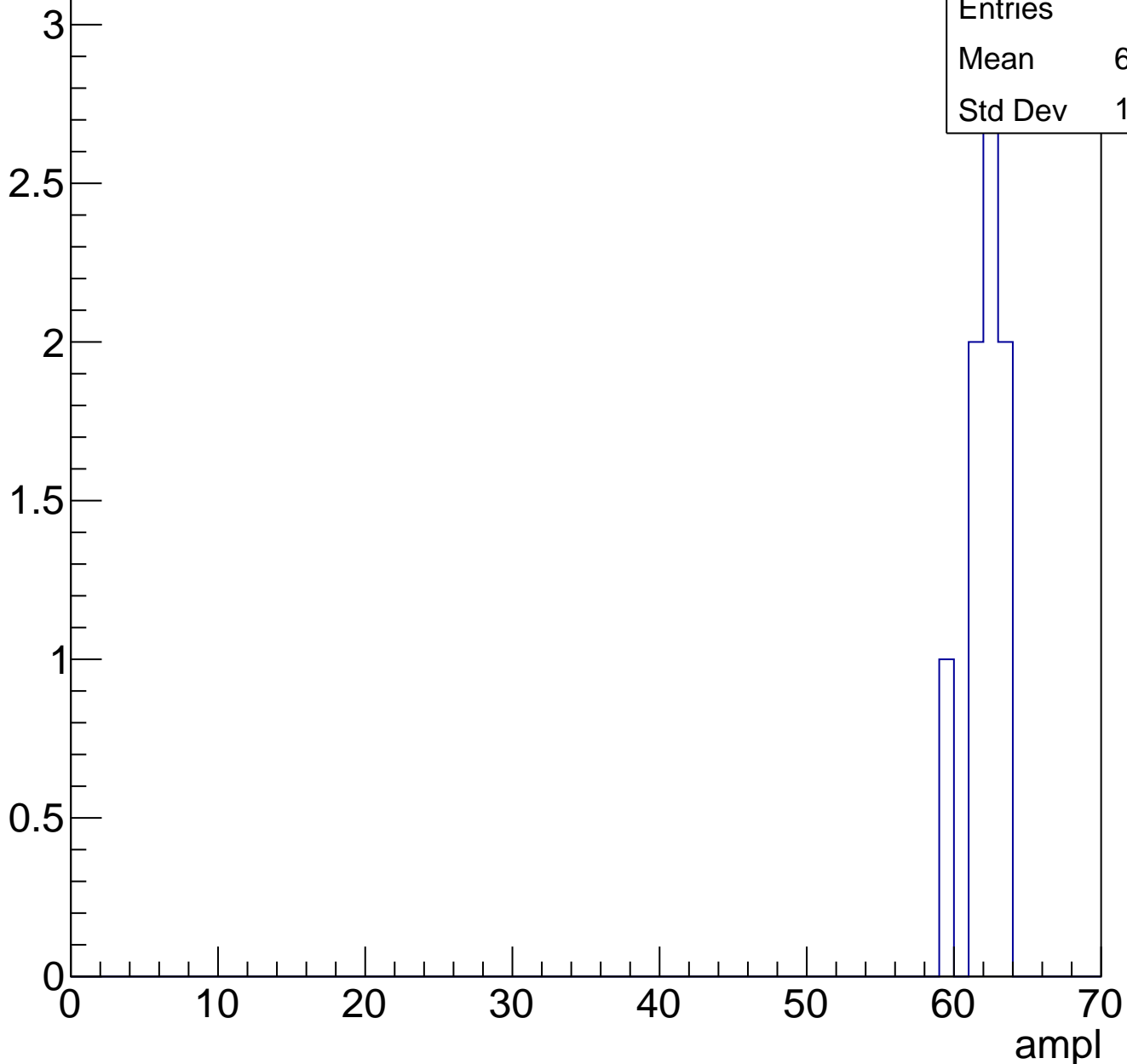
Entries	39
Mean	57.62
Std Dev	9.81



# B1L103S, U9-ch118, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U9-ch118, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U9-ch119, adc0

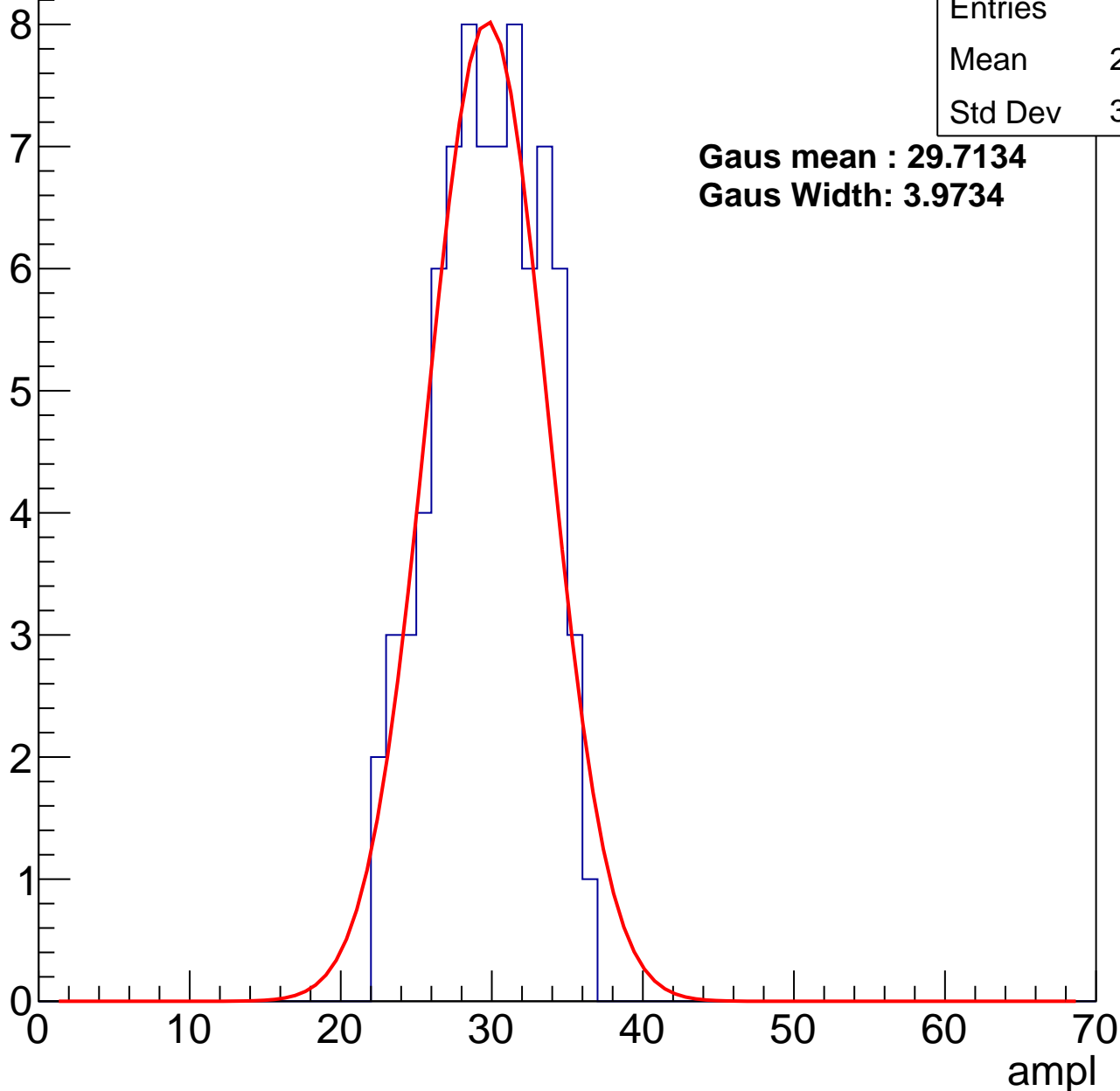
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	78
Mean	29.27
Std Dev	3.474

**Gaus mean : 29.7134**

**Gaus Width: 3.9734**



# B1L103S, U9-ch119, adc1

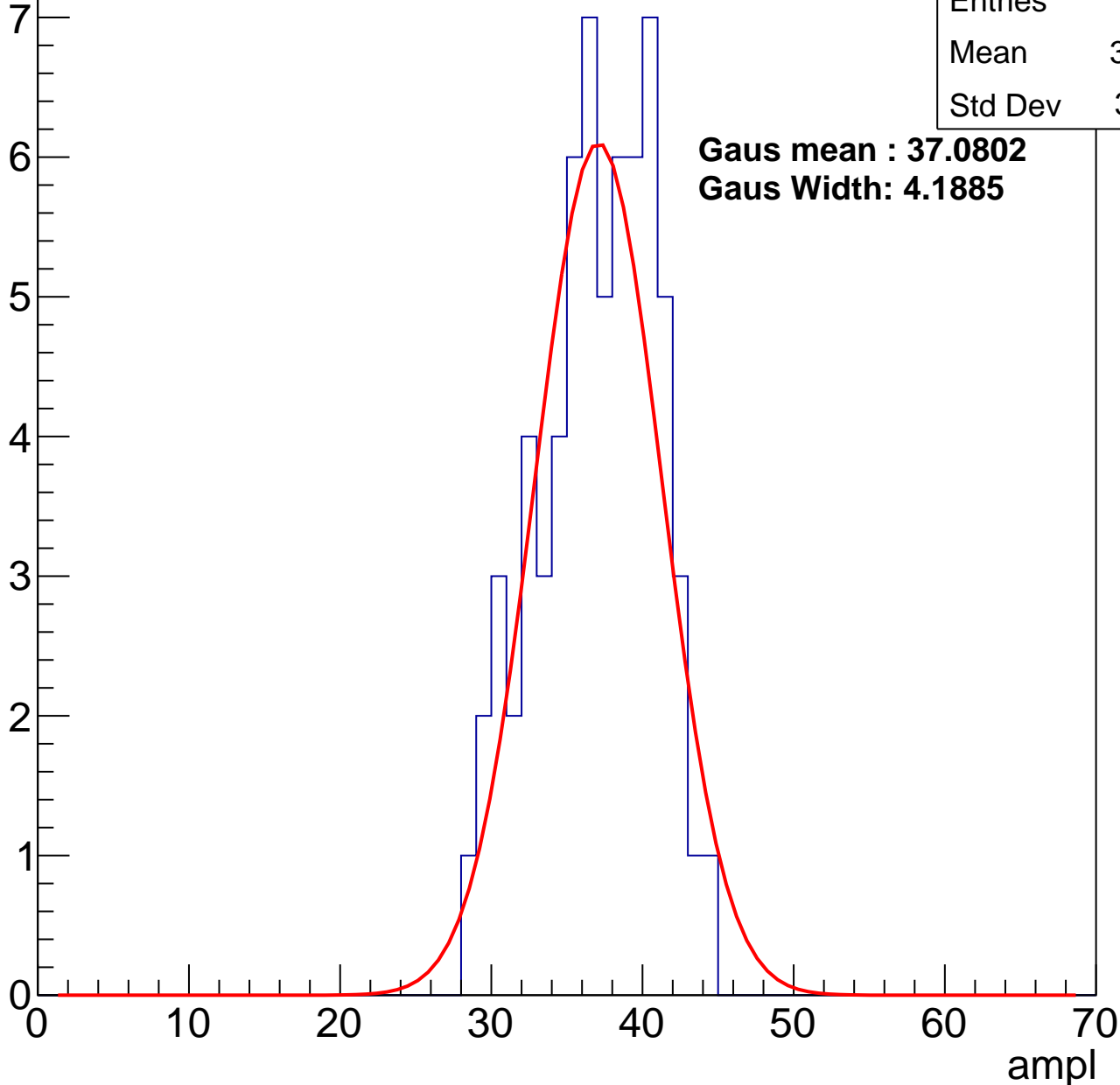
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	36.48
Std Dev	3.811

**Gaus mean : 37.0802**

**Gaus Width: 4.1885**



# B1L103S, U9-ch119, adc2

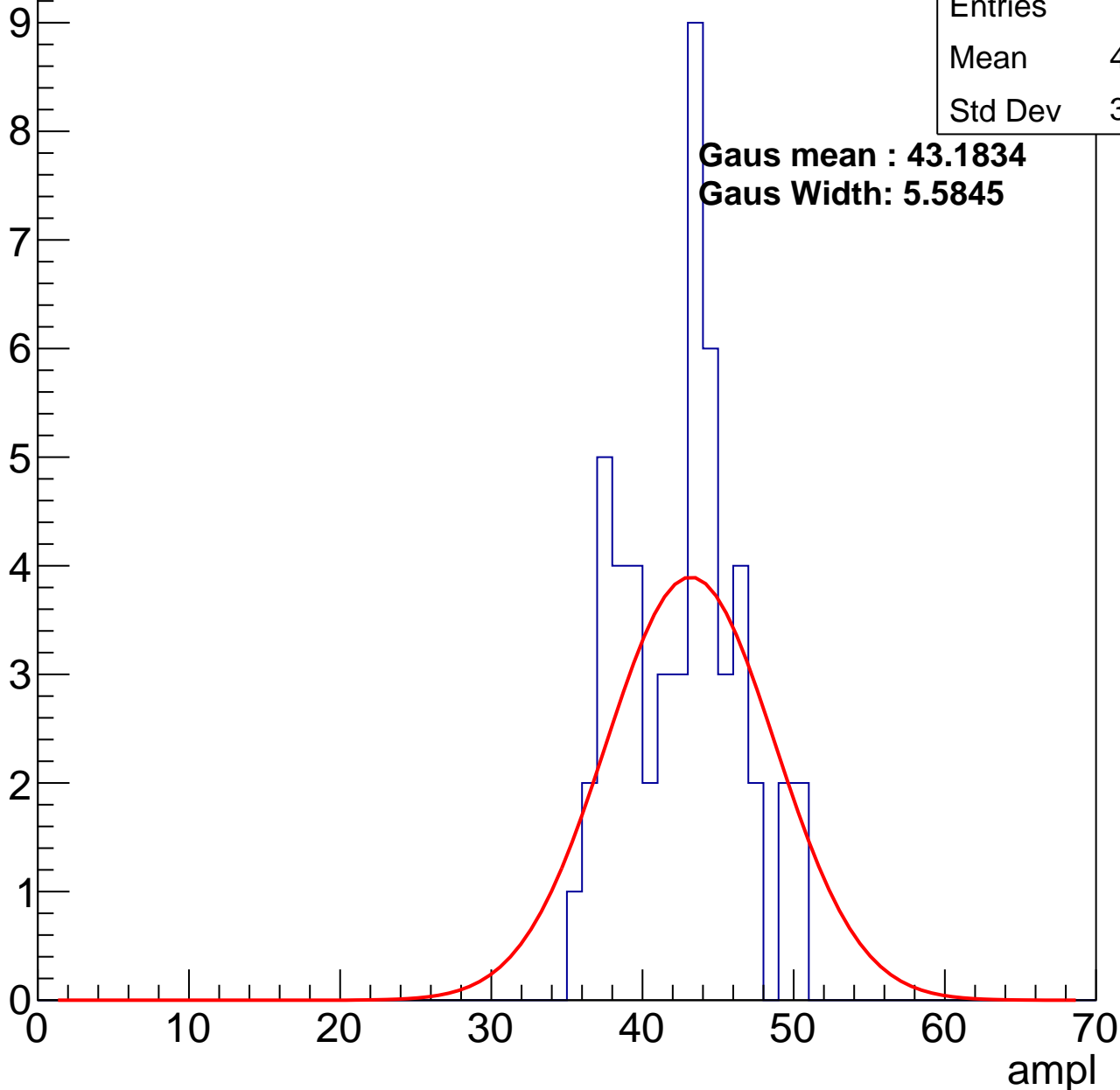
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	52
Mean	42.13
Std Dev	3.813

**Gaus mean : 43.1834**

**Gaus Width: 5.5845**

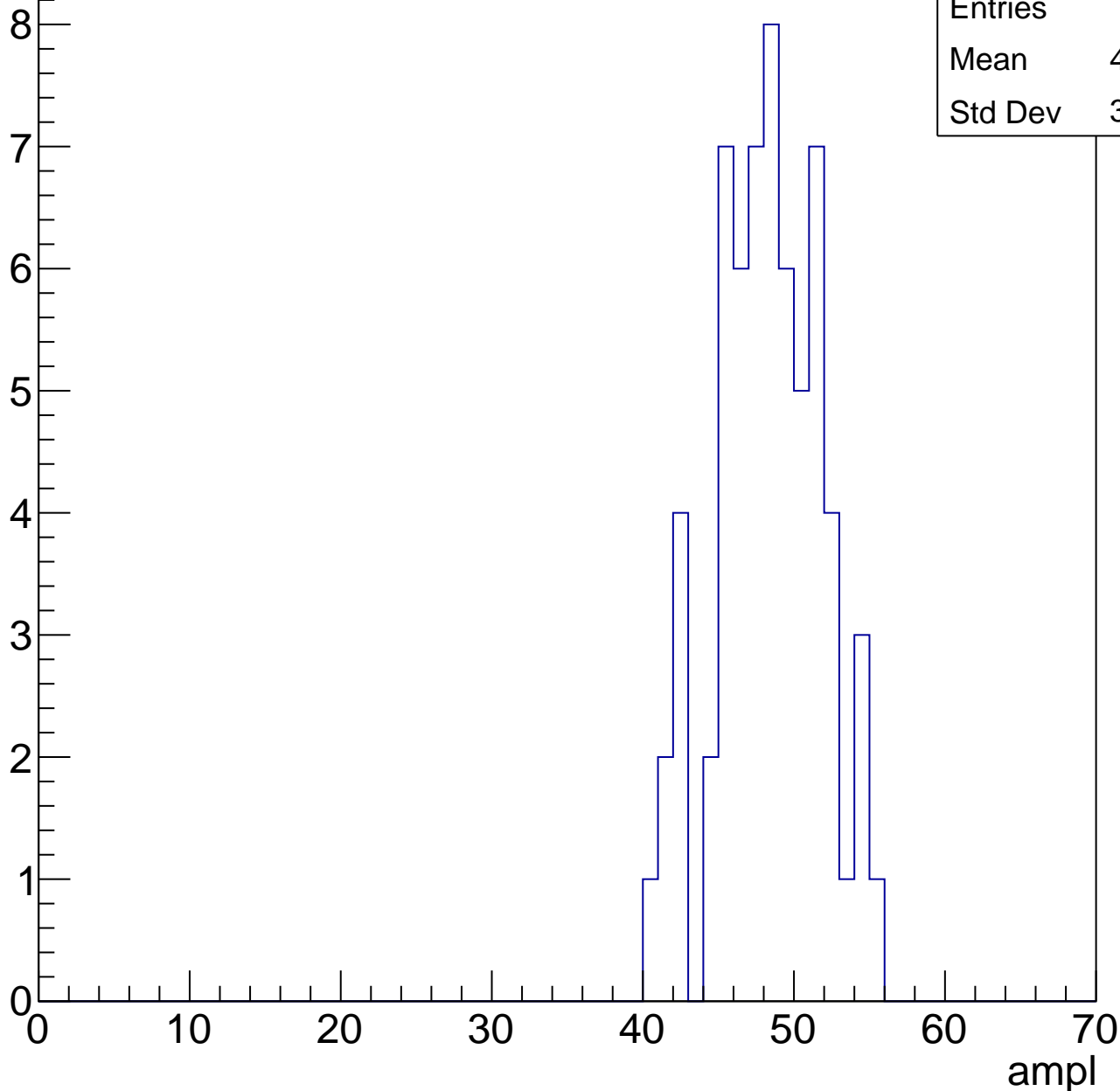


# B1L103S, U9-ch119, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	47.83
Std Dev	3.458

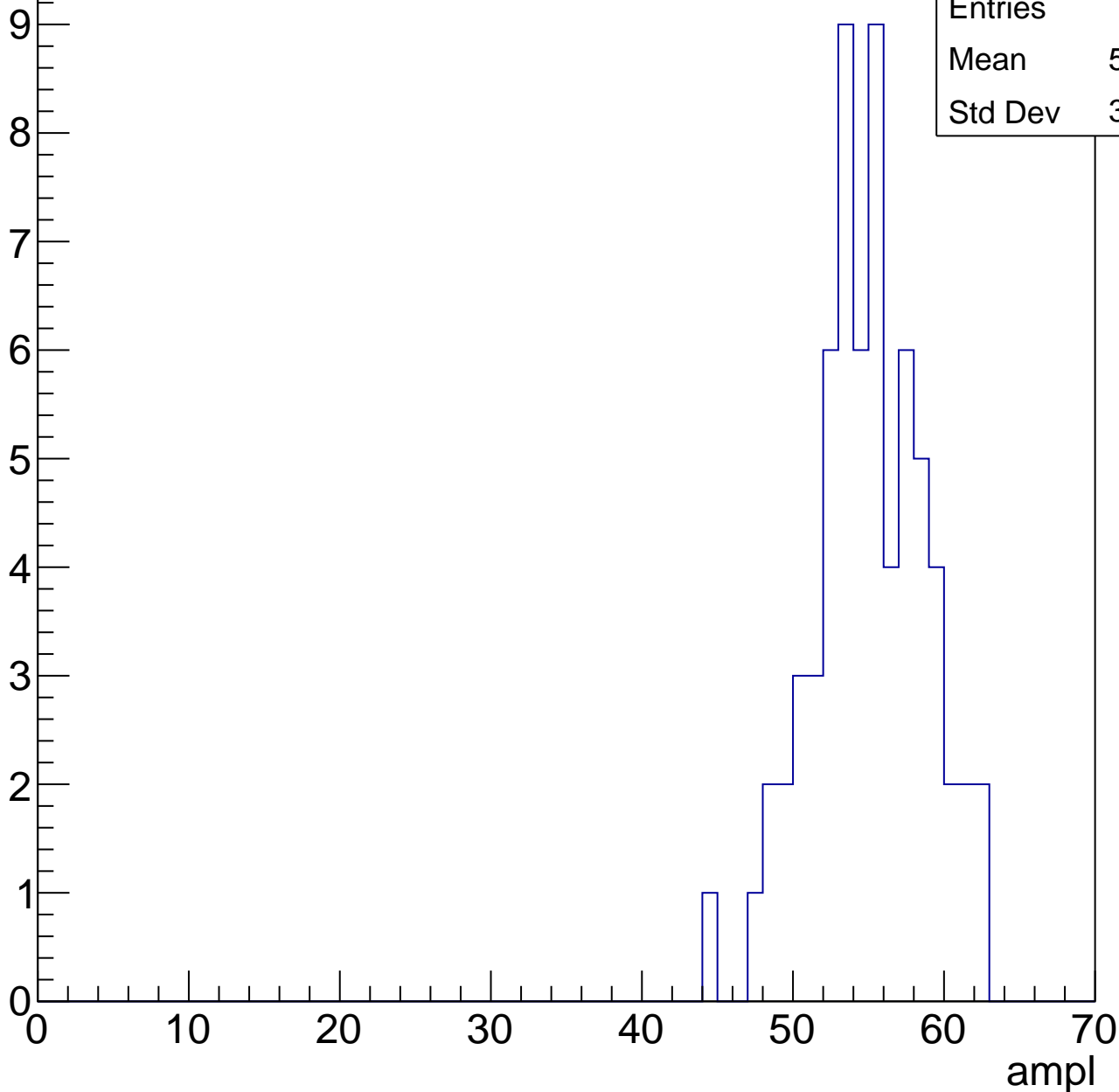


# B1L103S, U9-ch119, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	54.54
Std Dev	3.699

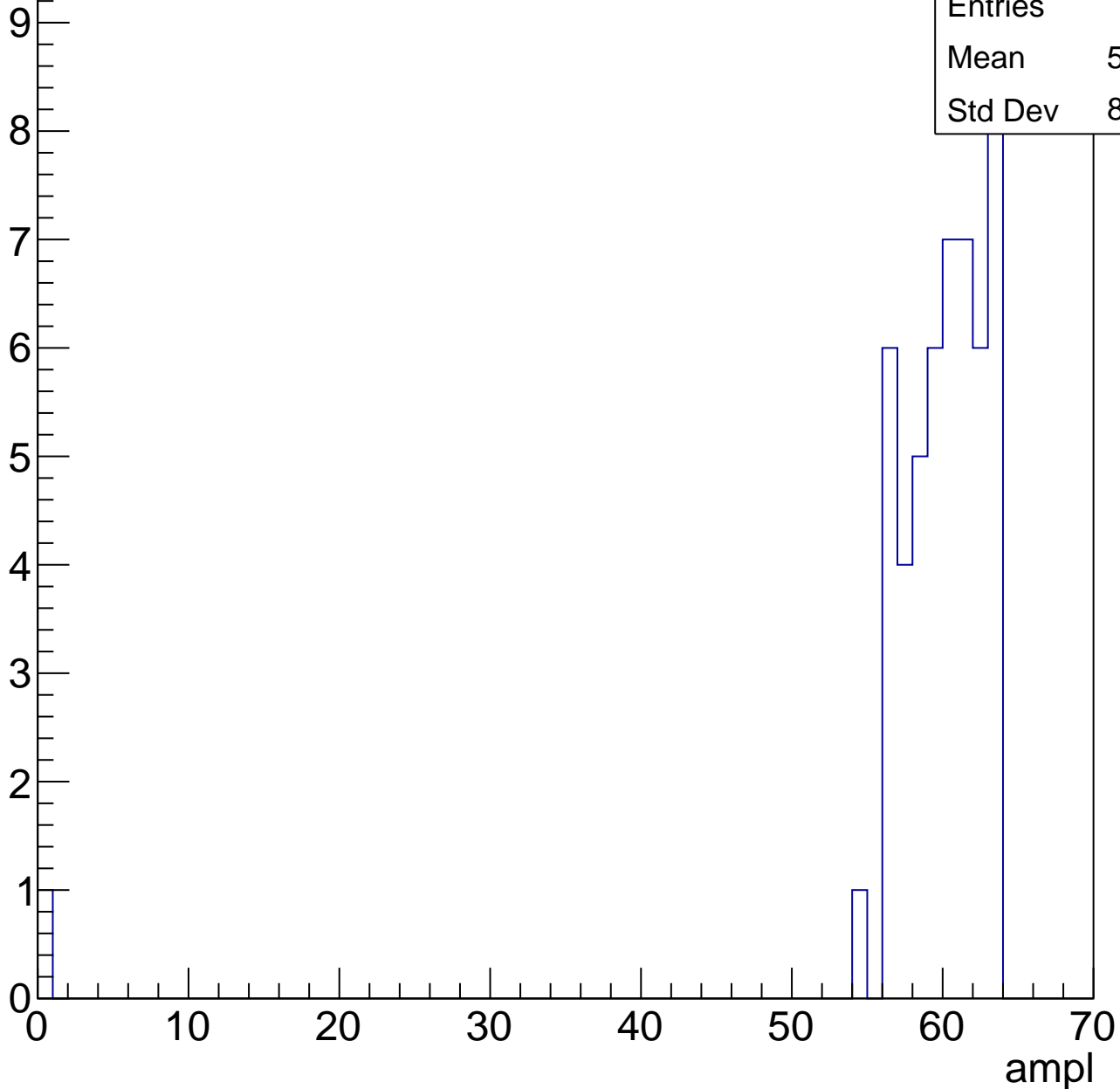


# B1L103S, U9-ch119, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	52
Mean	58.62
Std Dev	8.556



# B1L103S, U9-ch119, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	5
Mean	61.6
Std Dev	1.02



# B1L103S, U9-ch119, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U9-ch120, adc0

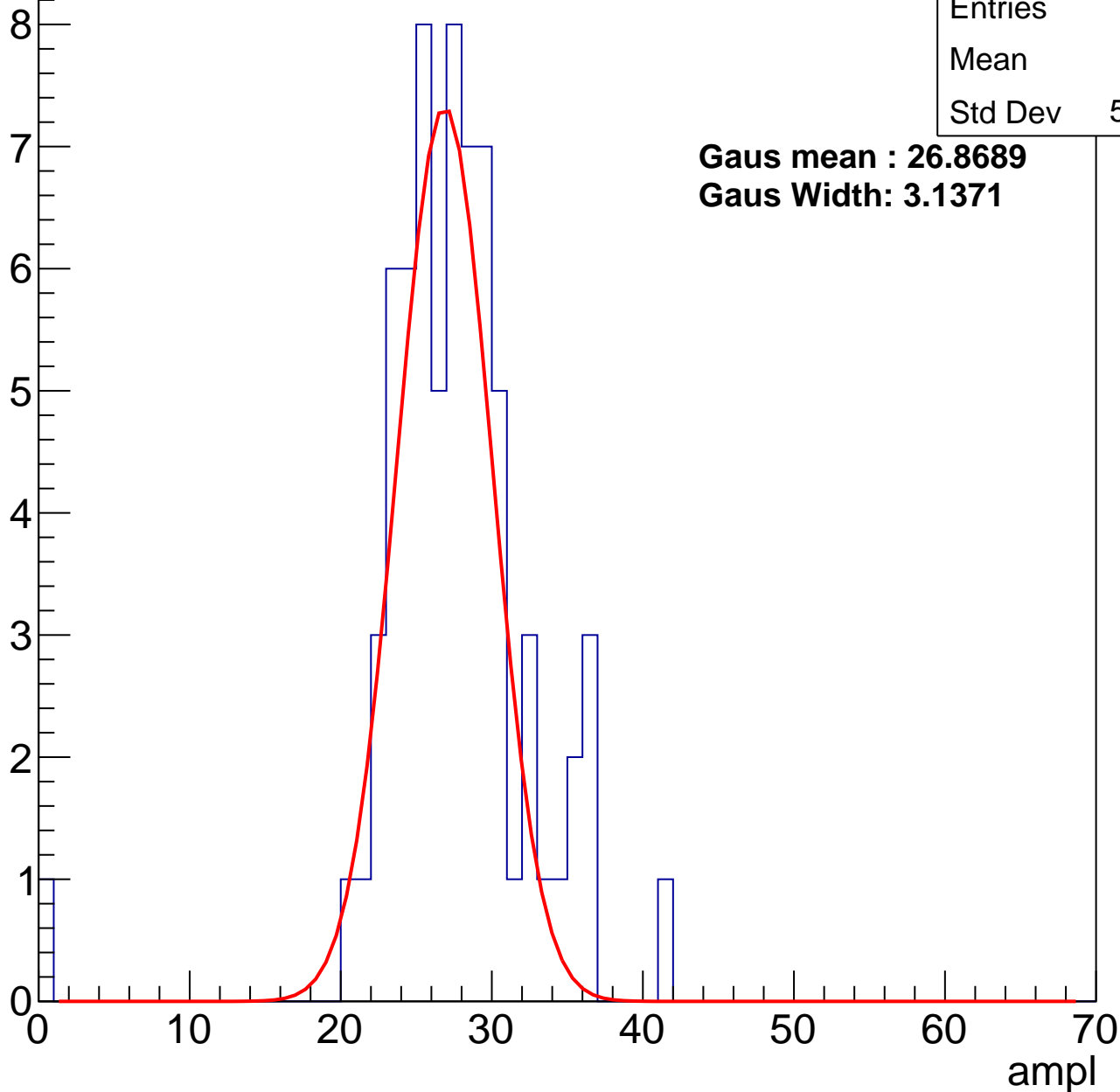
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	70
Mean	27.1
Std Dev	5.208

**Gaus mean : 26.8689**

**Gaus Width: 3.1371**



# B1L103S, U9-ch120, adc1

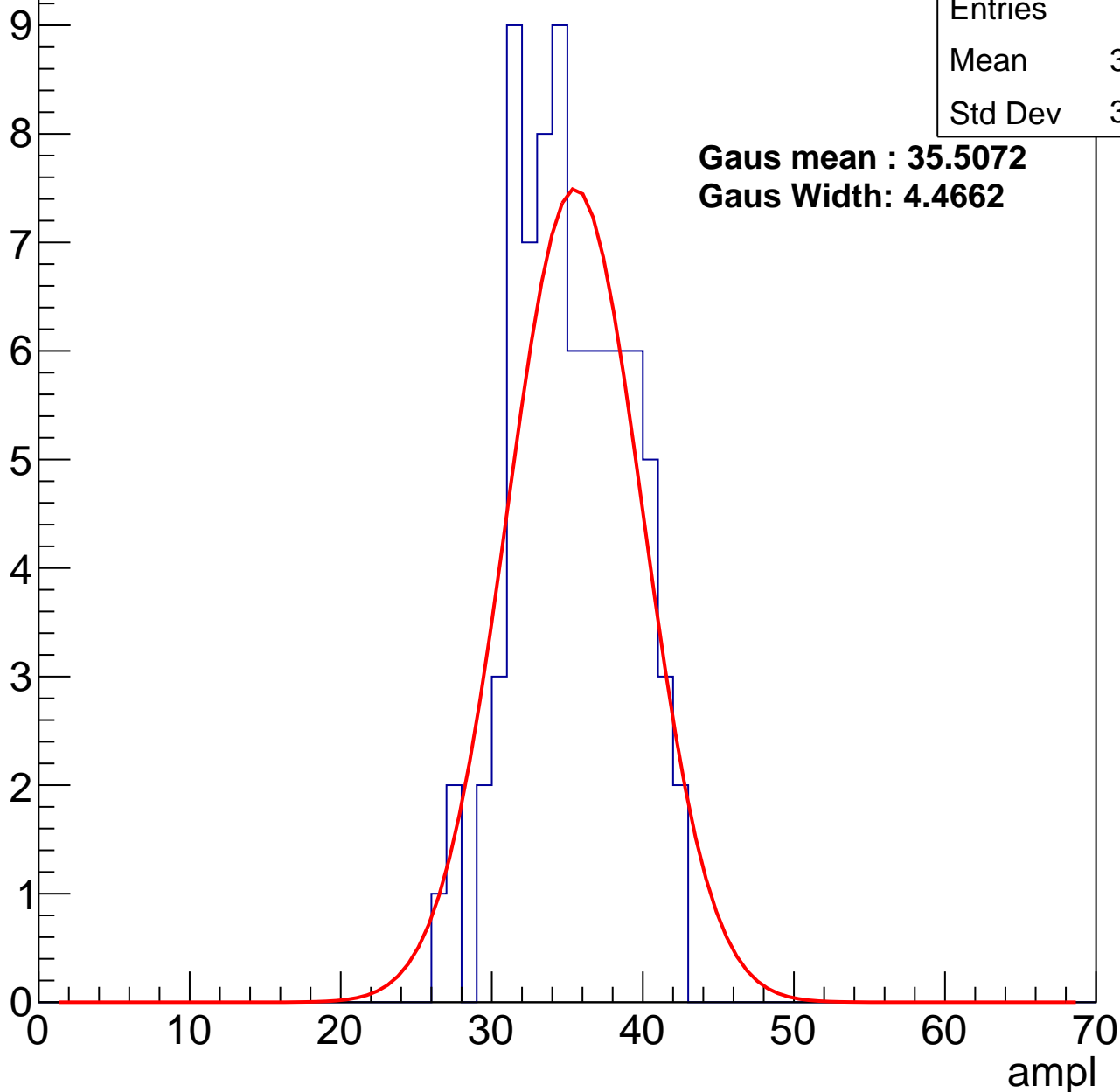
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	81
Mean	34.79
Std Dev	3.704

**Gaus mean : 35.5072**

**Gaus Width: 4.4662**



# B1L103S, U9-ch120, adc2

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	38
Mean	40.47
Std Dev	3.37

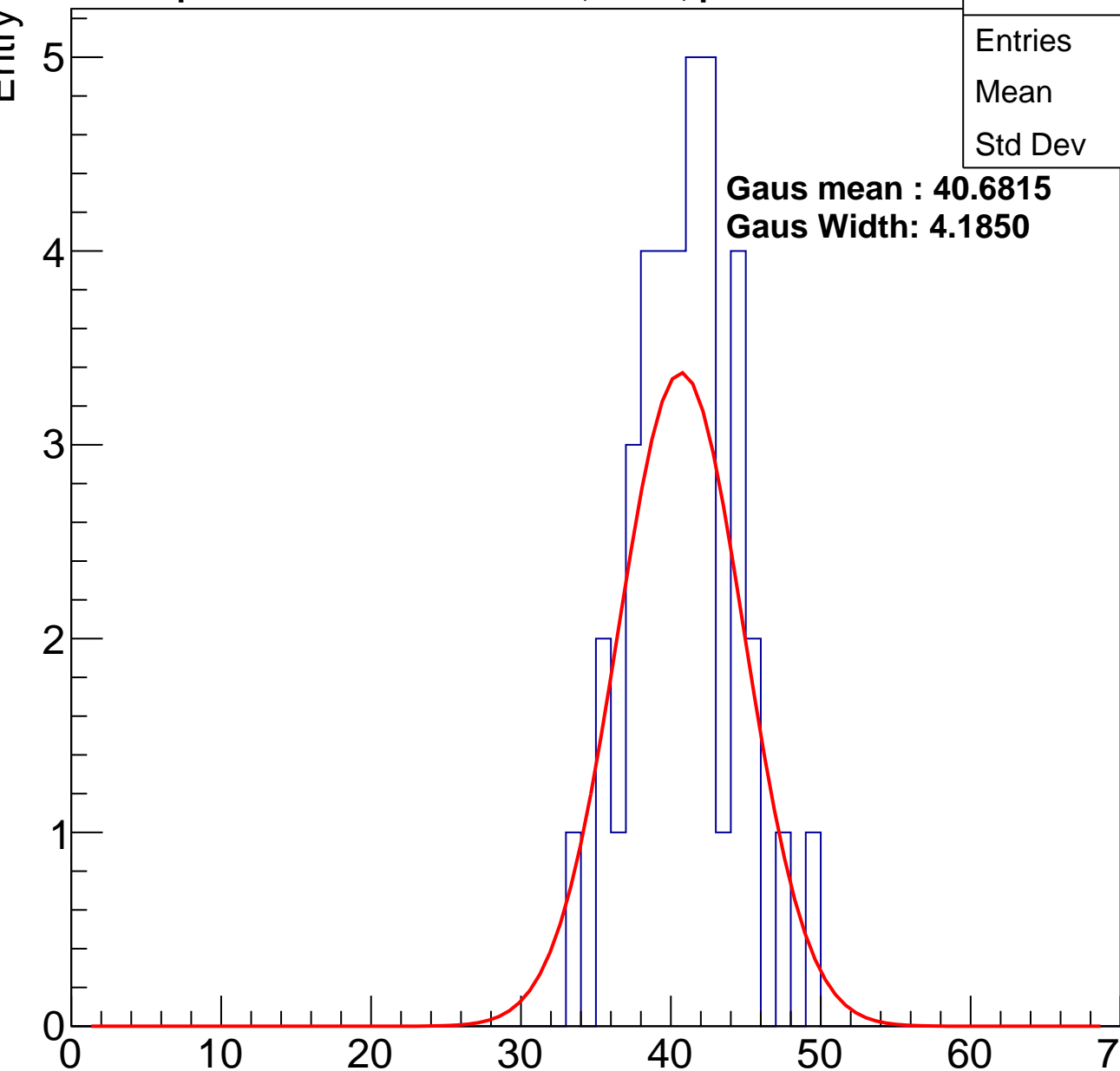
**Gaus mean : 40.6815**

**Gaus Width: 4.1850**

5  
4  
3  
2  
1  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U9-ch120, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

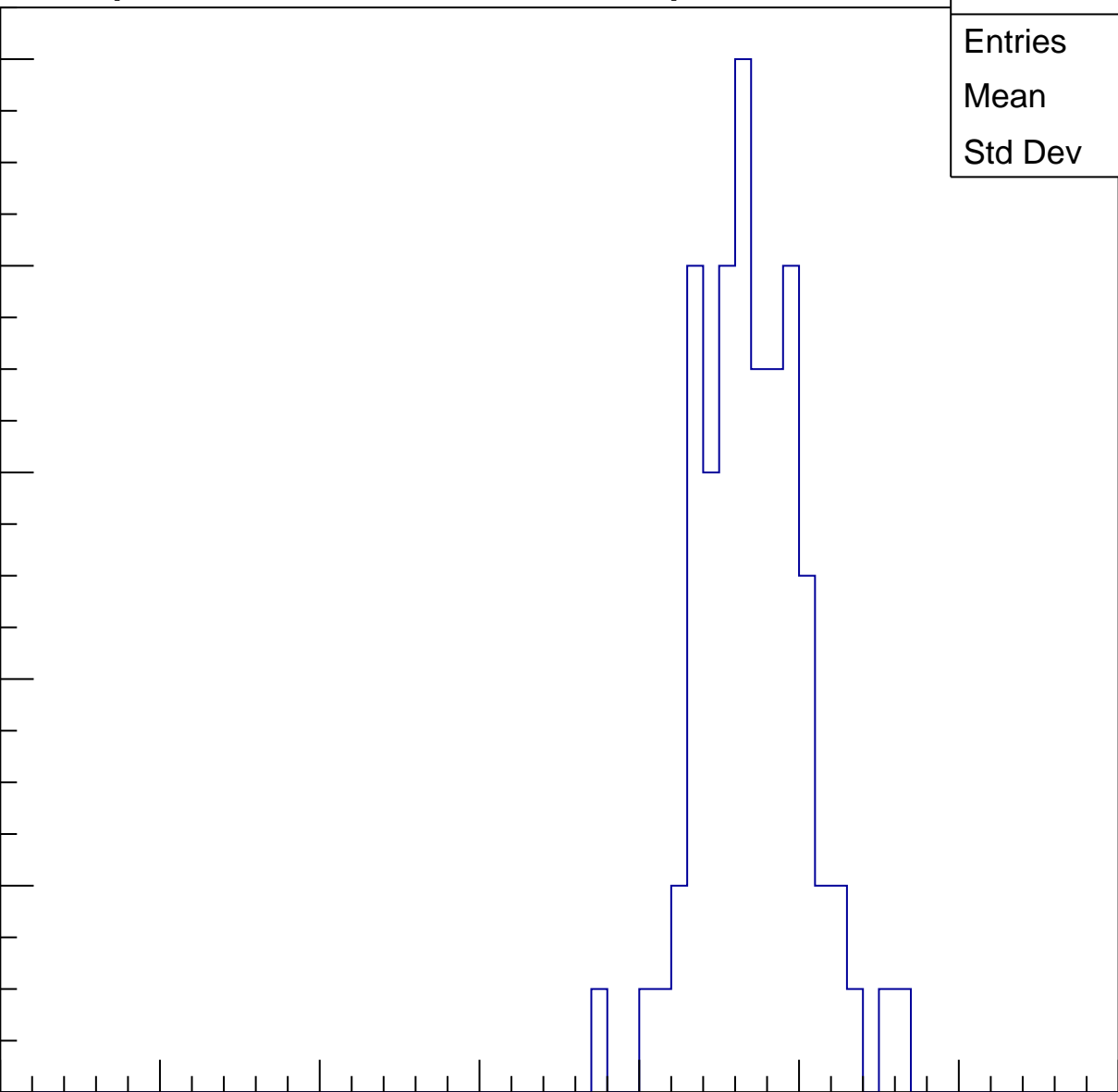
Entries	71
Mean	46.58
Std Dev	3.343

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

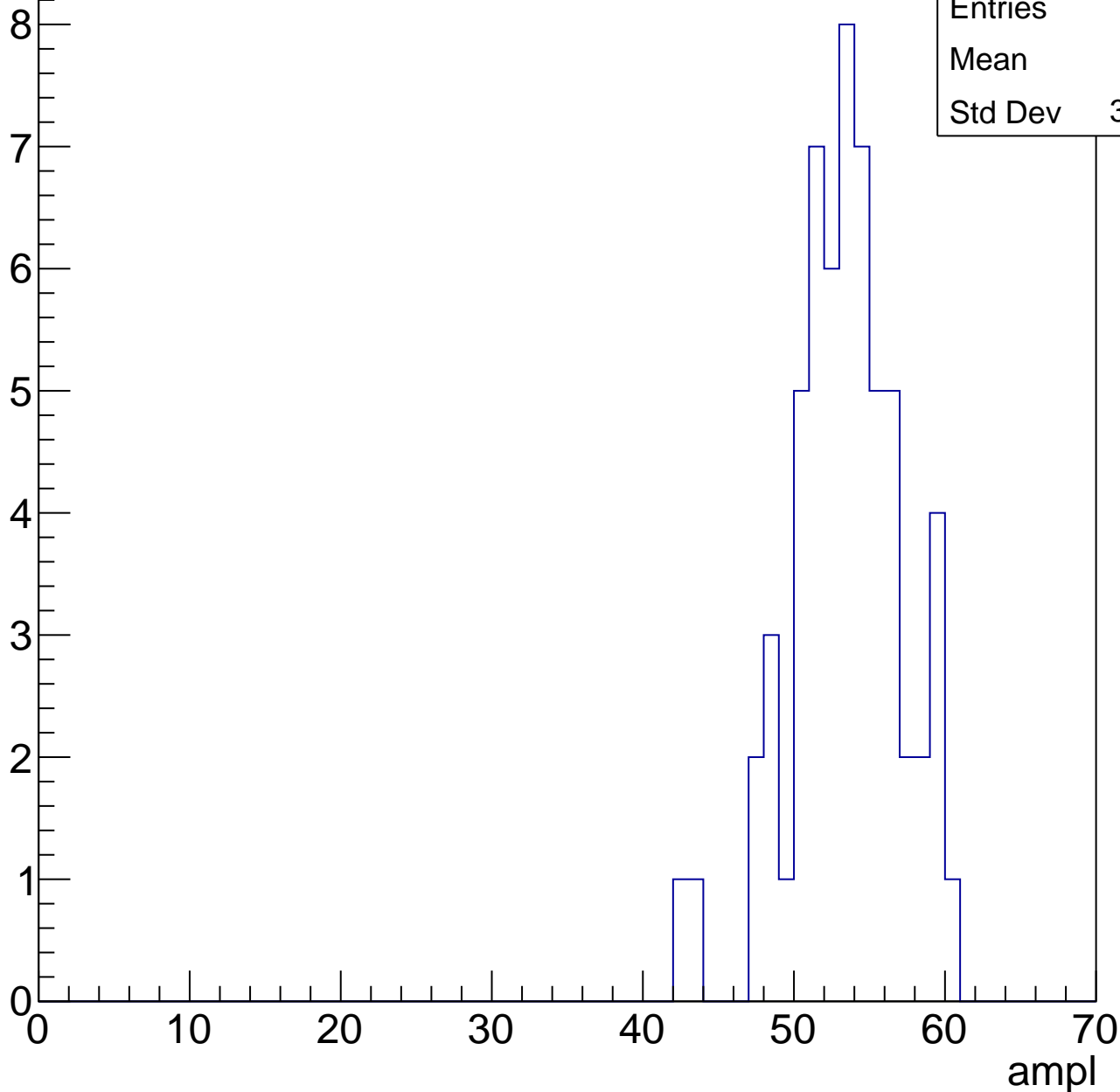


# B1L103S, U9-ch120, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	60
Mean	52.9
Std Dev	3.673

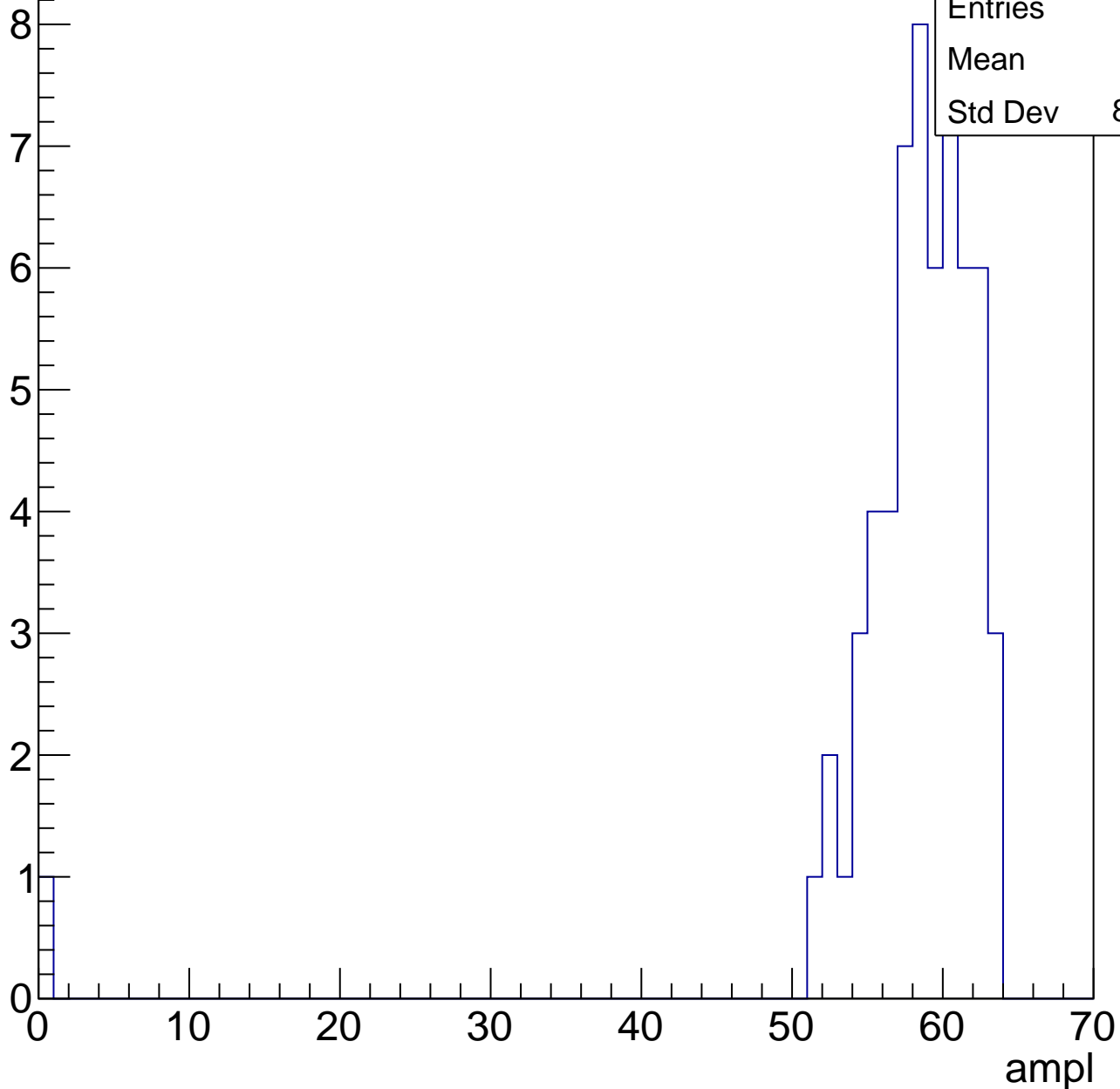


# B1L103S, U9-ch120, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	60
Mean	57.3
Std Dev	8.011

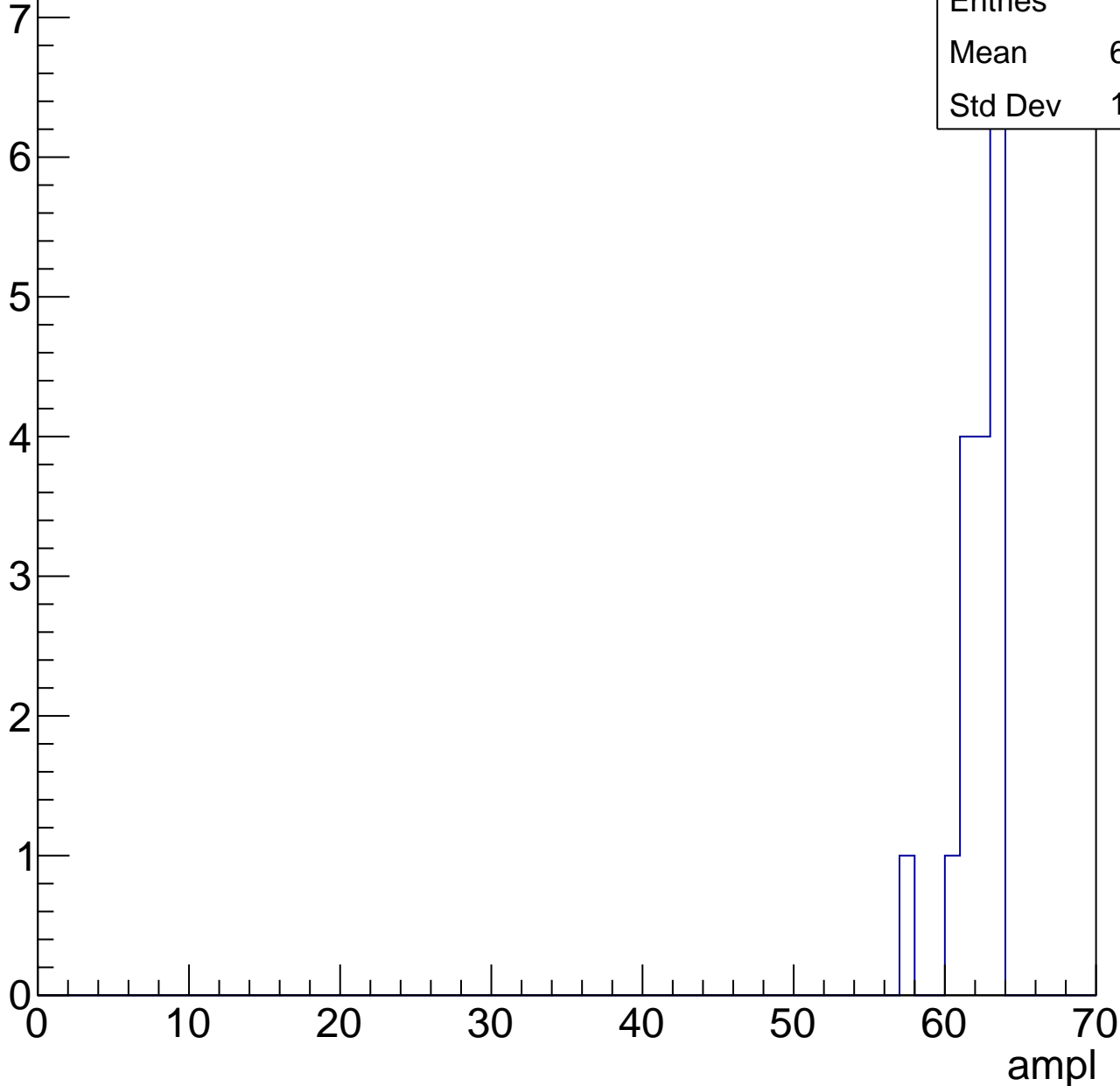


# B1L103S, U9-ch120, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	17
Mean	61.76
Std Dev	1.516





# B1L103S, U9-ch120, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L103S, U9-ch121, adc0

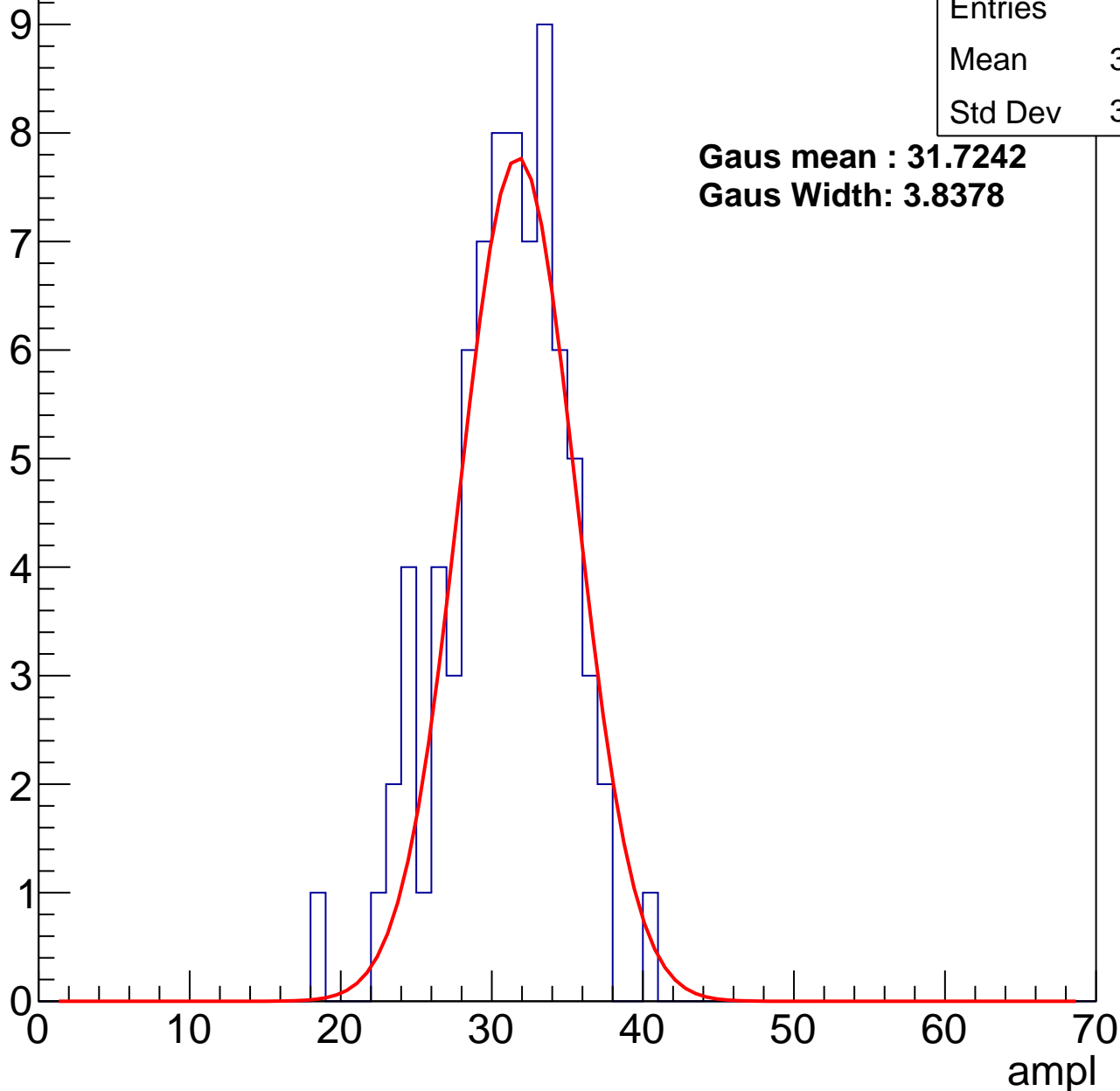
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	78
Mean	30.42
Std Dev	3.966

**Gaus mean : 31.7242**

**Gaus Width: 3.8378**



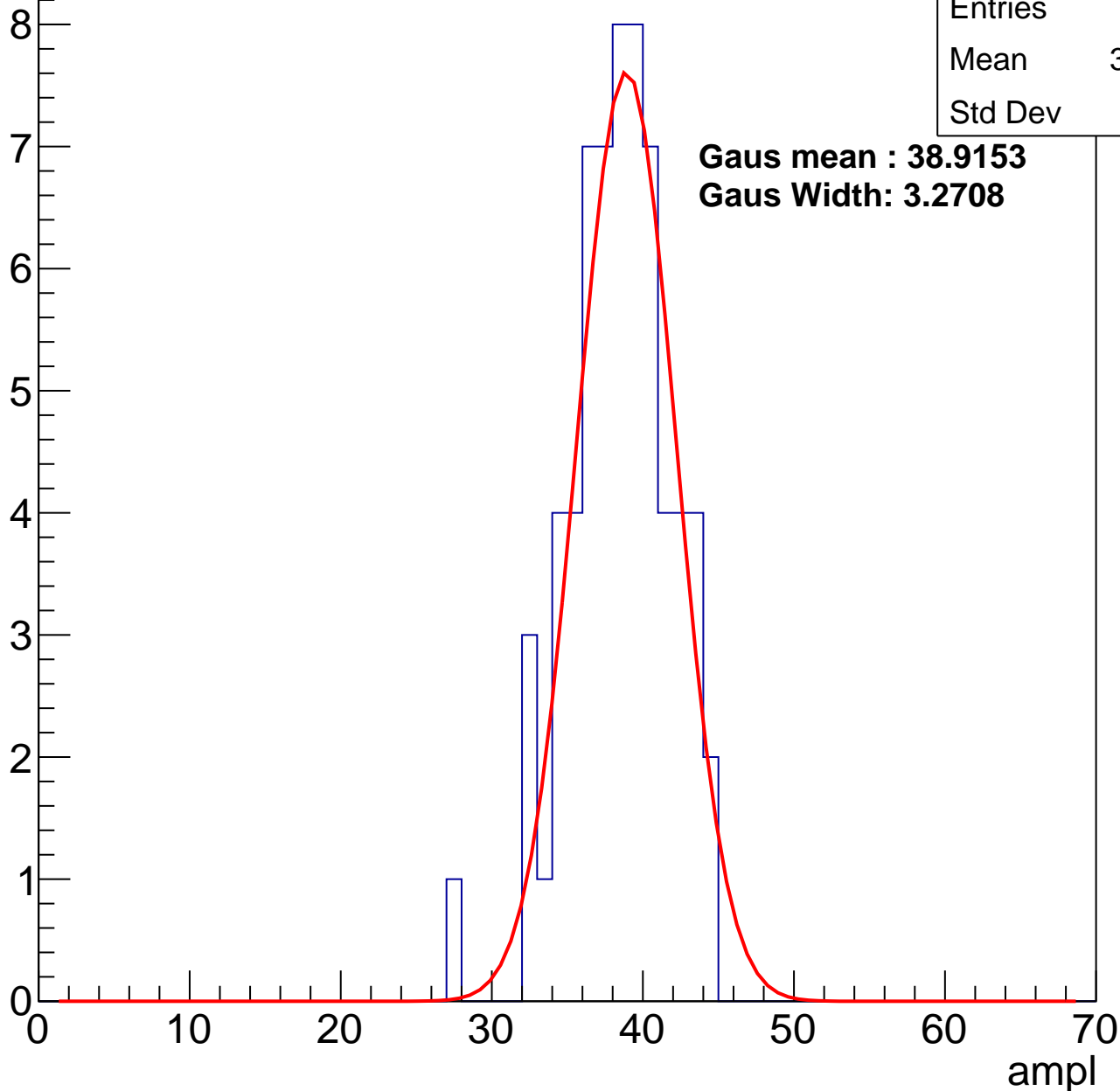
# B1L103S, U9-ch121, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	37.98
Std Dev	3.3

**Gaus mean : 38.9153**  
**Gaus Width: 3.2708**



# B1L103S, U9-ch121, adc2

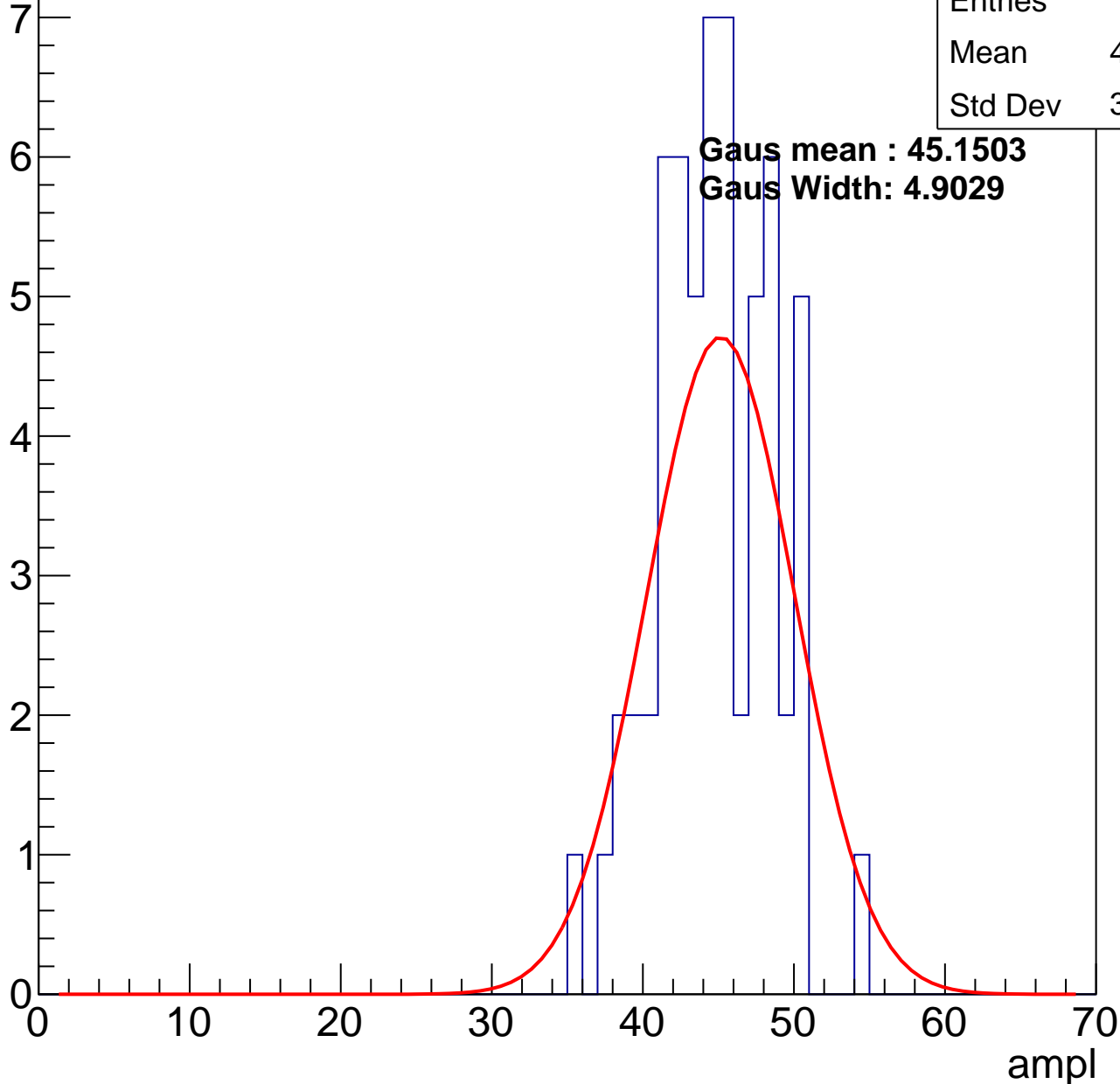
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	60
Mean	44.32
Std Dev	3.757

**Gaus mean : 45.1503**

**Gaus Width: 4.9029**



# B1L103S, U9-ch121, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	71
Mean	50.48
Std Dev	3.718

Entry

10

8

6

4

2

0

0

10

20

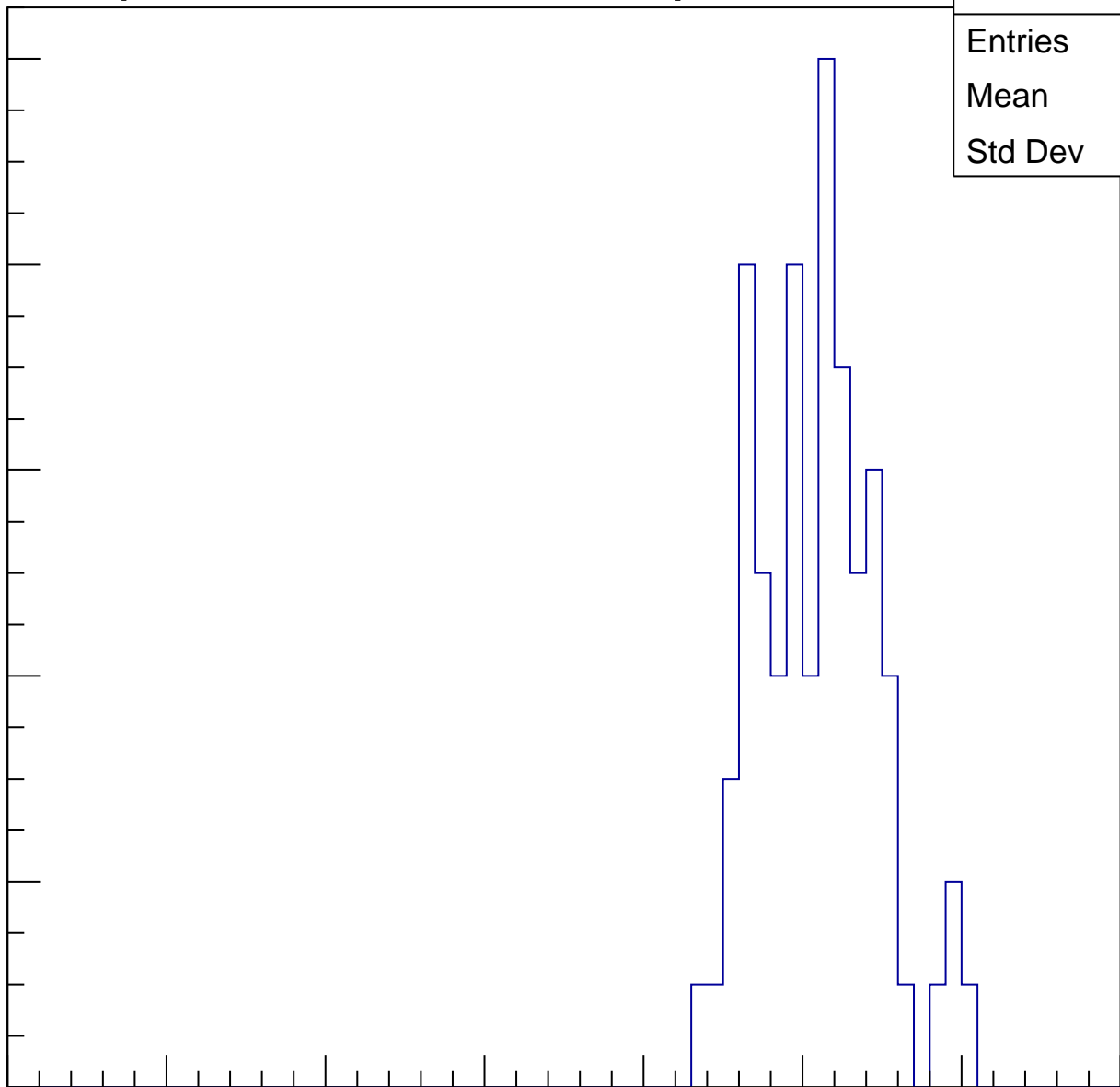
30

40

50

60

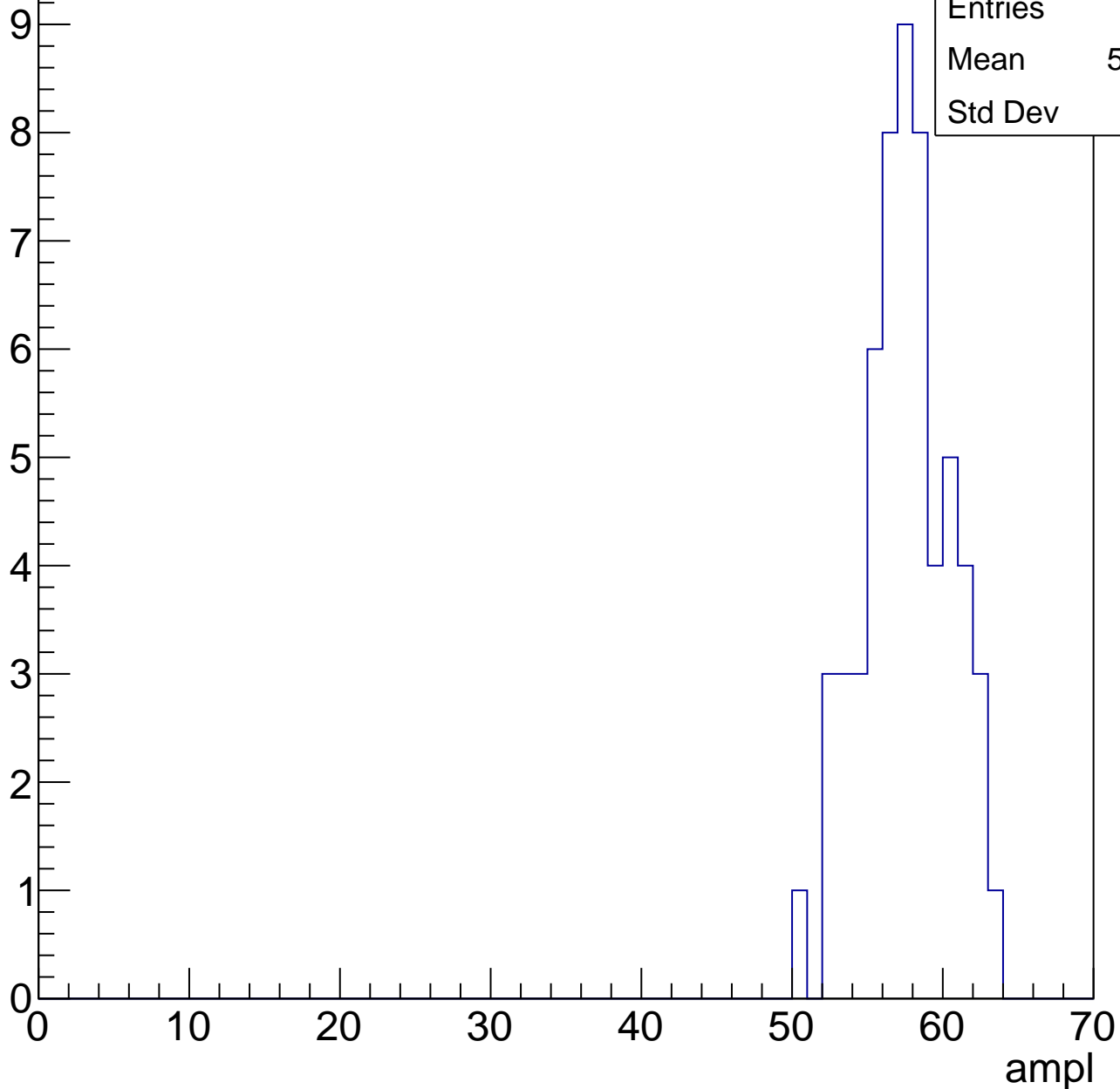
ampl



# B1L103S, U9-ch121, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



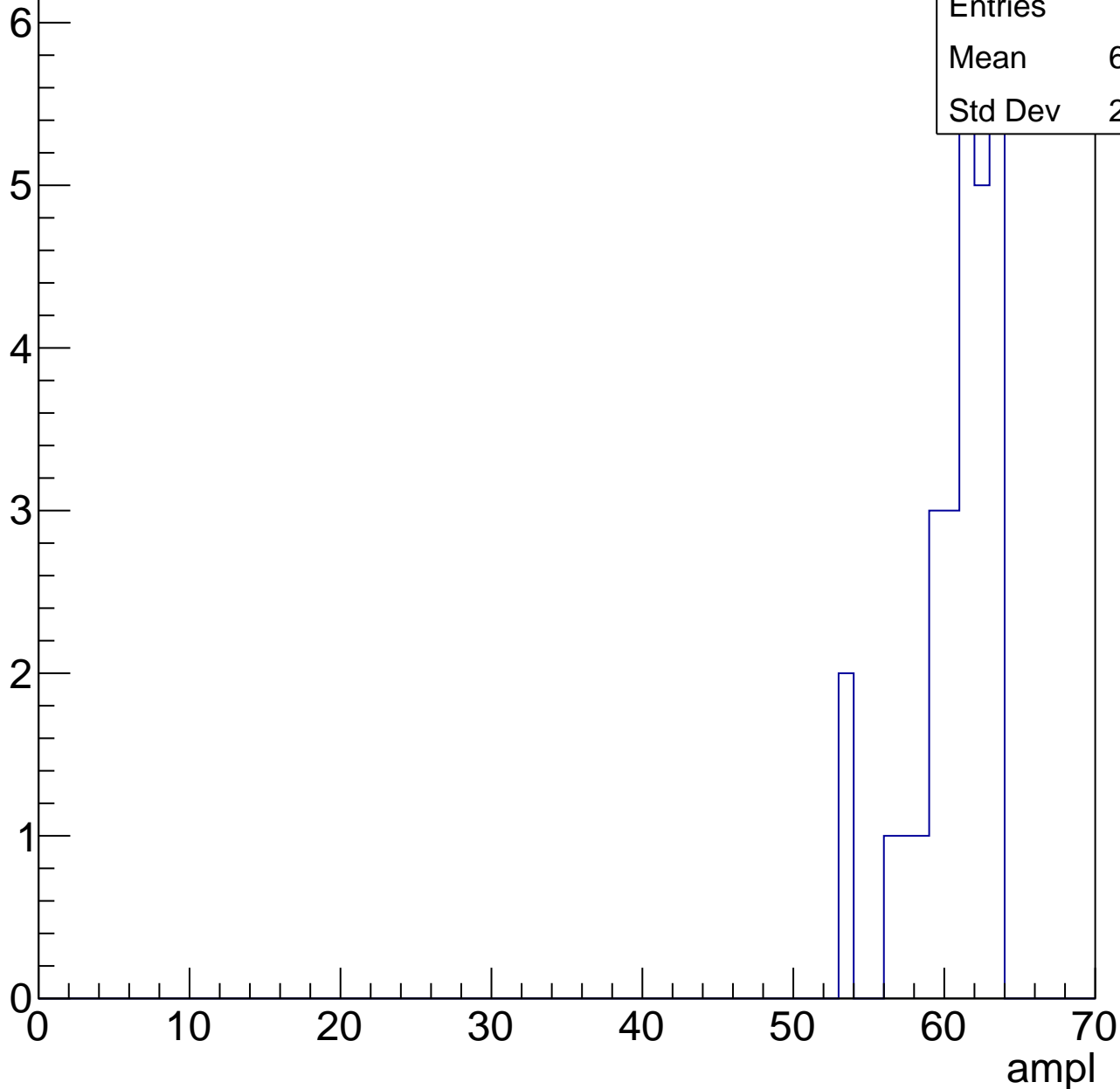
Entries	58
Mean	57.09
Std Dev	2.86

# B1L103S, U9-ch121, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

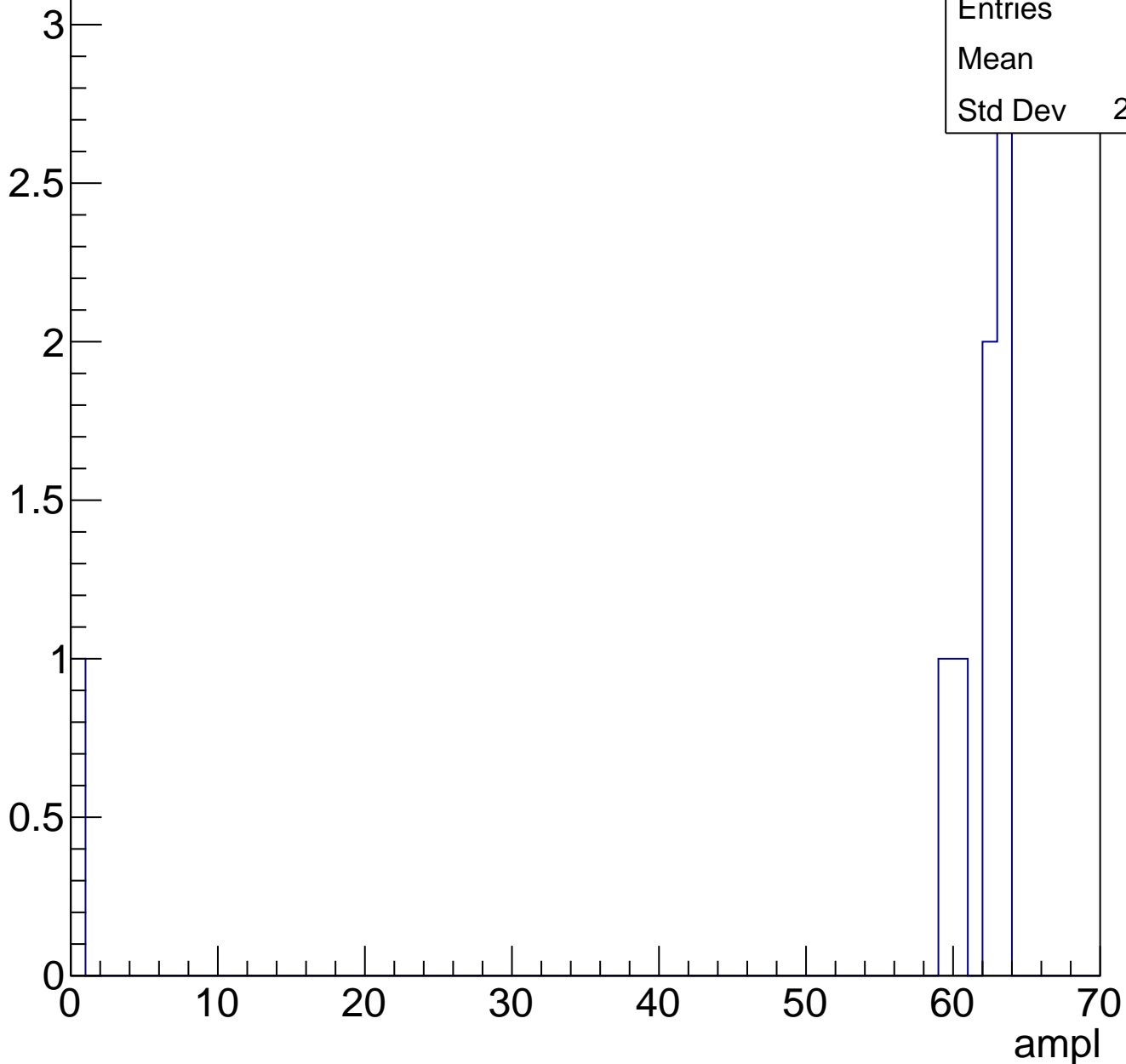
Entries	28
Mean	60.29
Std Dev	2.724



# B1L103S, U9-ch121, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	8
Mean	54
Std Dev	20.46



# B1L103S, U9-ch121, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U9-ch122, adc0

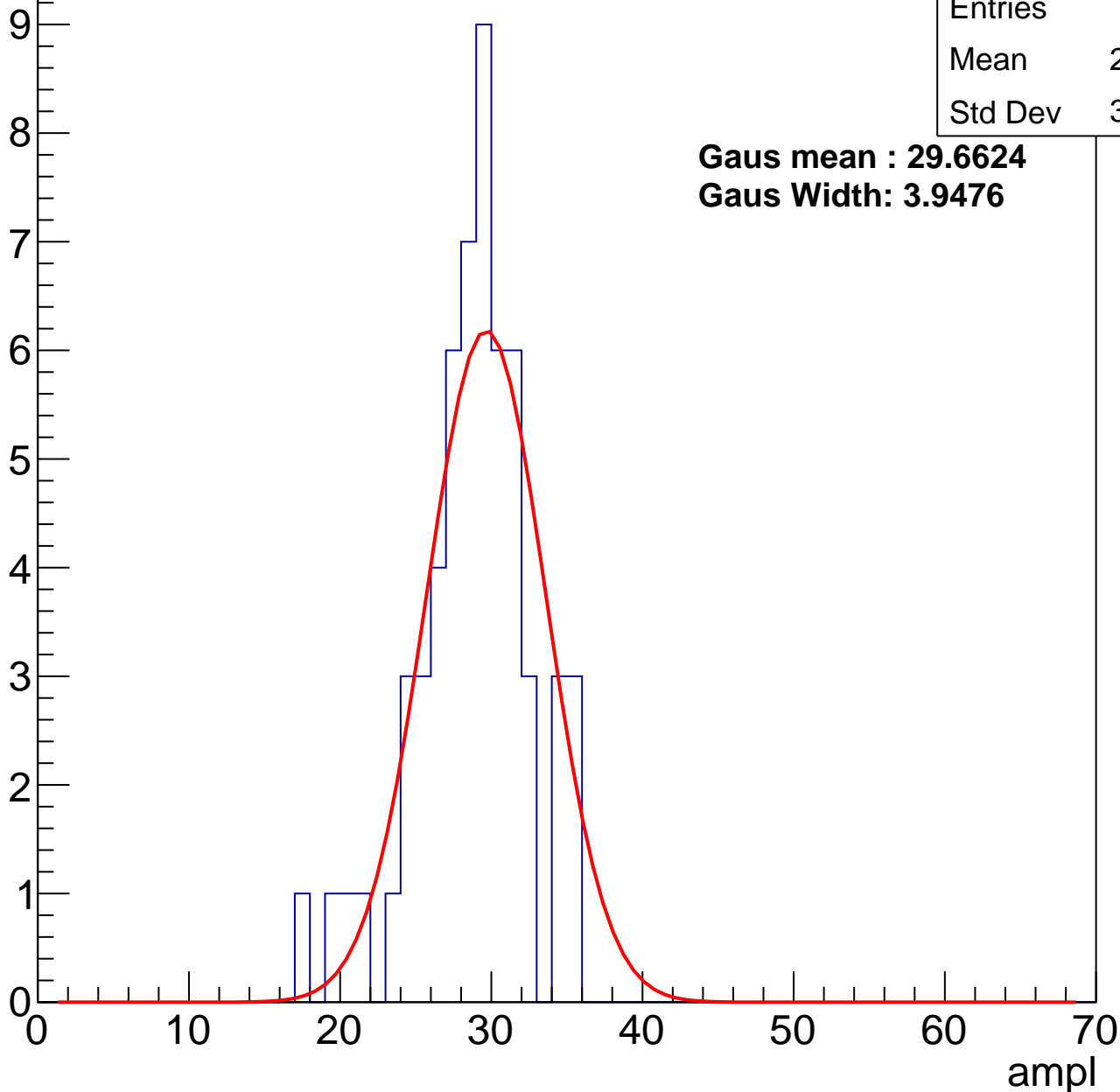
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	58
Mean	28.26
Std Dev	3.767

**Gaus mean : 29.6624**

**Gaus Width: 3.9476**



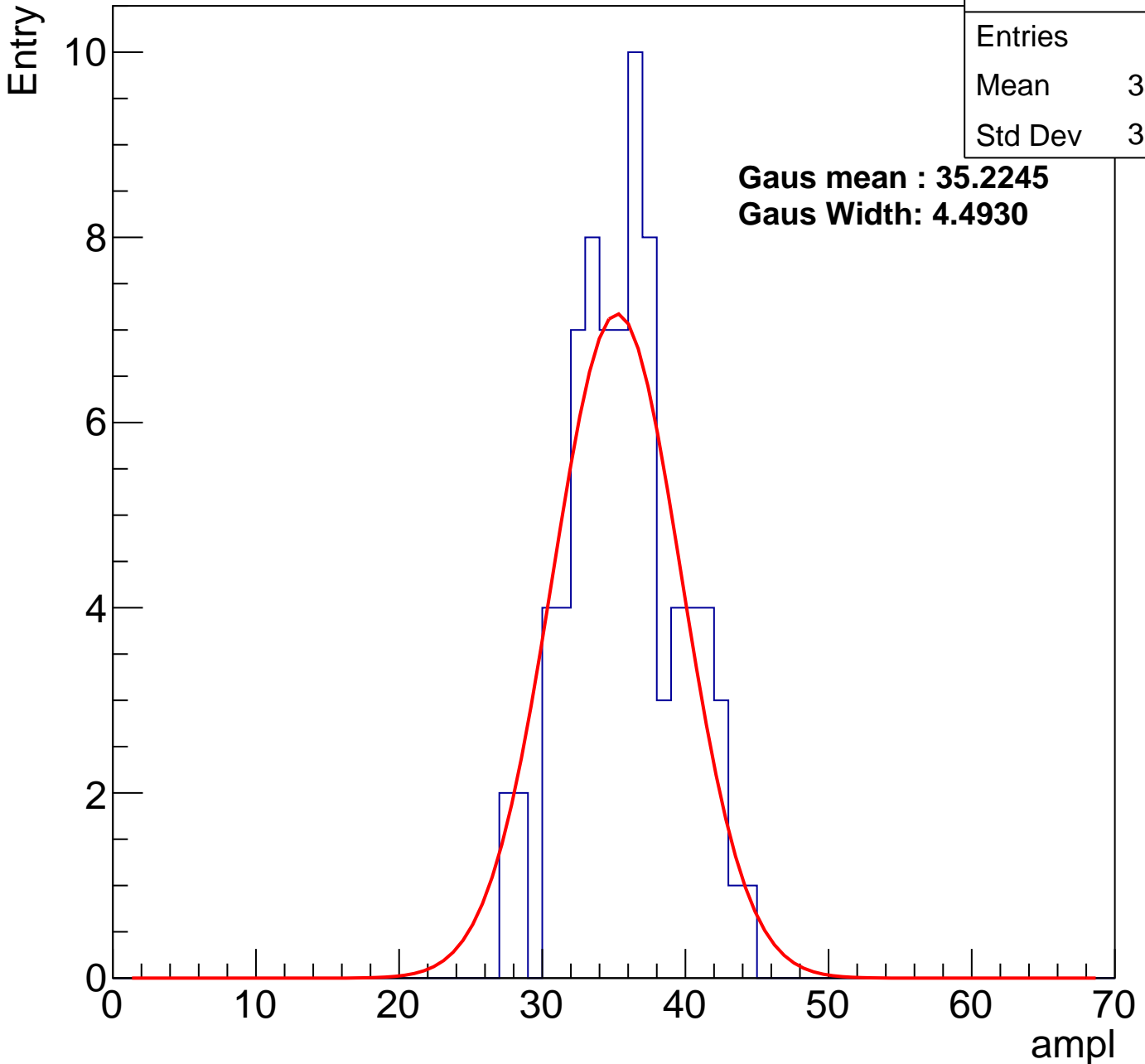
# B1L103S, U9-ch122, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	79
Mean	35.29
Std Dev	3.822

**Gaus mean : 35.2245**

**Gaus Width: 4.4930**



# B1L103S, U9-ch122, adc2

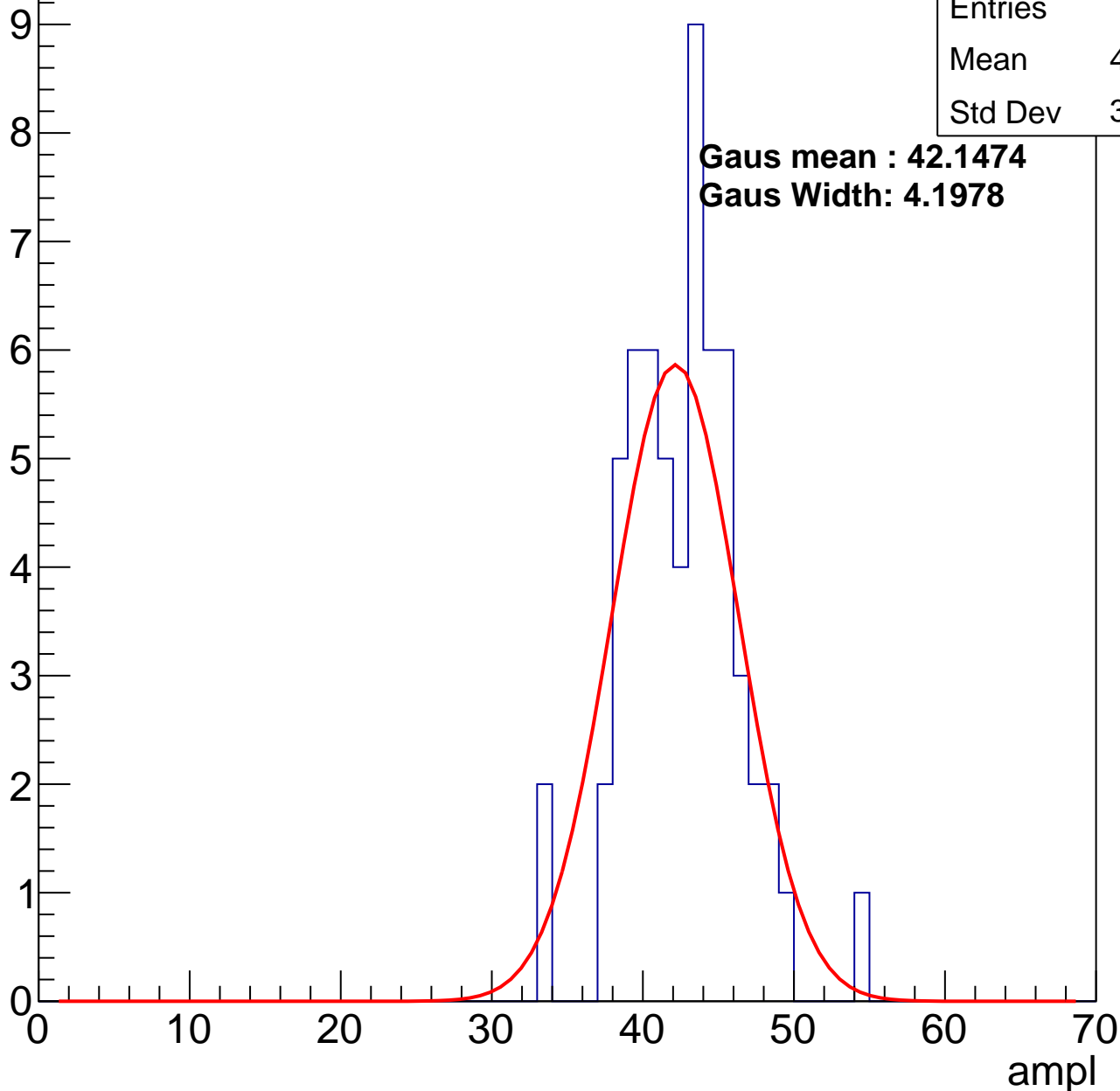
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	60
Mean	42.15
Std Dev	3.705

**Gaus mean : 42.1474**

**Gaus Width: 4.1978**

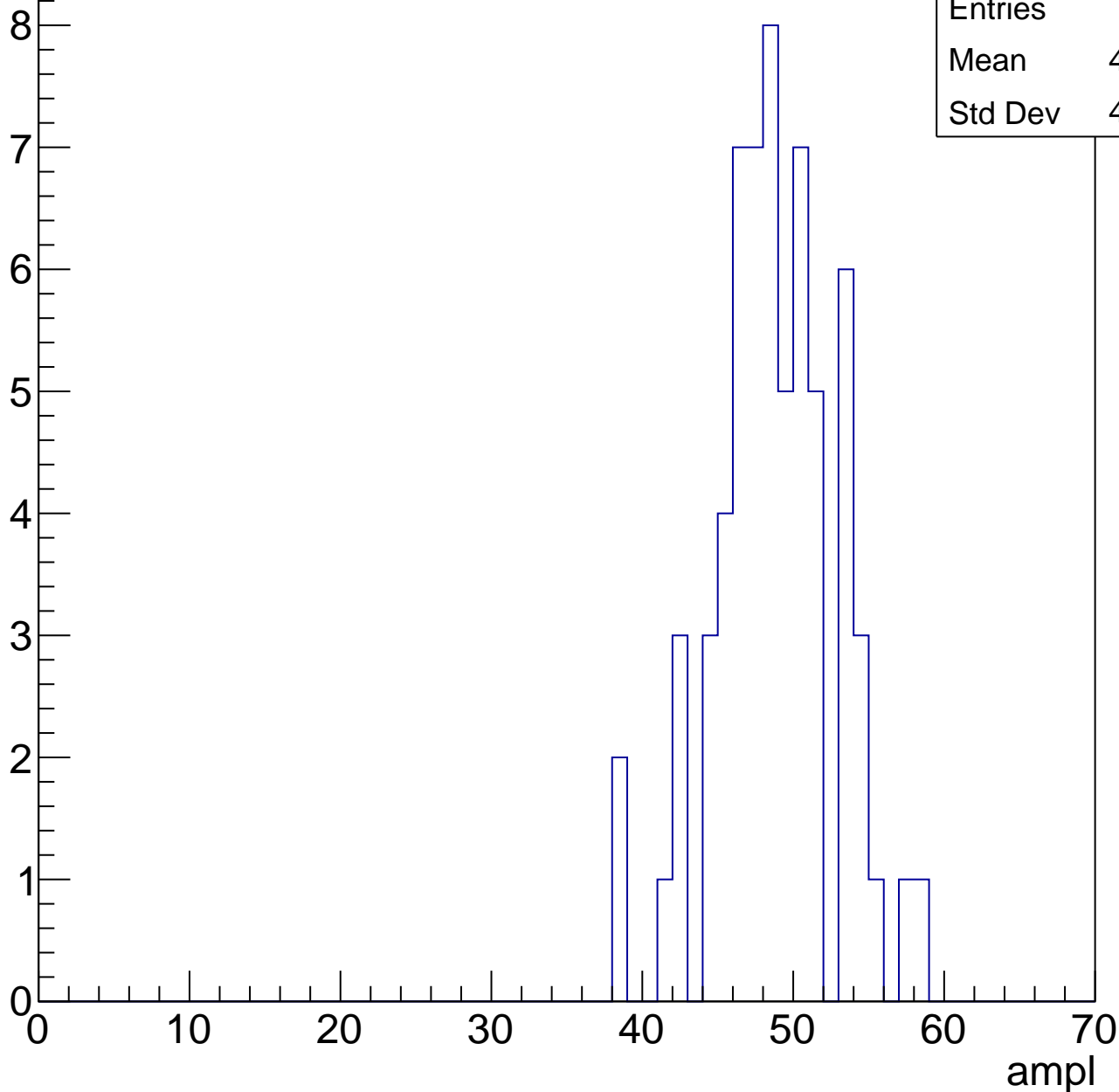


# B1L103S, U9-ch122, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	48.28
Std Dev	4.025

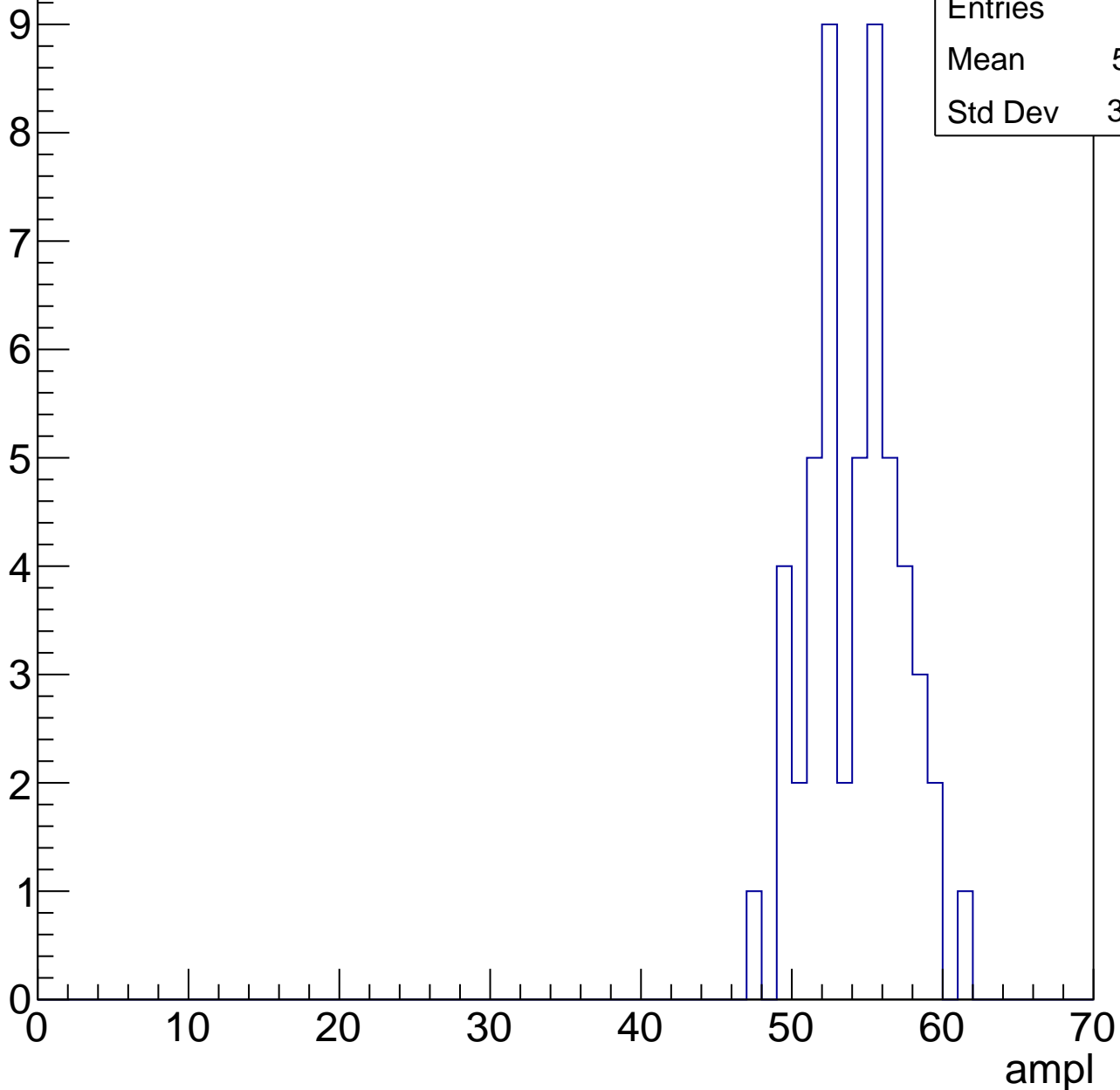


# B1L103S, U9-ch122, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

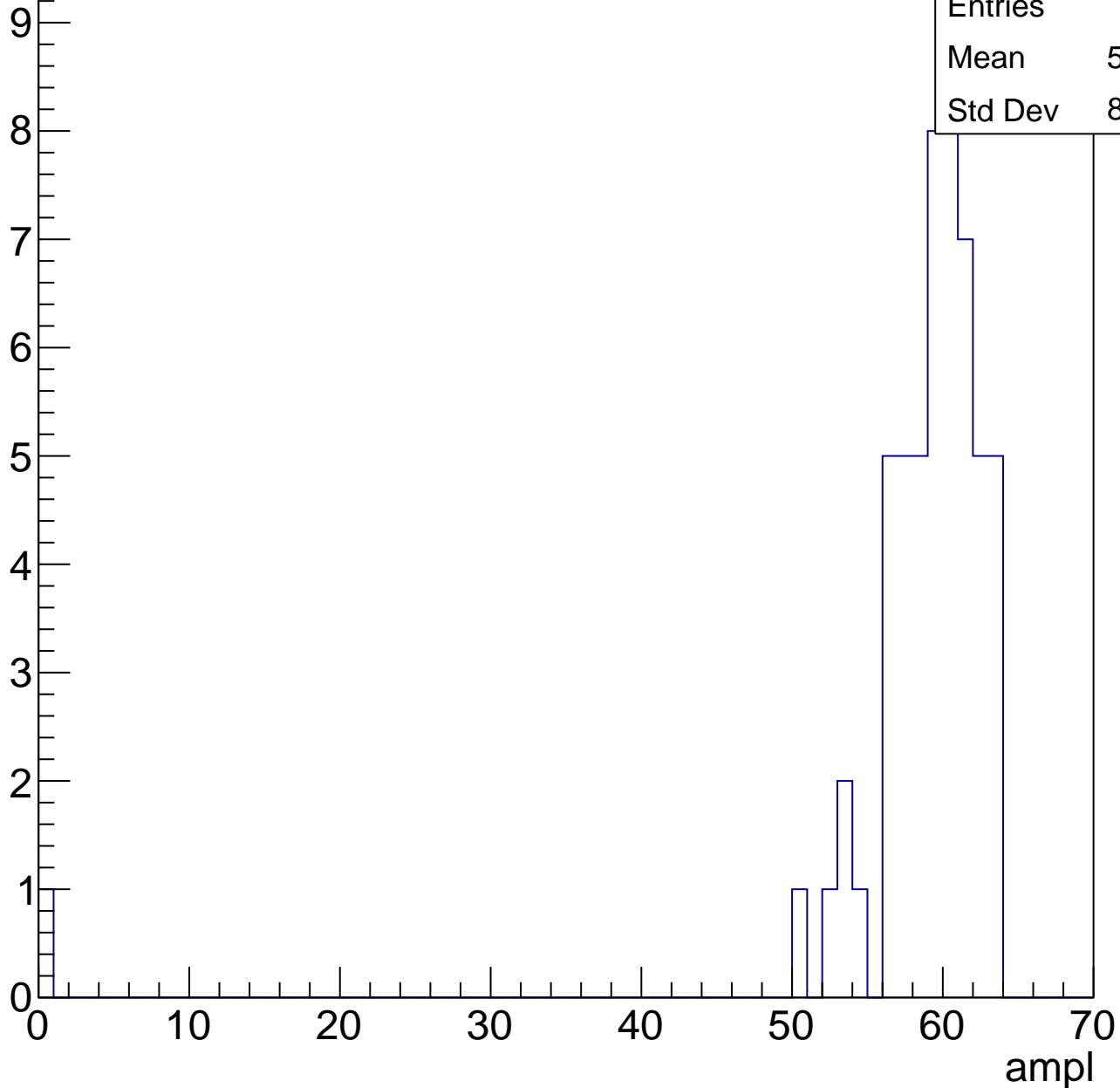
Entries	52
Mean	53.81
Std Dev	3.019



# B1L103S, U9-ch122, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

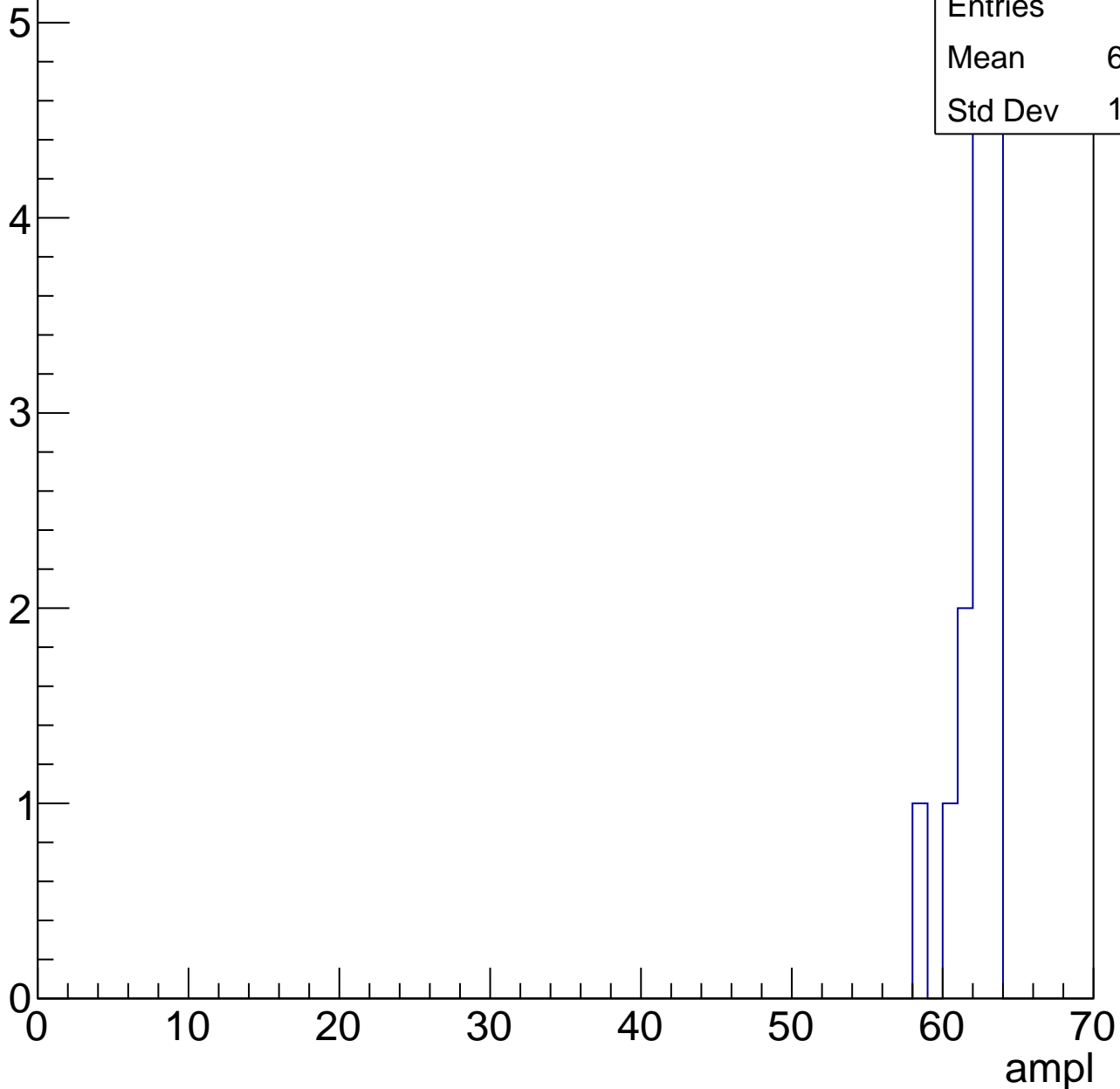


# B1L103S, U9-ch122, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	14
Mean	61.79
Std Dev	1.372





# B1L103S, U9-ch122, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U9-ch123, adc0

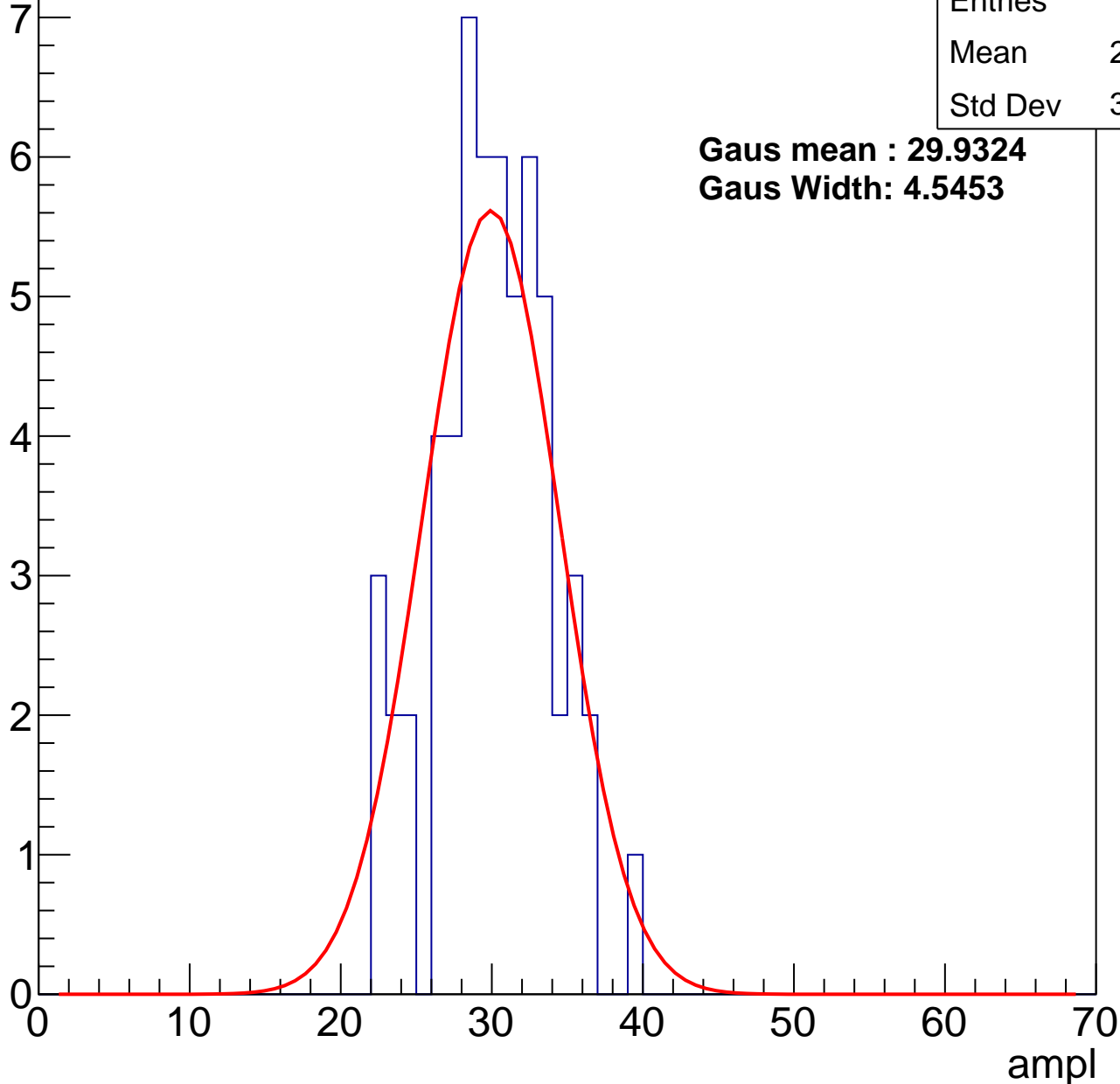
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	58
Mean	29.62
Std Dev	3.764

**Gaus mean : 29.9324**

**Gaus Width: 4.5453**



# B1L103S, U9-ch123, adc1

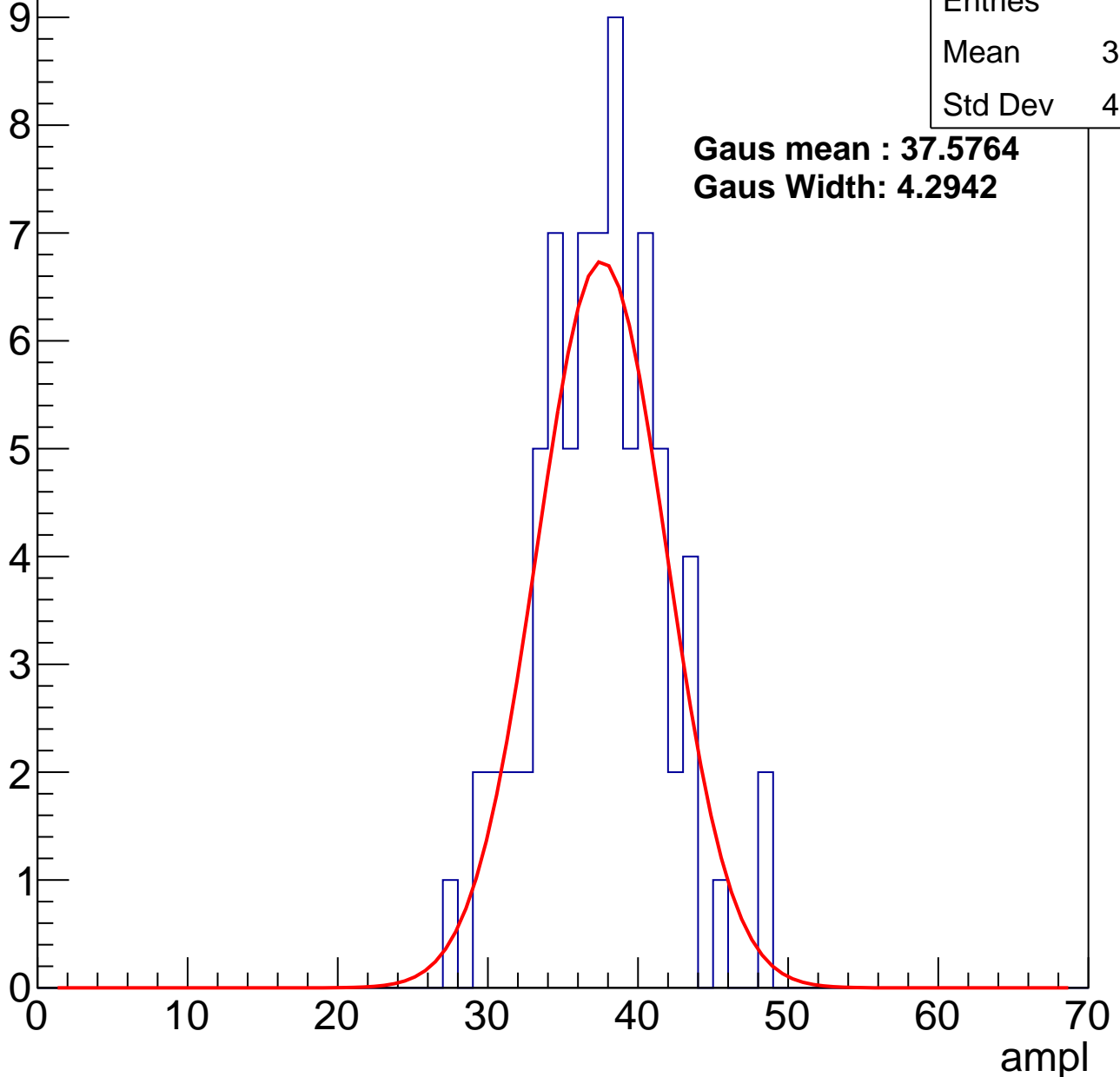
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	75
Mean	37.05
Std Dev	4.147

**Gaus mean : 37.5764**

**Gaus Width: 4.2942**



# B1L103S, U9-ch123, adc2

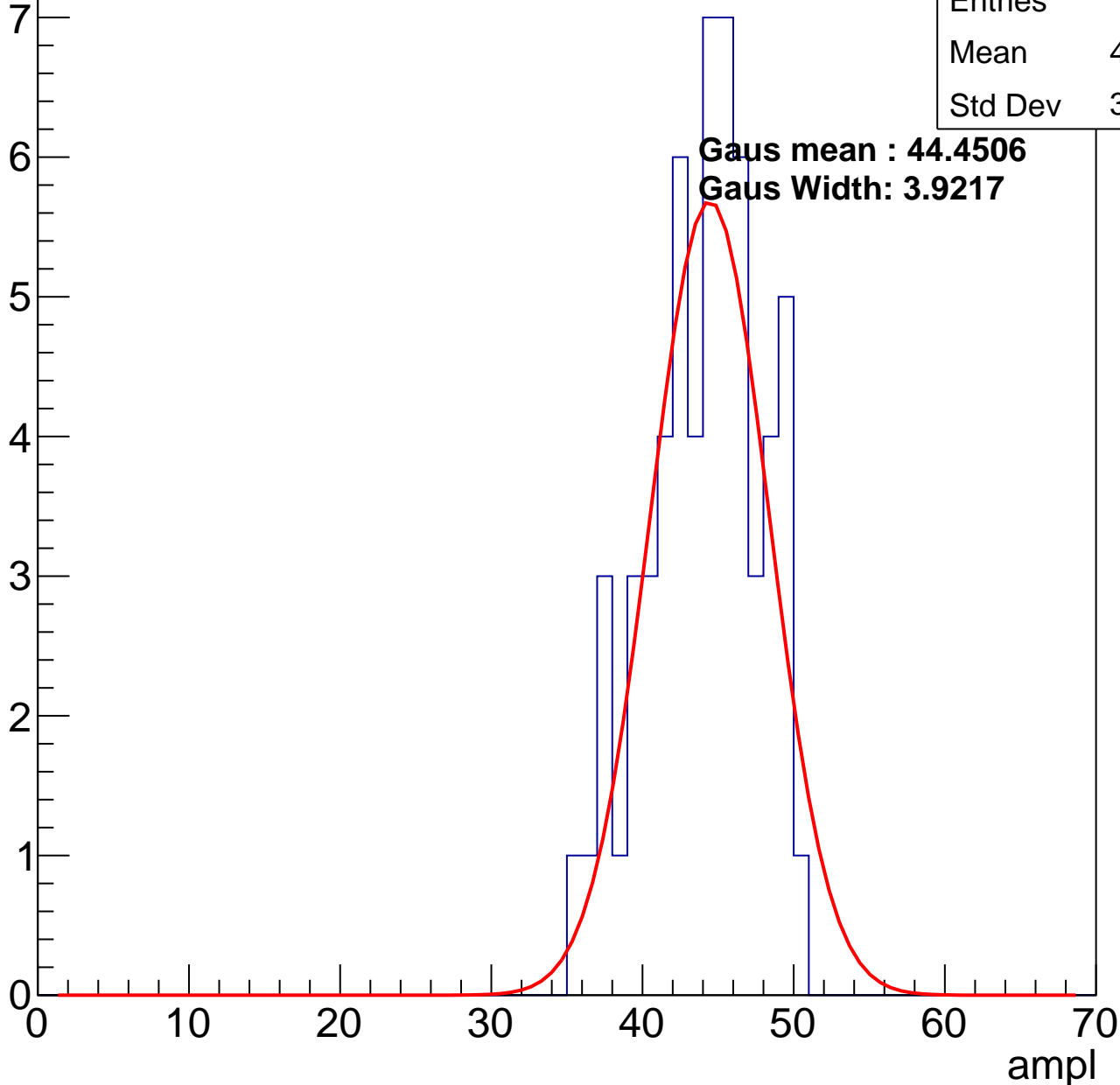
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	59
Mean	43.59
Std Dev	3.655

**Gaus mean : 44.4506**

**Gaus Width: 3.9217**

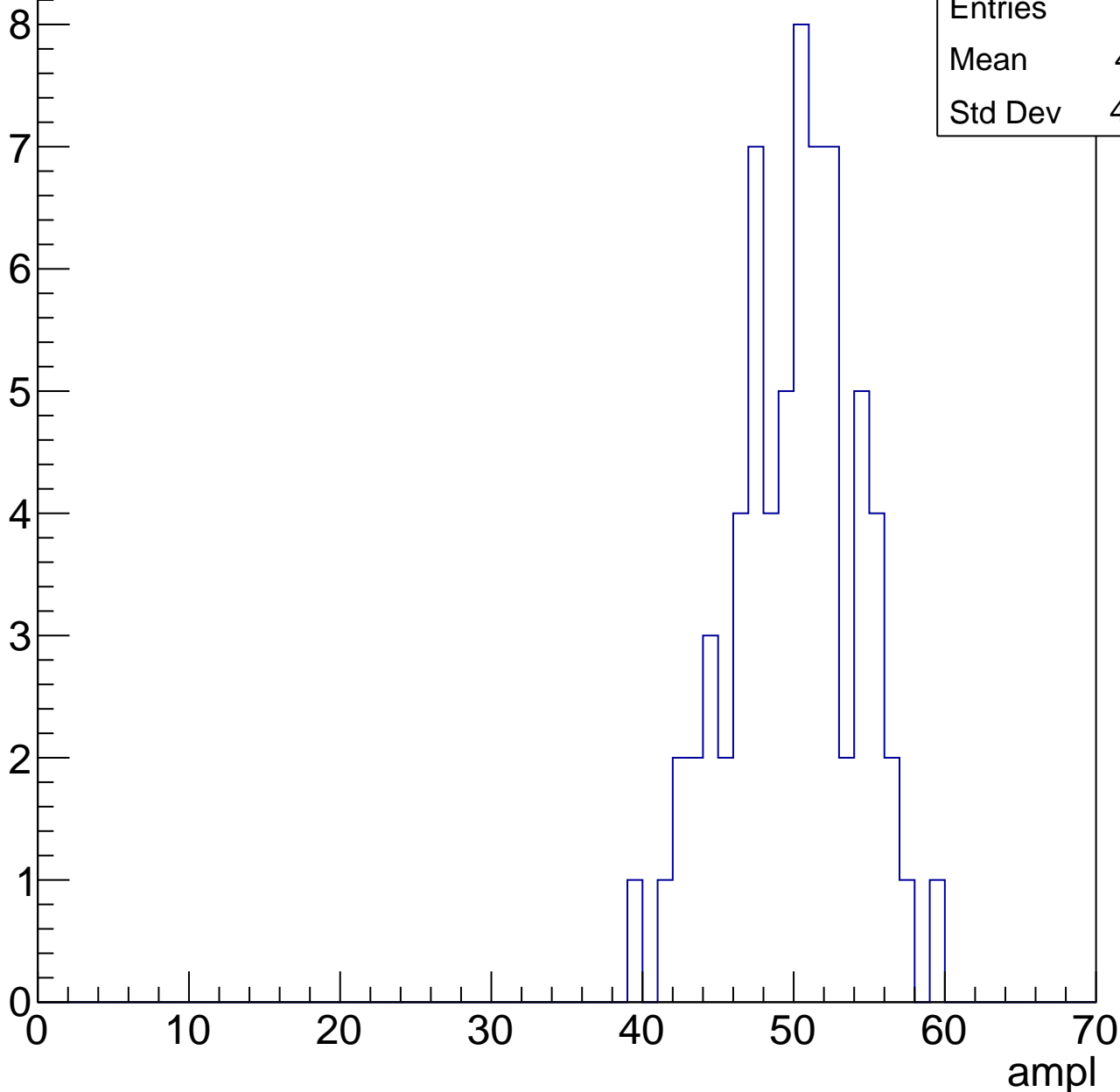


# B1L103S, U9-ch123, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	68
Mean	49.51
Std Dev	4.118



# B1L103S, U9-ch123, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

7

6

5

4

3

2

1

0

Entries	51
Mean	56.04
Std Dev	2.917

ampl

0

10

20

30

40

50

60

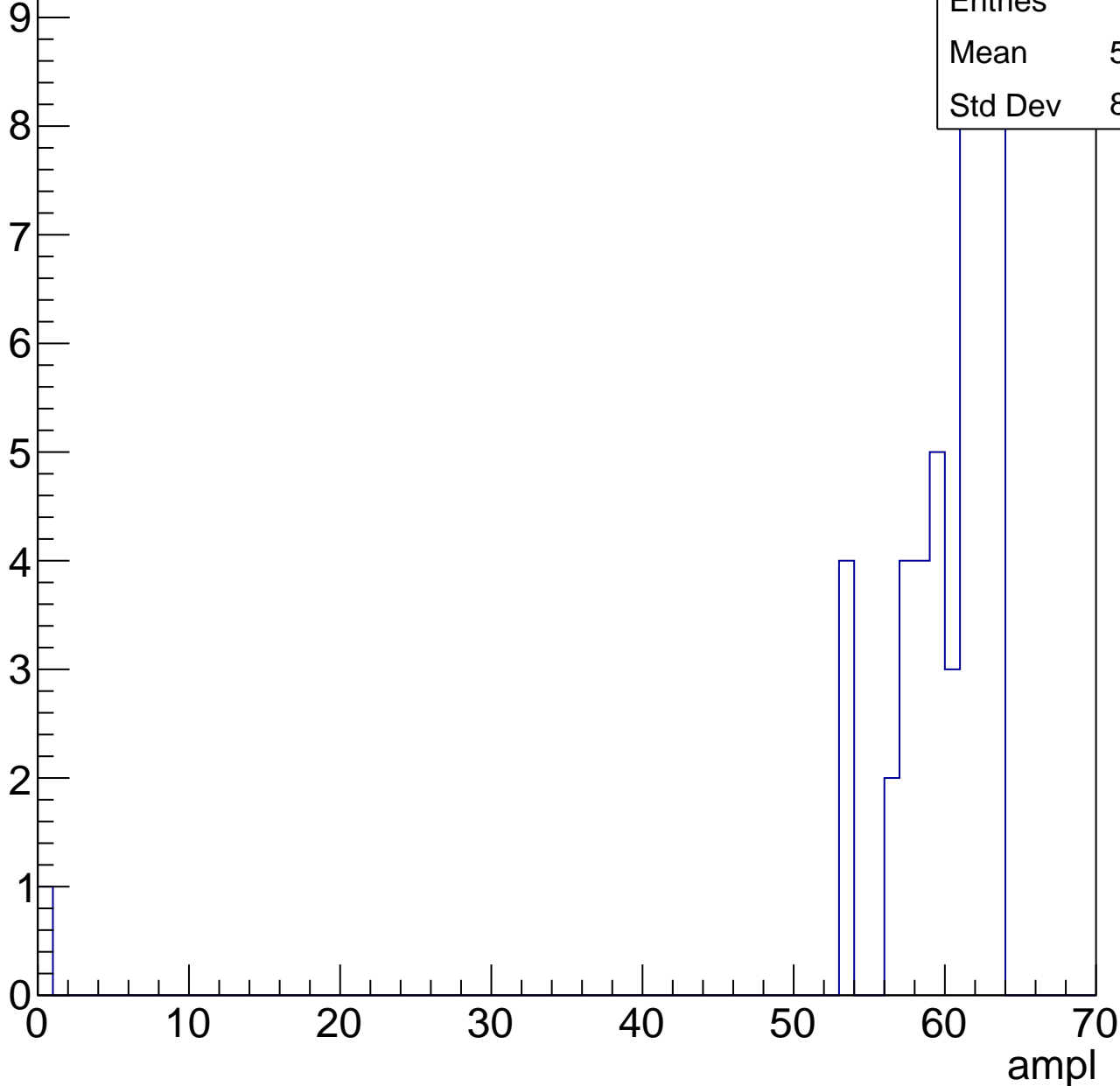
70

# B1L103S, U9-ch123, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	49
Mean	58.57
Std Dev	8.924



# B1L103S, U9-ch123, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

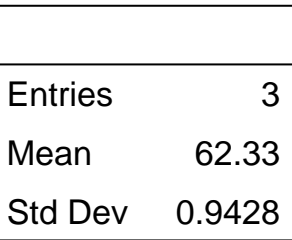
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	3
Mean	62.33
Std Dev	0.9428

ampl

0 10 20 30 40 50 60 70





# B1L103S, U9-ch123, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U9-ch124, adc0

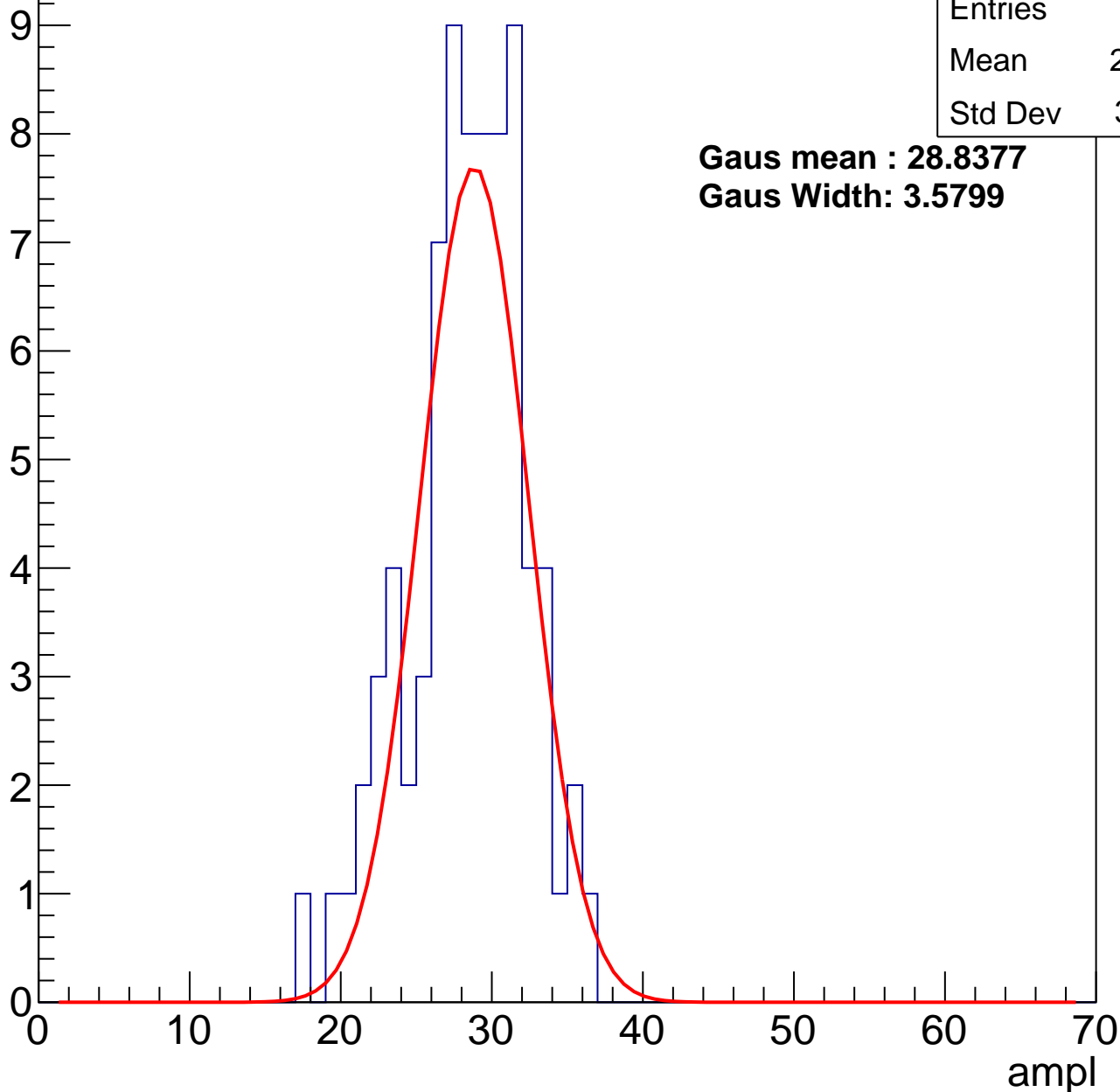
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	78
Mean	27.94
Std Dev	3.841

**Gaus mean : 28.8377**

**Gaus Width: 3.5799**



# B1L103S, U9-ch124, adc1

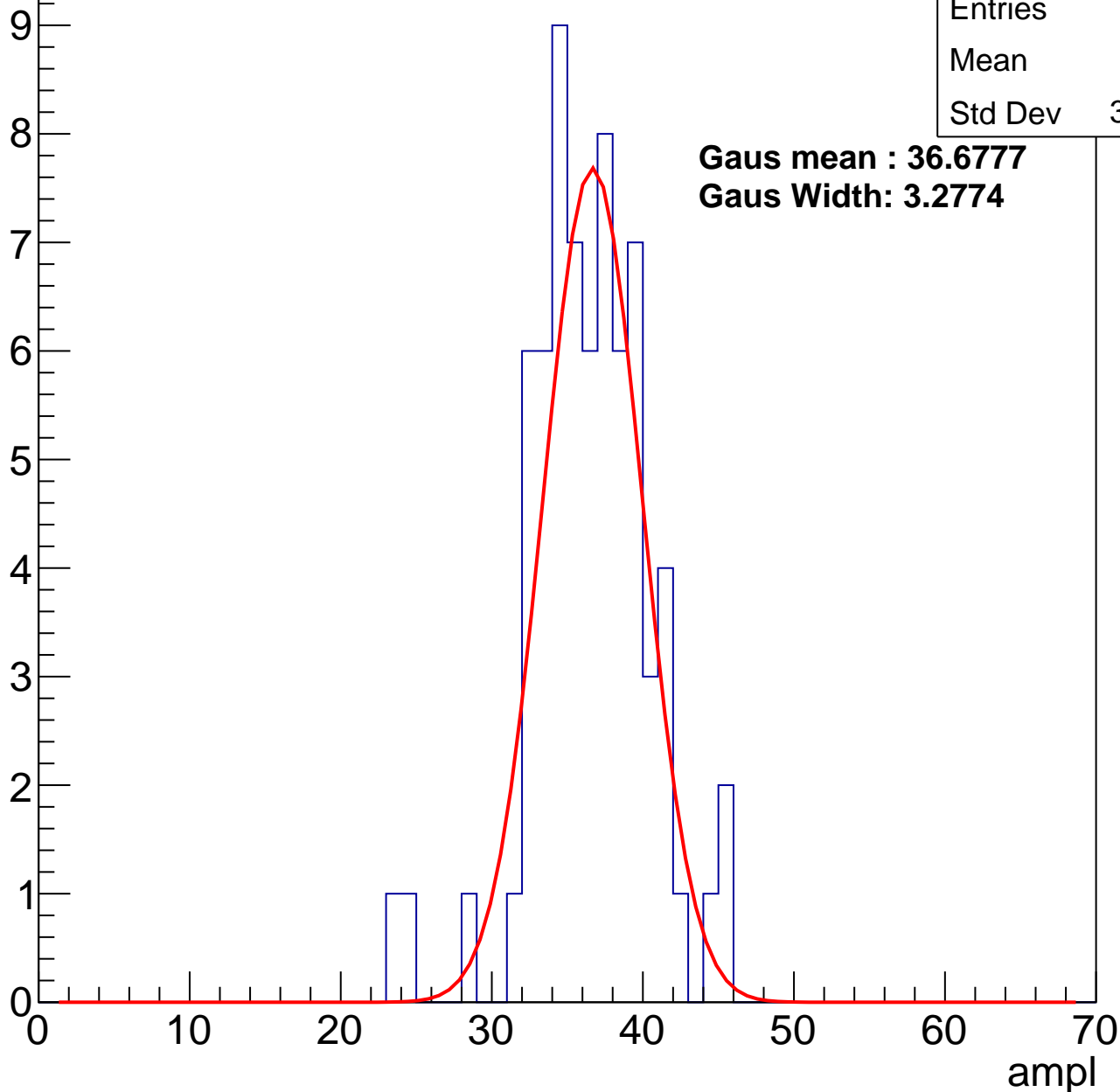
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	70
Mean	36
Std Dev	3.964

**Gaus mean : 36.6777**

**Gaus Width: 3.2774**



# B1L103S, U9-ch124, adc2

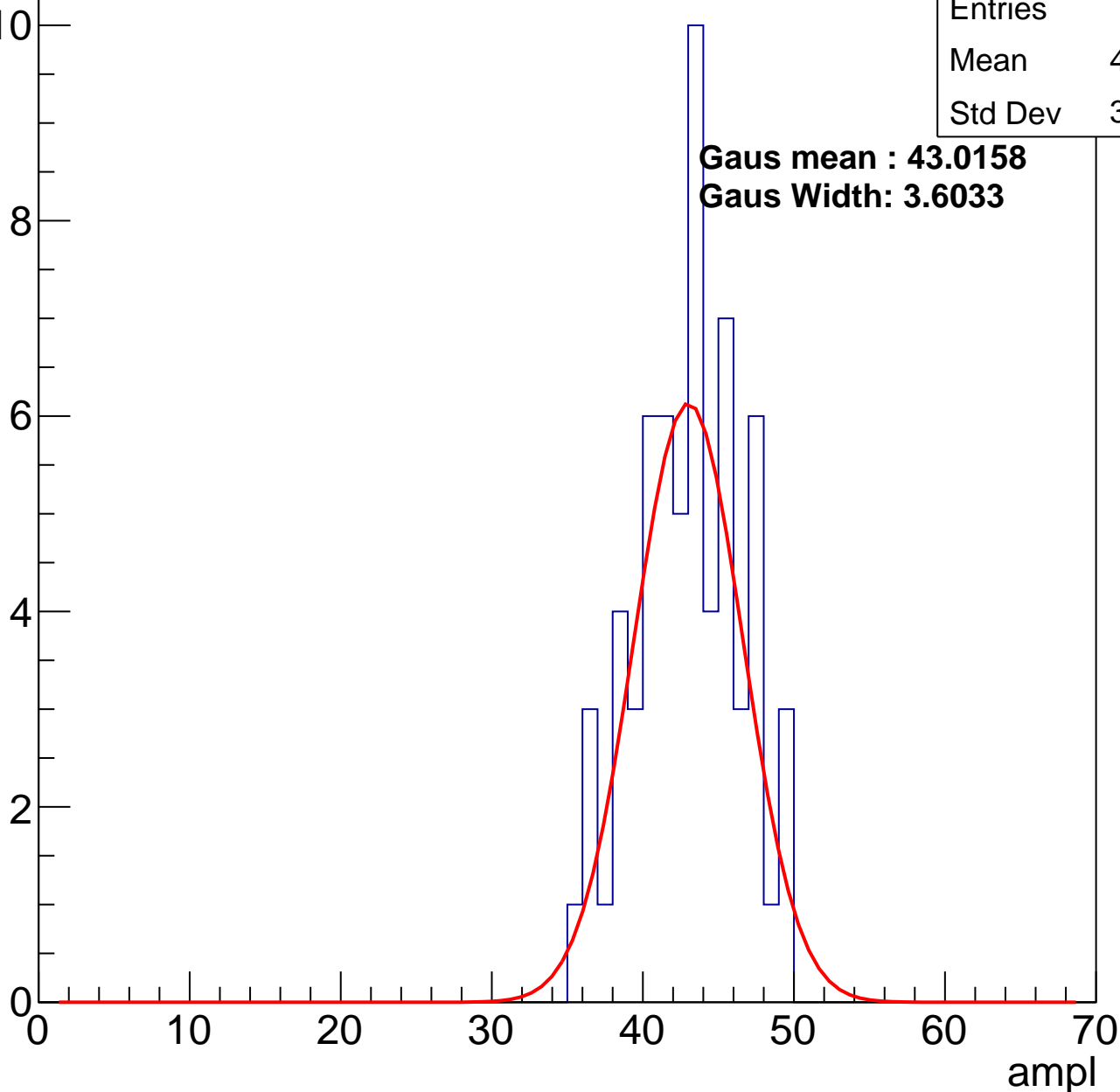
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	42.56
Std Dev	3.458

**Gaus mean : 43.0158**

**Gaus Width: 3.6033**

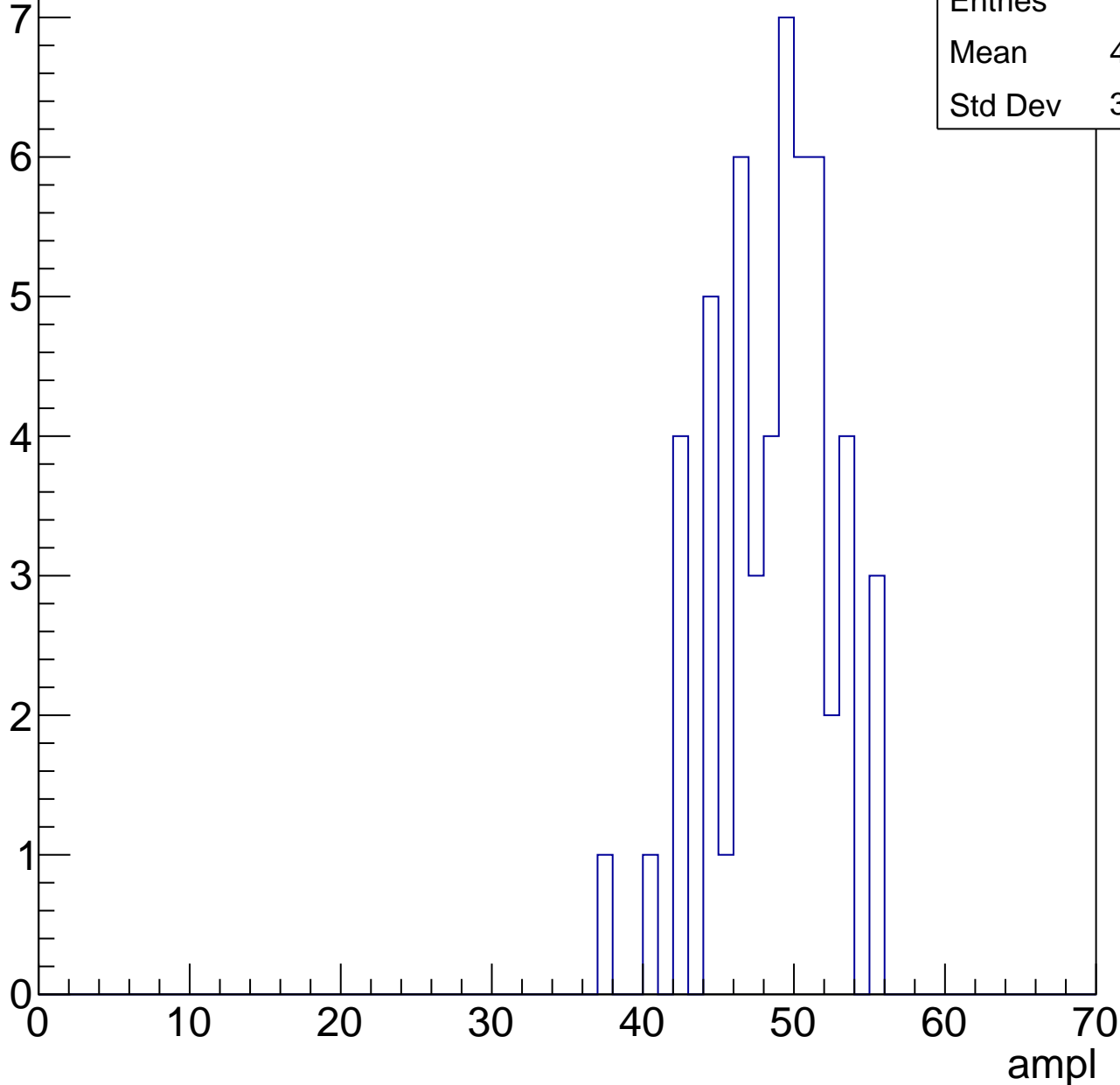


# B1L103S, U9-ch124, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	53
Mean	48.09
Std Dev	3.906

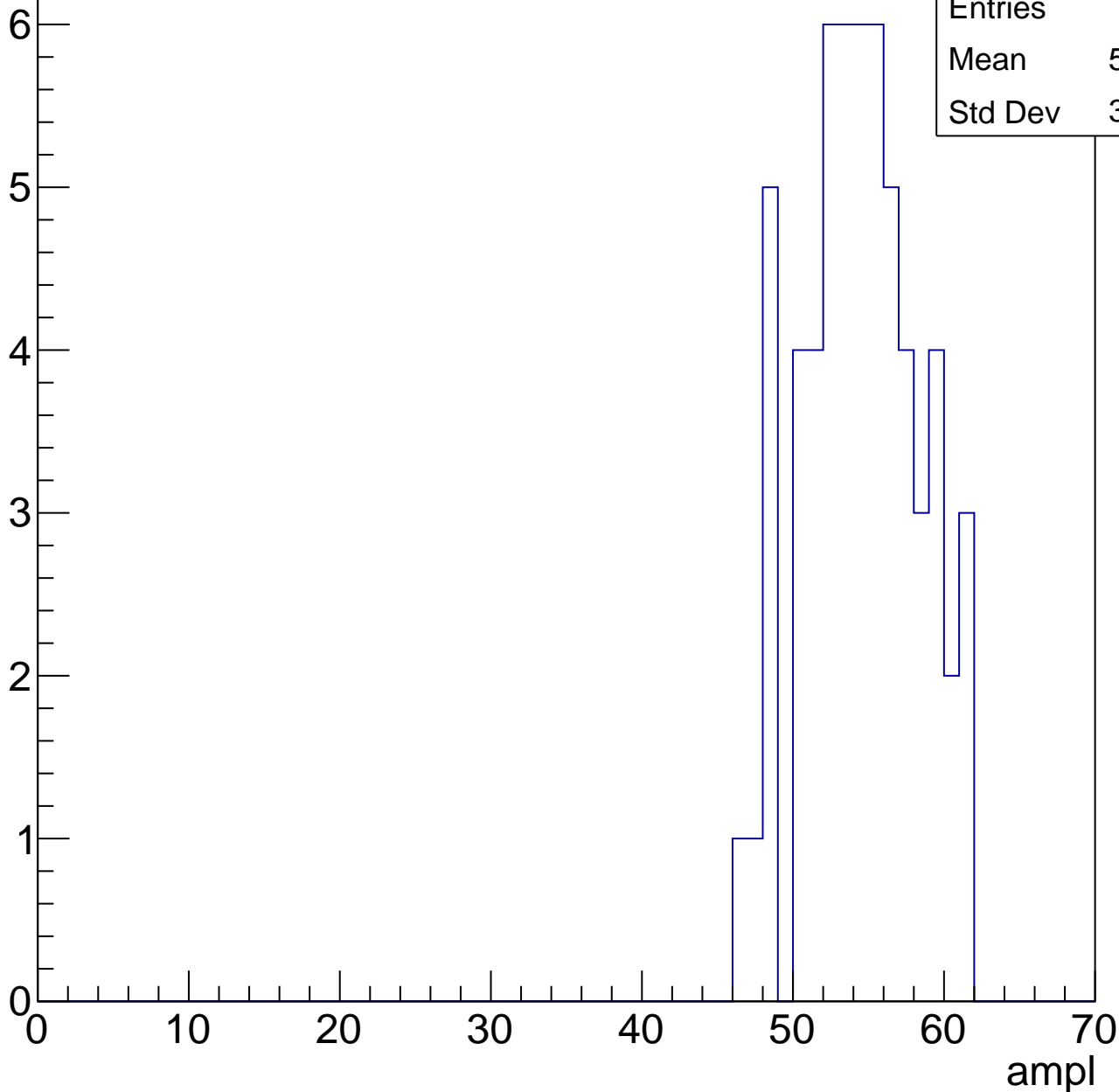


# B1L103S, U9-ch124, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

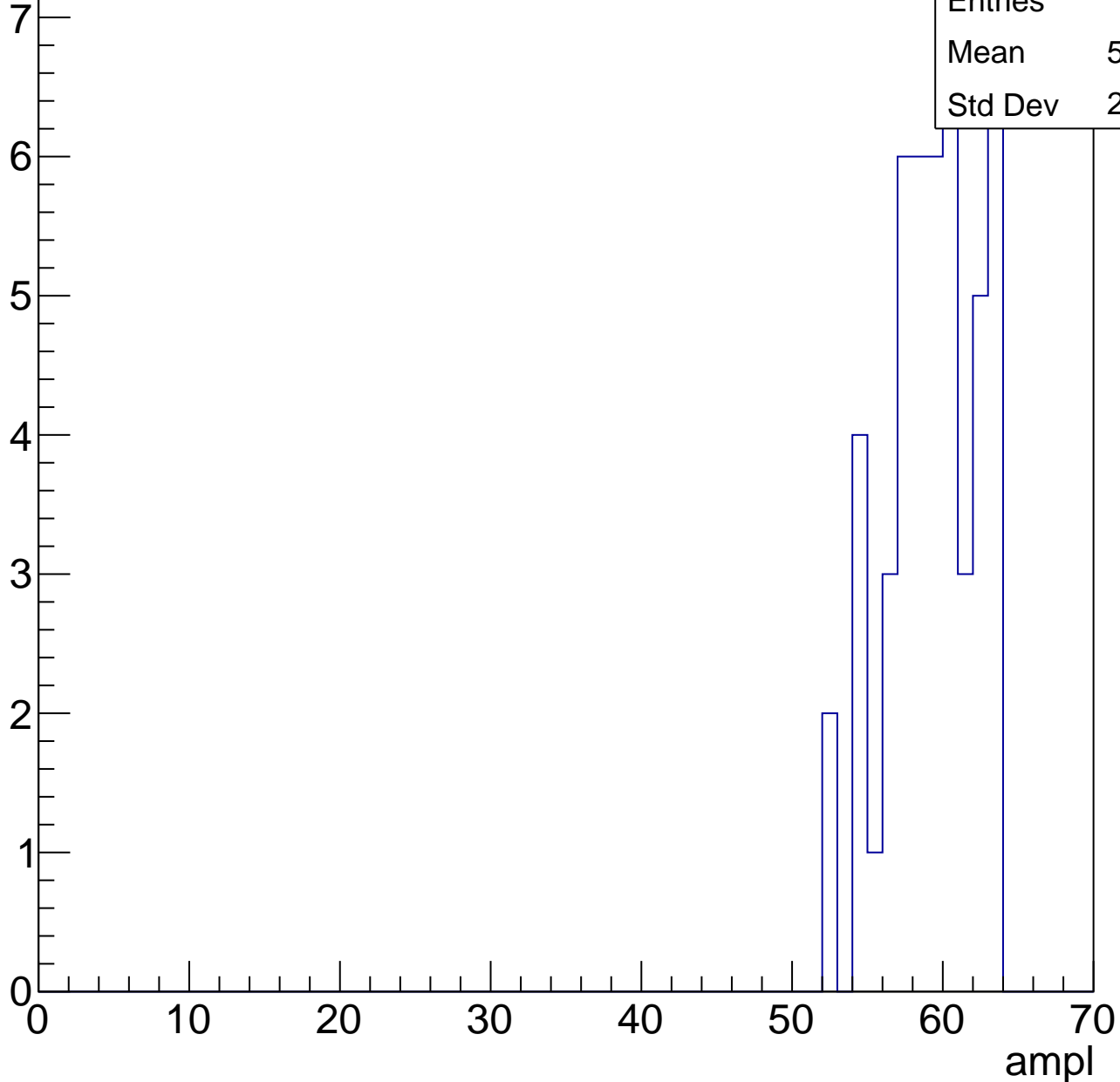
Entries	60
Mean	54.03
Std Dev	3.768



# B1L103S, U9-ch124, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

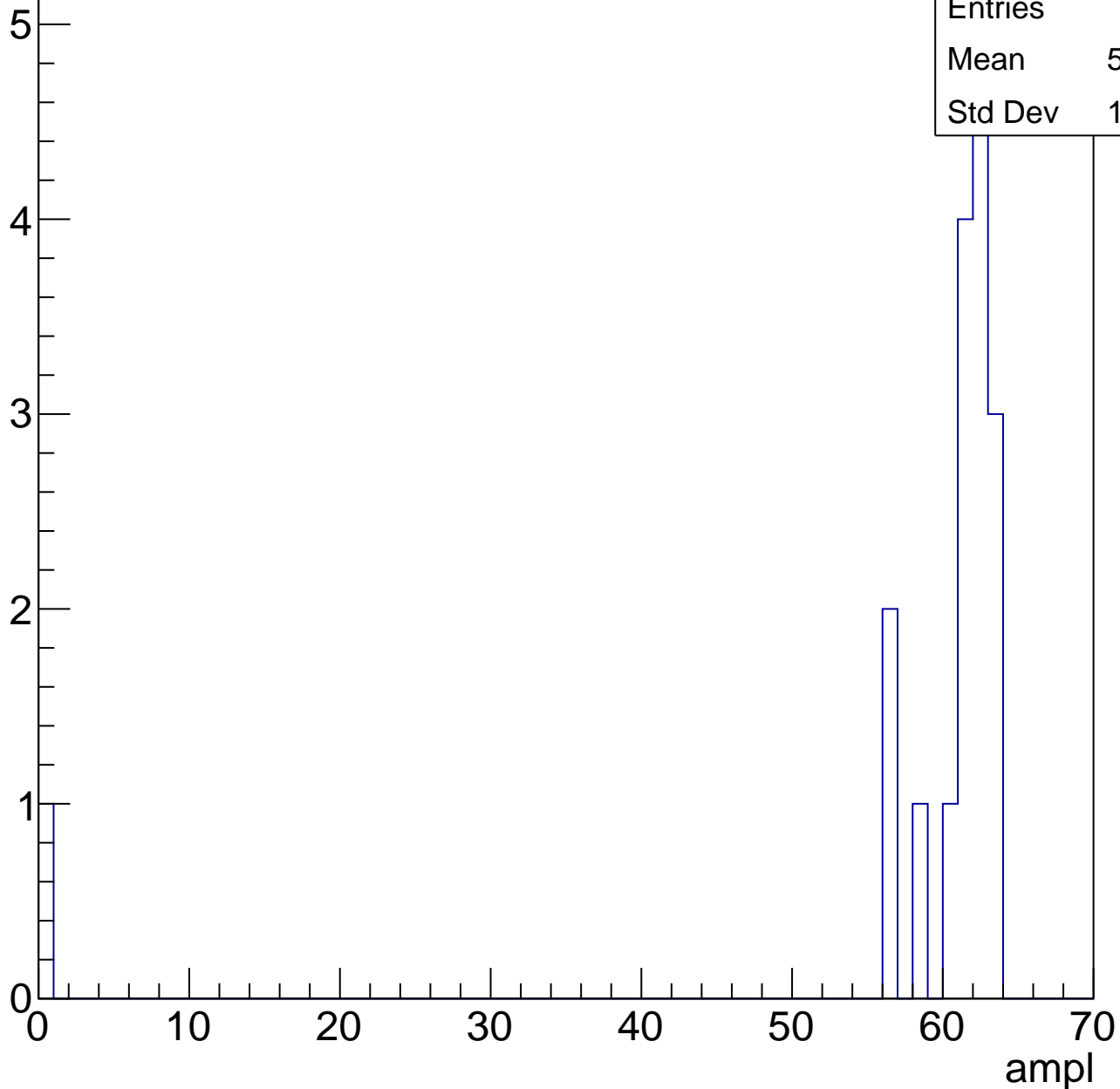


# B1L103S, U9-ch124, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	17
Mean	57.24
Std Dev	14.47





# B1L103S, U9-ch124, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L103S, U9-ch125, adc0

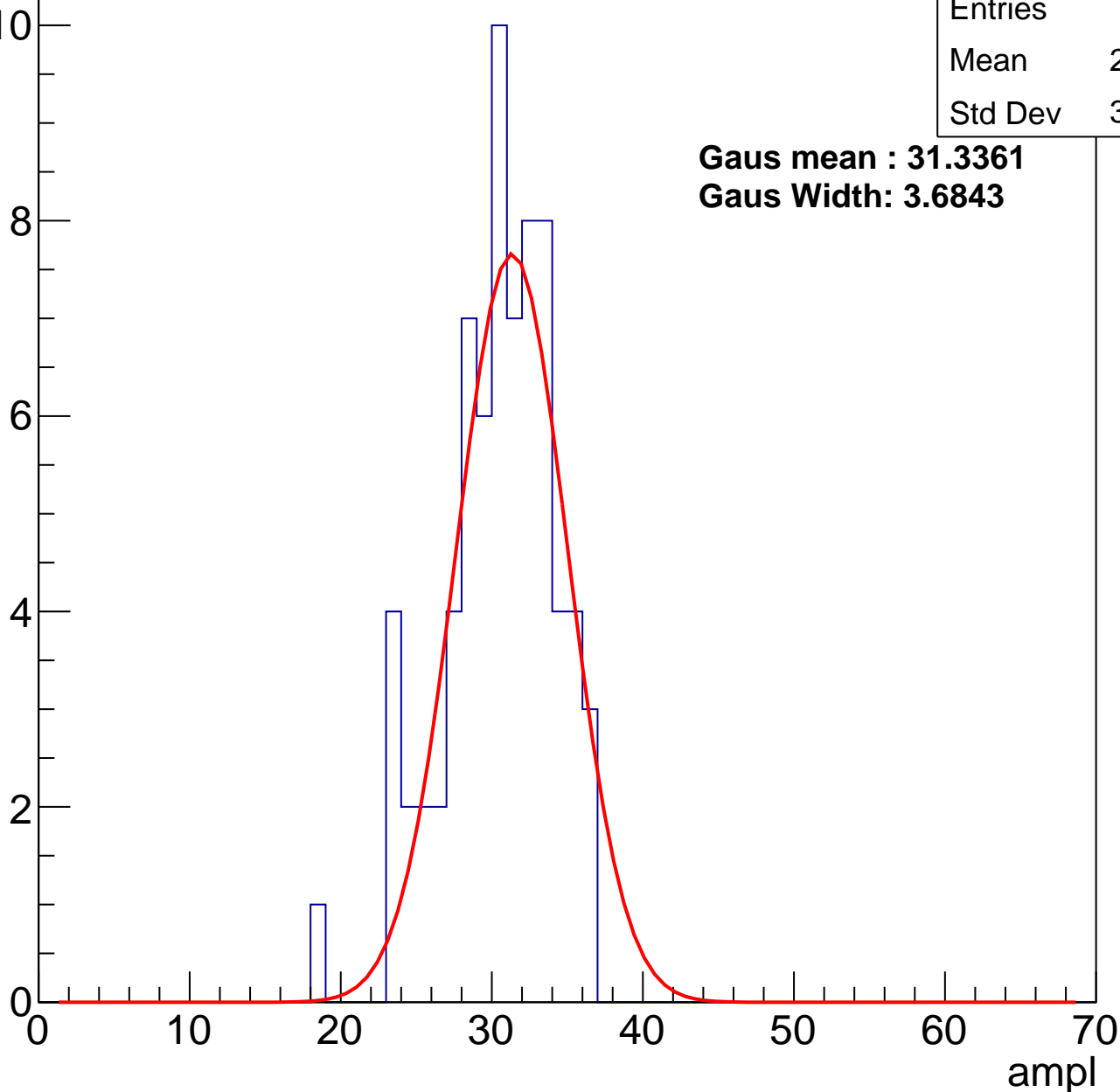
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	72
Mean	29.99
Std Dev	3.627

**Gaus mean : 31.3361**

**Gaus Width: 3.6843**



# B1L103S, U9-ch125, adc1

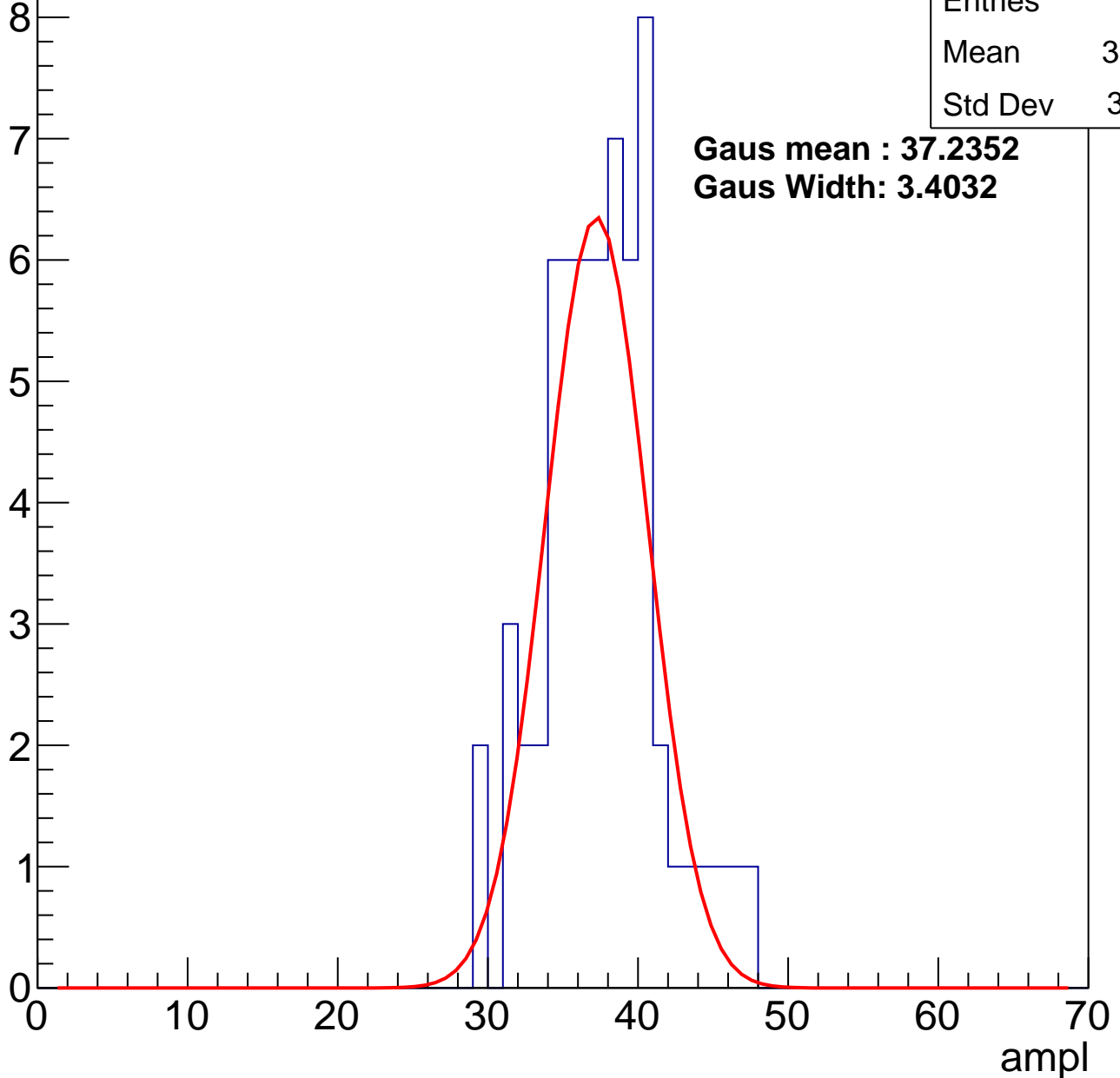
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	37.13
Std Dev	3.791

**Gaus mean : 37.2352**

**Gaus Width: 3.4032**



# B1L103S, U9-ch125, adc2

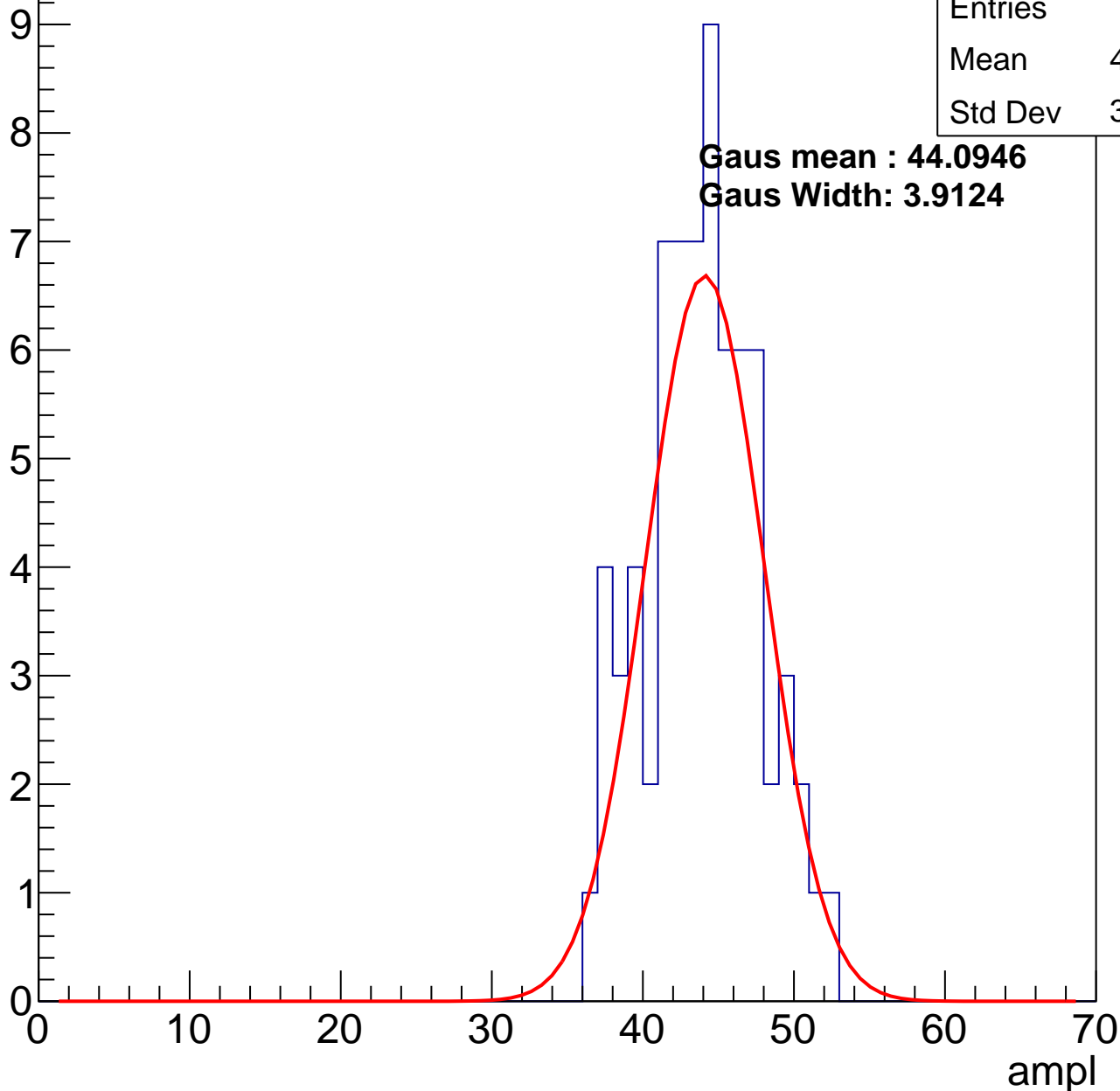
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	71
Mean	43.46
Std Dev	3.665

**Gaus mean : 44.0946**

**Gaus Width: 3.9124**

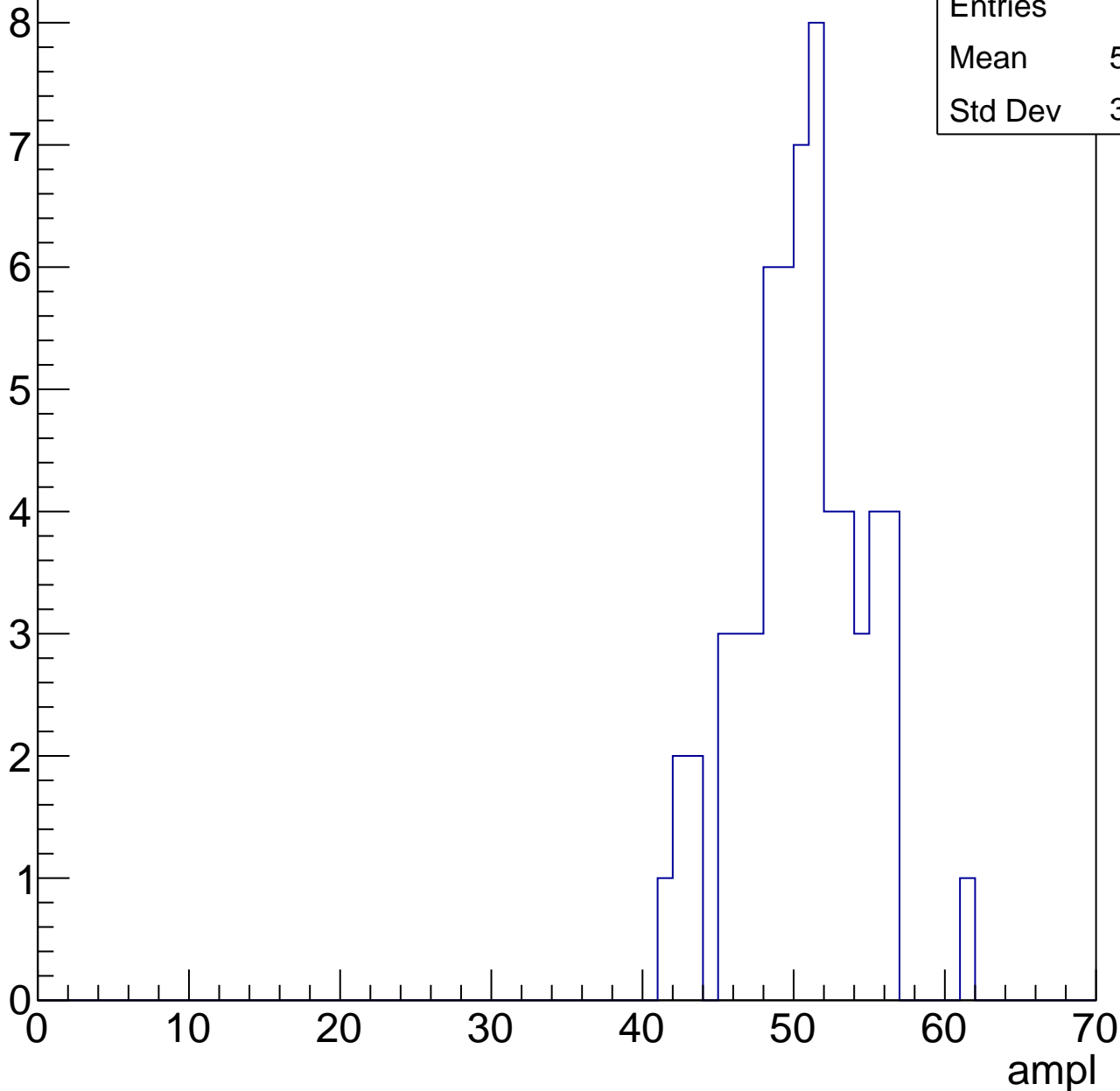


# B1L103S, U9-ch125, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	61
Mean	50.03
Std Dev	3.967

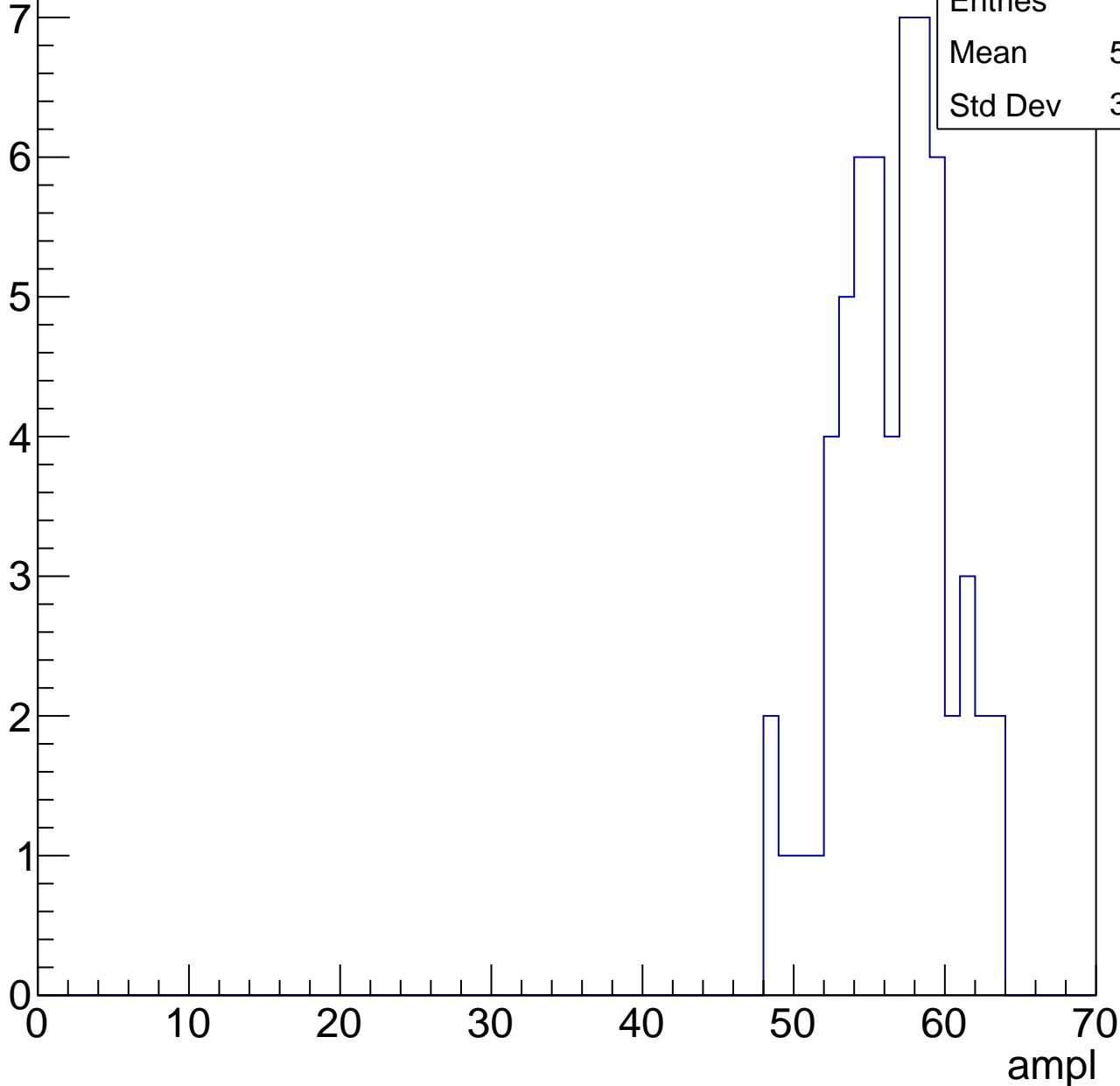


# B1L103S, U9-ch125, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	59
Mean	56.08
Std Dev	3.548

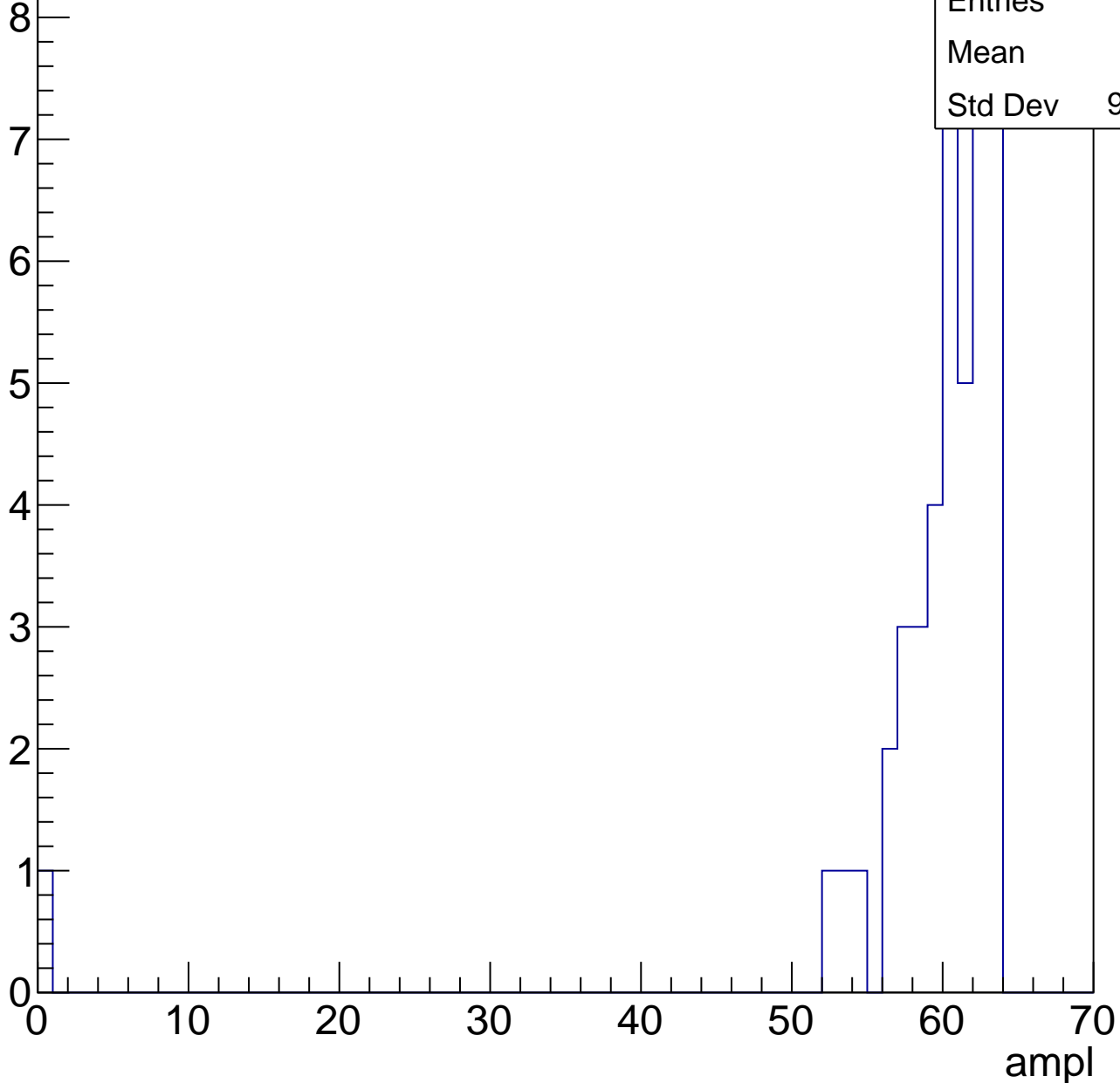


# B1L103S, U9-ch125, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	45
Mean	58.6
Std Dev	9.243



# B1L103S, U9-ch125, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U9-ch125, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U9-ch126, adc0

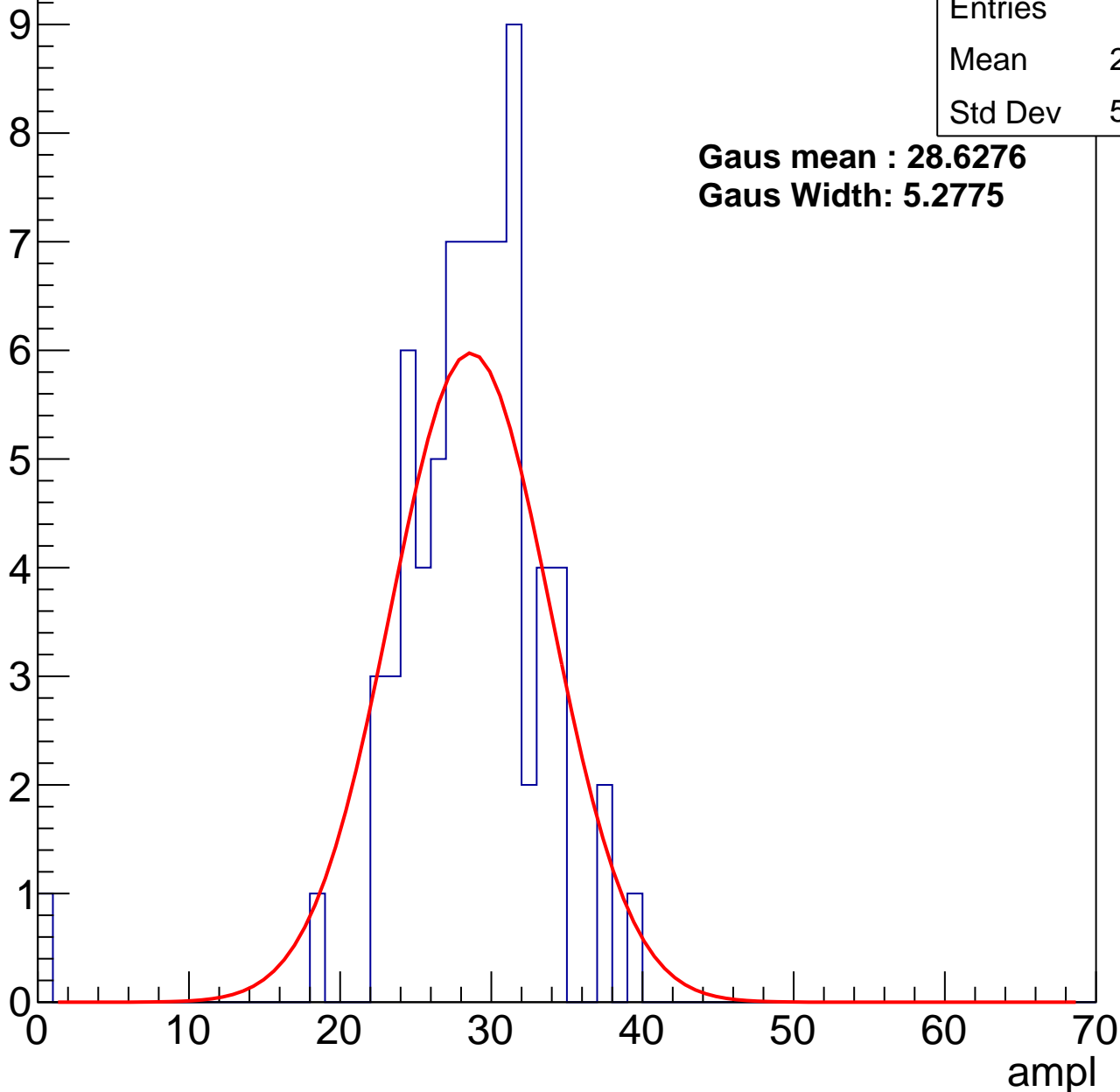
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	73
Mean	28.07
Std Dev	5.103

**Gaus mean : 28.6276**

**Gaus Width: 5.2775**



# B1L103S, U9-ch126, adc1

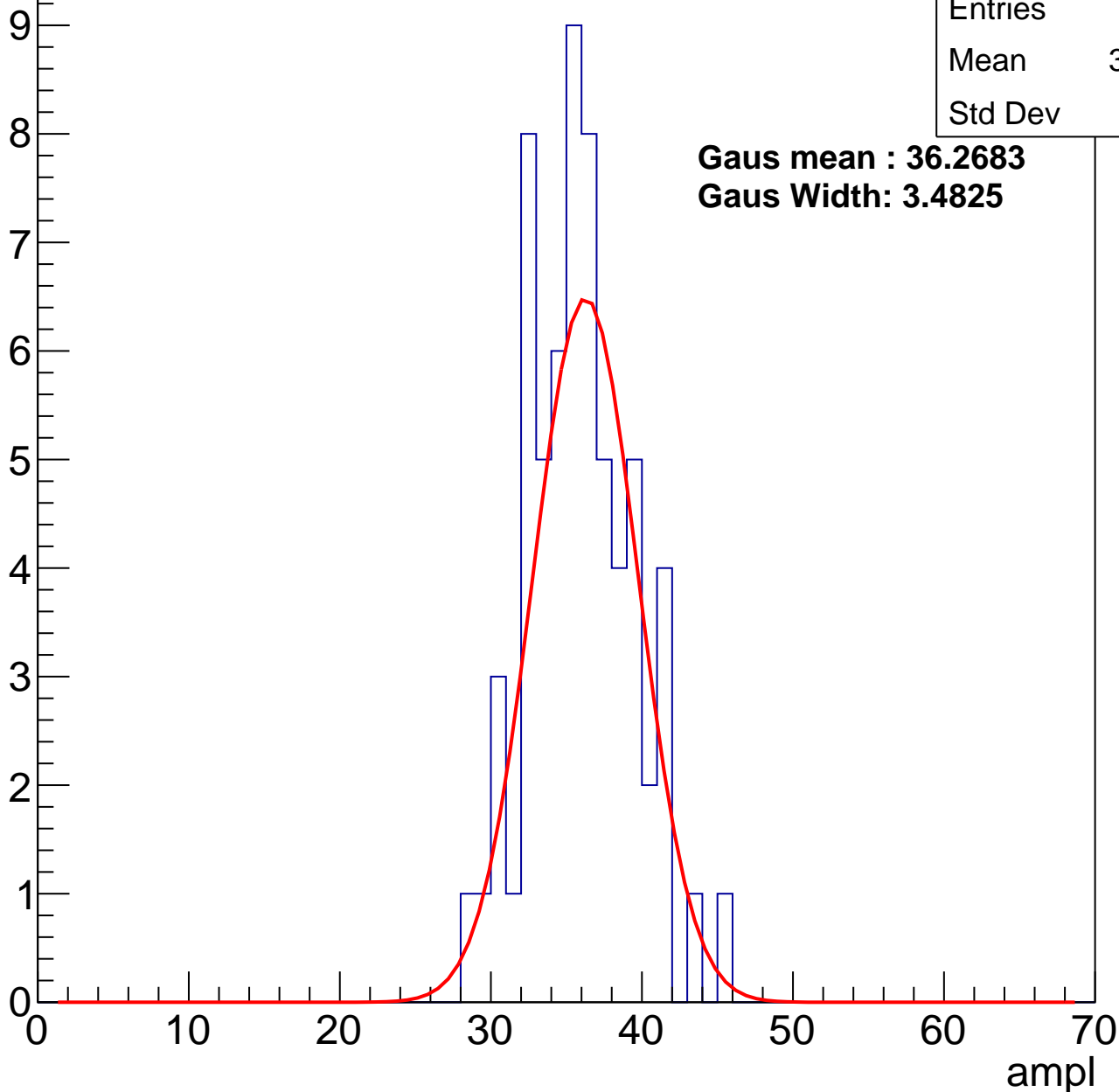
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	35.47
Std Dev	3.45

**Gaus mean : 36.2683**

**Gaus Width: 3.4825**



# B1L103S, U9-ch126, adc2

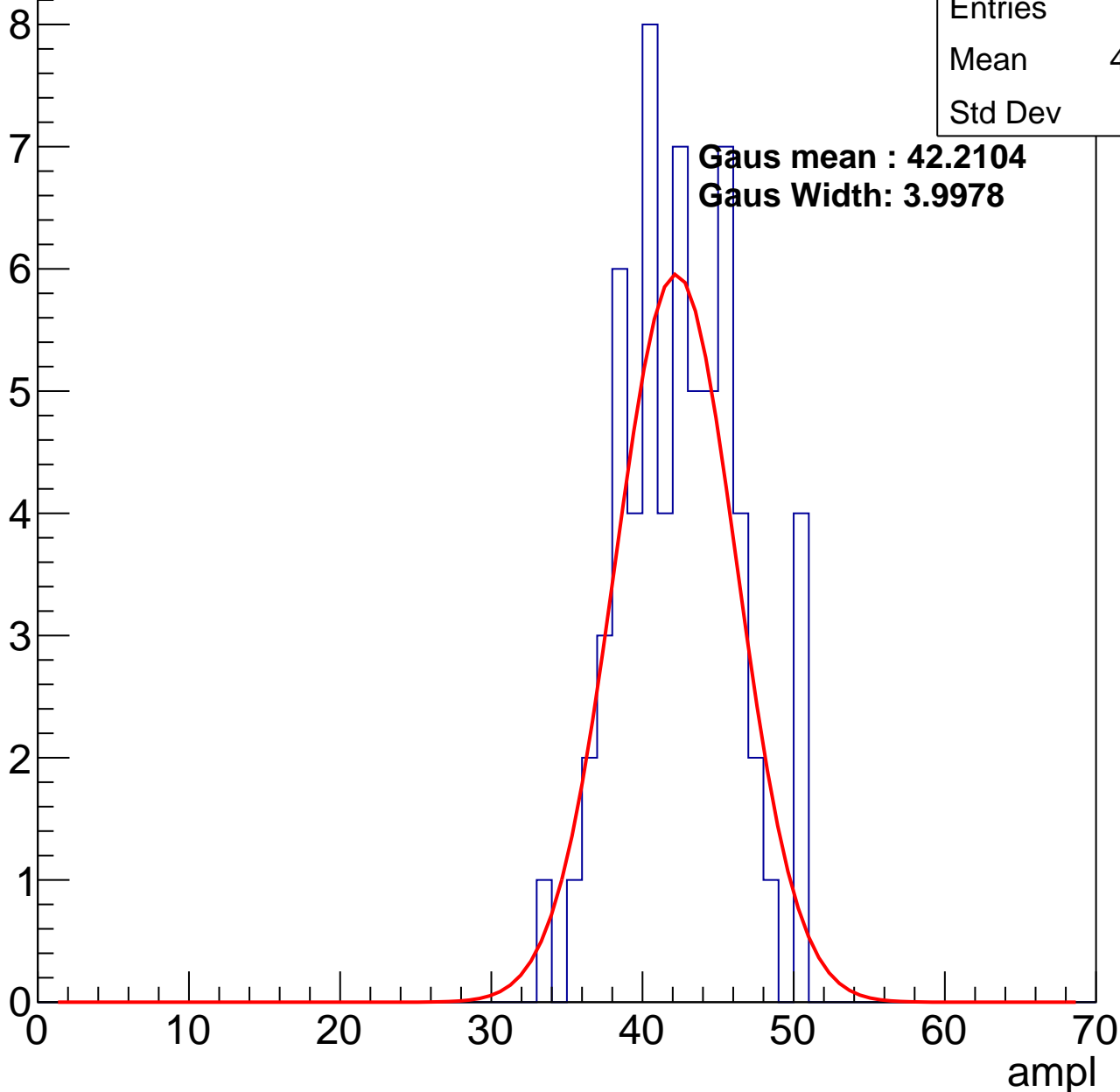
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	42.02
Std Dev	3.83

**Gaus mean : 42.2104**

**Gaus Width: 3.9978**

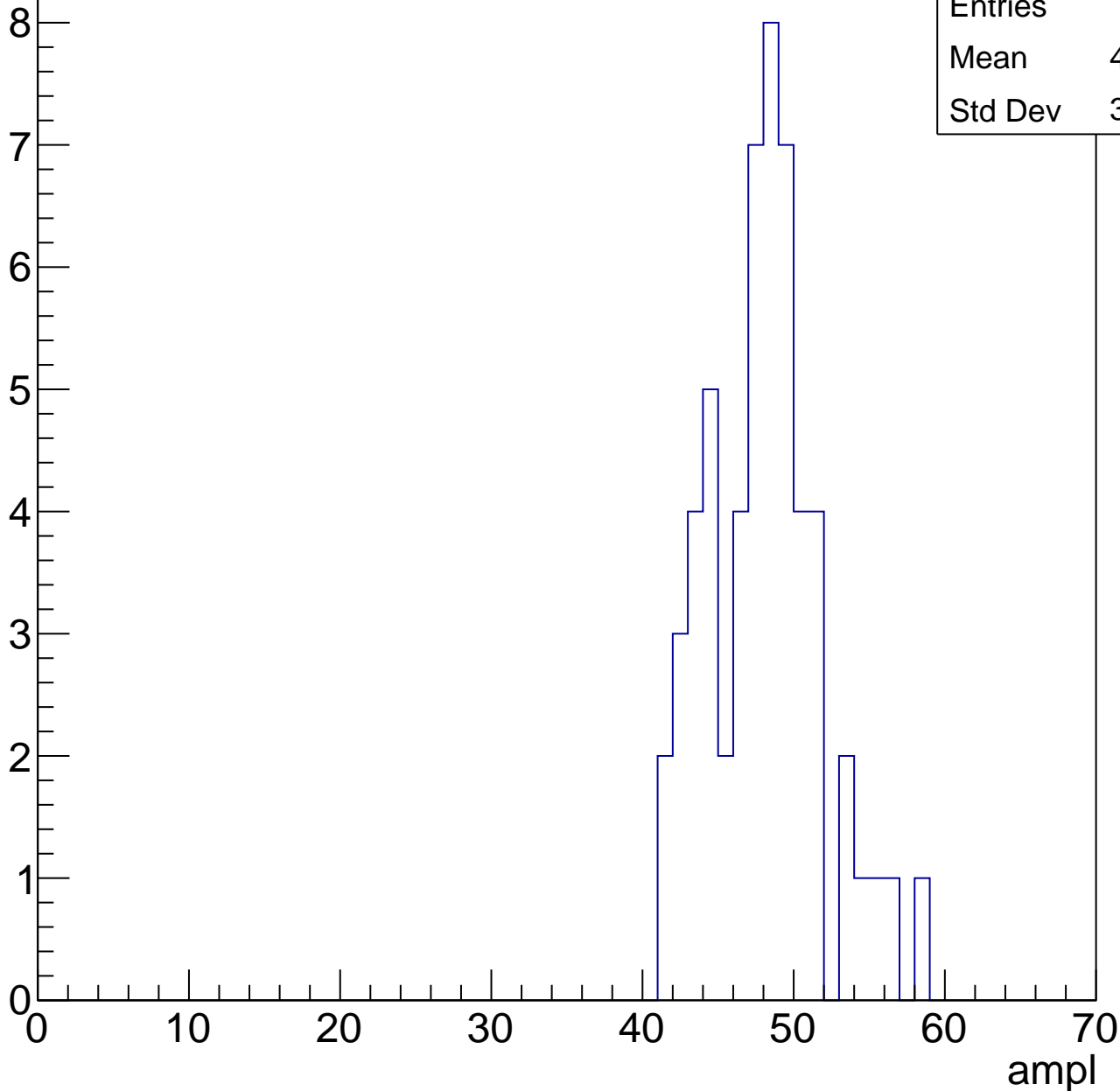


# B1L103S, U9-ch126, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	56
Mean	47.55
Std Dev	3.717

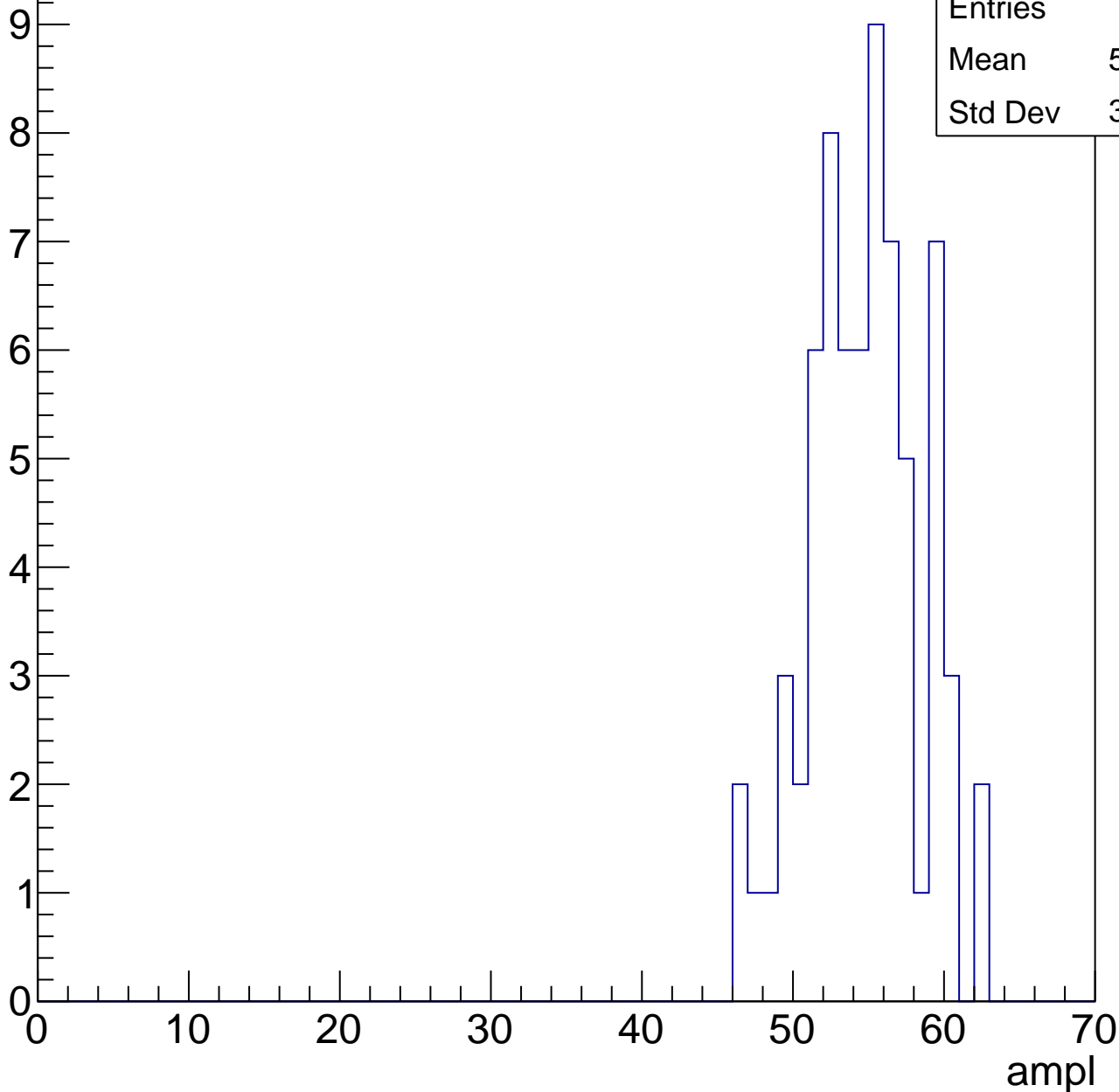


# B1L103S, U9-ch126, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	69
Mean	54.28
Std Dev	3.643

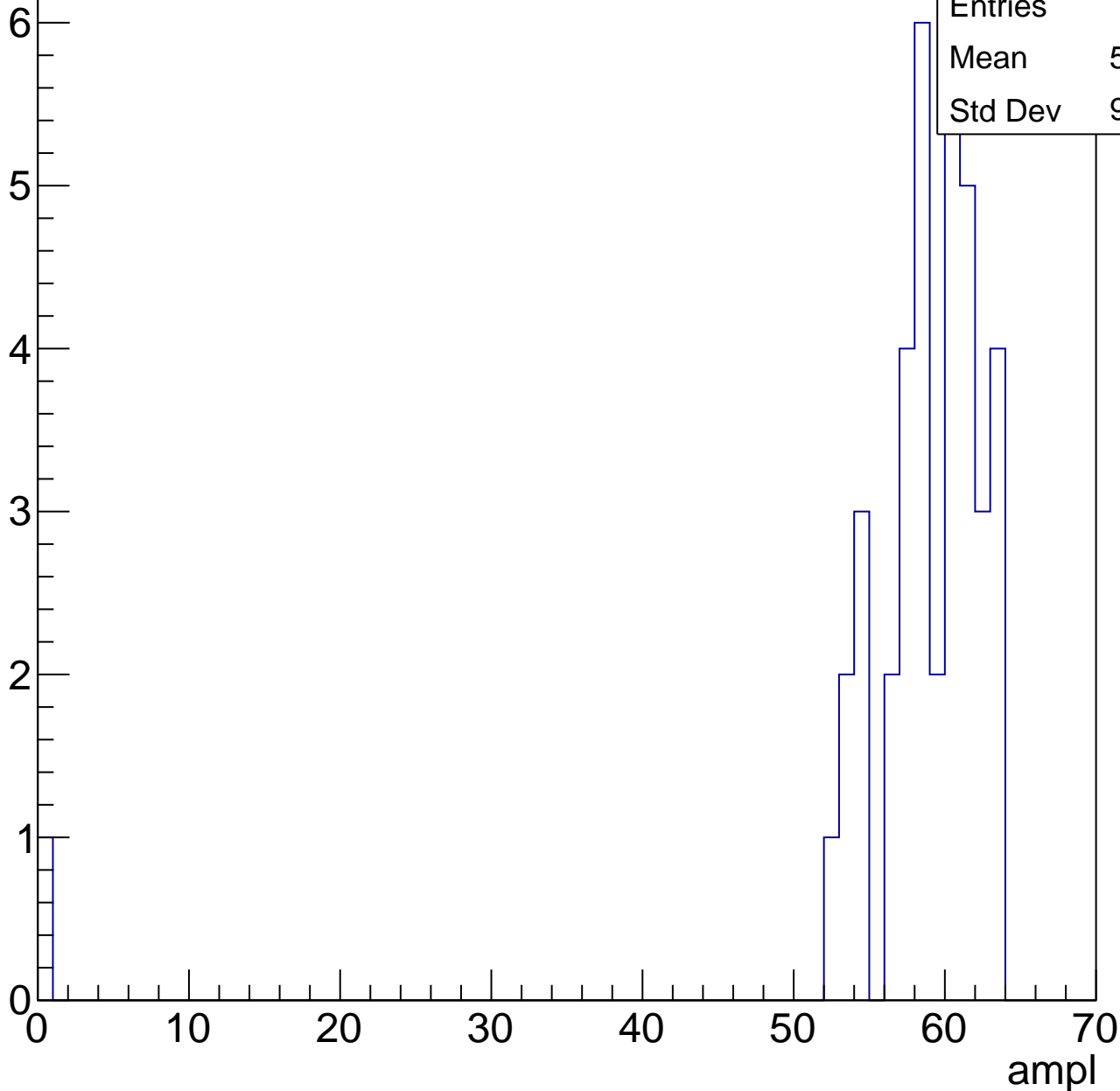


# B1L103S, U9-ch126, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	39
Mean	57.15
Std Dev	9.742

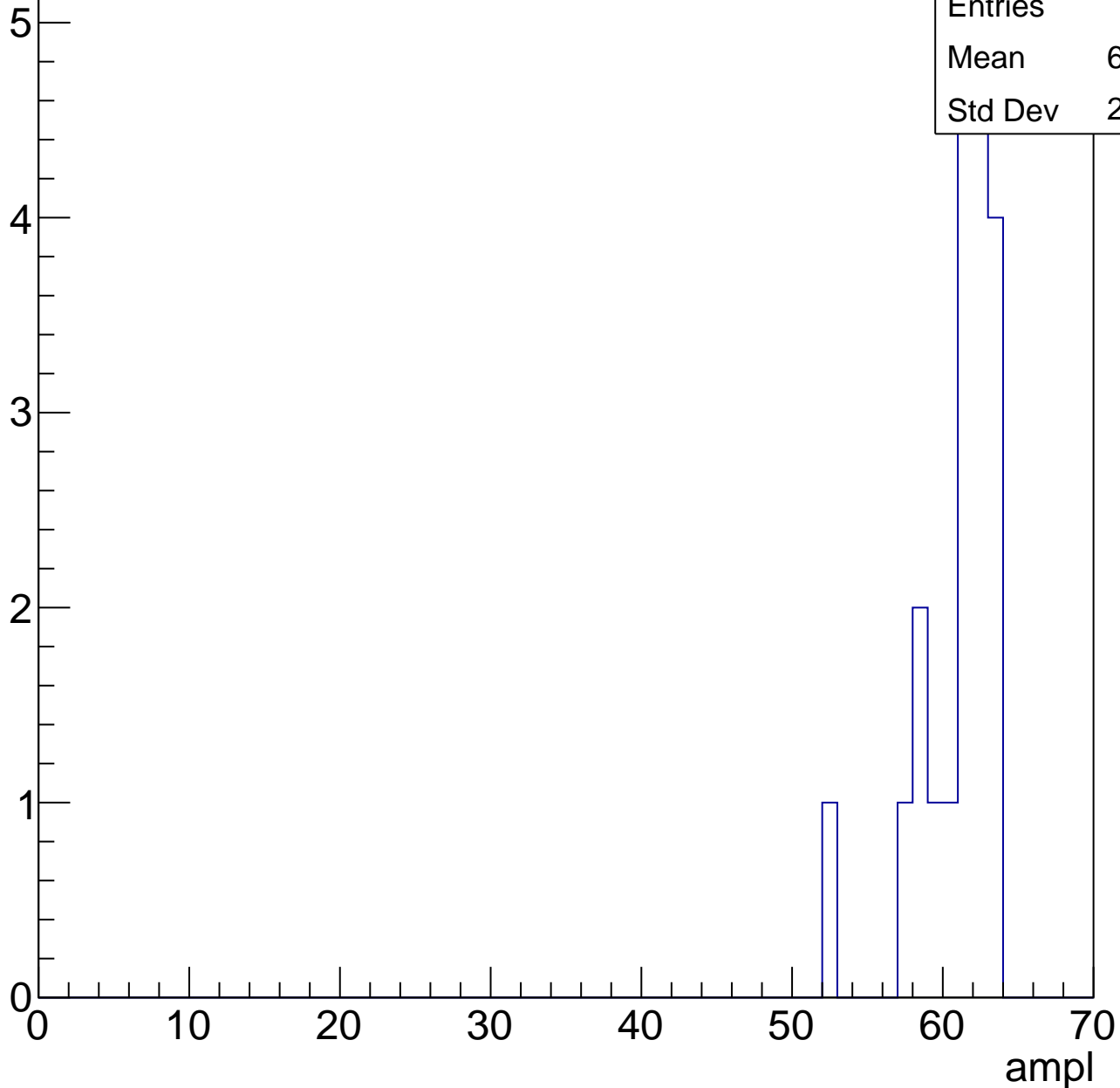


# B1L103S, U9-ch126, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	20
Mean	60.55
Std Dev	2.617





# B1L103S, U9-ch126, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U9-ch127, adc0

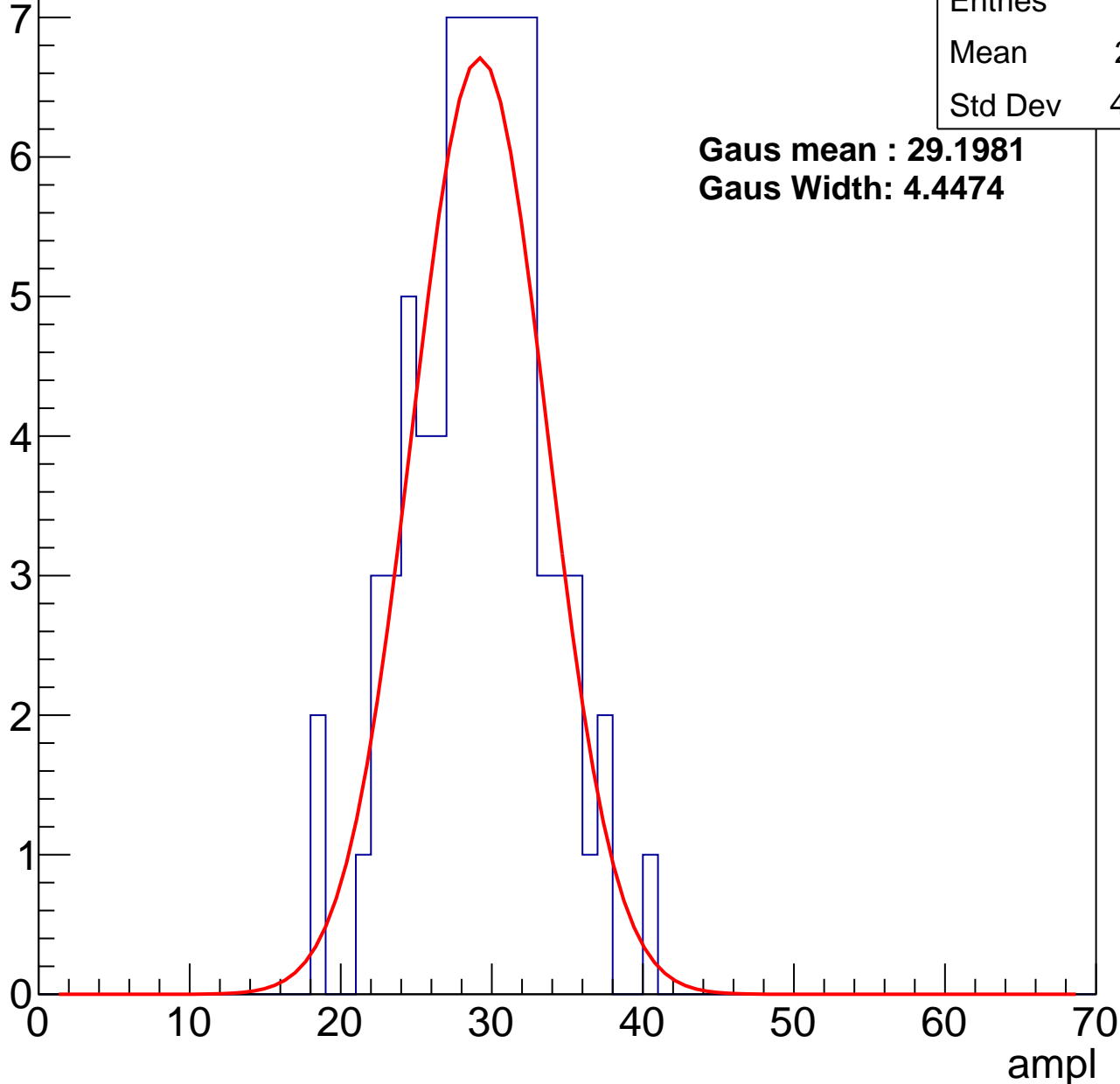
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	77
Mean	28.71
Std Dev	4.327

**Gaus mean : 29.1981**

**Gaus Width: 4.4474**



# B1L103S, U9-ch127, adc1

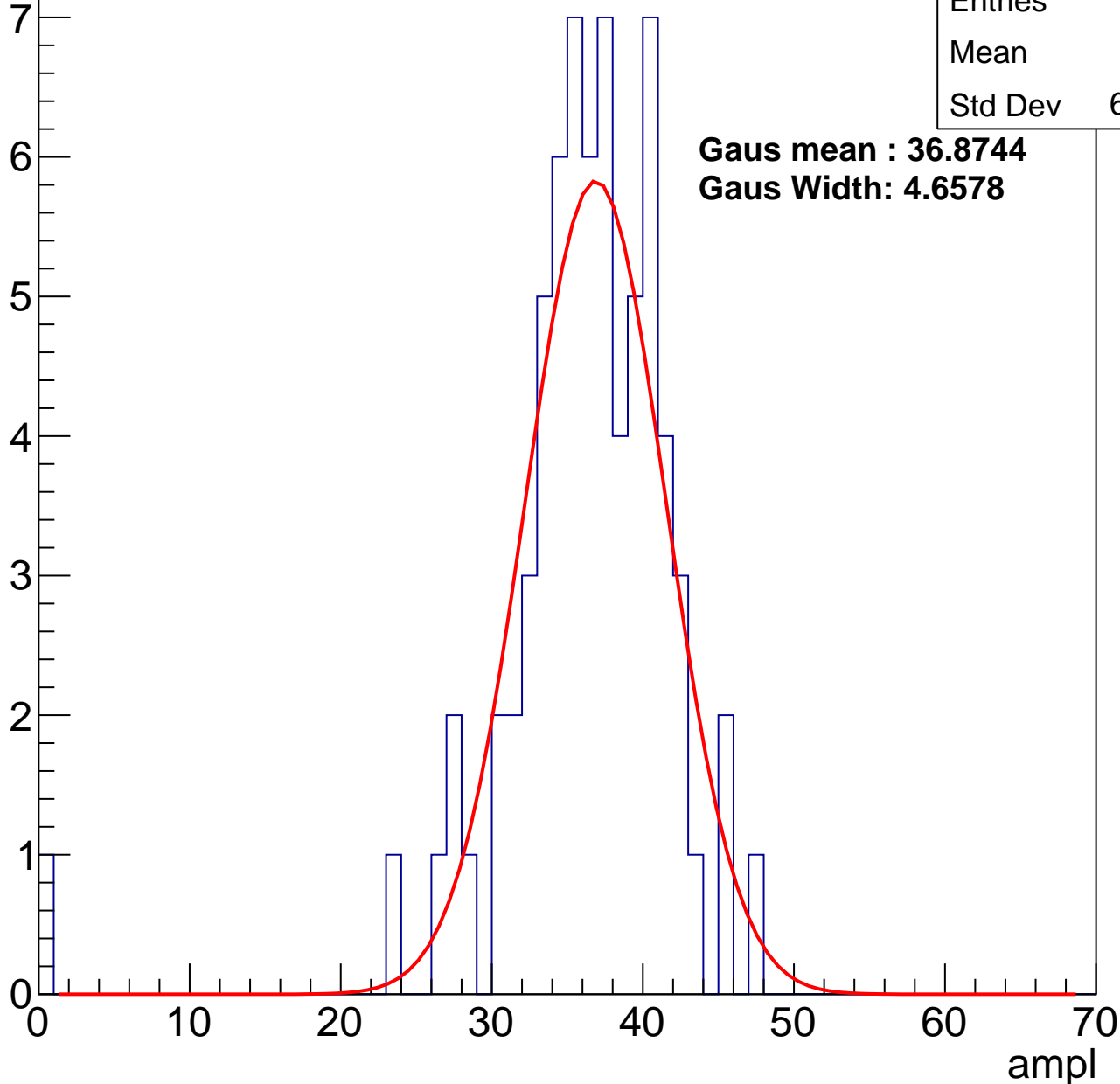
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	71
Mean	35.7
Std Dev	6.224

**Gaus mean : 36.8744**

**Gaus Width: 4.6578**



# B1L103S, U9-ch127, adc2

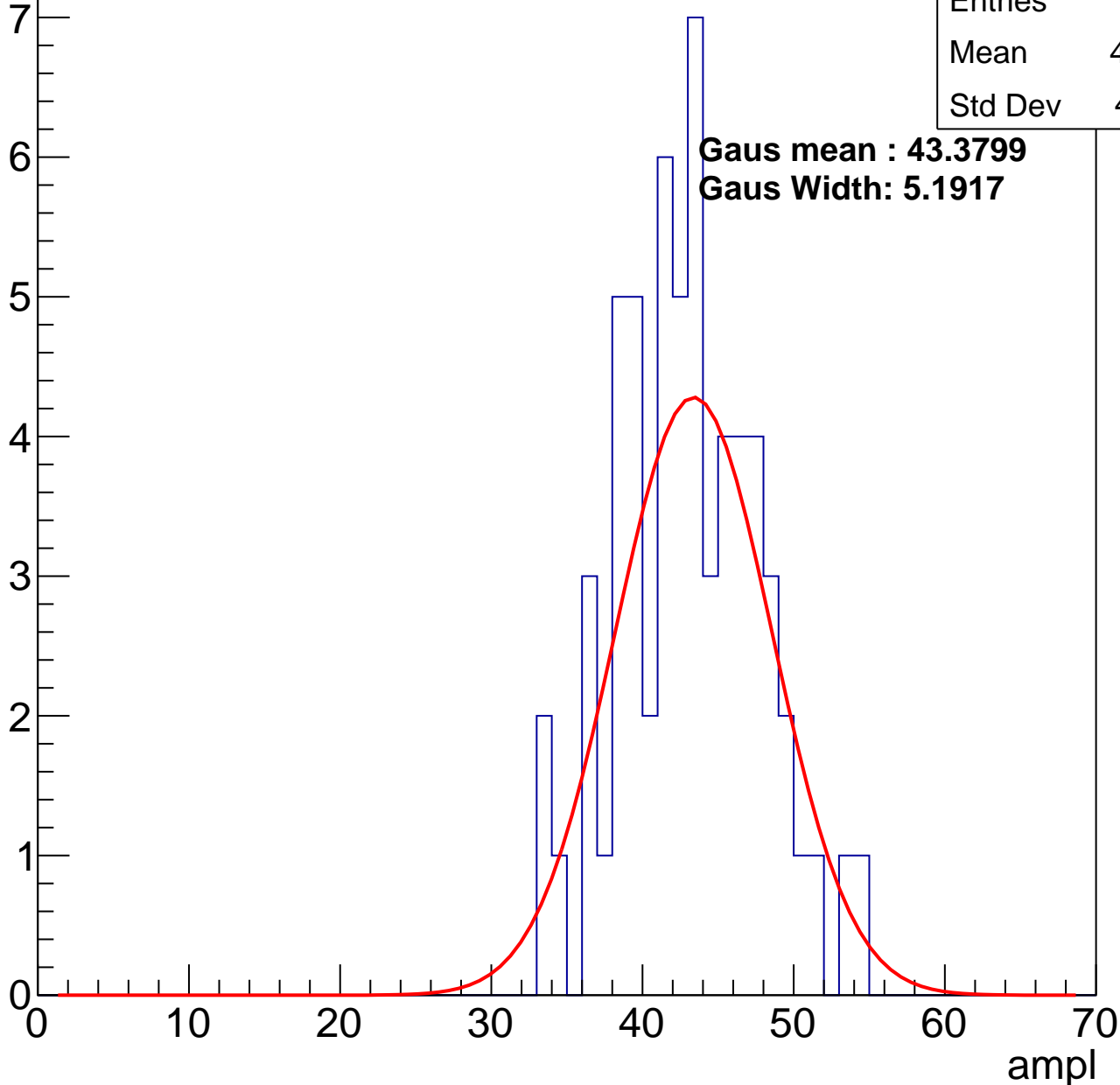
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	61
Mean	42.64
Std Dev	4.631

**Gaus mean : 43.3799**

**Gaus Width: 5.1917**

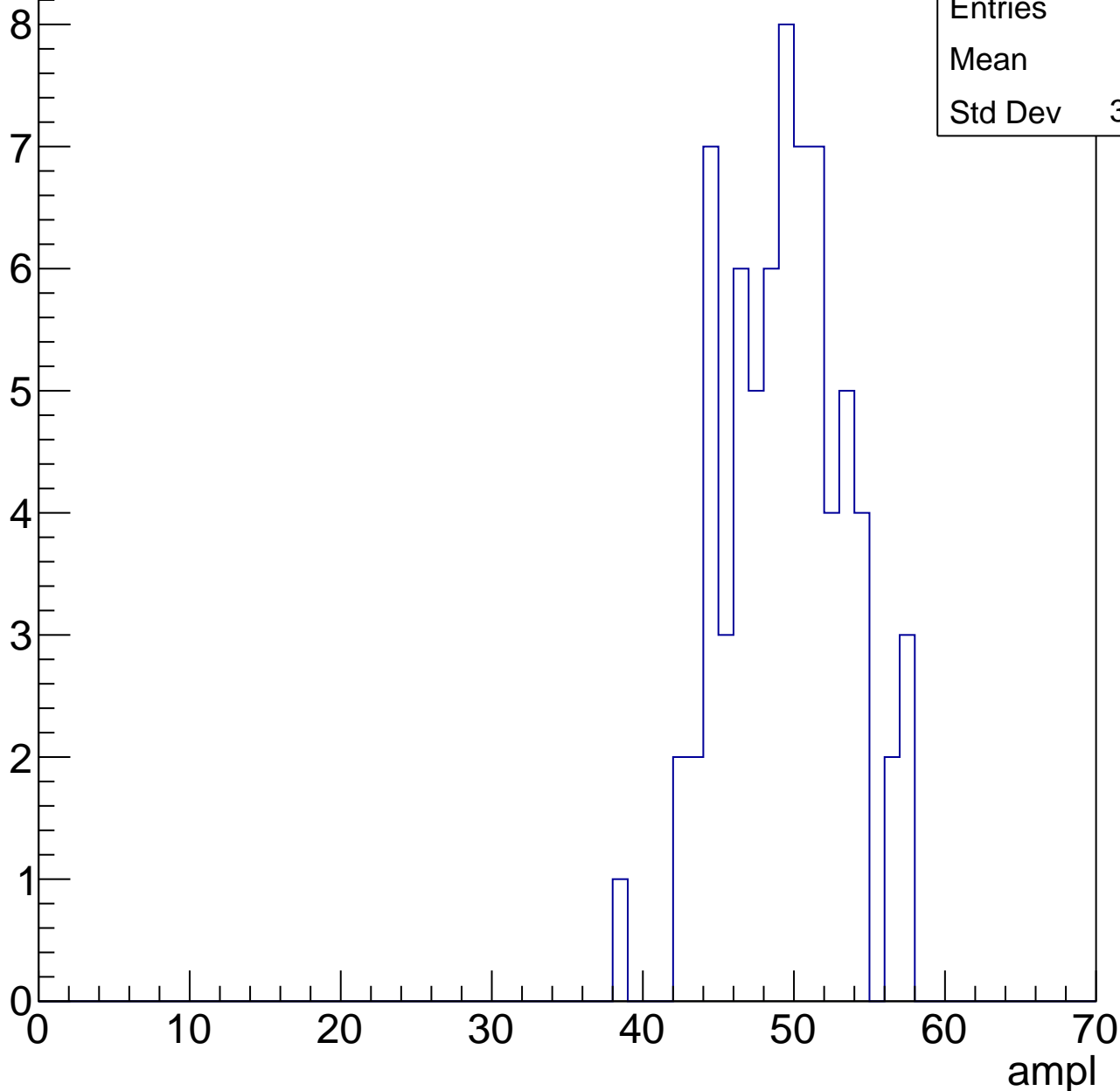


# B1L103S, U9-ch127, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	72
Mean	48.9
Std Dev	3.969

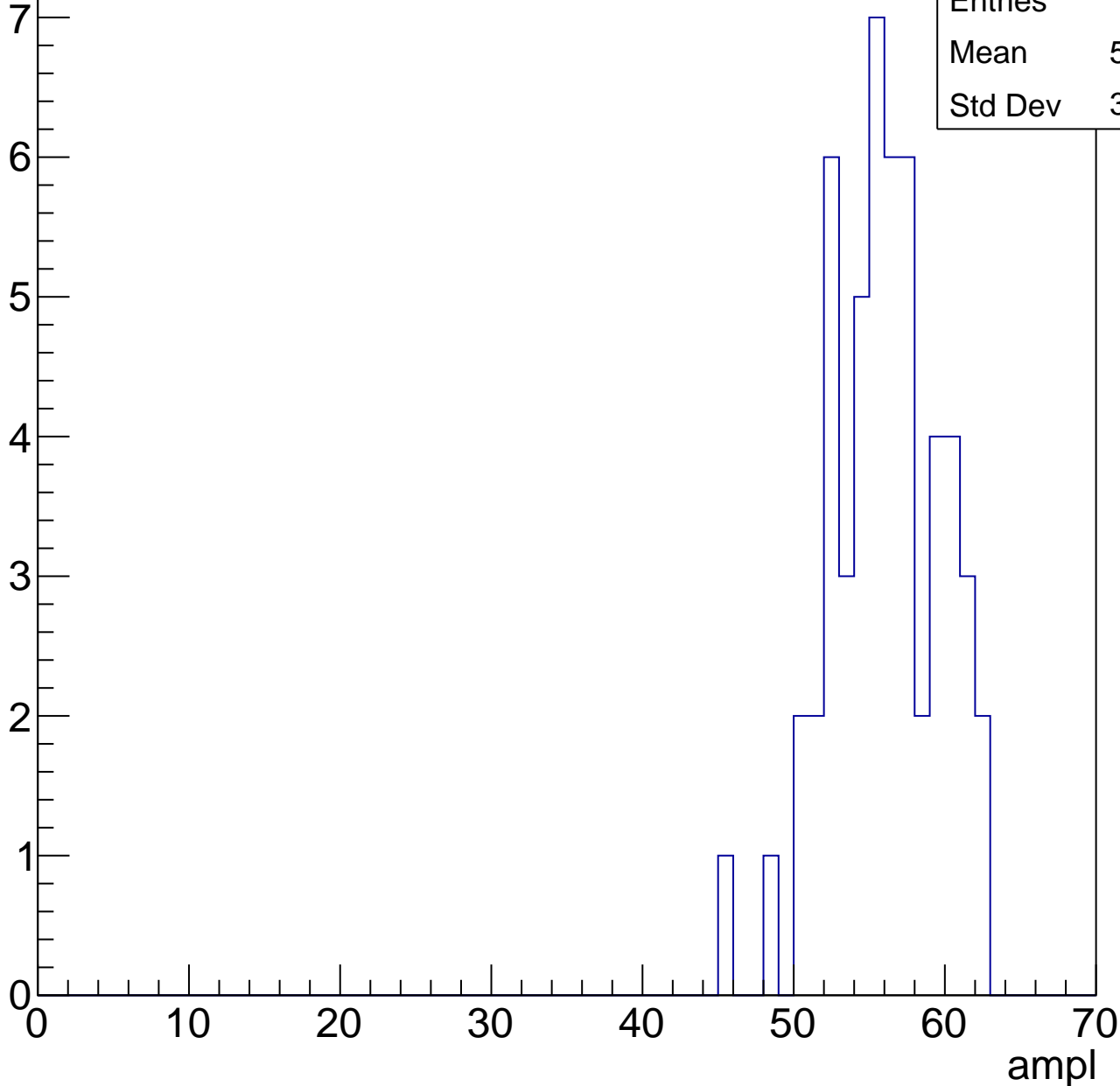


# B1L103S, U9-ch127, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	54
Mean	55.52
Std Dev	3.614

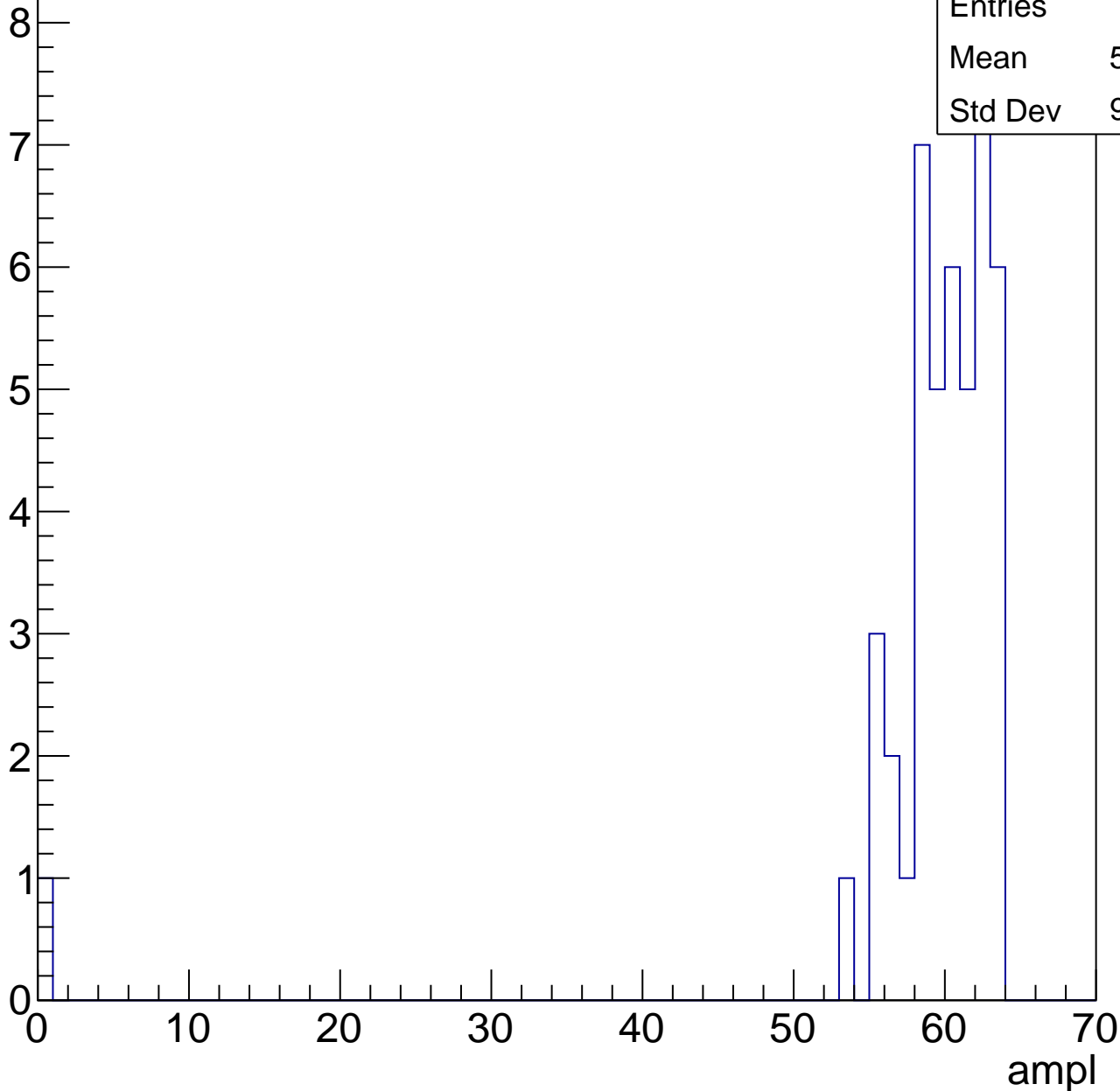


# B1L103S, U9-ch127, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

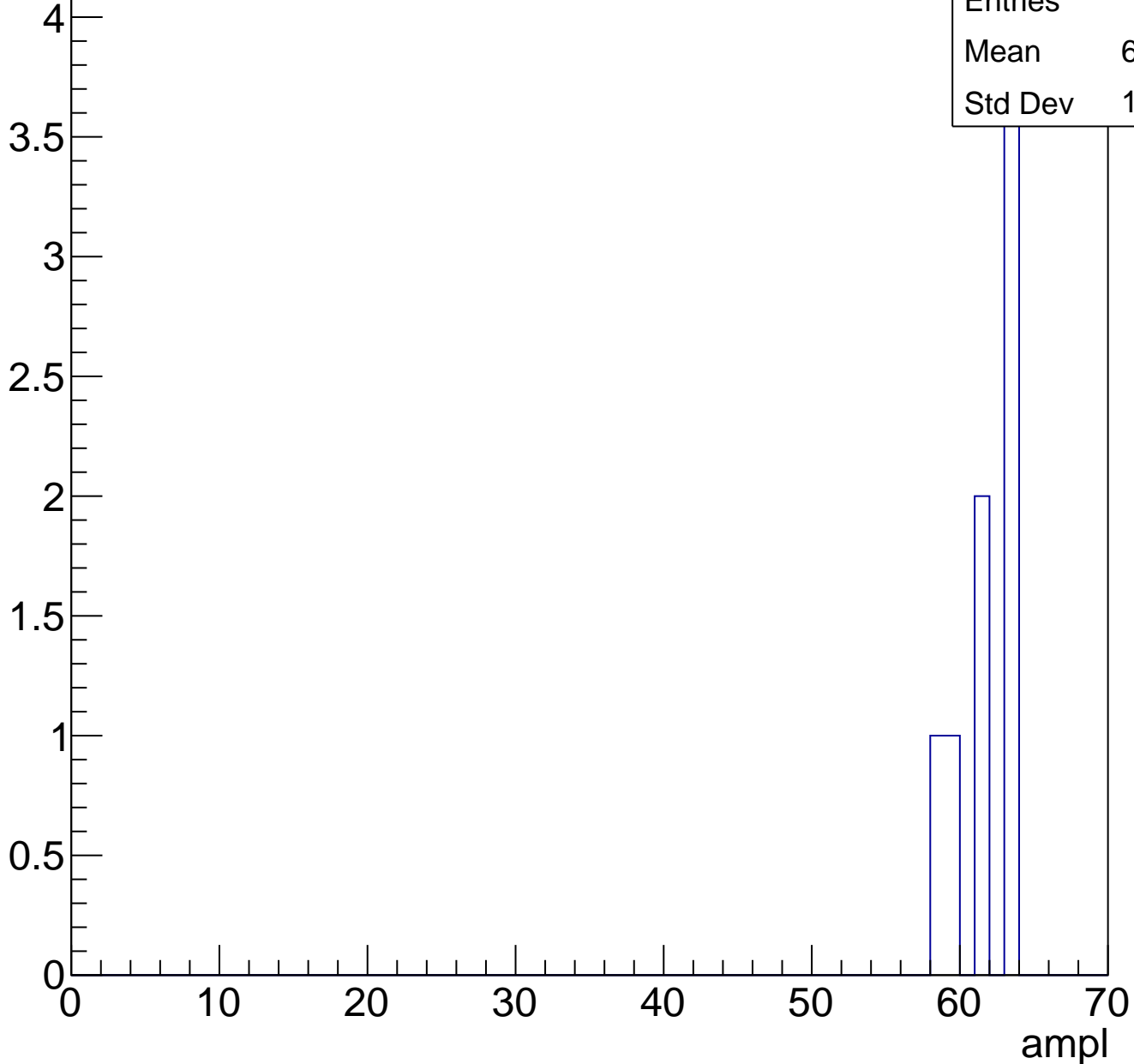
Entries	45
Mean	58.38
Std Dev	9.154



# B1L103S, U9-ch127, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U9-ch127, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L103S, U9-ch127, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

