



# B1L103S, U26-ch0, adc0

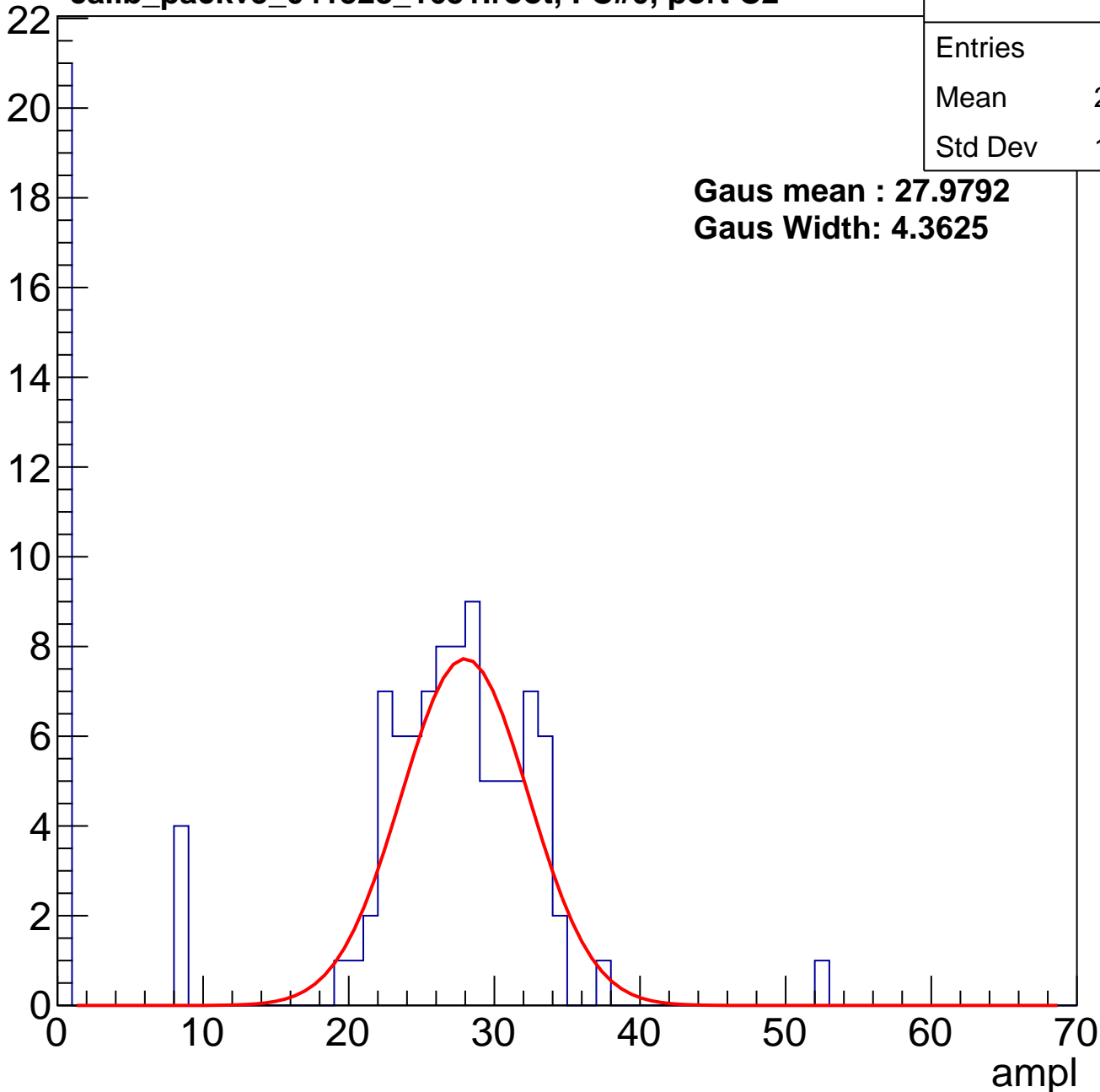
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	112
Mean	21.69
Std Dev	11.77

**Gaus mean : 27.9792**

**Gaus Width: 4.3625**

Entry



# B1L103S, U26-ch0, adc1

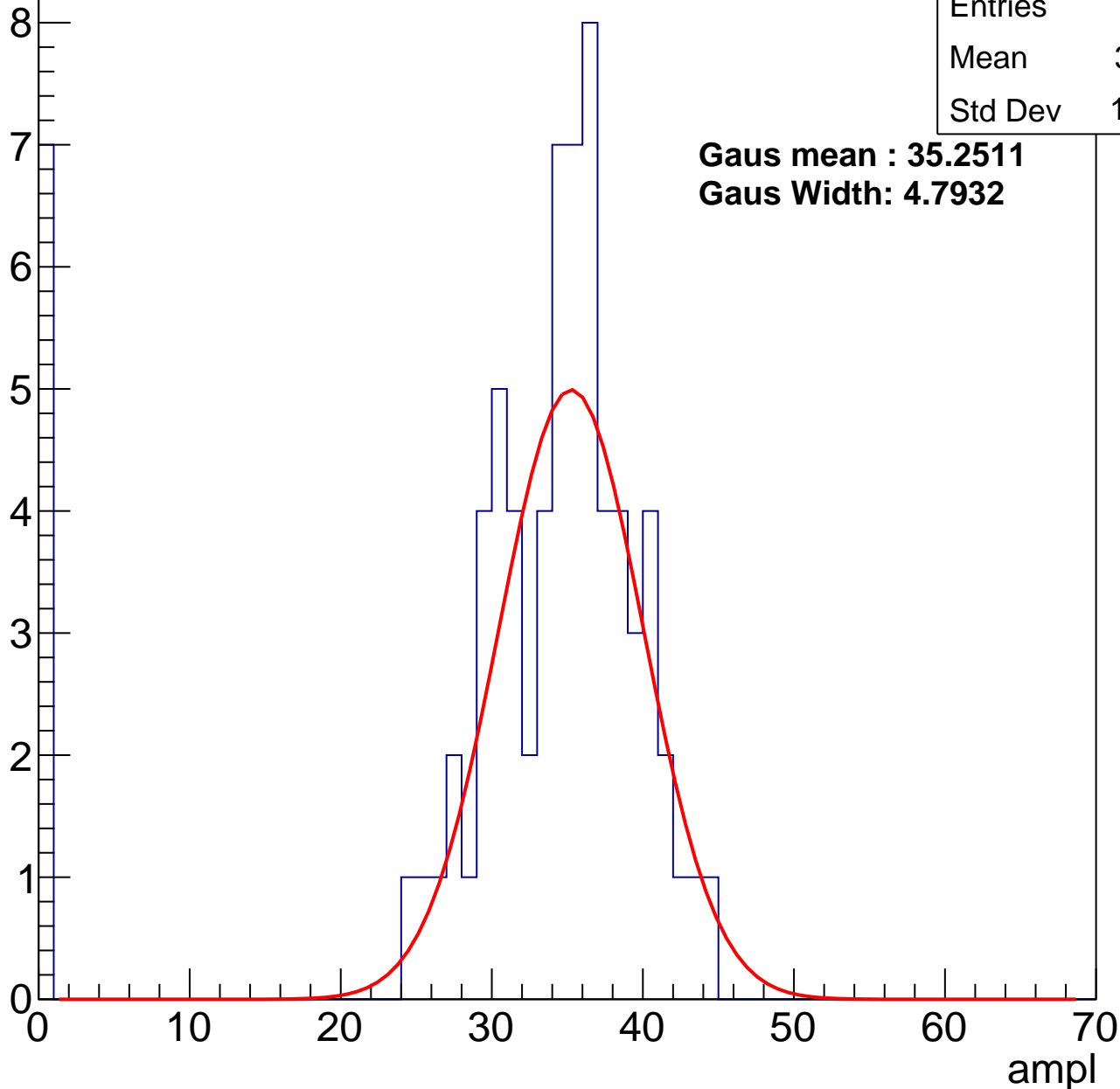
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	74
Mean	31.11
Std Dev	10.89

**Gaus mean : 35.2511**

**Gaus Width: 4.7932**



# B1L103S, U26-ch0, adc2

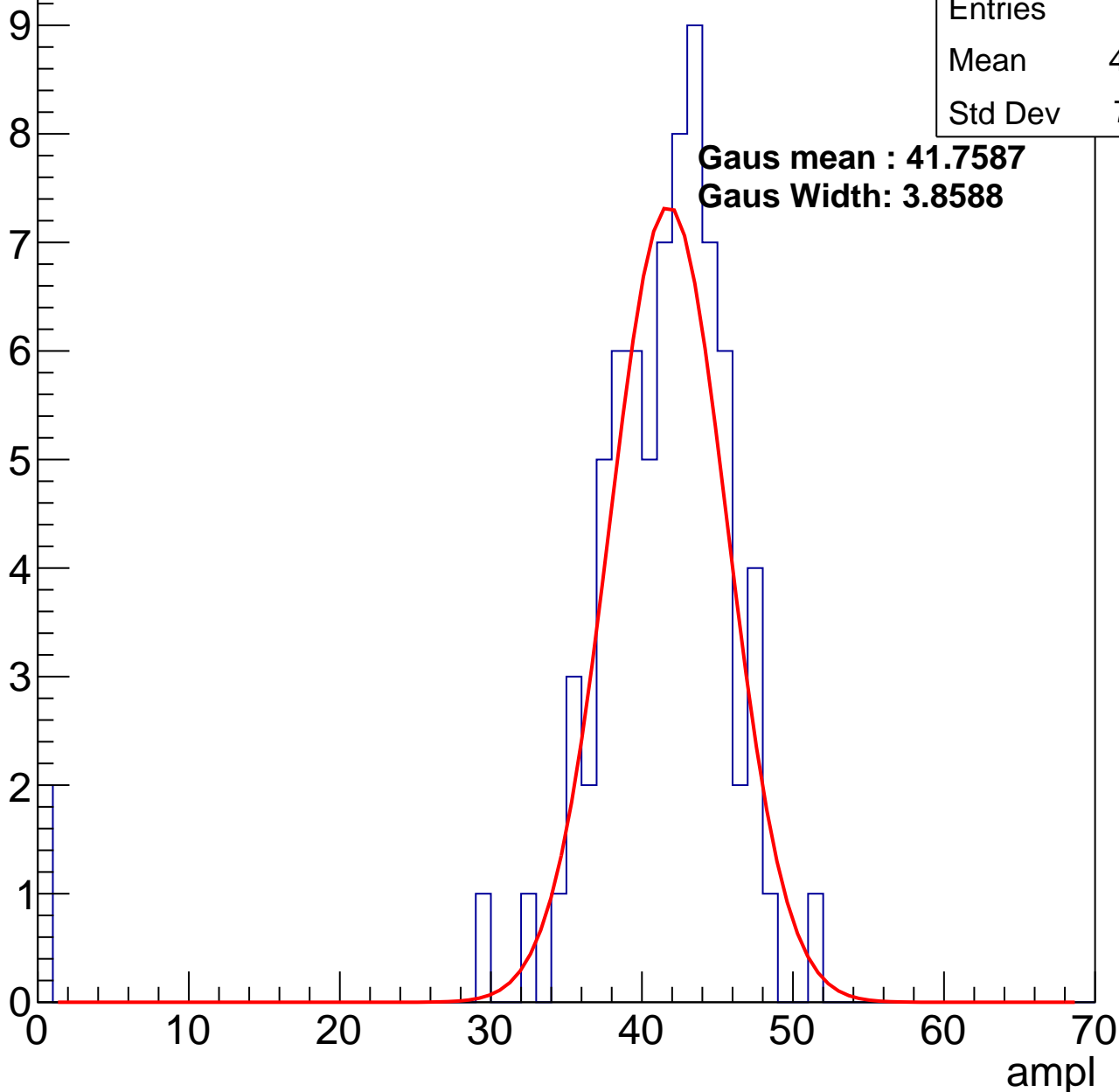
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	77
Mean	40.08
Std Dev	7.591

**Gaus mean : 41.7587**

**Gaus Width: 3.8588**

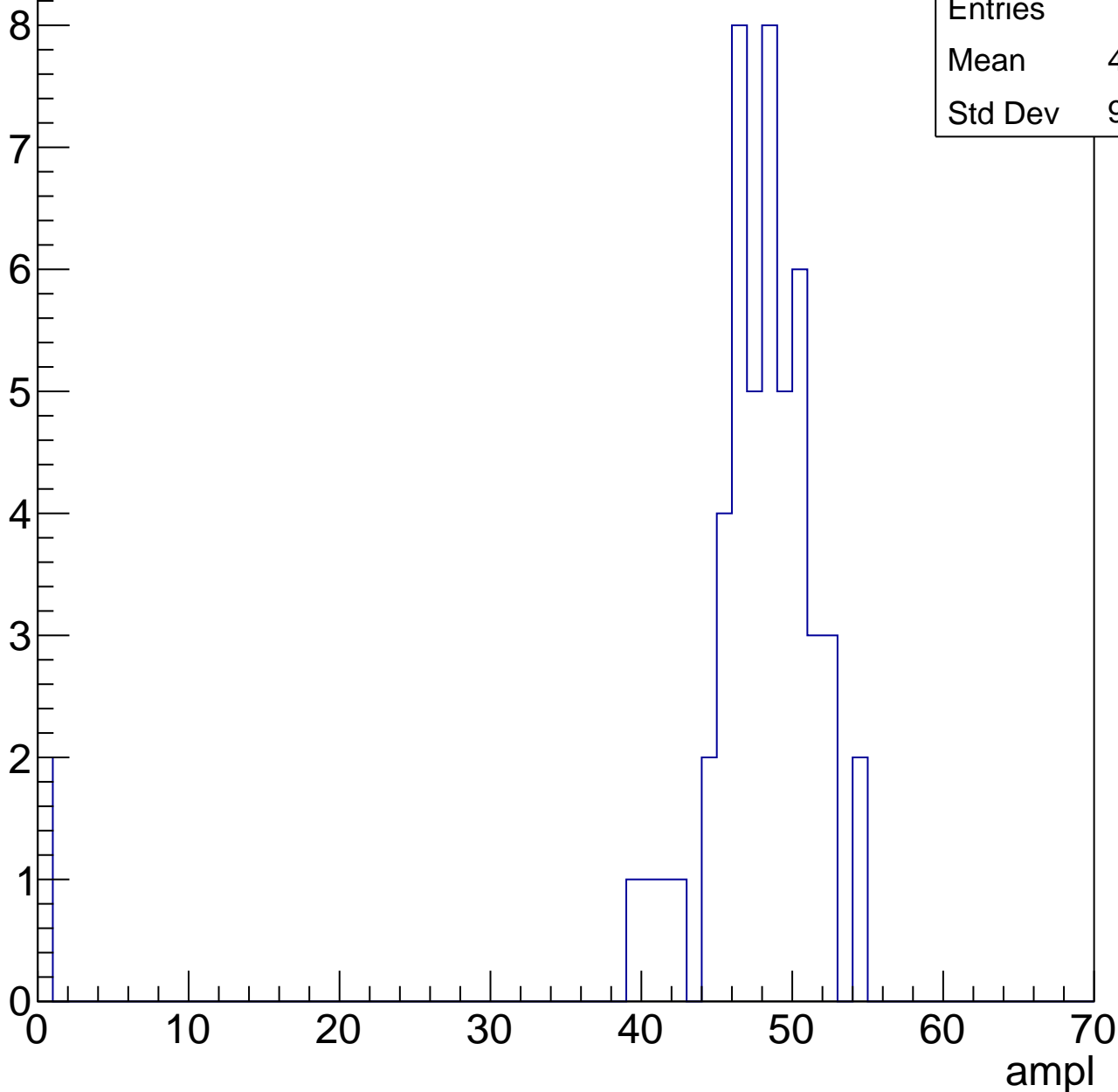


# B1L103S, U26-ch0, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	52
Mean	45.75
Std Dev	9.663

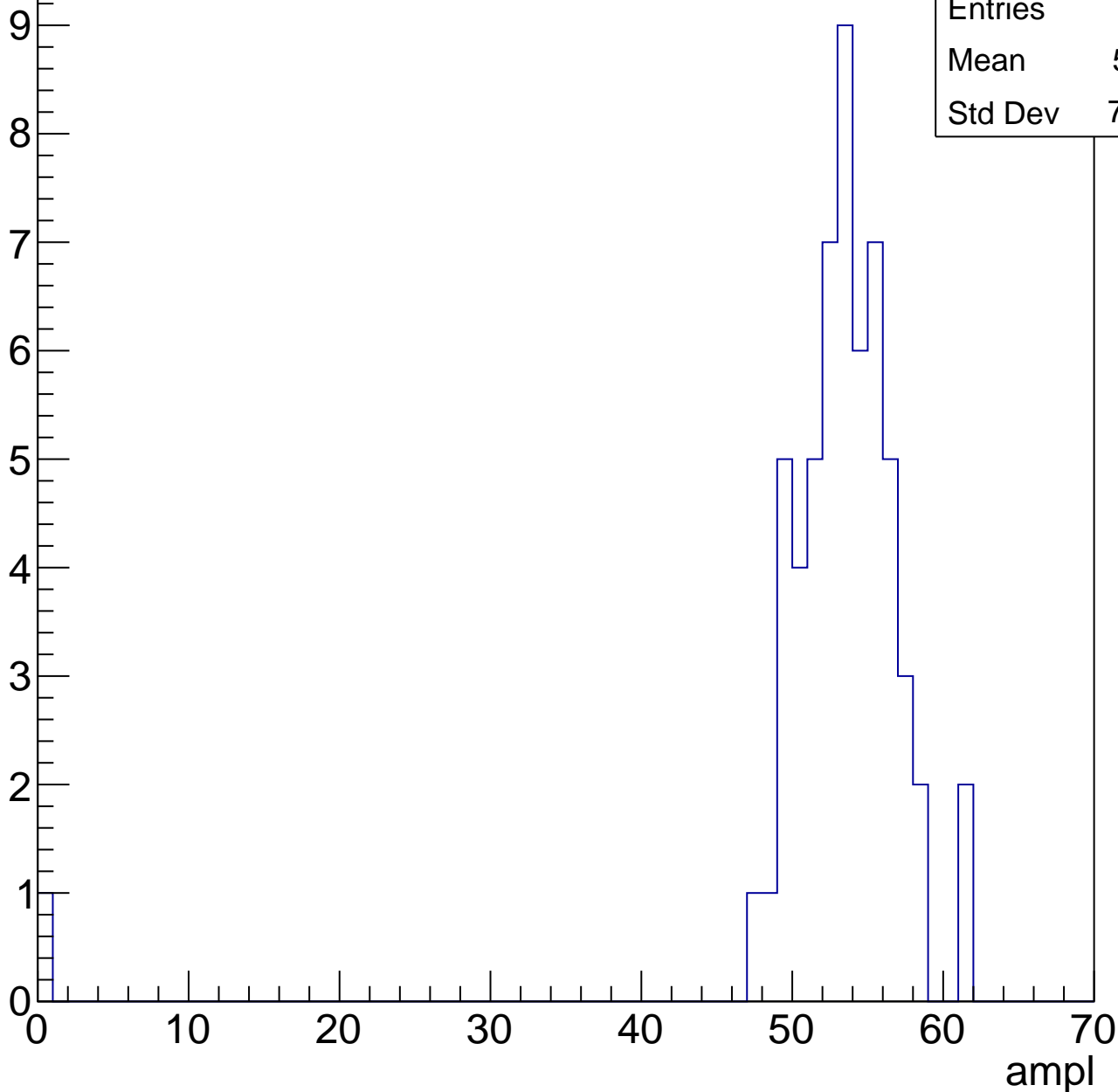


# B1L103S, U26-ch0, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	58
Mean	52.31
Std Dev	7.532

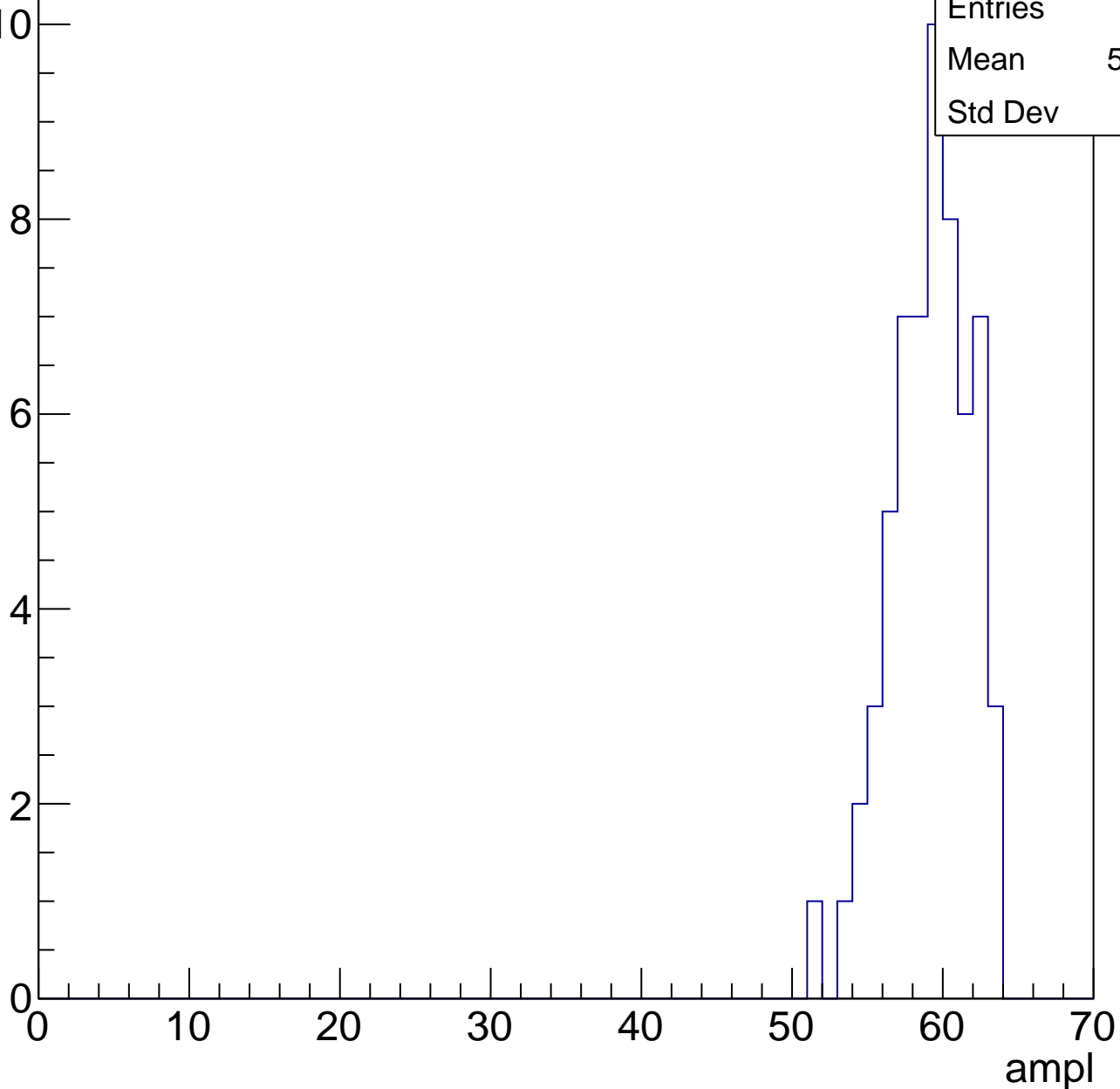


# B1L103S, U26-ch0, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	60
Mean	58.68
Std Dev	2.63

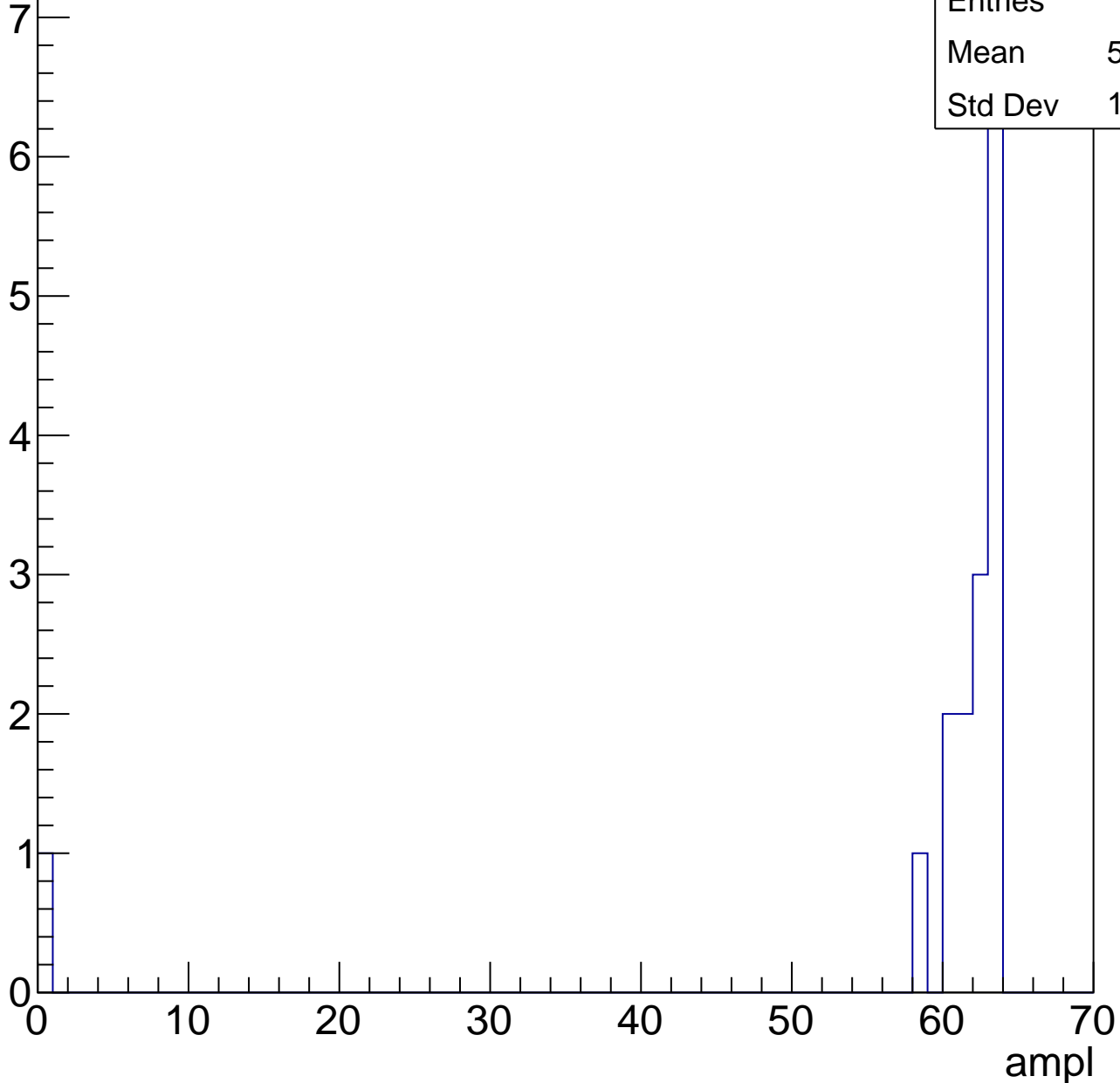


# B1L103S, U26-ch0, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	16
Mean	57.94
Std Dev	15.03



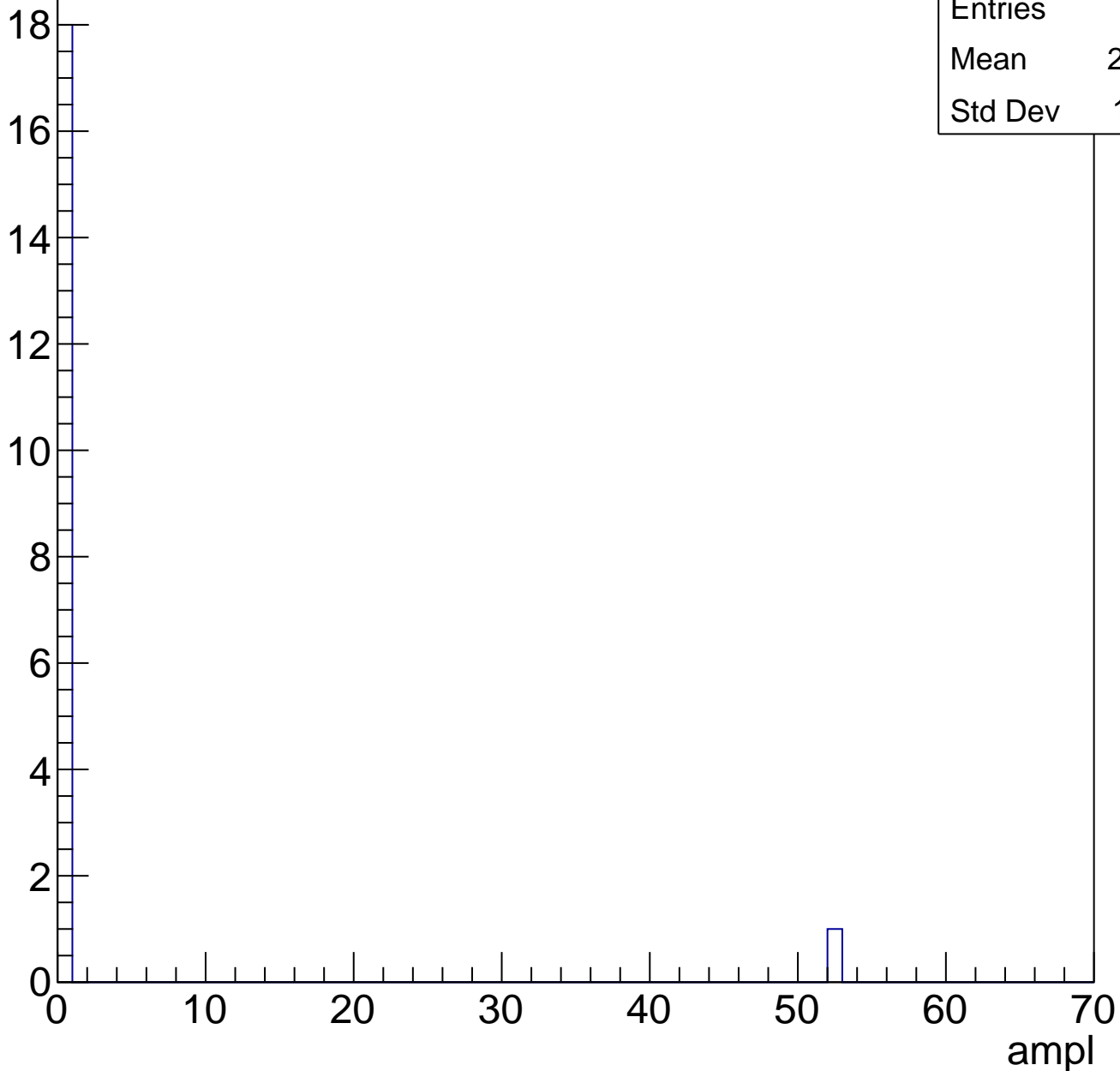


# B1L103S, U26-ch0, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	19
Mean	2.737
Std Dev	11.61

Entry



# B1L103S, U26-ch1, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	61
Mean	24.08
Std Dev	11.61

**Gaus mean : 29.8578**

**Gaus Width: 3.7143**

Entry

10

8

6

4

2

0

0

10

20

30

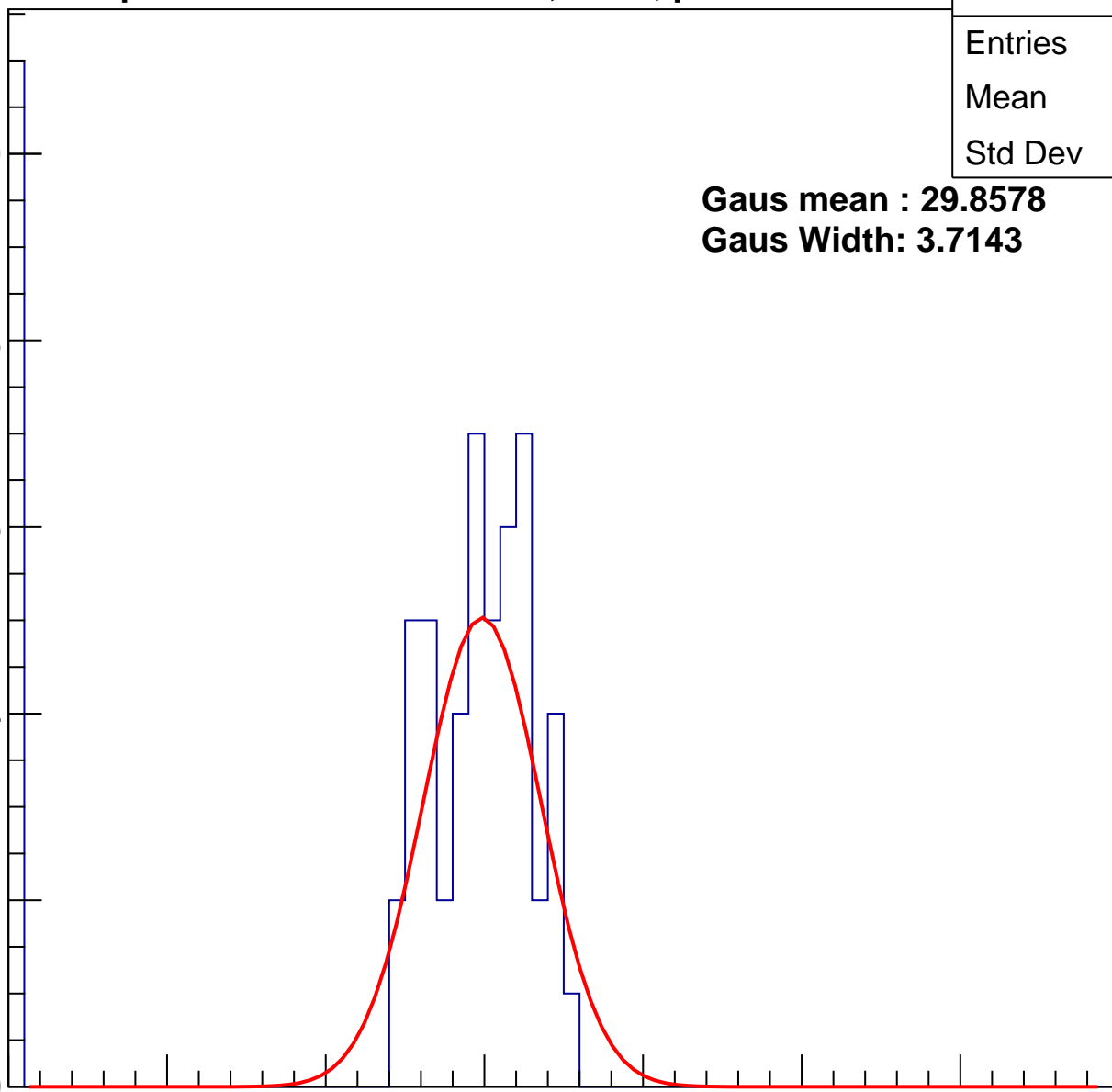
40

50

60

70

ampl



# B1L103S, U26-ch1, adc1

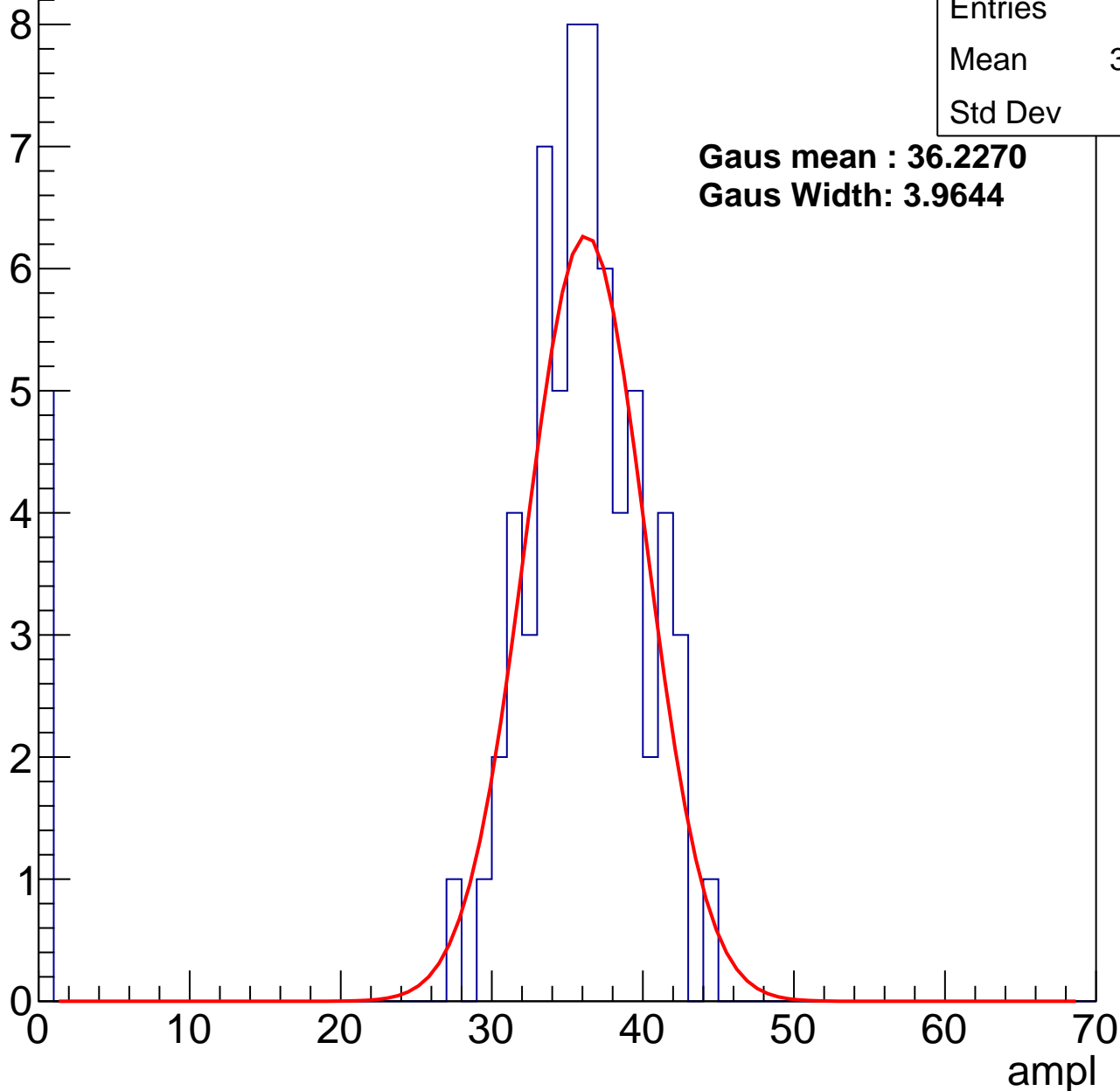
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	69
Mean	33.16
Std Dev	9.88

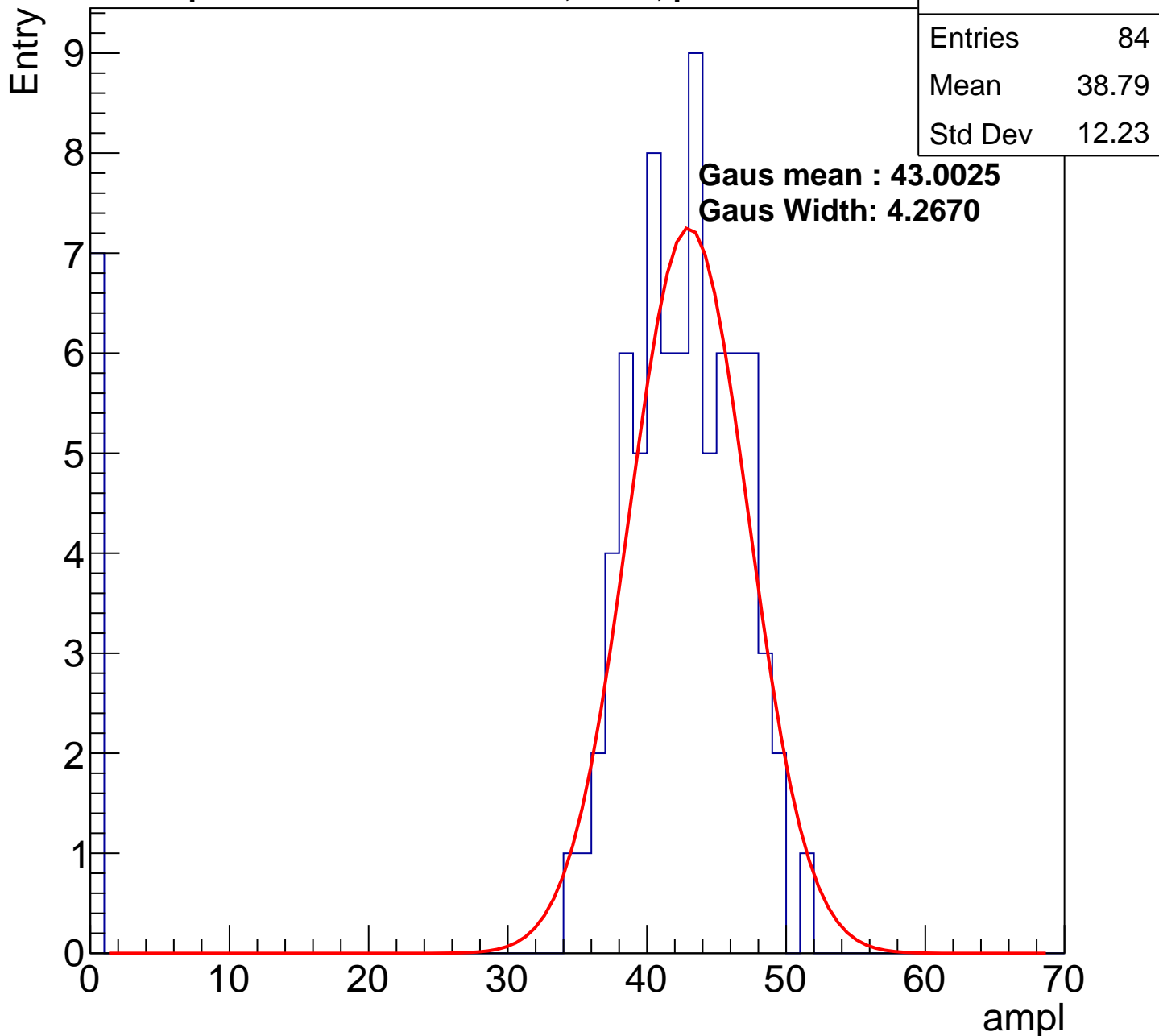
**Gaus mean : 36.2270**

**Gaus Width: 3.9644**



# B1L103S, U26-ch1, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

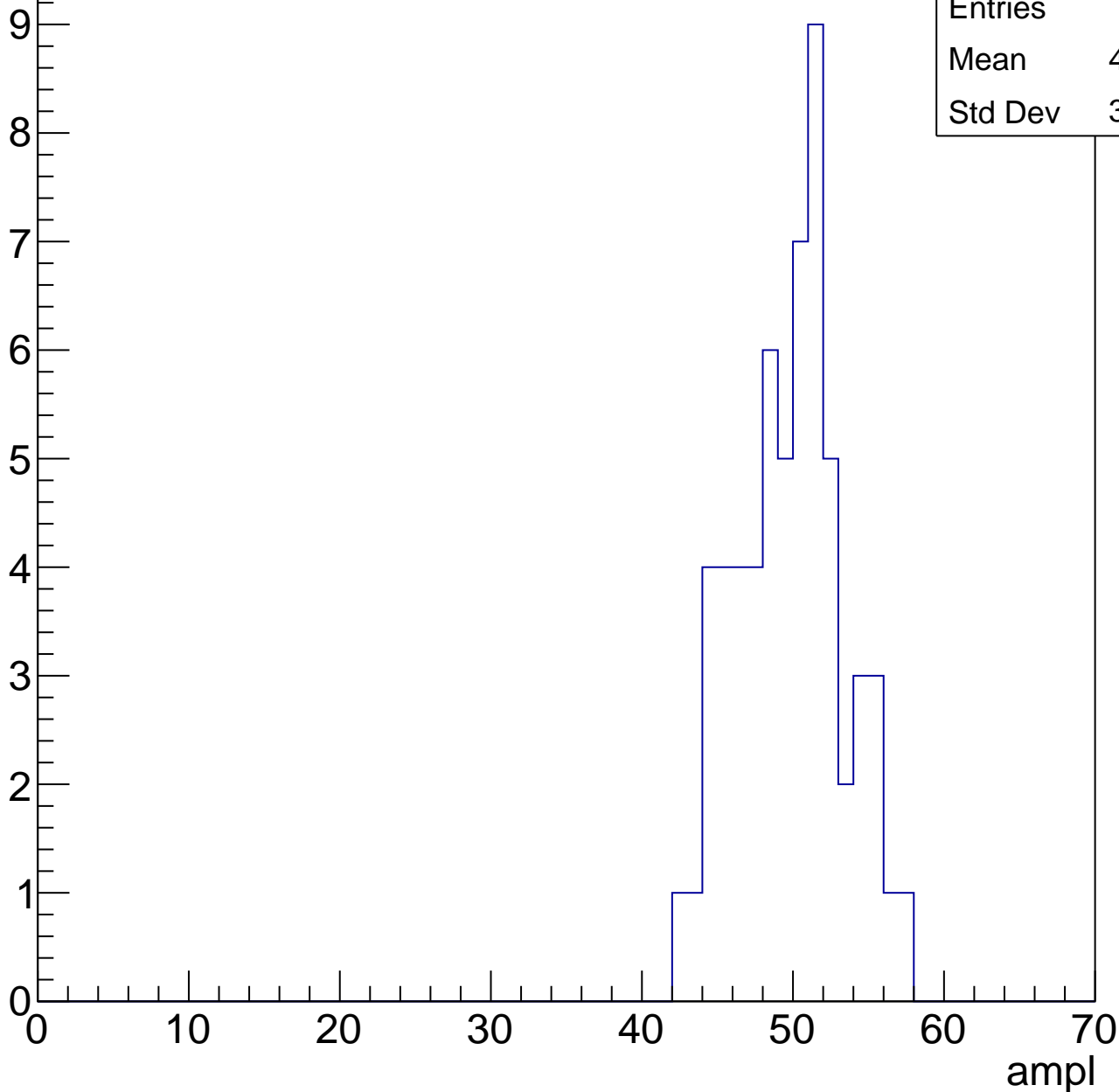


# B1L103S, U26-ch1, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	60
Mean	49.35
Std Dev	3.454

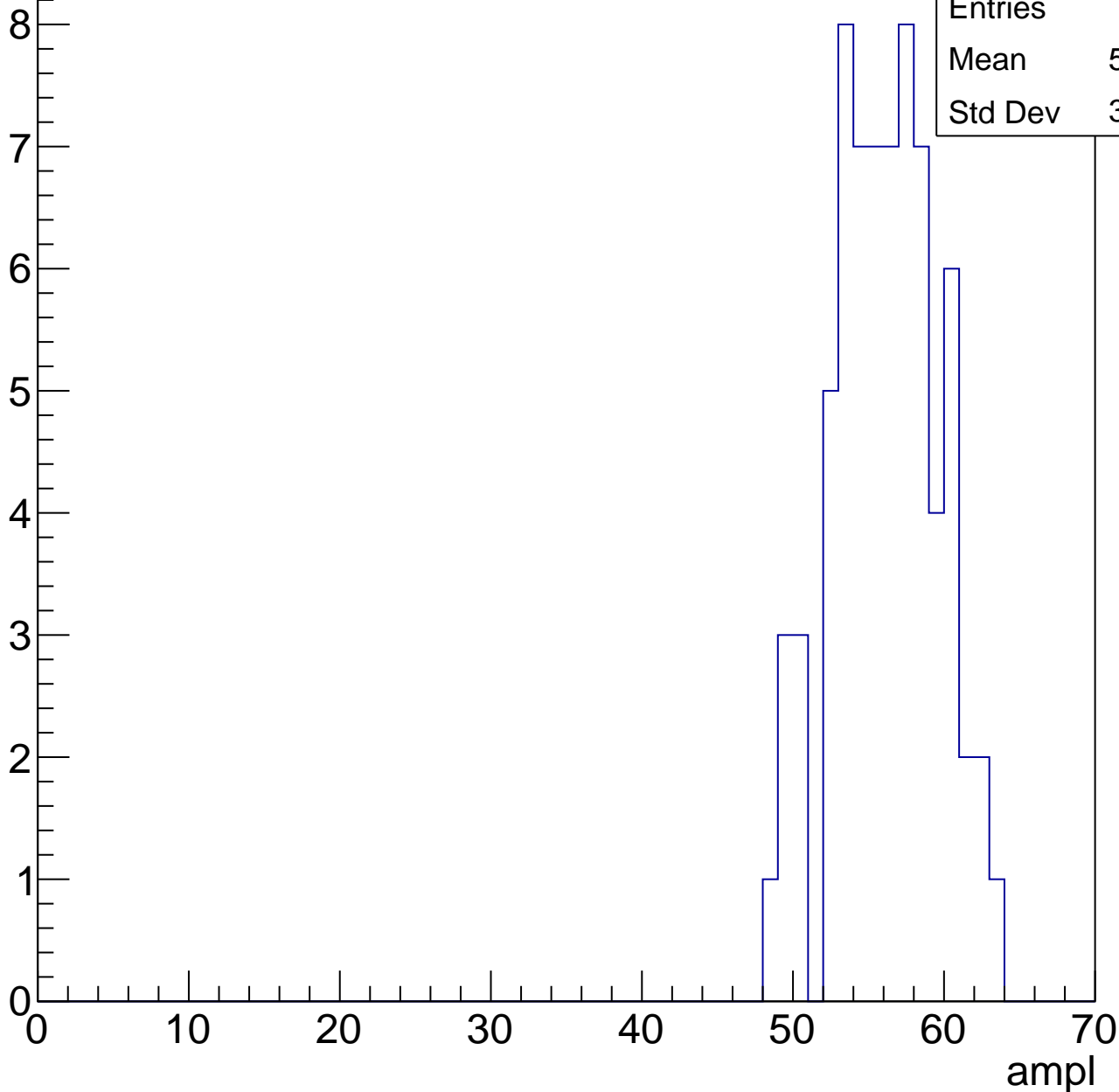


# B1L103S, U26-ch1, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	71
Mean	55.65
Std Dev	3.432

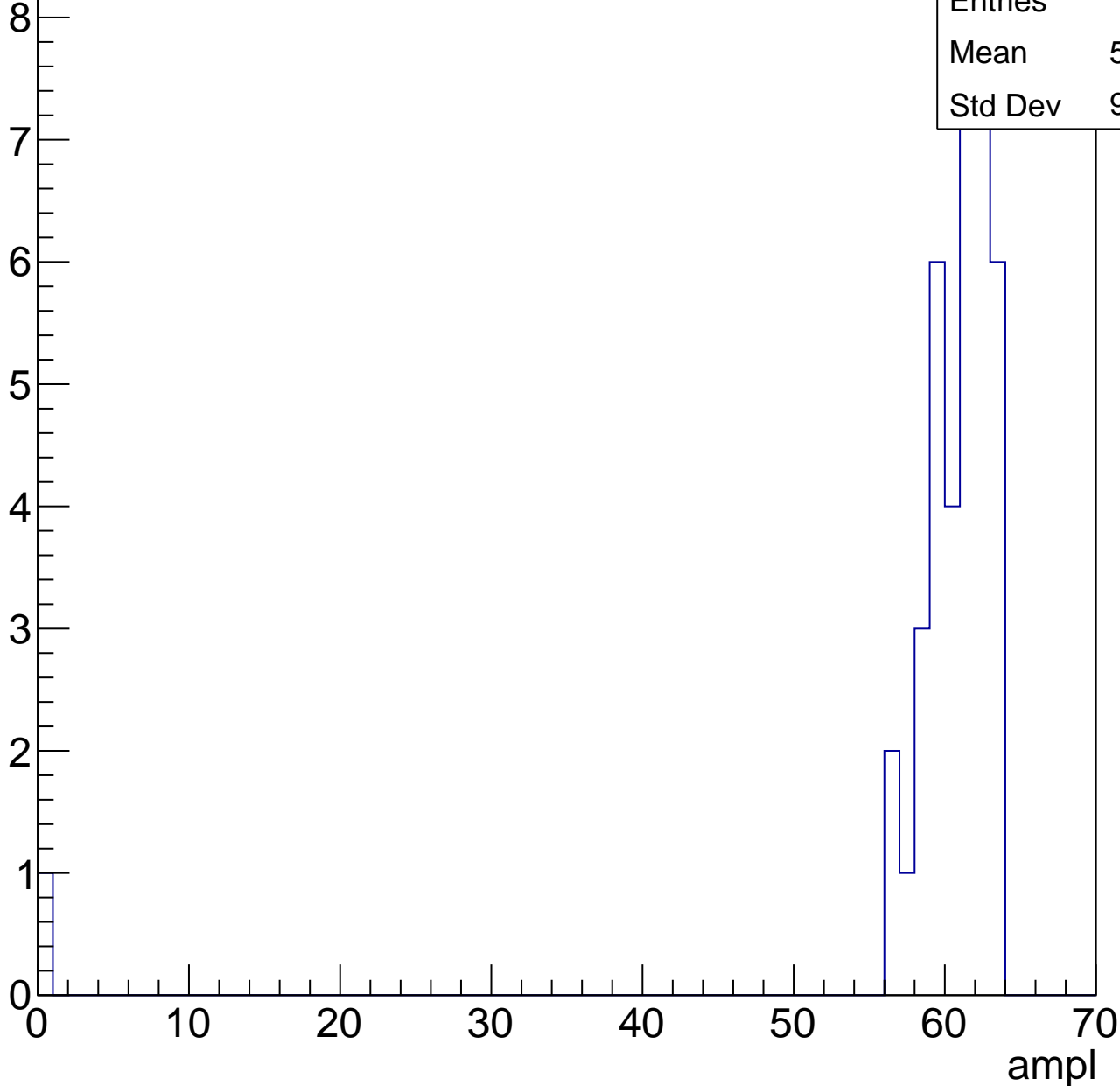


# B1L103S, U26-ch1, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

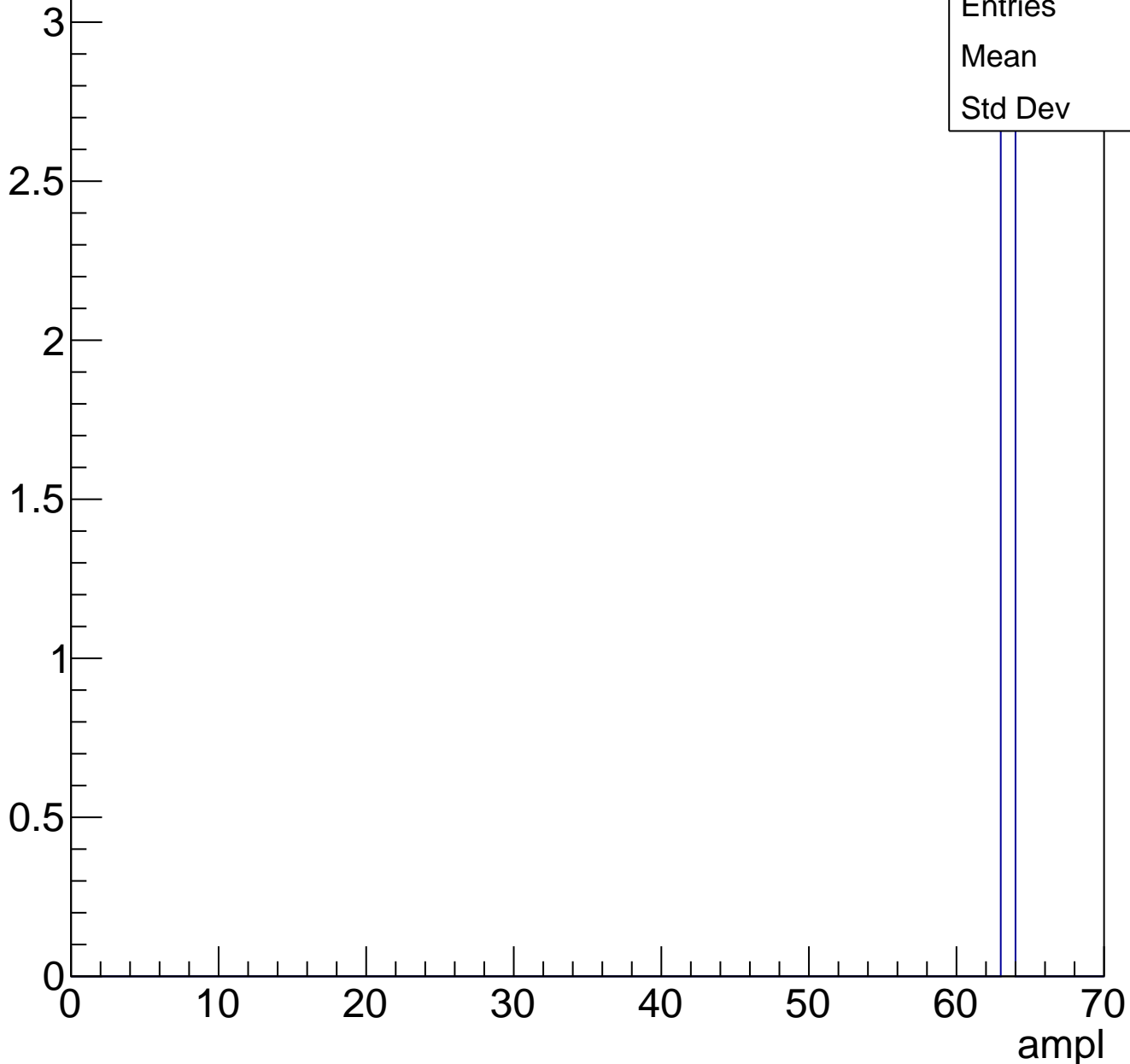
Entries	39
Mean	58.95
Std Dev	9.753



# B1L103S, U26-ch1, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry





# B1L103S, U26-ch1, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

18  
16  
14  
12  
10  
8  
6  
4  
2  
0

Entries	19
Mean	0
Std Dev	0

ampl

# B1L103S, U26-ch2, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	119
Mean	20.62
Std Dev	11.96

**Gaus mean : 27.4166**

**Gaus Width: 4.3613**

Entry

25

20

15

10

5

0

0

10

20

30

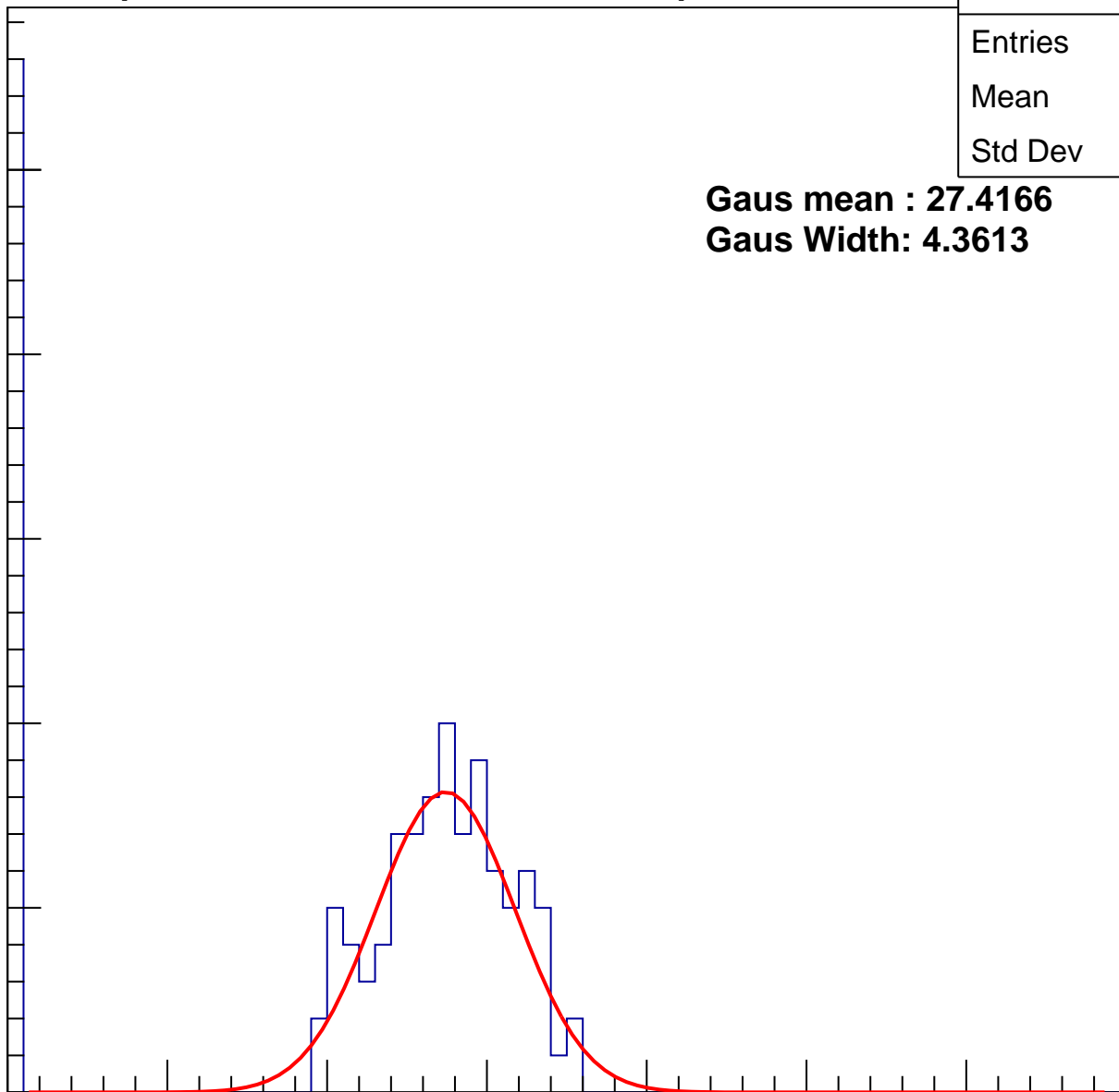
40

50

60

70

ampl



# B1L103S, U26-ch2, adc1

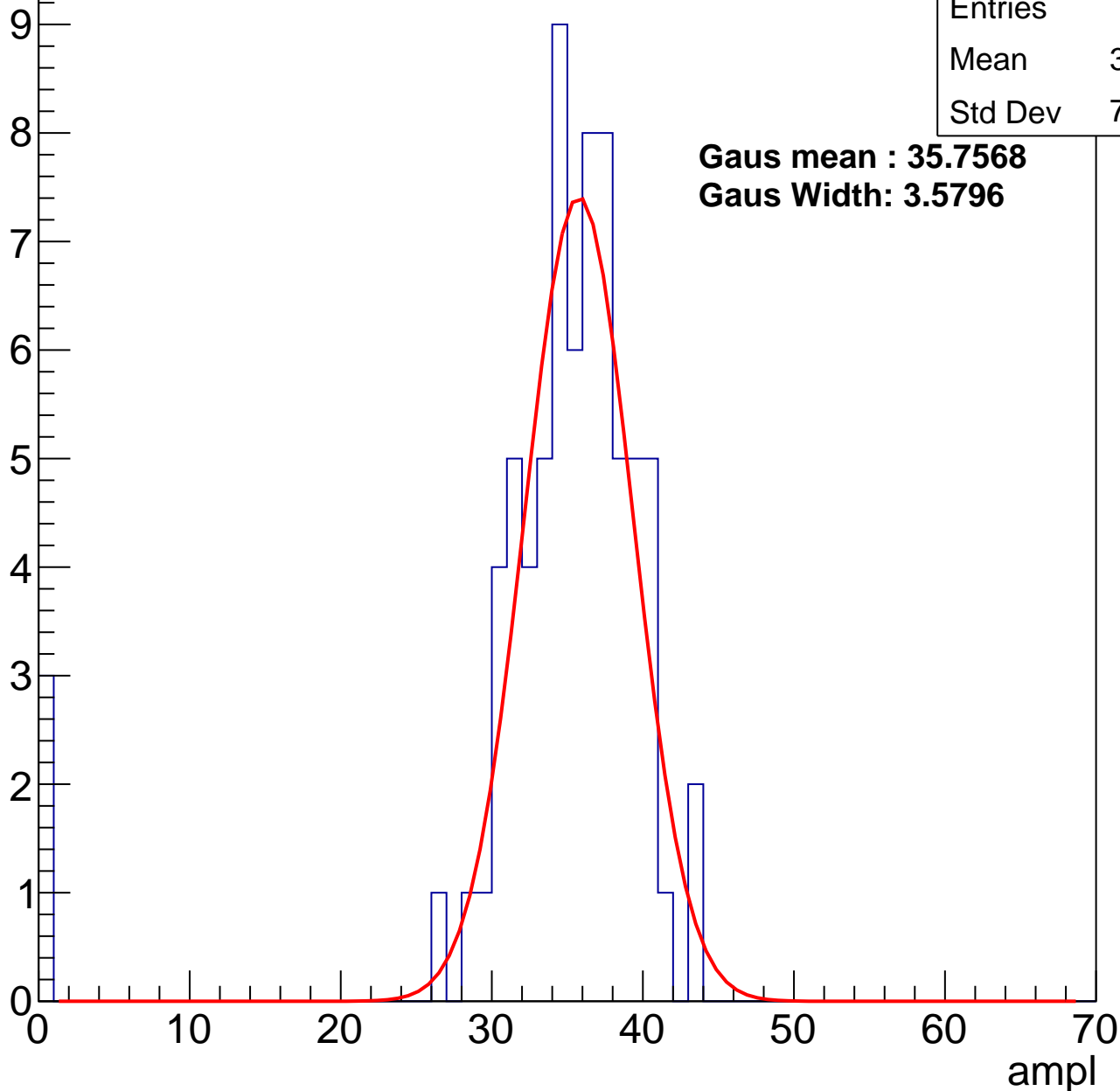
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	73
Mean	33.74
Std Dev	7.785

**Gaus mean : 35.7568**

**Gaus Width: 3.5796**



# B1L103S, U26-ch2, adc2

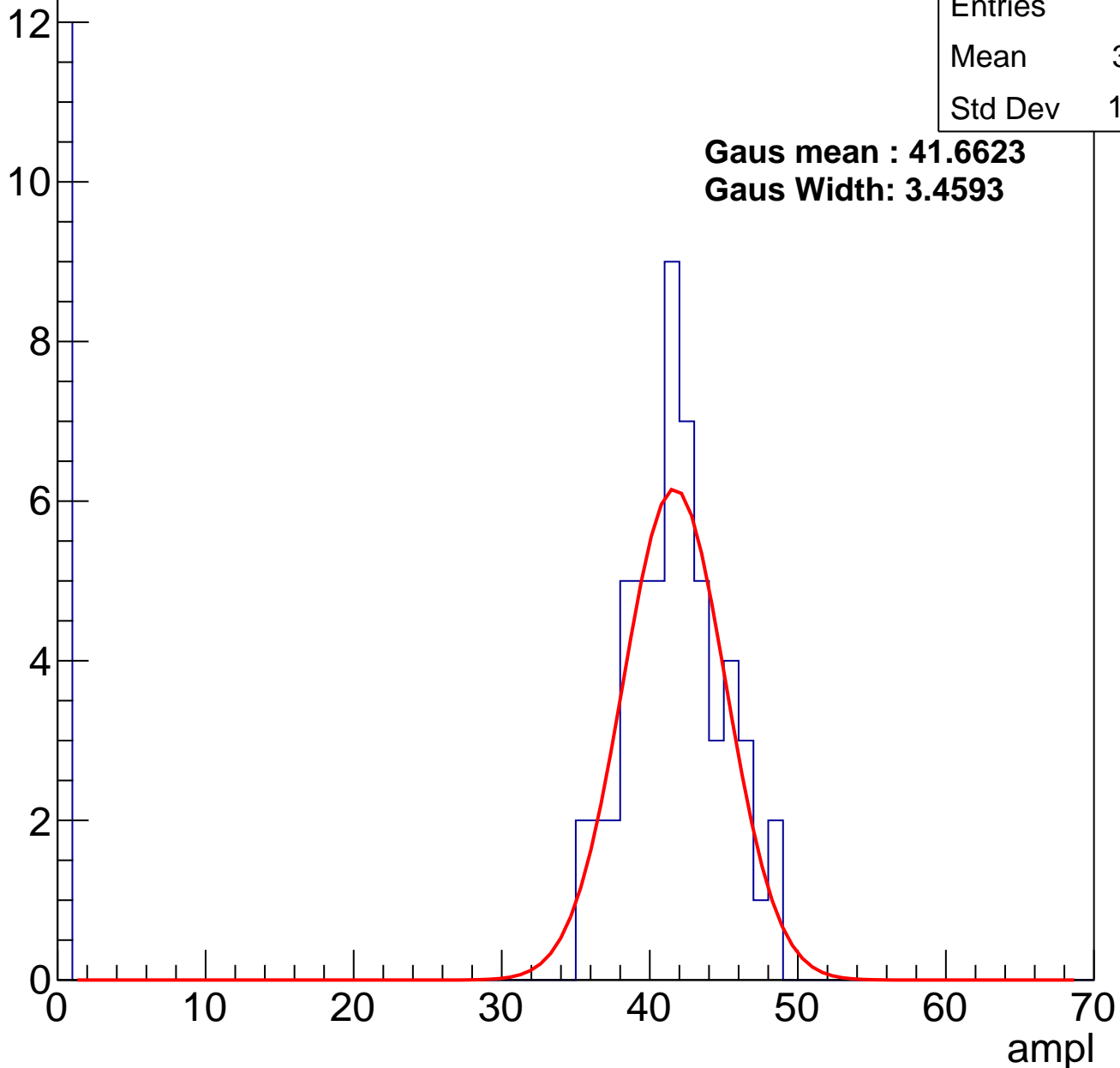
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	67
Mean	33.91
Std Dev	16.09

**Gaus mean : 41.6623**

**Gaus Width: 3.4593**

Entry

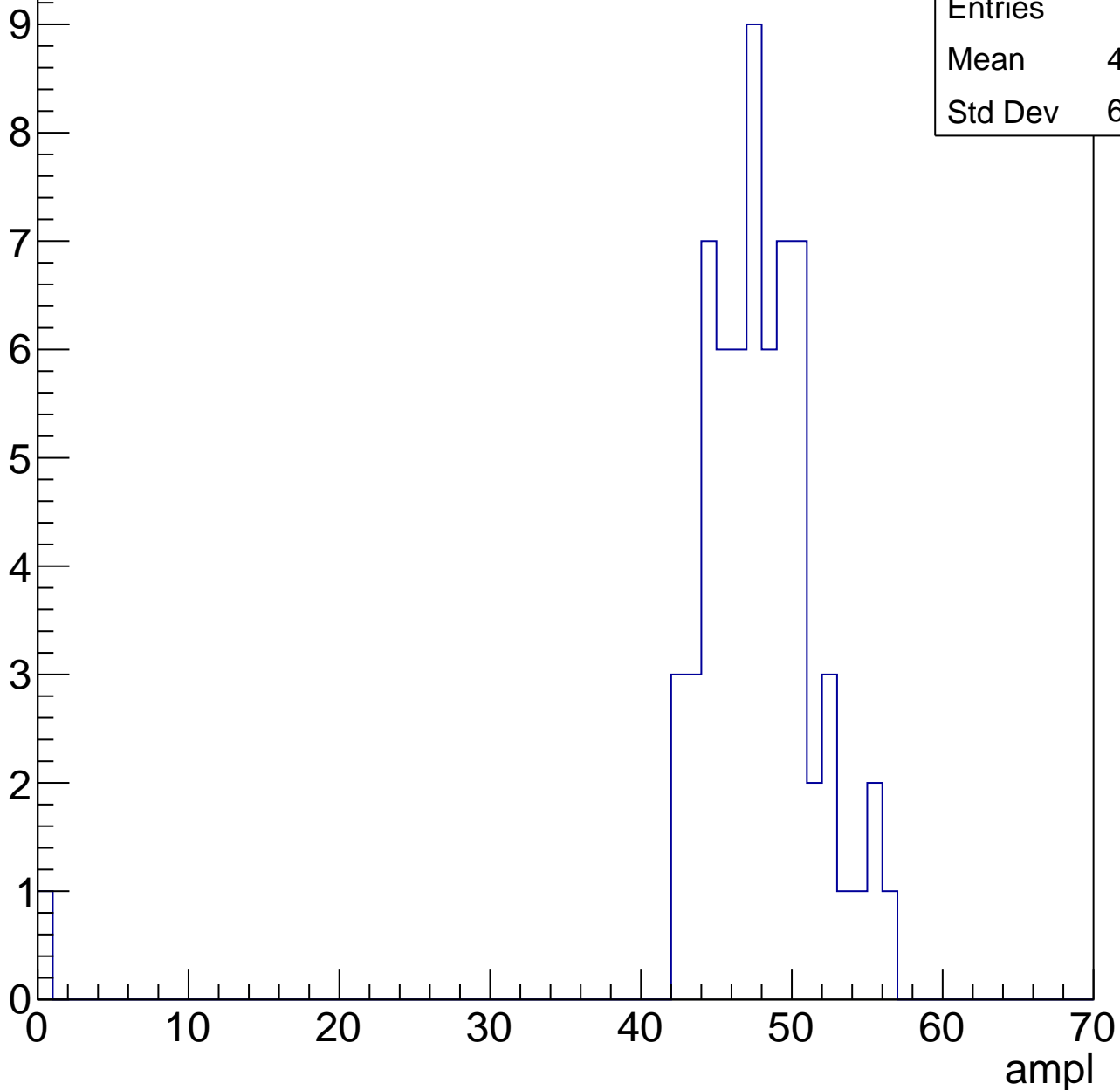


# B1L103S, U26-ch2, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	65
Mean	46.83
Std Dev	6.704

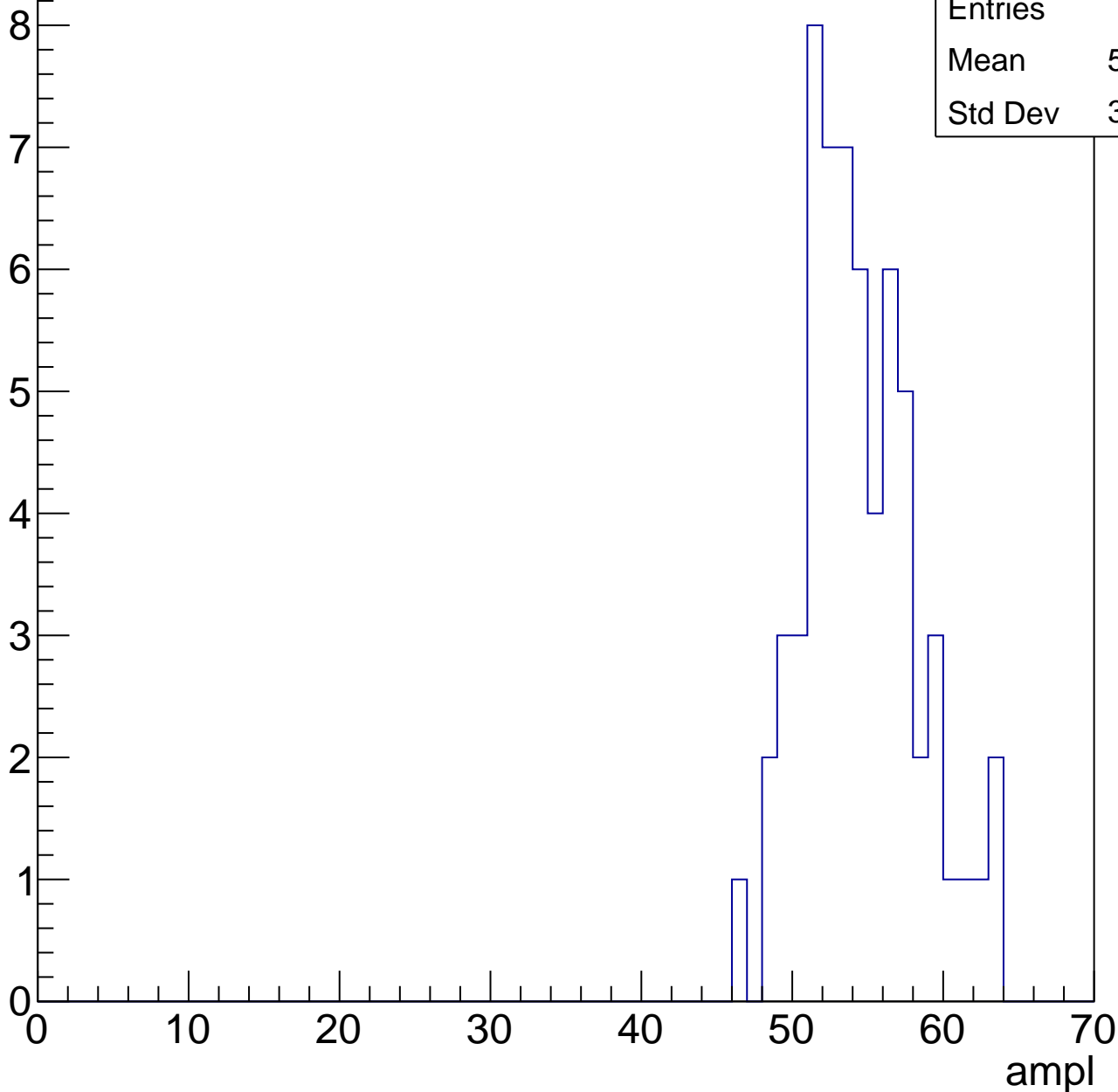


# B1L103S, U26-ch2, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	62
Mean	54.02
Std Dev	3.718



# B1L103S, U26-ch2, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

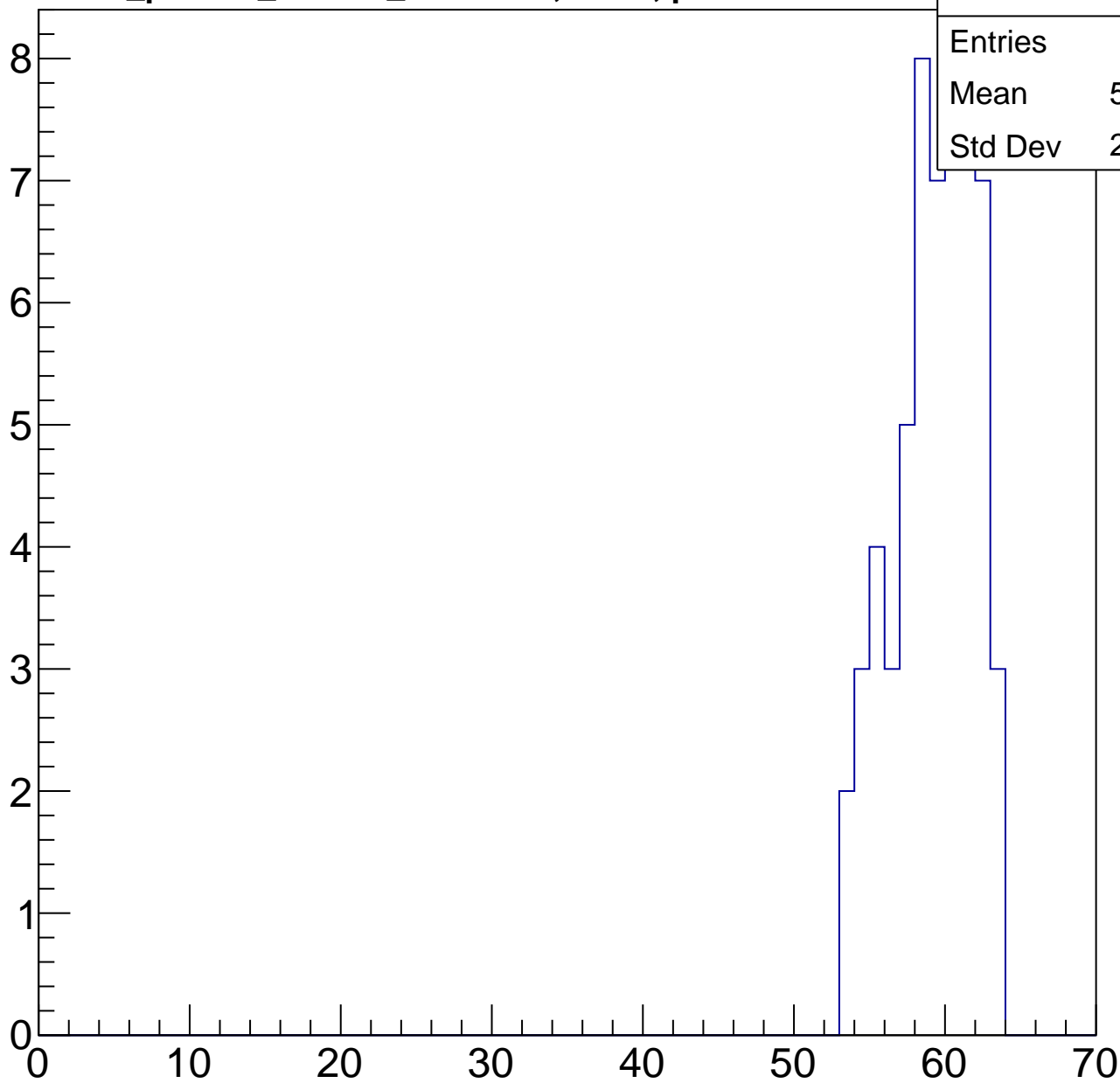
Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	58
Mean	58.78
Std Dev	2.672

ampl

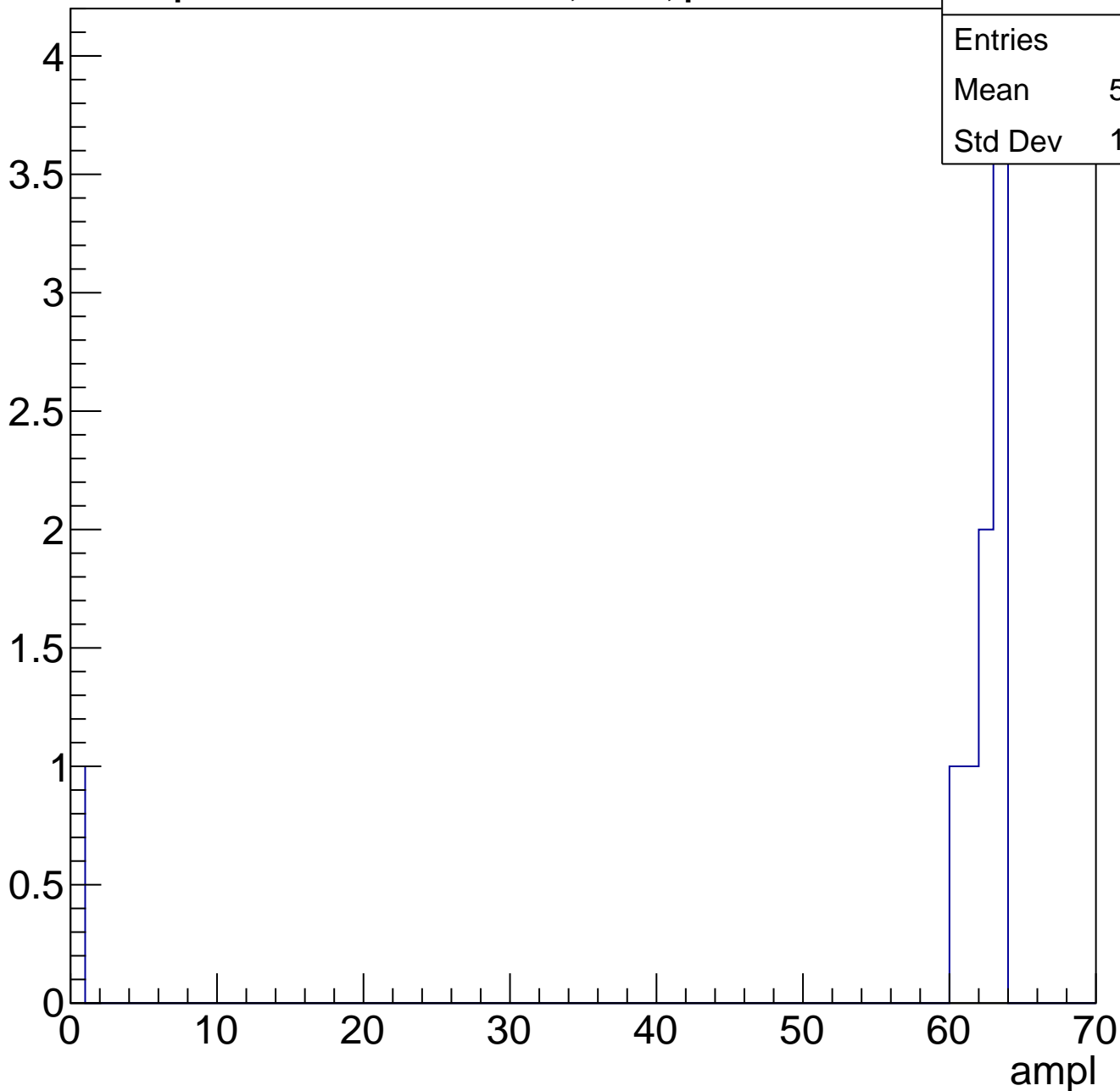
0 10 20 30 40 50 60 70



# B1L103S, U26-ch2, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry





# B1L103S, U26-ch2, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

18  
16  
14  
12  
10  
8  
6  
4  
2  
0

Entries	20
Mean	3.15
Std Dev	13.73

ampl

0 10 20 30 40 50 60 70

# B1L103S, U26-ch3, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	104
Mean	22.22
Std Dev	13.2

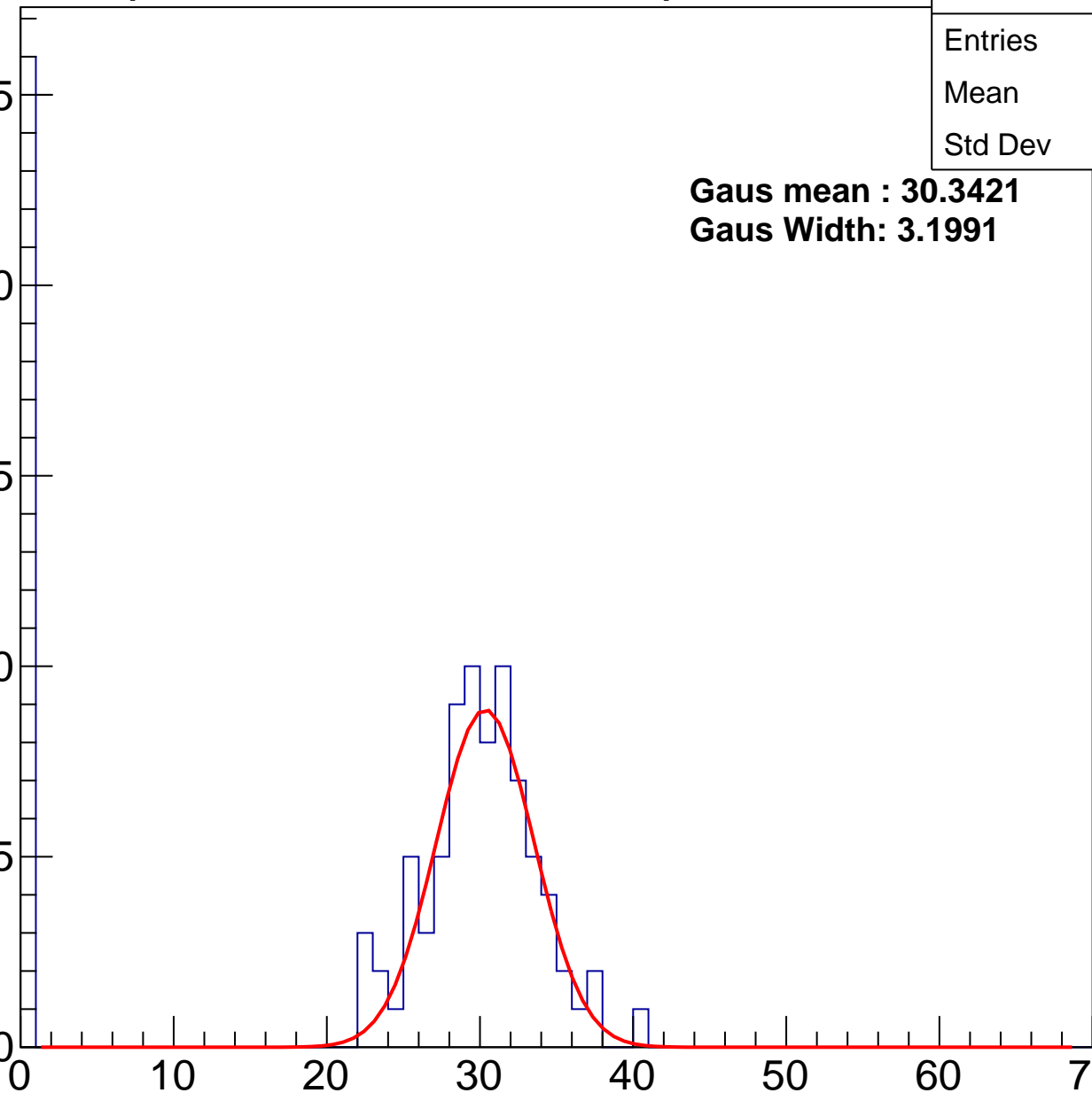
**Gaus mean : 30.3421**

**Gaus Width: 3.1991**

Entry

25  
20  
15  
10  
5  
0

ampl



# B1L103S, U26-ch3, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	85
Mean	32.21
Std Dev	12.85

**Gaus mean : 37.2318**

**Gaus Width: 3.8922**

Entry

10

8

6

4

2

0

0

10

20

30

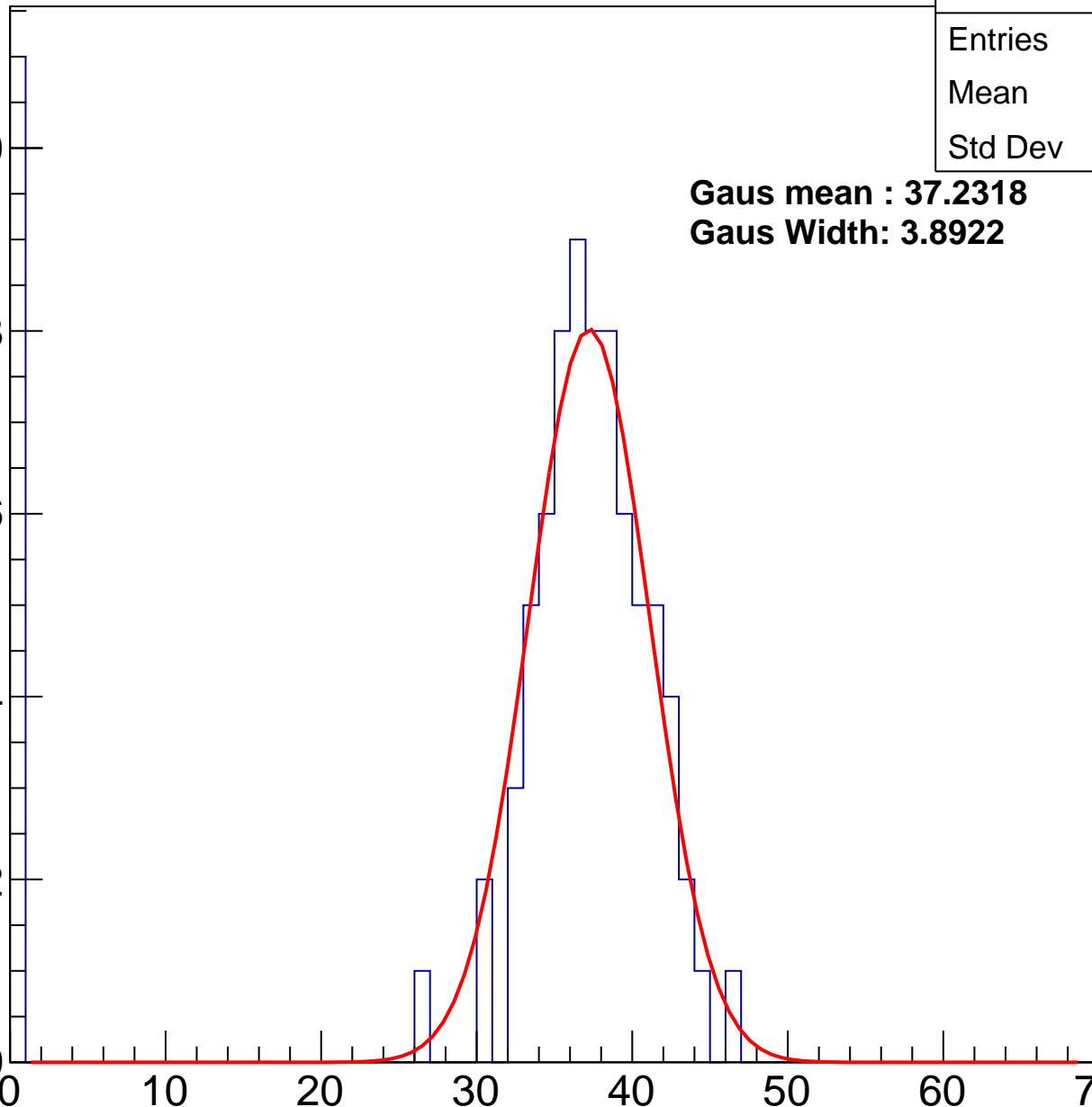
40

50

60

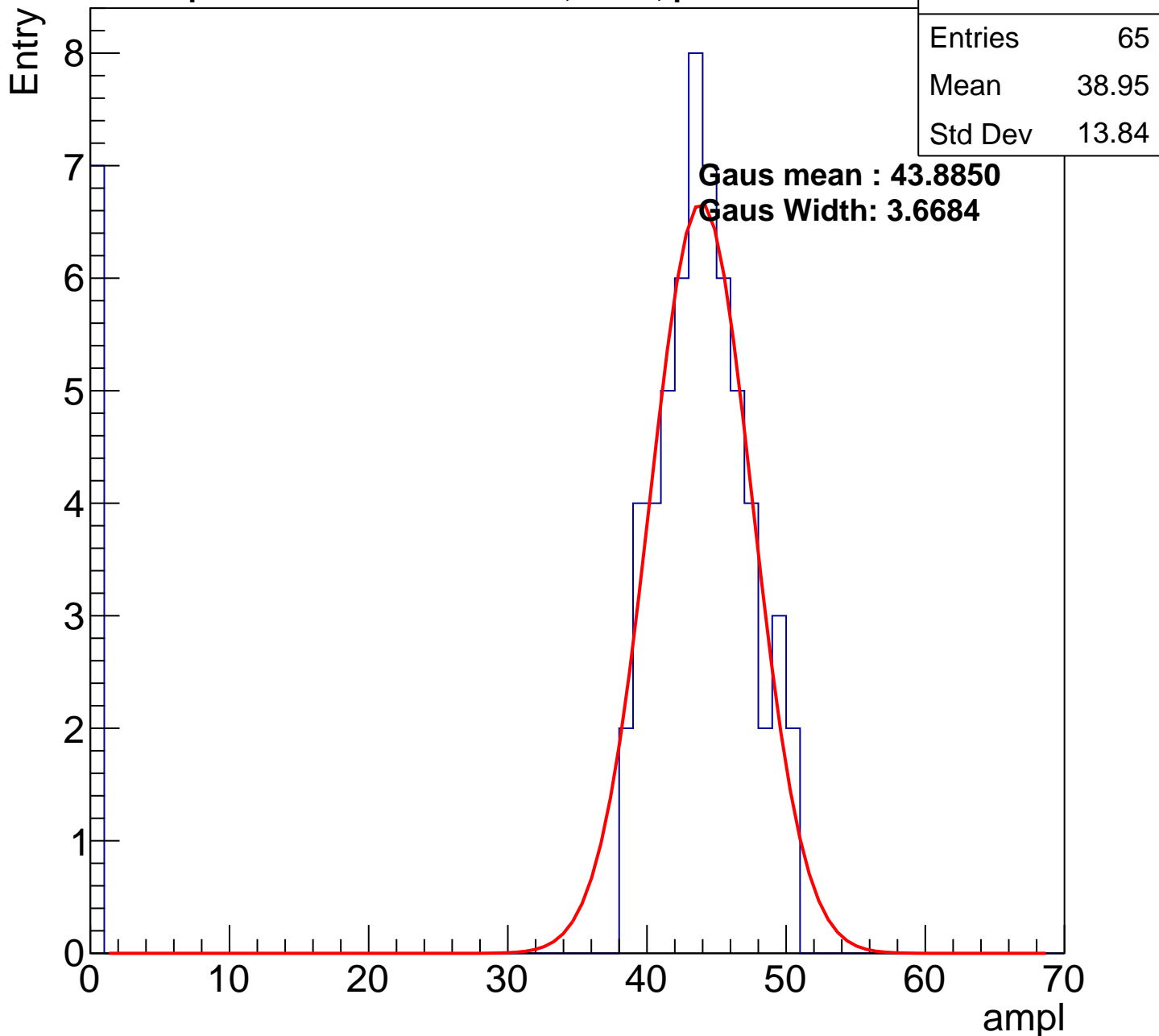
70

ampl



# B1L103S, U26-ch3, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

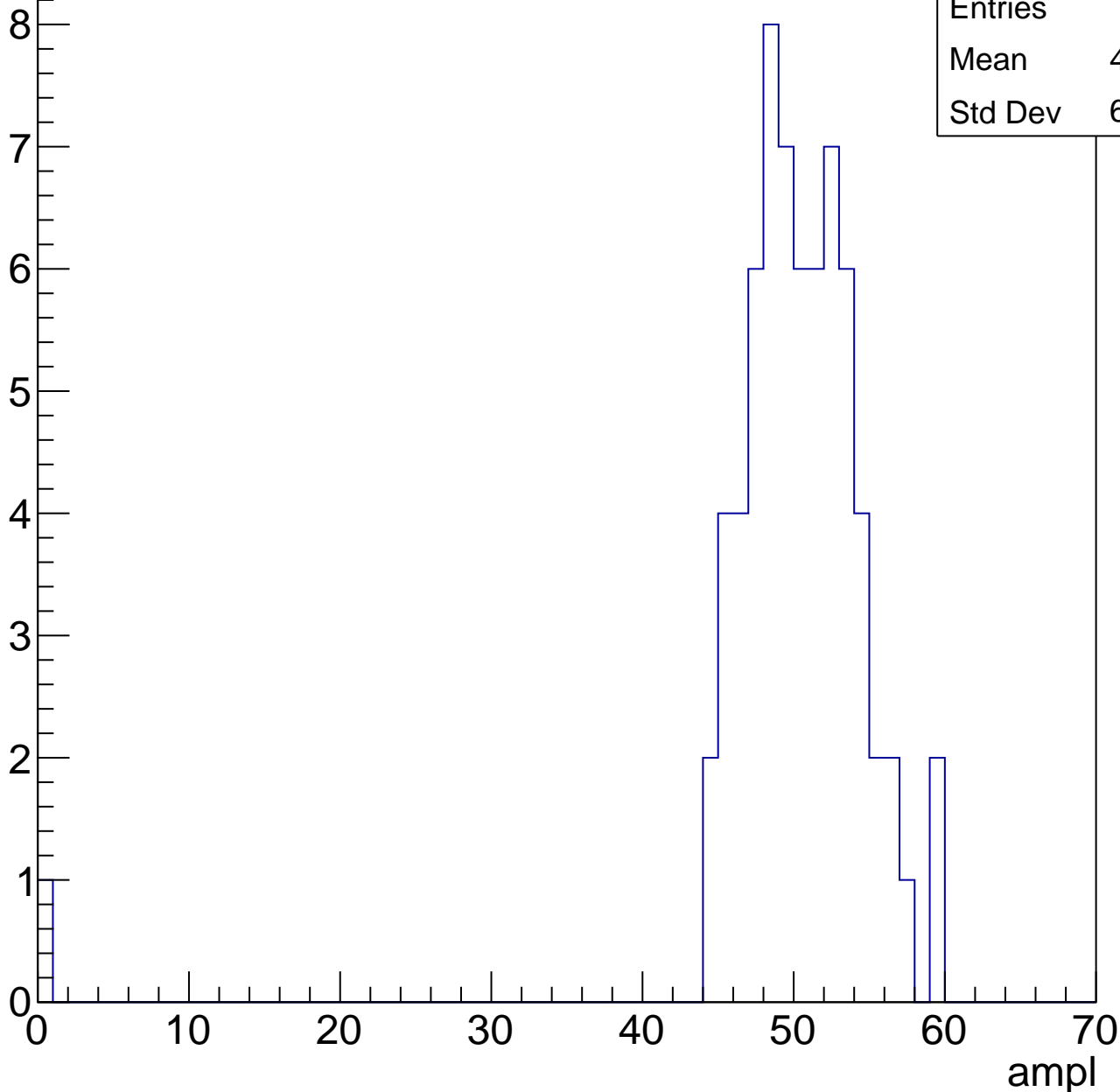


# B1L103S, U26-ch3, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	68
Mean	49.44
Std Dev	6.959

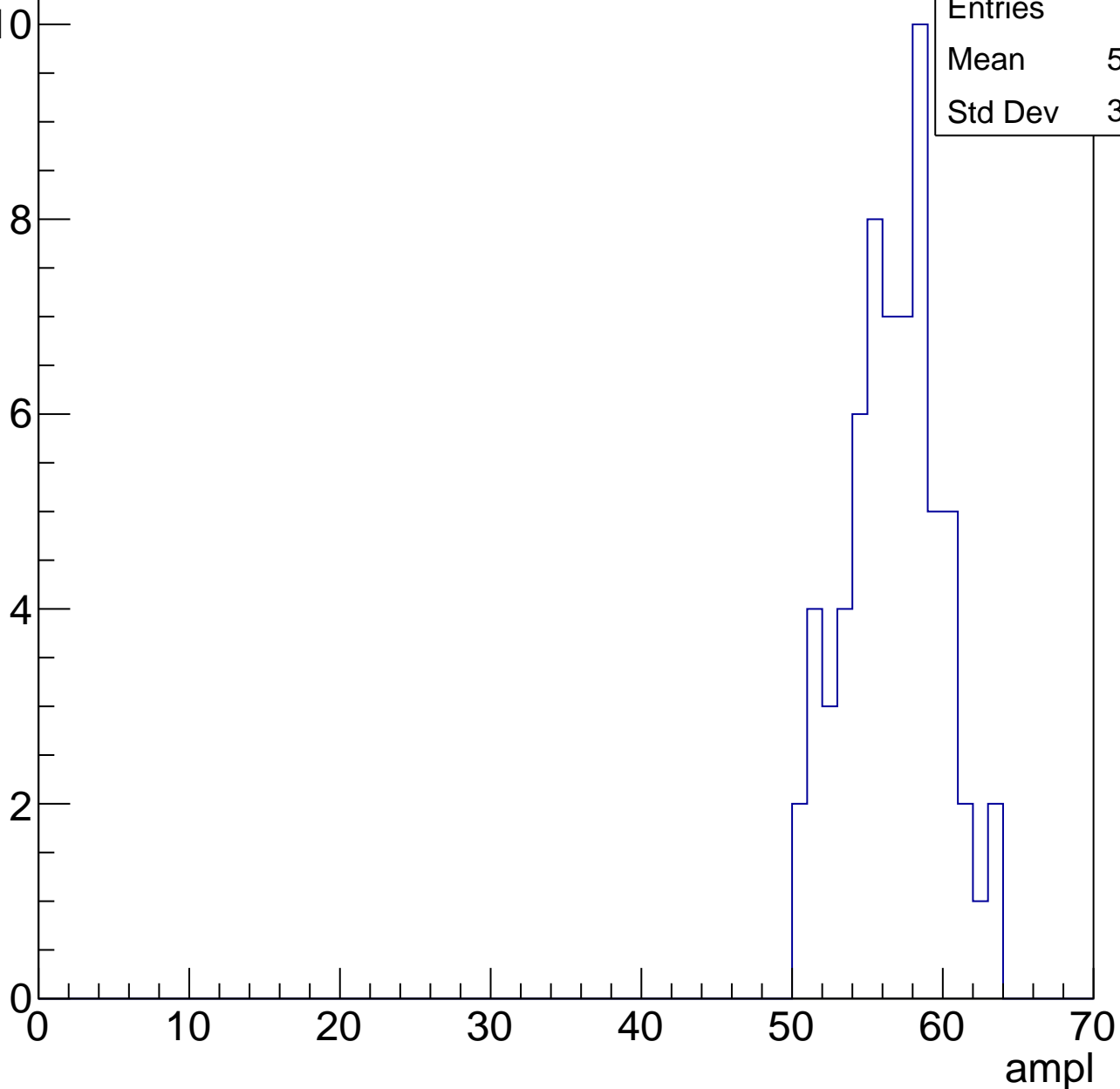


# B1L103S, U26-ch3, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	66
Mean	56.24
Std Dev	3.114

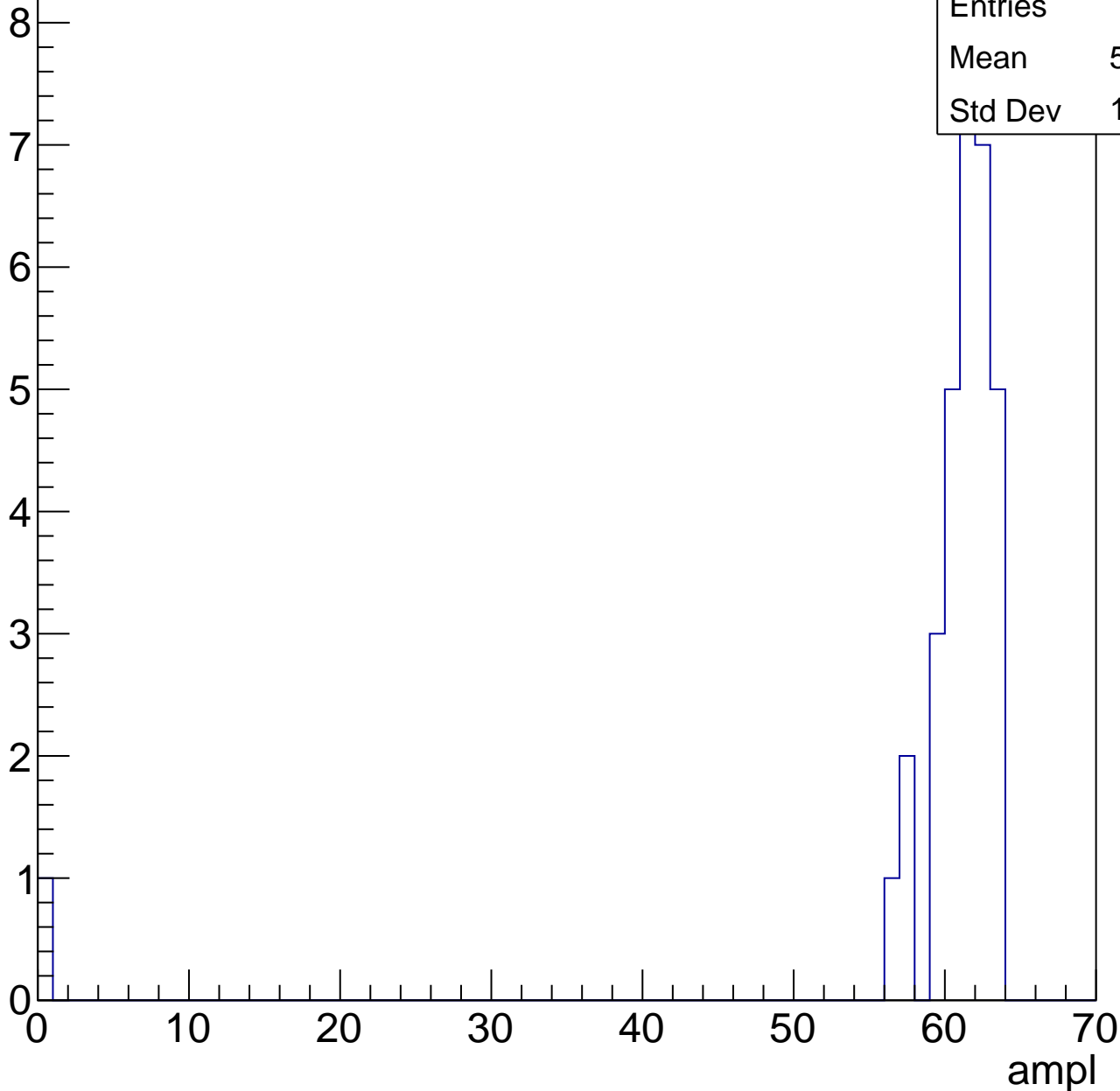


# B1L103S, U26-ch3, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	32
Mean	58.88
Std Dev	10.72



# B1L103S, U26-ch3, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

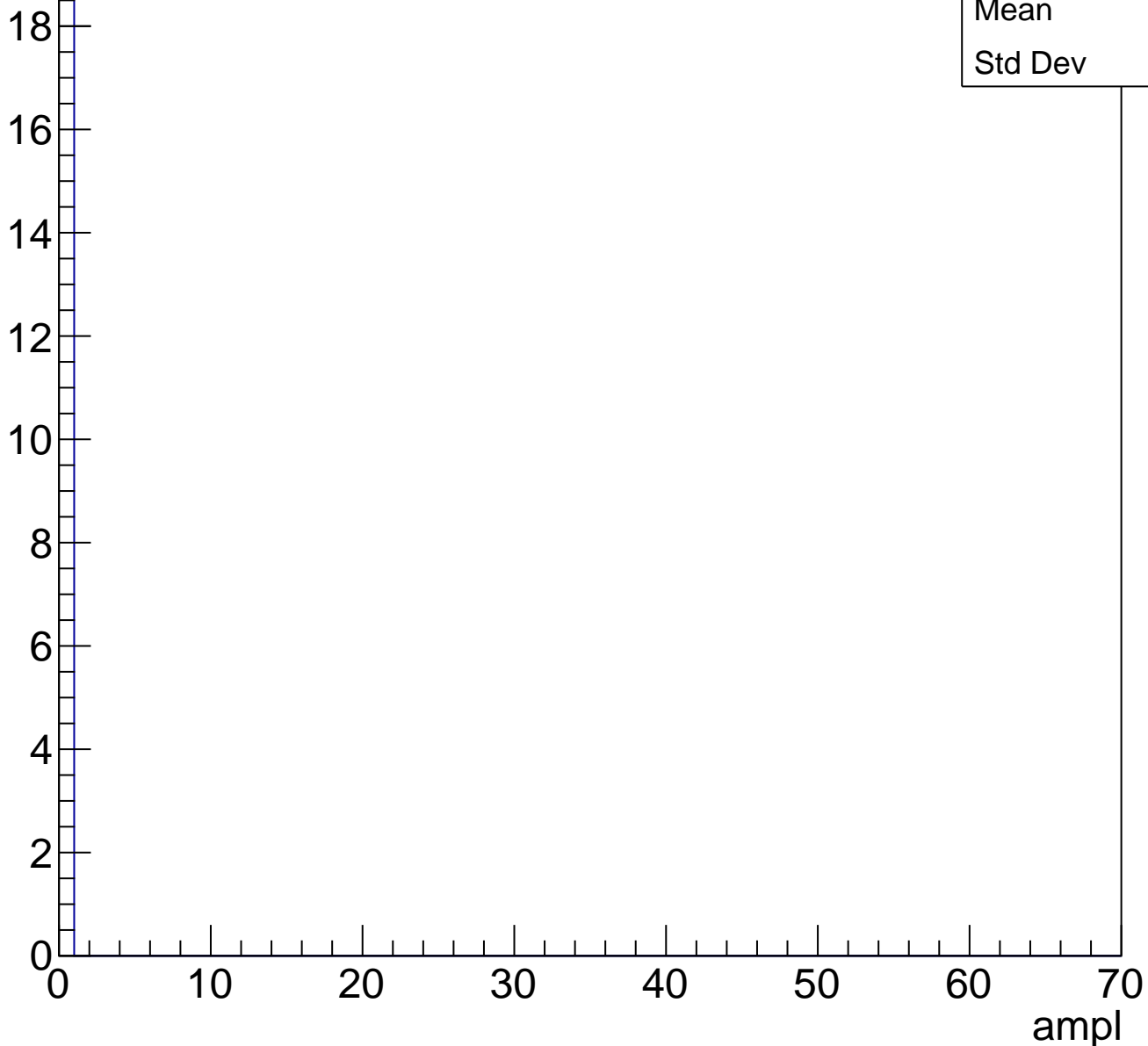




# B1L103S, U26-ch3, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



# B1L103S, U26-ch4, adc0

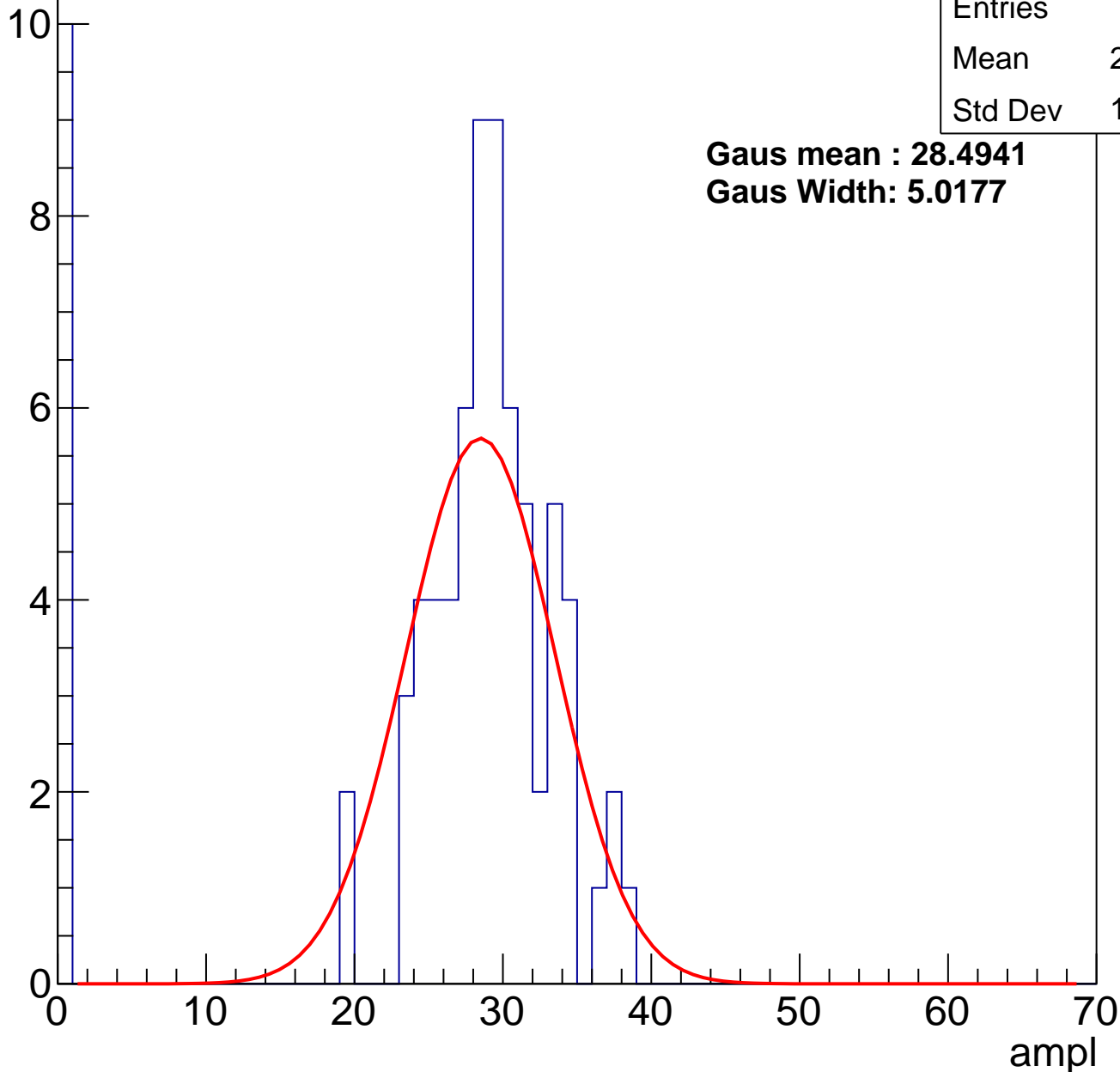
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	77
Mean	25.06
Std Dev	10.35

**Gaus mean : 28.4941**

**Gaus Width: 5.0177**

Entry



# B1L103S, U26-ch4, adc1

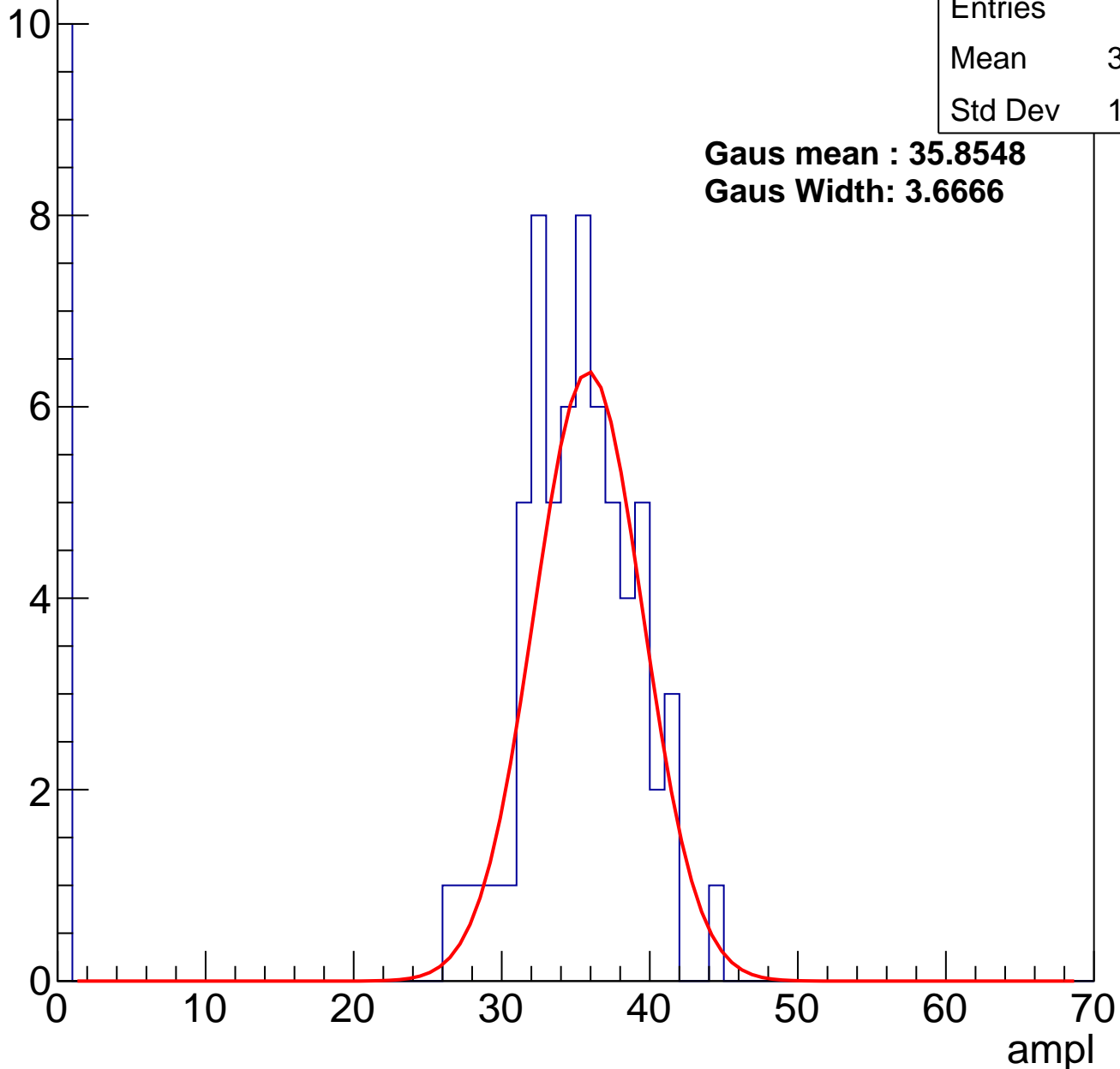
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	73
Mean	30.07
Std Dev	12.44

**Gaus mean : 35.8548**

**Gaus Width: 3.6666**

Entry



# B1L103S, U26-ch4, adc2

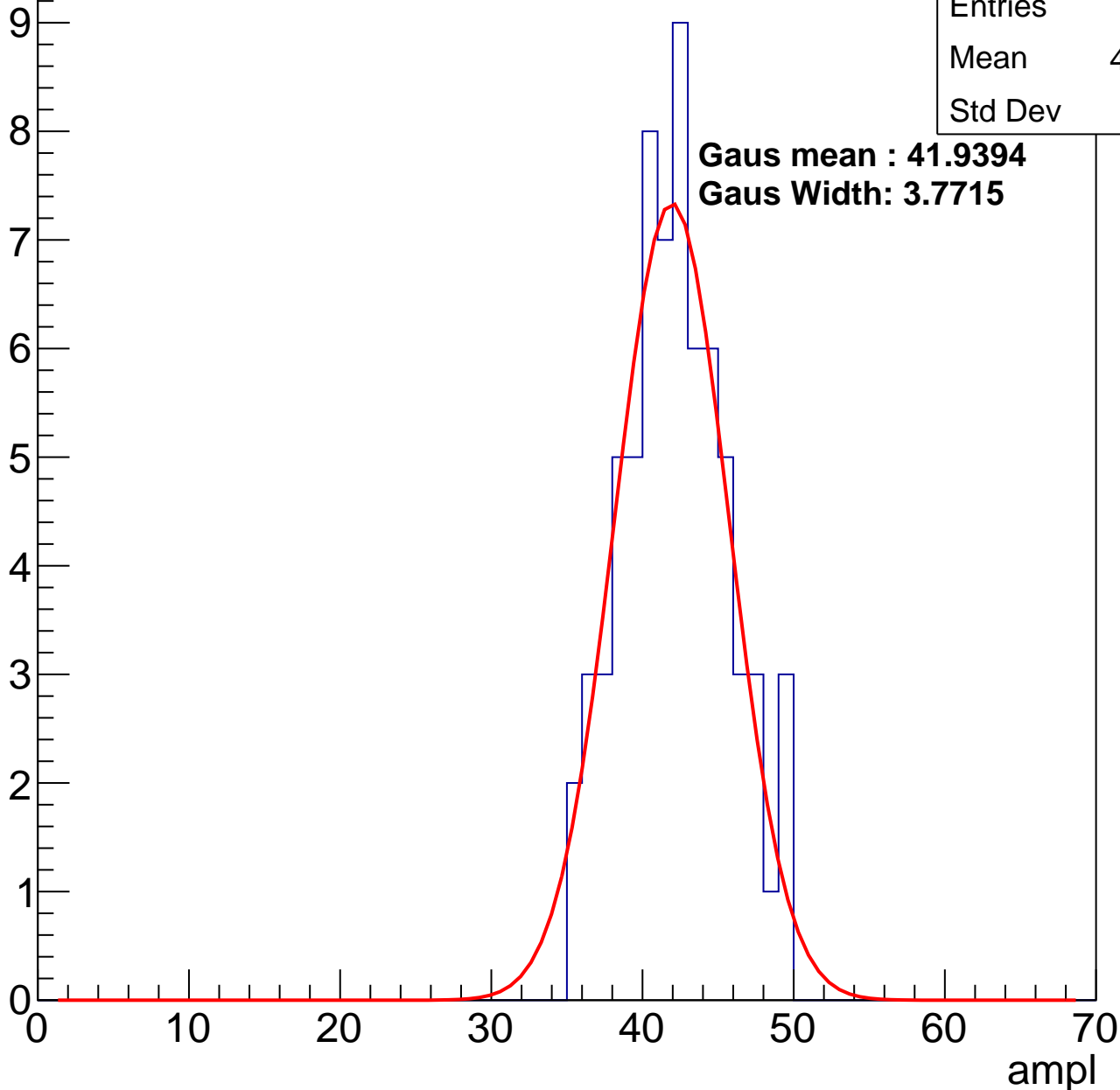
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	69
Mean	41.74
Std Dev	3.45

**Gaus mean : 41.9394**

**Gaus Width: 3.7715**

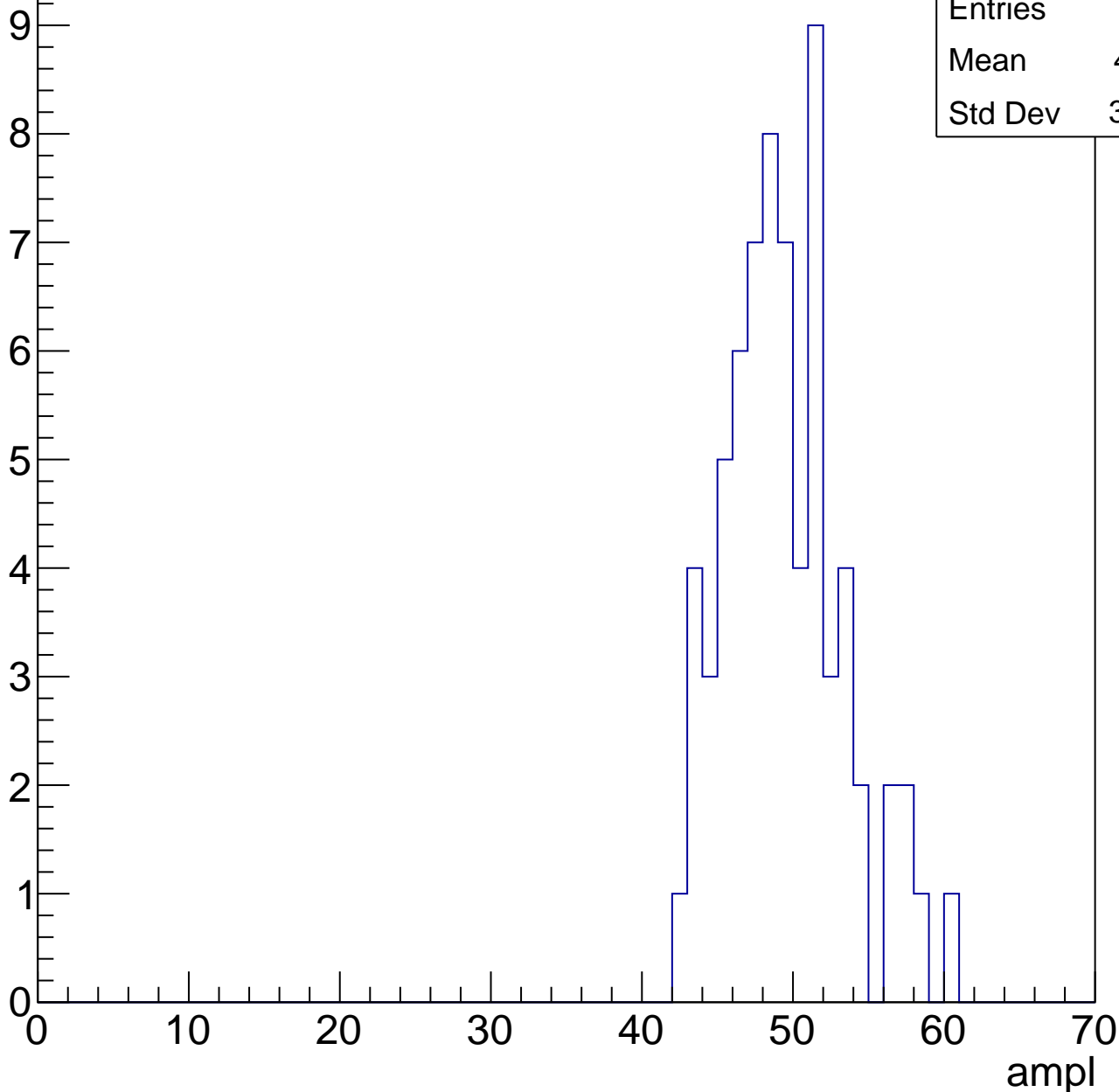


# B1L103S, U26-ch4, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	69
Mean	49.01
Std Dev	3.895

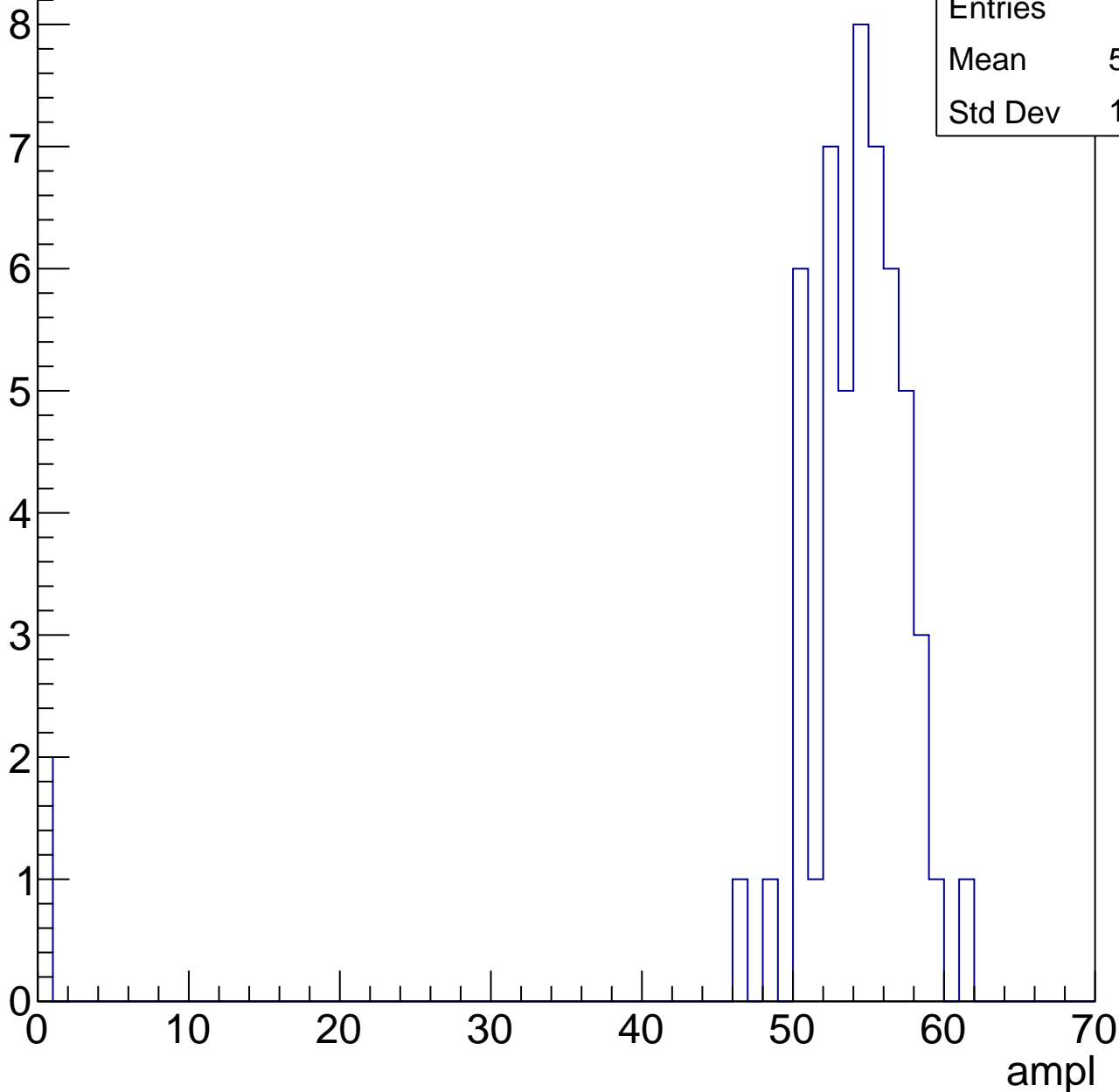


# B1L103S, U26-ch4, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	54
Mean	51.96
Std Dev	10.58

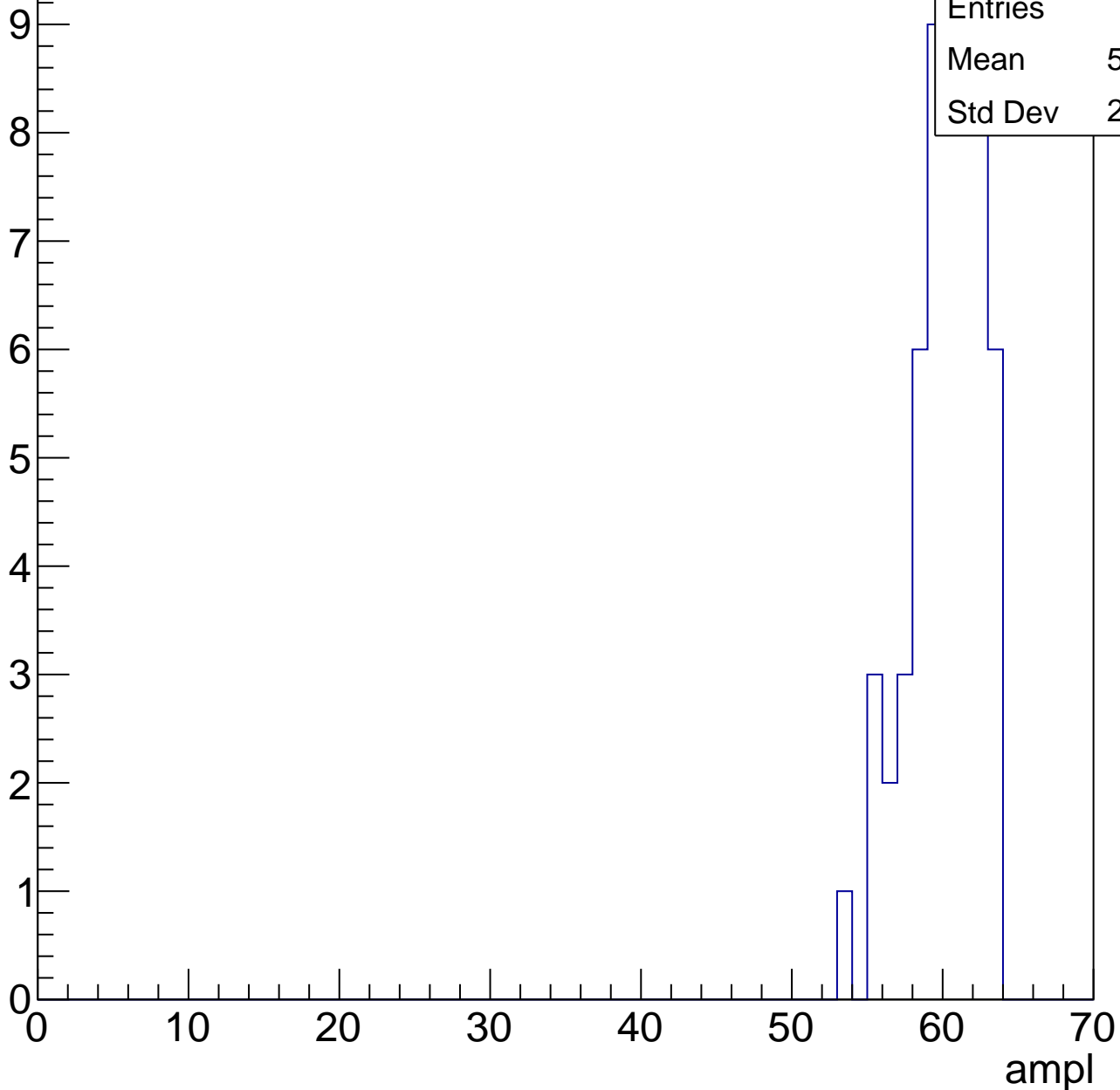


# B1L103S, U26-ch4, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

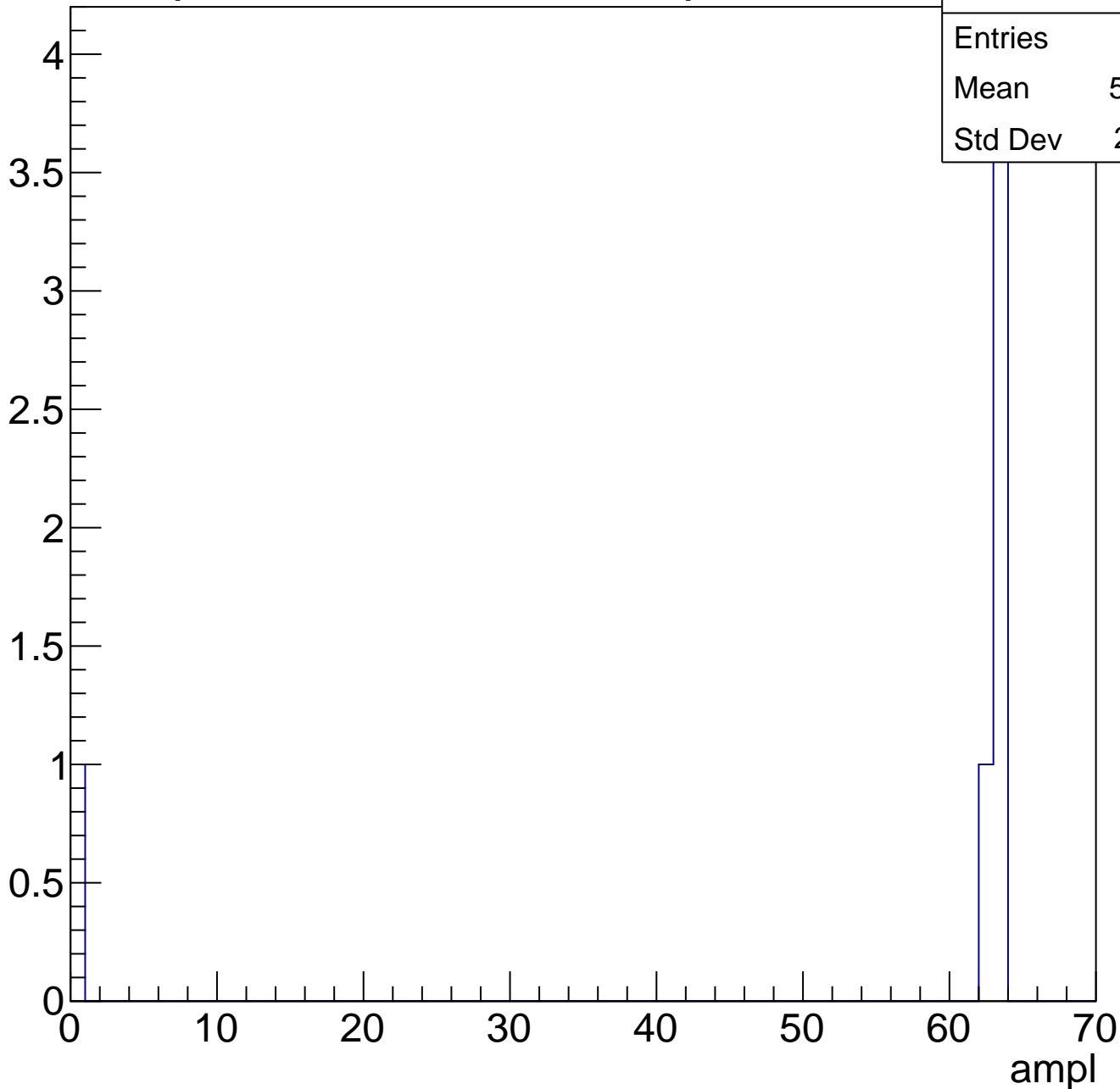
Entries	57
Mean	59.74
Std Dev	2.336



# B1L103S, U26-ch4, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry





# B1L103S, U26-ch4, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

18  
16  
14  
12  
10  
8  
6  
4  
2  
0

Entries	19
Mean	0
Std Dev	0

ampl

# B1L103S, U26-ch5, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	94
Mean	26.9
Std Dev	8.915

**Gaus mean : 30.3231**

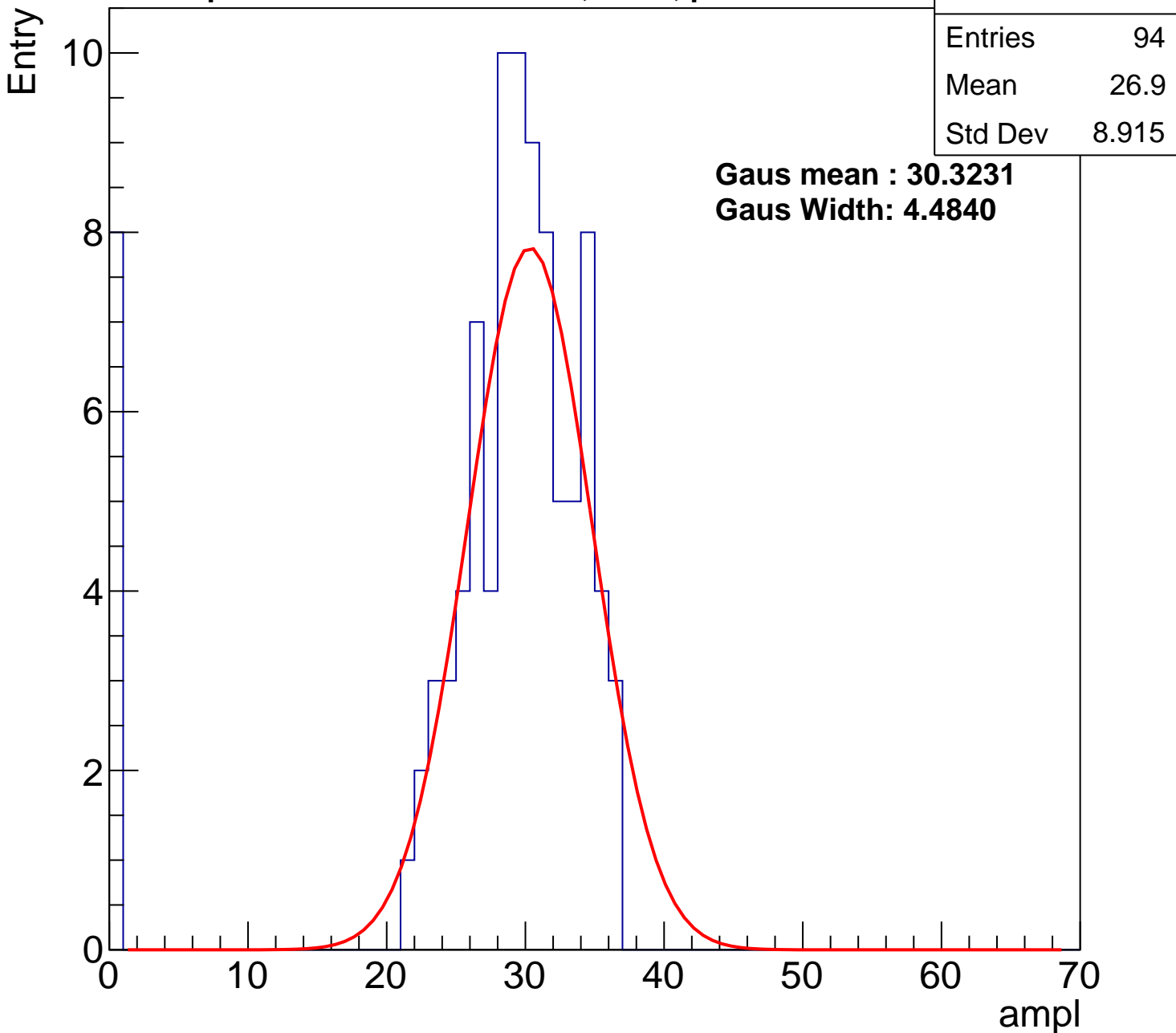
**Gaus Width: 4.4840**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U26-ch5, adc1

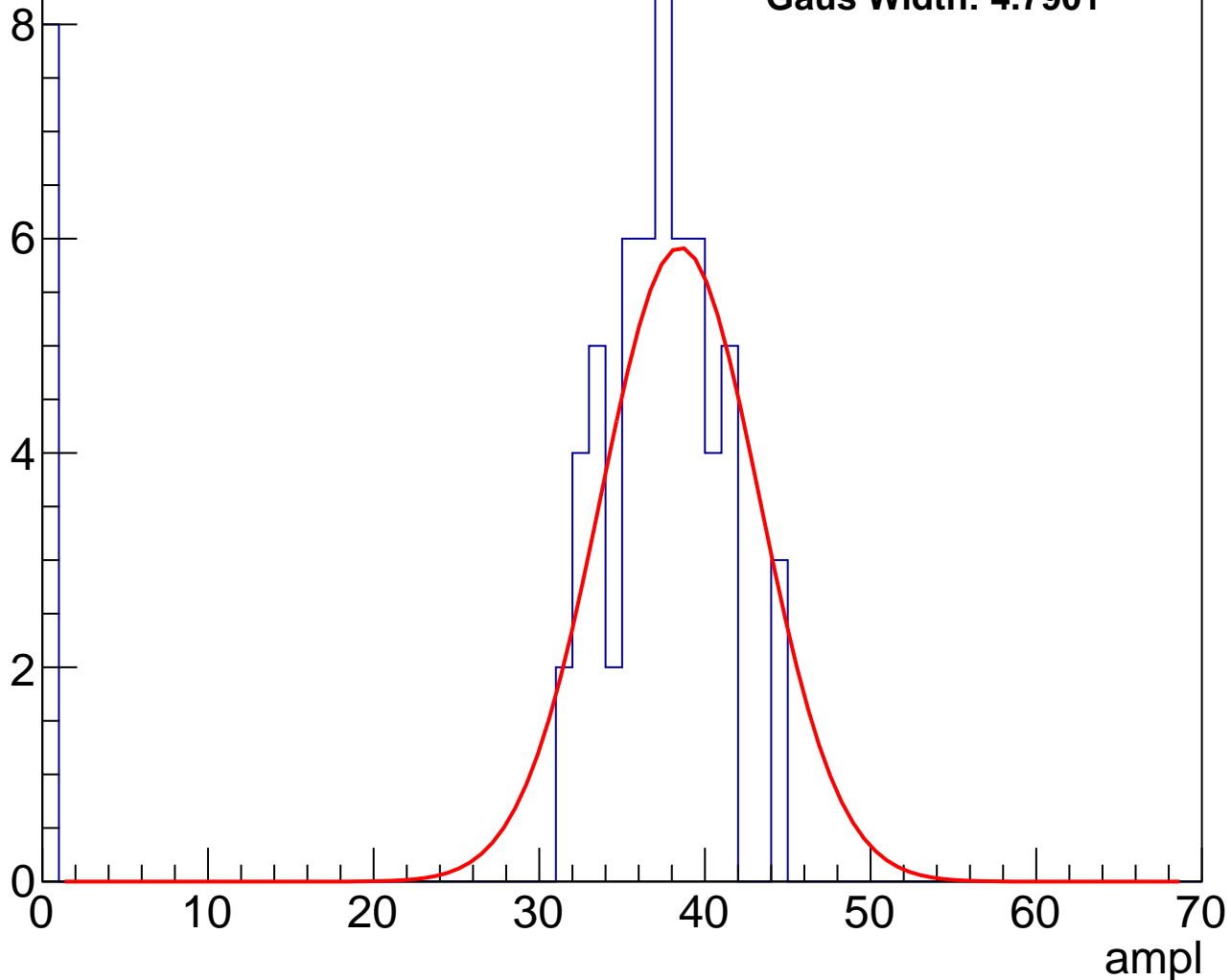
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	67
Mean	32.51
Std Dev	12.33

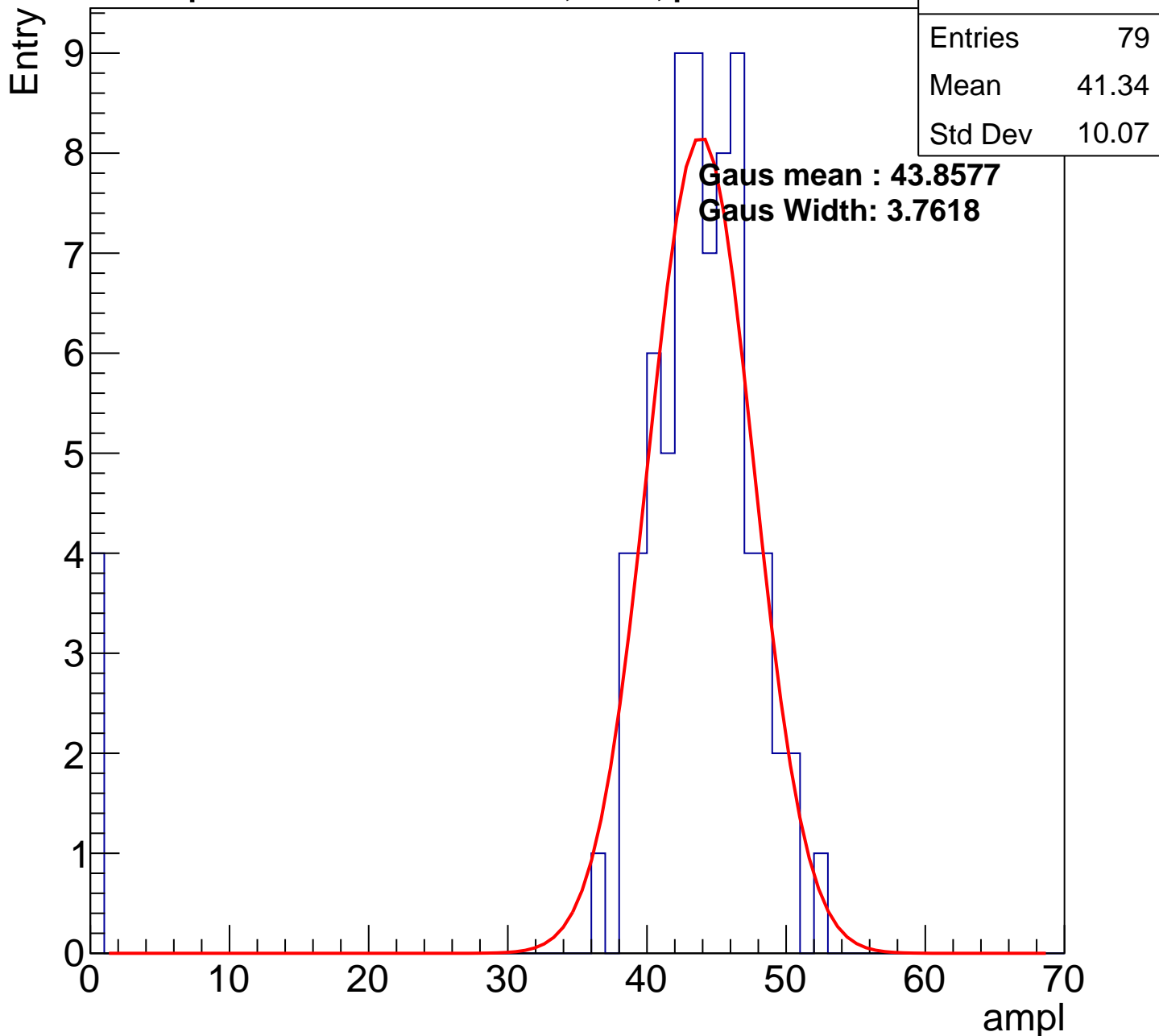
**Gaus mean : 38.4955**

**Gaus Width: 4.7901**



# B1L103S, U26-ch5, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

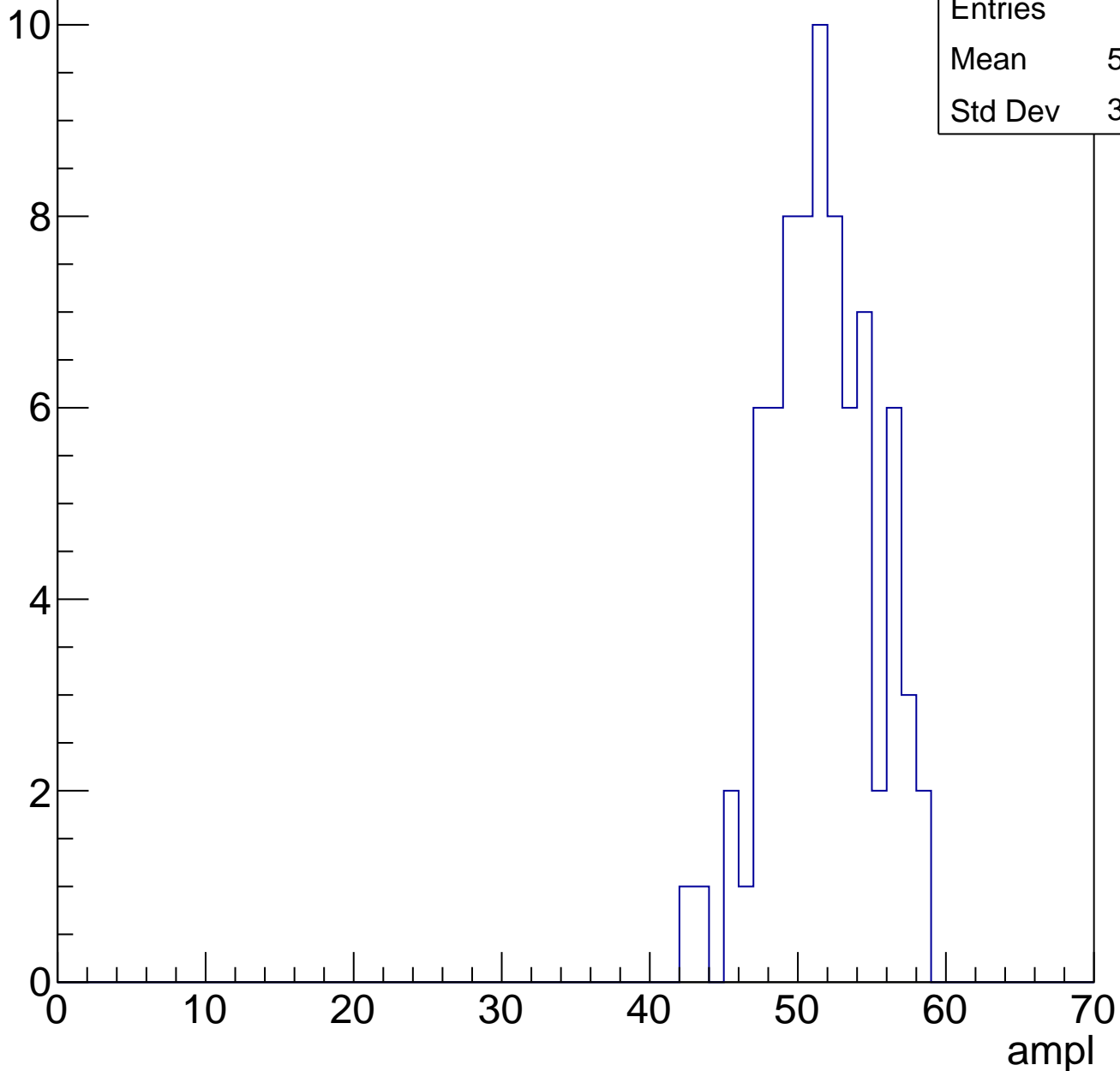


# B1L103S, U26-ch5, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	77
Mean	51.14
Std Dev	3.444

Entry



# B1L103S, U26-ch5, adc4

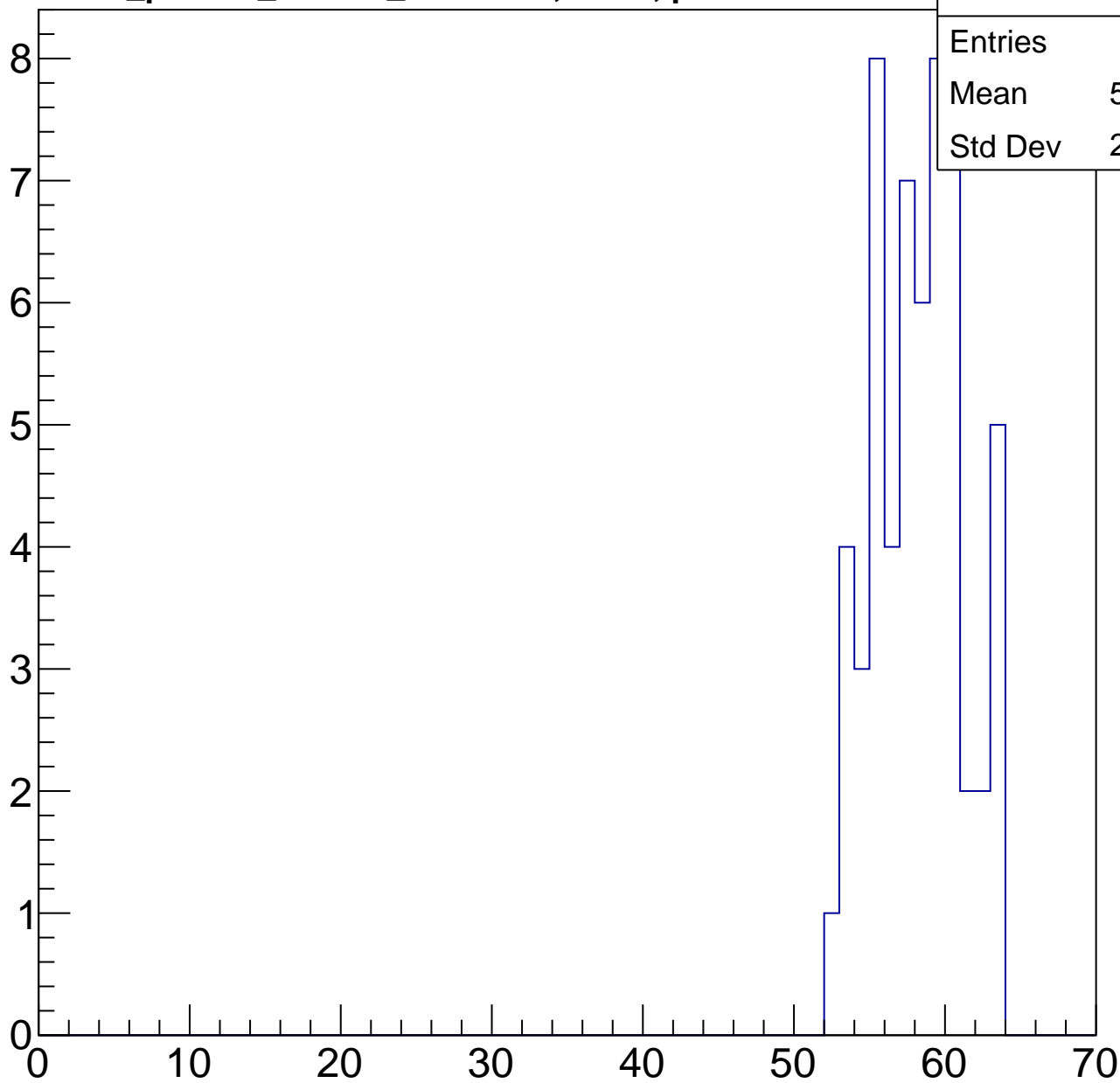
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	58
Mean	57.76
Std Dev	2.908

ampl

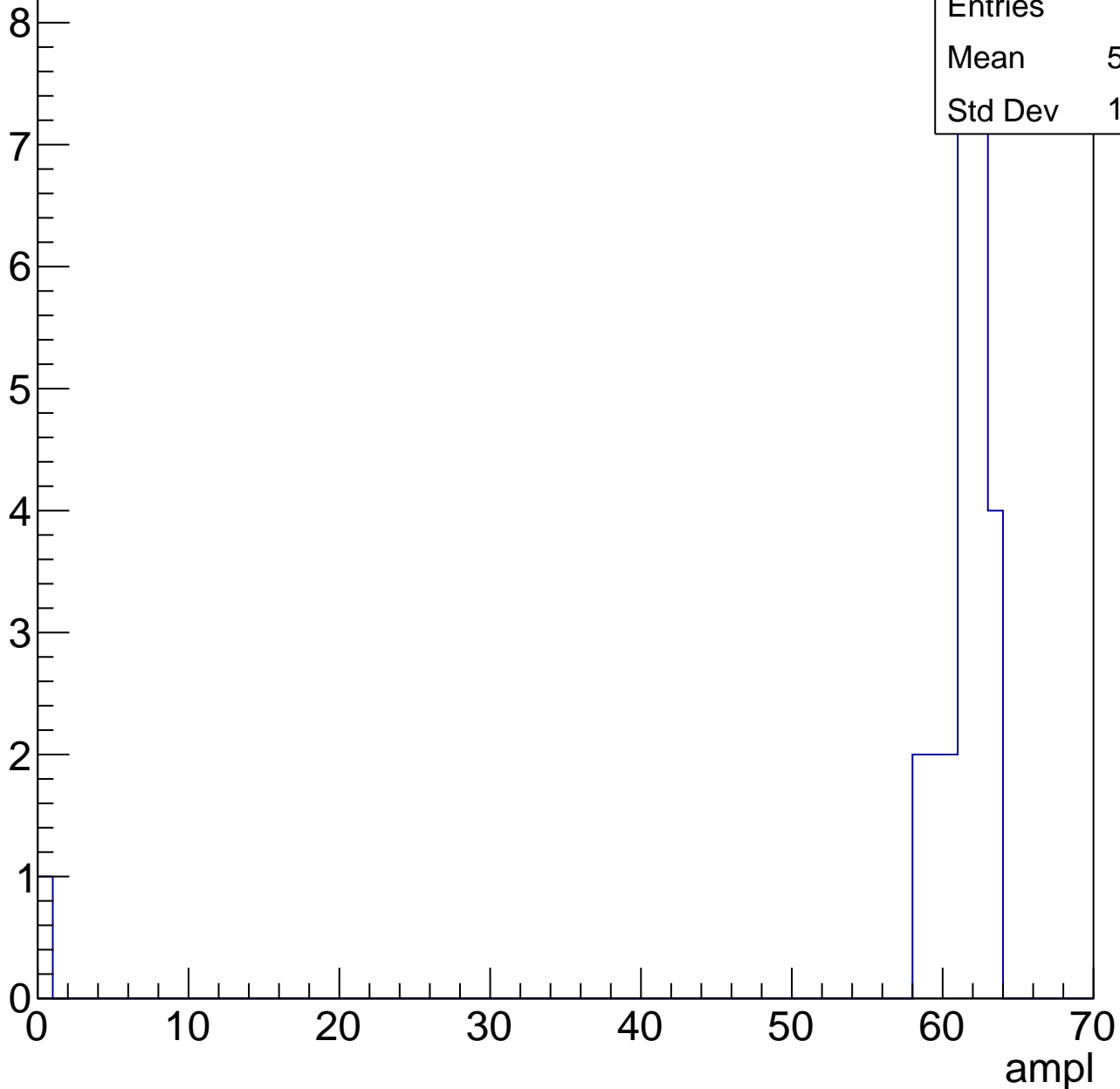


# B1L103S, U26-ch5, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	27
Mean	58.89
Std Dev	11.63



# B1L103S, U26-ch5, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



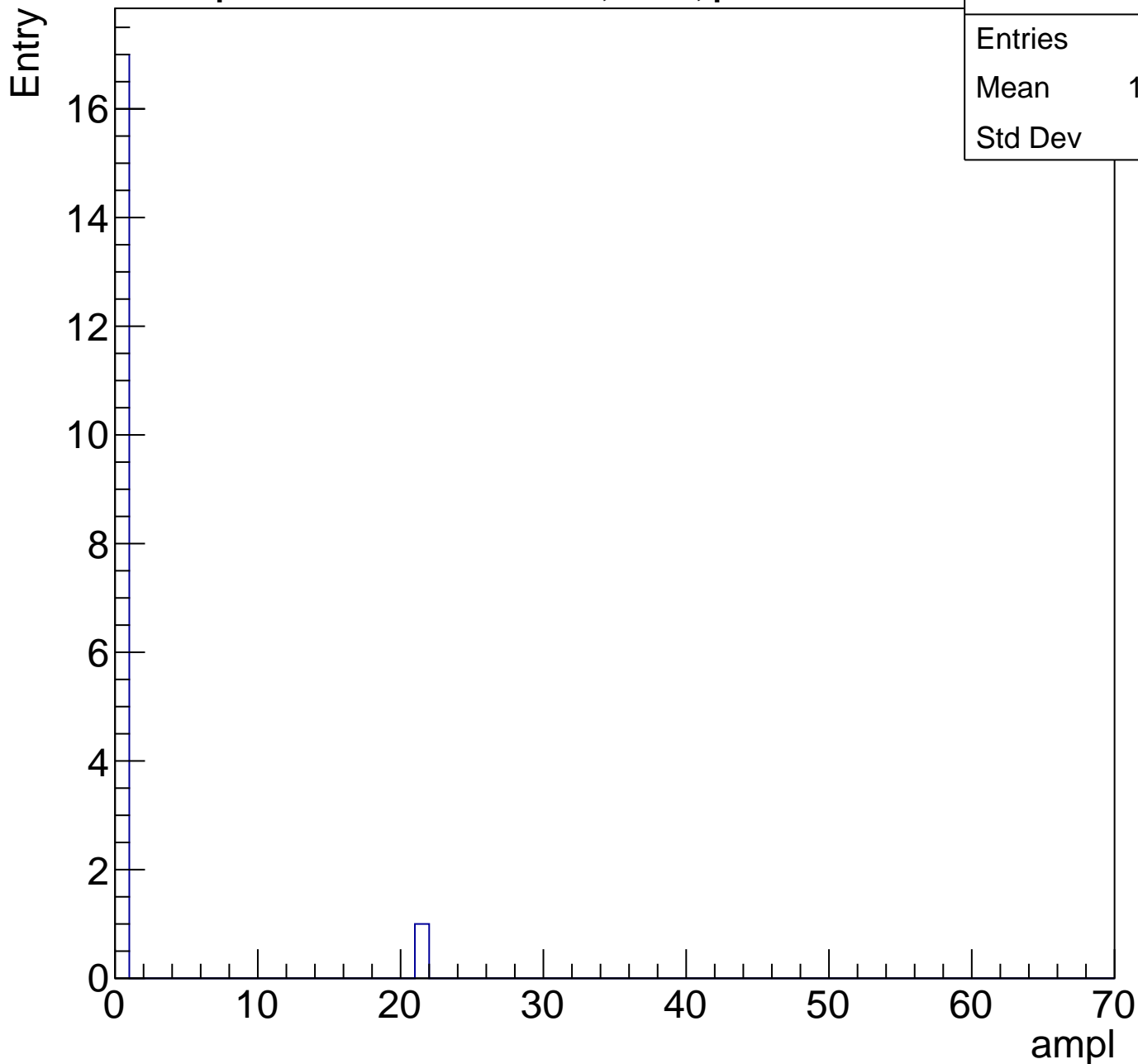
Entries	1
Mean	63
Std Dev	0



# B1L103S, U26-ch5, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	18
Mean	1.167
Std Dev	4.81



# B1L103S, U26-ch6, adc0

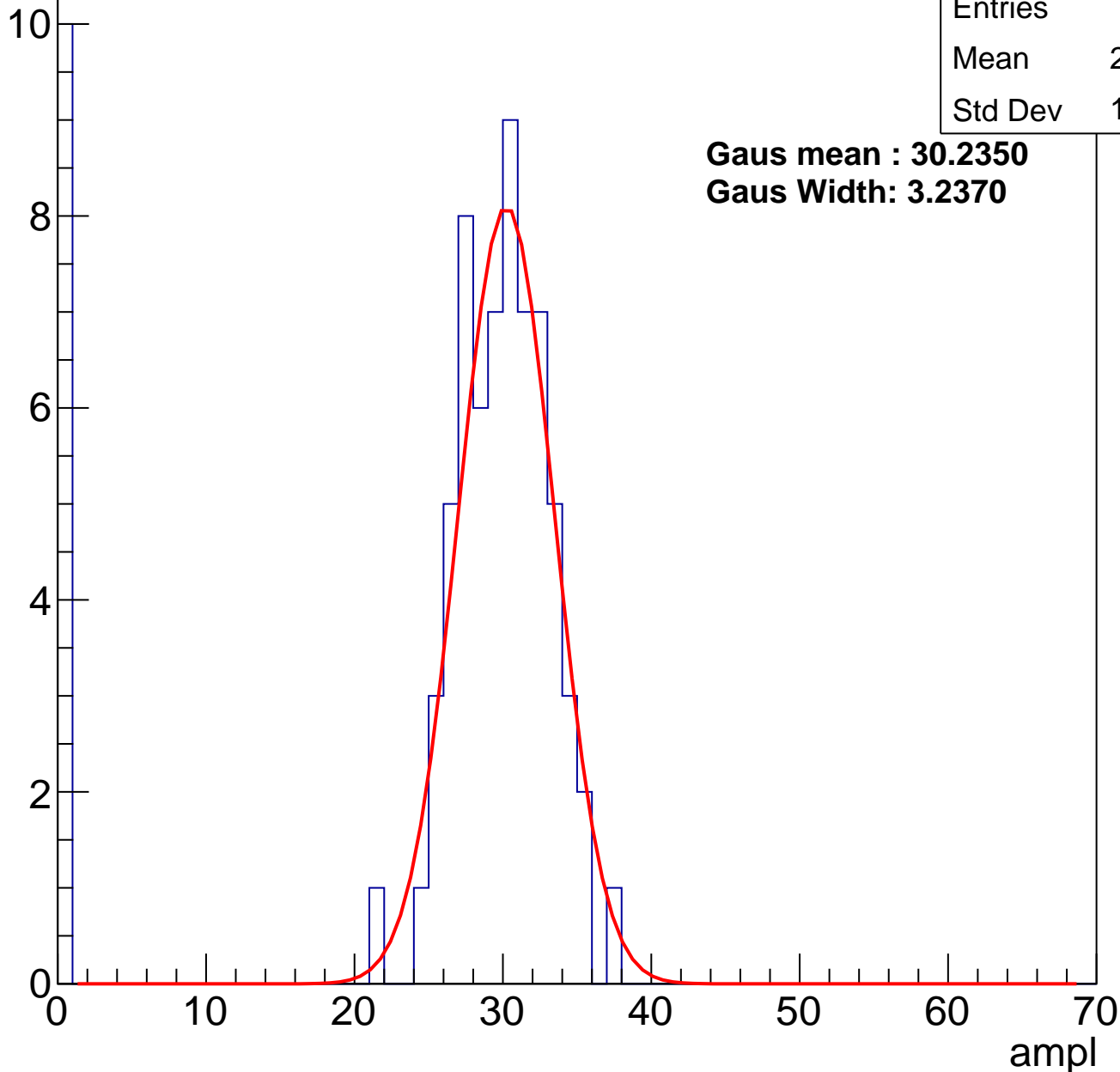
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	75
Mean	25.63
Std Dev	10.44

**Gaus mean : 30.2350**

**Gaus Width: 3.2370**

Entry



# B1L103S, U26-ch6, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

10

8

6

4

2

0

0

10

20

30

40

50

60

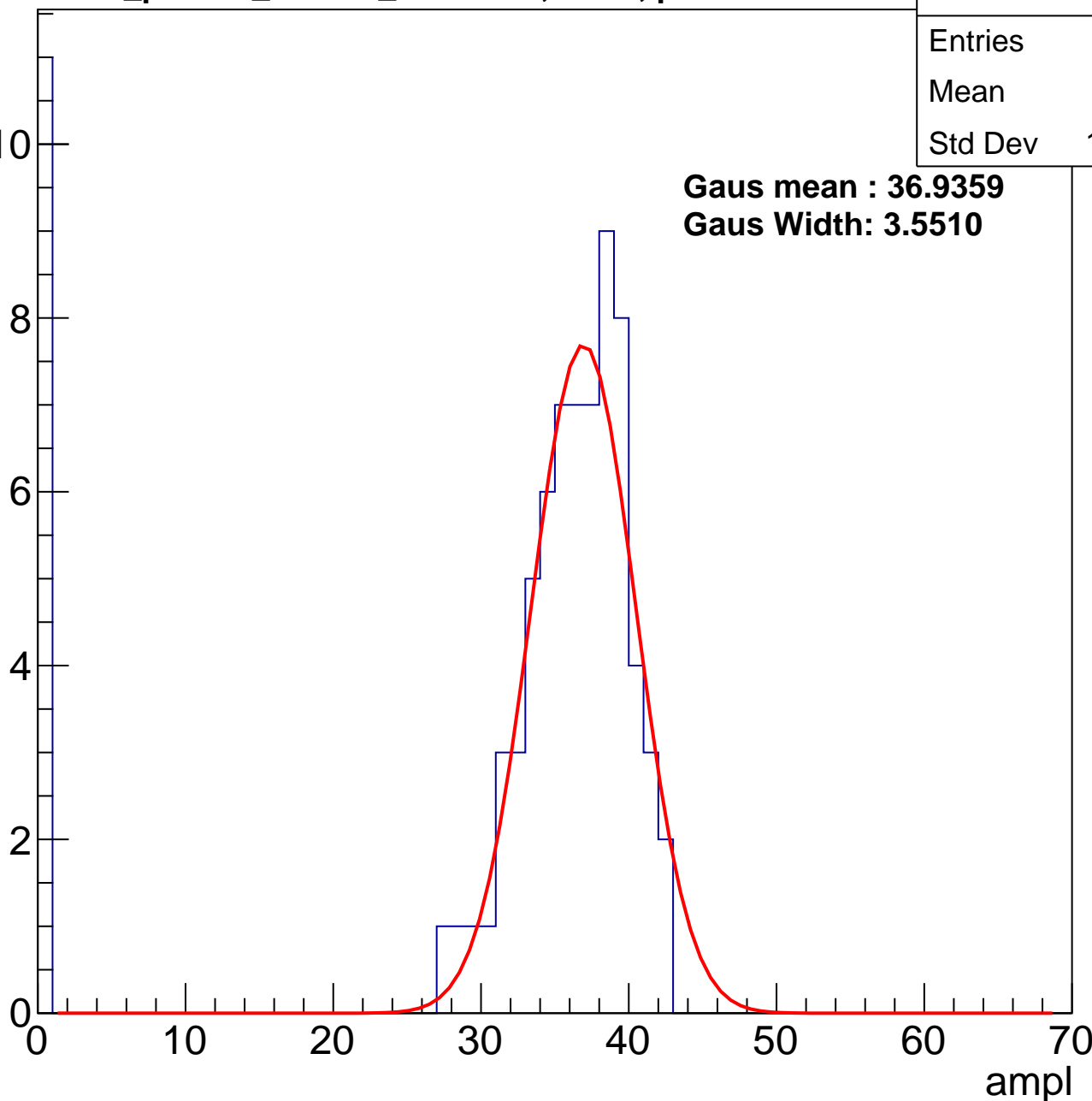
70

ampl

Entries	79
Mean	31
Std Dev	12.85

**Gaus mean : 36.9359**

**Gaus Width: 3.5510**



# B1L103S, U26-ch6, adc2

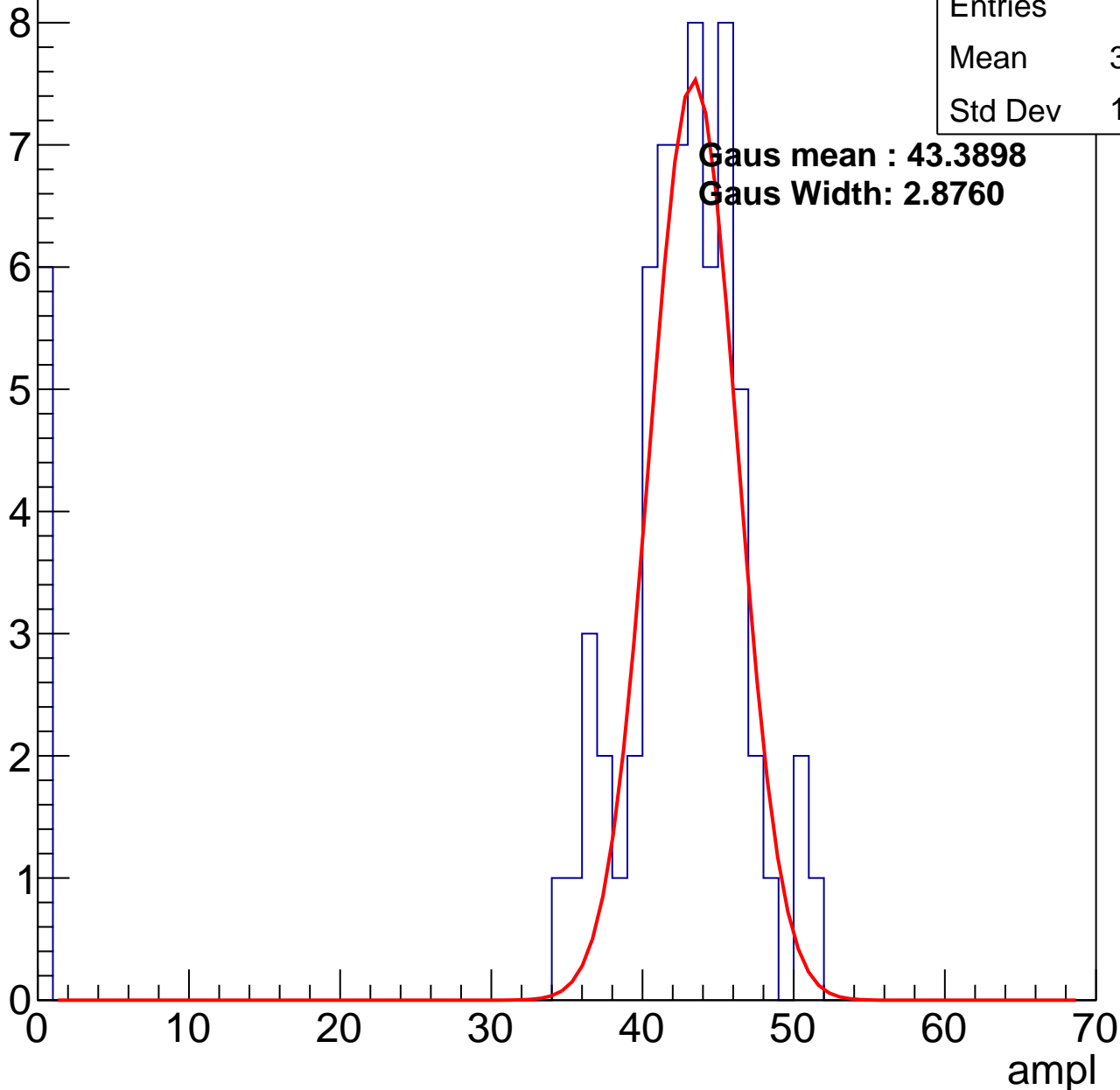
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	69
Mean	38.83
Std Dev	12.46

**Gaus mean : 43.3898**

**Gaus Width: 2.8760**



# B1L103S, U26-ch6, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

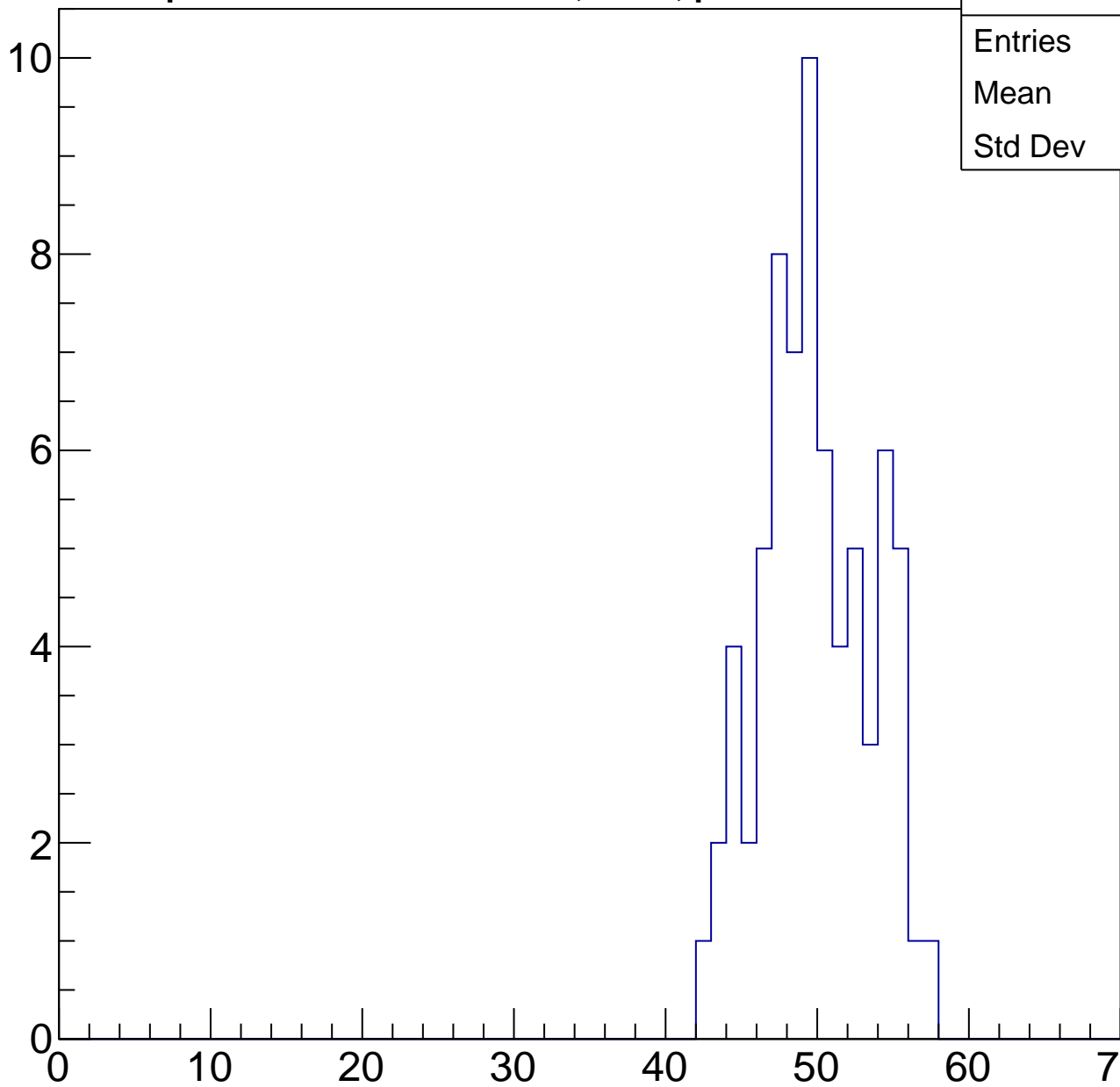
Entries	70
Mean	49.44
Std Dev	3.548

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

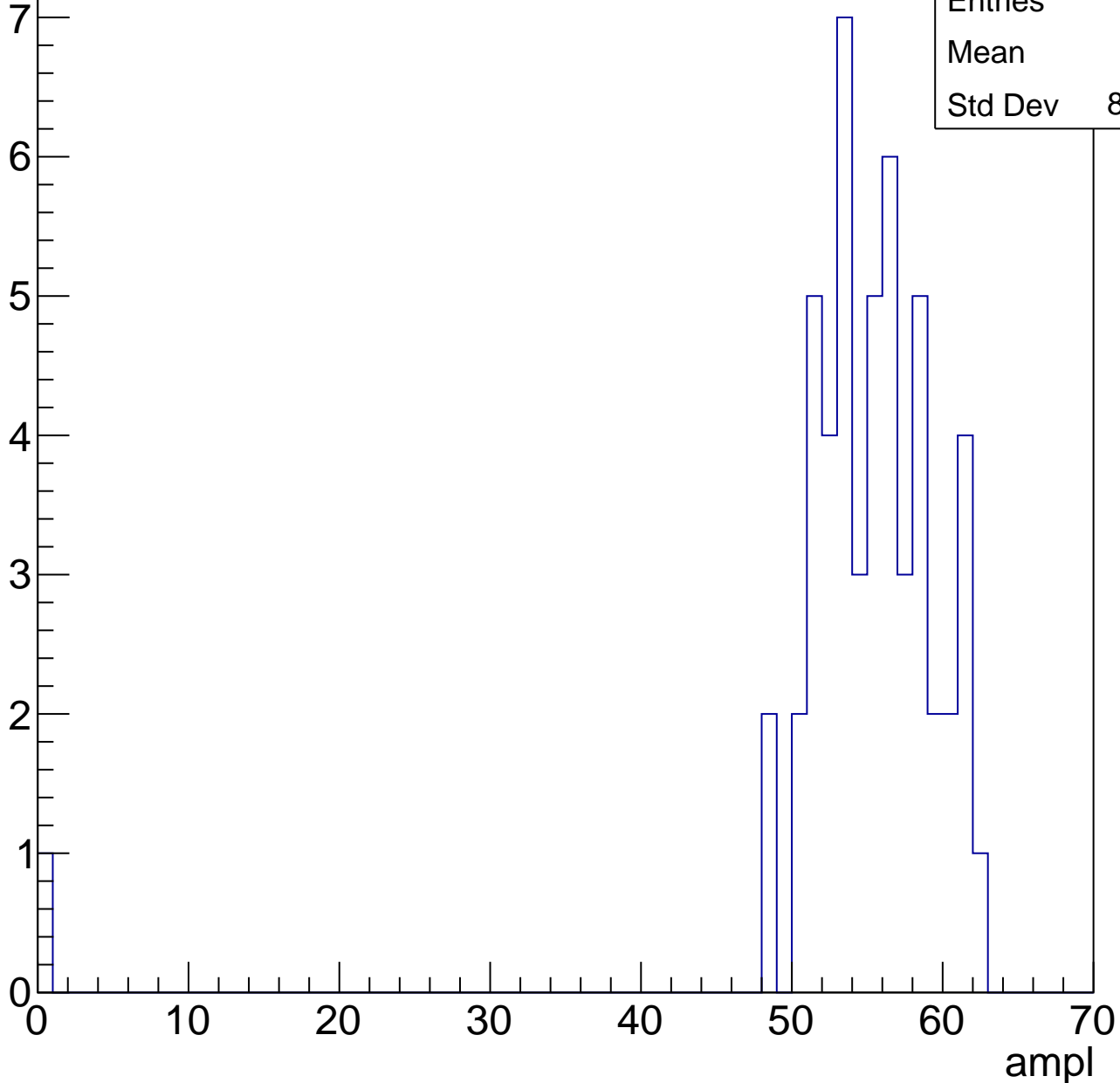


# B1L103S, U26-ch6, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

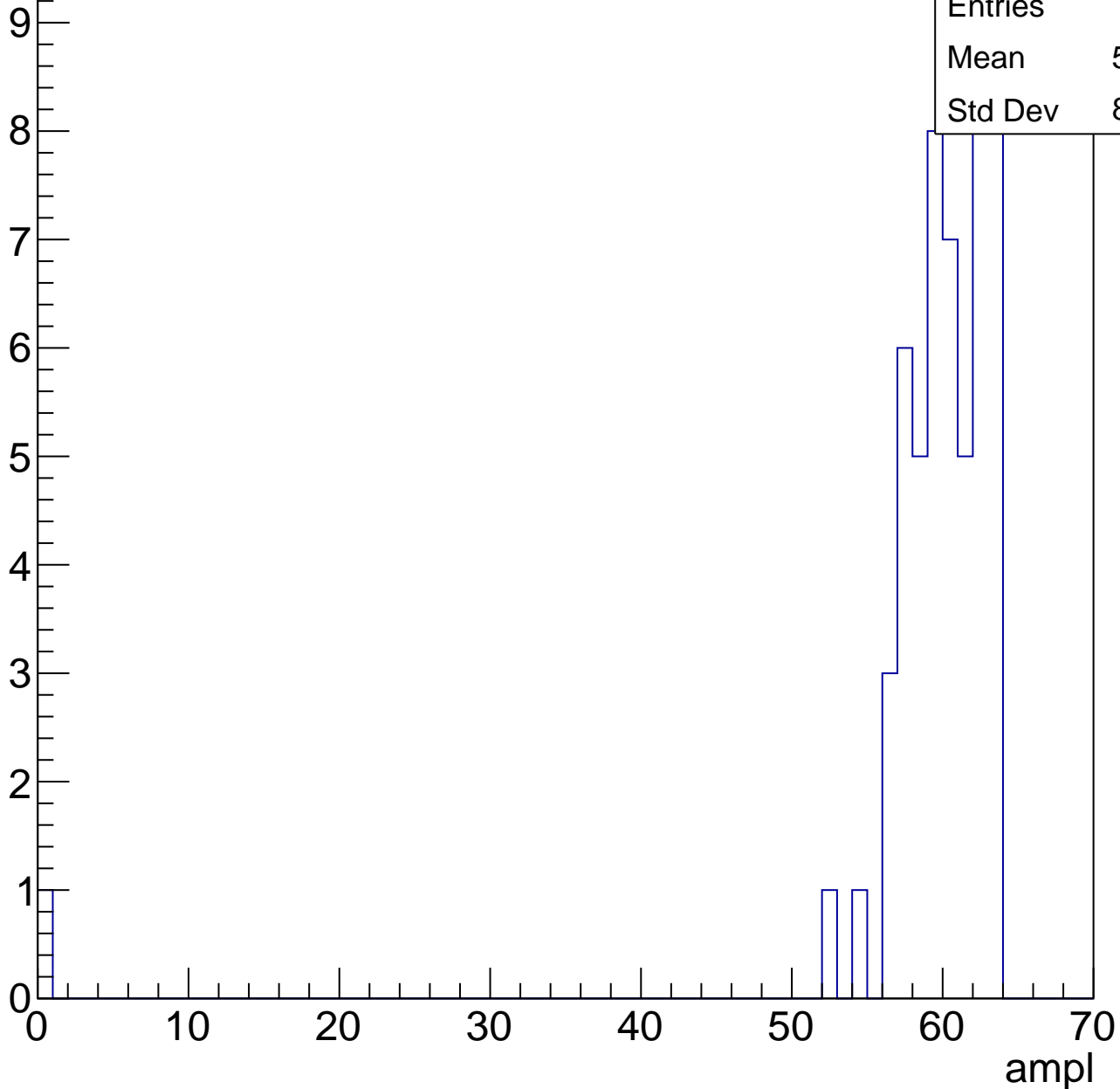
Entries	52
Mean	54
Std Dev	8.327



# B1L103S, U26-ch6, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



# B1L103S, U26-ch6, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry





# B1L103S, U26-ch6, adc7

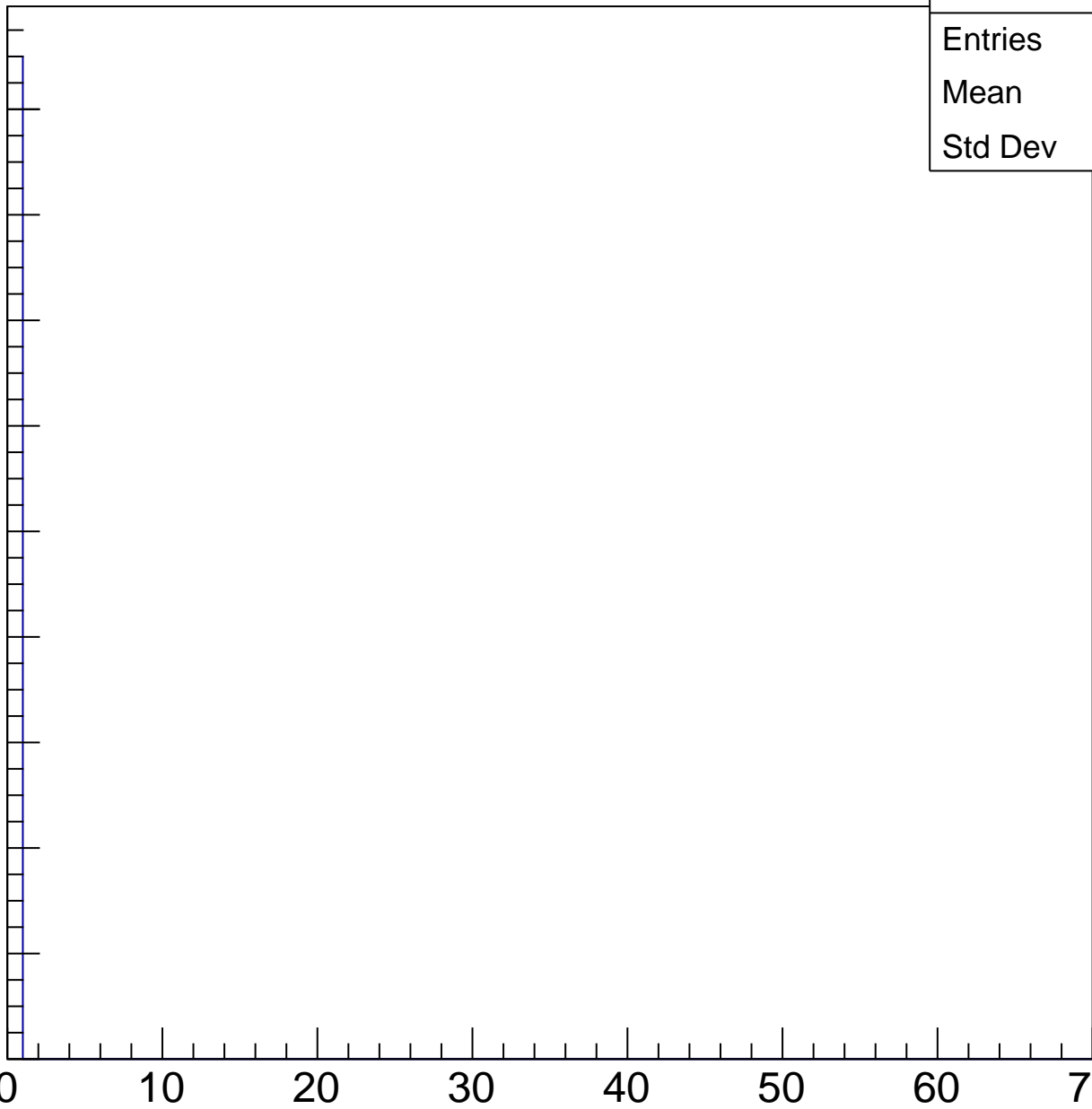
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

18  
16  
14  
12  
10  
8  
6  
4  
2  
0

Entries	19
Mean	0
Std Dev	0

ampl



# B1L103S, U26-ch7, adc0

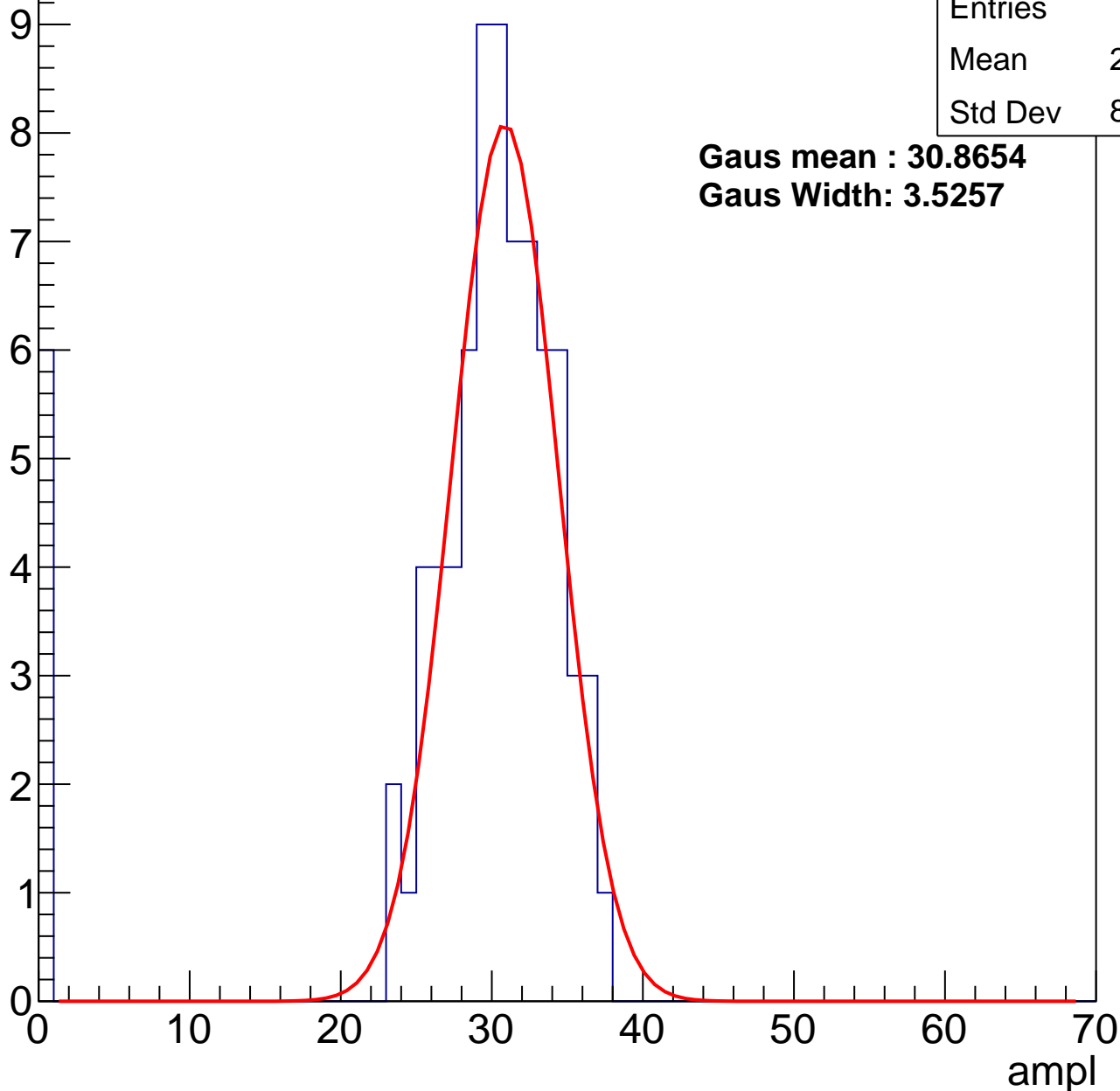
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	78
Mean	27.87
Std Dev	8.646

**Gaus mean : 30.8654**

**Gaus Width: 3.5257**



# B1L103S, U26-ch7, adc1

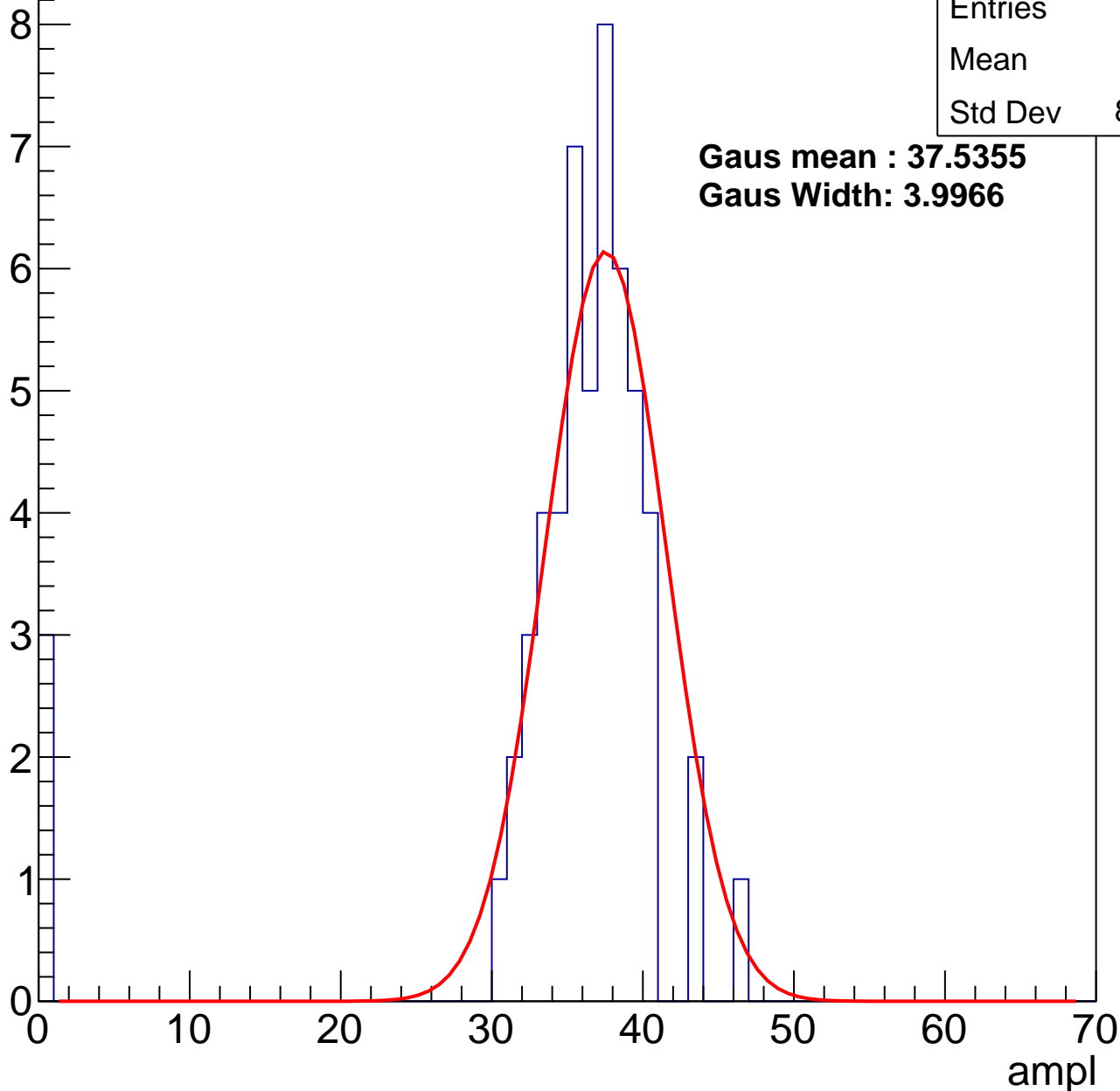
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	55
Mean	34.4
Std Dev	8.821

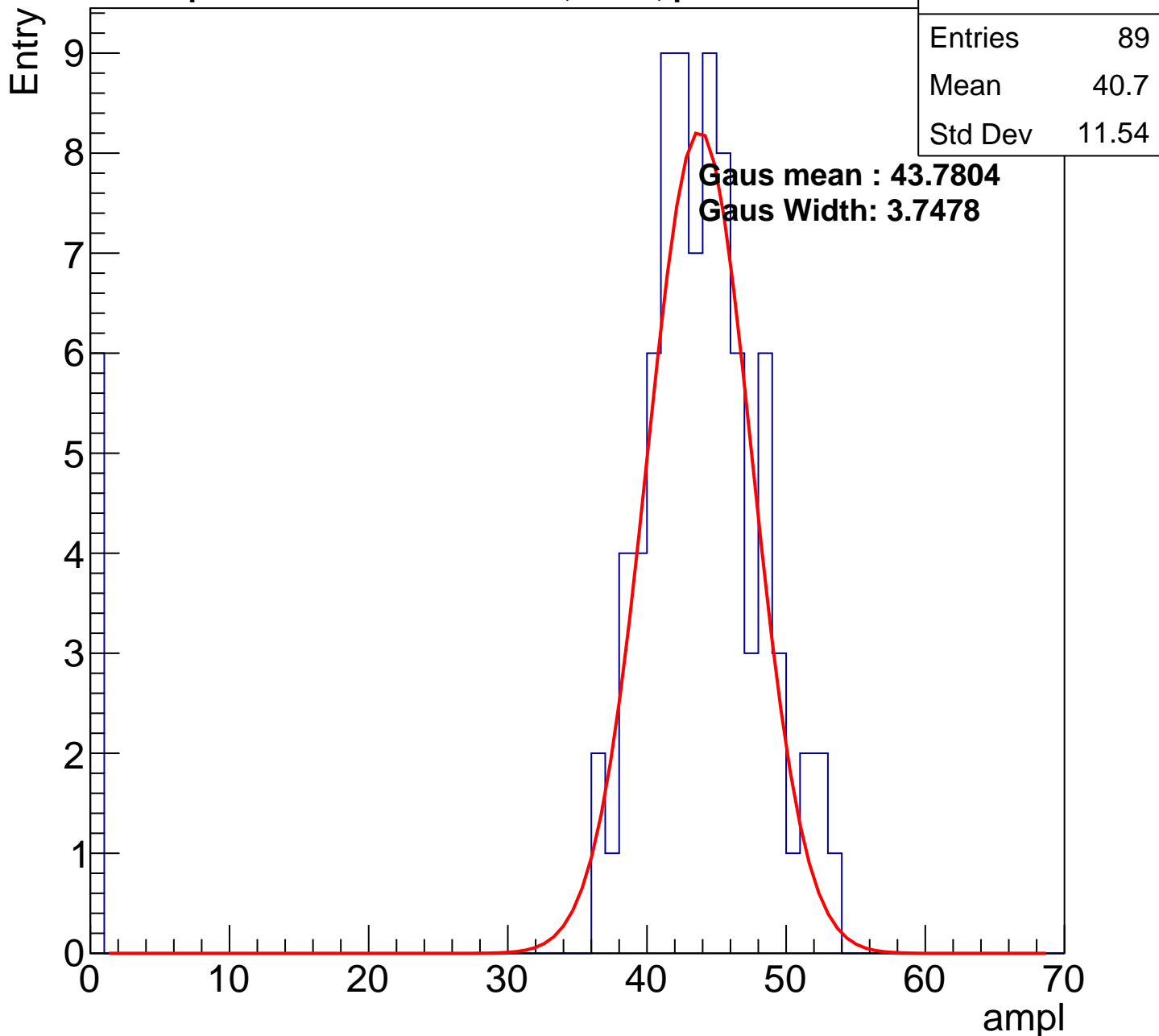
**Gaus mean : 37.5355**

**Gaus Width: 3.9966**



# B1L103S, U26-ch7, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

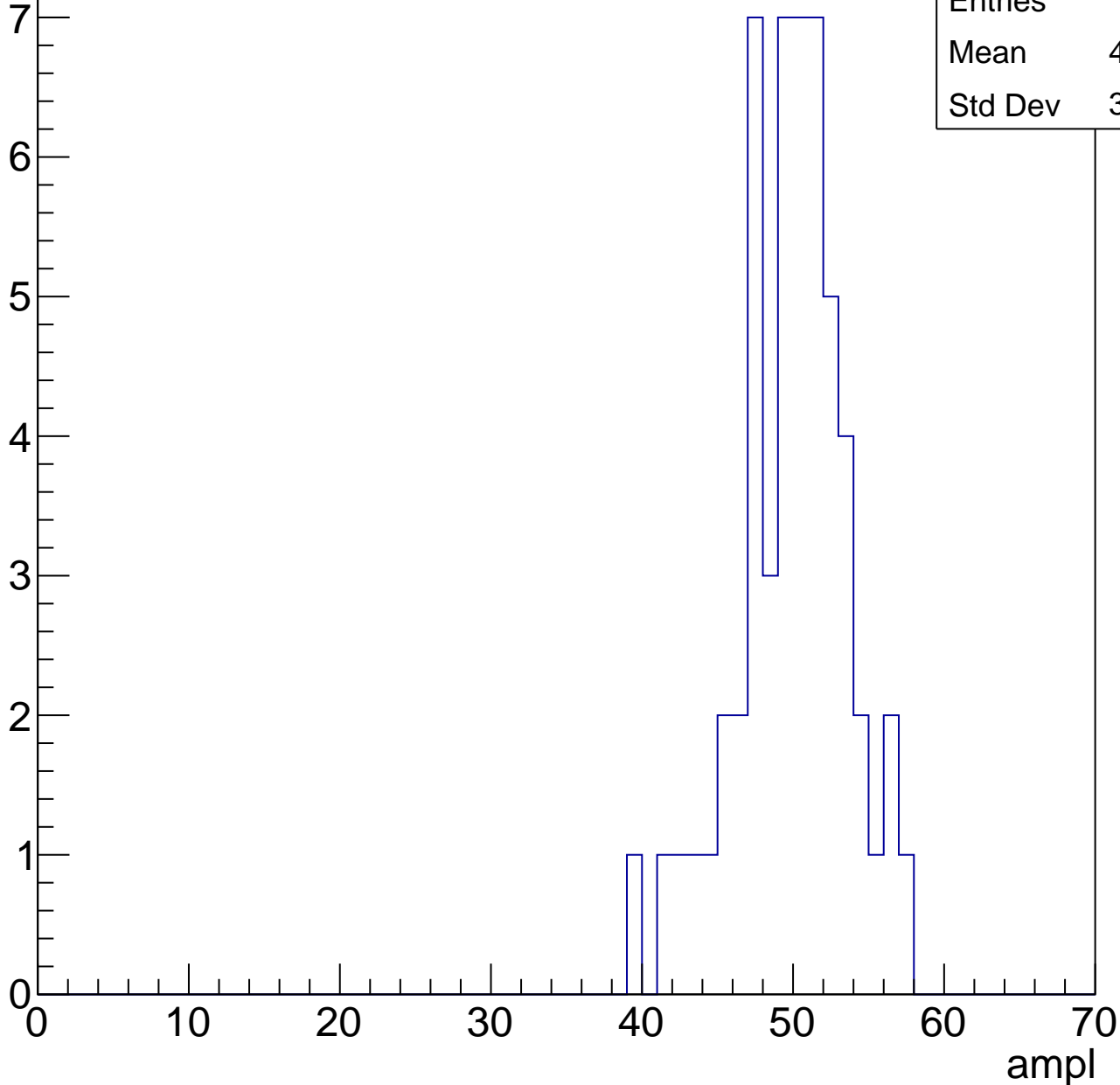


# B1L103S, U26-ch7, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	55
Mean	49.42
Std Dev	3.662

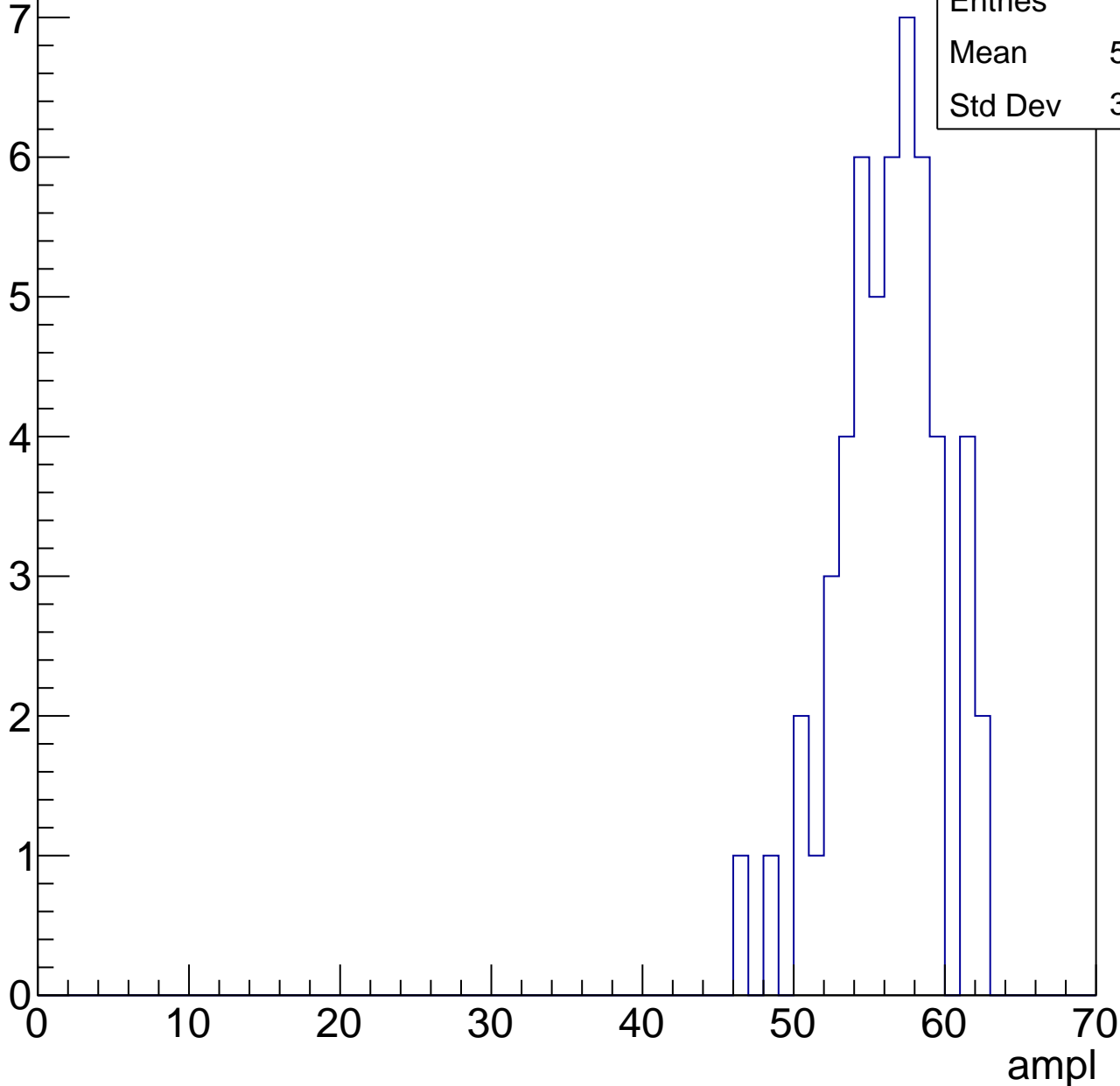


# B1L103S, U26-ch7, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	52
Mean	55.75
Std Dev	3.424

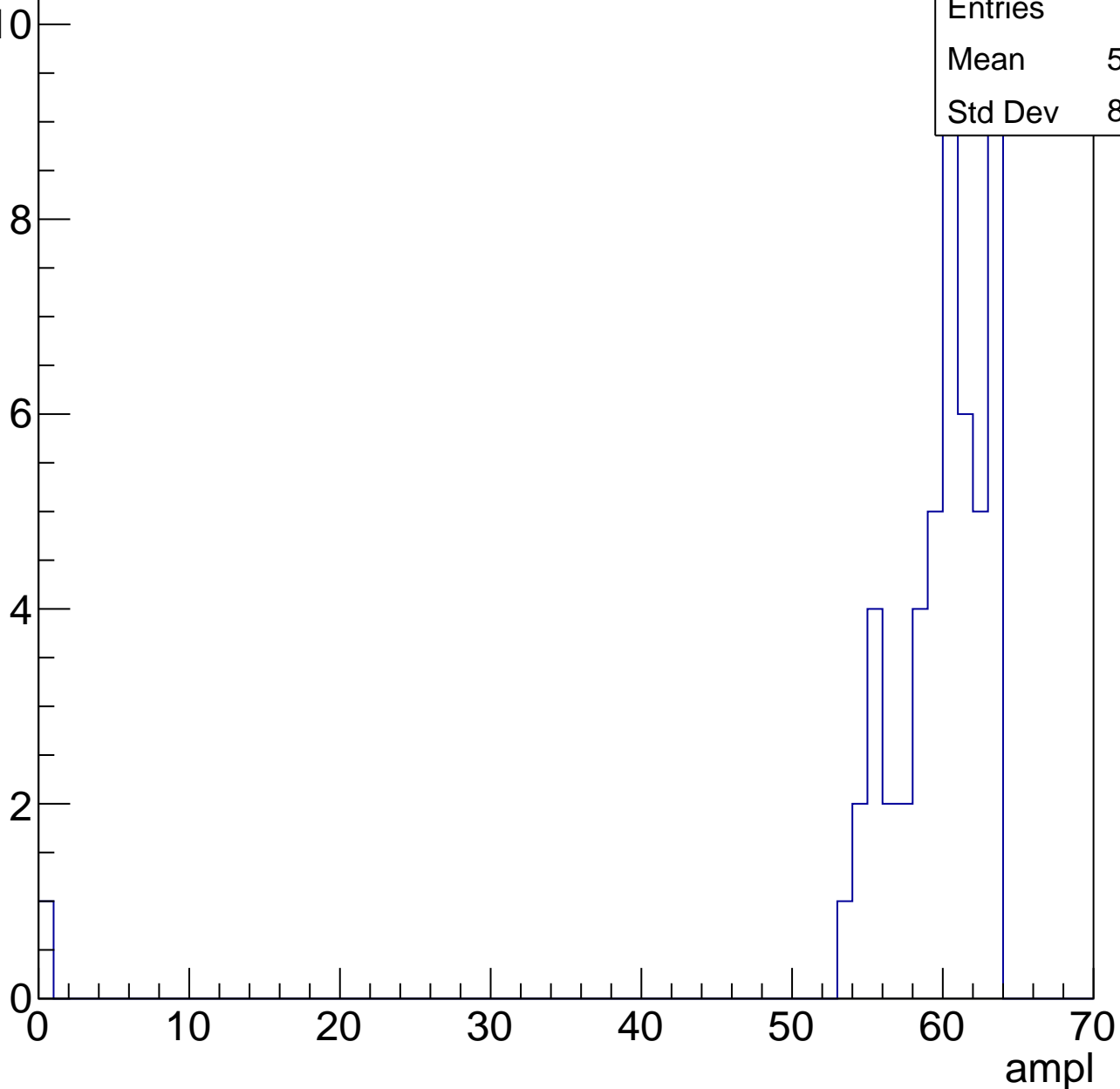


# B1L103S, U26-ch7, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

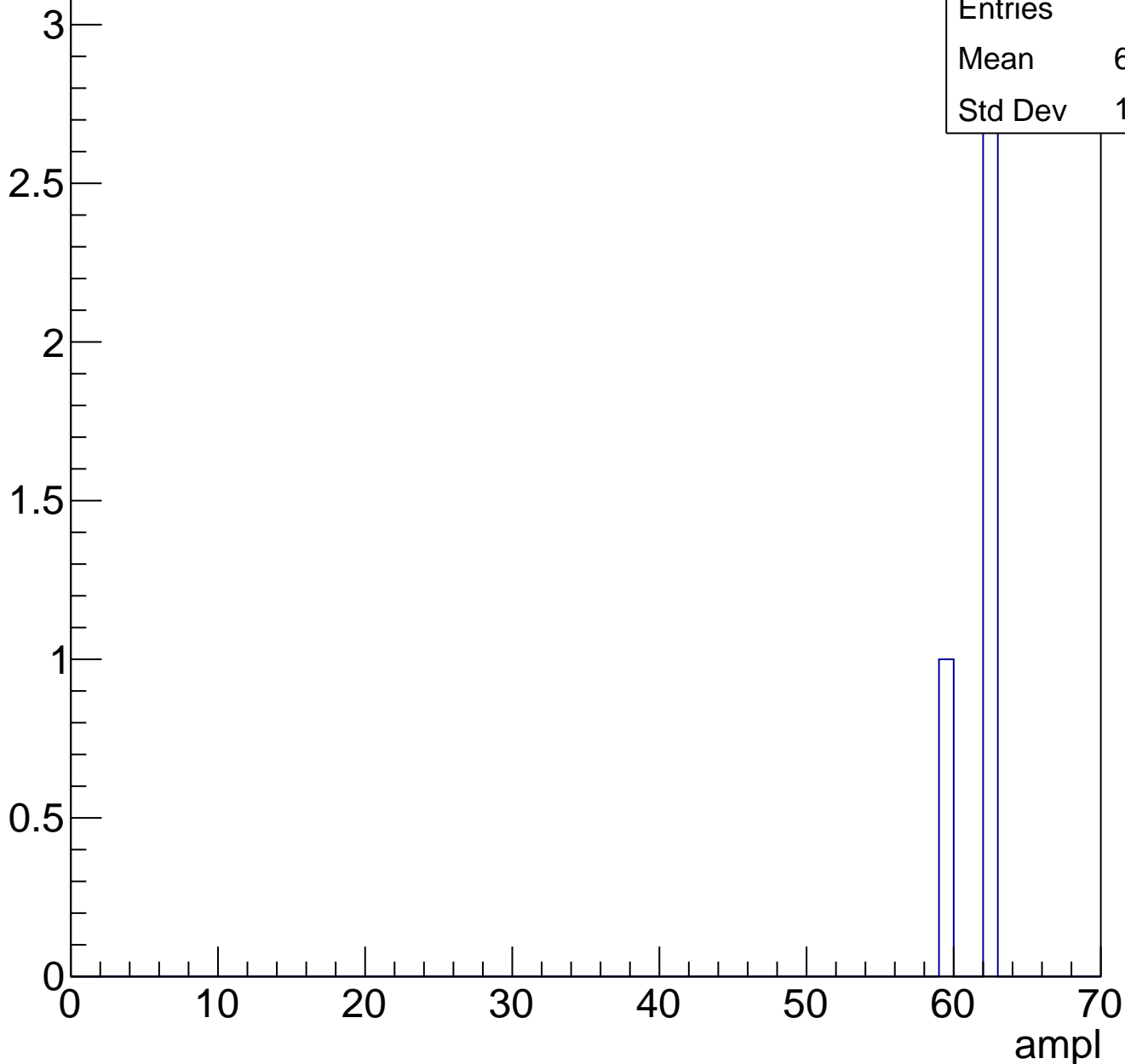
Entries	52
Mean	58.46
Std Dev	8.643



# B1L103S, U26-ch7, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry





# B1L103S, U26-ch7, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



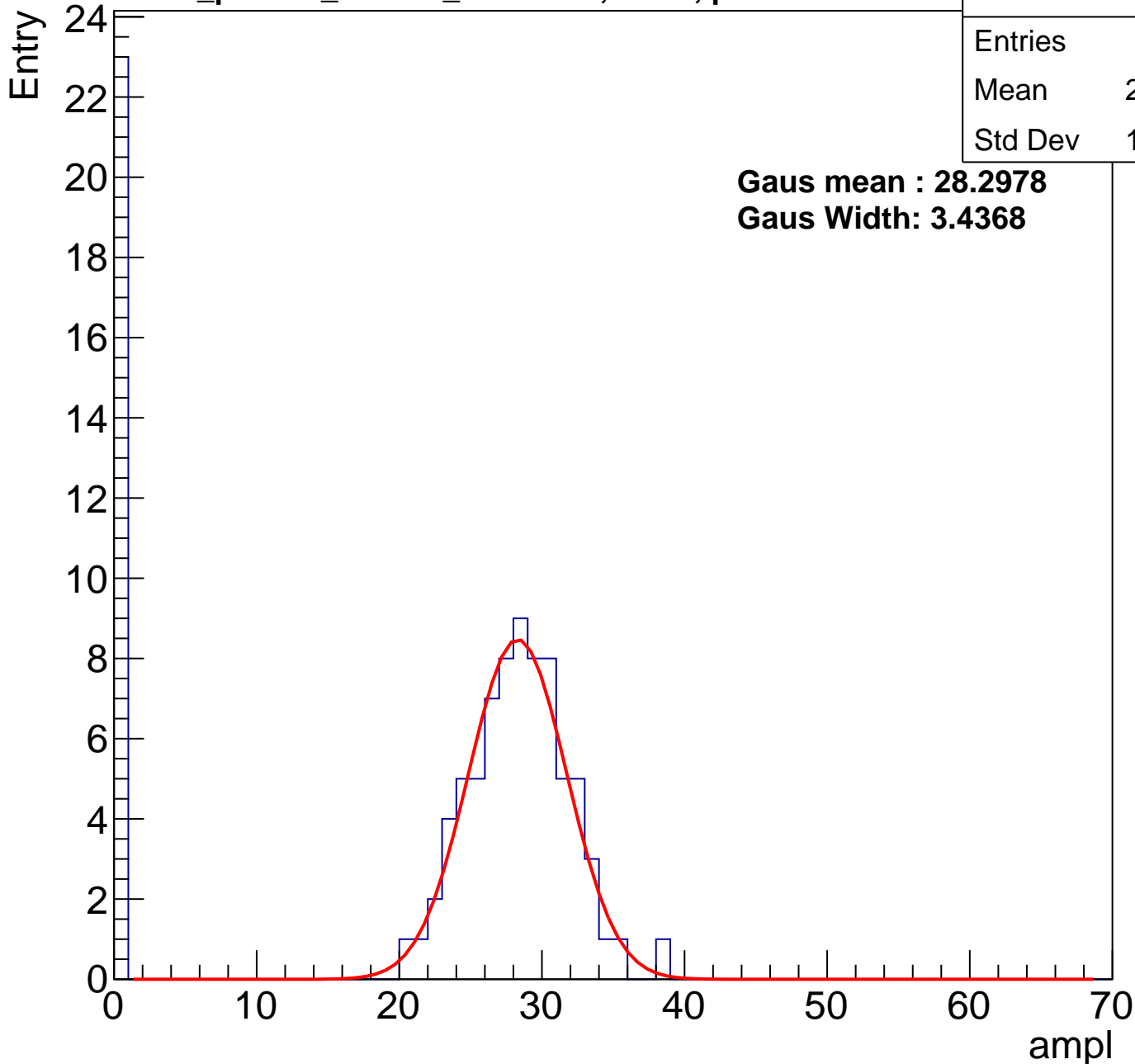
# B1L103S, U26-ch8, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	97
Mean	21.29
Std Dev	12.24

**Gaus mean : 28.2978**

**Gaus Width: 3.4368**



# B1L103S, U26-ch8, adc1

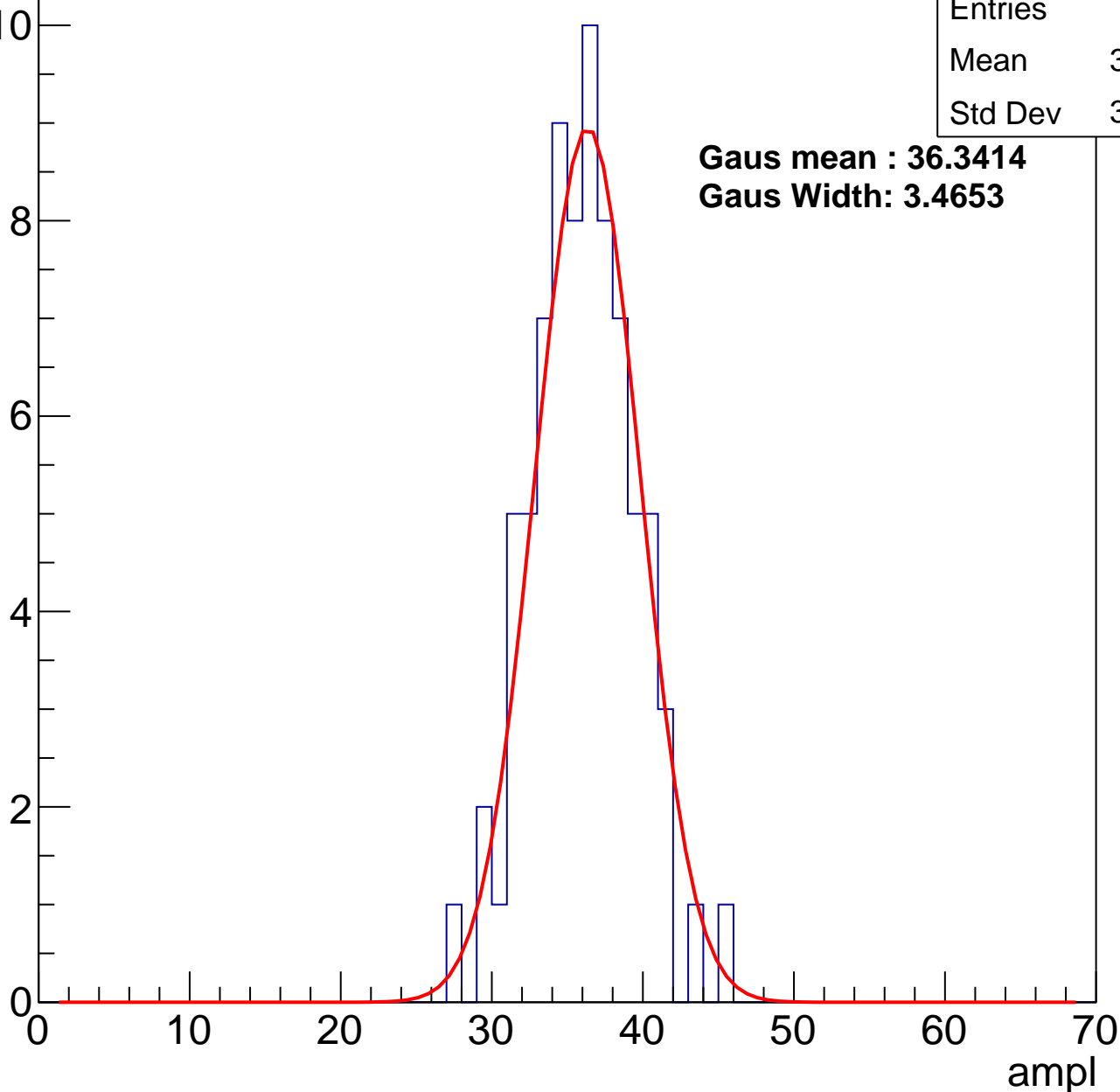
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	78
Mean	35.58
Std Dev	3.357

**Gaus mean : 36.3414**

**Gaus Width: 3.4653**



# B1L103S, U26-ch8, adc2

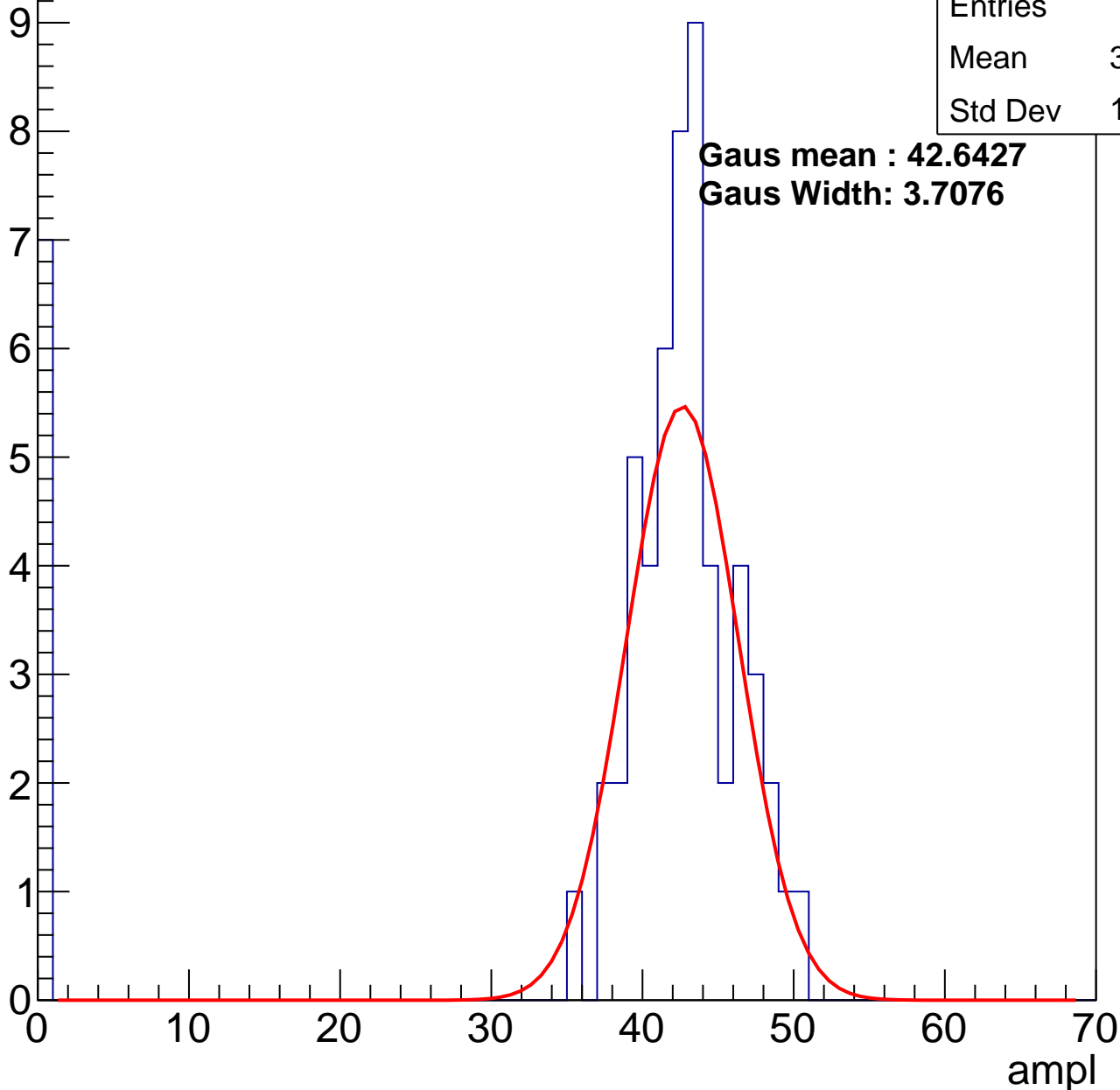
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	61
Mean	37.62
Std Dev	13.88

**Gaus mean : 42.6427**

**Gaus Width: 3.7076**

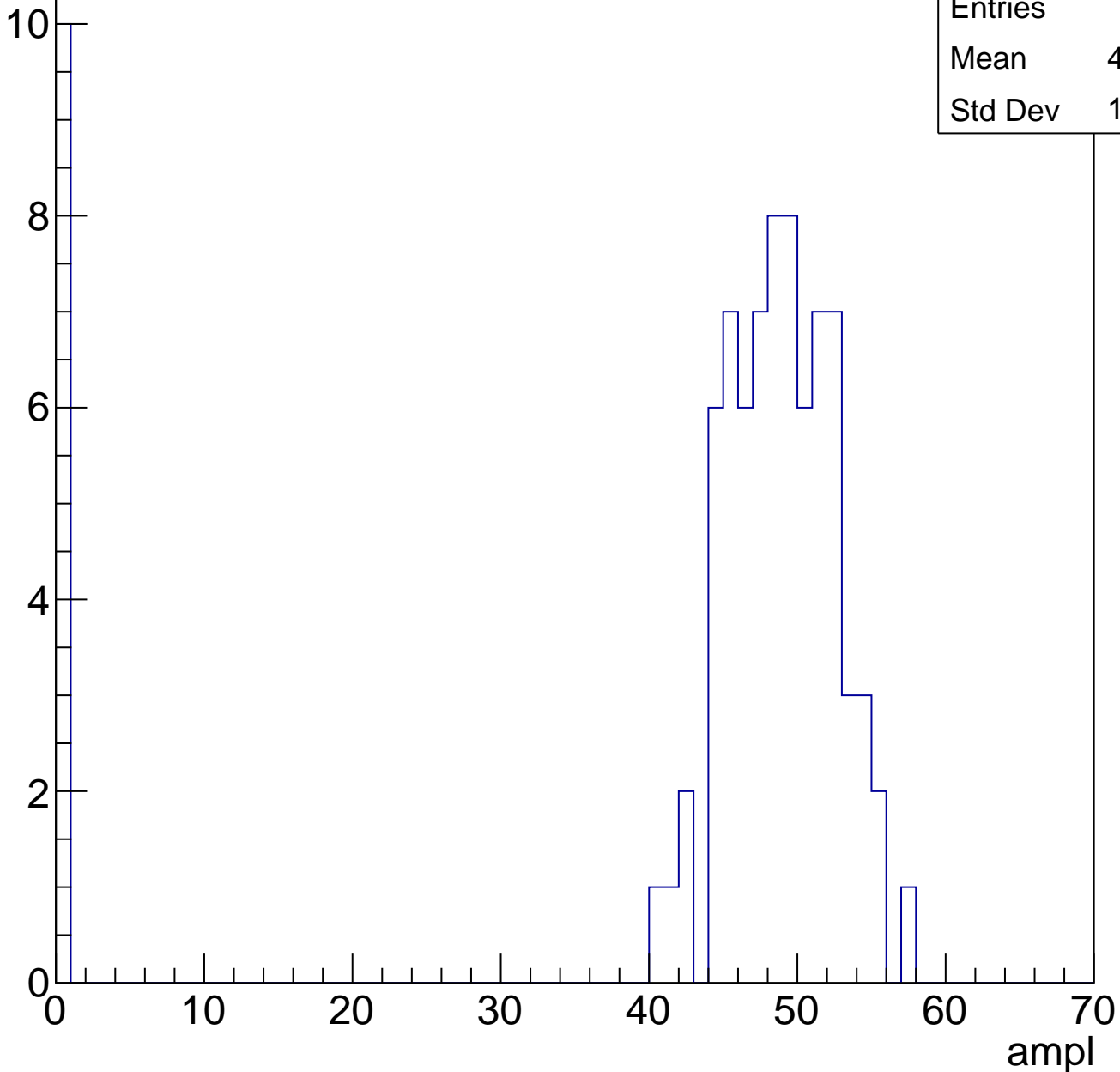


# B1L103S, U26-ch8, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	85
Mean	42.75
Std Dev	15.96

Entry

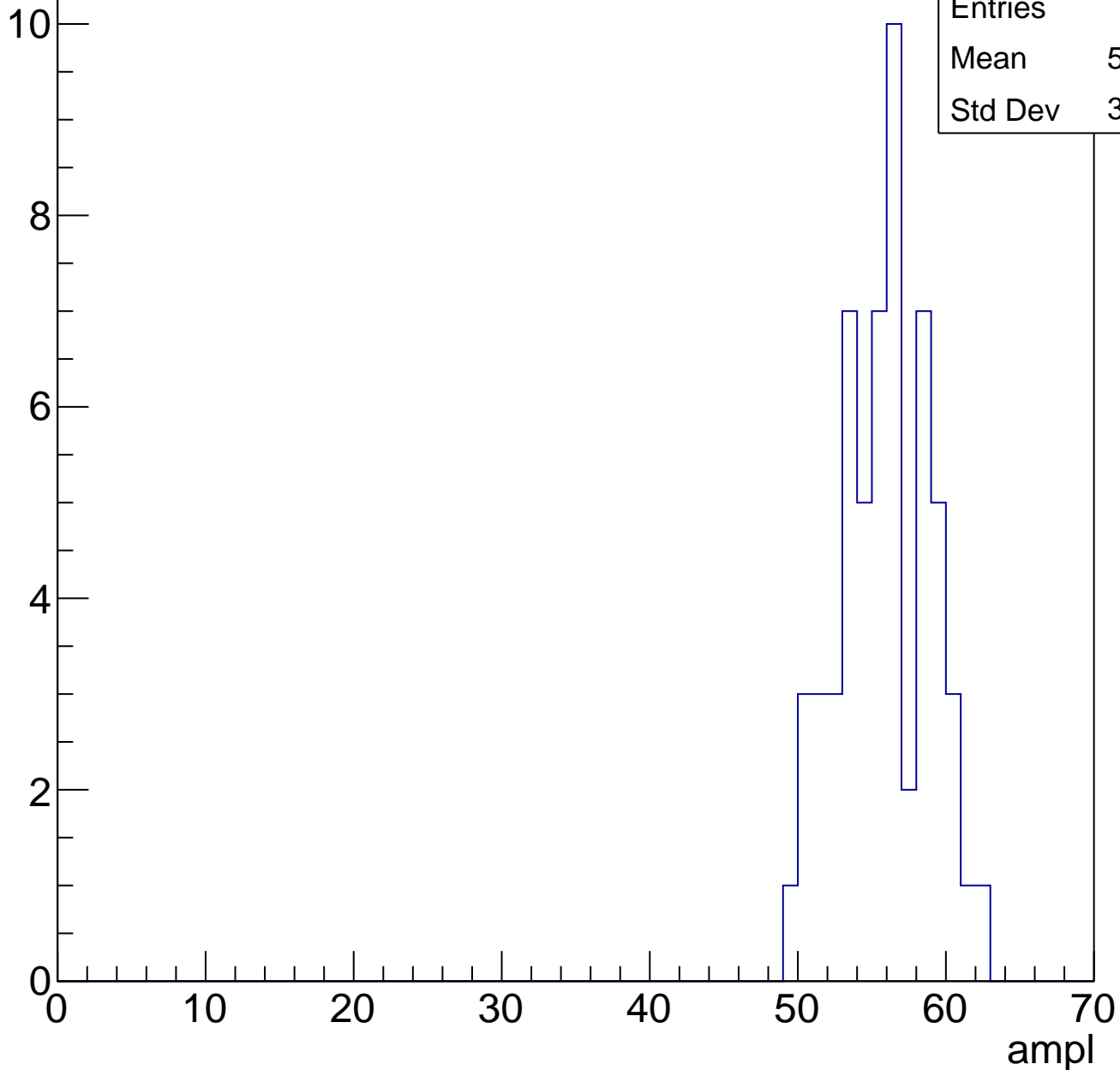


# B1L103S, U26-ch8, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	58
Mean	55.38
Std Dev	3.028

Entry

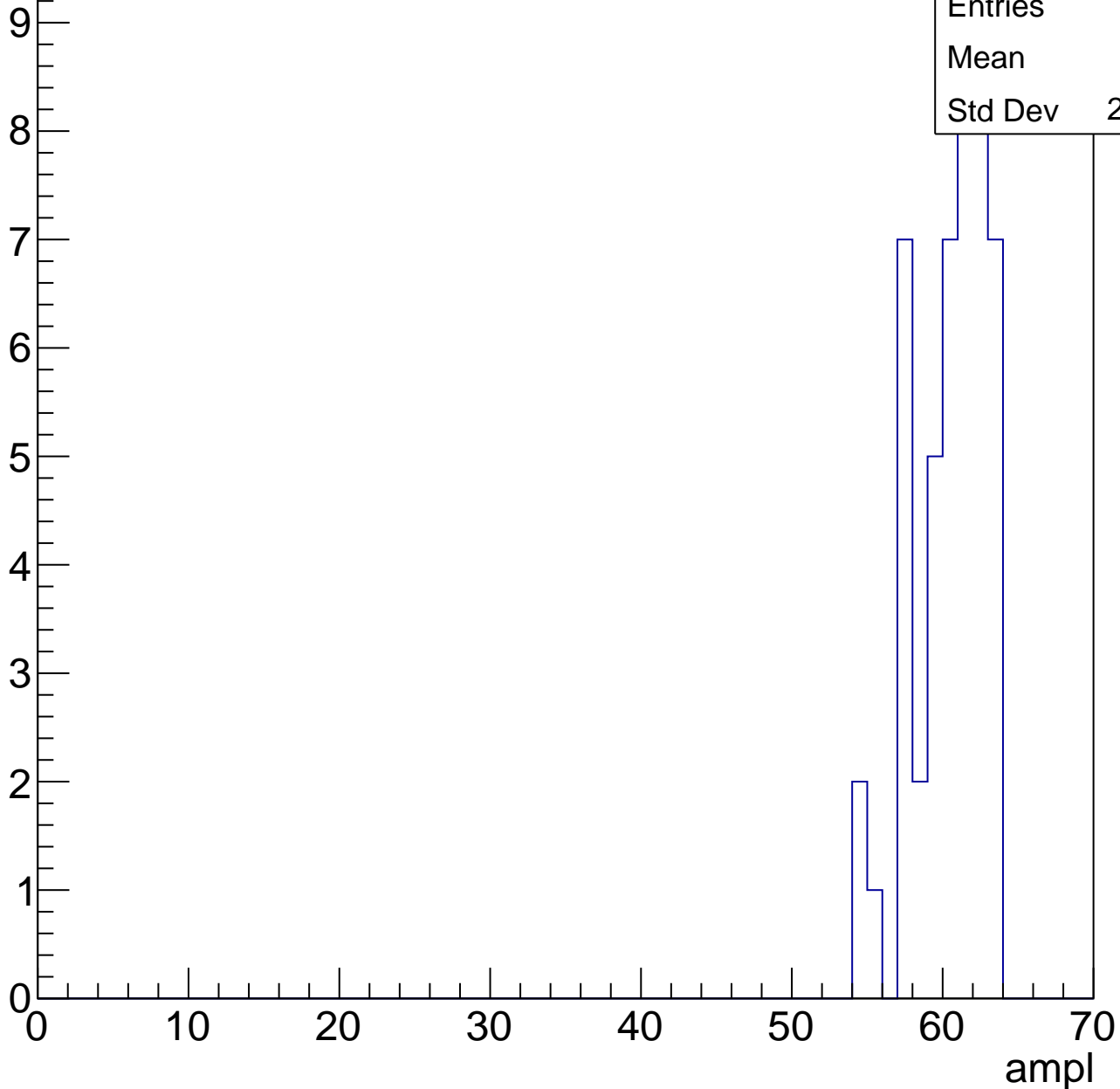


# B1L103S, U26-ch8, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

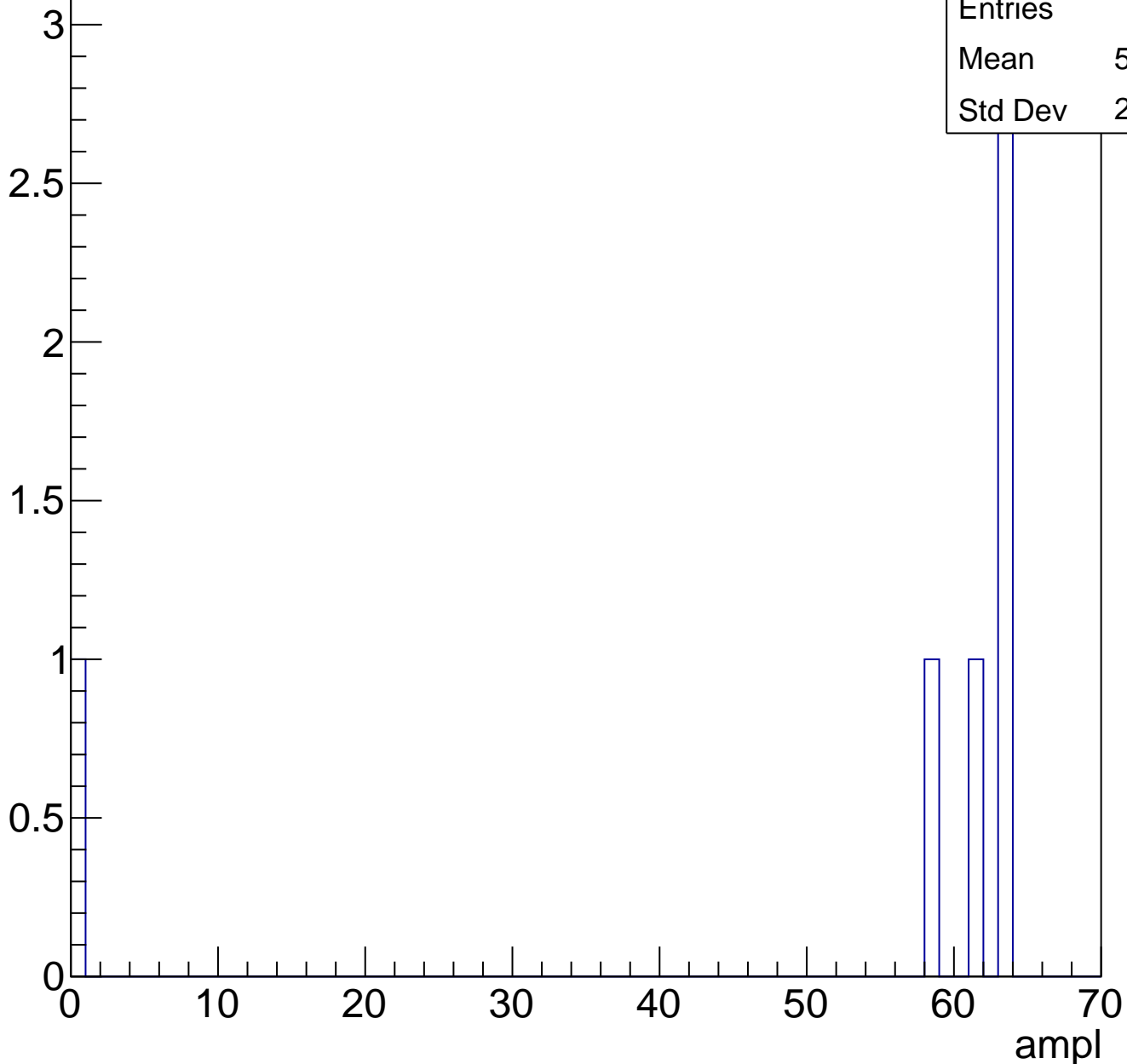
Entries	48
Mean	60
Std Dev	2.415



# B1L103S, U26-ch8, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry





# B1L103S, U26-ch8, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

18  
16  
14  
12  
10  
8  
6  
4  
2  
0

Entries	19
Mean	0
Std Dev	0

ampl

# B1L103S, U26-ch9, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	103
Mean	25.5
Std Dev	8.576

**Gaus mean : 28.4921**

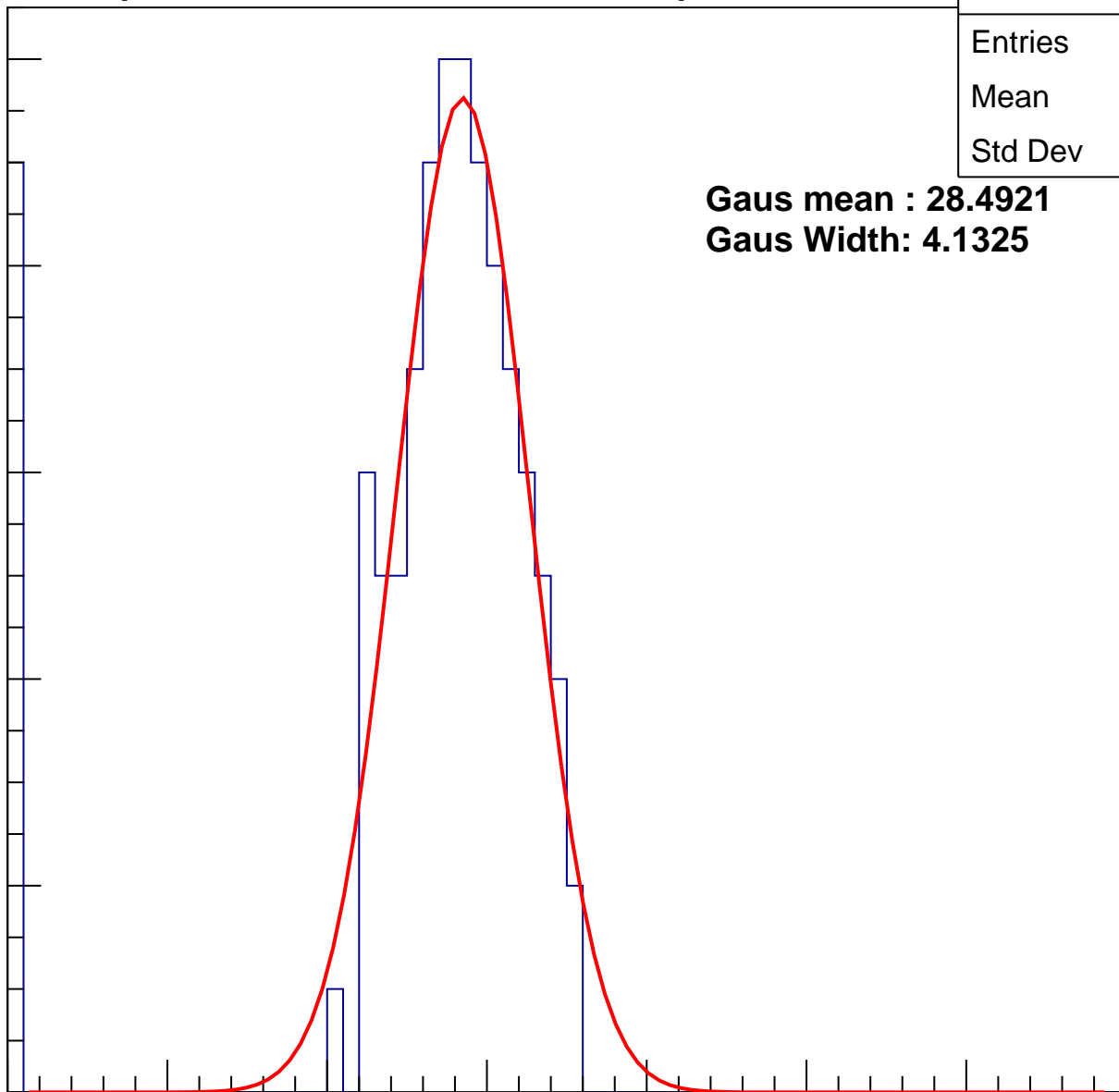
**Gaus Width: 4.1325**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B1L103S, U26-ch9, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	61
Mean	34.87
Std Dev	5.635

**Gaus mean : 35.9765**

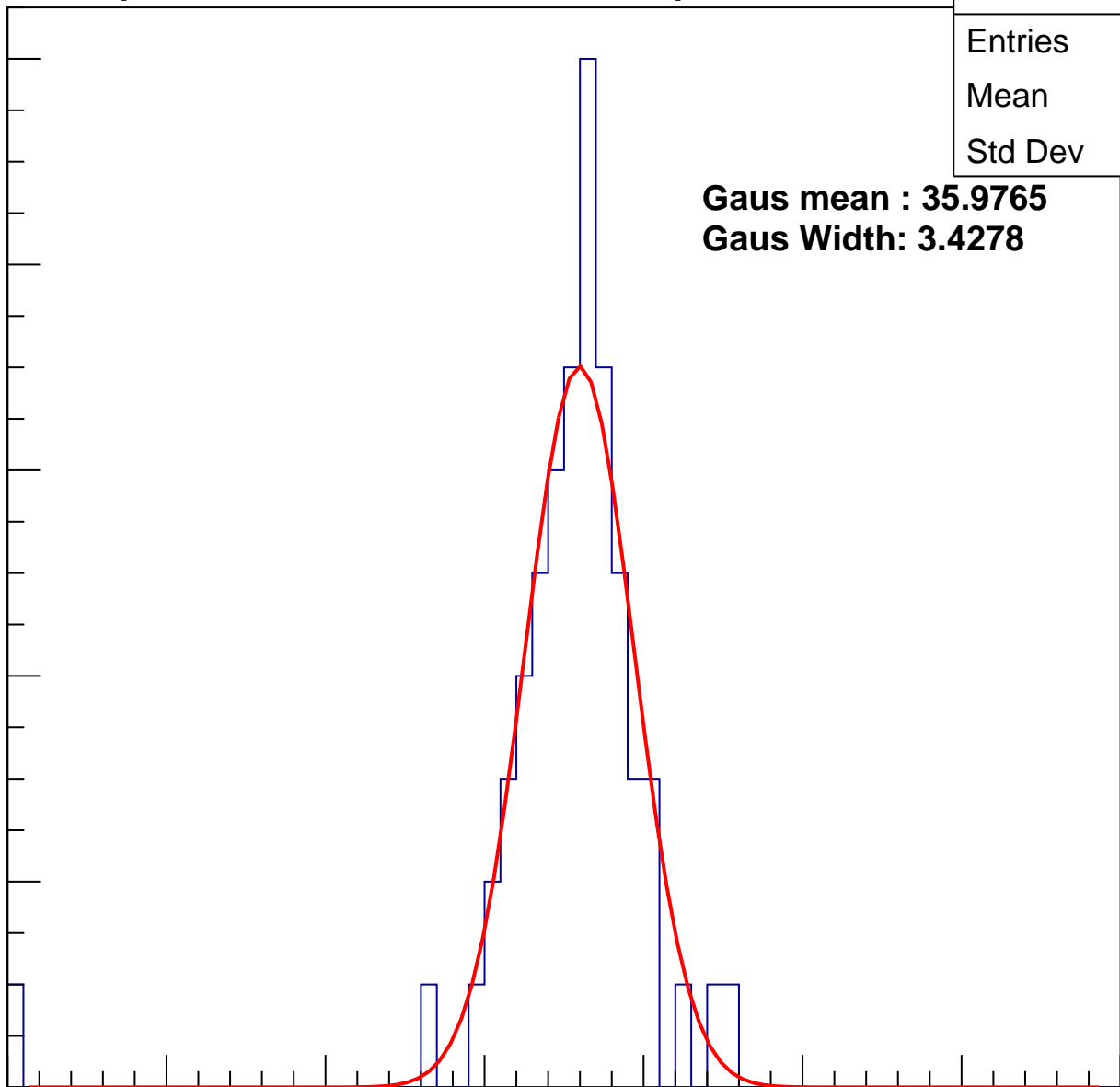
**Gaus Width: 3.4278**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U26-ch9, adc2

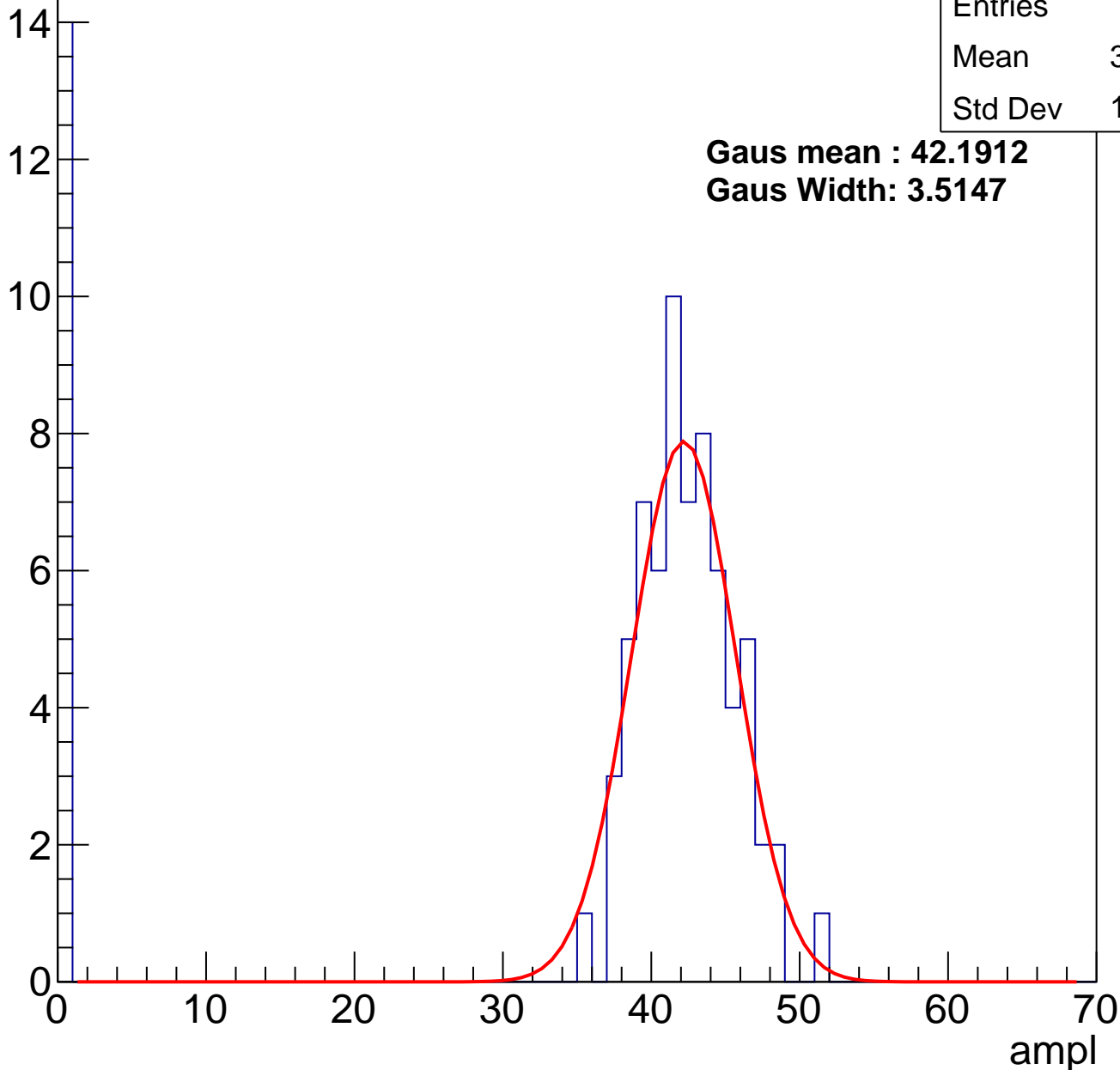
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	81
Mean	34.72
Std Dev	16.12

**Gaus mean : 42.1912**

**Gaus Width: 3.5147**

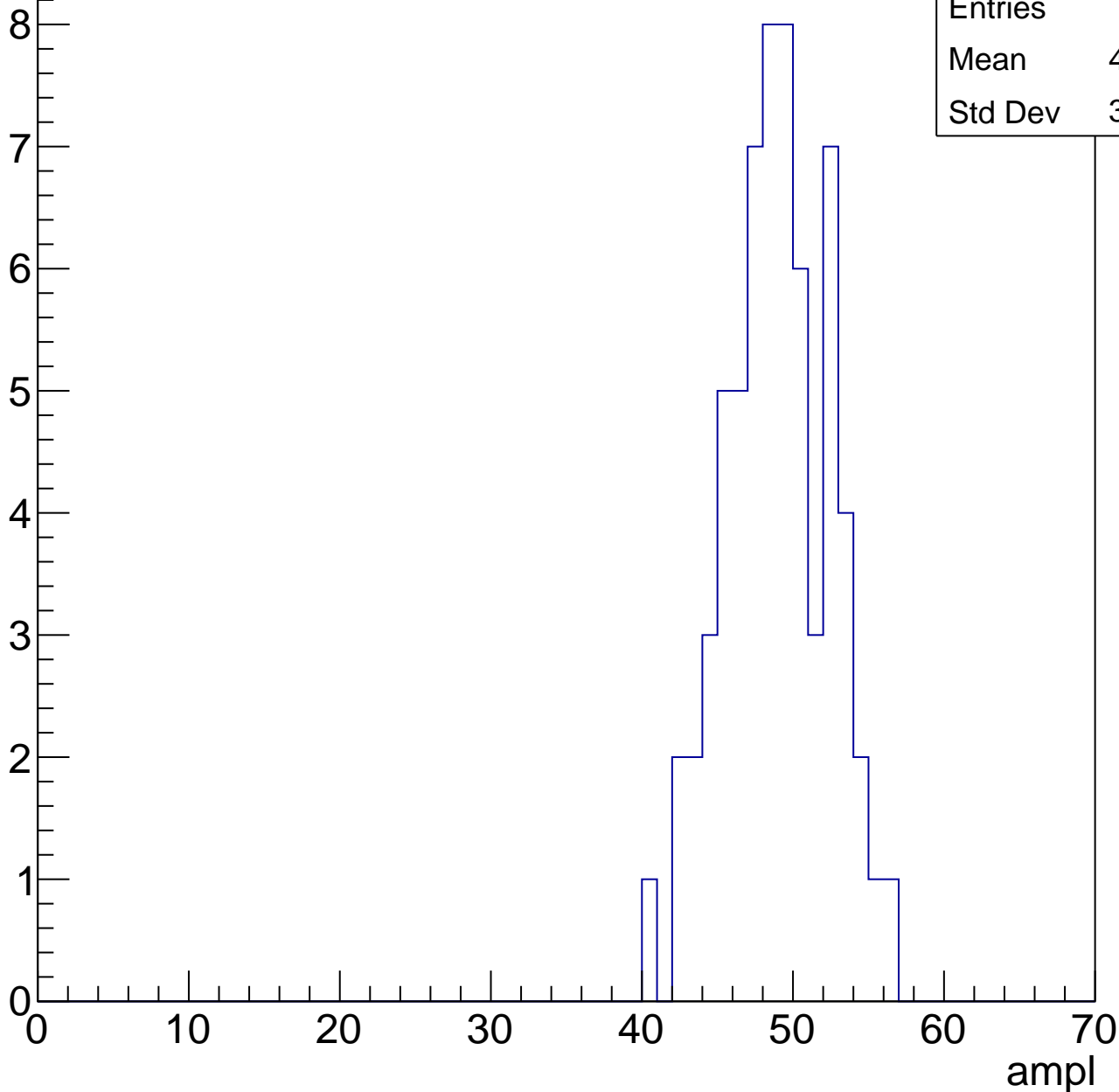


# B1L103S, U26-ch9, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	65
Mean	48.46
Std Dev	3.393

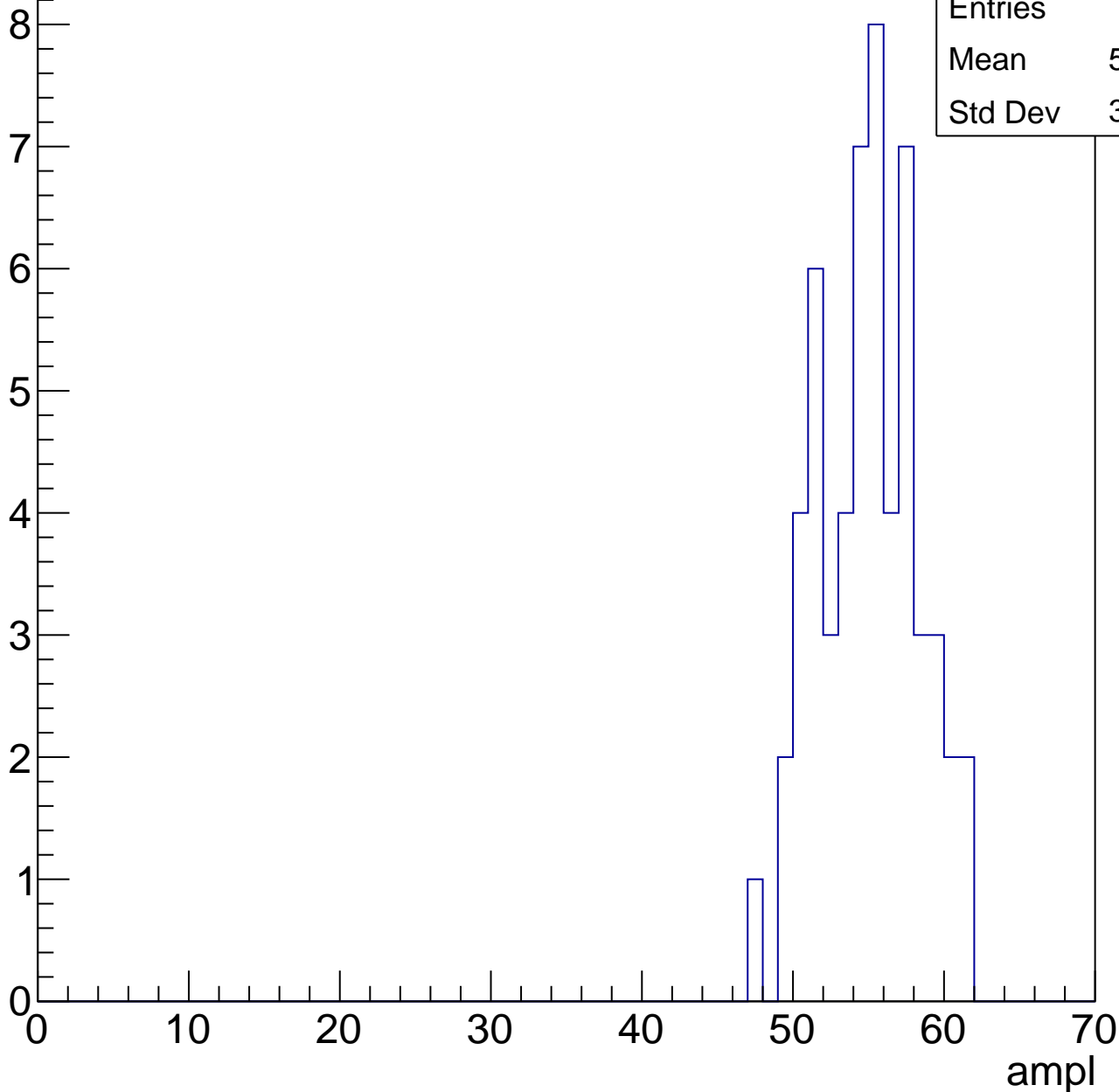


# B1L103S, U26-ch9, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	56
Mean	54.52
Std Dev	3.268



# B1L103S, U26-ch9, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

7

6

5

4

3

2

1

0

Entries	51
Mean	58.06
Std Dev	8.61

ampl

0

10

20

30

40

50

60

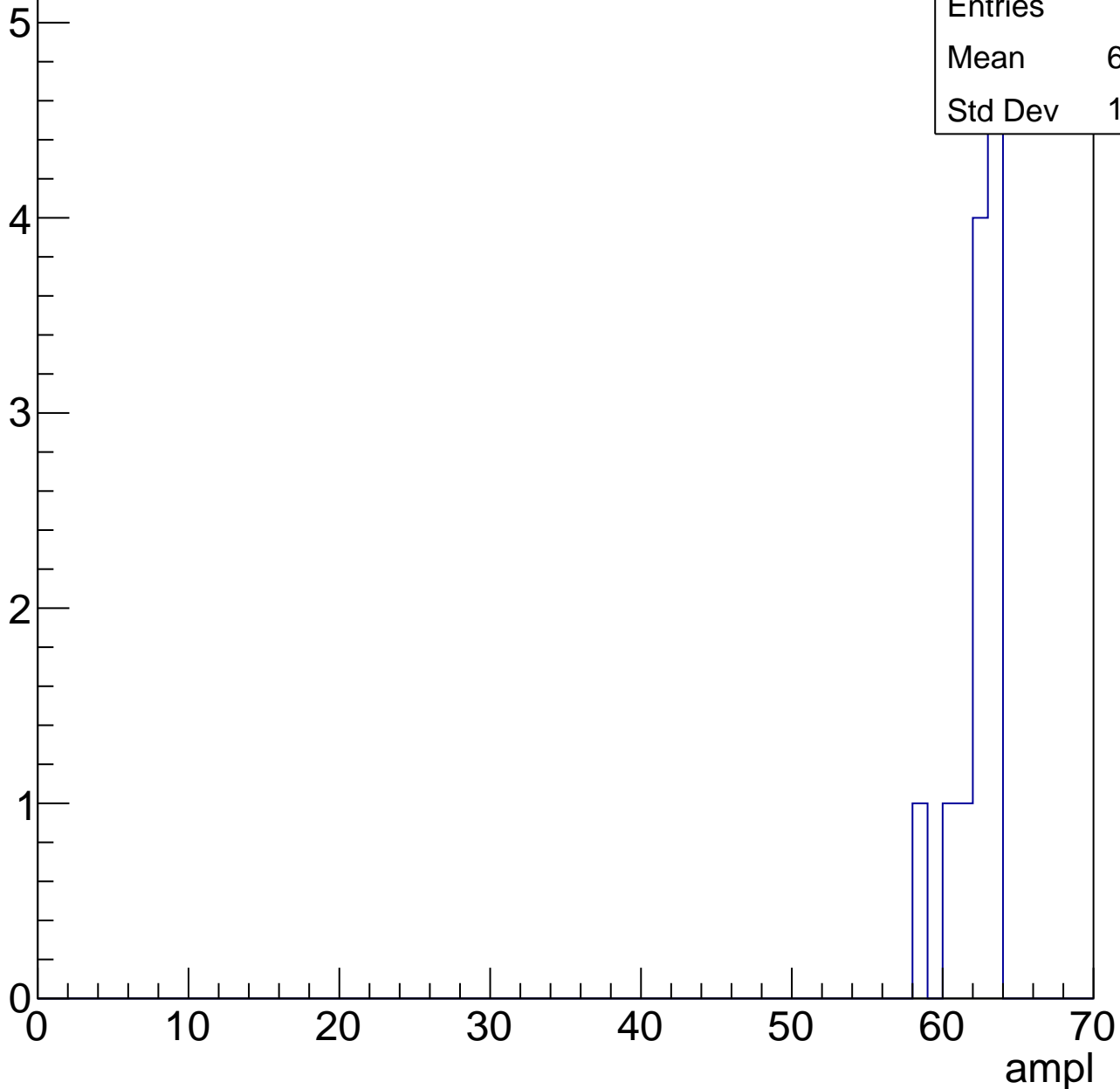
70

# B1L103S, U26-ch9, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	12
Mean	61.83
Std Dev	1.462





# B1L103S, U26-ch9, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



# B1L103S, U26-ch10, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	81
Mean	24.79
Std Dev	10.65

**Gaus mean : 28.8707**

**Gaus Width: 4.8471**

Entry

10

8

6

4

2

0

0

10

20

30

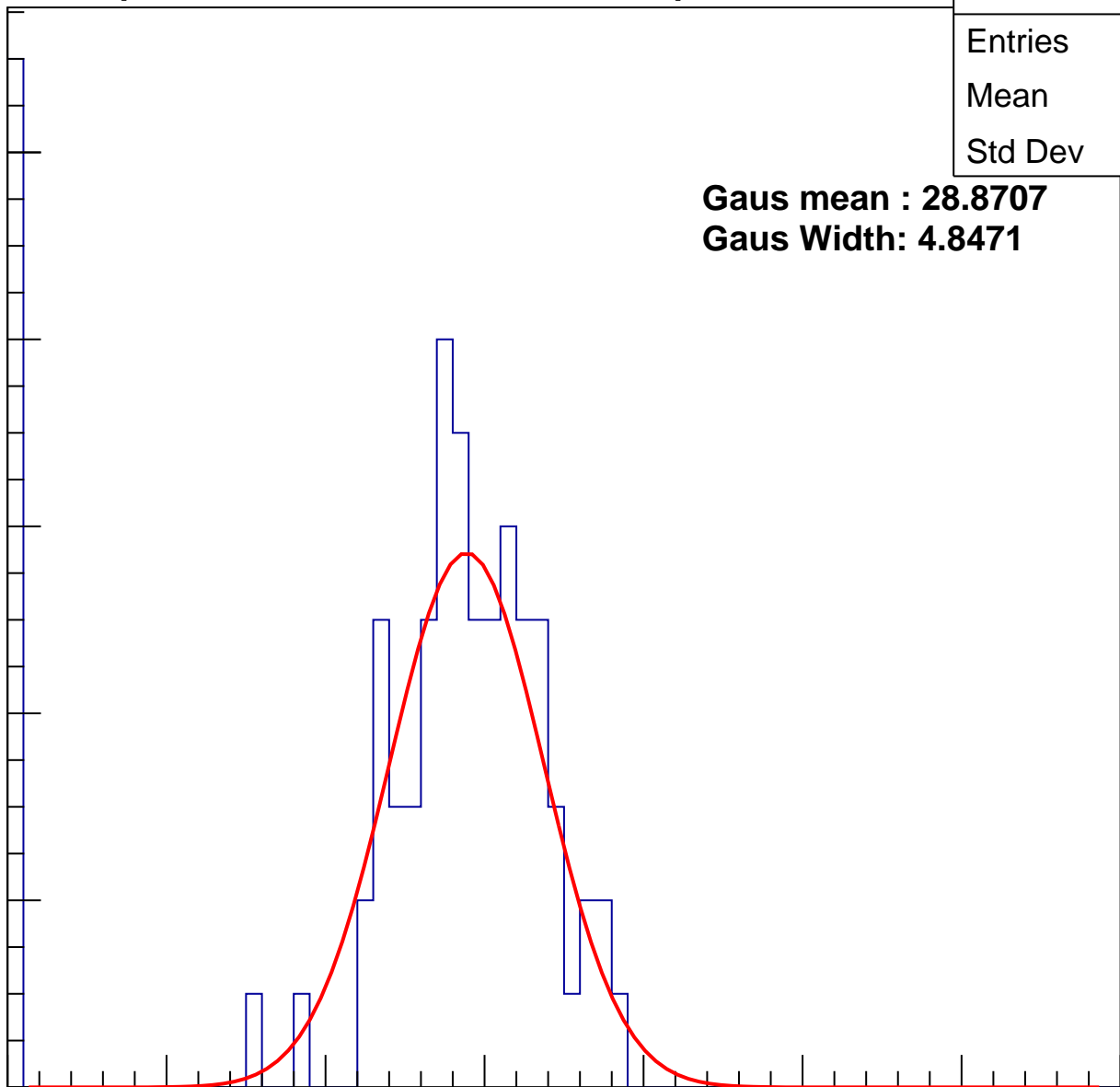
40

50

60

70

ampl



# B1L103S, U26-ch10, adc1

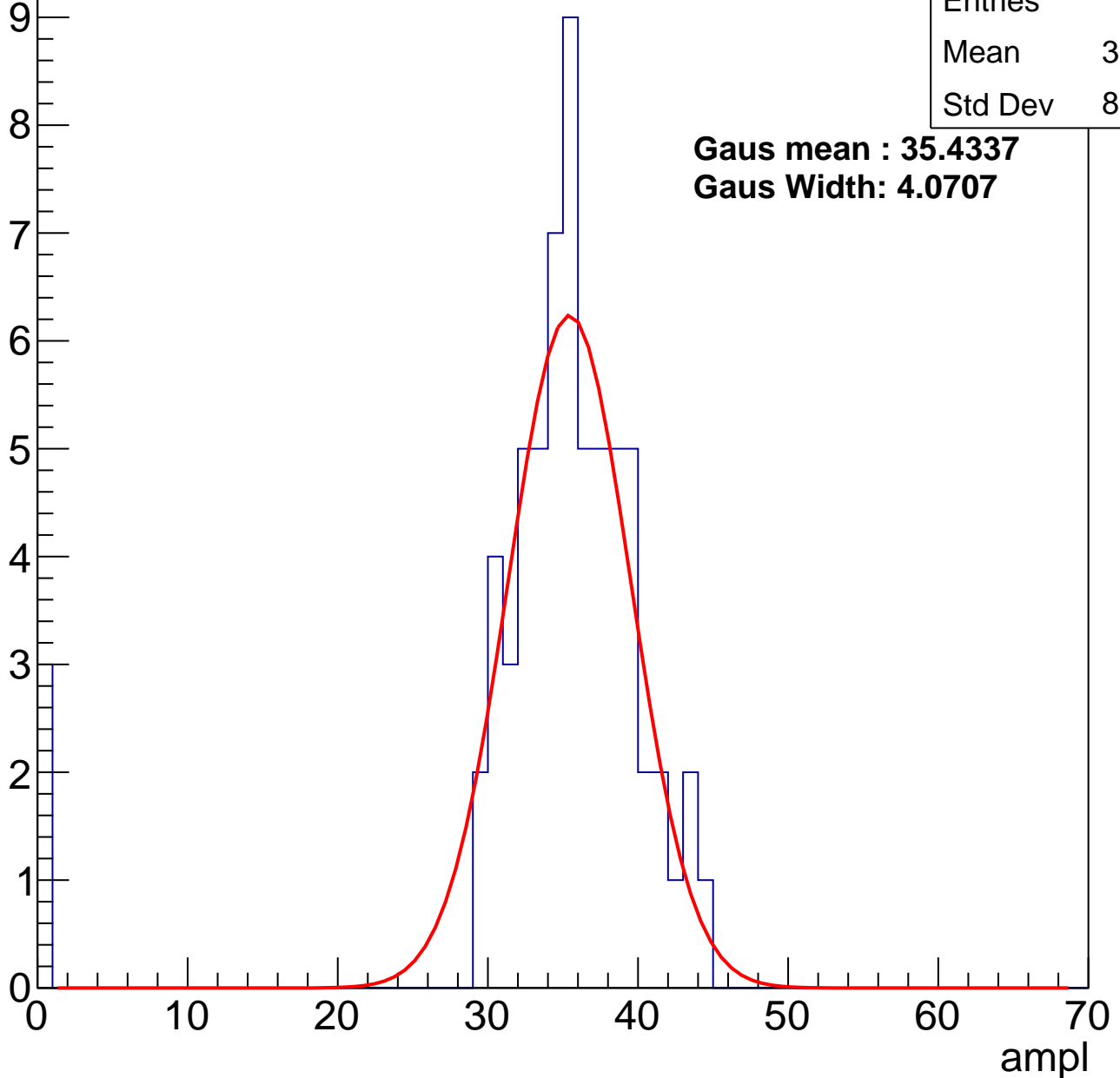
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	66
Mean	33.83
Std Dev	8.172

**Gaus mean : 35.4337**

**Gaus Width: 4.0707**



# B1L103S, U26-ch10, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	76
Mean	34.92
Std Dev	16.18

**Gaus mean : 41.8024**

**Gaus Width: 3.9647**

Entry

12

10

8

6

4

2

0

0

10

20

30

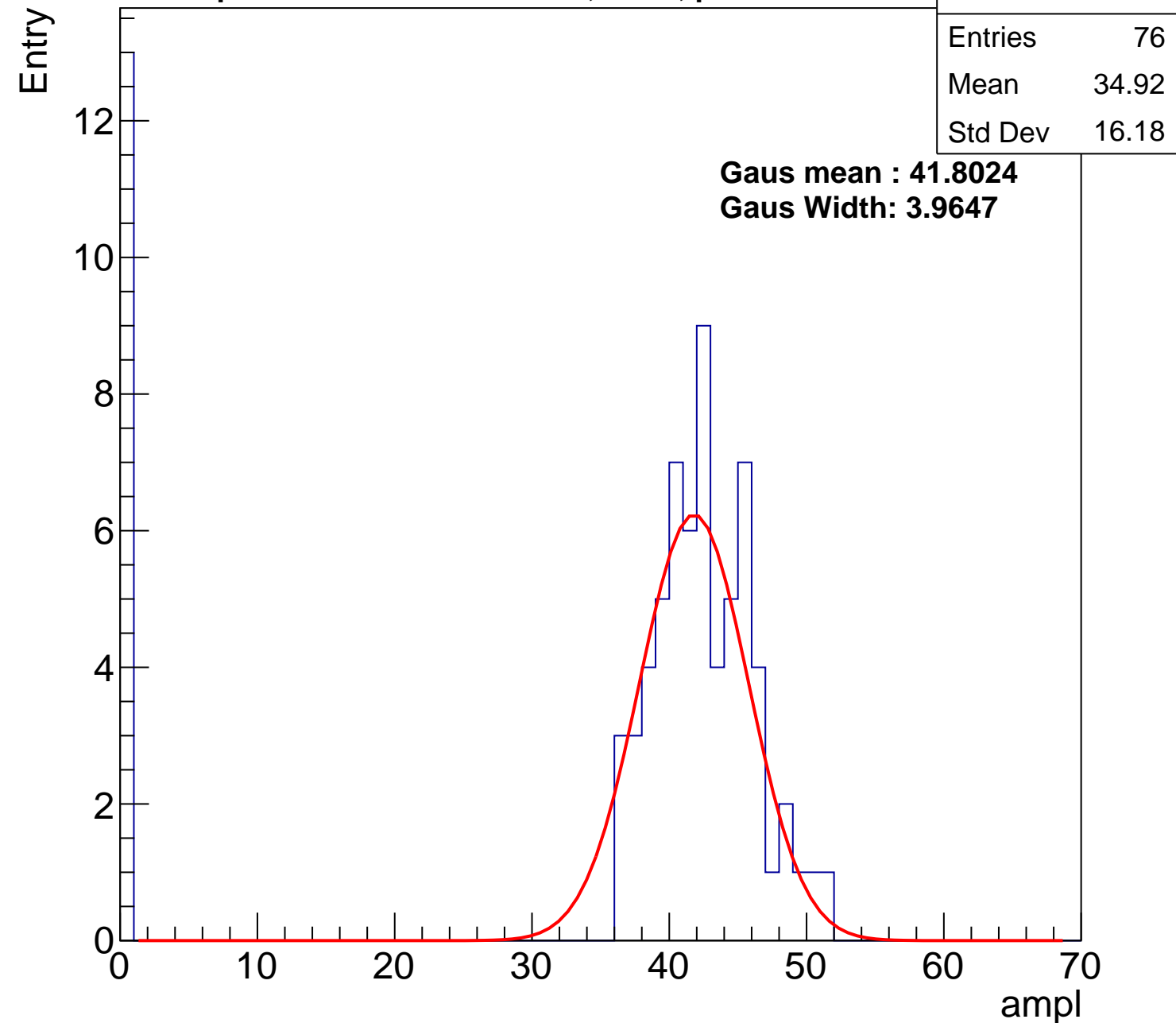
40

50

60

70

ampl

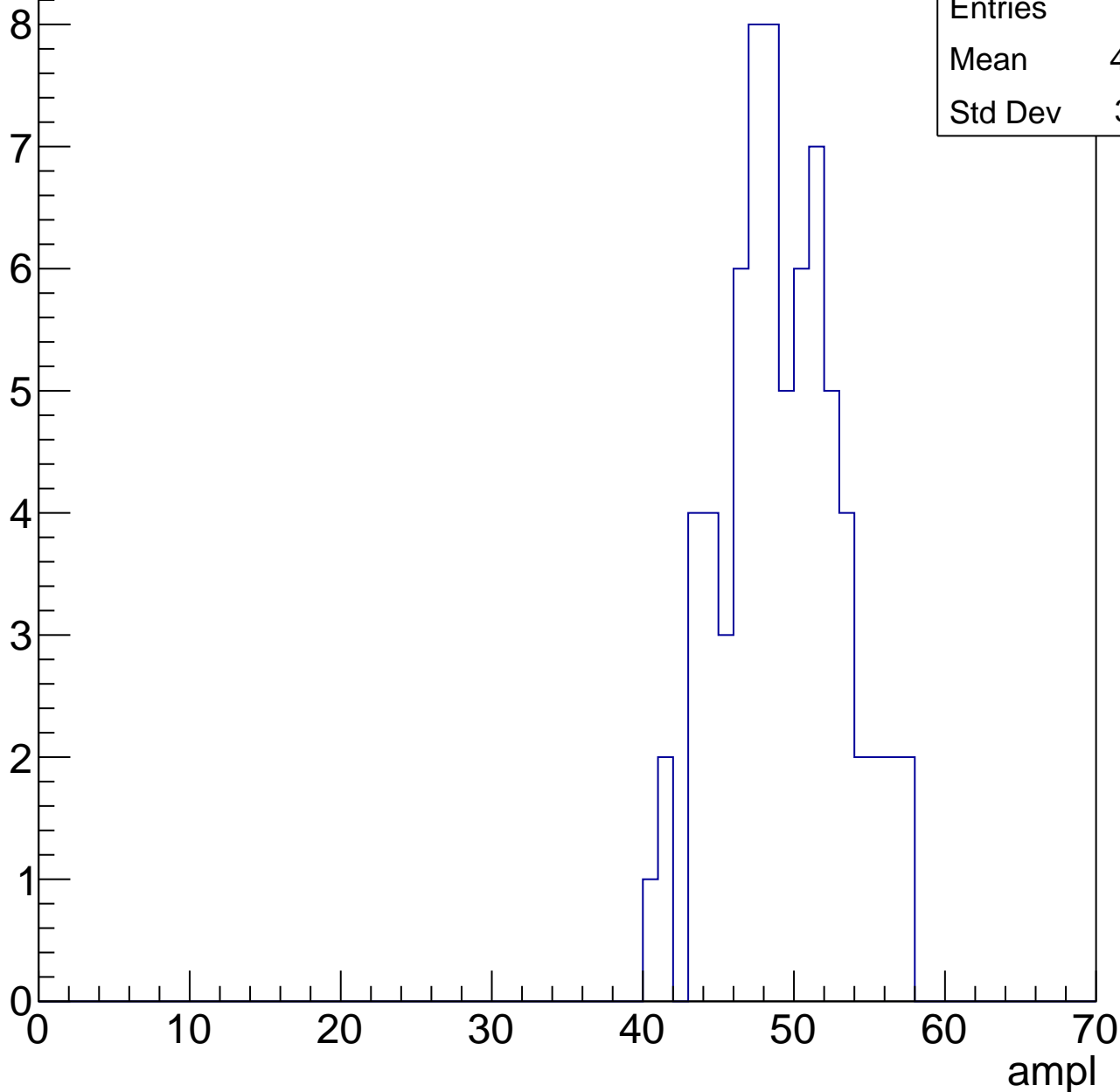


# B1L103S, U26-ch10, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	71
Mean	48.72
Std Dev	3.901

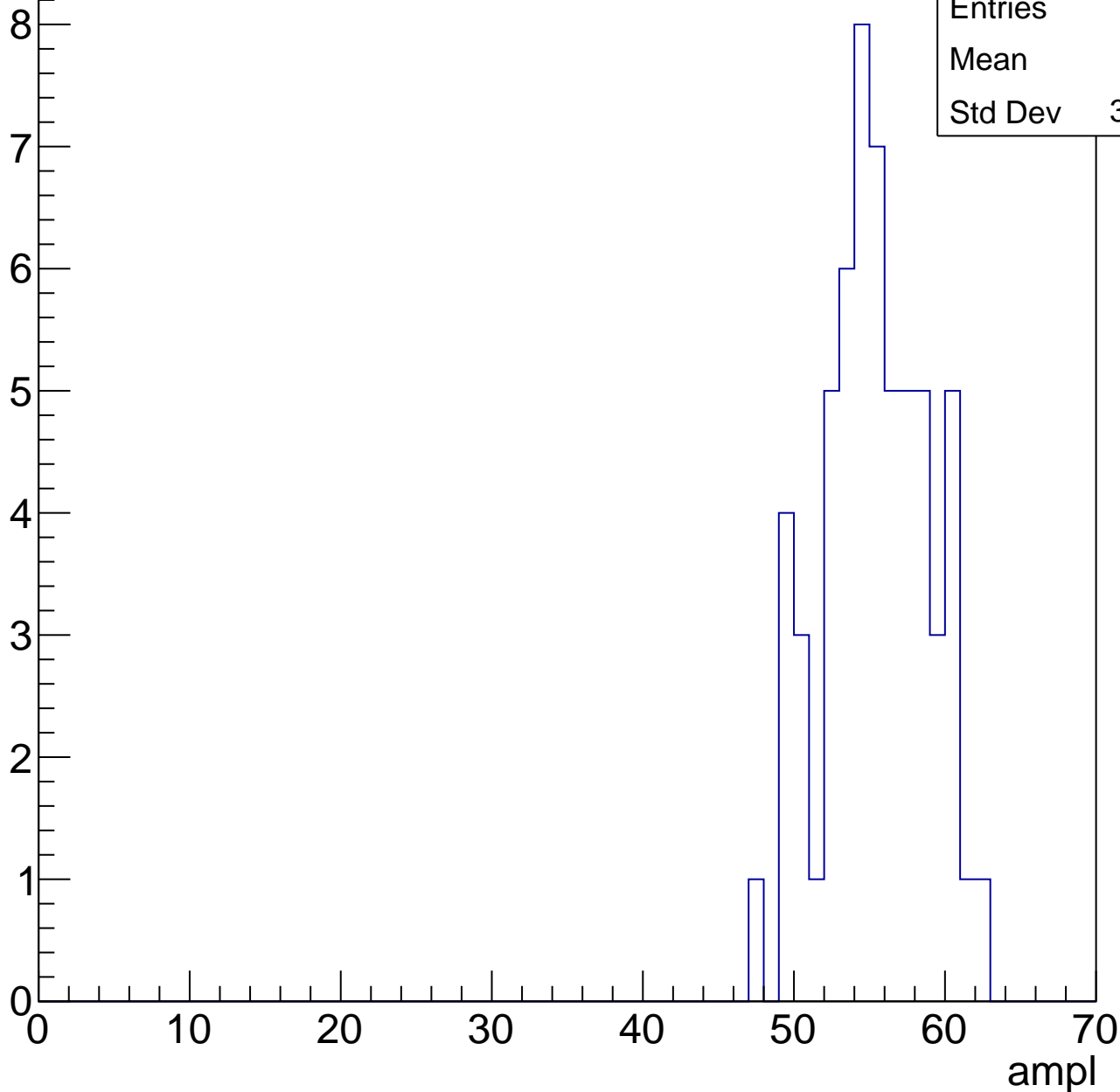


# B1L103S, U26-ch10, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	60
Mean	54.9
Std Dev	3.424

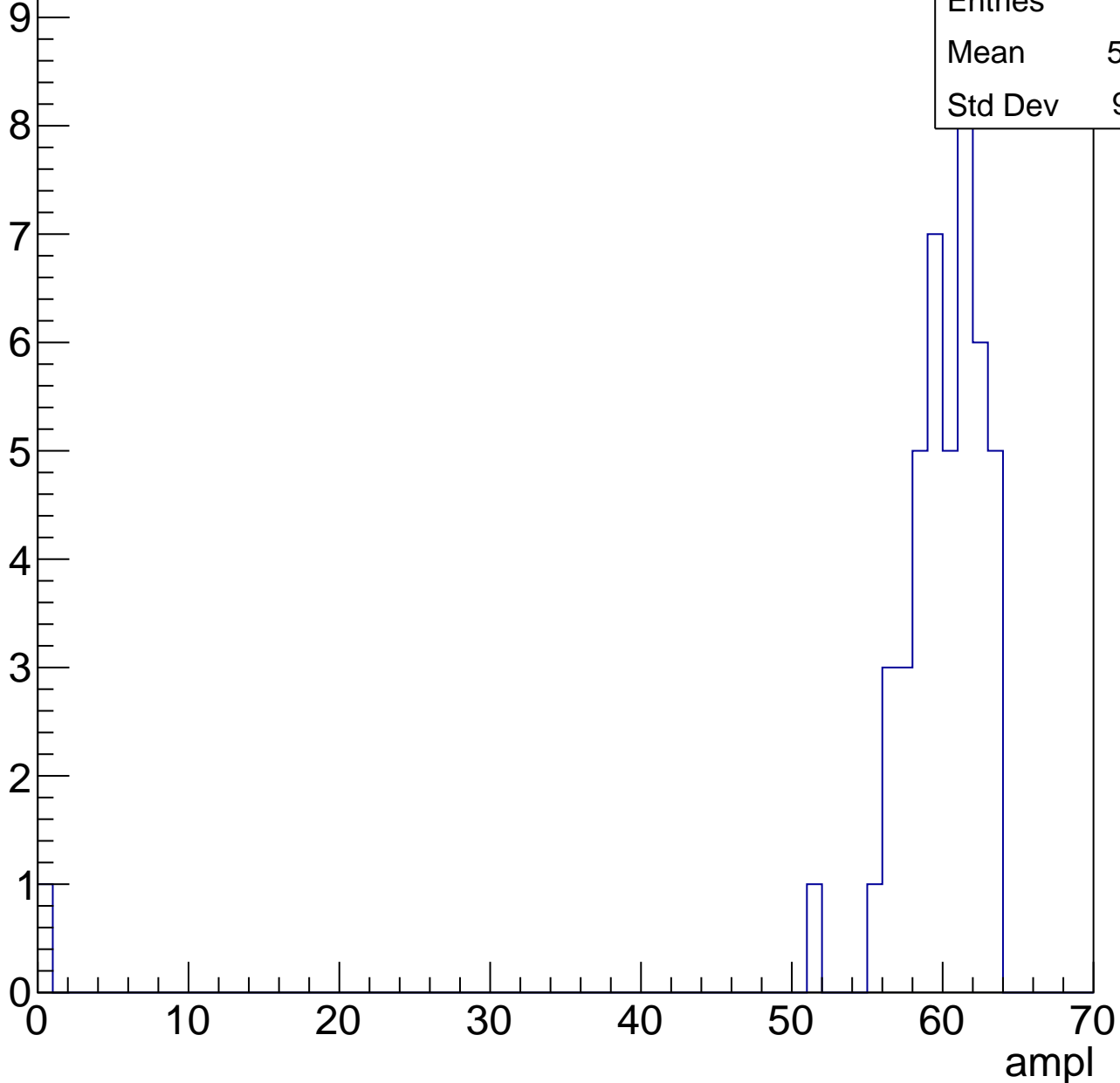


# B1L103S, U26-ch10, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	46
Mean	58.35
Std Dev	9.041



# B1L103S, U26-ch10, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry





# B1L103S, U26-ch10, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	19
Mean	3.316
Std Dev	14.07

Entry



# B1L103S, U26-ch11, adc0

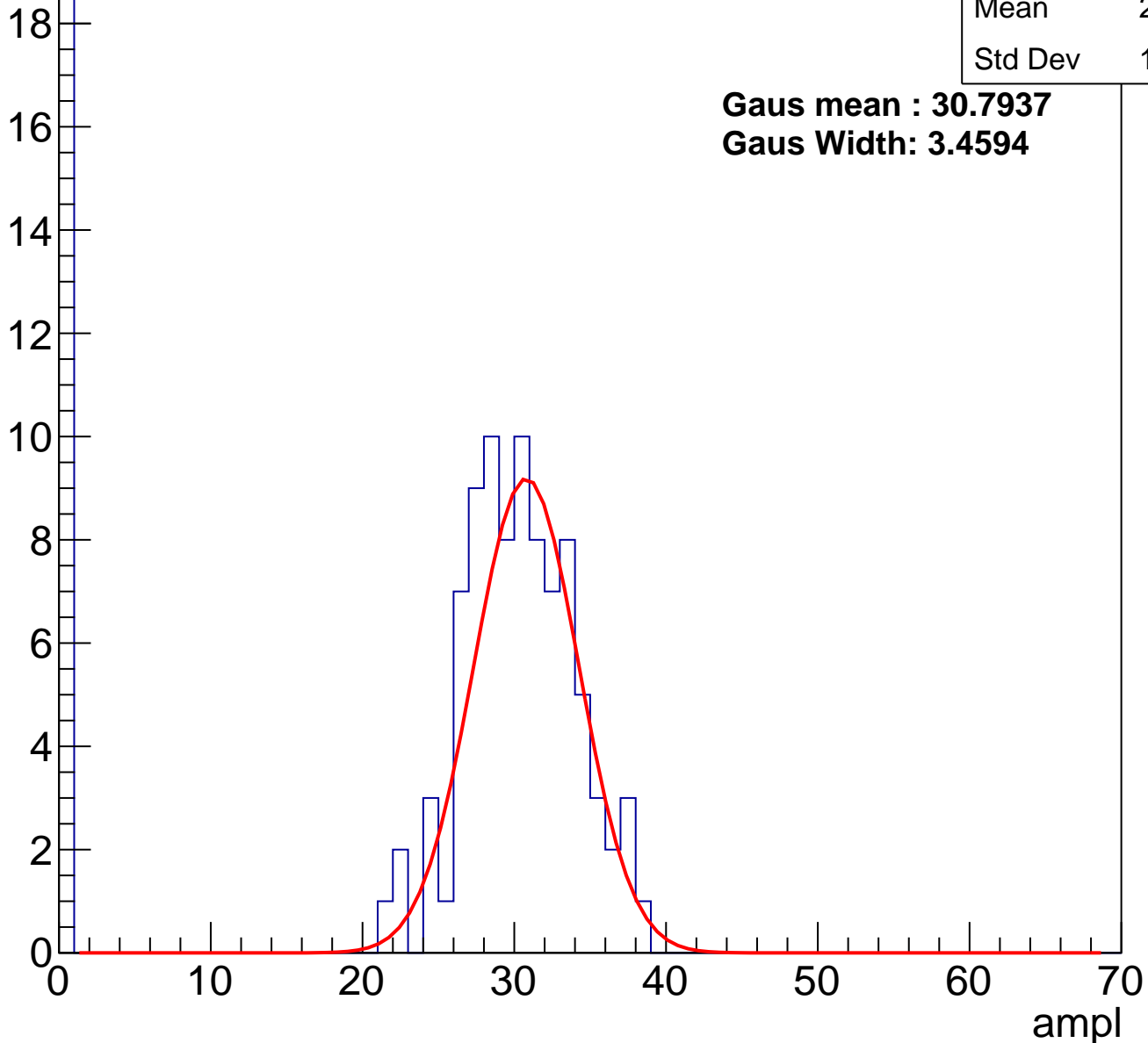
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	107
Mean	24.59
Std Dev	11.88

**Gaus mean : 30.7937**

**Gaus Width: 3.4594**

Entry



# B1L103S, U26-ch11, adc1

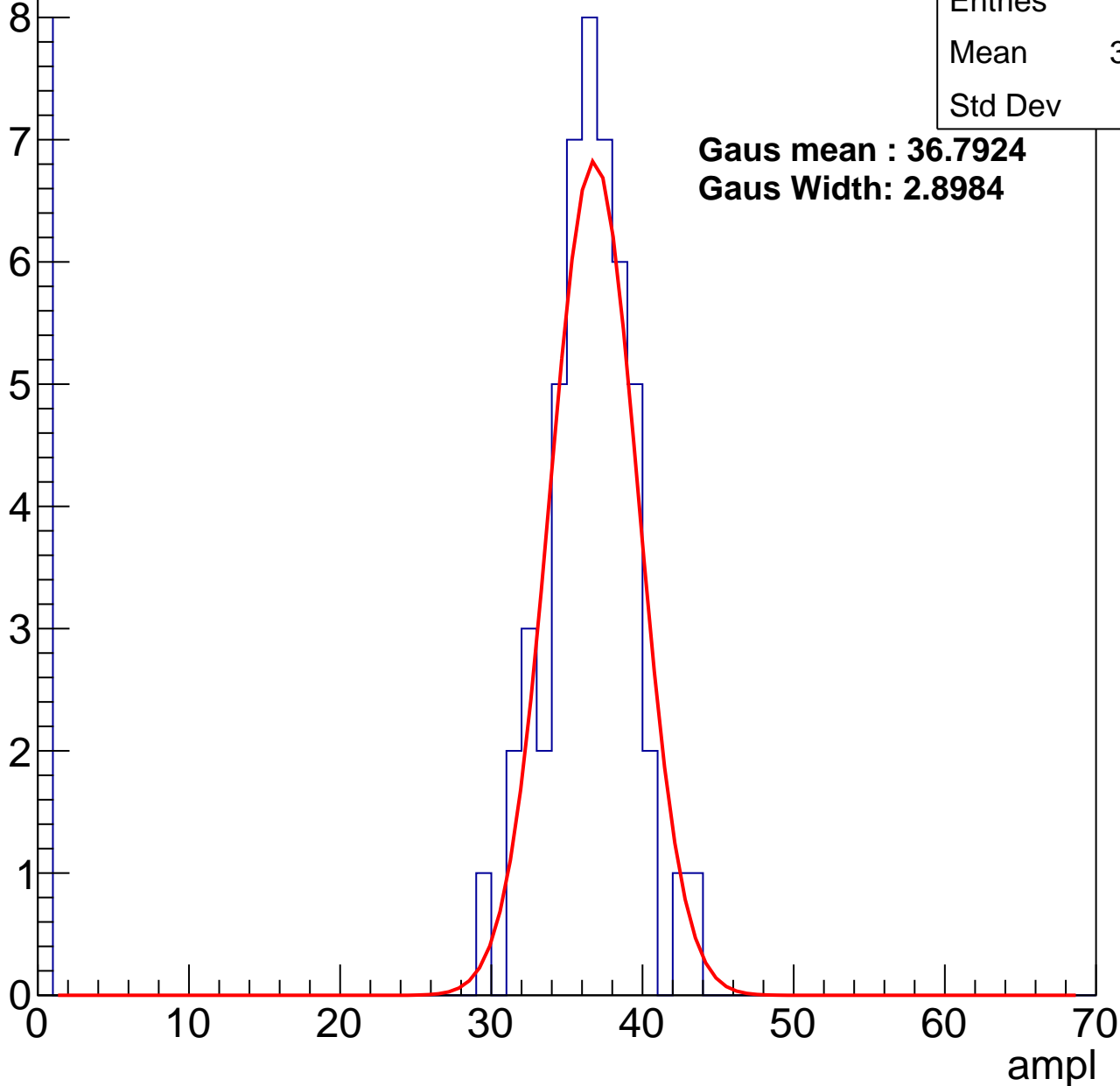
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	58
Mean	31.09
Std Dev	12.7

**Gaus mean : 36.7924**

**Gaus Width: 2.8984**



# B1L103S, U26-ch11, adc2

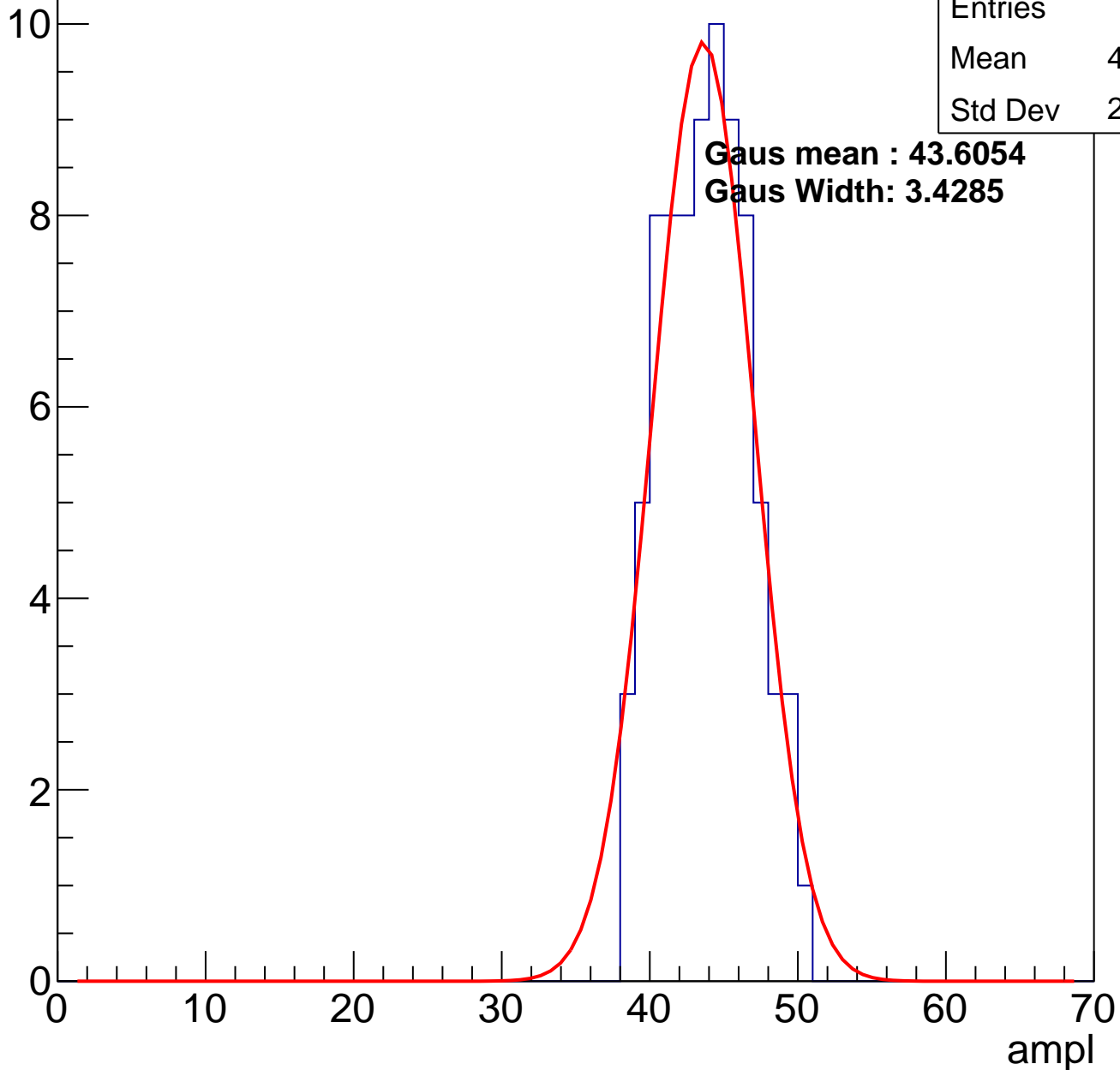
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	80
Mean	43.36
Std Dev	2.929

**Gaus mean : 43.6054**

**Gaus Width: 3.4285**

Entry

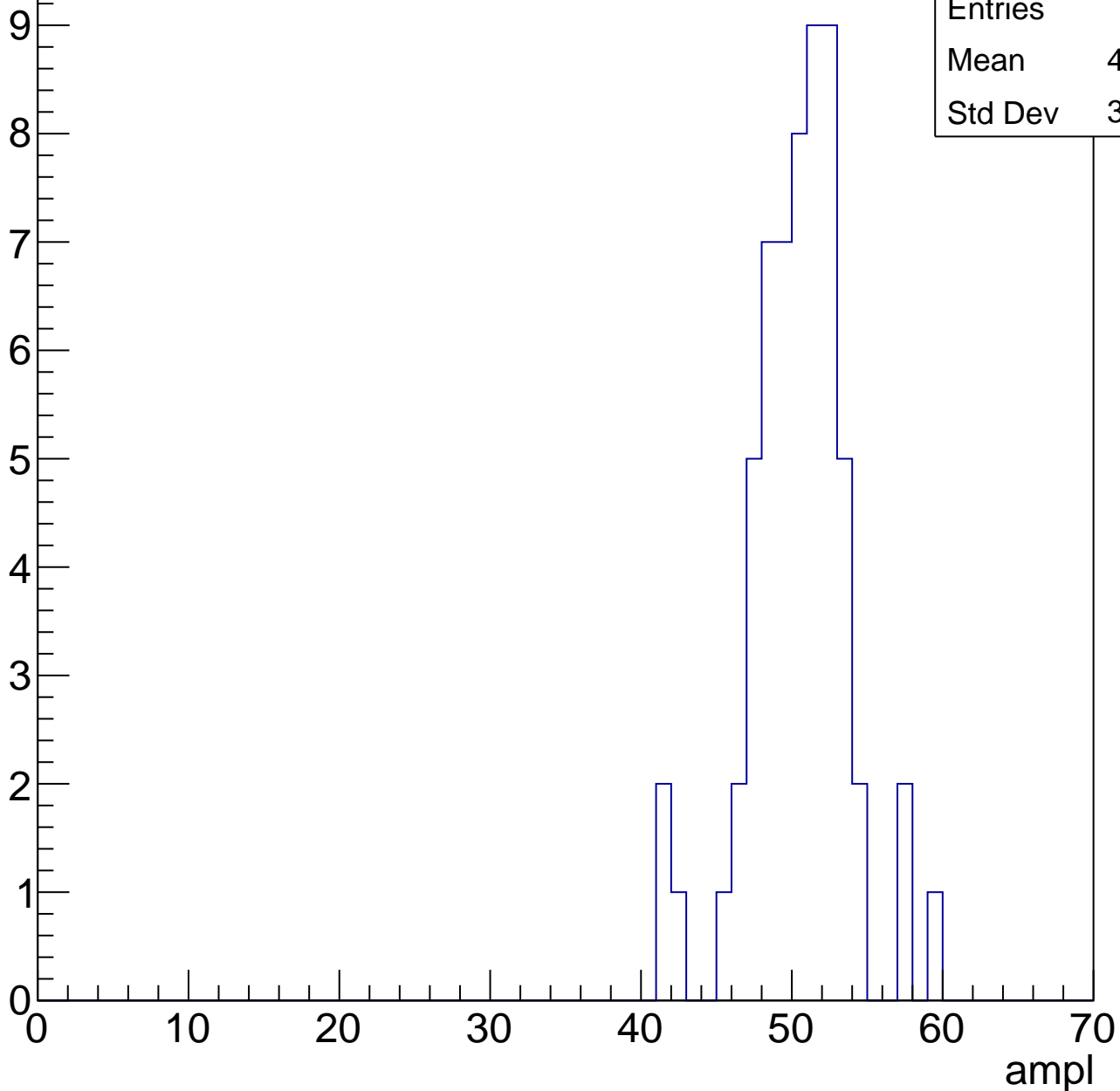


# B1L103S, U26-ch11, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	61
Mean	49.97
Std Dev	3.299

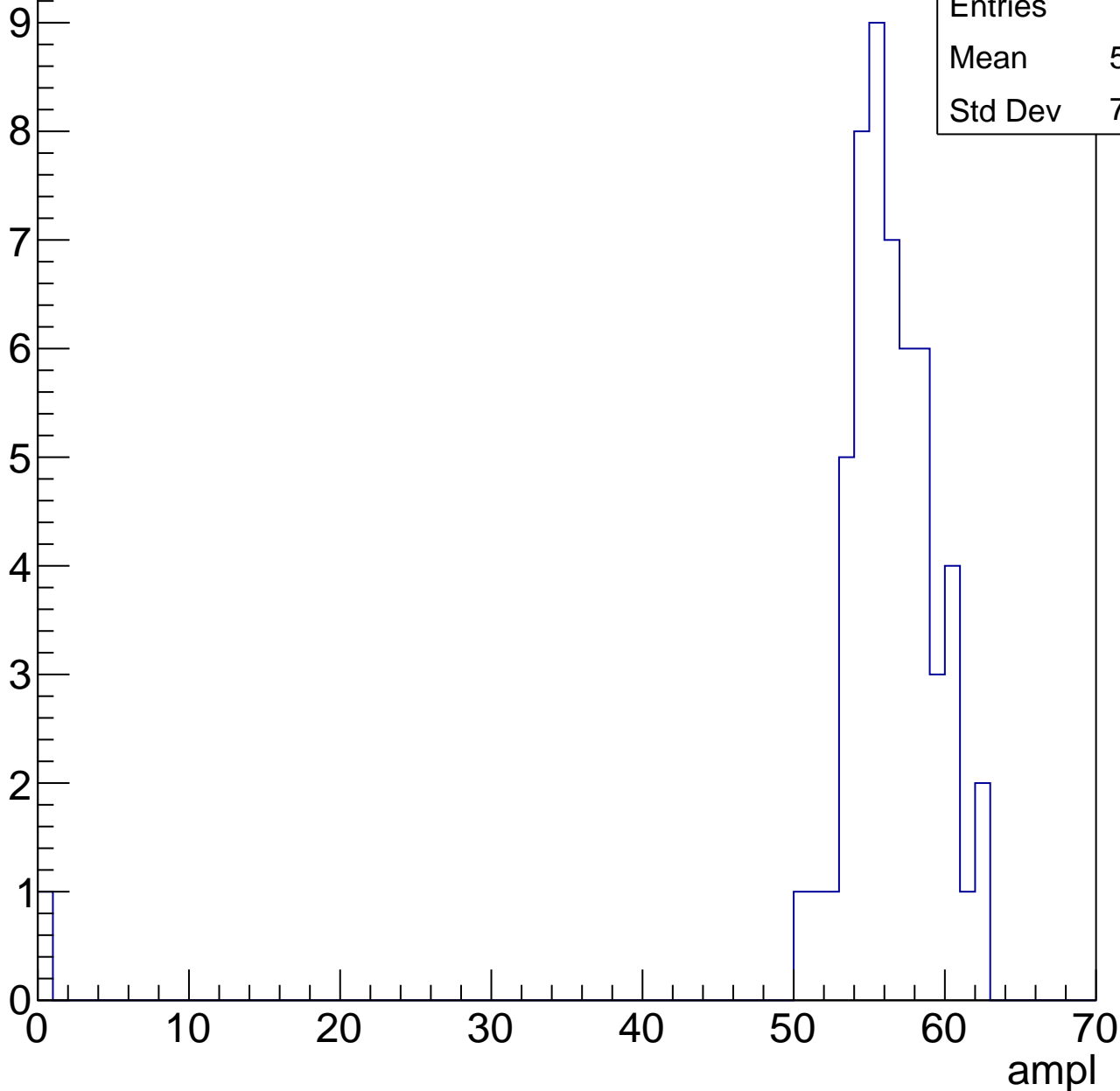


# B1L103S, U26-ch11, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	55
Mean	55.07
Std Dev	7.943

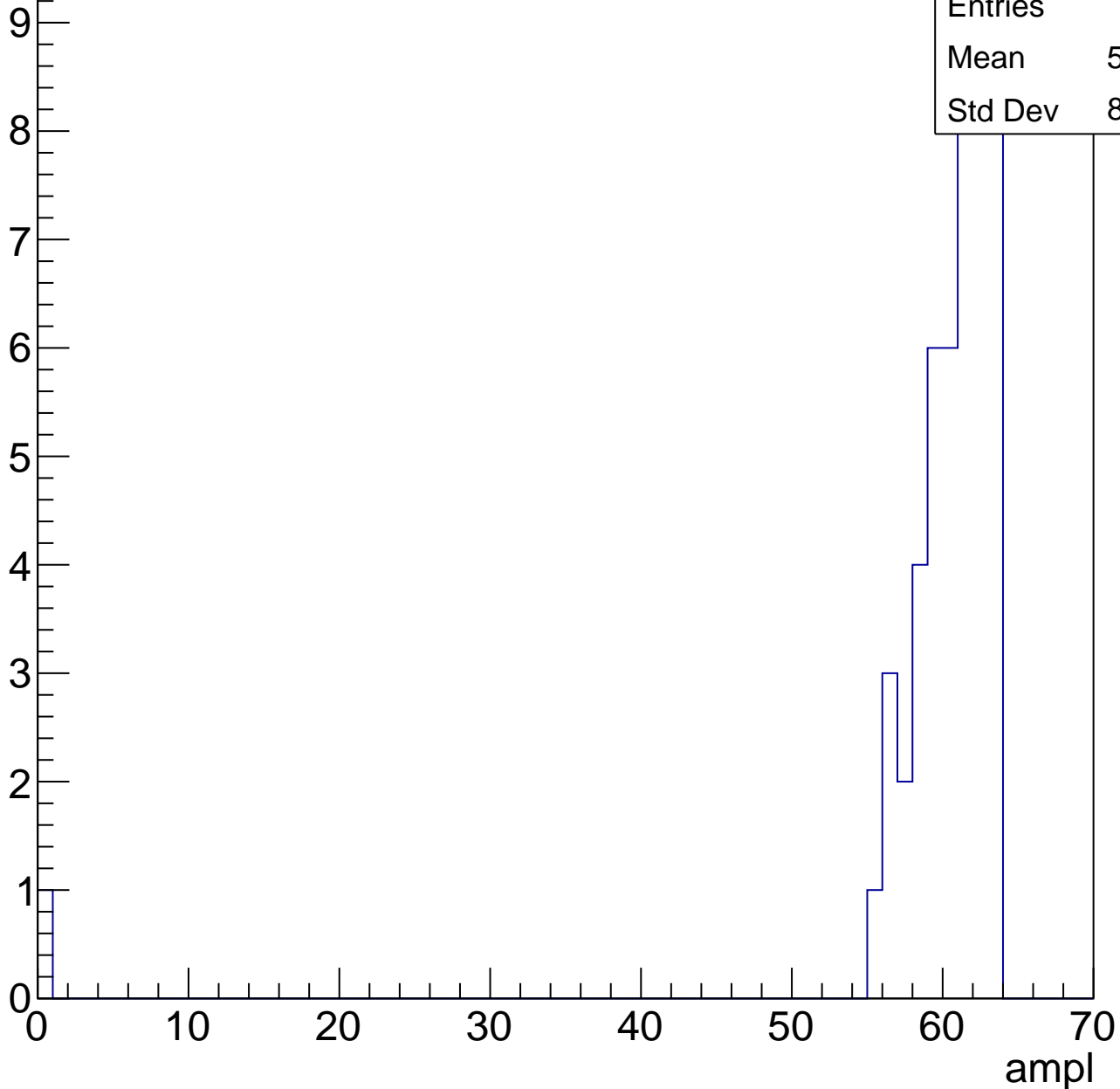


# B1L103S, U26-ch11, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	49
Mean	59.08
Std Dev	8.799



# B1L103S, U26-ch11, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry





# B1L103S, U26-ch11, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

18  
16  
14  
12  
10  
8  
6  
4  
2  
0

Entries	19
Mean	0
Std Dev	0

ampl

# B1L103S, U26-ch12, adc0

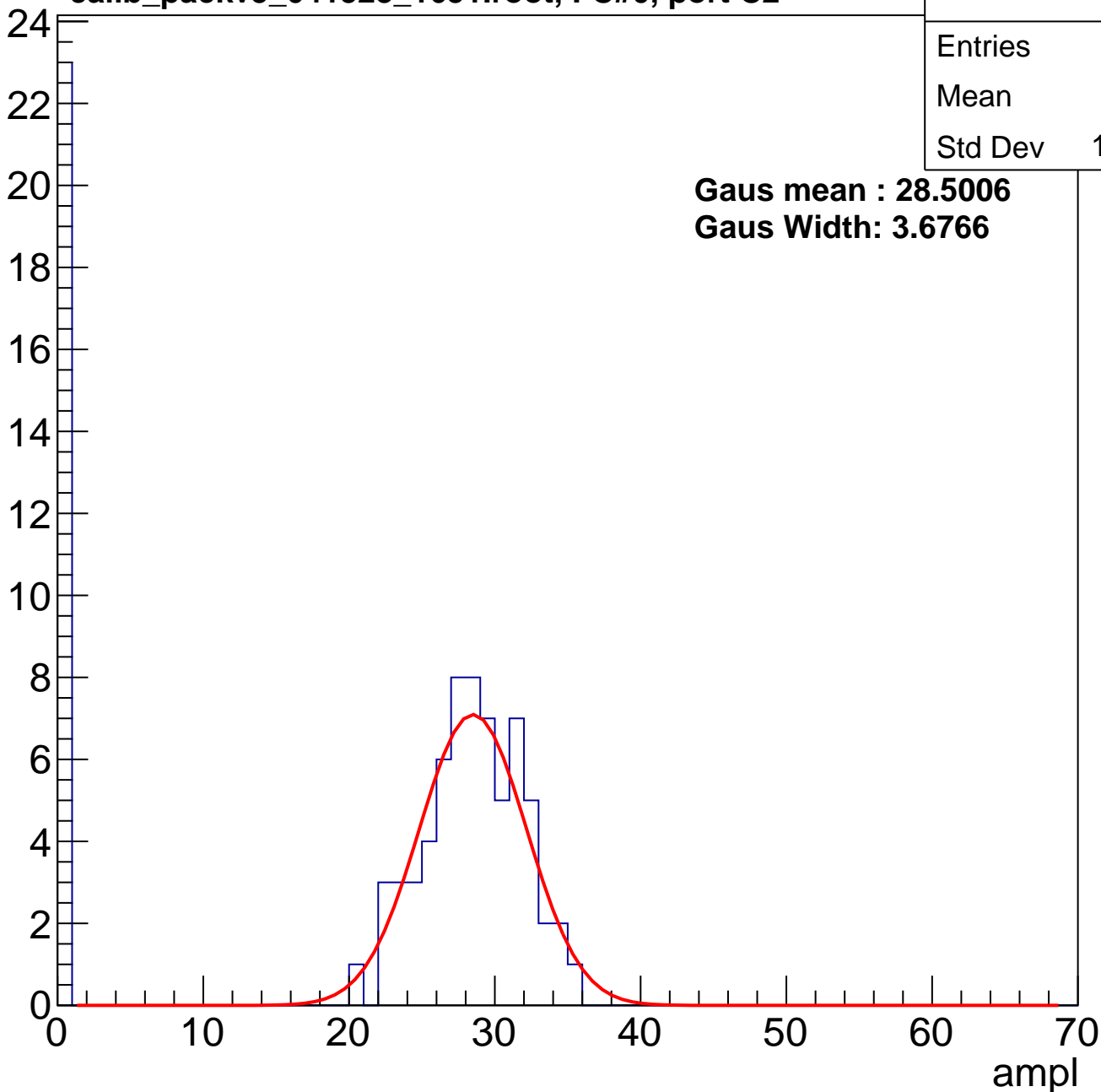
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	88
Mean	20.7
Std Dev	12.64

**Gaus mean : 28.5006**

**Gaus Width: 3.6766**

Entry



# B1L103S, U26-ch12, adc1

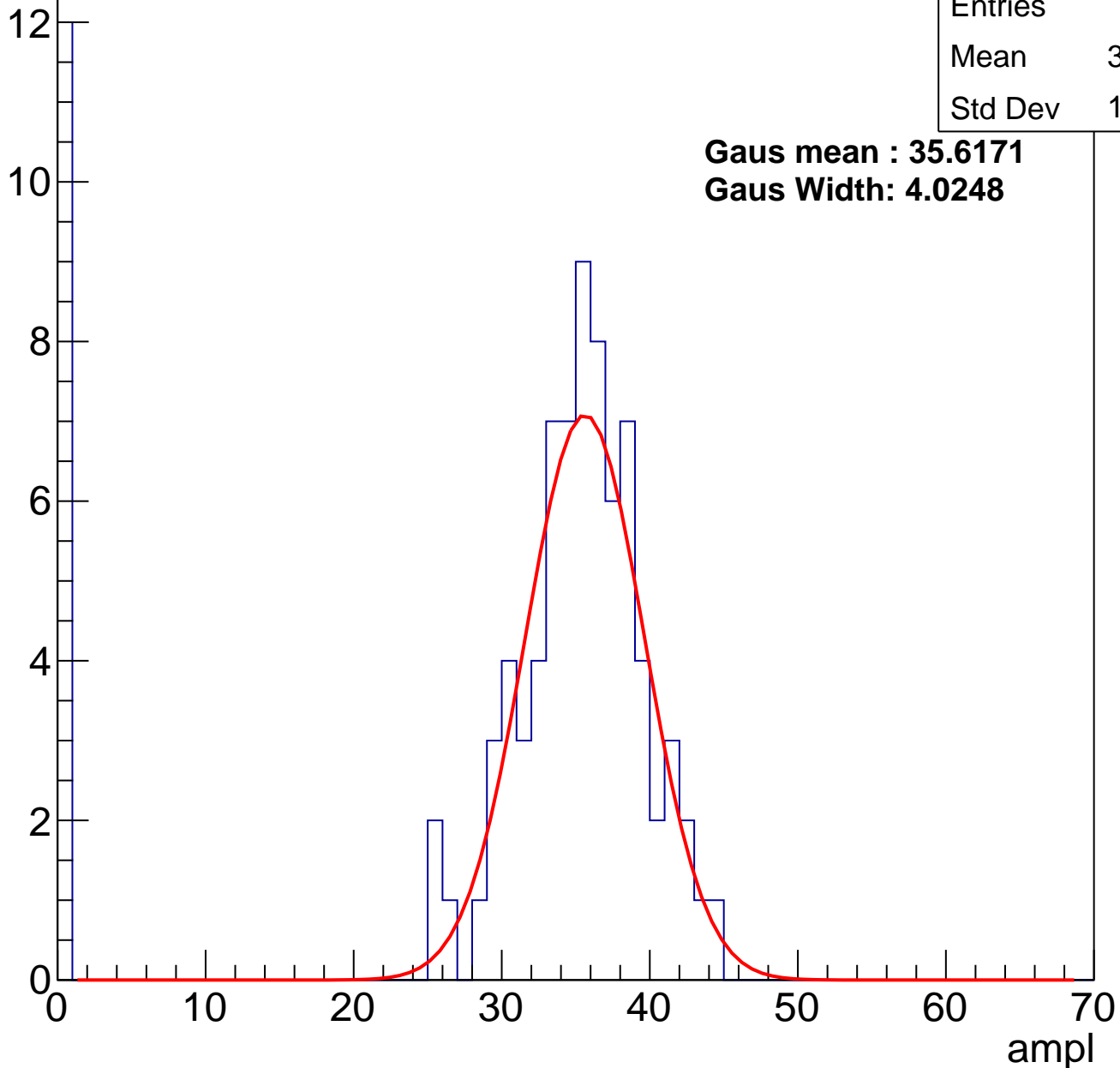
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	87
Mean	30.14
Std Dev	12.62

**Gaus mean : 35.6171**

**Gaus Width: 4.0248**

Entry



# B1L103S, U26-ch12, adc2

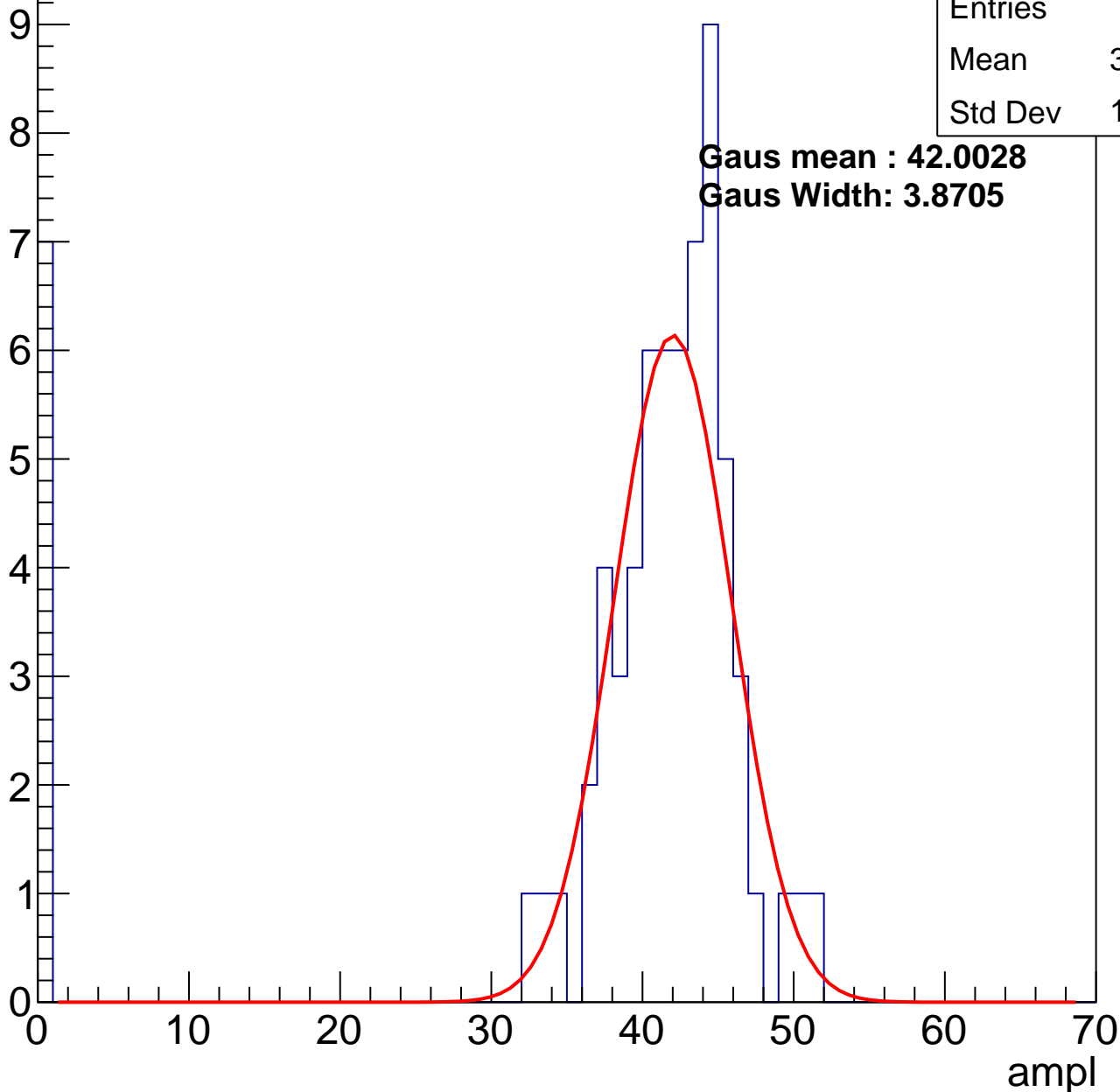
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	69
Mean	37.45
Std Dev	13.08

**Gaus mean : 42.0028**

**Gaus Width: 3.8705**

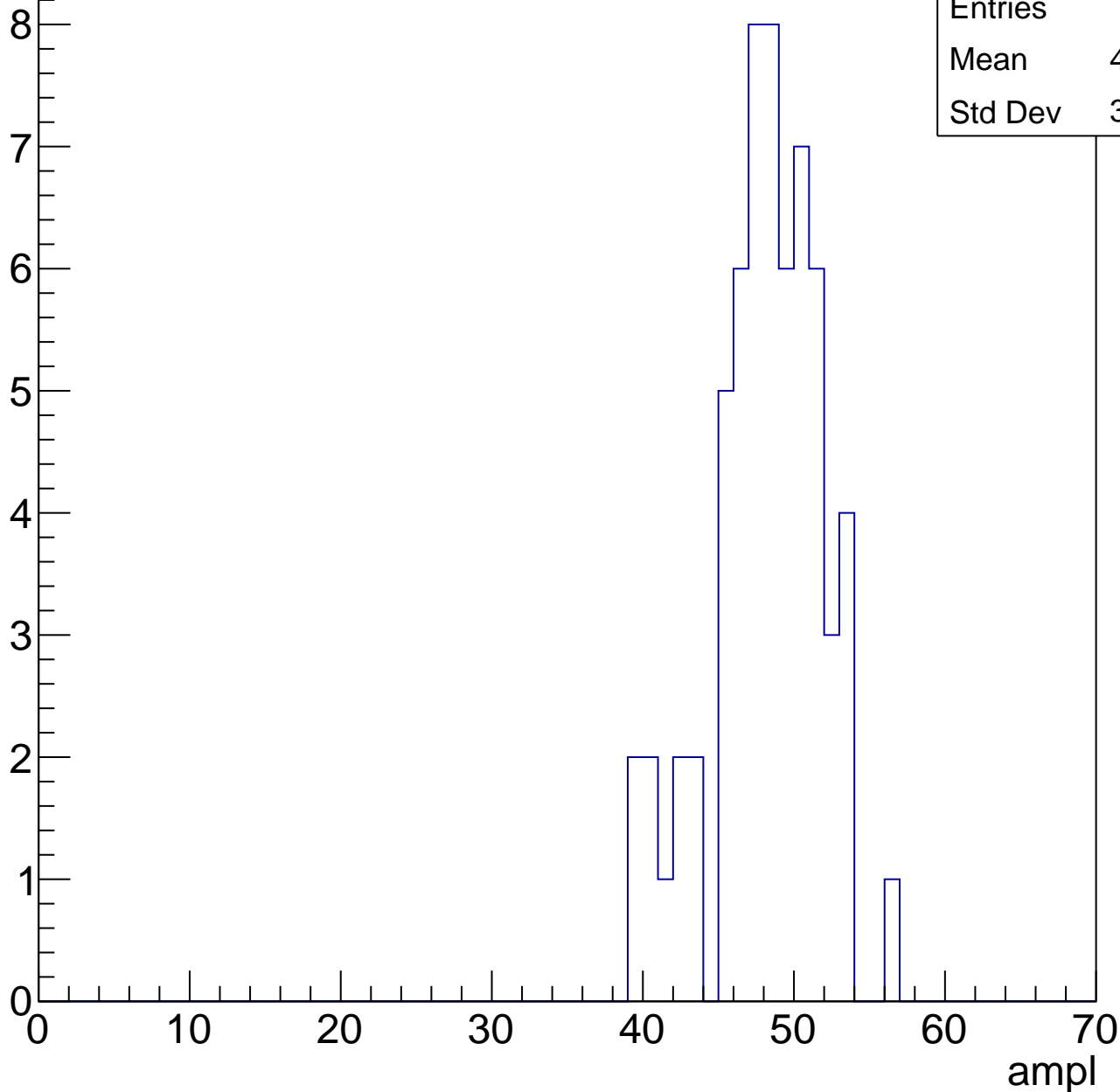


# B1L103S, U26-ch12, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	63
Mean	47.68
Std Dev	3.633

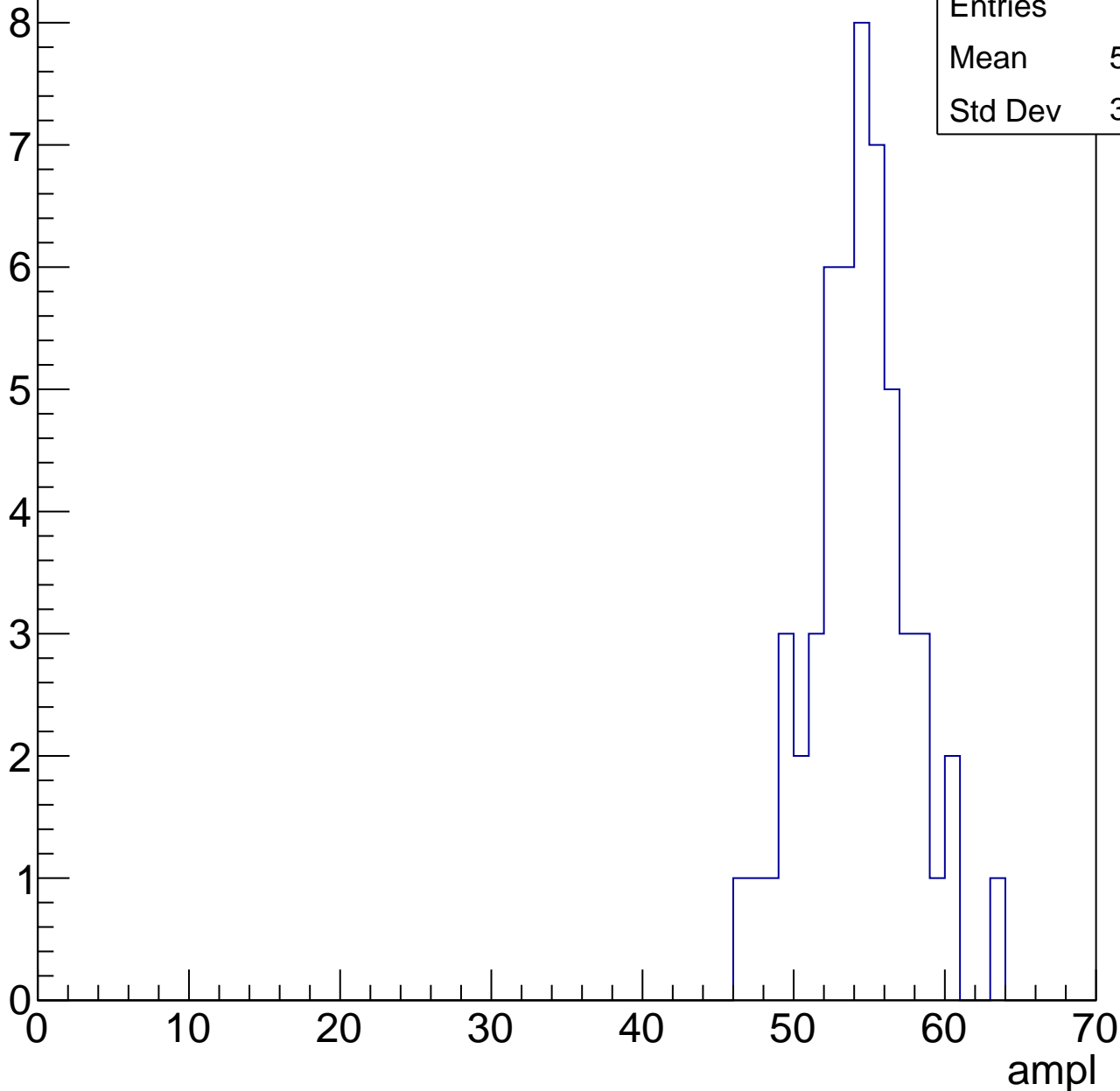


# B1L103S, U26-ch12, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	53
Mean	53.87
Std Dev	3.342

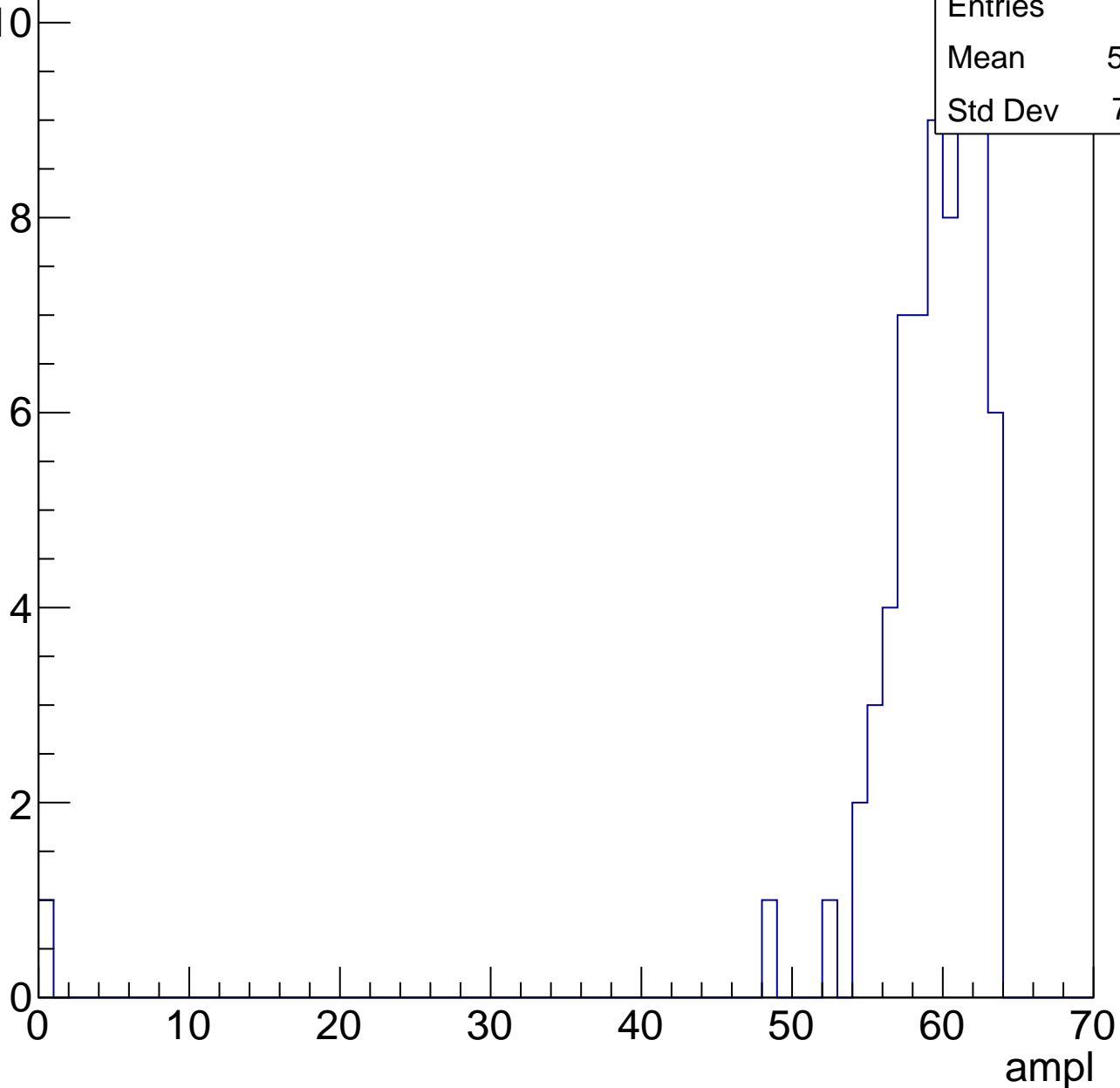


# B1L103S, U26-ch12, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	69
Mean	58.28
Std Dev	7.631



# B1L103S, U26-ch12, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry





# B1L103S, U26-ch12, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

18  
16  
14  
12  
10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

Entries	19
Mean	0
Std Dev	0

# B1L103S, U26-ch13, adc0

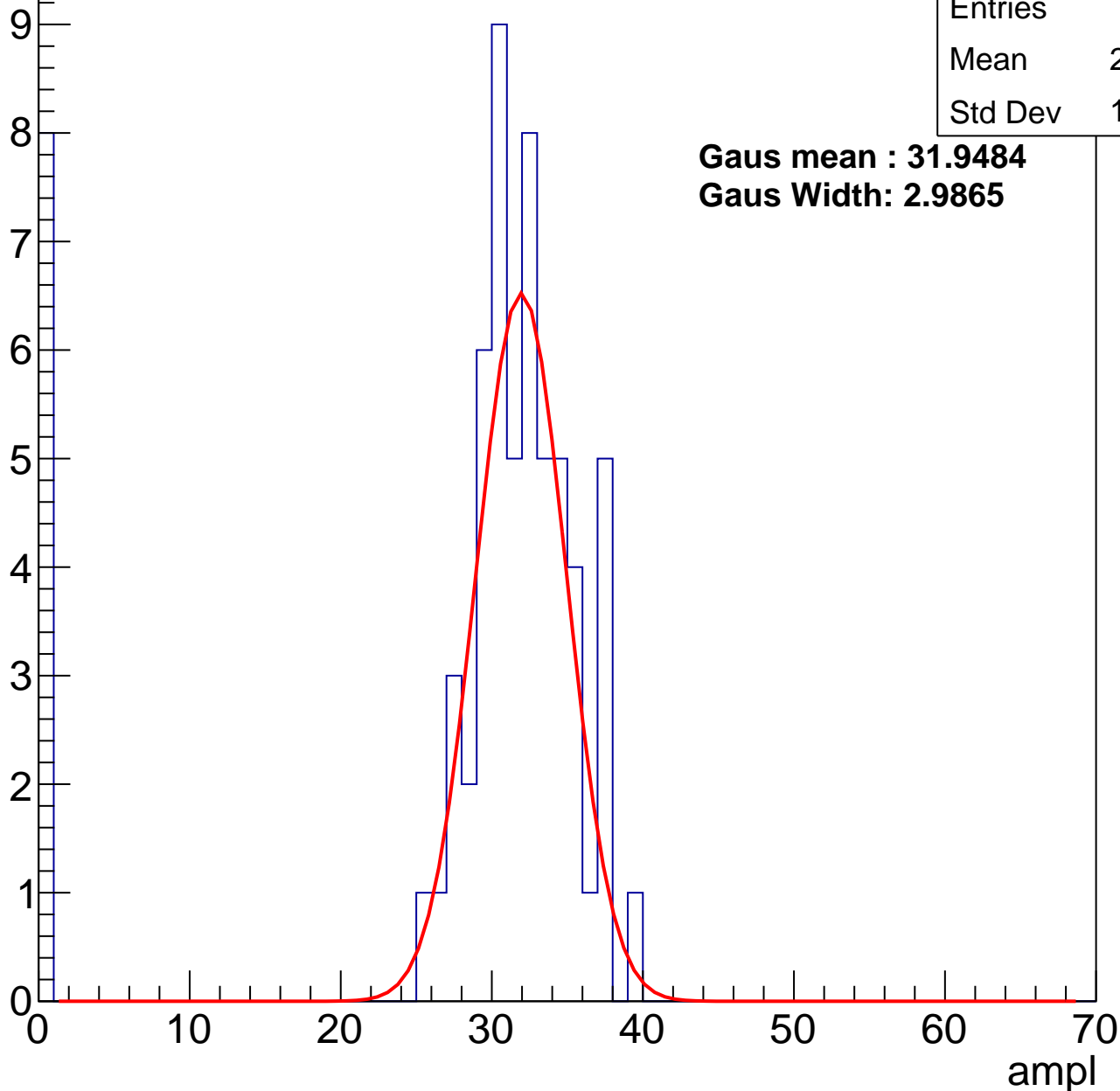
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	64
Mean	27.78
Std Dev	10.89

**Gaus mean : 31.9484**

**Gaus Width: 2.9865**



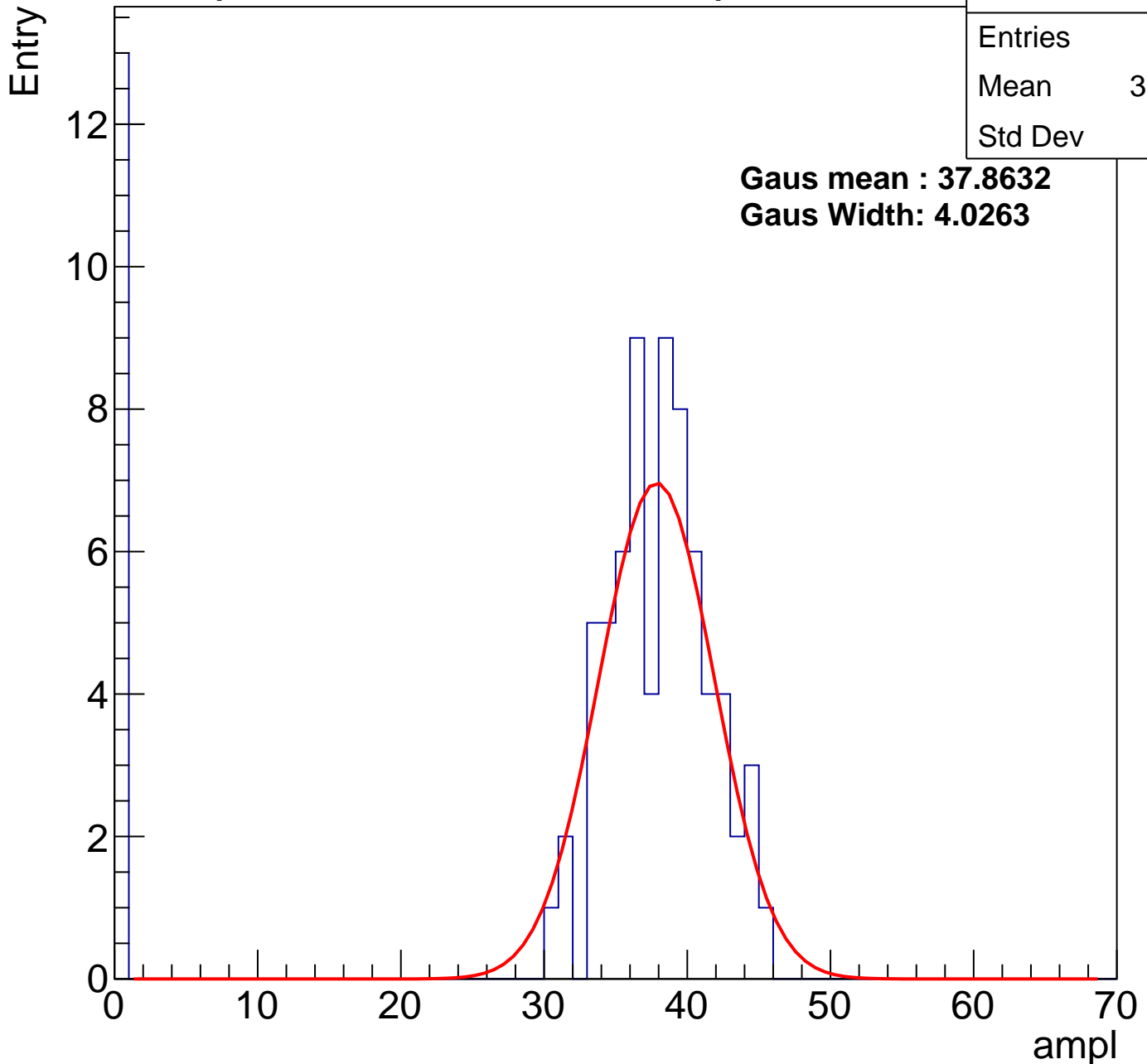
# B1L103S, U26-ch13, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	82
Mean	31.68
Std Dev	14.1

**Gaus mean : 37.8632**

**Gaus Width: 4.0263**



# B1L103S, U26-ch13, adc2

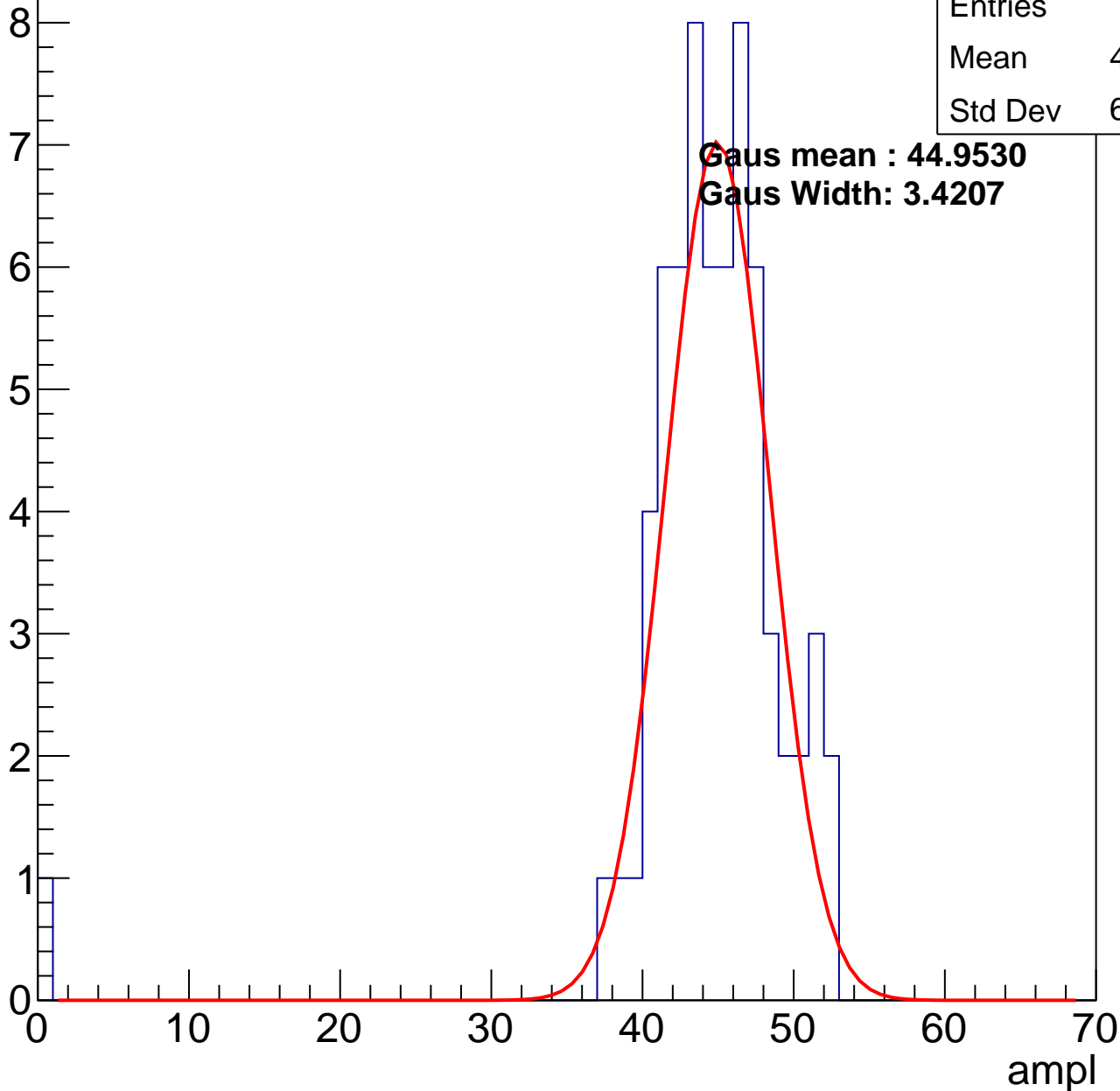
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	66
Mean	43.92
Std Dev	6.435

**Gaus mean : 44.9530**

**Gaus Width: 3.4207**

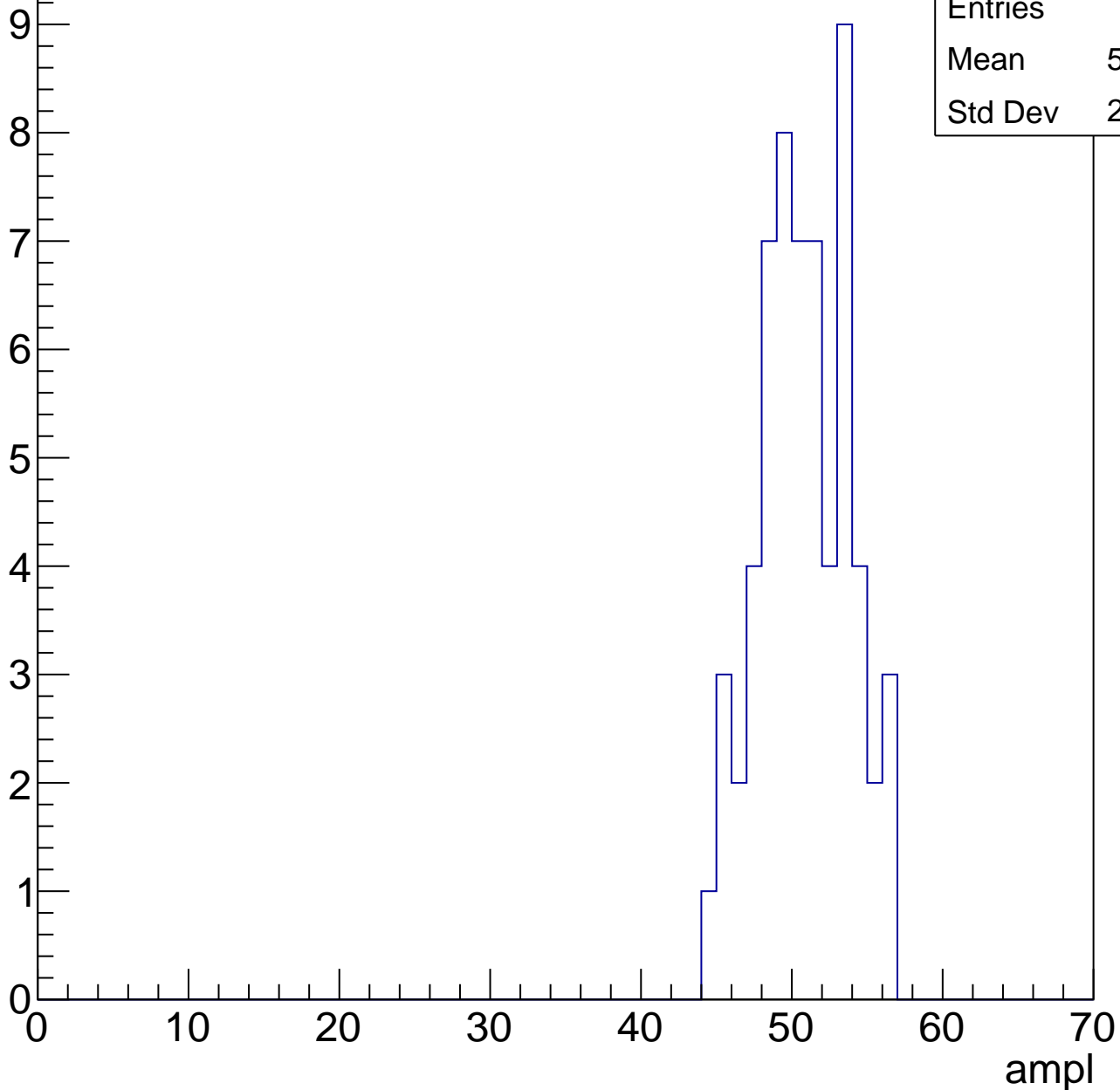


# B1L103S, U26-ch13, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	61
Mean	50.38
Std Dev	2.954



# B1L103S, U26-ch13, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

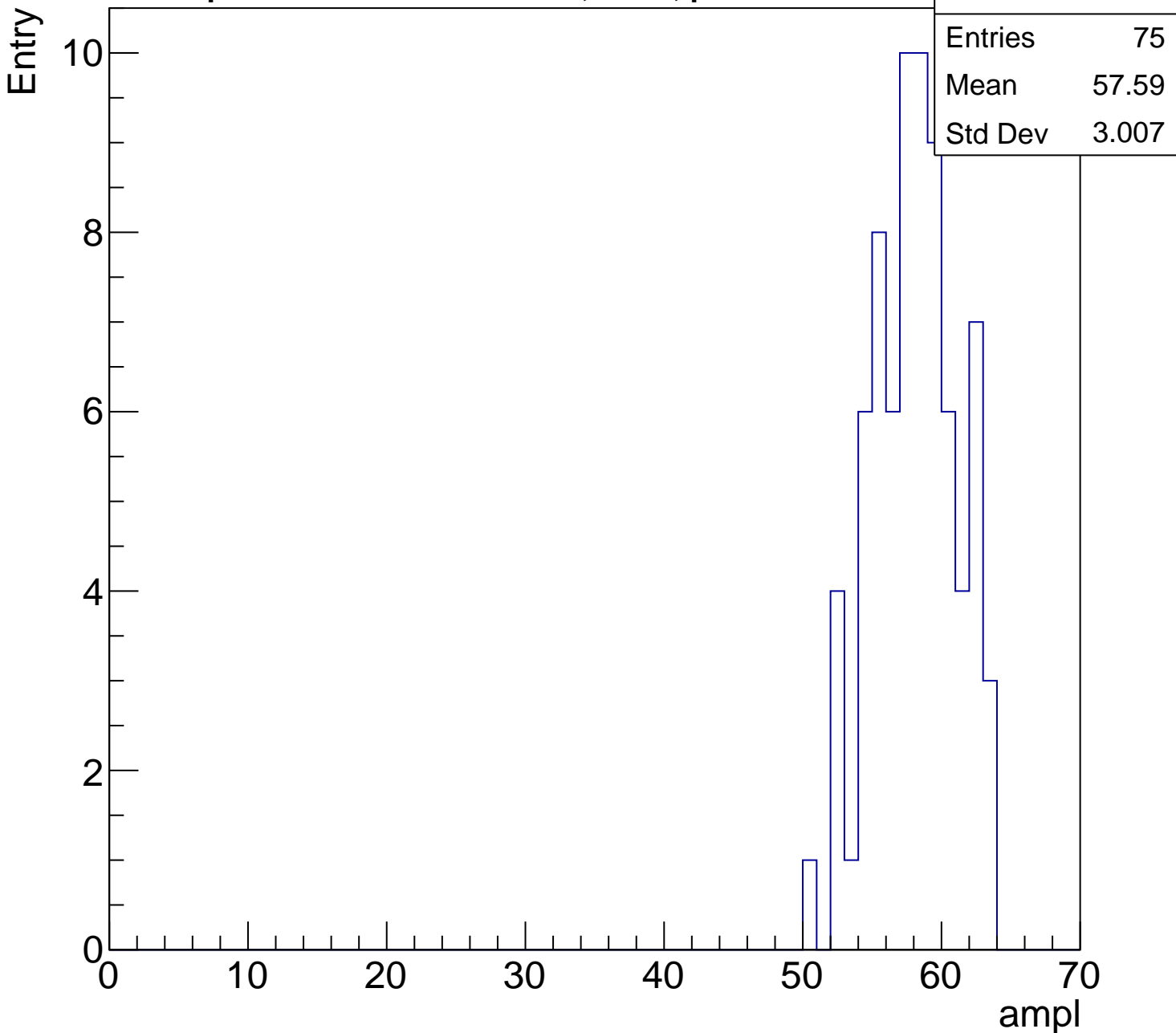
Entries	75
Mean	57.59
Std Dev	3.007

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

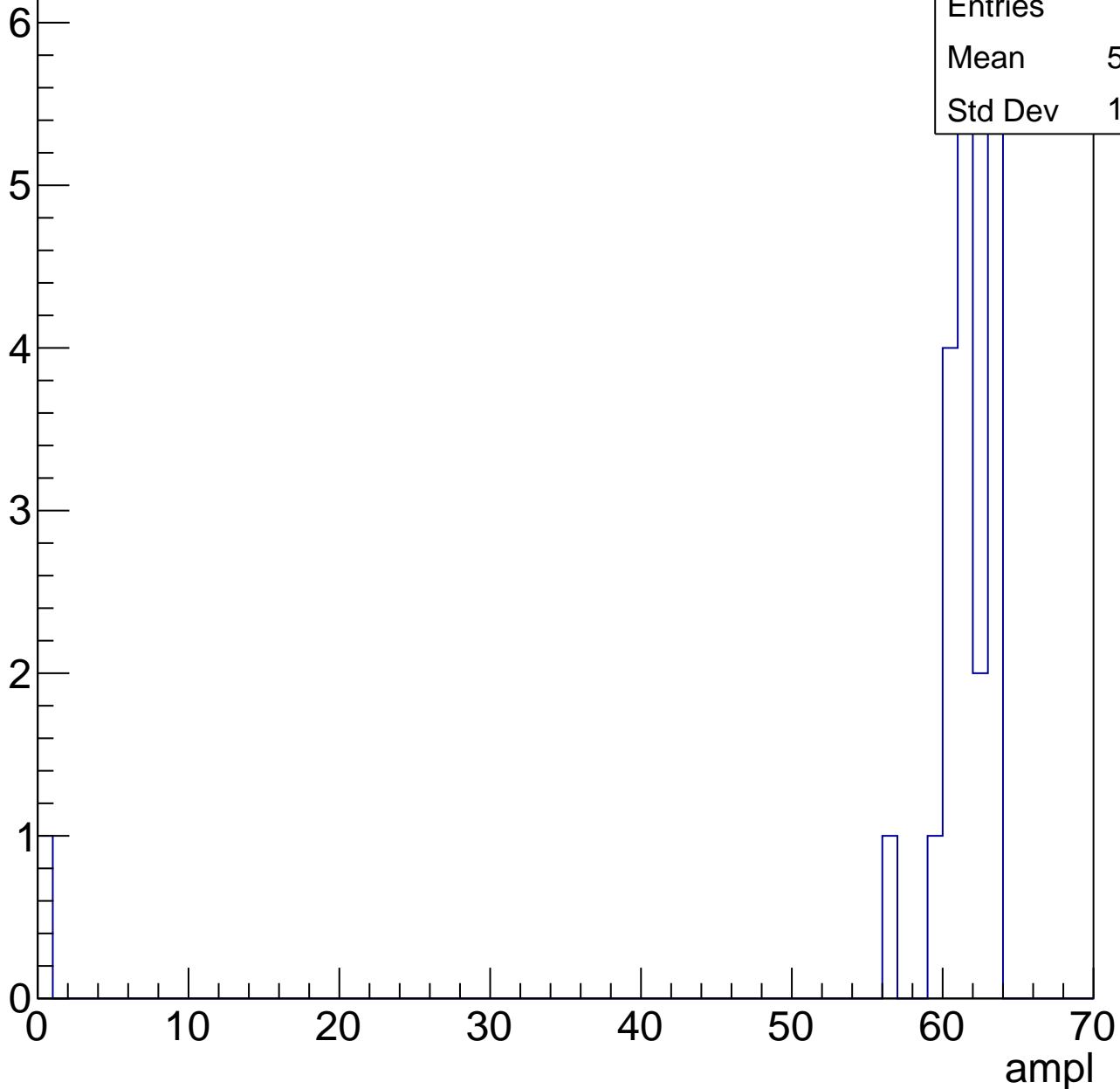


# B1L103S, U26-ch13, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	21
Mean	58.24
Std Dev	13.13



# B1L103S, U26-ch13, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry





# B1L103S, U26-ch13, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



# B1L103S, U26-ch14, adc0

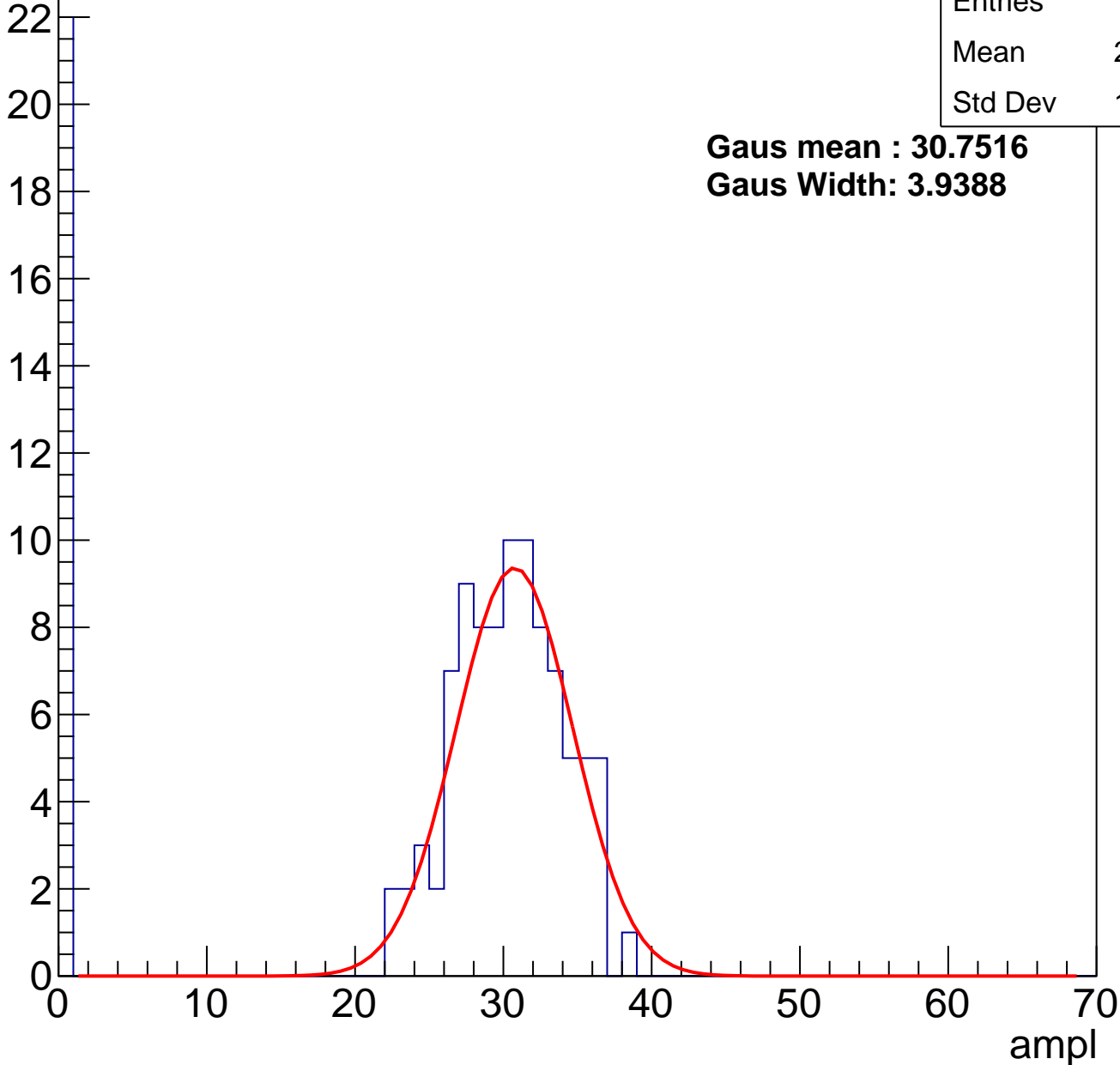
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	114
Mean	24.15
Std Dev	12.24

**Gaus mean : 30.7516**

**Gaus Width: 3.9388**

Entry



# B1L103S, U26-ch14, adc1

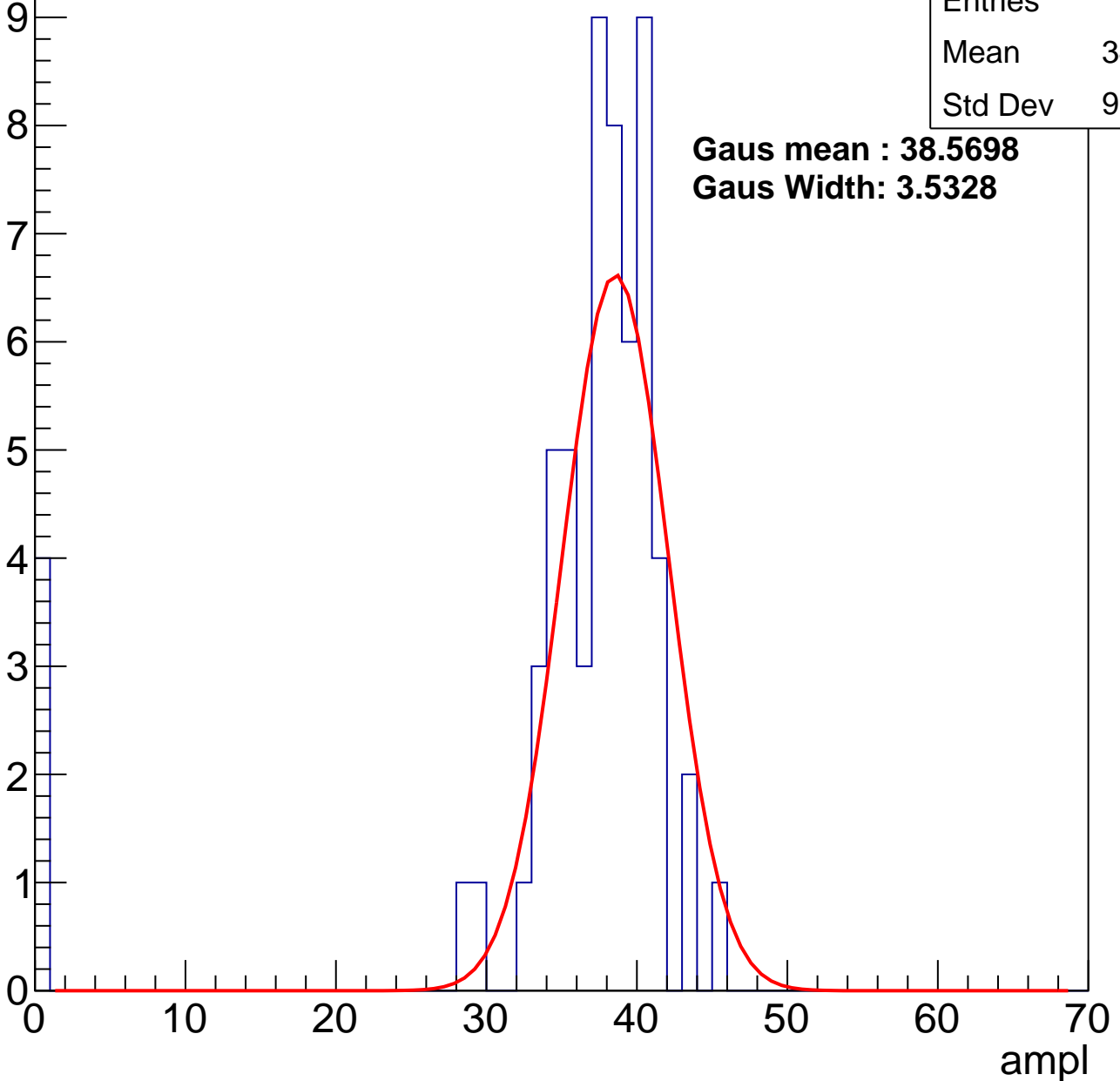
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	62
Mean	34.95
Std Dev	9.684

**Gaus mean : 38.5698**

**Gaus Width: 3.5328**



# B1L103S, U26-ch14, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	74
Mean	36.96
Std Dev	15.72

**Gaus mean : 44.4538**

**Gaus Width: 2.7928**

Entry

10

8

6

4

2

0

0

10

20

30

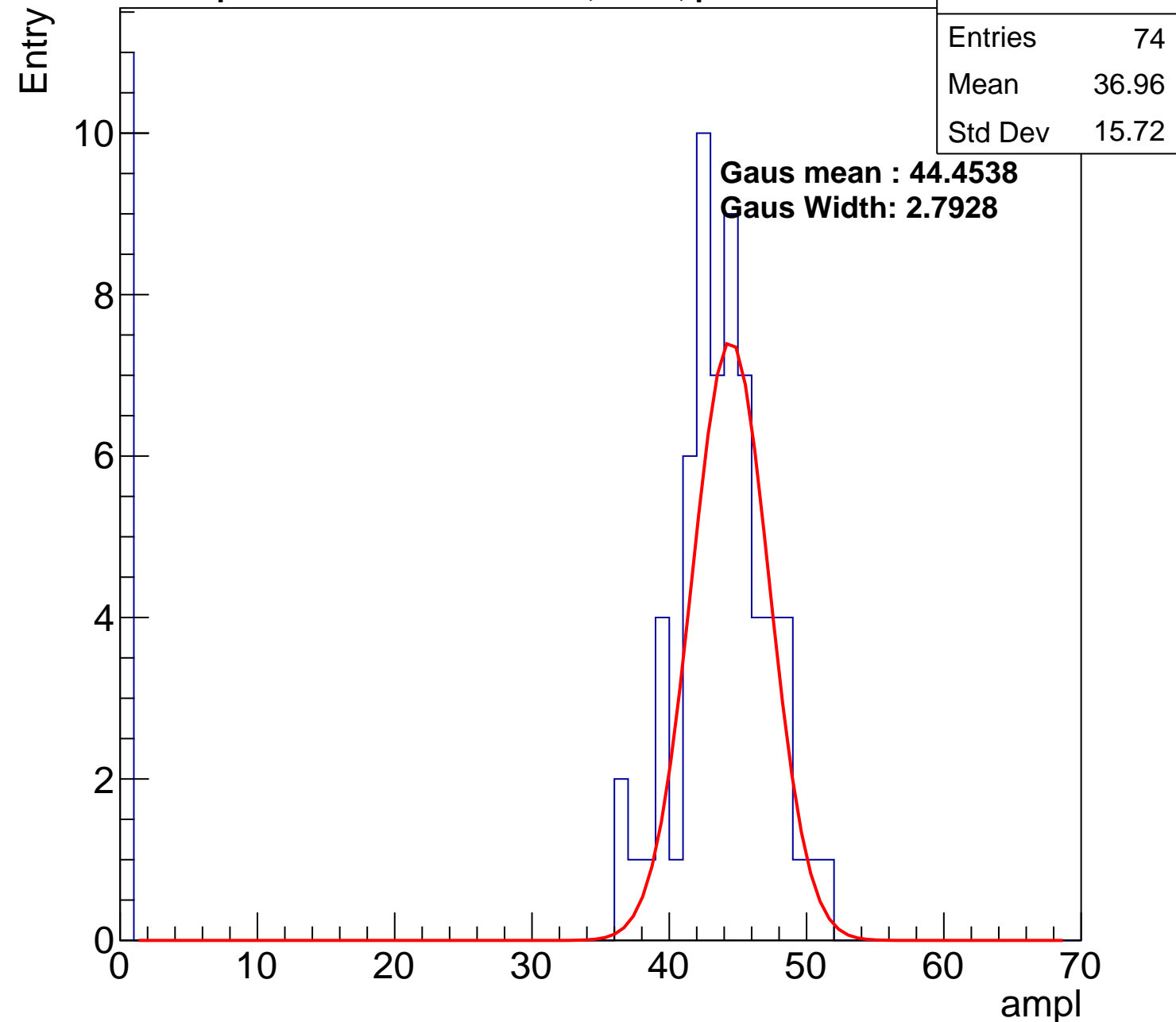
40

50

60

70

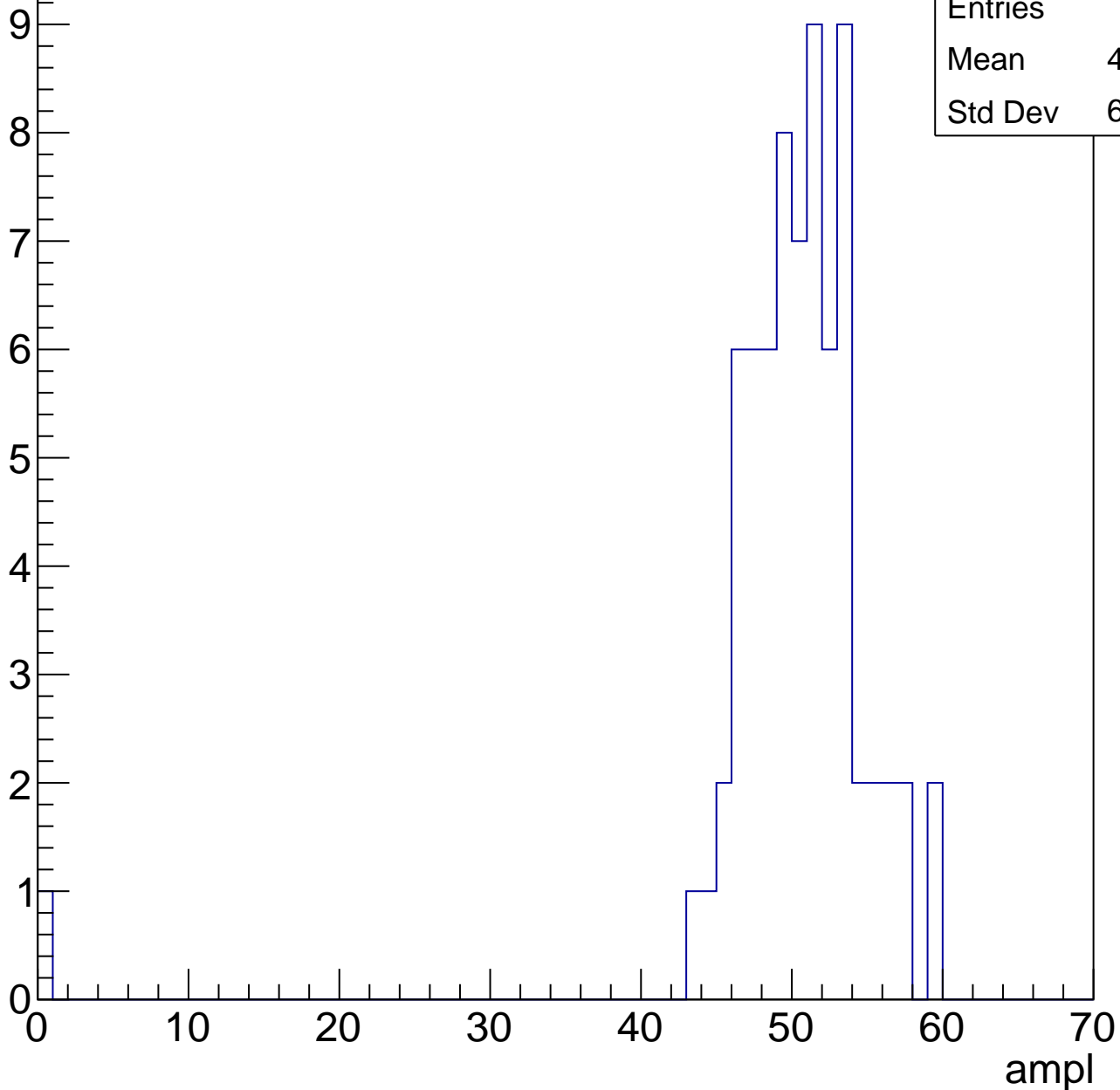
ampl



# B1L103S, U26-ch14, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

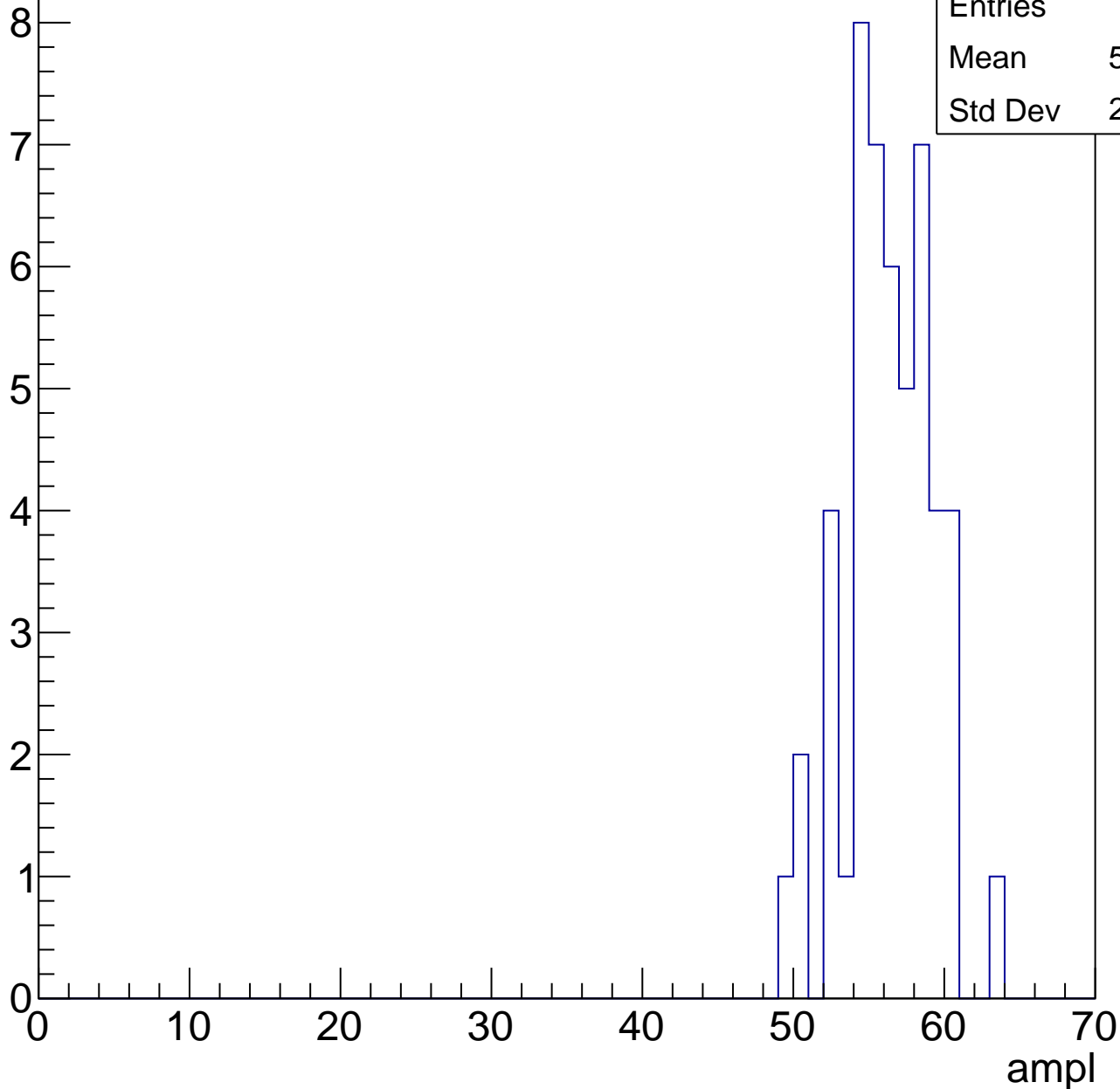


# B1L103S, U26-ch14, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

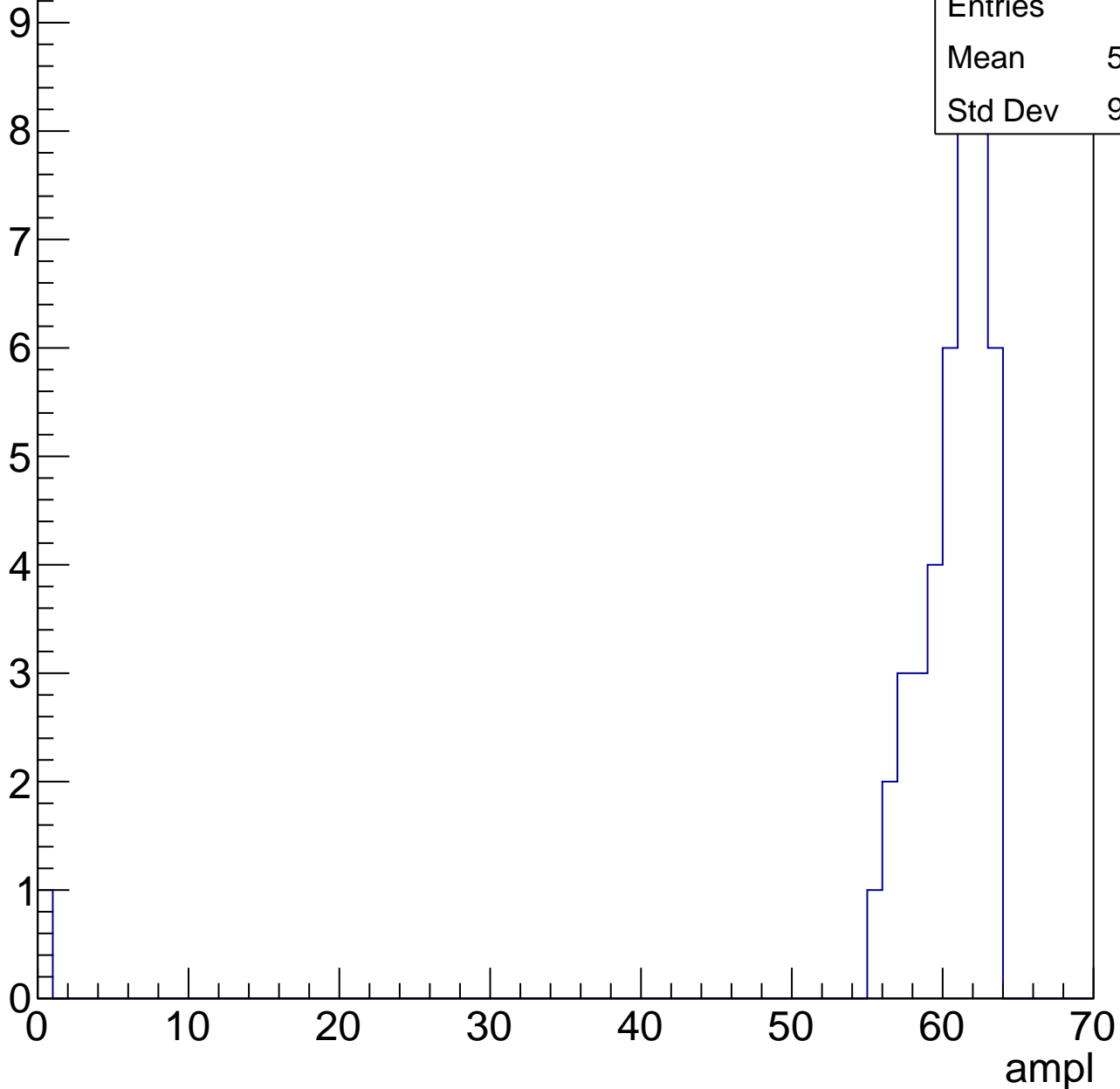
Entries	50
Mean	55.86
Std Dev	2.878



# B1L103S, U26-ch14, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



# B1L103S, U26-ch14, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry





# B1L103S, U26-ch14, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

18  
16  
14  
12  
10  
8  
6  
4  
2  
0

Entries	19
Mean	0
Std Dev	0

ampl

# B1L103S, U26-ch15, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	94
Mean	25.78
Std Dev	10.85

**Gaus mean : 30.8640**

**Gaus Width: 3.5036**

Entry

12

10

8

6

4

2

0

0

10

20

30

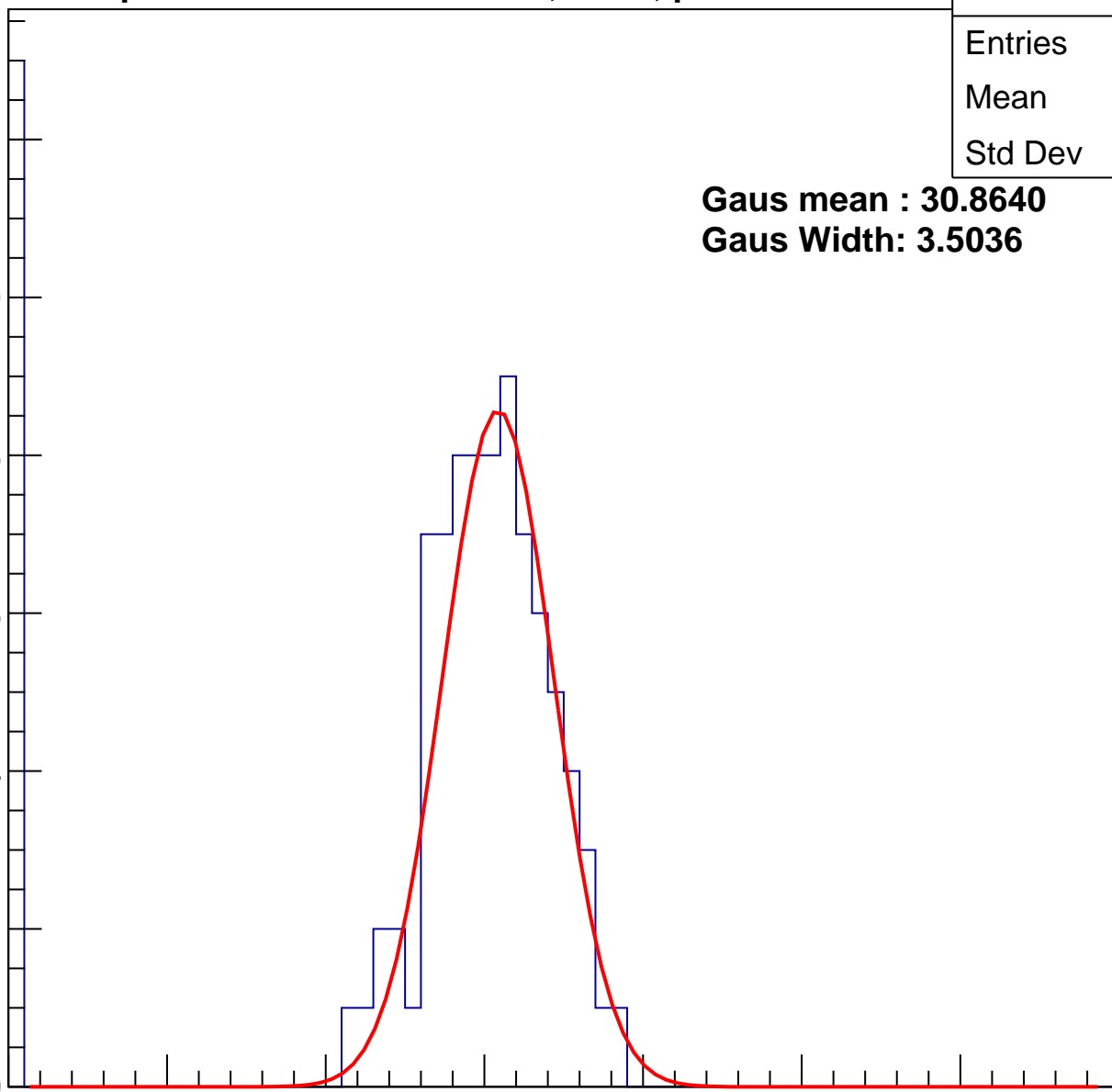
40

50

60

70

ampl



# B1L103S, U26-ch15, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	68
Mean	29.49
Std Dev	14.71

**Gaus mean : 37.4085**

**Gaus Width: 4.0734**

Entry

12

10

8

6

4

2

0

0

10

20

30

40

50

60

70

ampl

0

2

4

6

8

10

12

# B1L103S, U26-ch15, adc2

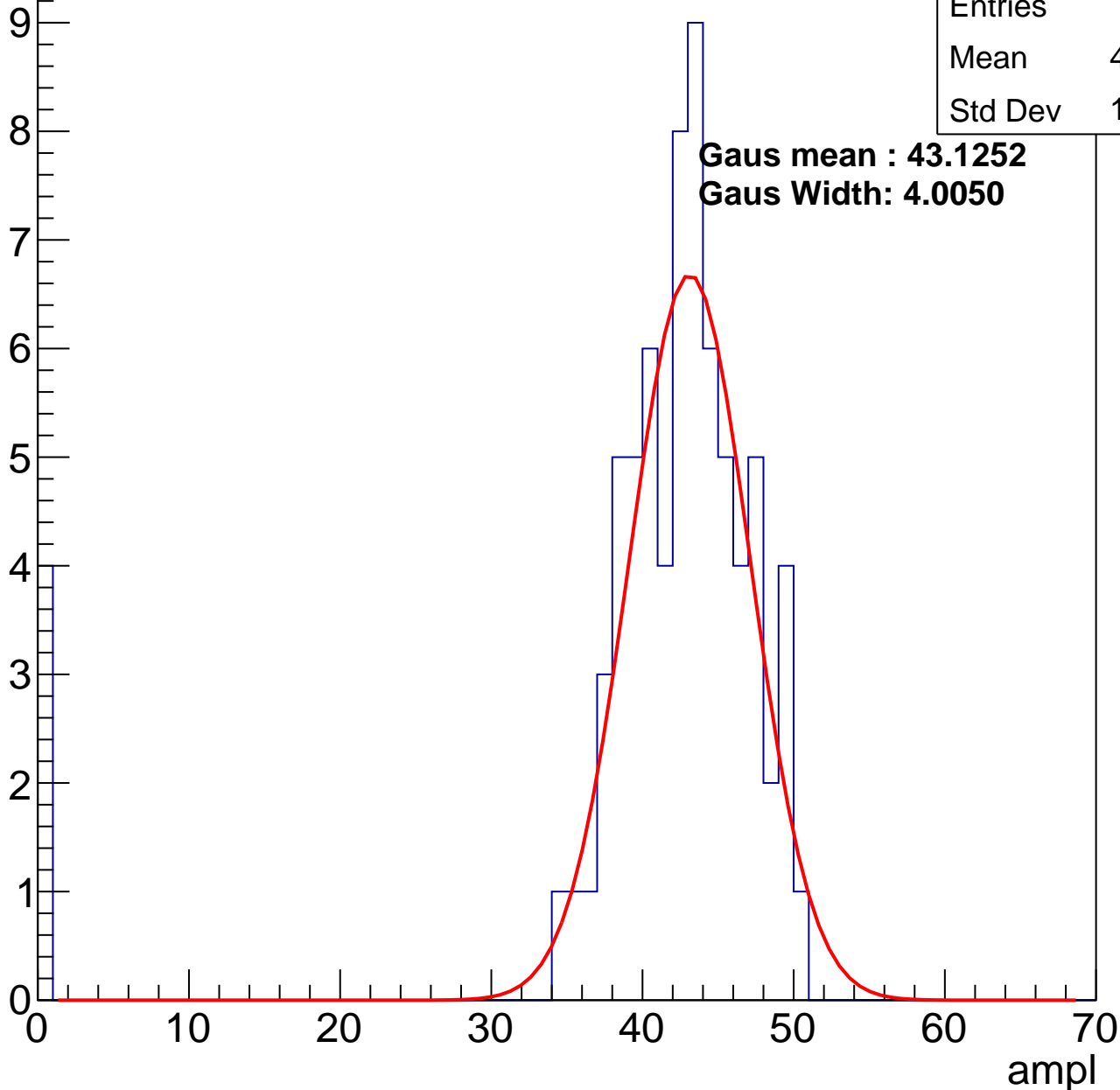
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	74
Mean	40.24
Std Dev	10.27

**Gaus mean : 43.1252**

**Gaus Width: 4.0050**

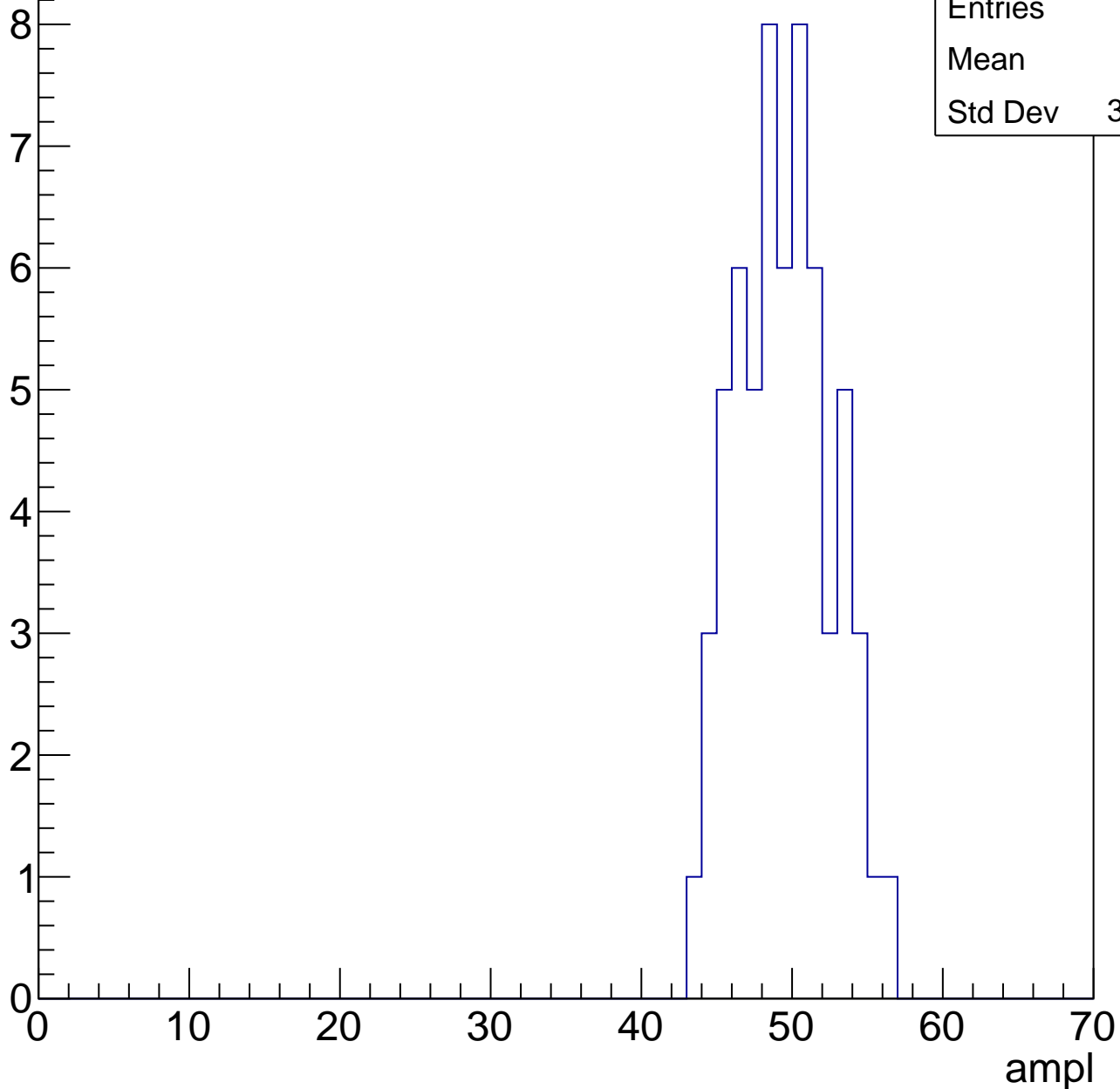


# B1L103S, U26-ch15, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	61
Mean	49
Std Dev	3.062

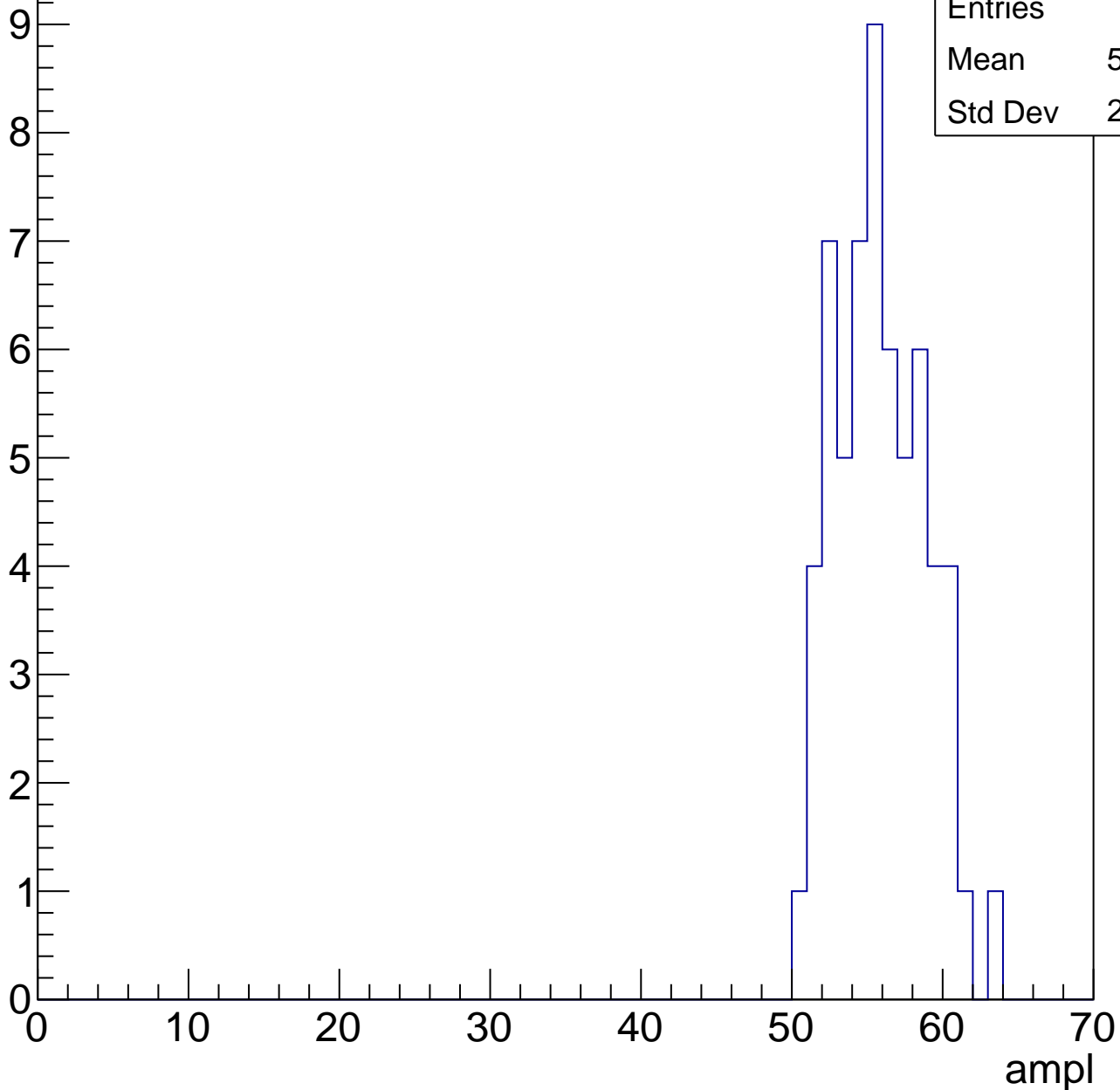


# B1L103S, U26-ch15, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	60
Mean	55.42
Std Dev	2.923

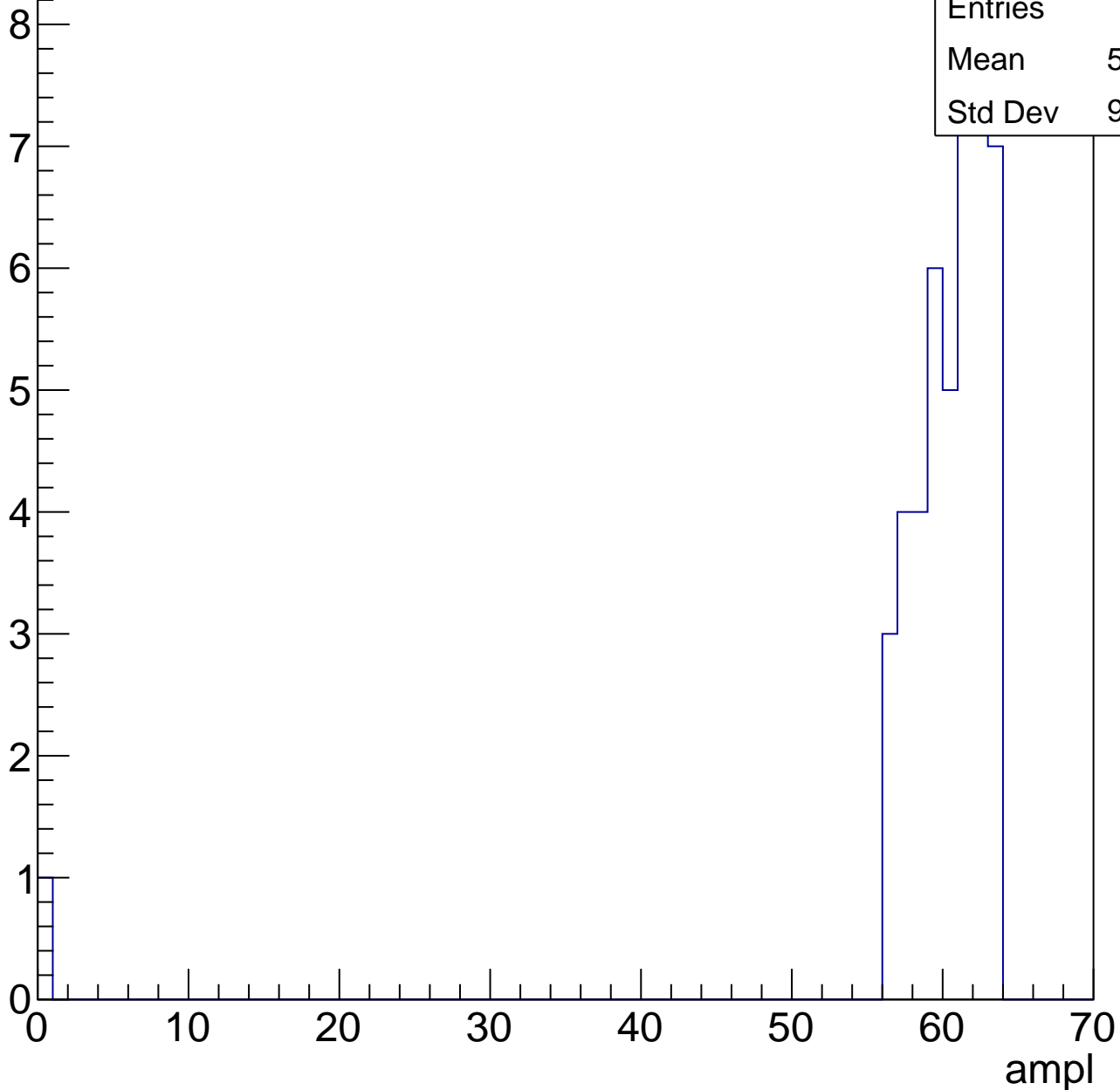


# B1L103S, U26-ch15, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

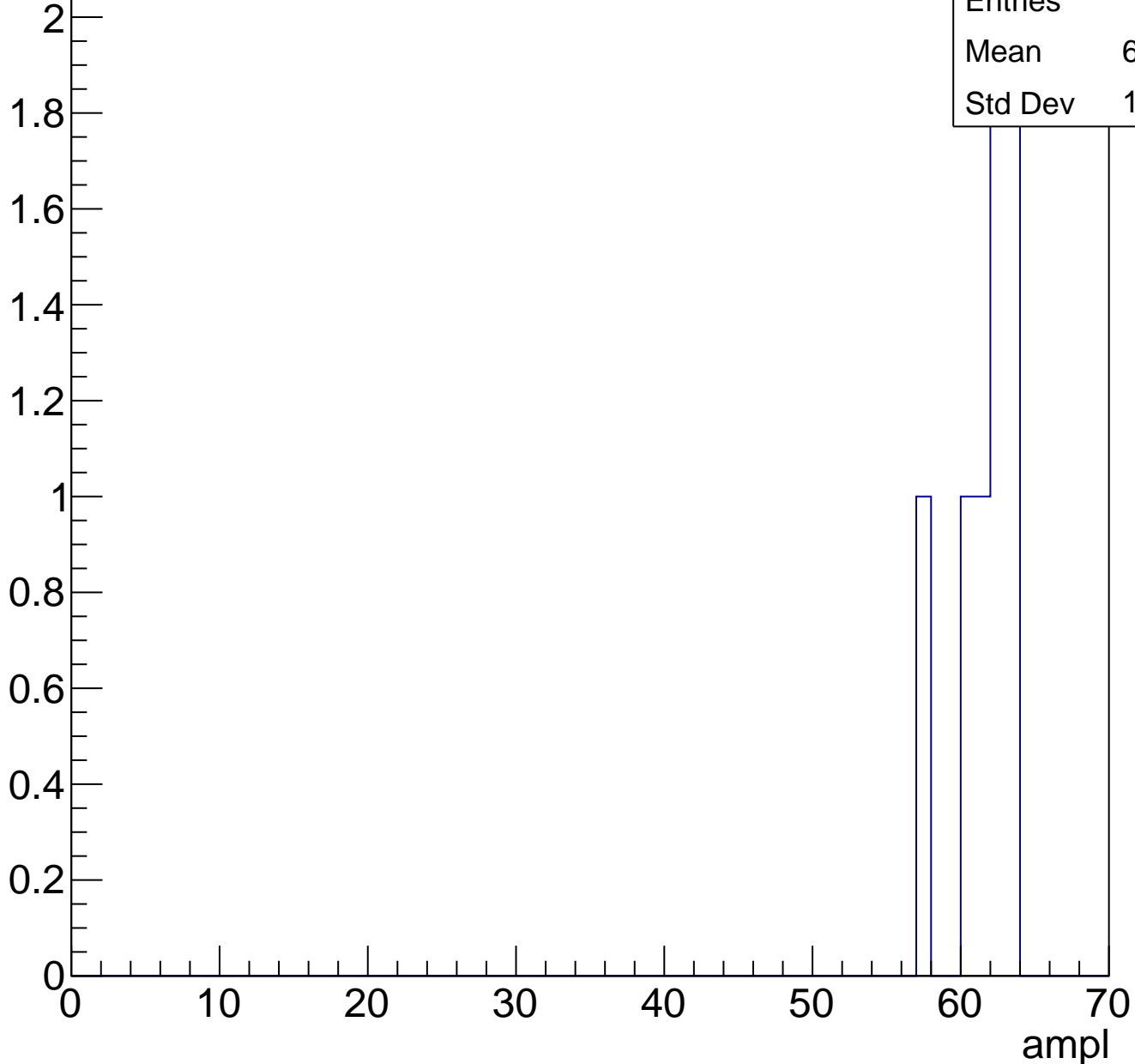
Entries	46
Mean	58.85
Std Dev	9.026



# B1L103S, U26-ch15, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry





# B1L103S, U26-ch15, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

18  
16  
14  
12  
10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

Entries	19
Mean	0
Std Dev	0

# B1L103S, U26-ch16, adc0

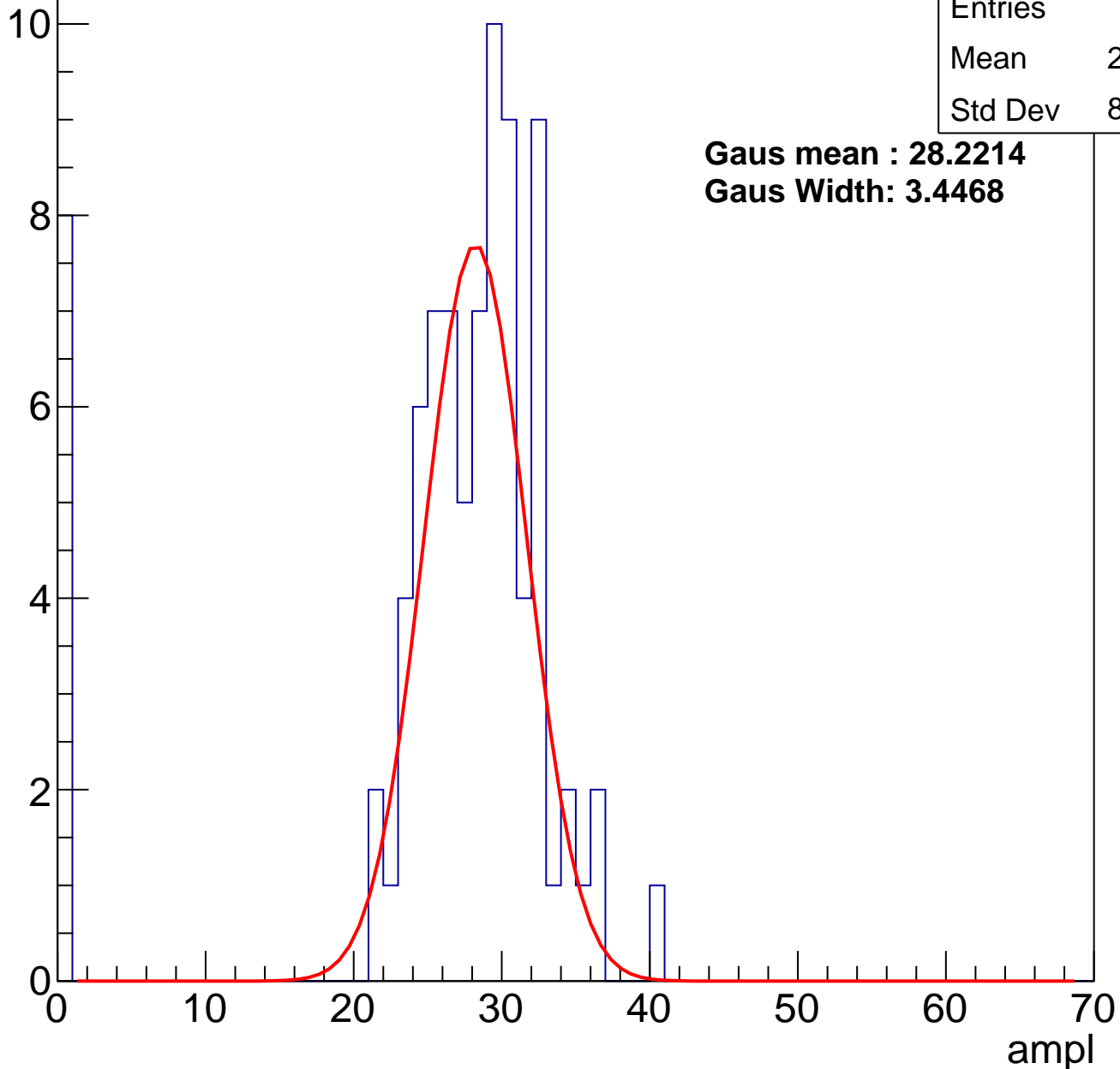
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	86
Mean	25.67
Std Dev	8.942

**Gaus mean : 28.2214**

**Gaus Width: 3.4468**

Entry



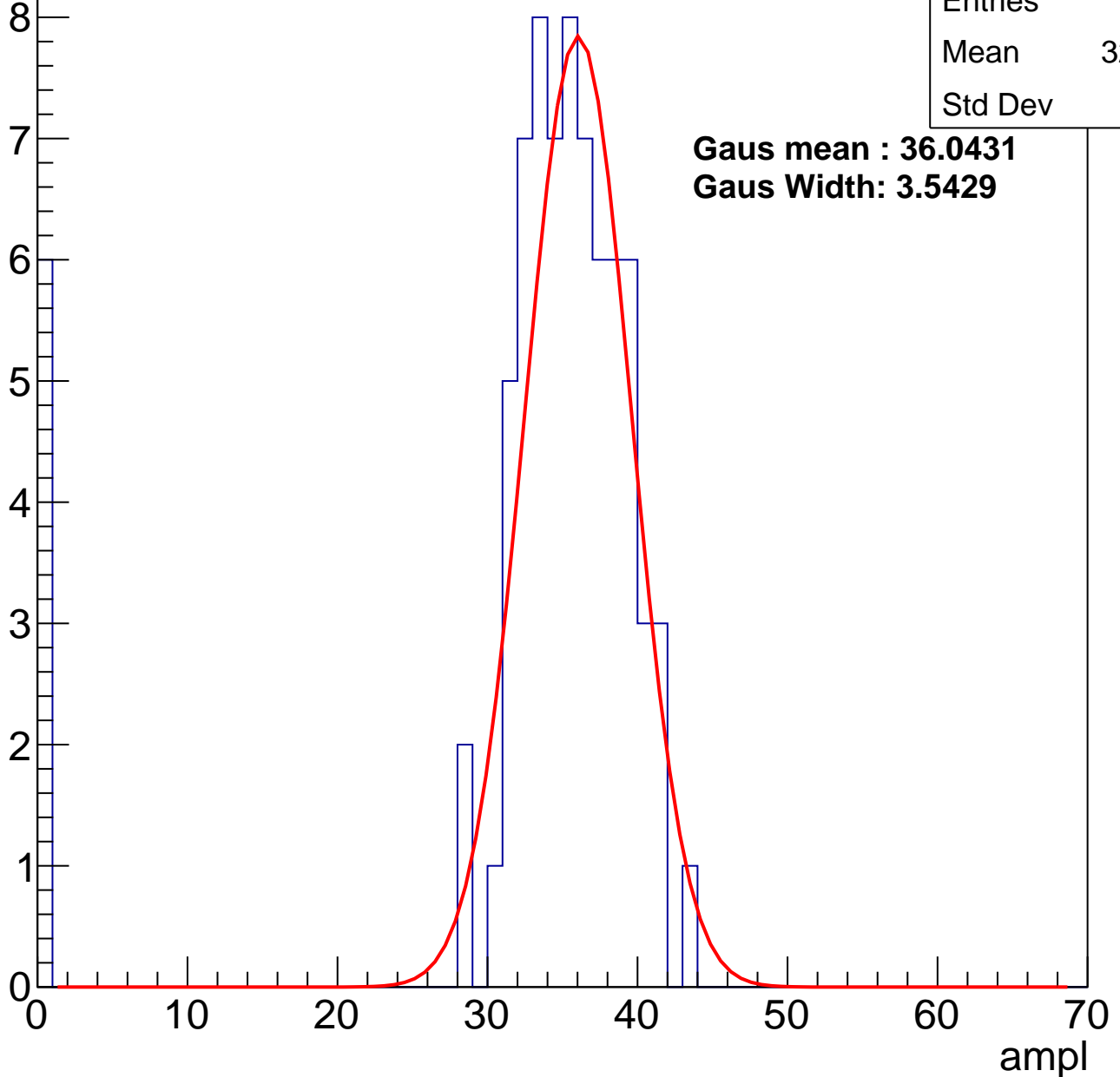
# B1L103S, U26-ch16, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	76
Mean	32.49
Std Dev	10

**Gaus mean : 36.0431**  
**Gaus Width: 3.5429**



# B1L103S, U26-ch16, adc2

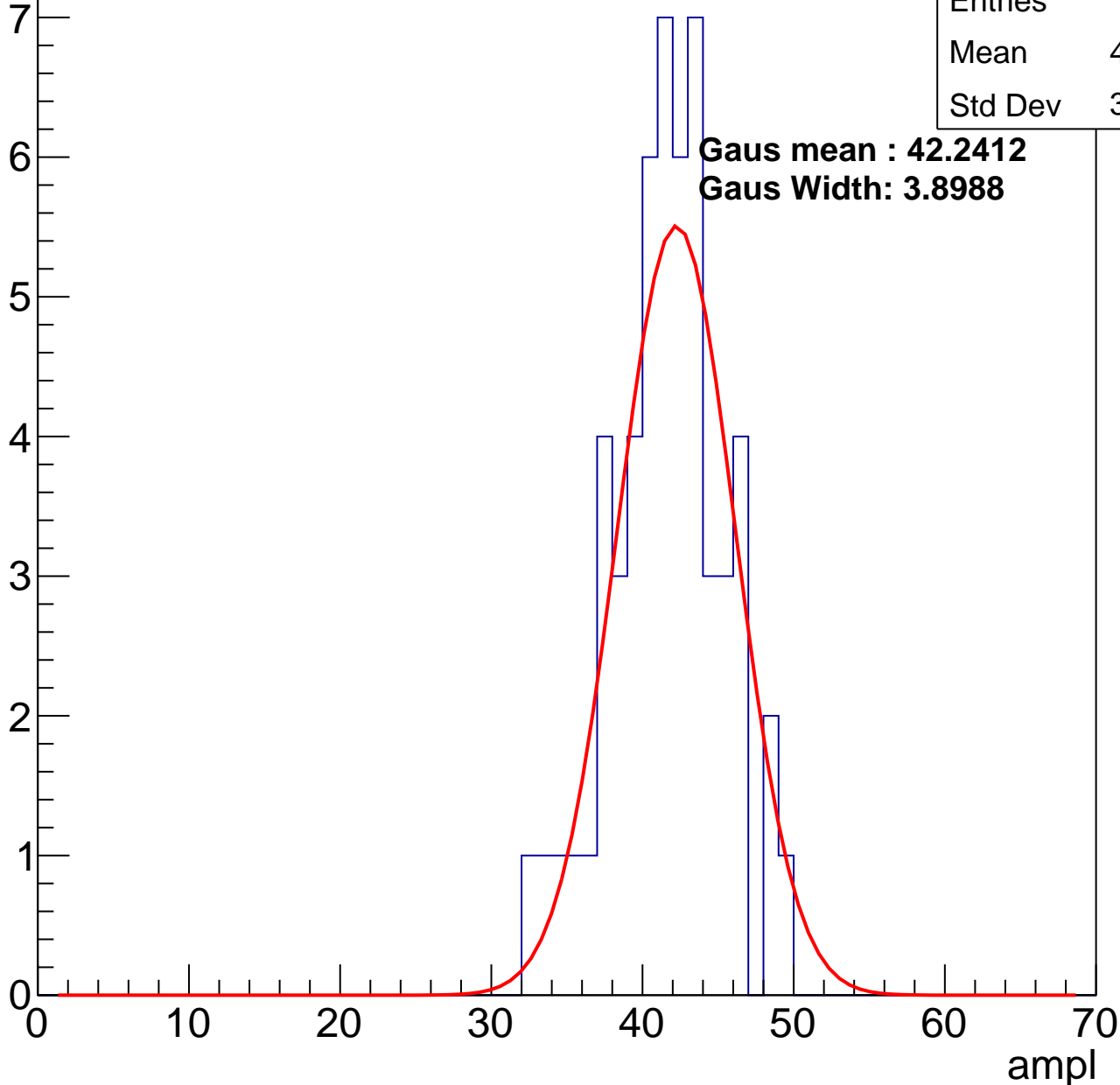
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	55
Mean	41.16
Std Dev	3.662

**Gaus mean : 42.2412**

**Gaus Width: 3.8988**

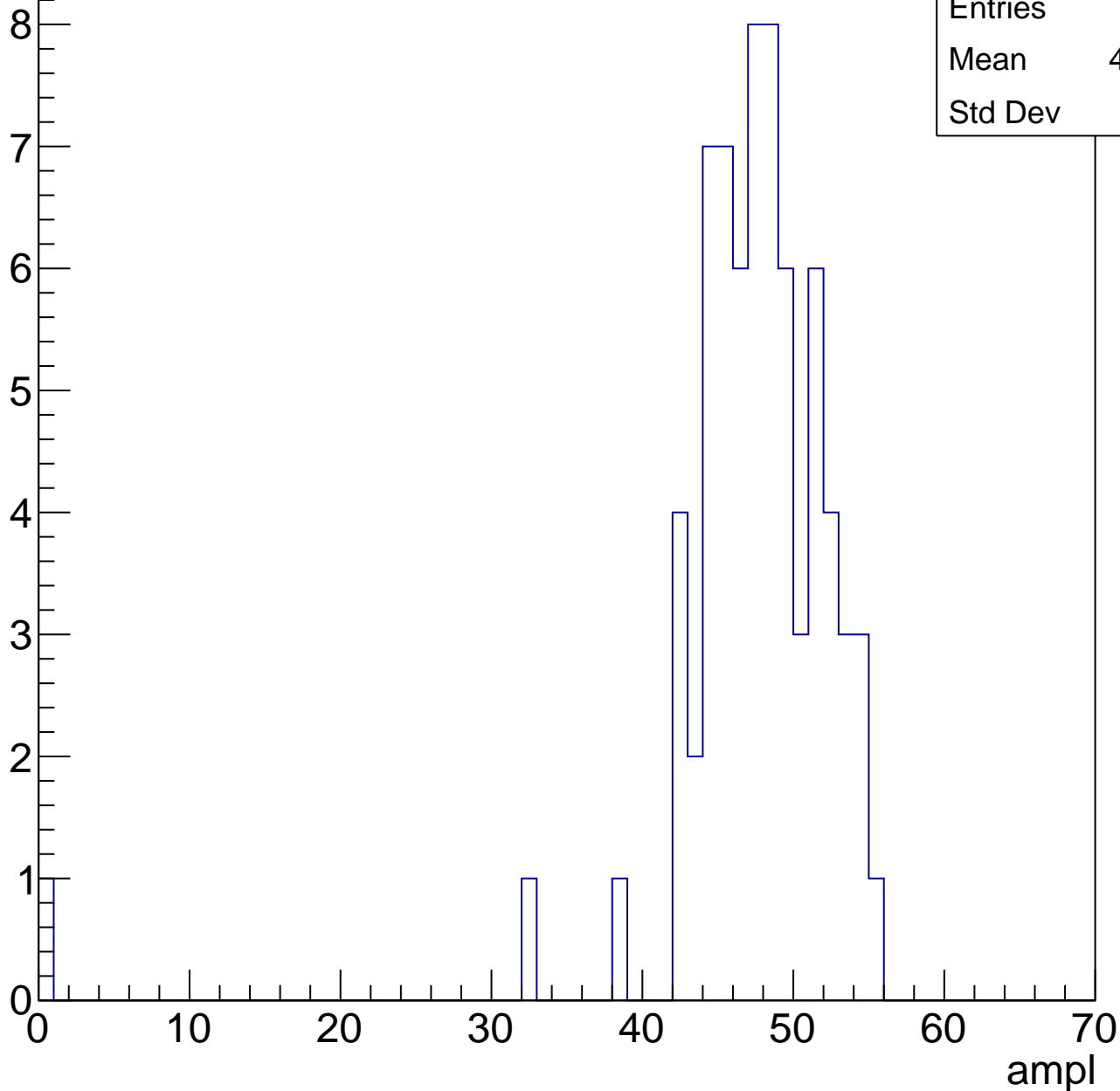


# B1L103S, U26-ch16, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	71
Mean	46.72
Std Dev	6.83

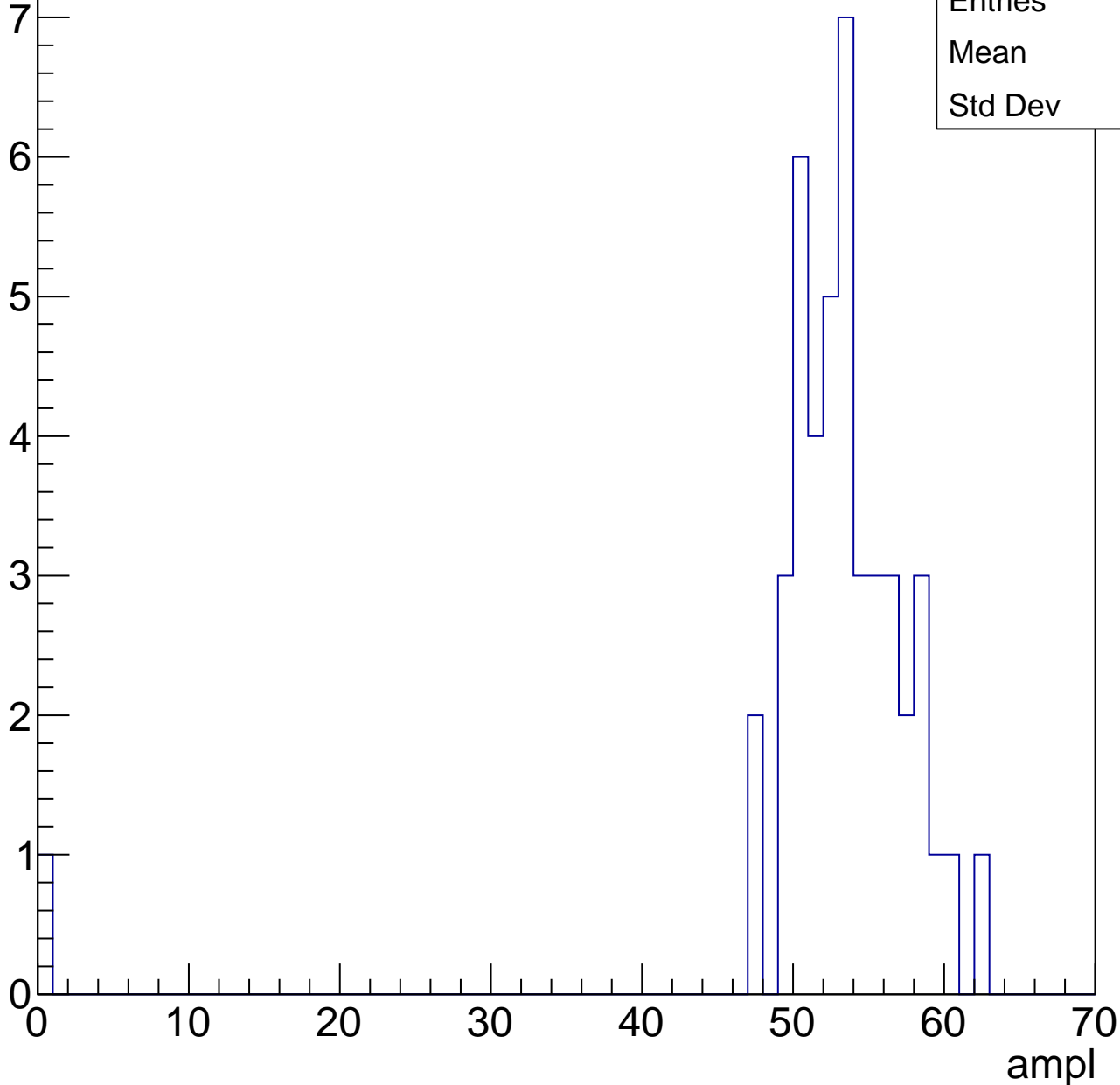


# B1L103S, U26-ch16, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	45
Mean	52
Std Dev	8.53

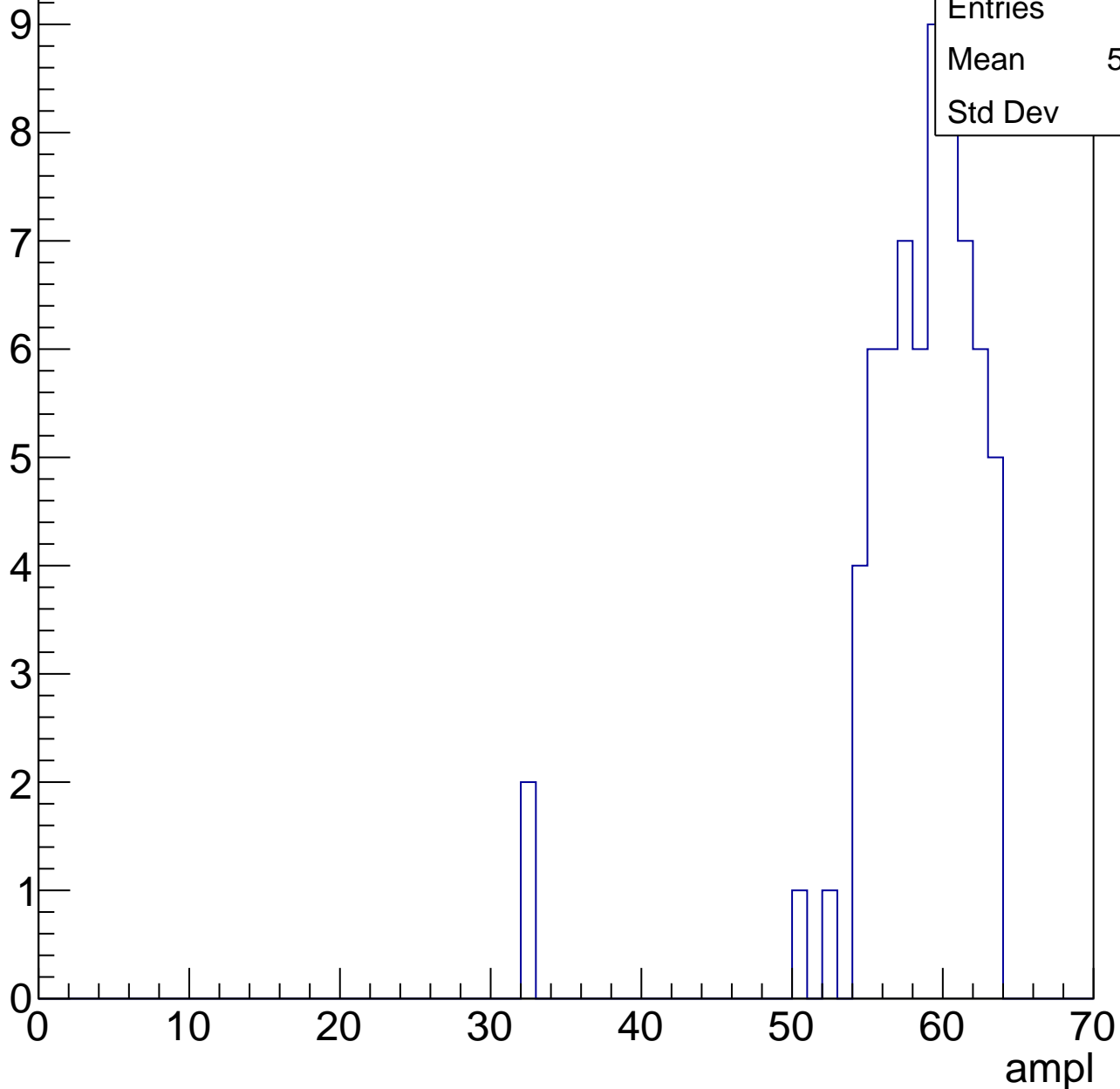


# B1L103S, U26-ch16, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	68
Mean	57.65
Std Dev	5.31

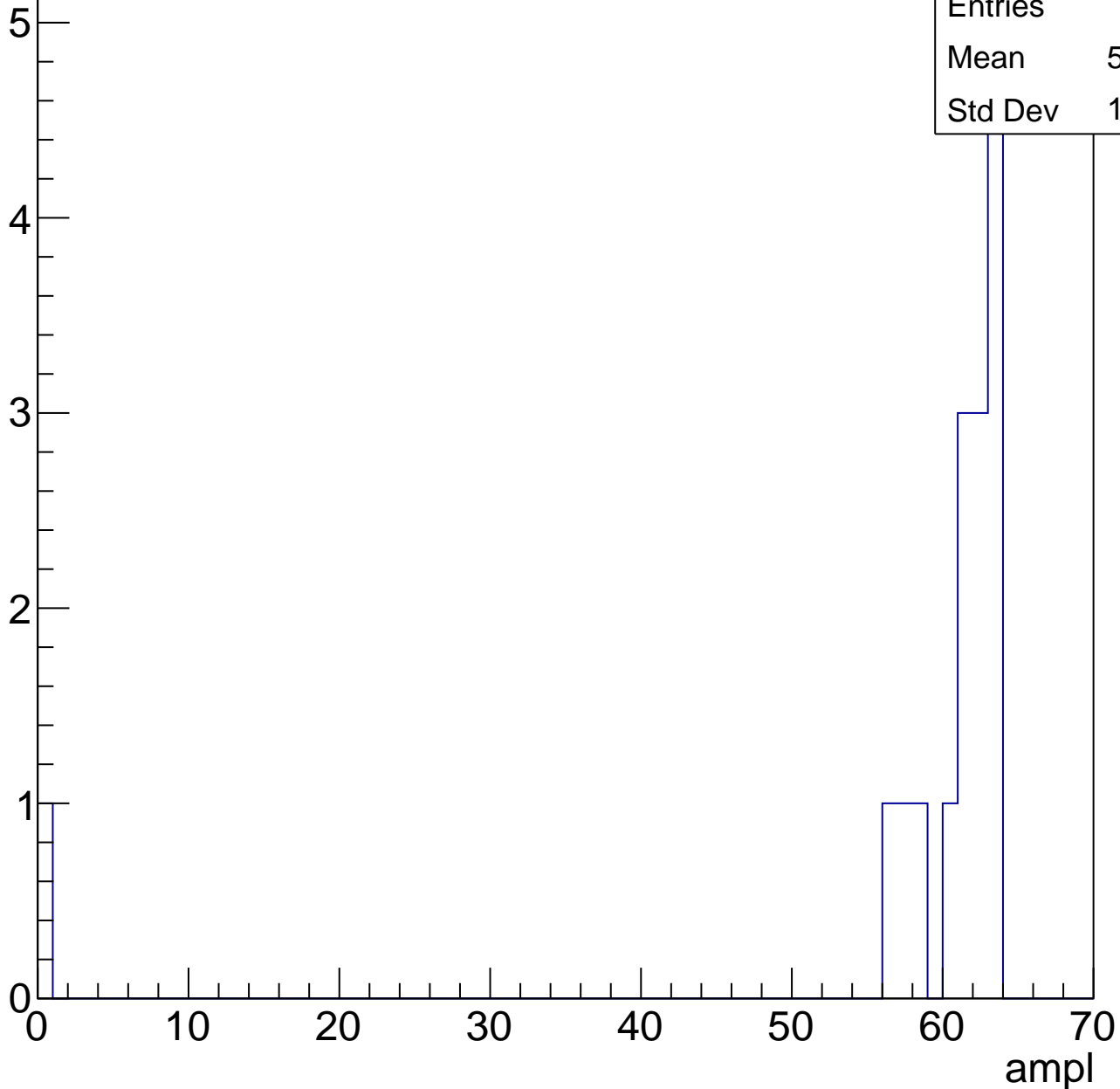


# B1L103S, U26-ch16, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	16
Mean	57.19
Std Dev	14.92





# B1L103S, U26-ch16, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

18  
16  
14  
12  
10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

Entries	19
Mean	0
Std Dev	0

# B1L103S, U26-ch17, adc0

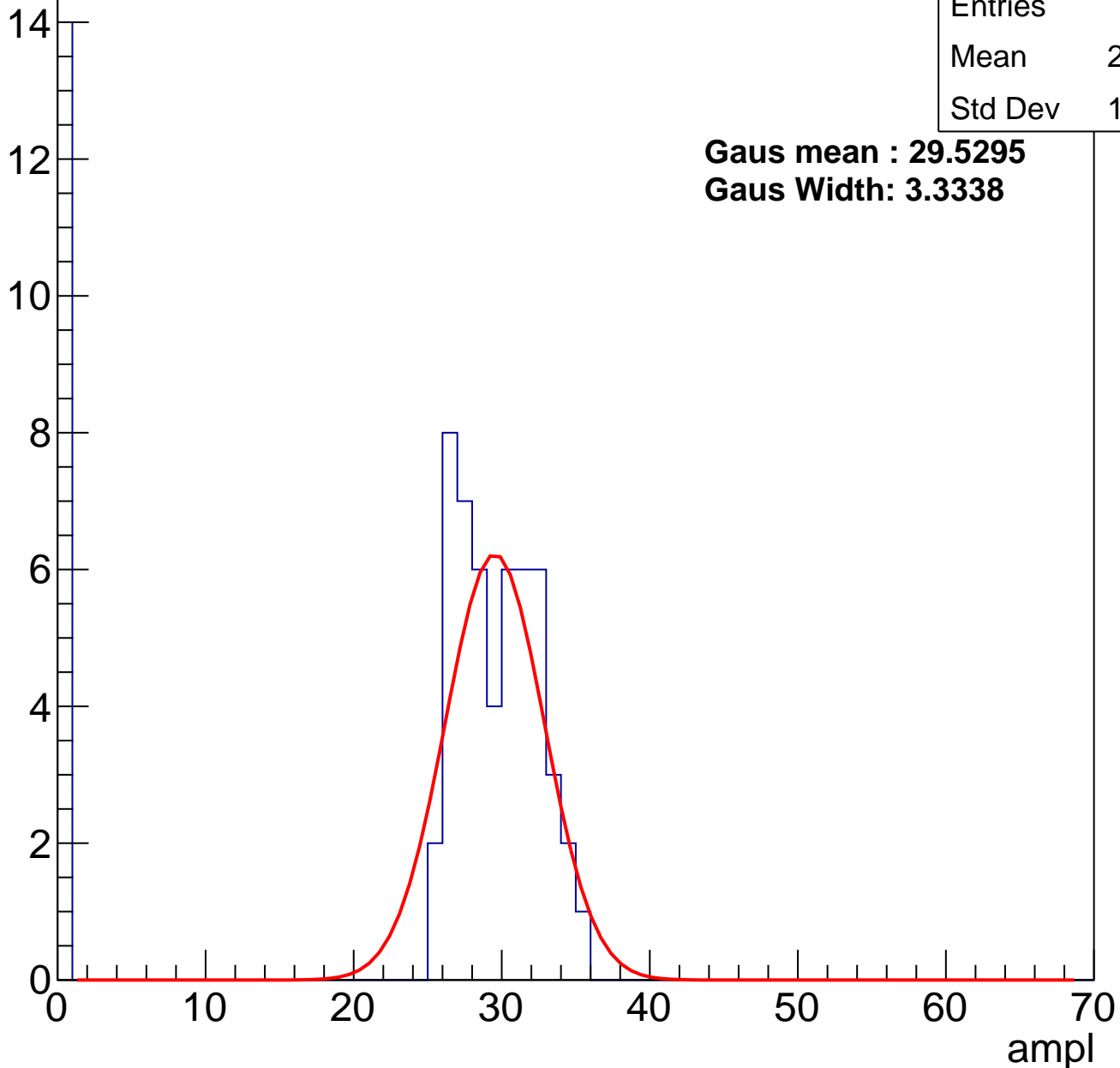
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	65
Mean	22.94
Std Dev	12.24

**Gaus mean : 29.5295**

**Gaus Width: 3.3338**

Entry



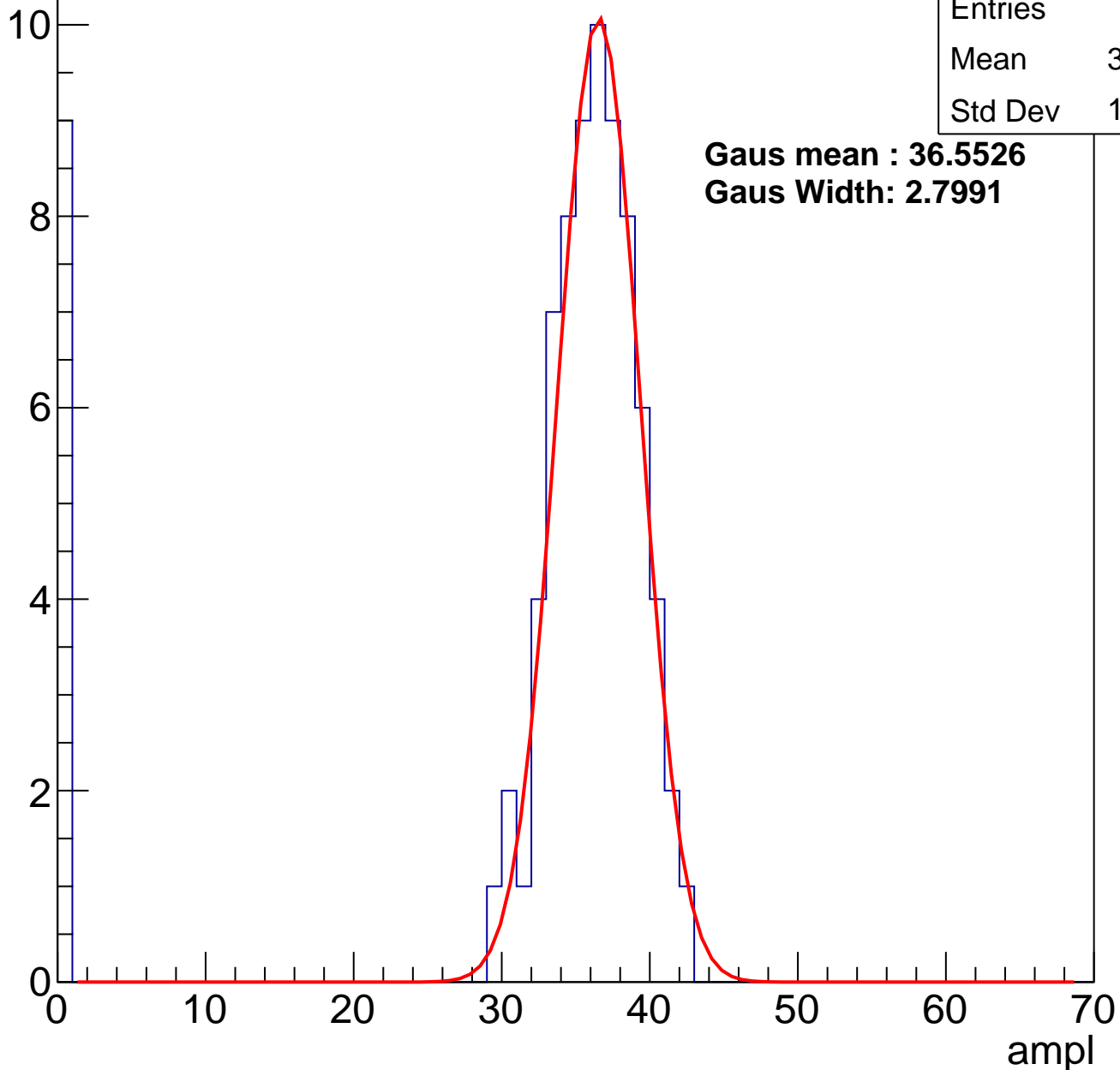
# B1L103S, U26-ch17, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	81
Mean	31.86
Std Dev	11.57

**Gaus mean : 36.5526**  
**Gaus Width: 2.7991**

Entry



# B1L103S, U26-ch17, adc2

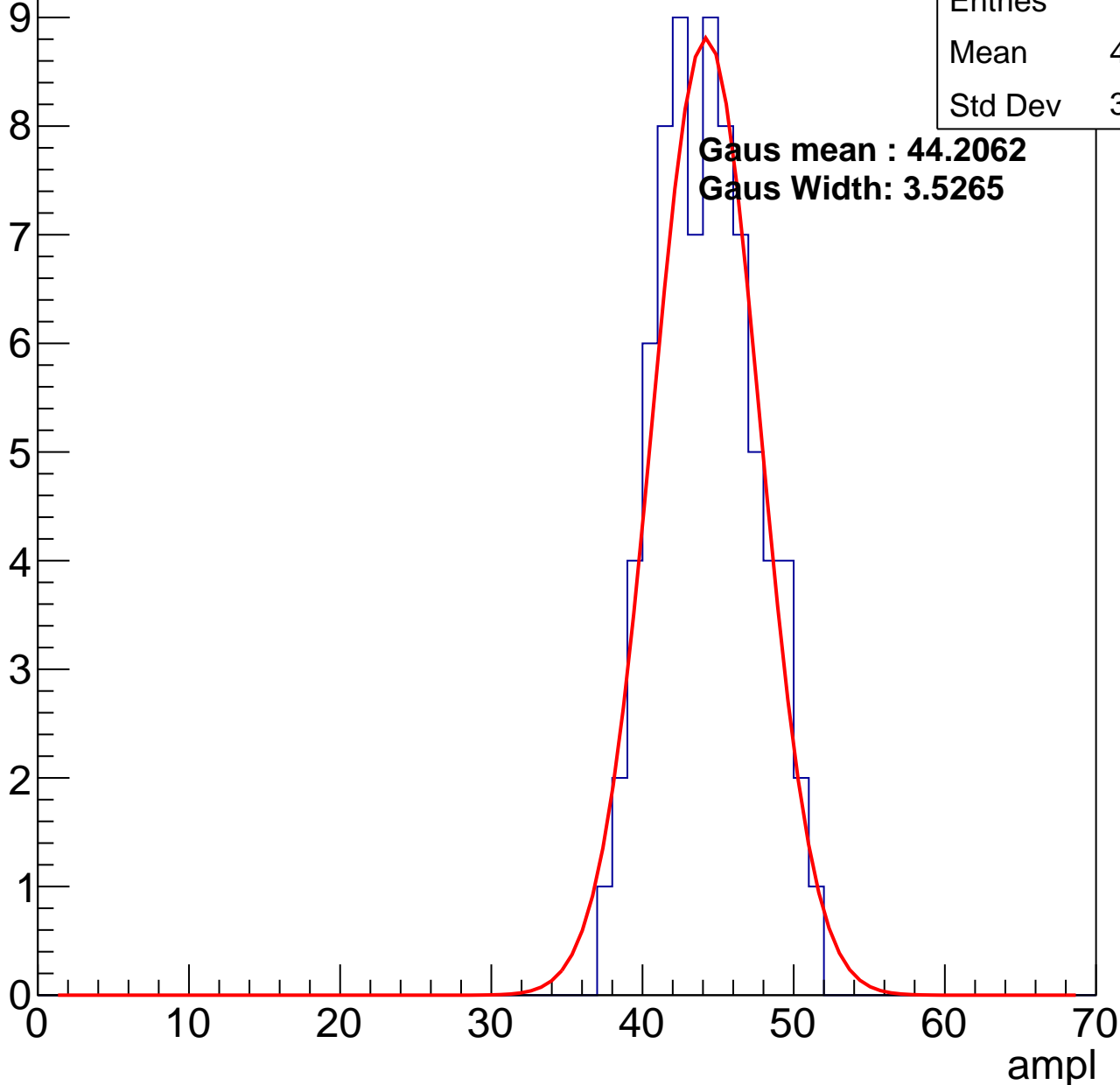
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	77
Mean	43.74
Std Dev	3.209

**Gaus mean : 44.2062**

**Gaus Width: 3.5265**

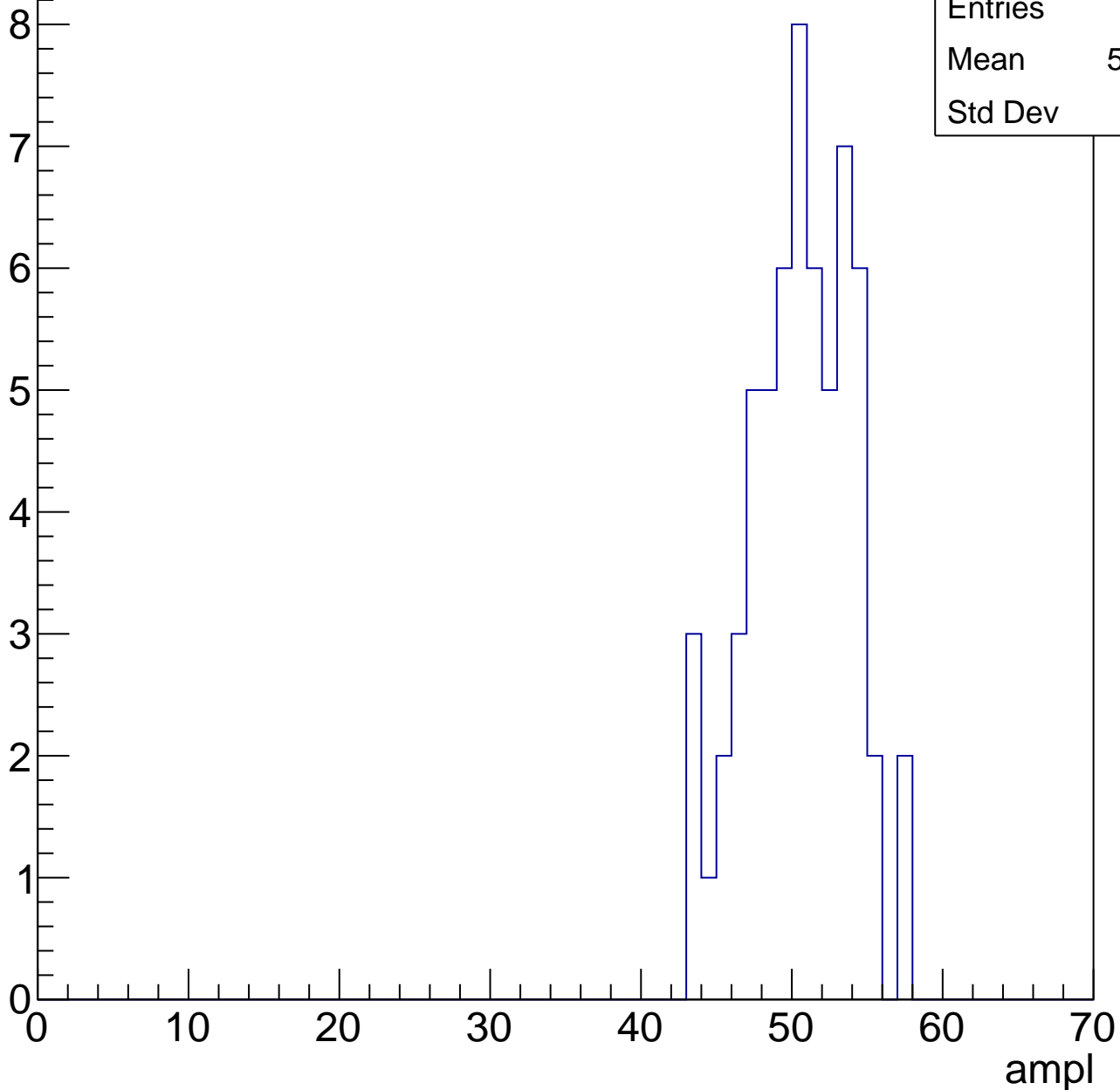


# B1L103S, U26-ch17, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	61
Mean	50.08
Std Dev	3.35



# B1L103S, U26-ch17, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	53
Mean	55.79
Std Dev	2.999

Entry

10

8

6

4

2

0

0

10

20

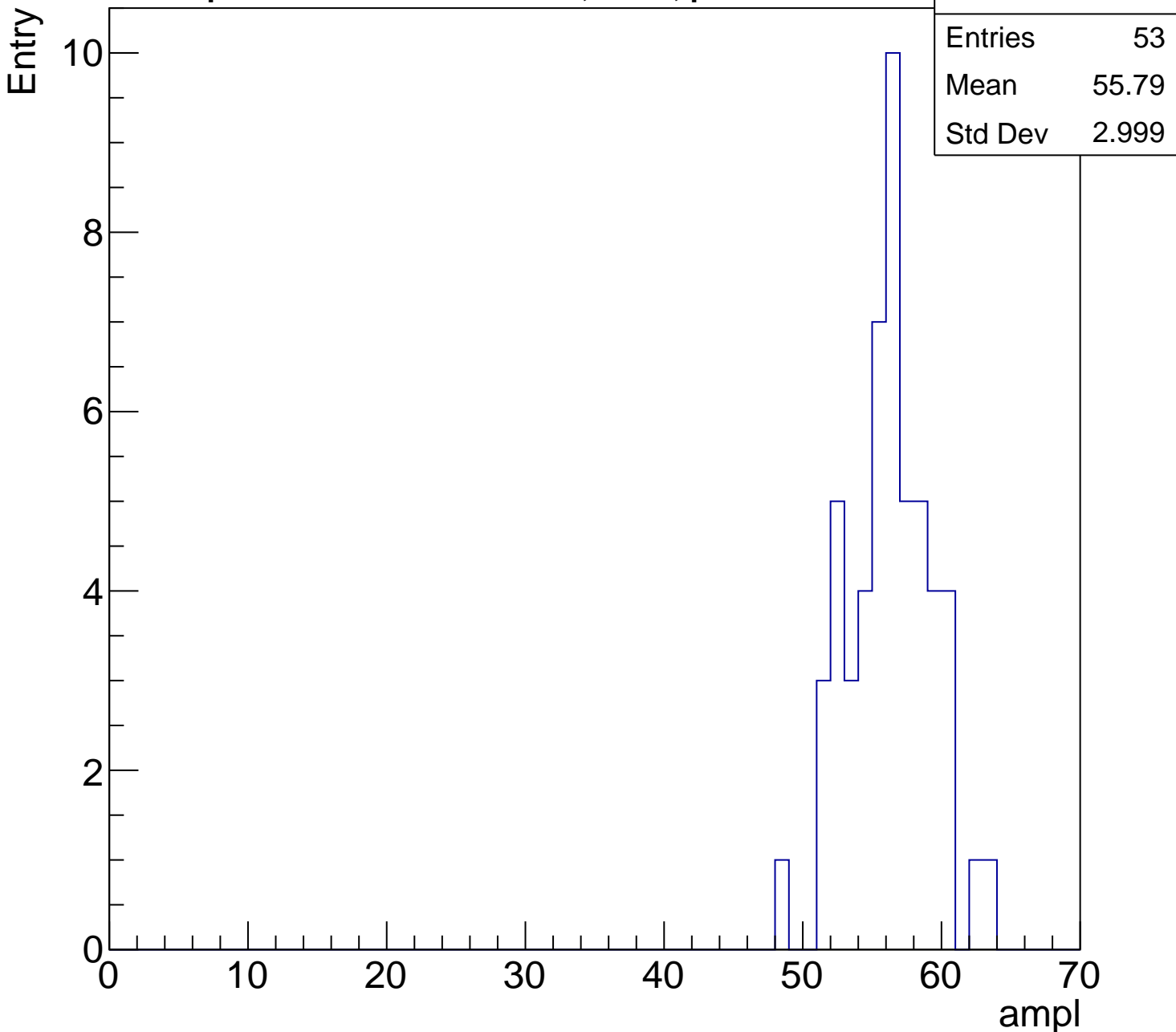
30

40

50

60

ampl

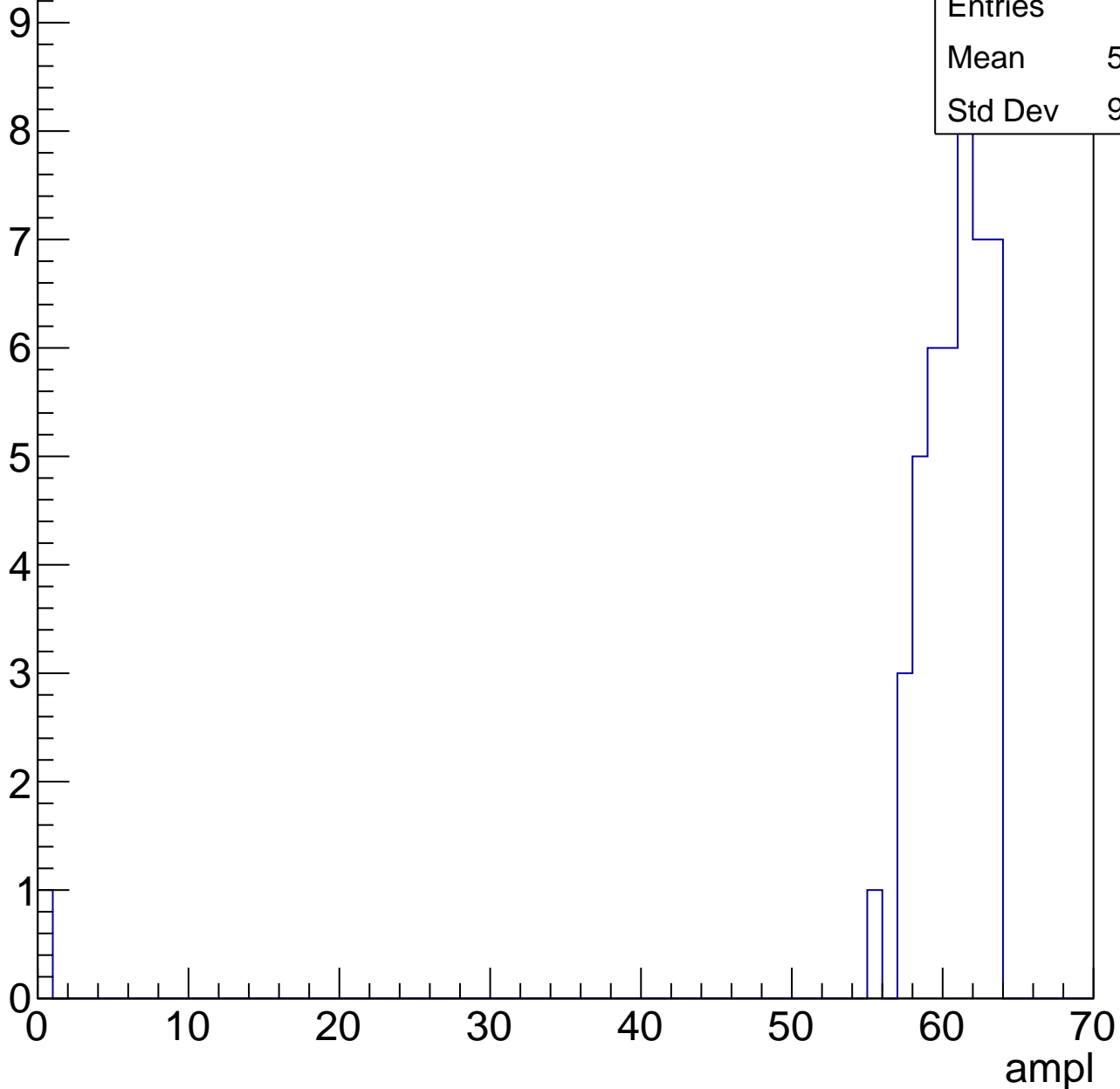


# B1L103S, U26-ch17, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	45
Mean	58.98
Std Dev	9.106



# B1L103S, U26-ch17, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	5
Mean	62.2
Std Dev	0.7483

ampl

0 10 20 30 40 50 60 70

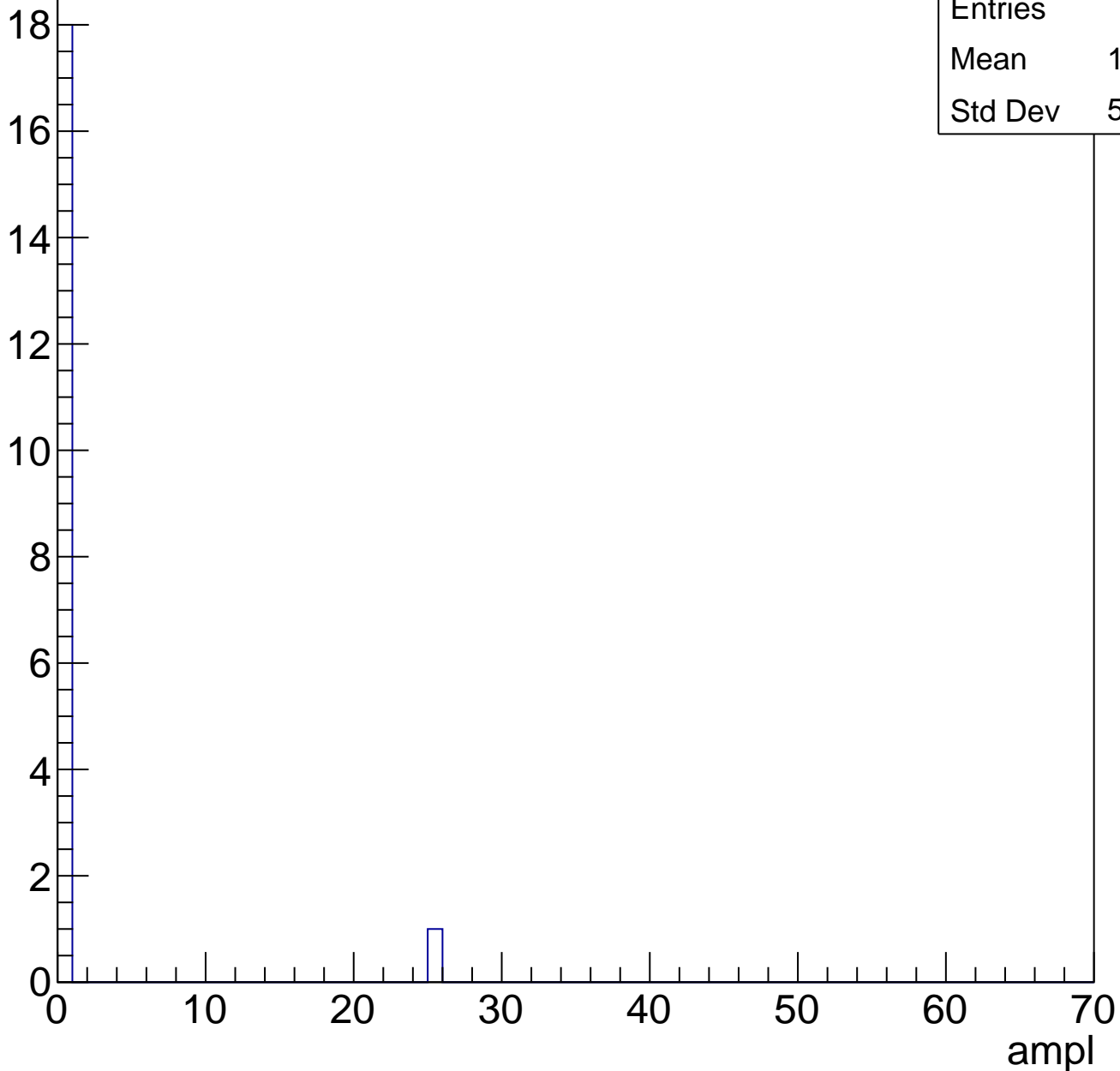


# B1L103S, U26-ch17, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	19
Mean	1.316
Std Dev	5.582

Entry



# B1L103S, U26-ch18, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	93
Mean	25.78
Std Dev	10.92

**Gaus mean : 30.5680**

**Gaus Width: 3.8054**

Entry

12

10

8

6

4

2

0

0

10

20

30

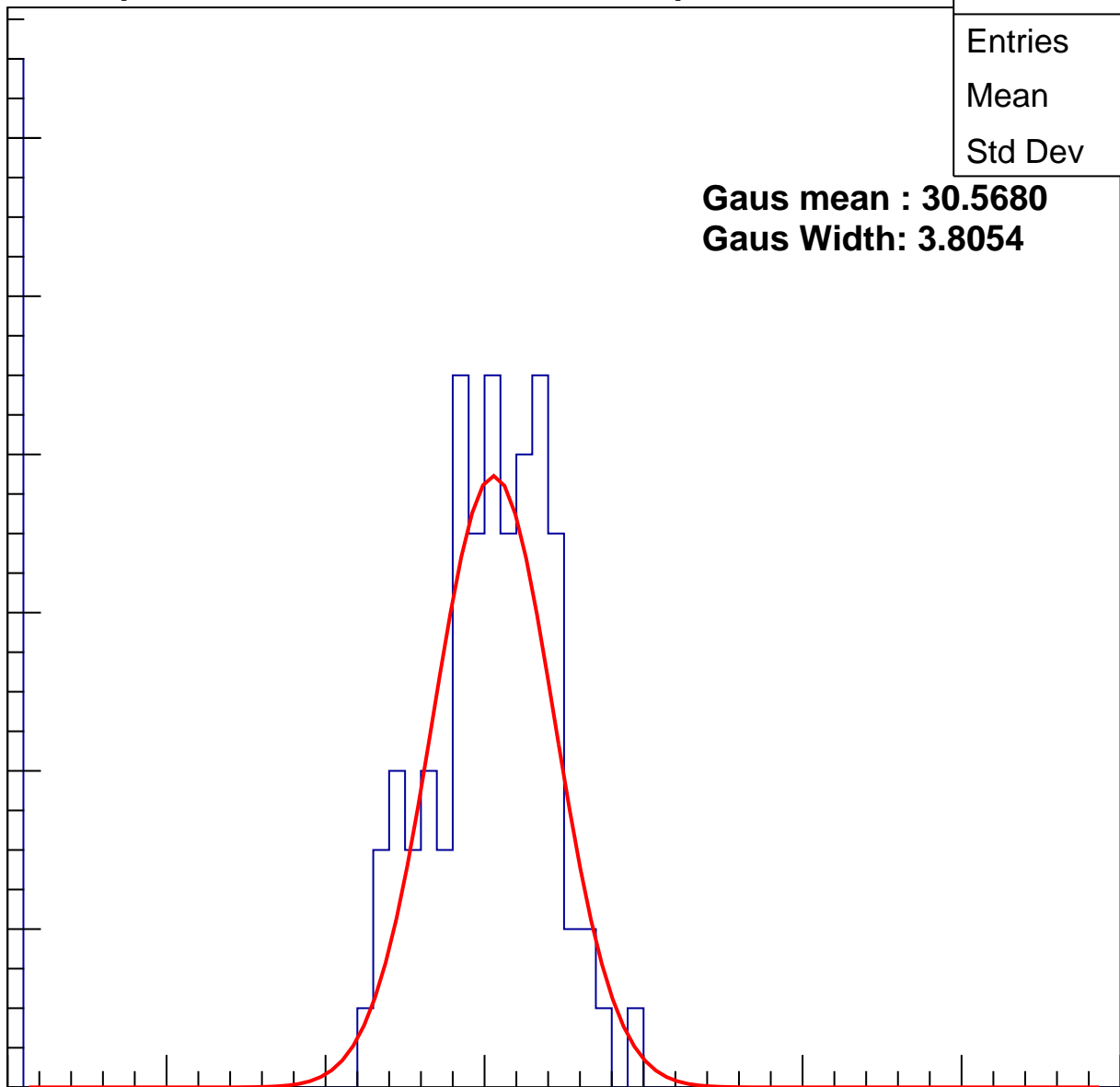
40

50

60

70

ampl



# B1L103S, U26-ch18, adc1

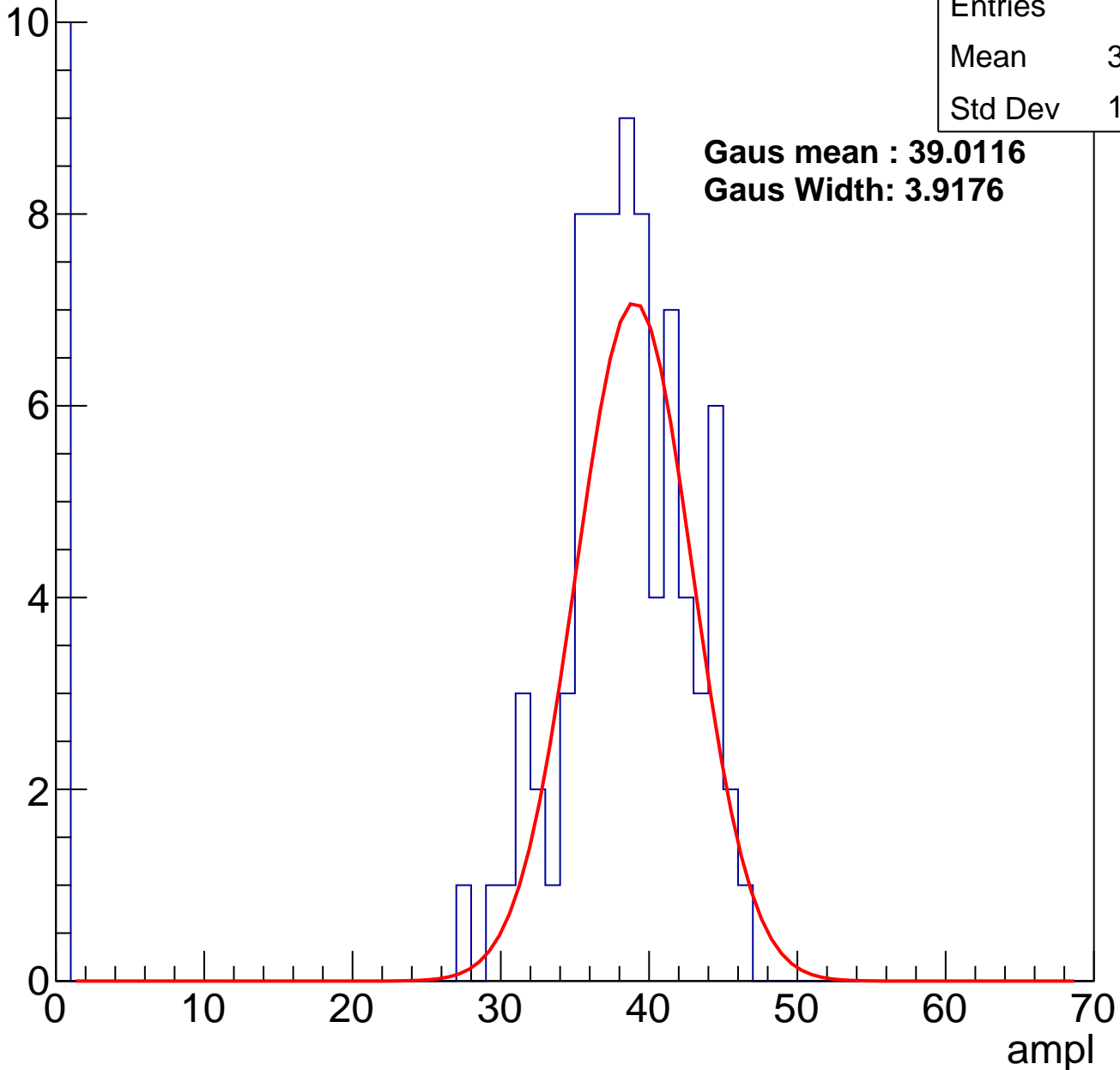
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	90
Mean	33.78
Std Dev	12.52

**Gaus mean : 39.0116**

**Gaus Width: 3.9176**

Entry



# B1L103S, U26-ch18, adc2

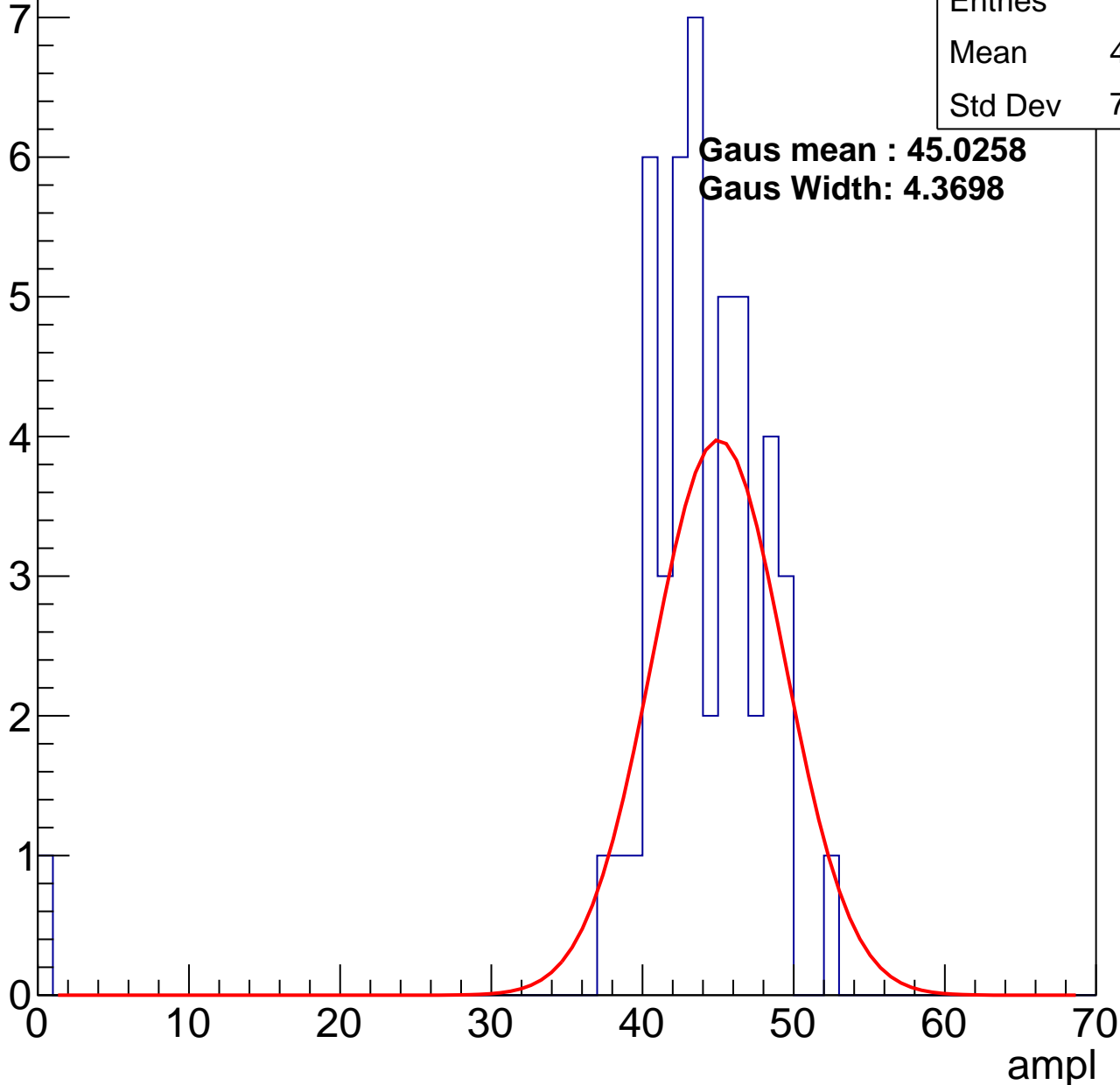
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	48
Mean	42.88
Std Dev	7.049

**Gaus mean : 45.0258**

**Gaus Width: 4.3698**

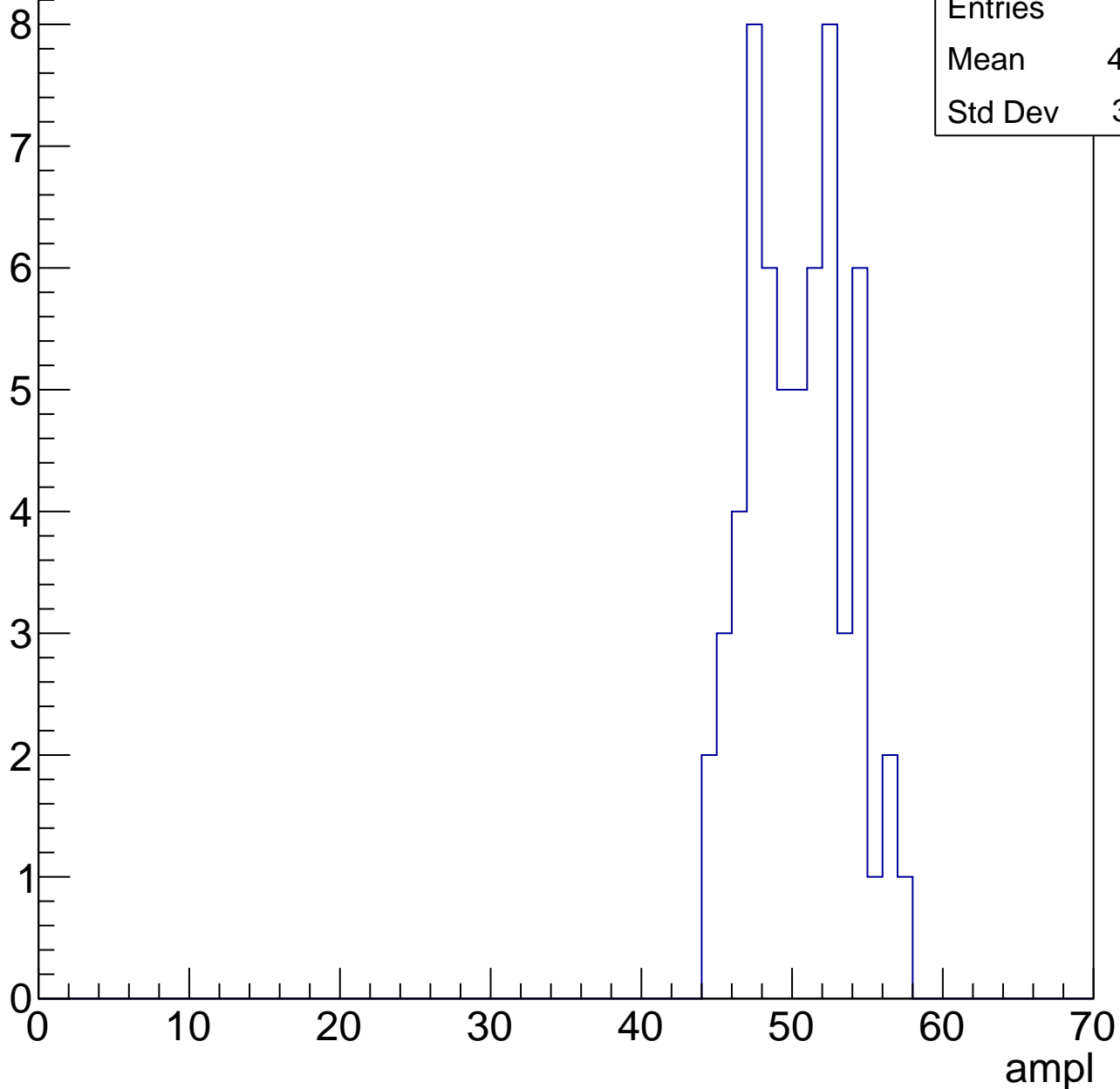


# B1L103S, U26-ch18, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

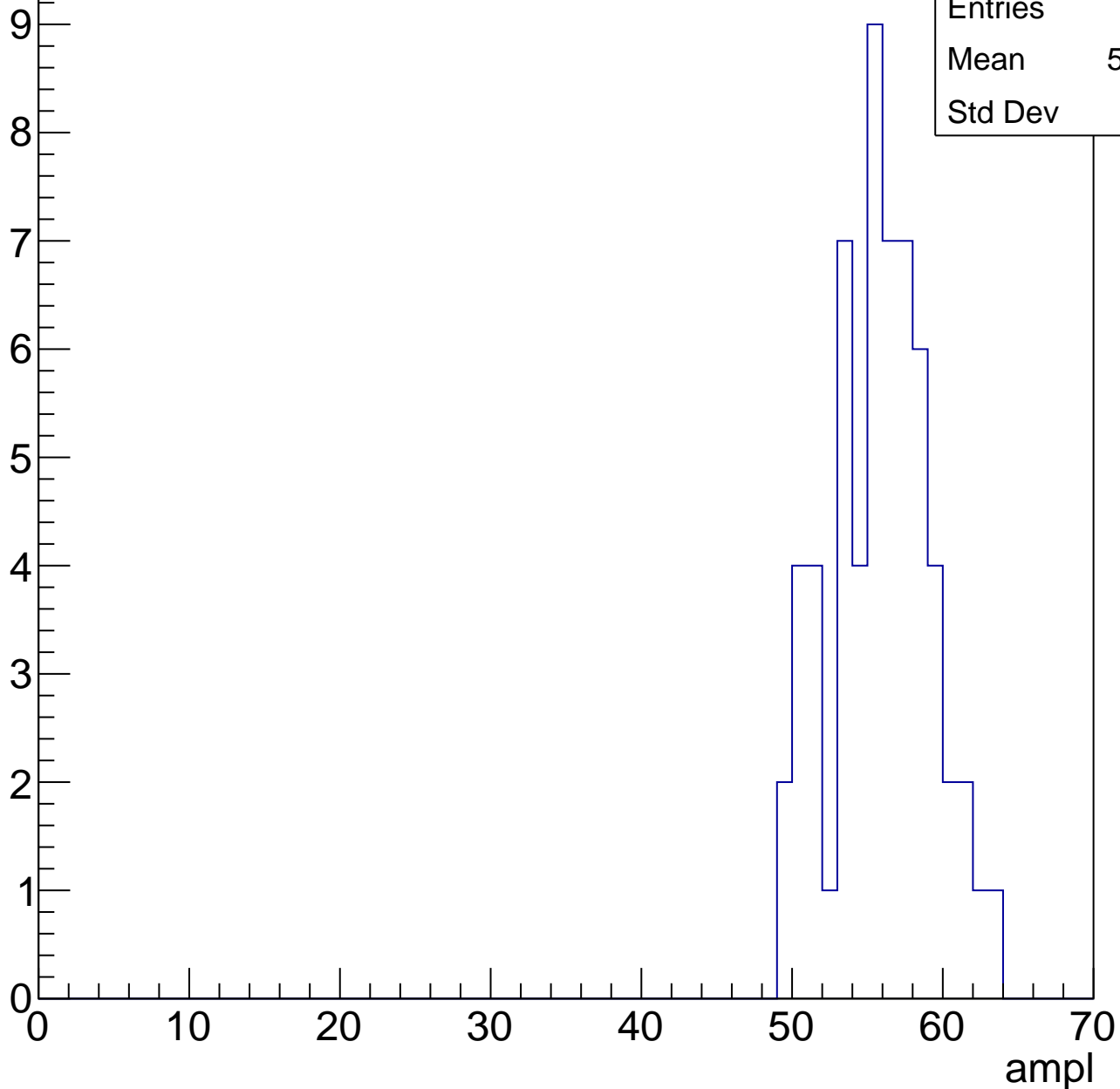
Entries	60
Mean	49.92
Std Dev	3.211



# B1L103S, U26-ch18, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

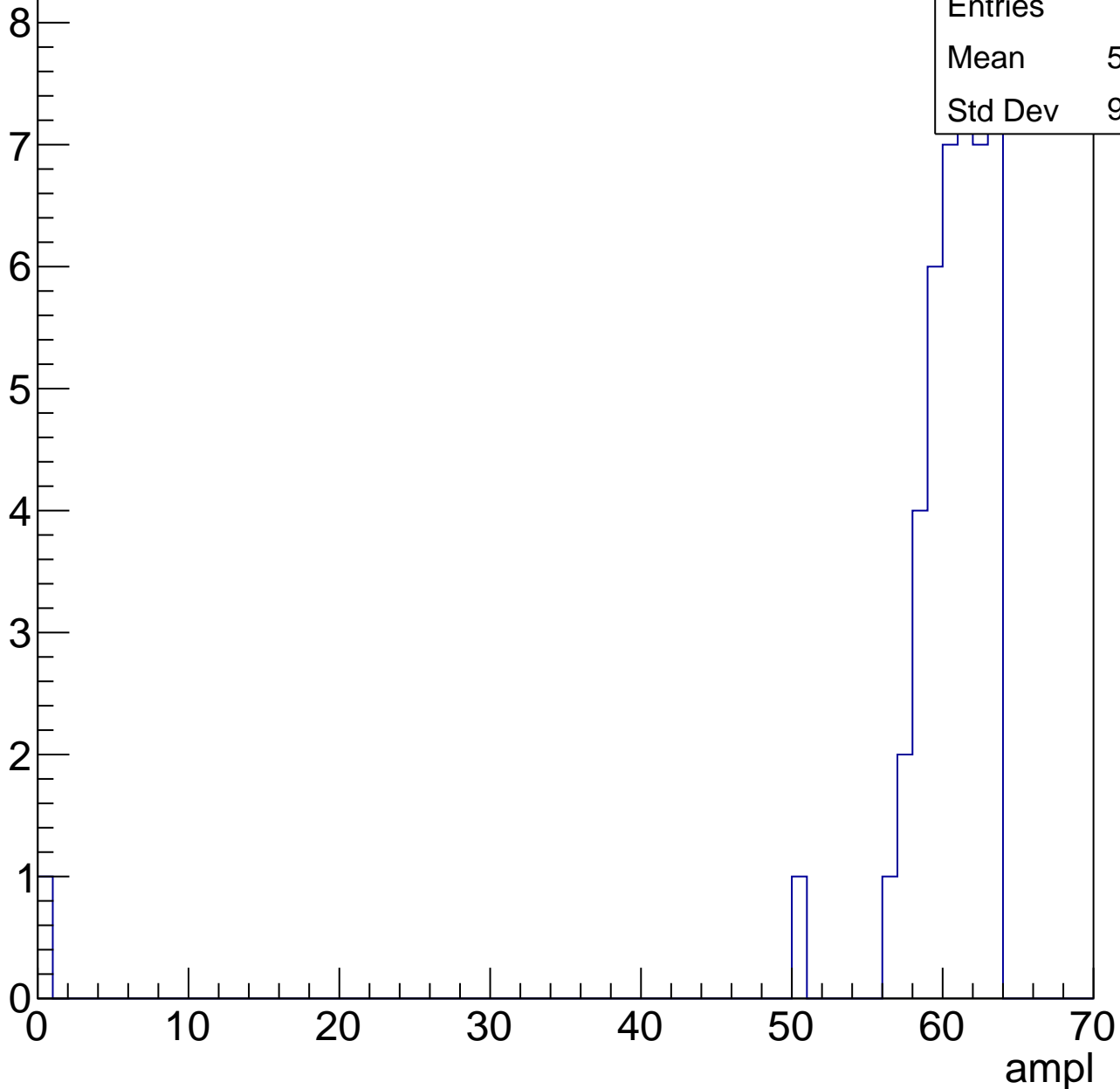


# B1L103S, U26-ch18, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

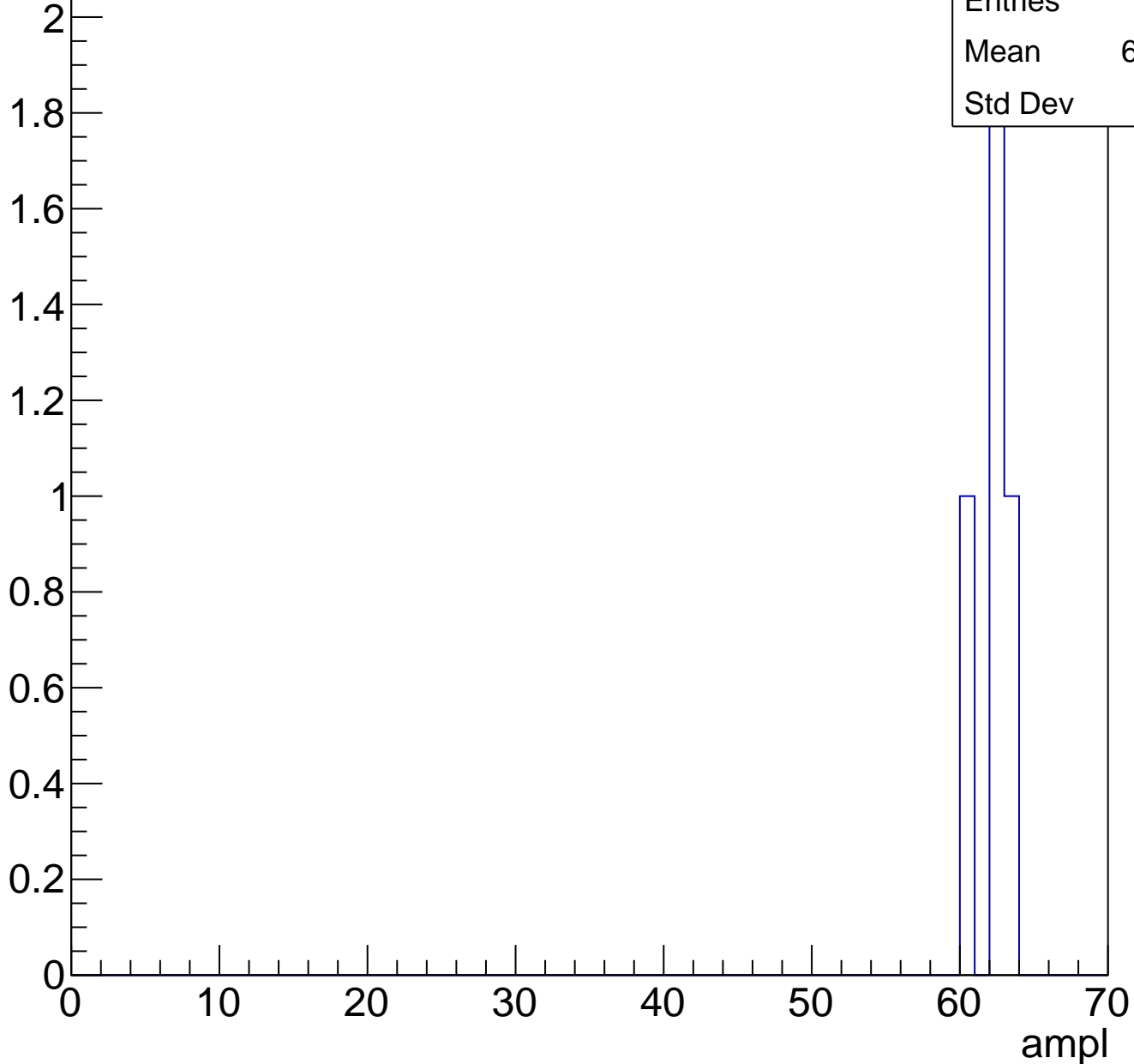
Entries	45
Mean	58.93
Std Dev	9.205



# B1L103S, U26-ch18, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry





# B1L103S, U26-ch18, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

18  
16  
14  
12  
10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

Entries	19
Mean	0
Std Dev	0

# B1L103S, U26-ch19, adc0

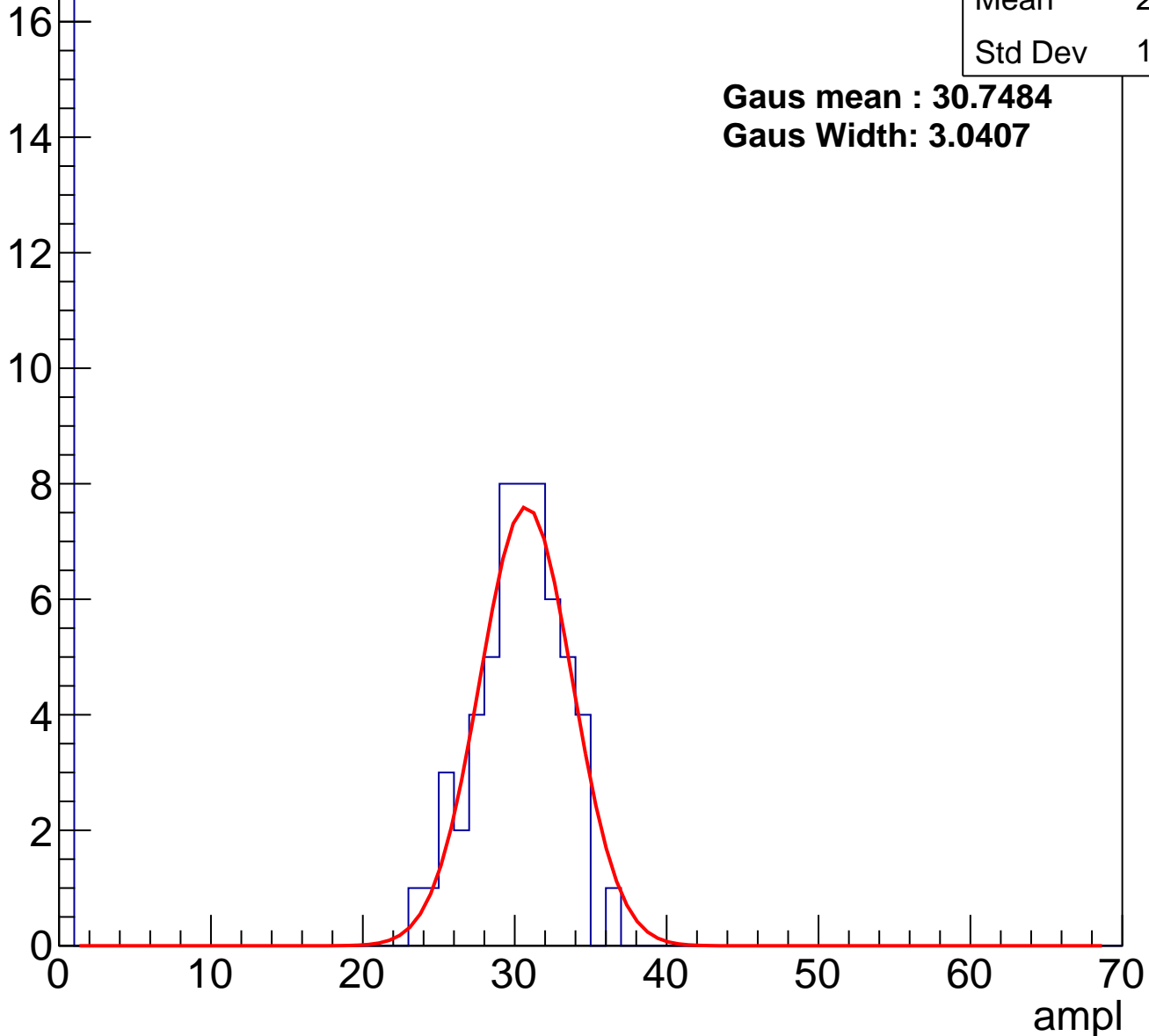
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	73
Mean	22.89
Std Dev	12.84

**Gaus mean : 30.7484**

**Gaus Width: 3.0407**

Entry



# B1L103S, U26-ch19, adc1

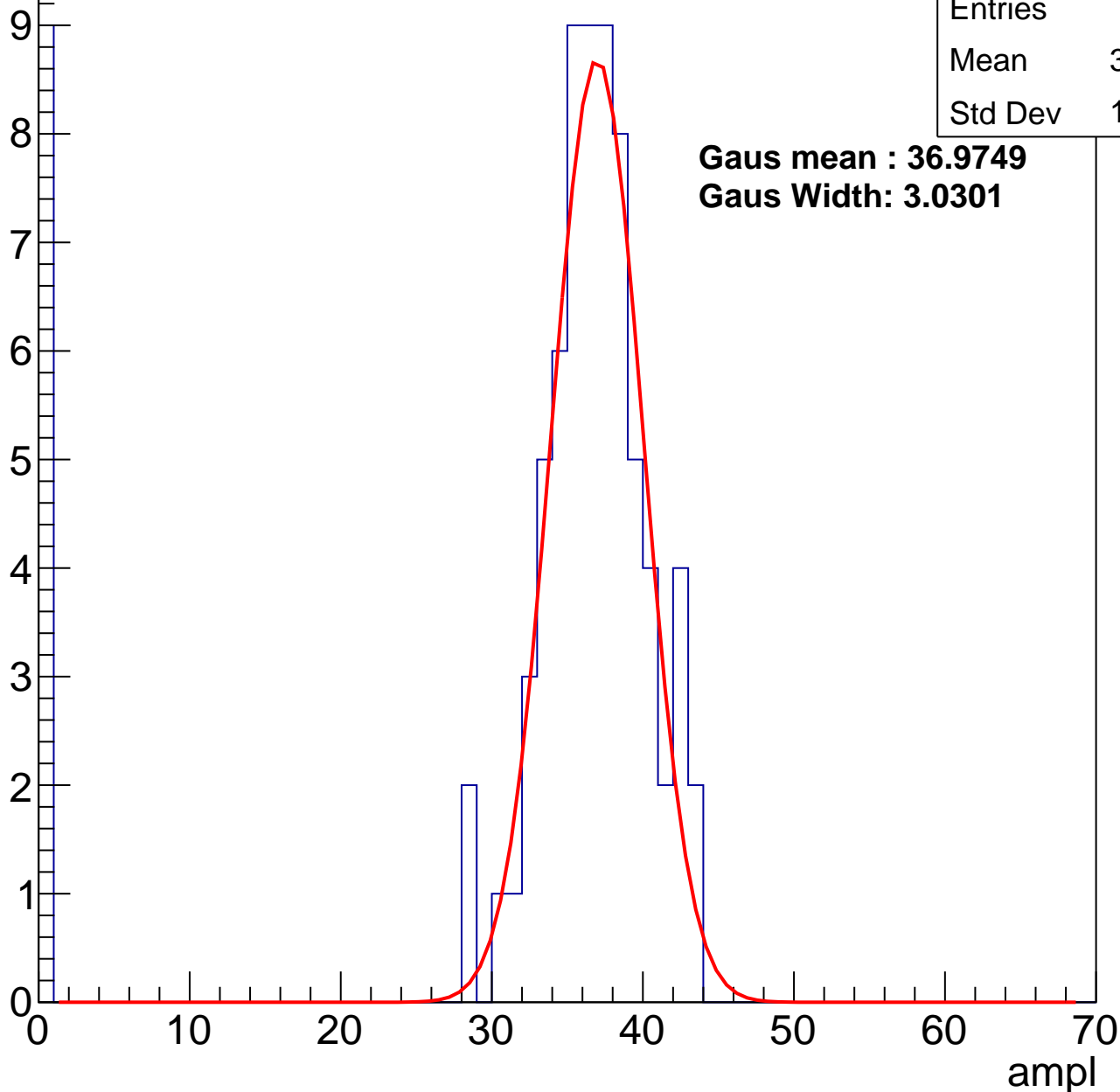
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	79
Mean	32.27
Std Dev	11.97

**Gaus mean : 36.9749**

**Gaus Width: 3.0301**



# B1L103S, U26-ch19, adc2

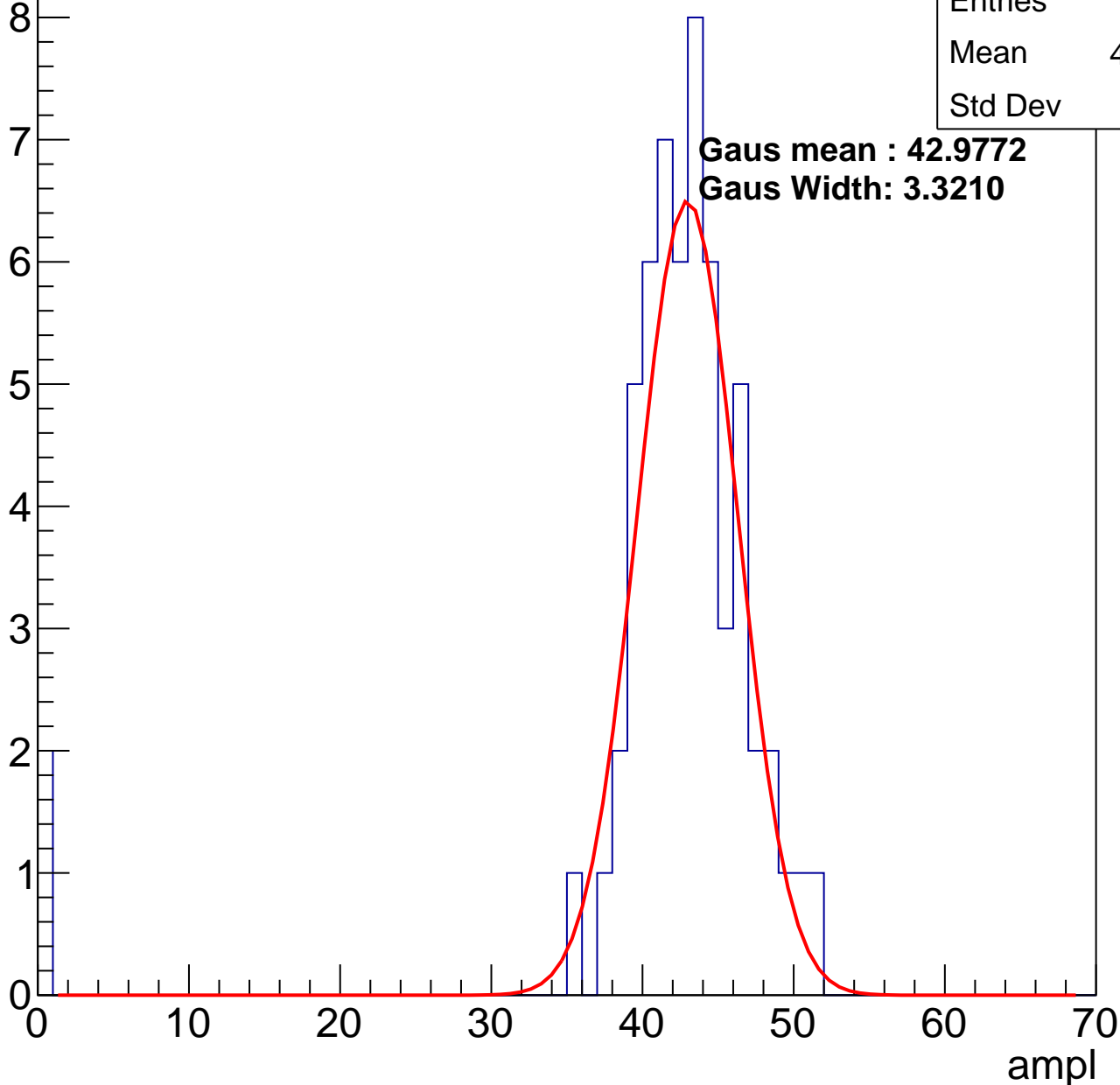
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	59
Mean	41.27
Std Dev	8.37

**Gaus mean : 42.9772**

**Gaus Width: 3.3210**

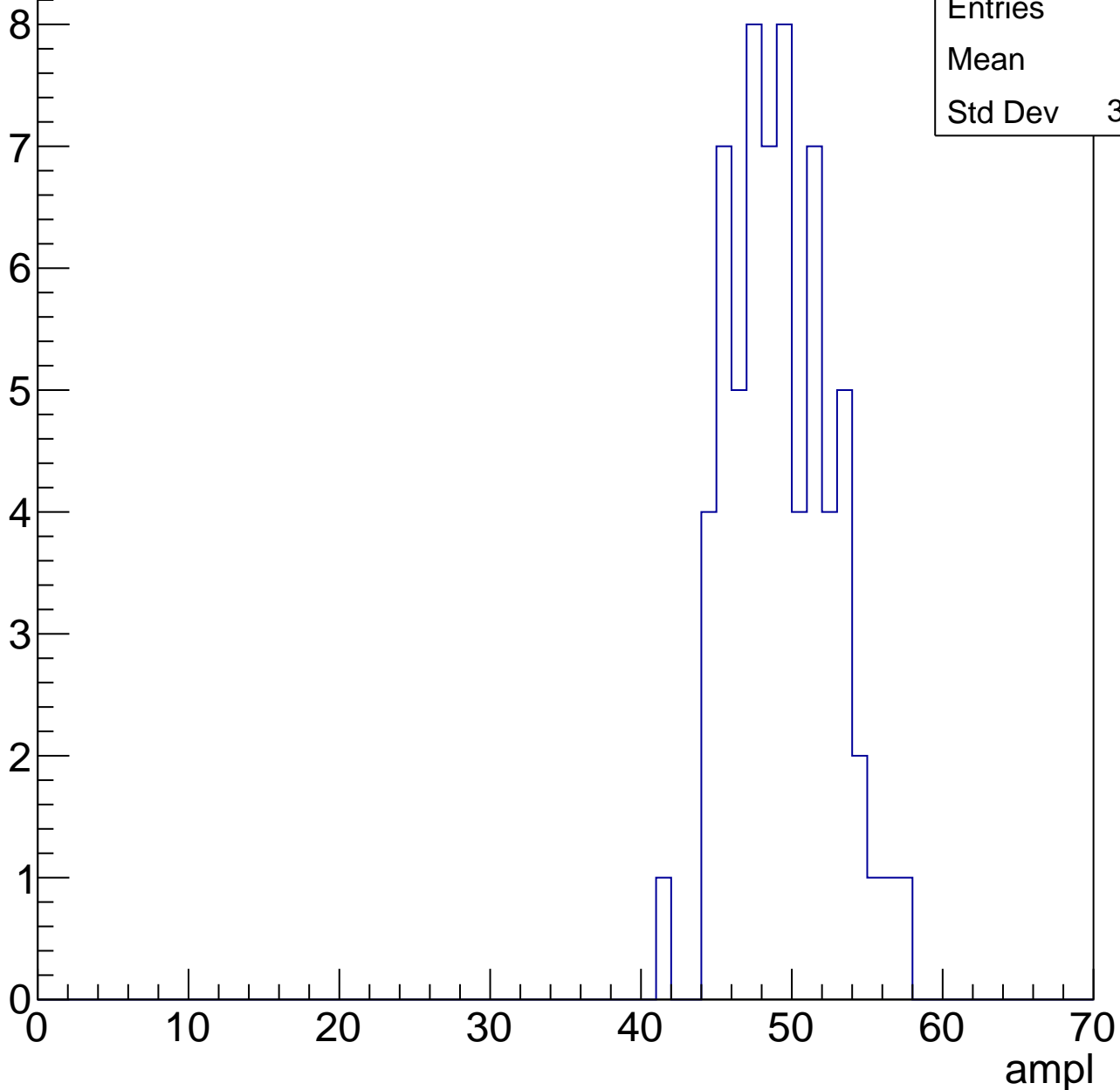


# B1L103S, U26-ch19, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

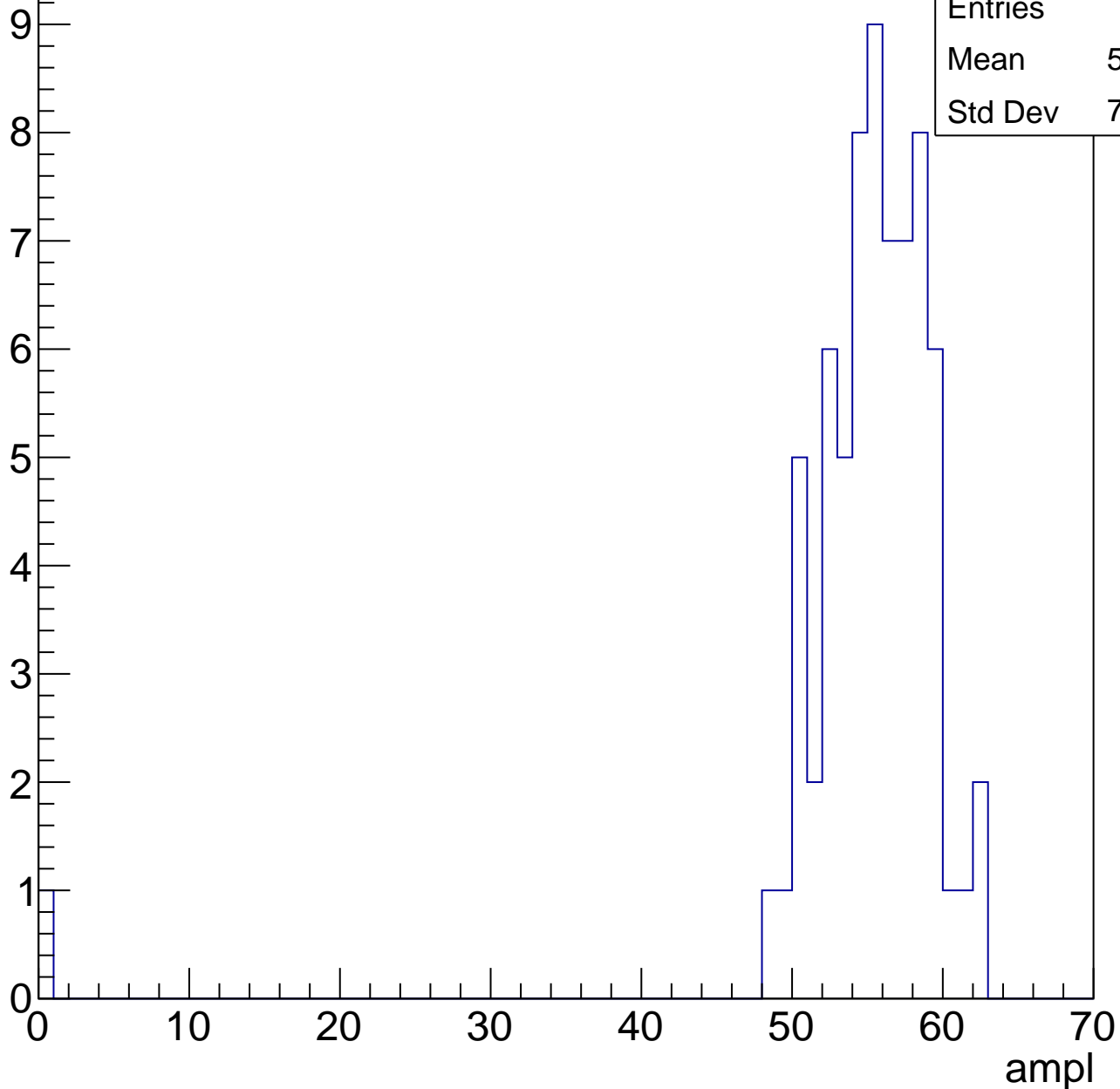
Entries	65
Mean	48.8
Std Dev	3.292



# B1L103S, U26-ch19, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

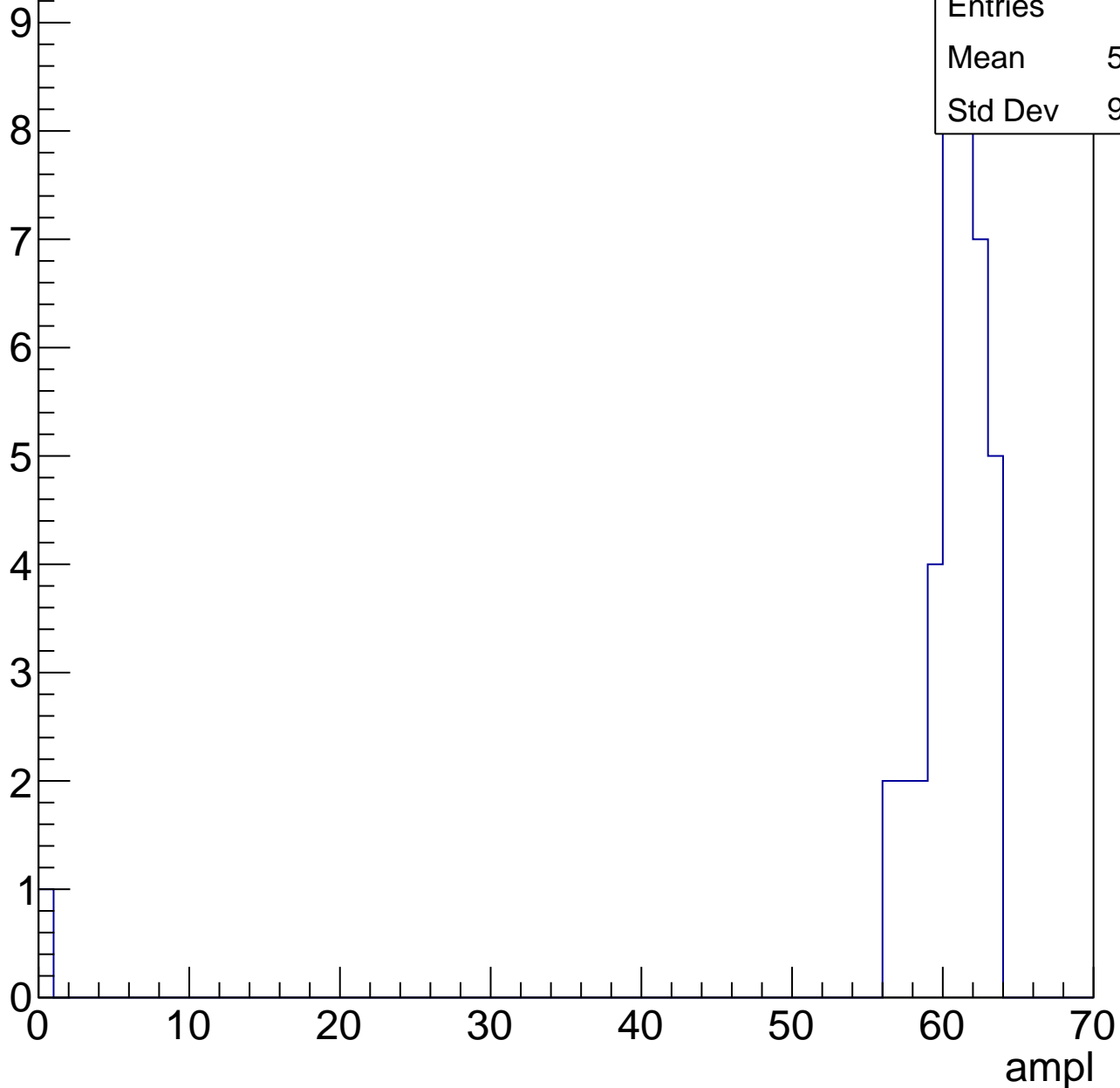
Entry



# B1L103S, U26-ch19, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

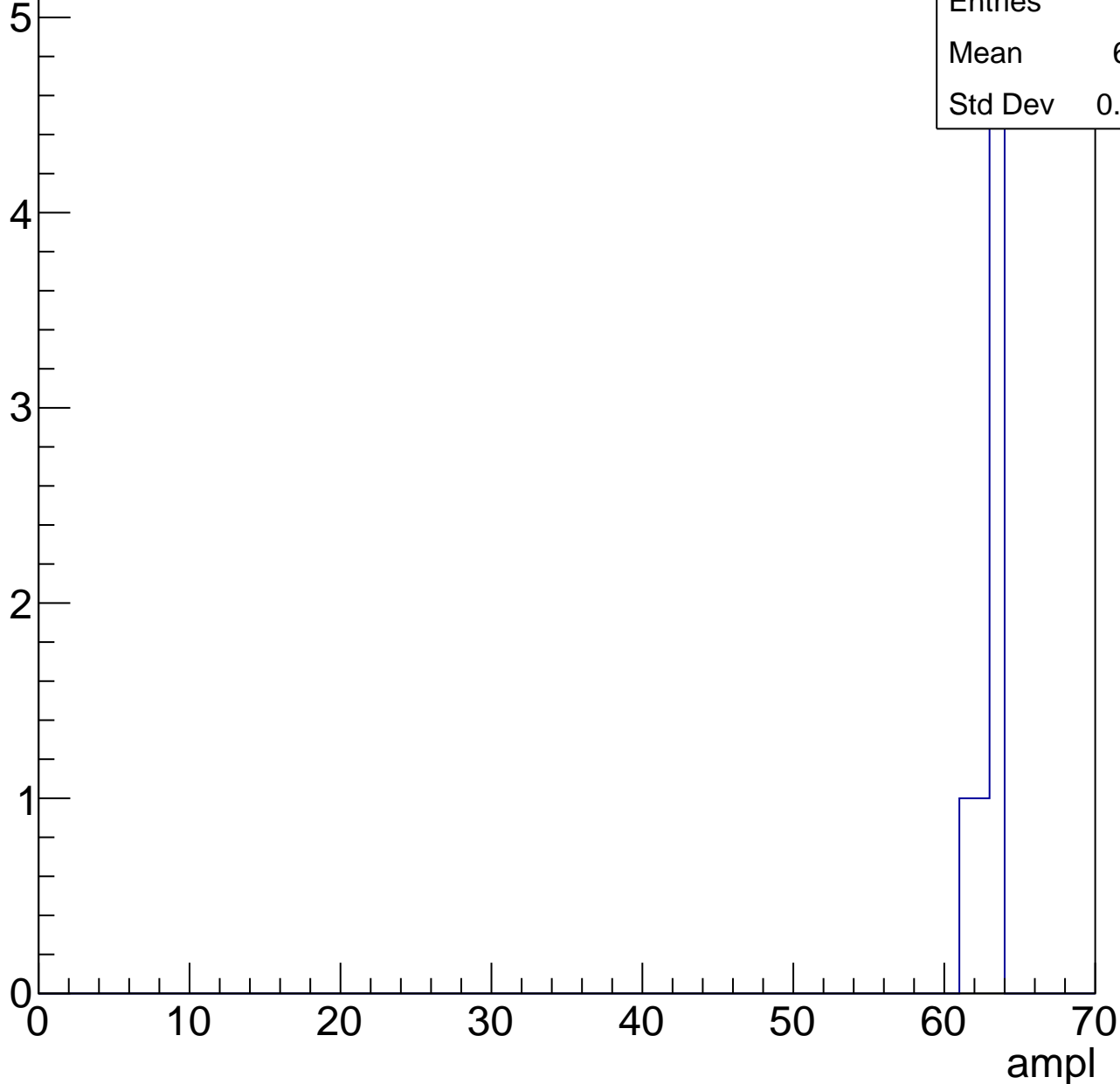


# B1L103S, U26-ch19, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	7
Mean	62.57
Std Dev	0.7284





# B1L103S, U26-ch19, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



Entries	18
Mean	0
Std Dev	0

# B1L103S, U26-ch20, adc0

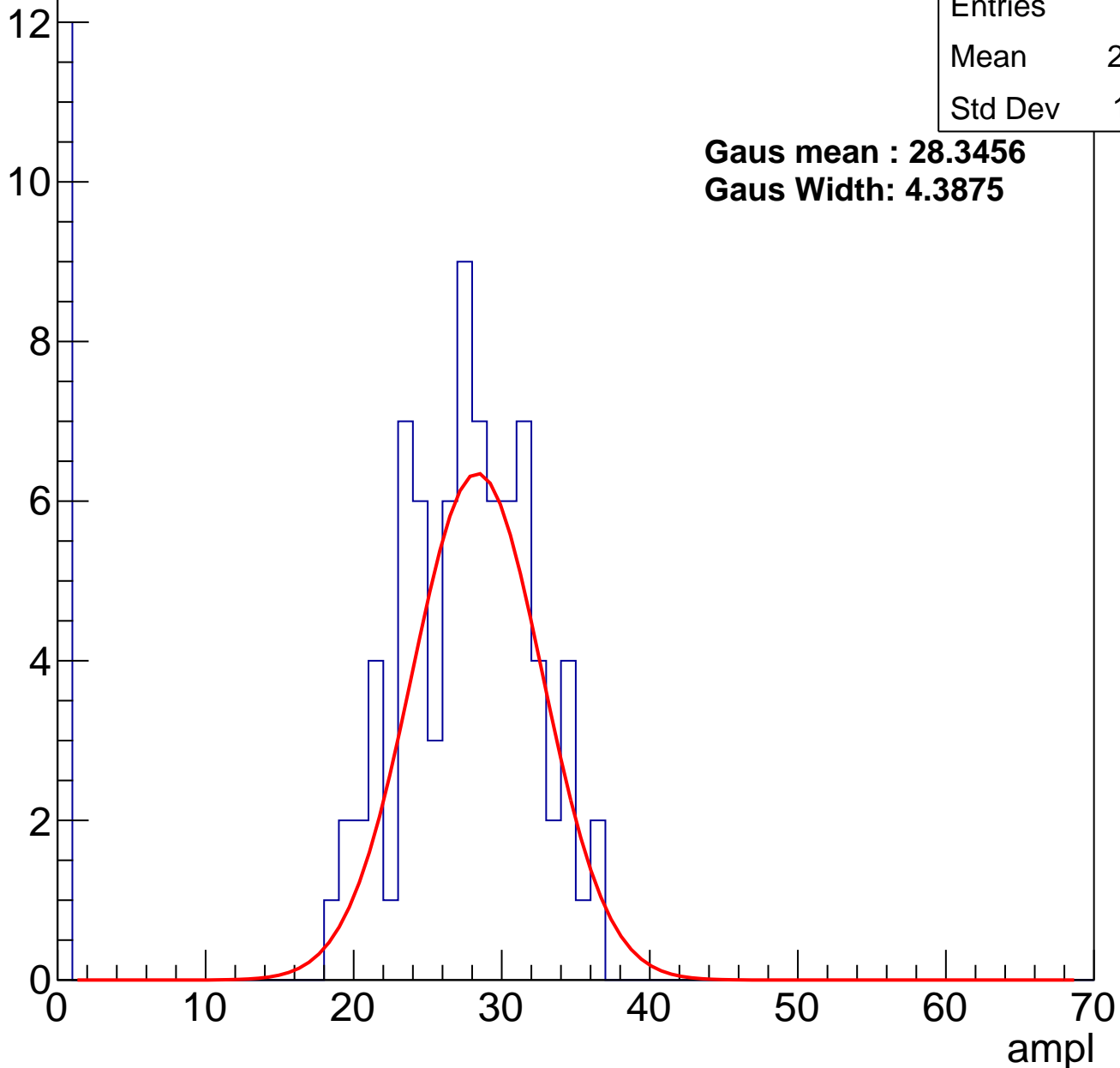
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	92
Mean	23.75
Std Dev	10.01

**Gaus mean : 28.3456**

**Gaus Width: 4.3875**

Entry



# B1L103S, U26-ch20, adc1

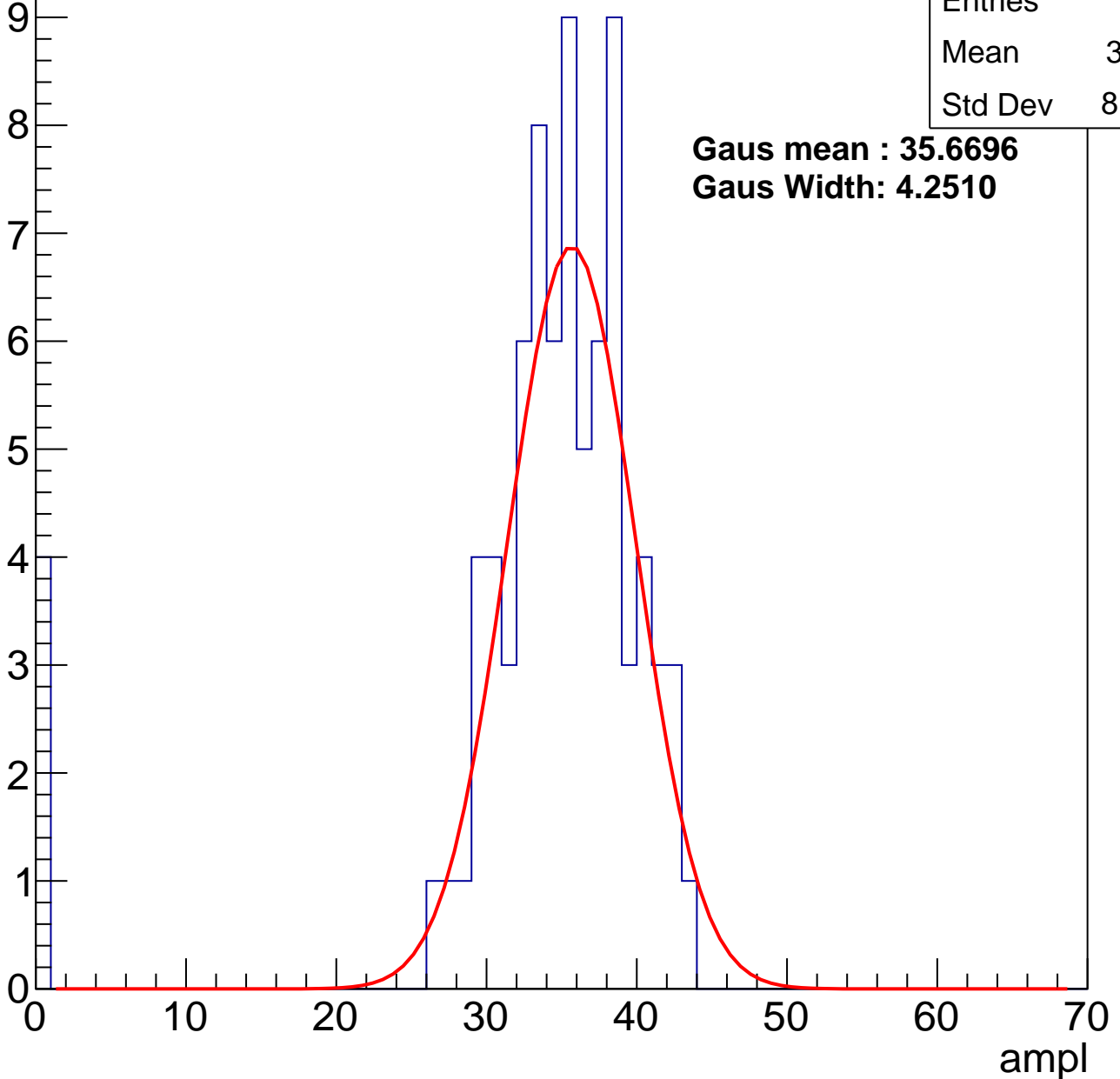
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	81
Mean	33.31
Std Dev	8.479

**Gaus mean : 35.6696**

**Gaus Width: 4.2510**



# B1L103S, U26-ch20, adc2

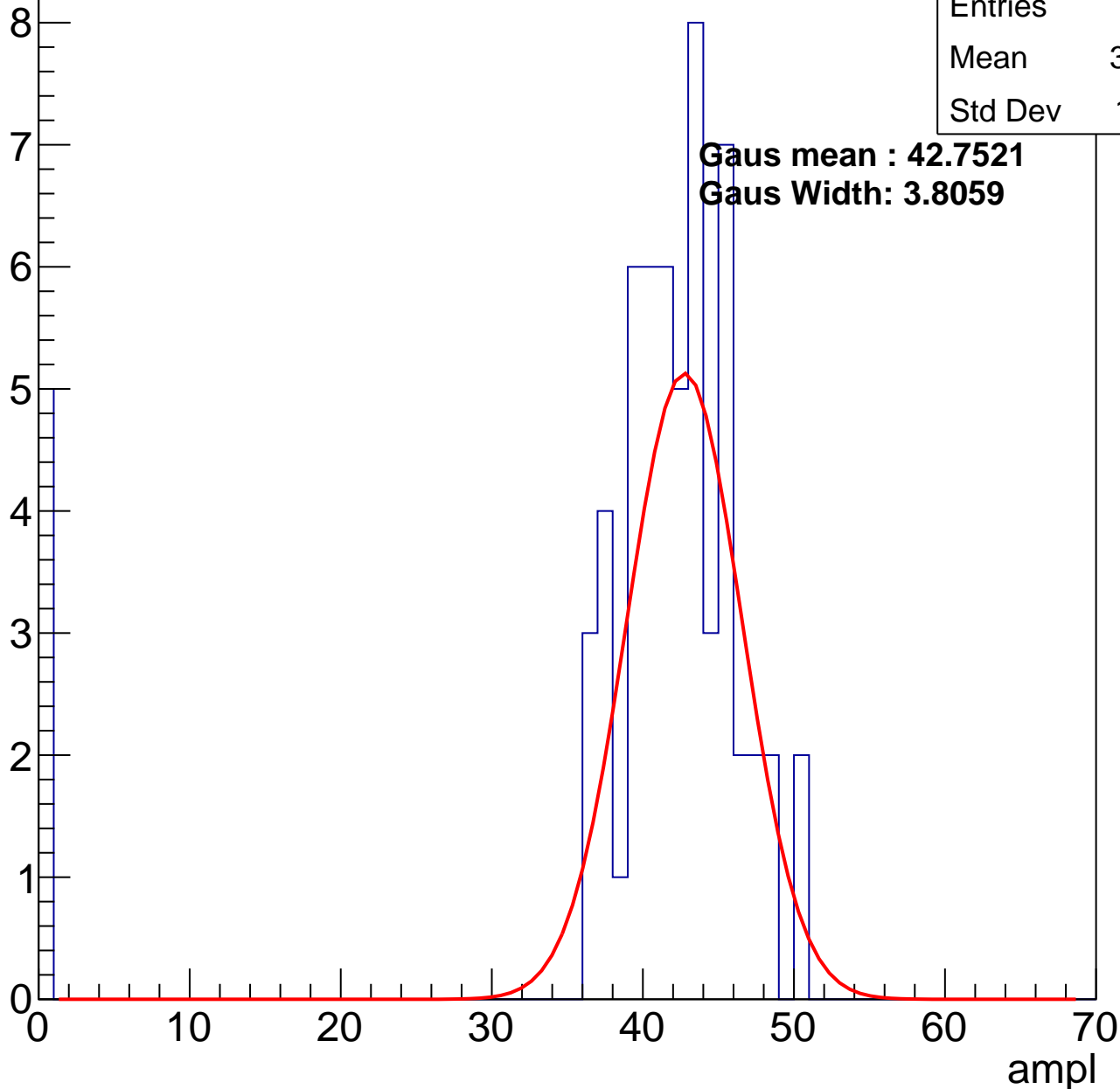
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	62
Mean	38.66
Std Dev	11.91

**Gaus mean : 42.7521**

**Gaus Width: 3.8059**

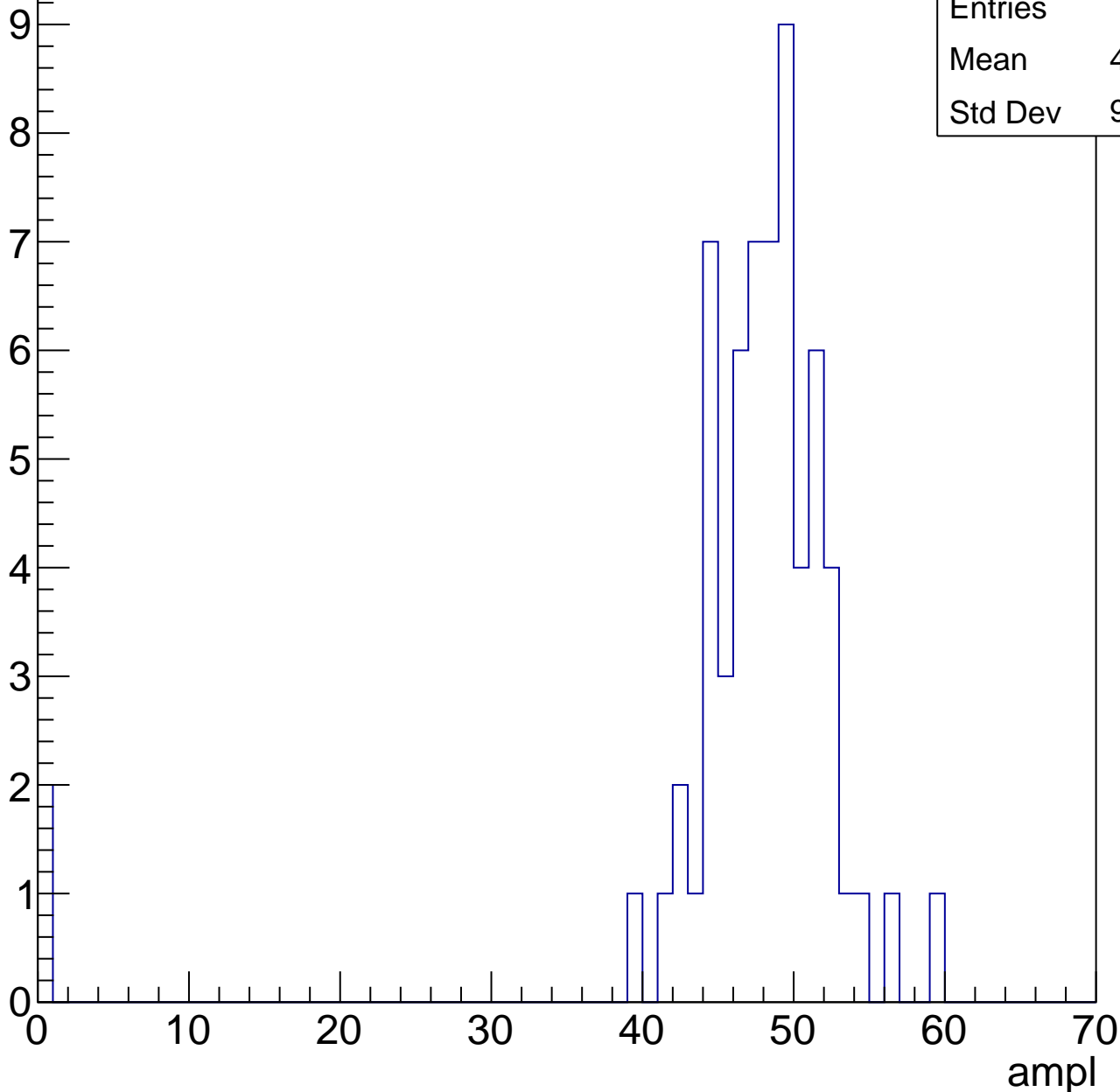


# B1L103S, U26-ch20, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	64
Mean	46.38
Std Dev	9.036

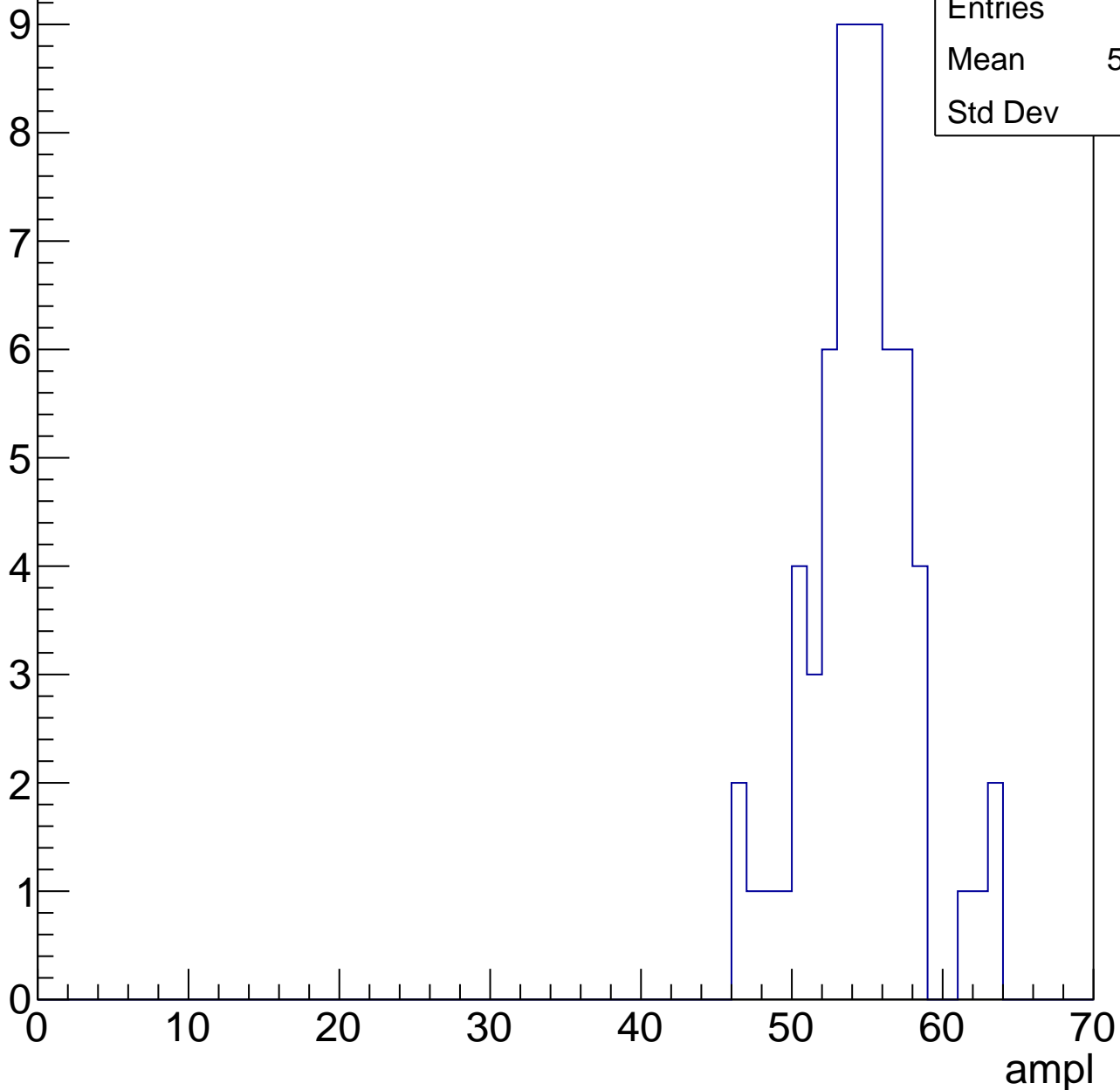


# B1L103S, U26-ch20, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	65
Mean	54.12
Std Dev	3.48

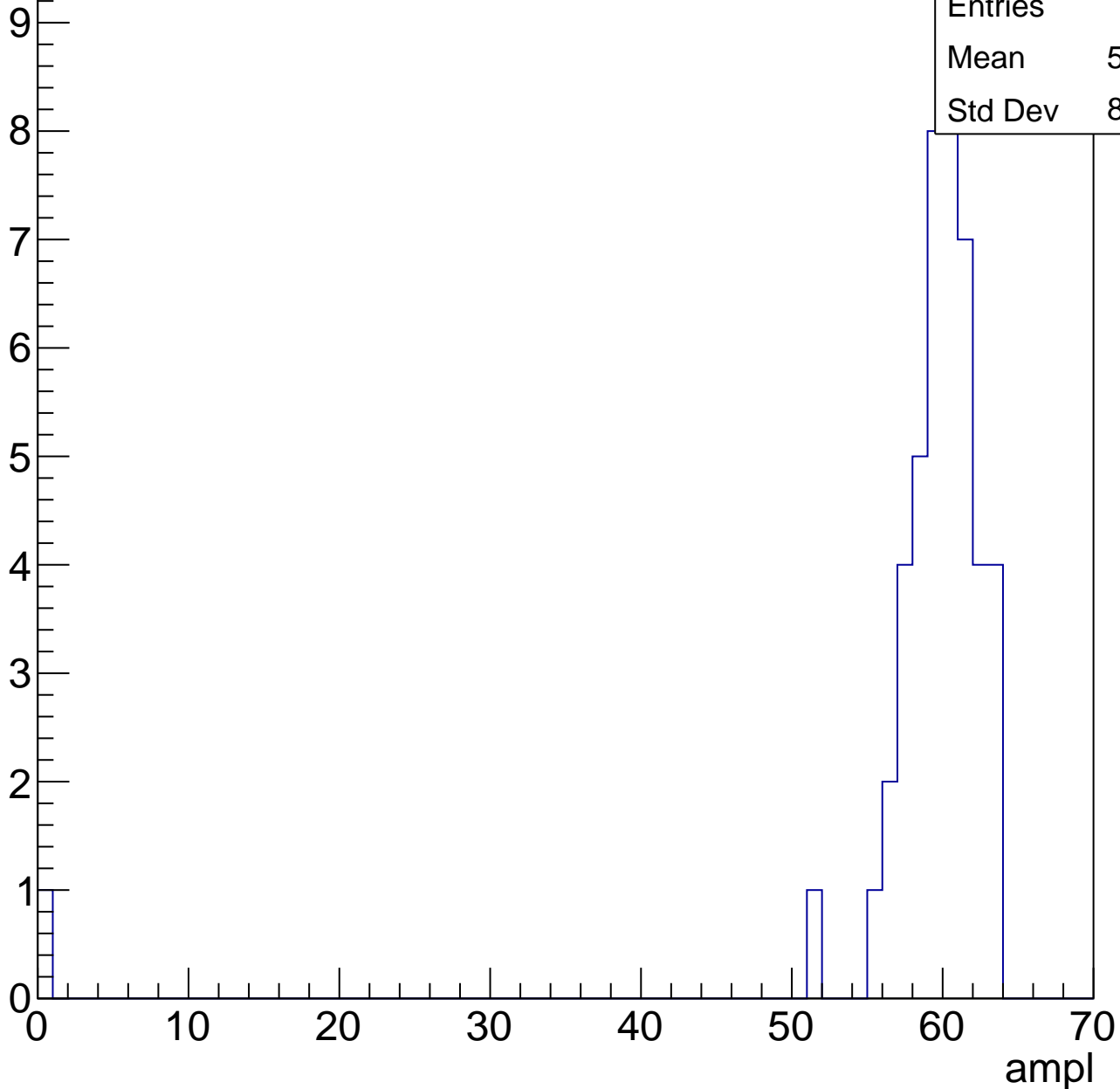


# B1L103S, U26-ch20, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	46
Mean	58.15
Std Dev	8.973

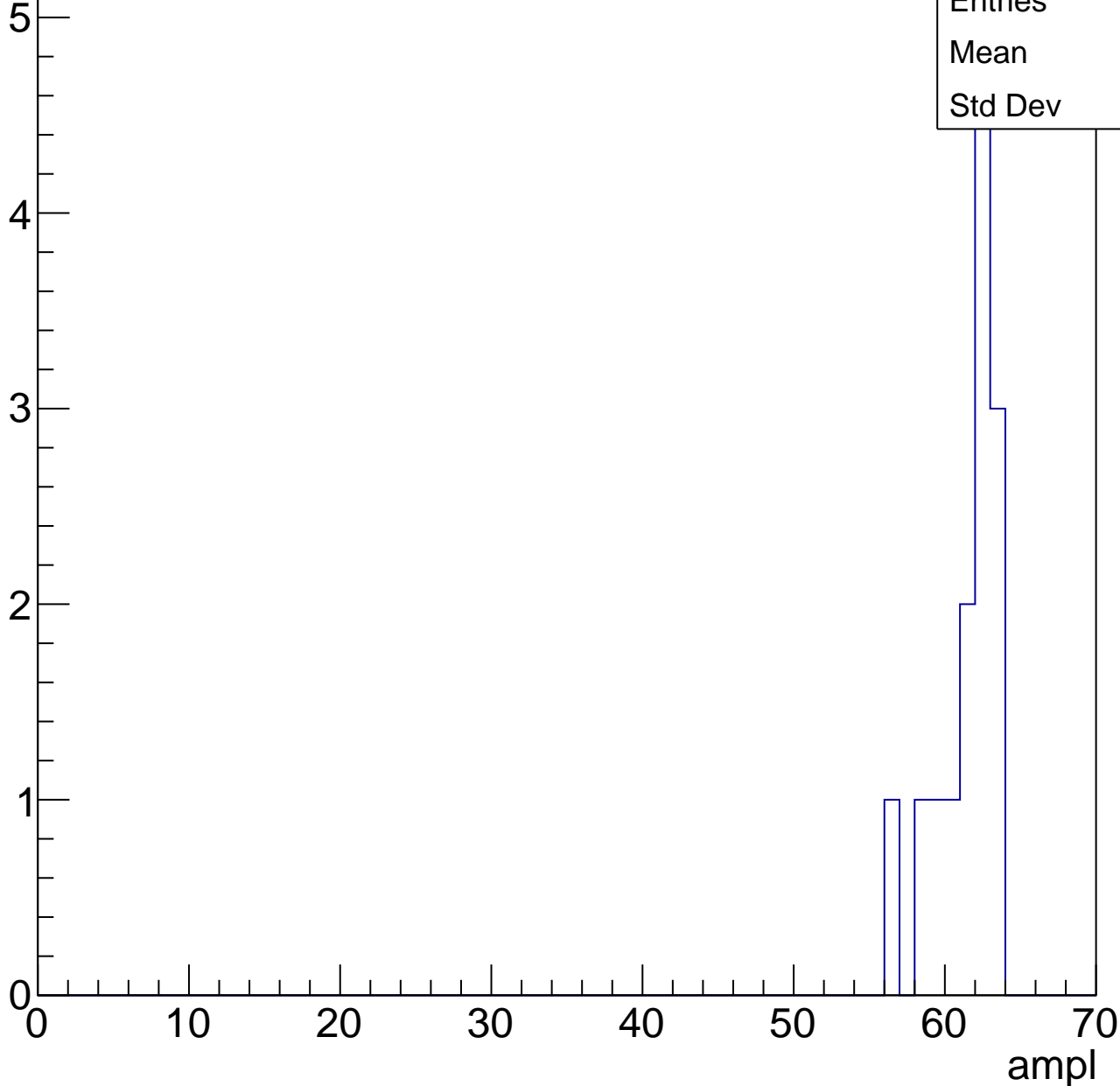


# B1L103S, U26-ch20, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	14
Mean	61
Std Dev	2





# B1L103S, U26-ch20, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	20
Mean	3.15
Std Dev	13.73

Entry



# B1L103S, U26-ch21, adc0

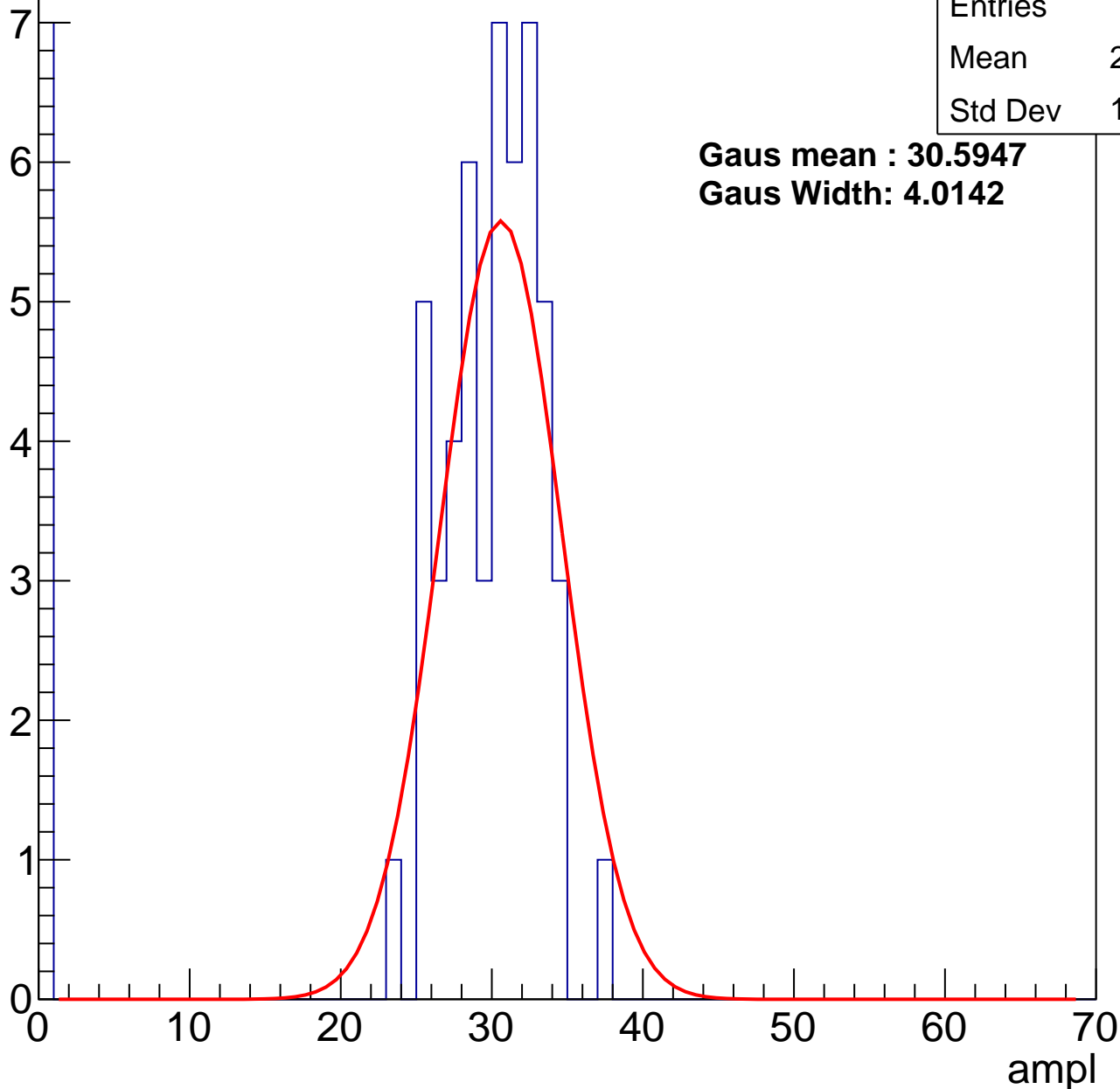
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	58
Mean	26.09
Std Dev	10.06

**Gaus mean : 30.5947**

**Gaus Width: 4.0142**



# B1L103S, U26-ch21, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	75
Mean	35.95
Std Dev	3.2

**Gaus mean : 36.3122**

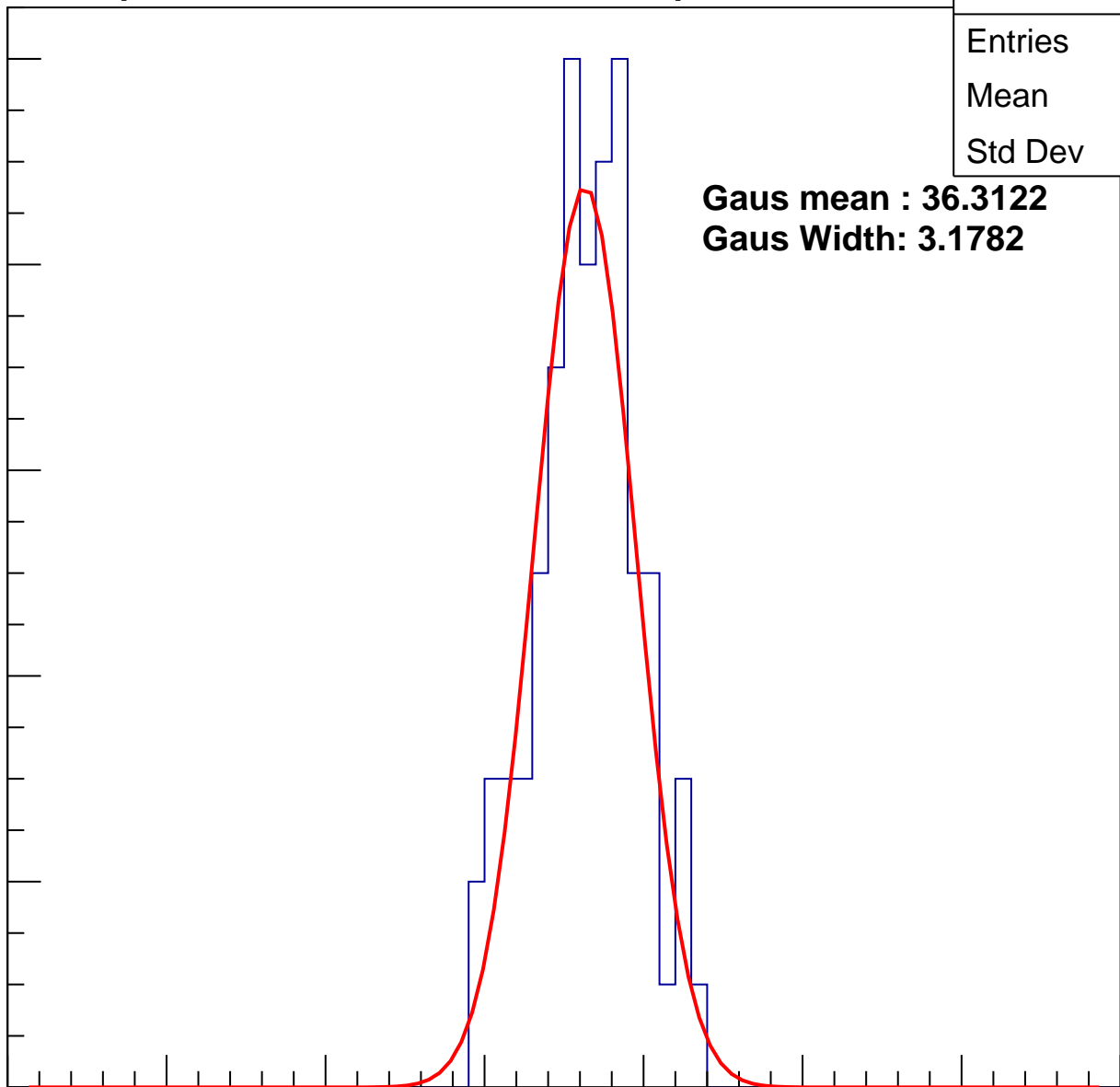
**Gaus Width: 3.1782**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U26-ch21, adc2

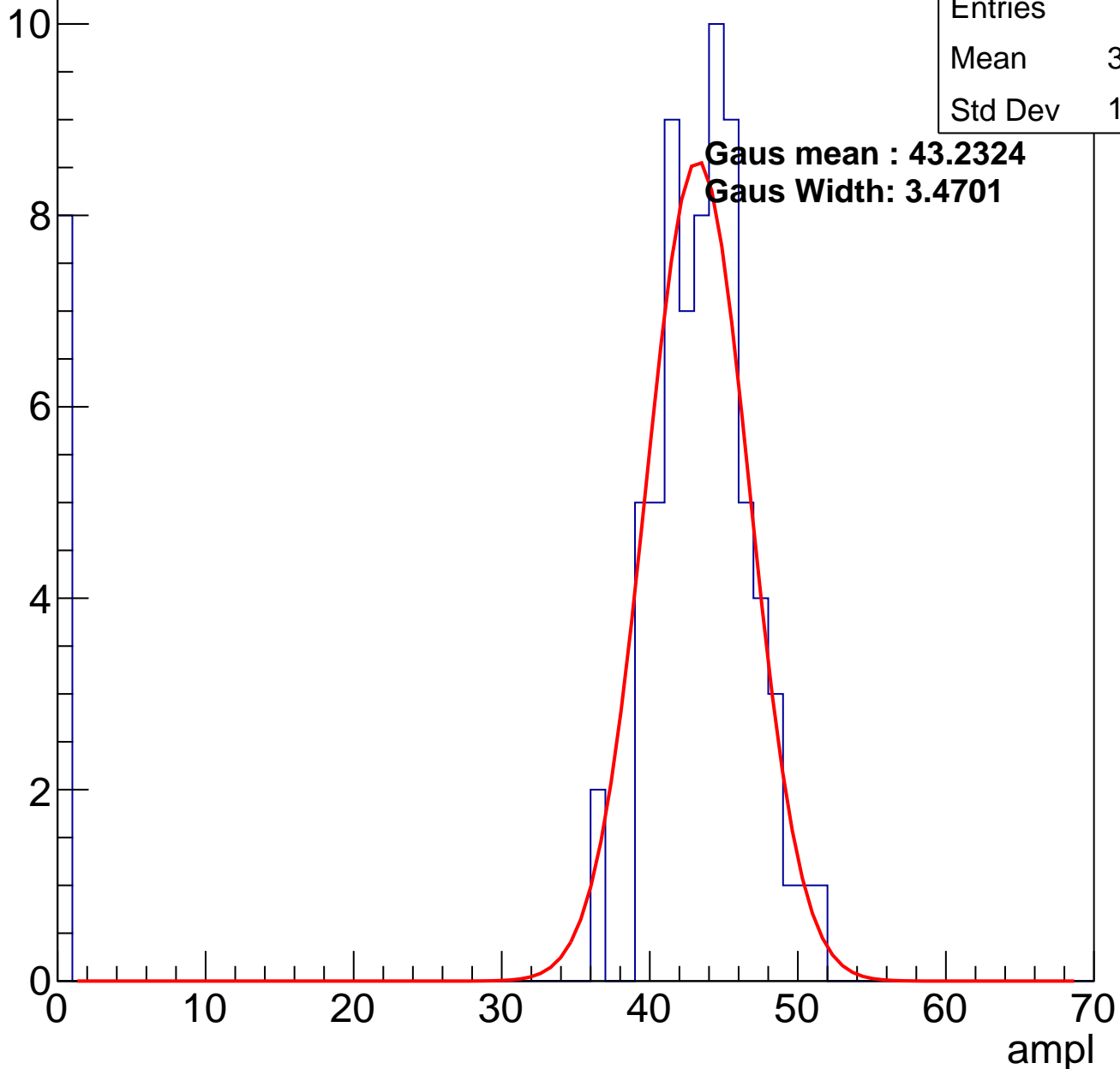
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	78
Mean	38.86
Std Dev	13.44

**Gaus mean : 43.2324**

**Gaus Width: 3.4701**

Entry

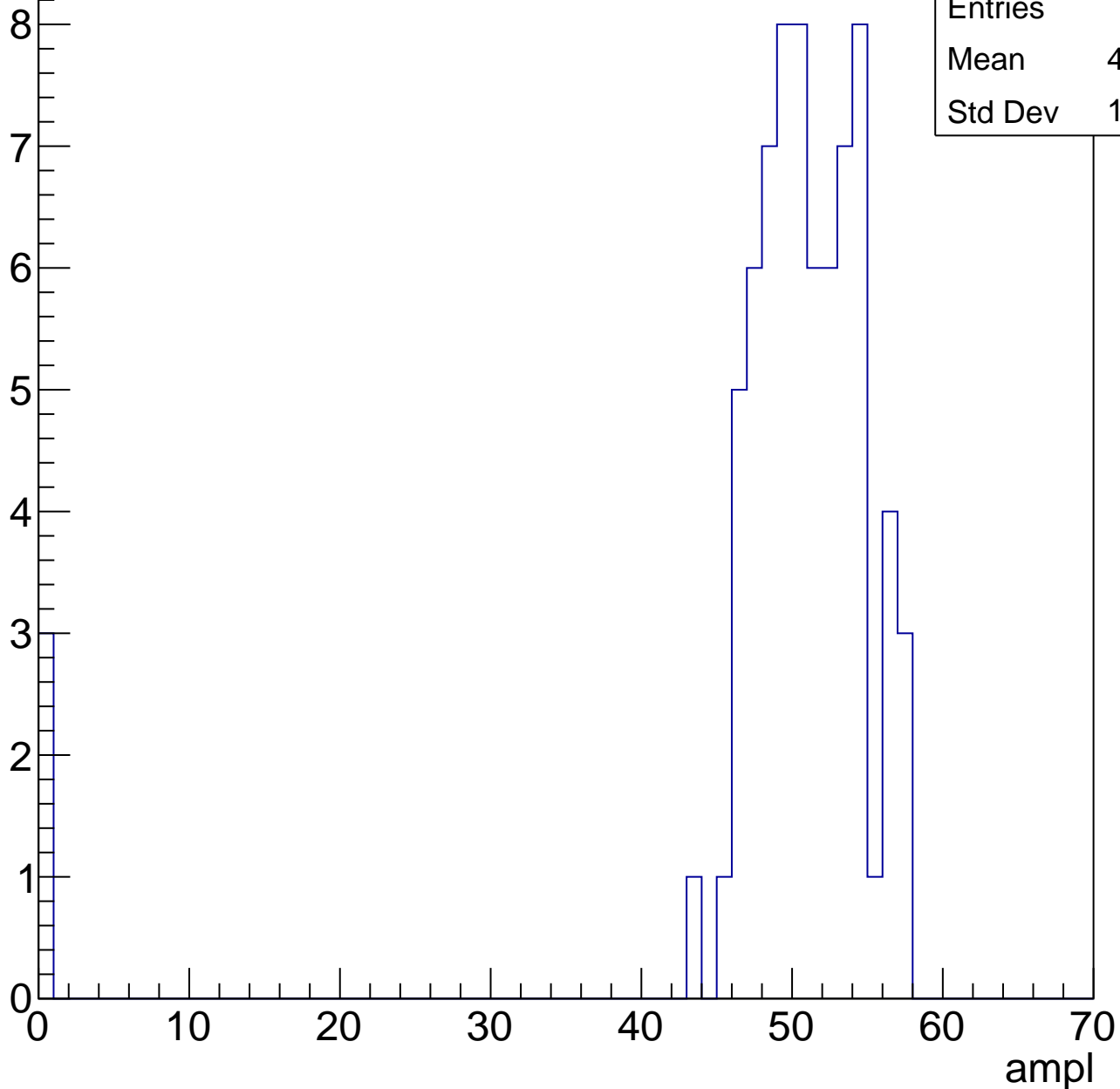


# B1L103S, U26-ch21, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	74
Mean	48.64
Std Dev	10.49

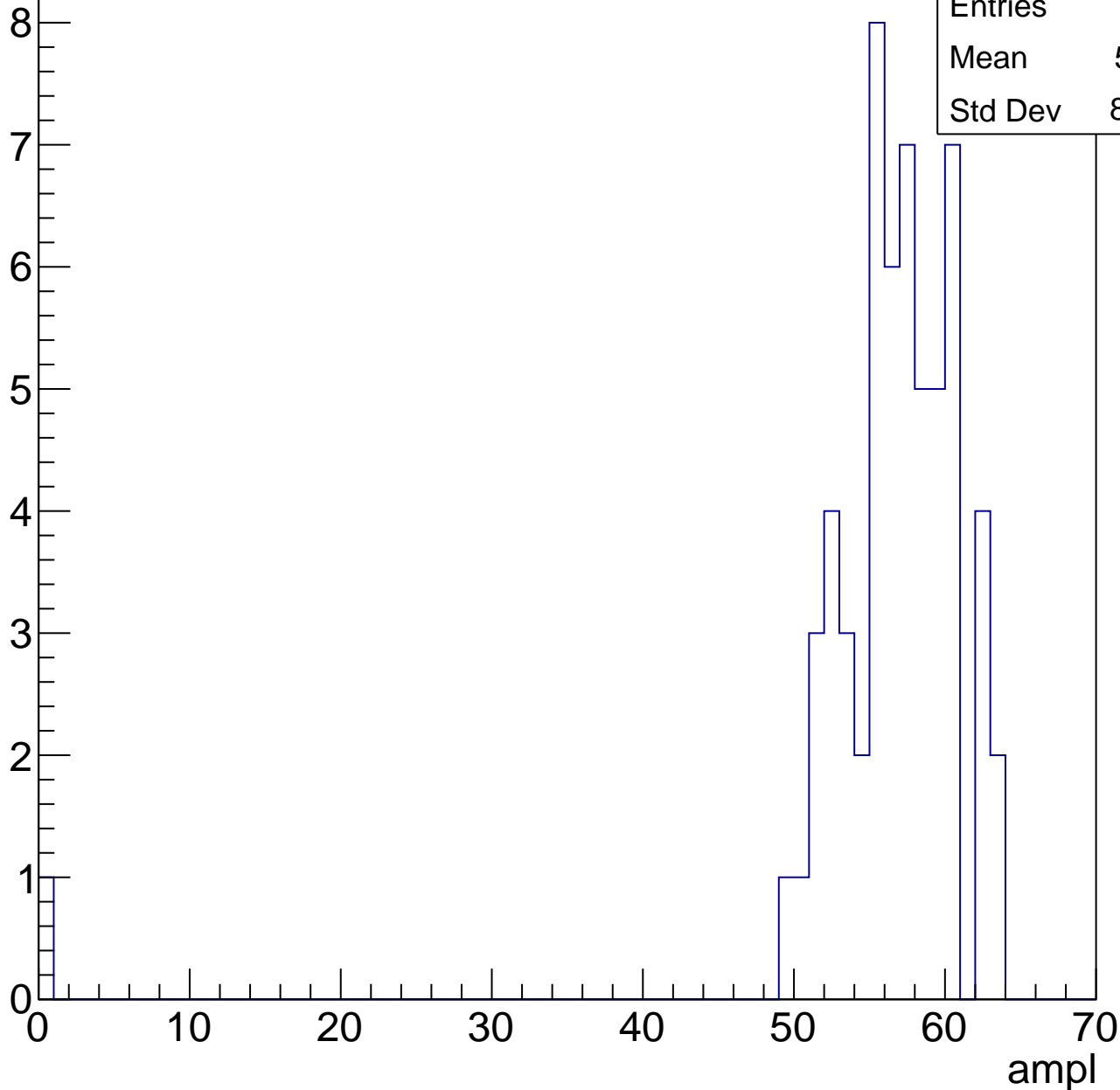


# B1L103S, U26-ch21, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	59
Mean	55.61
Std Dev	8.047

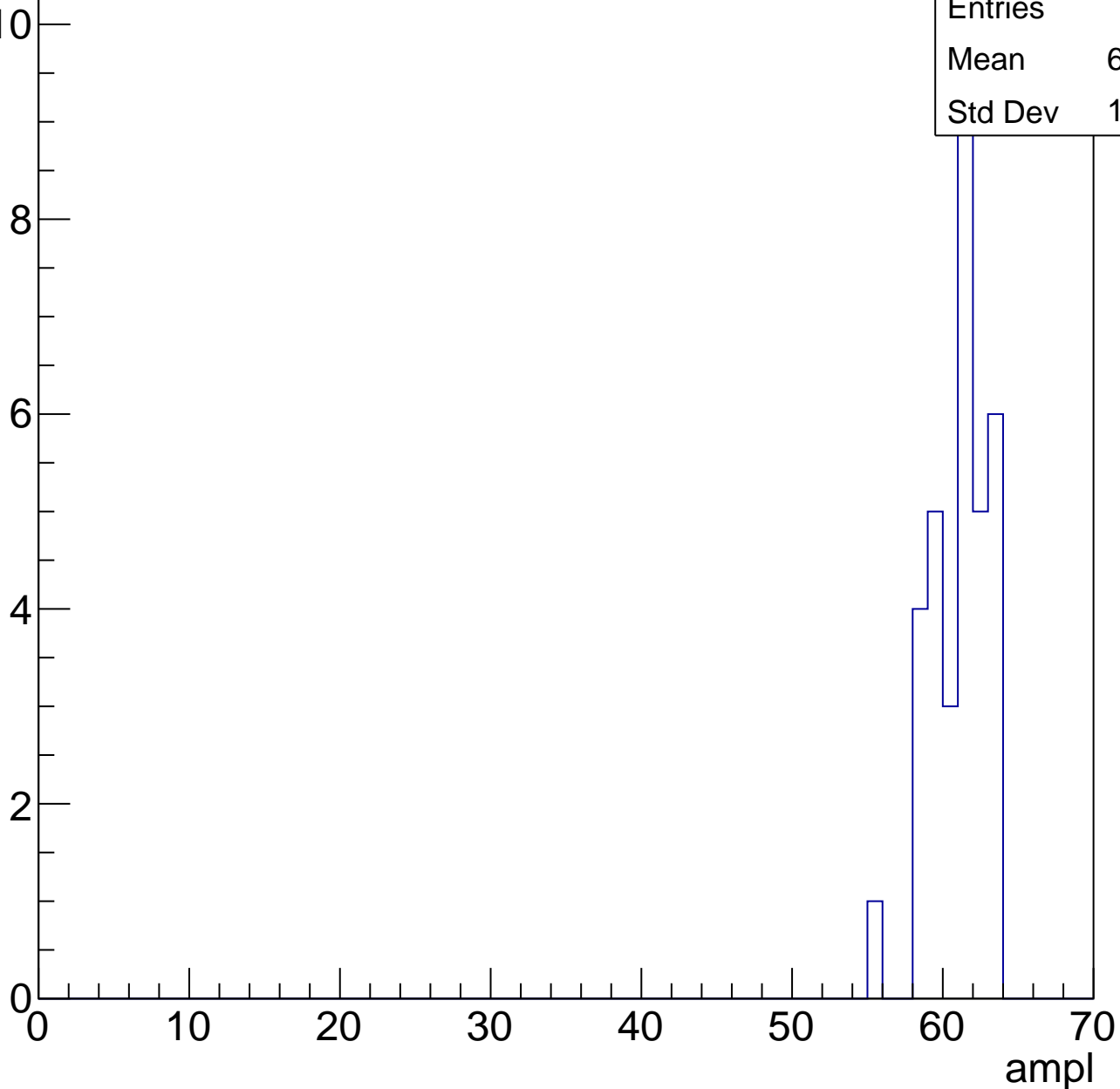


# B1L103S, U26-ch21, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	34
Mean	60.59
Std Dev	1.865



# B1L103S, U26-ch21, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry





# B1L103S, U26-ch21, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

18  
16  
14  
12  
10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

Entries	19
Mean	0
Std Dev	0

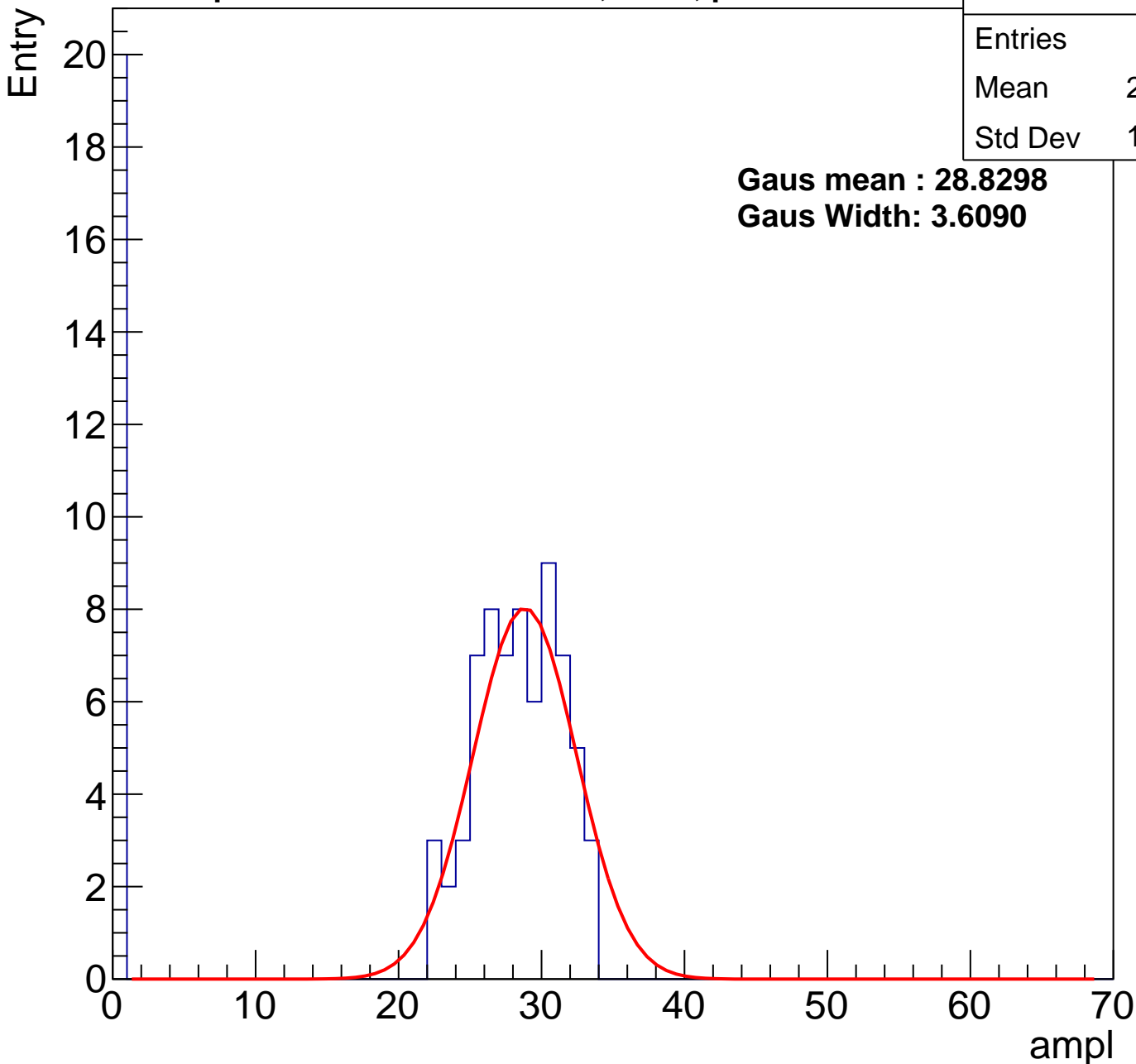
# B1L103S, U26-ch22, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	88
Mean	21.59
Std Dev	11.98

**Gaus mean : 28.8298**

**Gaus Width: 3.6090**



# B1L103S, U26-ch22, adc1

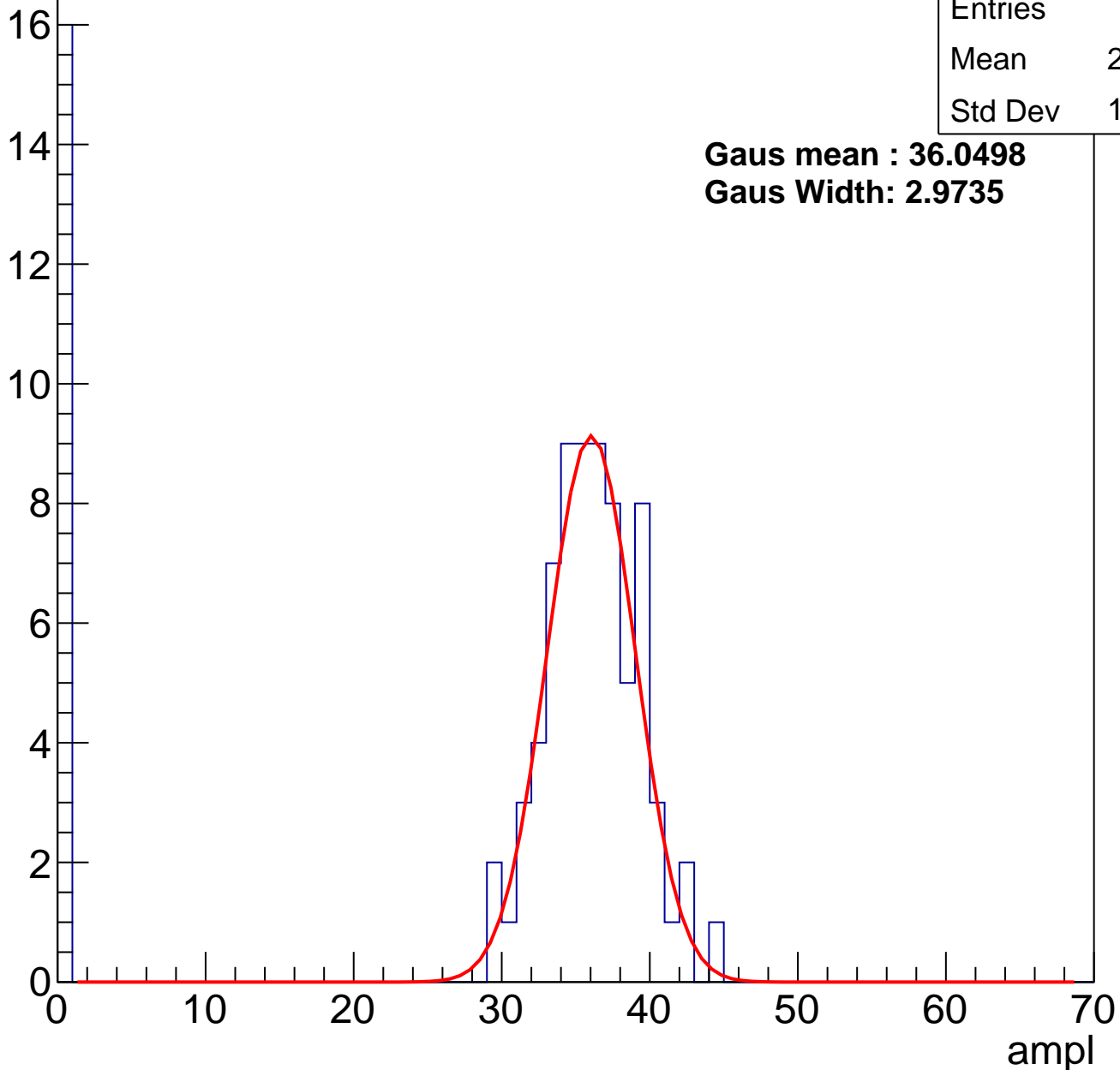
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	88
Mean	29.23
Std Dev	14.06

**Gaus mean : 36.0498**

**Gaus Width: 2.9735**

Entry



# B1L103S, U26-ch22, adc2

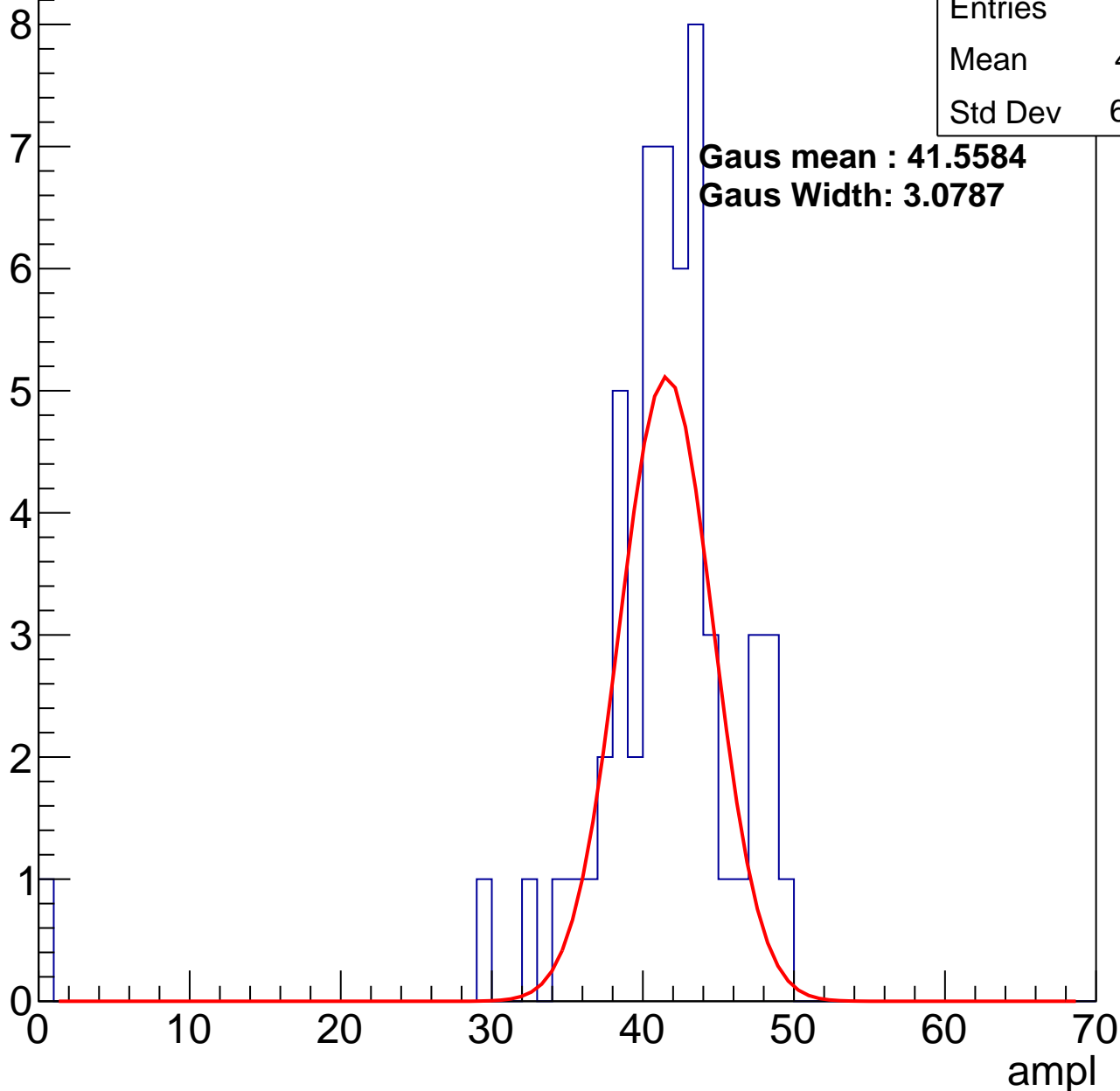
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	55
Mean	40.51
Std Dev	6.769

**Gaus mean : 41.5584**

**Gaus Width: 3.0787**

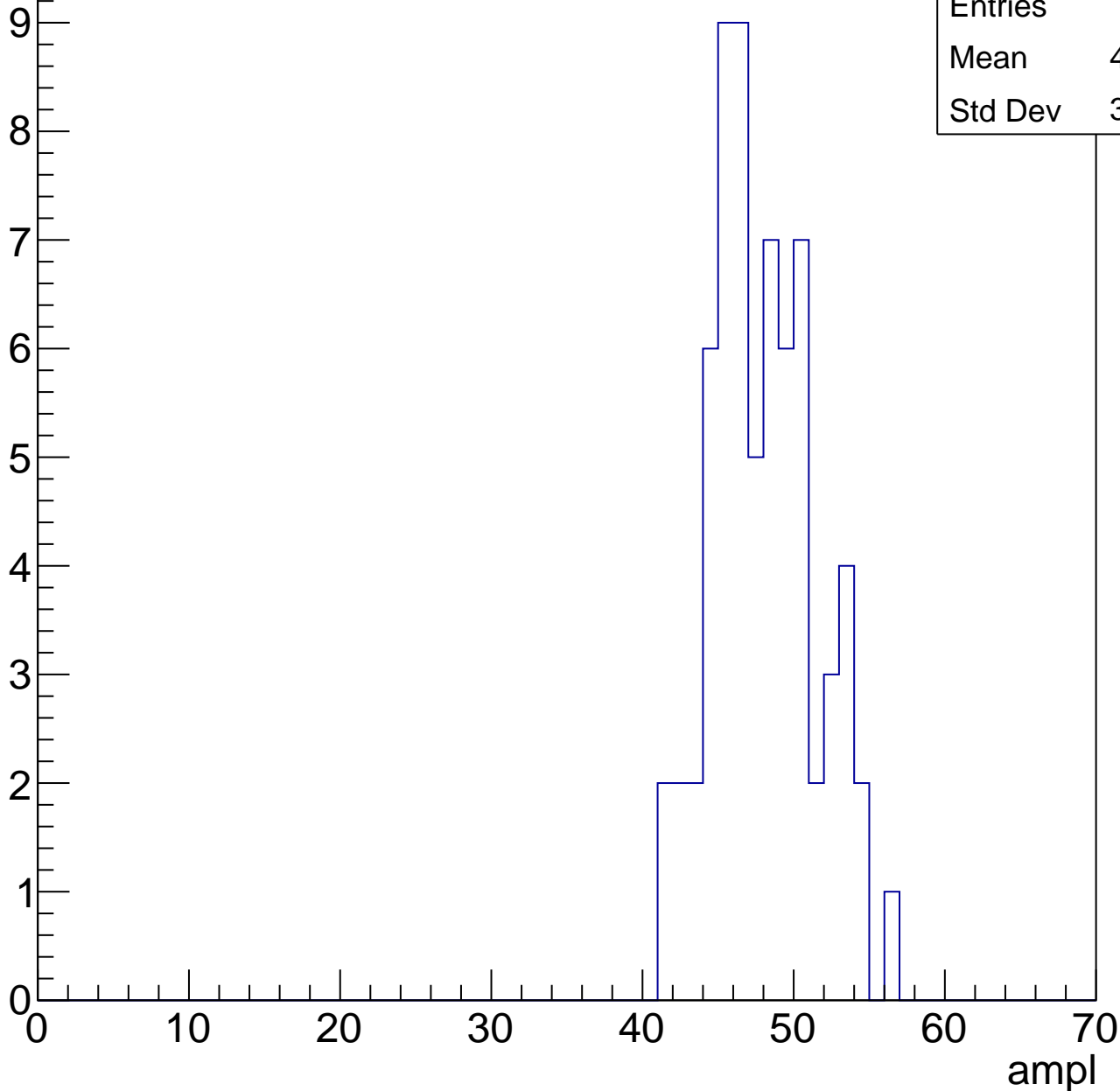


# B1L103S, U26-ch22, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	67
Mean	47.52
Std Dev	3.365

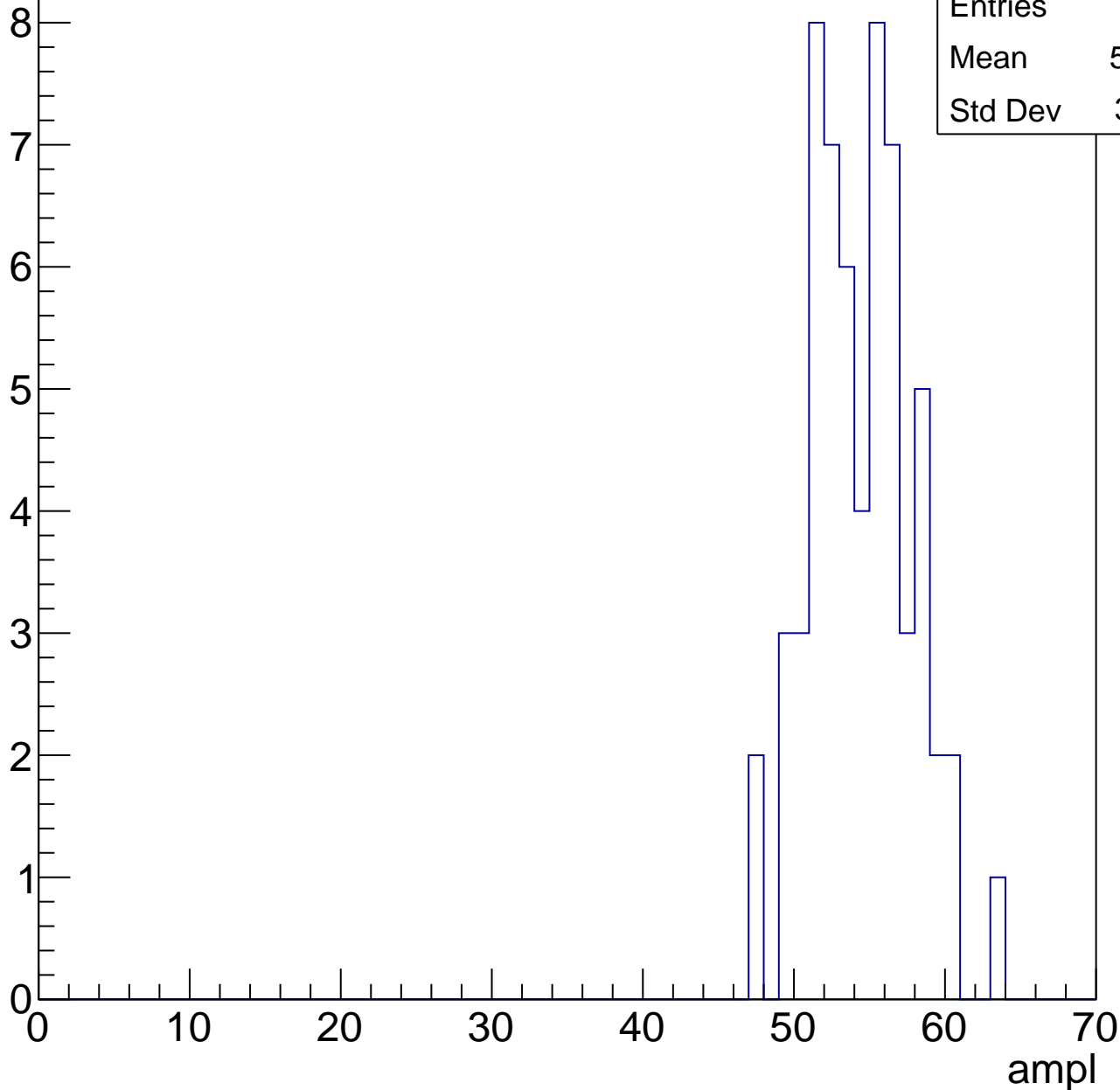


# B1L103S, U26-ch22, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

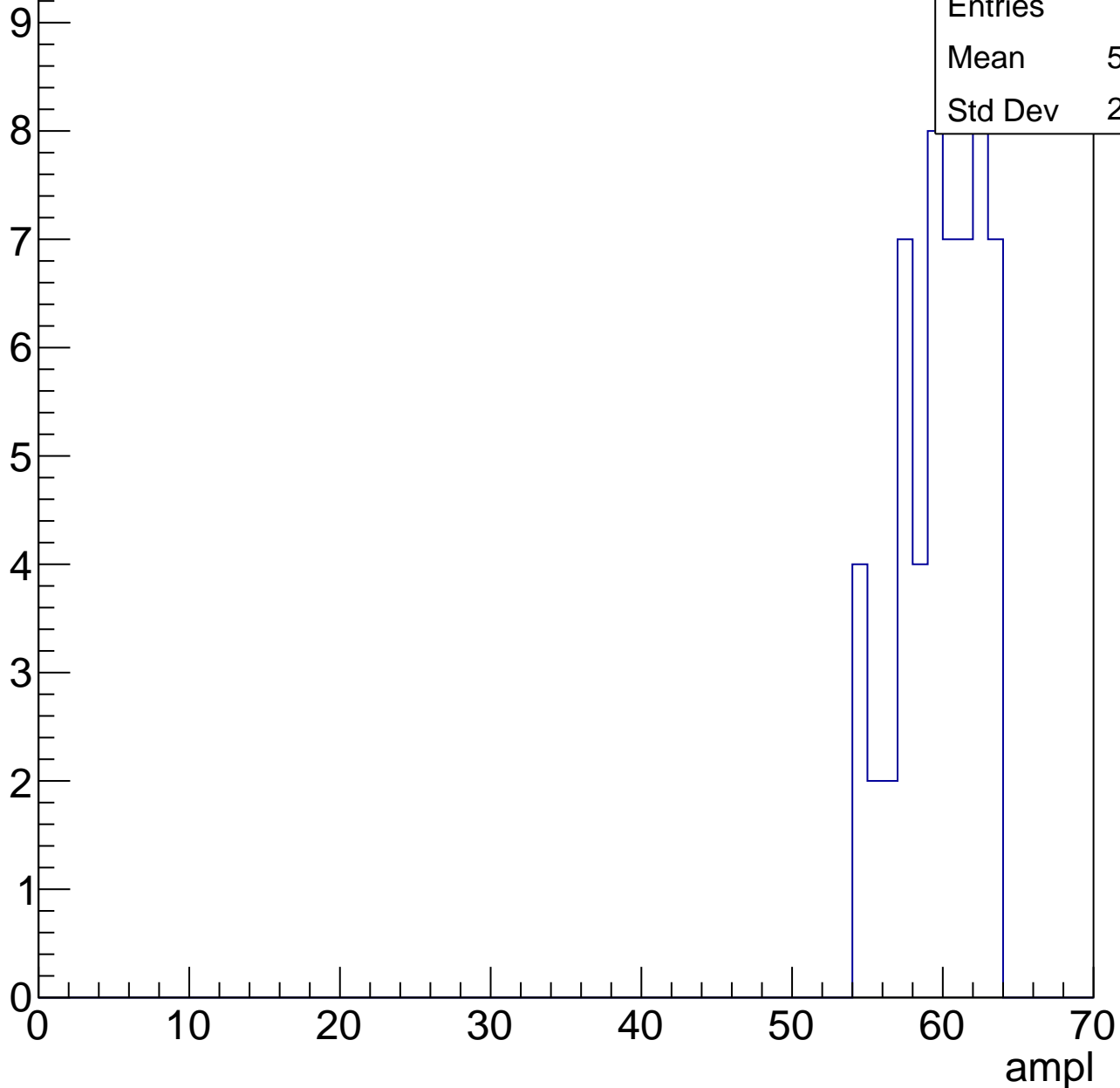
Entries	61
Mean	53.95
Std Dev	3.321



# B1L103S, U26-ch22, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



Entries	57
Mean	59.42
Std Dev	2.649

# B1L103S, U26-ch22, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

3

2.5

2

1.5

1

0.5

0

ampl

Entries	9
Mean	54.33
Std Dev	19.26

0 10 20 30 40 50 60 70



# B1L103S, U26-ch22, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



Entries	18
Mean	0
Std Dev	0

# B1L103S, U26-ch23, adc0

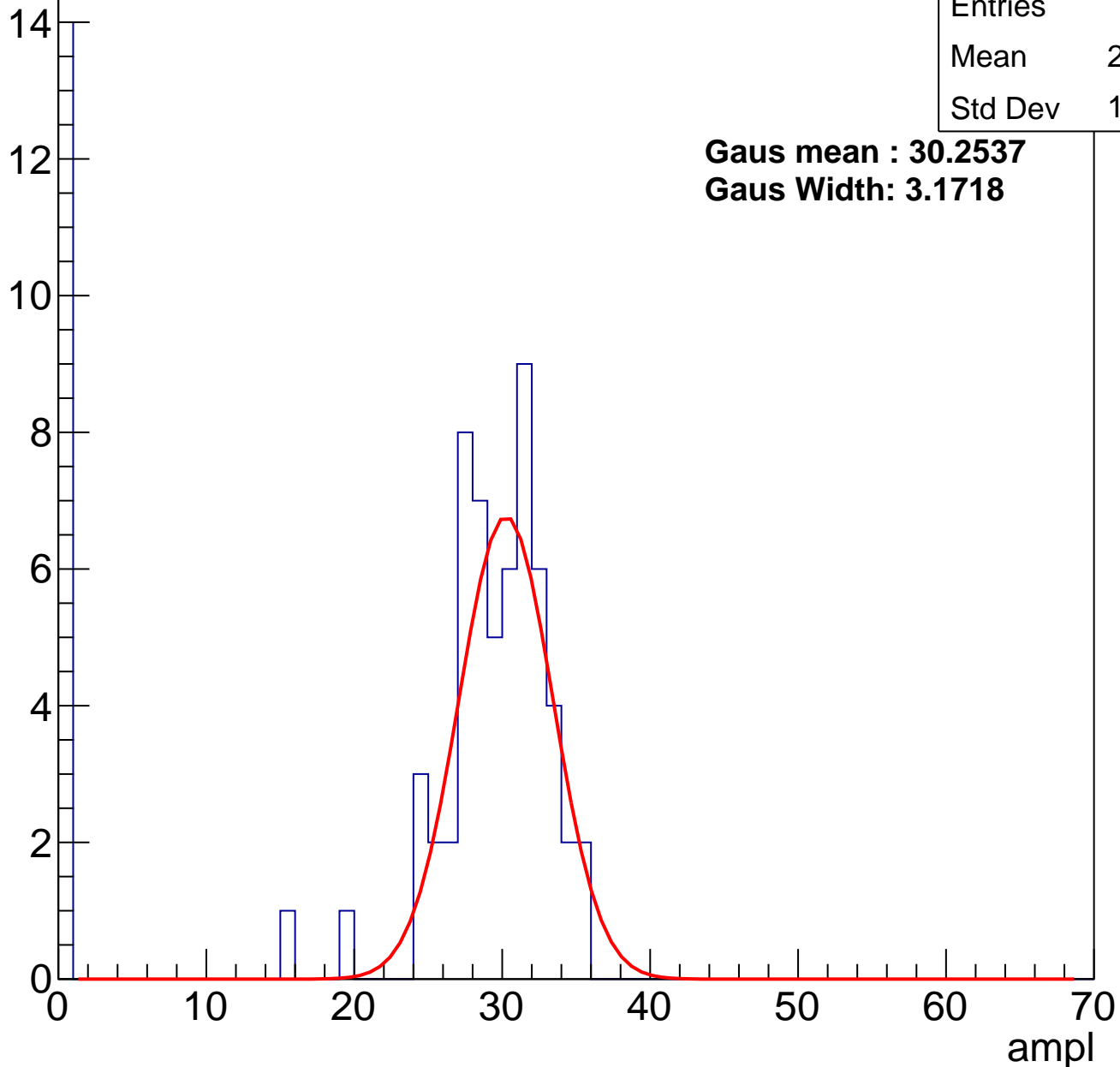
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	72
Mean	23.42
Std Dev	11.94

**Gaus mean : 30.2537**

**Gaus Width: 3.1718**

Entry



# B1L103S, U26-ch23, adc1

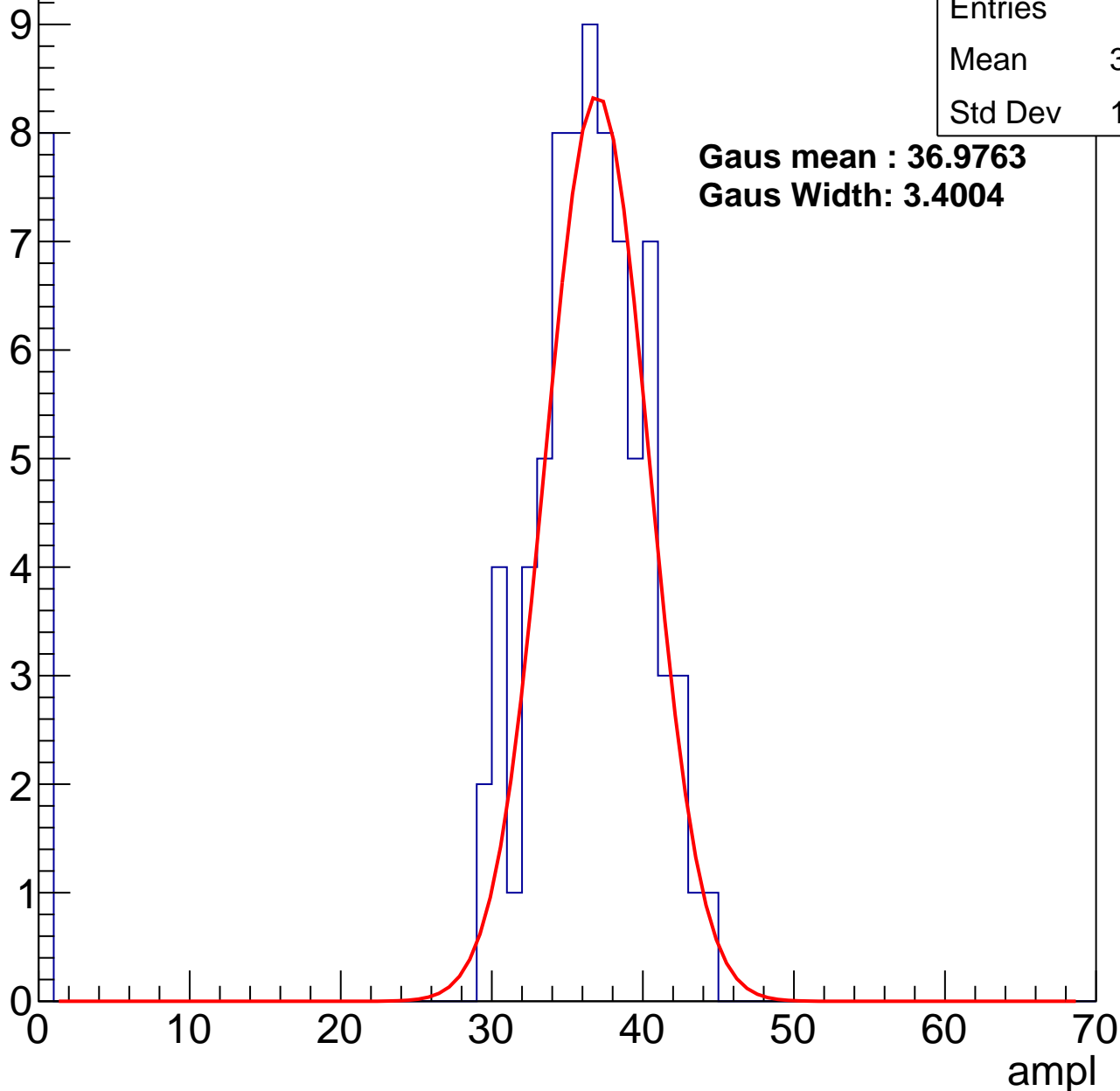
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	84
Mean	32.75
Std Dev	11.12

**Gaus mean : 36.9763**

**Gaus Width: 3.4004**



# B1L103S, U26-ch23, adc2

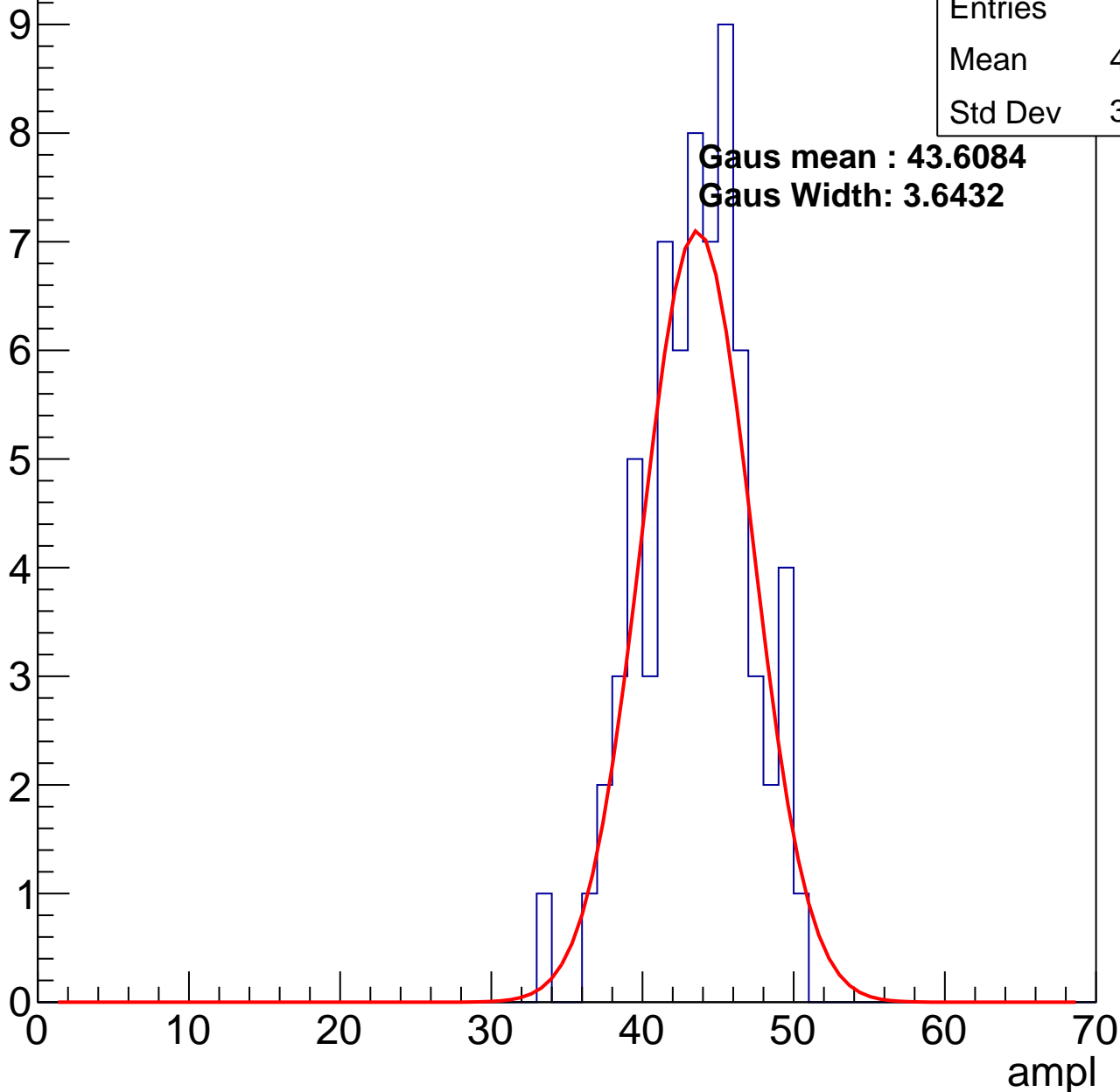
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	68
Mean	43.04
Std Dev	3.483

**Gaus mean : 43.6084**

**Gaus Width: 3.6432**

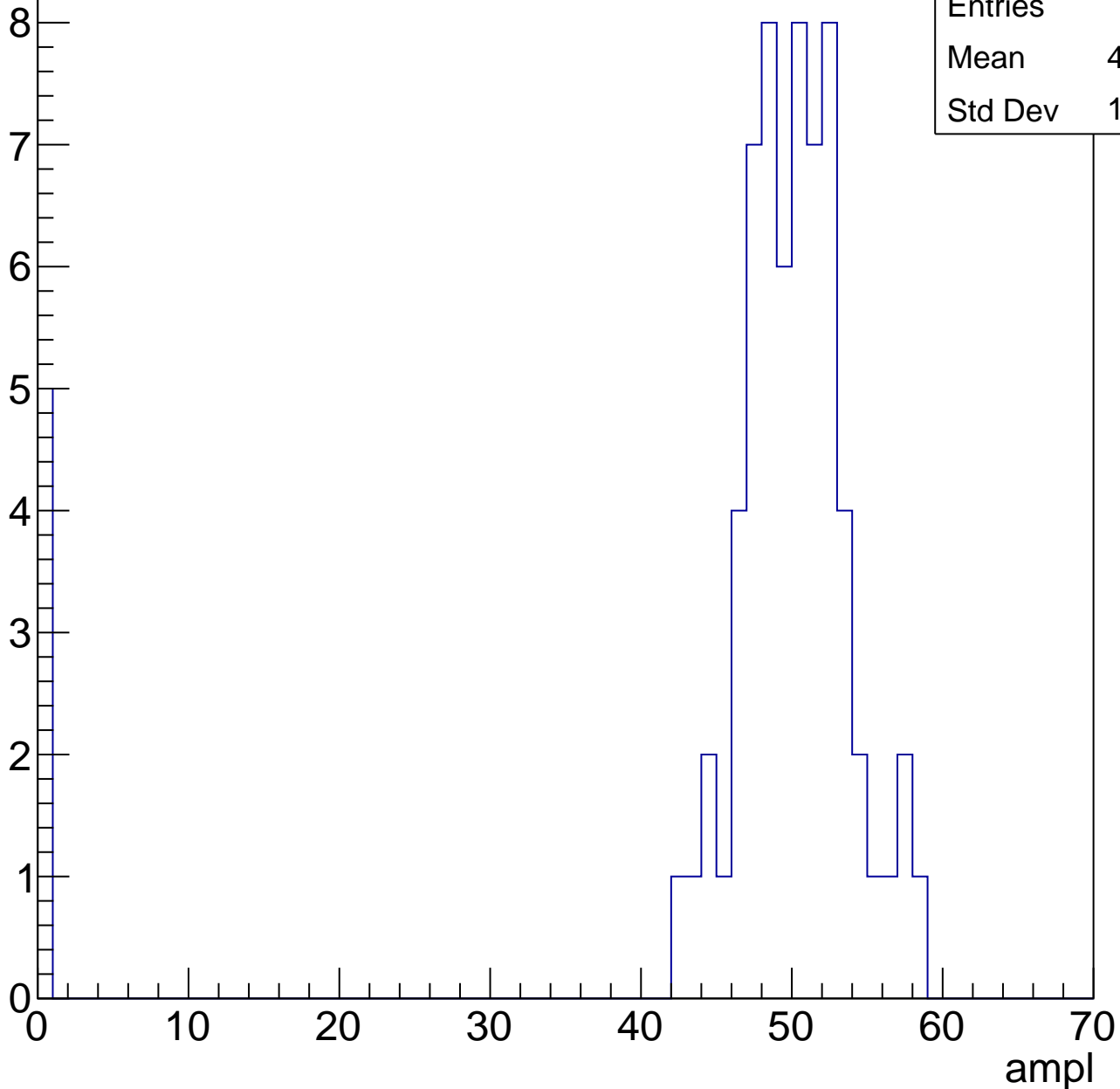


# B1L103S, U26-ch23, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	69
Mean	46.16
Std Dev	13.29

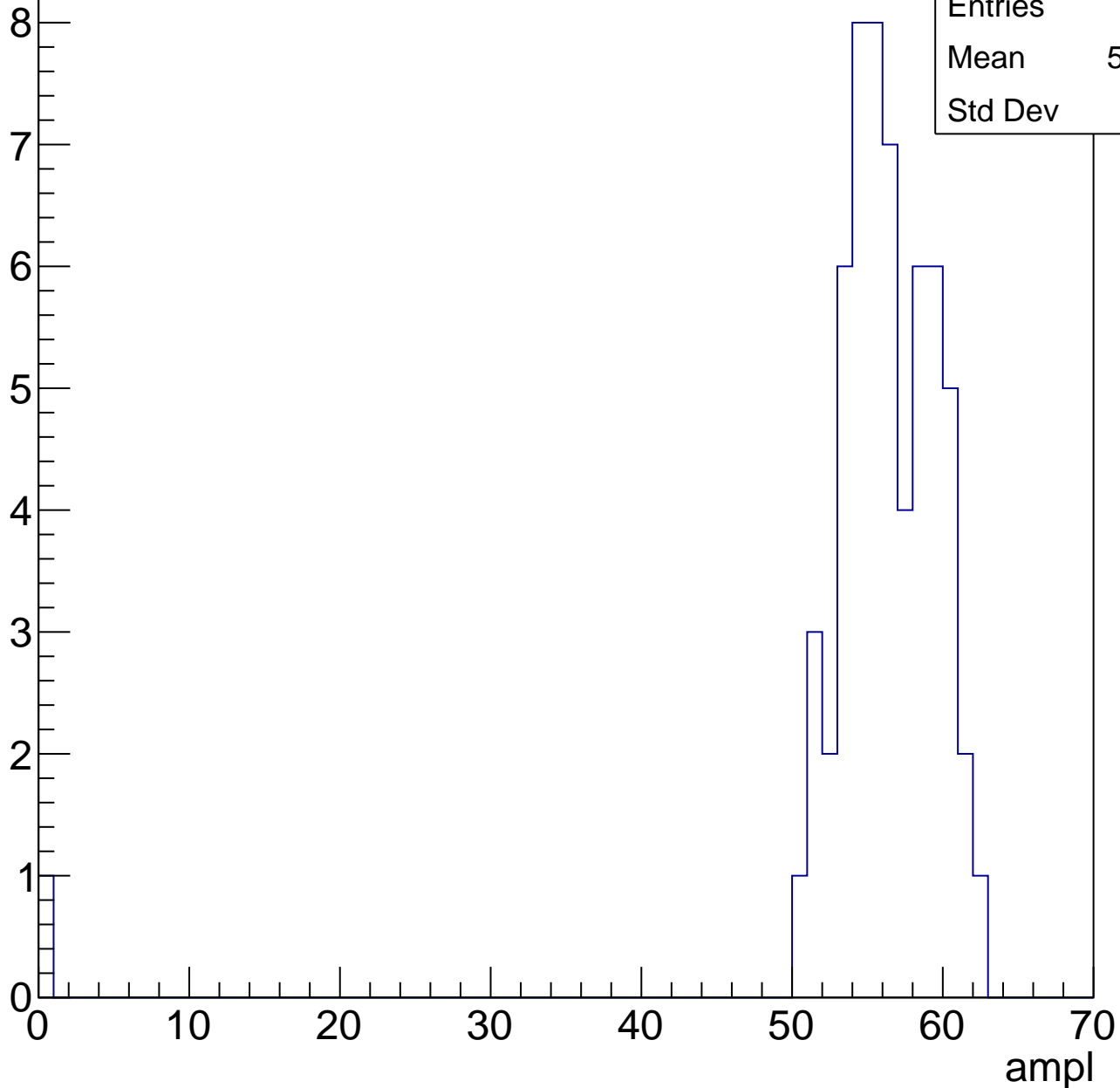


# B1L103S, U26-ch23, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

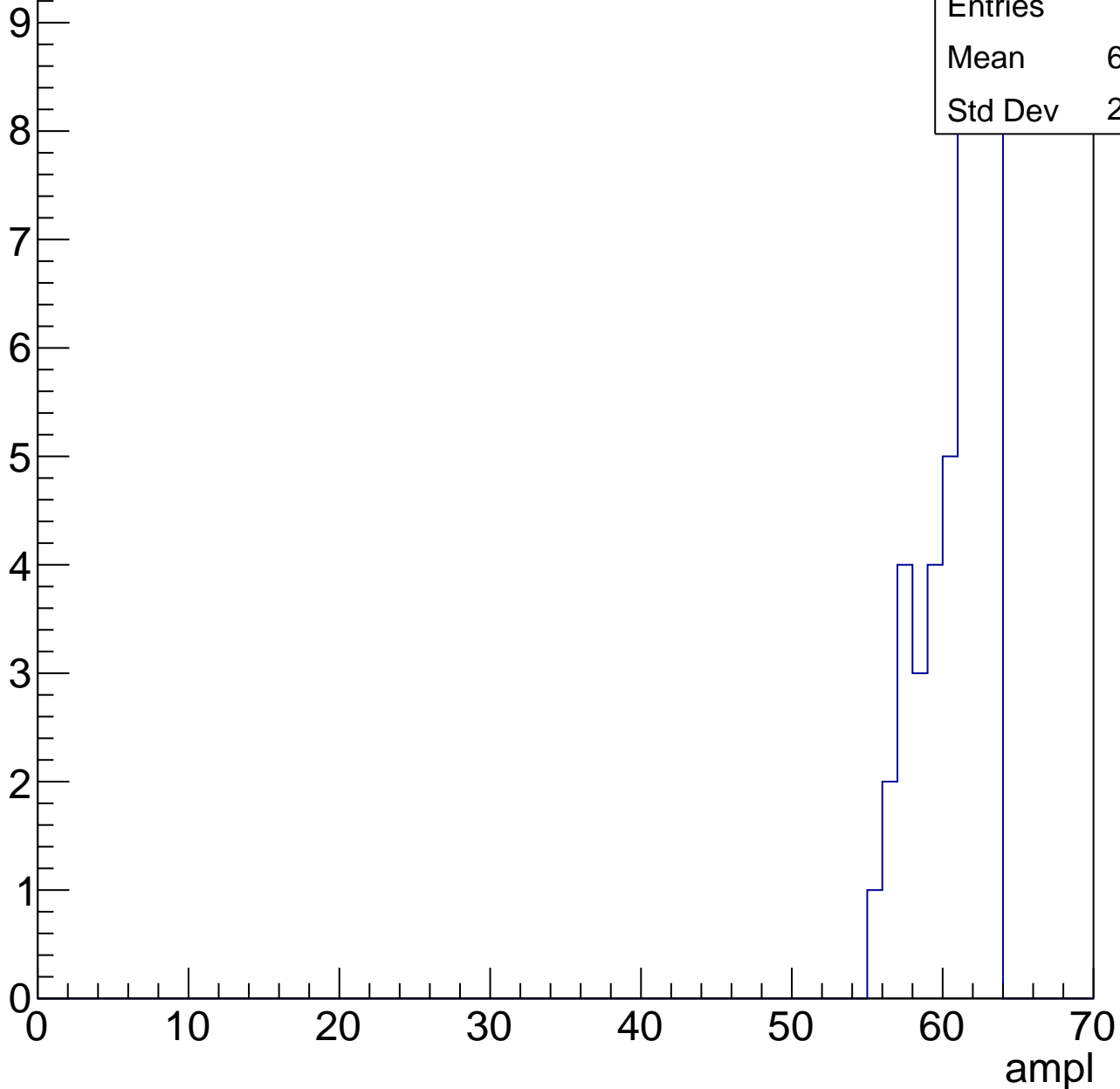
Entries	60
Mean	55.05
Std Dev	7.71



# B1L103S, U26-ch23, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



# B1L103S, U26-ch23, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	2
Mean	63
Std Dev	0

0 10 20 30 40 50 60 70

ampl



# B1L103S, U26-ch23, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

18  
16  
14  
12  
10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

Entries	19
Mean	0
Std Dev	0

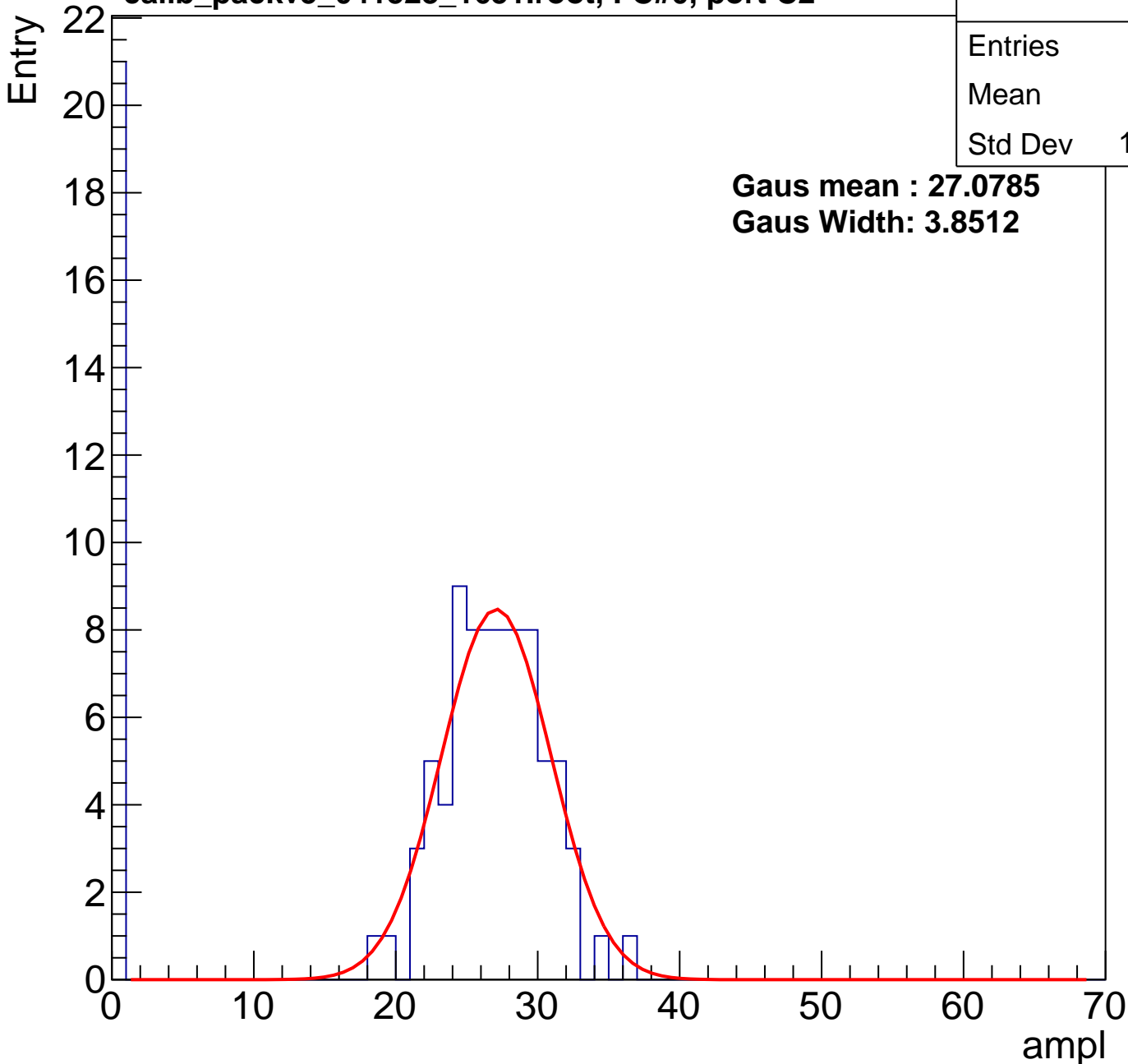
# B1L103S, U26-ch24, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	99
Mean	20.9
Std Dev	11.26

**Gaus mean : 27.0785**

**Gaus Width: 3.8512**



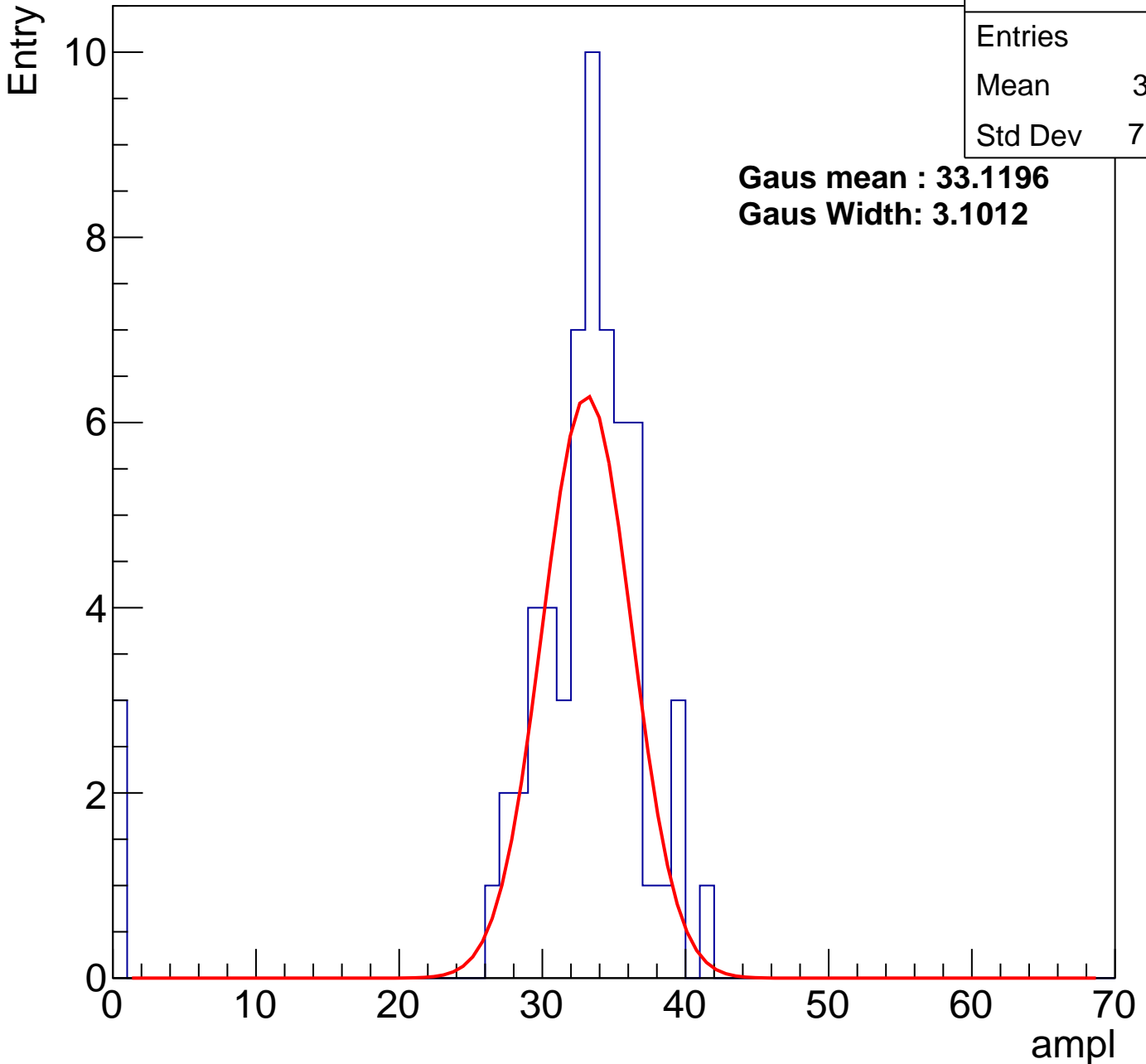
# B1L103S, U26-ch24, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	61
Mean	31.41
Std Dev	7.789

**Gaus mean : 33.1196**

**Gaus Width: 3.1012**



# B1L103S, U26-ch24, adc2

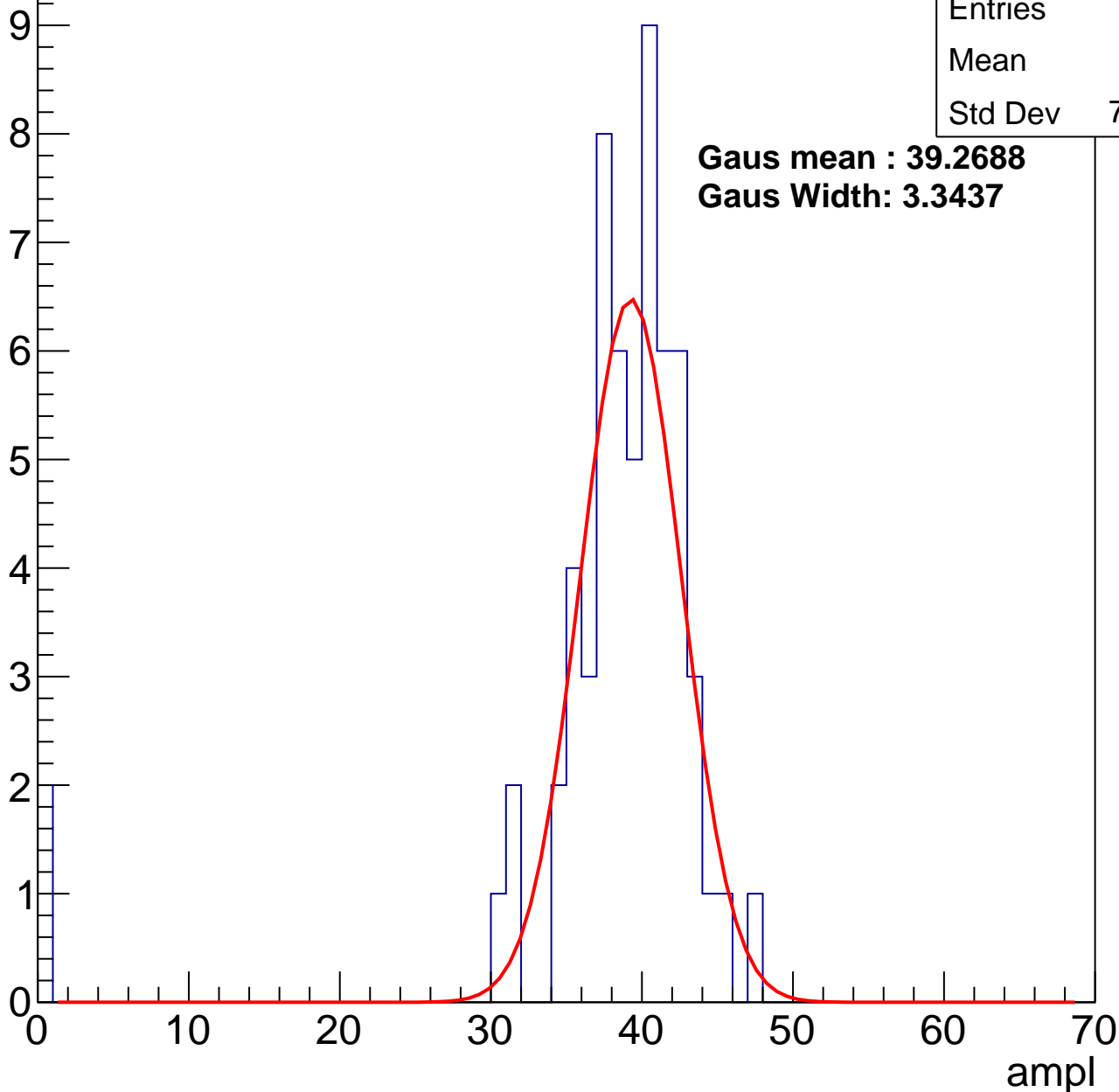
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	60
Mean	37.5
Std Dev	7.697

**Gaus mean : 39.2688**

**Gaus Width: 3.3437**

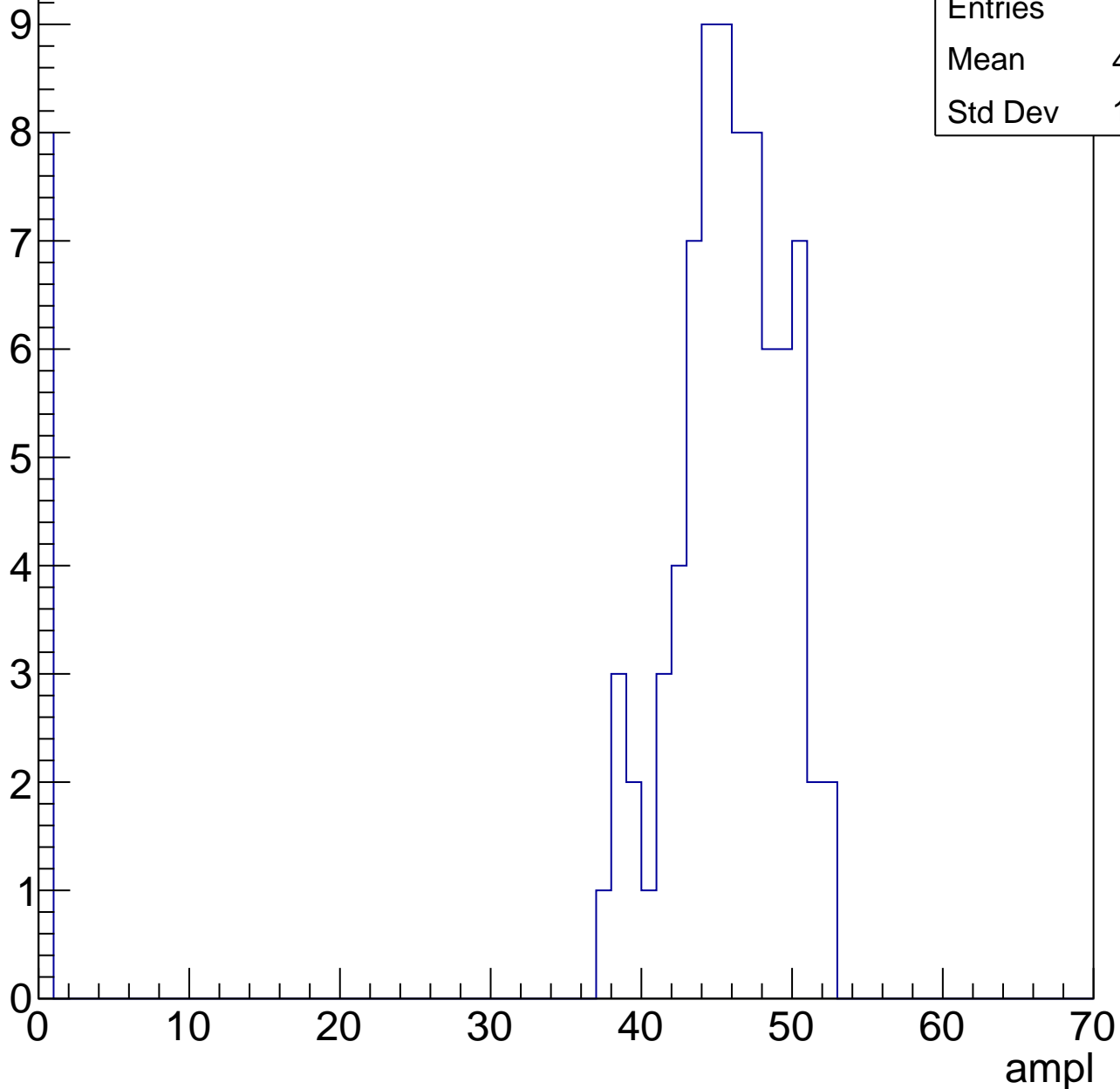


# B1L103S, U26-ch24, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	86
Mean	41.21
Std Dev	13.61

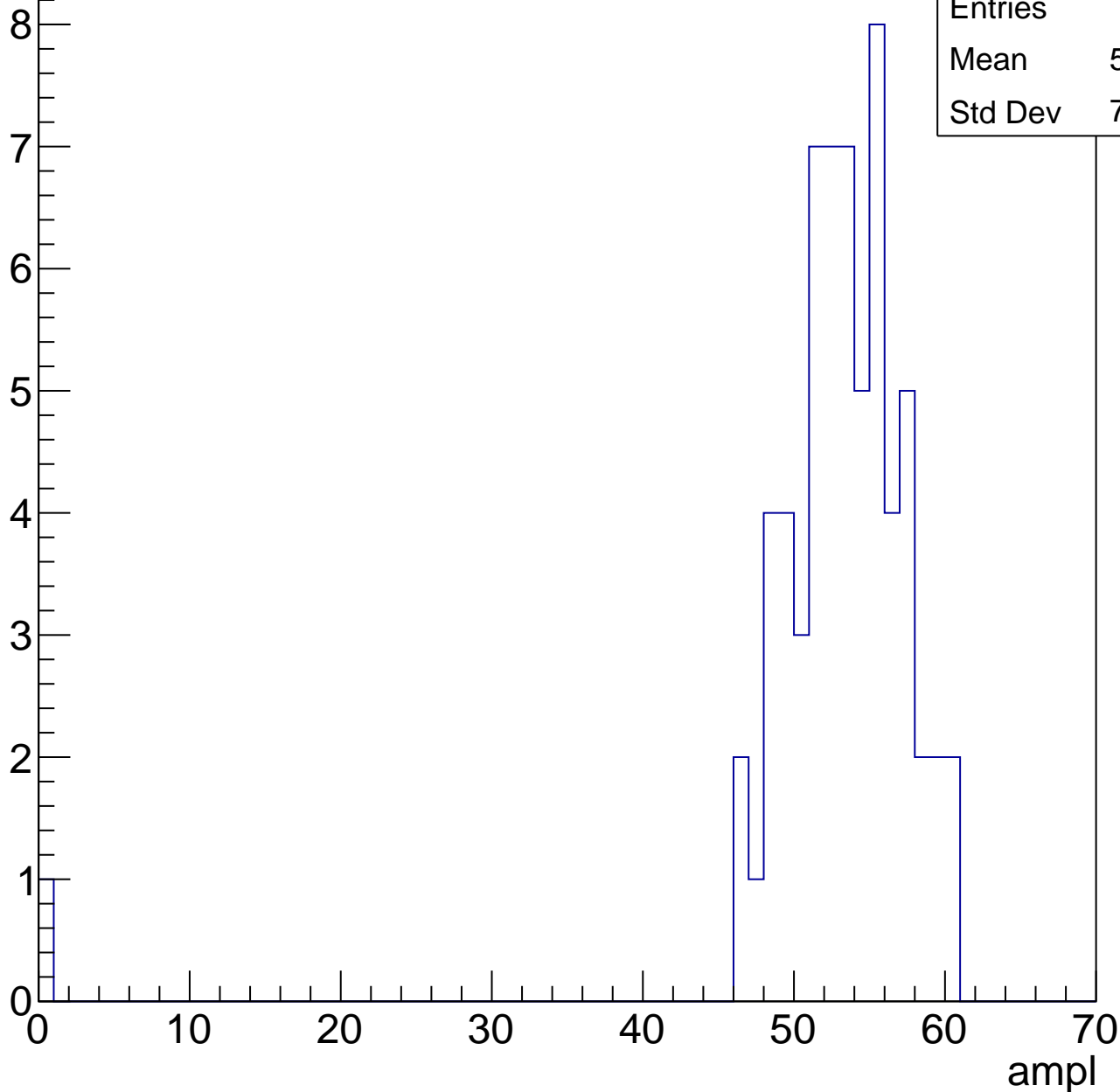


# B1L103S, U26-ch24, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	64
Mean	52.22
Std Dev	7.398

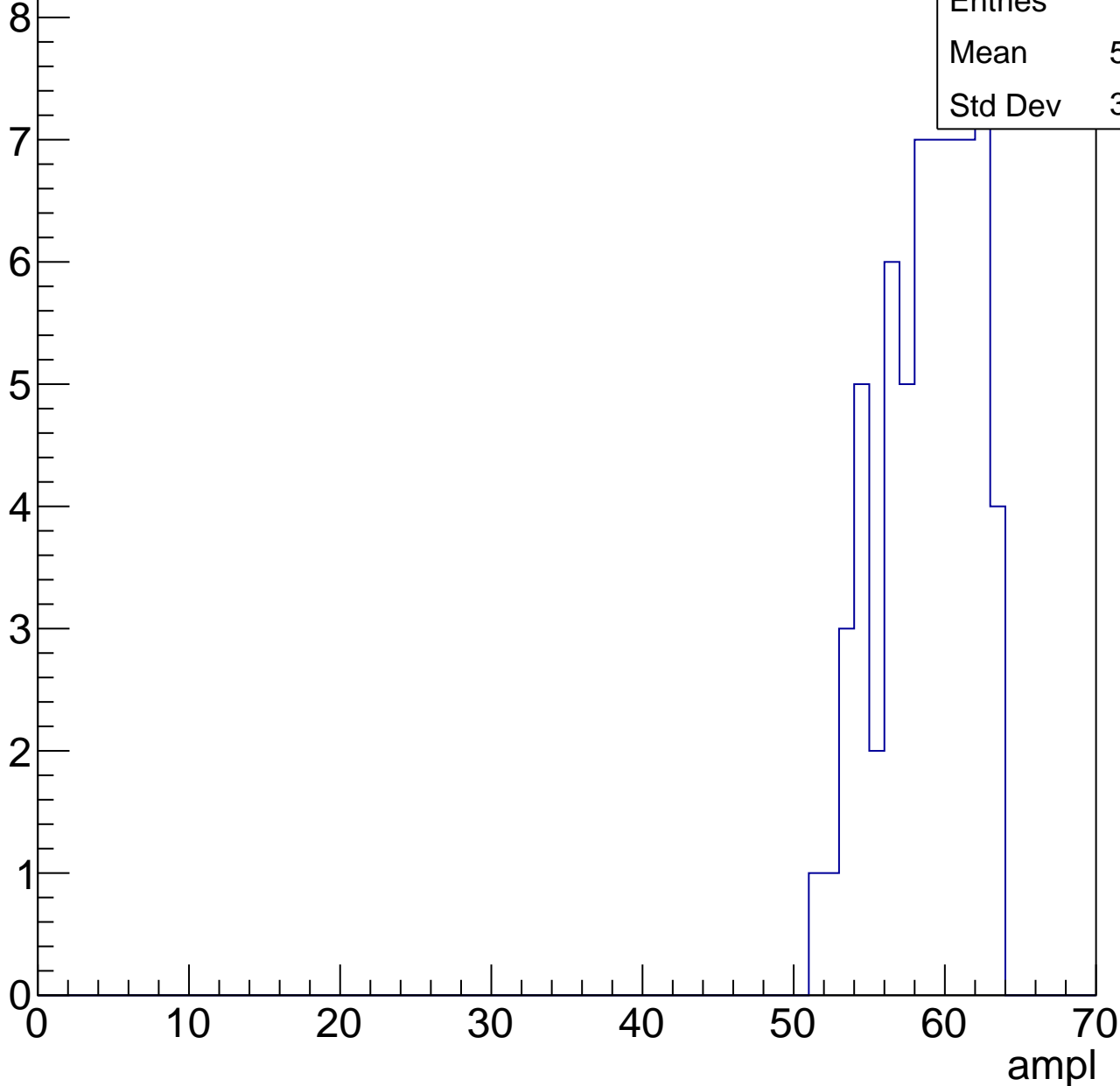


# B1L103S, U26-ch24, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

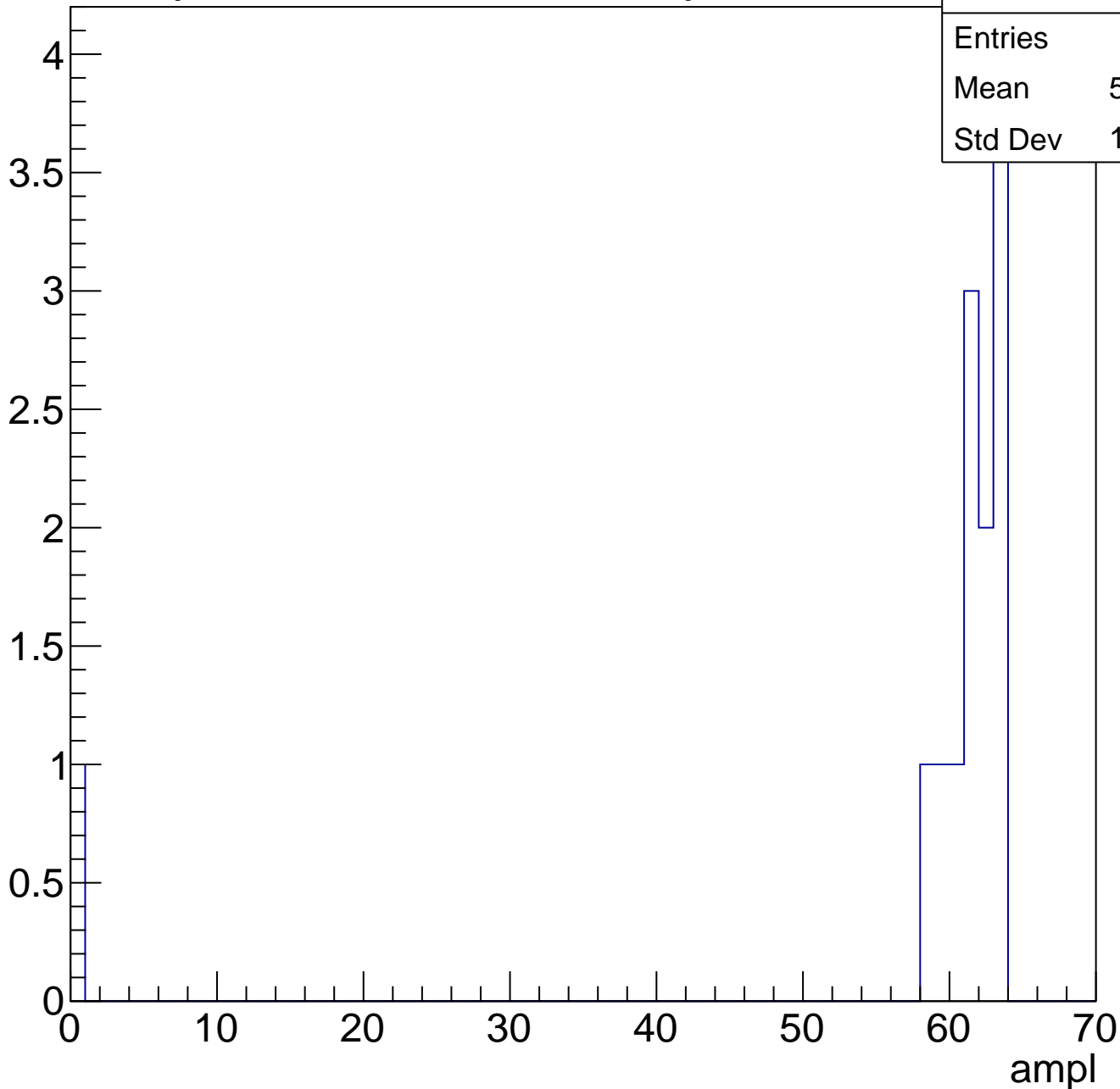
Entries	63
Mean	58.37
Std Dev	3.098



# B1L103S, U26-ch24, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



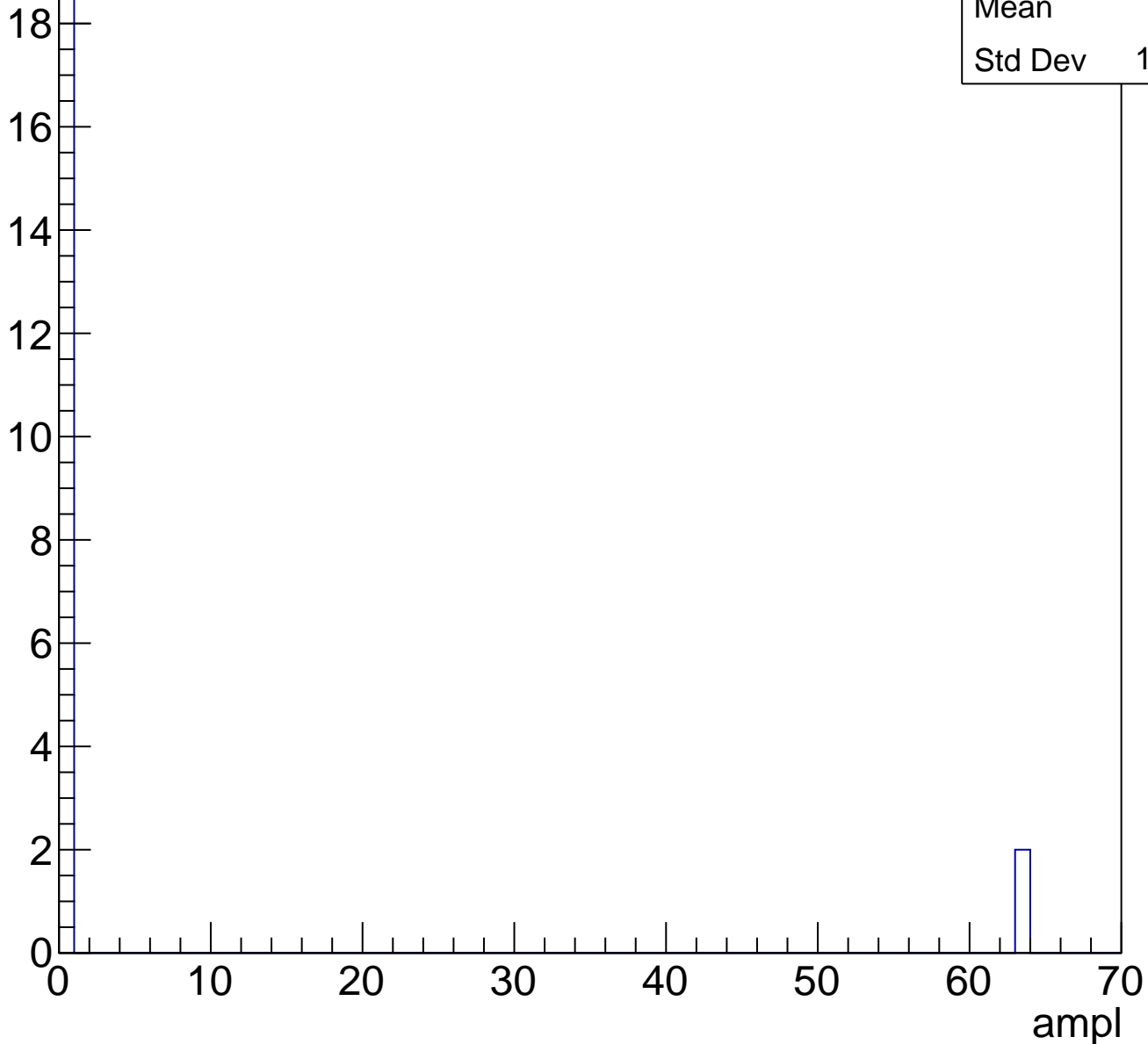


# B1L103S, U26-ch24, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	21
Mean	6
Std Dev	18.49

Entry



# B1L103S, U26-ch25, adc0

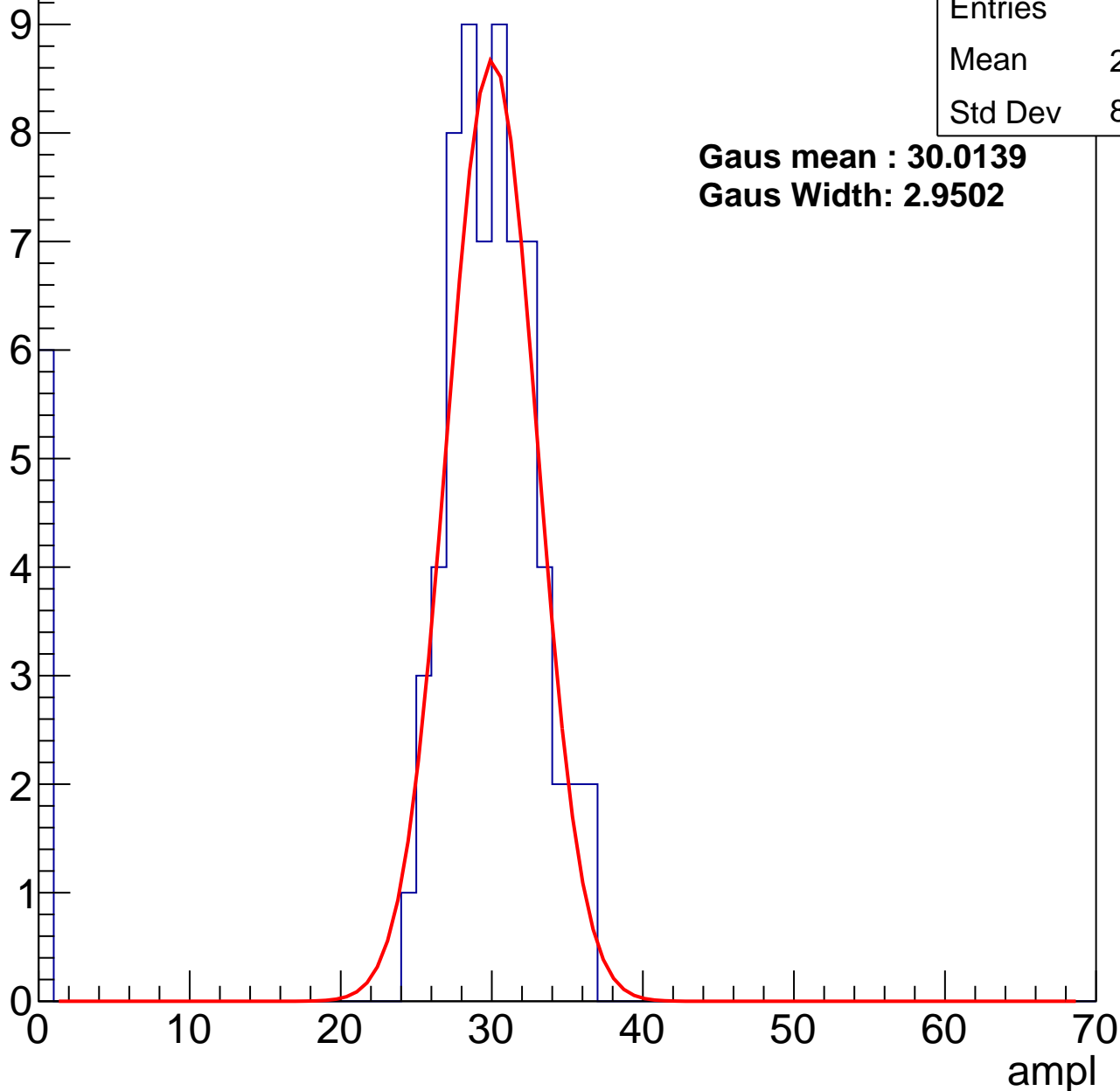
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	71
Mean	27.14
Std Dev	8.668

**Gaus mean : 30.0139**

**Gaus Width: 2.9502**



# B1L103S, U26-ch25, adc1

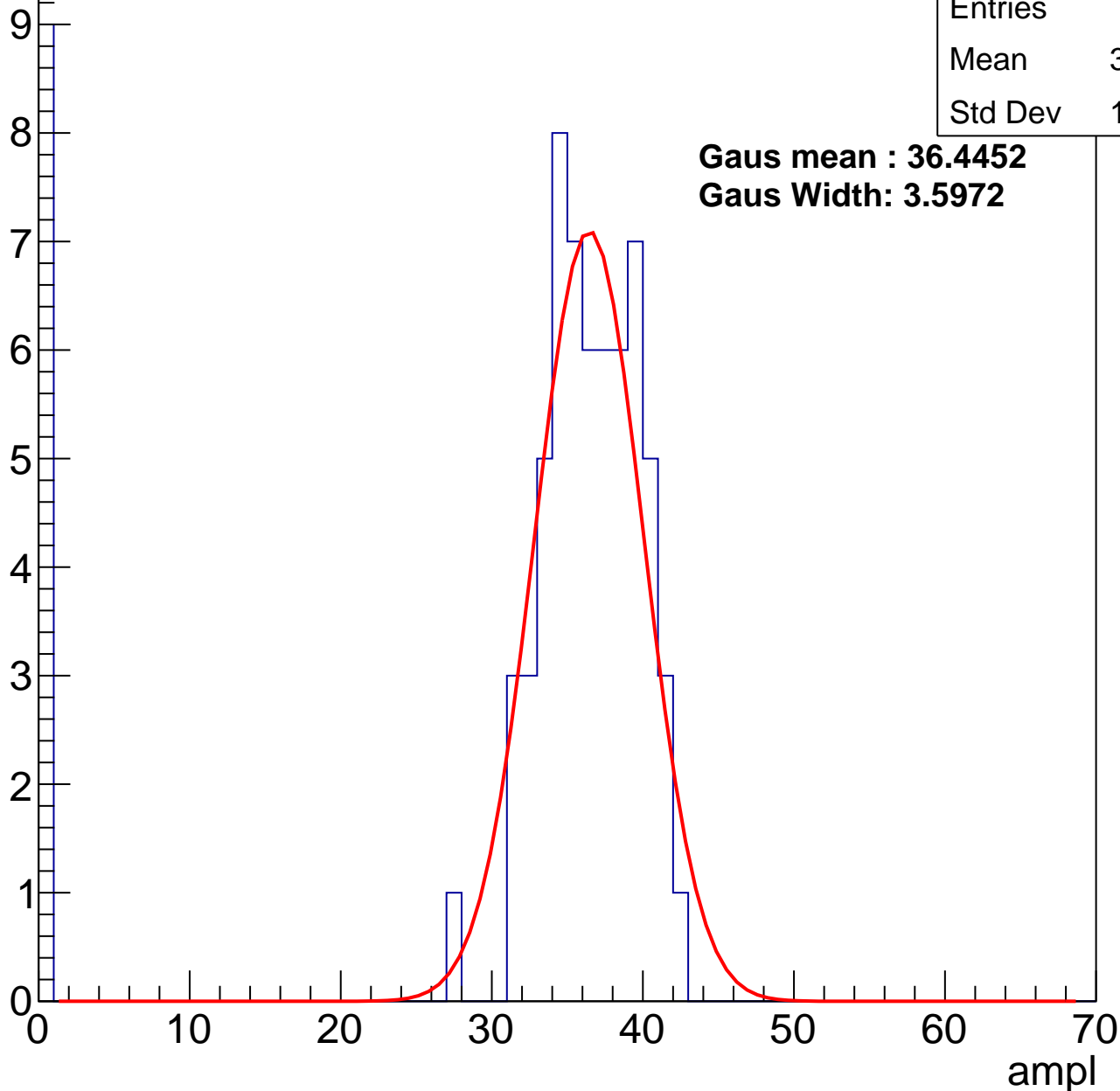
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	70
Mean	31.46
Std Dev	12.42

**Gaus mean : 36.4452**

**Gaus Width: 3.5972**



# B1L103S, U26-ch25, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	79
Mean	42.08
Std Dev	5.949

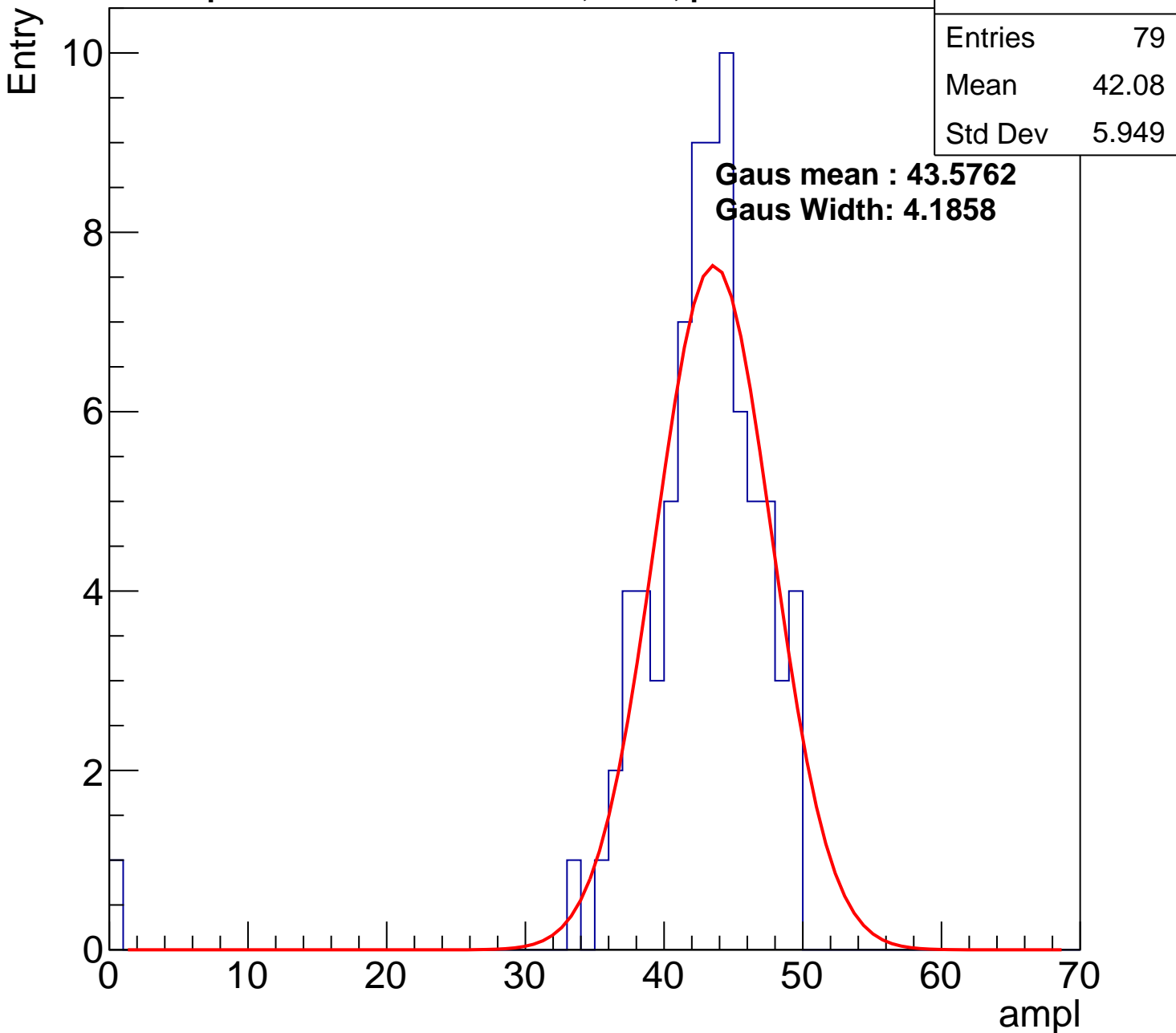
**Gaus mean : 43.5762**  
**Gaus Width: 4.1858**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

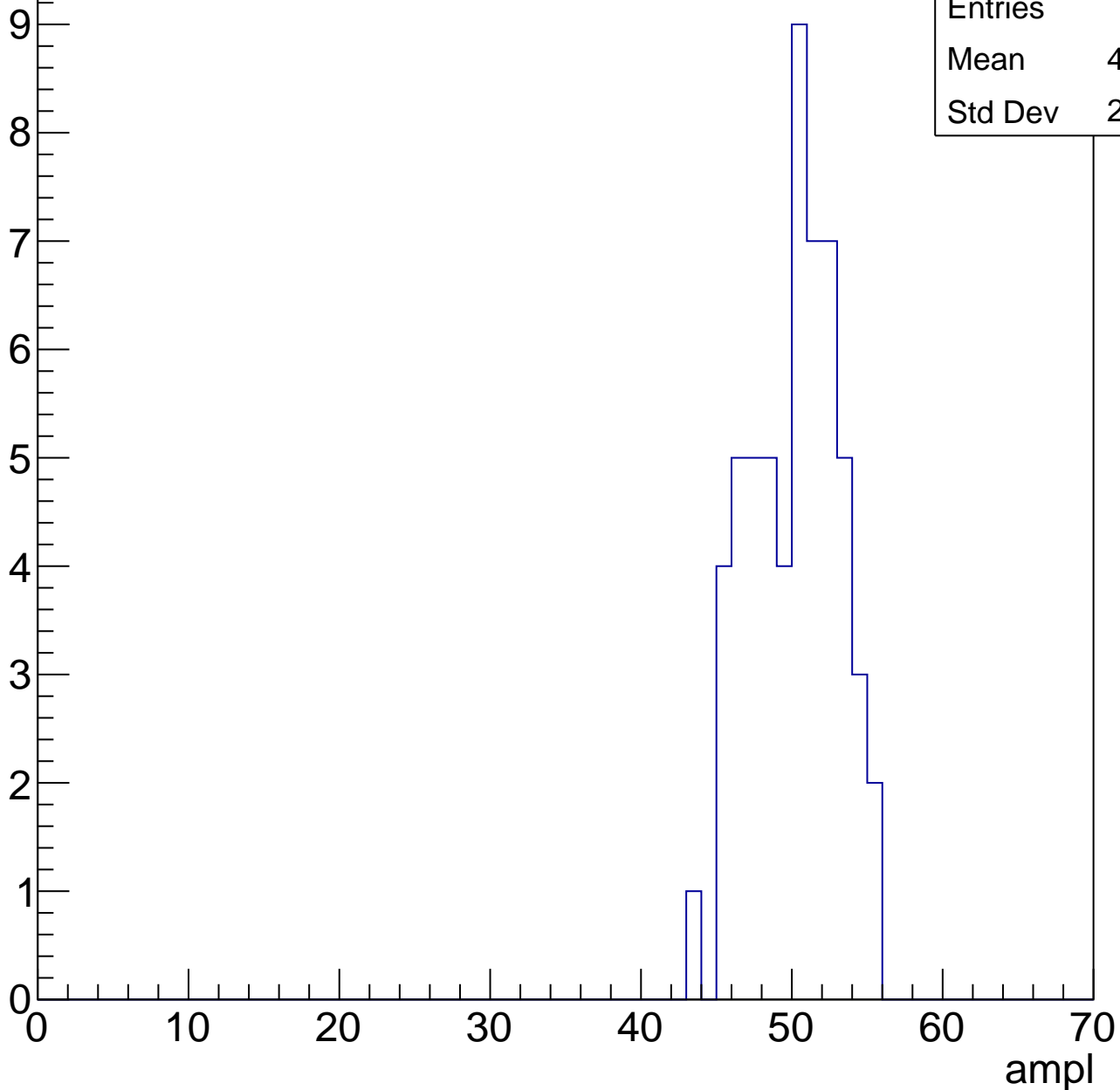


# B1L103S, U26-ch25, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

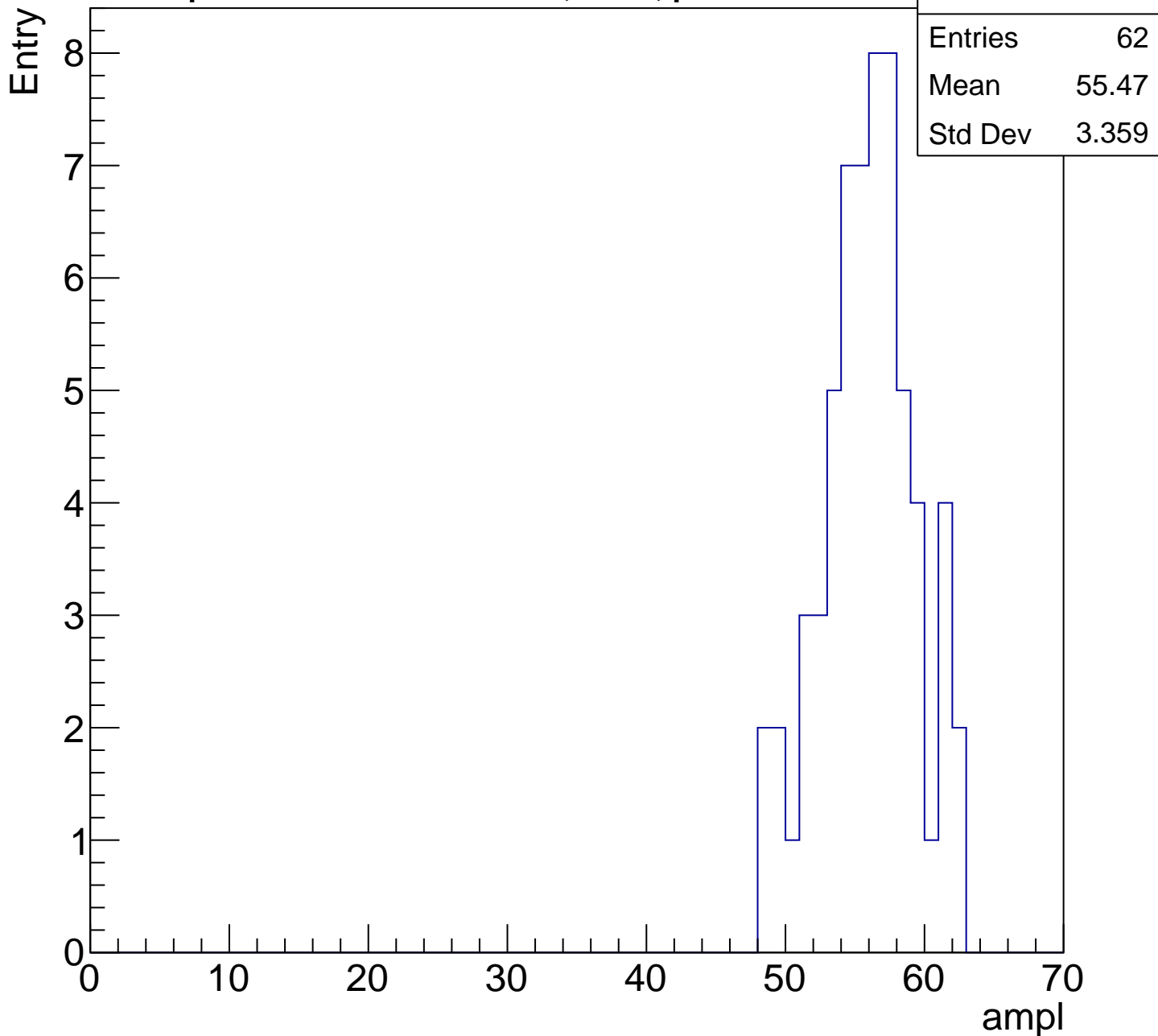
Entry

Entries	57
Mean	49.68
Std Dev	2.872



# B1L103S, U26-ch25, adc4

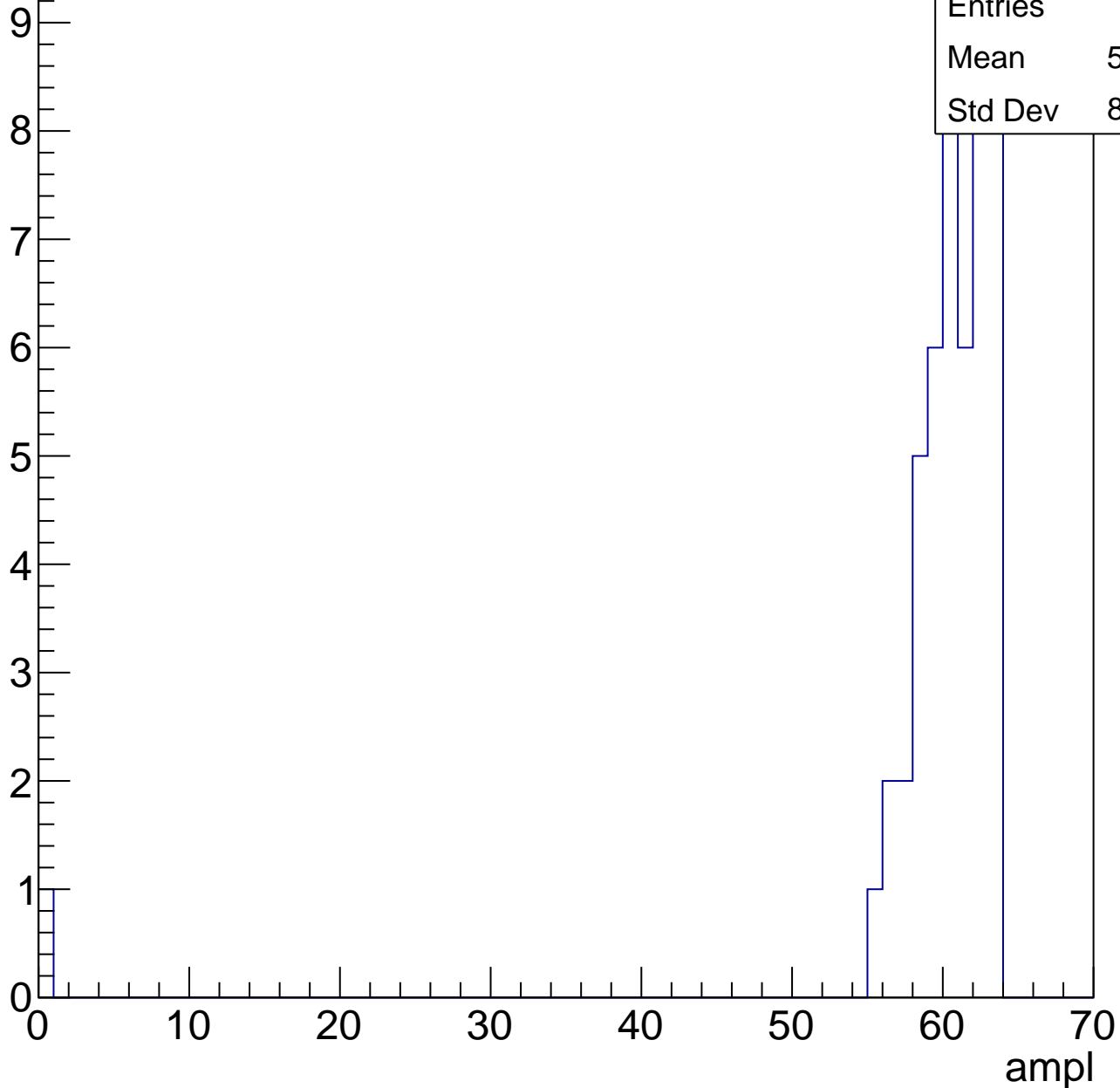
calib\_packv5\_041523\_1651.root, FC#0, port C2



# B1L103S, U26-ch25, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



# B1L103S, U26-ch25, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry





# B1L103S, U26-ch25, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	19
Mean	1.211
Std Dev	5.136

Entry



# B1L103S, U26-ch26, adc0

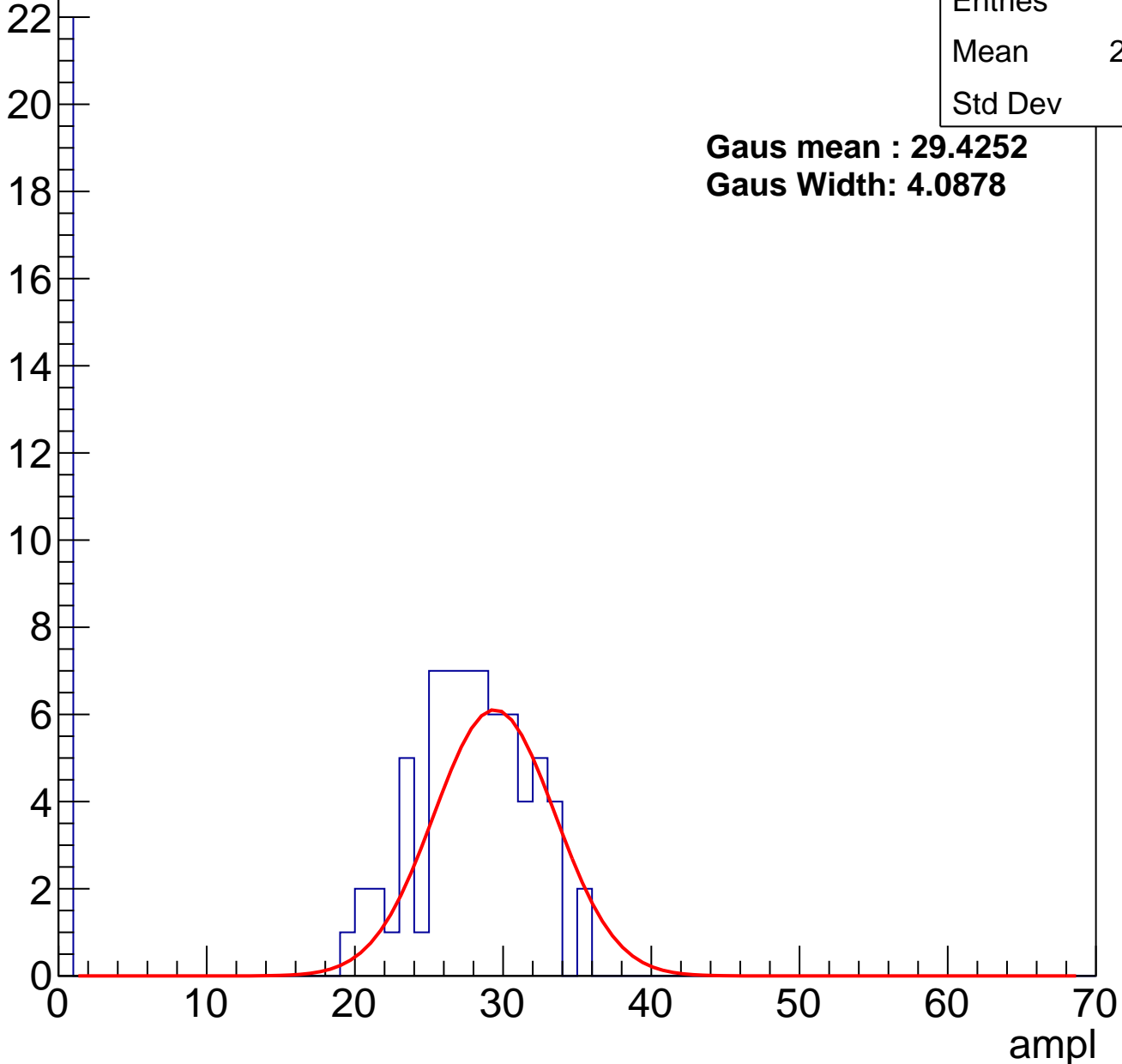
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	89
Mean	20.72
Std Dev	12.3

**Gaus mean : 29.4252**

**Gaus Width: 4.0878**

Entry



# B1L103S, U26-ch26, adc1

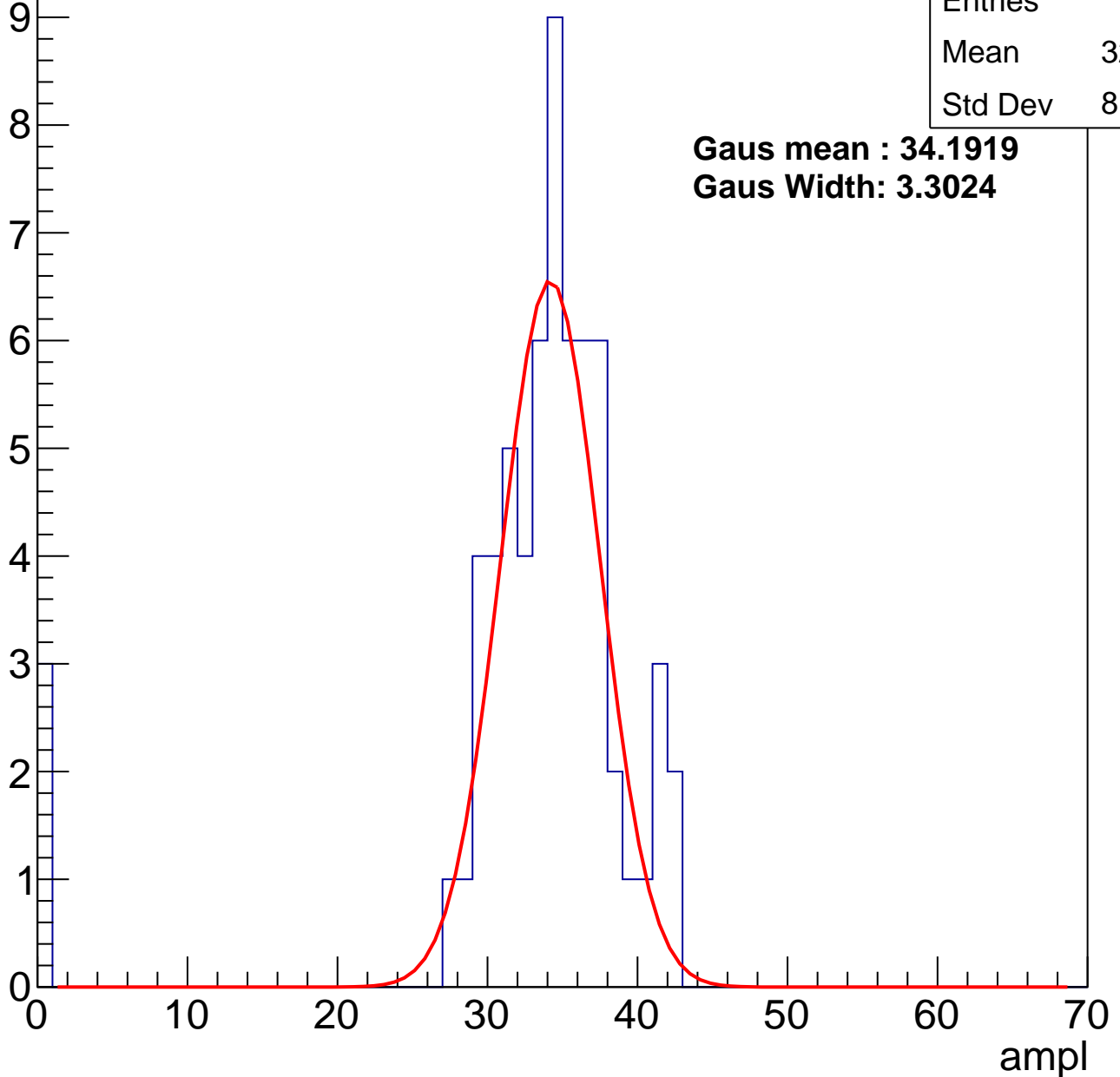
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	64
Mean	32.62
Std Dev	8.019

**Gaus mean : 34.1919**

**Gaus Width: 3.3024**



# B1L103S, U26-ch26, adc2

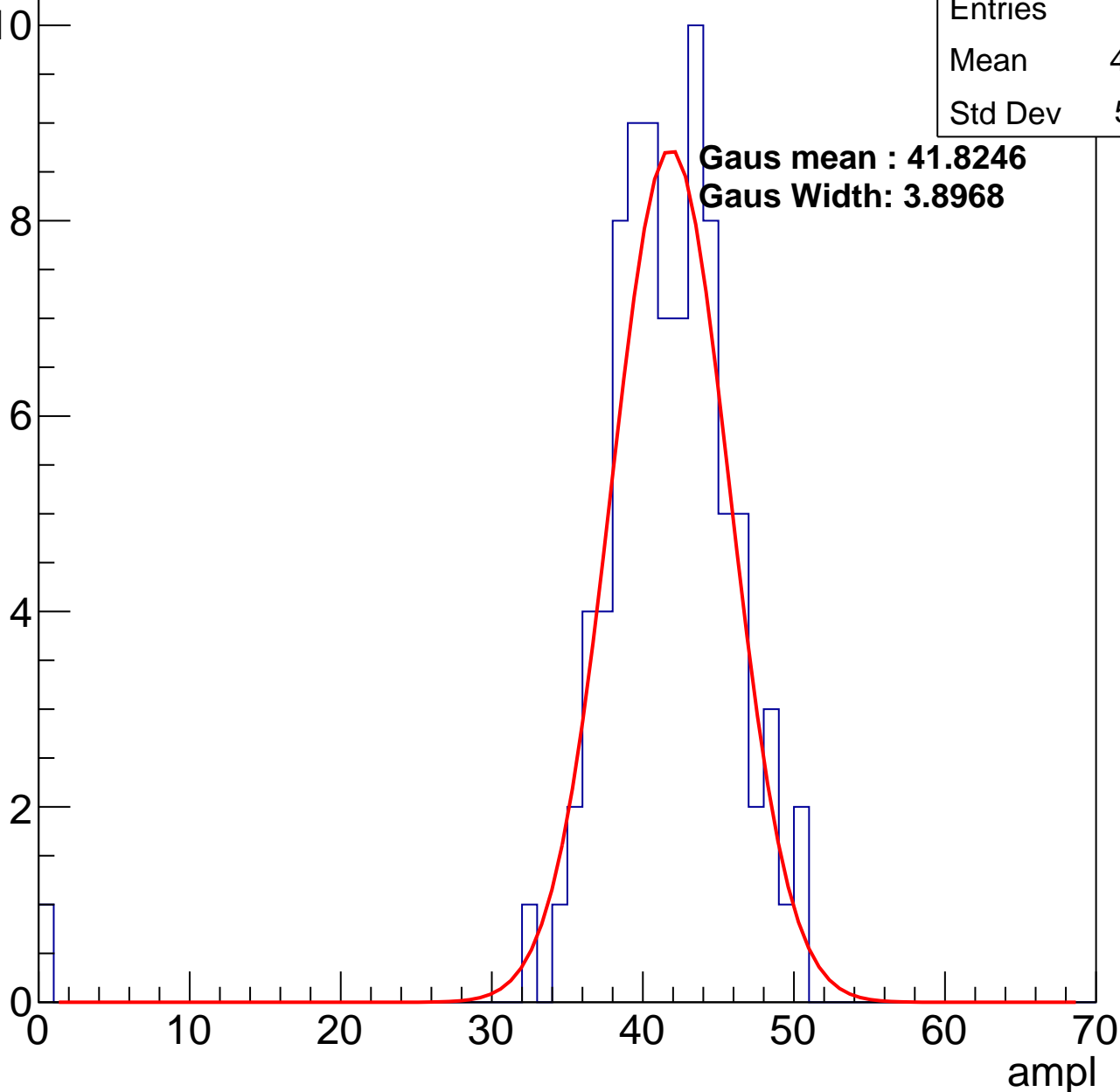
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	89
Mean	40.99
Std Dev	5.741

**Gaus mean : 41.8246**

**Gaus Width: 3.8968**

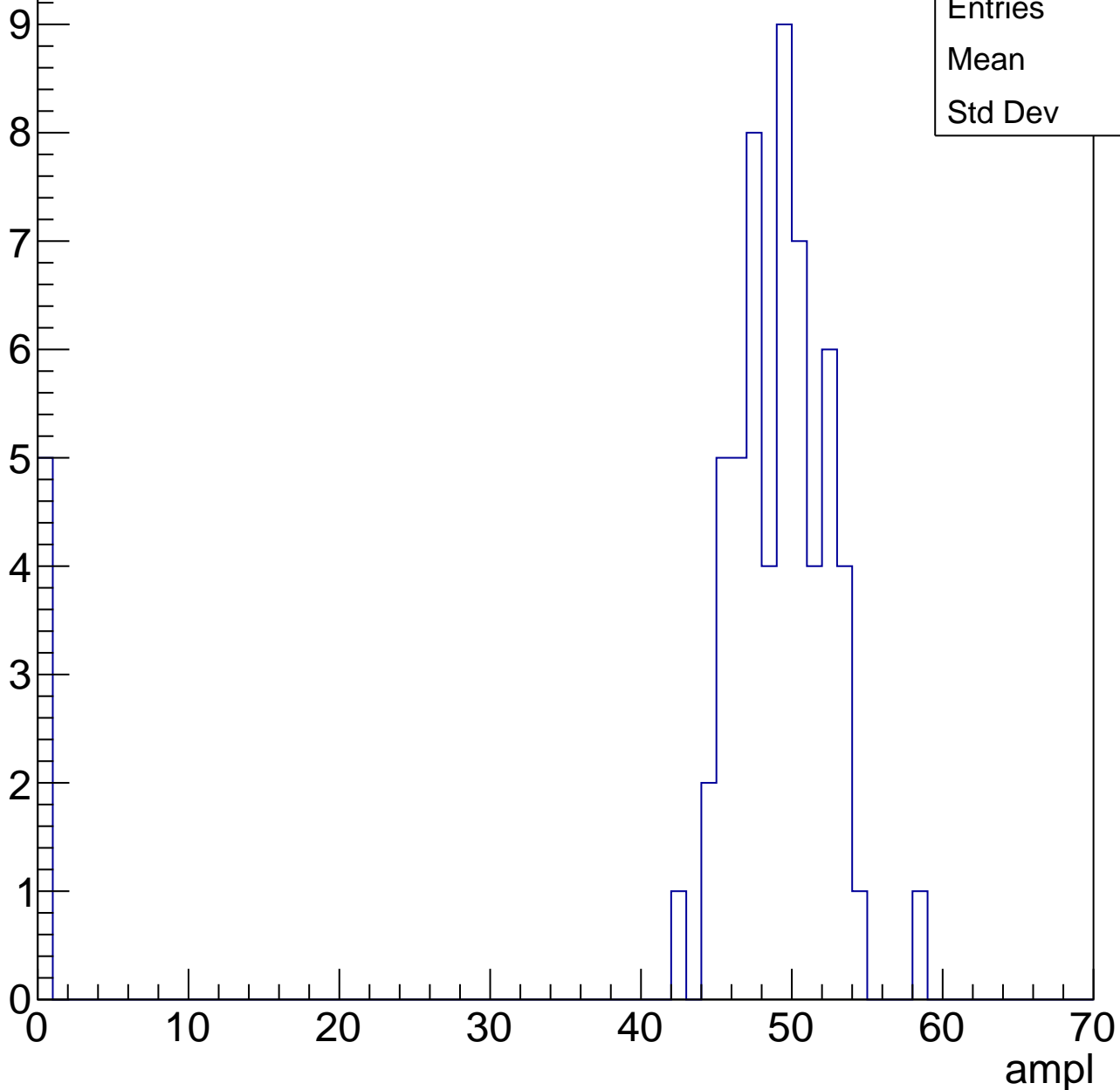


# B1L103S, U26-ch26, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	62
Mean	44.9
Std Dev	13.6

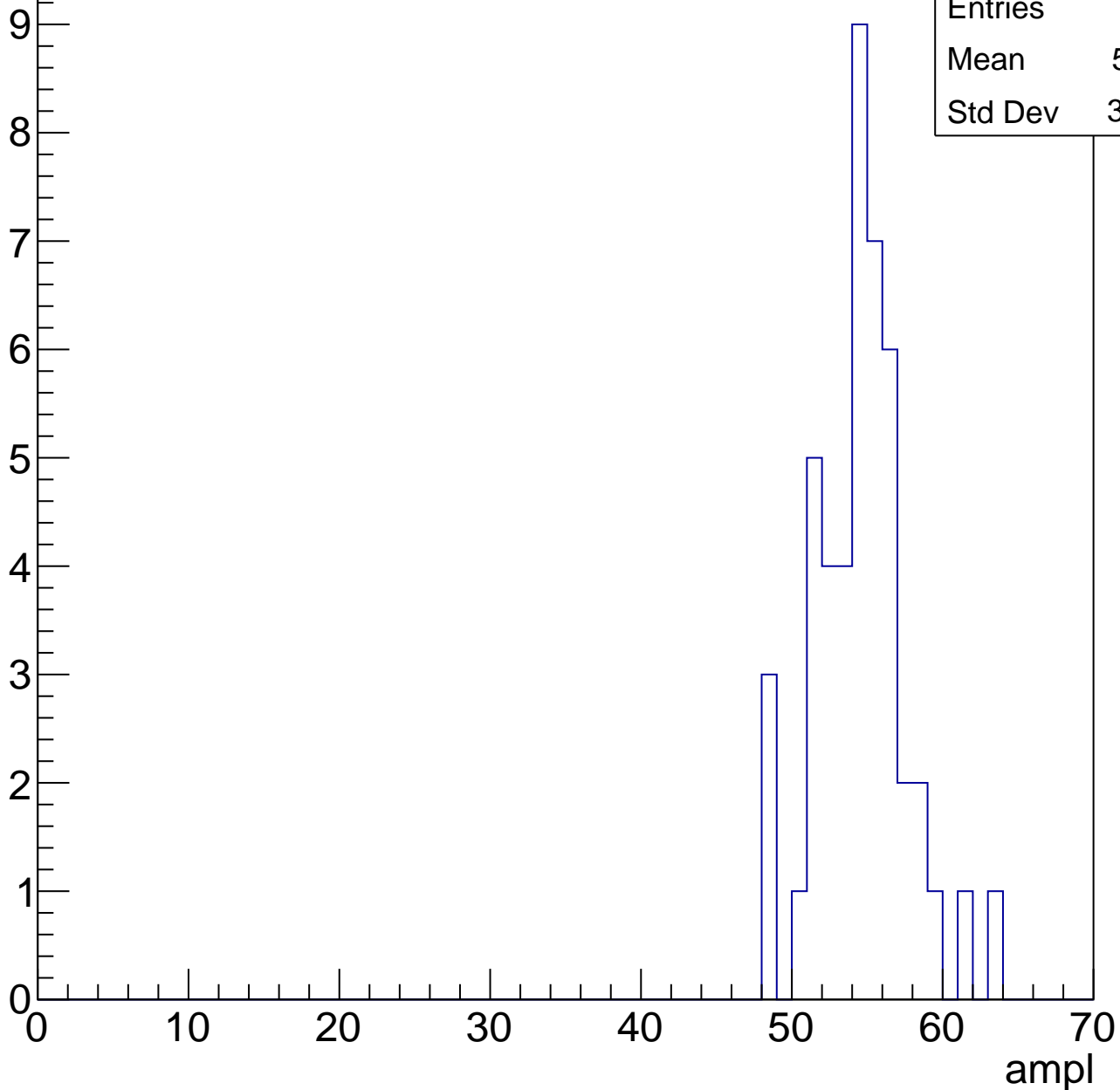


# B1L103S, U26-ch26, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	46
Mean	54.11
Std Dev	3.038

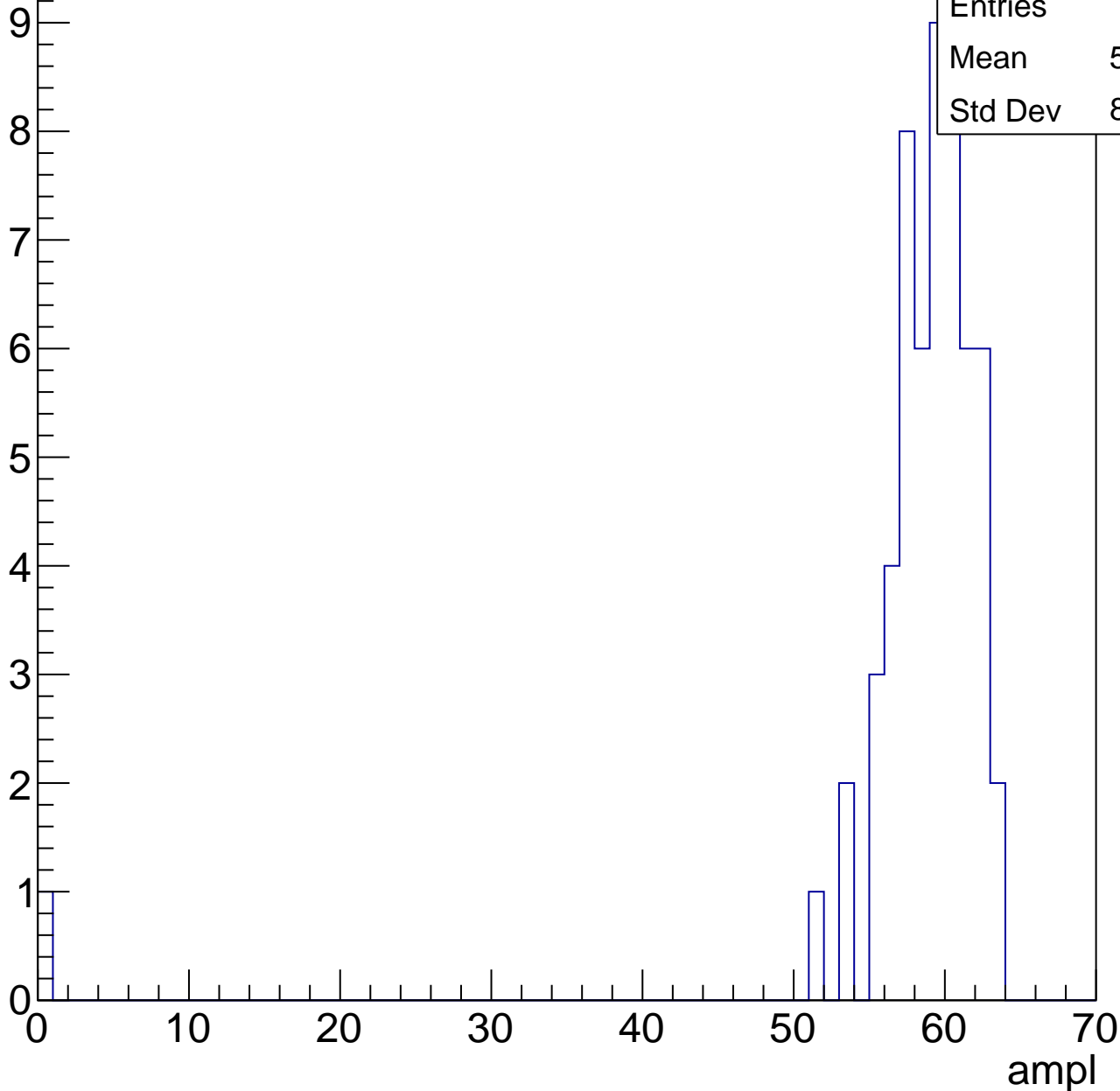


# B1L103S, U26-ch26, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	57
Mean	57.63
Std Dev	8.112

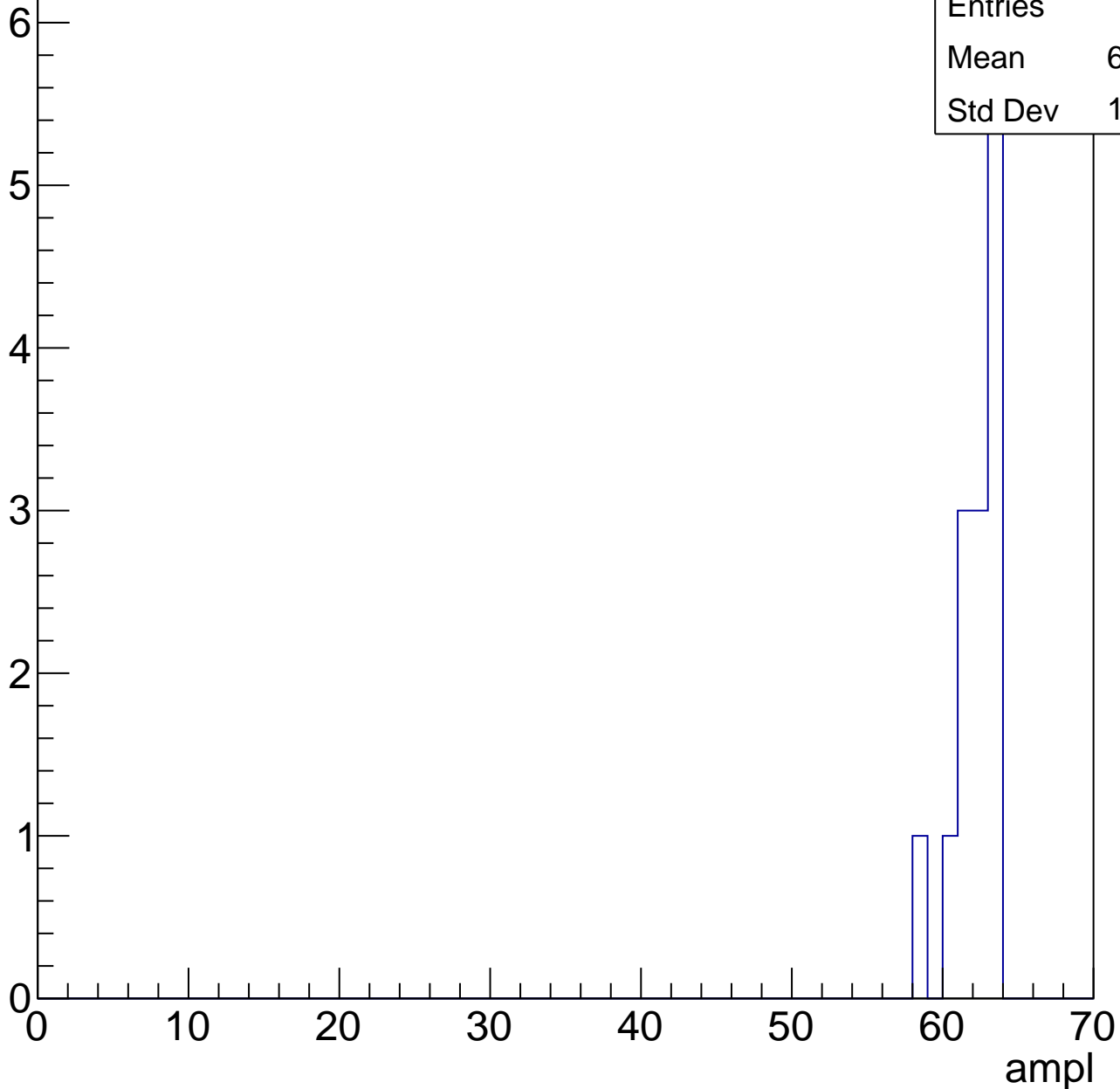


# B1L103S, U26-ch26, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	14
Mean	61.79
Std Dev	1.423





# B1L103S, U26-ch26, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	21
Mean	5.952
Std Dev	18.35

Entry



# B1L103S, U26-ch27, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	66
Mean	22.67
Std Dev	10.57

**Gaus mean : 27.1836**

**Gaus Width: 4.0948**

Entry

10

8

6

4

2

0

0

10

20

30

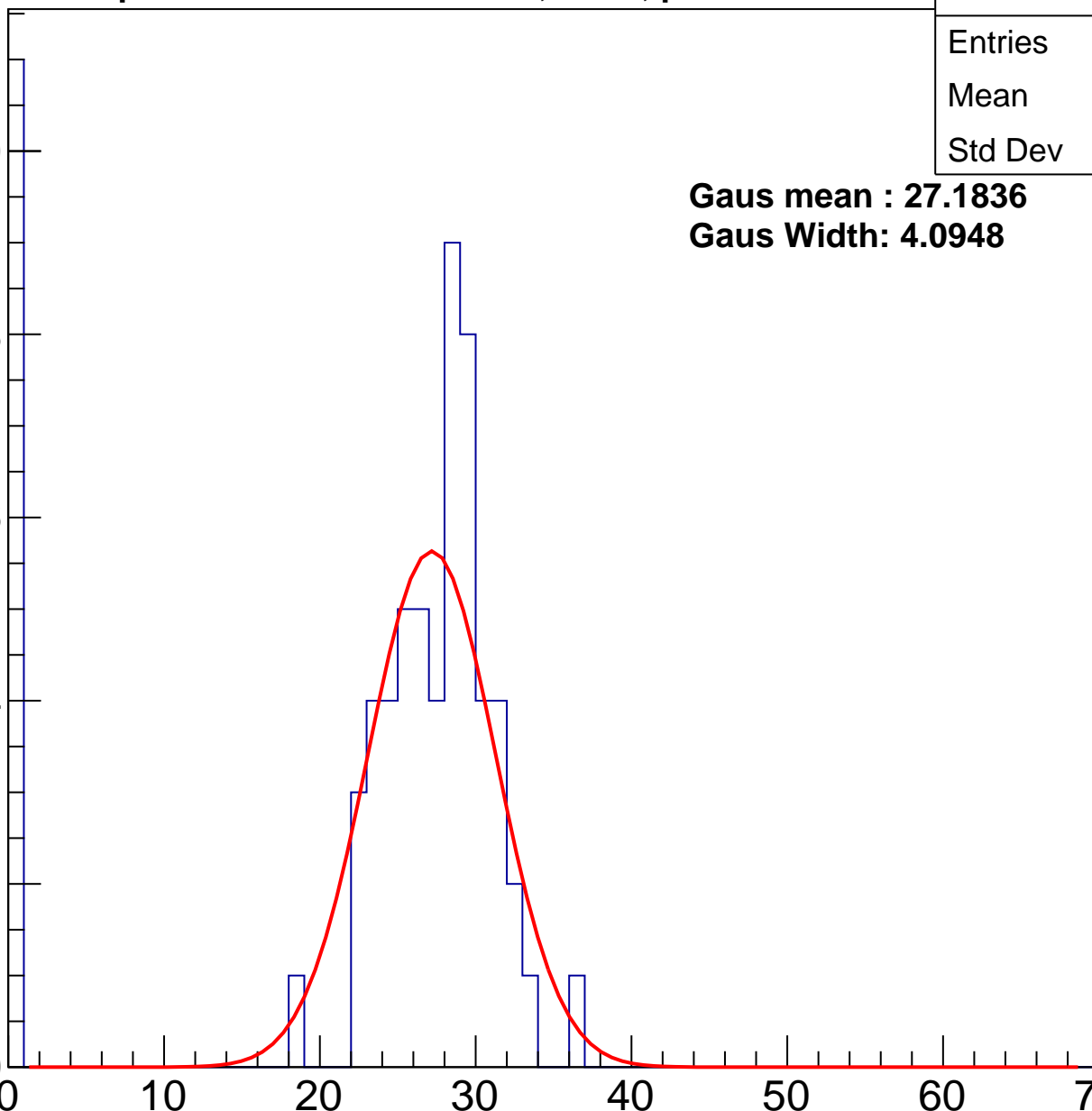
40

50

60

70

ampl



# B1L103S, U26-ch27, adc1

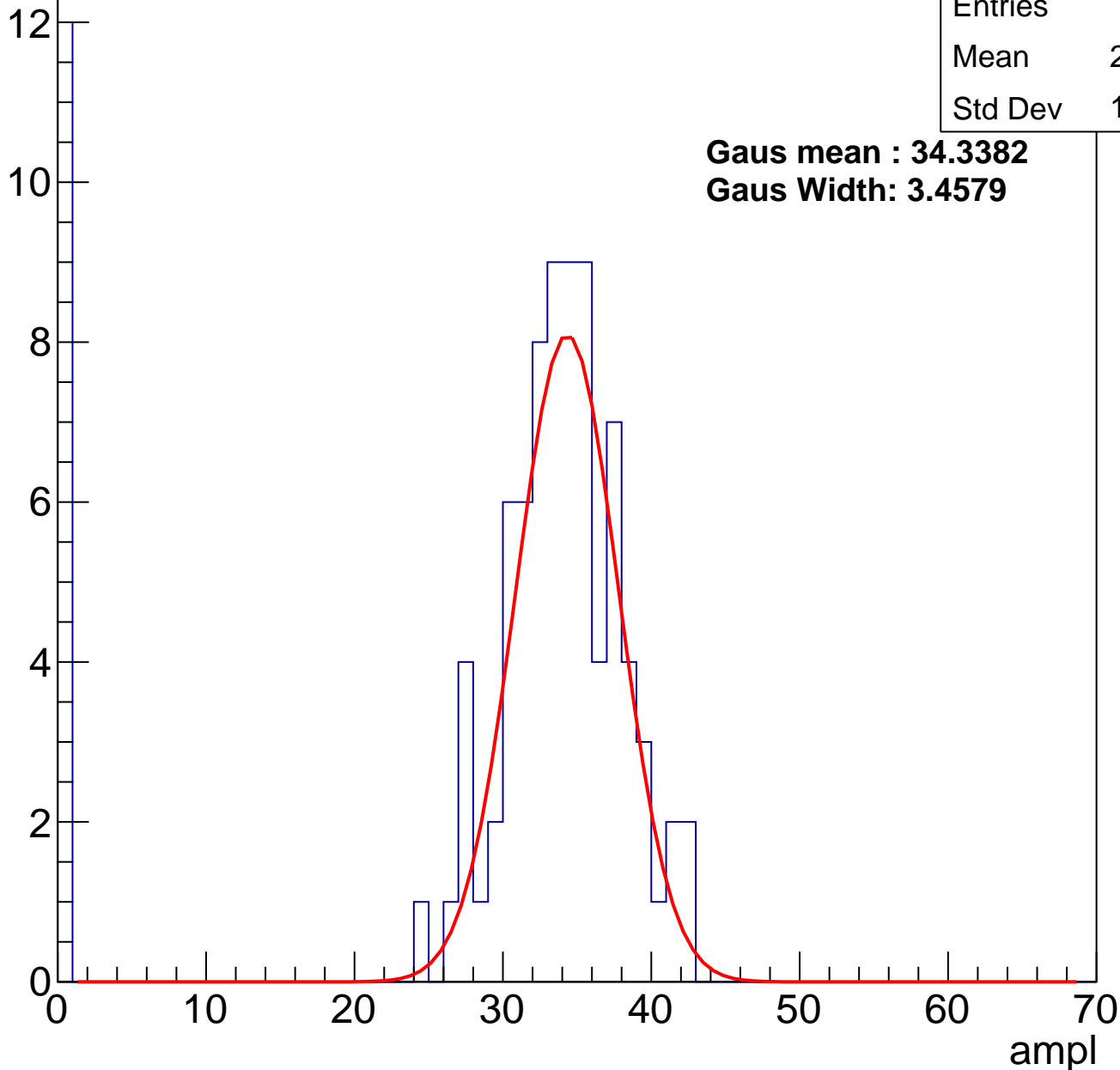
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	91
Mean	29.25
Std Dev	11.93

**Gaus mean : 34.3382**

**Gaus Width: 3.4579**

Entry



# B1L103S, U26-ch27, adc2

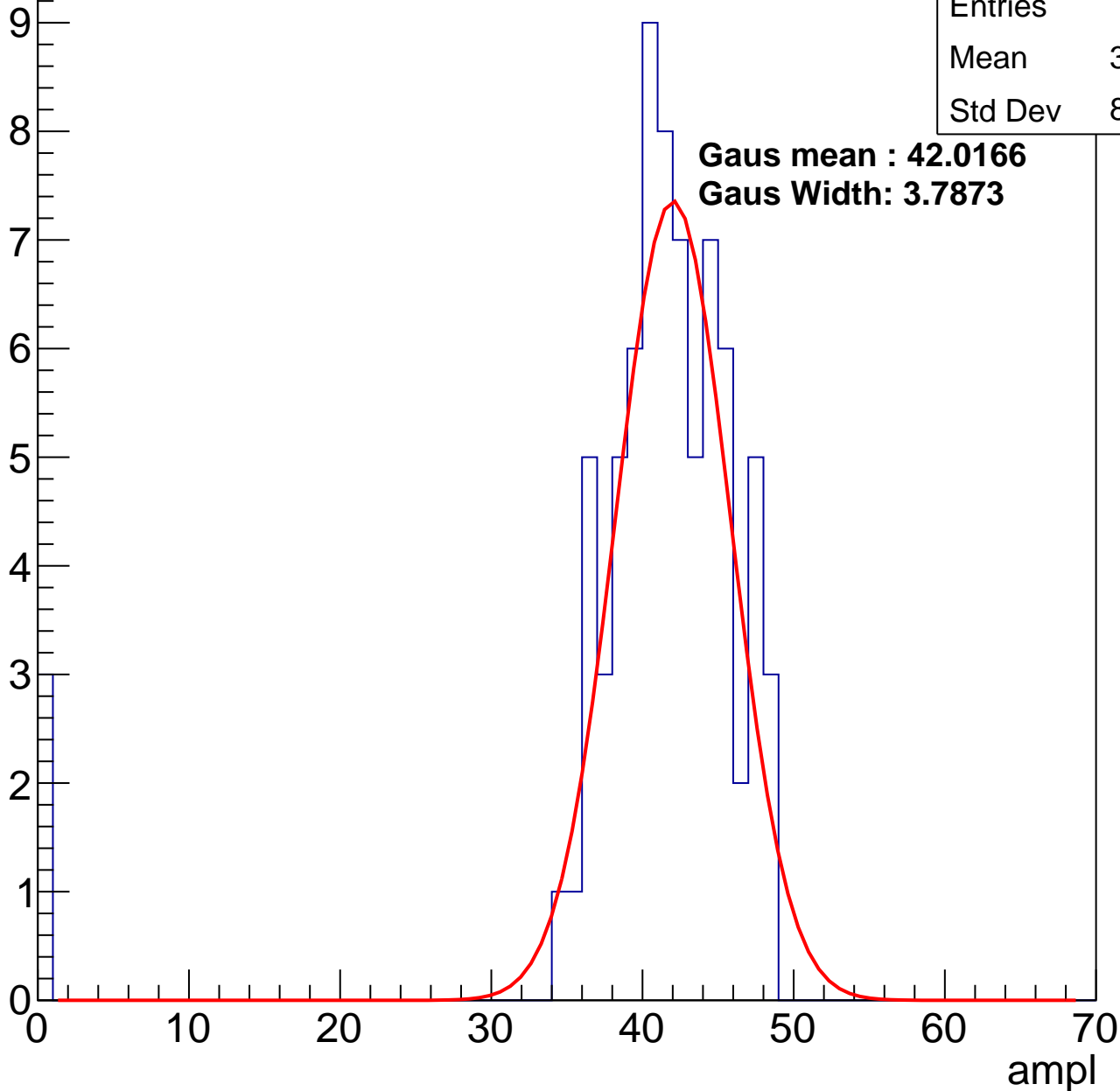
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	76
Mean	39.87
Std Dev	8.769

**Gaus mean : 42.0166**

**Gaus Width: 3.7873**

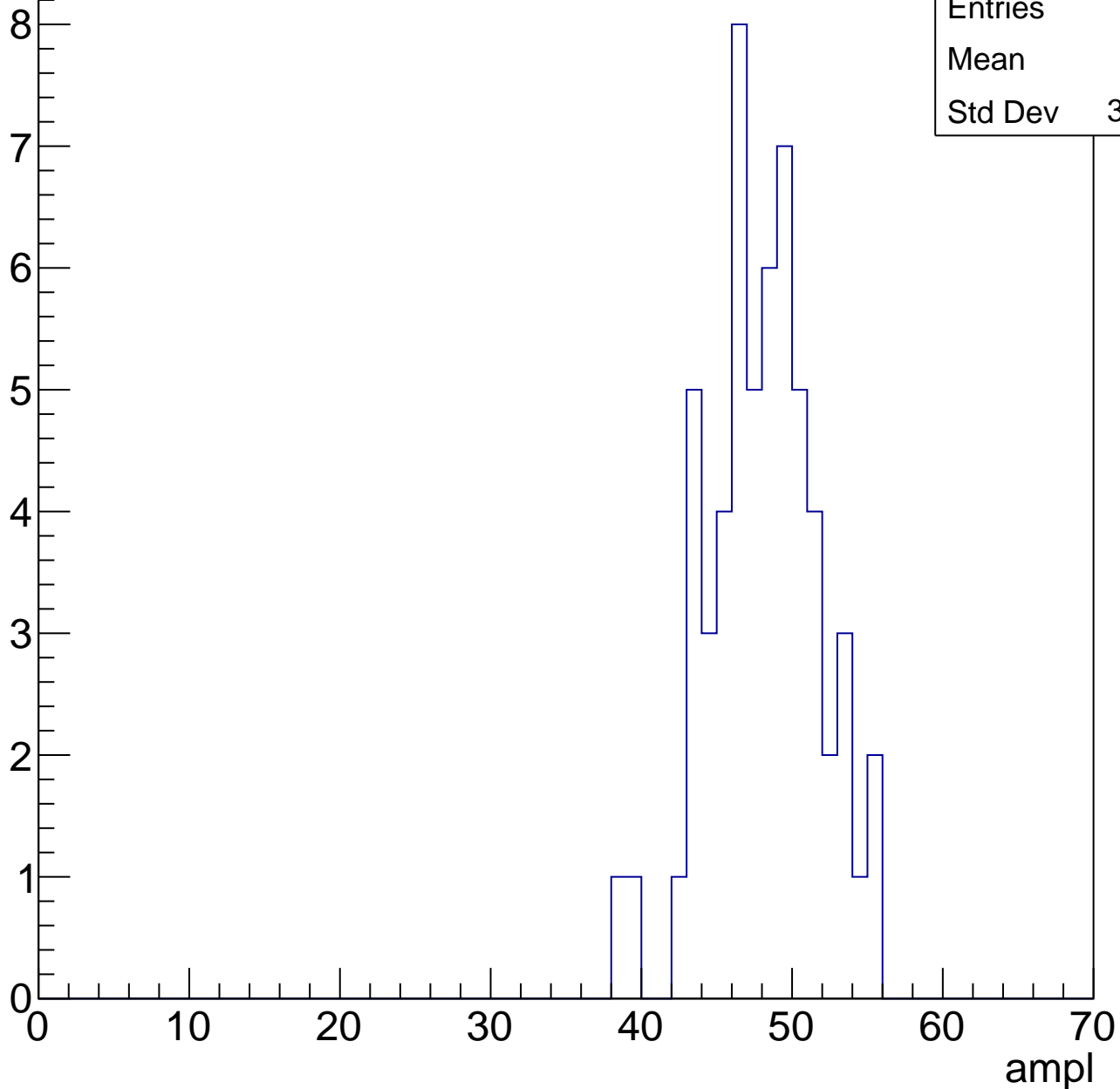


# B1L103S, U26-ch27, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	58
Mean	47.6
Std Dev	3.615

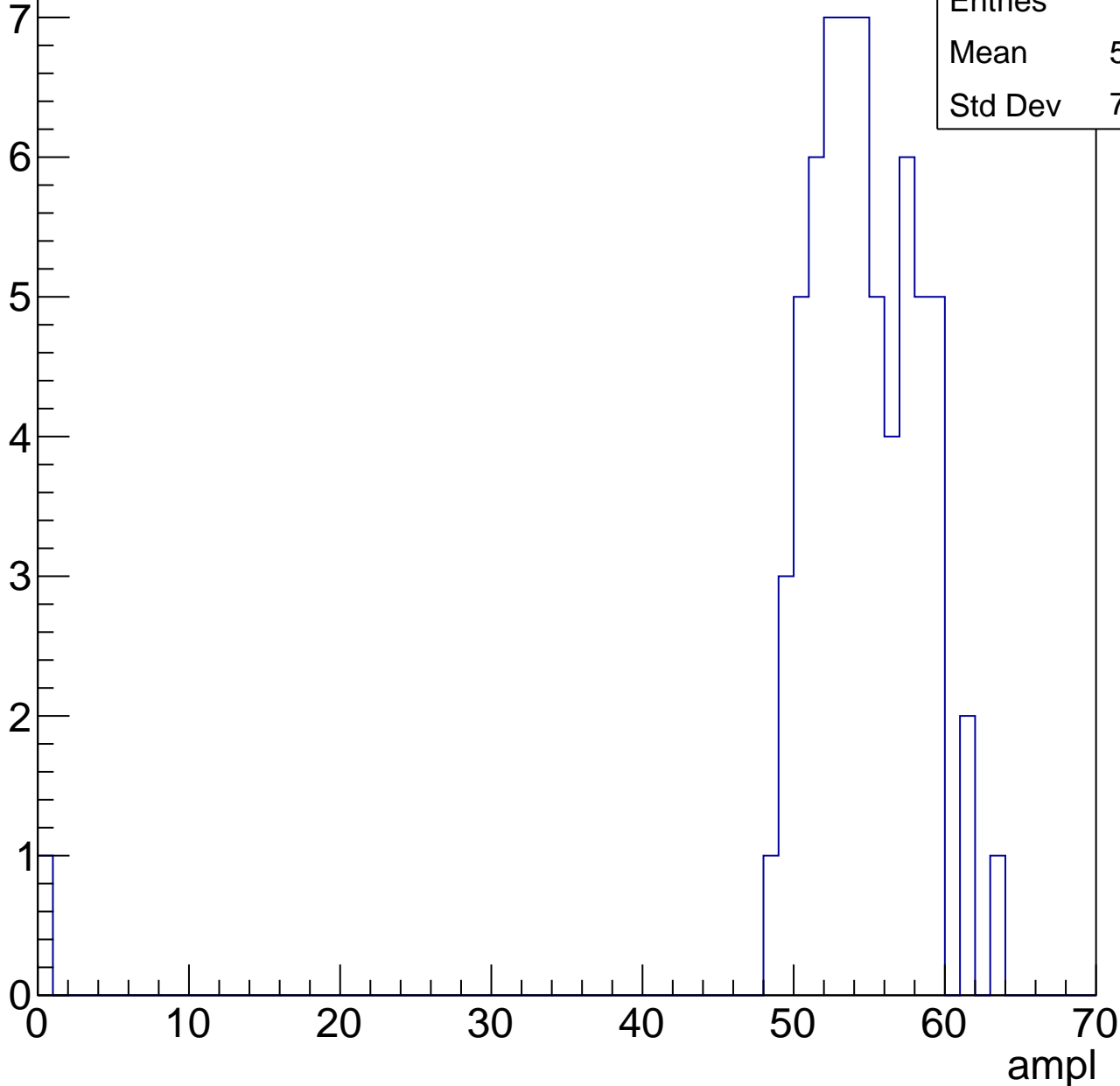


# B1L103S, U26-ch27, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	65
Mean	53.46
Std Dev	7.479

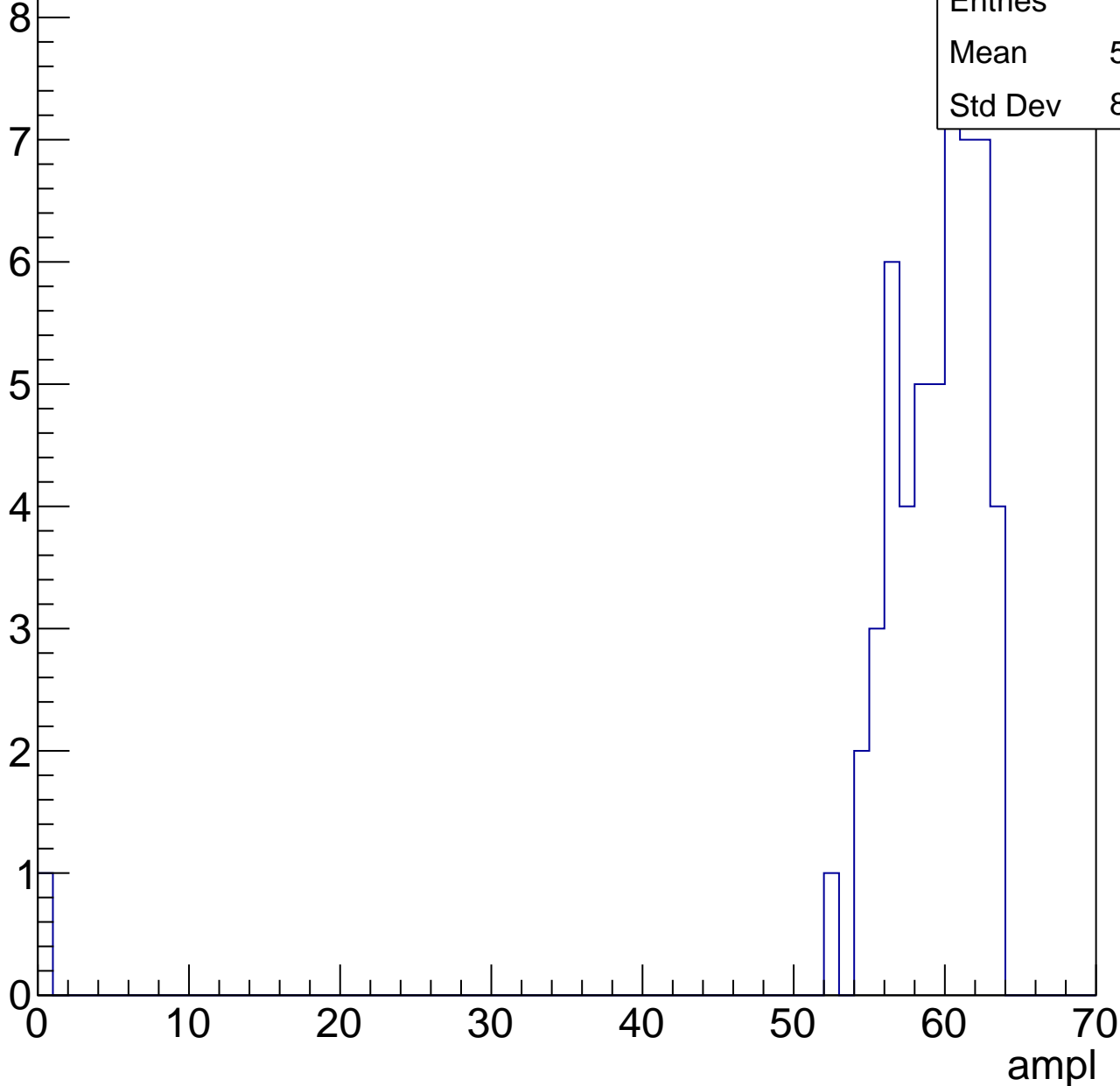


# B1L103S, U26-ch27, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	53
Mean	57.87
Std Dev	8.465

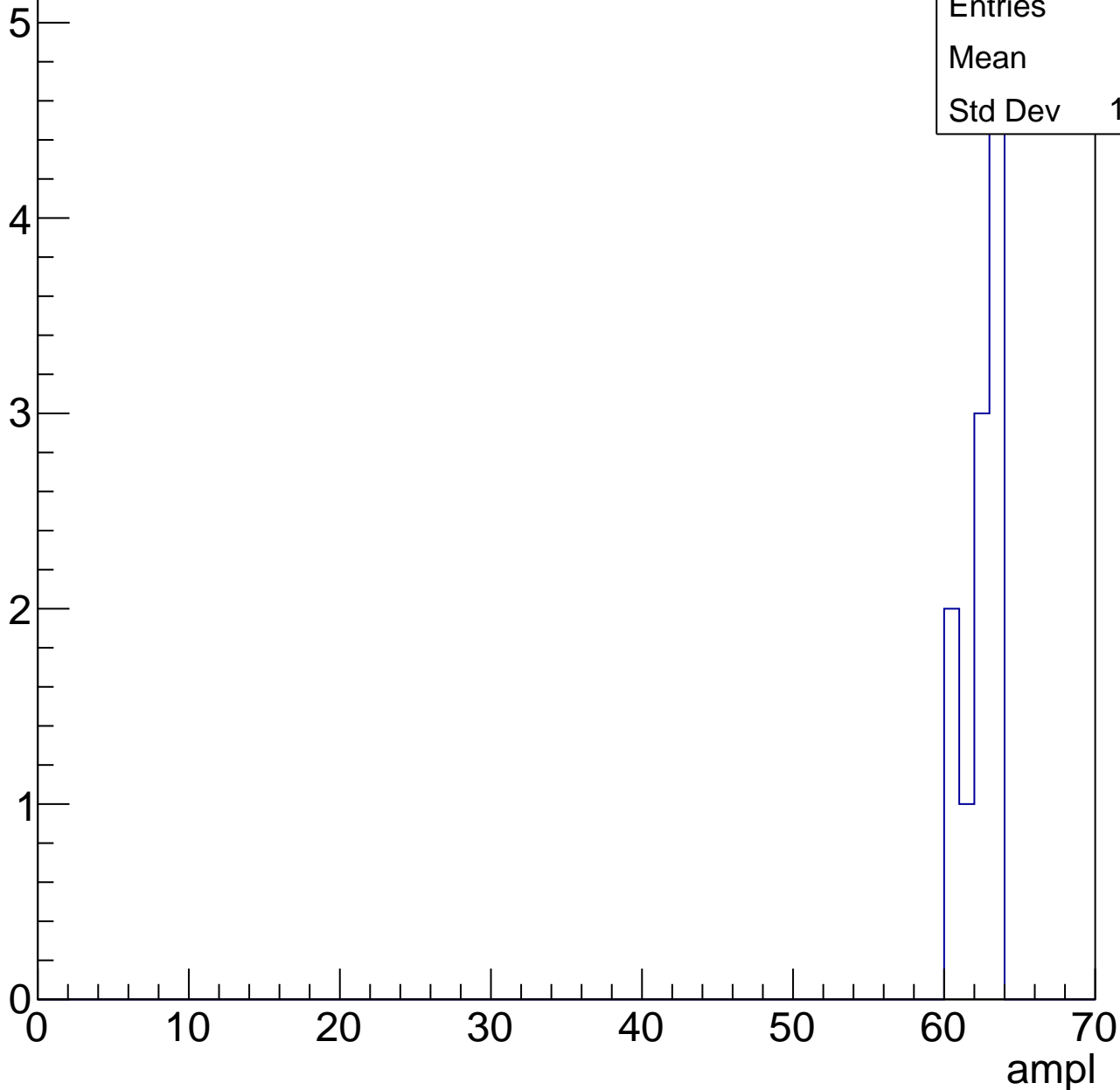


# B1L103S, U26-ch27, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	11
Mean	62
Std Dev	1.128





# B1L103S, U26-ch27, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



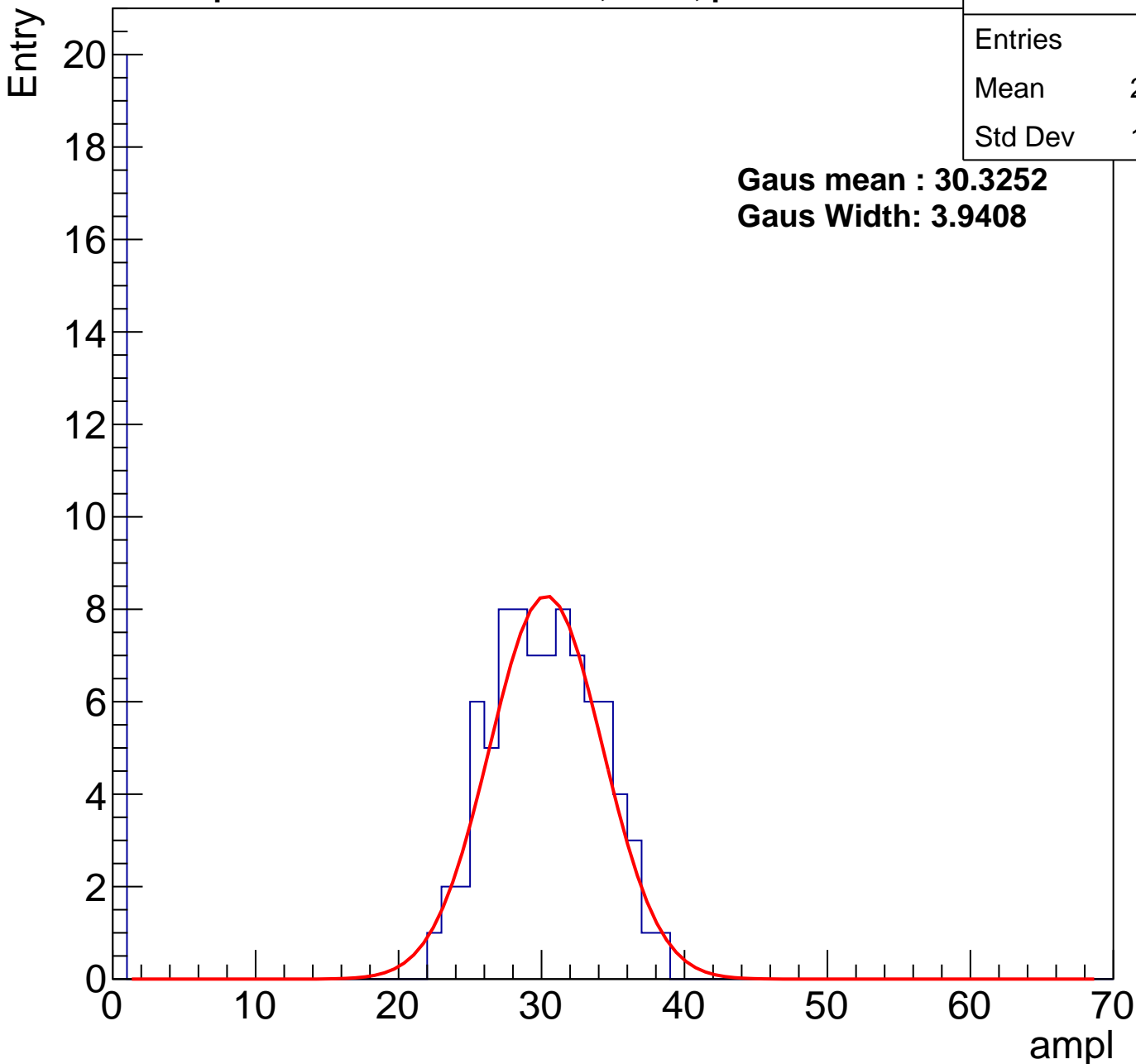
# B1L103S, U26-ch28, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	102
Mean	23.98
Std Dev	12.28

**Gaus mean : 30.3252**

**Gaus Width: 3.9408**



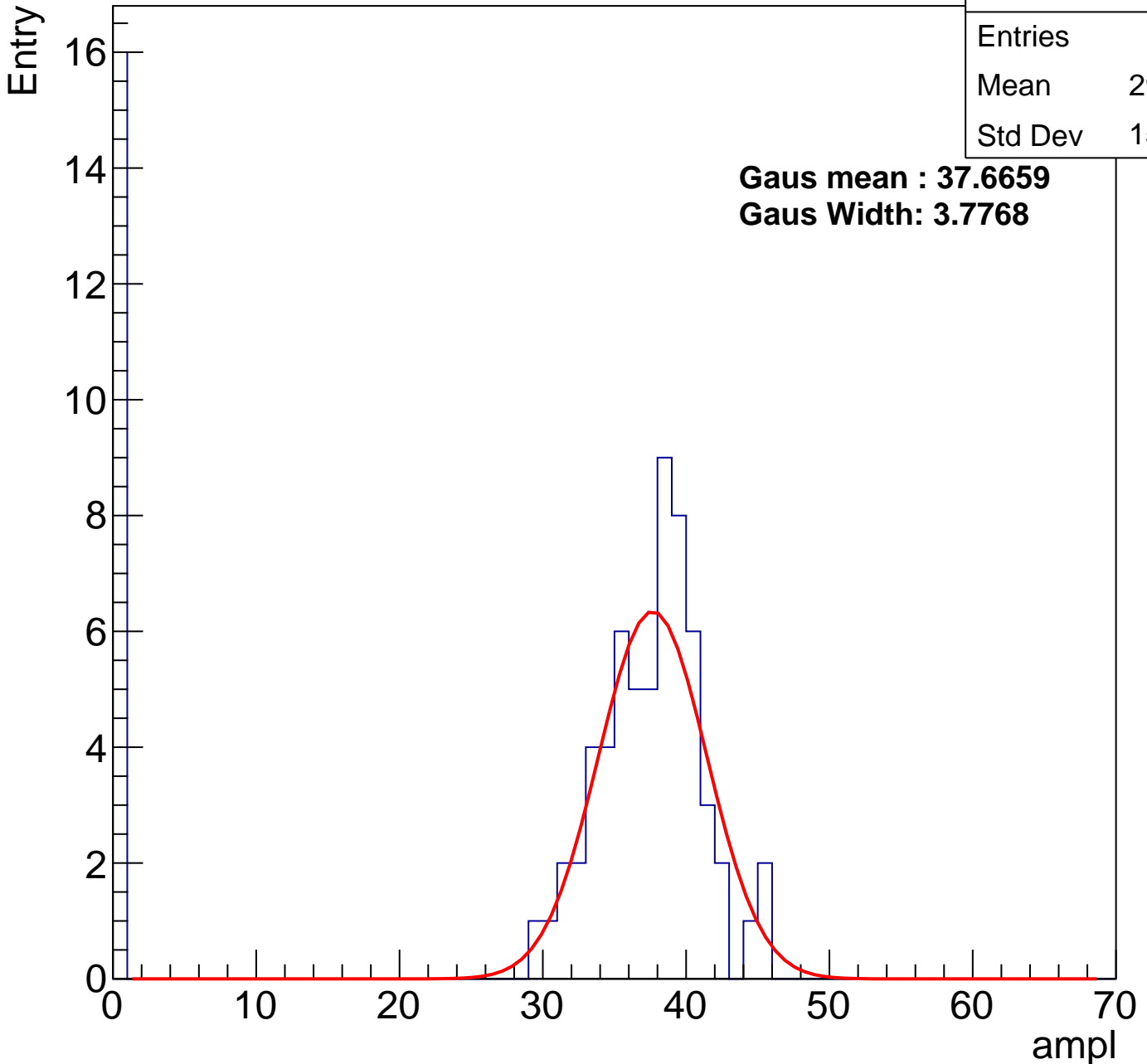
# B1L103S, U26-ch28, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	77
Mean	29.39
Std Dev	15.36

**Gaus mean : 37.6659**

**Gaus Width: 3.7768**



# B1L103S, U26-ch28, adc2

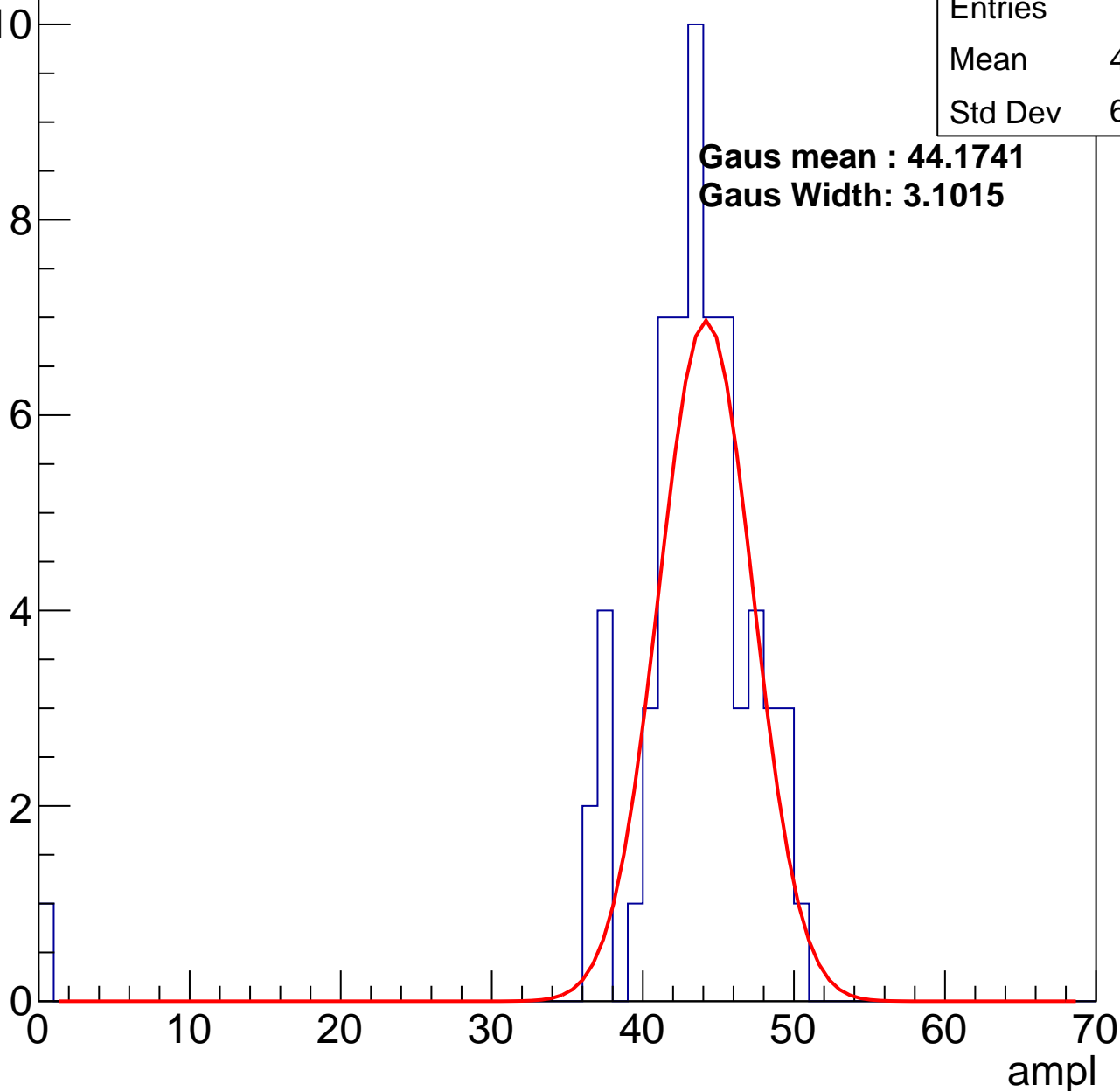
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	63
Mean	42.54
Std Dev	6.317

**Gaus mean : 44.1741**

**Gaus Width: 3.1015**

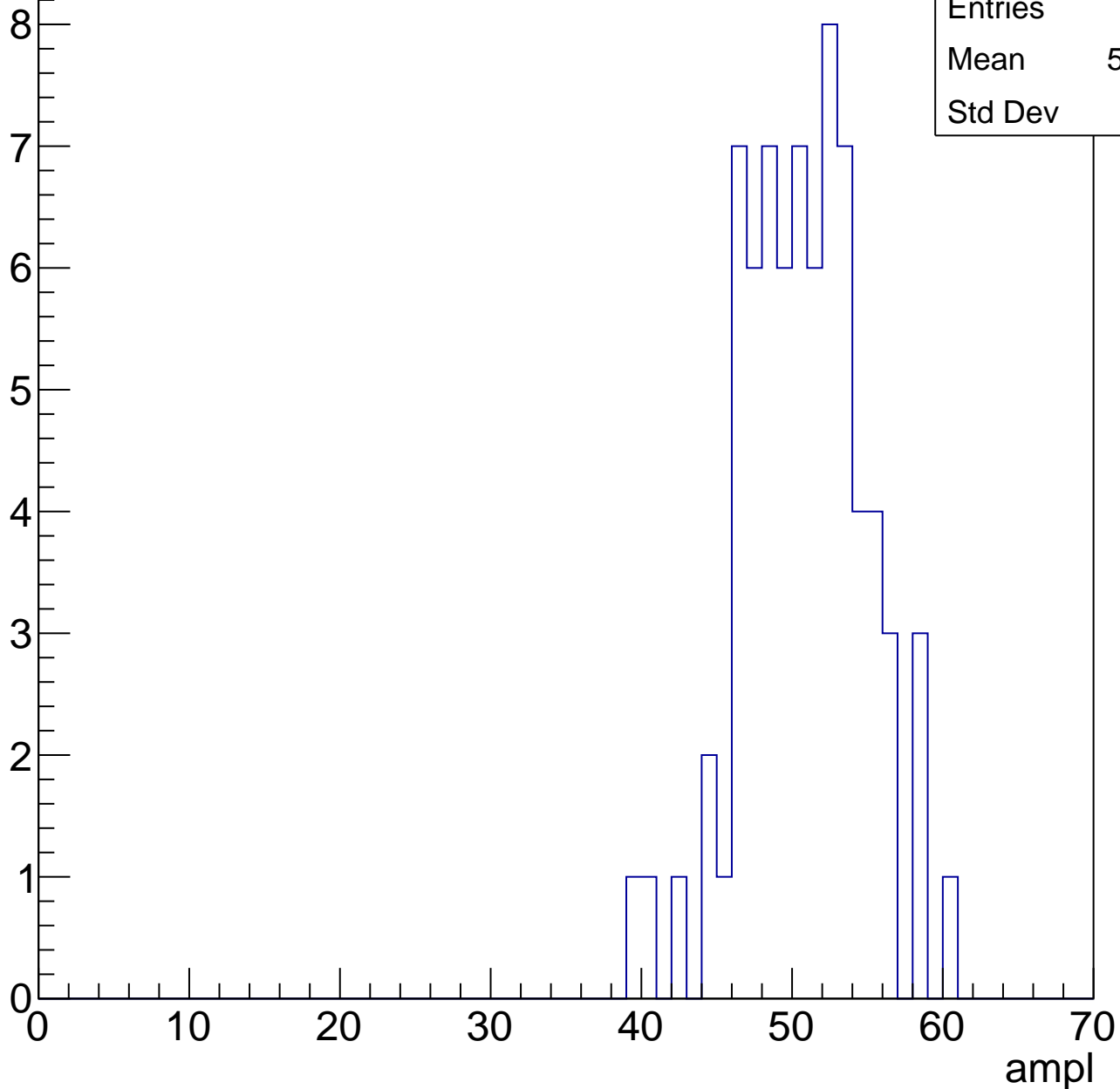


# B1L103S, U26-ch28, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	75
Mean	50.25
Std Dev	4.07

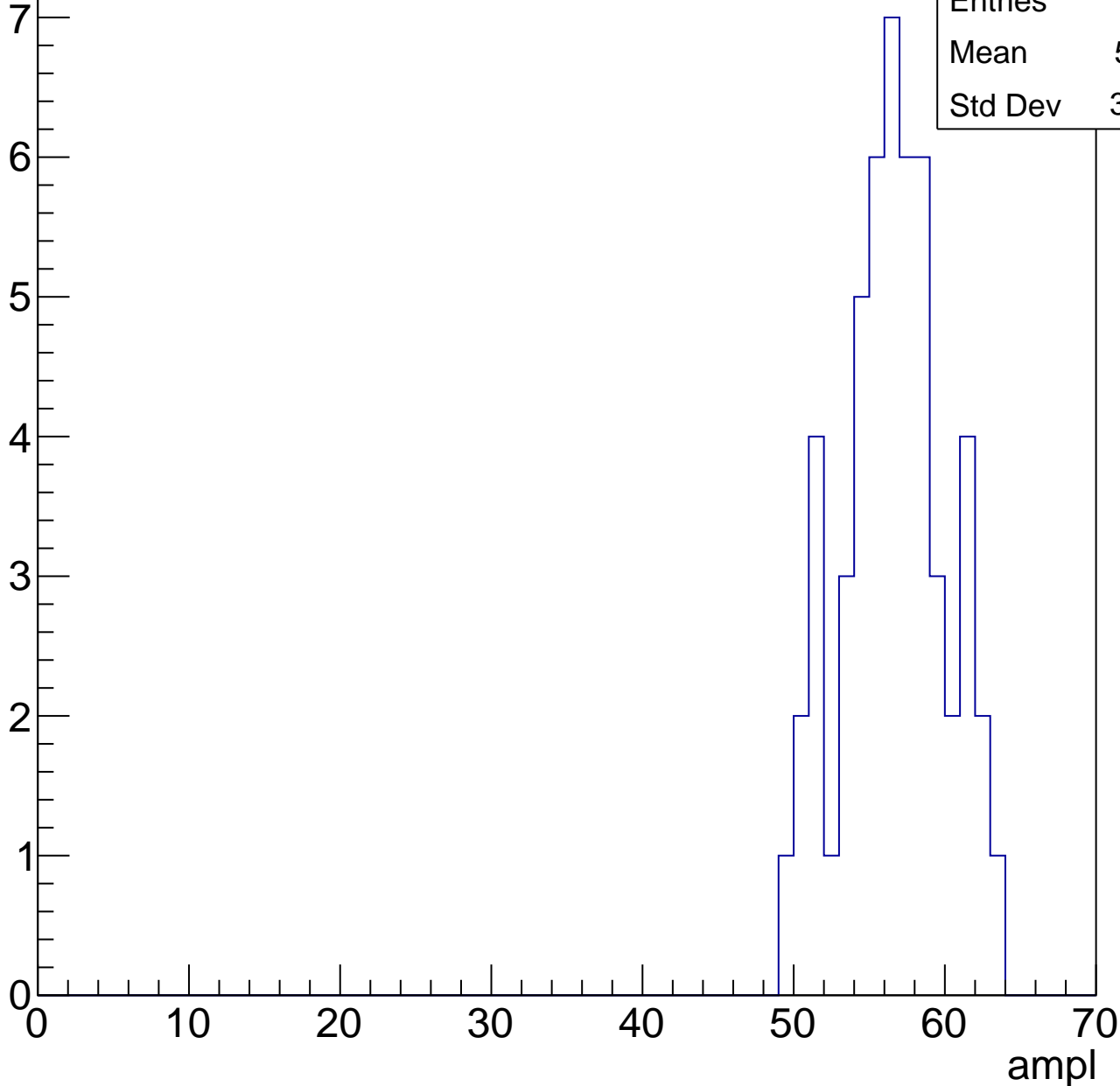


# B1L103S, U26-ch28, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

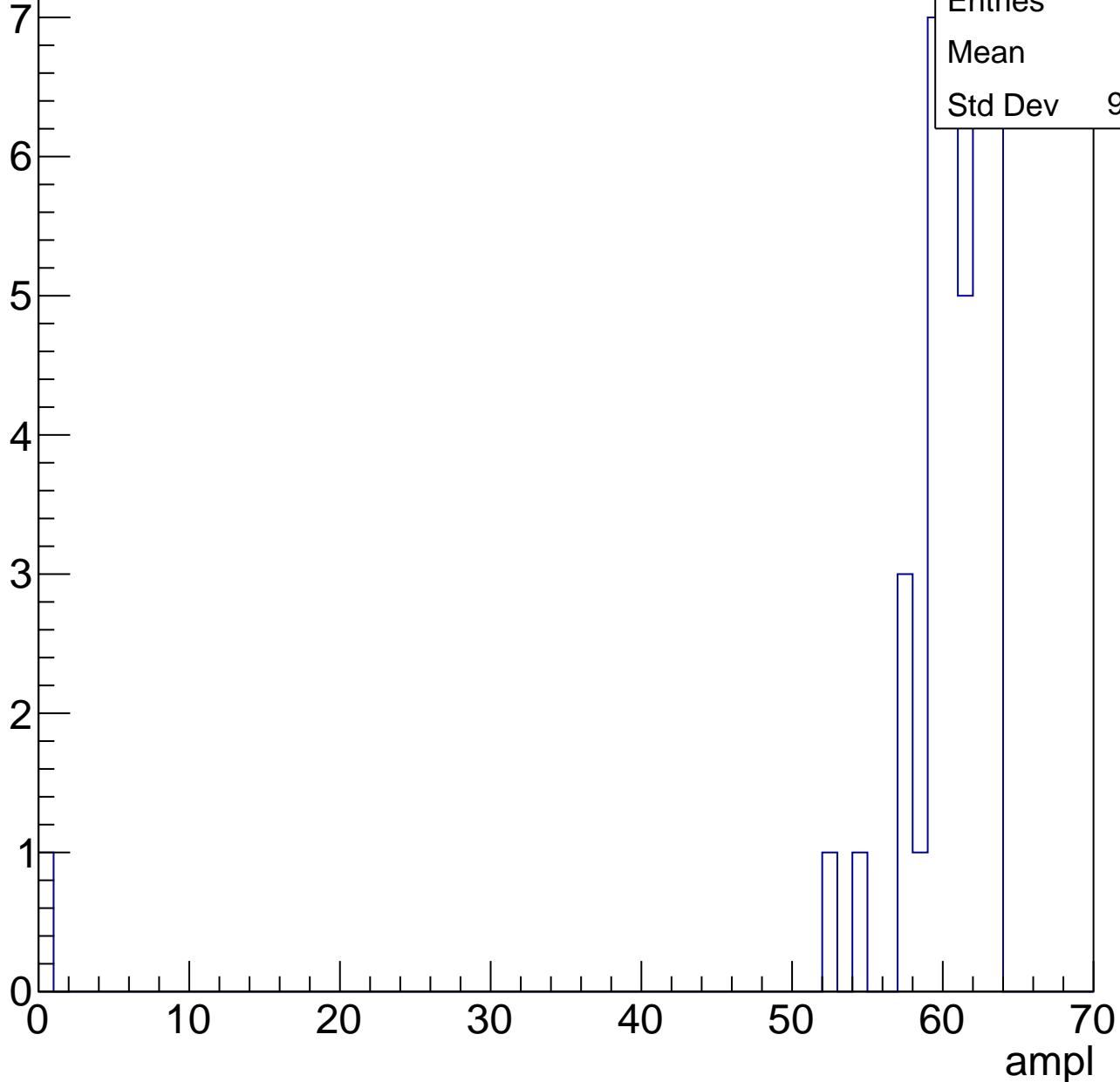
Entries	53
Mean	56.11
Std Dev	3.363



# B1L103S, U26-ch28, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

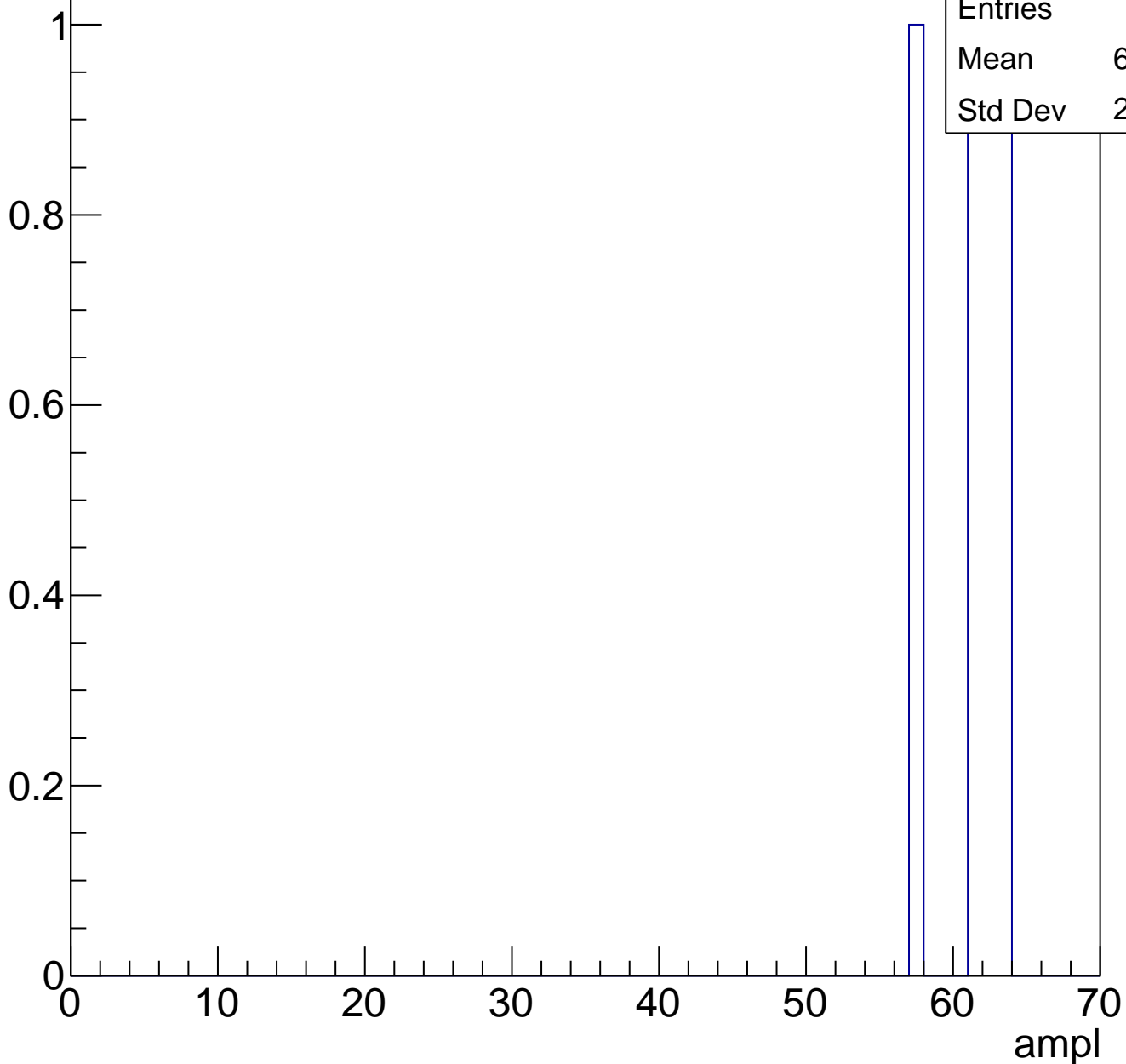
Entry



# B1L103S, U26-ch28, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry





# B1L103S, U26-ch28, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	20
Mean	3.15
Std Dev	13.73



# B1L103S, U26-ch29, adc0

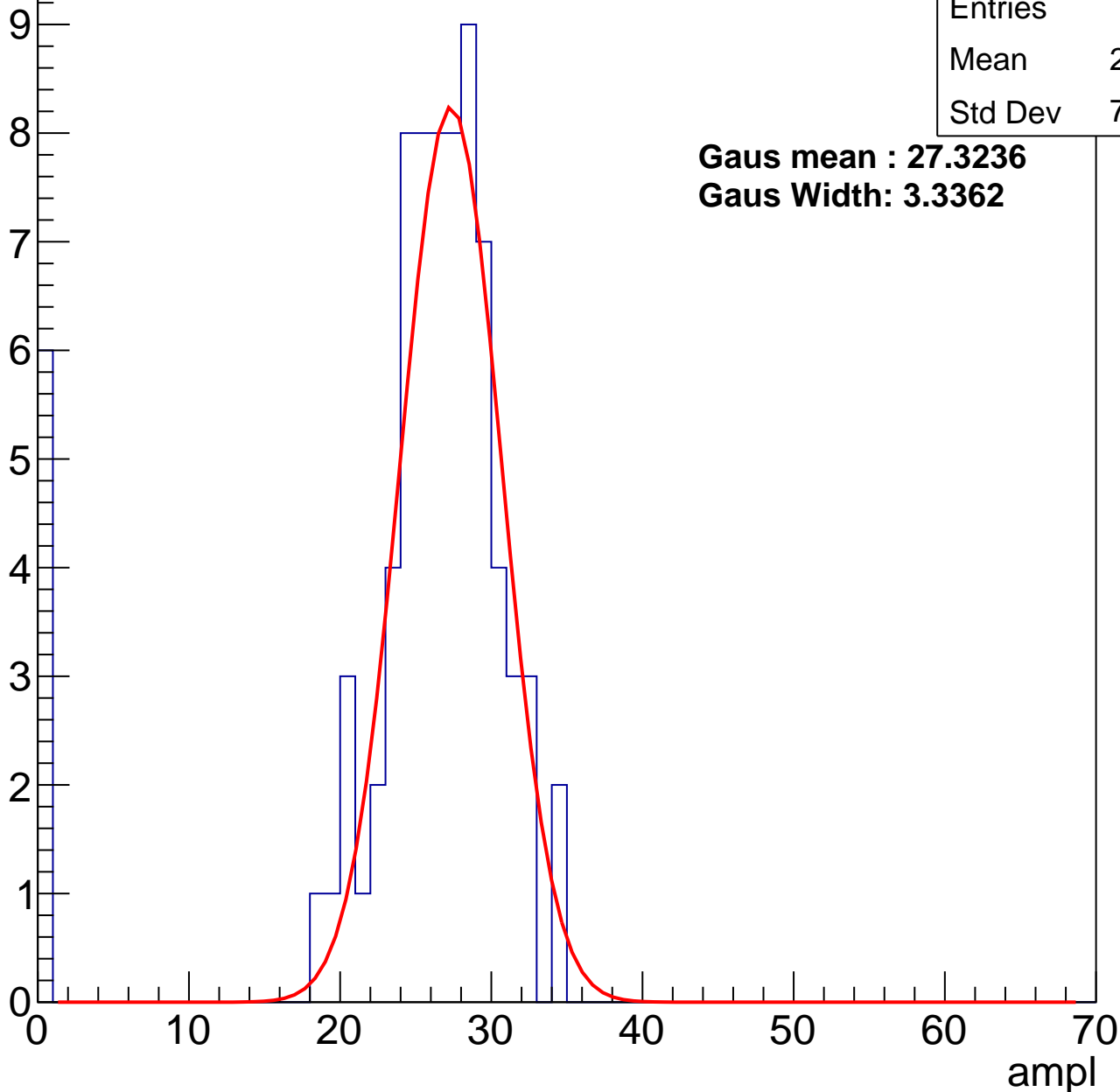
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	78
Mean	24.38
Std Dev	7.753

**Gaus mean : 27.3236**

**Gaus Width: 3.3362**



# B1L103S, U26-ch29, adc1

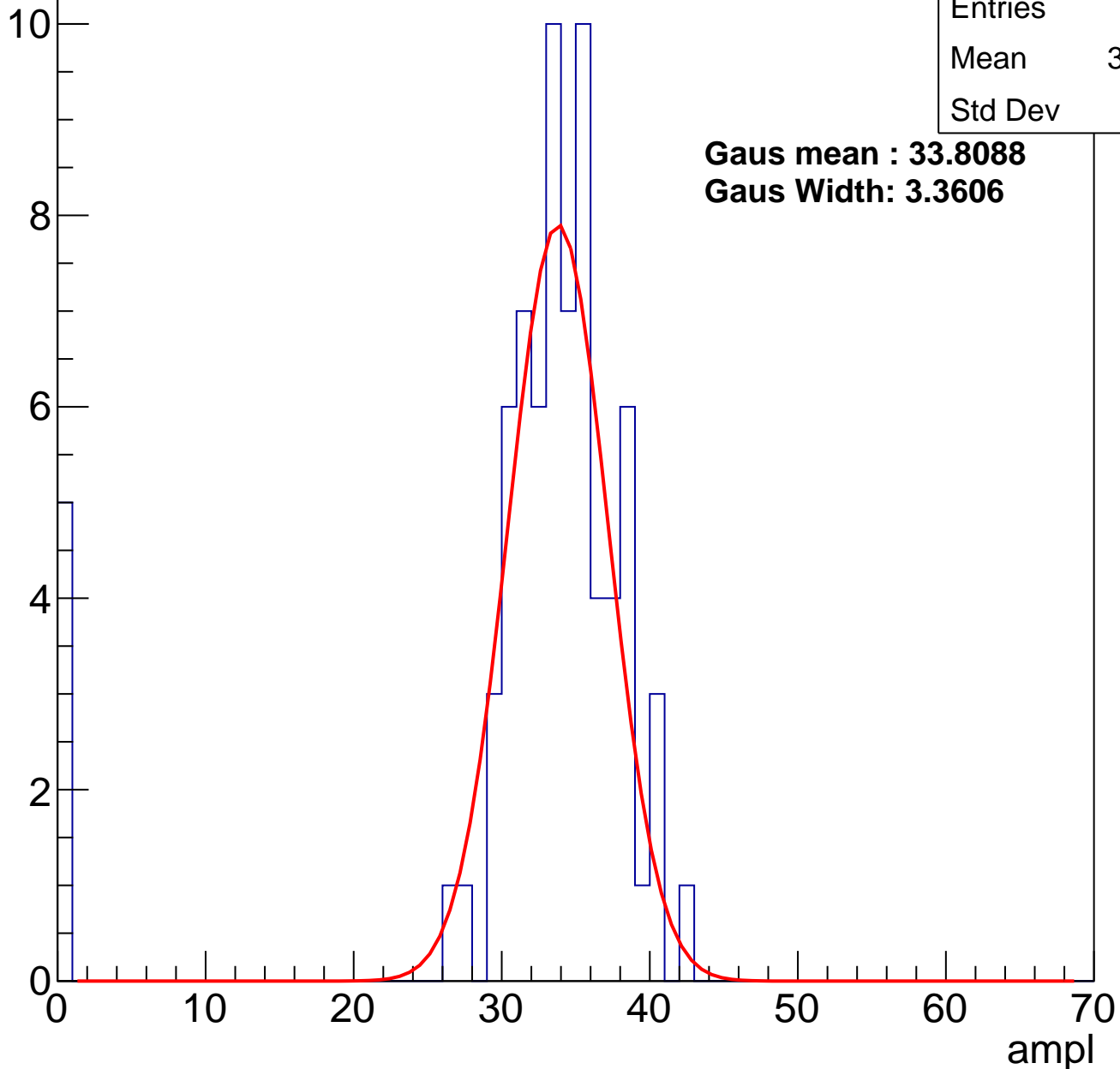
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	75
Mean	31.57
Std Dev	9

**Gaus mean : 33.8088**

**Gaus Width: 3.3606**

Entry



# B1L103S, U26-ch29, adc2

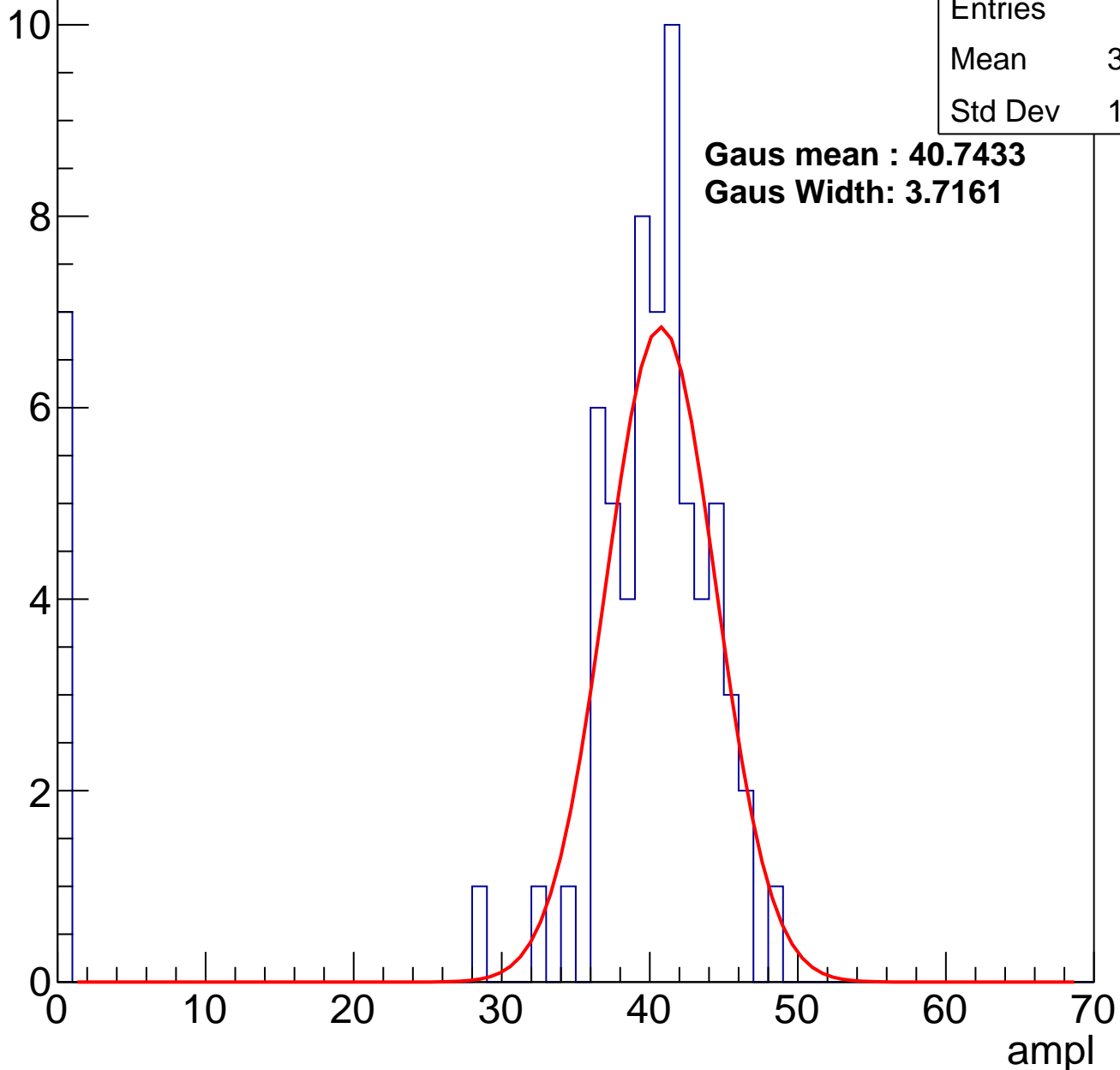
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	70
Mean	36.09
Std Dev	12.47

**Gaus mean : 40.7433**

**Gaus Width: 3.7161**

Entry



# B1L103S, U26-ch29, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	66
Mean	46.71
Std Dev	3.237

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

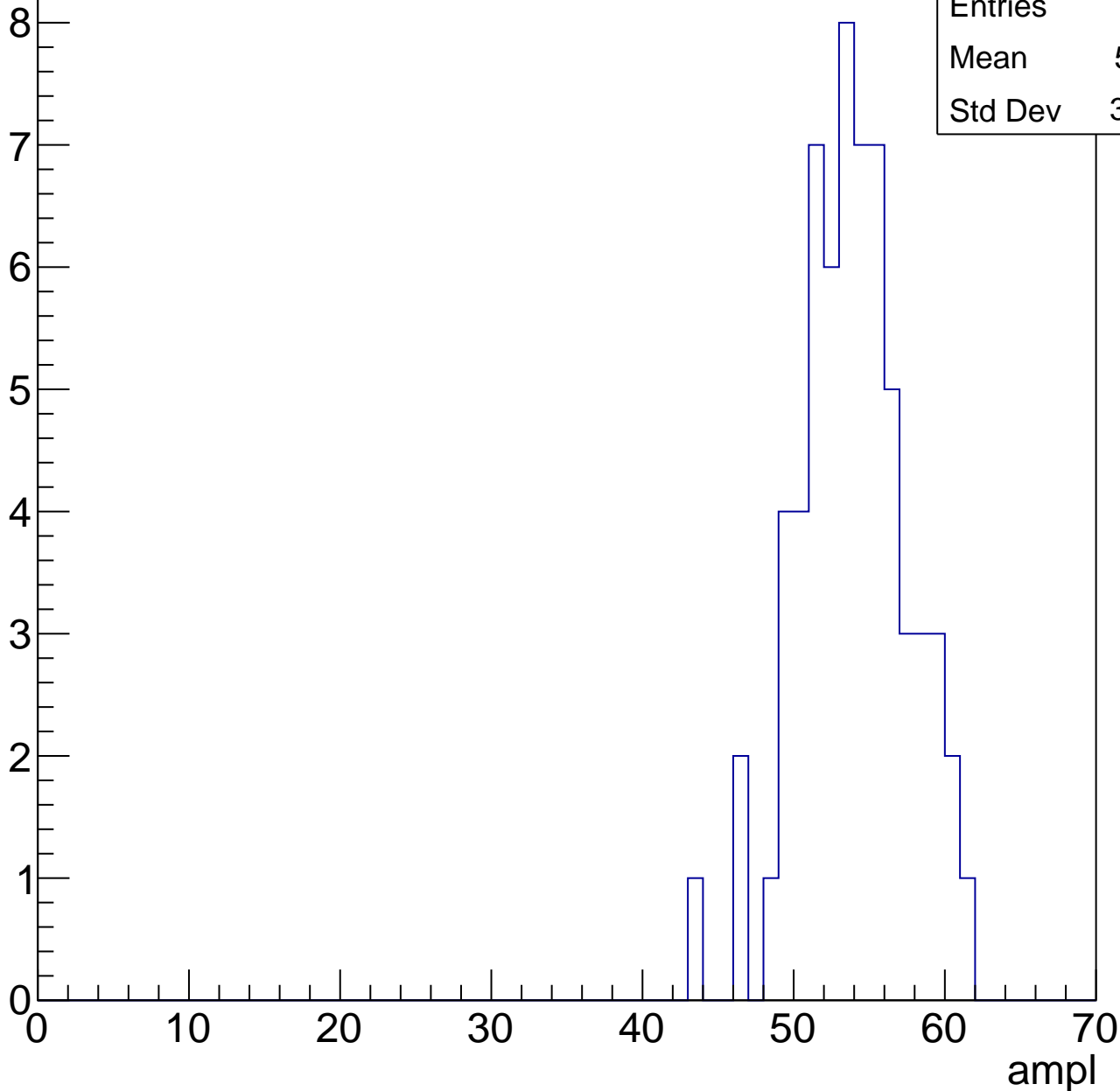


# B1L103S, U26-ch29, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

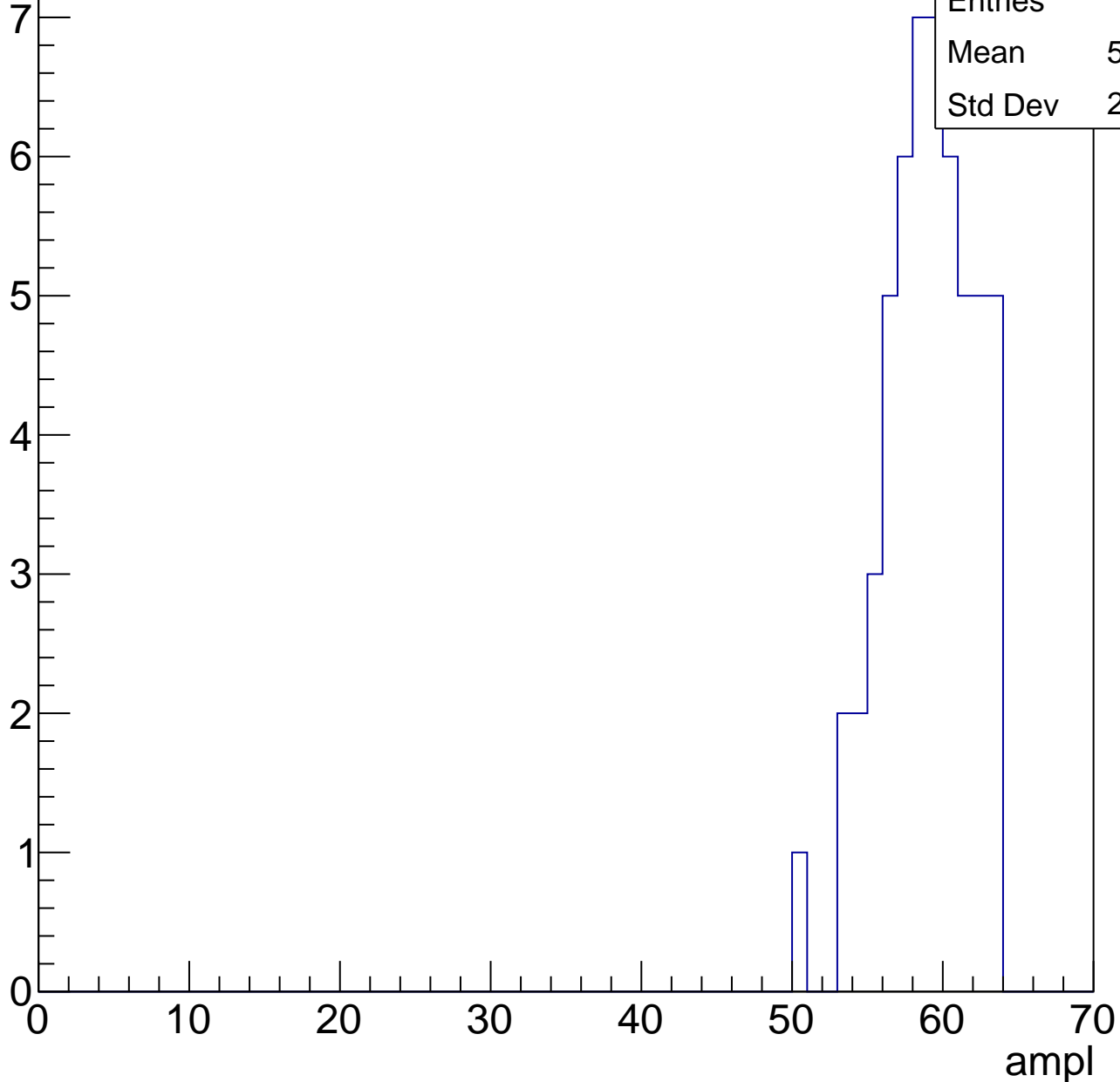
Entries	64
Mean	53.41
Std Dev	3.578



# B1L103S, U26-ch29, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



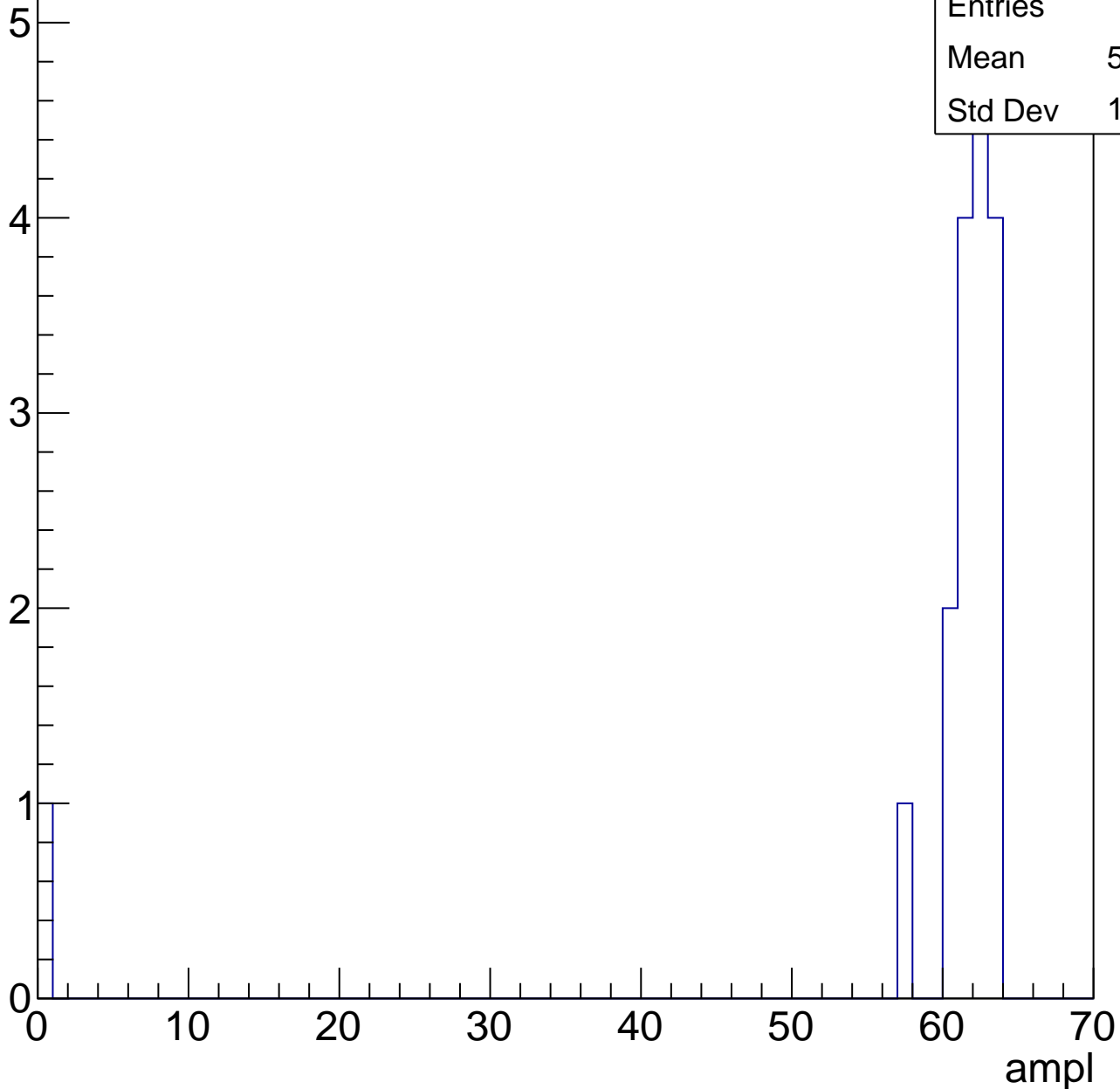
Entries	54
Mean	58.52
Std Dev	2.936

# B1L103S, U26-ch29, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	17
Mean	57.82
Std Dev	14.53





# B1L103S, U26-ch29, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

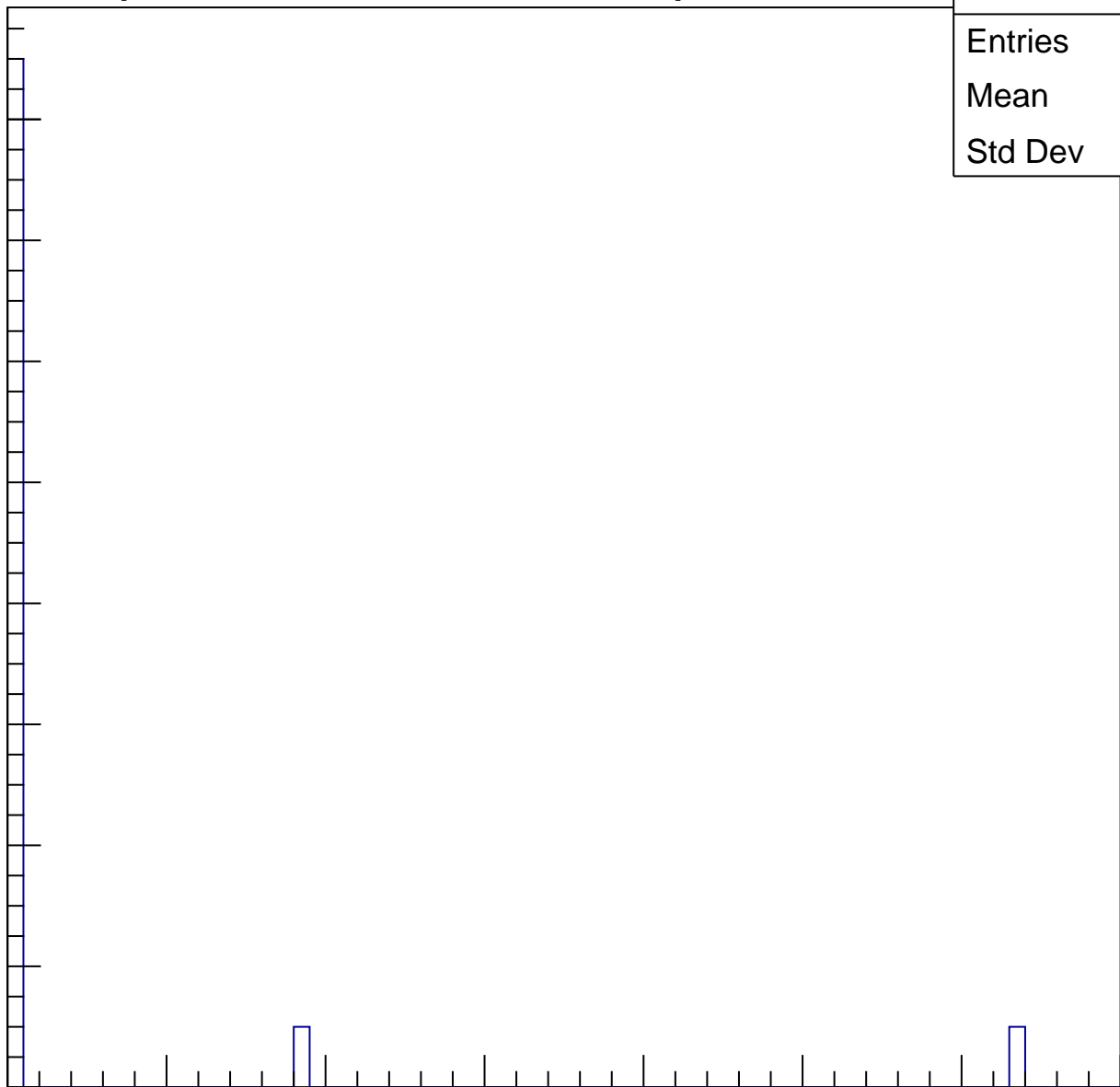
Entries	19
Mean	4.263
Std Dev	14.41

Entry

16  
14  
12  
10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B1L103S, U26-ch30, adc0

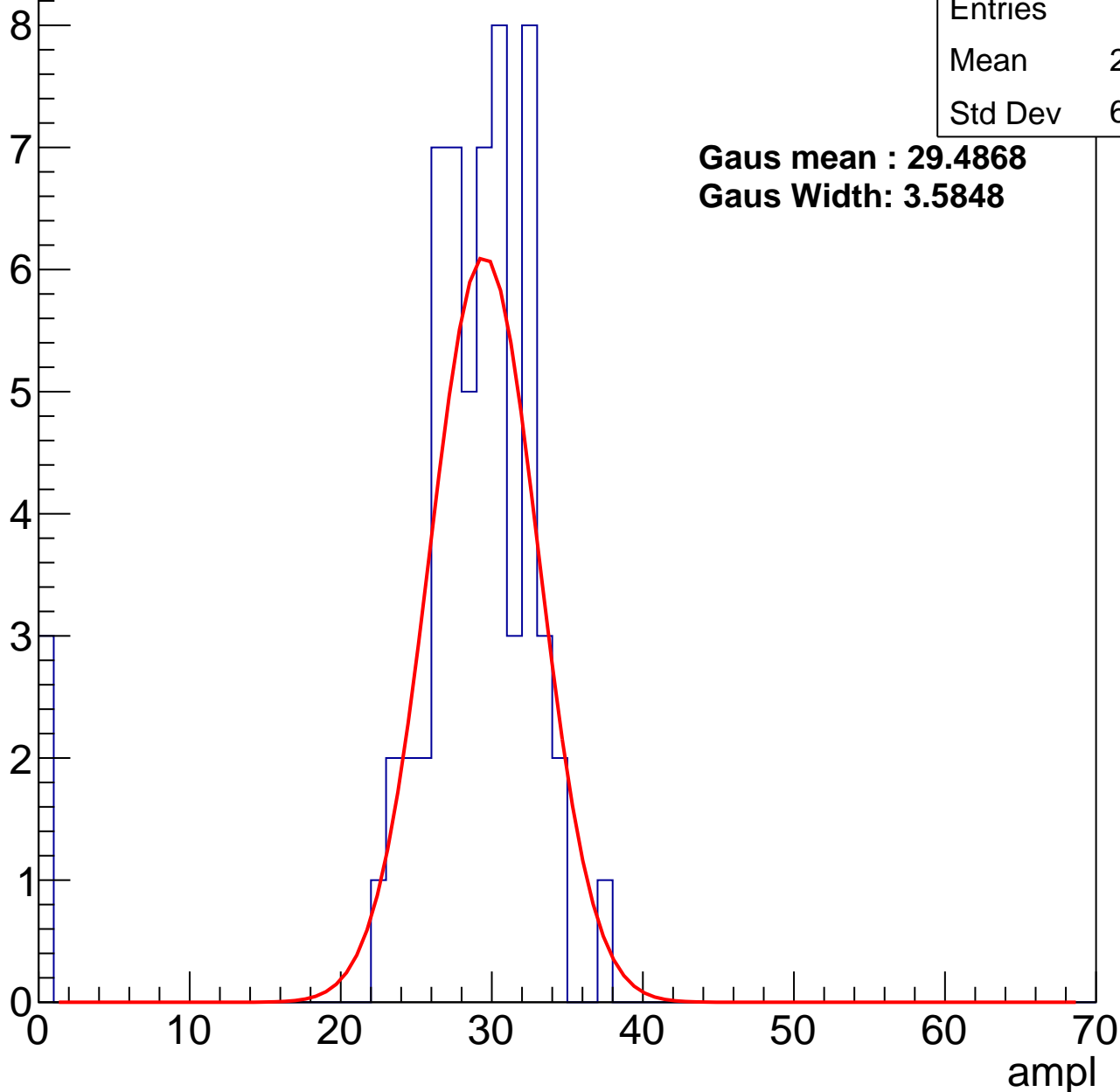
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	61
Mean	27.43
Std Dev	6.925

**Gaus mean : 29.4868**

**Gaus Width: 3.5848**



# B1L103S, U26-ch30, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	82
Mean	32.41
Std Dev	10.44

**Gaus mean : 36.2057**  
**Gaus Width: 3.1158**

Entry

10

8

6

4

2

0

0

10

20

30

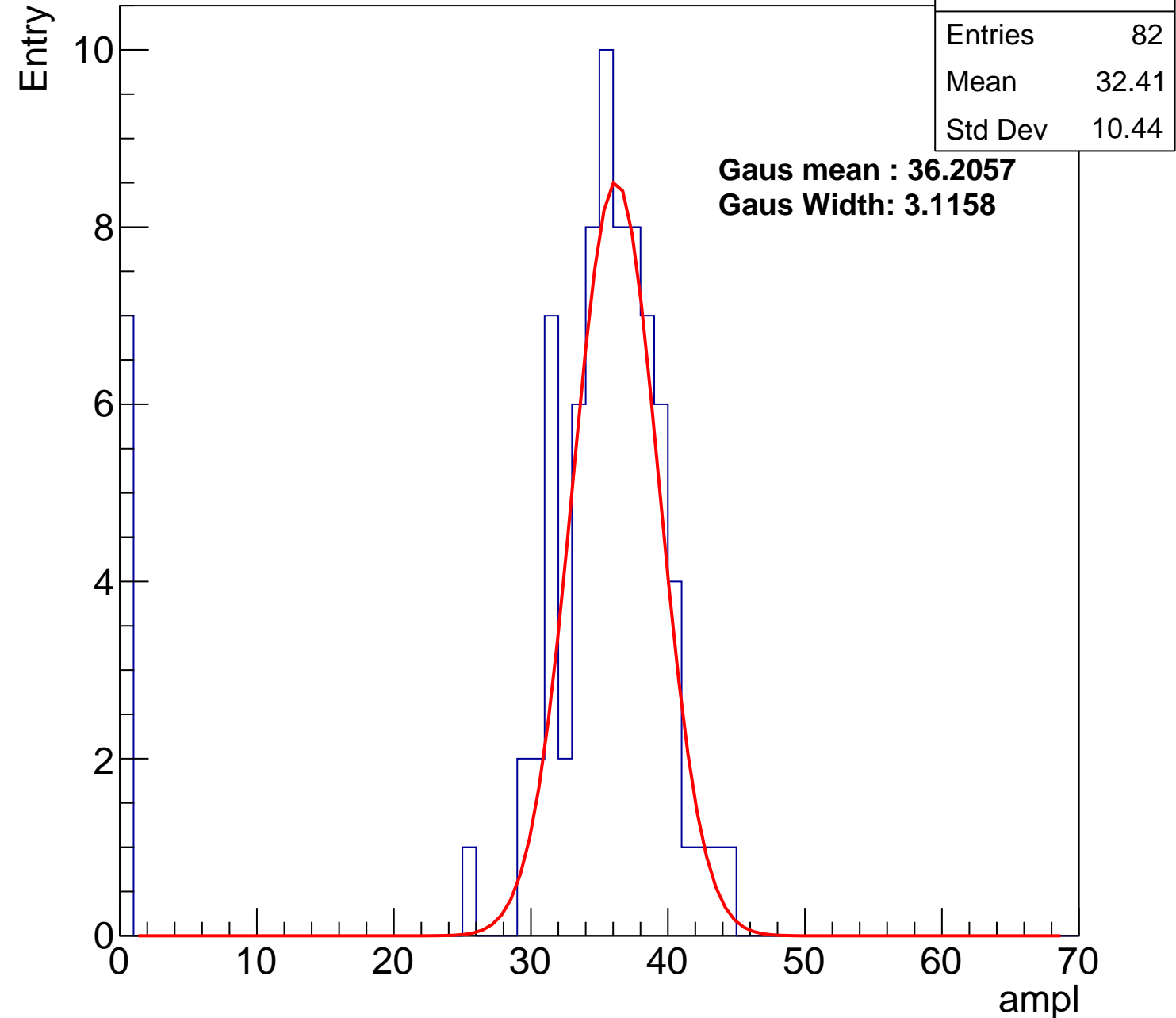
40

50

60

70

ampl



# B1L103S, U26-ch30, adc2

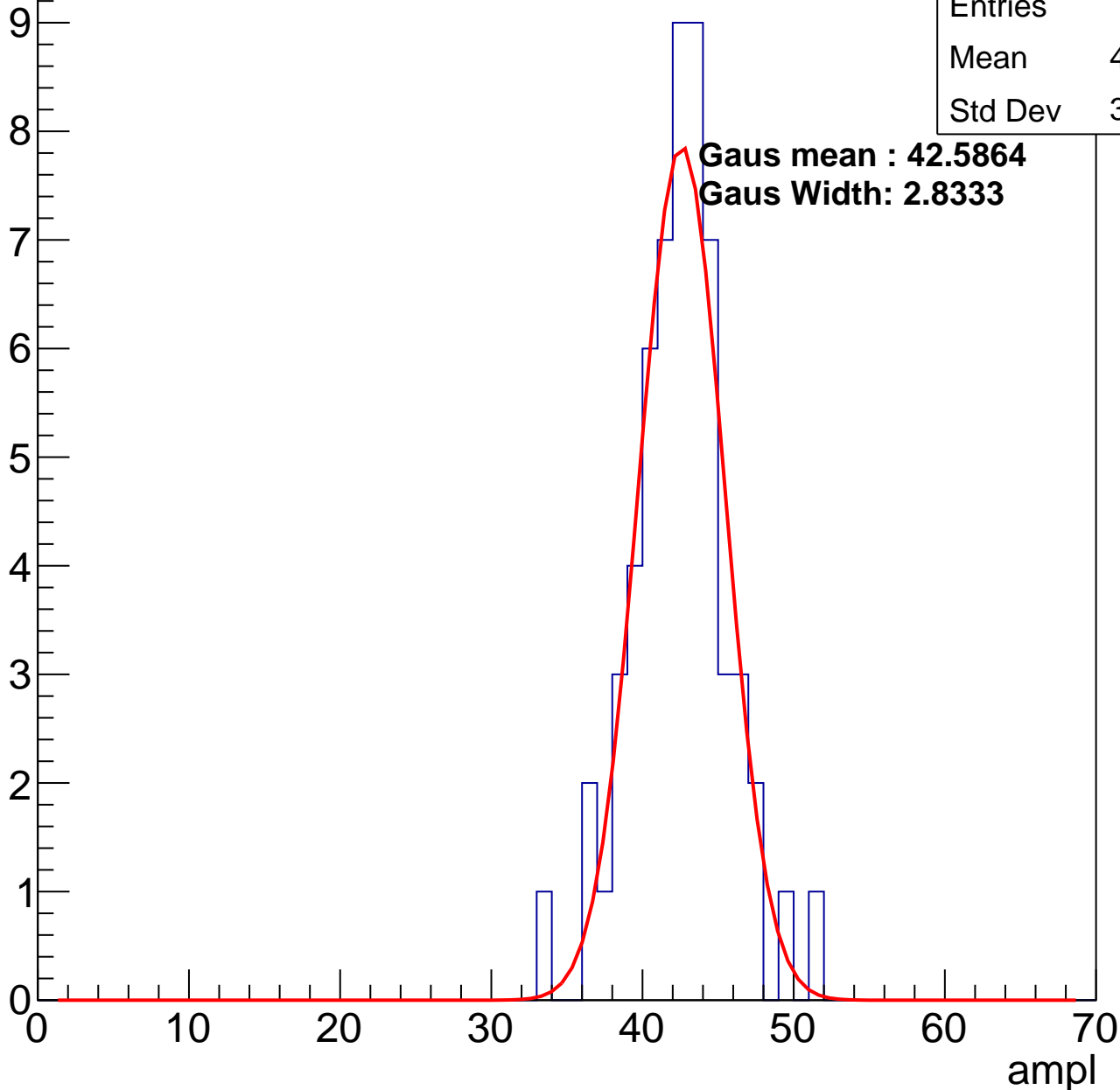
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	59
Mean	42.02
Std Dev	3.149

**Gaus mean : 42.5864**

**Gaus Width: 2.8333**

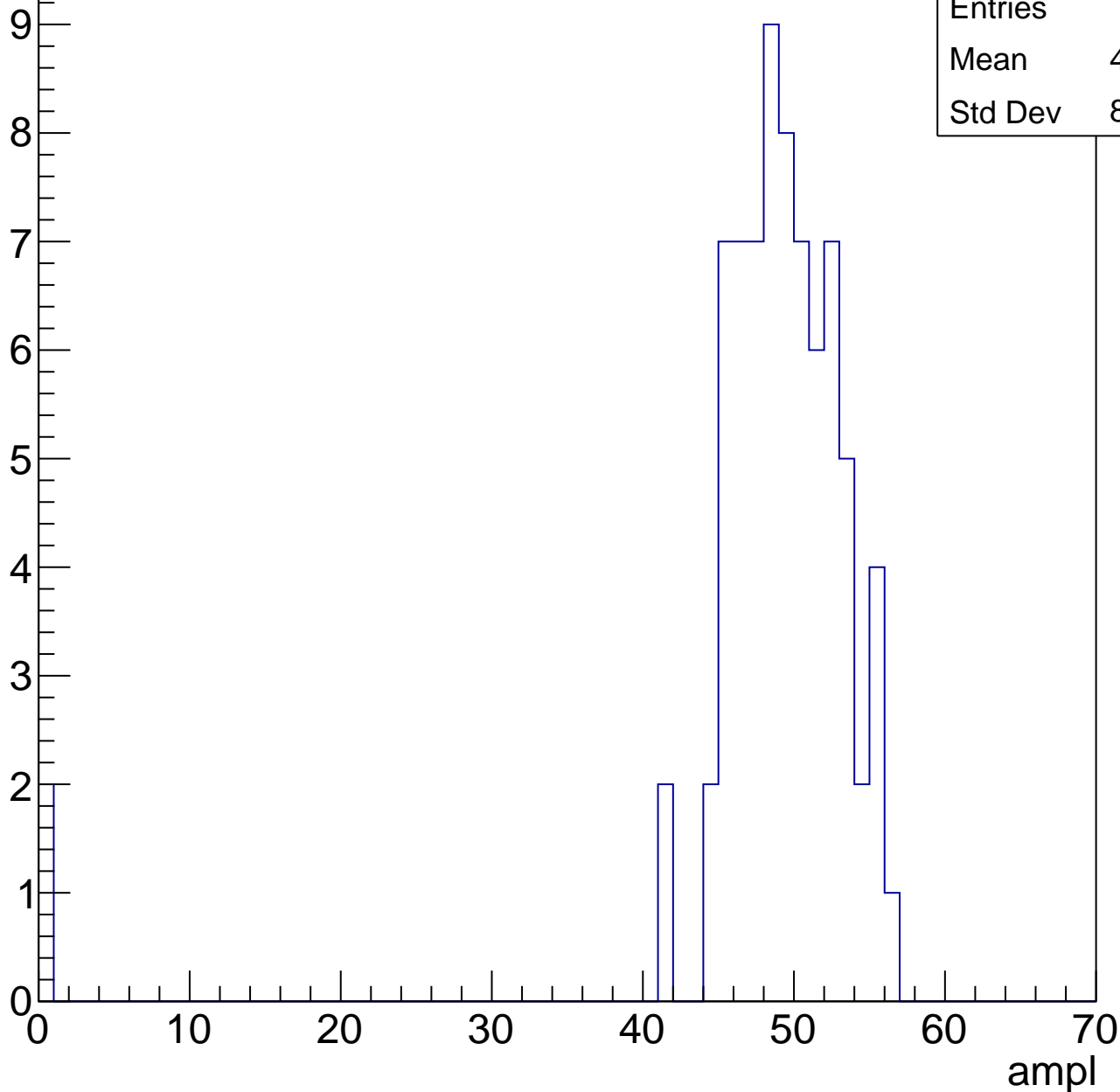


# B1L103S, U26-ch30, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	76
Mean	47.75
Std Dev	8.499

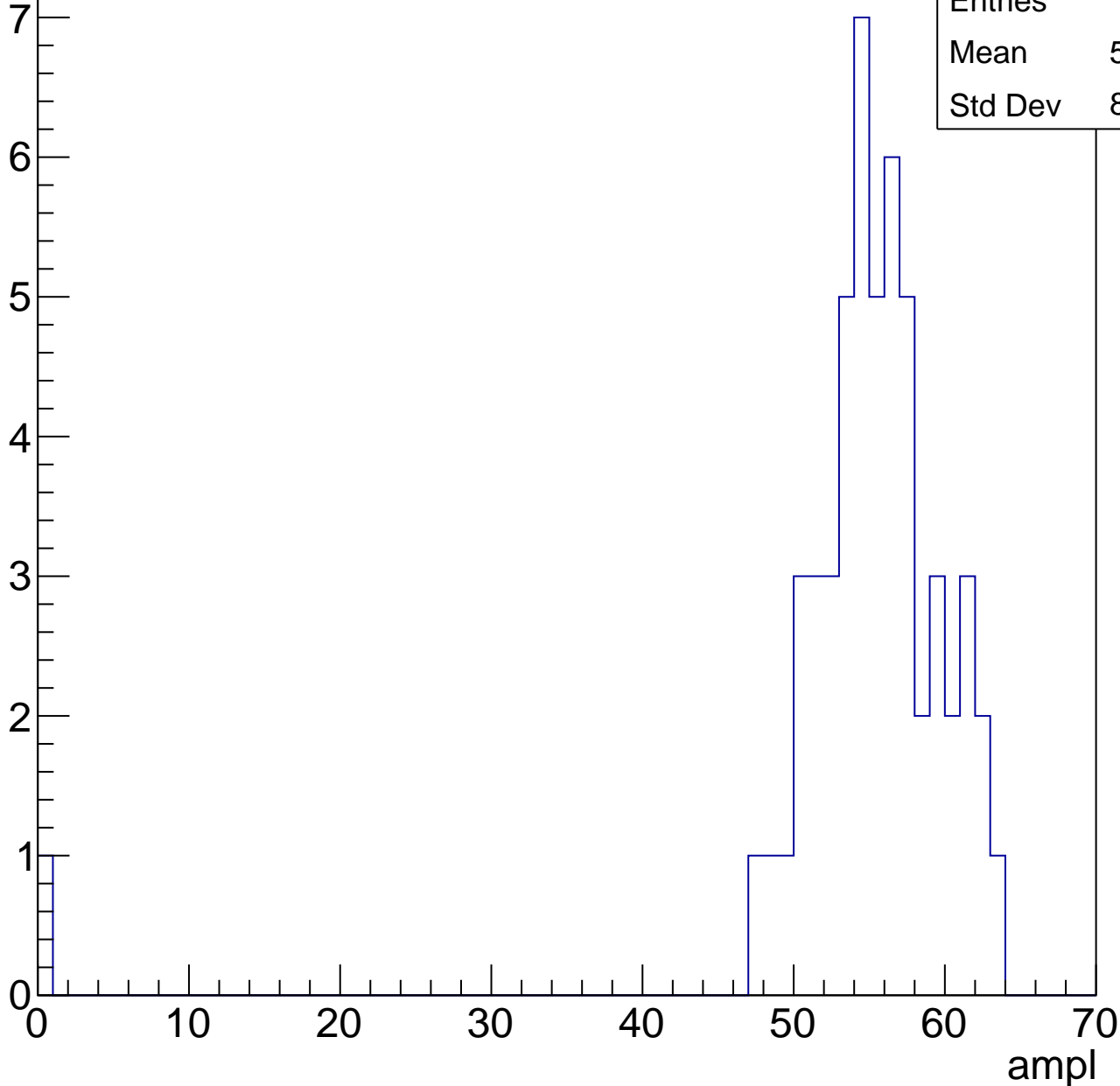


# B1L103S, U26-ch30, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	54
Mean	54.17
Std Dev	8.306

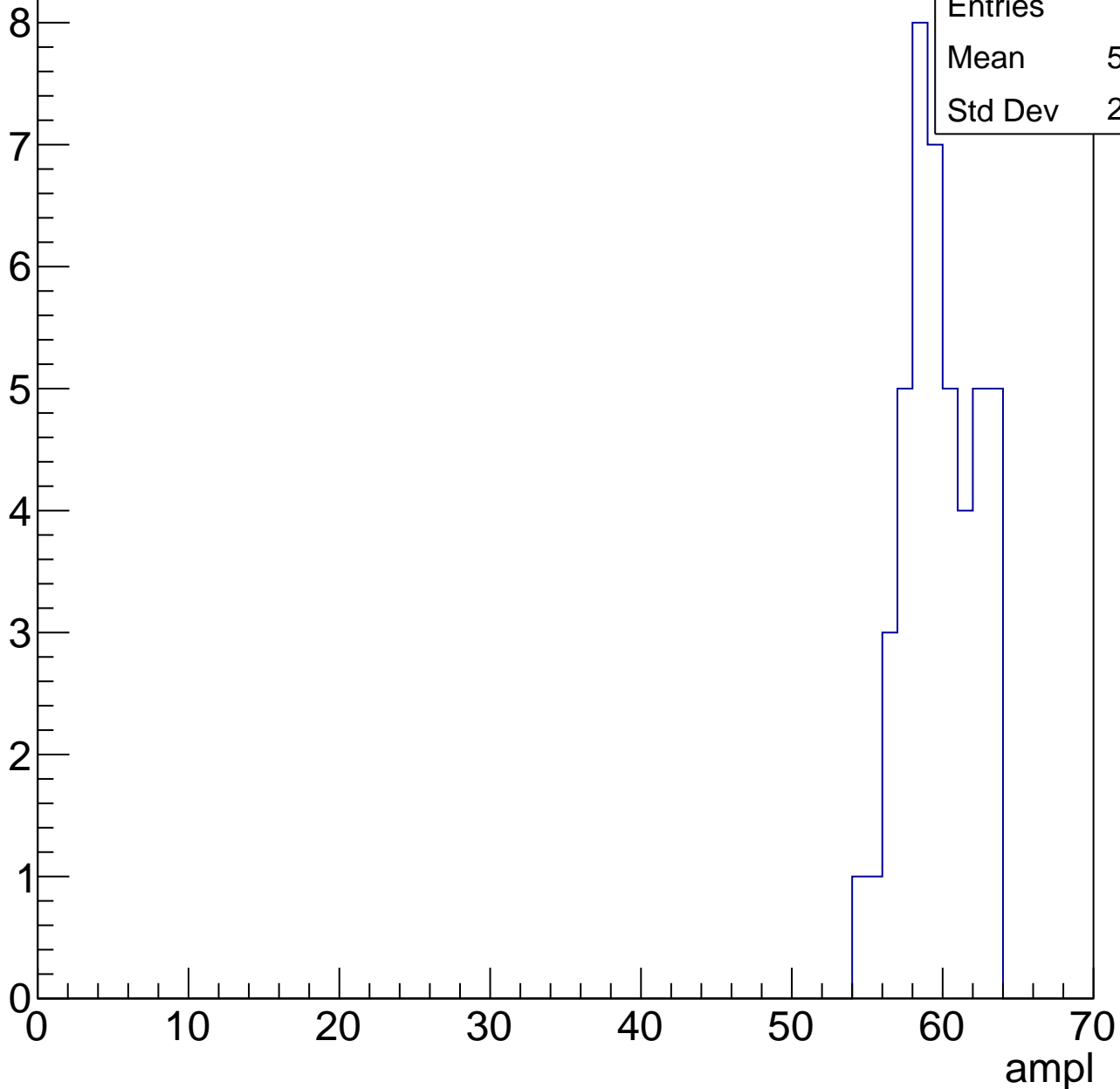


# B1L103S, U26-ch30, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

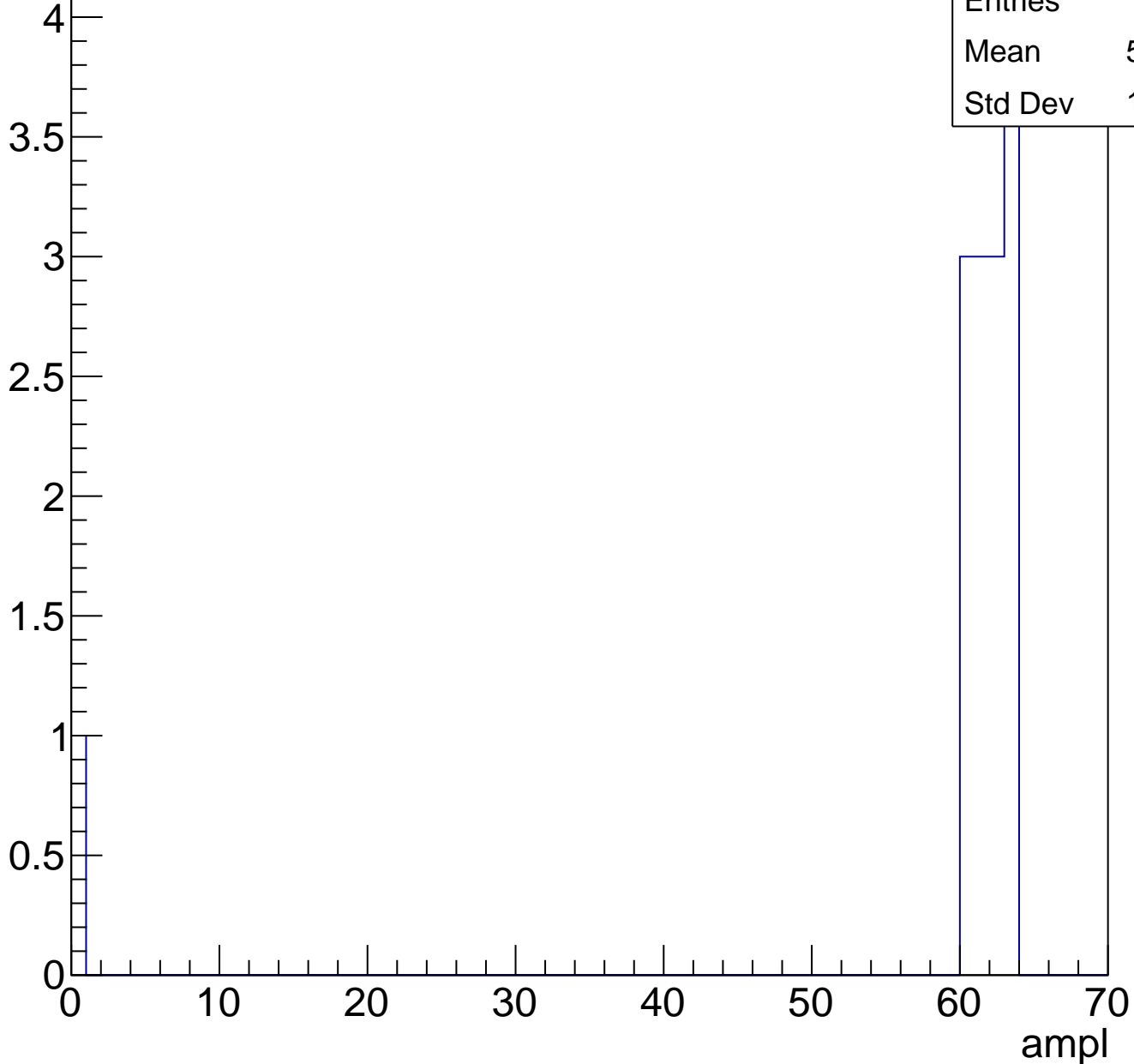
Entries	44
Mean	59.27
Std Dev	2.329



# B1L103S, U26-ch30, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry





# B1L103S, U26-ch30, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



# B1L103S, U26-ch31, adc0

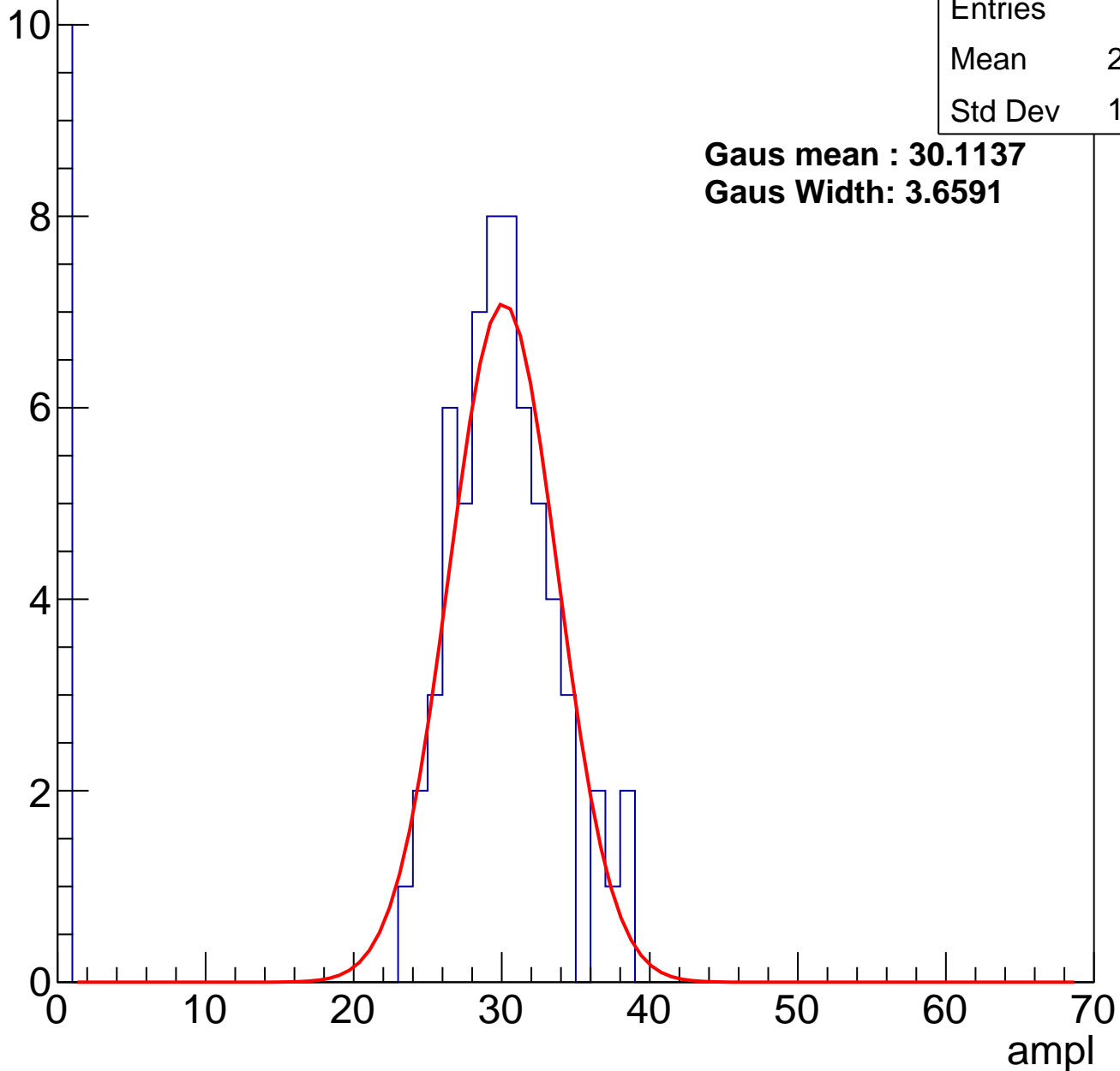
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	73
Mean	25.62
Std Dev	10.68

**Gaus mean : 30.1137**

**Gaus Width: 3.6591**

Entry



# B1L103S, U26-ch31, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	82
Mean	34.16
Std Dev	9.272

**Gaus mean : 36.8638**

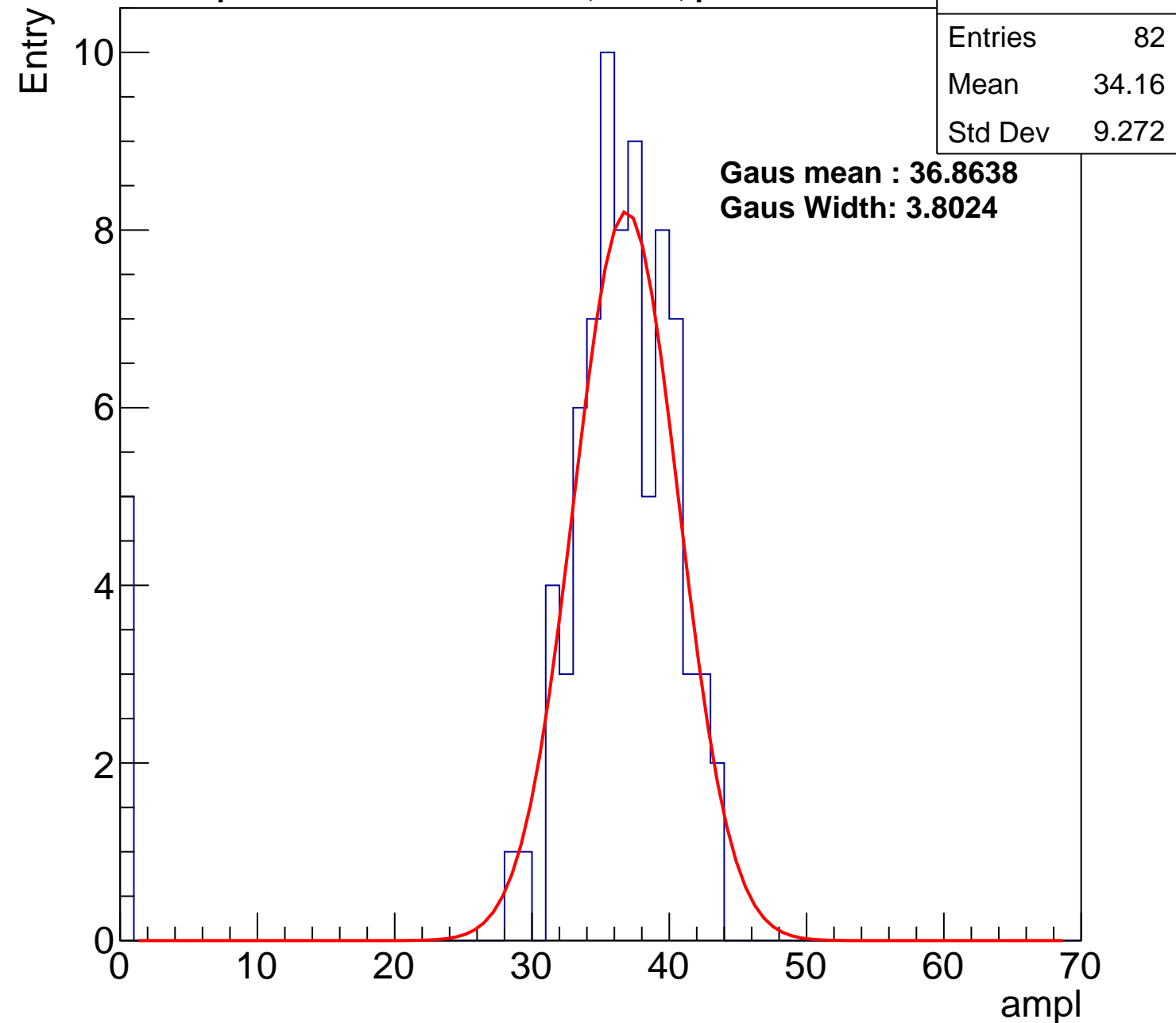
**Gaus Width: 3.8024**

Entry

10  
8  
6  
4  
2  
0

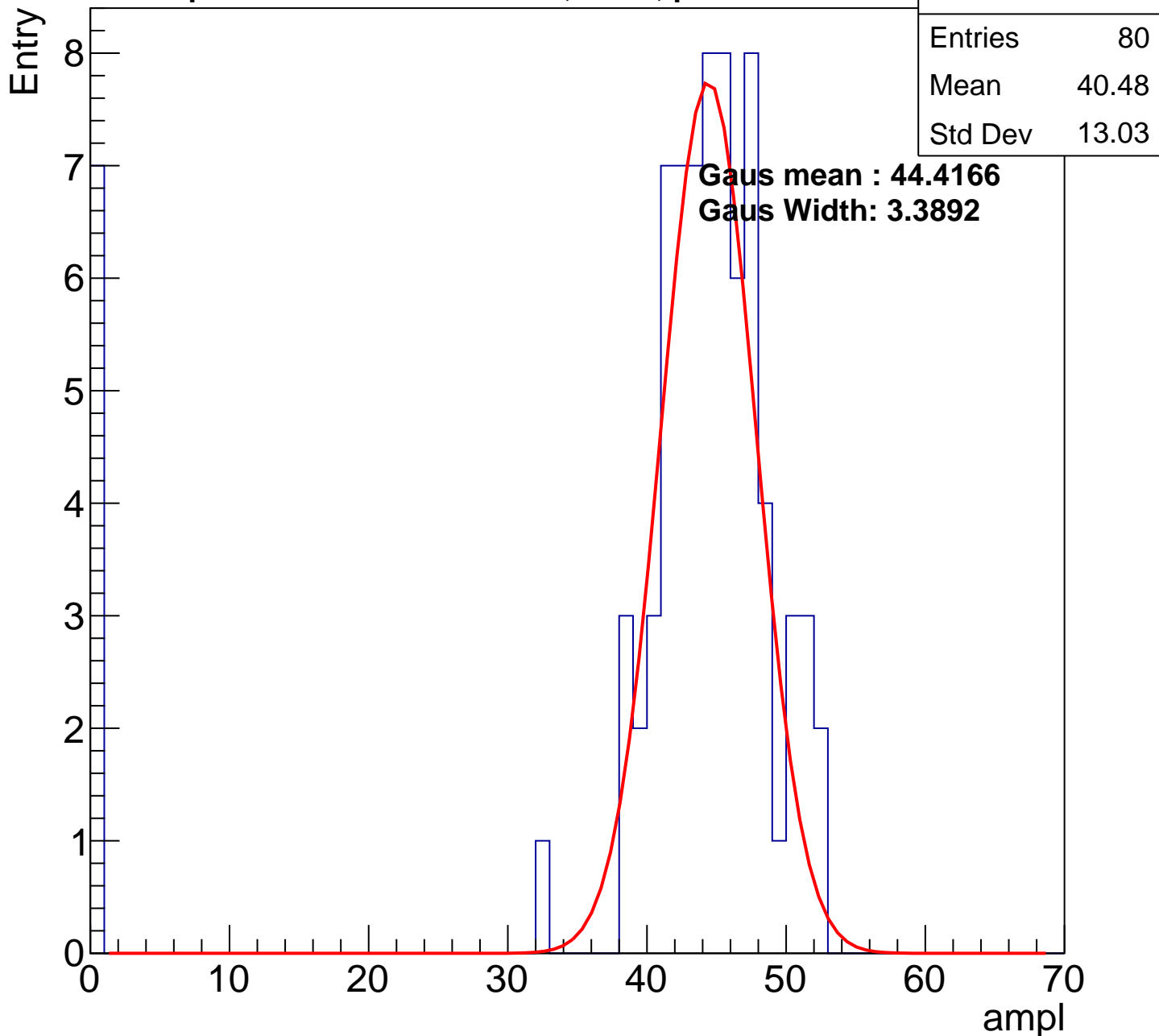
ampl

0 10 20 30 40 50 60 70



# B1L103S, U26-ch31, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

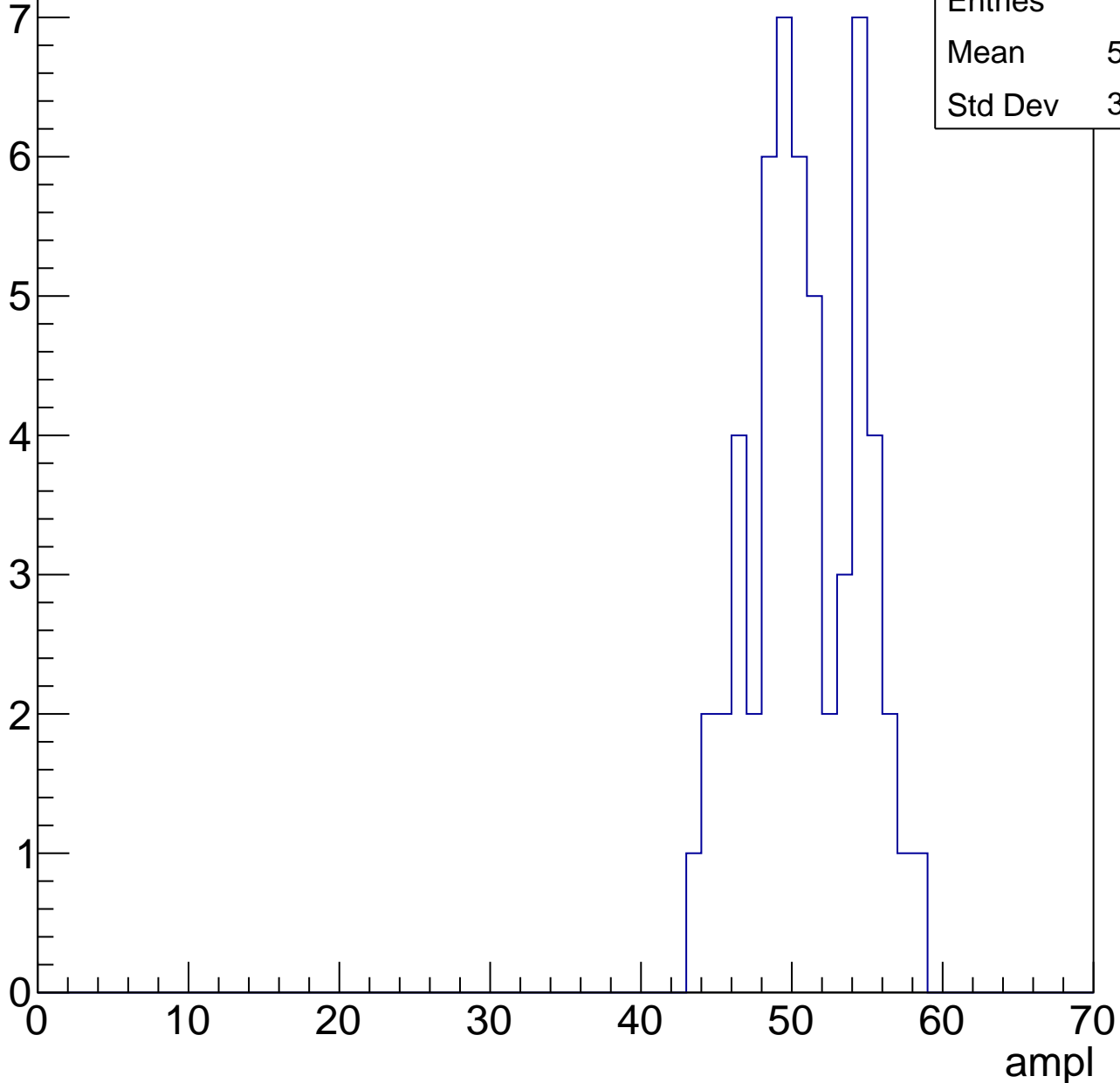


# B1L103S, U26-ch31, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	55
Mean	50.42
Std Dev	3.596

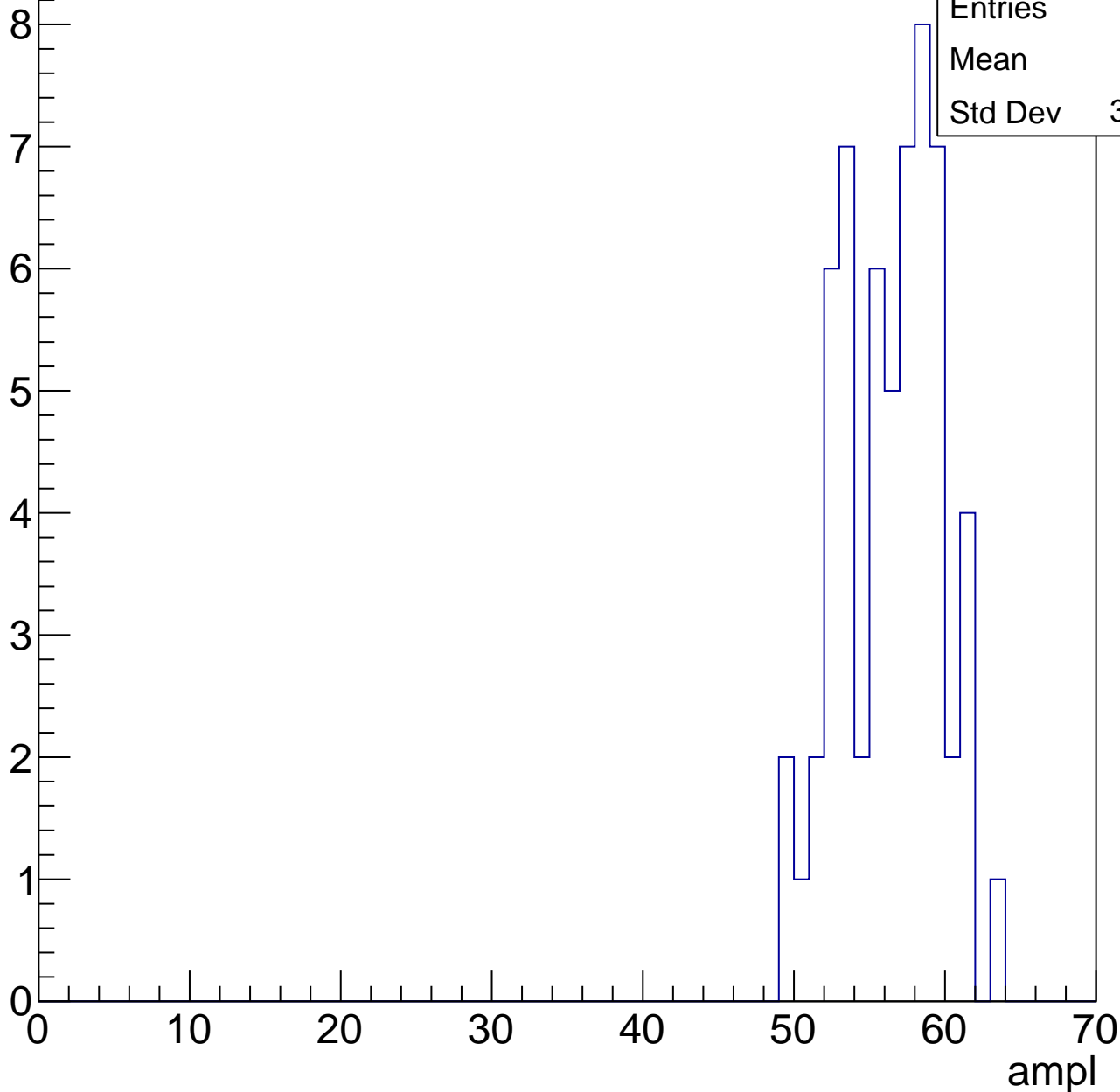


# B1L103S, U26-ch31, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

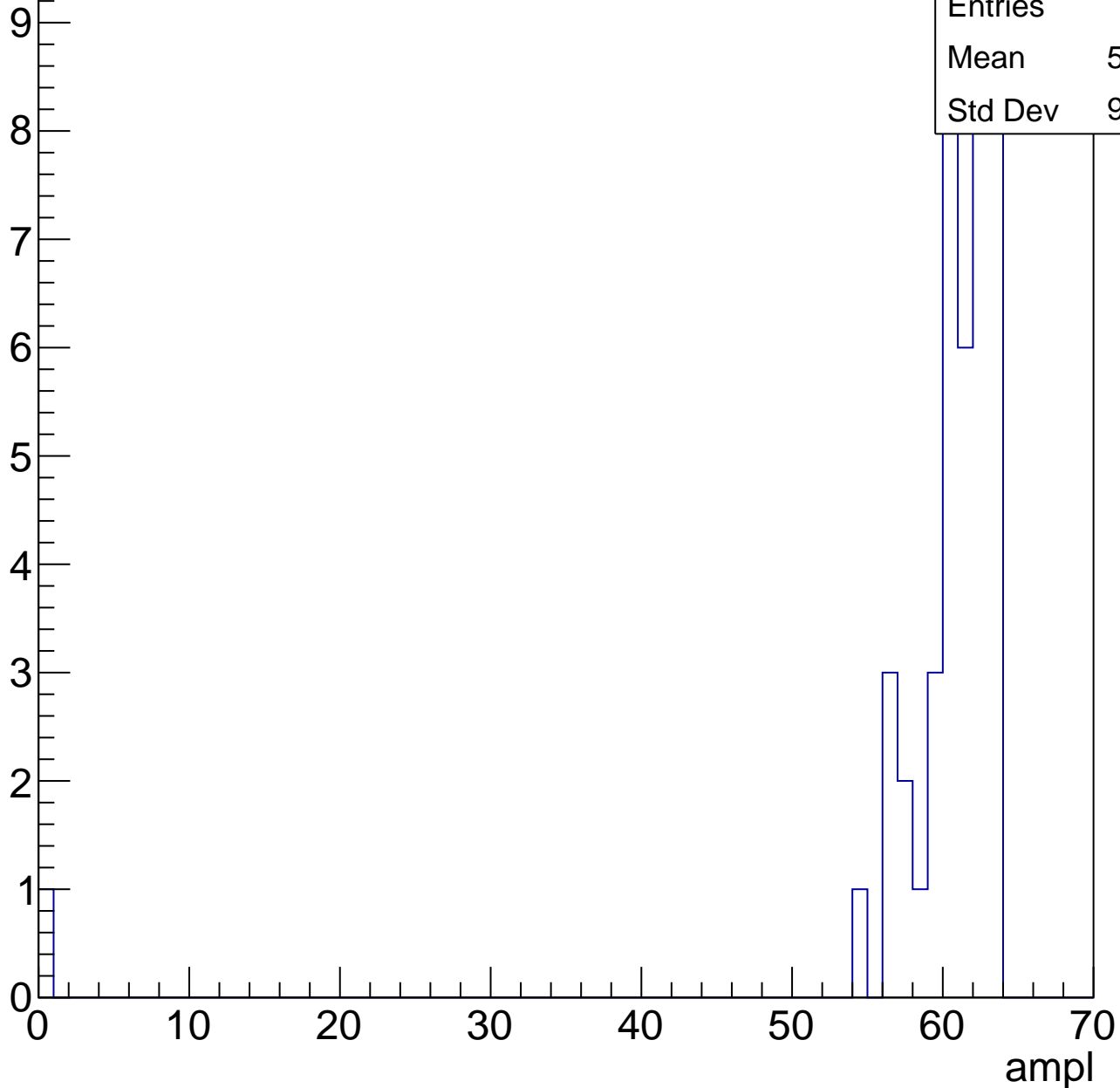
Entries	60
Mean	55.9
Std Dev	3.264



# B1L103S, U26-ch31, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



# B1L103S, U26-ch31, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry





# B1L103S, U26-ch31, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



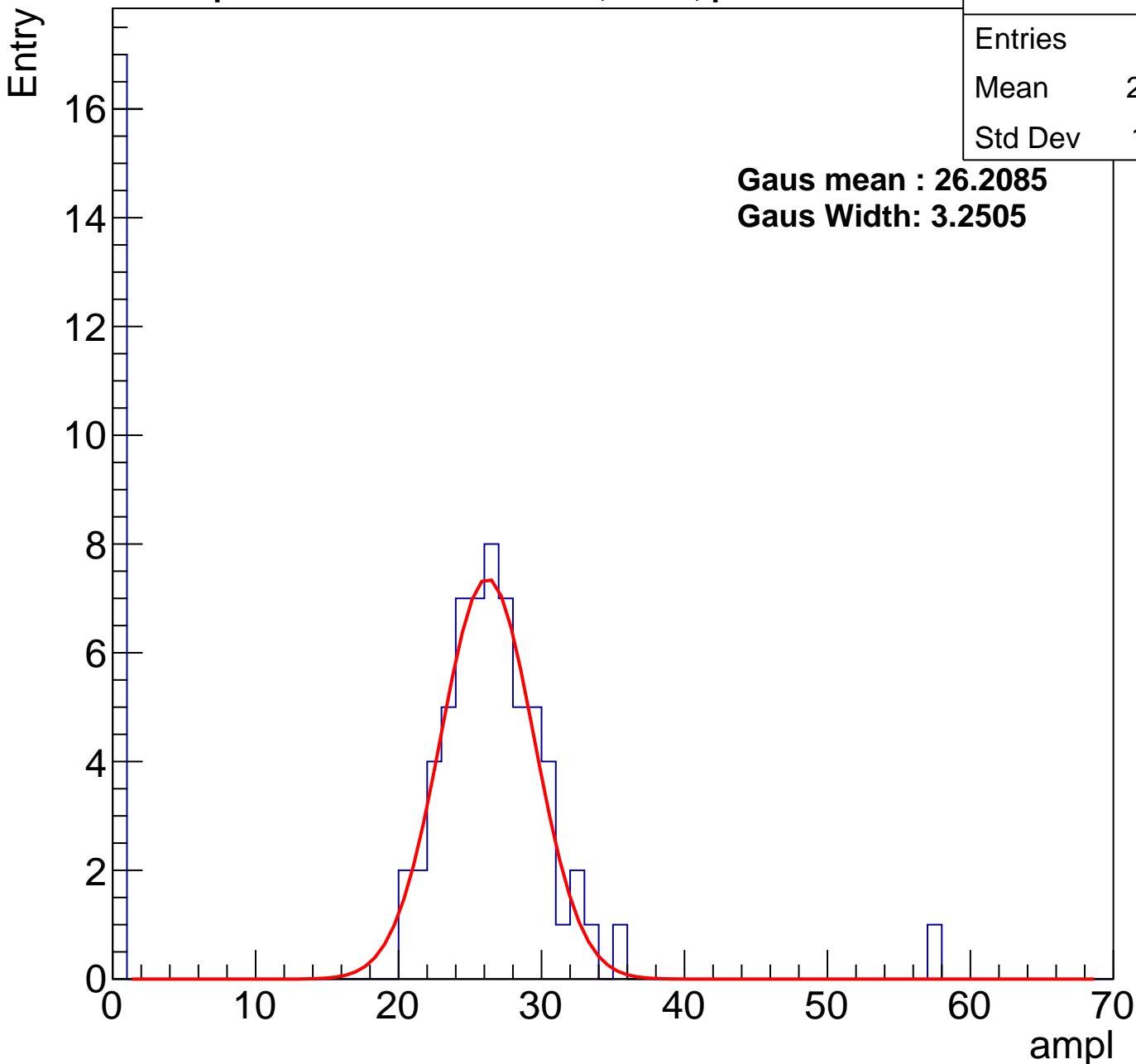
# B1L103S, U26-ch32, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	79
Mean	20.89
Std Dev	11.81

**Gaus mean : 26.2085**

**Gaus Width: 3.2505**



# B1L103S, U26-ch32, adc1

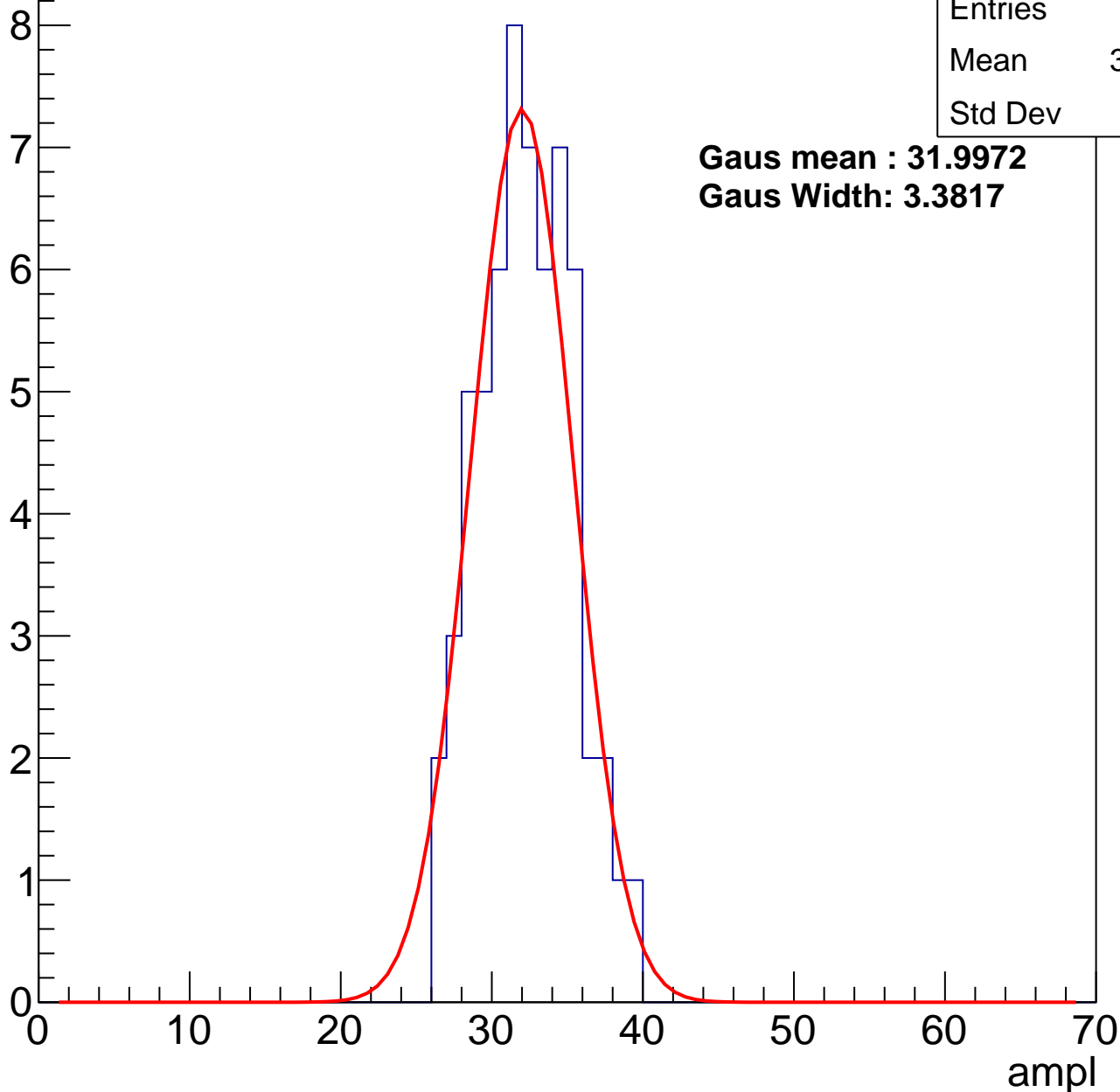
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	61
Mean	31.79
Std Dev	3.02

**Gaus mean : 31.9972**

**Gaus Width: 3.3817**



# B1L103S, U26-ch32, adc2

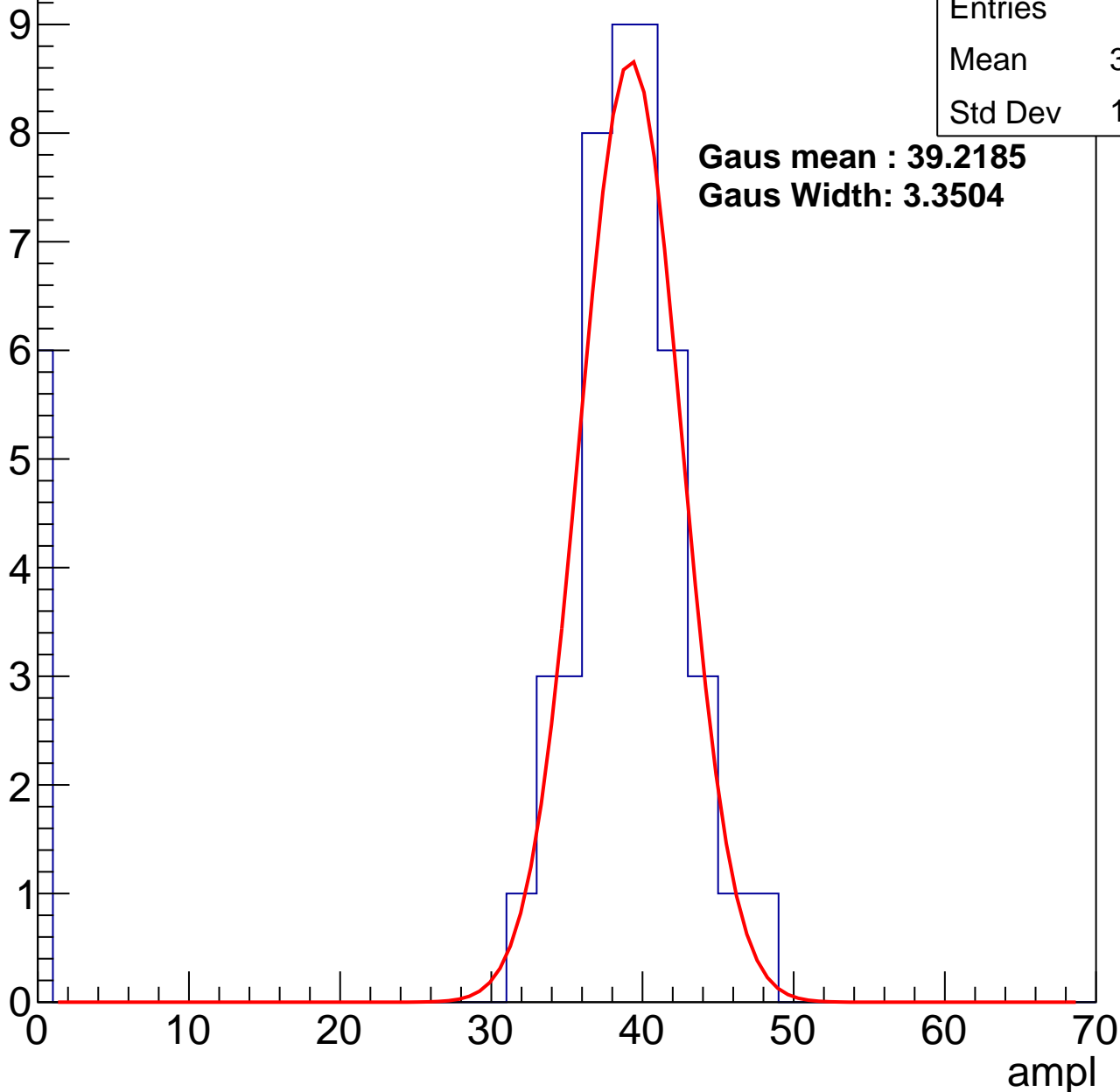
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	82
Mean	35.99
Std Dev	10.64

**Gaus mean : 39.2185**

**Gaus Width: 3.3504**

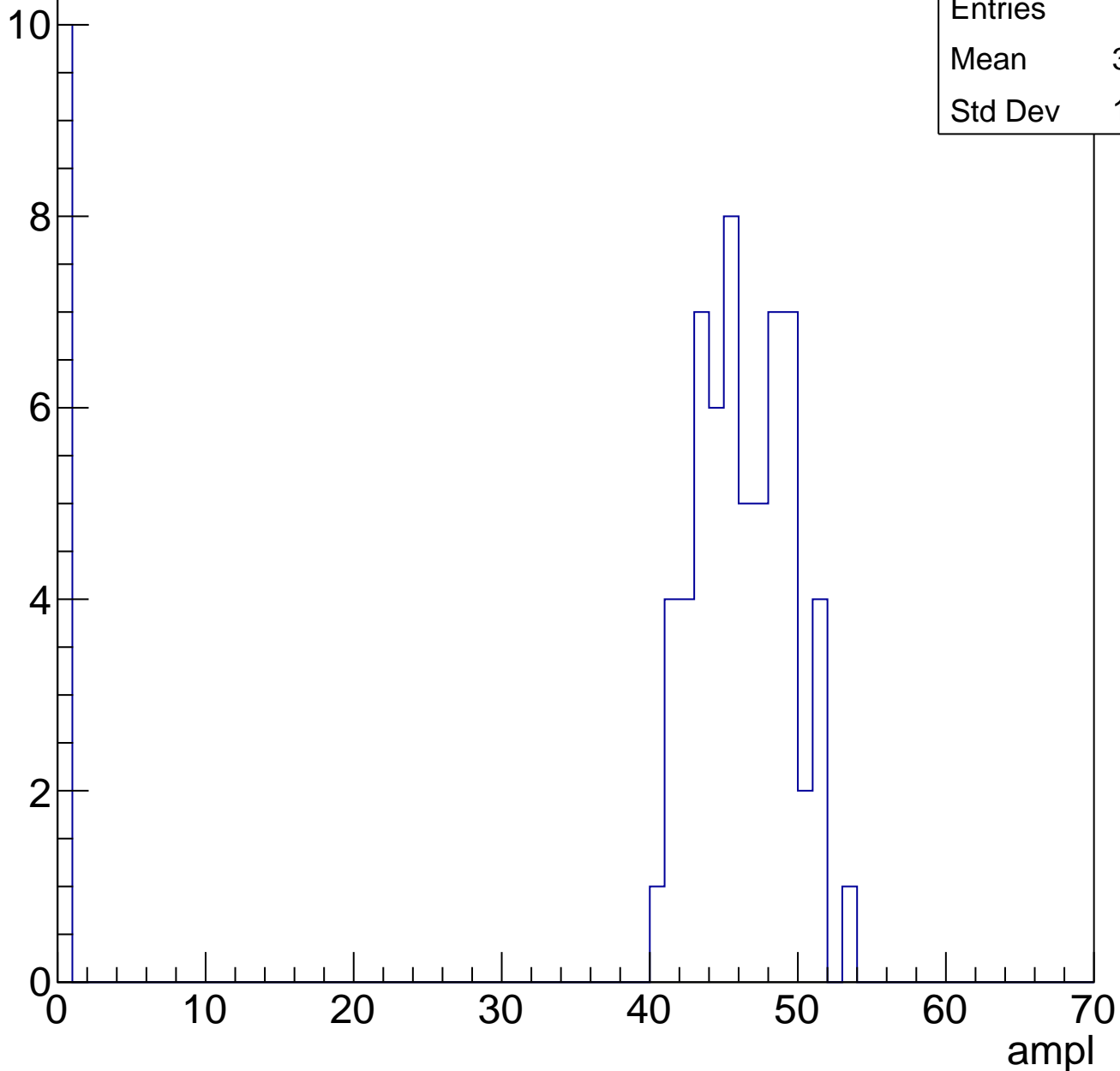


# B1L103S, U26-ch32, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

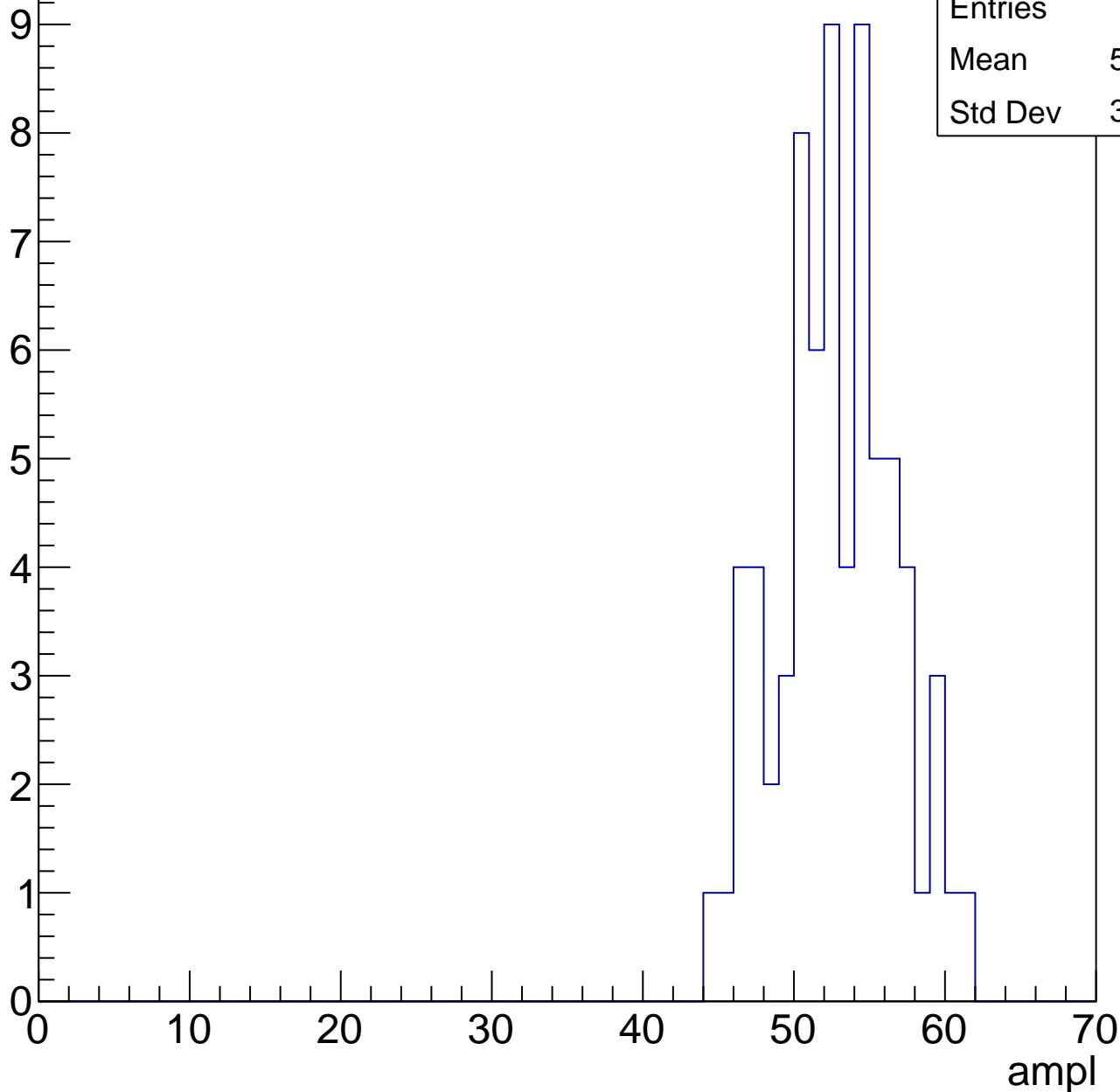
Entries	71
Mean	39.41
Std Dev	16.21



# B1L103S, U26-ch32, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

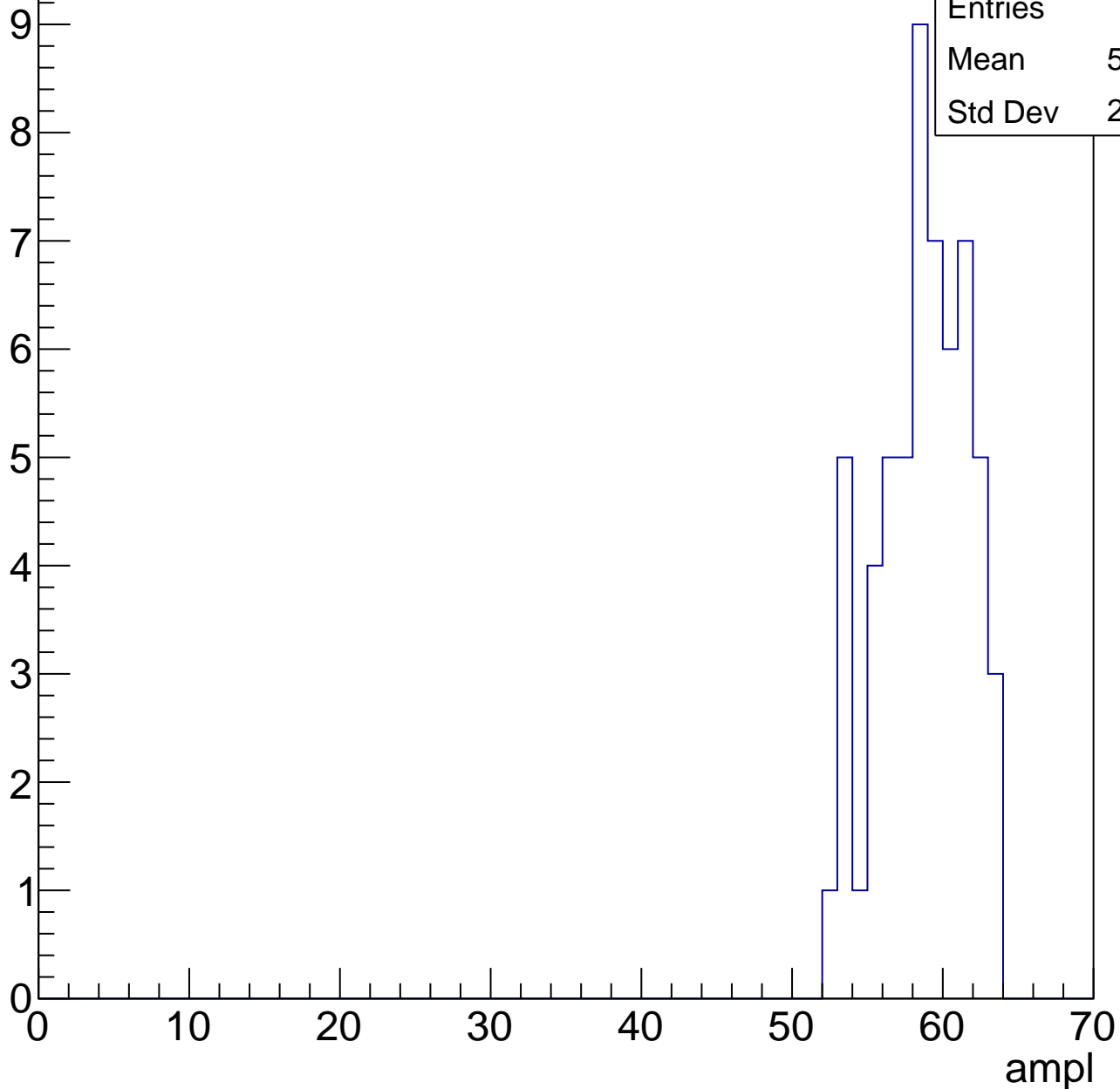


# B1L103S, U26-ch32, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	58
Mean	58.22
Std Dev	2.889

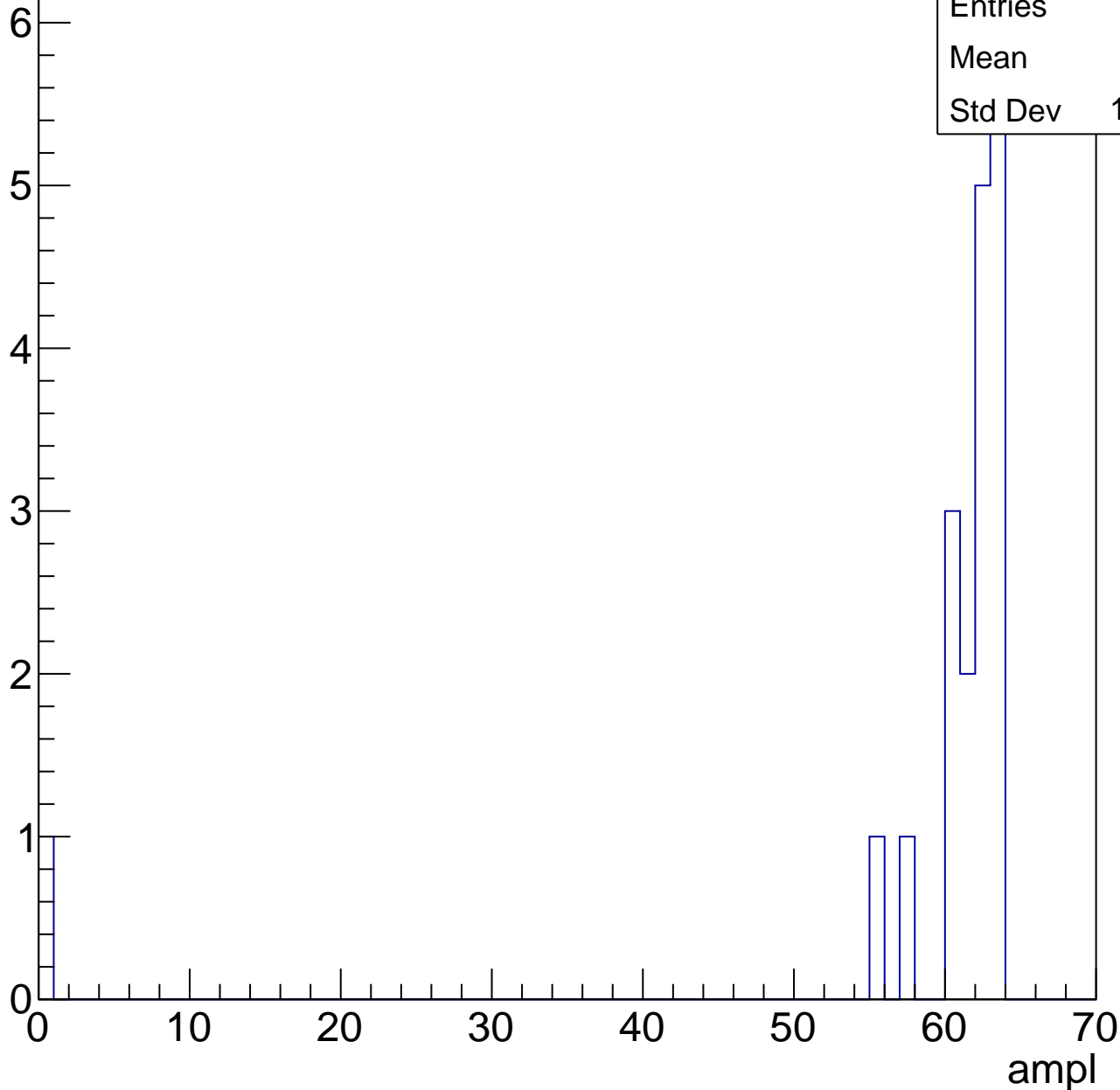


# B1L103S, U26-ch32, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	19
Mean	58
Std Dev	13.83





# B1L103S, U26-ch32, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

18  
16  
14  
12  
10  
8  
6  
4  
2  
0

Entries	19
Mean	3.316
Std Dev	14.07

ampl

0 10 20 30 40 50 60 70

# B1L103S, U26-ch33, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	89
Mean	27.34
Std Dev	10.3

**Gaus mean : 31.1543**

**Gaus Width: 4.2292**

Entry

10

8

6

4

2

0

0

10

20

30

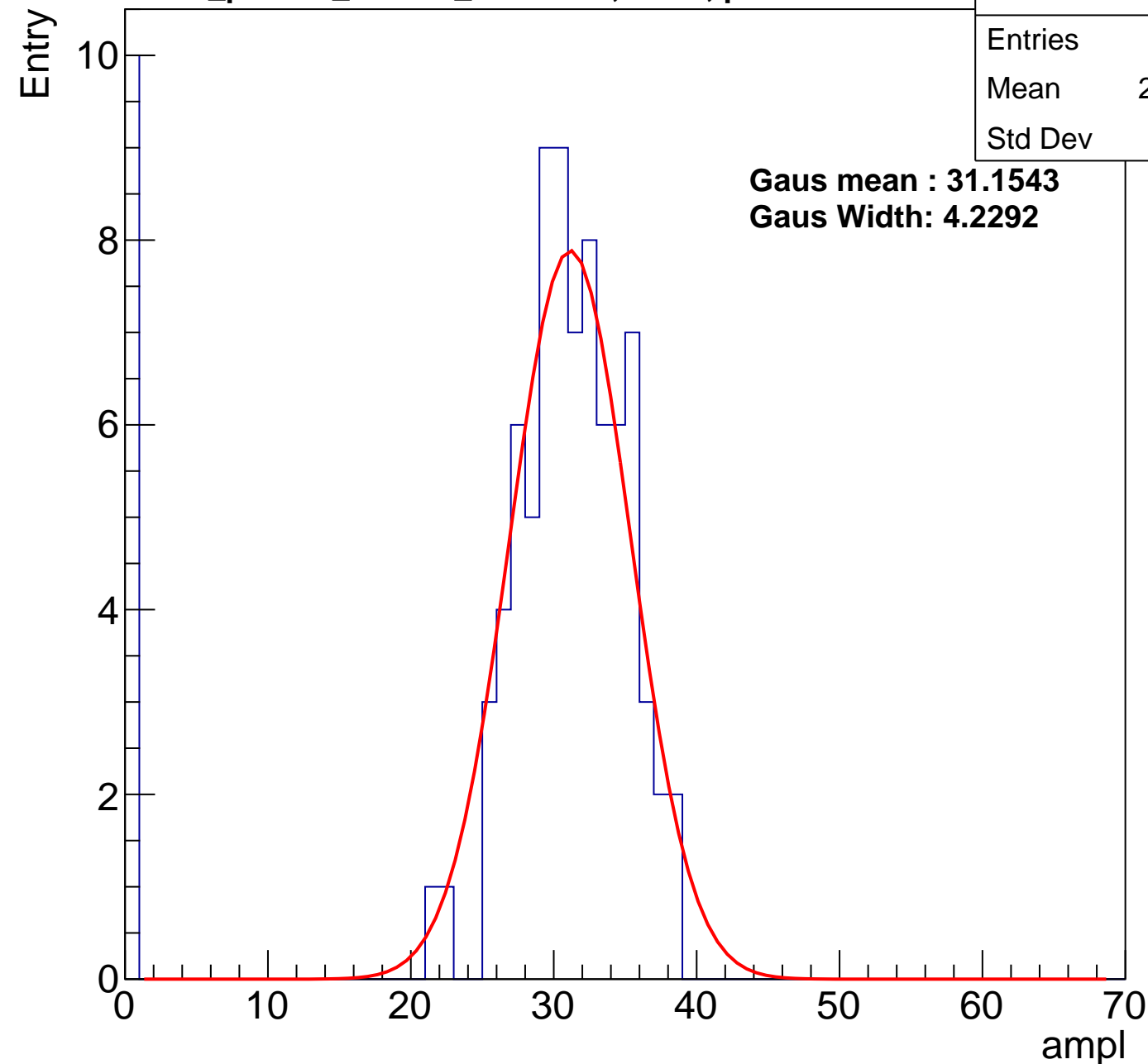
40

50

60

70

ampl



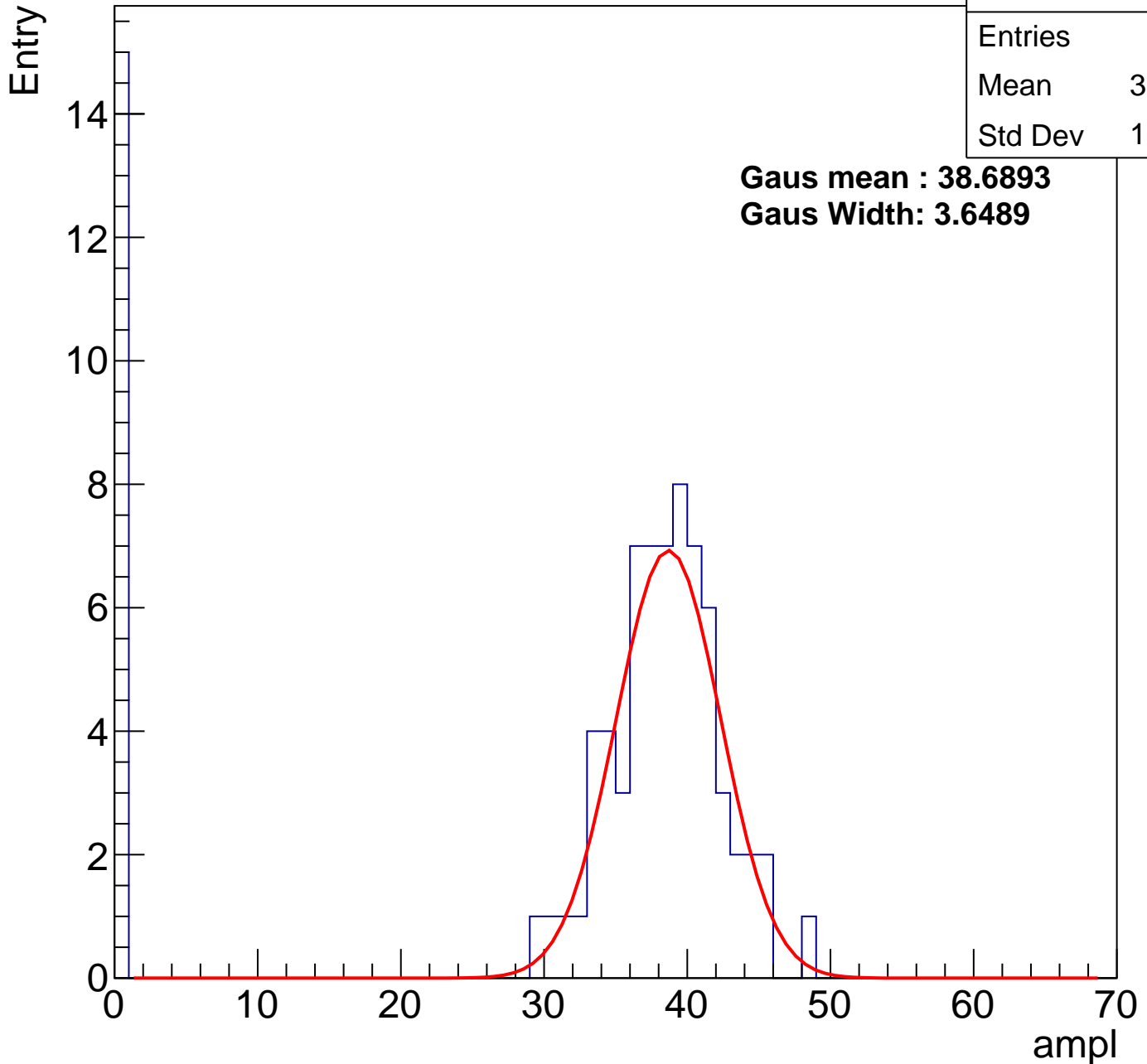
# B1L103S, U26-ch33, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	82
Mean	31.07
Std Dev	15.08

**Gaus mean : 38.6893**

**Gaus Width: 3.6489**



# B1L103S, U26-ch33, adc2

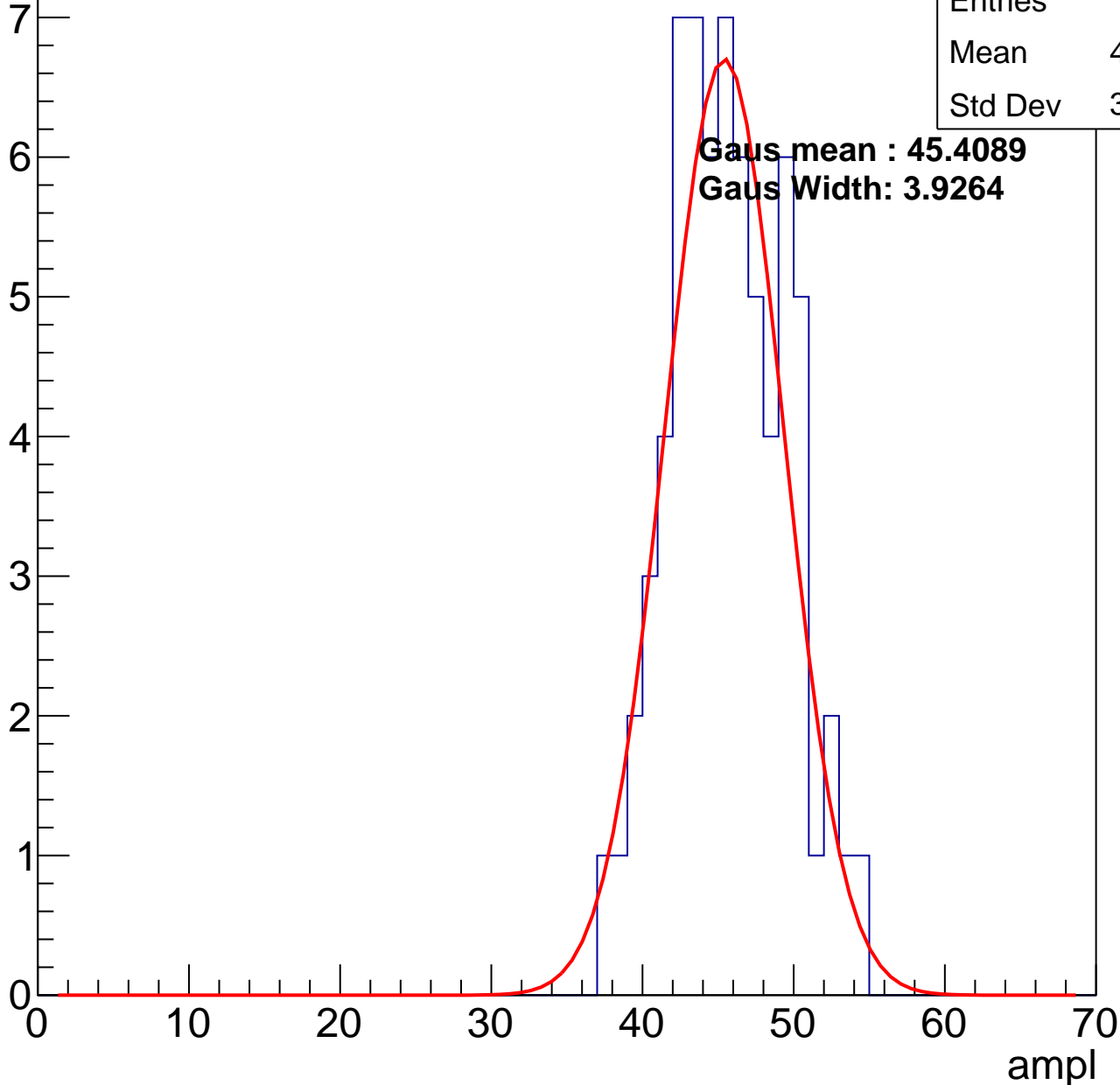
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	69
Mean	45.22
Std Dev	3.768

**Gaus mean : 45.4089**

**Gaus Width: 3.9264**

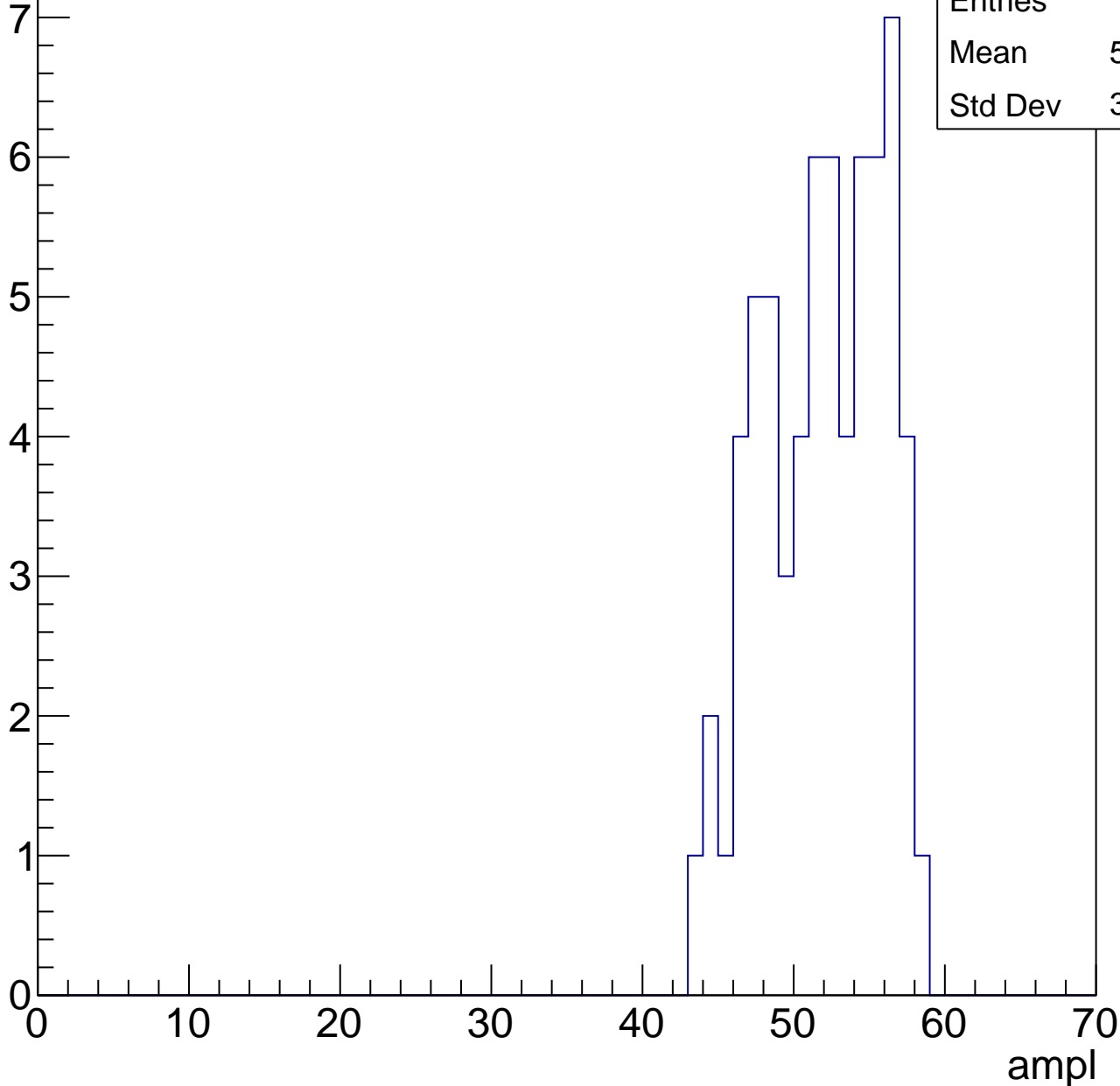


# B1L103S, U26-ch33, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	65
Mean	51.45
Std Dev	3.855

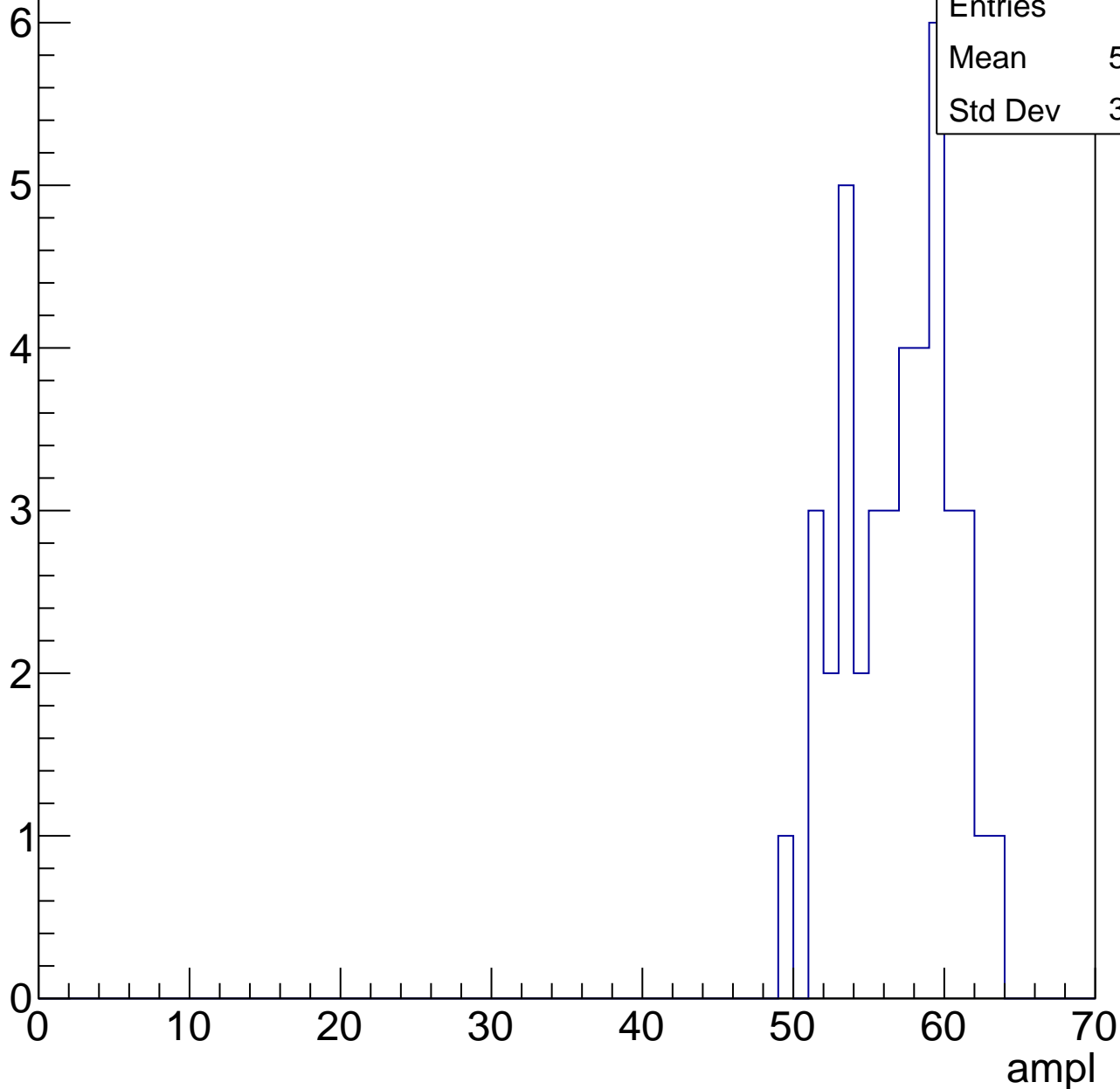


# B1L103S, U26-ch33, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	41
Mean	56.44
Std Dev	3.443

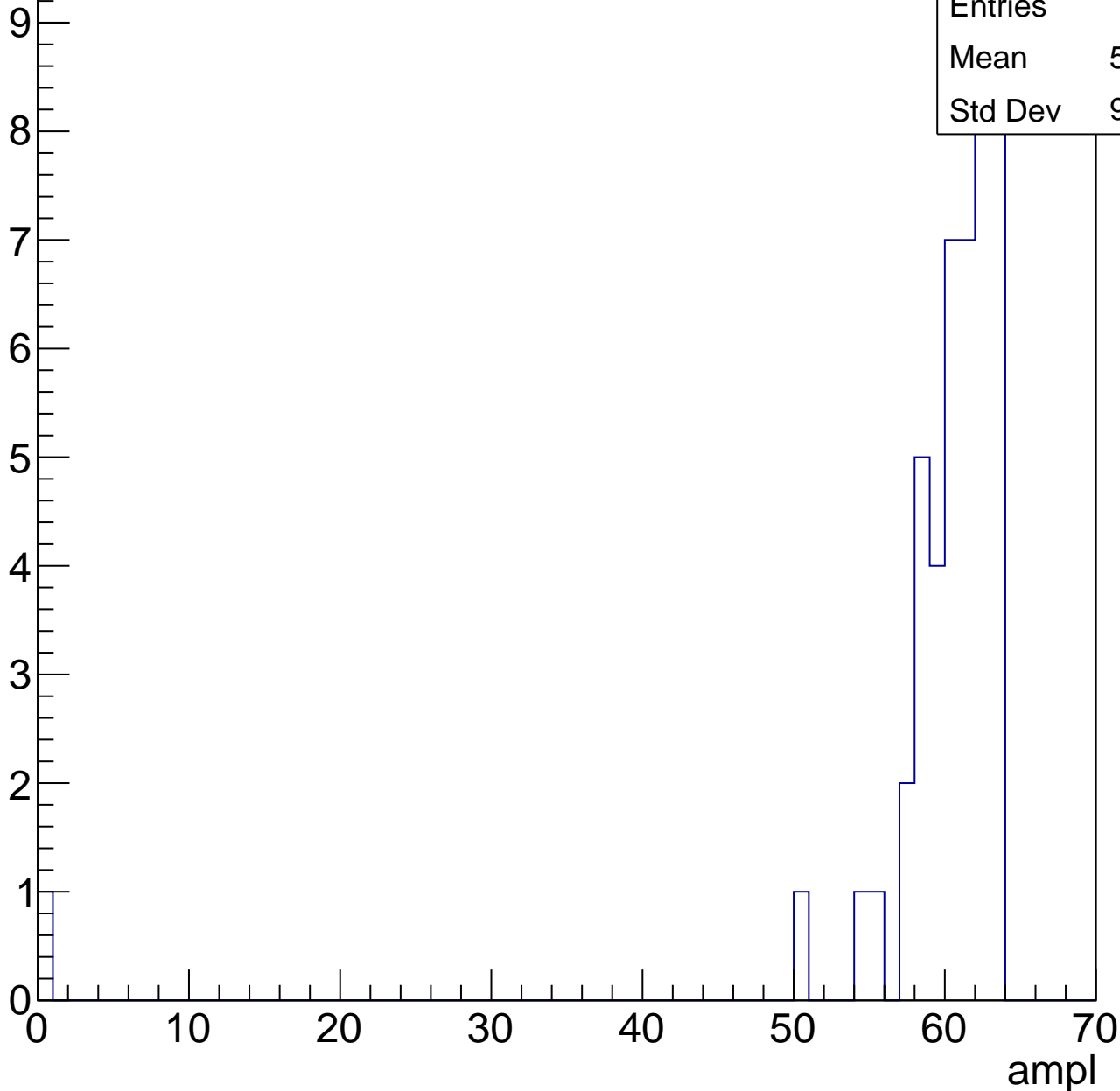


# B1L103S, U26-ch33, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	46
Mean	58.87
Std Dev	9.159



# B1L103S, U26-ch33, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry





# B1L103S, U26-ch33, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

18  
16  
14  
12  
10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

Entries	19
Mean	0
Std Dev	0

# B1L103S, U26-ch34, adc0

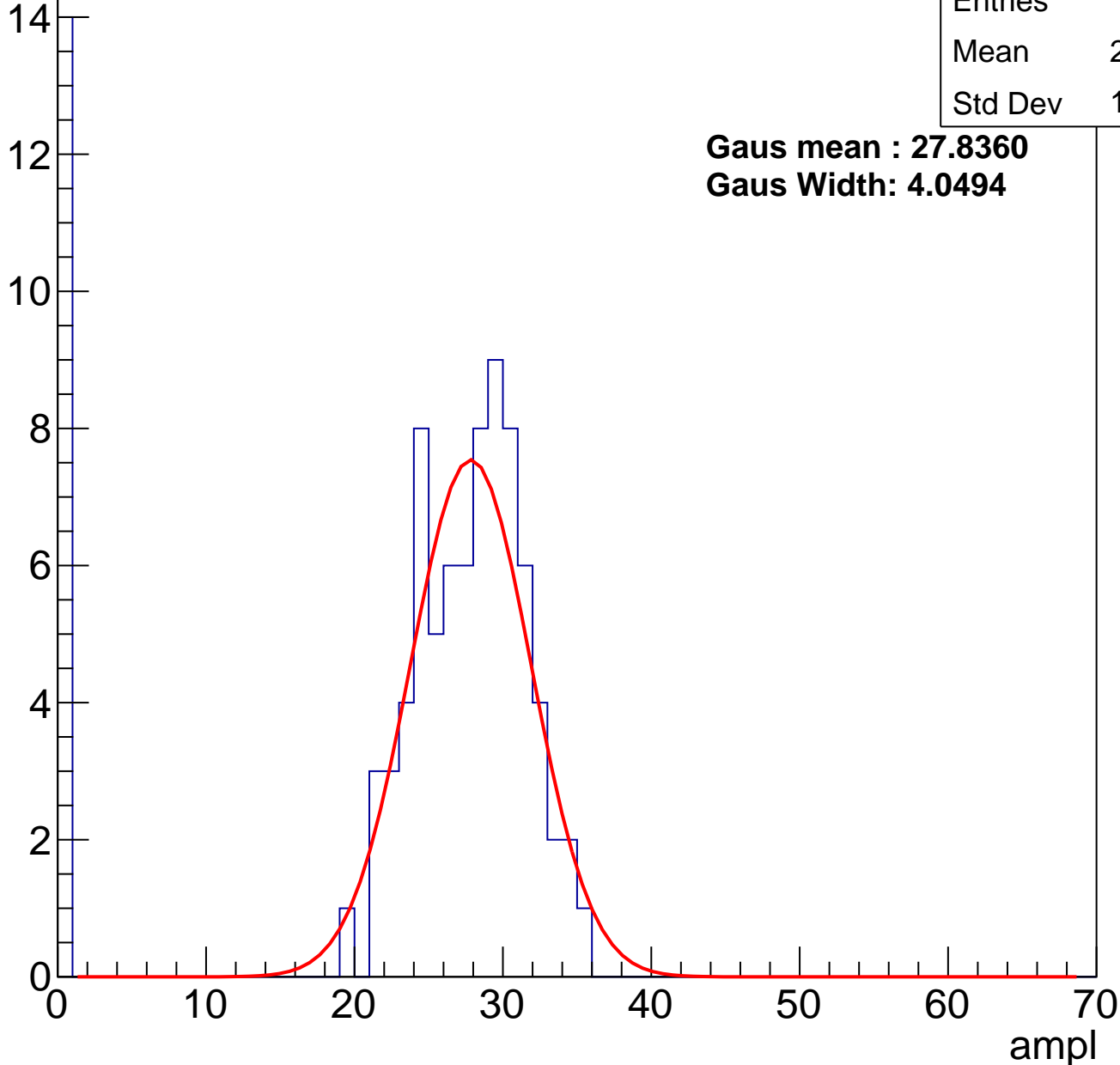
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	90
Mean	23.14
Std Dev	10.45

**Gaus mean : 27.8360**

**Gaus Width: 4.0494**

Entry



# B1L103S, U26-ch34, adc1

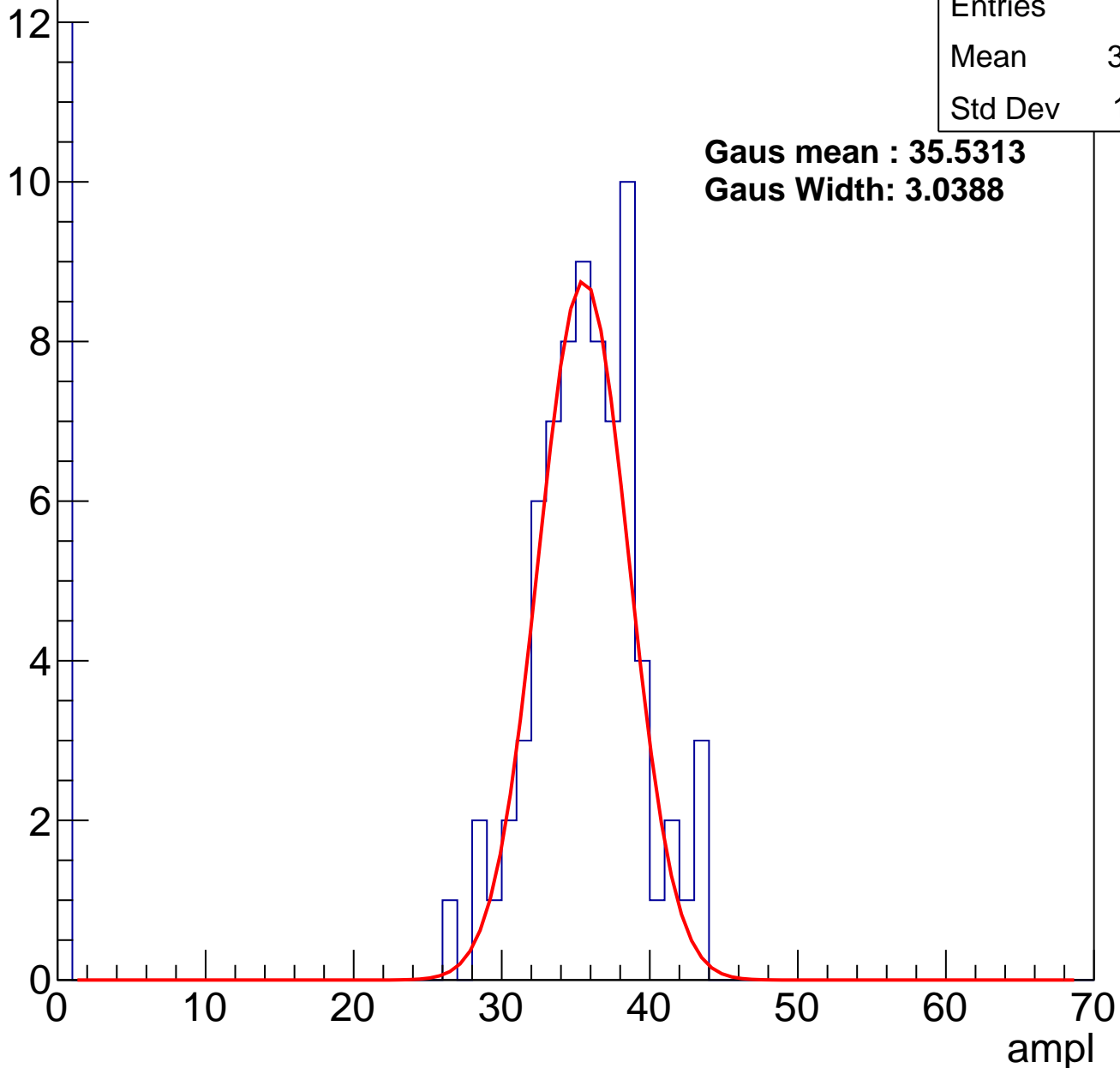
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	87
Mean	30.46
Std Dev	12.61

**Gaus mean : 35.5313**

**Gaus Width: 3.0388**

Entry



# B1L103S, U26-ch34, adc2

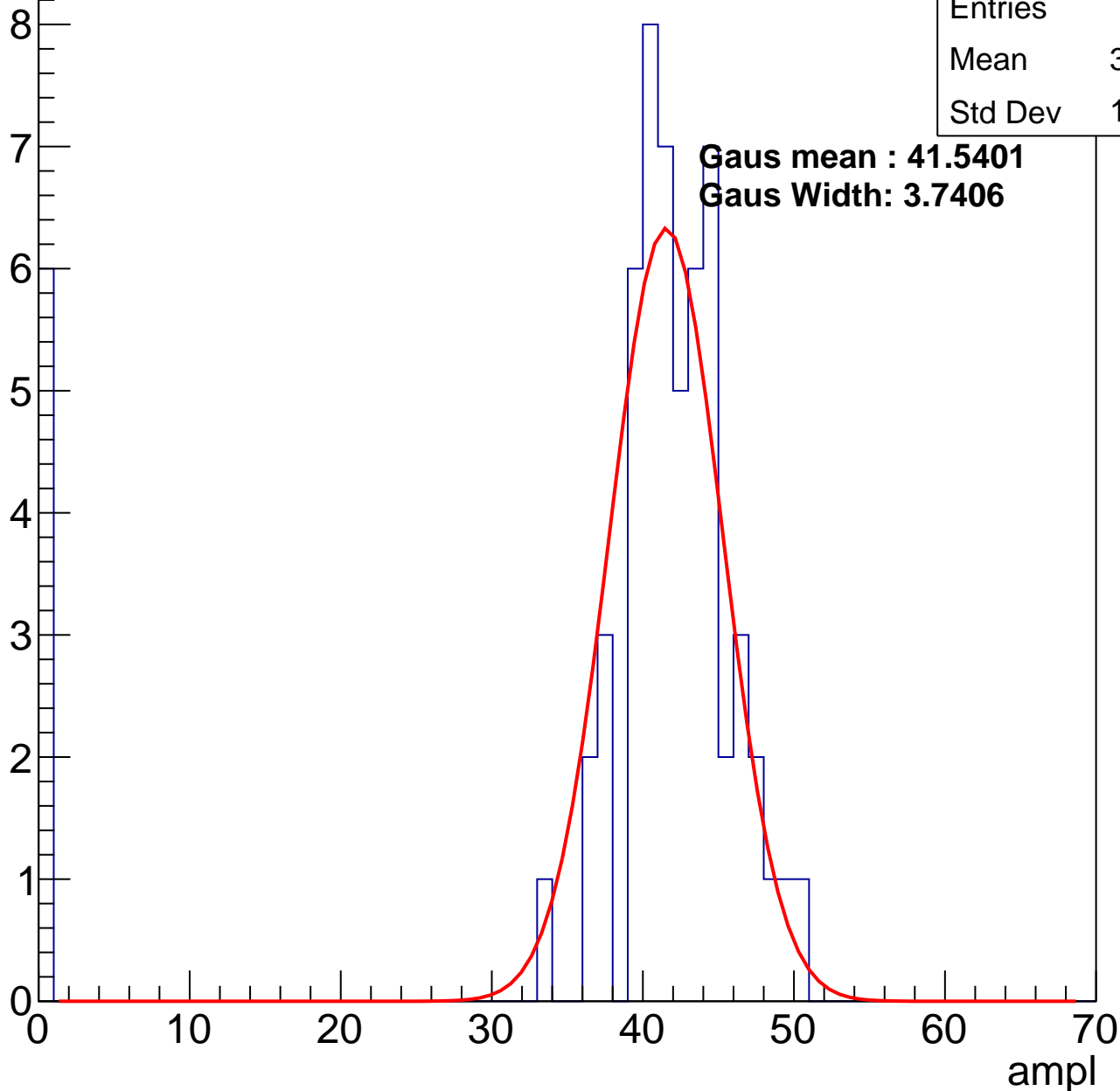
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	61
Mean	37.74
Std Dev	12.86

**Gaus mean : 41.5401**

**Gaus Width: 3.7406**

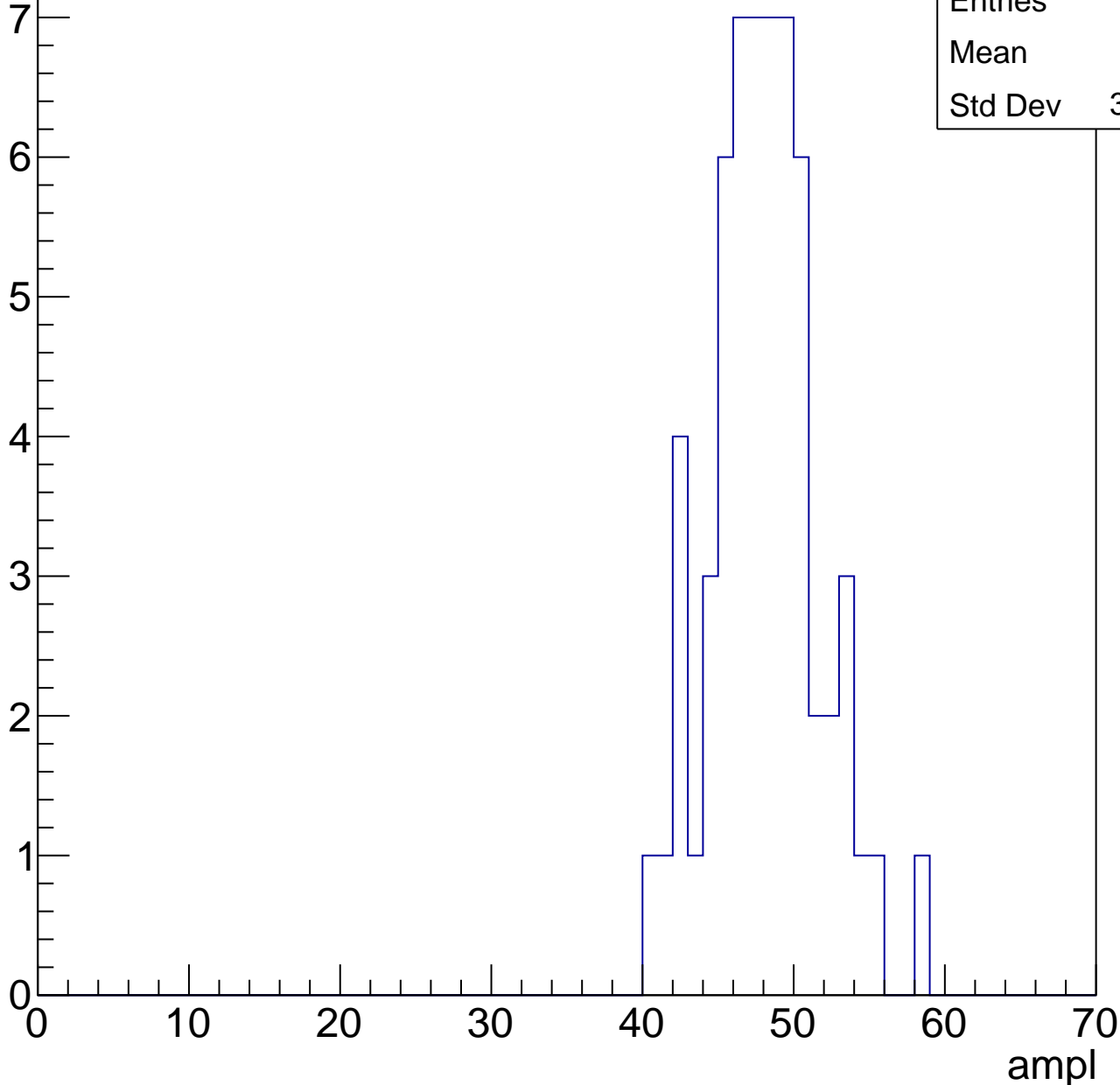


# B1L103S, U26-ch34, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	60
Mean	47.6
Std Dev	3.536

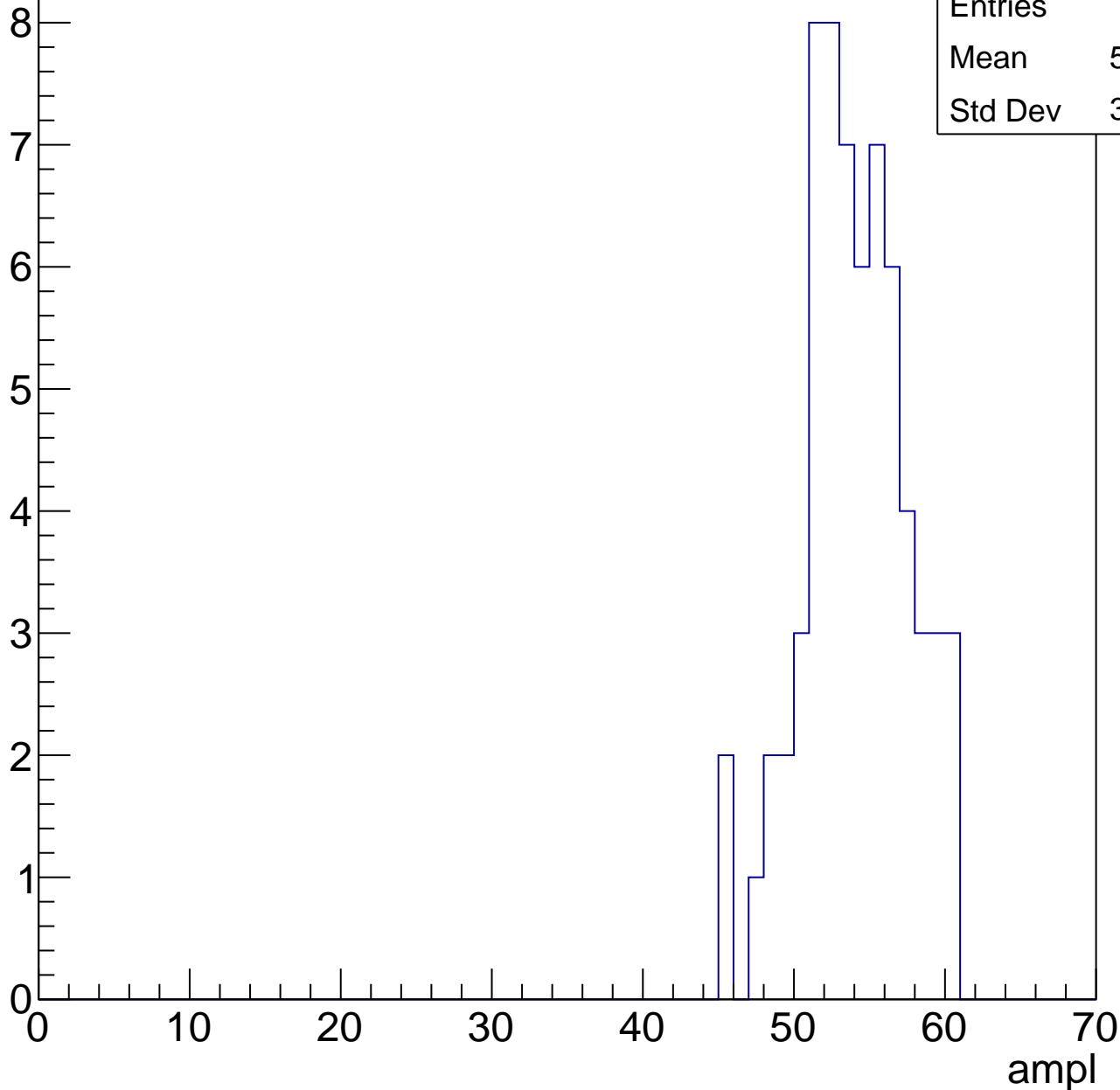


# B1L103S, U26-ch34, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

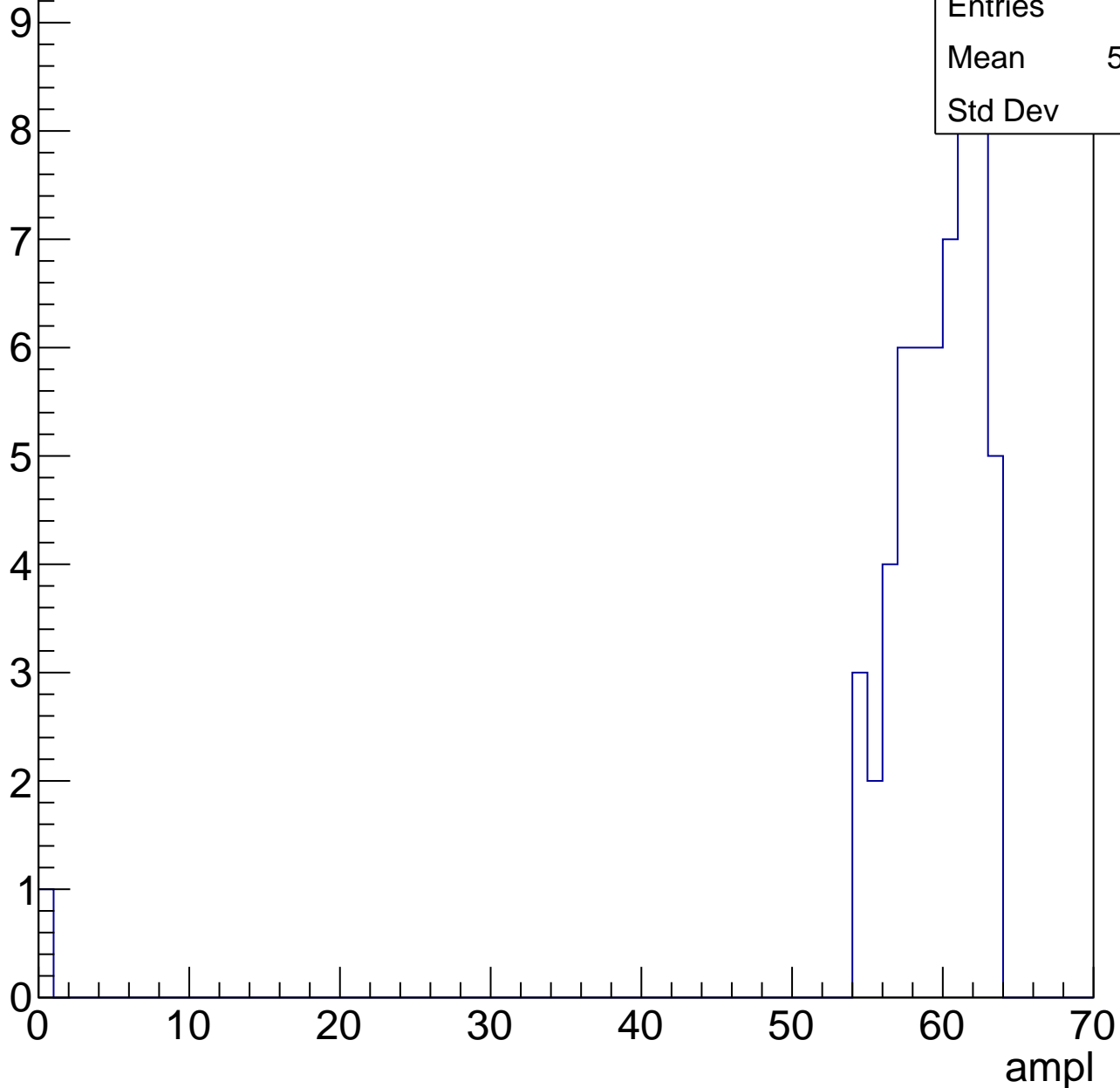
Entries	65
Mean	53.54
Std Dev	3.456



# B1L103S, U26-ch34, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

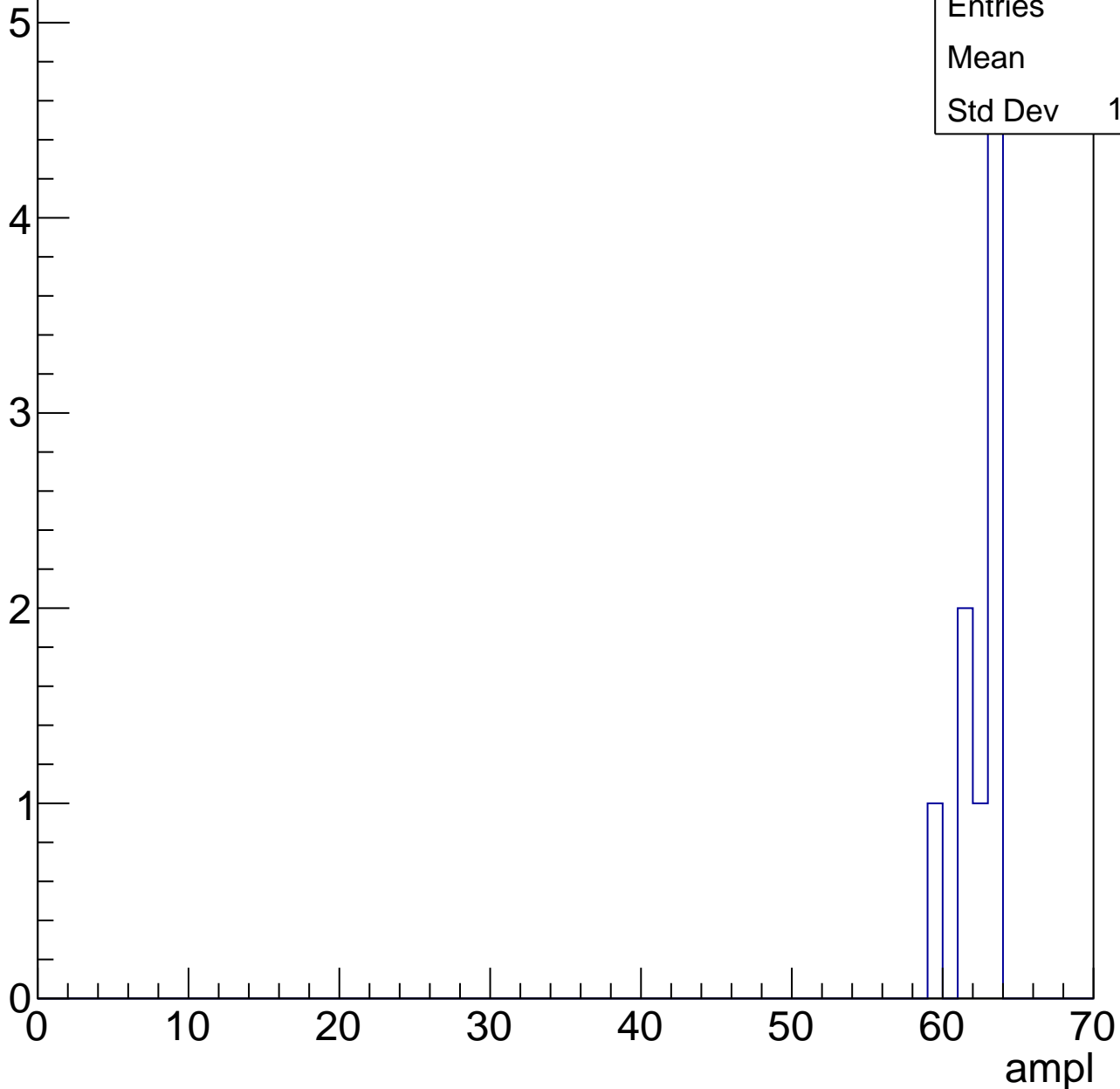


# B1L103S, U26-ch34, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	9
Mean	62
Std Dev	1.333





# B1L103S, U26-ch34, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

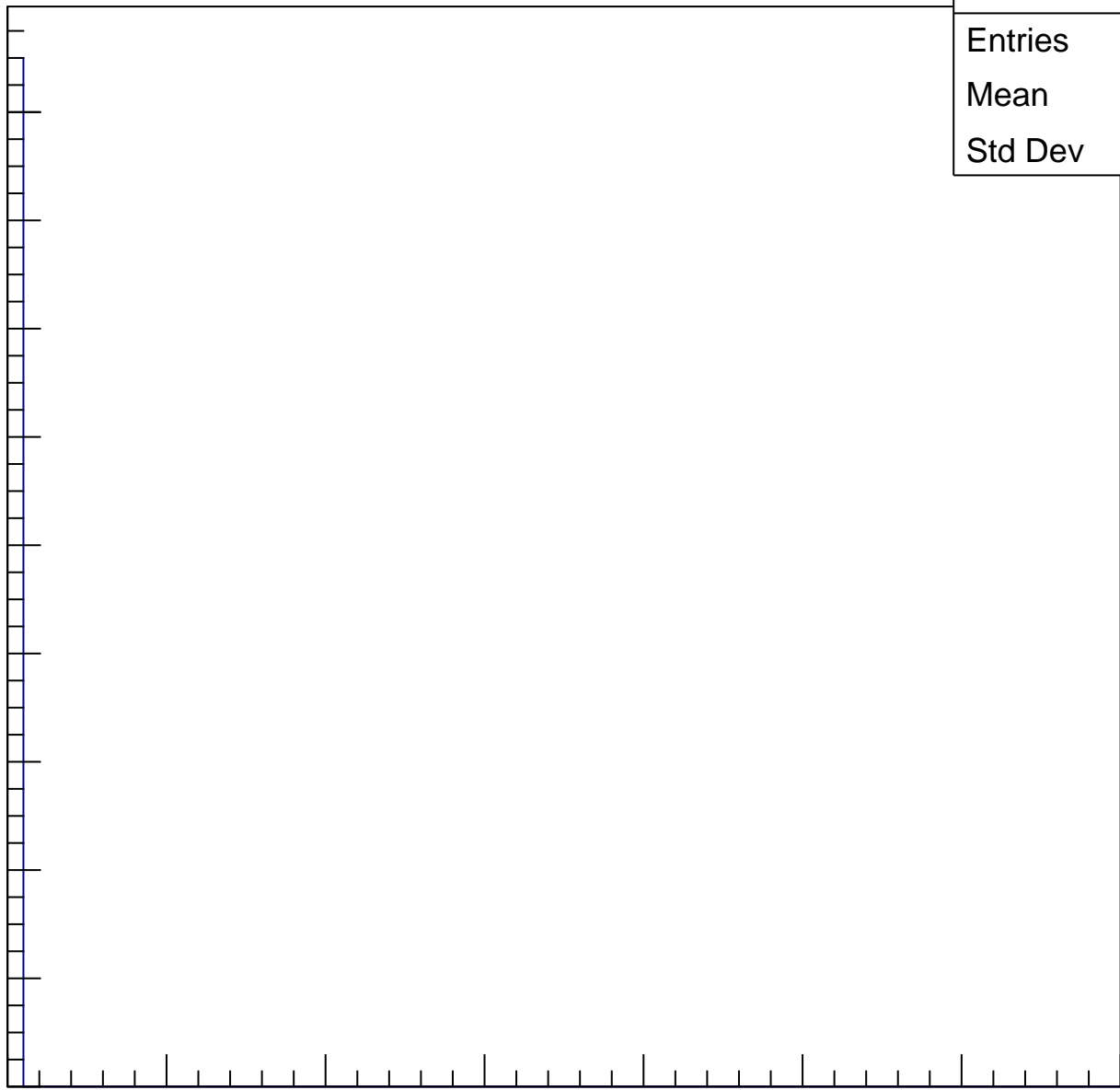
Entries	19
Mean	0
Std Dev	0

Entry

18  
16  
14  
12  
10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



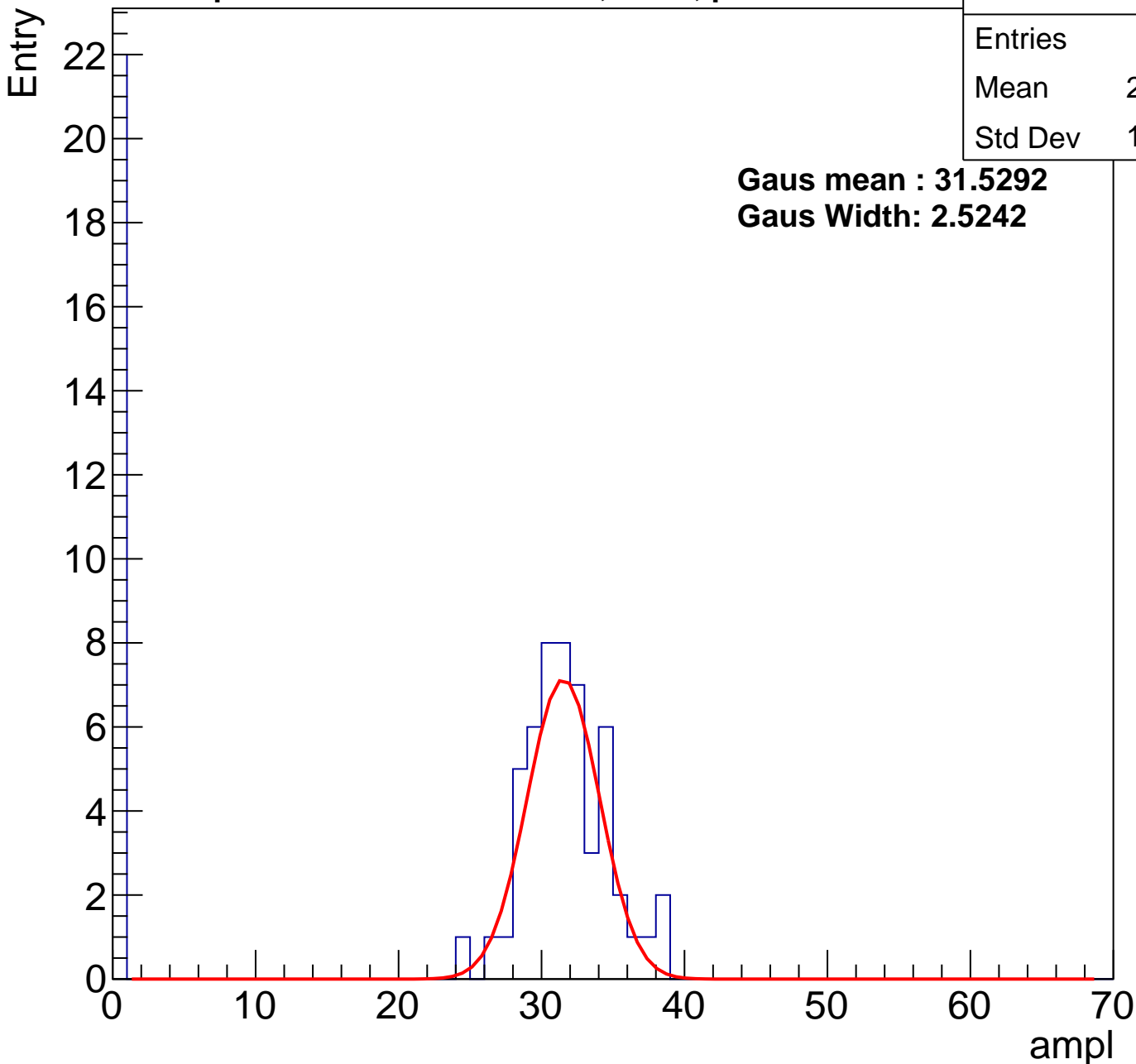
# B1L103S, U26-ch35, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	74
Mean	21.96
Std Dev	14.48

**Gaus mean : 31.5292**

**Gaus Width: 2.5242**



# B1L103S, U26-ch35, adc1

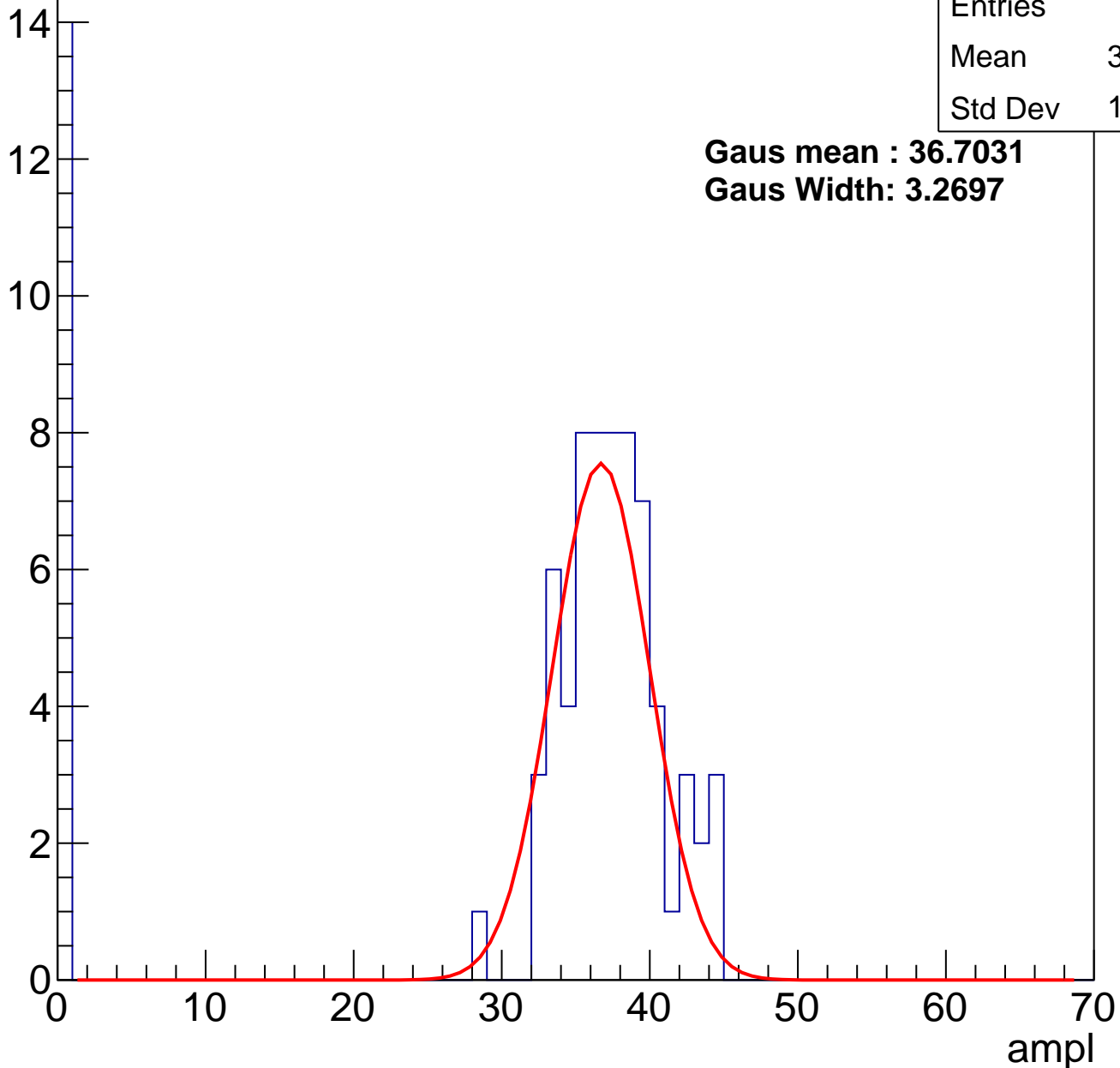
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	80
Mean	30.55
Std Dev	14.38

**Gaus mean : 36.7031**

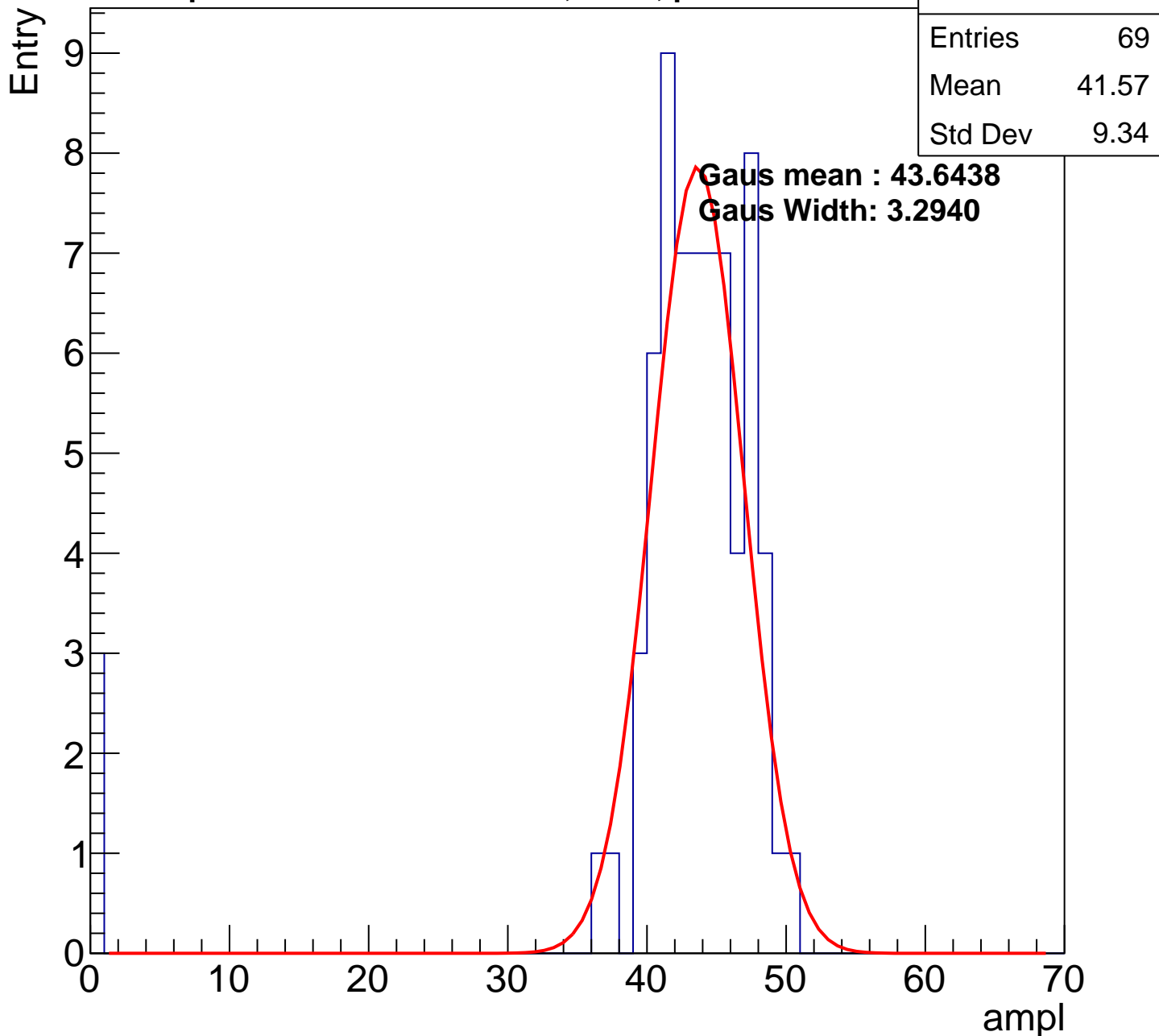
**Gaus Width: 3.2697**

Entry



# B1L103S, U26-ch35, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

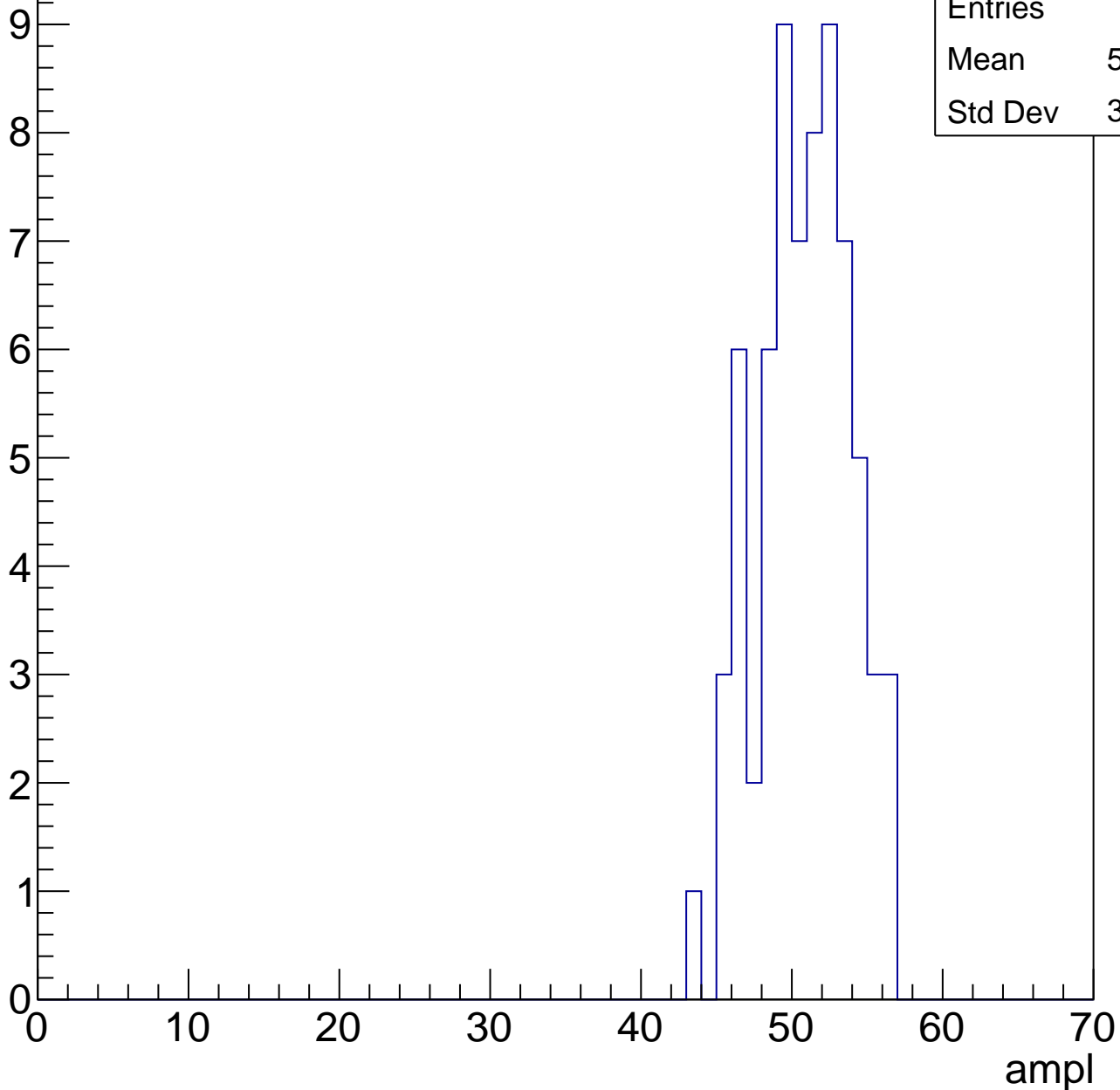


# B1L103S, U26-ch35, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	69
Mean	50.39
Std Dev	3.023

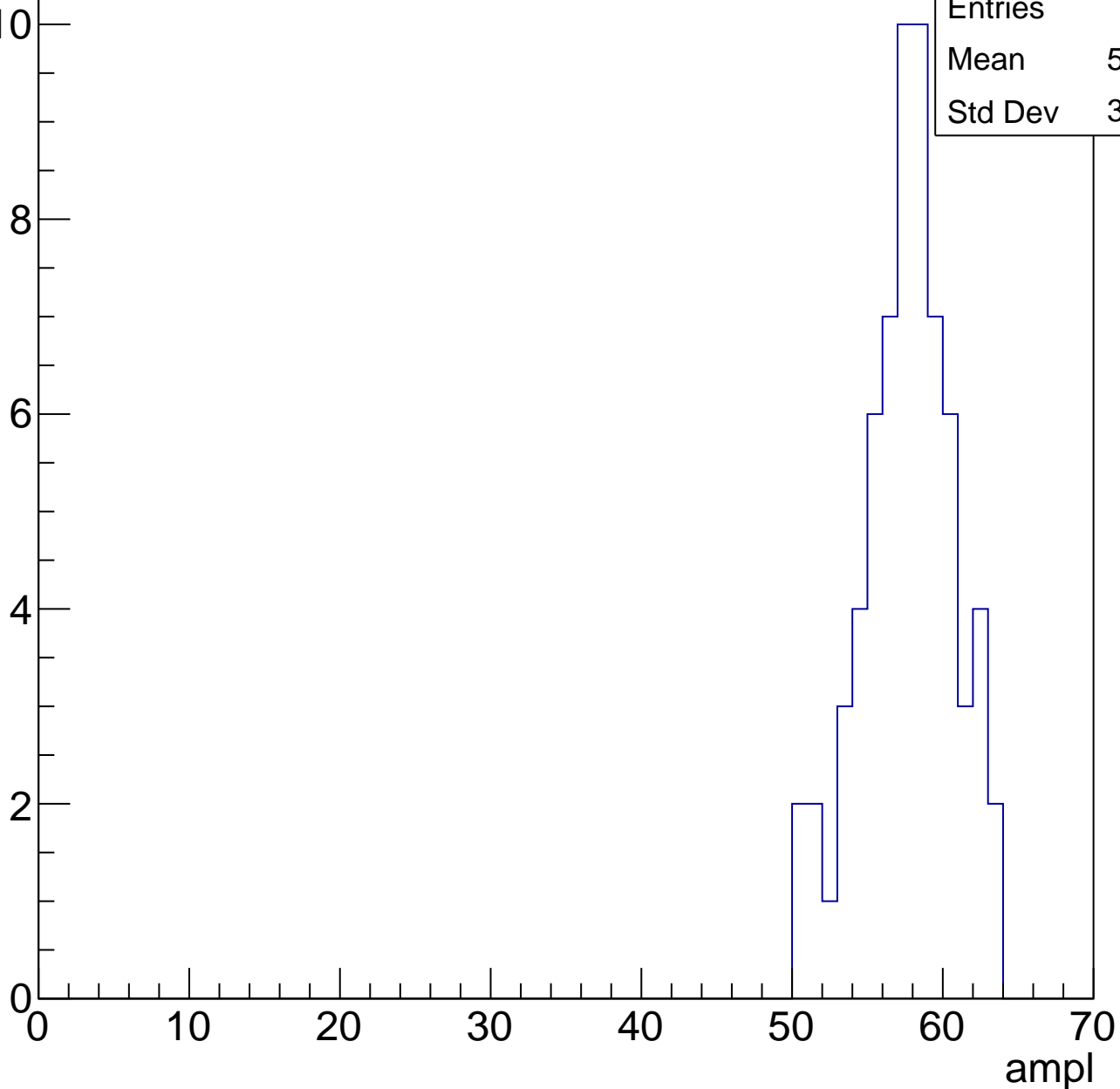


# B1L103S, U26-ch35, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	67
Mean	57.18
Std Dev	3.042

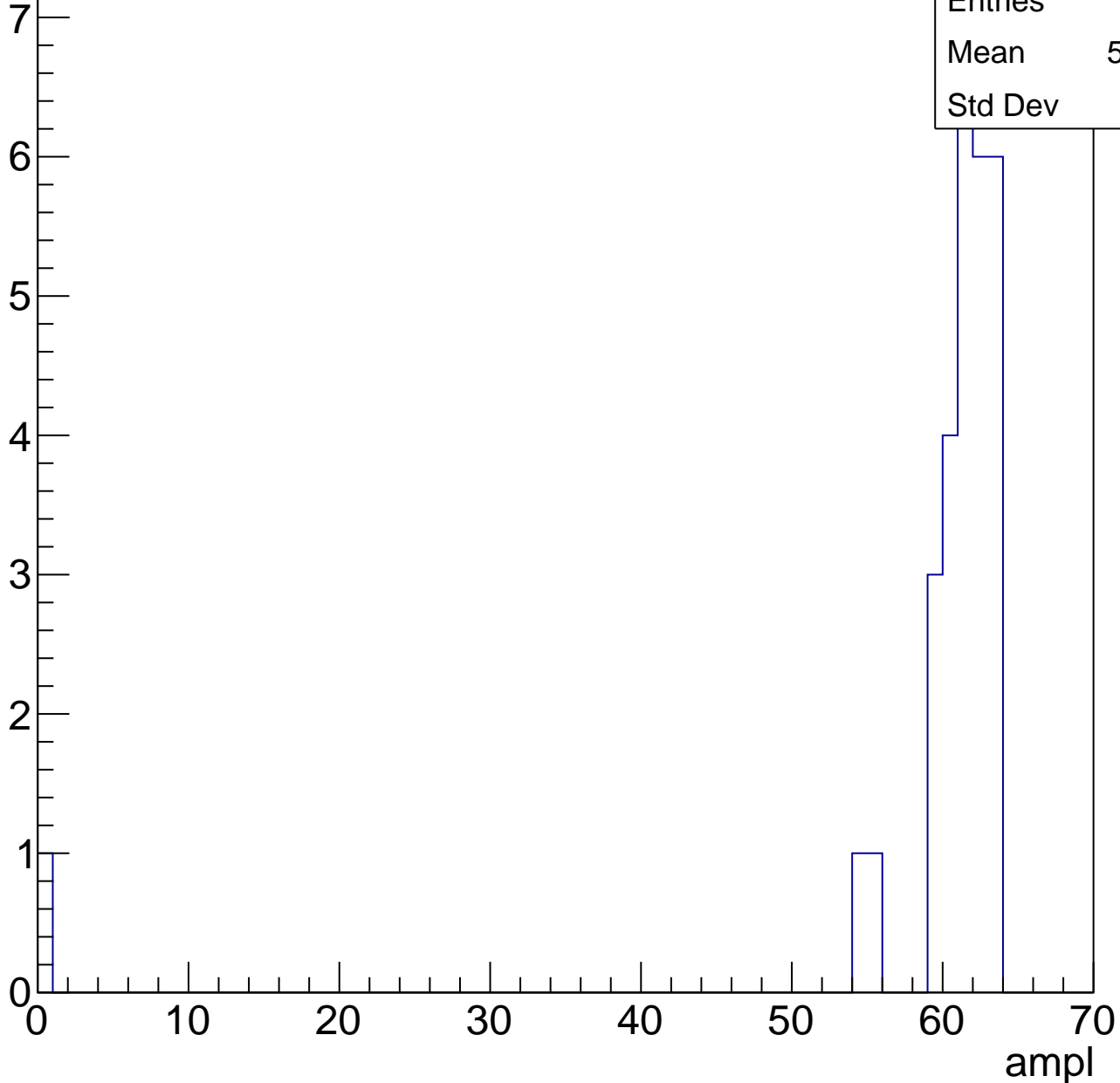


# B1L103S, U26-ch35, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	29
Mean	58.72
Std Dev	11.3



# B1L103S, U26-ch35, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry





# B1L103S, U26-ch35, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

18  
16  
14  
12  
10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

Entries	19
Mean	0
Std Dev	0

# B1L103S, U26-ch36, adc0

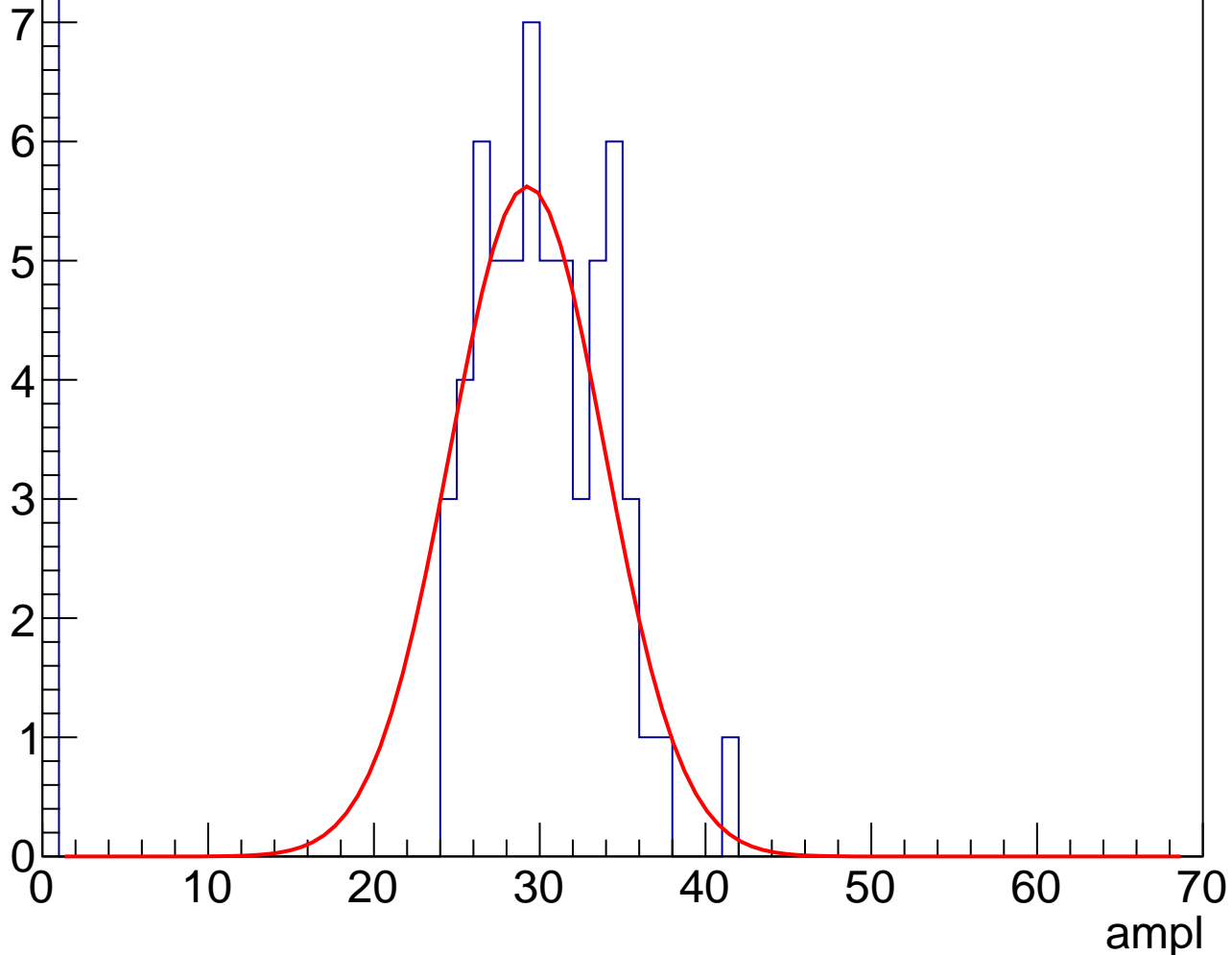
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	69
Mean	26.01
Std Dev	10.65

**Gaus mean : 29.2579**

**Gaus Width: 4.6682**



# B1L103S, U26-ch36, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	76
Mean	30.71
Std Dev	13

**Gaus mean : 36.4222**

**Gaus Width: 3.7512**

Entry

10

8

6

4

2

0

0

10

20

30

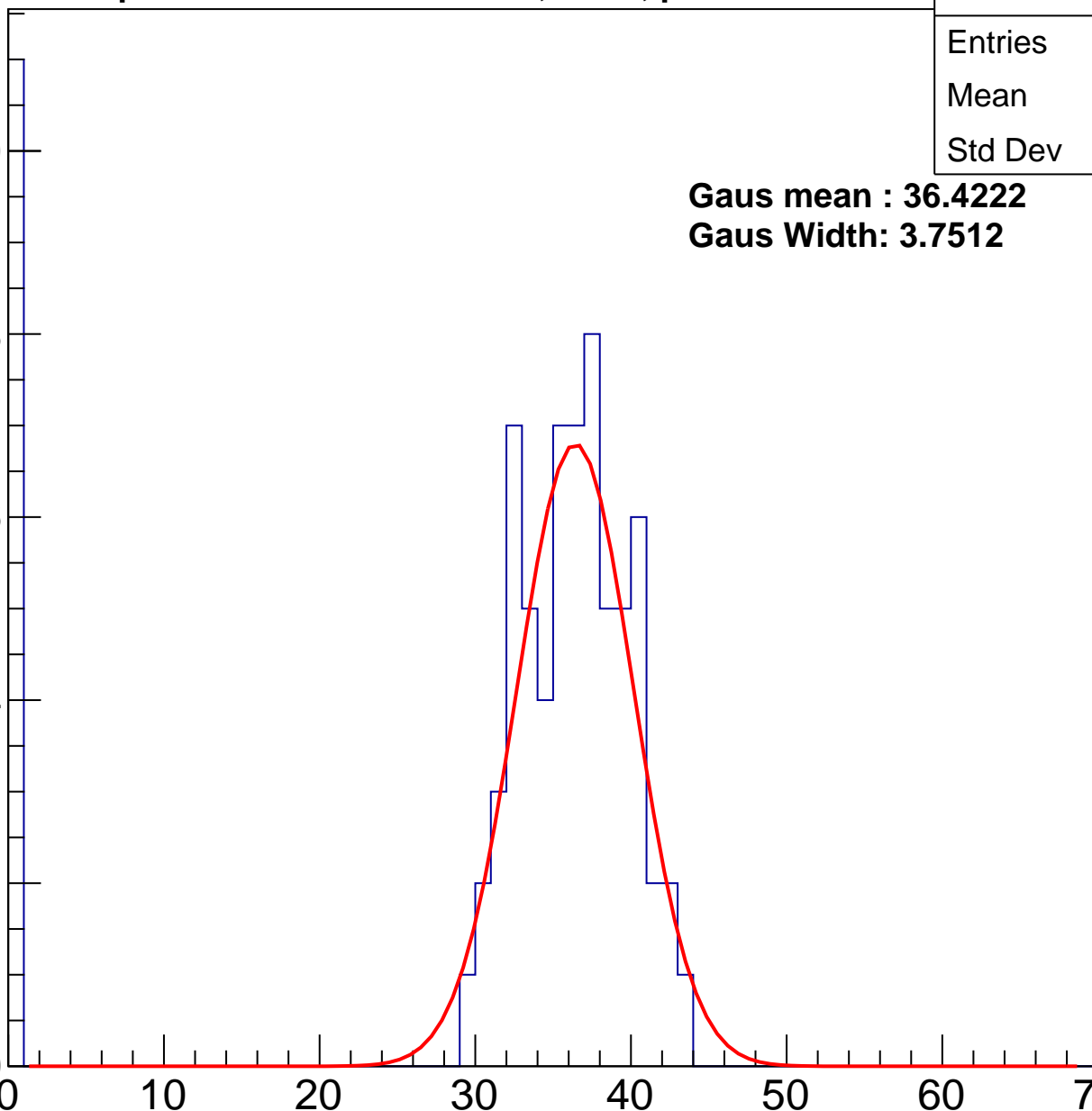
40

50

60

70

ampl



# B1L103S, U26-ch36, adc2

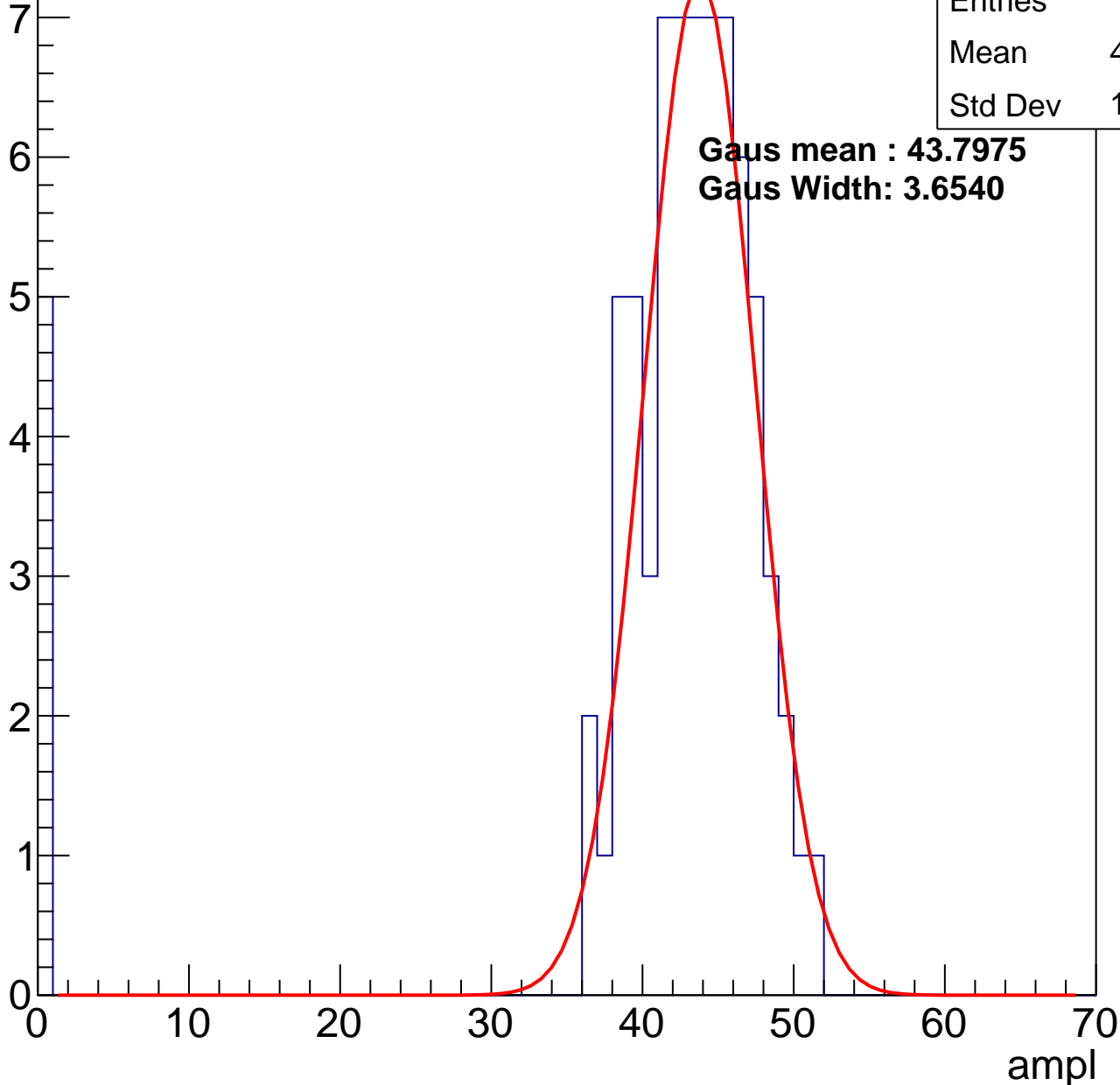
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	74
Mean	40.18
Std Dev	11.32

**Gaus mean : 43.7975**

**Gaus Width: 3.6540**

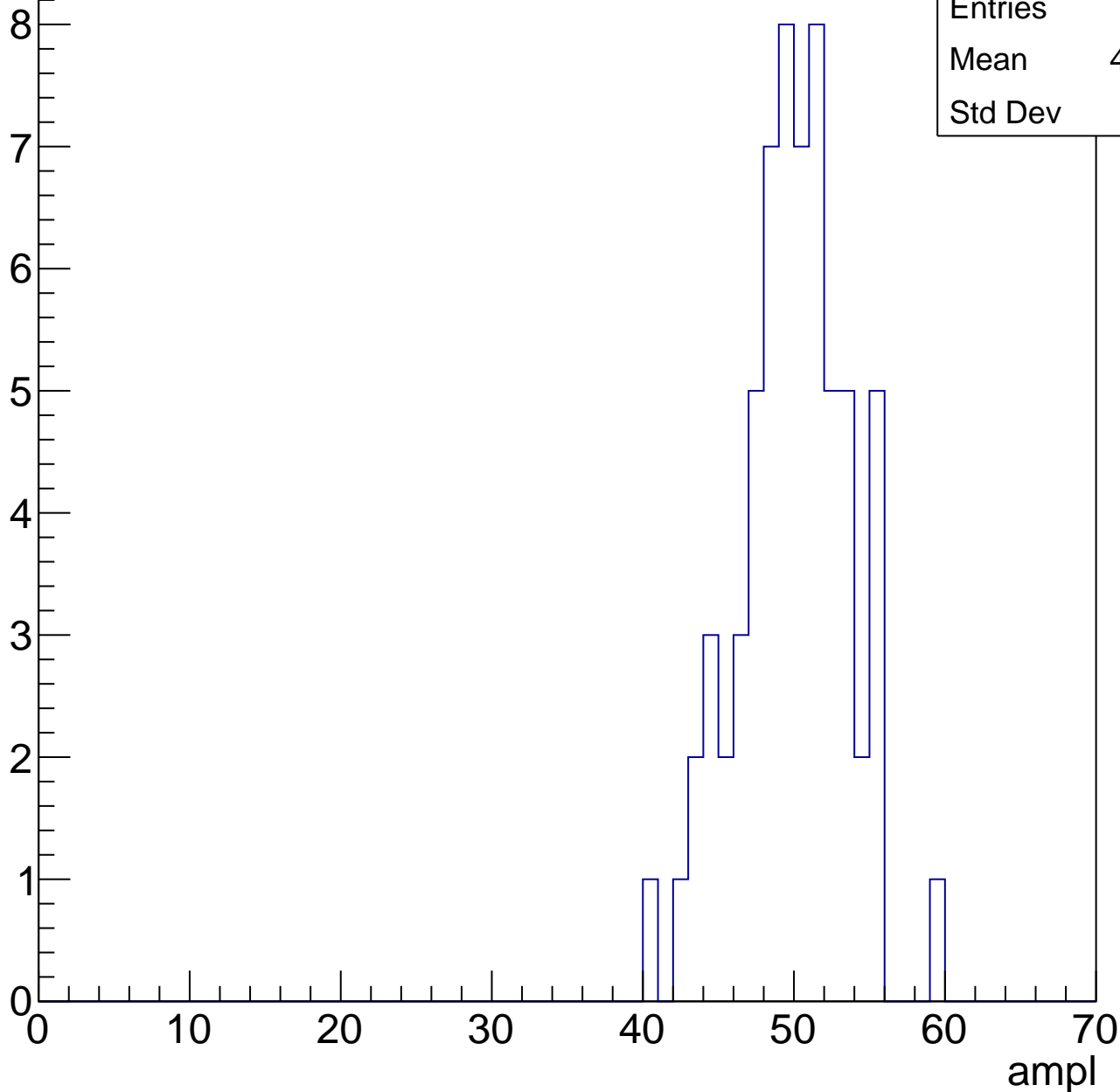


# B1L103S, U26-ch36, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	65
Mean	49.48
Std Dev	3.6

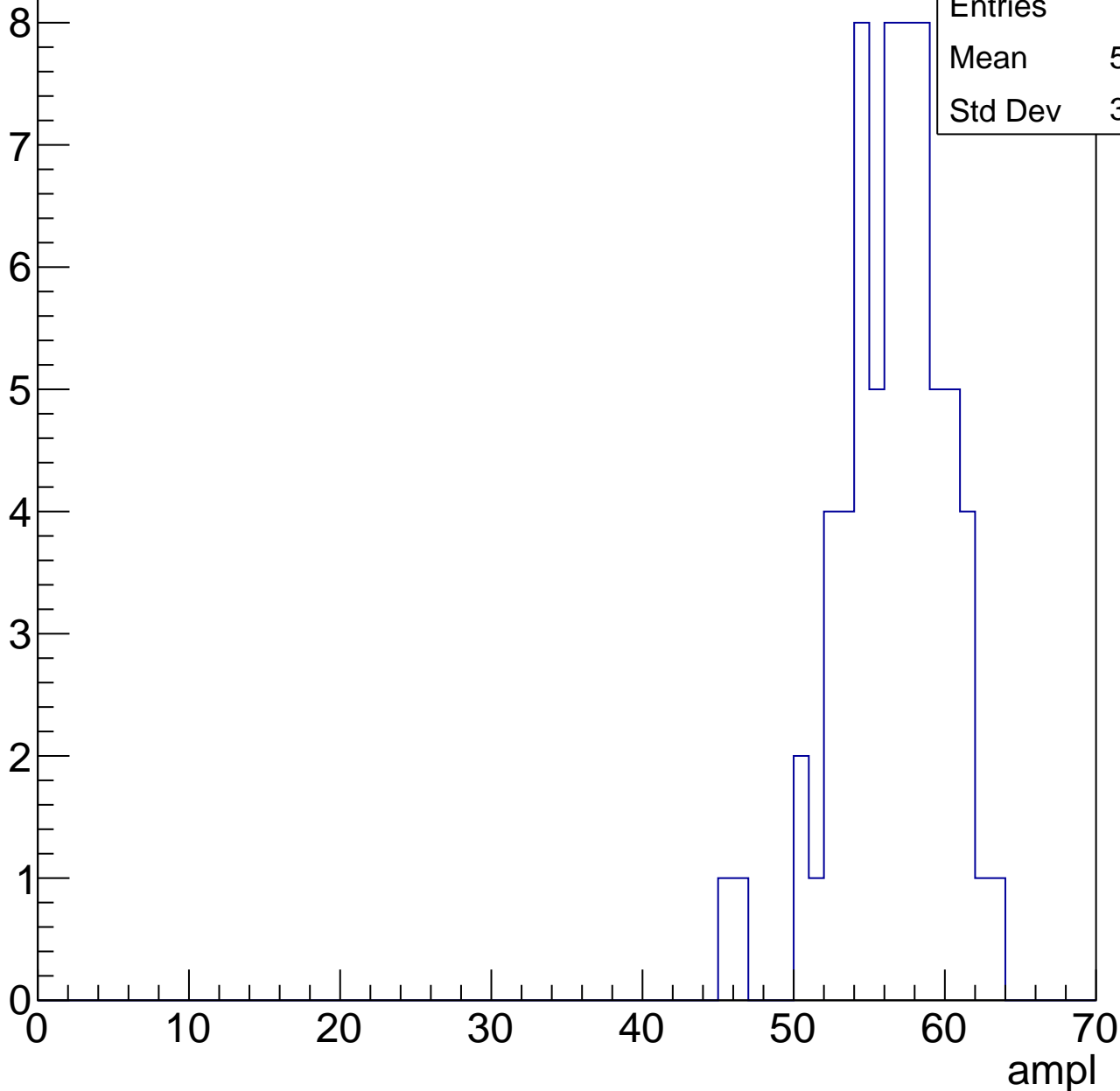


# B1L103S, U26-ch36, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	66
Mean	56.08
Std Dev	3.492

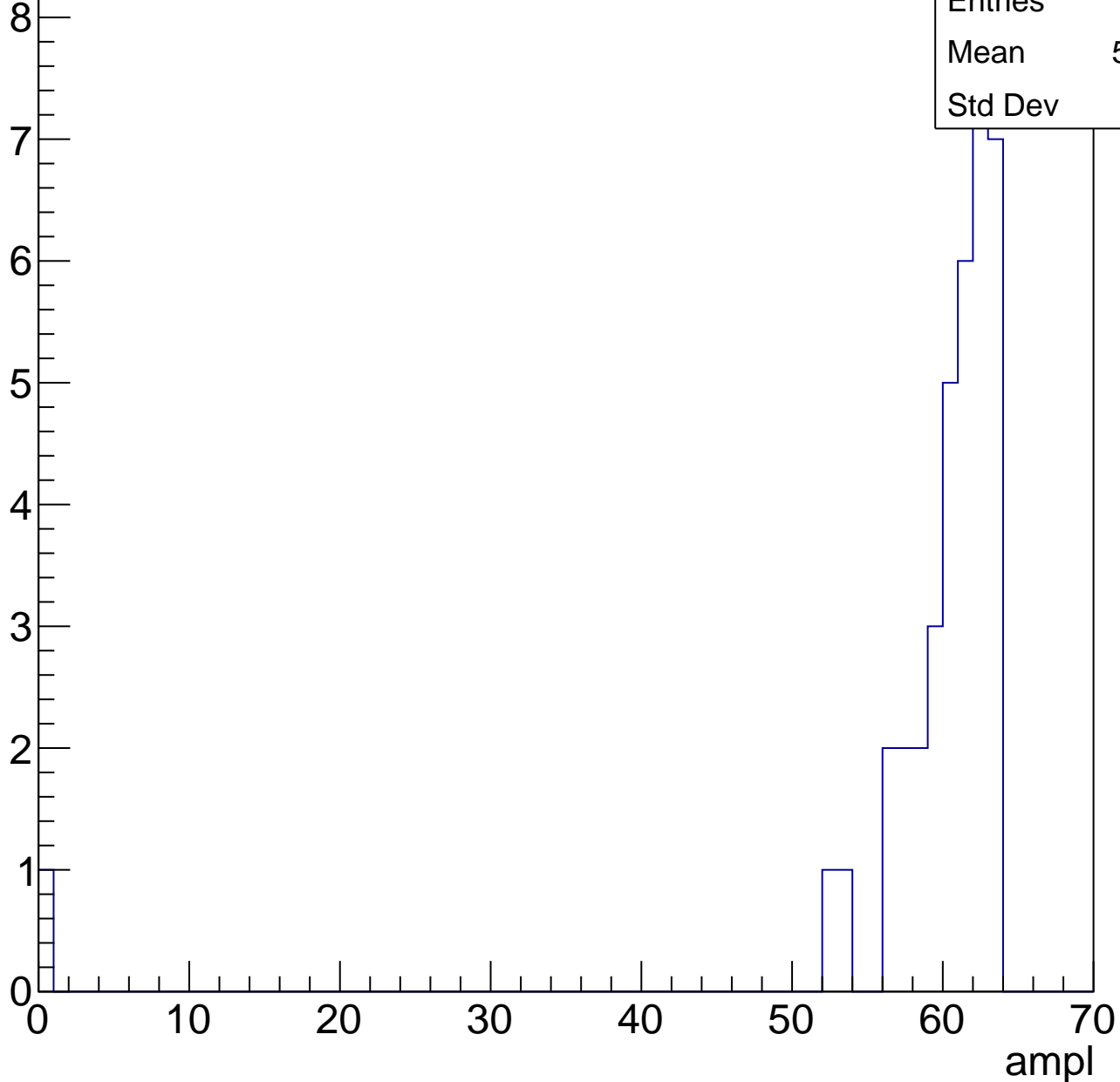


# B1L103S, U26-ch36, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	38
Mean	58.61
Std Dev	10



# B1L103S, U26-ch36, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry





# B1L103S, U26-ch36, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

18  
16  
14  
12  
10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

Entries	19
Mean	0
Std Dev	0

# B1L103S, U26-ch37, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	92
Mean	24.72
Std Dev	11.76

**Gaus mean : 30.6240**

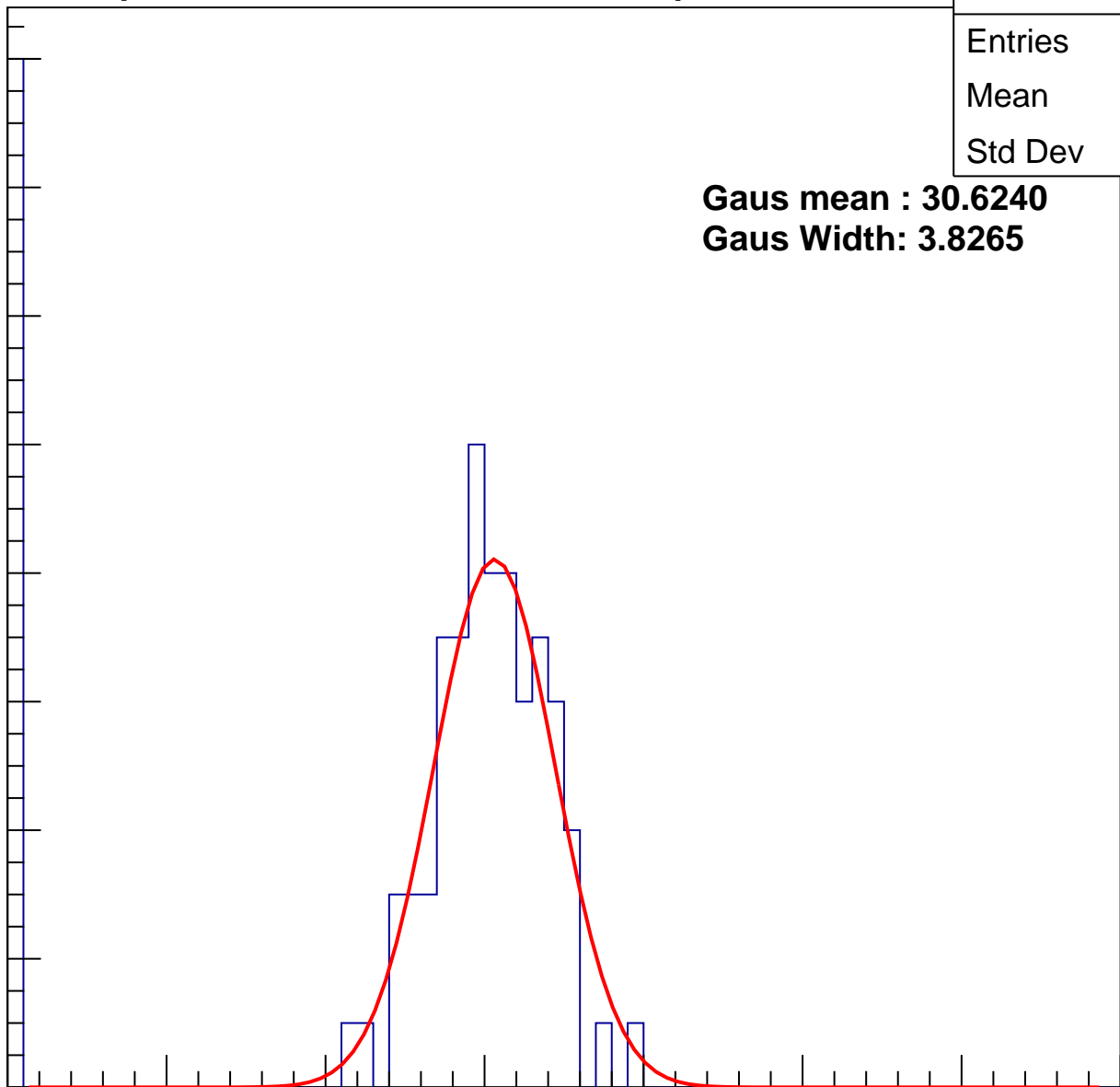
**Gaus Width: 3.8265**

Entry

16  
14  
12  
10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U26-ch37, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	90
Mean	32.01
Std Dev	13.59

**Gaus mean : 37.6261**

**Gaus Width: 3.6054**

Entry

12

10

8

6

4

2

0

0

10

20

30

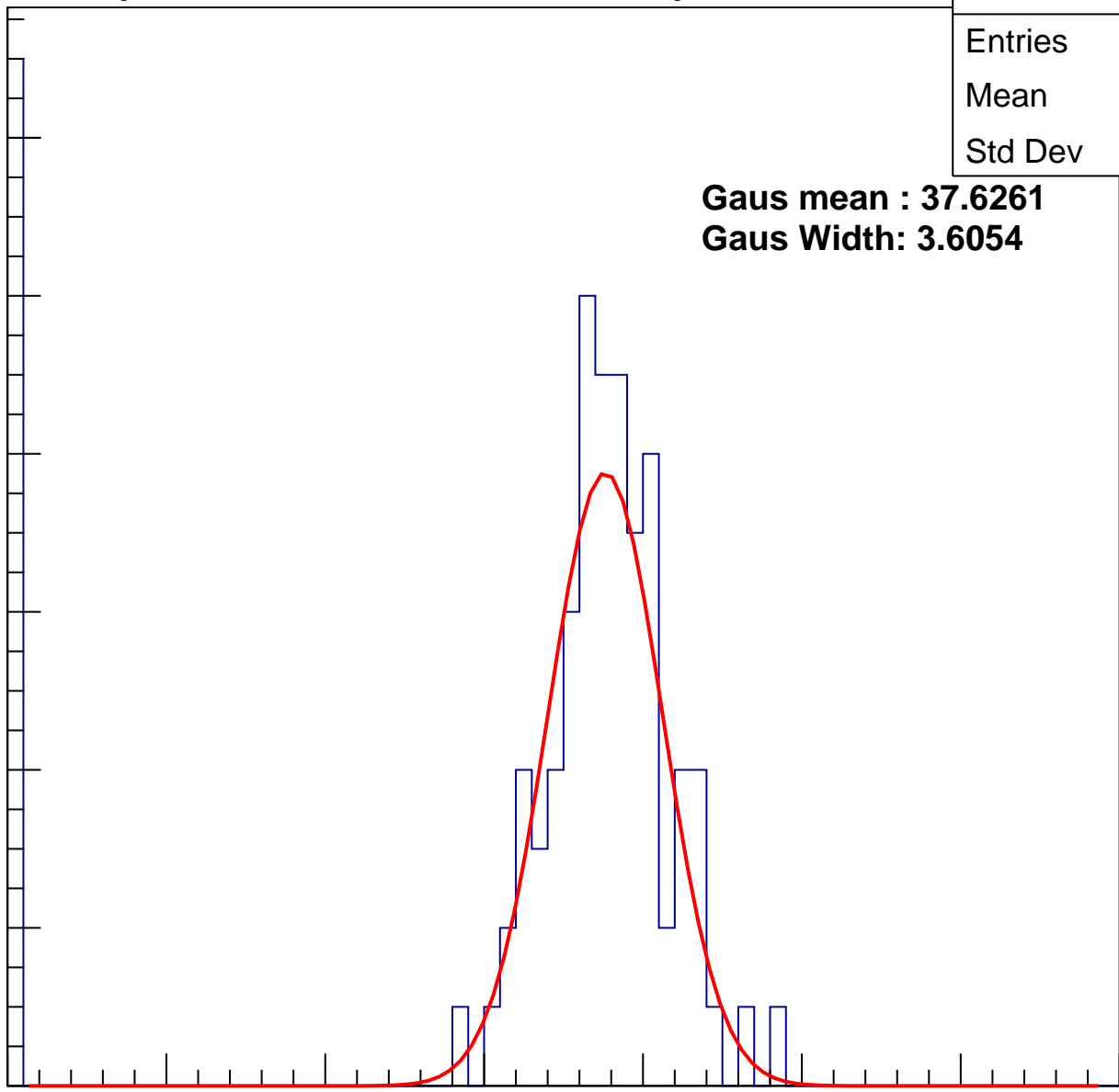
40

50

60

70

ampl



# B1L103S, U26-ch37, adc2

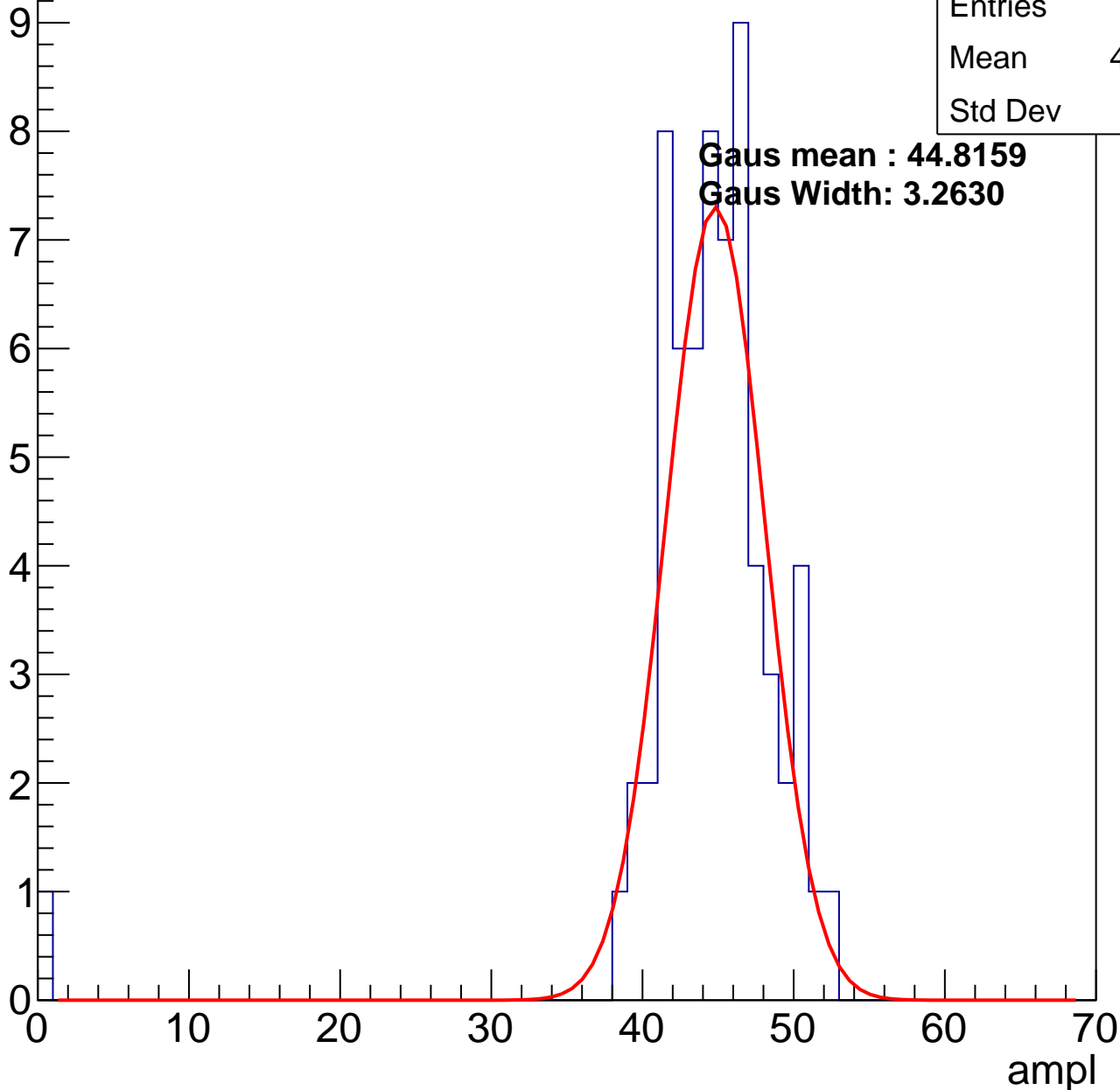
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	65
Mean	43.82
Std Dev	6.31

**Gaus mean : 44.8159**

**Gaus Width: 3.2630**

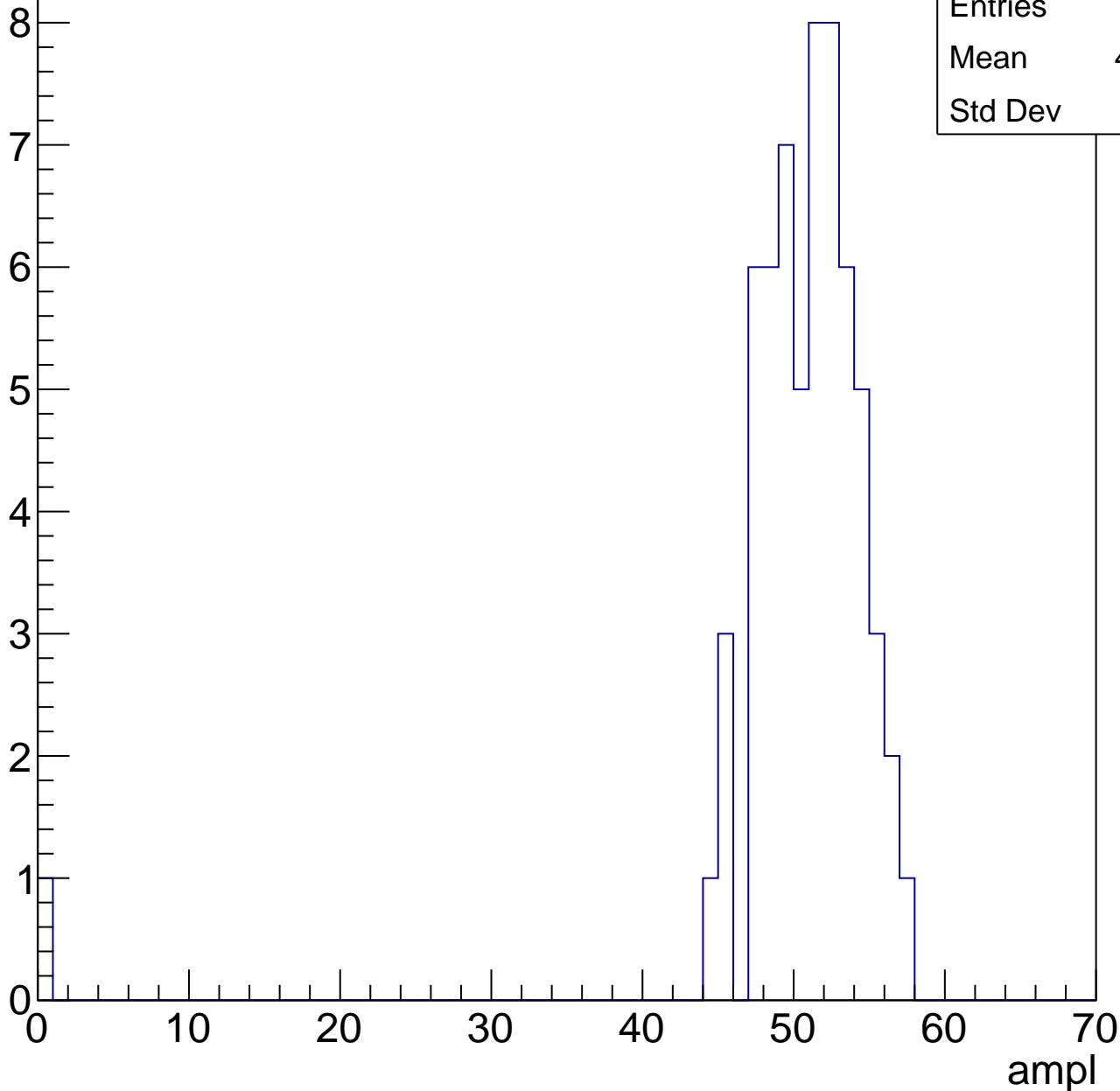


# B1L103S, U26-ch37, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

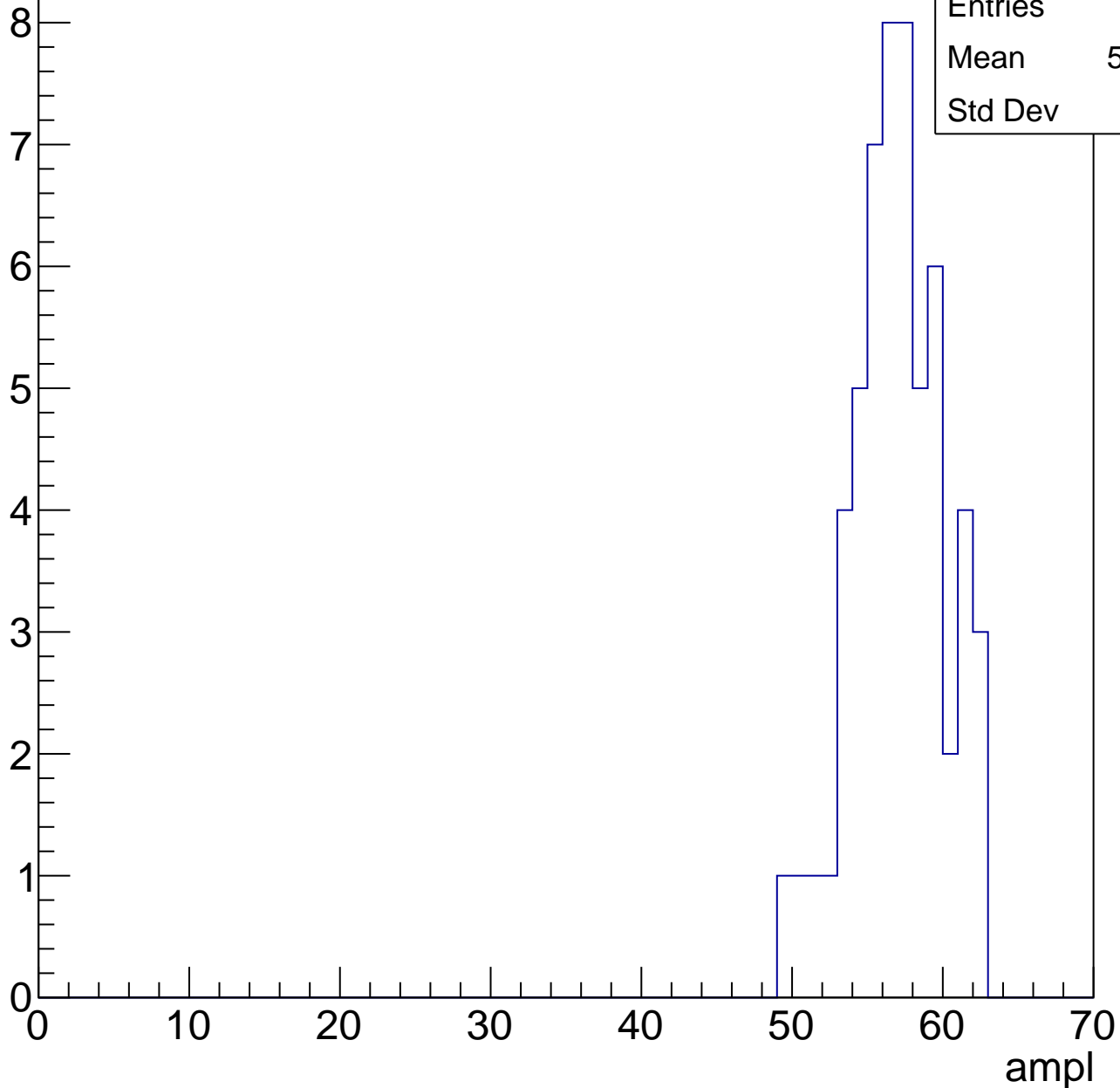
Entries	62
Mean	49.81
Std Dev	7.03



# B1L103S, U26-ch37, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



Entries	56
Mean	56.55
Std Dev	2.97

# B1L103S, U26-ch37, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	42
Mean	59.36
Std Dev	9.436

Entry

10

8

6

4

2

0

0

10

20

30

40

50

60

70

ampl

0

2

4

6

8

10

# B1L103S, U26-ch37, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



Entries	0
Mean	0
Std Dev	0



# B1L103S, U26-ch37, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



# B1L103S, U26-ch38, adc0

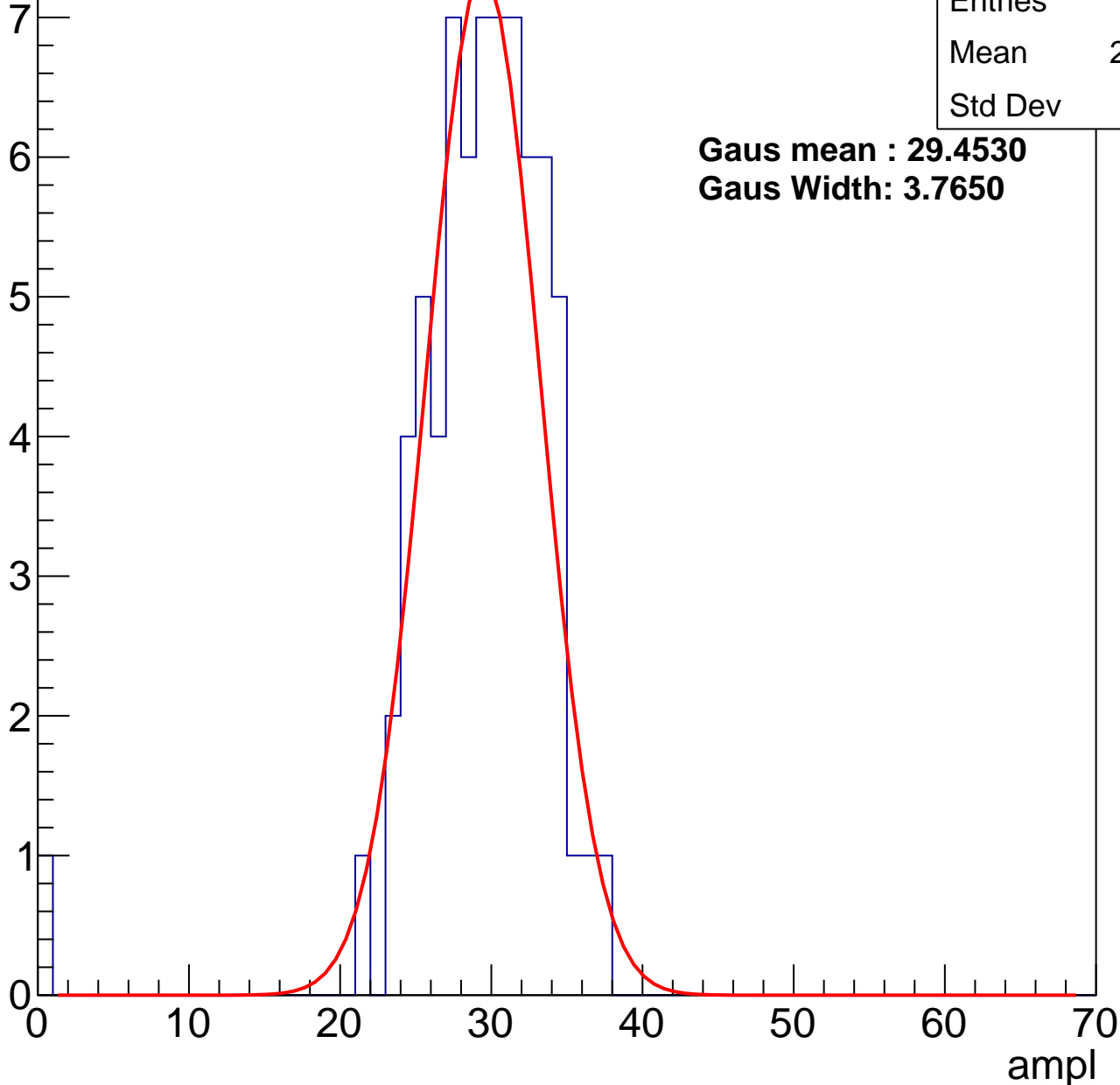
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	71
Mean	28.83
Std Dev	4.87

**Gaus mean : 29.4530**

**Gaus Width: 3.7650**



# B1L103S, U26-ch38, adc1

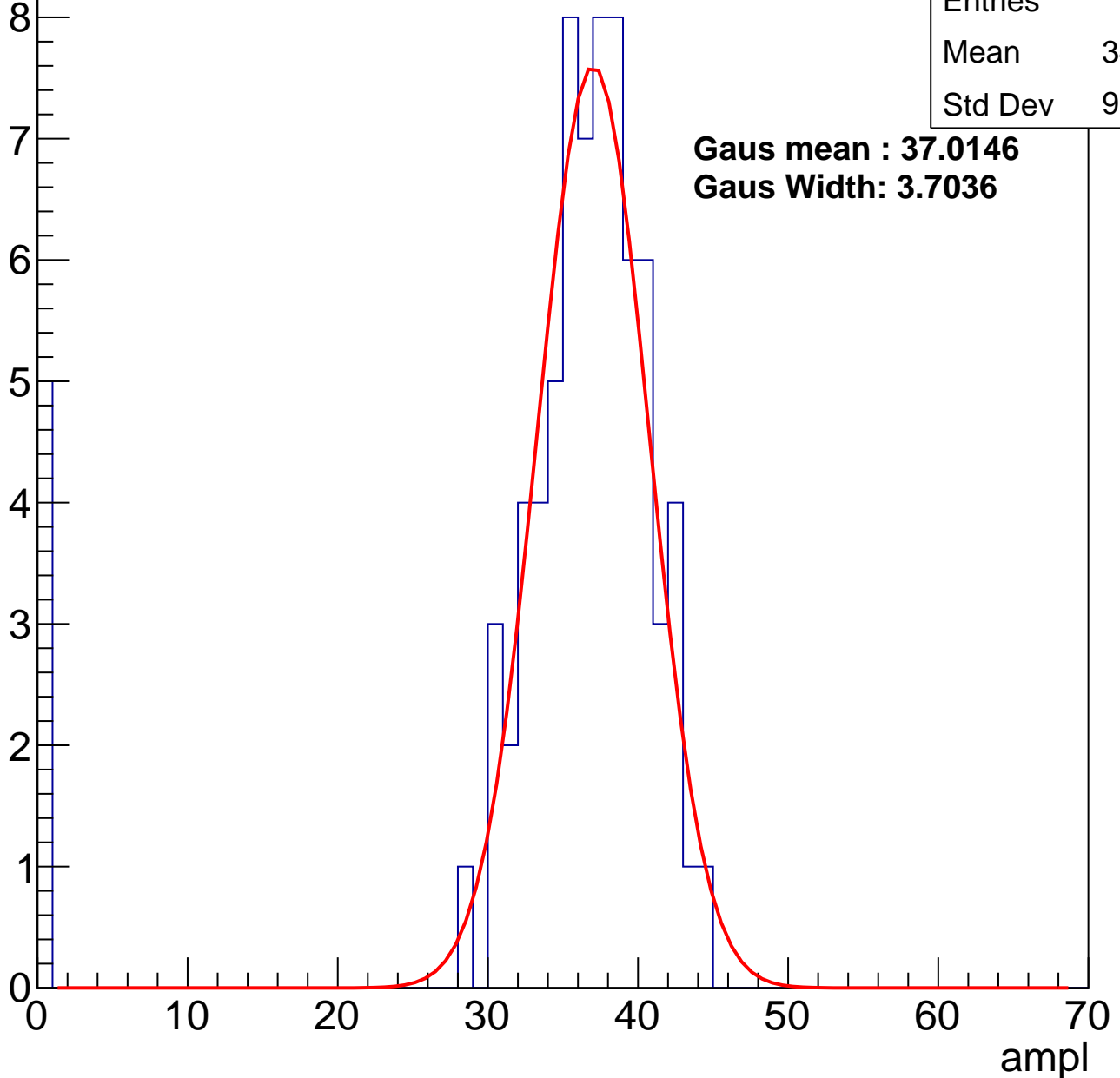
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	76
Mean	34.13
Std Dev	9.656

**Gaus mean : 37.0146**

**Gaus Width: 3.7036**



# B1L103S, U26-ch38, adc2

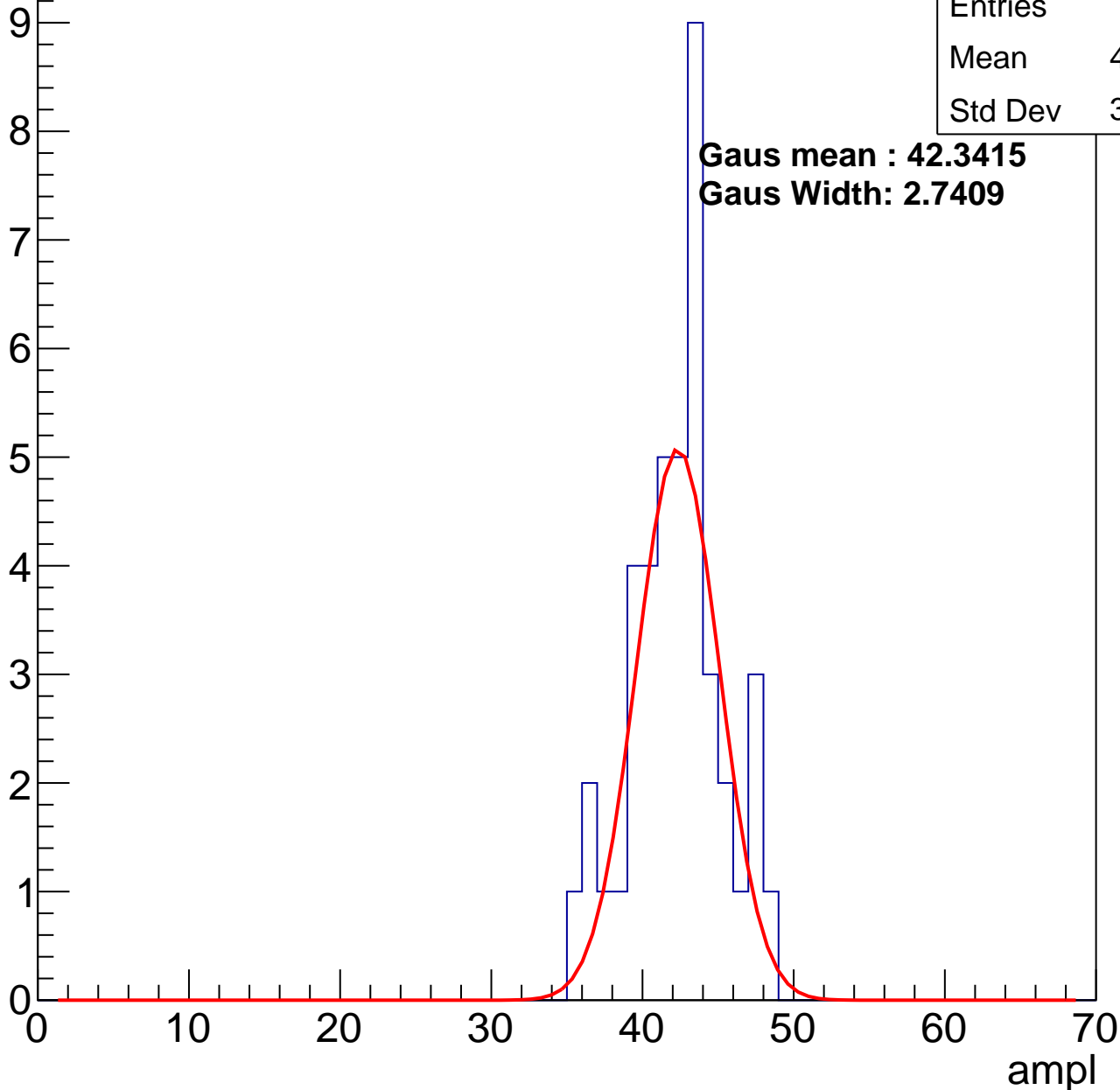
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	42
Mean	41.83
Std Dev	3.023

**Gaus mean : 42.3415**

**Gaus Width: 2.7409**

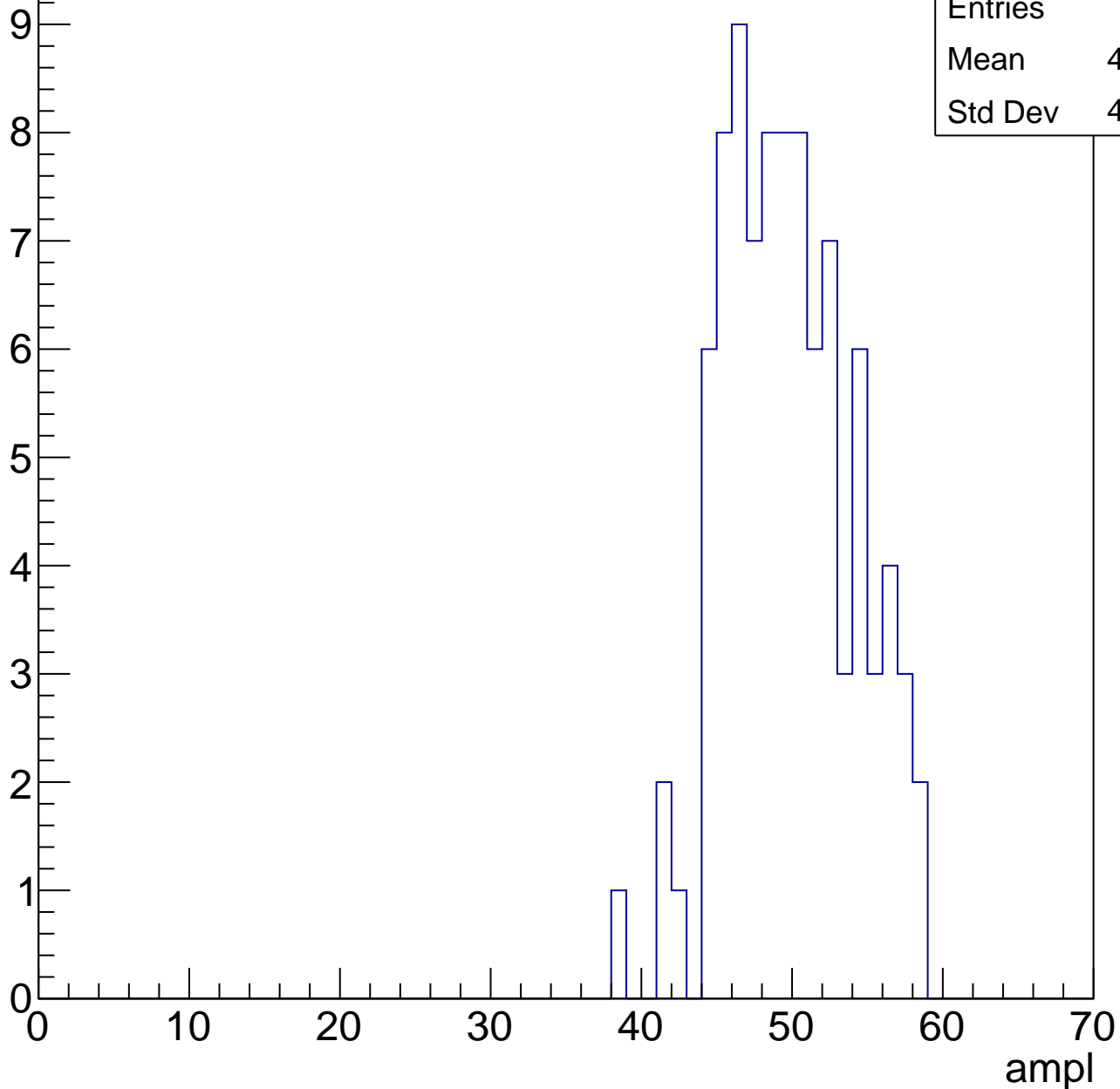


# B1L103S, U26-ch38, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	92
Mean	49.28
Std Dev	4.218

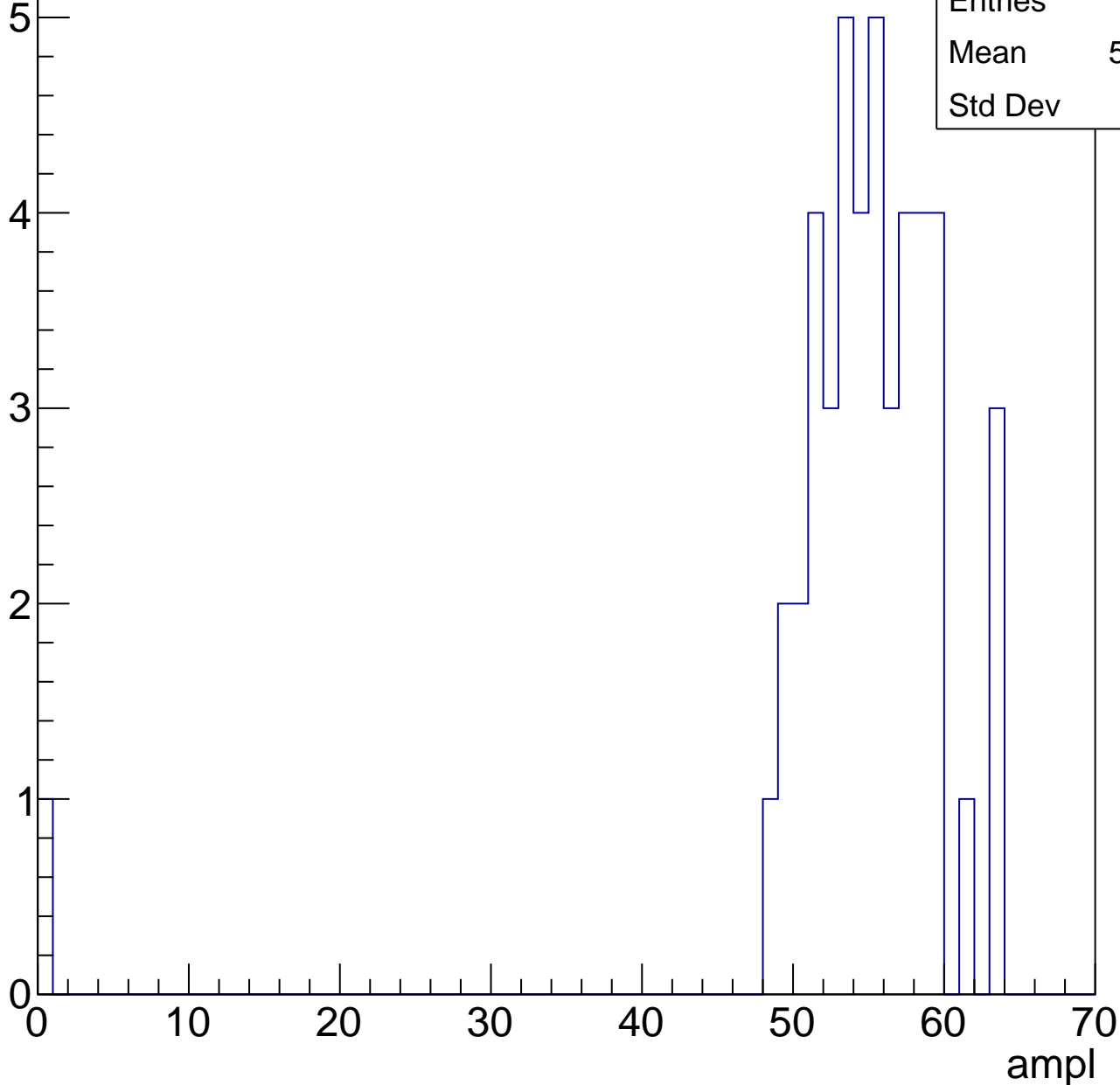


# B1L103S, U26-ch38, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

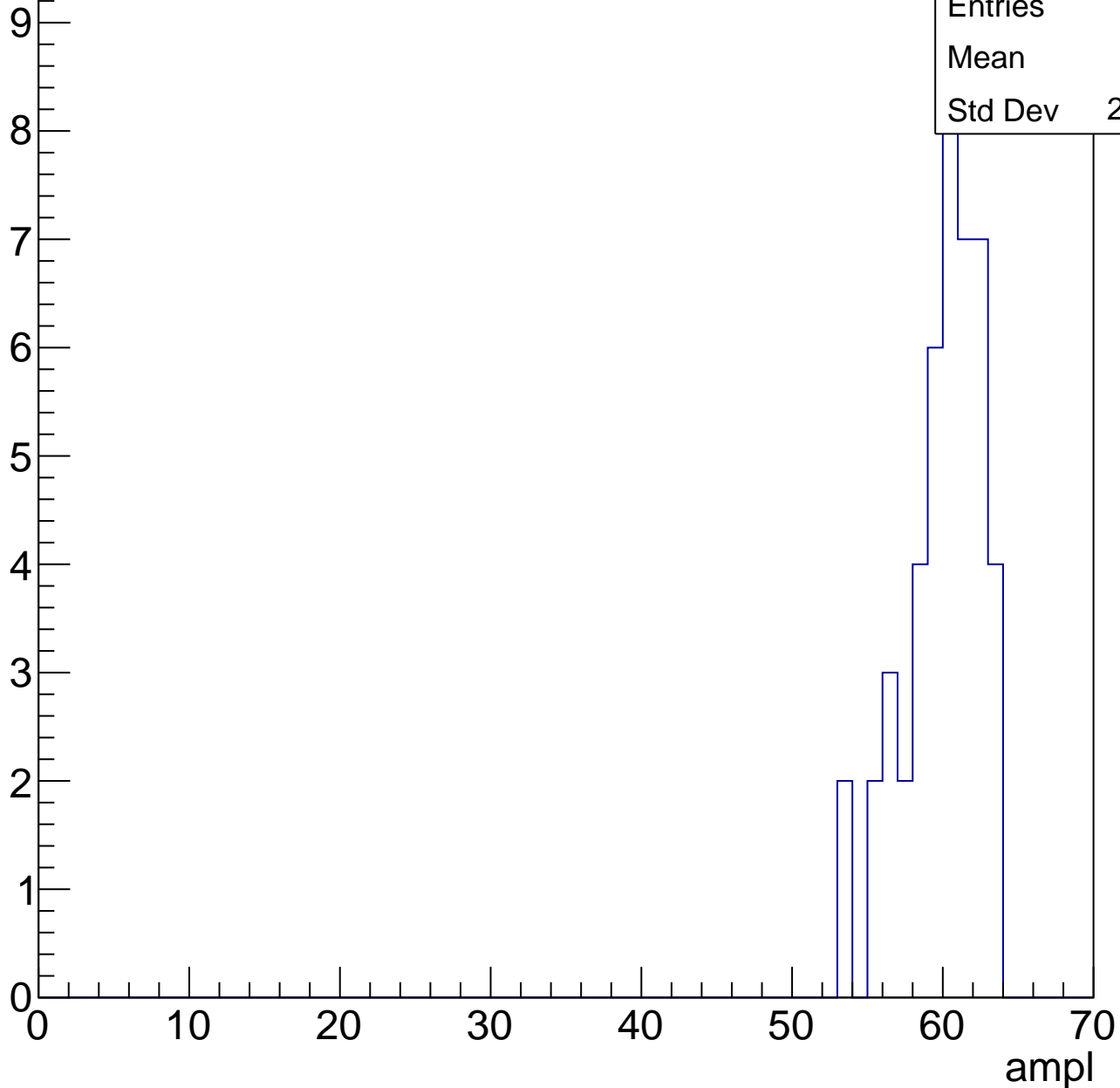
Entries	46
Mean	53.83
Std Dev	8.84



# B1L103S, U26-ch38, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

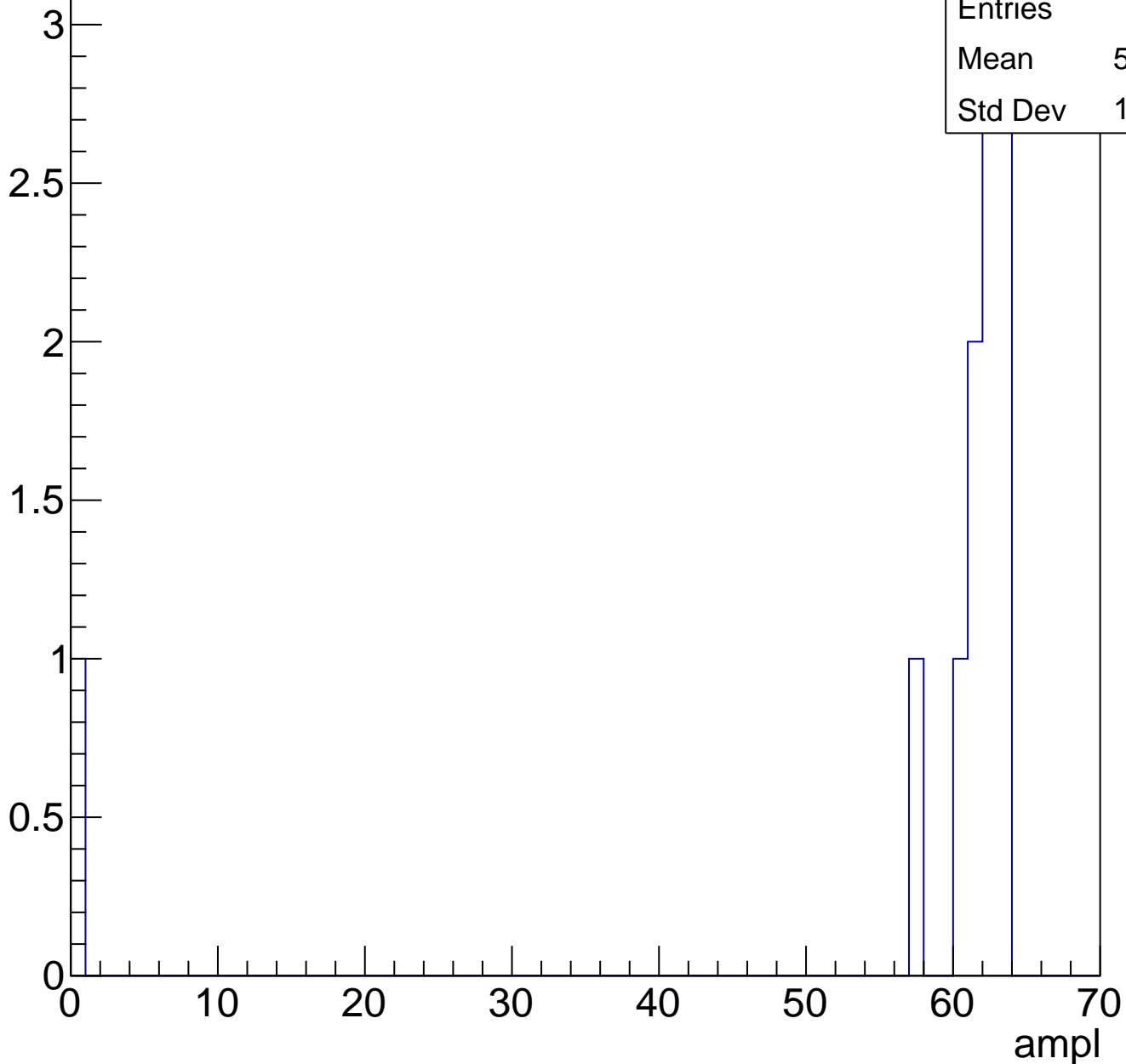
Entry



# B1L103S, U26-ch38, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry





# B1L103S, U26-ch38, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



# B1L103S, U26-ch39, adc0

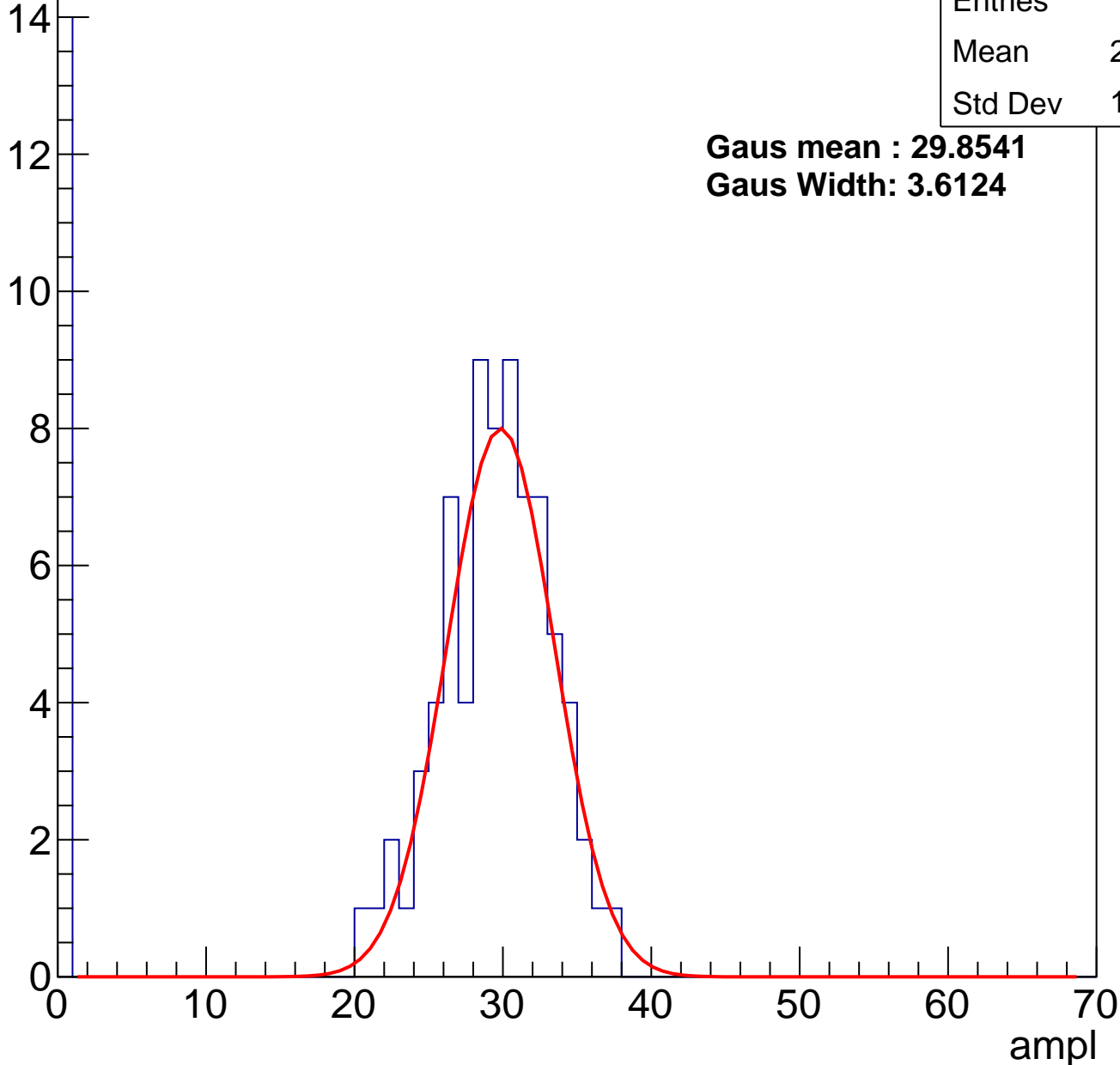
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	90
Mean	24.54
Std Dev	11.03

**Gaus mean : 29.8541**

**Gaus Width: 3.6124**

Entry



# B1L103S, U26-ch39, adc1

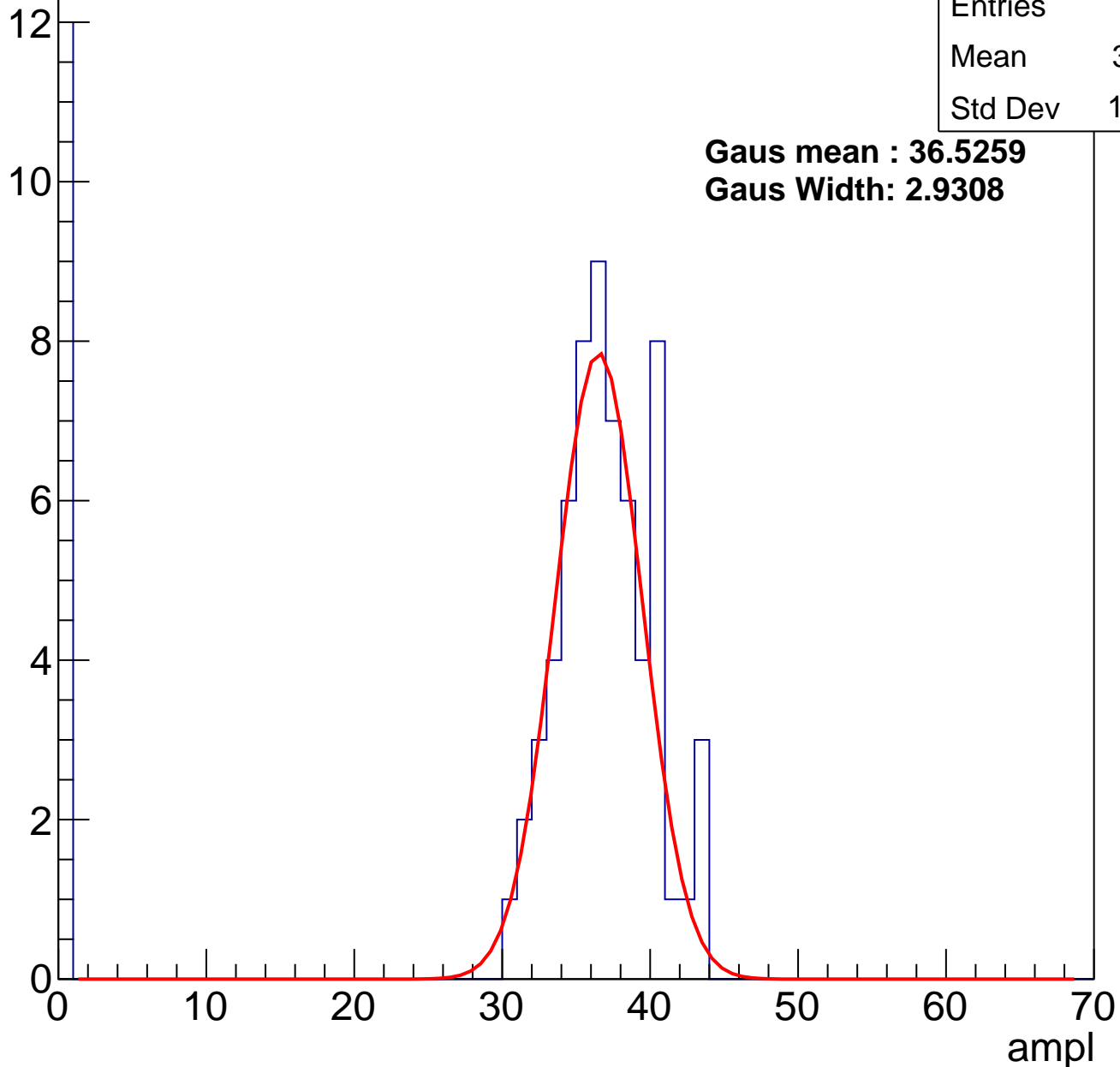
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	75
Mean	30.71
Std Dev	13.69

**Gaus mean : 36.5259**

**Gaus Width: 2.9308**

Entry



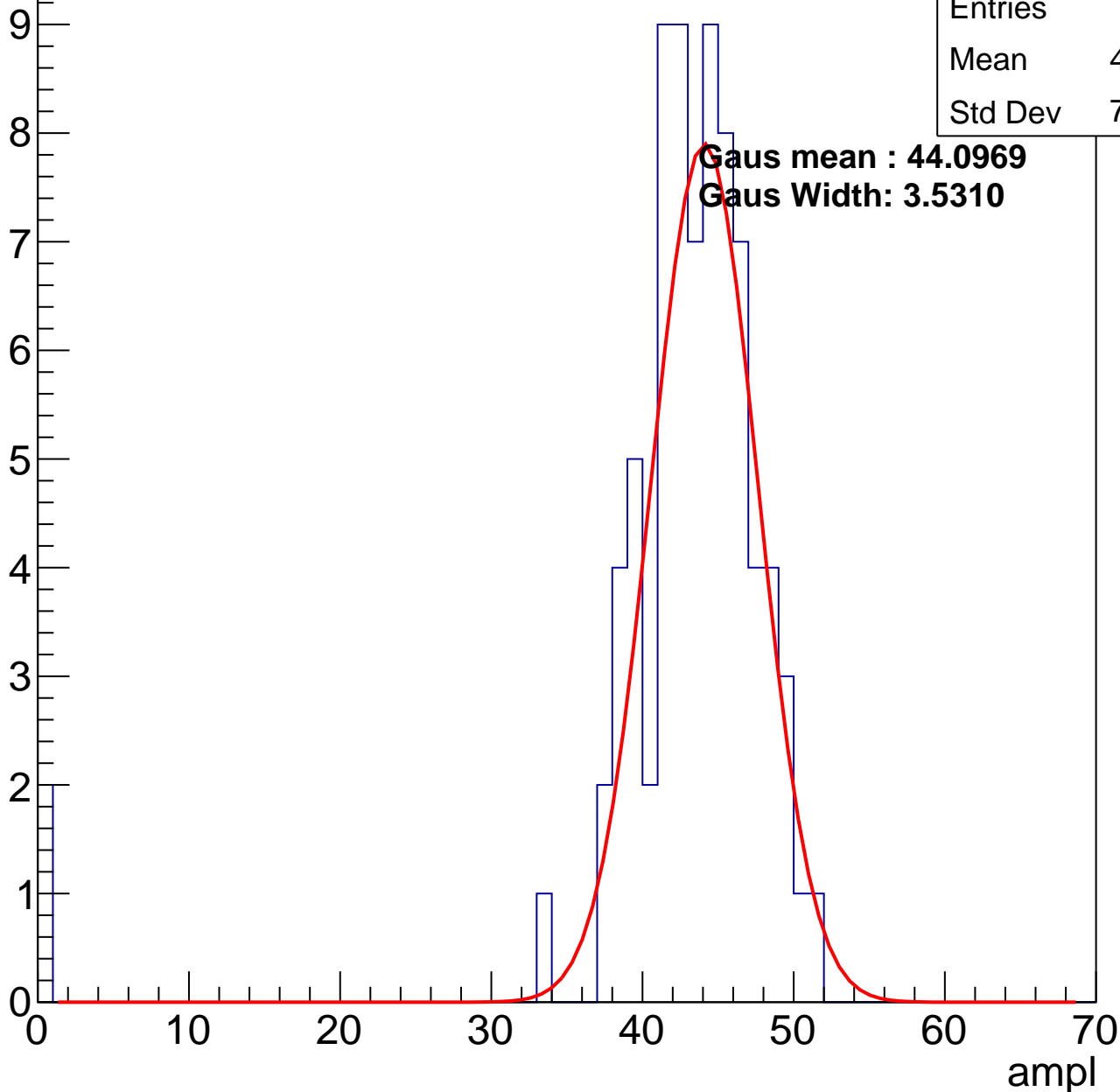
# B1L103S, U26-ch39, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	78
Mean	42.15
Std Dev	7.634

**Gaus mean : 44.0969**  
**Gaus Width: 3.5310**

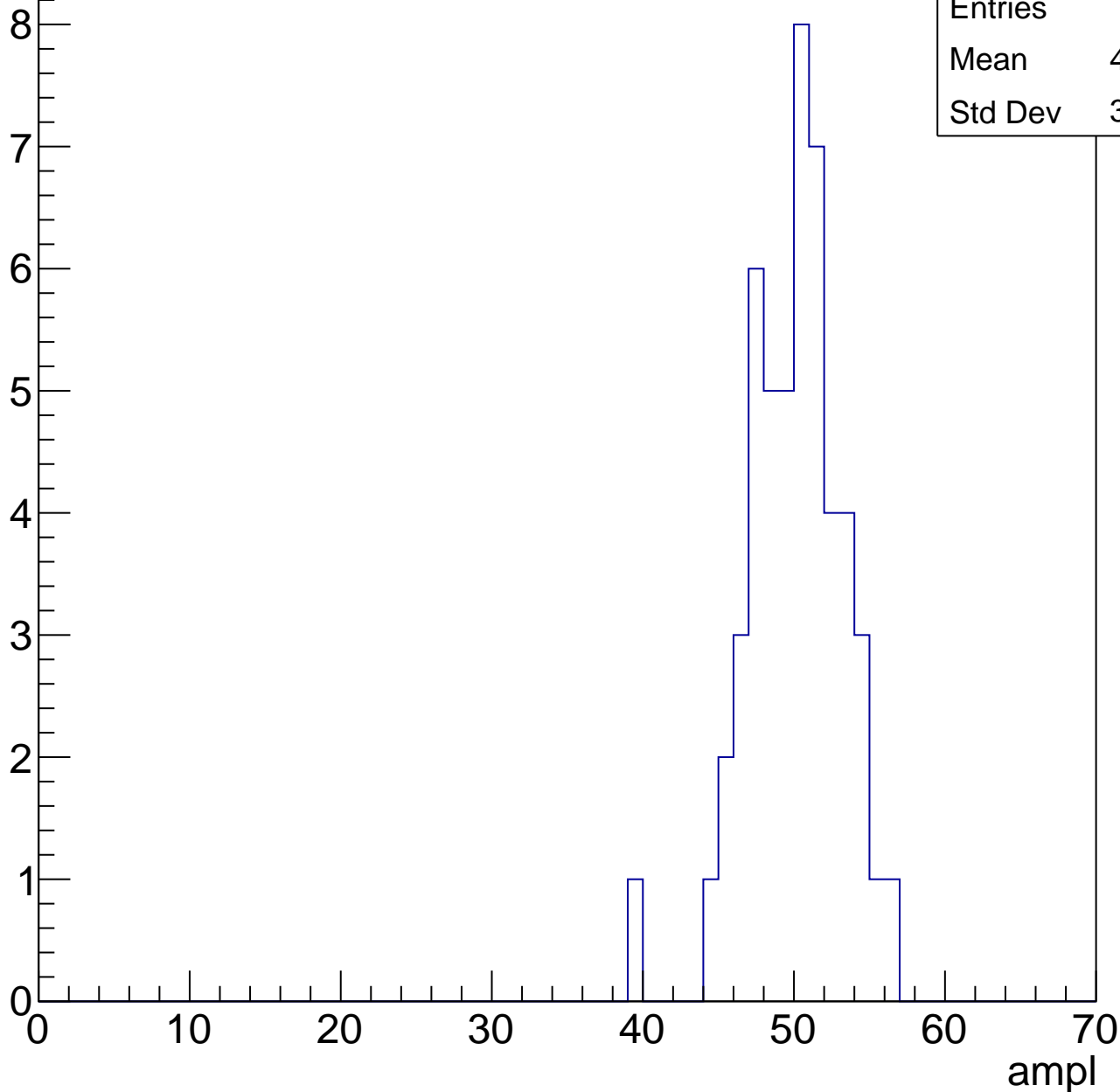


# B1L103S, U26-ch39, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

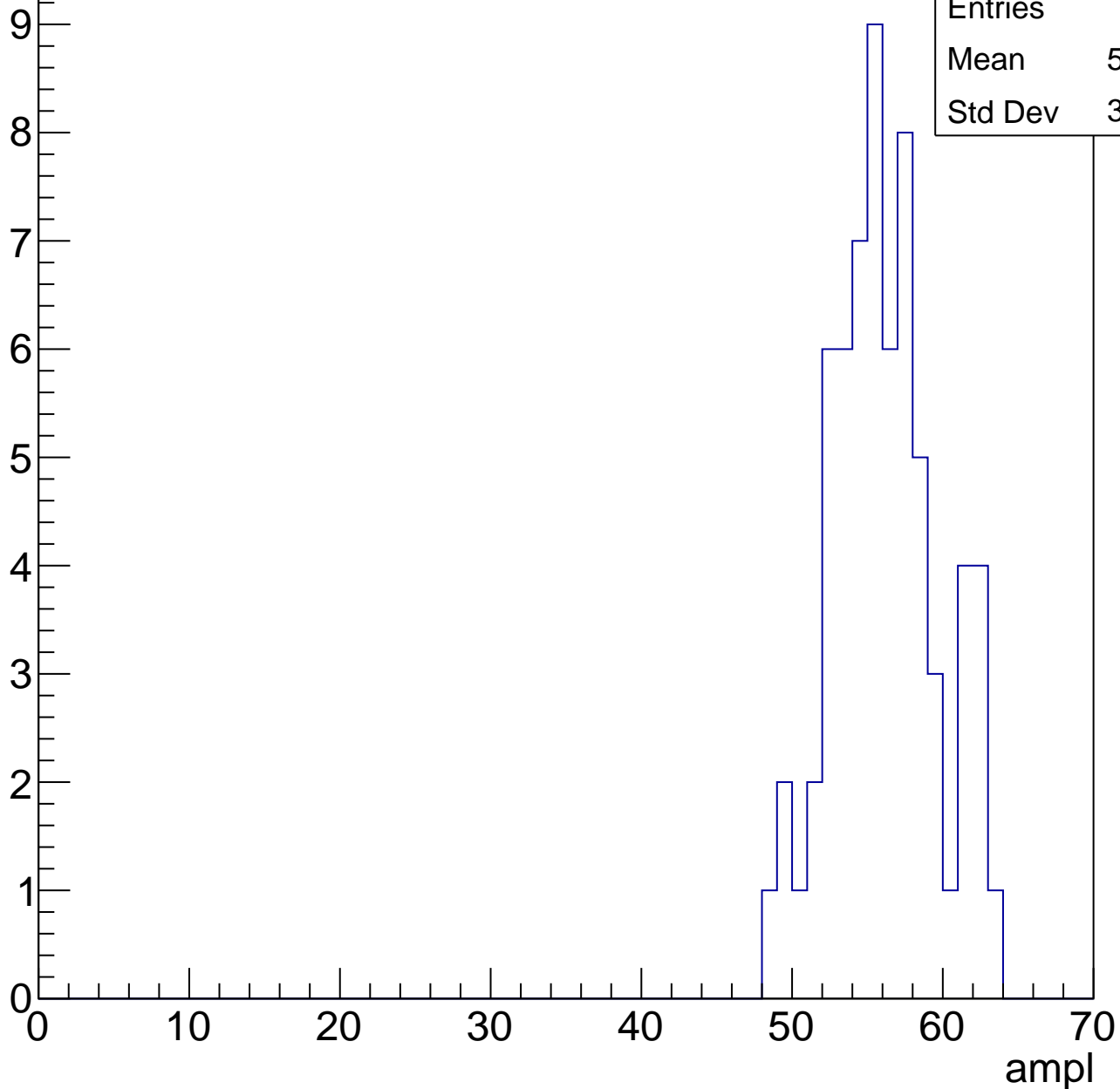
Entries	51
Mean	49.57
Std Dev	3.108



# B1L103S, U26-ch39, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

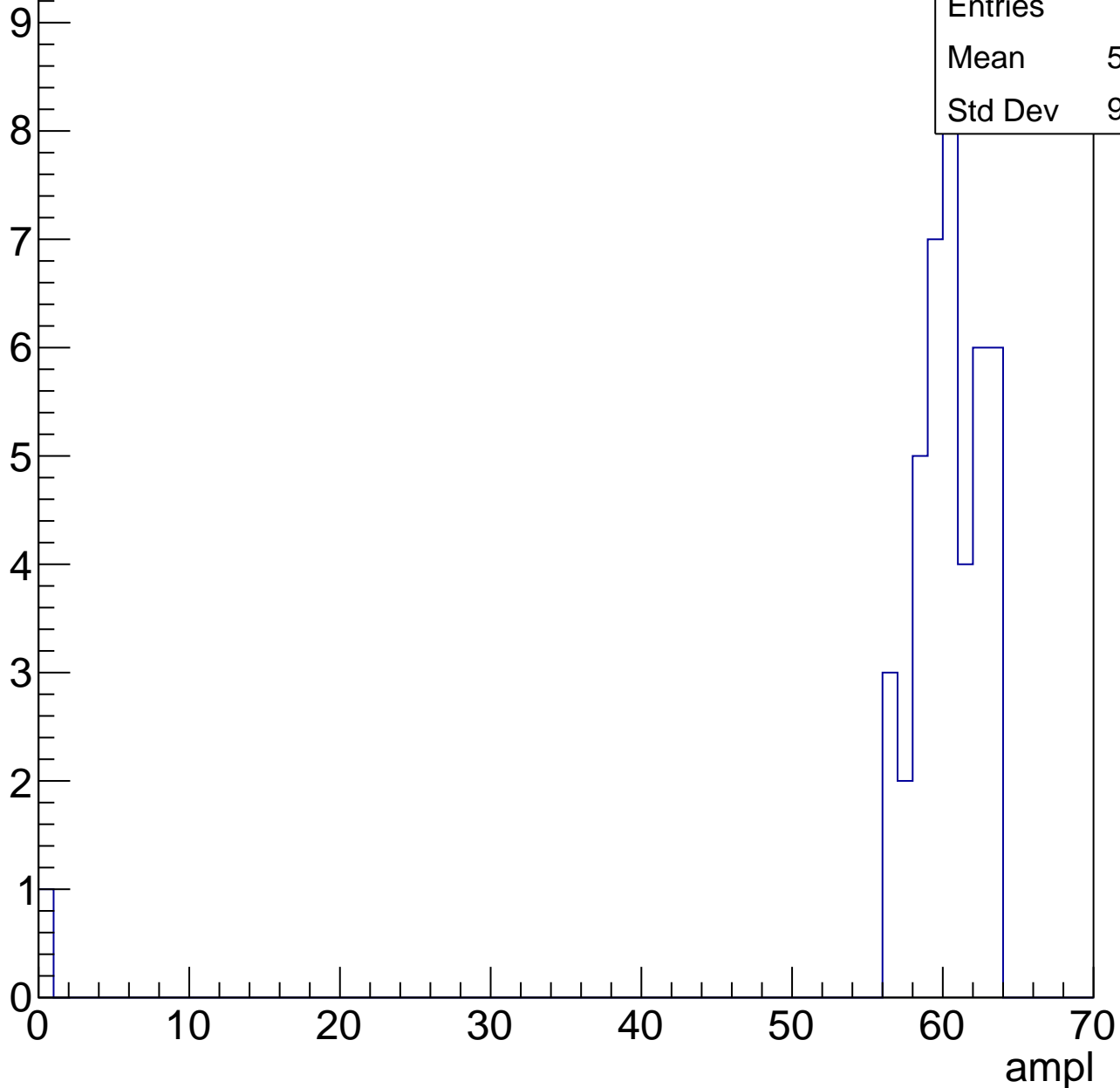


Entries	66
Mean	55.68
Std Dev	3.465

# B1L103S, U26-ch39, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

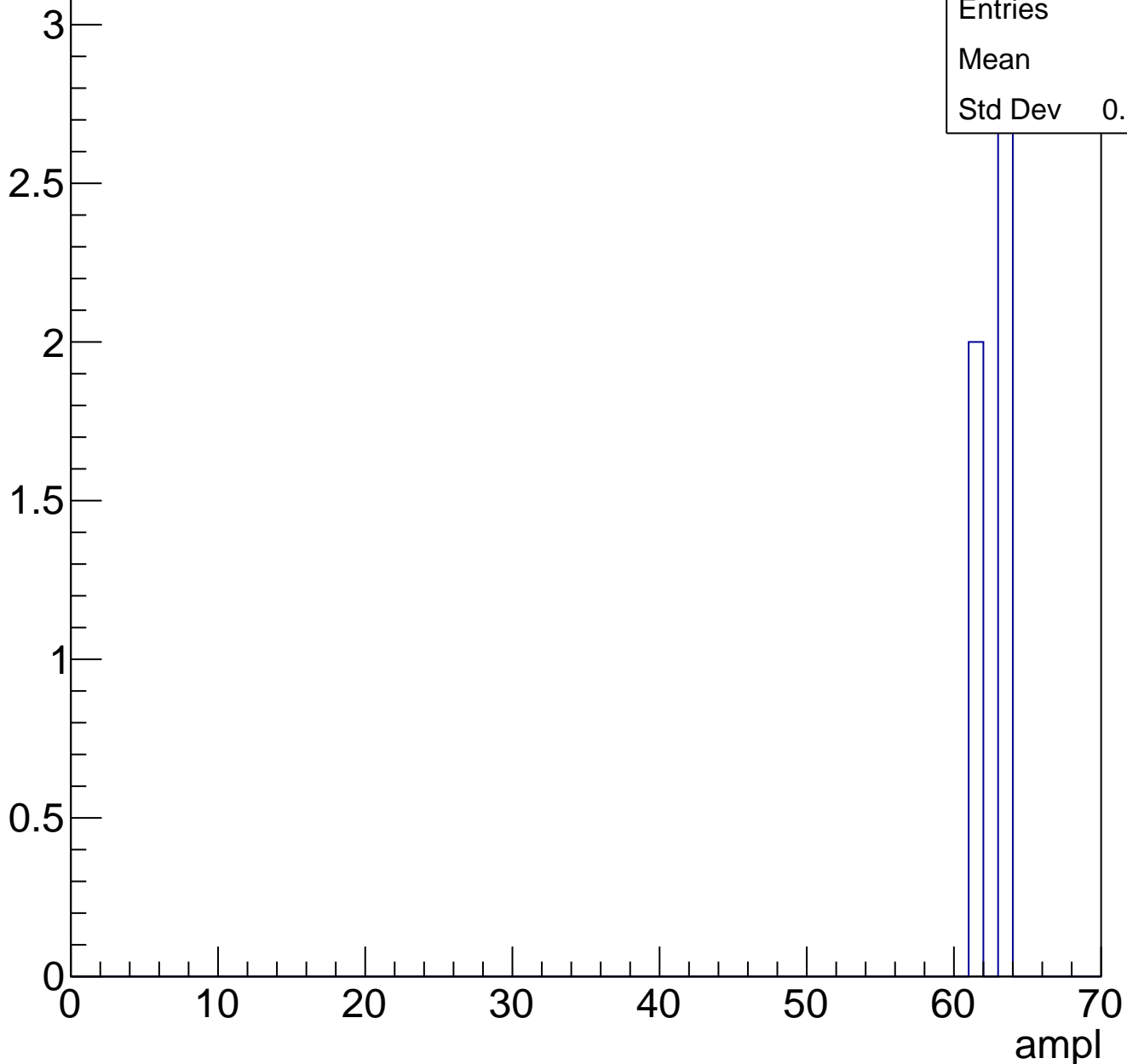
Entry



# B1L103S, U26-ch39, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry





# B1L103S, U26-ch39, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

18  
16  
14  
12  
10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

Entries	19
Mean	0
Std Dev	0

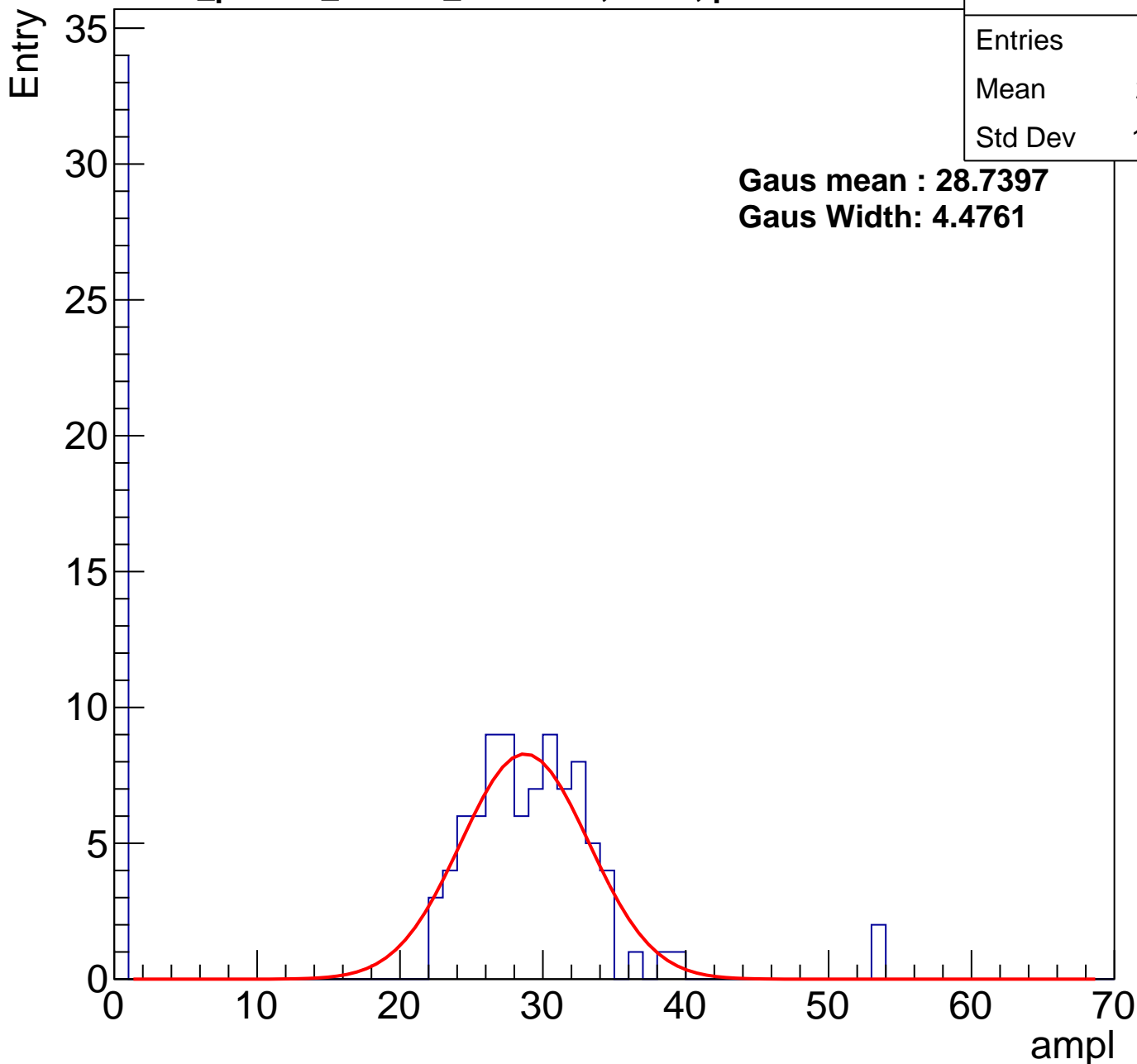
# B1L103S, U26-ch40, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	122
Mean	21.01
Std Dev	13.77

**Gaus mean : 28.7397**

**Gaus Width: 4.4761**



# B1L103S, U26-ch40, adc1

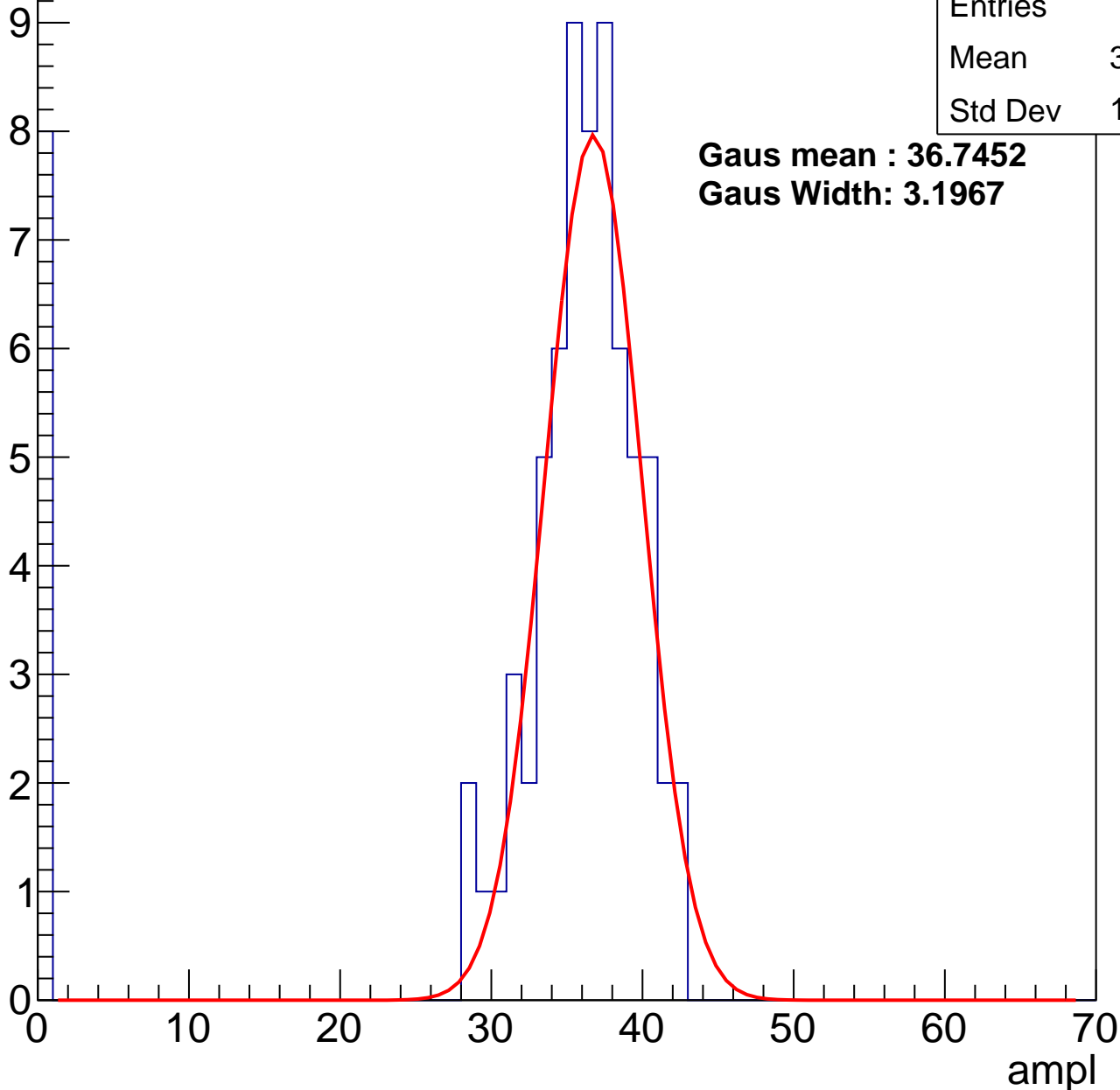
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	74
Mean	31.97
Std Dev	11.53

**Gaus mean : 36.7452**

**Gaus Width: 3.1967**



# B1L103S, U26-ch40, adc2

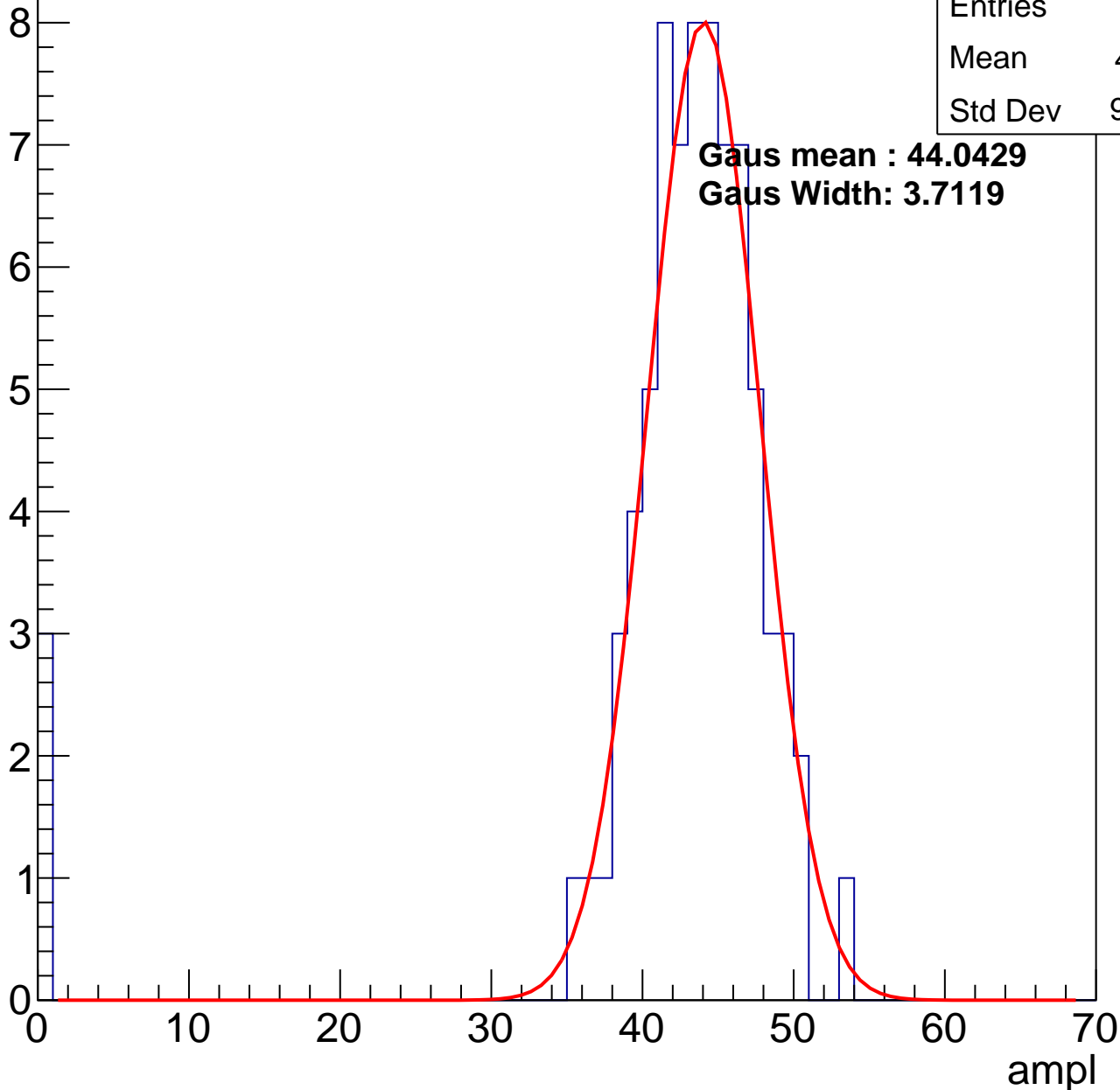
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	77
Mean	41.71
Std Dev	9.082

**Gaus mean : 44.0429**

**Gaus Width: 3.7119**

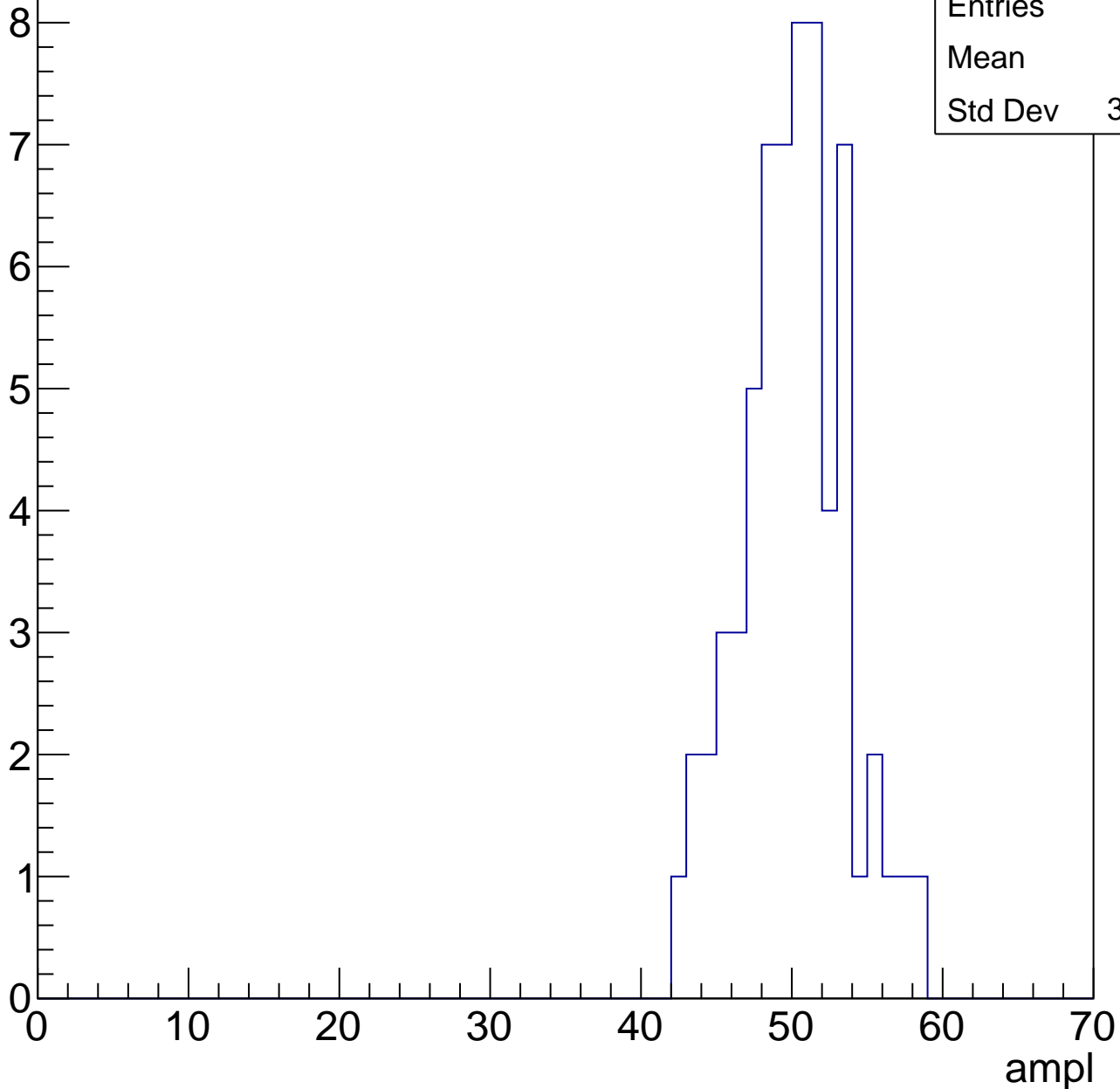


# B1L103S, U26-ch40, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	63
Mean	49.6
Std Dev	3.402

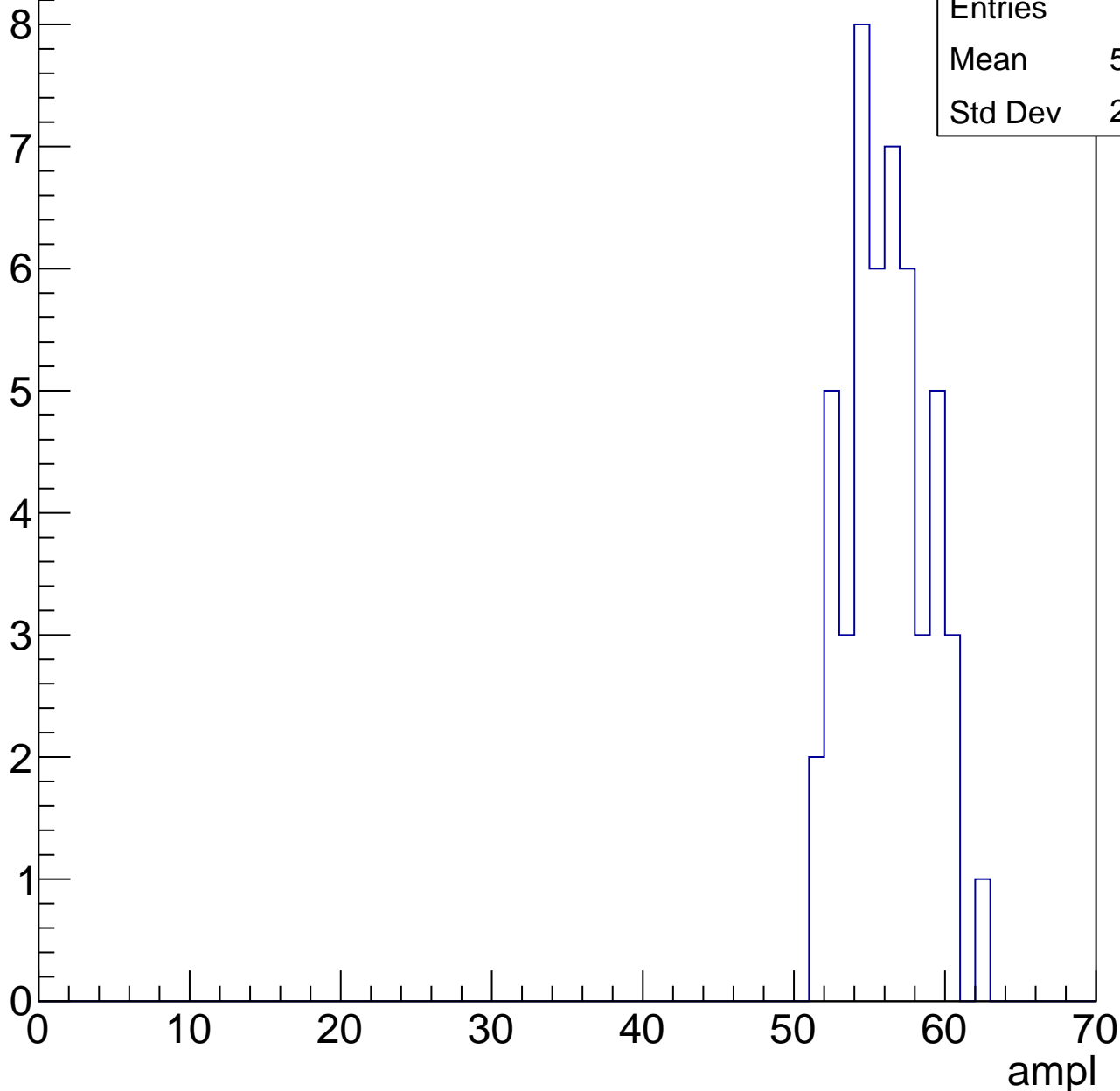


# B1L103S, U26-ch40, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	49
Mean	55.67
Std Dev	2.622

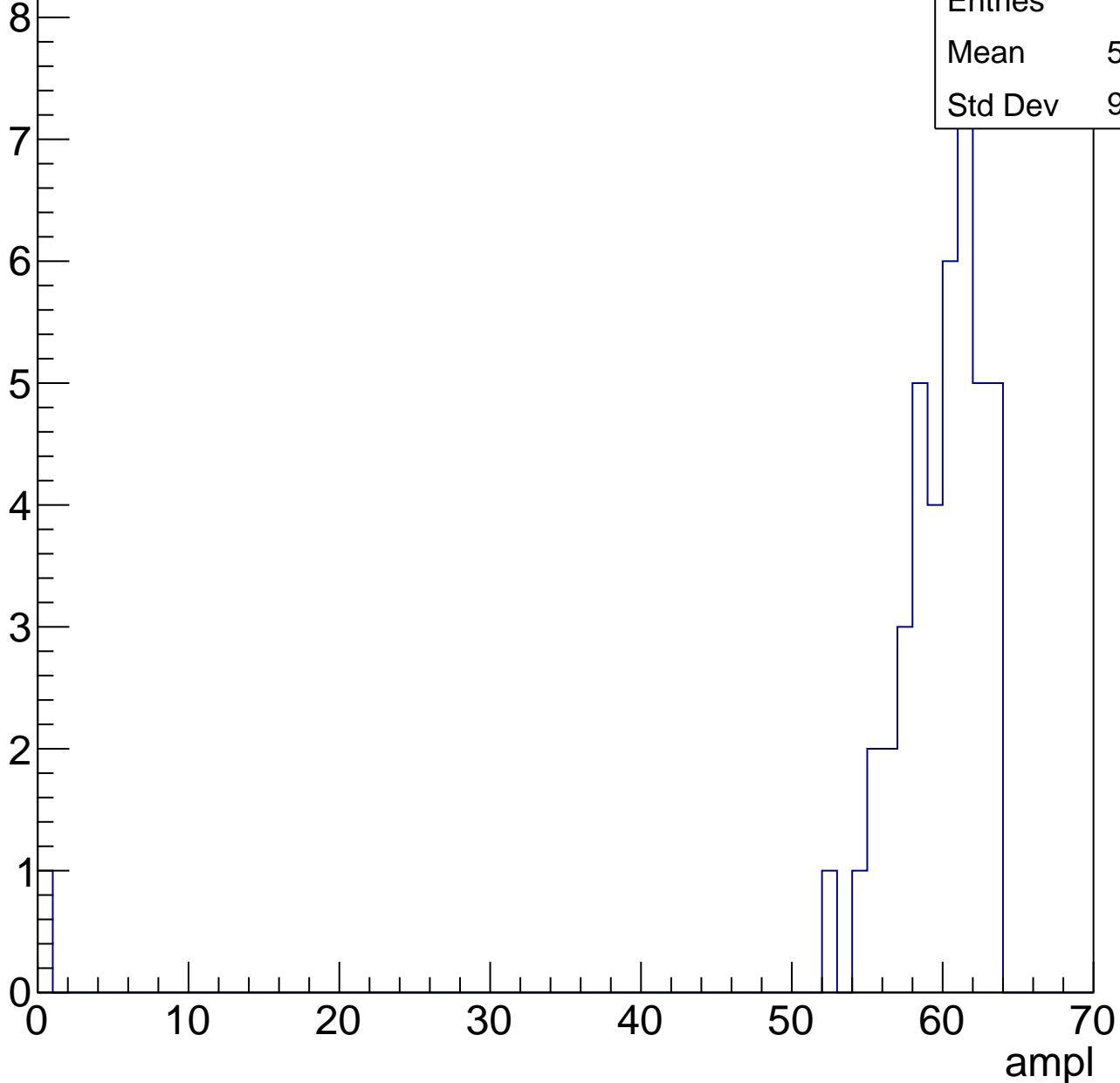


# B1L103S, U26-ch40, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	43
Mean	58.09
Std Dev	9.338

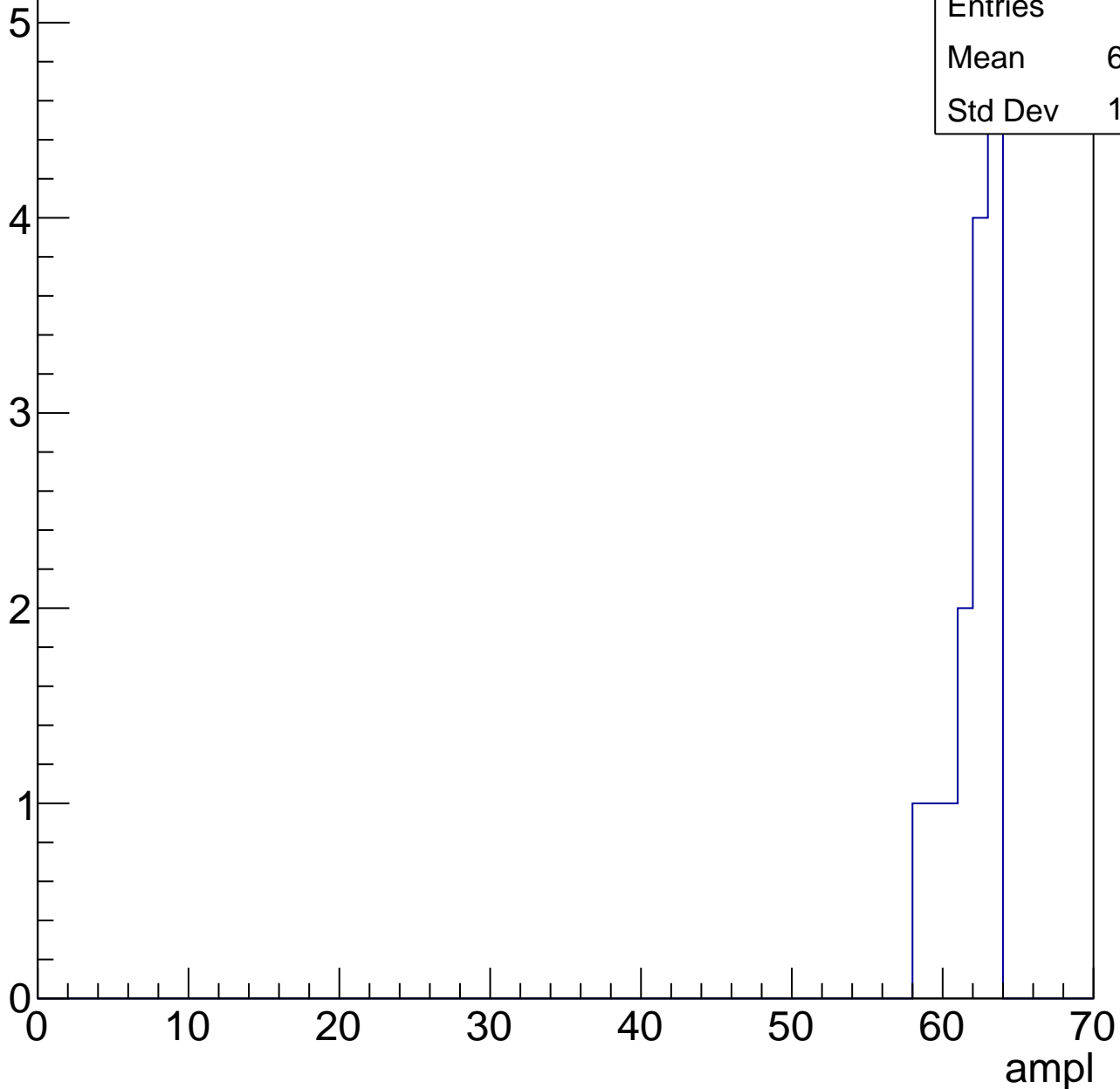


# B1L103S, U26-ch40, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	14
Mean	61.57
Std Dev	1.545





# B1L103S, U26-ch40, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



# B1L103S, U26-ch41, adc0

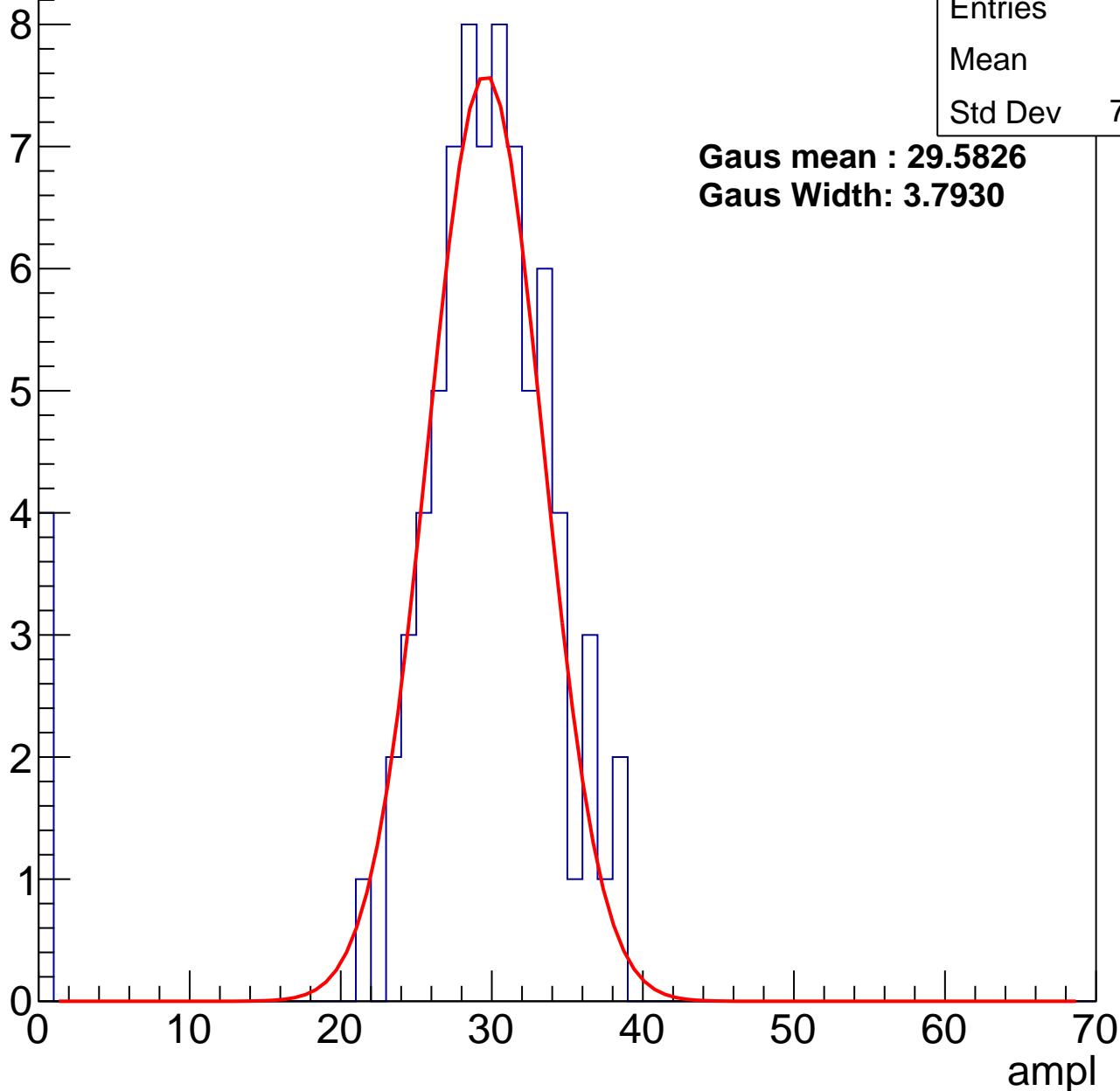
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	78
Mean	28.1
Std Dev	7.462

**Gaus mean : 29.5826**

**Gaus Width: 3.7930**



# B1L103S, U26-ch41, adc1

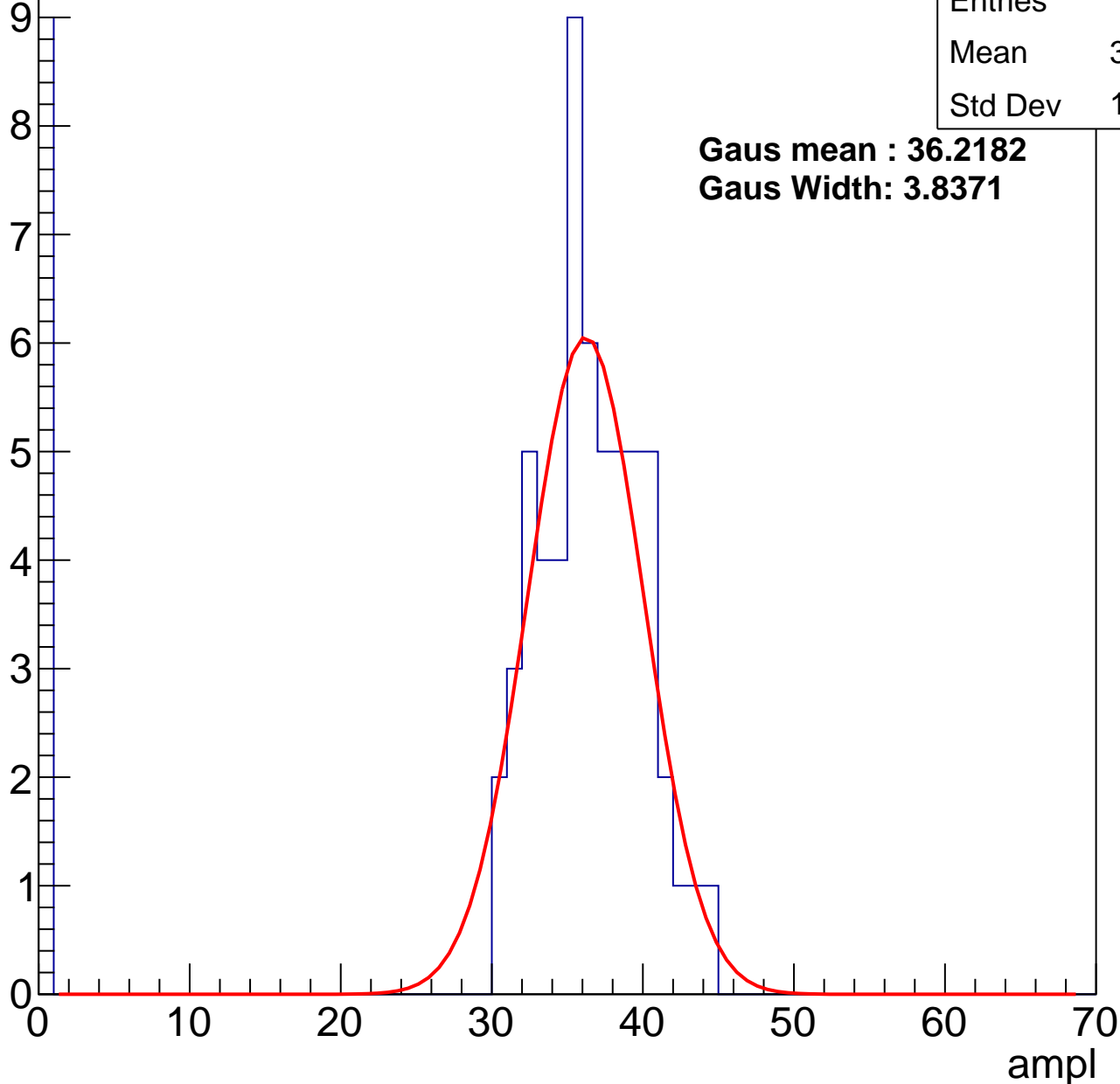
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	67
Mean	31.24
Std Dev	12.69

**Gaus mean : 36.2182**

**Gaus Width: 3.8371**



# B1L103S, U26-ch41, adc2

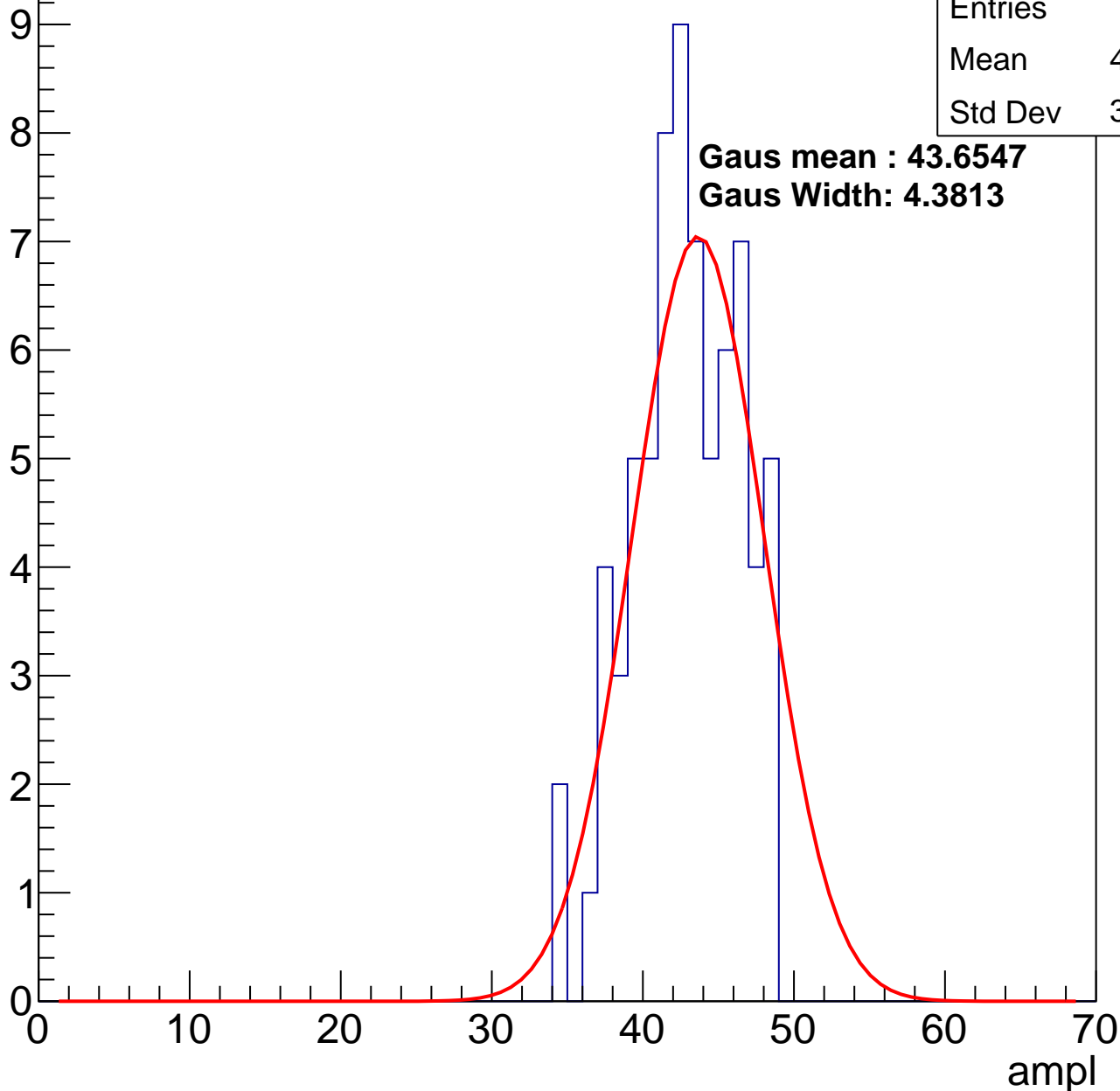
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	71
Mean	42.37
Std Dev	3.457

**Gaus mean : 43.6547**

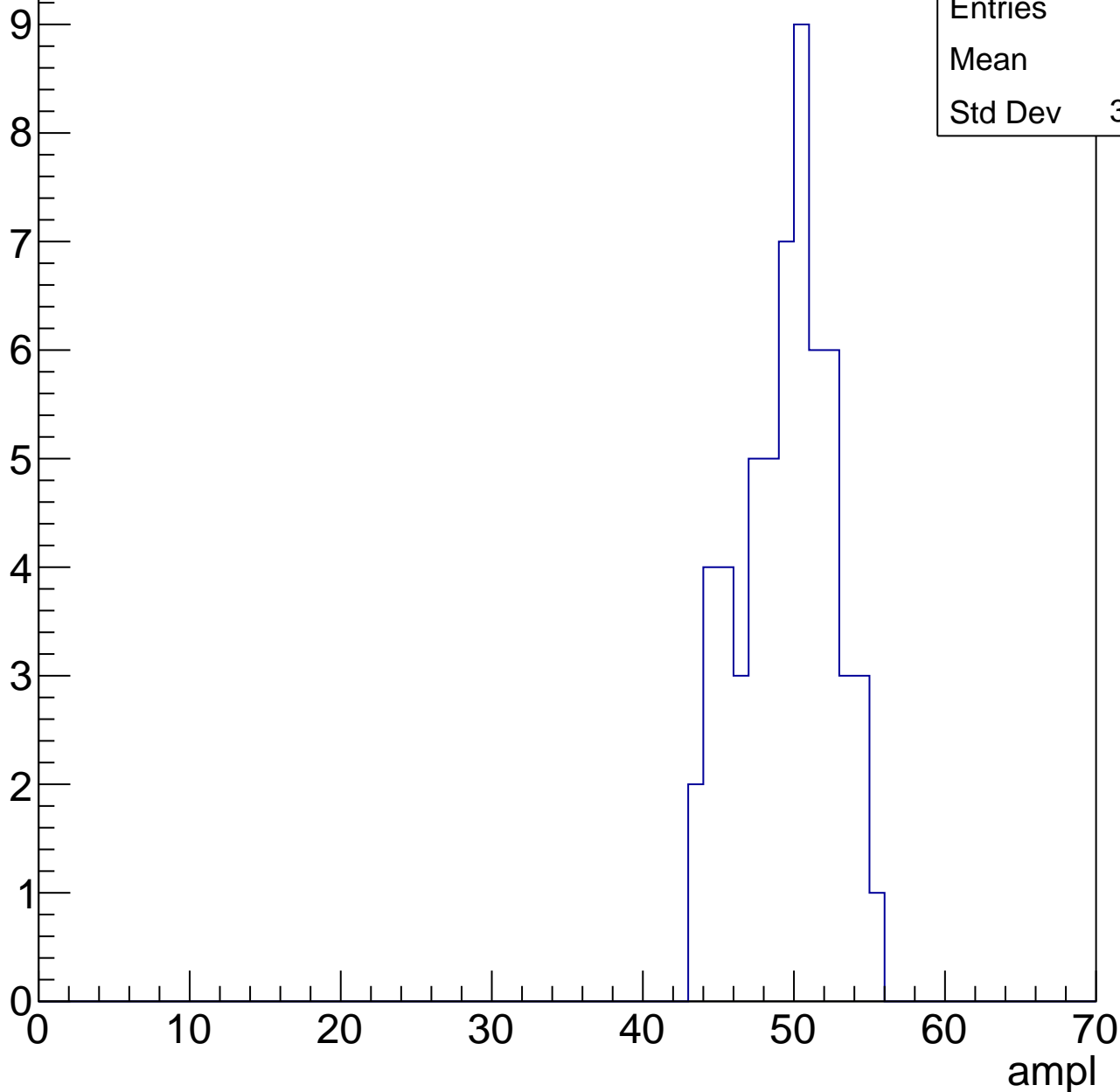
**Gaus Width: 4.3813**



# B1L103S, U26-ch41, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



# B1L103S, U26-ch41, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	65
Mean	55.18
Std Dev	3.205

Entry

10

8

6

4

2

0

0

10

20

30

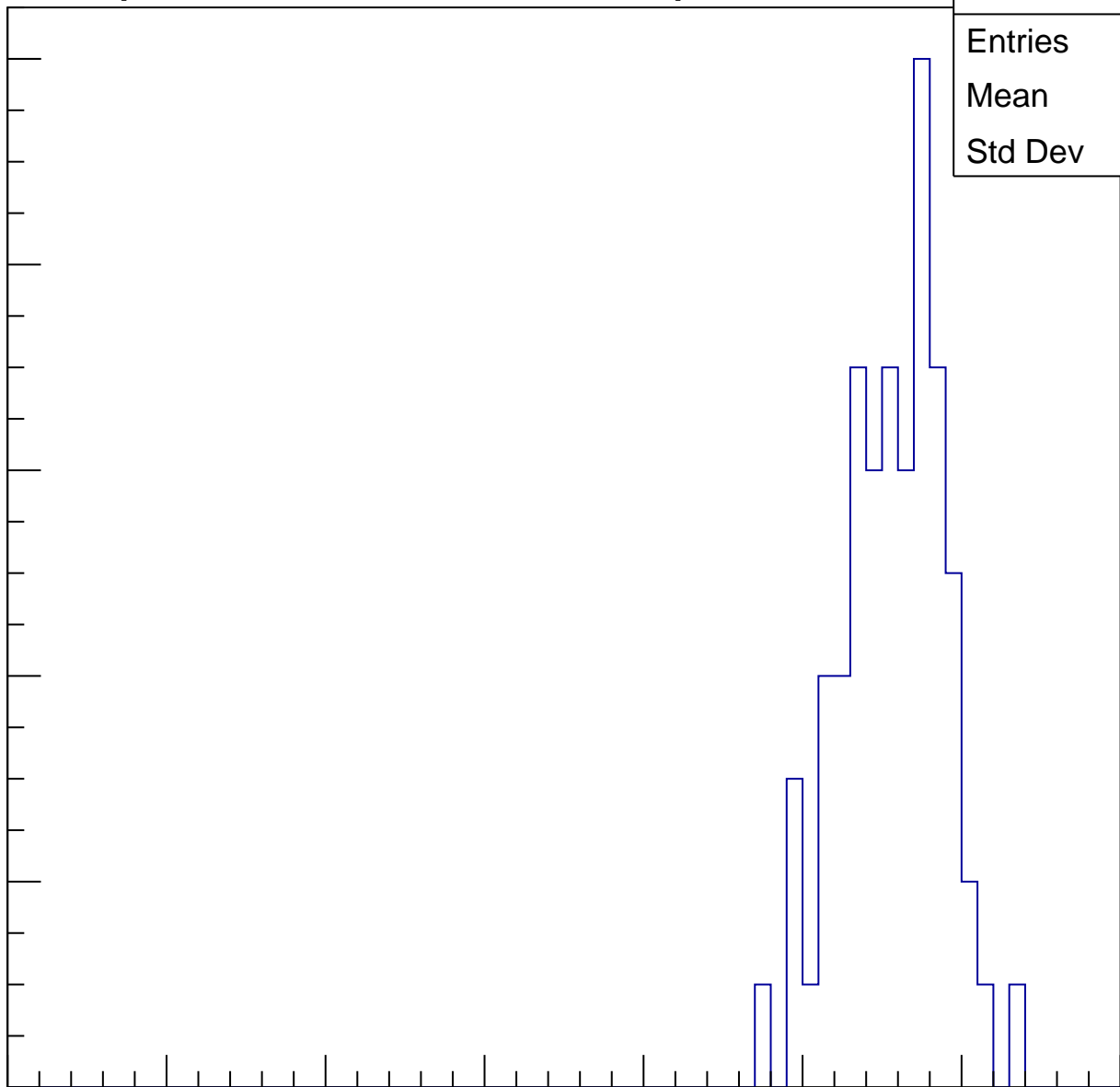
40

50

60

70

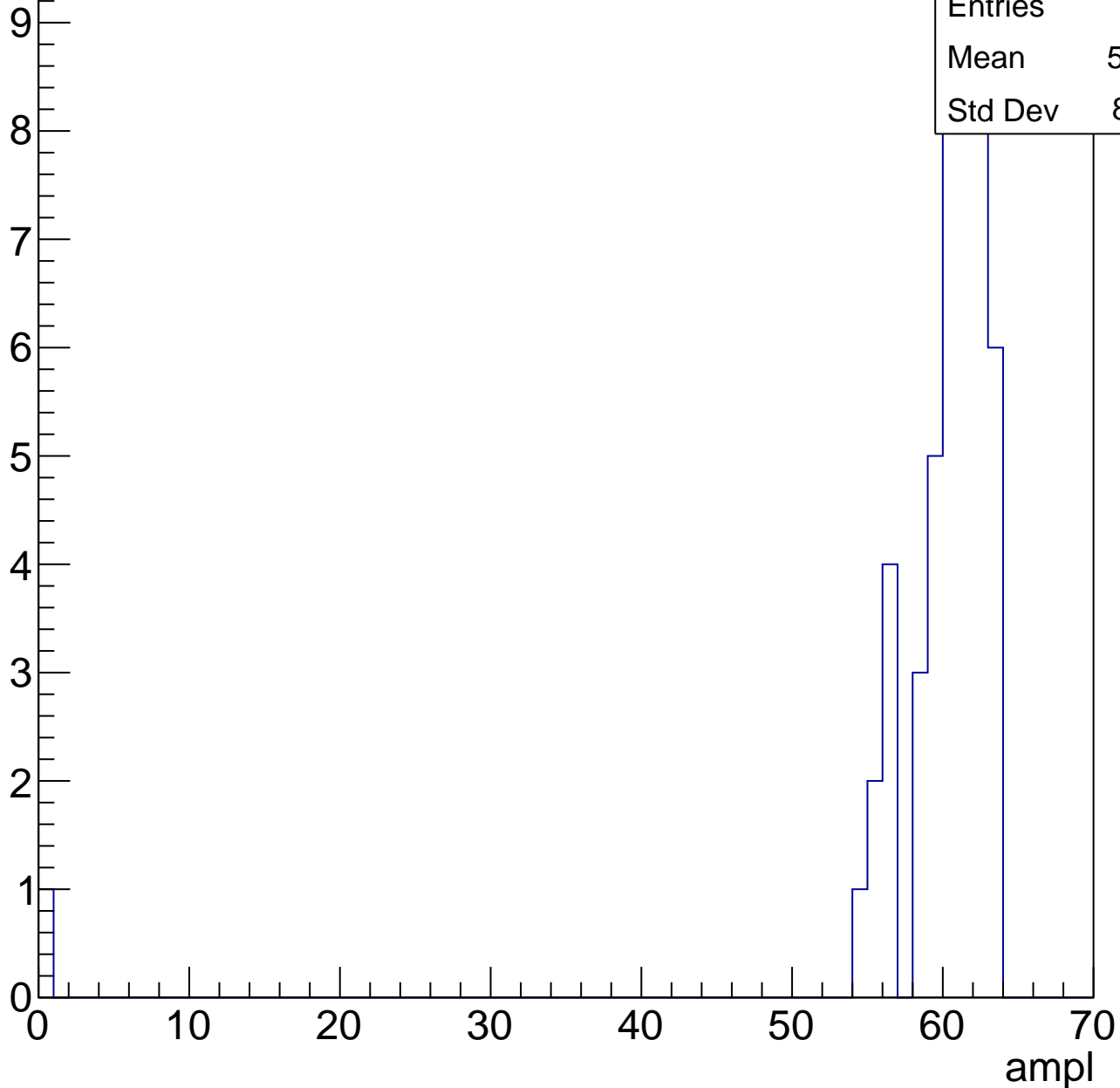
ampl



# B1L103S, U26-ch41, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



# B1L103S, U26-ch41, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry





# B1L103S, U26-ch41, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



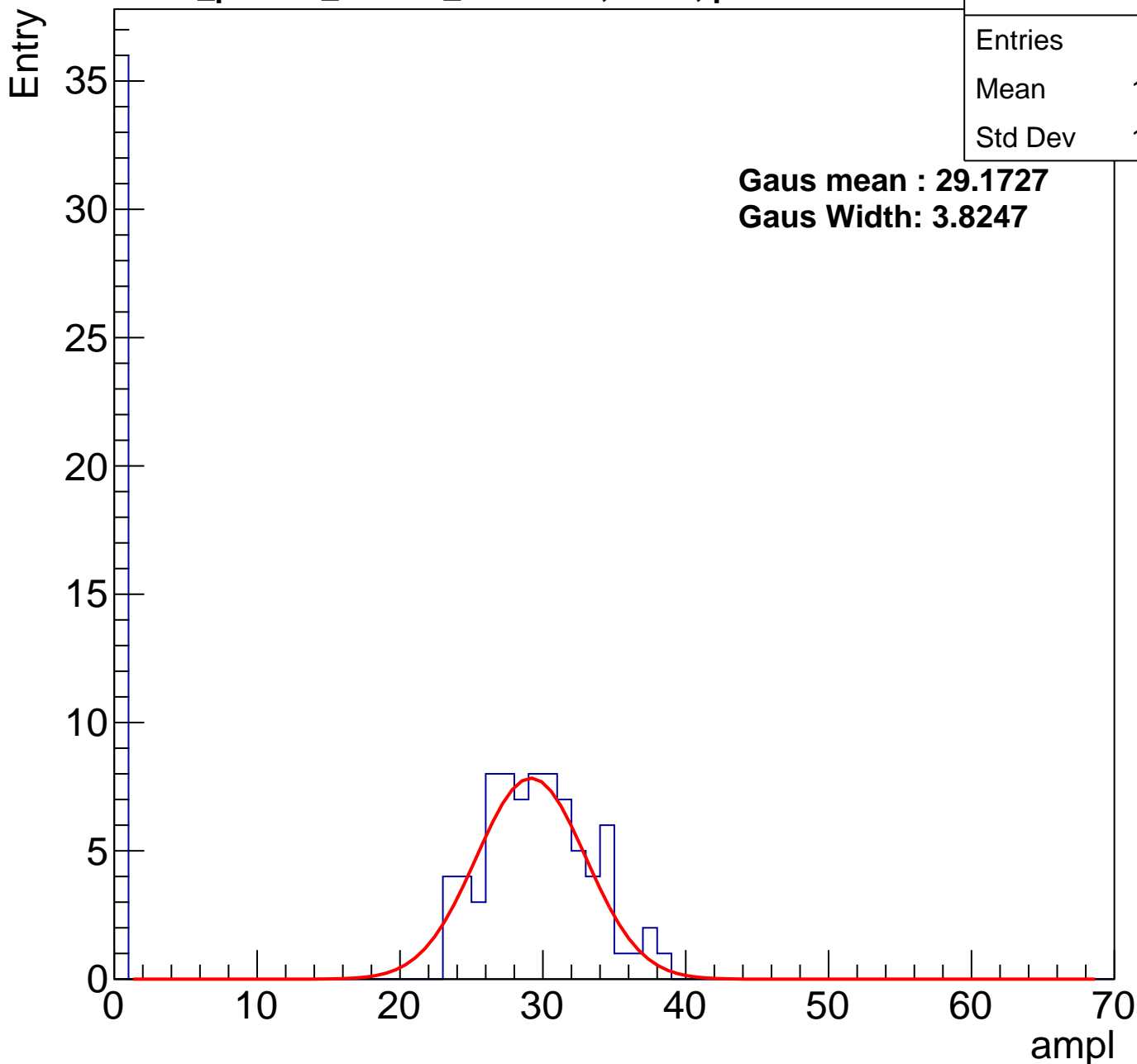
# B1L103S, U26-ch42, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	113
Mean	19.92
Std Dev	13.94

**Gaus mean : 29.1727**

**Gaus Width: 3.8247**



# B1L103S, U26-ch42, adc1

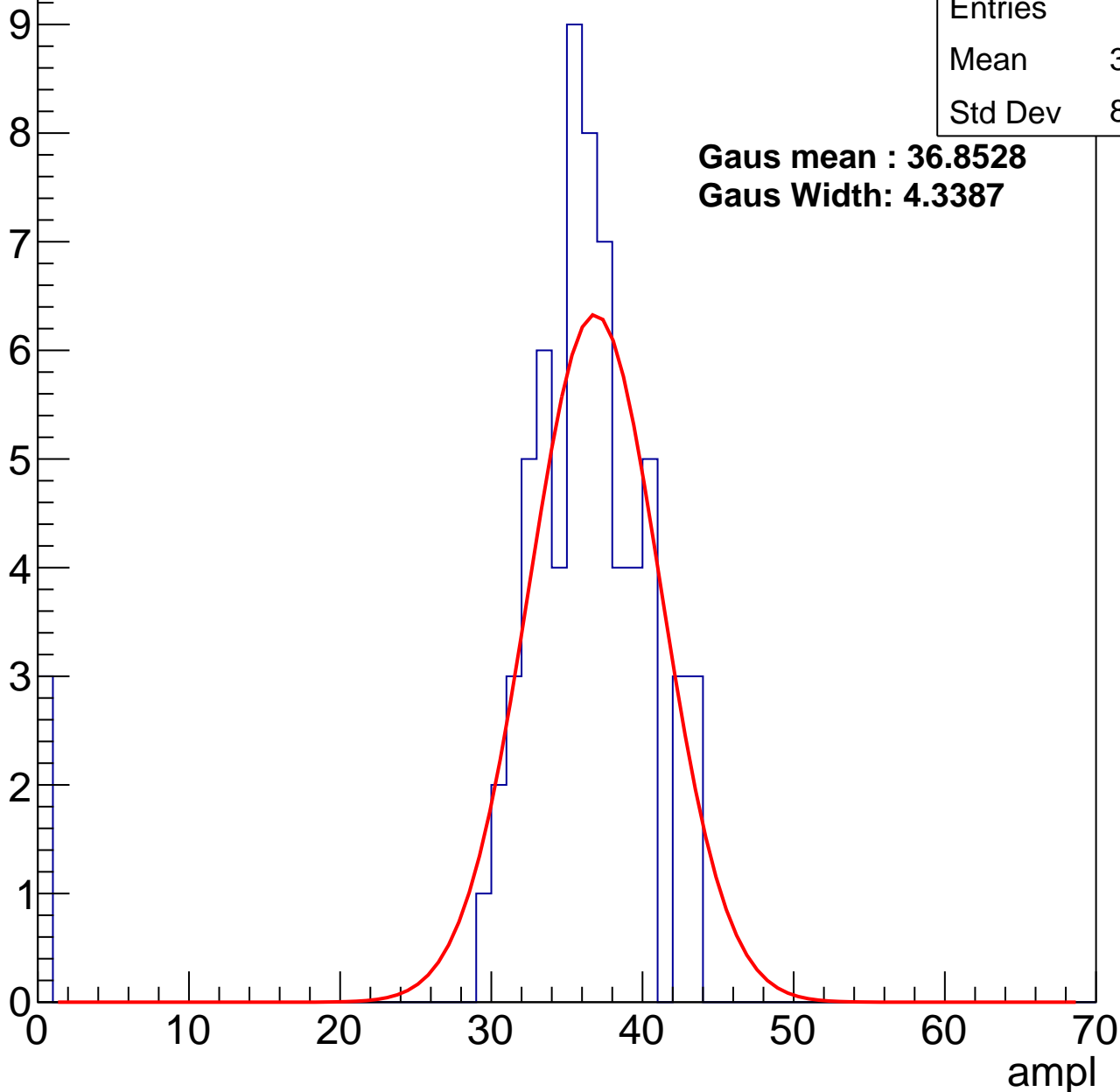
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	67
Mean	34.34
Std Dev	8.153

**Gaus mean : 36.8528**

**Gaus Width: 4.3387**



# B1L103S, U26-ch42, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	71
Mean	40.89
Std Dev	9.177

**Gaus mean : 43.2300**

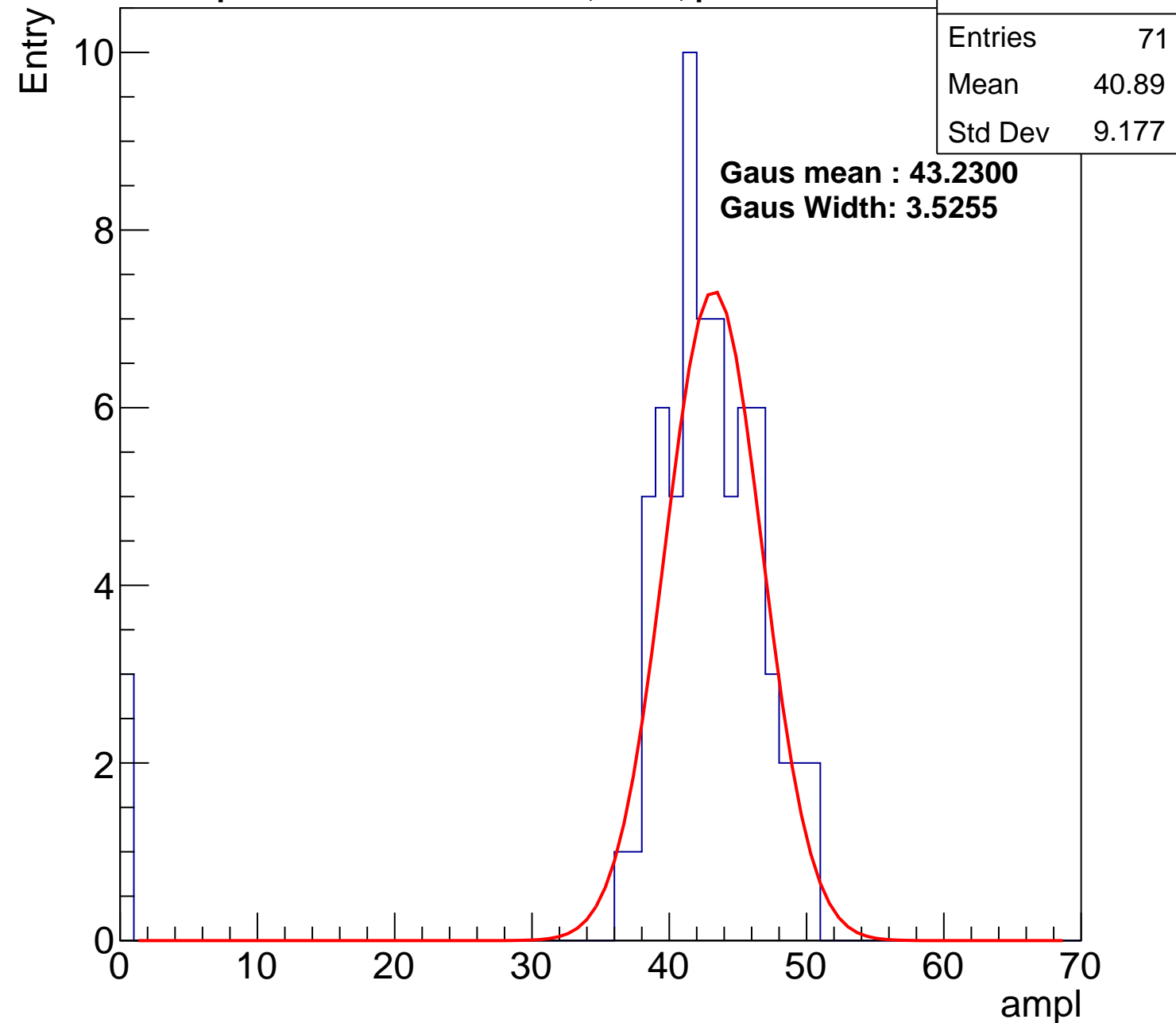
**Gaus Width: 3.5255**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

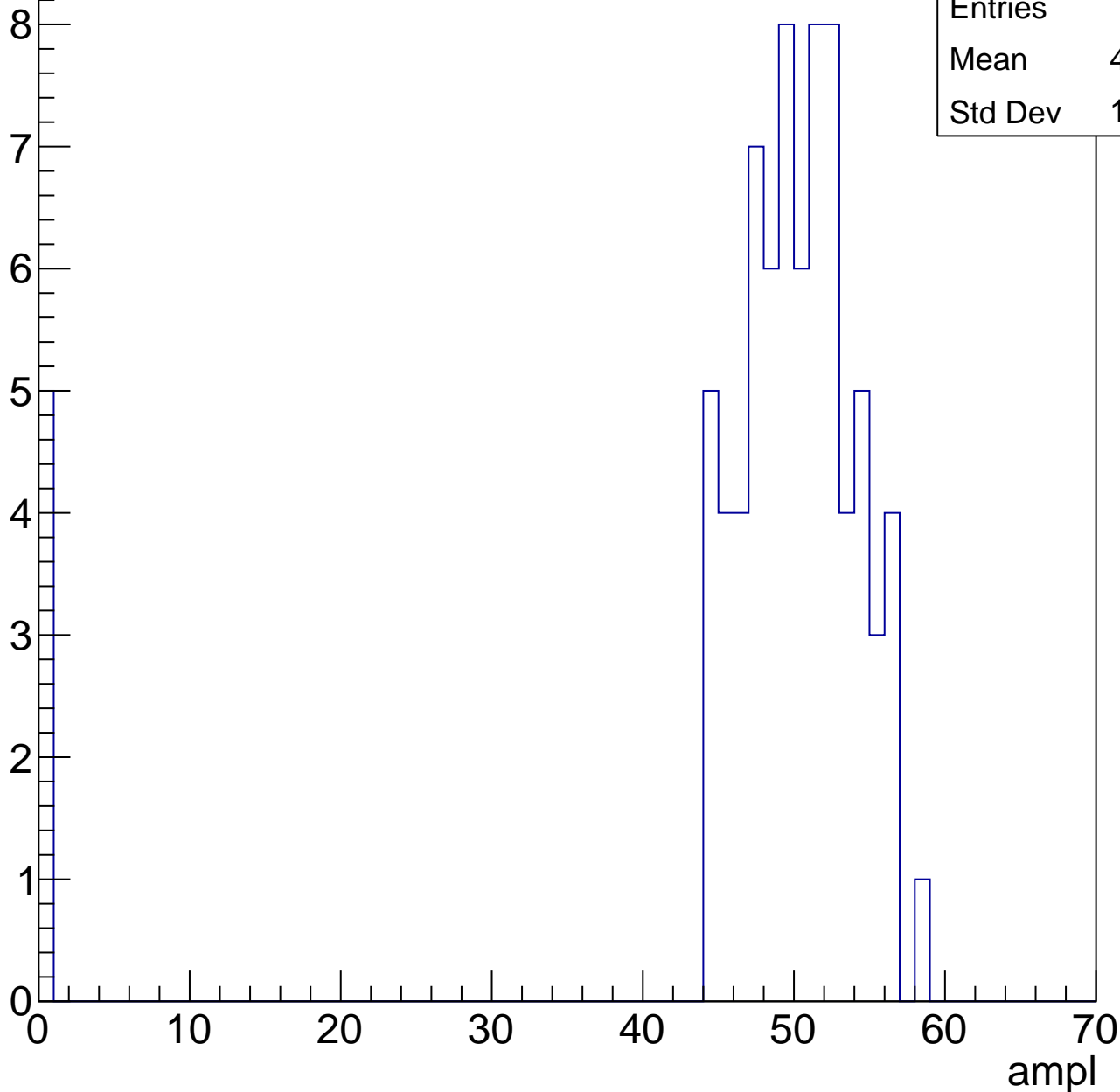


# B1L103S, U26-ch42, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	78
Mean	46.74
Std Dev	12.68

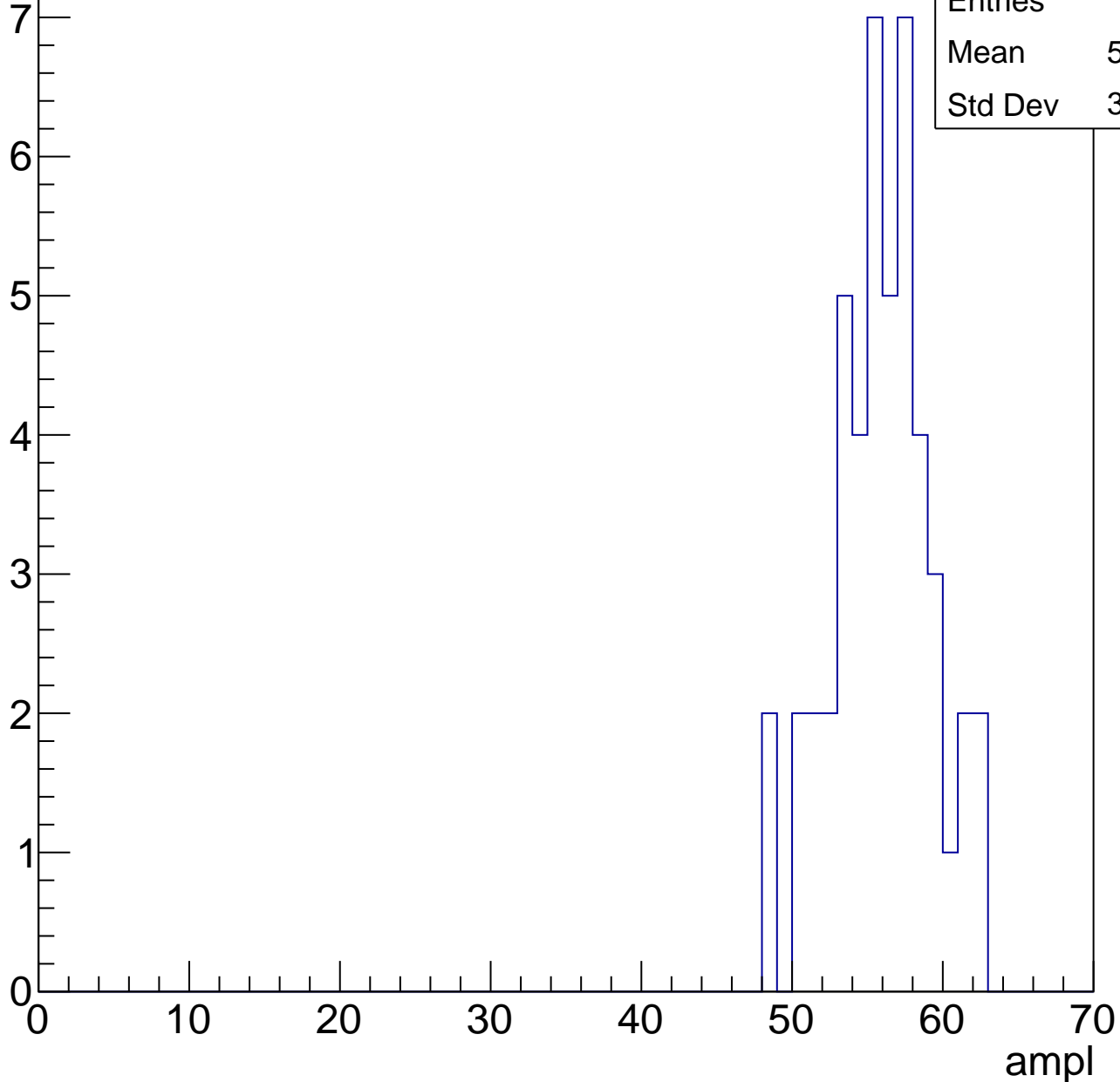


# B1L103S, U26-ch42, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	48
Mean	55.46
Std Dev	3.304

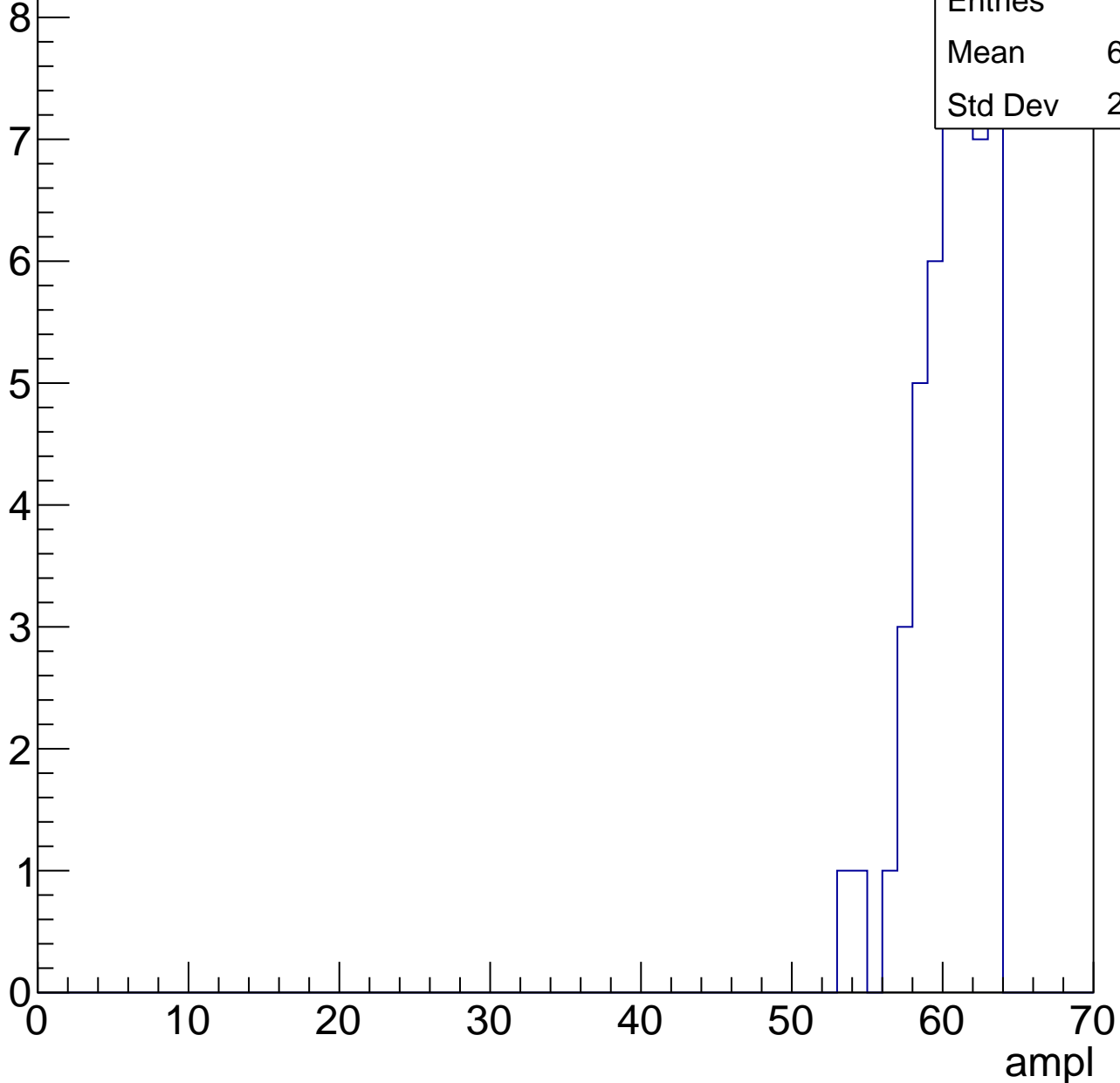


# B1L103S, U26-ch42, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	48
Mean	60.08
Std Dev	2.335



# B1L103S, U26-ch42, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

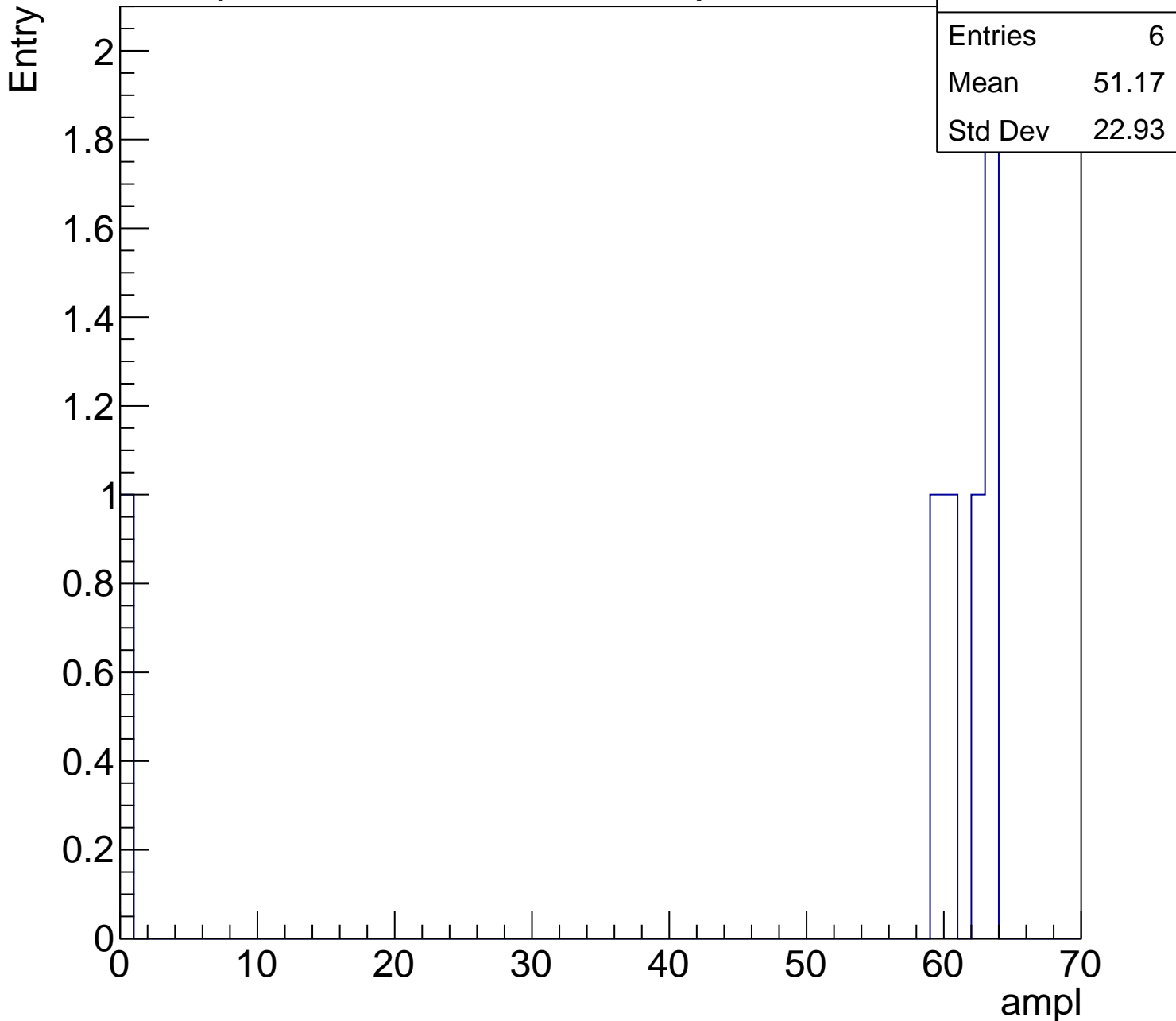
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	6
Mean	51.17
Std Dev	22.93

0 10 20 30 40 50 60 70

ampl





# B1L103S, U26-ch42, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

18  
16  
14  
12  
10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

Entries	19
Mean	0
Std Dev	0

# B1L103S, U26-ch43, adc0

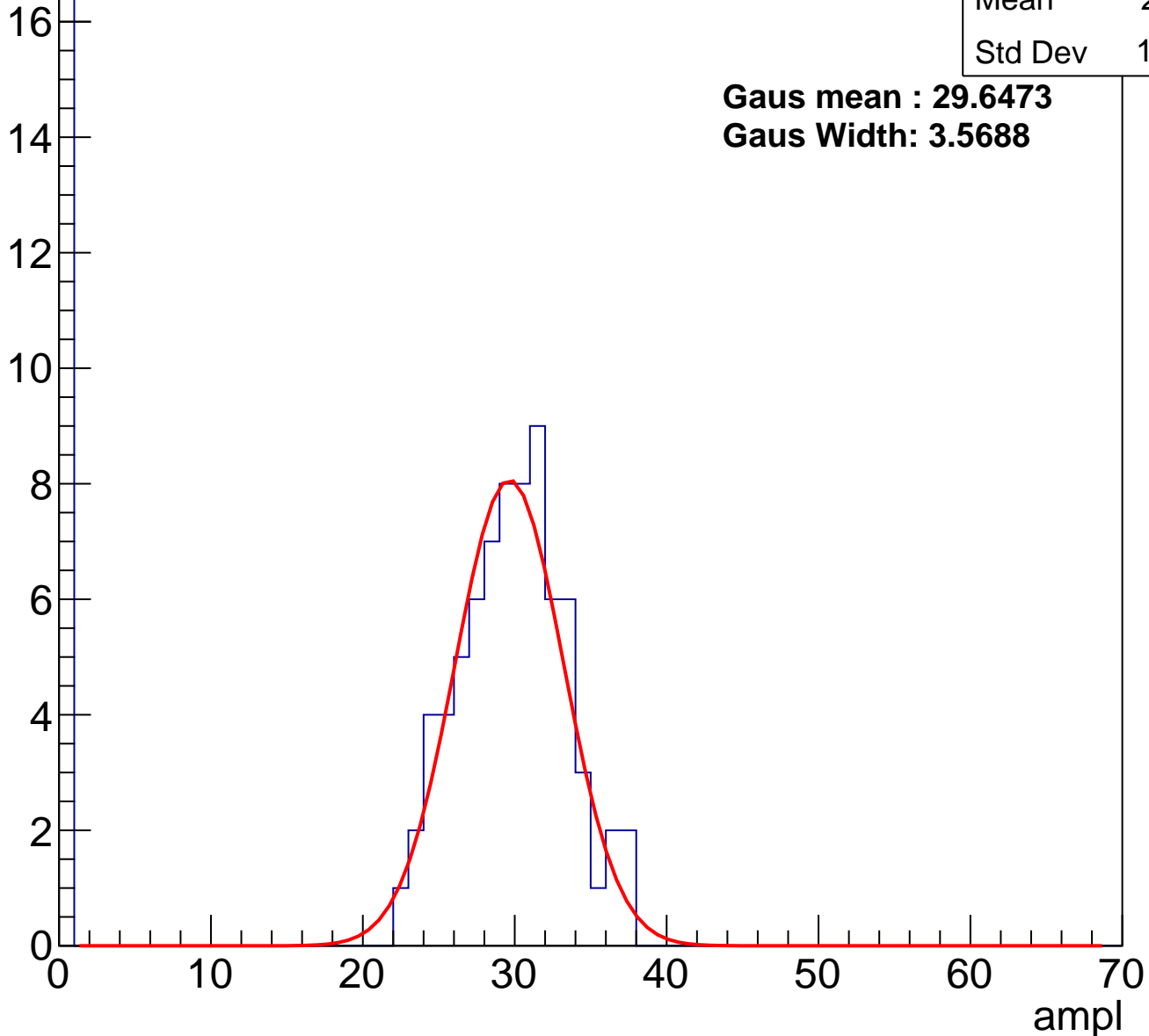
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	91
Mean	23.91
Std Dev	11.88

**Gaus mean : 29.6473**

**Gaus Width: 3.5688**

Entry



# B1L103S, U26-ch43, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	86
Mean	31.12
Std Dev	14.05

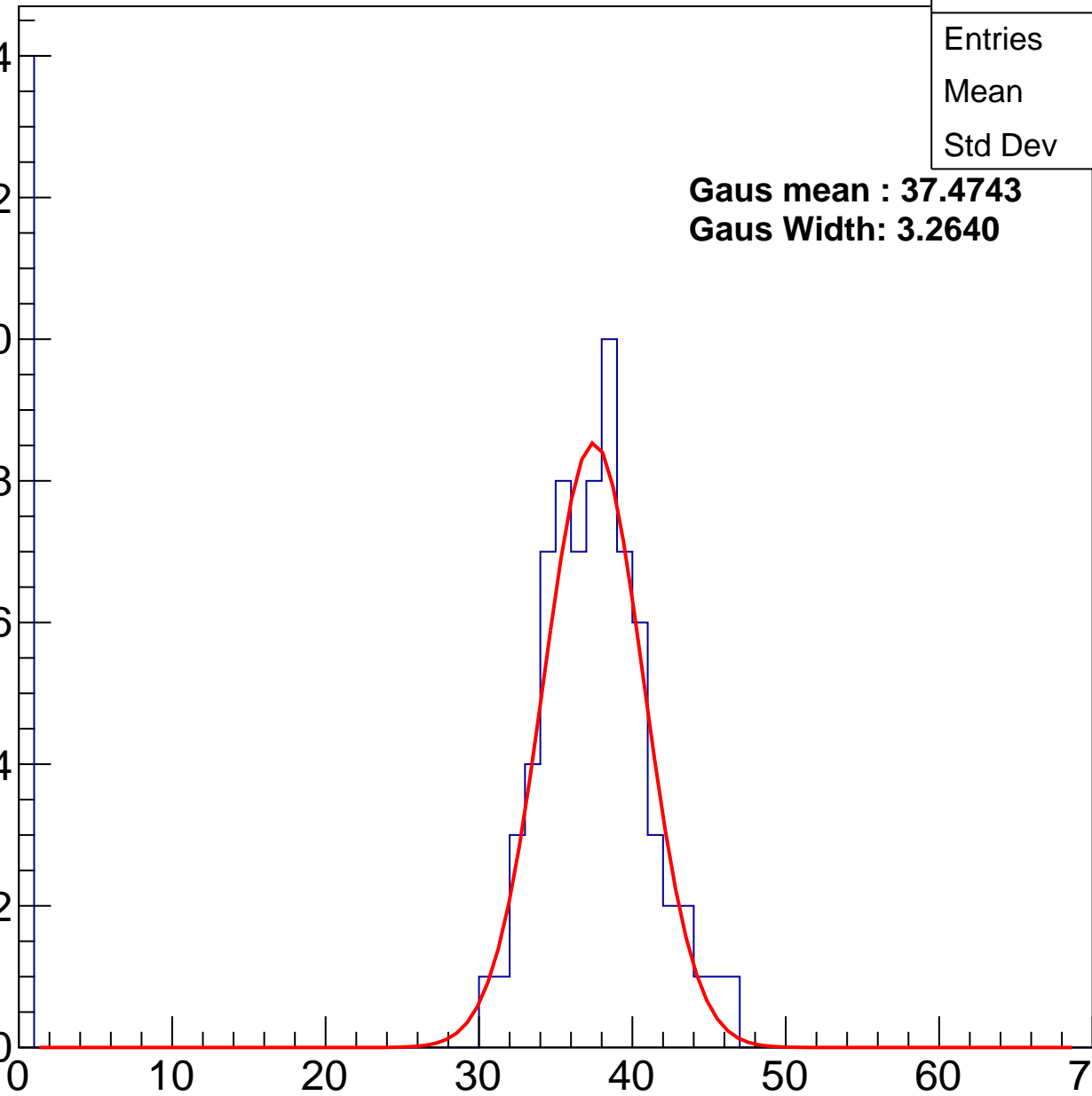
**Gaus mean : 37.4743**

**Gaus Width: 3.2640**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U26-ch43, adc2

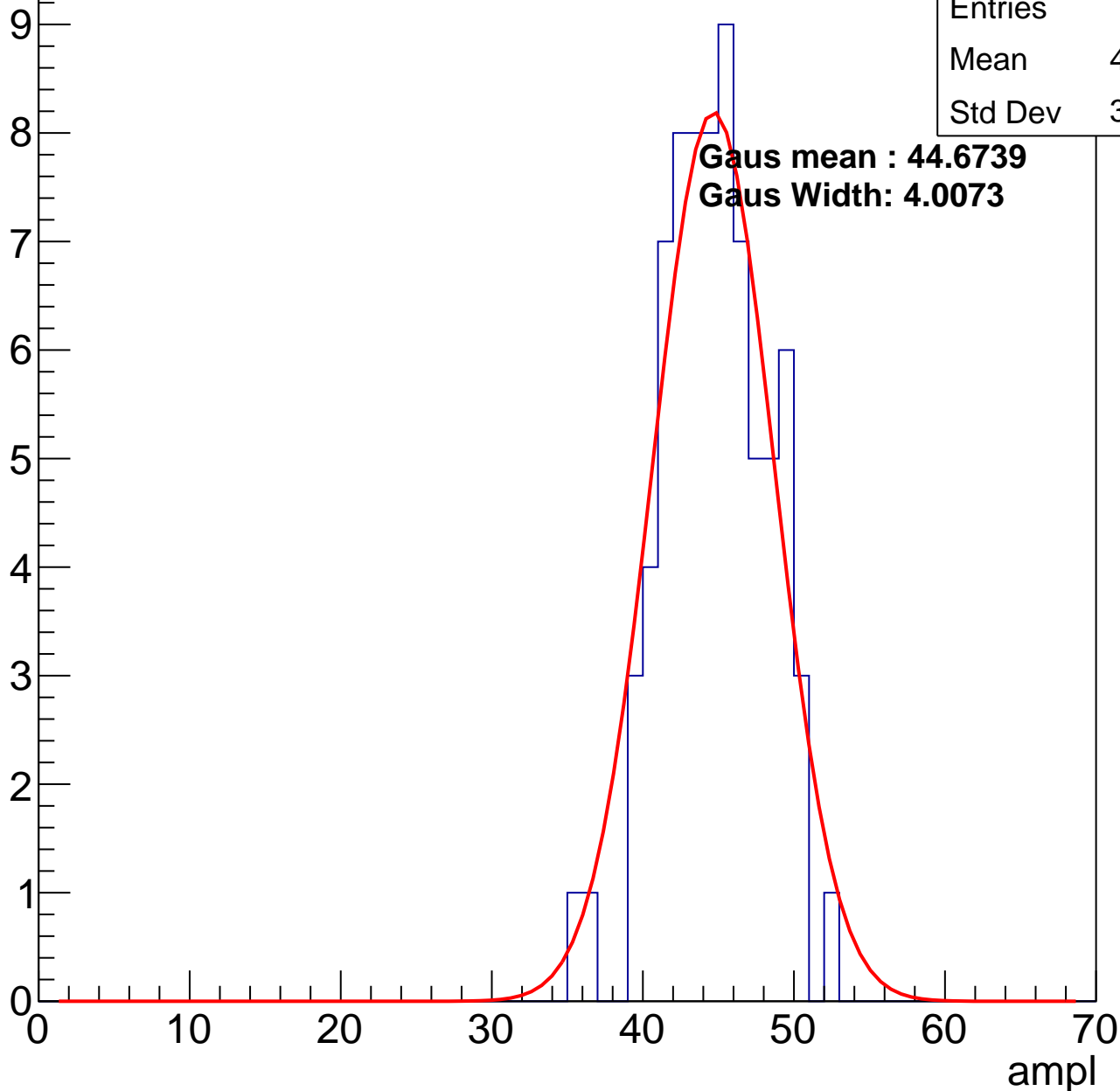
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	76
Mean	44.28
Std Dev	3.374

**Gaus mean : 44.6739**

**Gaus Width: 4.0073**

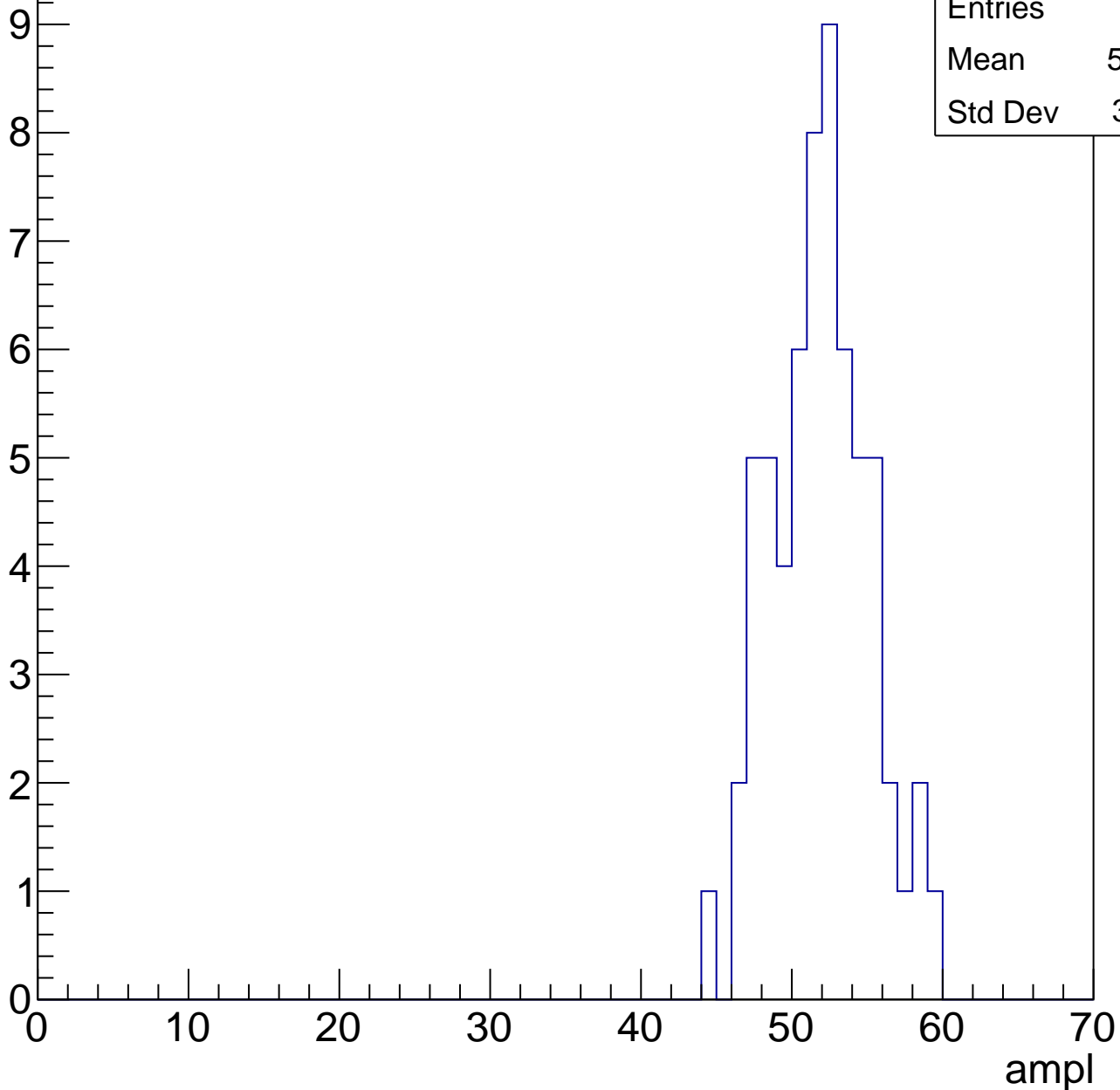


# B1L103S, U26-ch43, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	62
Mean	51.45
Std Dev	3.211

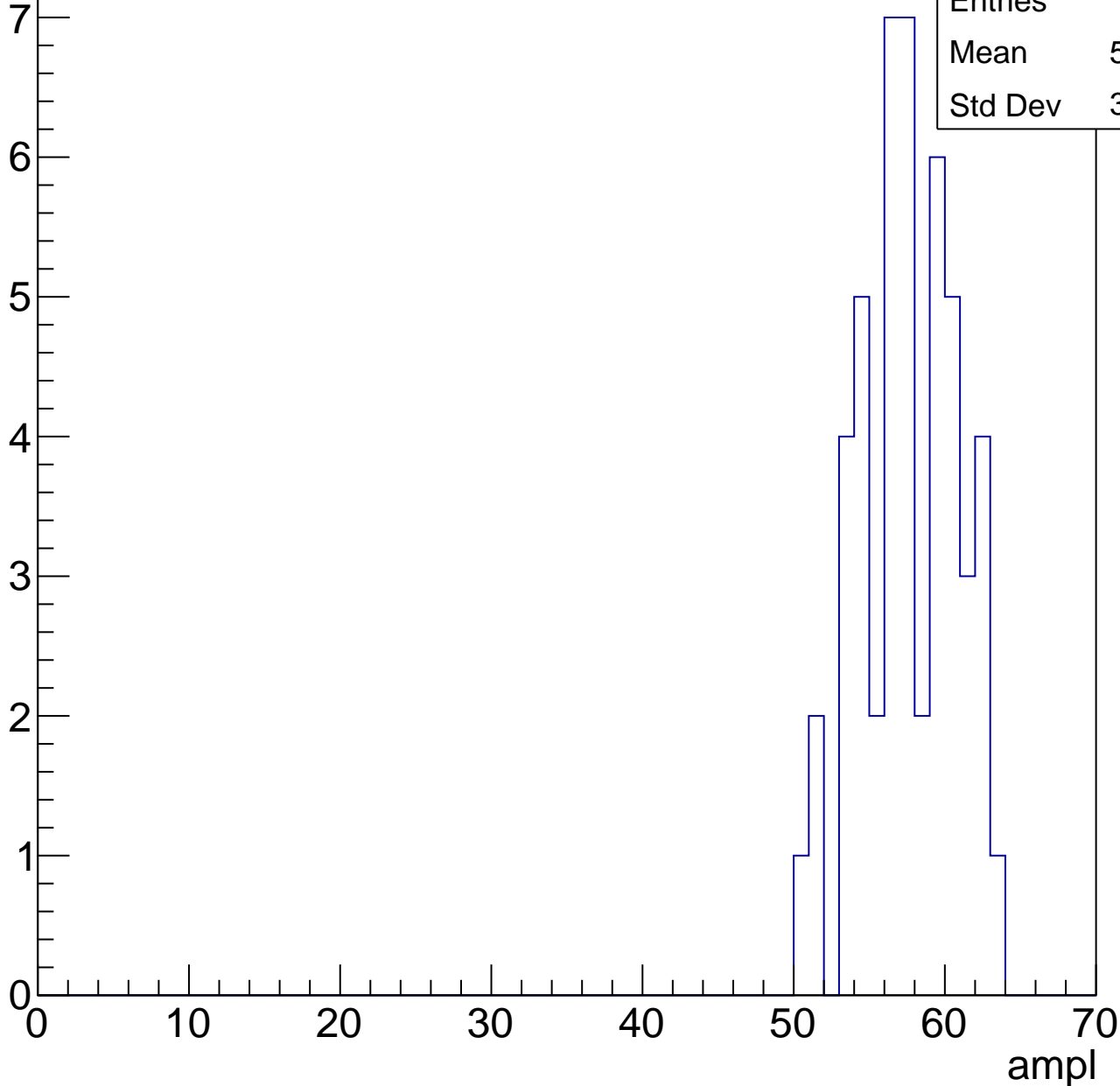


# B1L103S, U26-ch43, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	49
Mean	57.12
Std Dev	3.192

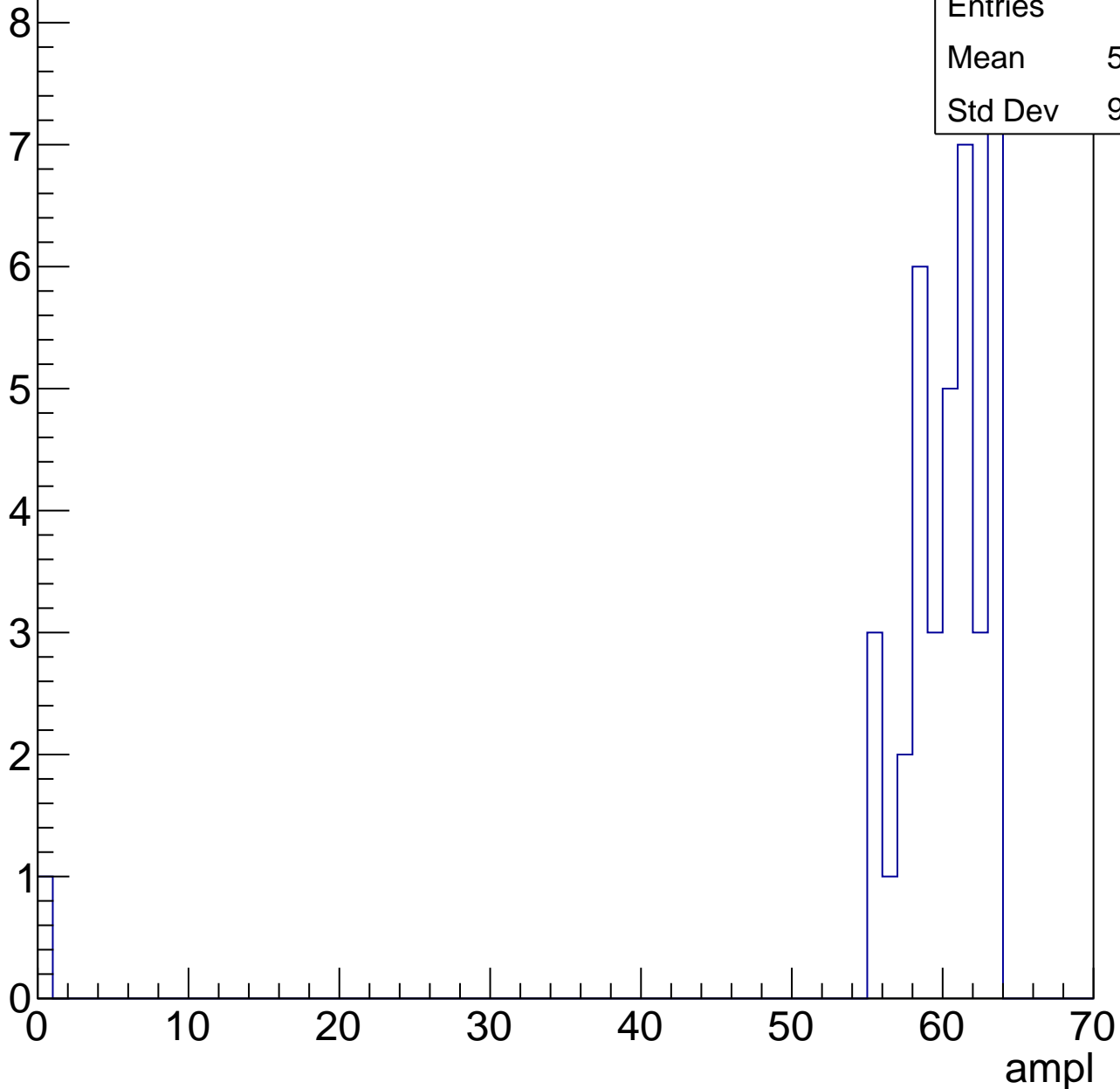


# B1L103S, U26-ch43, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	39
Mean	58.38
Std Dev	9.773



# B1L103S, U26-ch43, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry





# B1L103S, U26-ch43, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



# B1L103S, U26-ch44, adc0

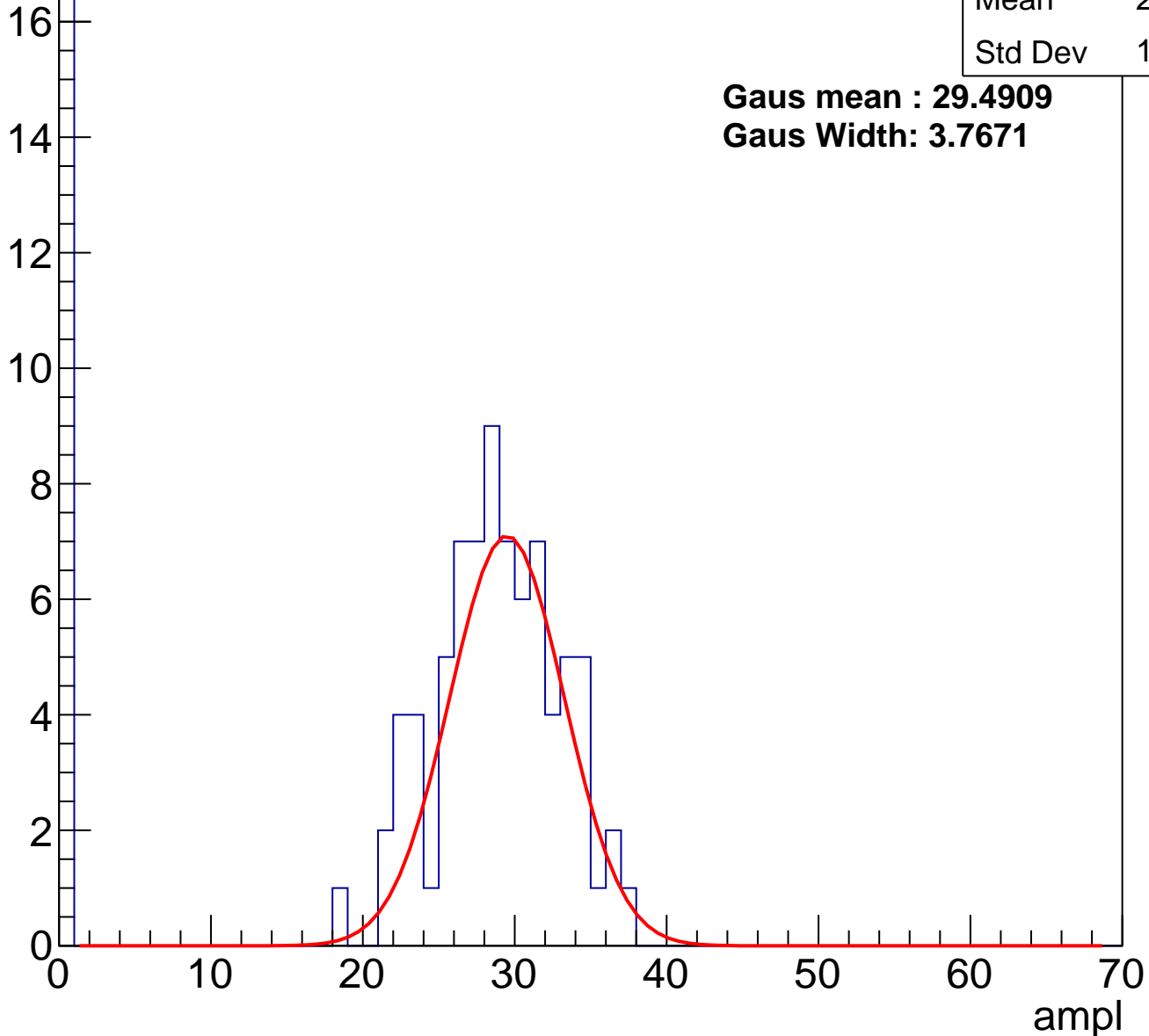
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	95
Mean	23.36
Std Dev	11.49

**Gaus mean : 29.4909**

**Gaus Width: 3.7671**

Entry



# B1L103S, U26-ch44, adc1

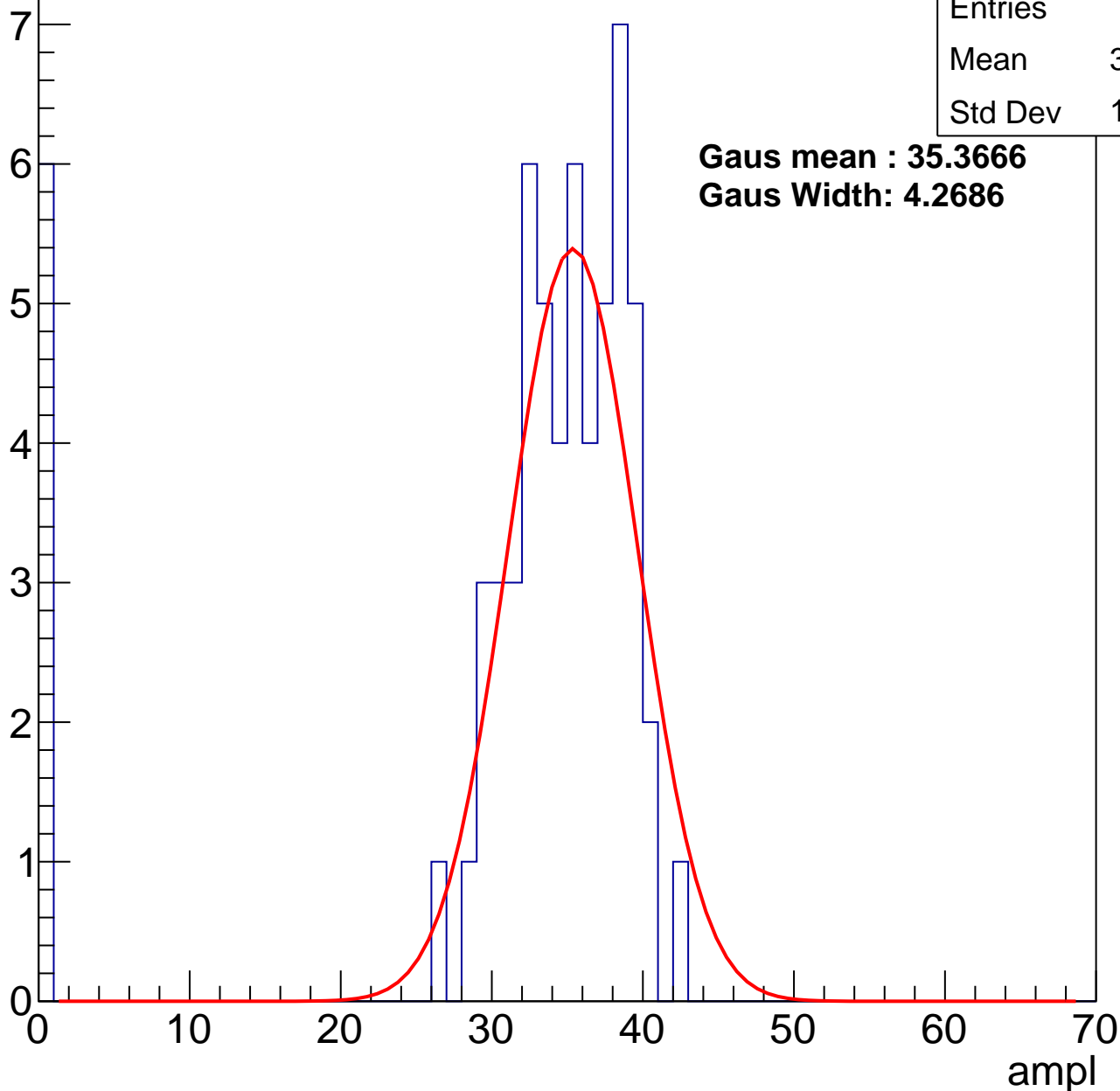
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	62
Mean	31.27
Std Dev	10.77

**Gaus mean : 35.3666**

**Gaus Width: 4.2686**



# B1L103S, U26-ch44, adc2

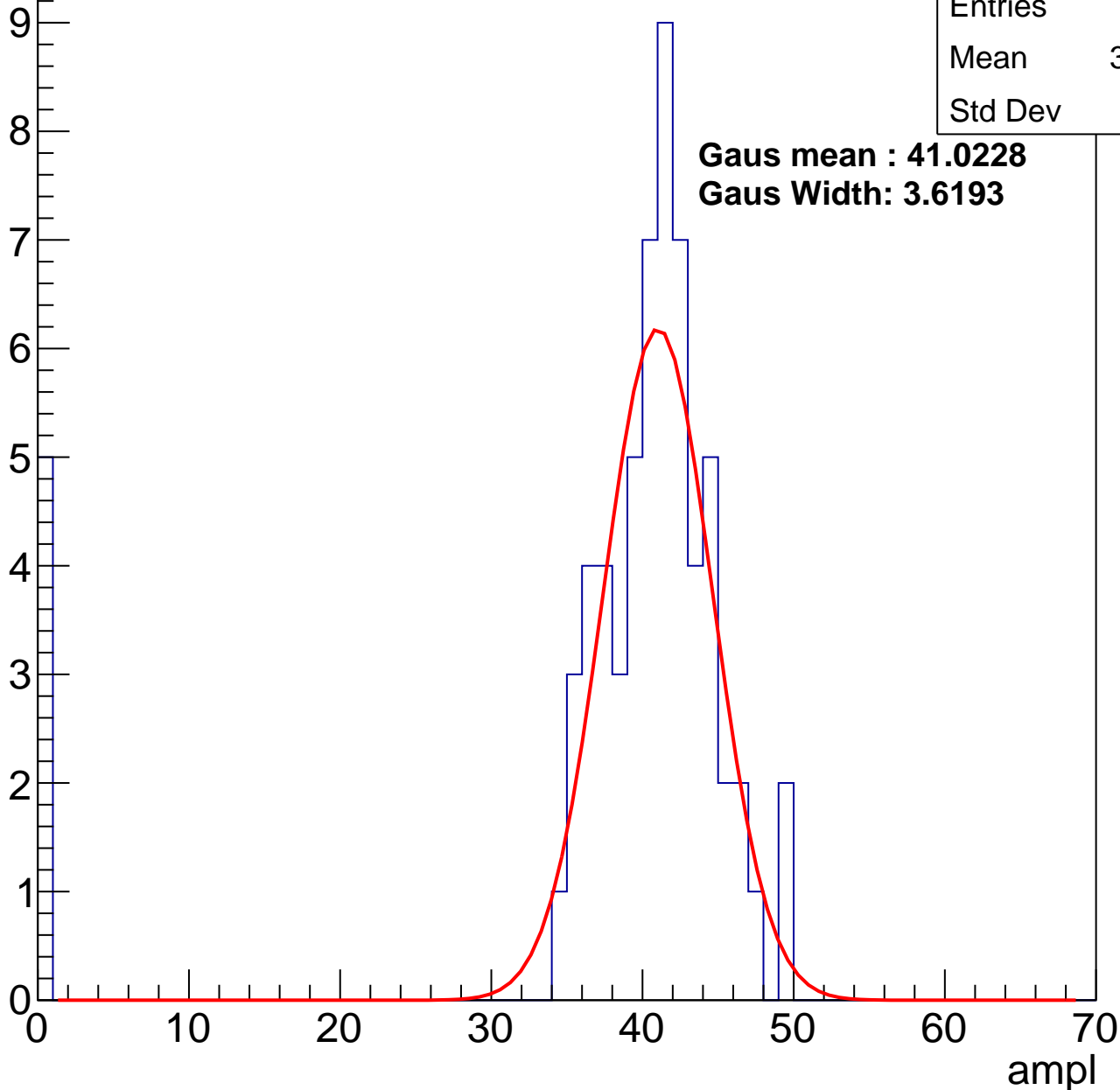
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	64
Mean	37.53
Std Dev	11.4

**Gaus mean : 41.0228**

**Gaus Width: 3.6193**

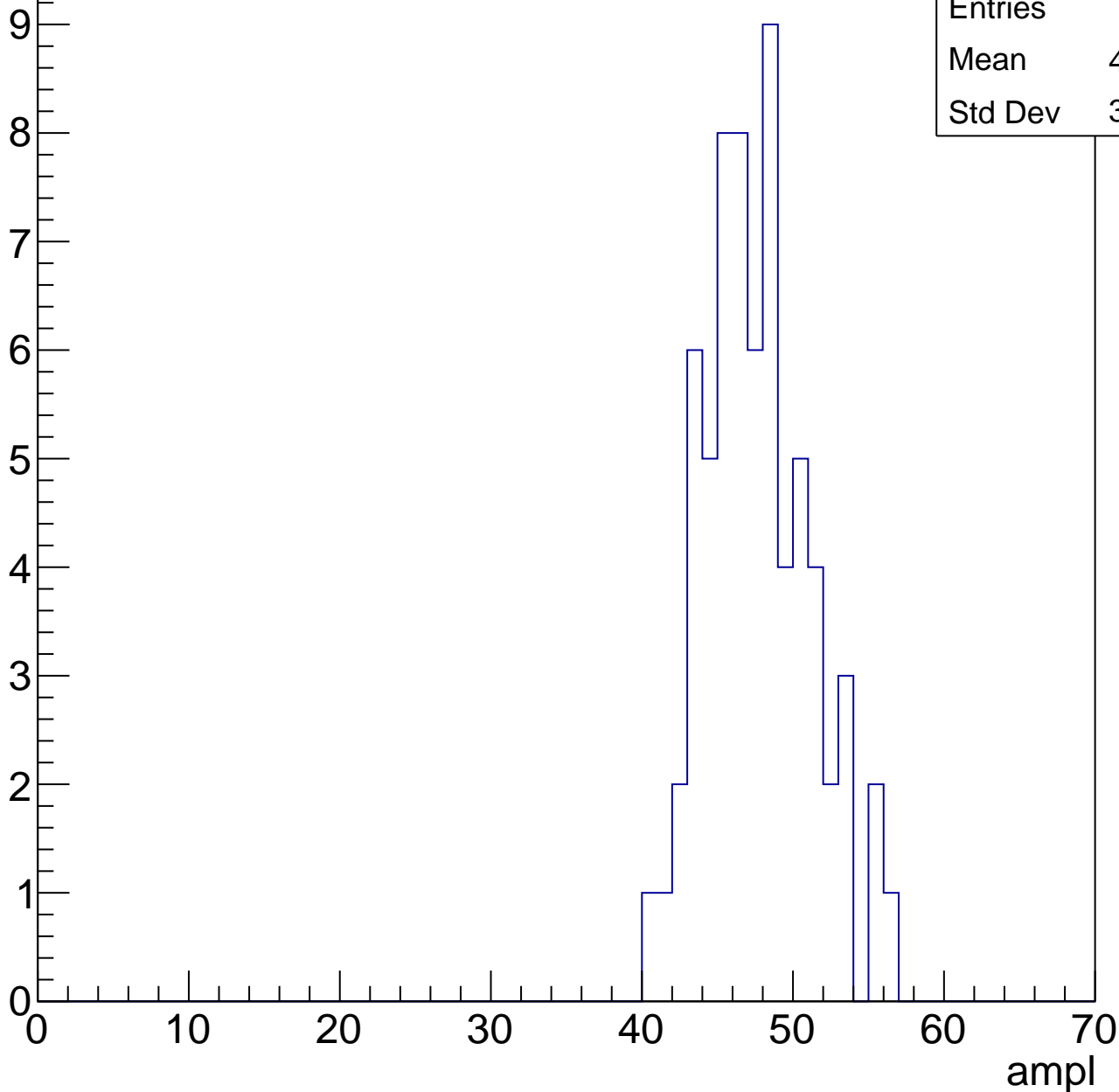


# B1L103S, U26-ch44, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	67
Mean	47.22
Std Dev	3.485

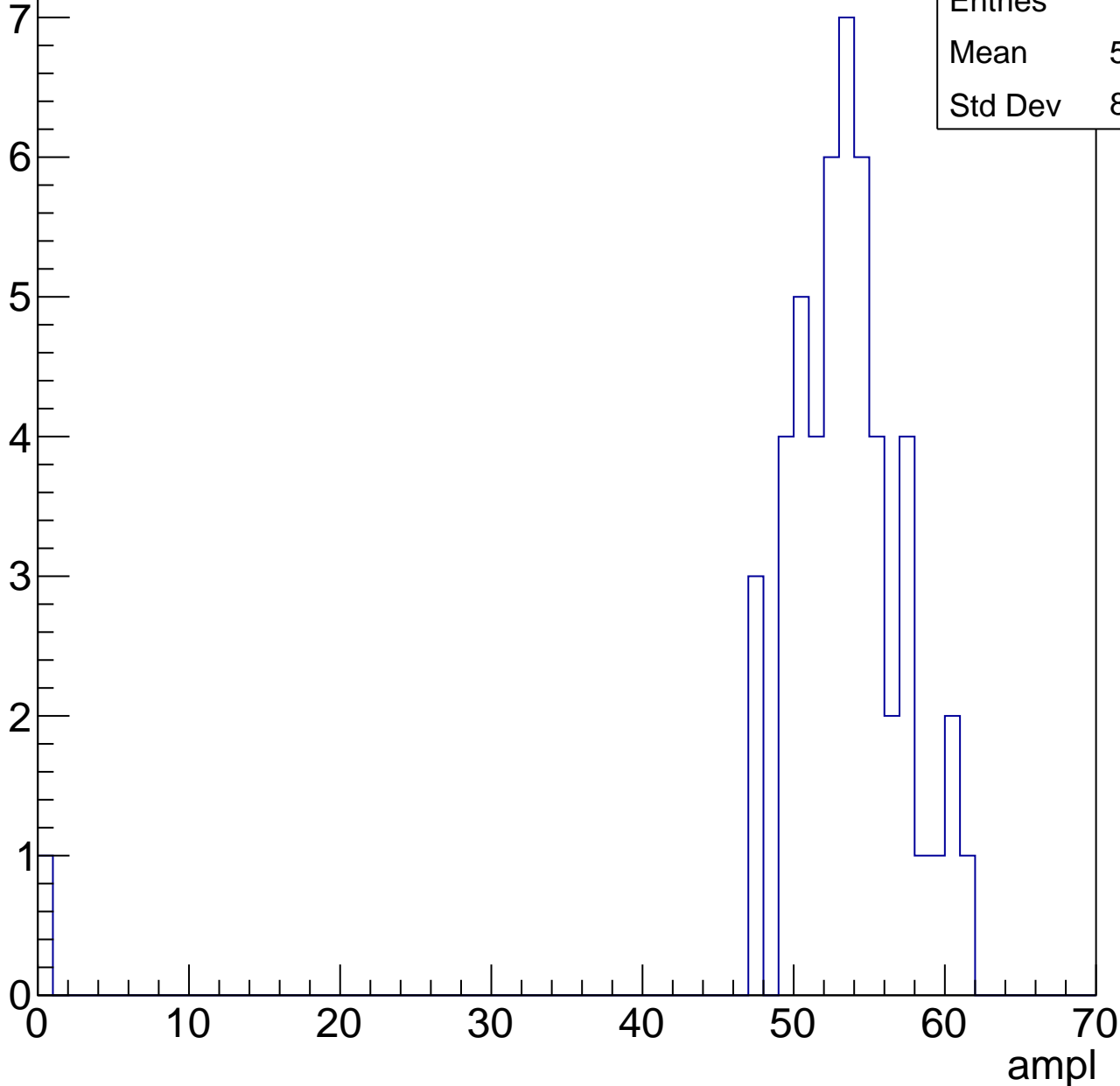


# B1L103S, U26-ch44, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	51
Mean	52.08
Std Dev	8.083

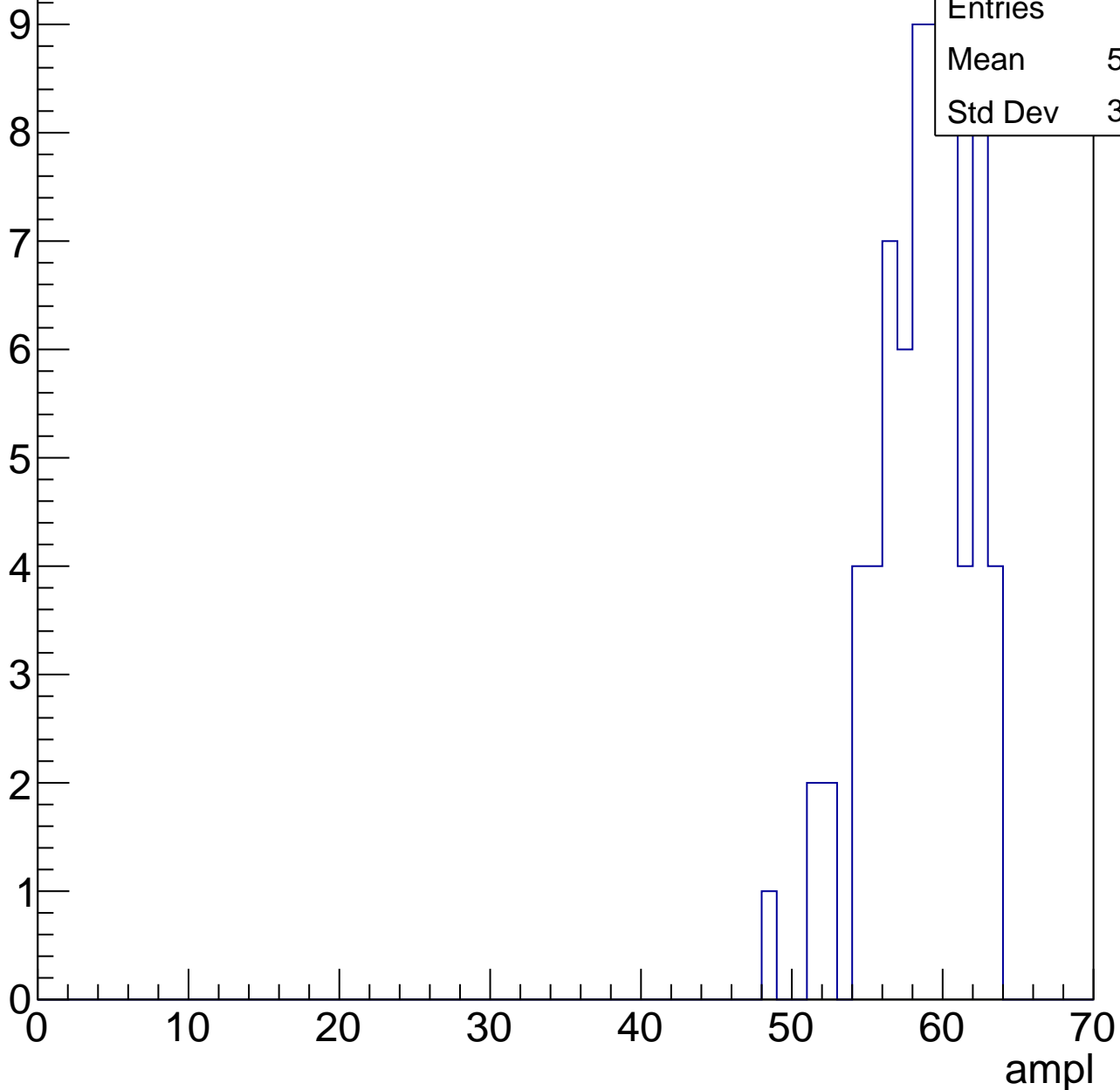


# B1L103S, U26-ch44, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	69
Mean	58.13
Std Dev	3.239

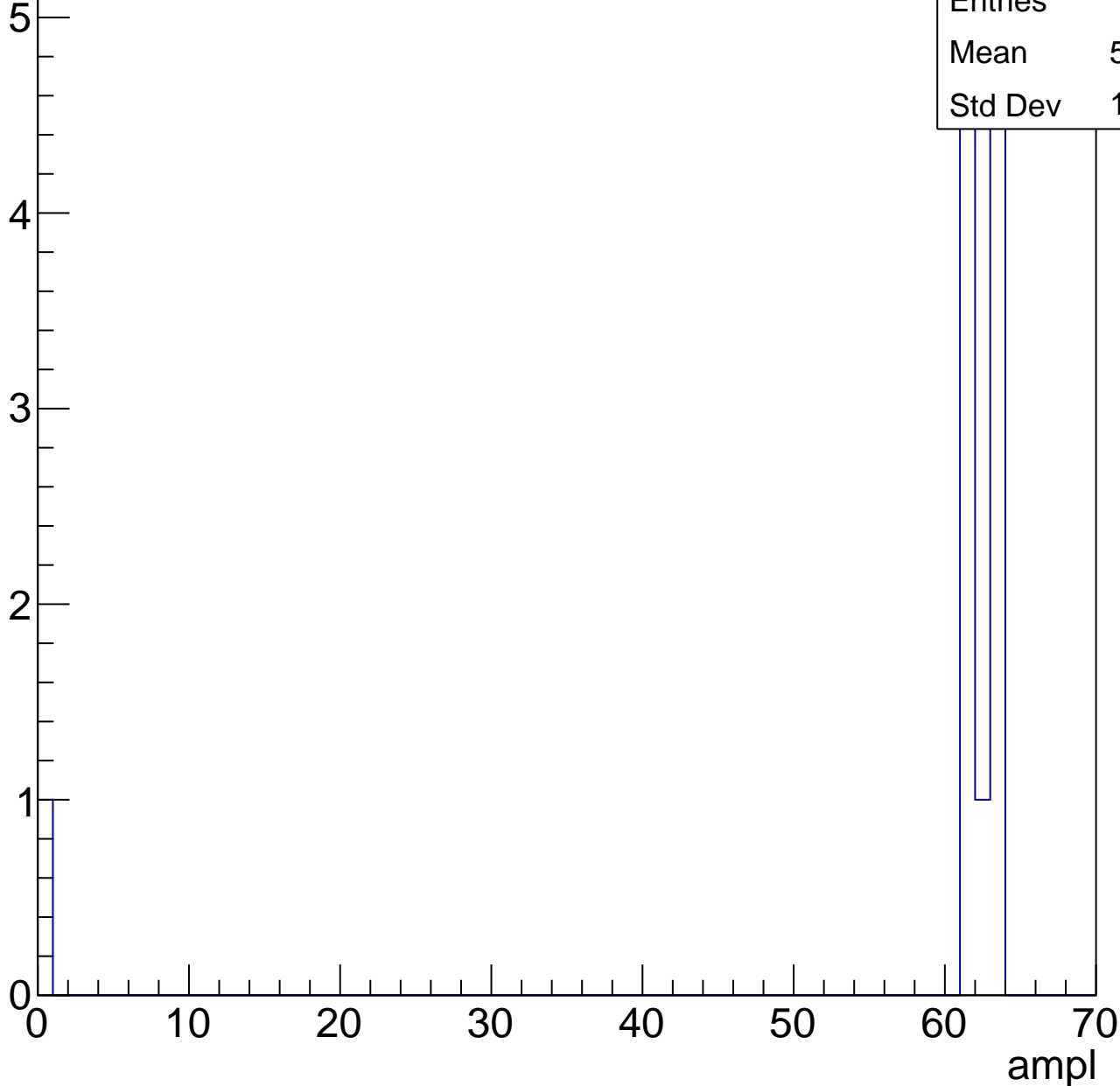


# B1L103S, U26-ch44, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	12
Mean	56.83
Std Dev	17.16





# B1L103S, U26-ch44, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	20
Mean	3.15
Std Dev	13.73

Entry

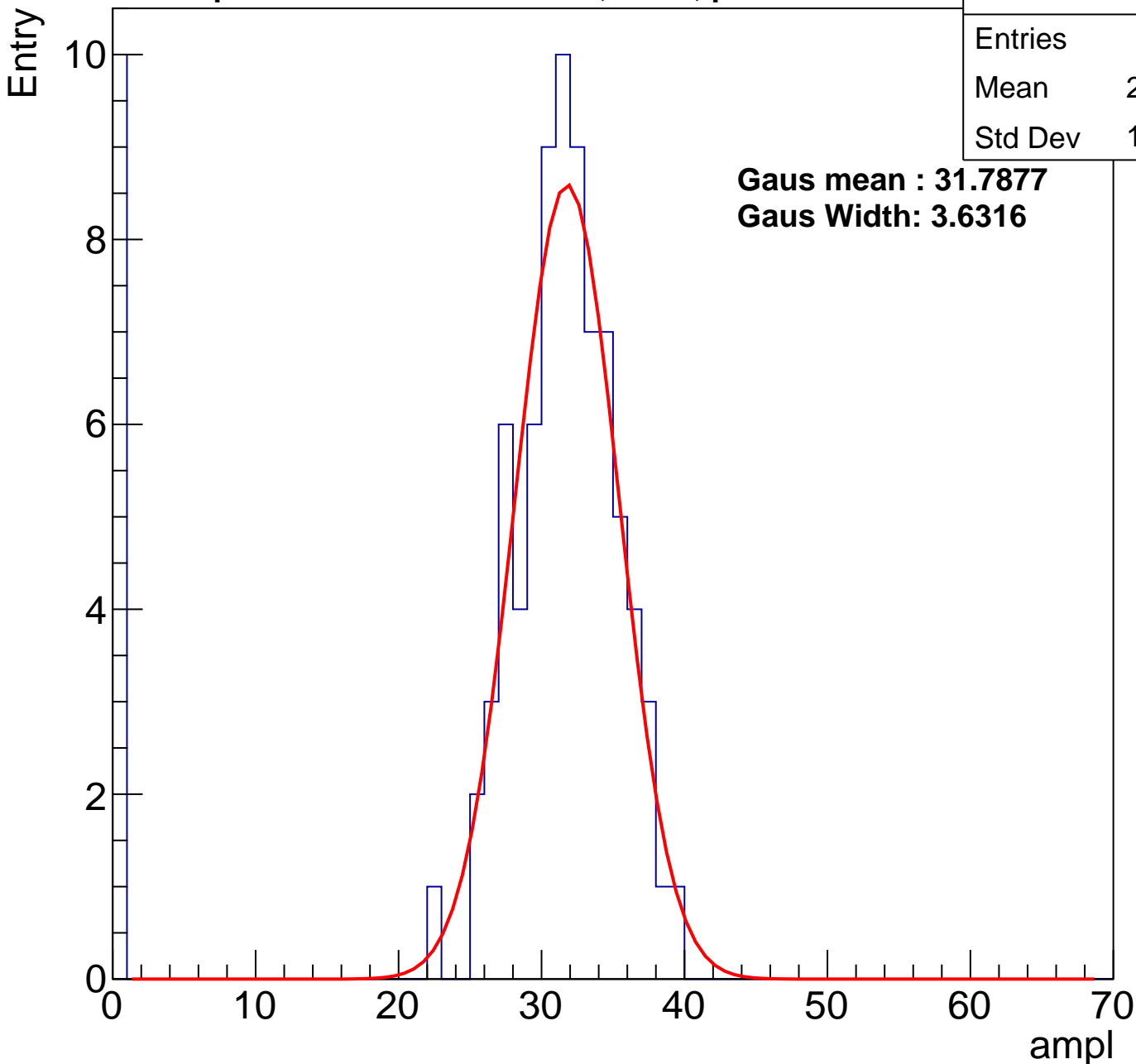


# B1L103S, U26-ch45, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	88
Mean	27.75
Std Dev	10.43

**Gaus mean : 31.7877**  
**Gaus Width: 3.6316**



# B1L103S, U26-ch45, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	62
Mean	30.69
Std Dev	14.49

**Gaus mean : 37.6499**

**Gaus Width: 2.9133**

Entry

10

8

6

4

2

0

0

10

20

30

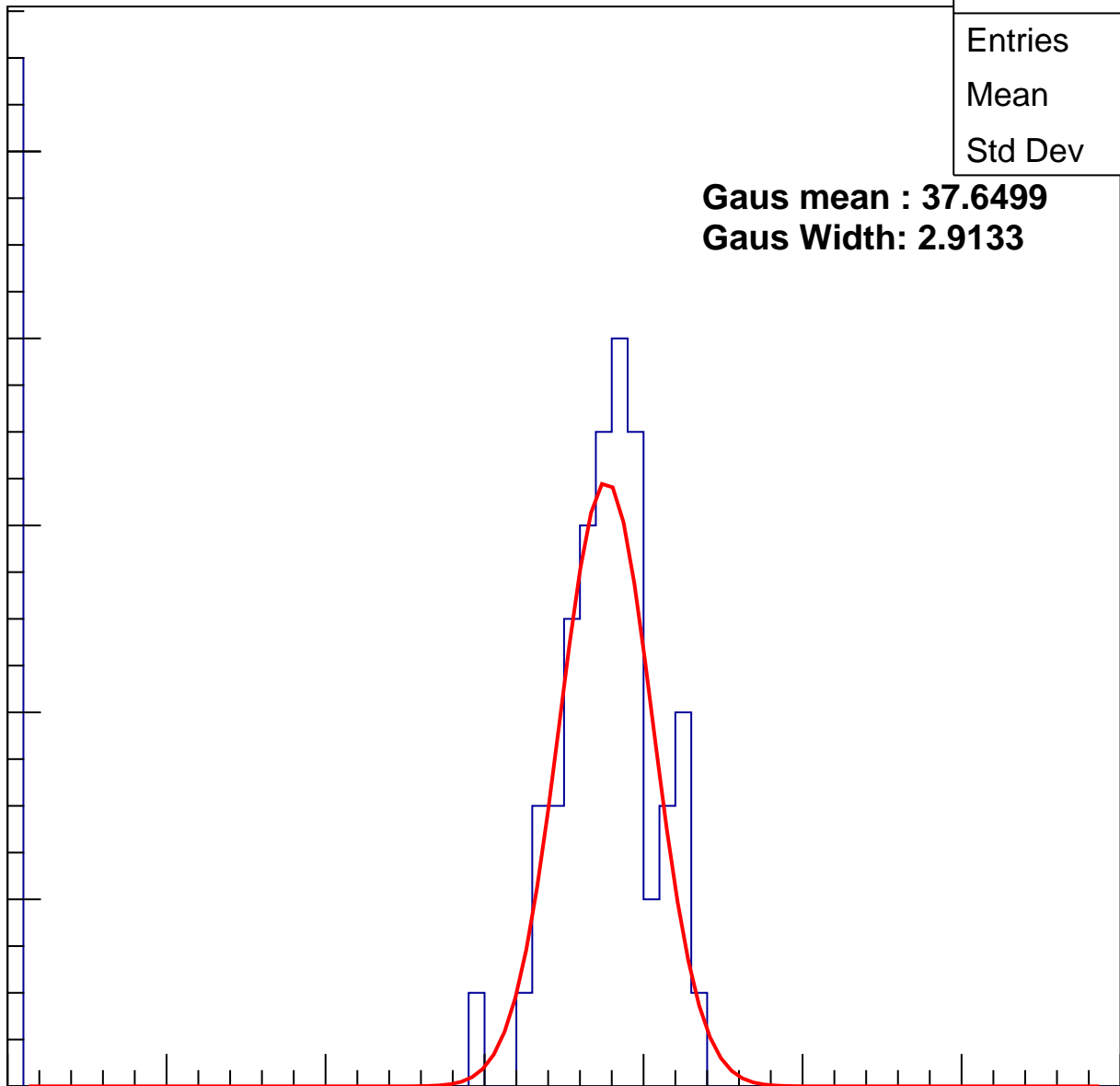
40

50

60

70

ampl



# B1L103S, U26-ch45, adc2

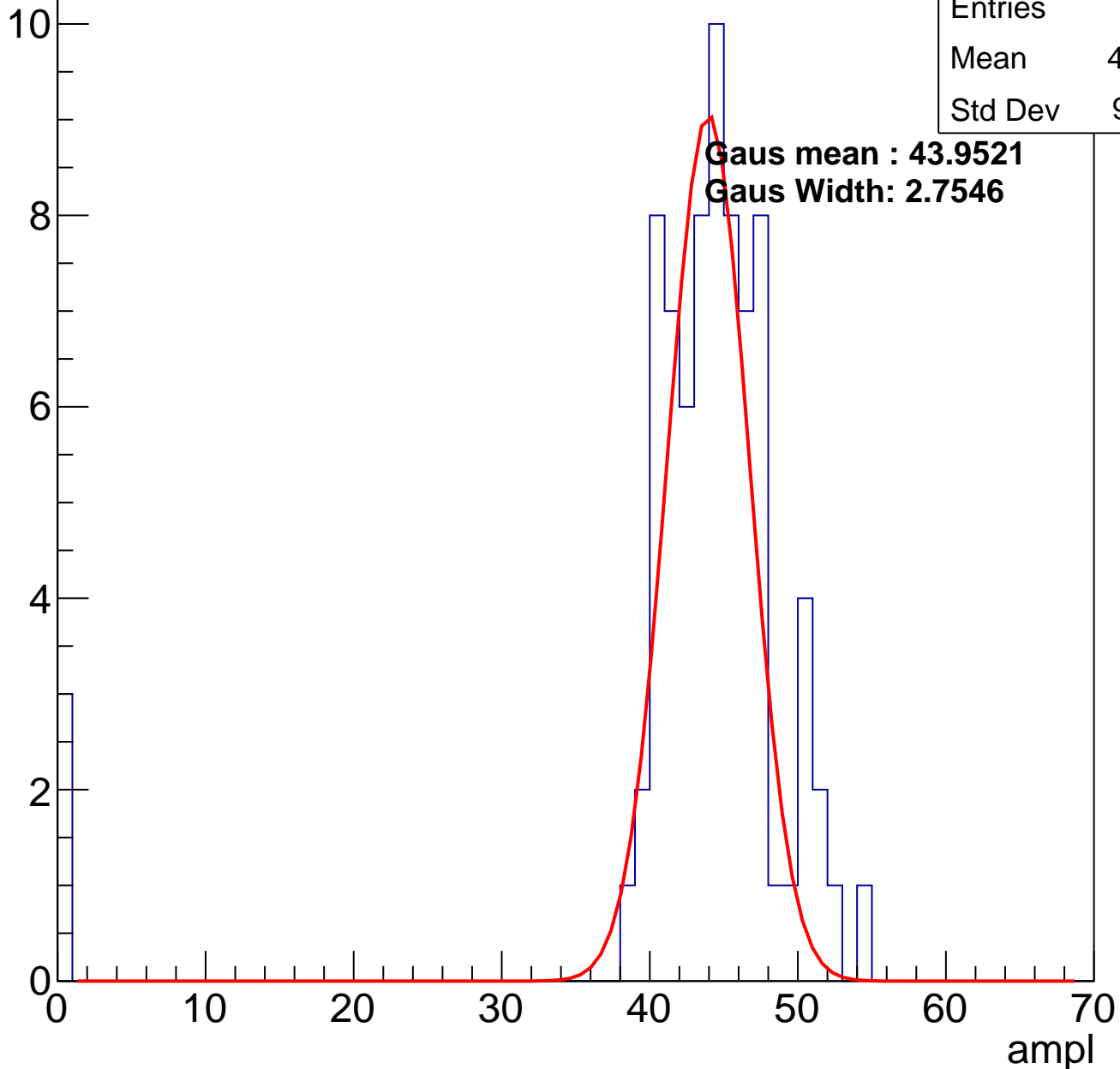
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	78
Mean	42.59
Std Dev	9.141

**Gaus mean : 43.9521**

**Gaus Width: 2.7546**

Entry

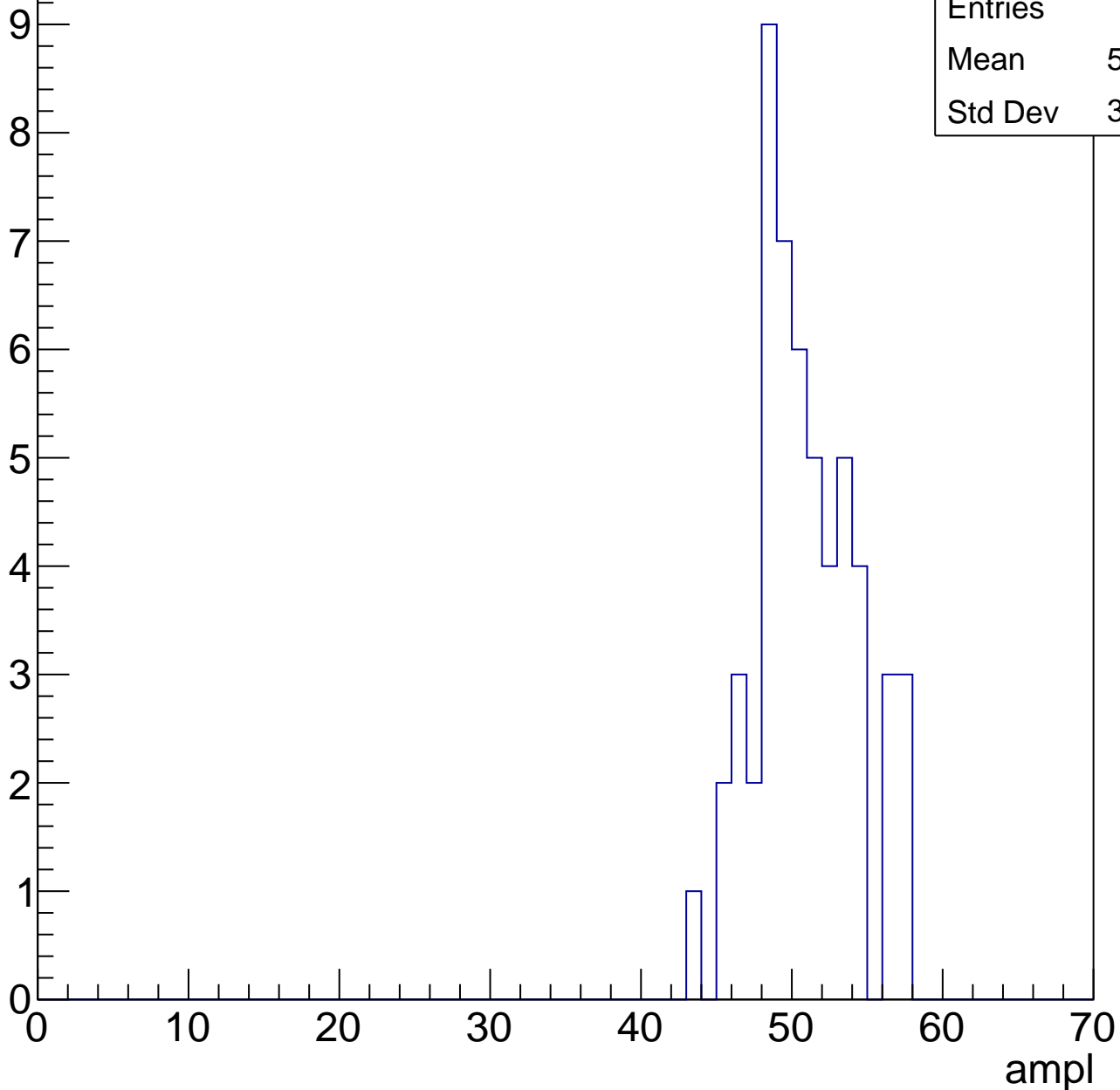


# B1L103S, U26-ch45, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

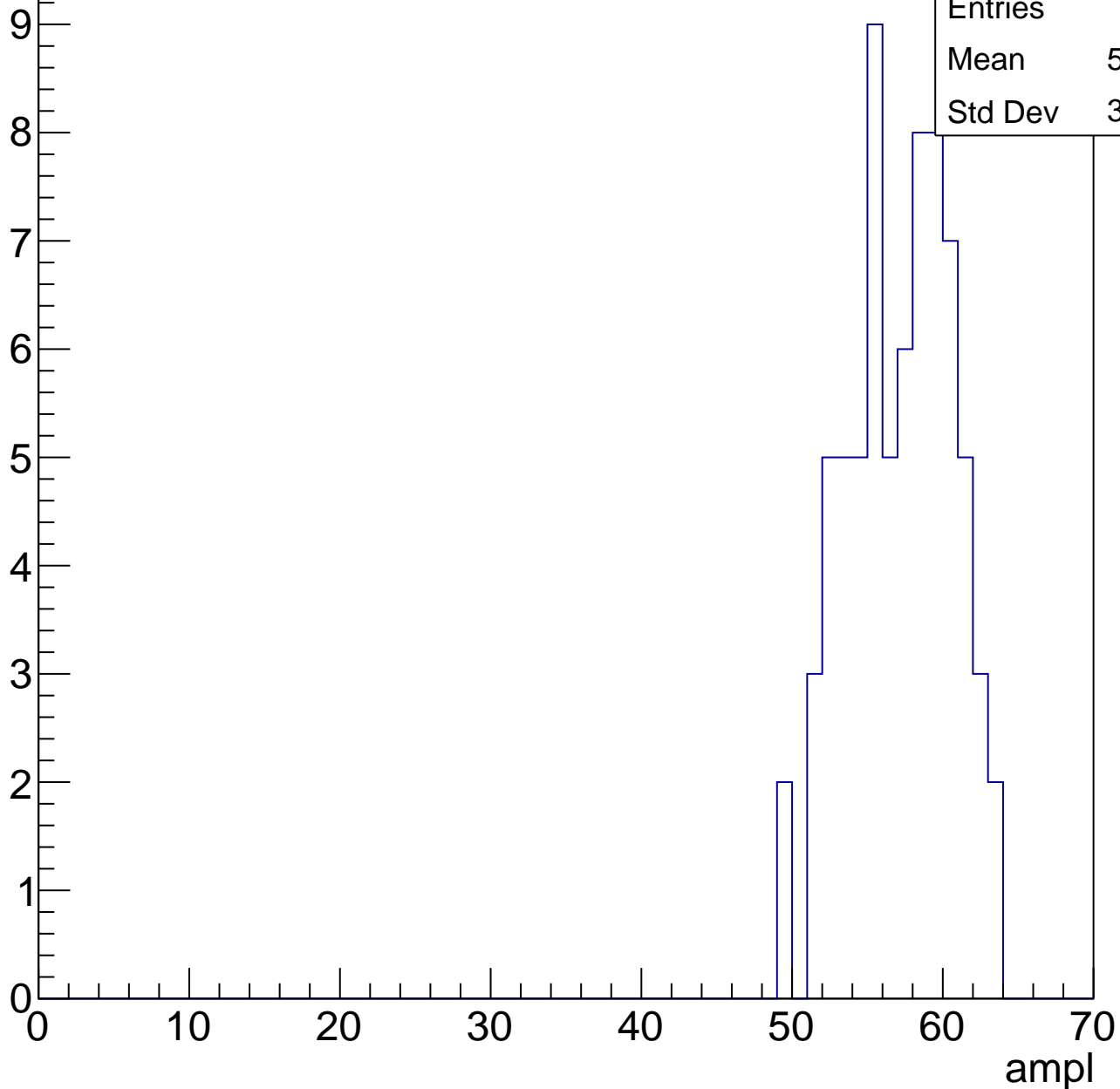
Entries	54
Mean	50.43
Std Dev	3.286



# B1L103S, U26-ch45, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



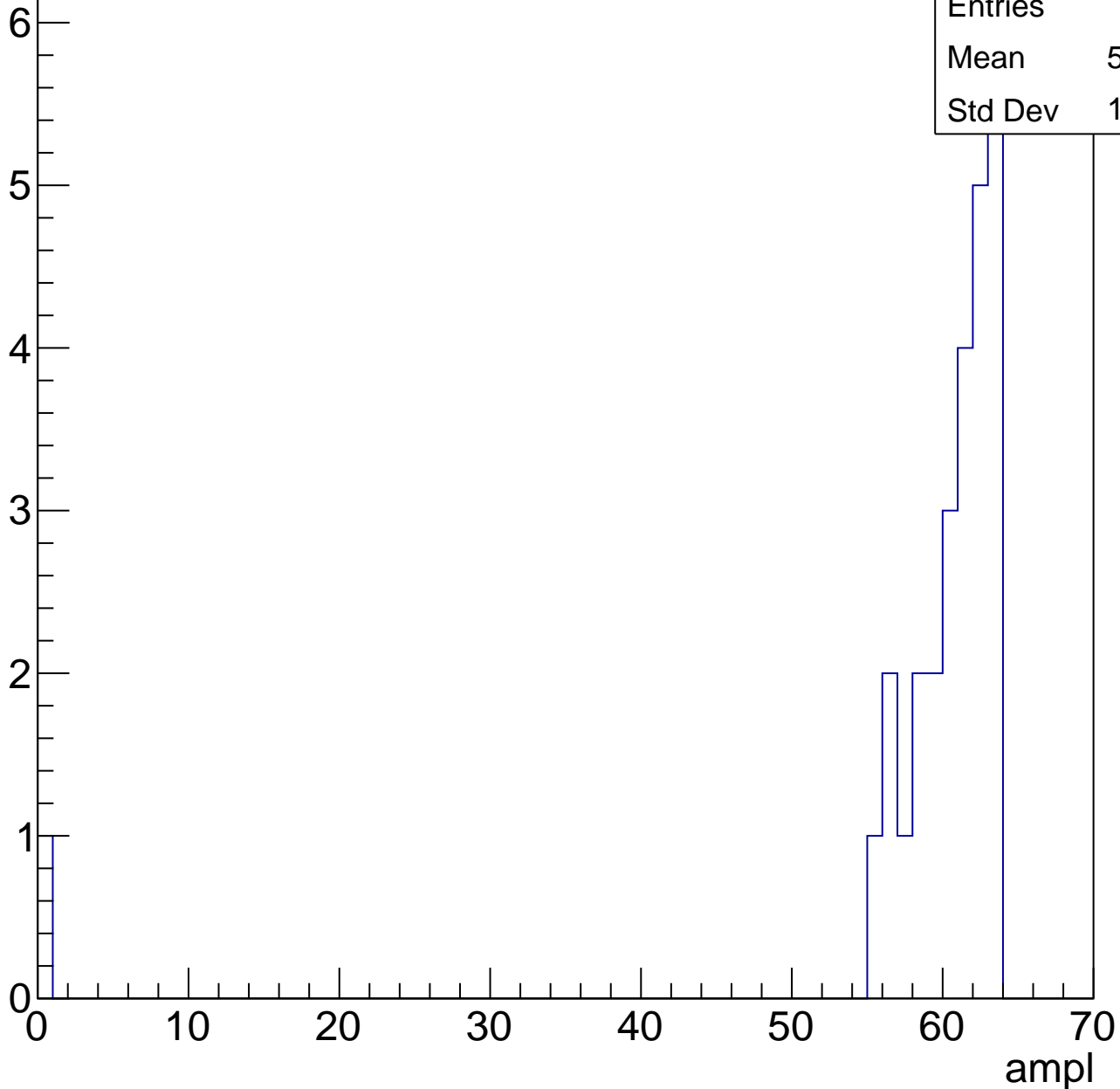
Entries	73
Mean	56.66
Std Dev	3.409

# B1L103S, U26-ch45, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	27
Mean	58.15
Std Dev	11.65



# B1L103S, U26-ch45, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	5
Mean	62.2
Std Dev	0.7483

ampl

0 10 20 30 40 50 60 70



# B1L103S, U26-ch45, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



Entries	18
Mean	0
Std Dev	0

# B1L103S, U26-ch46, adc0

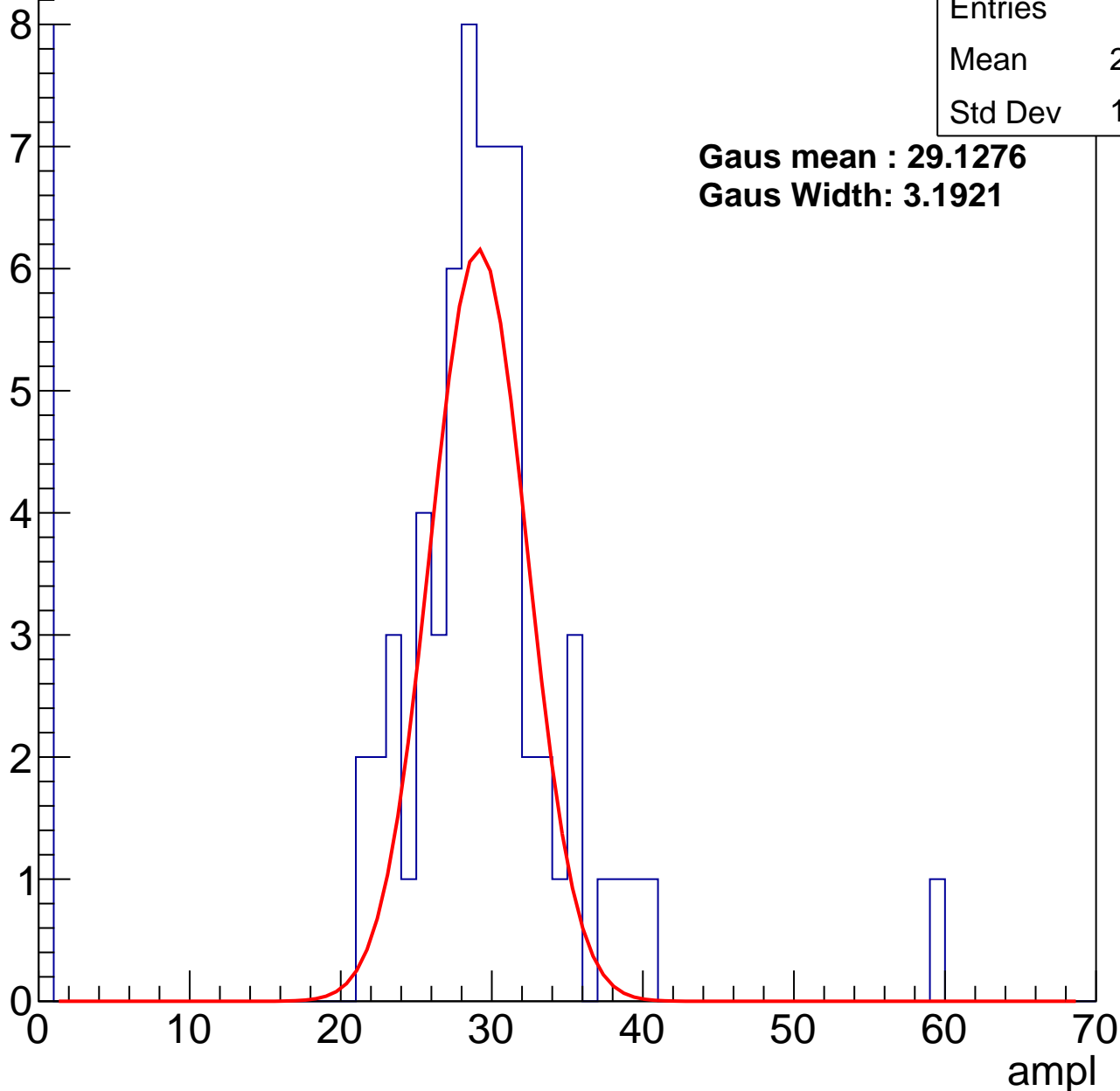
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	71
Mean	26.13
Std Dev	10.69

**Gaus mean : 29.1276**

**Gaus Width: 3.1921**



# B1L103S, U26-ch46, adc1

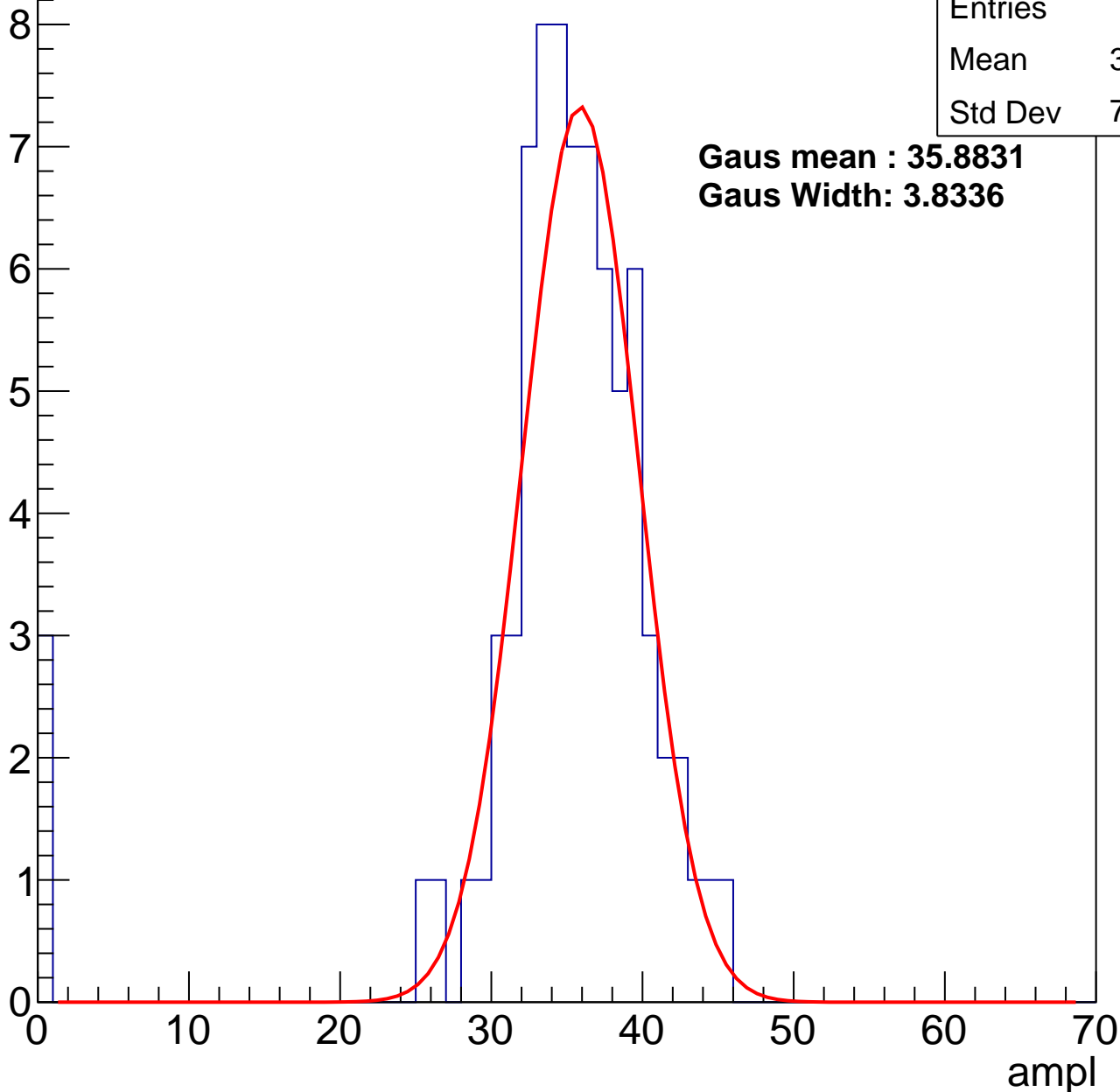
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	77
Mean	33.92
Std Dev	7.846

**Gaus mean : 35.8831**

**Gaus Width: 3.8336**



# B1L103S, U26-ch46, adc2

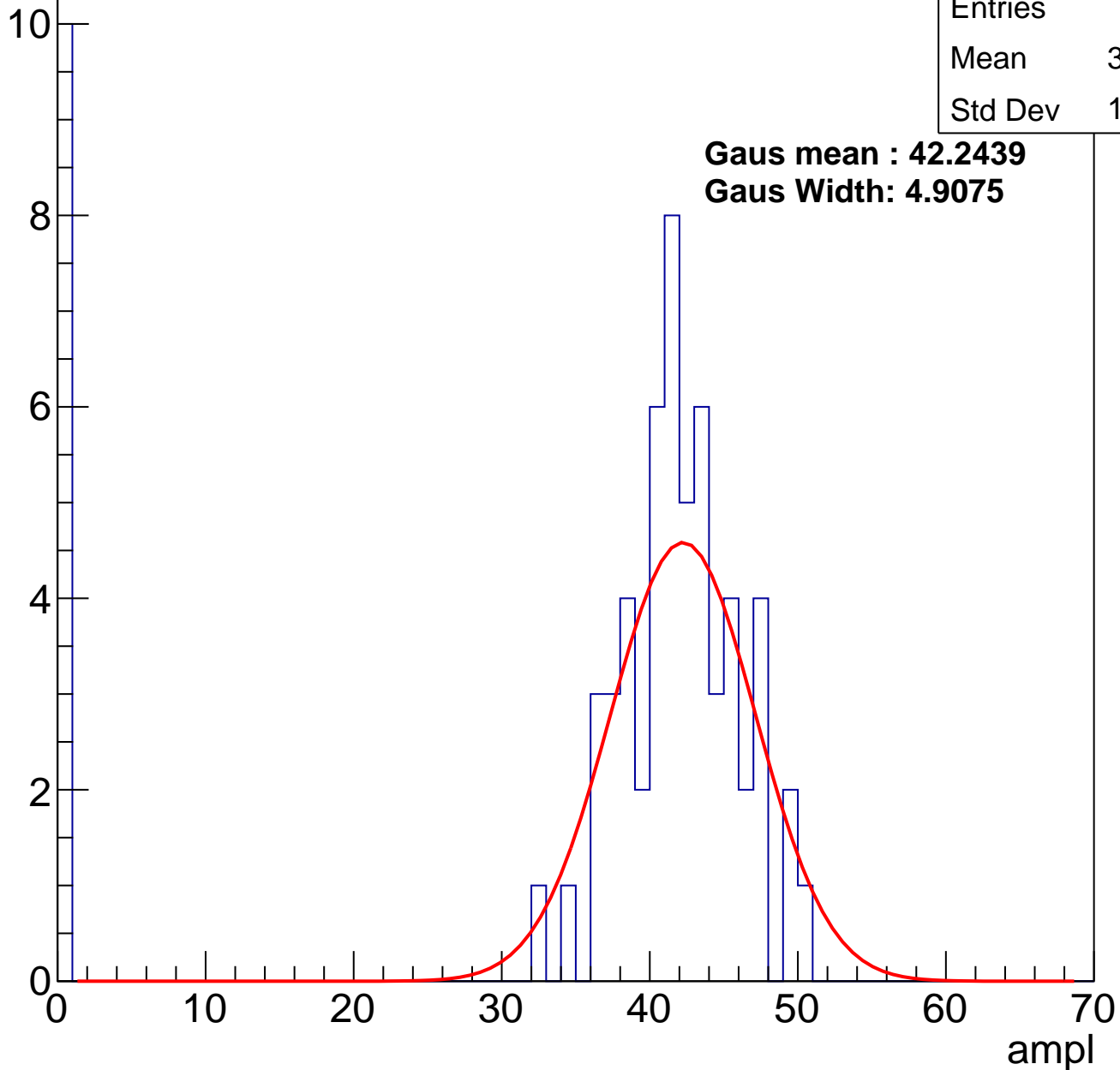
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	65
Mean	35.25
Std Dev	15.43

**Gaus mean : 42.2439**

**Gaus Width: 4.9075**

Entry

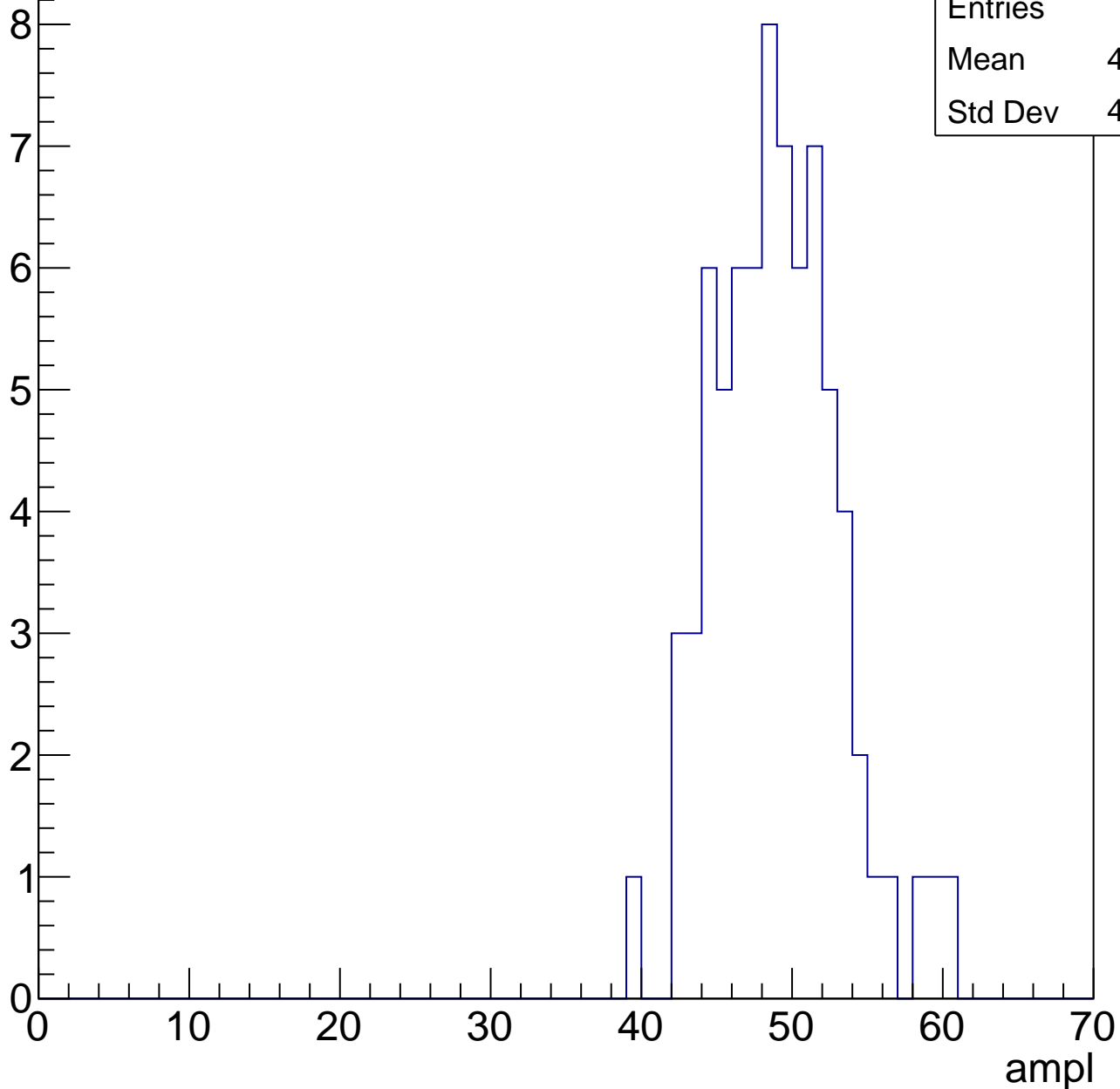


# B1L103S, U26-ch46, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

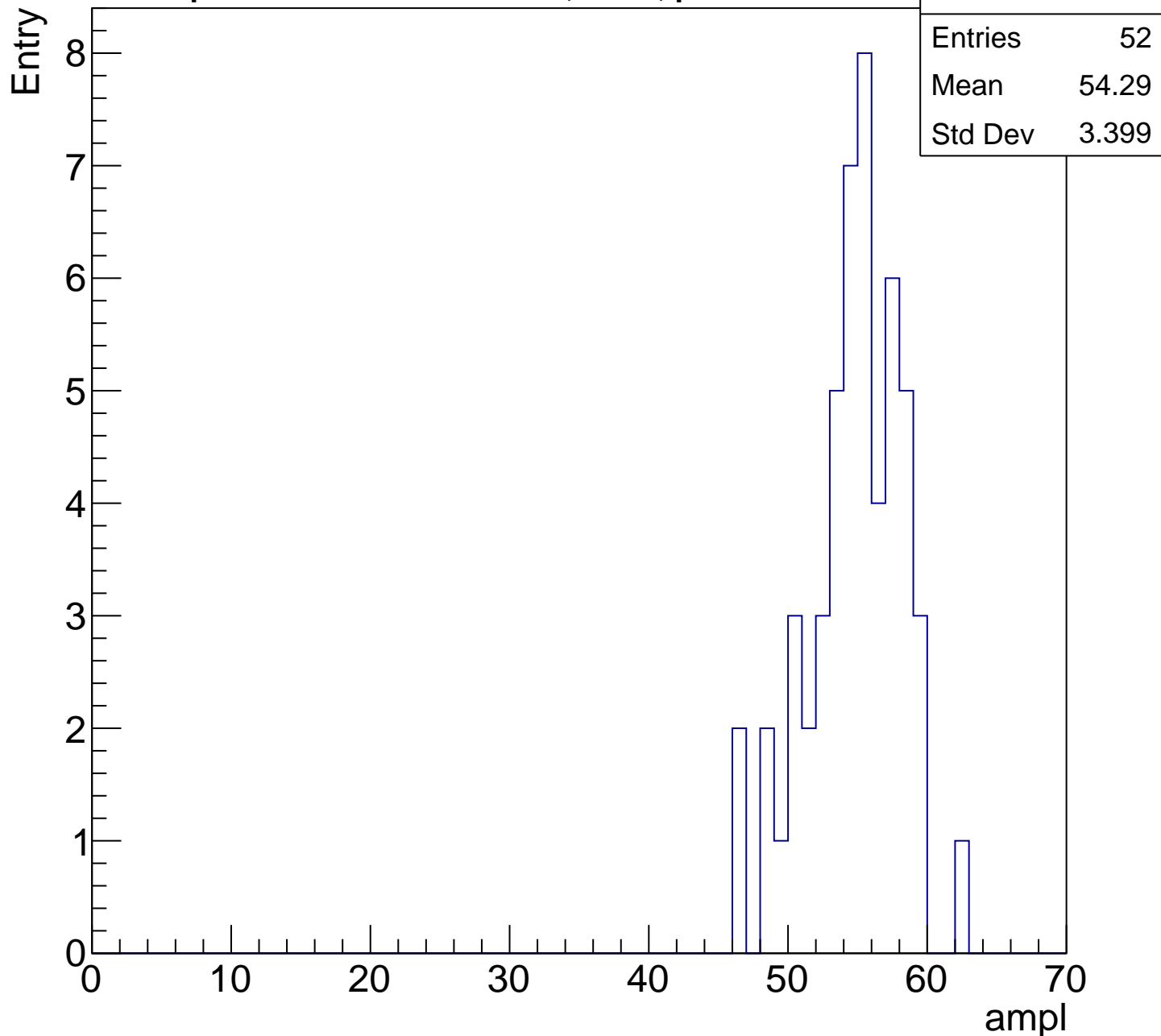
Entry

Entries	74
Mean	48.55
Std Dev	4.087



# B1L103S, U26-ch46, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

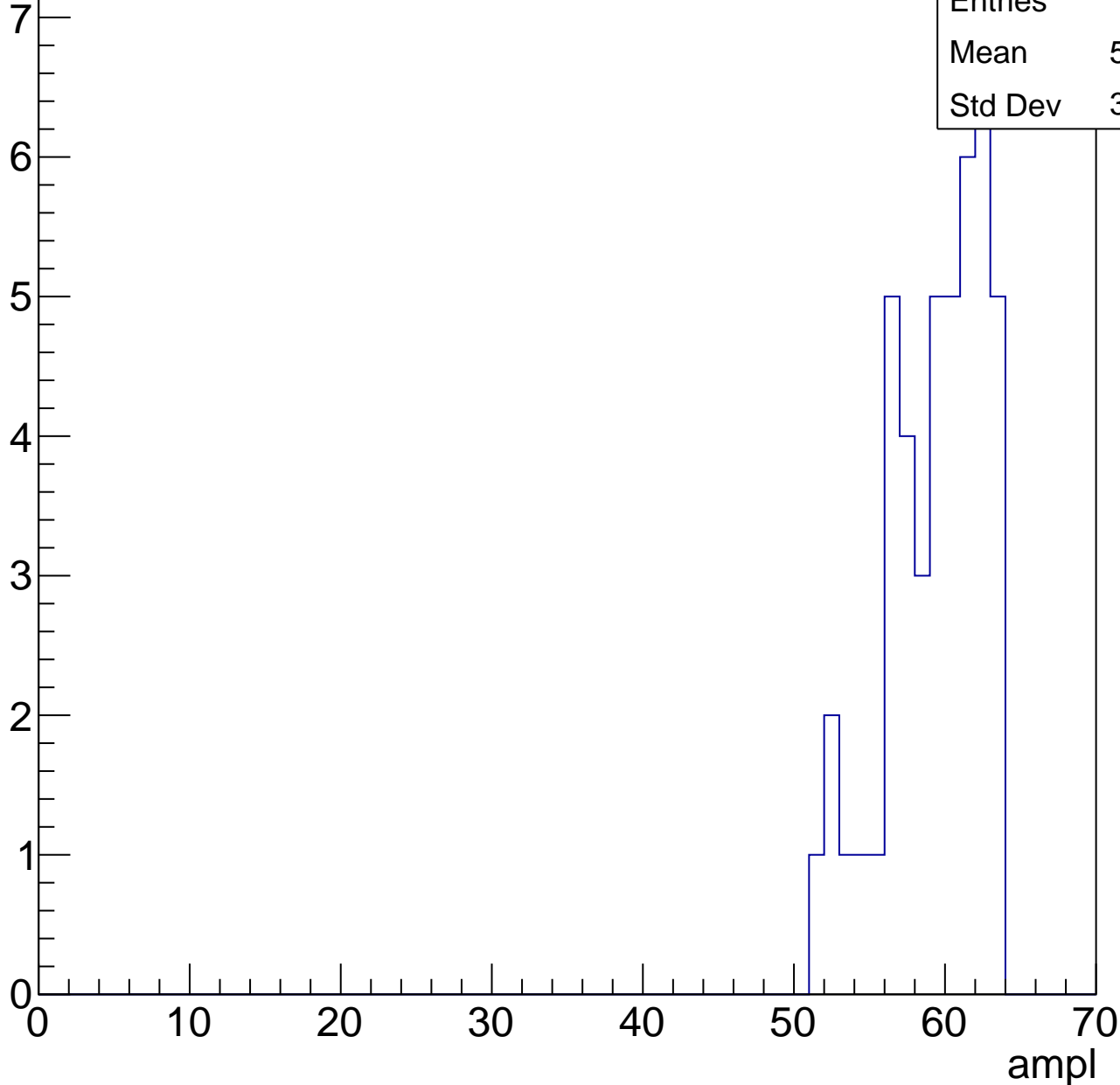


# B1L103S, U26-ch46, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	46
Mean	58.89
Std Dev	3.212

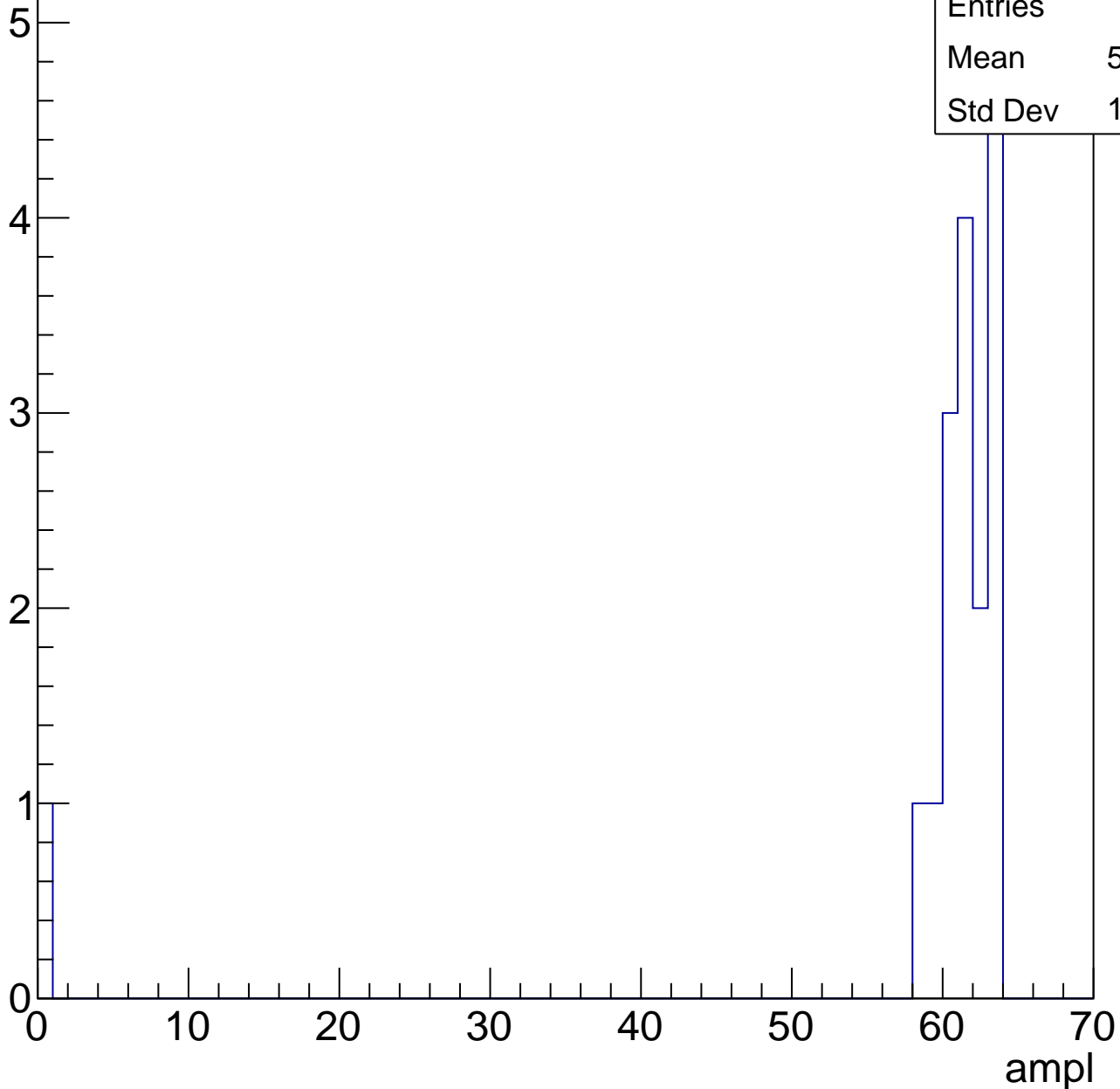


# B1L103S, U26-ch46, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	17
Mean	57.65
Std Dev	14.49



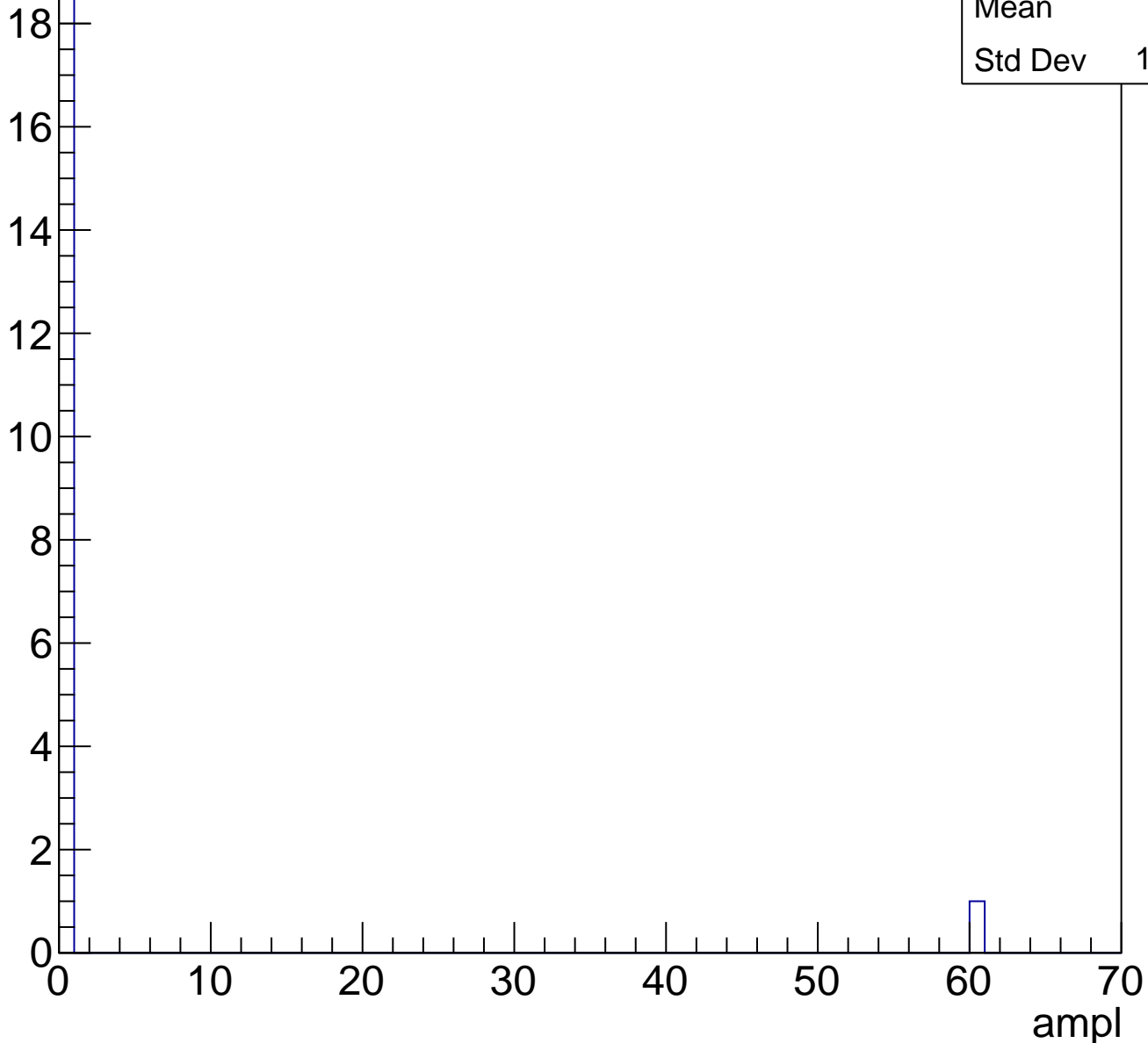


# B1L103S, U26-ch46, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	20
Mean	3
Std Dev	13.08

Entry



# B1L103S, U26-ch47, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	112
Mean	22.26
Std Dev	12.66

**Gaus mean : 29.3814**

**Gaus Width: 3.7327**

Entry

25

20

15

10

5

0

0

10

20

30

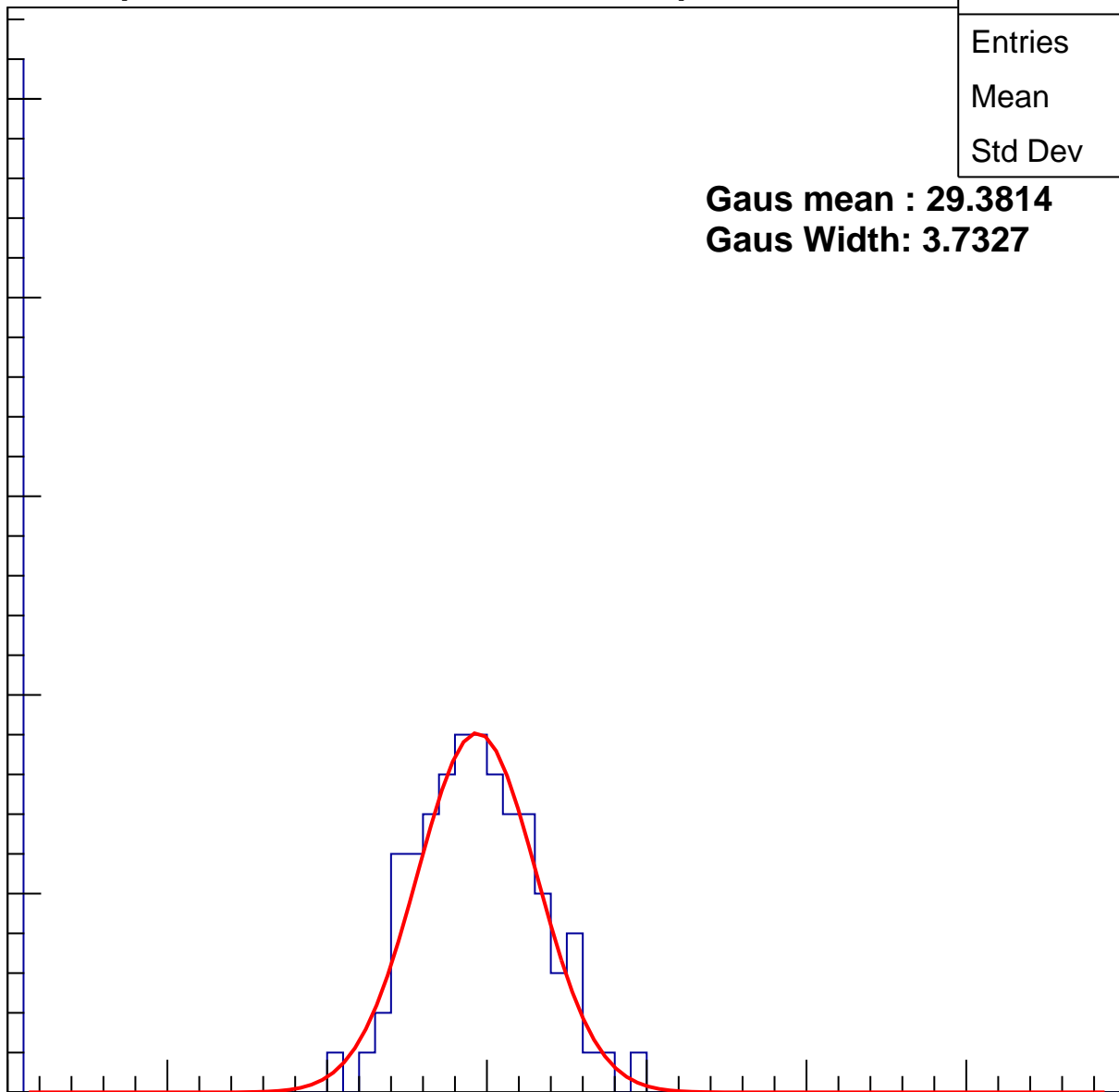
40

50

60

70

ampl



# B1L103S, U26-ch47, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	79
Mean	34.27
Std Dev	9.552

**Gaus mean : 37.4561**

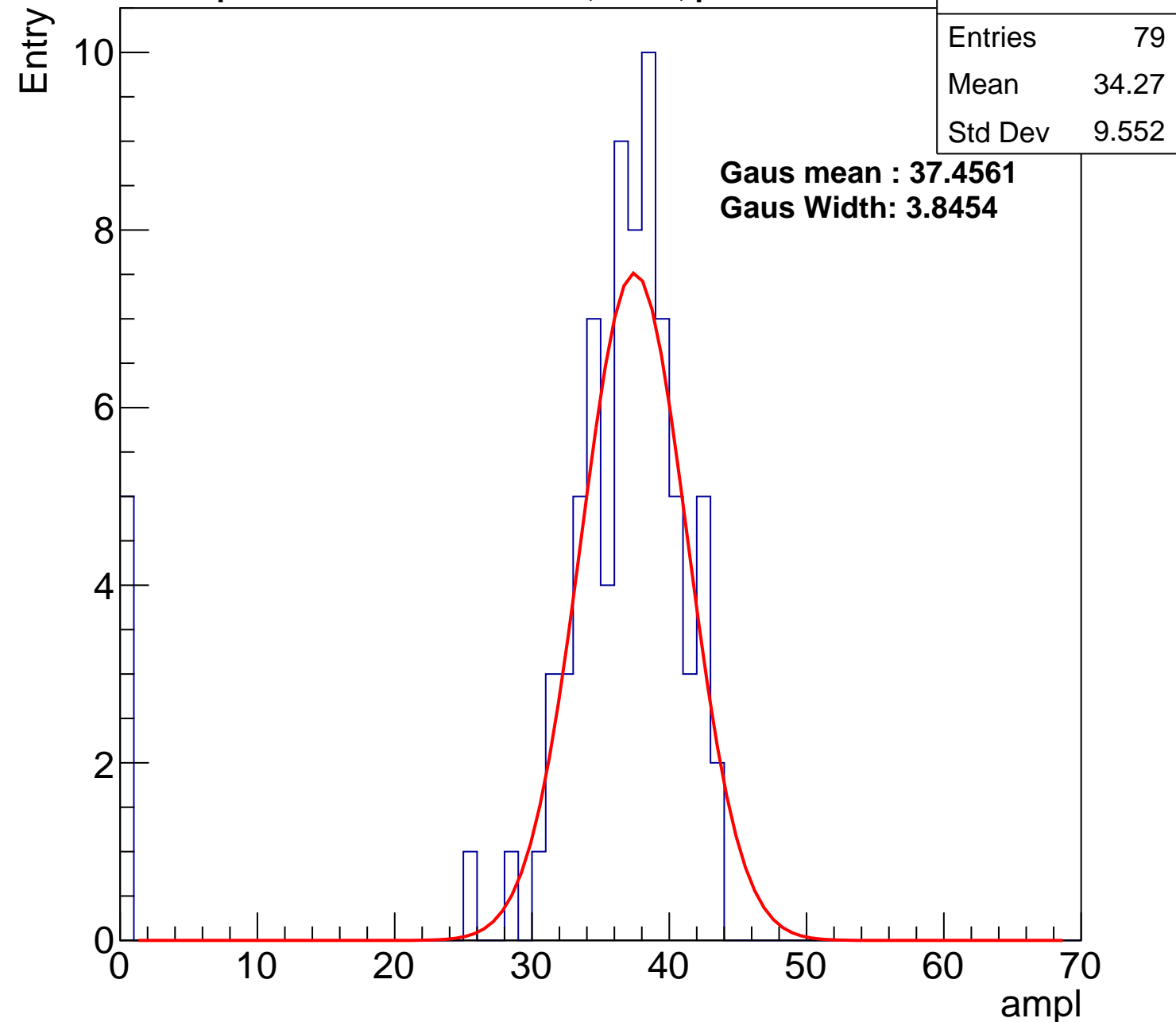
**Gaus Width: 3.8454**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U26-ch47, adc2

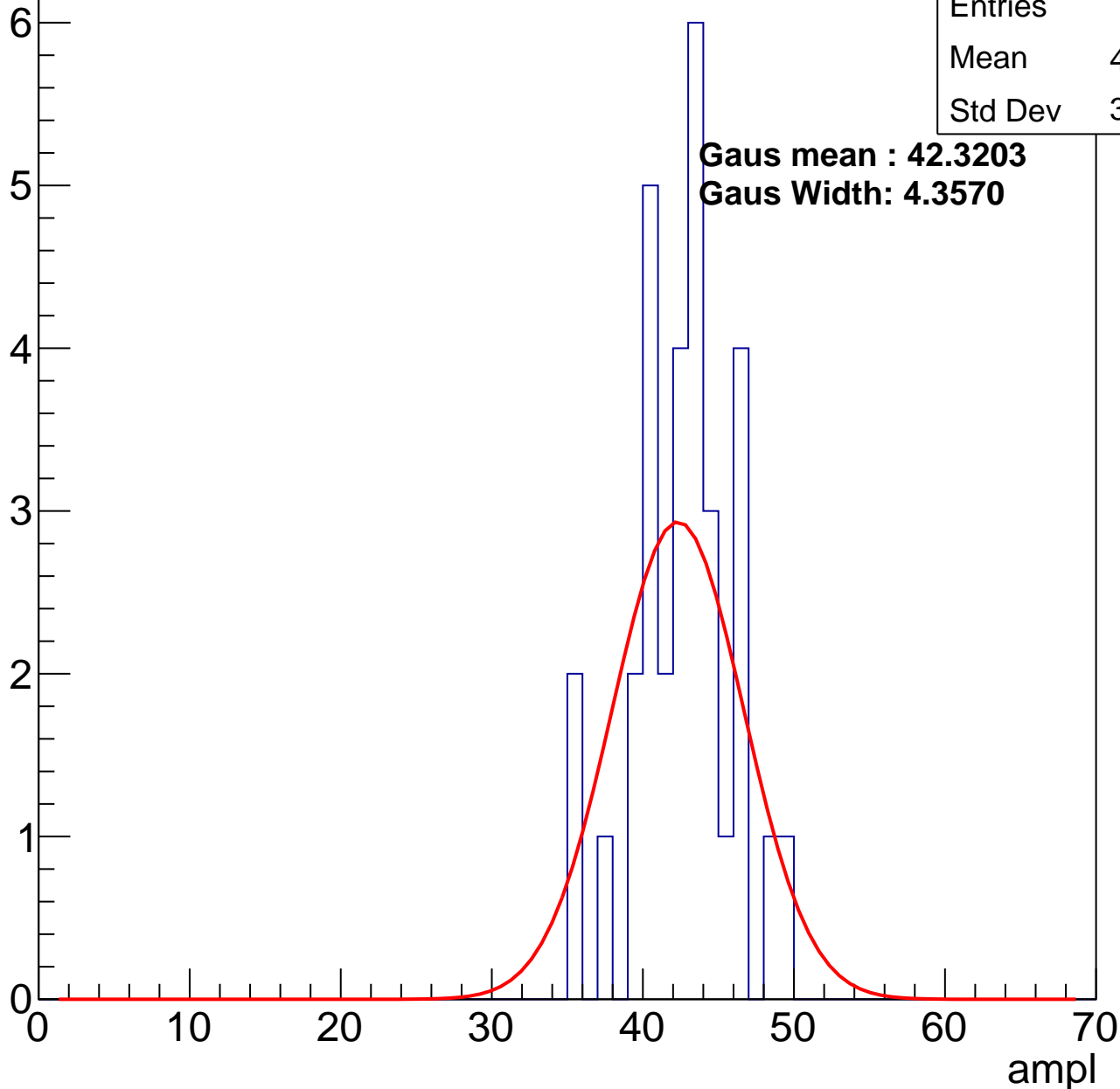
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	32
Mean	42.22
Std Dev	3.247

**Gaus mean : 42.3203**

**Gaus Width: 4.3570**

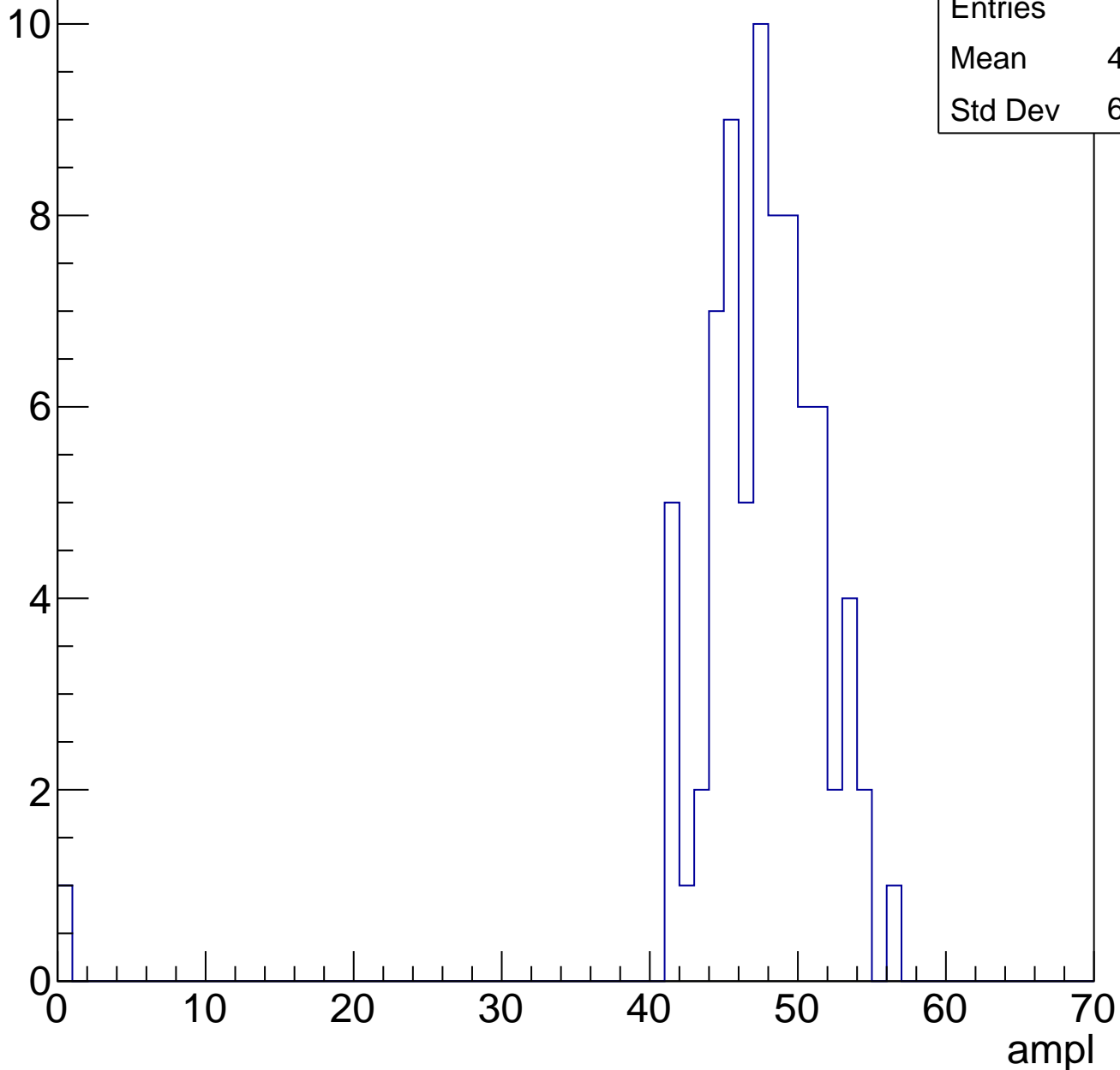


# B1L103S, U26-ch47, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	77
Mean	46.86
Std Dev	6.357

Entry

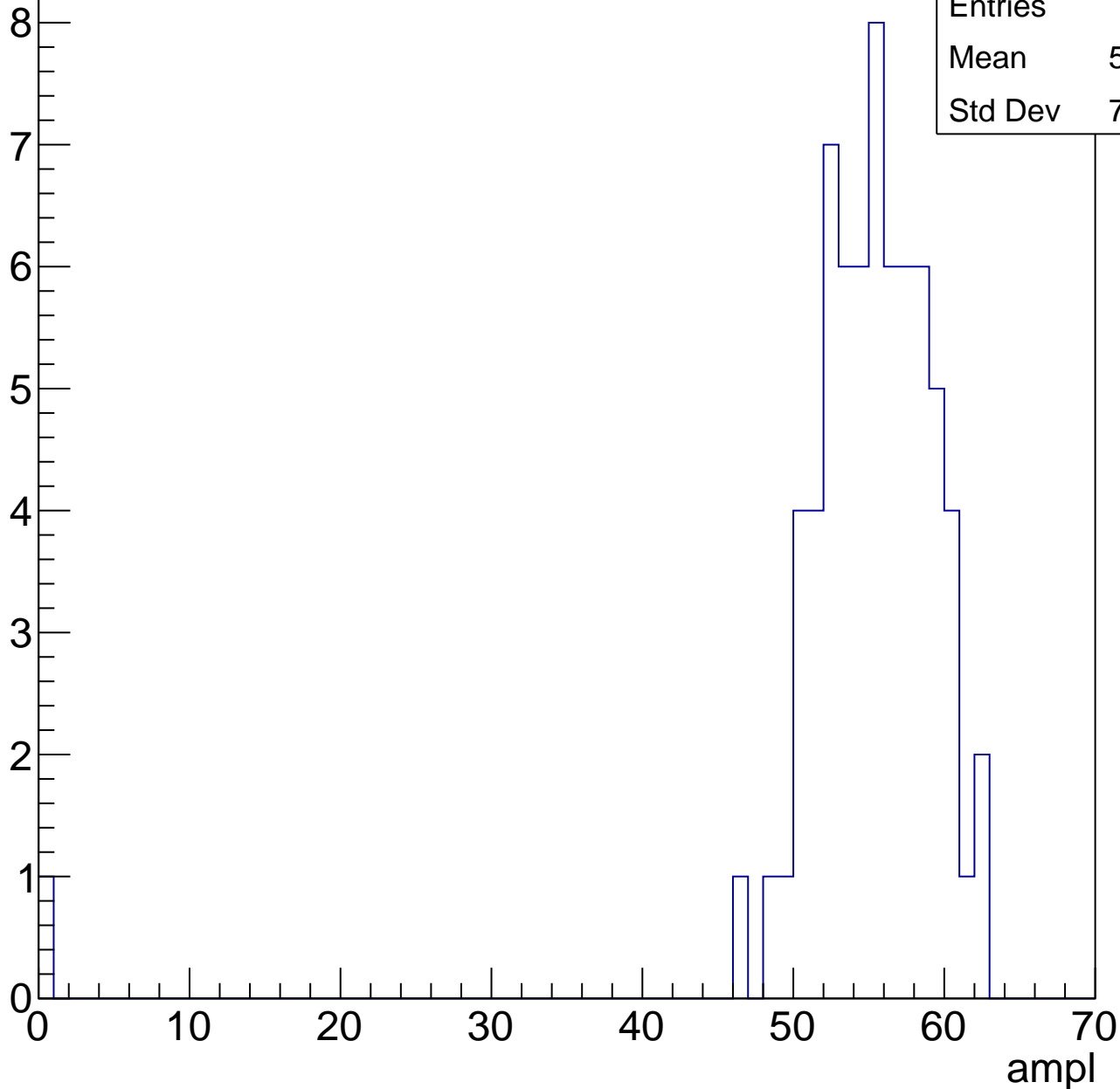


# B1L103S, U26-ch47, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	69
Mean	54.19
Std Dev	7.422

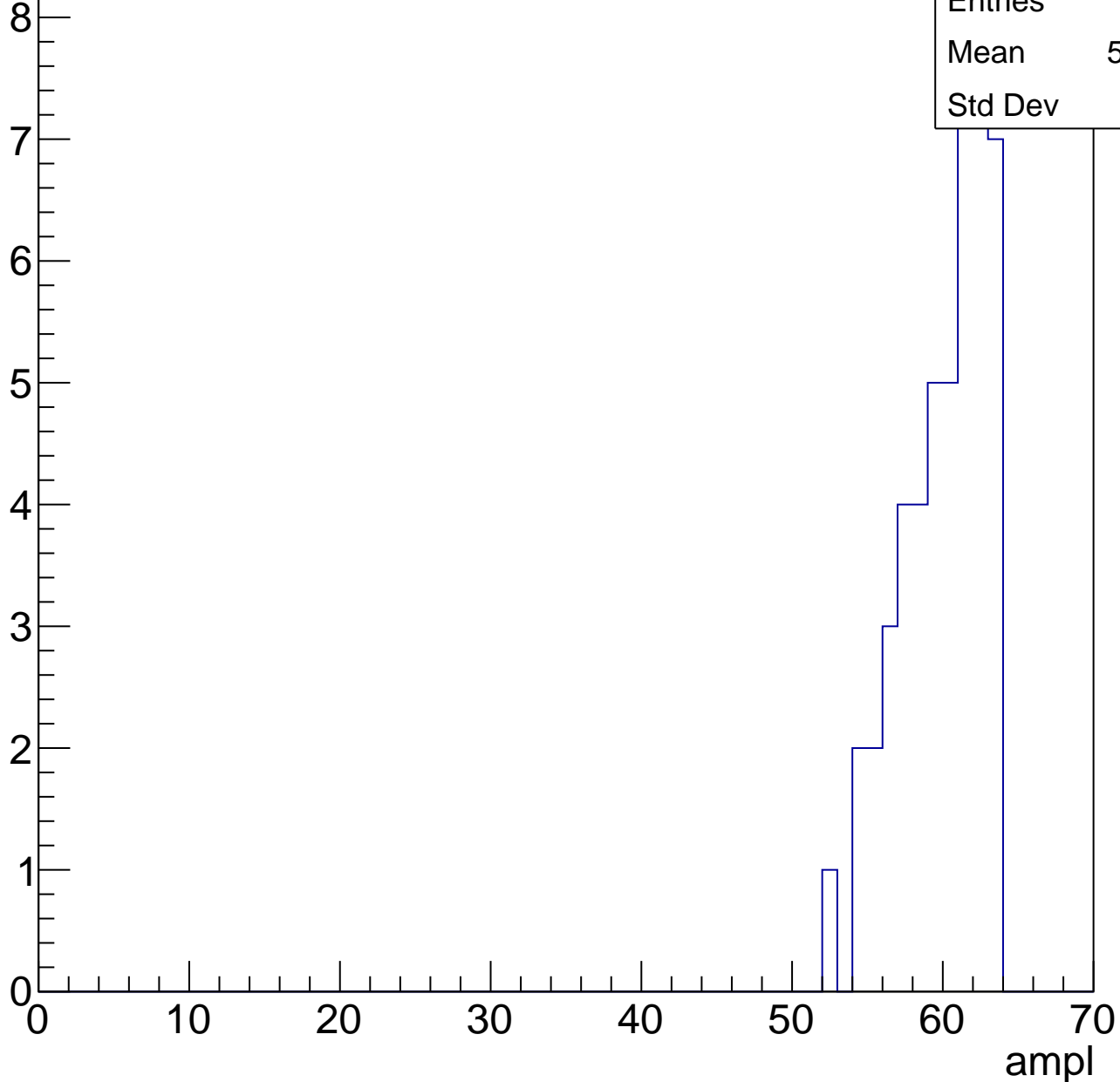


# B1L103S, U26-ch47, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	49
Mean	59.55
Std Dev	2.8



# B1L103S, U26-ch47, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

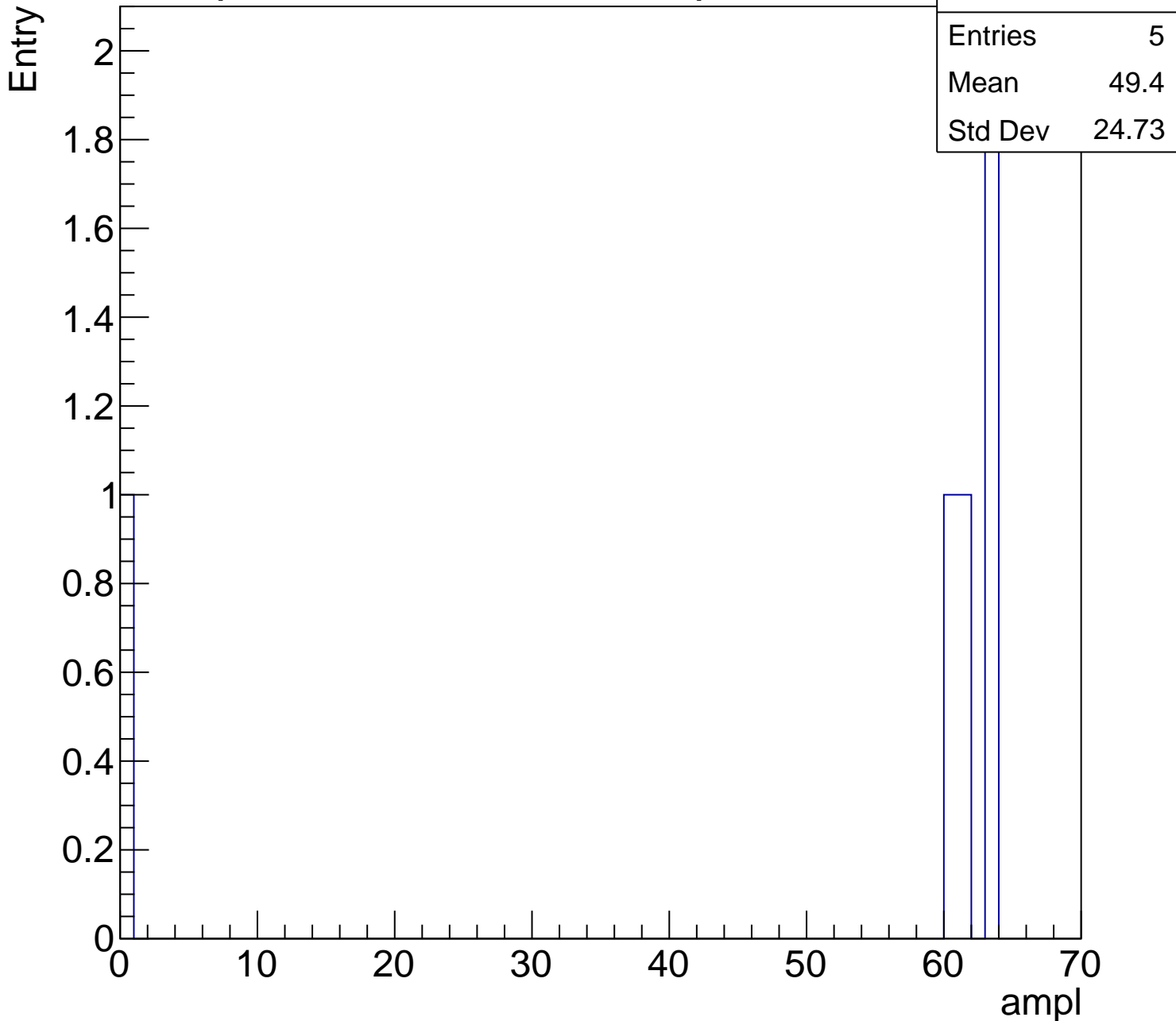
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	5
Mean	49.4
Std Dev	24.73

0 10 20 30 40 50 60 70

ampl





# B1L103S, U26-ch47, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	19
Mean	3.316
Std Dev	14.07

Entry



# B1L103S, U26-ch48, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	95
Mean	24.37
Std Dev	10.32

**Gaus mean : 28.8813**

**Gaus Width: 3.6614**

Entry

12

10

8

6

4

2

0

0

10

20

30

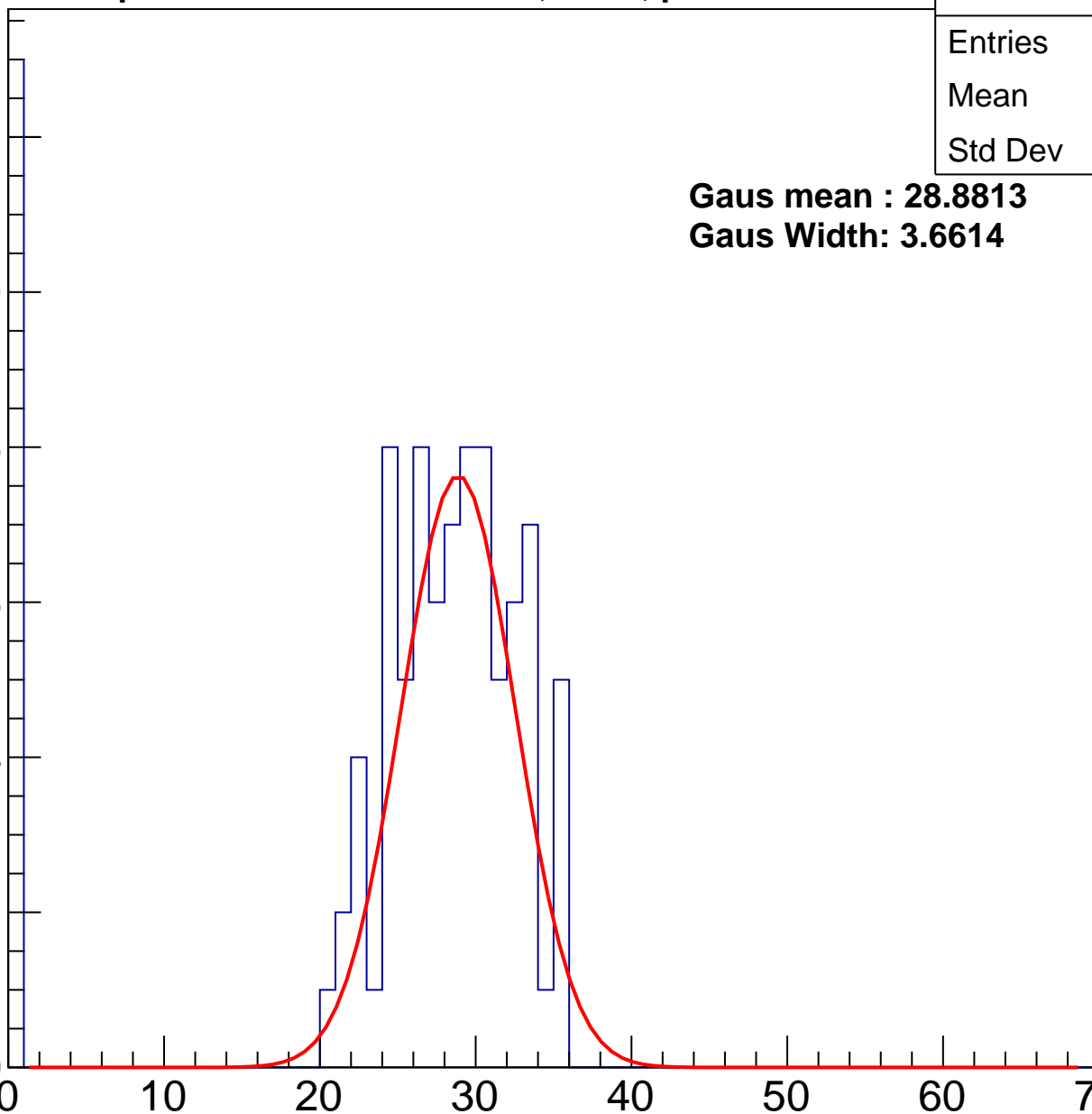
40

50

60

70

ampl



# B1L103S, U26-ch48, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	84
Mean	31.25
Std Dev	12.59

**Gaus mean : 36.8473**

**Gaus Width: 3.7041**

Entry

10

8

6

4

2

0

0

10

20

30

40

50

60

70

ampl

0

2

4

6

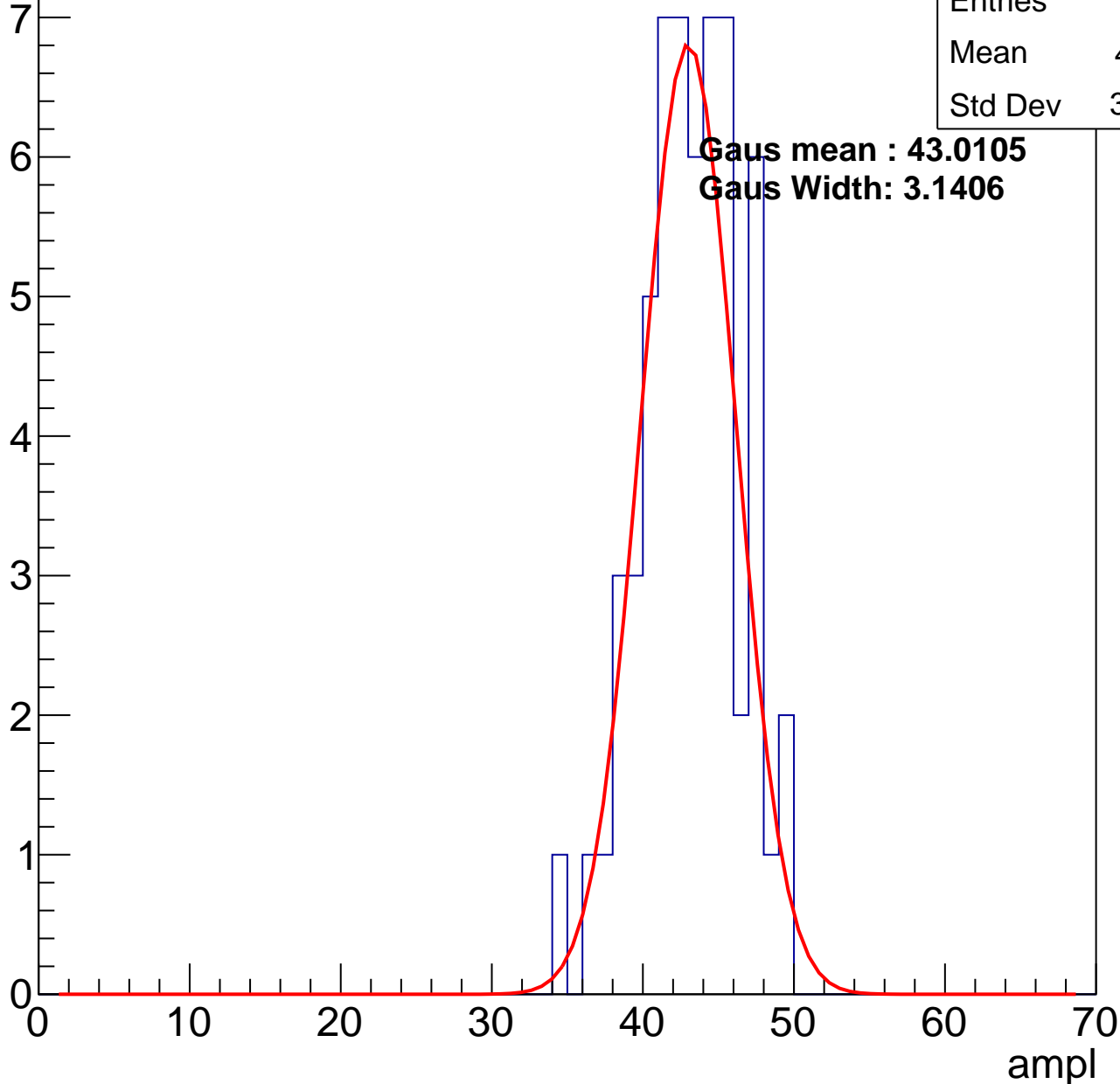
8

10

# B1L103S, U26-ch48, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

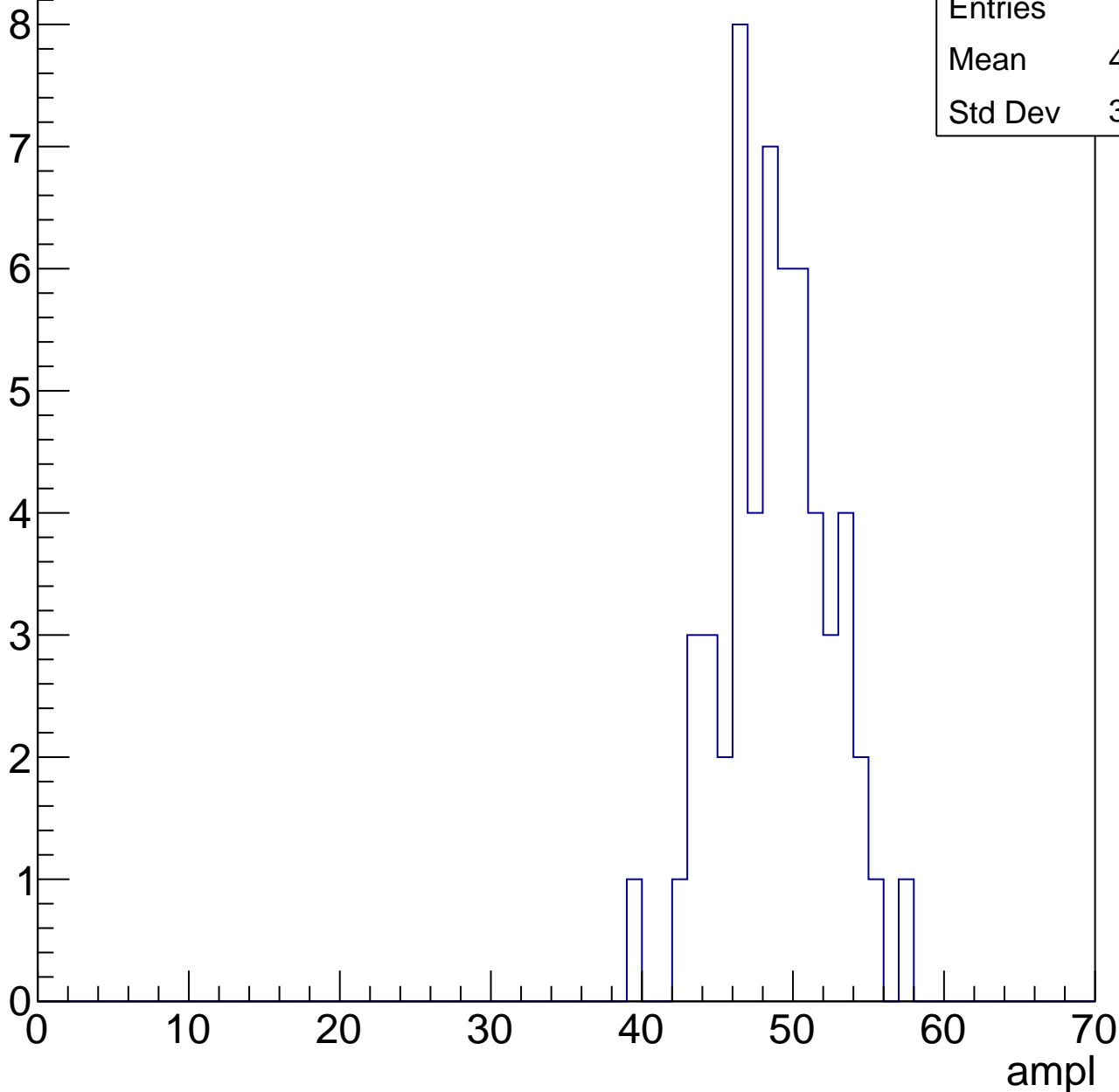


# B1L103S, U26-ch48, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	56
Mean	48.39
Std Dev	3.539

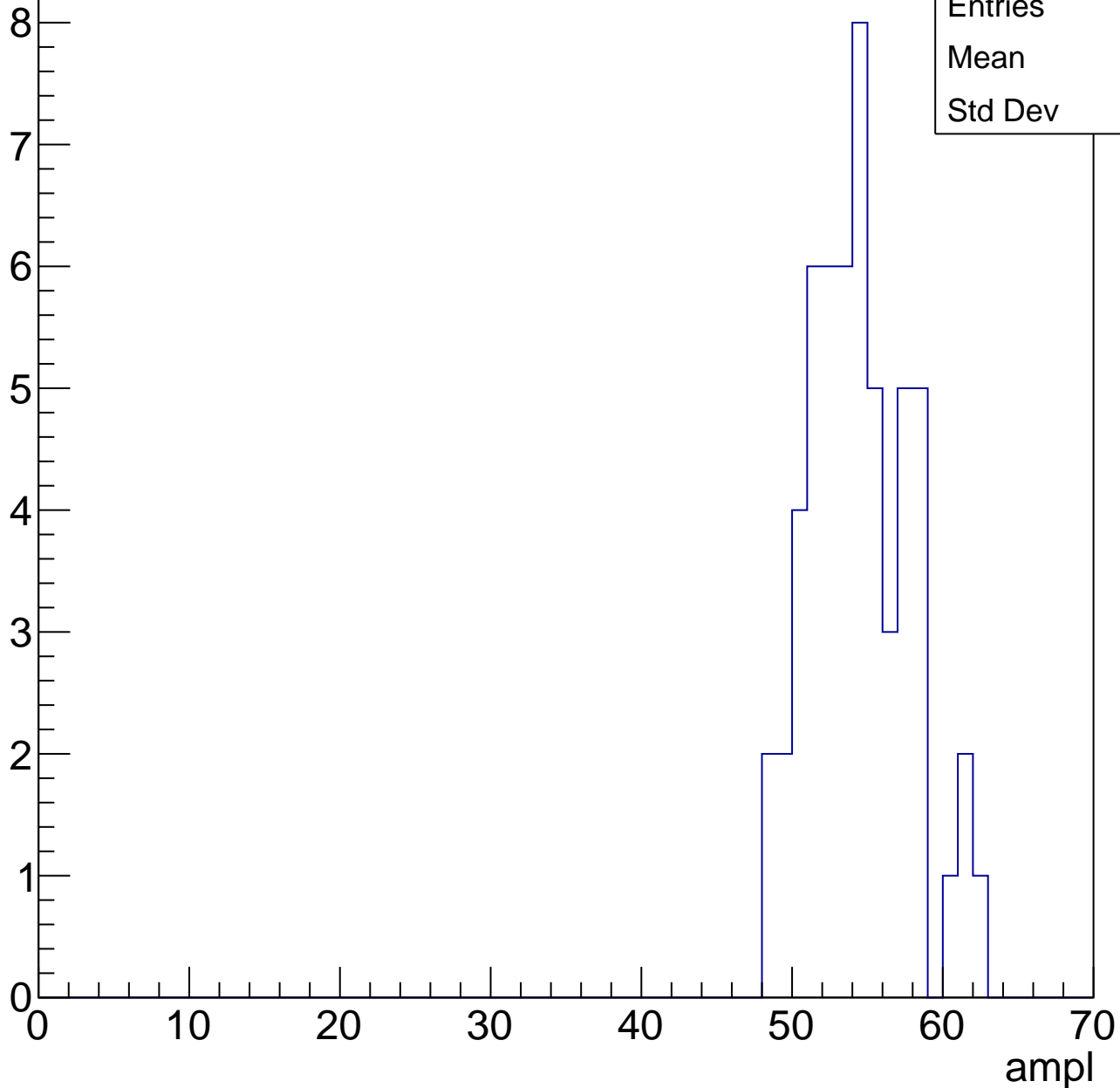


# B1L103S, U26-ch48, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	56
Mean	54
Std Dev	3.3

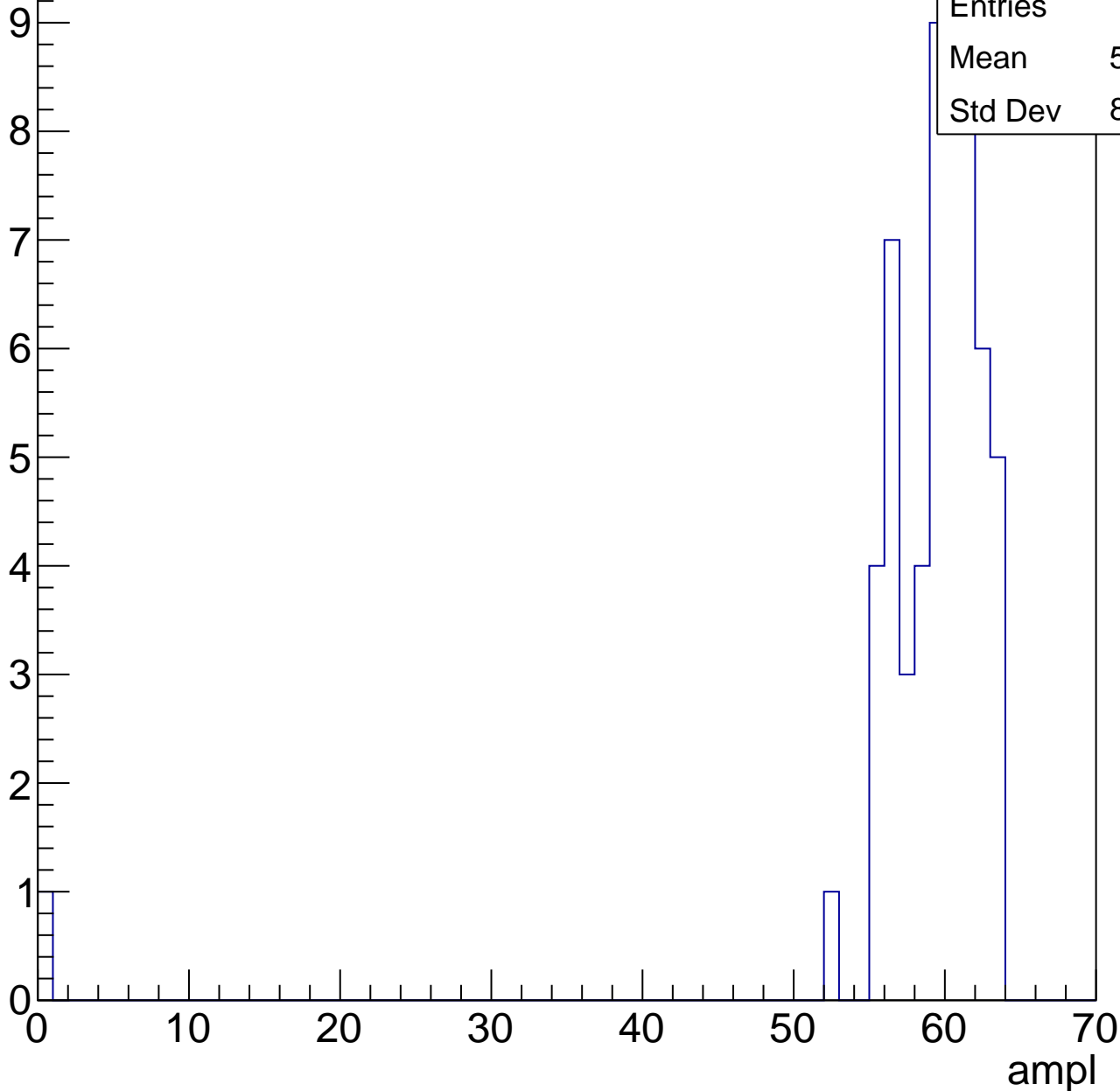


# B1L103S, U26-ch48, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	56
Mean	58.09
Std Dev	8.238

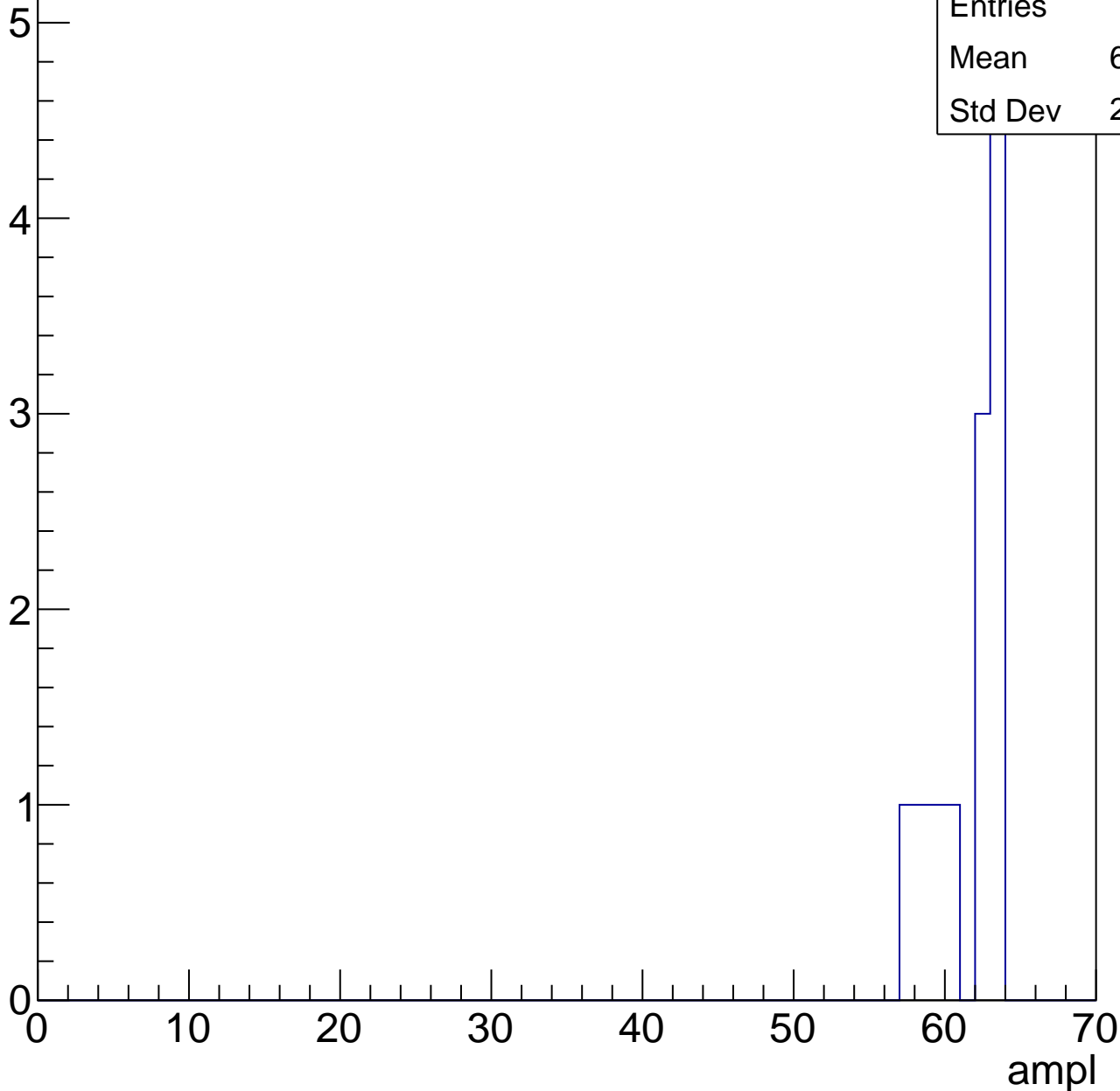


# B1L103S, U26-ch48, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	12
Mean	61.25
Std Dev	2.087





# B1L103S, U26-ch48, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

18  
16  
14  
12  
10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

Entries	19
Mean	0
Std Dev	0

# B1L103S, U26-ch49, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	87
Mean	24.71
Std Dev	9.953

**Gaus mean : 29.0403**

**Gaus Width: 3.7698**

Entry

10

8

6

4

2

0

0

10

20

30

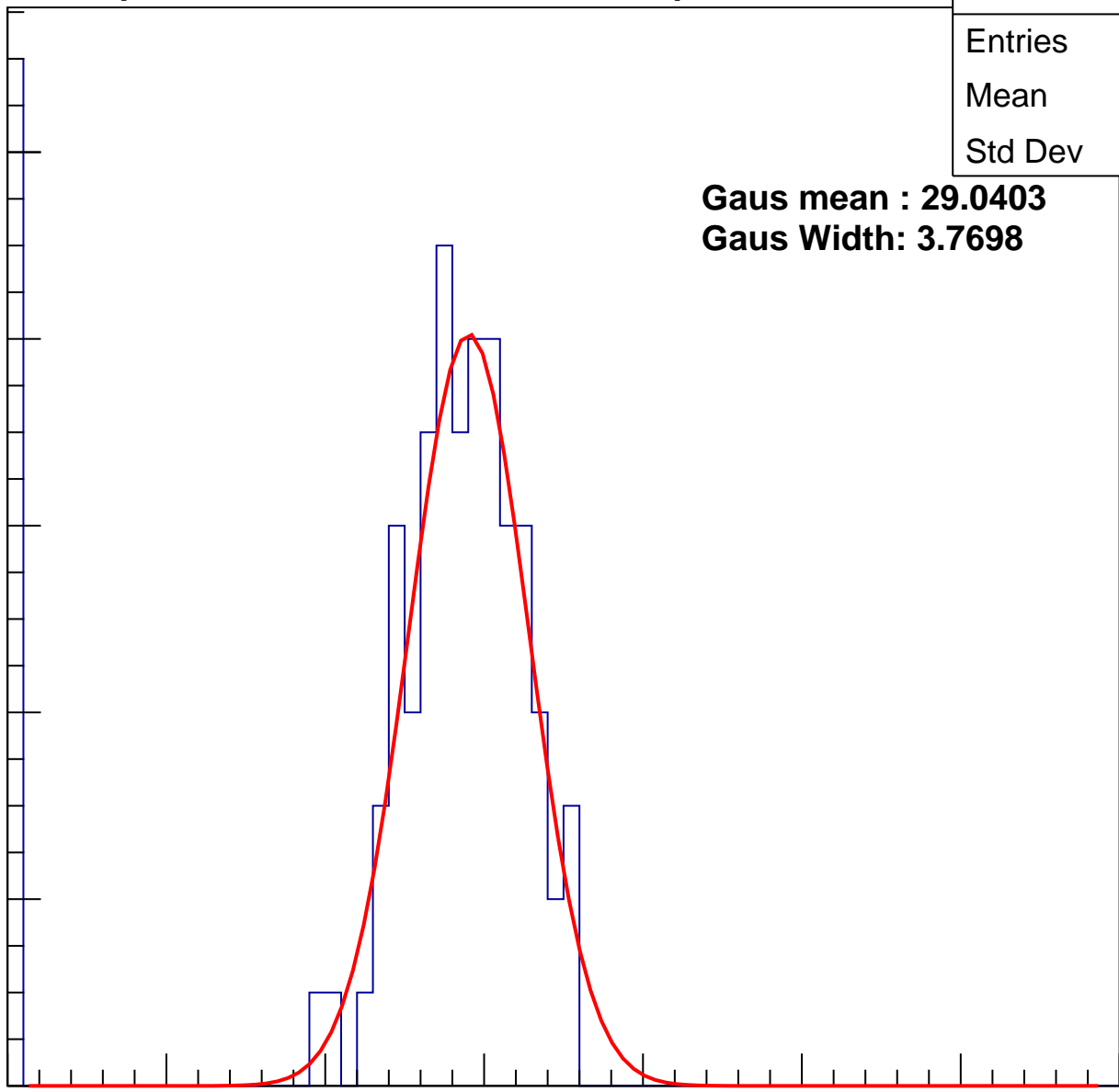
40

50

60

70

ampl



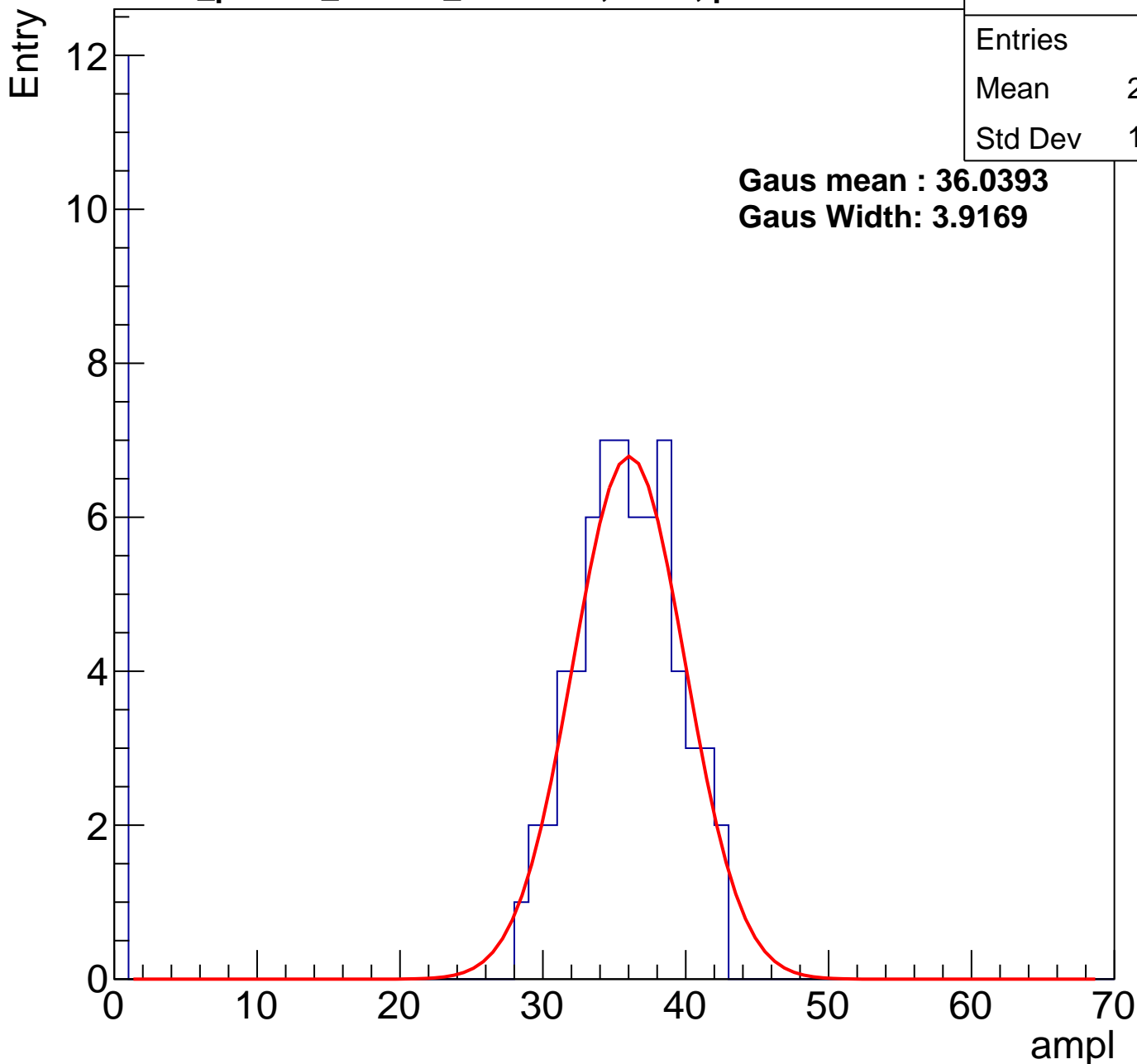
# B1L103S, U26-ch49, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	76
Mean	29.82
Std Dev	13.28

**Gaus mean : 36.0393**

**Gaus Width: 3.9169**



# B1L103S, U26-ch49, adc2

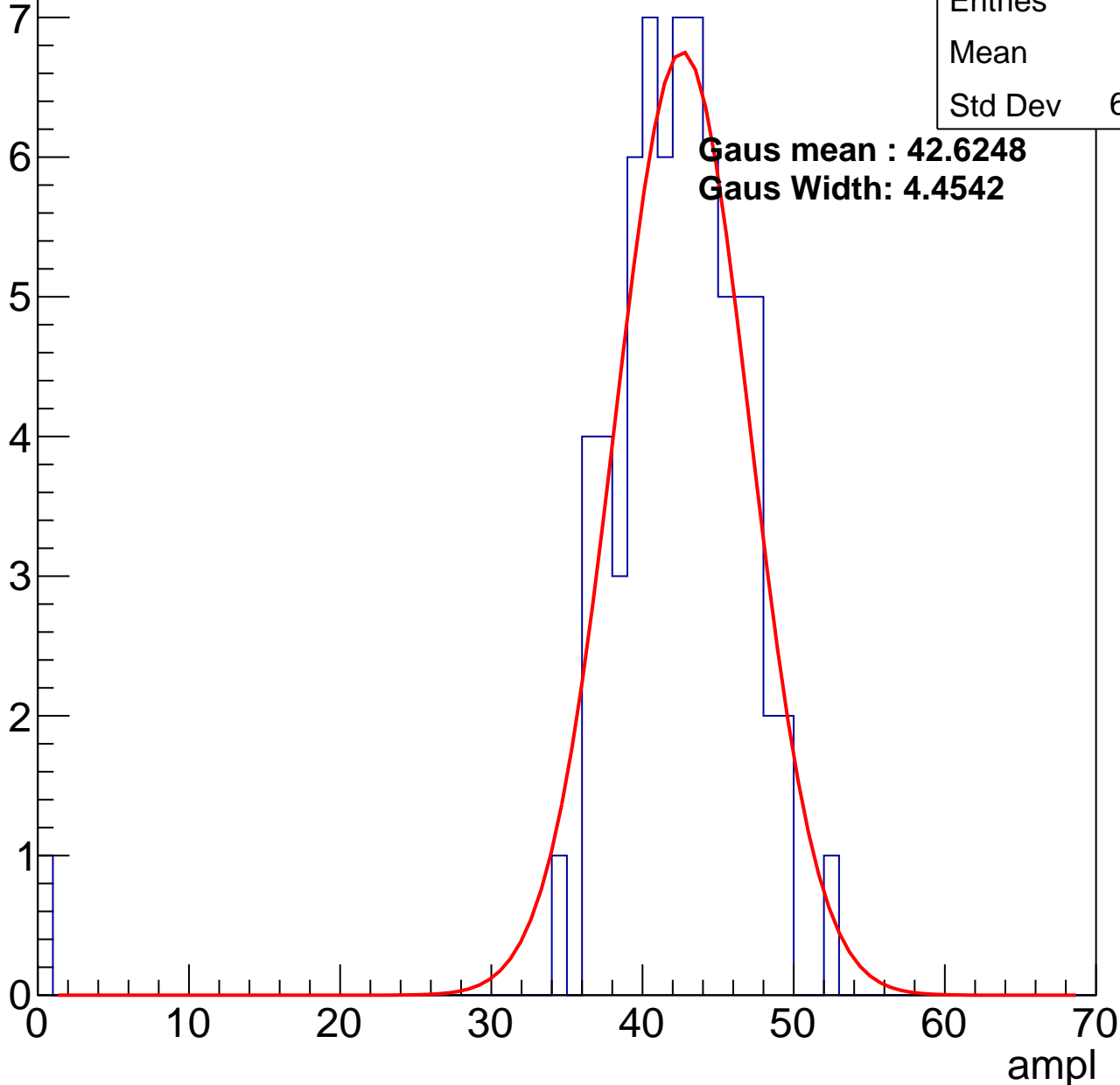
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	72
Mean	41.6
Std Dev	6.177

**Gaus mean : 42.6248**

**Gaus Width: 4.4542**

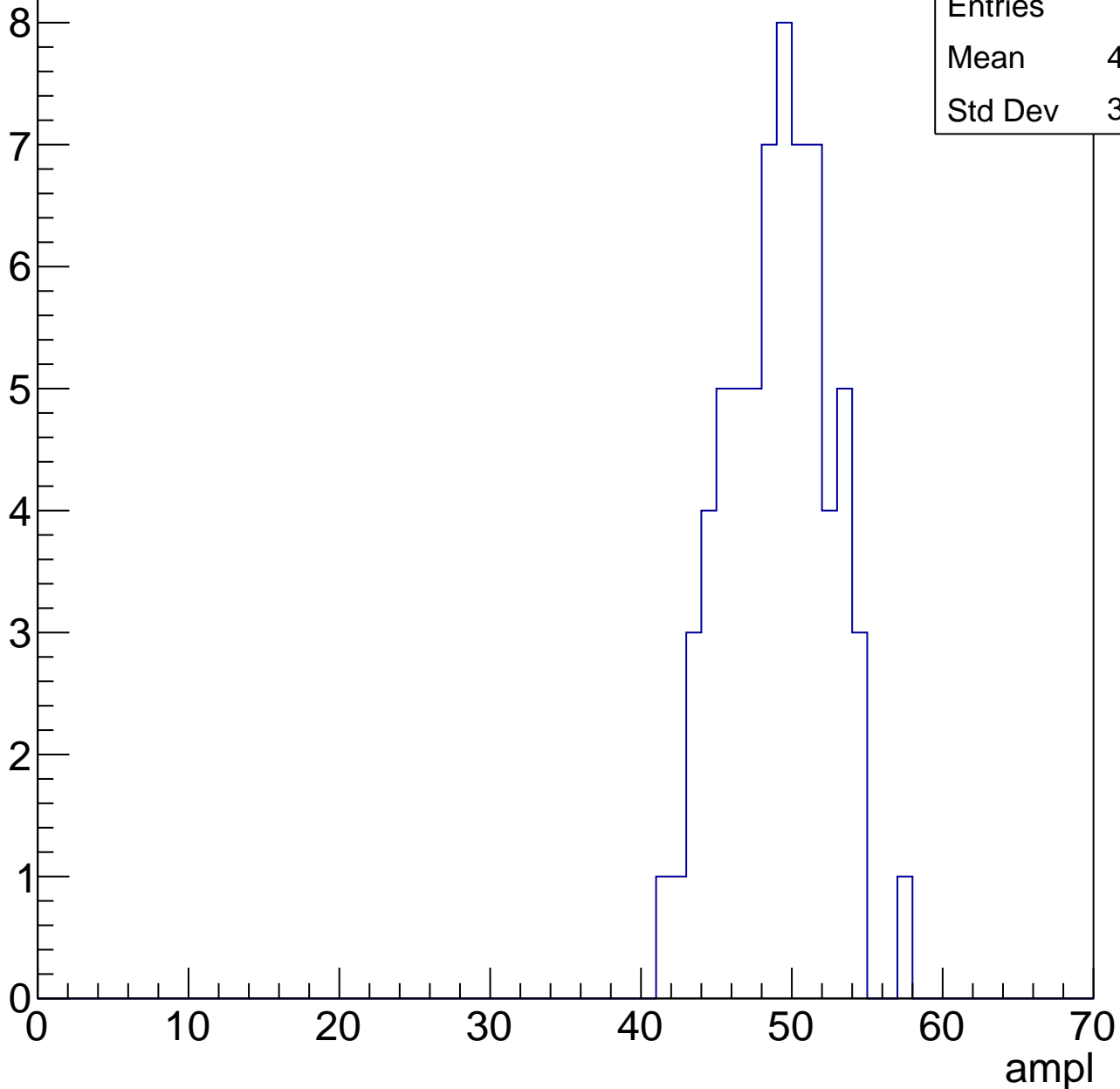


# B1L103S, U26-ch49, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

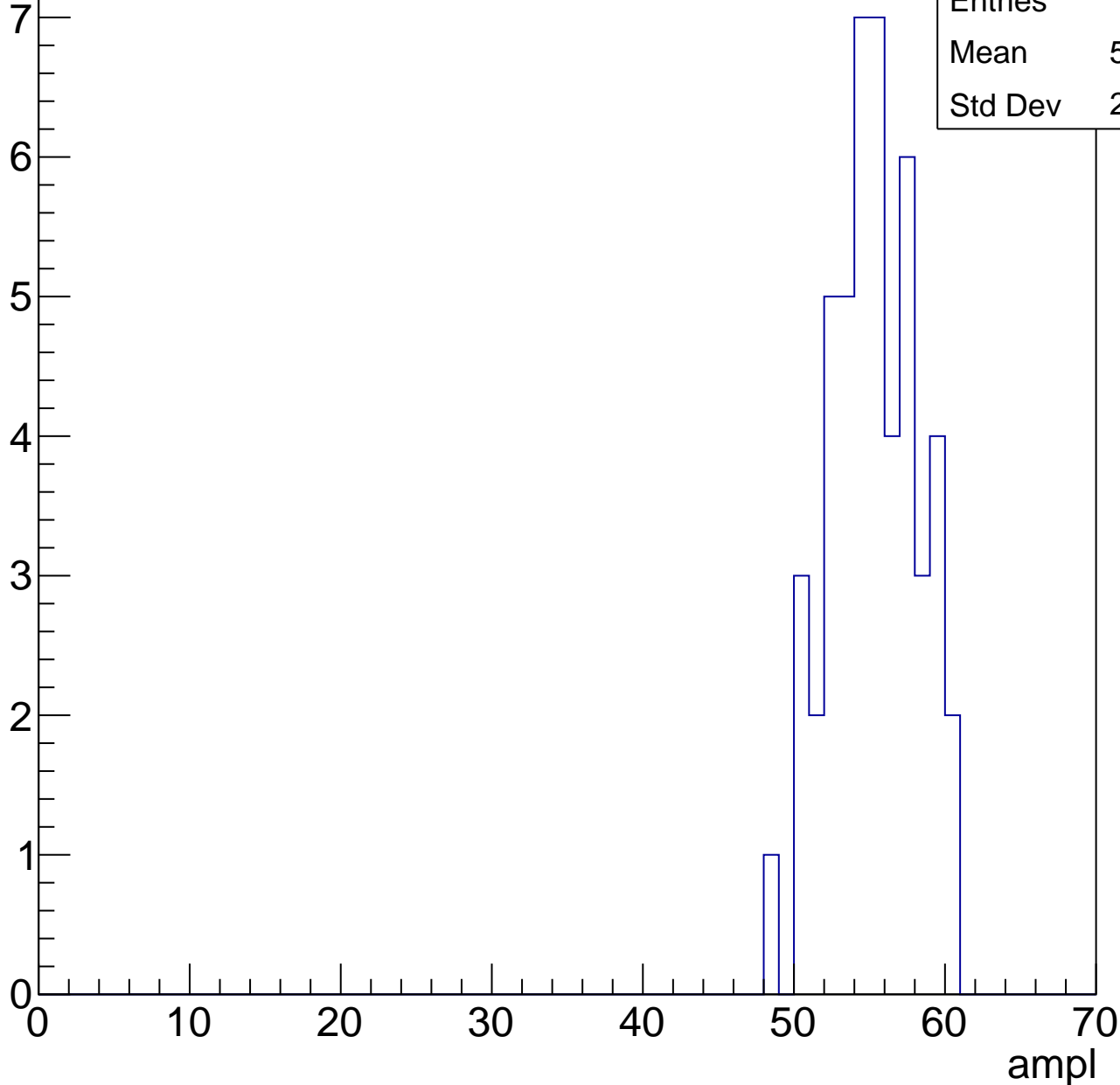
Entries	66
Mean	48.56
Std Dev	3.372



# B1L103S, U26-ch49, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

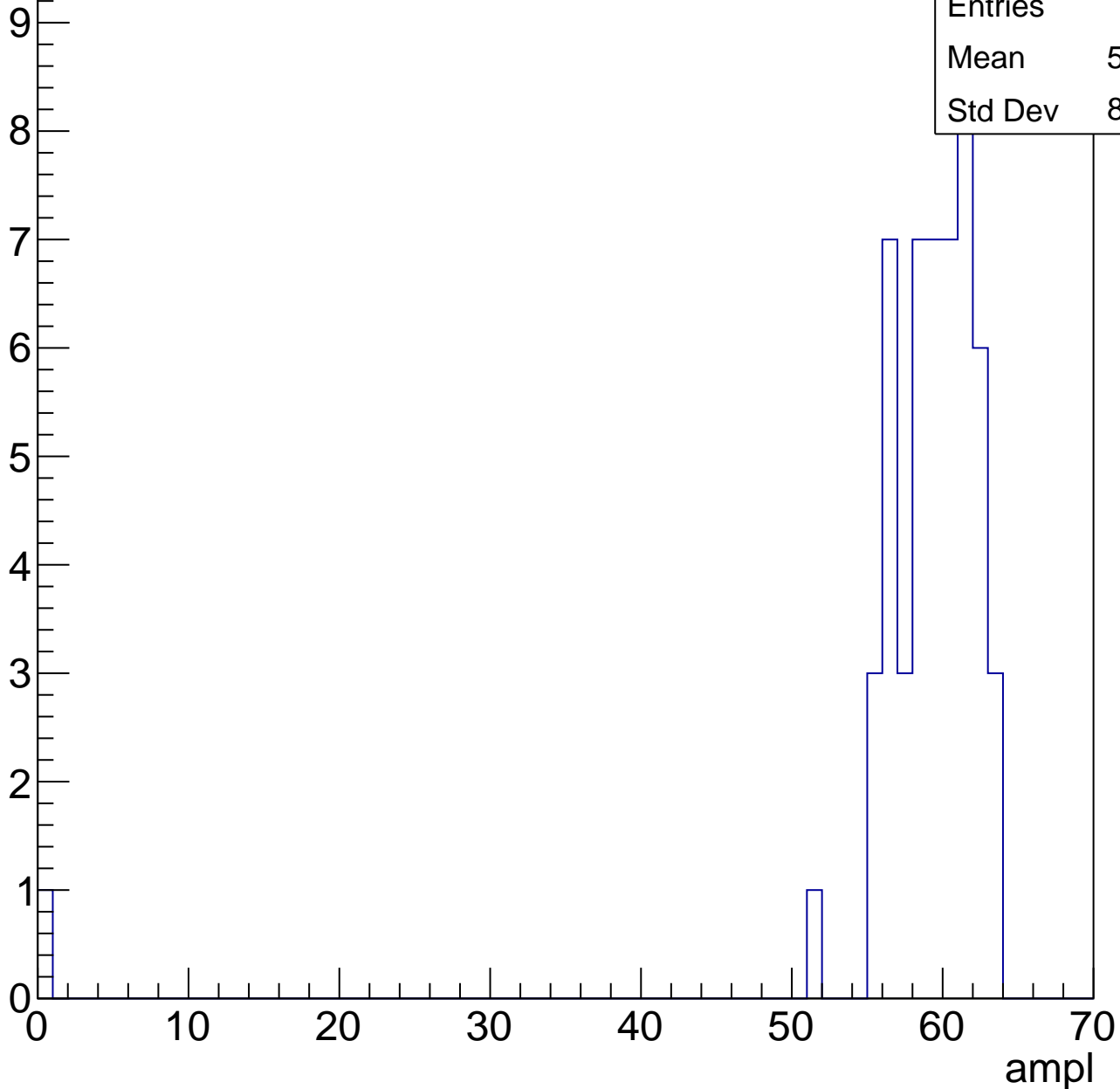


# B1L103S, U26-ch49, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	54
Mean	57.93
Std Dev	8.342

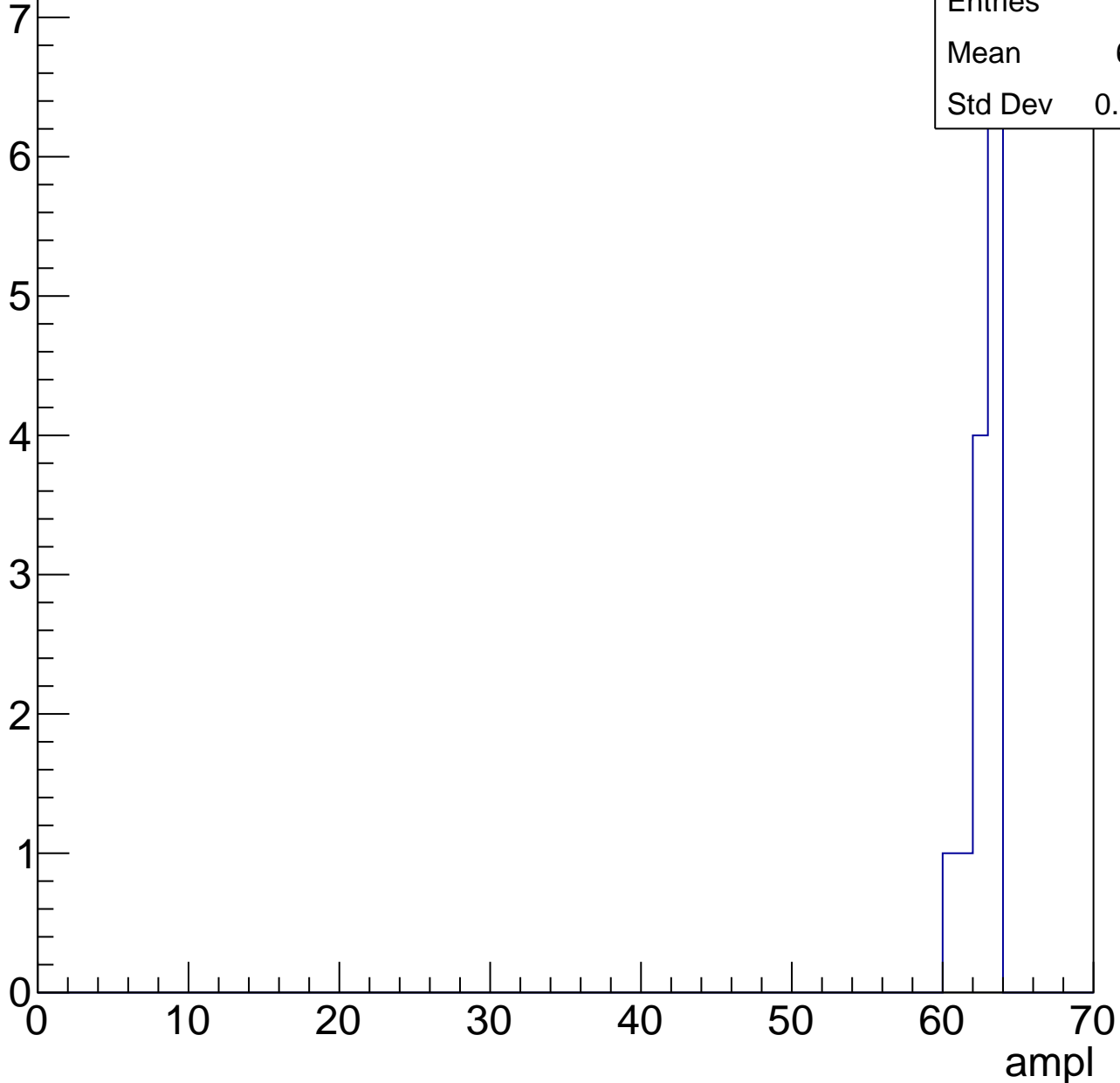


# B1L103S, U26-ch49, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	13
Mean	62.31
Std Dev	0.9102





# B1L103S, U26-ch49, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

18  
16  
14  
12  
10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

Entries	19
Mean	0
Std Dev	0

# B1L103S, U26-ch50, adc0

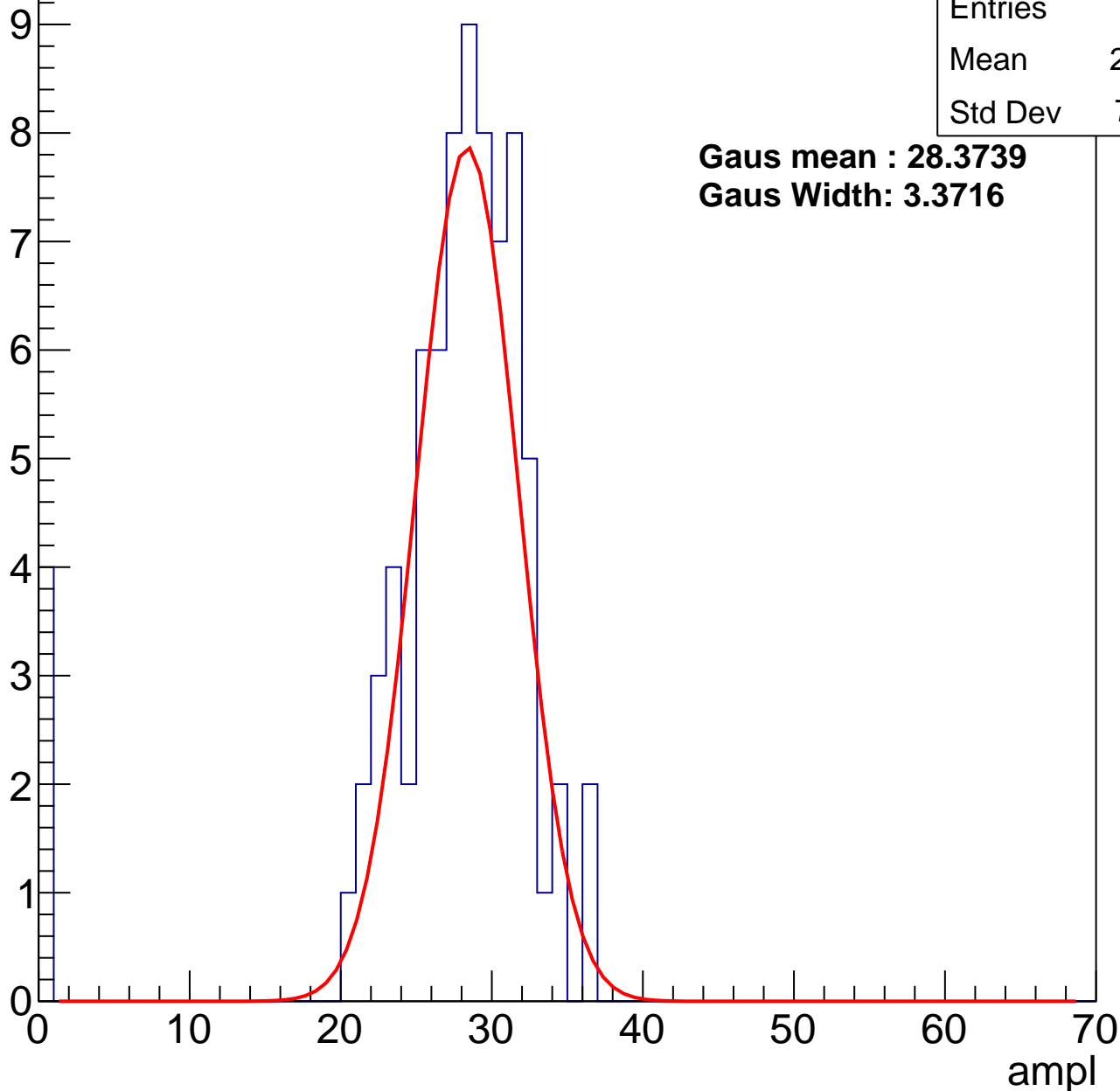
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	78
Mean	26.47
Std Dev	7.031

**Gaus mean : 28.3739**

**Gaus Width: 3.3716**



# B1L103S, U26-ch50, adc1

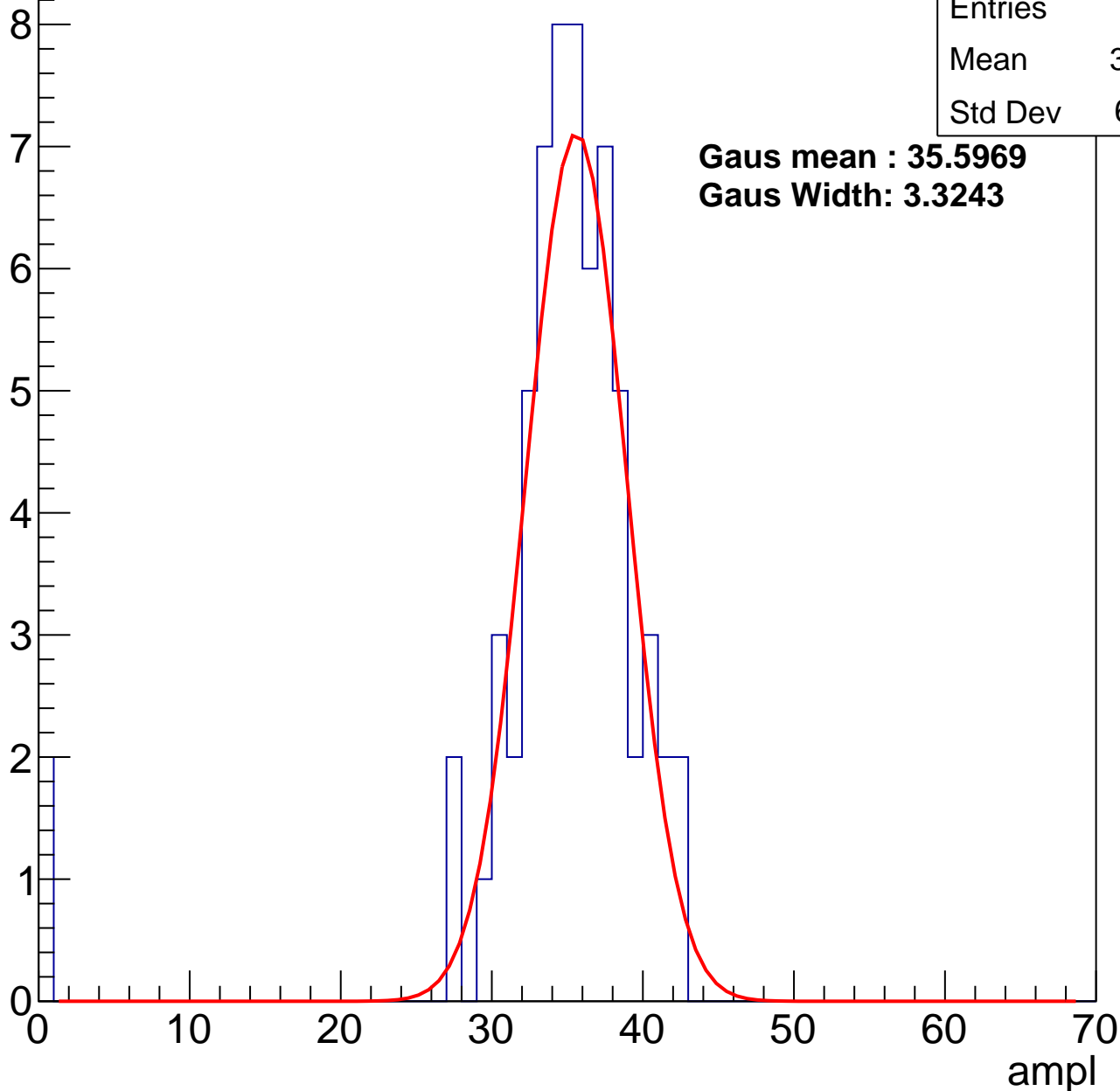
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	65
Mean	33.95
Std Dev	6.891

**Gaus mean : 35.5969**

**Gaus Width: 3.3243**



# B1L103S, U26-ch50, adc2

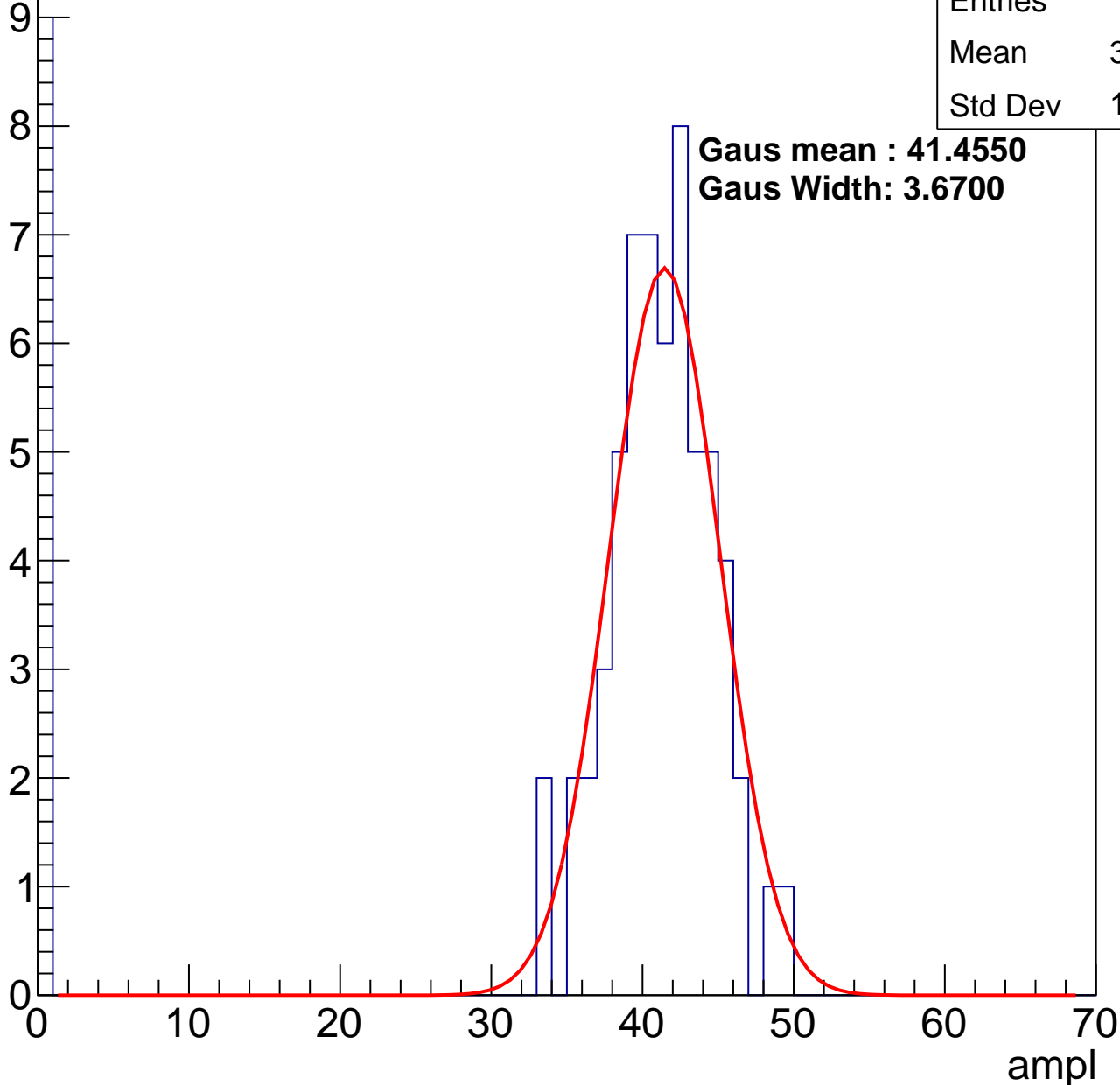
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	69
Mean	35.48
Std Dev	14.09

**Gaus mean : 41.4550**

**Gaus Width: 3.6700**

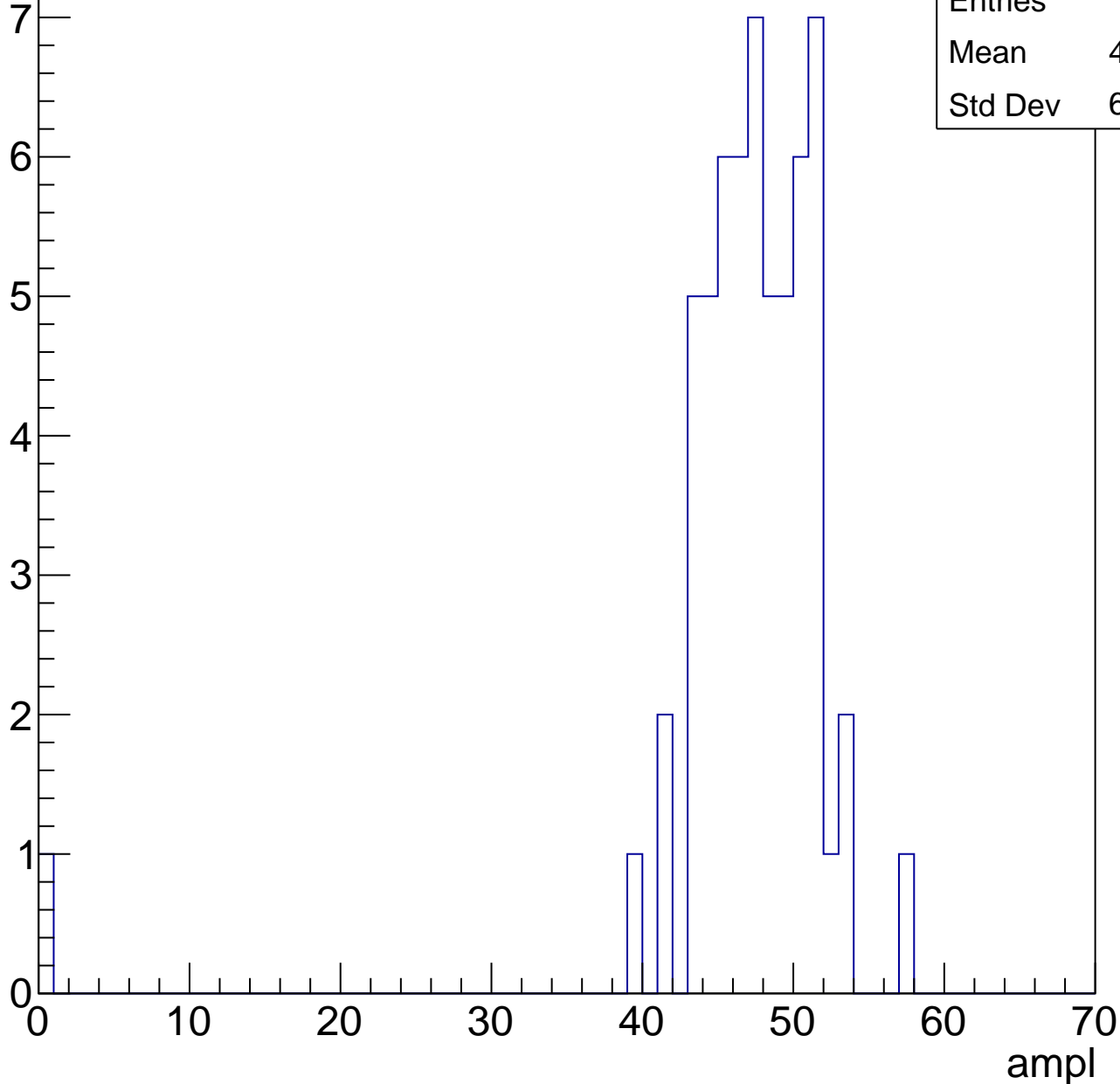


# B1L103S, U26-ch50, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

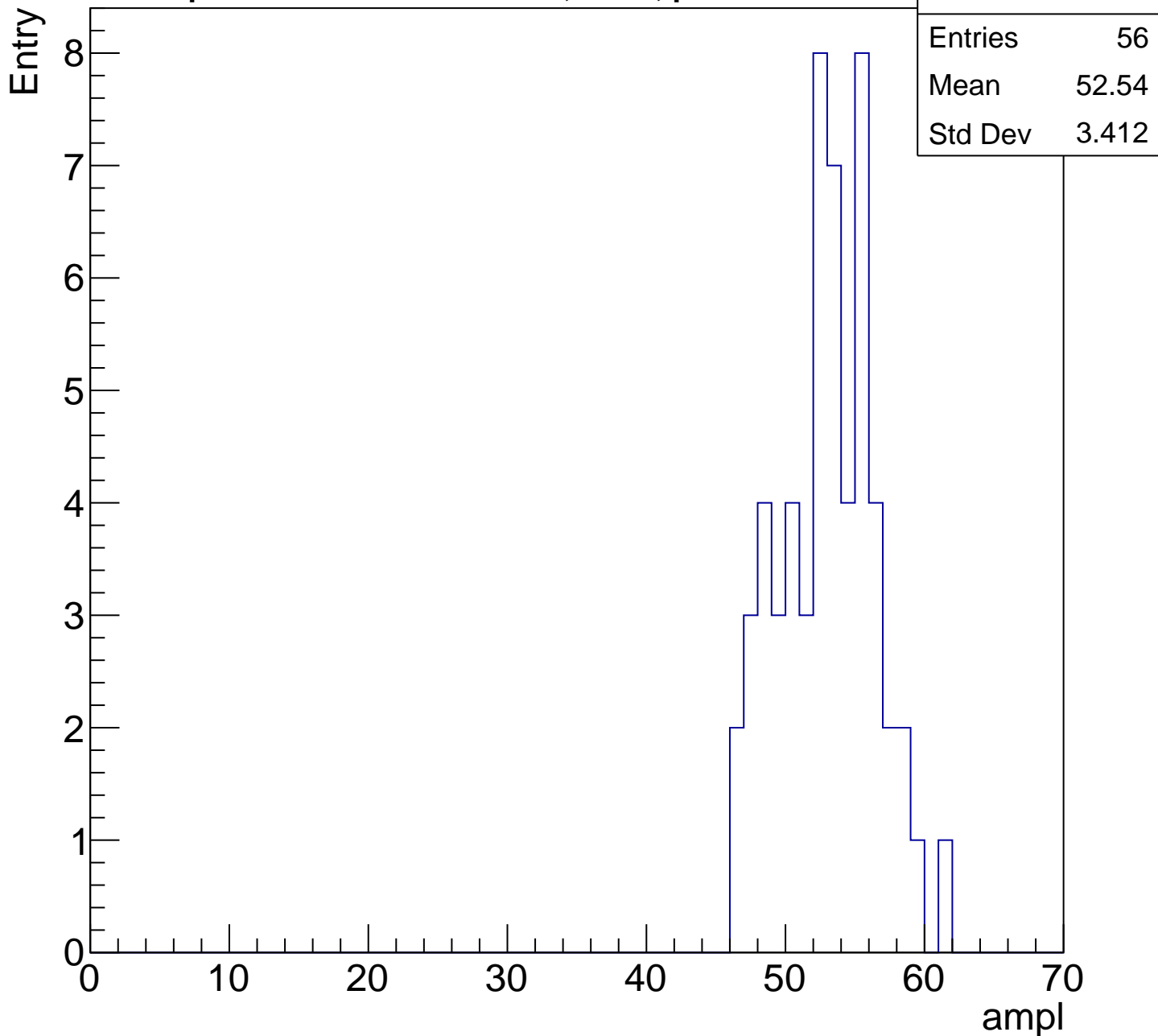
Entry

Entries	60
Mean	46.47
Std Dev	6.917



# B1L103S, U26-ch50, adc4

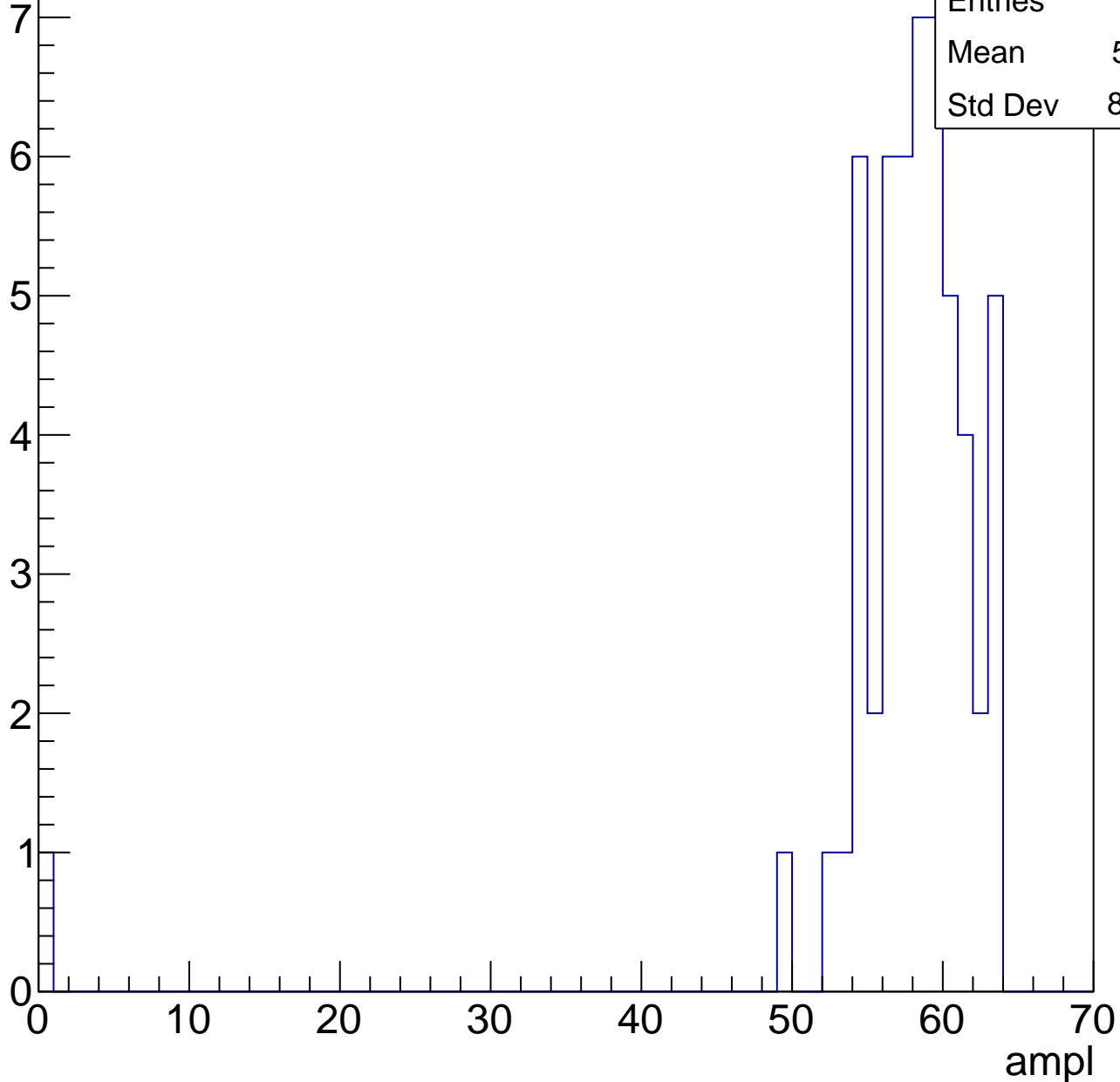
calib\_packv5\_041523\_1651.root, FC#0, port C2



# B1L103S, U26-ch50, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

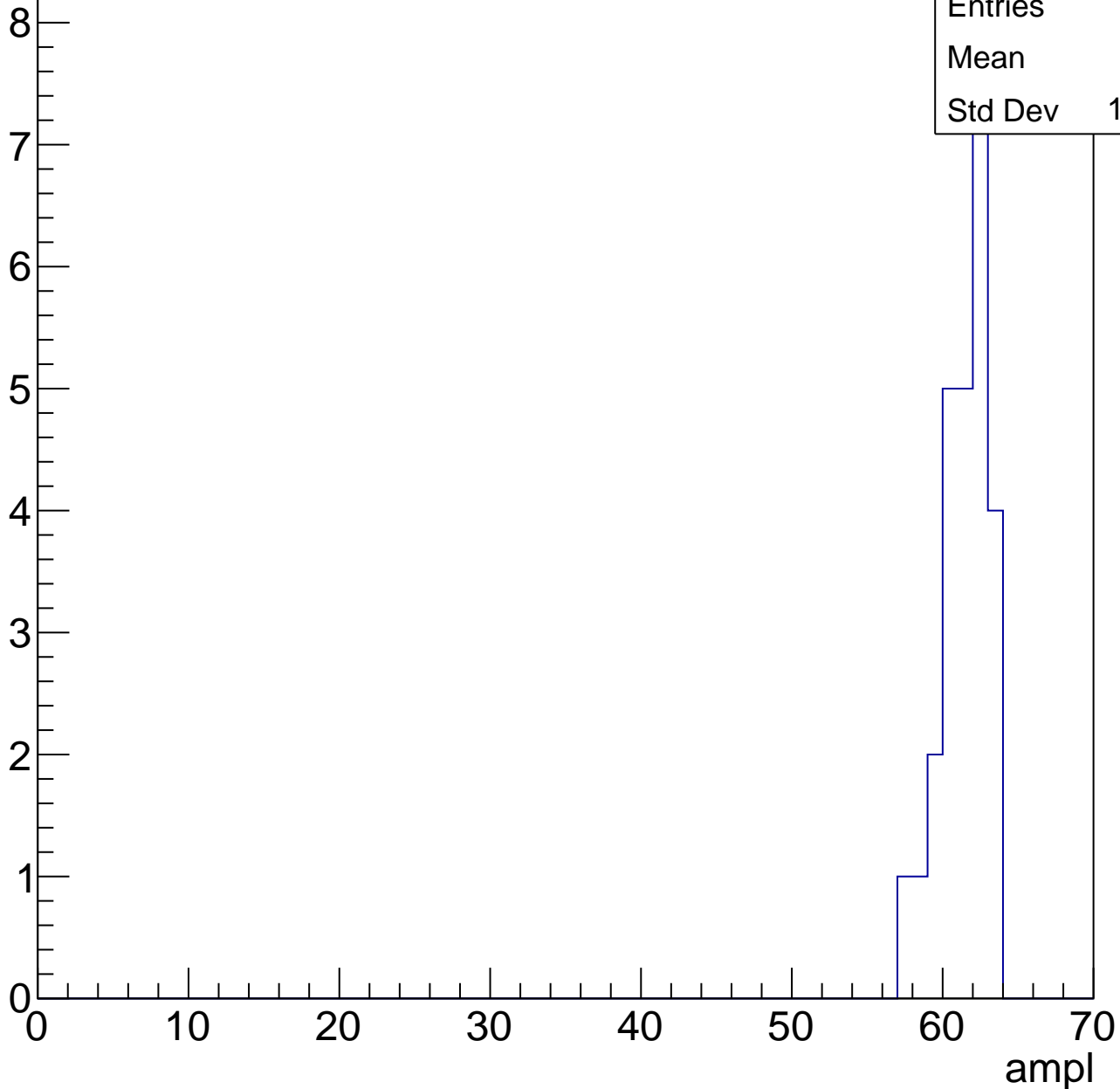


# B1L103S, U26-ch50, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	26
Mean	61
Std Dev	1.544





# B1L103S, U26-ch50, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	19
Mean	3.316
Std Dev	14.07

Entry



# B1L103S, U26-ch51, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	111
Mean	22.26
Std Dev	13.35

**Gaus mean : 30.1526**

**Gaus Width: 3.6634**

Entry

25

20

15

10

5

0

0

10

20

30

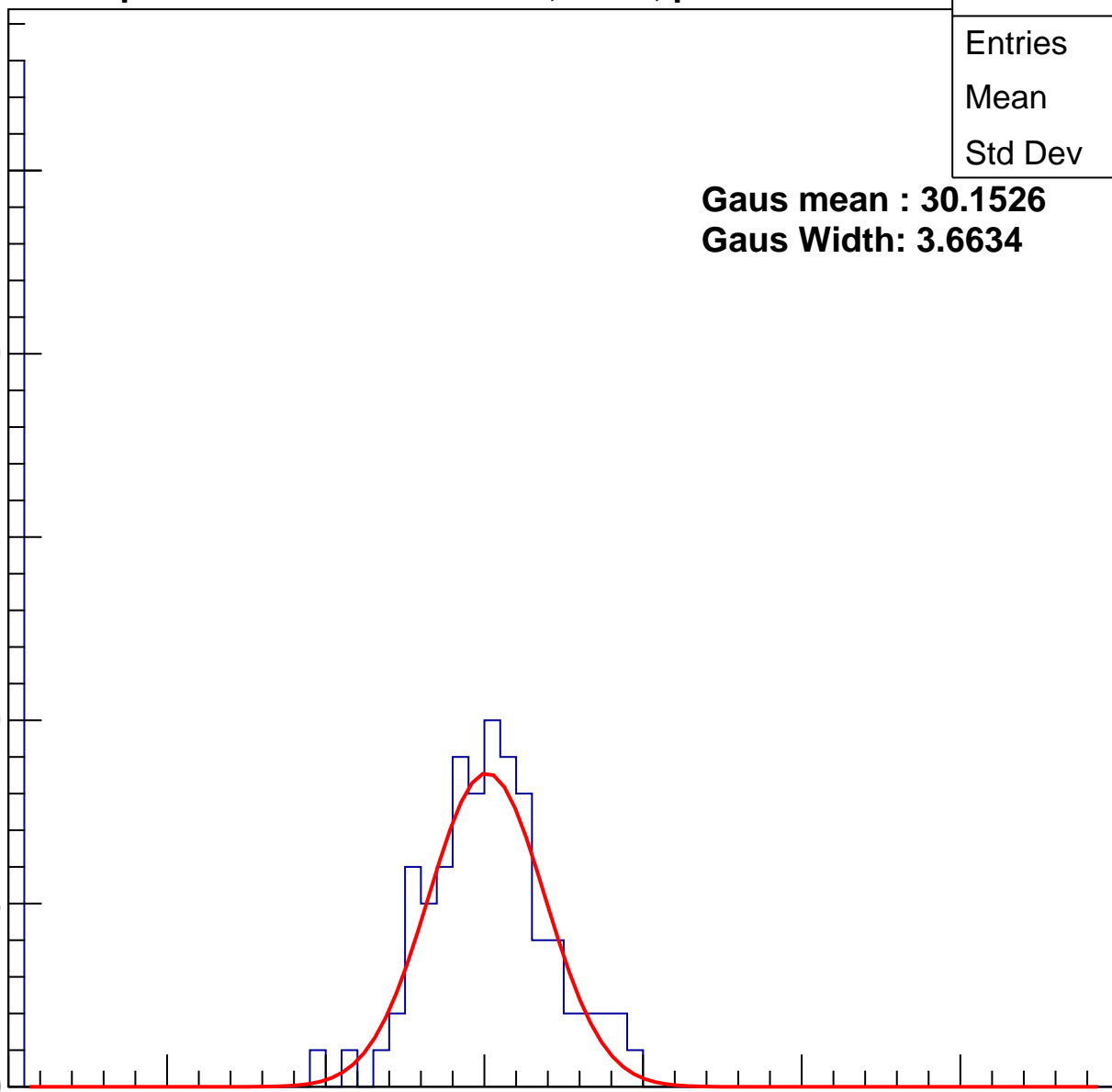
40

50

60

70

ampl



# B1L103S, U26-ch51, adc1

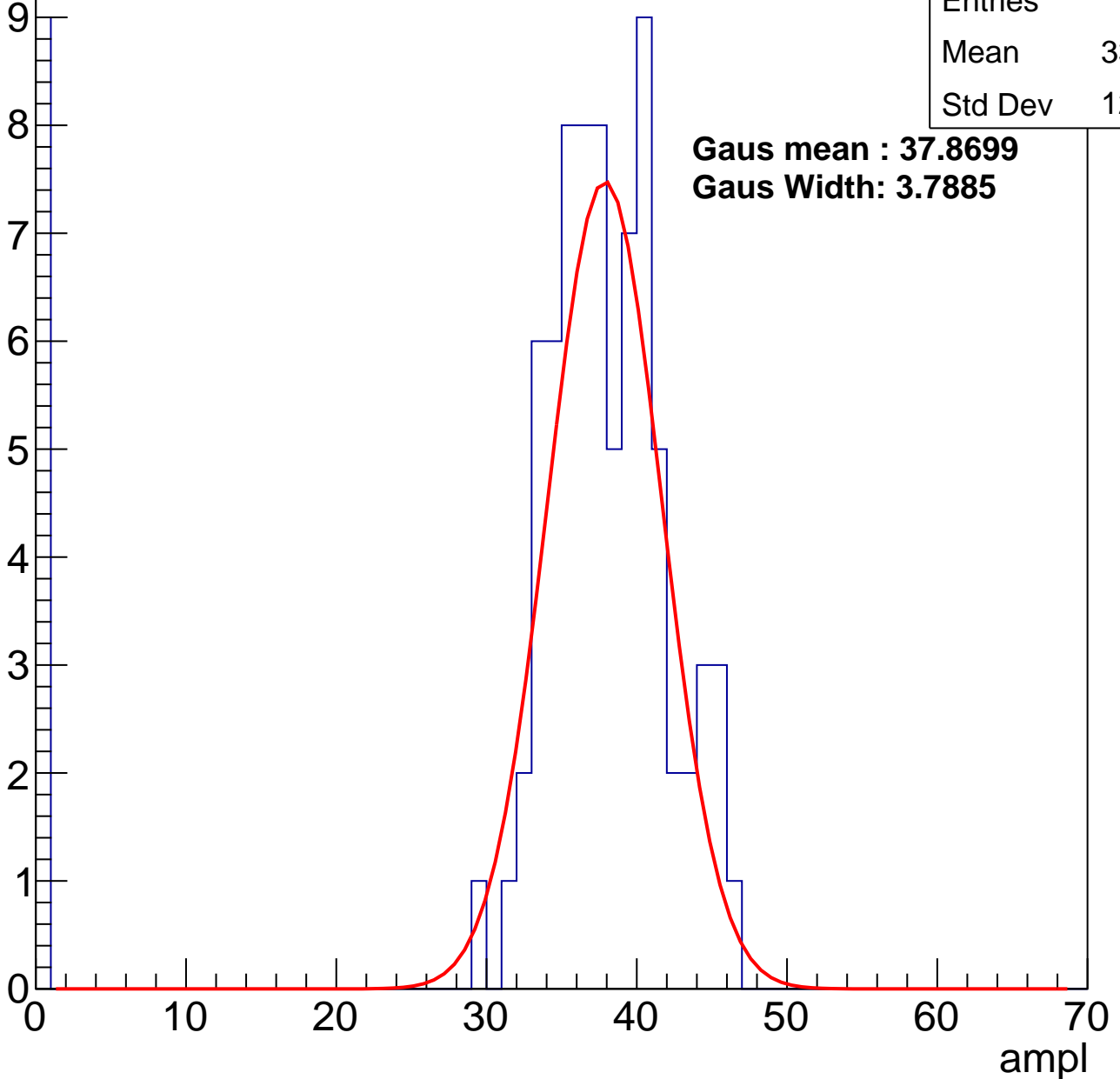
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	86
Mean	33.73
Std Dev	12.05

**Gaus mean : 37.8699**

**Gaus Width: 3.7885**



# B1L103S, U26-ch51, adc2

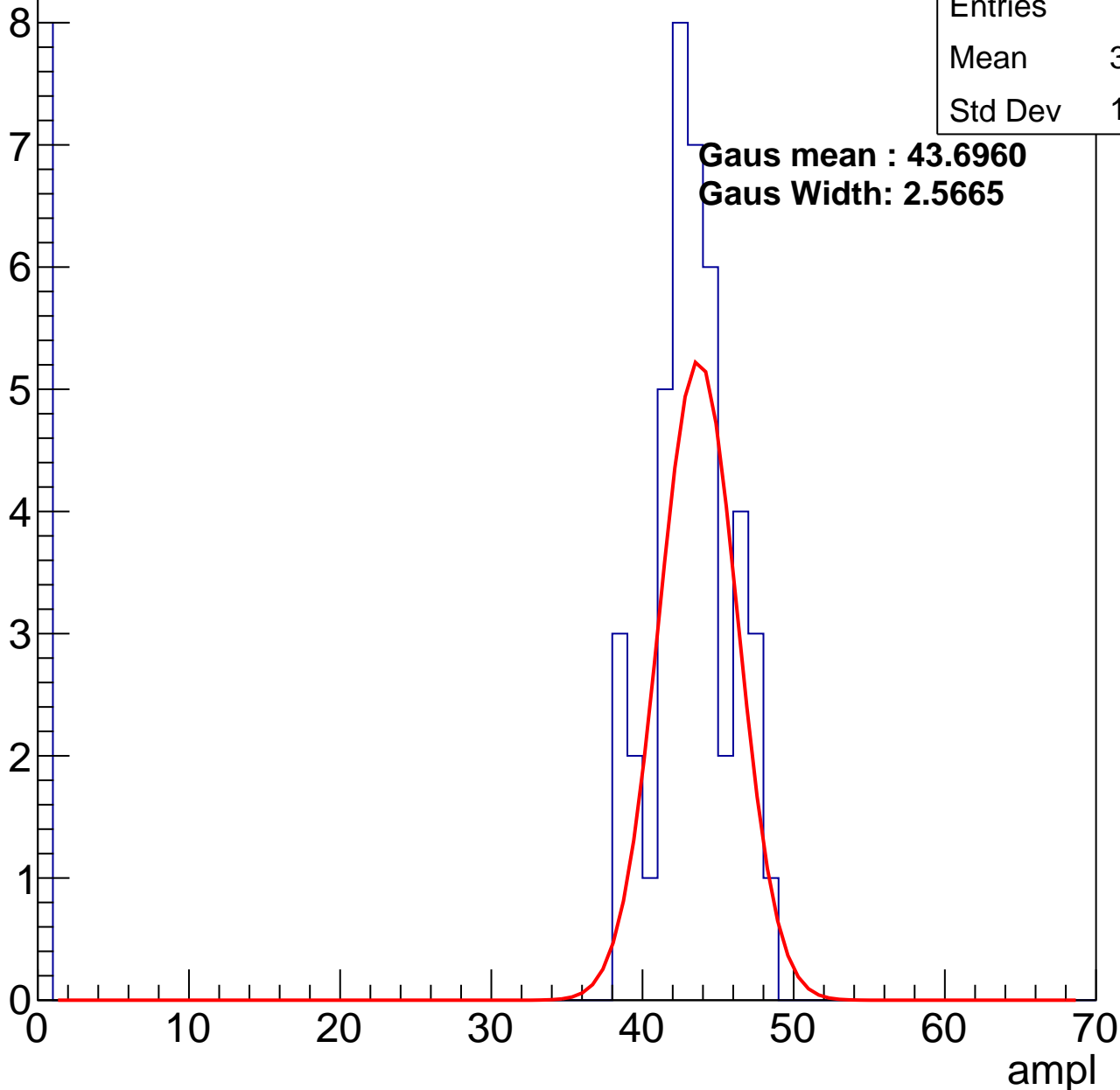
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	50
Mean	36.02
Std Dev	15.89

**Gaus mean : 43.6960**

**Gaus Width: 2.5665**



# B1L103S, U26-ch51, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	70
Mean	49.93
Std Dev	3.445

Entry

10

8

6

4

2

0

0

10

20

30

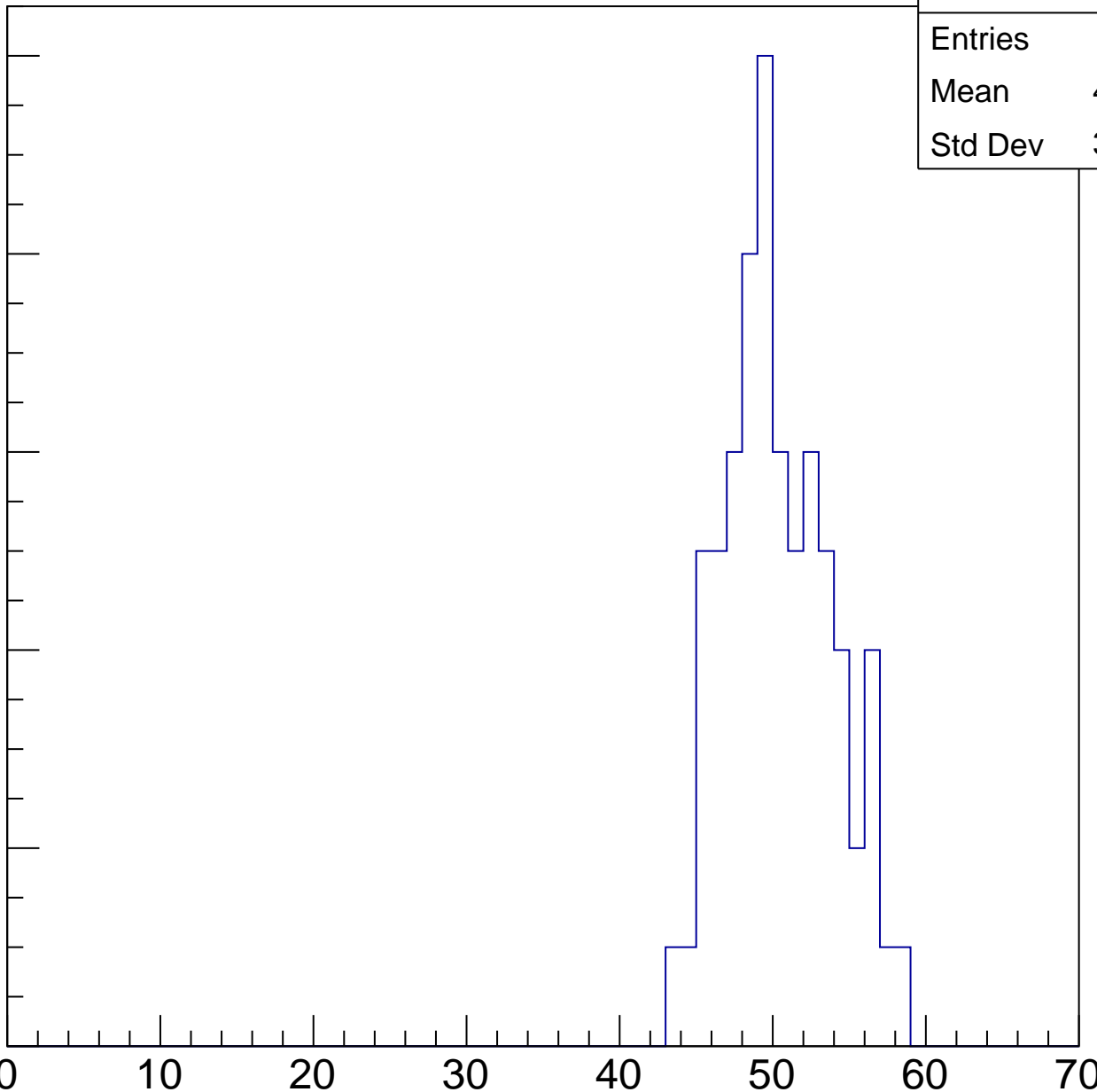
40

50

60

ampl

70

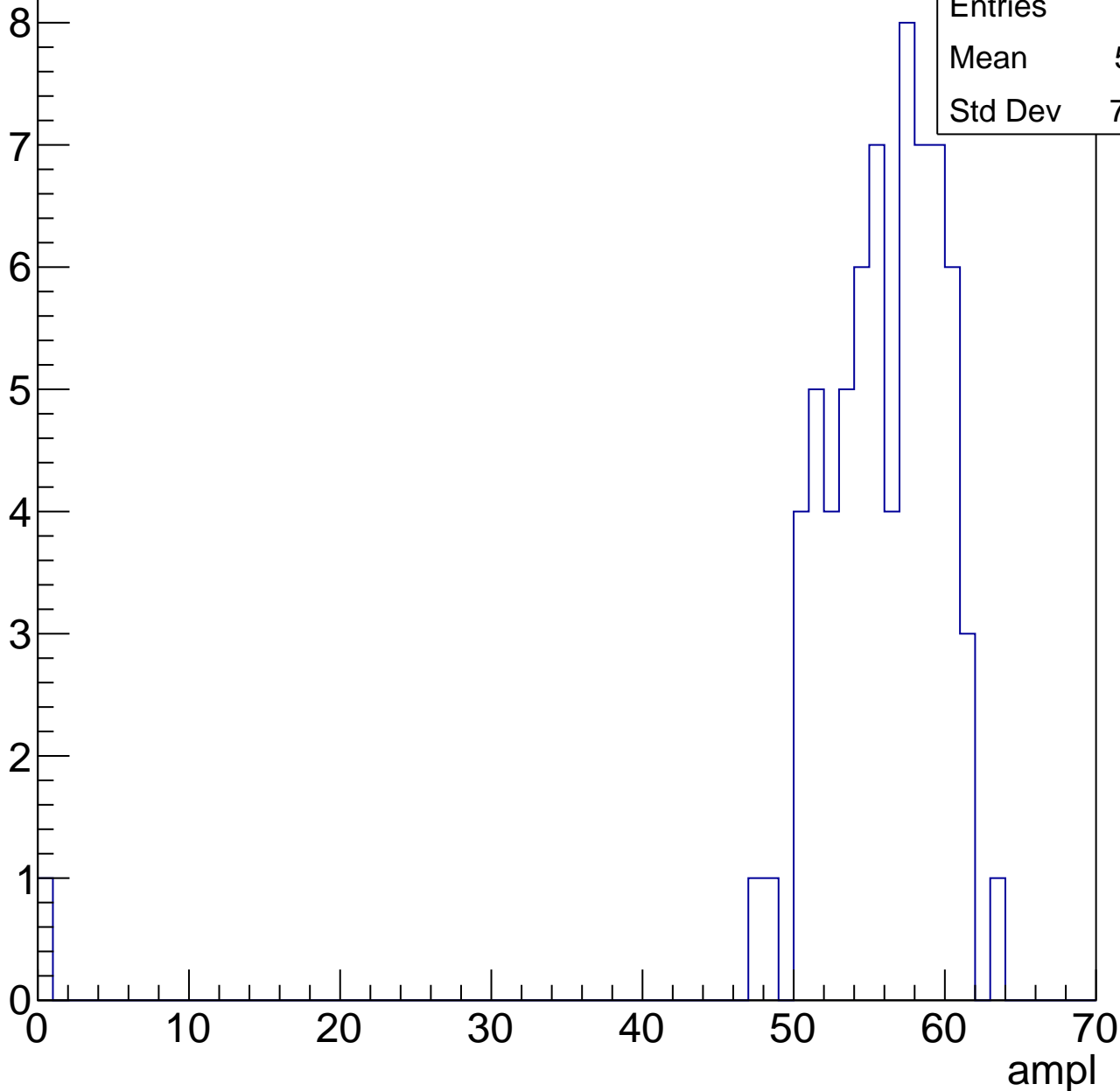


# B1L103S, U26-ch51, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	70
Mean	54.81
Std Dev	7.474



# B1L103S, U26-ch51, adc5

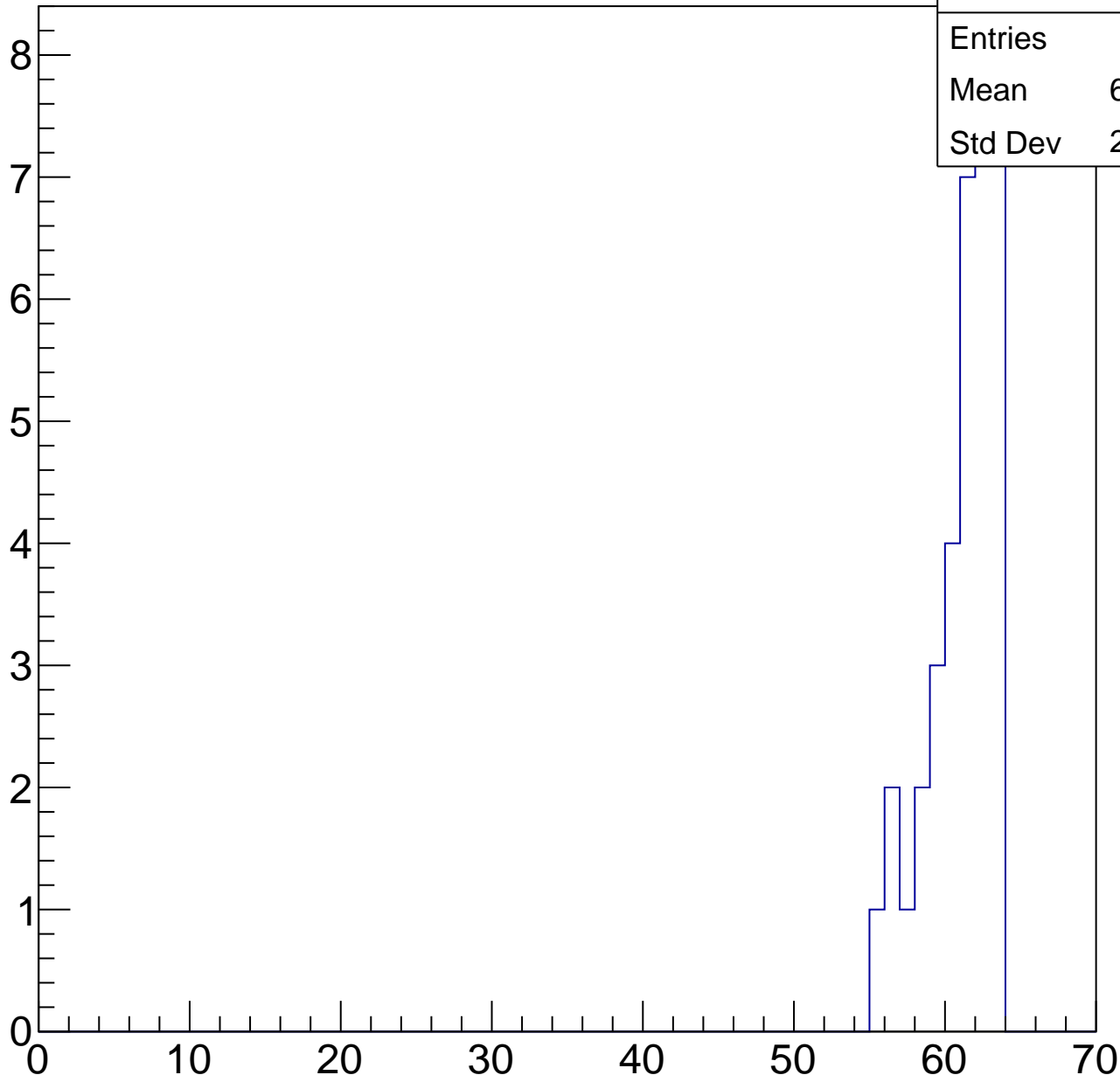
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	36
Mean	60.67
Std Dev	2.186

ampl



# B1L103S, U26-ch51, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry





# B1L103S, U26-ch51, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



Entries	18
Mean	0
Std Dev	0

# B1L103S, U26-ch52, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	72
Mean	24.78
Std Dev	12.03

**Gaus mean : 30.4699**

**Gaus Width: 3.7058**

Entry

12

10

8

6

4

2

0

0

10

20

30

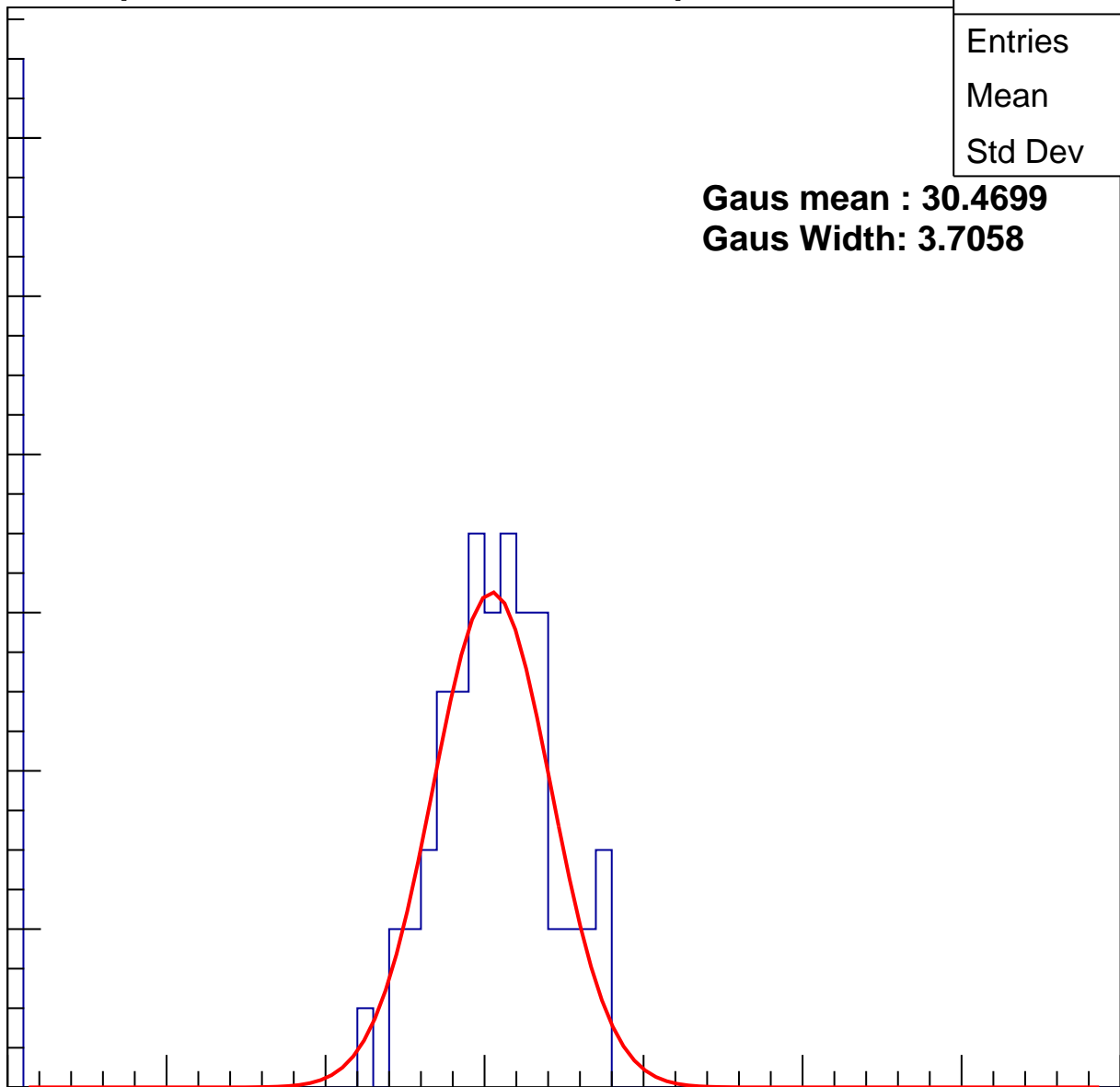
40

50

60

70

ampl



# B1L103S, U26-ch52, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	106
Mean	32.23
Std Dev	13.66

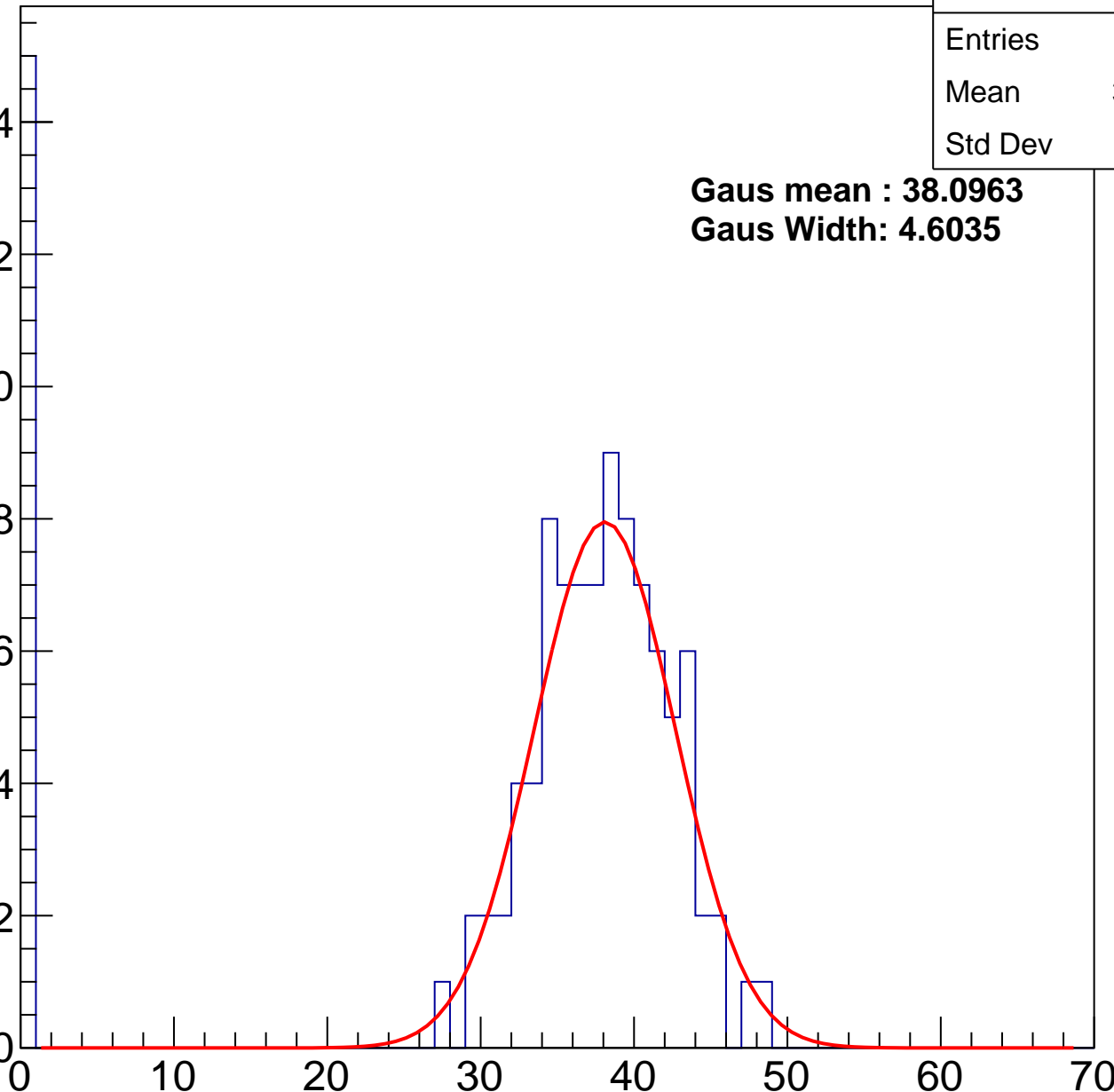
**Gaus mean : 38.0963**

**Gaus Width: 4.6035**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U26-ch52, adc2

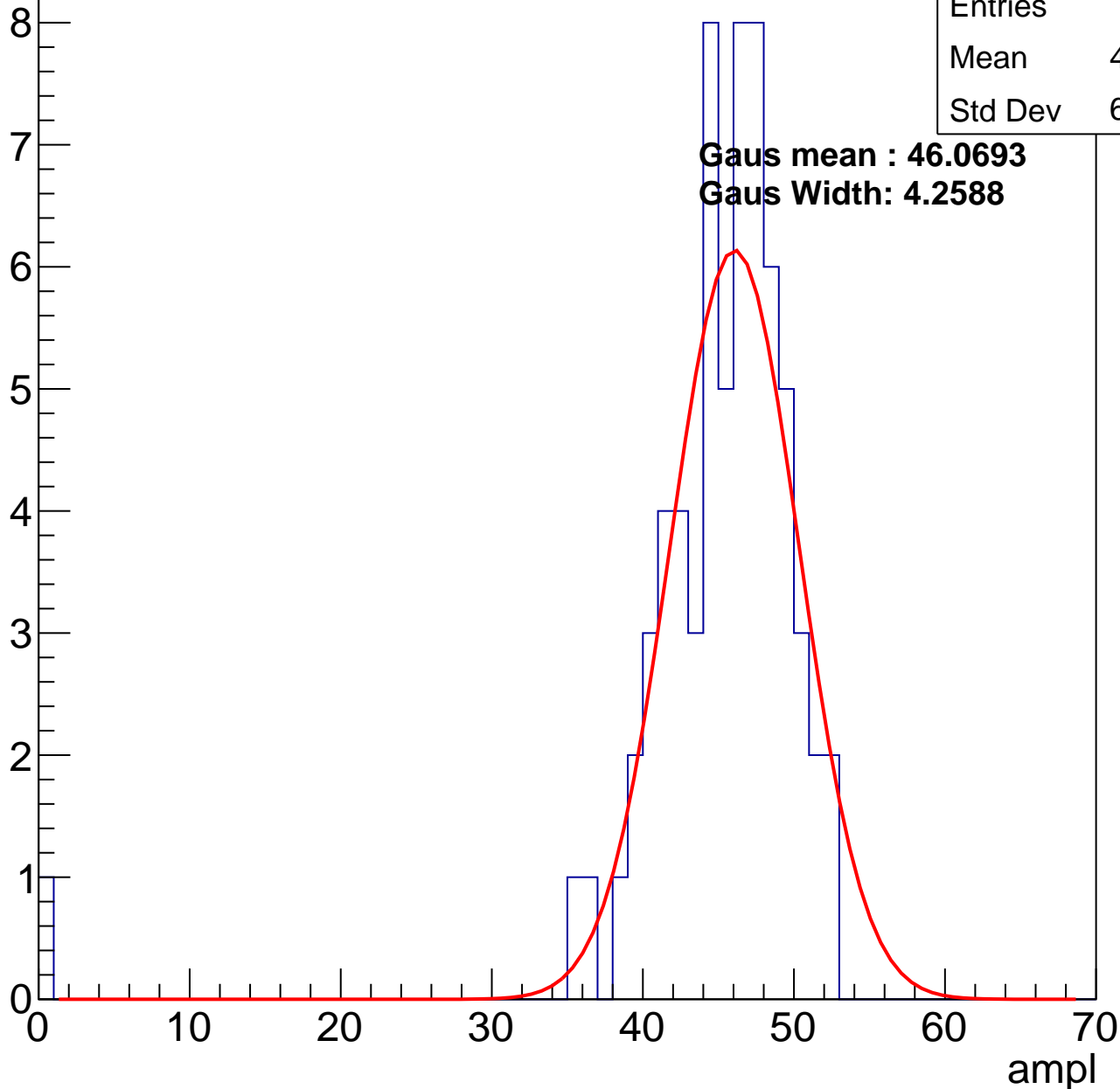
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	67
Mean	44.45
Std Dev	6.602

**Gaus mean : 46.0693**

**Gaus Width: 4.2588**

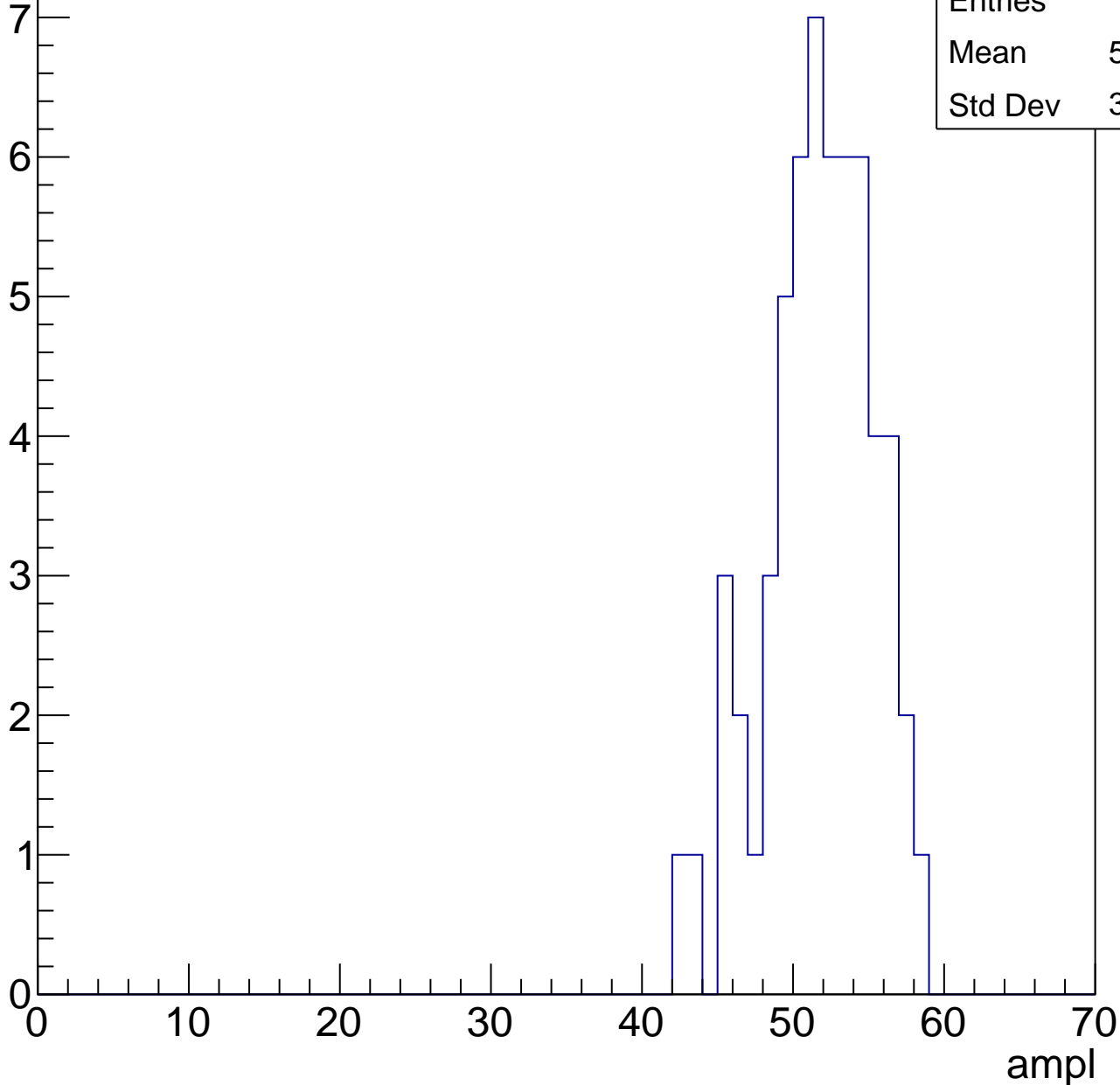


# B1L103S, U26-ch52, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	58
Mean	51.29
Std Dev	3.562

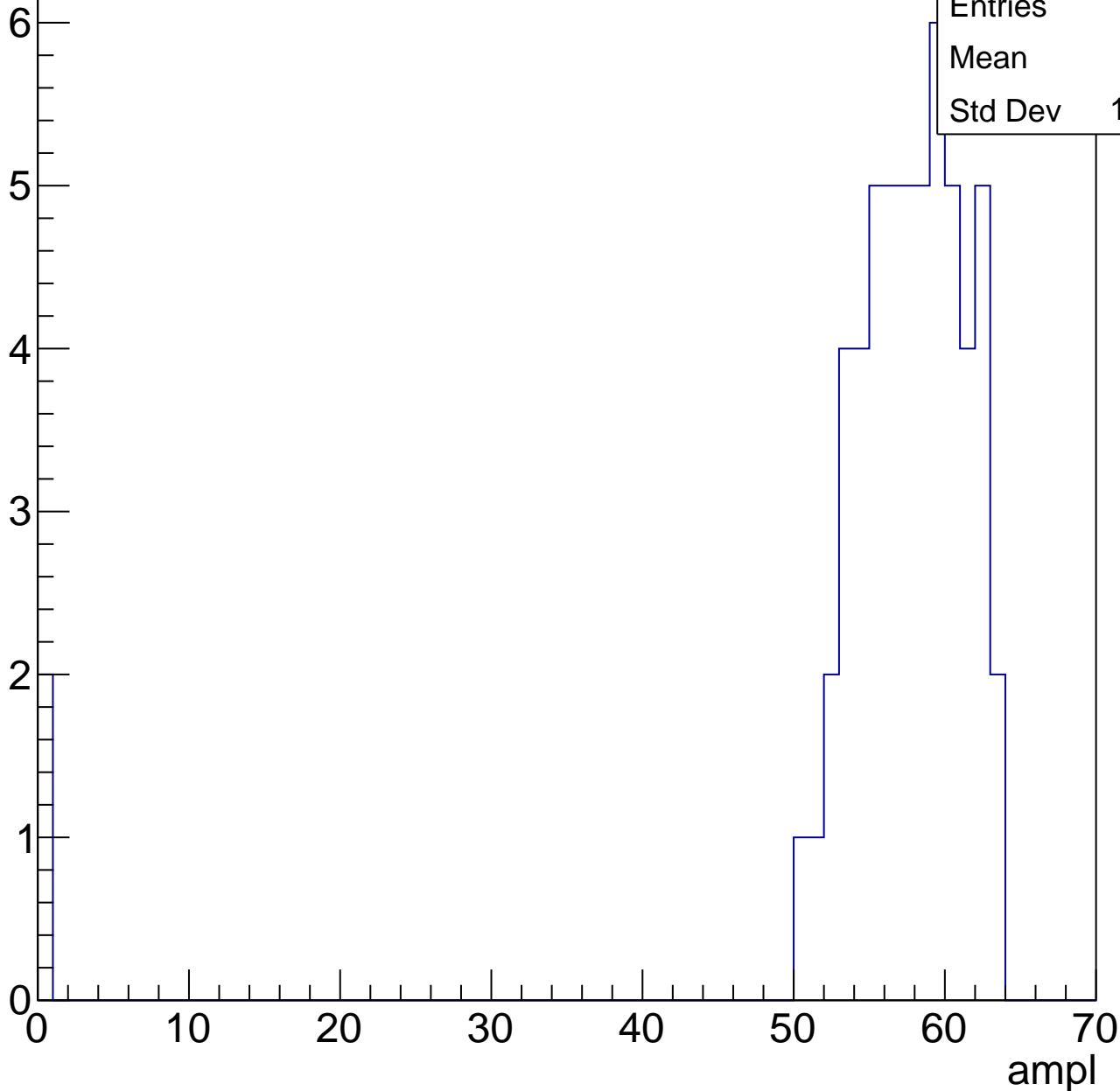


# B1L103S, U26-ch52, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	56
Mean	55.3
Std Dev	11.13

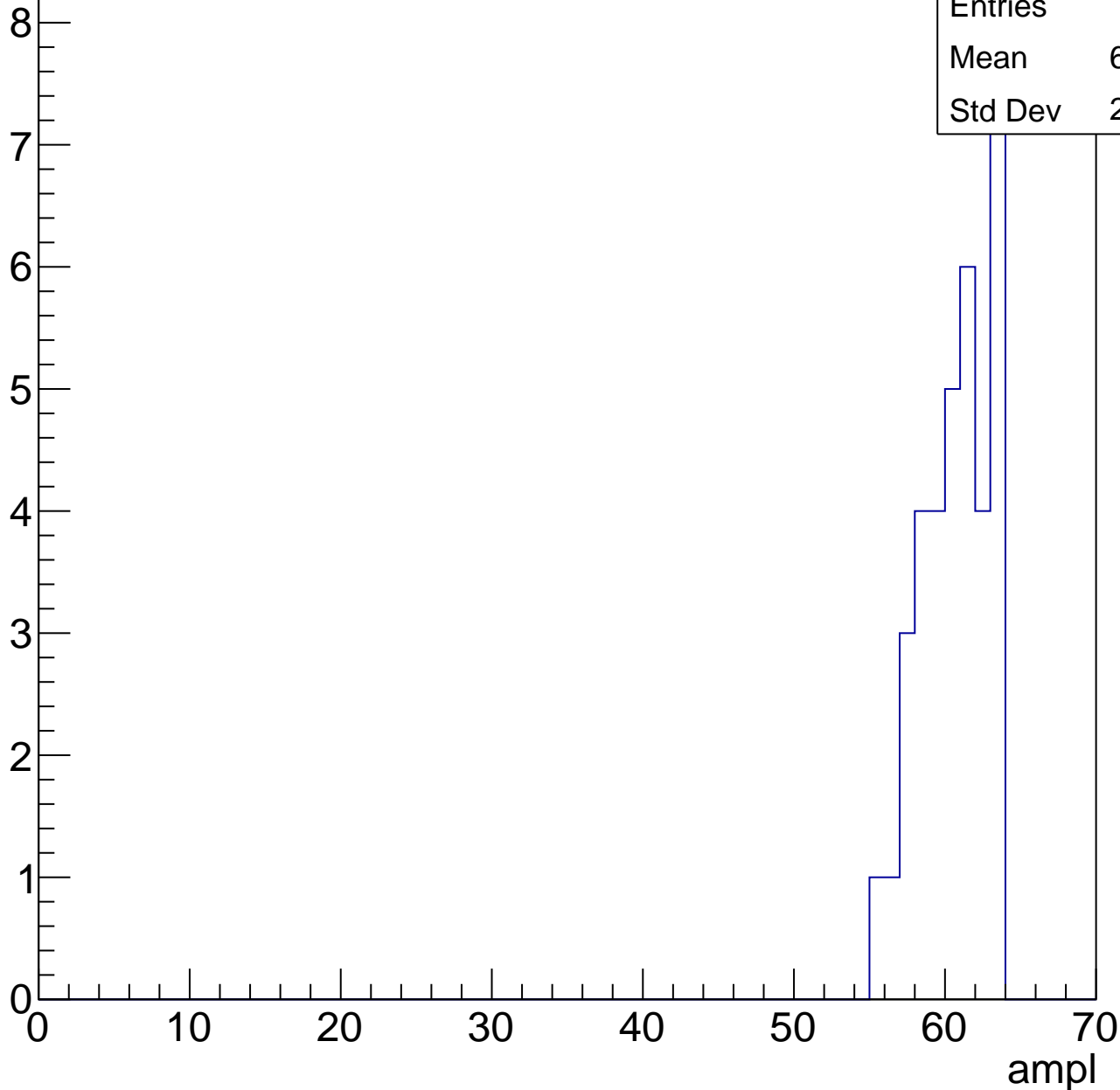


# B1L103S, U26-ch52, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	36
Mean	60.22
Std Dev	2.237



# B1L103S, U26-ch52, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry





# B1L103S, U26-ch52, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



# B1L103S, U26-ch53, adc0

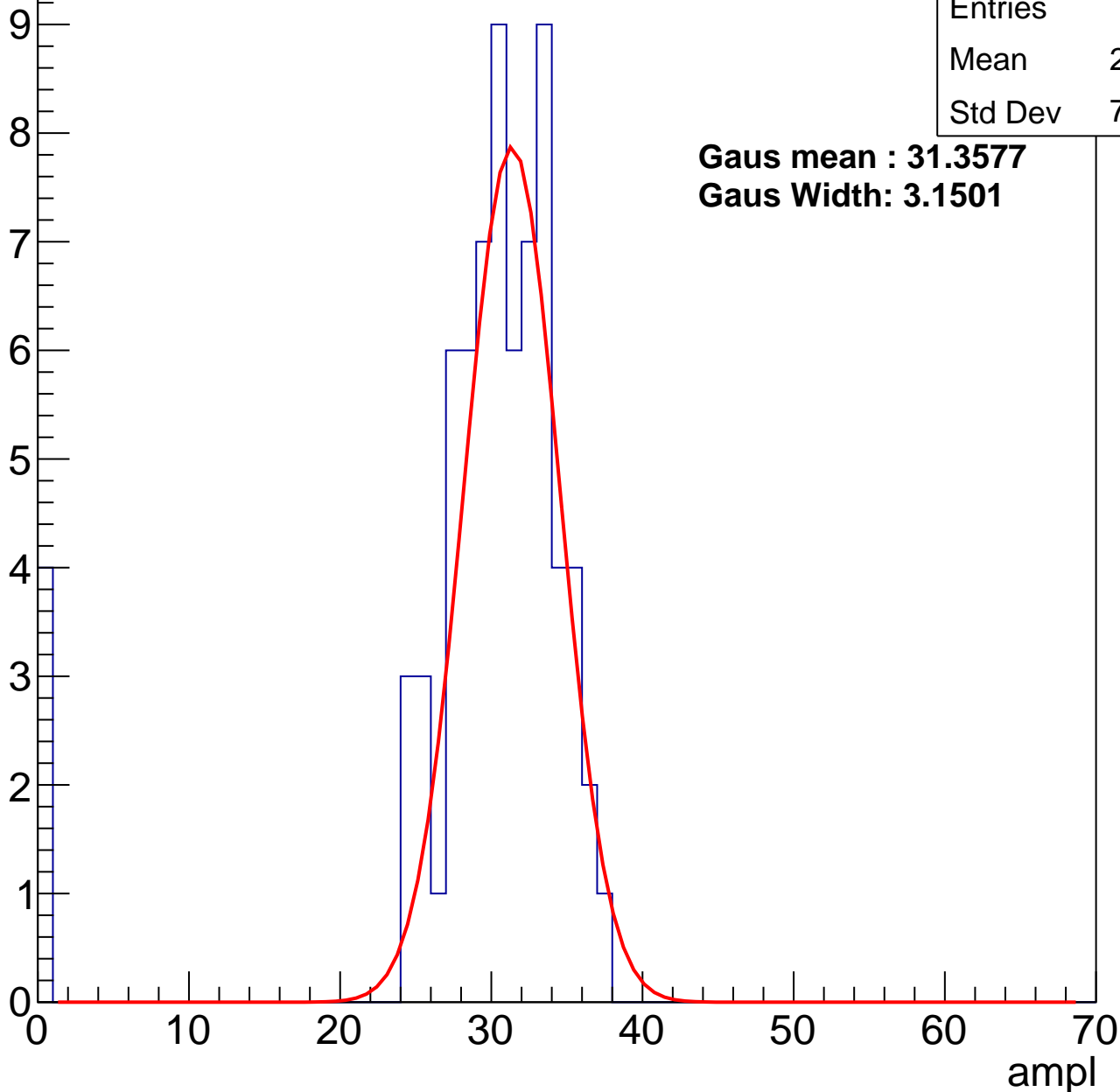
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	72
Mean	28.72
Std Dev	7.607

**Gaus mean : 31.3577**

**Gaus Width: 3.1501**



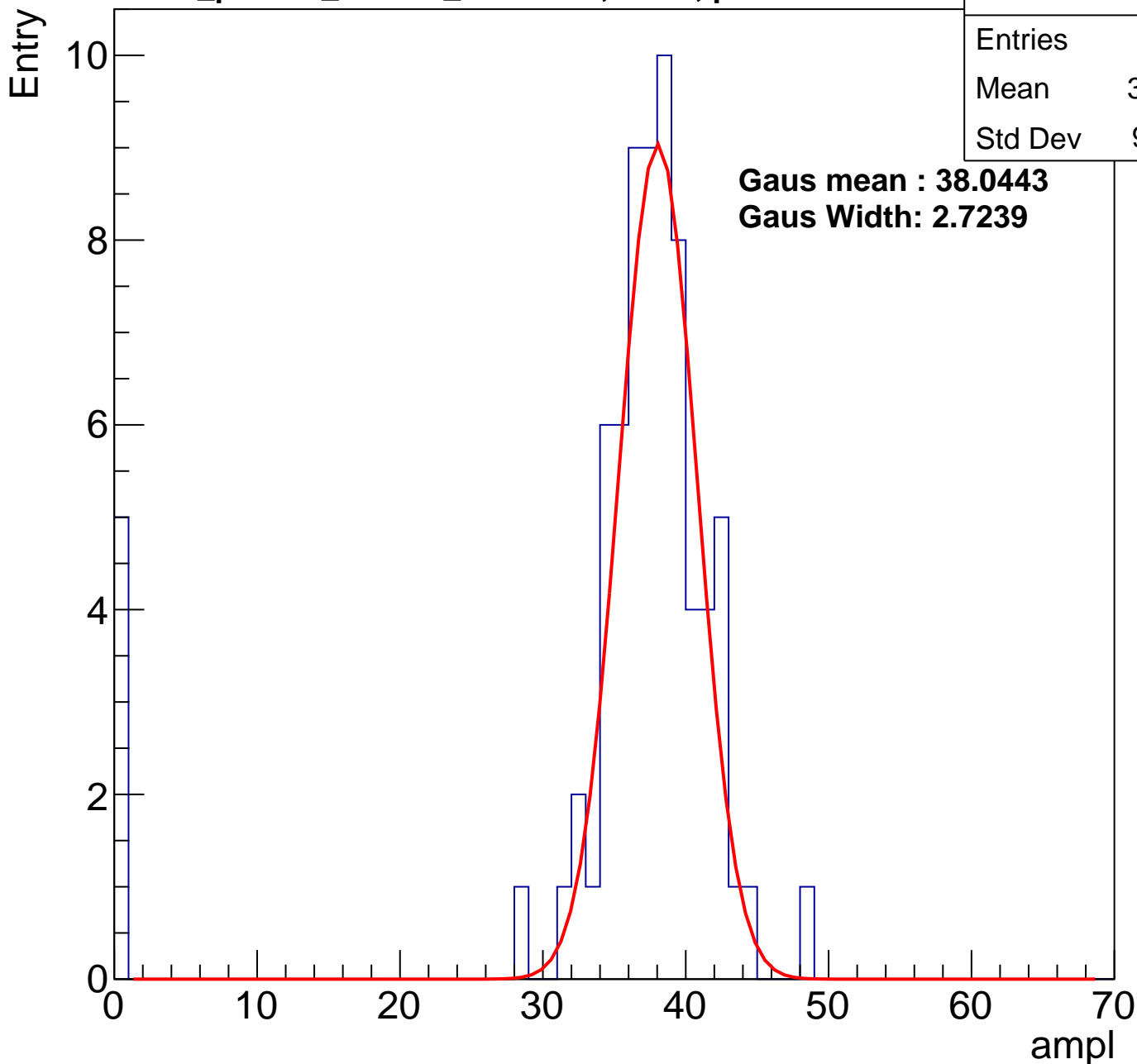
# B1L103S, U26-ch53, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	74
Mean	34.97
Std Dev	9.921

**Gaus mean : 38.0443**

**Gaus Width: 2.7239**



# B1L103S, U26-ch53, adc2

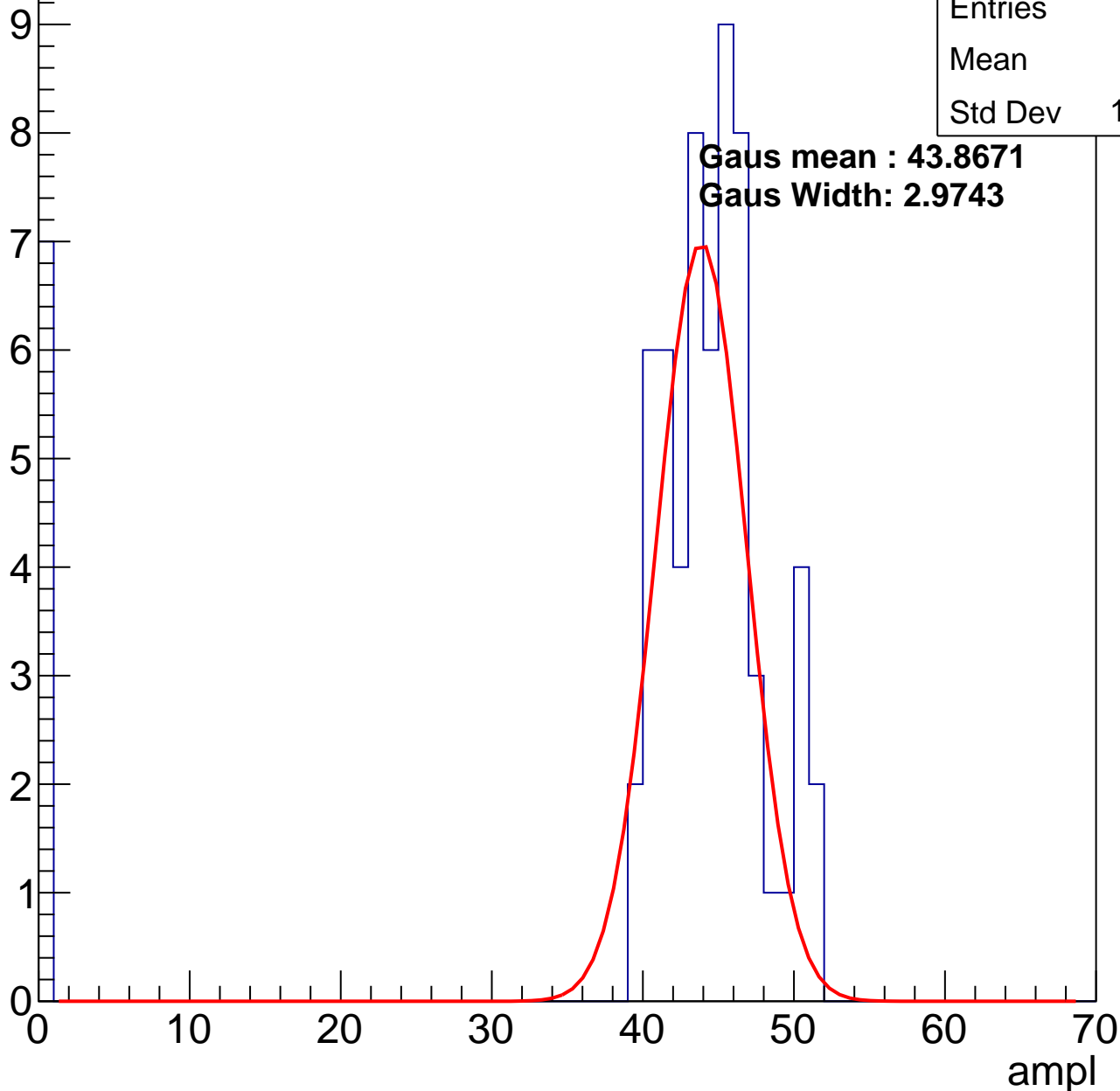
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	67
Mean	39.6
Std Dev	13.84

**Gaus mean : 43.8671**

**Gaus Width: 2.9743**

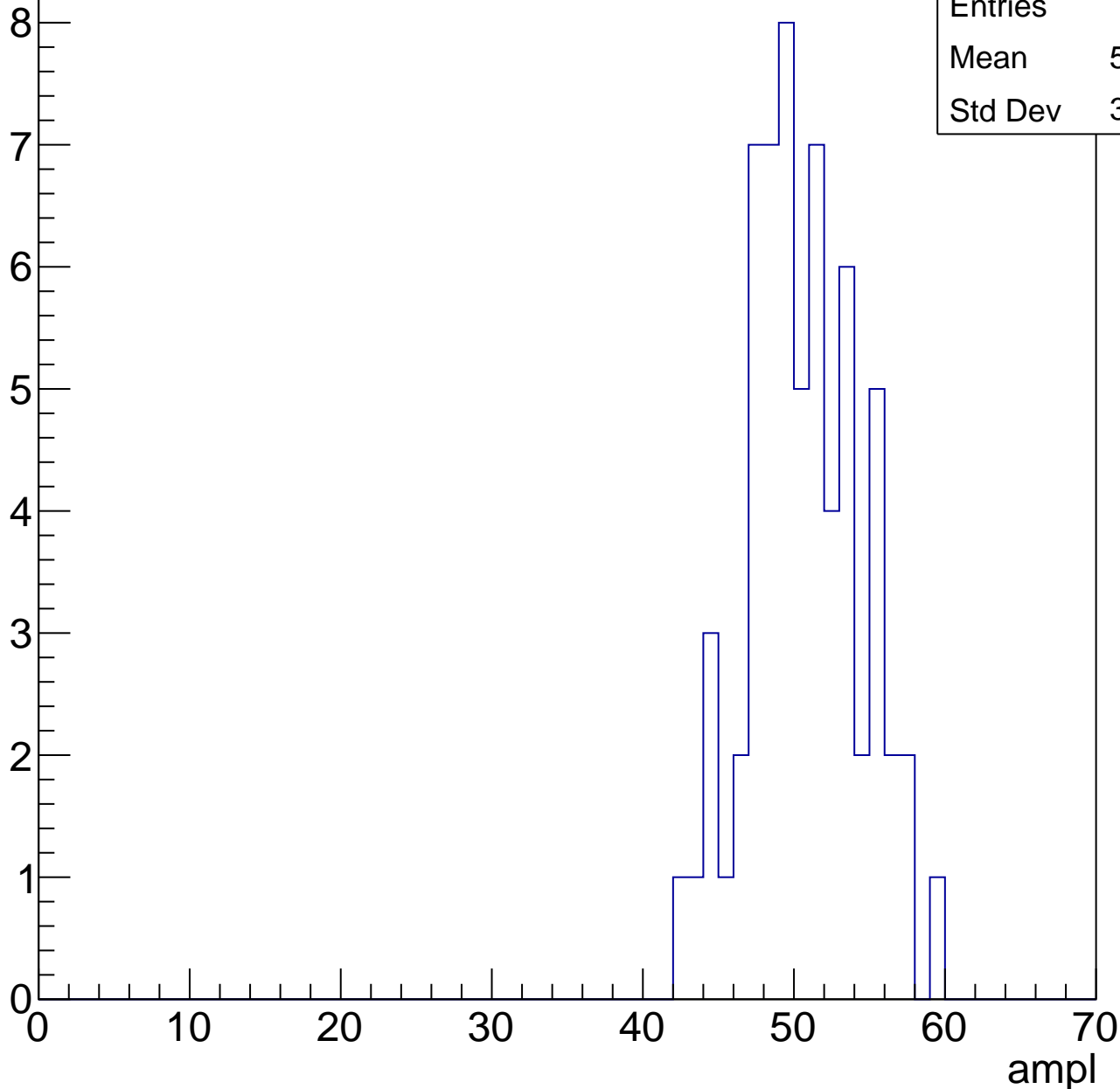


# B1L103S, U26-ch53, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	64
Mean	50.19
Std Dev	3.665

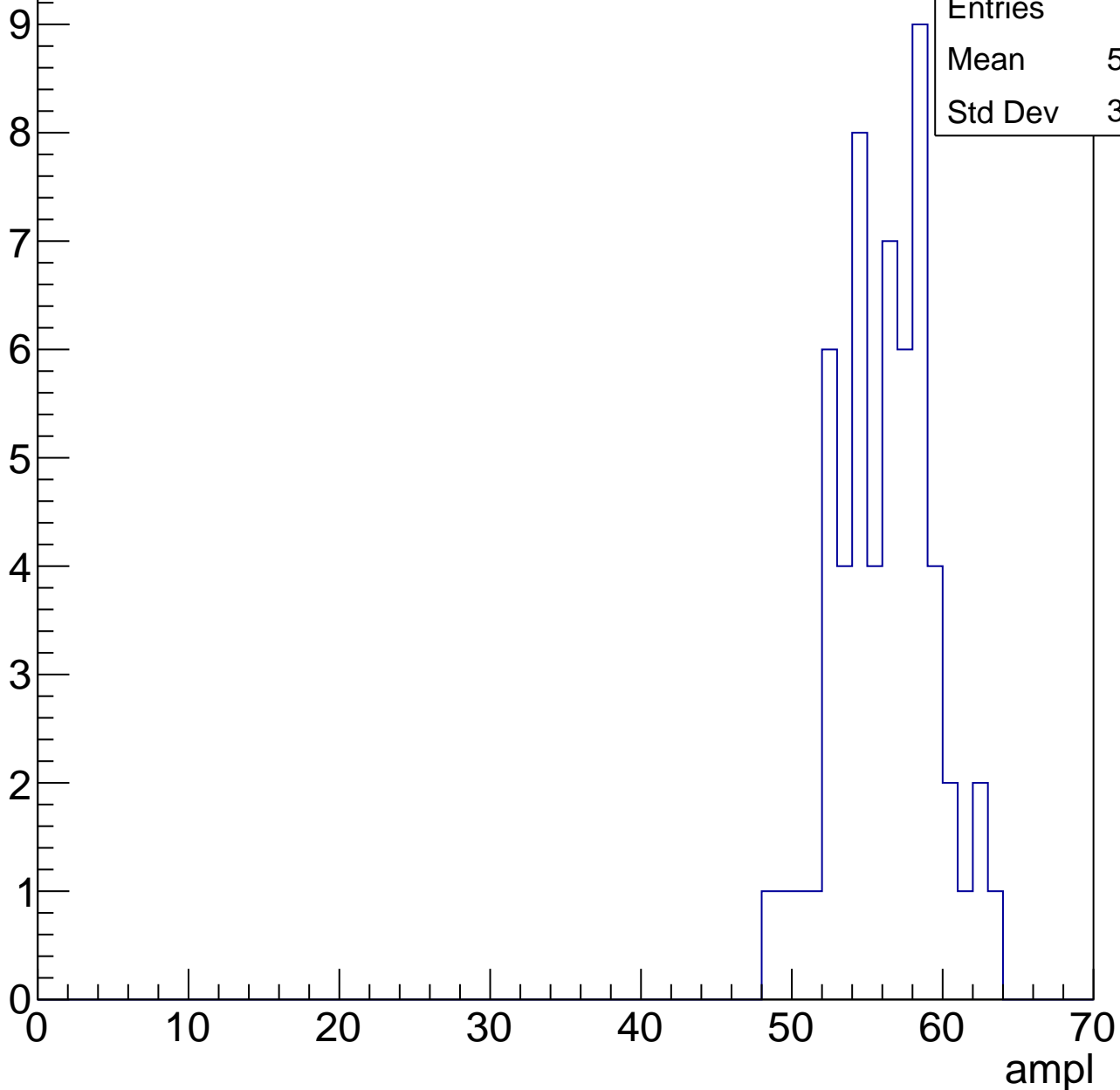


# B1L103S, U26-ch53, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

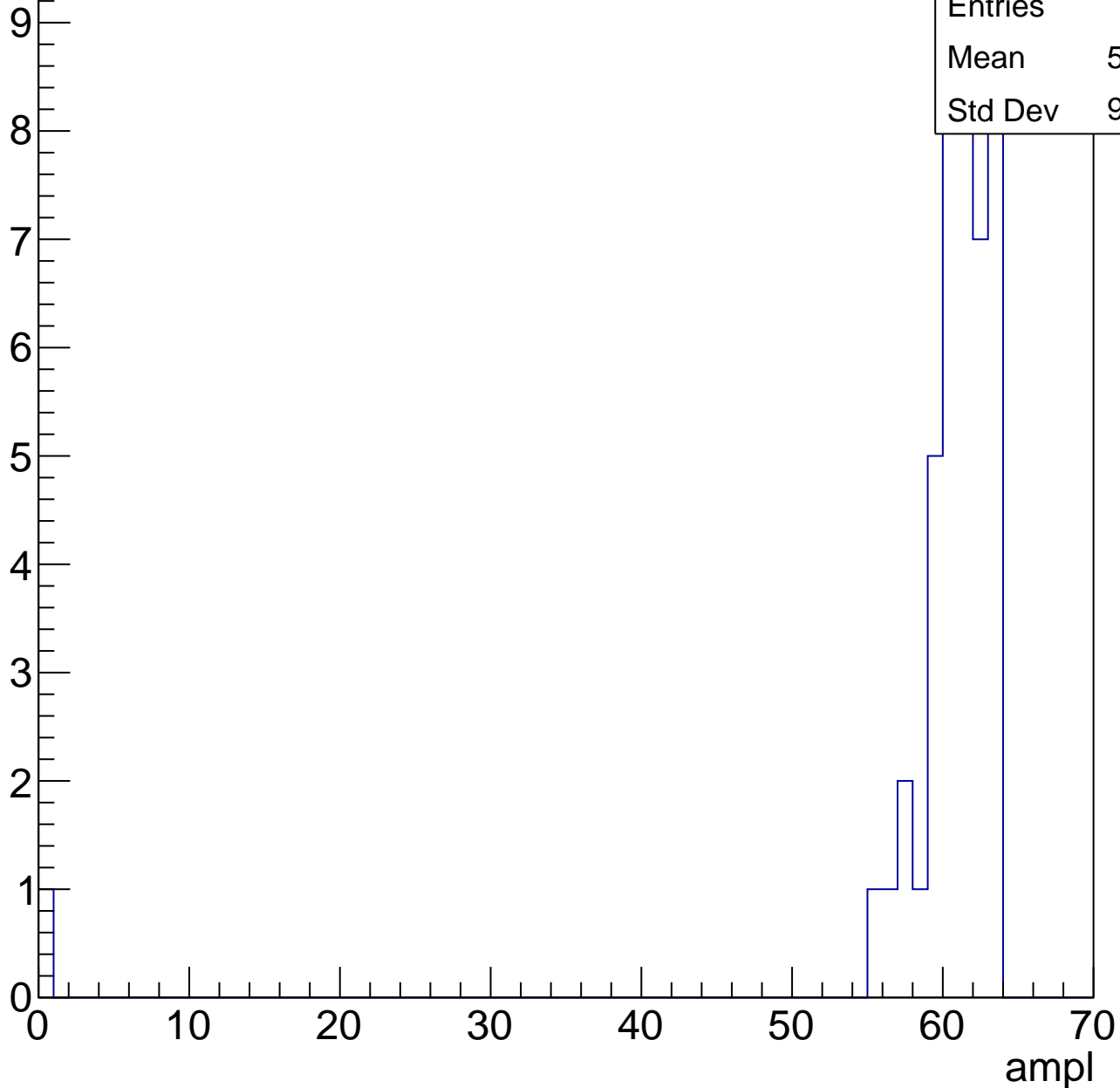
Entries	58
Mean	55.76
Std Dev	3.202



# B1L103S, U26-ch53, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



# B1L103S, U26-ch53, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry





# B1L103S, U26-ch53, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



Entries	18
Mean	0
Std Dev	0

# B1L103S, U26-ch54, adc0

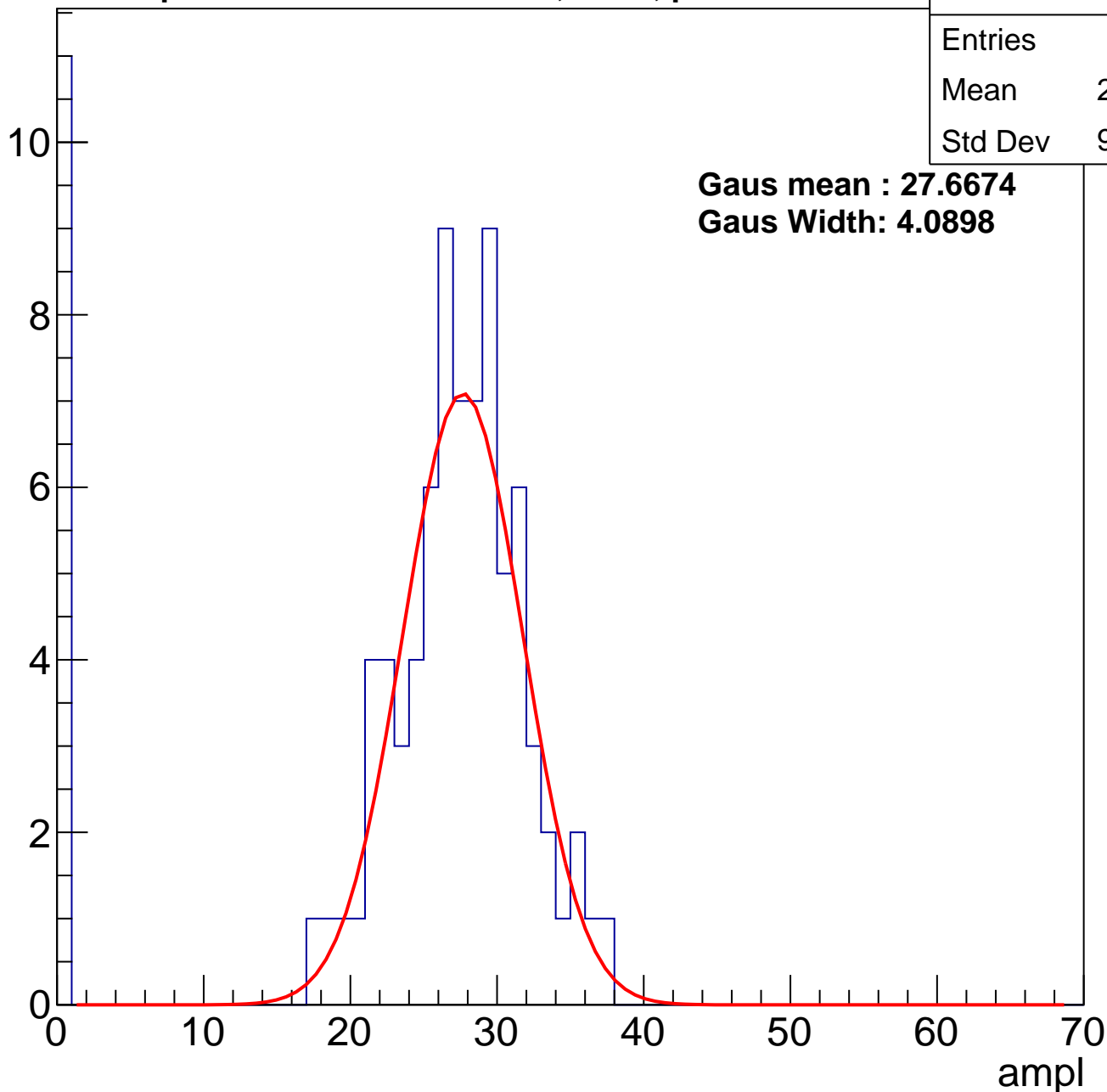
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	89
Mean	23.78
Std Dev	9.737

**Gaus mean : 27.6674**

**Gaus Width: 4.0898**

Entry



# B1L103S, U26-ch54, adc1

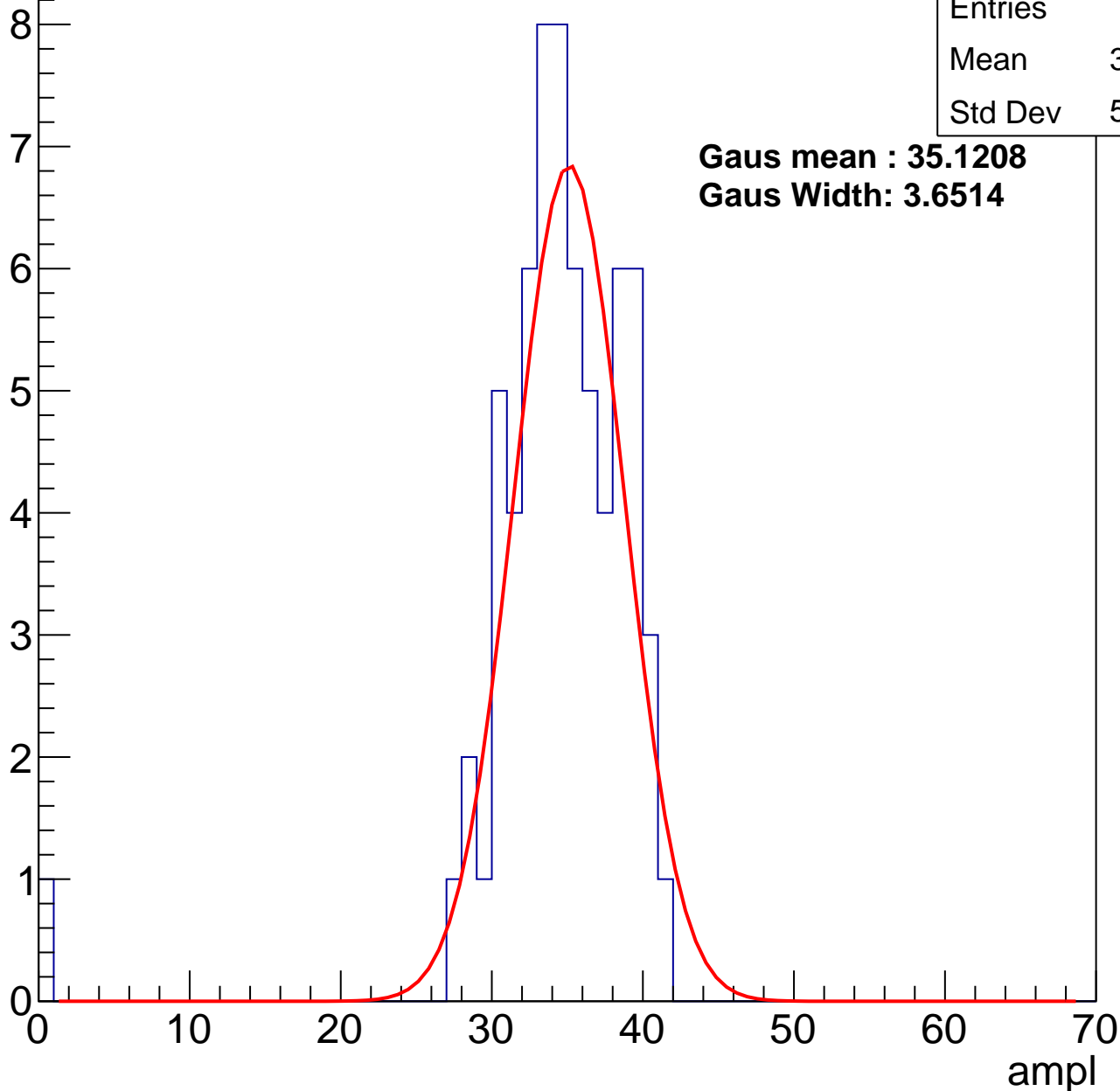
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	67
Mean	33.96
Std Dev	5.346

**Gaus mean : 35.1208**

**Gaus Width: 3.6514**



# B1L103S, U26-ch54, adc2

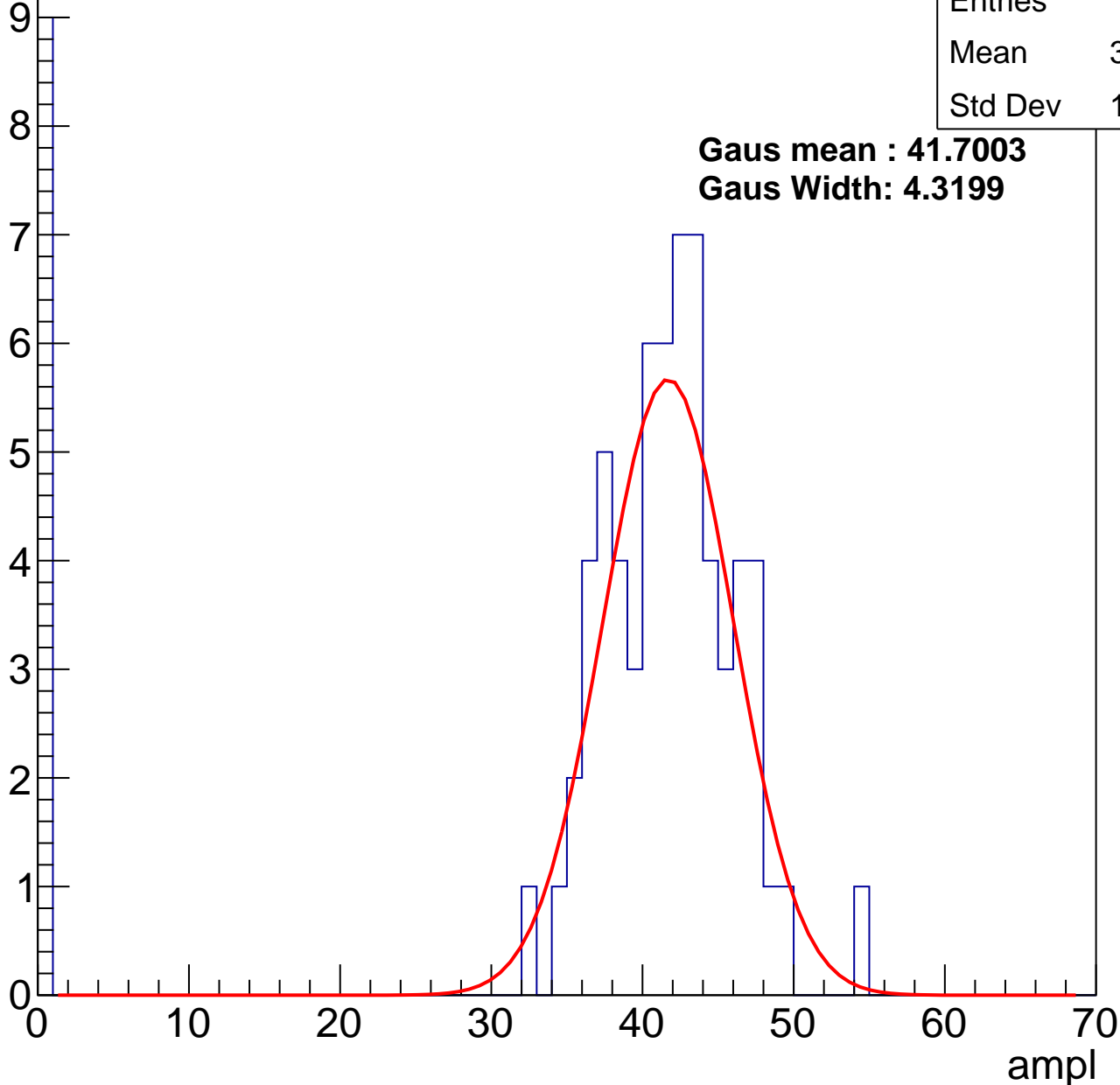
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	73
Mean	36.29
Std Dev	14.14

**Gaus mean : 41.7003**

**Gaus Width: 4.3199**

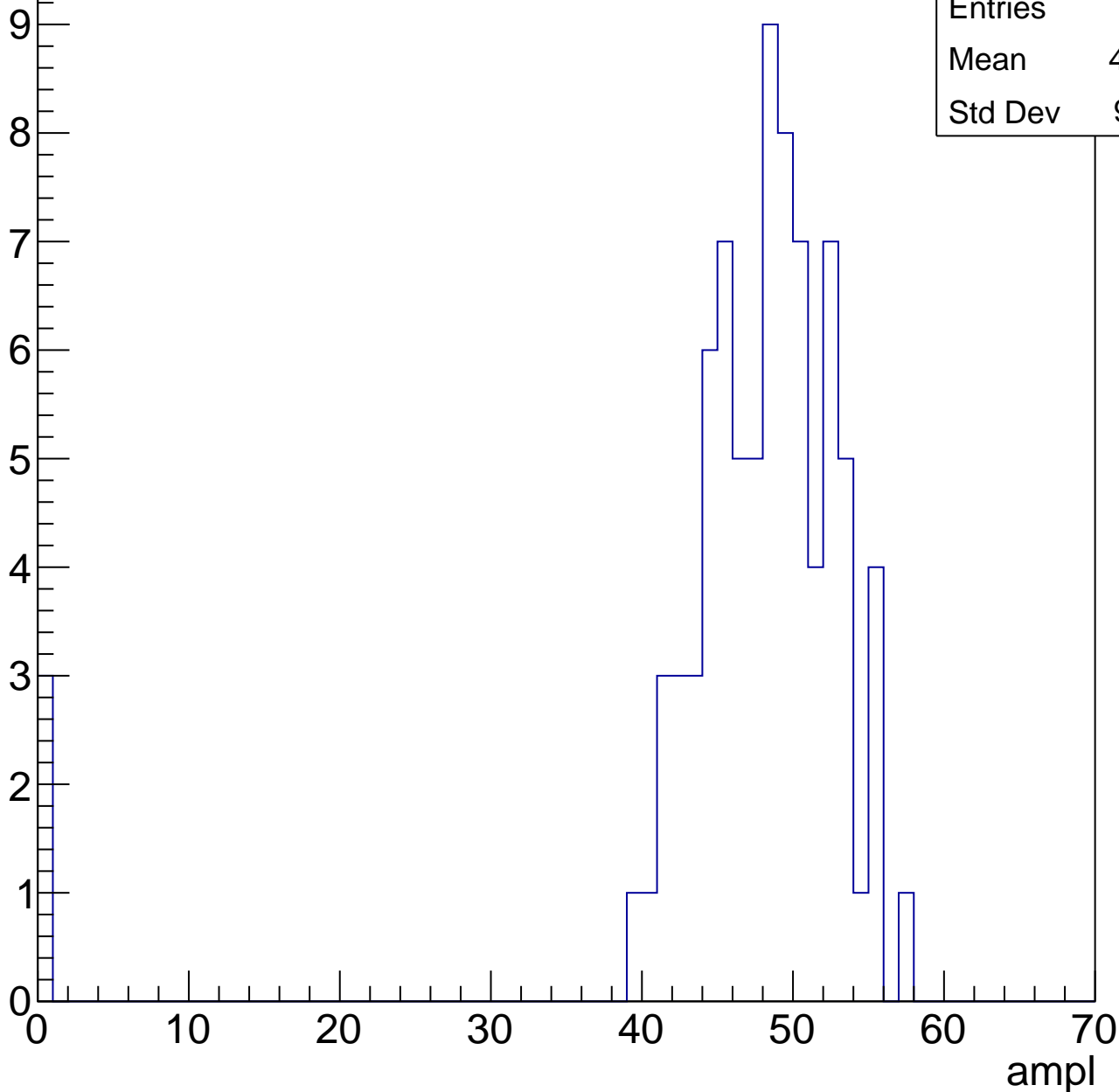


# B1L103S, U26-ch54, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	83
Mean	46.25
Std Dev	9.781

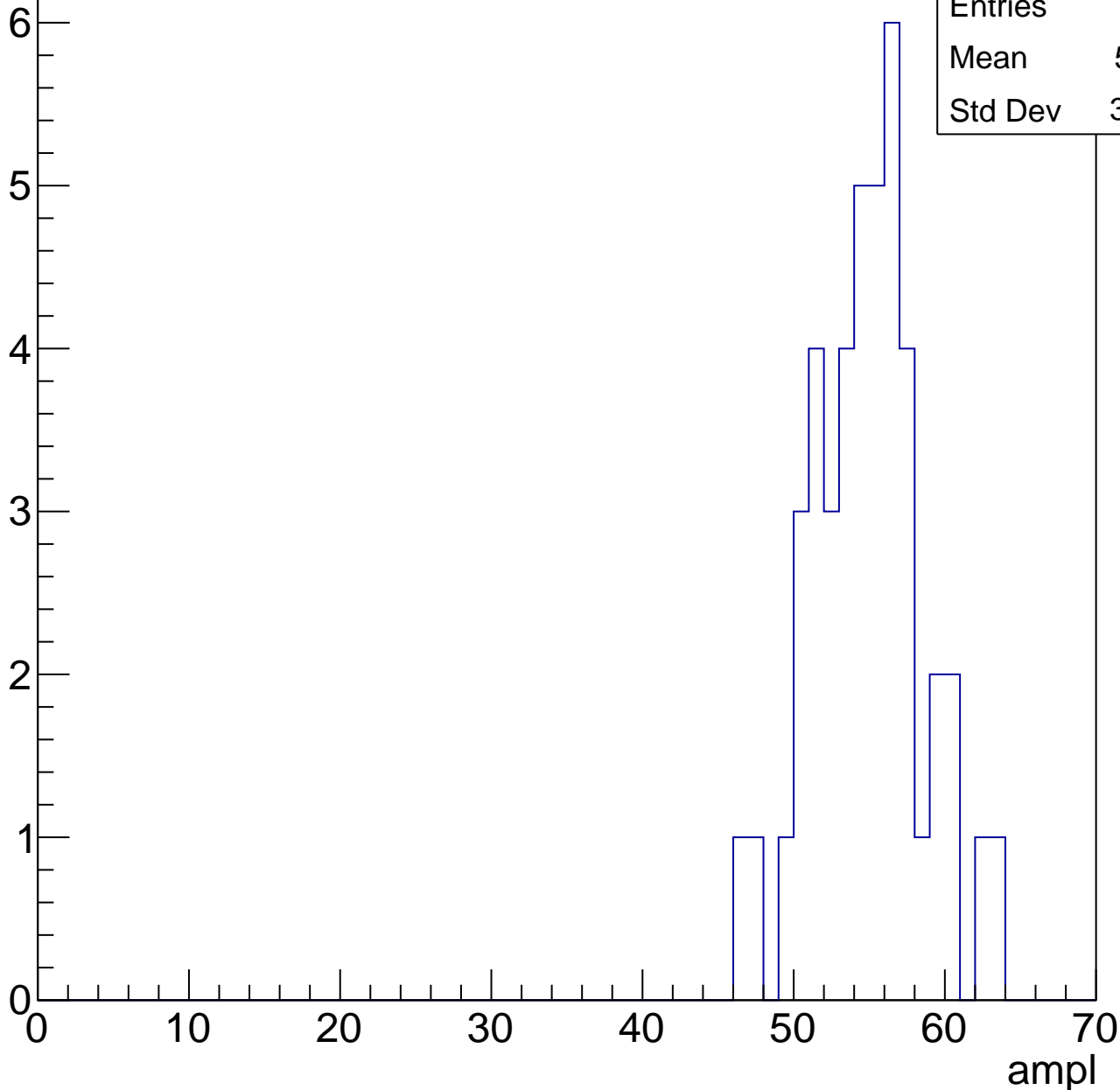


# B1L103S, U26-ch54, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	44
Mean	54.41
Std Dev	3.626

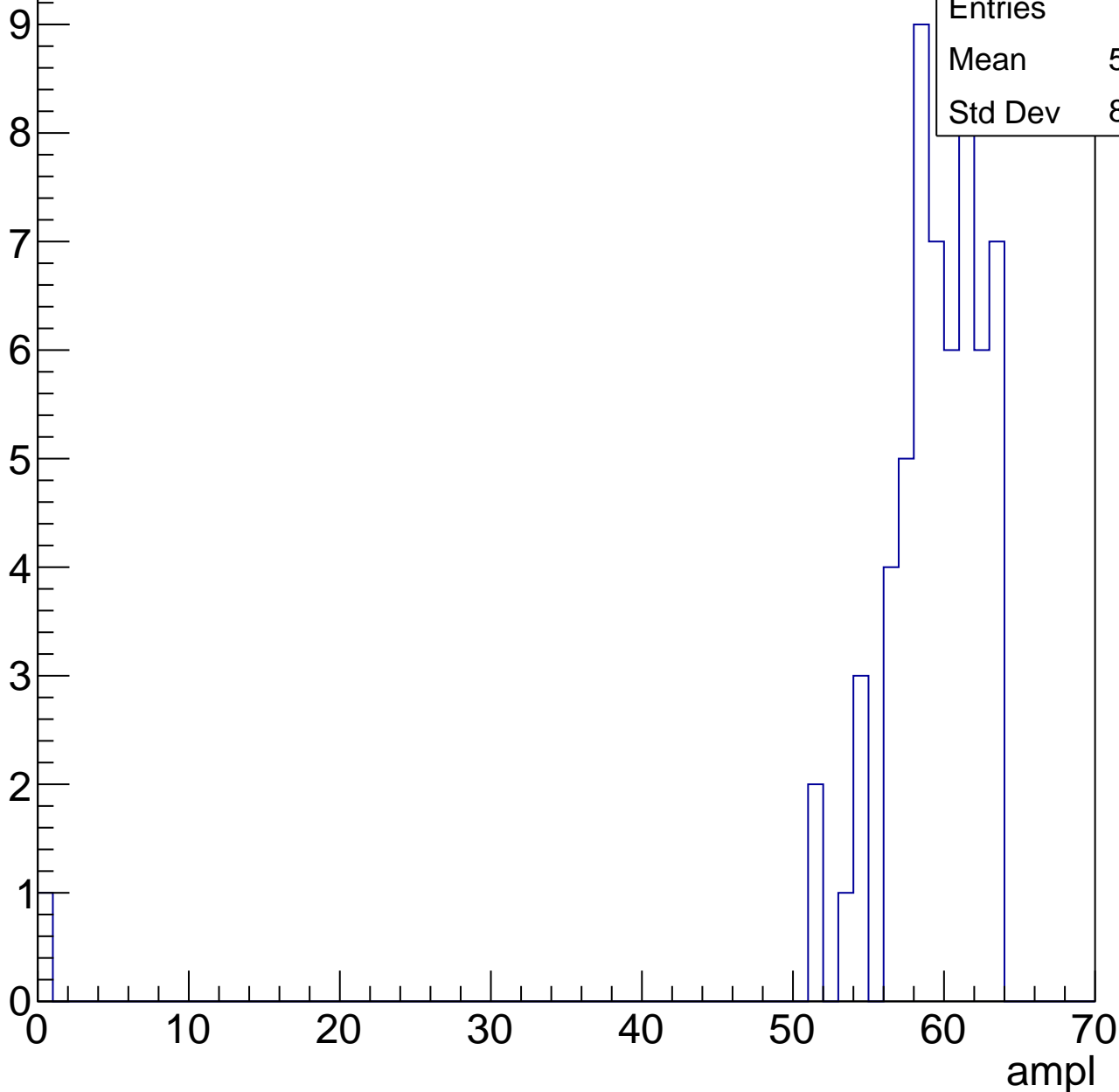


# B1L103S, U26-ch54, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	60
Mean	58.05
Std Dev	8.102



# B1L103S, U26-ch54, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	9
Mean	60.56
Std Dev	2.362

ampl

0 10 20 30 40 50 60 70



# B1L103S, U26-ch54, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	19
Mean	3.263
Std Dev	13.84

Entry



# B1L103S, U26-ch55, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	74
Mean	23.64
Std Dev	11.28

**Gaus mean : 28.7150**

**Gaus Width: 3.3336**

Entry

12

10

8

6

4

2

0

0

10

20

30

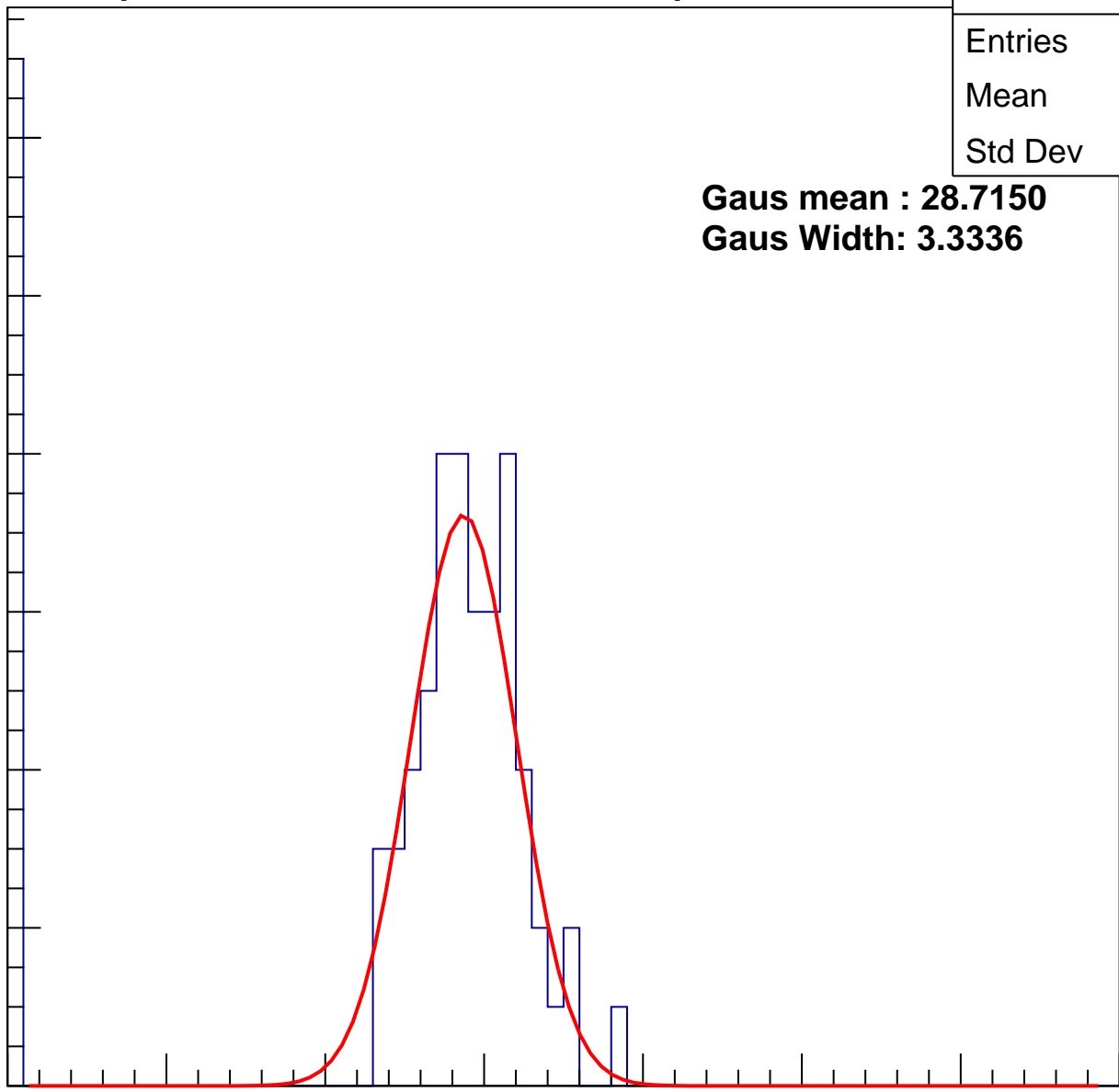
40

50

60

70

ampl



# B1L103S, U26-ch55, adc1

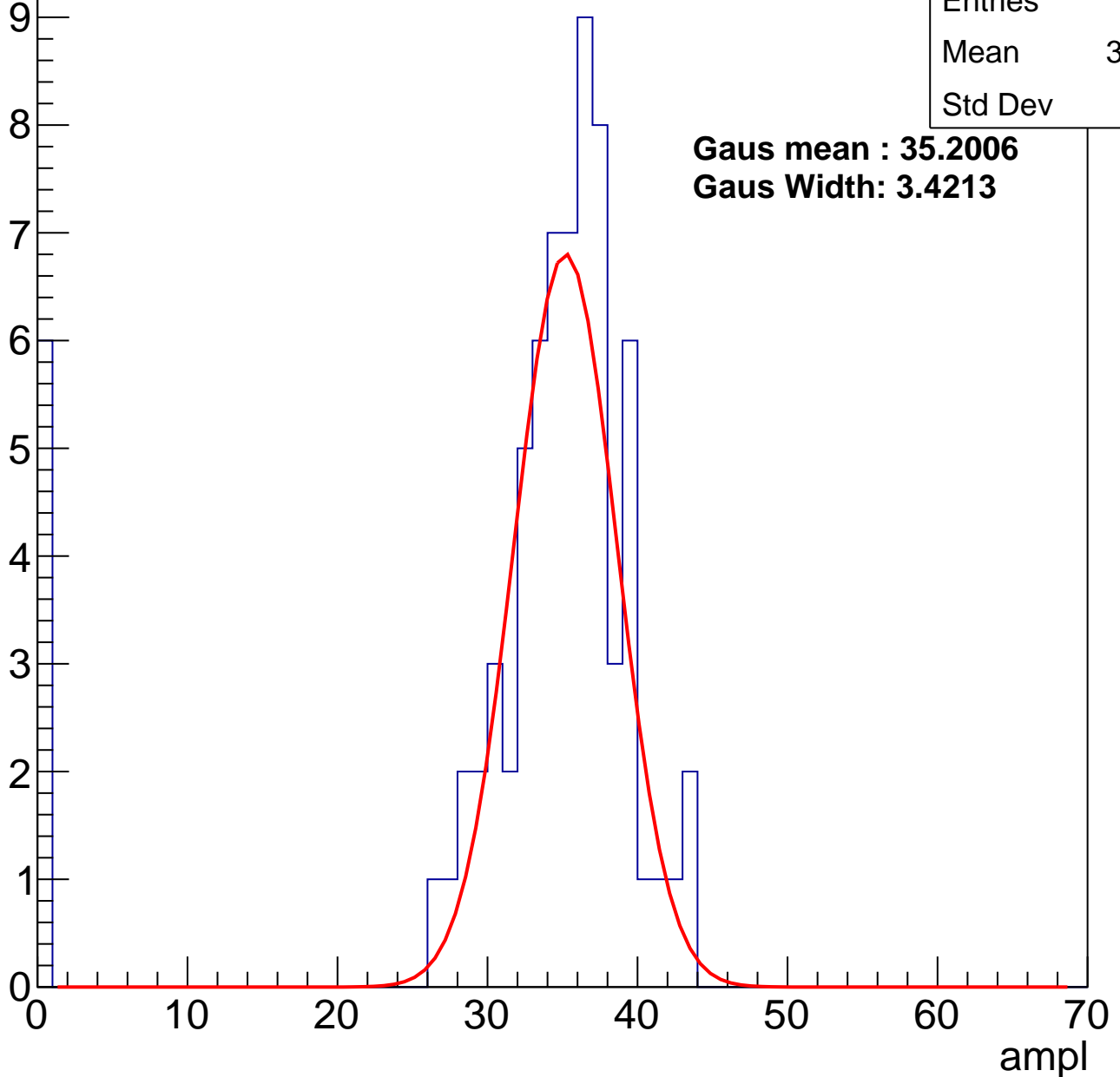
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	73
Mean	32.01
Std Dev	10.2

**Gaus mean : 35.2006**

**Gaus Width: 3.4213**



# B1L103S, U26-ch55, adc2

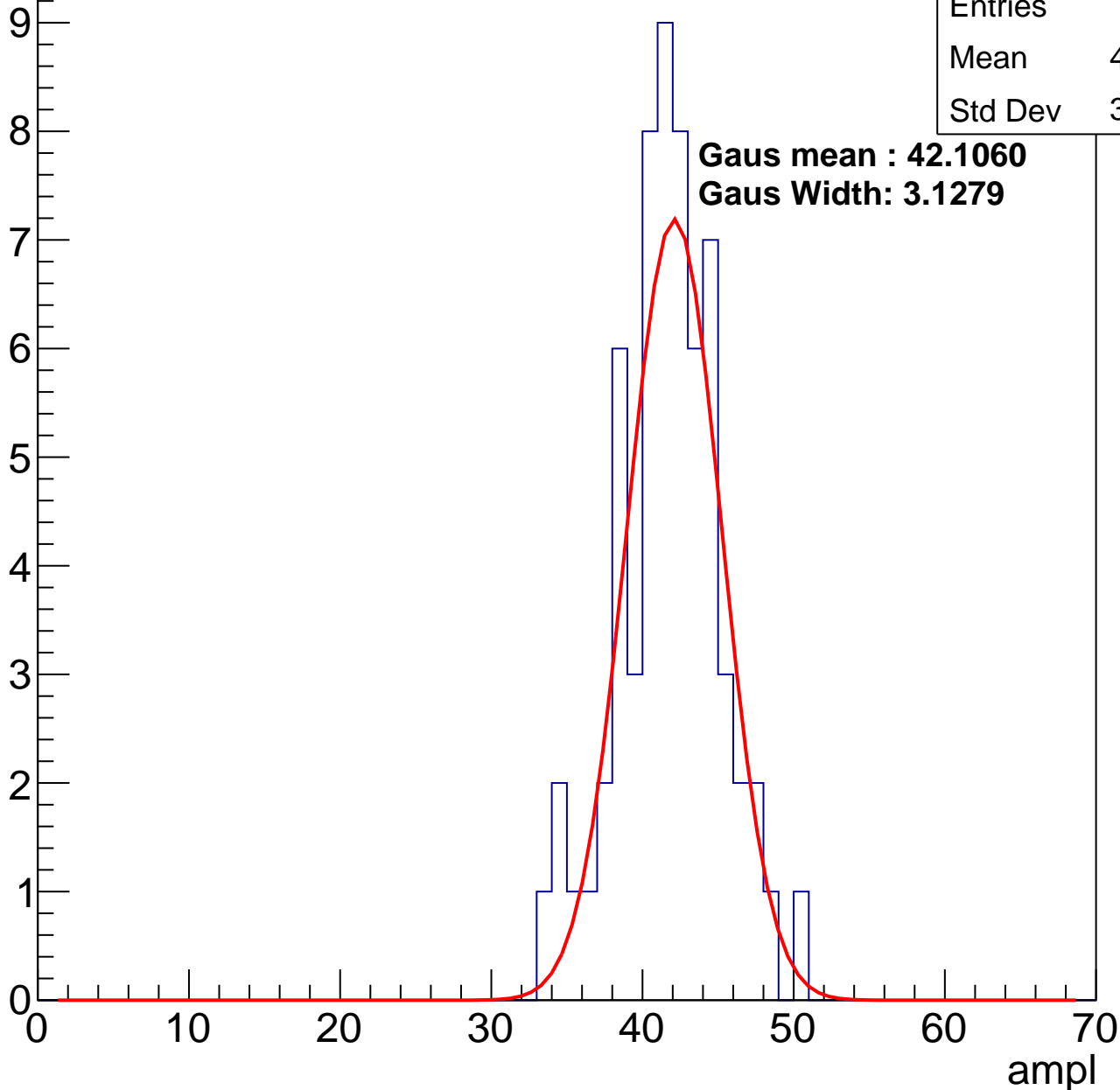
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	63
Mean	41.29
Std Dev	3.378

**Gaus mean : 42.1060**

**Gaus Width: 3.1279**

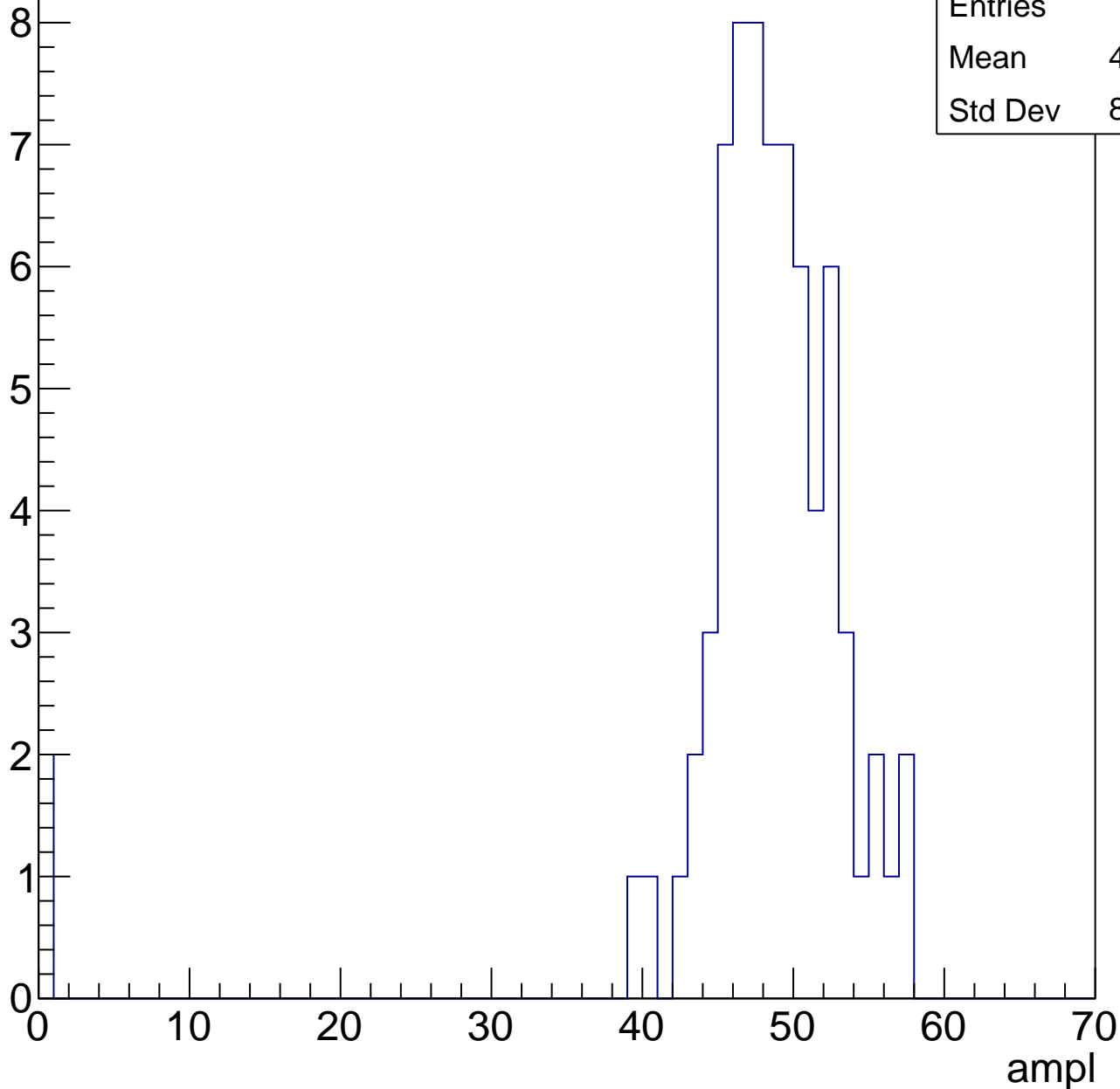


# B1L103S, U26-ch55, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

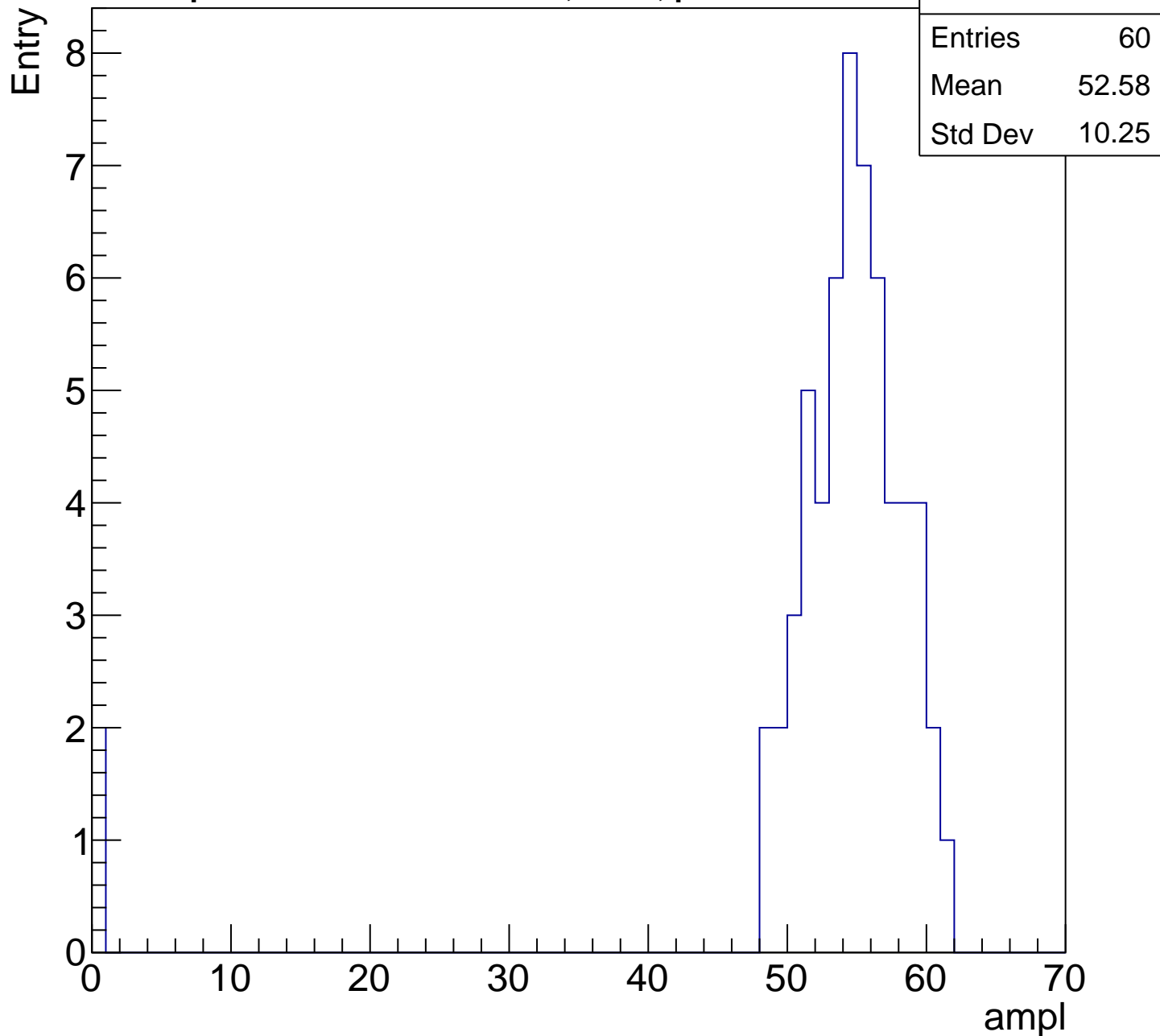
Entry

Entries	72
Mean	47.03
Std Dev	8.756



# B1L103S, U26-ch55, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

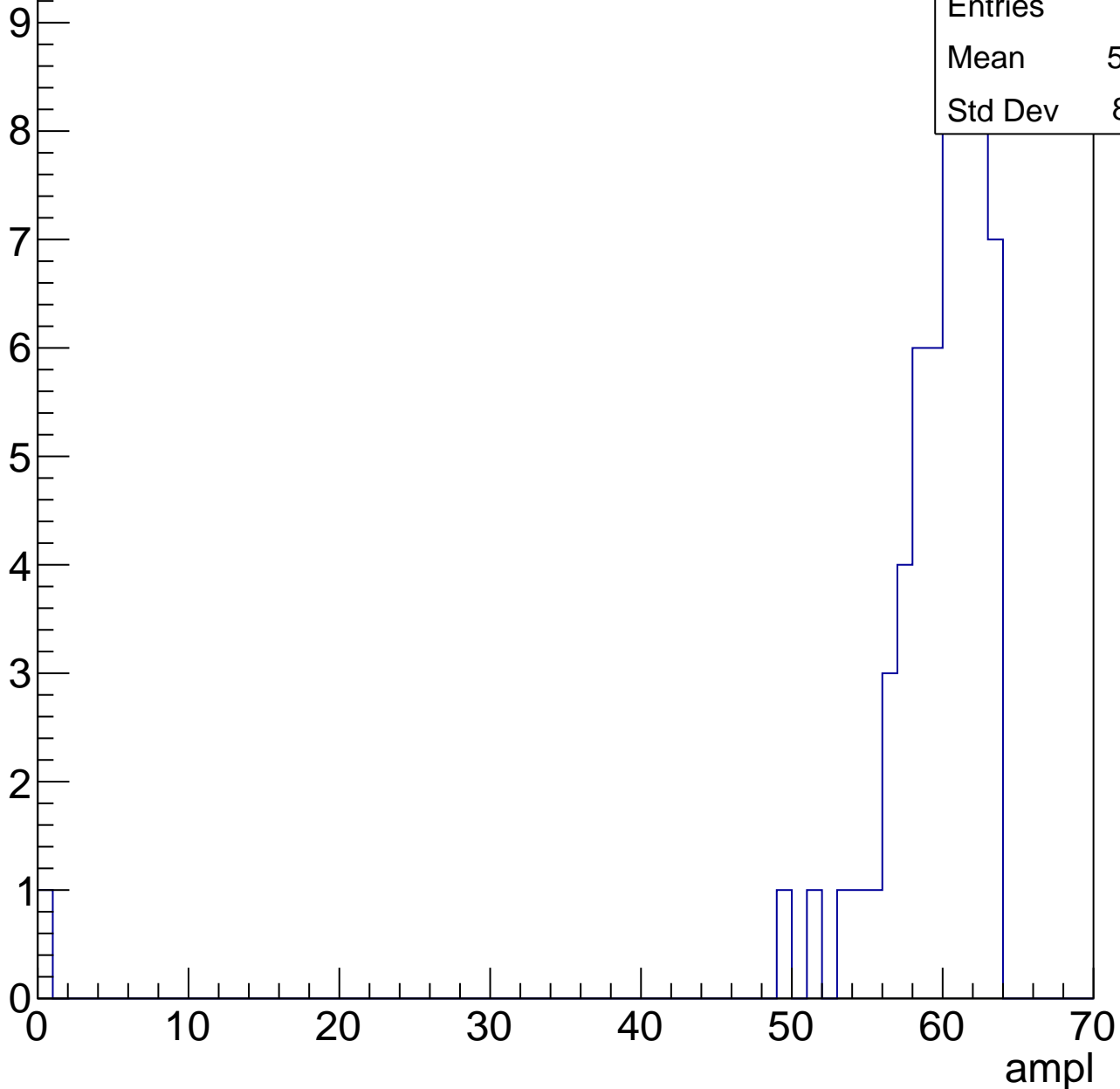


# B1L103S, U26-ch55, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	57
Mean	58.35
Std Dev	8.351



# B1L103S, U26-ch55, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry





# B1L103S, U26-ch55, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

18  
16  
14  
12  
10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

Entries	19
Mean	0
Std Dev	0

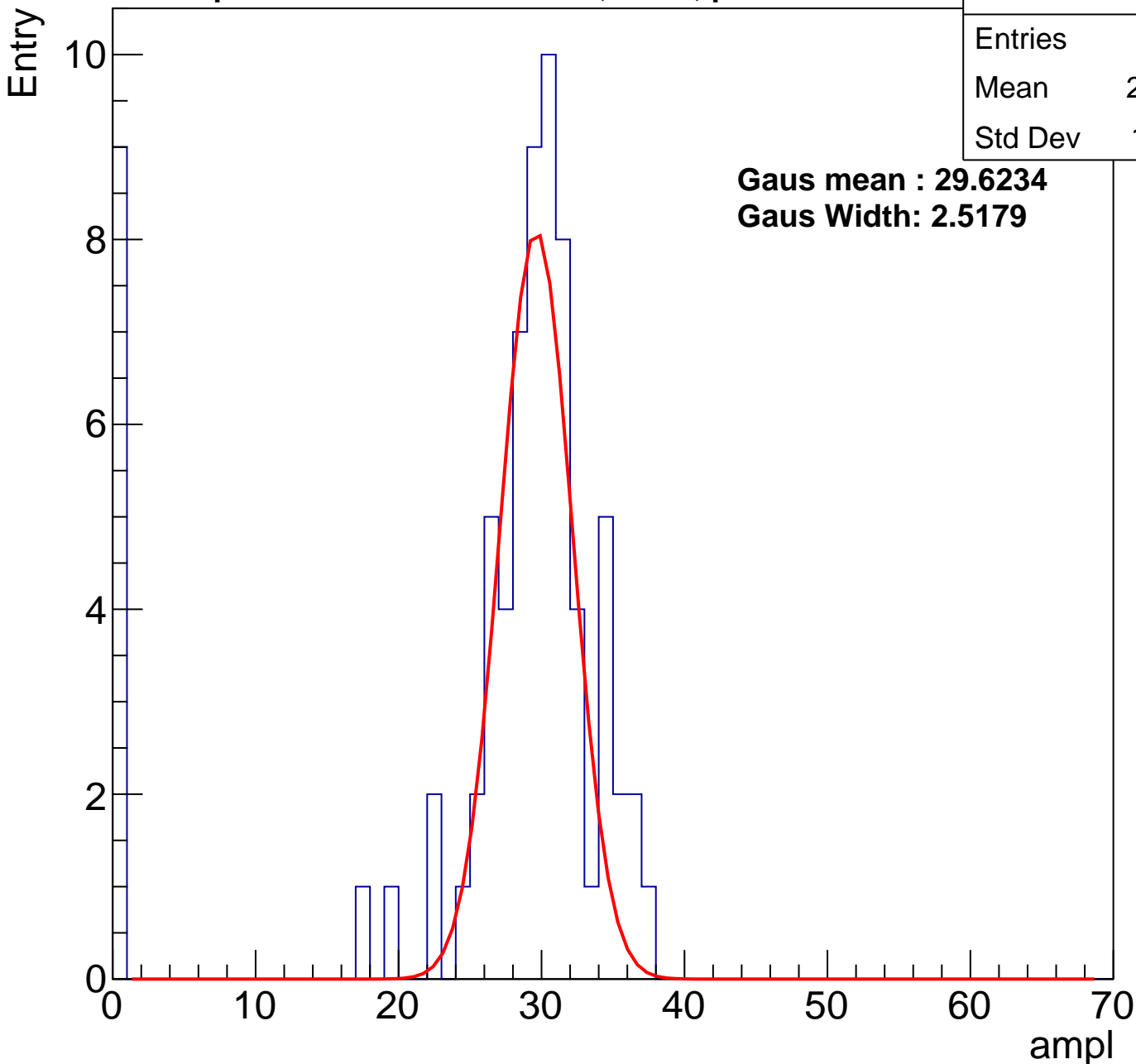
# B1L103S, U26-ch56, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	74
Mean	25.77
Std Dev	10.21

**Gaus mean : 29.6234**

**Gaus Width: 2.5179**



# B1L103S, U26-ch56, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	84
Mean	31.56
Std Dev	12.57

**Gaus mean : 37.0503**

**Gaus Width: 3.1900**

Entry

10

8

6

4

2

0

0

10

20

30

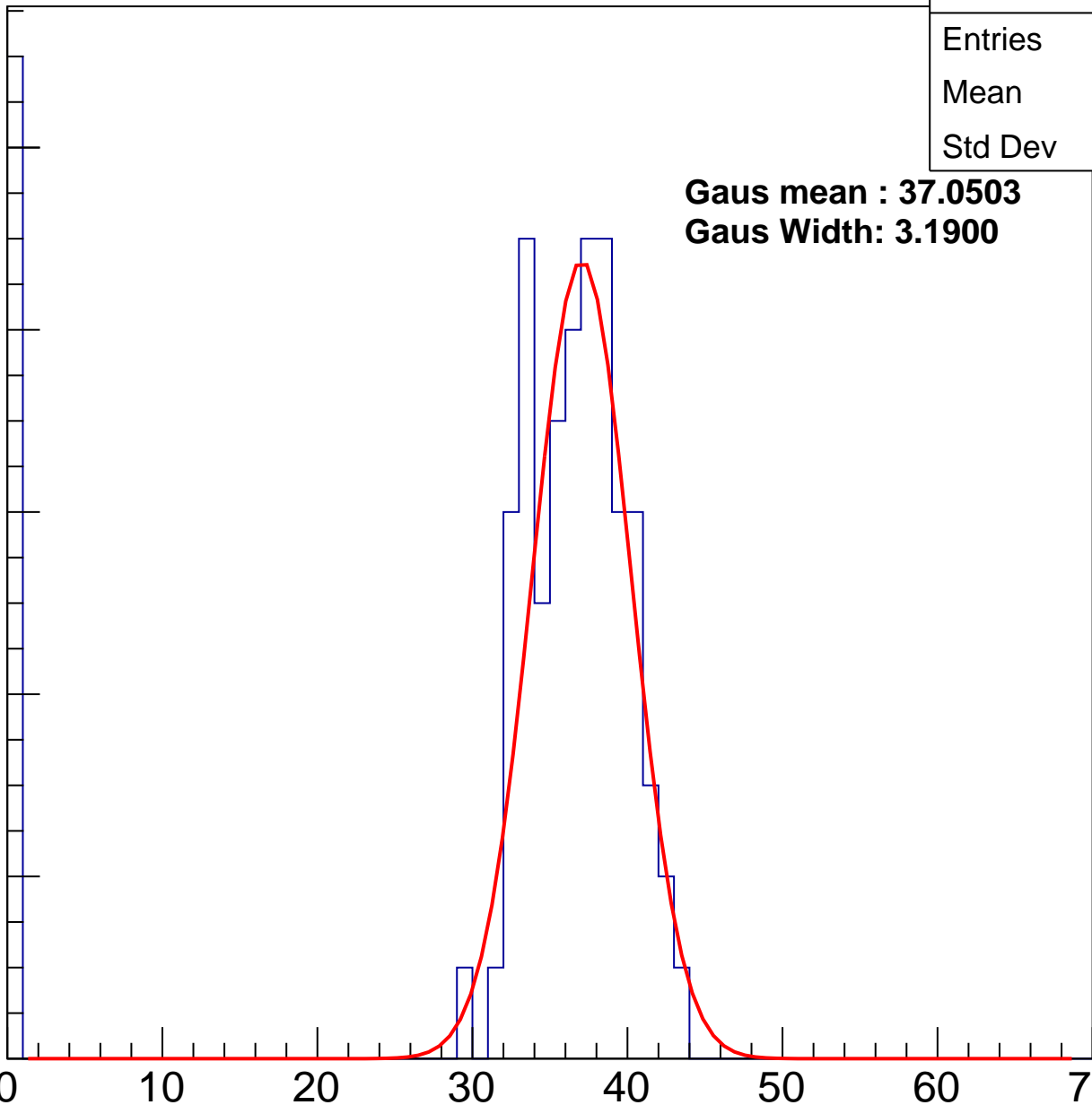
40

50

60

70

ampl



# B1L103S, U26-ch56, adc2

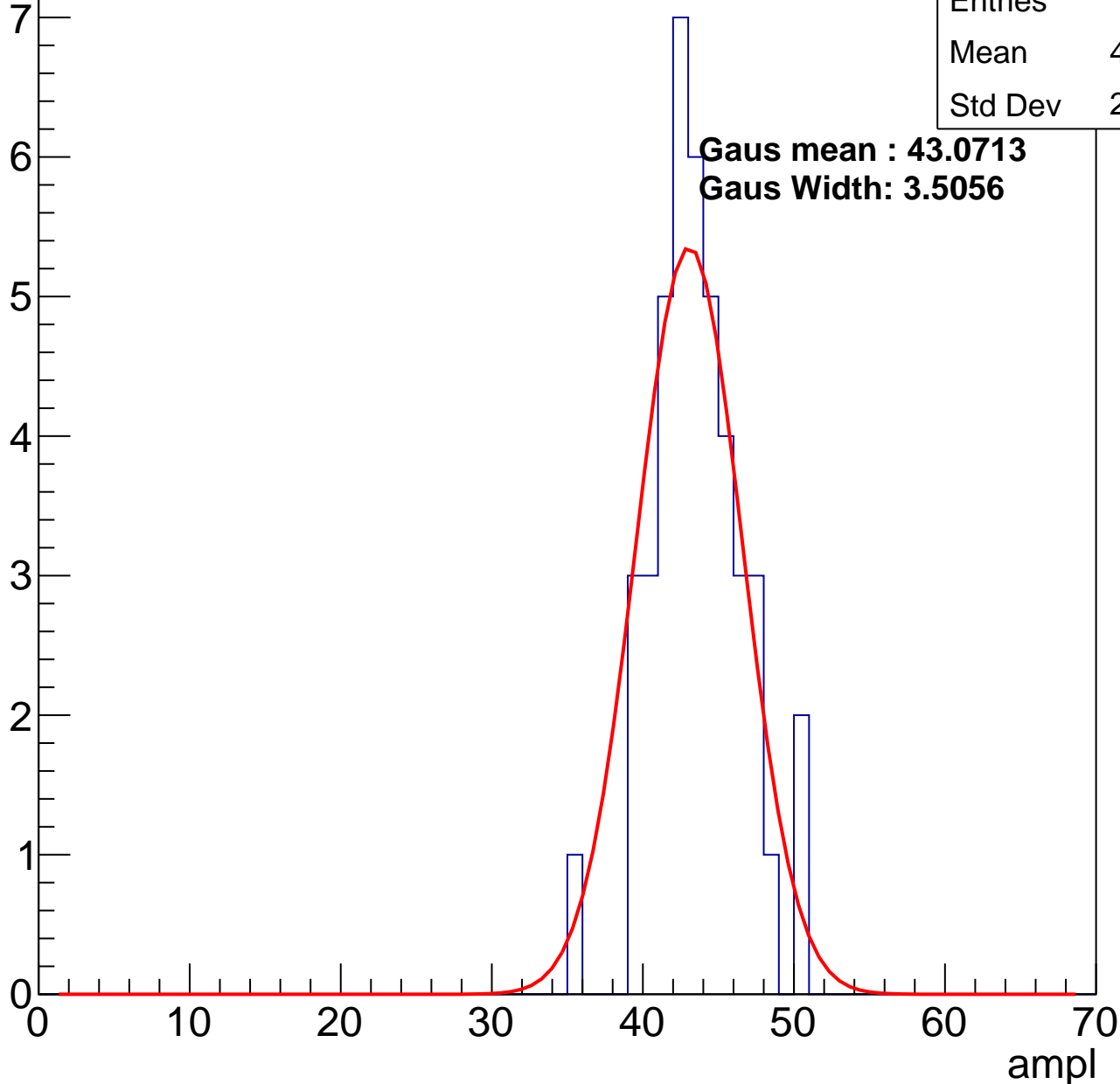
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	43
Mean	43.16
Std Dev	2.988

**Gaus mean : 43.0713**

**Gaus Width: 3.5056**

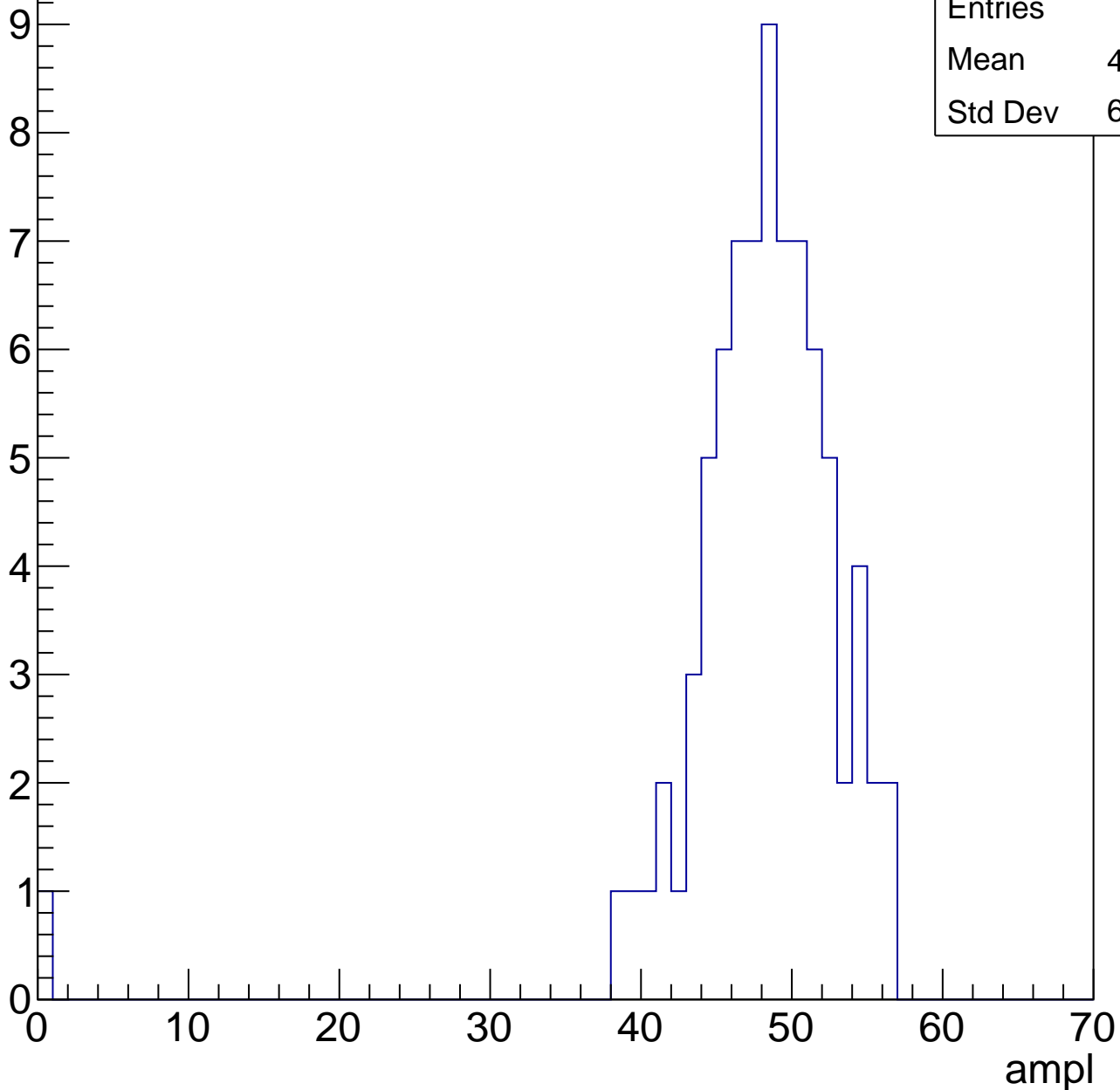


# B1L103S, U26-ch56, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	79
Mean	47.42
Std Dev	6.646

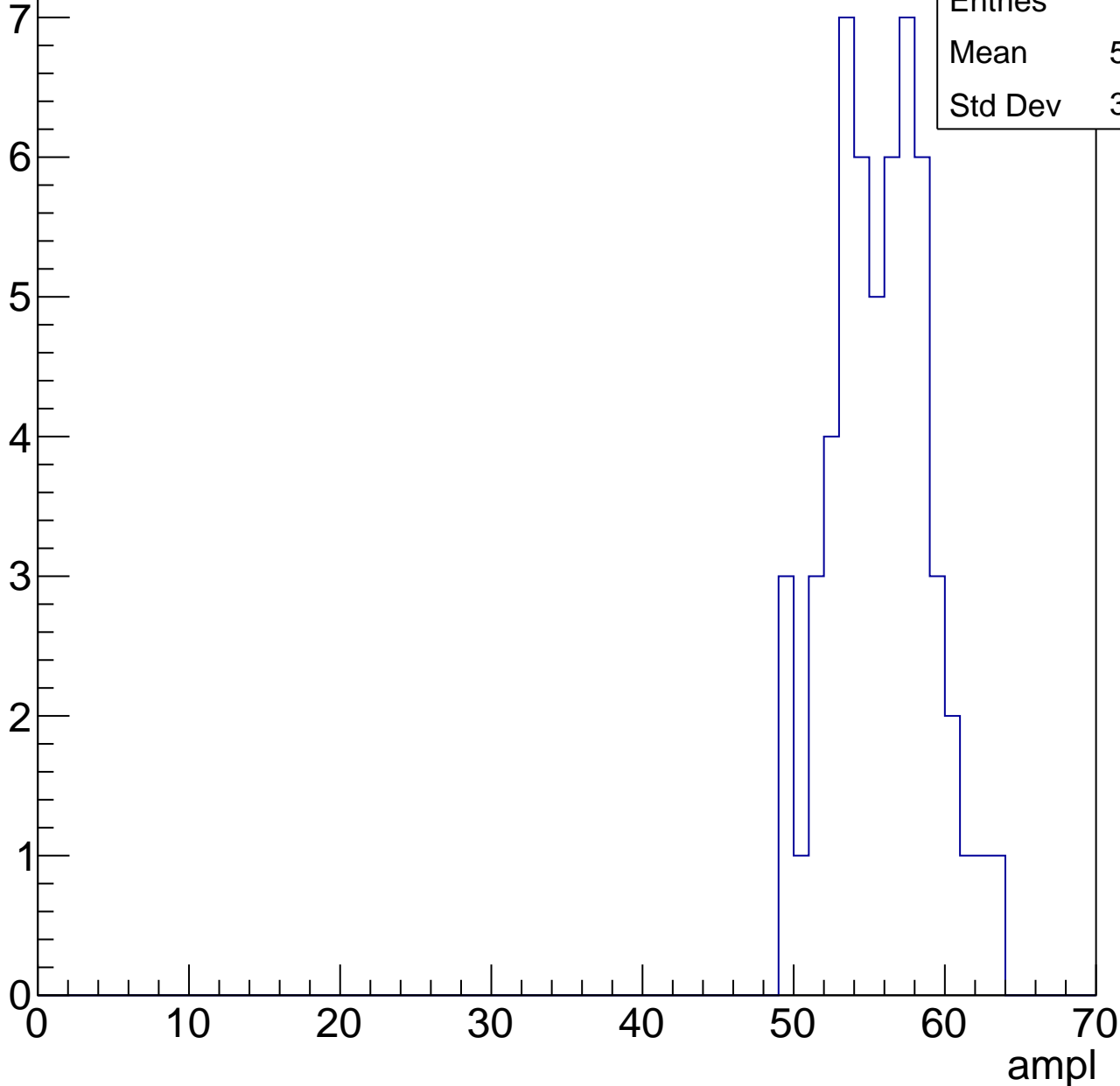


# B1L103S, U26-ch56, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	56
Mean	55.25
Std Dev	3.225

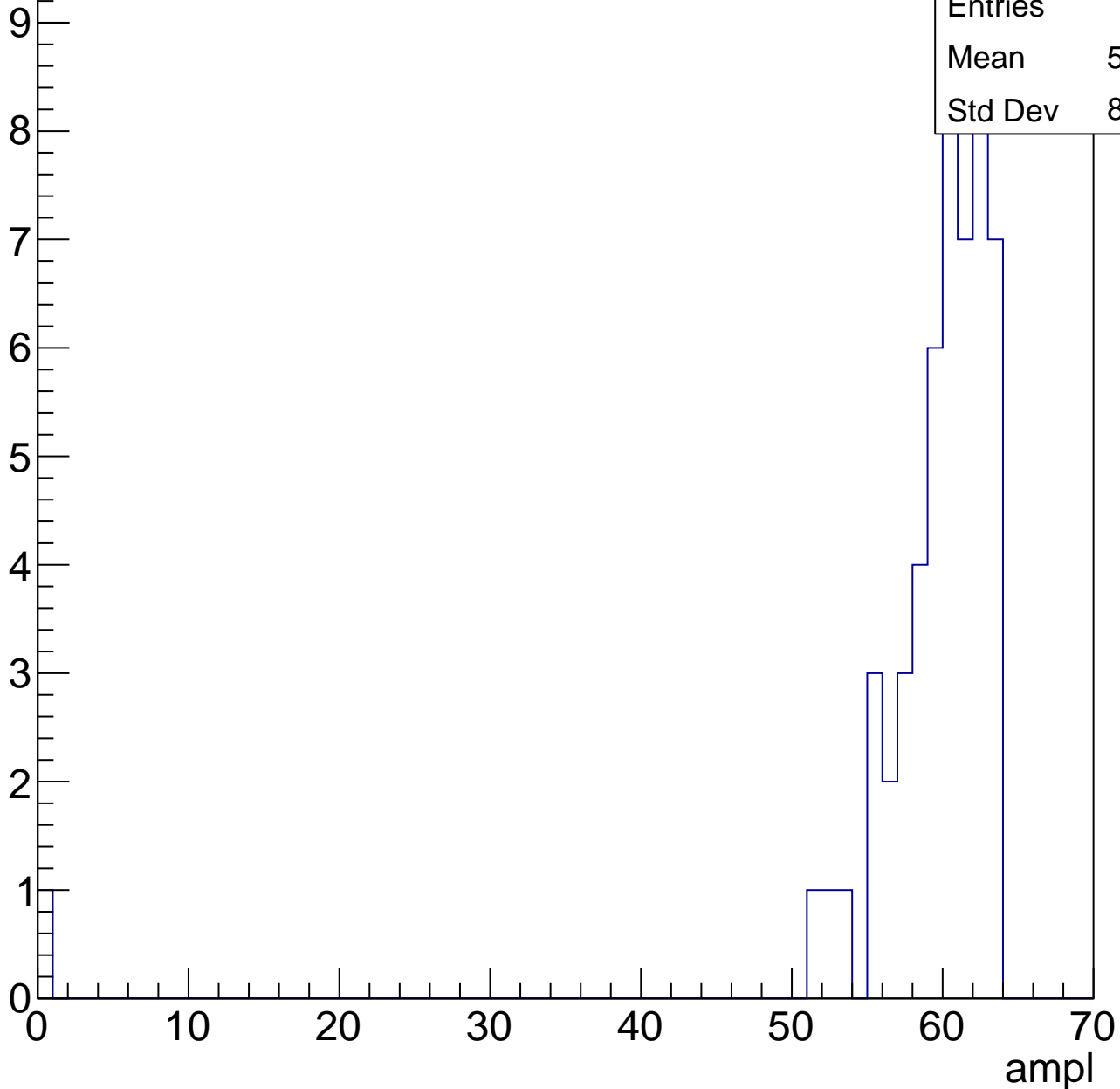


# B1L103S, U26-ch56, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

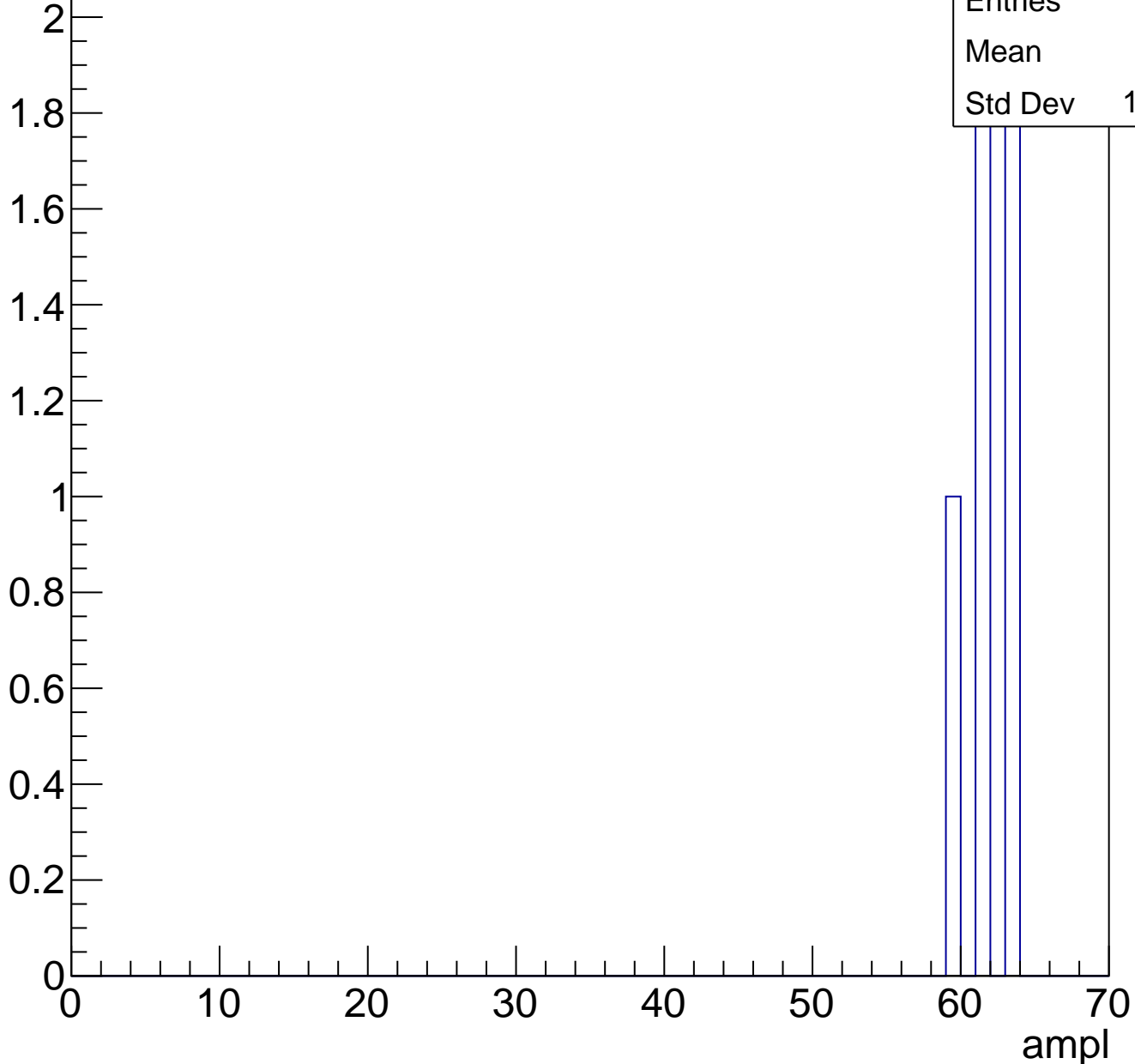
Entries	53
Mean	58.42
Std Dev	8.603



# B1L103S, U26-ch56, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry





# B1L103S, U26-ch56, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



Entries	18
Mean	0
Std Dev	0

# B1L103S, U26-ch57, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	67
Mean	24.27
Std Dev	11.09

**Gaus mean : 29.3823**

**Gaus Width: 3.3487**

10

8

6

4

2

0

0

10

20

30

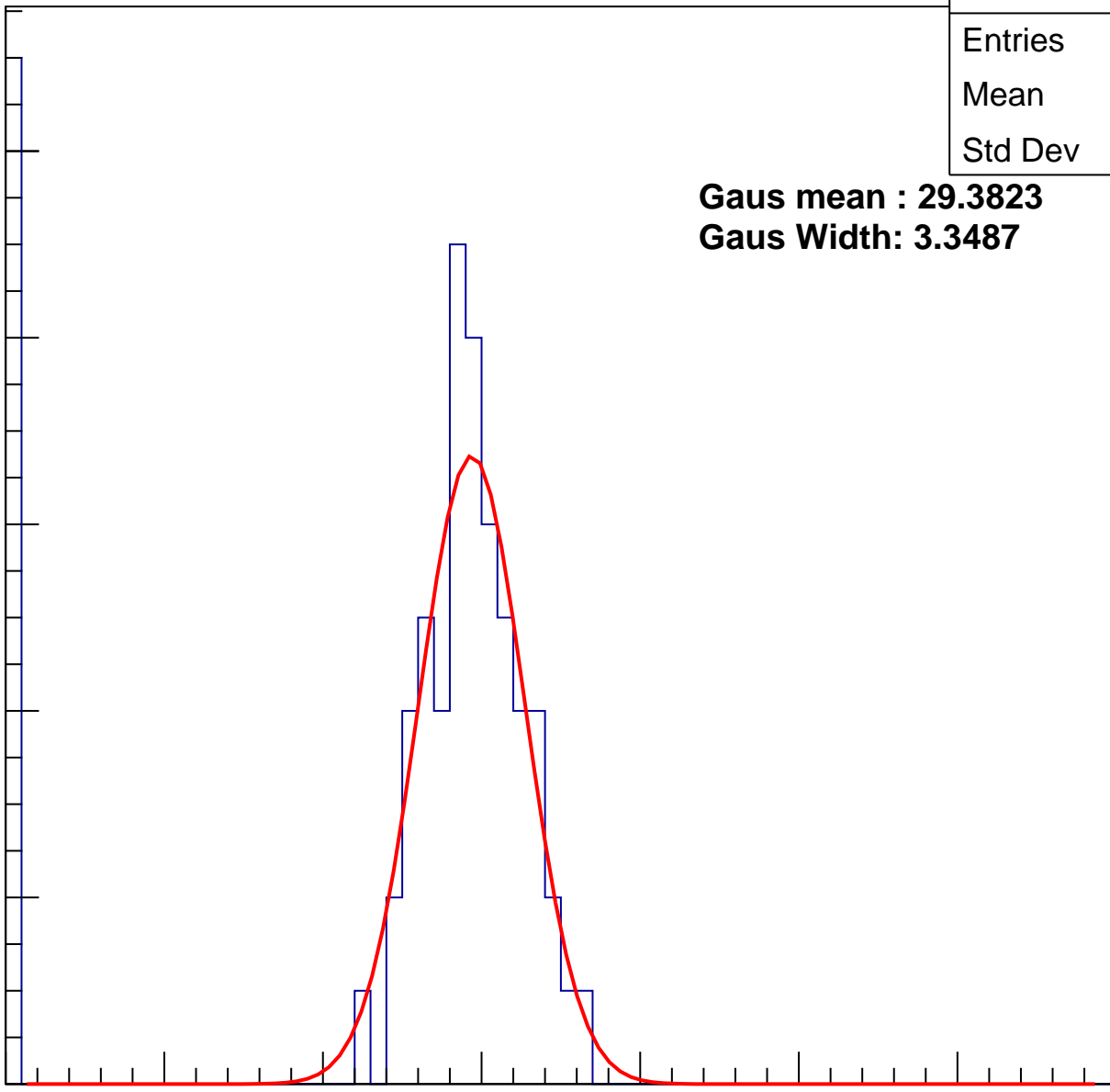
40

50

60

70

ampl



# B1L103S, U26-ch57, adc1

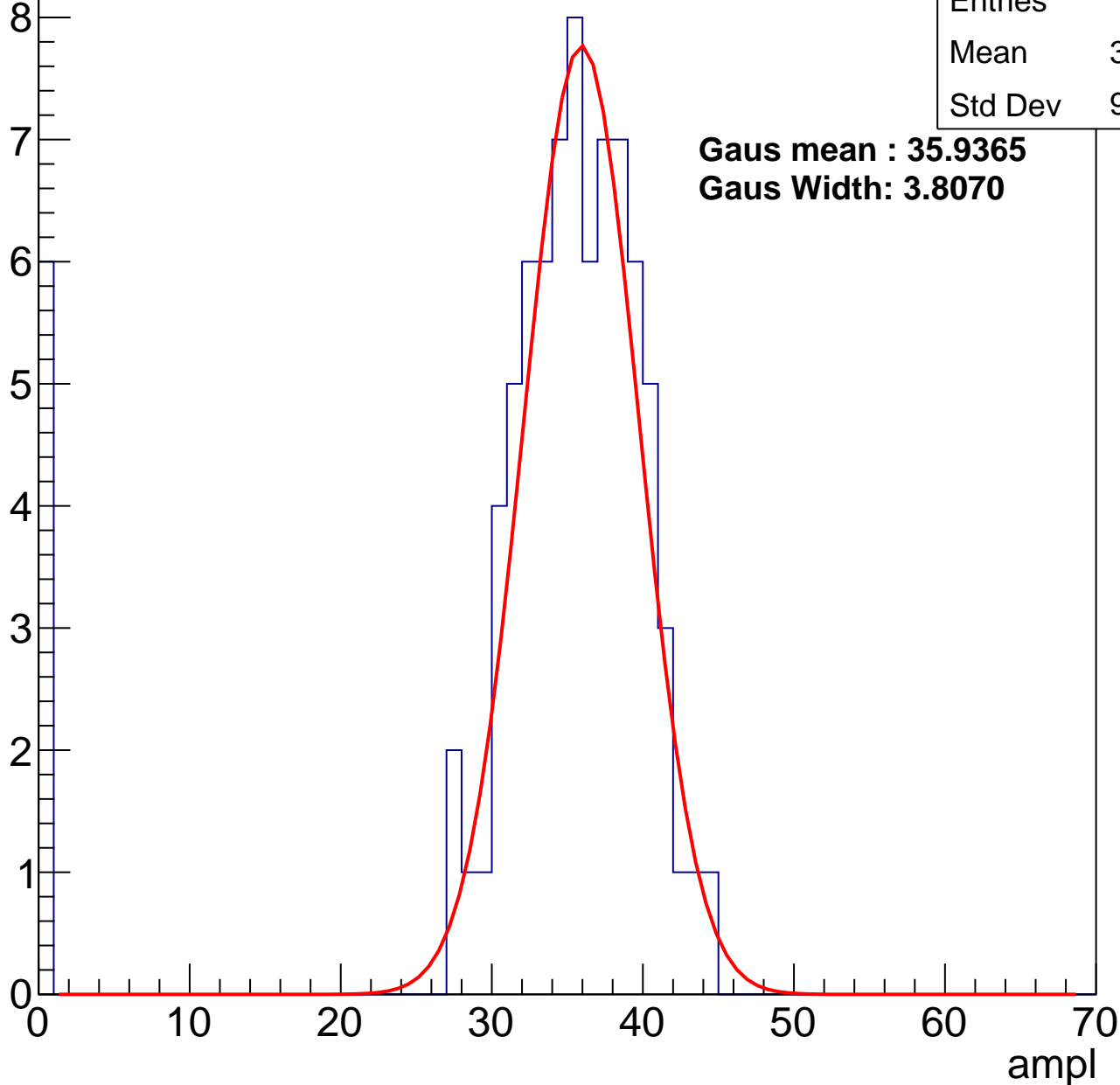
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	83
Mean	32.78
Std Dev	9.842

**Gaus mean : 35.9365**

**Gaus Width: 3.8070**



# B1L103S, U26-ch57, adc2

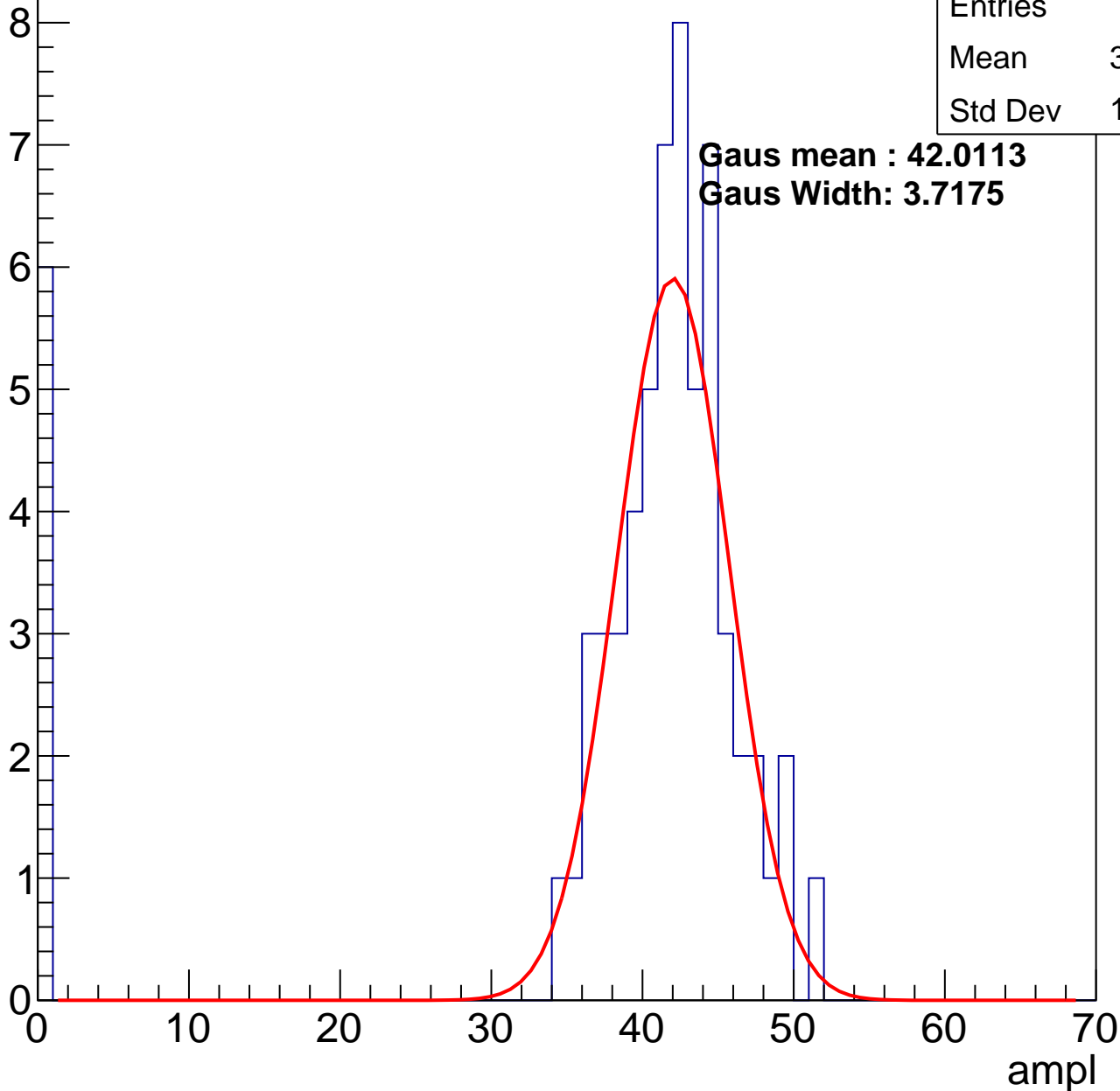
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	64
Mean	37.84
Std Dev	12.65

**Gaus mean : 42.0113**

**Gaus Width: 3.7175**

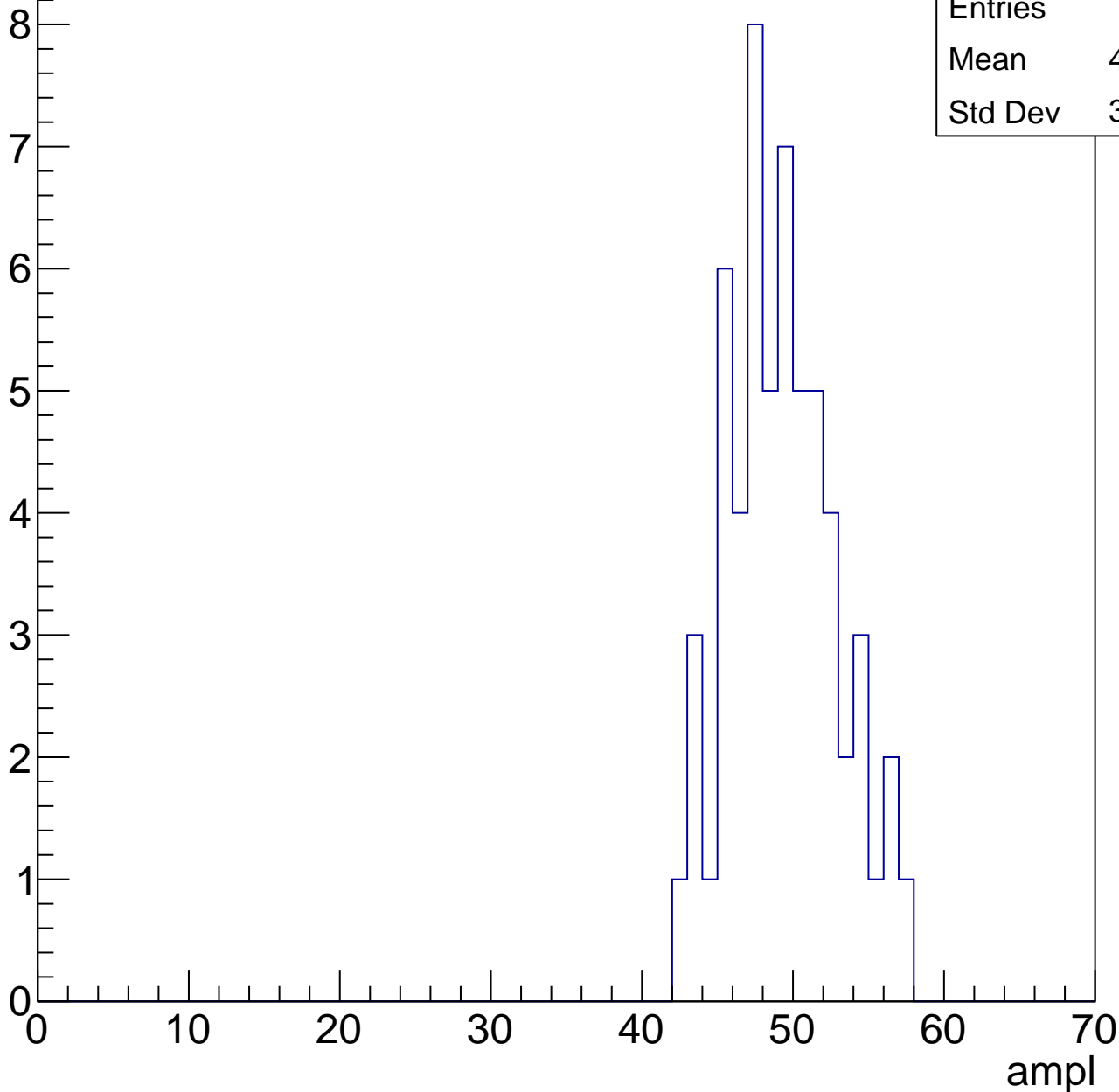


# B1L103S, U26-ch57, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	58
Mean	48.84
Std Dev	3.513

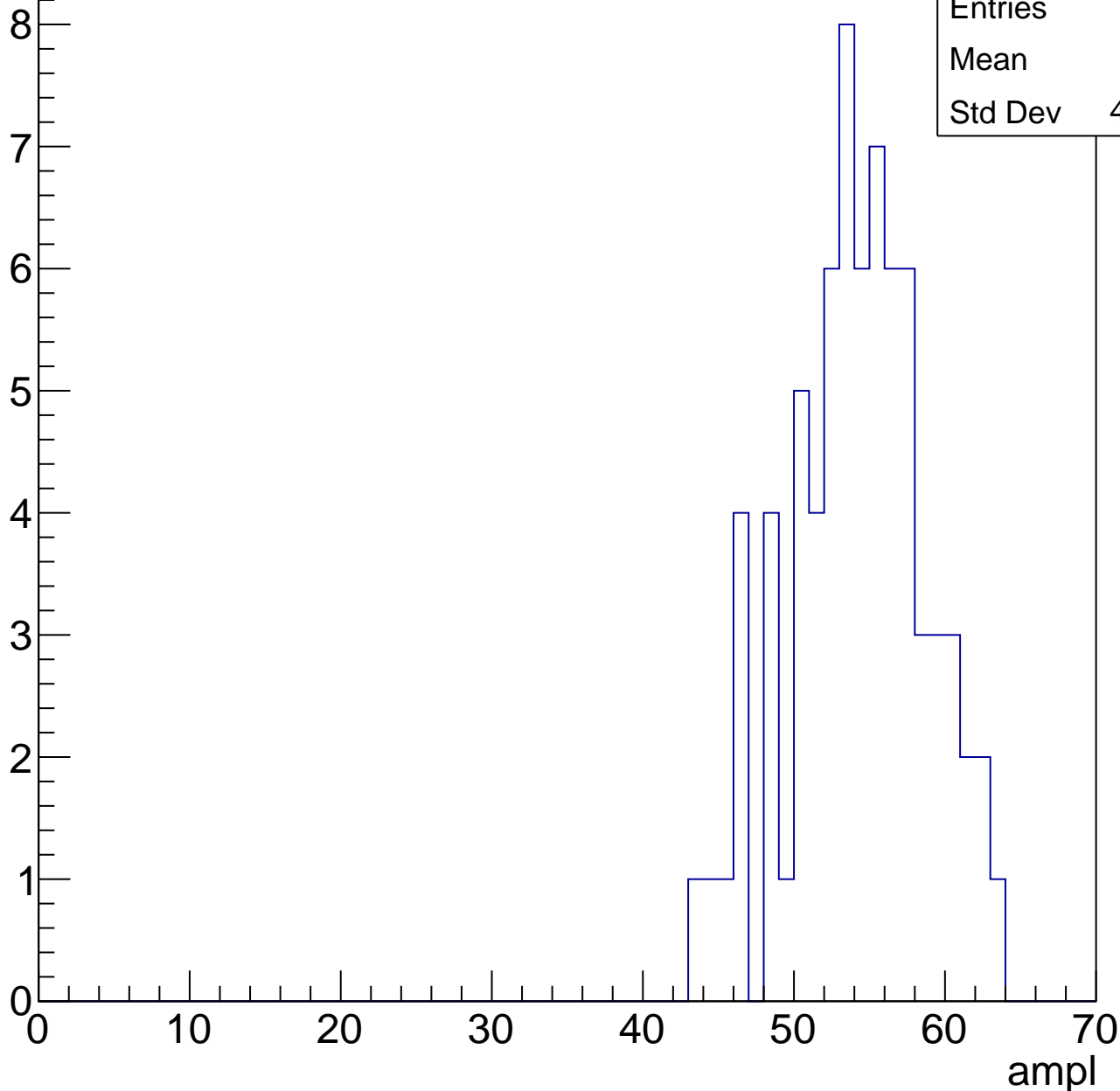


# B1L103S, U26-ch57, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

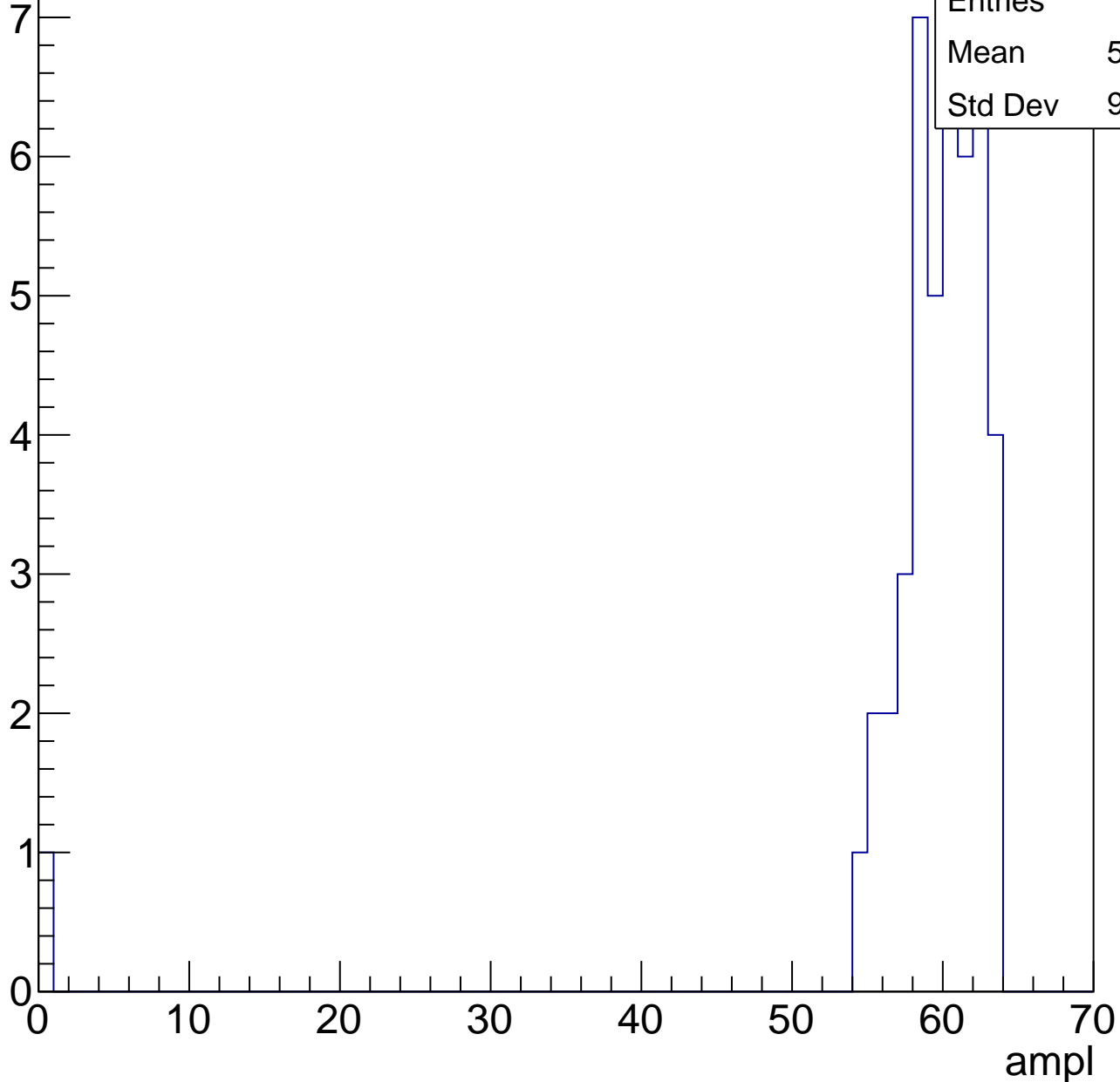
Entries	74
Mean	53.7
Std Dev	4.489



# B1L103S, U26-ch57, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

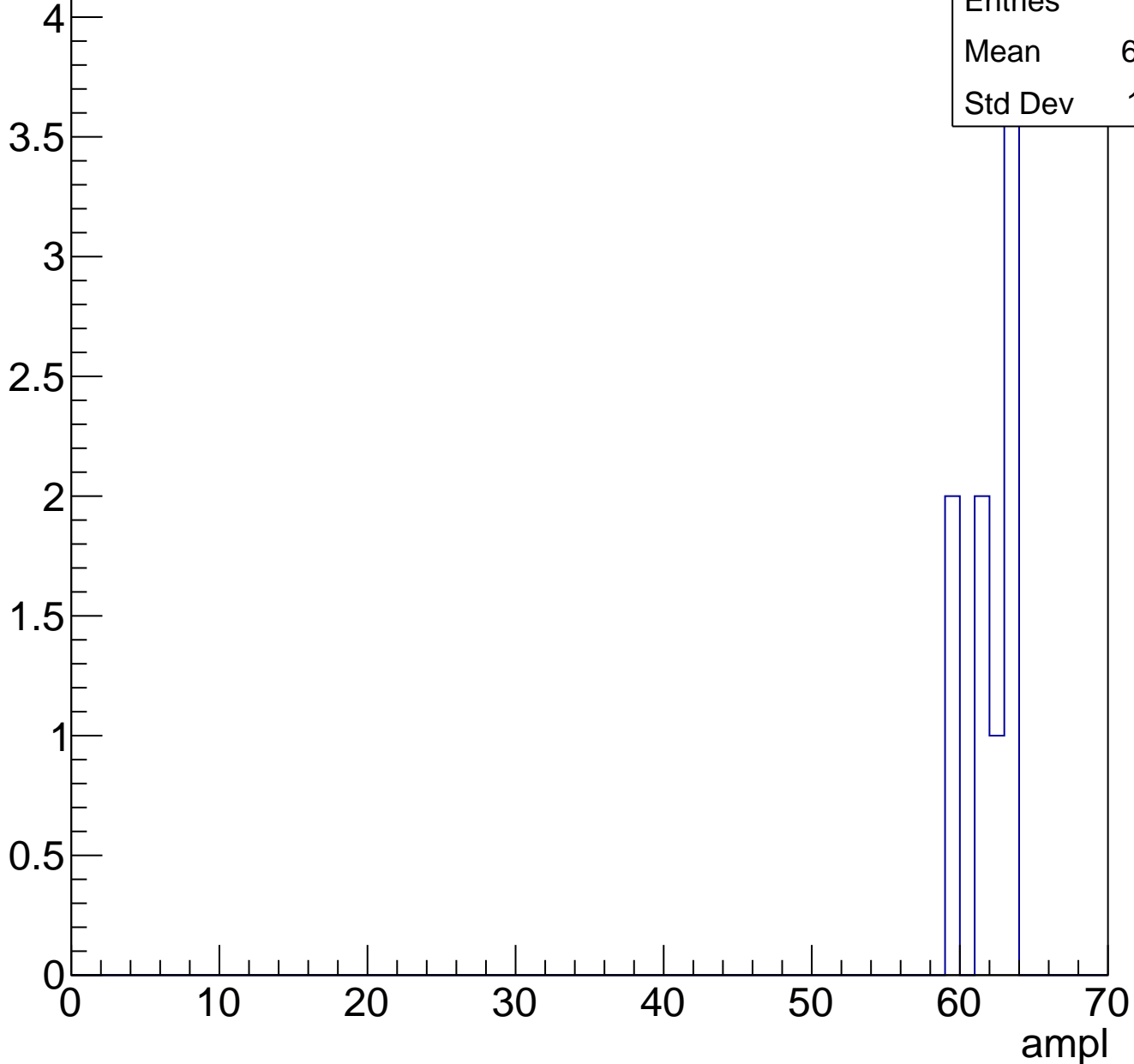
Entry



# B1L103S, U26-ch57, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



Entries	9
Mean	61.56
Std Dev	1.571

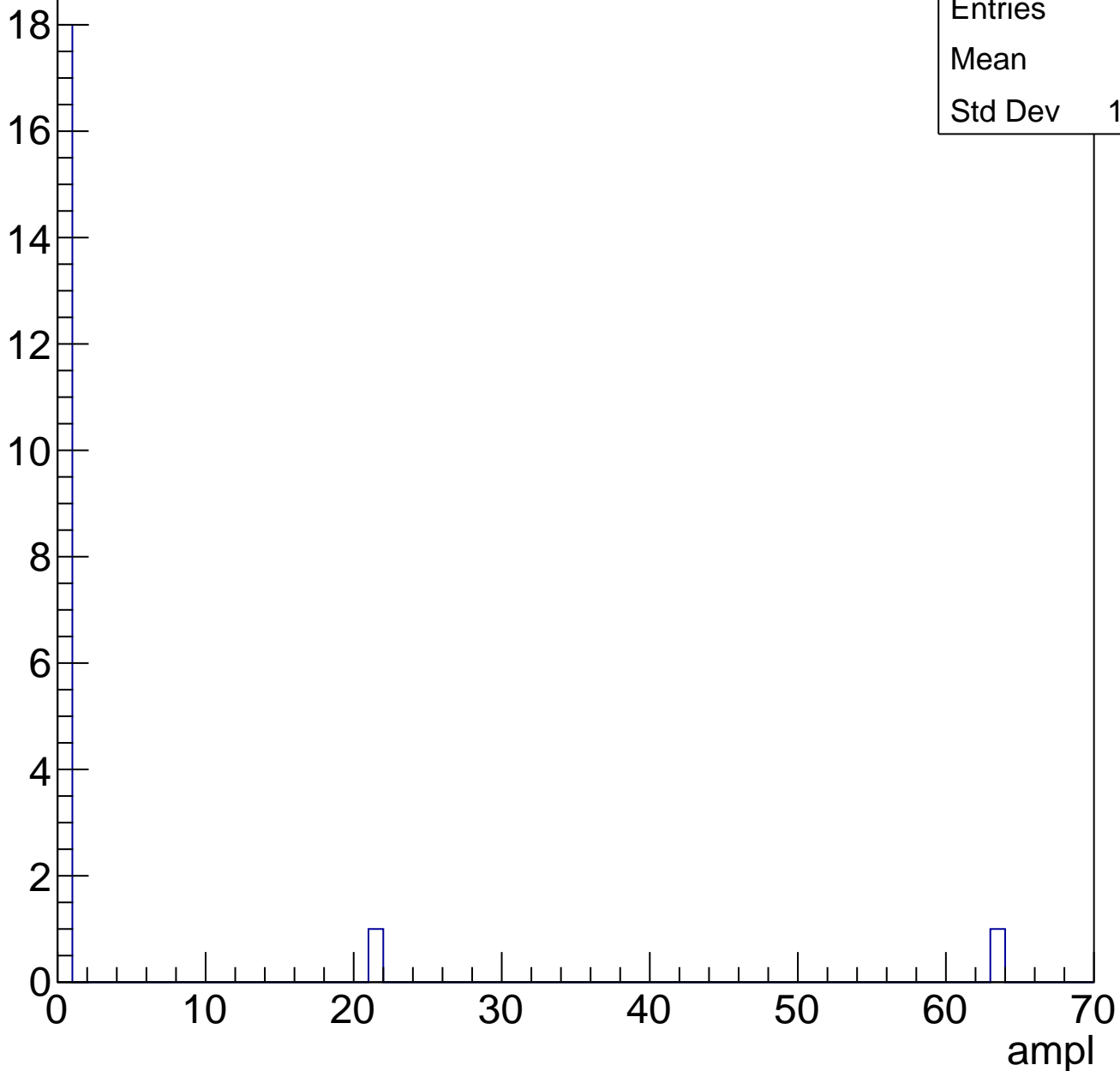


# B1L103S, U26-ch57, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	20
Mean	4.2
Std Dev	14.24

Entry



# B1L103S, U26-ch58, adc0

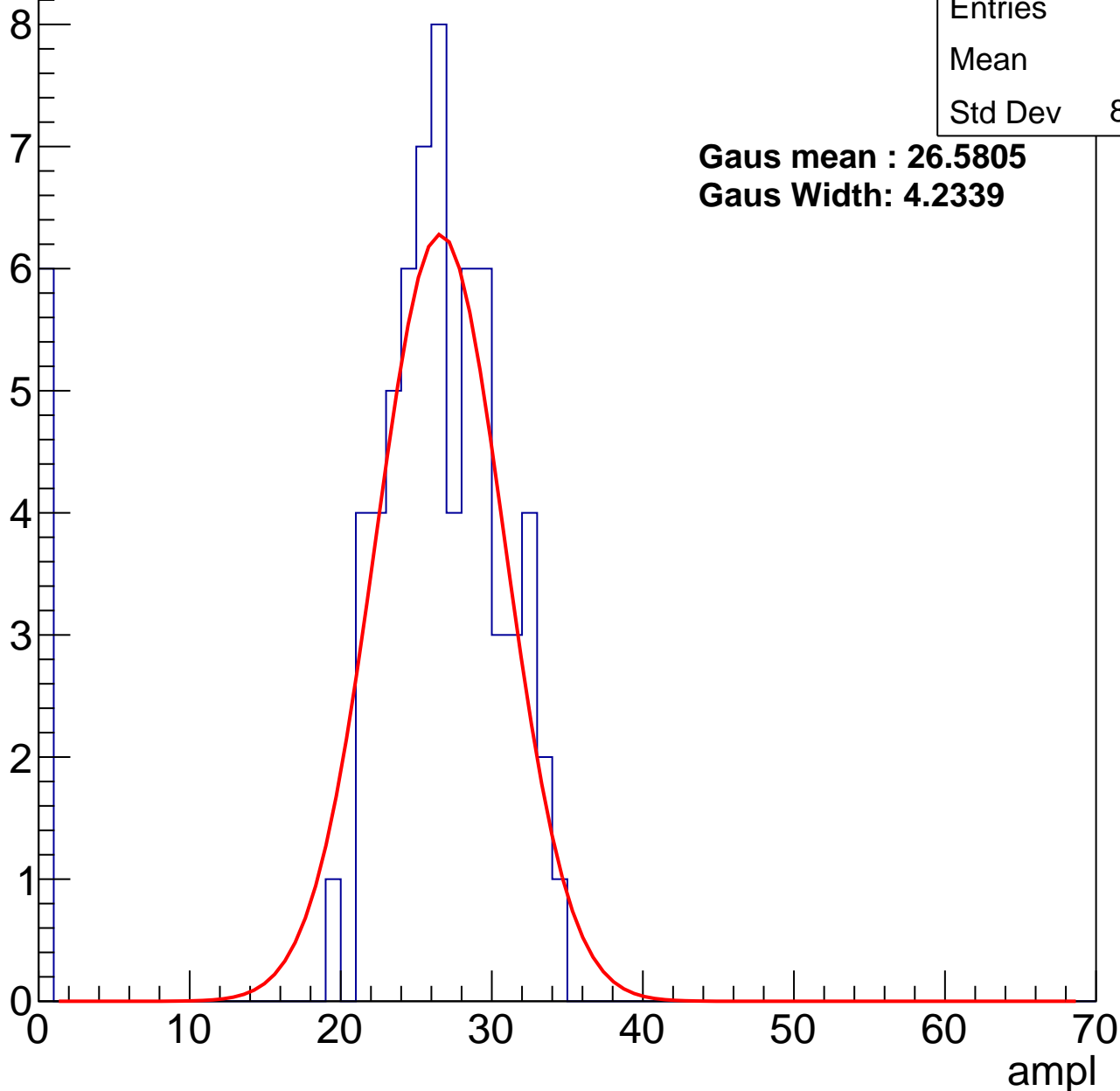
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	70
Mean	24.2
Std Dev	8.132

**Gaus mean : 26.5805**

**Gaus Width: 4.2339**



# B1L103S, U26-ch58, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	85
Mean	31.28
Std Dev	8.58

**Gaus mean : 33.4334**

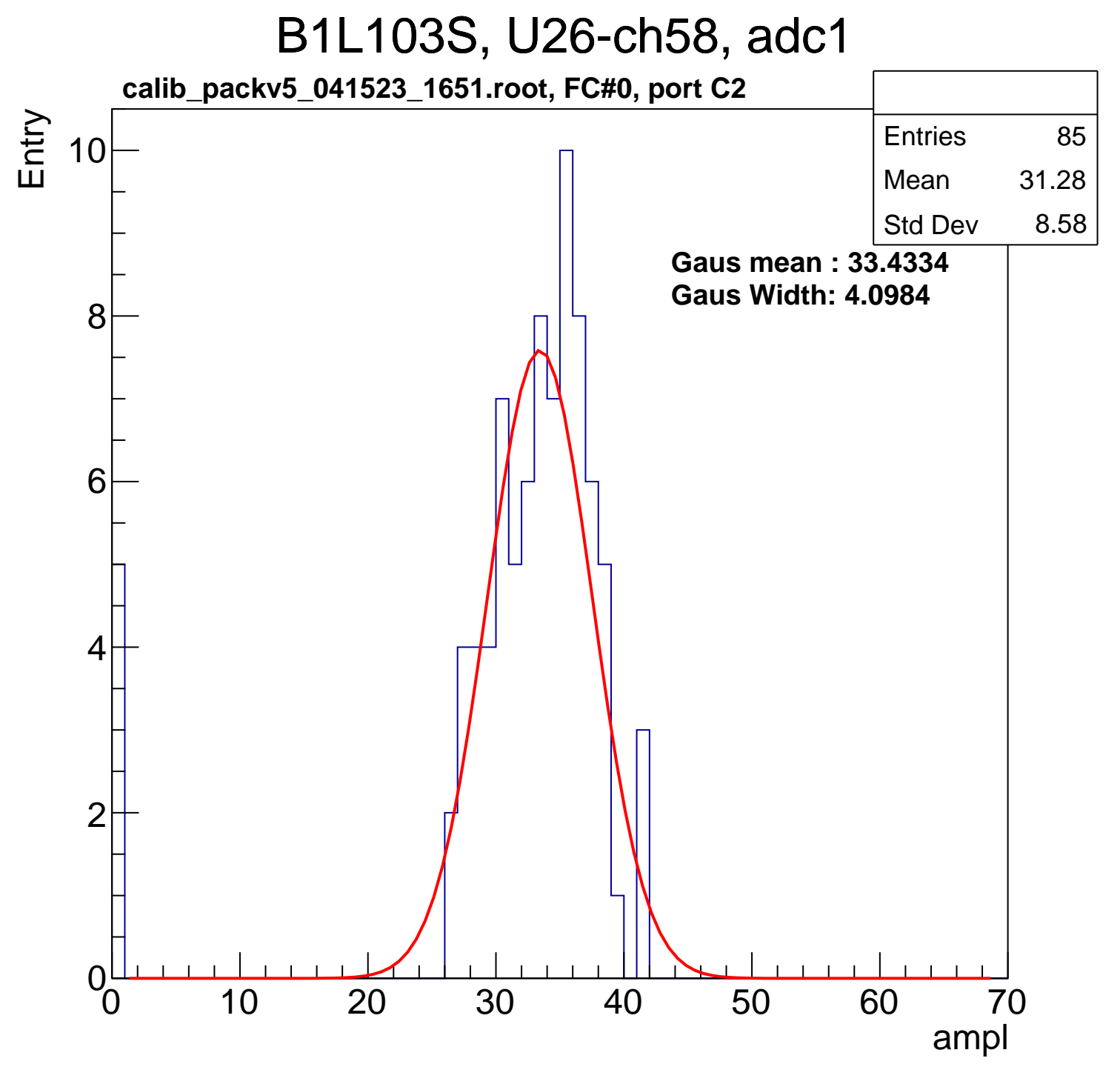
**Gaus Width: 4.0984**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U26-ch58, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	81
Mean	36.74
Std Dev	13.42

**Gaus mean : 41.5827**

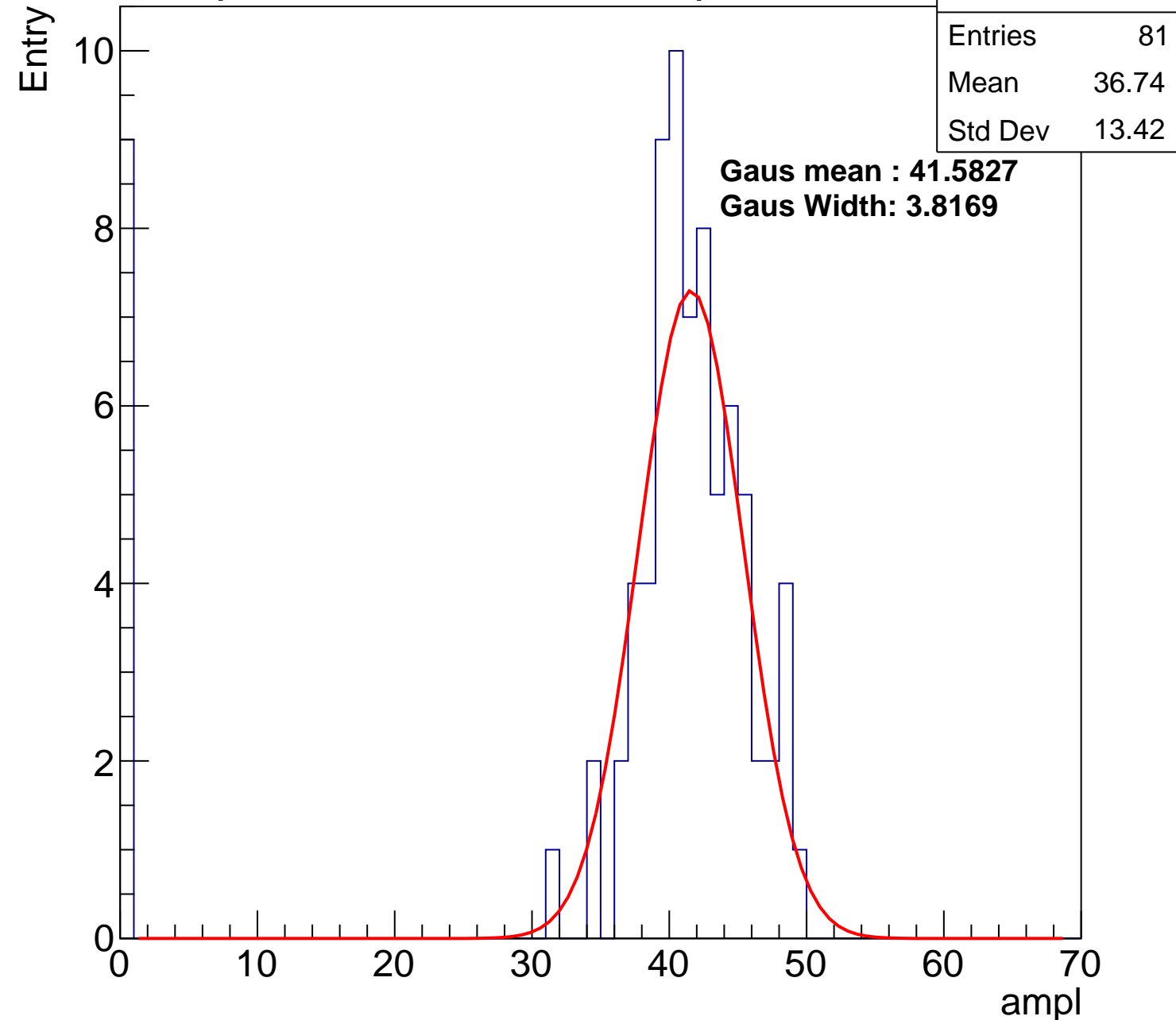
**Gaus Width: 3.8169**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

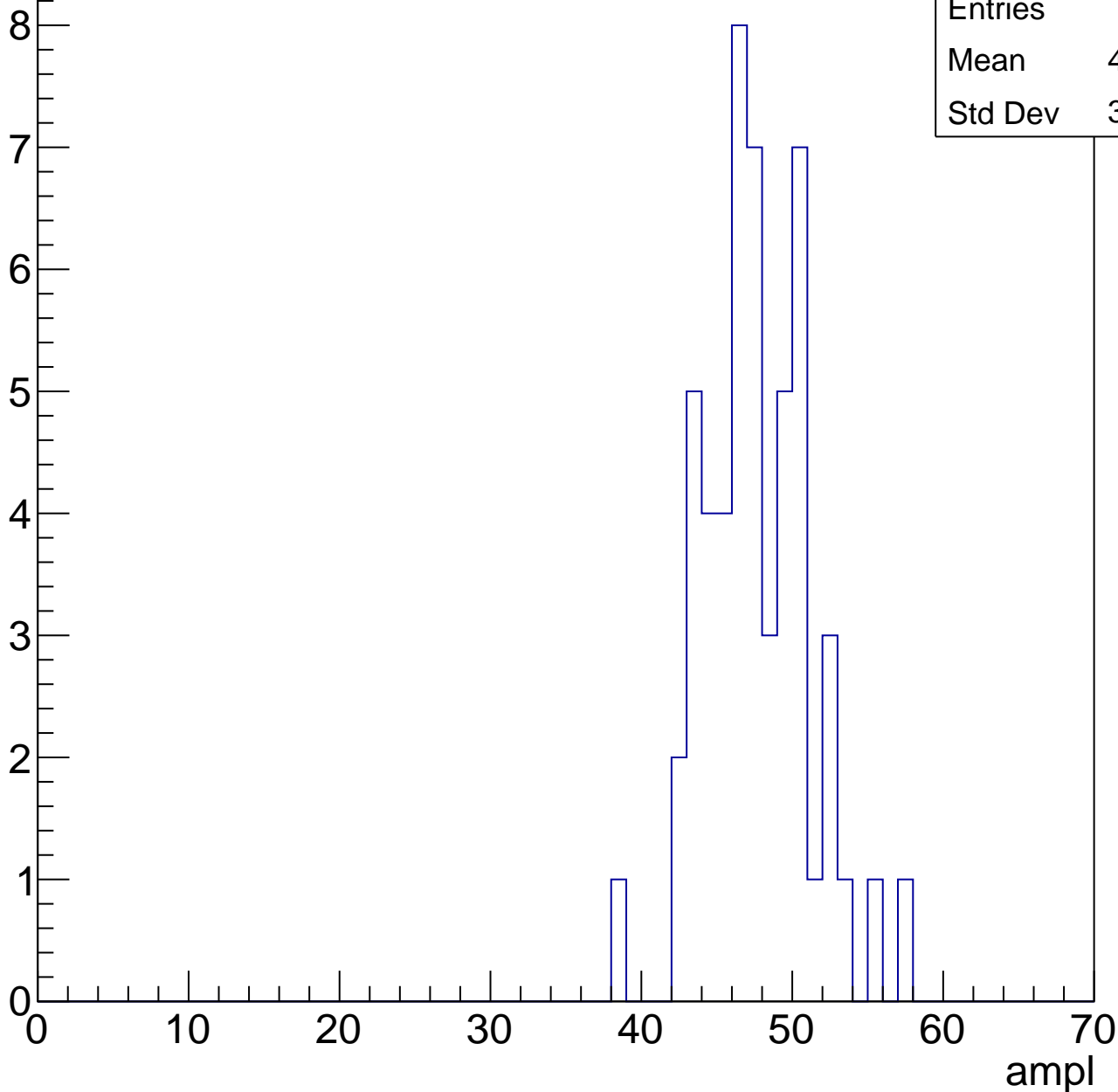


# B1L103S, U26-ch58, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	53
Mean	47.19
Std Dev	3.492

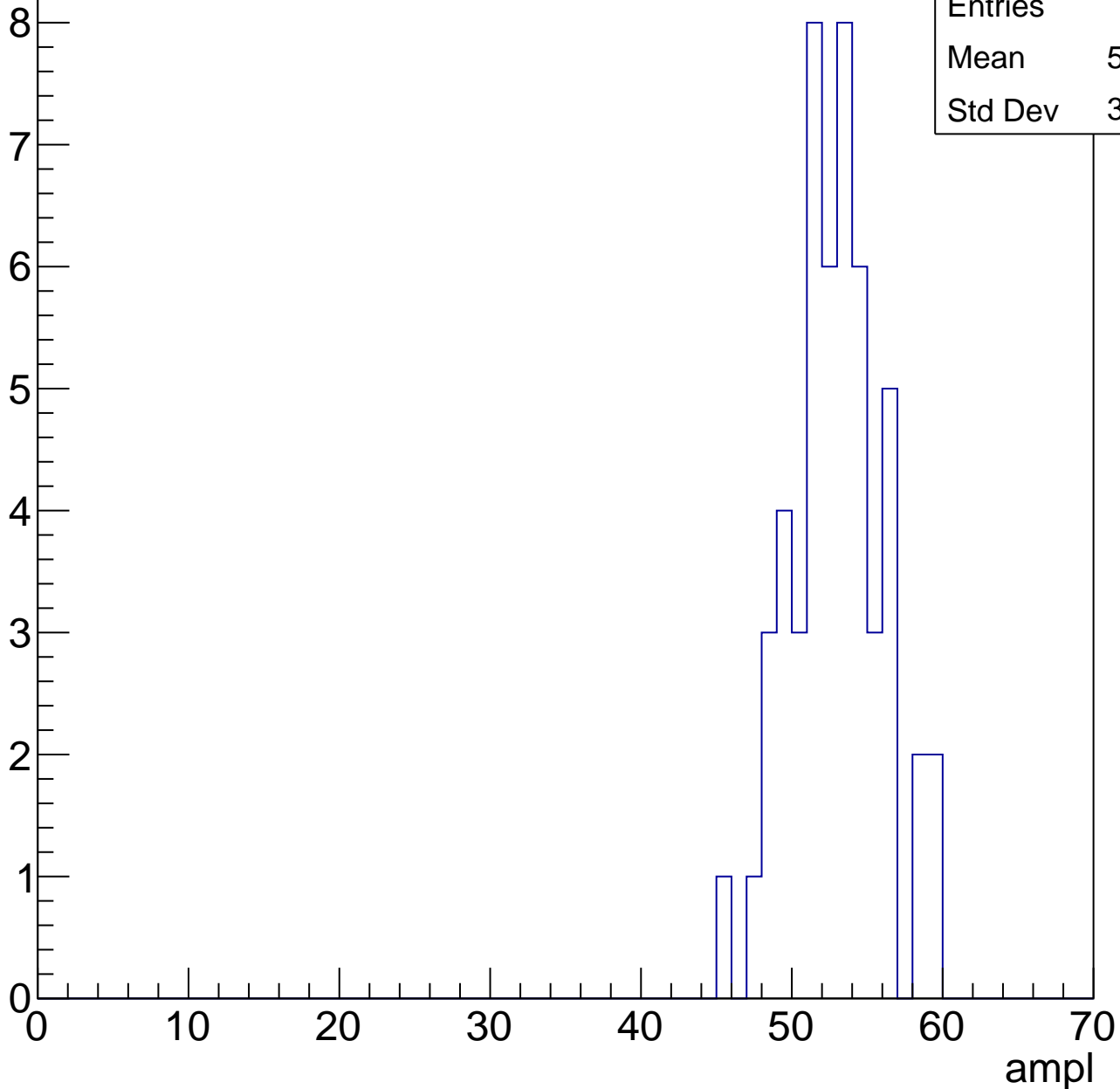


# B1L103S, U26-ch58, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

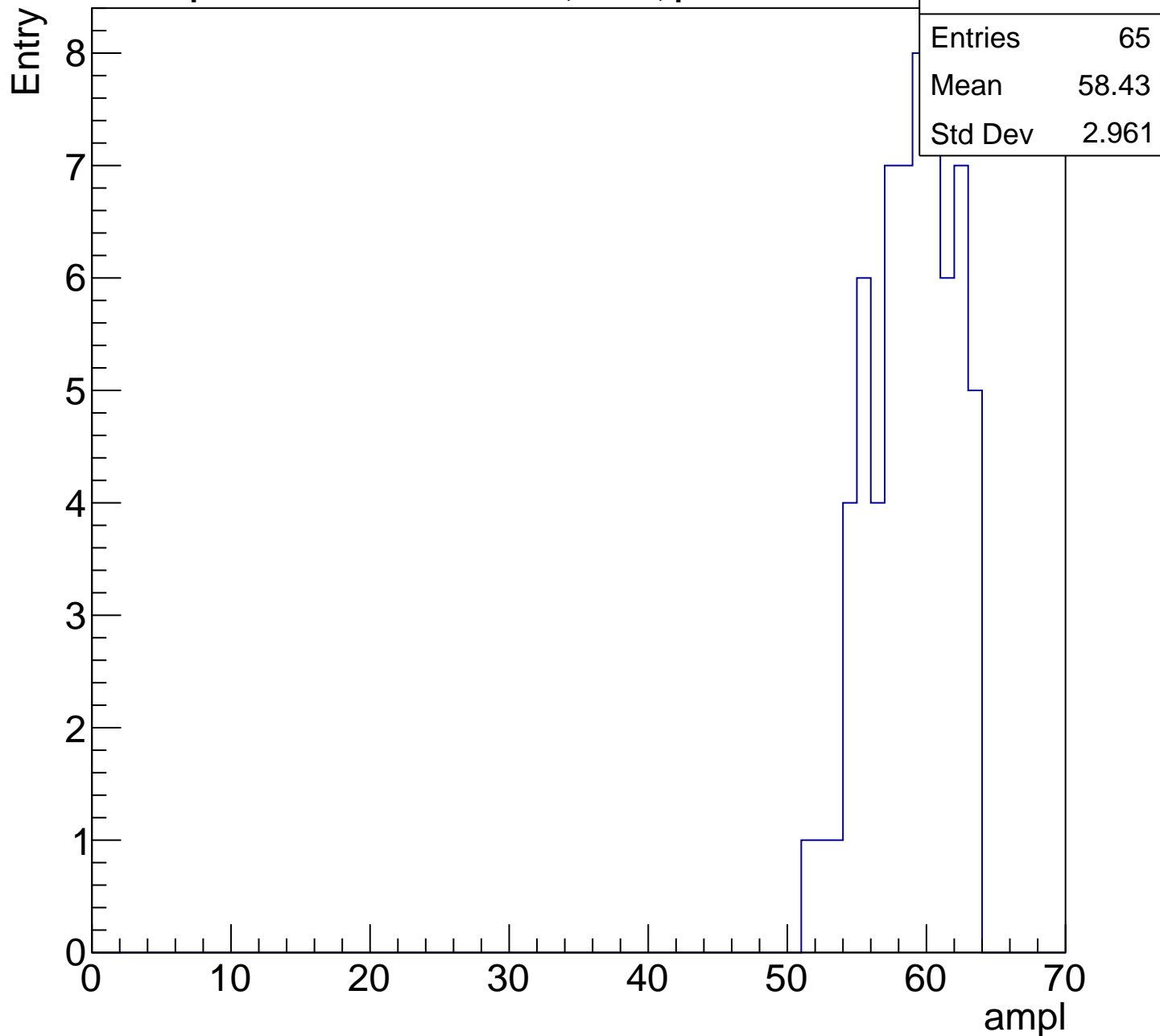
Entry

Entries	52
Mean	52.48
Std Dev	3.022



# B1L103S, U26-ch58, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

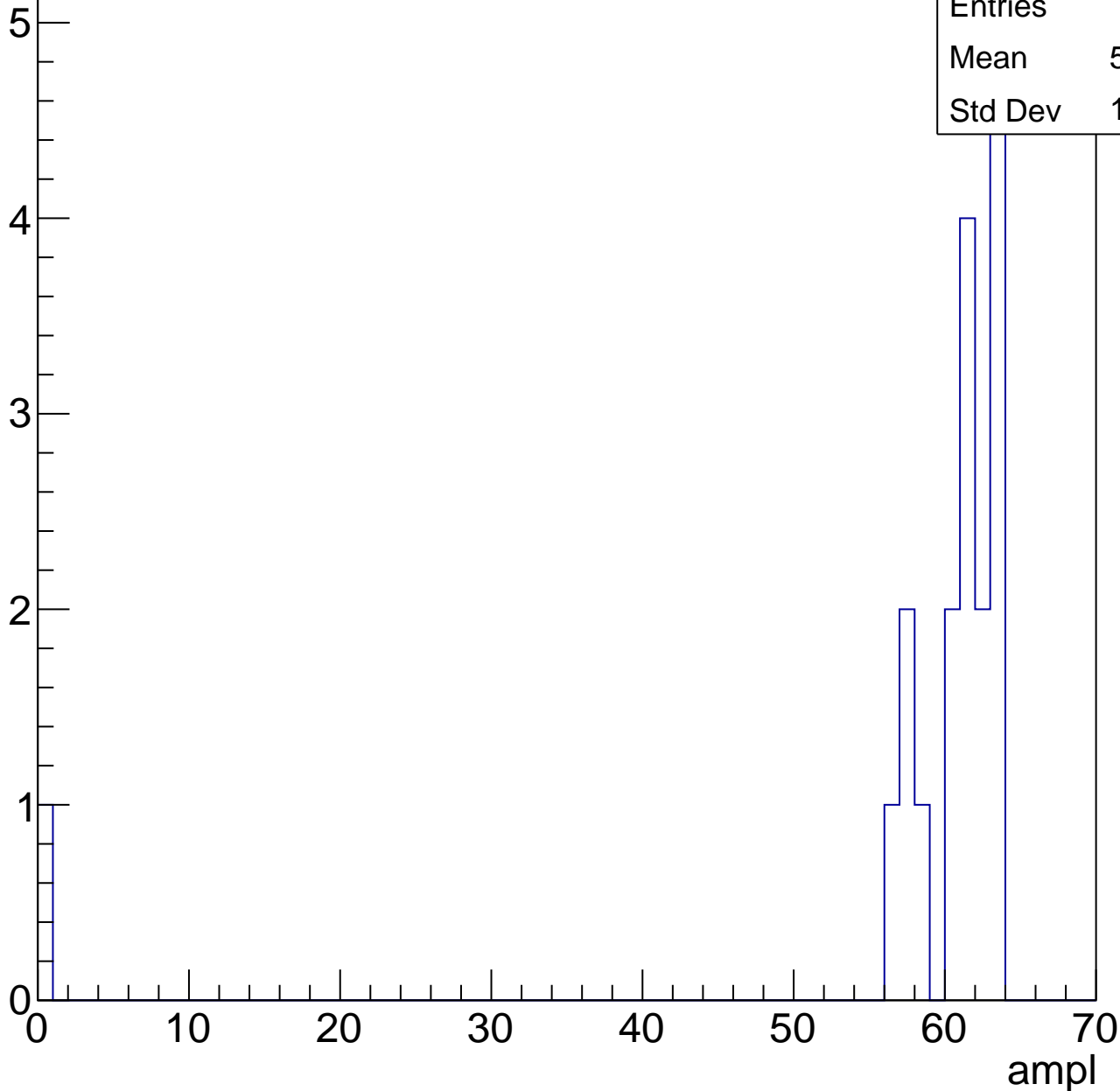


# B1L103S, U26-ch58, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	18
Mean	57.28
Std Dev	14.07





# B1L103S, U26-ch58, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	20
Mean	3.1
Std Dev	13.51

Entry



# B1L103S, U26-ch59, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	83
Mean	25.53
Std Dev	11.41

**Gaus mean : 31.2831**

**Gaus Width: 4.1802**

Entry

12

10

8

6

4

2

0

0

10

20

30

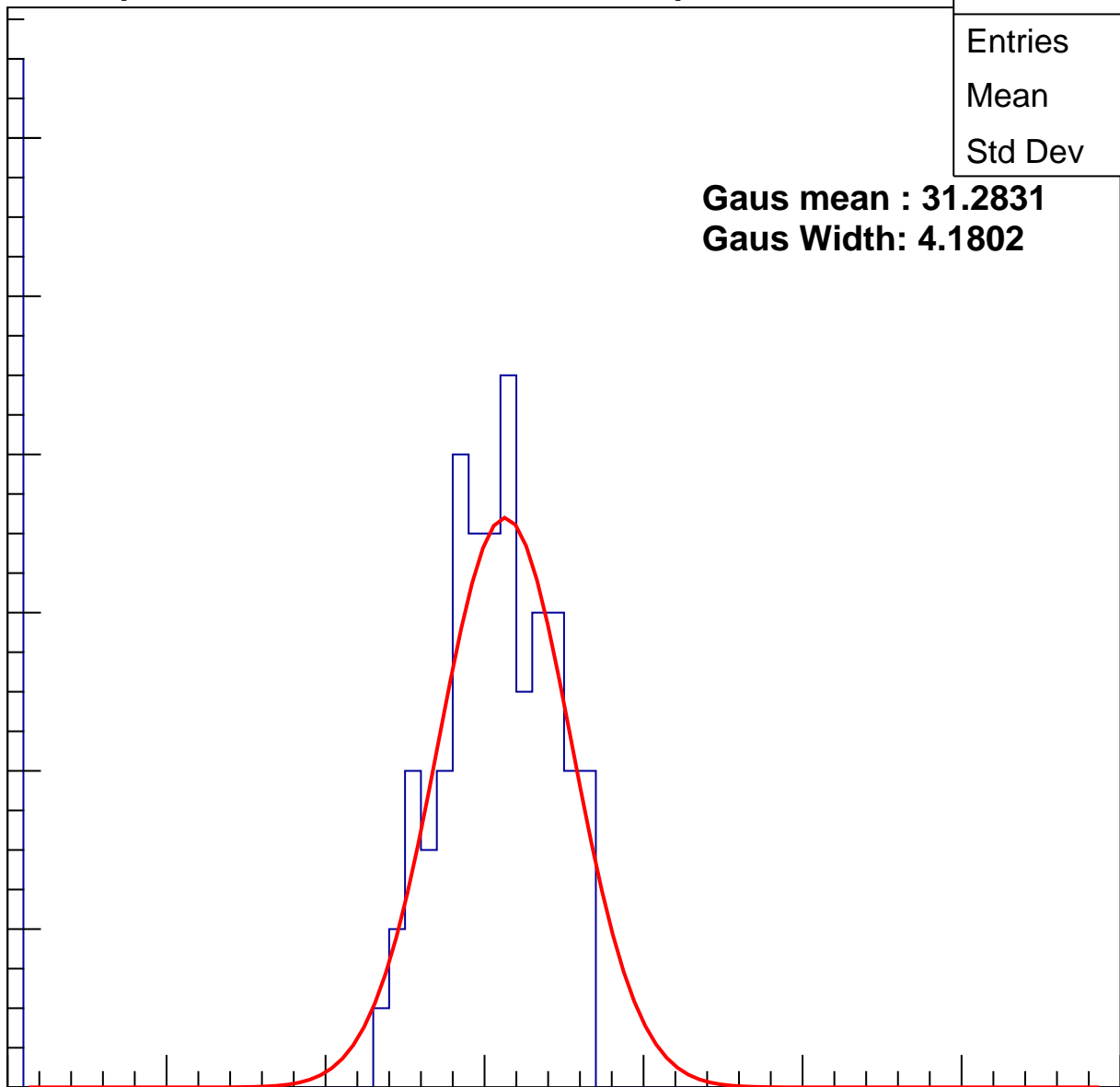
40

50

60

70

ampl



# B1L103S, U26-ch59, adc1

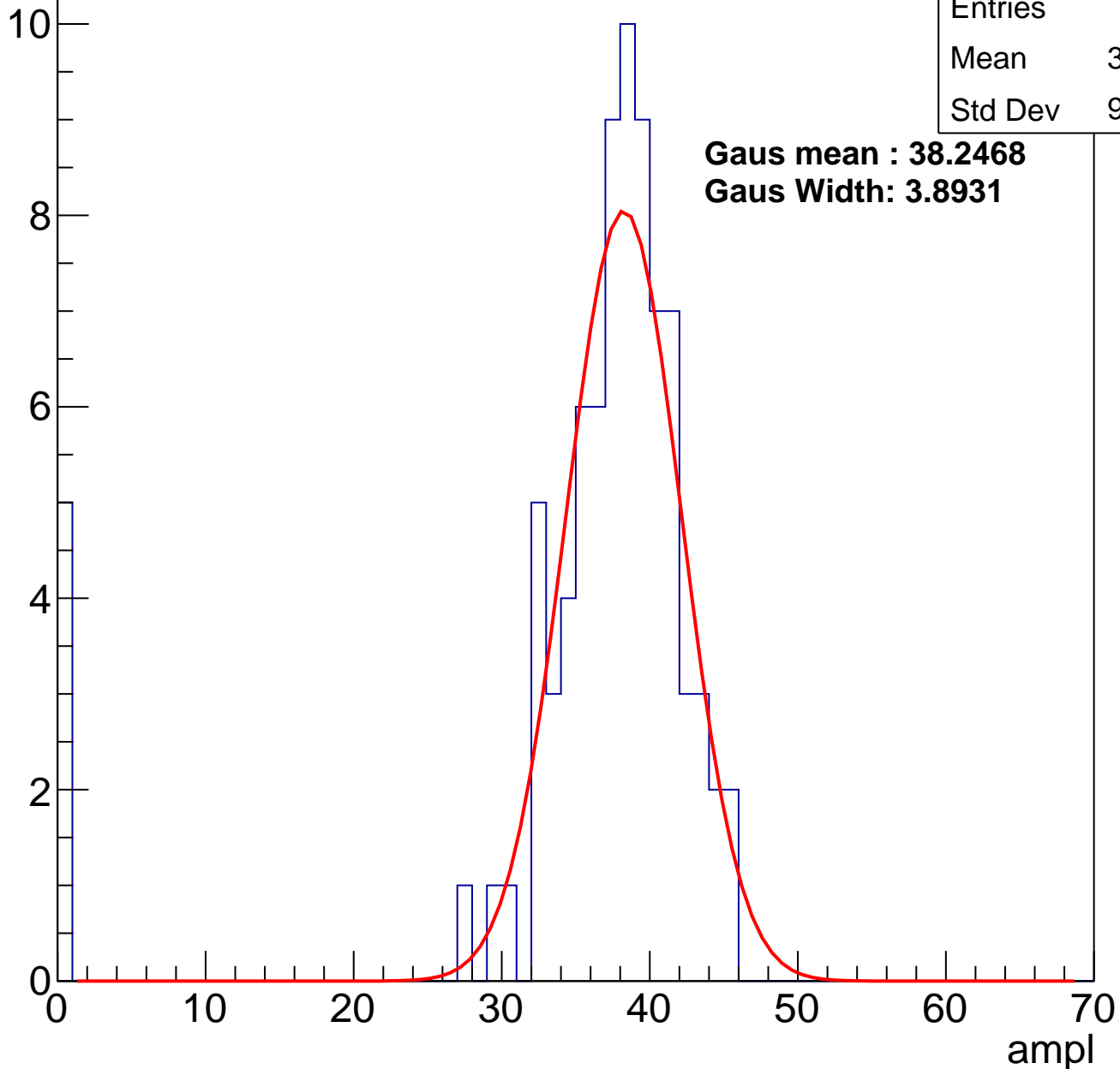
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	84
Mean	35.37
Std Dev	9.576

**Gaus mean : 38.2468**

**Gaus Width: 3.8931**

Entry



# B1L103S, U26-ch59, adc2

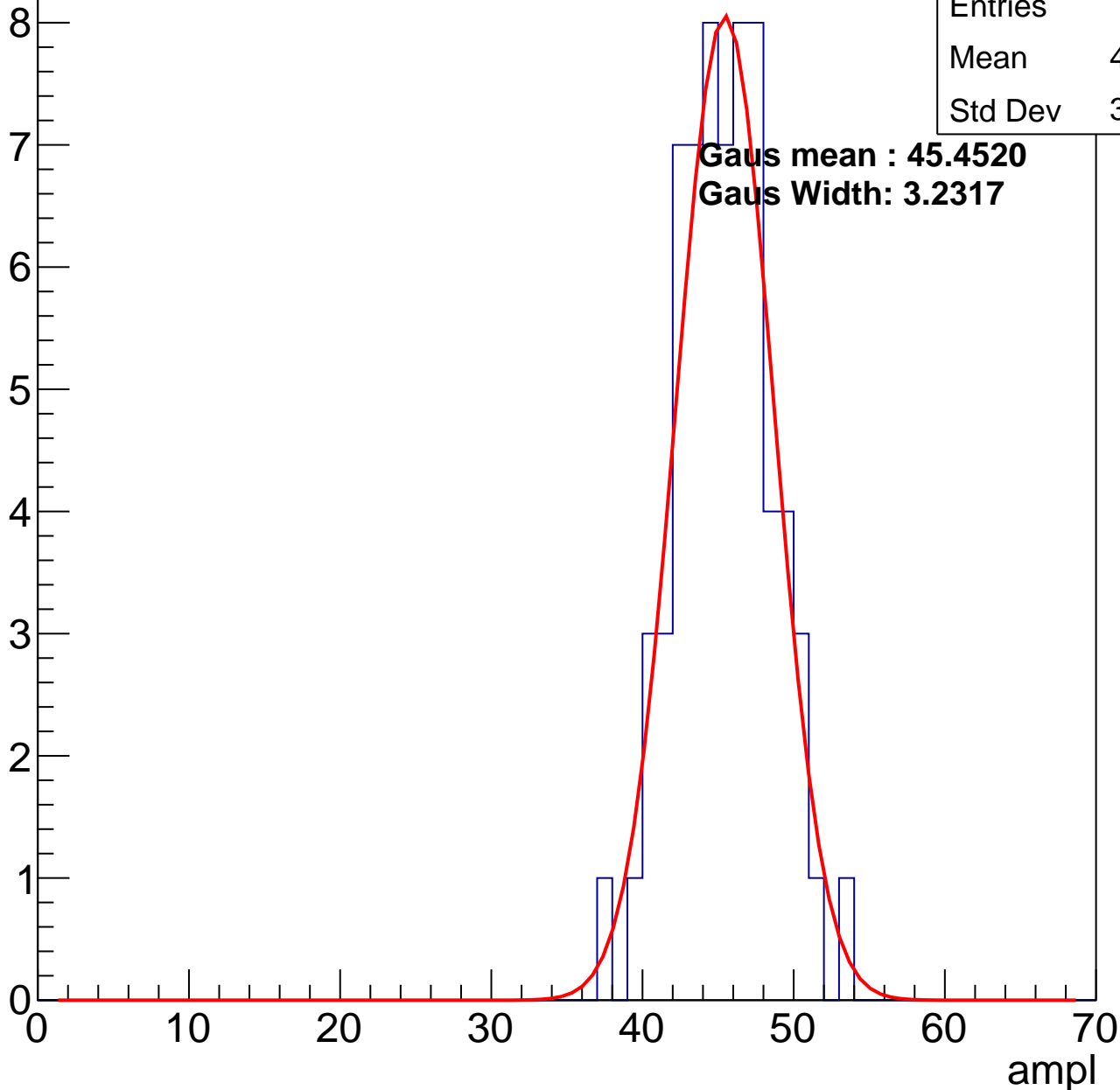
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	66
Mean	44.95
Std Dev	3.106

**Gaus mean : 45.4520**

**Gaus Width: 3.2317**

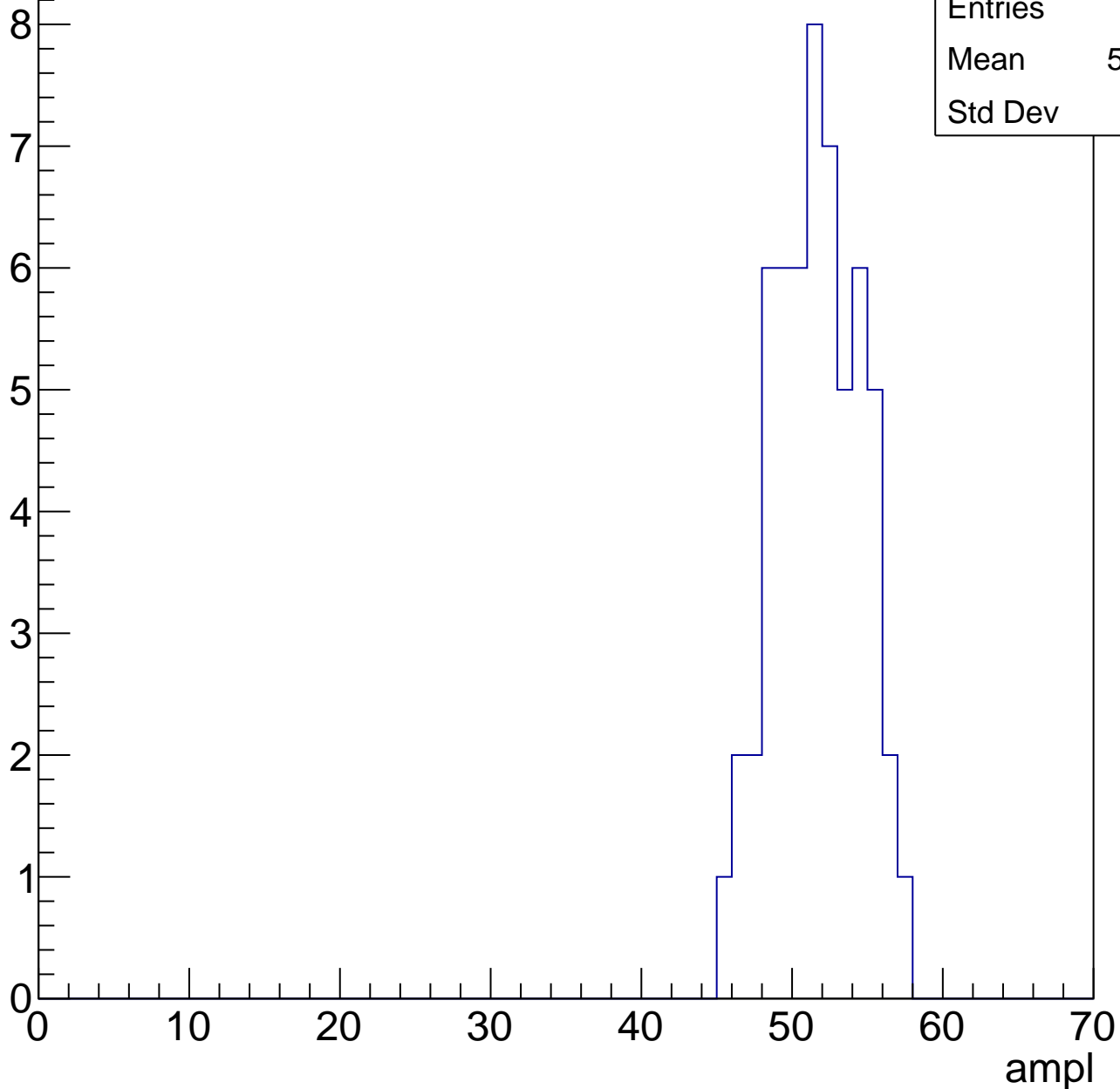


# B1L103S, U26-ch59, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	57
Mean	51.19
Std Dev	2.8



# B1L103S, U26-ch59, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	55
Mean	55.38
Std Dev	7.983

Entry

10

8

6

4

2

0

0

10

20

30

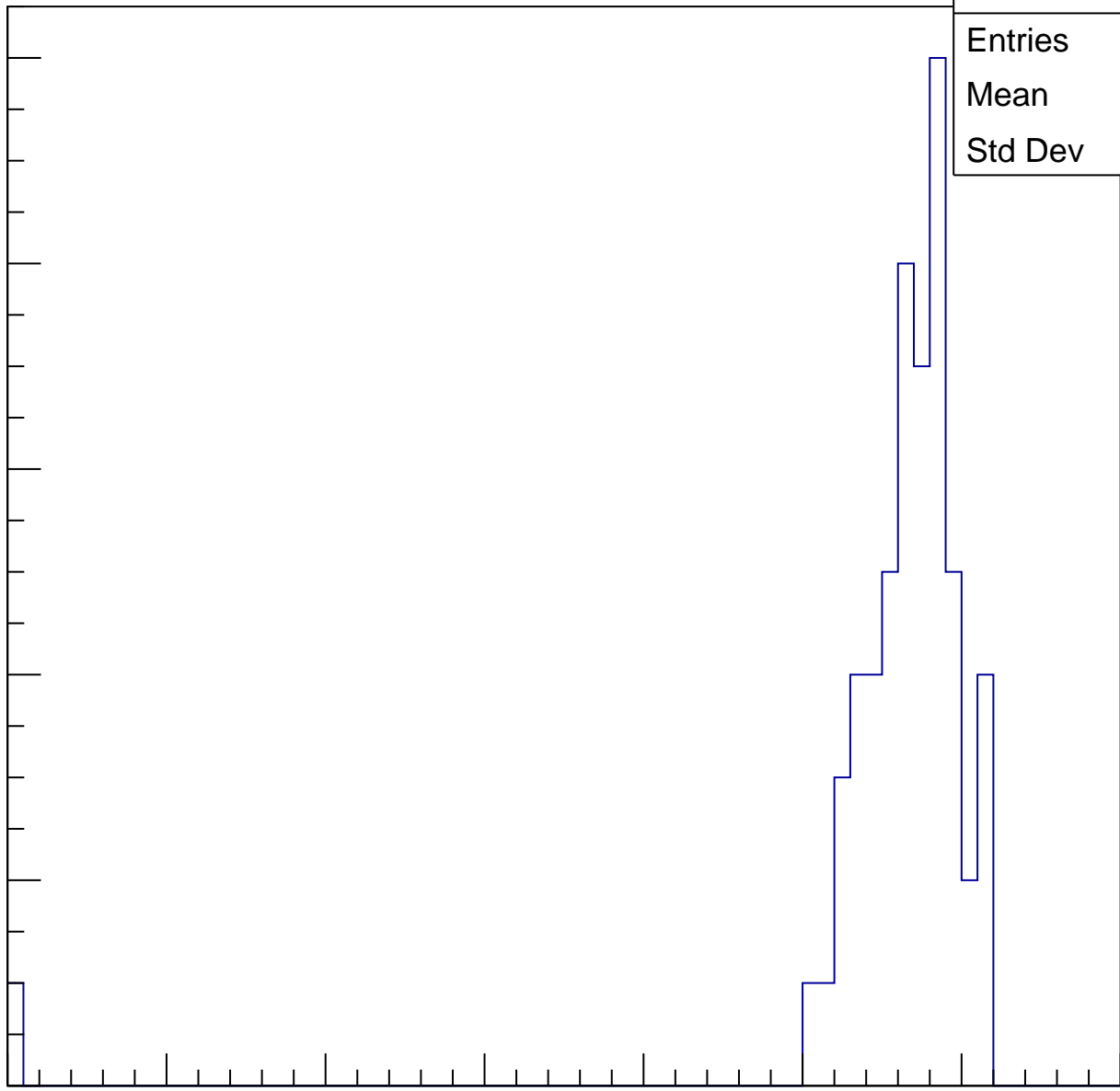
40

50

60

70

ampl



# B1L103S, U26-ch59, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	34
Mean	60.91
Std Dev	1.634

ampl

0 10 20 30 40 50 60 70

0

1

2

3

4

5

6

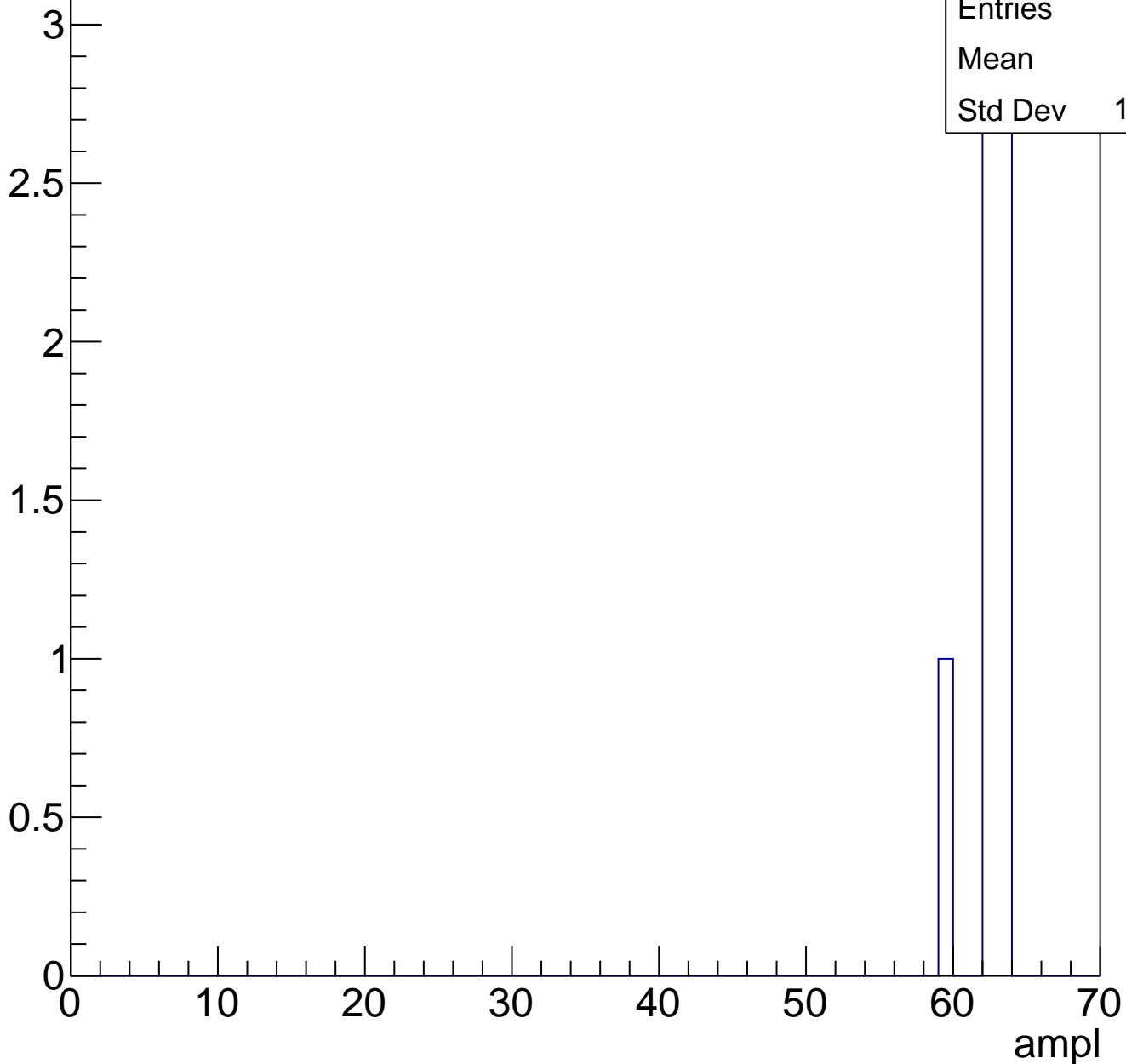
7

8

# B1L103S, U26-ch59, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry





# B1L103S, U26-ch59, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



# B1L103S, U26-ch60, adc0

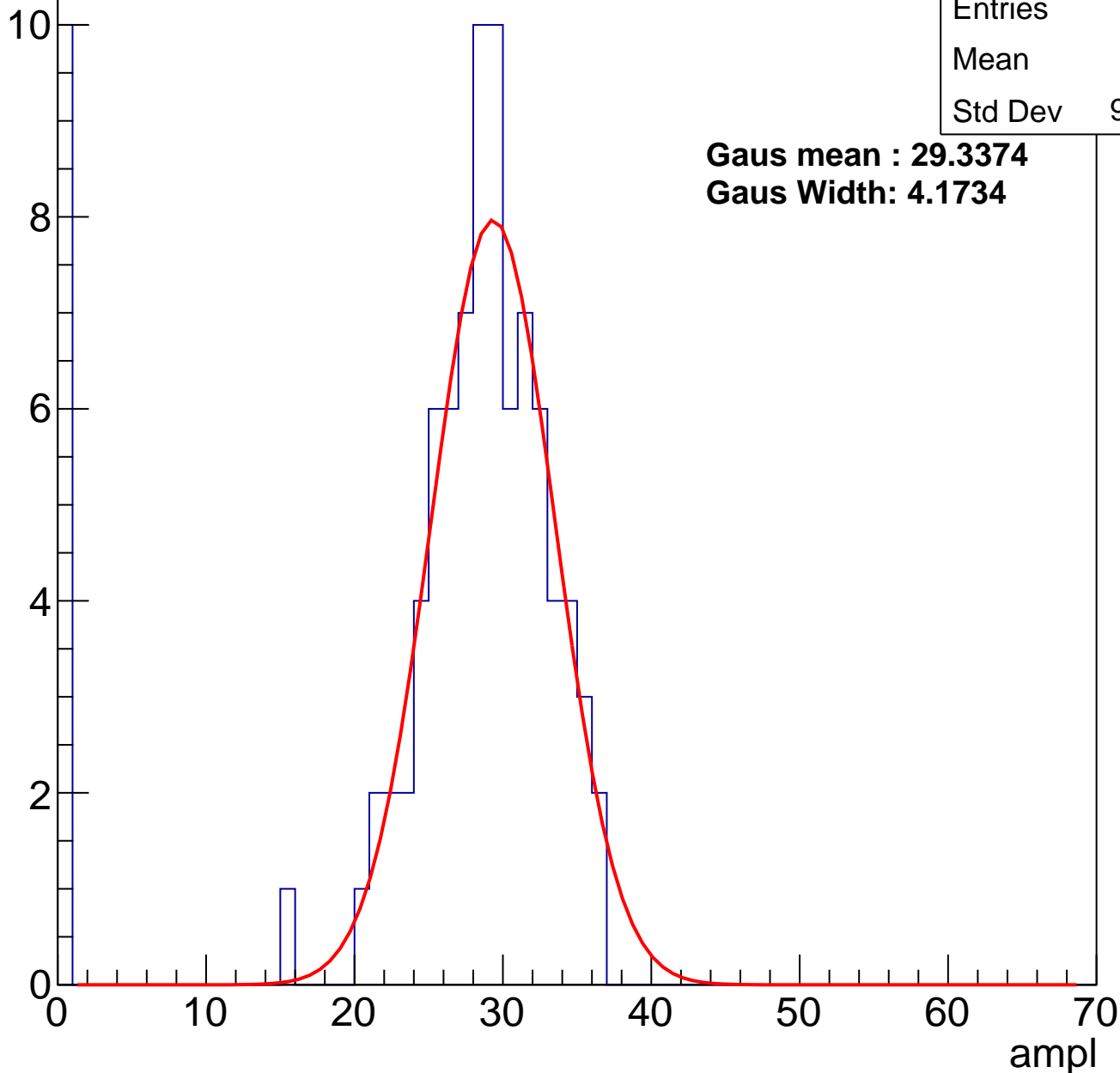
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	93
Mean	25.4
Std Dev	9.574

**Gaus mean : 29.3374**

**Gaus Width: 4.1734**

Entry



# B1L103S, U26-ch60, adc1

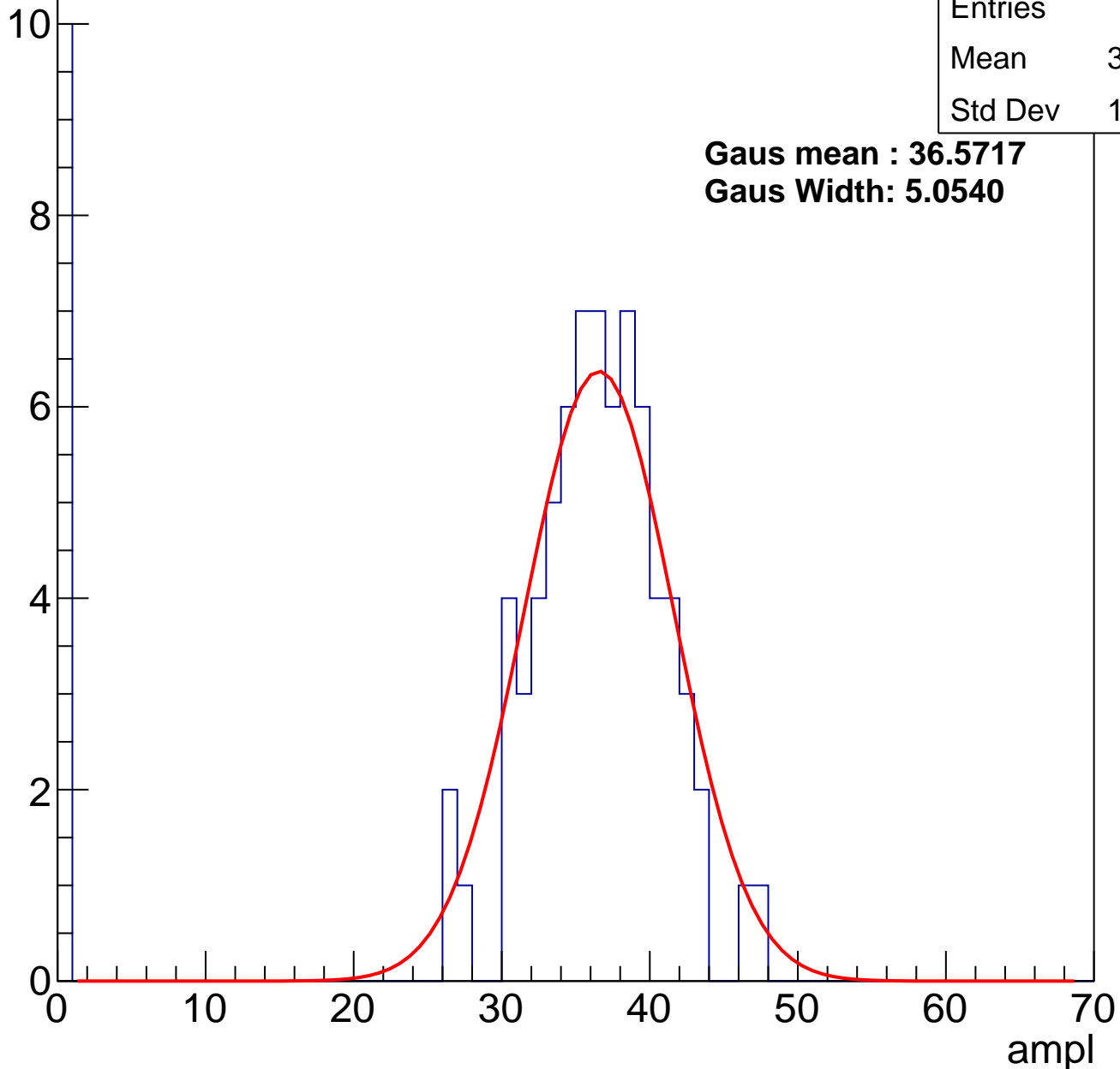
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	83
Mean	31.77
Std Dev	12.42

**Gaus mean : 36.5717**

**Gaus Width: 5.0540**

Entry



# B1L103S, U26-ch60, adc2

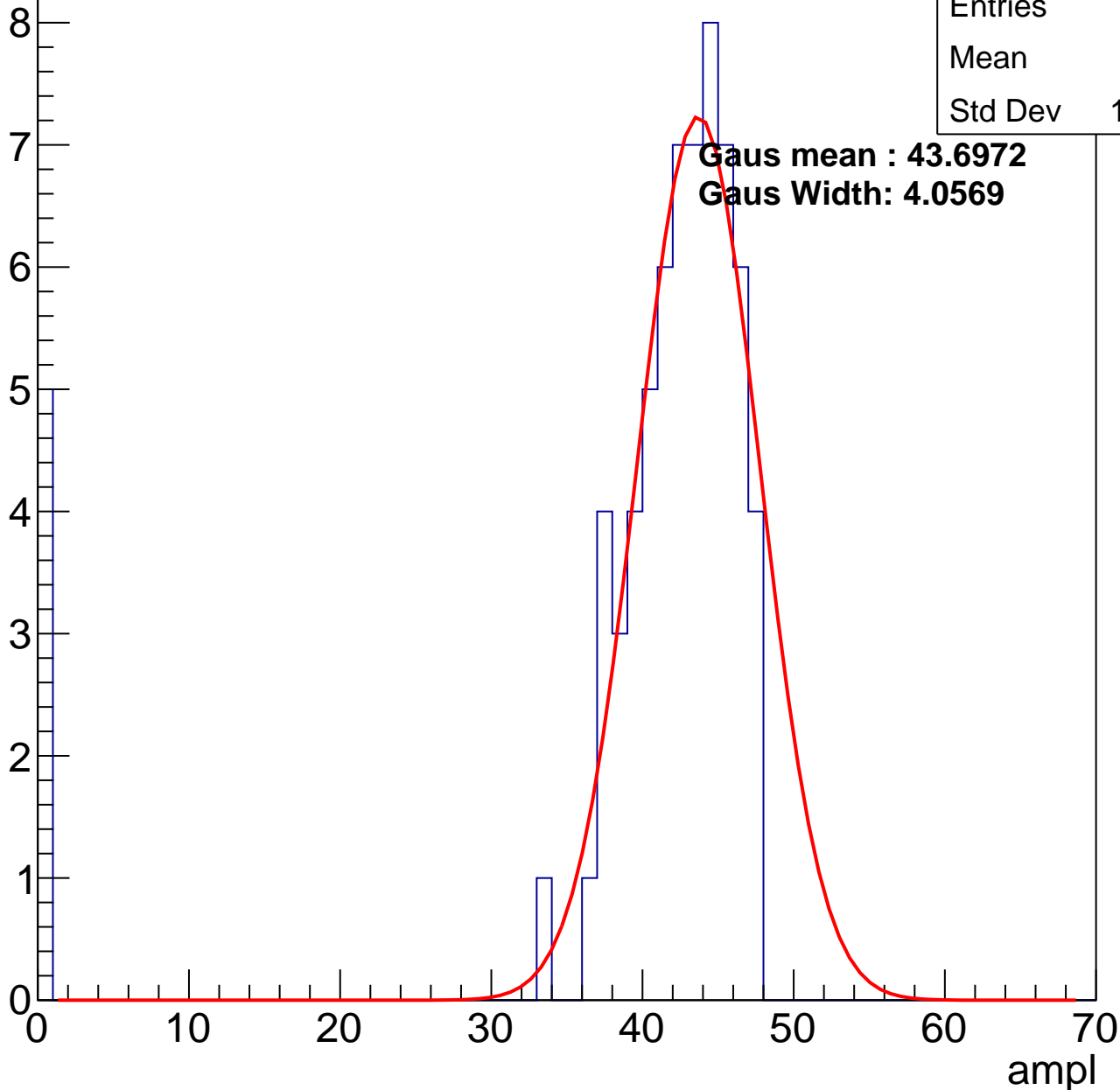
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	68
Mean	39.1
Std Dev	11.42

**Gaus mean : 43.6972**

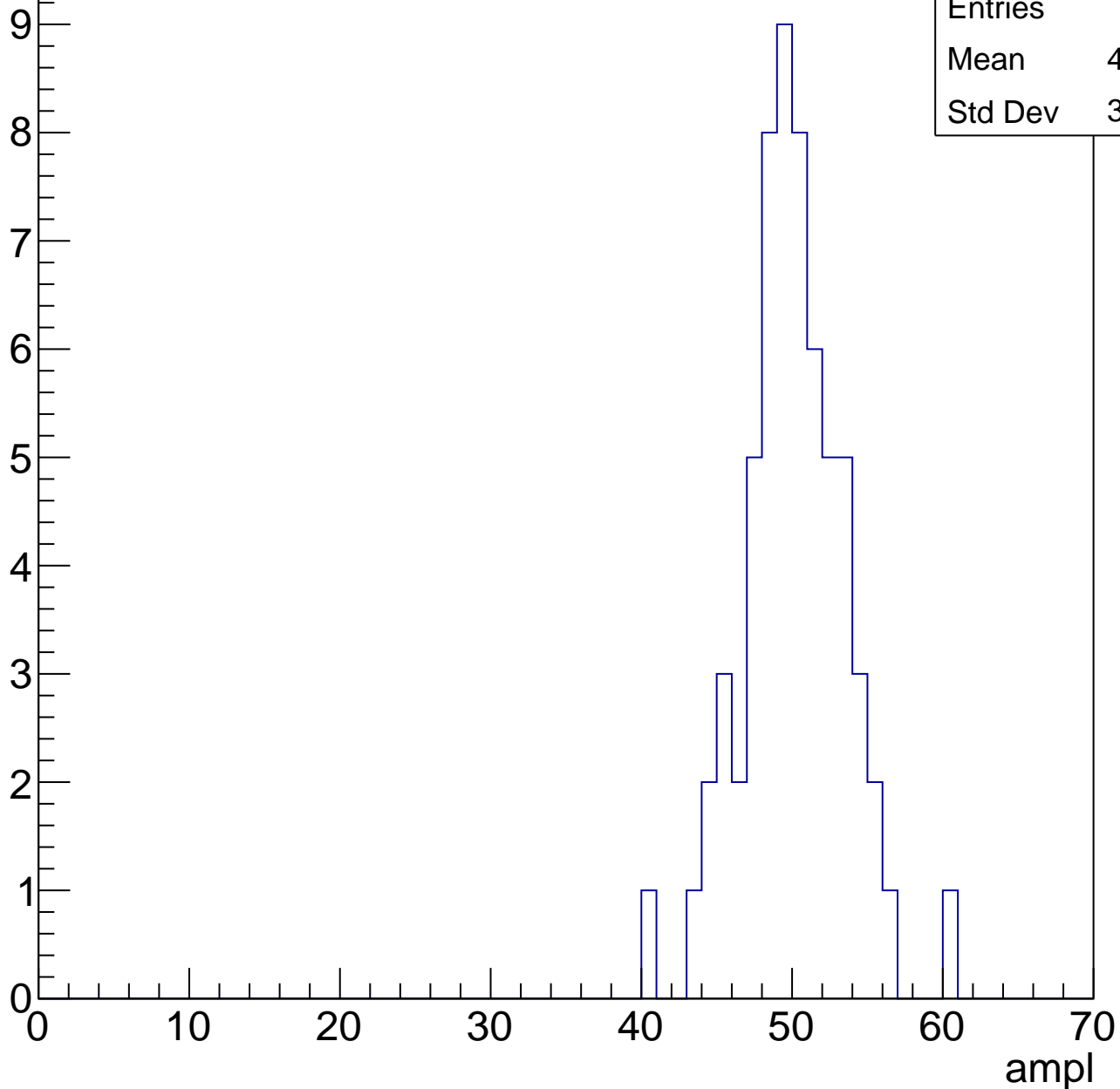
**Gaus Width: 4.0569**



# B1L103S, U26-ch60, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

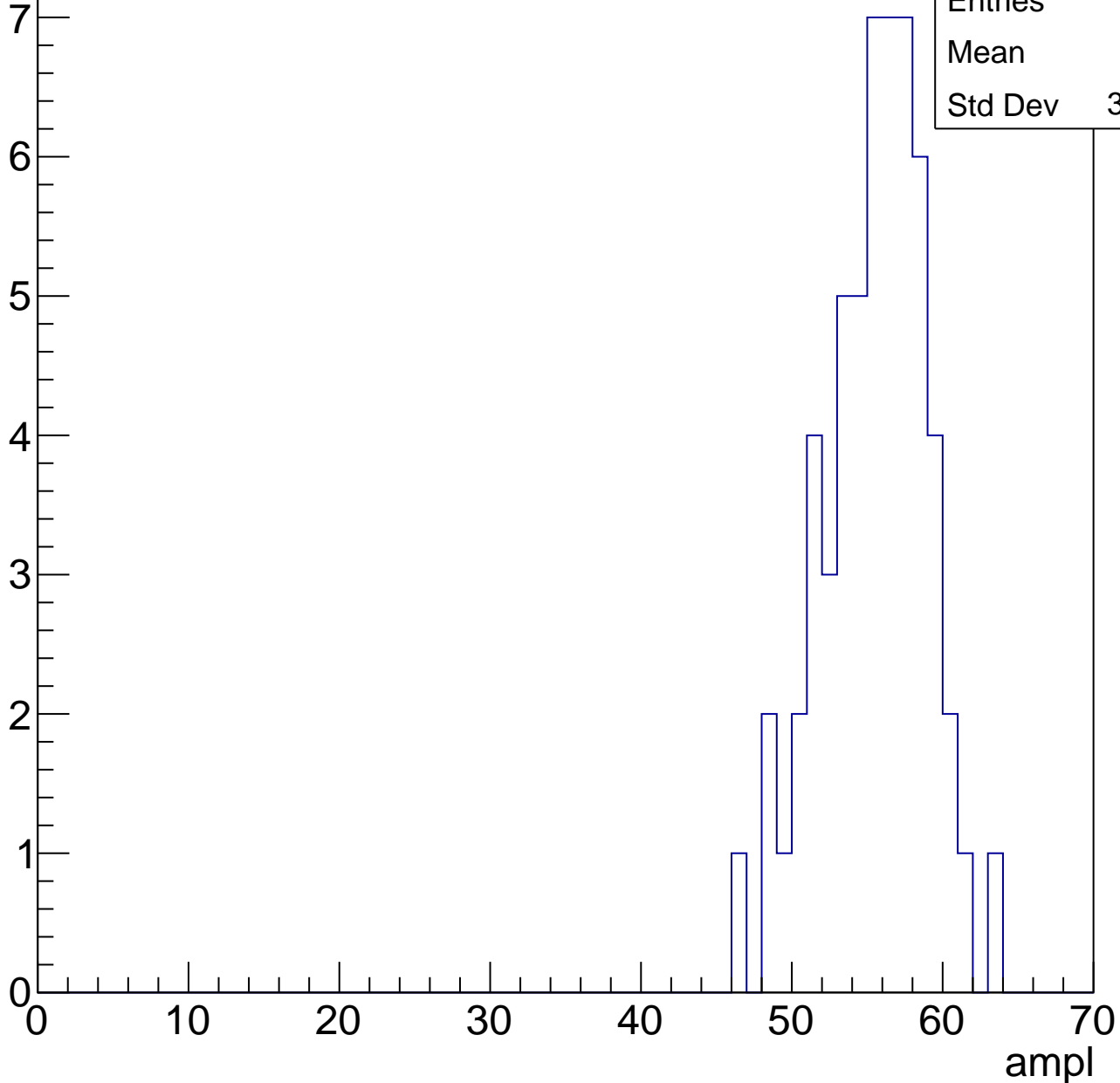


# B1L103S, U26-ch60, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	58
Mean	55
Std Dev	3.434

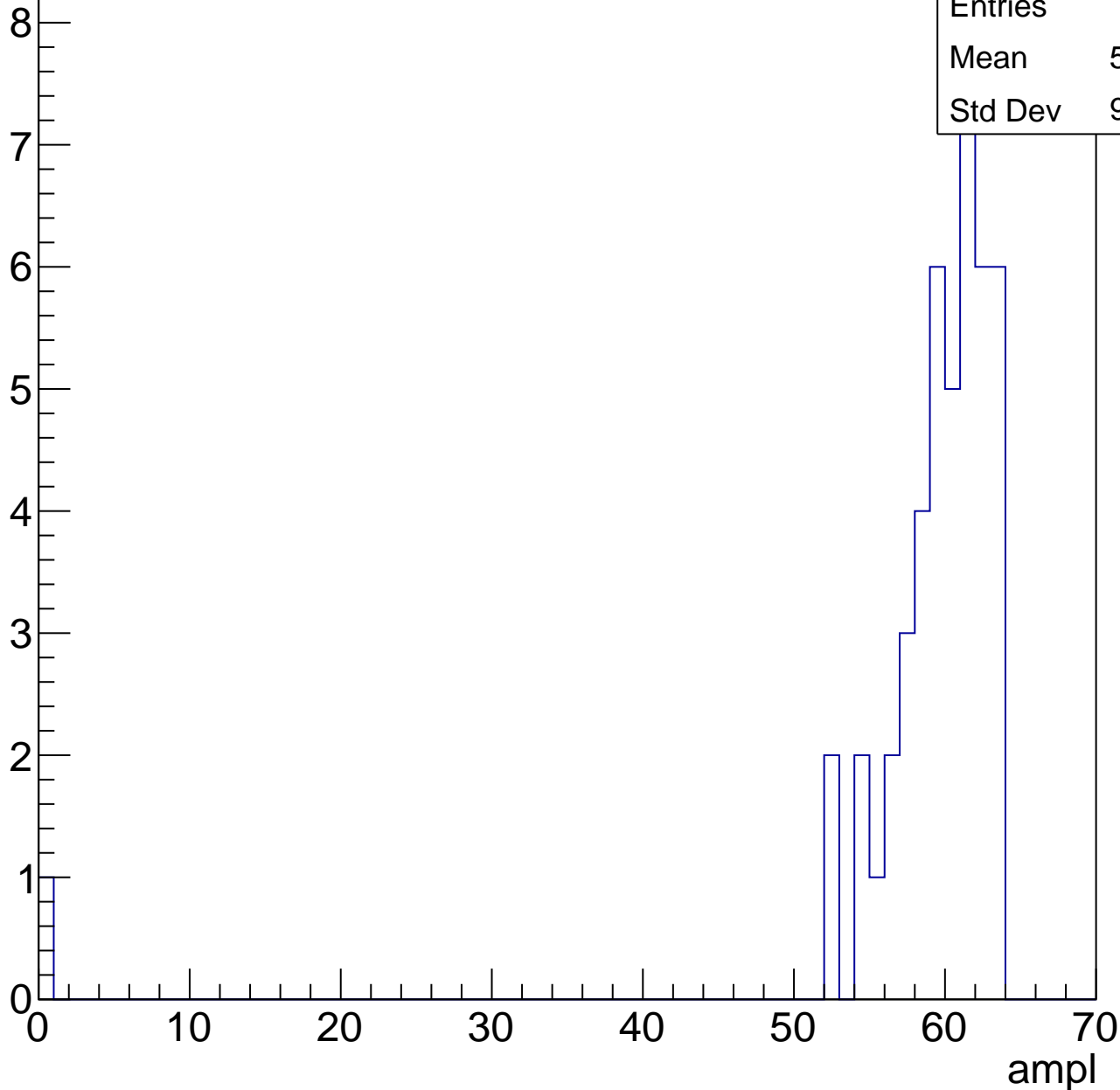


# B1L103S, U26-ch60, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

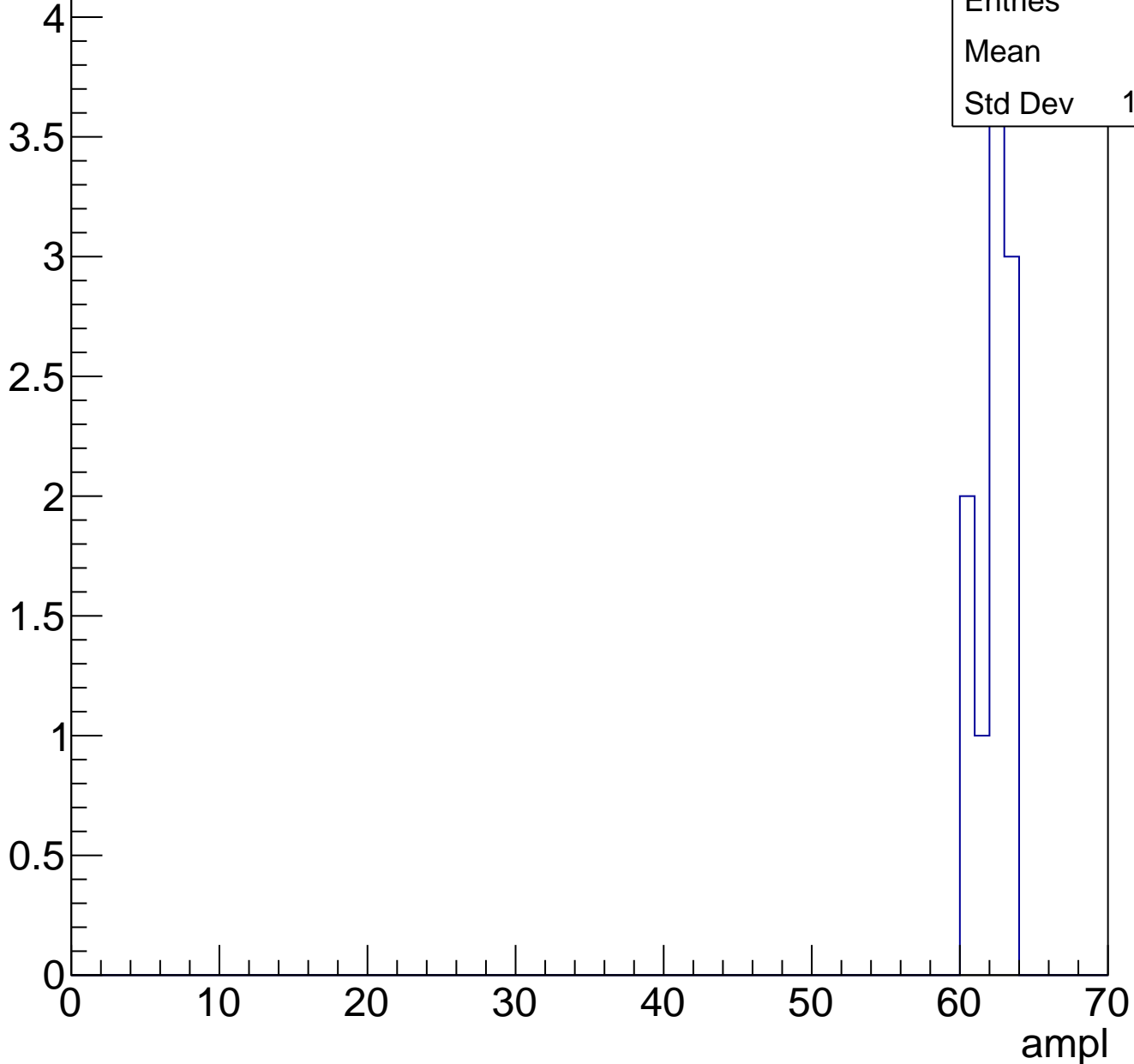
Entries	46
Mean	58.13
Std Dev	9.126



# B1L103S, U26-ch60, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry





# B1L103S, U26-ch60, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

18  
16  
14  
12  
10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

Entries	19
Mean	0
Std Dev	0

# B1L103S, U26-ch61, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	76
Mean	28.28
Std Dev	7.5

**Gaus mean : 30.7647**

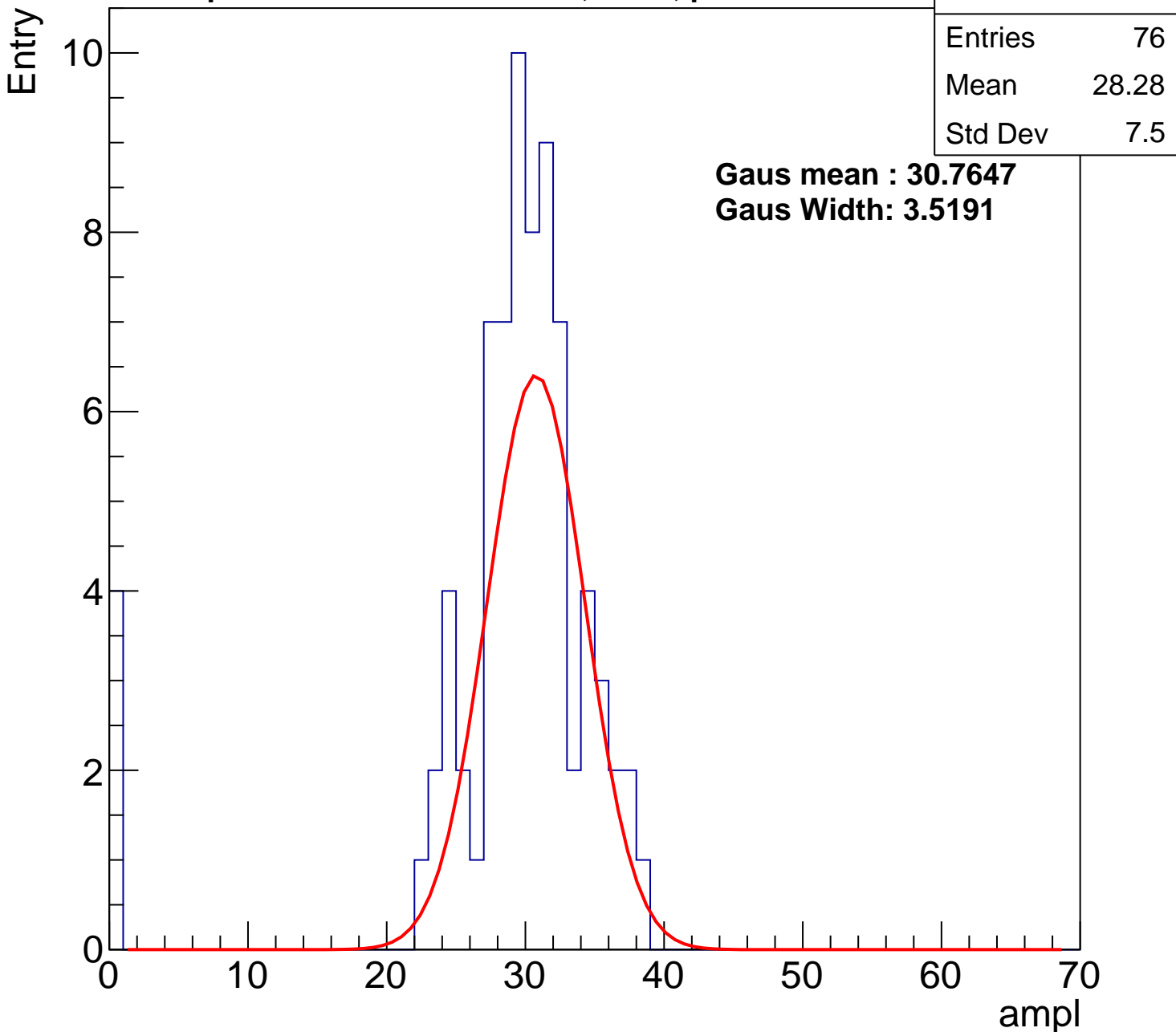
**Gaus Width: 3.5191**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



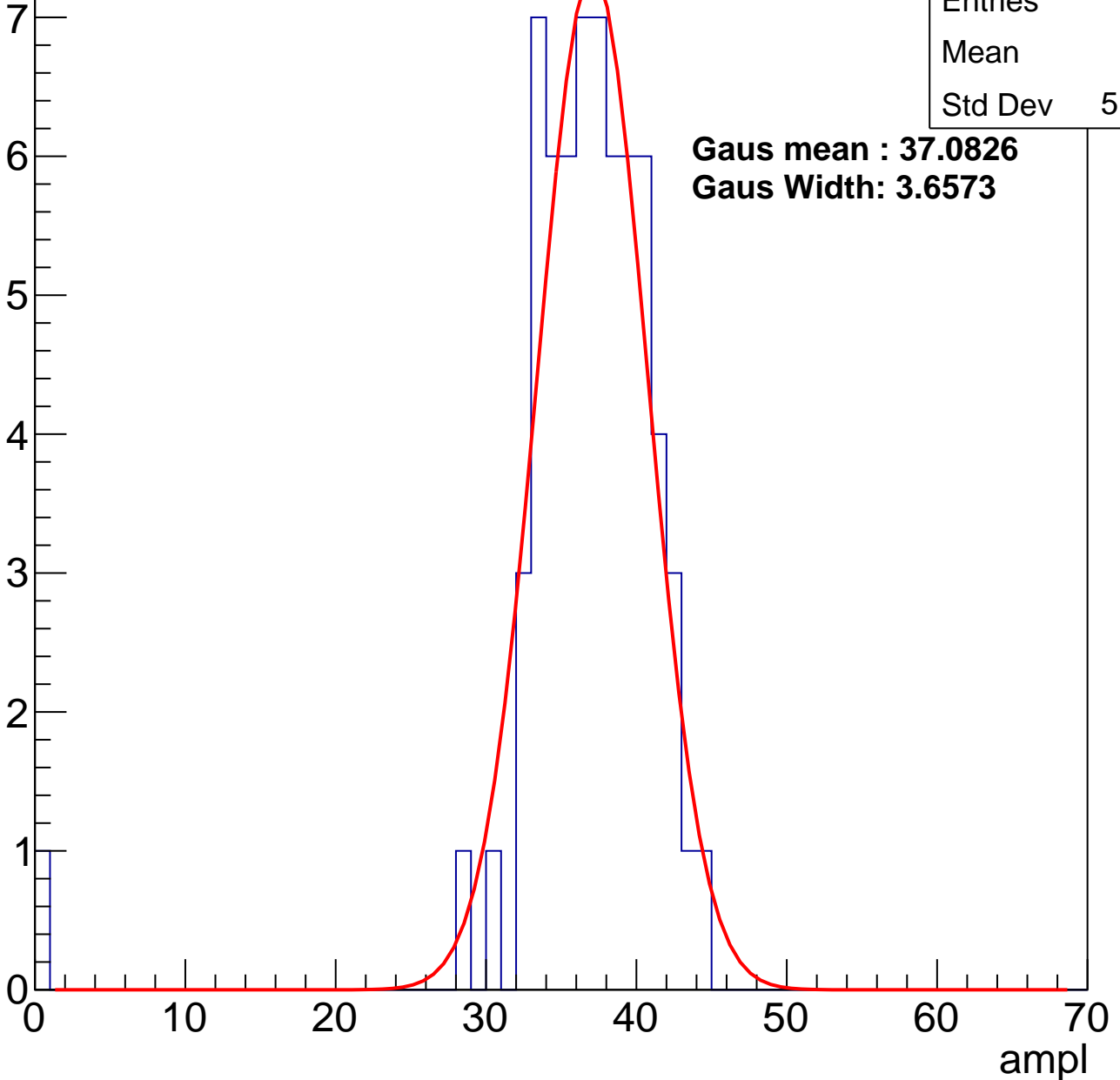
# B1L103S, U26-ch61, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	66
Mean	36.2
Std Dev	5.555

**Gaus mean : 37.0826**  
**Gaus Width: 3.6573**



# B1L103S, U26-ch61, adc2

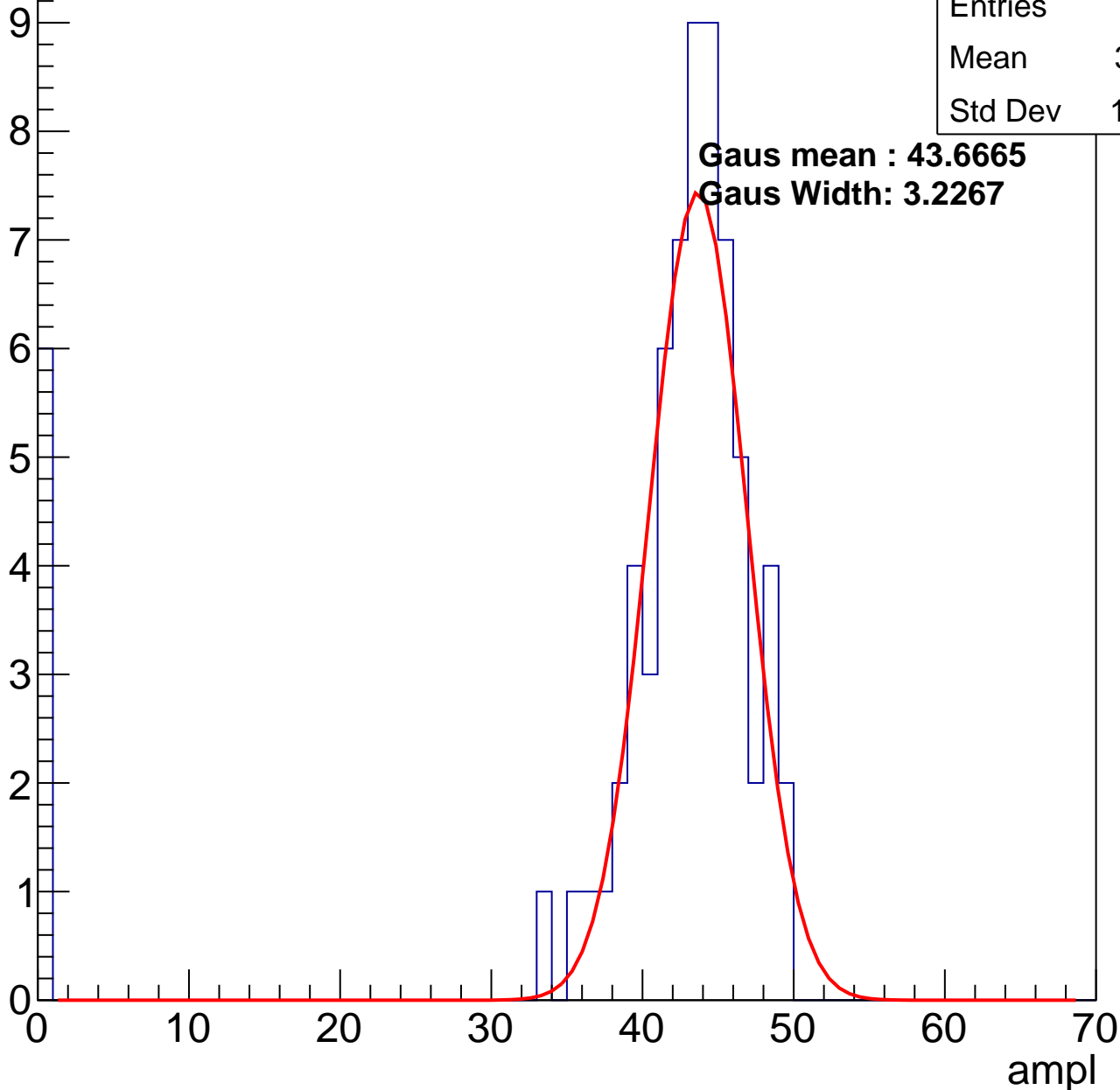
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	70
Mean	39.21
Std Dev	12.42

**Gaus mean : 43.6665**

**Gaus Width: 3.2267**

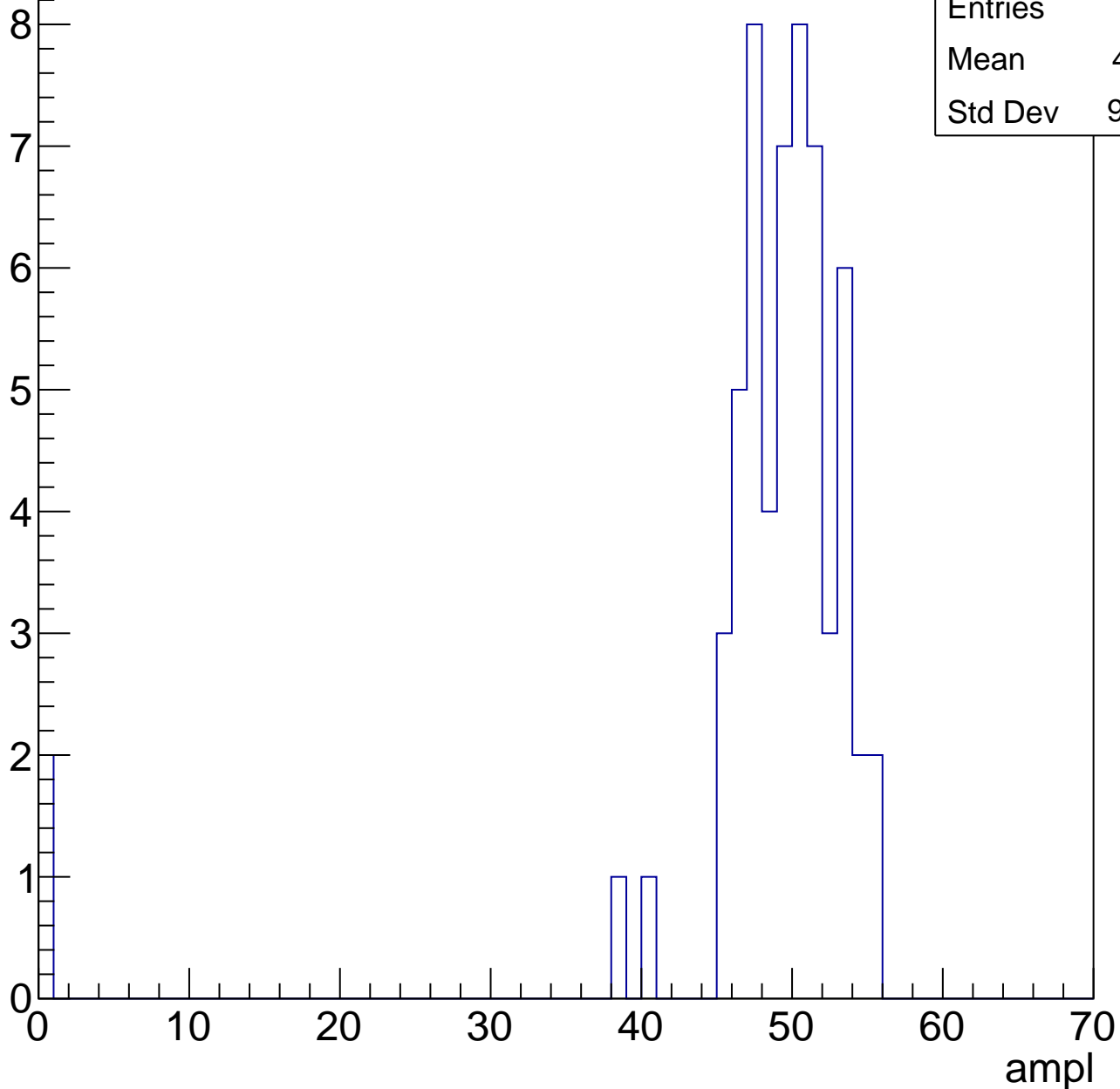


# B1L103S, U26-ch61, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	59
Mean	47.51
Std Dev	9.462

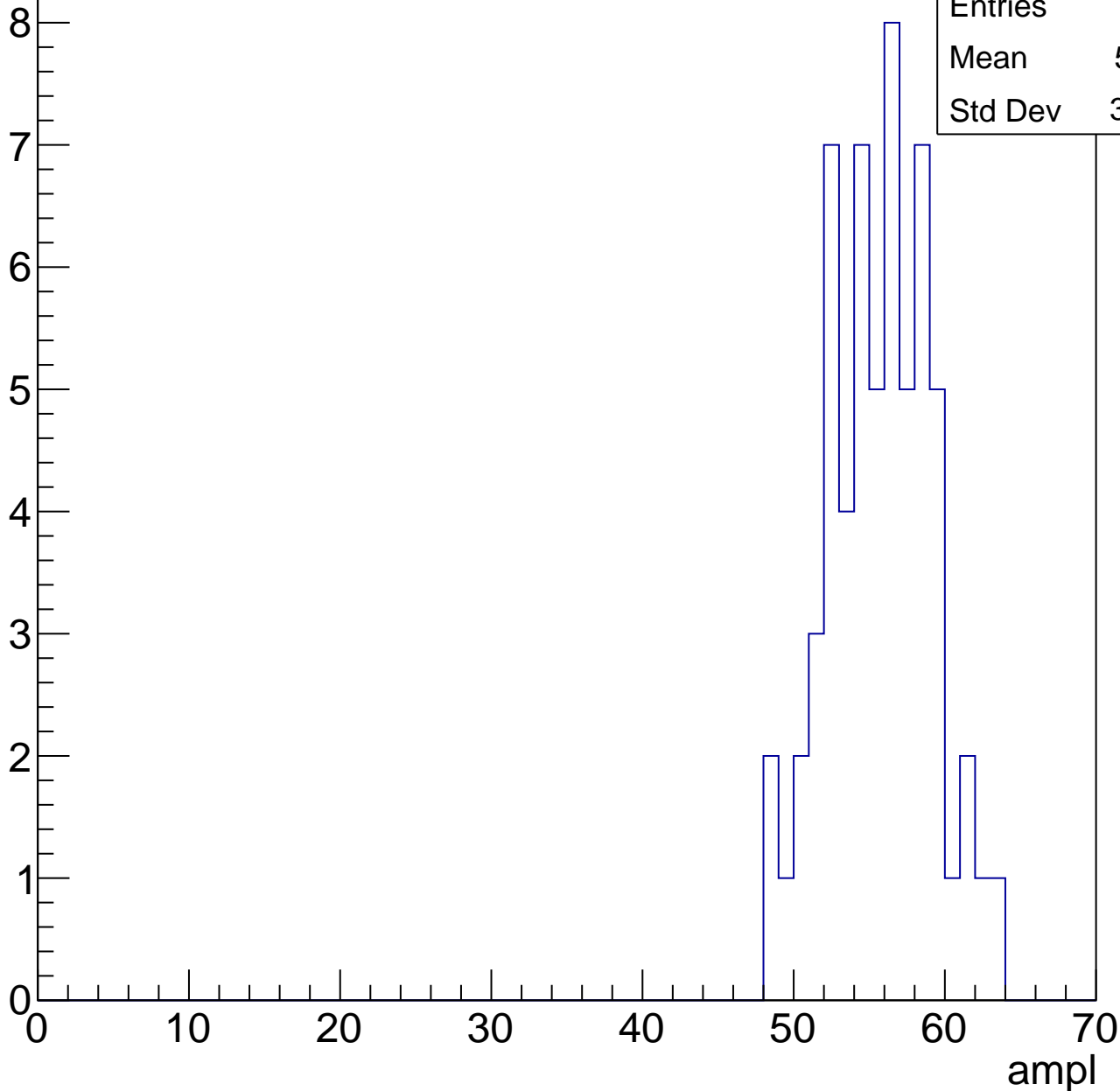


# B1L103S, U26-ch61, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

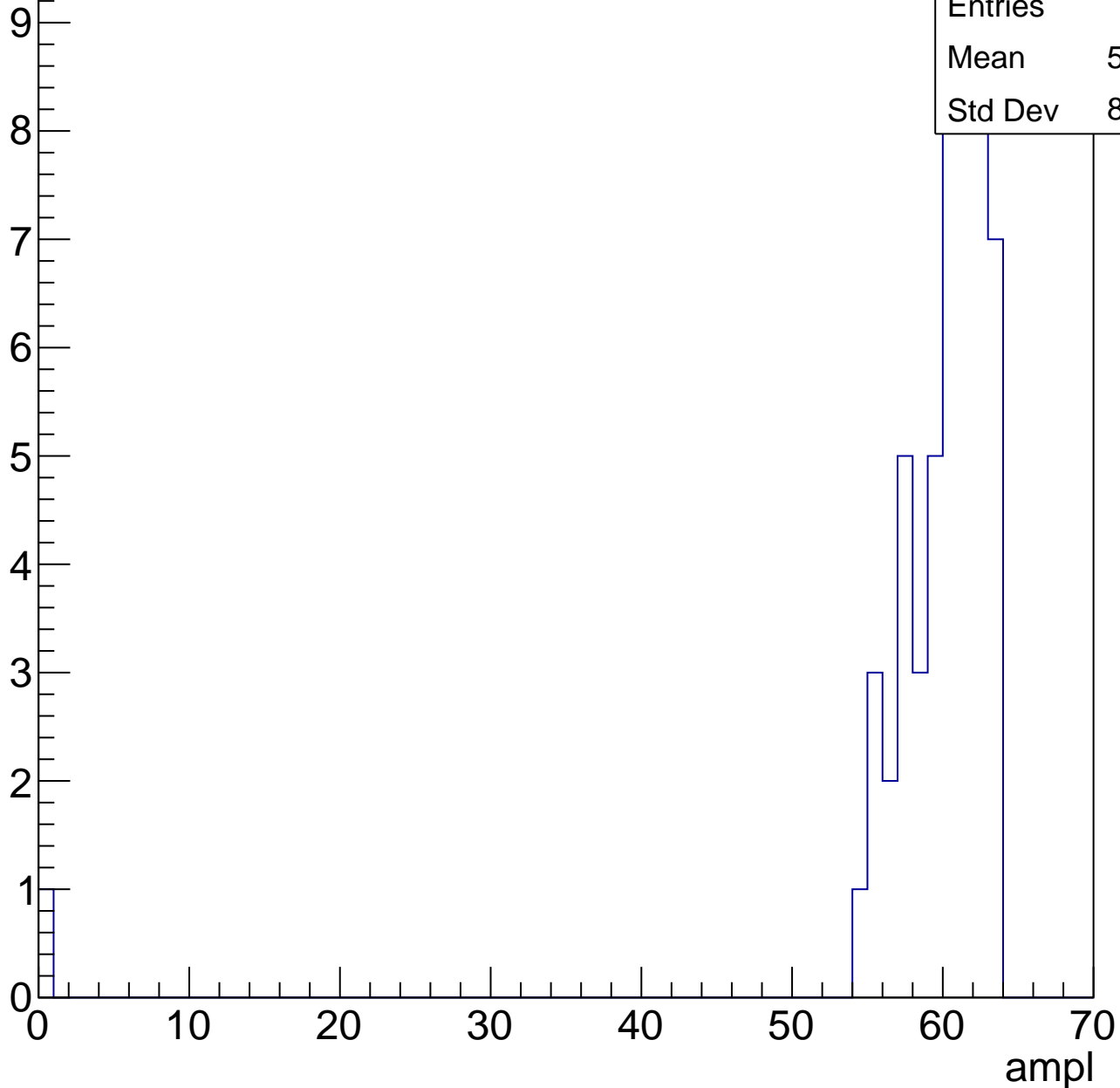
Entries	61
Mean	55.21
Std Dev	3.378



# B1L103S, U26-ch61, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



# B1L103S, U26-ch61, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	2
Mean	63
Std Dev	0

ampl



# B1L103S, U26-ch61, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



# B1L103S, U26-ch62, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	84
Mean	22.83
Std Dev	10.44

**Gaus mean : 28.1244**

**Gaus Width: 4.3441**

Entry

12

10

8

6

4

2

0

ampl

0

10

20

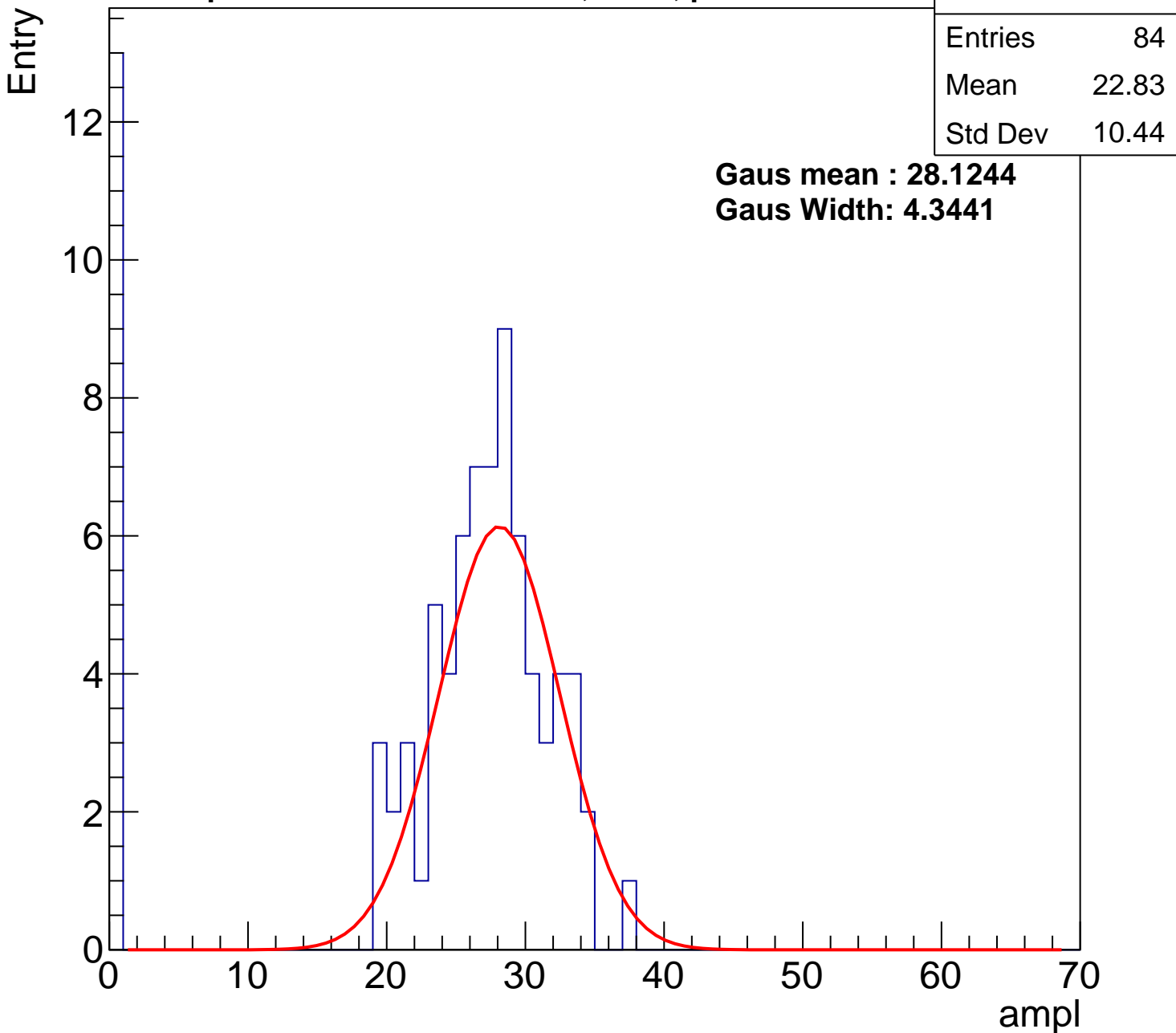
30

40

50

60

70



# B1L103S, U26-ch62, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	72
Mean	26.86
Std Dev	14.15

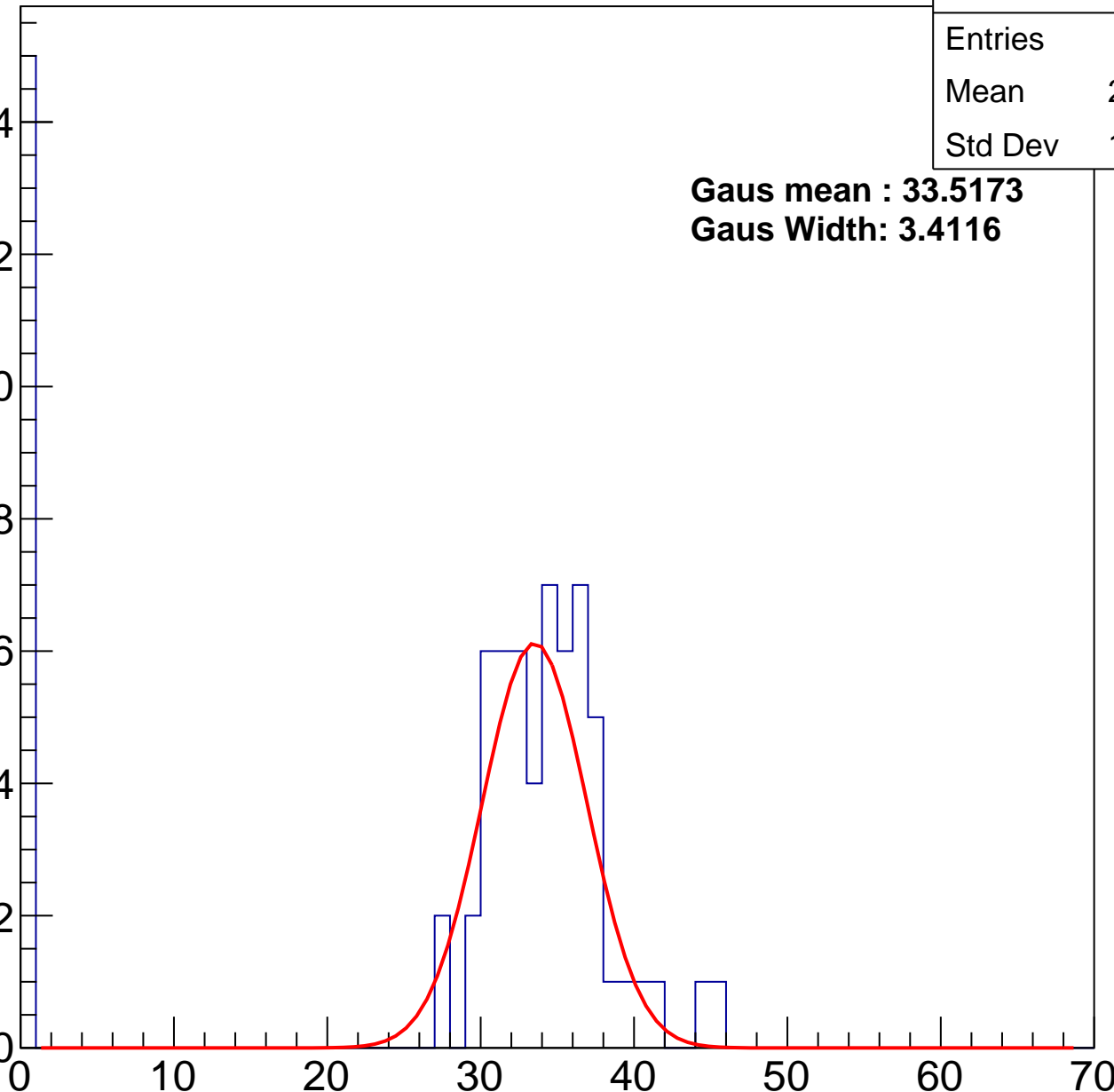
**Gaus mean : 33.5173**

**Gaus Width: 3.4116**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U26-ch62, adc2

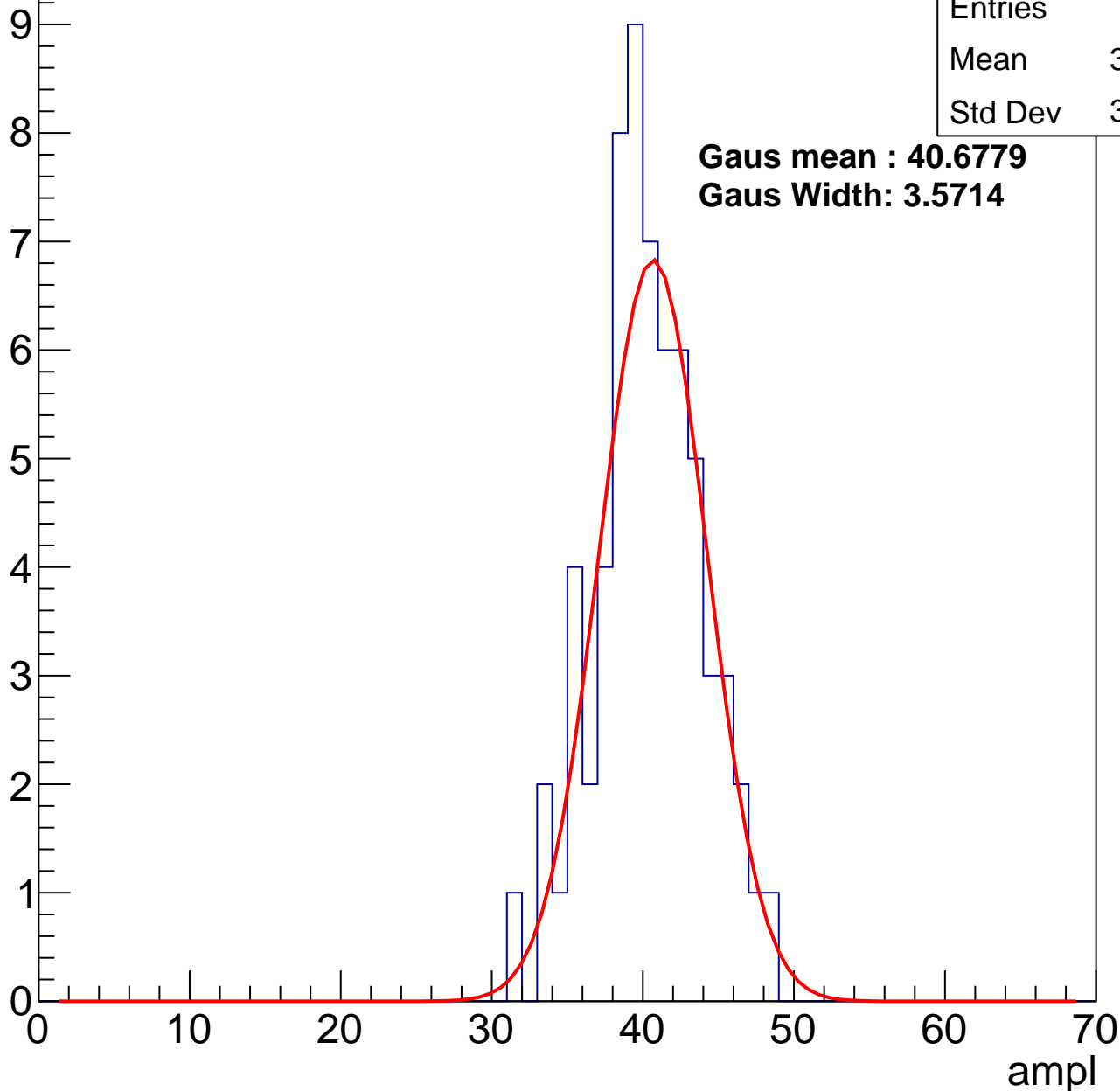
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	65
Mean	39.89
Std Dev	3.522

**Gaus mean : 40.6779**

**Gaus Width: 3.5714**

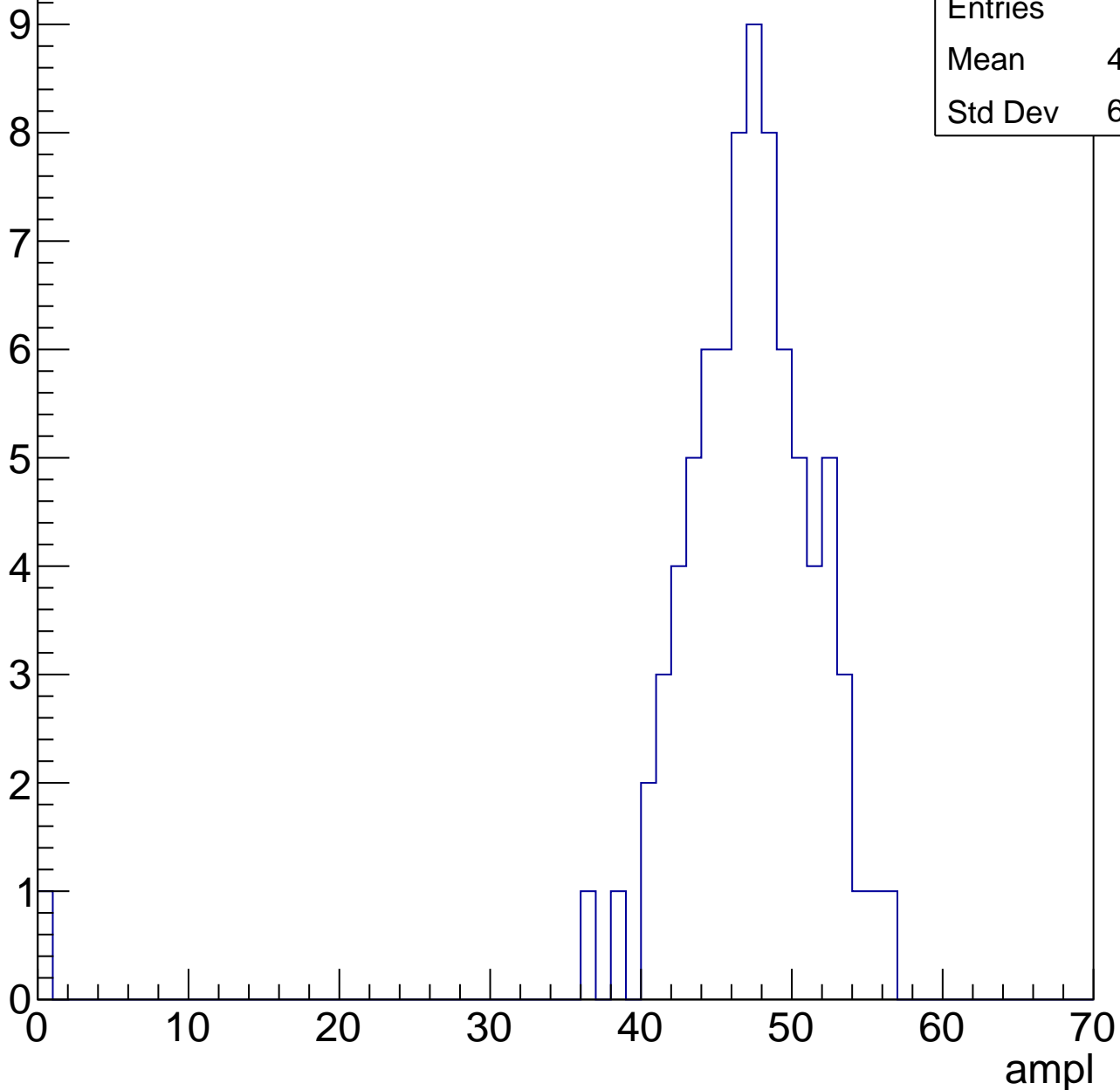


# B1L103S, U26-ch62, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	80
Mean	46.26
Std Dev	6.526

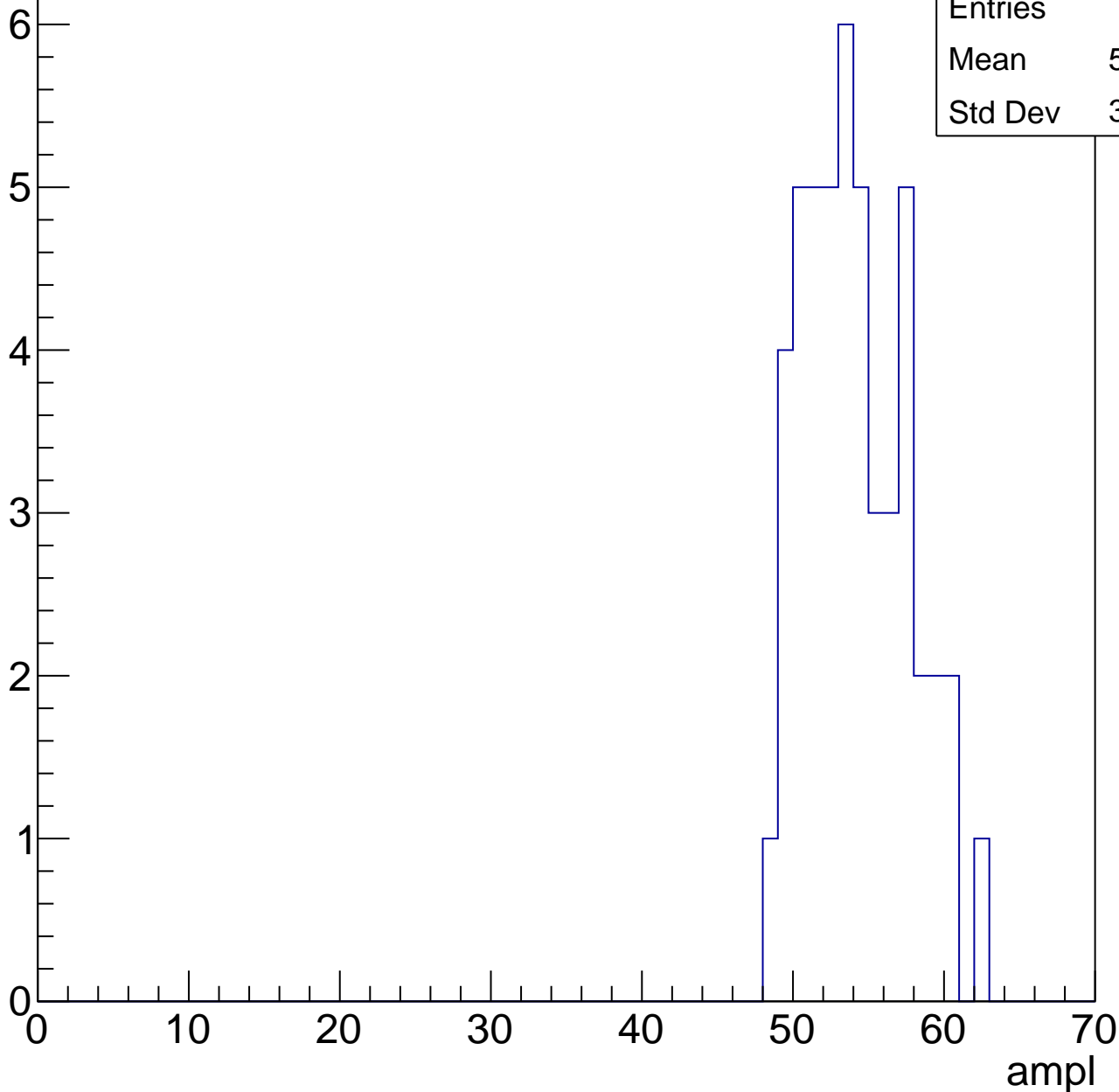


# B1L103S, U26-ch62, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	49
Mean	53.69
Std Dev	3.382

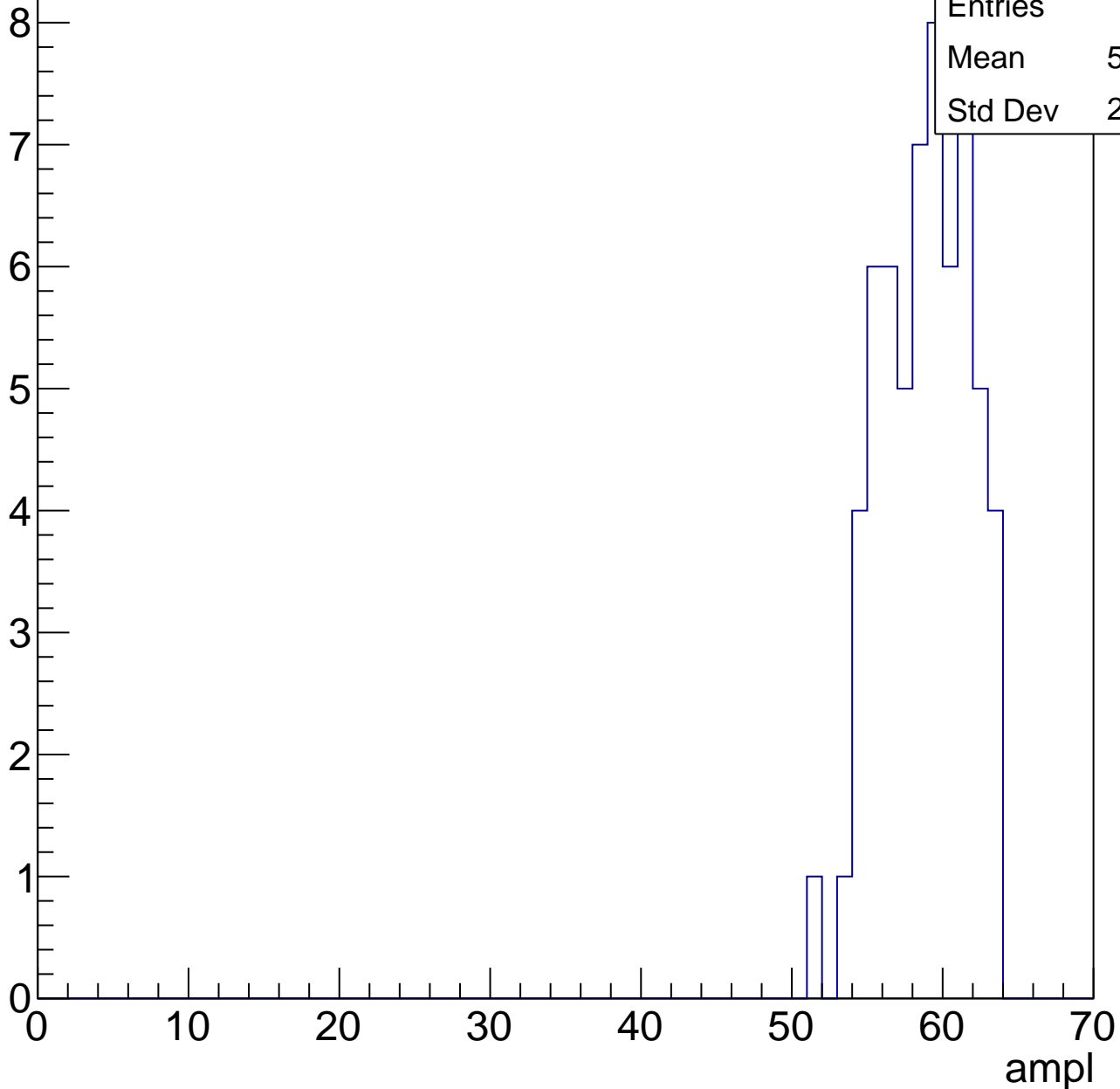


# B1L103S, U26-ch62, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	61
Mean	58.34
Std Dev	2.857

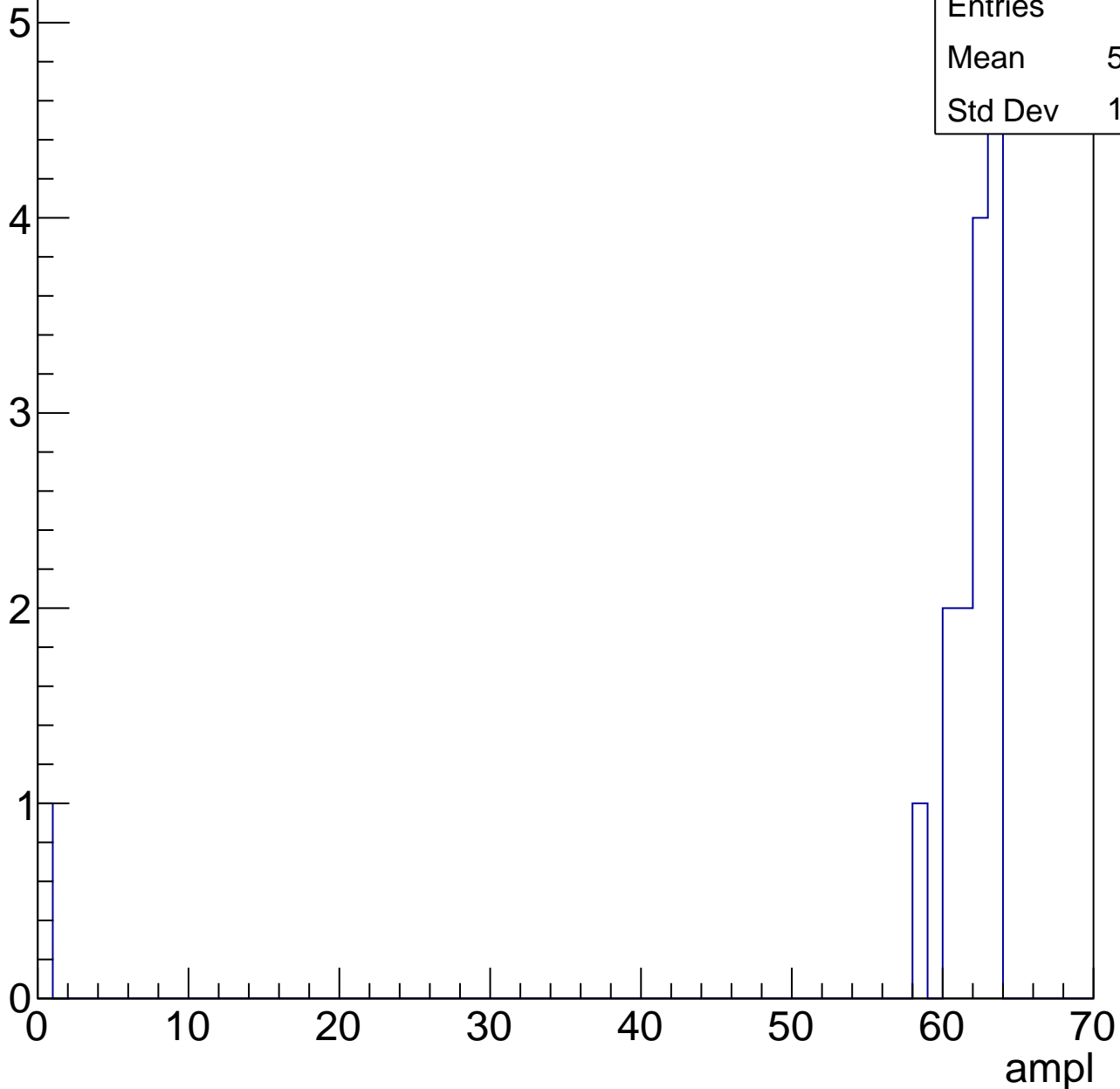


# B1L103S, U26-ch62, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	15
Mean	57.53
Std Dev	15.44





# B1L103S, U26-ch62, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	19
Mean	3.316
Std Dev	14.07

Entry



# B1L103S, U26-ch63, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

10

8

6

4

2

0

0

10

20

30

40

50

60

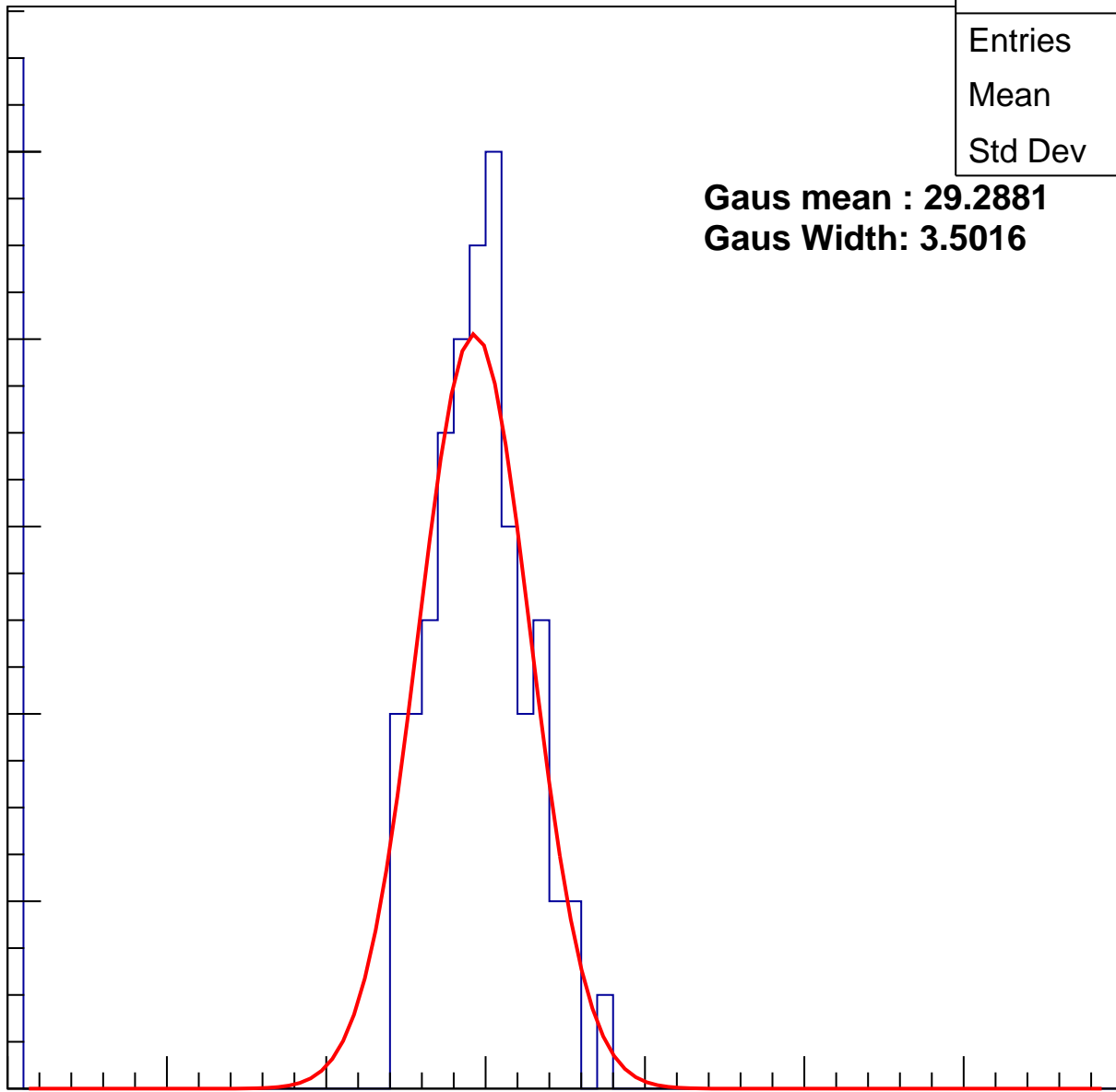
70

ampl

Entries	78
Mean	25.05
Std Dev	10.51

**Gaus mean : 29.2881**

**Gaus Width: 3.5016**



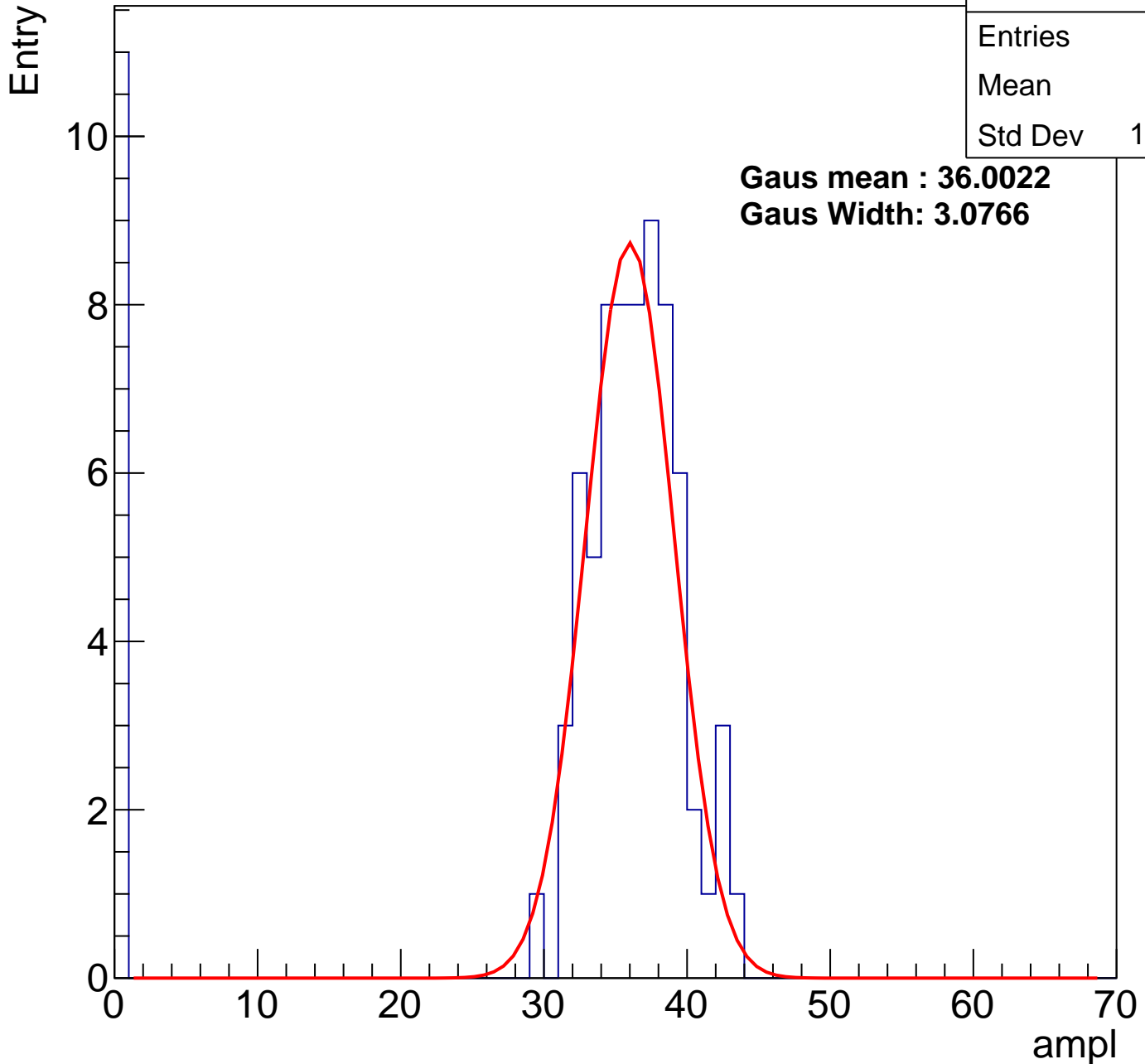
# B1L103S, U26-ch63, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	80
Mean	31
Std Dev	12.68

**Gaus mean : 36.0022**

**Gaus Width: 3.0766**



# B1L103S, U26-ch63, adc2

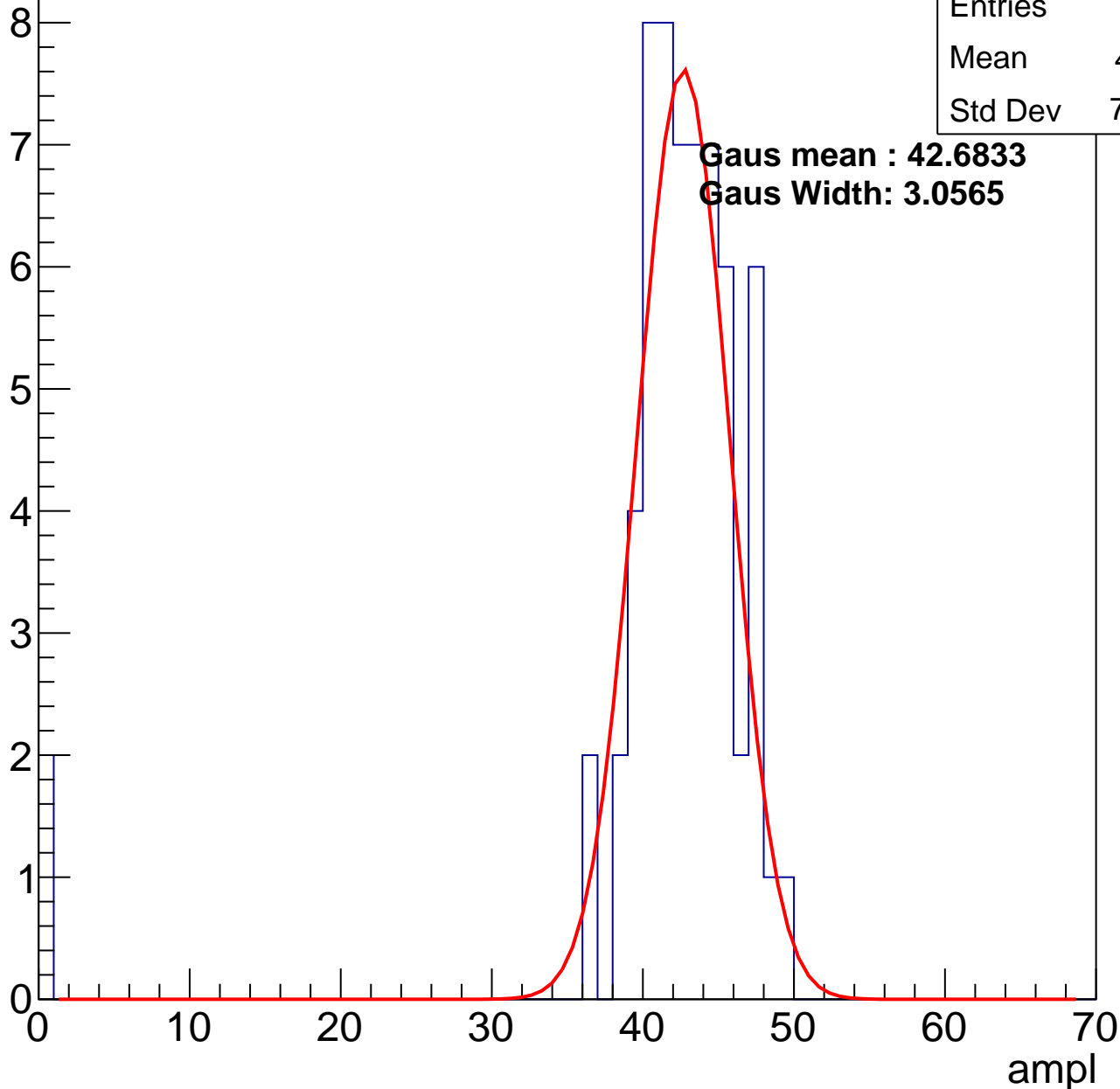
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	63
Mean	41.21
Std Dev	7.992

**Gaus mean : 42.6833**

**Gaus Width: 3.0565**



# B1L103S, U26-ch63, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	79
Mean	49.44
Std Dev	3.371

Entry

10

8

6

4

2

0

0

10

20

30

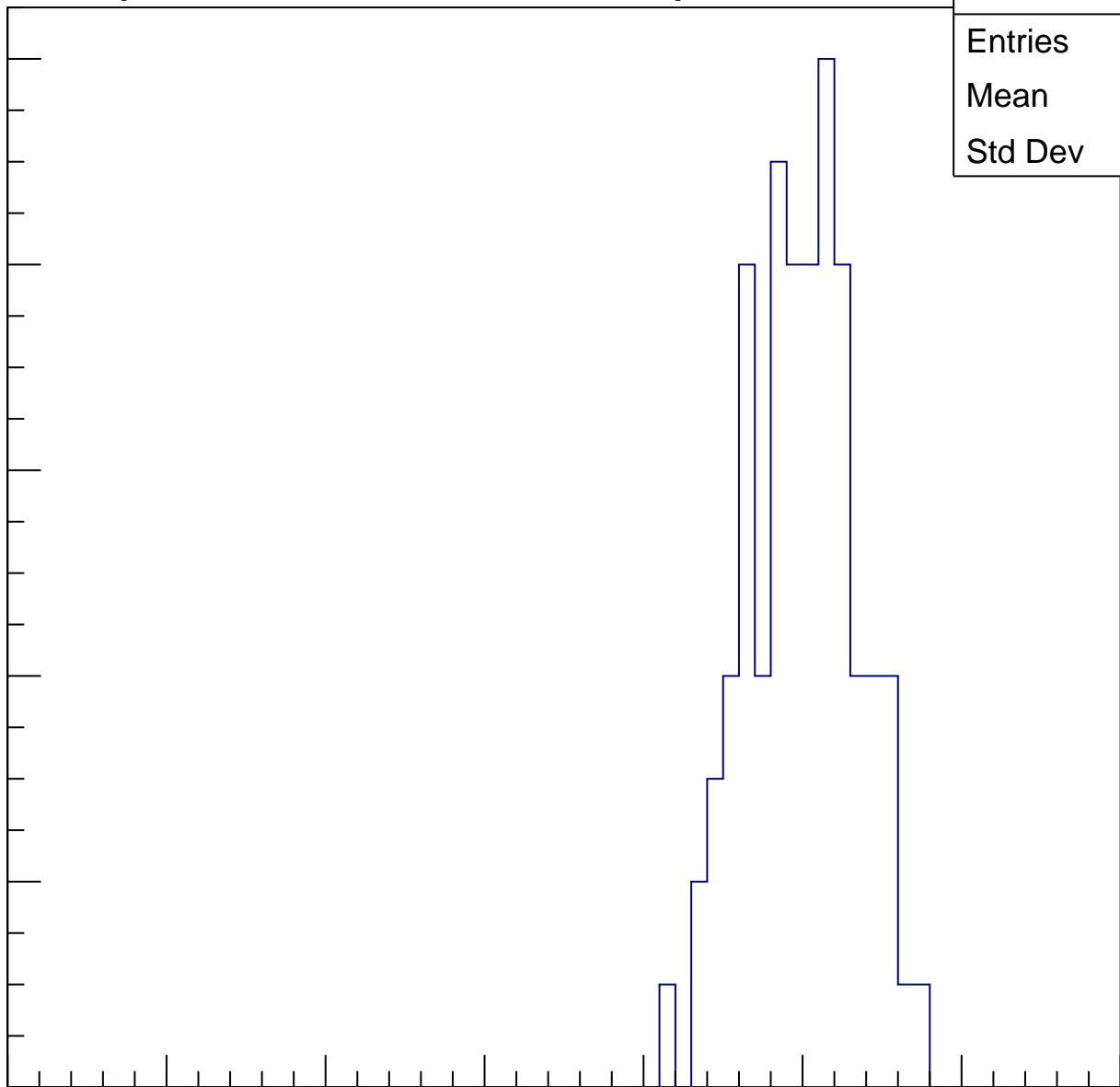
40

50

60

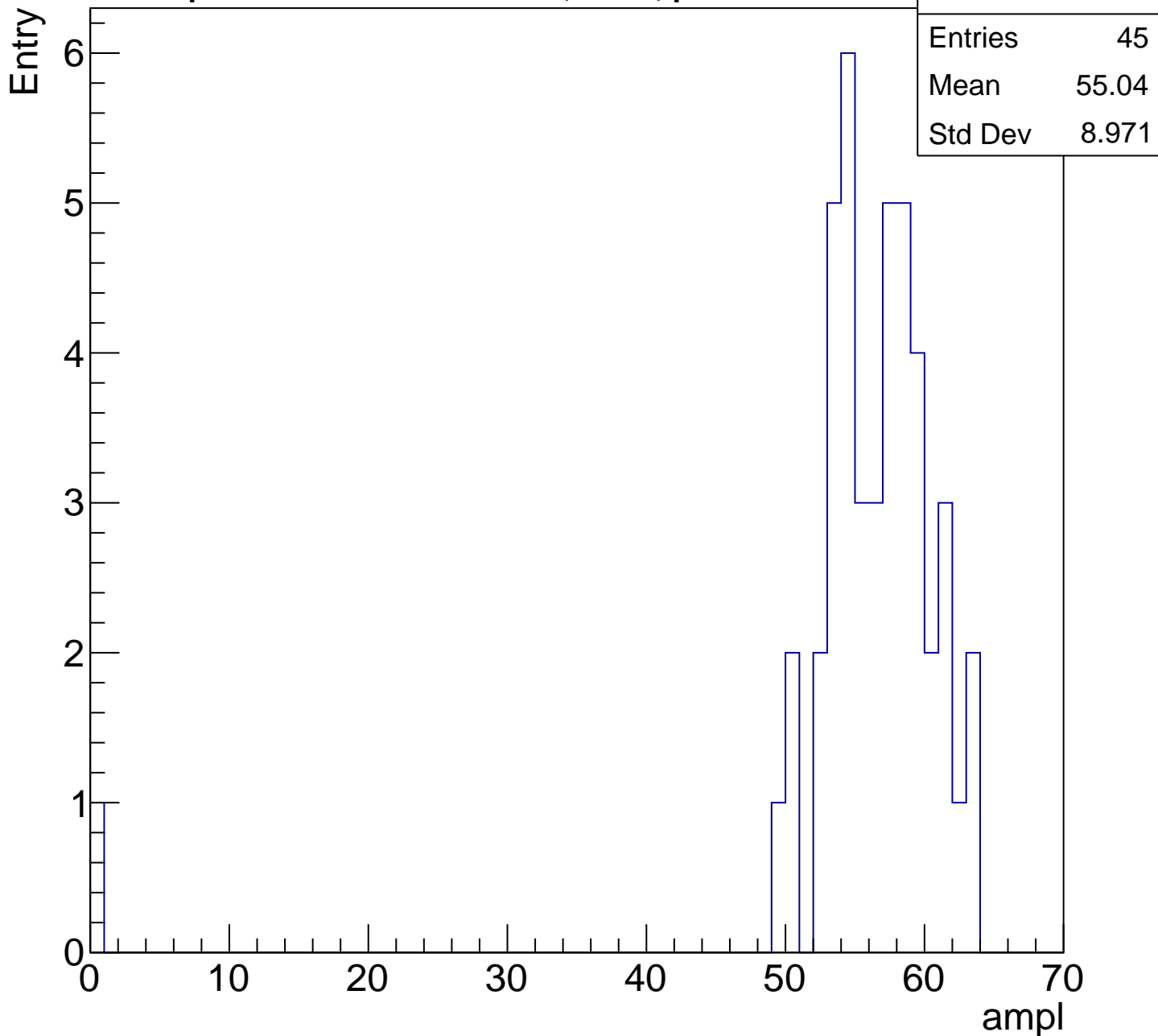
70

ampl



# B1L103S, U26-ch63, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

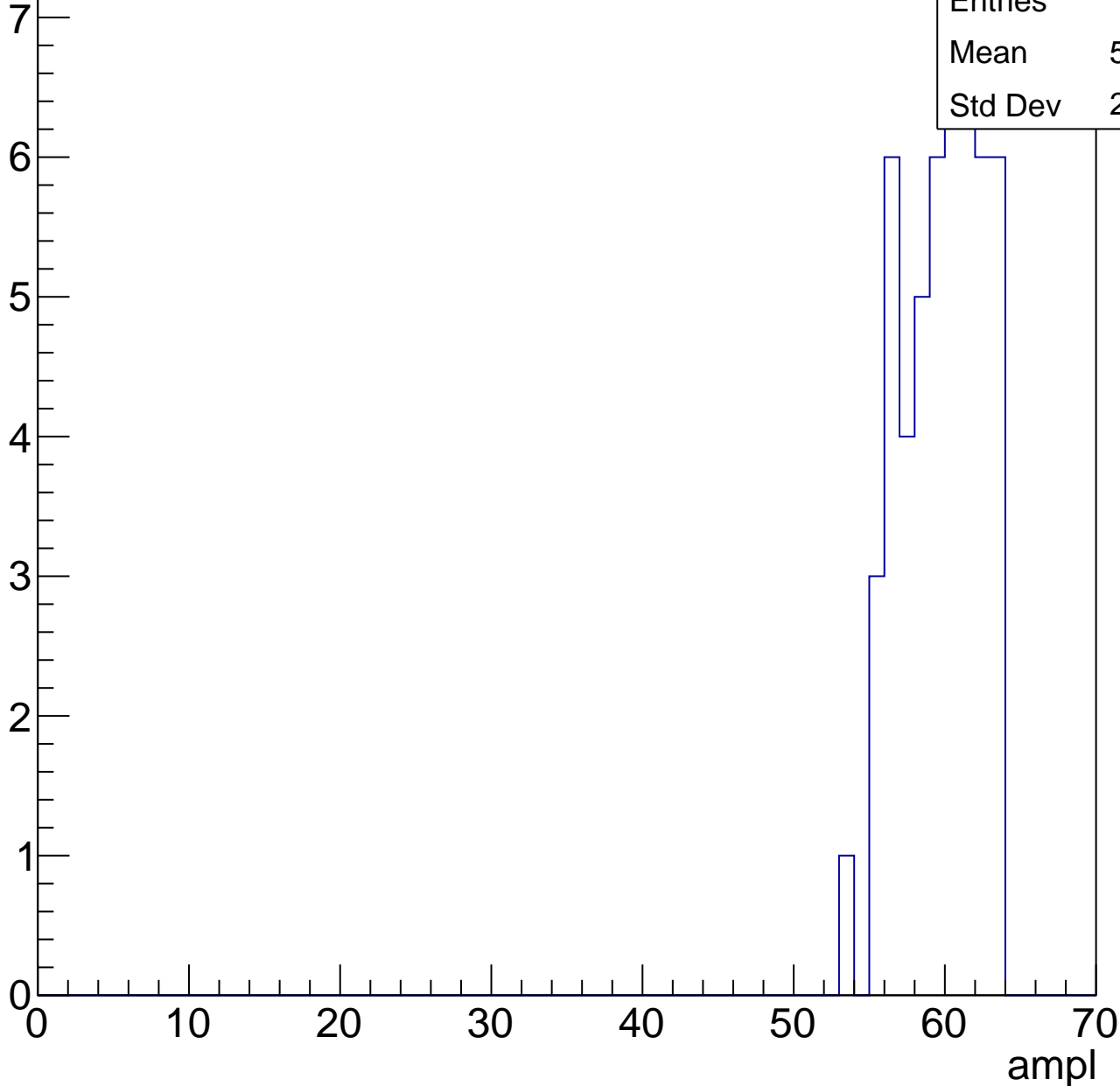


# B1L103S, U26-ch63, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

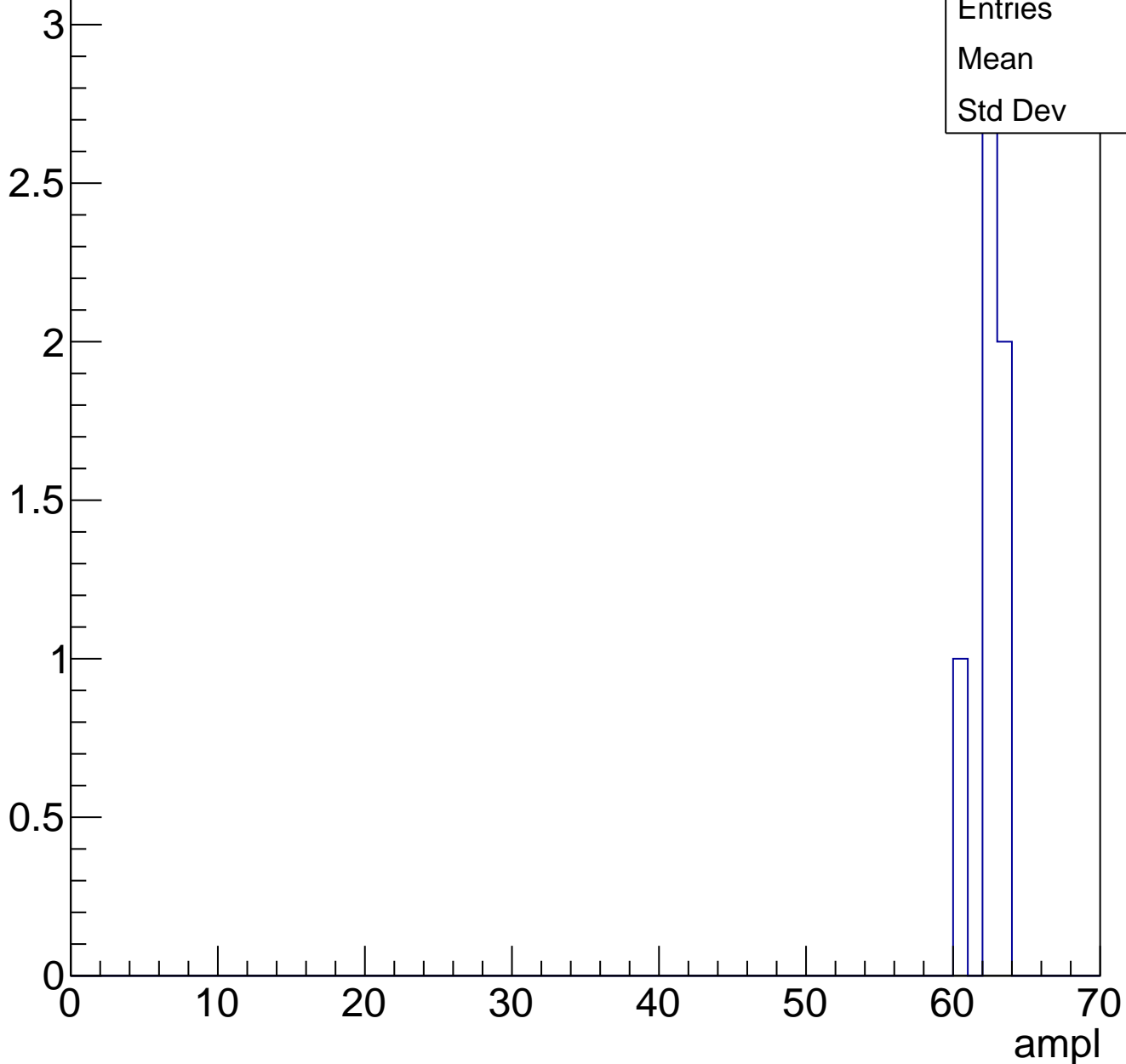
Entries	51
Mean	59.27
Std Dev	2.583



# B1L103S, U26-ch63, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry





# B1L103S, U26-ch63, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	19
Mean	1.211
Std Dev	5.136

Entry



# B1L103S, U26-ch64, adc0

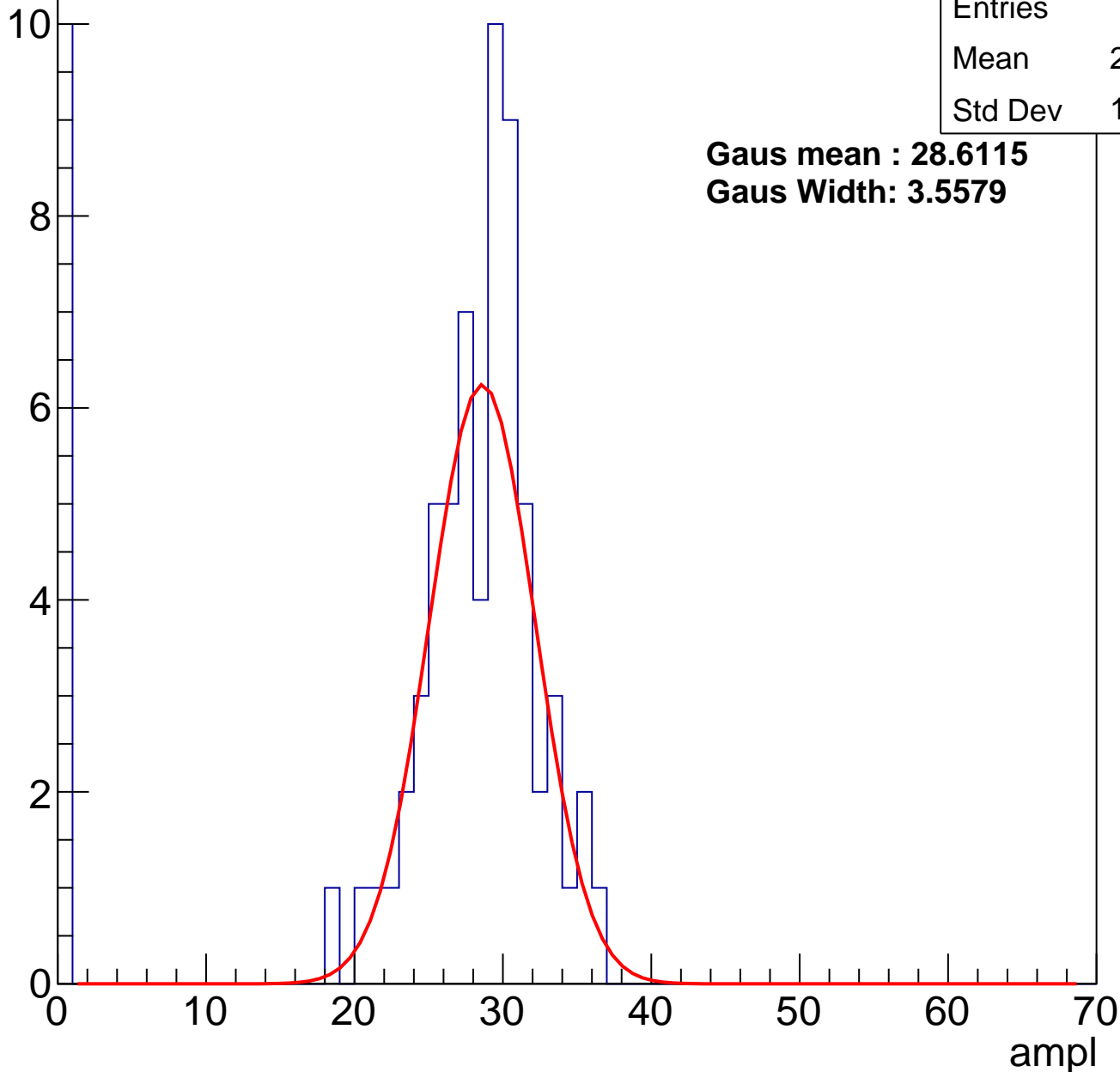
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	73
Mean	24.29
Std Dev	10.24

**Gaus mean : 28.6115**

**Gaus Width: 3.5579**

Entry



# B1L103S, U26-ch64, adc1

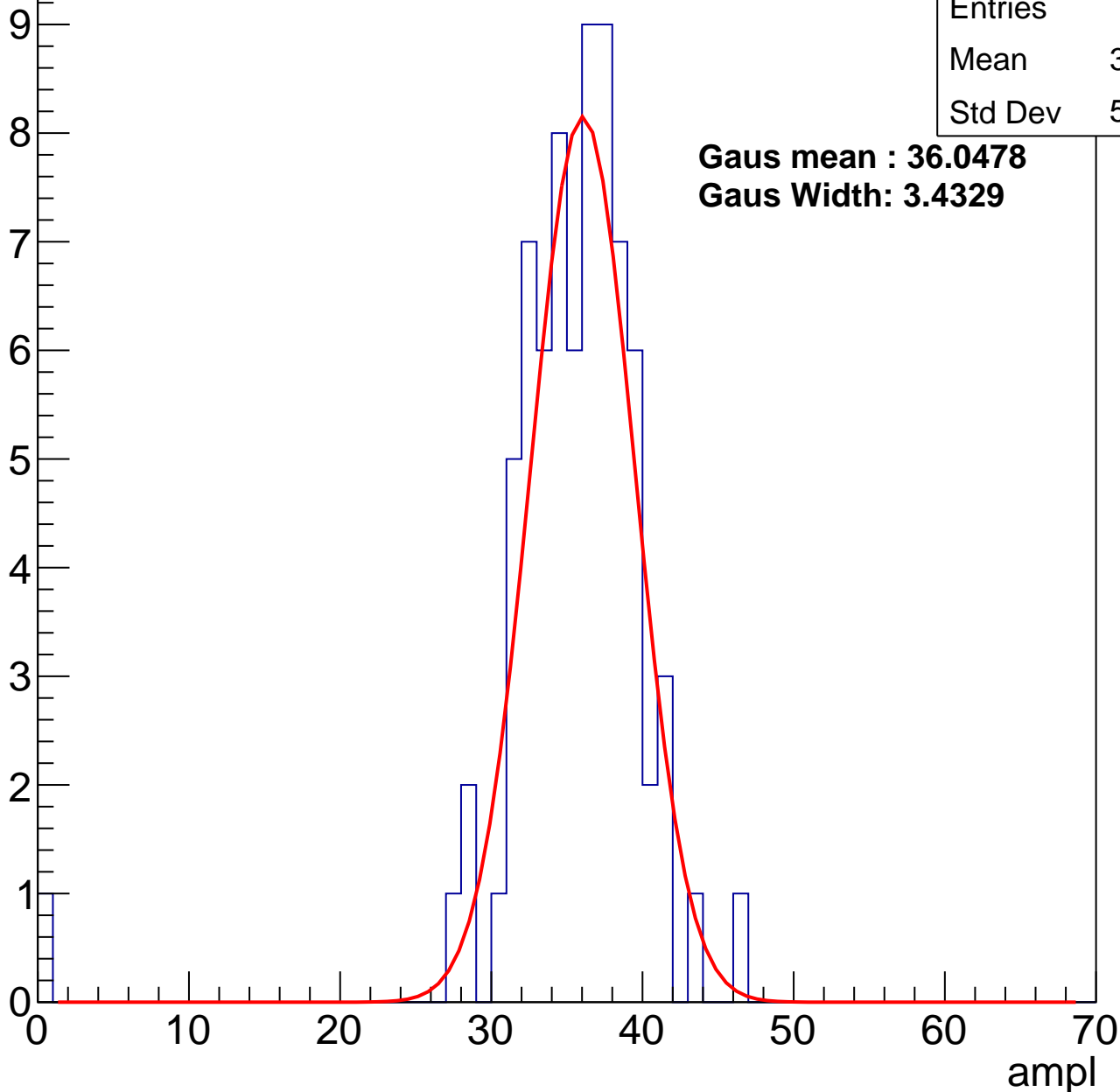
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	75
Mean	34.95
Std Dev	5.334

**Gaus mean : 36.0478**

**Gaus Width: 3.4329**



# B1L103S, U26-ch64, adc2

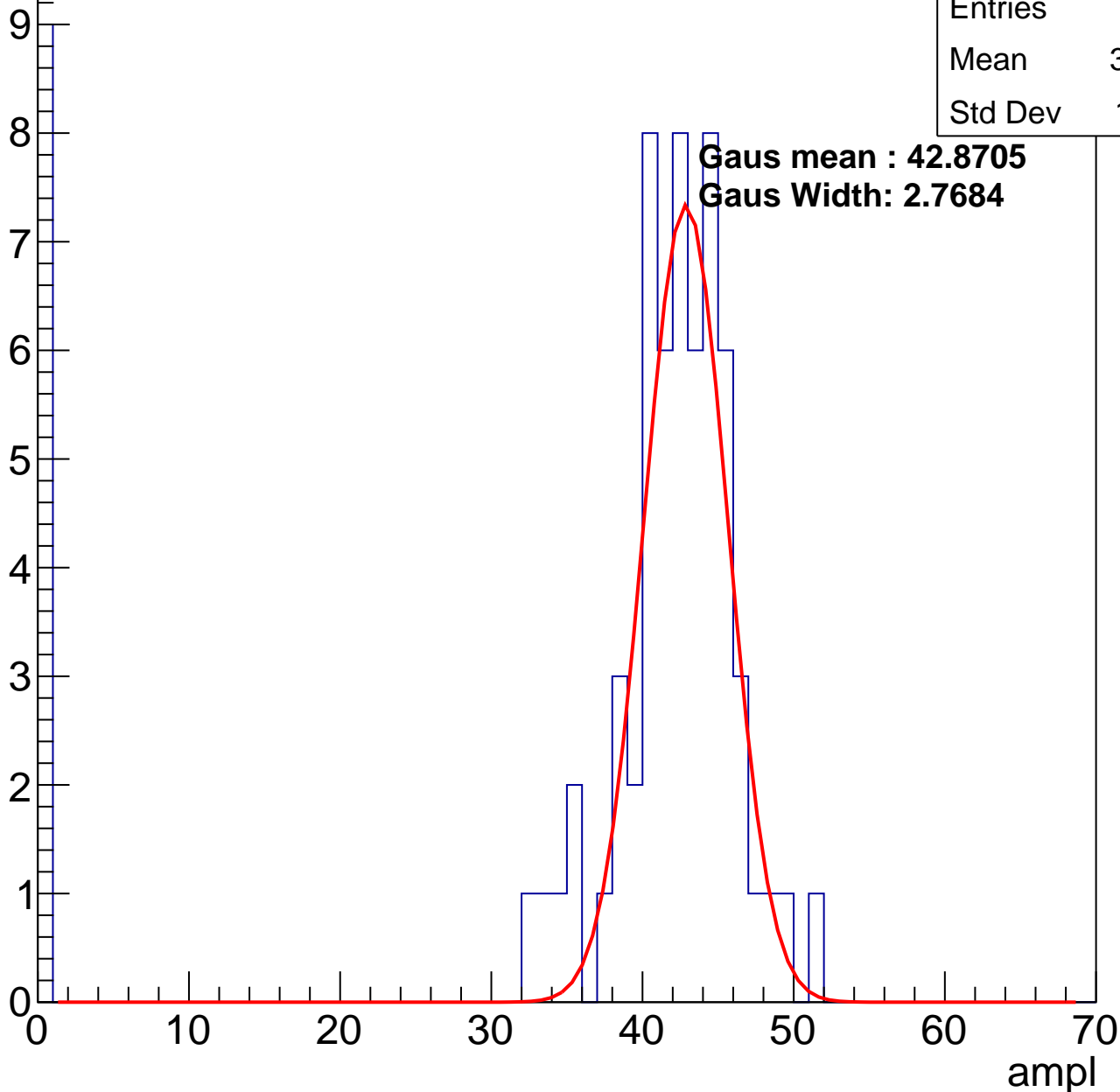
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	69
Mean	36.42
Std Dev	14.51

**Gaus mean : 42.8705**

**Gaus Width: 2.7684**

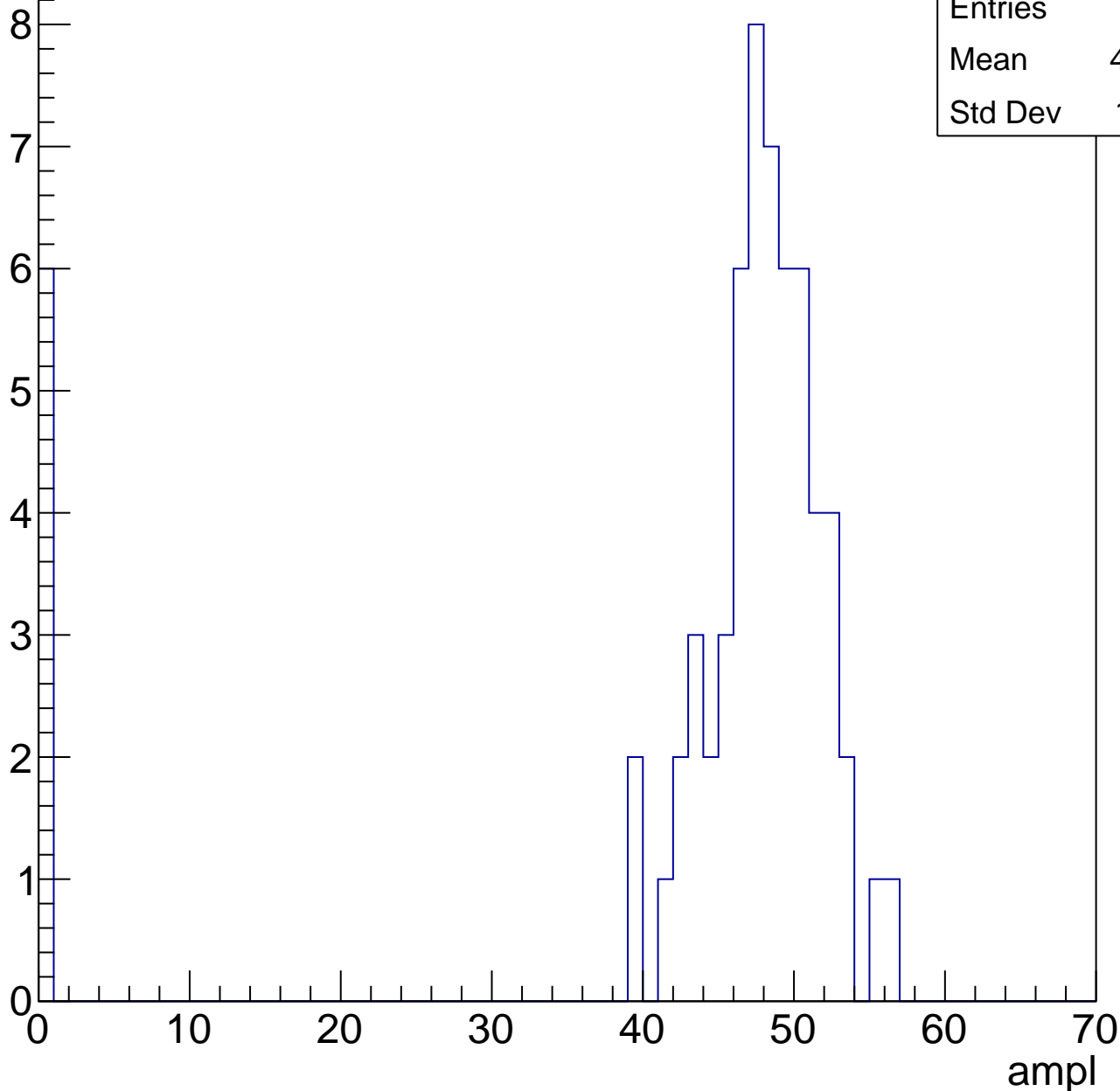


# B1L103S, U26-ch64, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	64
Mean	43.22
Std Dev	14.31

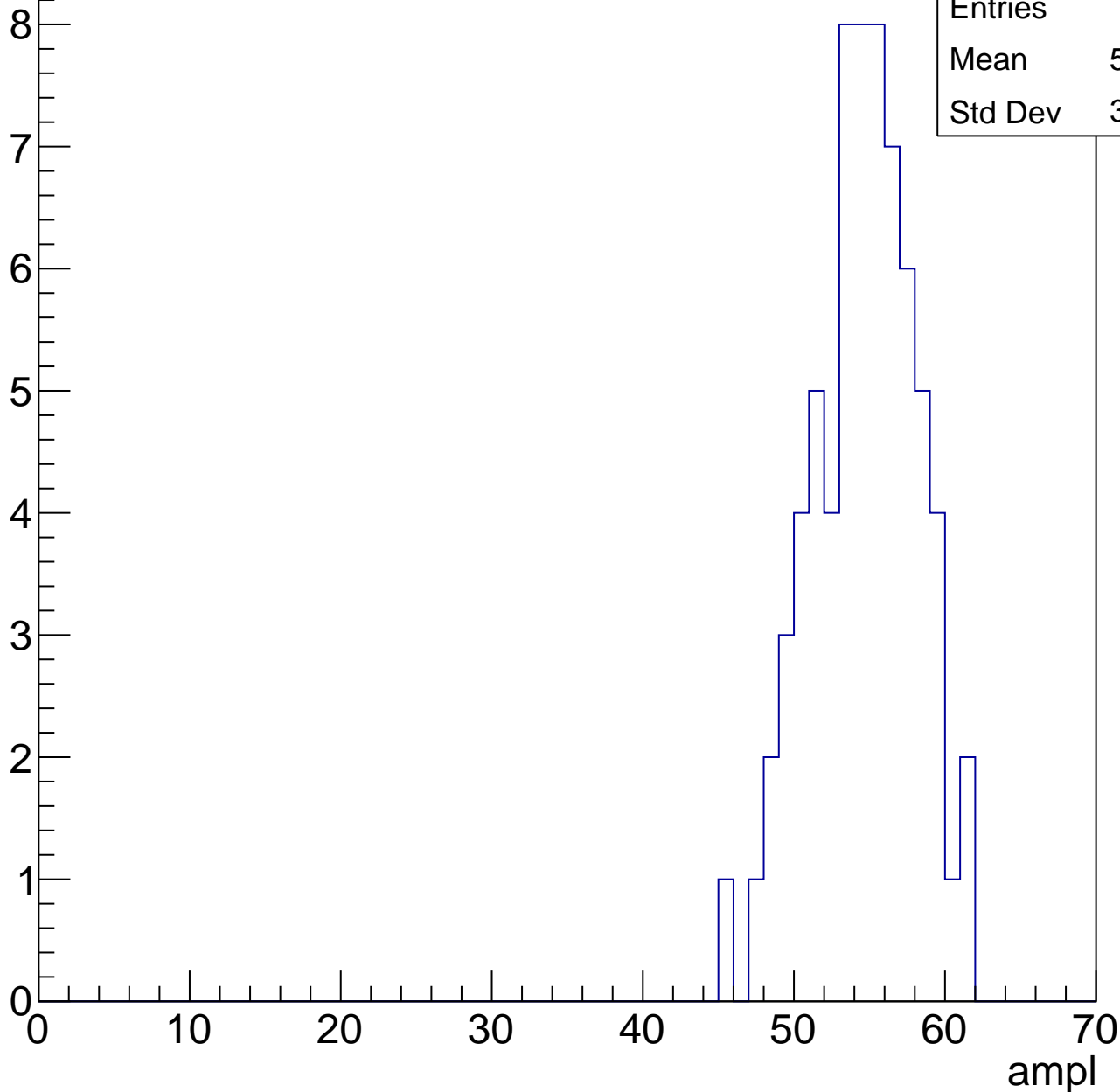


# B1L103S, U26-ch64, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	69
Mean	54.14
Std Dev	3.432



# B1L103S, U26-ch64, adc5

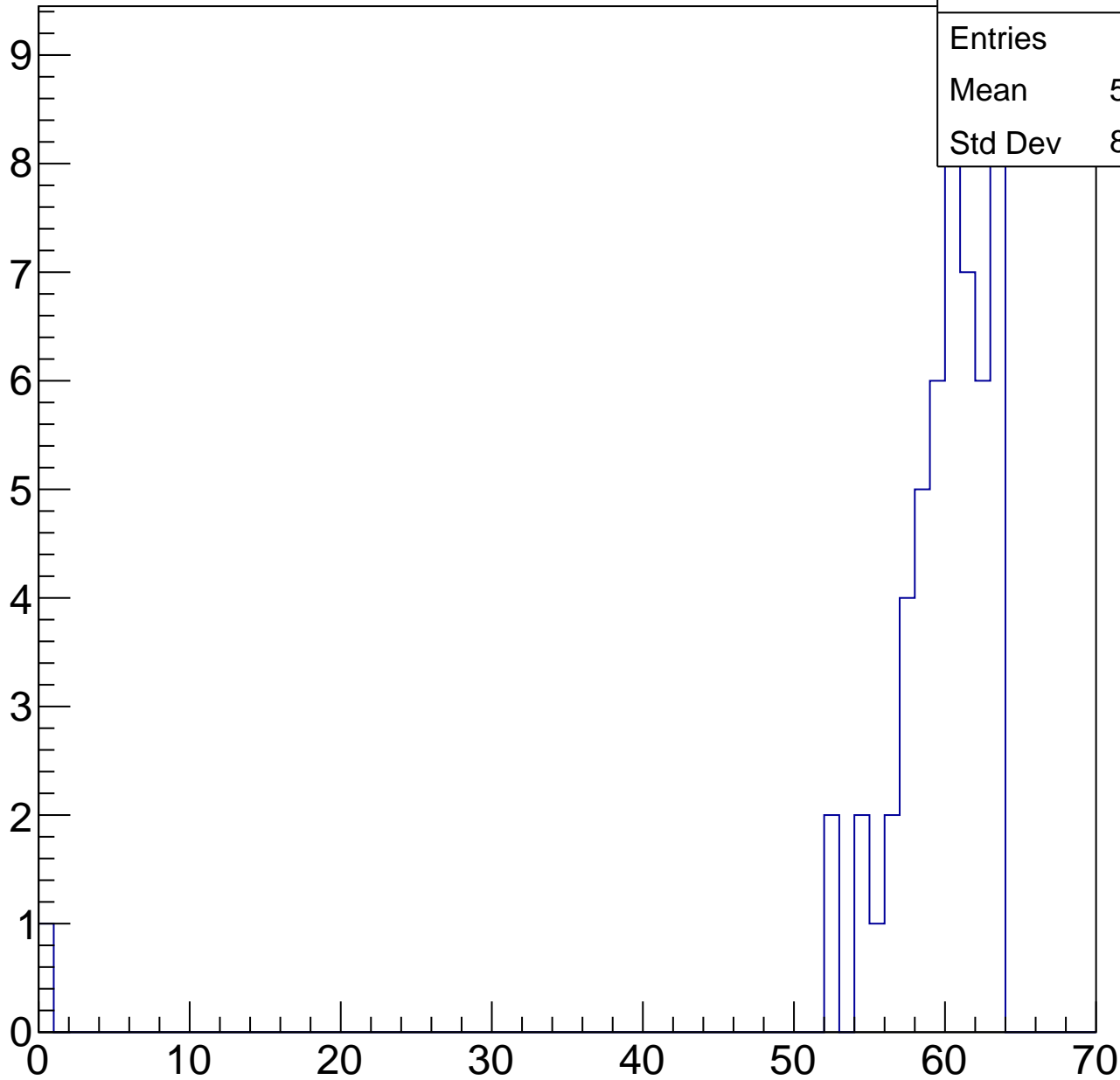
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	53
Mean	58.38
Std Dev	8.559

ampl



# B1L103S, U26-ch64, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry





# B1L103S, U26-ch64, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



# B1L103S, U26-ch65, adc0

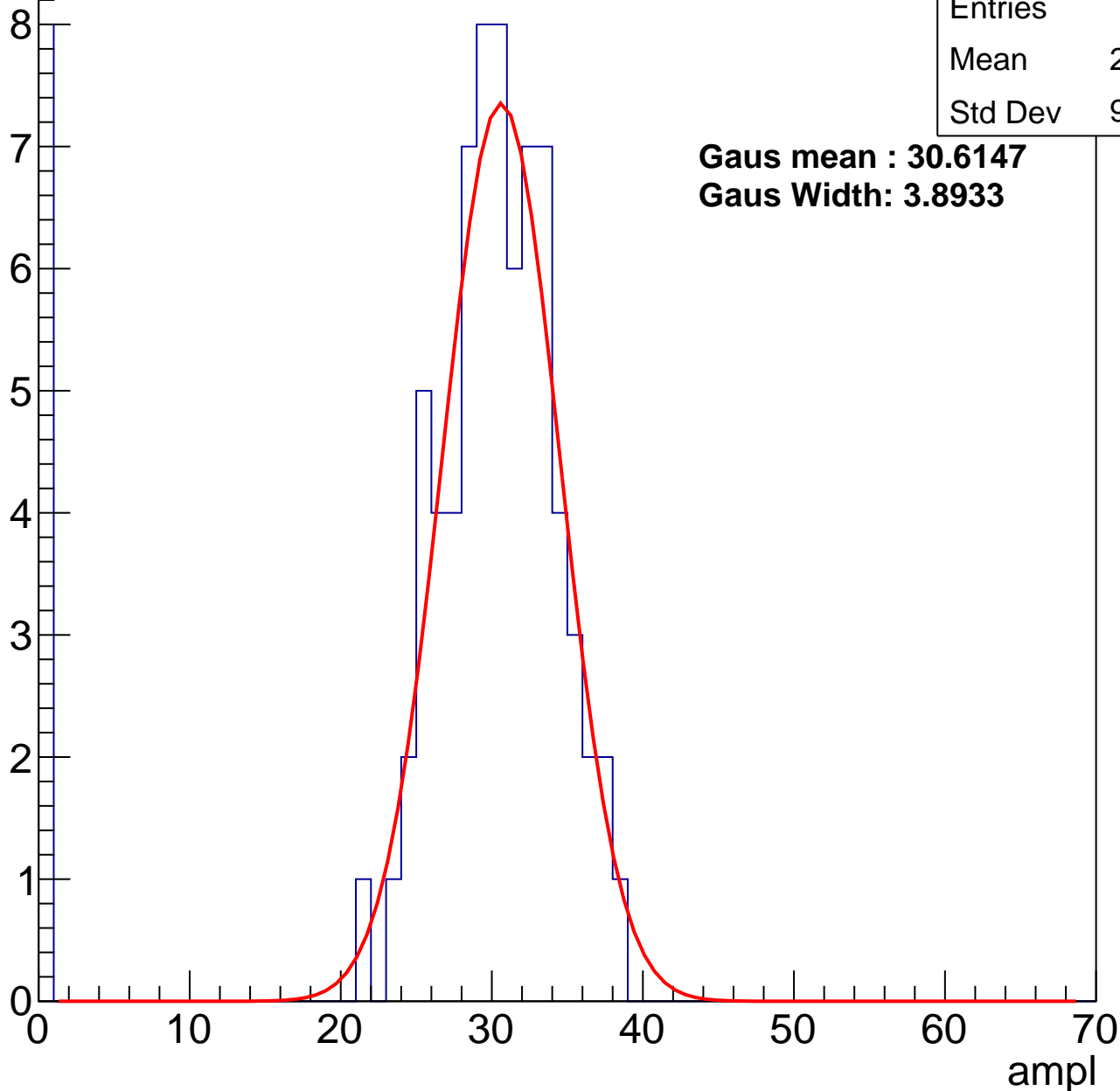
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	80
Mean	27.04
Std Dev	9.638

**Gaus mean : 30.6147**

**Gaus Width: 3.8933**



# B1L103S, U26-ch65, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	72
Mean	31.89
Std Dev	13.3

**Gaus mean : 37.0885**

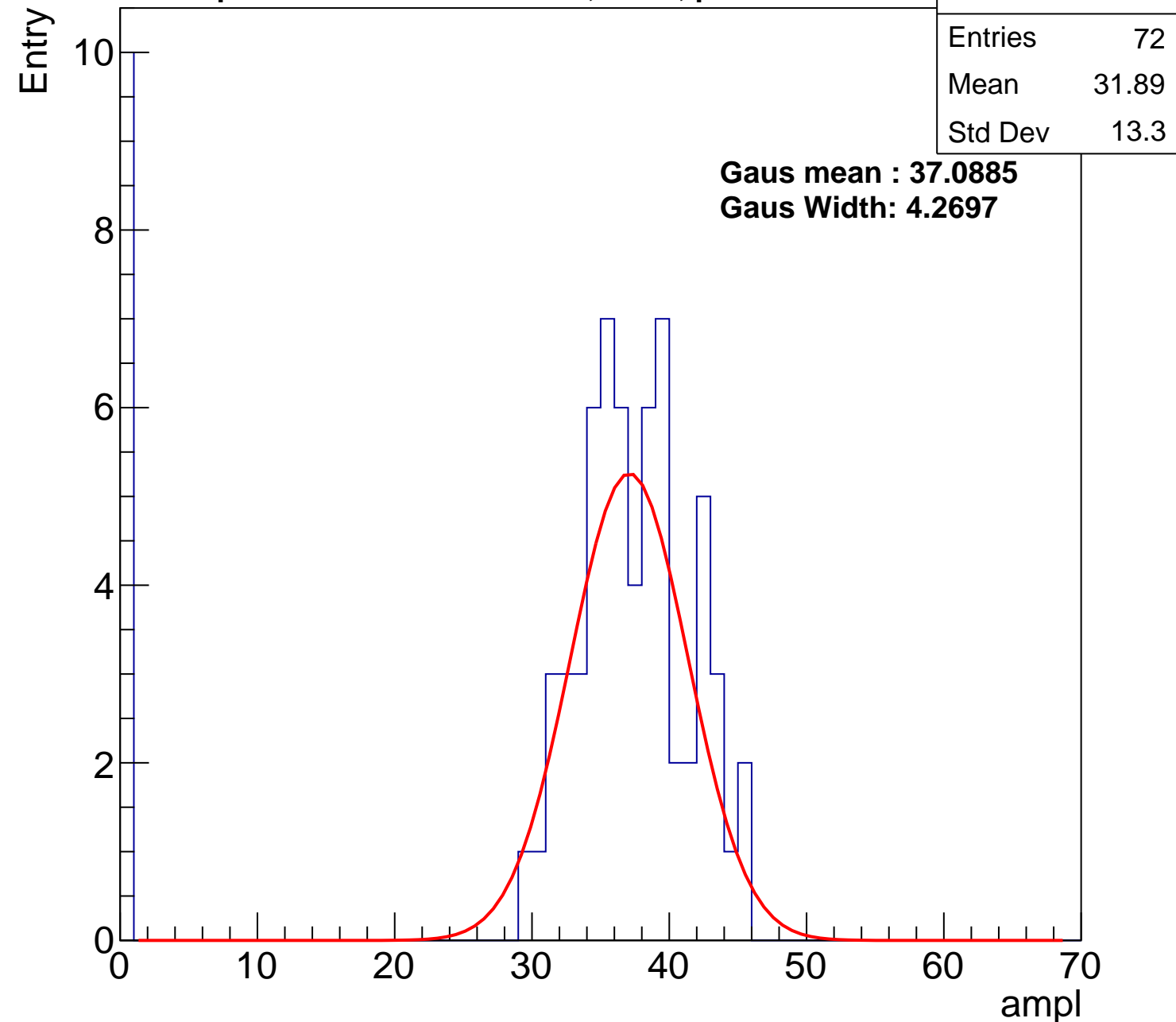
**Gaus Width: 4.2697**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U26-ch65, adc2

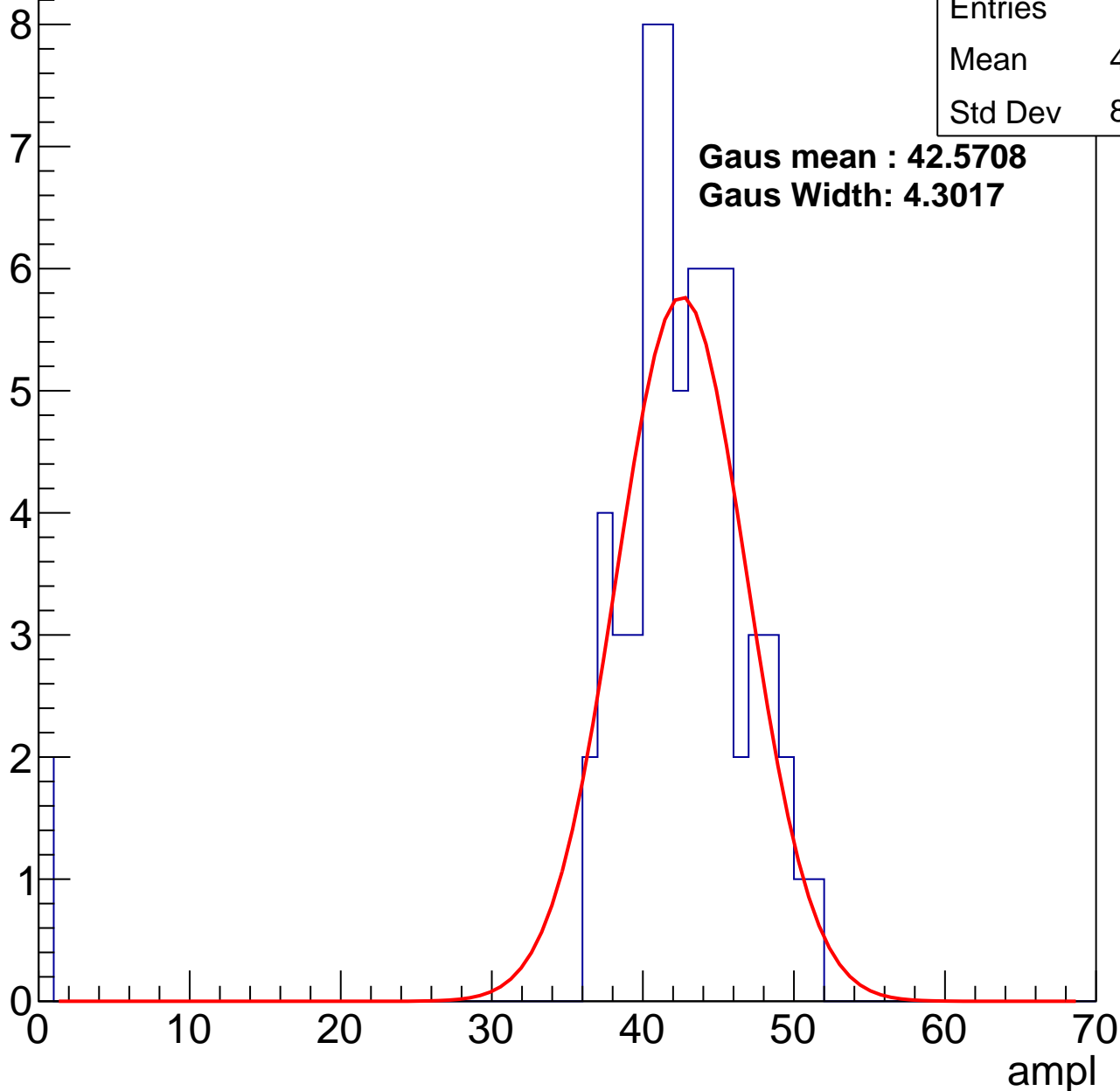
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	65
Mean	41.18
Std Dev	8.147

**Gaus mean : 42.5708**

**Gaus Width: 4.3017**

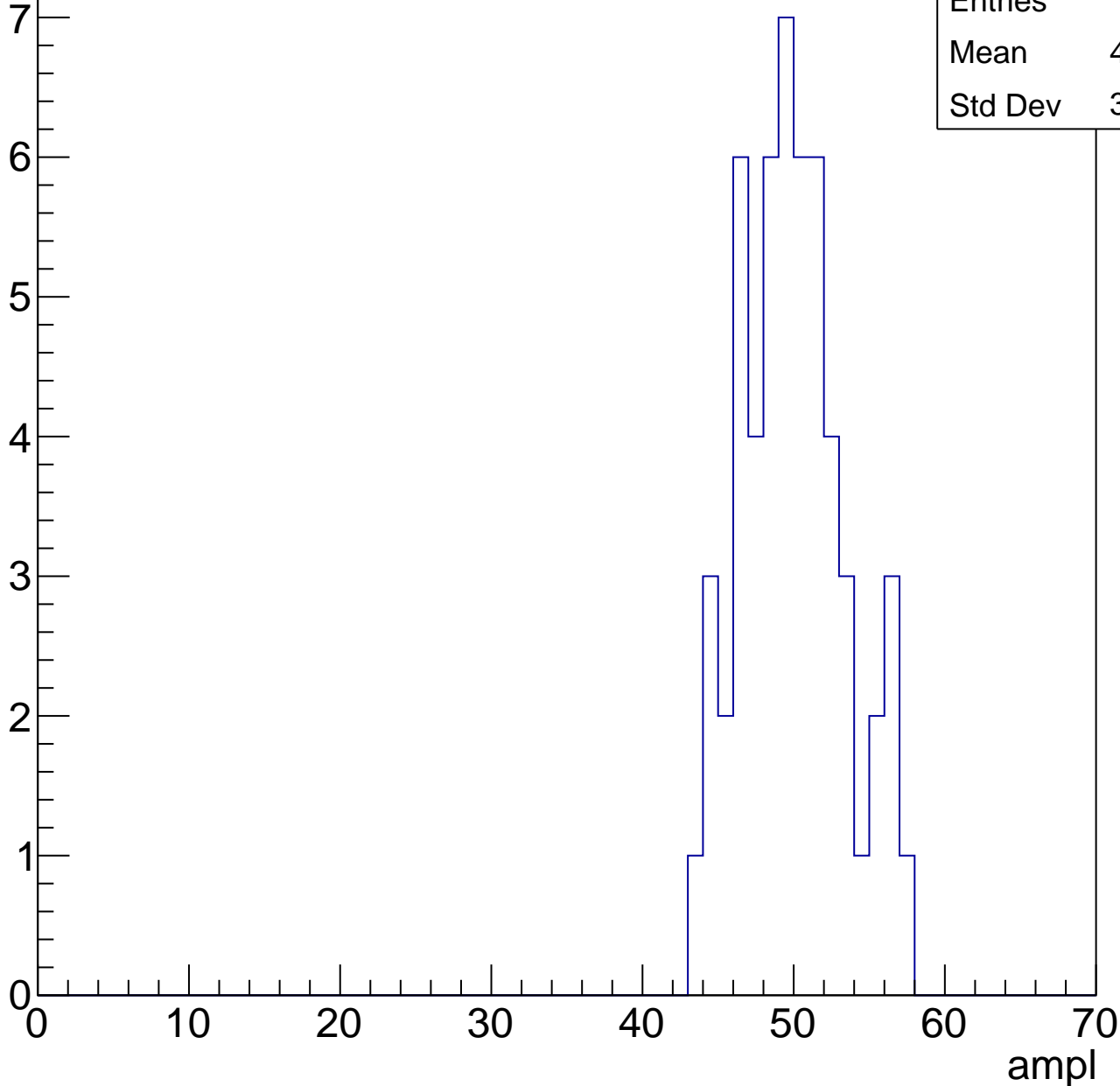


# B1L103S, U26-ch65, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	55
Mean	49.49
Std Dev	3.378

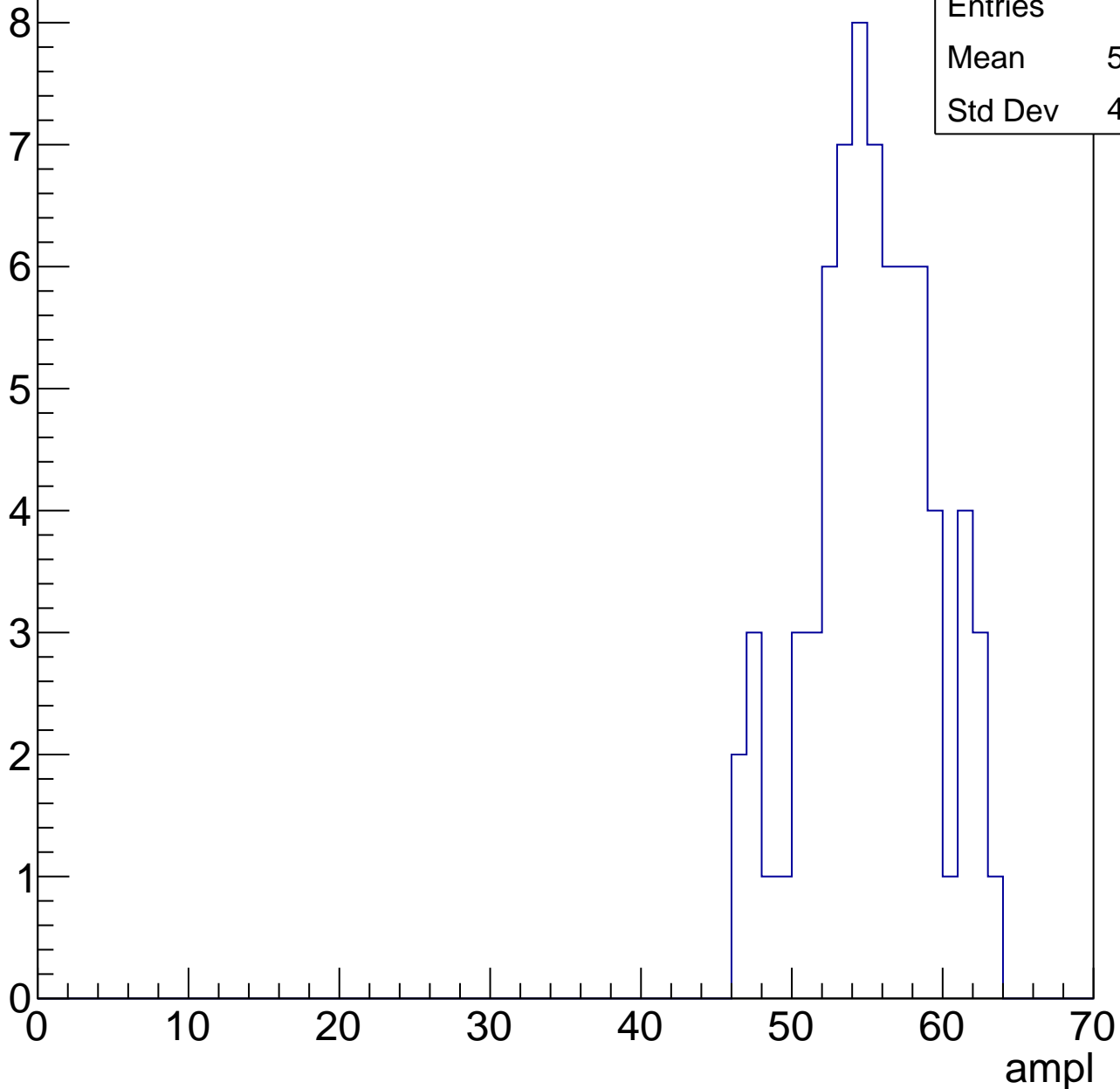


# B1L103S, U26-ch65, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

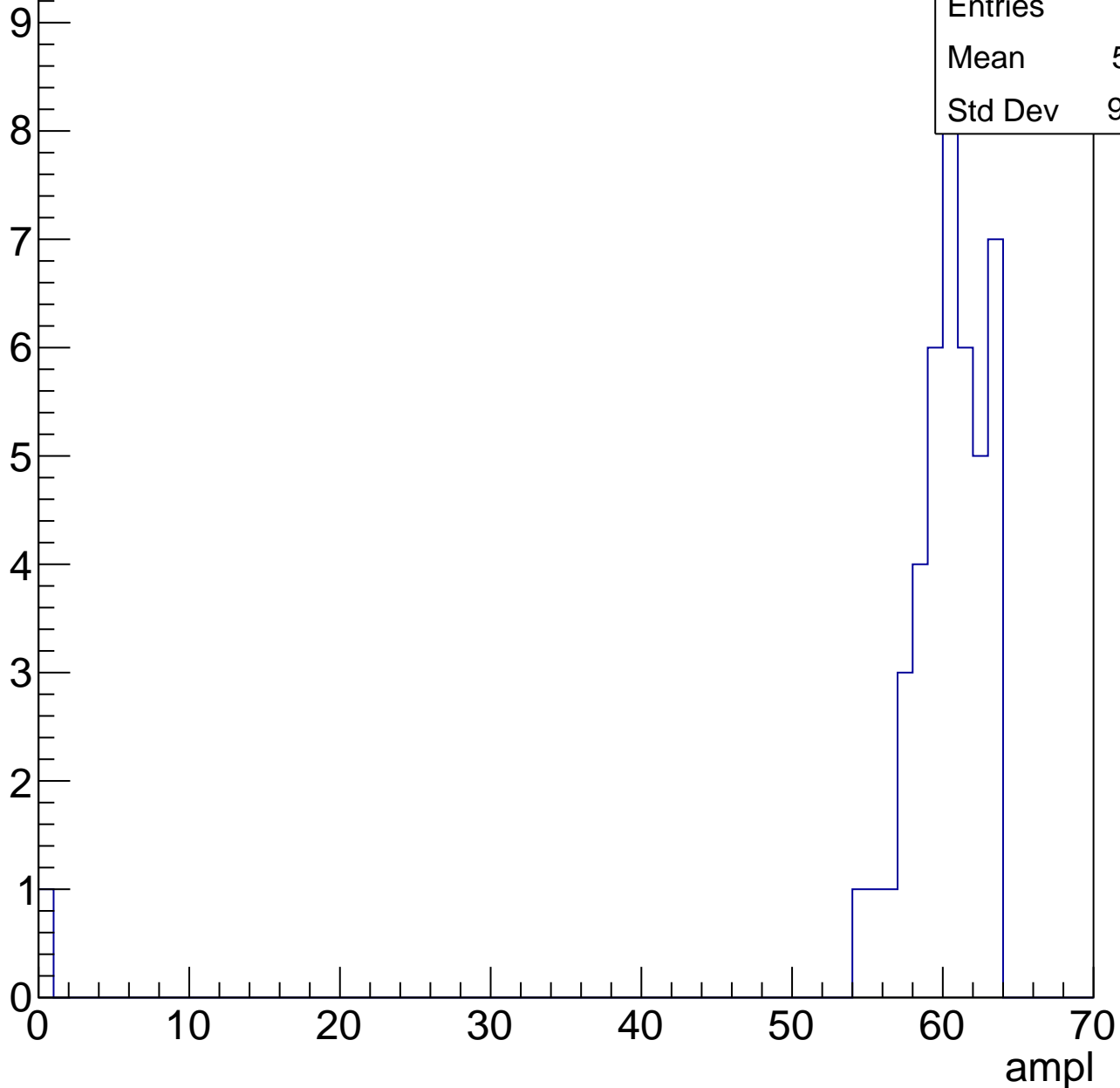
Entries	72
Mean	54.83
Std Dev	4.045



# B1L103S, U26-ch65, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



# B1L103S, U26-ch65, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry





# B1L103S, U26-ch65, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



# B1L103S, U26-ch66, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	81
Mean	23.51
Std Dev	11.77

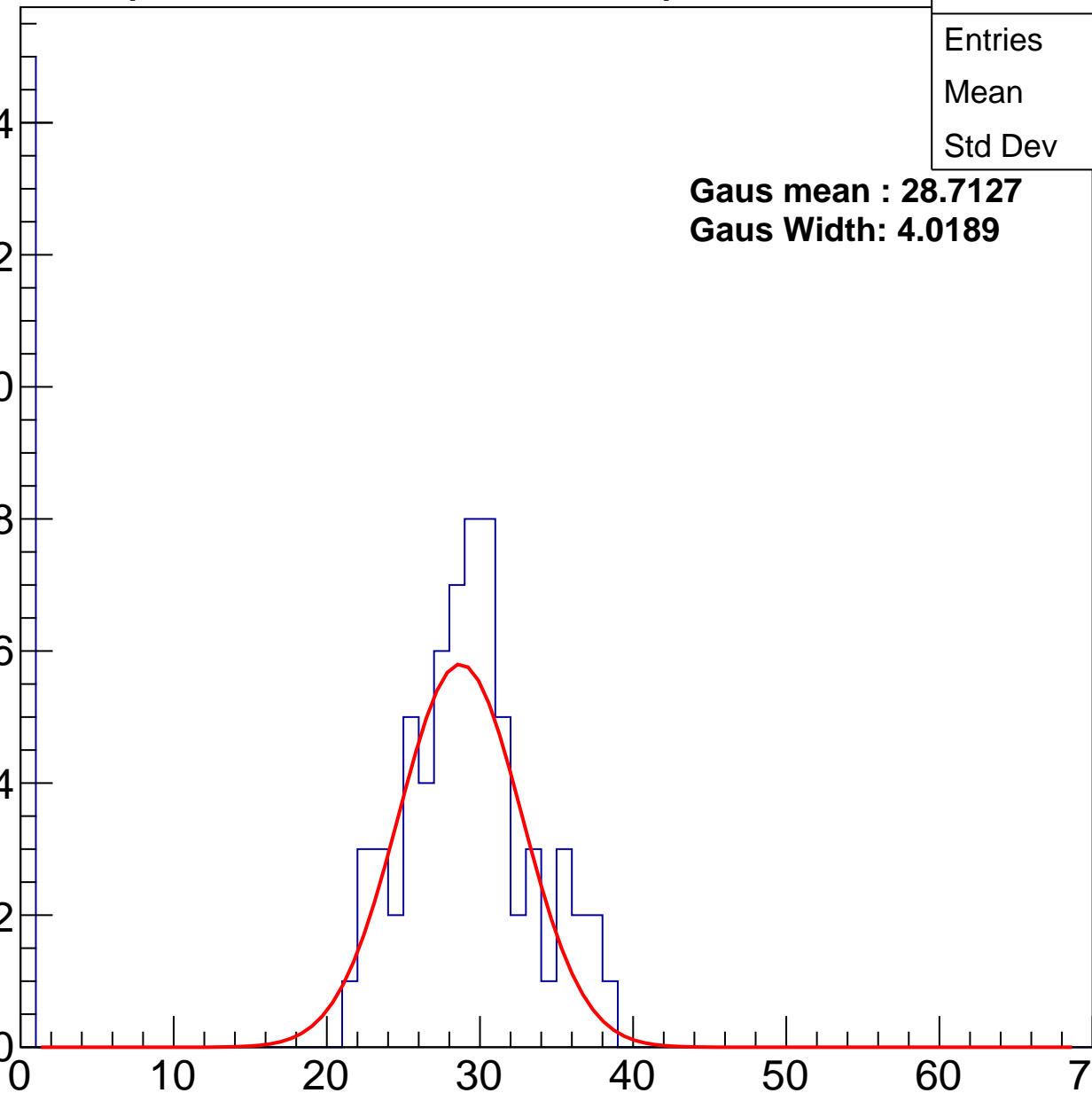
**Gaus mean : 28.7127**

**Gaus Width: 4.0189**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U26-ch66, adc1

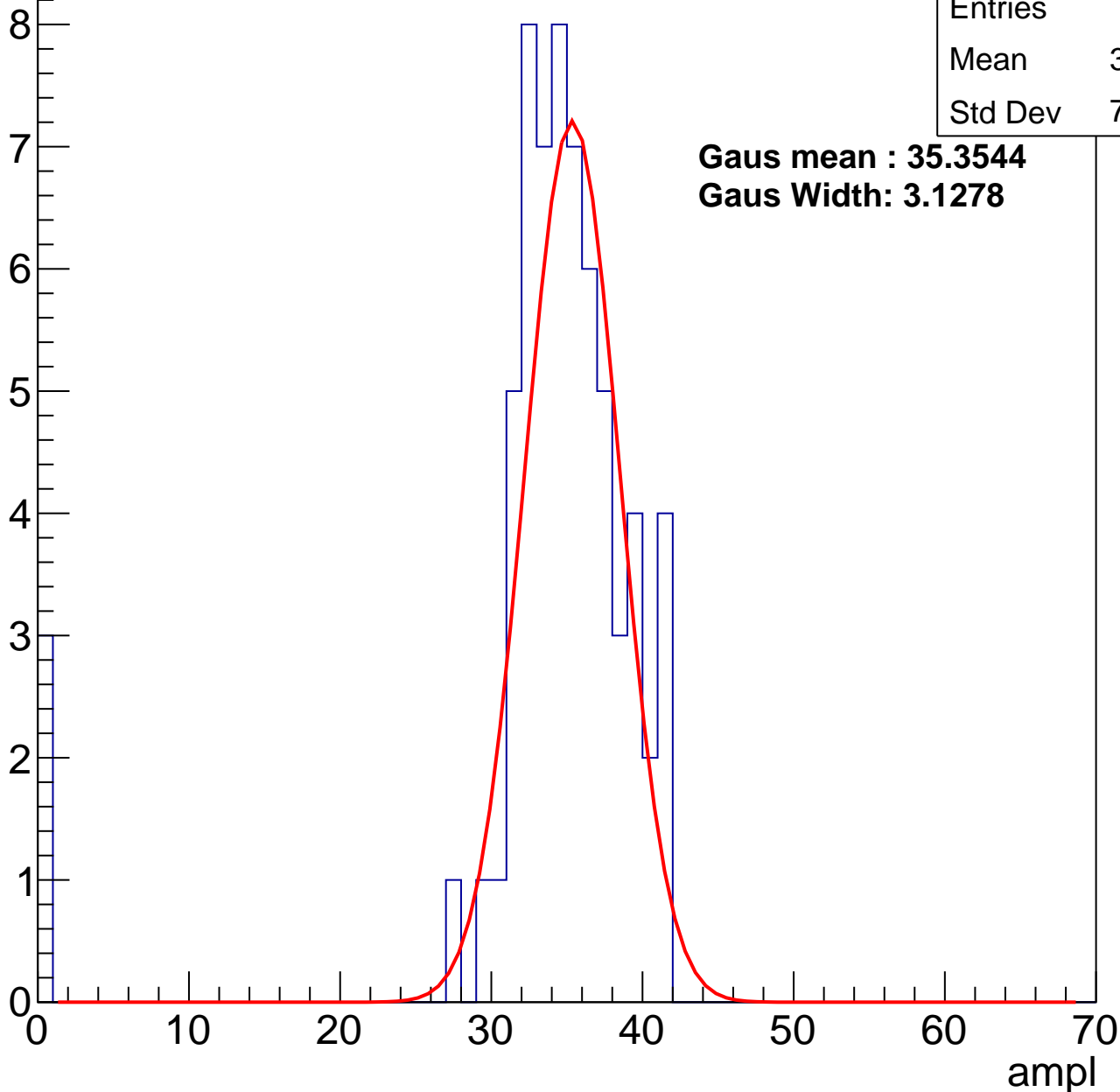
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	65
Mean	33.23
Std Dev	7.938

**Gaus mean : 35.3544**

**Gaus Width: 3.1278**



# B1L103S, U26-ch66, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	74
Mean	35.27
Std Dev	15.08

**Gaus mean : 41.8174**

**Gaus Width: 3.4770**

Entry

10

8

6

4

2

0

0

10

20

30

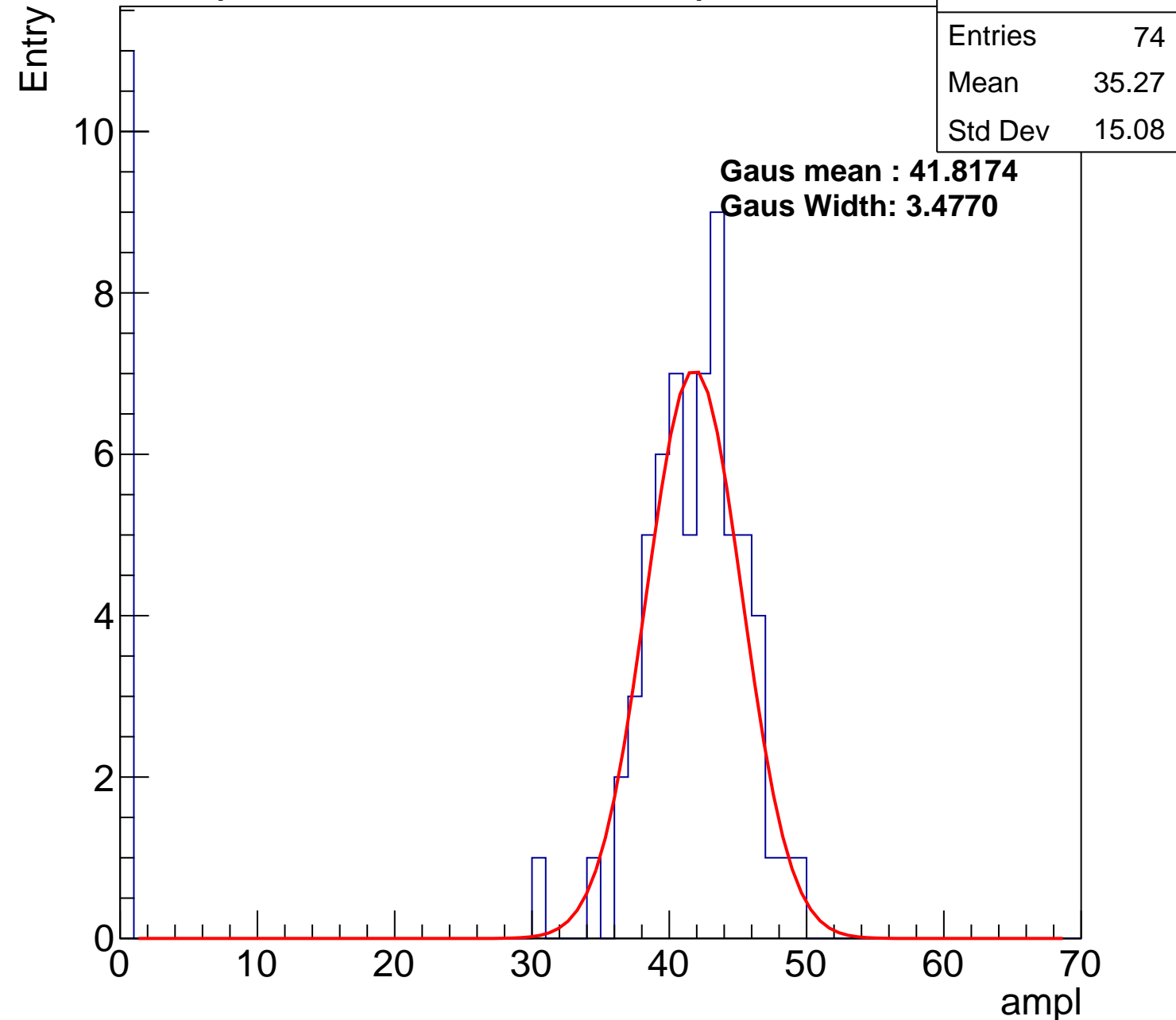
40

50

60

70

ampl

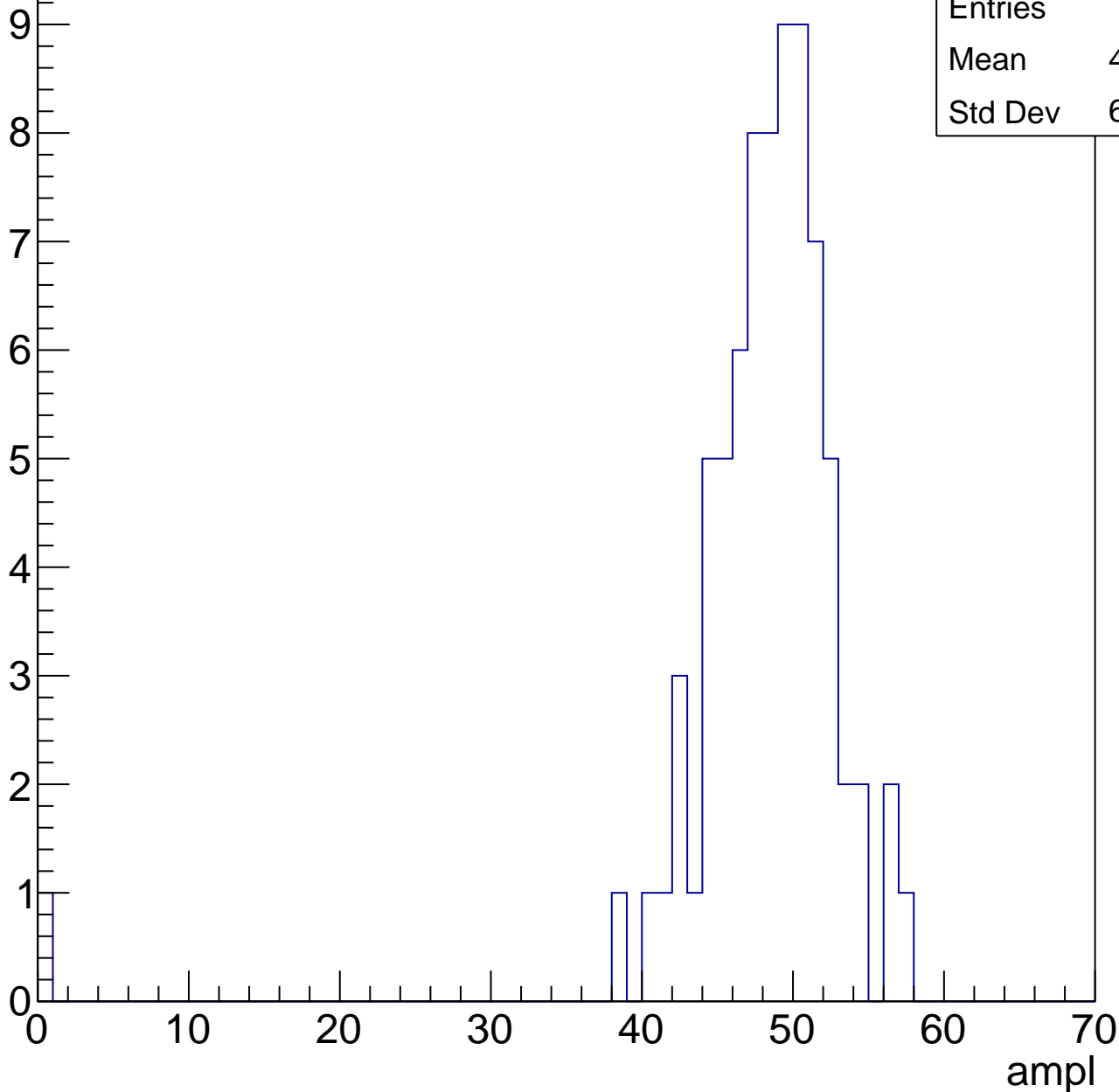


# B1L103S, U26-ch66, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	77
Mean	47.53
Std Dev	6.556

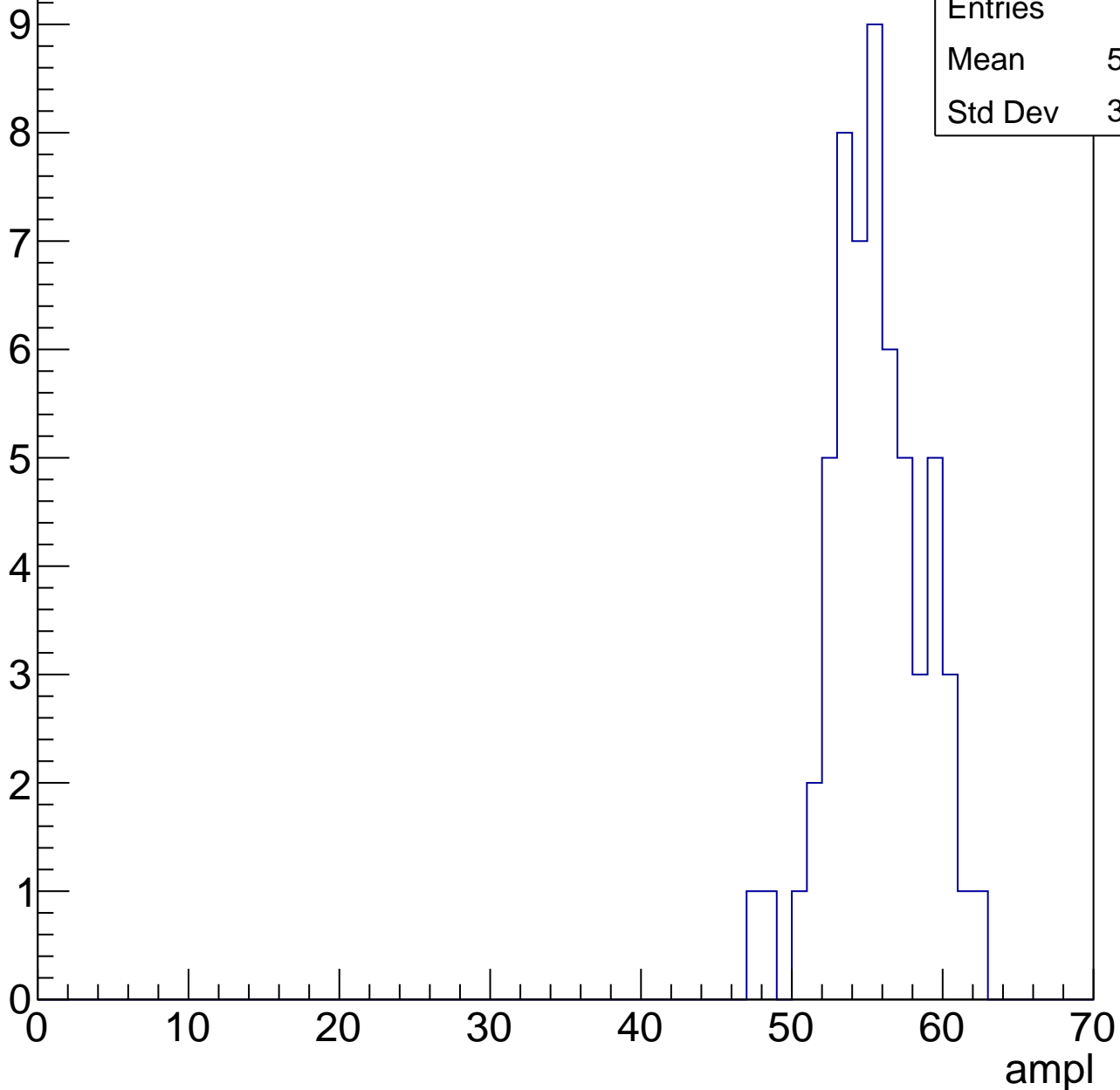


# B1L103S, U26-ch66, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	58
Mean	55.12
Std Dev	3.069

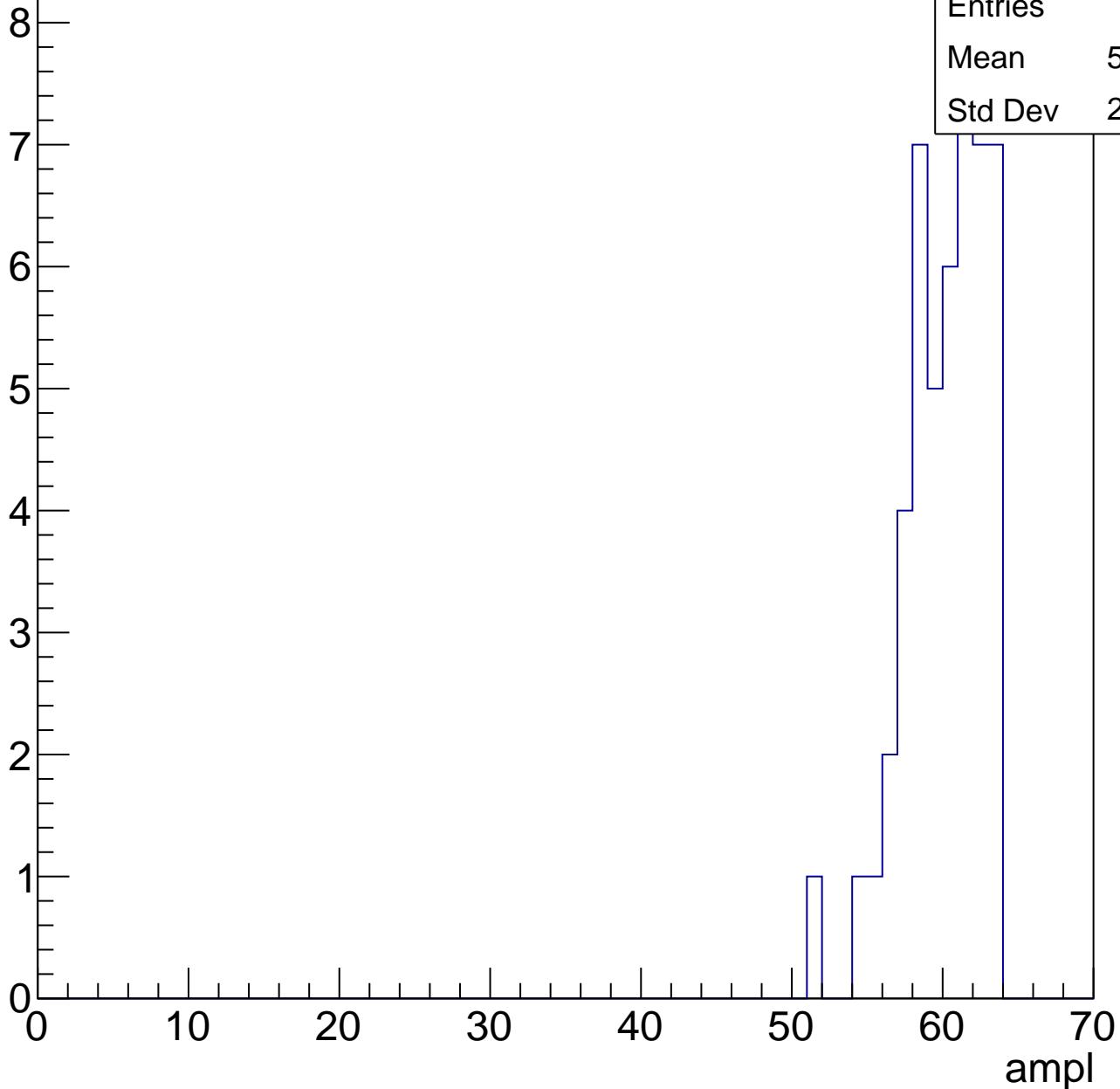


# B1L103S, U26-ch66, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	49
Mean	59.67
Std Dev	2.622



# B1L103S, U26-ch66, adc6

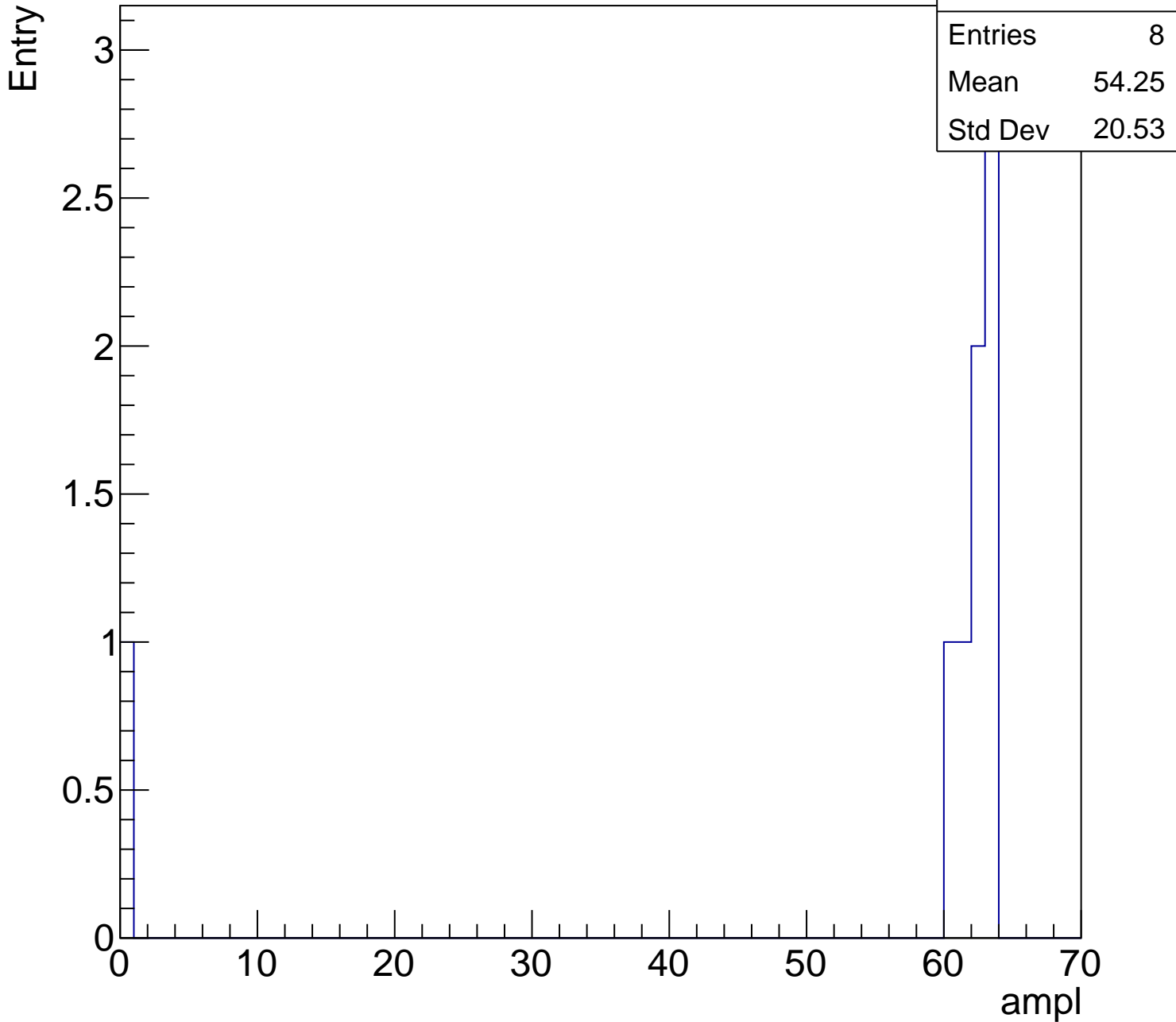
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

3  
2.5  
2  
1.5  
1  
0.5  
0

Entries	8
Mean	54.25
Std Dev	20.53

ampl





# B1L103S, U26-ch66, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

18  
16  
14  
12  
10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

Entries	19
Mean	0
Std Dev	0

# B1L103S, U26-ch67, adc0

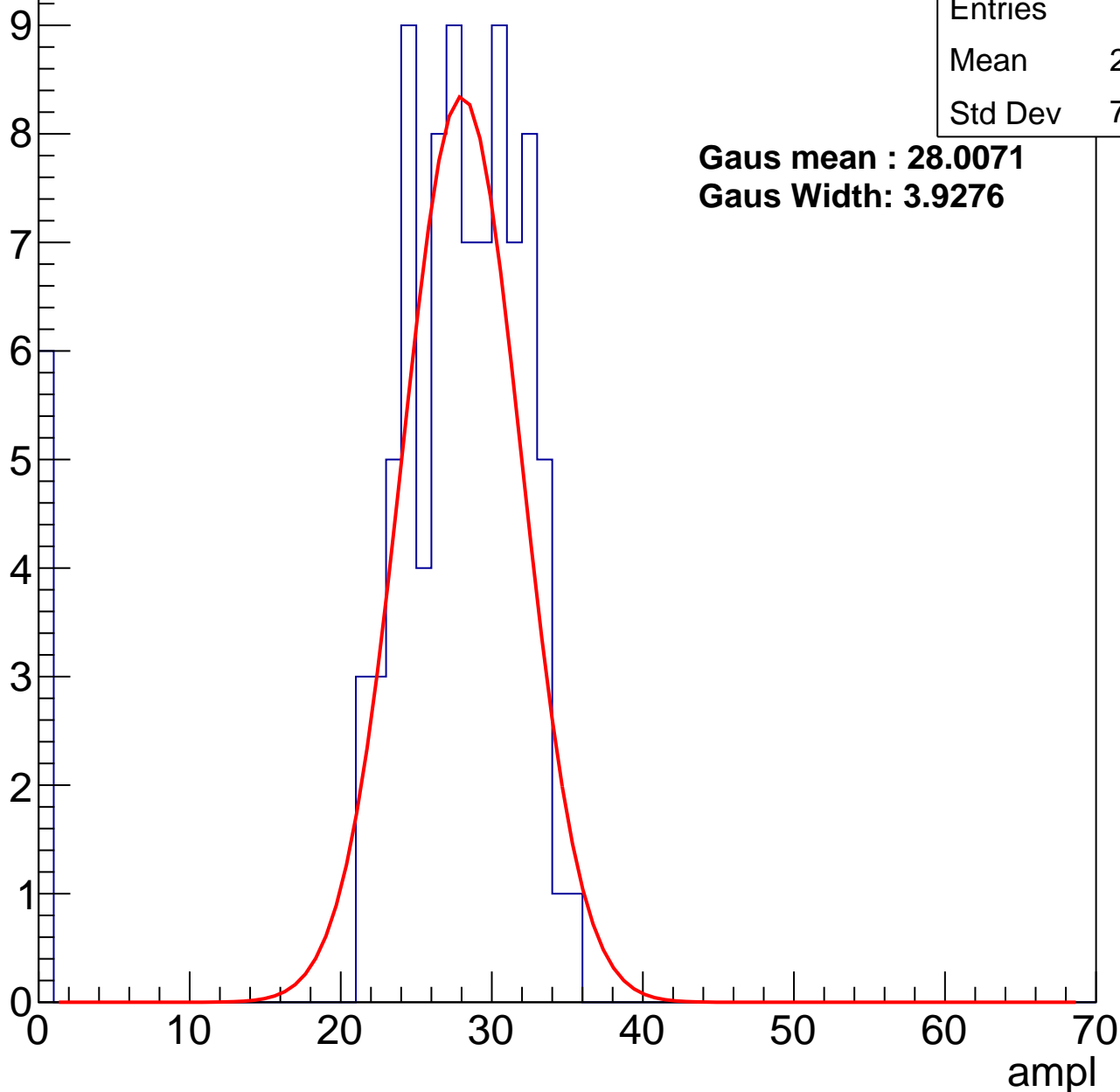
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	92
Mean	25.95
Std Dev	7.633

**Gaus mean : 28.0071**

**Gaus Width: 3.9276**



# B1L103S, U26-ch67, adc1

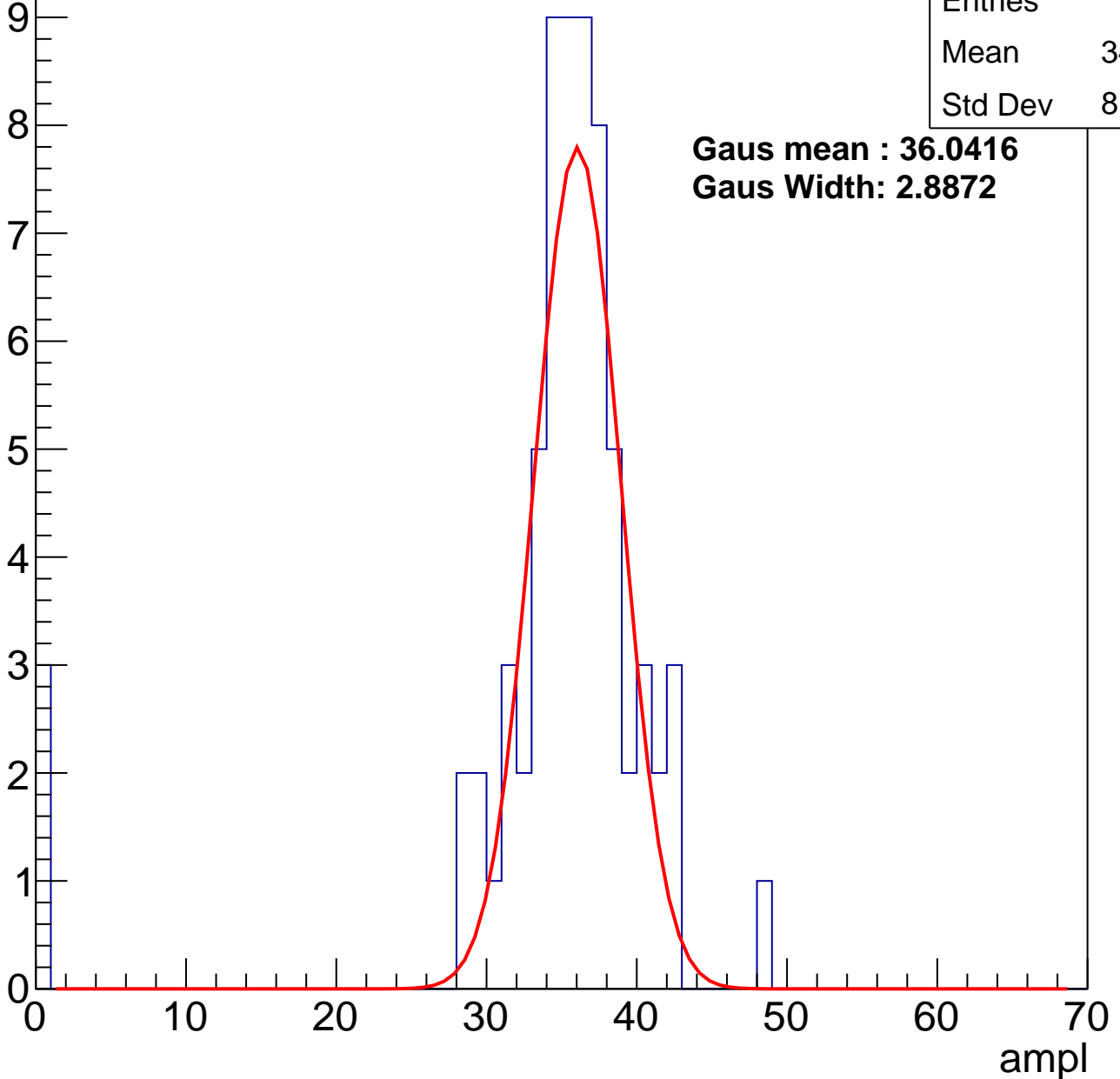
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	69
Mean	34.07
Std Dev	8.064

**Gaus mean : 36.0416**

**Gaus Width: 2.8872**



# B1L103S, U26-ch67, adc2

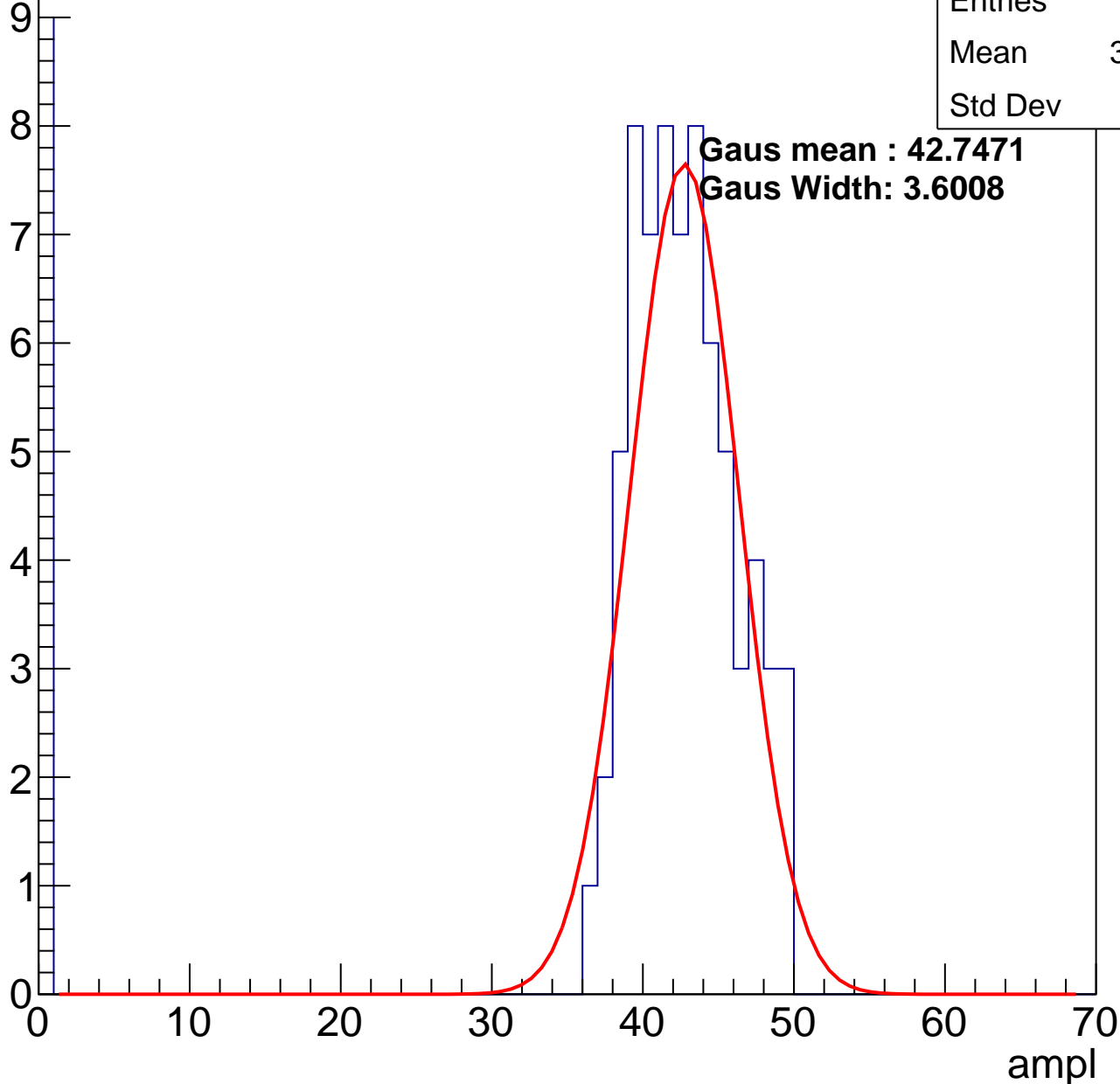
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	79
Mean	37.52
Std Dev	13.8

**Gaus mean : 42.7471**

**Gaus Width: 3.6008**

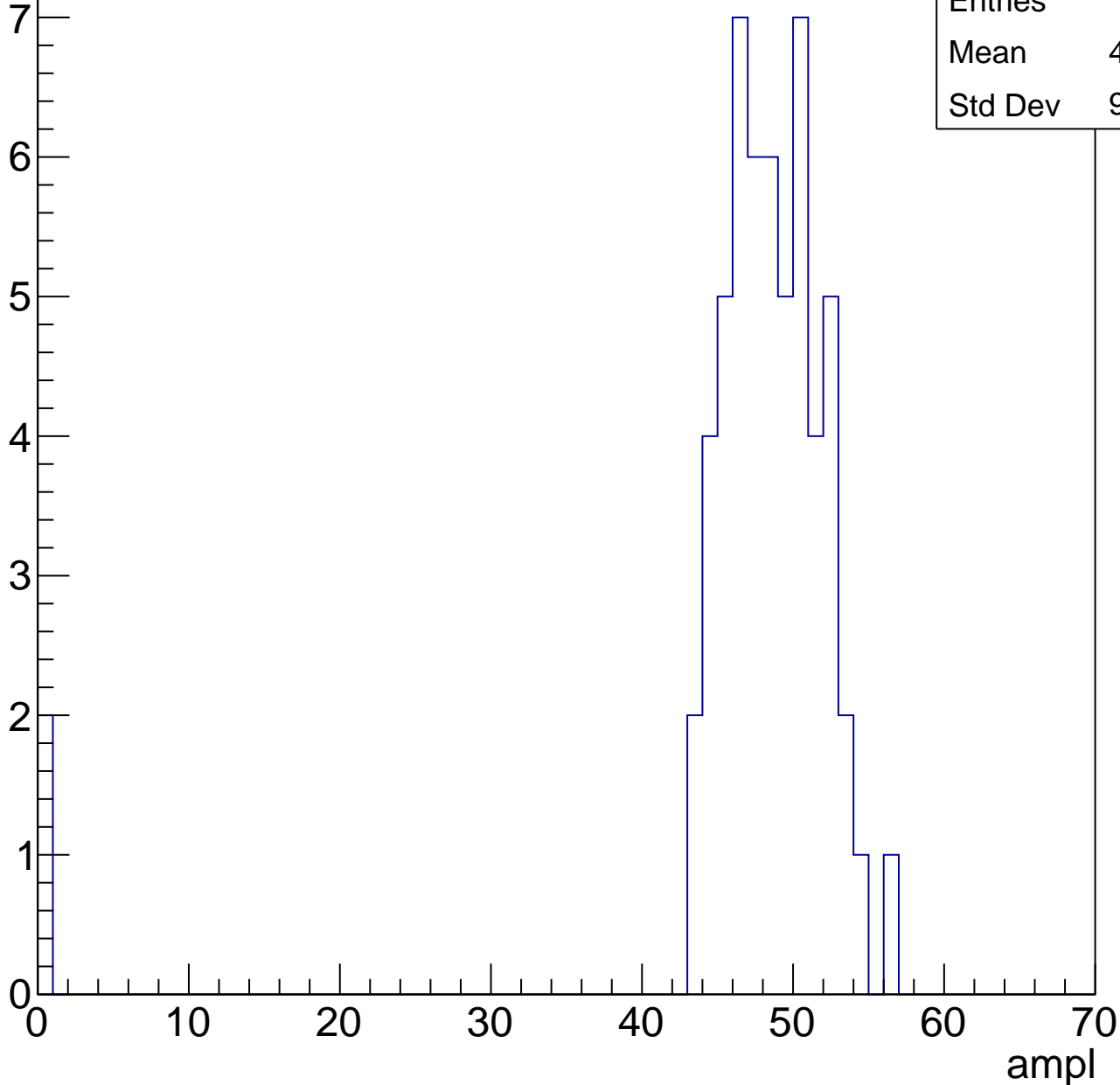


# B1L103S, U26-ch67, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

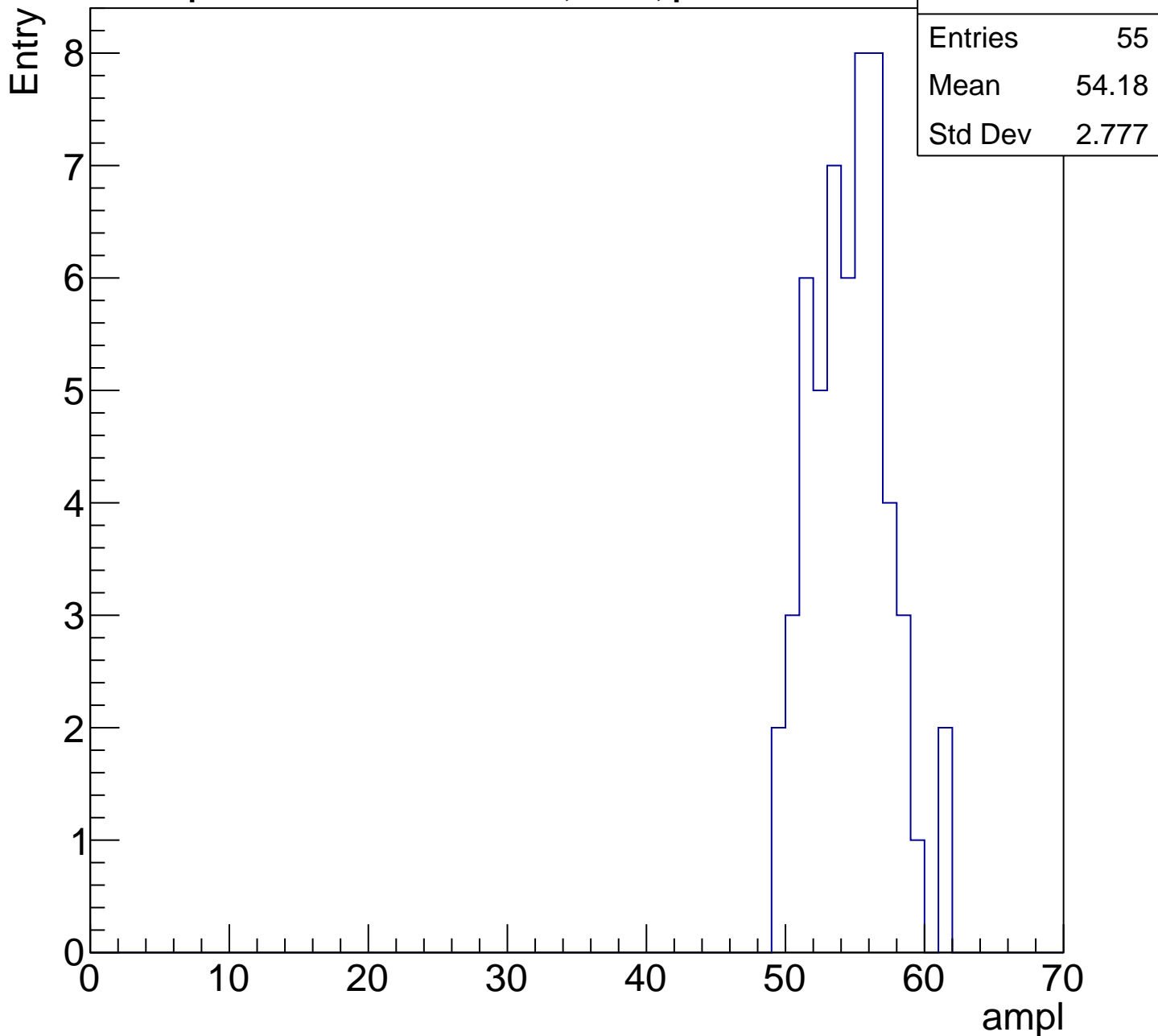
Entry

Entries	57
Mean	46.56
Std Dev	9.349



# B1L103S, U26-ch67, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

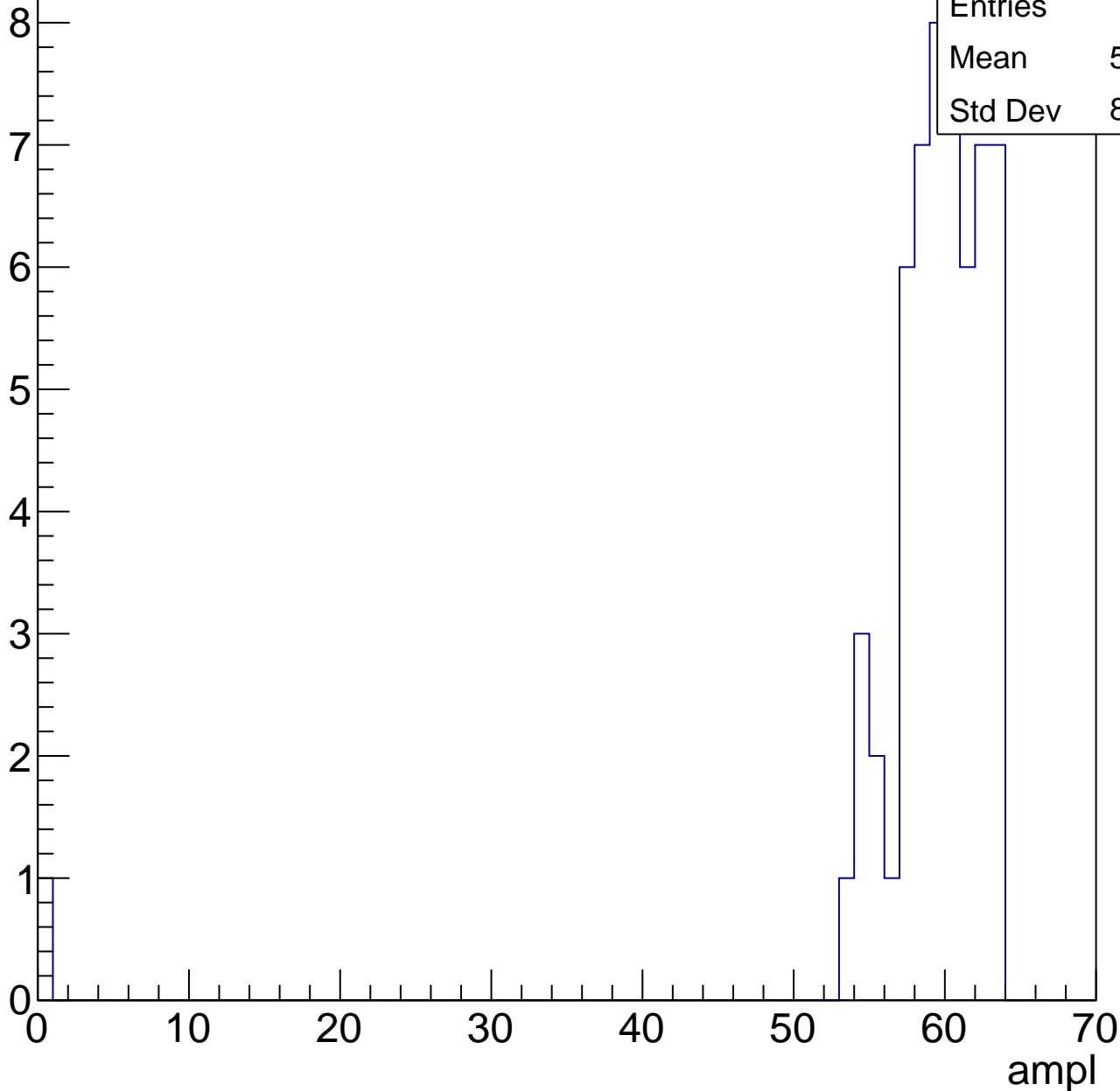


# B1L103S, U26-ch67, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	57
Mean	58.28
Std Dev	8.209



# B1L103S, U26-ch67, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

3

2.5

2

1.5

1

0.5

0

0

10

20

30

40

50

60

70

ampl

Entries	11
Mean	61.45
Std Dev	1.305

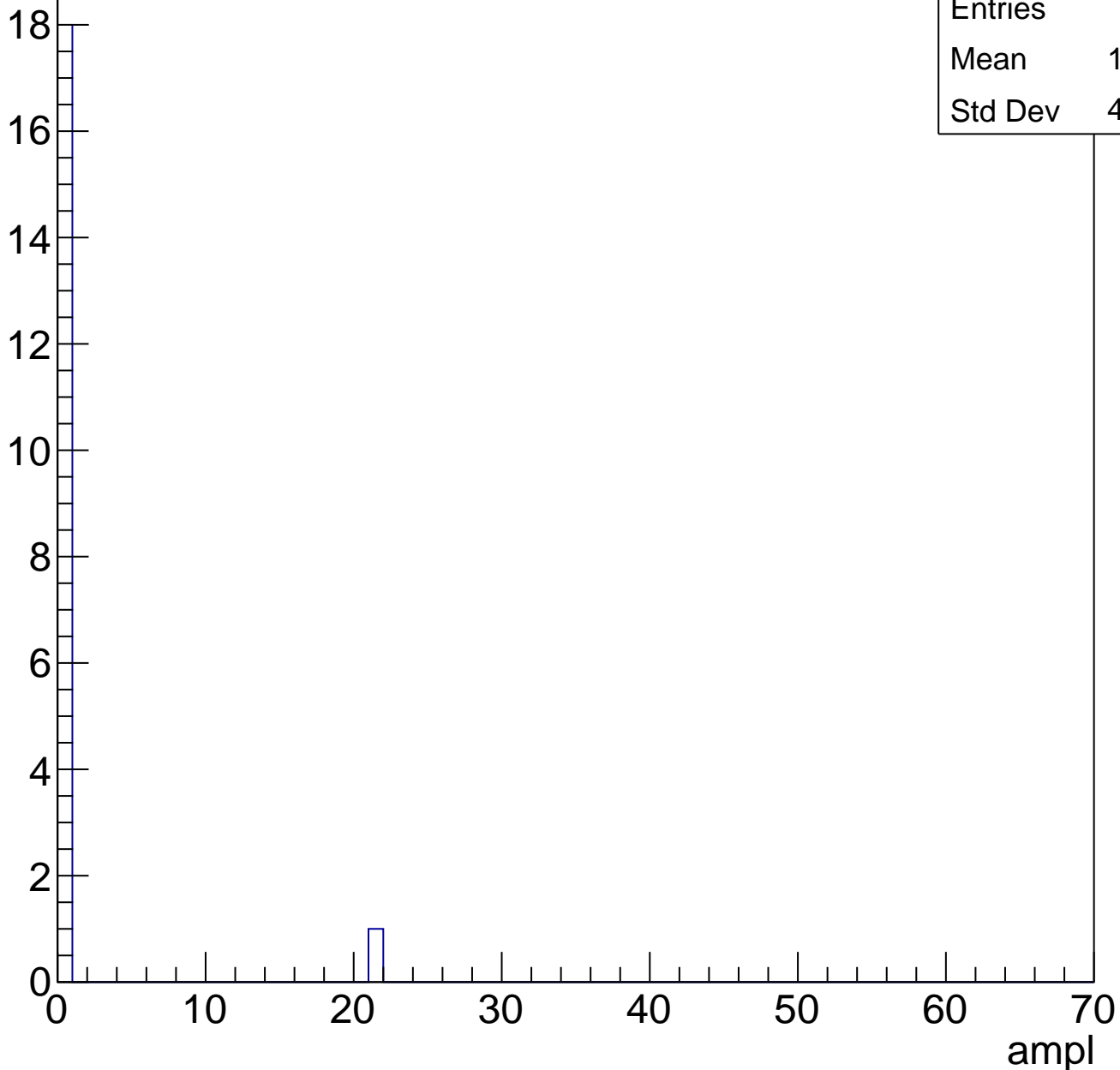


# B1L103S, U26-ch67, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	19
Mean	1.105
Std Dev	4.689

Entry



# B1L103S, U26-ch68, adc0

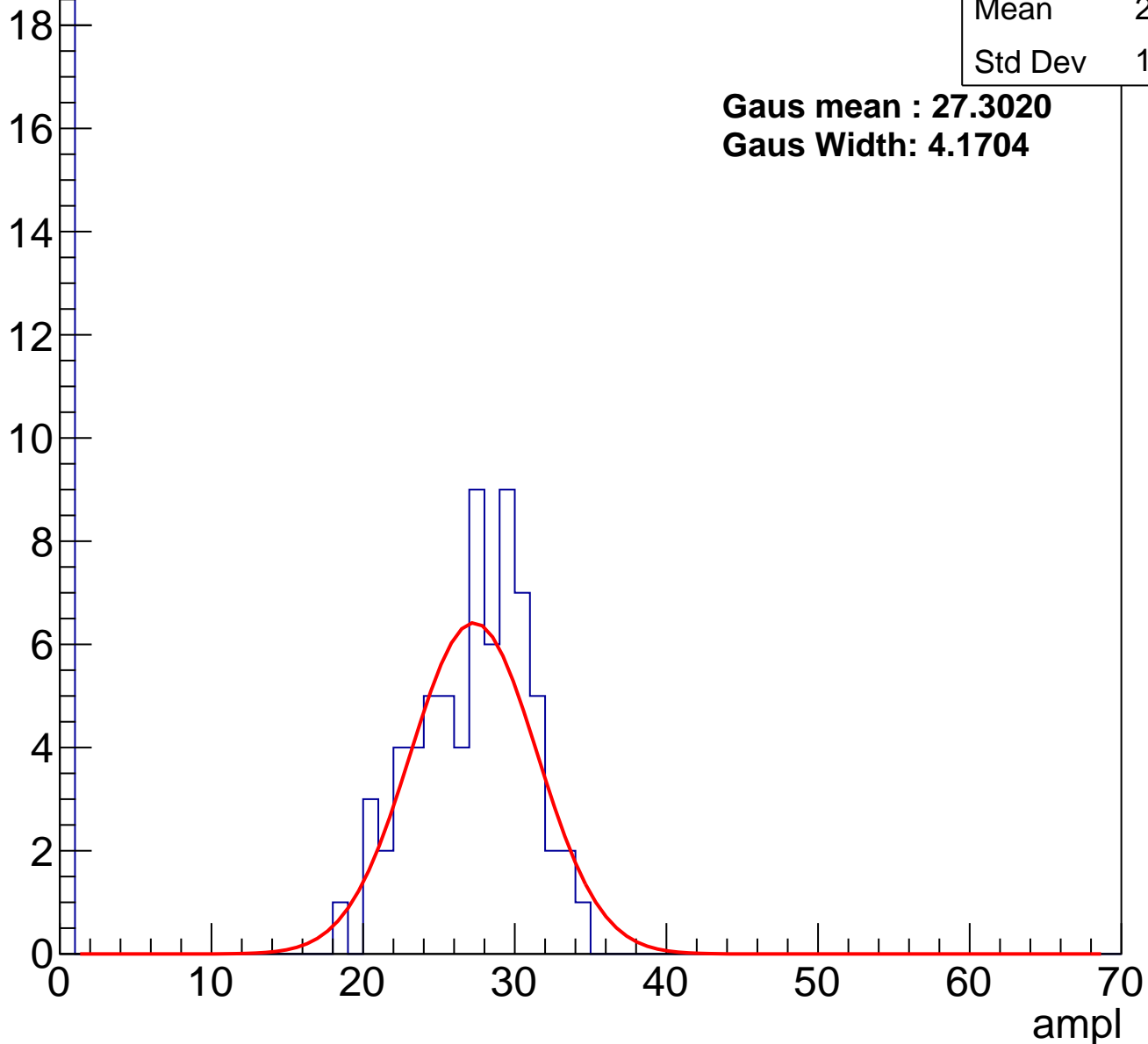
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	88
Mean	21.02
Std Dev	11.48

**Gaus mean : 27.3020**

**Gaus Width: 4.1704**

Entry



# B1L103S, U26-ch68, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	77
Mean	29.35
Std Dev	12.44

**Gaus mean : 35.9013**

**Gaus Width: 4.3920**

Entry

10

8

6

4

2

0

0

10

20

30

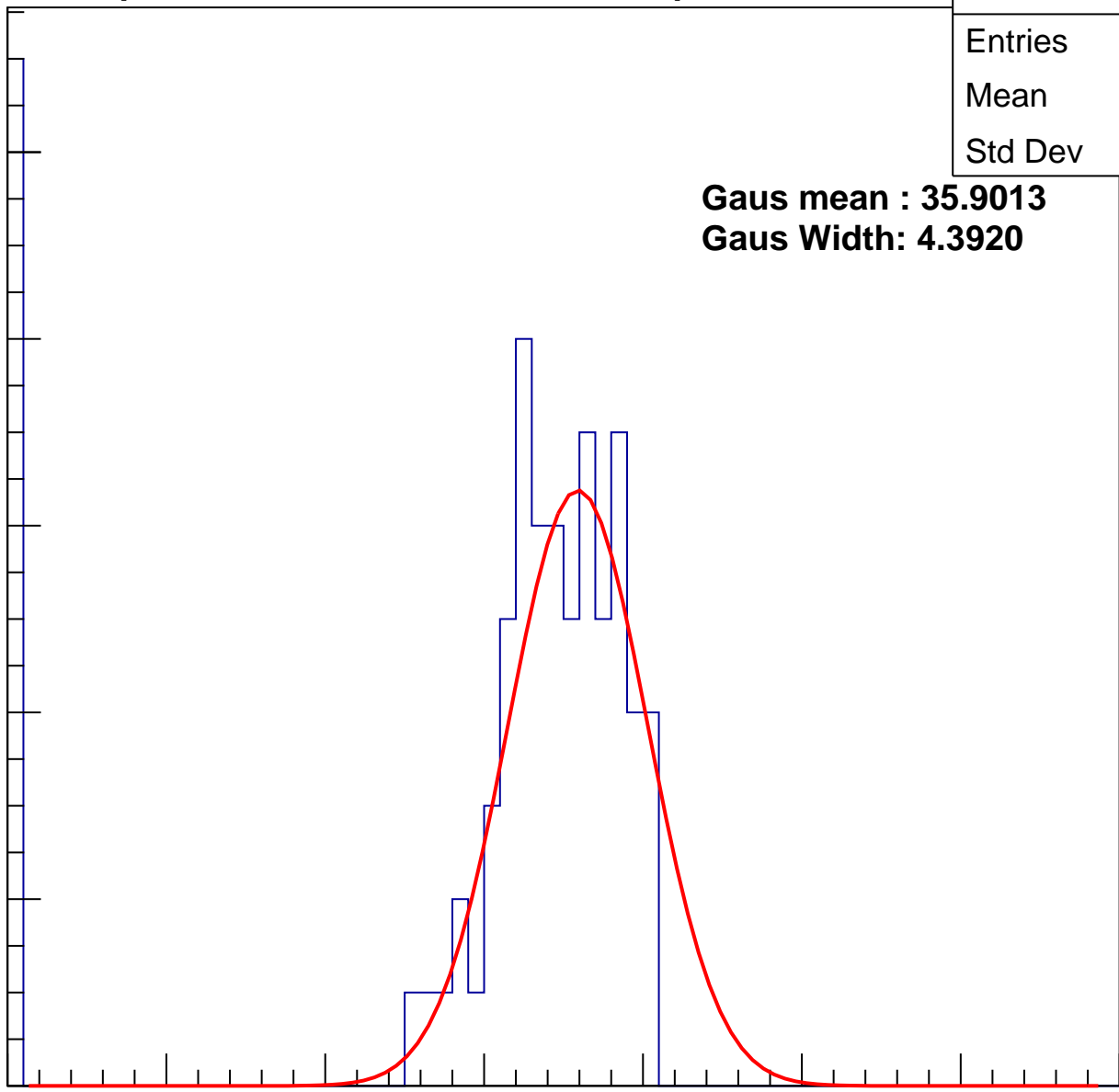
40

50

60

70

ampl



# B1L103S, U26-ch68, adc2

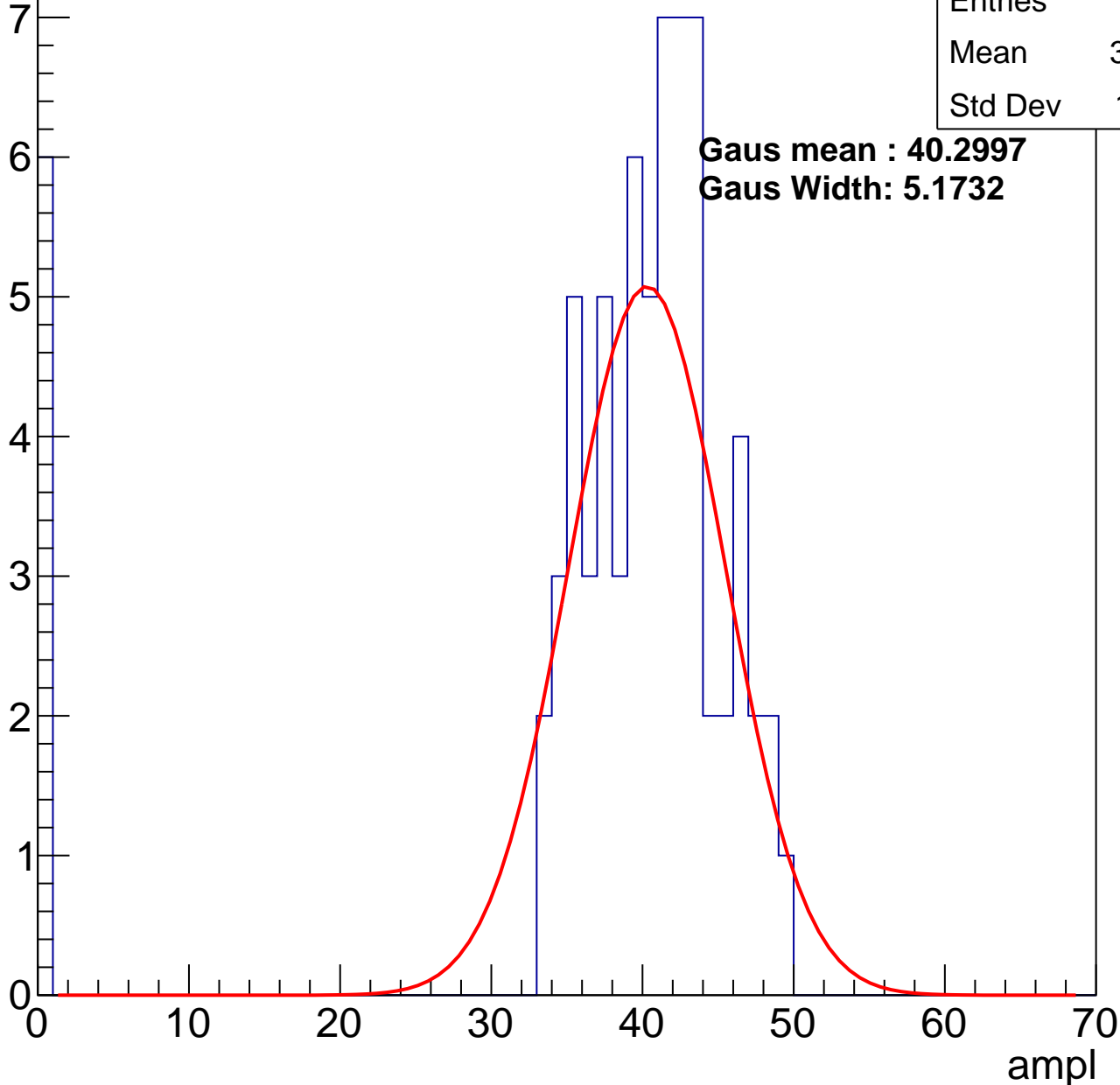
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	72
Mean	37.04
Std Dev	11.81

**Gaus mean : 40.2997**

**Gaus Width: 5.1732**

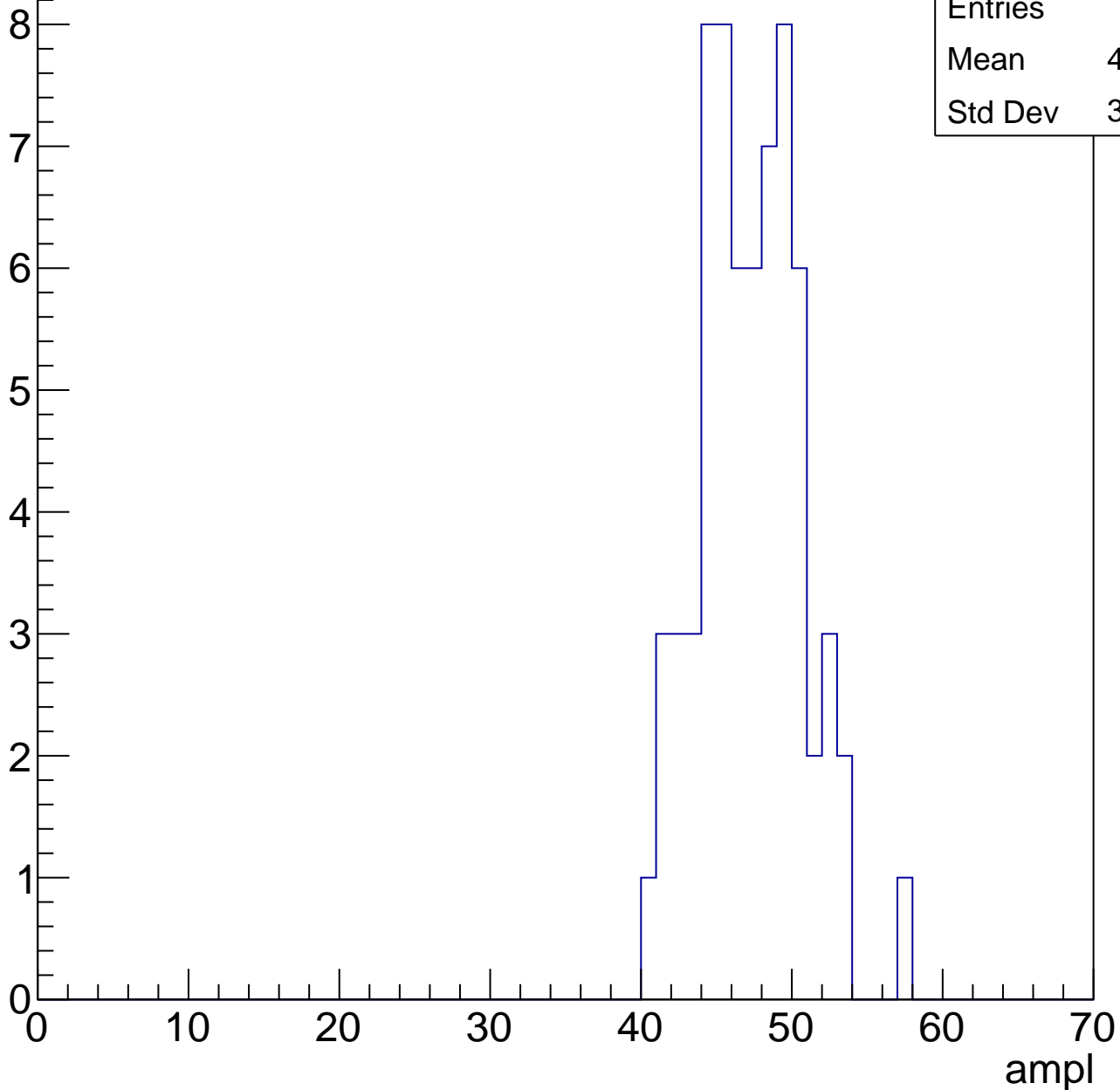


# B1L103S, U26-ch68, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

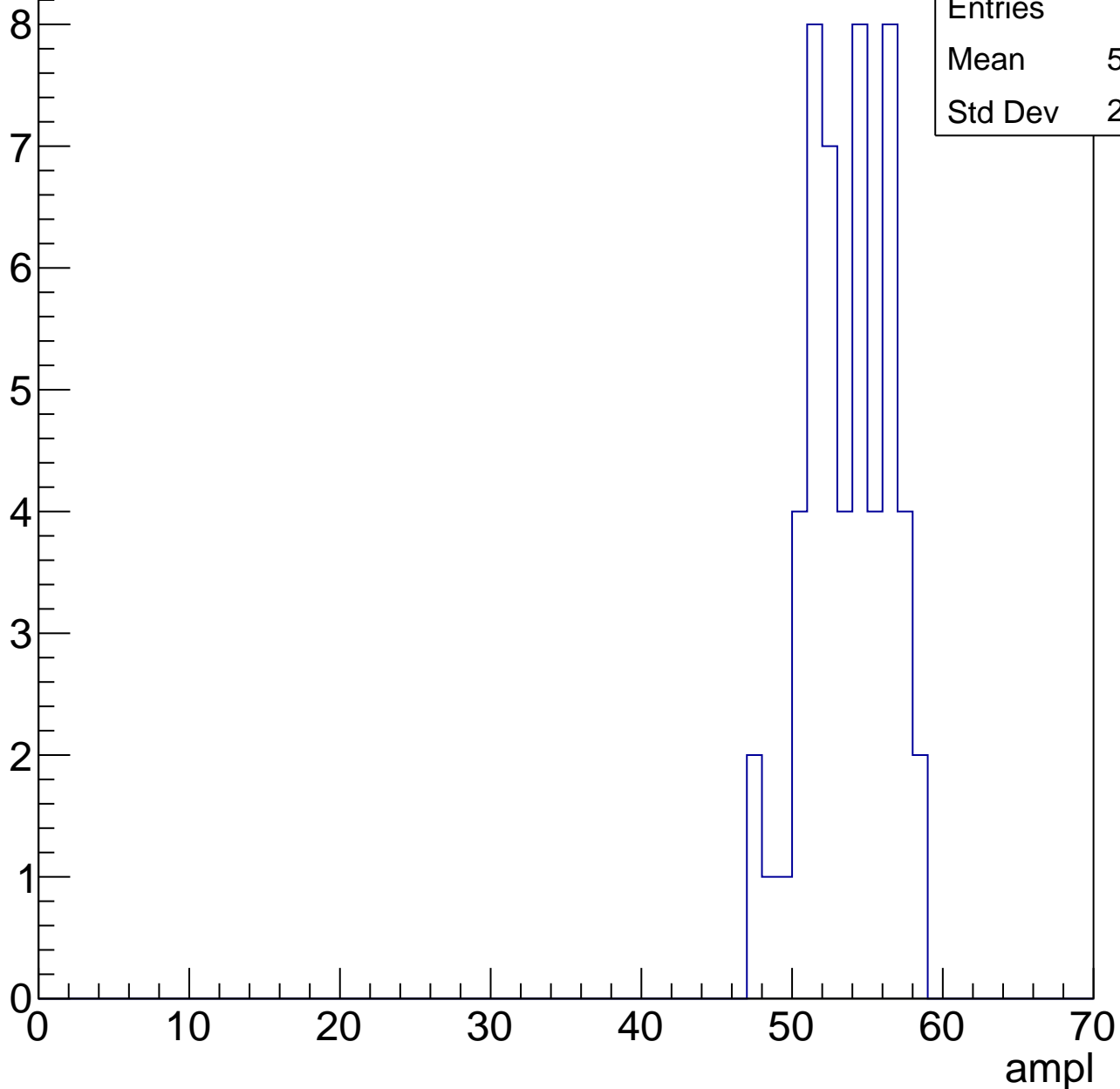
Entries	67
Mean	46.82
Std Dev	3.368



# B1L103S, U26-ch68, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



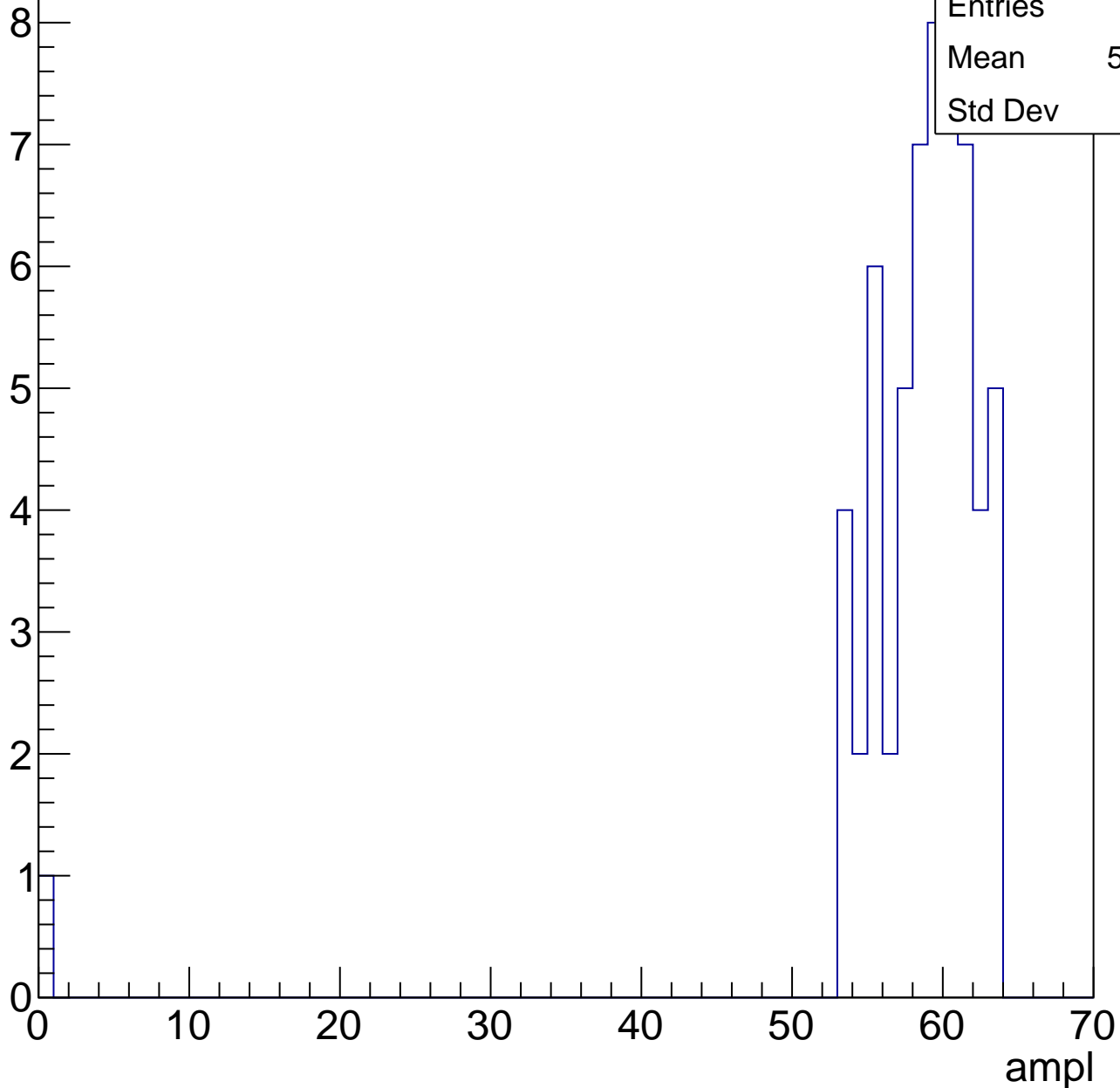
Entries	53
Mean	53.19
Std Dev	2.734

# B1L103S, U26-ch68, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	59
Mean	57.54
Std Dev	8.07

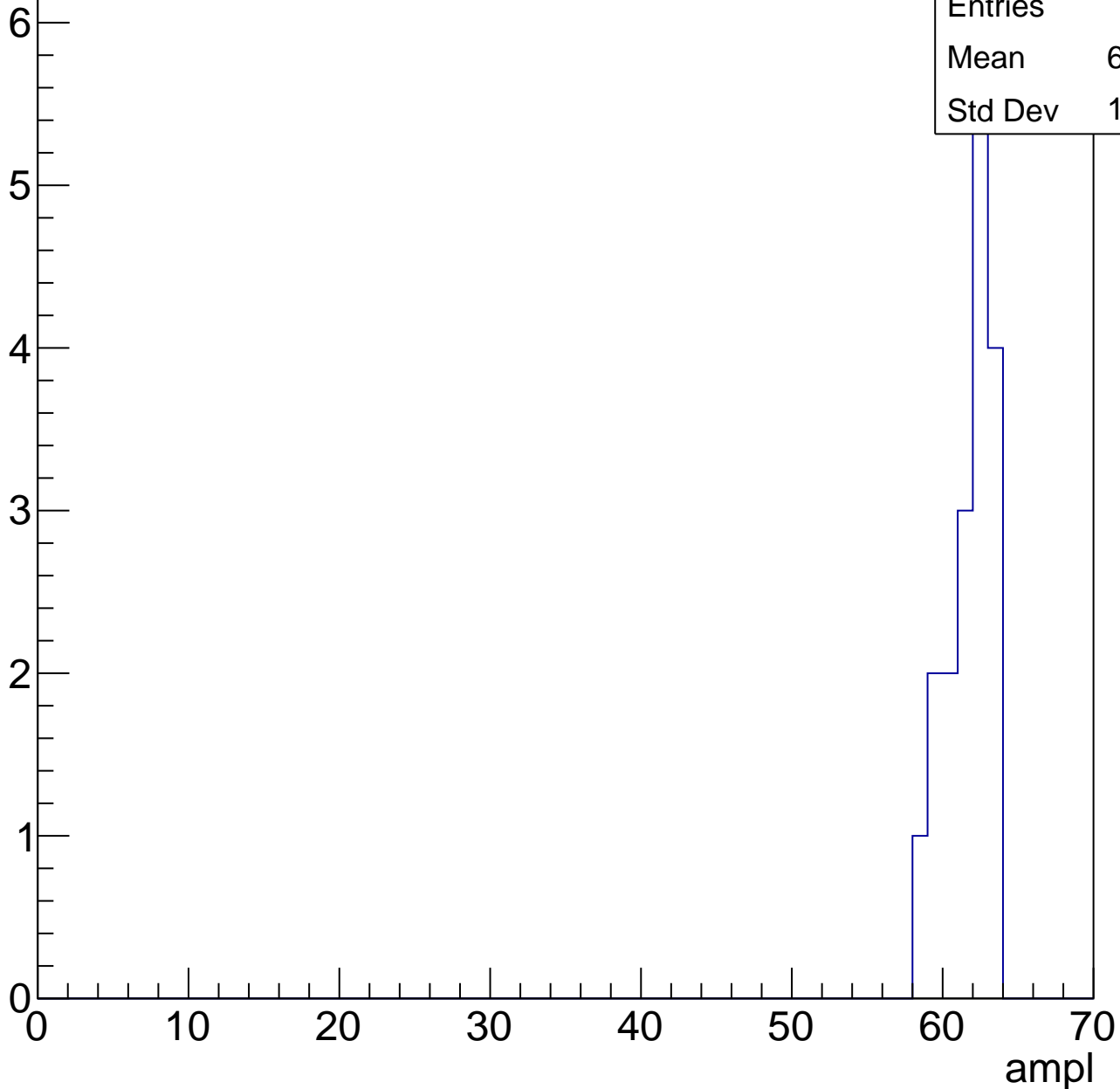


# B1L103S, U26-ch68, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	18
Mean	61.28
Std Dev	1.483





# B1L103S, U26-ch68, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	20
Mean	3.15
Std Dev	13.73

Entry



# B1L103S, U26-ch69, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	89
Mean	25.45
Std Dev	10.08

**Gaus mean : 29.3877**

**Gaus Width: 3.5642**

Entry

10

8

6

4

2

0

0

10

20

30

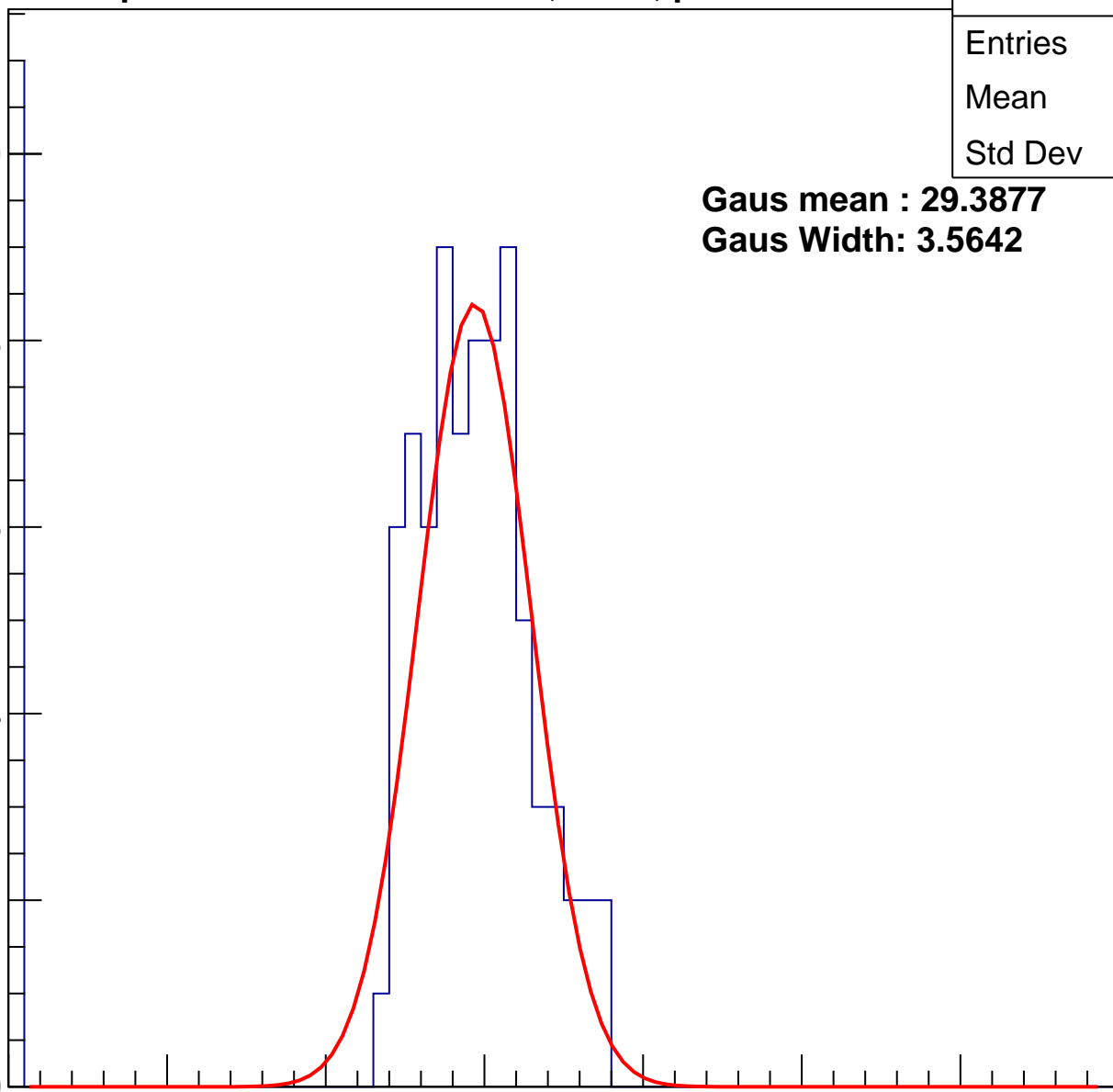
40

50

60

70

ampl



# B1L103S, U26-ch69, adc1

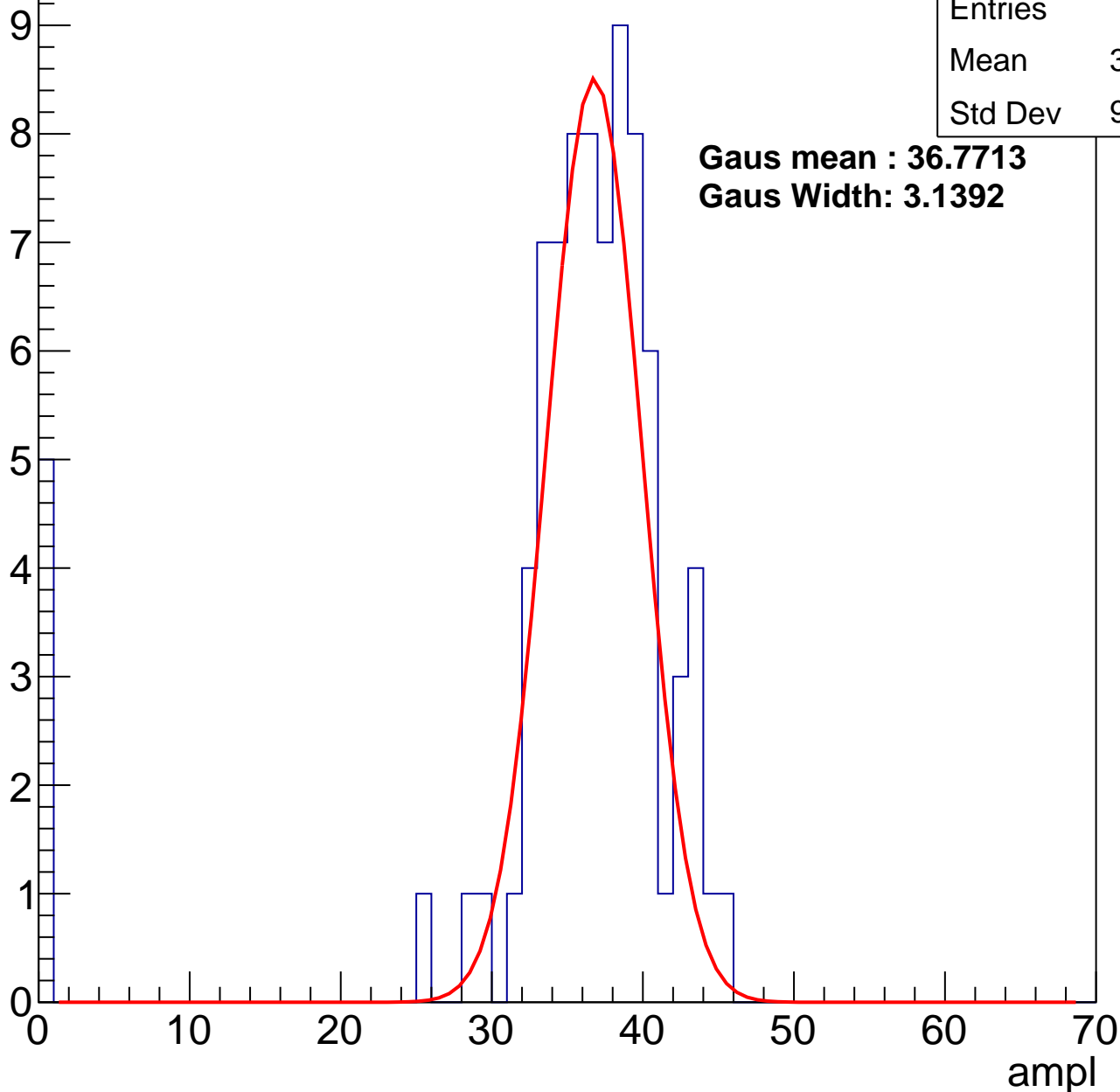
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	83
Mean	34.45
Std Dev	9.434

**Gaus mean : 36.7713**

**Gaus Width: 3.1392**



# B1L103S, U26-ch69, adc2

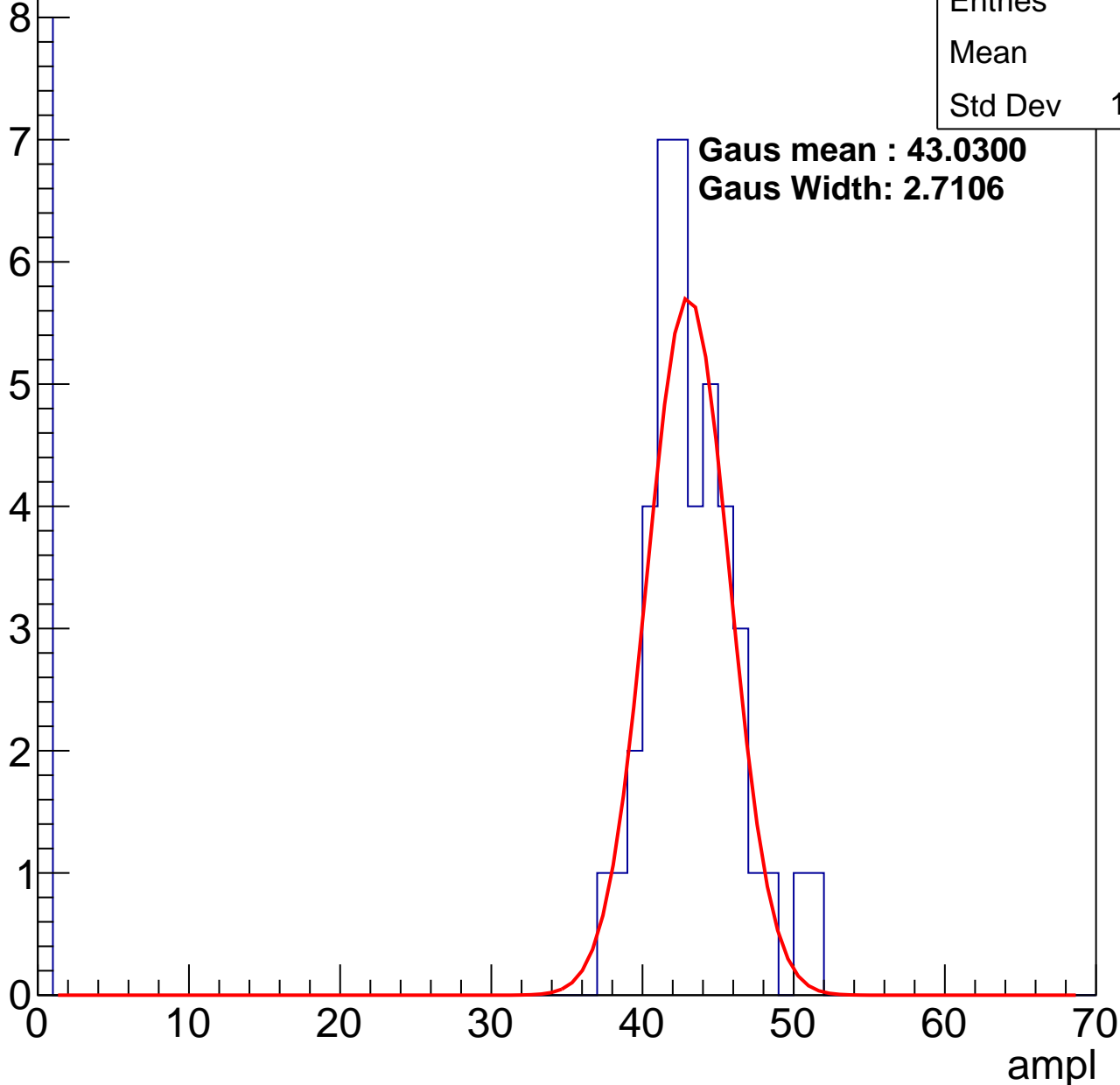
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	50
Mean	36
Std Dev	15.94

**Gaus mean : 43.0300**

**Gaus Width: 2.7106**

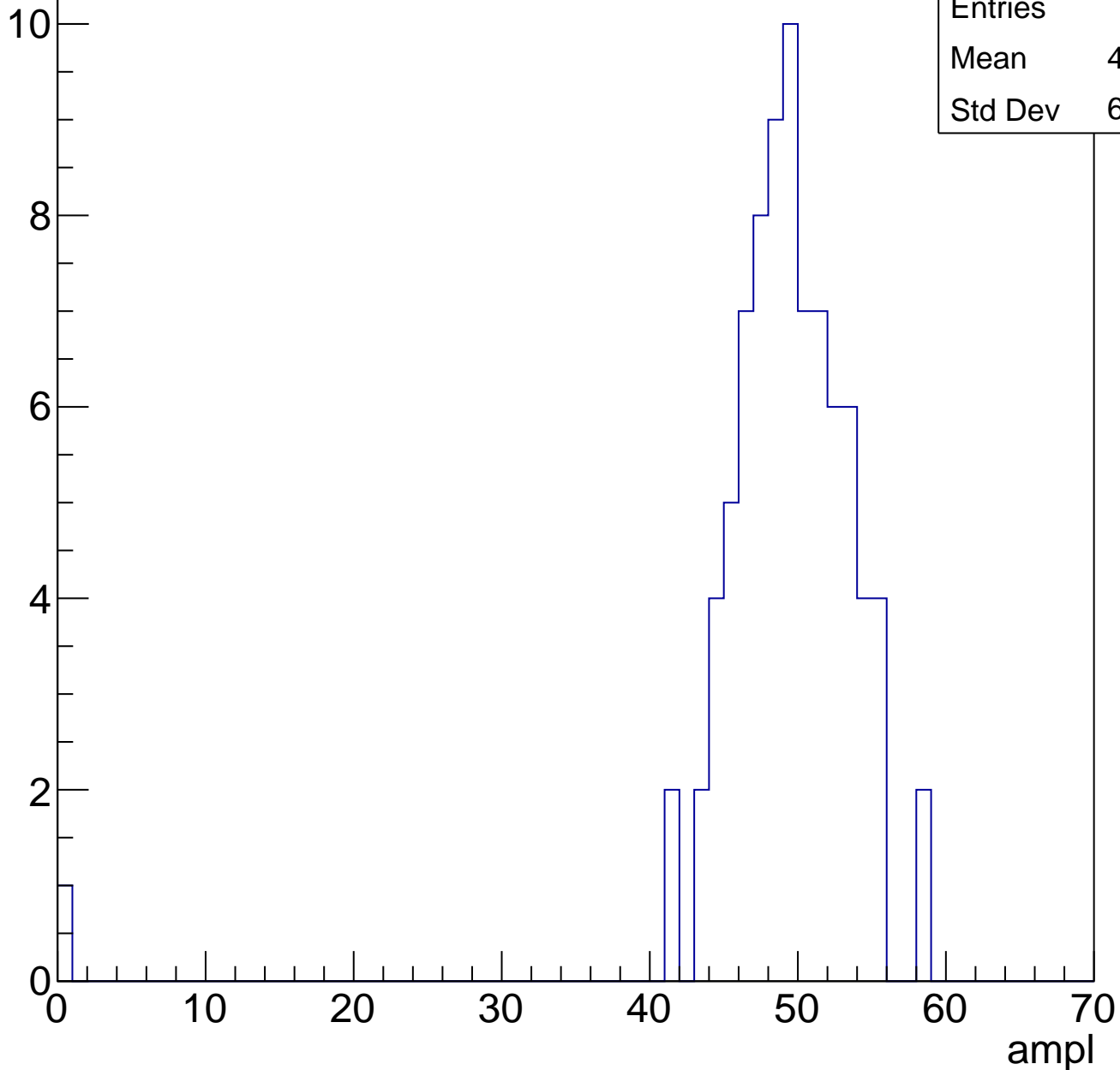


# B1L103S, U26-ch69, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	84
Mean	48.55
Std Dev	6.417

Entry

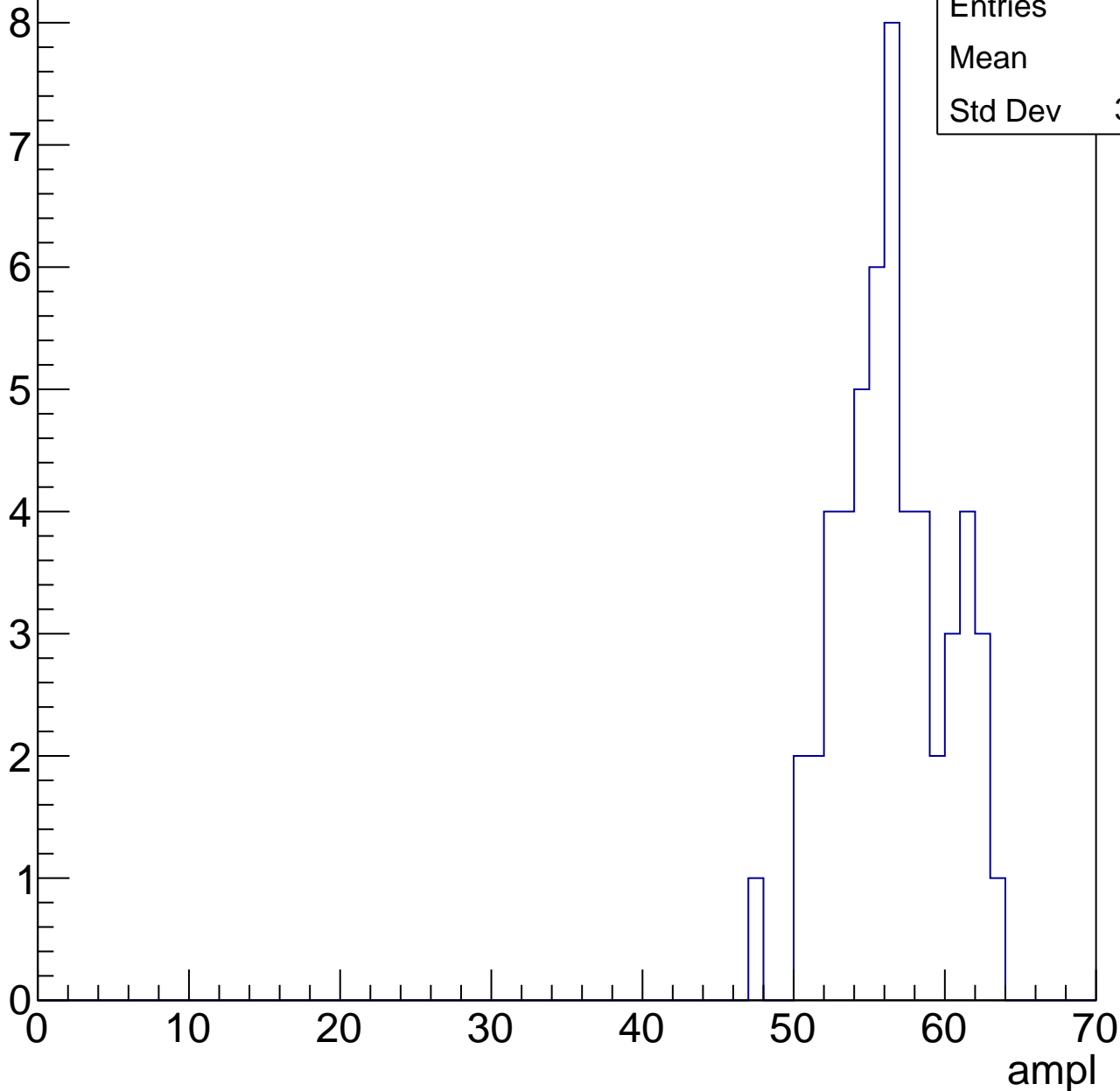


# B1L103S, U26-ch69, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	53
Mean	56
Std Dev	3.561

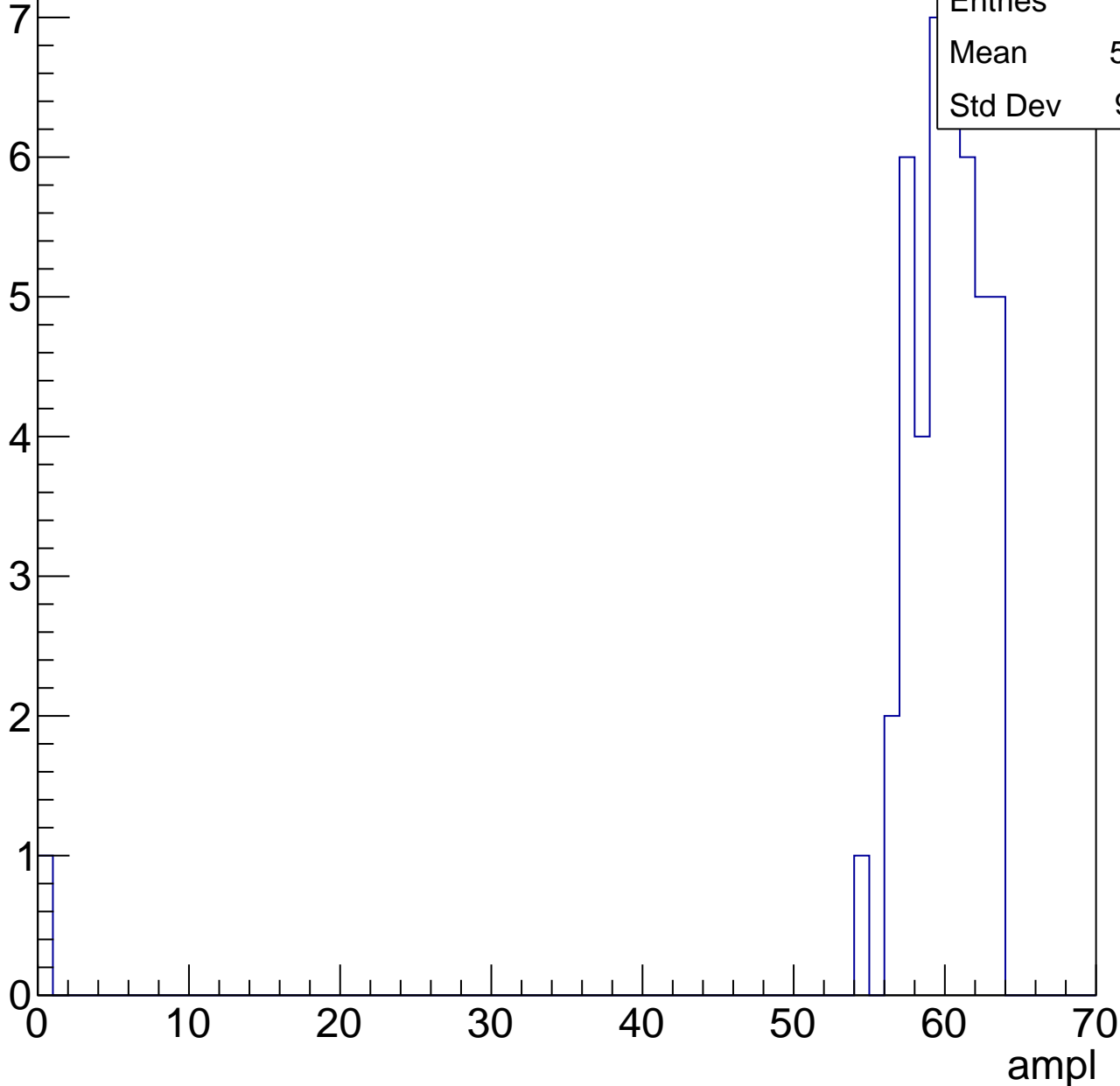


# B1L103S, U26-ch69, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

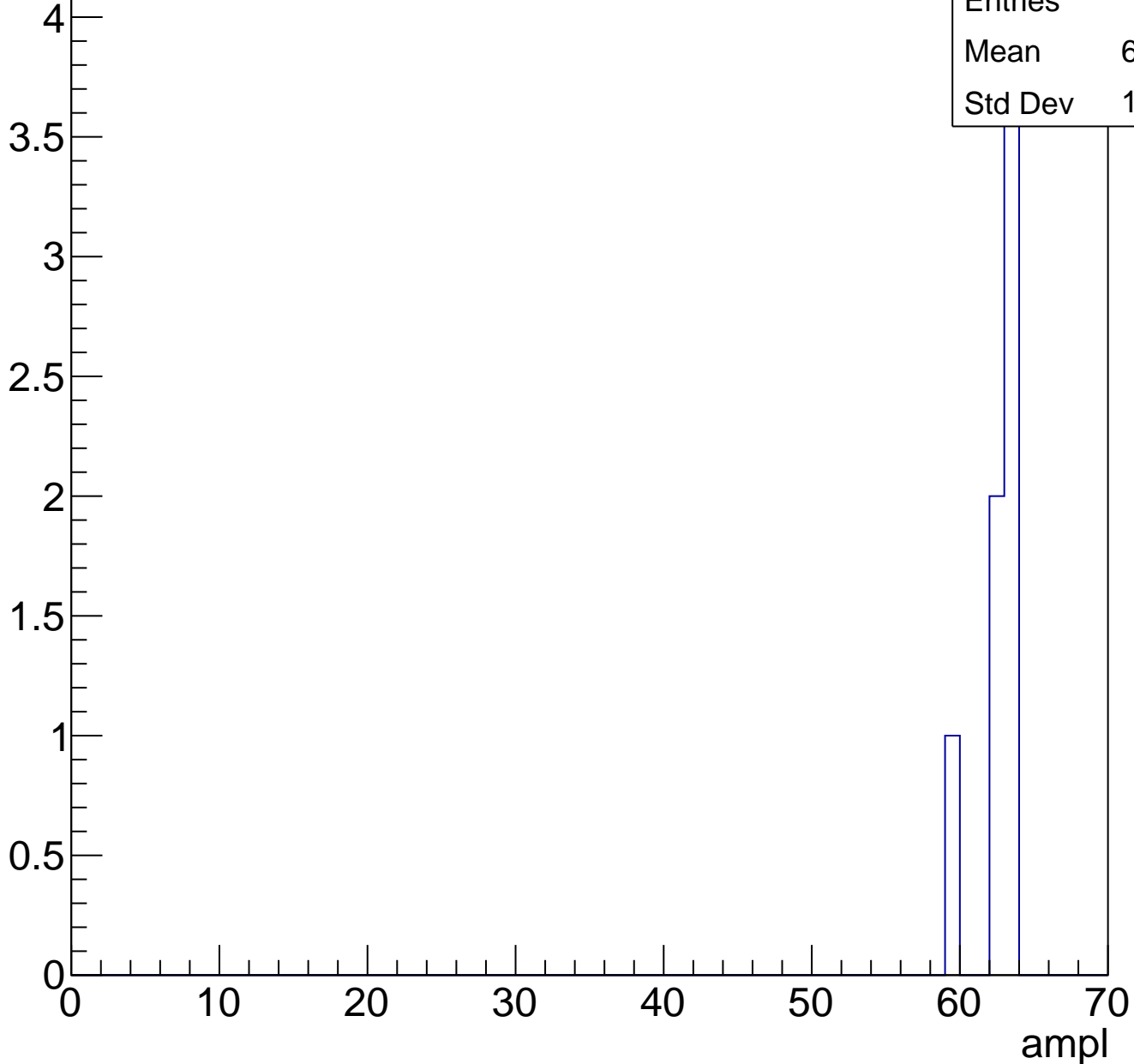
Entries	44
Mean	58.27
Std Dev	9.151



# B1L103S, U26-ch69, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry





# B1L103S, U26-ch69, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	19
Mean	1.211
Std Dev	5.136

Entry



# B1L103S, U26-ch70, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	67
Mean	23.01
Std Dev	10.14

**Gaus mean : 27.2737**

**Gaus Width: 3.1524**

Entry

10

8

6

4

2

0

0

10

20

30

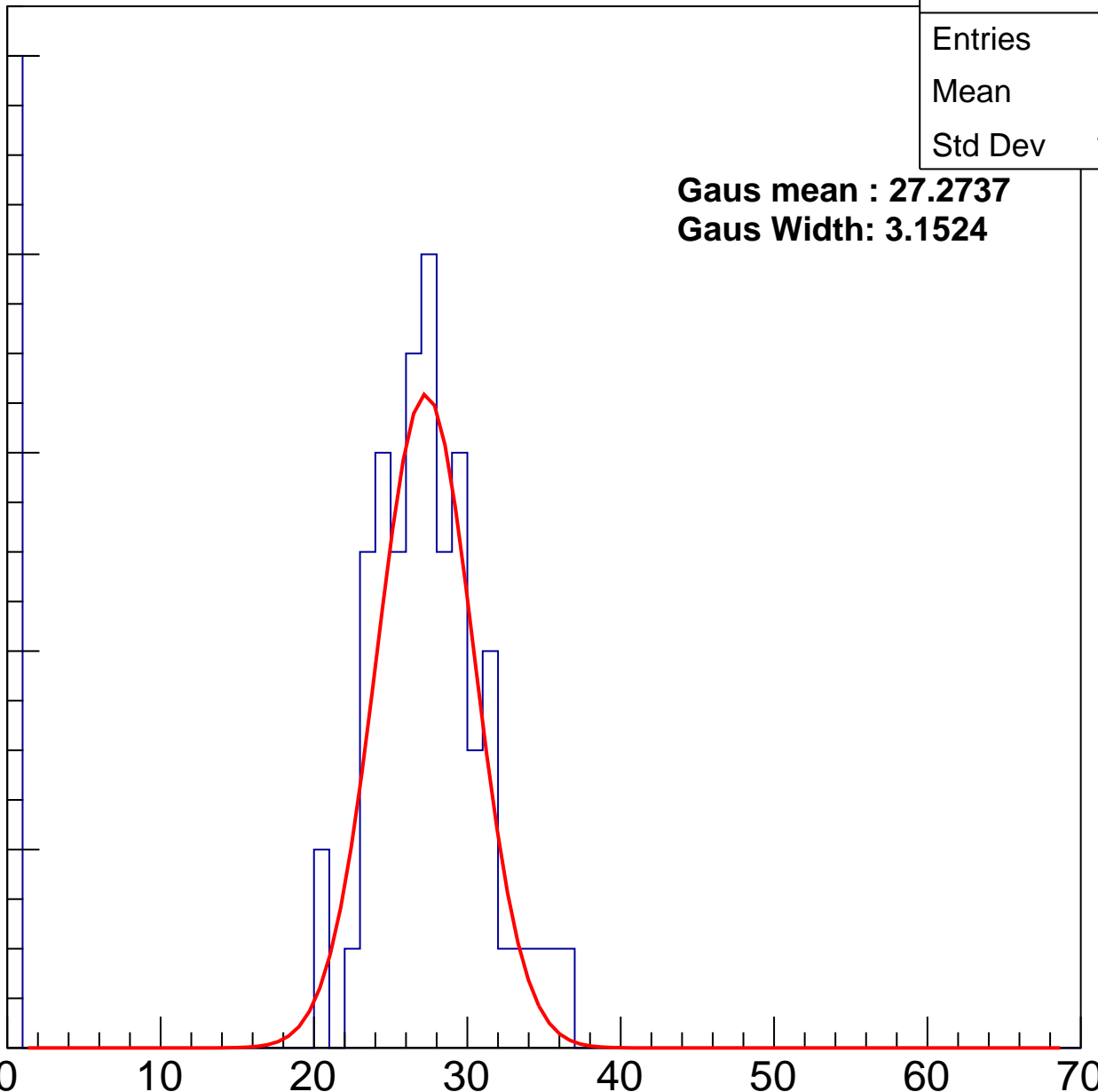
40

50

60

70

ampl



# B1L103S, U26-ch70, adc1

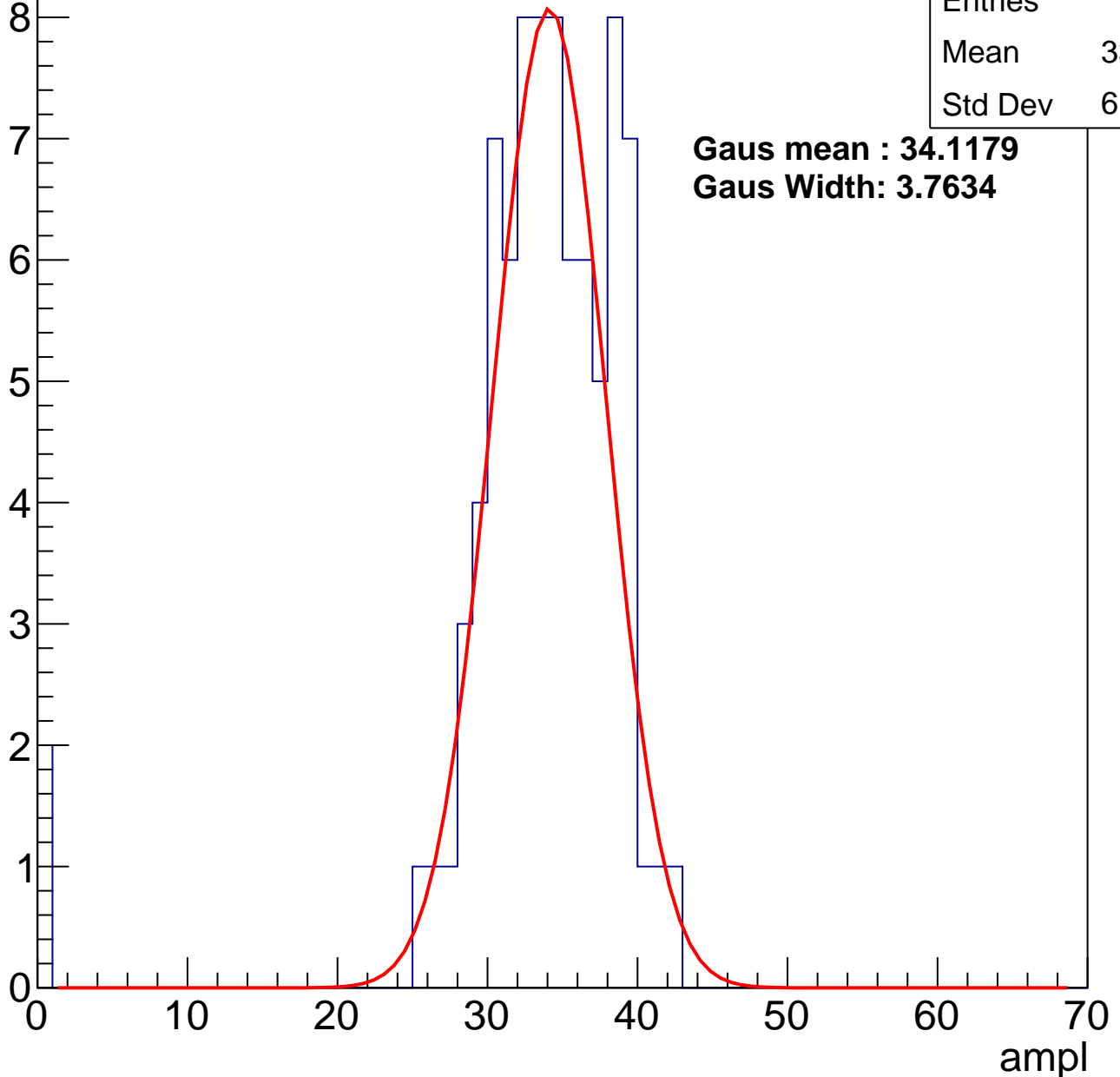
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	84
Mean	33.06
Std Dev	6.336

**Gaus mean : 34.1179**

**Gaus Width: 3.7634**



# B1L103S, U26-ch70, adc2

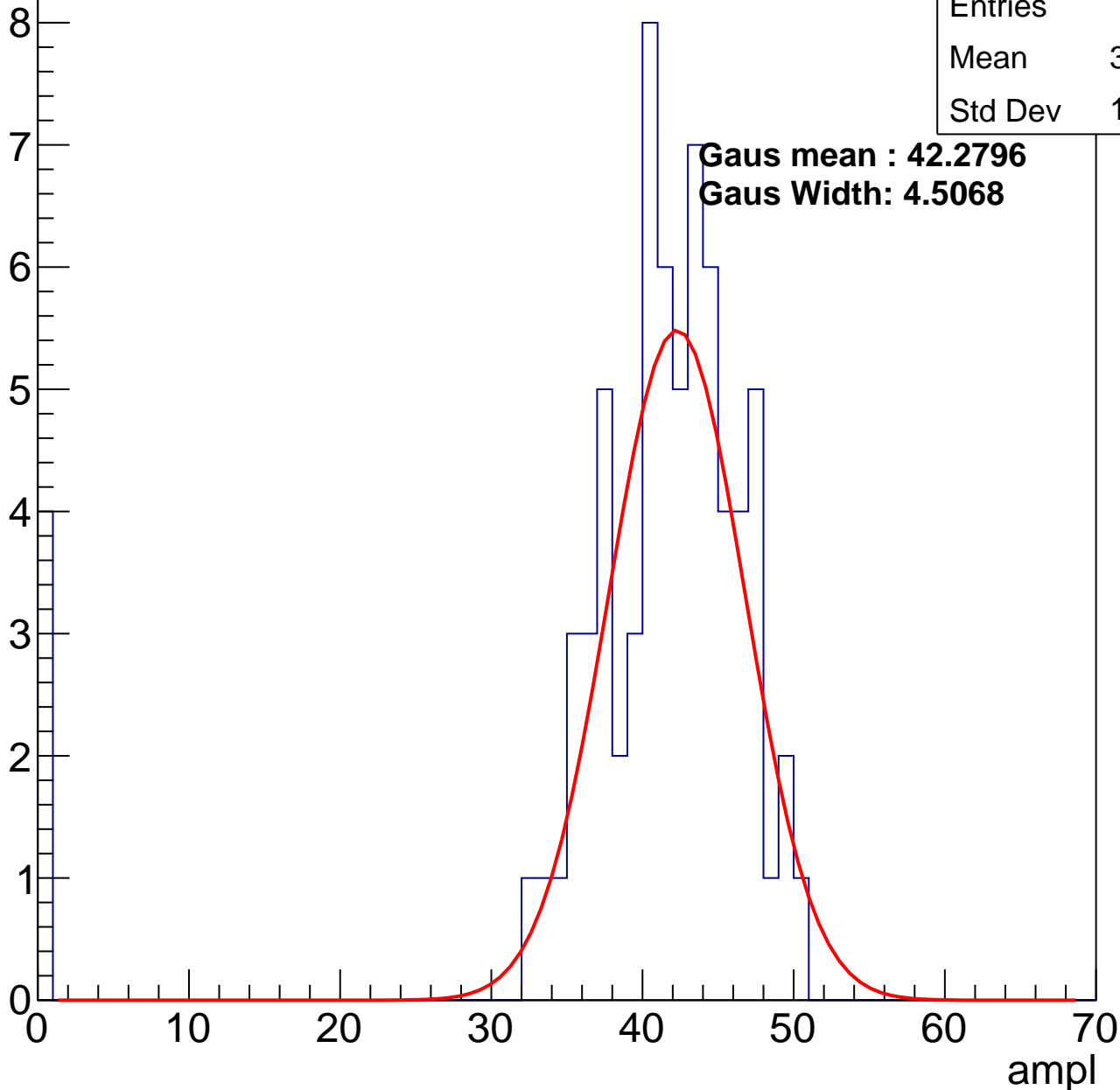
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	72
Mean	39.25
Std Dev	10.33

**Gaus mean : 42.2796**

**Gaus Width: 4.5068**

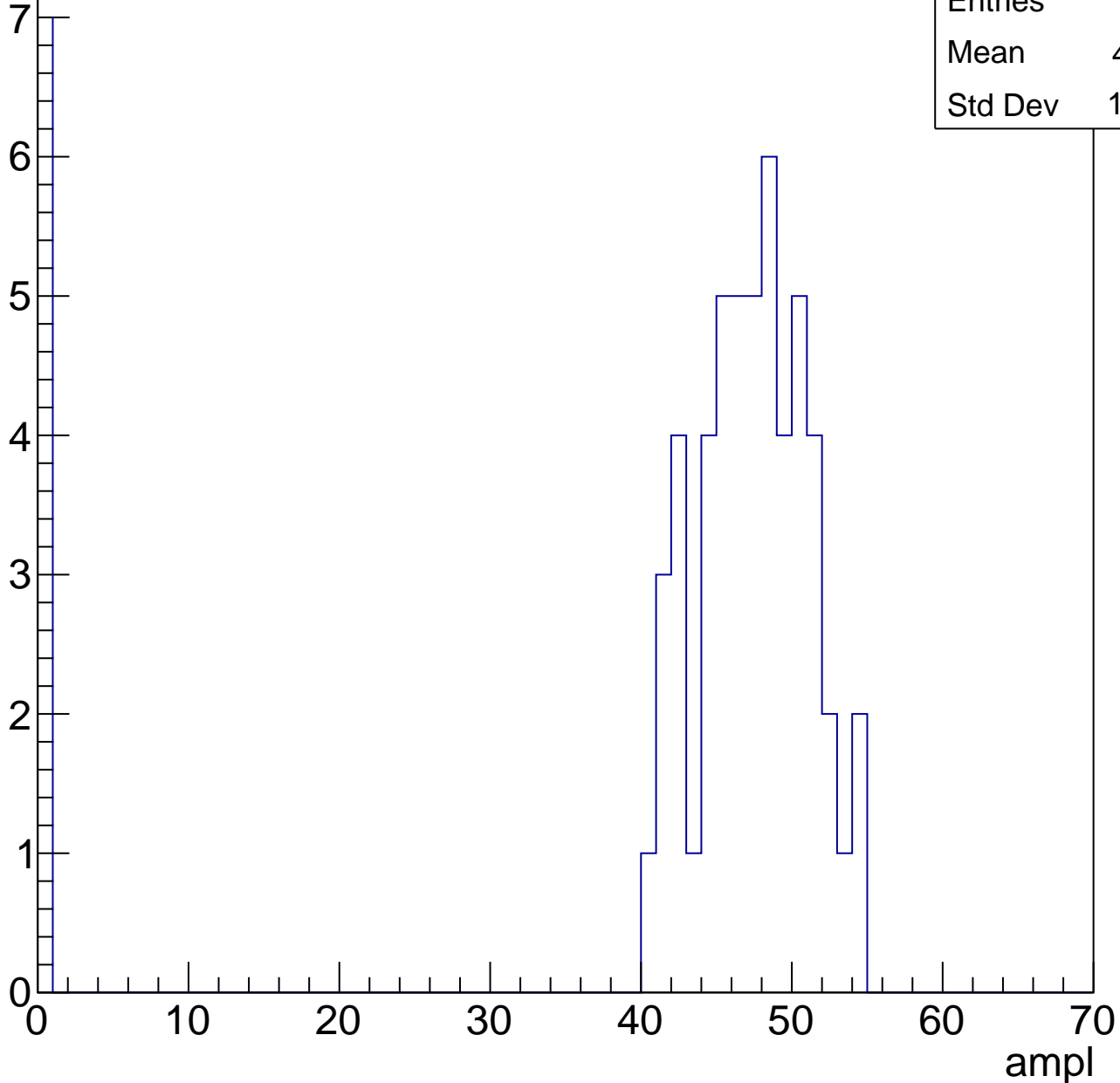


# B1L103S, U26-ch70, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	59
Mean	41.41
Std Dev	15.55

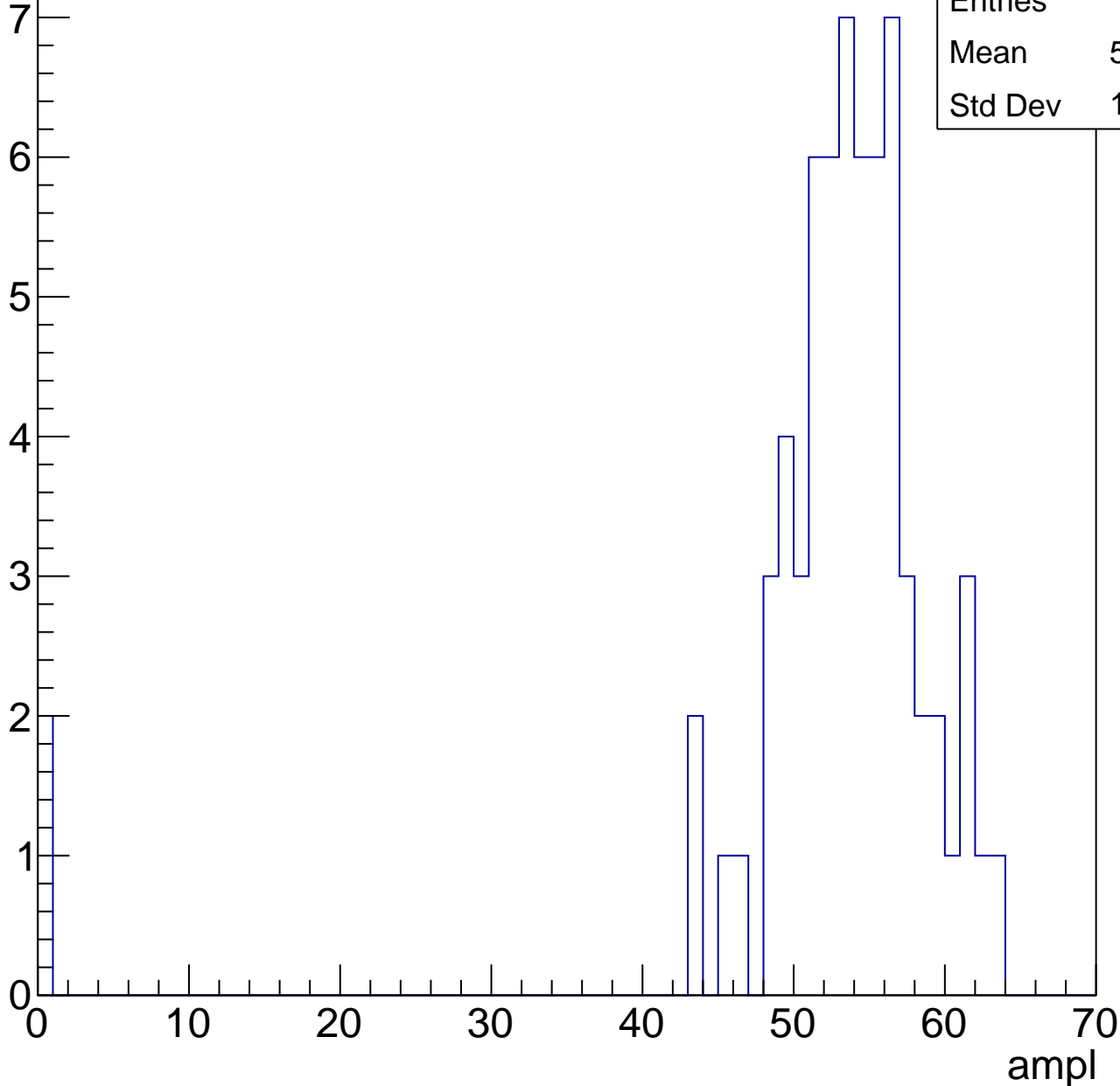


# B1L103S, U26-ch70, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	67
Mean	51.87
Std Dev	10.02

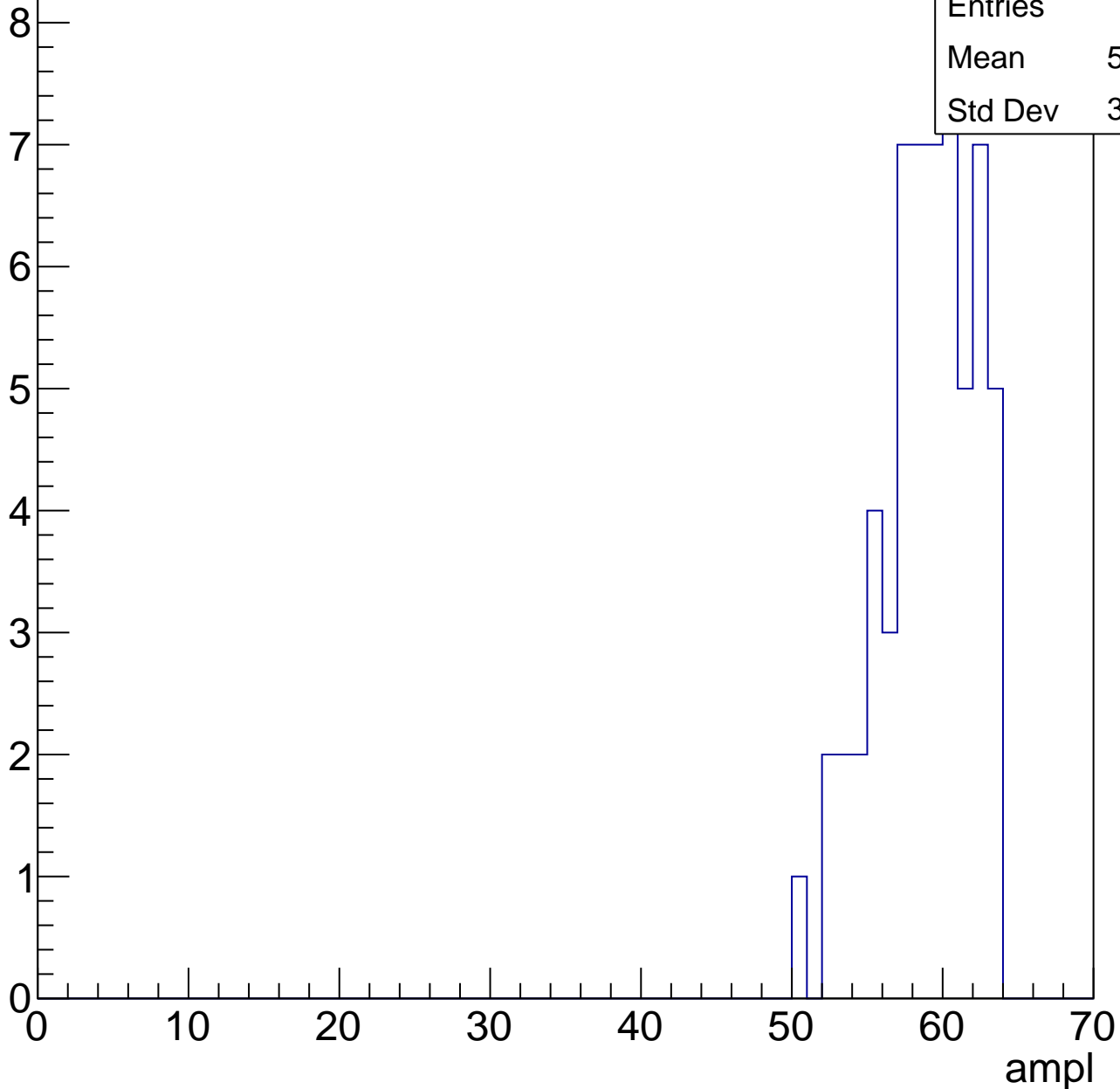


# B1L103S, U26-ch70, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	60
Mean	58.47
Std Dev	3.112



# B1L103S, U26-ch70, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

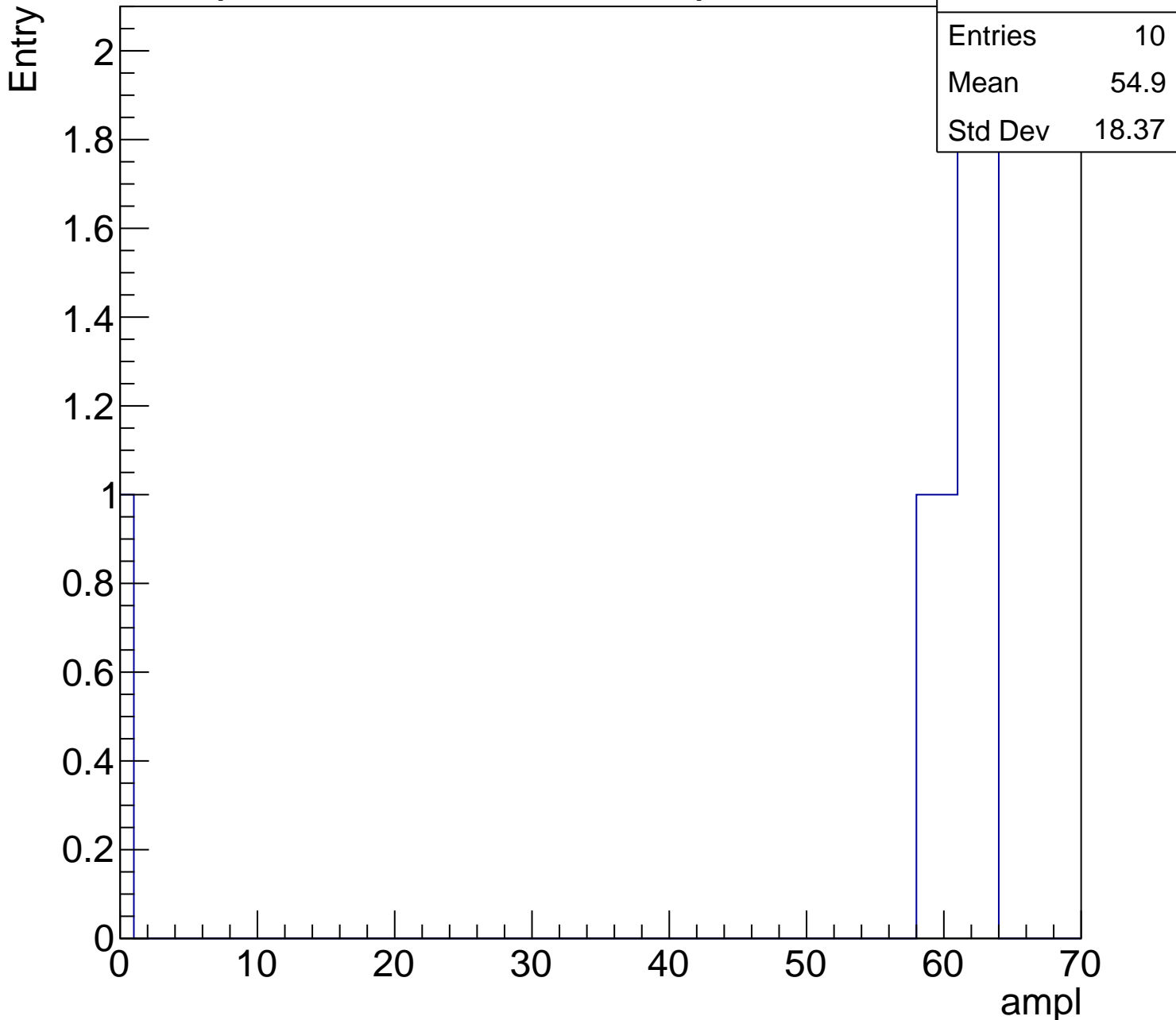
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	10
Mean	54.9
Std Dev	18.37

0 10 20 30 40 50 60 70

ampl



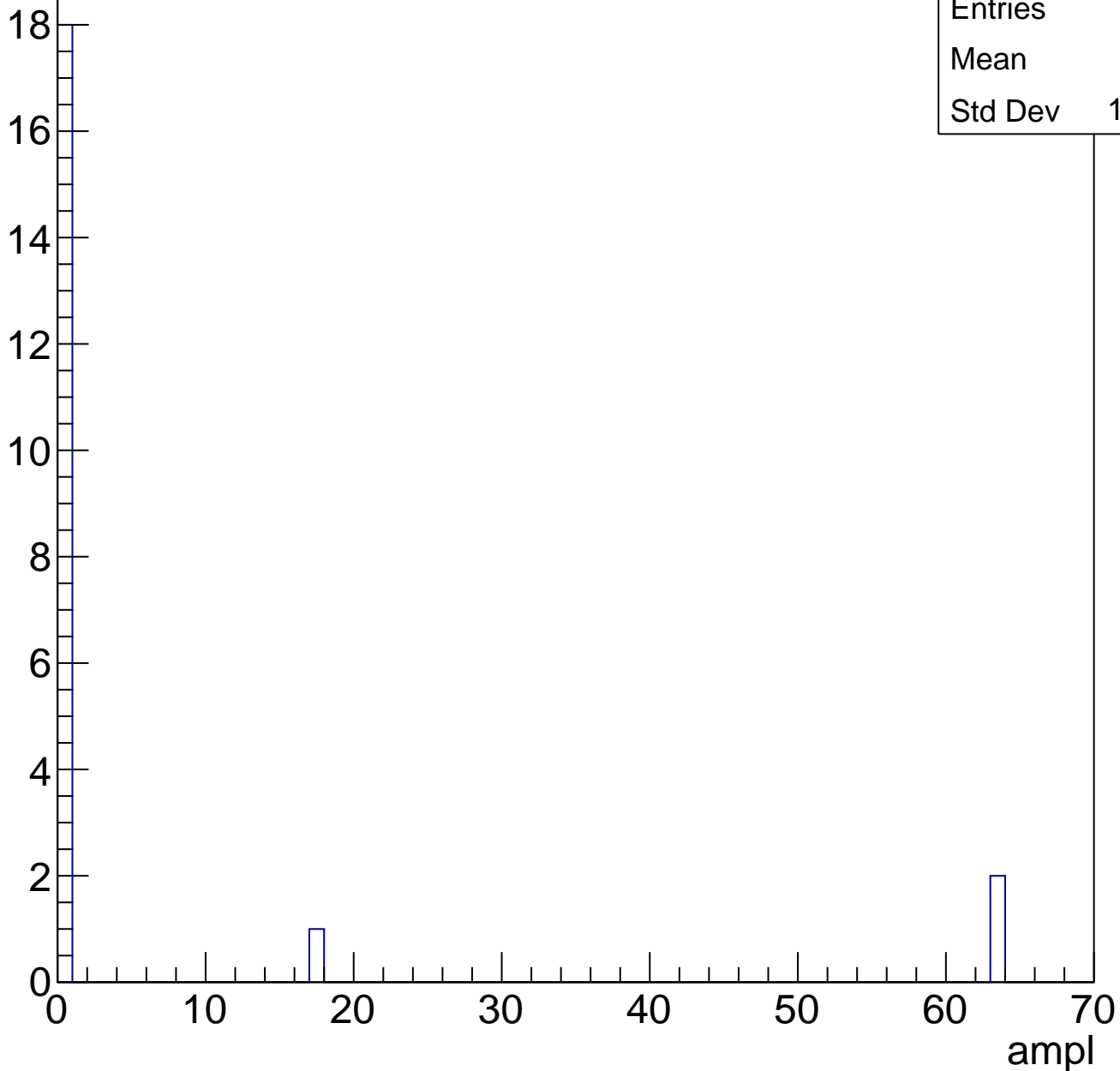


# B1L103S, U26-ch70, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	21
Mean	6.81
Std Dev	18.58

Entry



# B1L103S, U26-ch71, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	80
Mean	24
Std Dev	11

**Gaus mean : 29.9803**

**Gaus Width: 3.3388**

Entry

12

10

8

6

4

2

0

0

10

20

30

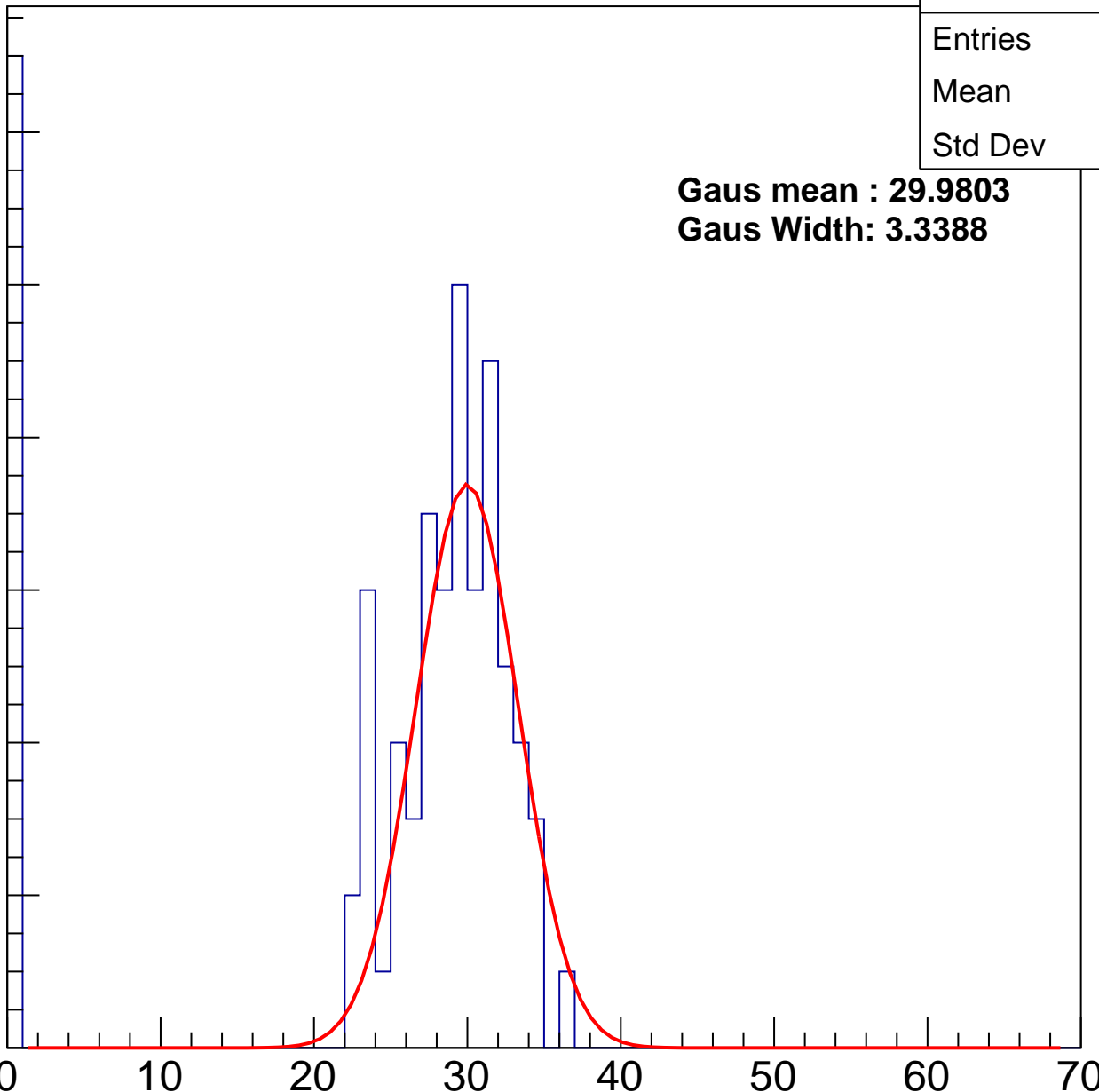
40

50

60

70

ampl



# B1L103S, U26-ch71, adc1

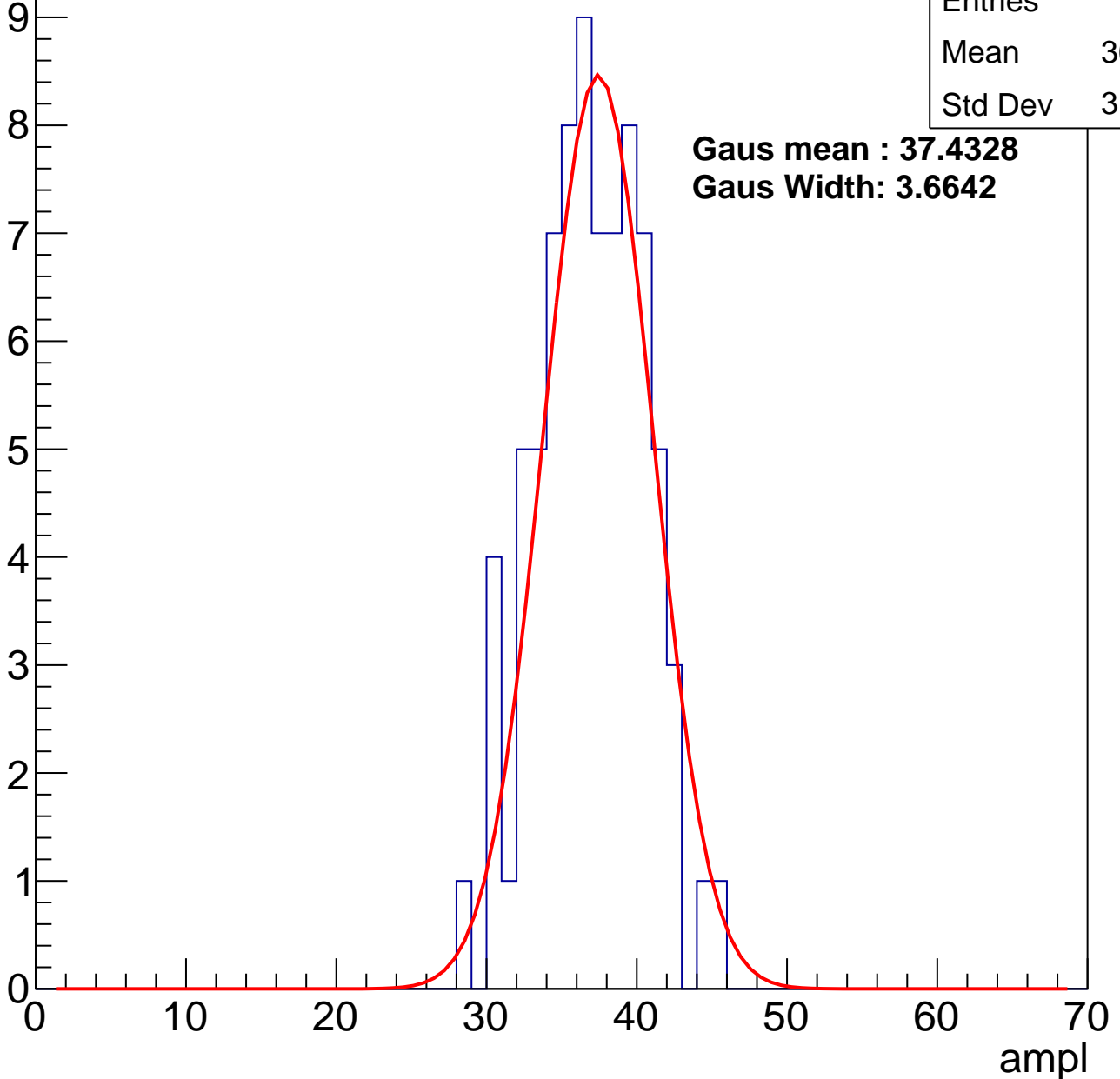
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	79
Mean	36.49
Std Dev	3.507

**Gaus mean : 37.4328**

**Gaus Width: 3.6642**



# B1L103S, U26-ch71, adc2

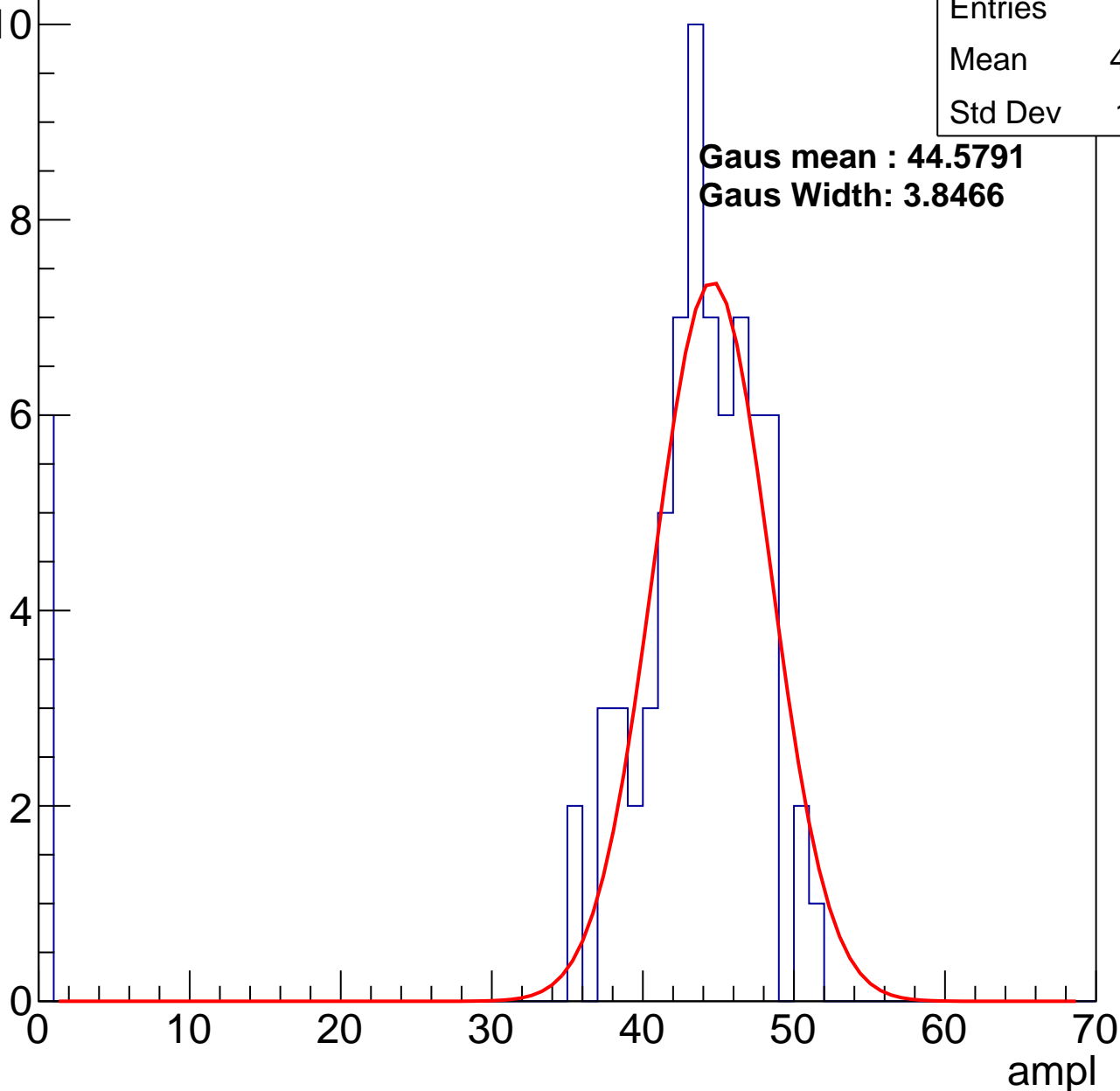
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	76
Mean	40.04
Std Dev	12.21

**Gaus mean : 44.5791**

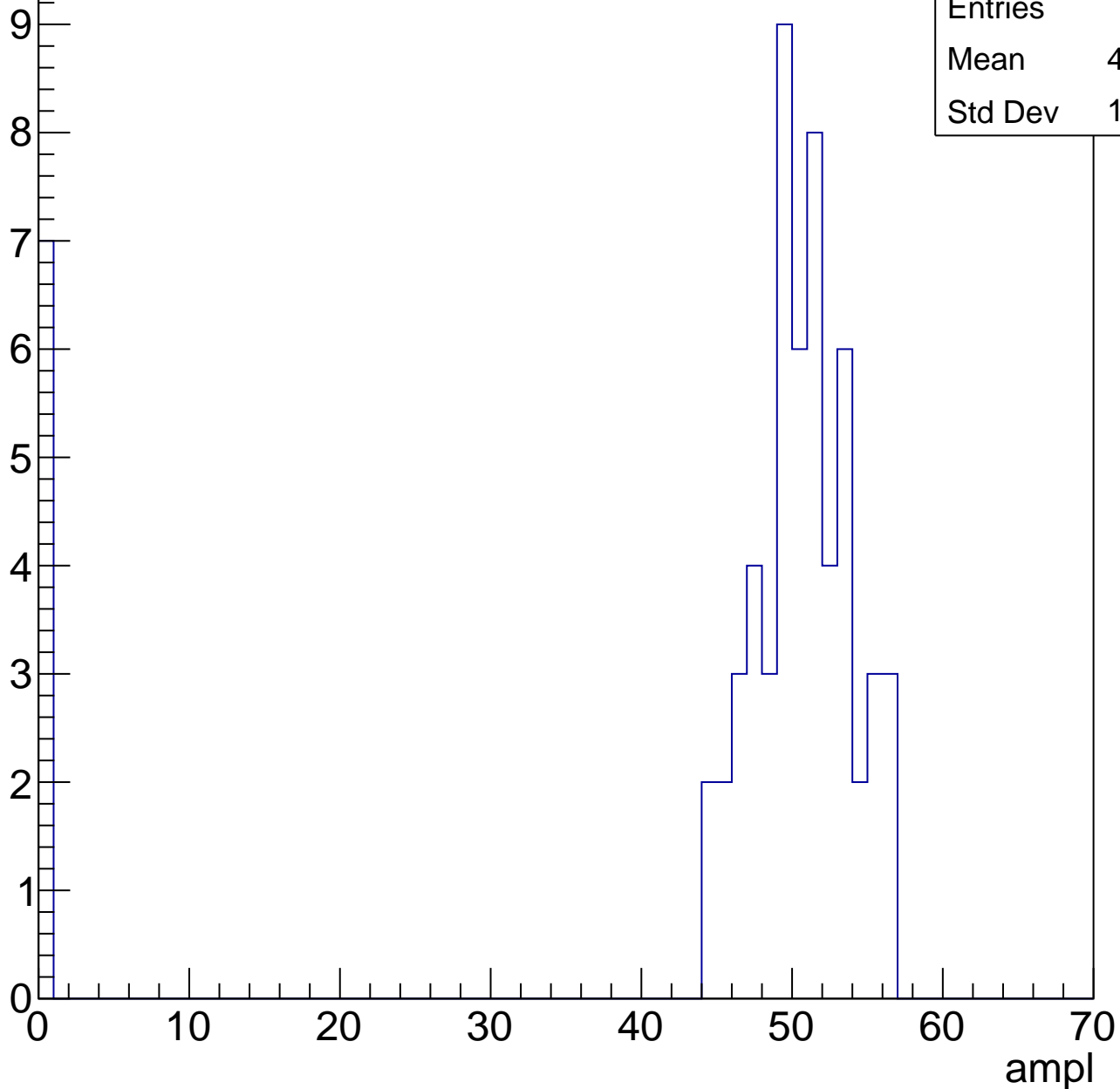
**Gaus Width: 3.8466**



# B1L103S, U26-ch71, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

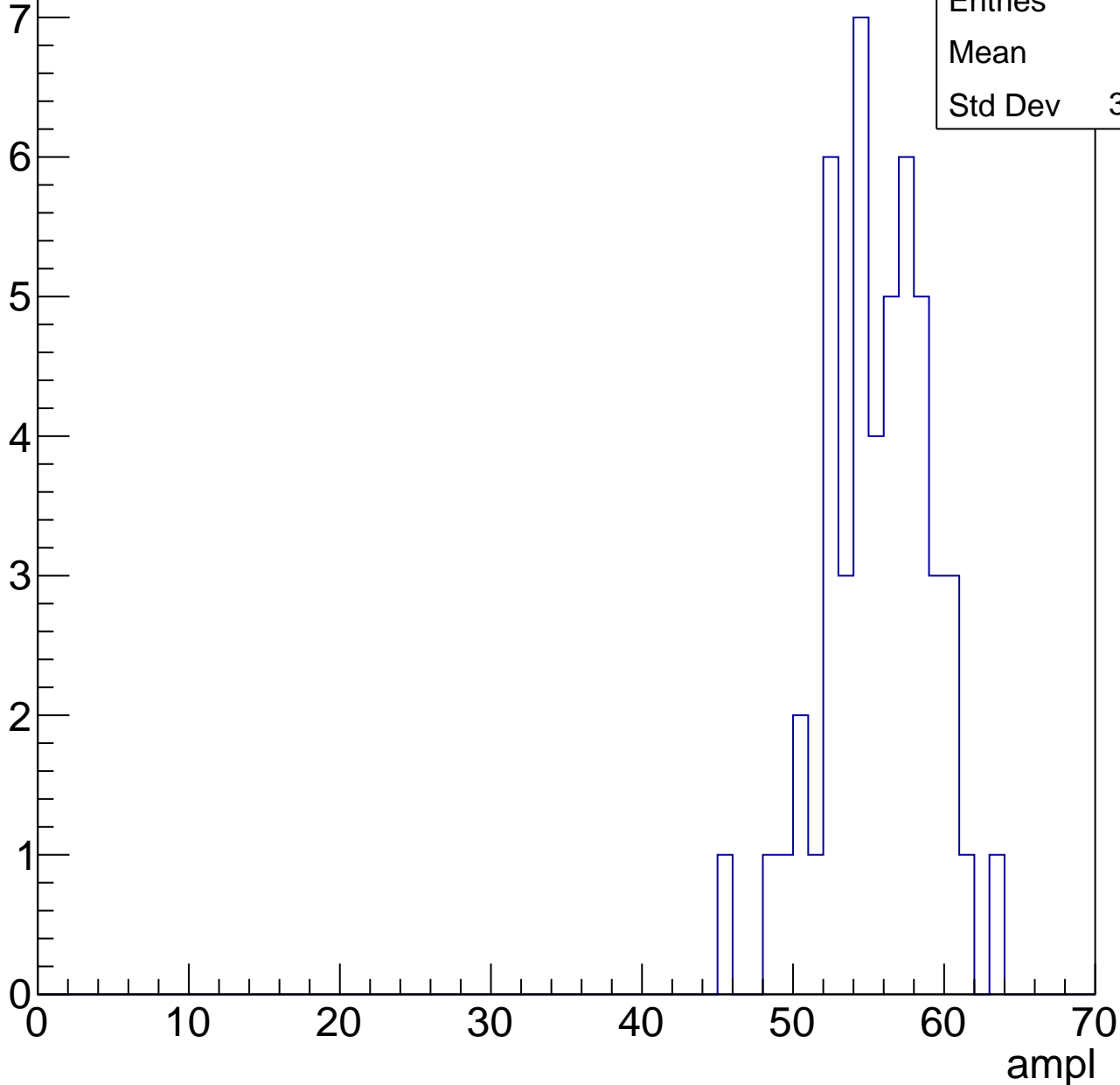


# B1L103S, U26-ch71, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	50
Mean	55.1
Std Dev	3.523

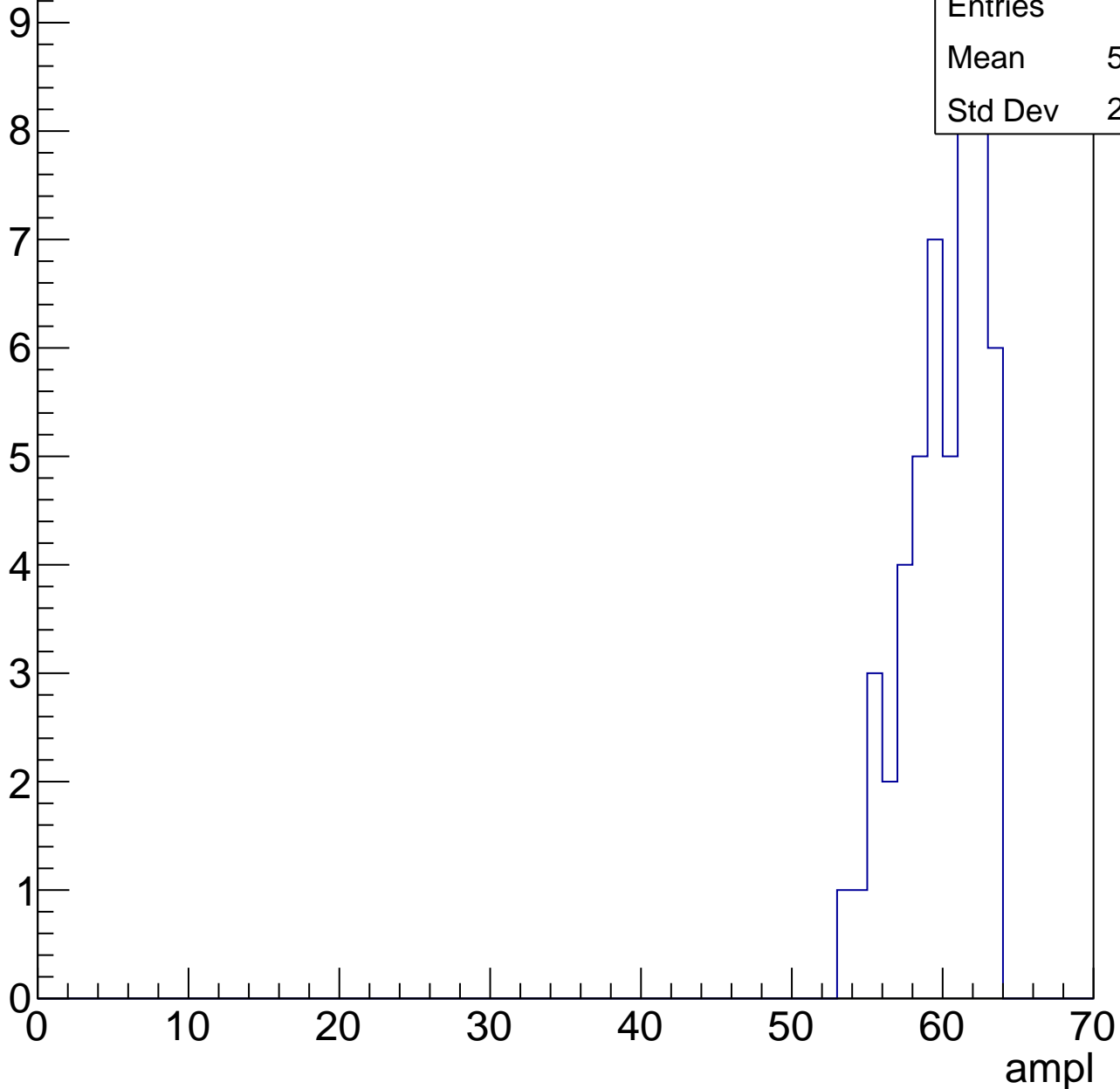


# B1L103S, U26-ch71, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

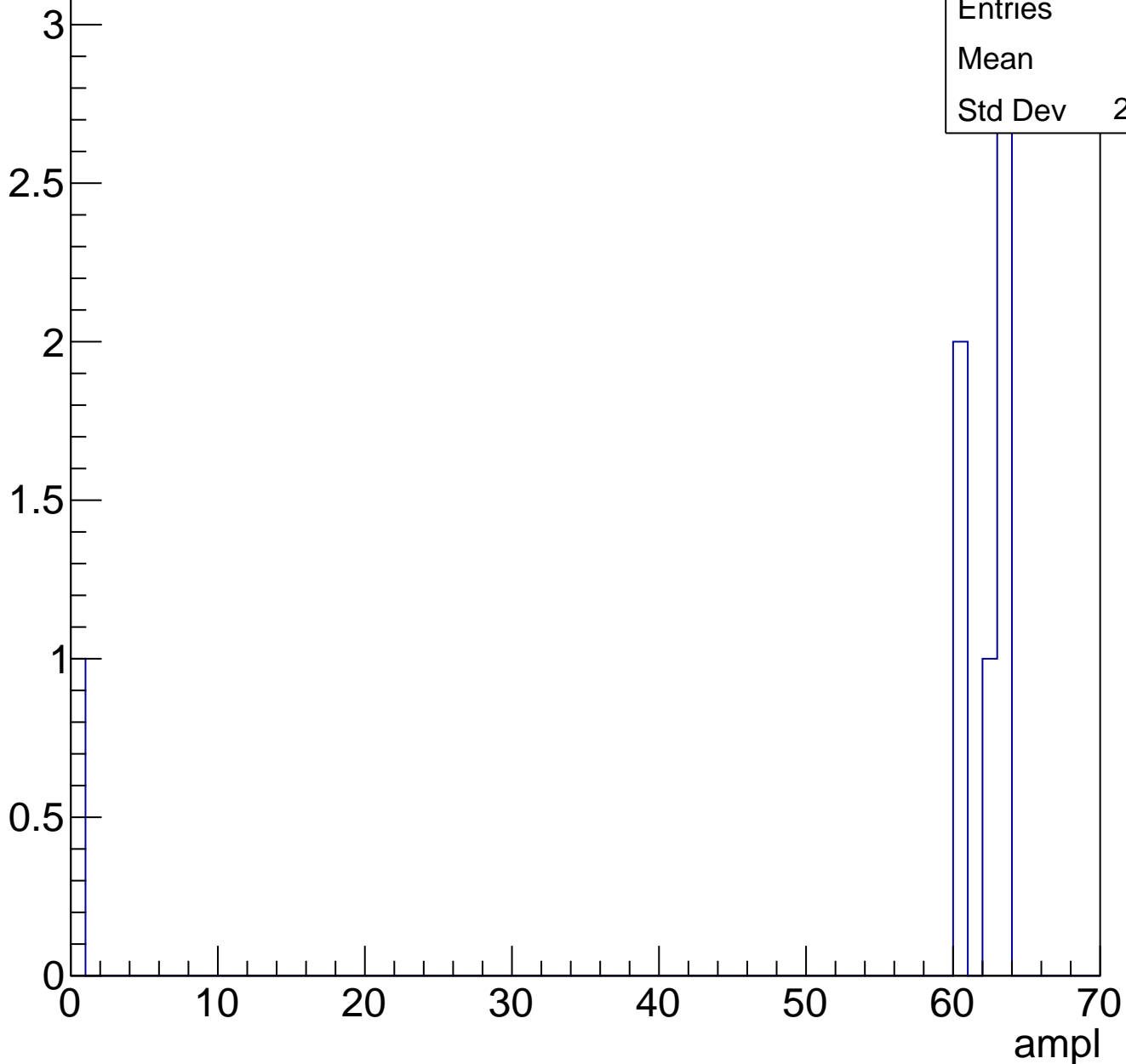
Entries	51
Mean	59.59
Std Dev	2.598



# B1L103S, U26-ch71, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



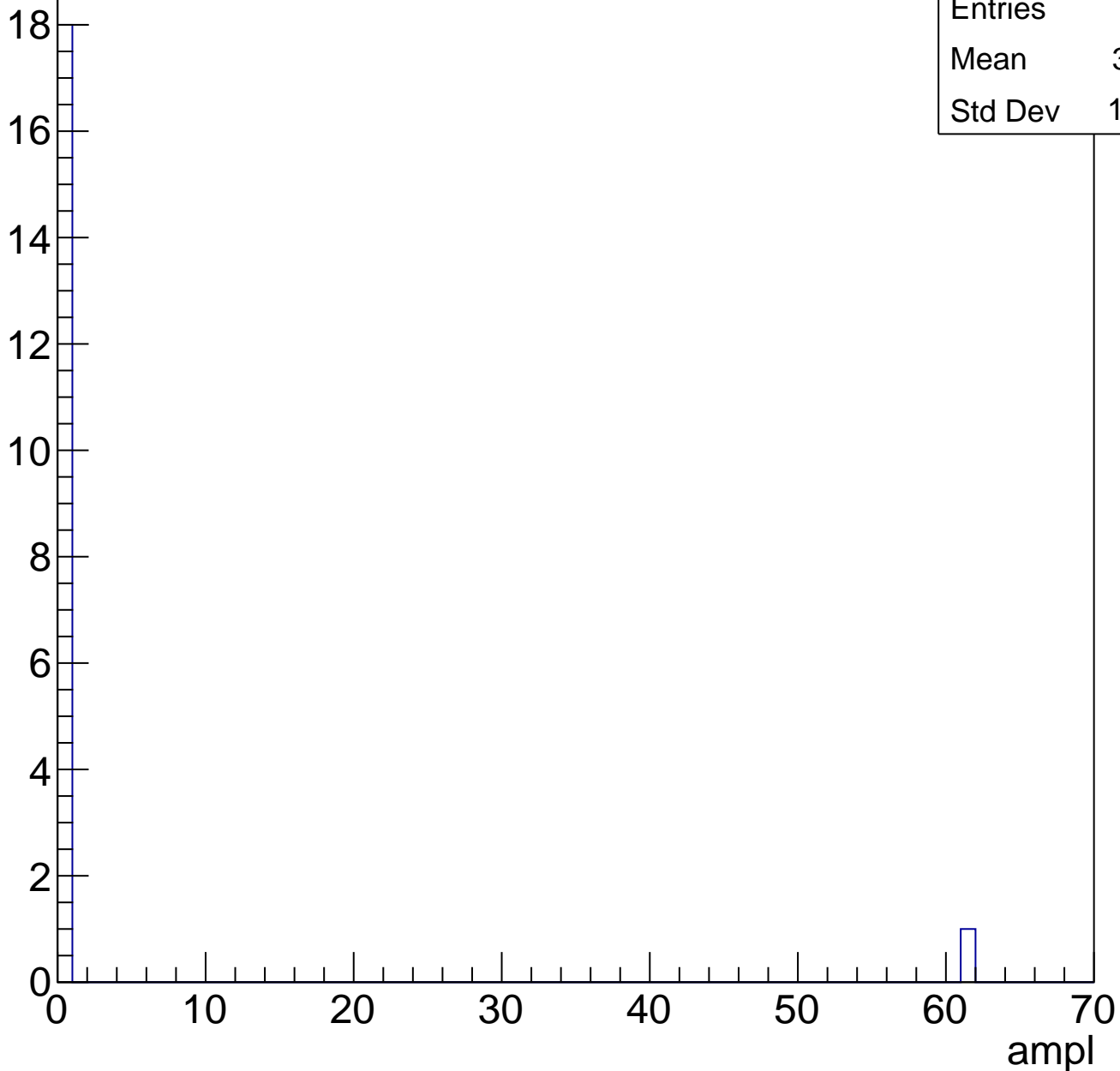


# B1L103S, U26-ch71, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	19
Mean	3.211
Std Dev	13.62

Entry



# B1L103S, U26-ch72, adc0

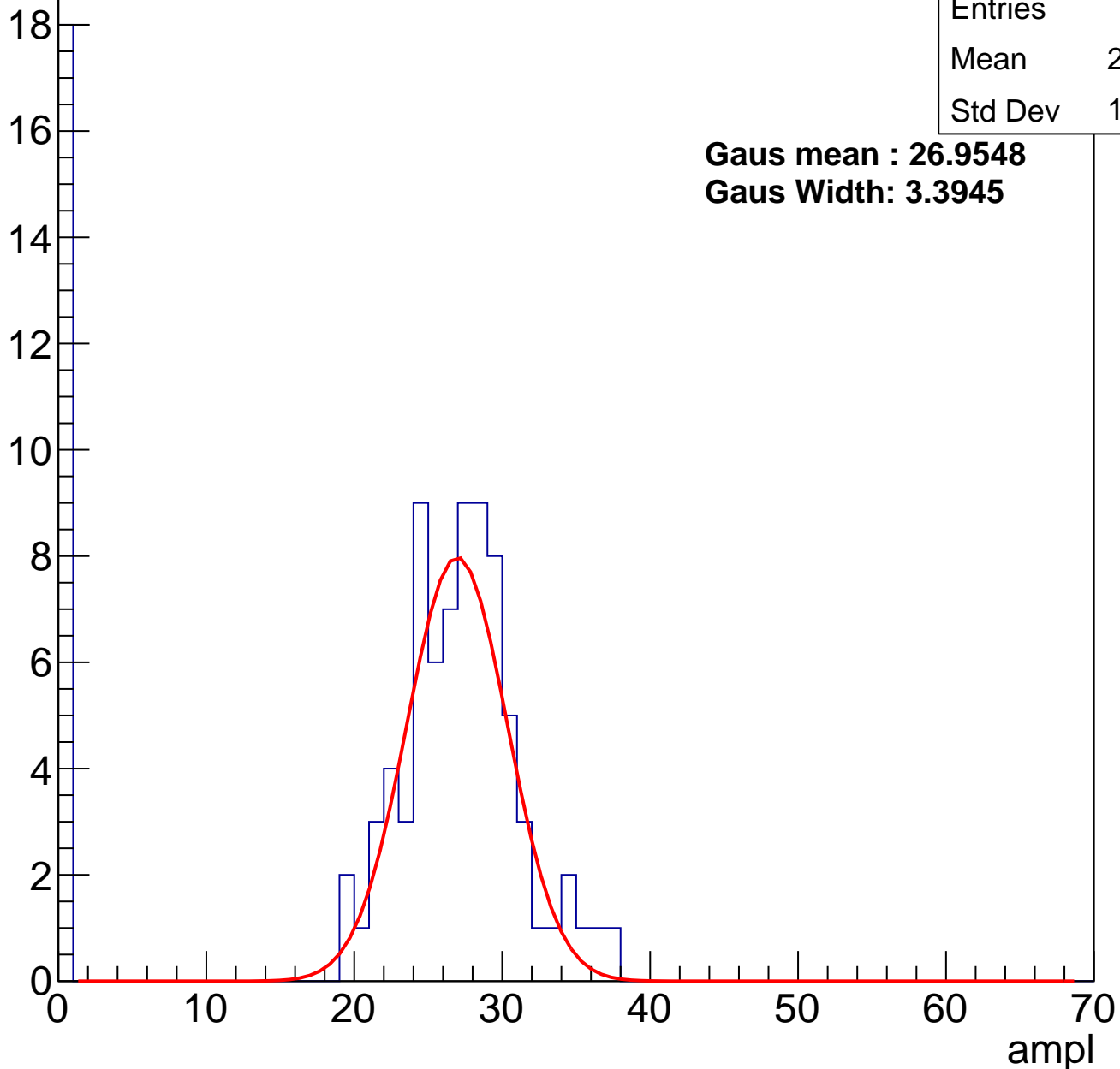
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	94
Mean	21.67
Std Dev	11.08

**Gaus mean : 26.9548**

**Gaus Width: 3.3945**

Entry



# B1L103S, U26-ch72, adc1

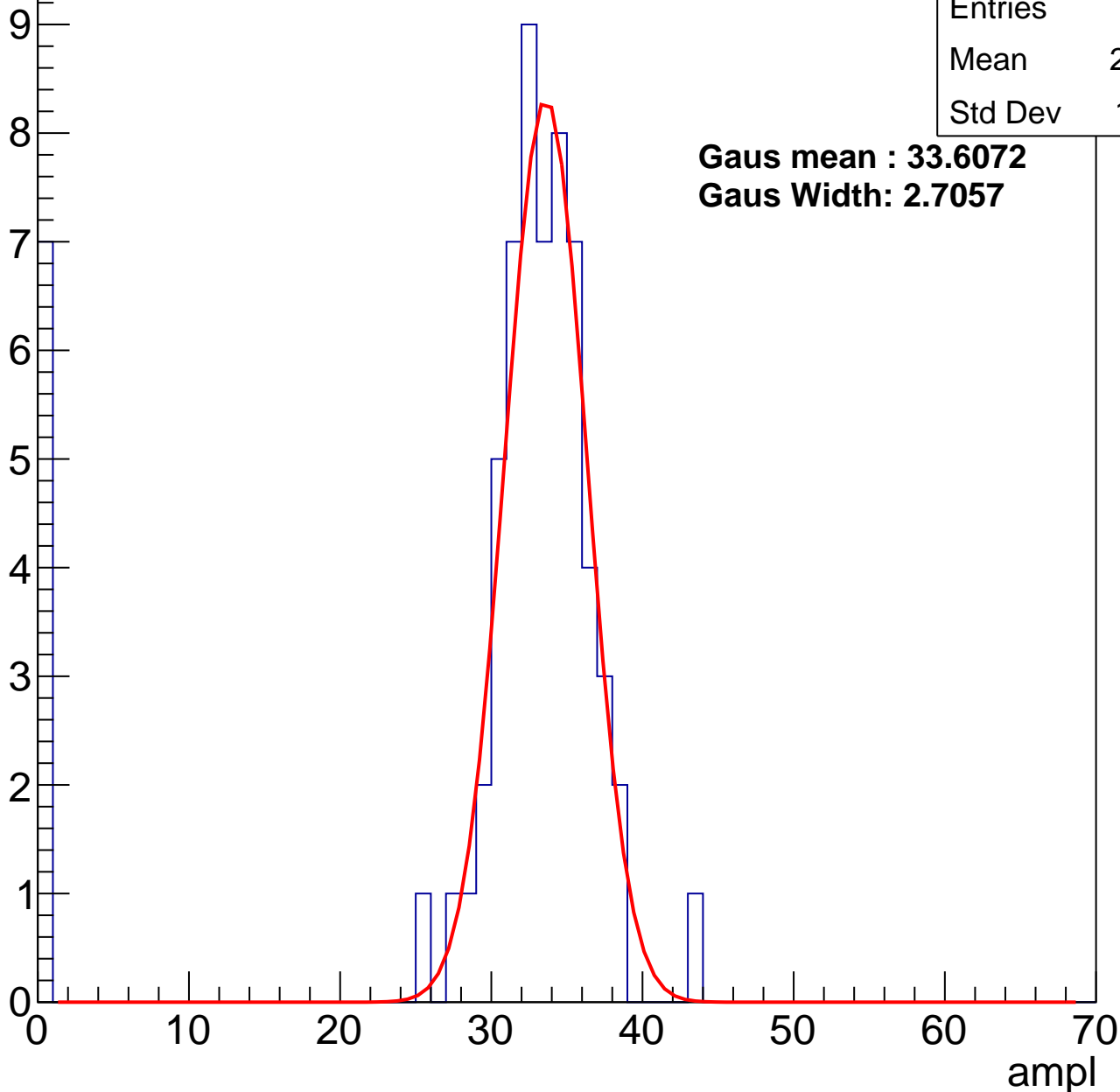
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	65
Mean	29.46
Std Dev	10.61

**Gaus mean : 33.6072**

**Gaus Width: 2.7057**



# B1L103S, U26-ch72, adc2

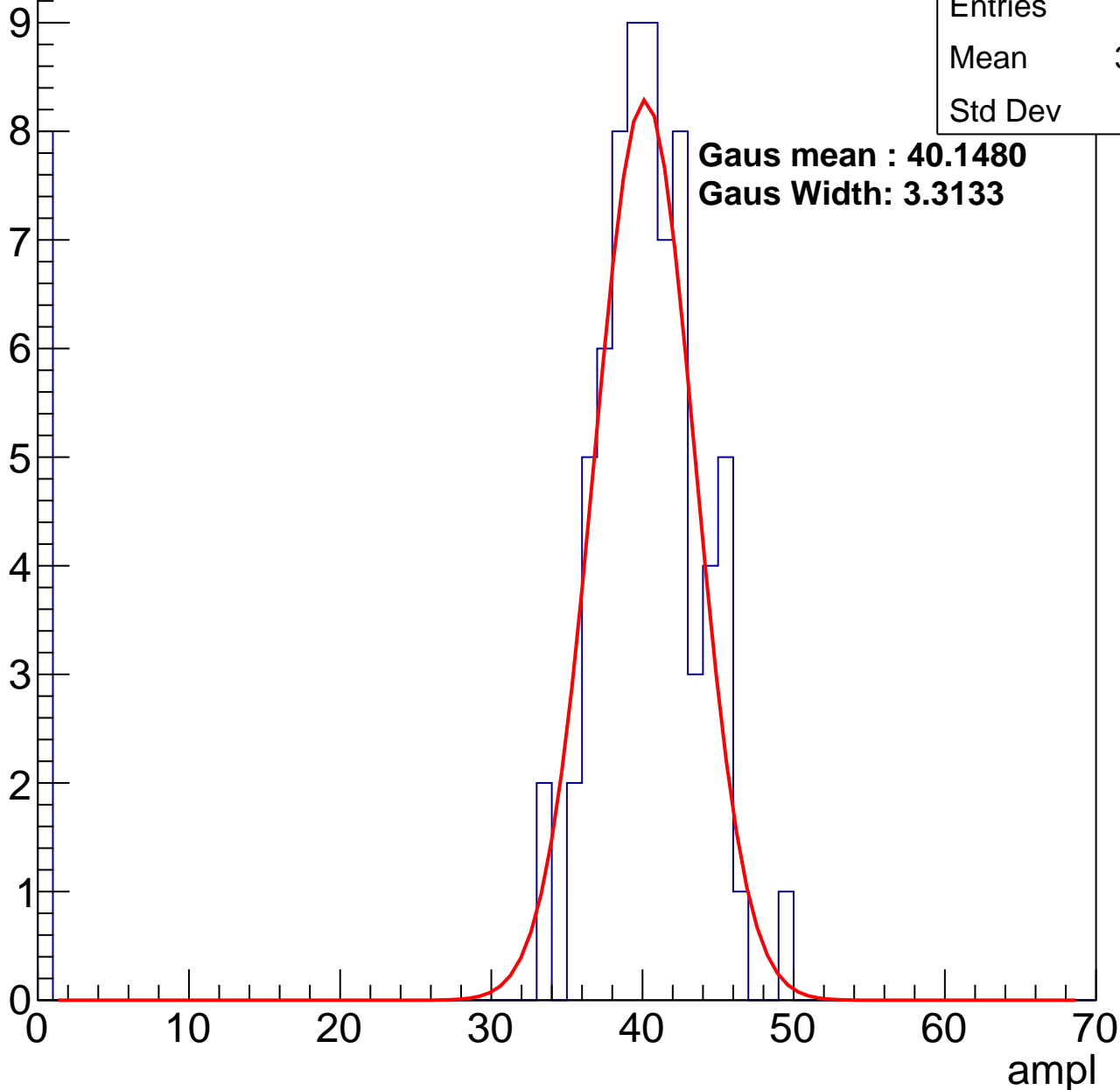
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	78
Mean	35.91
Std Dev	12.5

**Gaus mean : 40.1480**

**Gaus Width: 3.3133**

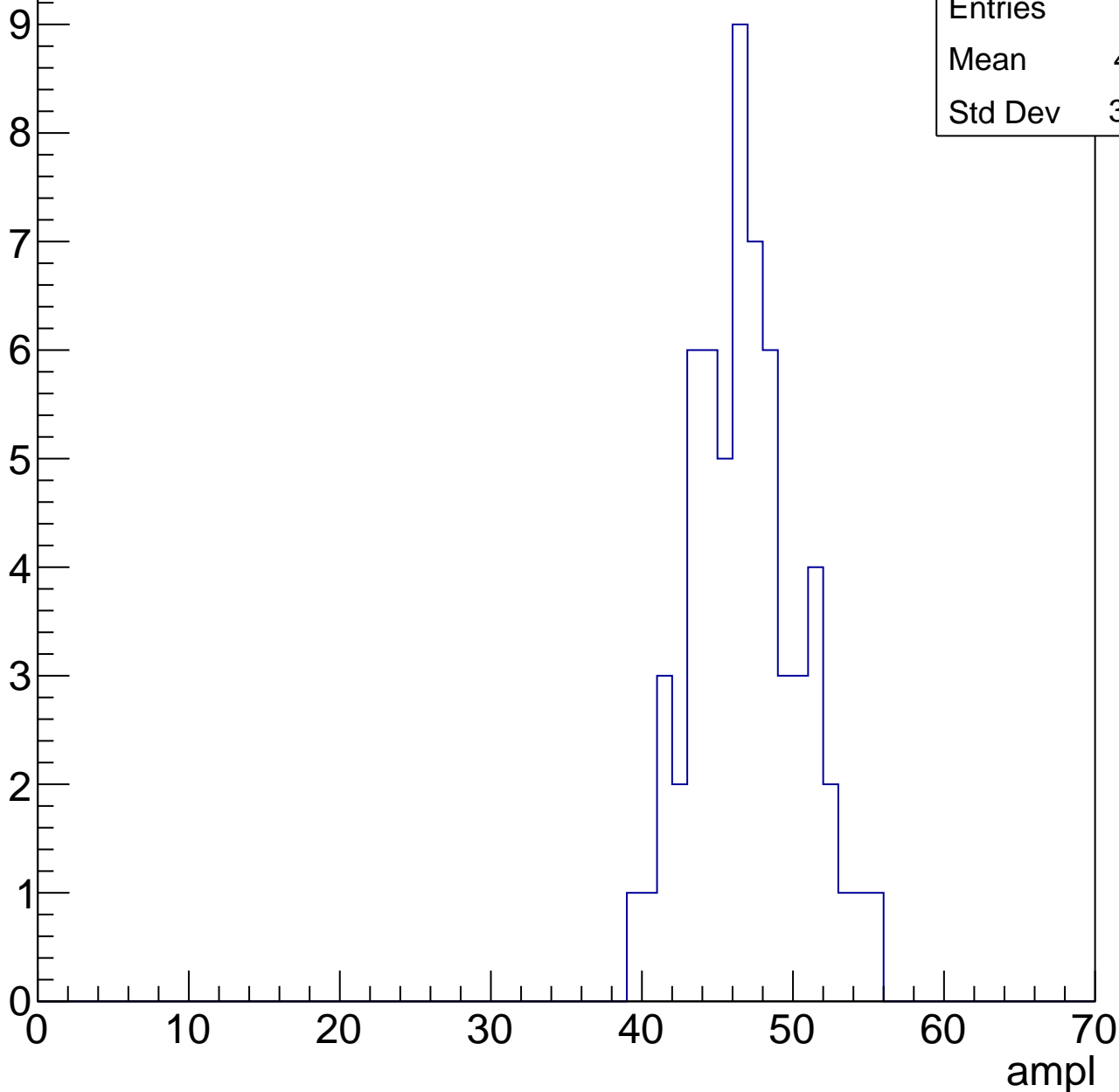


# B1L103S, U26-ch72, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

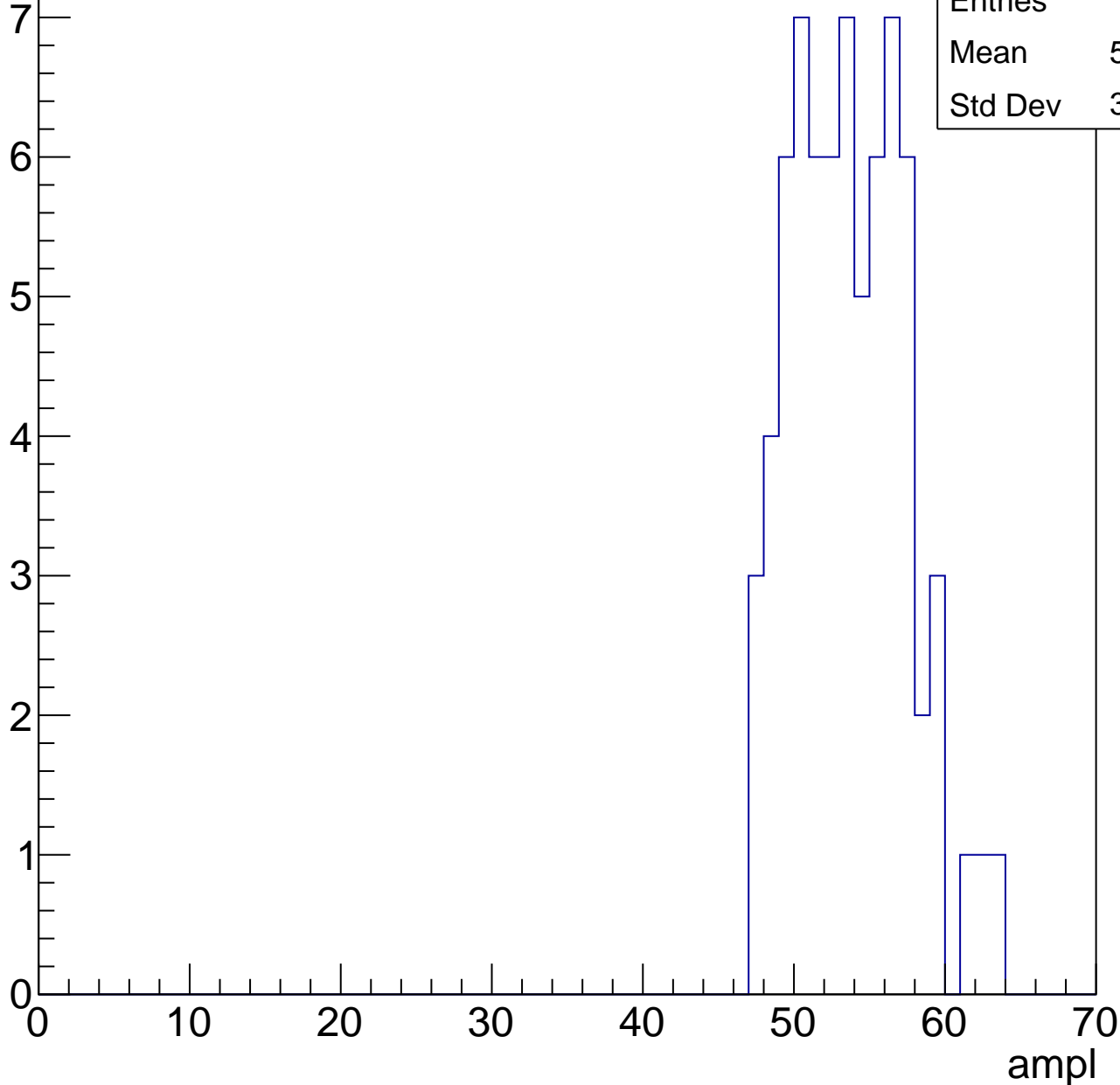
Entries	61
Mean	46.41
Std Dev	3.475



# B1L103S, U26-ch72, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

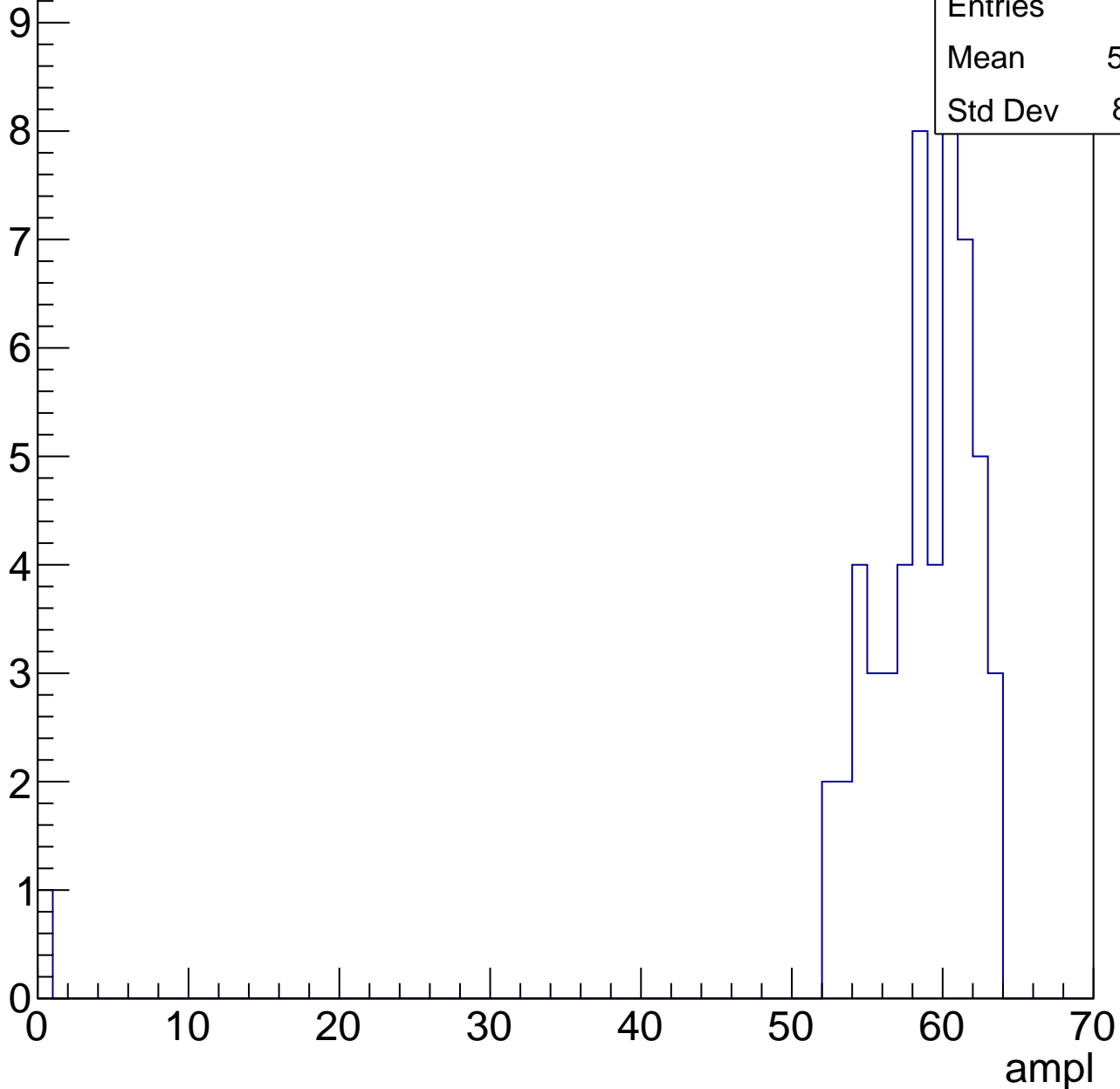


# B1L103S, U26-ch72, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	55
Mean	57.33
Std Dev	8.341

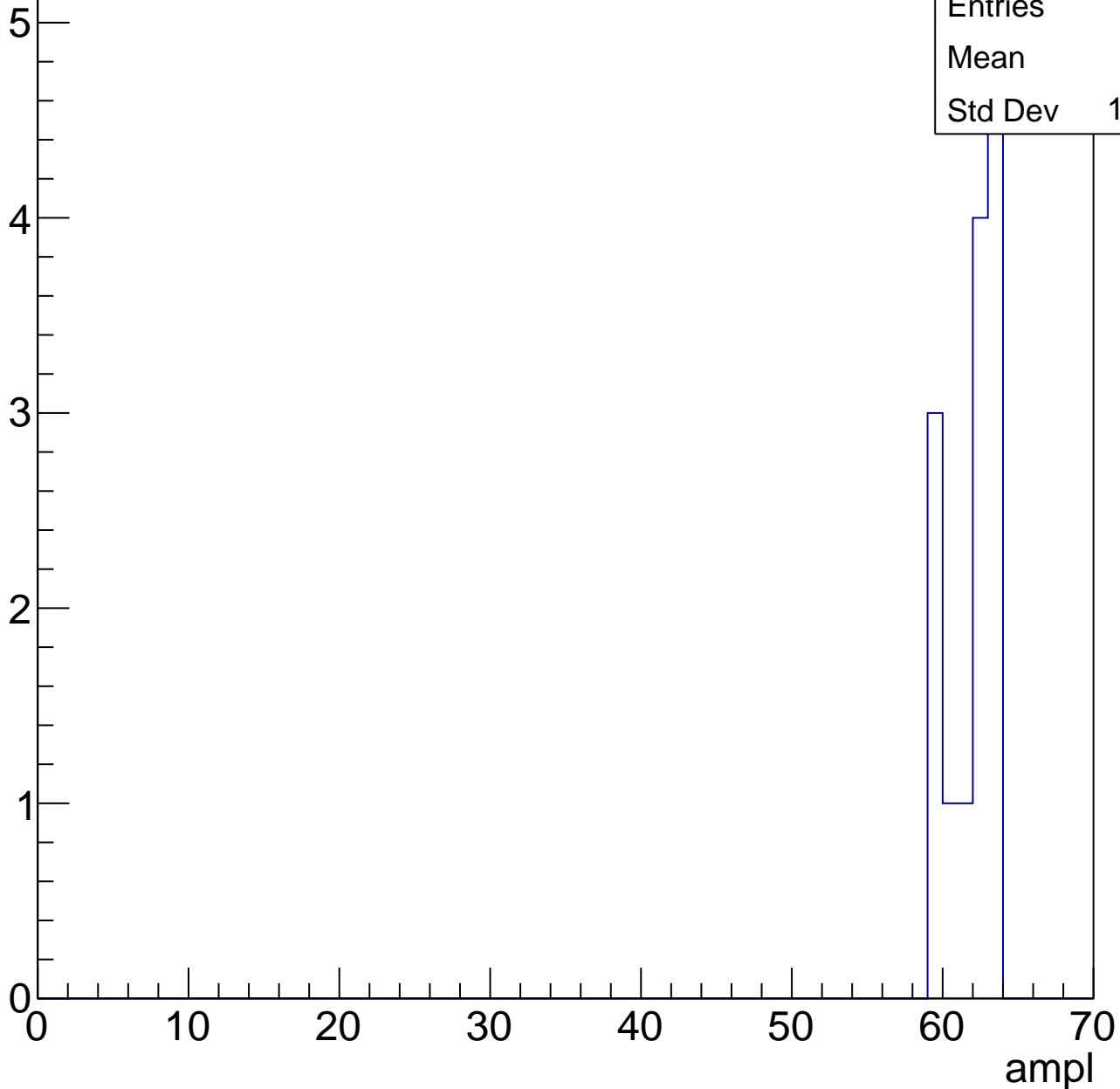


# B1L103S, U26-ch72, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	14
Mean	61.5
Std Dev	1.547



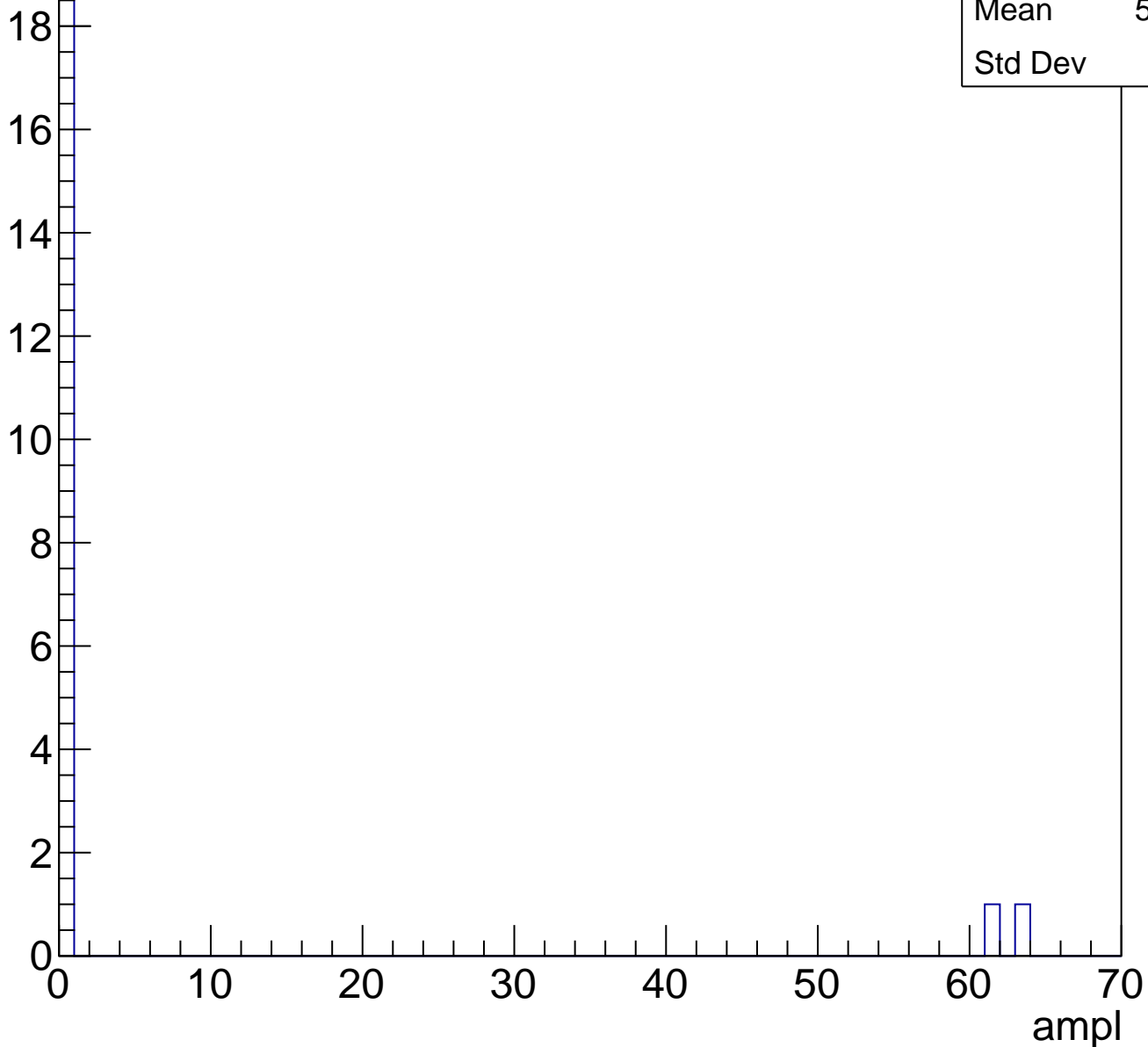


# B1L103S, U26-ch72, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	21
Mean	5.905
Std Dev	18.2

Entry



# B1L103S, U26-ch73, adc0

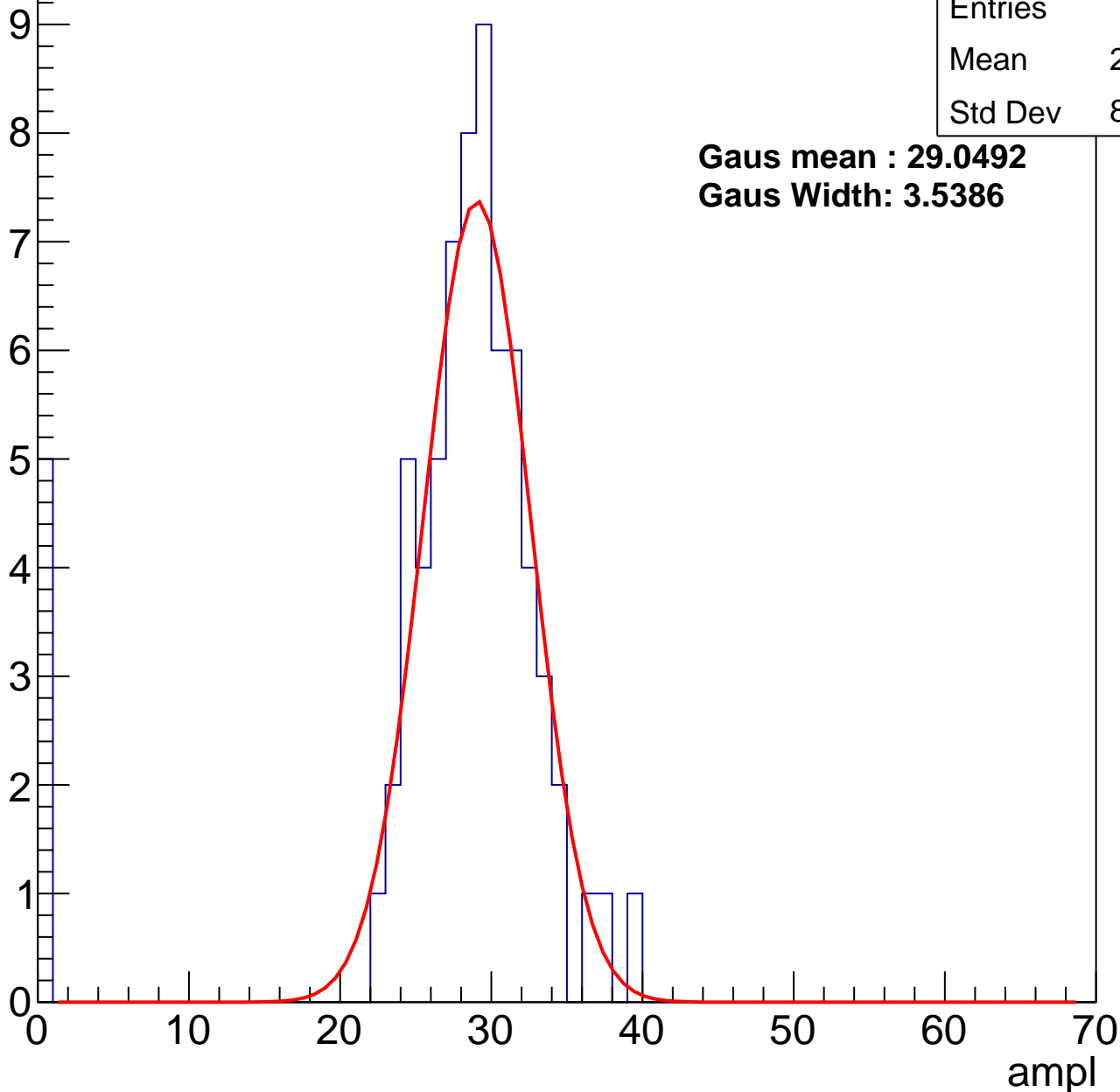
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	70
Mean	26.64
Std Dev	8.092

**Gaus mean : 29.0492**

**Gaus Width: 3.5386**



# B1L103S, U26-ch73, adc1

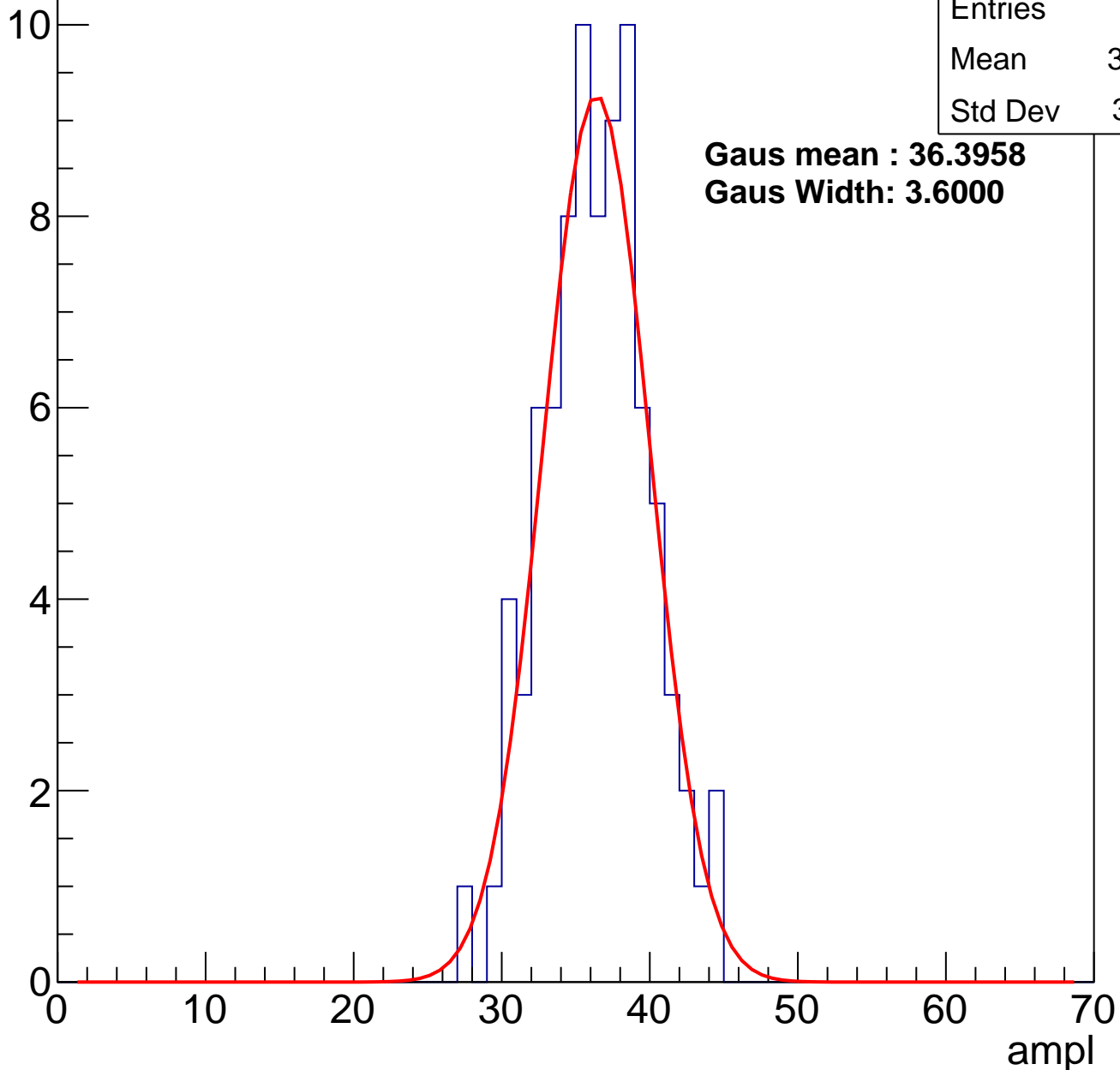
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	85
Mean	35.93
Std Dev	3.511

**Gaus mean : 36.3958**

**Gaus Width: 3.6000**

Entry



# B1L103S, U26-ch73, adc2

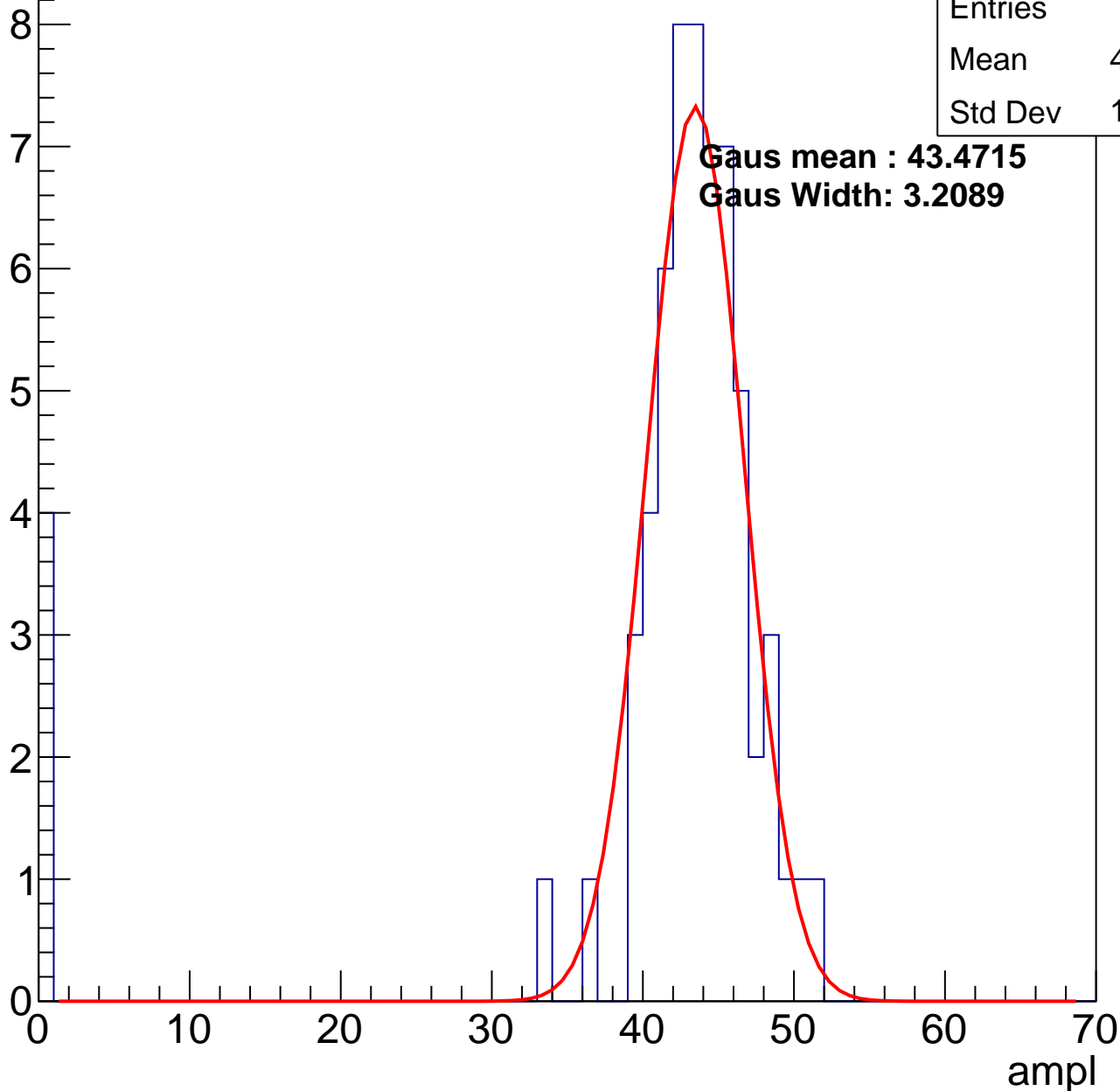
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	62
Mean	40.53
Std Dev	11.09

**Gaus mean : 43.4715**

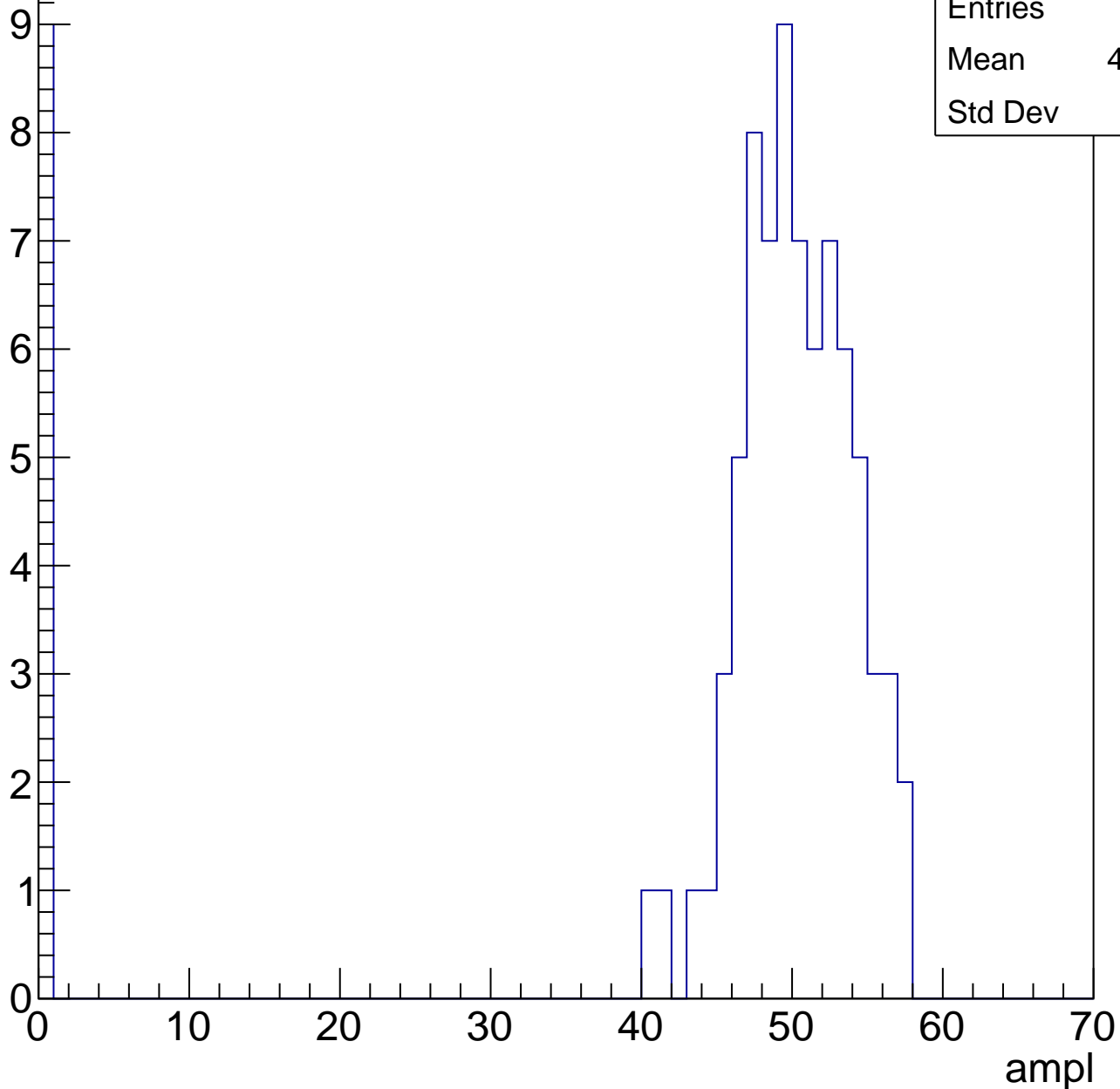
**Gaus Width: 3.2089**



# B1L103S, U26-ch73, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

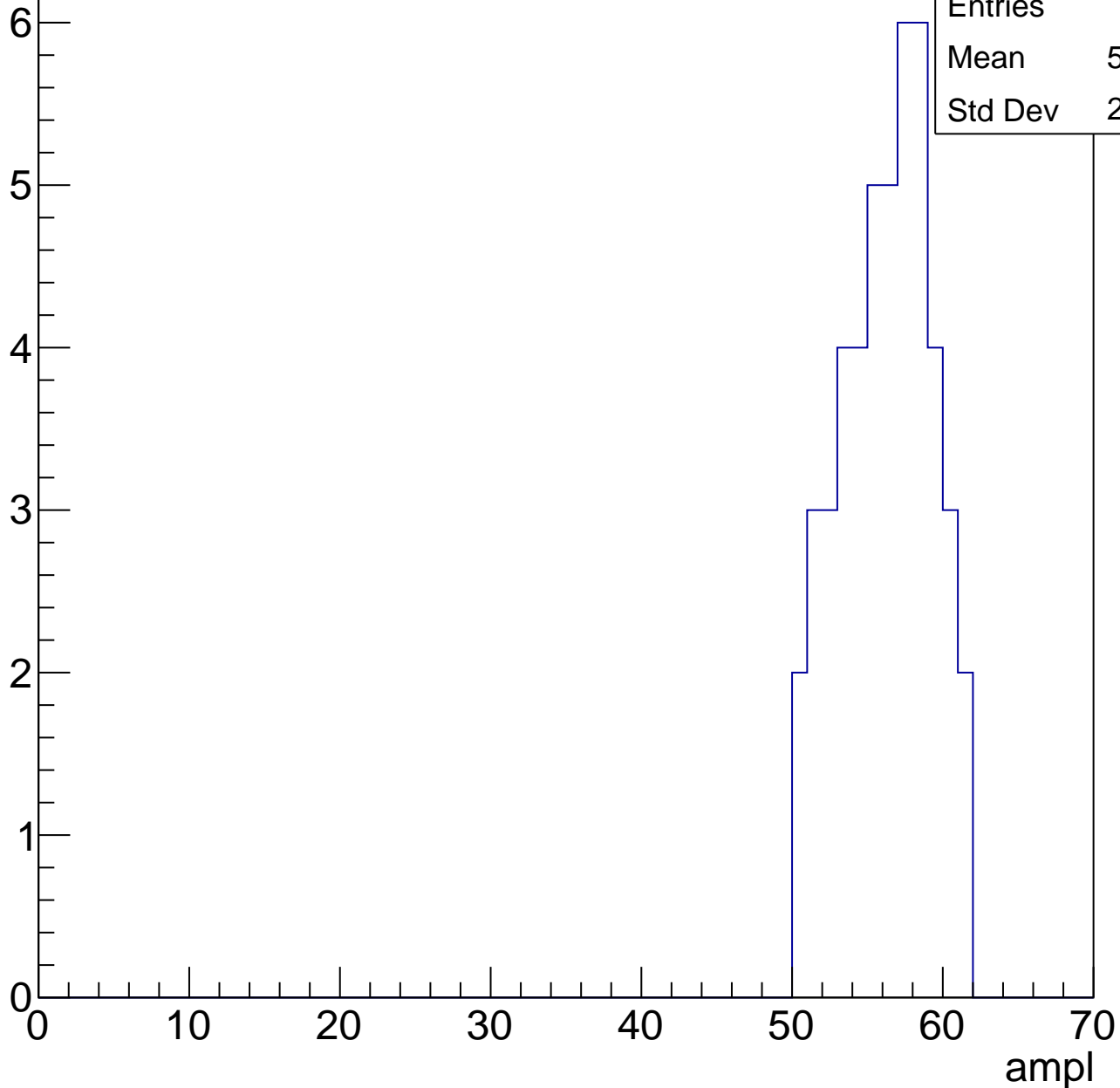
Entry



# B1L103S, U26-ch73, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



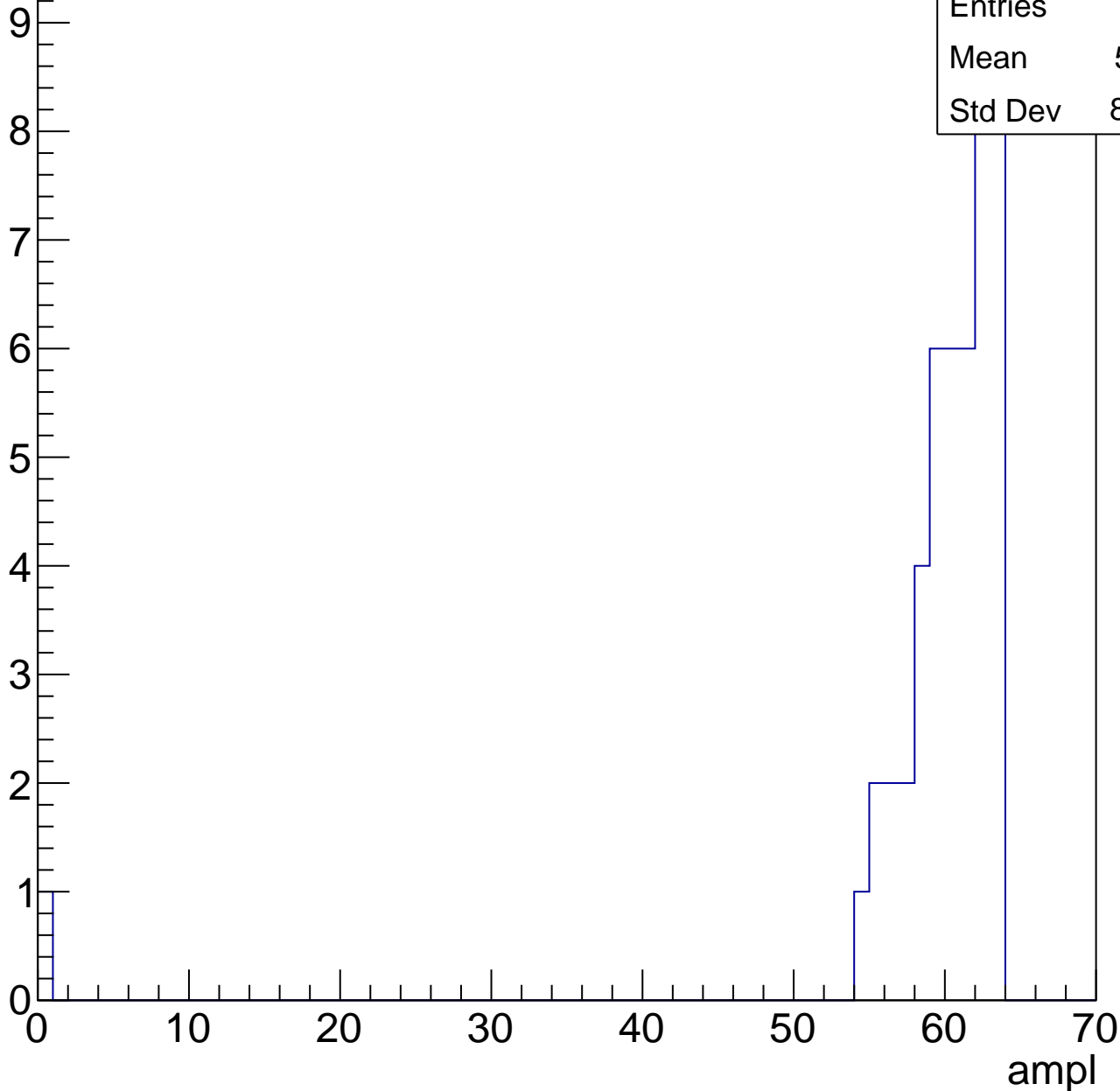
Entries	47
Mean	55.74
Std Dev	2.964

# B1L103S, U26-ch73, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	47
Mean	58.81
Std Dev	8.998



# B1L103S, U26-ch73, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

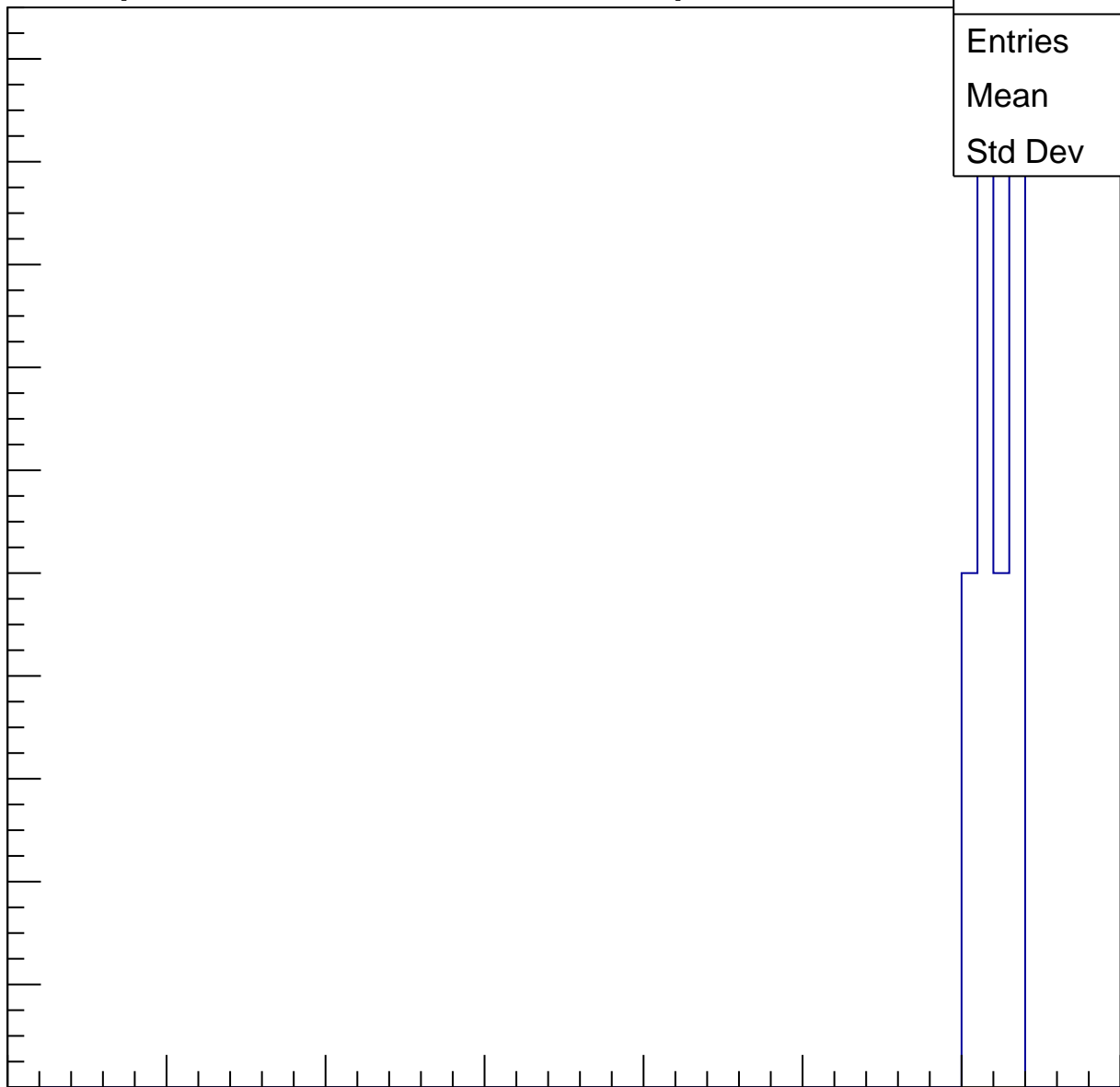
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	6
Mean	61.67
Std Dev	1.106

0 10 20 30 40 50 60 70

ampl





# B1L103S, U26-ch73, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

18  
16  
14  
12  
10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

Entries	19
Mean	0
Std Dev	0

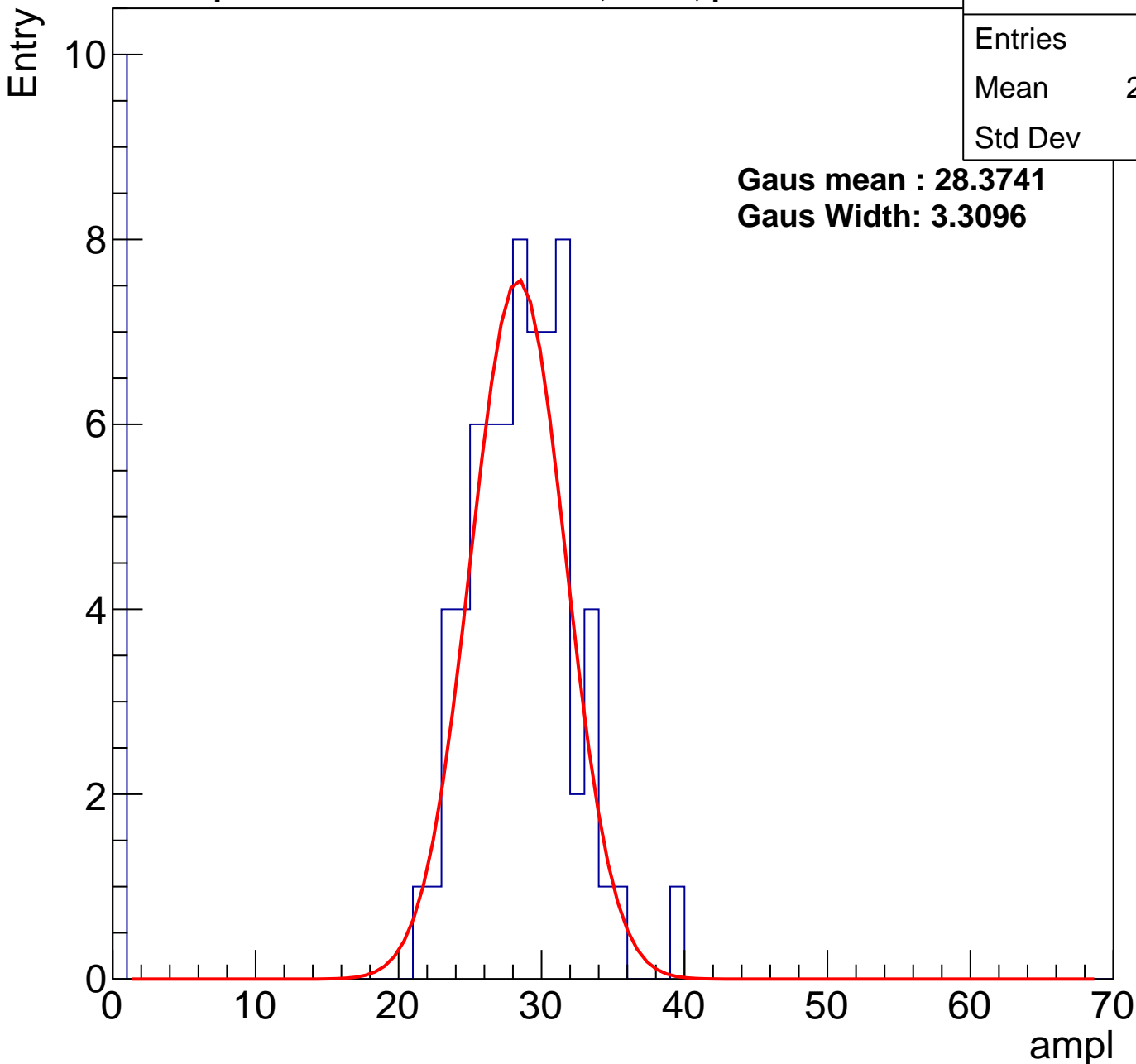
# B1L103S, U26-ch74, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	77
Mean	24.52
Std Dev	9.99

**Gaus mean : 28.3741**

**Gaus Width: 3.3096**



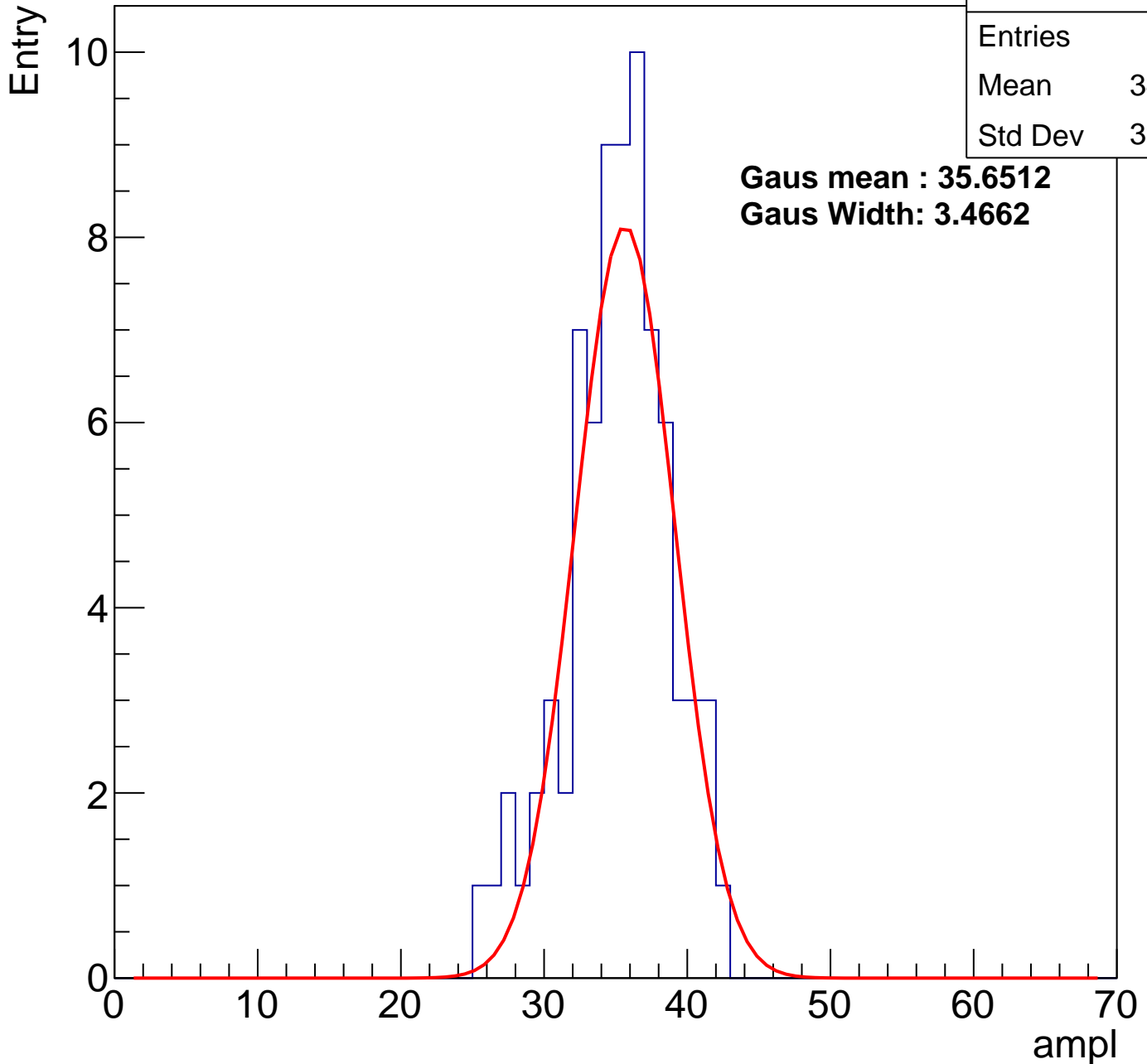
# B1L103S, U26-ch74, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	76
Mean	34.67
Std Dev	3.622

**Gaus mean : 35.6512**

**Gaus Width: 3.4662**



# B1L103S, U26-ch74, adc2

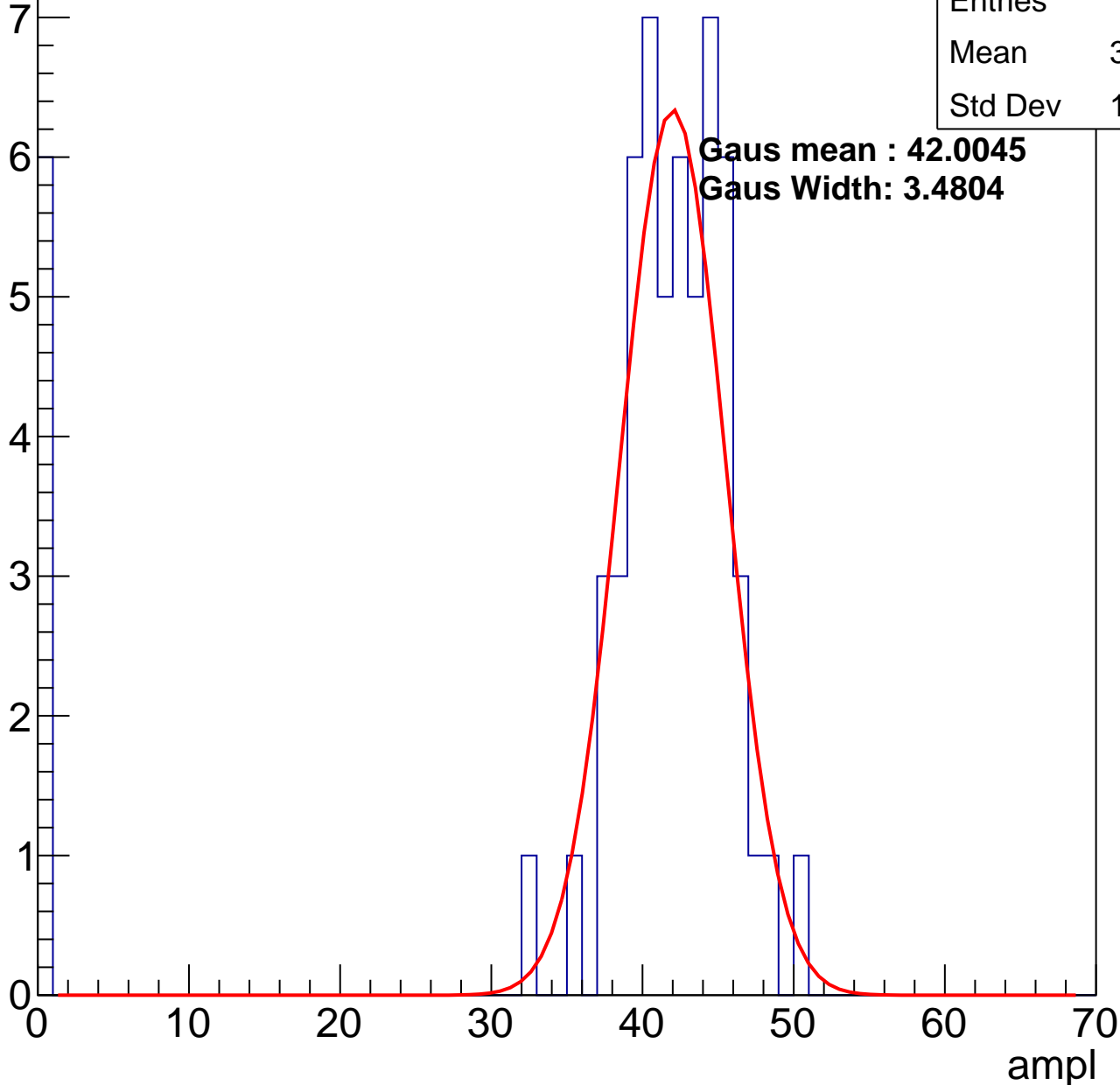
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	62
Mean	37.73
Std Dev	12.74

**Gaus mean : 42.0045**

**Gaus Width: 3.4804**

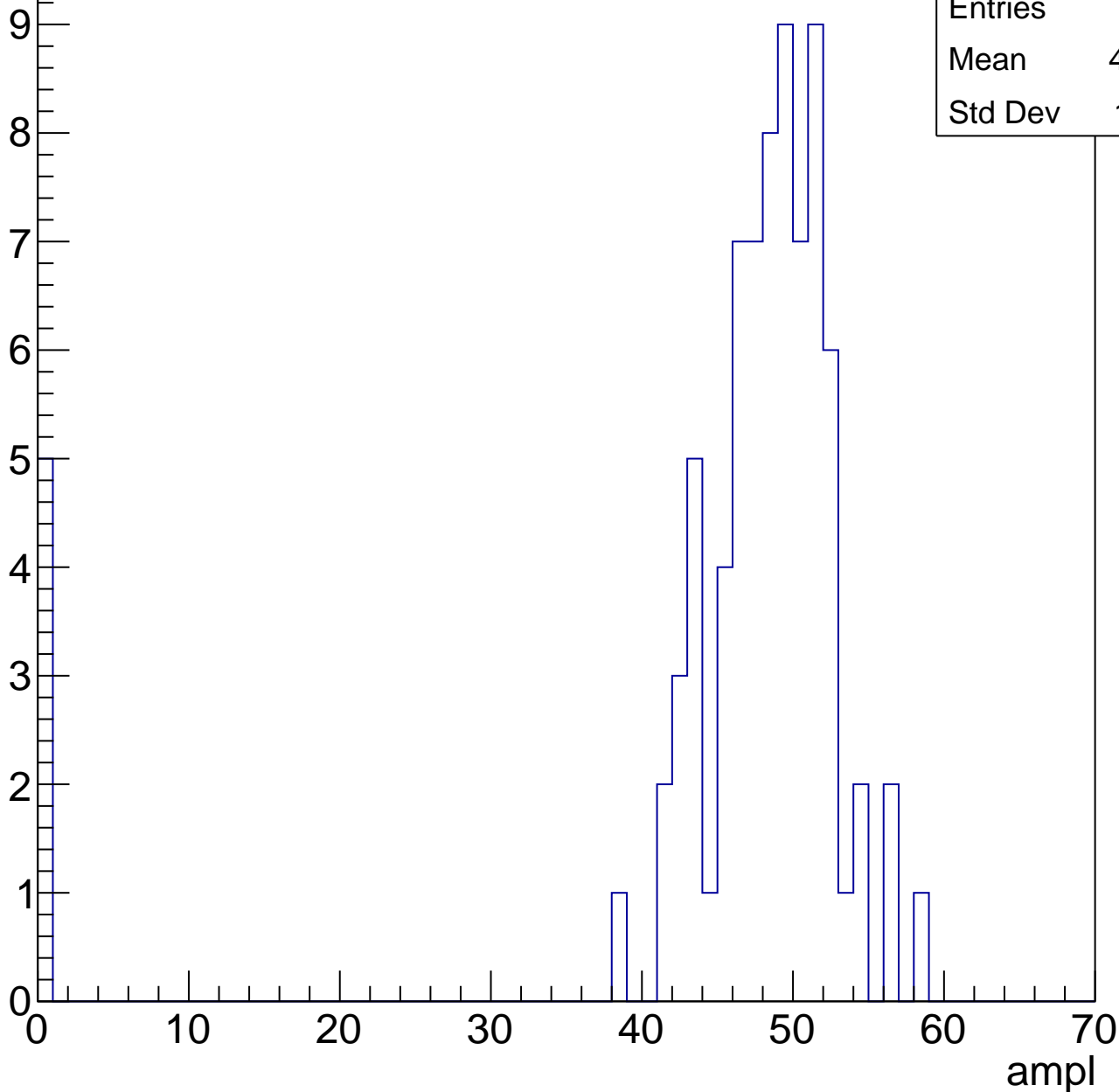


# B1L103S, U26-ch74, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

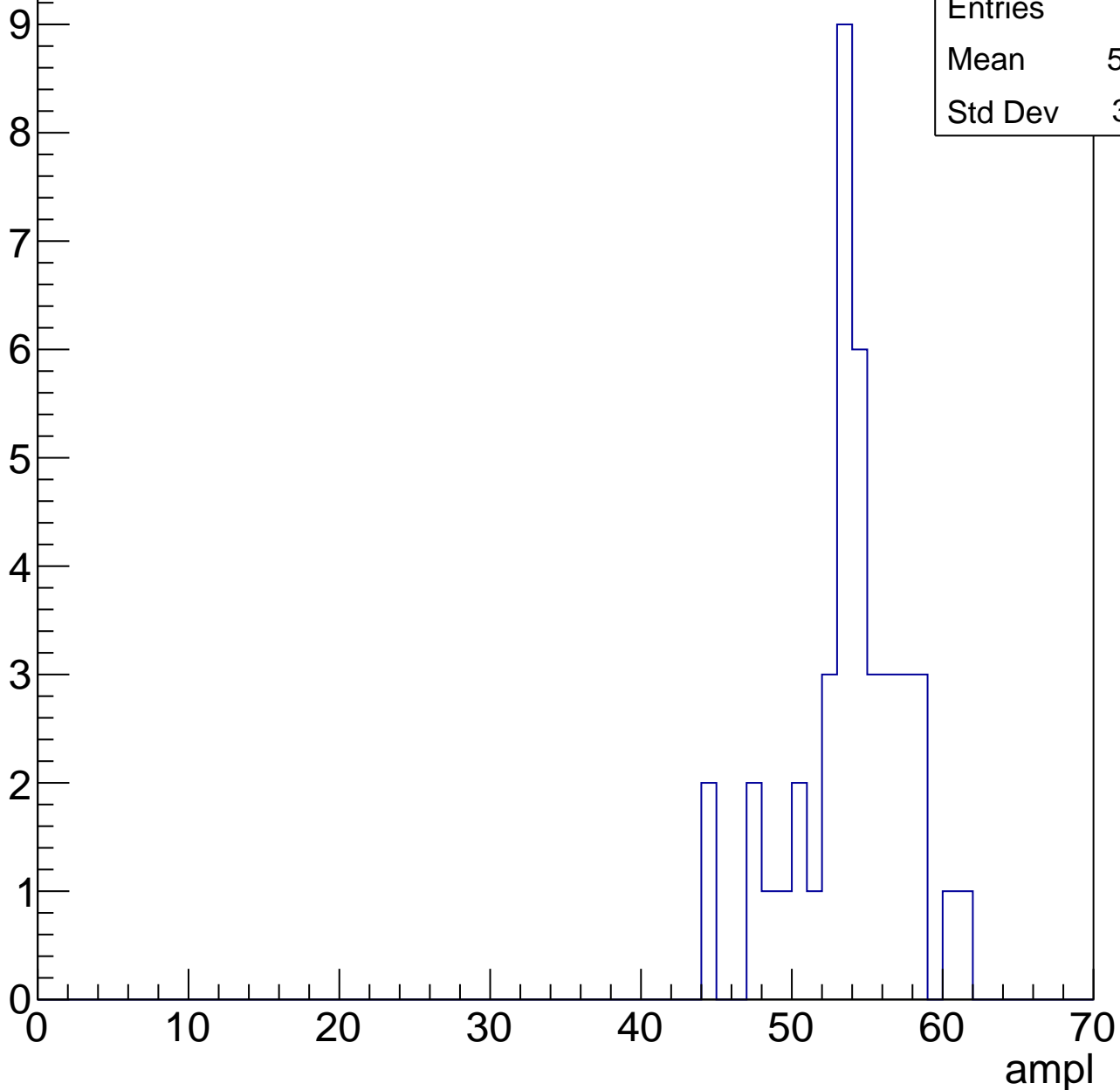
Entries	80
Mean	45.16
Std Dev	12.21



# B1L103S, U26-ch74, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

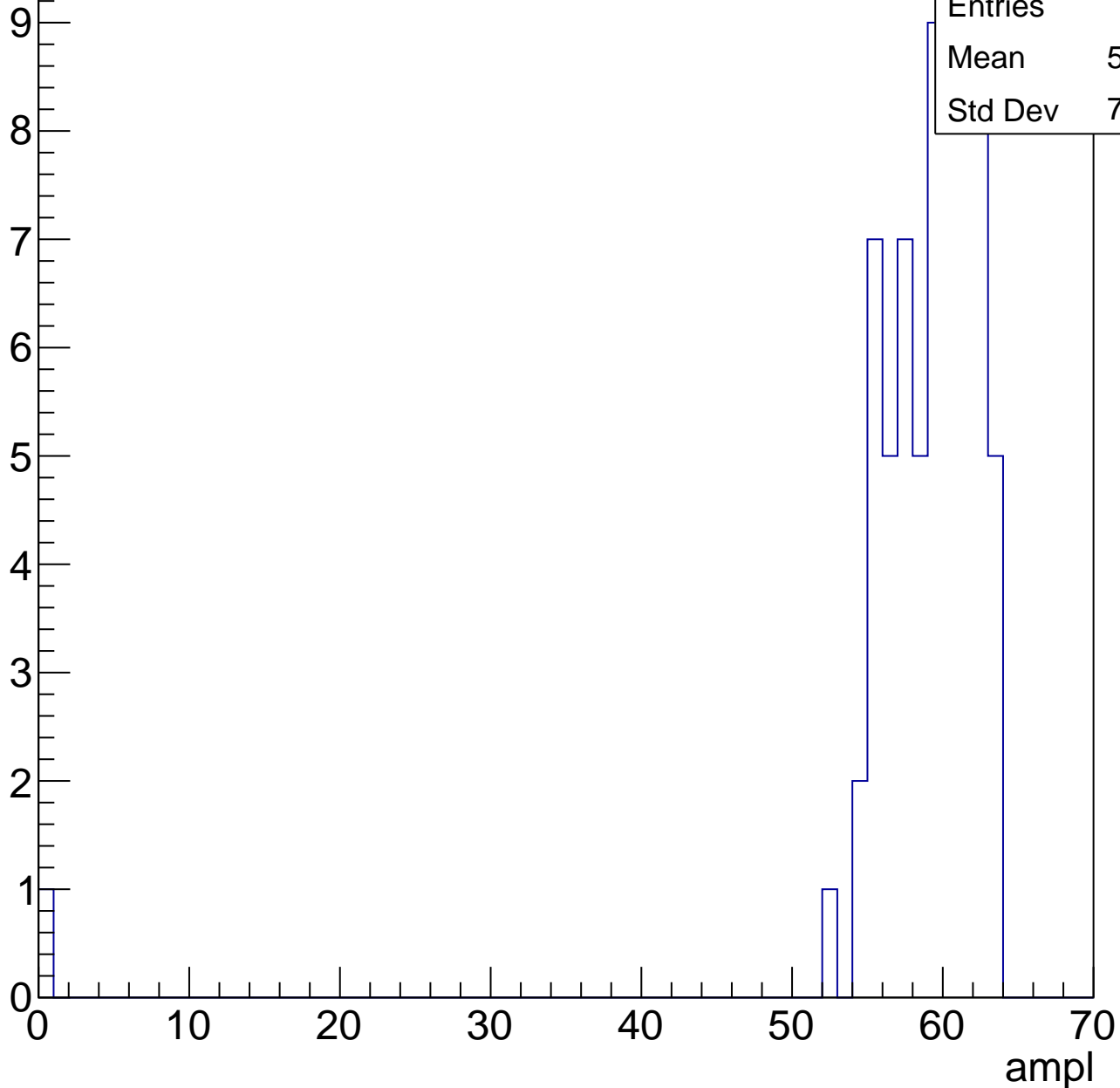


# B1L103S, U26-ch74, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	68
Mean	58.04
Std Dev	7.586

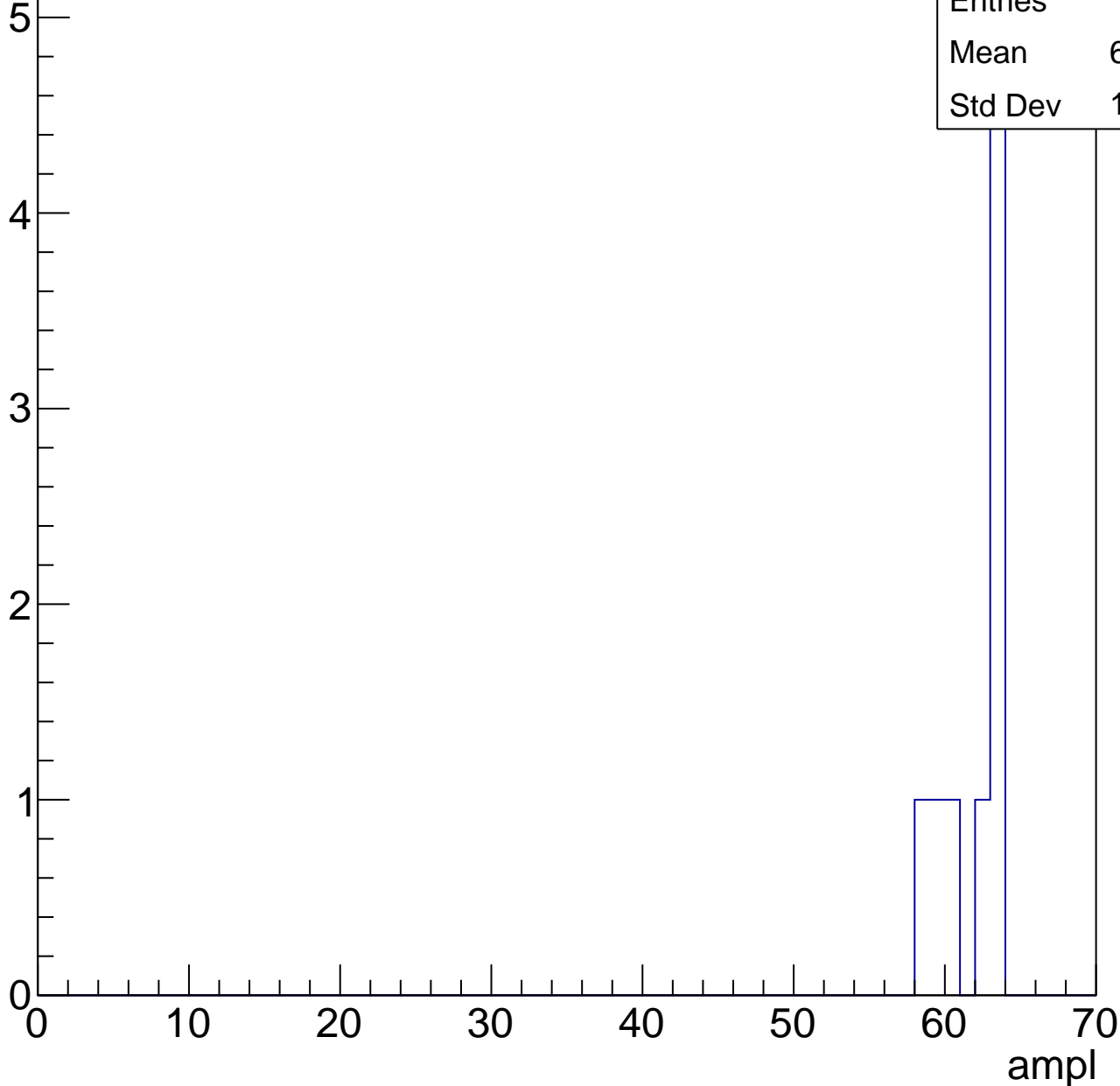


# B1L103S, U26-ch74, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	9
Mean	61.56
Std Dev	1.892





# B1L103S, U26-ch74, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

18  
16  
14  
12  
10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

Entries	19
Mean	0
Std Dev	0

# B1L103S, U26-ch75, adc0

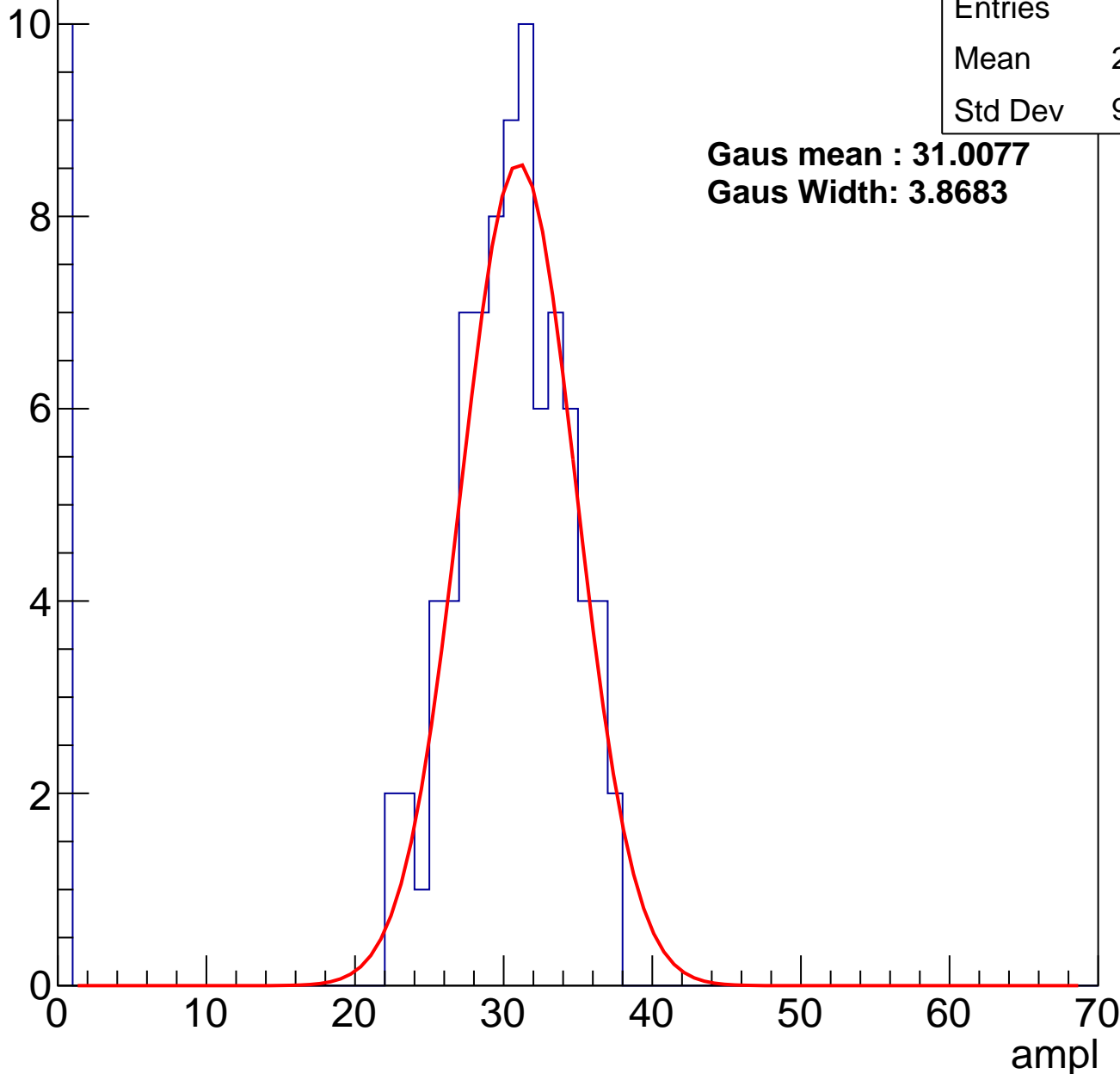
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	93
Mean	26.88
Std Dev	9.922

**Gaus mean : 31.0077**

**Gaus Width: 3.8683**

Entry



# B1L103S, U26-ch75, adc1

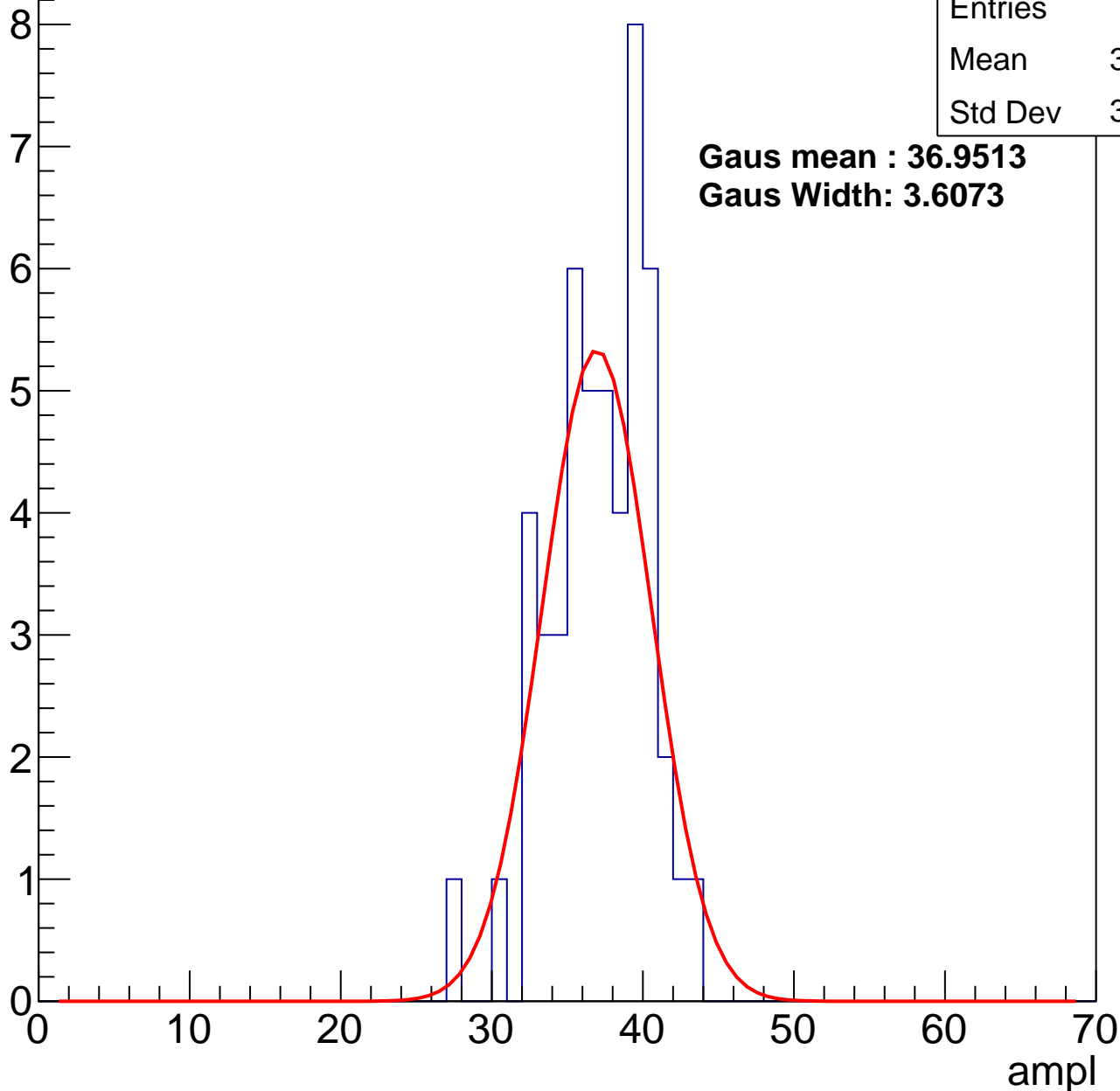
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	50
Mean	36.64
Std Dev	3.254

**Gaus mean : 36.9513**

**Gaus Width: 3.6073**



# B1L103S, U26-ch75, adc2

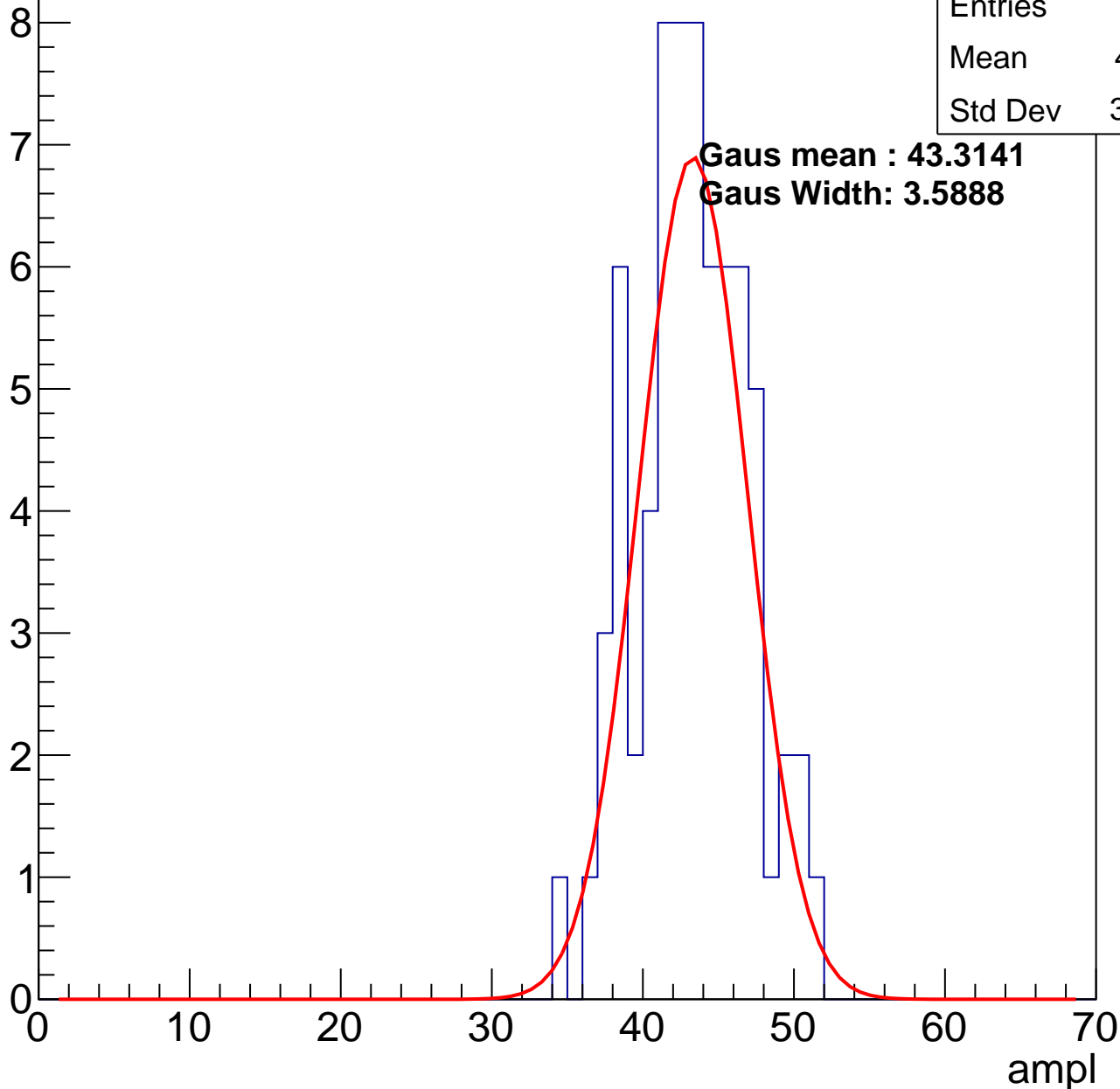
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	70
Mean	42.81
Std Dev	3.619

**Gaus mean : 43.3141**

**Gaus Width: 3.5888**

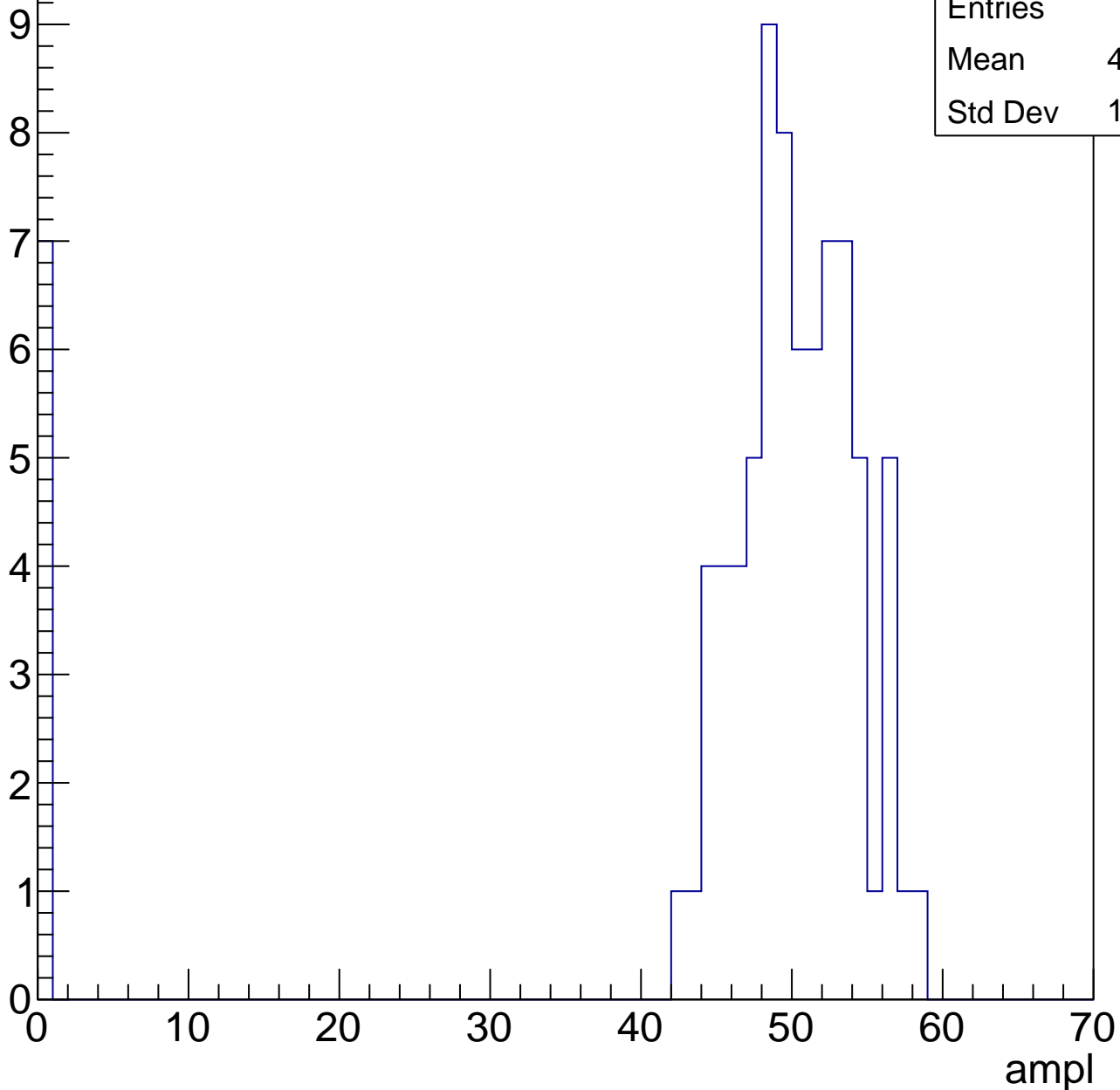


# B1L103S, U26-ch75, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

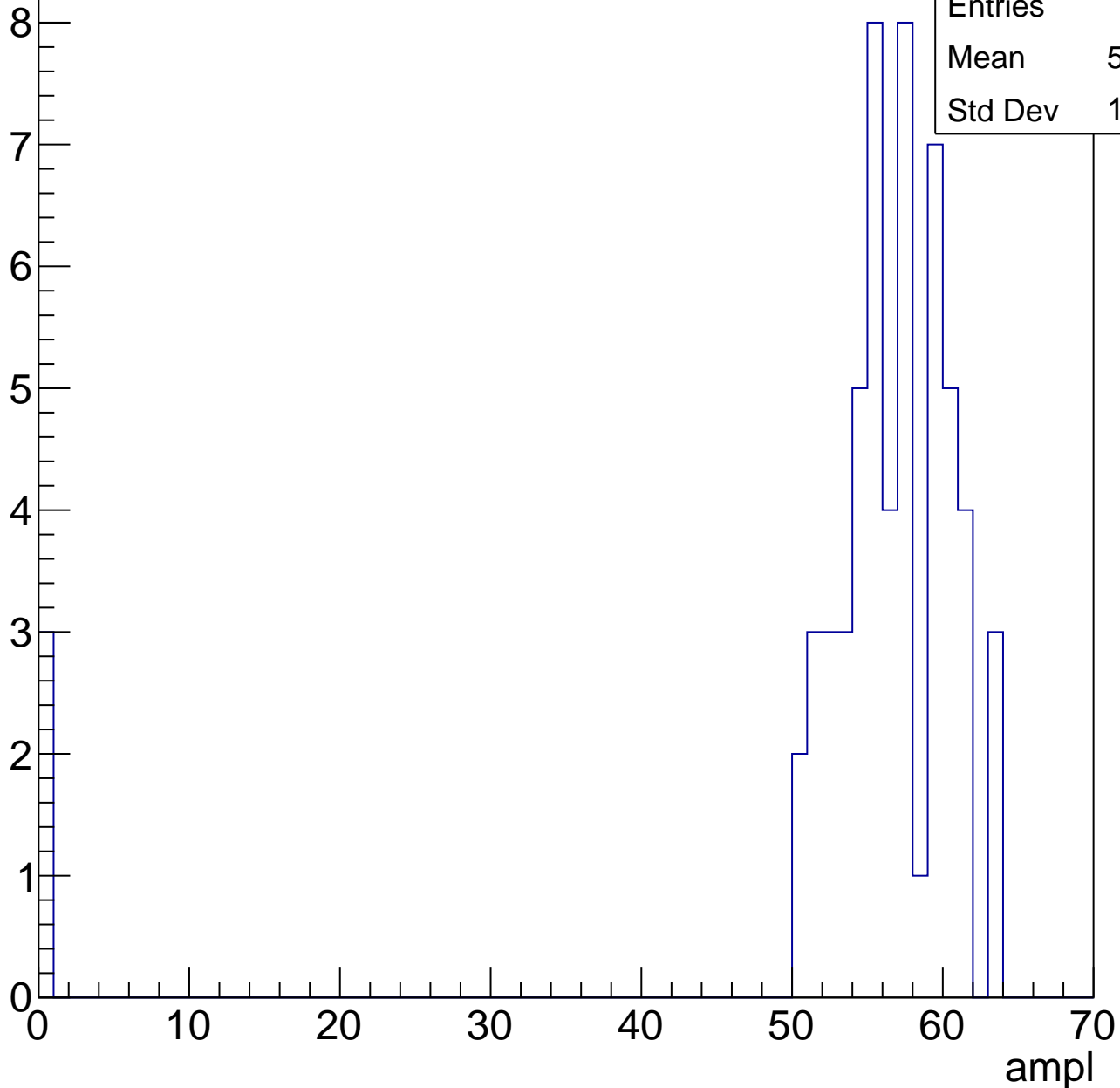
Entries	82
Mean	45.67
Std Dev	14.38



# B1L103S, U26-ch75, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

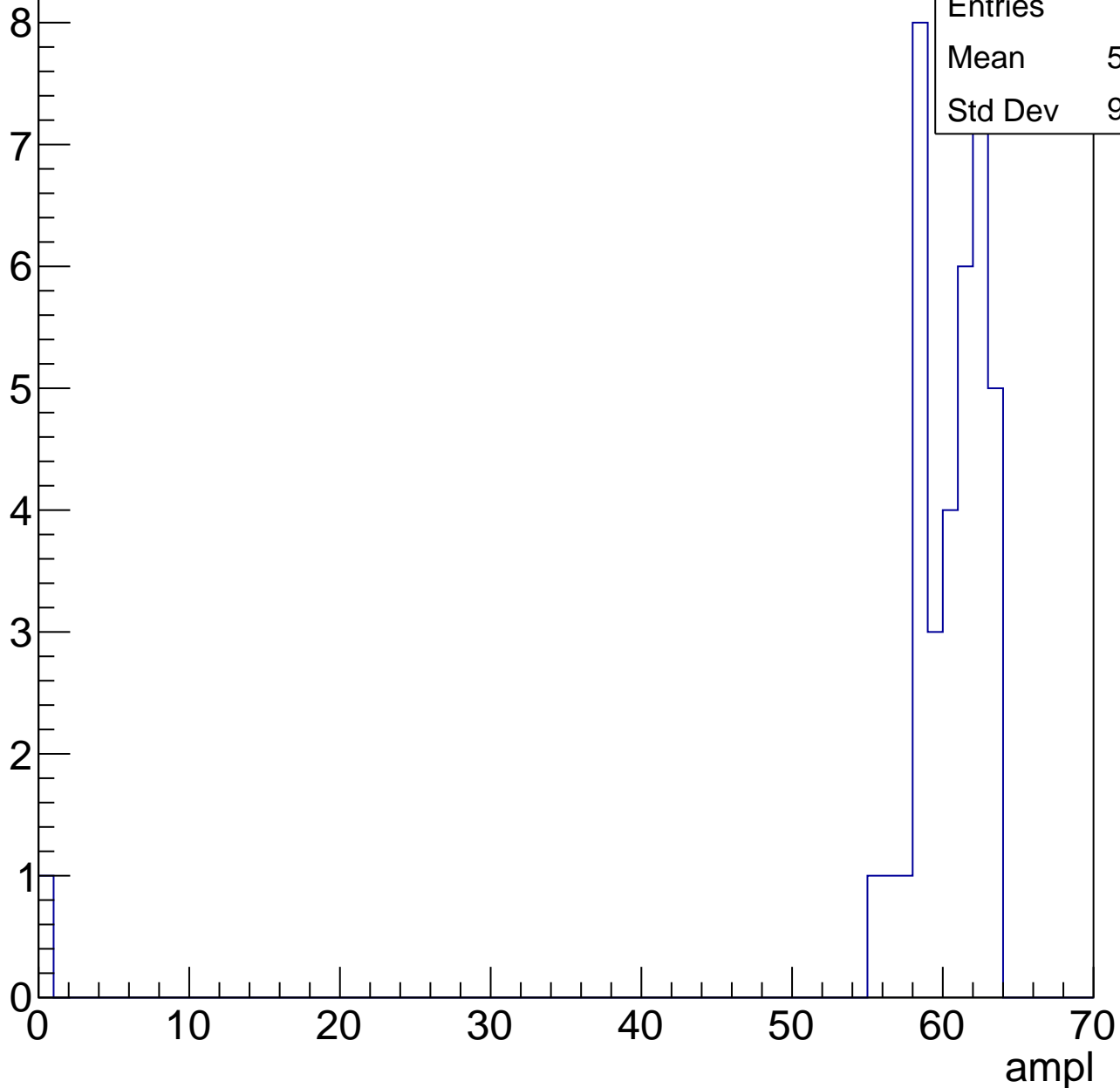
Entry



# B1L103S, U26-ch75, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



# B1L103S, U26-ch75, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



Entries	5
Mean	62
Std Dev	1.095



# B1L103S, U26-ch75, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	19
Mean	1.158
Std Dev	4.913

Entry



# B1L103S, U26-ch76, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	91
Mean	22.35
Std Dev	10.82

**Gaus mean : 27.5706**

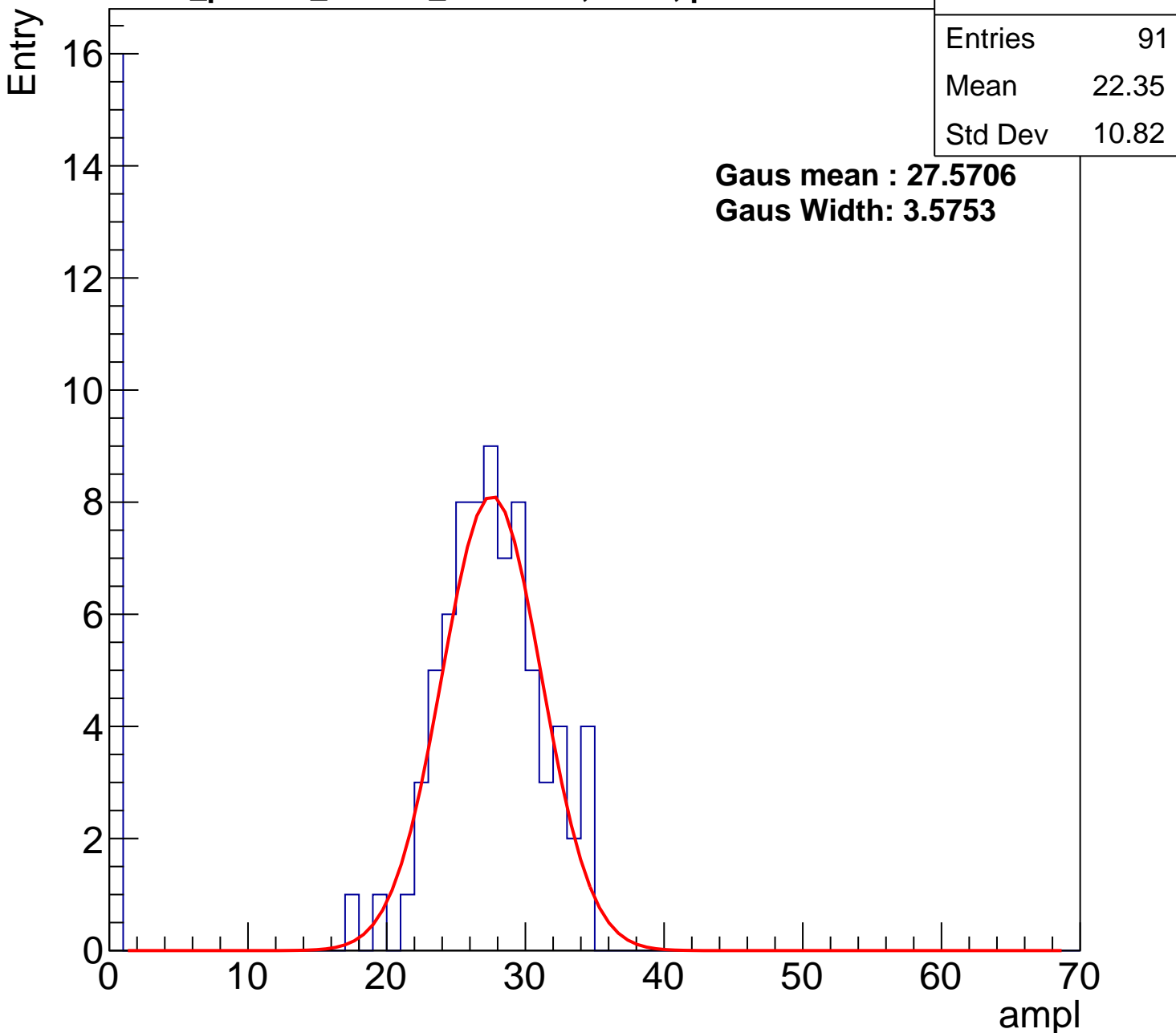
**Gaus Width: 3.5753**

Entry

16  
14  
12  
10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U26-ch76, adc1

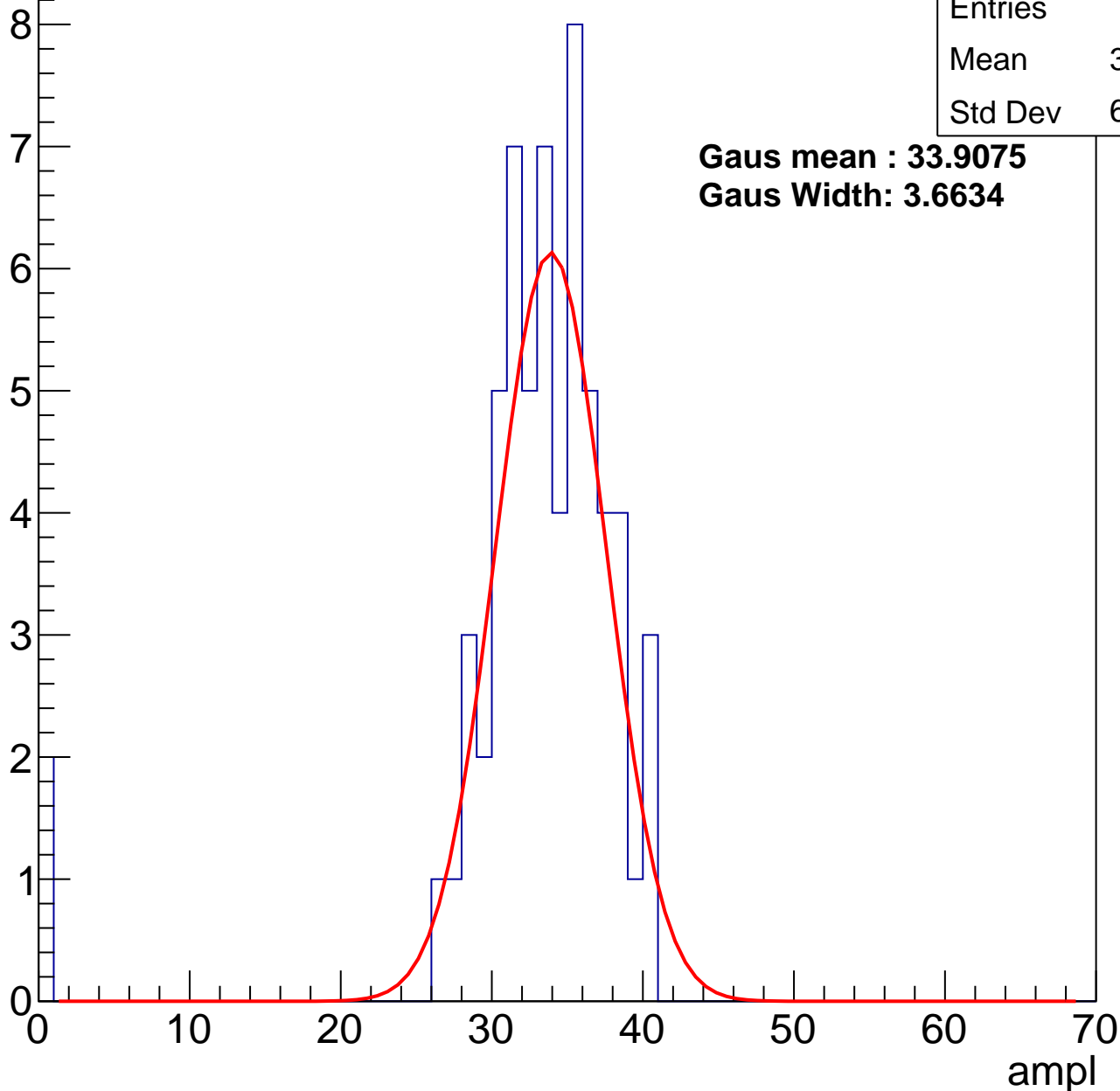
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	62
Mean	32.39
Std Dev	6.783

**Gaus mean : 33.9075**

**Gaus Width: 3.6634**



# B1L103S, U26-ch76, adc2

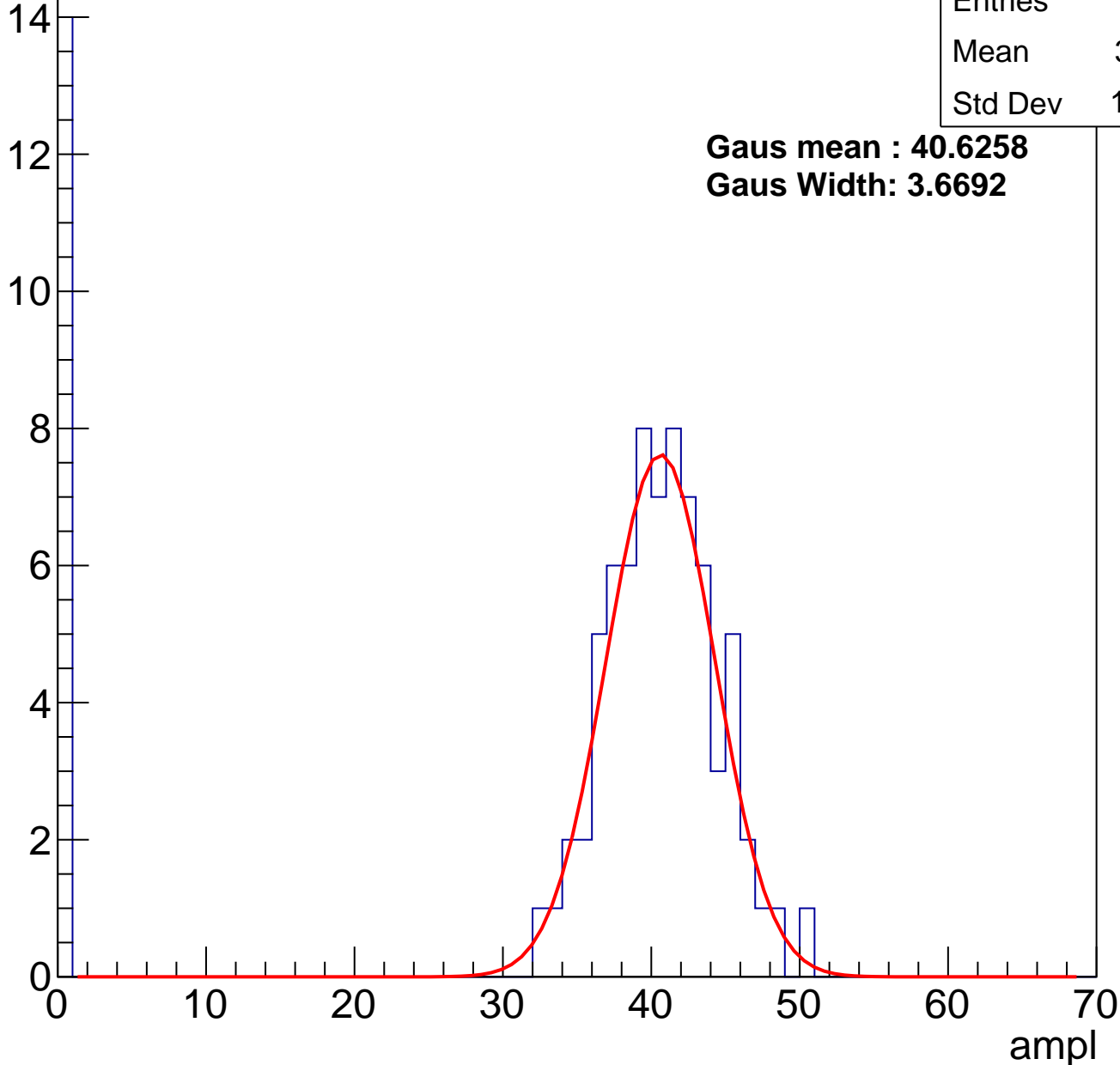
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	86
Mean	33.71
Std Dev	15.23

**Gaus mean : 40.6258**

**Gaus Width: 3.6692**

Entry

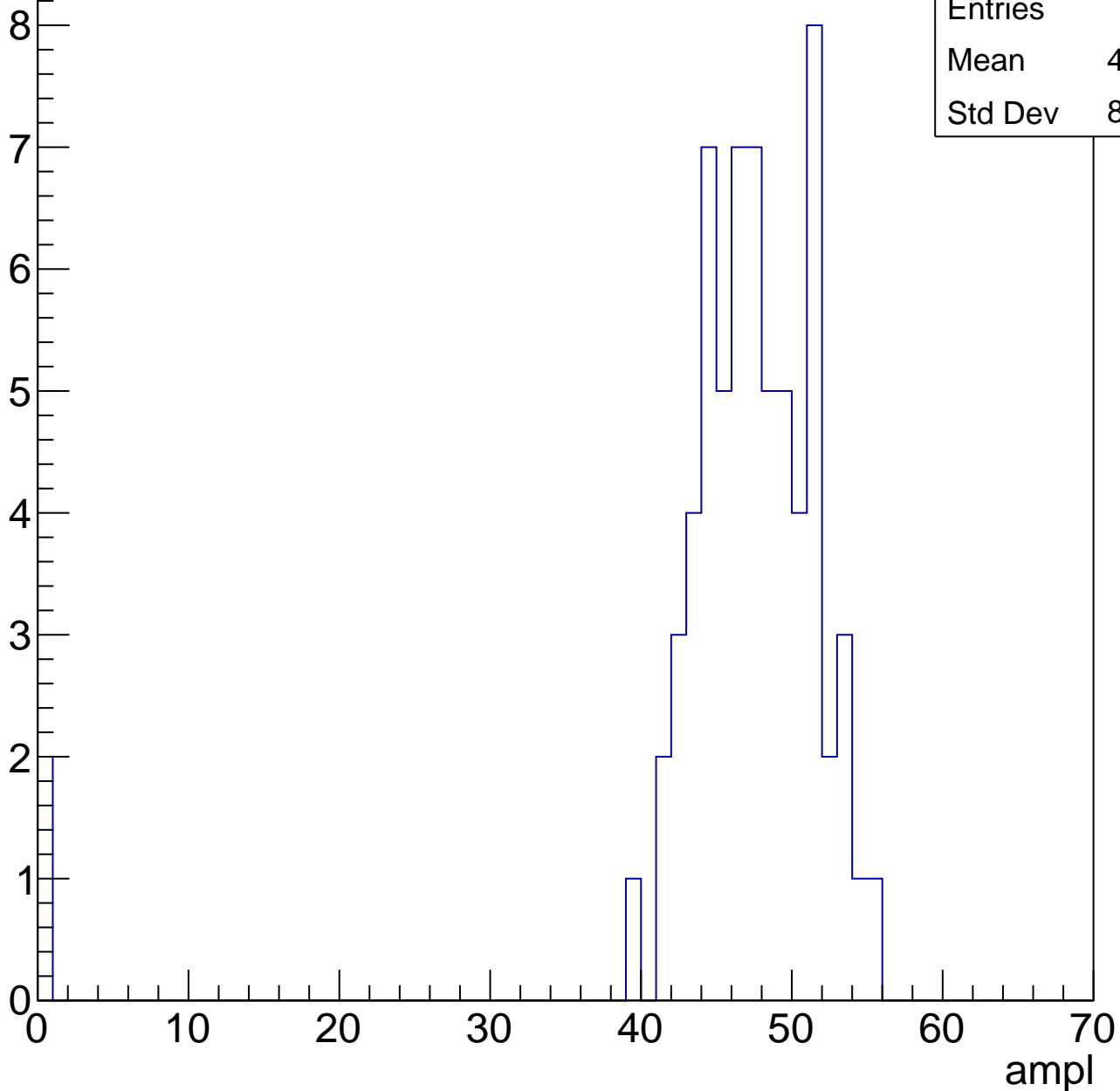


# B1L103S, U26-ch76, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	67
Mean	45.79
Std Dev	8.763

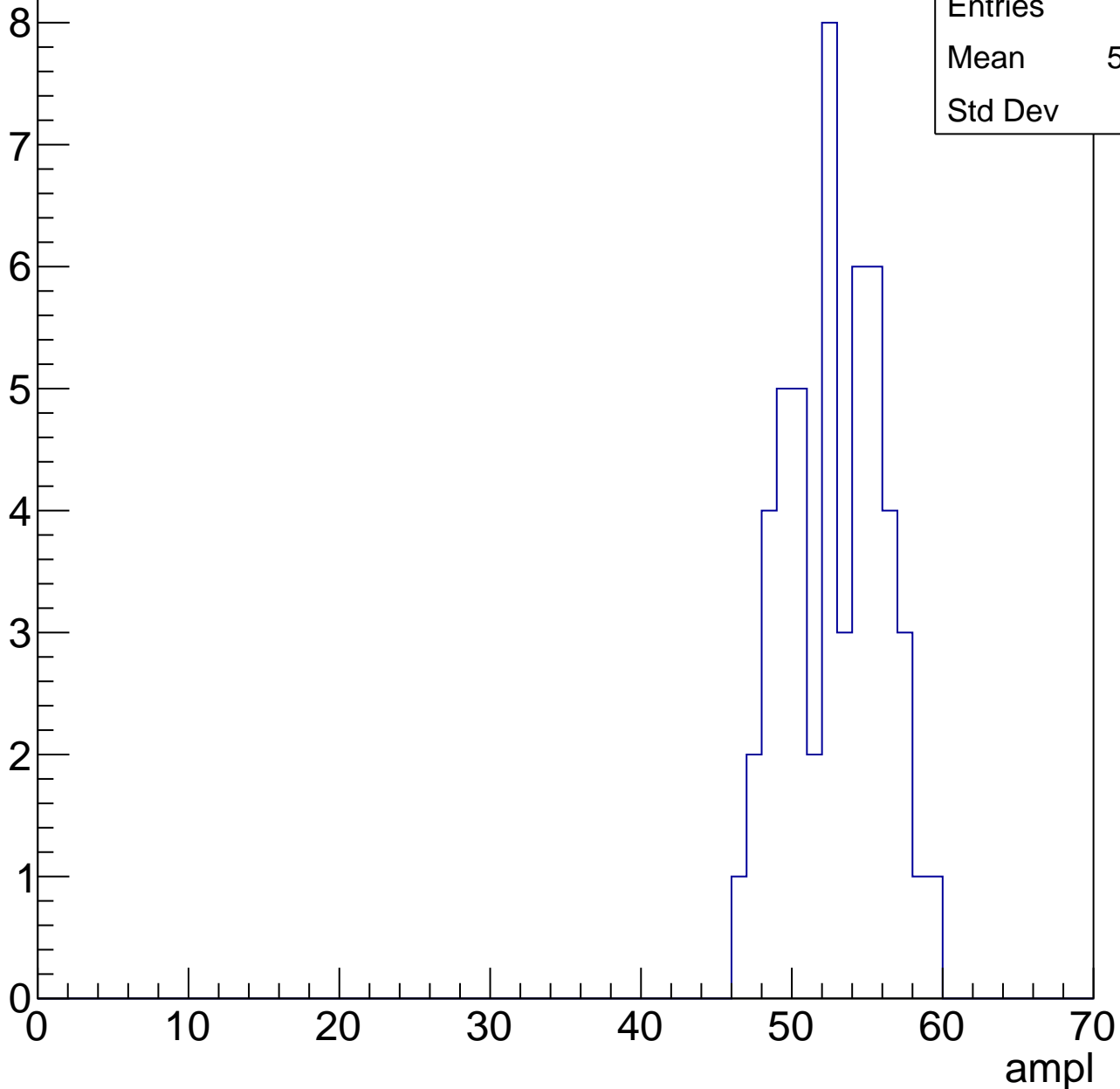


# B1L103S, U26-ch76, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

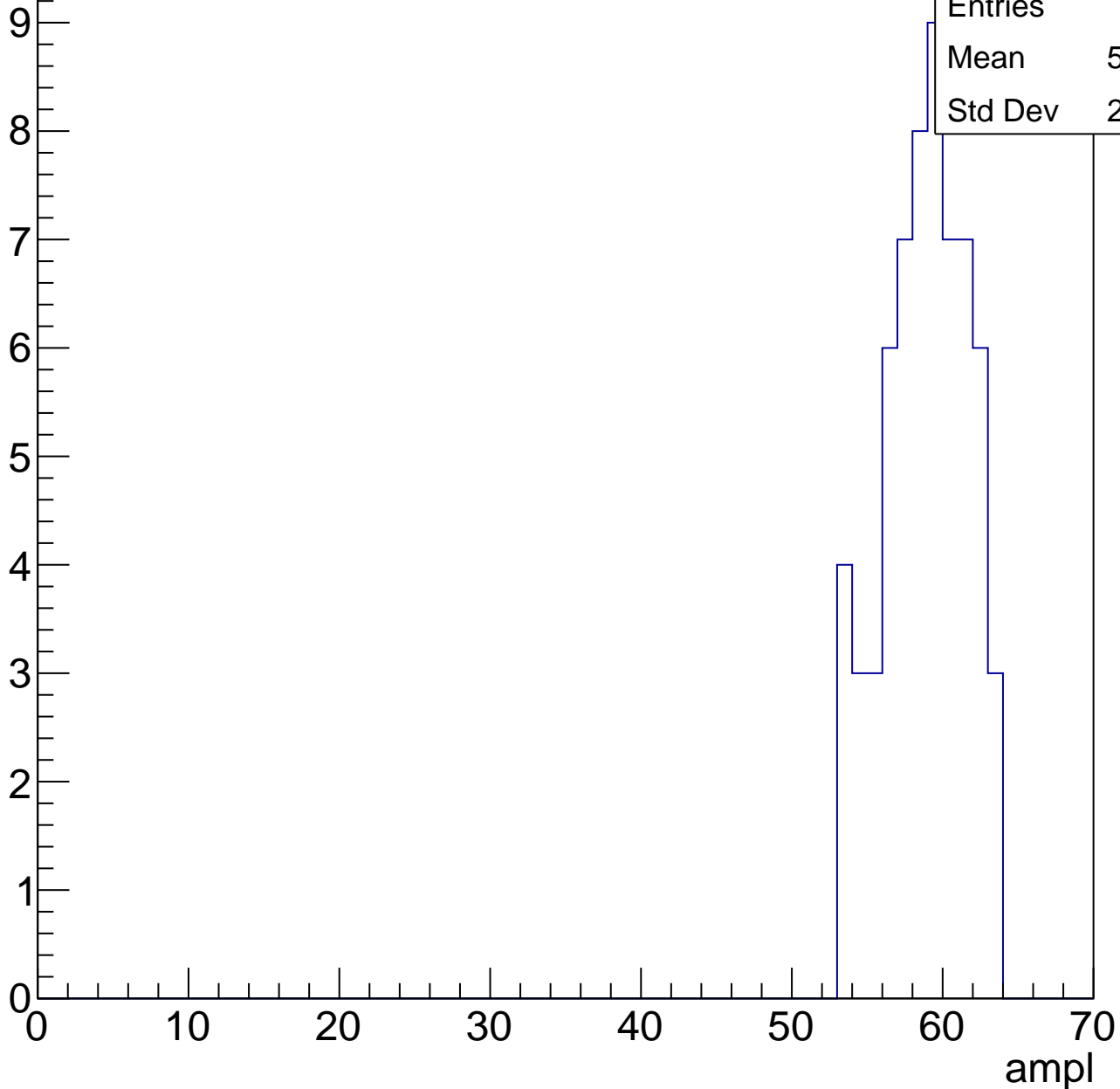
Entries	51
Mean	52.35
Std Dev	3.18



# B1L103S, U26-ch76, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

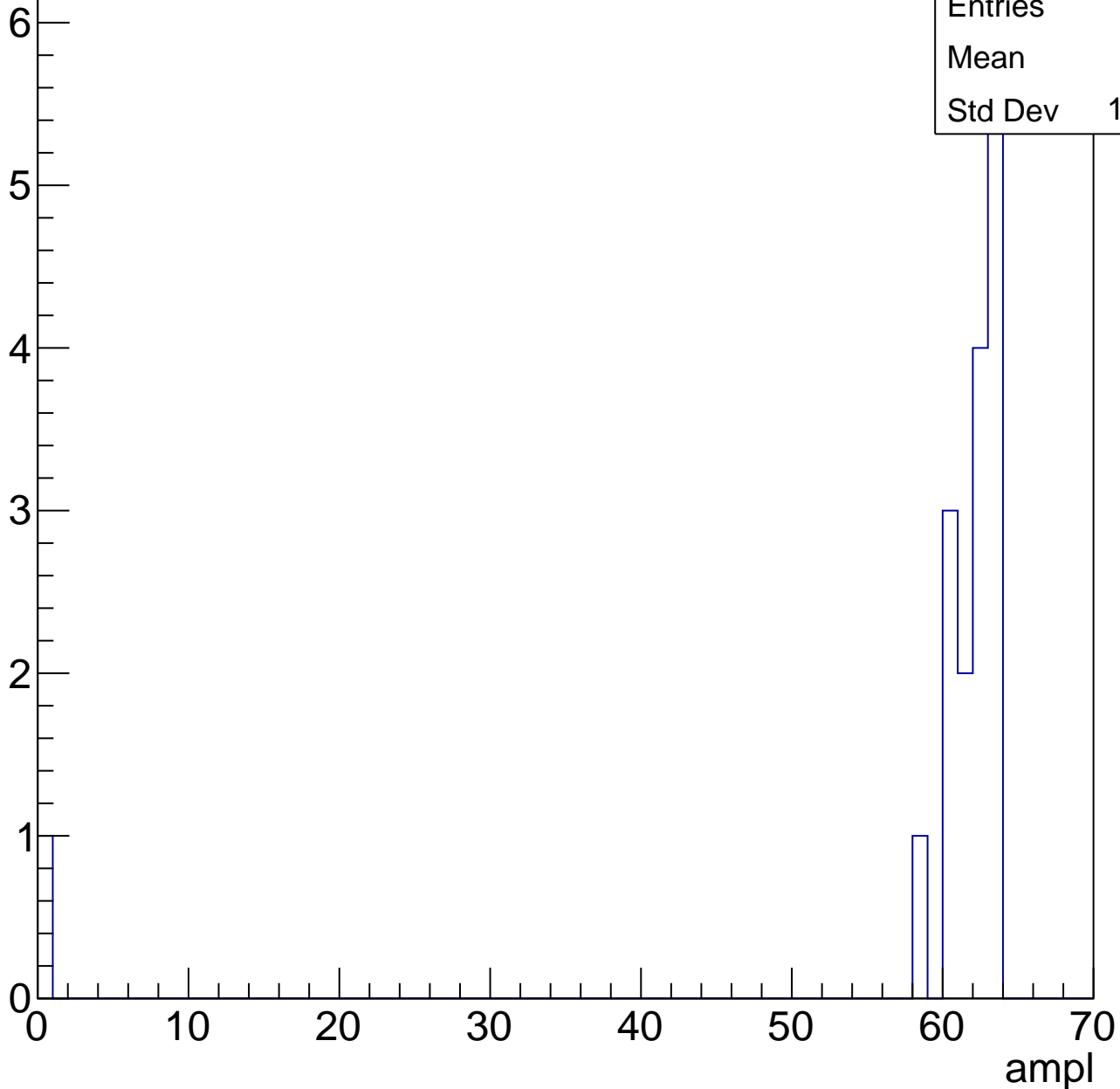


# B1L103S, U26-ch76, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	17
Mean	58
Std Dev	14.57





# B1L103S, U26-ch76, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	21
Mean	5.905
Std Dev	18.2

Entry



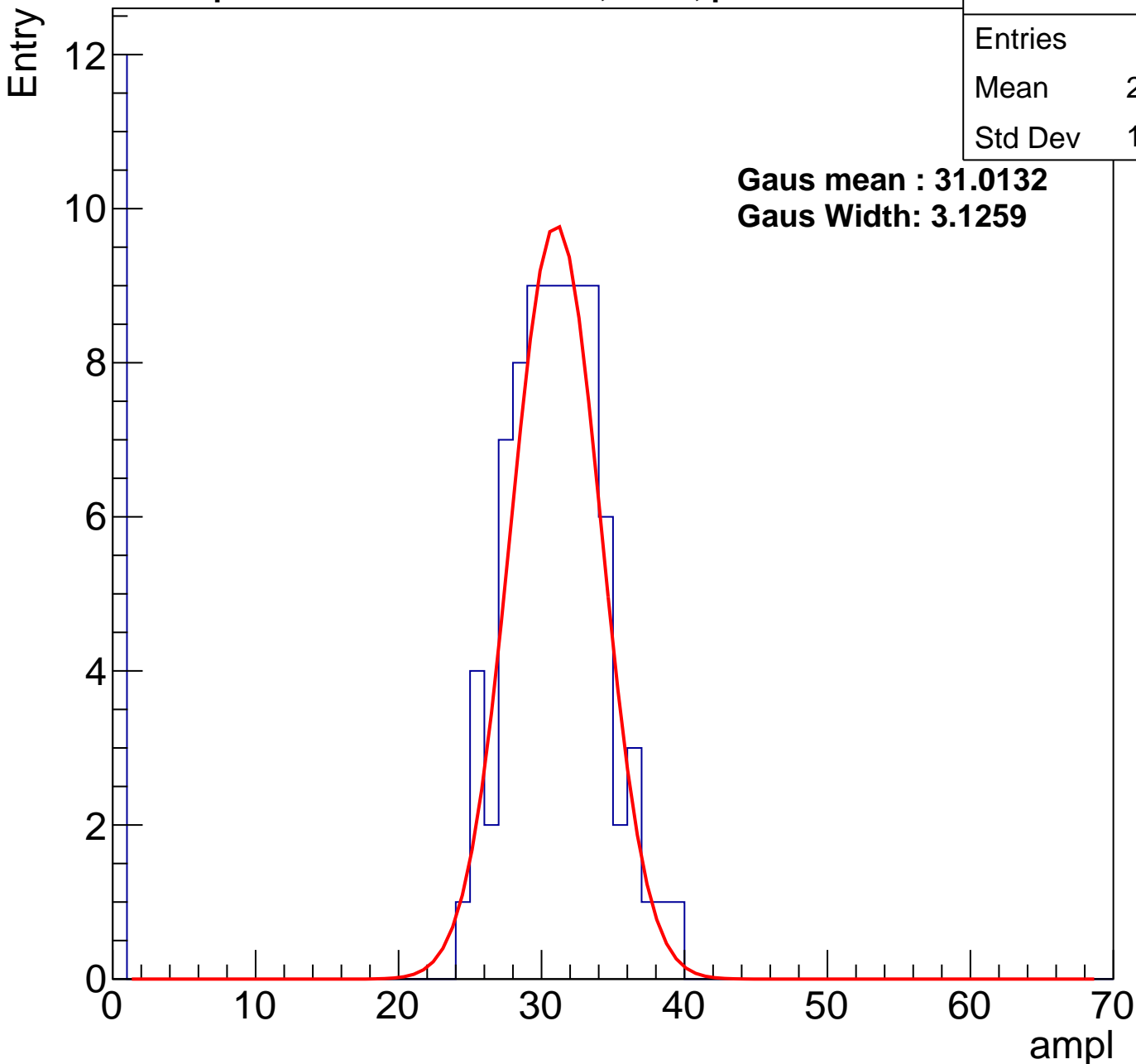
# B1L103S, U26-ch77, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	93
Mean	26.67
Std Dev	10.68

**Gaus mean : 31.0132**

**Gaus Width: 3.1259**



# B1L103S, U26-ch77, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	83
Mean	33.18
Std Dev	13.26

**Gaus mean : 38.8587**

**Gaus Width: 3.0917**

Entry

10

8

6

4

2

0

0

10

20

30

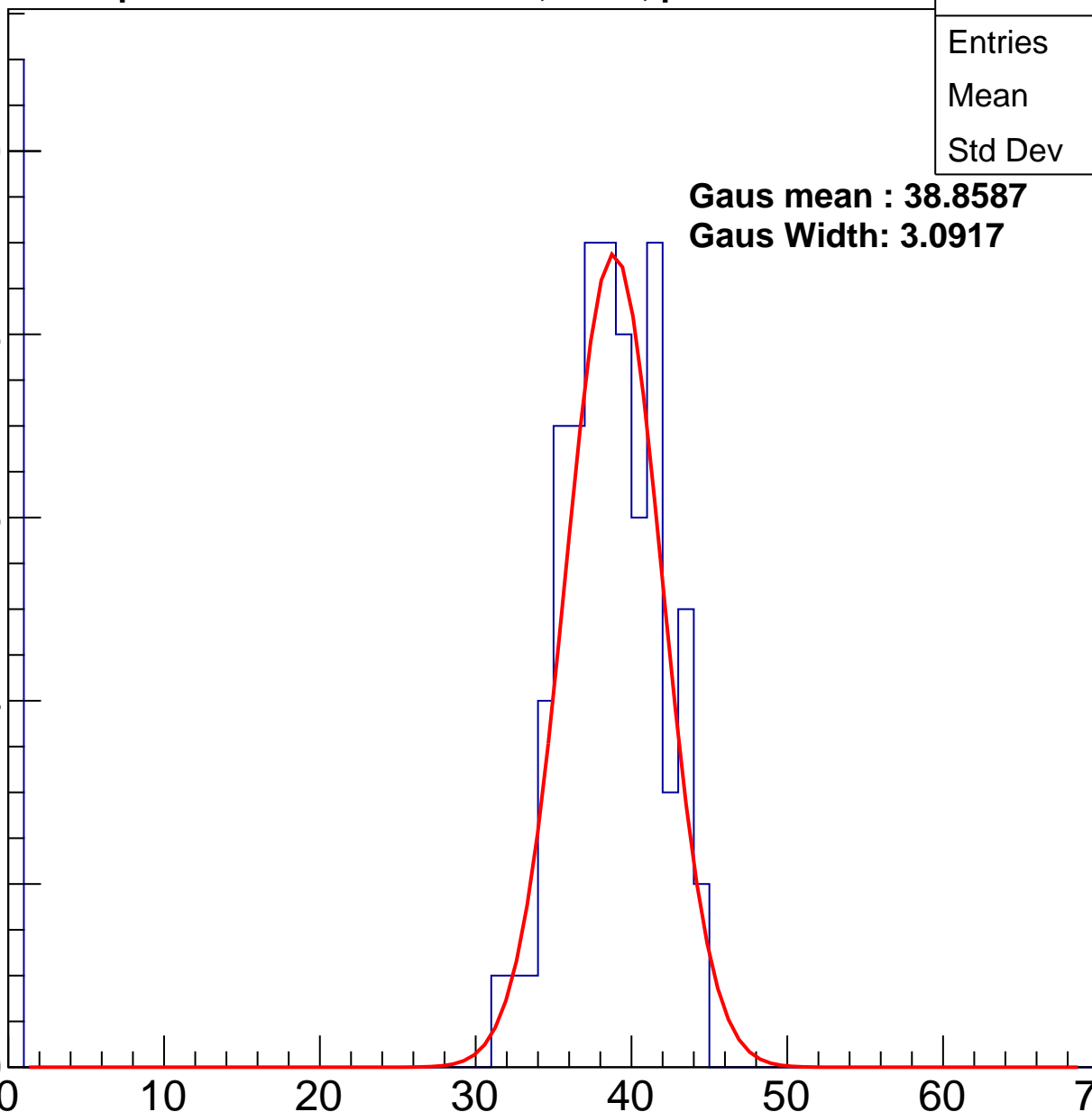
40

50

60

70

ampl



# B1L103S, U26-ch77, adc2

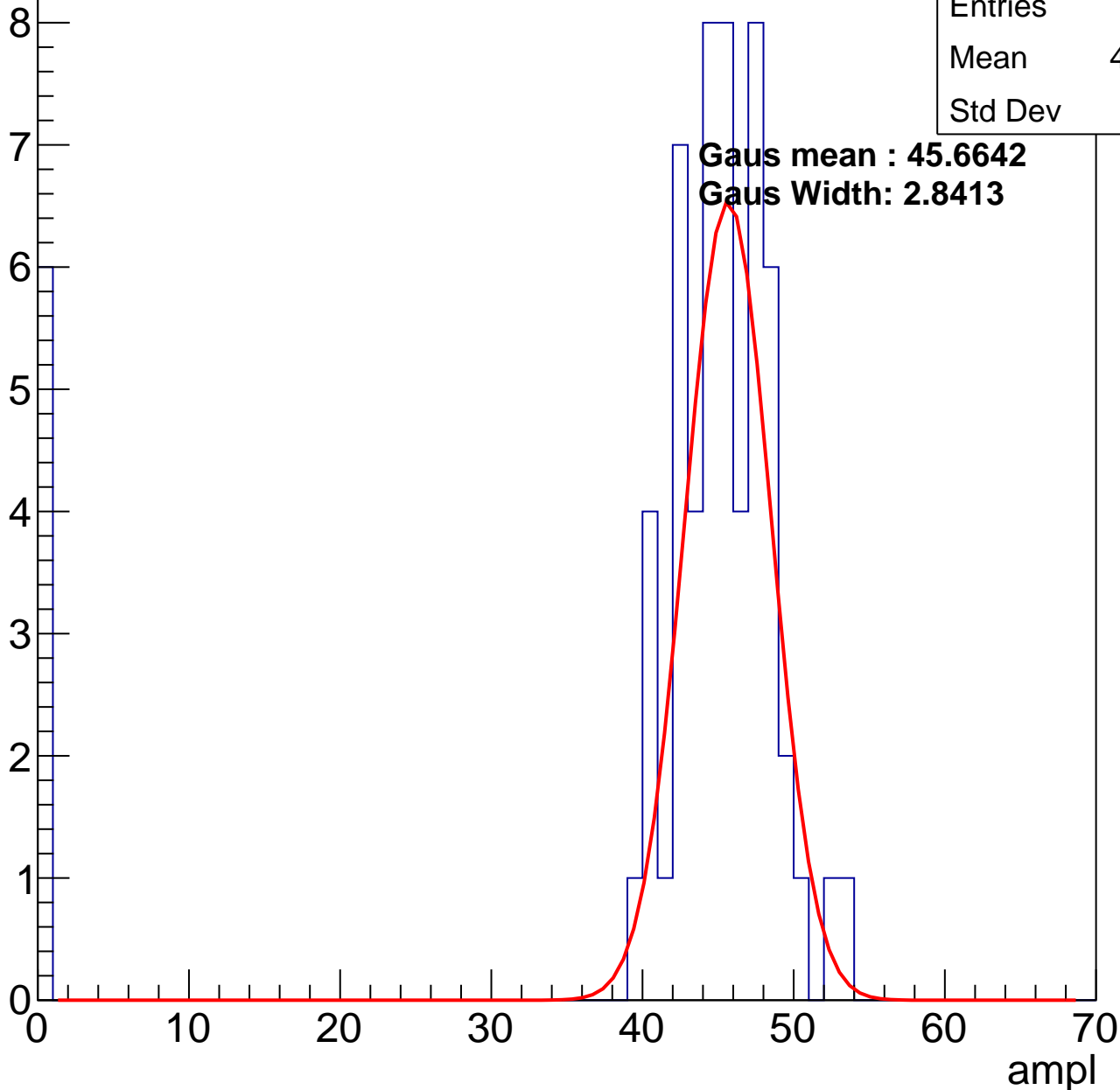
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	62
Mean	40.63
Std Dev	13.6

**Gaus mean : 45.6642**

**Gaus Width: 2.8413**

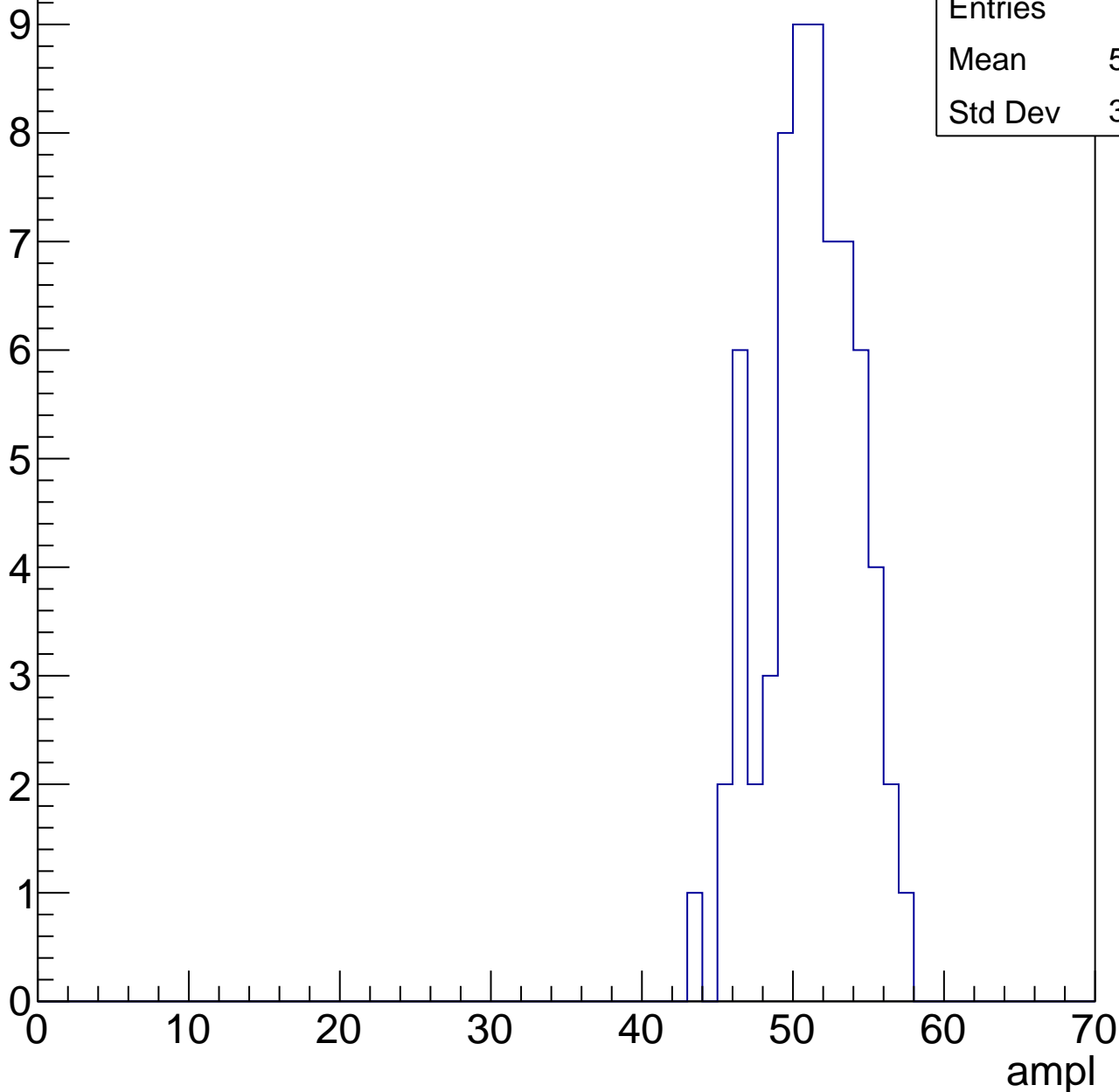


# B1L103S, U26-ch77, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	67
Mean	50.69
Std Dev	3.038

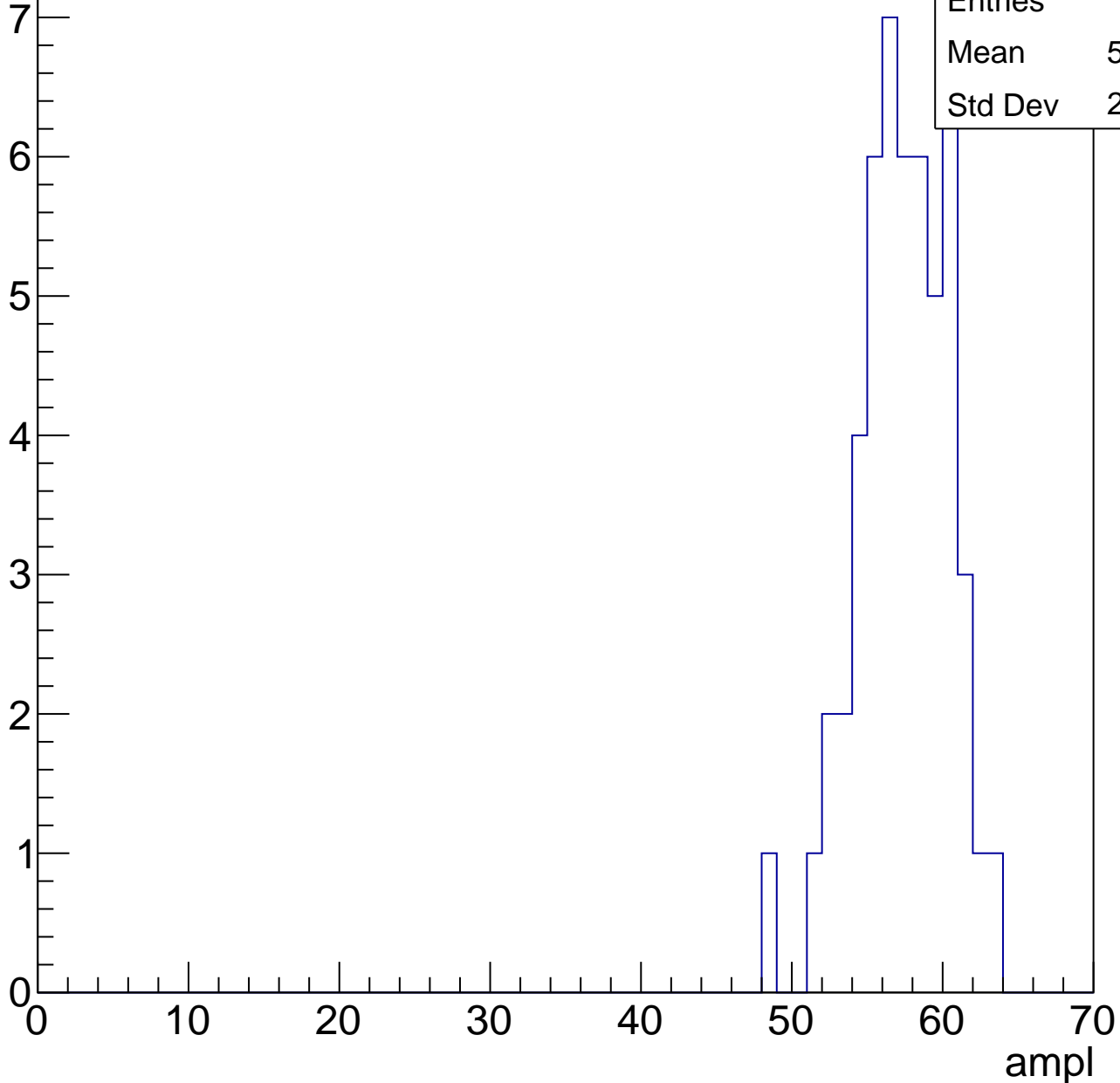


# B1L103S, U26-ch77, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	52
Mean	56.92
Std Dev	2.986

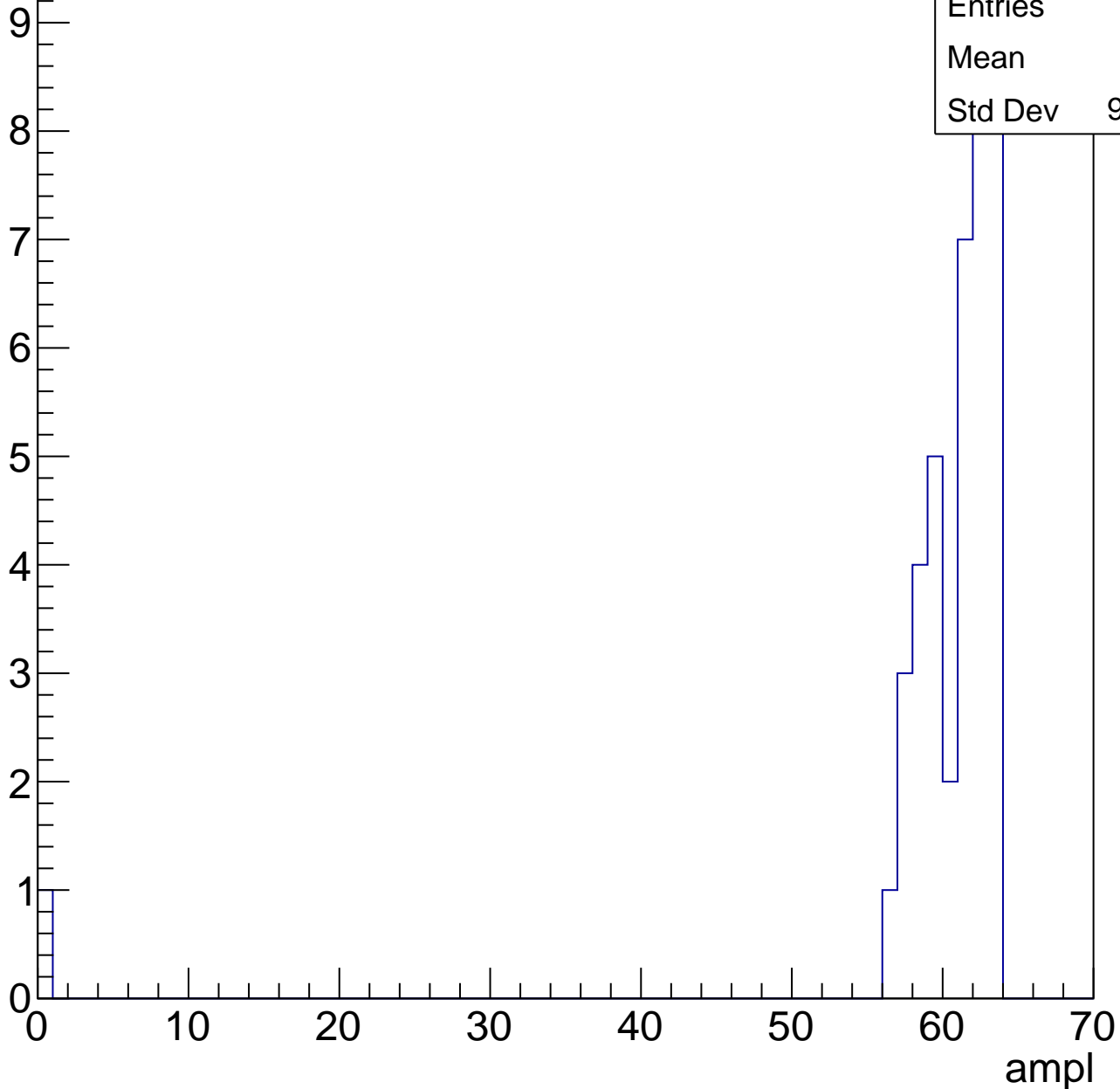


# B1L103S, U26-ch77, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

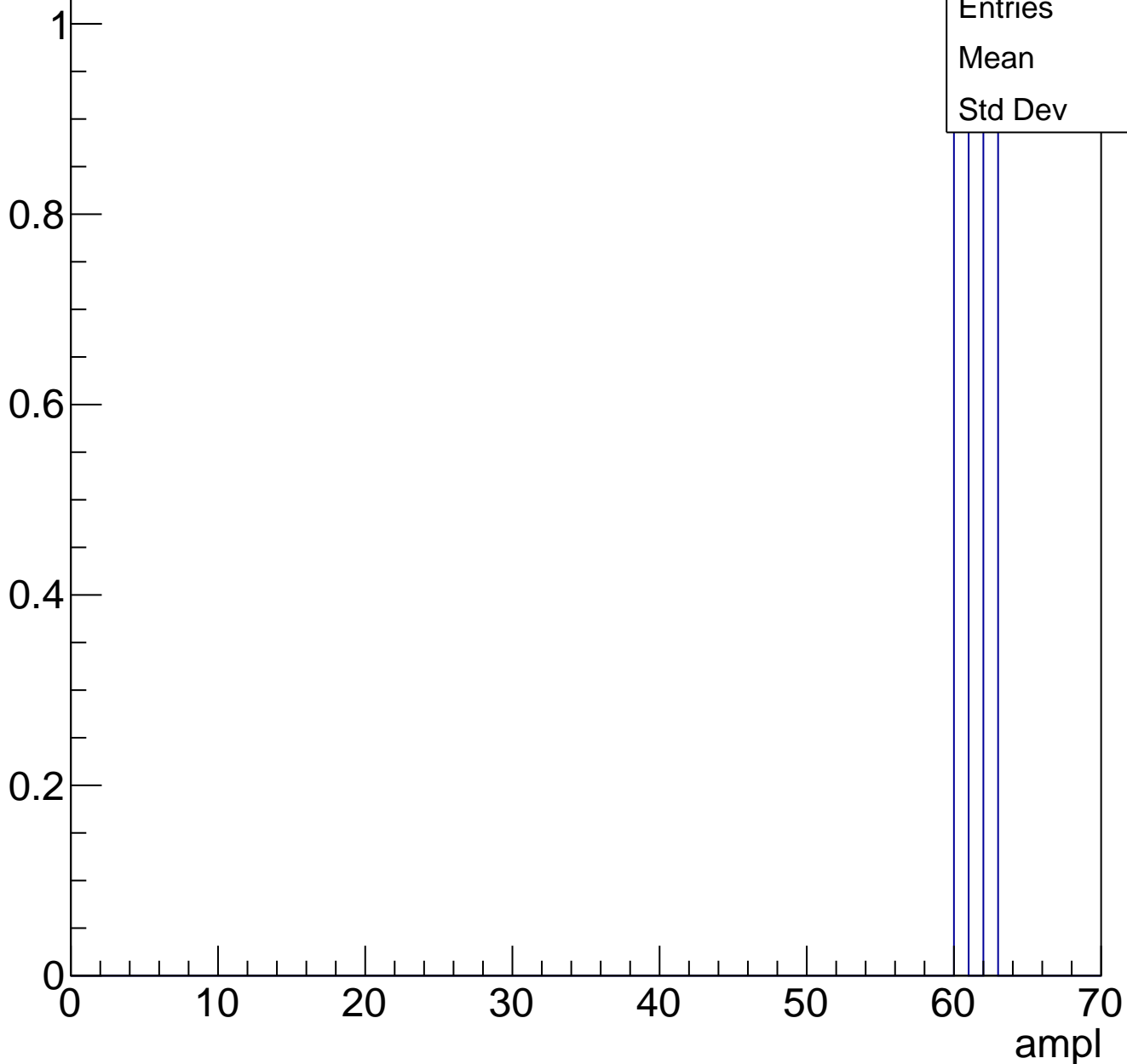
Entries	40
Mean	59.1
Std Dev	9.685



# B1L103S, U26-ch77, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



Entries	2
Mean	61
Std Dev	1



# B1L103S, U26-ch77, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

18  
16  
14  
12  
10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

Entries	19
Mean	0
Std Dev	0

# B1L103S, U26-ch78, adc0

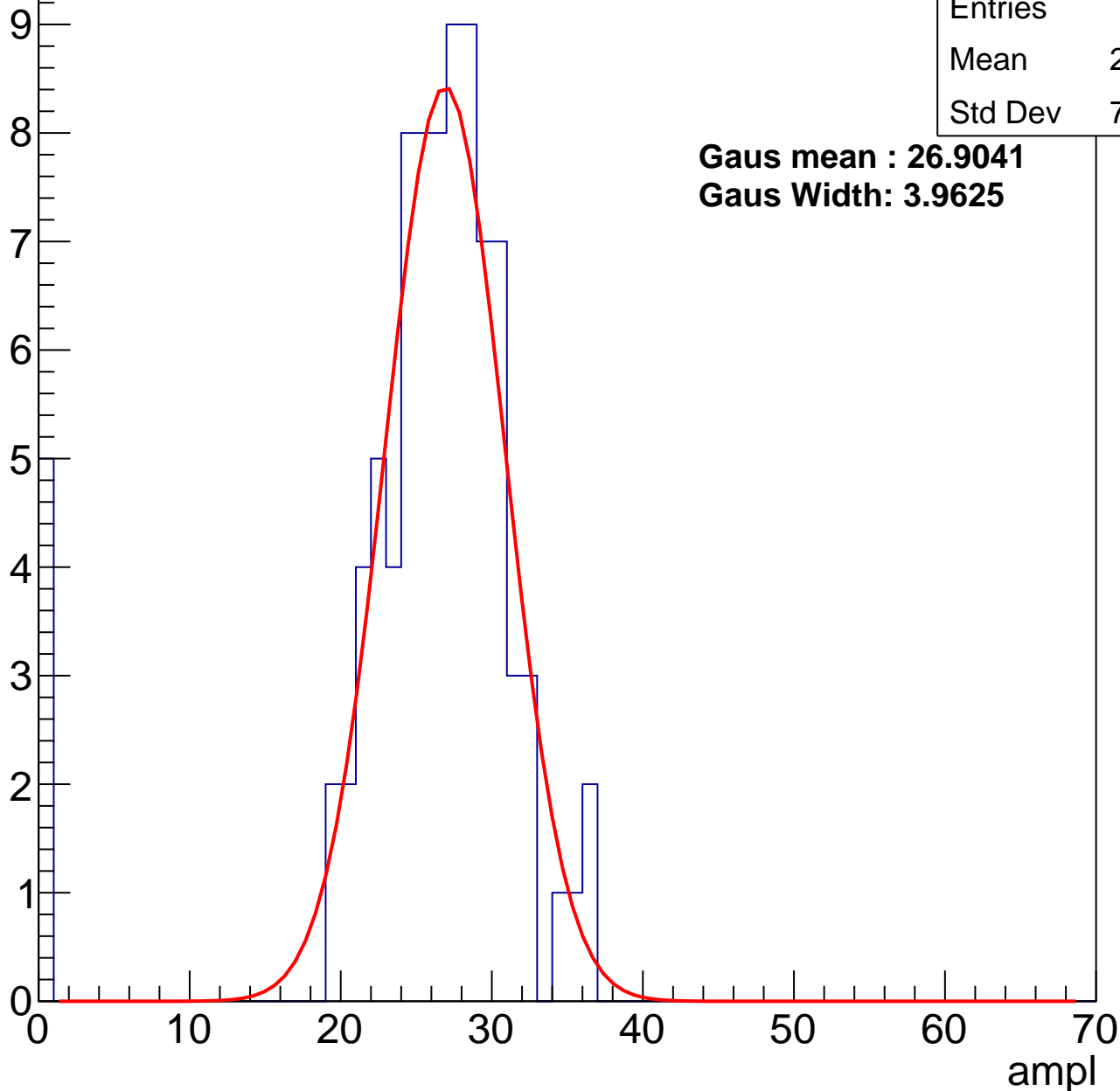
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	88
Mean	25.02
Std Dev	7.127

**Gaus mean : 26.9041**

**Gaus Width: 3.9625**



# B1L103S, U26-ch78, adc1

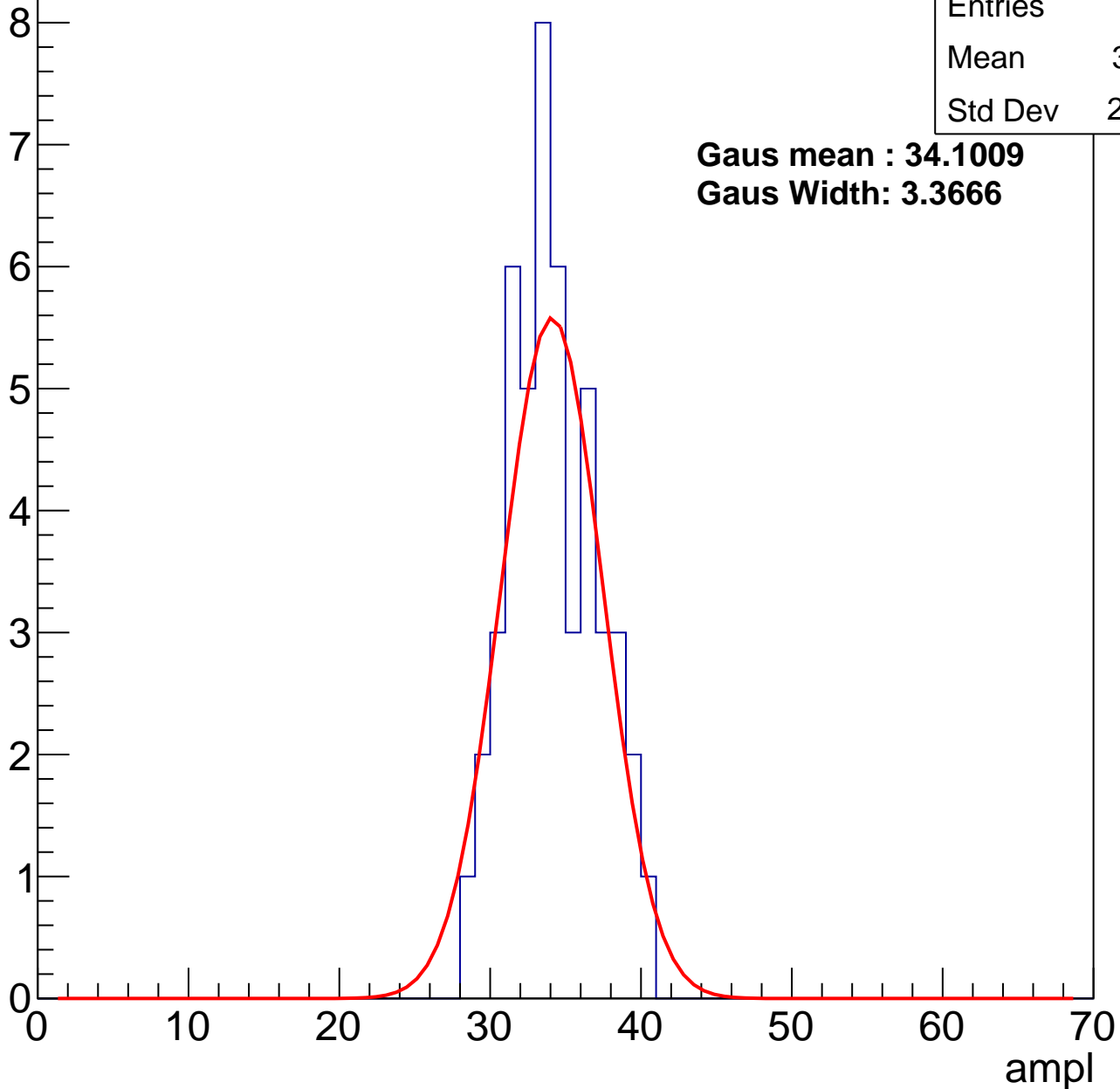
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	48
Mean	33.71
Std Dev	2.872

**Gaus mean : 34.1009**

**Gaus Width: 3.3666**



# B1L103S, U26-ch78, adc2

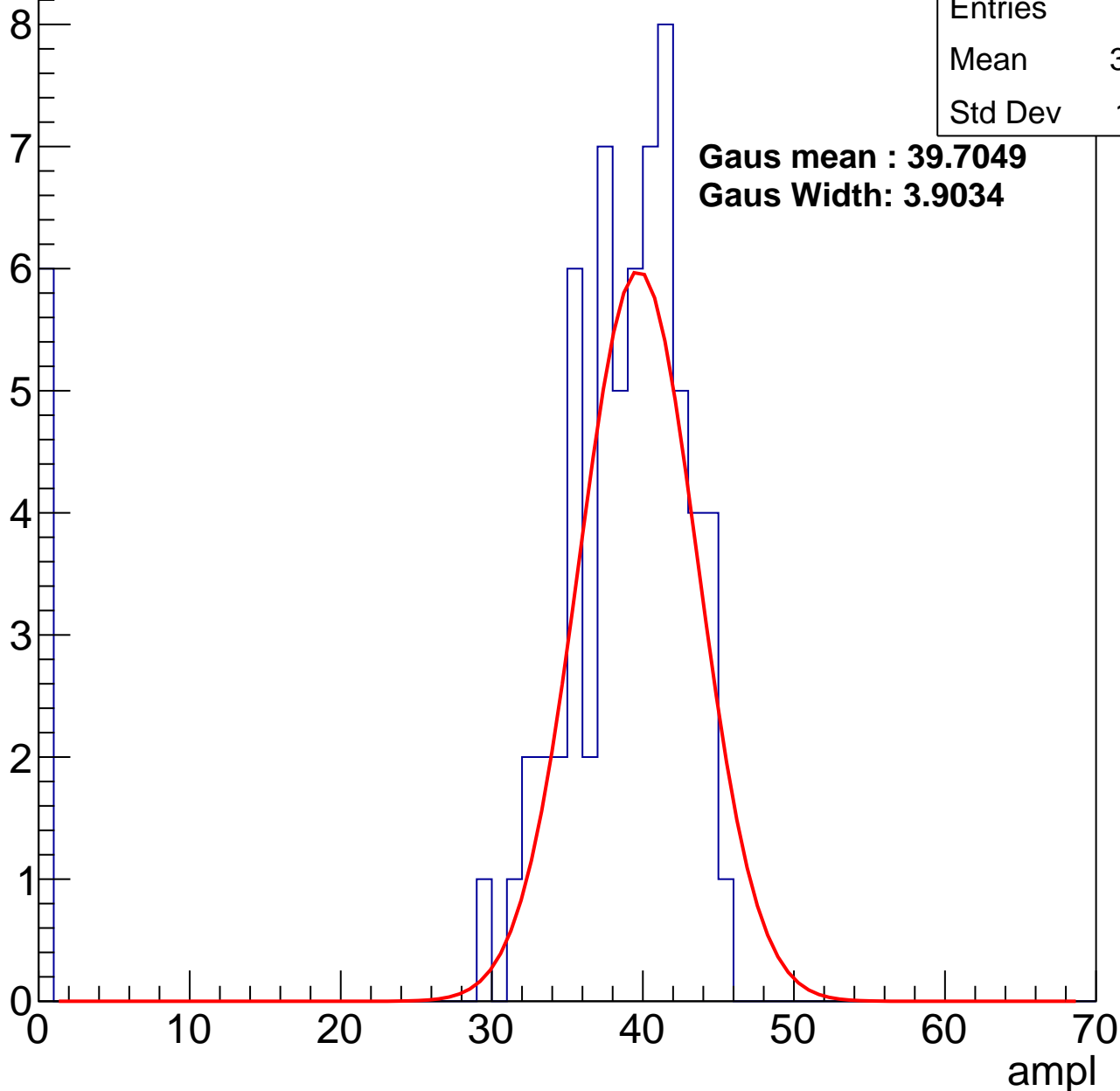
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	69
Mean	35.28
Std Dev	11.41

**Gaus mean : 39.7049**

**Gaus Width: 3.9034**

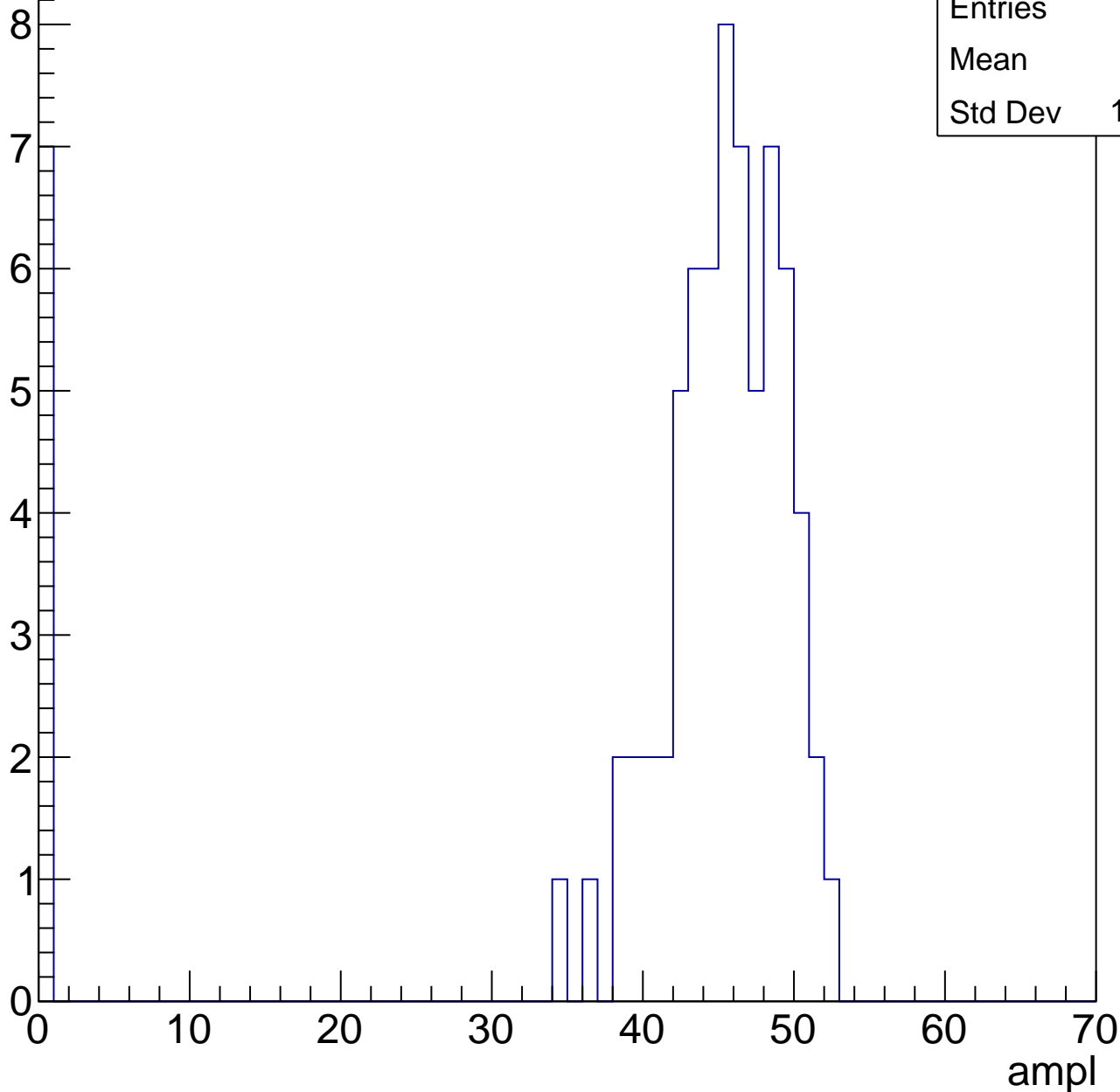


# B1L103S, U26-ch78, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	74
Mean	40.8
Std Dev	13.66

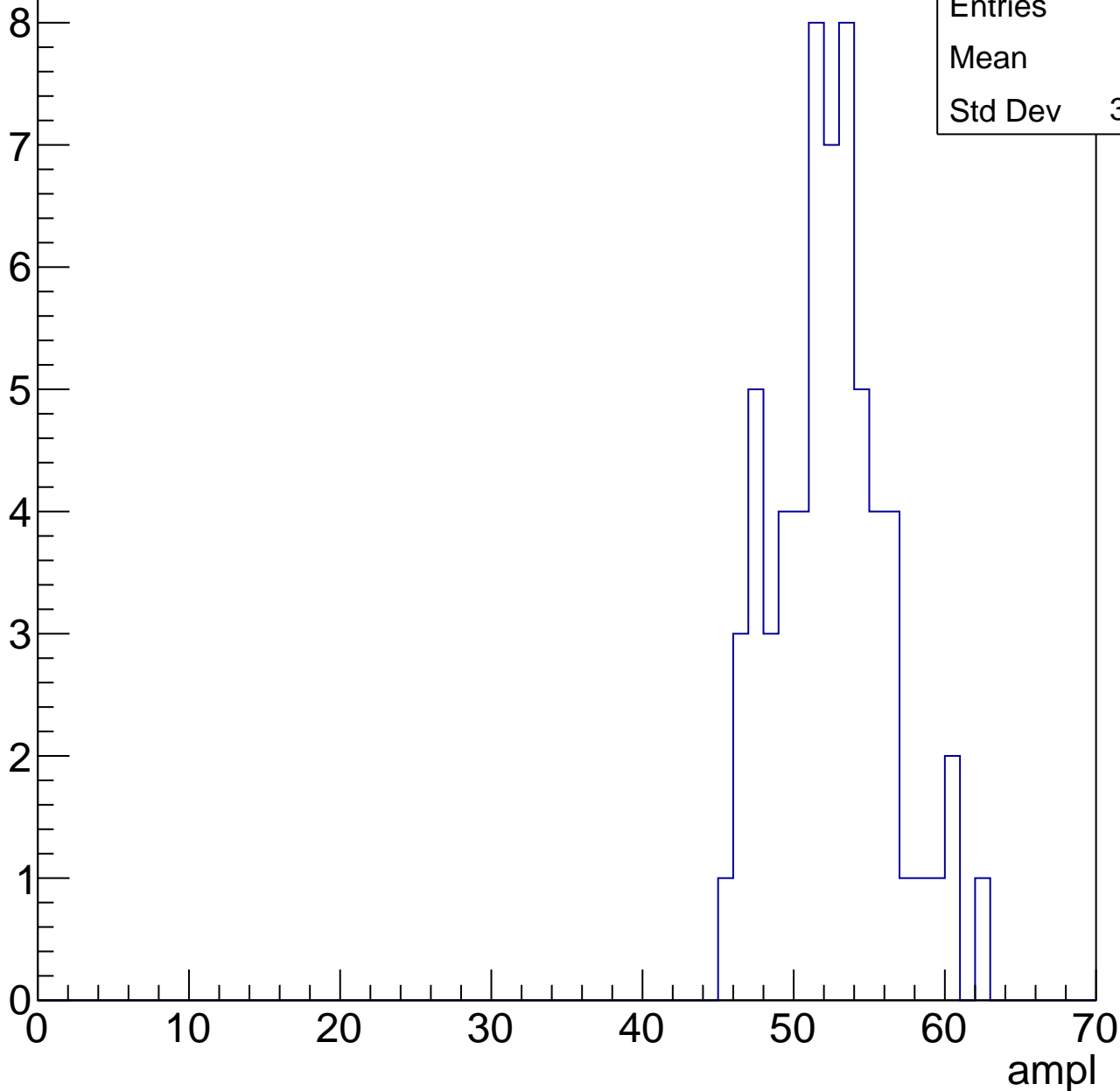


# B1L103S, U26-ch78, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

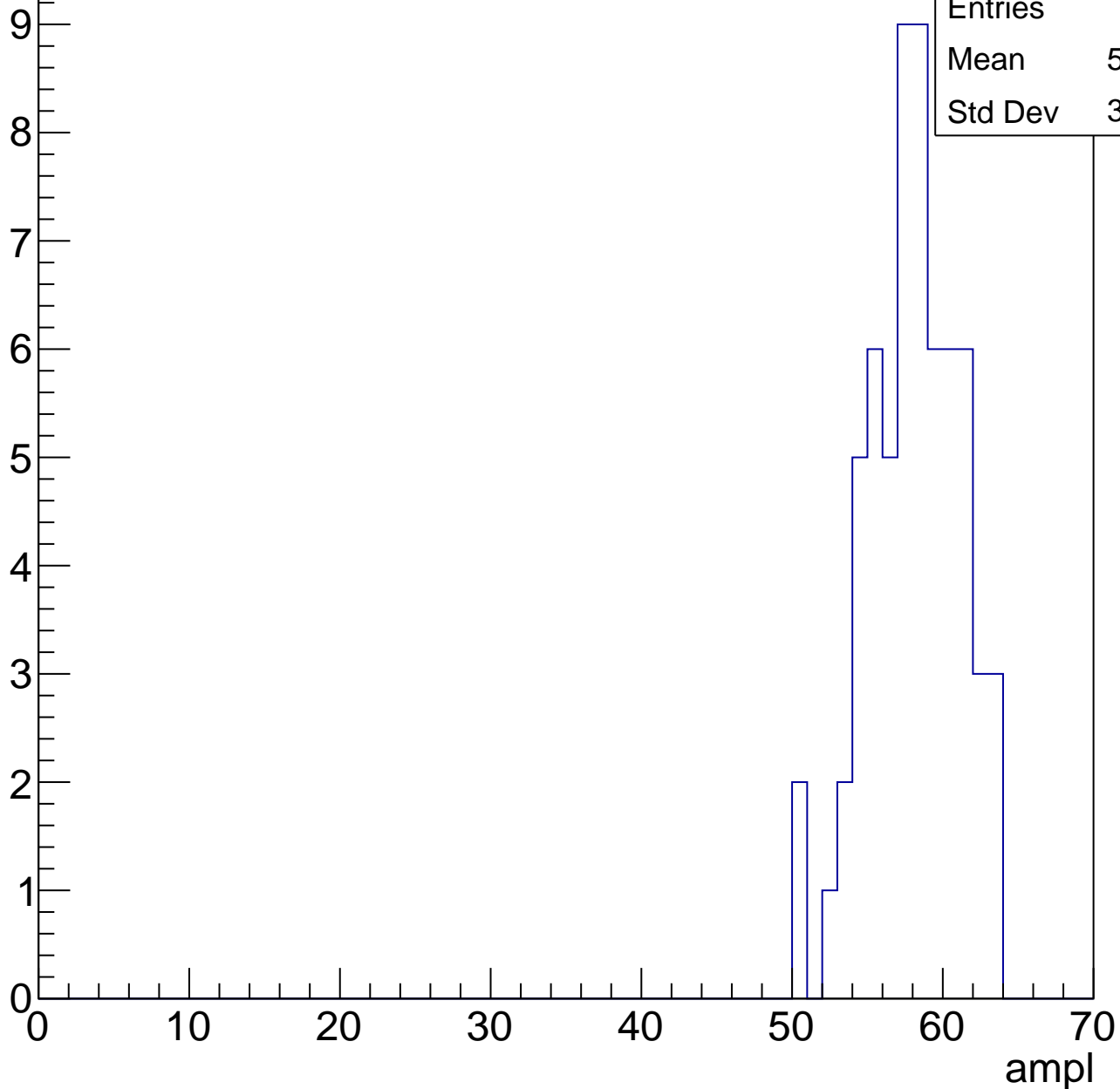
Entries	62
Mean	52
Std Dev	3.716



# B1L103S, U26-ch78, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



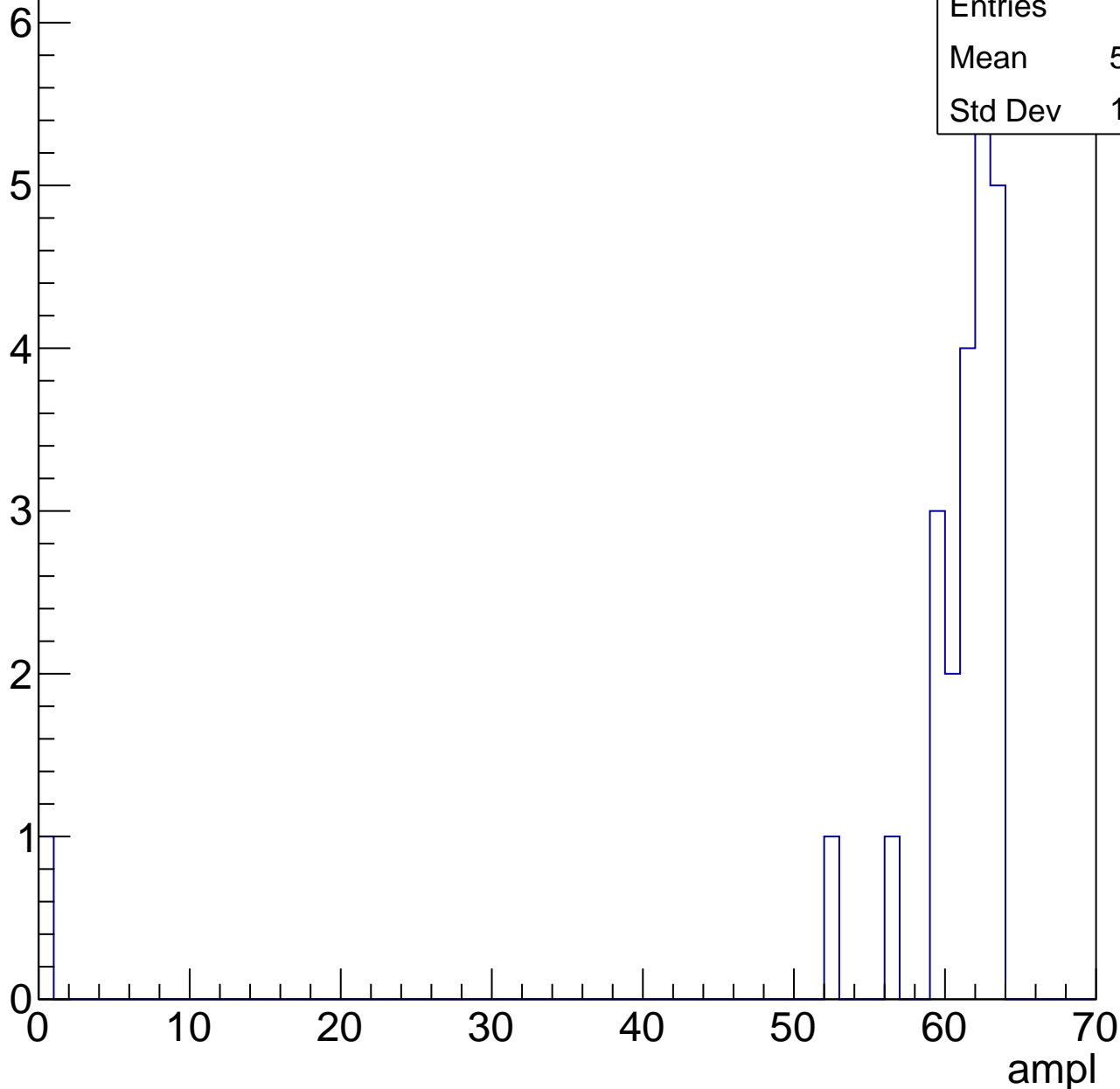
Entries	63
Mean	57.59
Std Dev	3.017

# B1L103S, U26-ch78, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	23
Mean	58.09
Std Dev	12.64



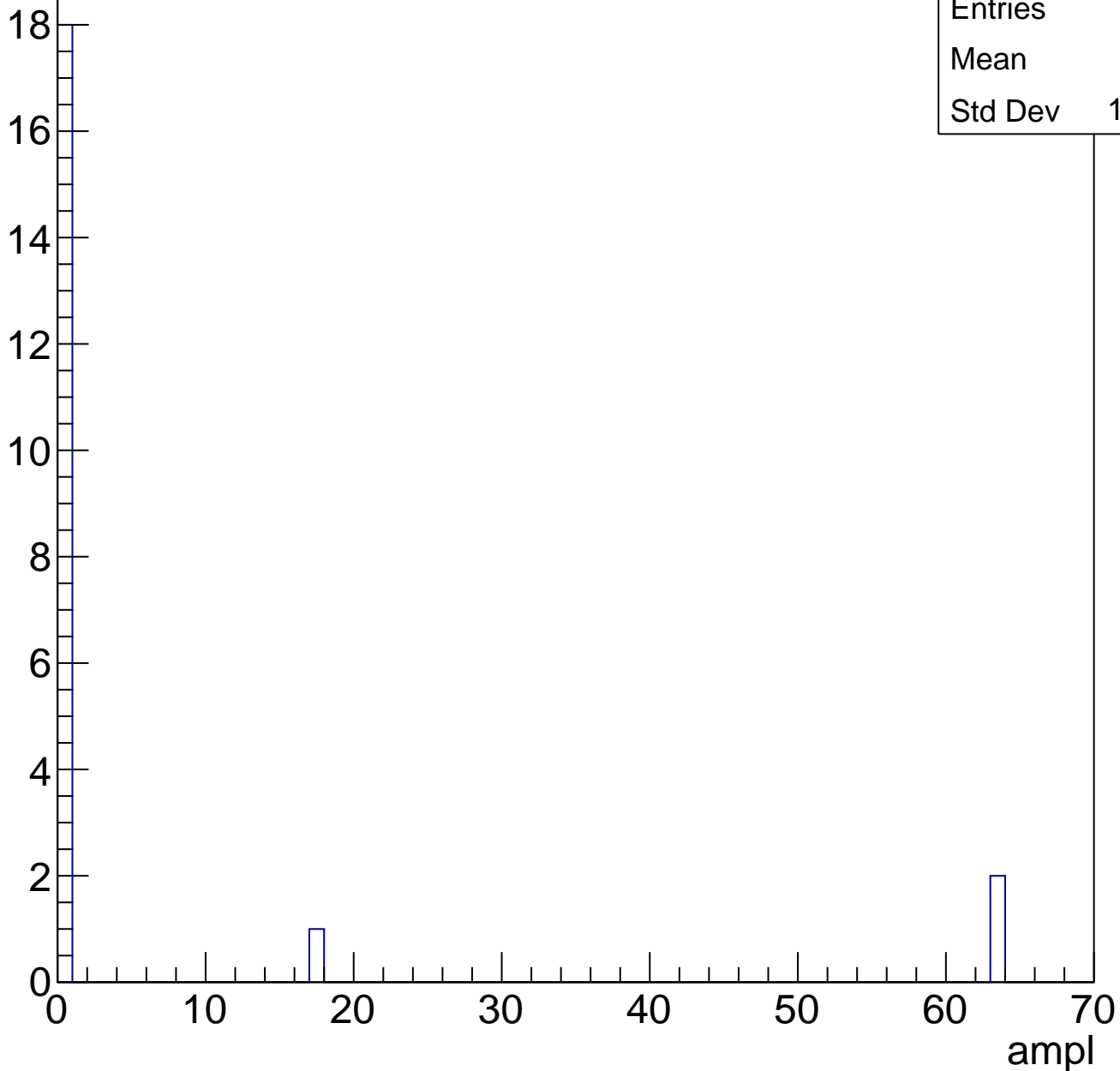


# B1L103S, U26-ch78, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	21
Mean	6.81
Std Dev	18.58

Entry



# B1L103S, U26-ch79, adc0

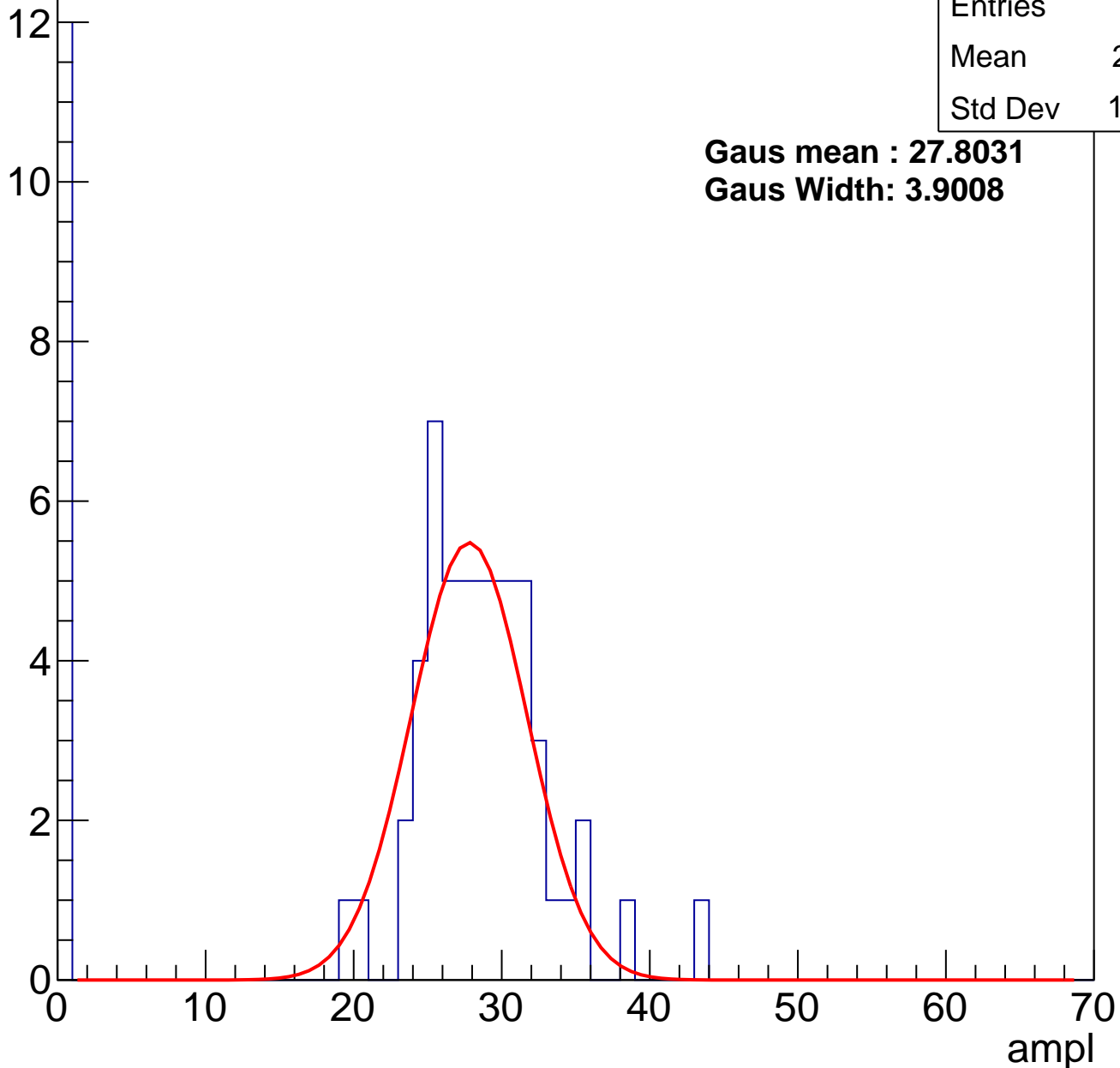
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	66
Mean	23.11
Std Dev	11.53

**Gaus mean : 27.8031**

**Gaus Width: 3.9008**

Entry



# B1L103S, U26-ch79, adc1

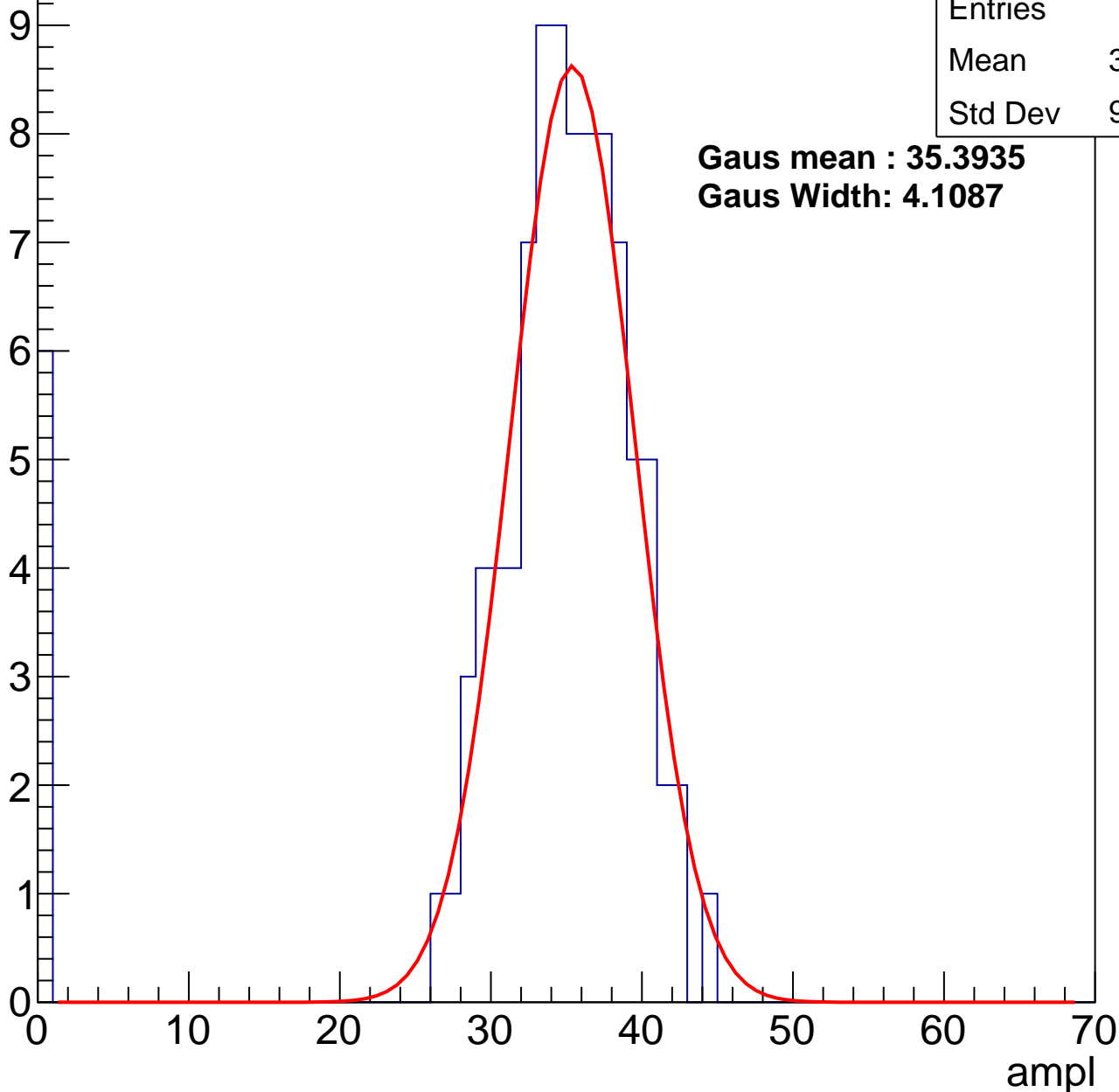
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	94
Mean	32.54
Std Dev	9.254

**Gaus mean : 35.3935**

**Gaus Width: 4.1087**



# B1L103S, U26-ch79, adc2

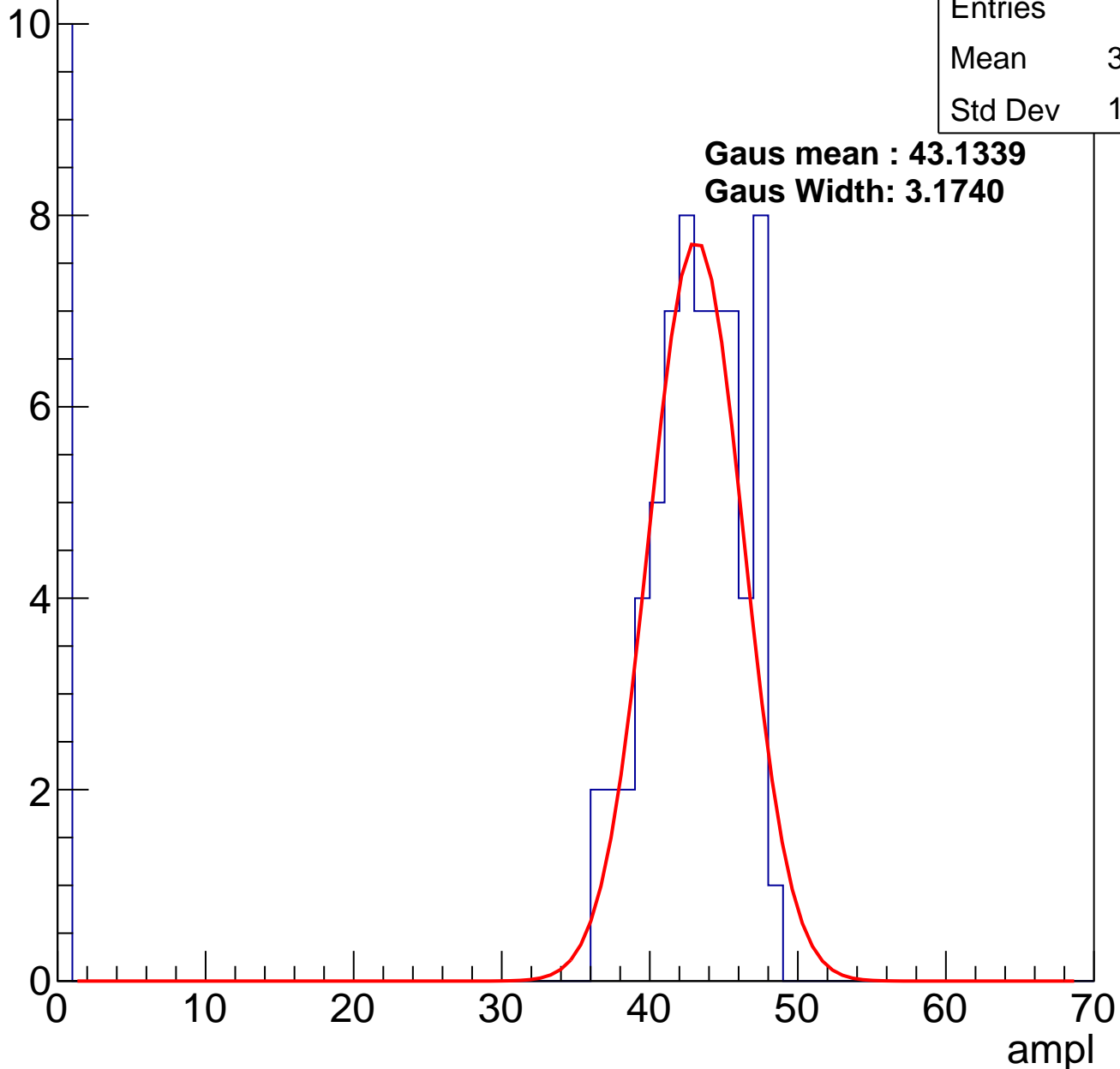
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	74
Mean	36.93
Std Dev	14.87

**Gaus mean : 43.1339**

**Gaus Width: 3.1740**

Entry

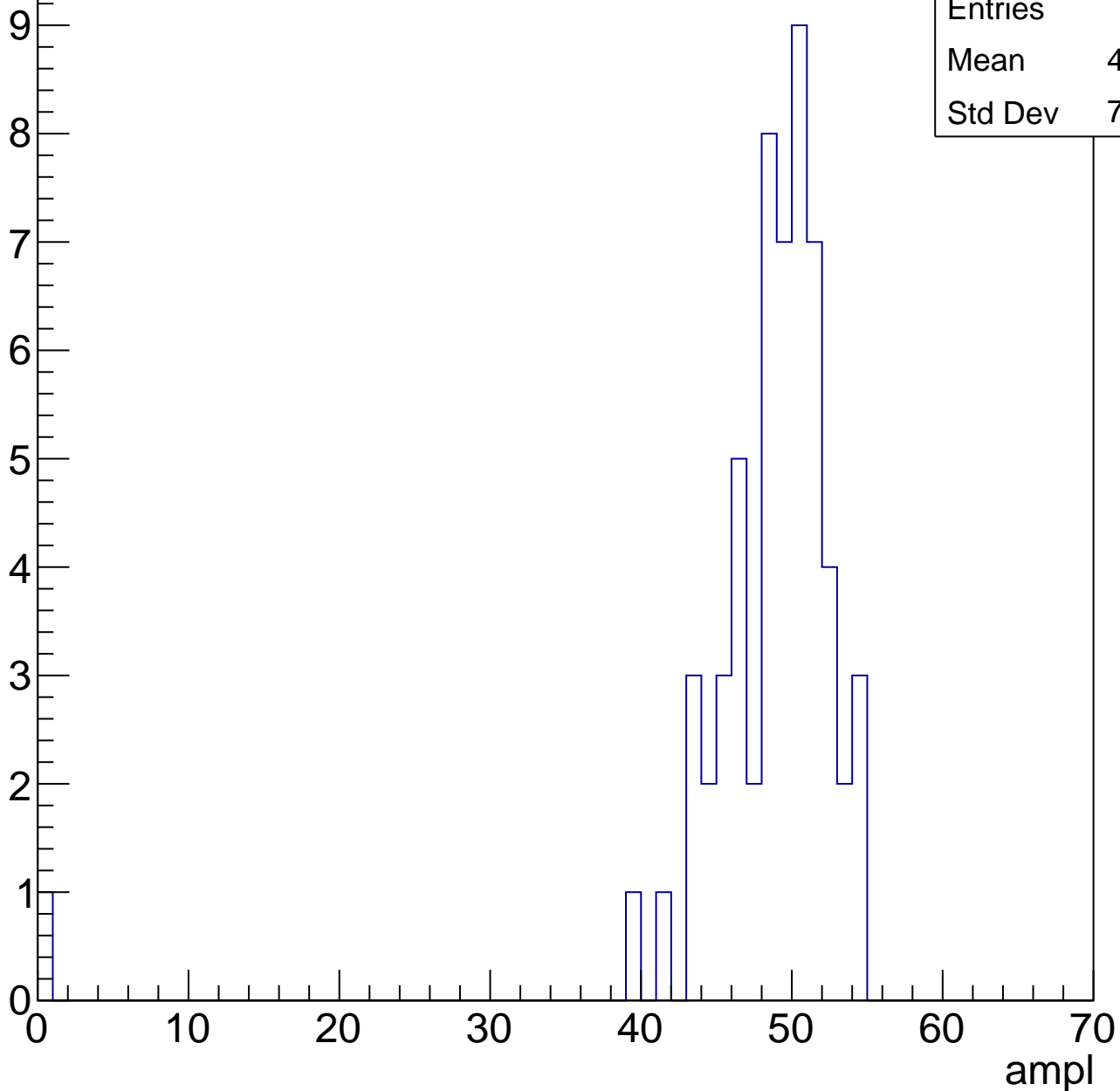


# B1L103S, U26-ch79, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

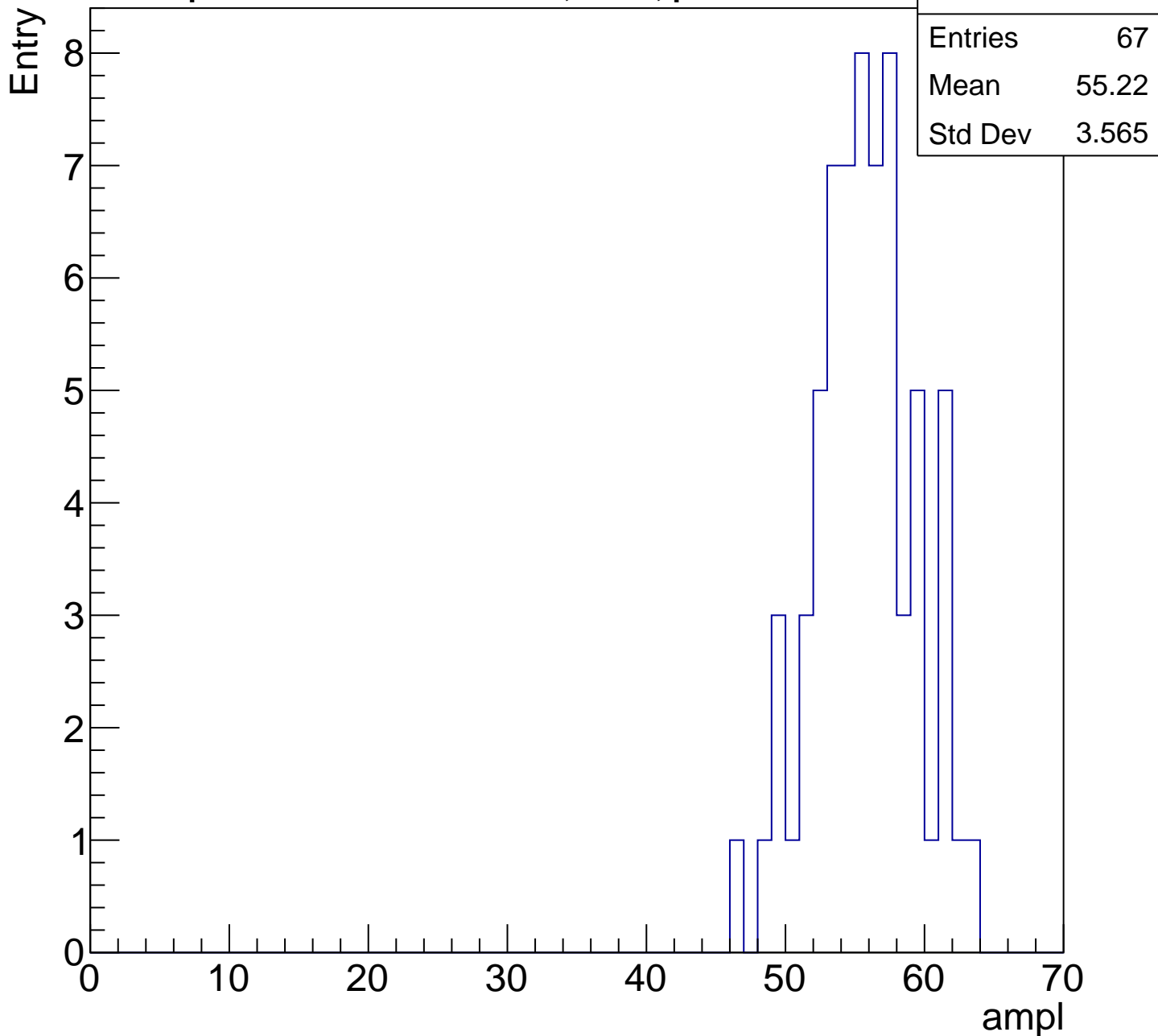
Entry

Entries	58
Mean	47.69
Std Dev	7.086



# B1L103S, U26-ch79, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

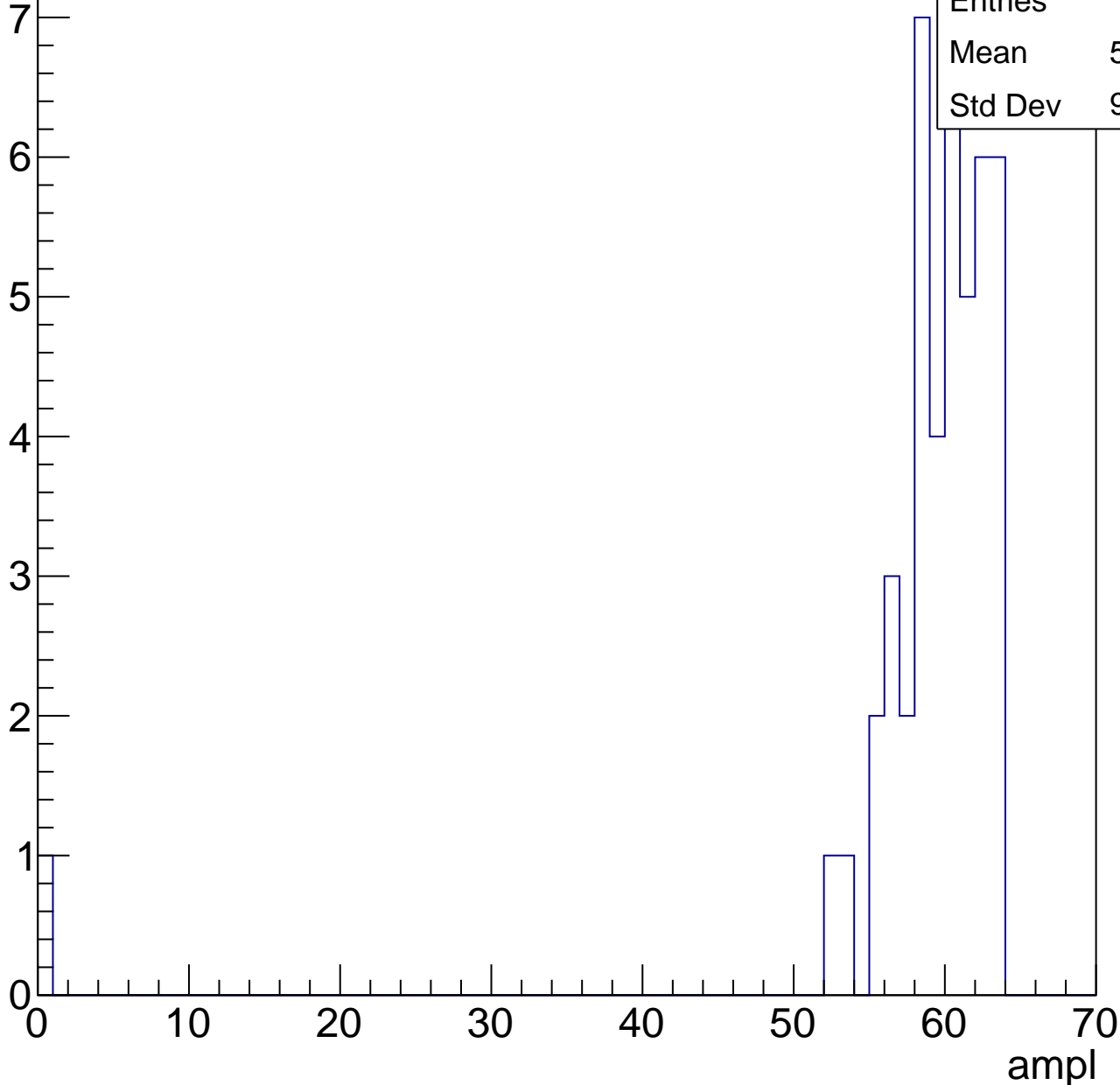


# B1L103S, U26-ch79, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	45
Mean	58.09
Std Dev	9.165



# B1L103S, U26-ch79, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

3

2.5

2

1.5

1

0.5

0

0

10

20

30

40

50

60

70

ampl

Entries

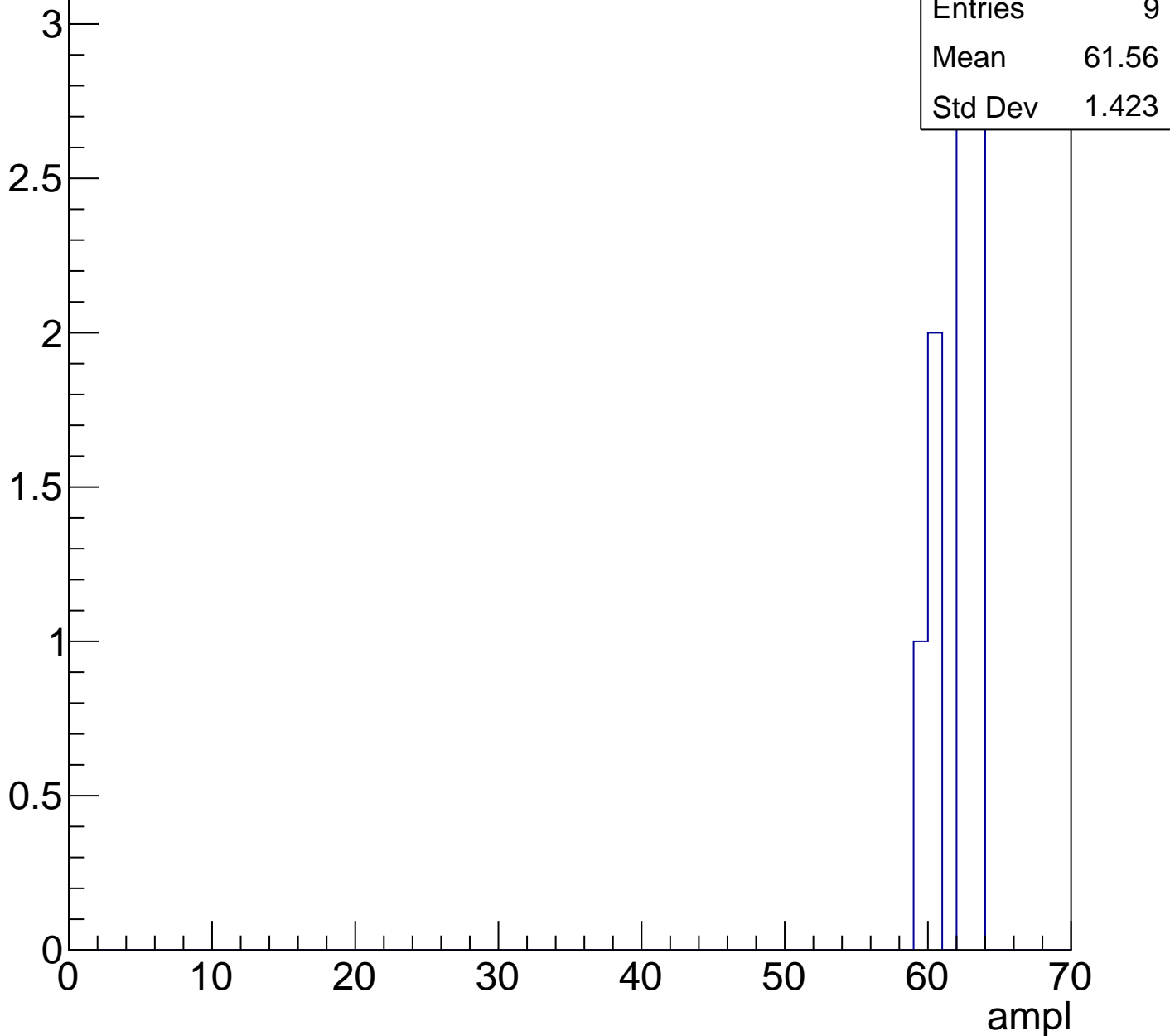
9

Mean

61.56

Std Dev

1.423





# B1L103S, U26-ch79, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

18  
16  
14  
12  
10  
8  
6  
4  
2  
0

Entries	19
Mean	0
Std Dev	0

ampl

# B1L103S, U26-ch80, adc0

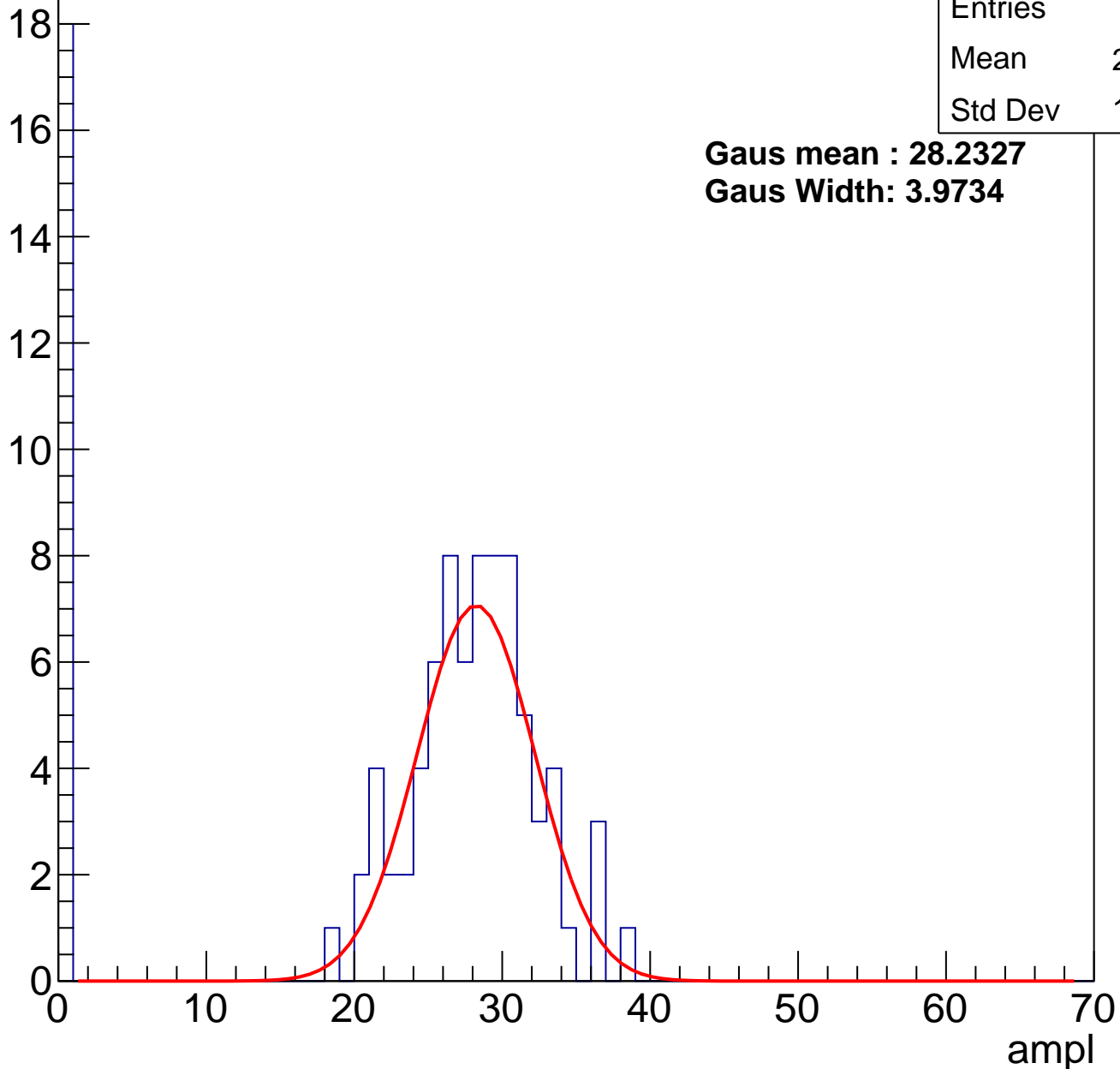
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	94
Mean	22.41
Std Dev	11.51

**Gaus mean : 28.2327**

**Gaus Width: 3.9734**

Entry



# B1L103S, U26-ch80, adc1

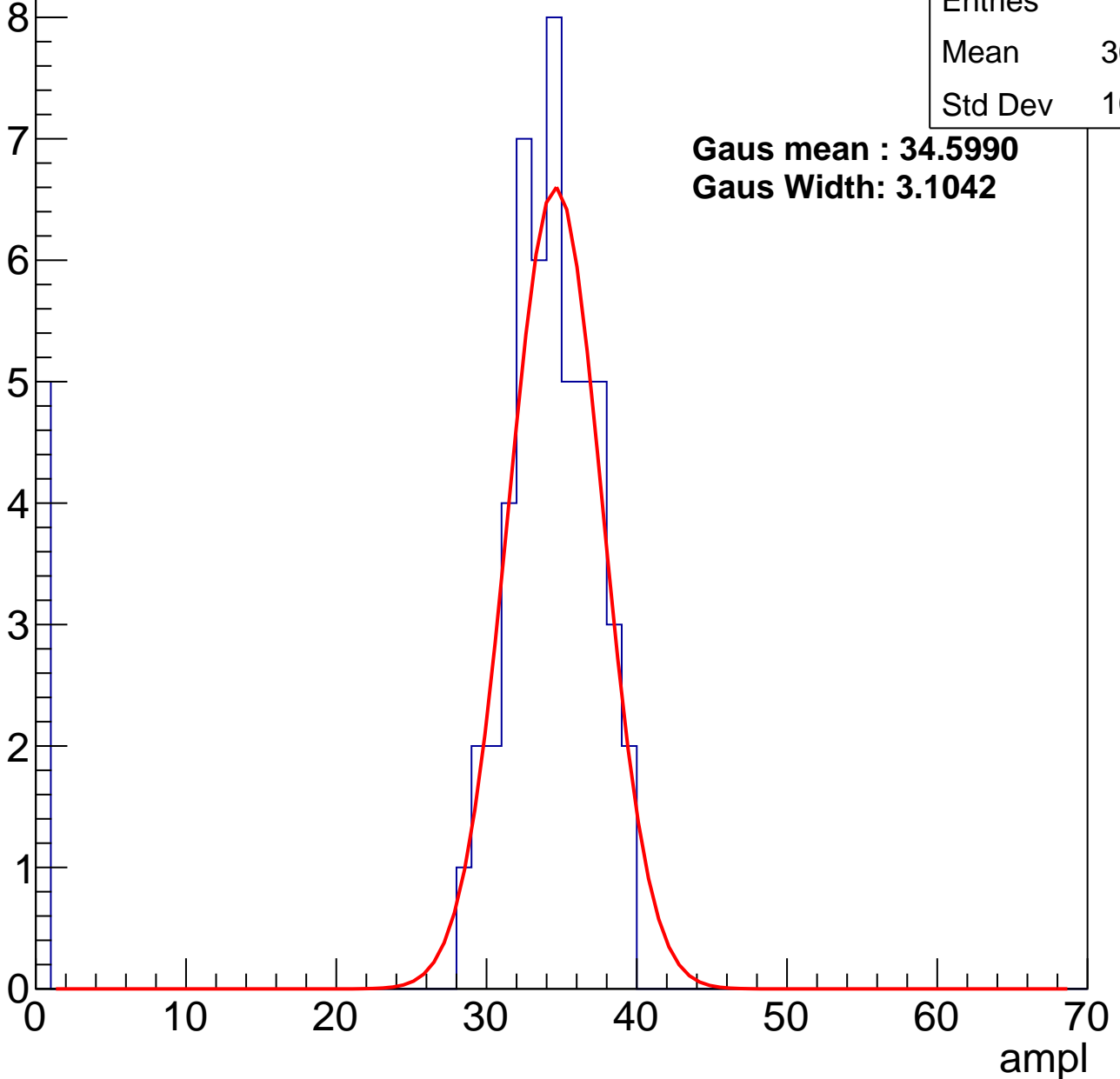
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	55
Mean	30.84
Std Dev	10.08

**Gaus mean : 34.5990**

**Gaus Width: 3.1042**



# B1L103S, U26-ch80, adc2

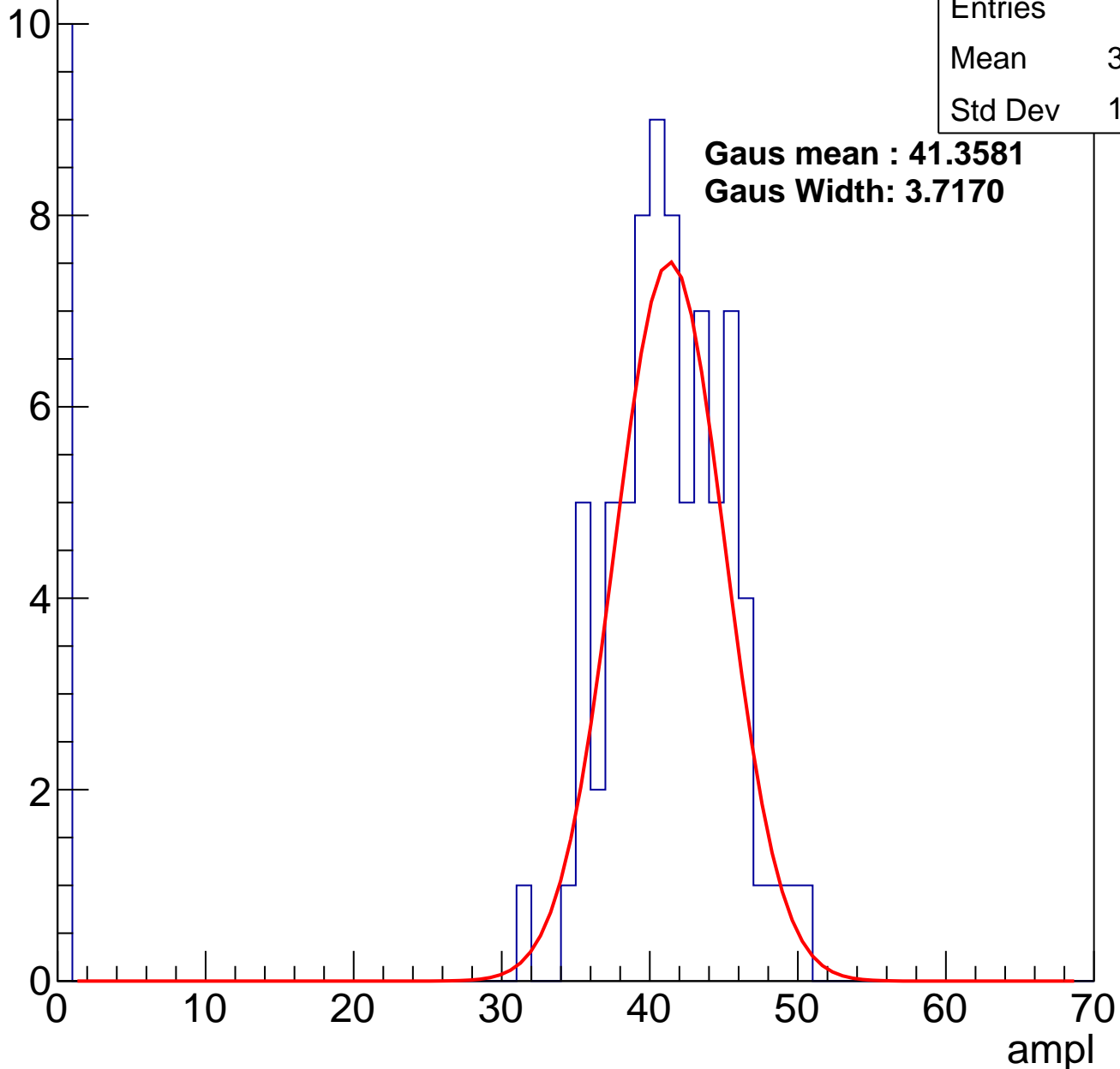
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	86
Mean	36.17
Std Dev	13.59

**Gaus mean : 41.3581**

**Gaus Width: 3.7170**

Entry

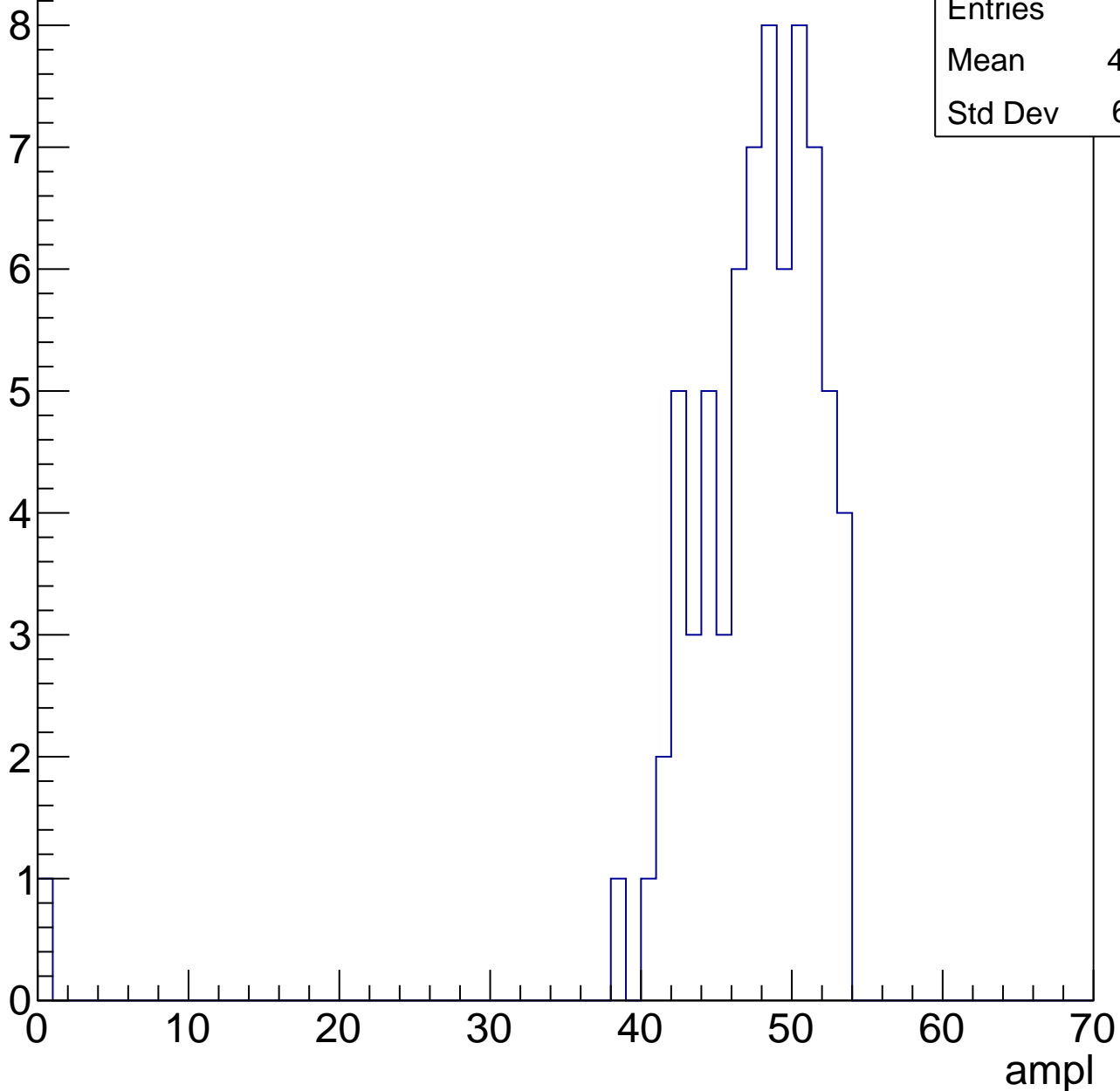


# B1L103S, U26-ch80, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	72
Mean	46.75
Std Dev	6.591

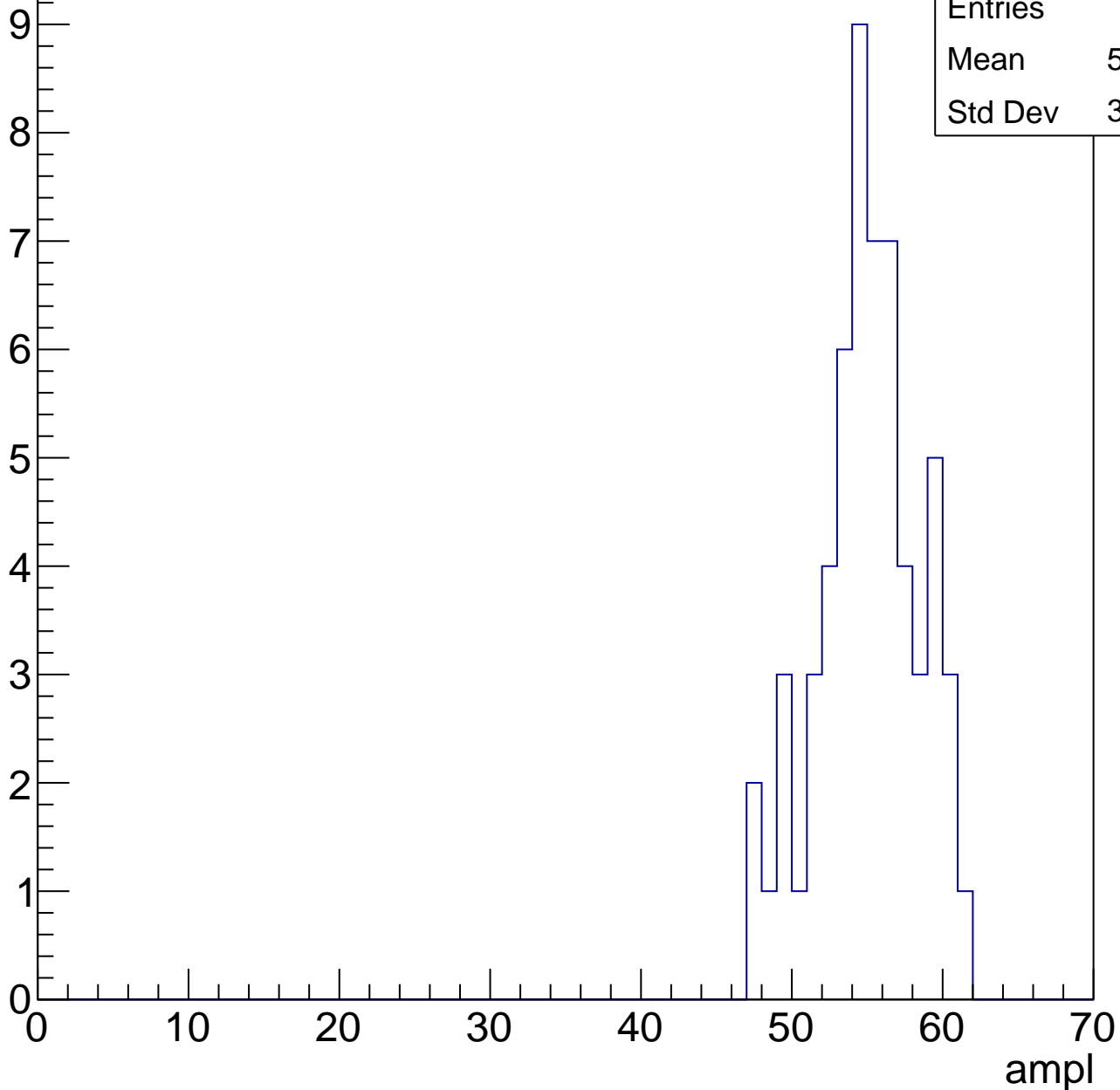


# B1L103S, U26-ch80, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	59
Mean	54.56
Std Dev	3.336

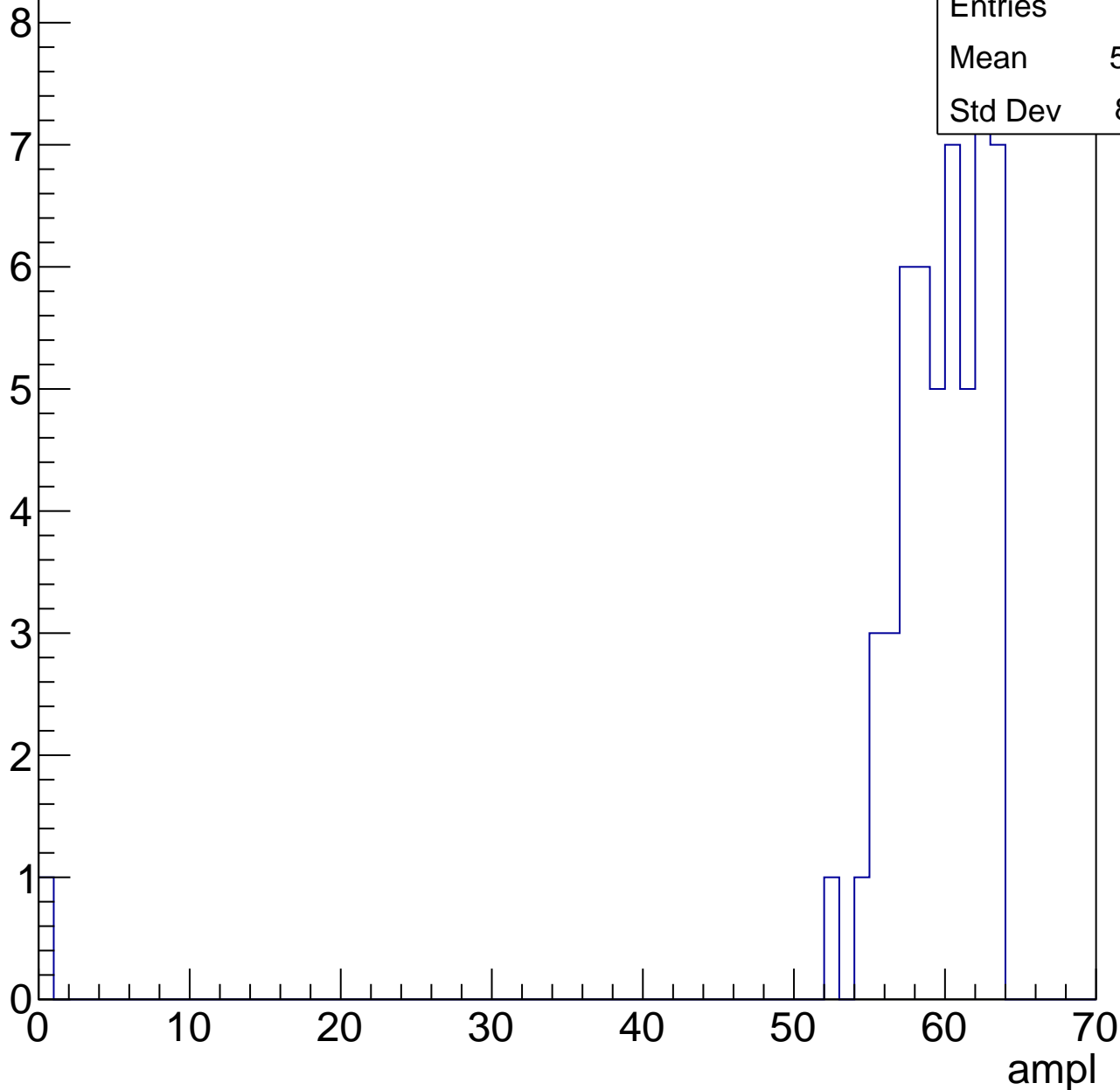


# B1L103S, U26-ch80, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

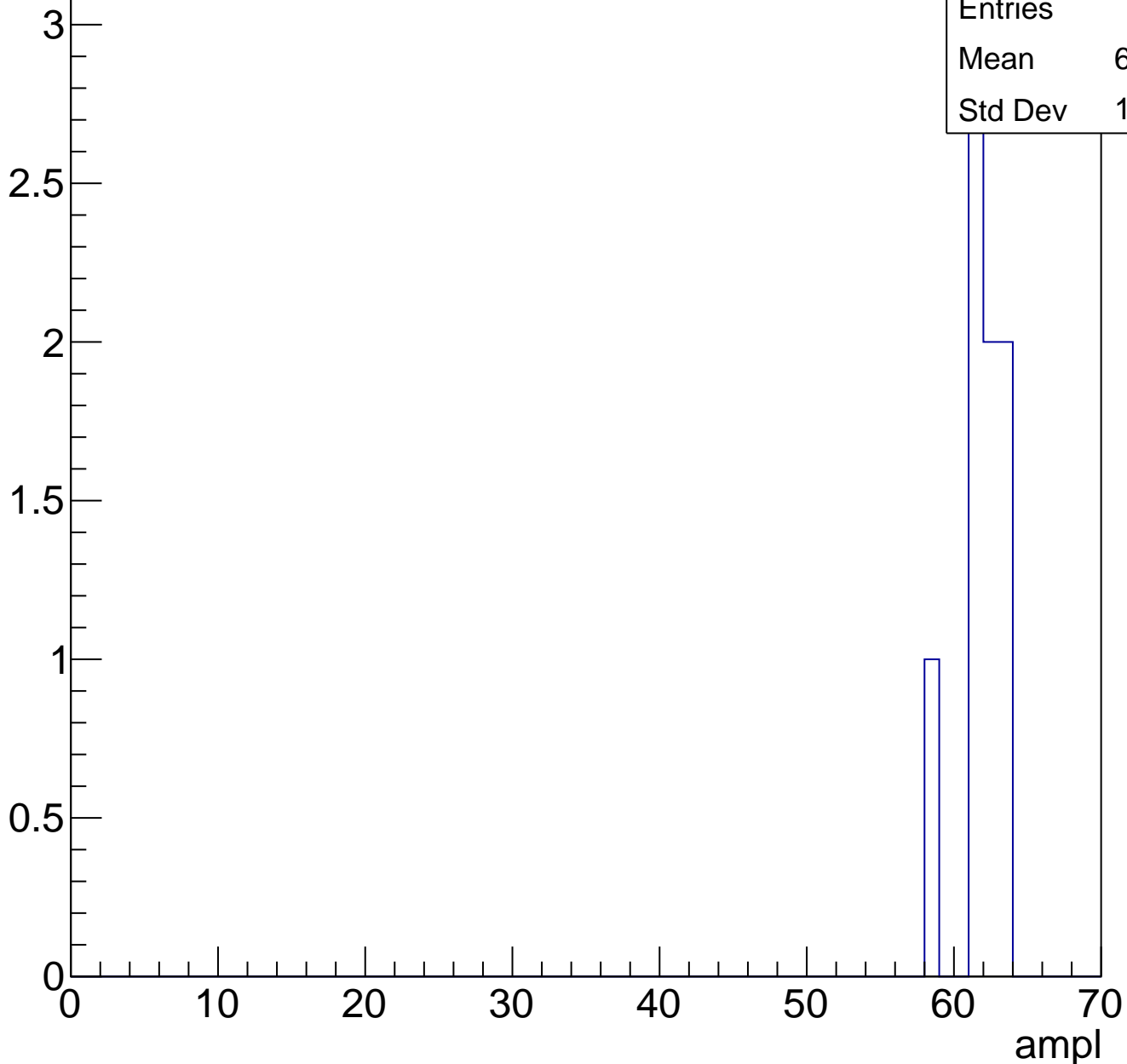
Entries	53
Mean	58.23
Std Dev	8.511



# B1L103S, U26-ch80, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

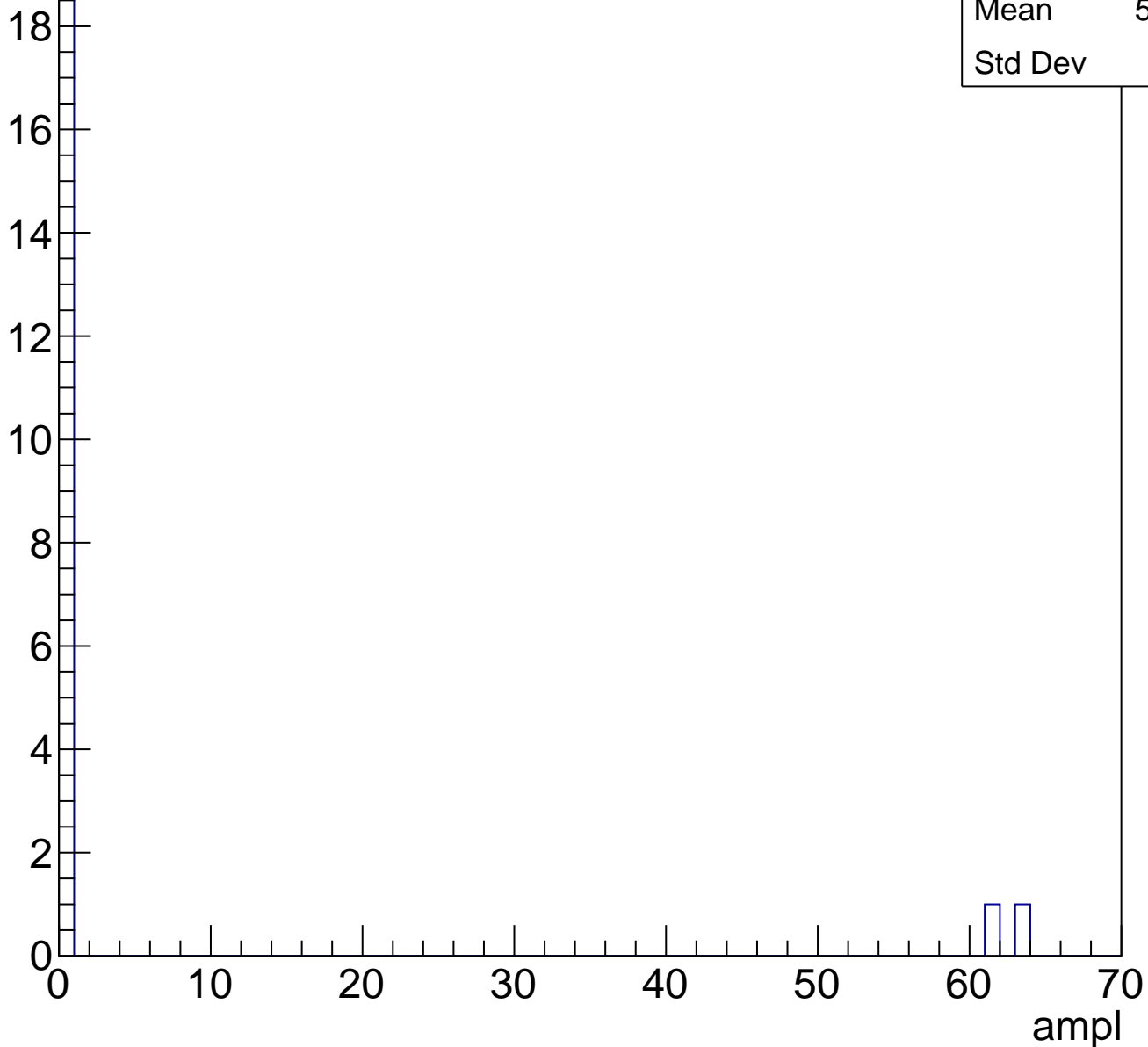




# B1L103S, U26-ch80, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



Entries	21
Mean	5.905
Std Dev	18.2

# B1L103S, U26-ch81, adc0

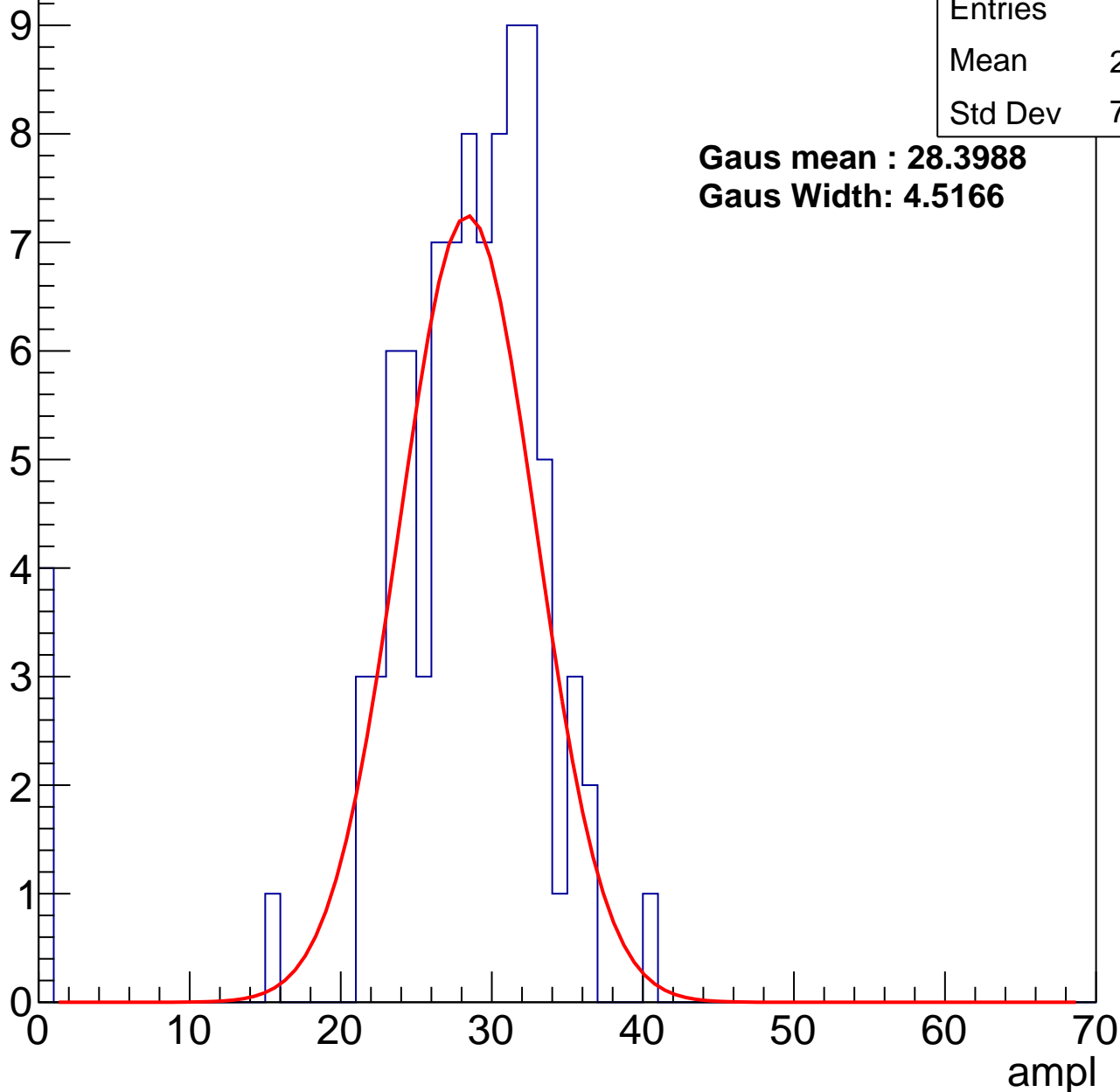
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	93
Mean	27.12
Std Dev	7.063

**Gaus mean : 28.3988**

**Gaus Width: 4.5166**



# B1L103S, U26-ch81, adc1

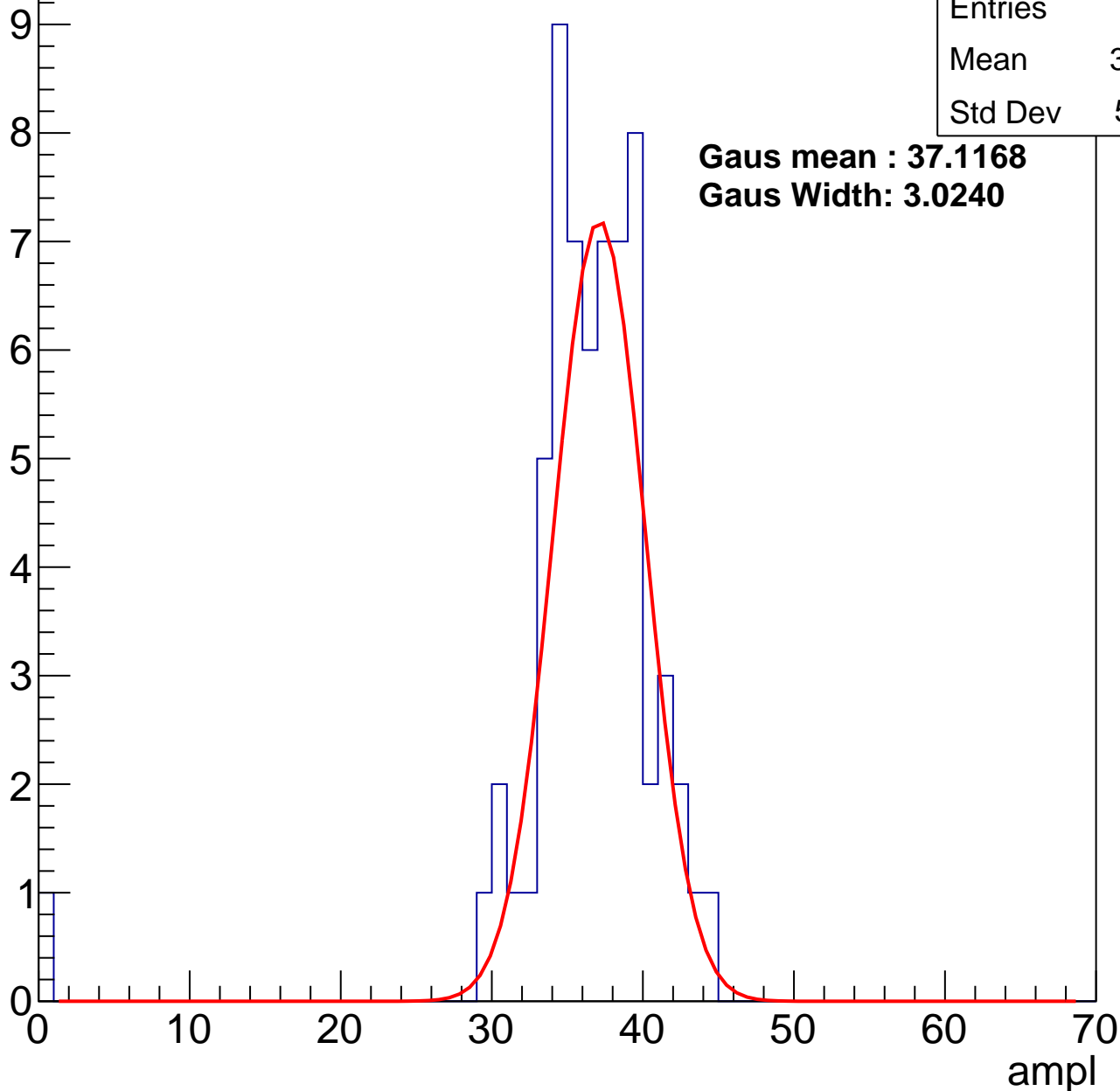
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	64
Mean	35.86
Std Dev	5.511

**Gaus mean : 37.1168**

**Gaus Width: 3.0240**



# B1L103S, U26-ch81, adc2

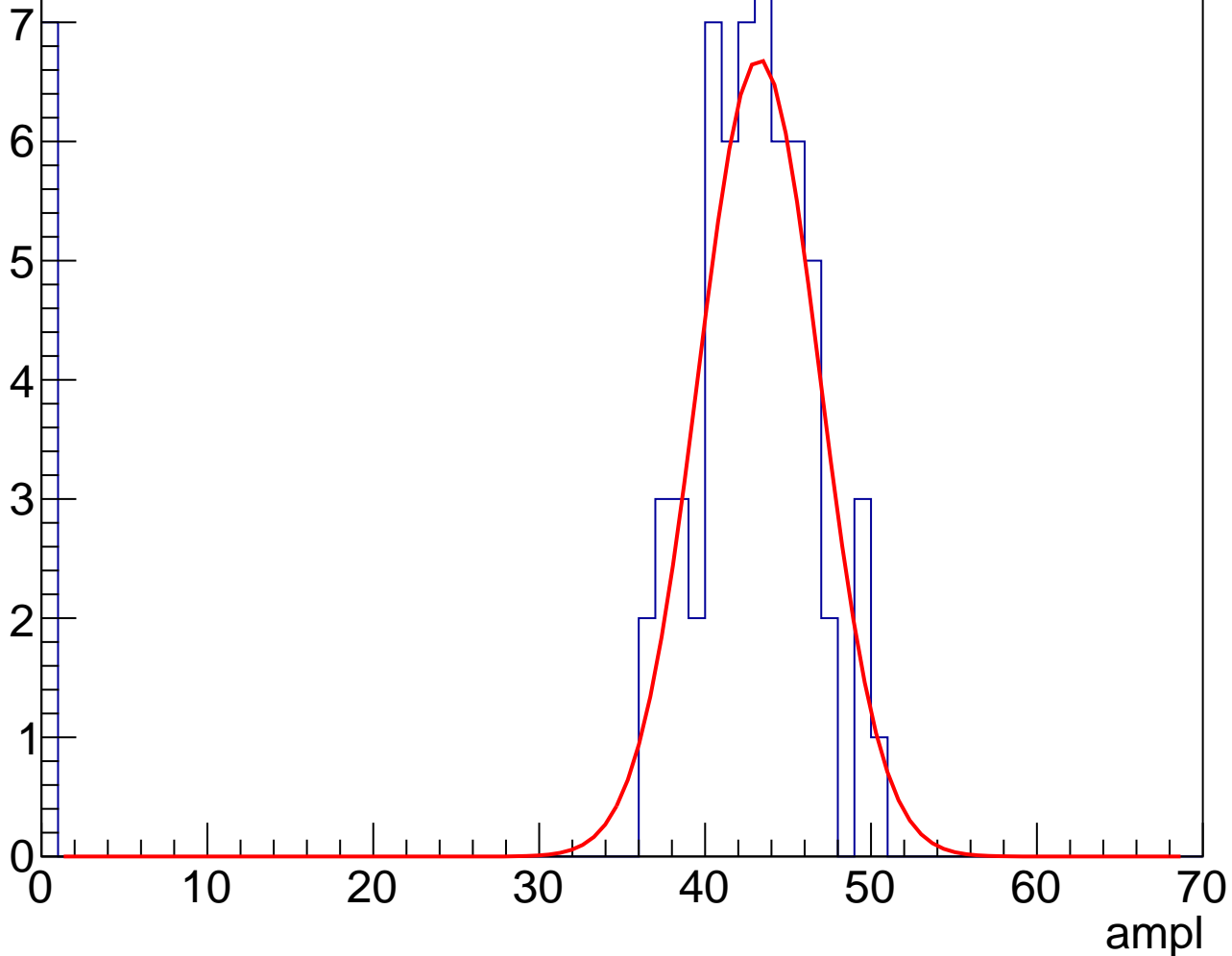
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	69
Mean	38.22
Std Dev	13.21

**Gaus mean : 43.2476**

**Gaus Width: 3.6530**

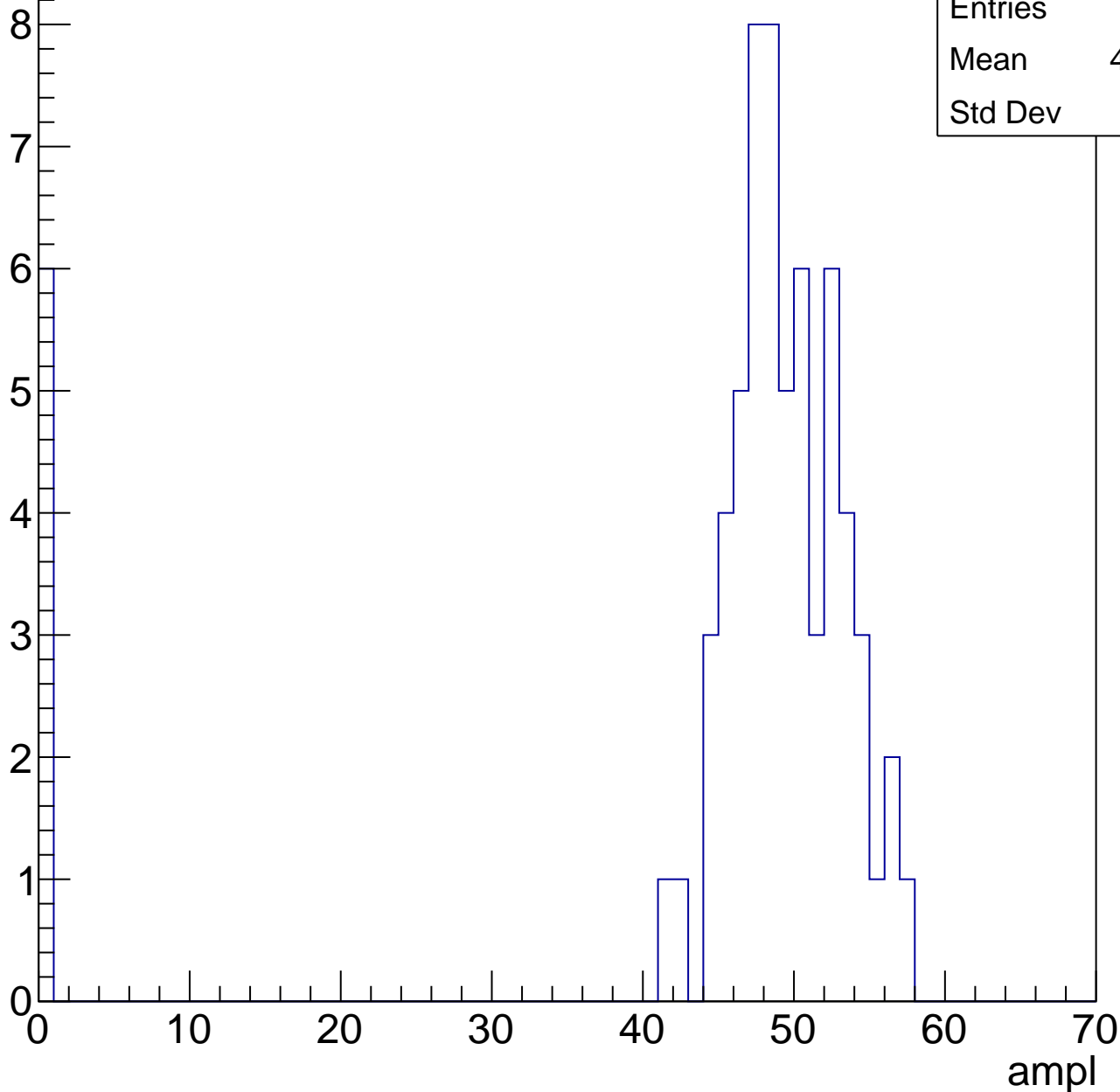


# B1L103S, U26-ch81, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	67
Mean	44.67
Std Dev	14.4

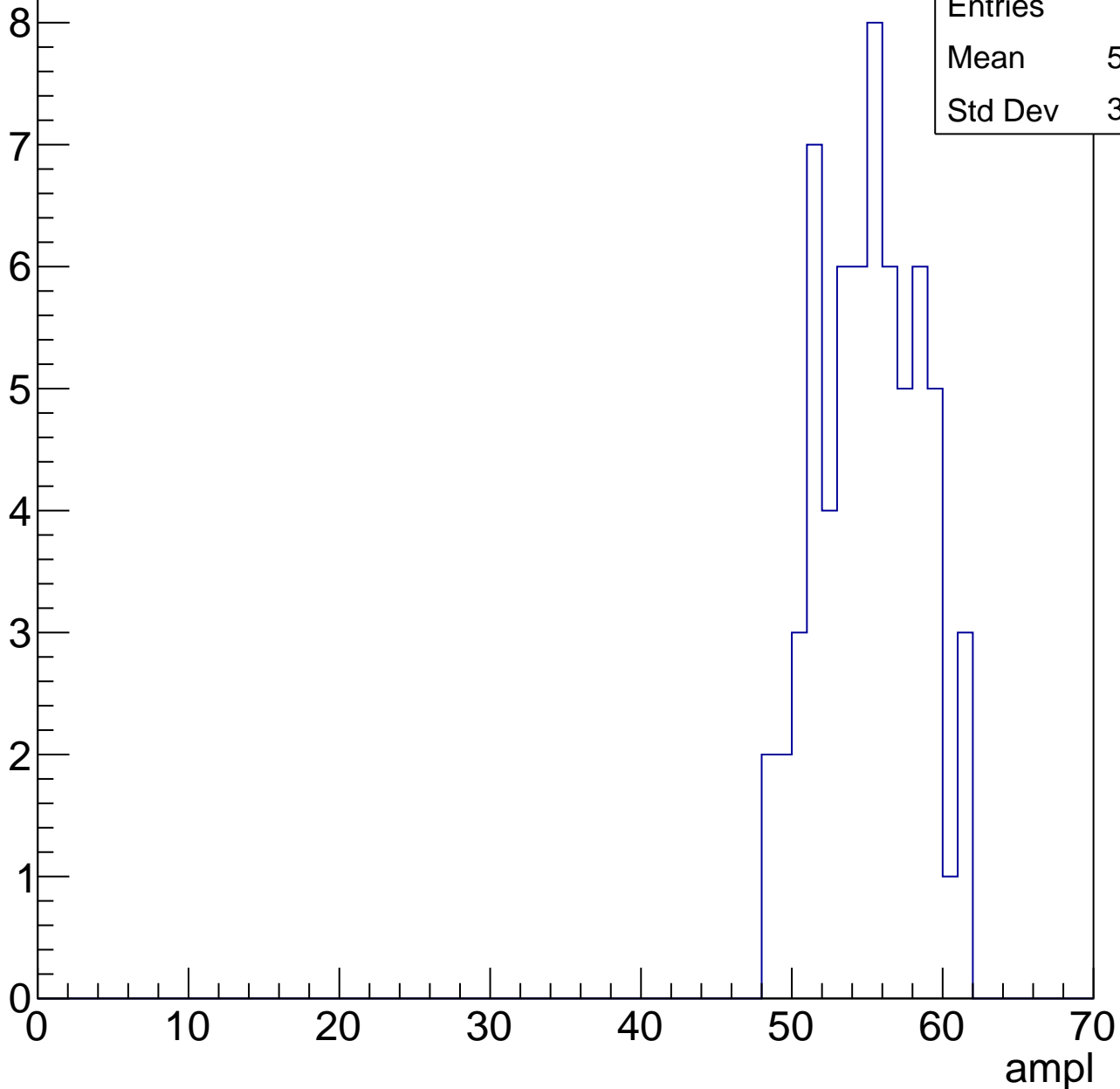


# B1L103S, U26-ch81, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	64
Mean	54.66
Std Dev	3.327



# B1L103S, U26-ch81, adc5

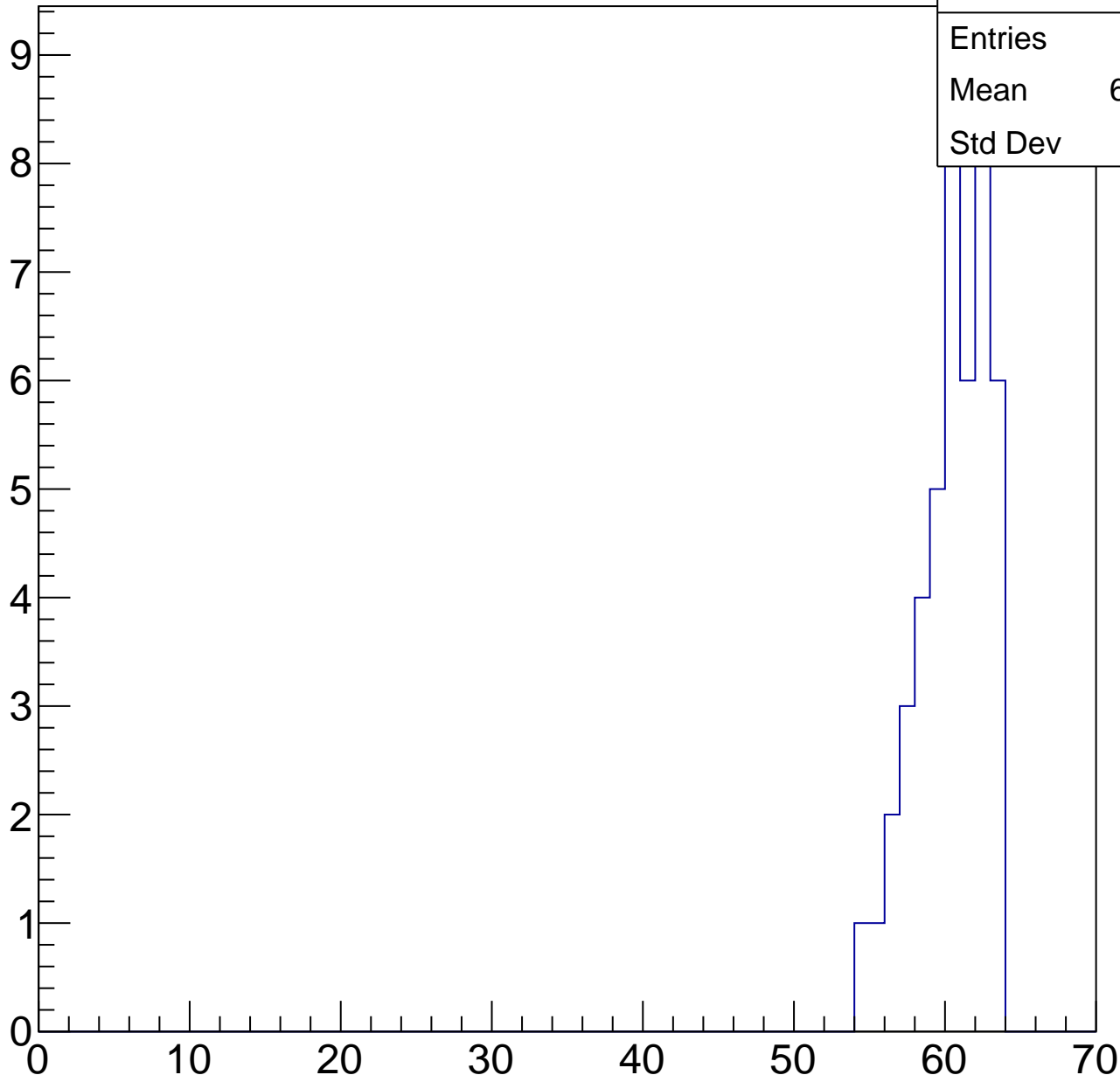
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	46
Mean	60.02
Std Dev	2.27

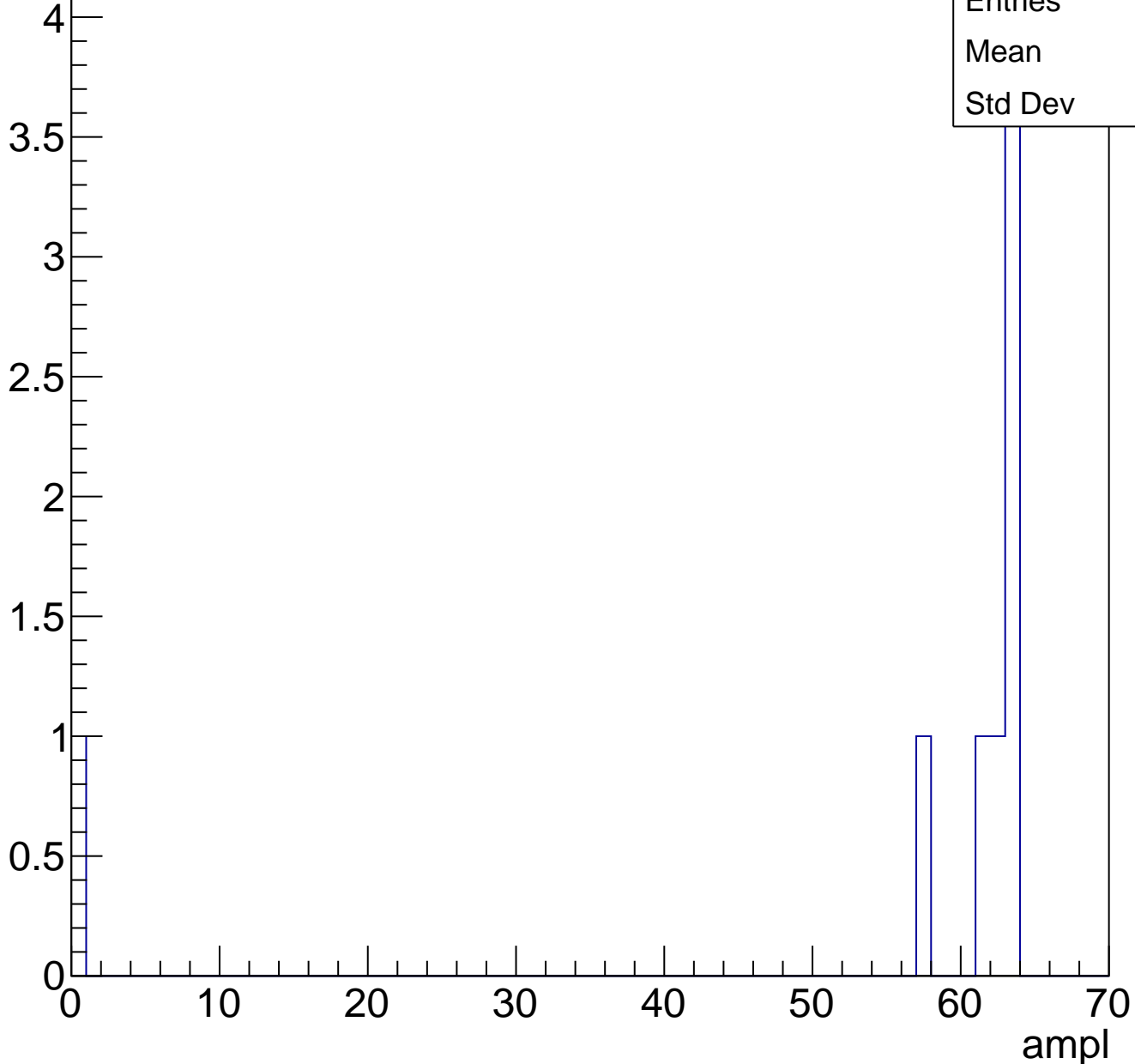
ampl



# B1L103S, U26-ch81, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



Entries	8
Mean	54
Std Dev	20.5



# B1L103S, U26-ch81, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



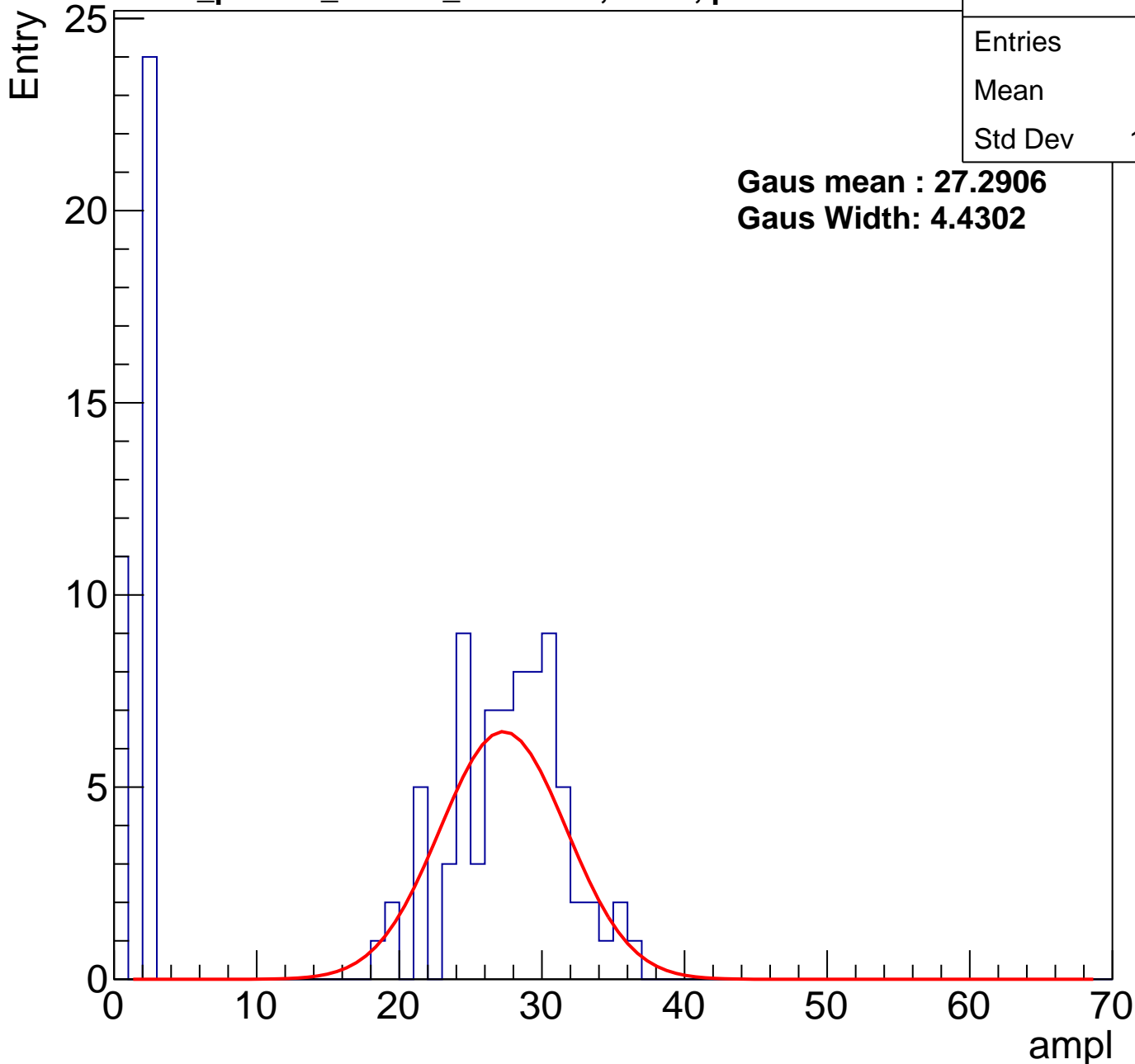
# B1L103S, U26-ch82, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	110
Mean	19.01
Std Dev	12.47

**Gaus mean : 27.2906**

**Gaus Width: 4.4302**



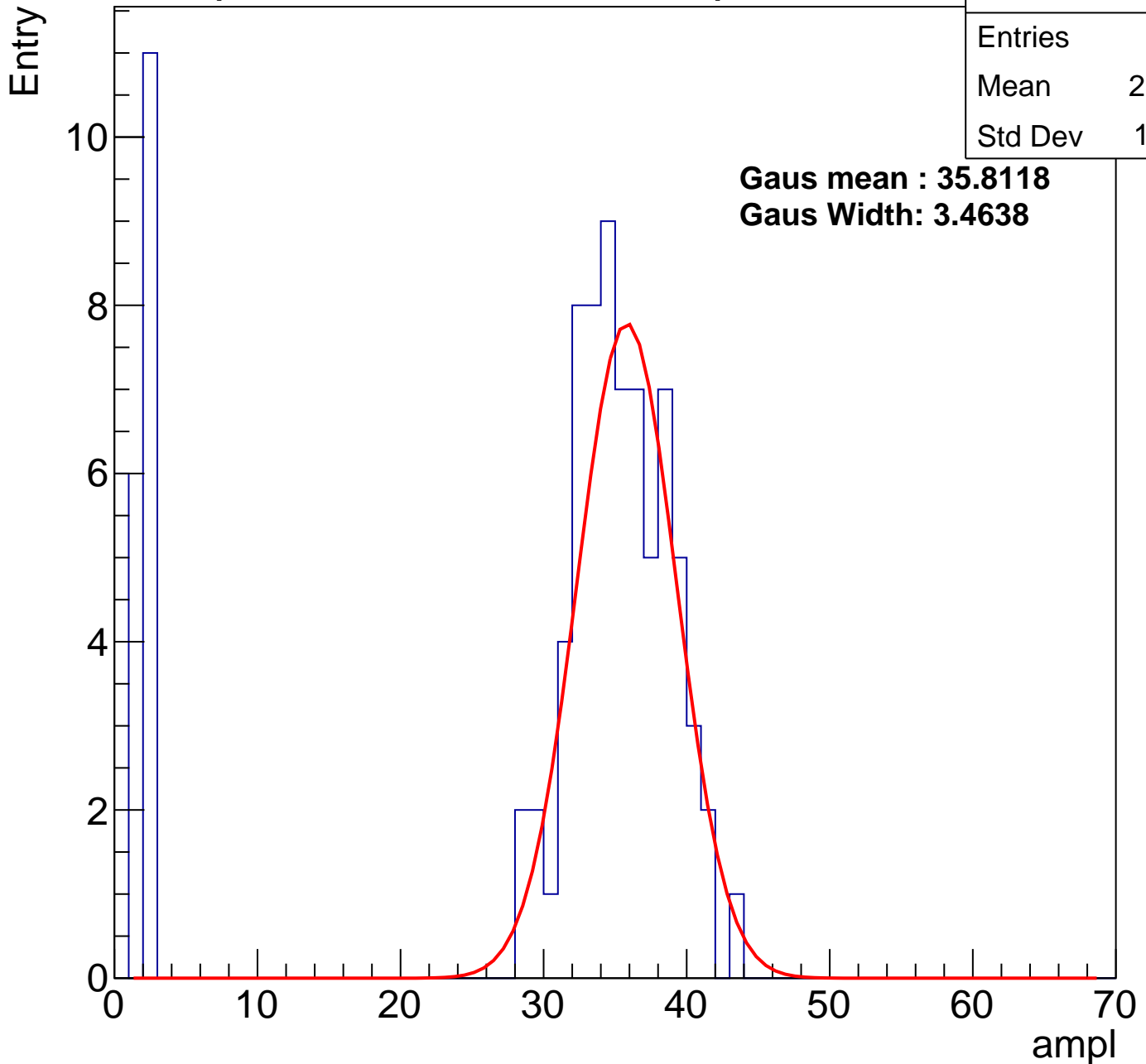
# B1L103S, U26-ch82, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	88
Mean	28.45
Std Dev	13.61

**Gaus mean : 35.8118**

**Gaus Width: 3.4638**



# B1L103S, U26-ch82, adc2

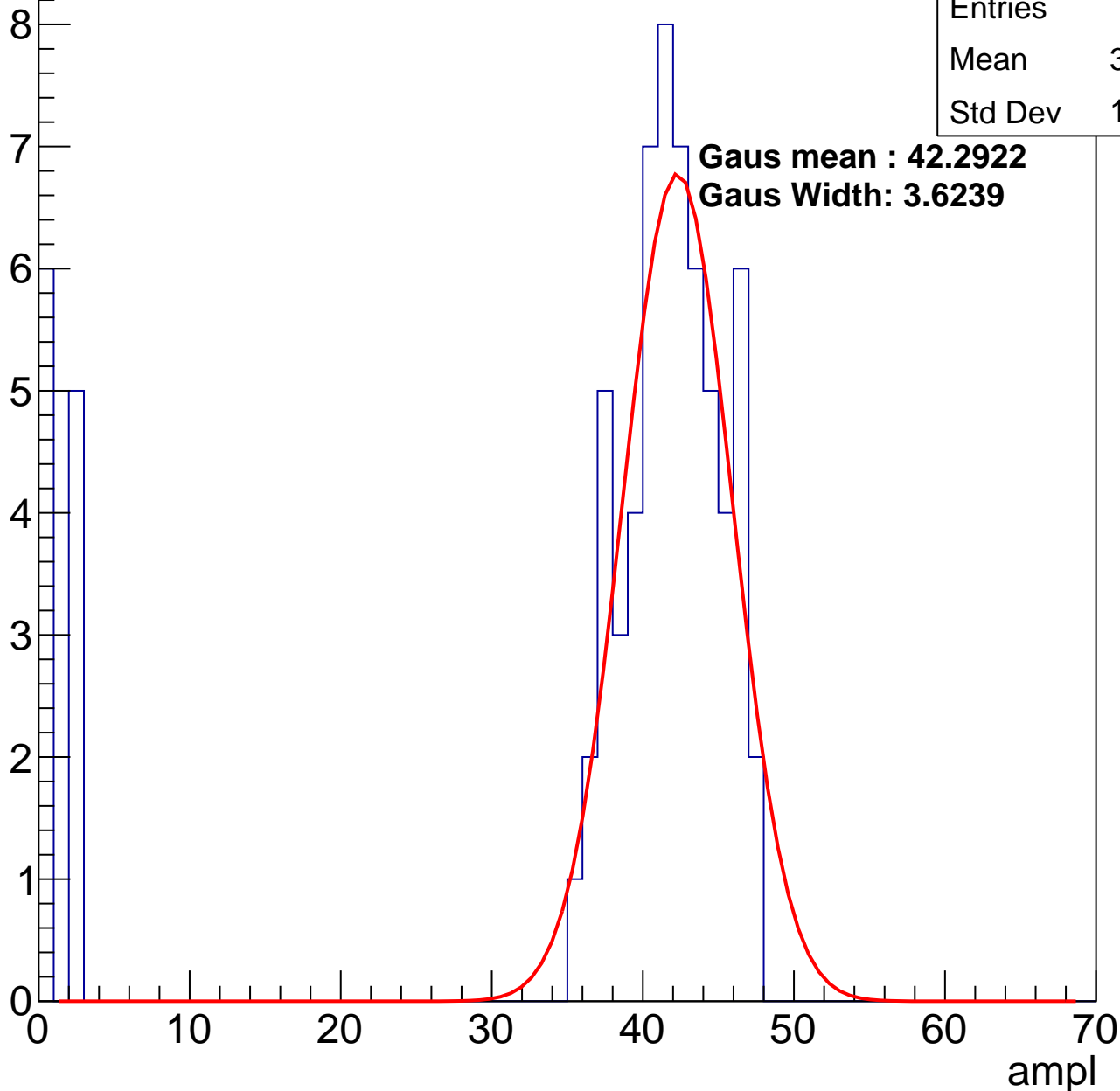
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	71
Mean	35.24
Std Dev	14.97

**Gaus mean : 42.2922**

**Gaus Width: 3.6239**



# B1L103S, U26-ch82, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	72
Mean	46.81
Std Dev	8.326

Entry

10

8

6

4

2

0

0

10

20

30

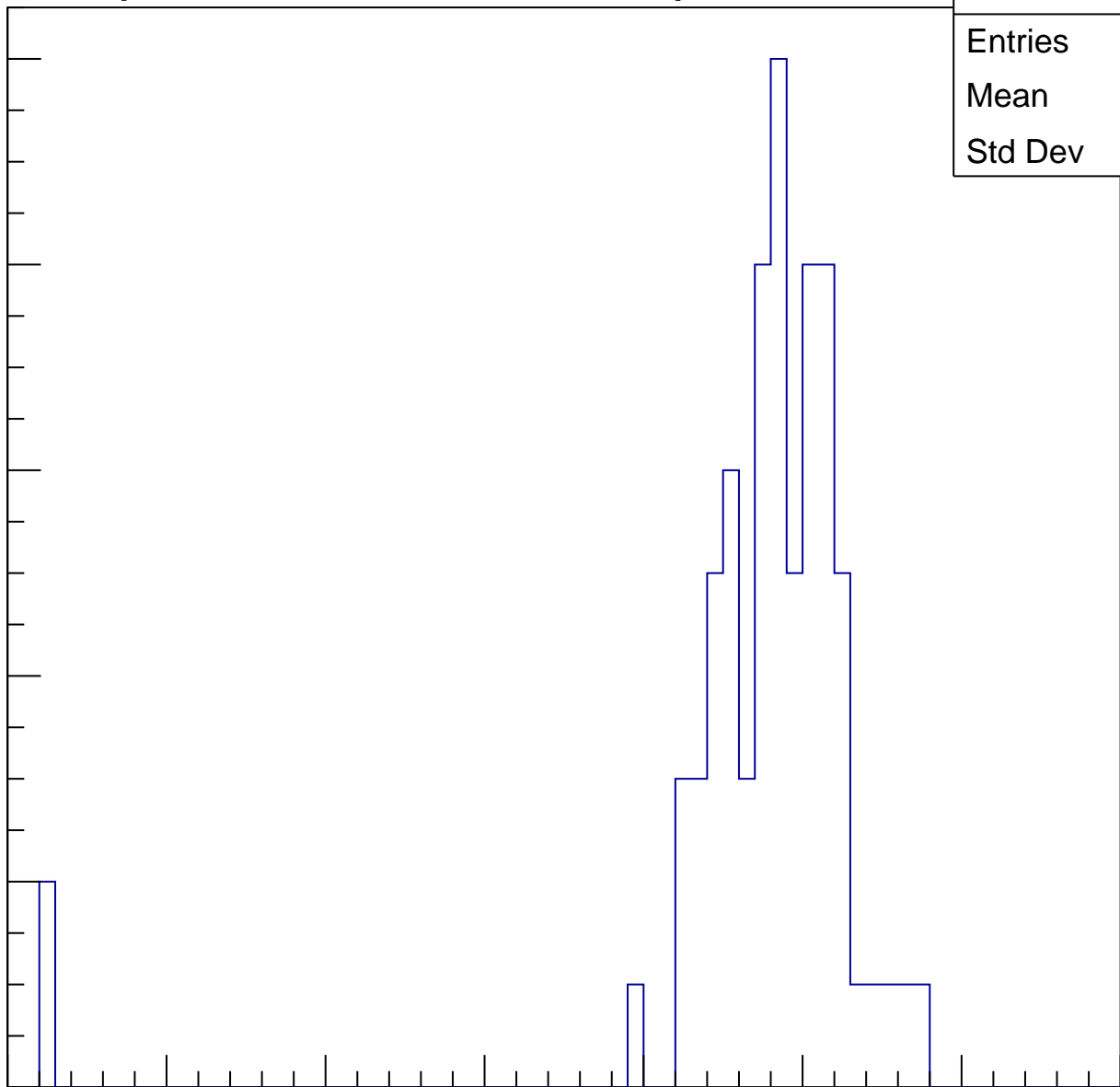
40

50

60

70

ampl

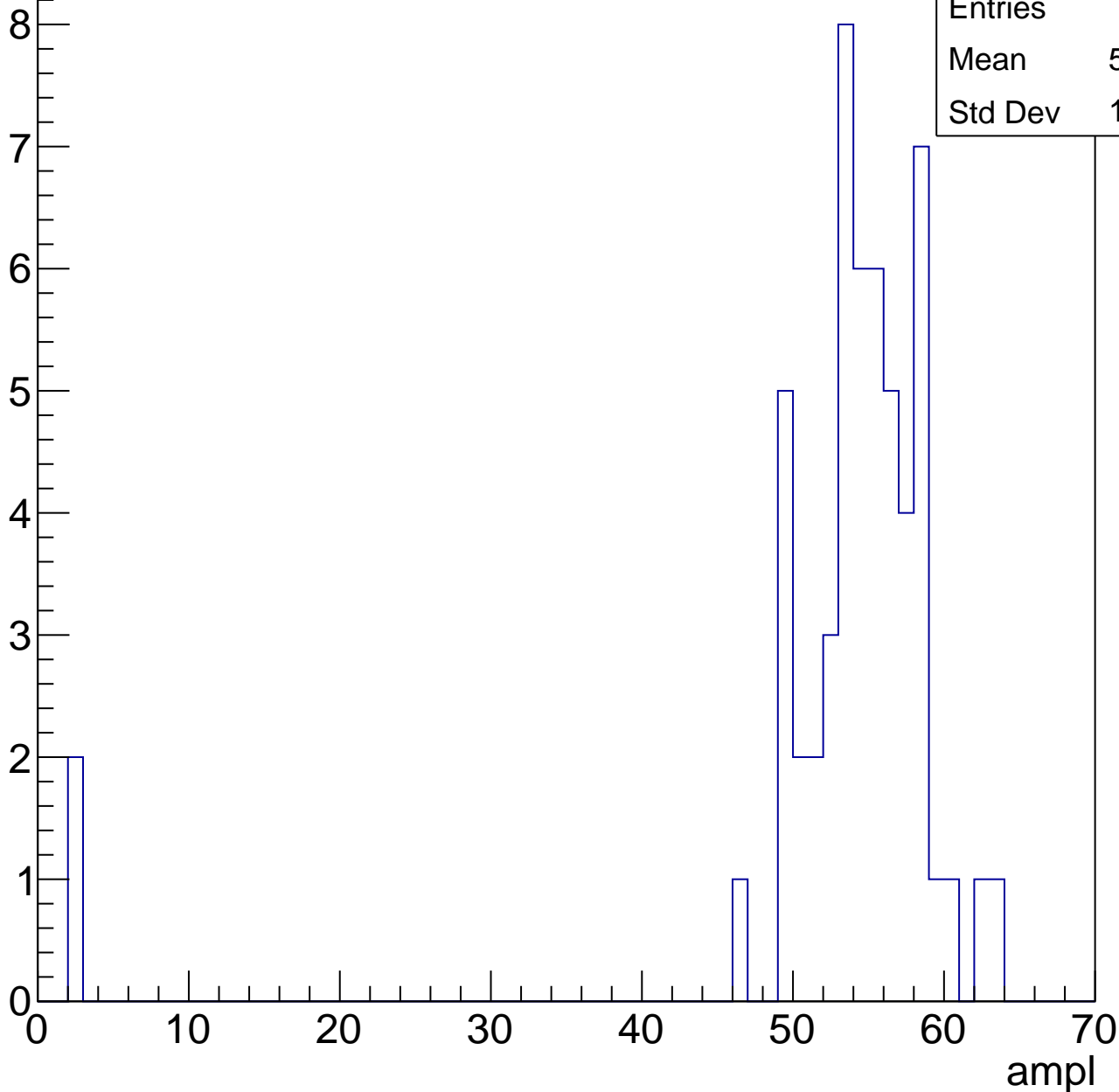


# B1L103S, U26-ch82, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

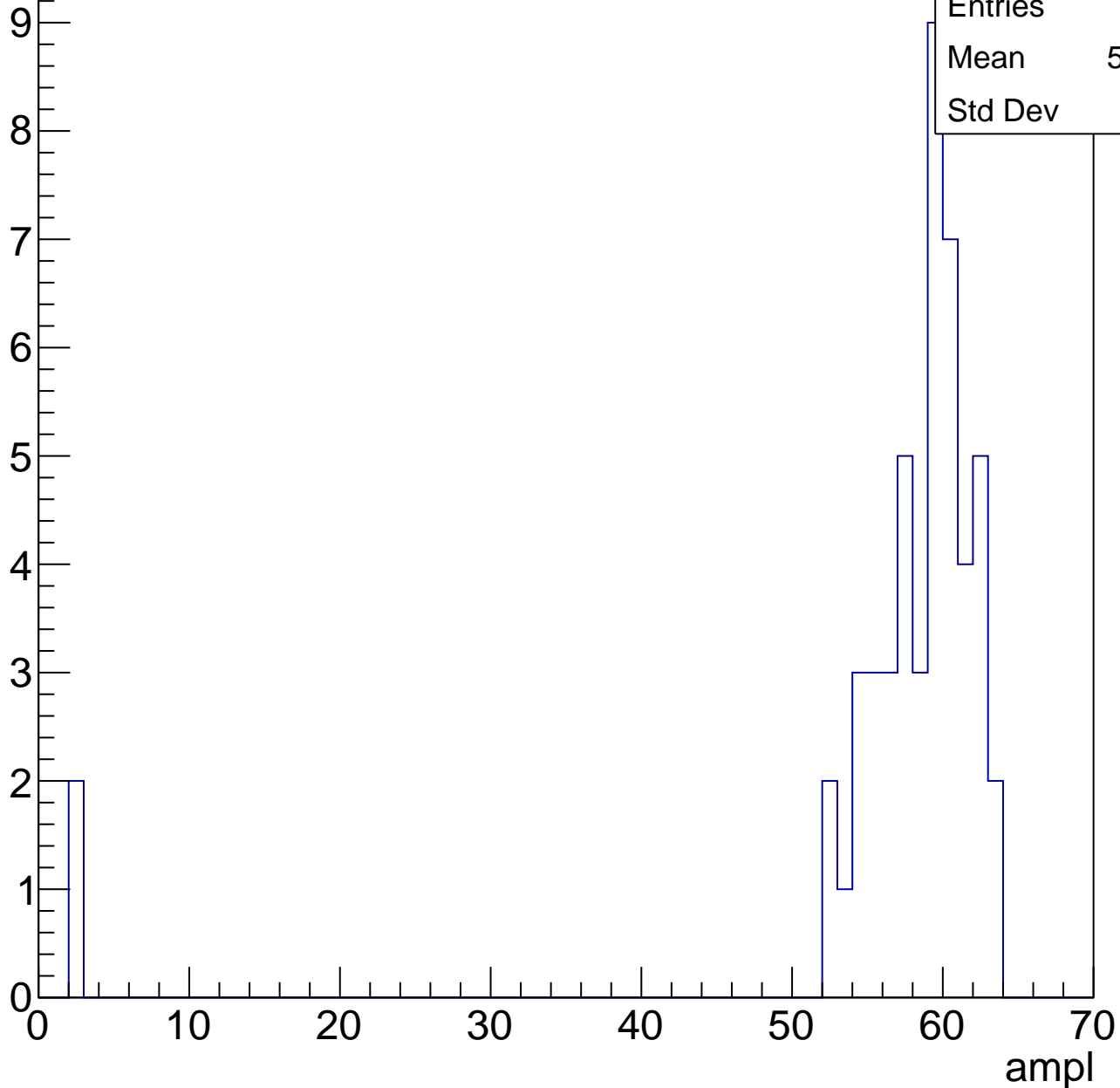
Entries	55
Mean	52.53
Std Dev	10.38



# B1L103S, U26-ch82, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

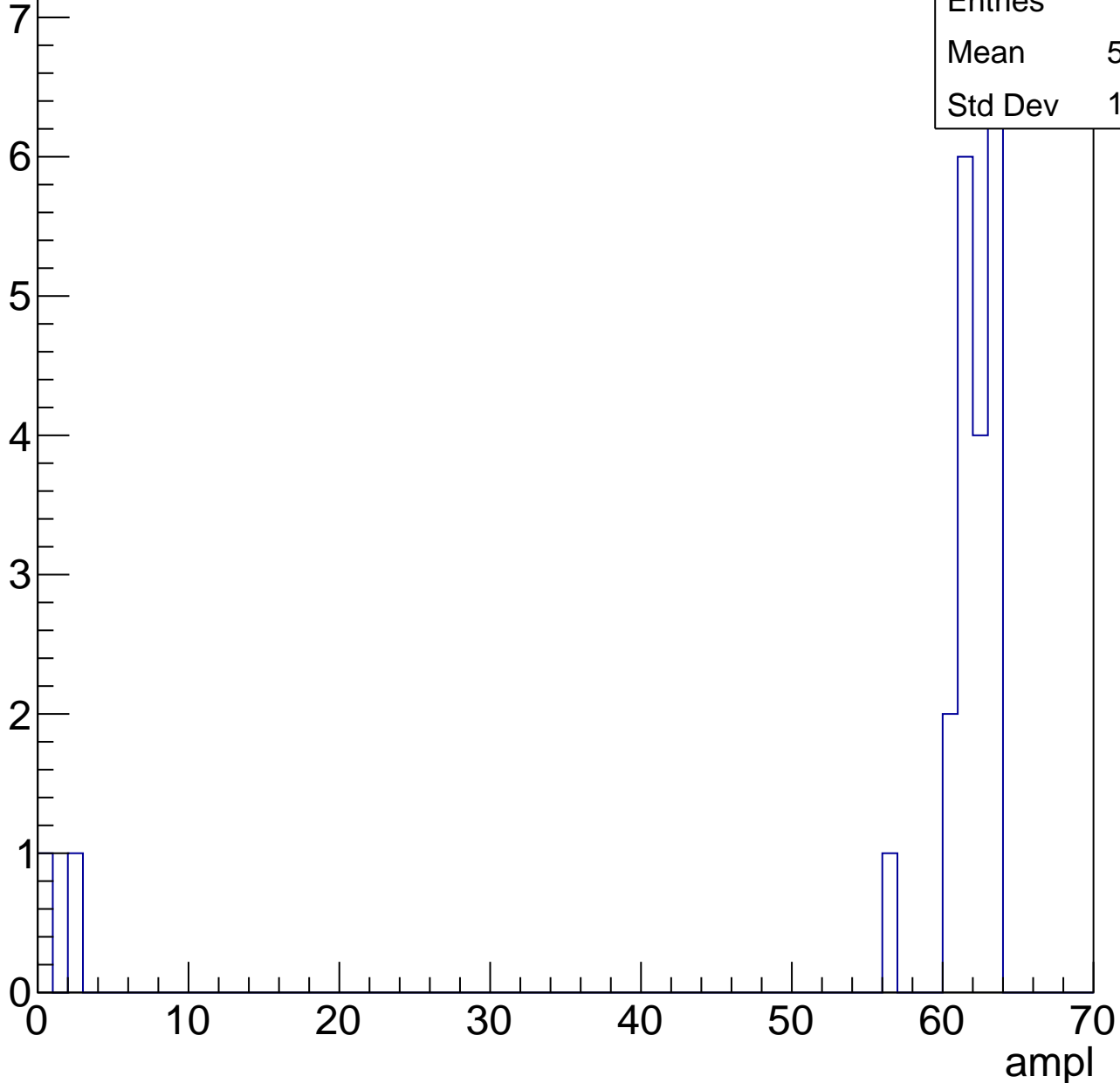


# B1L103S, U26-ch82, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	22
Mean	56.05
Std Dev	17.48



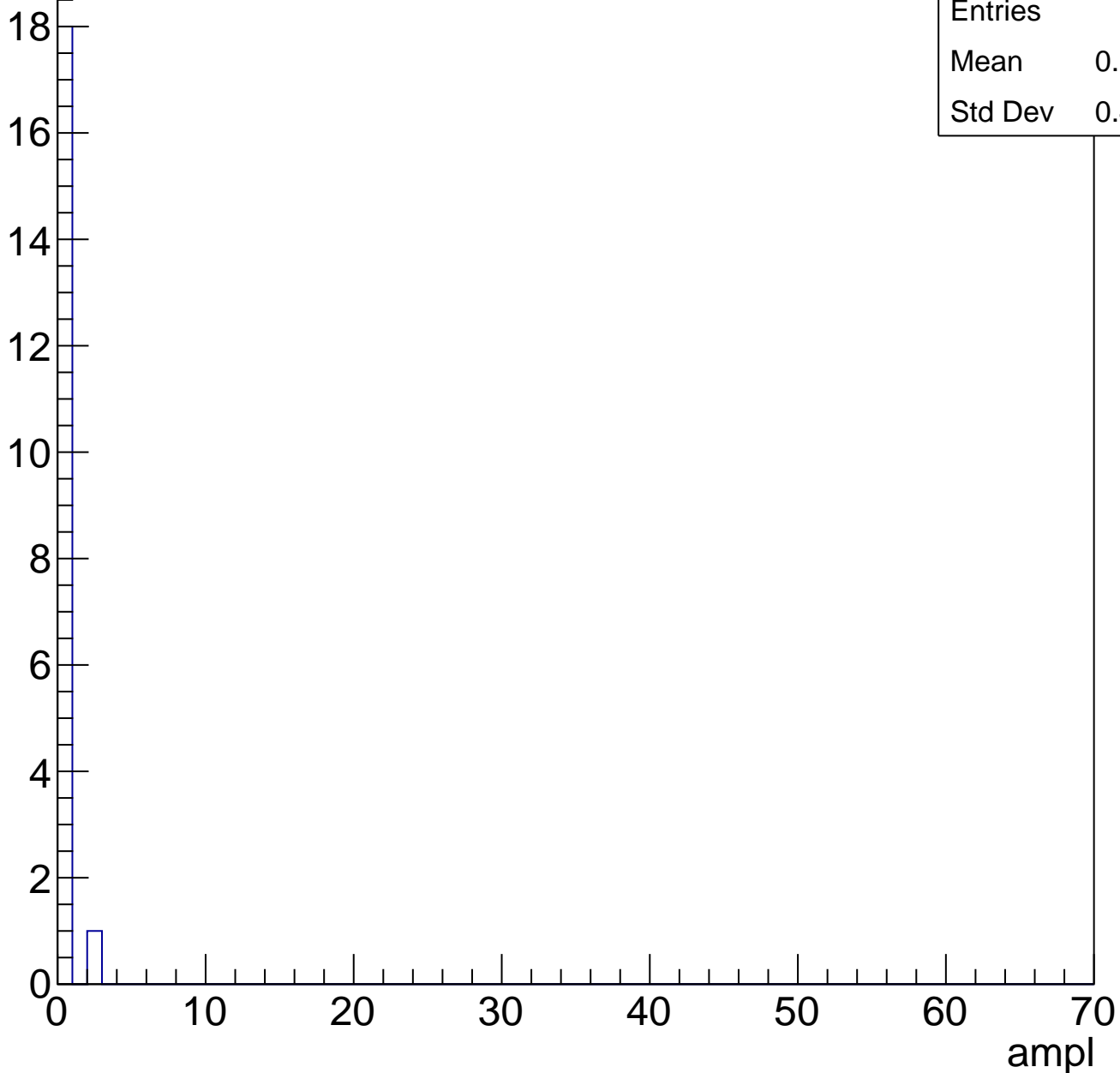


# B1L103S, U26-ch82, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	19
Mean	0.1053
Std Dev	0.4466

Entry



# B1L103S, U26-ch83, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	71
Mean	23.14
Std Dev	11.36

**Gaus mean : 28.7941**

**Gaus Width: 3.2352**

Entry

12

10

8

6

4

2

0

0

10

20

30

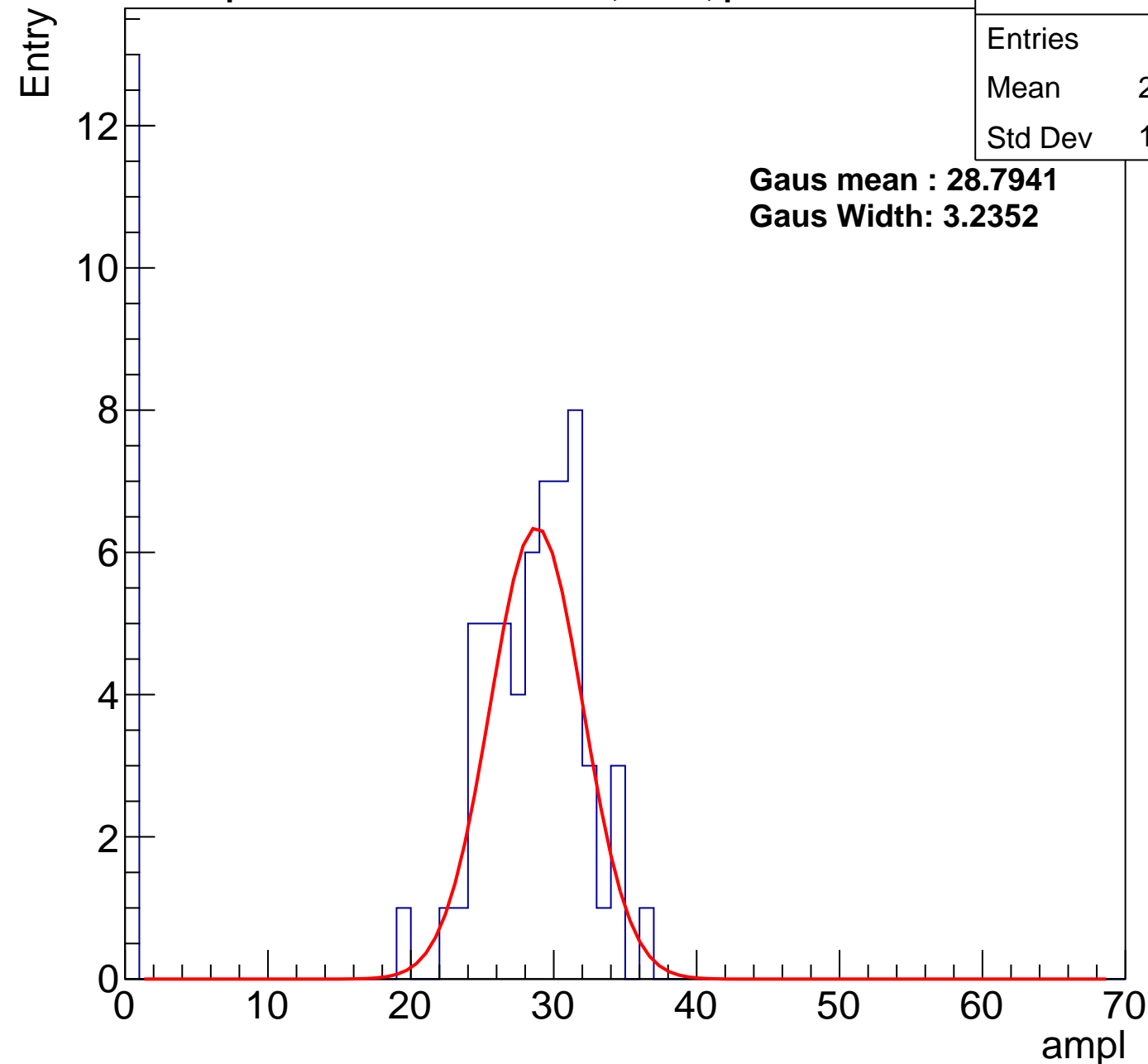
40

50

60

70

ampl



# B1L103S, U26-ch83, adc1

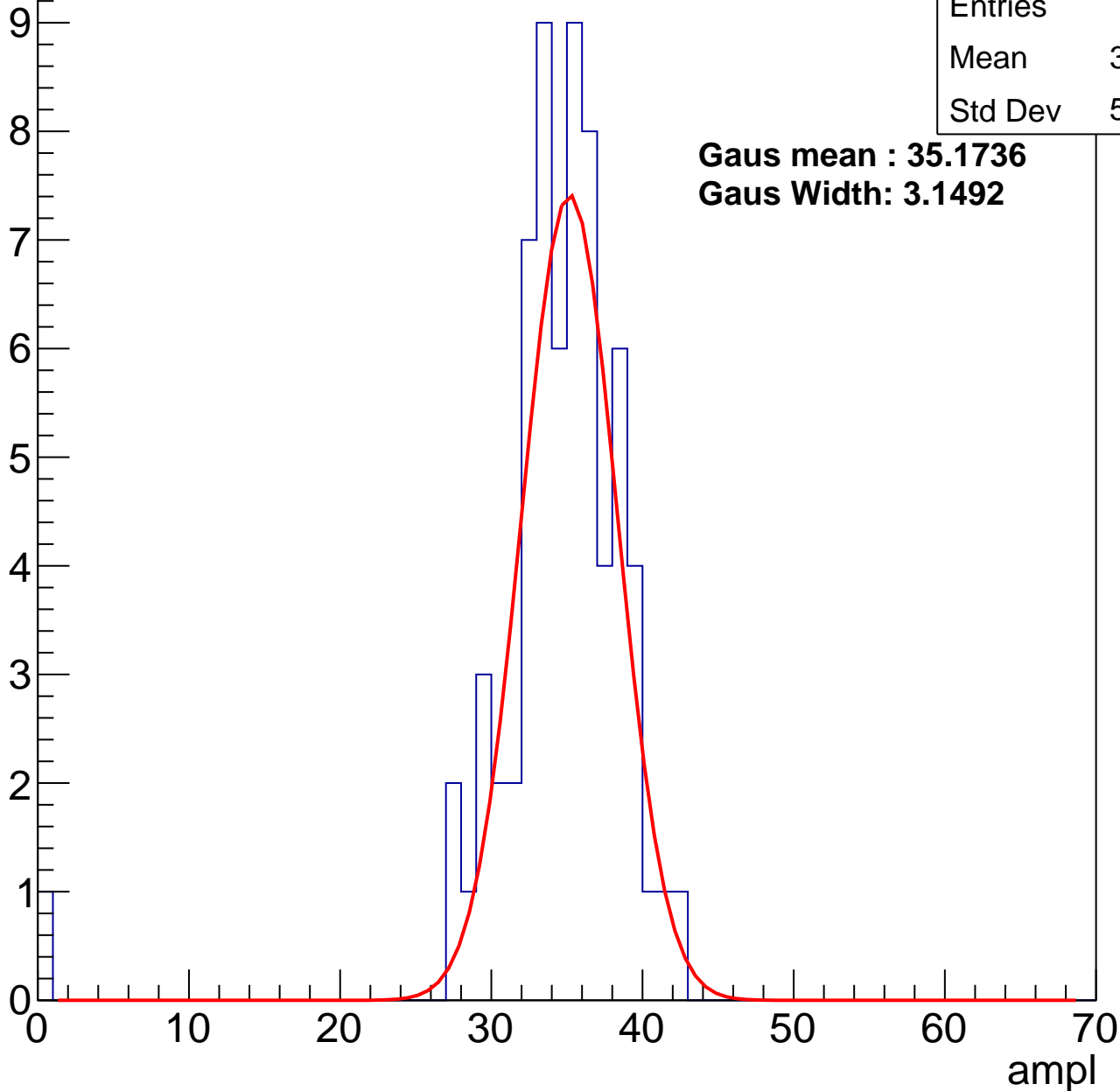
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	67
Mean	33.94
Std Dev	5.288

**Gaus mean : 35.1736**

**Gaus Width: 3.1492**



# B1L103S, U26-ch83, adc2

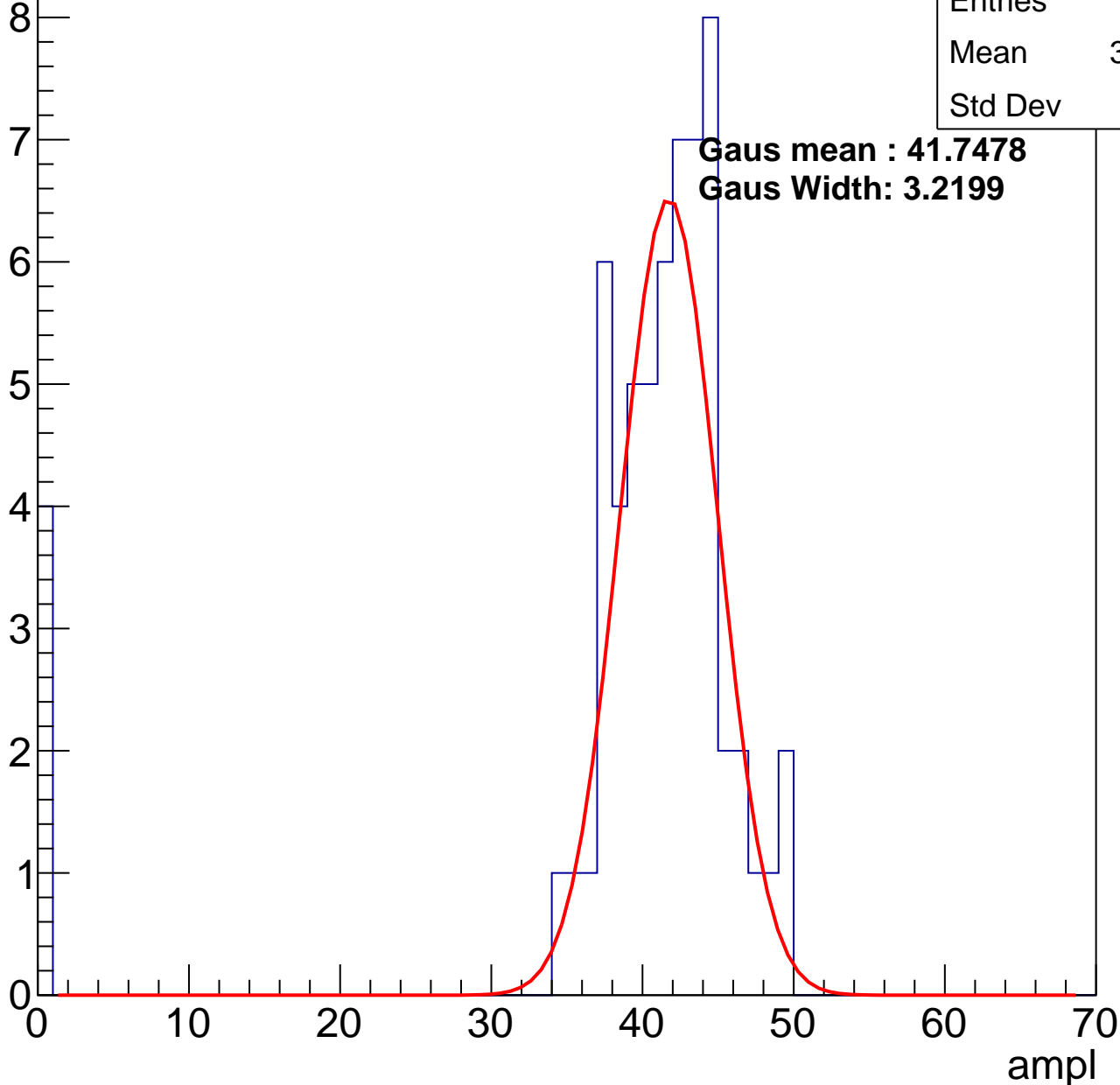
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	63
Mean	38.76
Std Dev	10.6

**Gaus mean : 41.7478**

**Gaus Width: 3.2199**

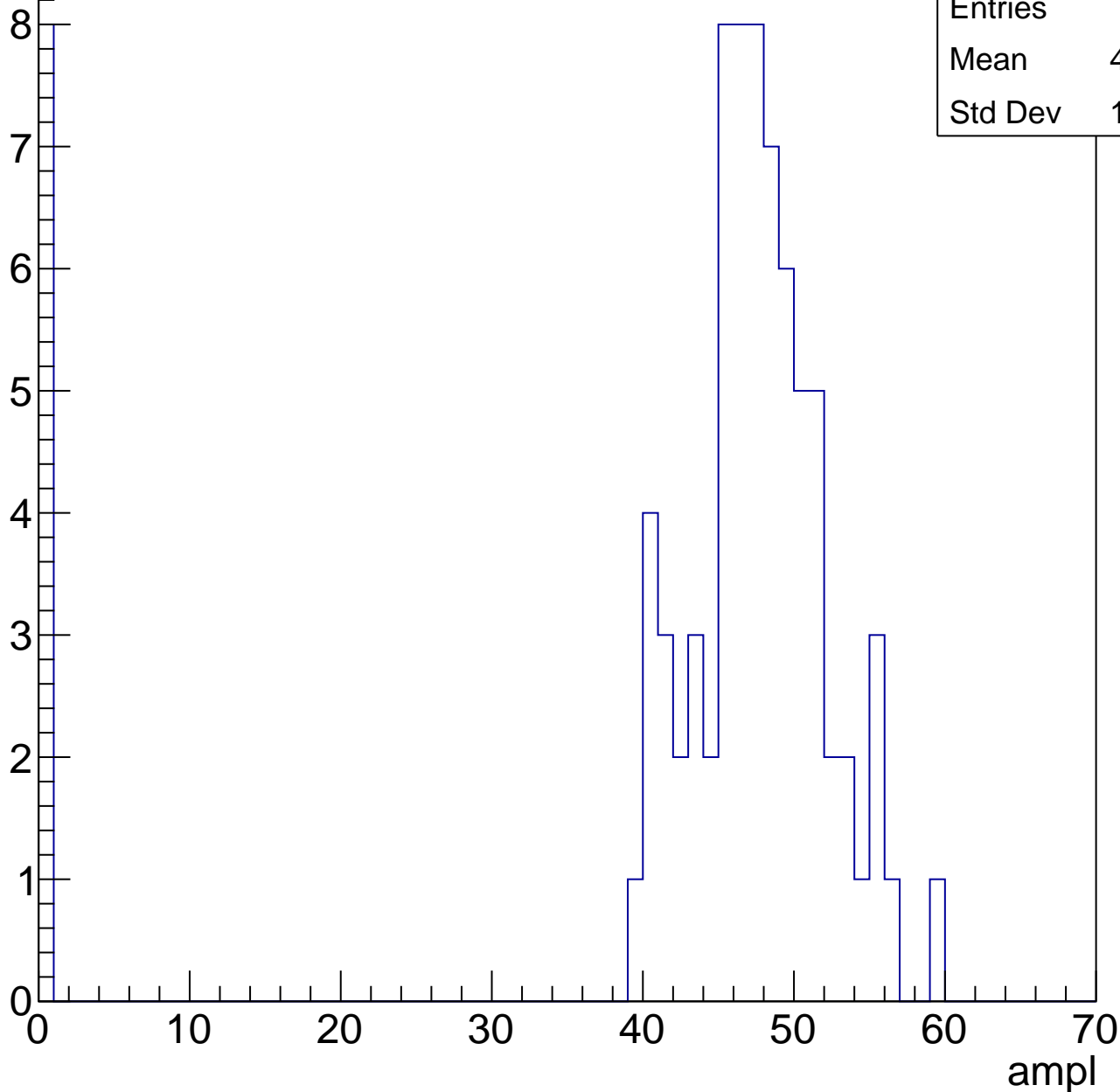


# B1L103S, U26-ch83, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	80
Mean	42.58
Std Dev	14.74

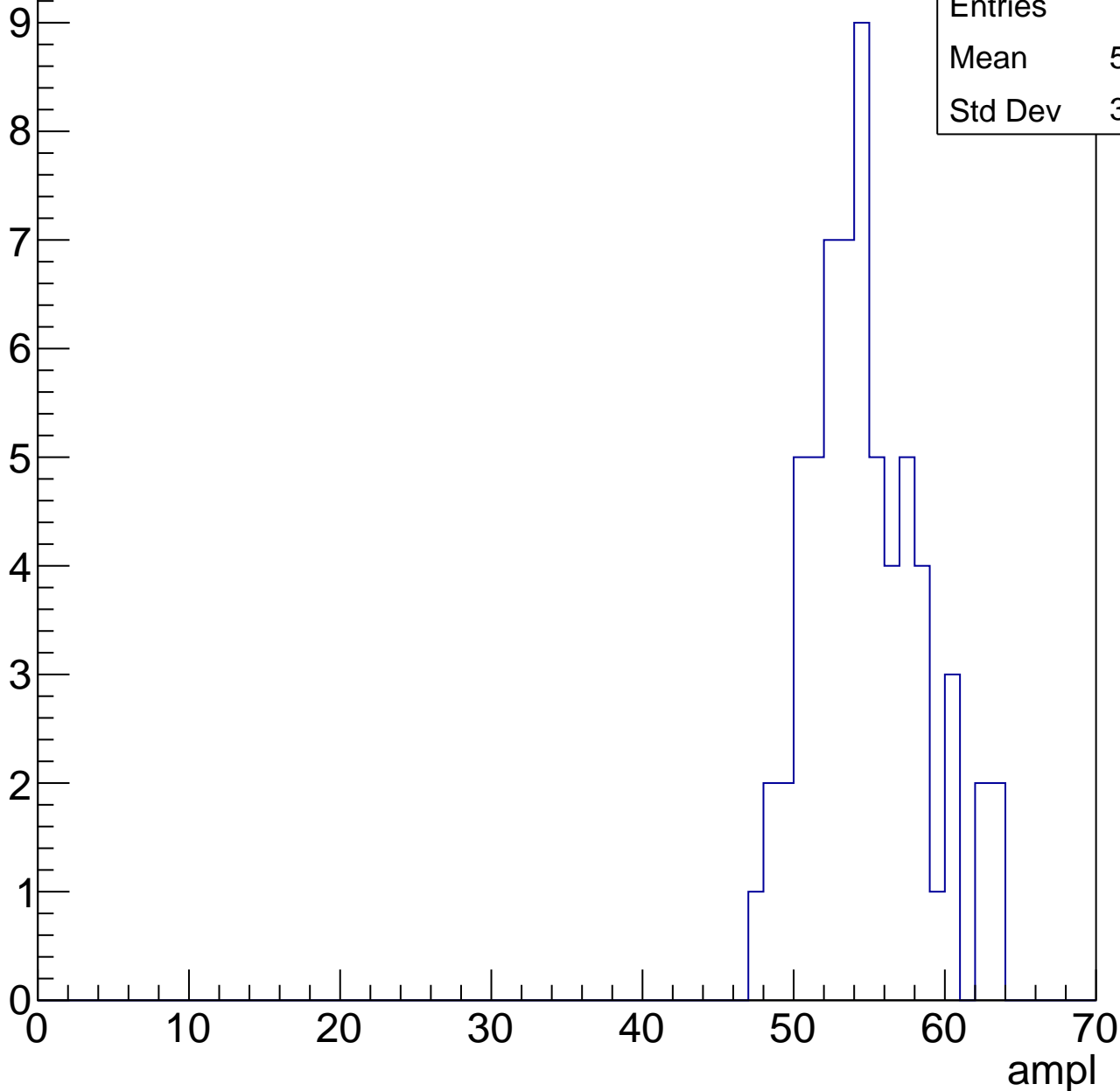


# B1L103S, U26-ch83, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

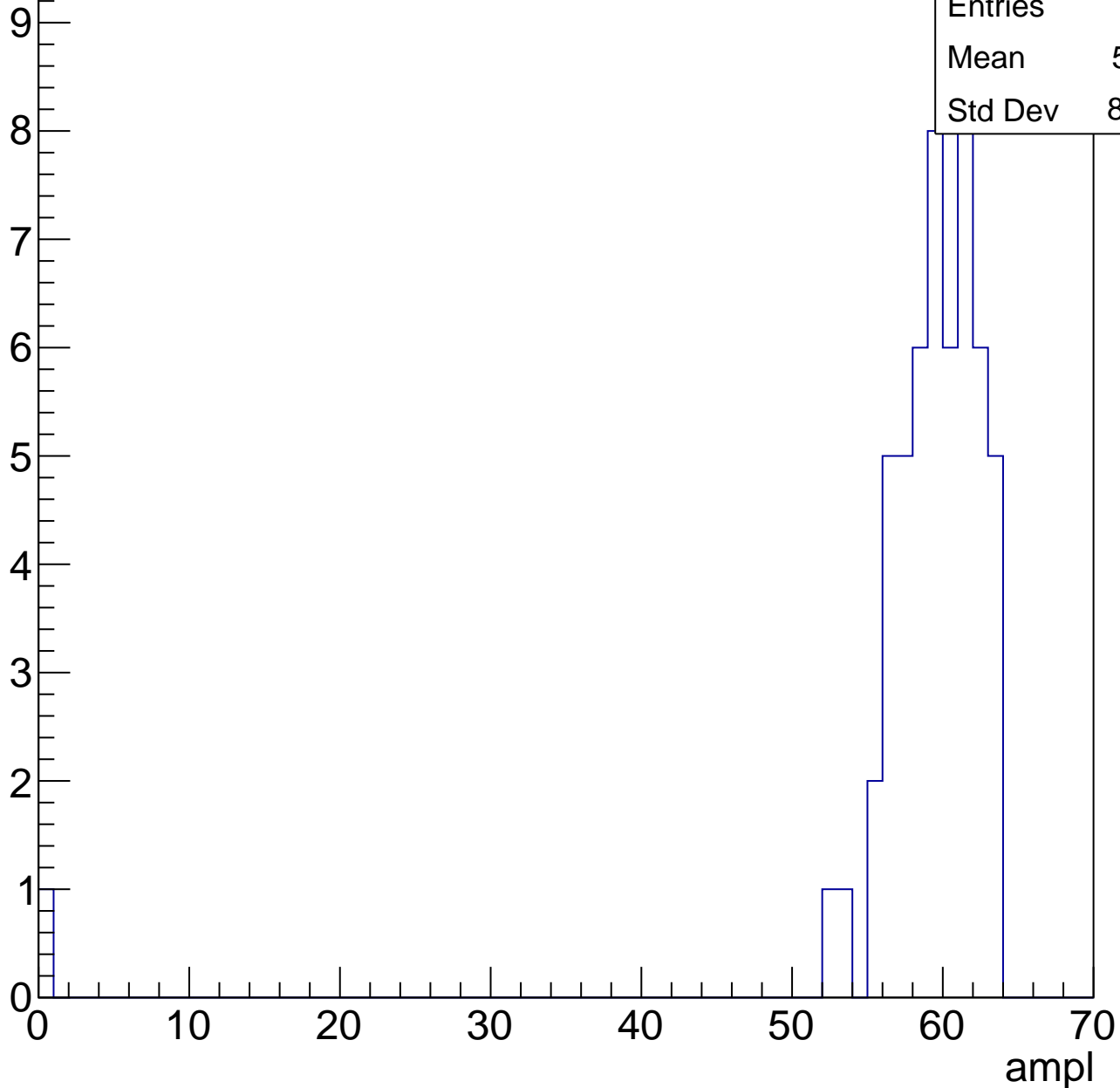
Entries	64
Mean	54.25
Std Dev	3.708



# B1L103S, U26-ch83, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



# B1L103S, U26-ch83, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

3

2.5

2

1.5

1

0.5

0

0

10

20

30

40

50

60

70

ampl

Entries

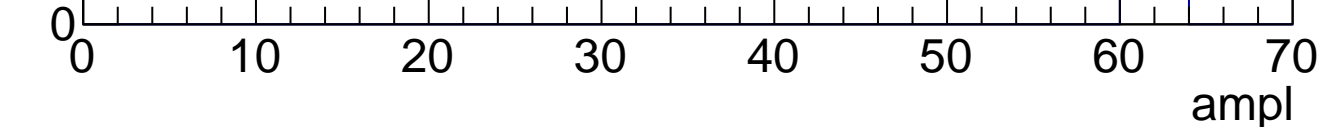
7

Mean

62

Std Dev

1.069





# B1L103S, U26-ch83, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



# B1L103S, U26-ch84, adc0

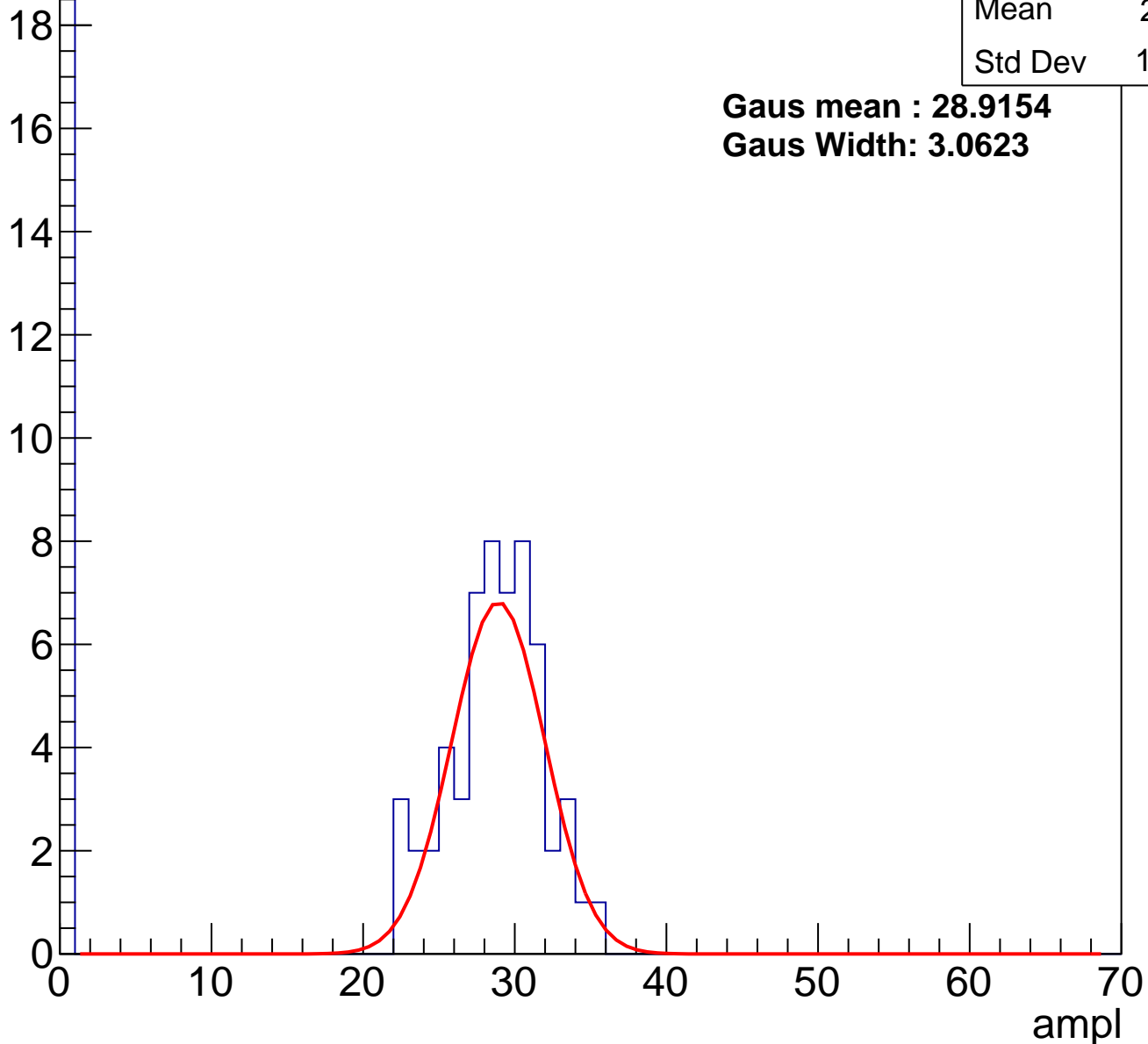
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	76
Mean	21.21
Std Dev	12.53

**Gaus mean : 28.9154**

**Gaus Width: 3.0623**

Entry



# B1L103S, U26-ch84, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	78
Mean	29.13
Std Dev	13.36

**Gaus mean : 35.3994**

**Gaus Width: 3.6270**

Entry

12

10

8

6

4

2

0

0

10

20

30

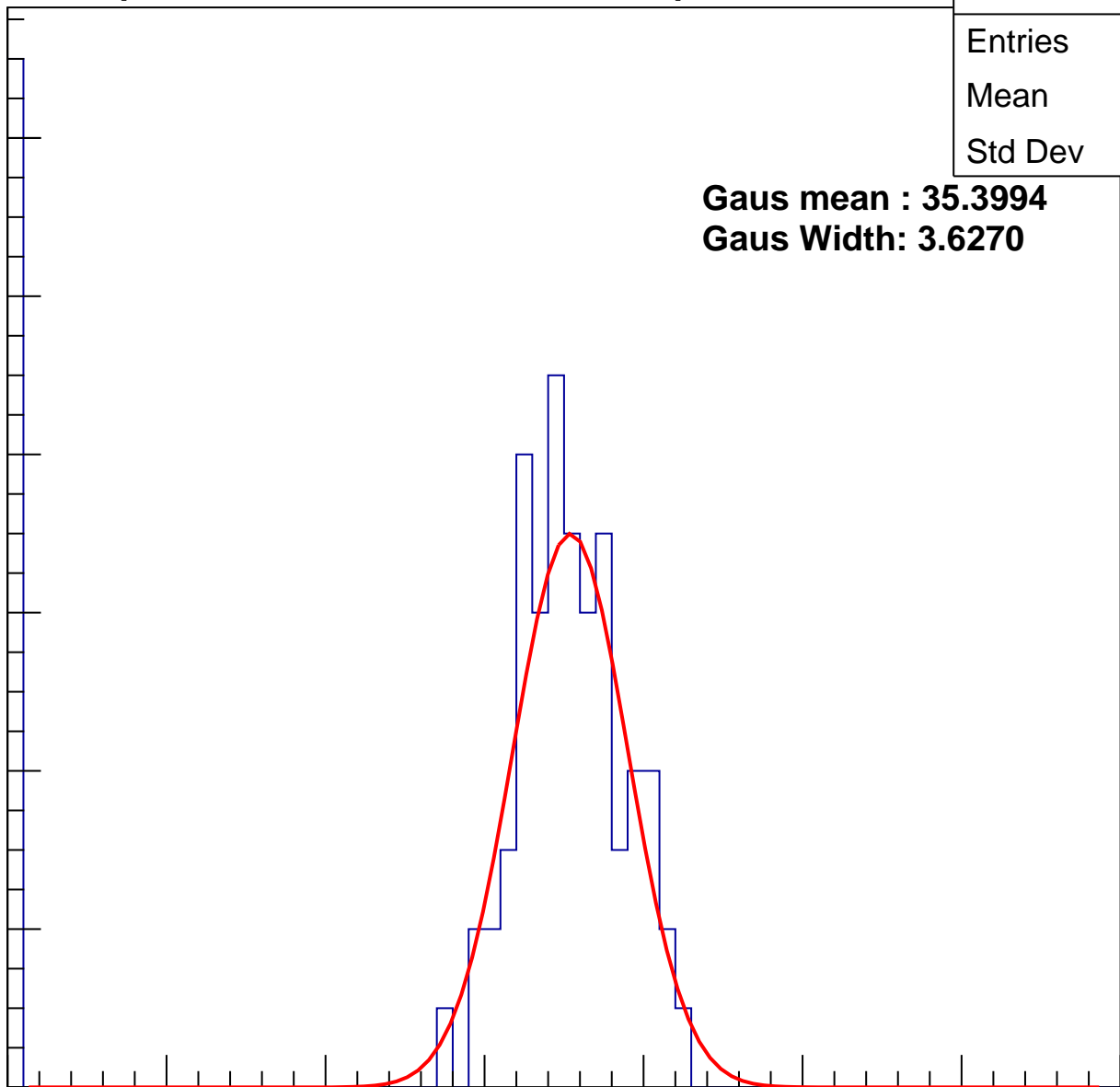
40

50

60

70

ampl



# B1L103S, U26-ch84, adc2

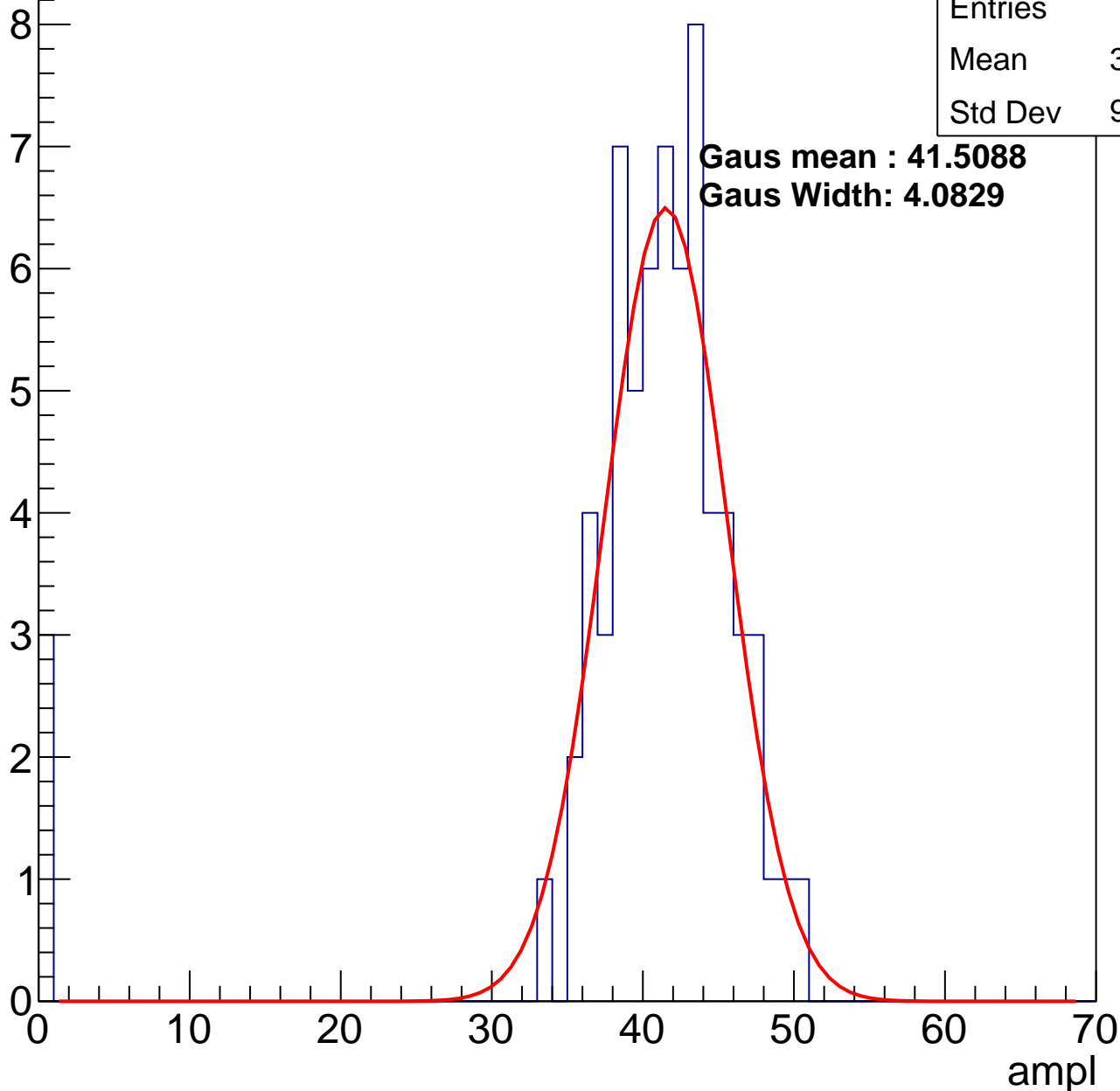
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	69
Mean	39.48
Std Dev	9.146

**Gaus mean : 41.5088**

**Gaus Width: 4.0829**

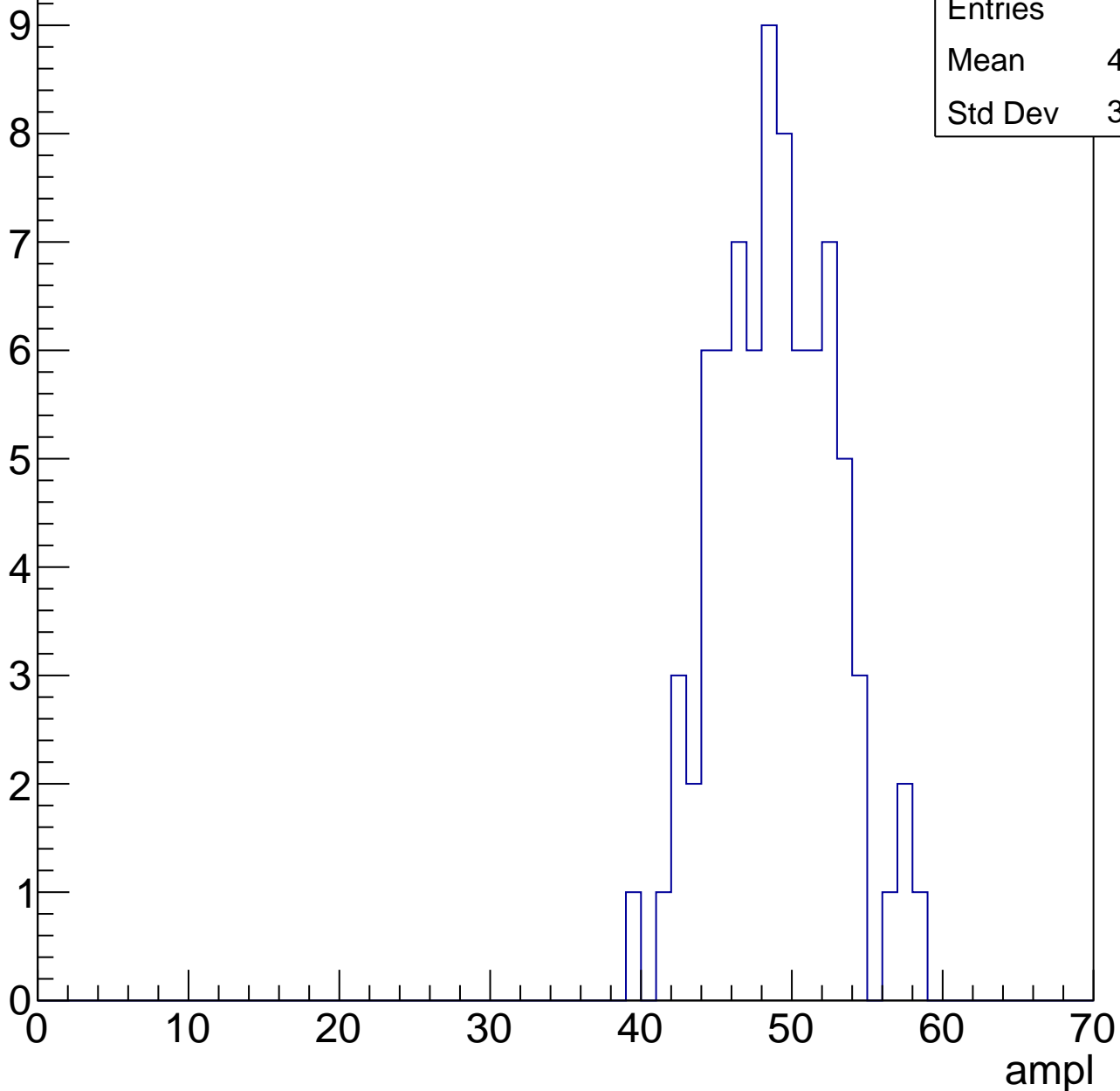


# B1L103S, U26-ch84, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	80
Mean	48.49
Std Dev	3.889

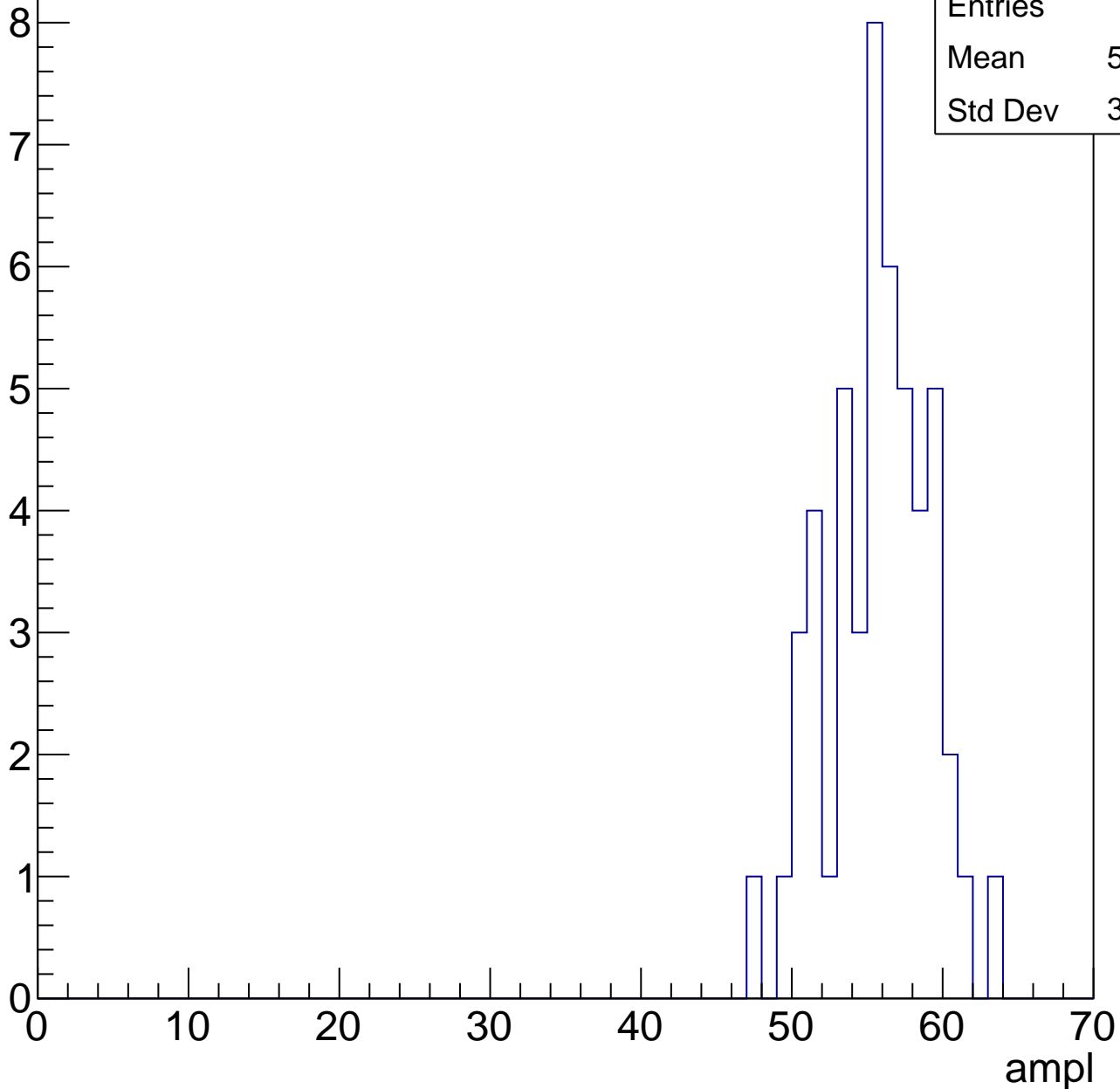


# B1L103S, U26-ch84, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	50
Mean	55.22
Std Dev	3.348



# B1L103S, U26-ch84, adc5

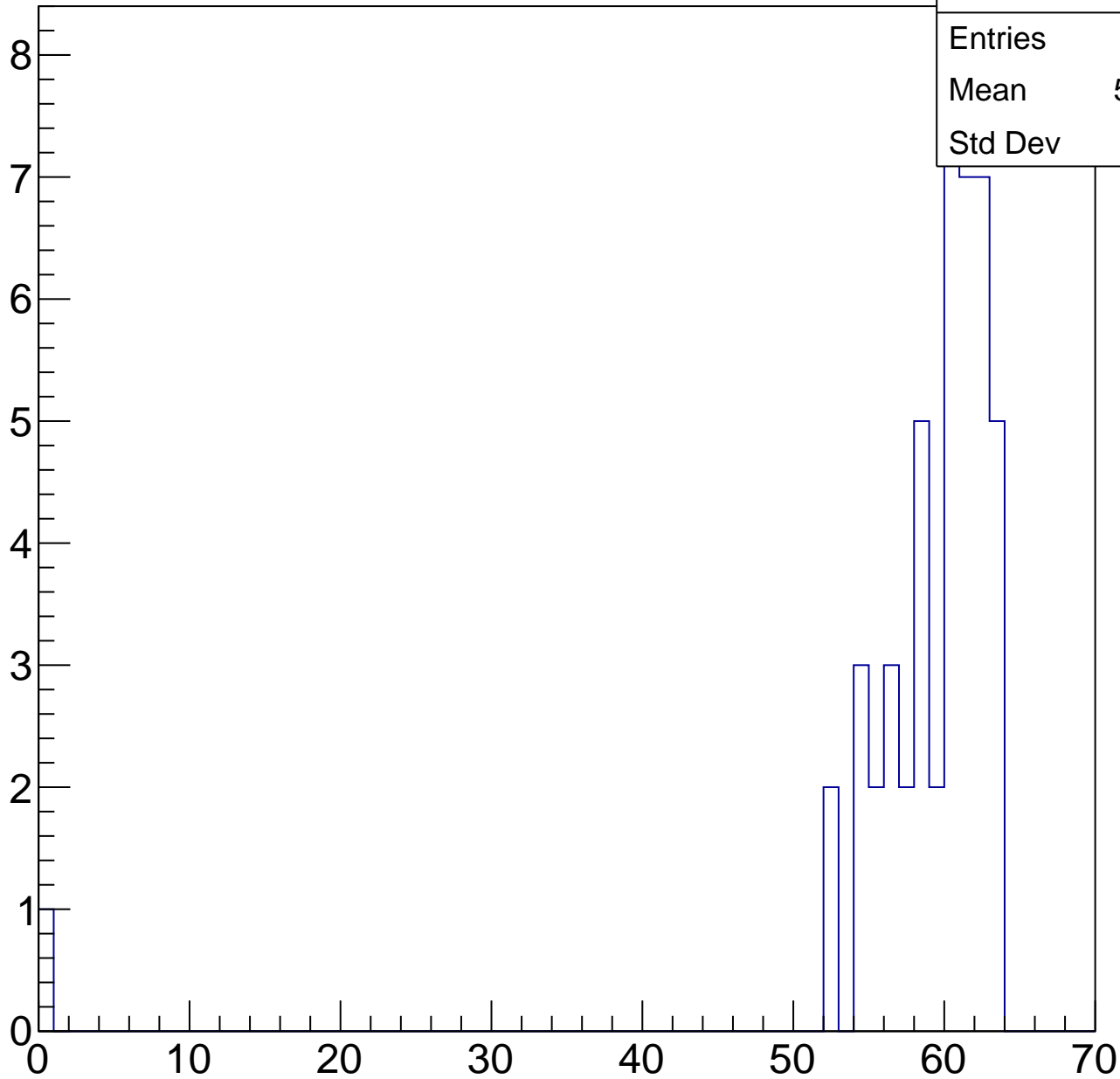
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	47
Mean	57.91
Std Dev	9.05

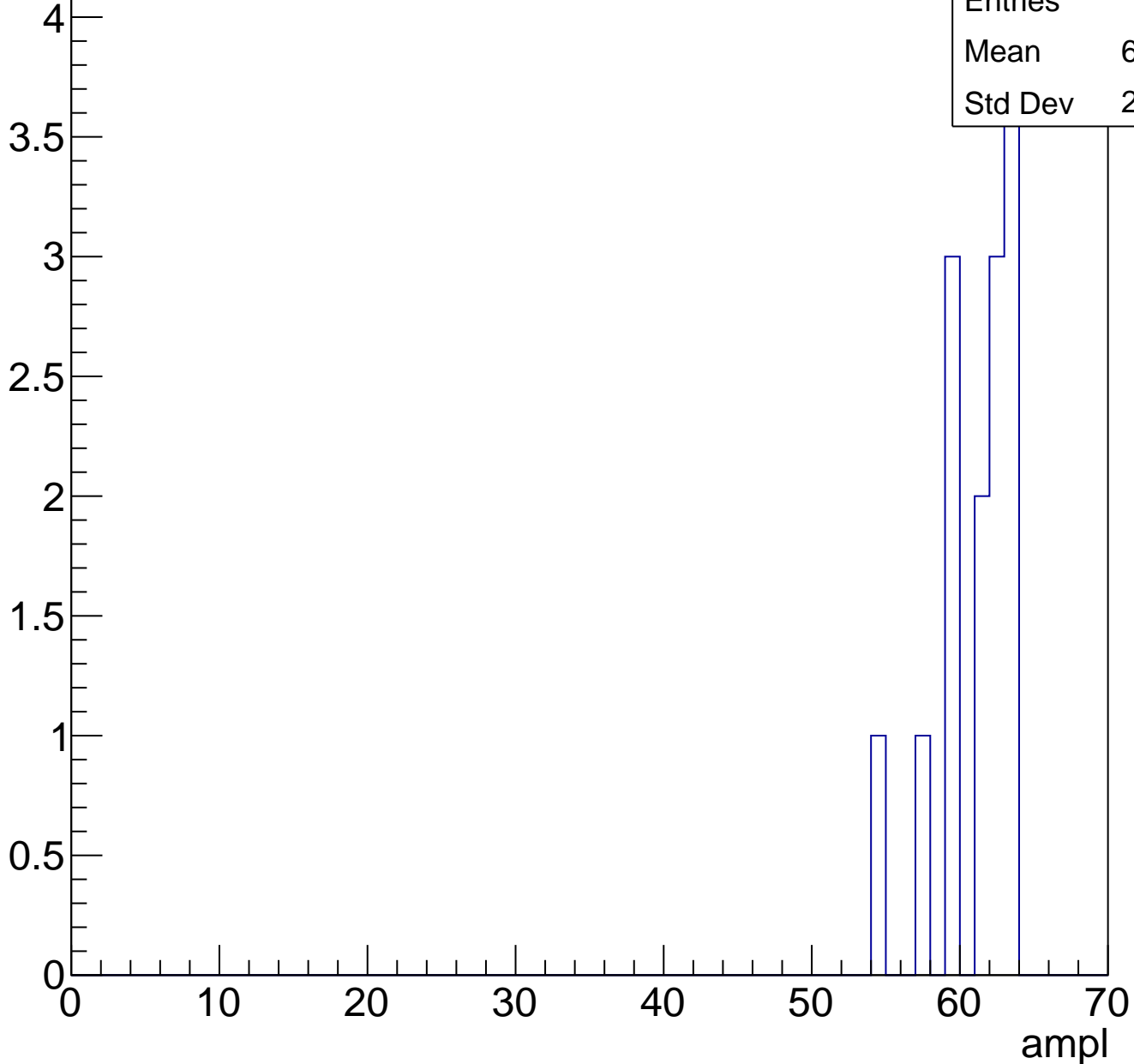
ampl



# B1L103S, U26-ch84, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry





# B1L103S, U26-ch84, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



# B1L103S, U26-ch85, adc0

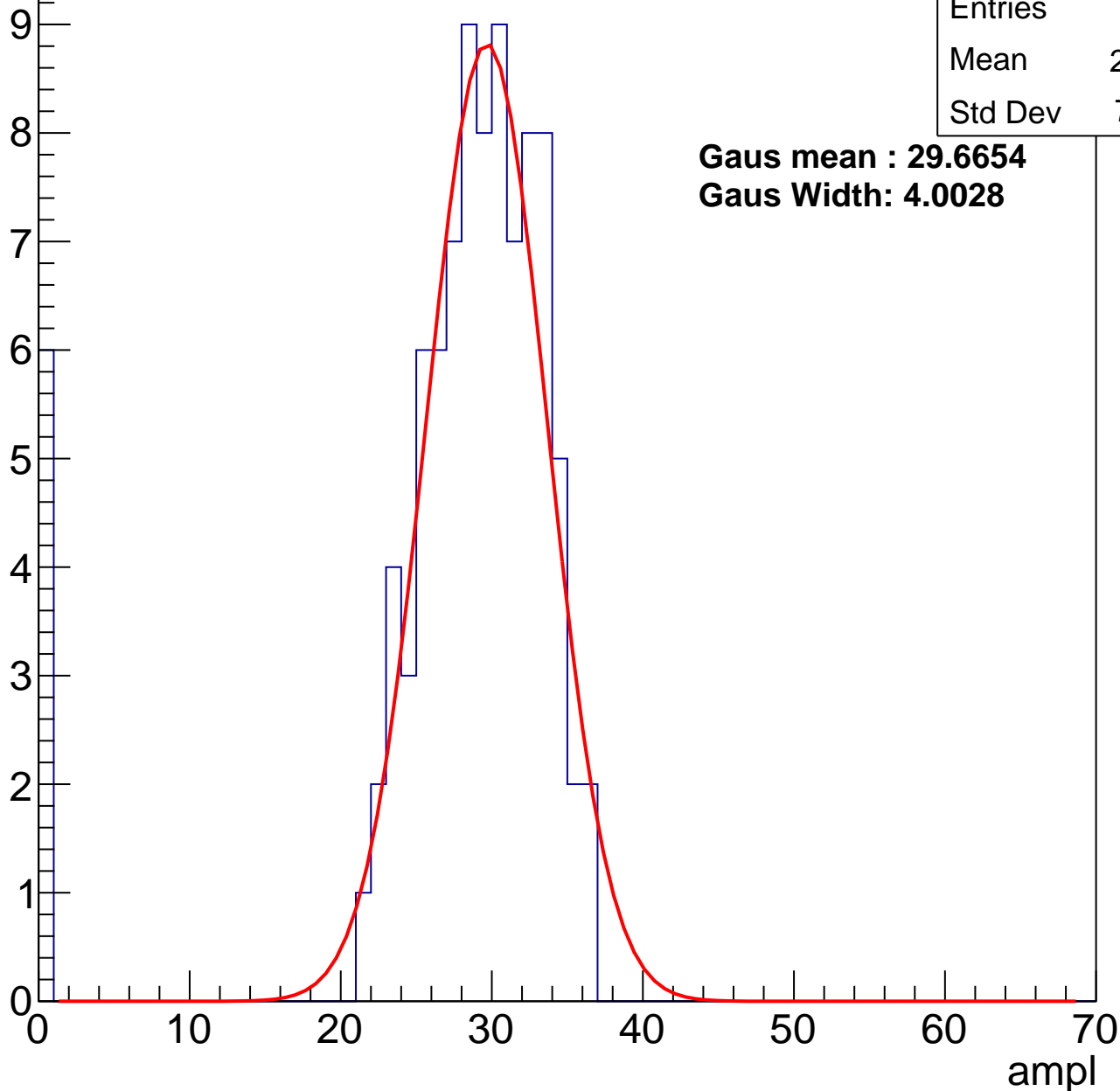
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	93
Mean	27.17
Std Dev	7.921

**Gaus mean : 29.6654**

**Gaus Width: 4.0028**



# B1L103S, U26-ch85, adc1

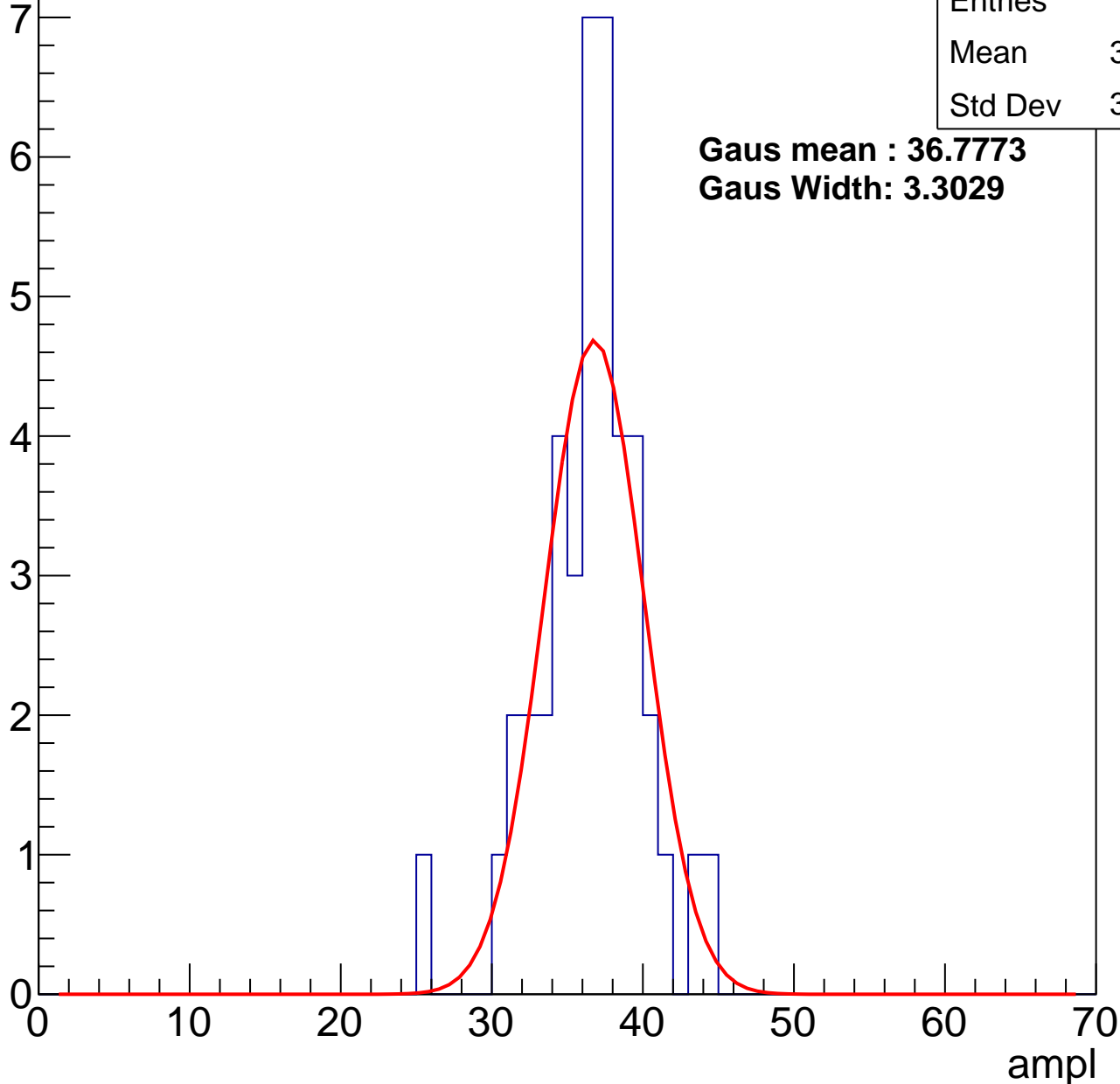
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	42
Mean	36.07
Std Dev	3.467

**Gaus mean : 36.7773**

**Gaus Width: 3.3029**



# B1L103S, U26-ch85, adc2

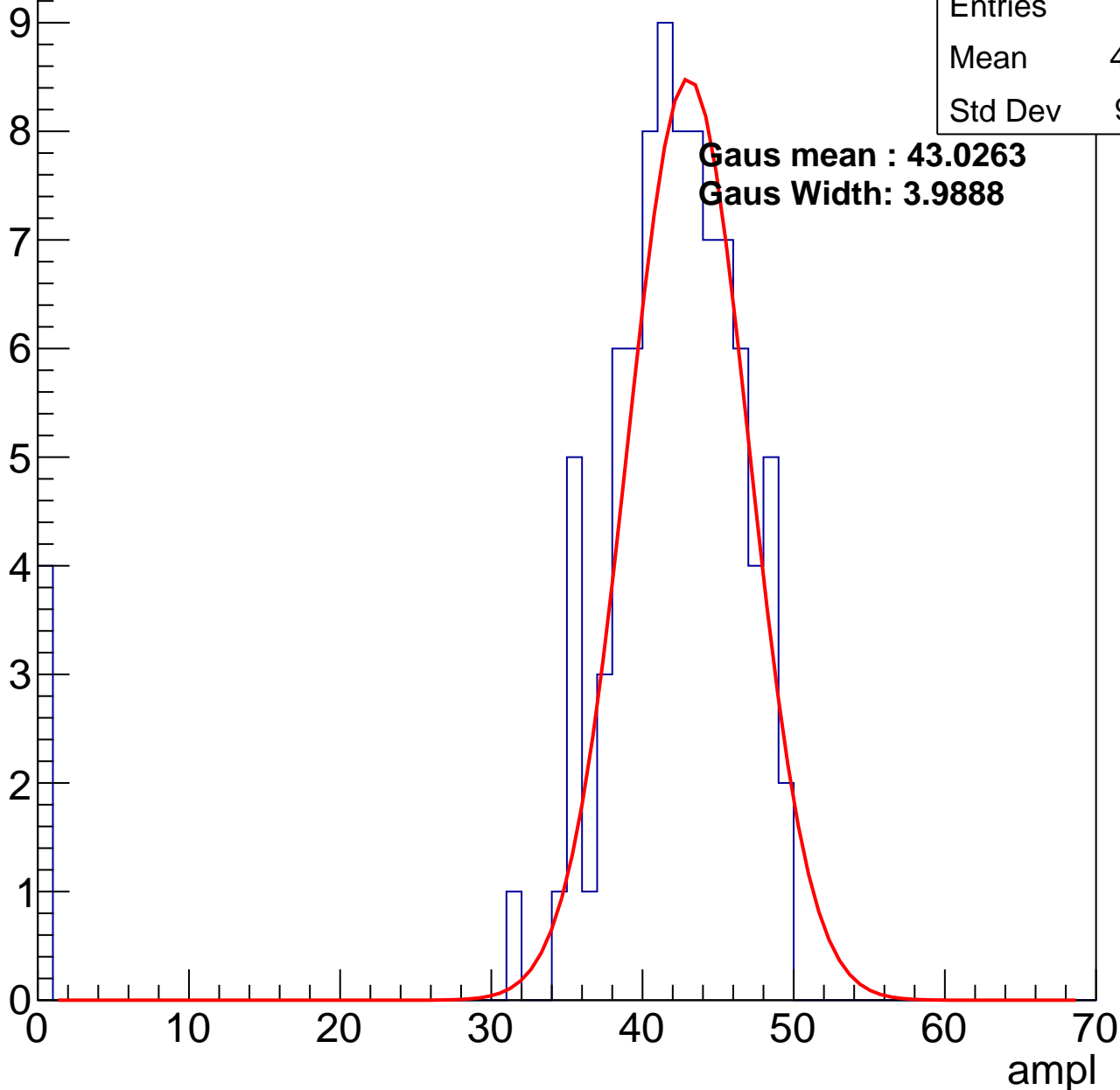
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	91
Mean	40.03
Std Dev	9.381

**Gaus mean : 43.0263**

**Gaus Width: 3.9888**

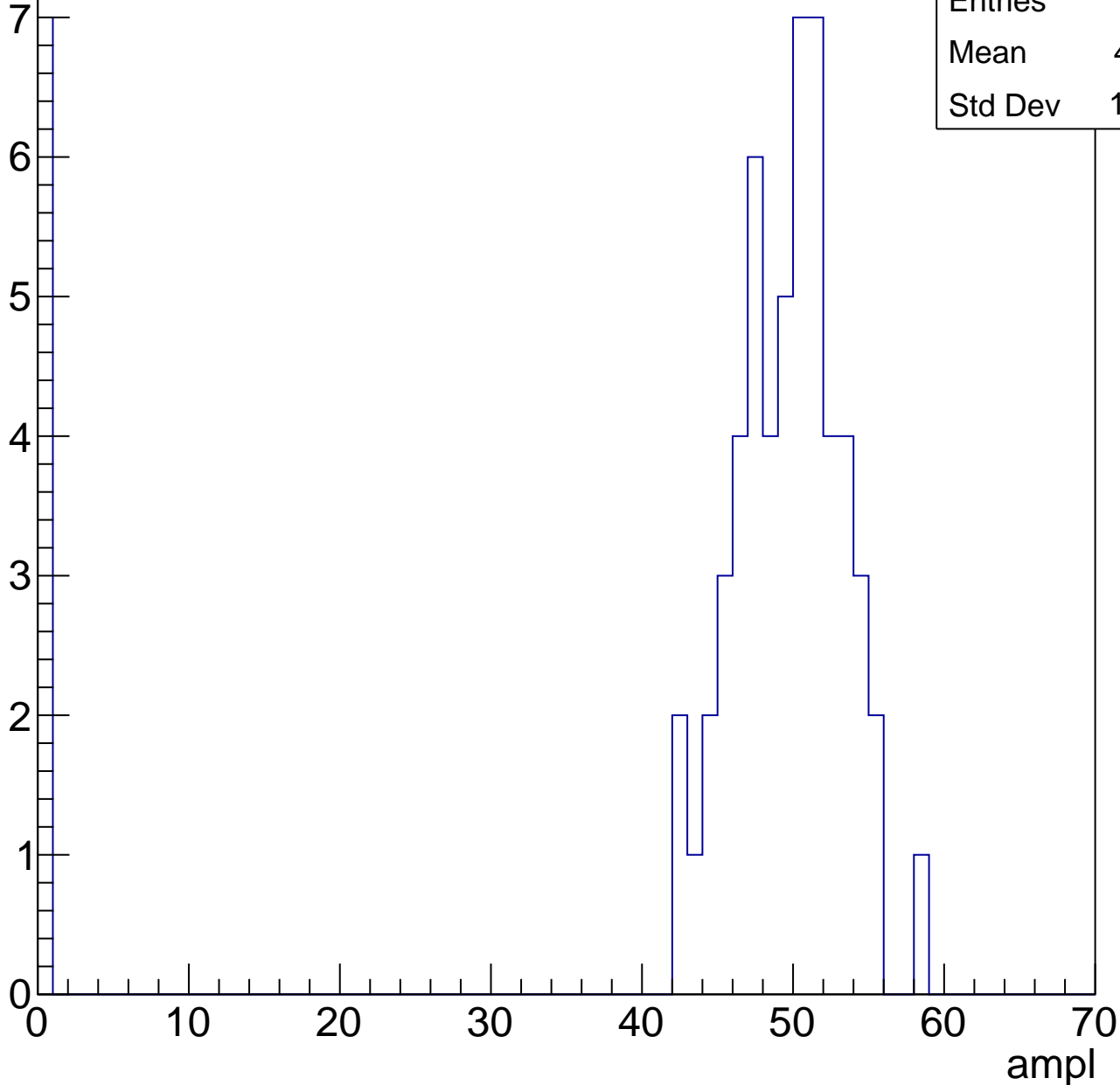


# B1L103S, U26-ch85, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

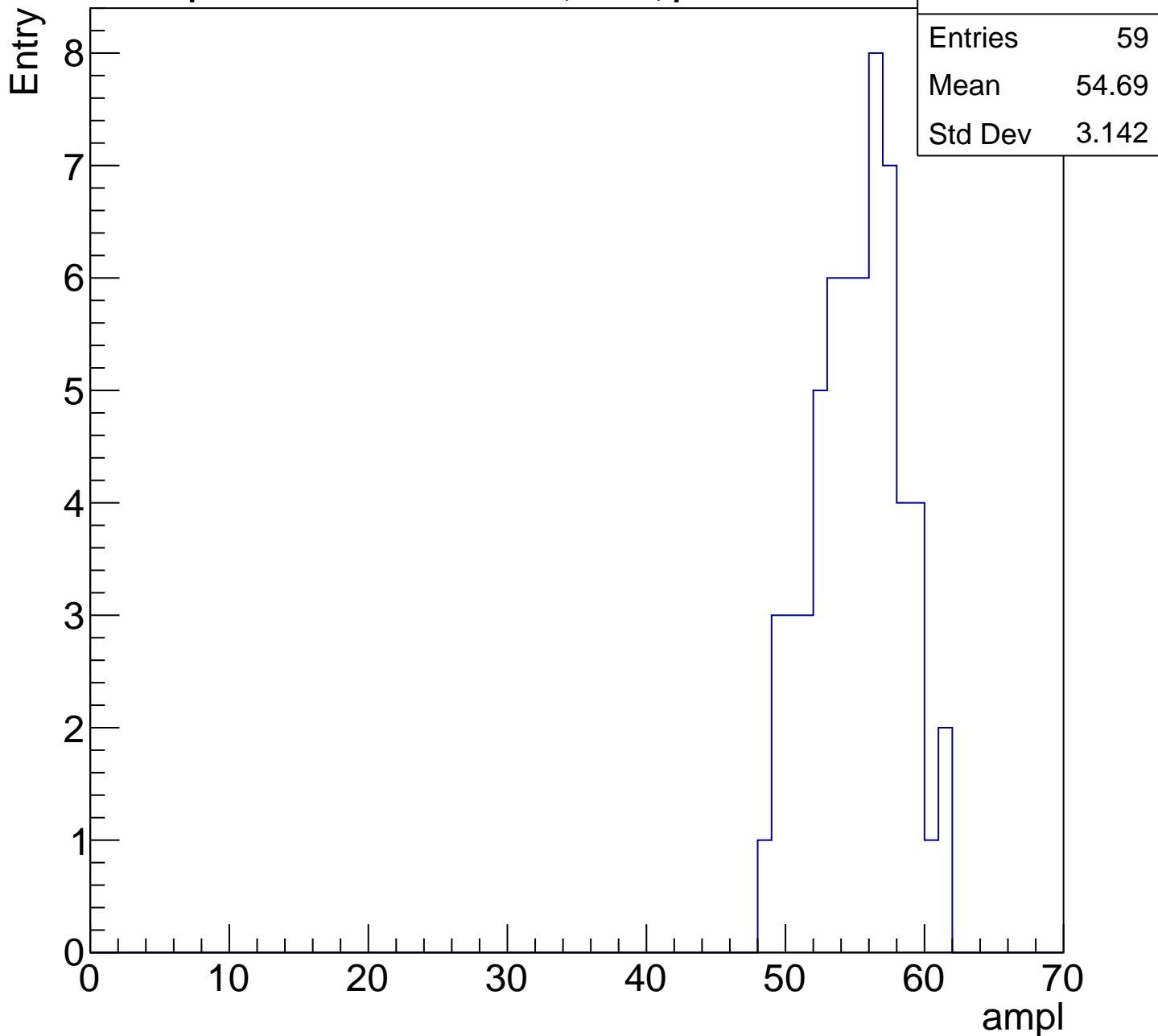
Entry

Entries	62
Mean	43.71
Std Dev	15.93



# B1L103S, U26-ch85, adc4

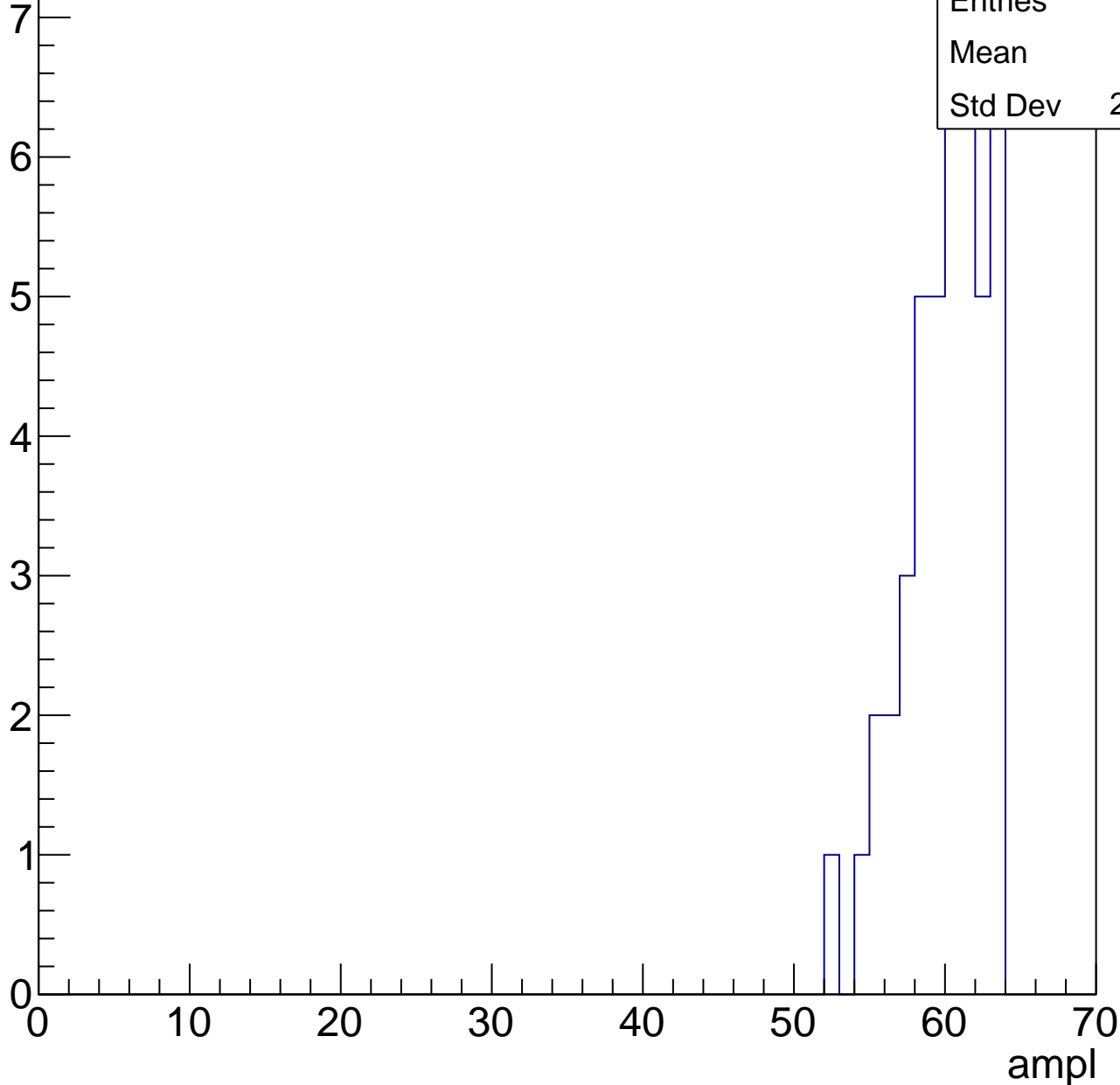
calib\_packv5\_041523\_1651.root, FC#0, port C2



# B1L103S, U26-ch85, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

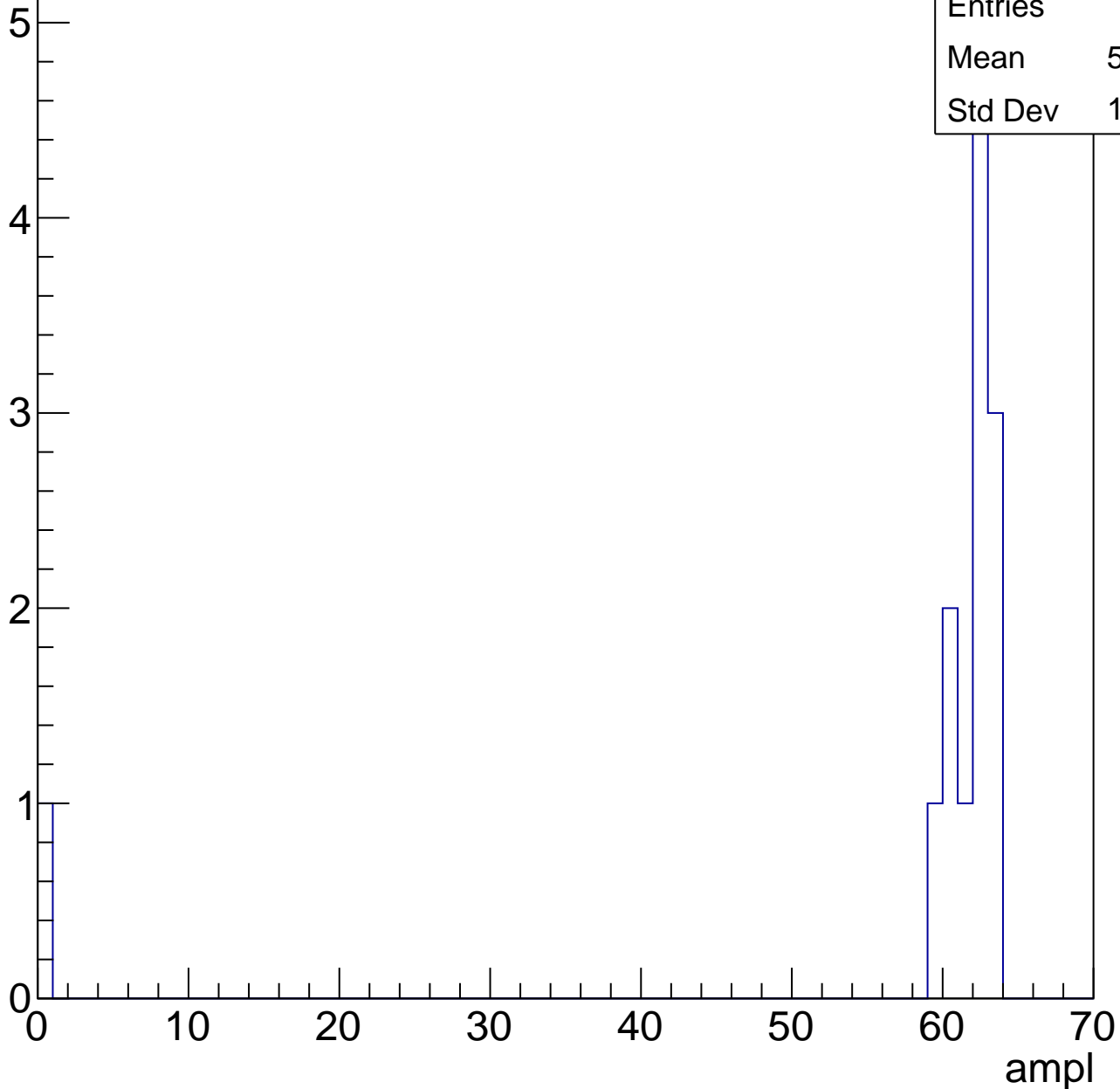


# B1L103S, U26-ch85, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	13
Mean	56.85
Std Dev	16.45





# B1L103S, U26-ch85, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



# B1L103S, U26-ch86, adc0

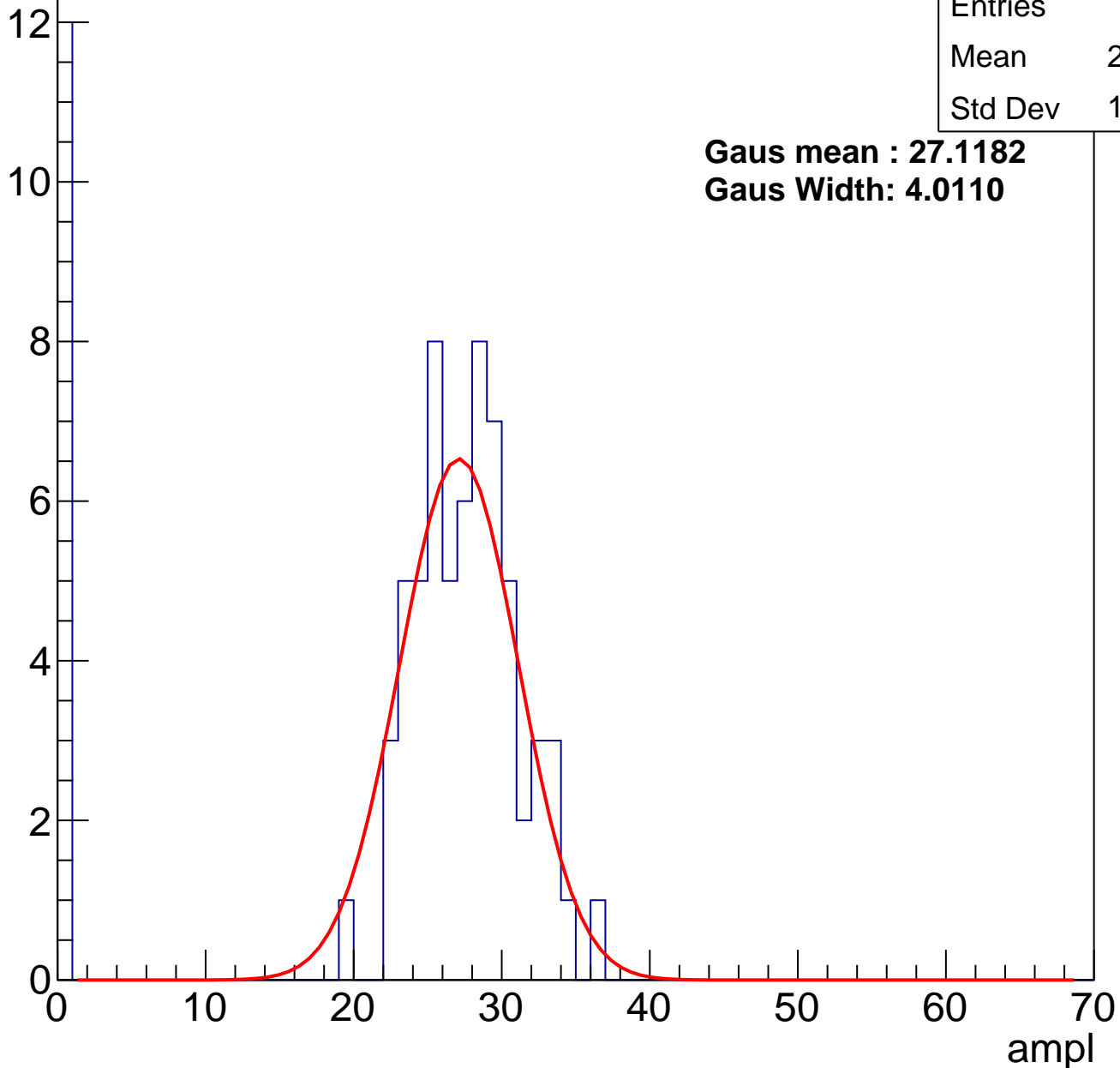
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	75
Mean	22.88
Std Dev	10.46

**Gaus mean : 27.1182**

**Gaus Width: 4.0110**

Entry



# B1L103S, U26-ch86, adc1

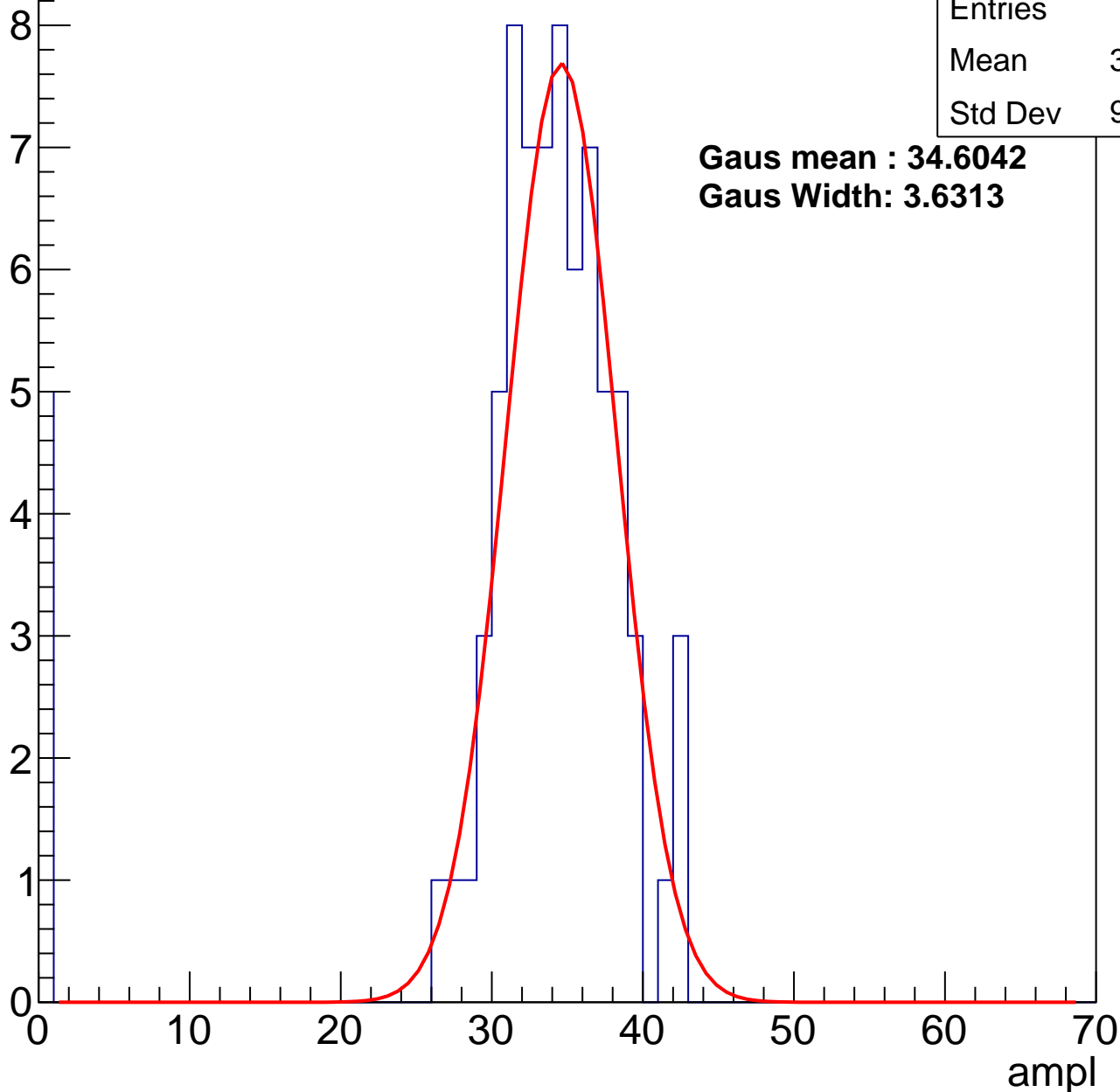
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	76
Mean	31.76
Std Dev	9.094

**Gaus mean : 34.6042**

**Gaus Width: 3.6313**



# B1L103S, U26-ch86, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	81
Mean	35.72
Std Dev	14.6

**Gaus mean : 41.2520**

**Gaus Width: 3.7343**

Entry

10

8

6

4

2

0

0

10

20

30

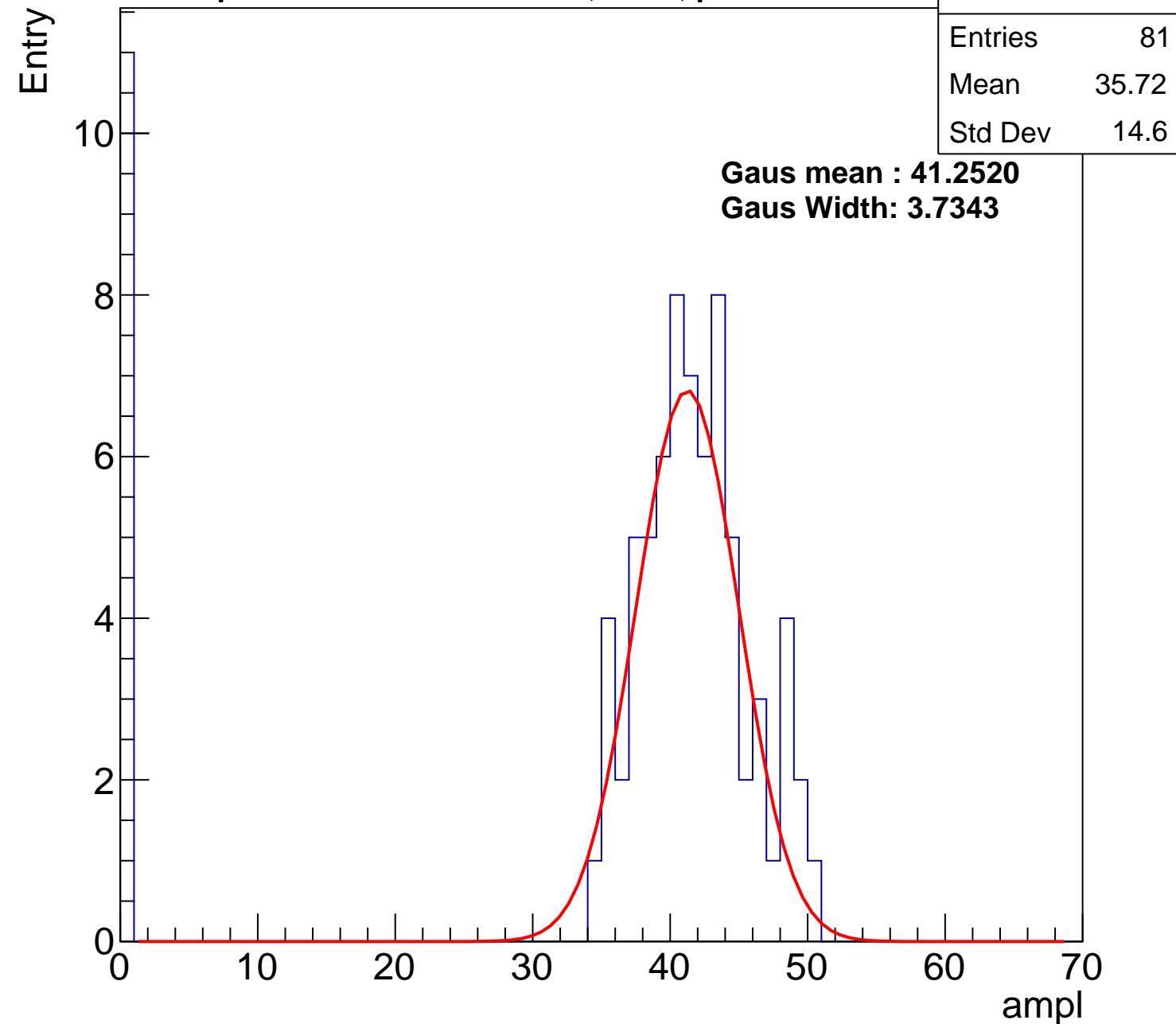
40

50

60

70

ampl

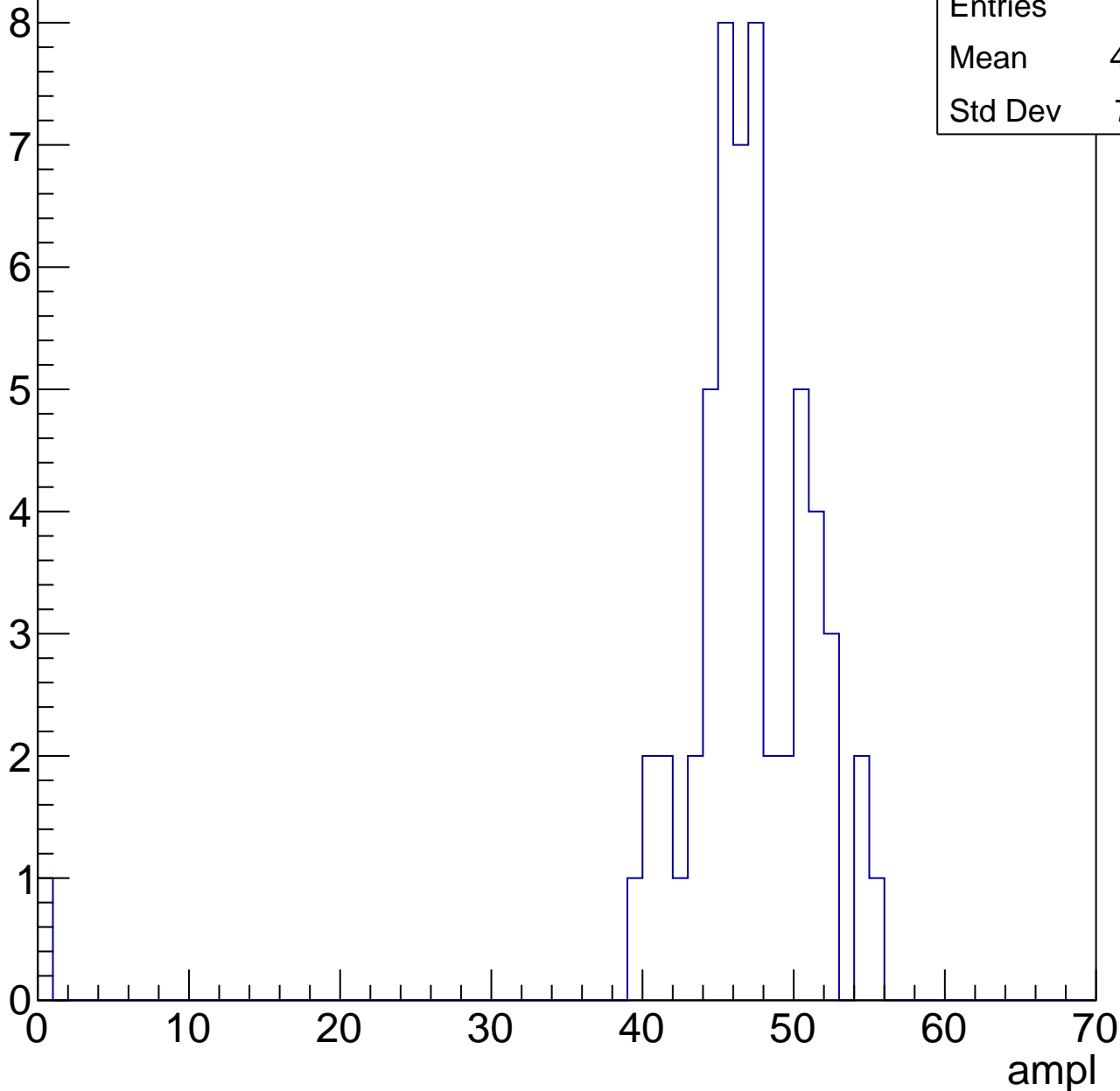


# B1L103S, U26-ch86, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	56
Mean	45.96
Std Dev	7.171

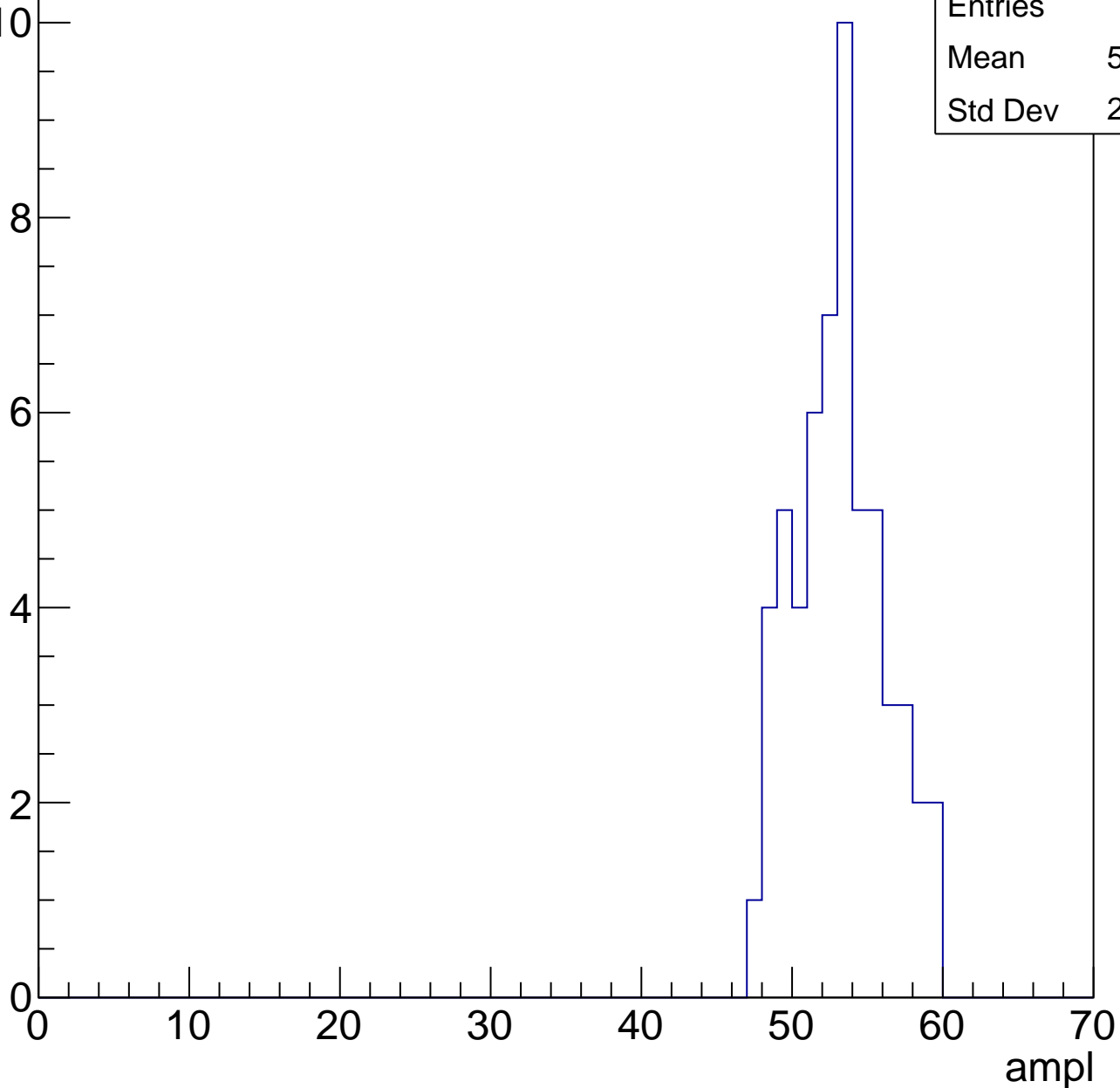


# B1L103S, U26-ch86, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	57
Mean	52.67
Std Dev	2.958

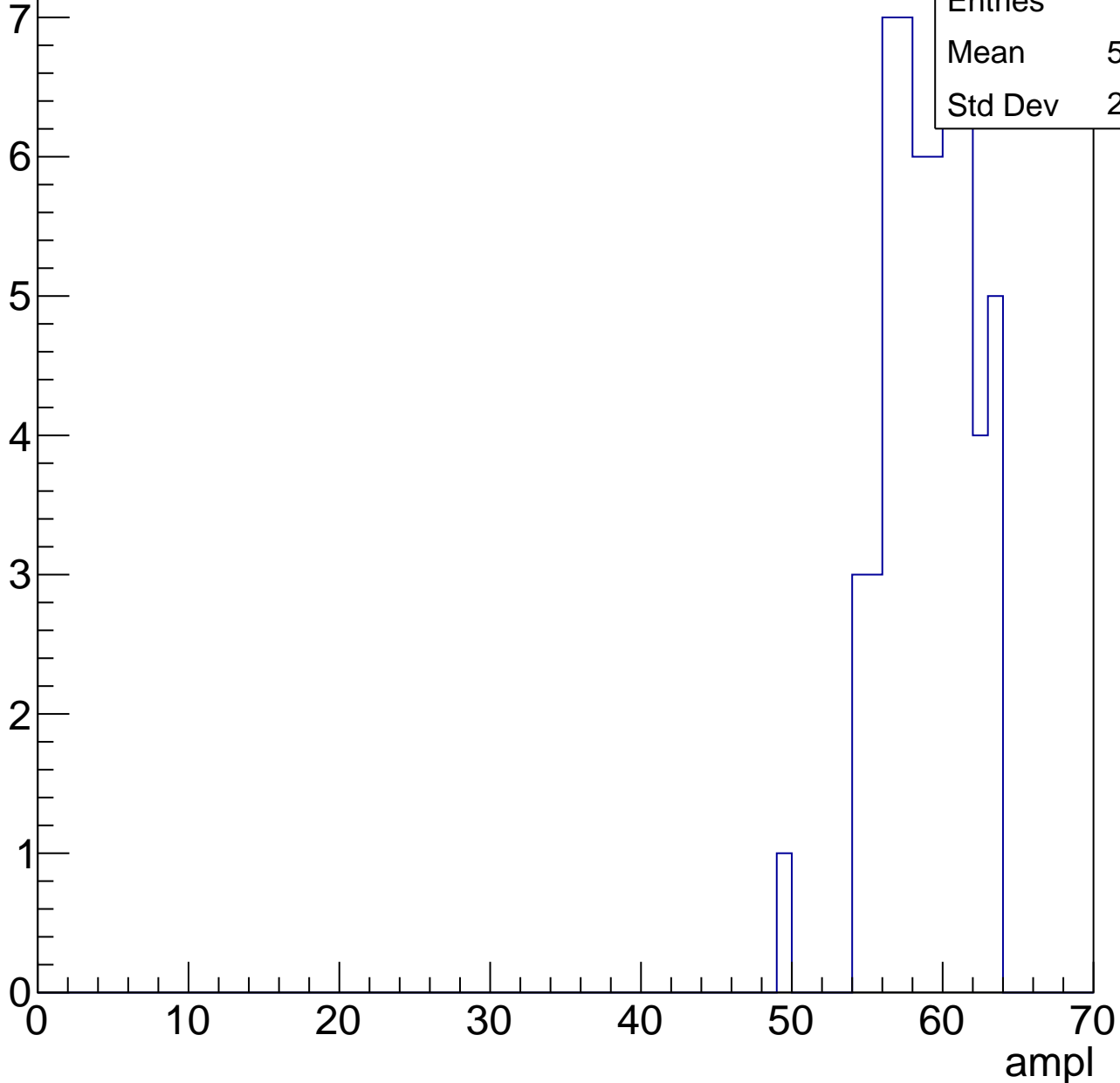


# B1L103S, U26-ch86, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	56
Mean	58.55
Std Dev	2.866

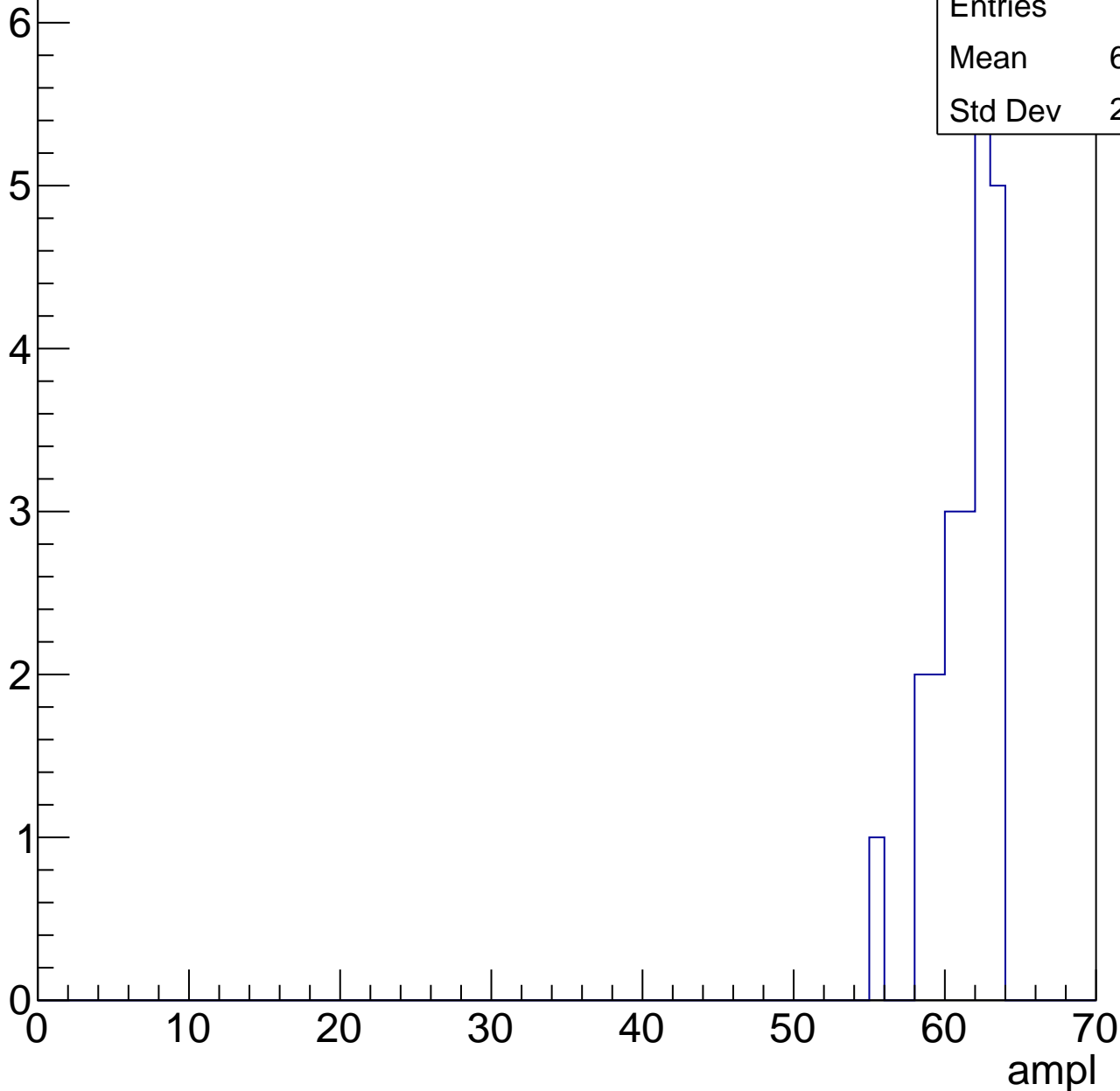


# B1L103S, U26-ch86, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	22
Mean	60.86
Std Dev	2.029





# B1L103S, U26-ch86, adc7

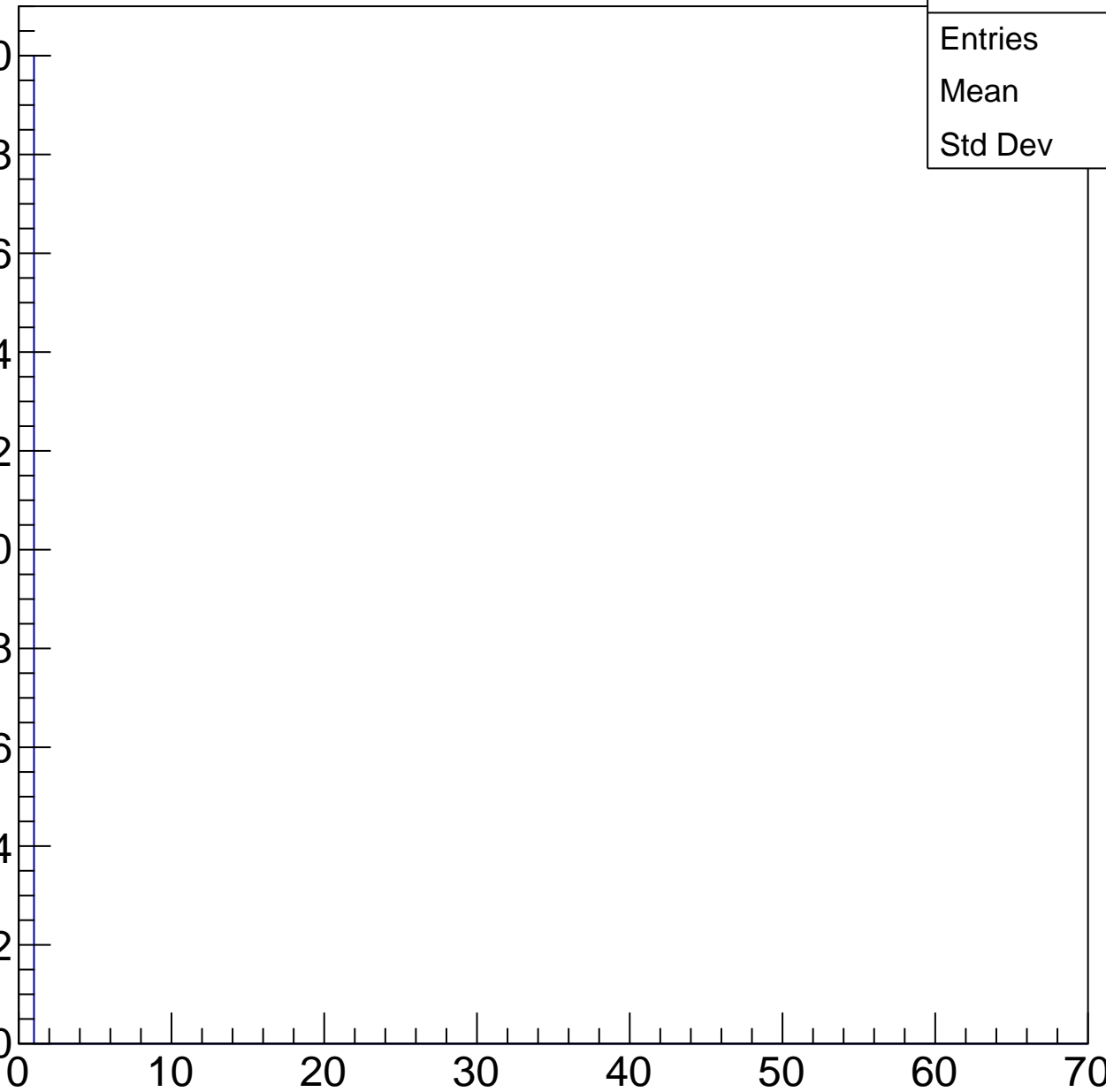
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

20  
18  
16  
14  
12  
10  
8  
6  
4  
2  
0

Entries	20
Mean	0
Std Dev	0

ampl



# B1L103S, U26-ch87, adc0

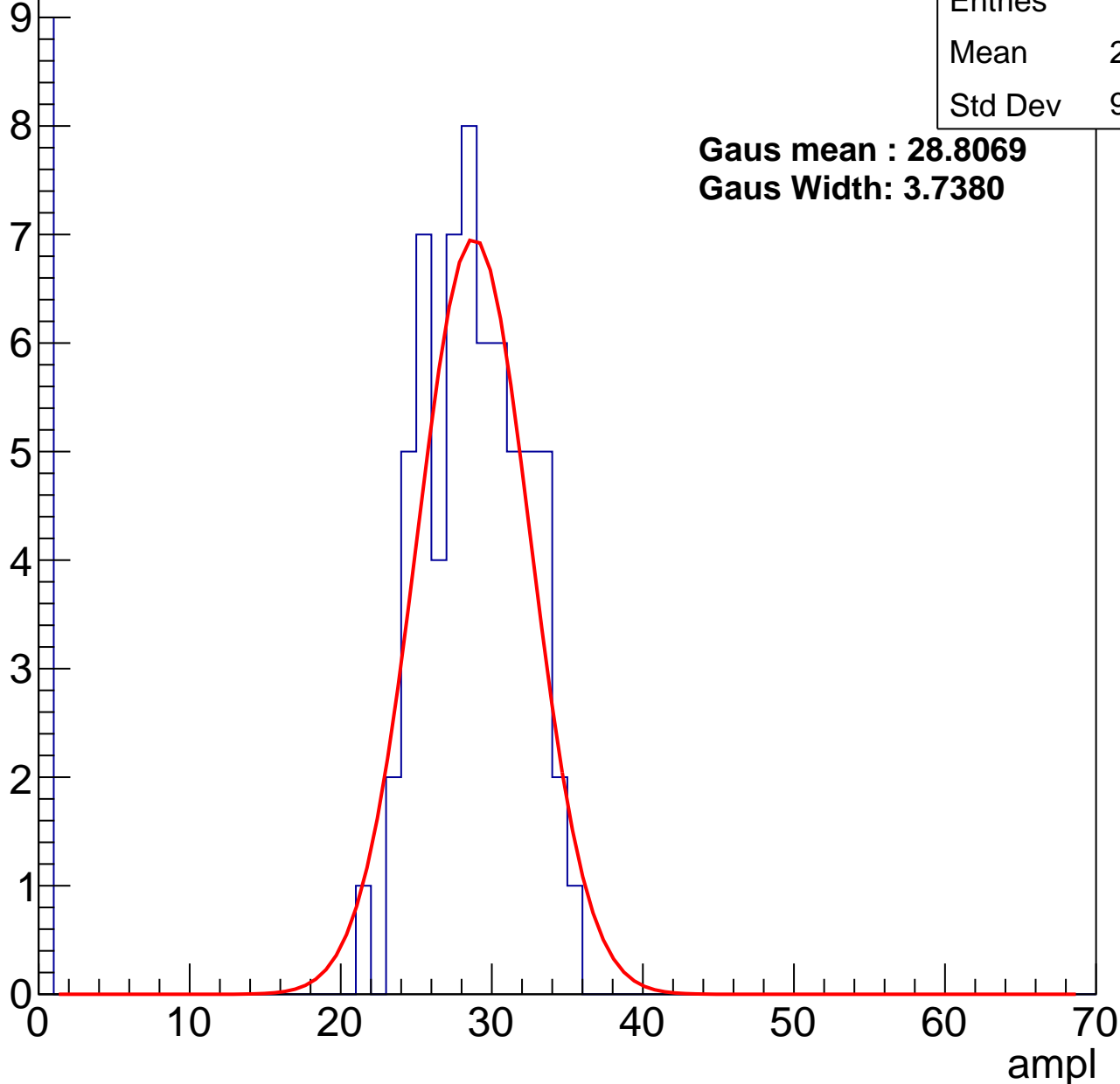
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	73
Mean	24.88
Std Dev	9.799

**Gaus mean : 28.8069**

**Gaus Width: 3.7380**



# B1L103S, U26-ch87, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	92
Mean	31.5
Std Dev	12.09

**Gaus mean : 36.0233**

**Gaus Width: 4.0662**

Entry

10

8

6

4

2

0

0

10

20

30

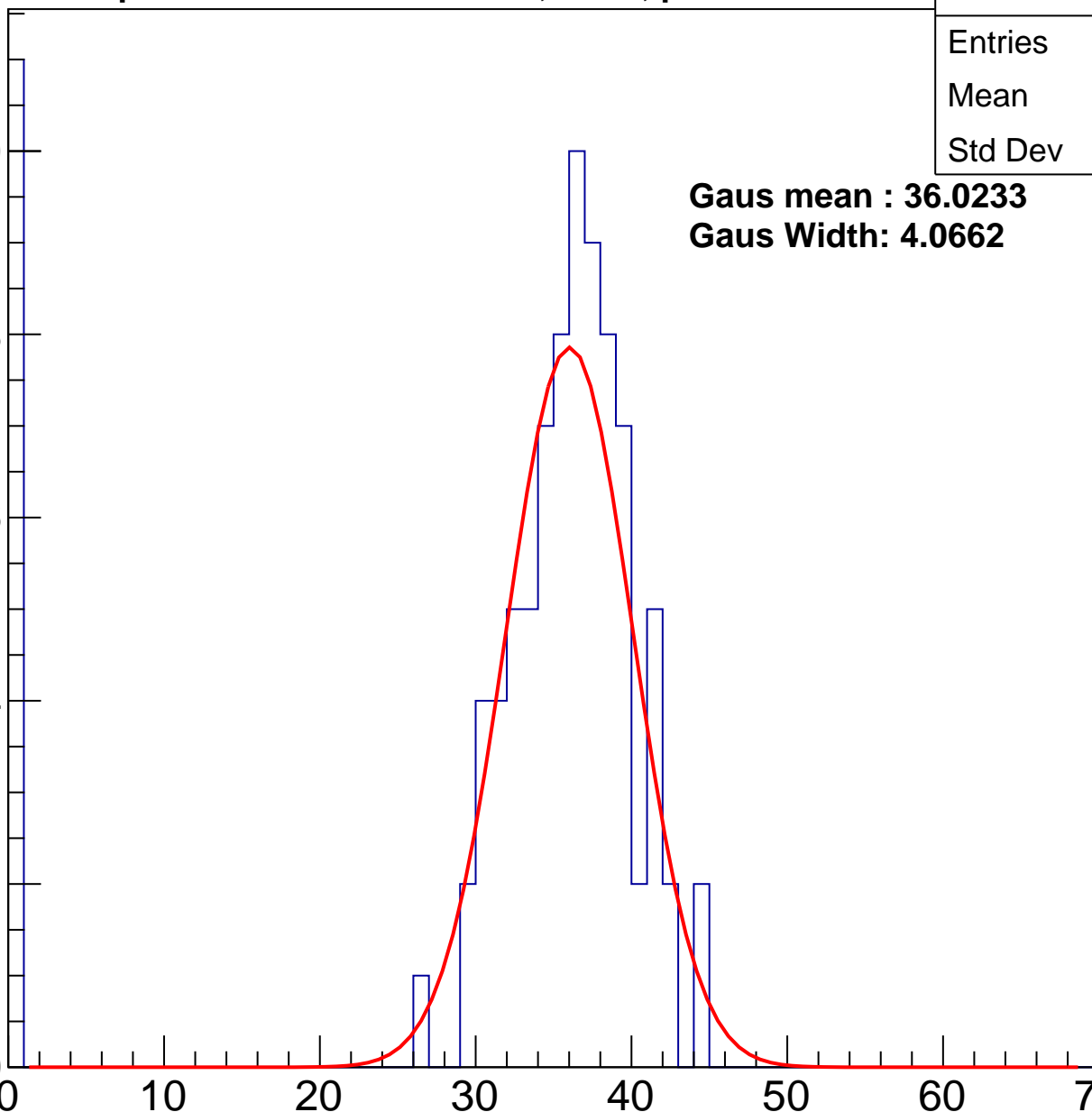
40

50

60

70

ampl



# B1L103S, U26-ch87, adc2

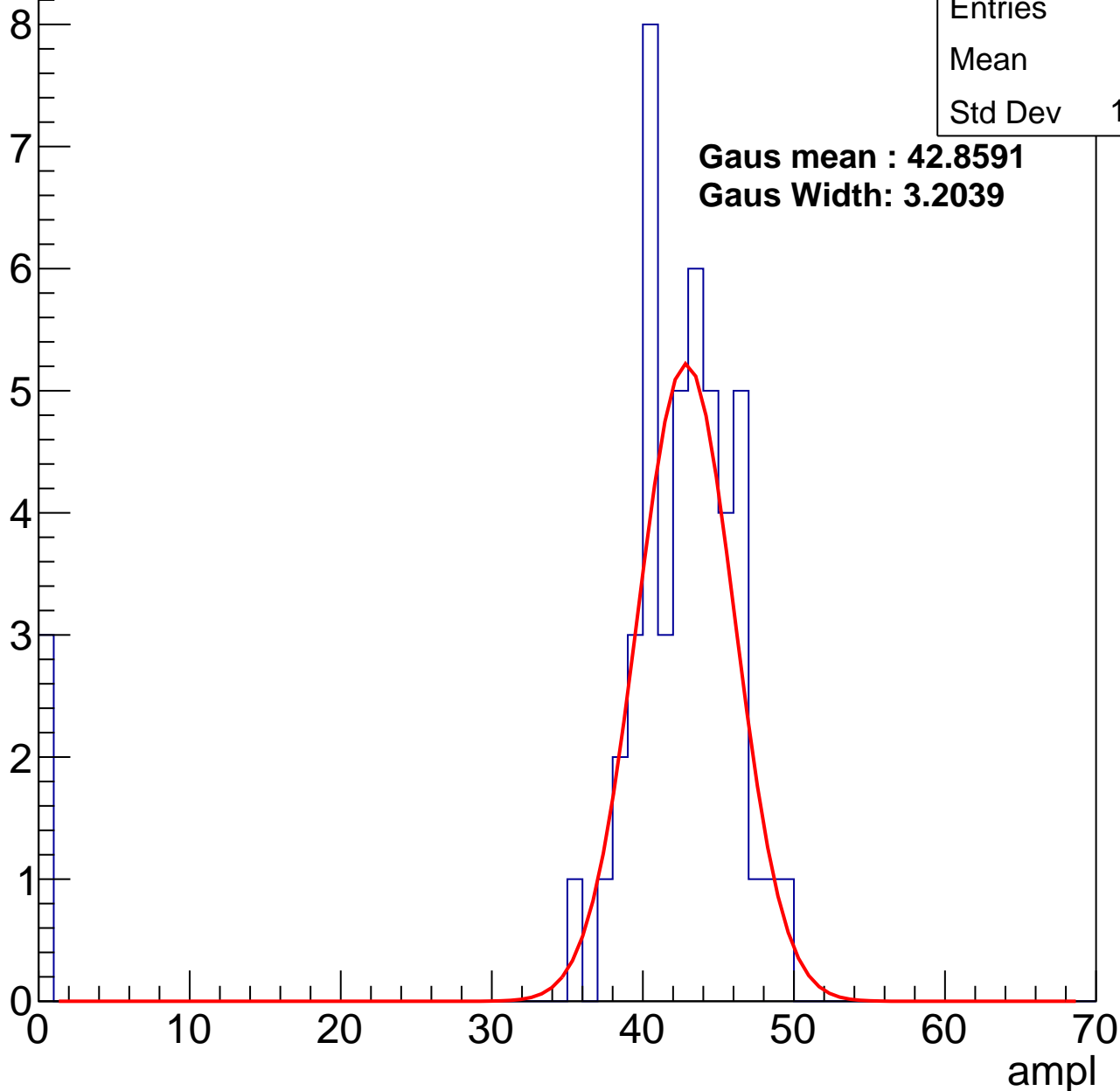
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	49
Mean	39.8
Std Dev	10.57

**Gaus mean : 42.8591**

**Gaus Width: 3.2039**

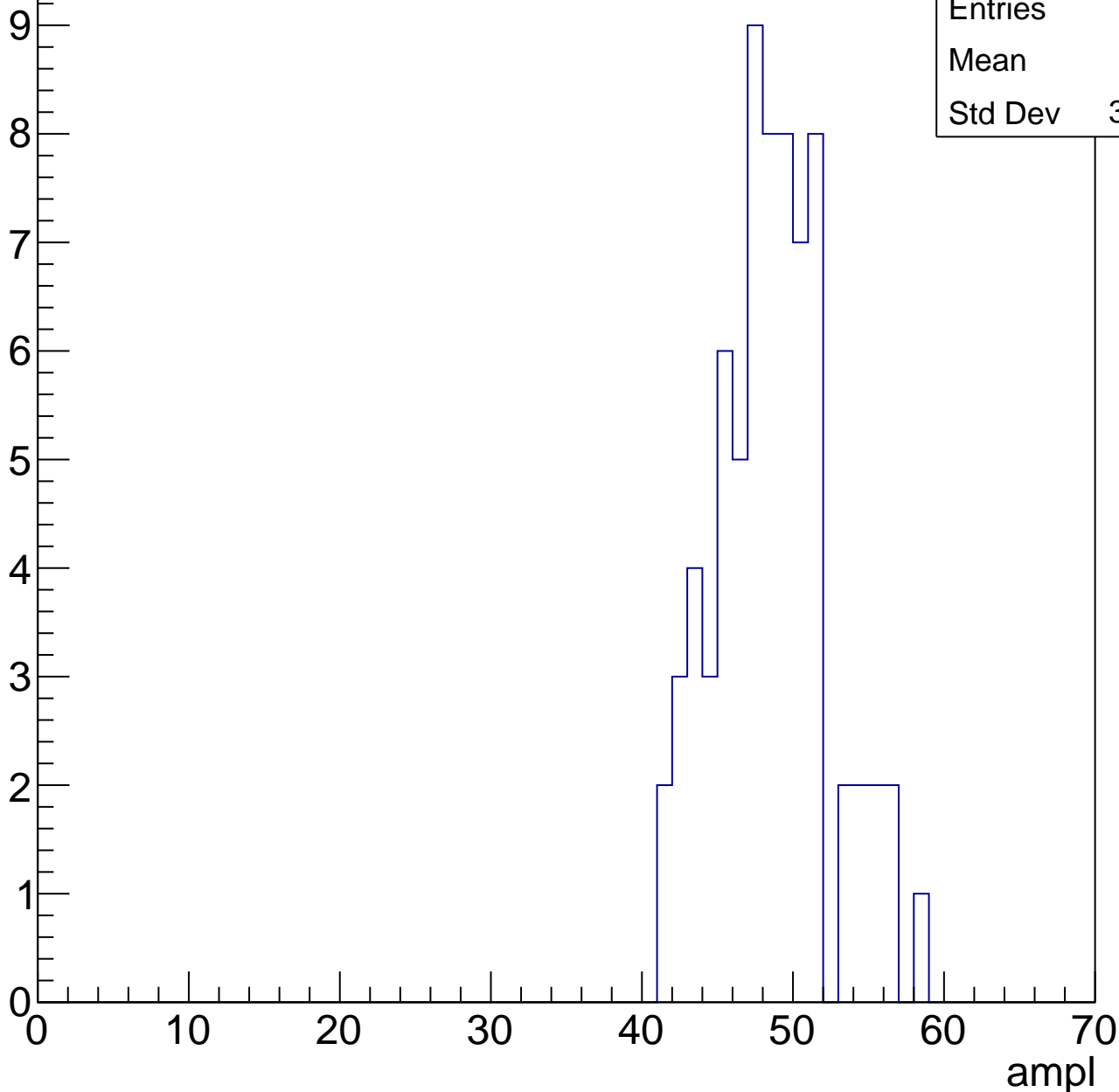


# B1L103S, U26-ch87, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	72
Mean	48.1
Std Dev	3.712



# B1L103S, U26-ch87, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	75
Mean	55.56
Std Dev	3.48

Entry

10

8

6

4

2

0

0

10

20

30

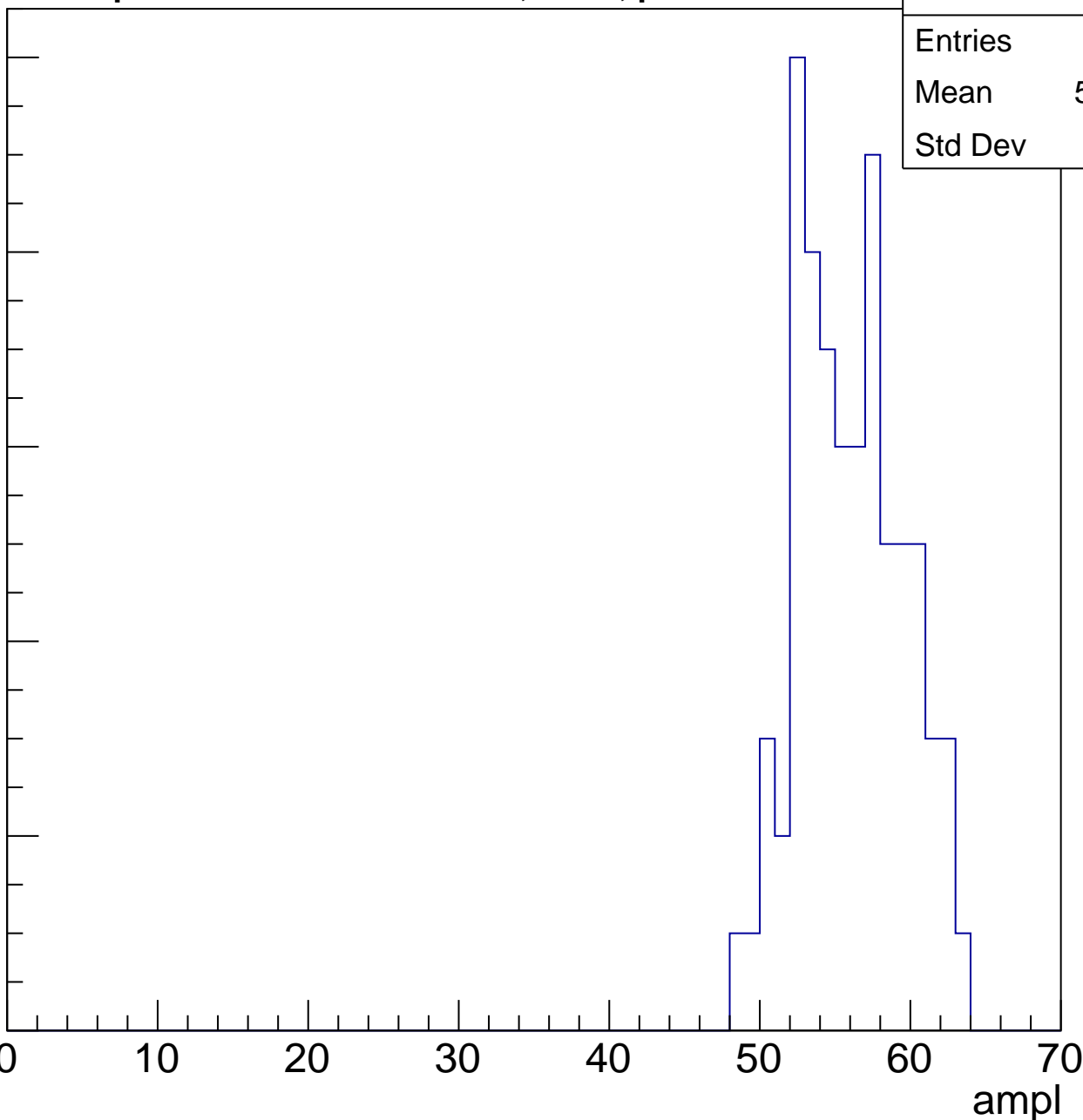
40

50

60

70

ampl

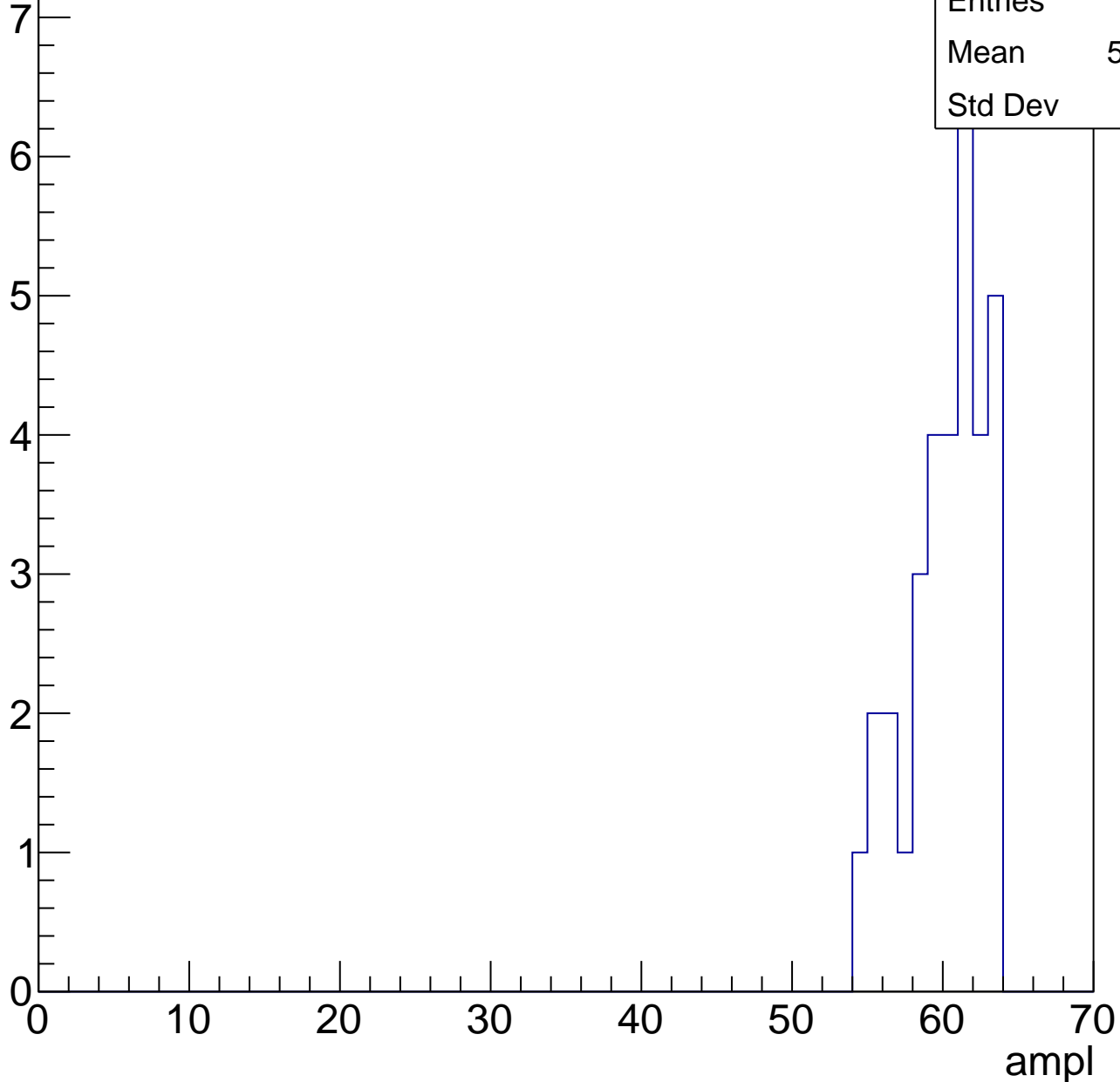


# B1L103S, U26-ch87, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

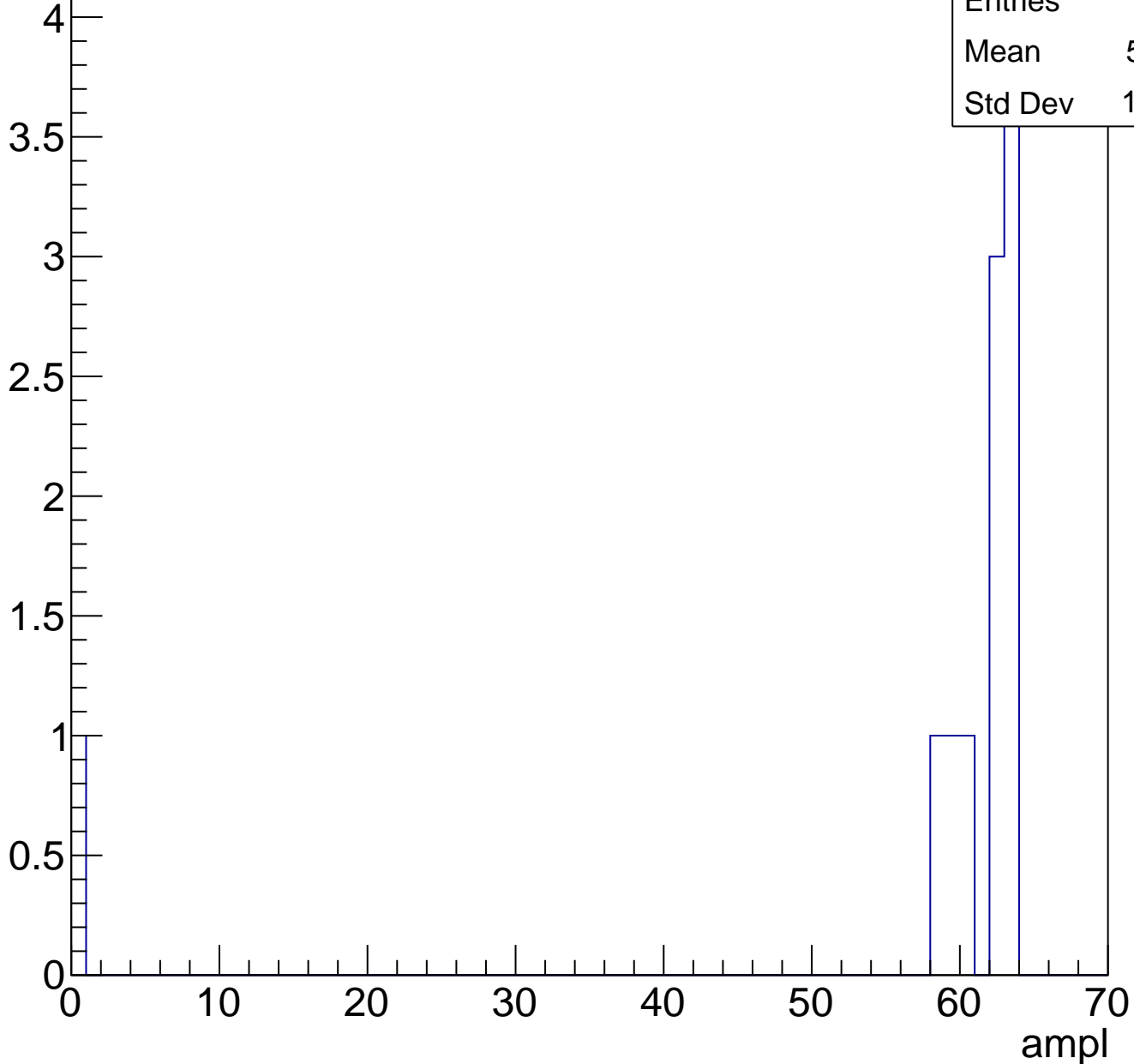
Entries	33
Mean	59.79
Std Dev	2.52



# B1L103S, U26-ch87, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry





# B1L103S, U26-ch87, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



# B1L103S, U26-ch88, adc0

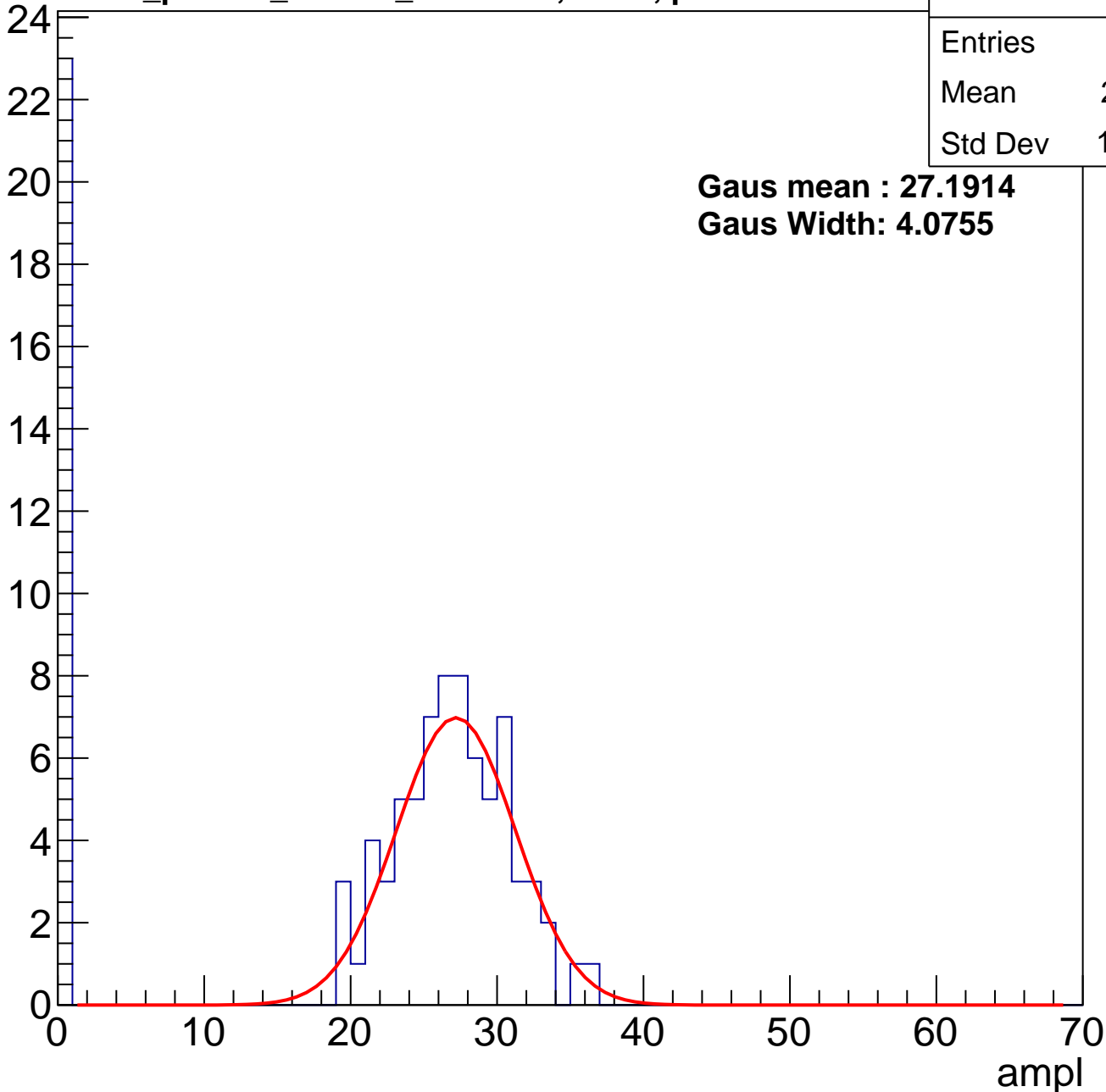
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	95
Mean	20.11
Std Dev	11.83

**Gaus mean : 27.1914**

**Gaus Width: 4.0755**

Entry



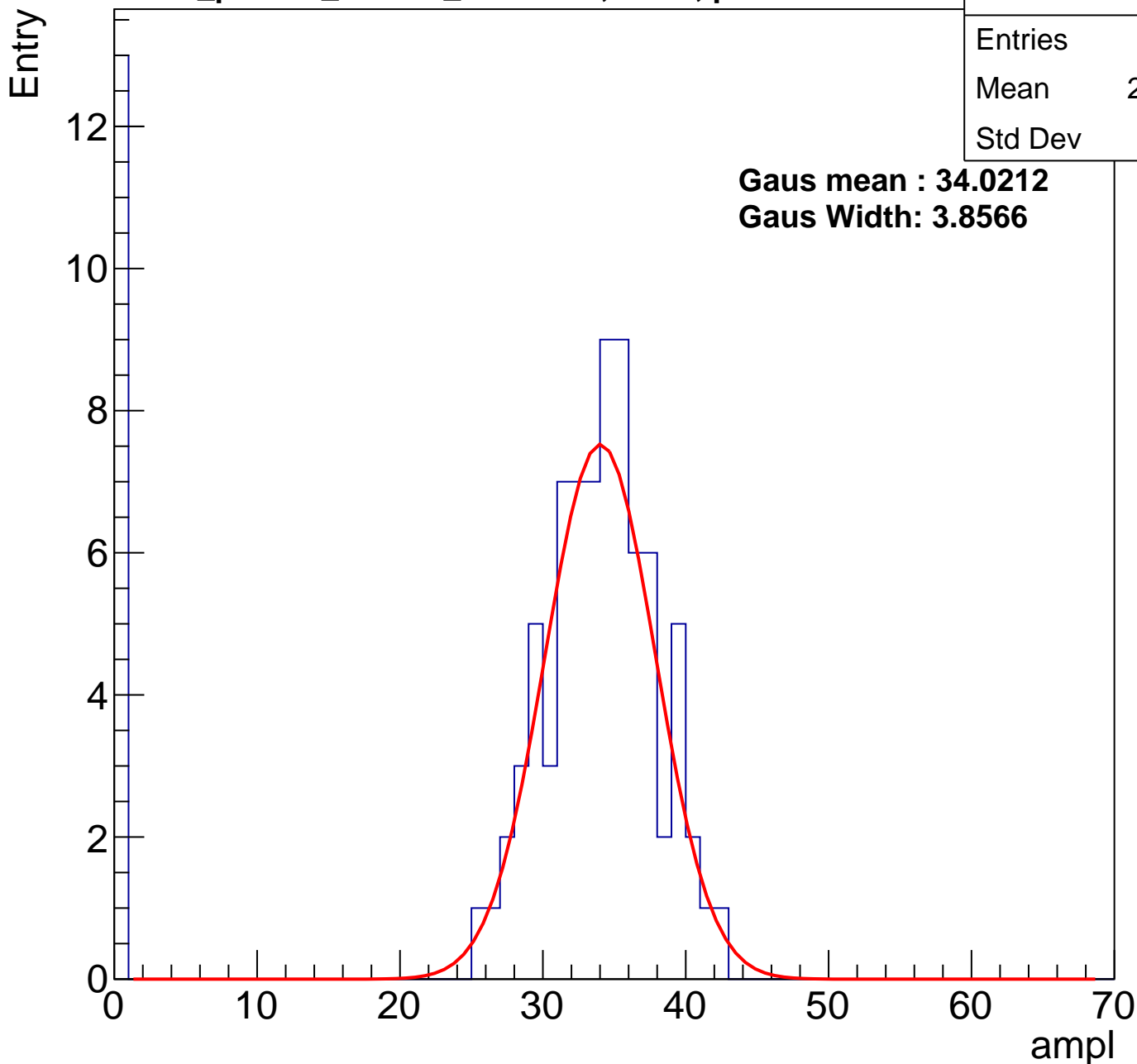
# B1L103S, U26-ch88, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	90
Mean	28.77
Std Dev	12.3

**Gaus mean : 34.0212**

**Gaus Width: 3.8566**



# B1L103S, U26-ch88, adc2

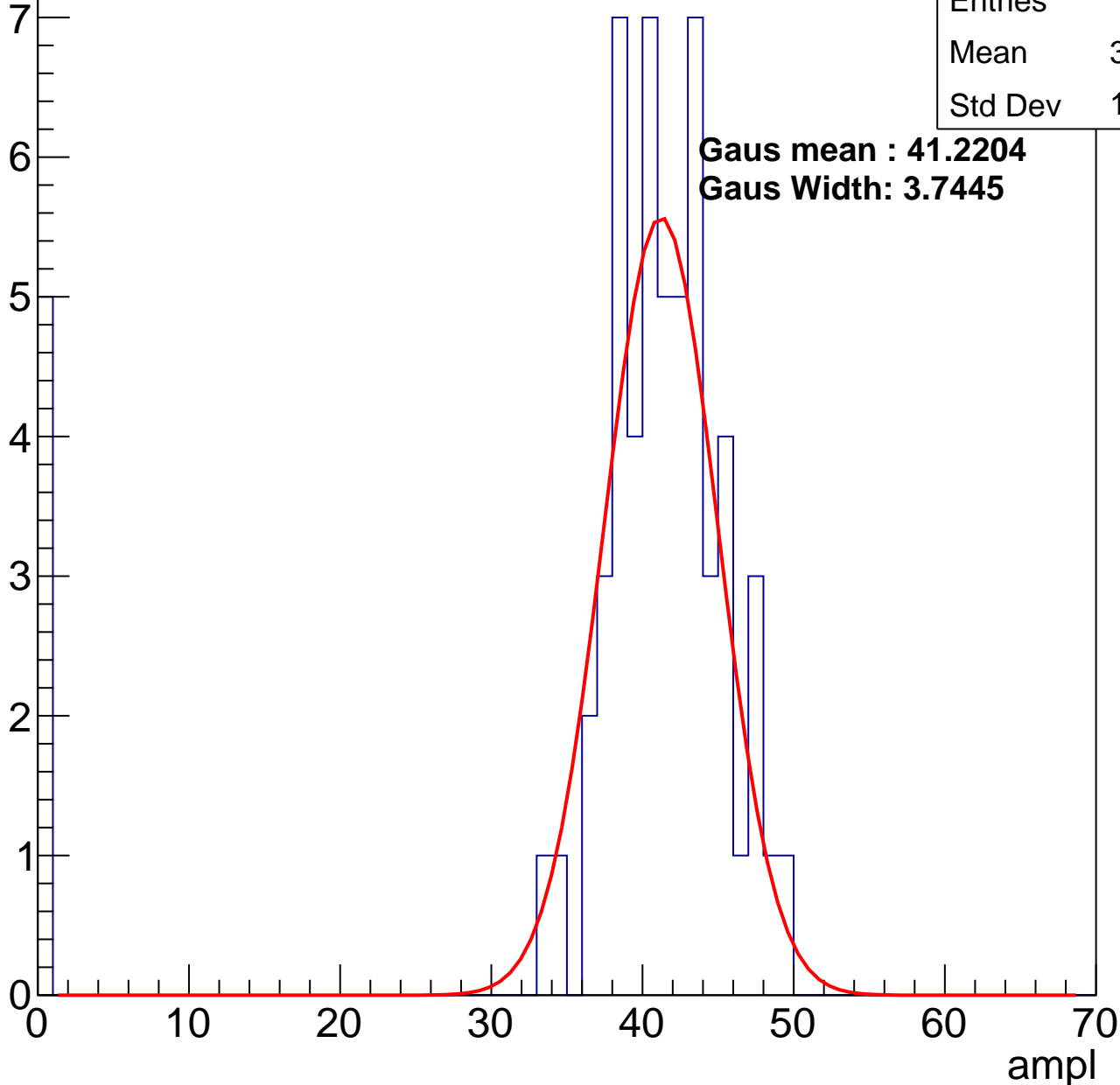
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	60
Mean	37.73
Std Dev	11.85

**Gaus mean : 41.2204**

**Gaus Width: 3.7445**

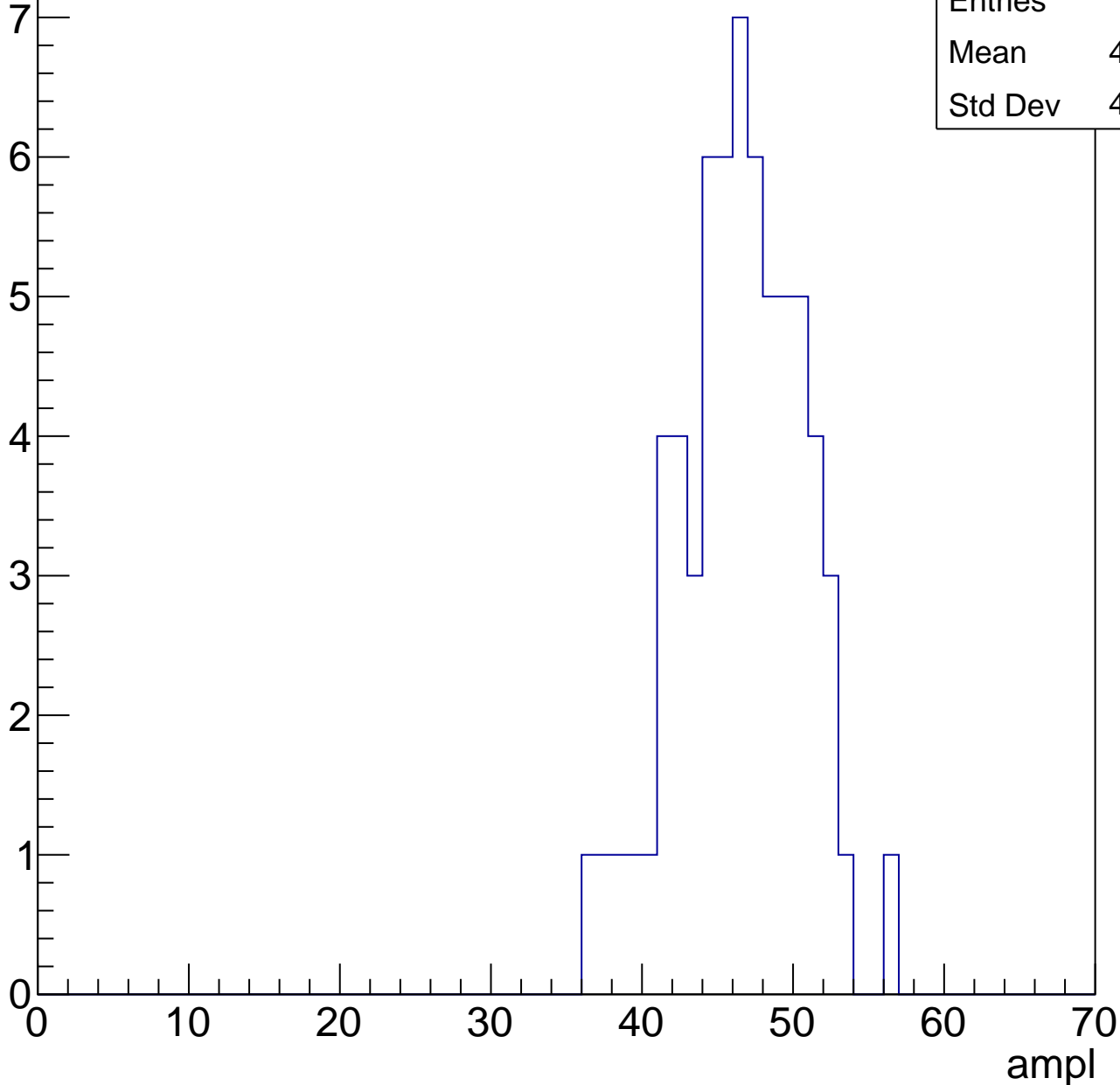


# B1L103S, U26-ch88, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	65
Mean	46.05
Std Dev	4.036

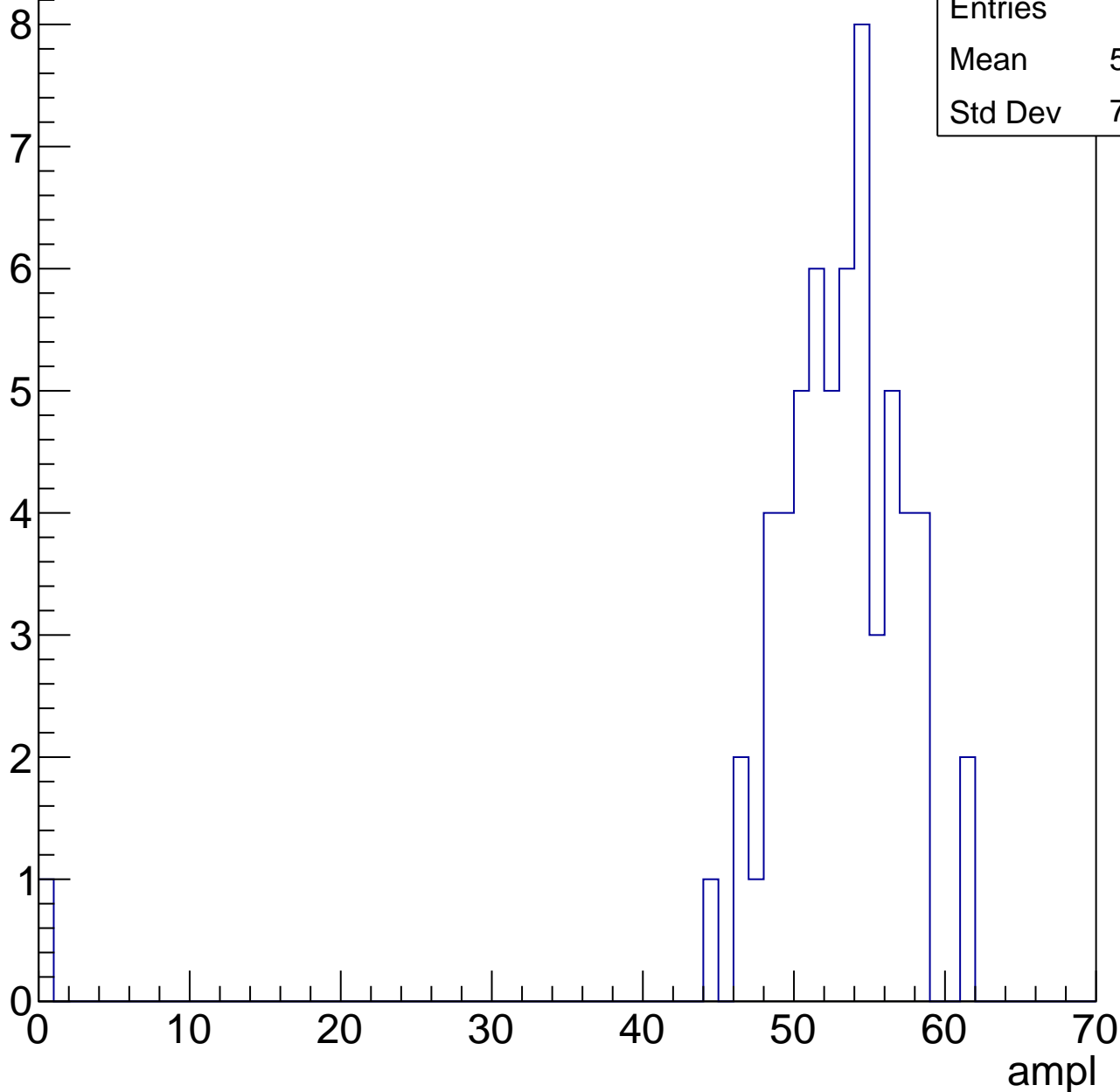


# B1L103S, U26-ch88, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	61
Mean	51.87
Std Dev	7.619

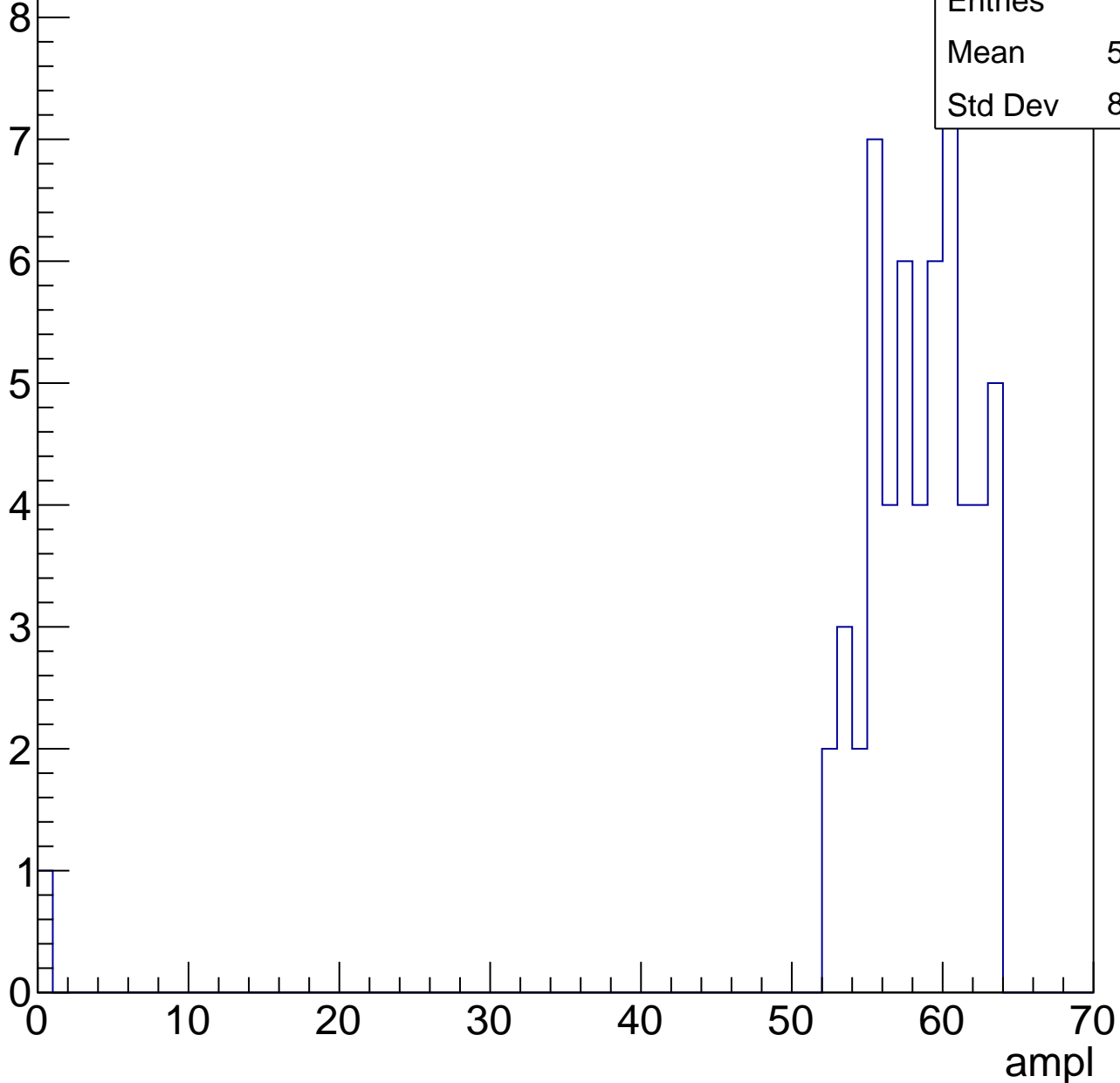


# B1L103S, U26-ch88, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	56
Mean	57.05
Std Dev	8.282

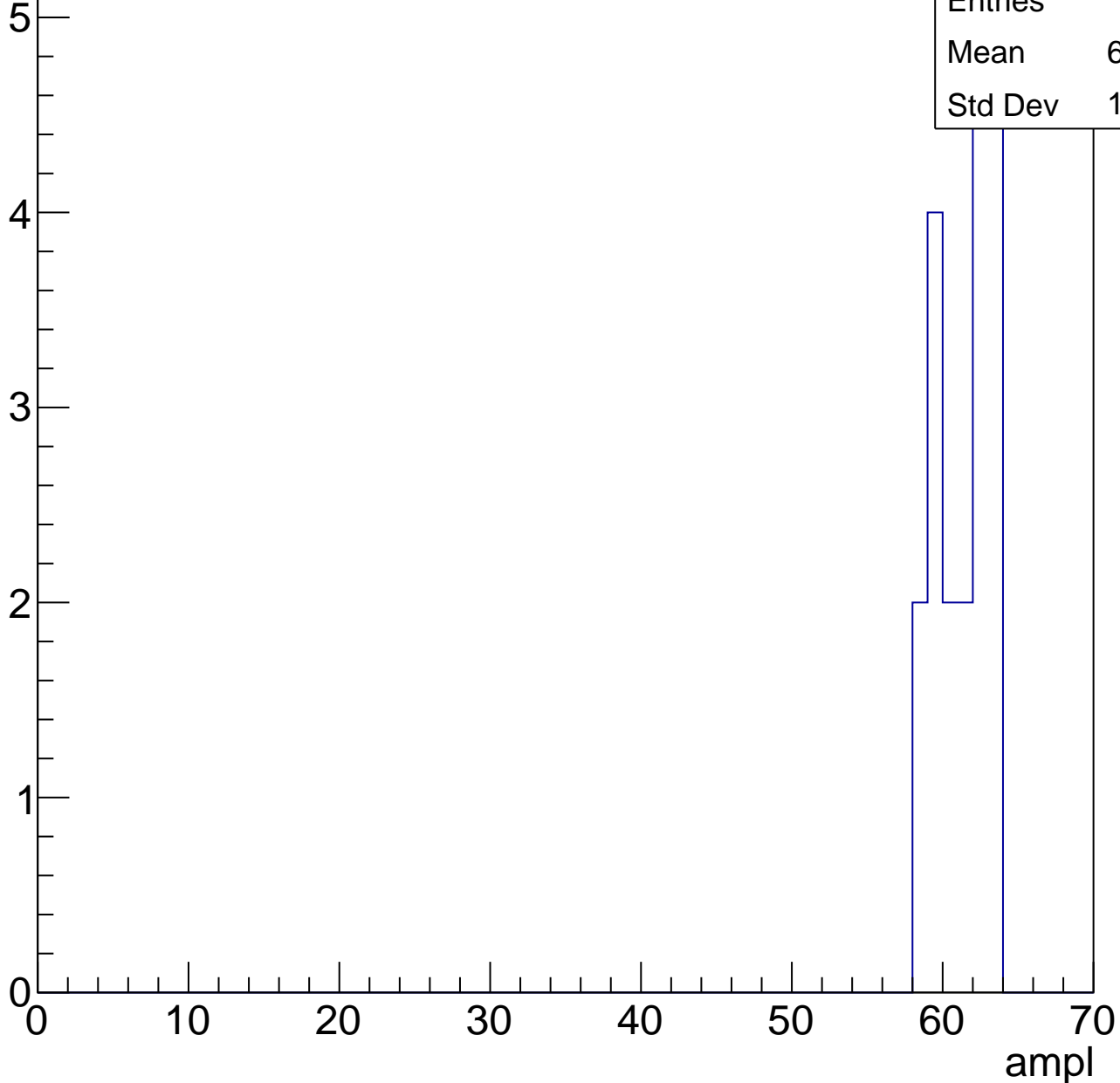


# B1L103S, U26-ch88, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	20
Mean	60.95
Std Dev	1.746



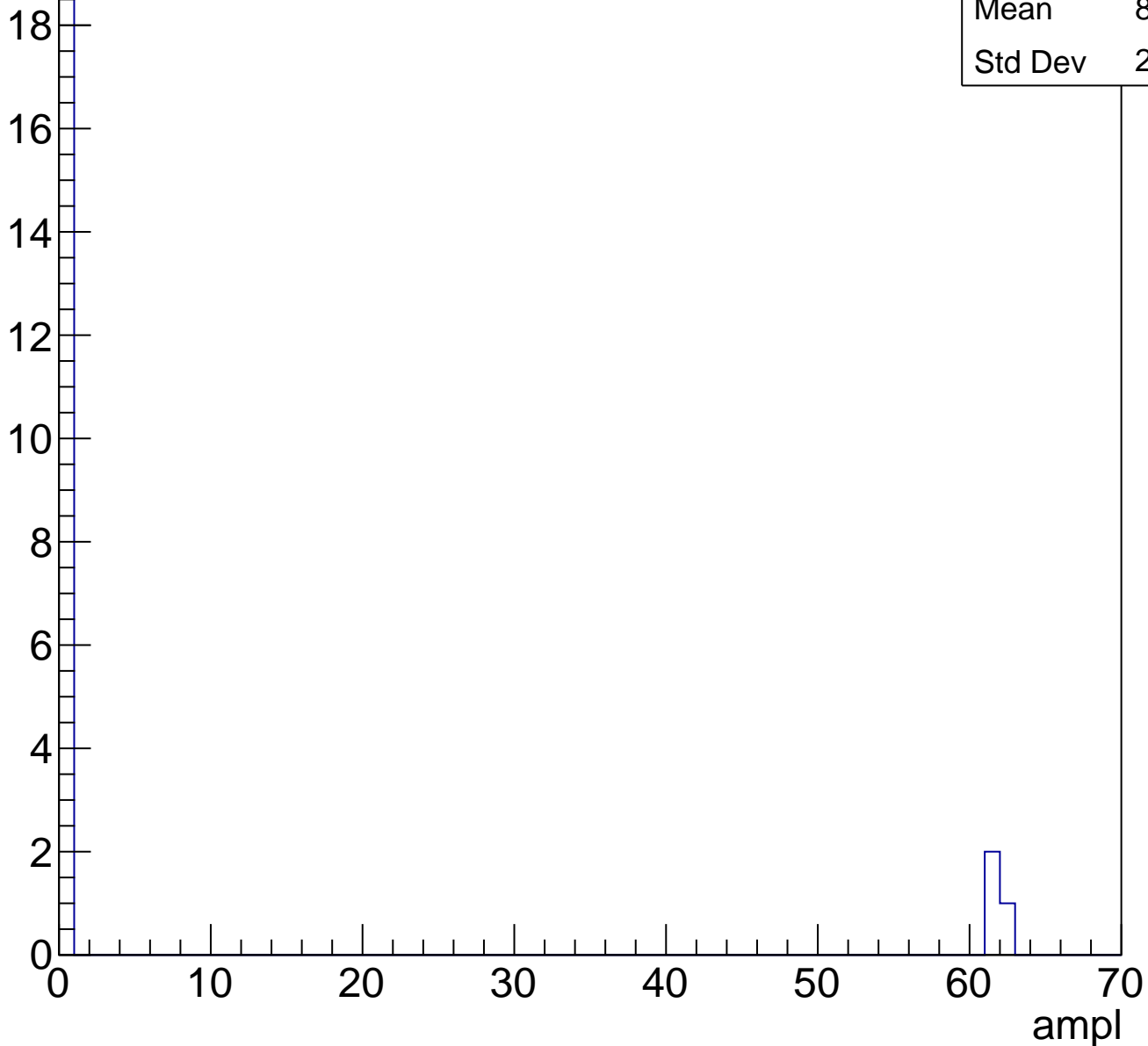


# B1L103S, U26-ch88, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	22
Mean	8.364
Std Dev	21.05

Entry



# B1L103S, U26-ch89, adc0

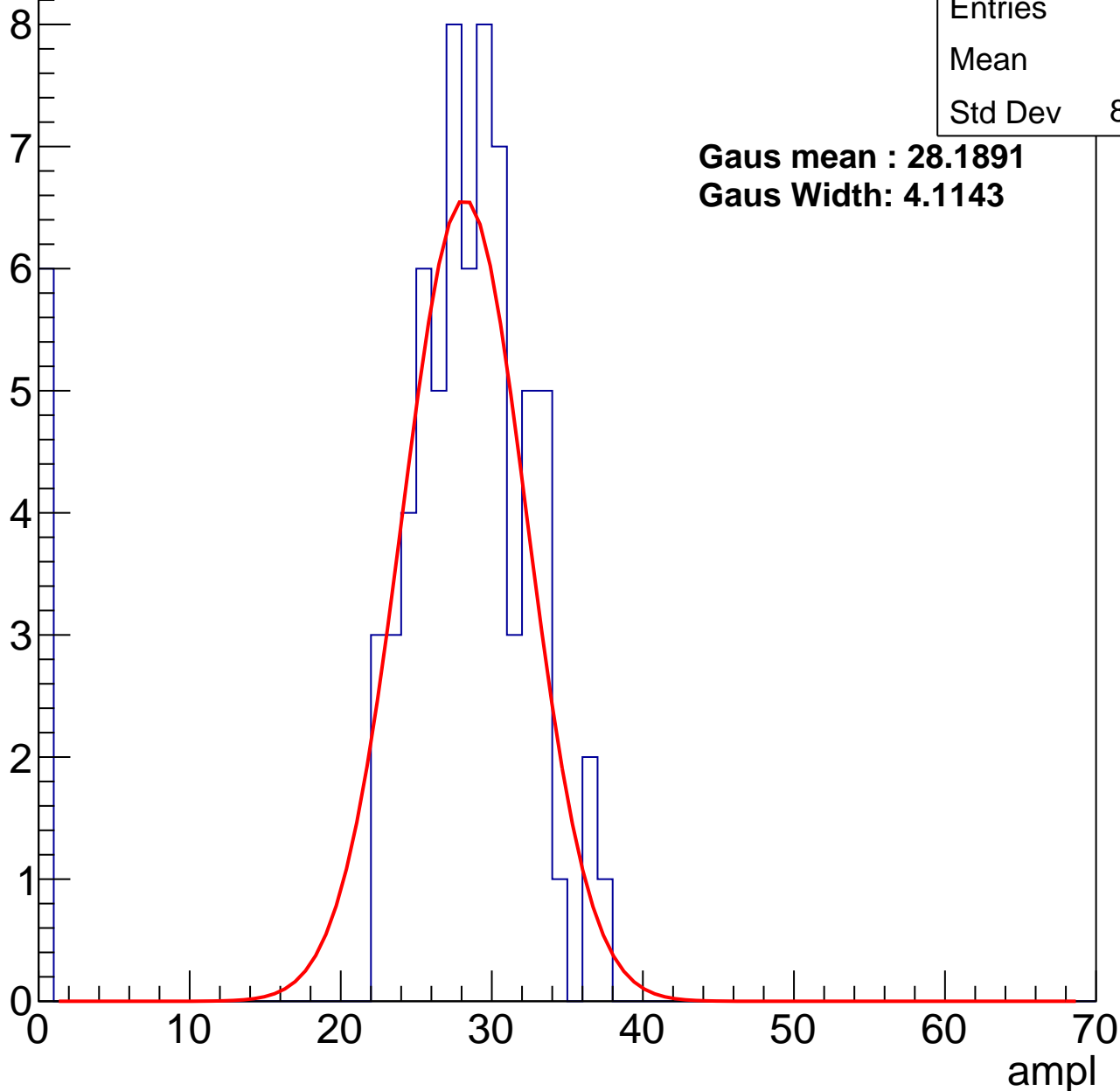
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	73
Mean	26
Std Dev	8.484

**Gaus mean : 28.1891**

**Gaus Width: 4.1143**



# B1L103S, U26-ch89, adc1

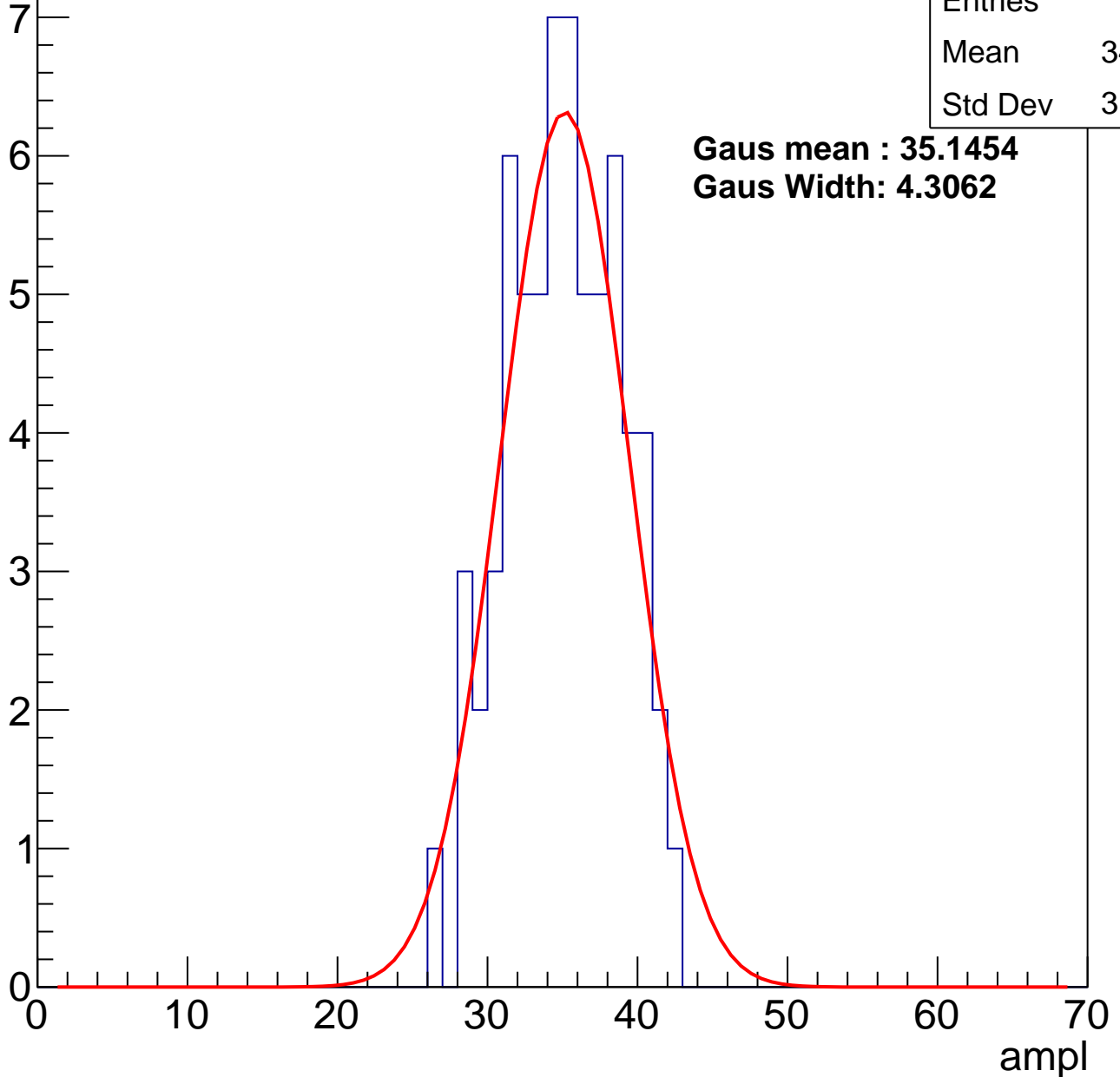
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	66
Mean	34.62
Std Dev	3.688

**Gaus mean : 35.1454**

**Gaus Width: 4.3062**



# B1L103S, U26-ch89, adc2

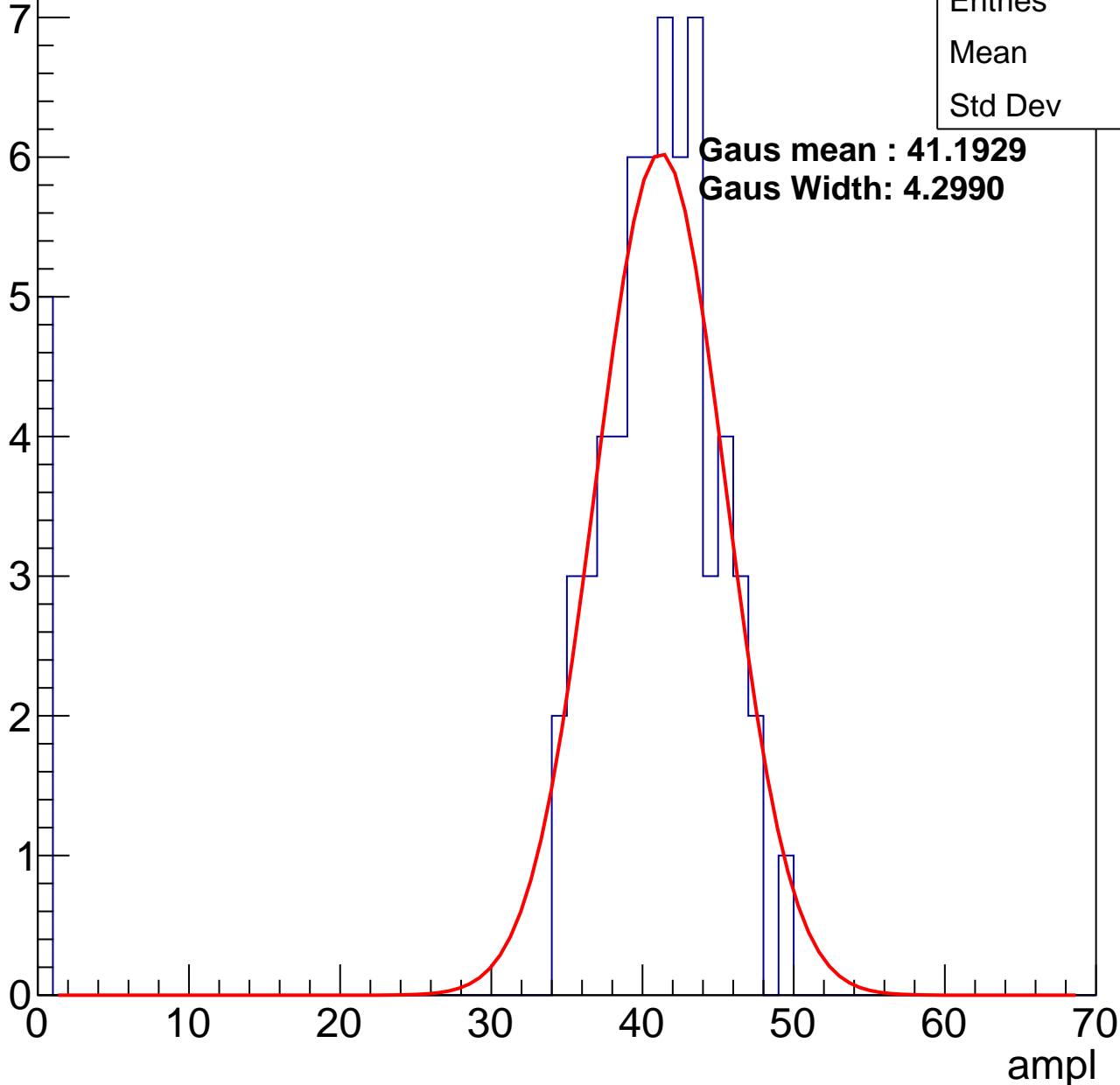
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	66
Mean	37.7
Std Dev	11.3

**Gaus mean : 41.1929**

**Gaus Width: 4.2990**

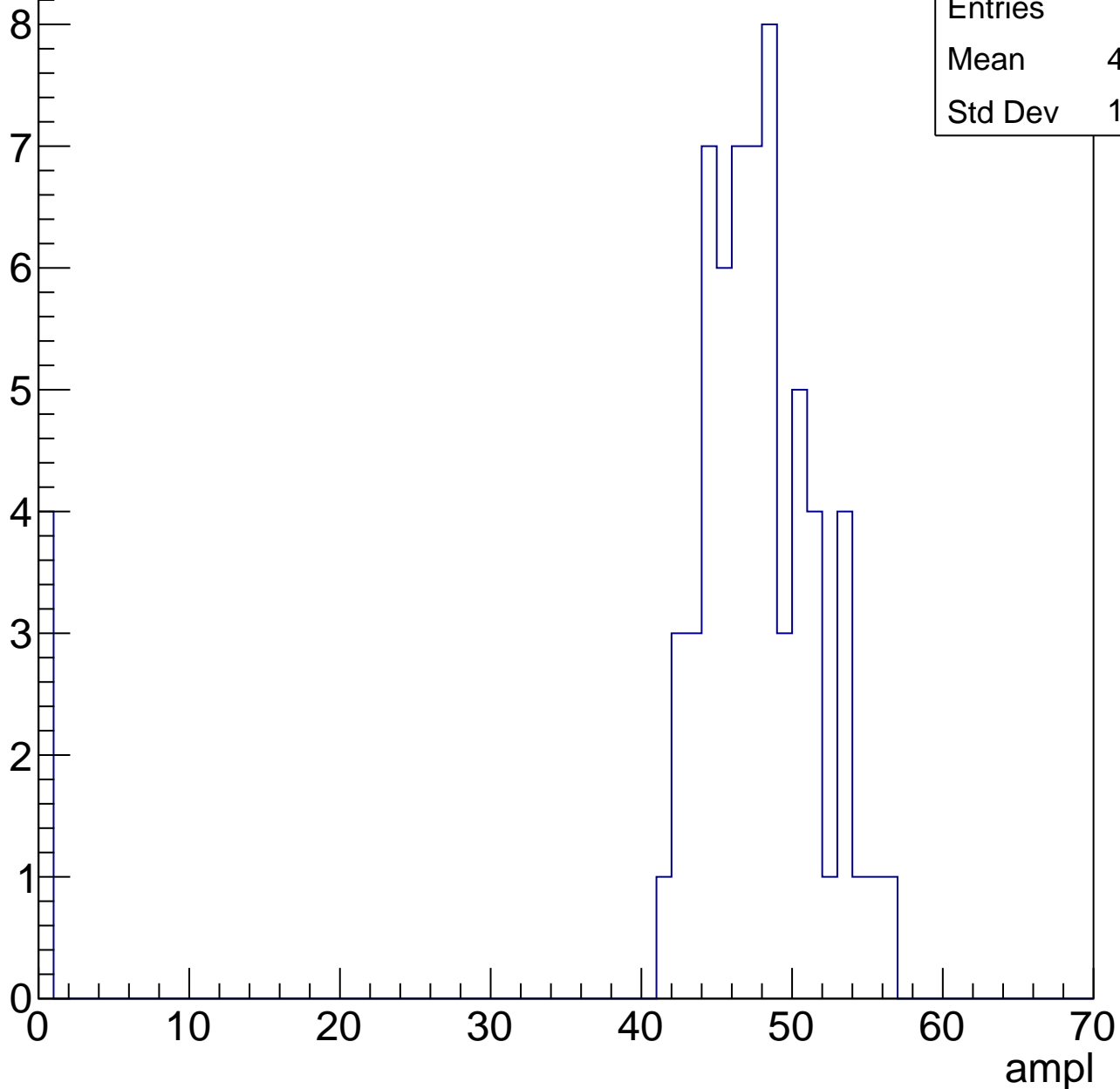


# B1L103S, U26-ch89, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

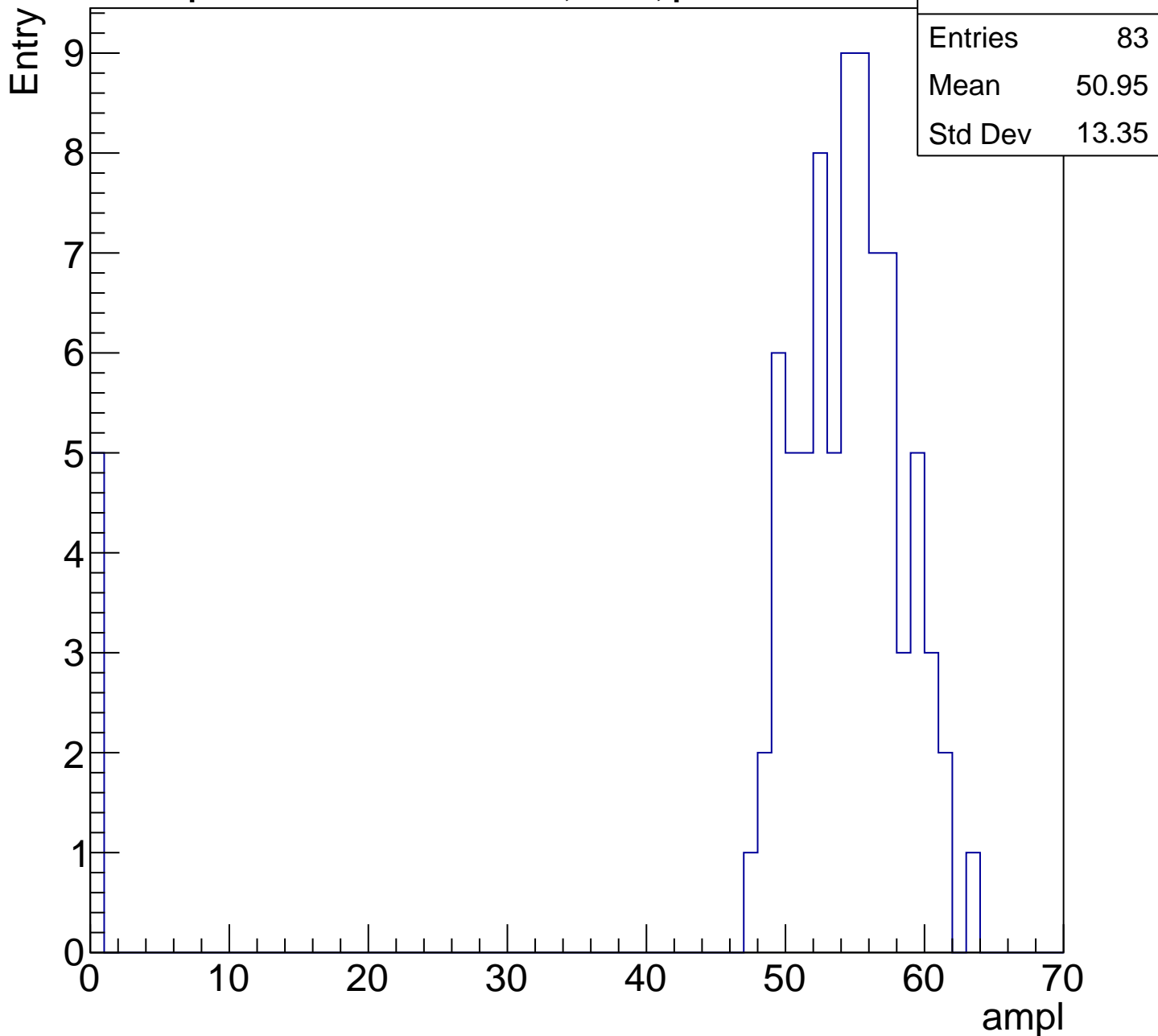
Entry

Entries	66
Mean	44.53
Std Dev	11.79



# B1L103S, U26-ch89, adc4

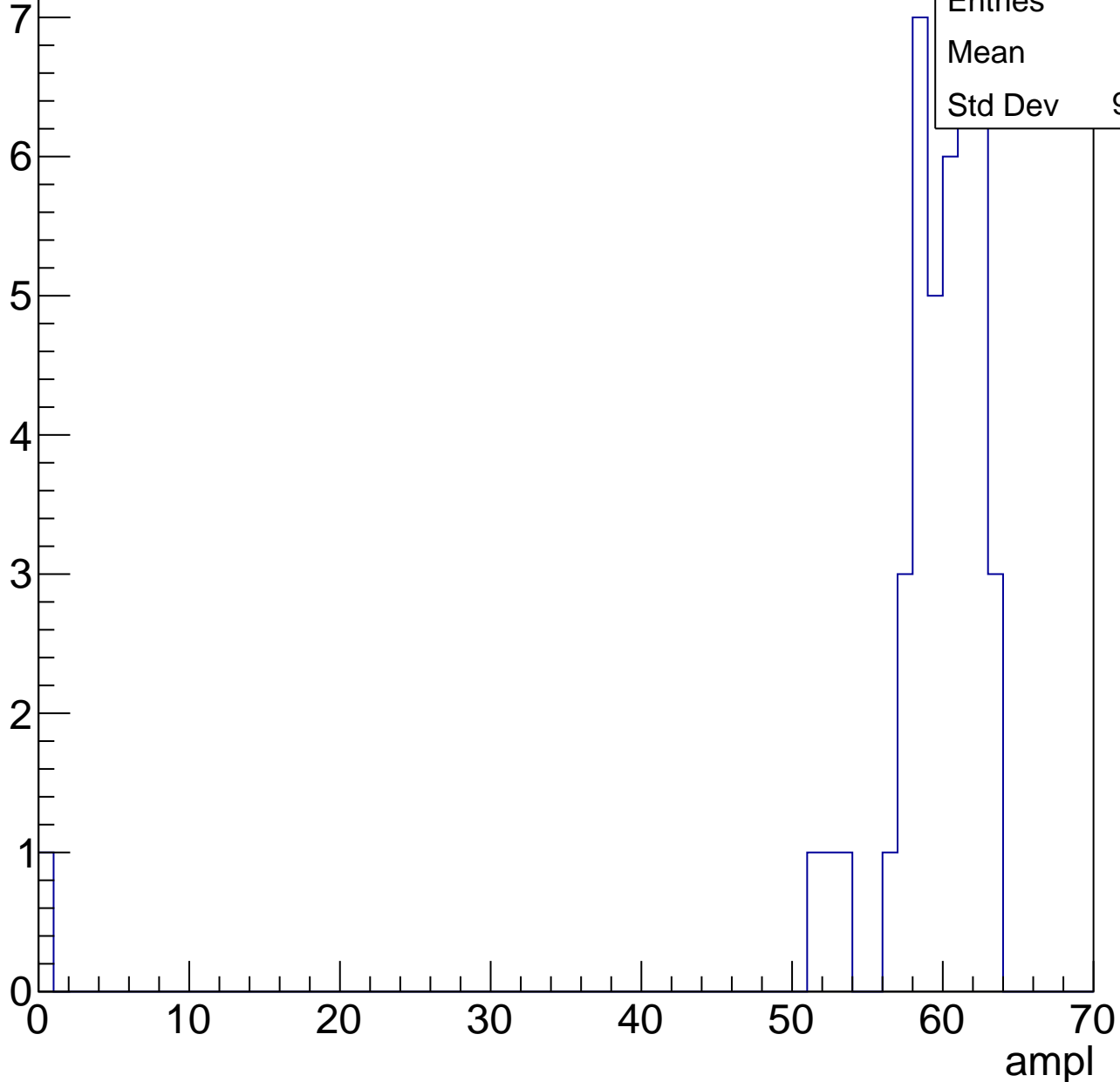
calib\_packv5\_041523\_1651.root, FC#0, port C2



# B1L103S, U26-ch89, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

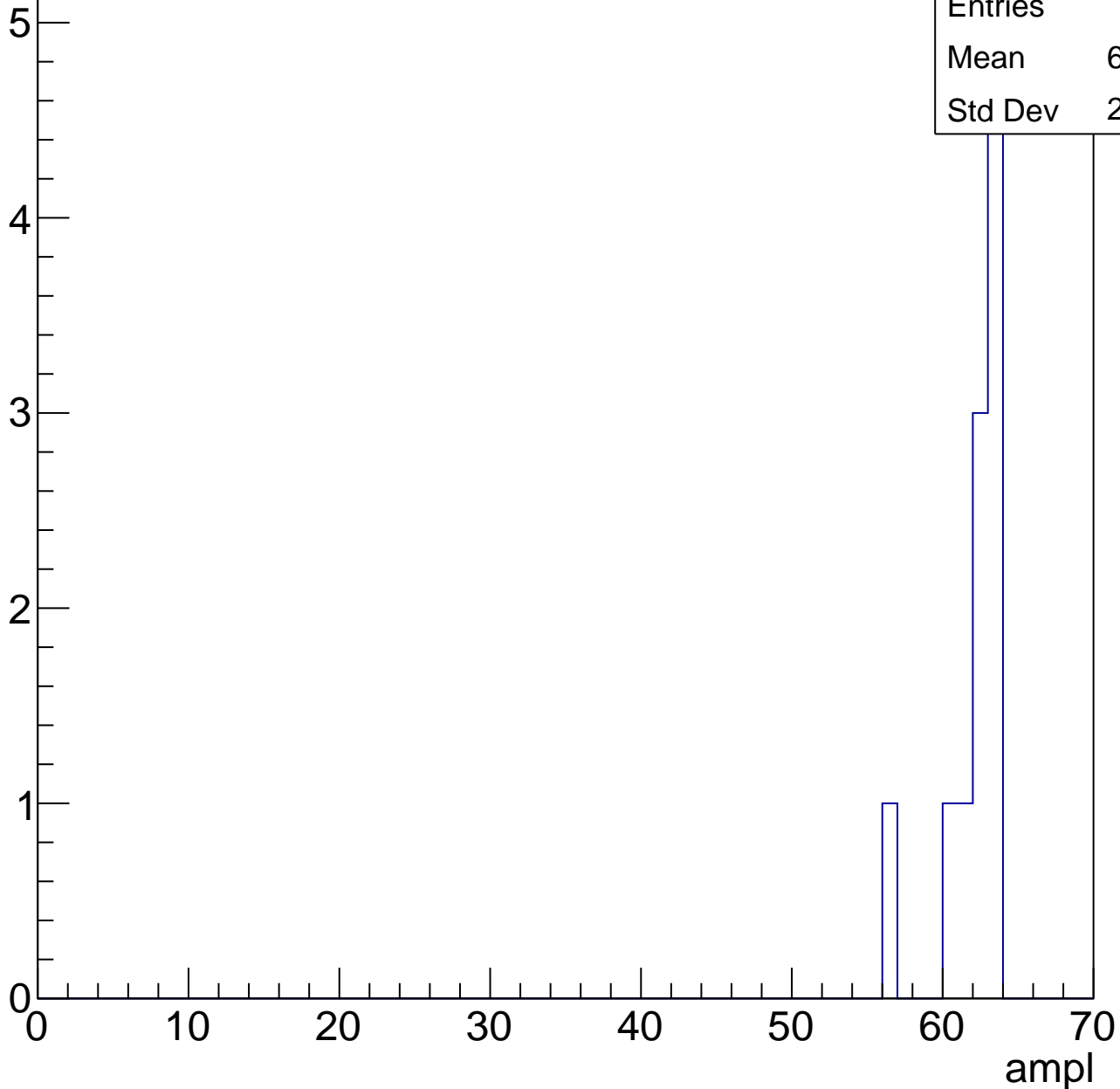


# B1L103S, U26-ch89, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	11
Mean	61.64
Std Dev	2.012



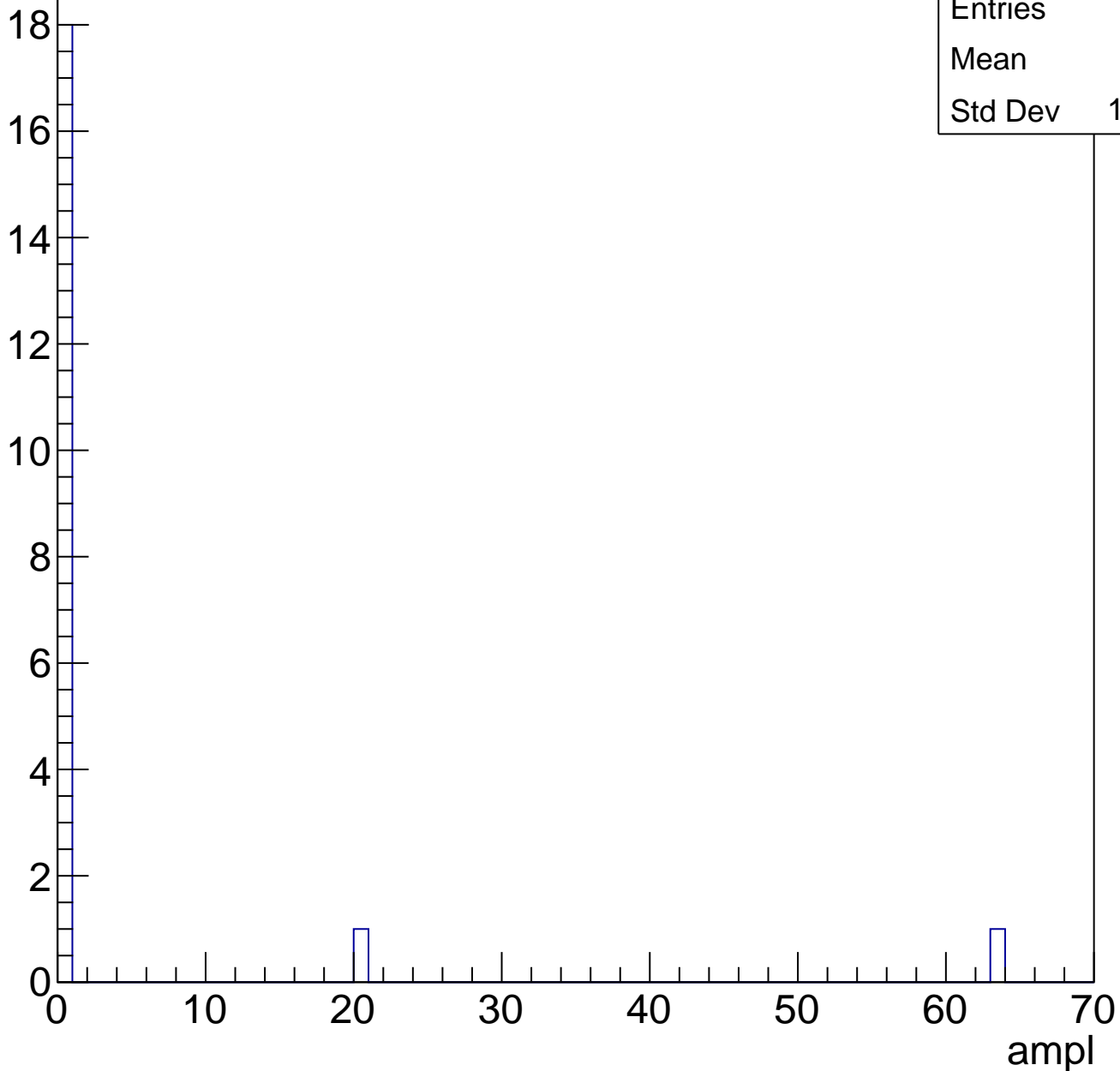


# B1L103S, U26-ch89, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	20
Mean	4.15
Std Dev	14.19

Entry



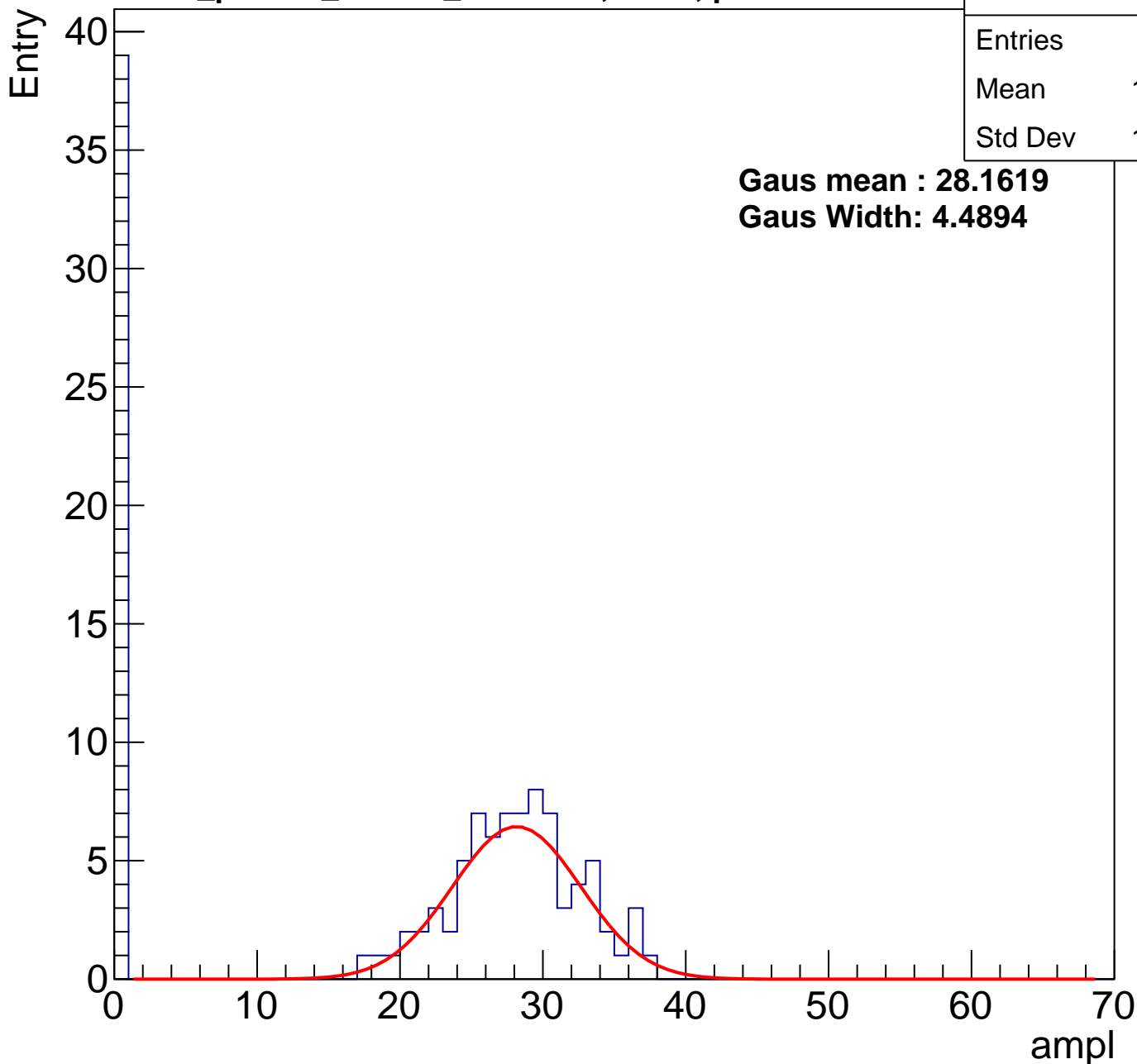
# B1L103S, U26-ch90, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	117
Mean	18.46
Std Dev	13.54

**Gaus mean : 28.1619**

**Gaus Width: 4.4894**



# B1L103S, U26-ch90, adc1

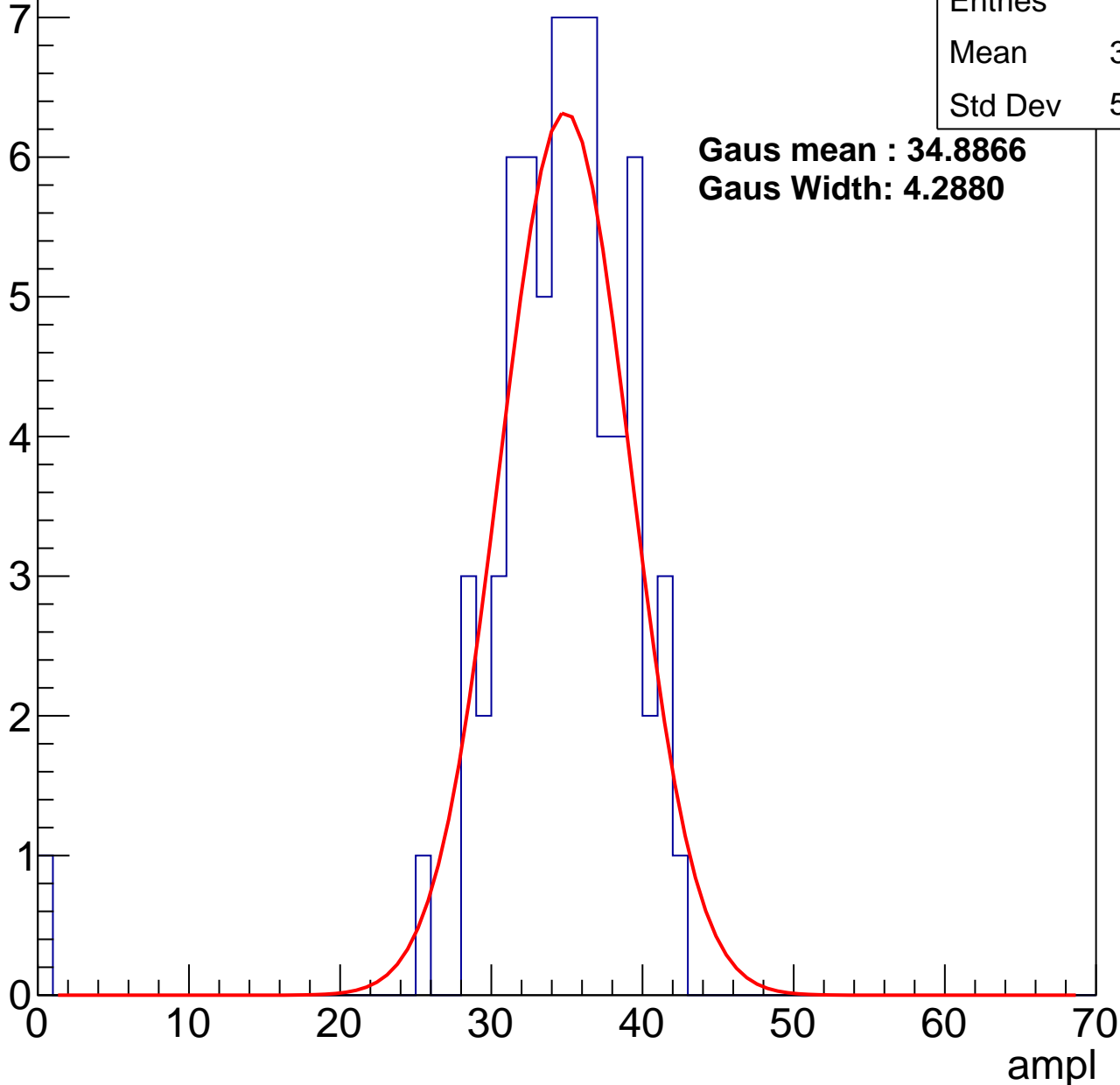
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	68
Mean	34.03
Std Dev	5.549

**Gaus mean : 34.8866**

**Gaus Width: 4.2880**



# B1L103S, U26-ch90, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	81
Mean	33.89
Std Dev	16.53

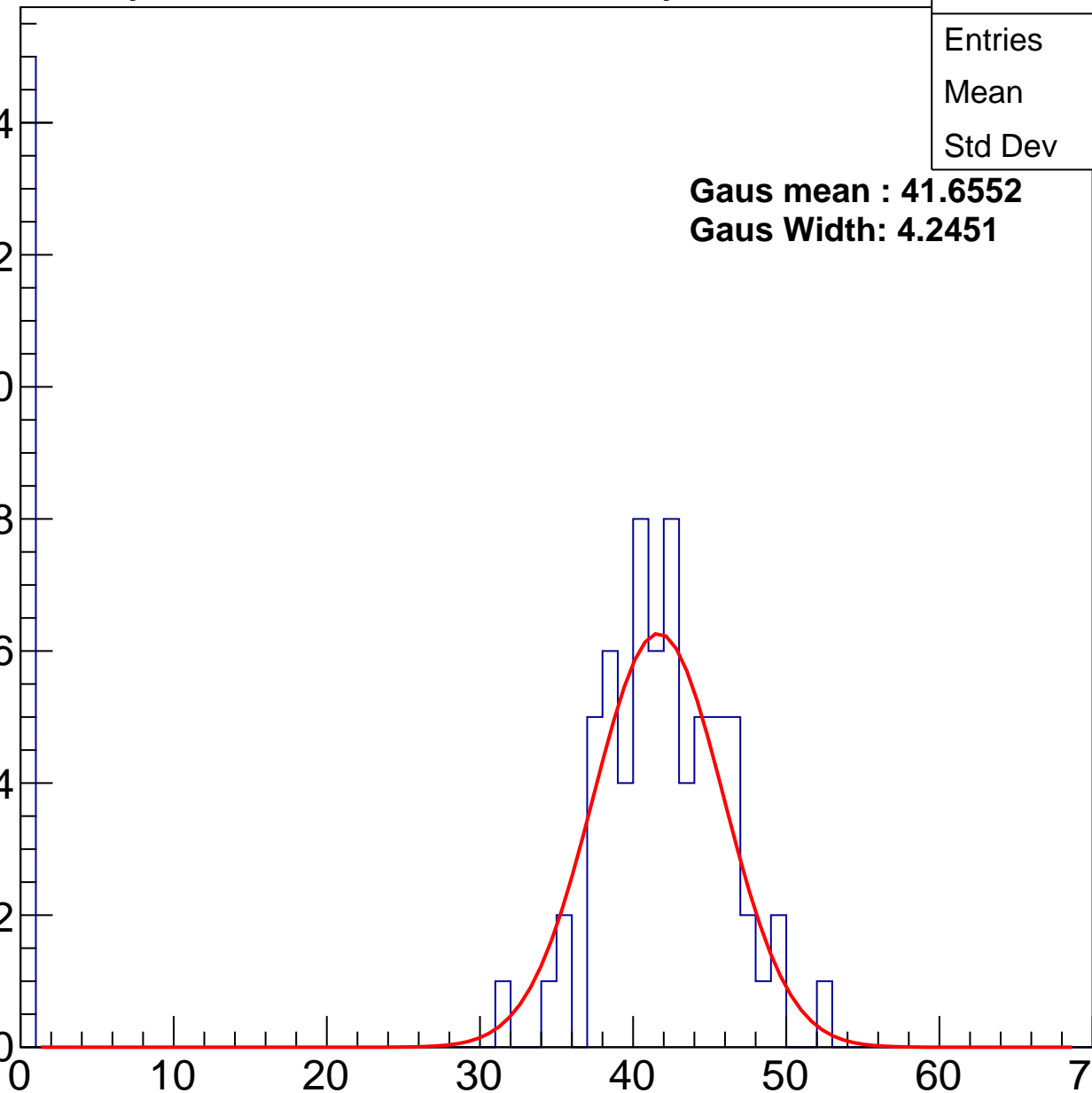
**Gaus mean : 41.6552**

**Gaus Width: 4.2451**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl

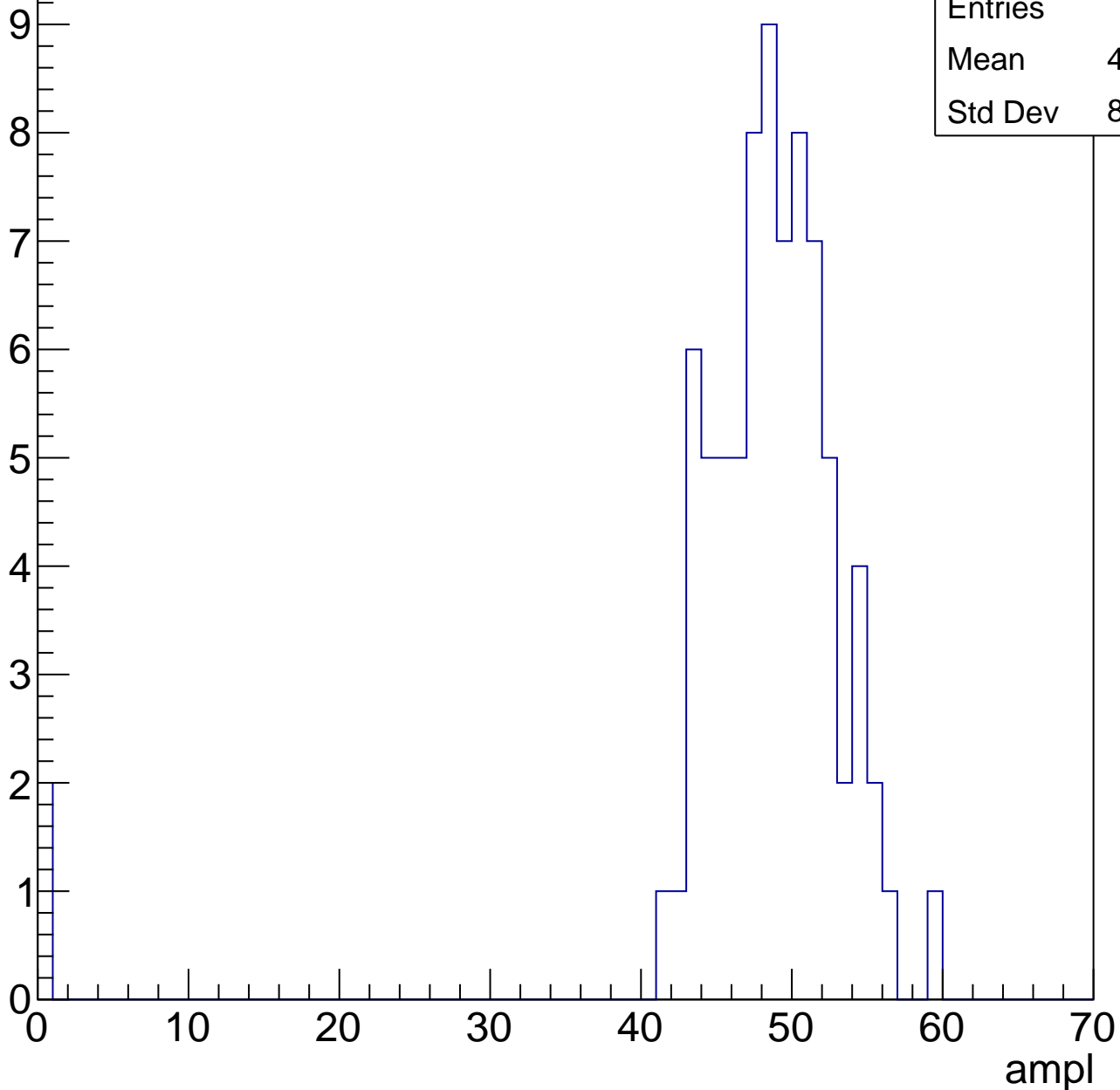


# B1L103S, U26-ch90, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	79
Mean	47.23
Std Dev	8.425



# B1L103S, U26-ch90, adc4

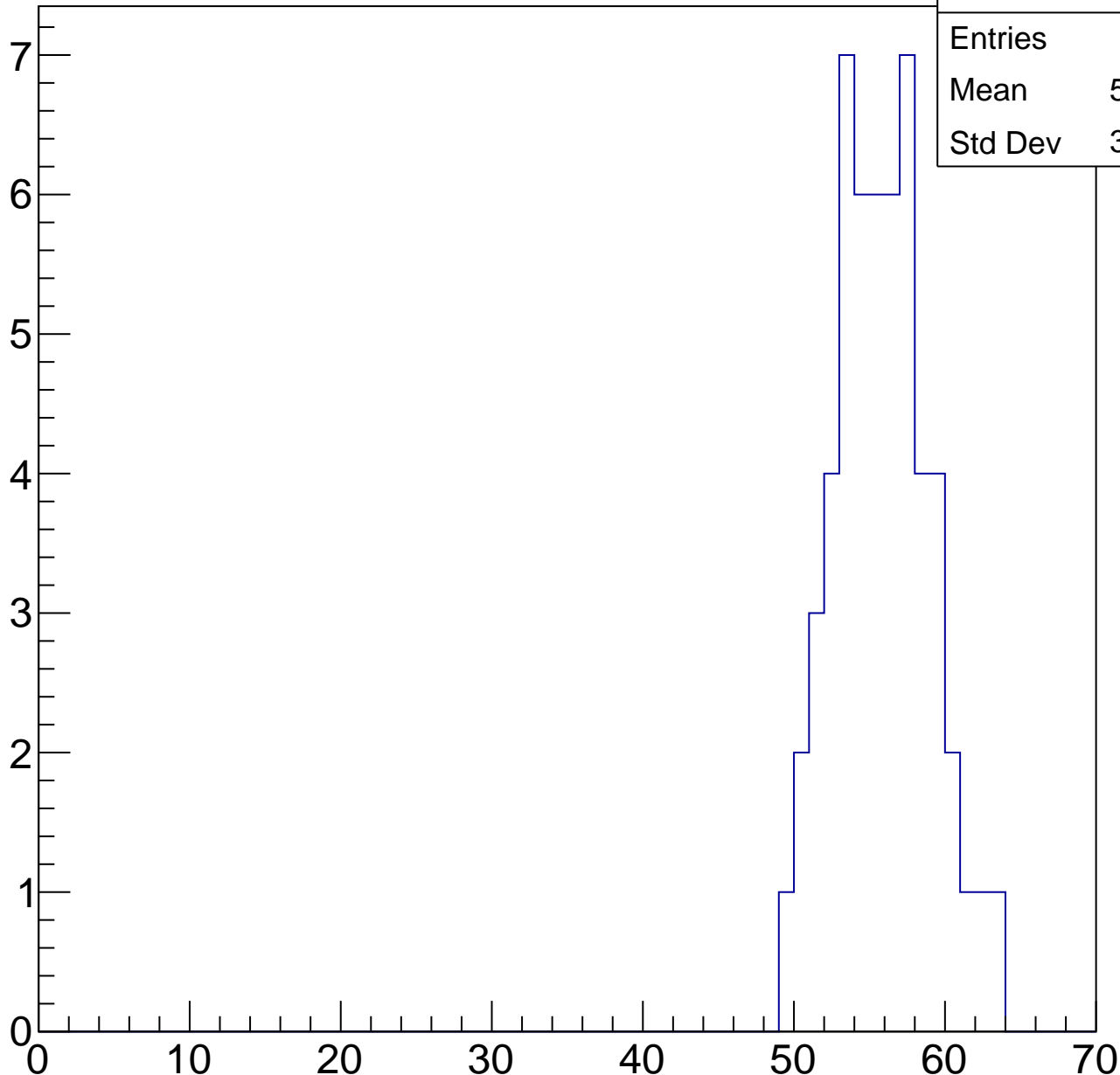
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

7  
6  
5  
4  
3  
2  
1  
0

Entries	55
Mean	55.35
Std Dev	3.106

ampl

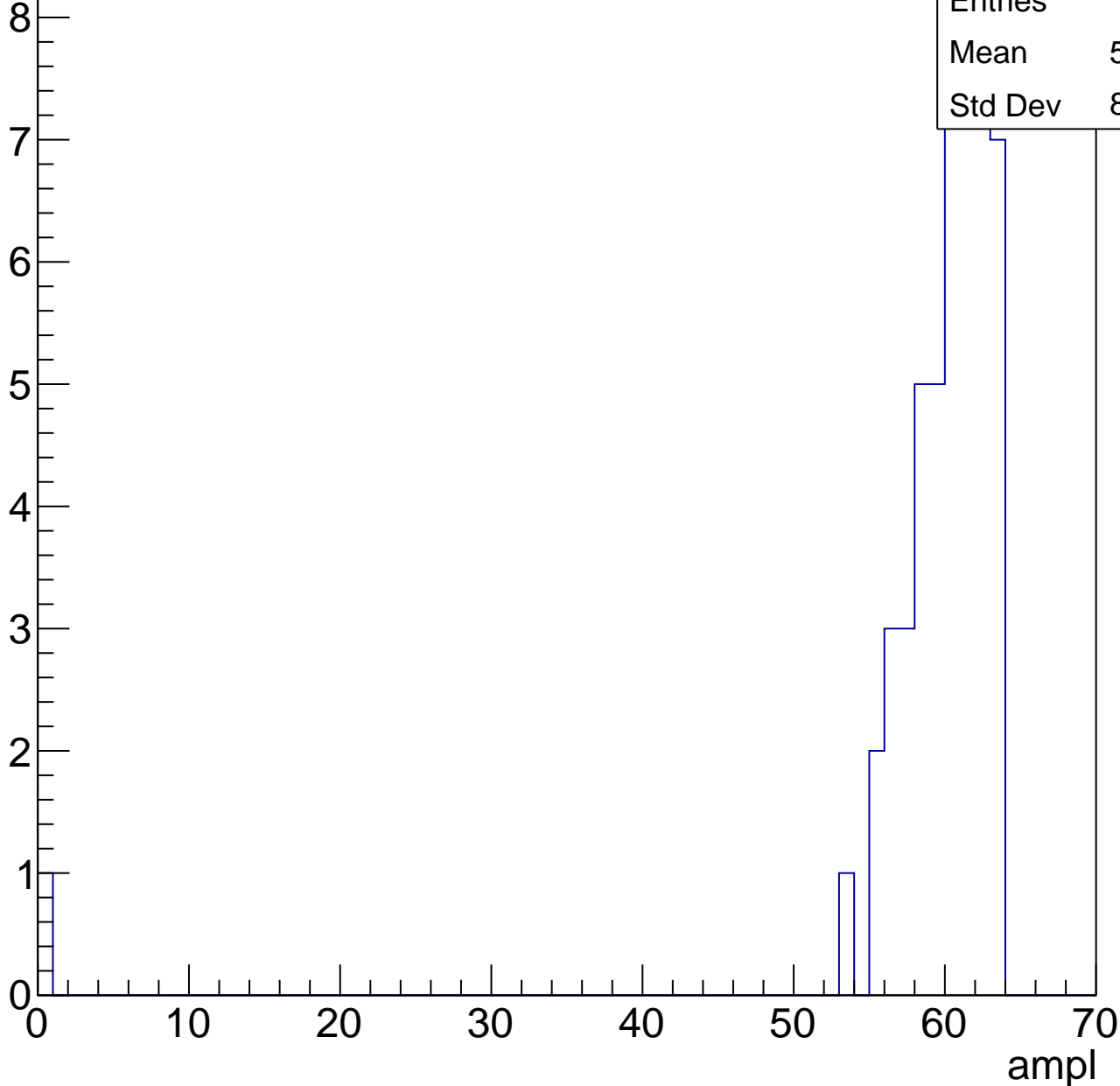


# B1L103S, U26-ch90, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

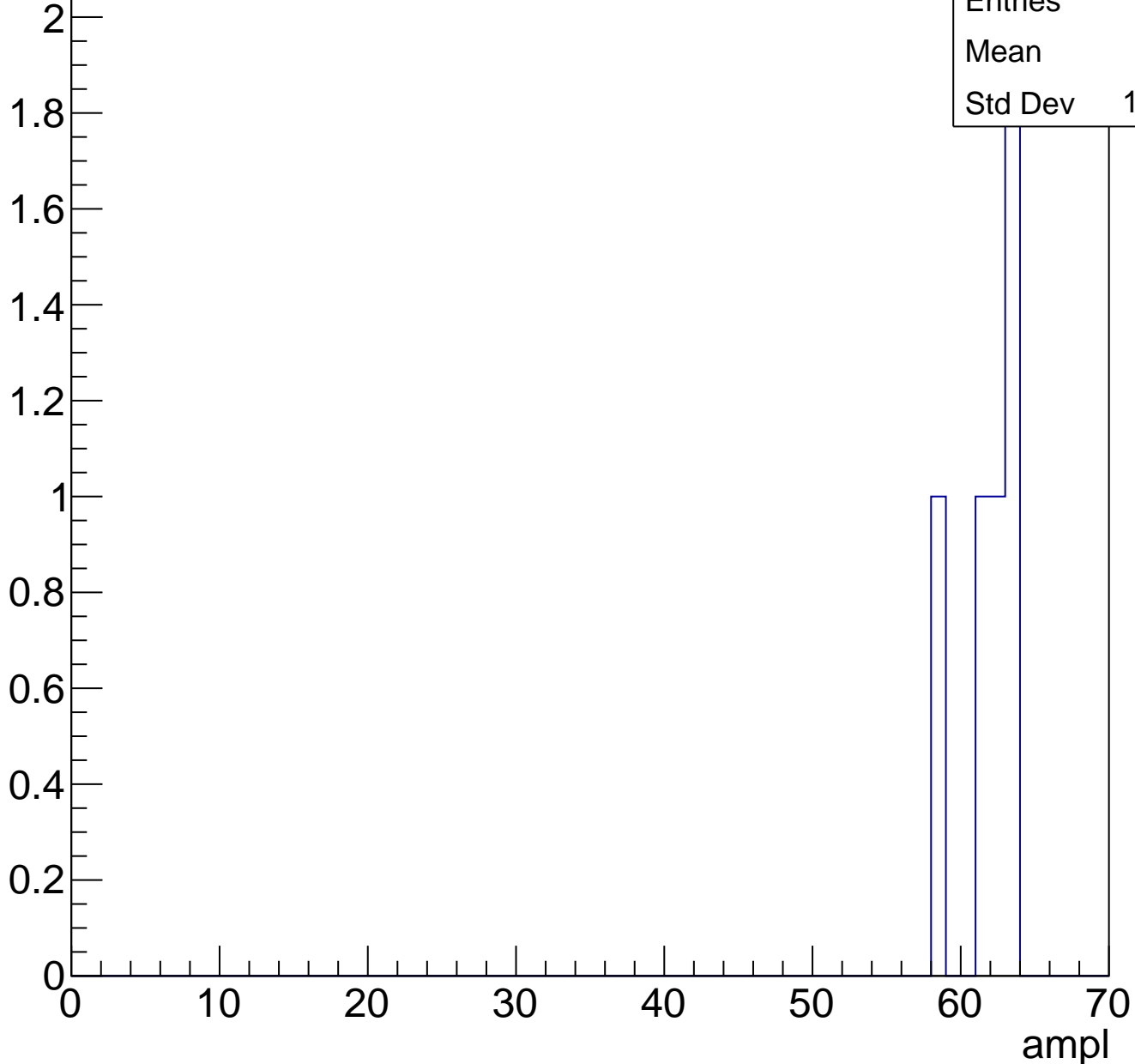
Entries	51
Mean	58.67
Std Dev	8.645



# B1L103S, U26-ch90, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



Entries	5
Mean	61.4
Std Dev	1.855



# B1L103S, U26-ch90, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



# B1L103S, U26-ch91, adc0

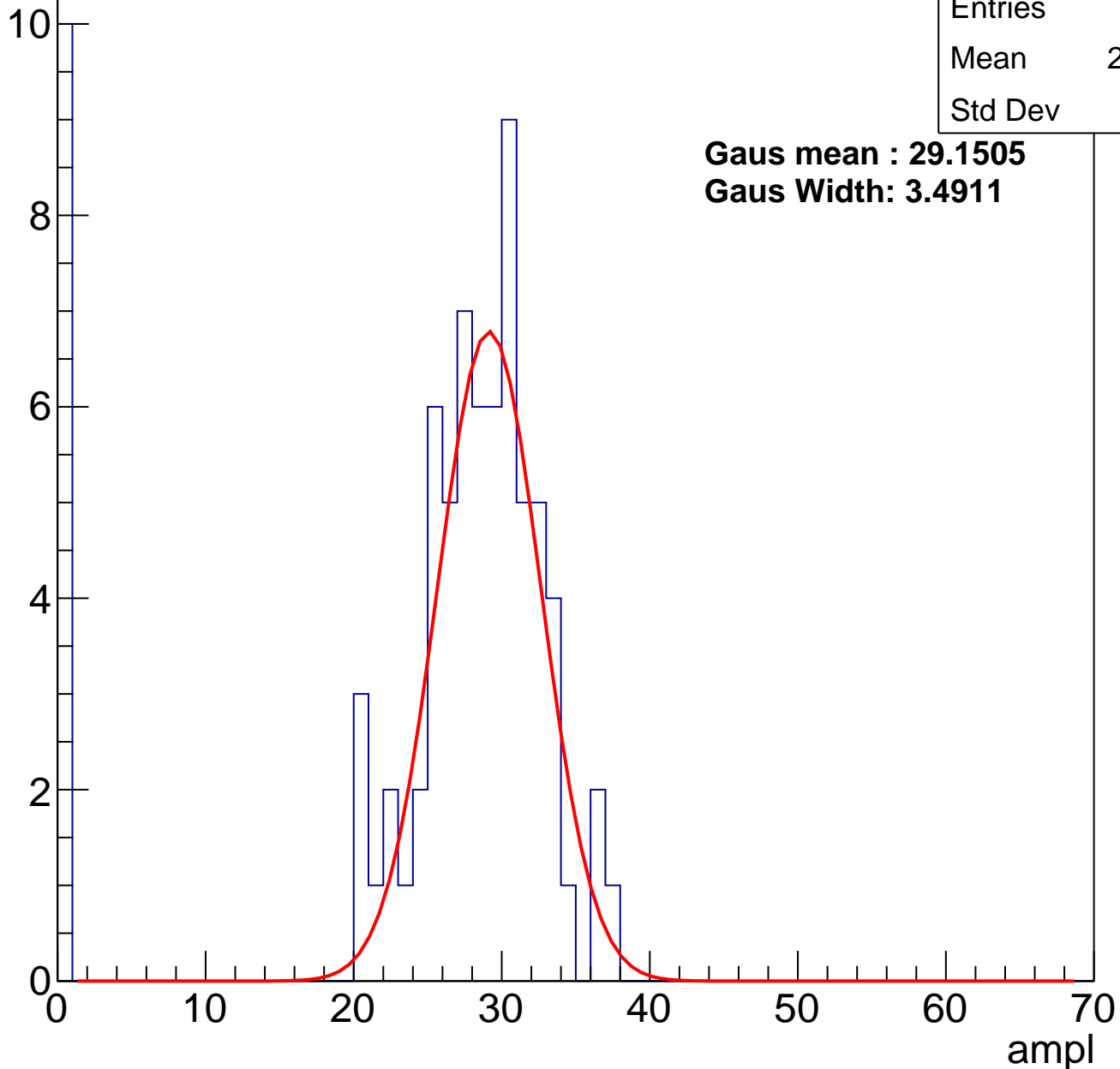
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	76
Mean	24.57
Std Dev	10.2

**Gaus mean : 29.1505**

**Gaus Width: 3.4911**

Entry



# B1L103S, U26-ch91, adc1

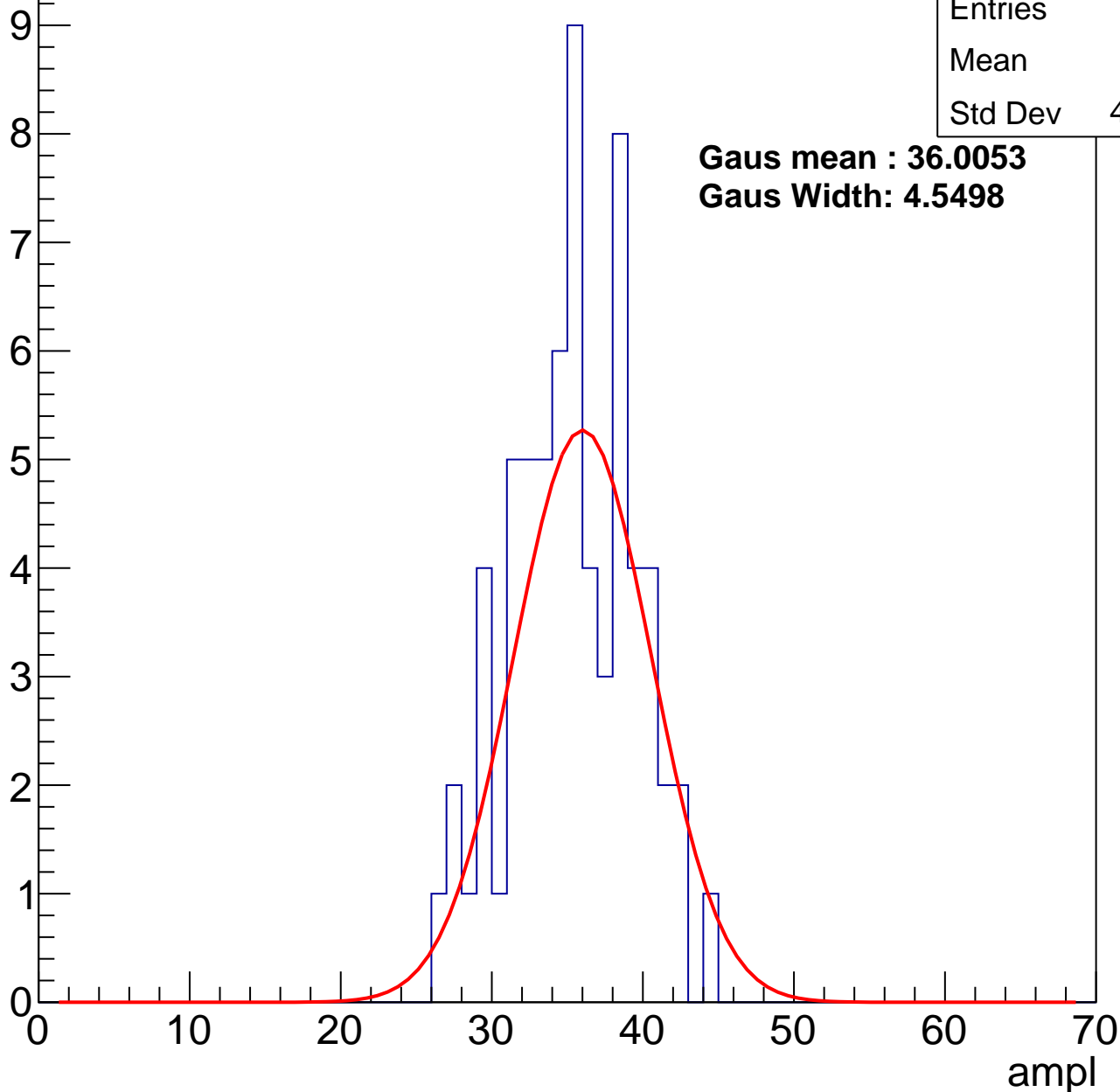
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	67
Mean	34.9
Std Dev	4.015

**Gaus mean : 36.0053**

**Gaus Width: 4.5498**



# B1L103S, U26-ch91, adc2

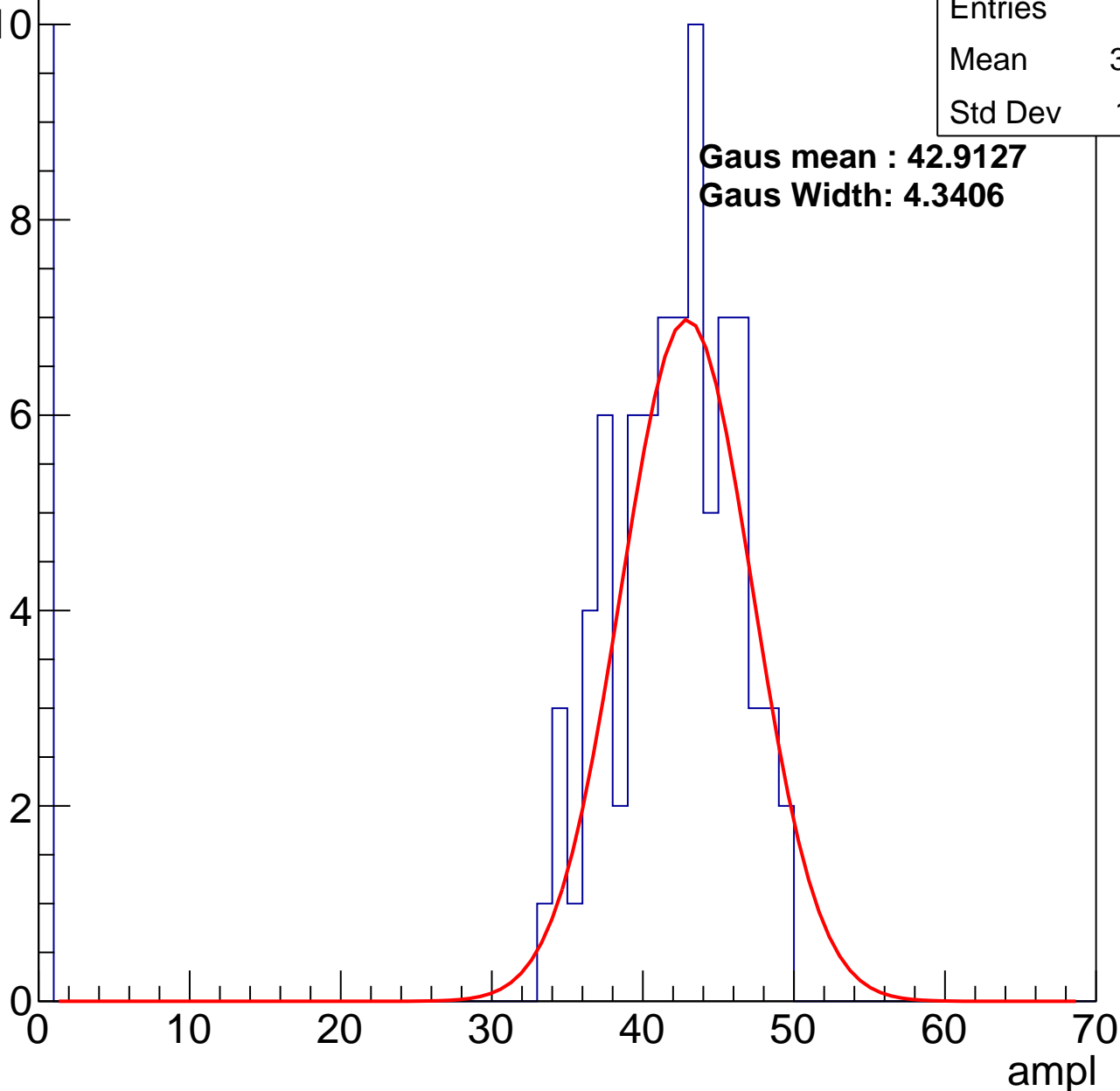
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	90
Mean	37.08
Std Dev	13.61

**Gaus mean : 42.9127**

**Gaus Width: 4.3406**

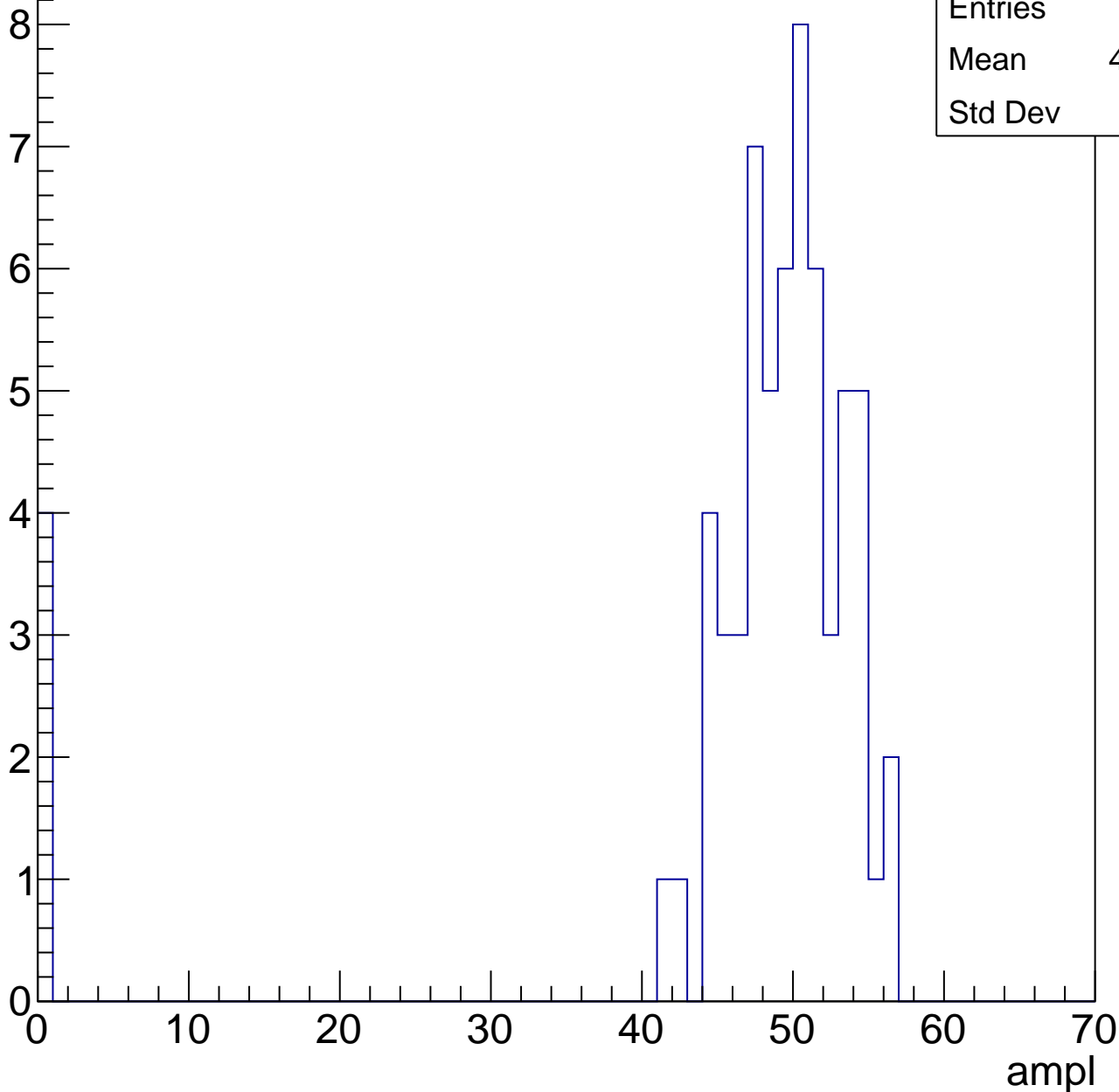


# B1L103S, U26-ch91, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	64
Mean	46.23
Std Dev	12.4

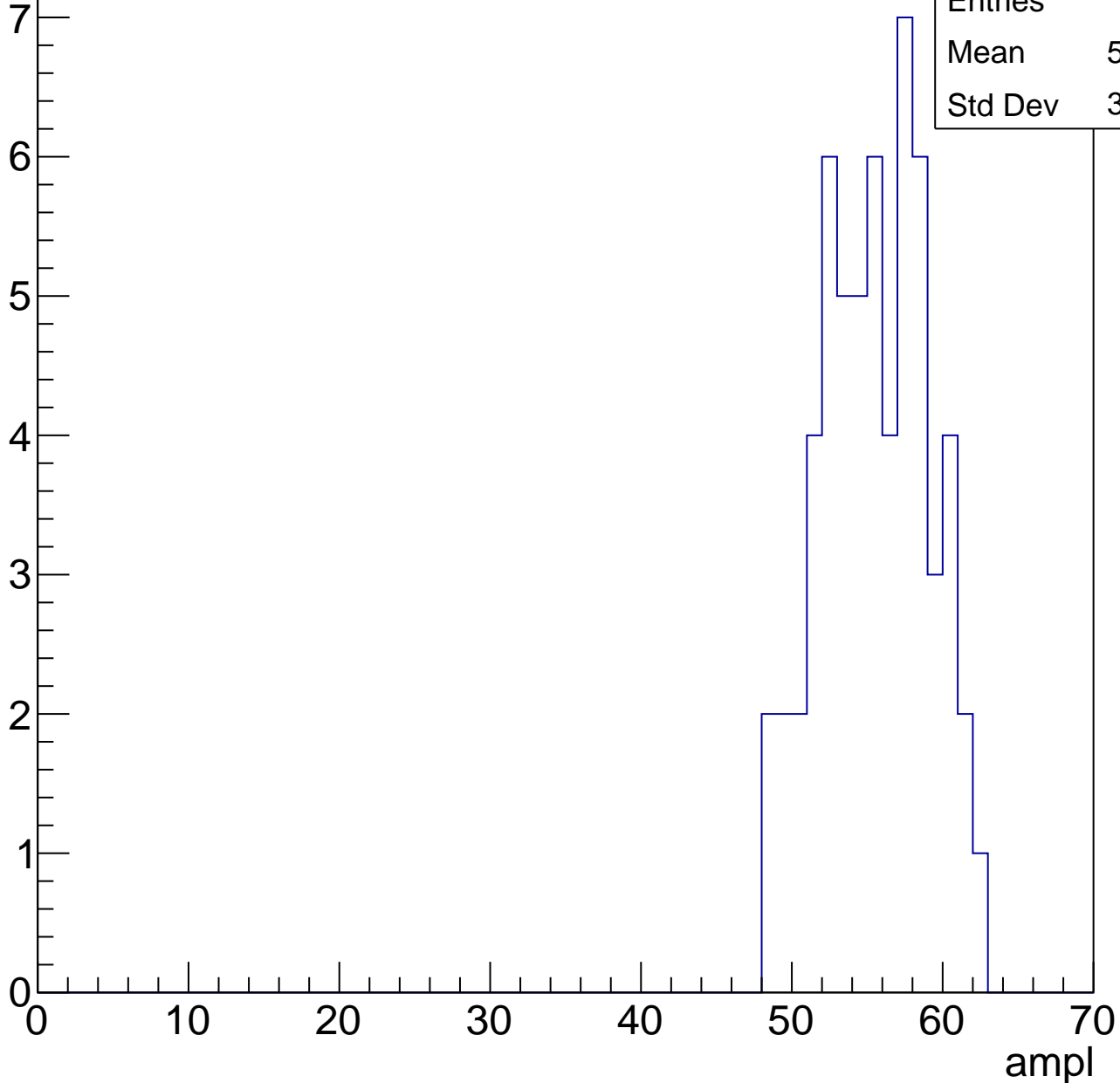


# B1L103S, U26-ch91, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	59
Mean	55.03
Std Dev	3.488



# B1L103S, U26-ch91, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

7

6

5

4

3

2

1

0

Entries 48

Mean 58.25

Std Dev 8.892

ampl

0

10

20

30

40

50

60

70

0

10

20

30

40

50

60

70

0

10

20

30

40

50

60

70

0

10

20

30

40

50

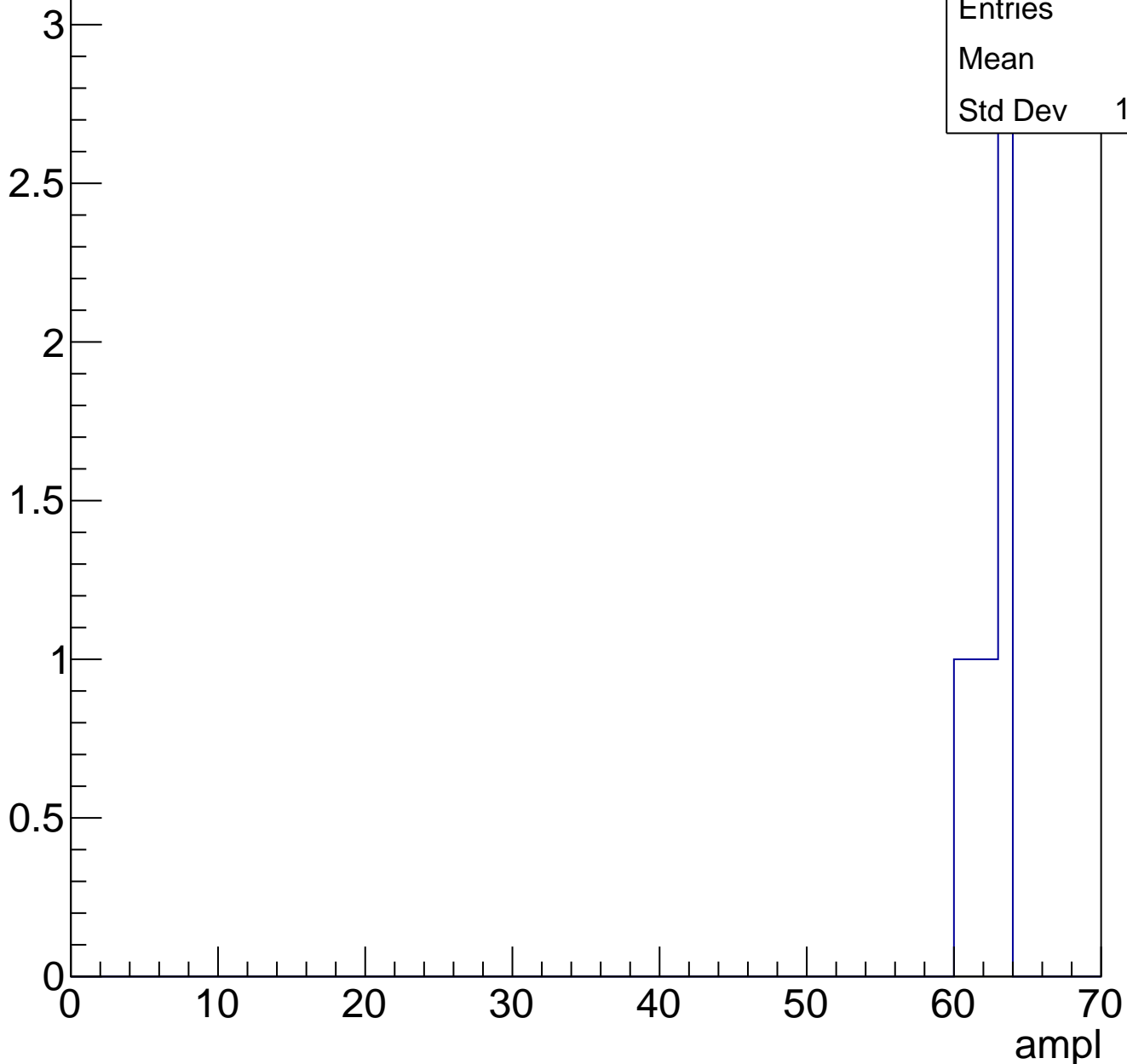
60

70

# B1L103S, U26-ch91, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



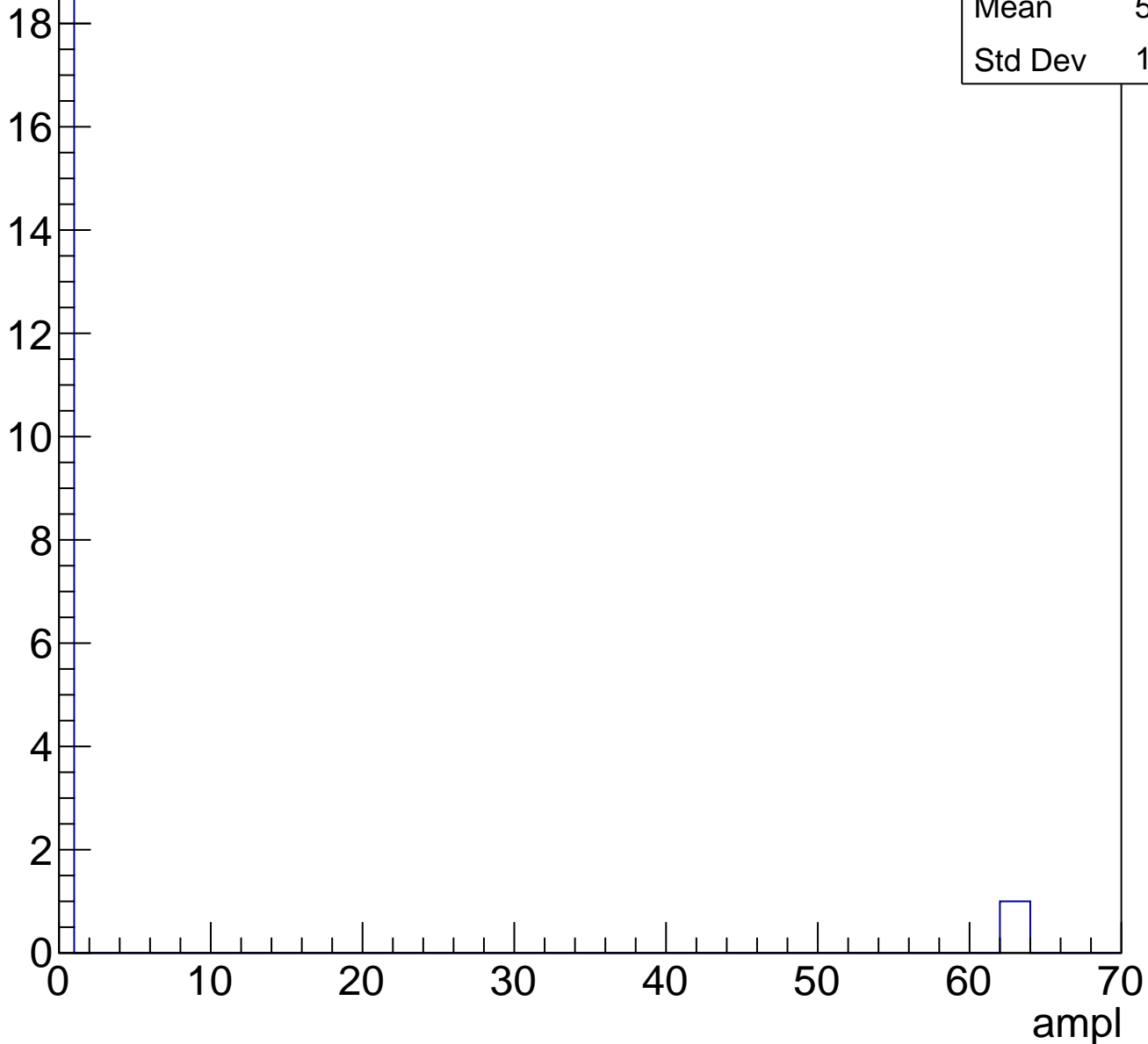


# B1L103S, U26-ch91, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	21
Mean	5.952
Std Dev	18.35

Entry



# B1L103S, U26-ch92, adc0

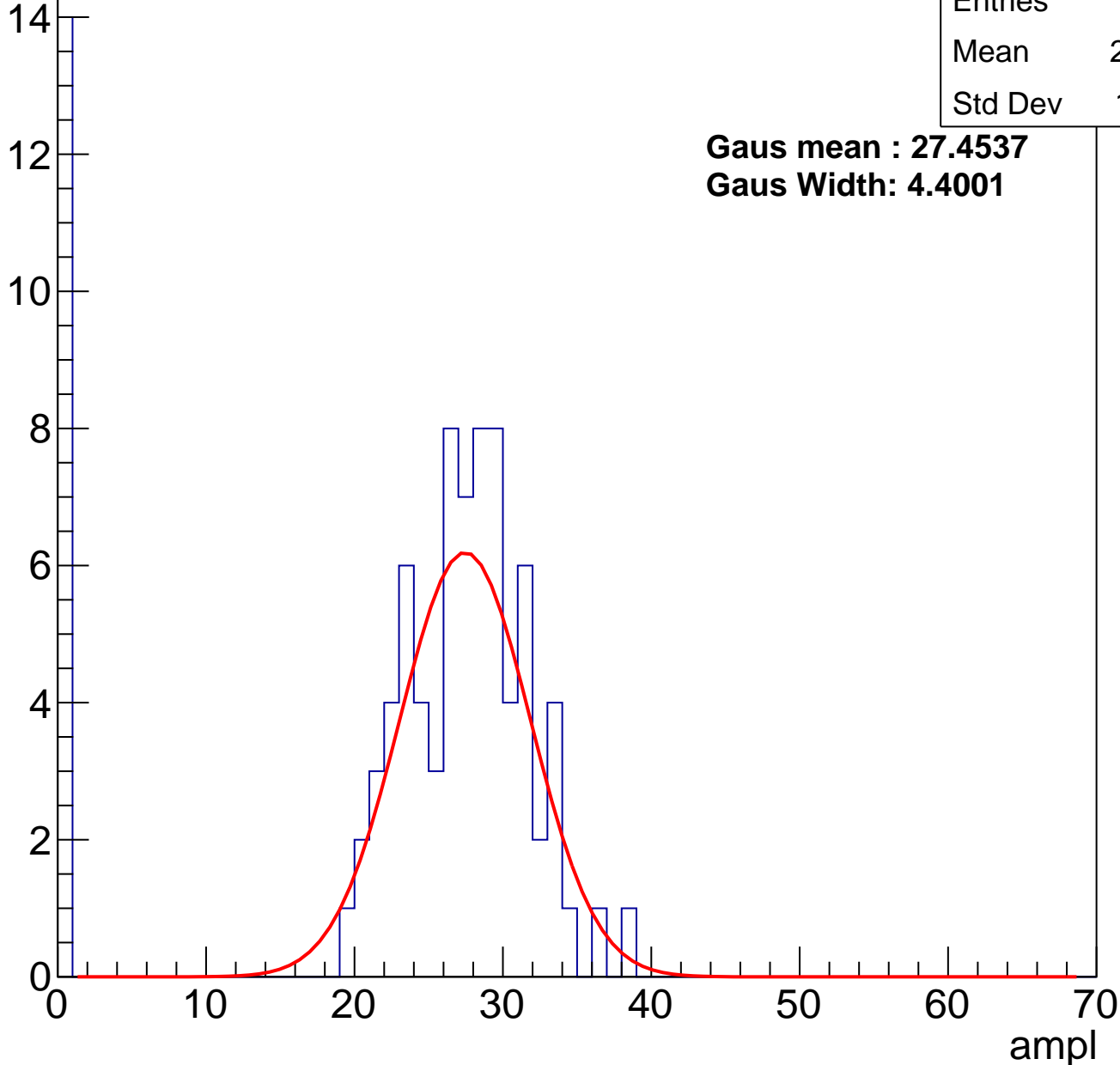
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	87
Mean	22.78
Std Dev	10.61

**Gaus mean : 27.4537**

**Gaus Width: 4.4001**

Entry



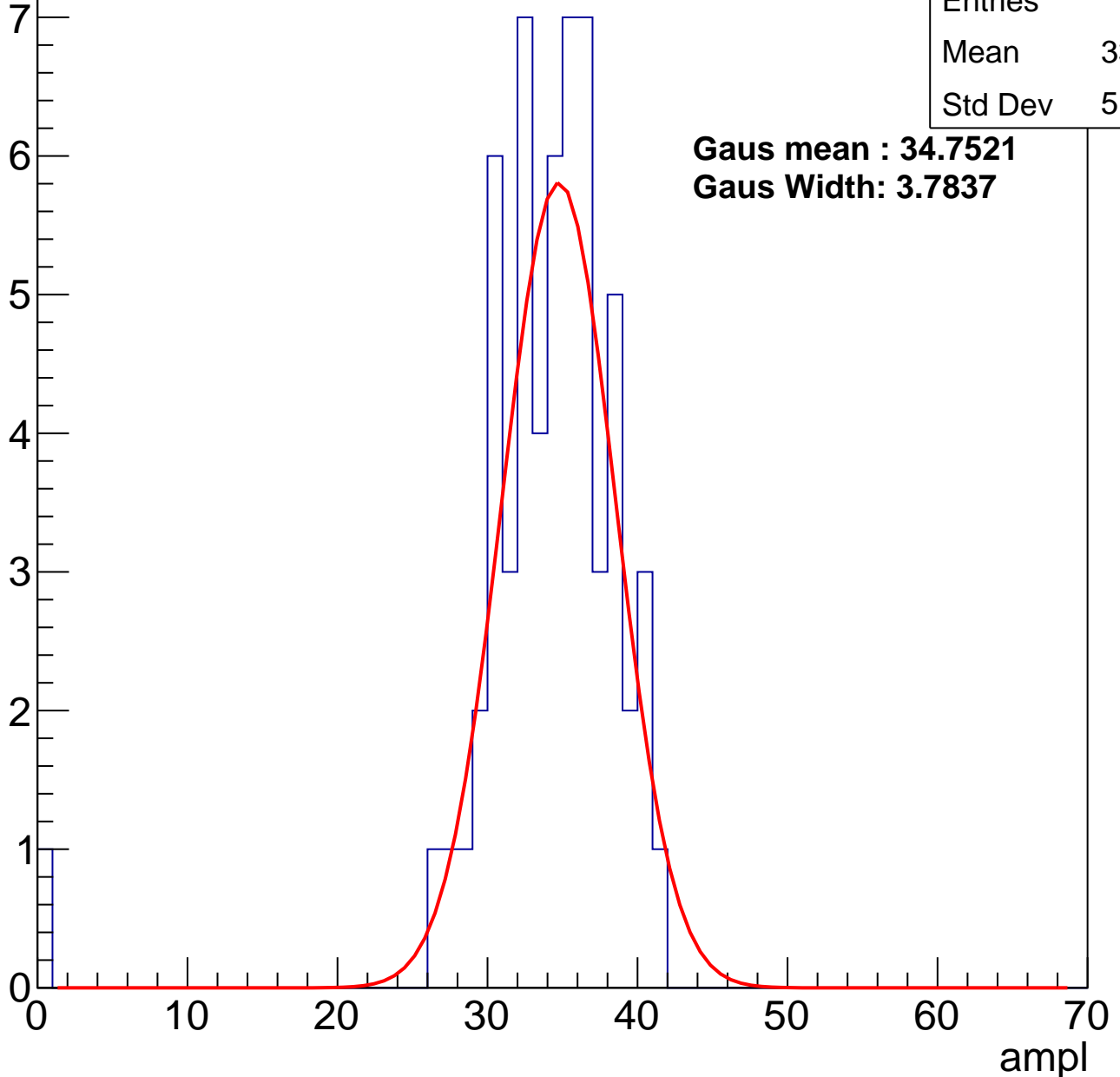
# B1L103S, U26-ch92, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	60
Mean	33.48
Std Dev	5.542

**Gaus mean : 34.7521**  
**Gaus Width: 3.7837**



# B1L103S, U26-ch92, adc2

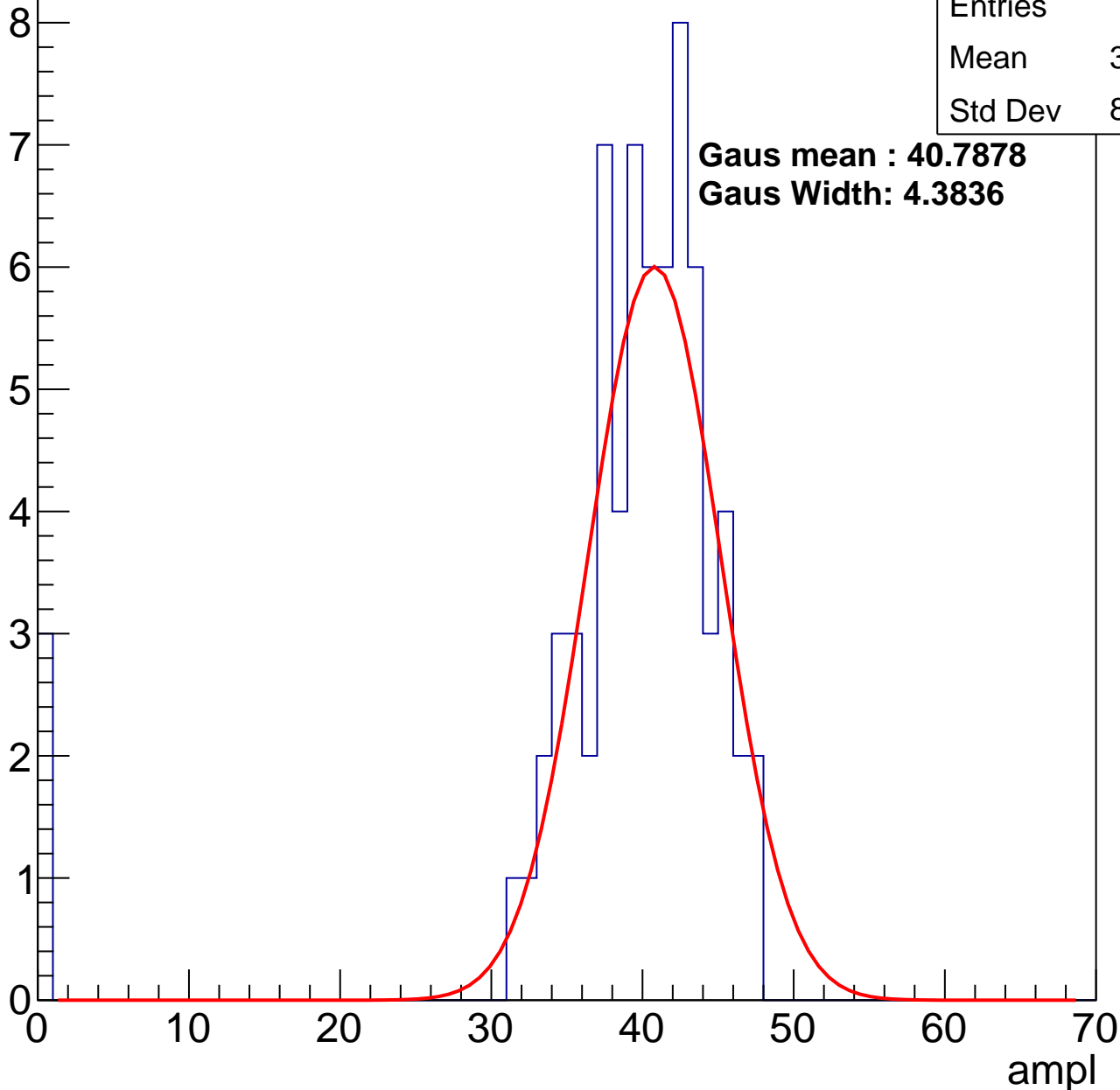
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	70
Mean	38.14
Std Dev	8.874

**Gaus mean : 40.7878**

**Gaus Width: 4.3836**

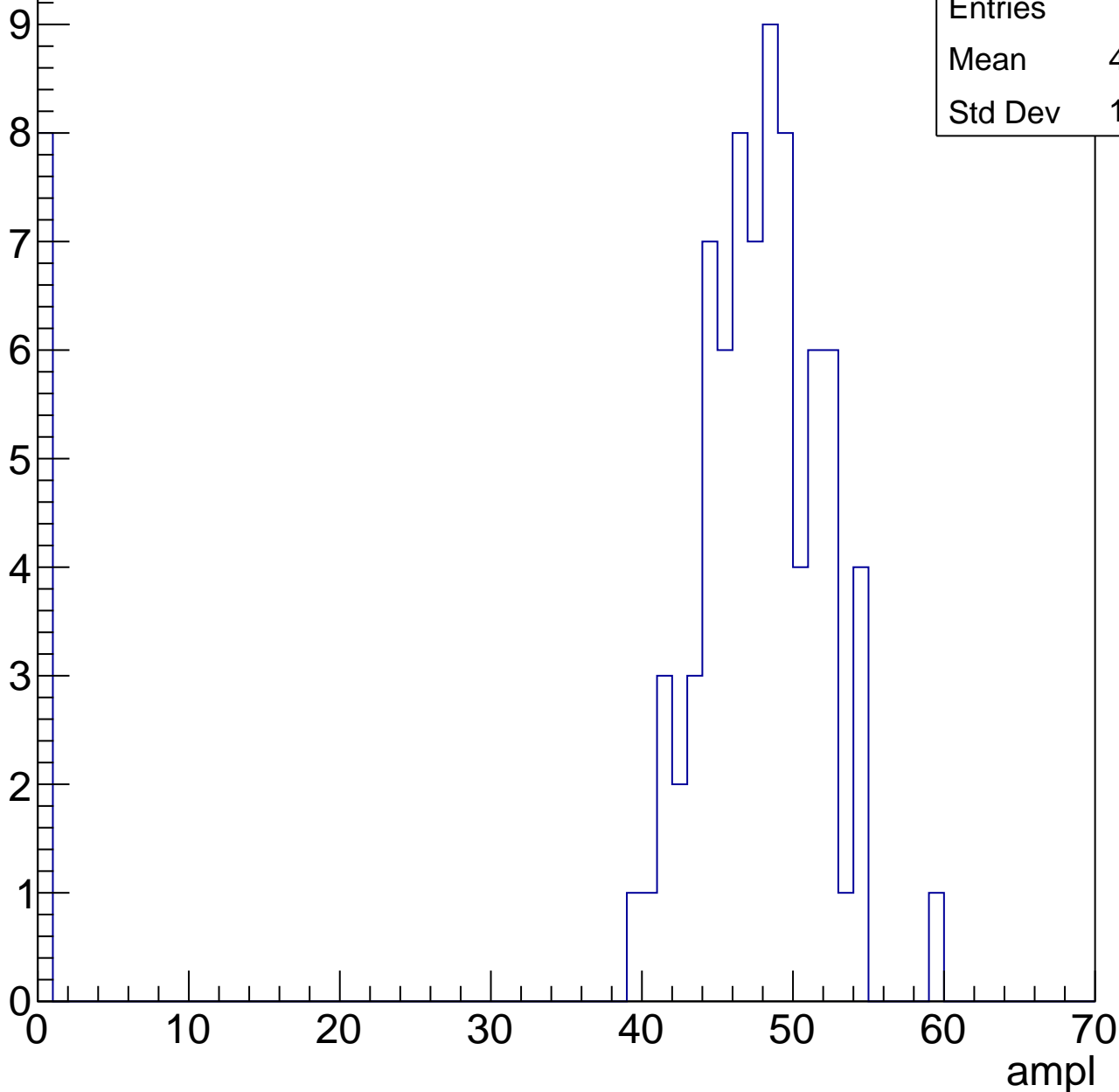


# B1L103S, U26-ch92, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	85
Mean	43.06
Std Dev	14.33

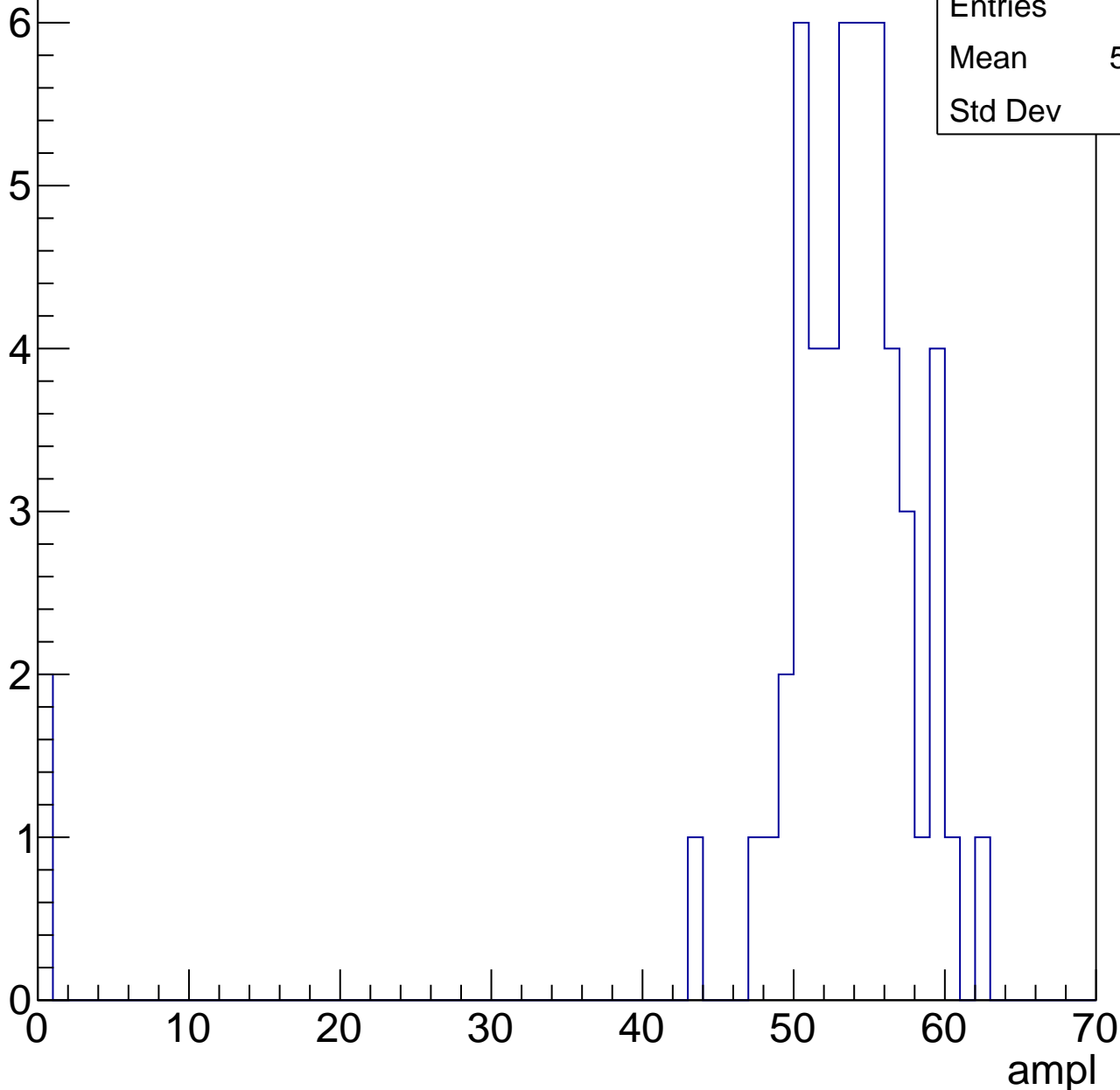


# B1L103S, U26-ch92, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

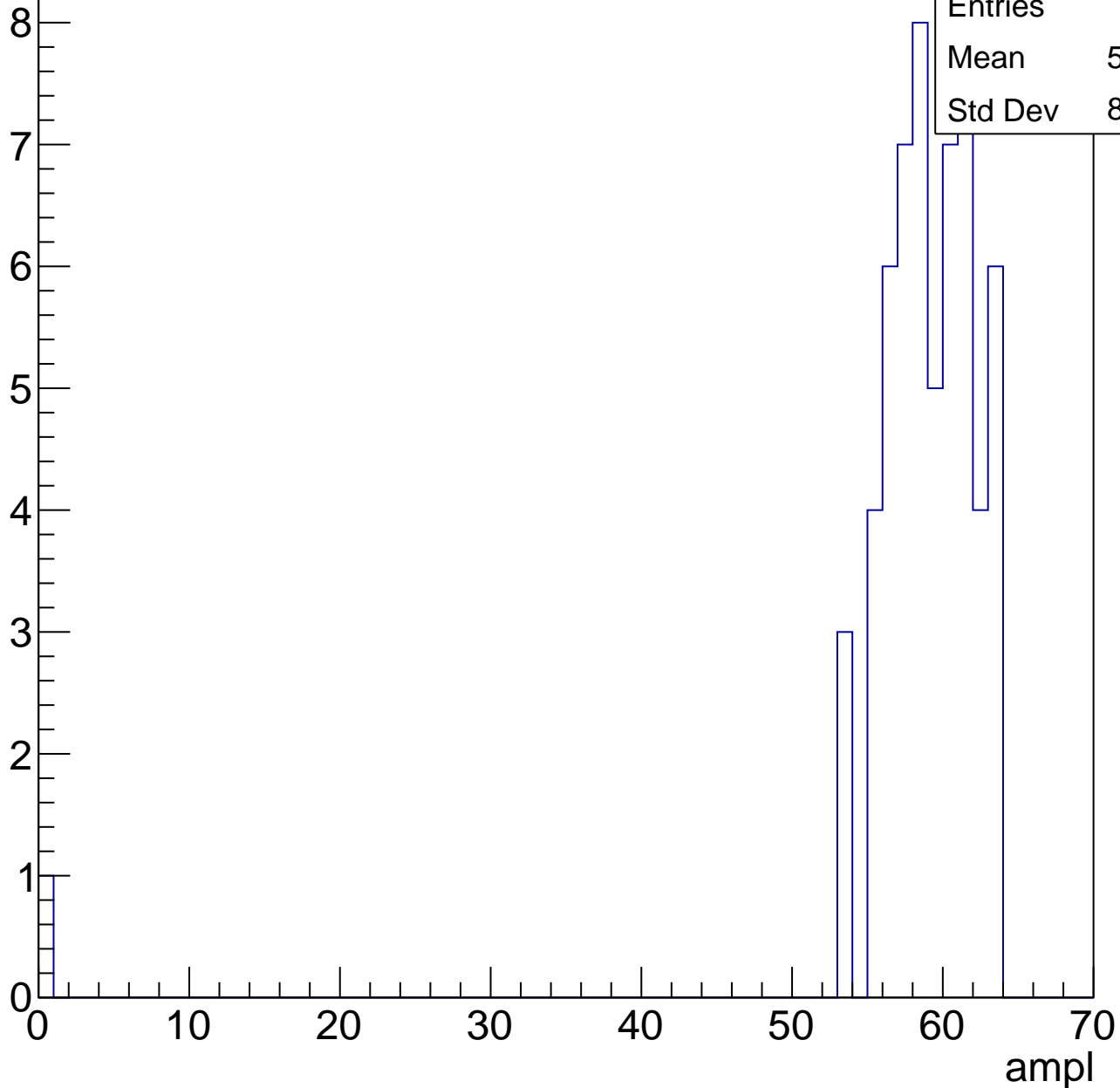
Entries	53
Mean	51.53
Std Dev	10.8



# B1L103S, U26-ch92, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

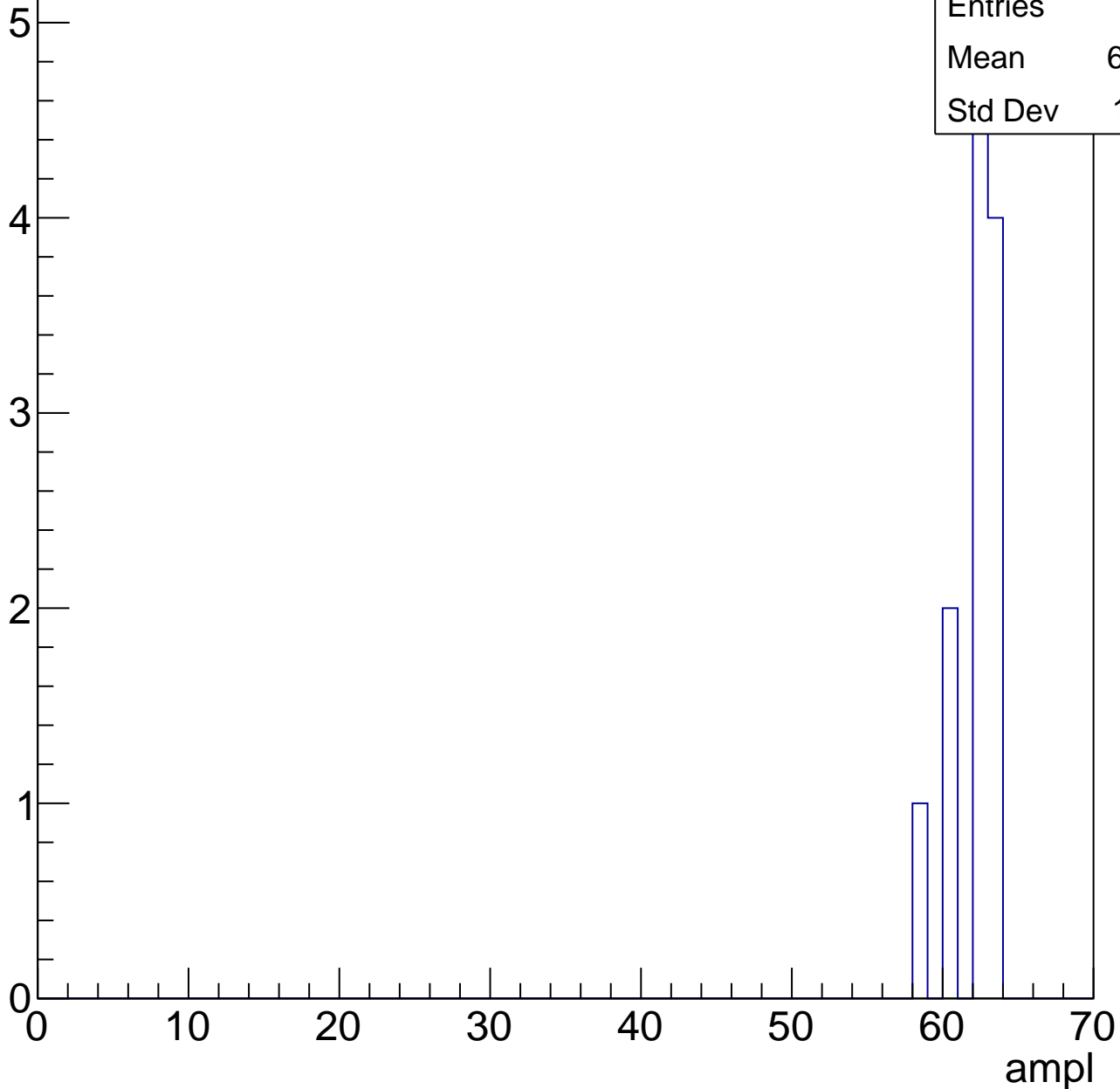


# B1L103S, U26-ch92, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	12
Mean	61.67
Std Dev	1.491



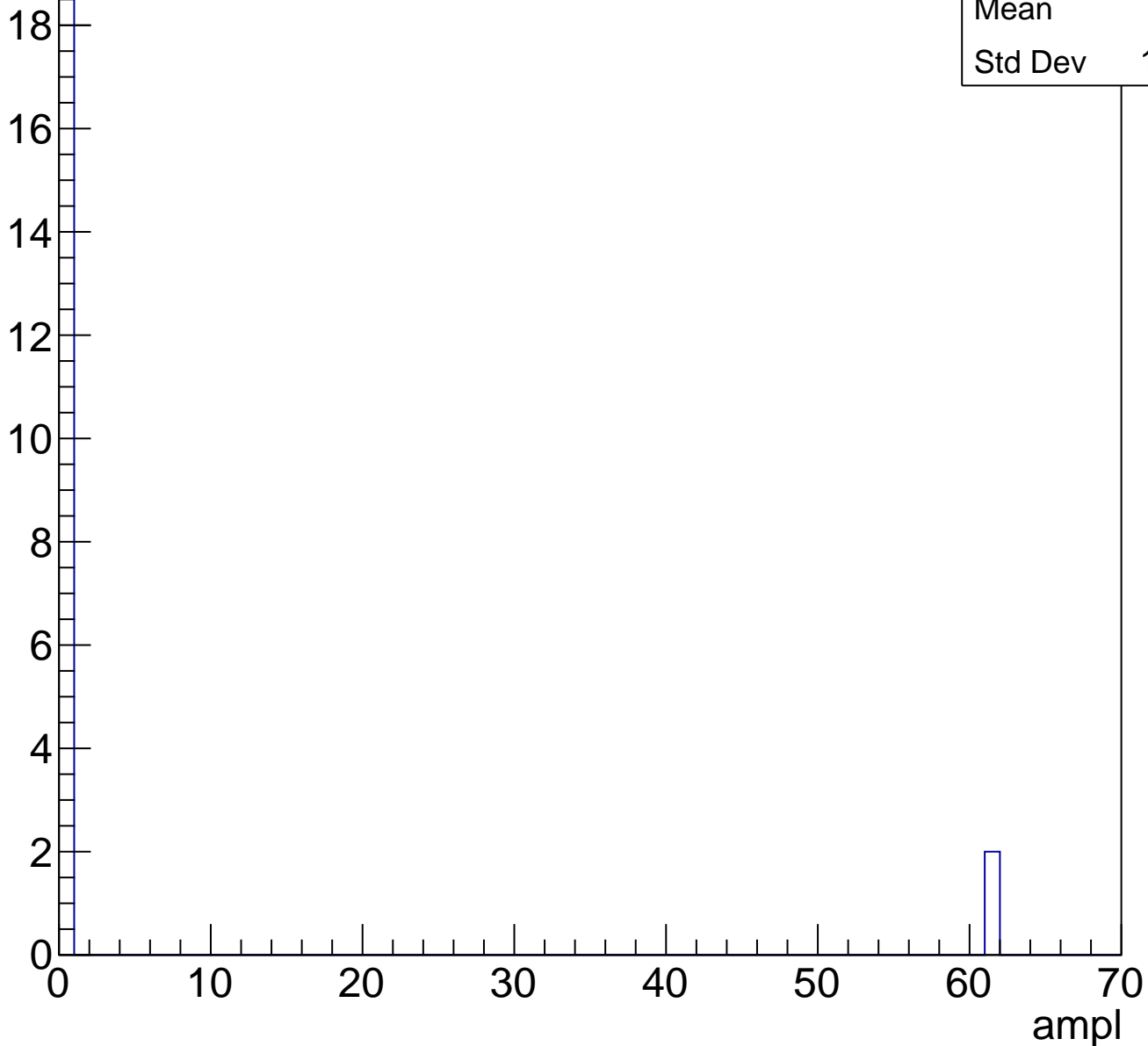


# B1L103S, U26-ch92, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	21
Mean	5.81
Std Dev	17.91

Entry



# B1L103S, U26-ch93, adc0

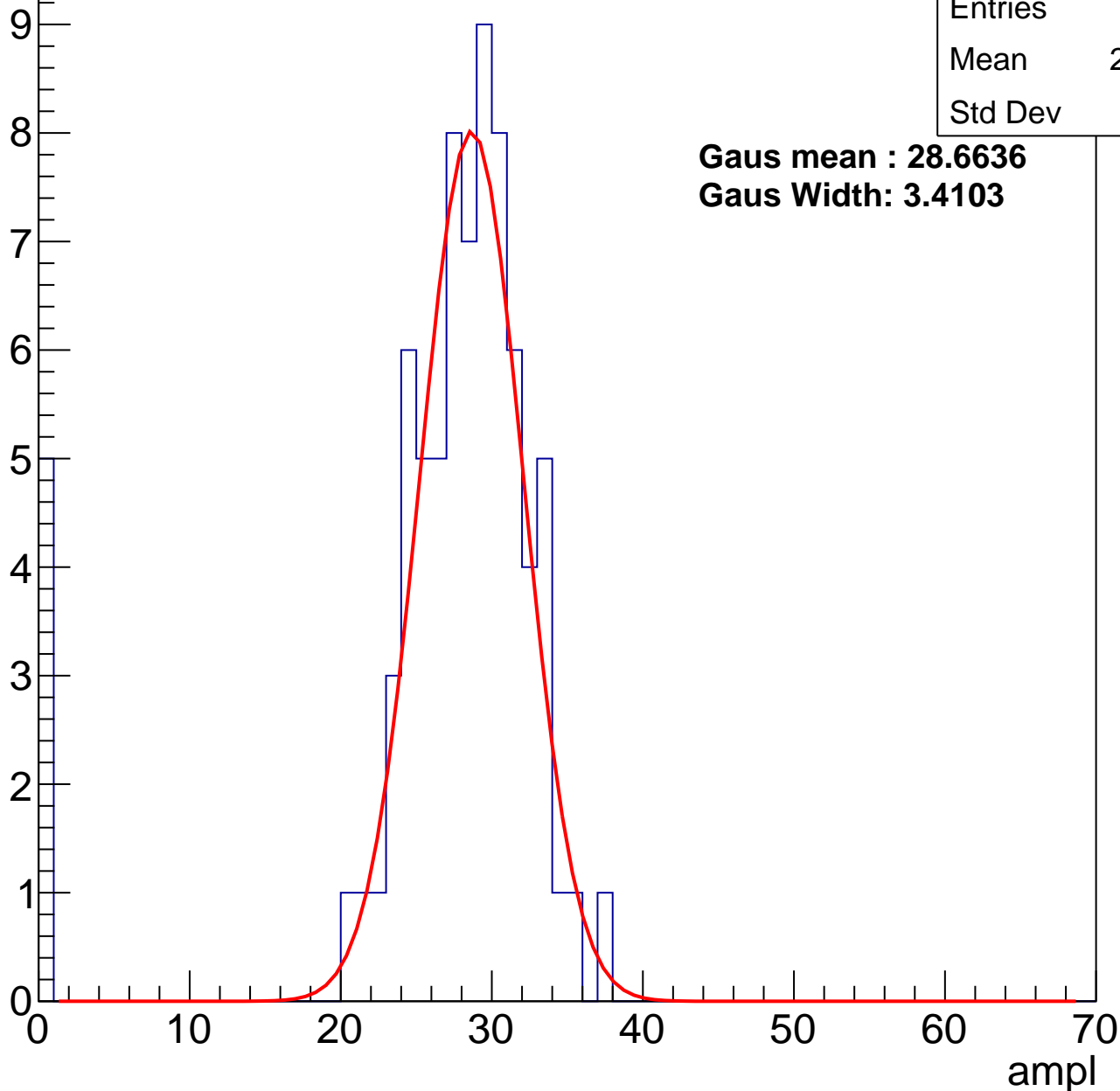
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	77
Mean	26.35
Std Dev	7.69

**Gaus mean : 28.6636**

**Gaus Width: 3.4103**



# B1L103S, U26-ch93, adc1

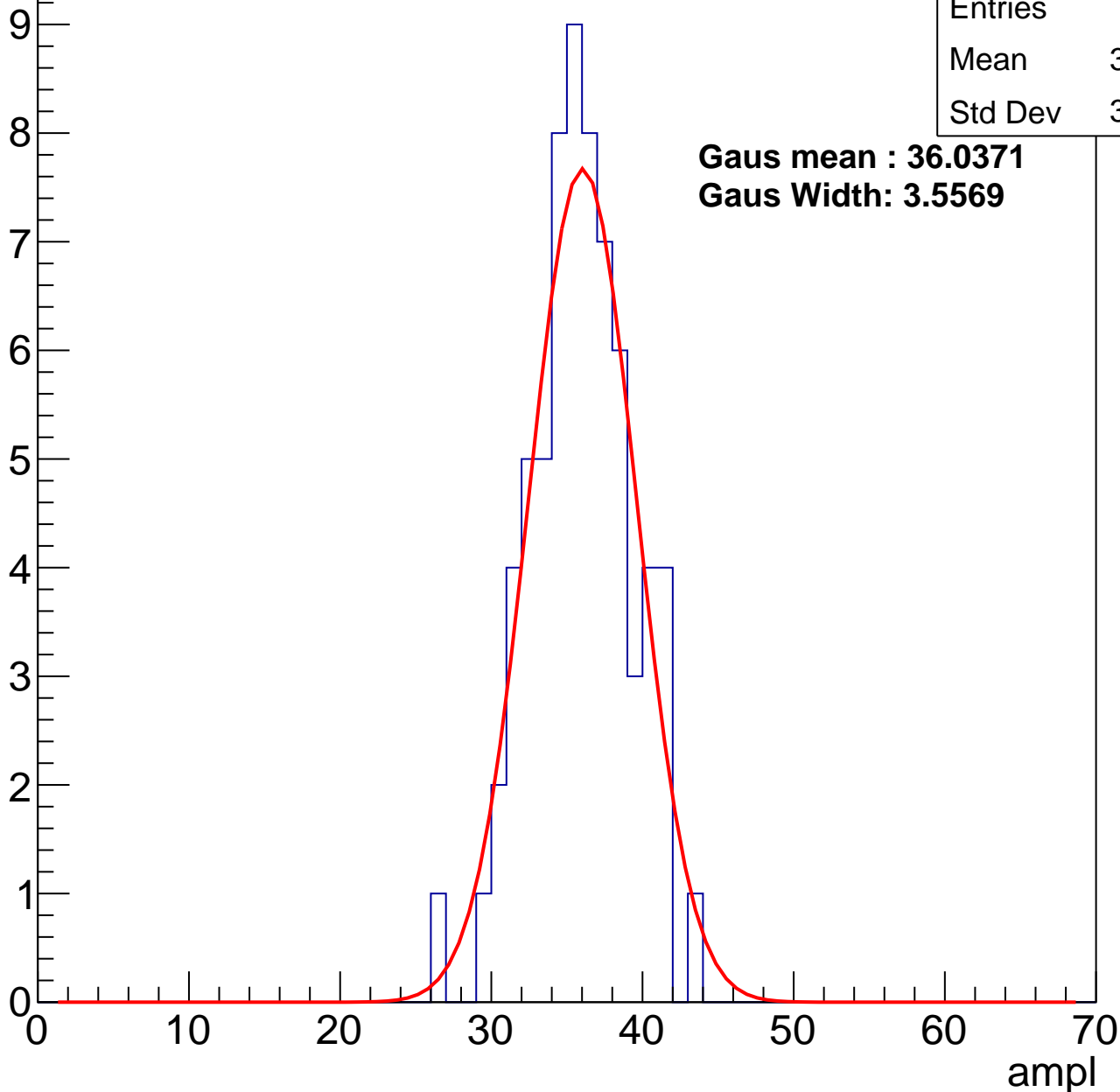
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	68
Mean	35.44
Std Dev	3.292

**Gaus mean : 36.0371**

**Gaus Width: 3.5569**



# B1L103S, U26-ch93, adc2

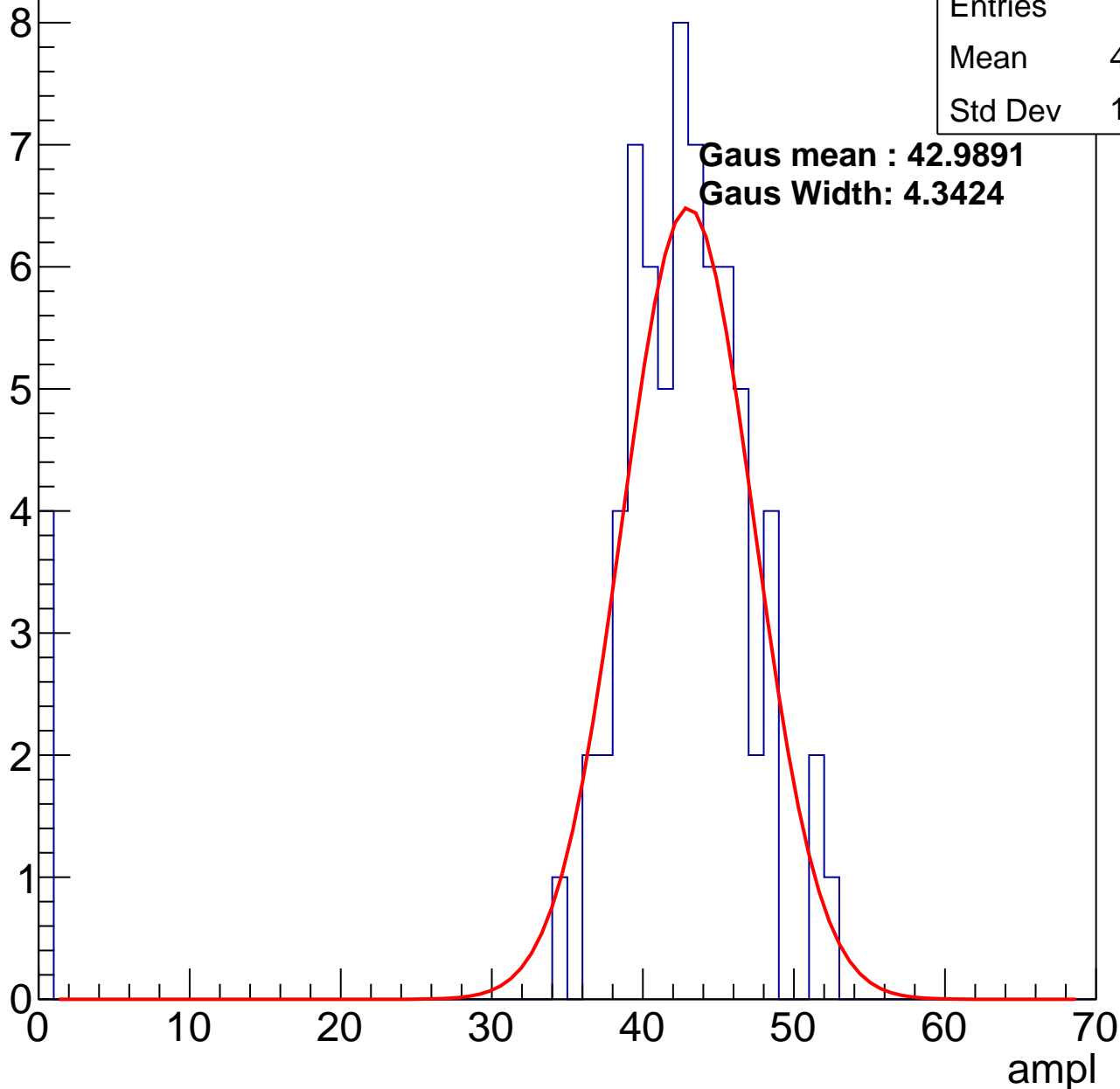
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	72
Mean	40.15
Std Dev	10.39

**Gaus mean : 42.9891**

**Gaus Width: 4.3424**

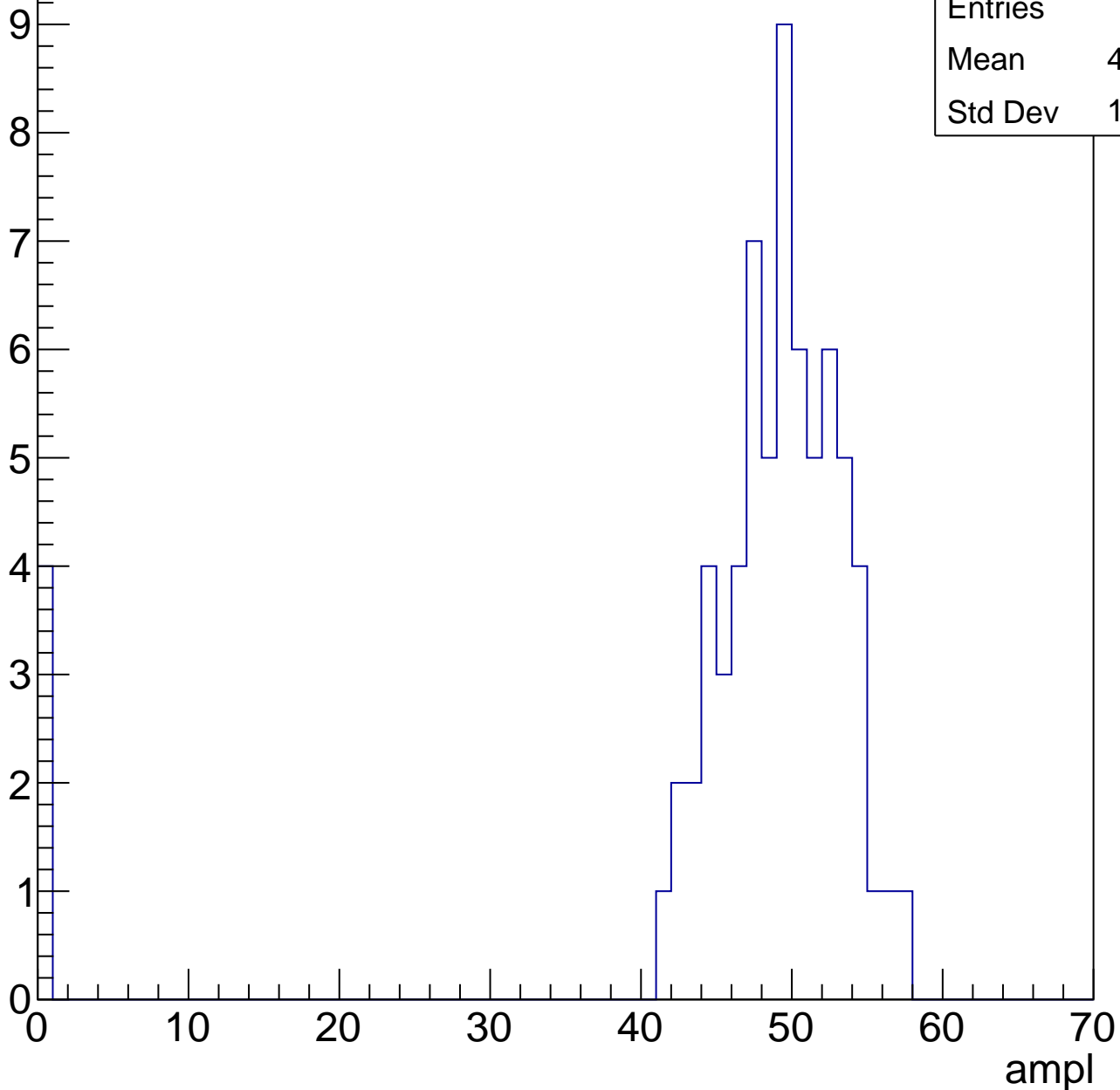


# B1L103S, U26-ch93, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	70
Mean	46.17
Std Dev	11.89

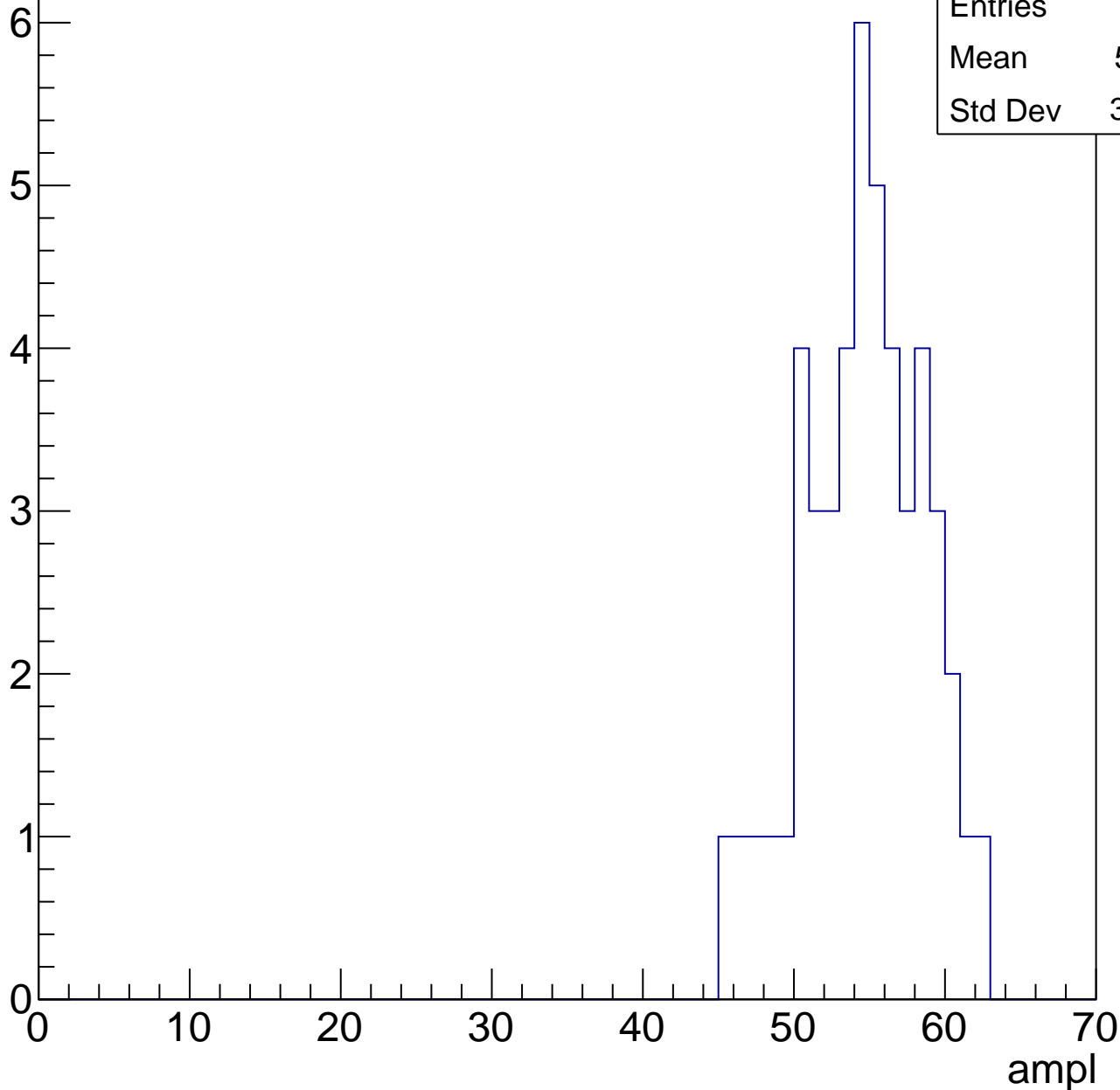


# B1L103S, U26-ch93, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	48
Mean	54.21
Std Dev	3.905

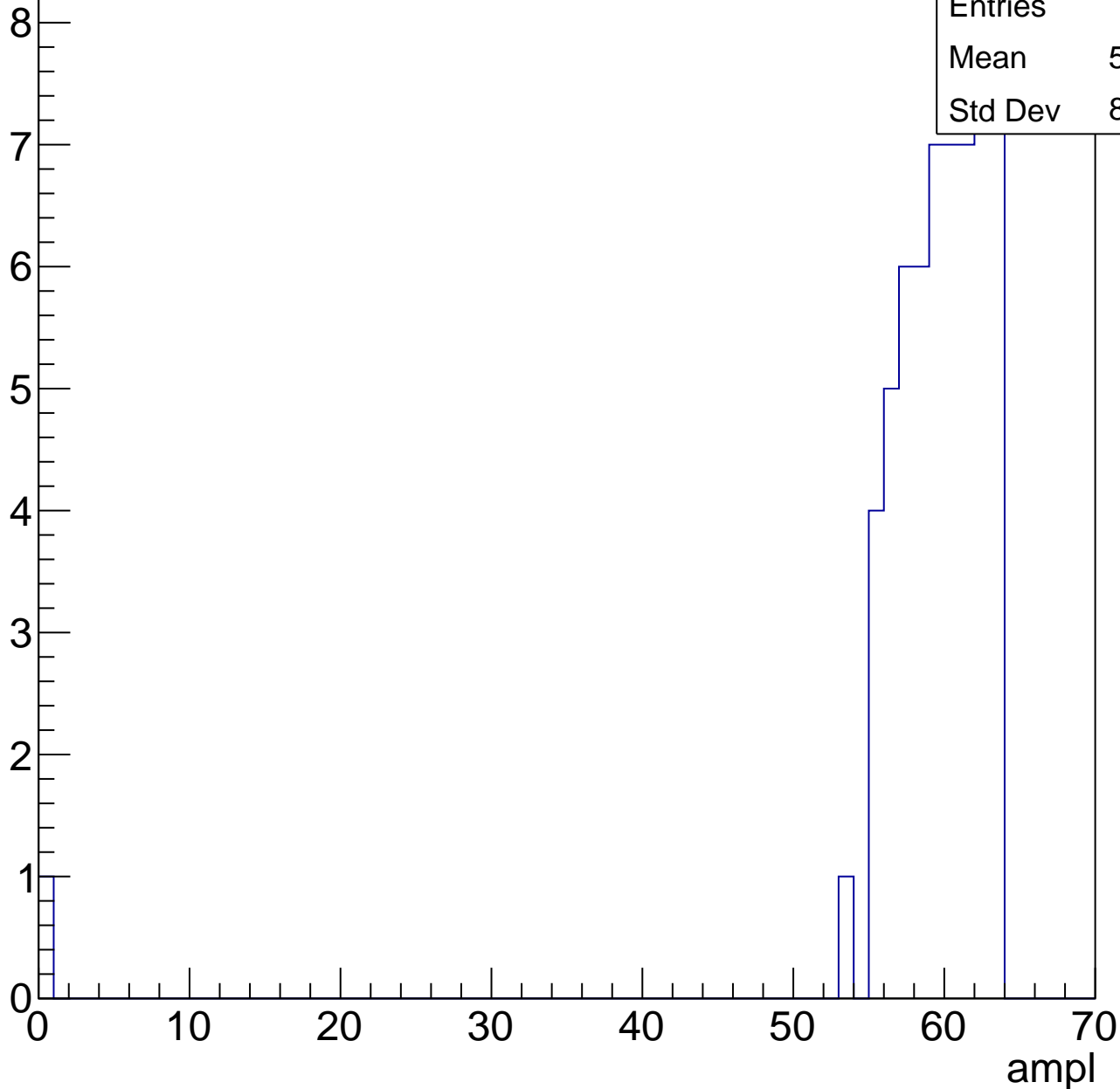


# B1L103S, U26-ch93, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	60
Mean	58.38
Std Dev	8.029



# B1L103S, U26-ch93, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

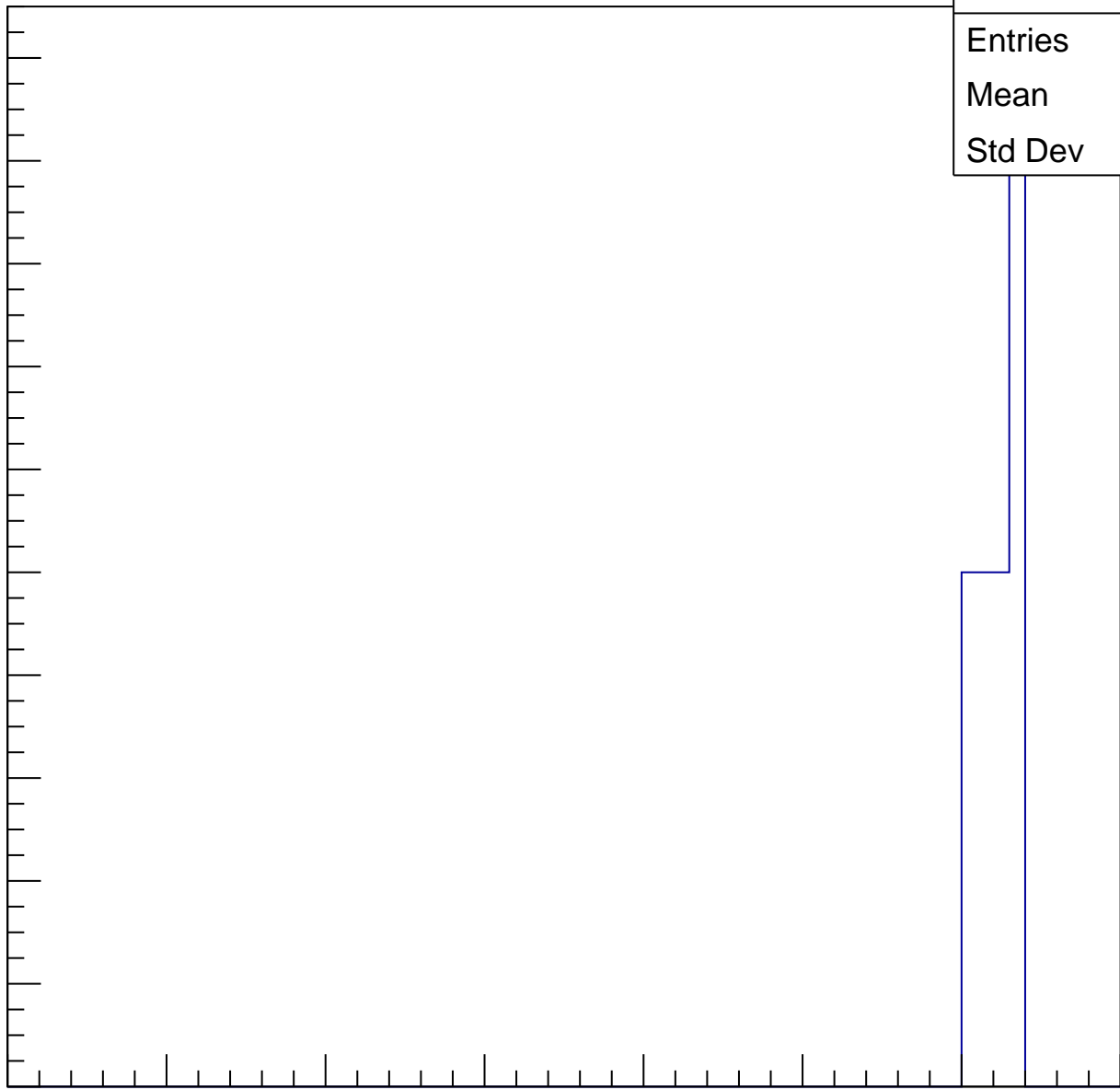
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	5
Mean	61.8
Std Dev	1.166

ampl

0 10 20 30 40 50 60 70





# B1L103S, U26-ch93, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	20
Mean	3.05
Std Dev	13.29

Entry



# B1L103S, U26-ch94, adc0

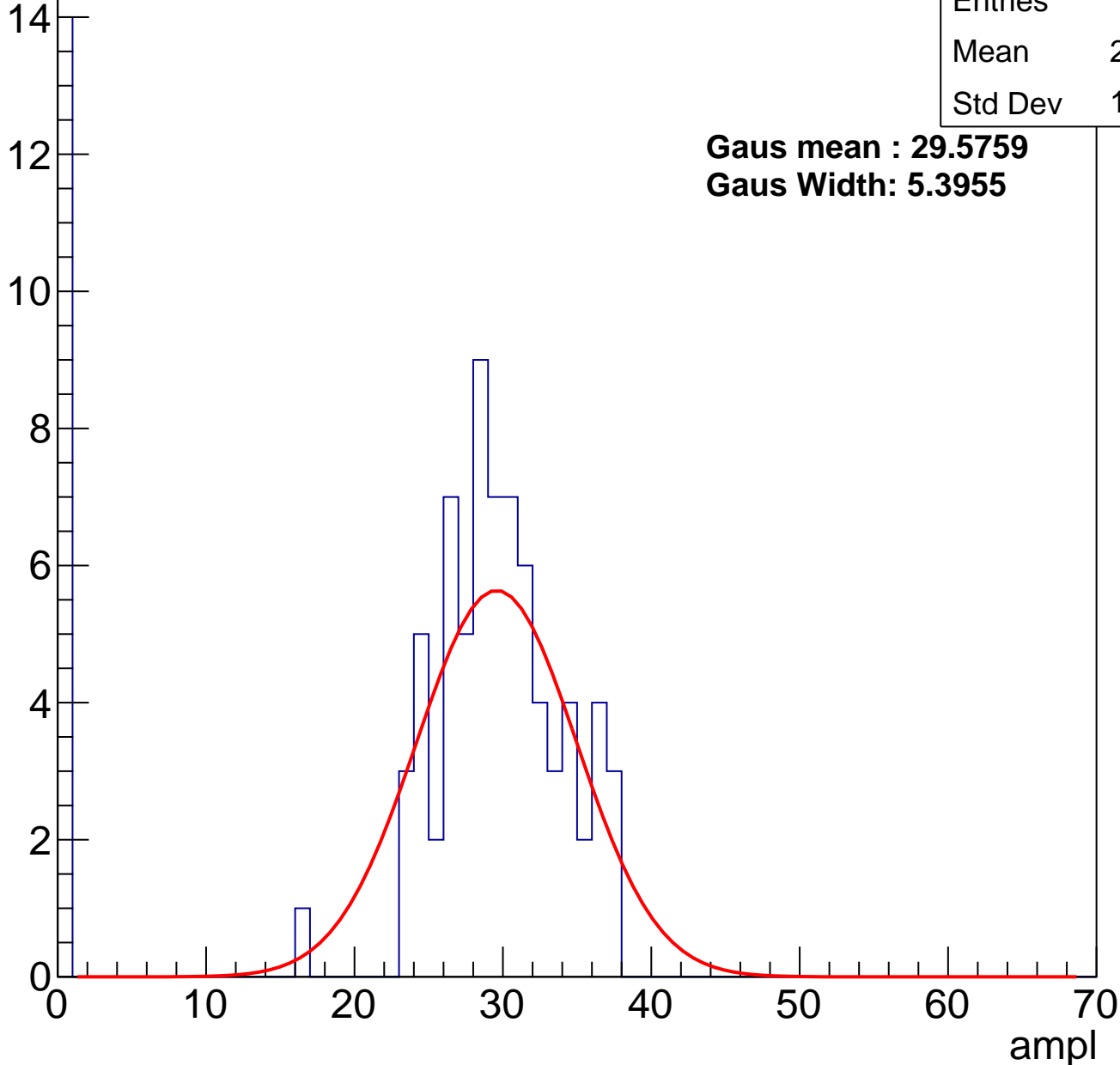
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	86
Mean	24.55
Std Dev	11.45

**Gaus mean : 29.5759**

**Gaus Width: 5.3955**

Entry



# B1L103S, U26-ch94, adc1

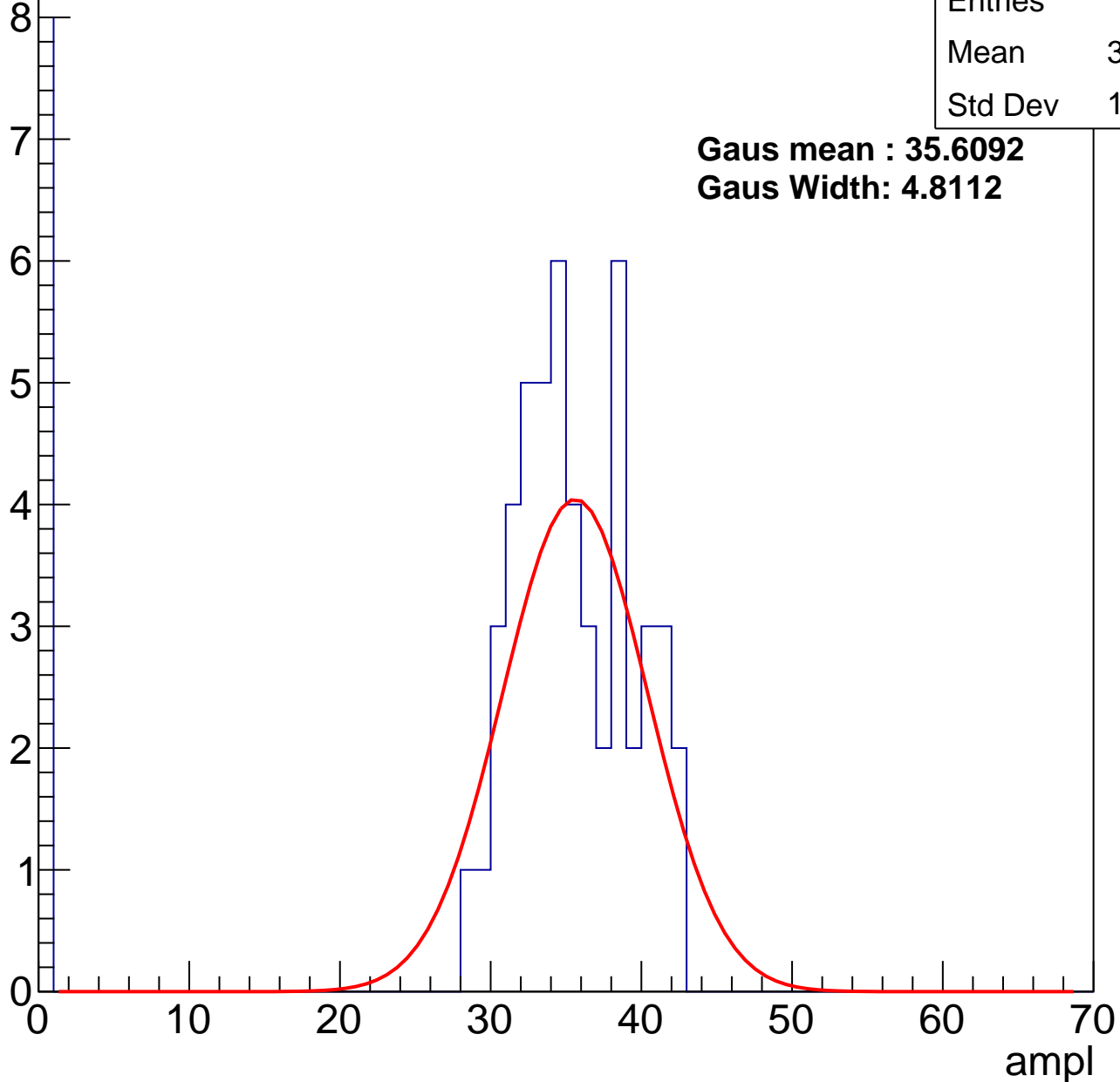
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	58
Mean	30.26
Std Dev	12.57

**Gaus mean : 35.6092**

**Gaus Width: 4.8112**



# B1L103S, U26-ch94, adc2

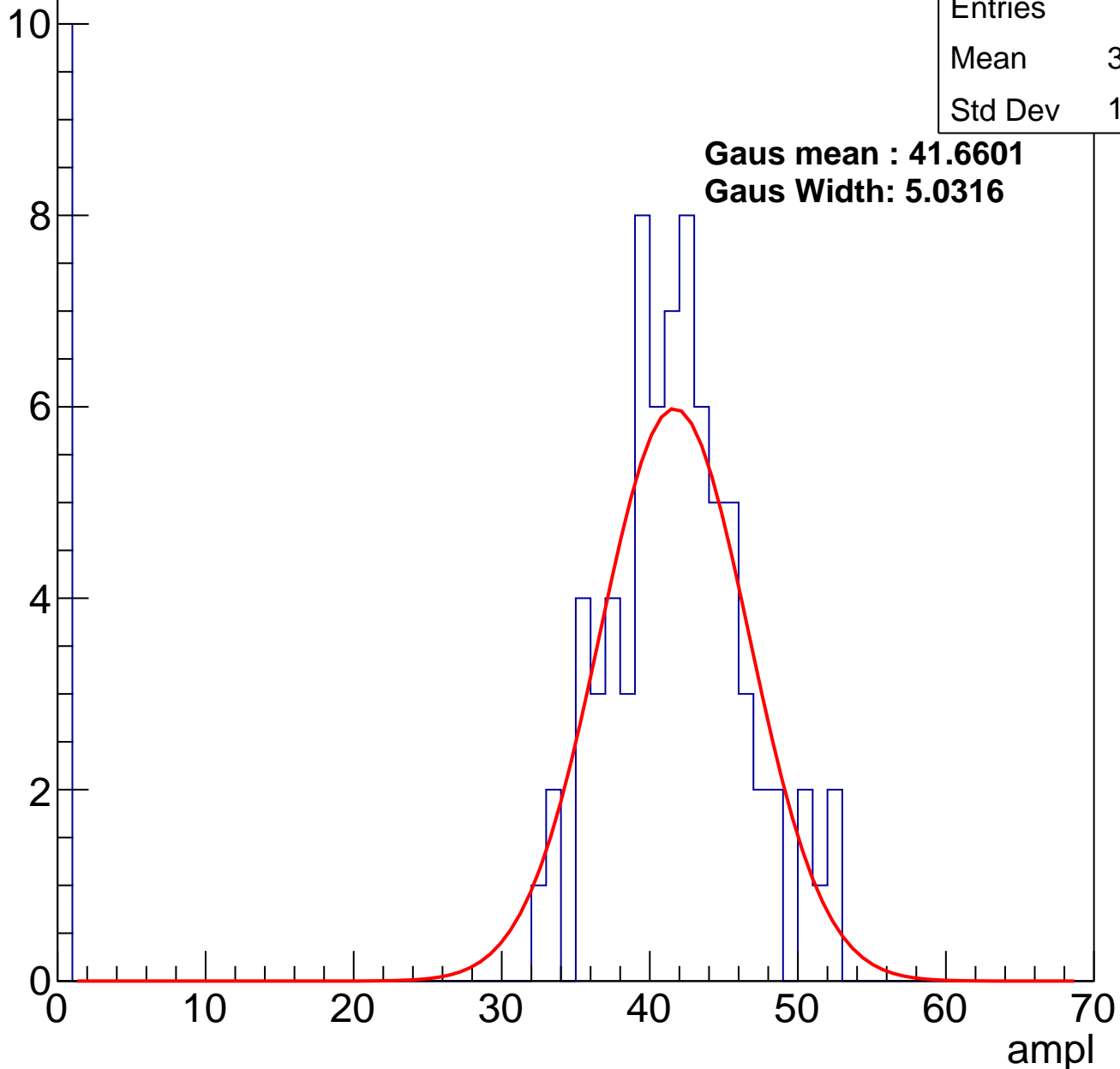
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	84
Mean	36.54
Std Dev	14.06

**Gaus mean : 41.6601**

**Gaus Width: 5.0316**

Entry

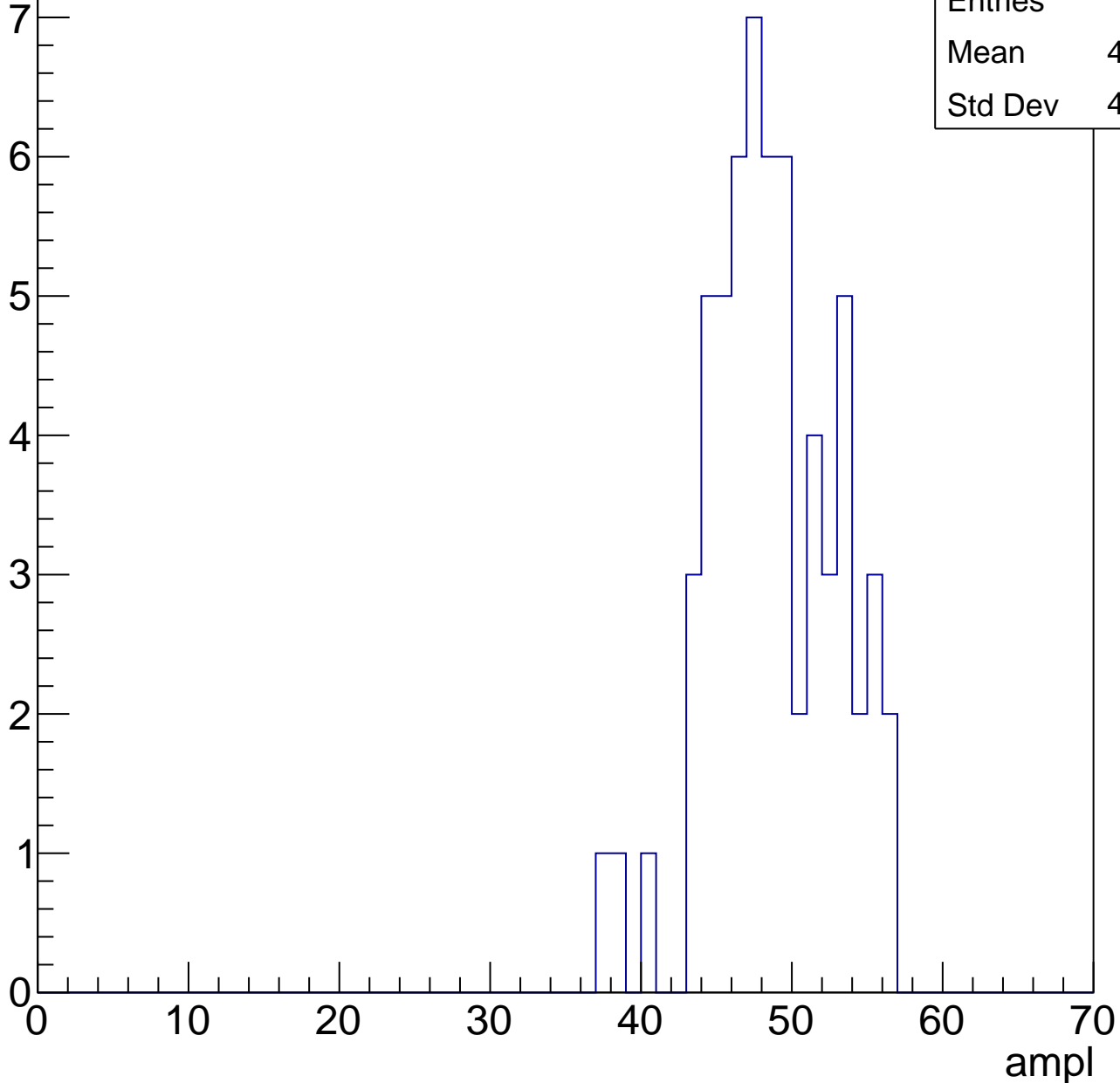


# B1L103S, U26-ch94, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	62
Mean	48.16
Std Dev	4.182

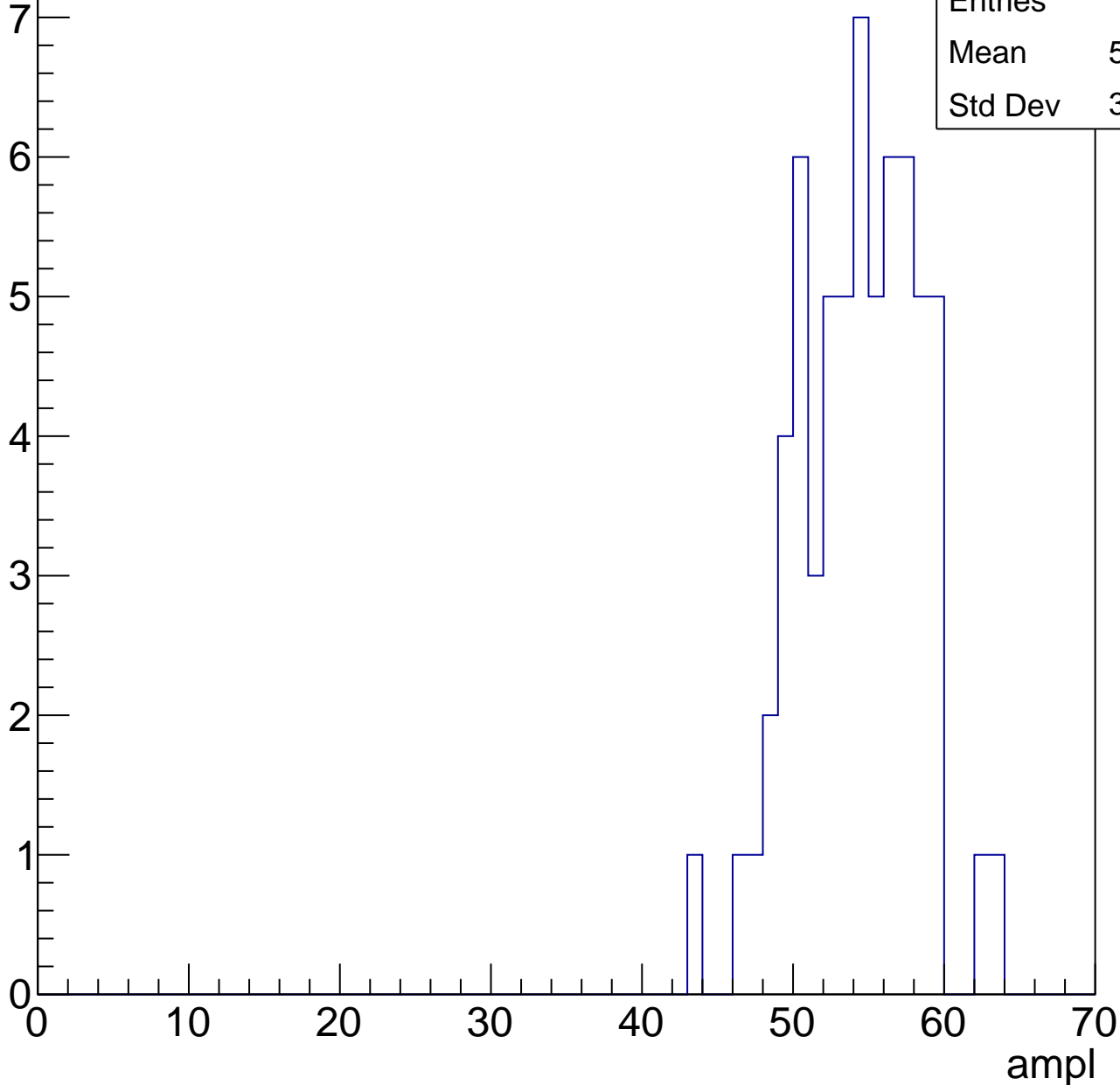


# B1L103S, U26-ch94, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	64
Mean	53.86
Std Dev	3.925

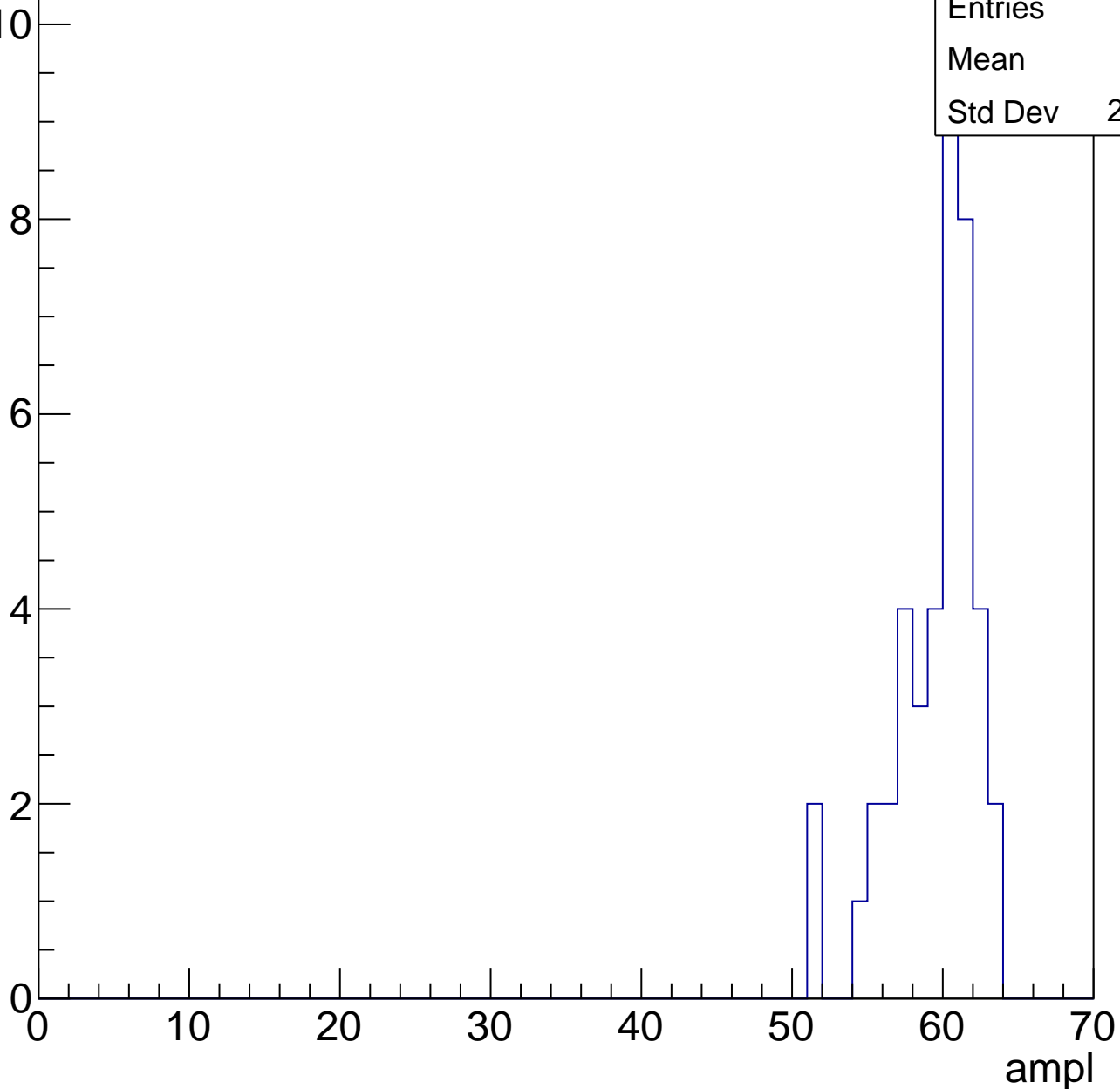


# B1L103S, U26-ch94, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	42
Mean	59
Std Dev	2.812

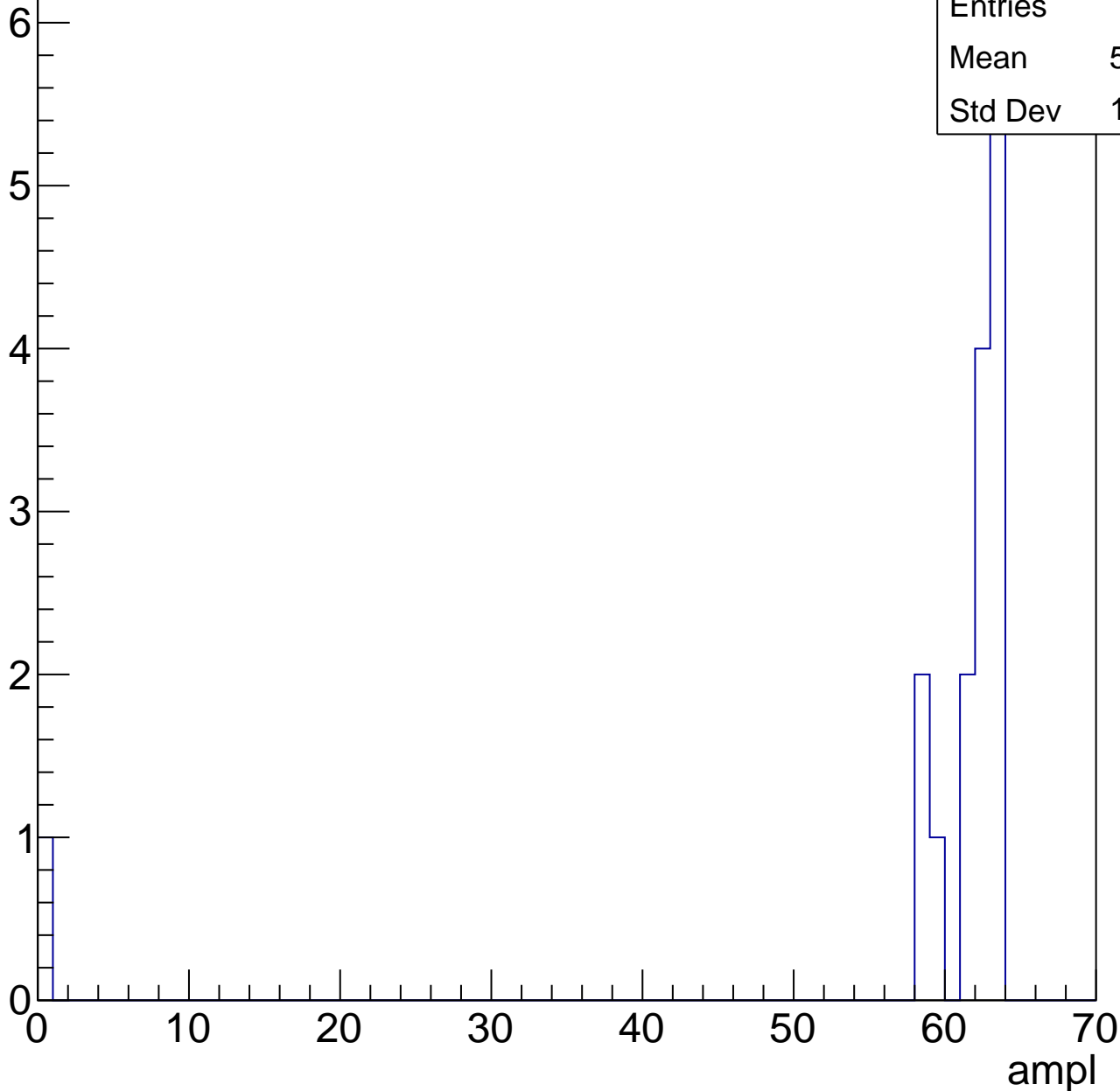


# B1L103S, U26-ch94, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	16
Mean	57.69
Std Dev	14.99



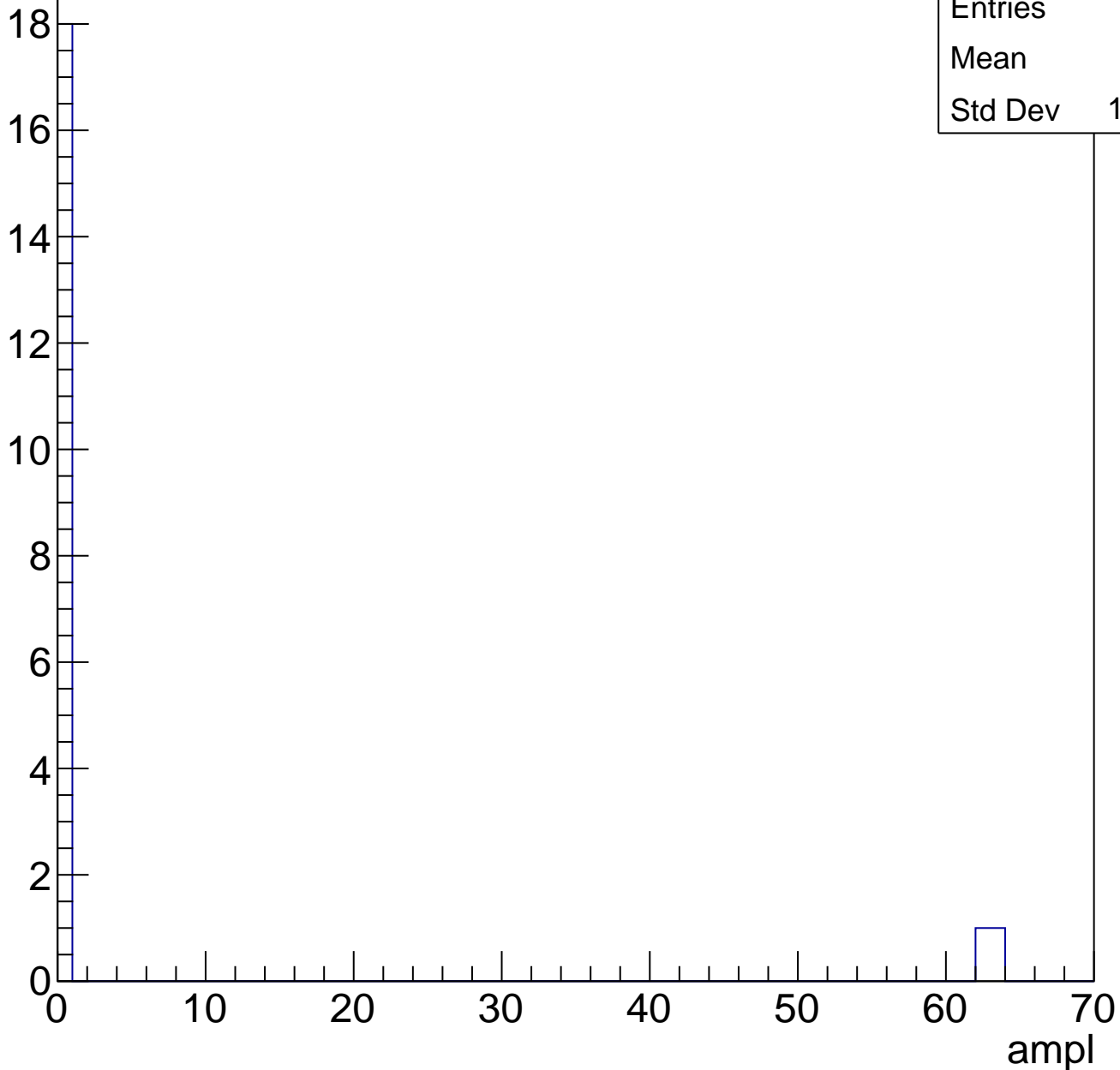


# B1L103S, U26-ch94, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	20
Mean	6.25
Std Dev	18.75

Entry



# B1L103S, U26-ch95, adc0

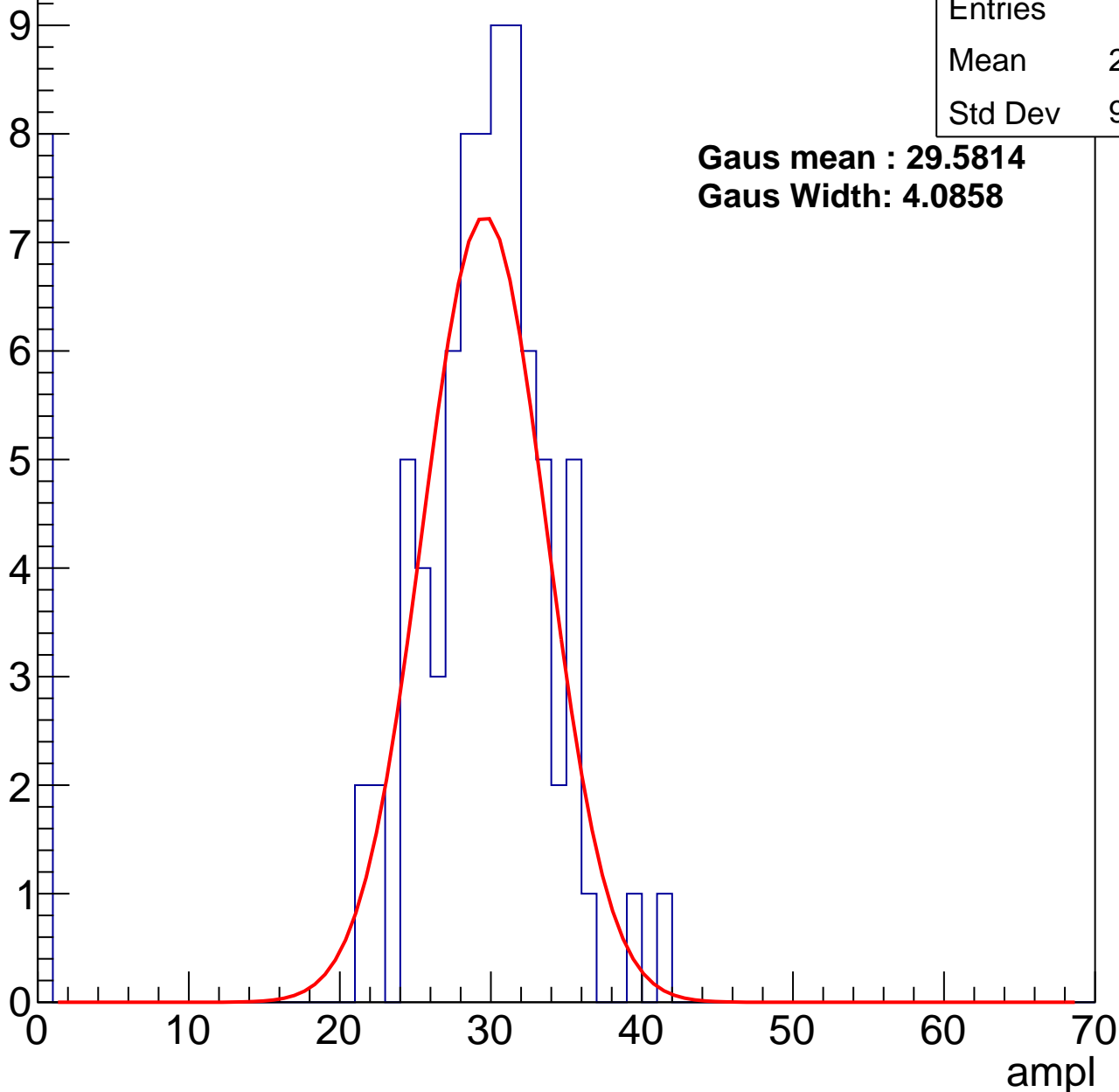
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	85
Mean	26.67
Std Dev	9.357

**Gaus mean : 29.5814**

**Gaus Width: 4.0858**



# B1L103S, U26-ch95, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	76
Mean	34.26
Std Dev	9.674

**Gaus mean : 37.5269**

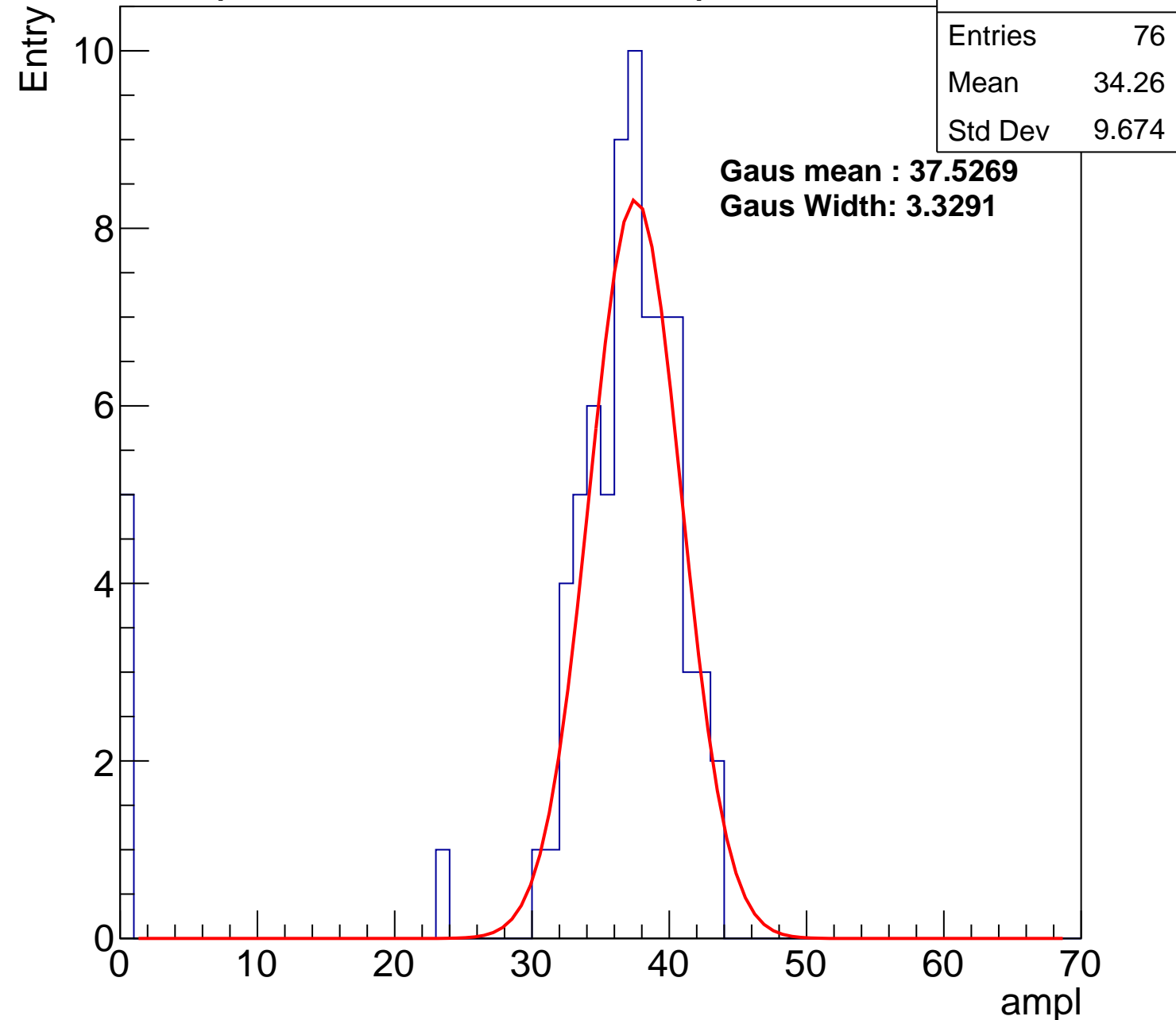
**Gaus Width: 3.3291**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U26-ch95, adc2

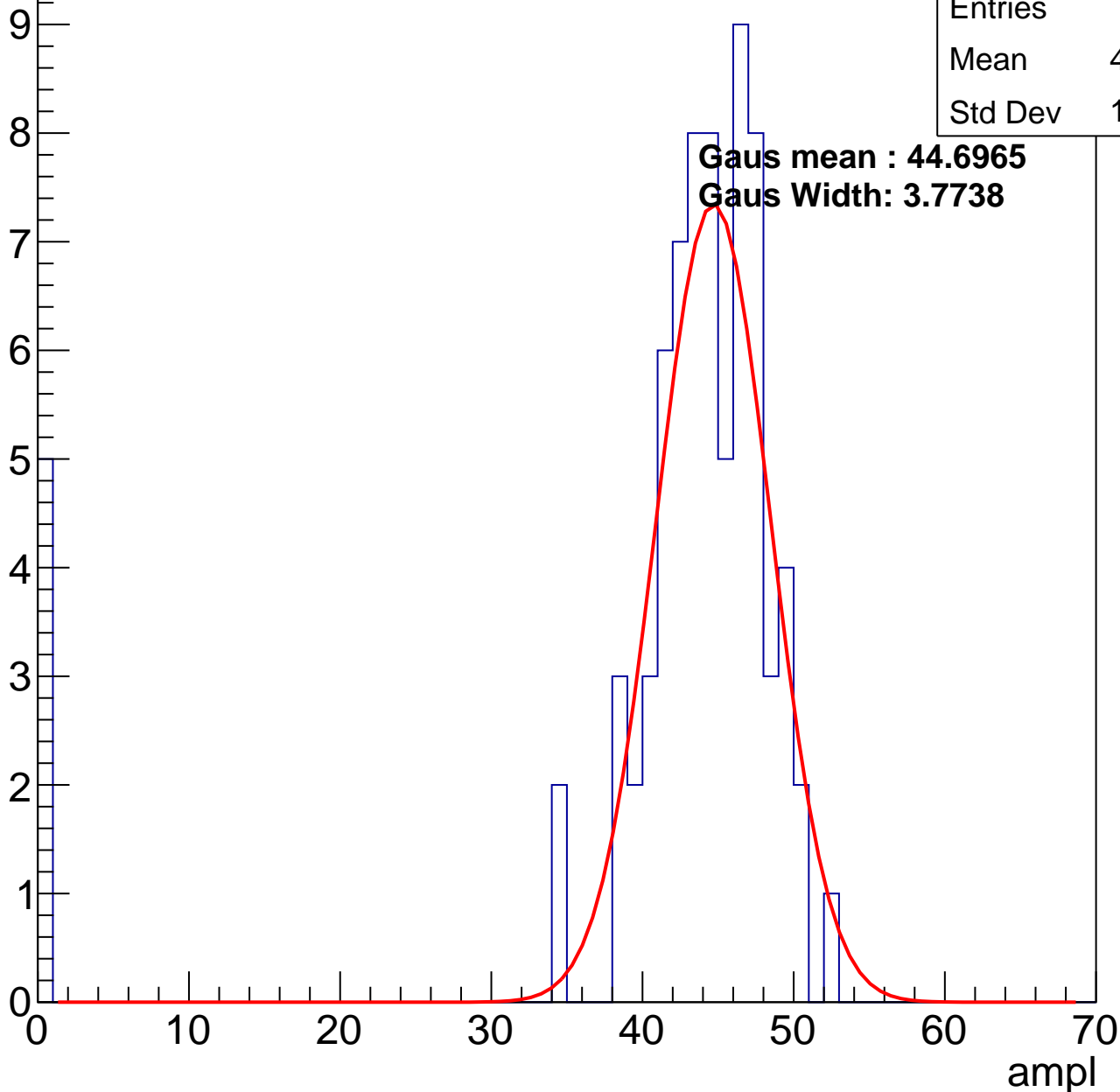
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	76
Mean	41.09
Std Dev	11.43

**Gaus mean : 44.6965**

**Gaus Width: 3.7738**



# B1L103S, U26-ch95, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	62
Mean	50.69
Std Dev	3.563

Entry

10

8

6

4

2

0

0

10

20

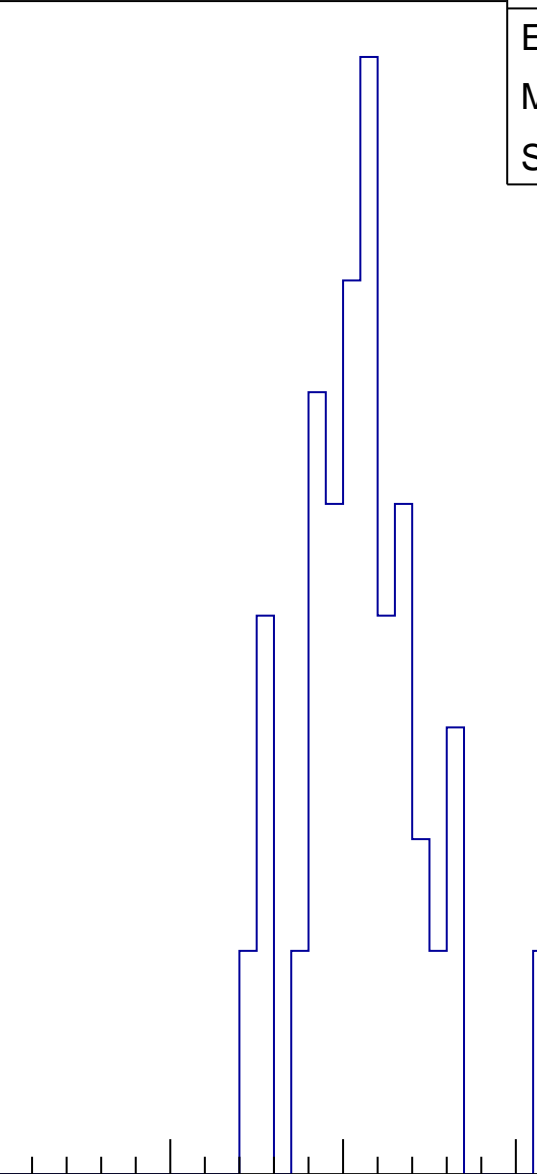
30

40

50

60

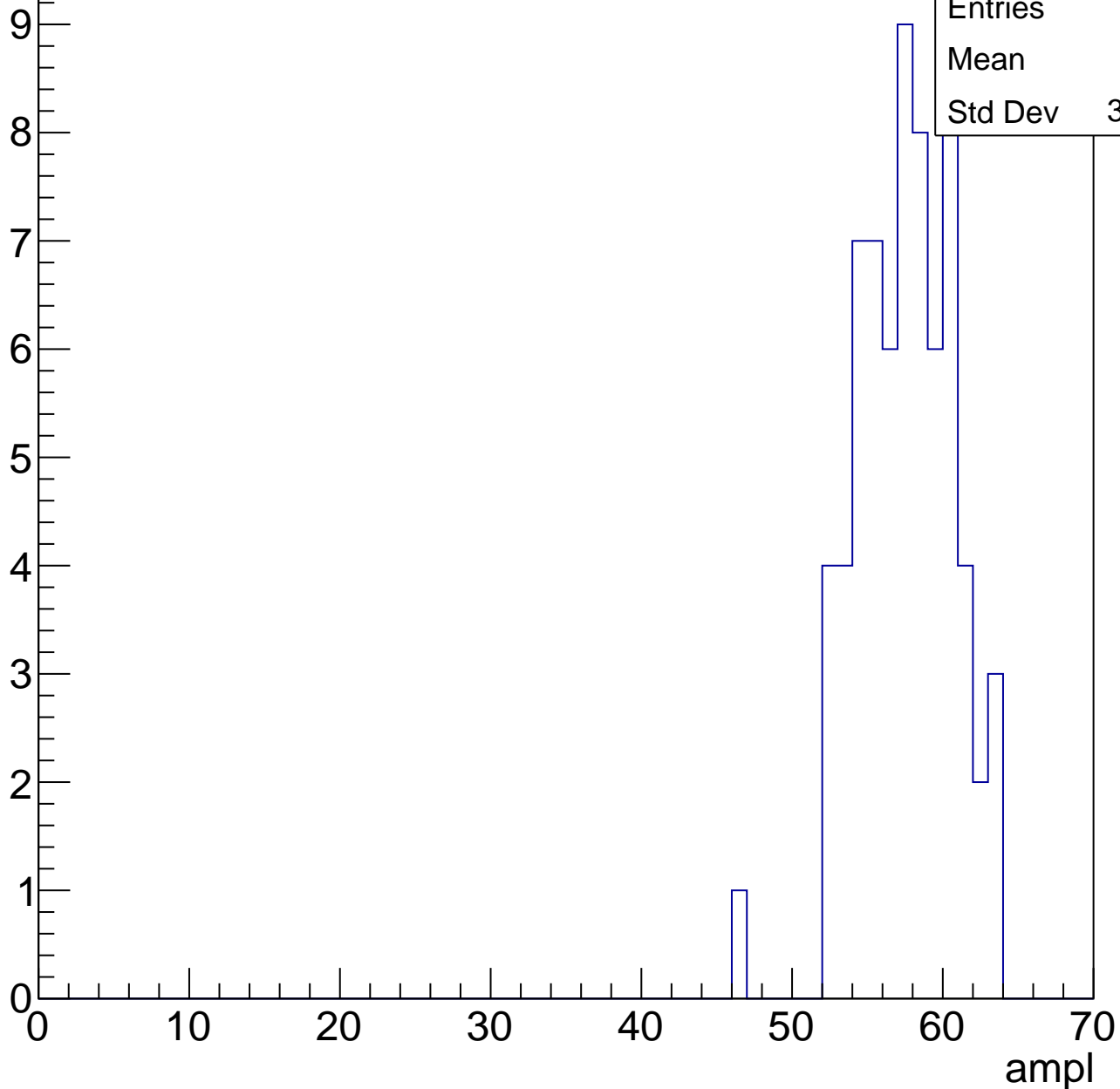
ampl



# B1L103S, U26-ch95, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

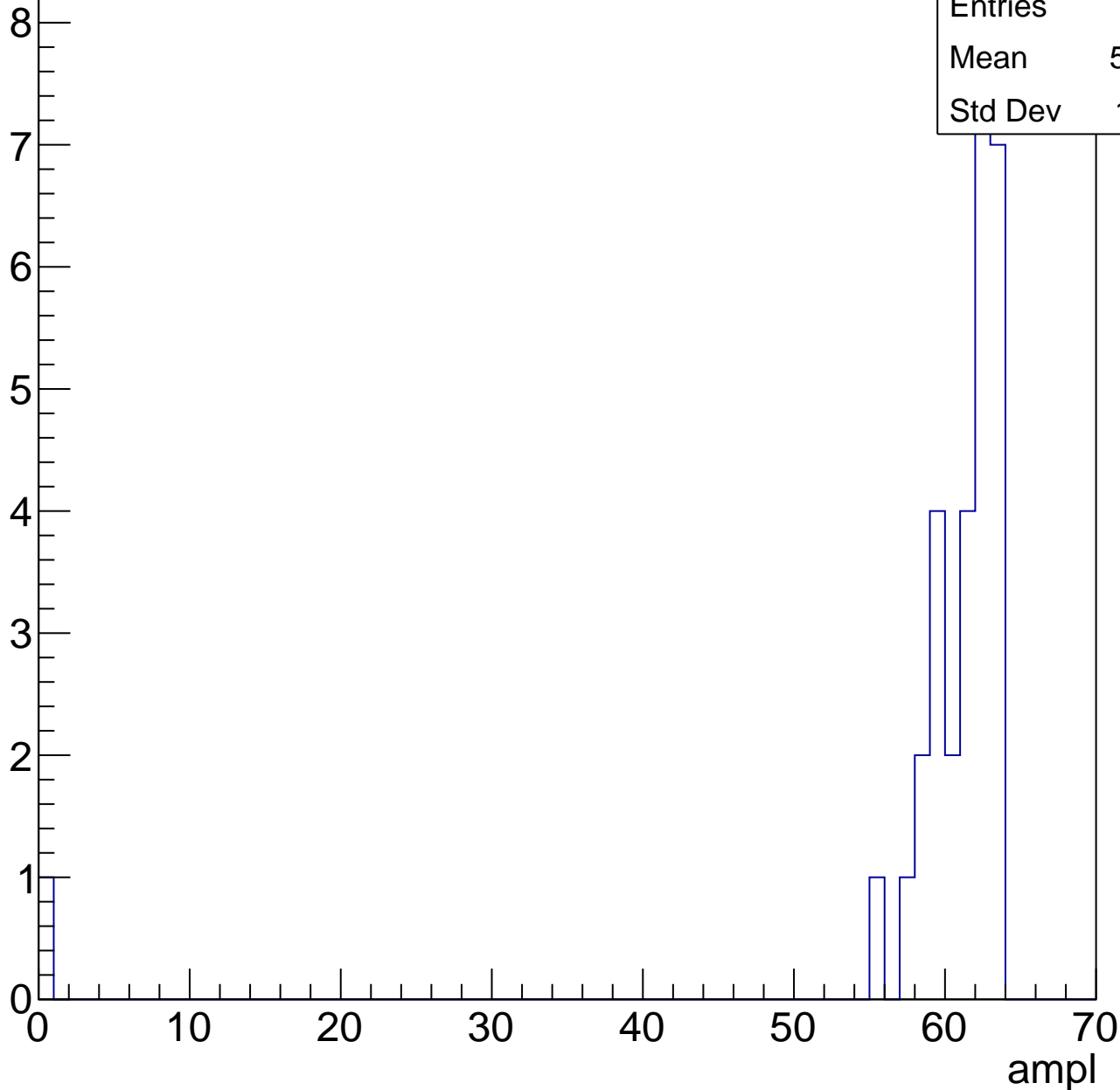


# B1L103S, U26-ch95, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	30
Mean	58.83
Std Dev	11.11



# B1L103S, U26-ch95, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



Entries	0
Mean	0
Std Dev	0



# B1L103S, U26-ch95, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



# B1L103S, U26-ch96, adc0

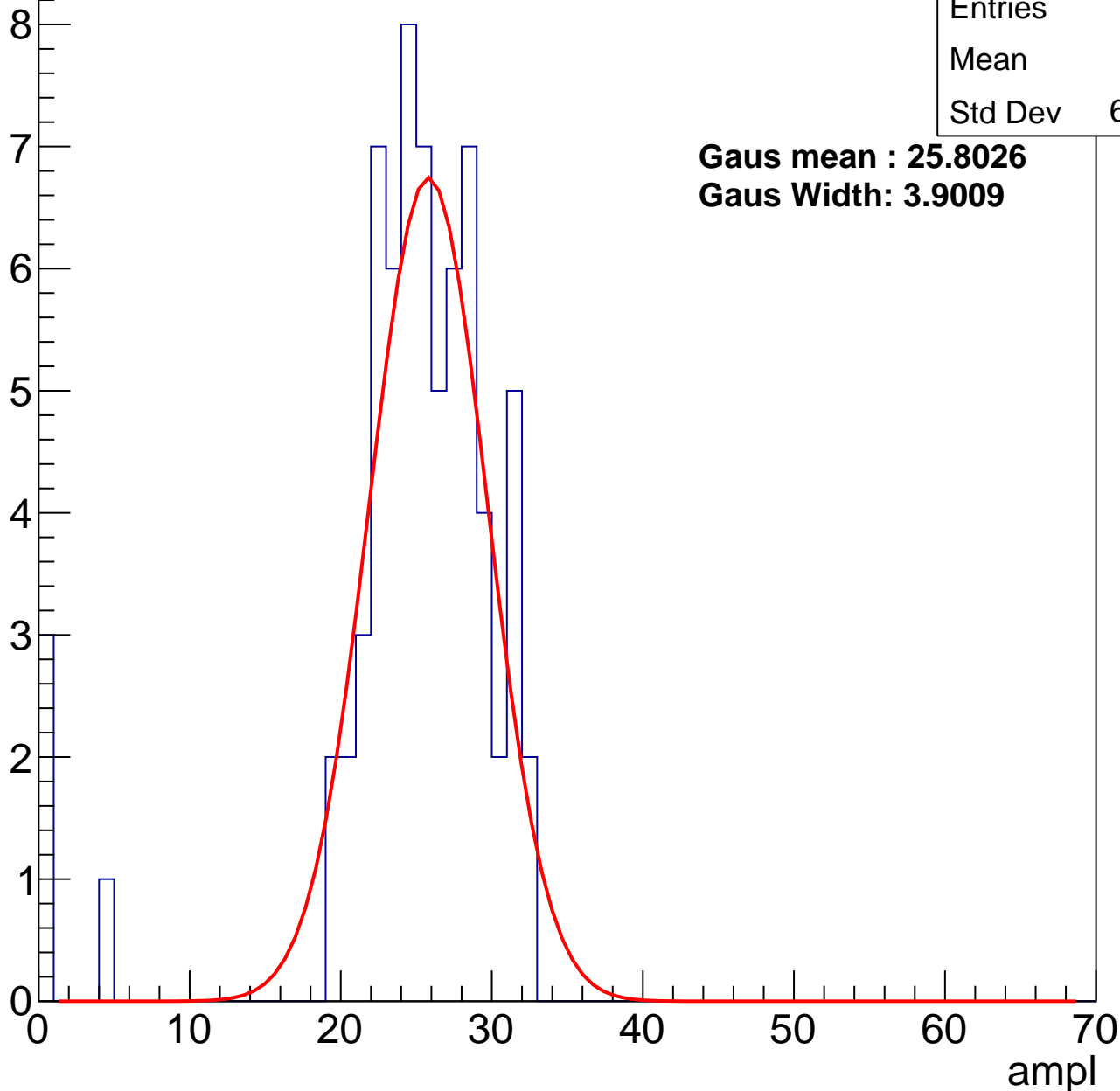
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	70
Mean	24.1
Std Dev	6.556

**Gaus mean : 25.8026**

**Gaus Width: 3.9009**



# B1L103S, U26-ch96, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	69
Mean	32.14
Std Dev	3.337

**Gaus mean : 32.3180**

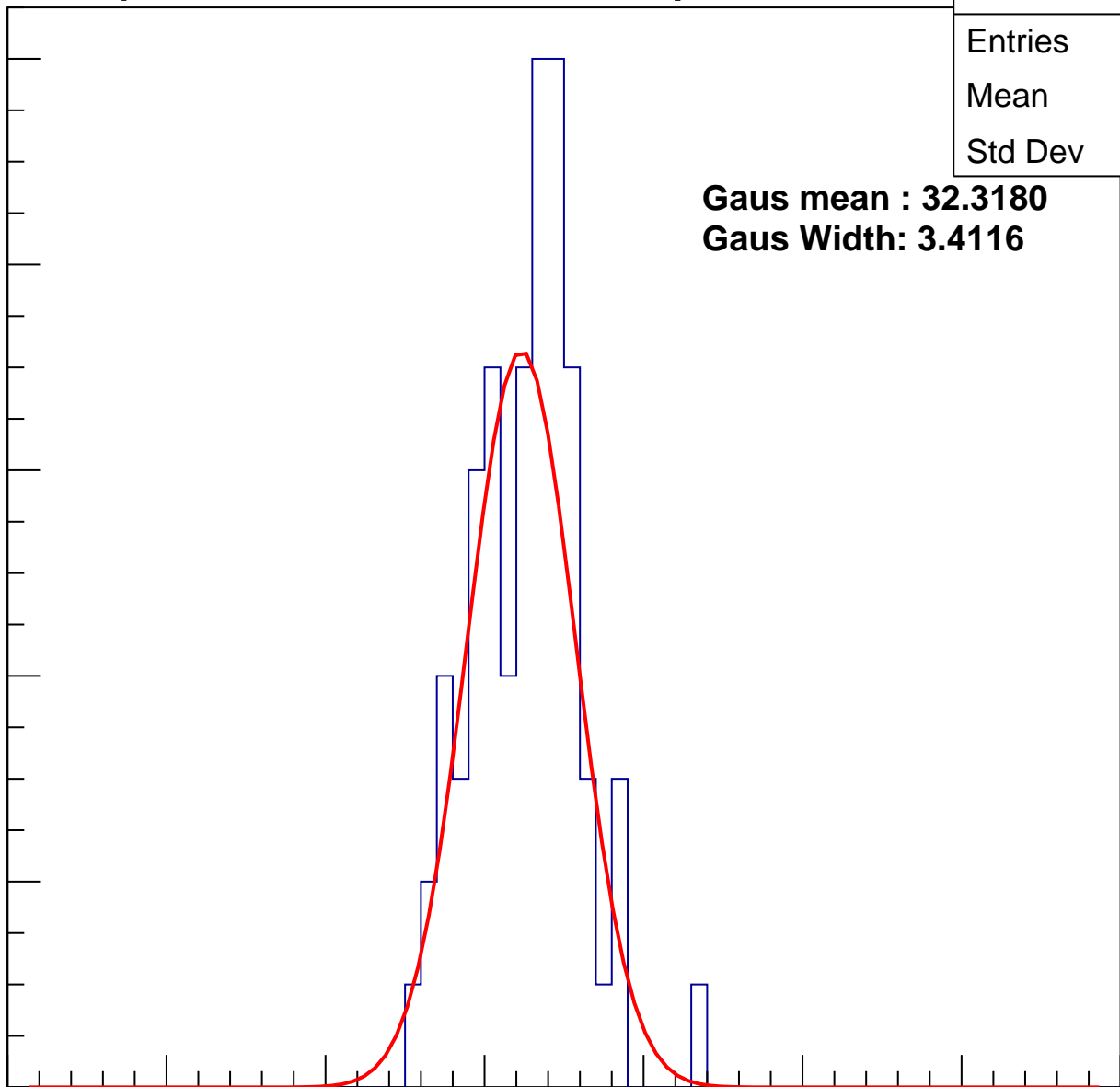
**Gaus Width: 3.4116**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U26-ch96, adc2

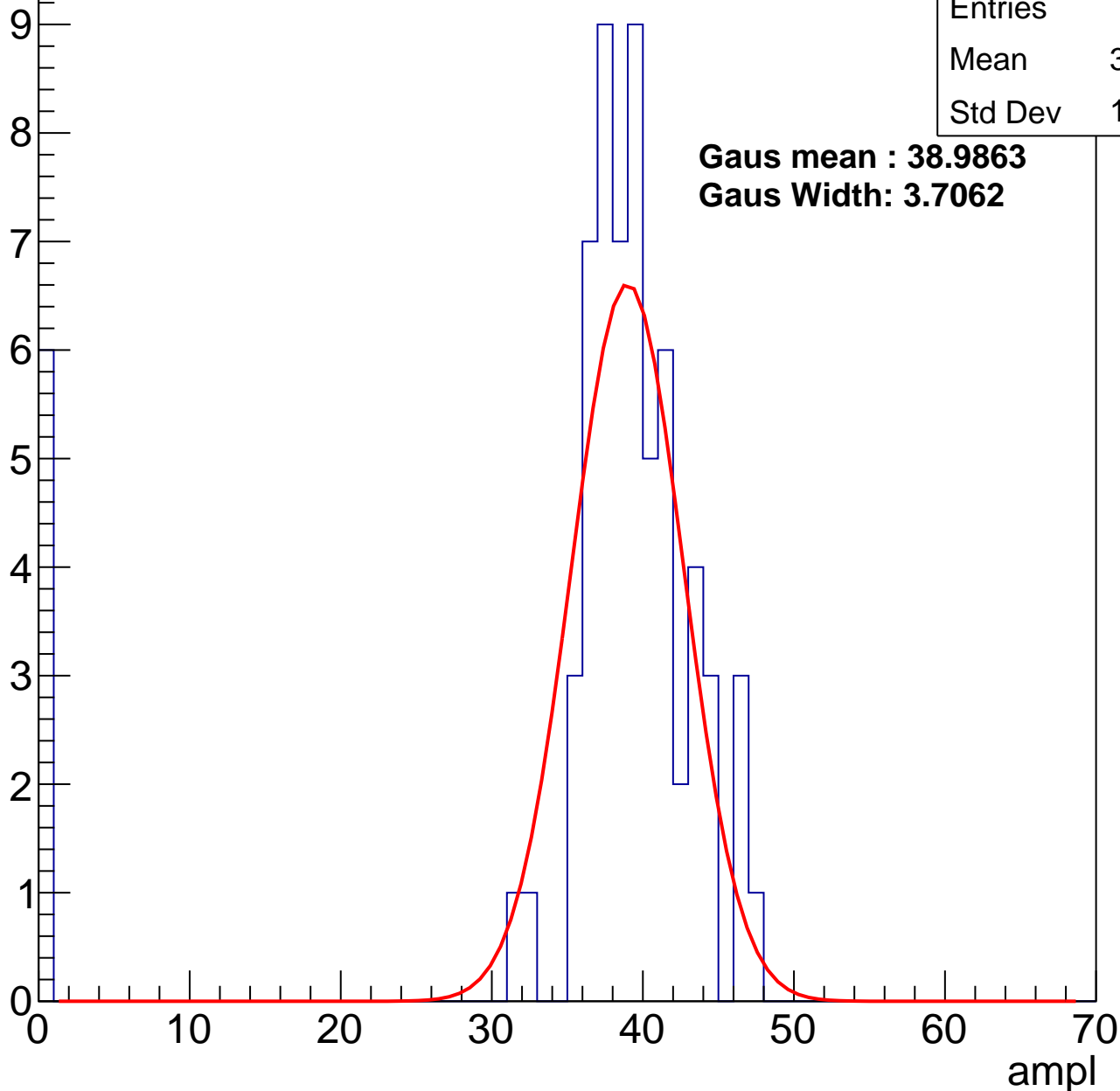
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	67
Mean	35.66
Std Dev	11.62

**Gaus mean : 38.9863**

**Gaus Width: 3.7062**

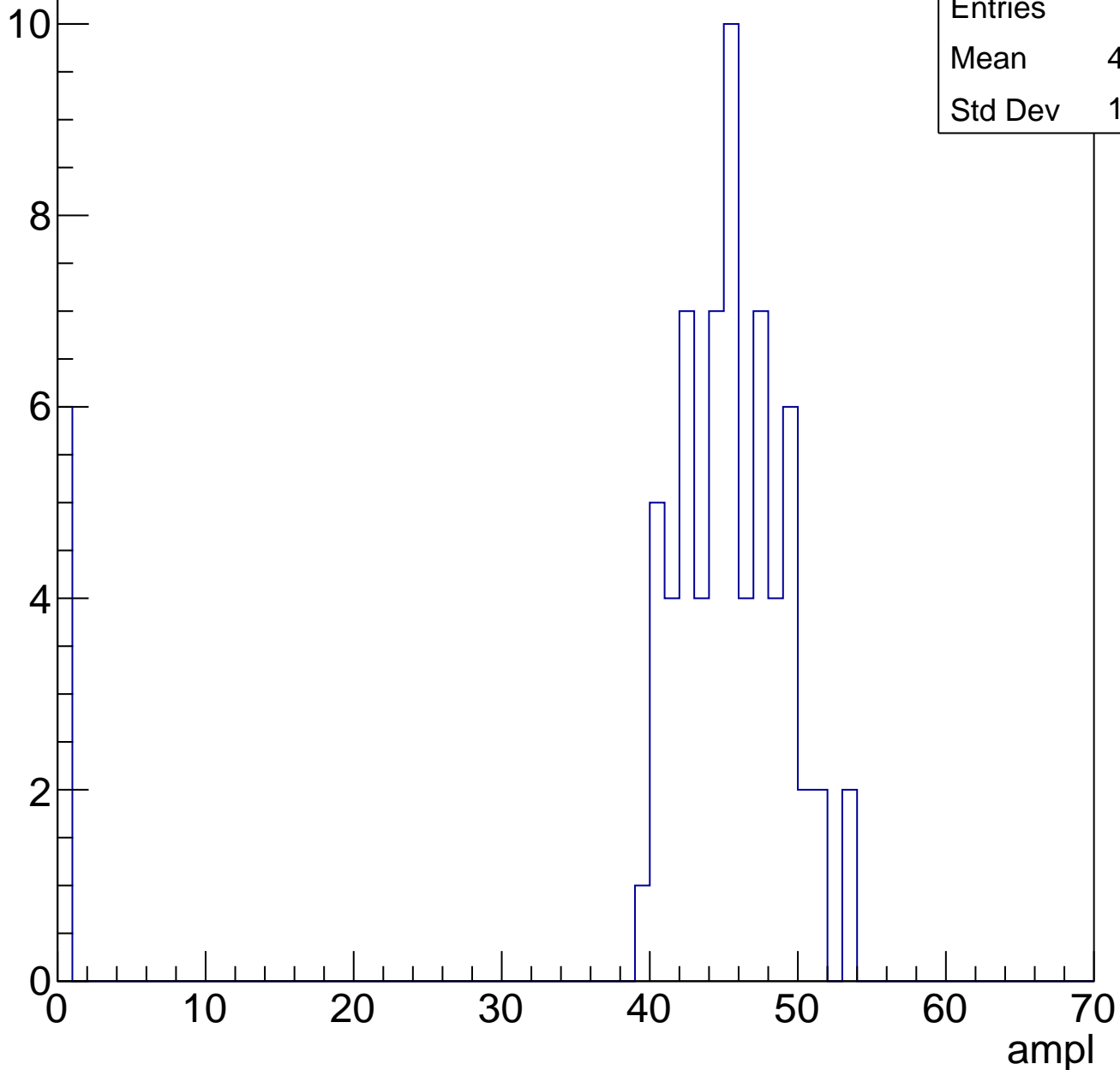


# B1L103S, U26-ch96, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	71
Mean	41.32
Std Dev	12.95

Entry

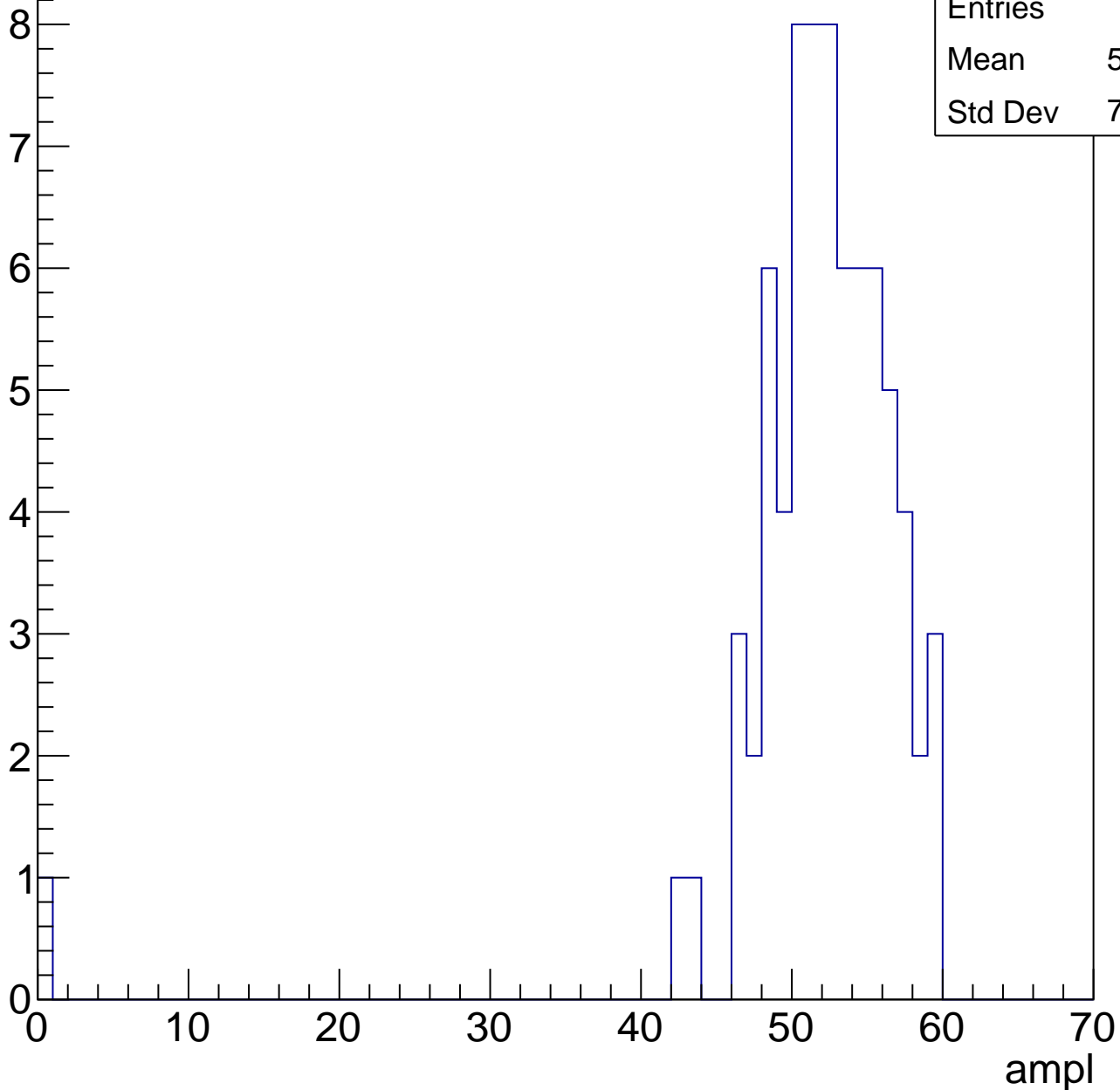


# B1L103S, U26-ch96, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	74
Mean	51.32
Std Dev	7.037

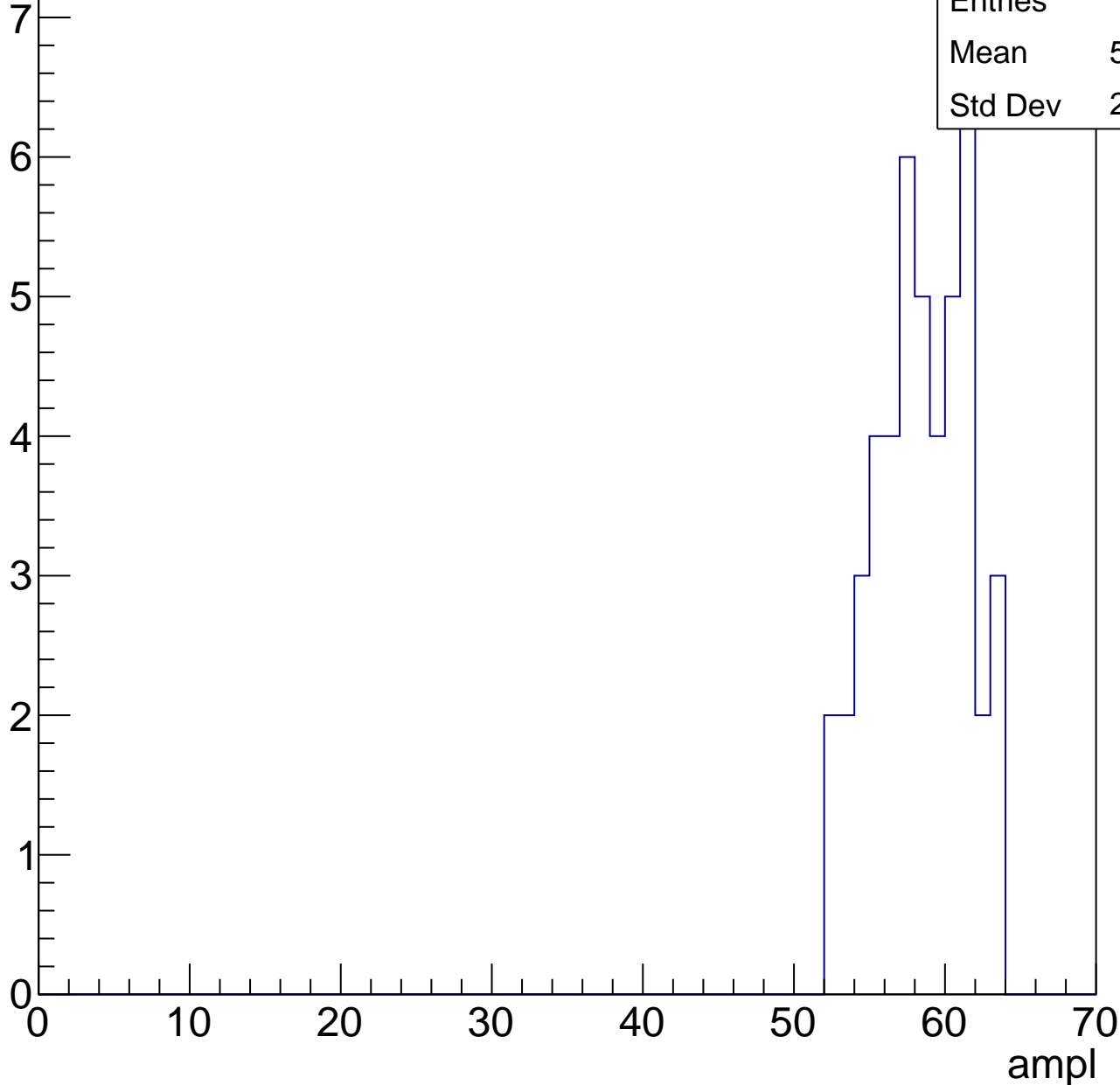


# B1L103S, U26-ch96, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	47
Mean	57.96
Std Dev	2.996

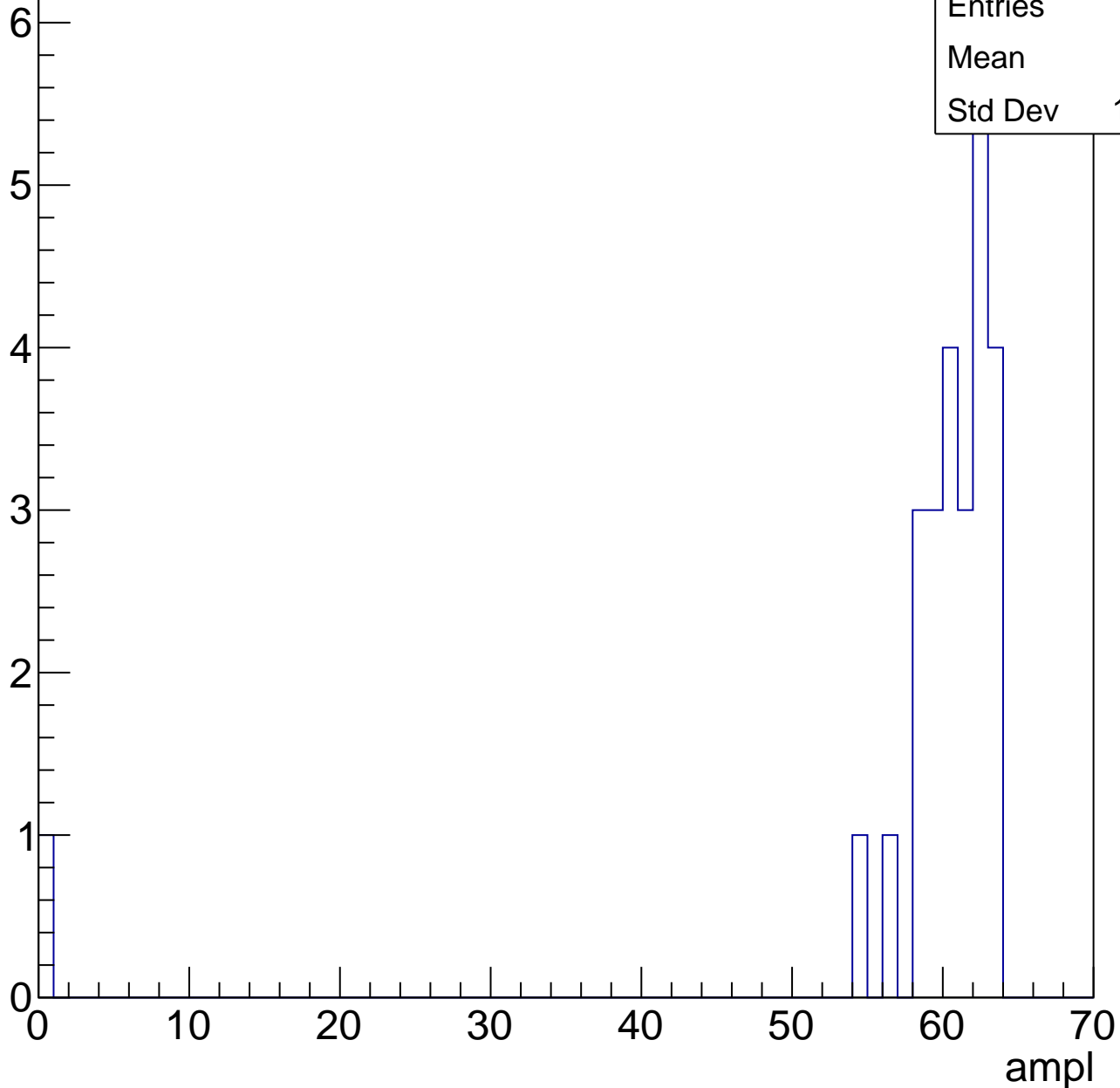


# B1L103S, U26-ch96, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	26
Mean	58
Std Dev	11.81



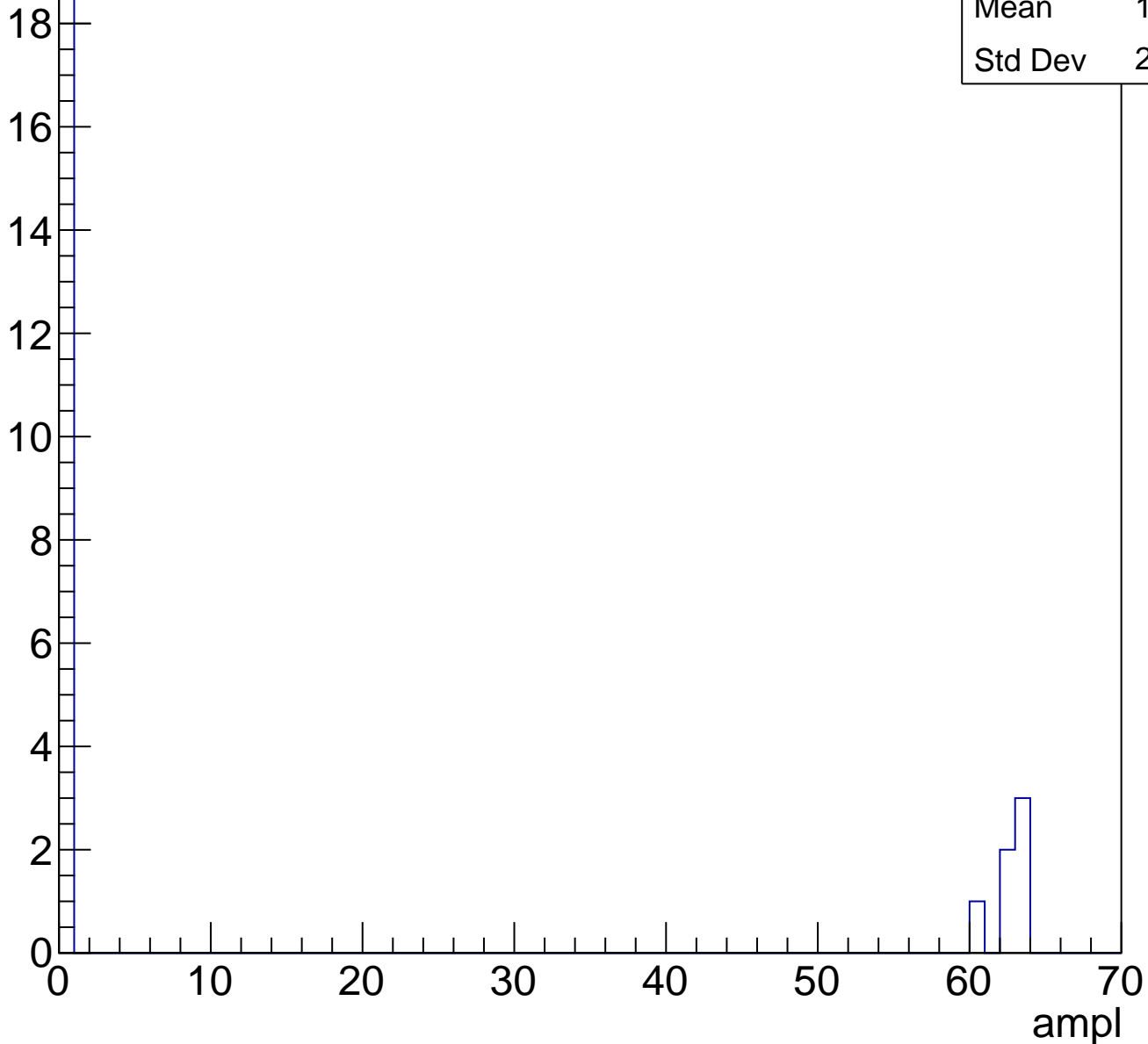


# B1L103S, U26-ch96, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	25
Mean	14.92
Std Dev	26.56

Entry



# B1L103S, U26-ch97, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	77
Mean	23.22
Std Dev	10.88

**Gaus mean : 28.1090**

**Gaus Width: 3.1010**

Entry

12

10

8

6

4

2

0

0

10

20

30

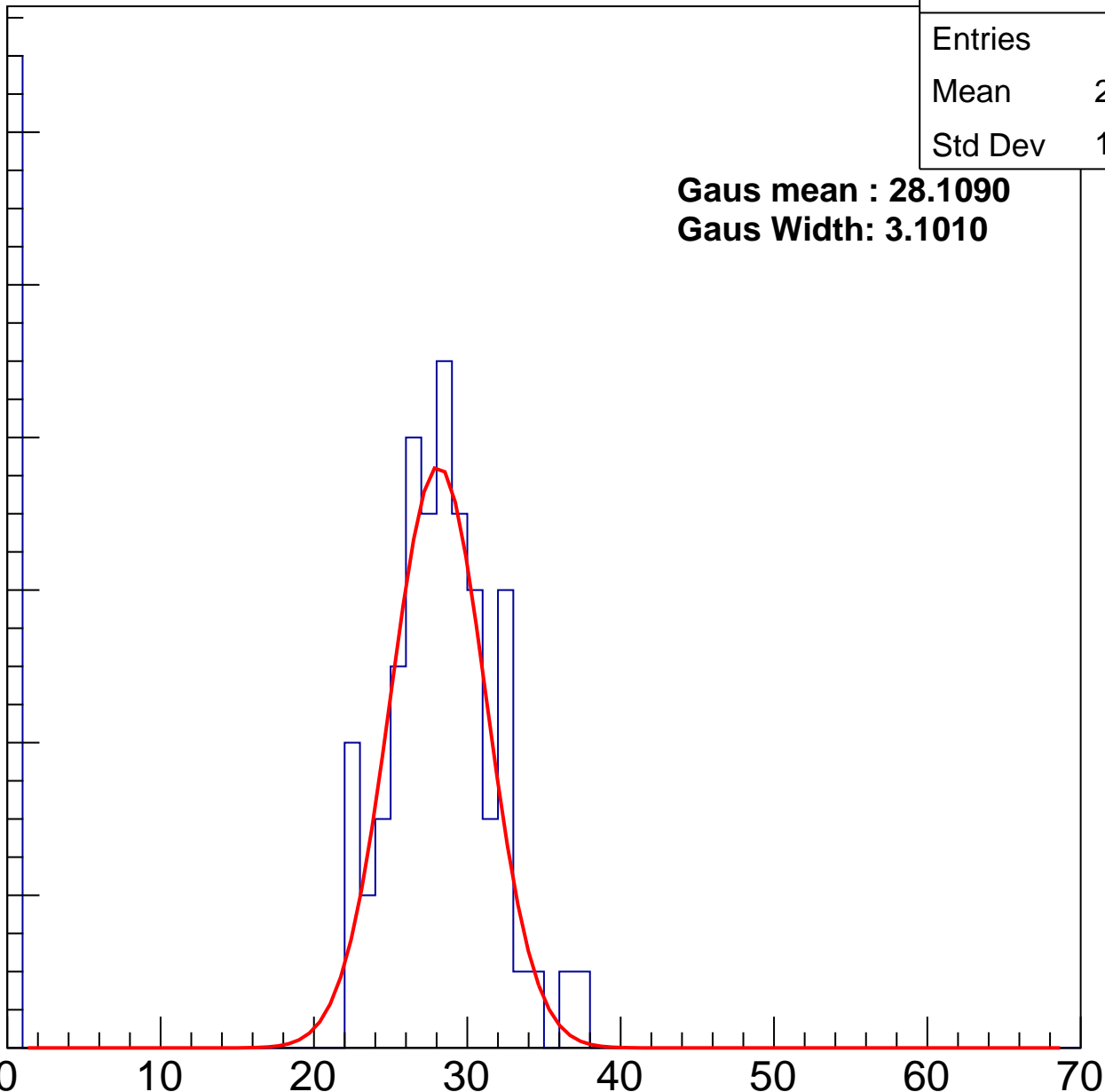
40

50

60

70

ampl



# B1L103S, U26-ch97, adc1

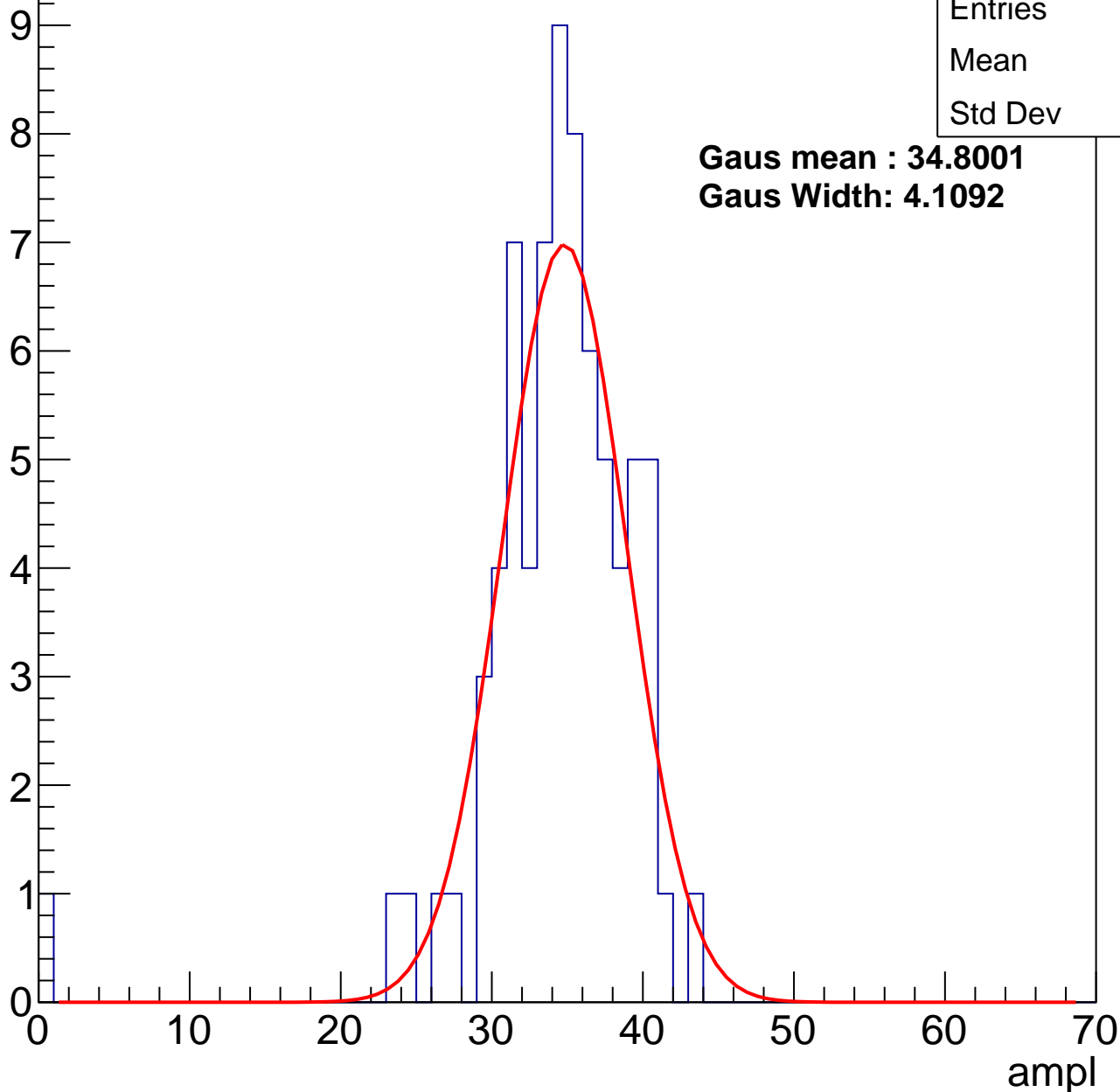
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	74
Mean	33.8
Std Dev	5.56

**Gaus mean : 34.8001**

**Gaus Width: 4.1092**



# B1L103S, U26-ch97, adc2

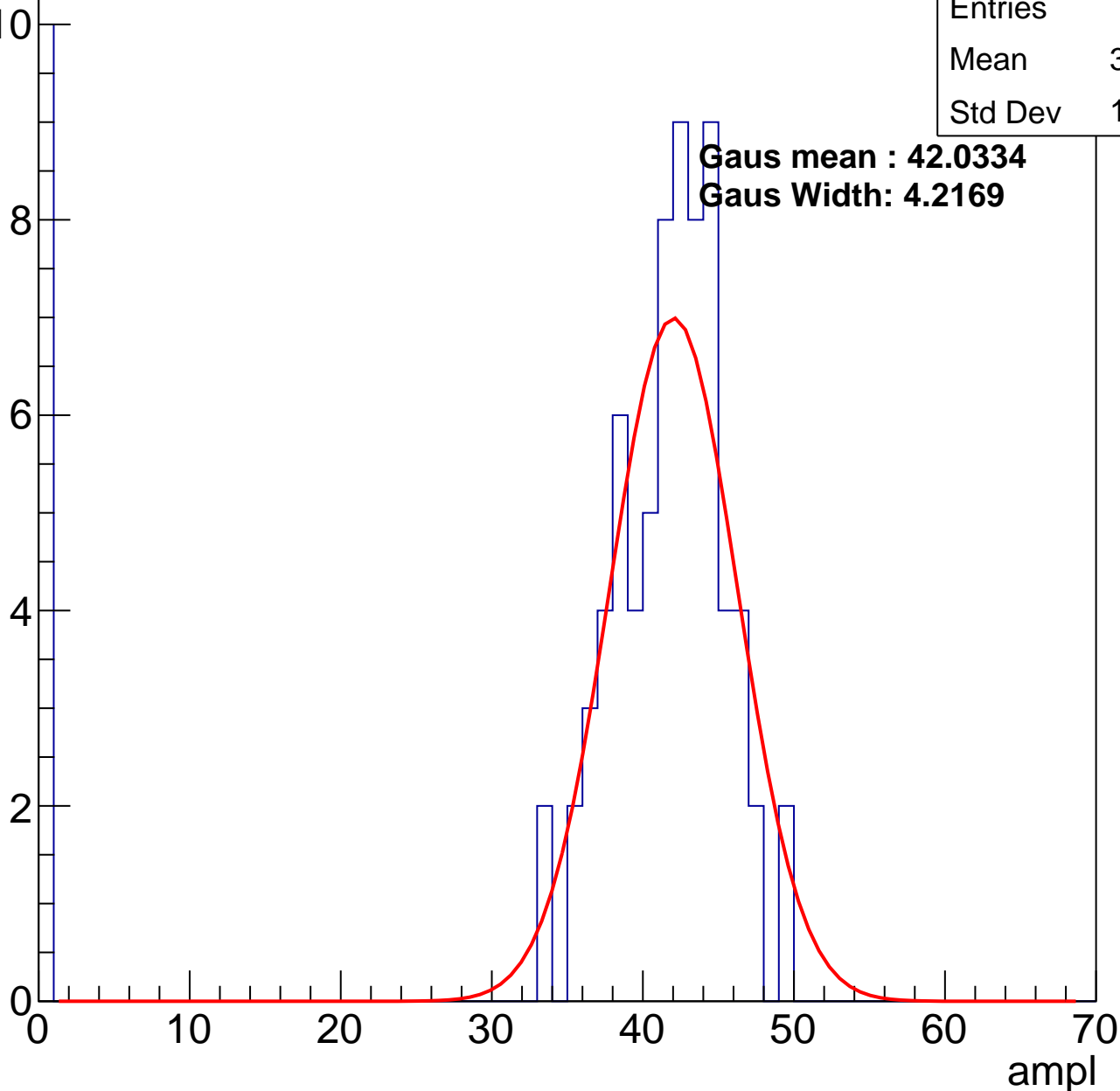
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	82
Mean	36.32
Std Dev	13.93

**Gaus mean : 42.0334**

**Gaus Width: 4.2169**



# B1L103S, U26-ch97, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

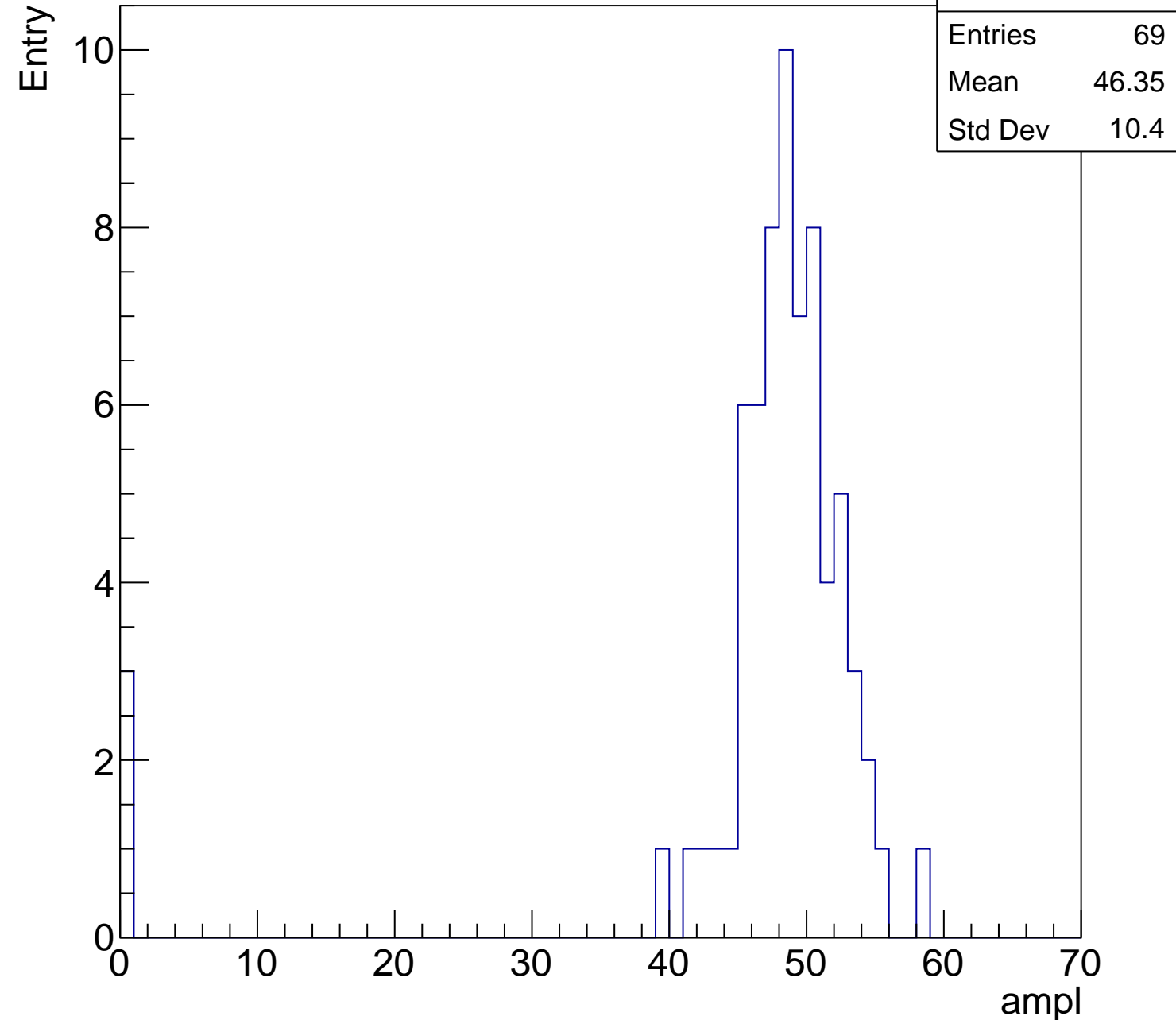
Entries	69
Mean	46.35
Std Dev	10.4

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

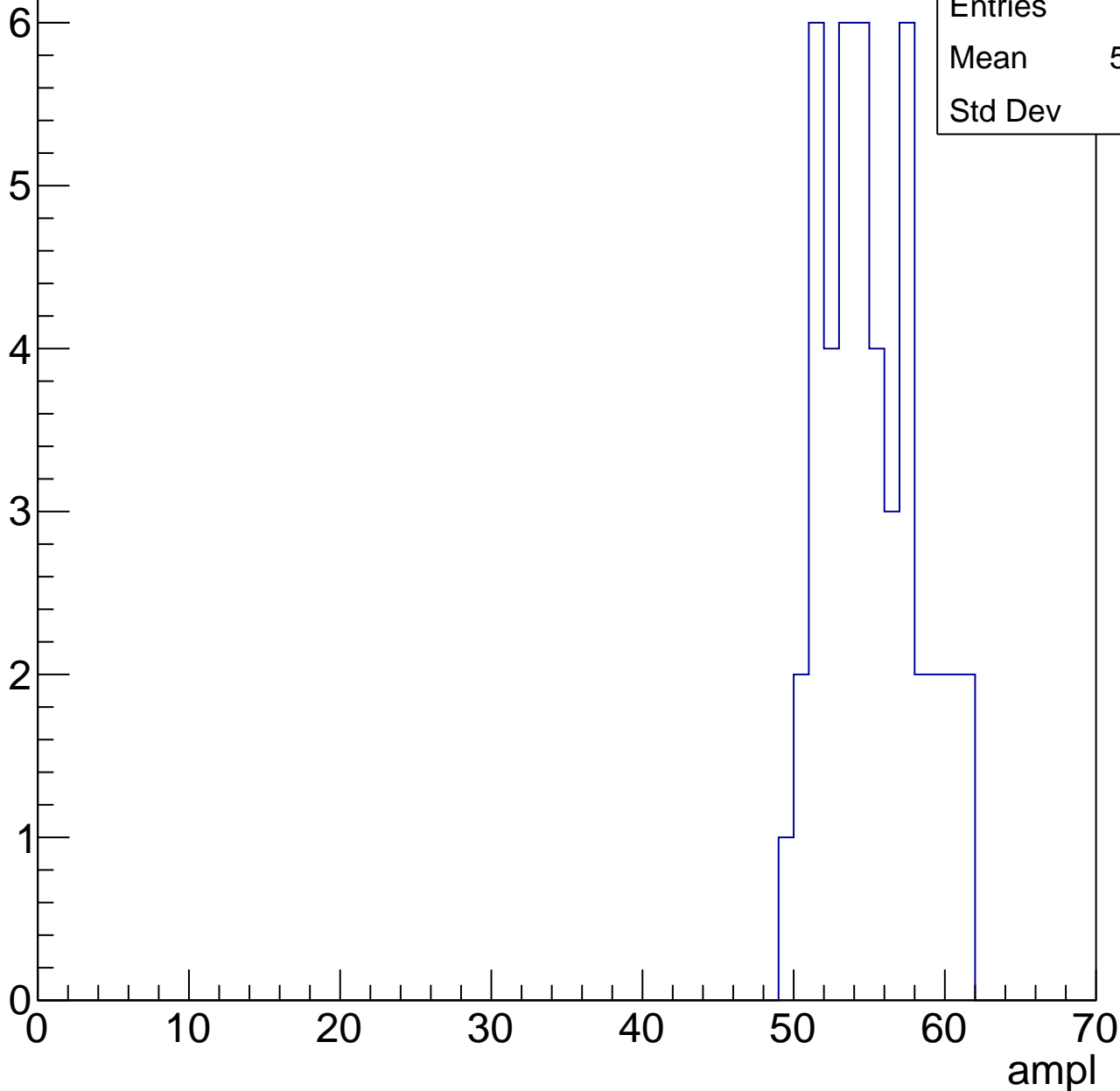


# B1L103S, U26-ch97, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	46
Mean	54.59
Std Dev	3.09

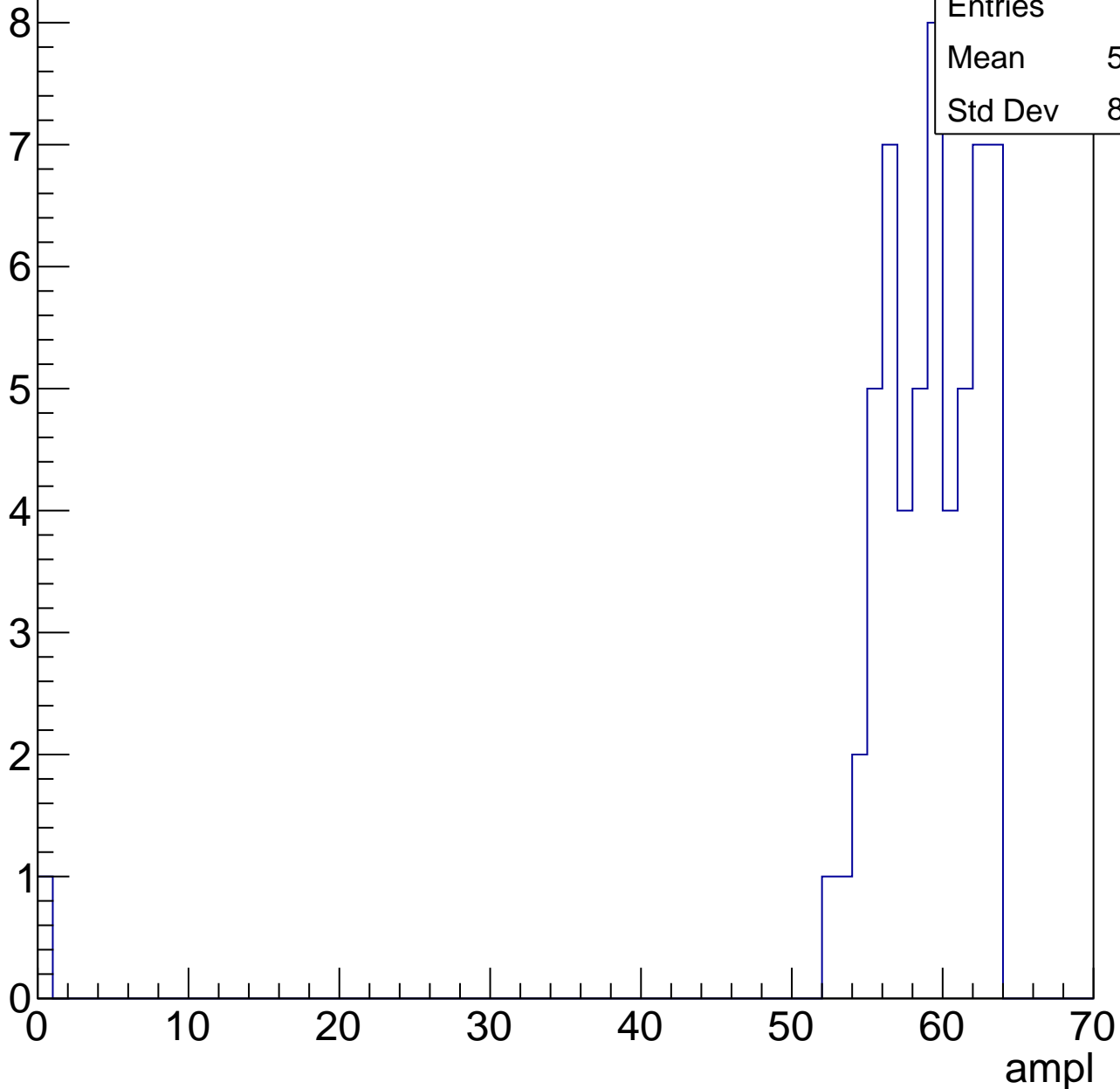


# B1L103S, U26-ch97, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

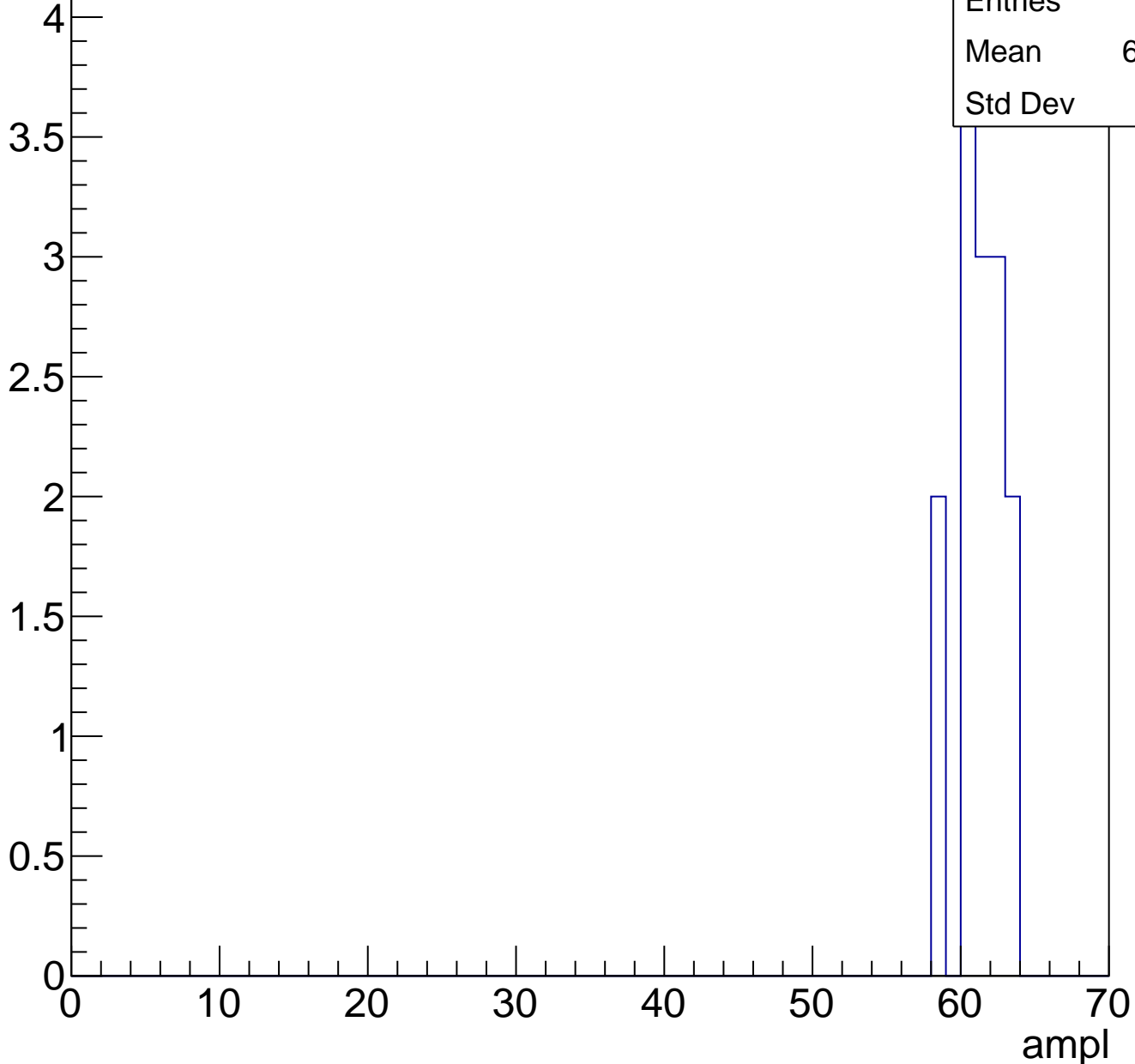
Entries	57
Mean	57.72
Std Dev	8.256



# B1L103S, U26-ch97, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



Entries	14
Mean	60.79
Std Dev	1.52

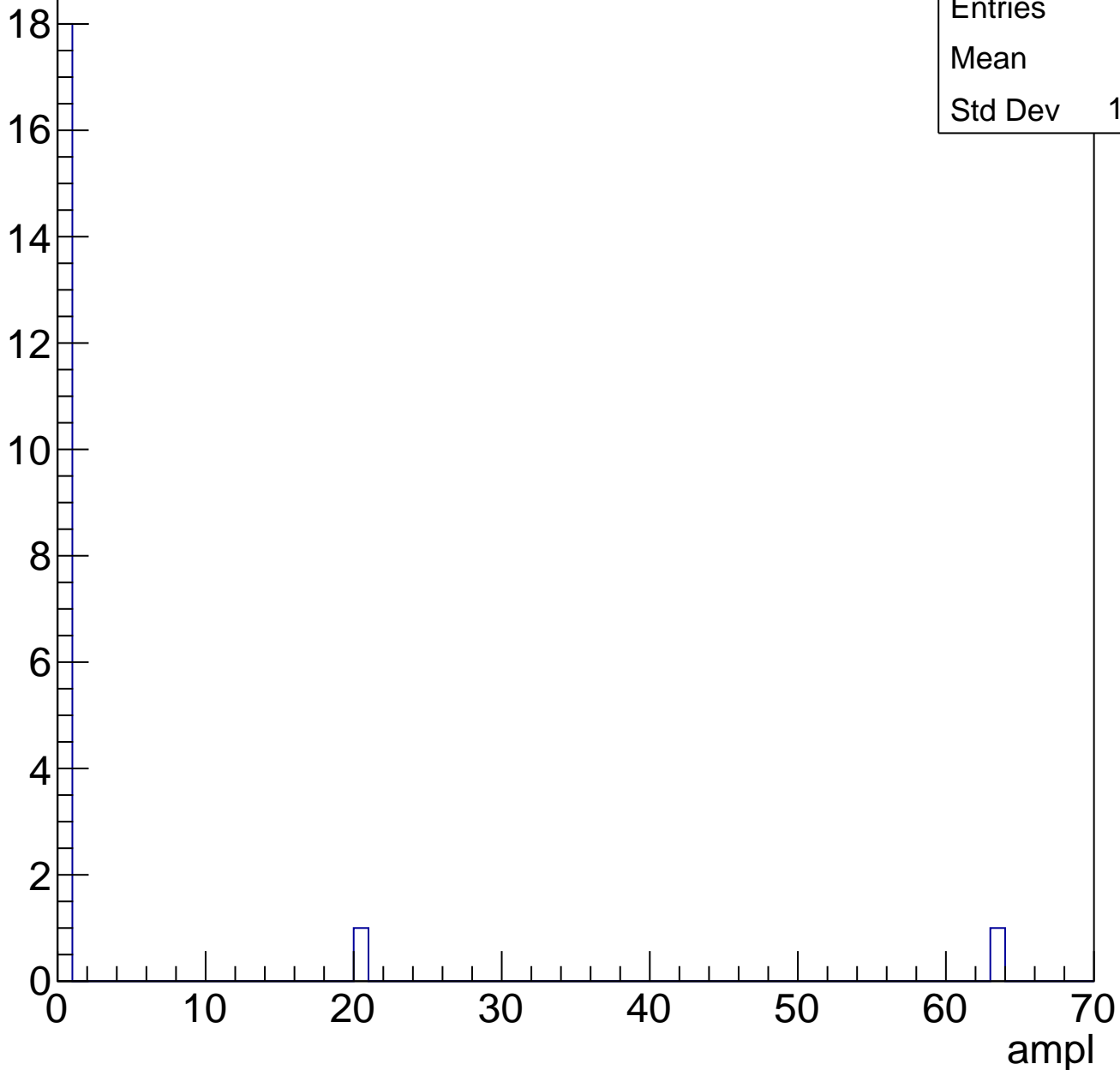


# B1L103S, U26-ch97, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	20
Mean	4.15
Std Dev	14.19

Entry



# B1L103S, U26-ch98, adc0

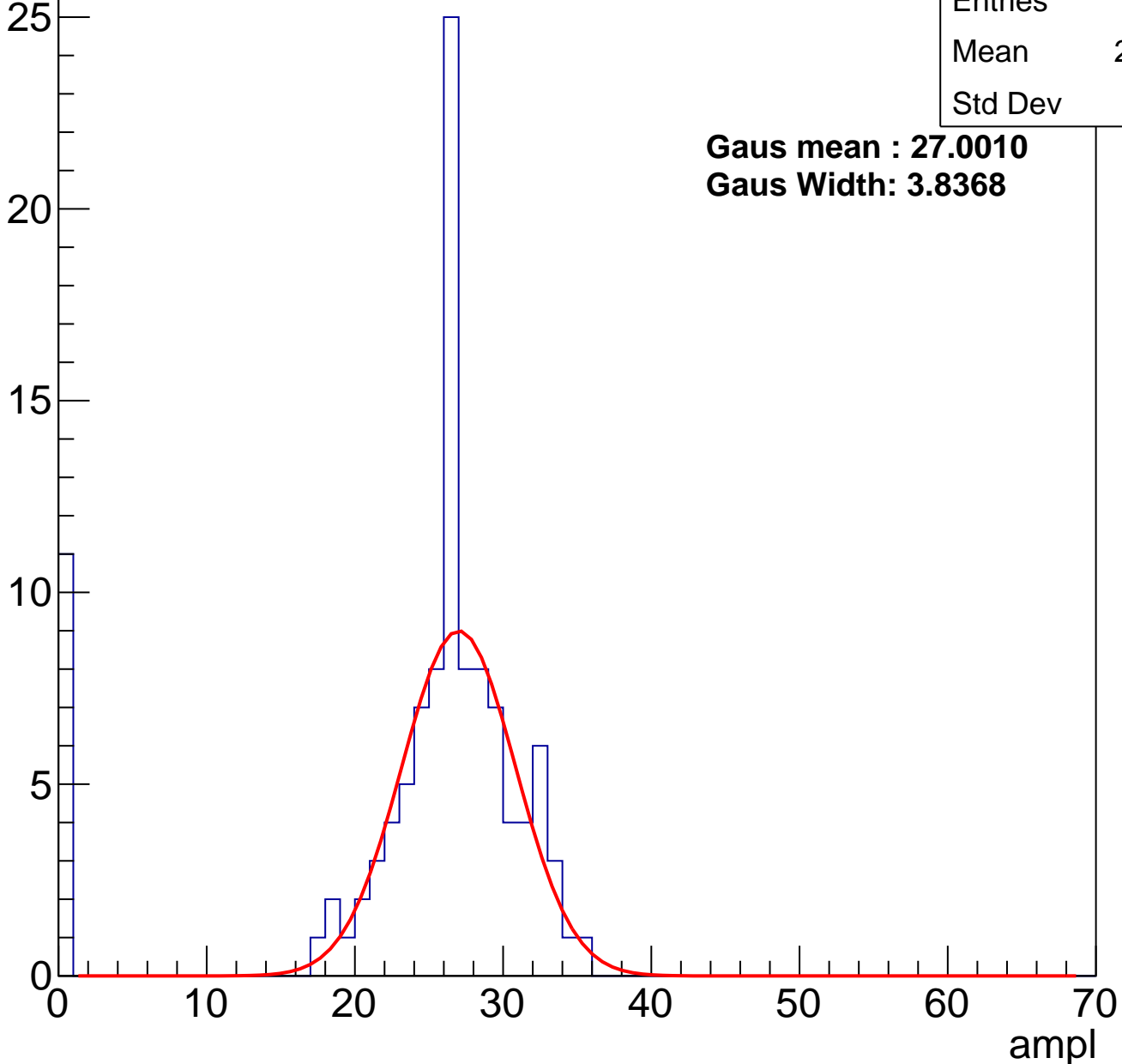
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	111
Mean	23.81
Std Dev	8.61

**Gaus mean : 27.0010**

**Gaus Width: 3.8368**

Entry



# B1L103S, U26-ch98, adc1

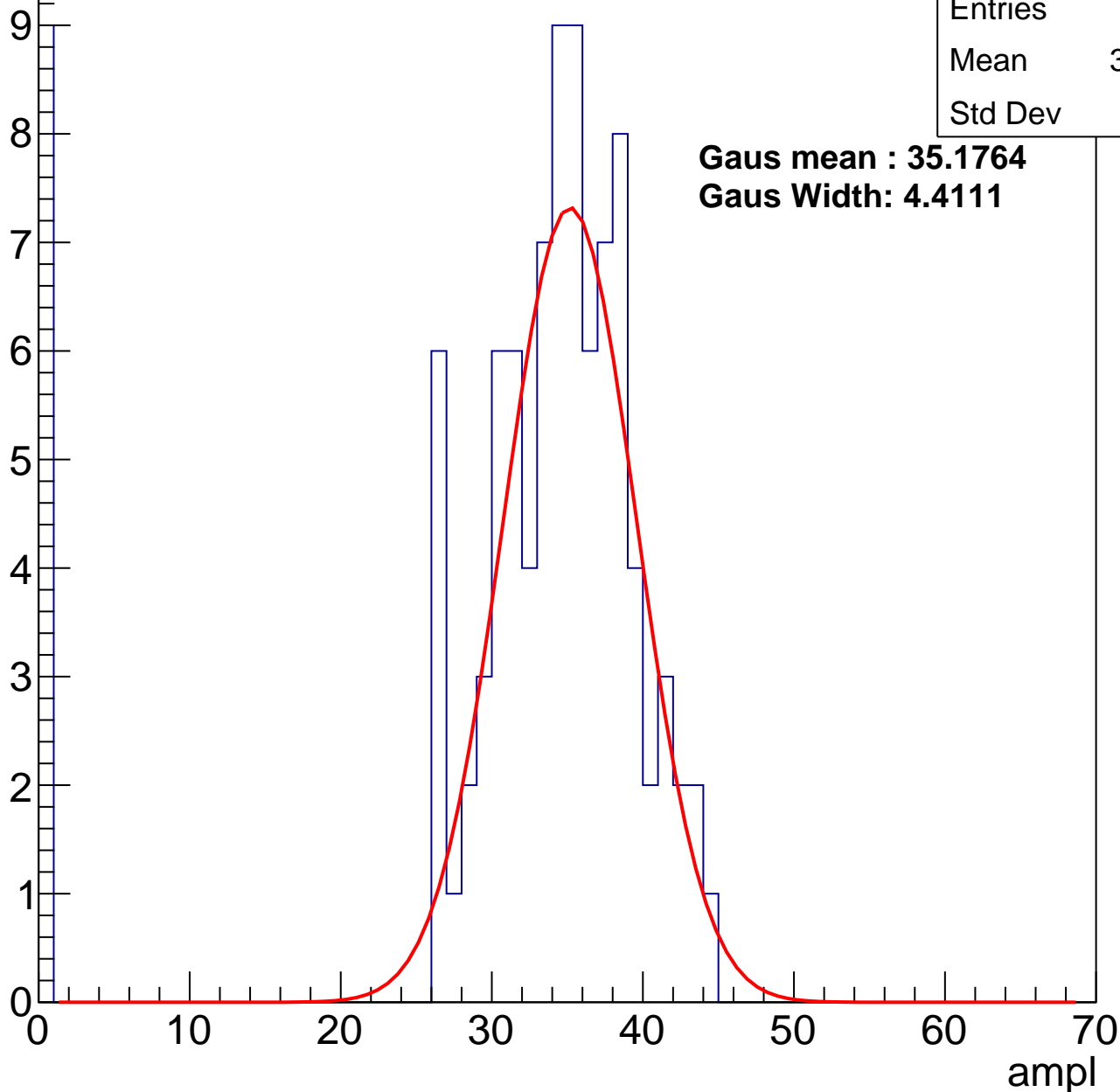
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	97
Mean	31.18
Std Dev	10.8

**Gaus mean : 35.1764**

**Gaus Width: 4.4111**



# B1L103S, U26-ch98, adc2

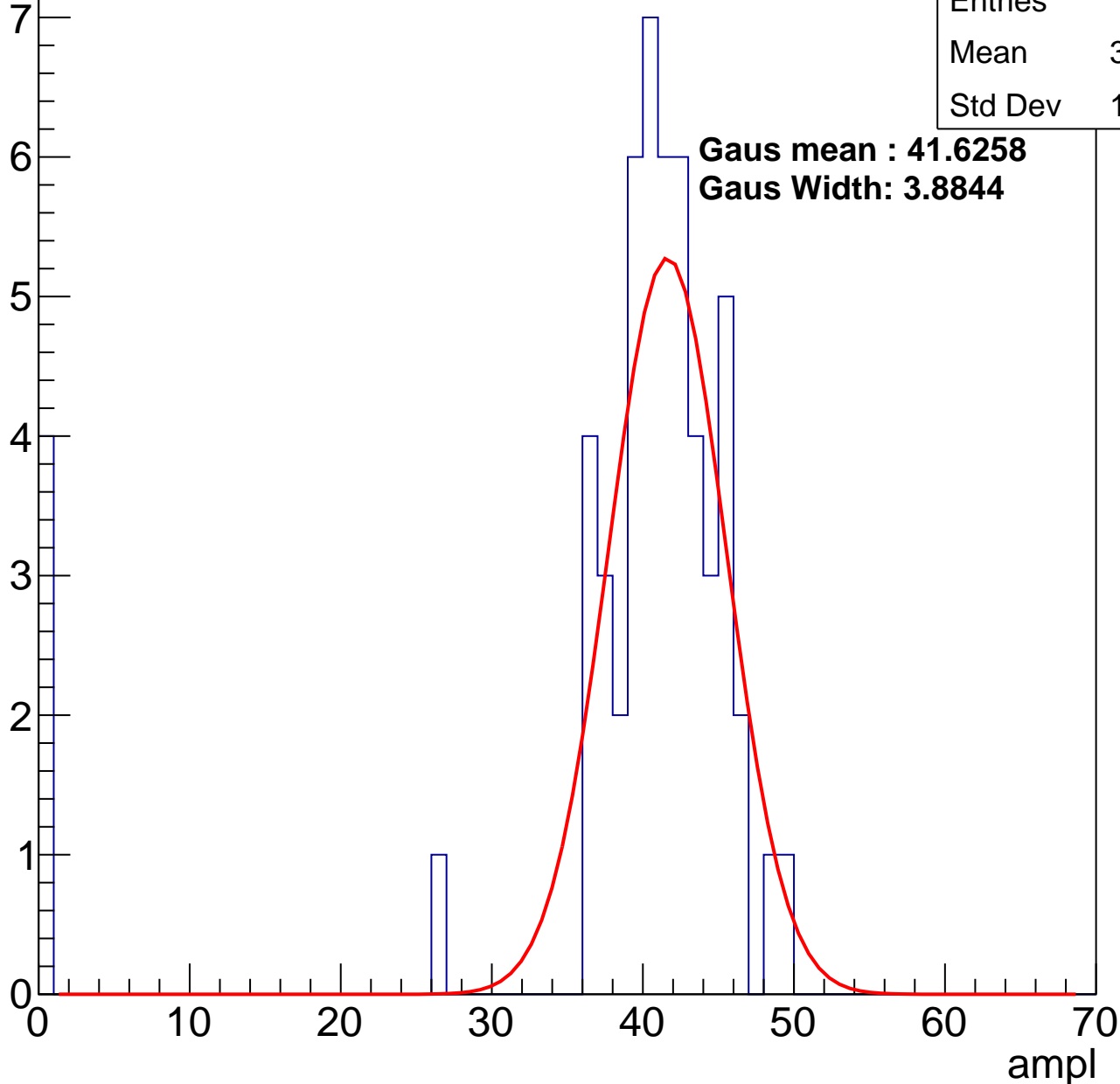
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	55
Mean	37.95
Std Dev	11.22

**Gaus mean : 41.6258**

**Gaus Width: 3.8844**

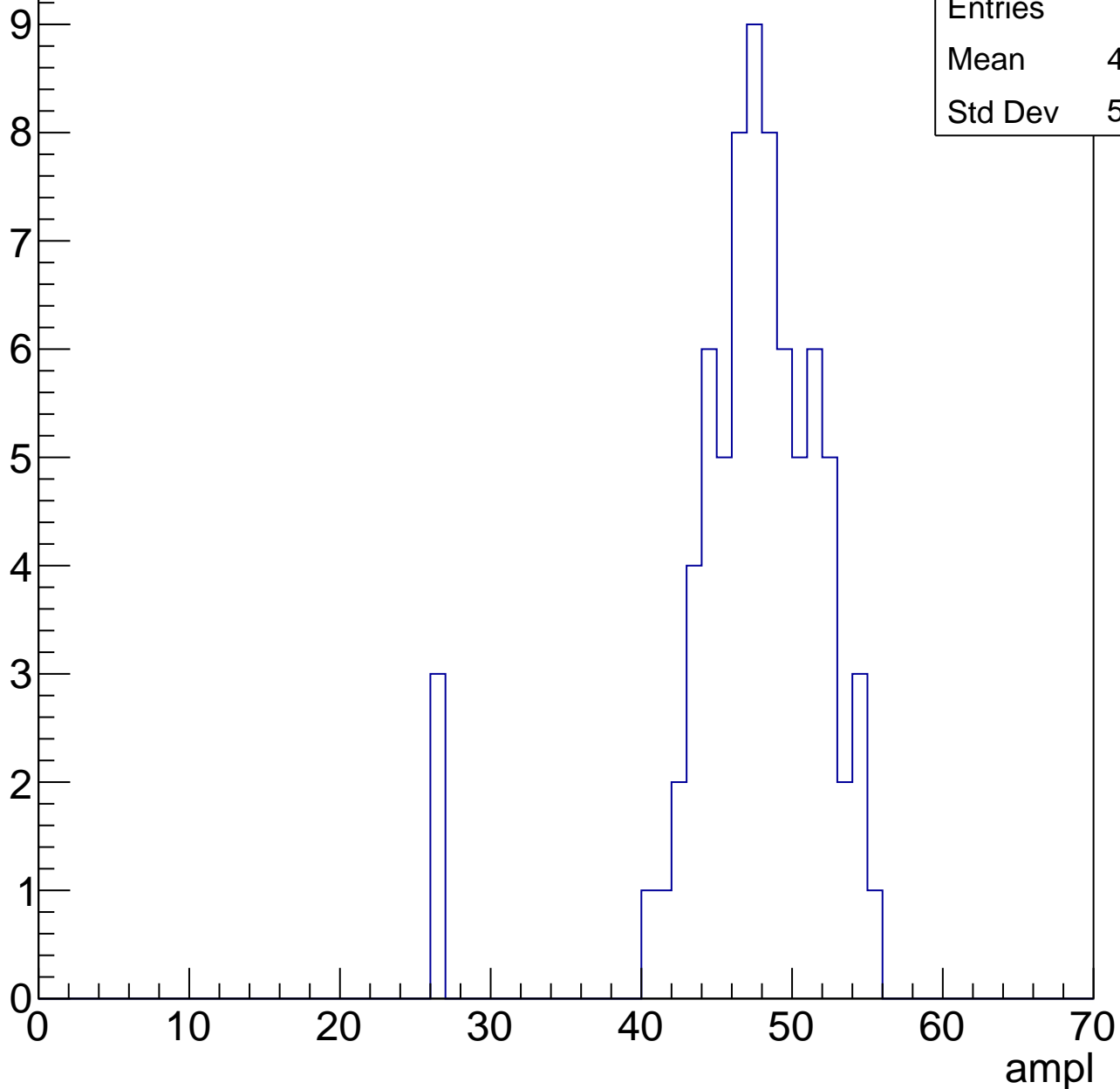


# B1L103S, U26-ch98, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

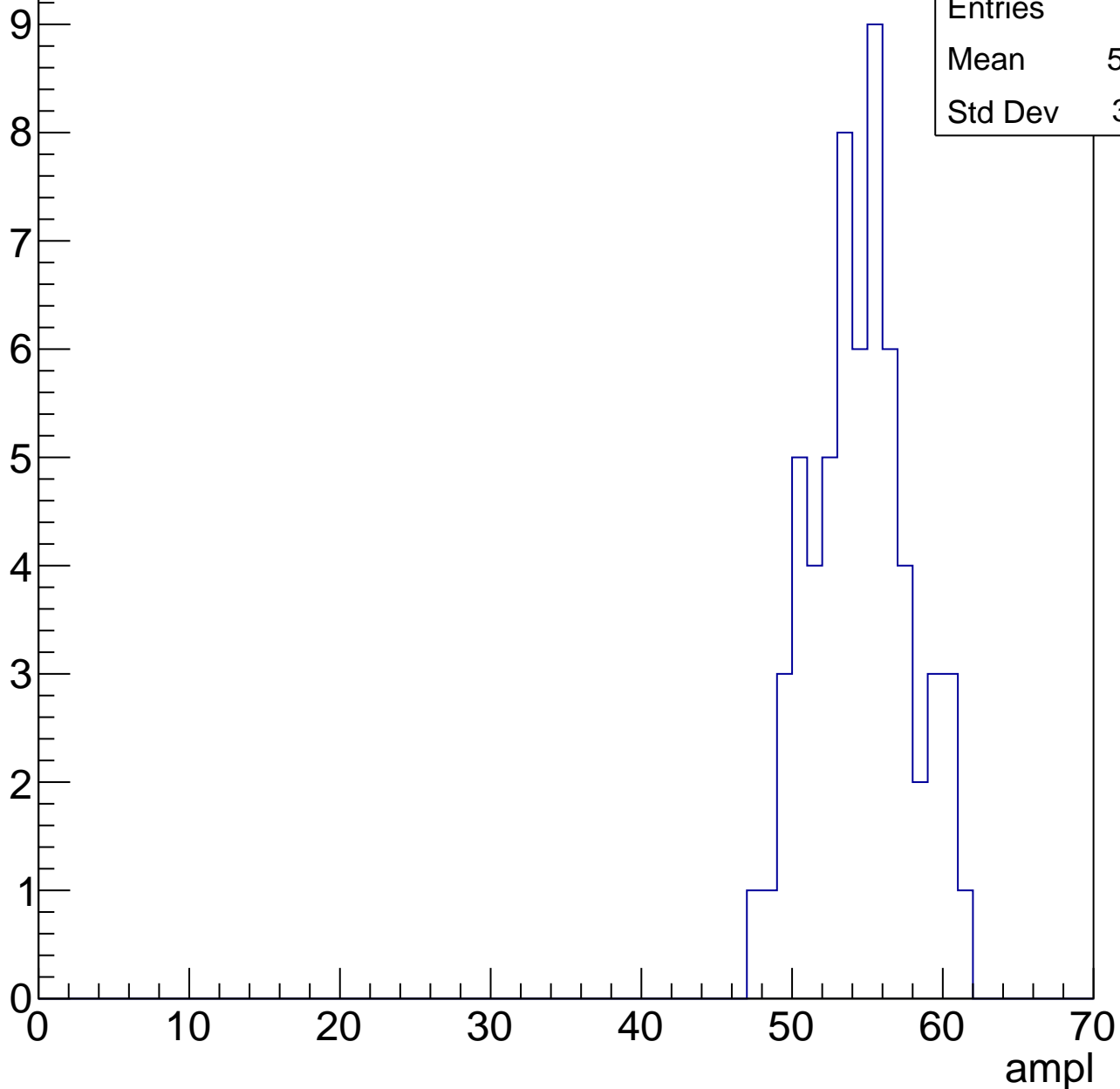
Entries	75
Mean	46.83
Std Dev	5.395



# B1L103S, U26-ch98, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

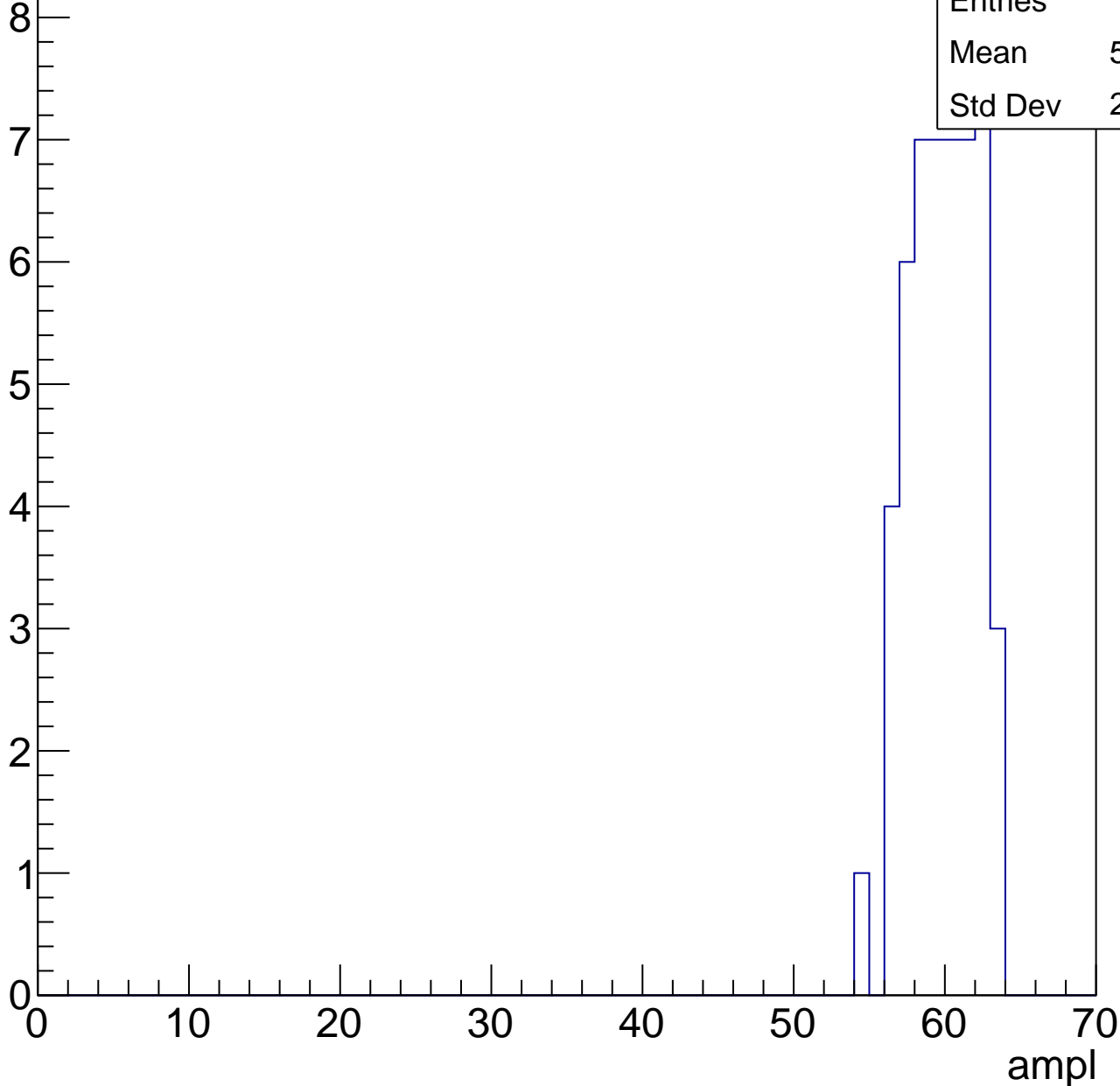


# B1L103S, U26-ch98, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	50
Mean	59.42
Std Dev	2.183

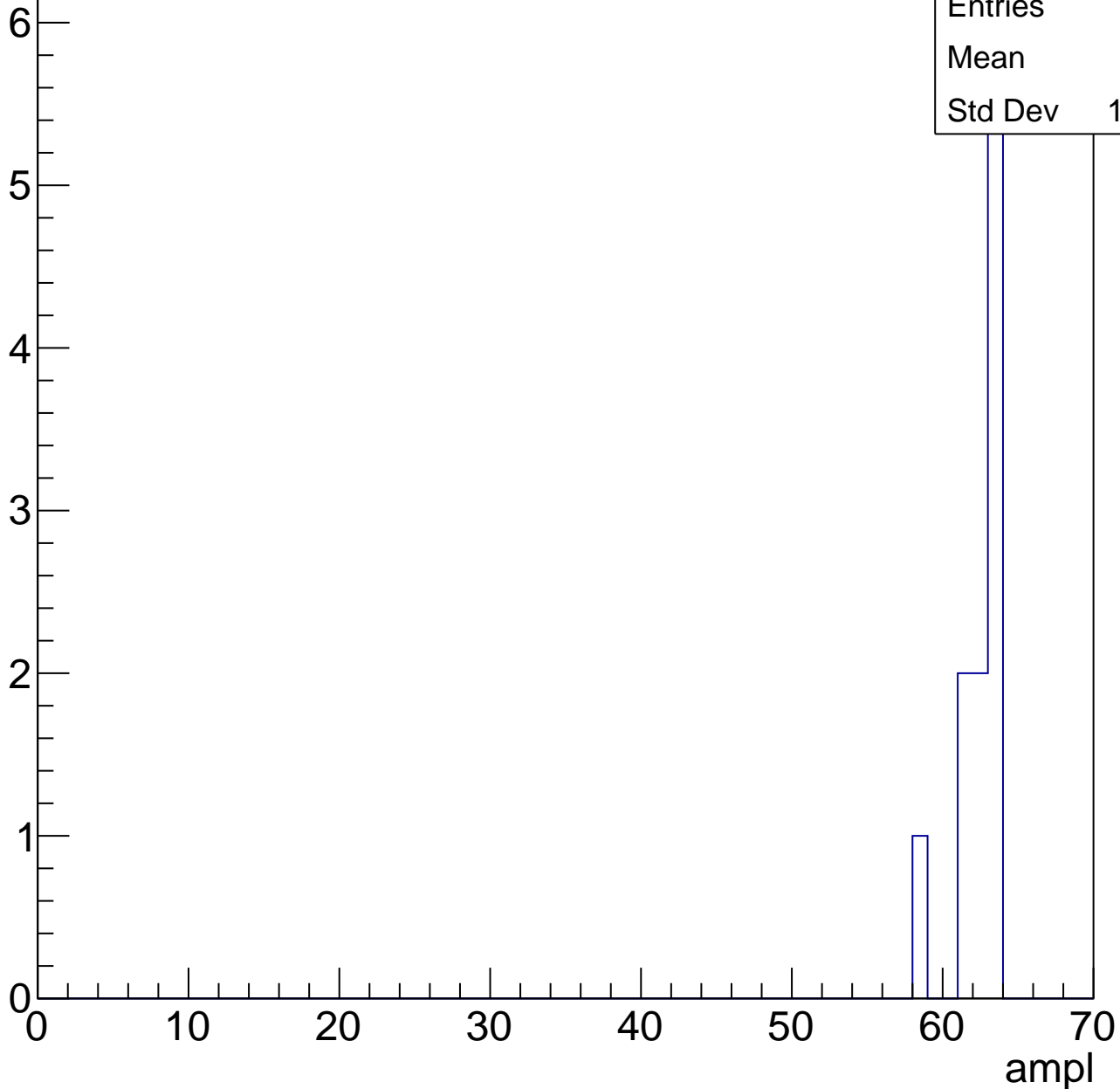


# B1L103S, U26-ch98, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	11
Mean	62
Std Dev	1.477





# B1L103S, U26-ch98, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

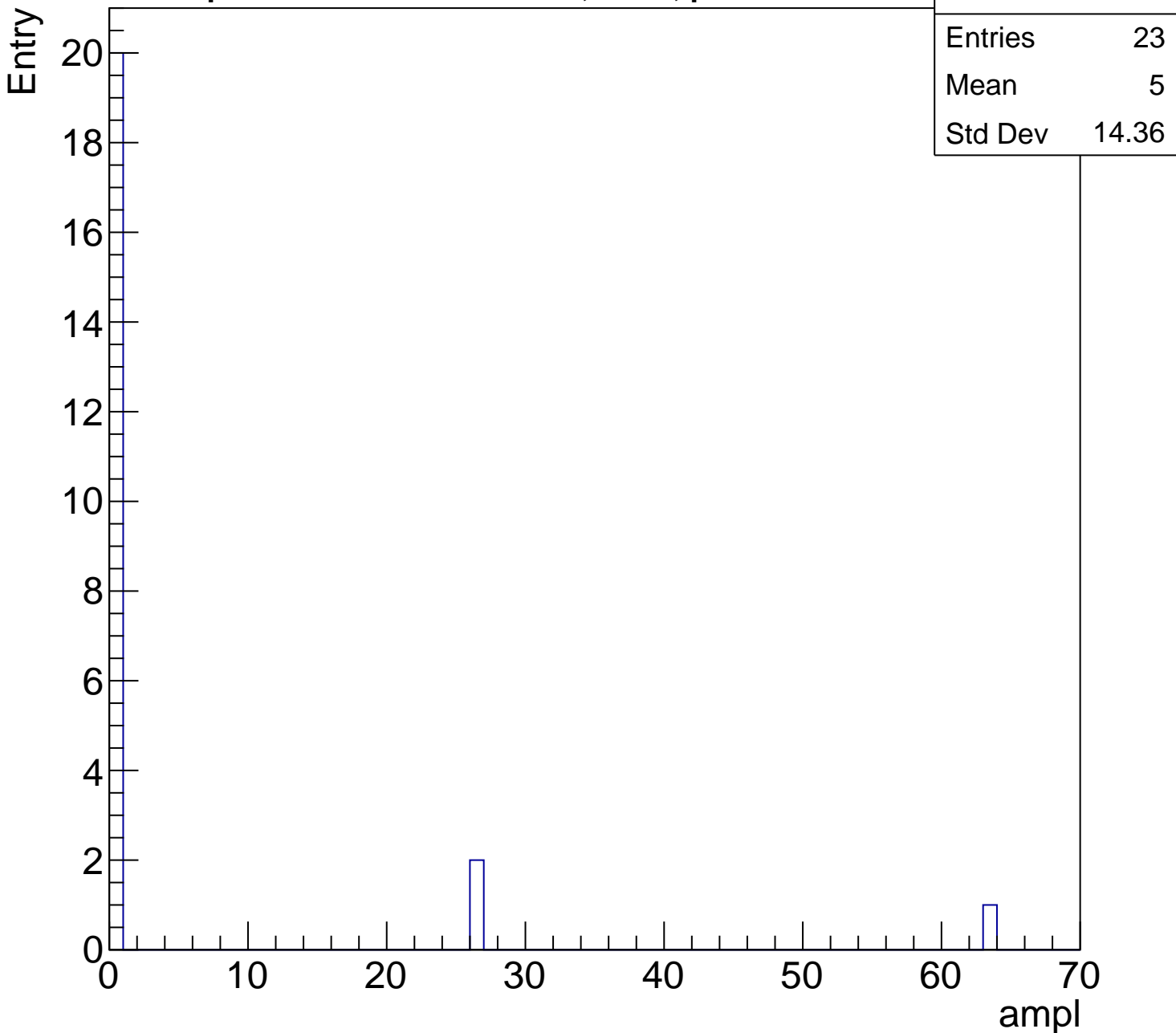
Entries	23
Mean	5
Std Dev	14.36

Entry

20  
18  
16  
14  
12  
10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B1L103S, U26-ch99, adc0

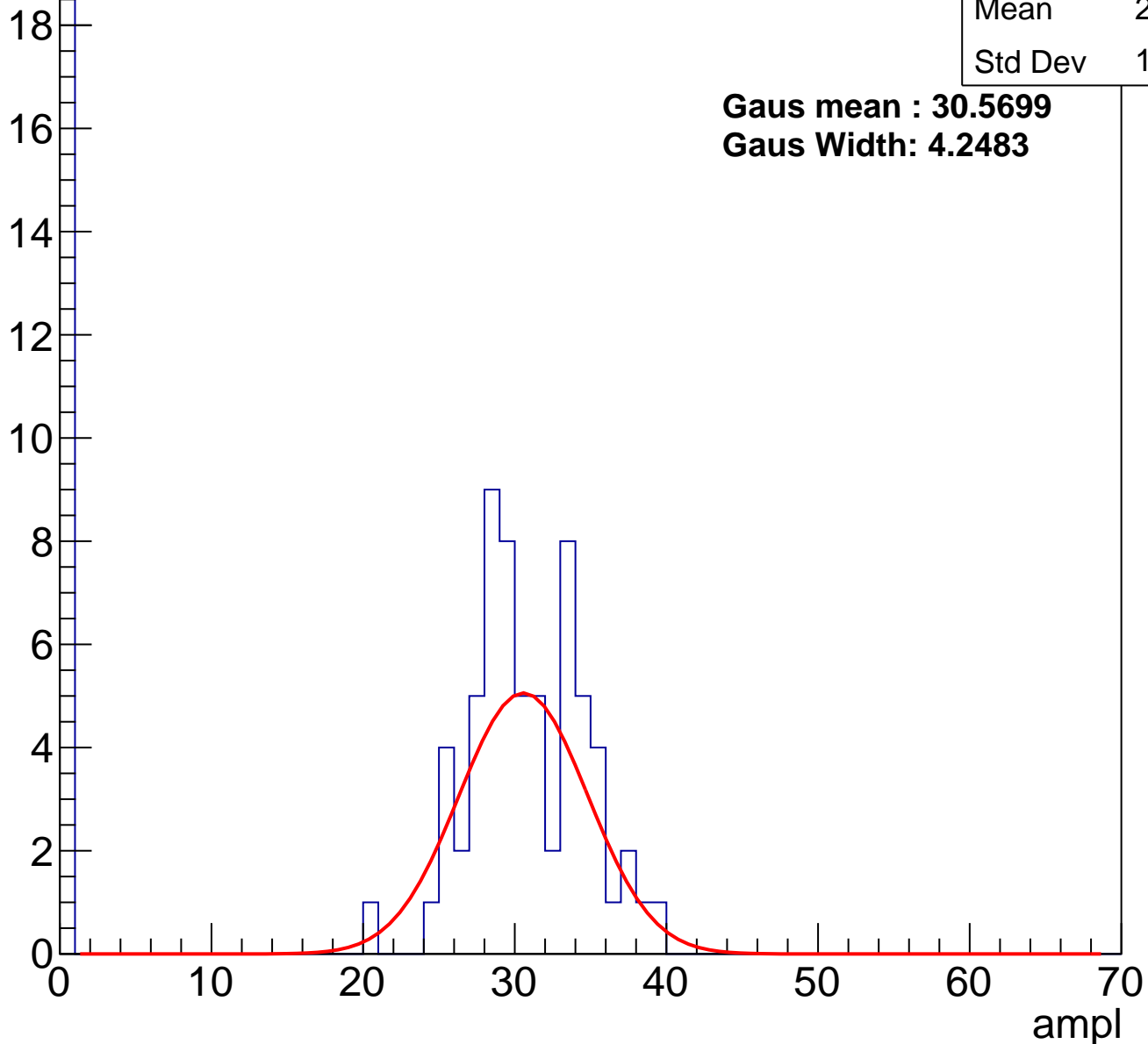
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	83
Mean	23.43
Std Dev	13.18

**Gaus mean : 30.5699**

**Gaus Width: 4.2483**

Entry



# B1L103S, U26-ch99, adc1

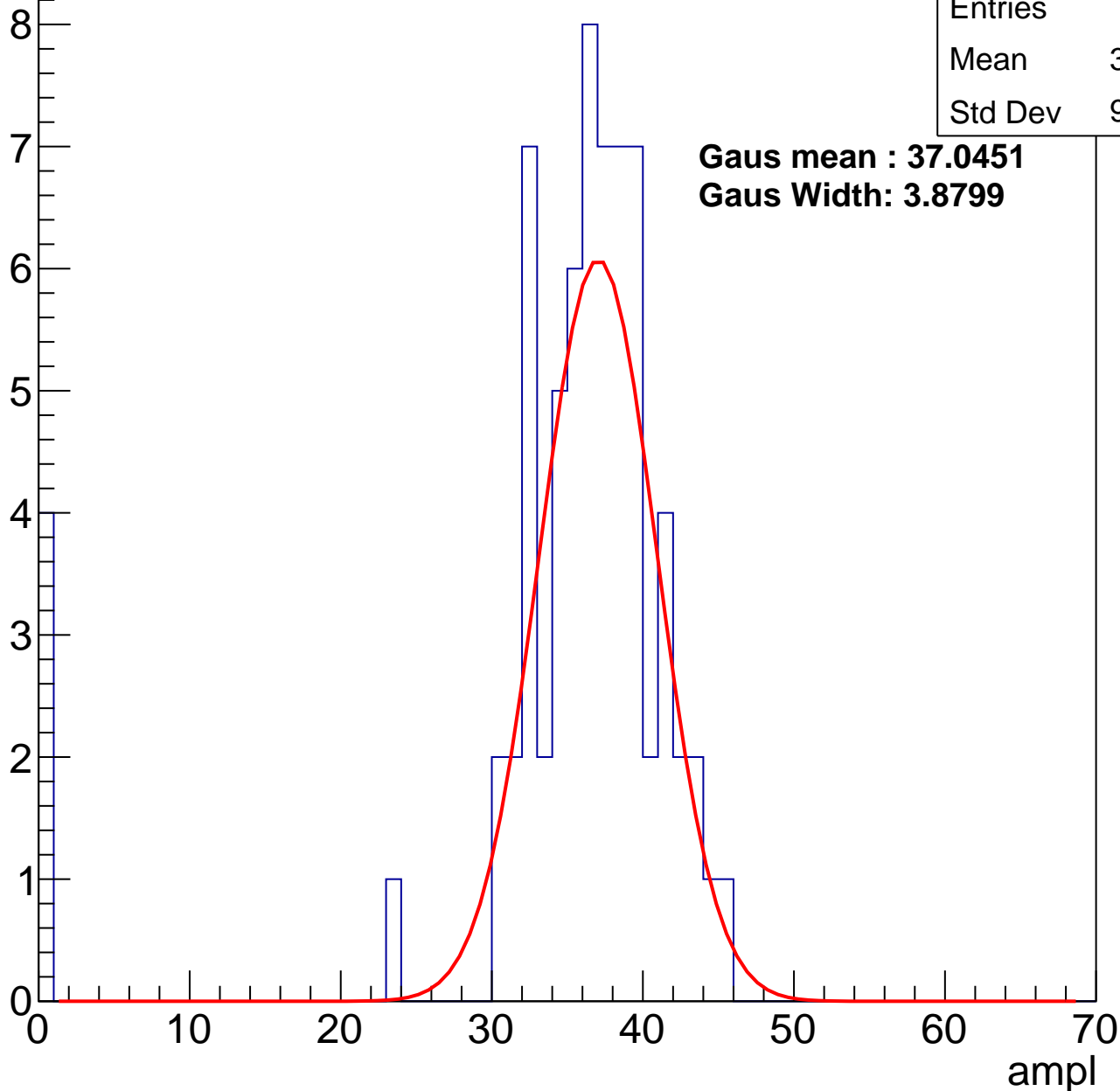
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	70
Mean	34.34
Std Dev	9.246

**Gaus mean : 37.0451**

**Gaus Width: 3.8799**



# B1L103S, U26-ch99, adc2

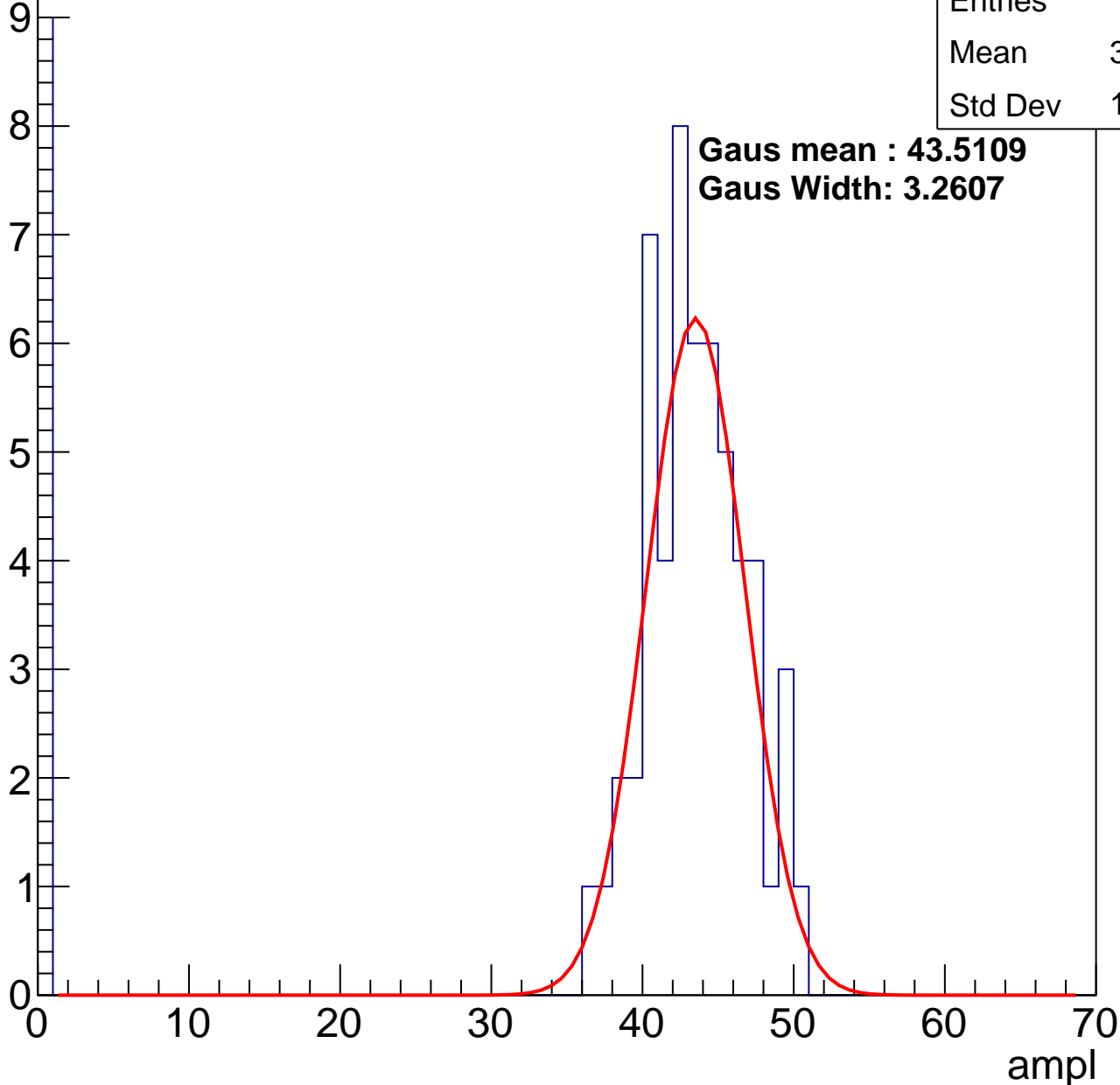
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	64
Mean	37.05
Std Dev	15.28

**Gaus mean : 43.5109**

**Gaus Width: 3.2607**

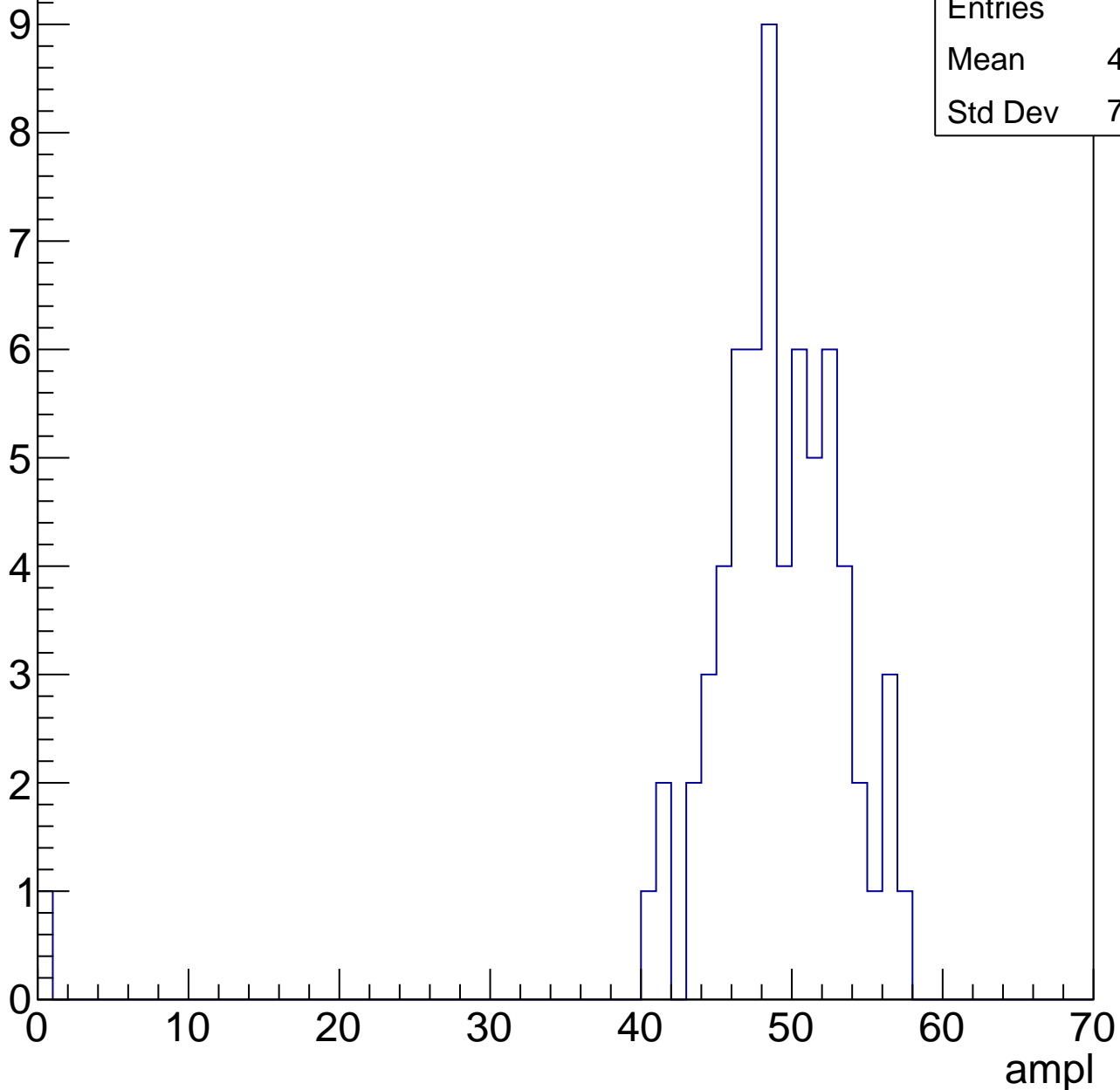


# B1L103S, U26-ch99, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	66
Mean	48.08
Std Dev	7.063

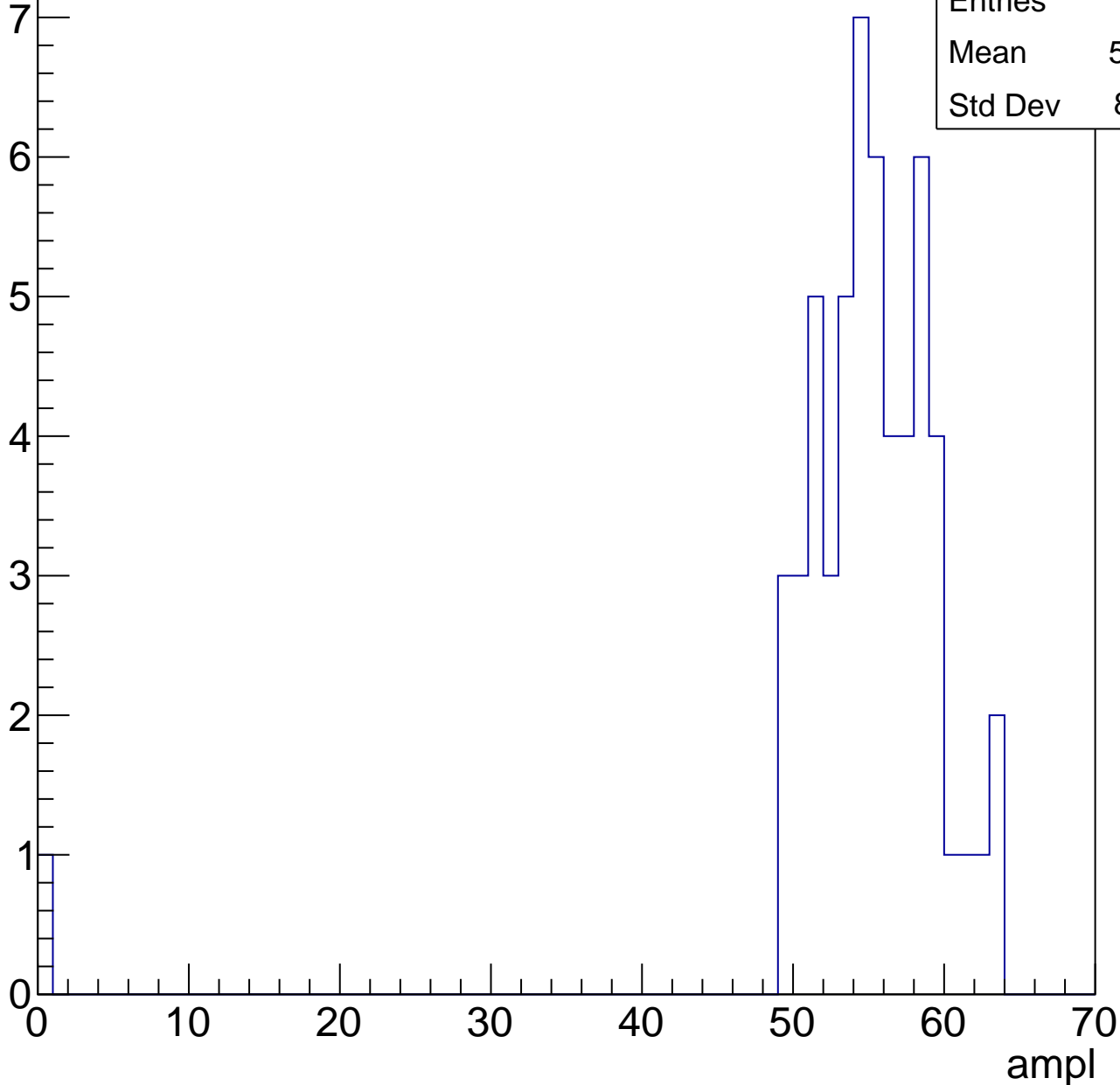


# B1L103S, U26-ch99, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

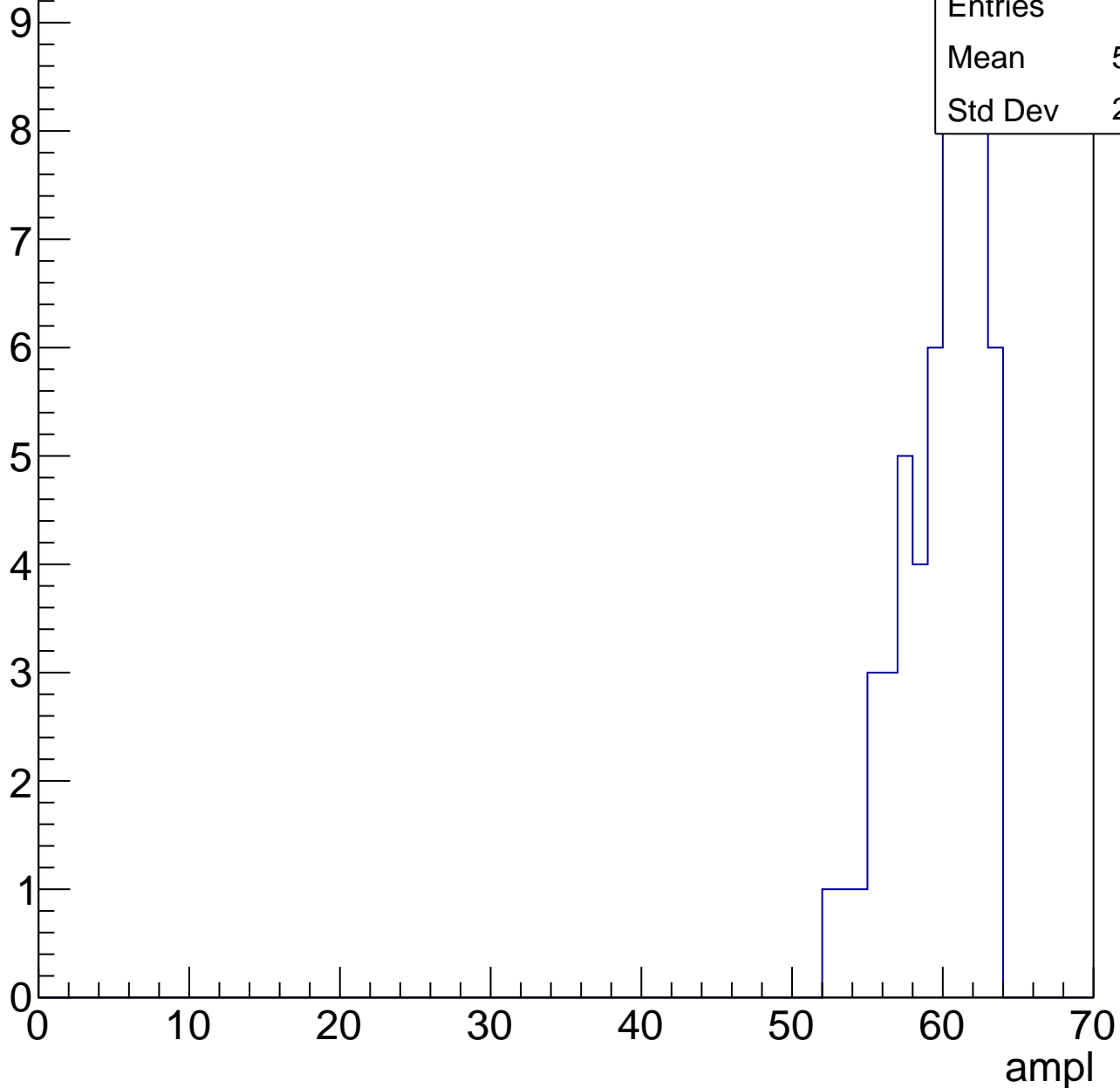
Entries	56
Mean	54.04
Std Dev	8.091



# B1L103S, U26-ch99, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



# B1L103S, U26-ch99, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	3
Mean	62.33
Std Dev	0.9428

0 10 20 30 40 50 60 70

ampl





# B1L103S, U26-ch99, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

18  
16  
14  
12  
10  
8  
6  
4  
2  
0

Entries	19
Mean	0
Std Dev	0

ampl

# B1L103S, U26-ch100, adc0

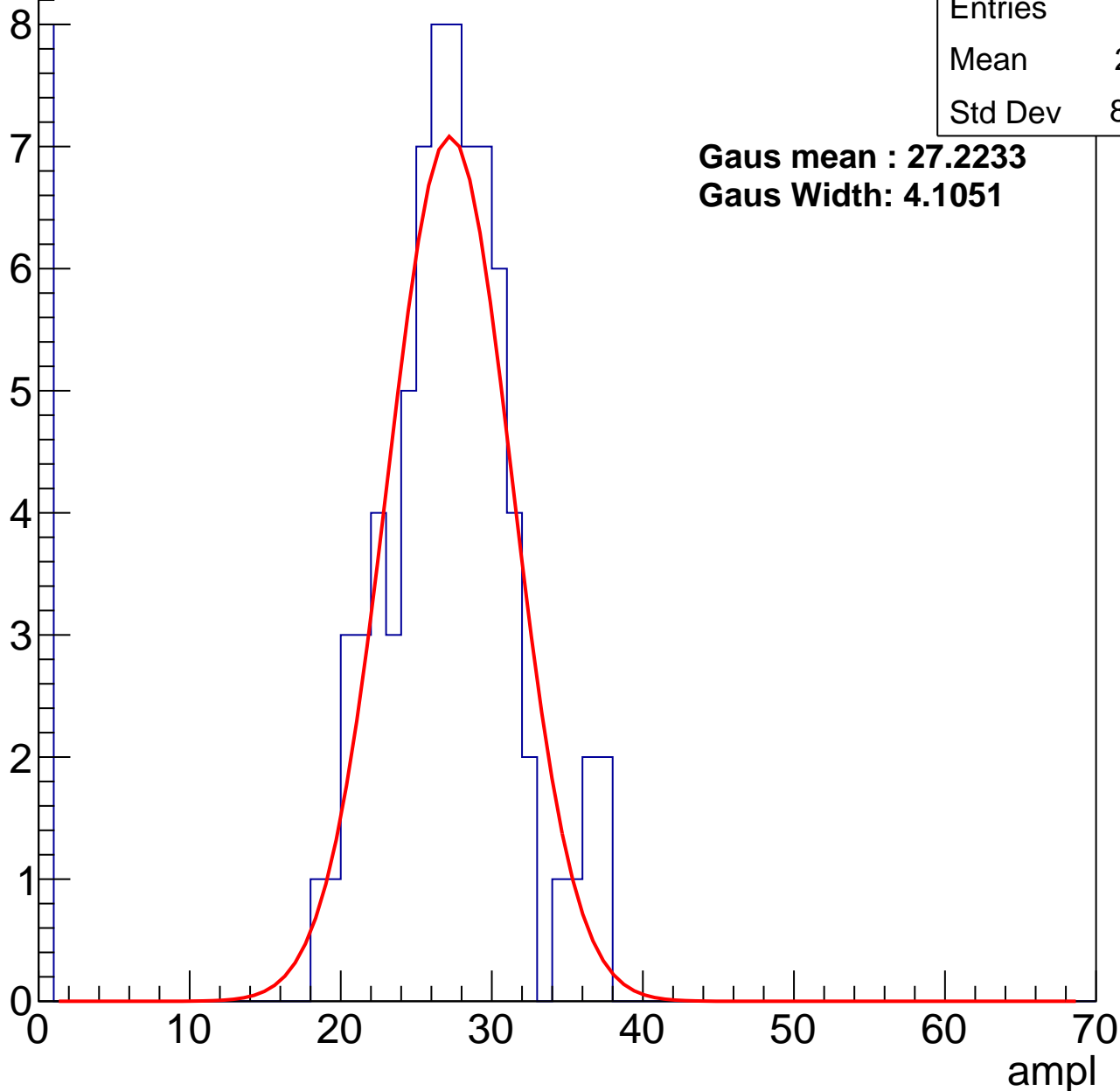
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	83
Mean	24.31
Std Dev	8.877

**Gaus mean : 27.2233**

**Gaus Width: 4.1051**



# B1L103S, U26-ch100, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	62
Mean	33.53
Std Dev	3.031

**Gaus mean : 34.0515**

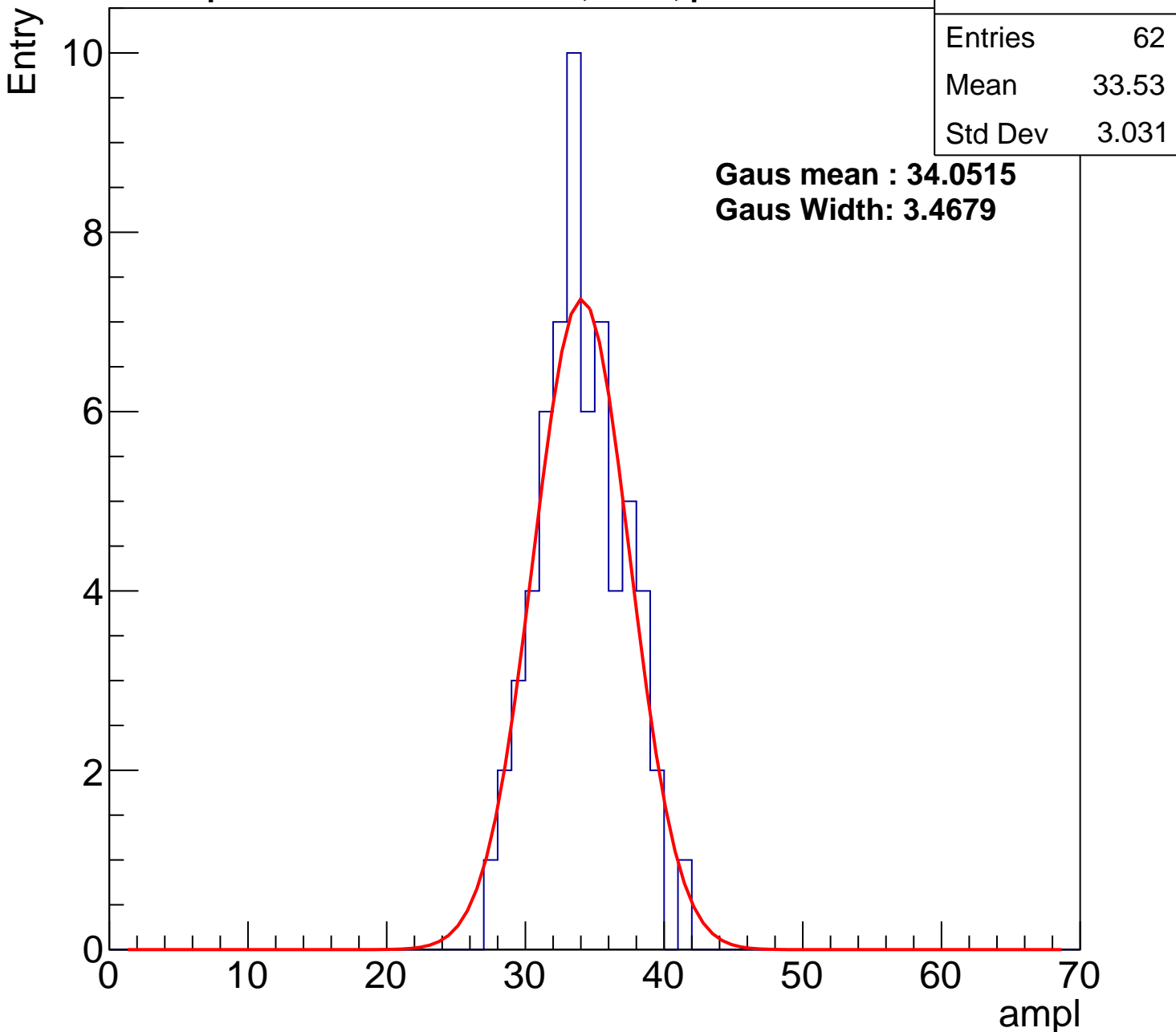
**Gaus Width: 3.4679**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U26-ch100, adc2

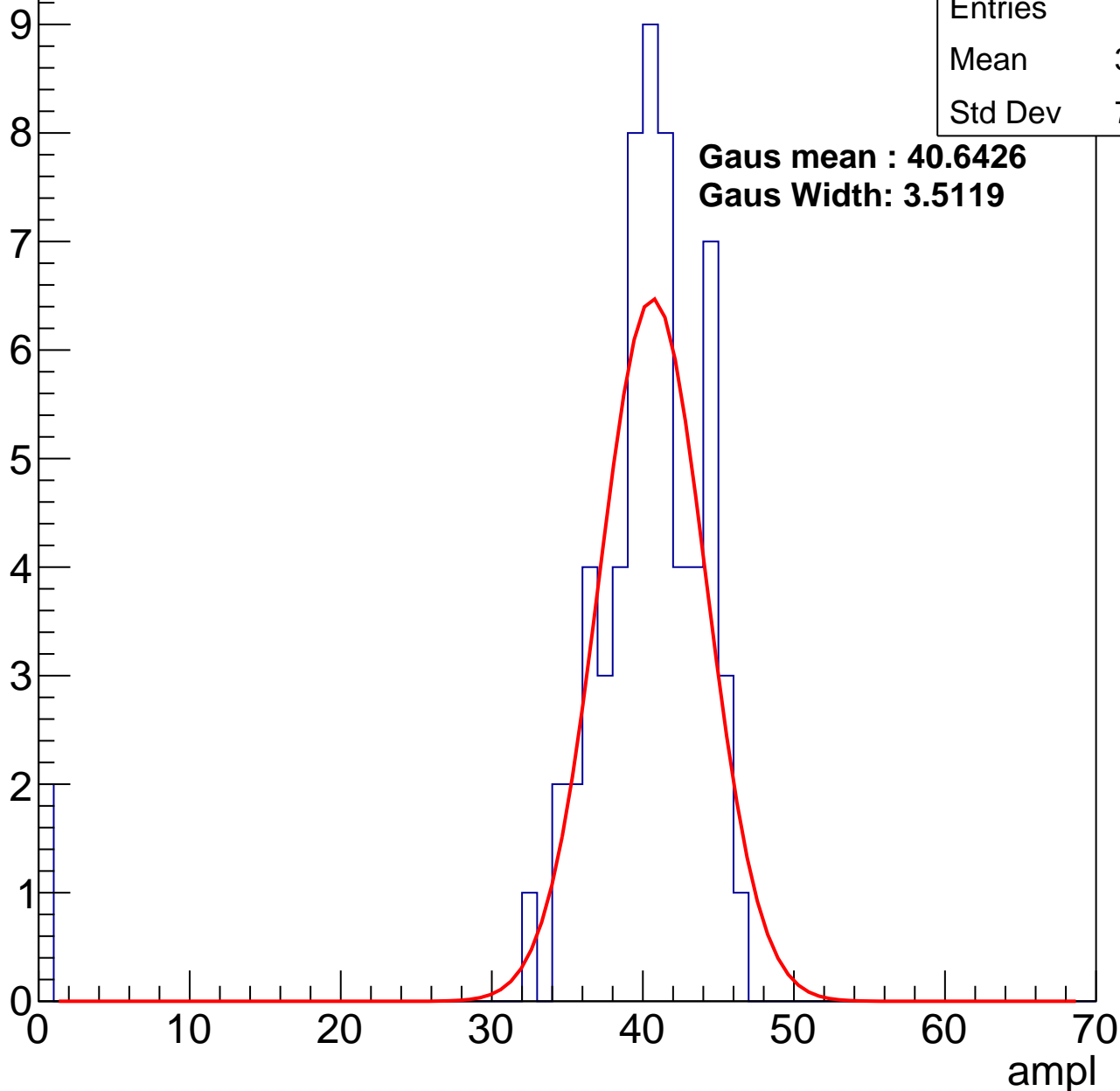
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	62
Mean	38.81
Std Dev	7.721

**Gaus mean : 40.6426**

**Gaus Width: 3.5119**



# B1L103S, U26-ch100, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	78
Mean	39.72
Std Dev	16.48

Entry

10

8

6

4

2

0

0

10

20

30

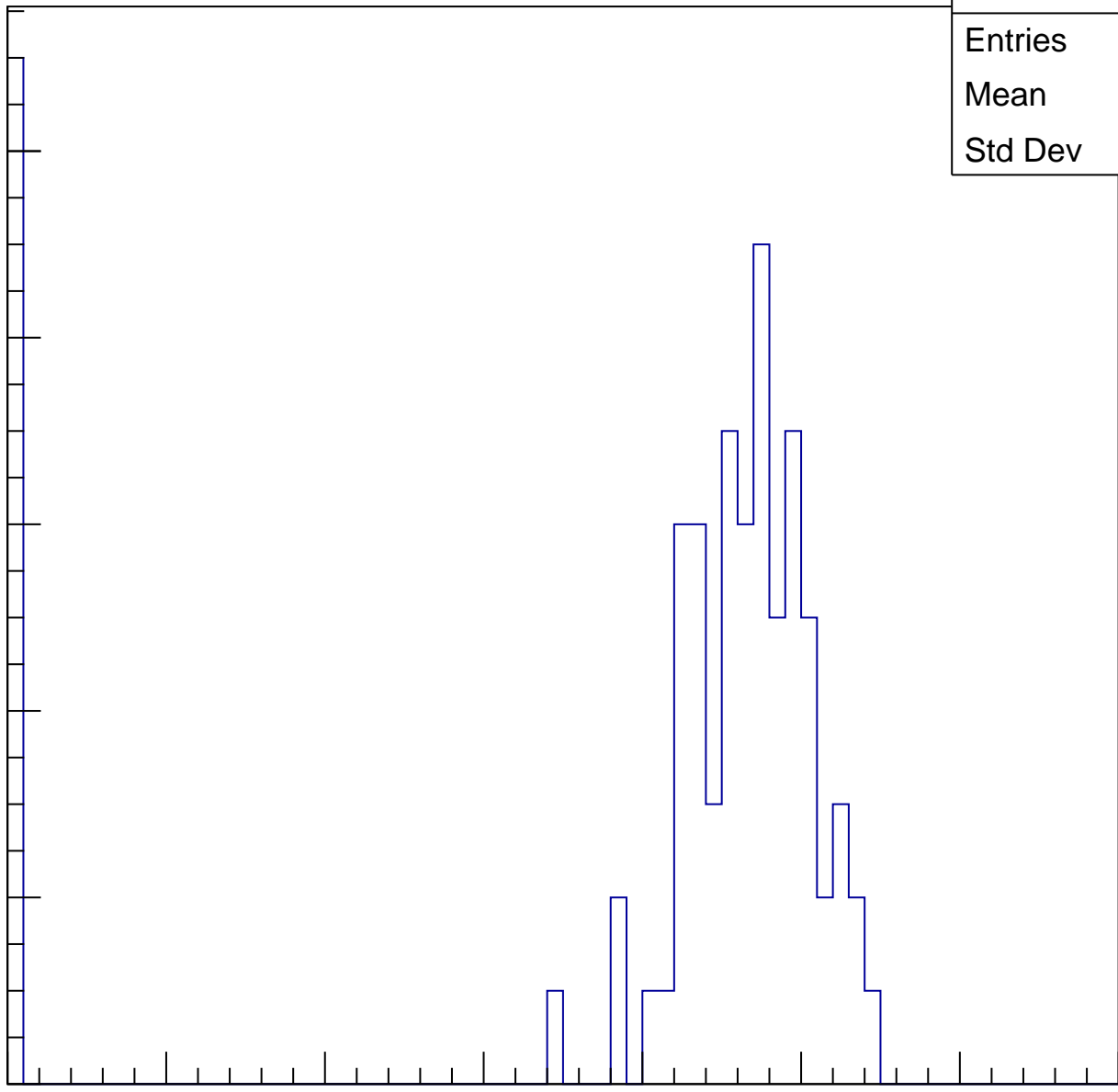
40

50

60

70

ampl

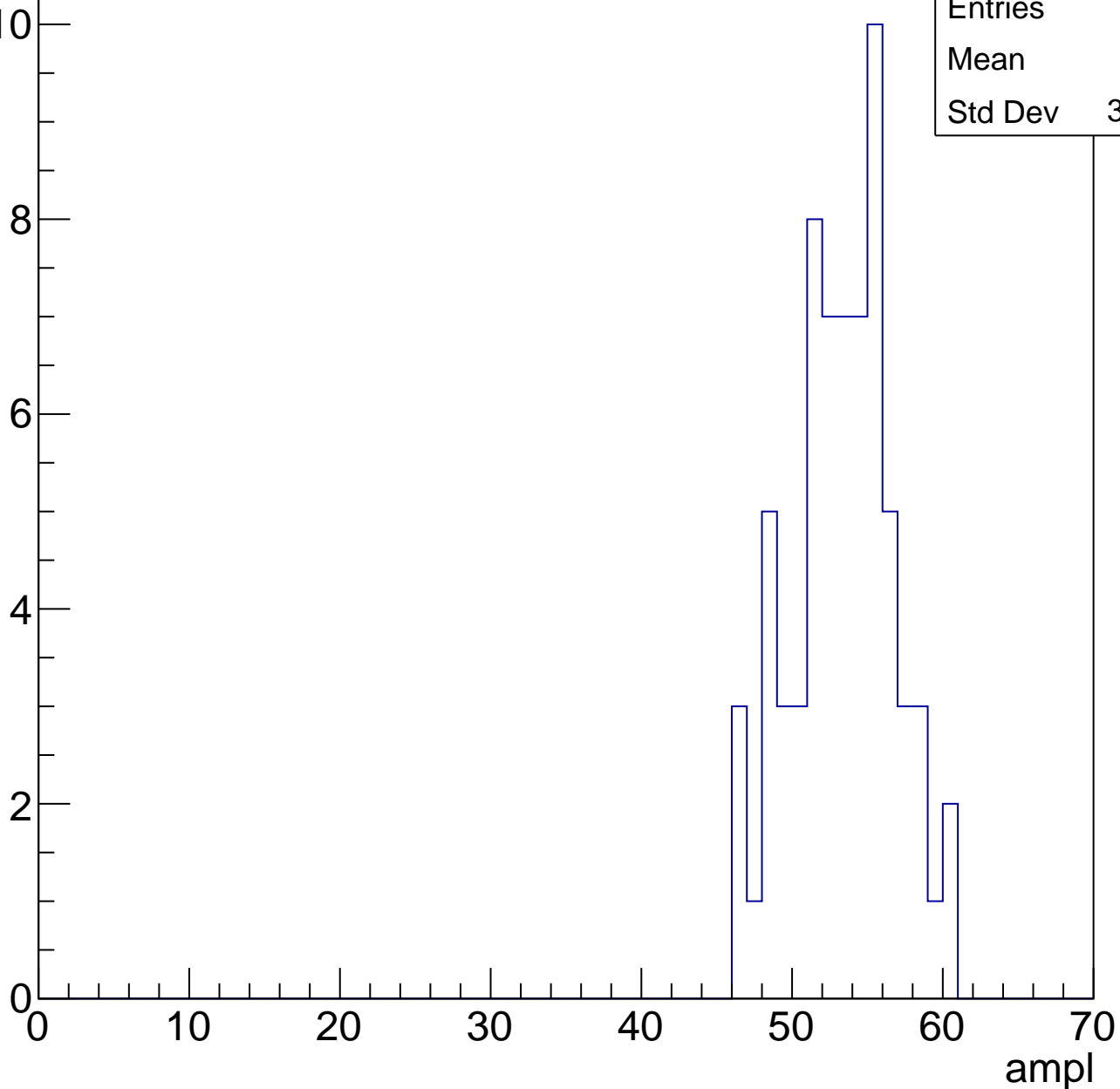


# B1L103S, U26-ch100, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	68
Mean	52.9
Std Dev	3.366

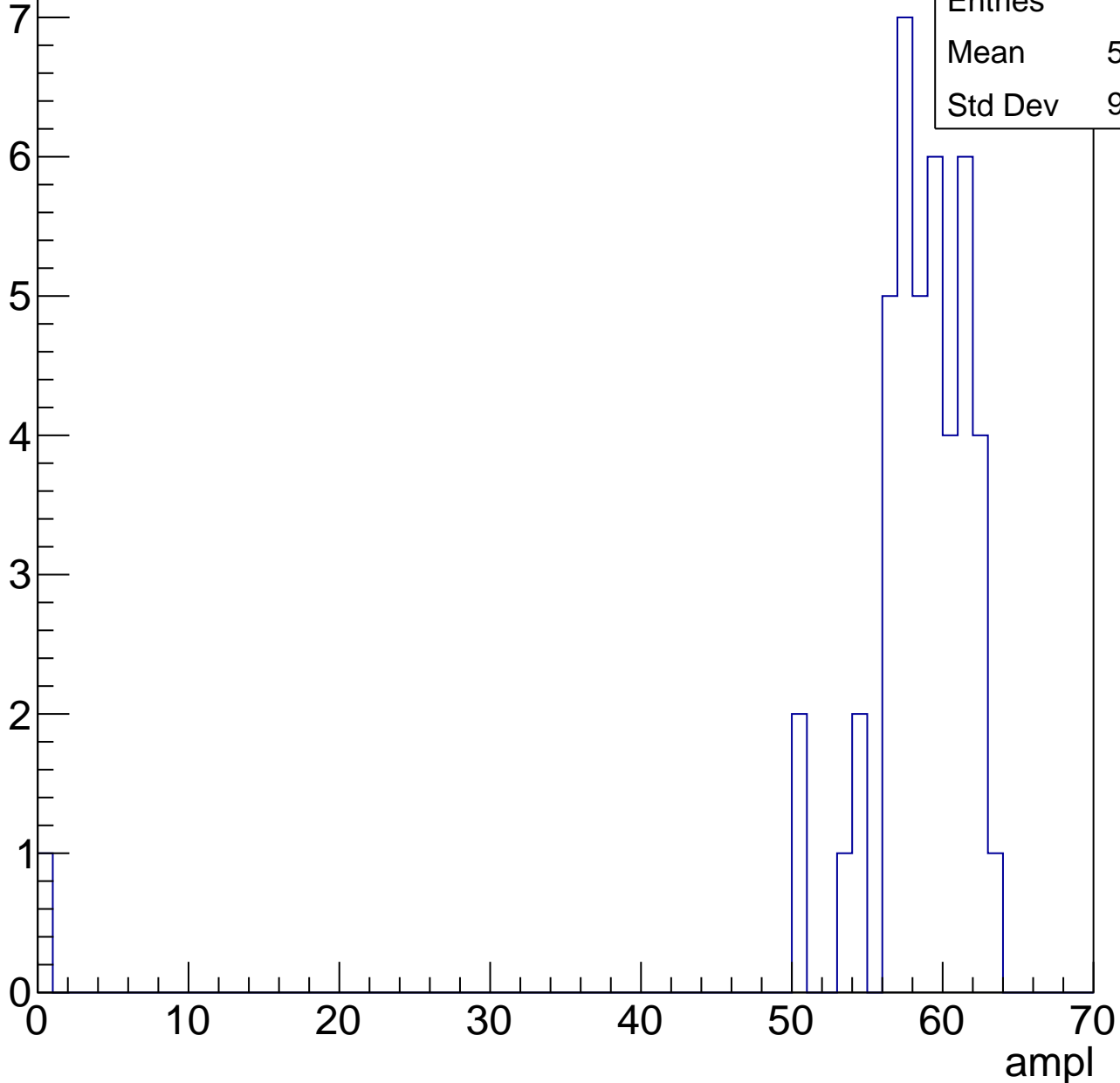


# B1L103S, U26-ch100, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	44
Mean	56.84
Std Dev	9.148

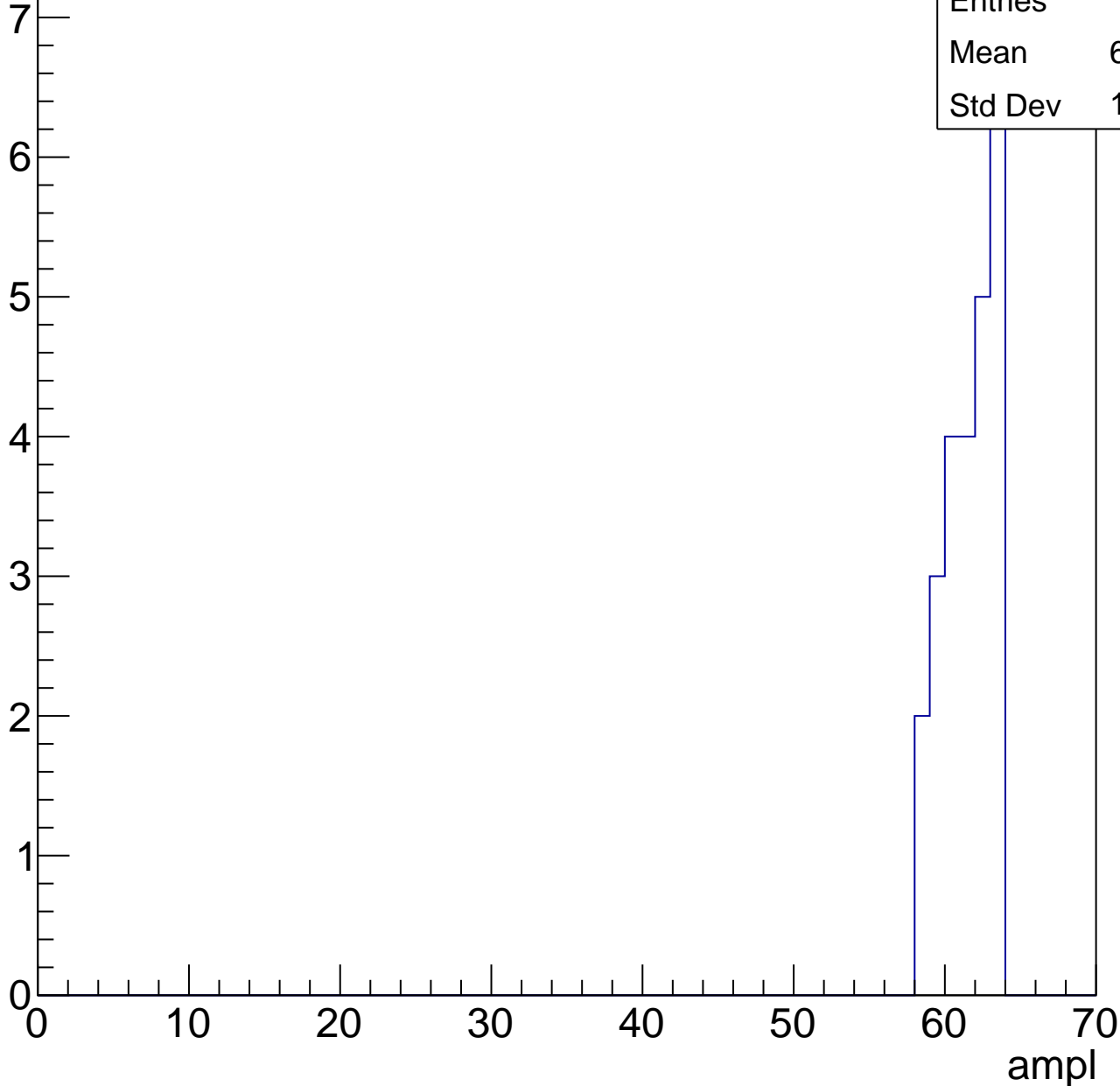


# B1L103S, U26-ch100, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	25
Mean	61.12
Std Dev	1.633





# B1L103S, U26-ch100, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	22
Mean	8.545
Std Dev	21.51

Entry



# B1L103S, U26-ch101, adc0

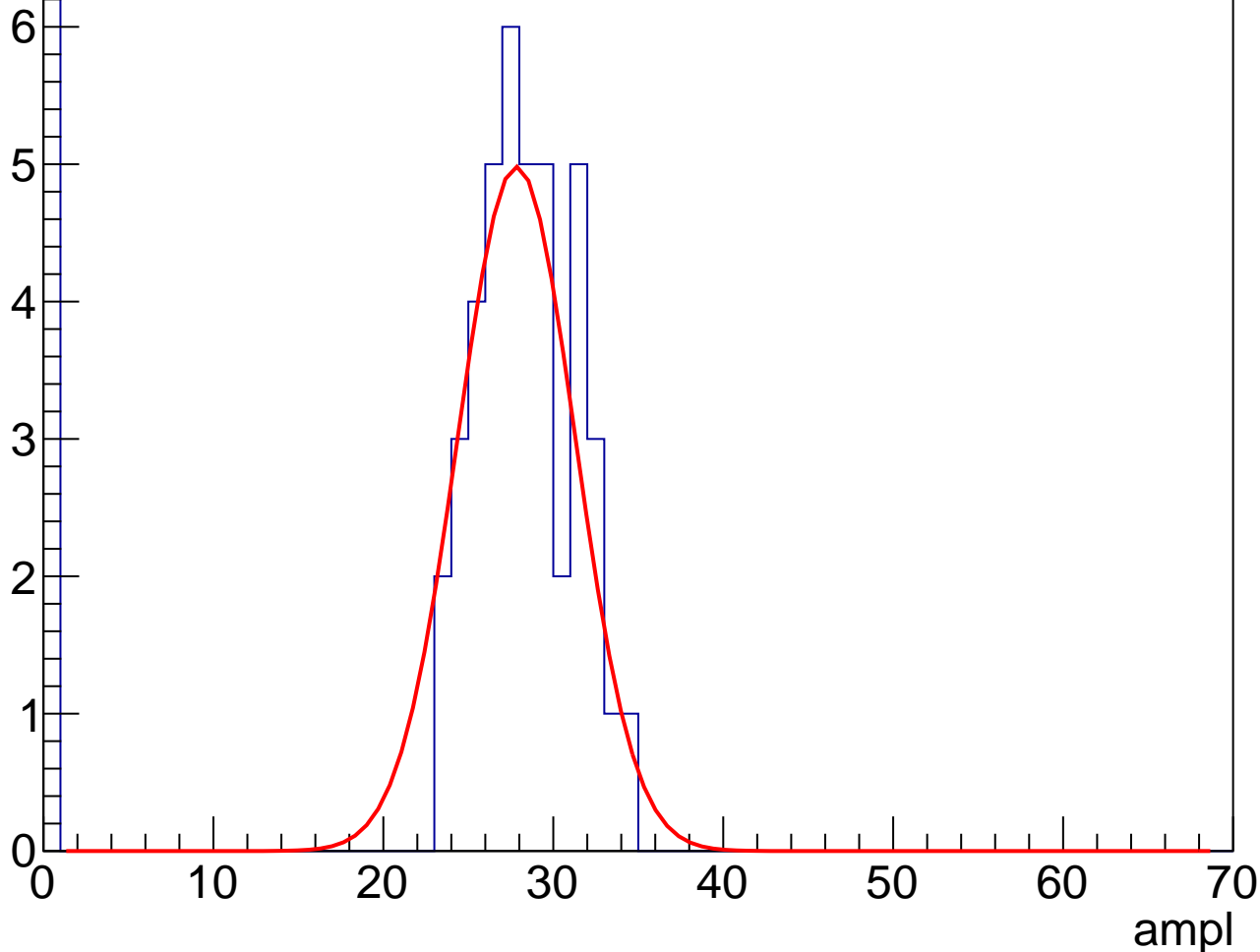
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	50
Mean	23.46
Std Dev	10.55

**Gaus mean : 27.8382**

**Gaus Width: 3.4473**



# B1L103S, U26-ch101, adc1

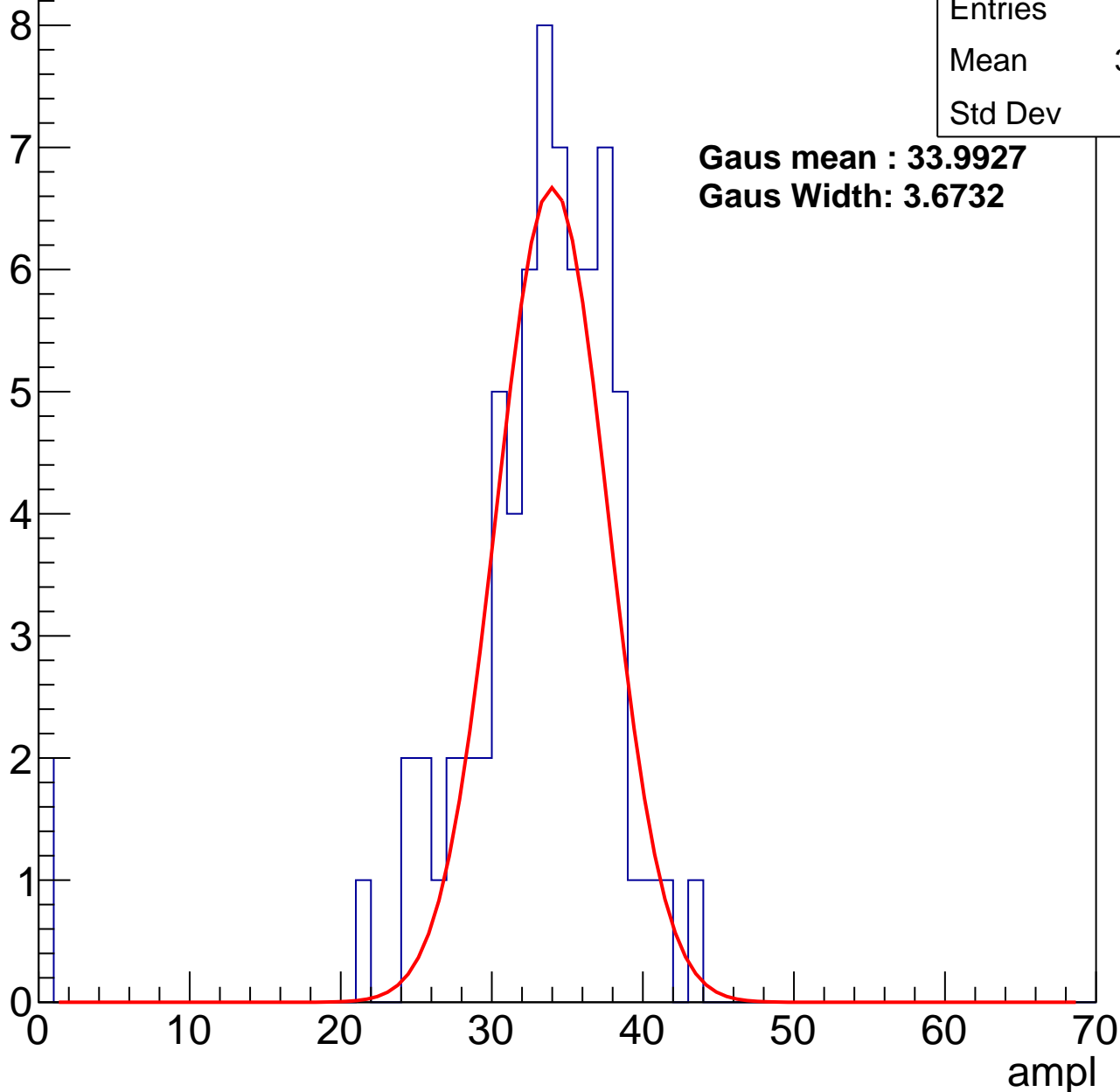
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	72
Mean	32.21
Std Dev	6.88

**Gaus mean : 33.9927**

**Gaus Width: 3.6732**



# B1L103S, U26-ch101, adc2

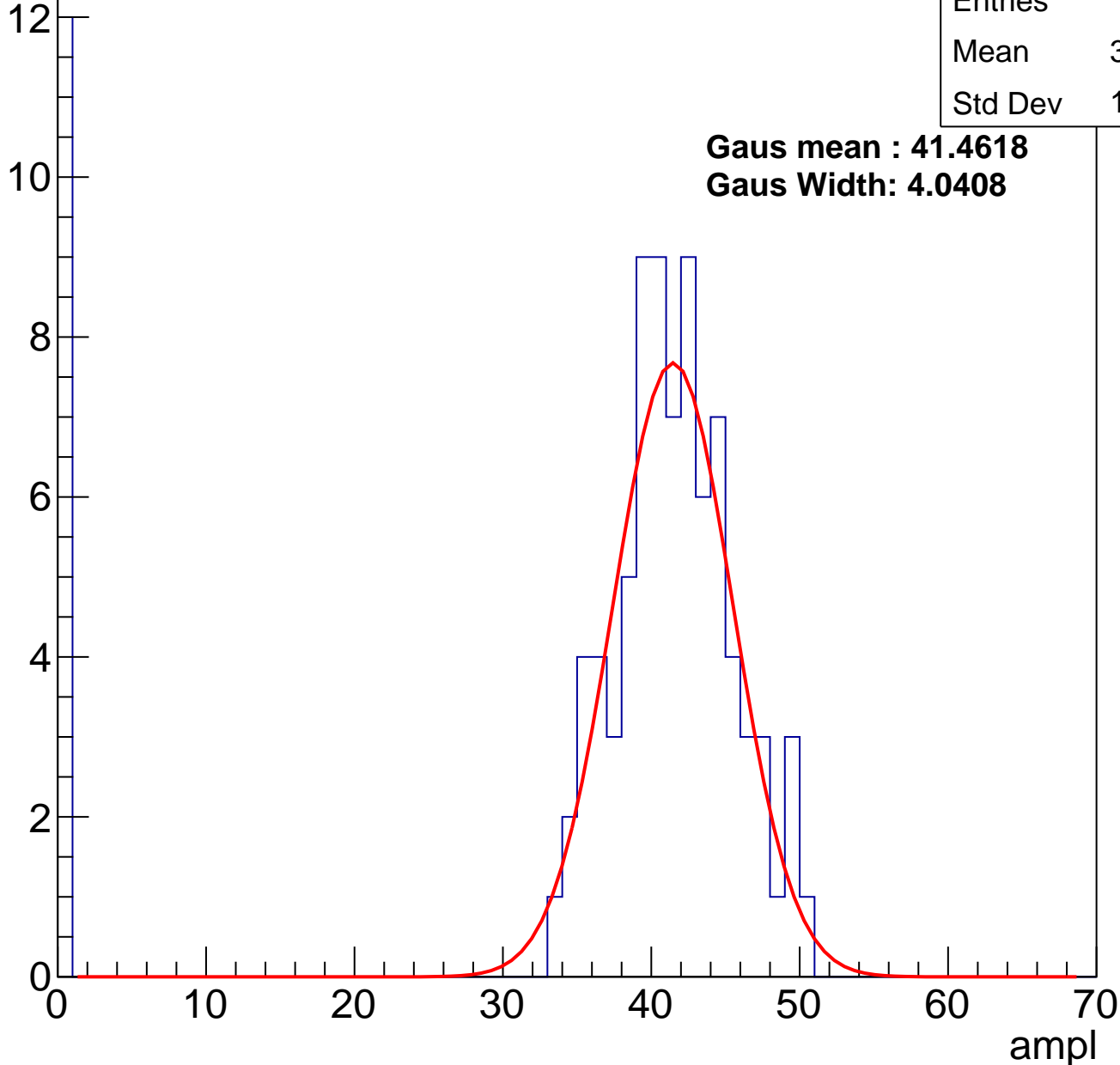
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	93
Mean	35.83
Std Dev	14.25

**Gaus mean : 41.4618**

**Gaus Width: 4.0408**

Entry

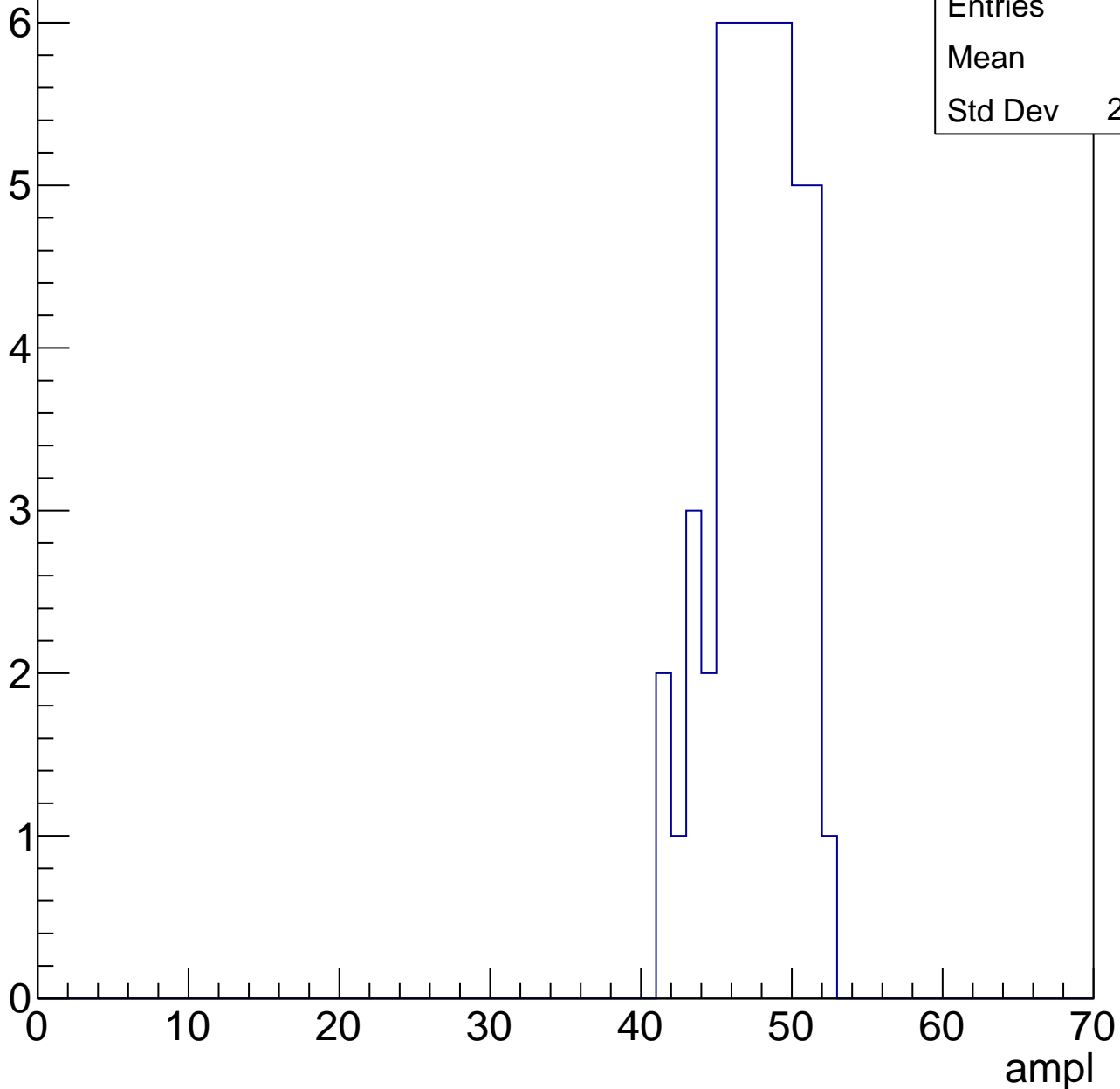


# B1L103S, U26-ch101, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	49
Mean	47.1
Std Dev	2.757



# B1L103S, U26-ch101, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

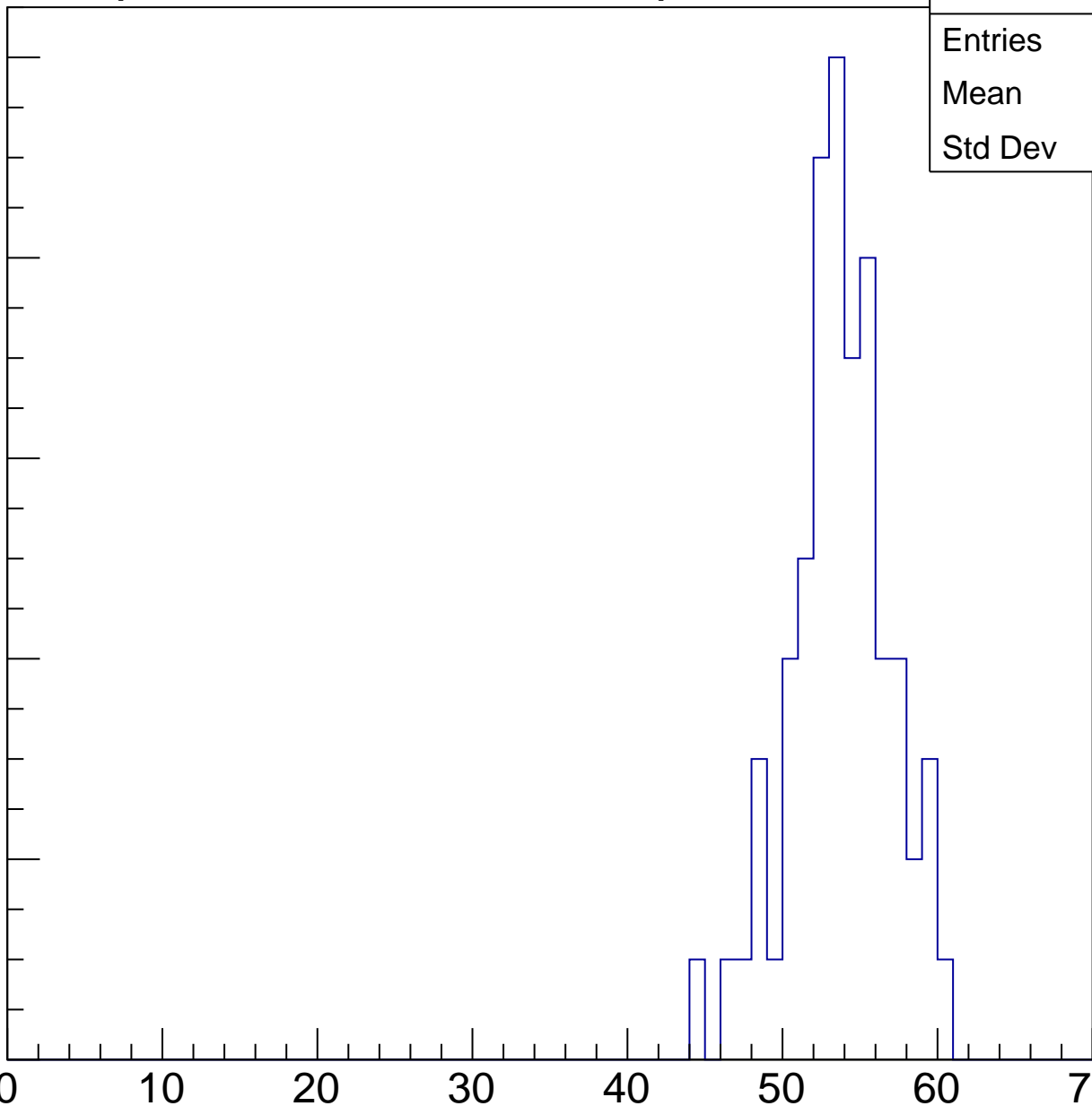
Entries	64
Mean	53.22
Std Dev	3.223

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

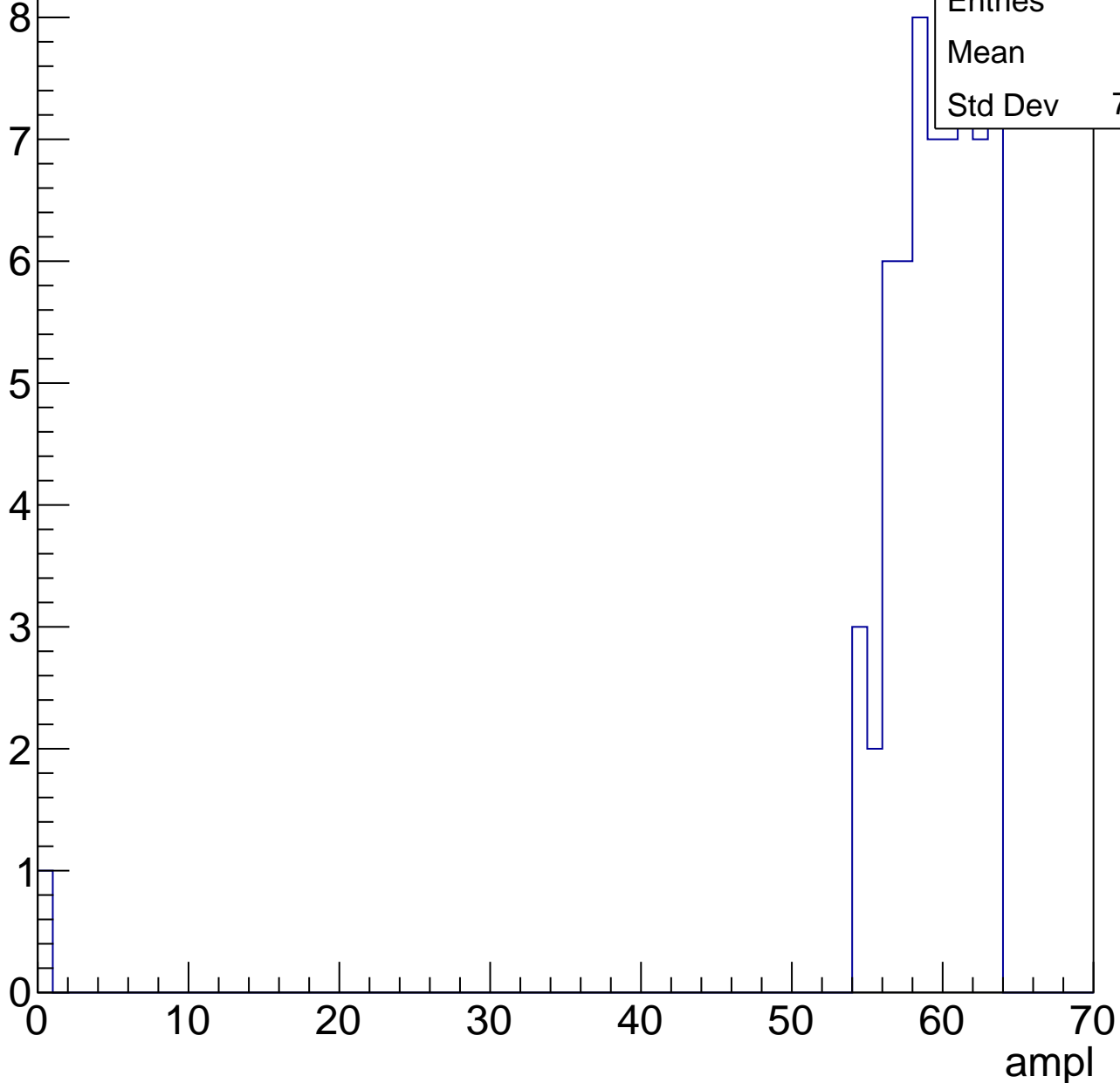


# B1L103S, U26-ch101, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

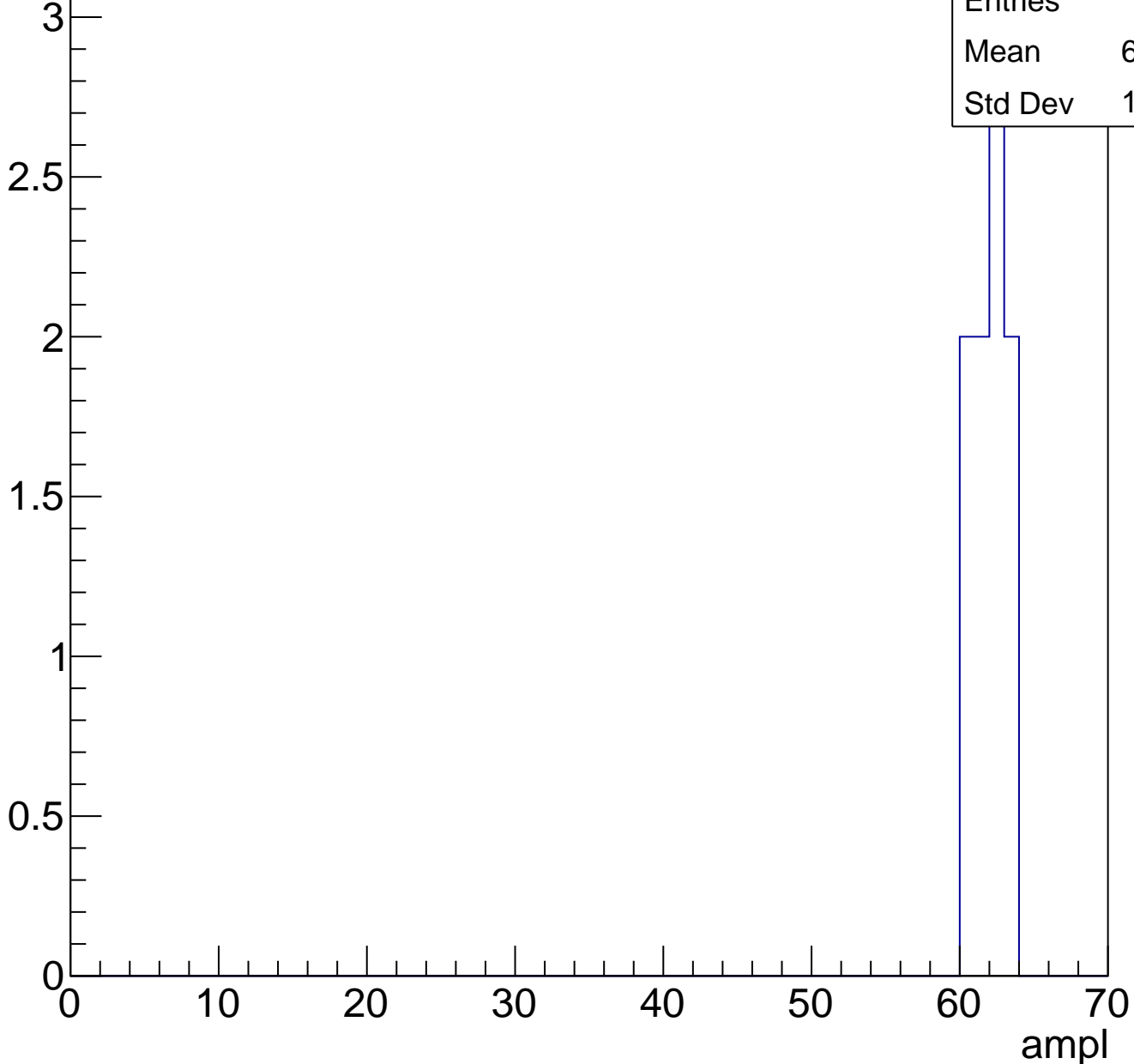
Entries	63
Mean	58.3
Std Dev	7.841



# B1L103S, U26-ch101, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



Entries	9
Mean	61.56
Std Dev	1.066



# B1L103S, U26-ch101, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



# B1L103S, U26-ch102, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	71
Mean	22.27
Std Dev	12.4

**Gaus mean : 29.4083**

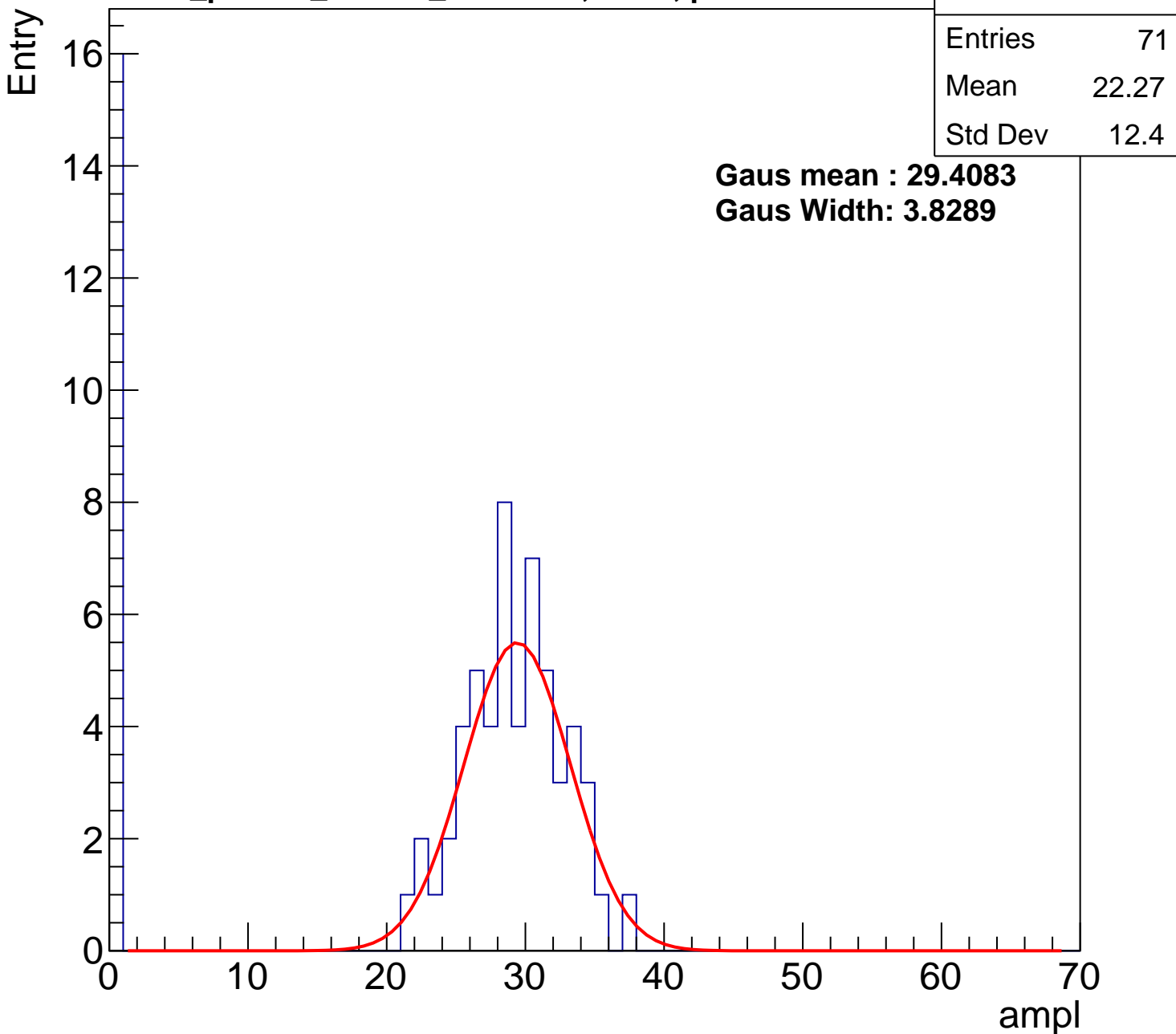
**Gaus Width: 3.8289**

Entry

16  
14  
12  
10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U26-ch102, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	82
Mean	34.5
Std Dev	5.538

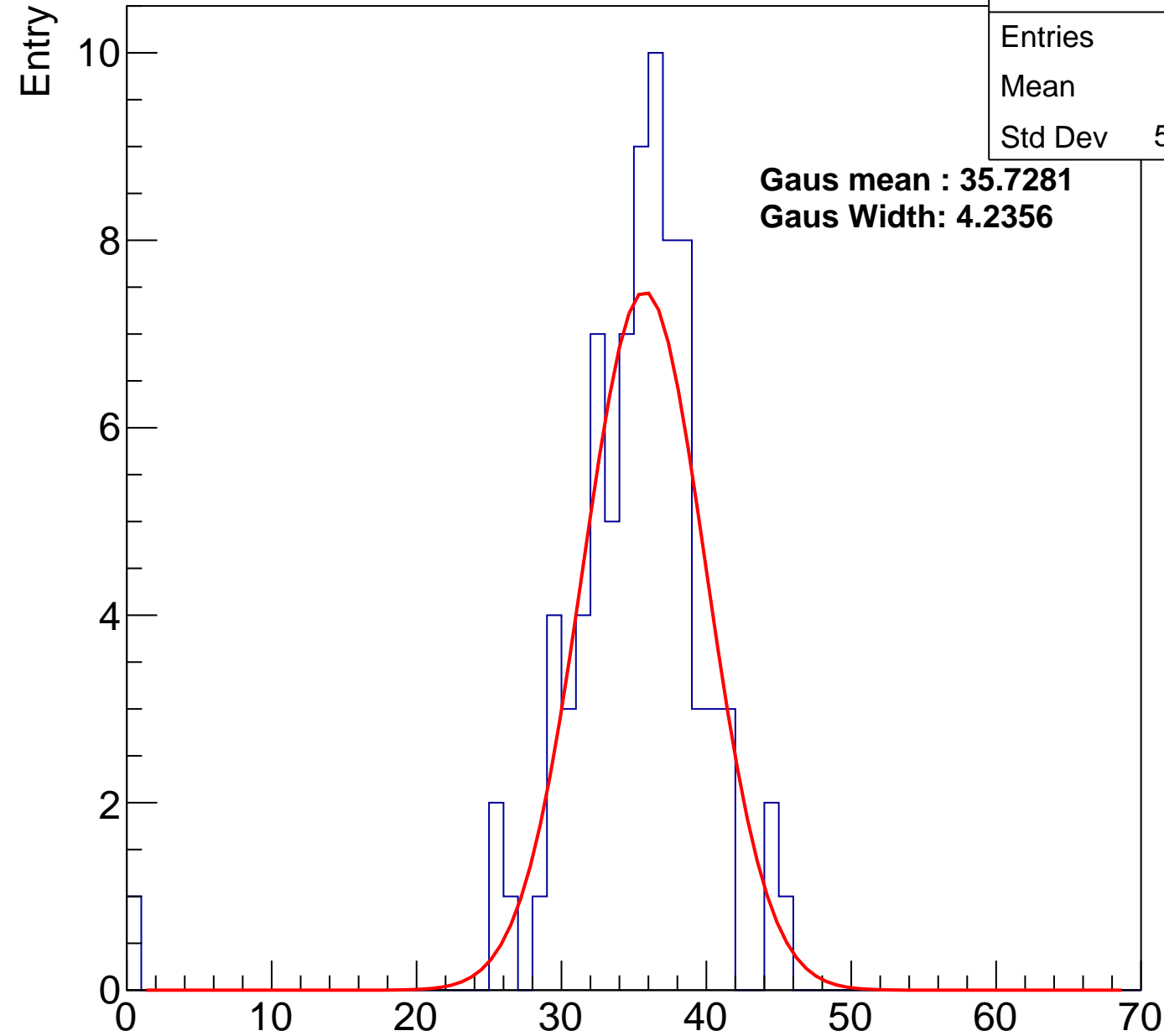
**Gaus mean : 35.7281**

**Gaus Width: 4.2356**

Entry

10  
8  
6  
4  
2  
0

ampl



# B1L103S, U26-ch102, adc2

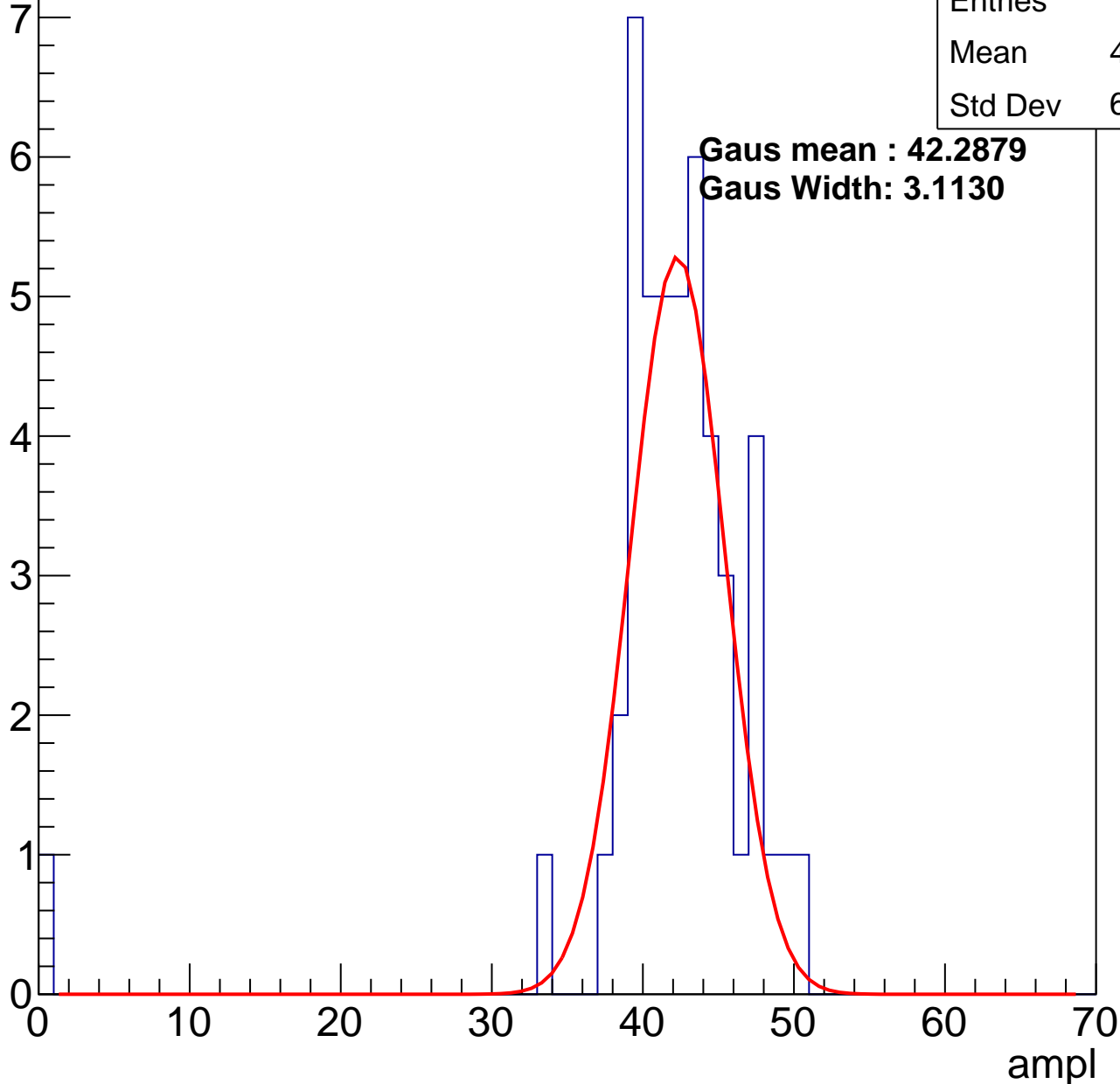
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	48
Mean	41.33
Std Dev	6.896

**Gaus mean : 42.2879**

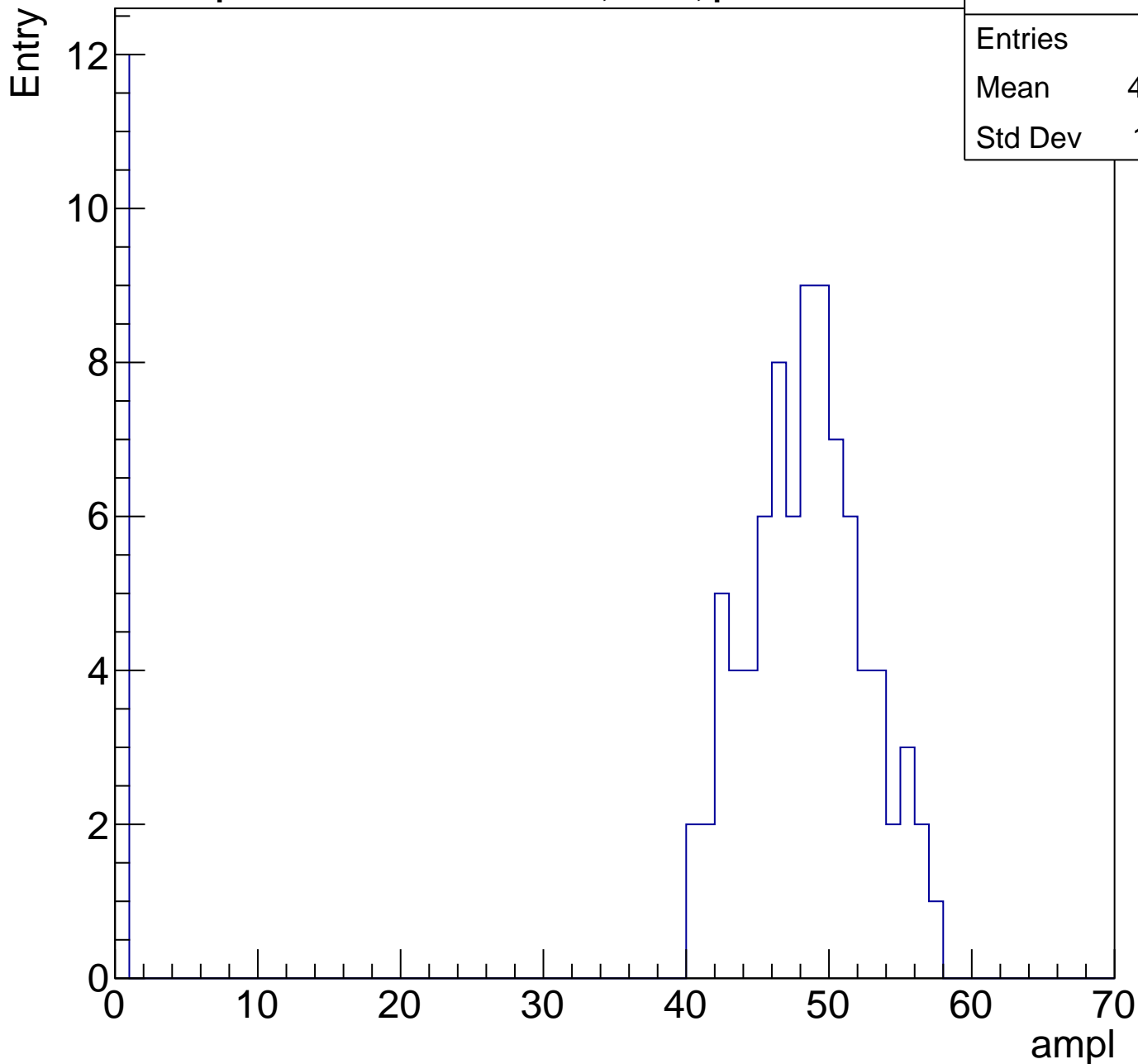
**Gaus Width: 3.1130**



# B1L103S, U26-ch102, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	96
Mean	41.99
Std Dev	16.31

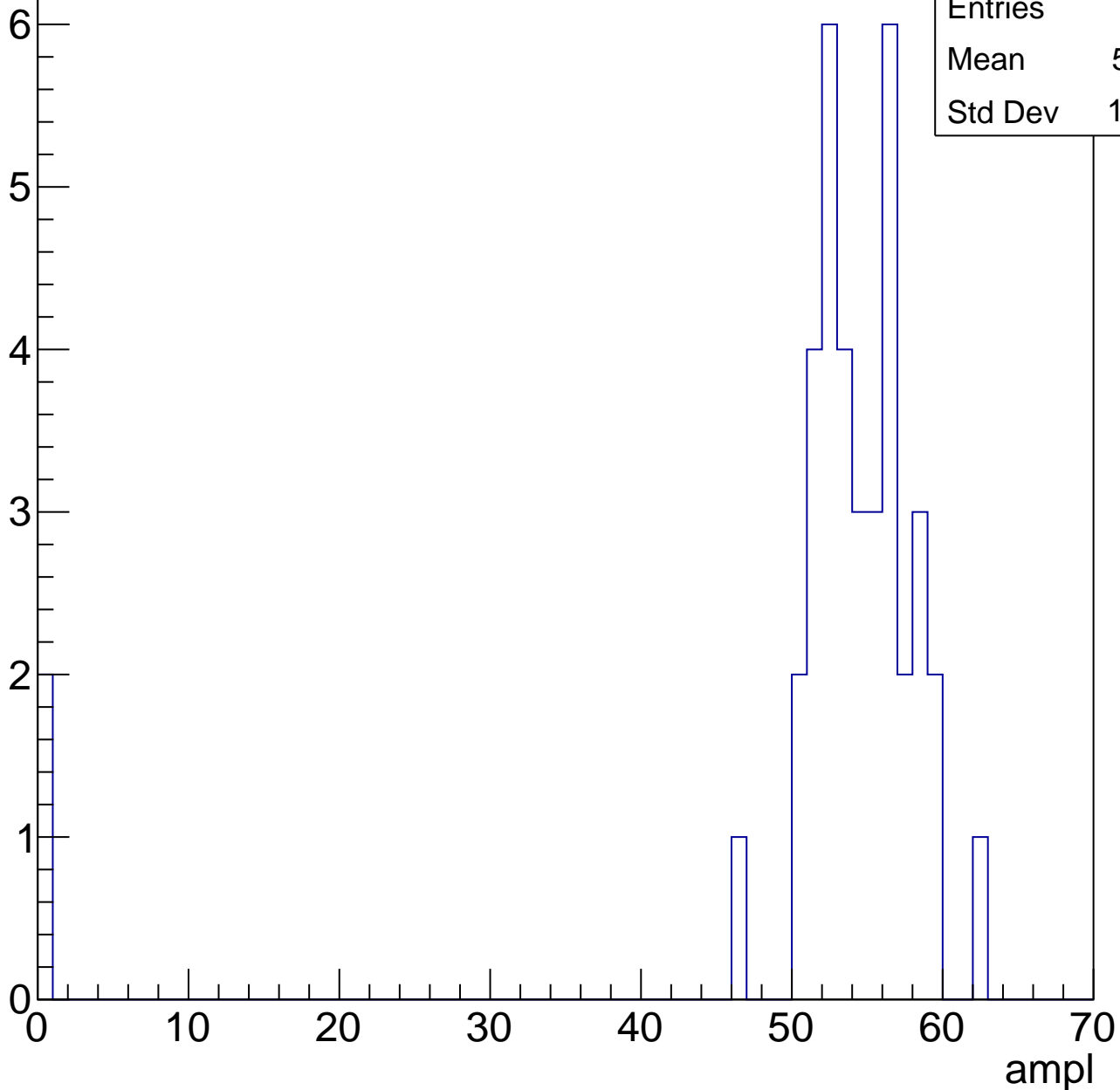


# B1L103S, U26-ch102, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

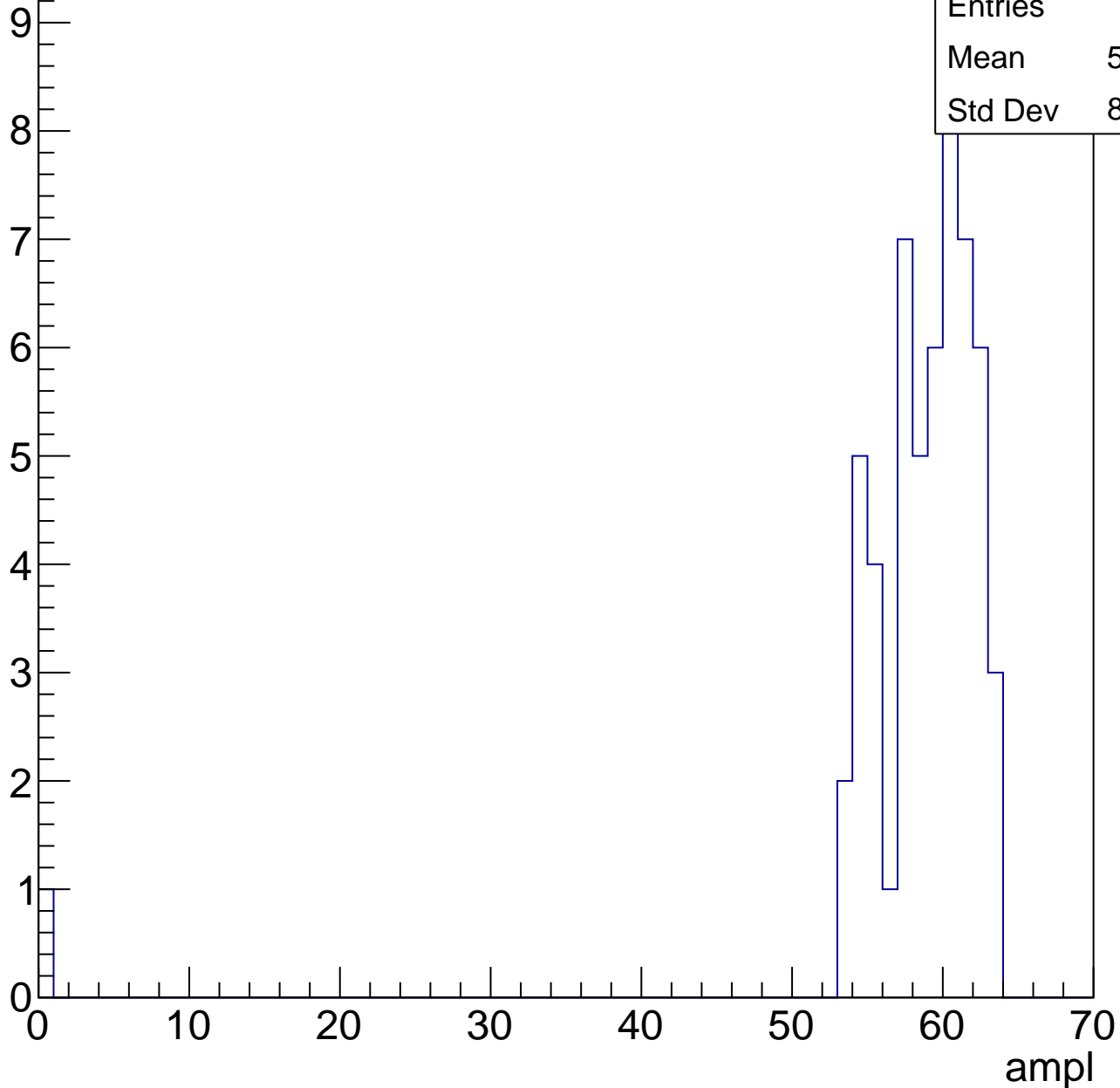
Entries	39
Mean	51.41
Std Dev	12.34



# B1L103S, U26-ch102, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



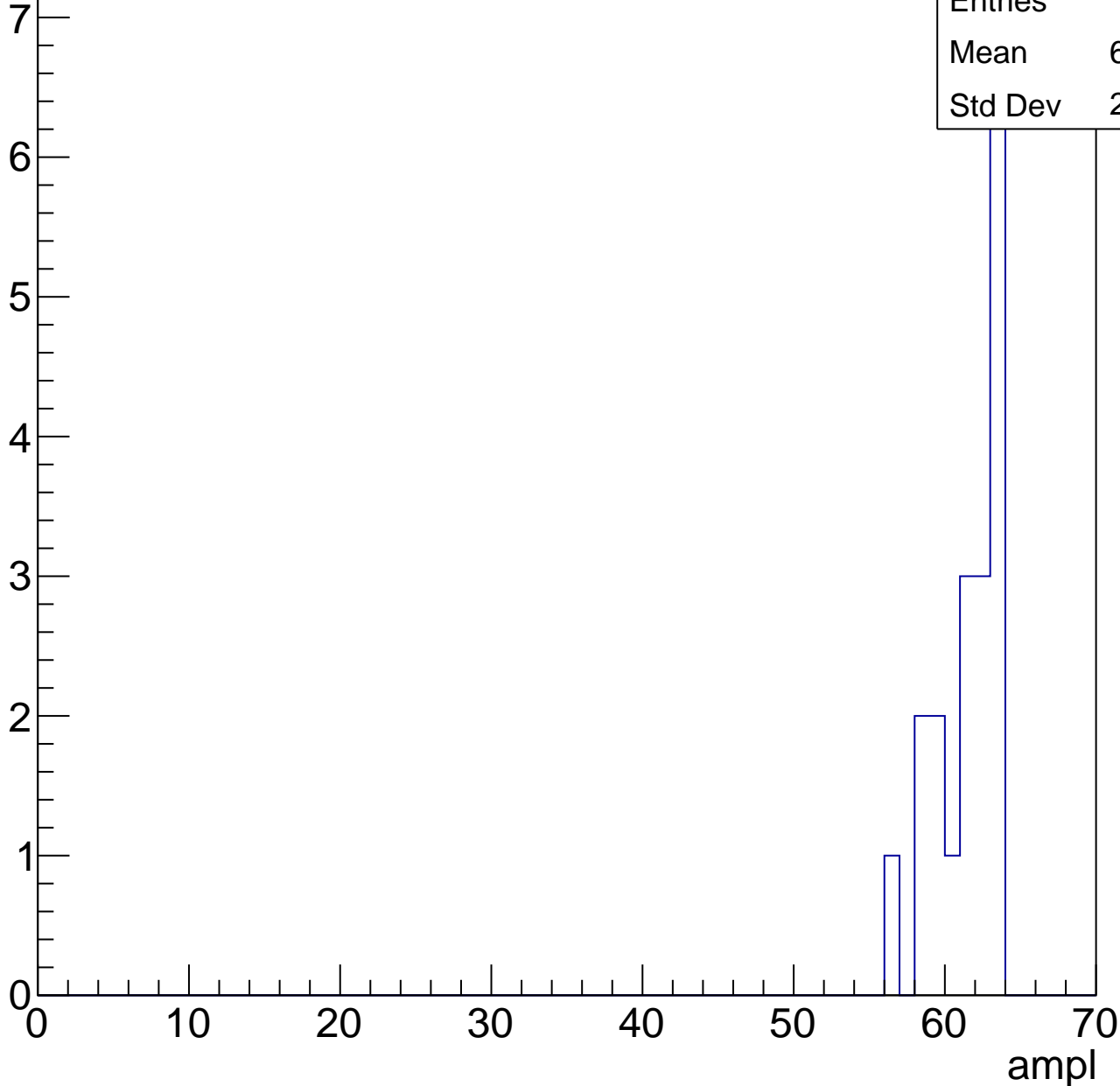
Entries	56
Mean	57.55
Std Dev	8.244

# B1L103S, U26-ch102, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	19
Mean	61.05
Std Dev	2.089





# B1L103S, U26-ch102, adc7

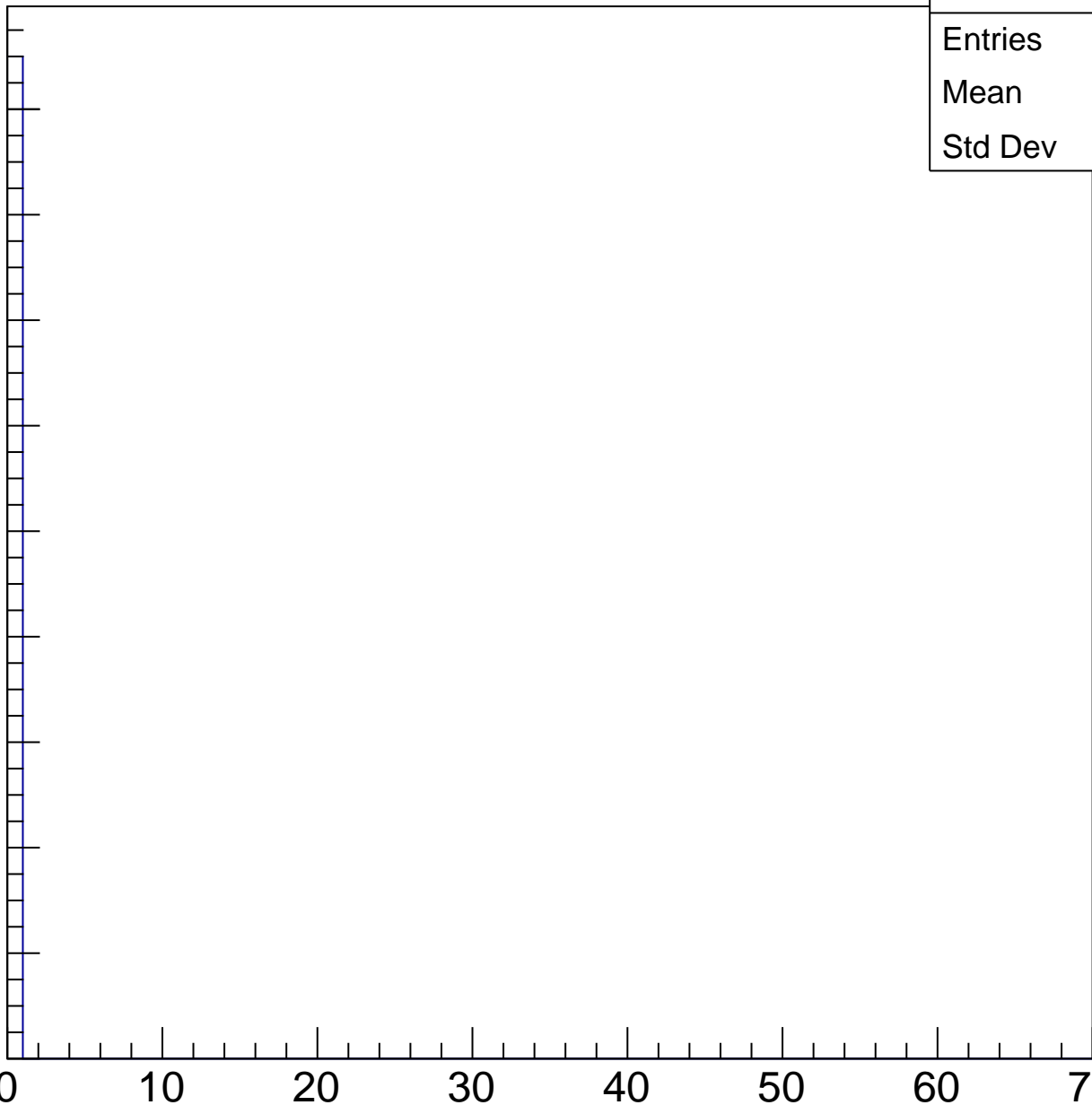
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

18  
16  
14  
12  
10  
8  
6  
4  
2  
0

Entries	19
Mean	0
Std Dev	0

ampl



# B1L103S, U26-ch103, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	72
Mean	24.94
Std Dev	9.276

**Gaus mean : 28.7399**

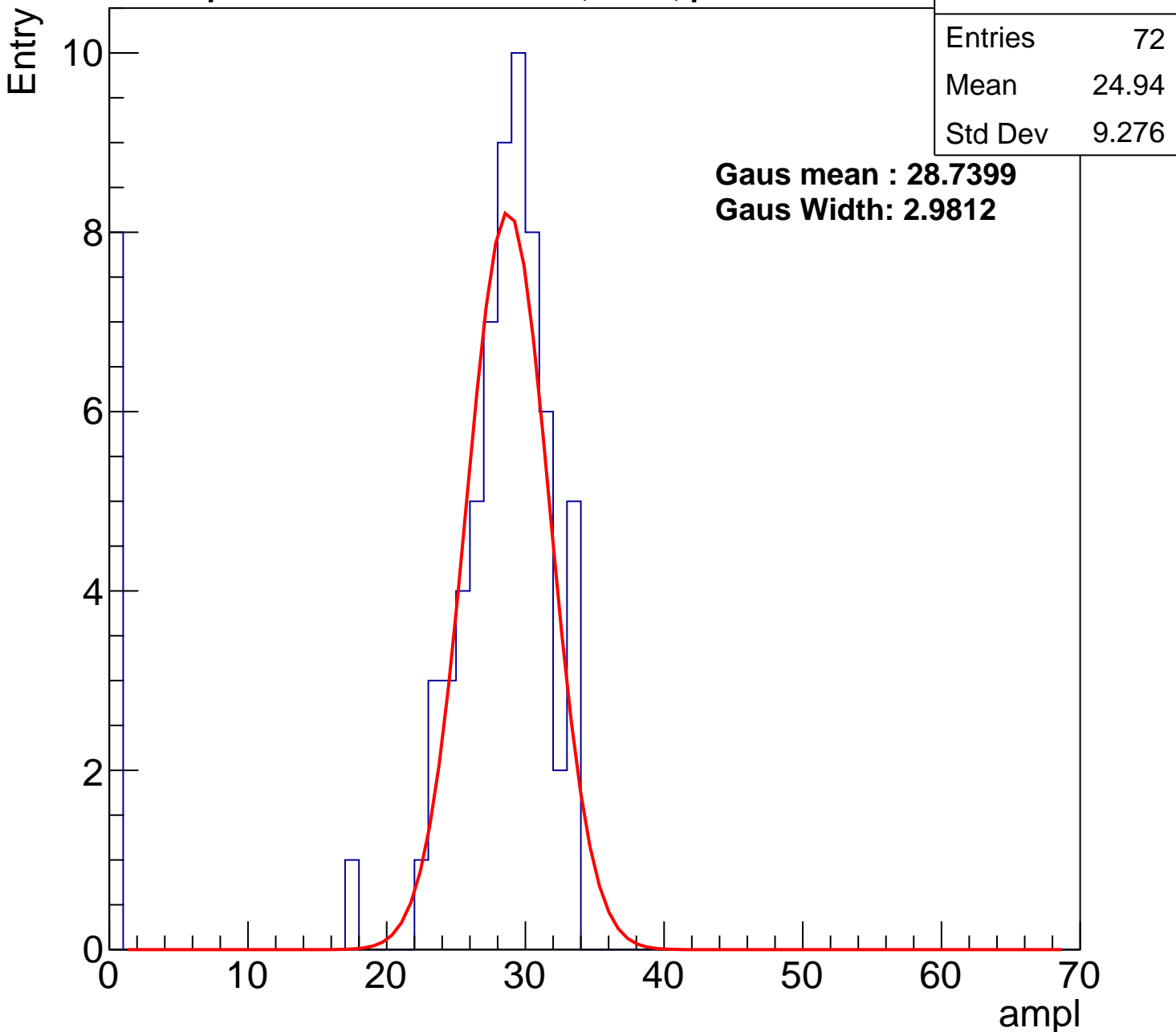
**Gaus Width: 2.9812**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U26-ch103, adc1

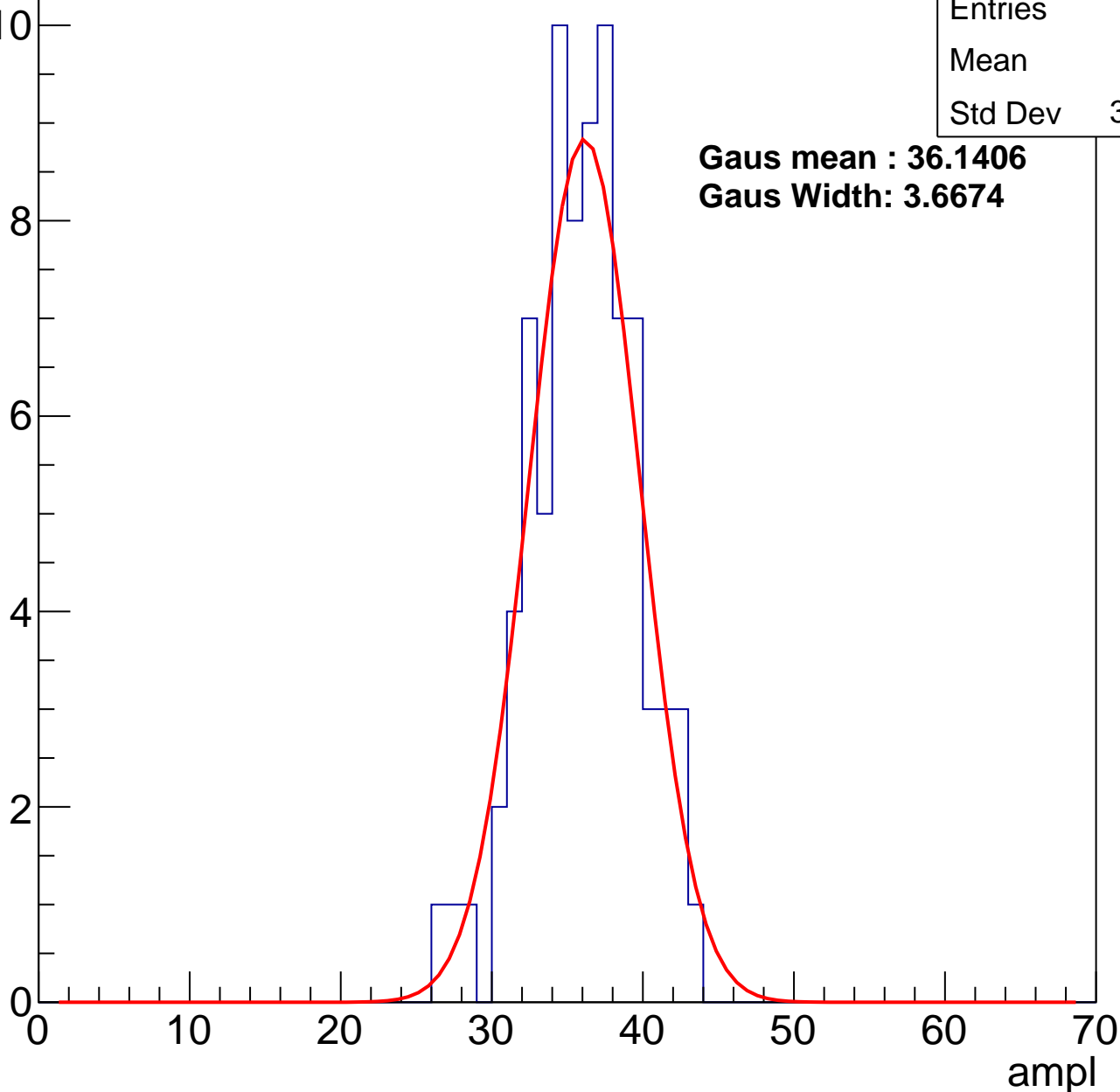
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	82
Mean	35.6
Std Dev	3.474

**Gaus mean : 36.1406**

**Gaus Width: 3.6674**



# B1L103S, U26-ch103, adc2

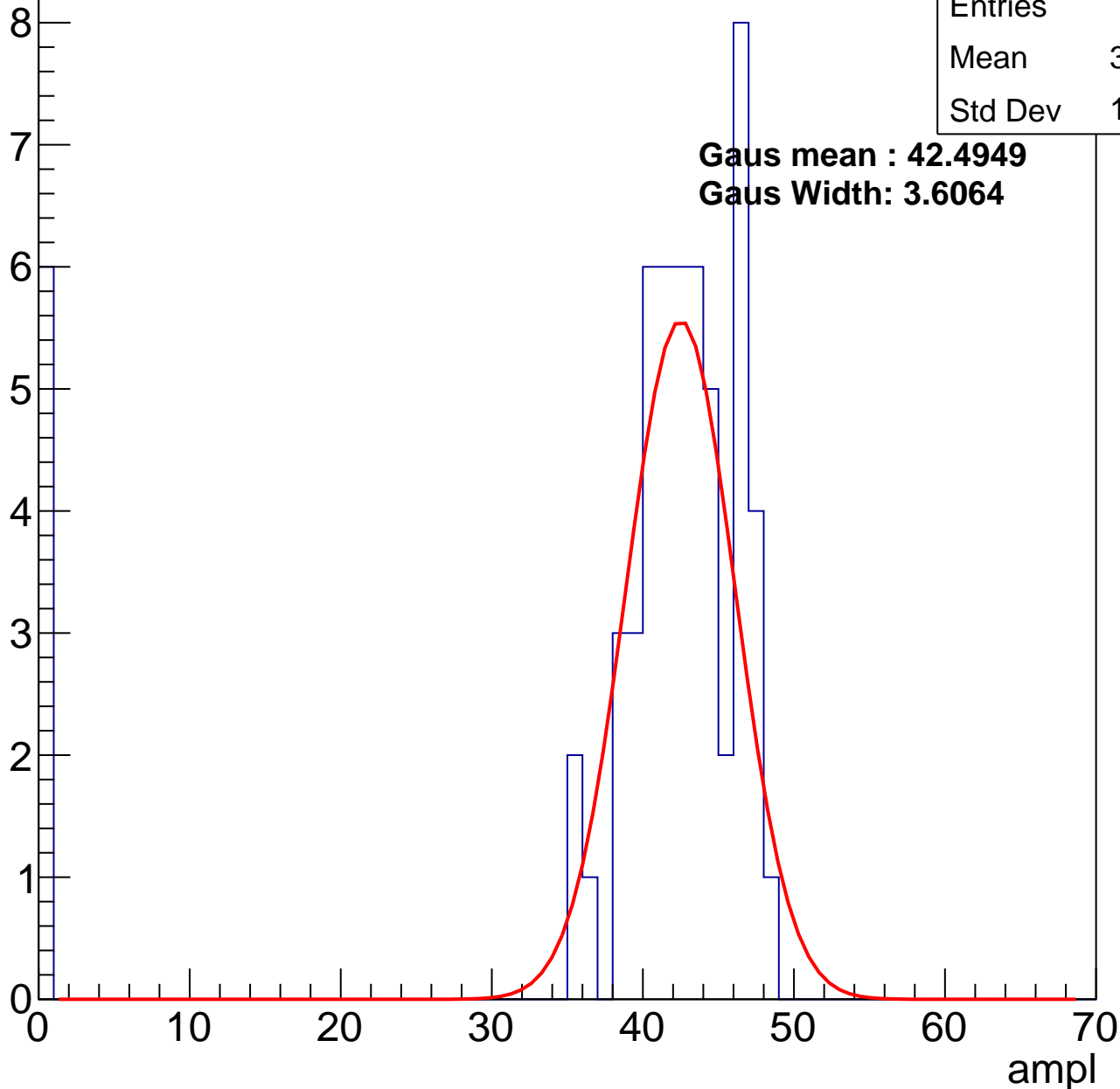
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	59
Mean	38.08
Std Dev	13.17

**Gaus mean : 42.4949**

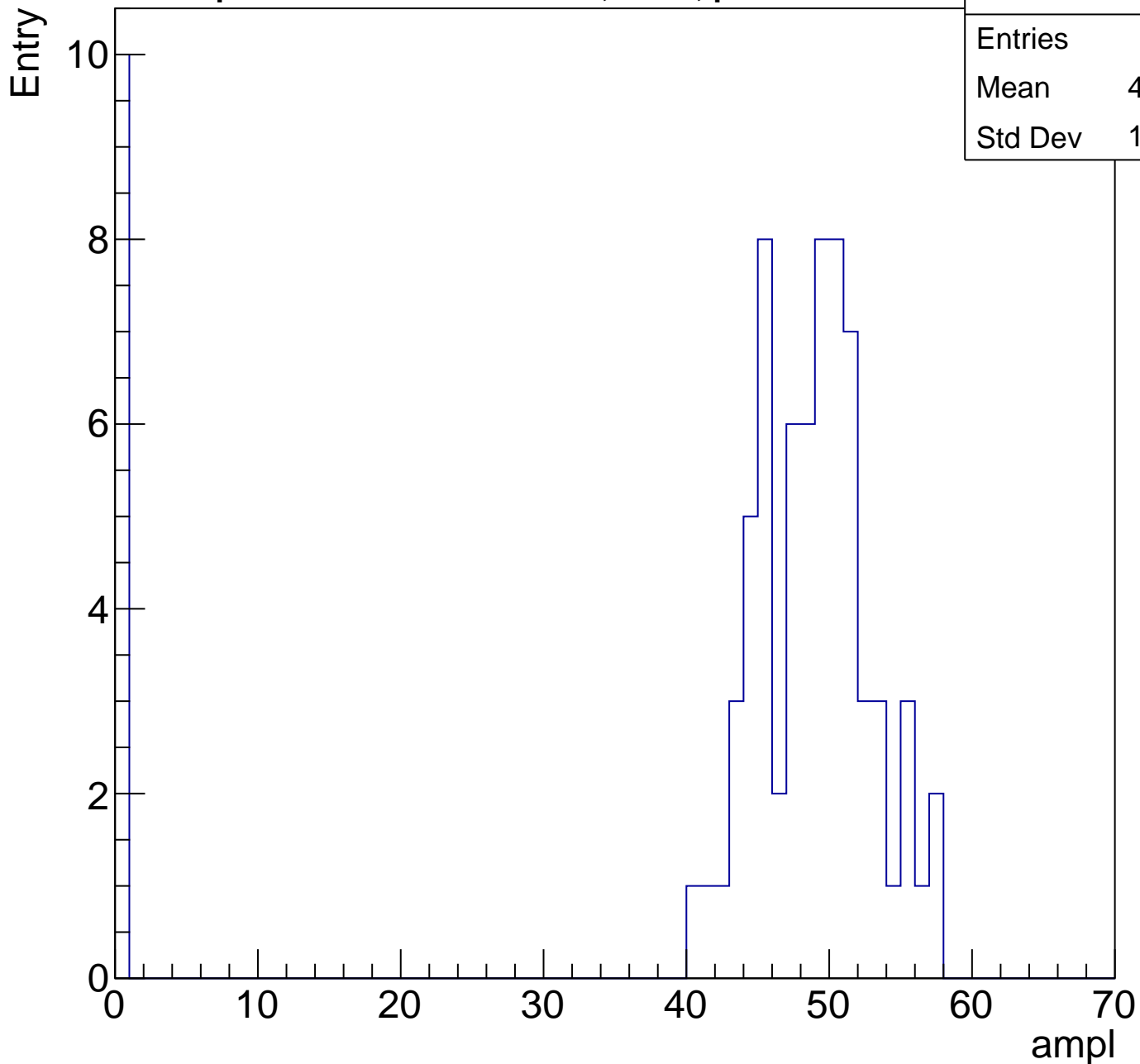
**Gaus Width: 3.6064**



# B1L103S, U26-ch103, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	79
Mean	42.37
Std Dev	16.52

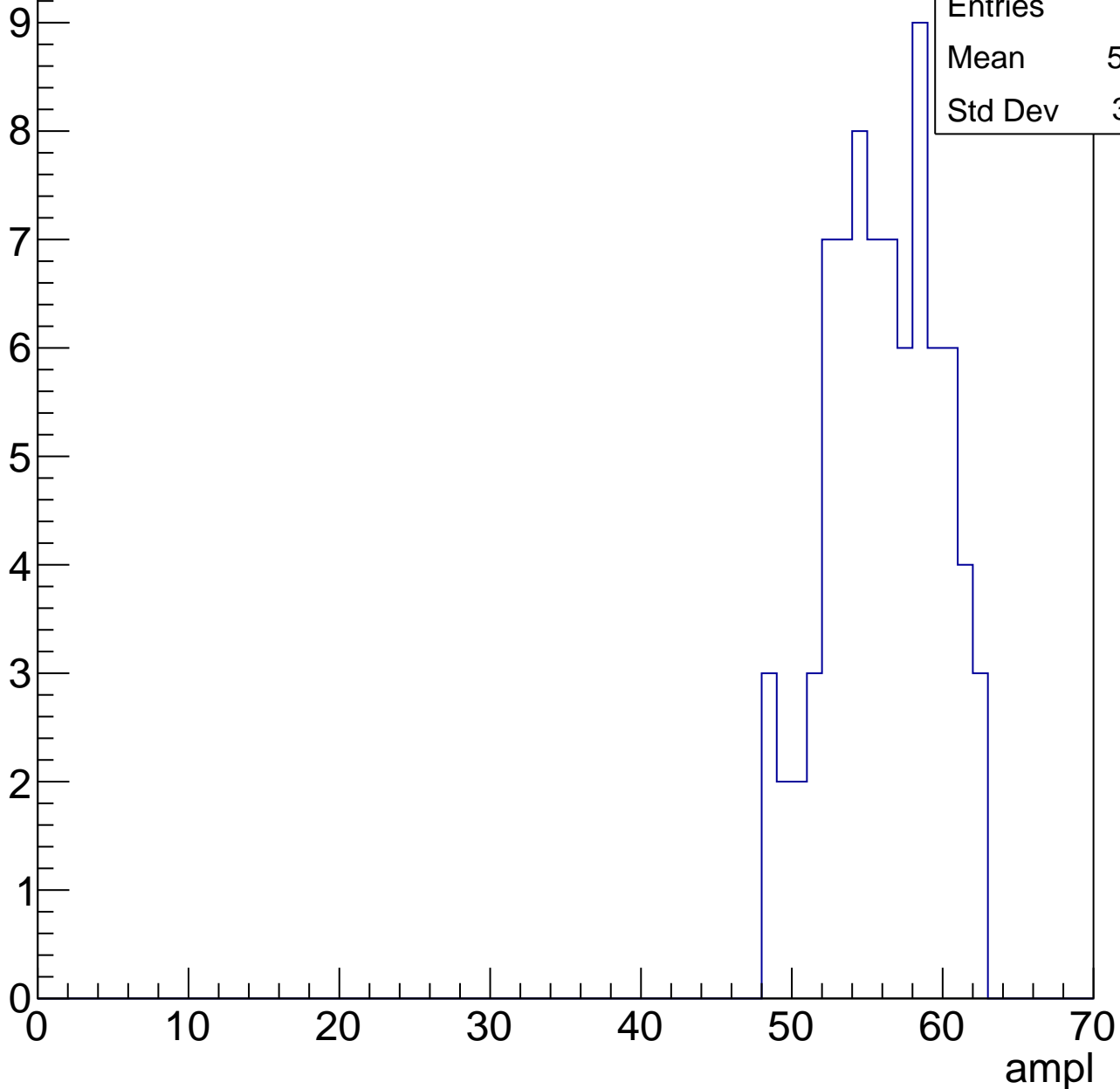


# B1L103S, U26-ch103, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	80
Mean	55.59
Std Dev	3.601

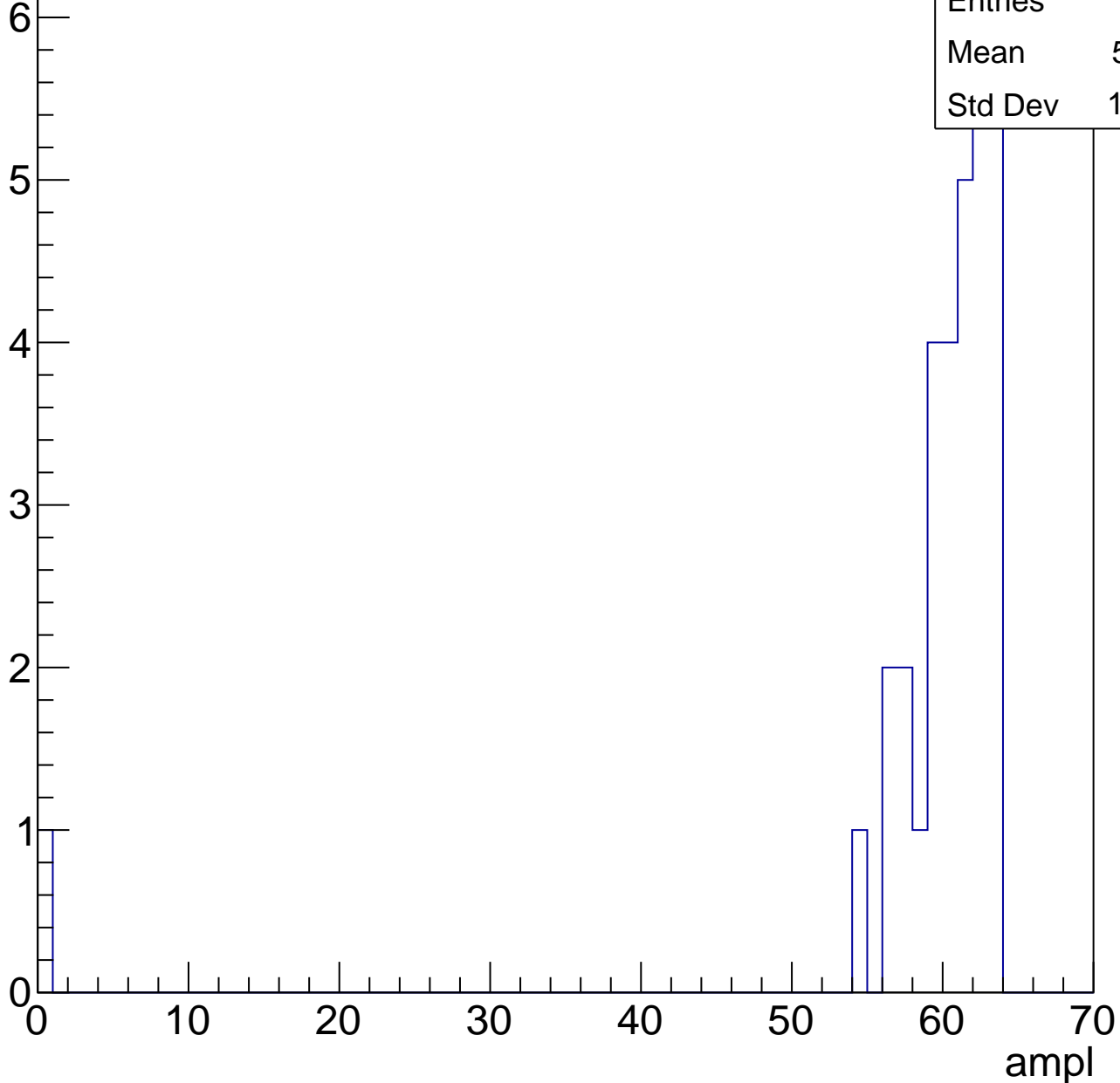


# B1L103S, U26-ch103, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	32
Mean	58.41
Std Dev	10.75



# B1L103S, U26-ch103, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



Entries	6
Mean	62.5
Std Dev	0.7638



# B1L103S, U26-ch103, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

16  
14  
12  
10  
8  
6  
4  
2  
0

Entries	17
Mean	0
Std Dev	0

ampl

# B1L103S, U26-ch104, adc0

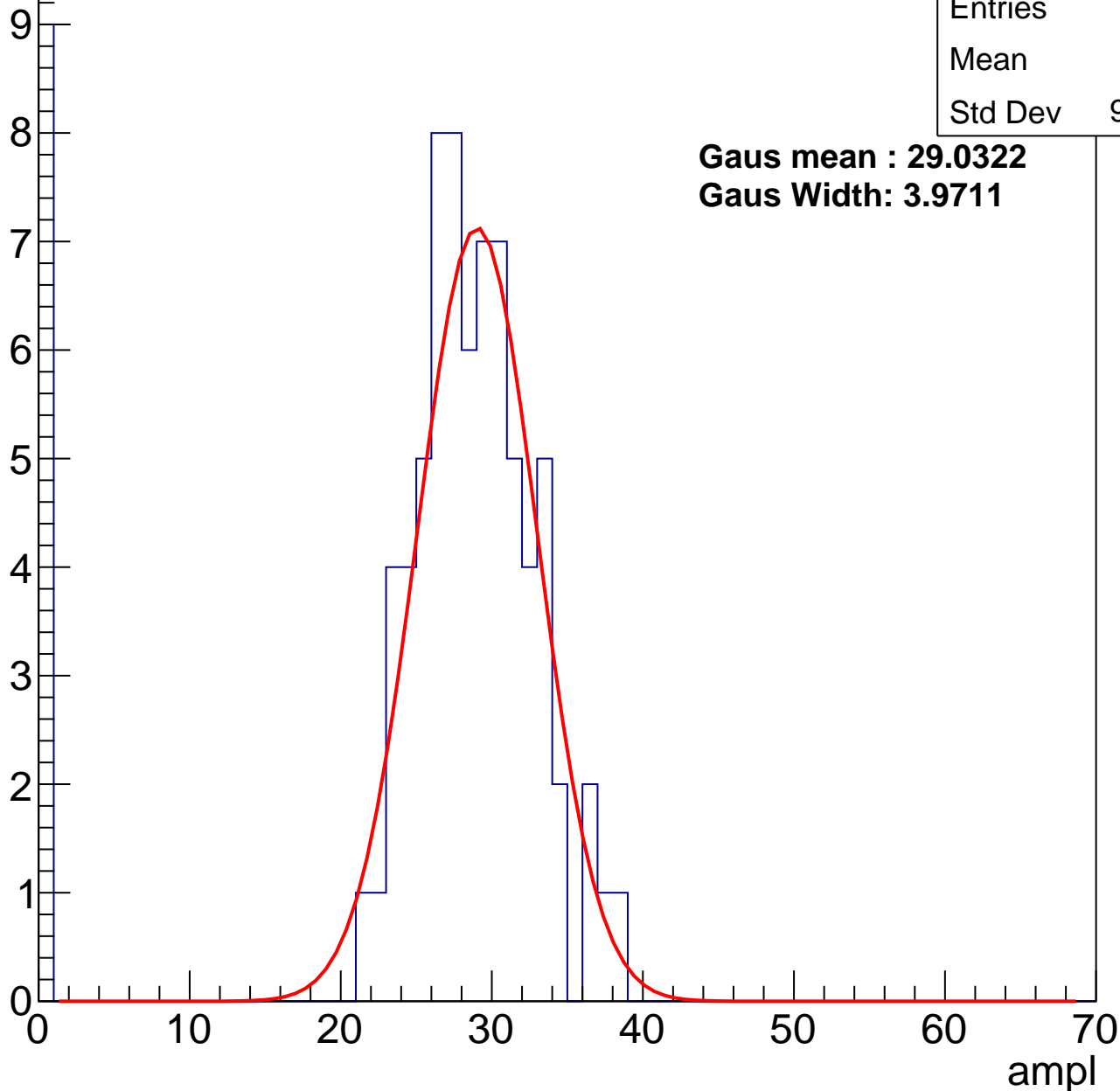
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	80
Mean	25.3
Std Dev	9.655

**Gaus mean : 29.0322**

**Gaus Width: 3.9711**



# B1L103S, U26-ch104, adc1

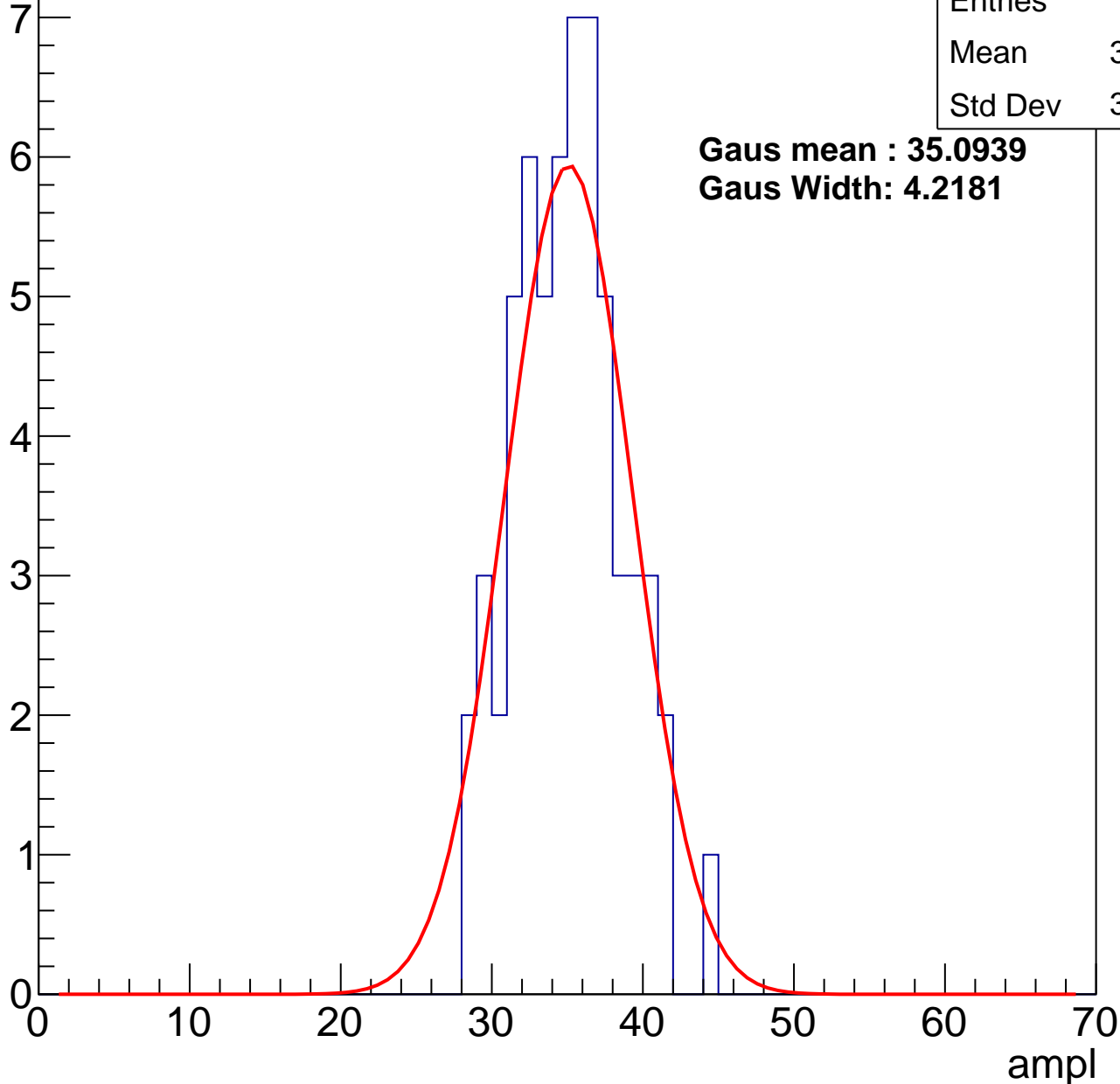
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	60
Mean	34.63
Std Dev	3.507

**Gaus mean : 35.0939**

**Gaus Width: 4.2181**



# B1L103S, U26-ch104, adc2

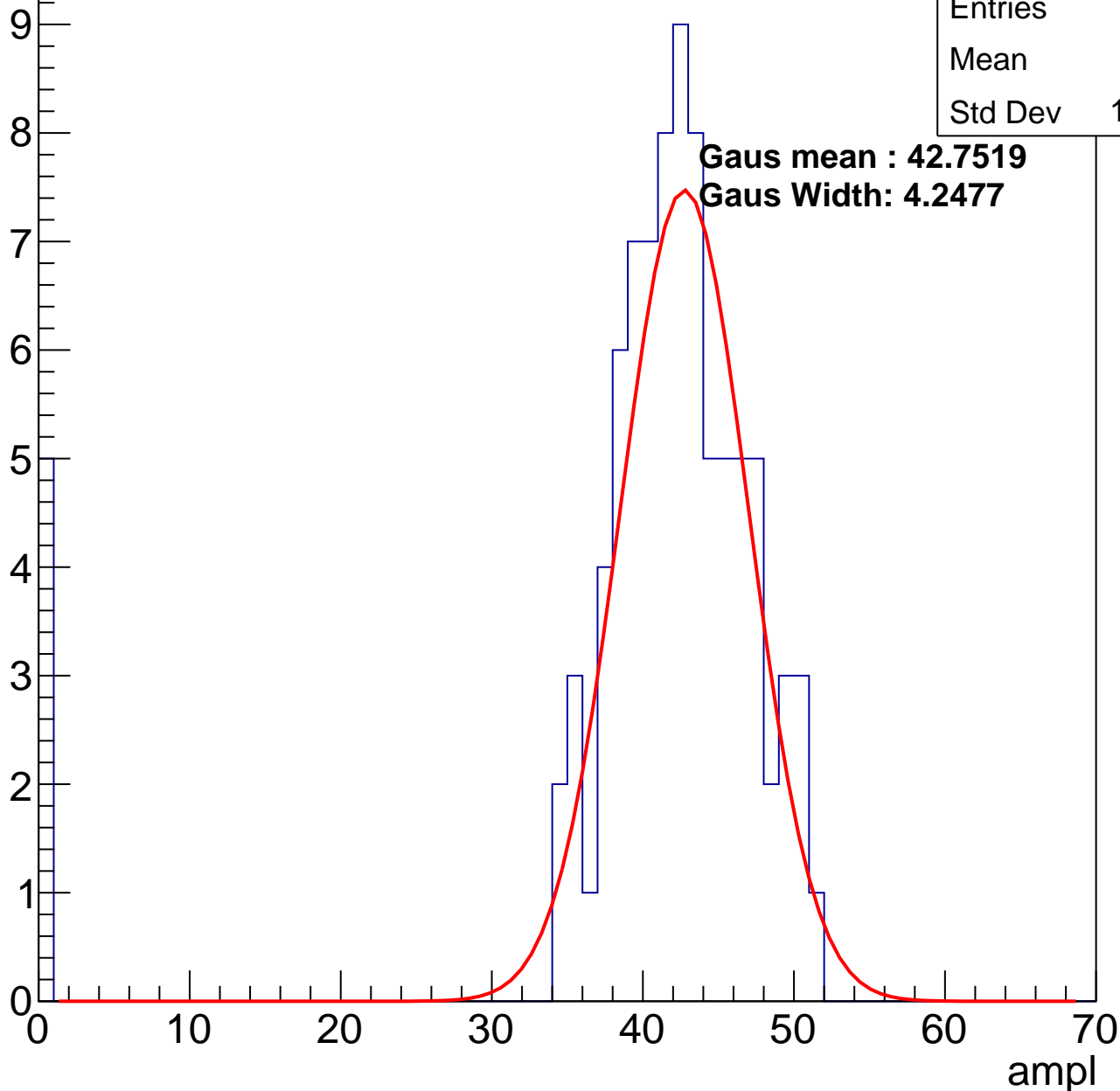
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	89
Mean	39.8
Std Dev	10.47

**Gaus mean : 42.7519**

**Gaus Width: 4.2477**

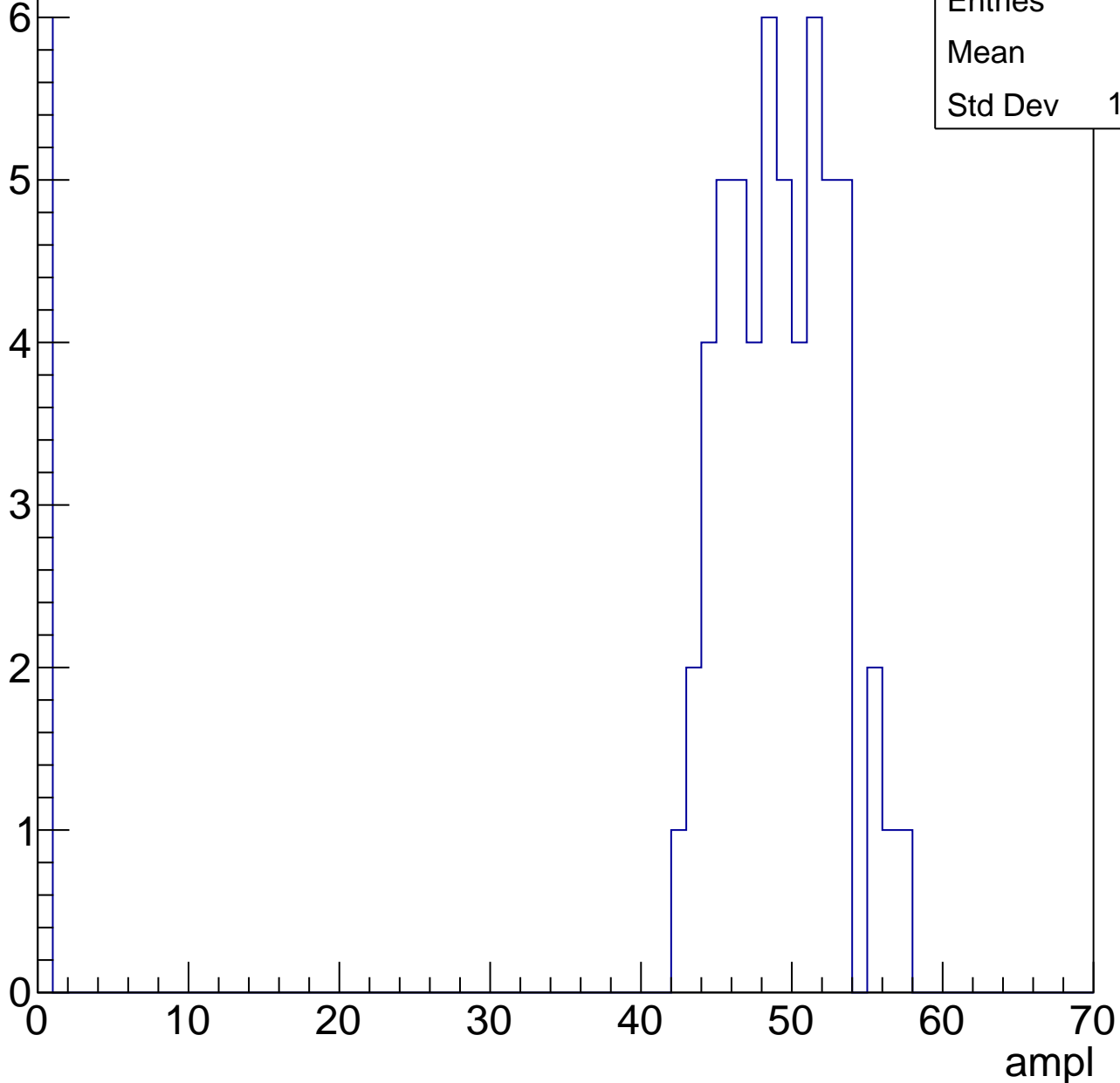


# B1L103S, U26-ch104, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

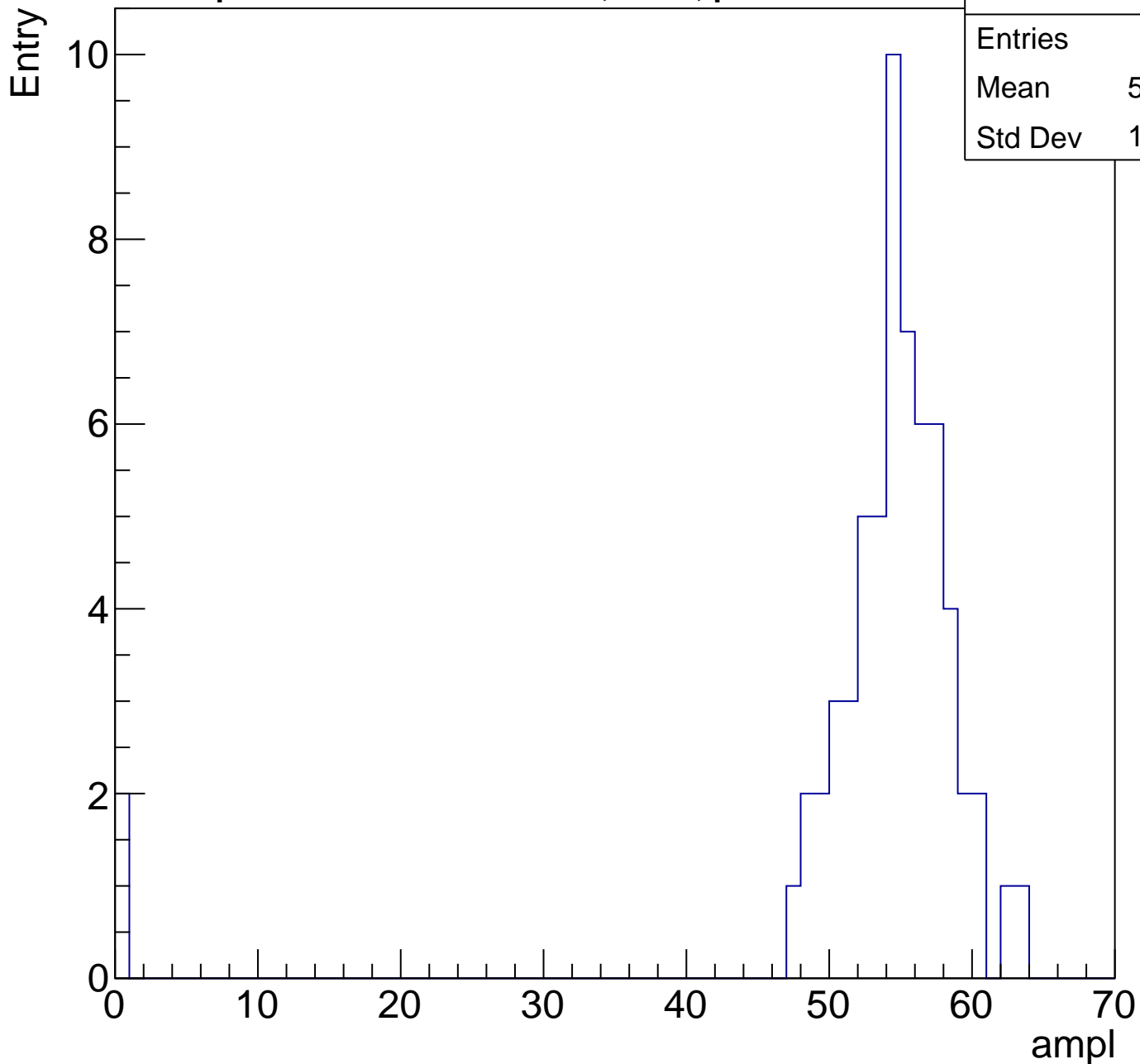
Entries	62
Mean	44.1
Std Dev	14.82



# B1L103S, U26-ch104, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	62
Mean	52.69
Std Dev	10.17

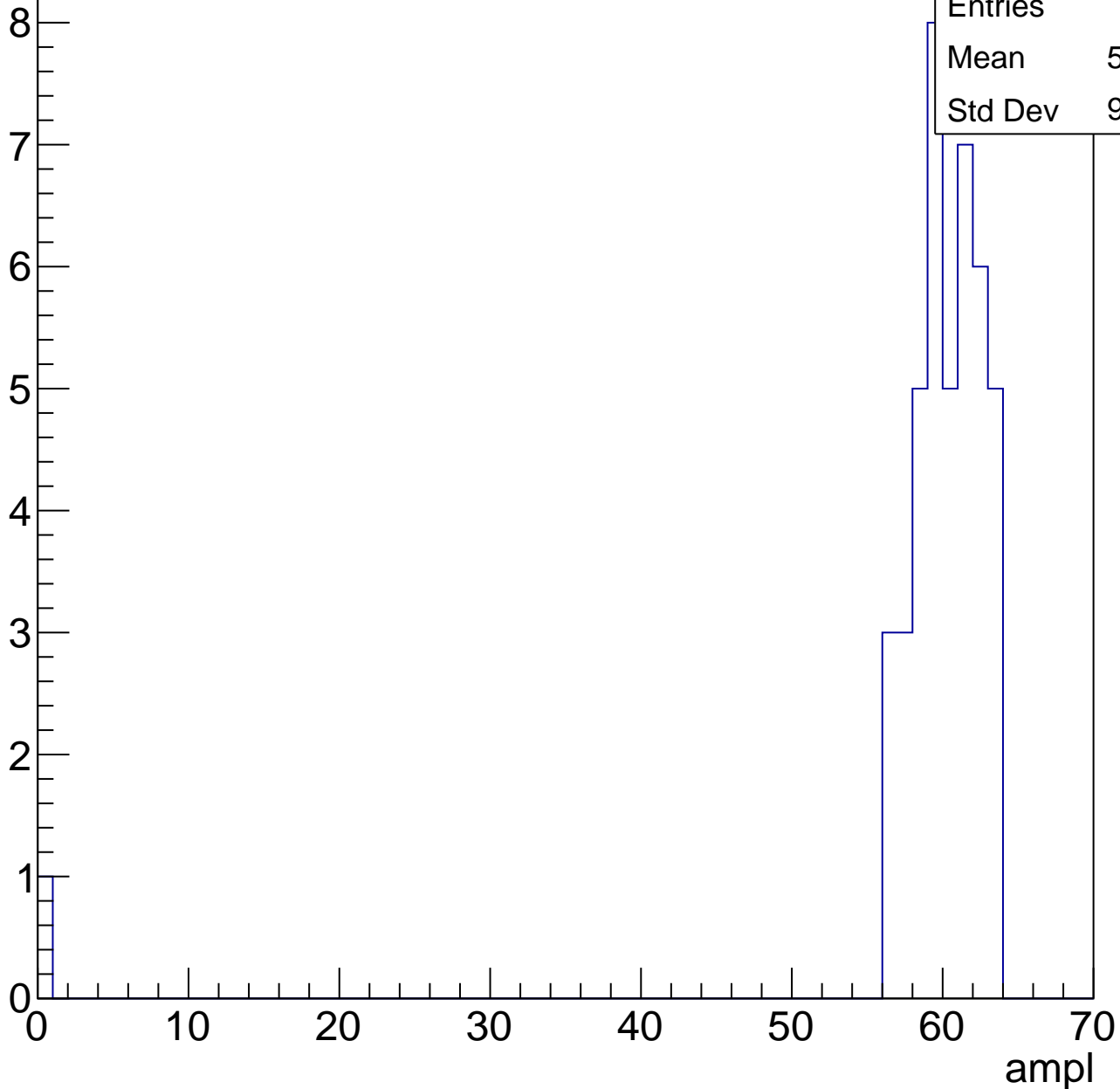


# B1L103S, U26-ch104, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

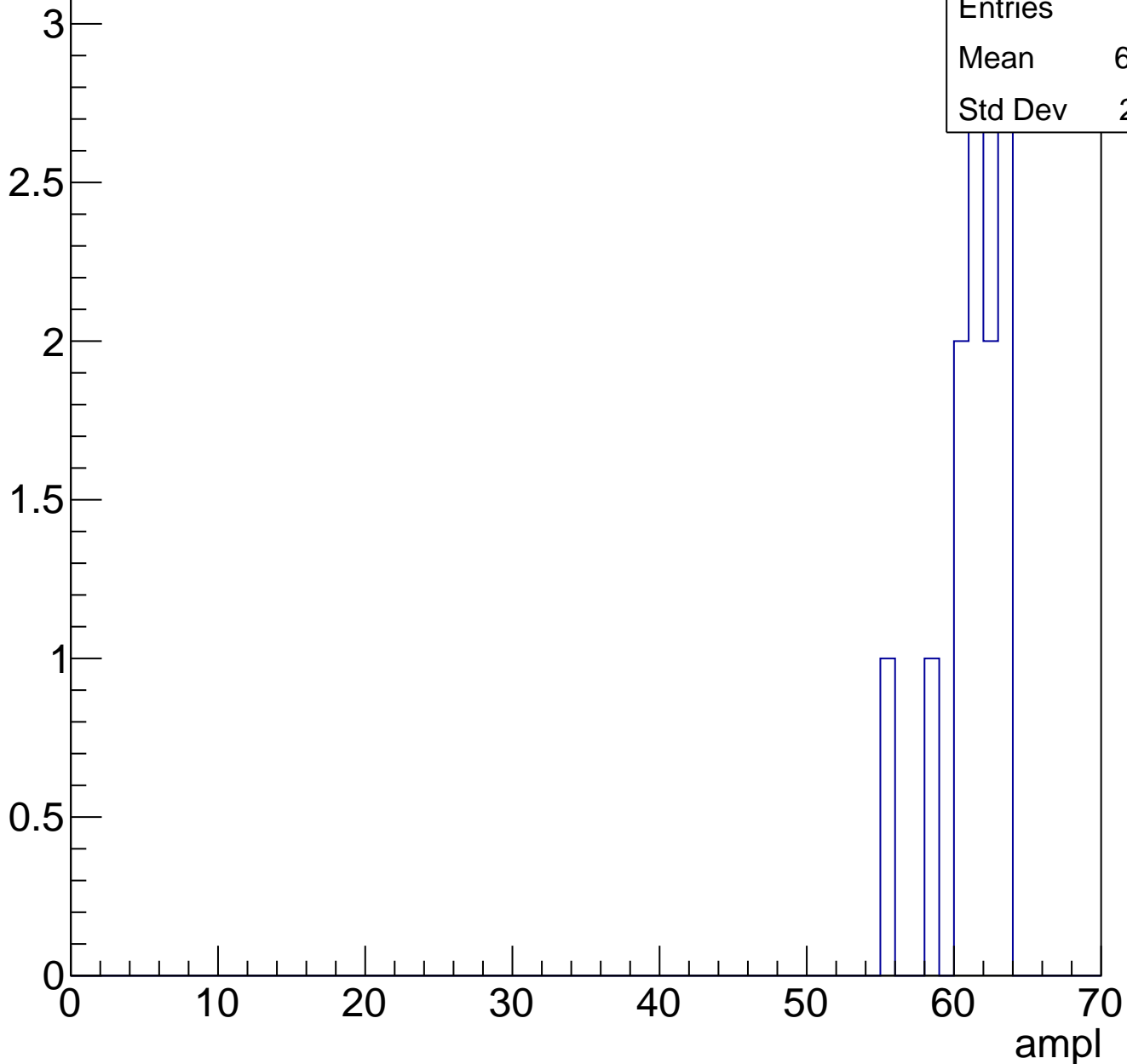
Entries	43
Mean	58.49
Std Dev	9.252



# B1L103S, U26-ch104, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



Entries	12
Mean	60.75
Std Dev	2.241

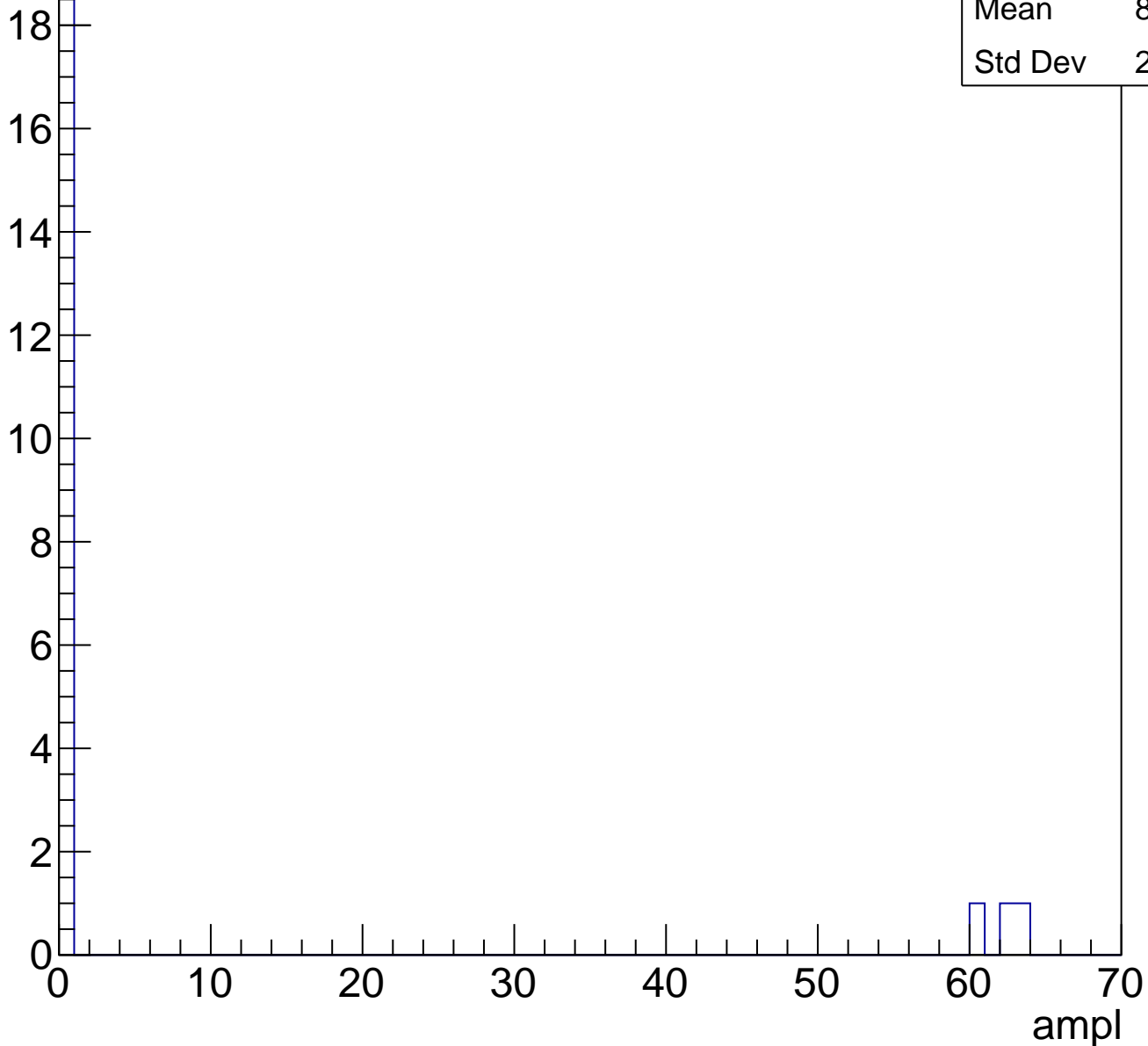


# B1L103S, U26-ch104, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	22
Mean	8.409
Std Dev	21.17

Entry



# B1L103S, U26-ch105, adc0

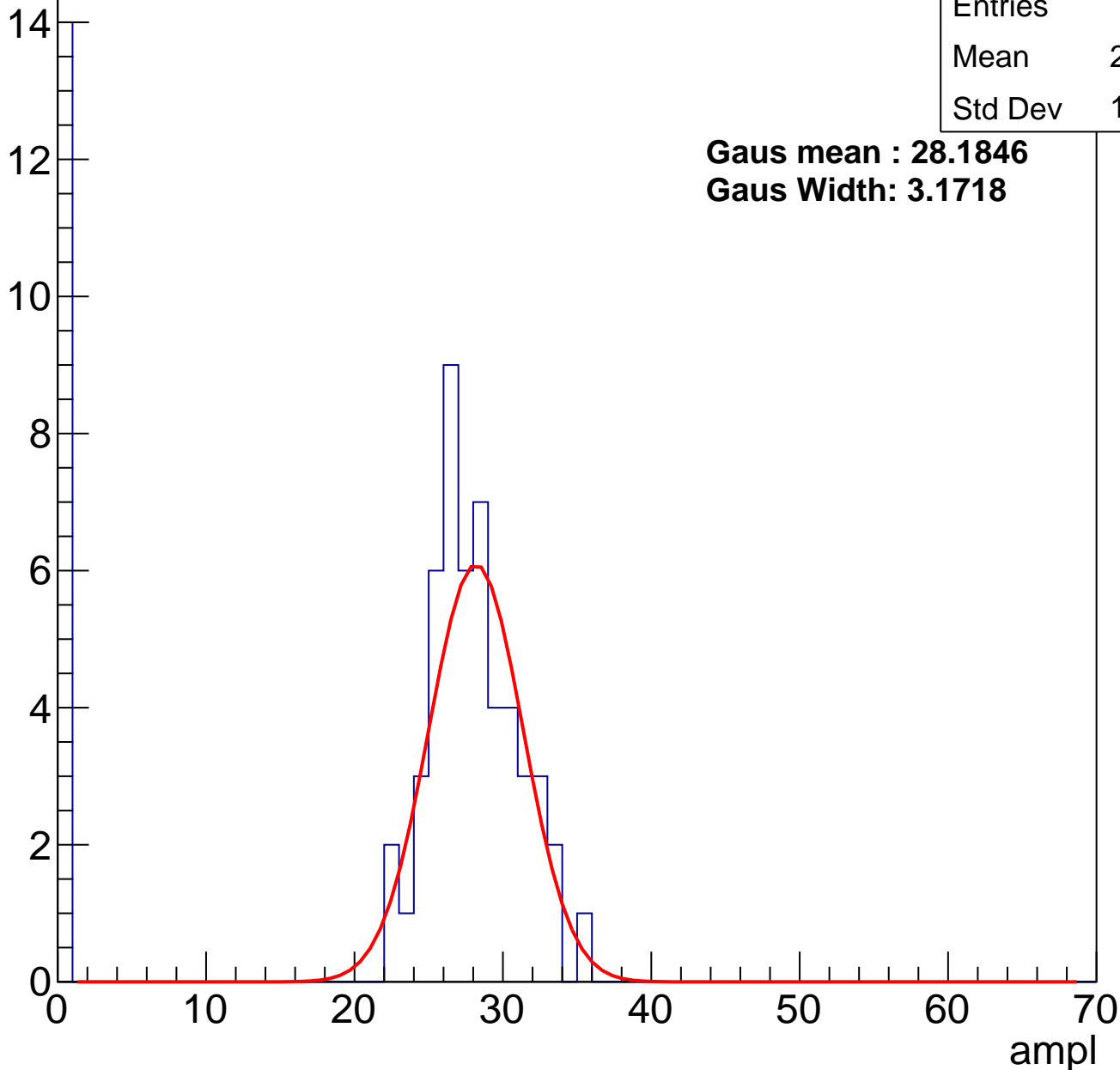
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	65
Mean	21.65
Std Dev	11.63

**Gaus mean : 28.1846**

**Gaus Width: 3.1718**

Entry



# B1L103S, U26-ch105, adc1

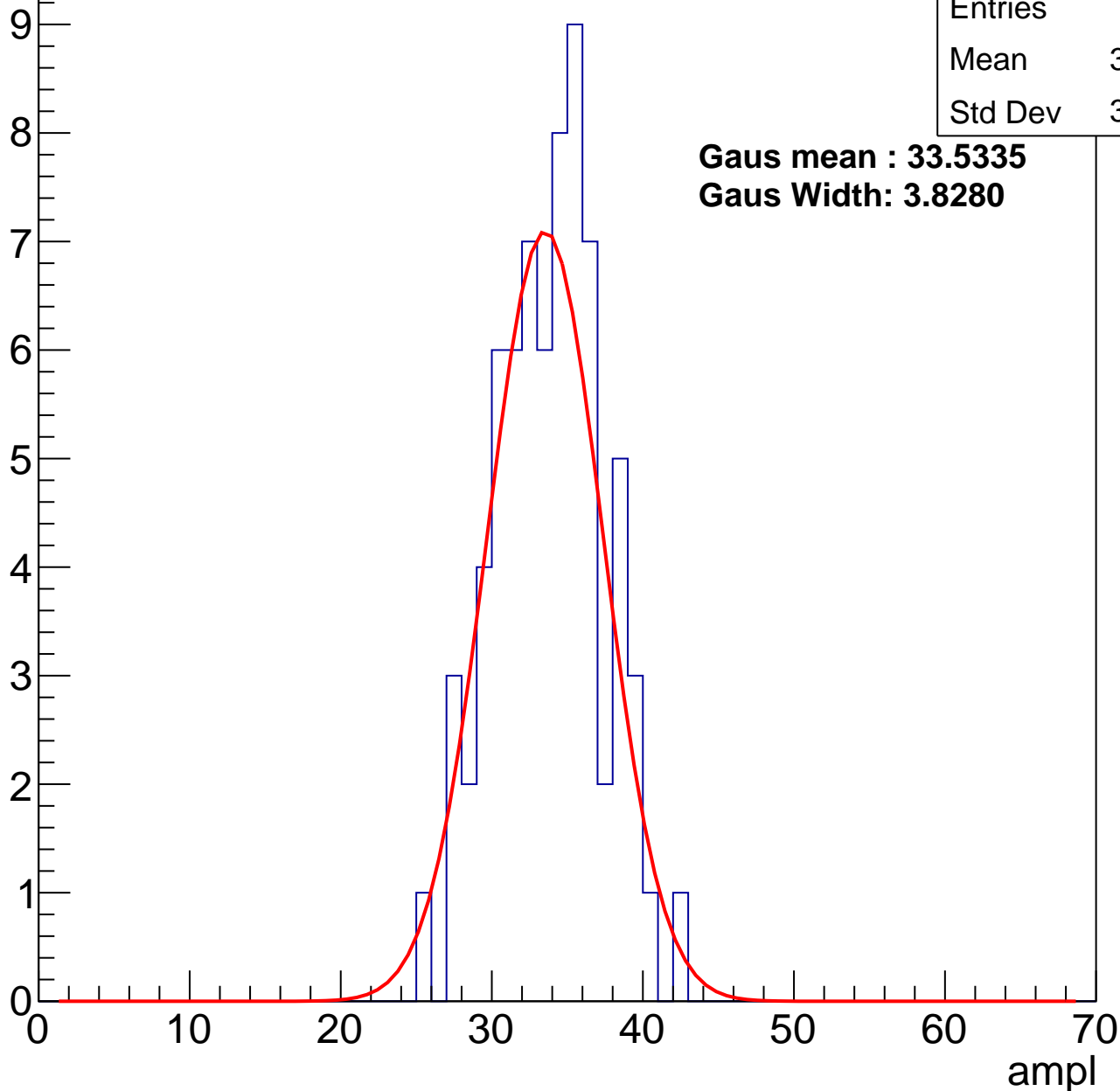
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	71
Mean	33.35
Std Dev	3.489

**Gaus mean : 33.5335**

**Gaus Width: 3.8280**



# B1L103S, U26-ch105, adc2

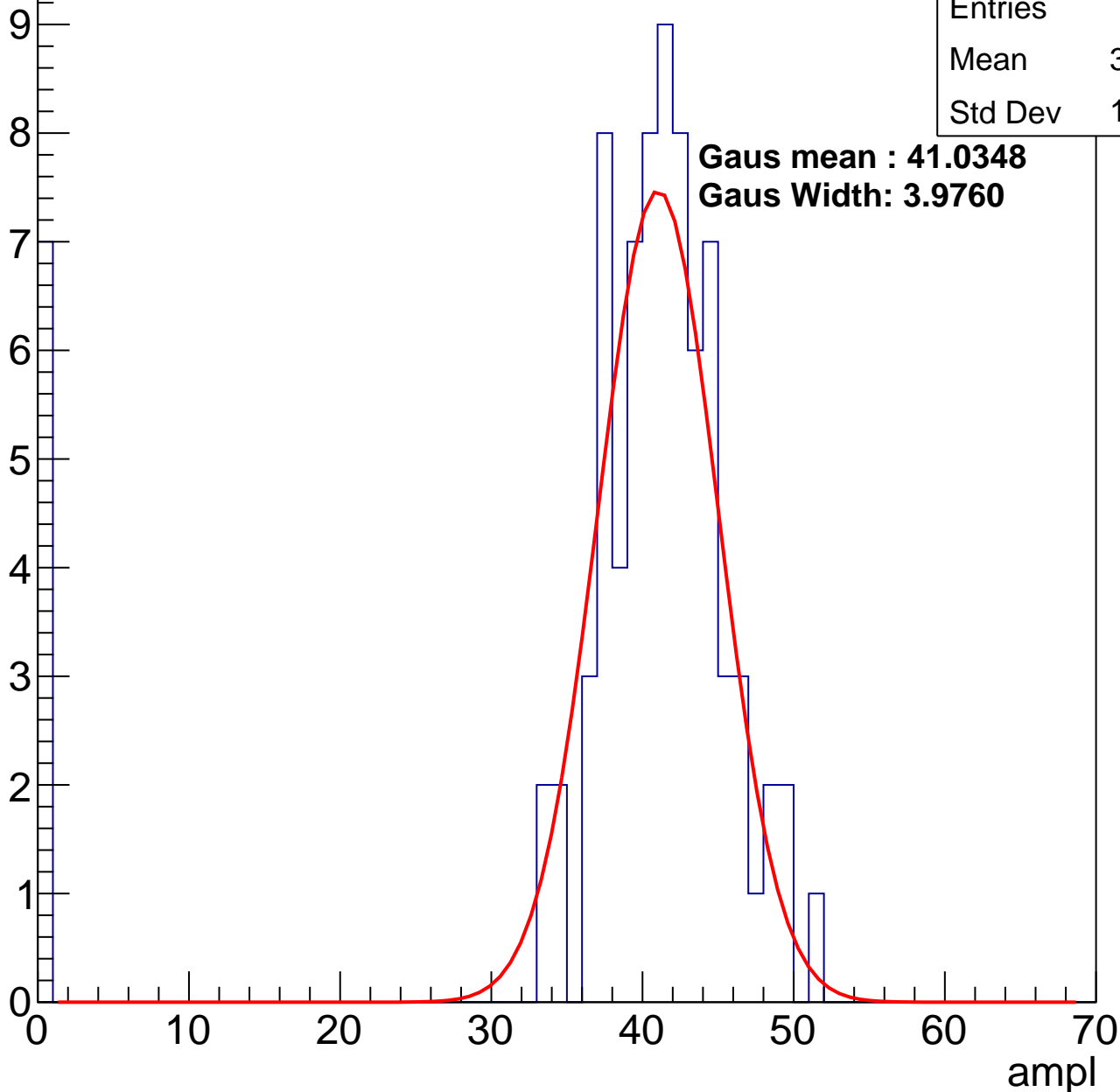
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	83
Mean	37.58
Std Dev	11.96

**Gaus mean : 41.0348**

**Gaus Width: 3.9760**

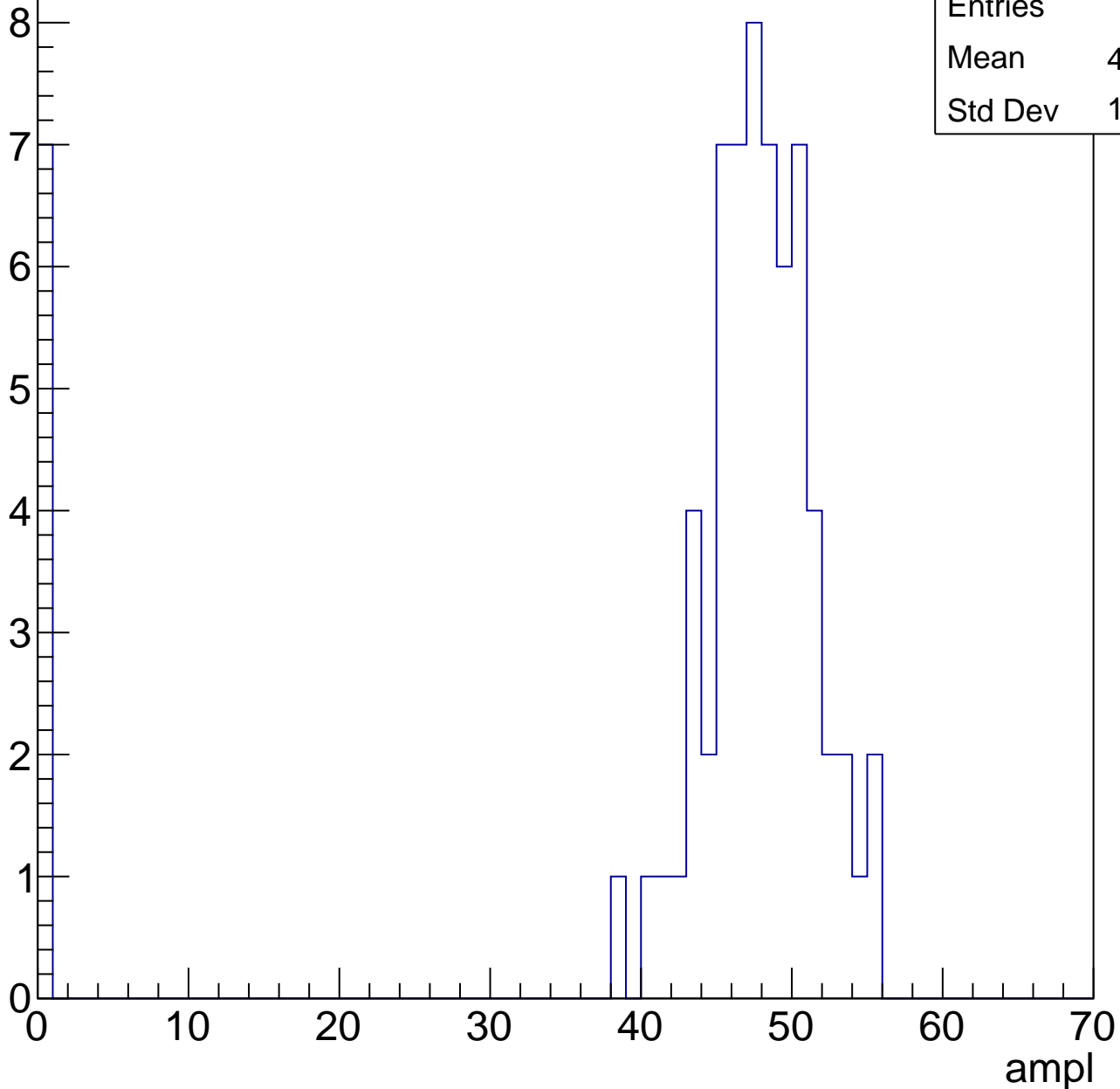


# B1L103S, U26-ch105, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	70
Mean	42.74
Std Dev	14.62

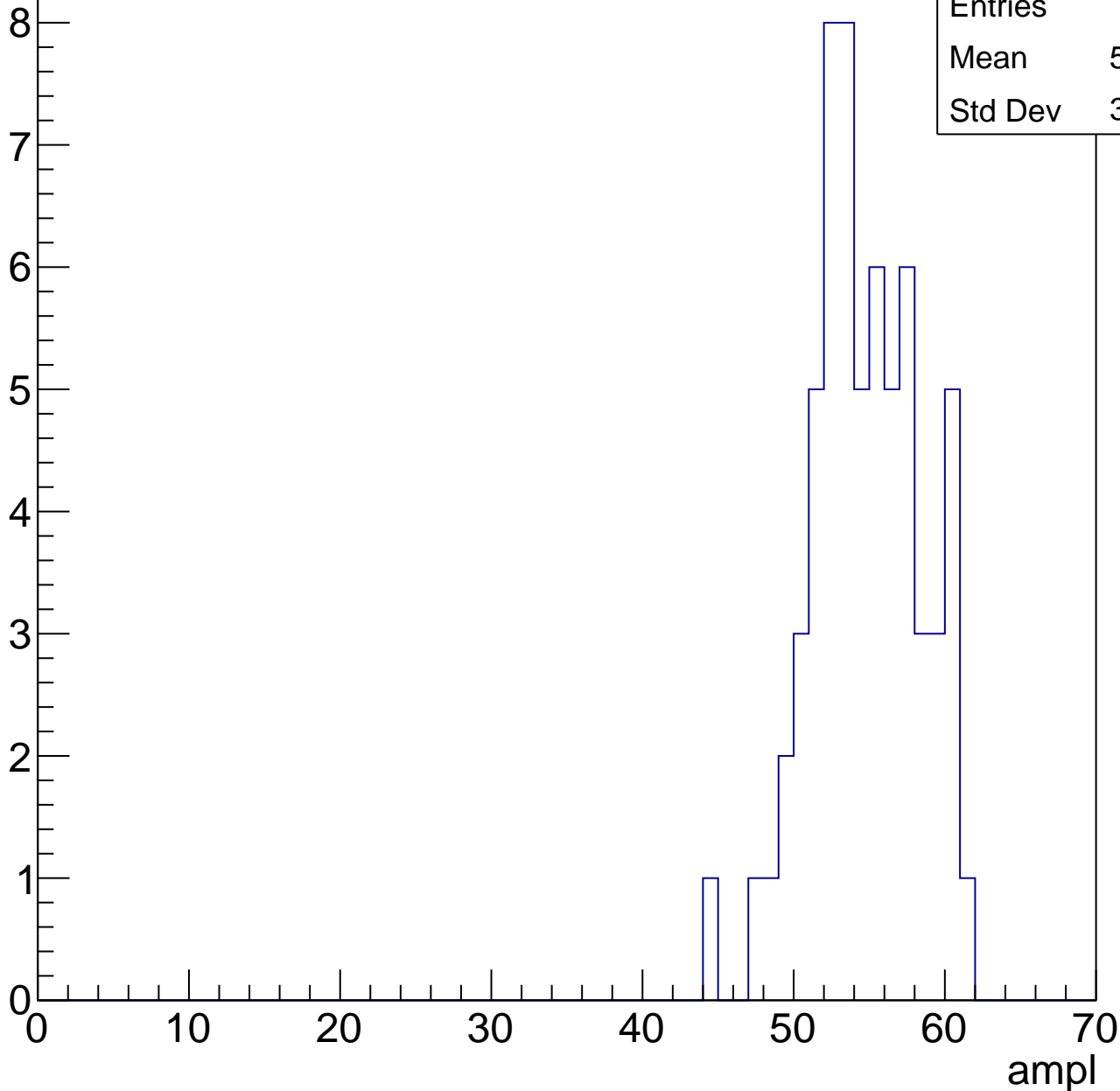


# B1L103S, U26-ch105, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	63
Mean	54.22
Std Dev	3.557

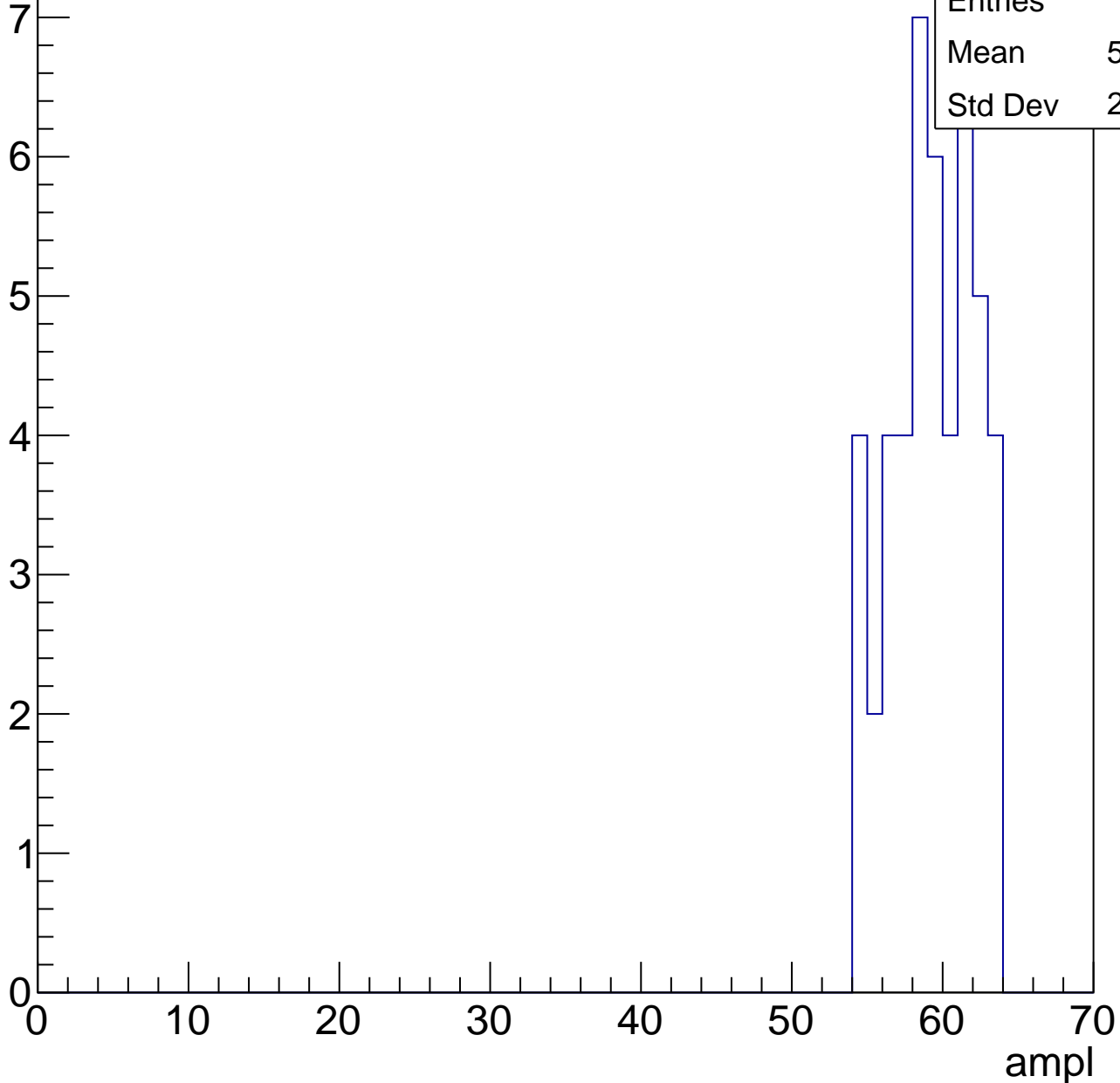


# B1L103S, U26-ch105, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	47
Mean	58.87
Std Dev	2.655

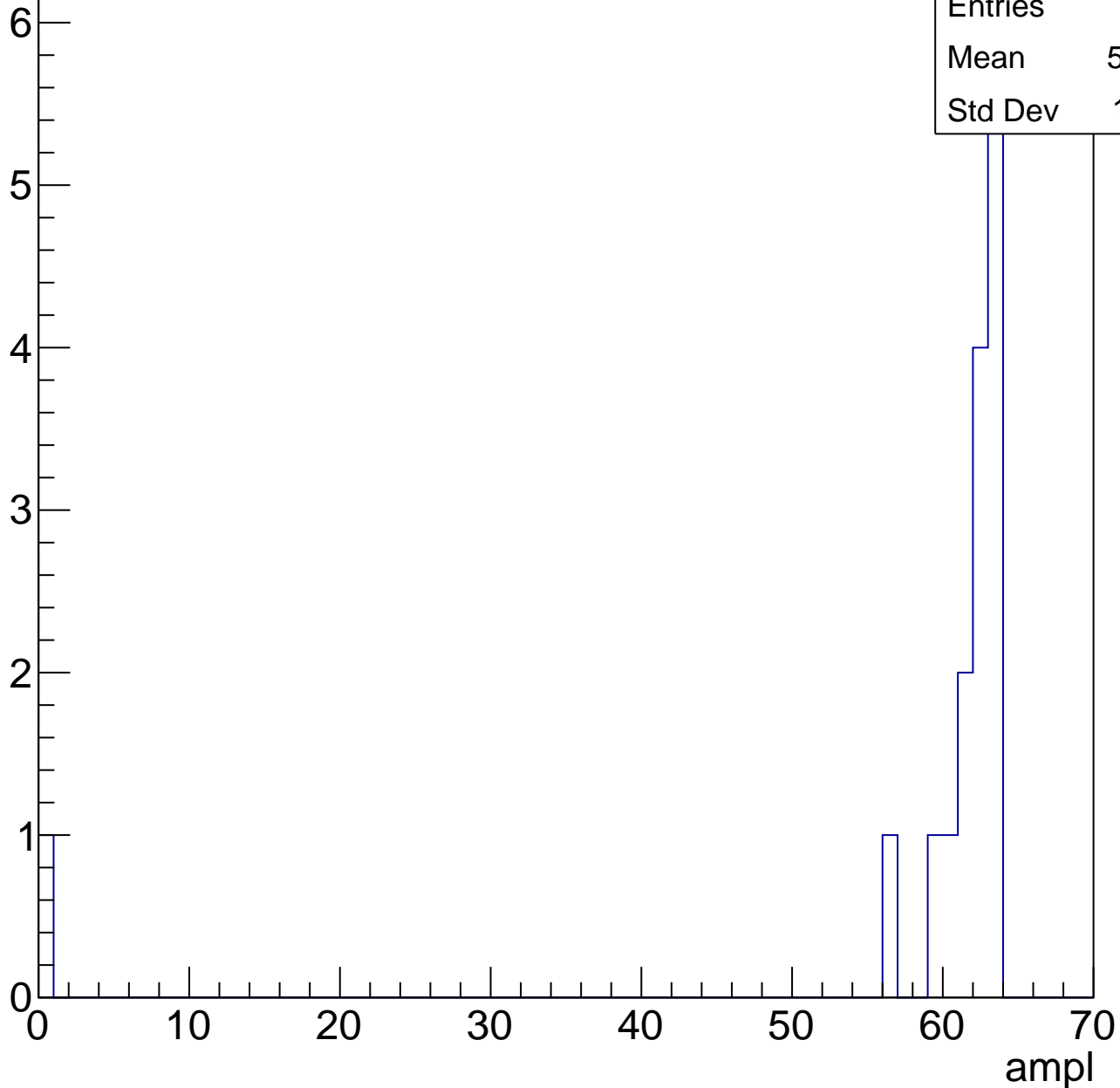


# B1L103S, U26-ch105, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	16
Mean	57.69
Std Dev	15.01



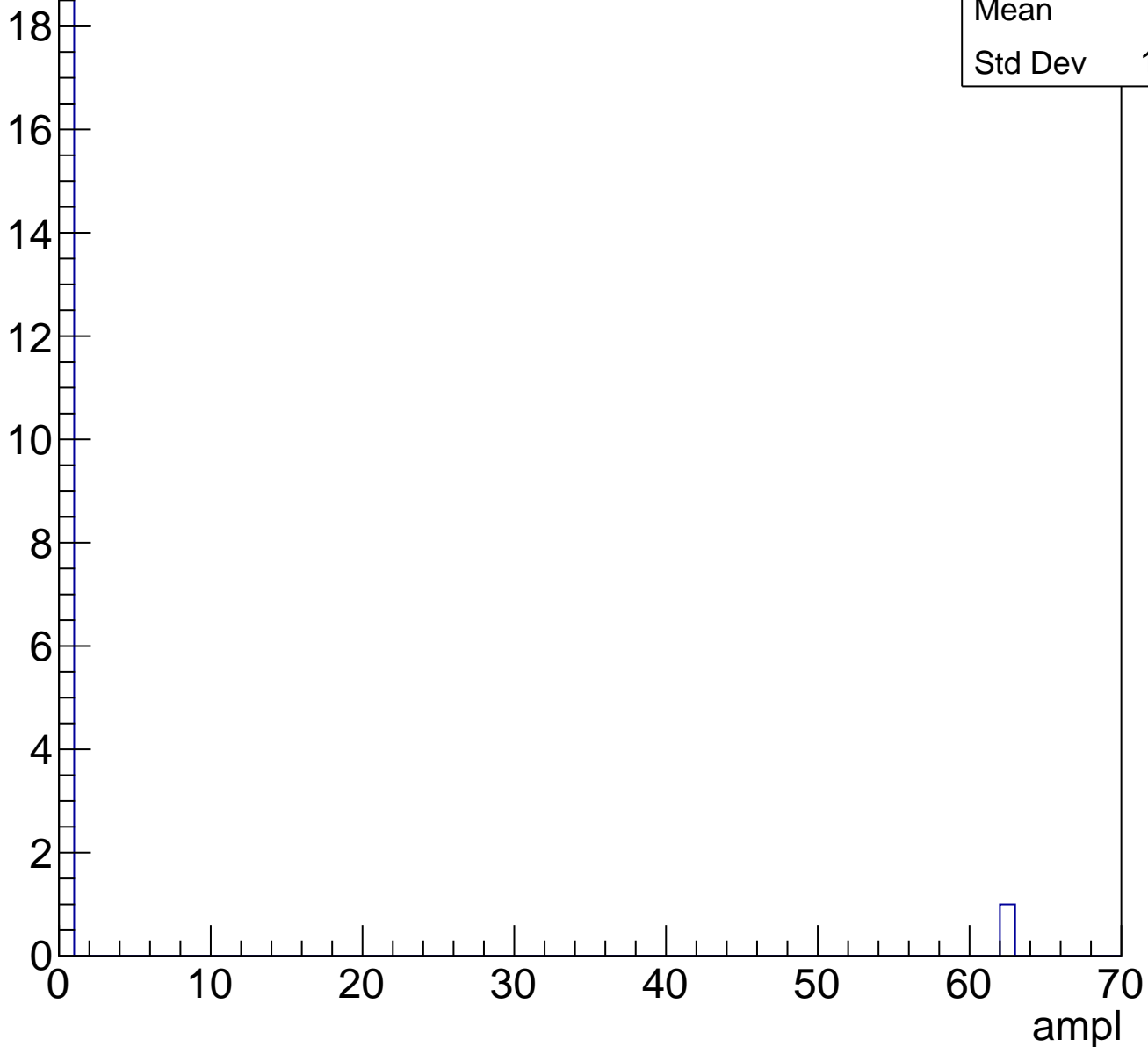


# B1L103S, U26-ch105, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	20
Mean	3.1
Std Dev	13.51

Entry



# B1L103S, U26-ch106, adc0

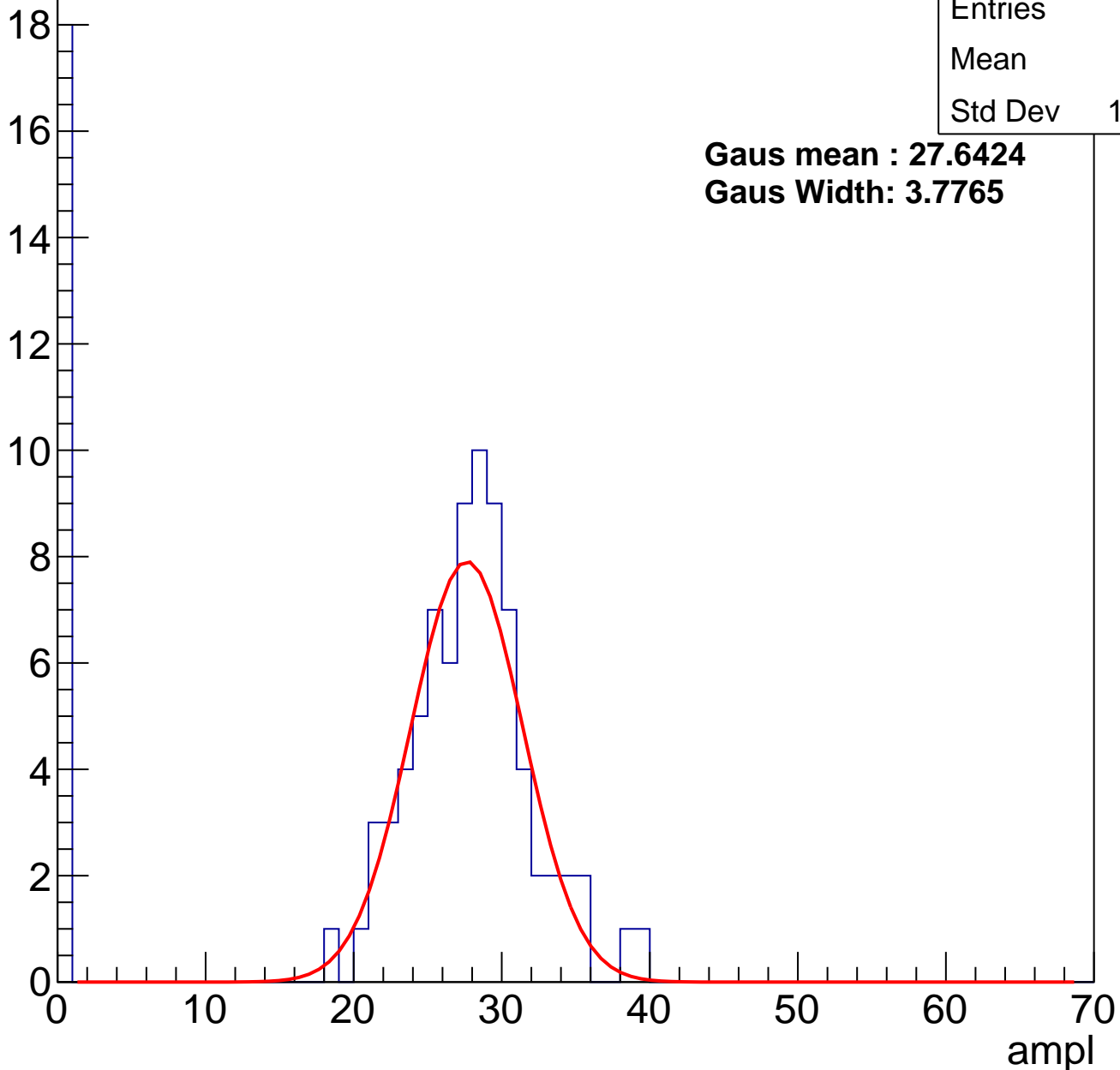
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	97
Mean	22.4
Std Dev	11.27

**Gaus mean : 27.6424**

**Gaus Width: 3.7765**

Entry



# B1L103S, U26-ch106, adc1

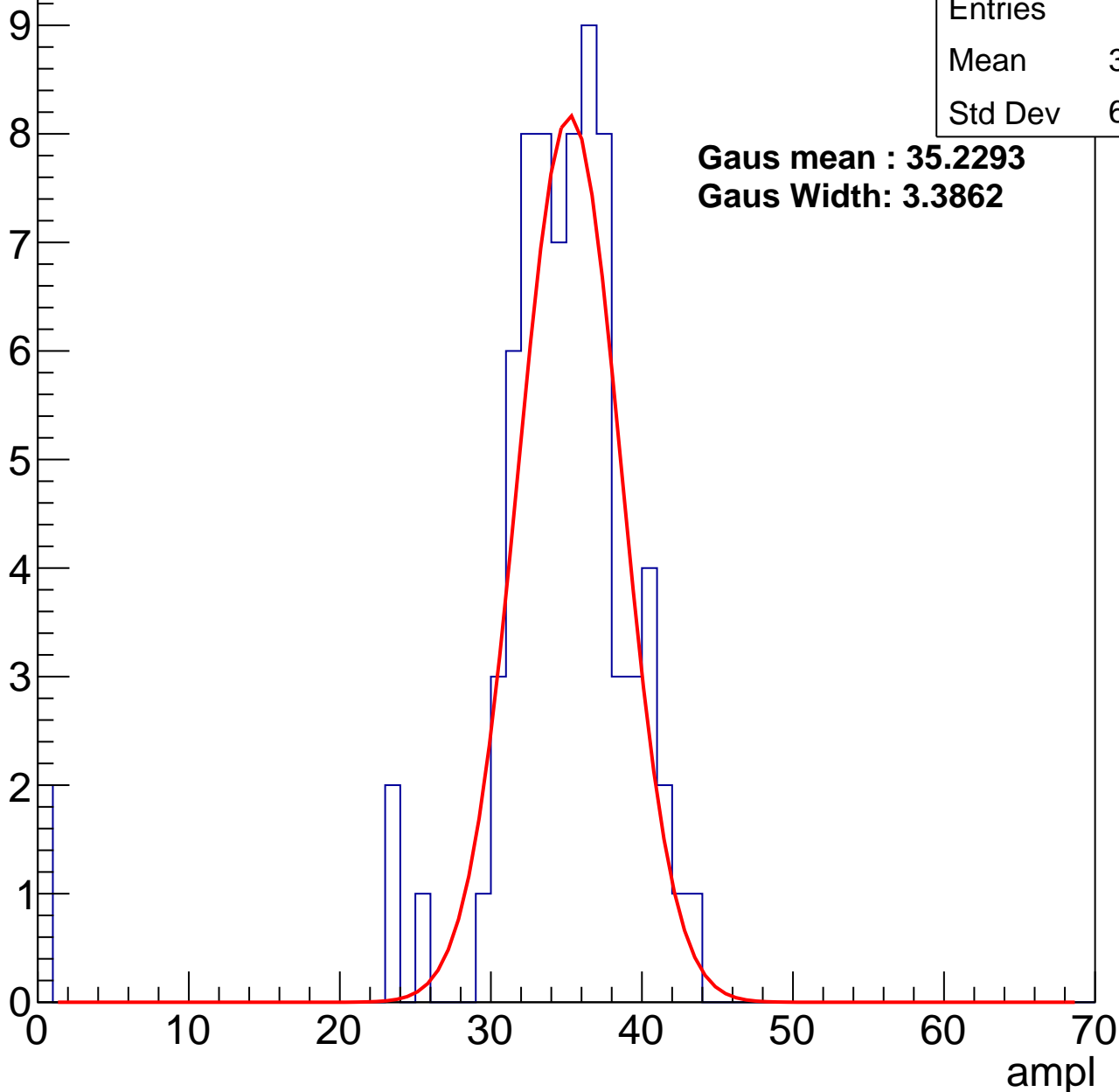
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	77
Mean	33.66
Std Dev	6.664

**Gaus mean : 35.2293**

**Gaus Width: 3.3862**



# B1L103S, U26-ch106, adc2

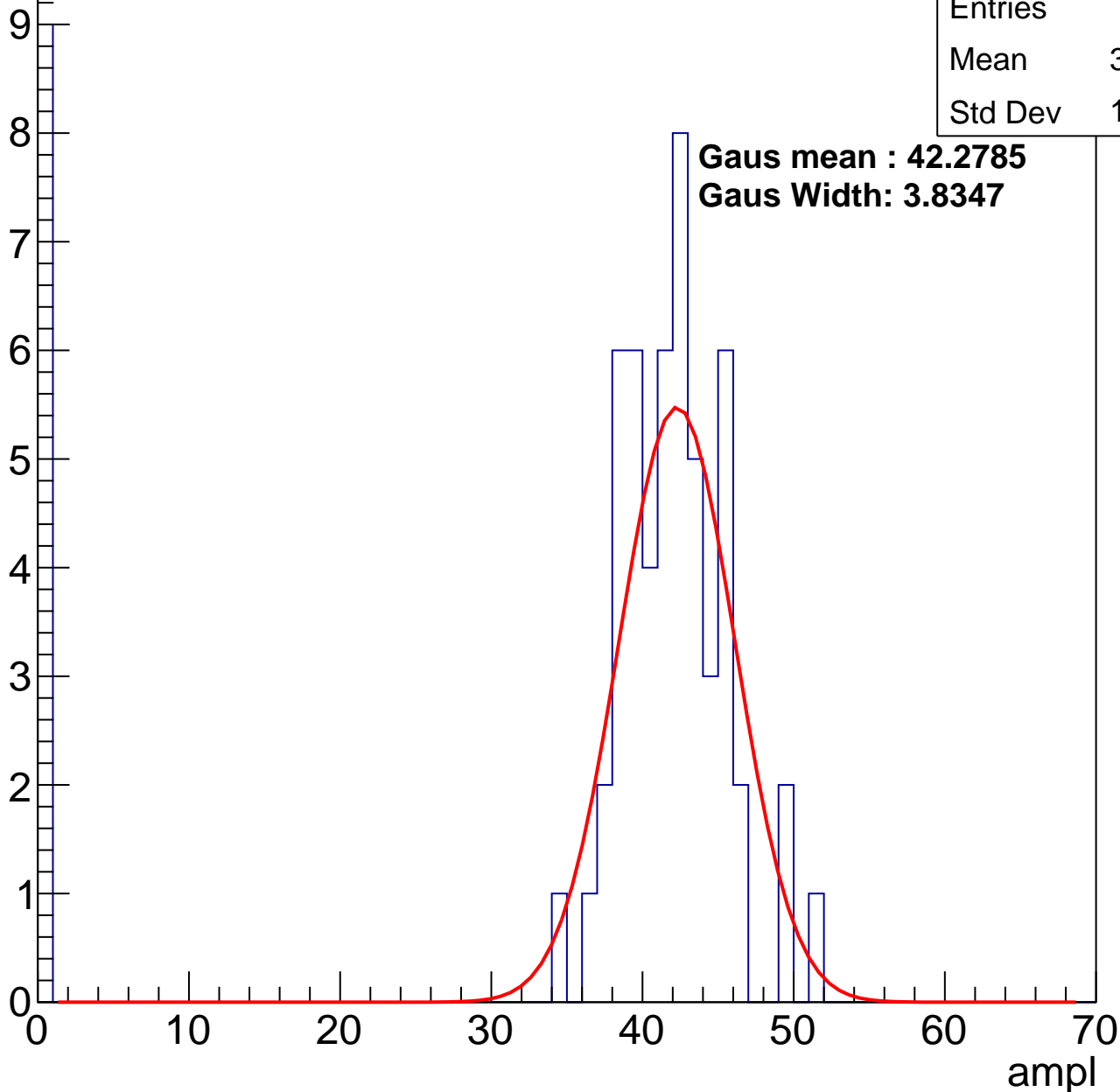
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	62
Mean	35.58
Std Dev	14.99

**Gaus mean : 42.2785**

**Gaus Width: 3.8347**

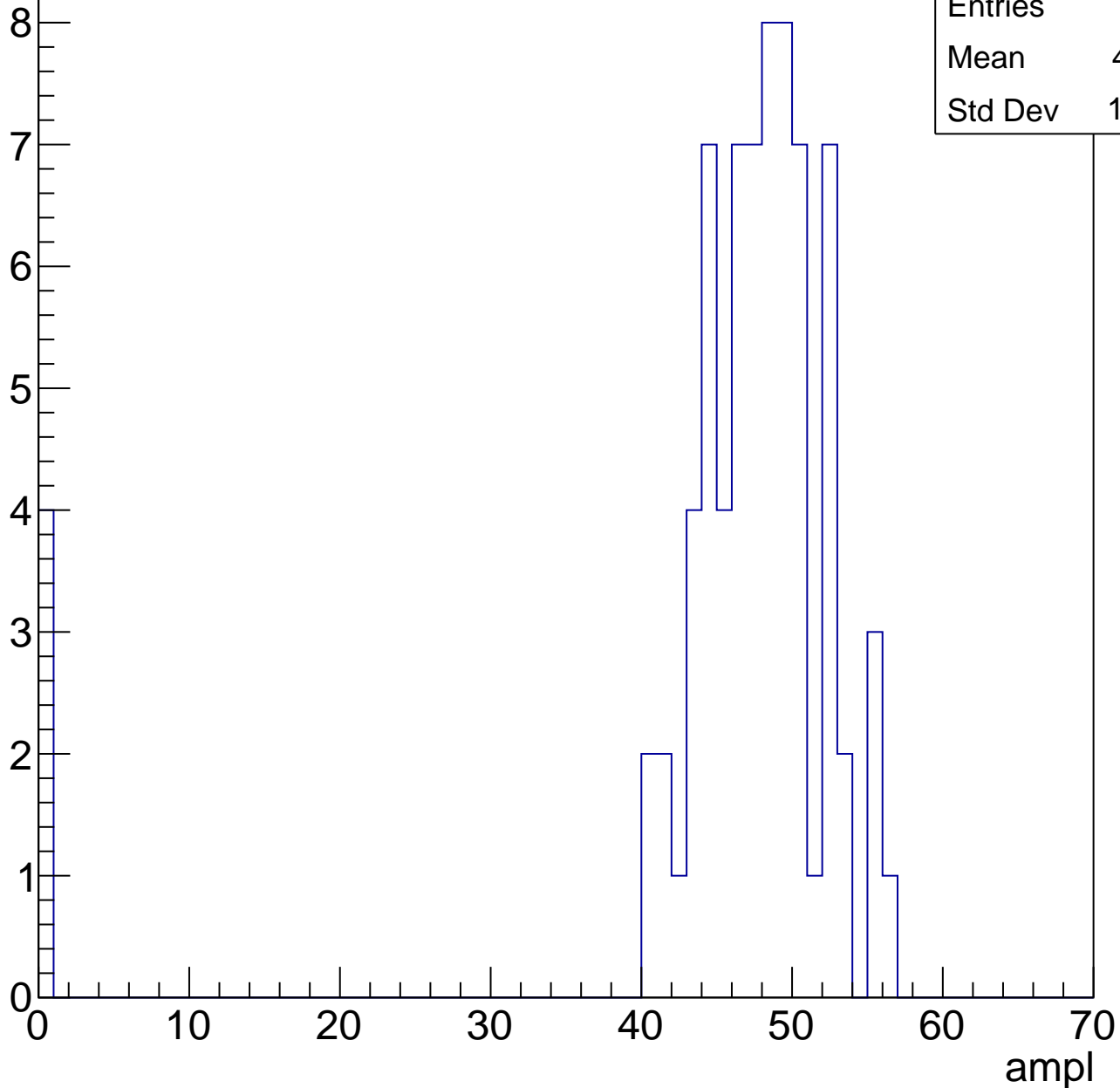


# B1L103S, U26-ch106, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	75
Mean	45.11
Std Dev	11.28

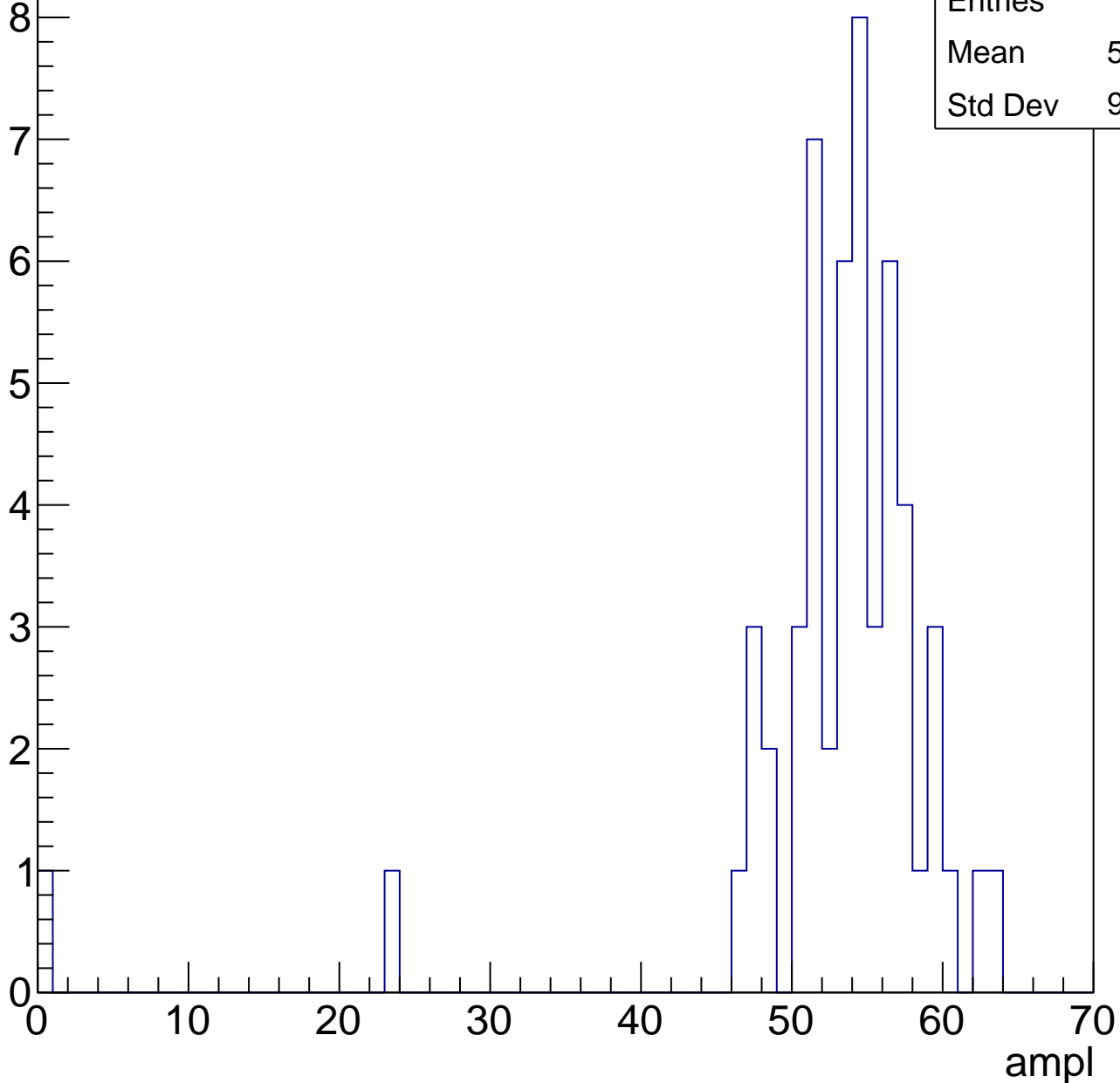


# B1L103S, U26-ch106, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	54
Mean	52.15
Std Dev	9.062

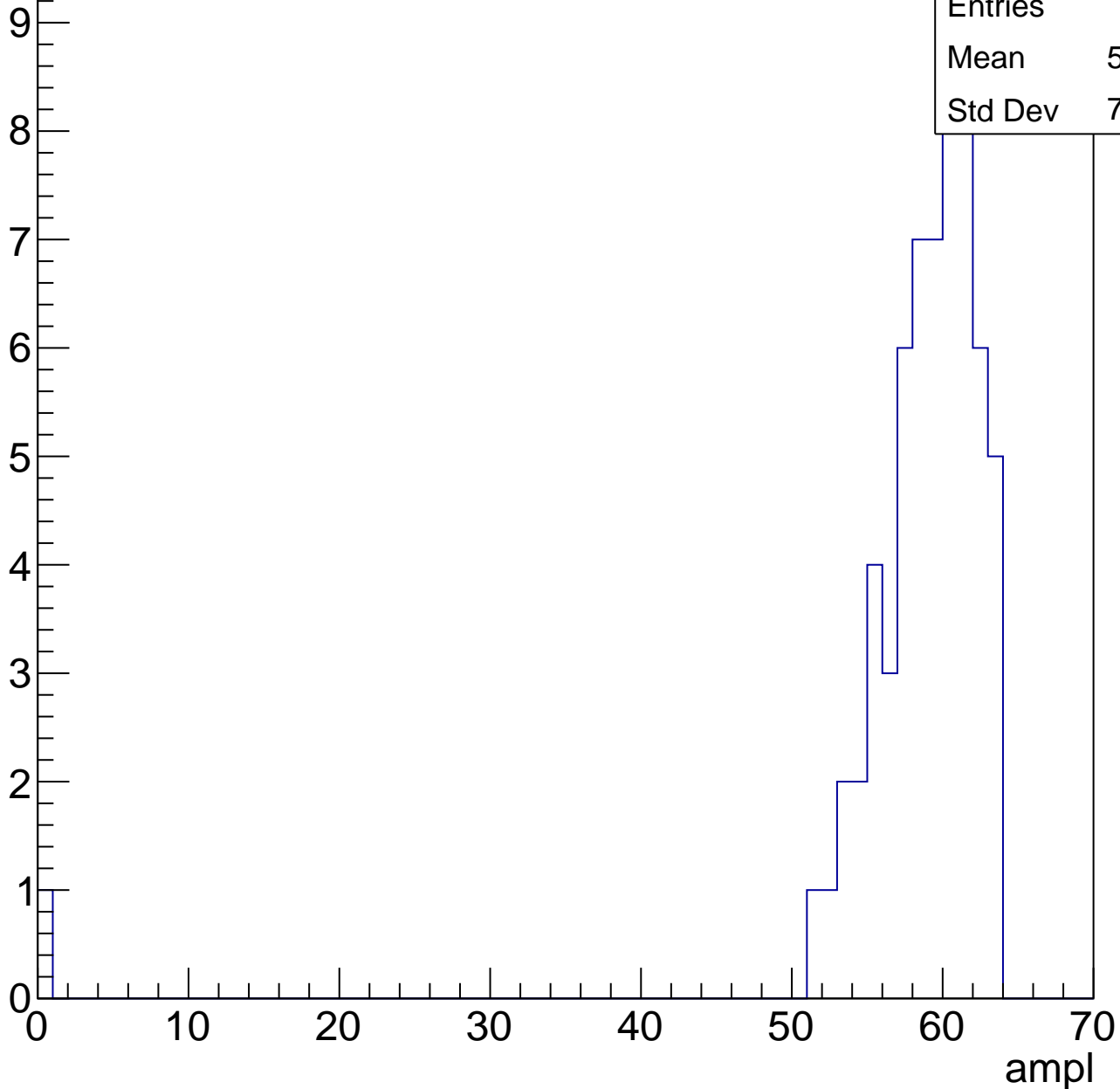


# B1L103S, U26-ch106, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

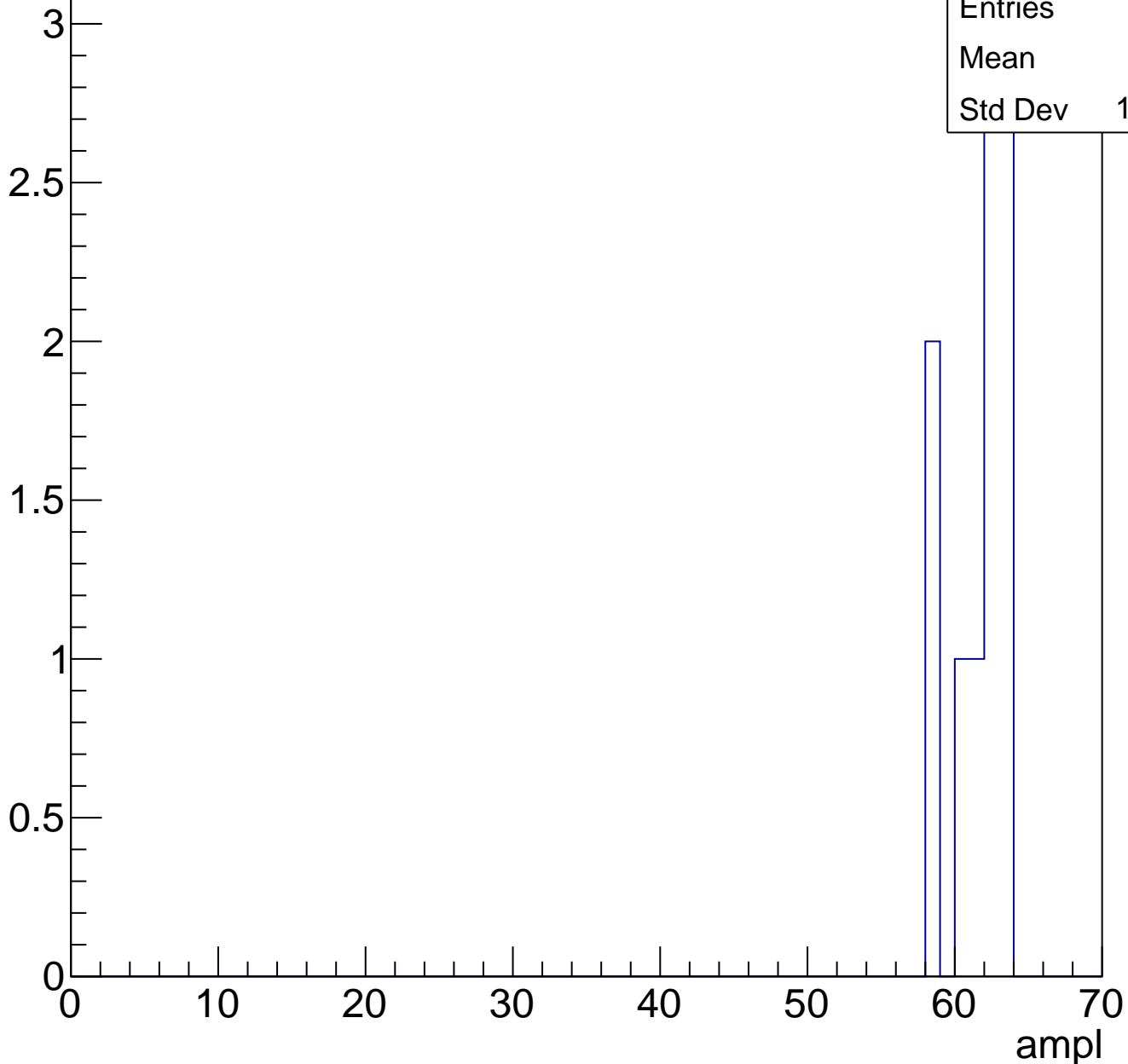
Entries	62
Mean	57.77
Std Dev	7.954



# B1L103S, U26-ch106, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



Entries	10
Mean	61.2
Std Dev	1.833



# B1L103S, U26-ch106, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	20
Mean	3.15
Std Dev	13.73



# B1L103S, U26-ch107, adc0

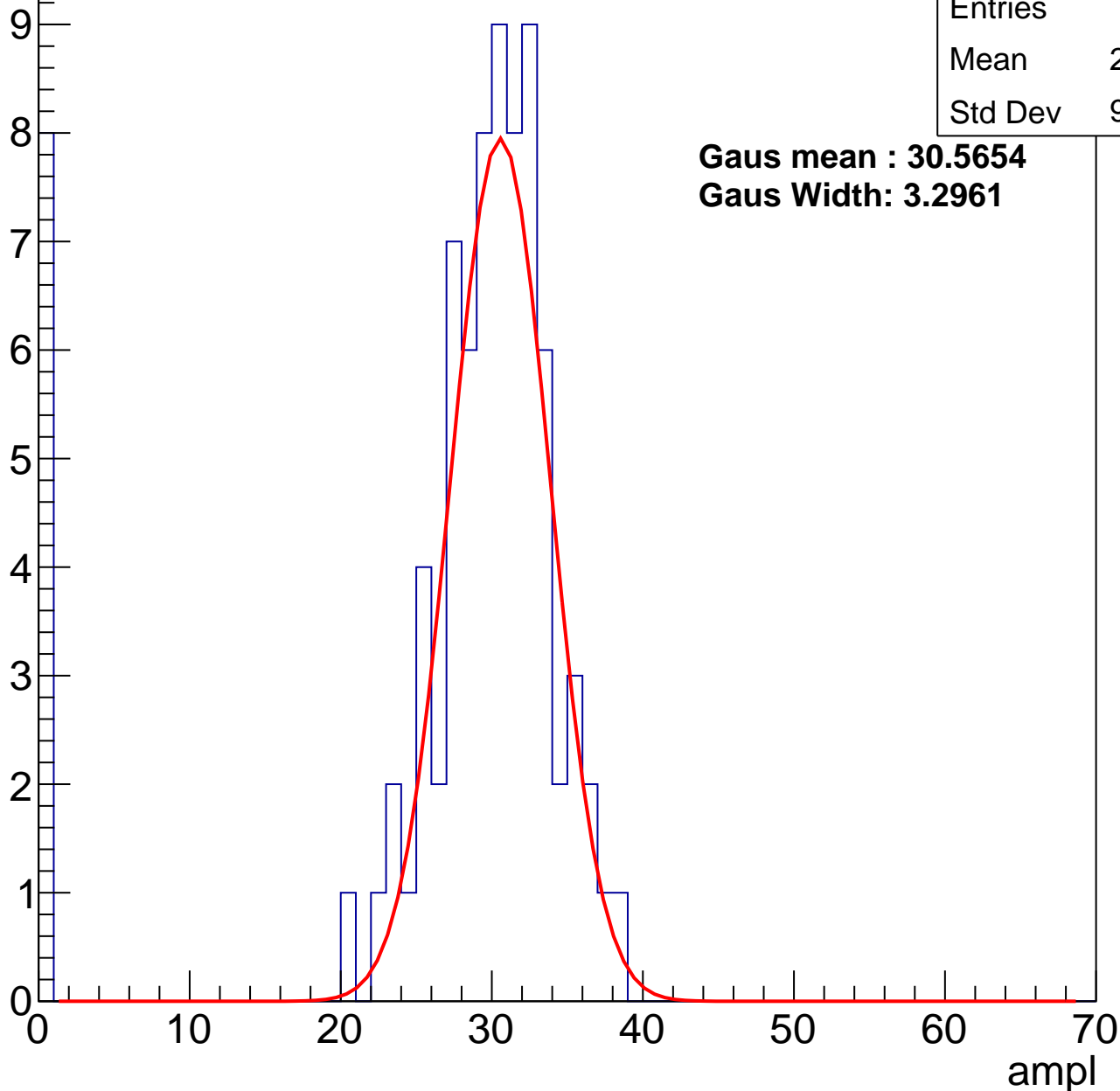
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	81
Mean	26.88
Std Dev	9.509

**Gaus mean : 30.5654**

**Gaus Width: 3.2961**



# B1L103S, U26-ch107, adc1

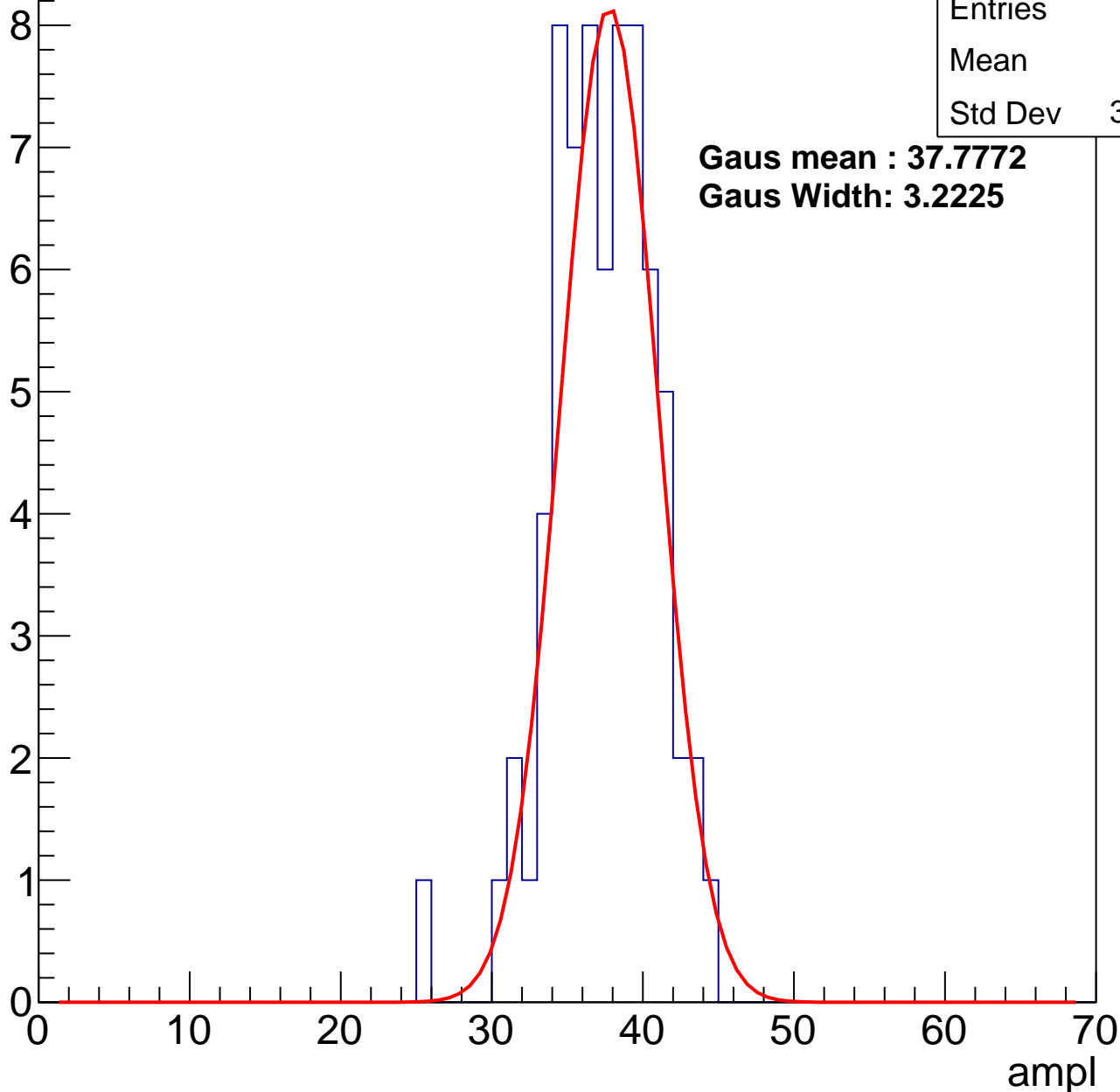
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	70
Mean	36.9
Std Dev	3.394

**Gaus mean : 37.7772**

**Gaus Width: 3.2225**



# B1L103S, U26-ch107, adc2

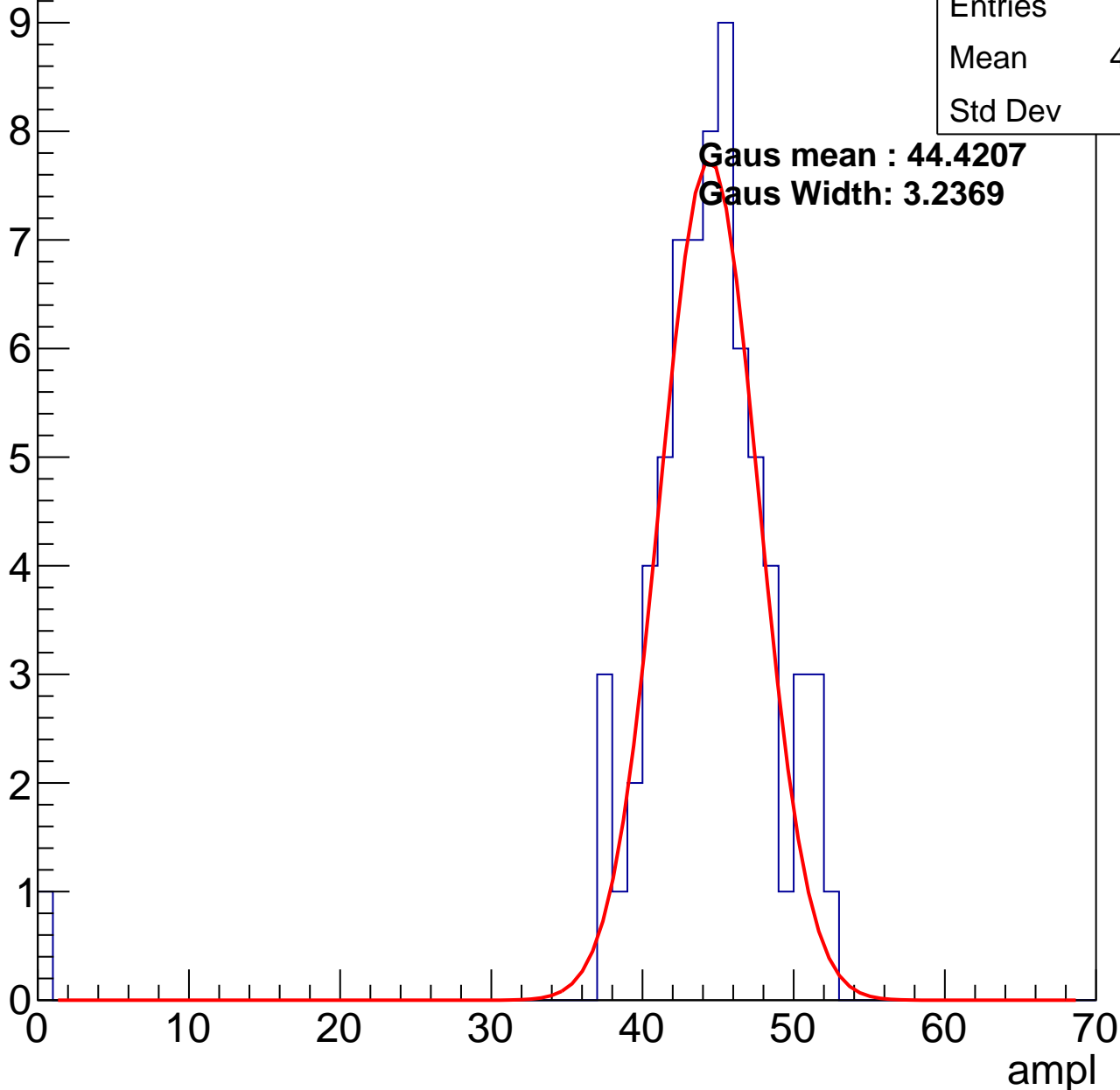
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	70
Mean	43.59
Std Dev	6.31

**Gaus mean : 44.4207**

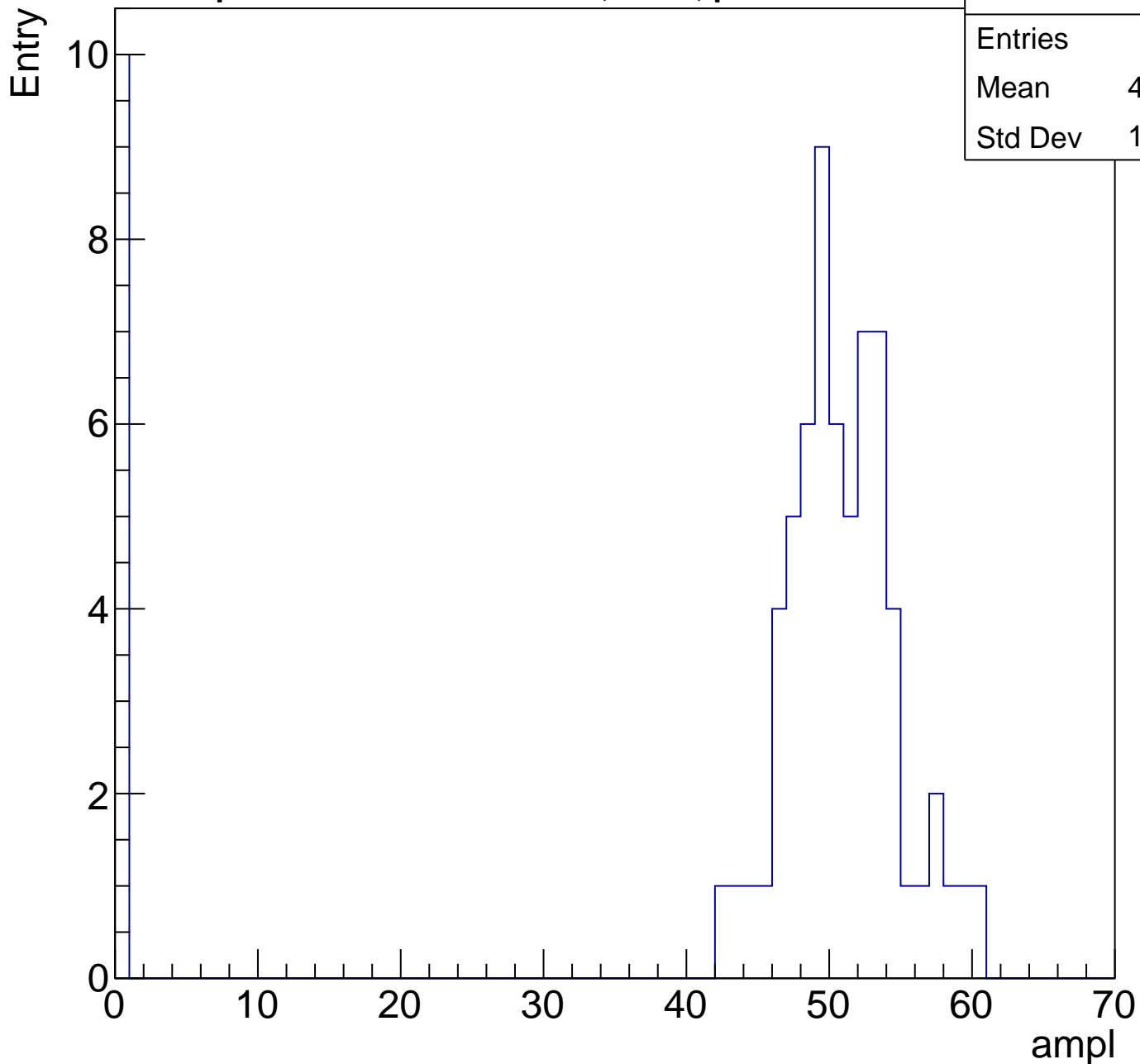
**Gaus Width: 3.2369**



# B1L103S, U26-ch107, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	74
Mean	43.65
Std Dev	17.59

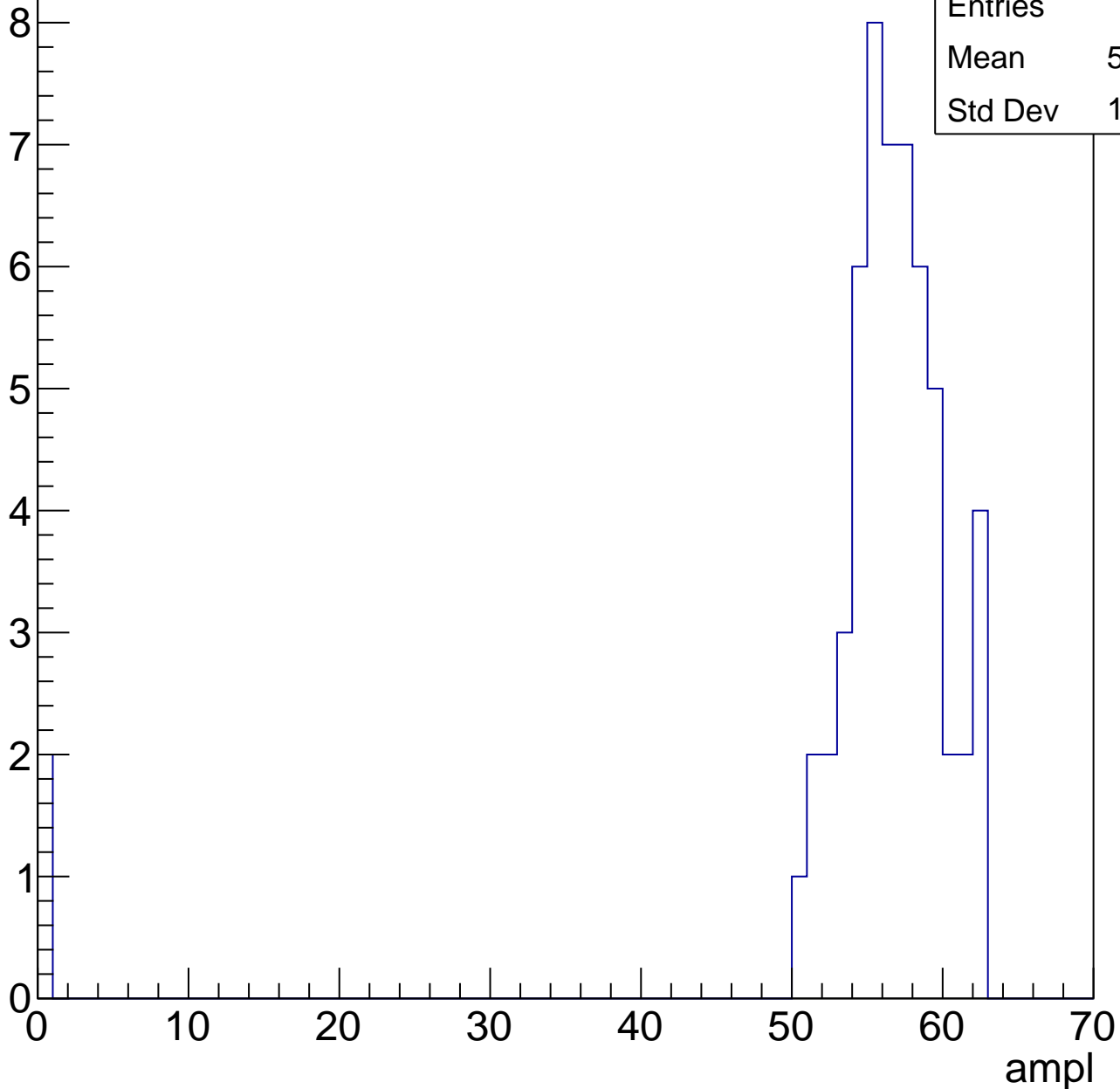


# B1L103S, U26-ch107, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	57
Mean	54.44
Std Dev	10.77



# B1L103S, U26-ch107, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

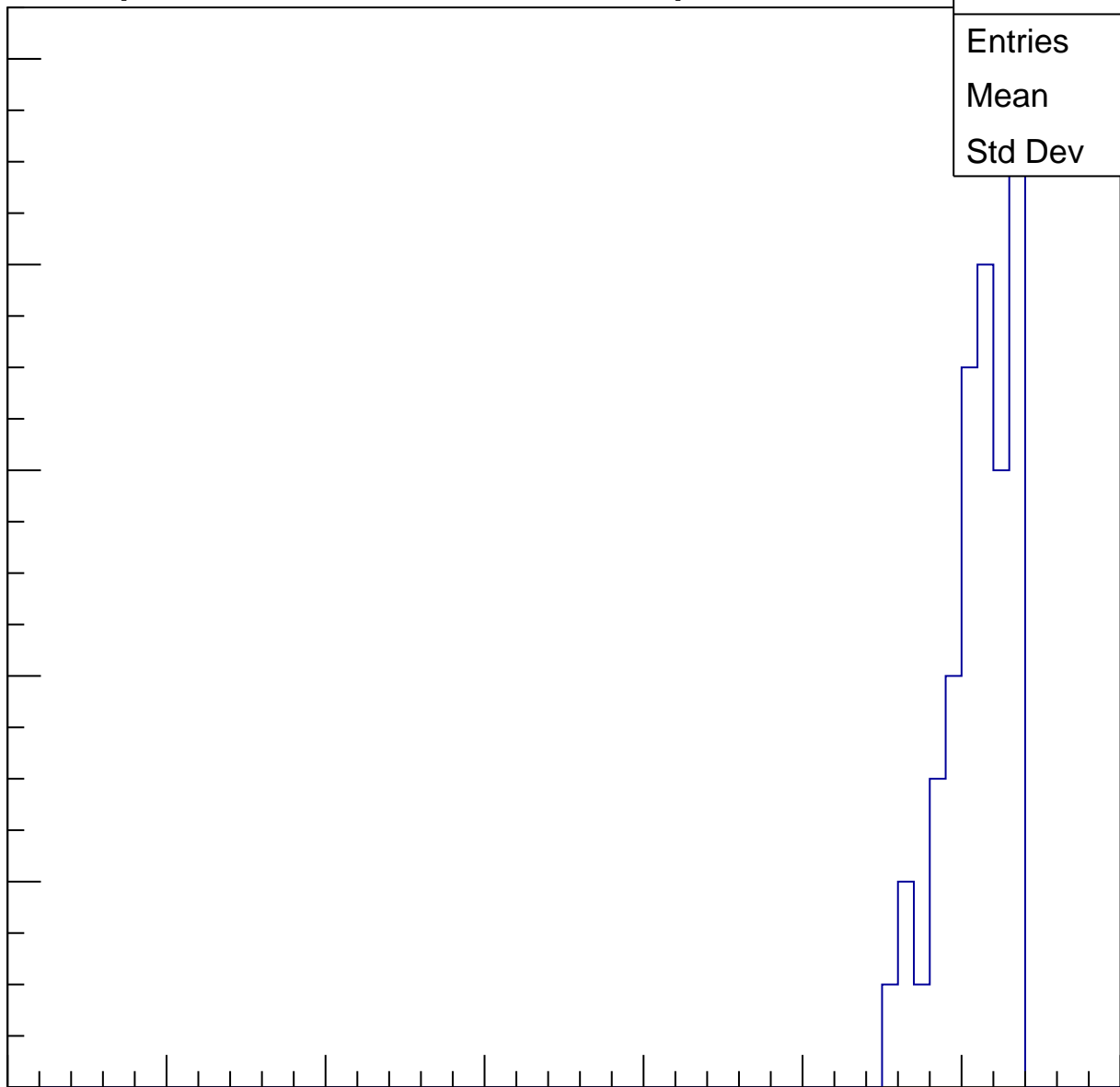
Entries	42
Mean	60.57
Std Dev	2.129

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B1L103S, U26-ch107, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



Entries	0
Mean	0
Std Dev	0



# B1L103S, U26-ch107, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



# B1L103S, U26-ch108, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	78
Mean	21.96
Std Dev	11.21

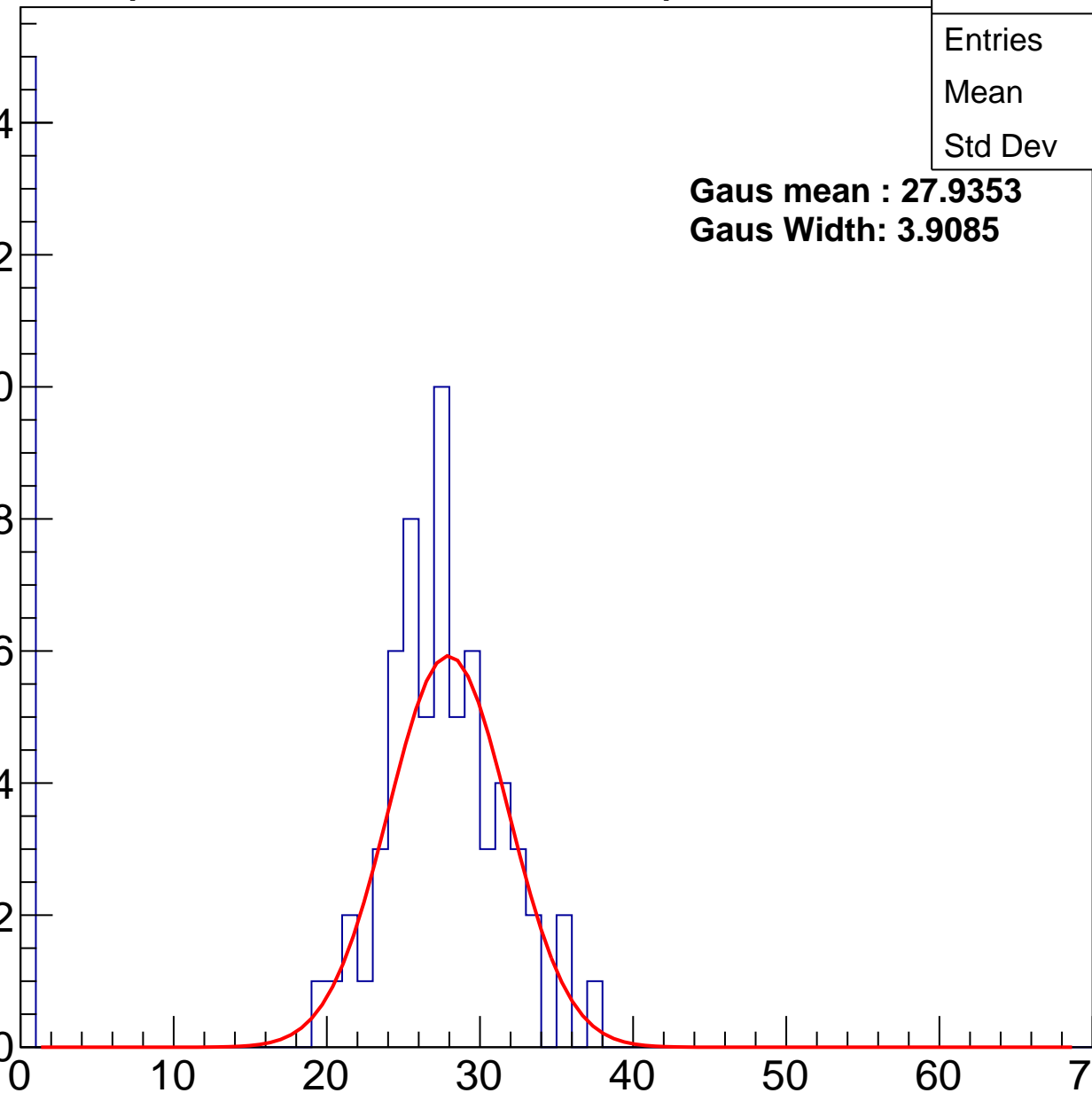
**Gaus mean : 27.9353**

**Gaus Width: 3.9085**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U26-ch108, adc1

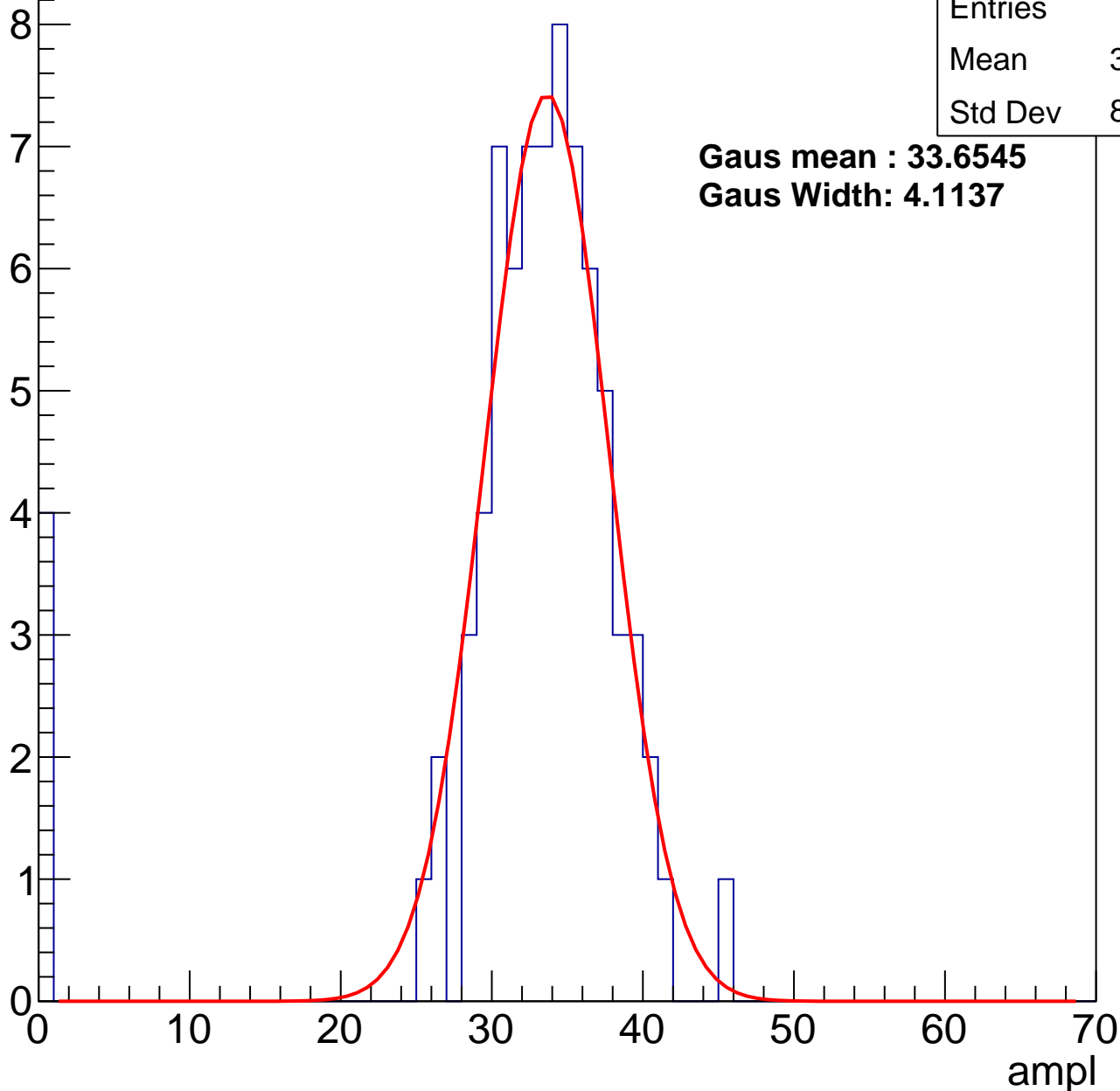
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	77
Mean	31.73
Std Dev	8.285

**Gaus mean : 33.6545**

**Gaus Width: 4.1137**



# B1L103S, U26-ch108, adc2

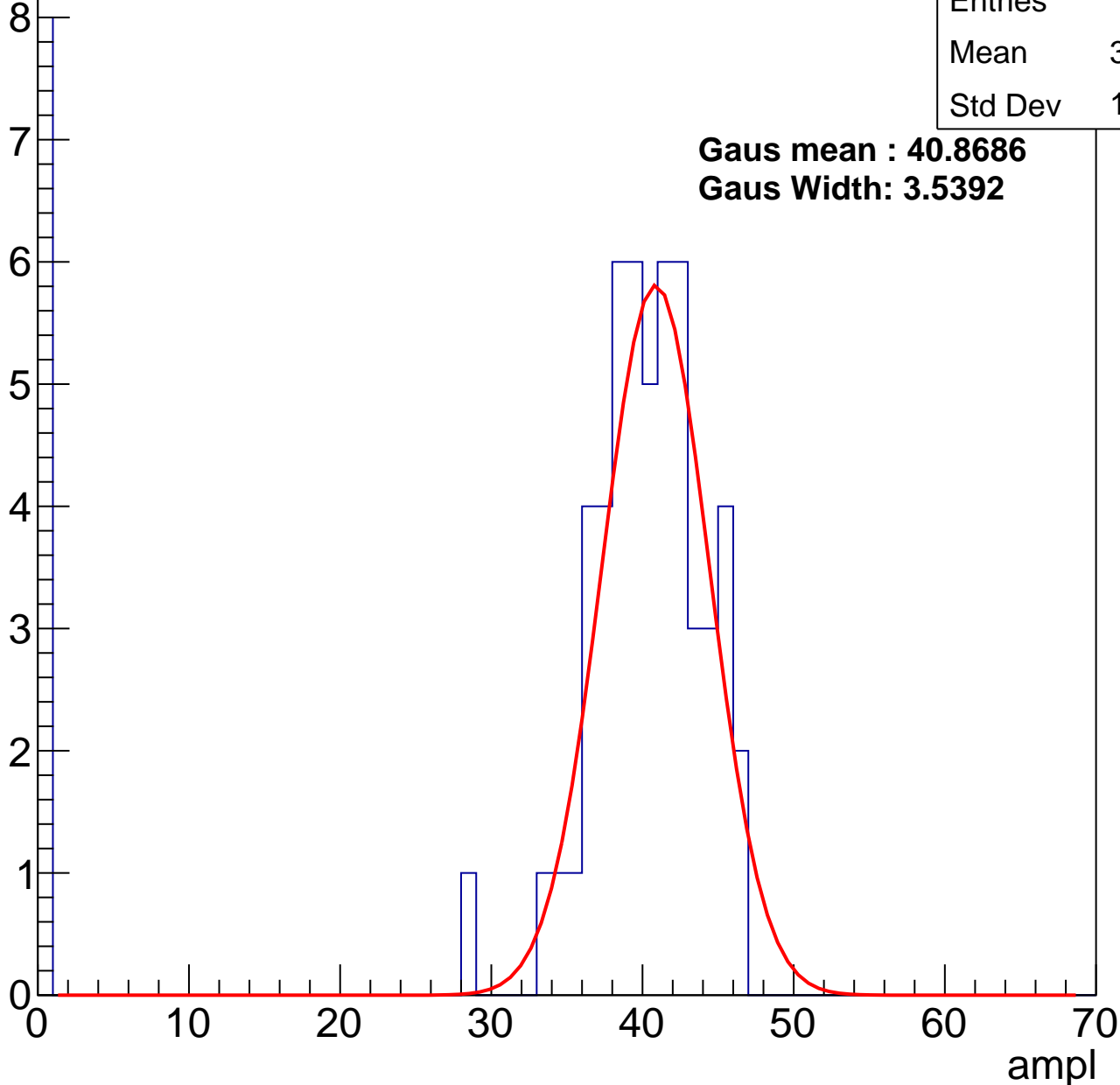
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	61
Mean	34.67
Std Dev	13.87

**Gaus mean : 40.8686**

**Gaus Width: 3.5392**

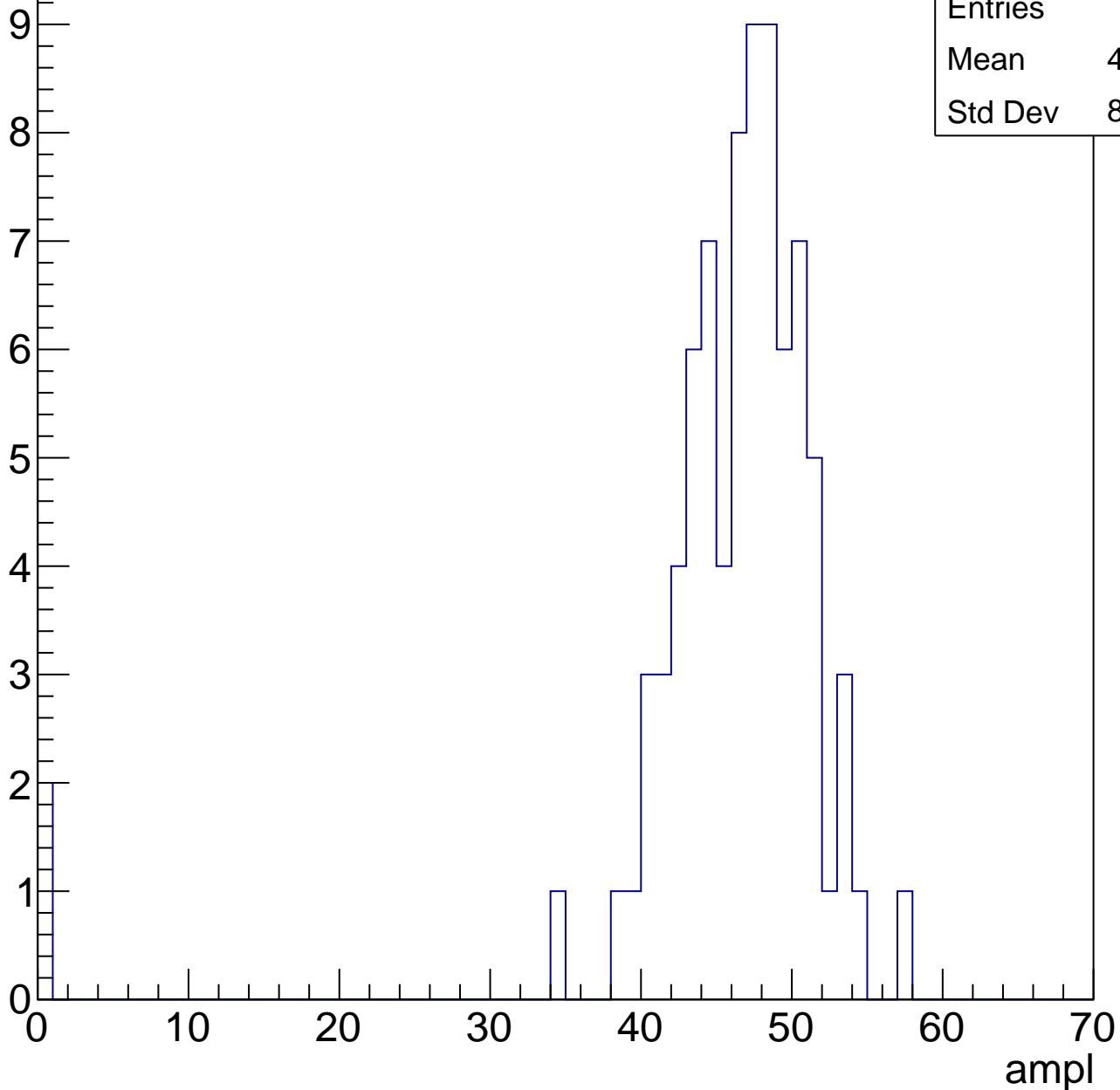


# B1L103S, U26-ch108, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	82
Mean	45.27
Std Dev	8.176

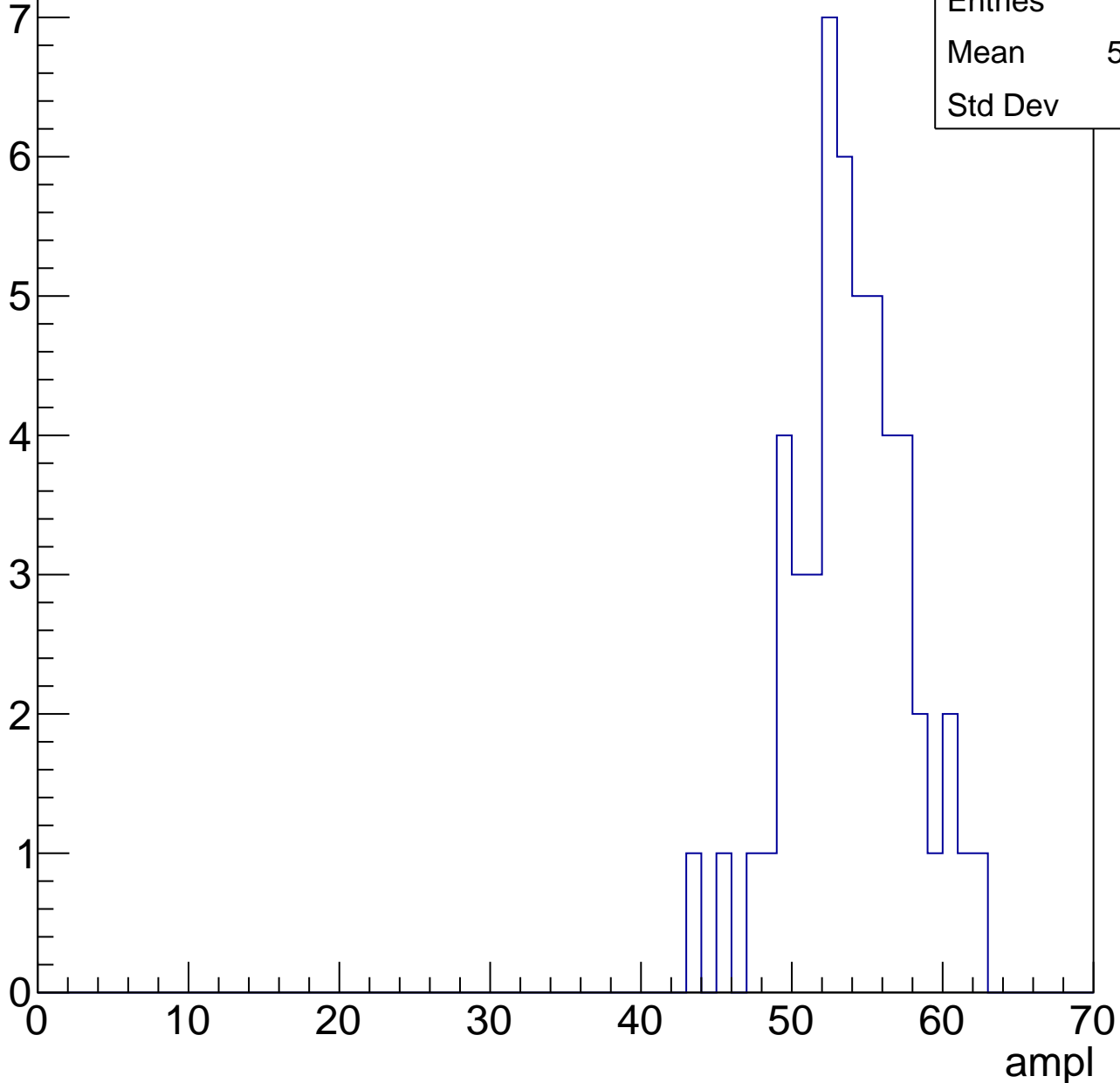


# B1L103S, U26-ch108, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	52
Mean	53.44
Std Dev	3.87

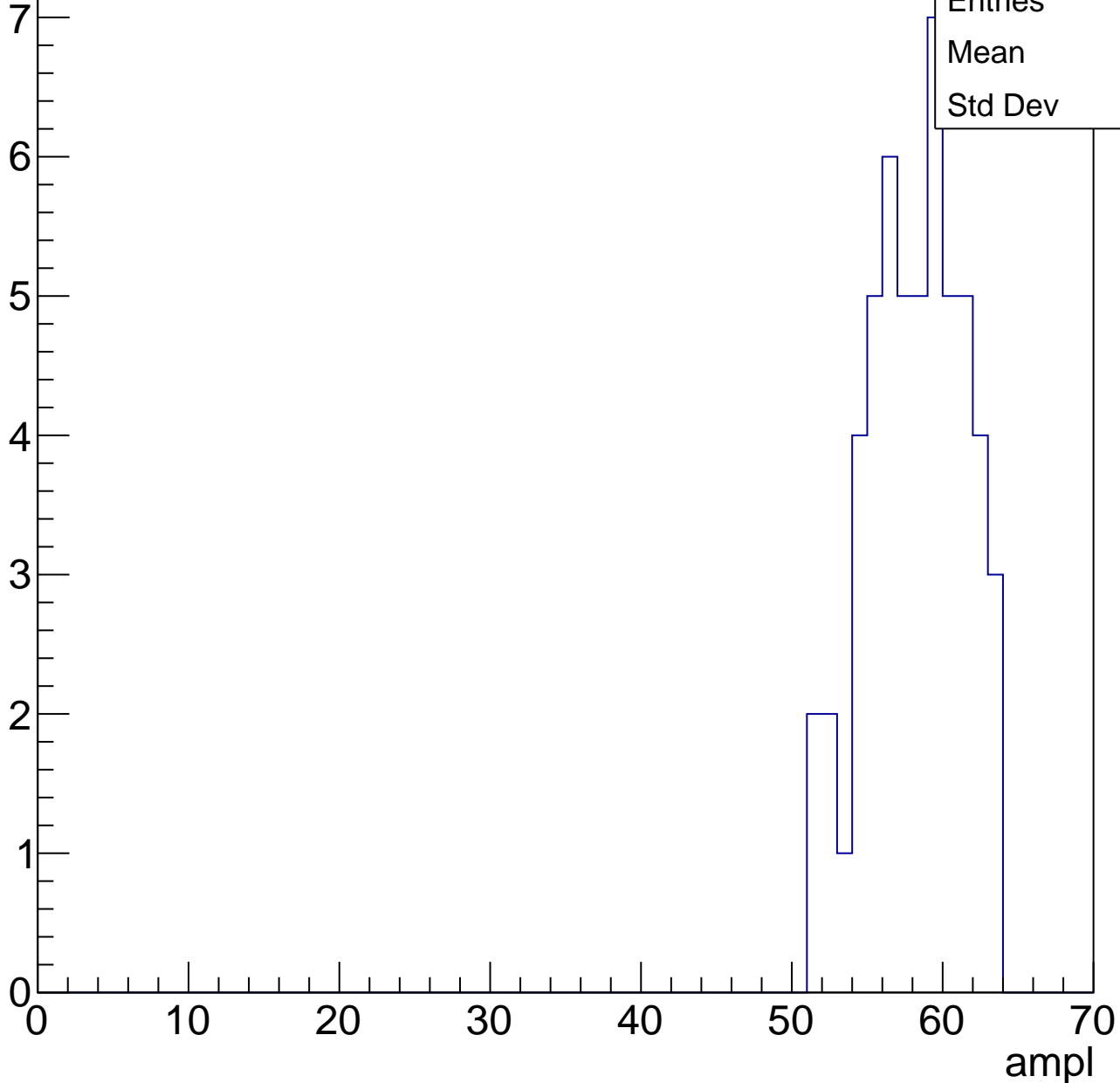


# B1L103S, U26-ch108, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	54
Mean	57.7
Std Dev	3.16

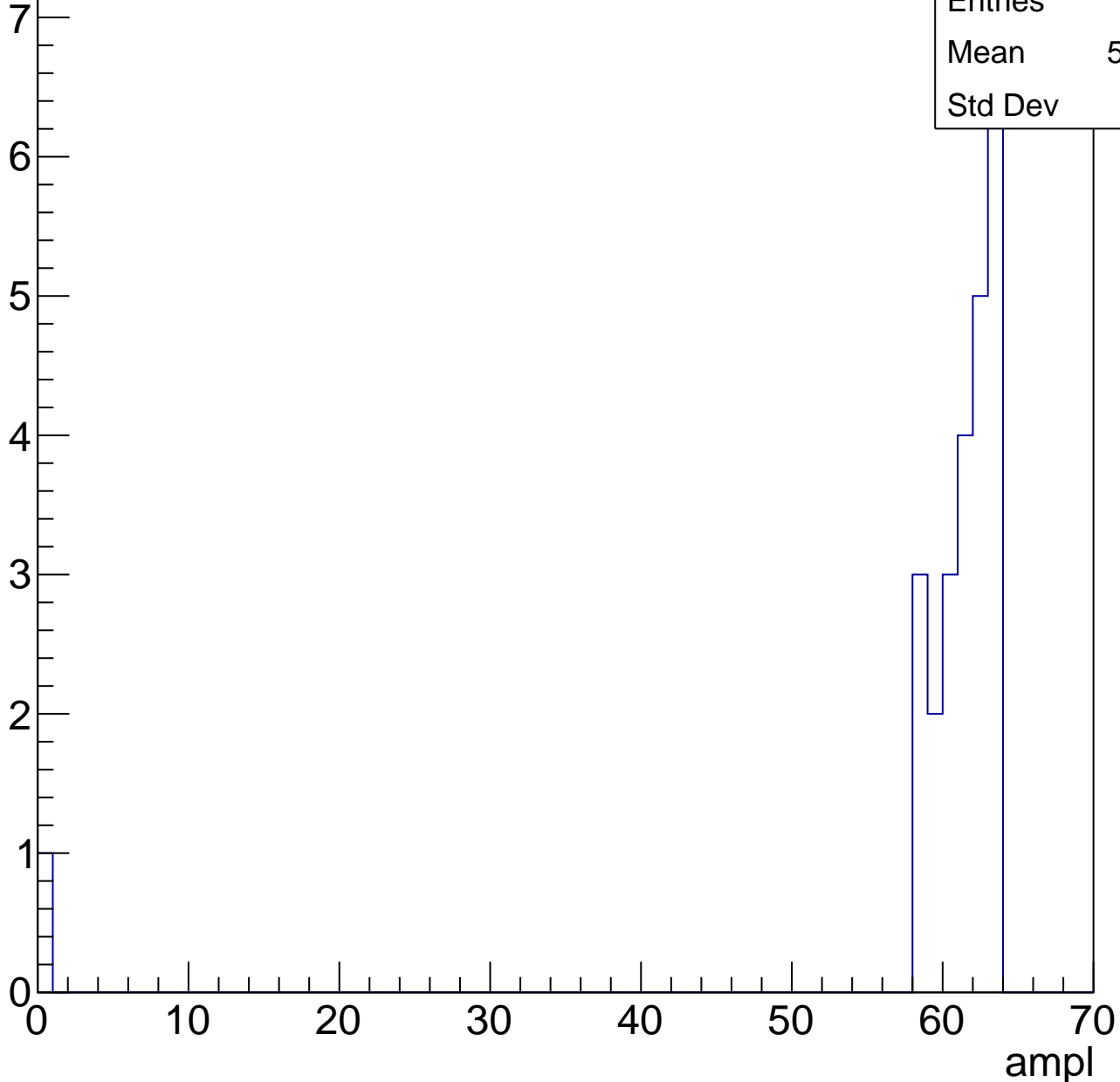


# B1L103S, U26-ch108, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	25
Mean	58.68
Std Dev	12.1

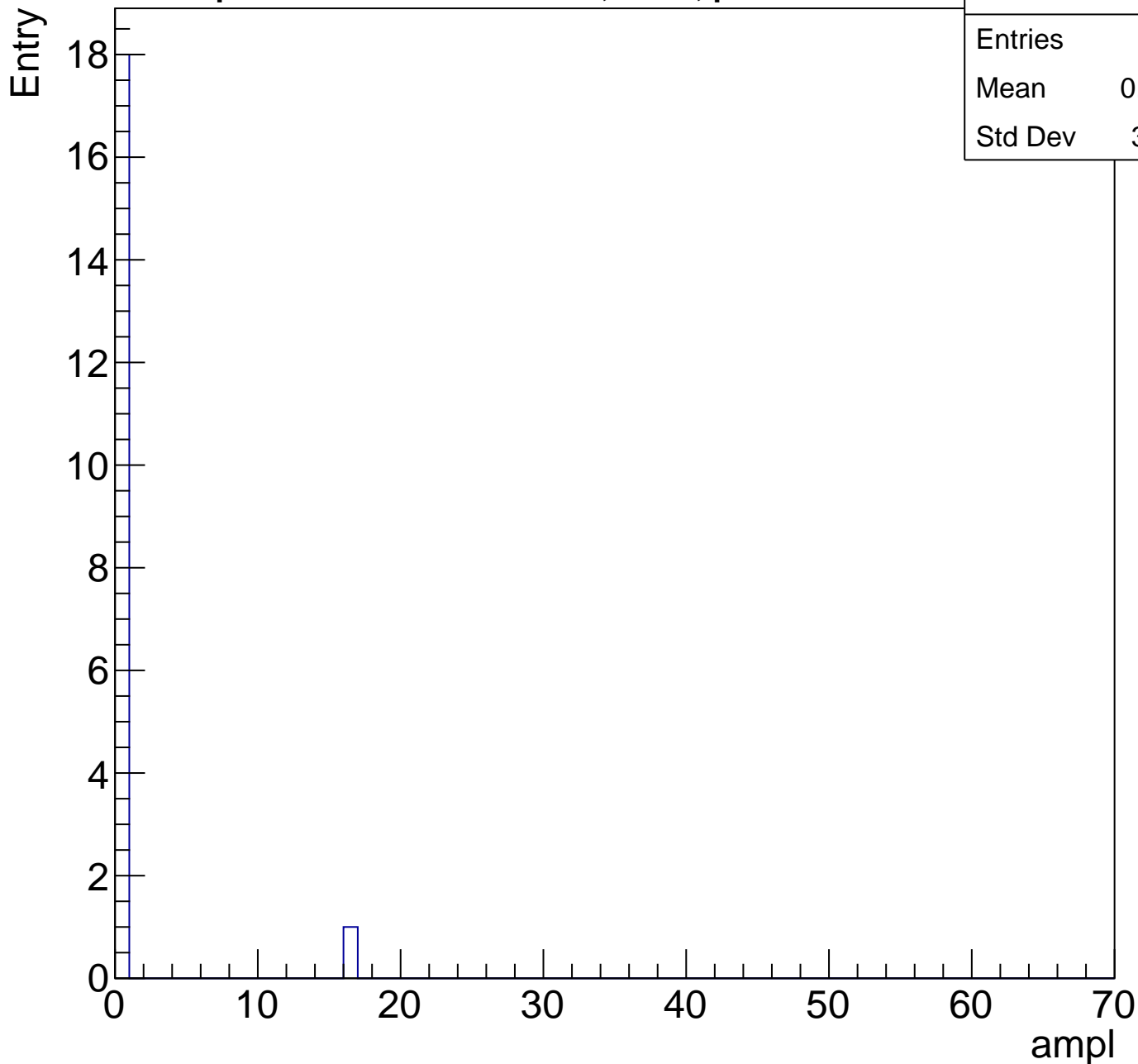




# B1L103S, U26-ch108, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	19
Mean	0.8421
Std Dev	3.573



# B1L103S, U26-ch109, adc0

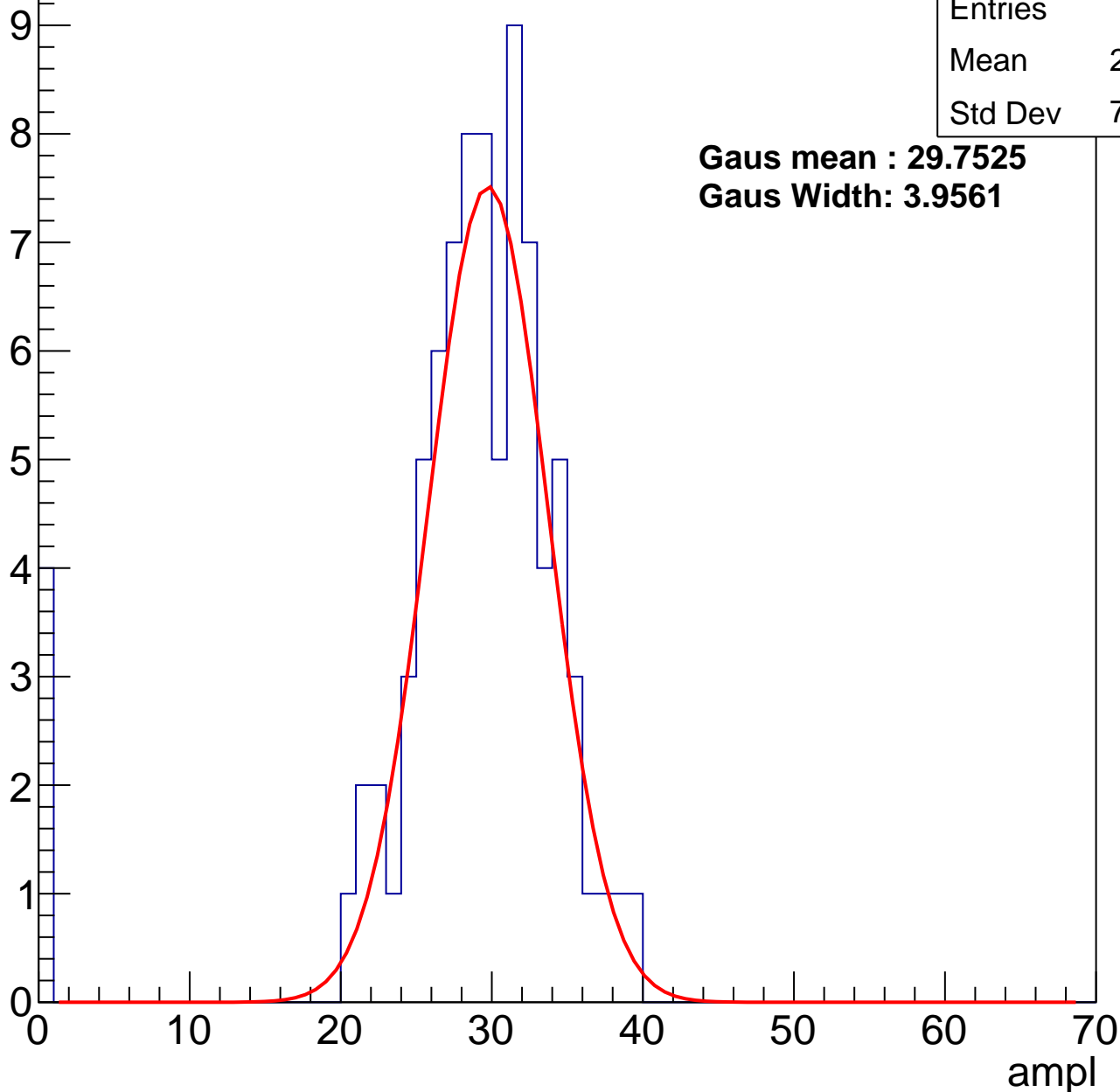
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	84
Mean	27.82
Std Dev	7.344

**Gaus mean : 29.7525**

**Gaus Width: 3.9561**



# B1L103S, U26-ch109, adc1

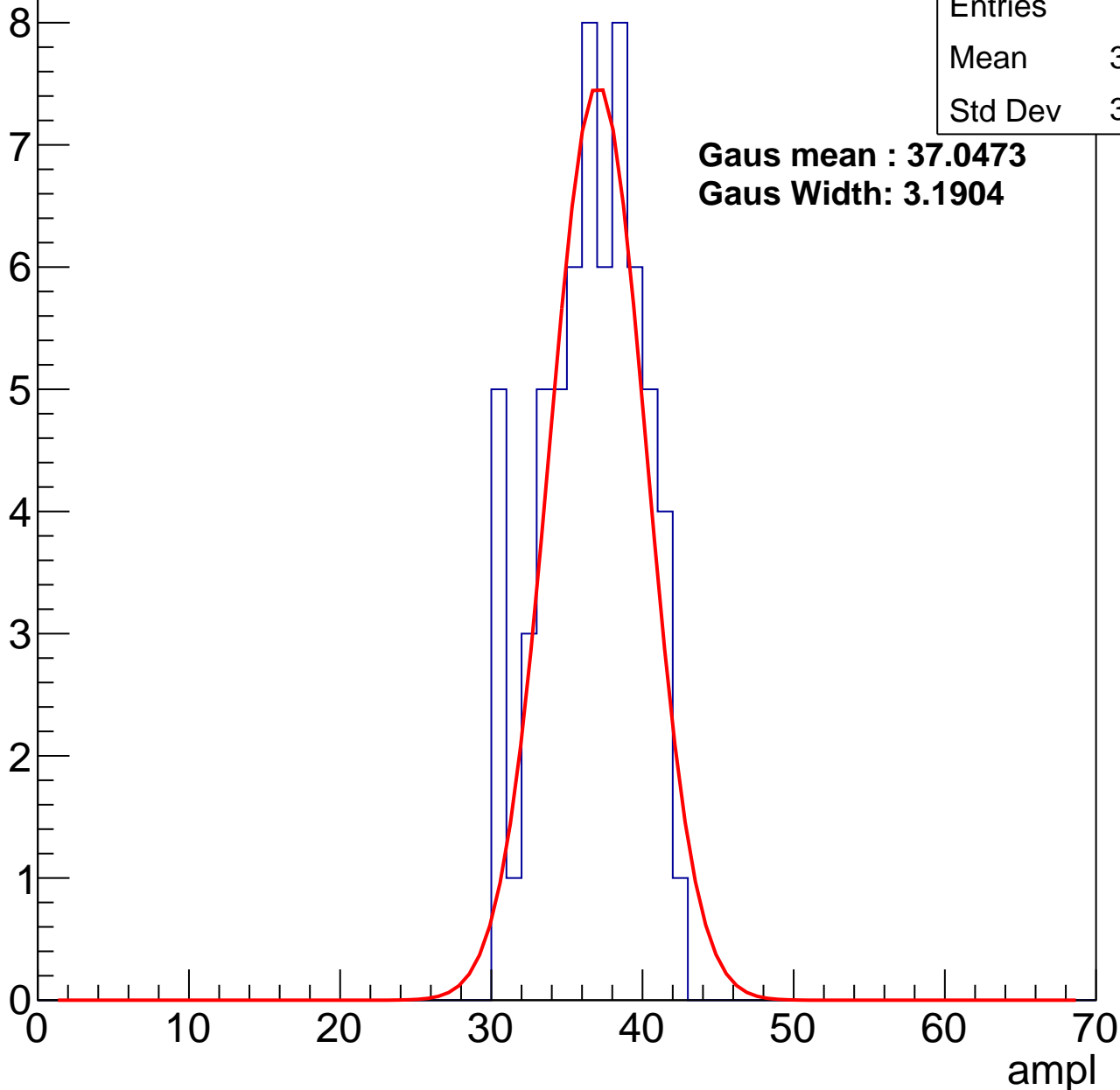
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	63
Mean	36.13
Std Dev	3.165

**Gaus mean : 37.0473**

**Gaus Width: 3.1904**



# B1L103S, U26-ch109, adc2

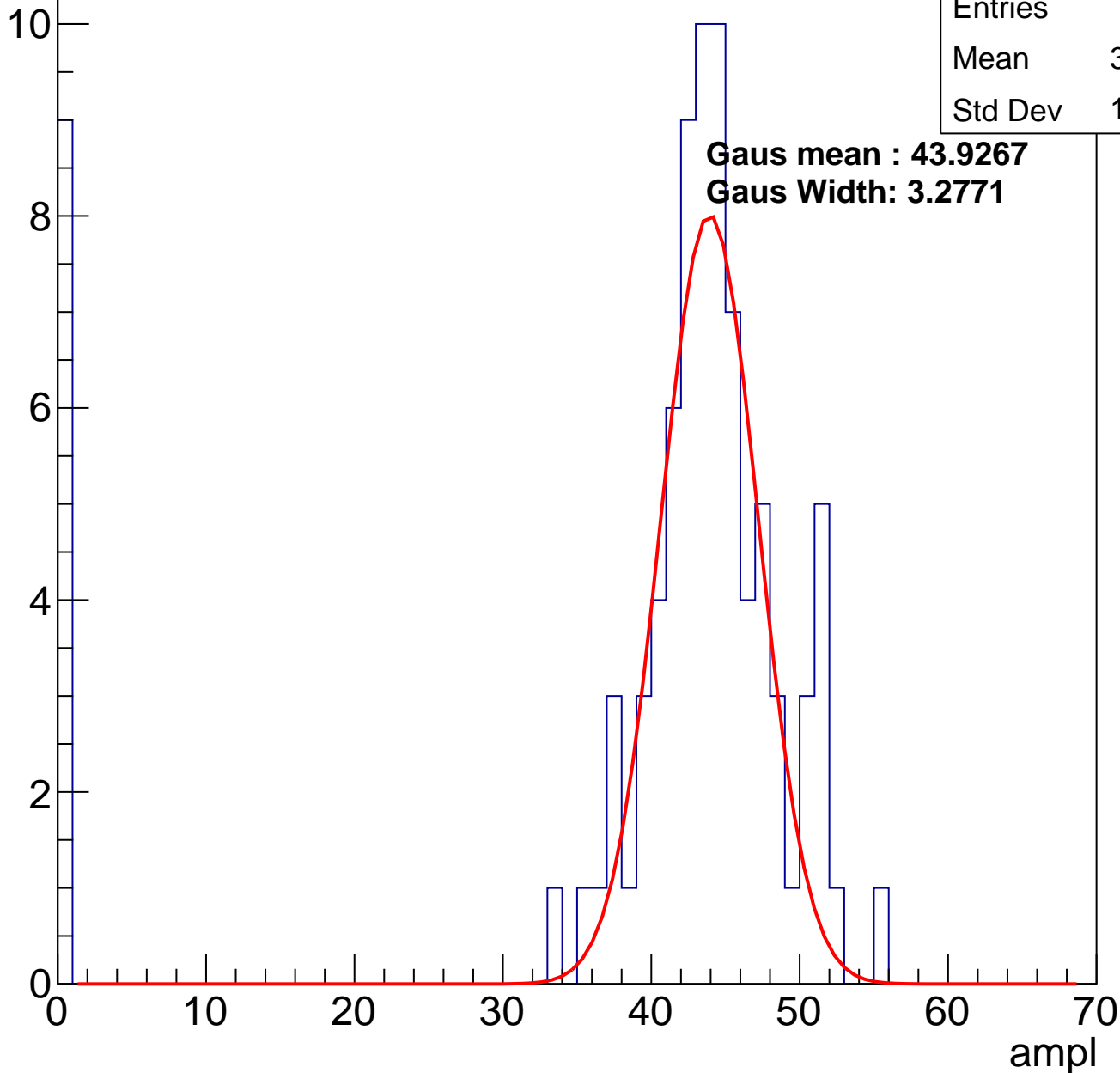
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	88
Mean	39.35
Std Dev	13.85

**Gaus mean : 43.9267**

**Gaus Width: 3.2771**

Entry

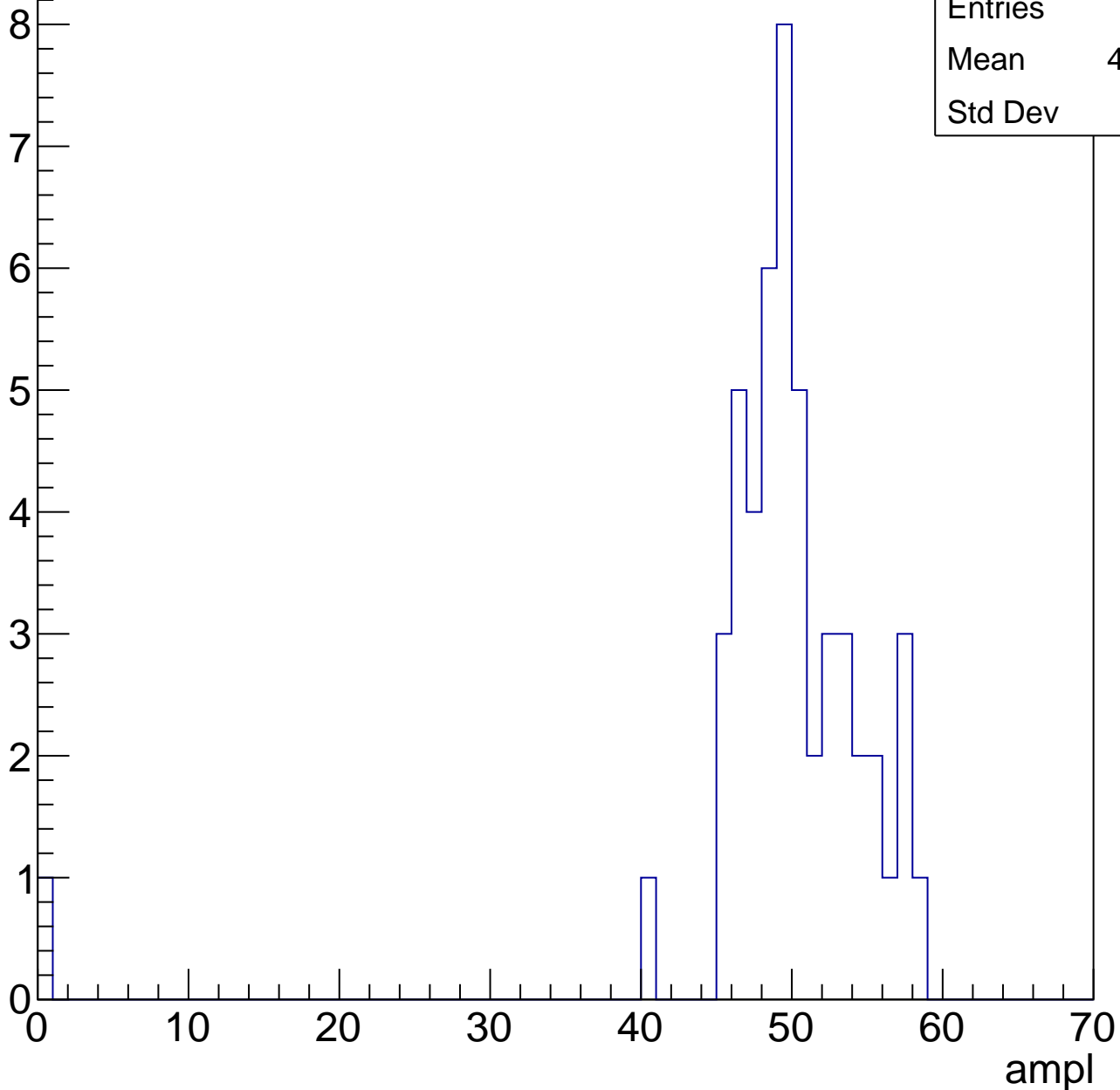


# B1L103S, U26-ch109, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	50
Mean	48.86
Std Dev	7.91

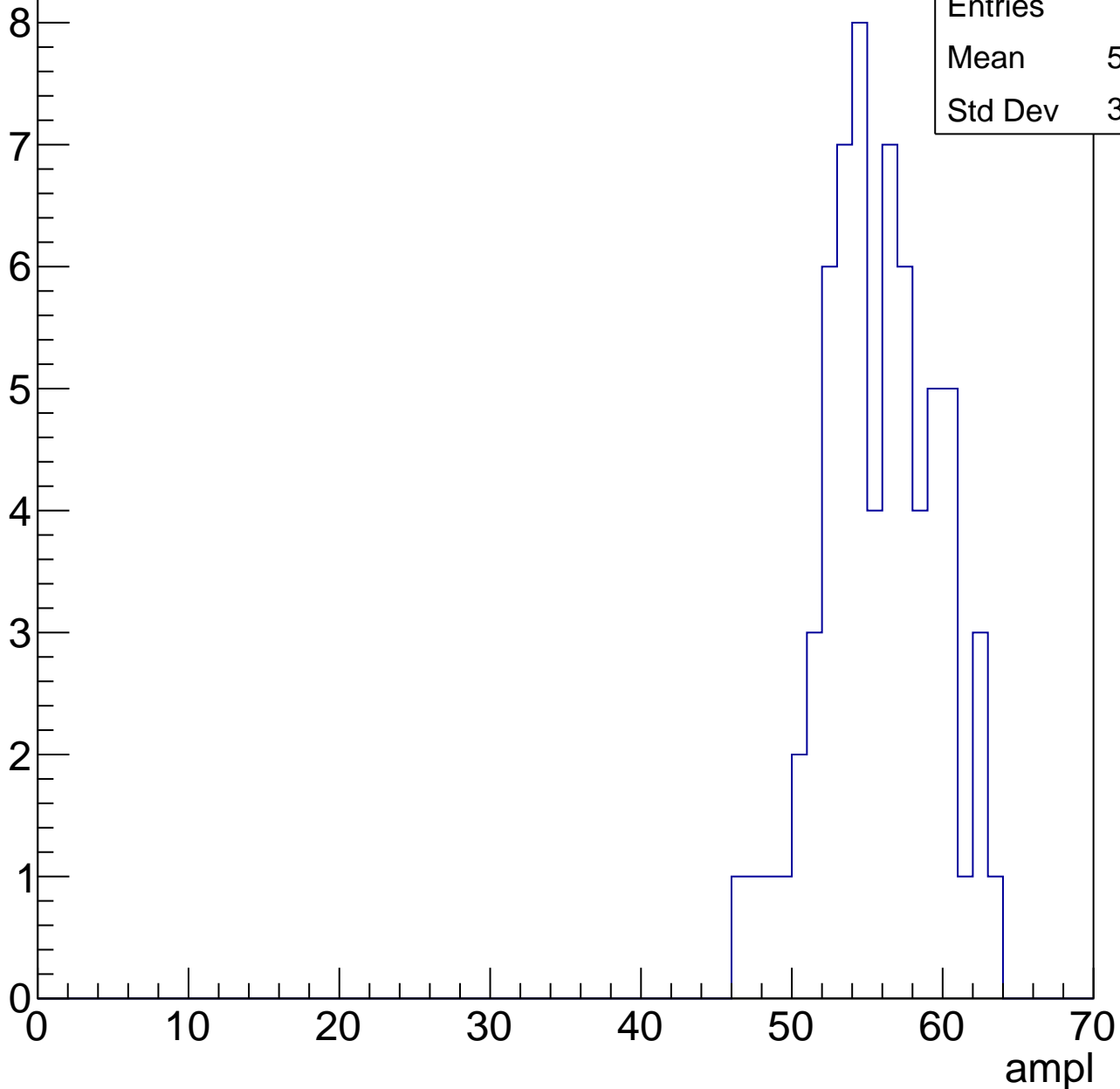


# B1L103S, U26-ch109, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	66
Mean	55.29
Std Dev	3.757

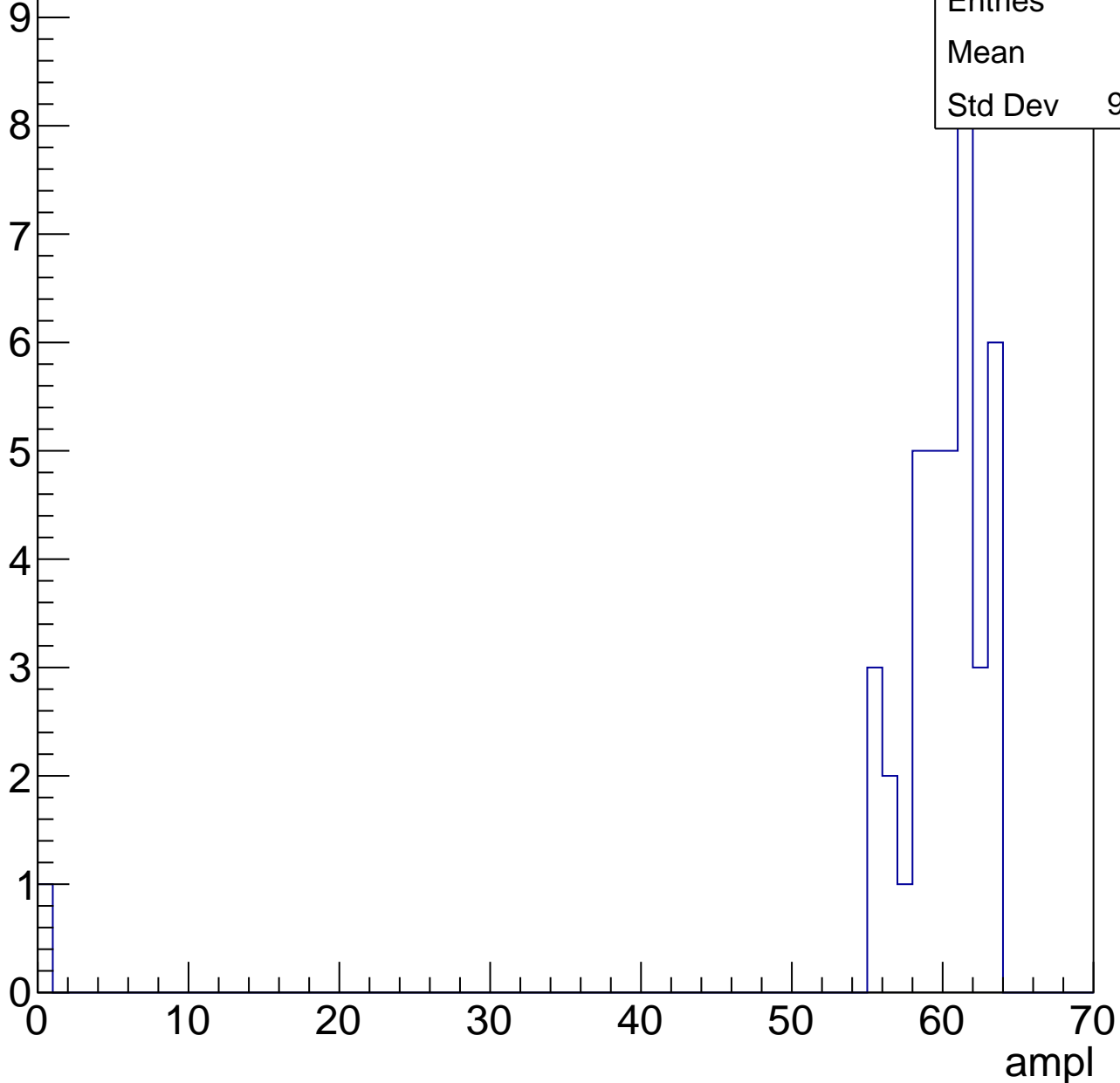


# B1L103S, U26-ch109, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

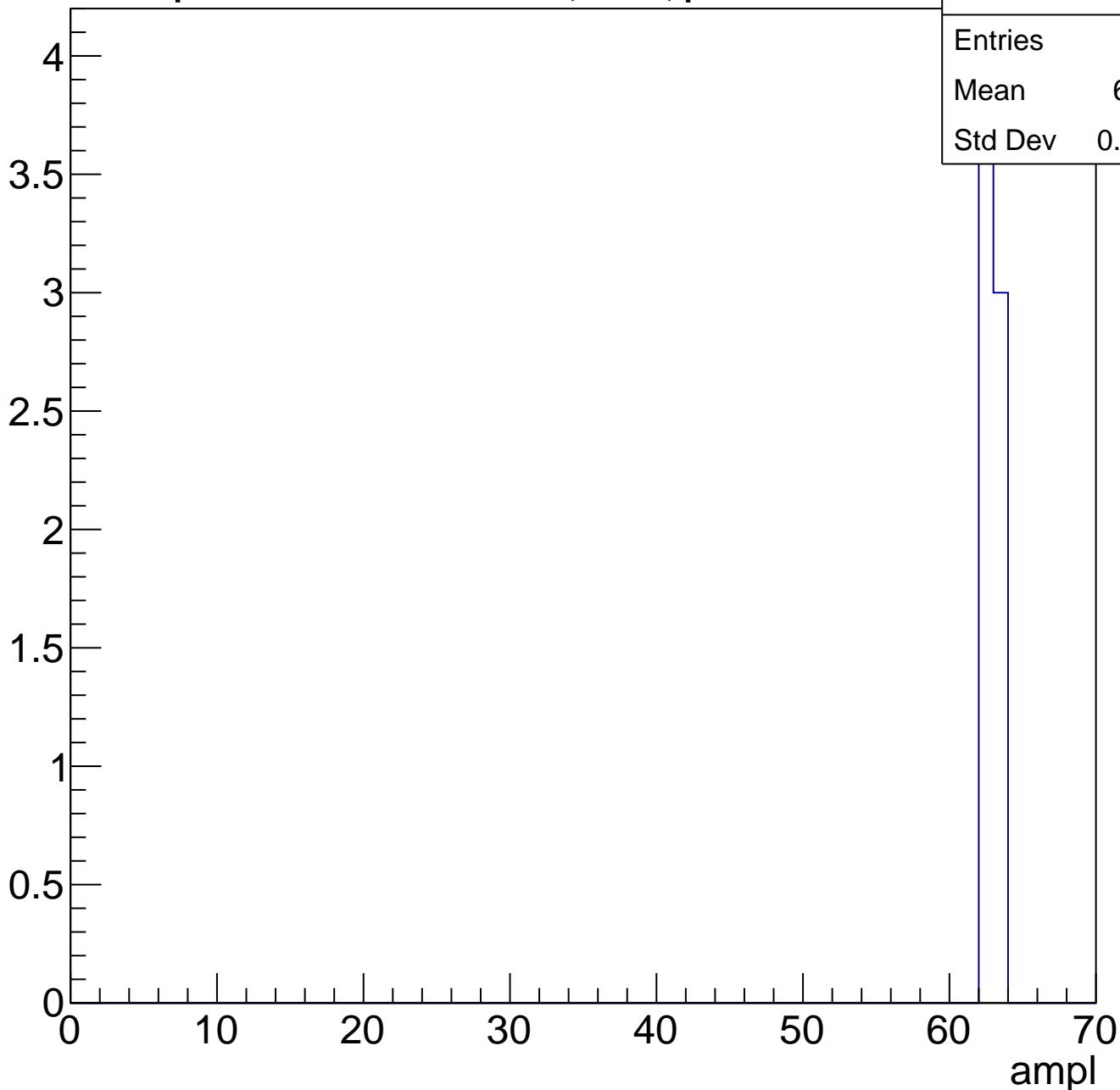
Entries	40
Mean	58.3
Std Dev	9.618



# B1L103S, U26-ch109, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



Entries	7
Mean	62.43
Std Dev	0.4949



# B1L103S, U26-ch109, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

18  
16  
14  
12  
10  
8  
6  
4  
2  
0

Entries	18
Mean	0
Std Dev	0

ampl

# B1L103S, U26-ch110, adc0

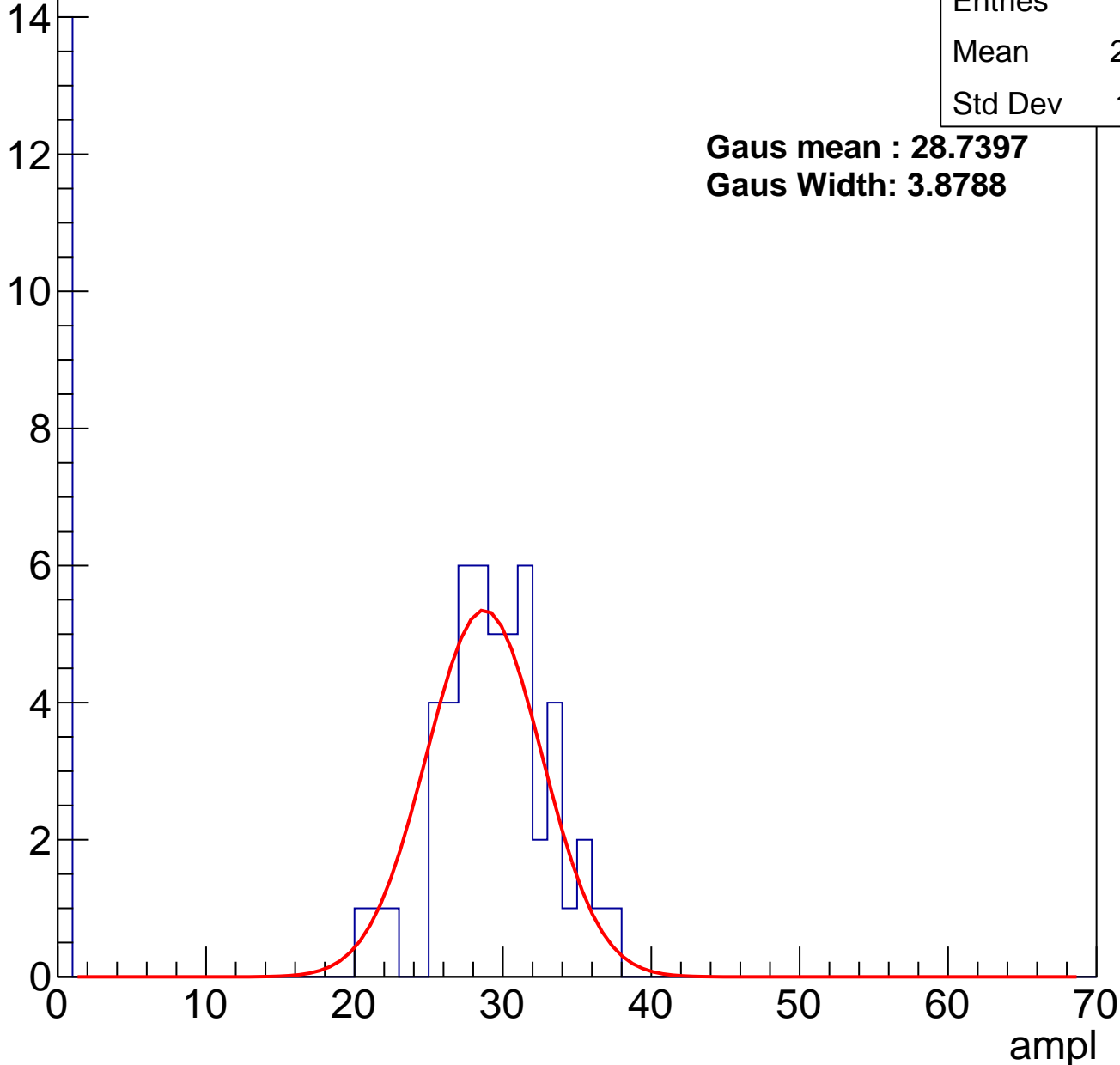
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	64
Mean	22.67
Std Dev	12.41

**Gaus mean : 28.7397**

**Gaus Width: 3.8788**

Entry



# B1L103S, U26-ch110, adc1

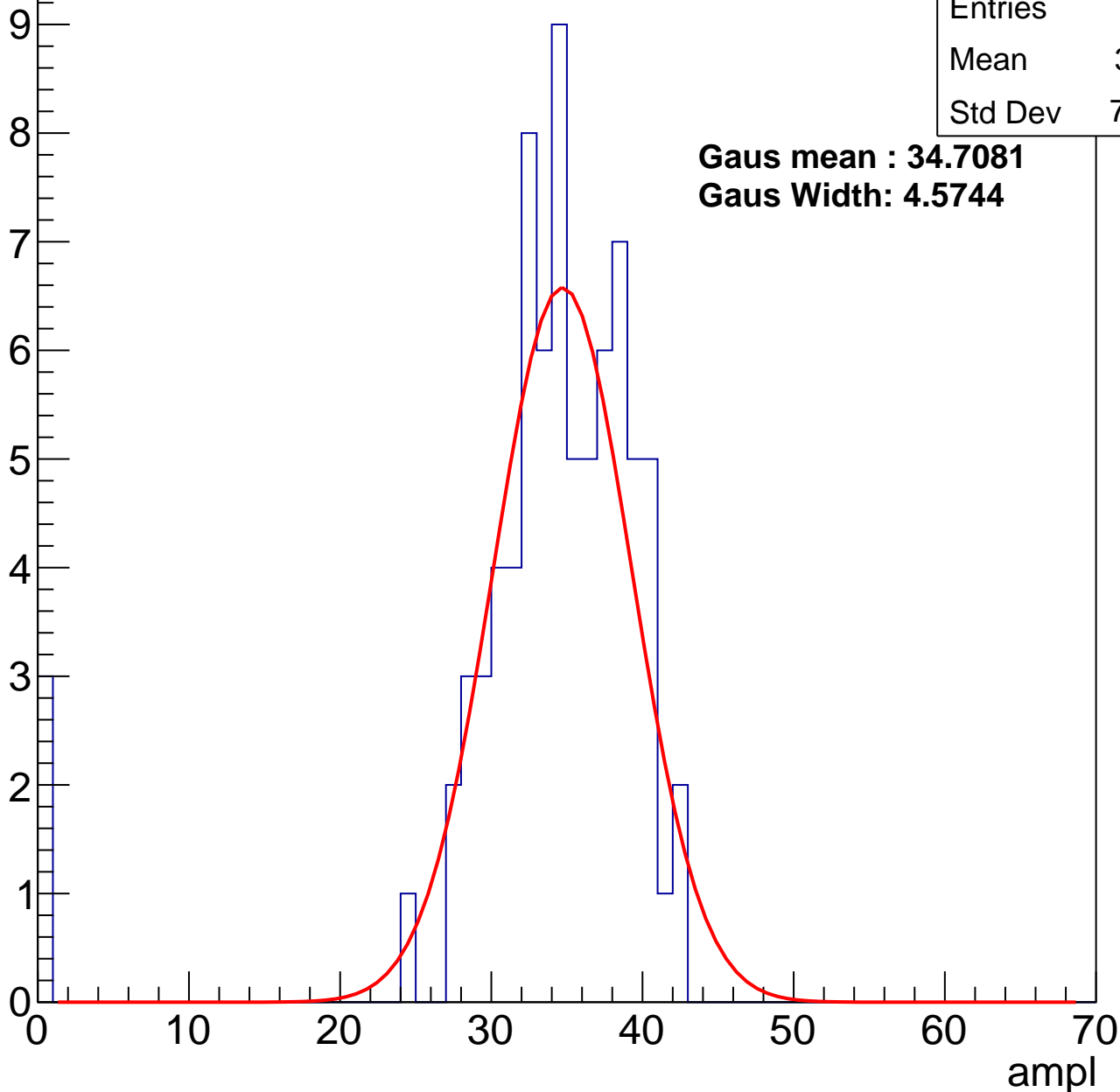
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	79
Mean	33.11
Std Dev	7.629

**Gaus mean : 34.7081**

**Gaus Width: 4.5744**



# B1L103S, U26-ch110, adc2

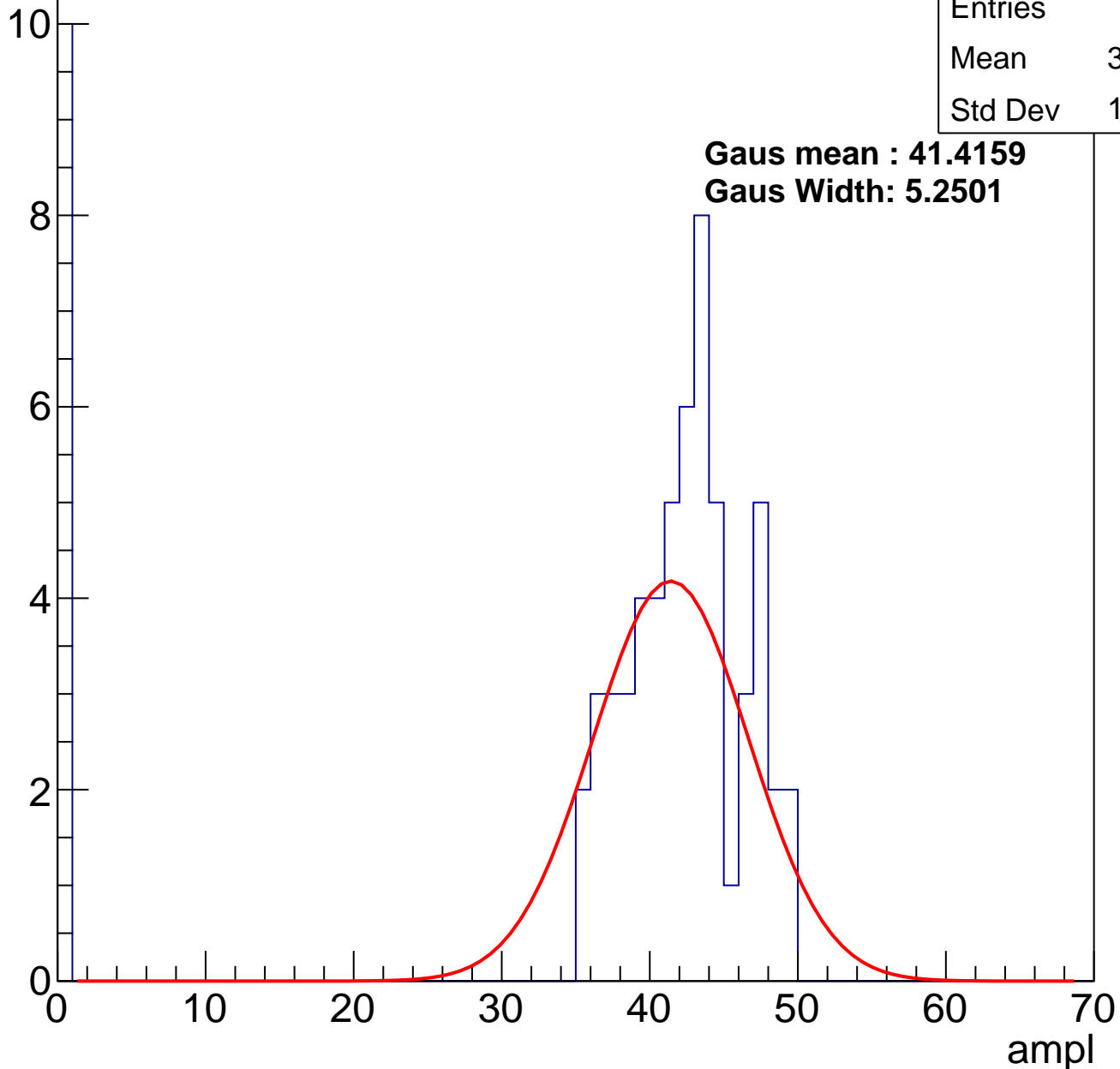
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	66
Mean	35.64
Std Dev	15.44

**Gaus mean : 41.4159**

**Gaus Width: 5.2501**

Entry

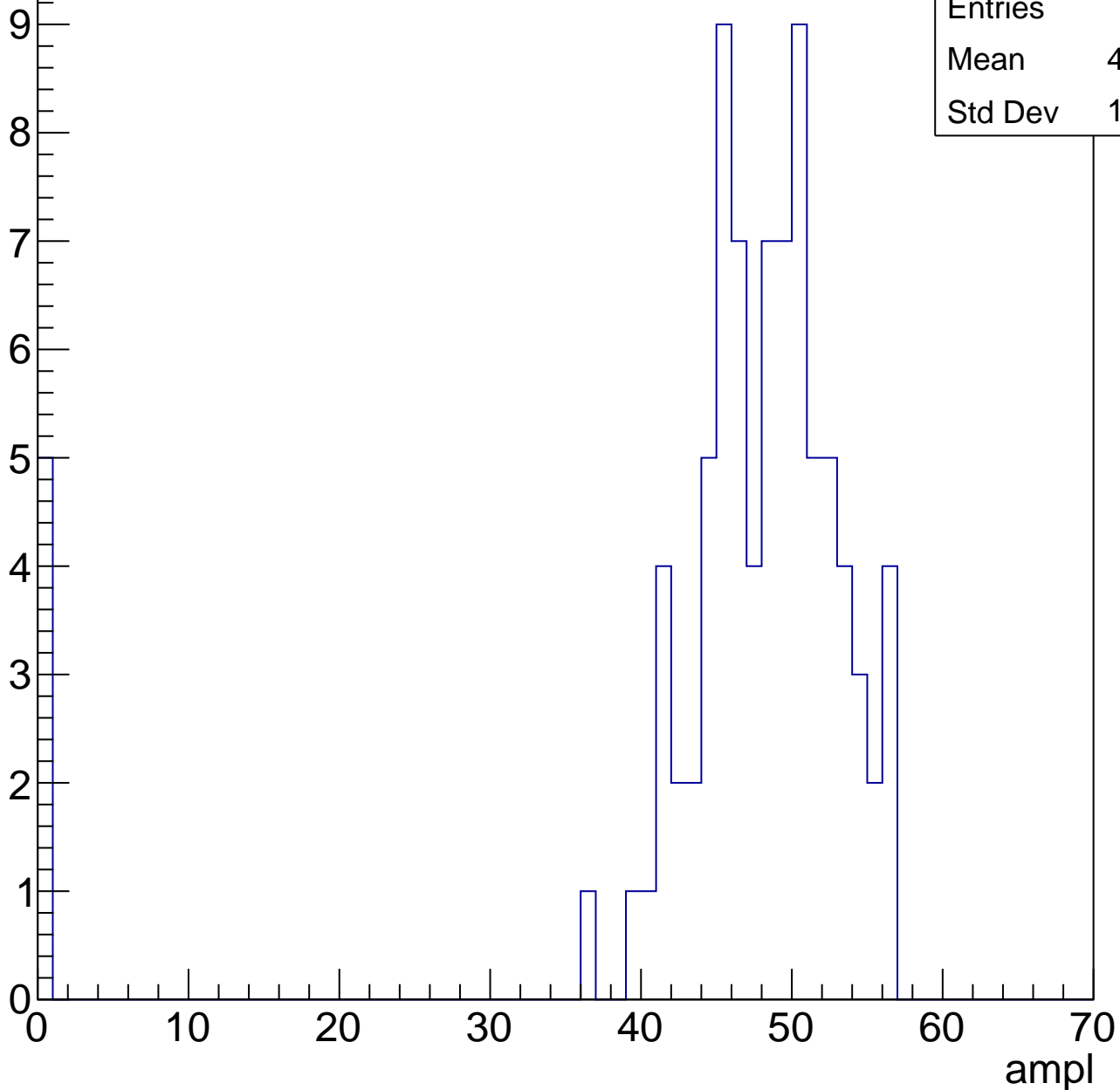


# B1L103S, U26-ch110, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	87
Mean	45.24
Std Dev	11.93

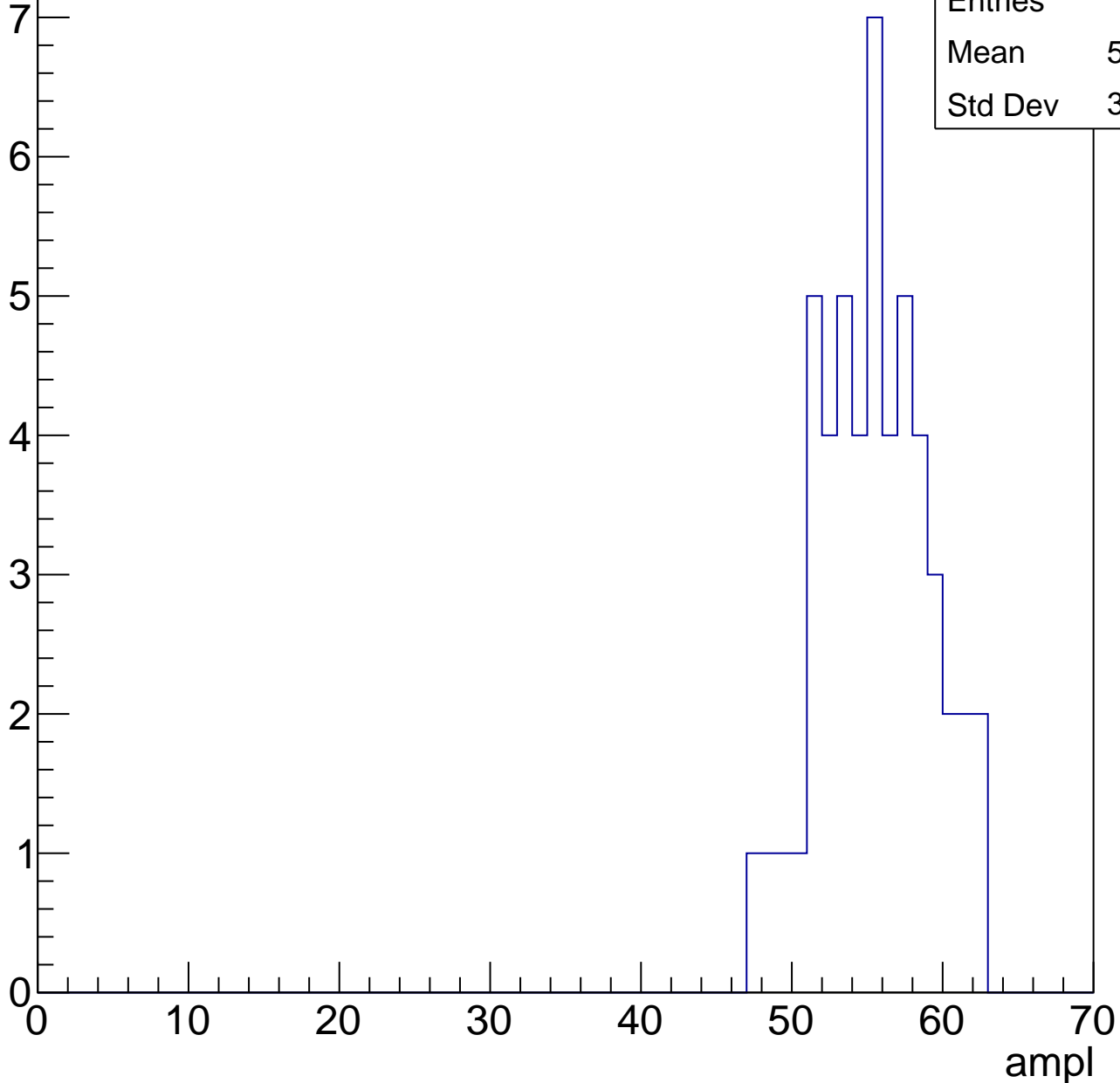


# B1L103S, U26-ch110, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	51
Mean	55.04
Std Dev	3.548

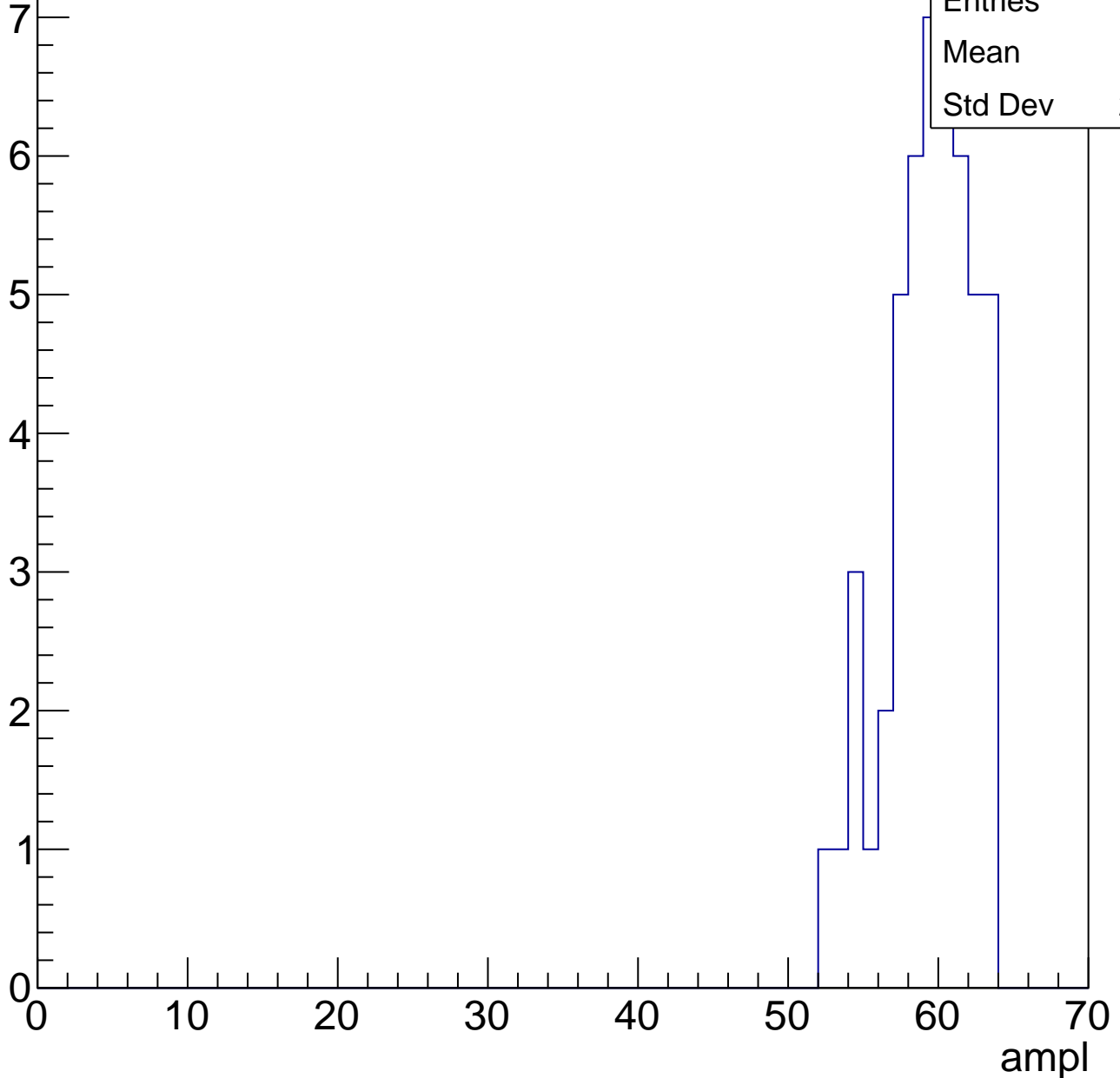


# B1L103S, U26-ch110, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	49
Mean	59
Std Dev	2.77



# B1L103S, U26-ch110, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



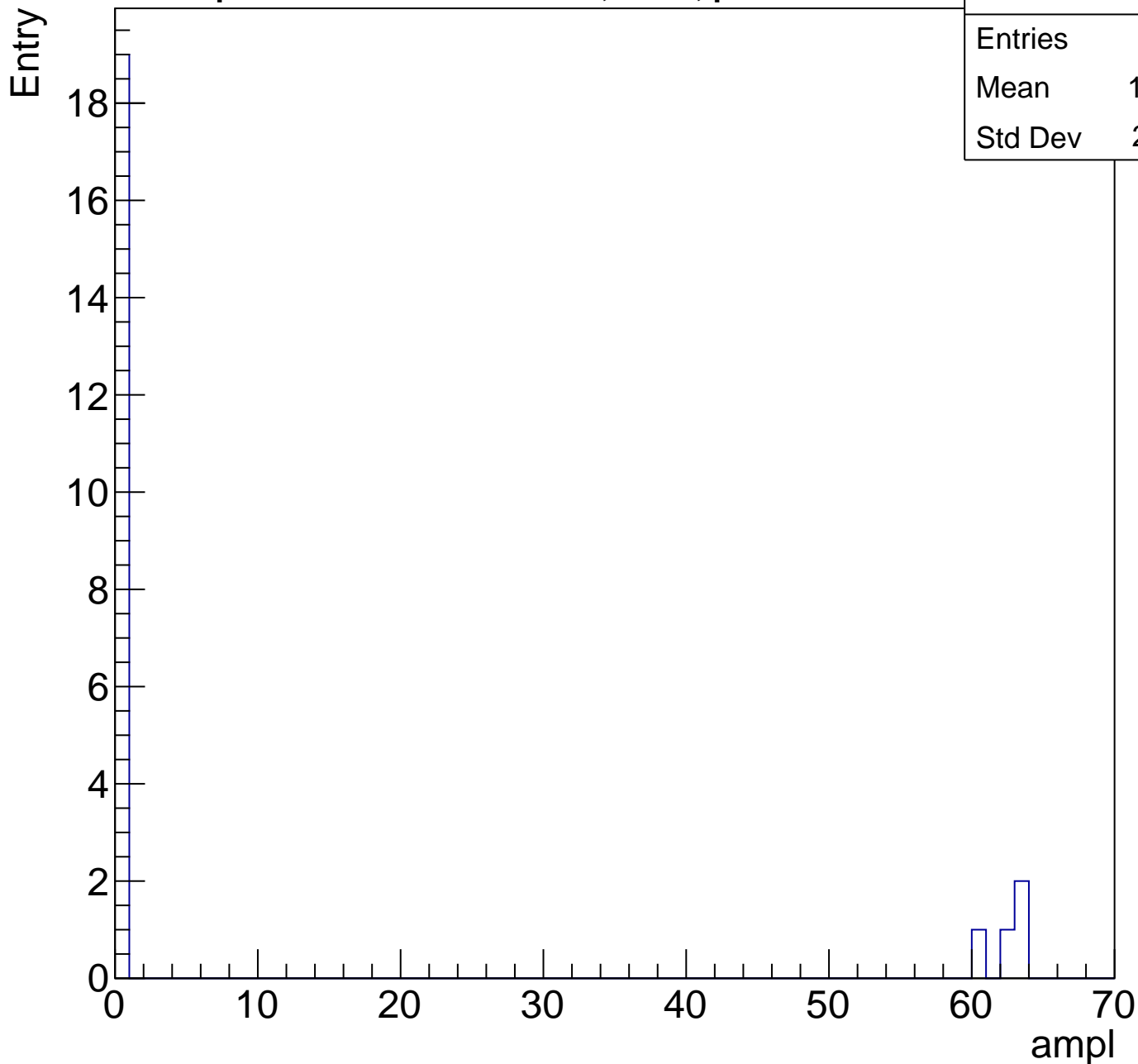
Entries	7
Mean	62.14
Std Dev	0.833



# B1L103S, U26-ch110, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	23
Mean	10.78
Std Dev	23.51



# B1L103S, U26-ch111, adc0

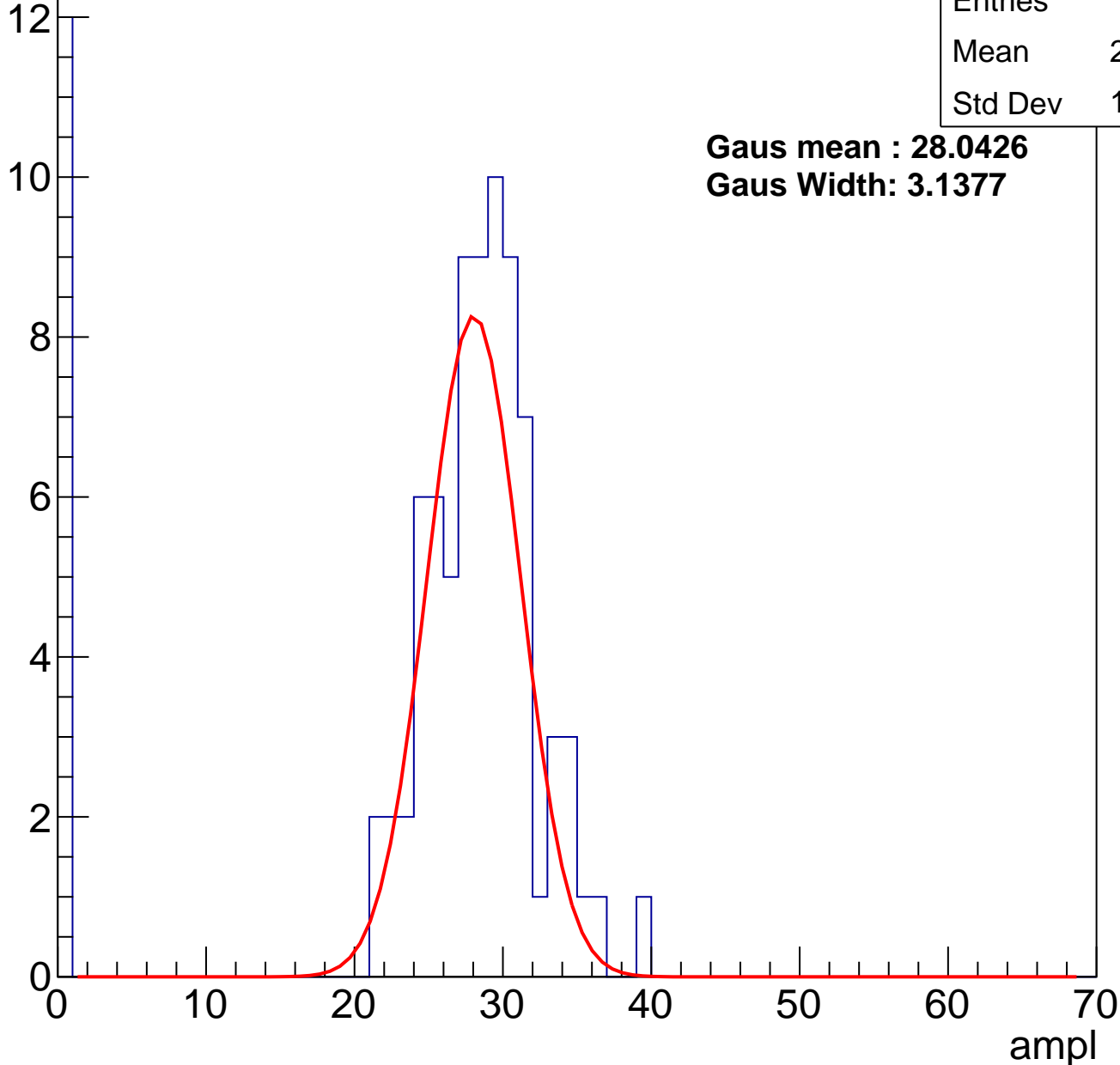
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	89
Mean	24.39
Std Dev	10.16

**Gaus mean : 28.0426**

**Gaus Width: 3.1377**

Entry



# B1L103S, U26-ch111, adc1

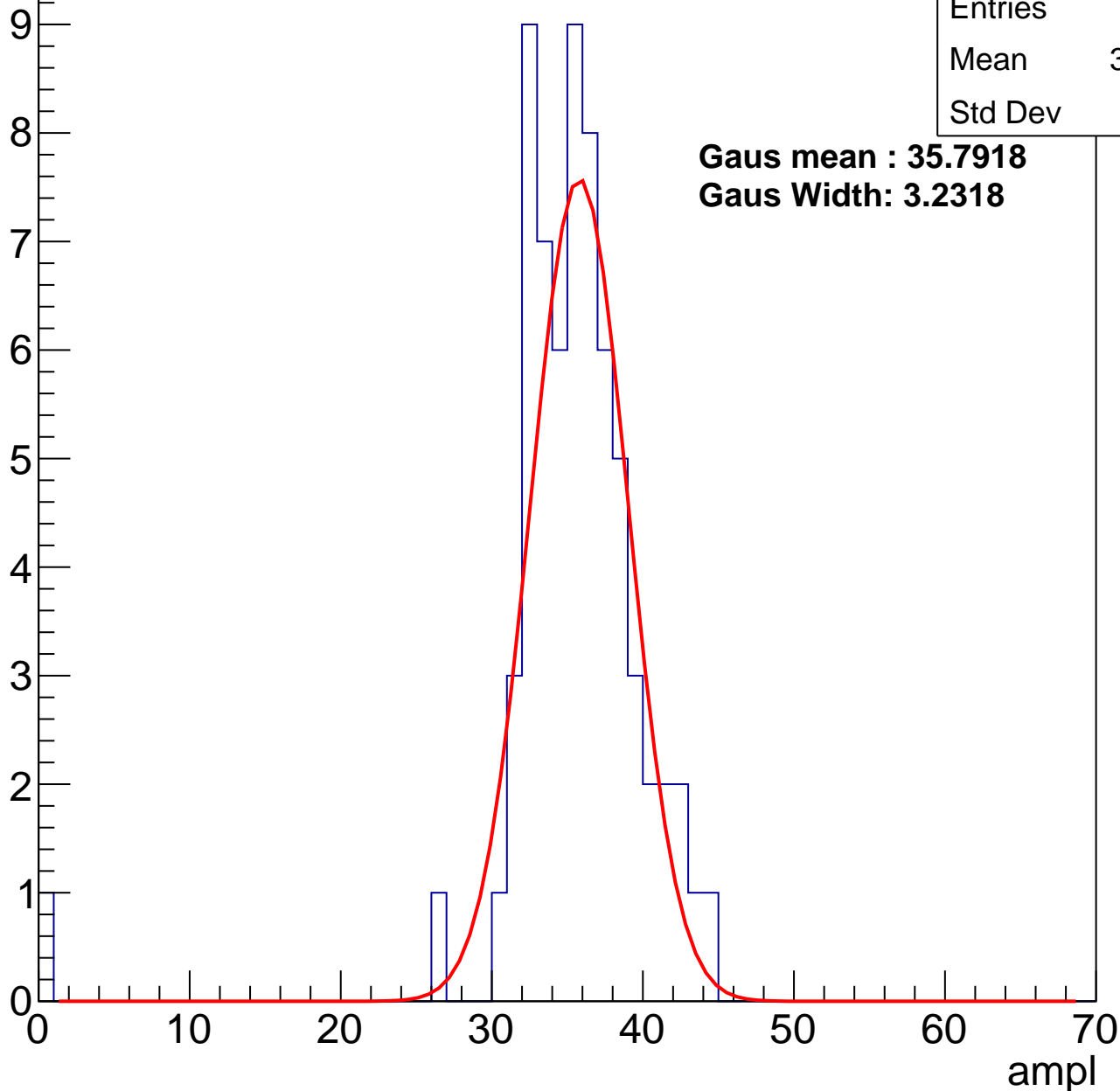
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	67
Mean	34.88
Std Dev	5.44

**Gaus mean : 35.7918**

**Gaus Width: 3.2318**



# B1L103S, U26-ch111, adc2

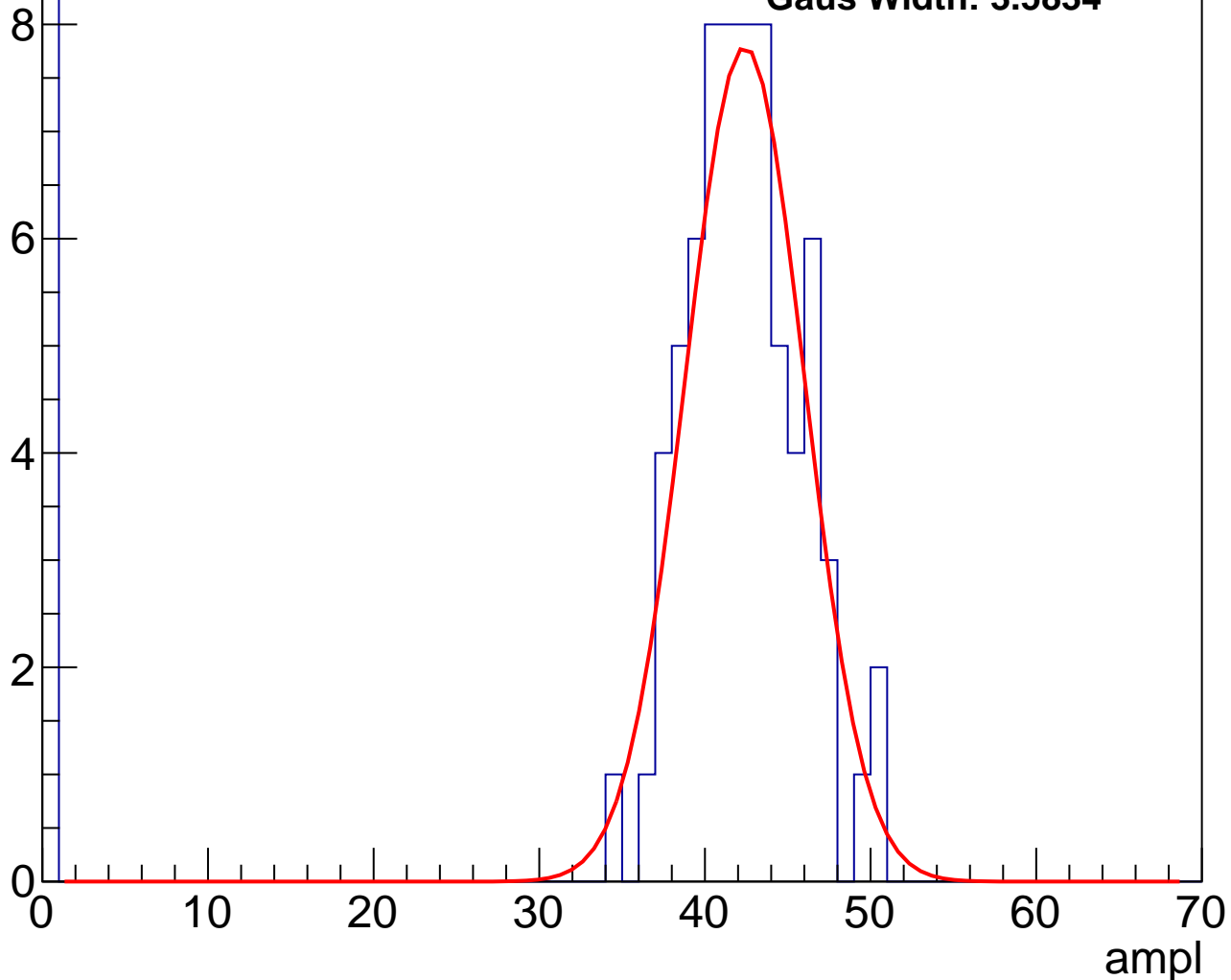
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	80
Mean	36.7
Std Dev	14.22

**Gaus mean : 42.4108**

**Gaus Width: 3.5834**



# B1L103S, U26-ch111, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	60
Mean	44.42
Std Dev	13.66

Entry

10

8

6

4

2

0

0

10

20

30

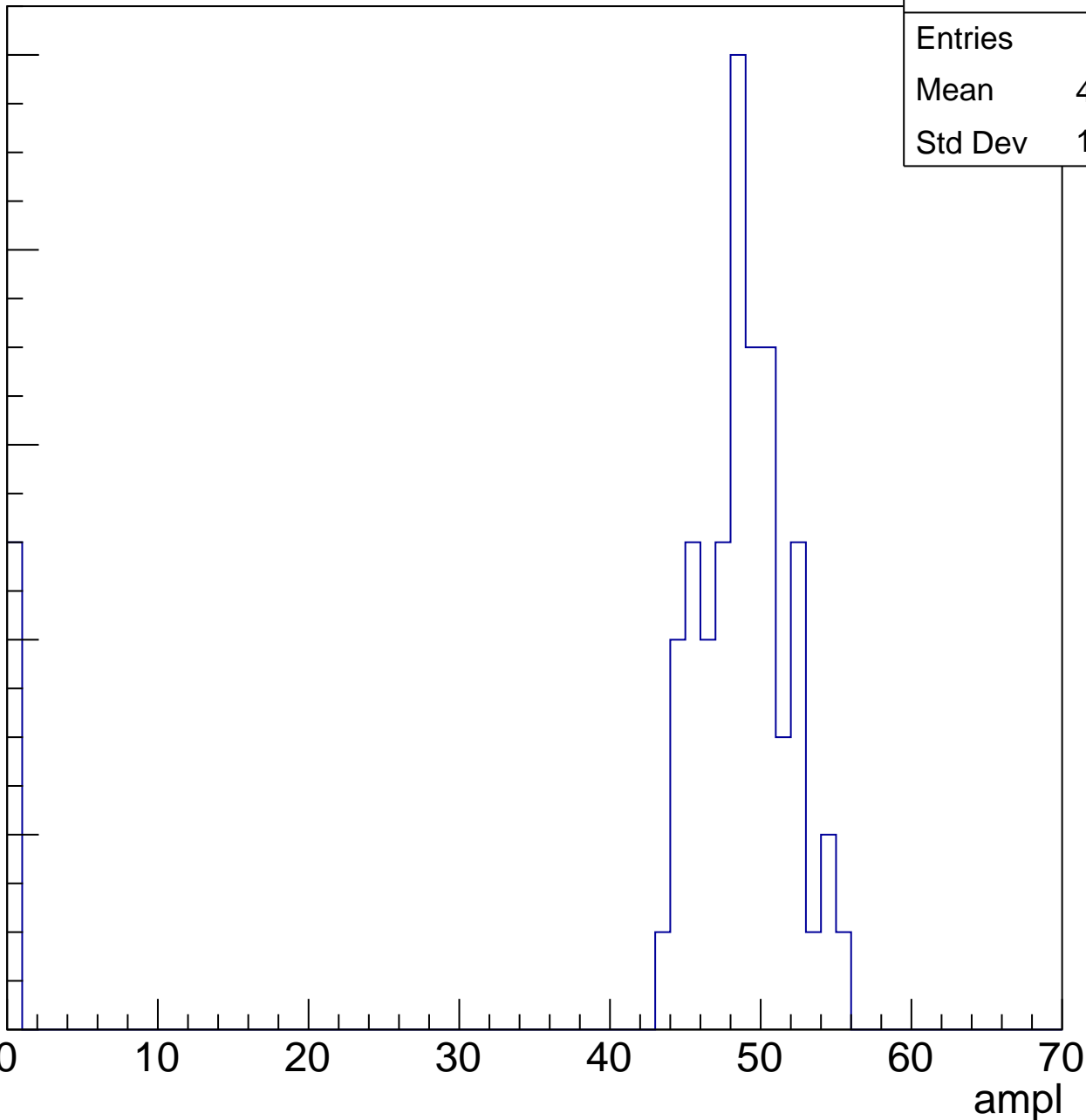
40

50

60

70

ampl

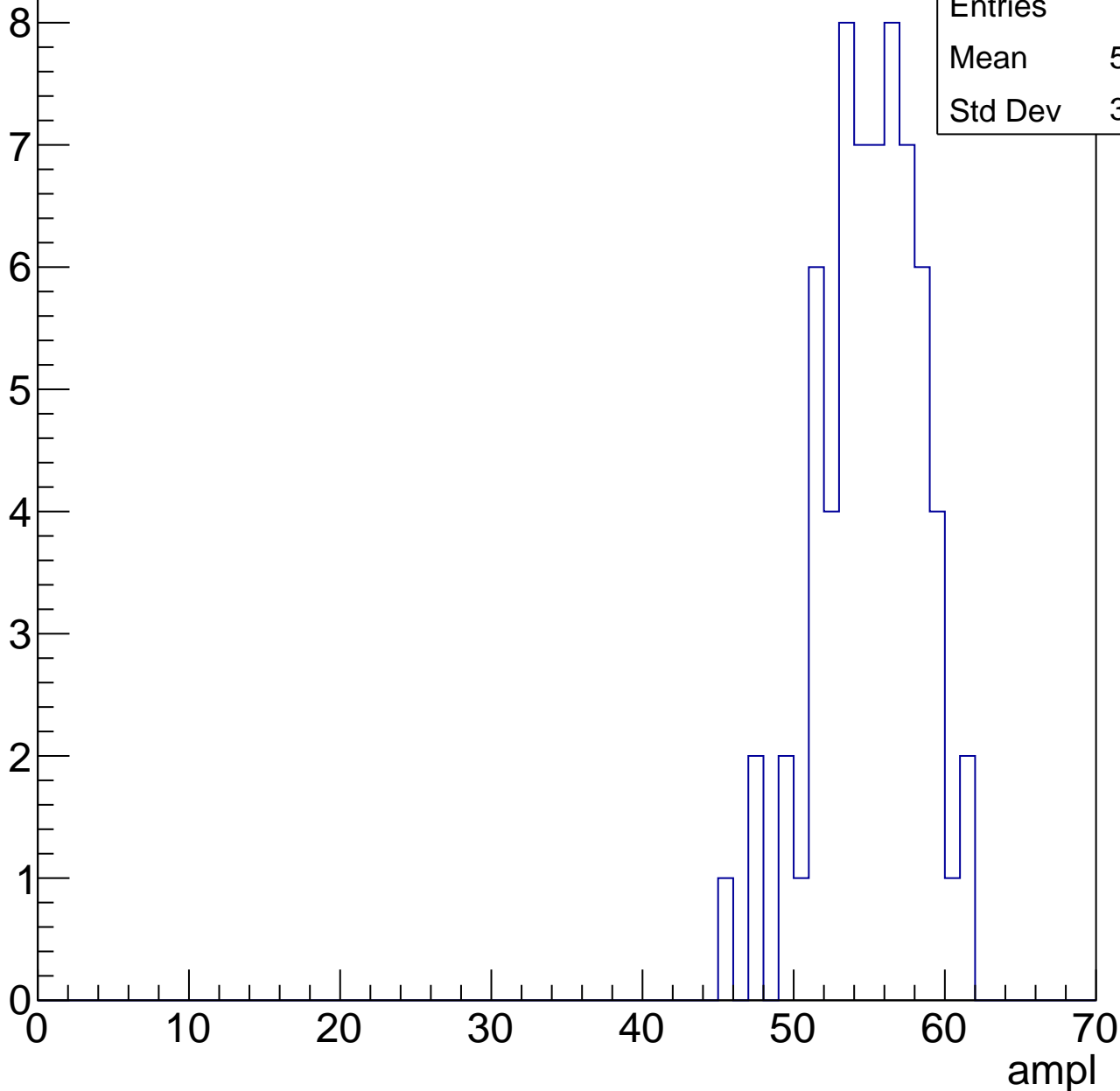


# B1L103S, U26-ch111, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

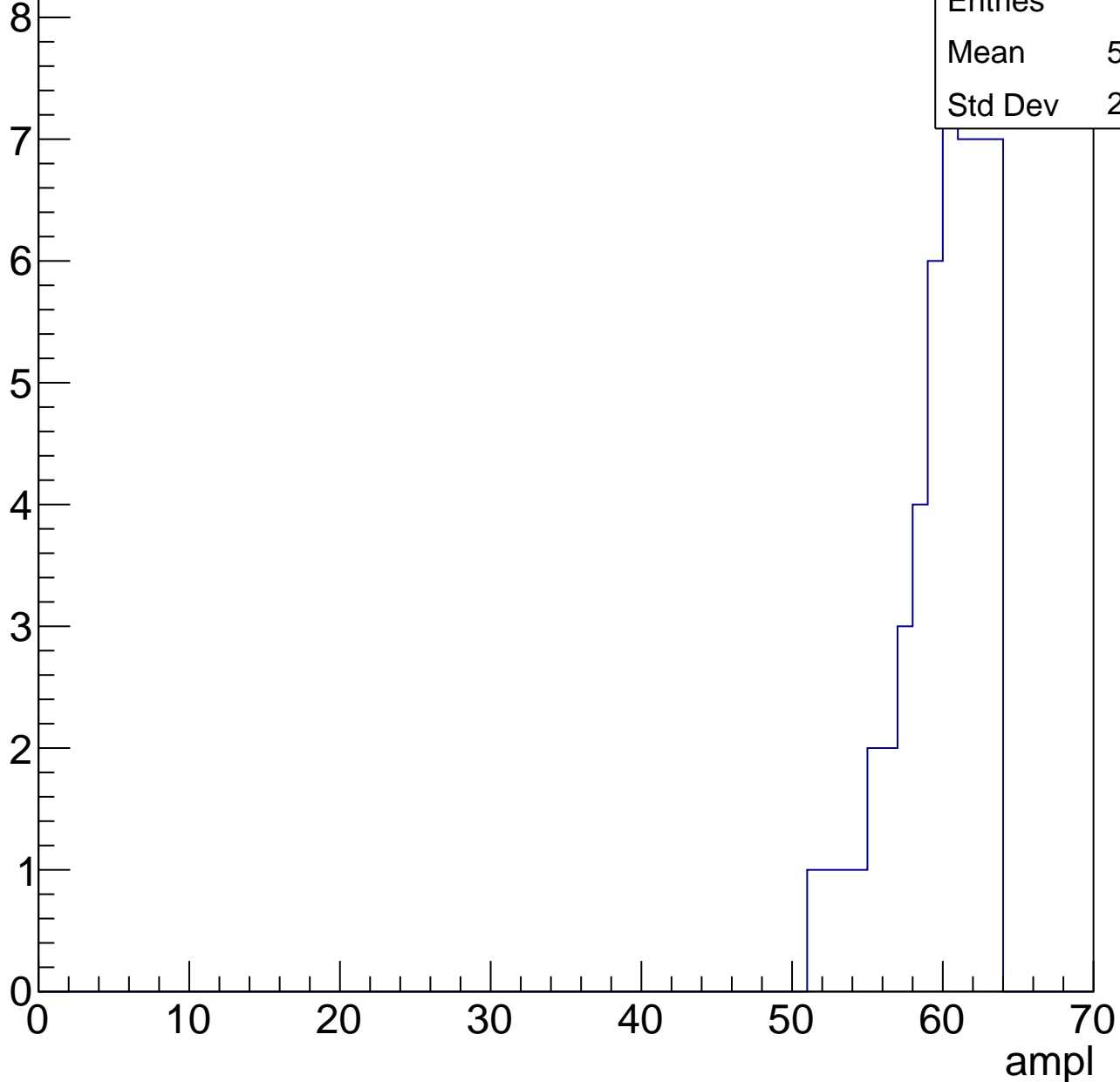
Entries	66
Mean	54.56
Std Dev	3.335



# B1L103S, U26-ch111, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

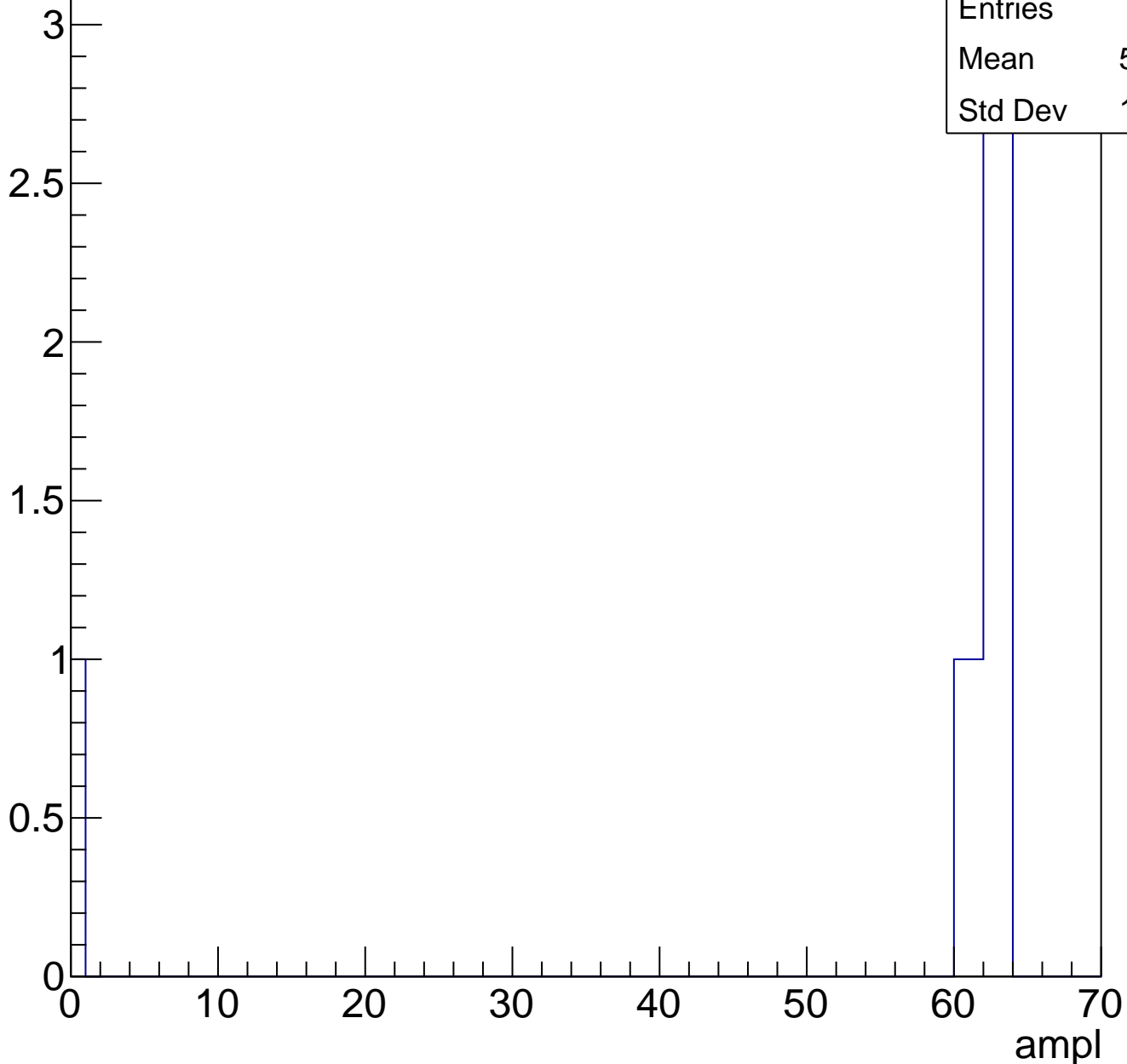


Entries	50
Mean	59.42
Std Dev	2.974

# B1L103S, U26-ch111, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry





# B1L103S, U26-ch111, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

18  
16  
14  
12  
10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

Entries	19
Mean	0
Std Dev	0

# B1L103S, U26-ch112, adc0

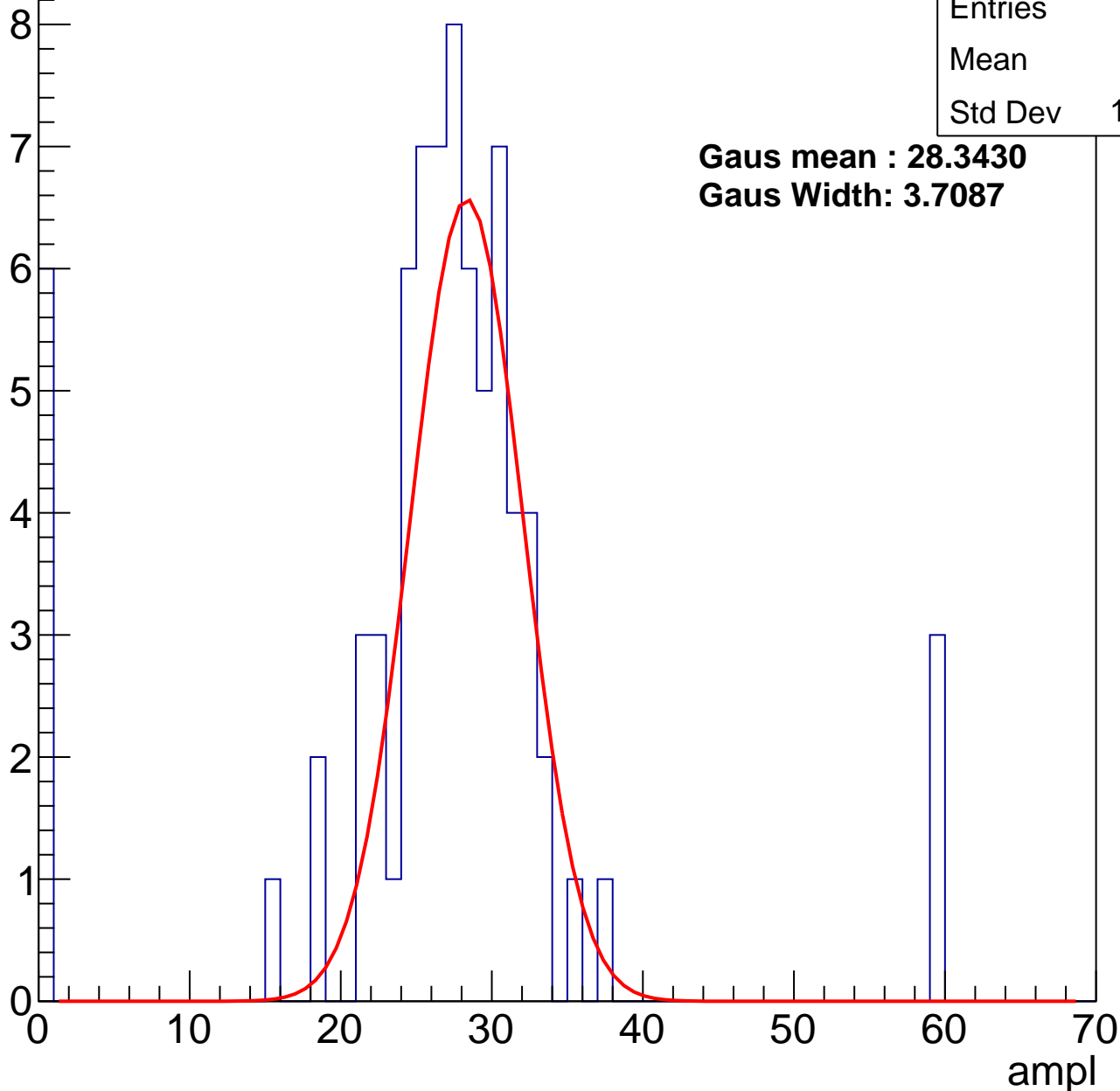
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	77
Mean	26.1
Std Dev	10.49

**Gaus mean : 28.3430**

**Gaus Width: 3.7087**



# B1L103S, U26-ch112, adc1

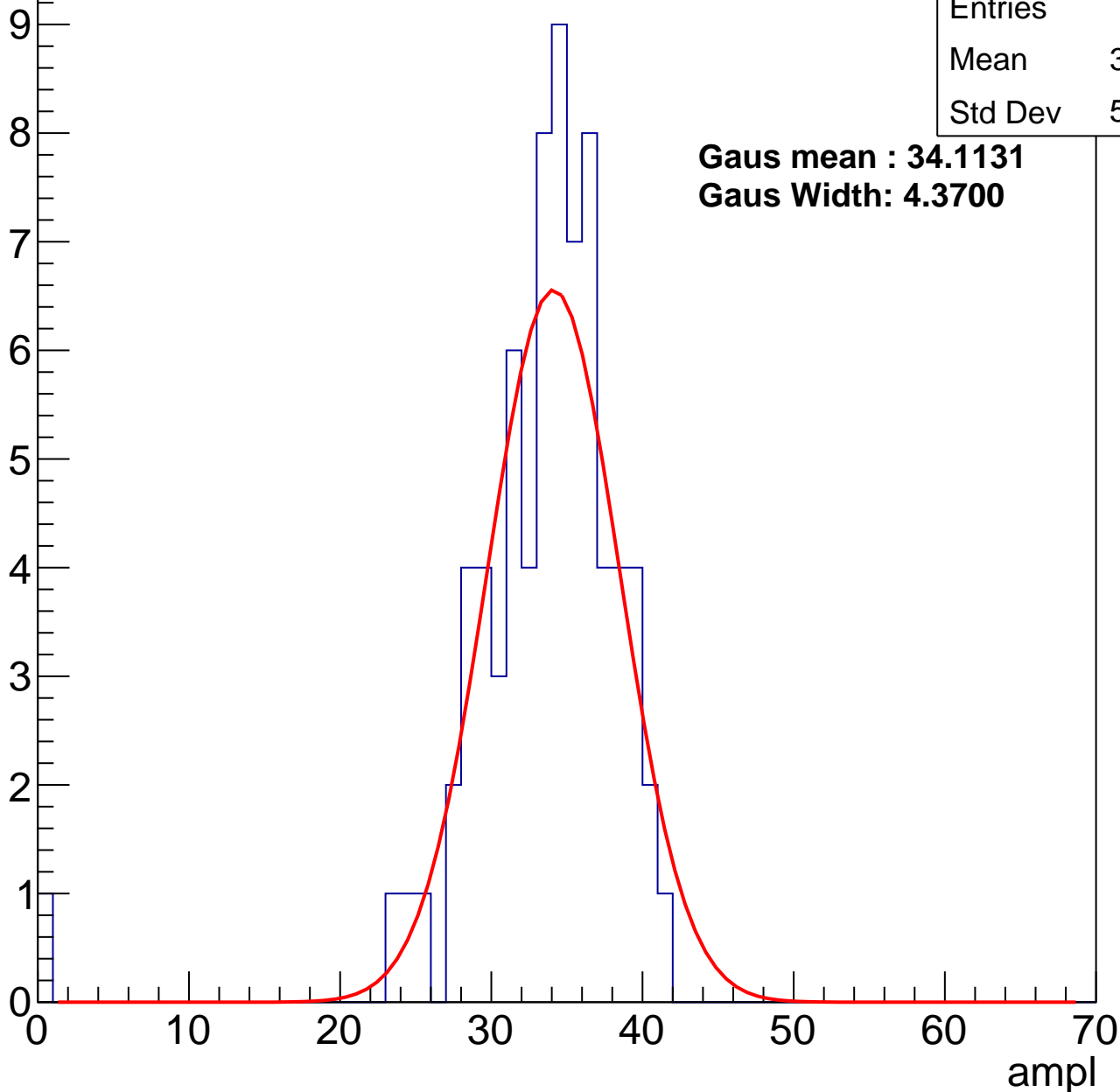
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	74
Mean	32.95
Std Dev	5.457

**Gaus mean : 34.1131**

**Gaus Width: 4.3700**



# B1L103S, U26-ch112, adc2

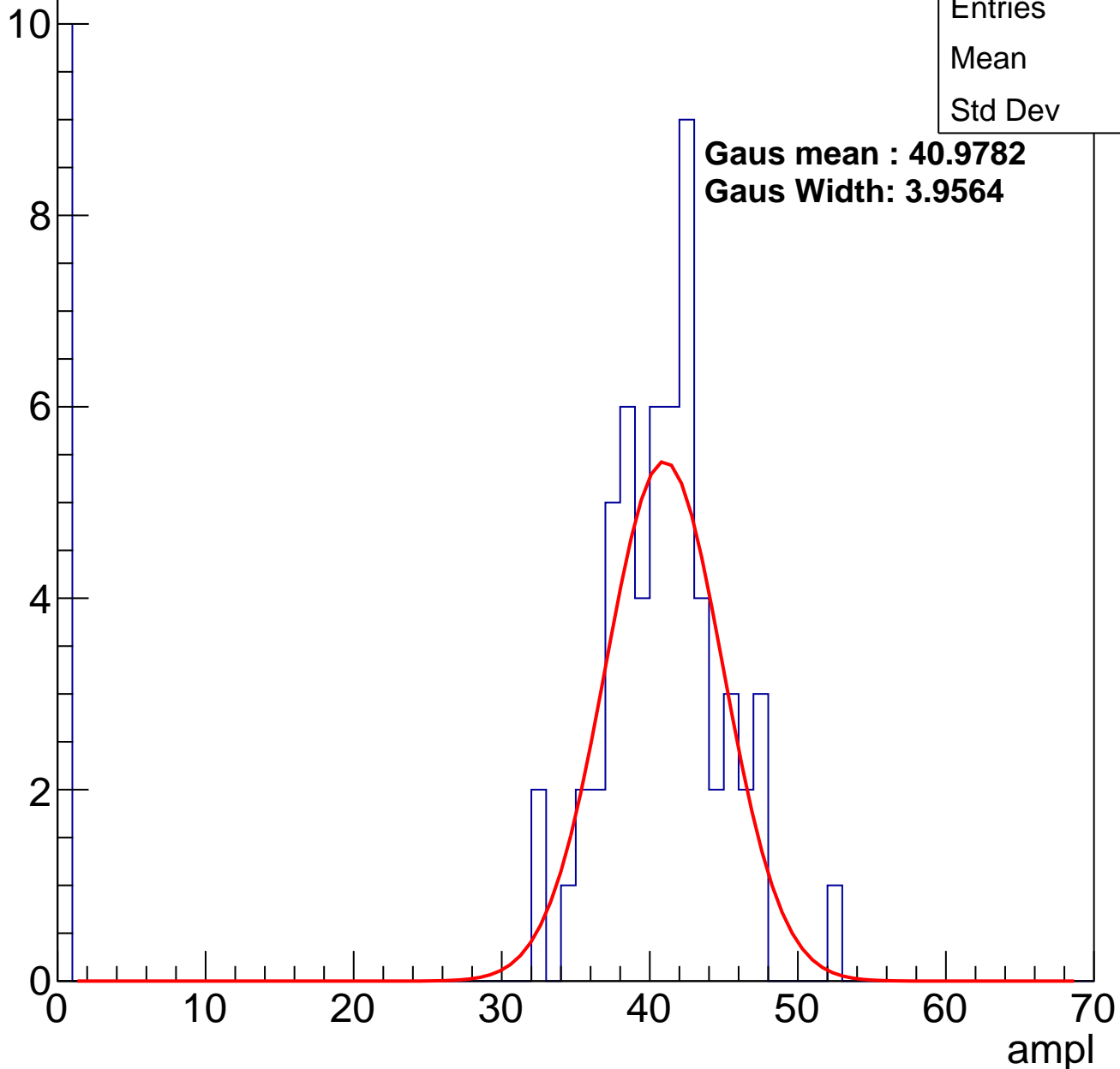
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	68
Mean	34.6
Std Dev	14.8

**Gaus mean : 40.9782**

**Gaus Width: 3.9564**

Entry

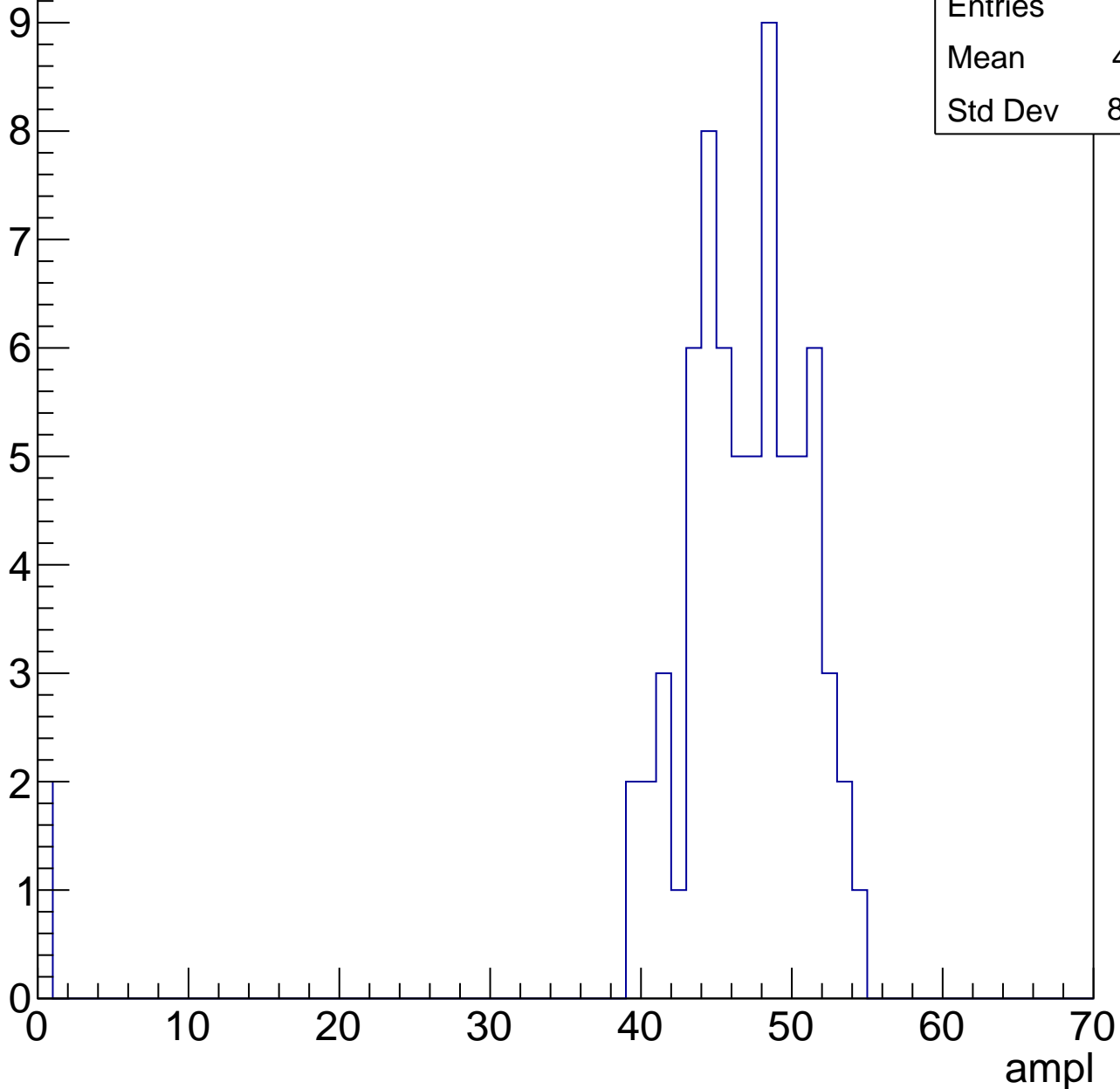


# B1L103S, U26-ch112, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	71
Mean	45.31
Std Dev	8.506

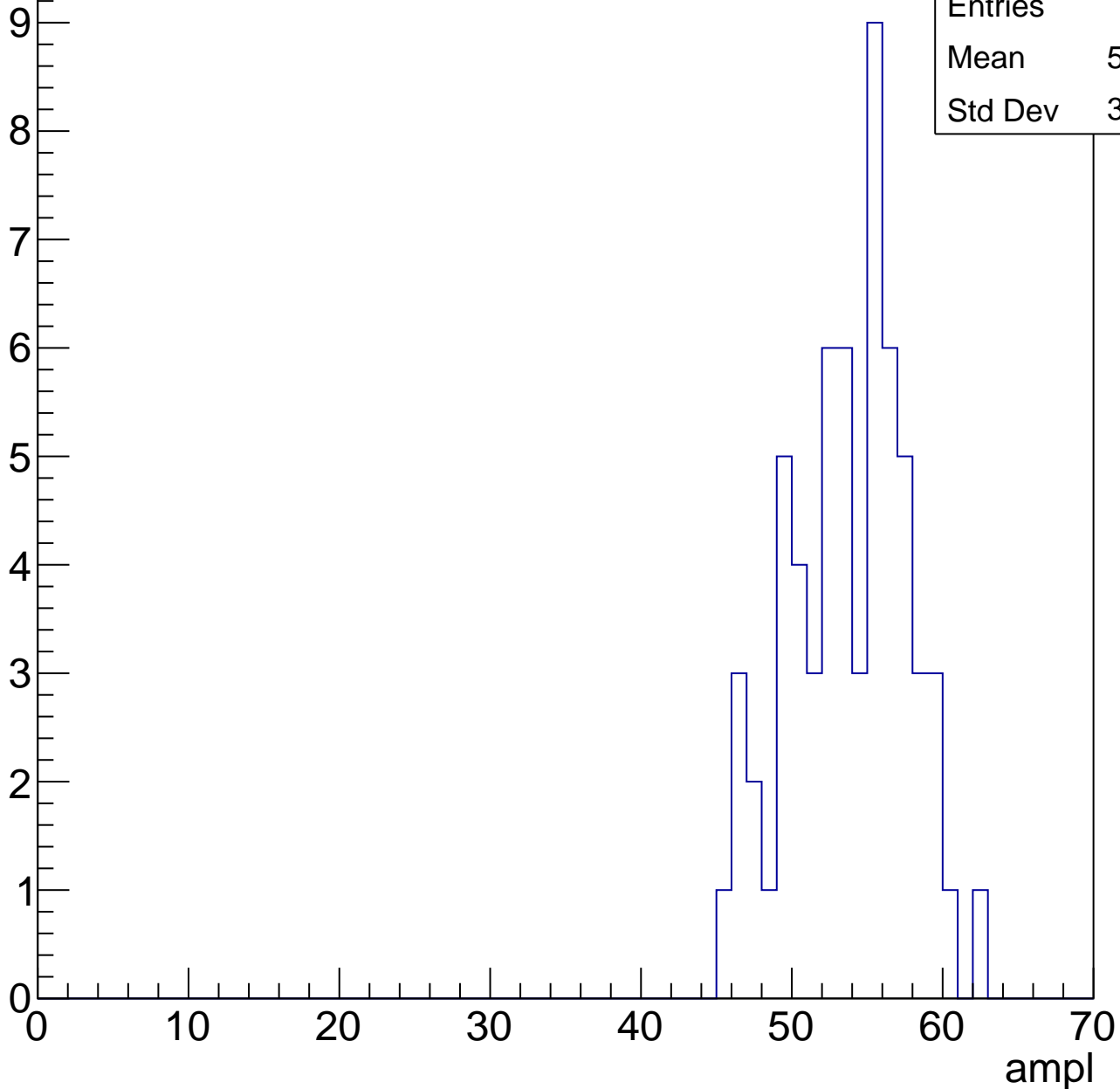


# B1L103S, U26-ch112, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	62
Mean	53.29
Std Dev	3.858

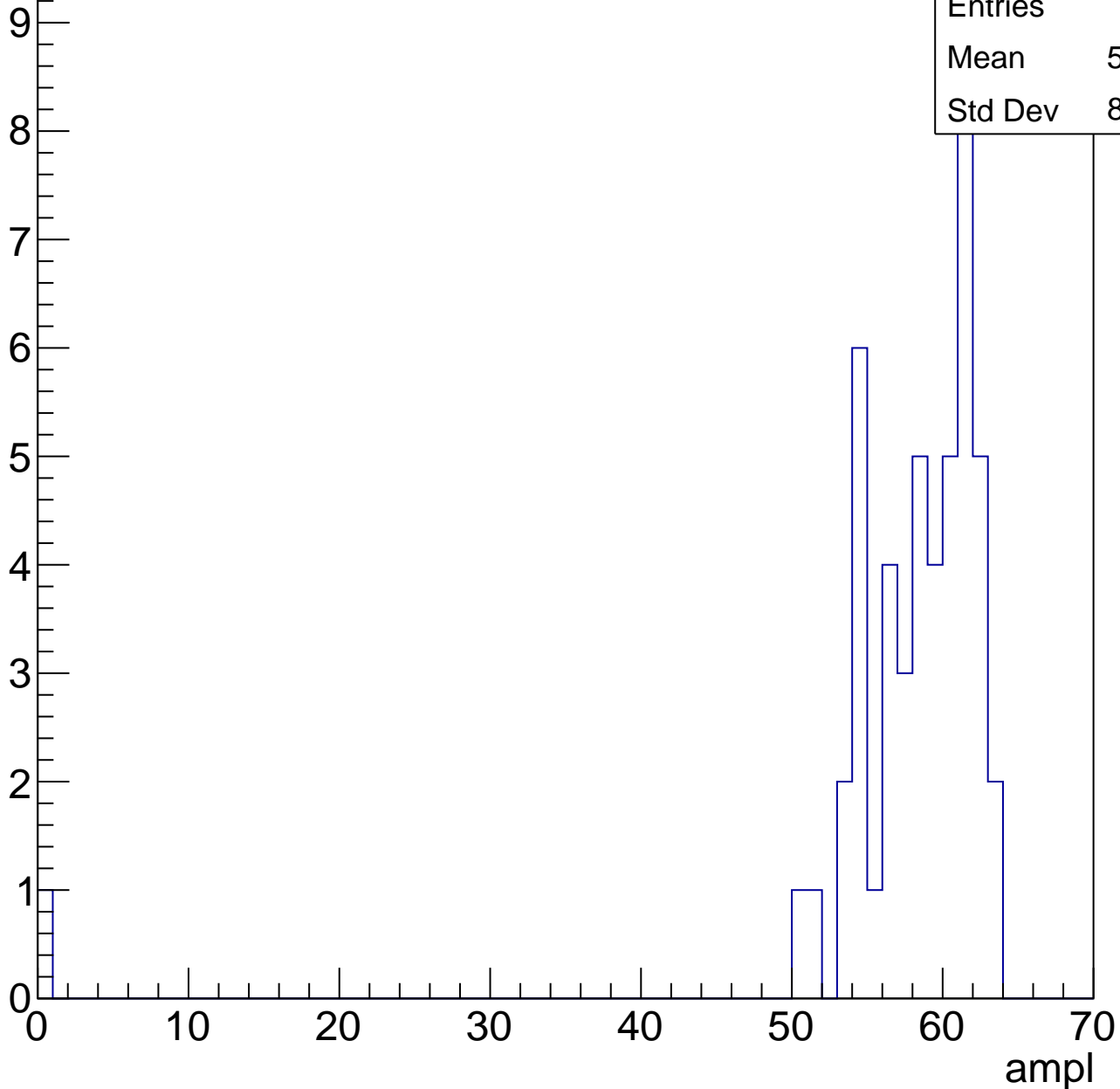


# B1L103S, U26-ch112, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	49
Mean	56.98
Std Dev	8.847

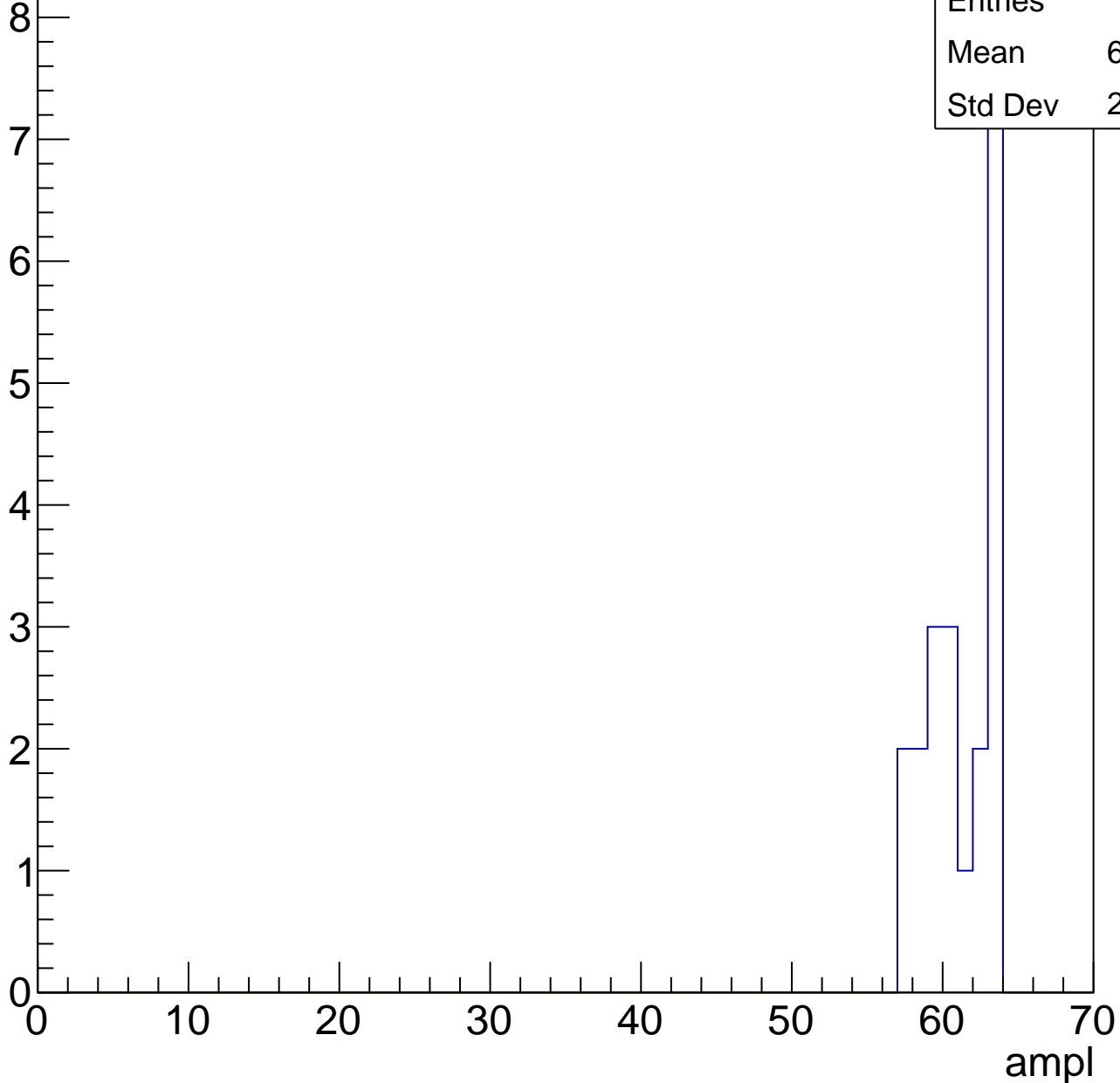


# B1L103S, U26-ch112, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	21
Mean	60.76
Std Dev	2.158



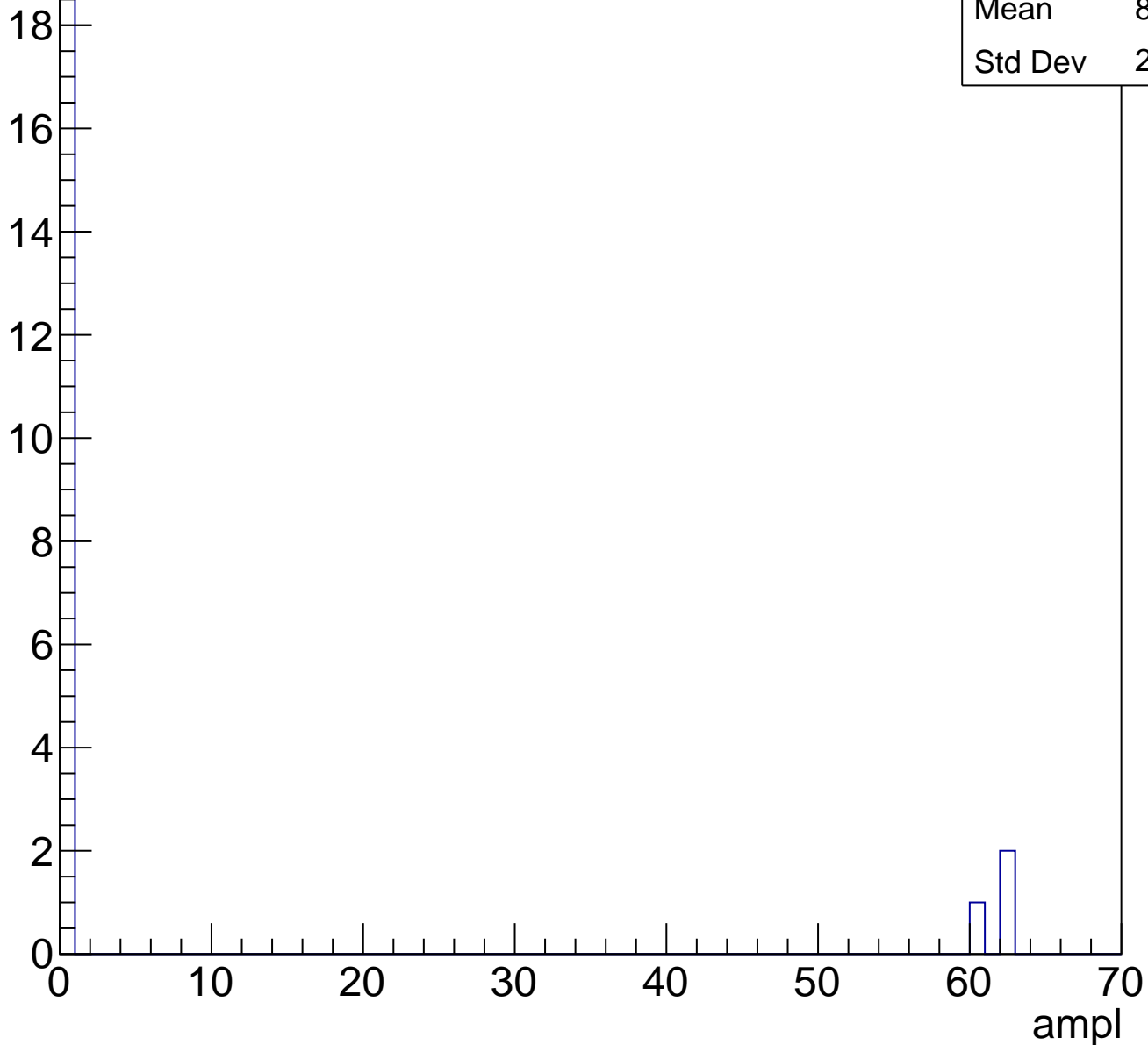


# B1L103S, U26-ch112, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	22
Mean	8.364
Std Dev	21.05

Entry



# B1L103S, U26-ch113, adc0

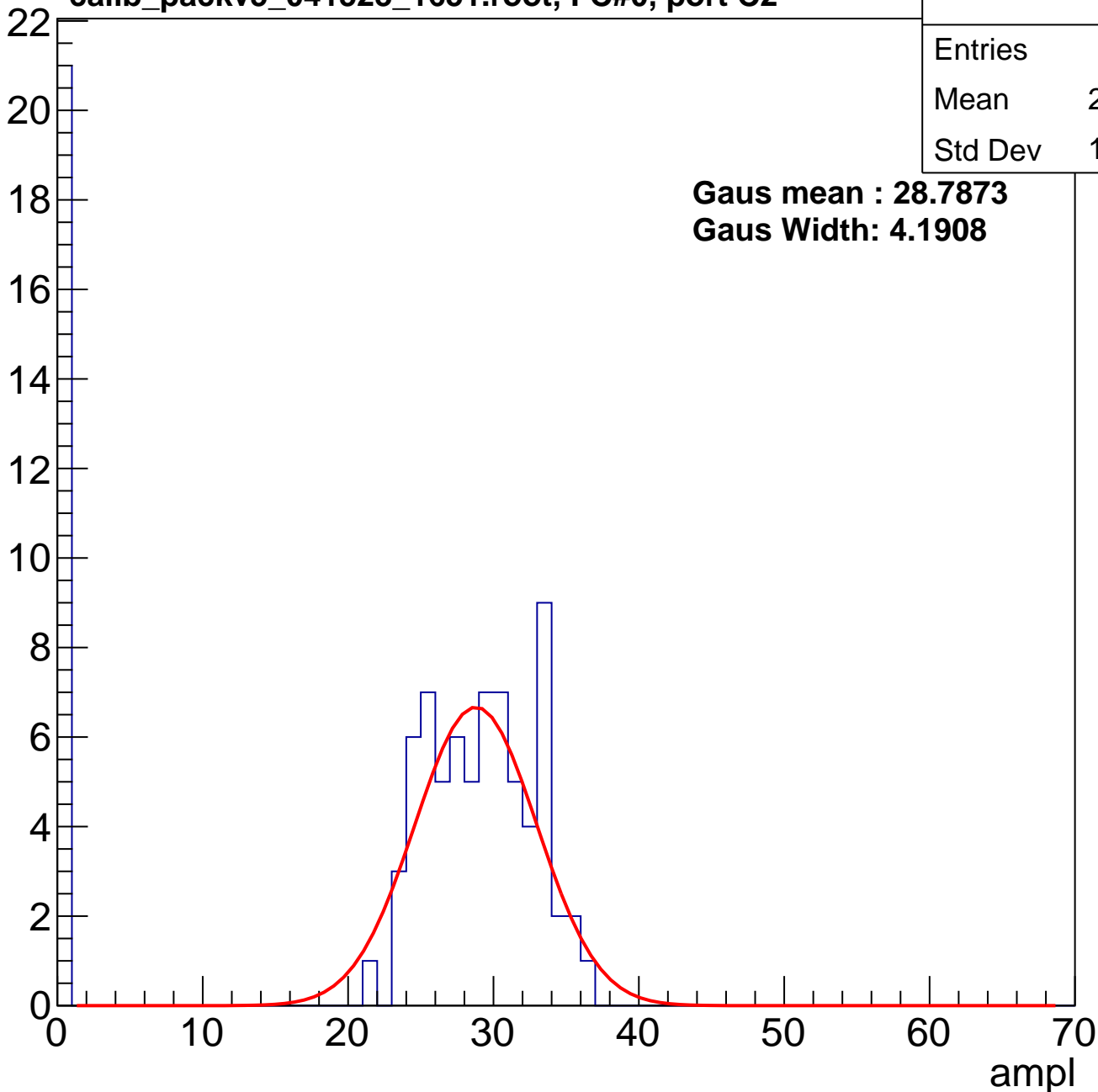
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	91
Mean	22.07
Std Dev	12.48

**Gaus mean : 28.7873**

**Gaus Width: 4.1908**

Entry



# B1L103S, U26-ch113, adc1

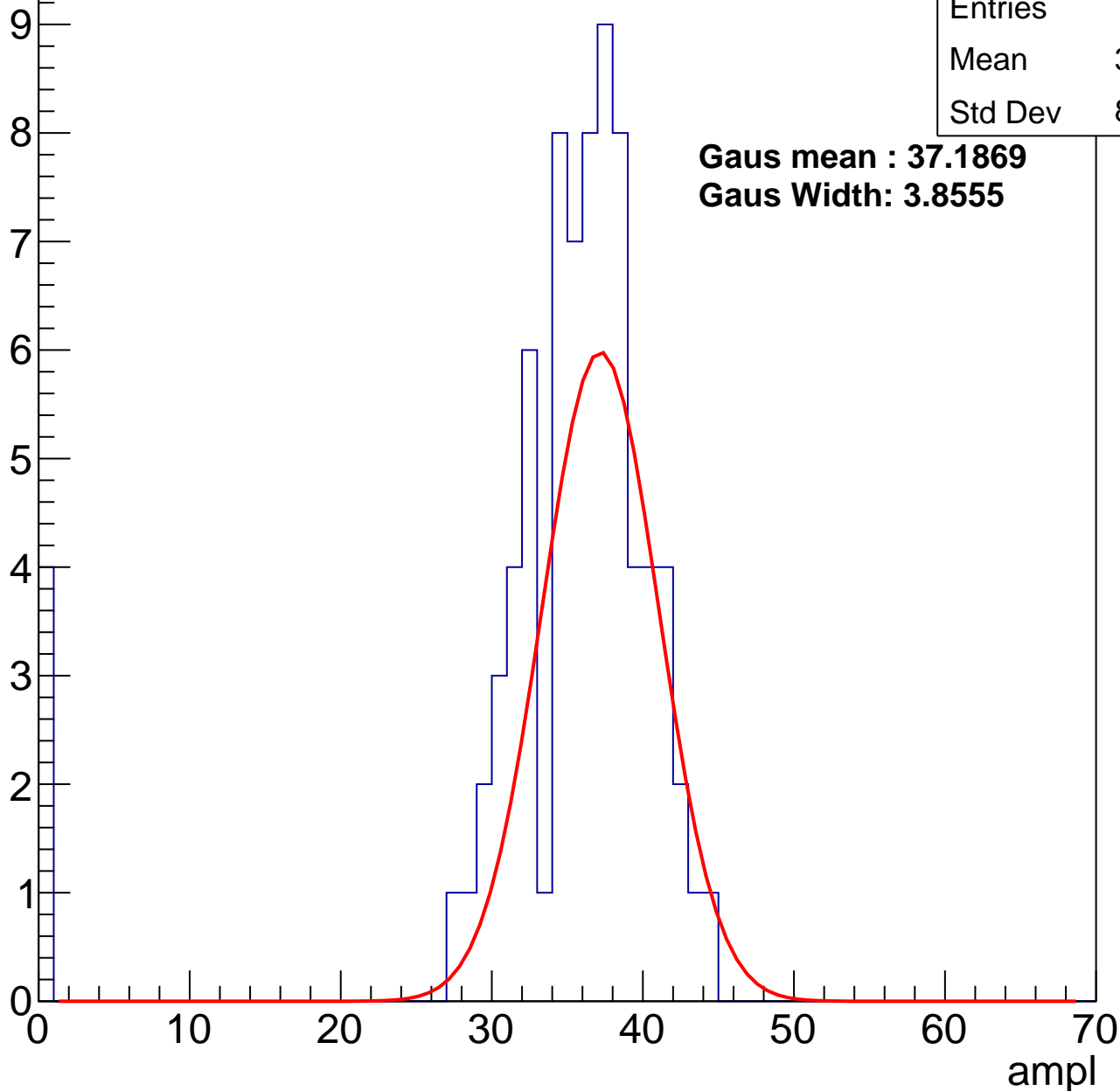
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	78
Mean	33.91
Std Dev	8.671

**Gaus mean : 37.1869**

**Gaus Width: 3.8555**



# B1L103S, U26-ch113, adc2

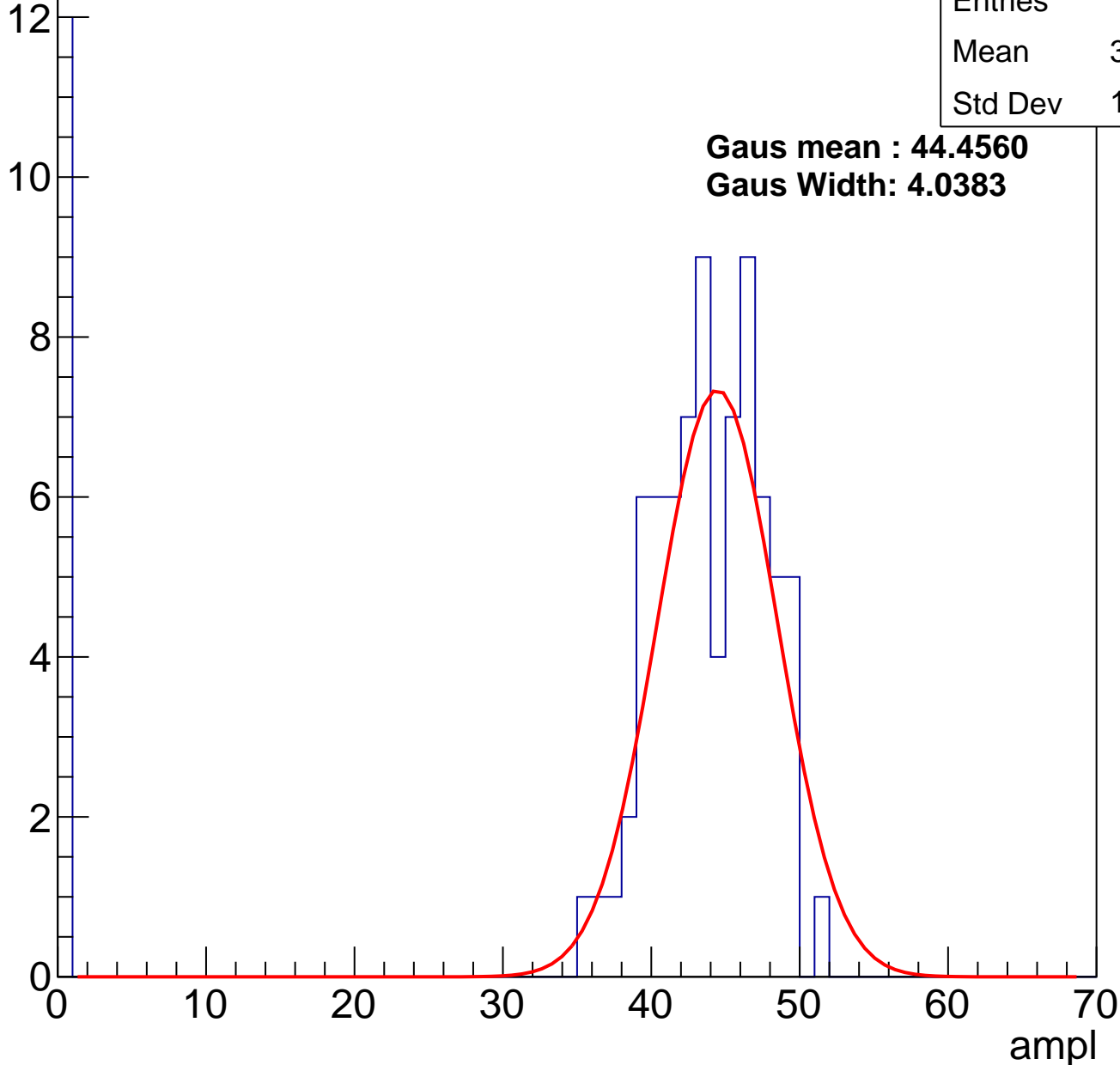
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	88
Mean	37.59
Std Dev	15.29

**Gaus mean : 44.4560**

**Gaus Width: 4.0383**

Entry

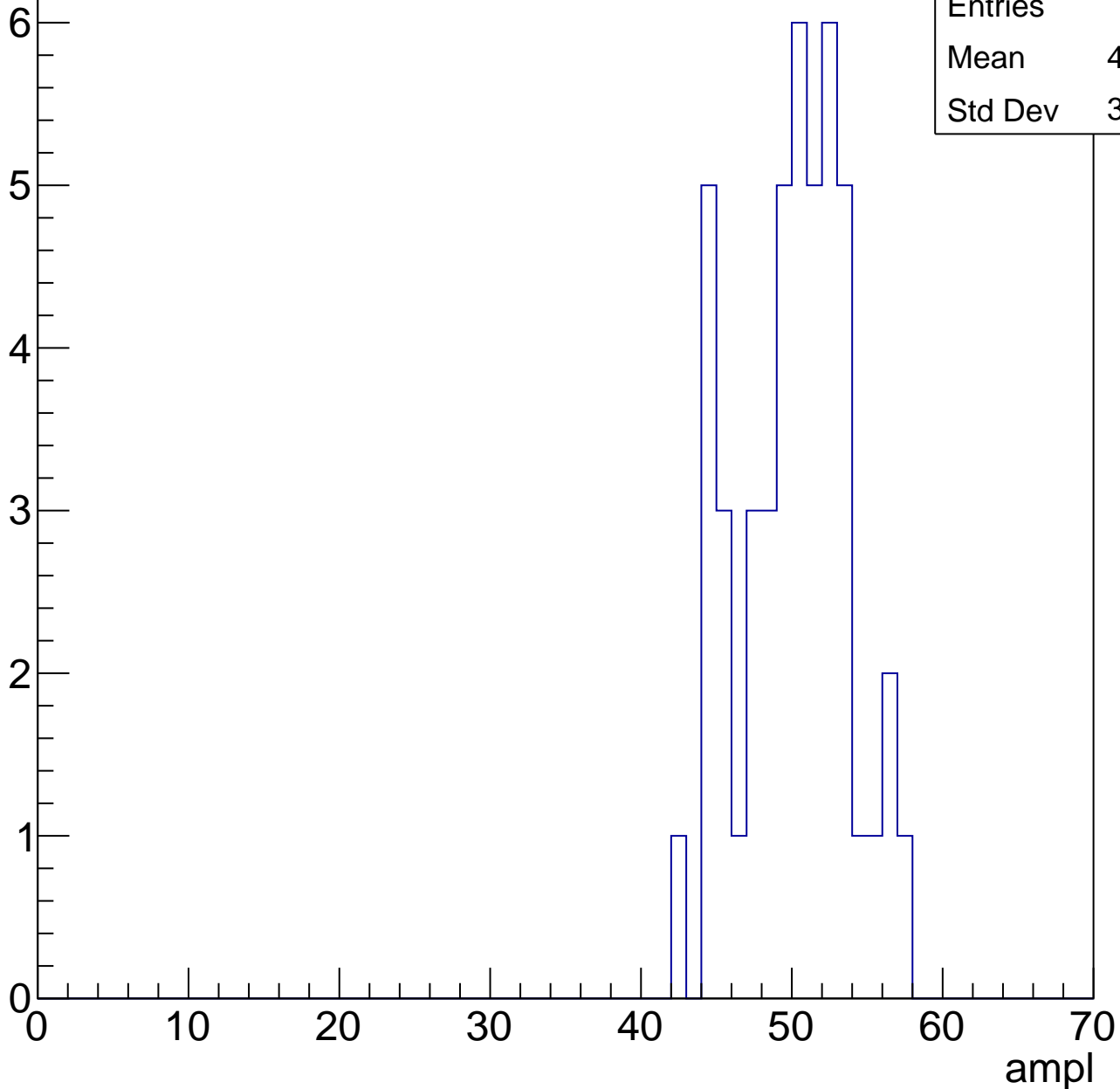


# B1L103S, U26-ch113, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	48
Mean	49.65
Std Dev	3.562

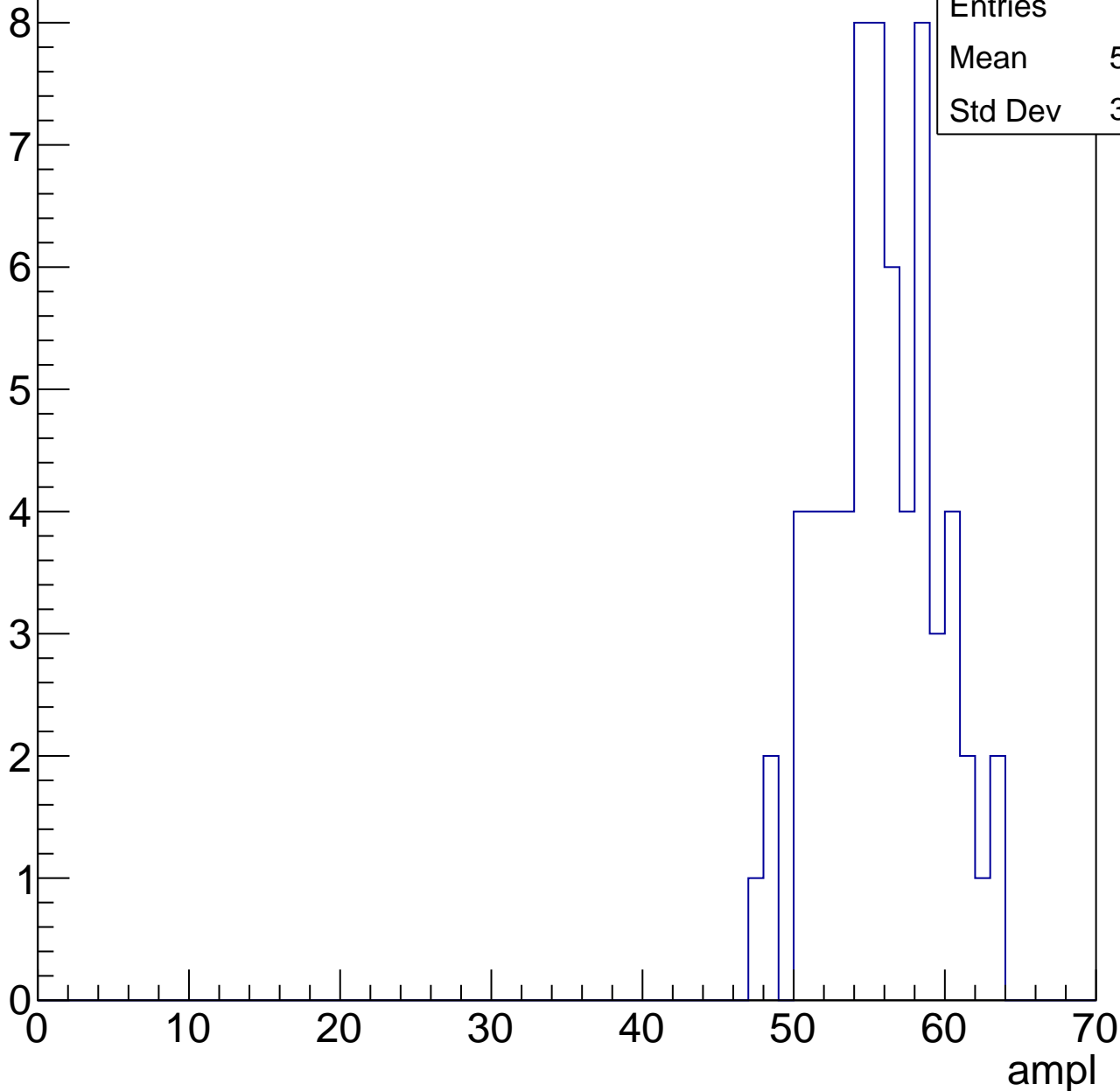


# B1L103S, U26-ch113, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

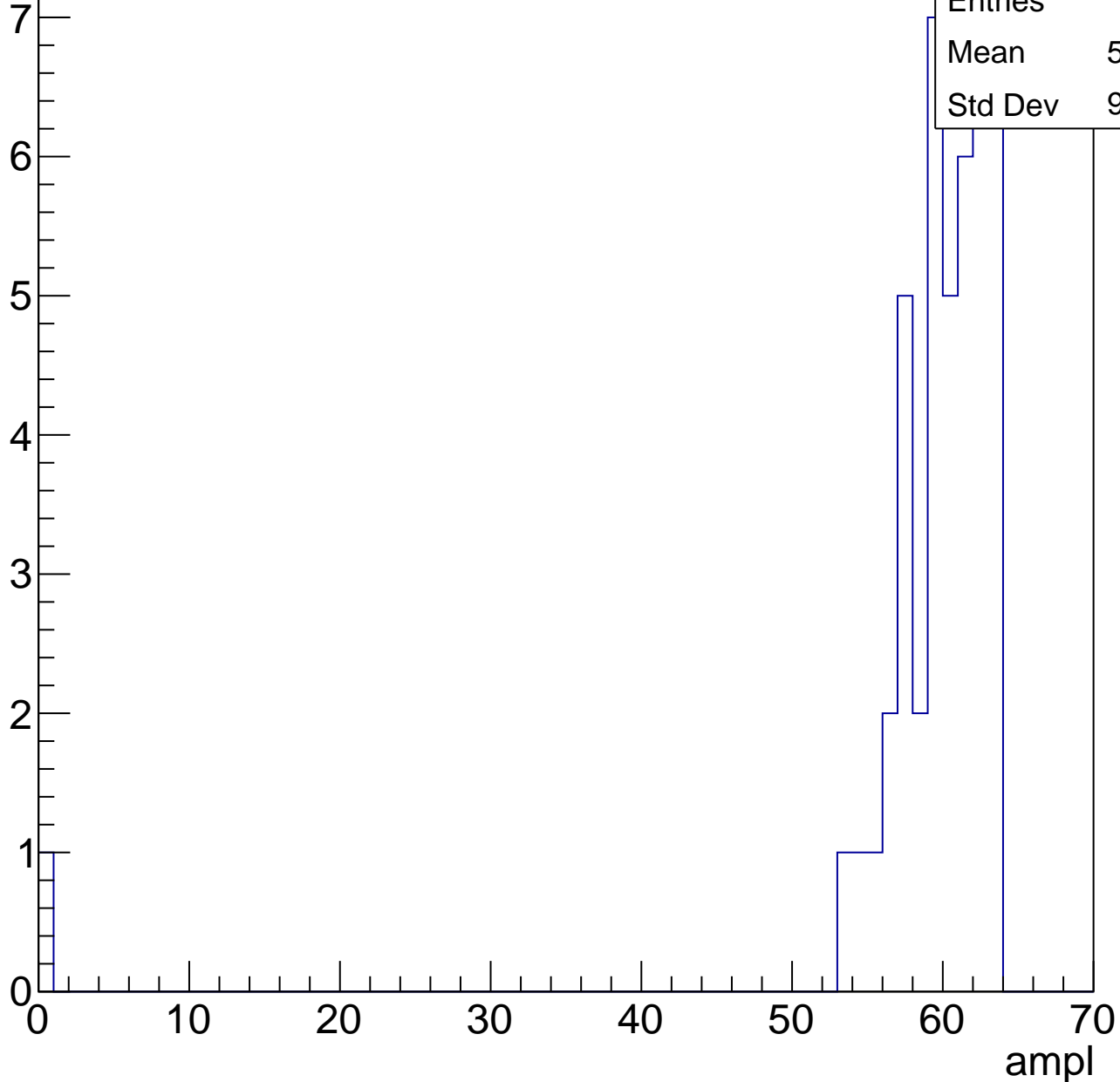
Entries	65
Mean	55.29
Std Dev	3.662



# B1L103S, U26-ch113, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



# B1L103S, U26-ch113, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

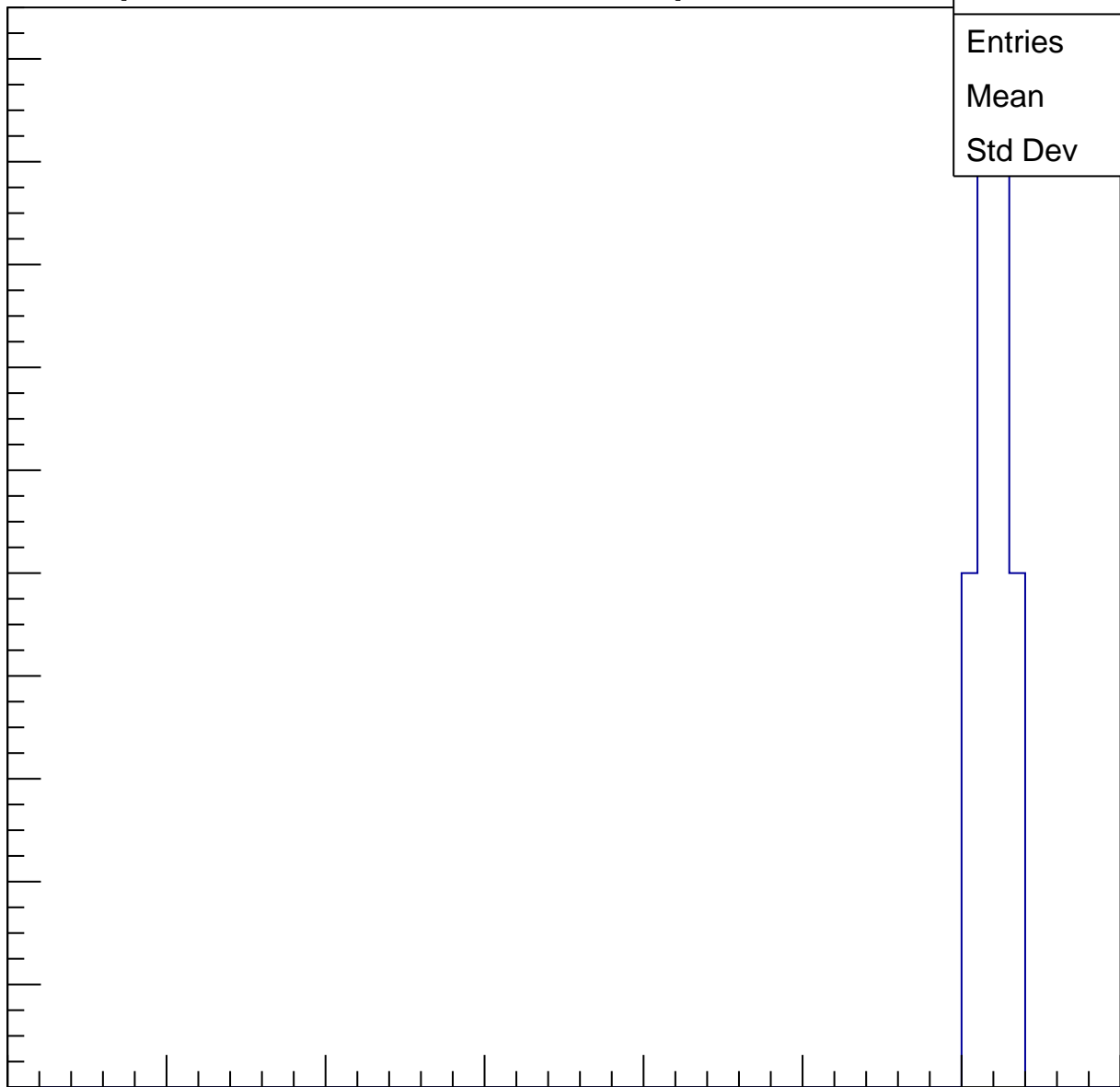
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	6
Mean	61.5
Std Dev	0.9574

0 10 20 30 40 50 60 70

ampl





# B1L103S, U26-ch113, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

18  
16  
14  
12  
10  
8  
6  
4  
2  
0

Entries	19
Mean	0
Std Dev	0

ampl

# B1L103S, U26-ch114, adc0

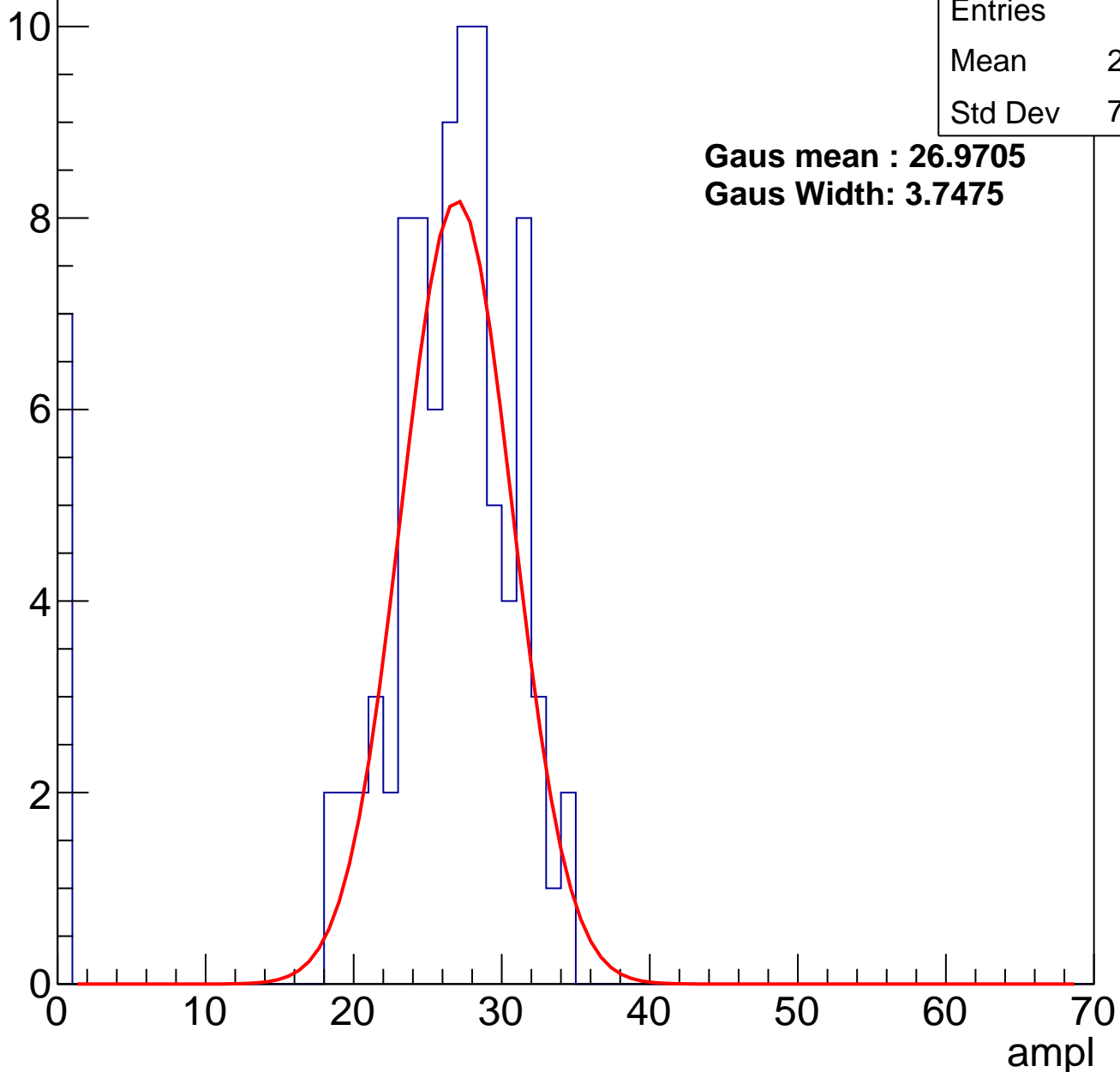
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	92
Mean	24.36
Std Dev	7.832

**Gaus mean : 26.9705**

**Gaus Width: 3.7475**

Entry



# B1L103S, U26-ch114, adc1

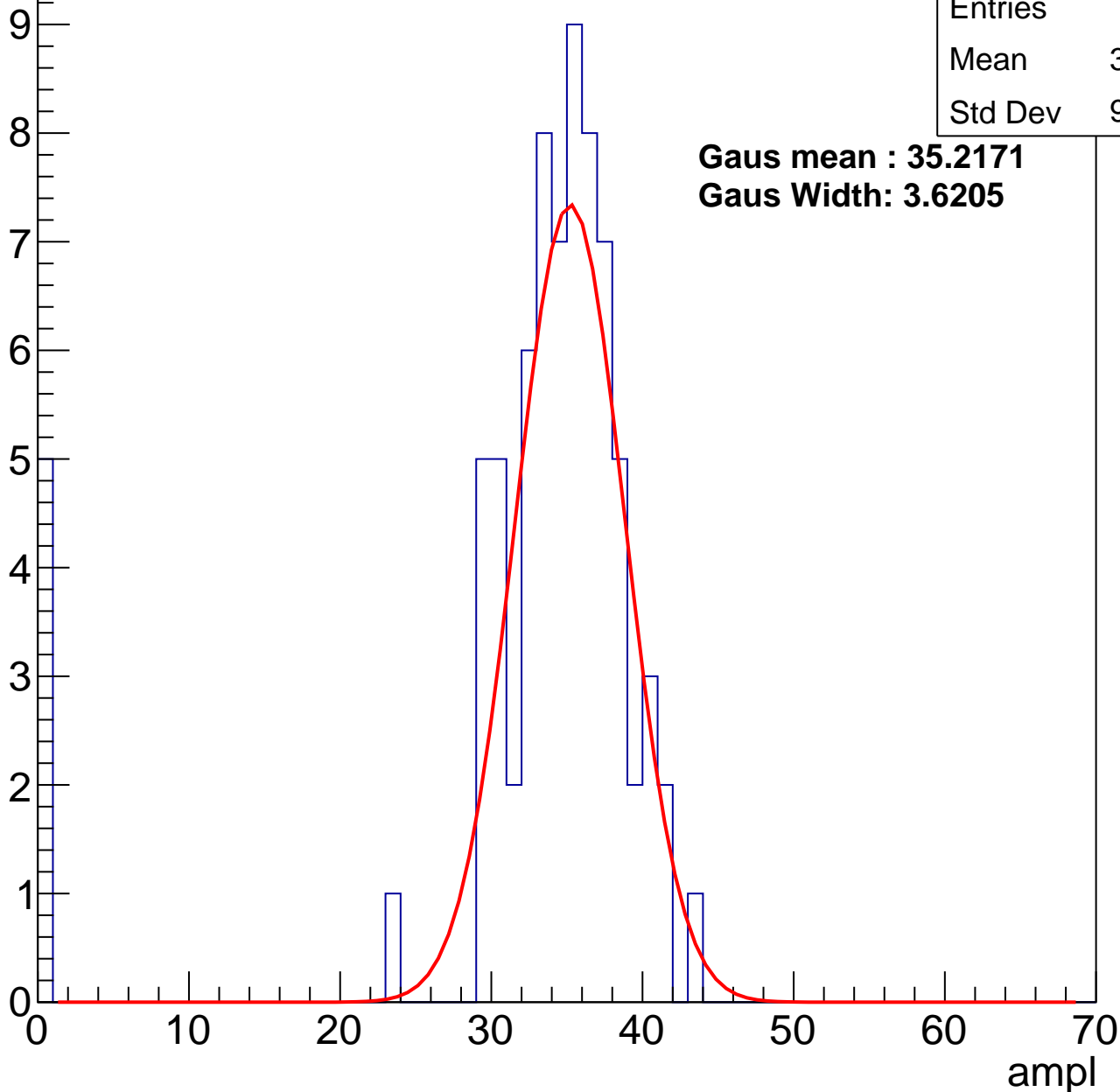
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	76
Mean	32.22
Std Dev	9.203

**Gaus mean : 35.2171**

**Gaus Width: 3.6205**



# B1L103S, U26-ch114, adc2

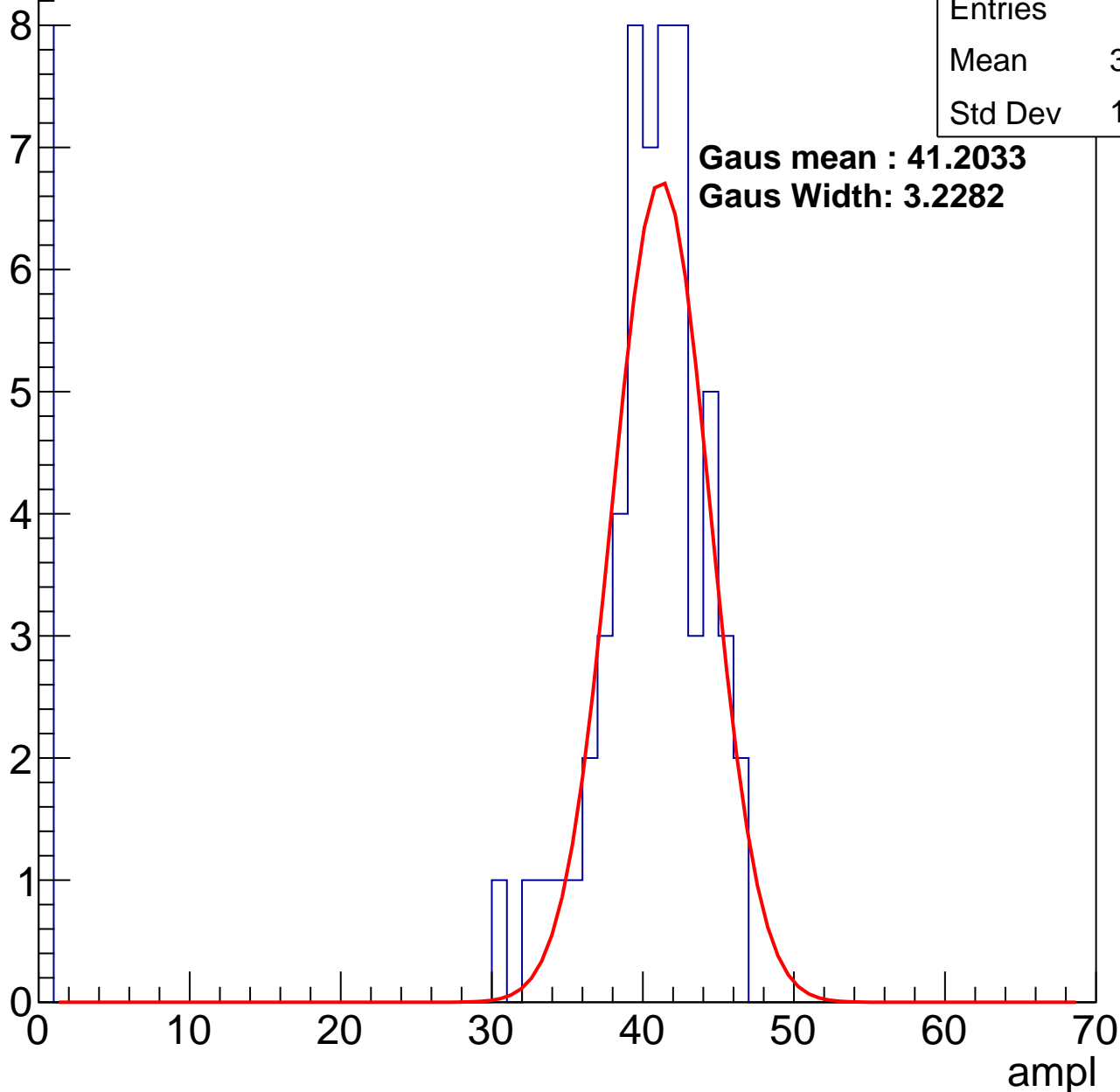
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	66
Mean	35.32
Std Dev	13.49

**Gaus mean : 41.2033**

**Gaus Width: 3.2282**

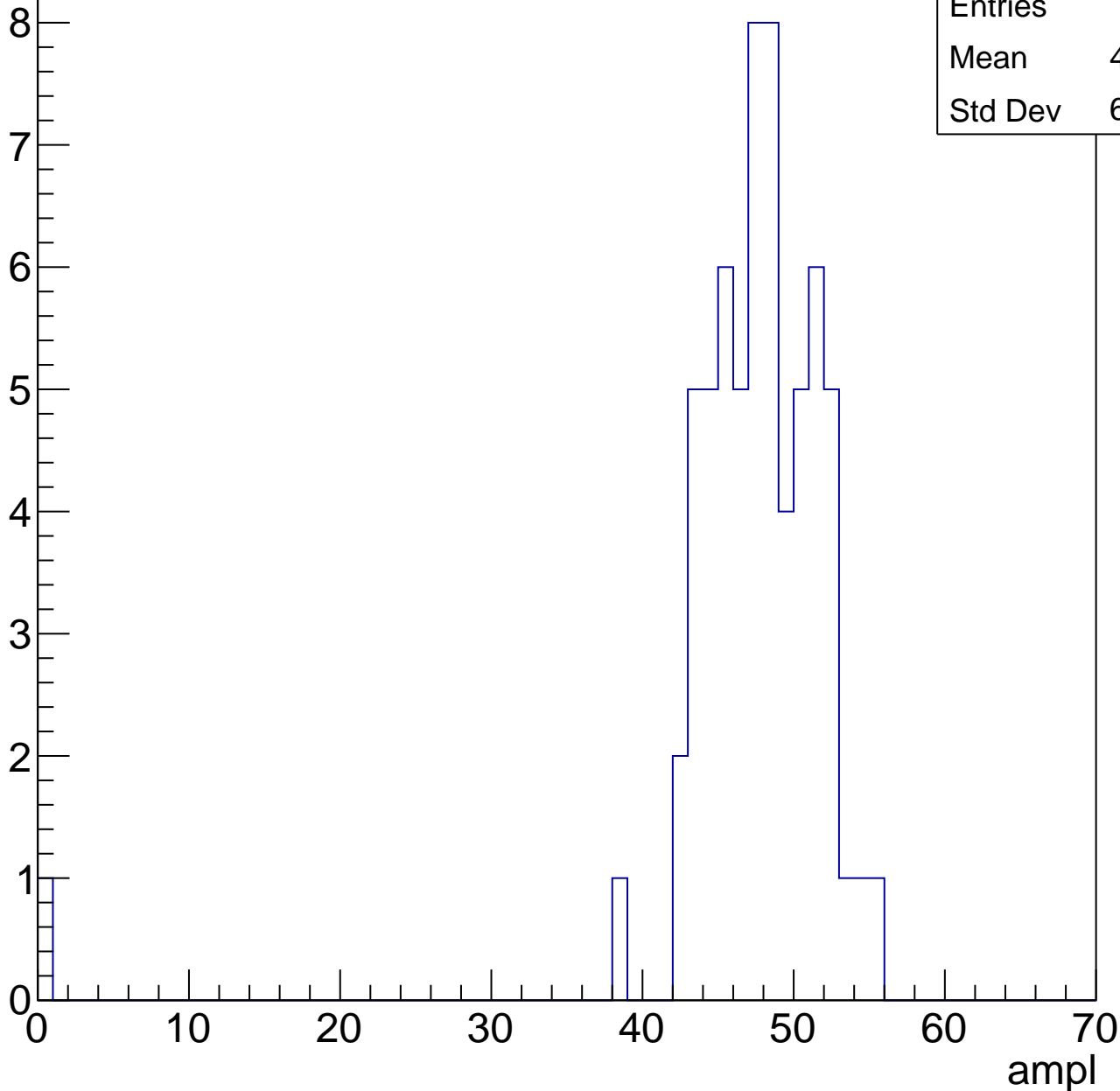


# B1L103S, U26-ch114, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	64
Mean	46.73
Std Dev	6.764

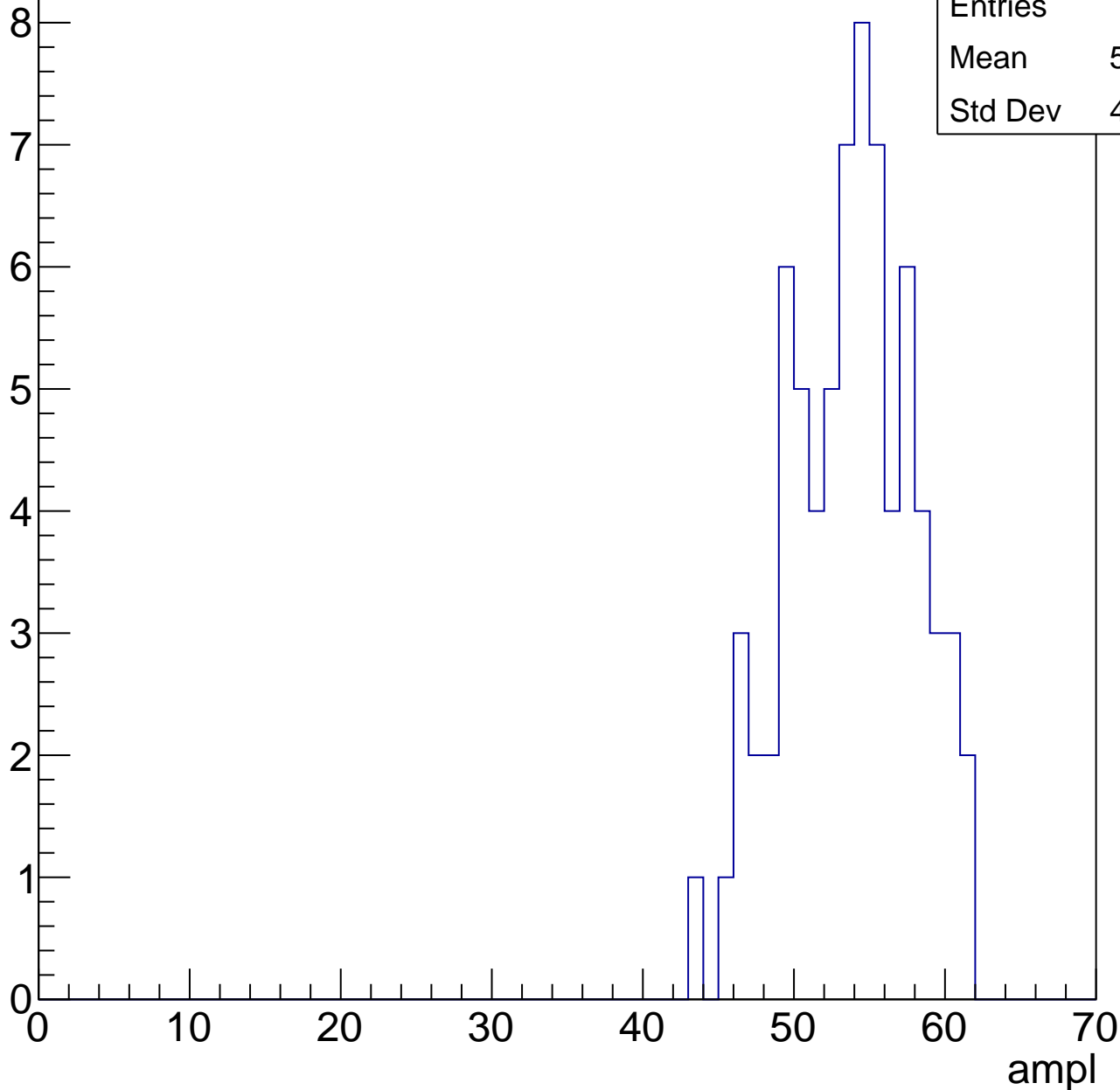


# B1L103S, U26-ch114, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	73
Mean	53.27
Std Dev	4.122

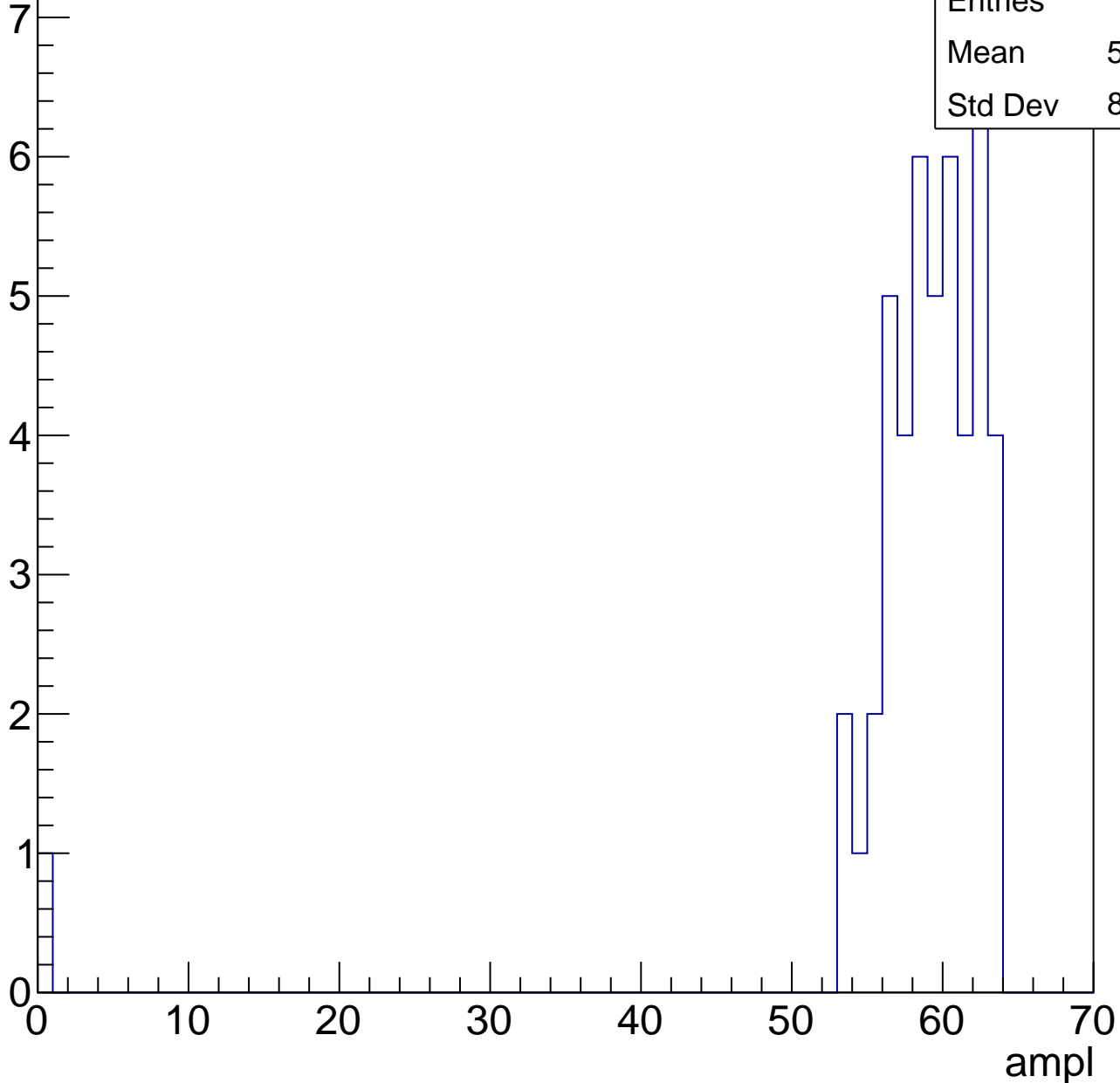


# B1L103S, U26-ch114, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	47
Mean	57.68
Std Dev	8.925

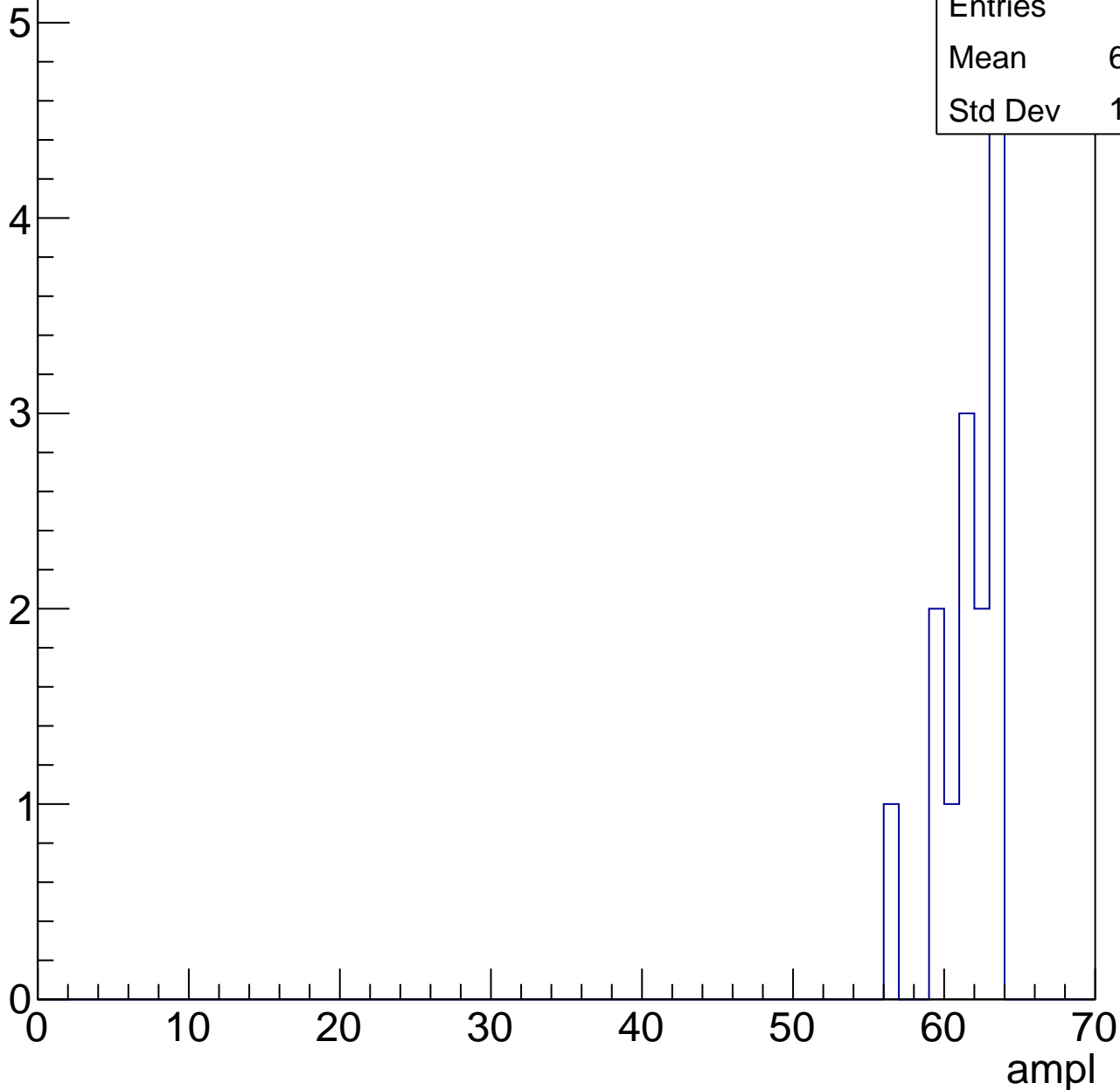


# B1L103S, U26-ch114, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	14
Mean	61.14
Std Dev	1.995

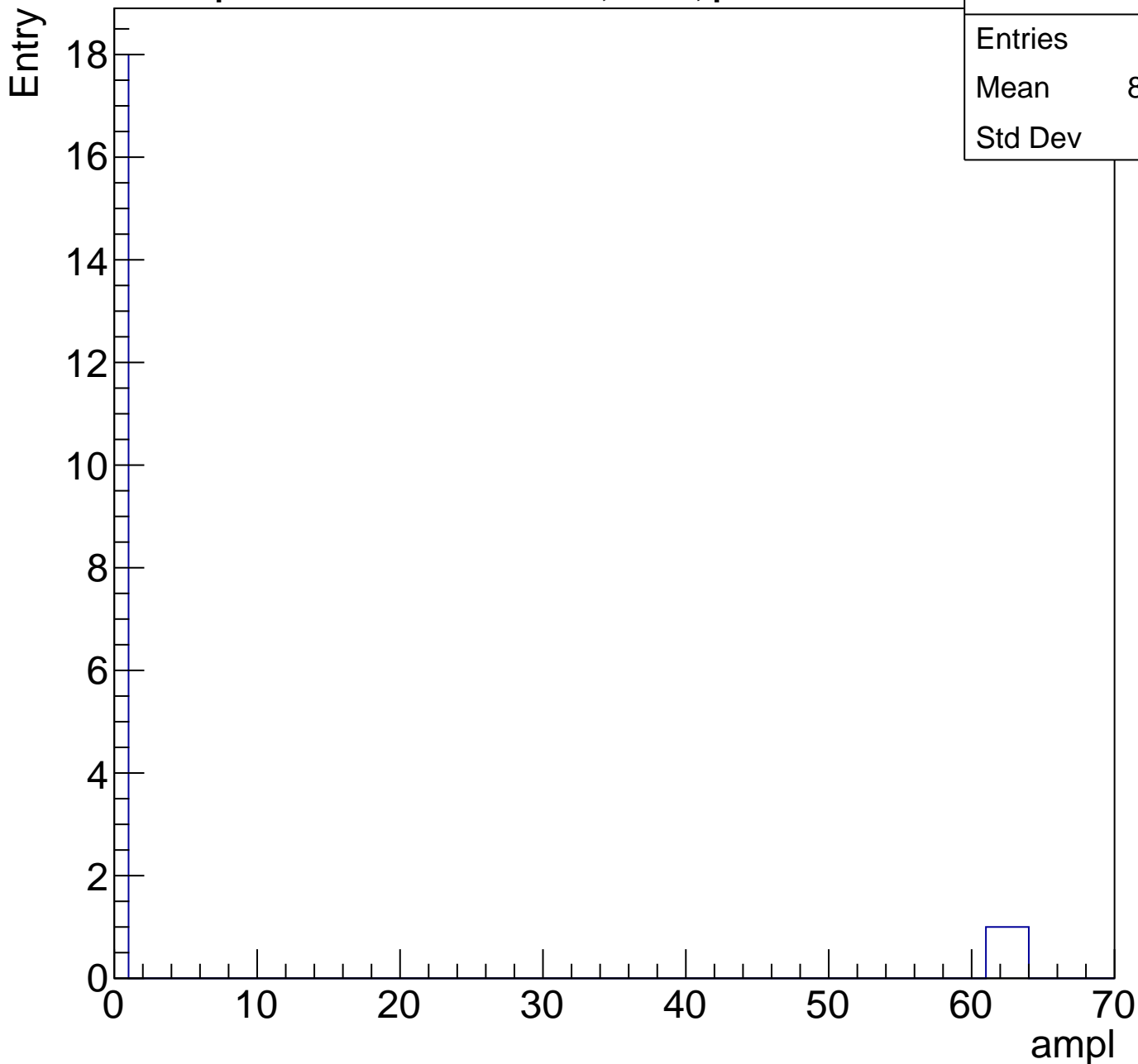




# B1L103S, U26-ch114, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	21
Mean	8.857
Std Dev	21.7



# B1L103S, U26-ch115, adc0

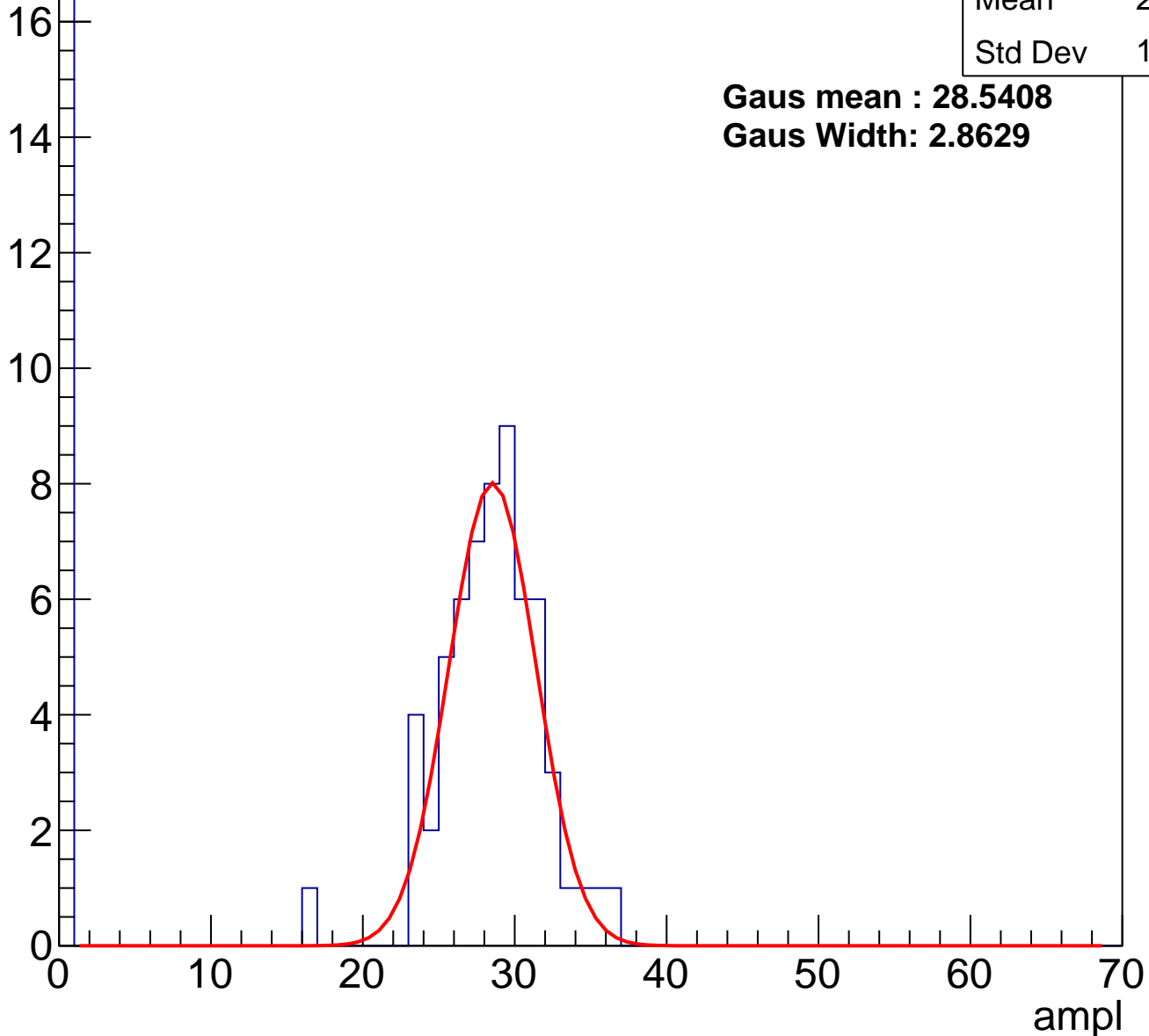
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	78
Mean	21.94
Std Dev	11.94

**Gaus mean : 28.5408**

**Gaus Width: 2.8629**

Entry



# B1L103S, U26-ch115, adc1

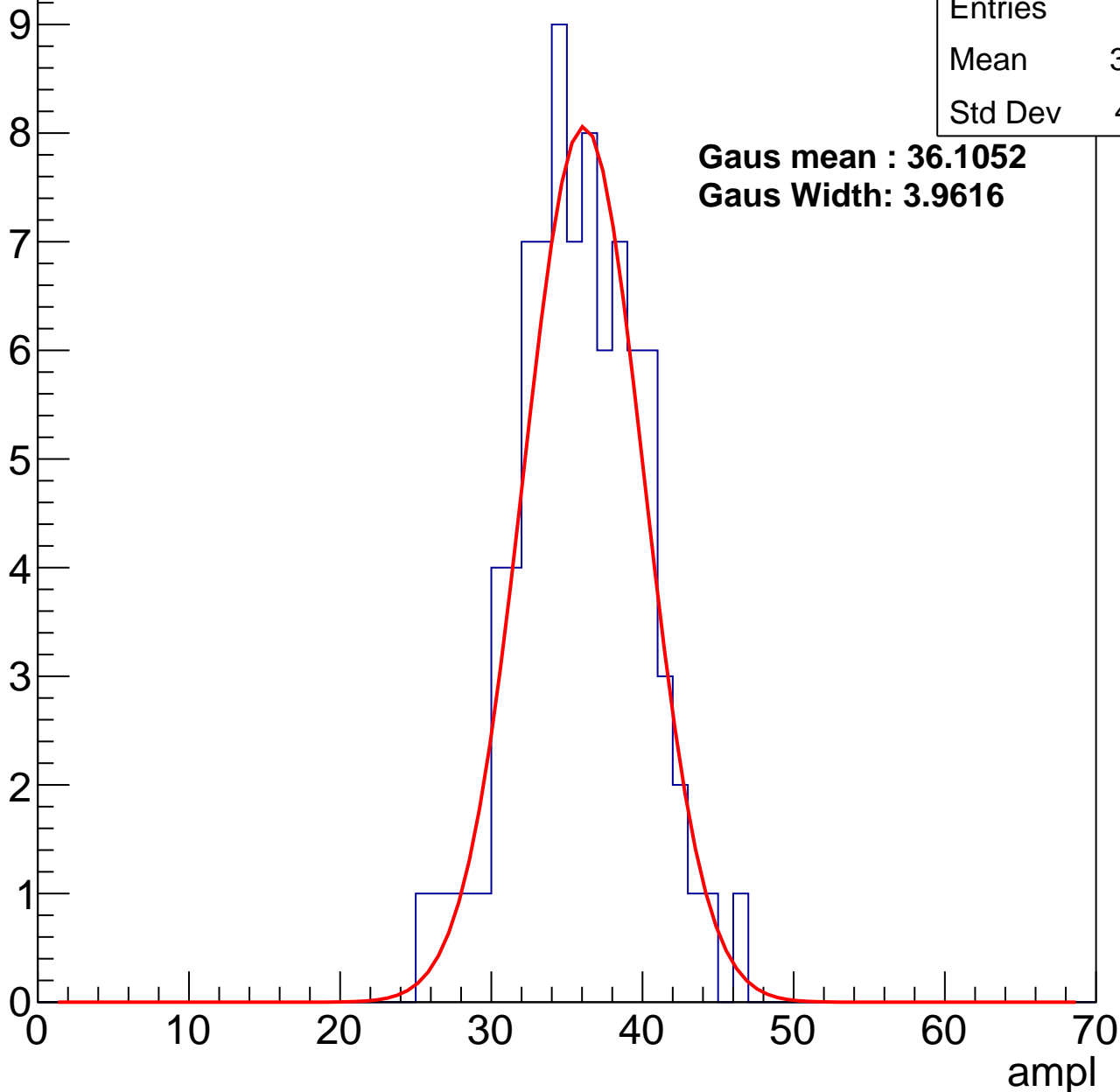
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	84
Mean	35.42
Std Dev	4.071

**Gaus mean : 36.1052**

**Gaus Width: 3.9616**



# B1L103S, U26-ch115, adc2

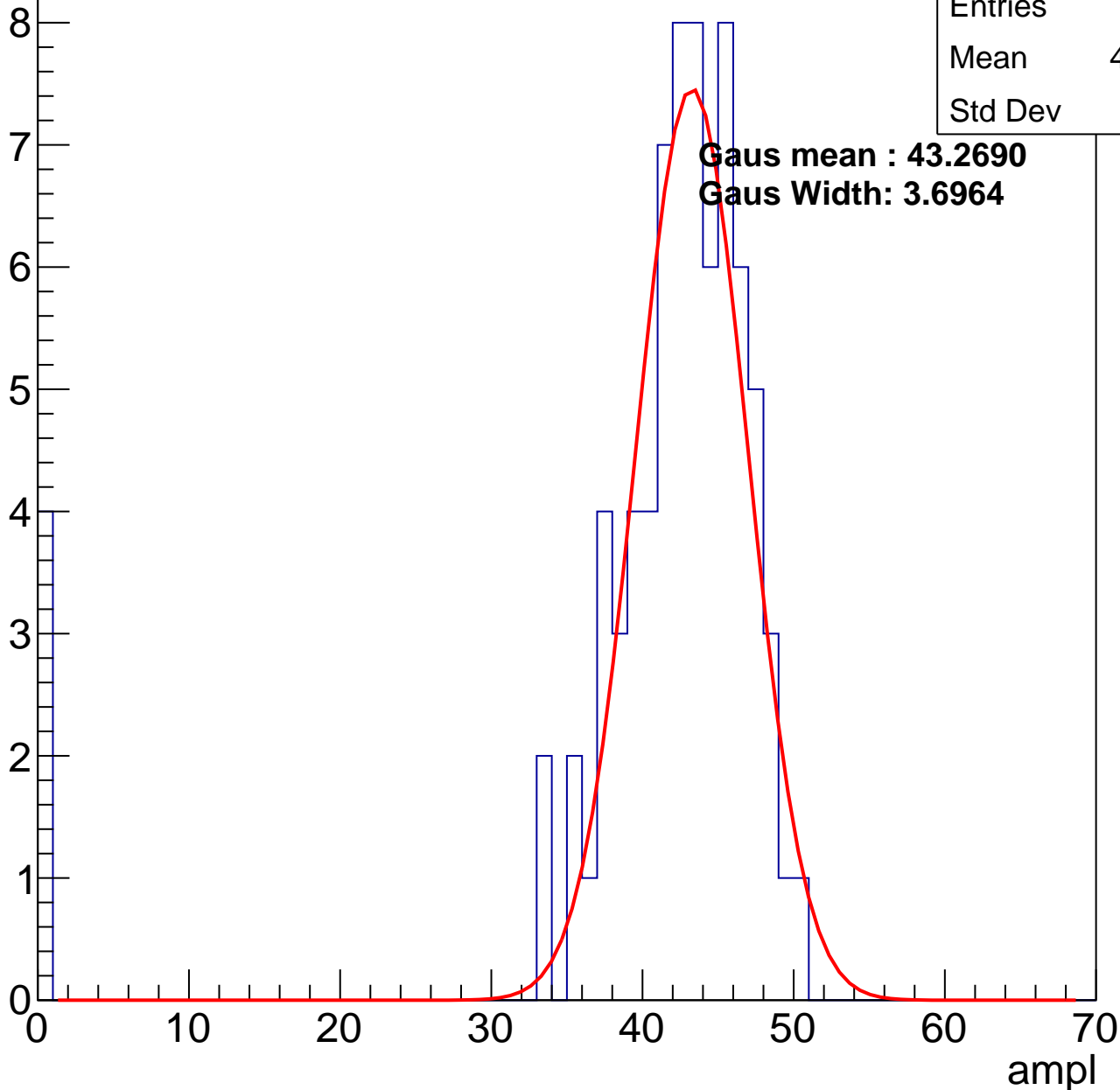
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	77
Mean	40.19
Std Dev	10.1

**Gaus mean : 43.2690**

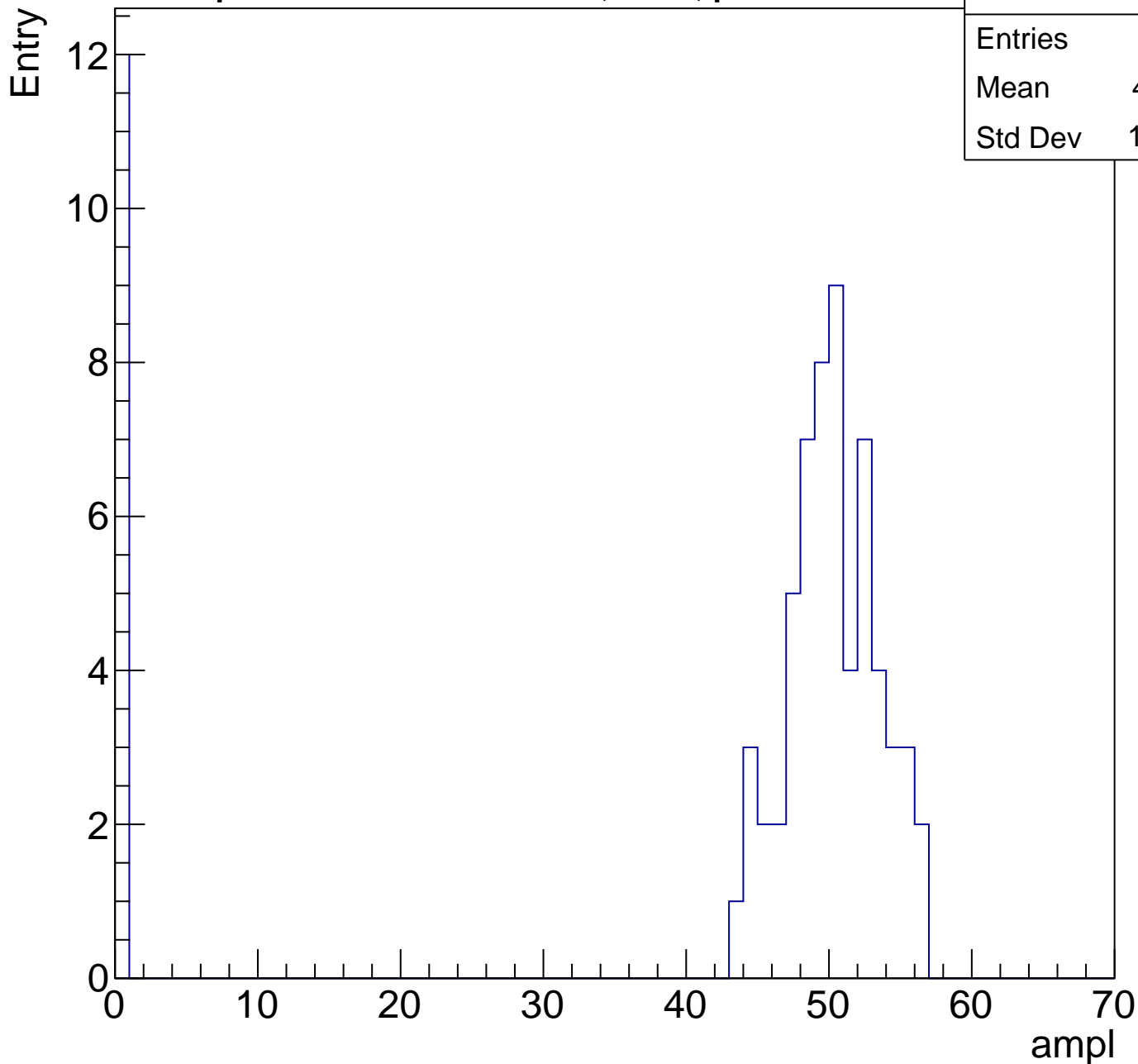
**Gaus Width: 3.6964**



# B1L103S, U26-ch115, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	72
Mean	41.51
Std Dev	18.78

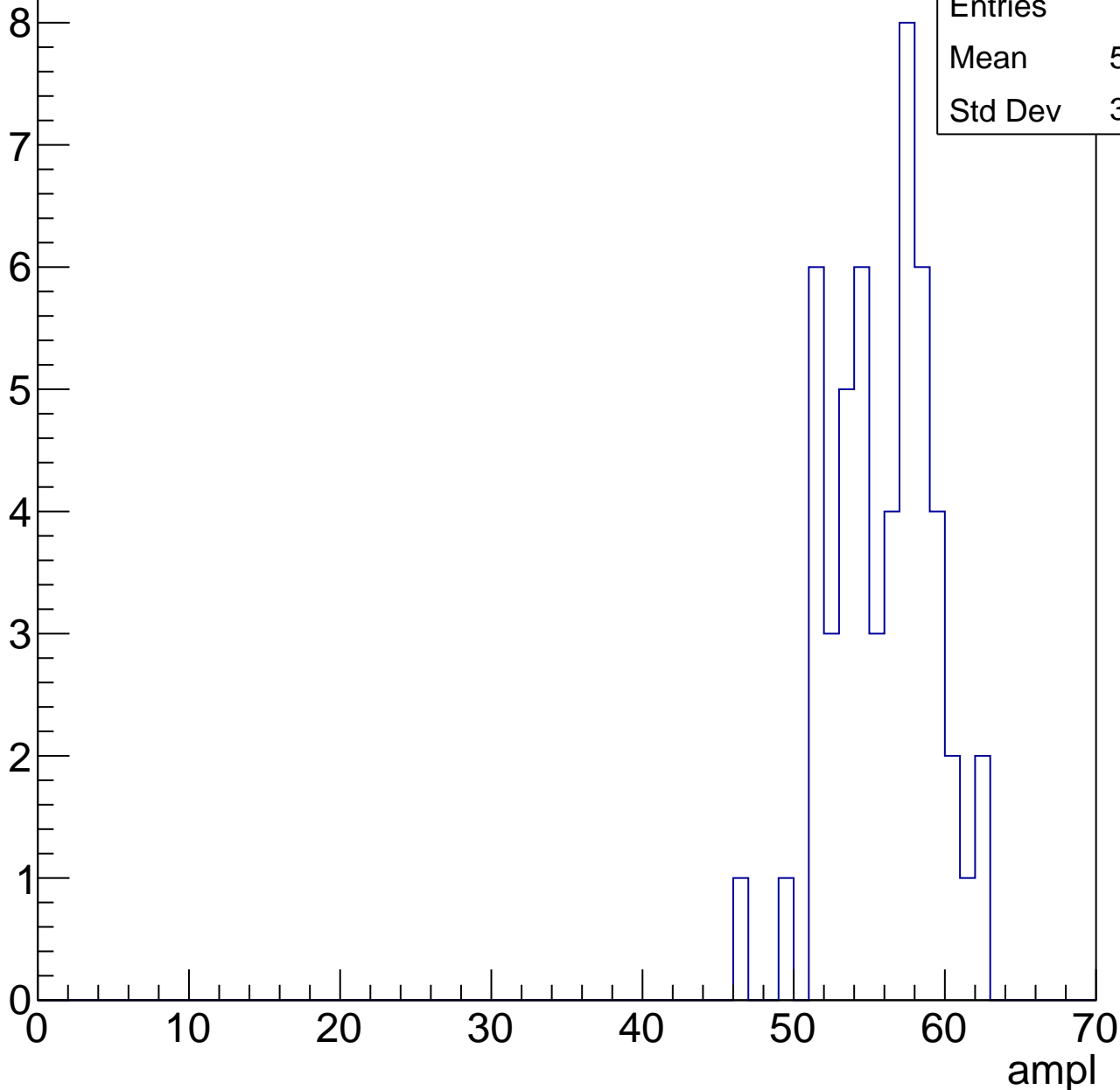


# B1L103S, U26-ch115, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	52
Mean	55.38
Std Dev	3.386

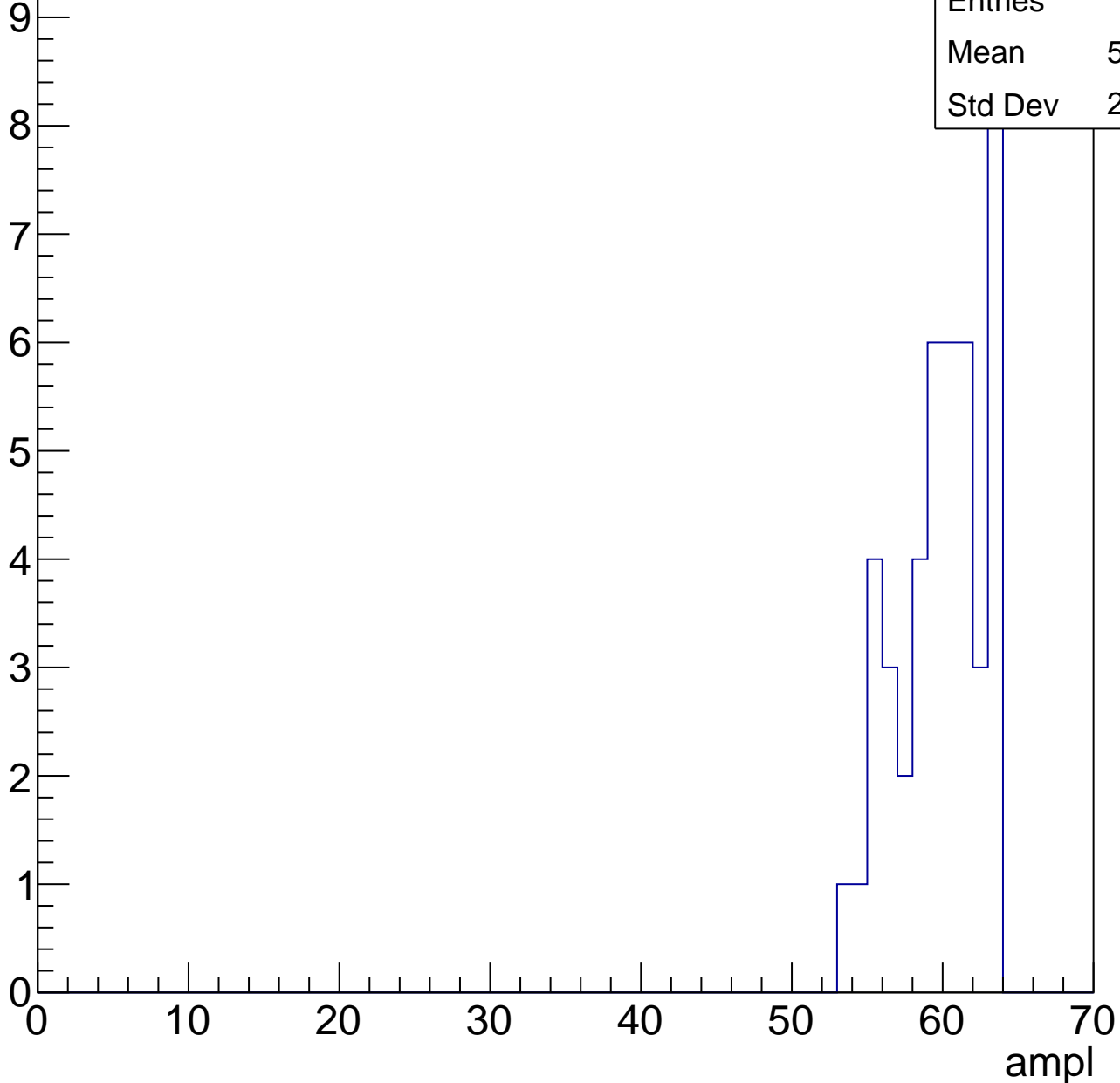


# B1L103S, U26-ch115, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

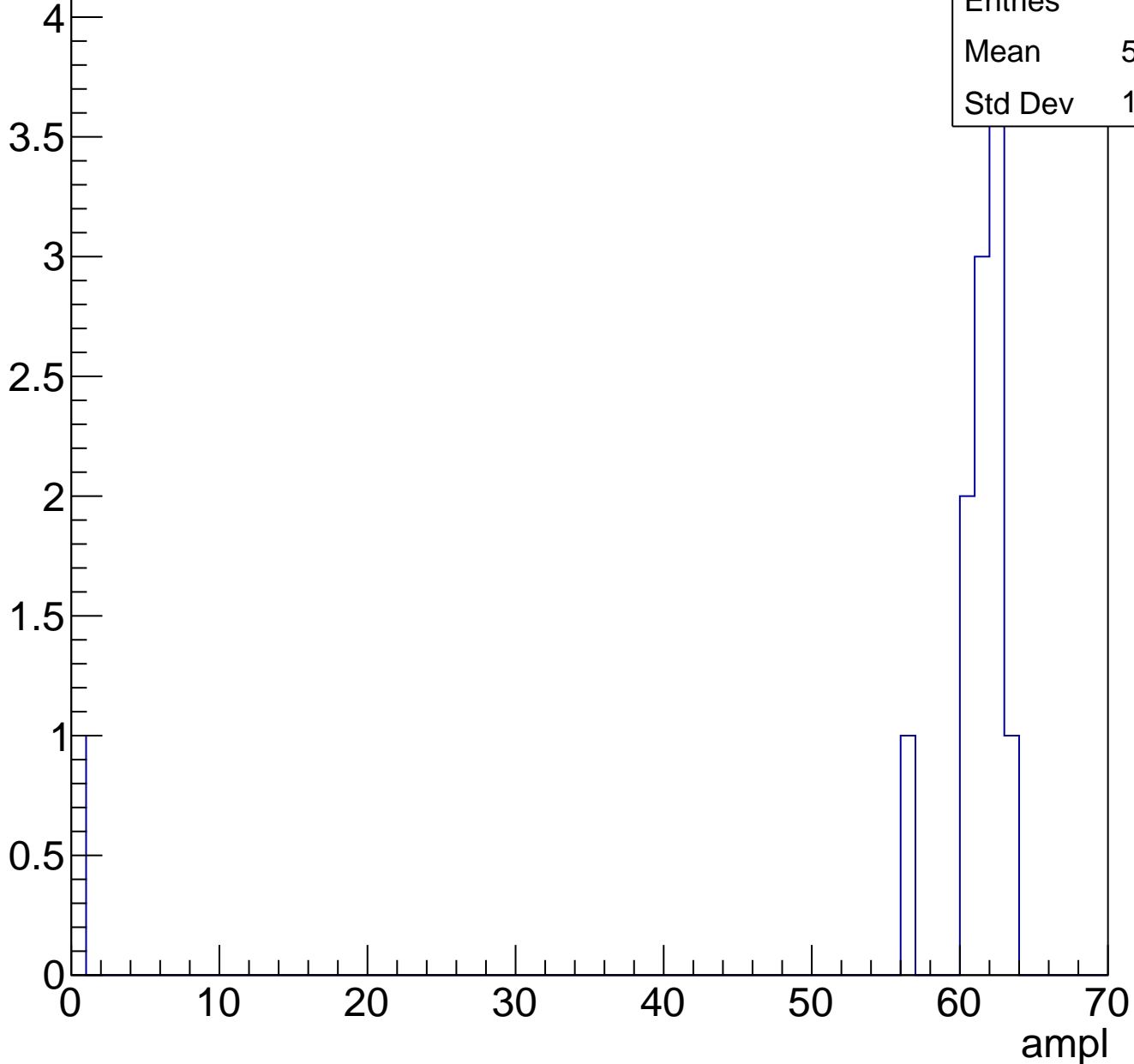
Entries	45
Mean	59.42
Std Dev	2.817



# B1L103S, U26-ch115, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

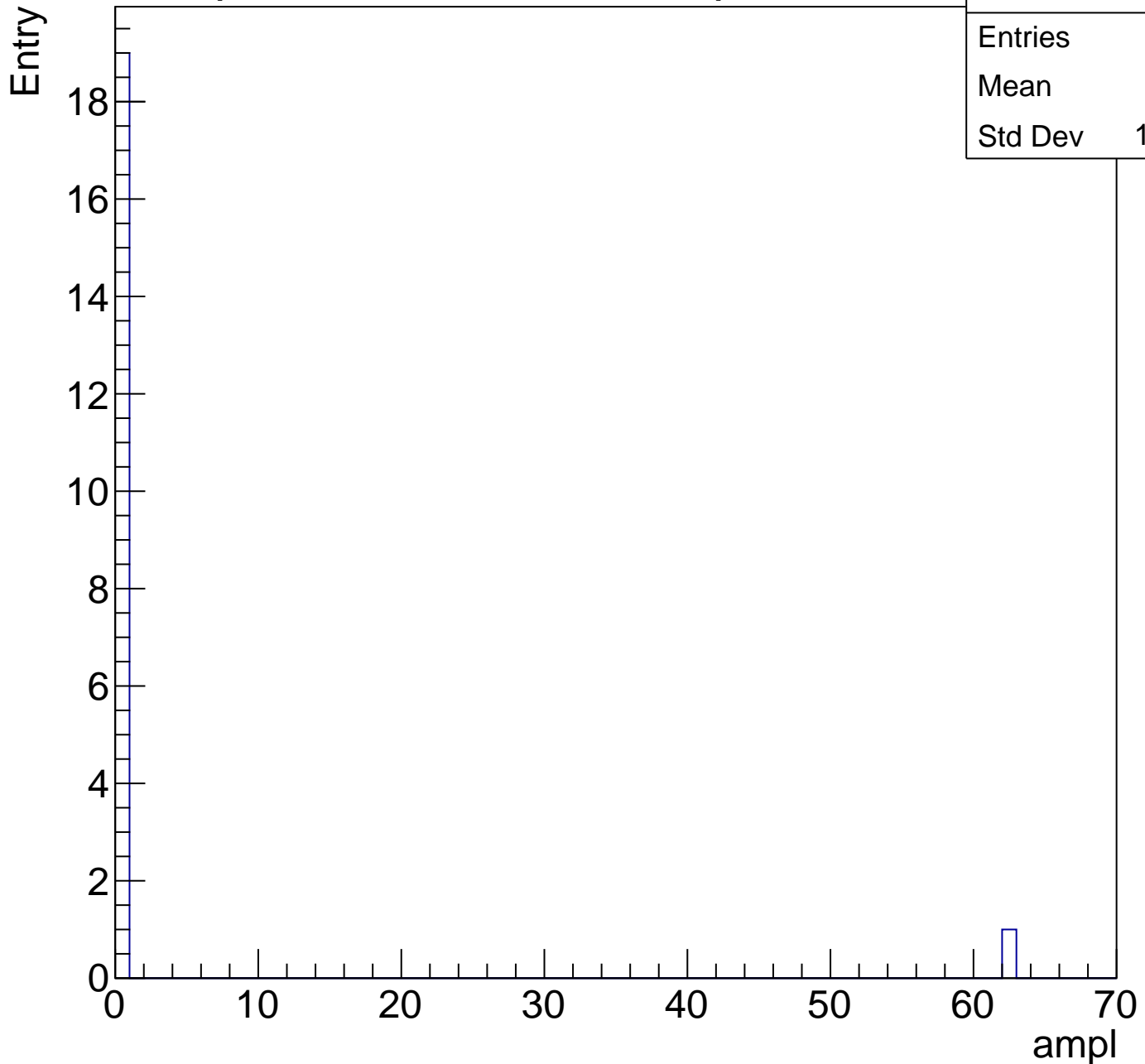




# B1L103S, U26-ch115, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	20
Mean	3.1
Std Dev	13.51



# B1L103S, U26-ch116, adc0

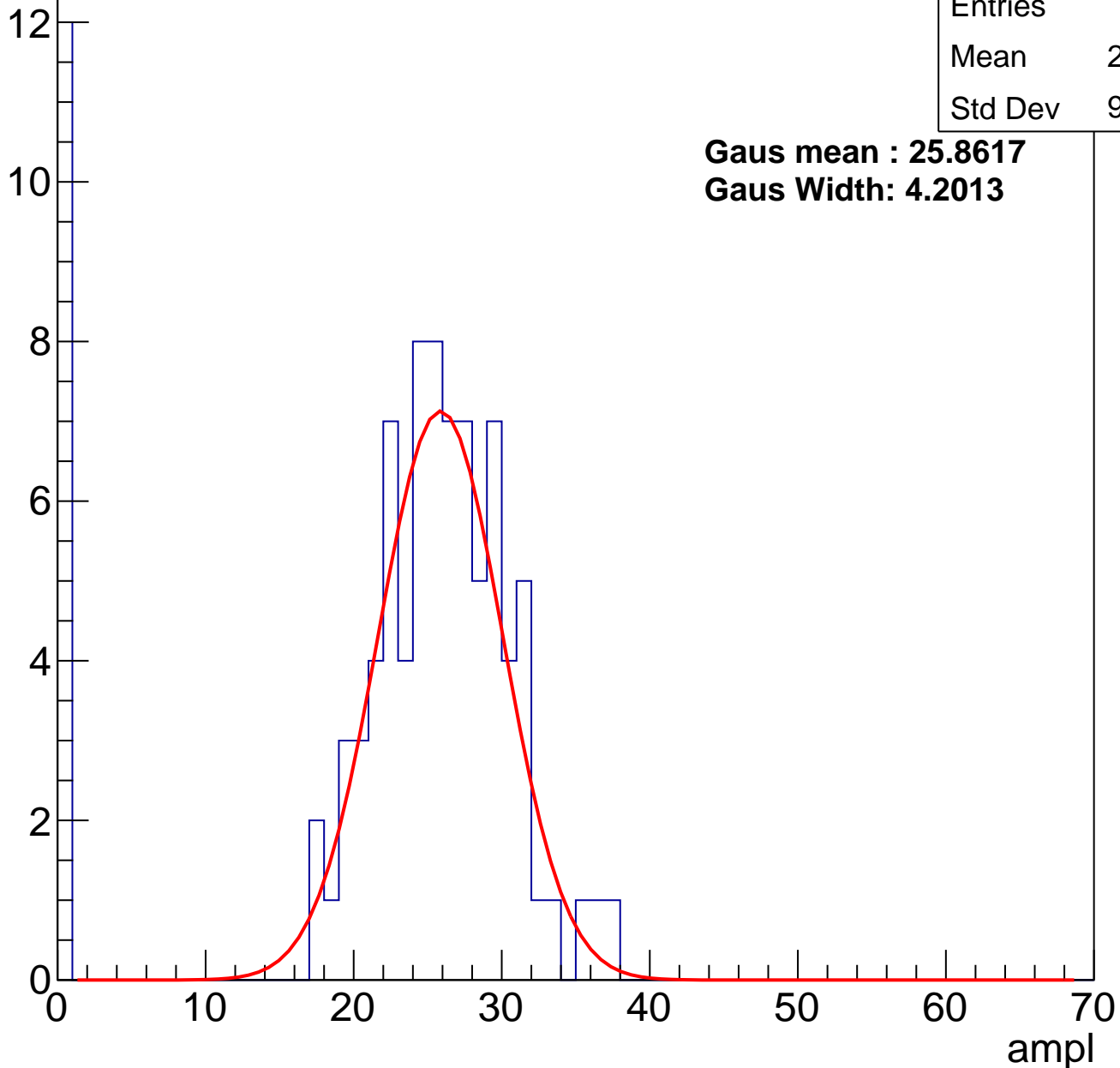
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	92
Mean	22.32
Std Dev	9.497

**Gaus mean : 25.8617**

**Gaus Width: 4.2013**

Entry



# B1L103S, U26-ch116, adc1

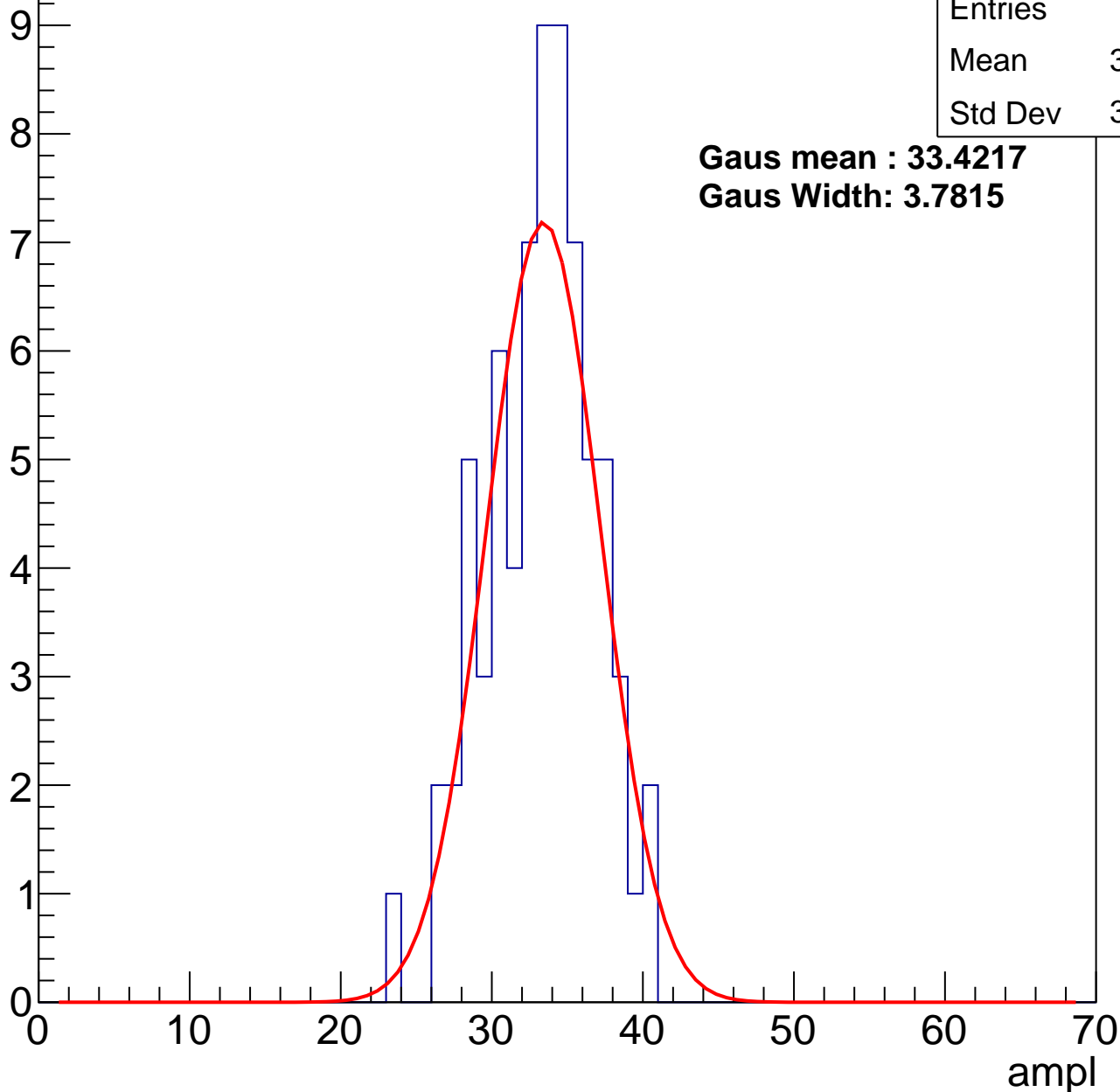
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	71
Mean	32.82
Std Dev	3.538

**Gaus mean : 33.4217**

**Gaus Width: 3.7815**



# B1L103S, U26-ch116, adc2

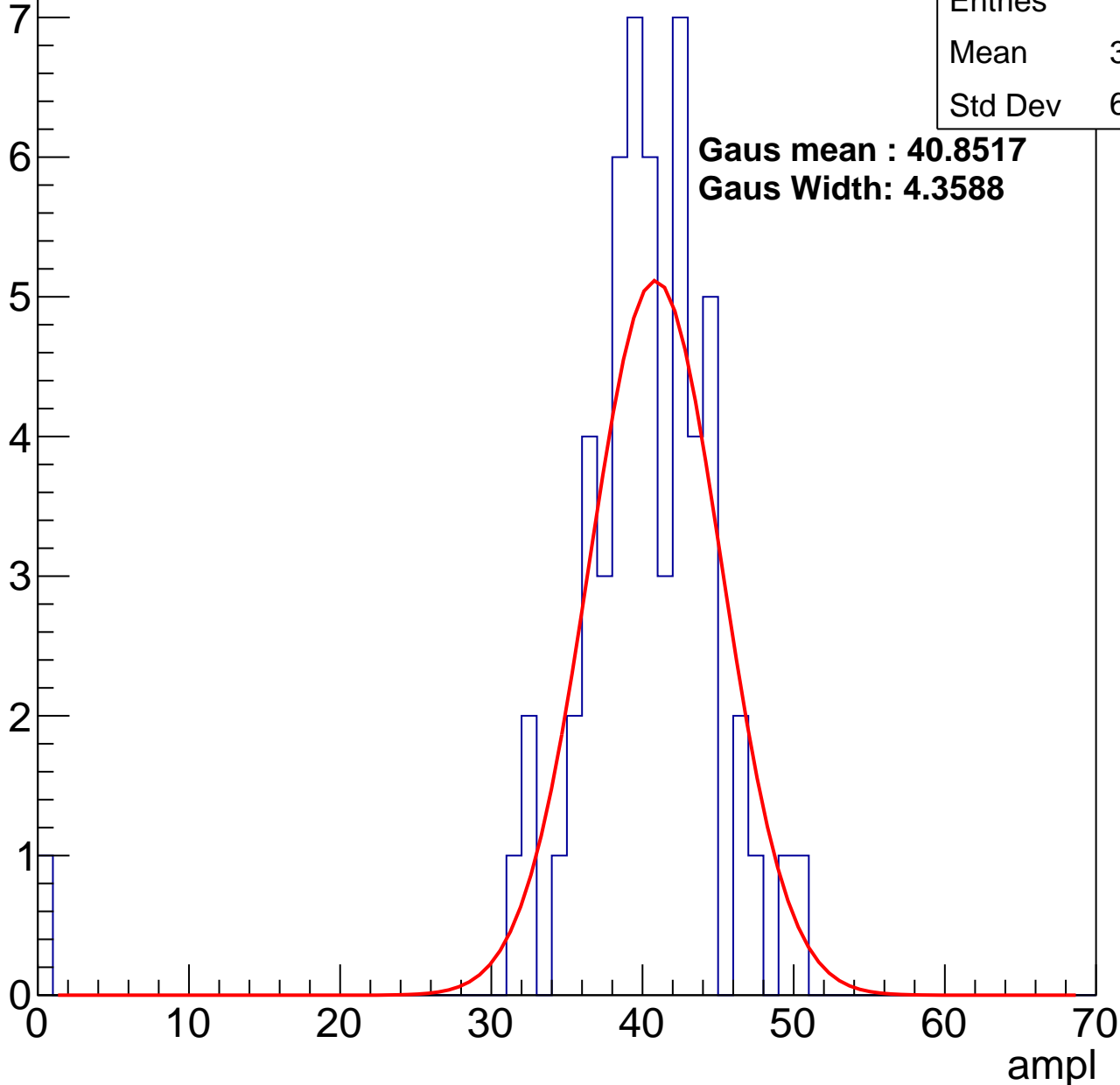
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	57
Mean	39.33
Std Dev	6.544

**Gaus mean : 40.8517**

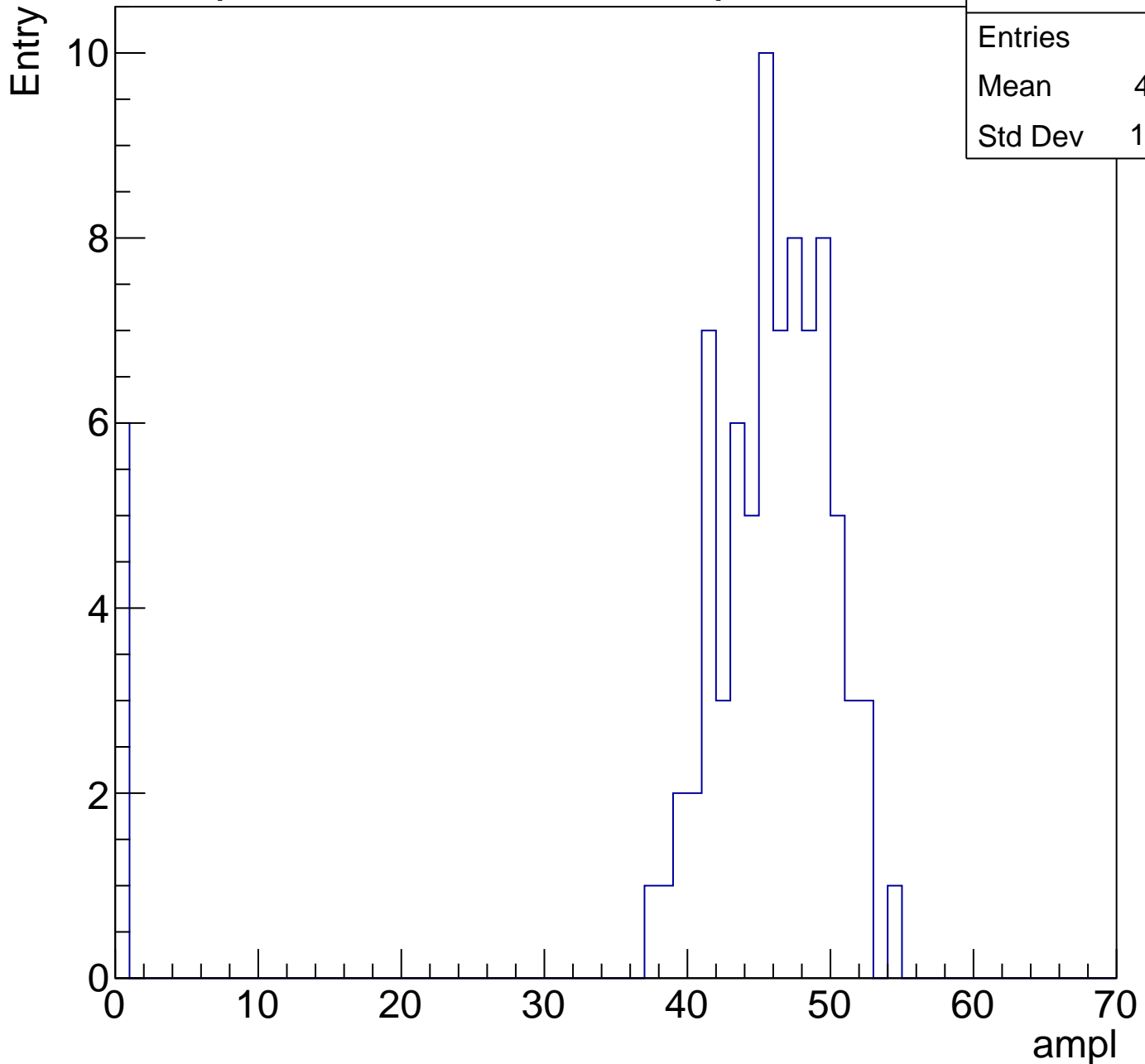
**Gaus Width: 4.3588**



# B1L103S, U26-ch116, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	85
Mean	42.51
Std Dev	12.23



# B1L103S, U26-ch116, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	68
Mean	51.22
Std Dev	11.45

Entry

10

8

6

4

2

0

0

10

20

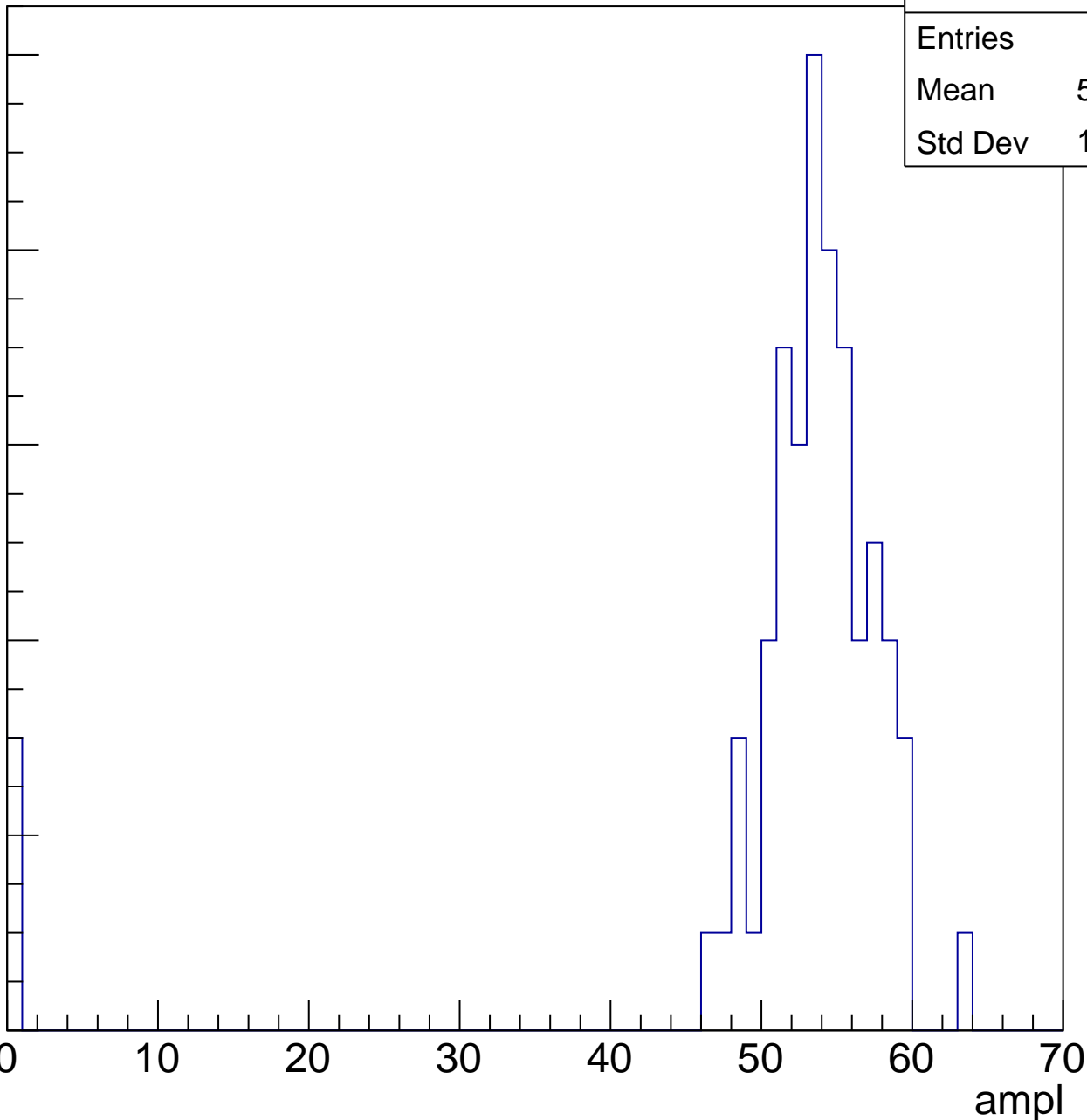
30

40

50

60

ampl

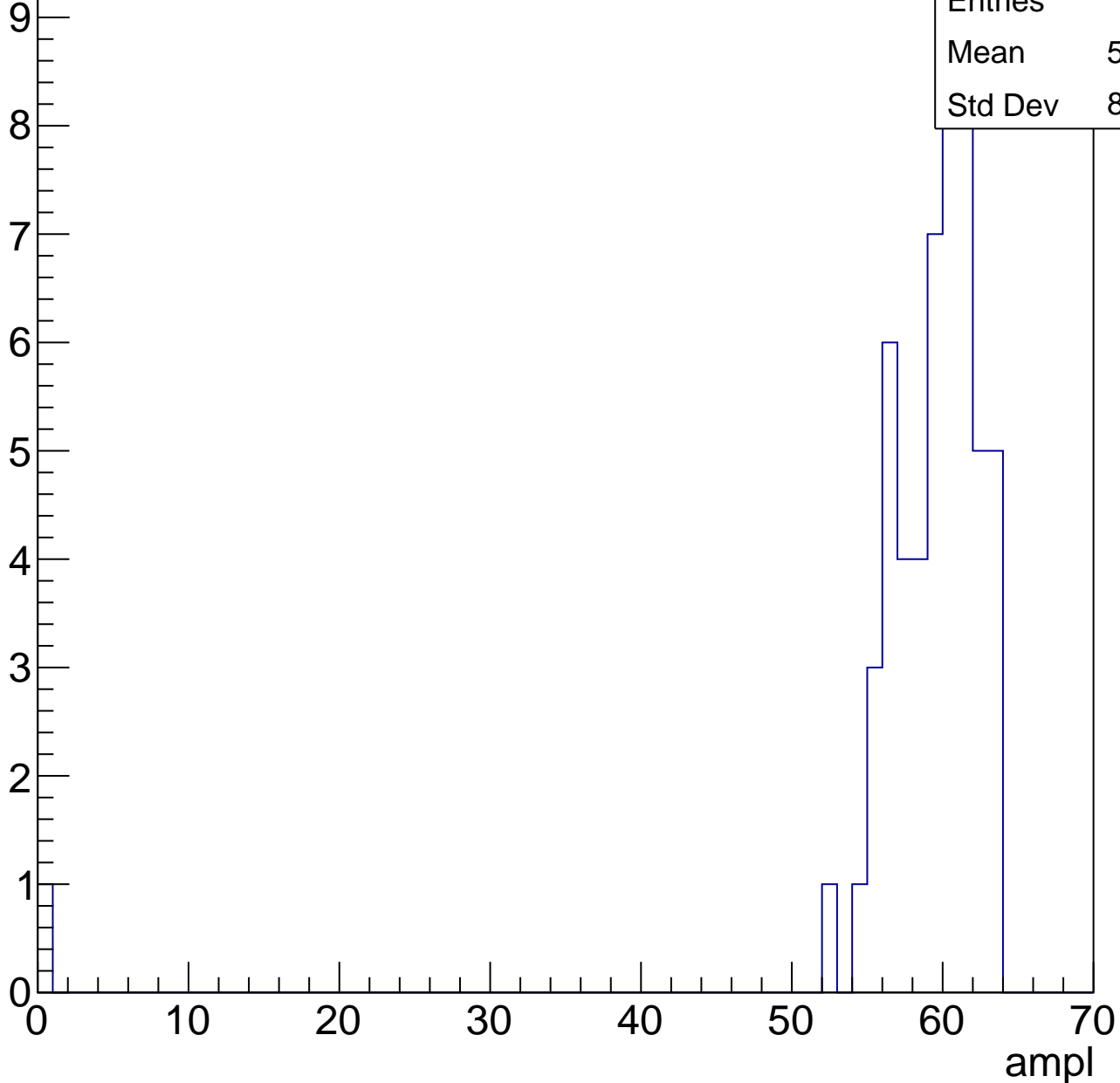


# B1L103S, U26-ch116, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	55
Mean	58.07
Std Dev	8.312

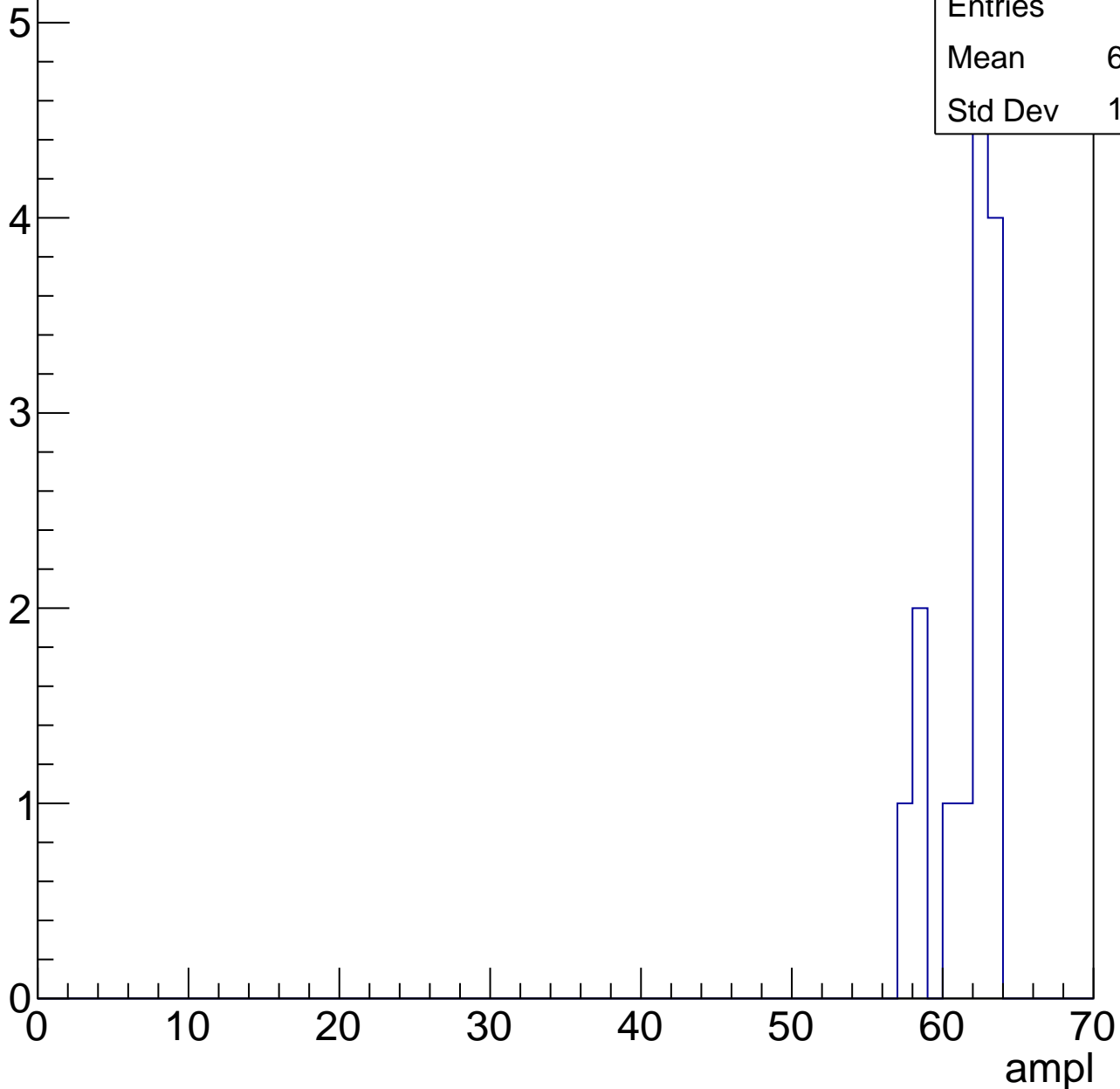


# B1L103S, U26-ch116, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	14
Mean	61.14
Std Dev	1.995





# B1L103S, U26-ch116, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

18  
16  
14  
12  
10  
8  
6  
4  
2  
0

Entries	18
Mean	0
Std Dev	0

ampl

# B1L103S, U26-ch117, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	97
Mean	25.36
Std Dev	11.76

**Gaus mean : 30.6582**

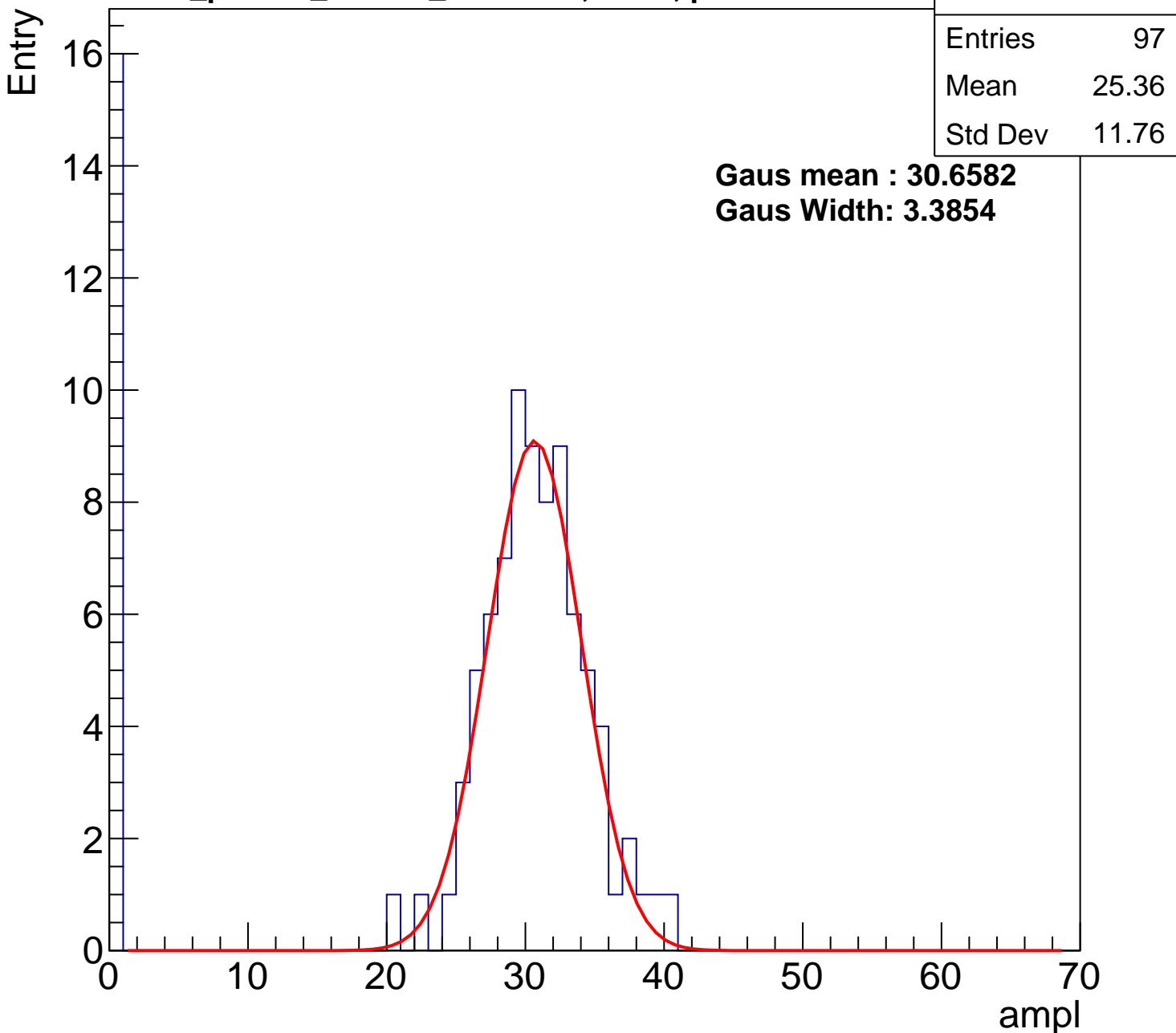
**Gaus Width: 3.3854**

Entry

16  
14  
12  
10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U26-ch117, adc1

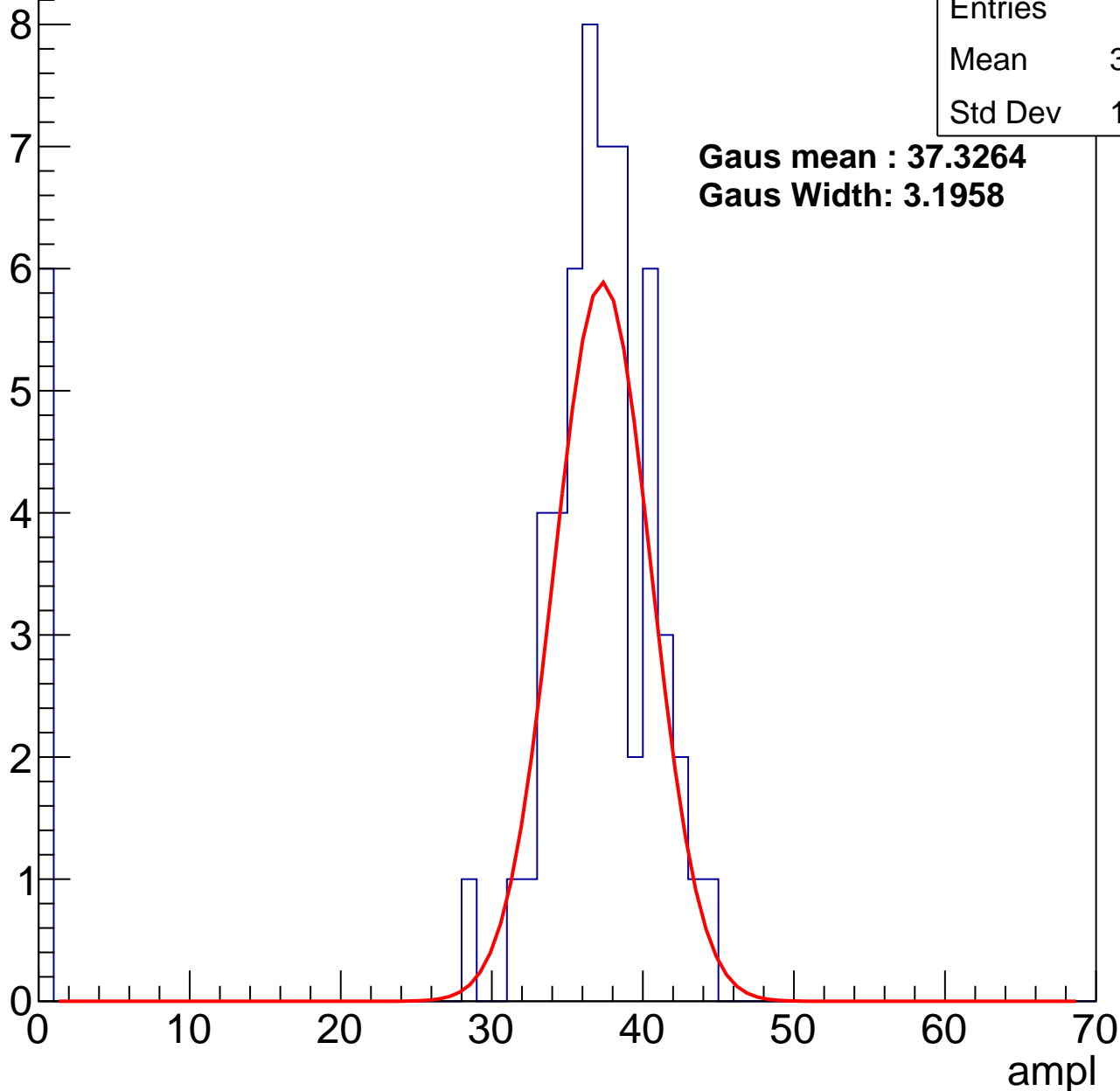
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	60
Mean	33.23
Std Dev	11.47

**Gaus mean : 37.3264**

**Gaus Width: 3.1958**



# B1L103S, U26-ch117, adc2

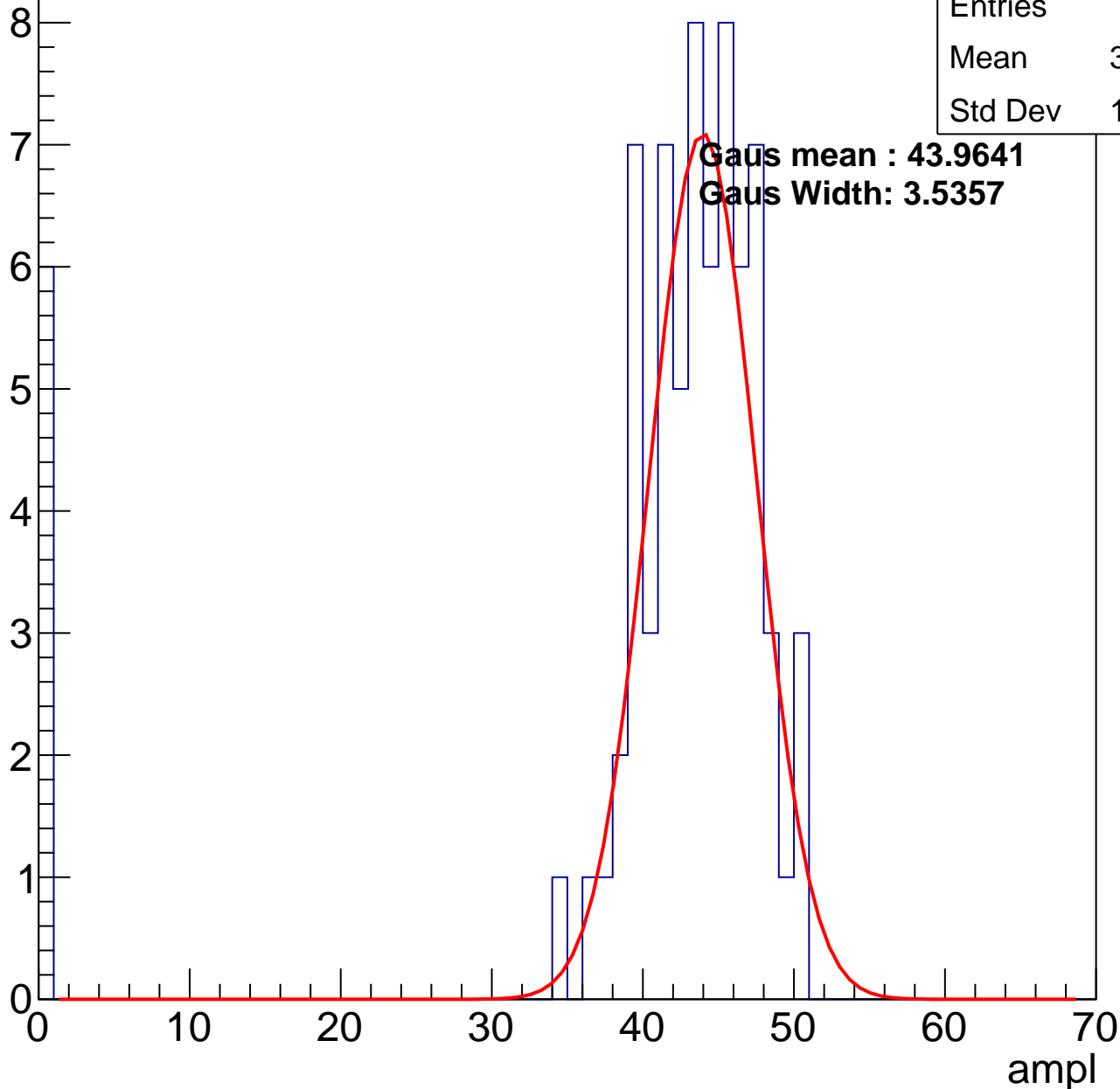
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	75
Mean	39.85
Std Dev	12.22

**Gaus mean : 43.9641**

**Gaus Width: 3.5357**

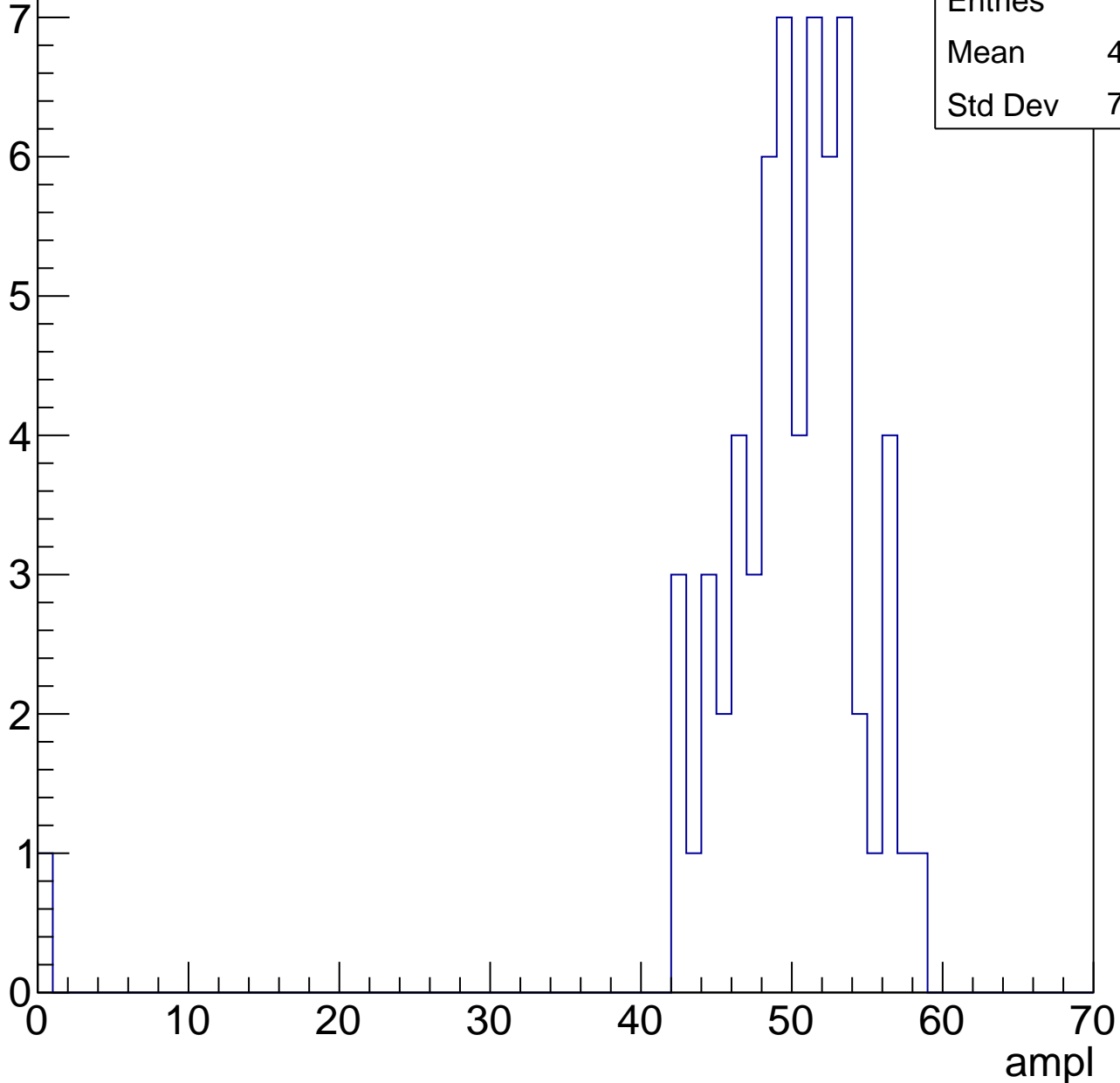


# B1L103S, U26-ch117, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	63
Mean	49.03
Std Dev	7.314

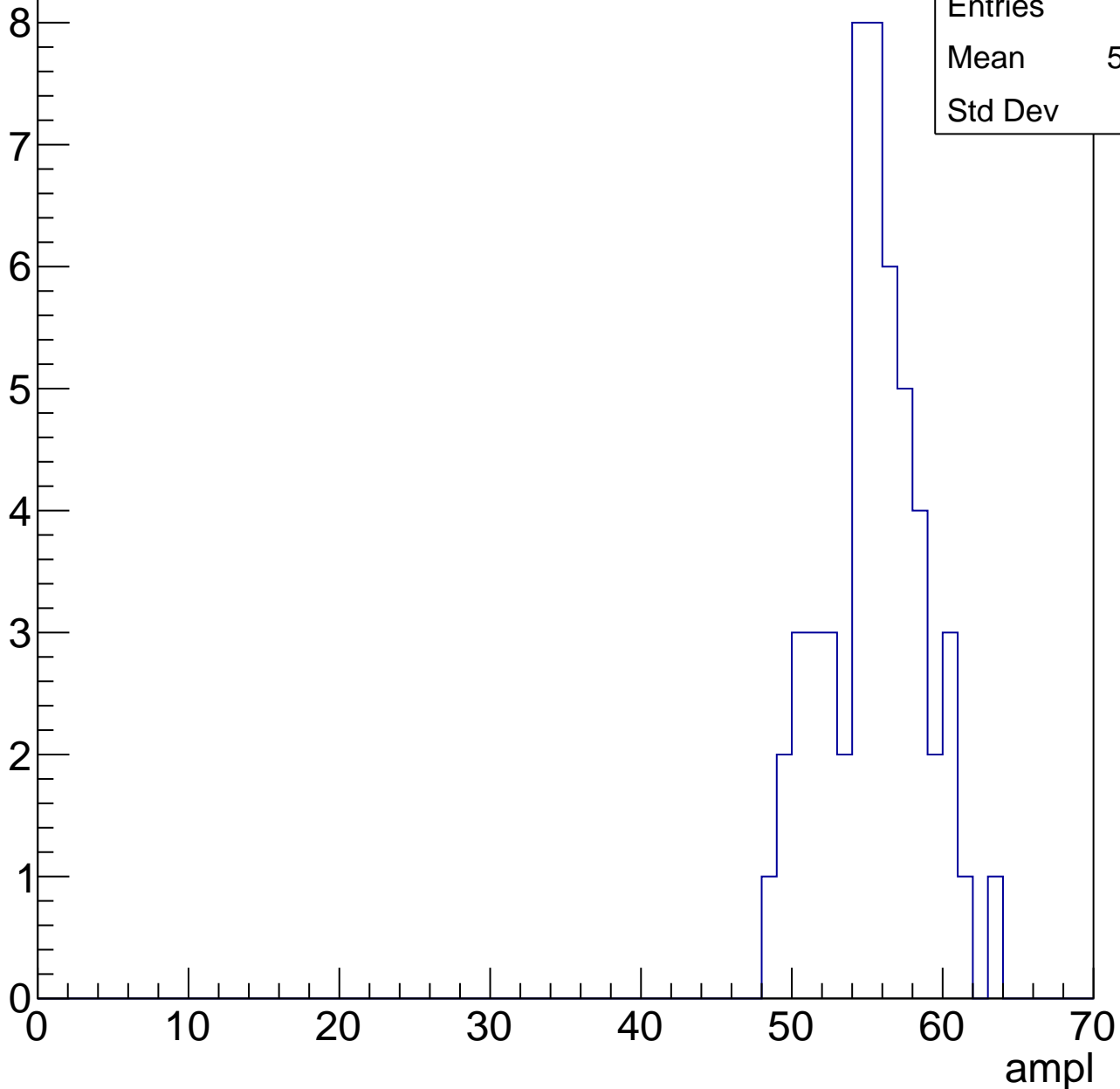


# B1L103S, U26-ch117, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	52
Mean	54.96
Std Dev	3.27

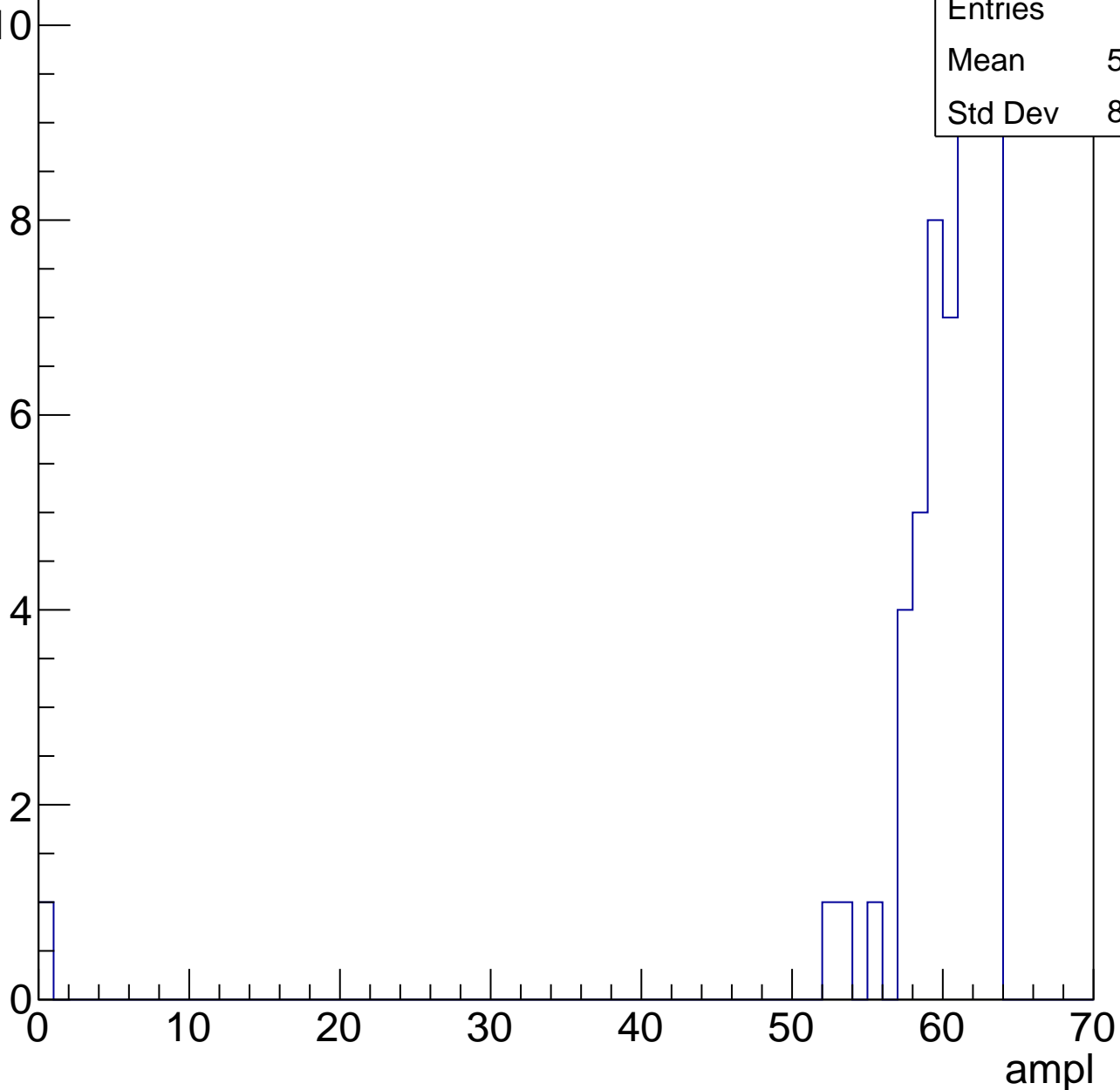


# B1L103S, U26-ch117, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	56
Mean	59.04
Std Dev	8.324



# B1L103S, U26-ch117, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



Entries	0
Mean	0
Std Dev	0



# B1L103S, U26-ch117, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

18  
16  
14  
12  
10  
8  
6  
4  
2  
0

Entries	19
Mean	0
Std Dev	0

ampl

# B1L103S, U26-ch118, adc0

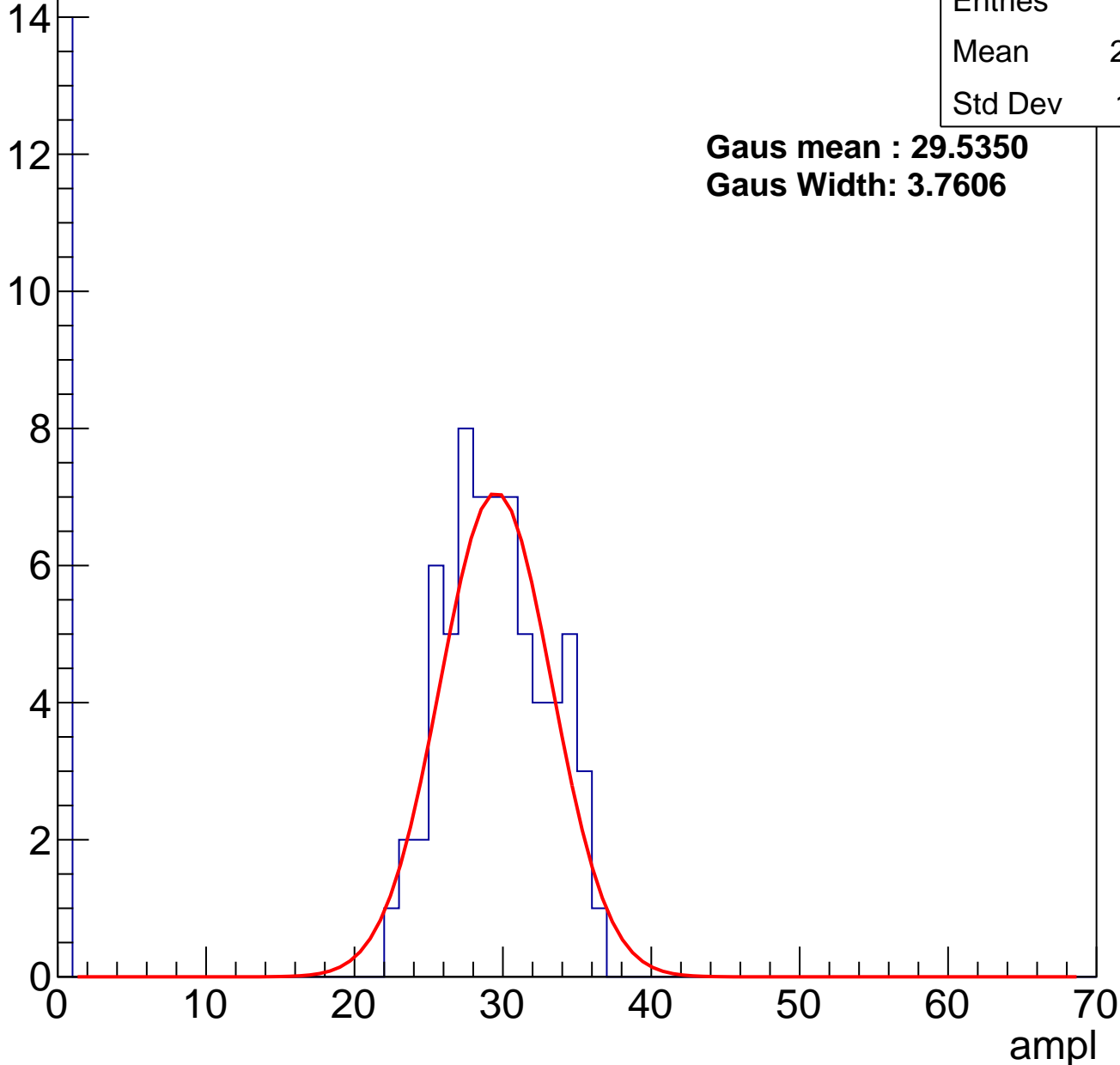
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	81
Mean	24.04
Std Dev	11.41

**Gaus mean : 29.5350**

**Gaus Width: 3.7606**

Entry



# B1L103S, U26-ch118, adc1

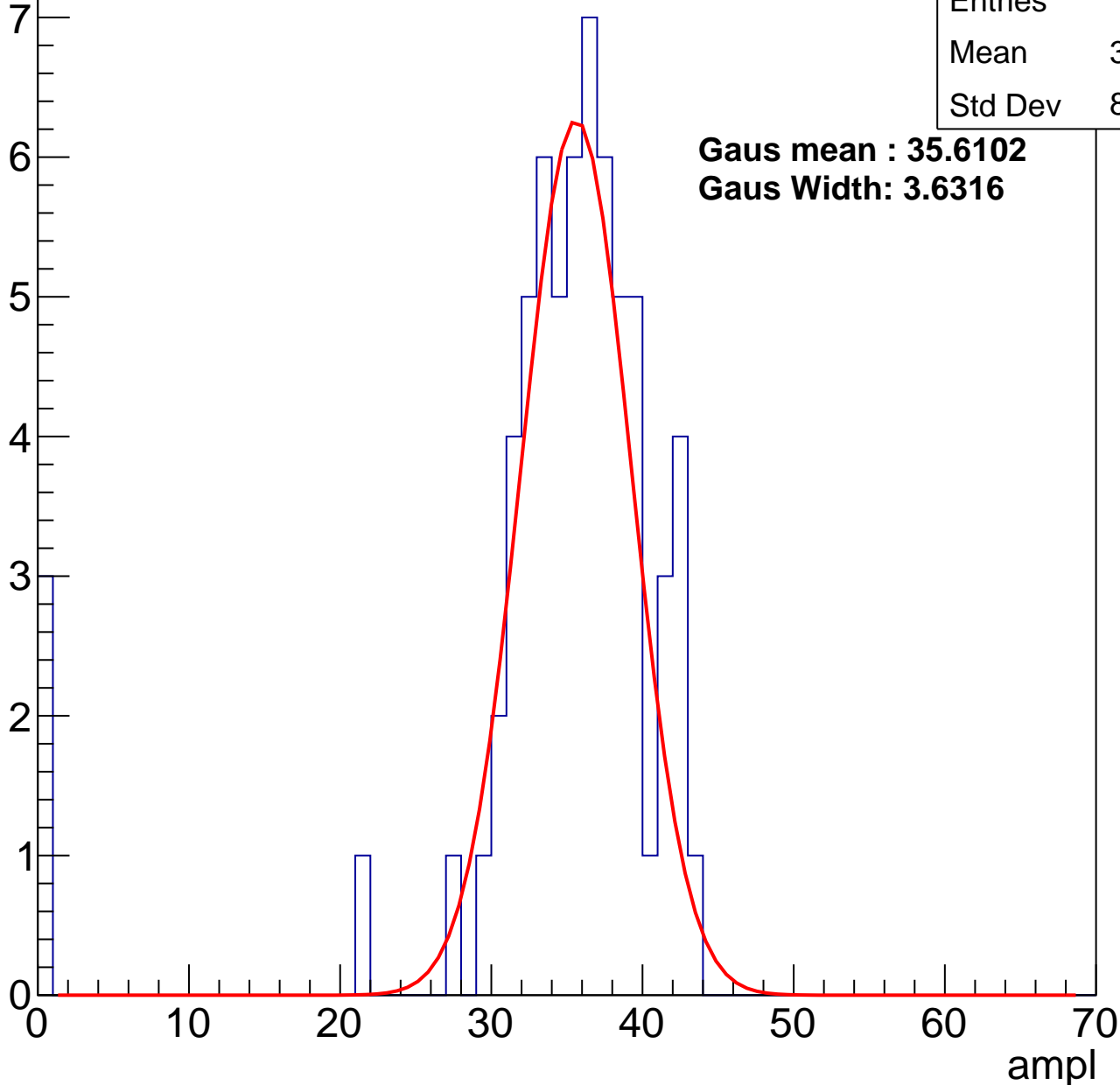
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	66
Mean	33.82
Std Dev	8.363

**Gaus mean : 35.6102**

**Gaus Width: 3.6316**



# B1L103S, U26-ch118, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	85
Mean	36.73
Std Dev	14.58

**Gaus mean : 42.5689**

**Gaus Width: 4.4086**

Entry

10

8

6

4

2

0

0

10

20

30

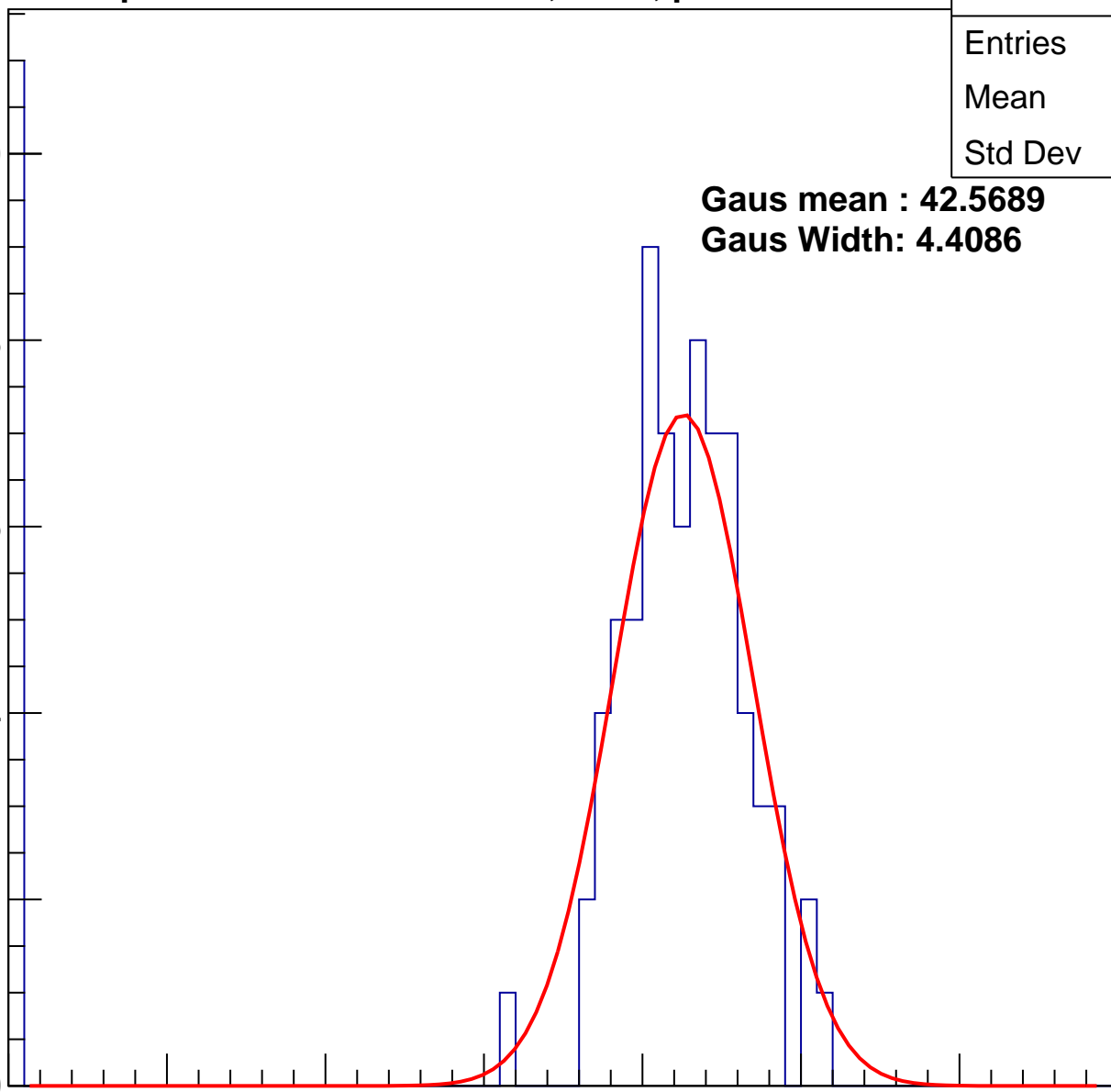
40

50

60

70

ampl

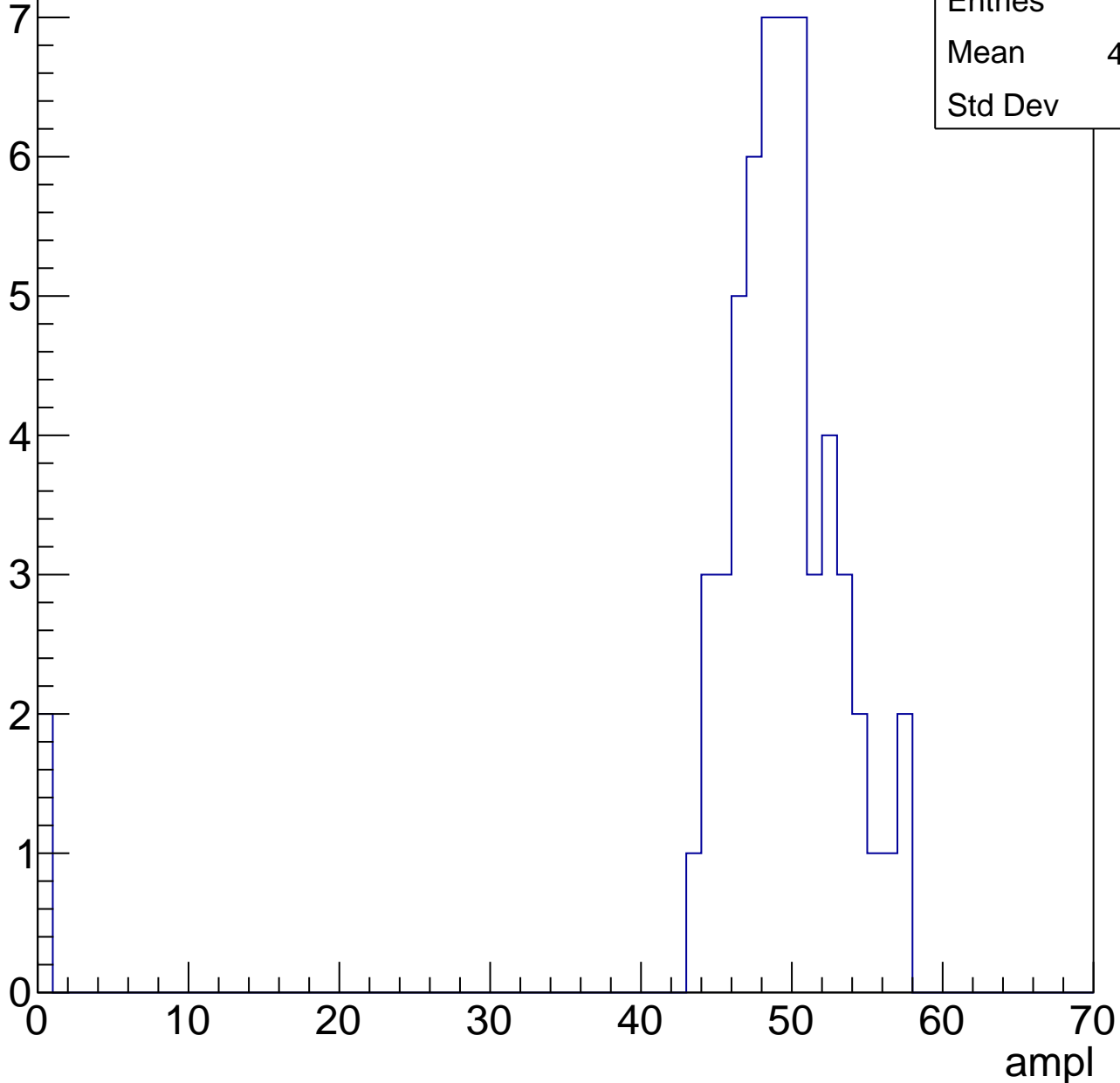


# B1L103S, U26-ch118, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	57
Mean	47.44
Std Dev	9.61

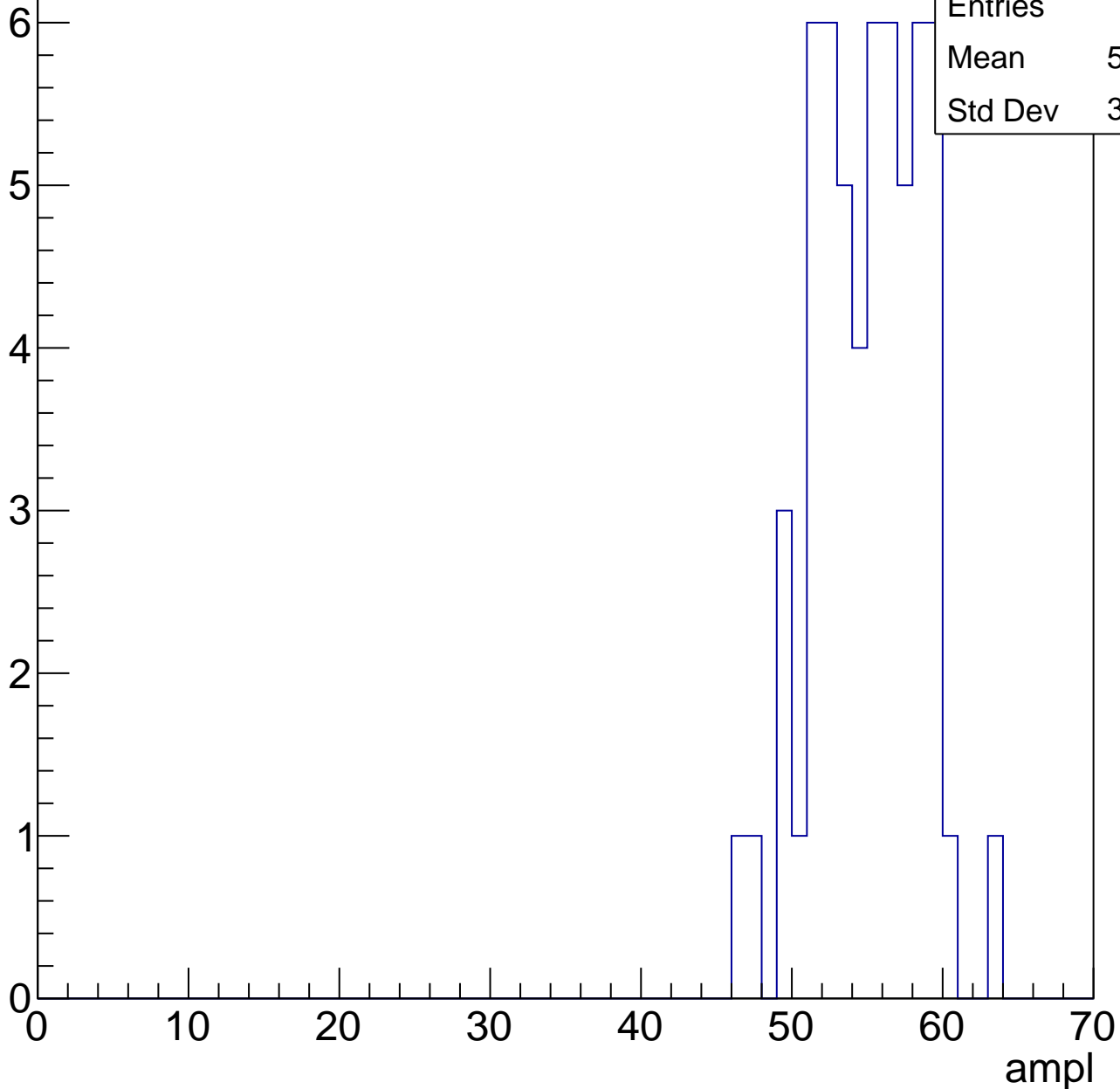


# B1L103S, U26-ch118, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	58
Mean	54.57
Std Dev	3.489

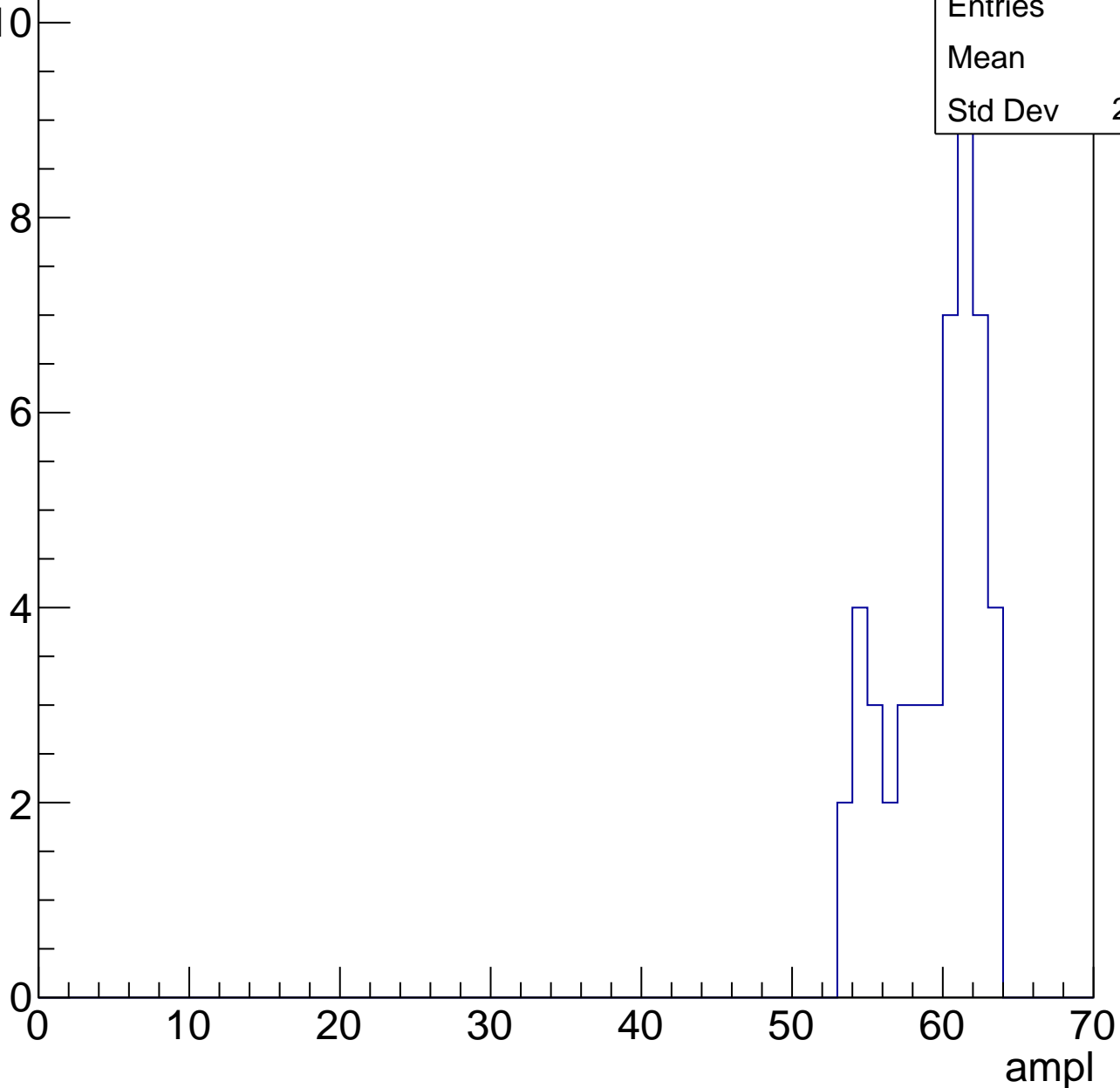


# B1L103S, U26-ch118, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

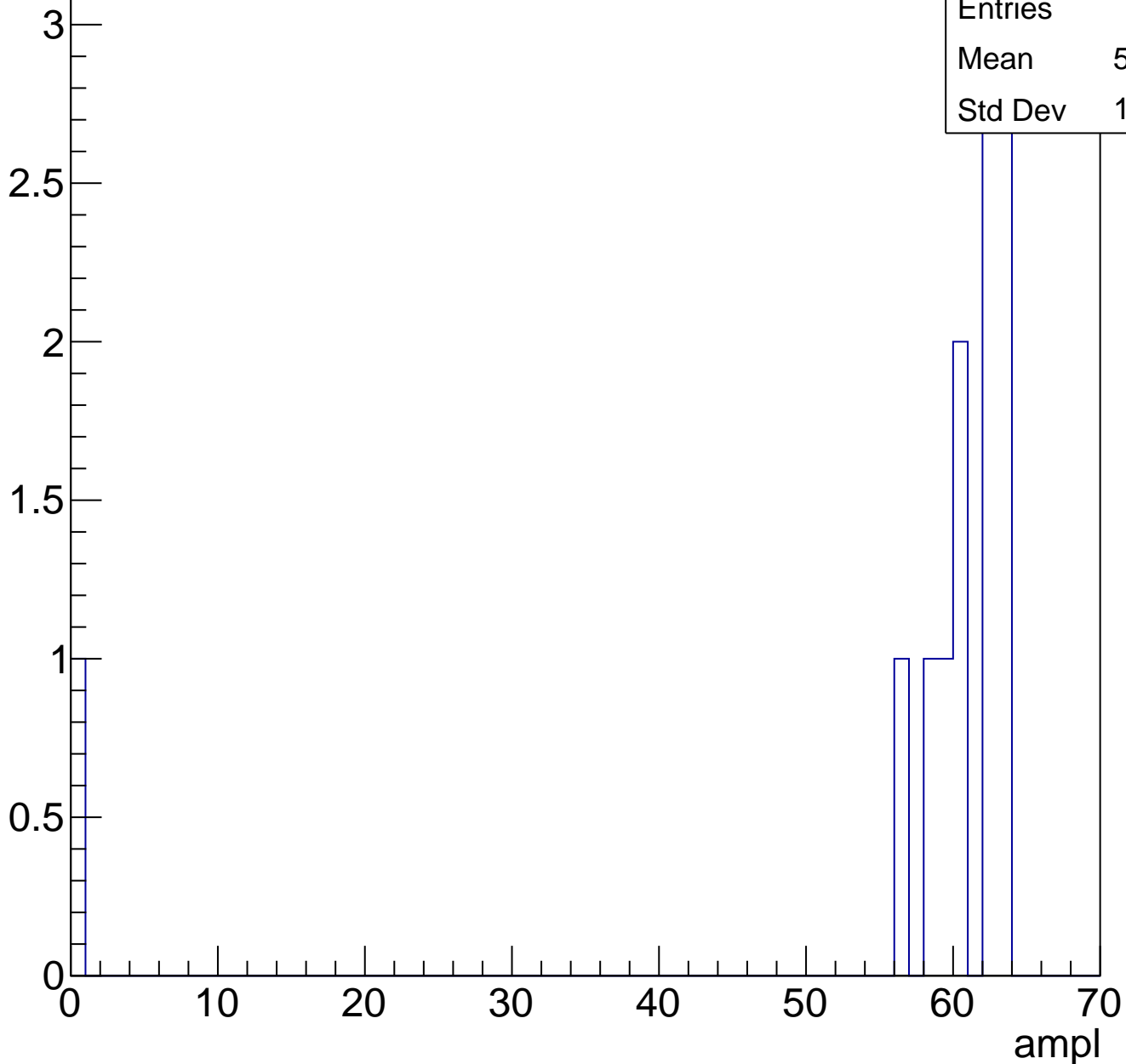
Entries	48
Mean	59.1
Std Dev	2.981



# B1L103S, U26-ch118, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry





# B1L103S, U26-ch118, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	21
Mean	6
Std Dev	18.49

Entry



# B1L103S, U26-ch119, adc0

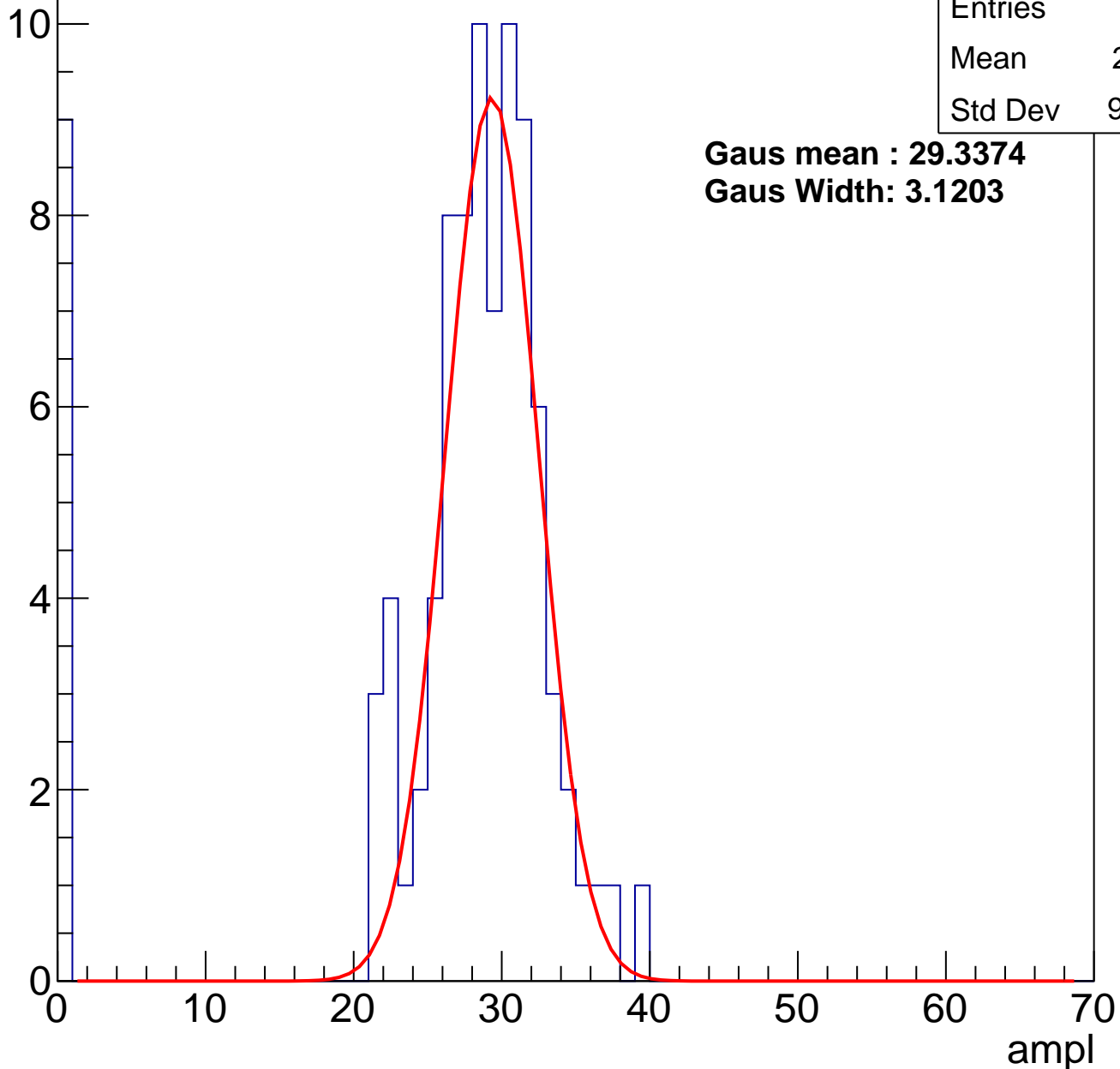
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	90
Mean	25.71
Std Dev	9.246

**Gaus mean : 29.3374**

**Gaus Width: 3.1203**

Entry



# B1L103S, U26-ch119, adc1

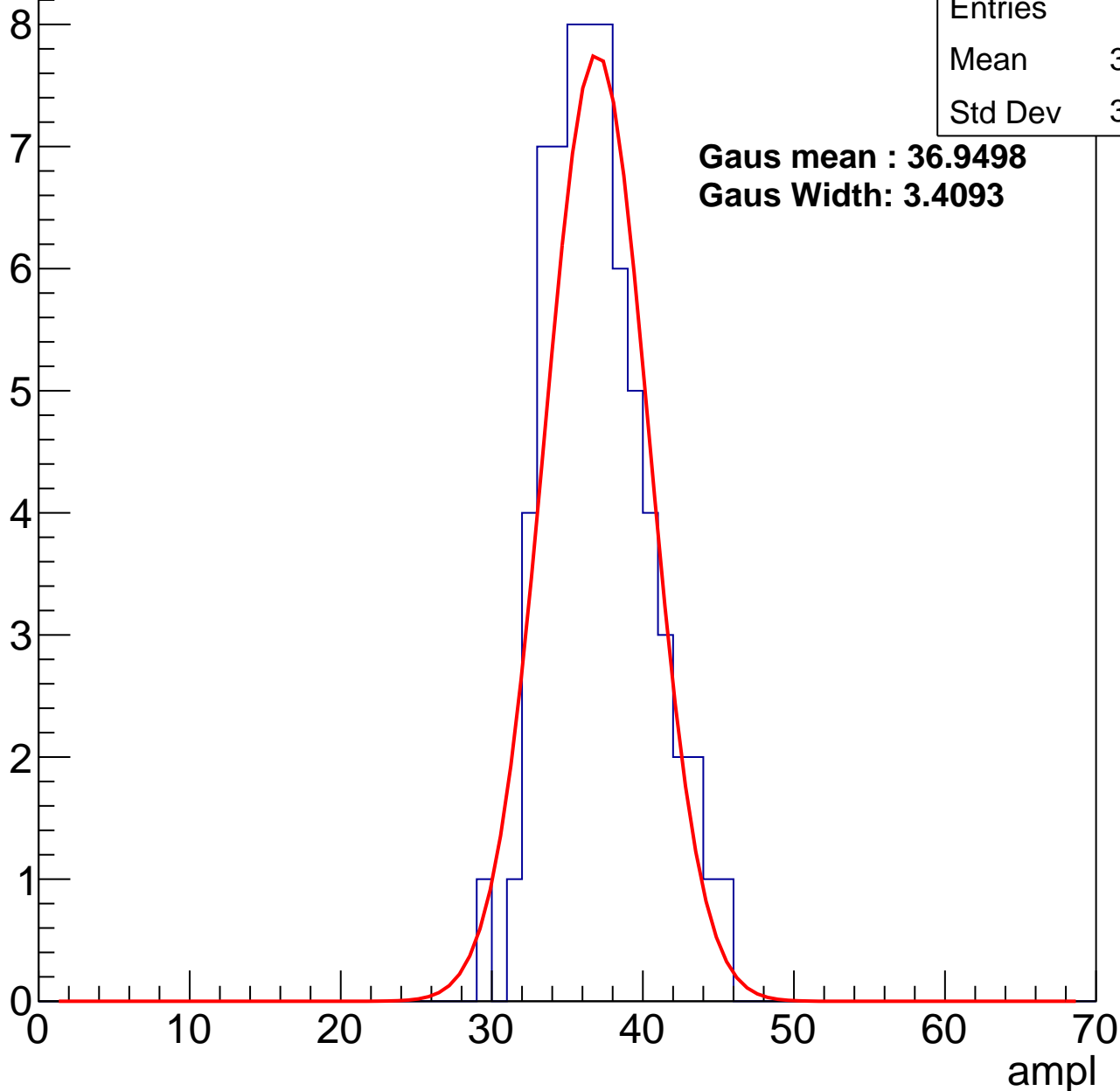
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	68
Mean	36.56
Std Dev	3.314

**Gaus mean : 36.9498**

**Gaus Width: 3.4093**

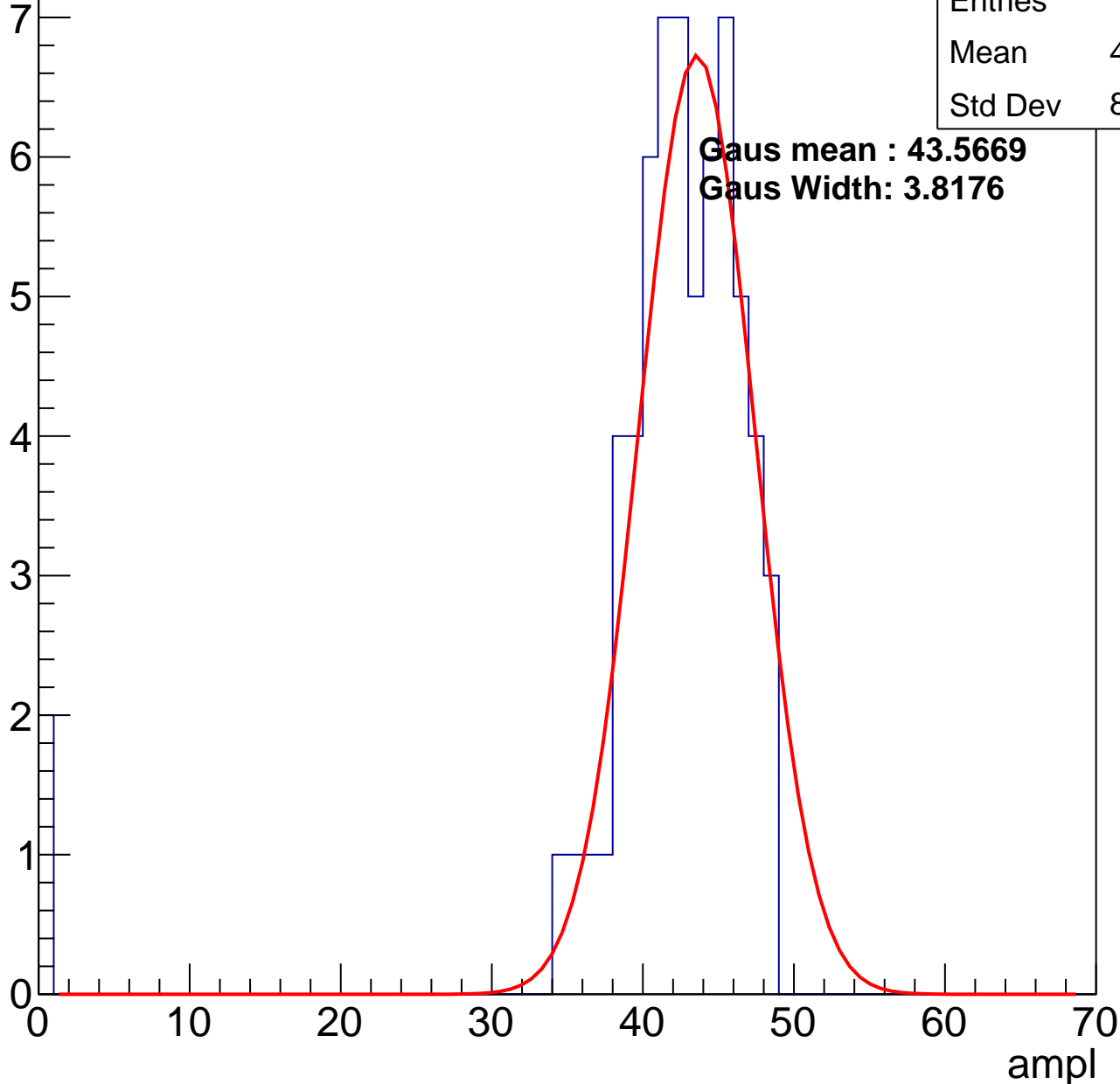


# B1L103S, U26-ch119, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	64
Mean	41.05
Std Dev	8.057



# B1L103S, U26-ch119, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	75
Mean	41.93
Std Dev	17.64

Entry

10

8

6

4

2

0

0

10

20

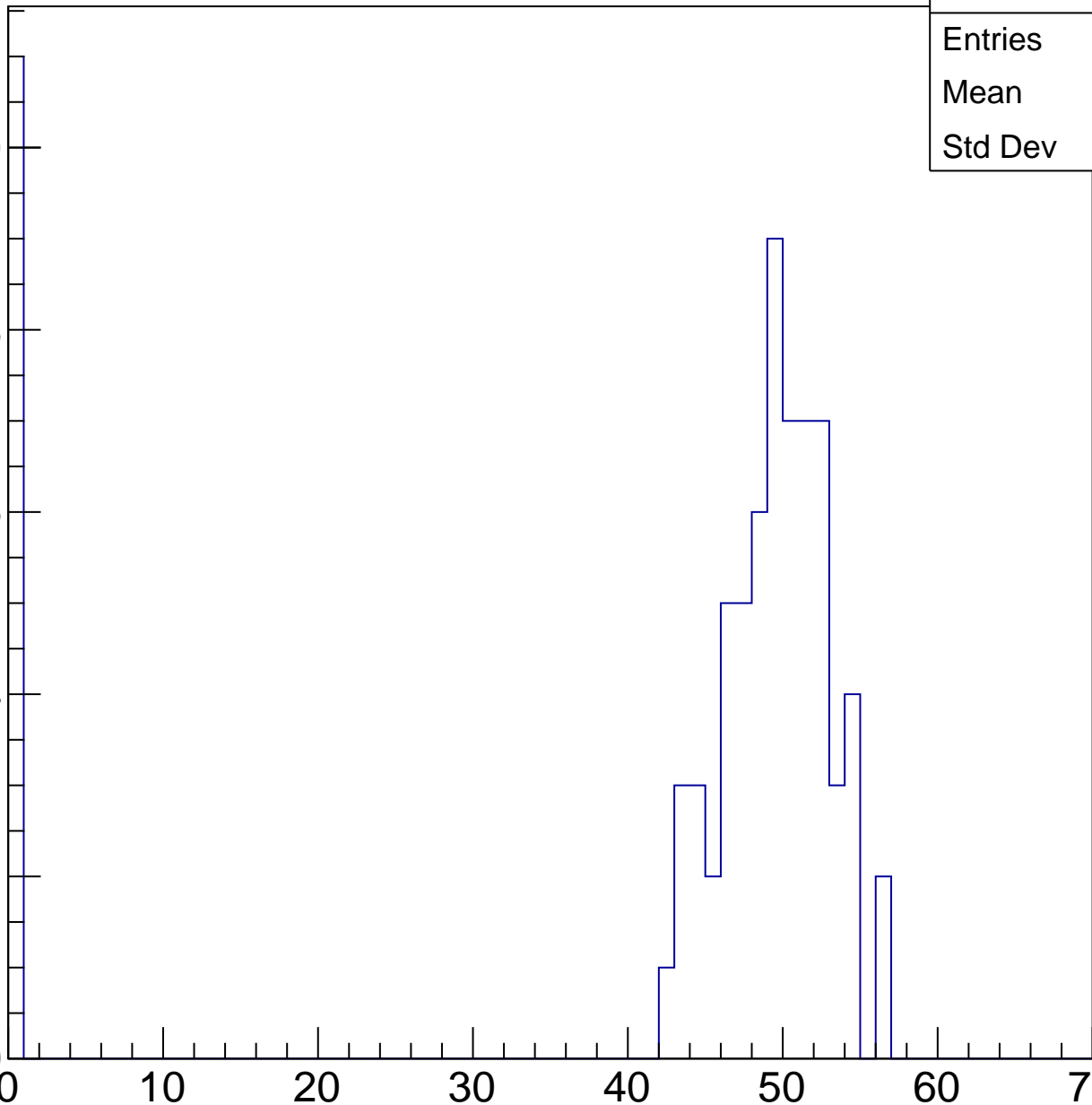
30

40

50

60

ampl



# B1L103S, U26-ch119, adc4

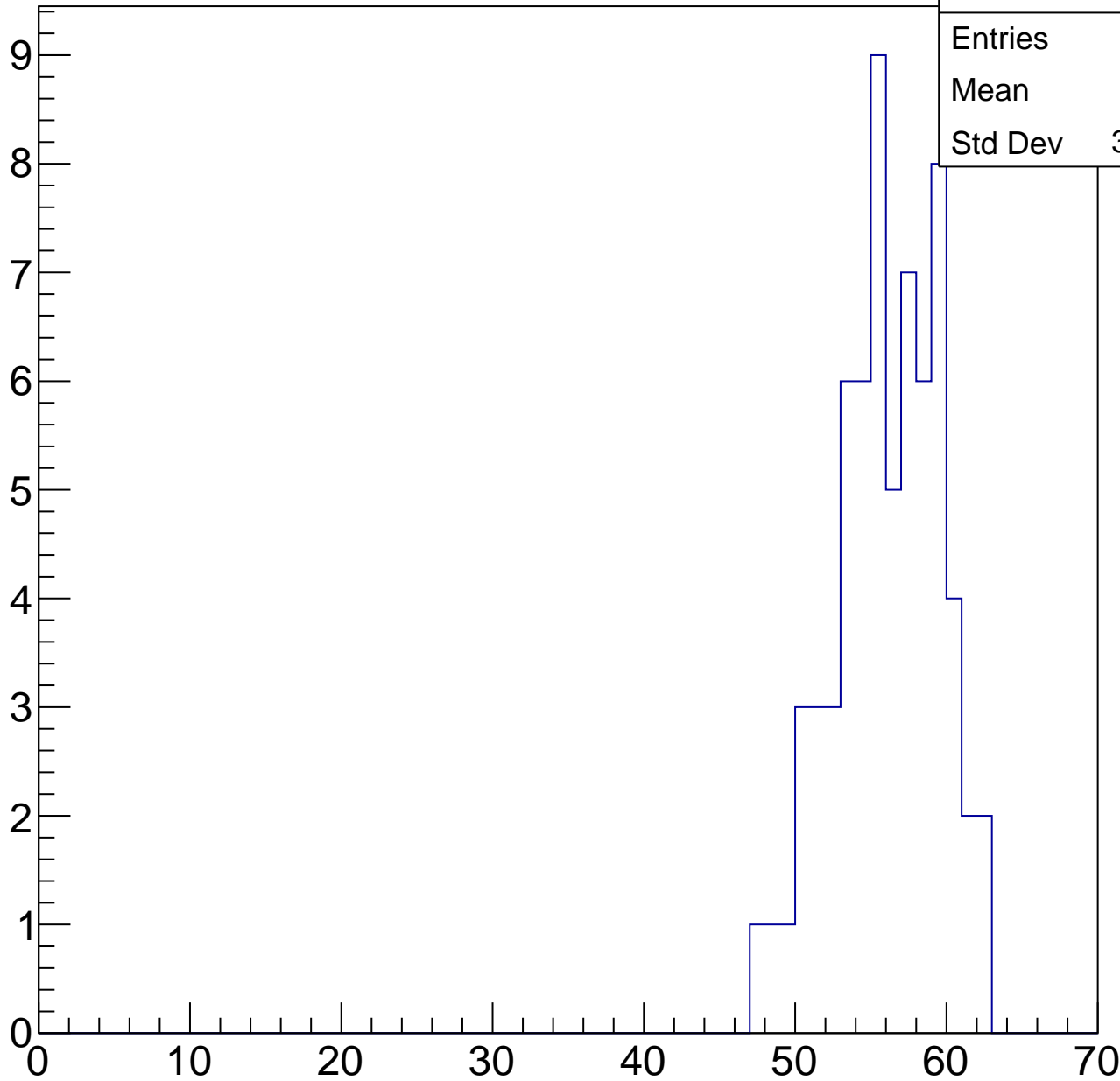
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	67
Mean	55.6
Std Dev	3.434

ampl

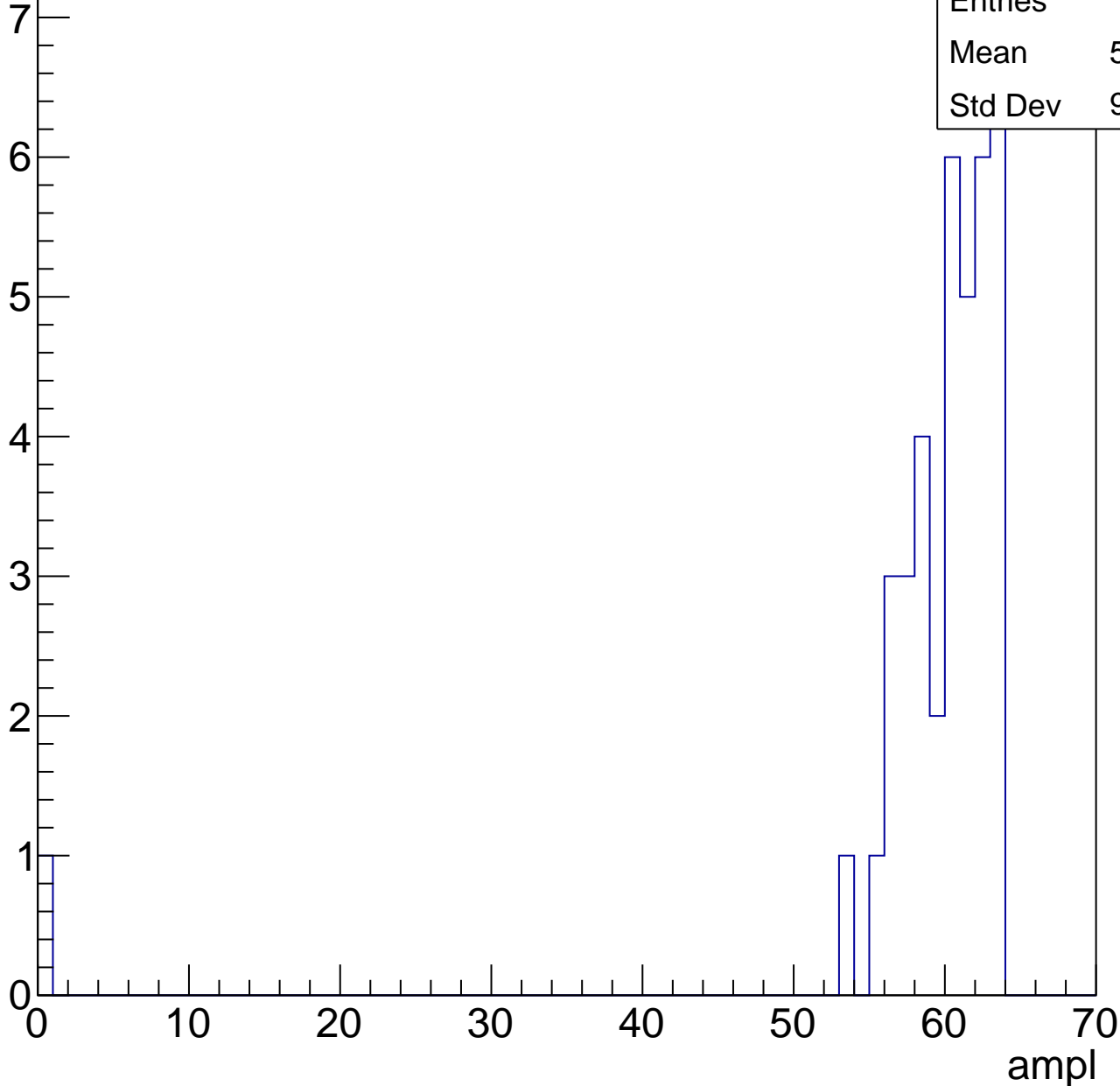


# B1L103S, U26-ch119, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	39
Mean	58.33
Std Dev	9.807



# B1L103S, U26-ch119, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

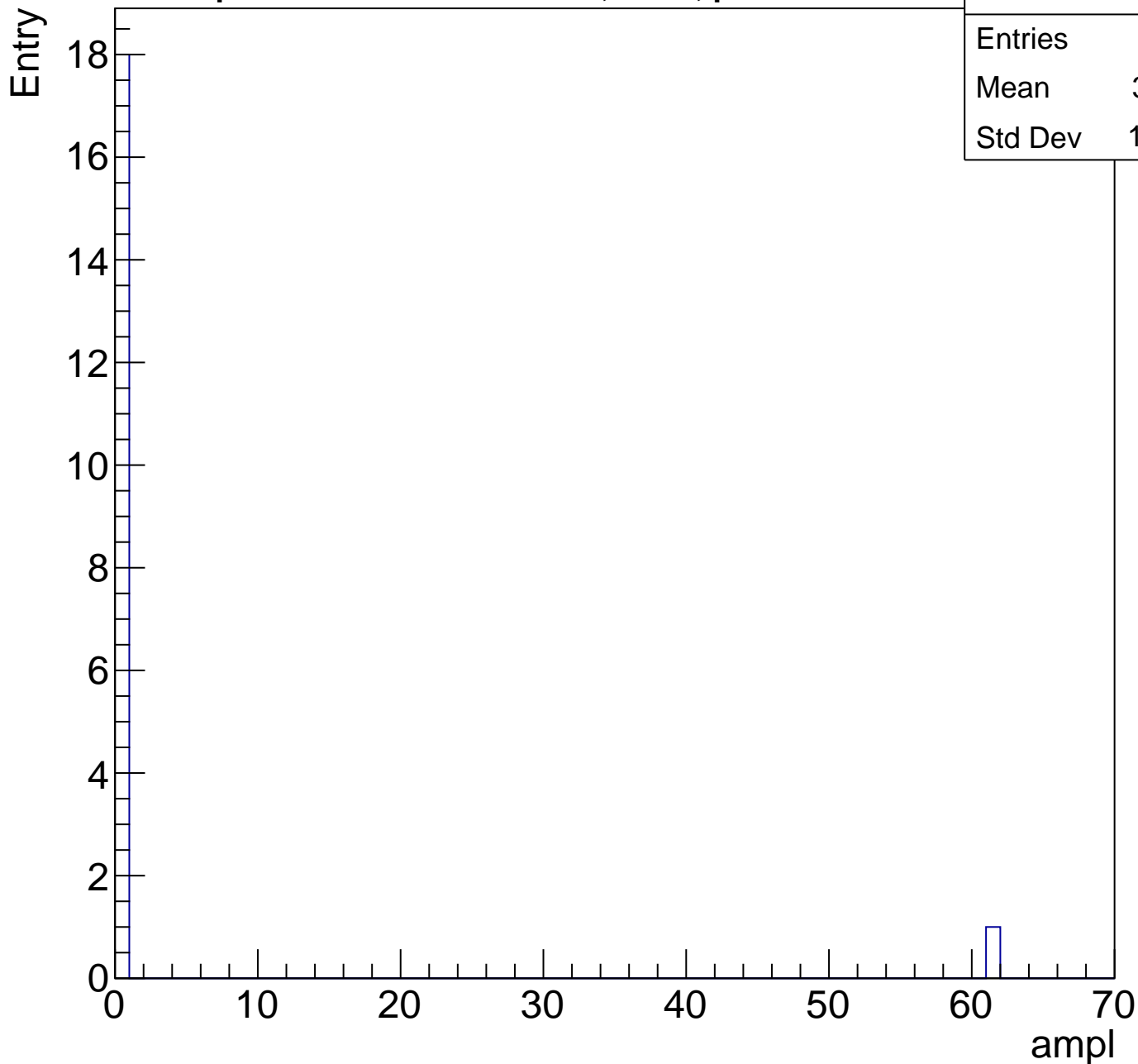




# B1L103S, U26-ch119, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	19
Mean	3.211
Std Dev	13.62



# B1L103S, U26-ch120, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	86
Mean	22.6
Std Dev	10.16

**Gaus mean : 27.4435**

**Gaus Width: 3.8396**

Entry

12

10

8

6

4

2

0

0

10

20

30

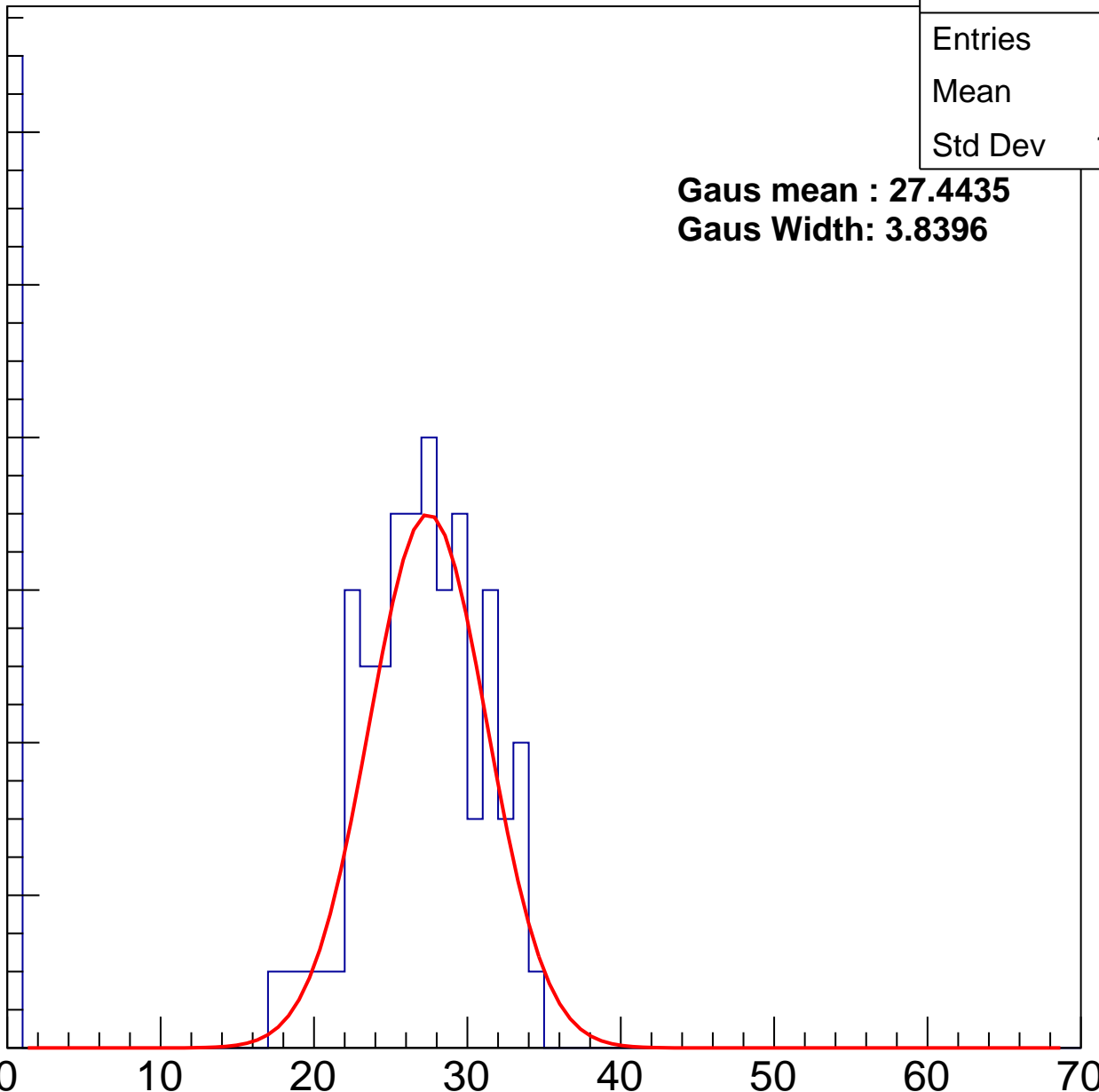
40

50

60

70

ampl



# B1L103S, U26-ch120, adc1

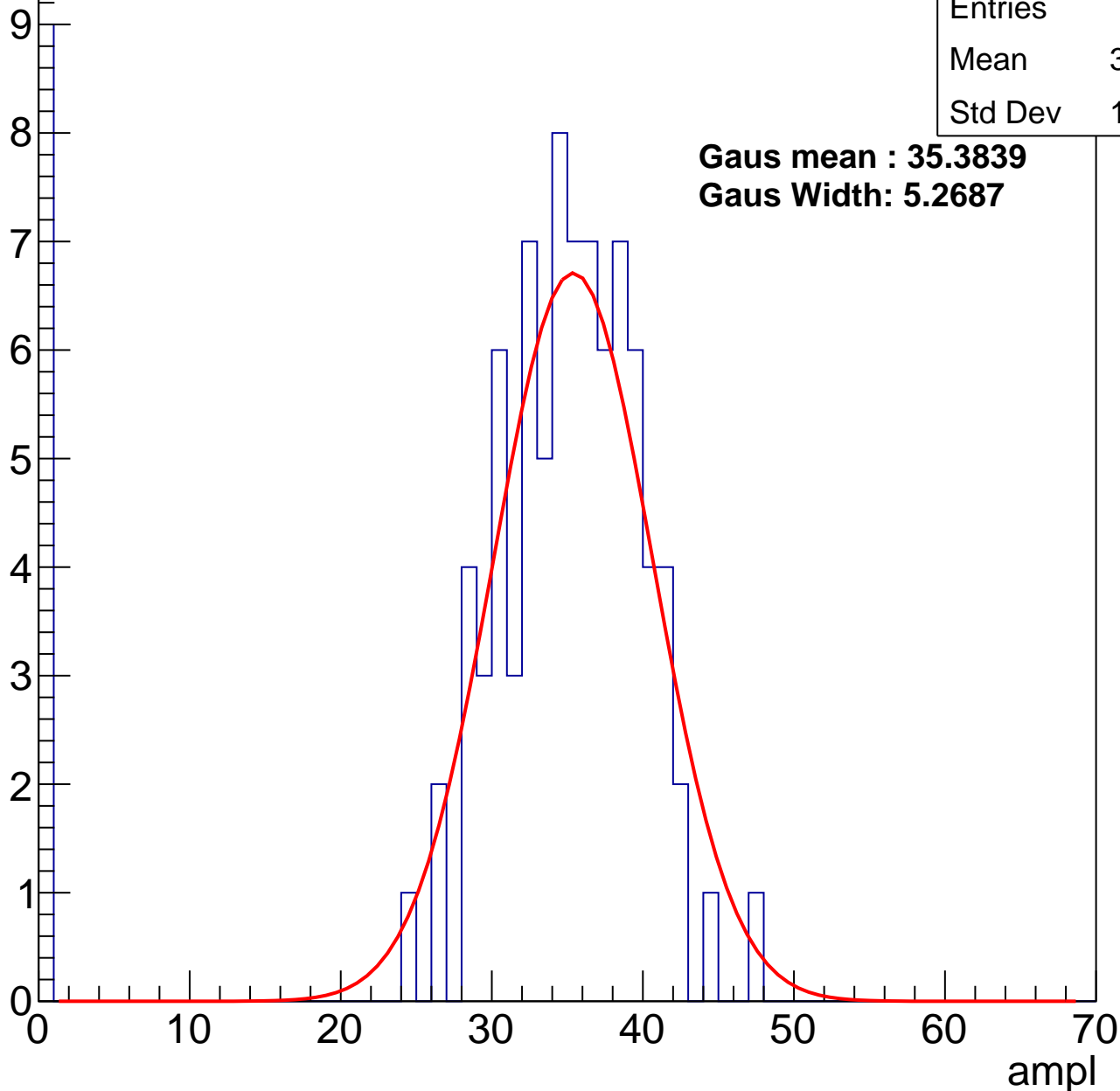
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	93
Mean	31.47
Std Dev	11.12

**Gaus mean : 35.3839**

**Gaus Width: 5.2687**



# B1L103S, U26-ch120, adc2

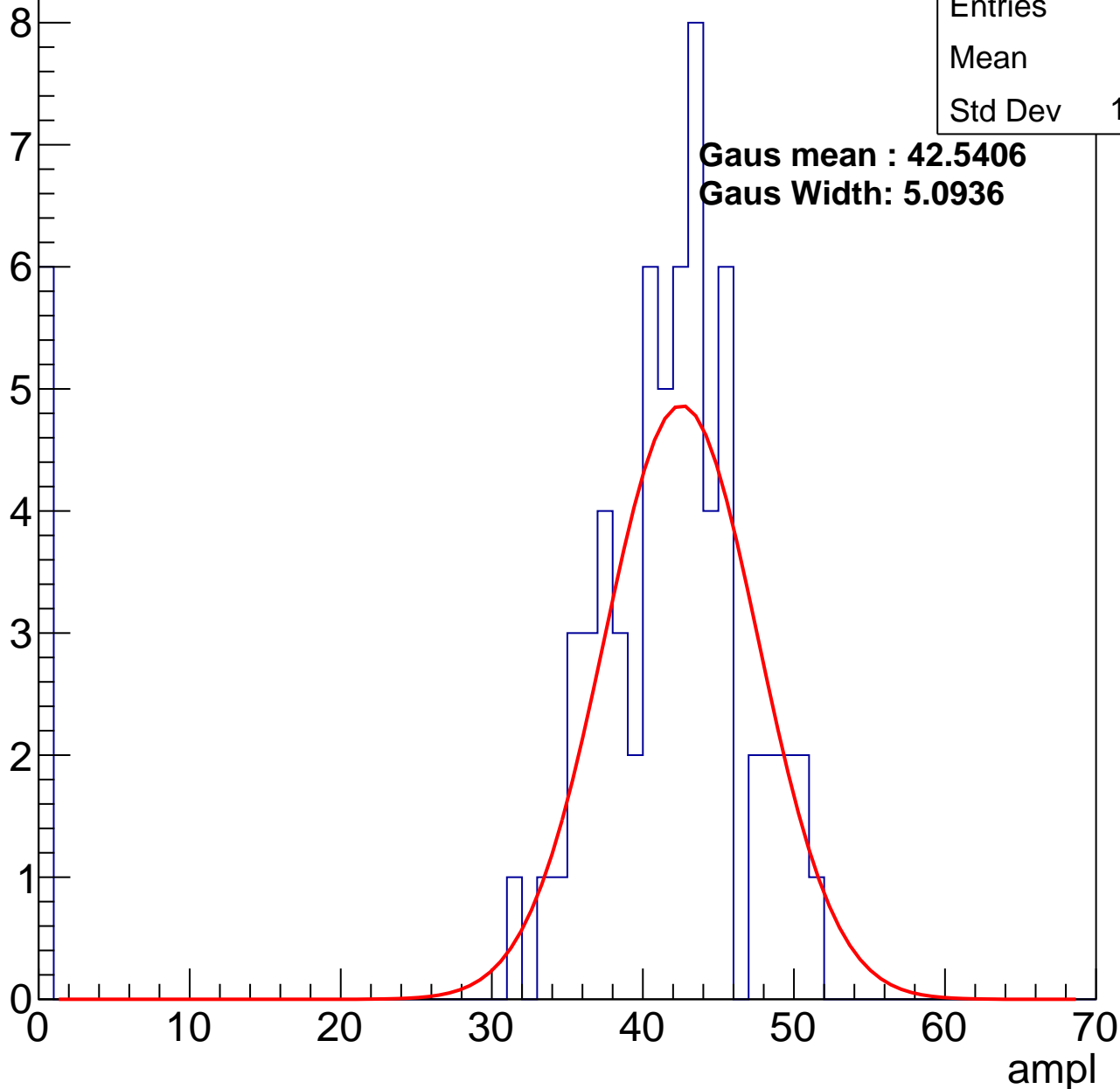
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	68
Mean	37.9
Std Dev	12.52

**Gaus mean : 42.5406**

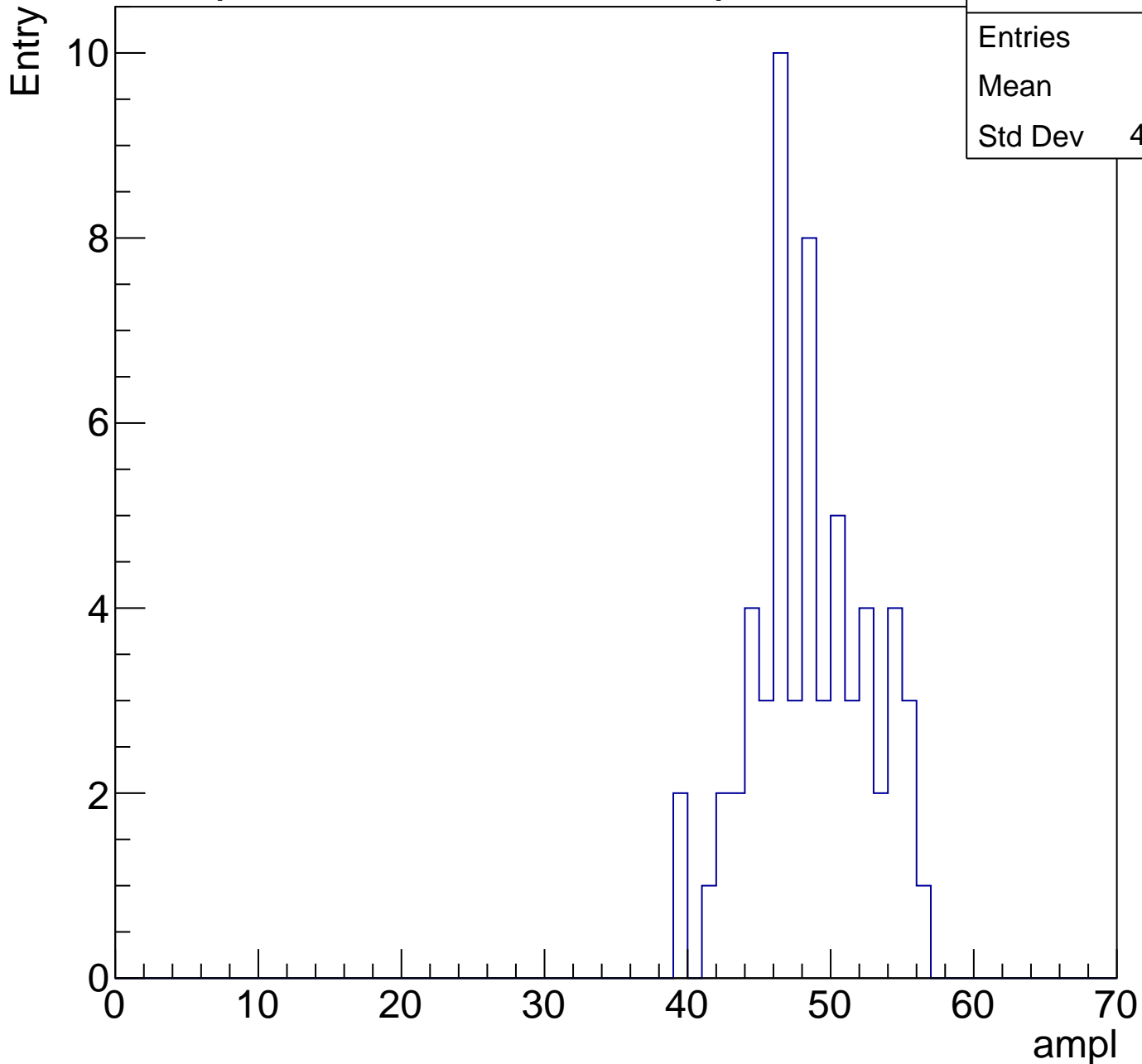
**Gaus Width: 5.0936**



# B1L103S, U26-ch120, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	60
Mean	48.1
Std Dev	4.053

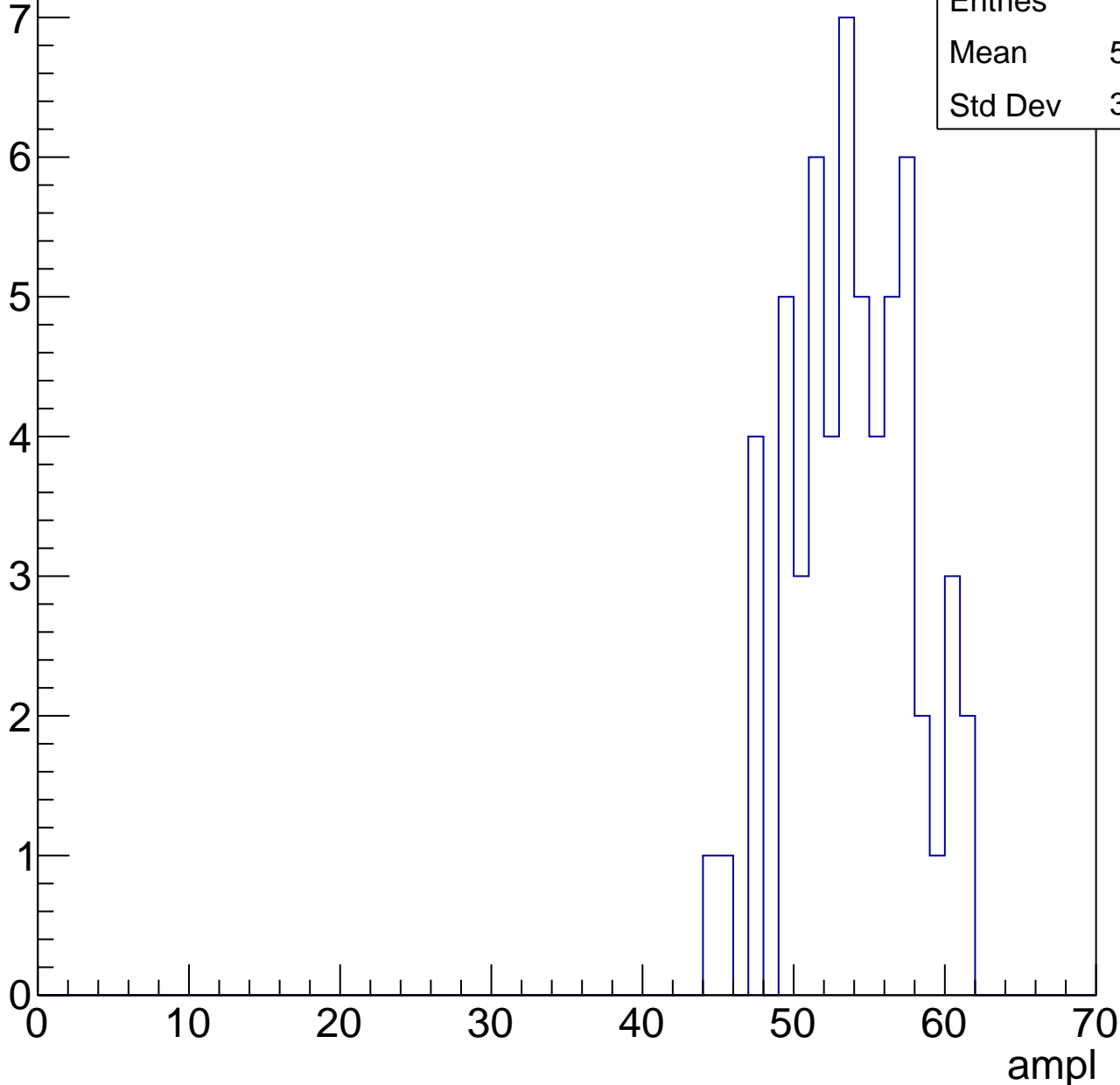


# B1L103S, U26-ch120, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

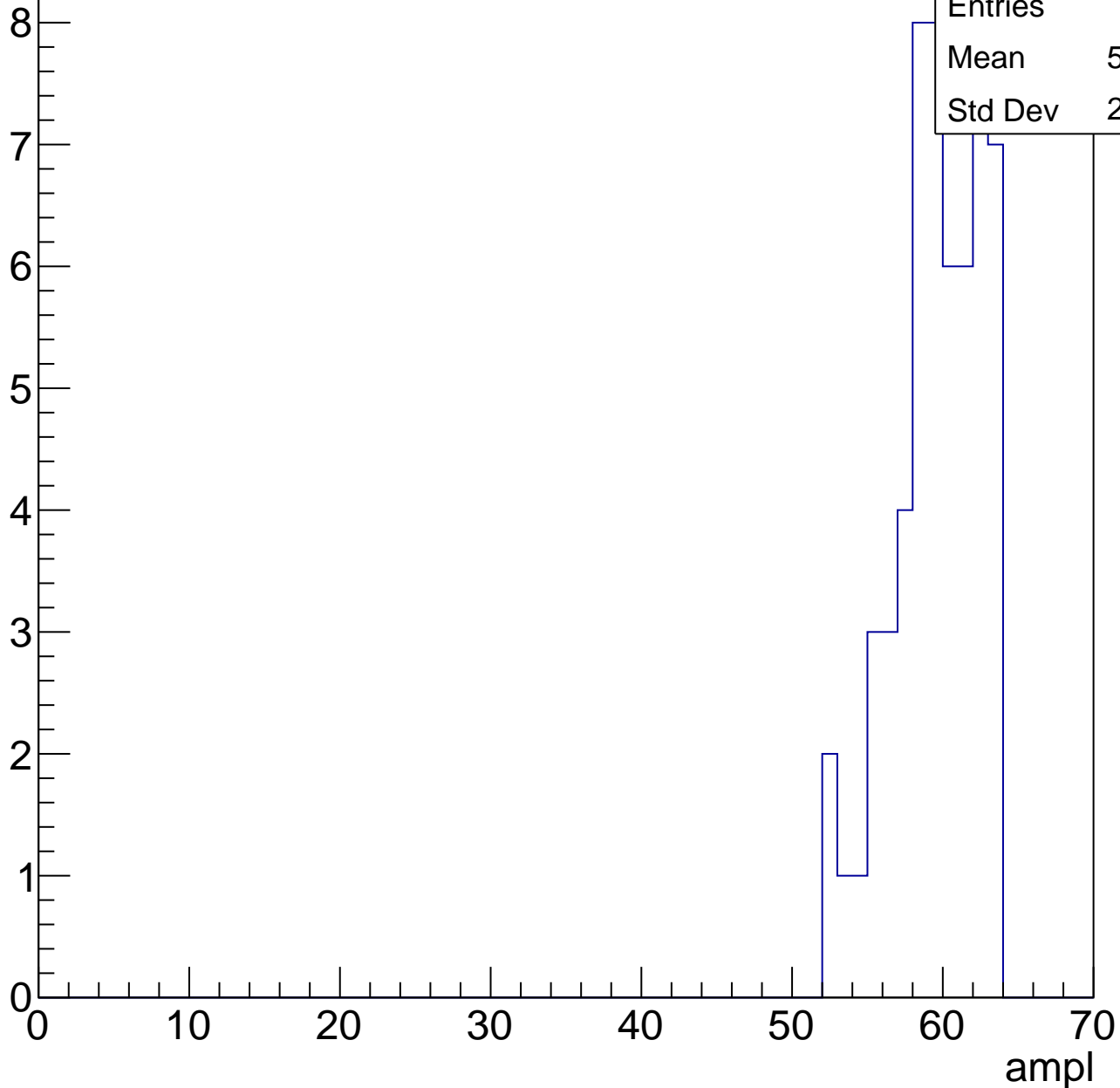
Entries	59
Mean	53.32
Std Dev	3.993



# B1L103S, U26-ch120, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

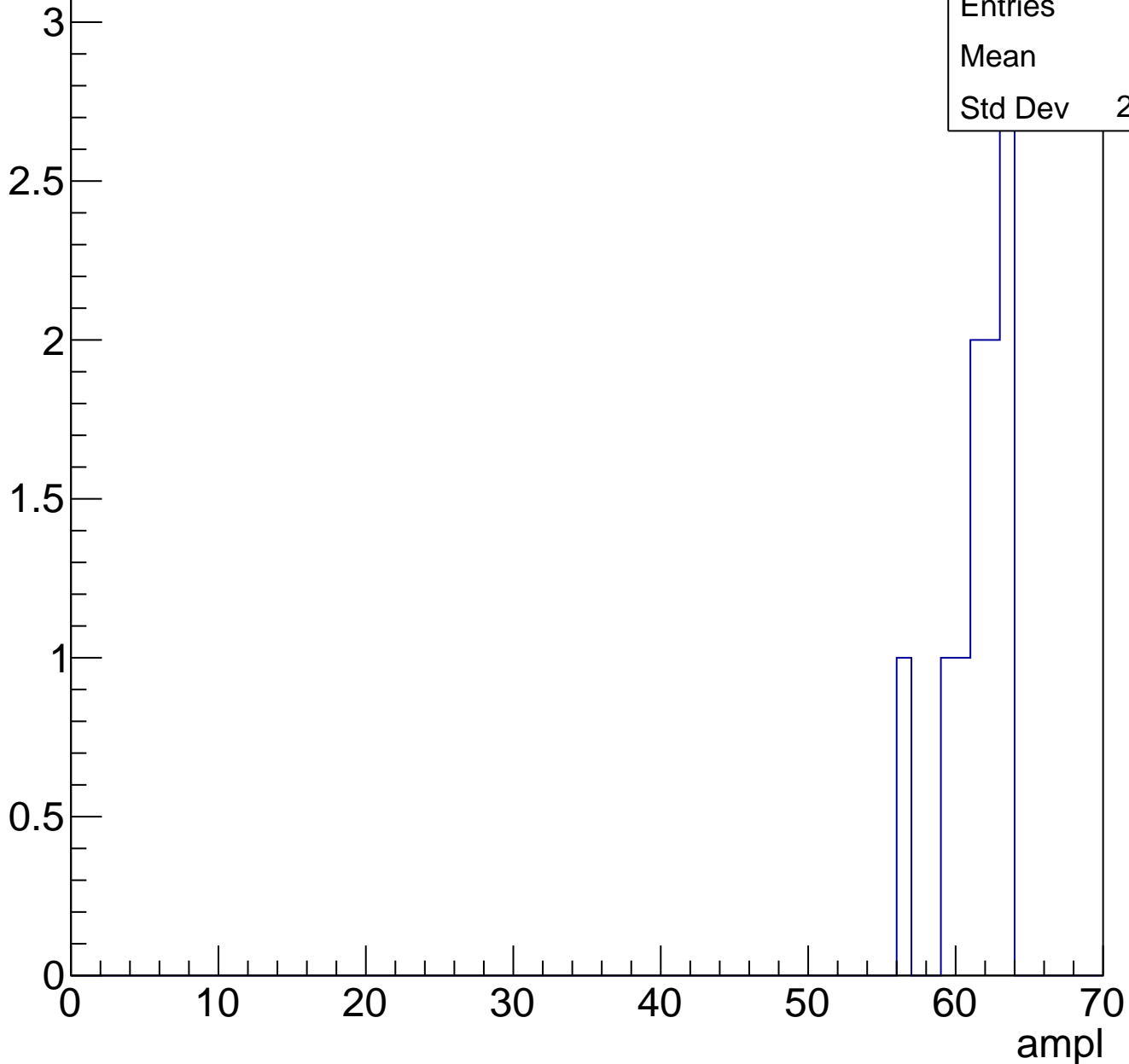
Entry



# B1L103S, U26-ch120, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry





# B1L103S, U26-ch120, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

20  
18  
16  
14  
12  
10  
8  
6  
4  
2  
0

Entries	20
Mean	0
Std Dev	0

ampl

# B1L103S, U26-ch121, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	75
Mean	24.2
Std Dev	10.57

**Gaus mean : 28.8161**

**Gaus Width: 4.1519**

Entry

10

8

6

4

2

0

0

10

20

30

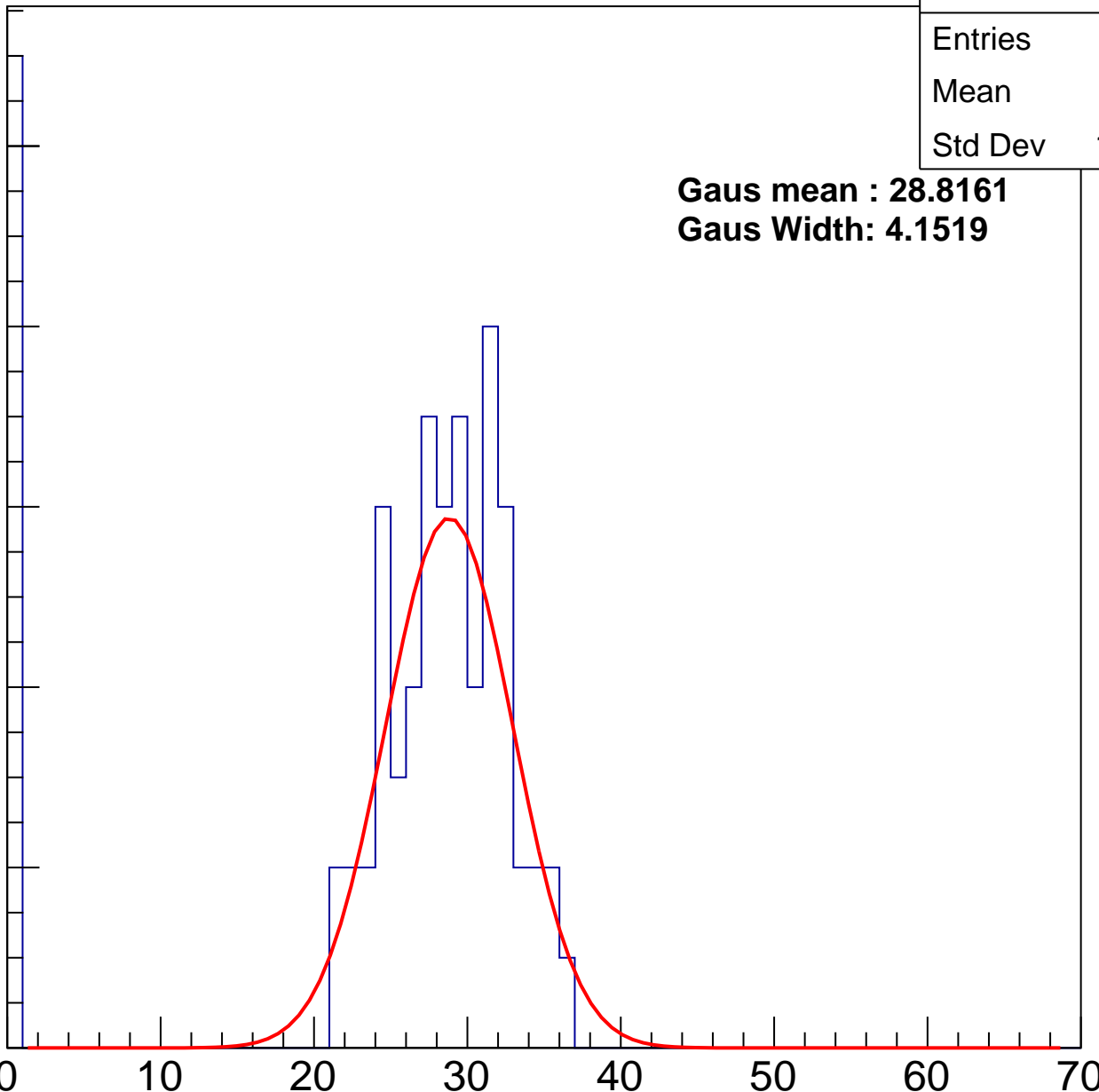
40

50

60

70

ampl



# B1L103S, U26-ch121, adc1

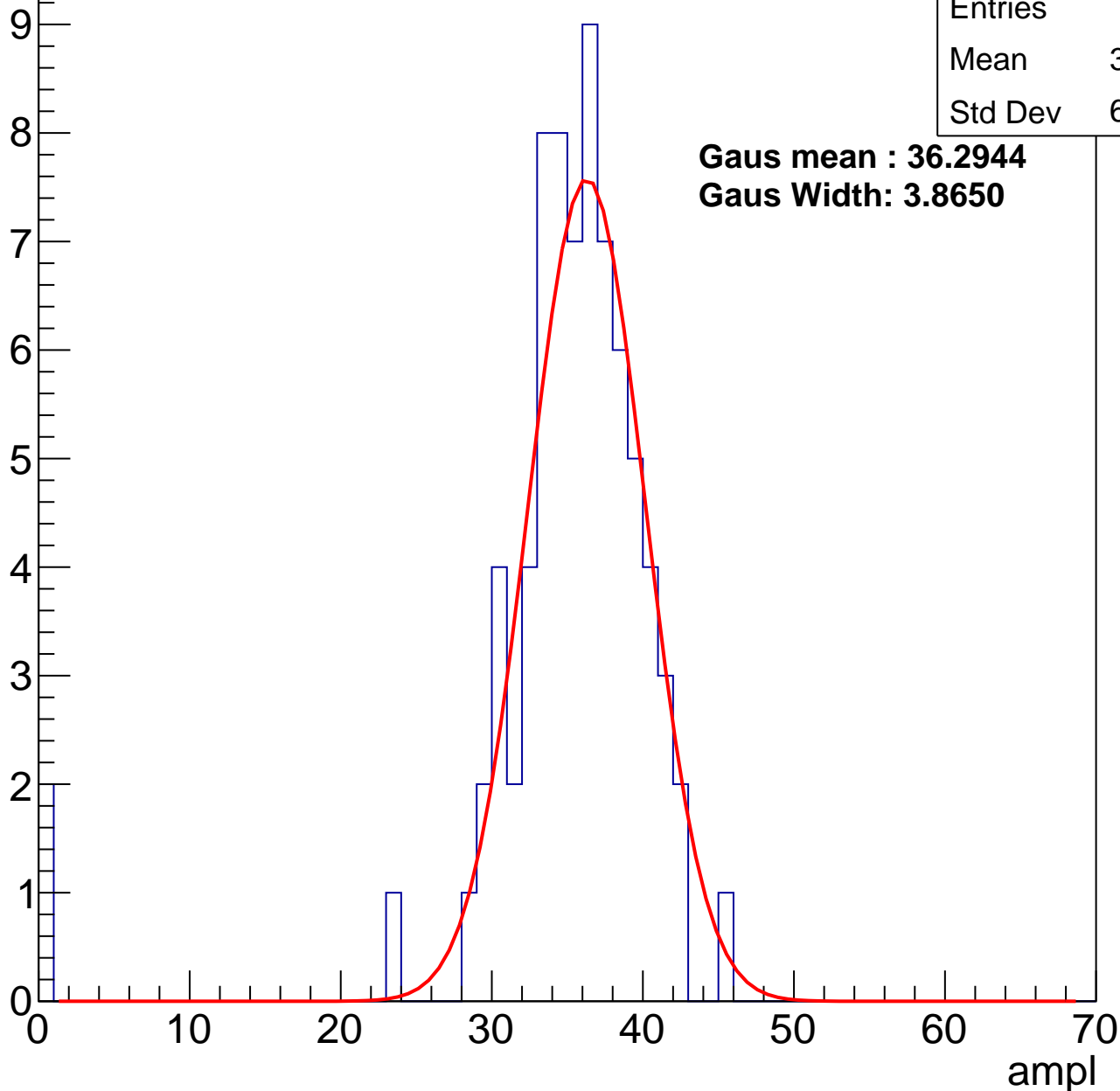
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	76
Mean	34.45
Std Dev	6.764

**Gaus mean : 36.2944**

**Gaus Width: 3.8650**



# B1L103S, U26-ch121, adc2

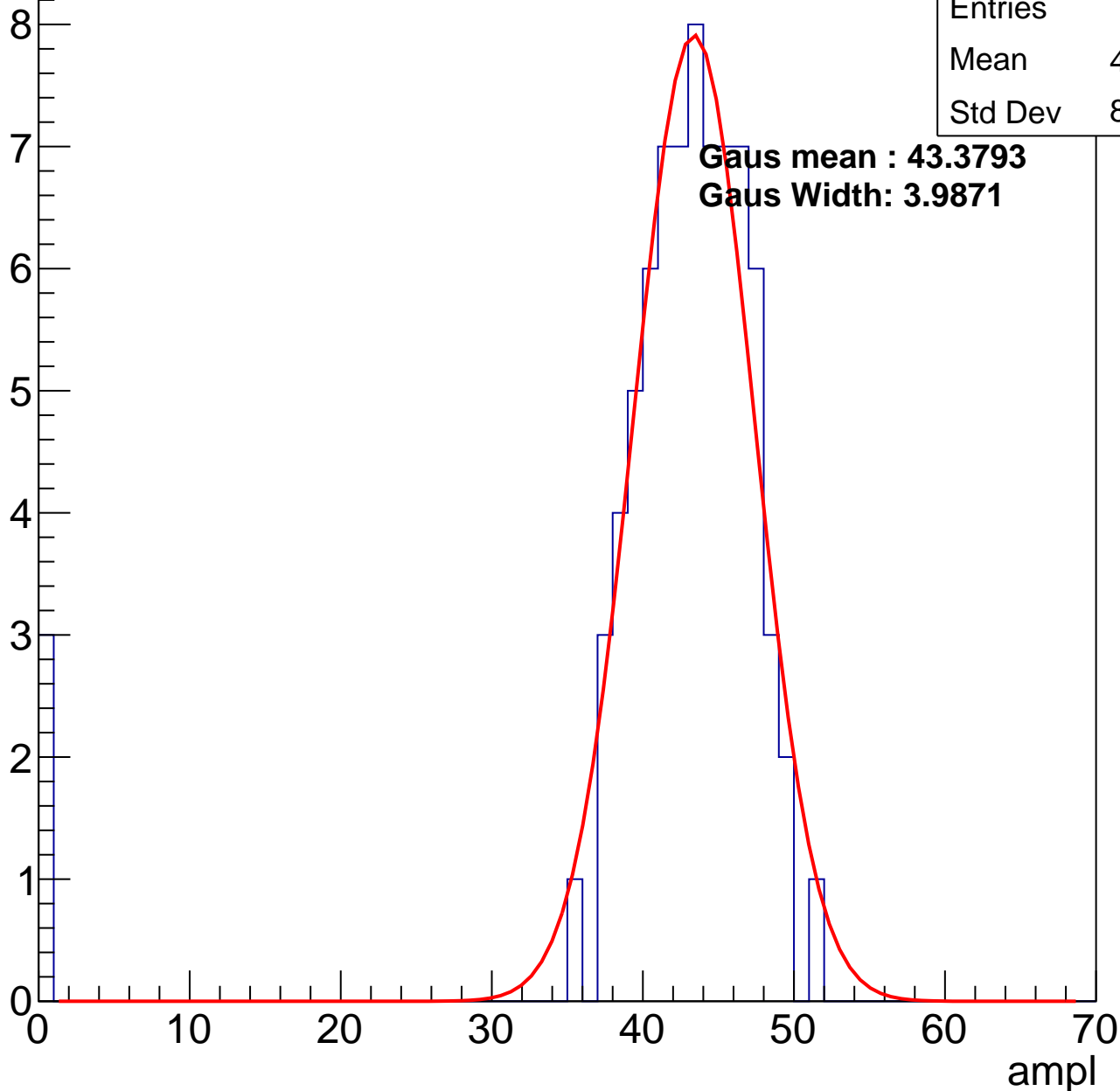
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	77
Mean	41.27
Std Dev	8.947

**Gaus mean : 43.3793**

**Gaus Width: 3.9871**

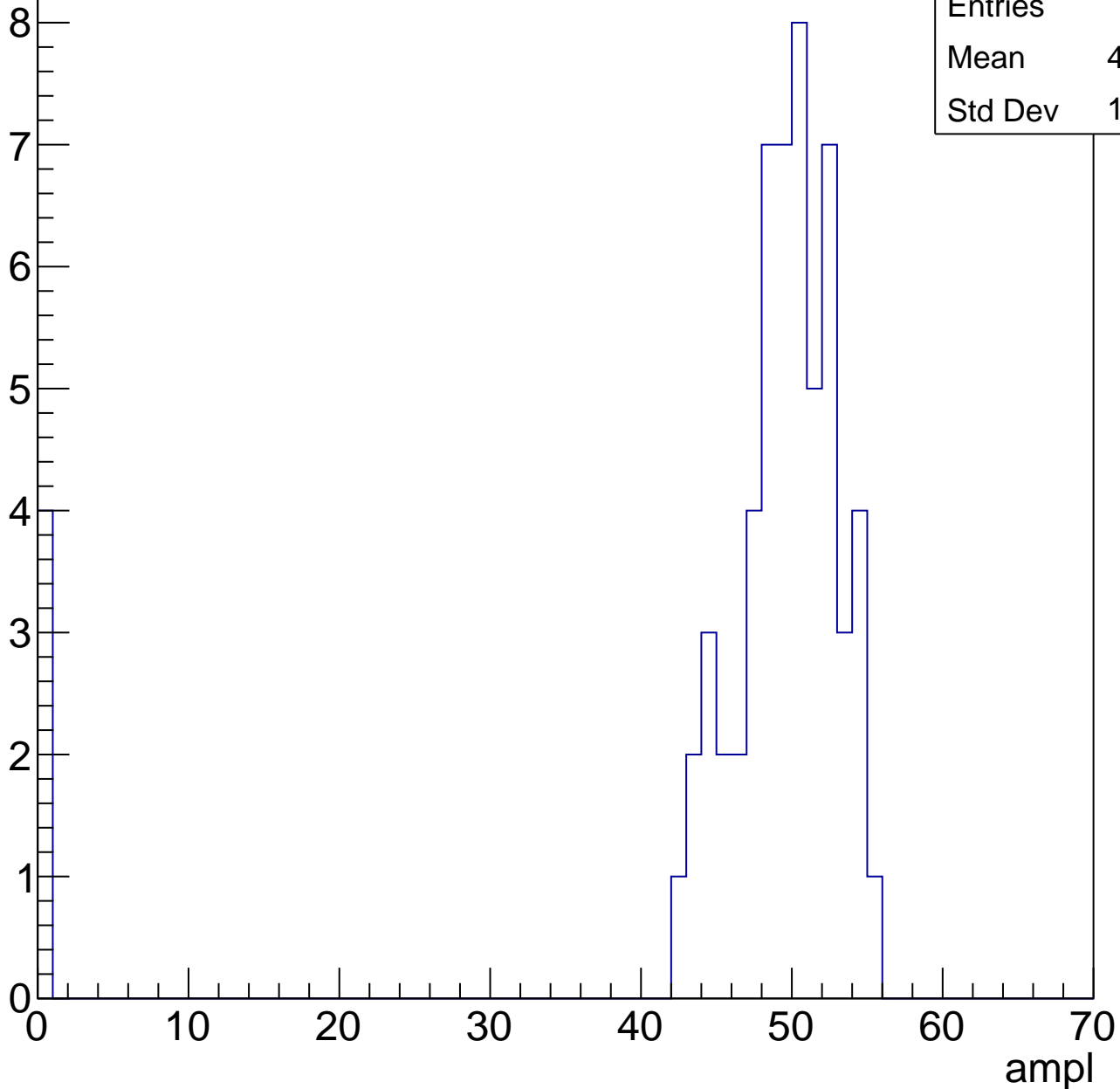


# B1L103S, U26-ch121, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

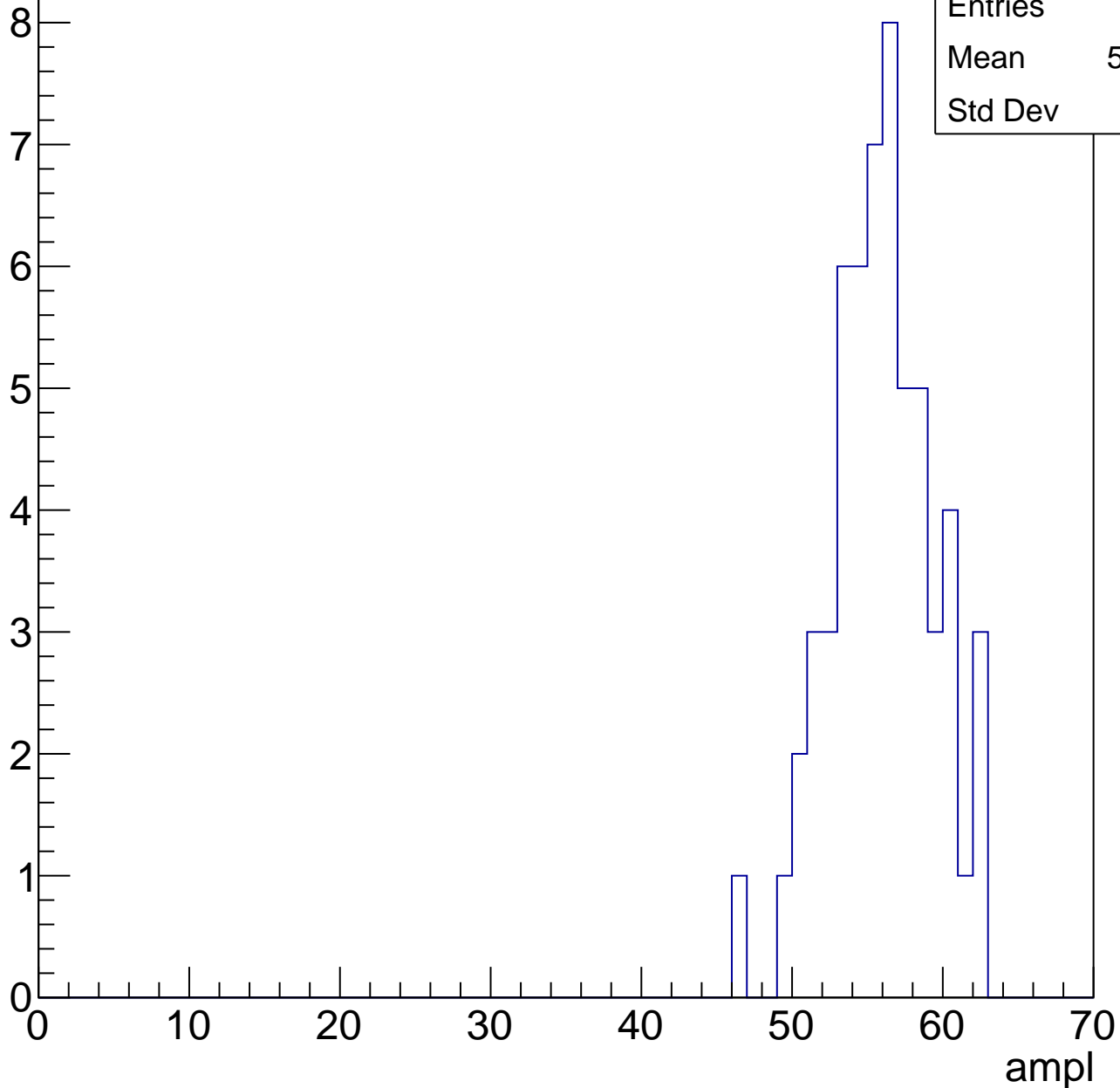
Entries	60
Mean	45.97
Std Dev	12.65



# B1L103S, U26-ch121, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



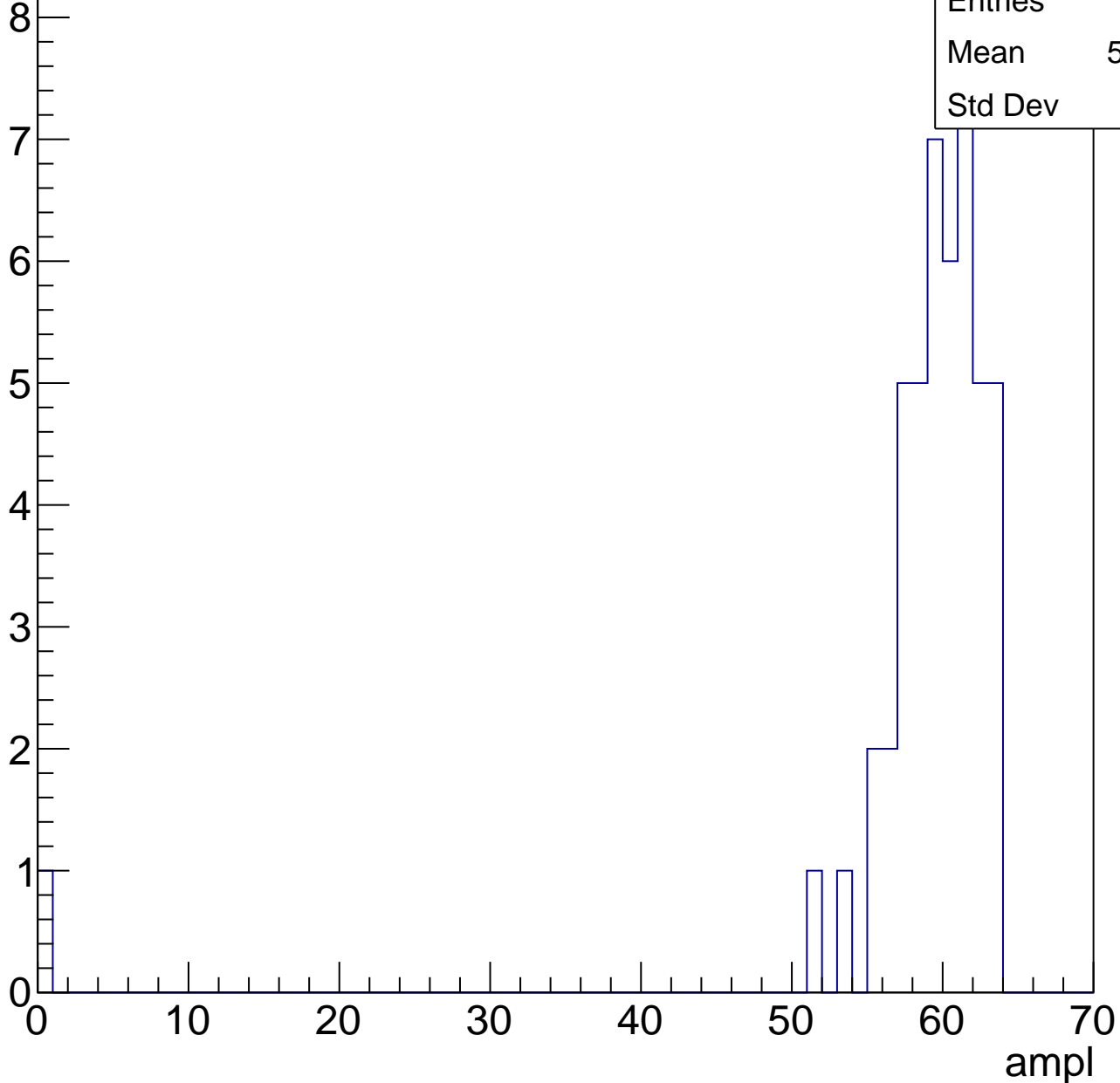
Entries	58
Mean	55.48
Std Dev	3.38

# B1L103S, U26-ch121, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	48
Mean	58.06
Std Dev	8.87

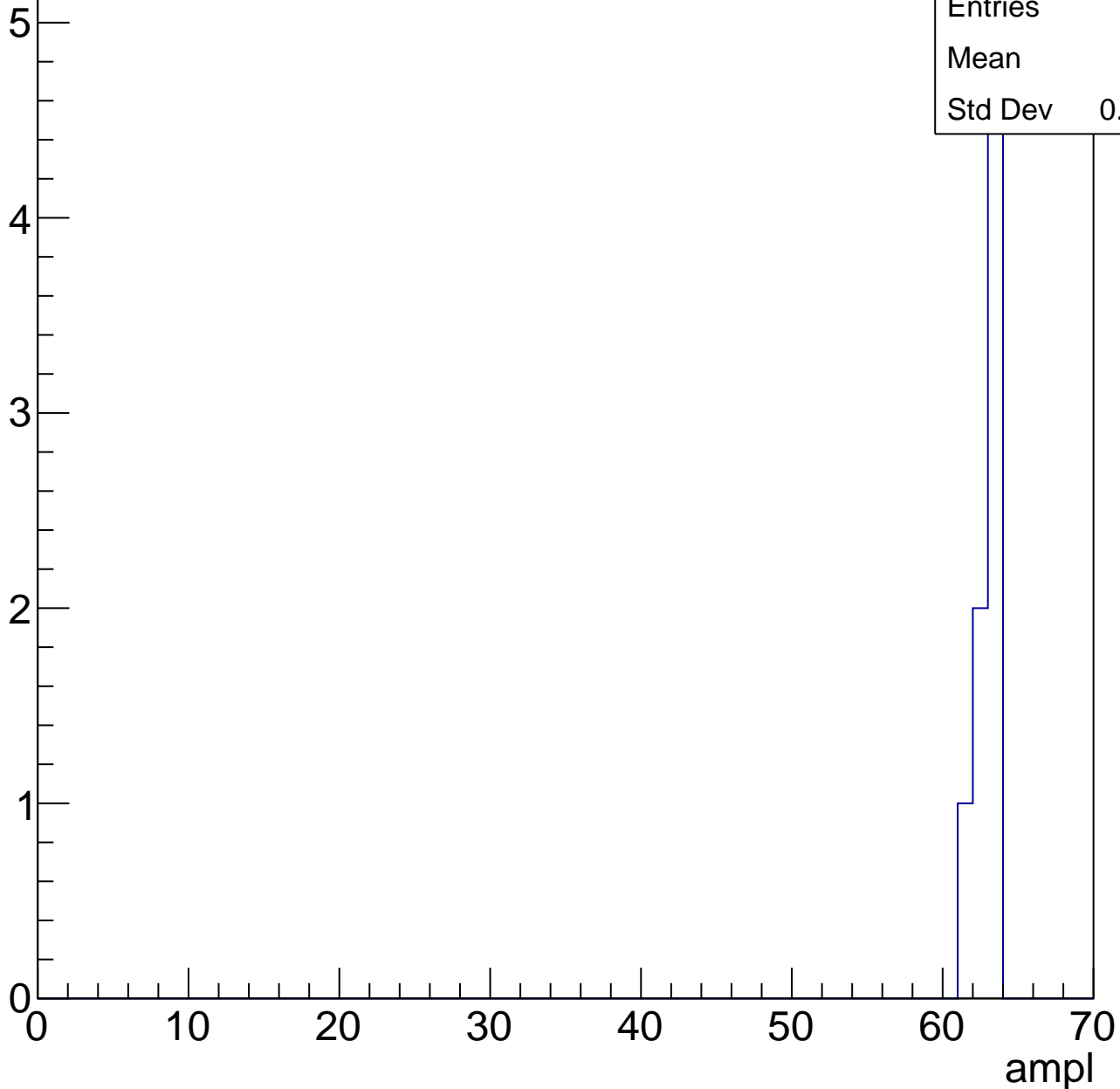


# B1L103S, U26-ch121, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	8
Mean	62.5
Std Dev	0.7071





# B1L103S, U26-ch121, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



# B1L103S, U26-ch122, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	78
Mean	24.64
Std Dev	11.64

**Gaus mean : 29.7324**

**Gaus Width: 4.3178**

Entry

12

10

8

6

4

2

0

0

10

20

30

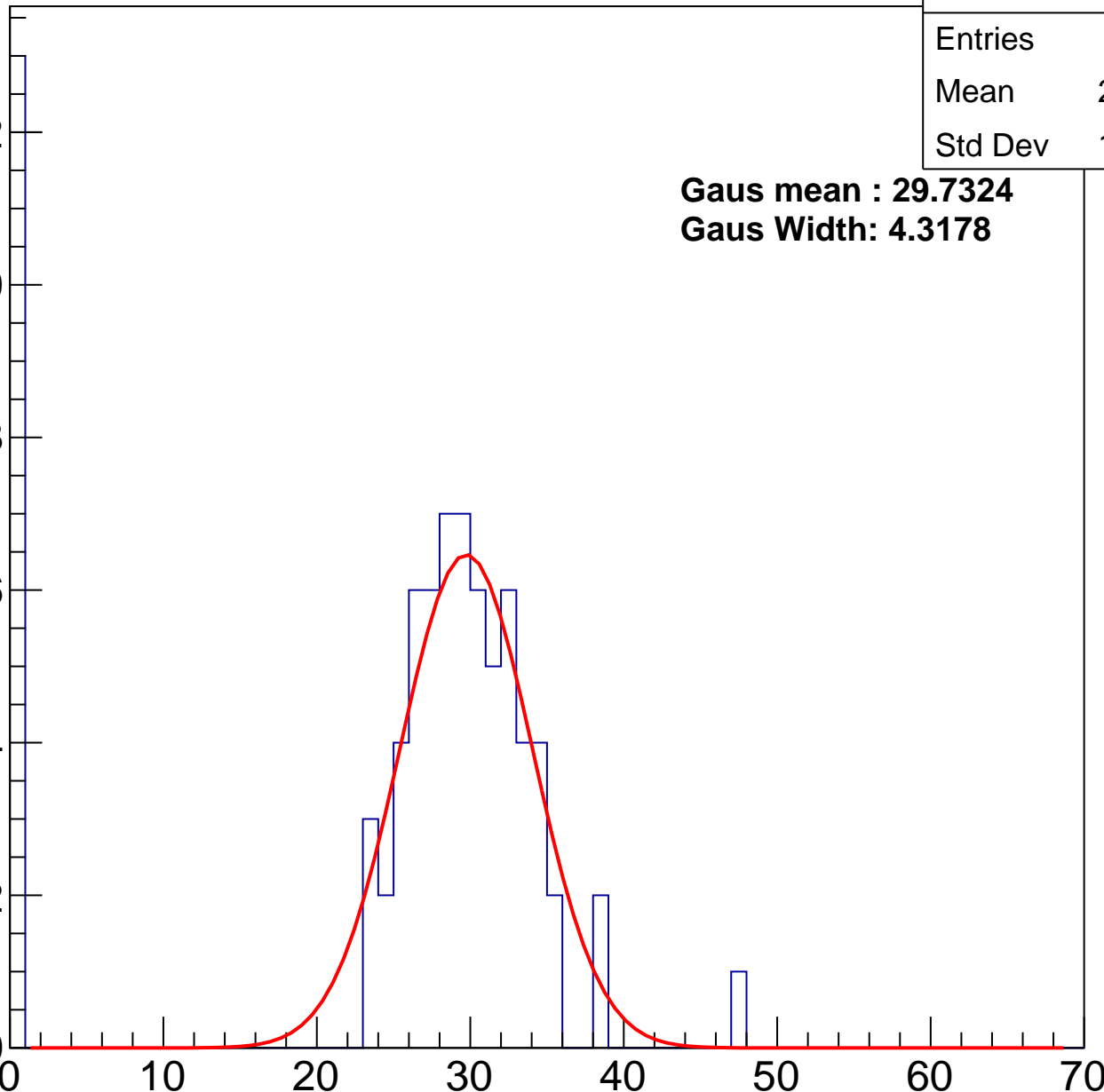
40

50

60

70

ampl



# B1L103S, U26-ch122, adc1

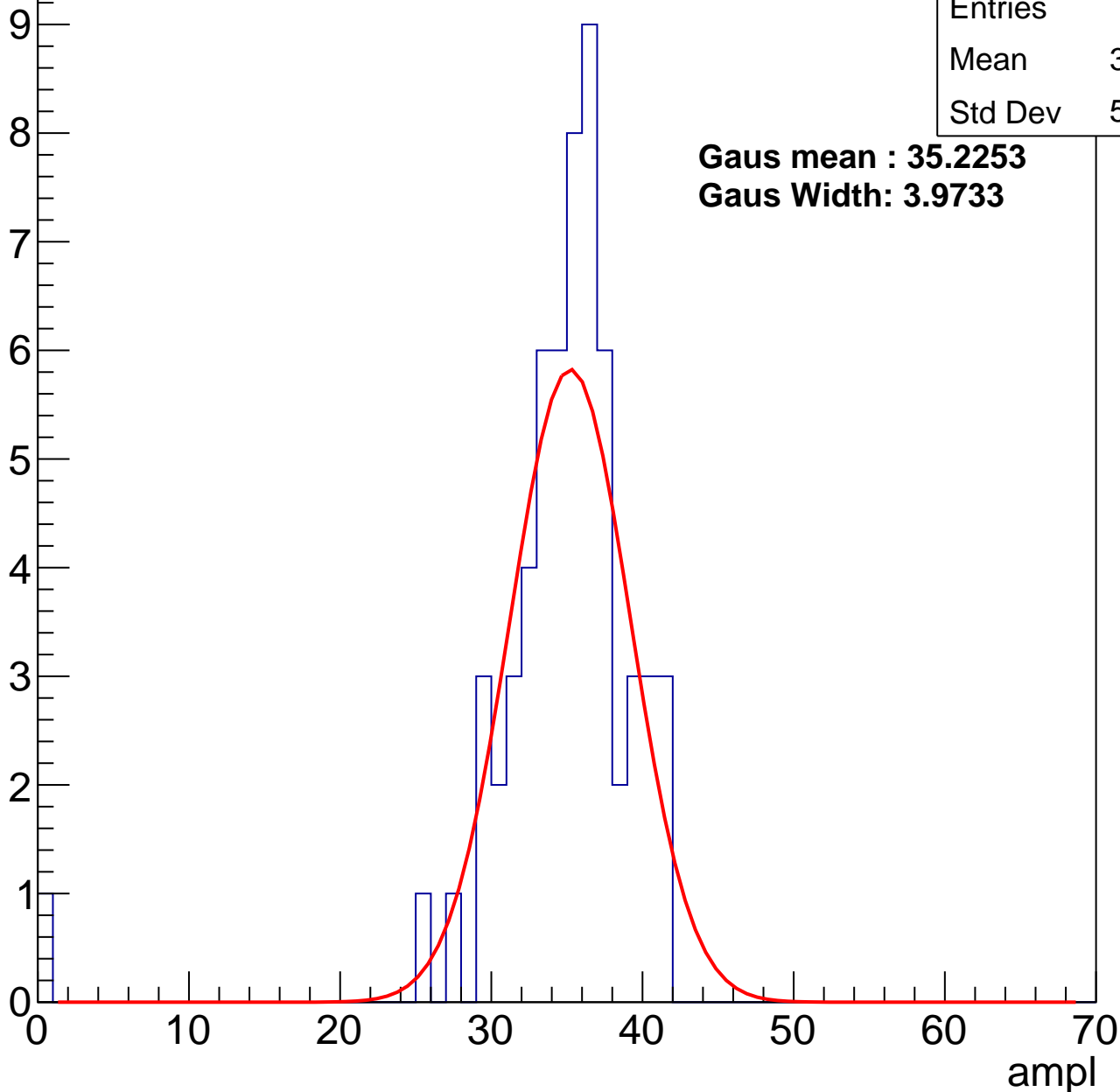
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	61
Mean	34.16
Std Dev	5.582

**Gaus mean : 35.2253**

**Gaus Width: 3.9733**



# B1L103S, U26-ch122, adc2

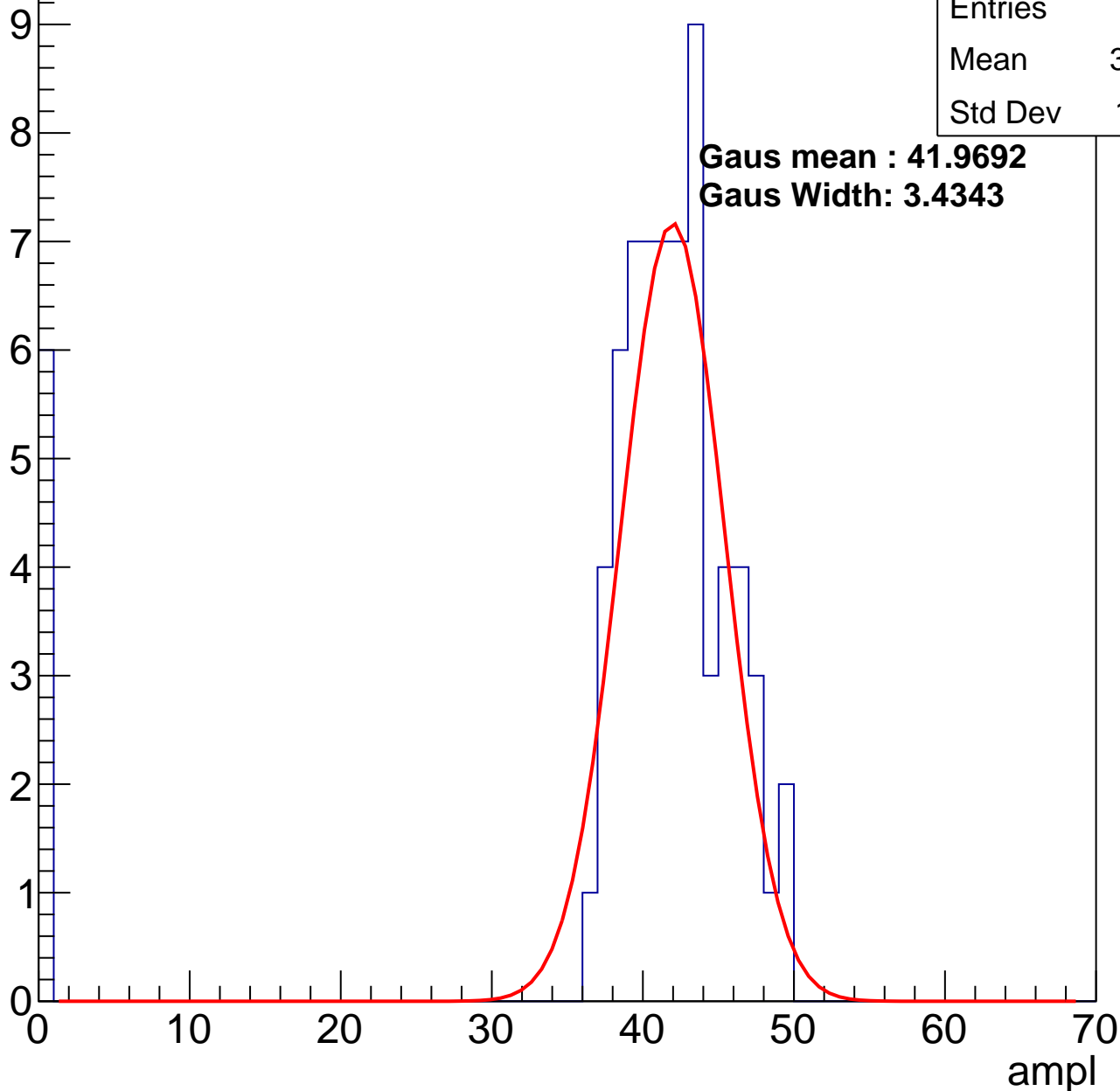
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	71
Mean	38.25
Std Dev	12.01

**Gaus mean : 41.9692**

**Gaus Width: 3.4343**

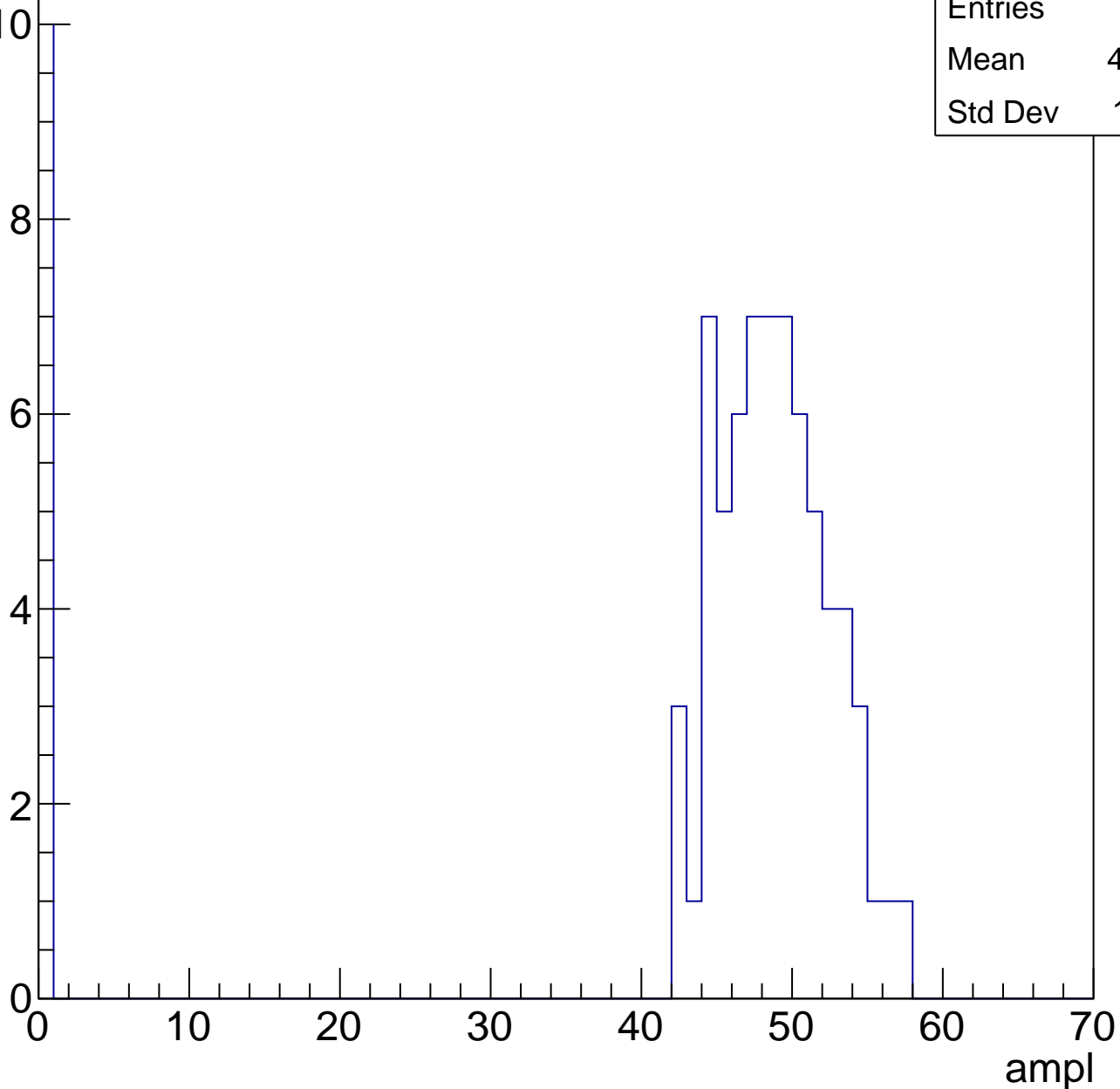


# B1L103S, U26-ch122, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	78
Mean	42.19
Std Dev	16.51

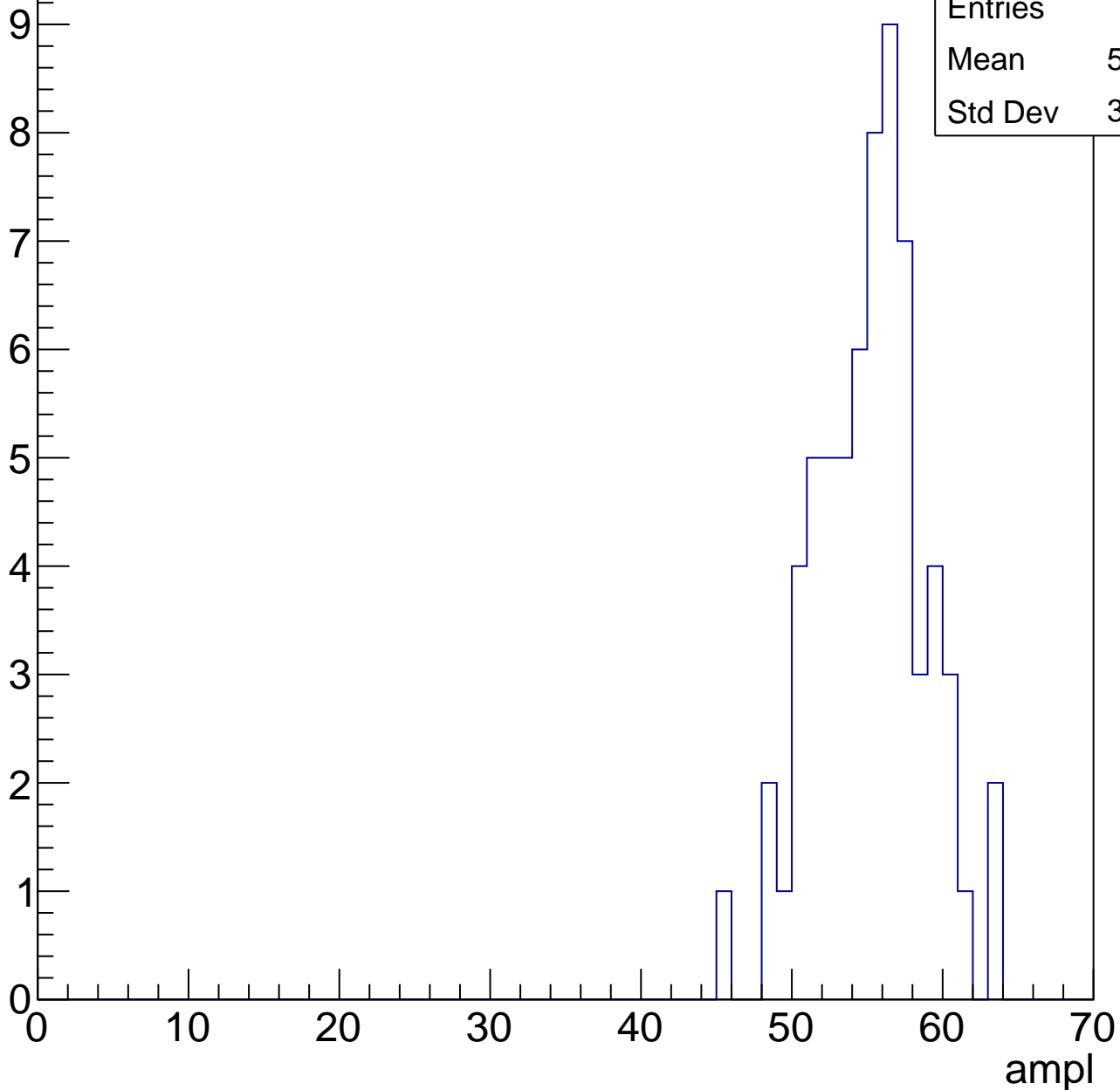


# B1L103S, U26-ch122, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	66
Mean	54.76
Std Dev	3.585



# B1L103S, U26-ch122, adc5

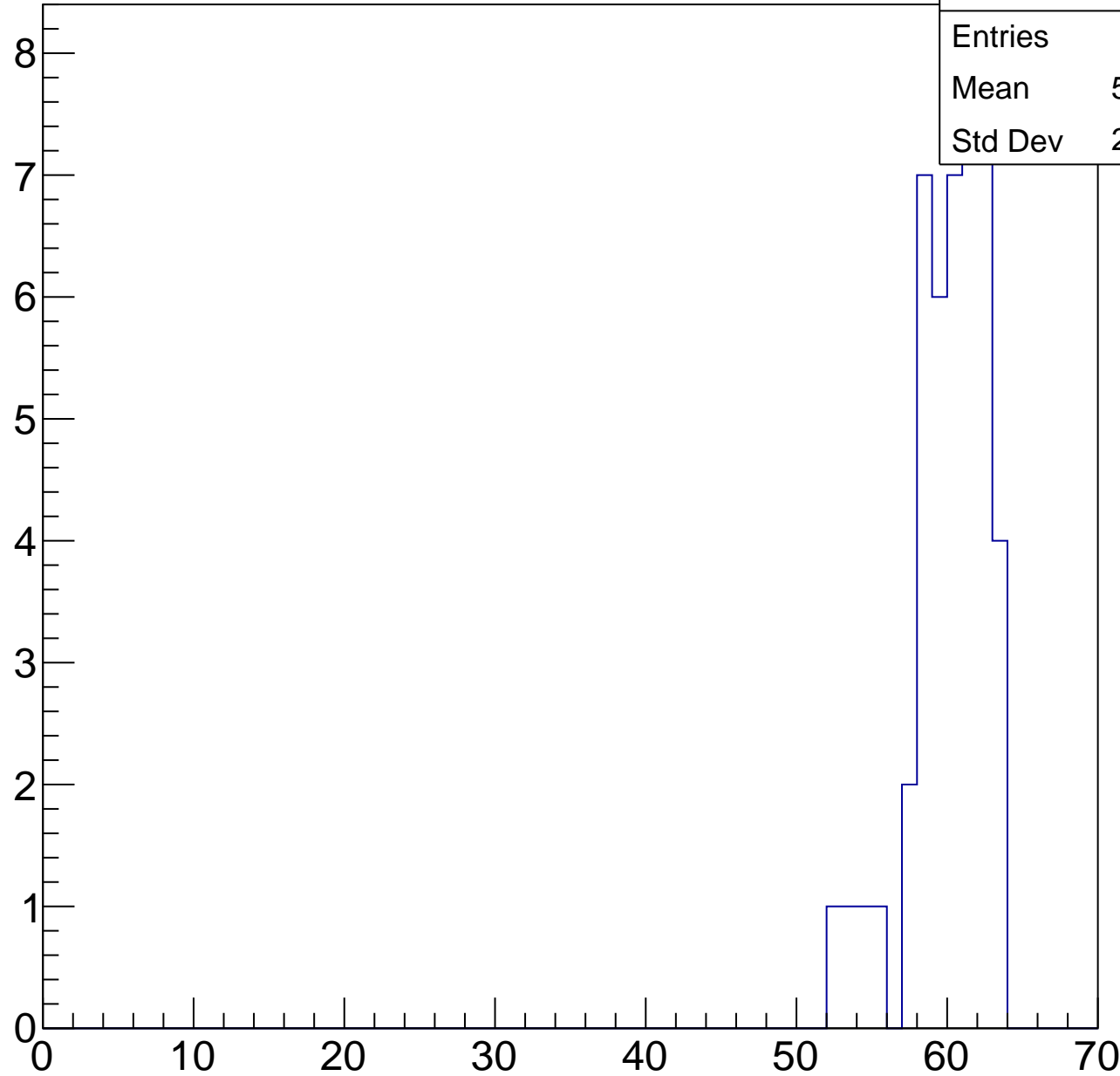
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	46
Mean	59.65
Std Dev	2.539

ampl



# B1L103S, U26-ch122, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	5
Mean	49.6
Std Dev	24.81

ampl

0 10 20 30 40 50 60 70

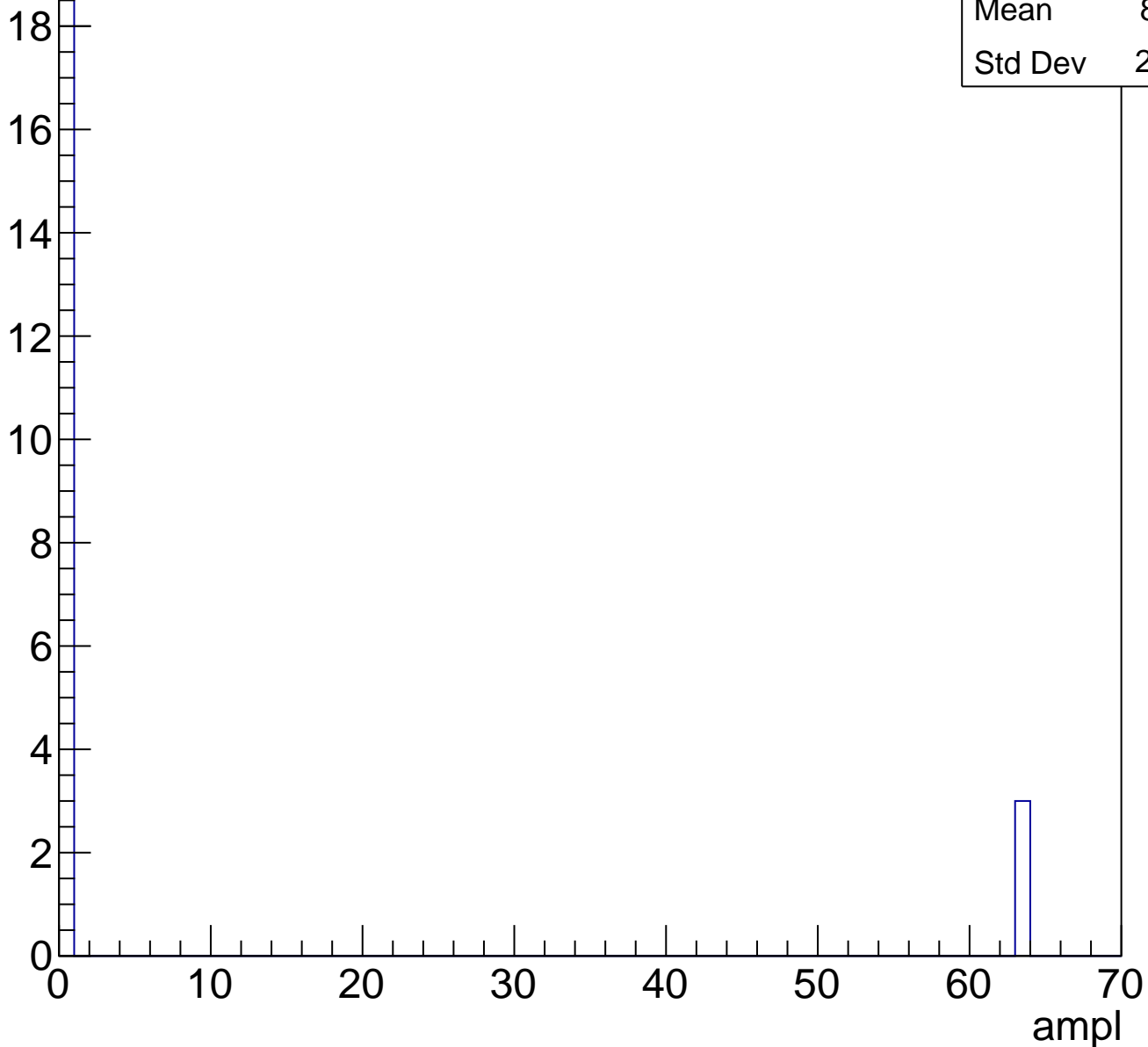


# B1L103S, U26-ch122, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	22
Mean	8.591
Std Dev	21.62

Entry



# B1L103S, U26-ch123, adc0

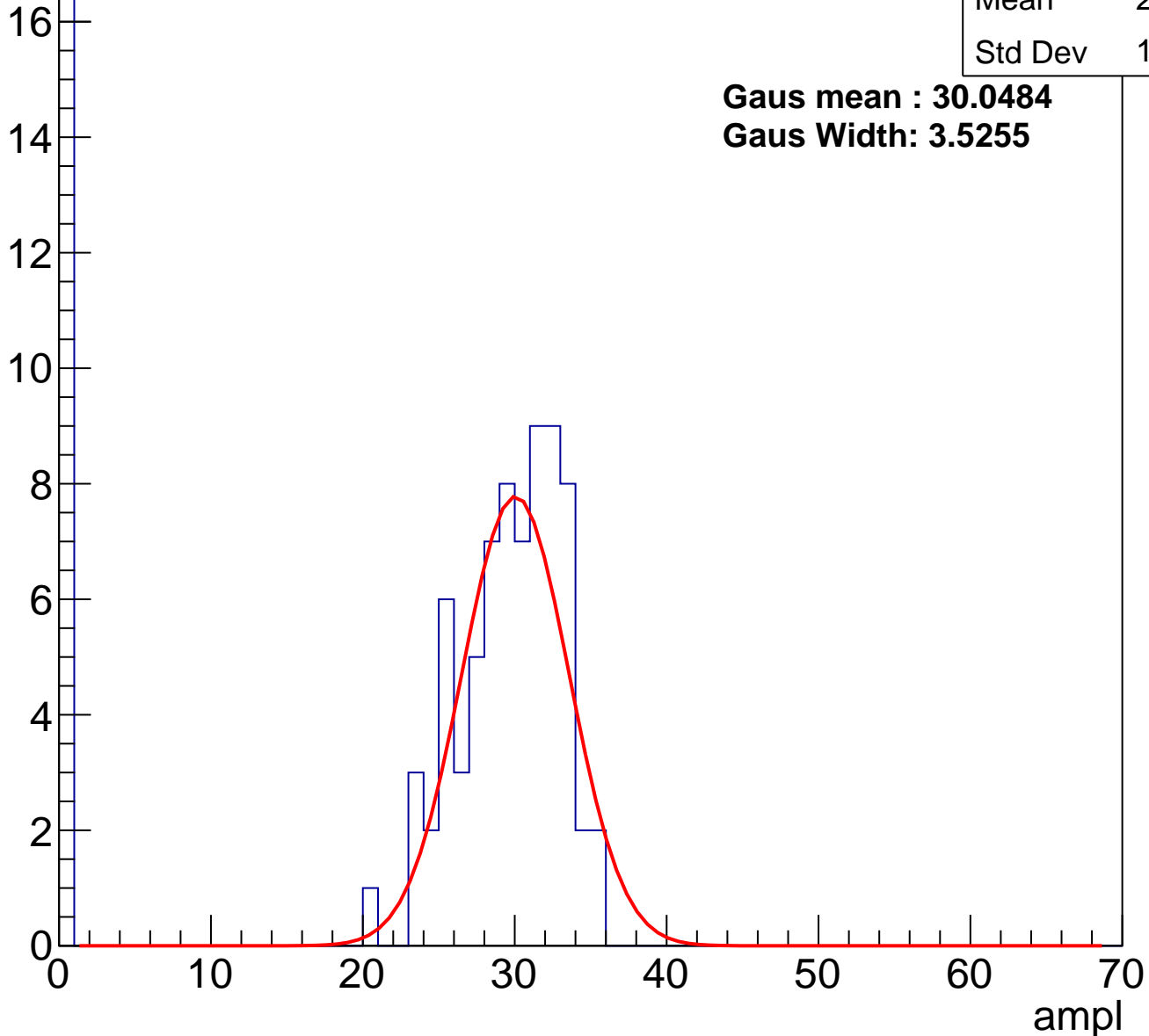
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	89
Mean	23.67
Std Dev	11.87

**Gaus mean : 30.0484**

**Gaus Width: 3.5255**

Entry



# B1L103S, U26-ch123, adc1

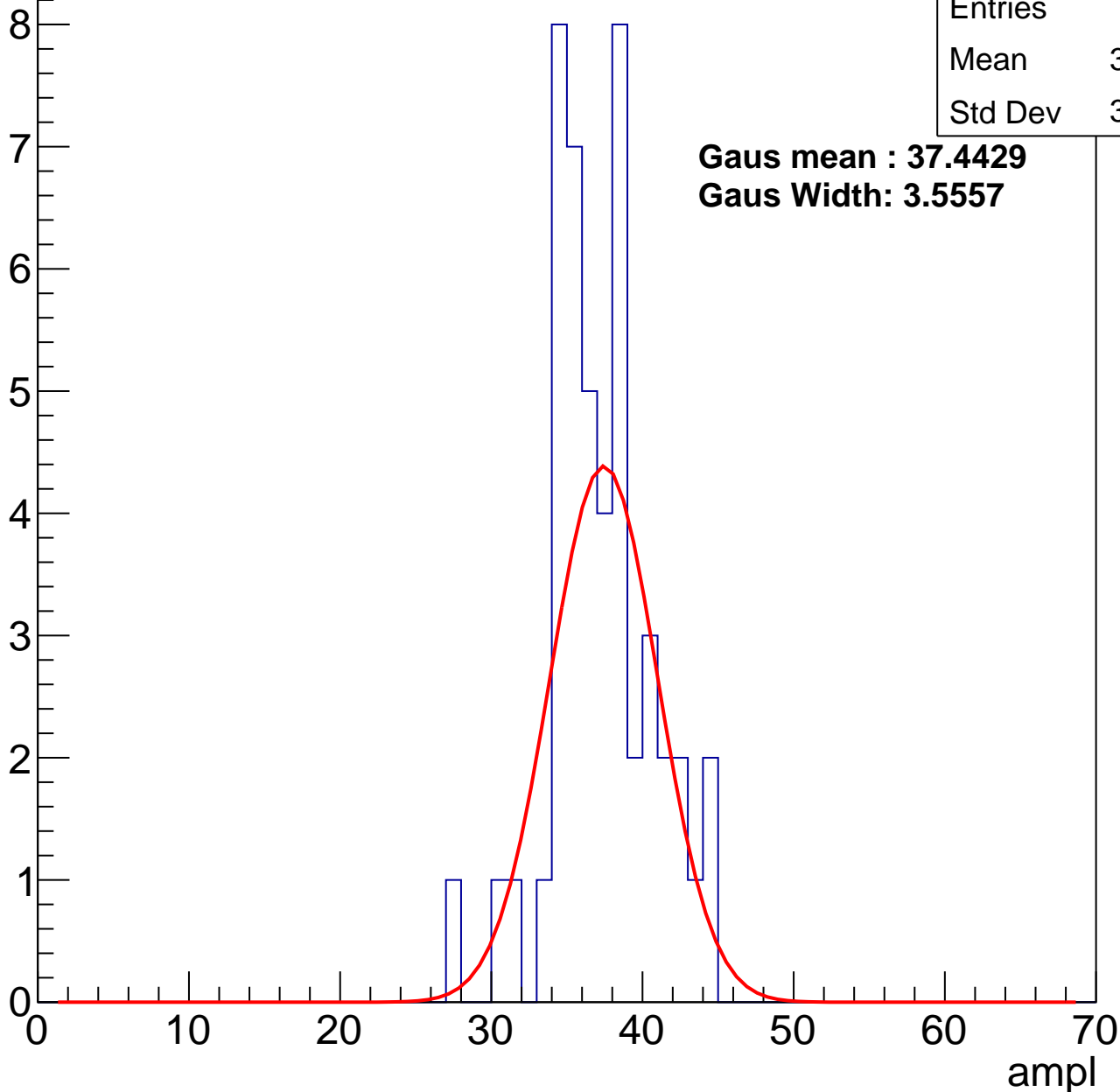
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	48
Mean	36.77
Std Dev	3.423

**Gaus mean : 37.4429**

**Gaus Width: 3.5557**



# B1L103S, U26-ch123, adc2

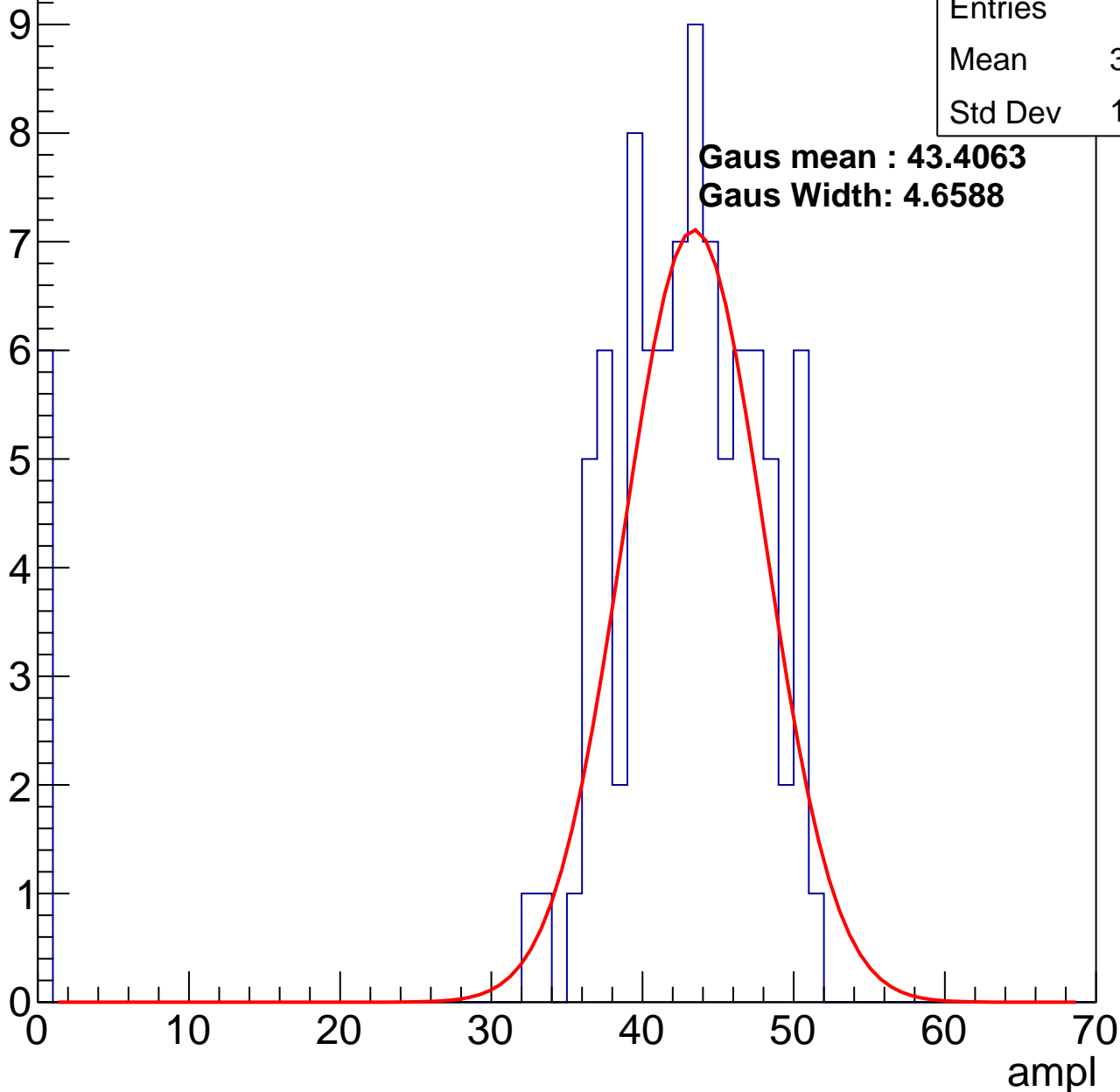
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	96
Mean	39.97
Std Dev	11.16

**Gaus mean : 43.4063**

**Gaus Width: 4.6588**



# B1L103S, U26-ch123, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	83
Mean	43.43
Std Dev	17.38

Entry

10

8

6

4

2

0

0

10

20

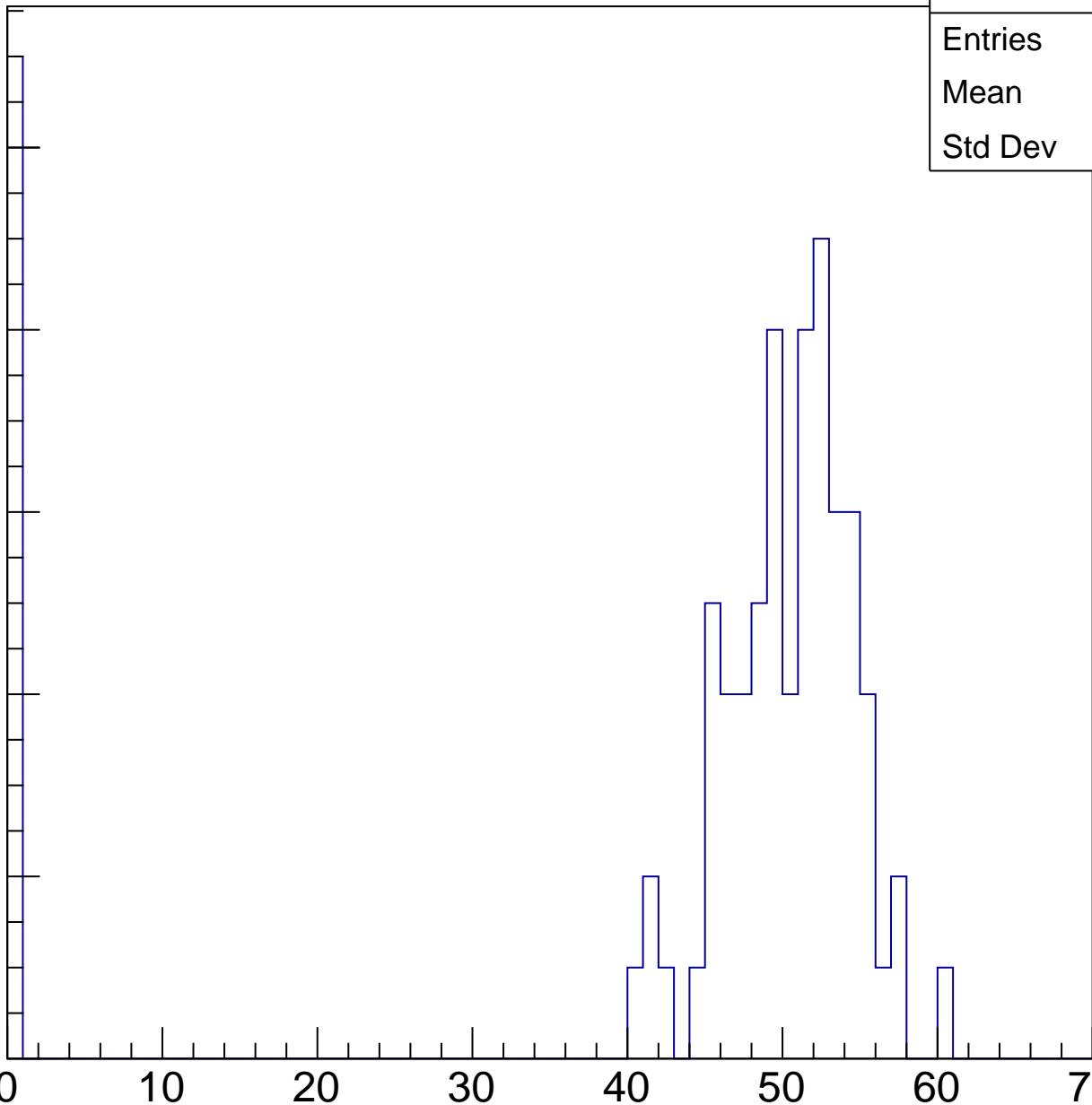
30

40

50

60

ampl

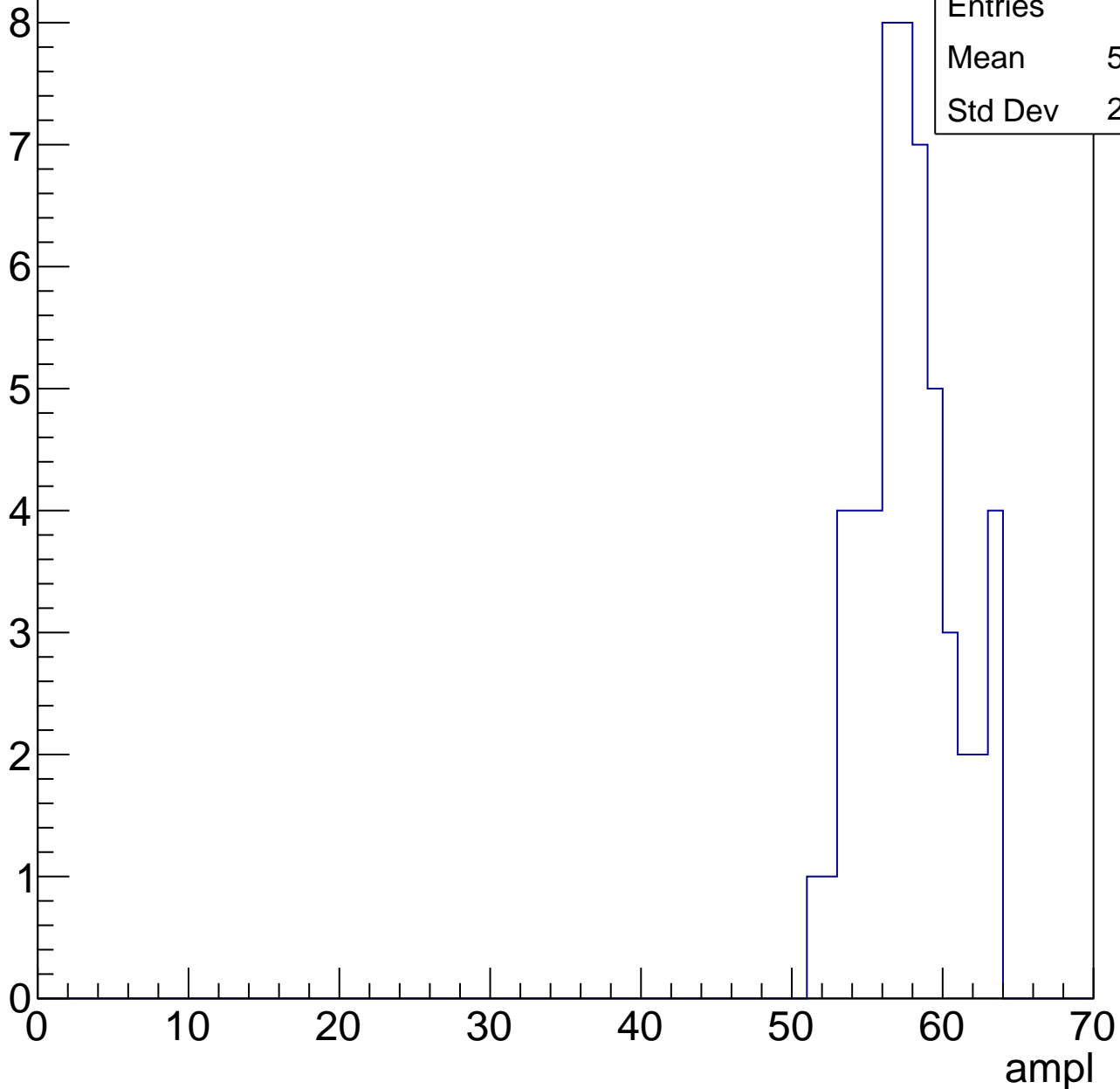


# B1L103S, U26-ch123, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	53
Mean	57.25
Std Dev	2.952

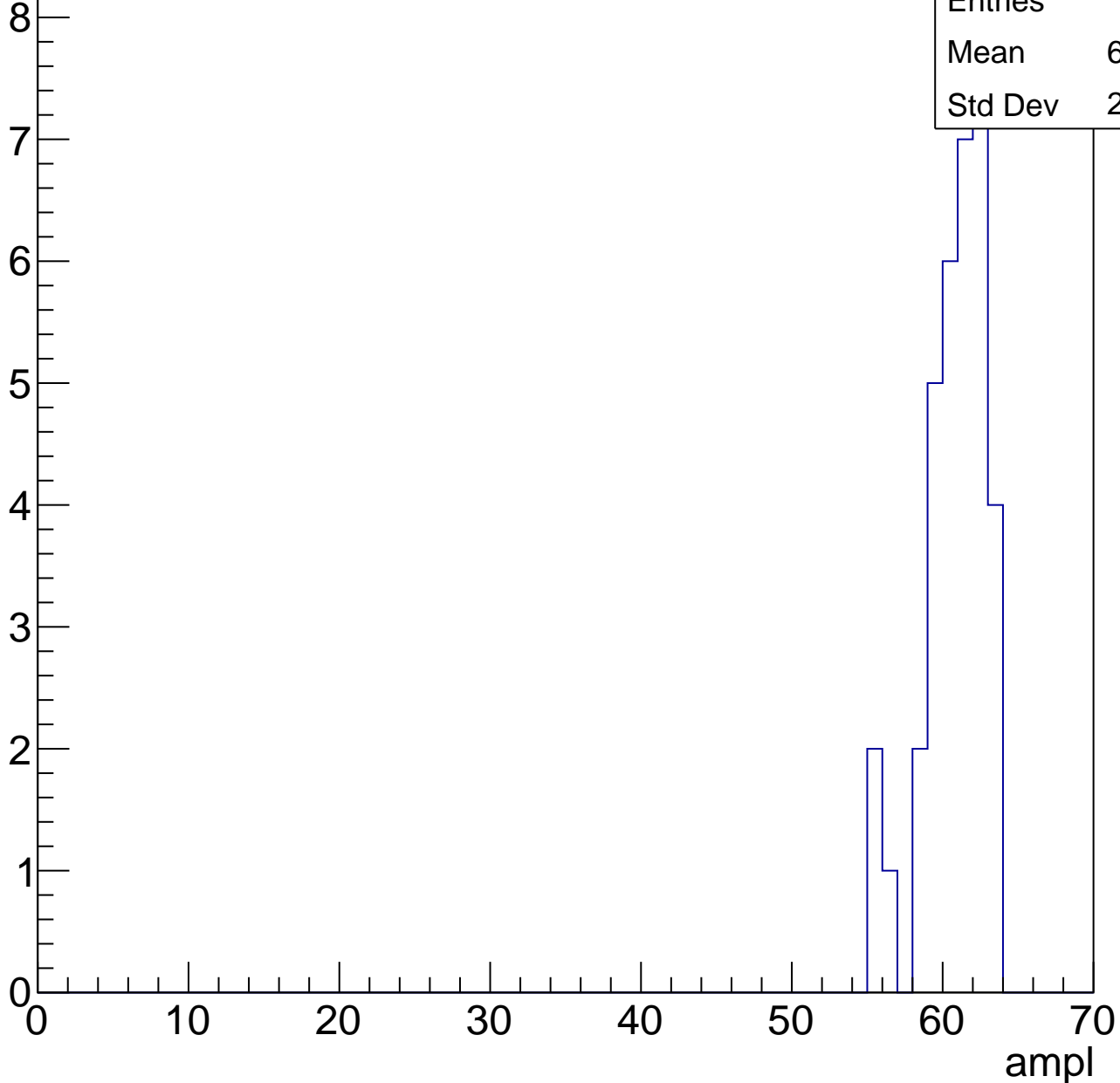


# B1L103S, U26-ch123, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

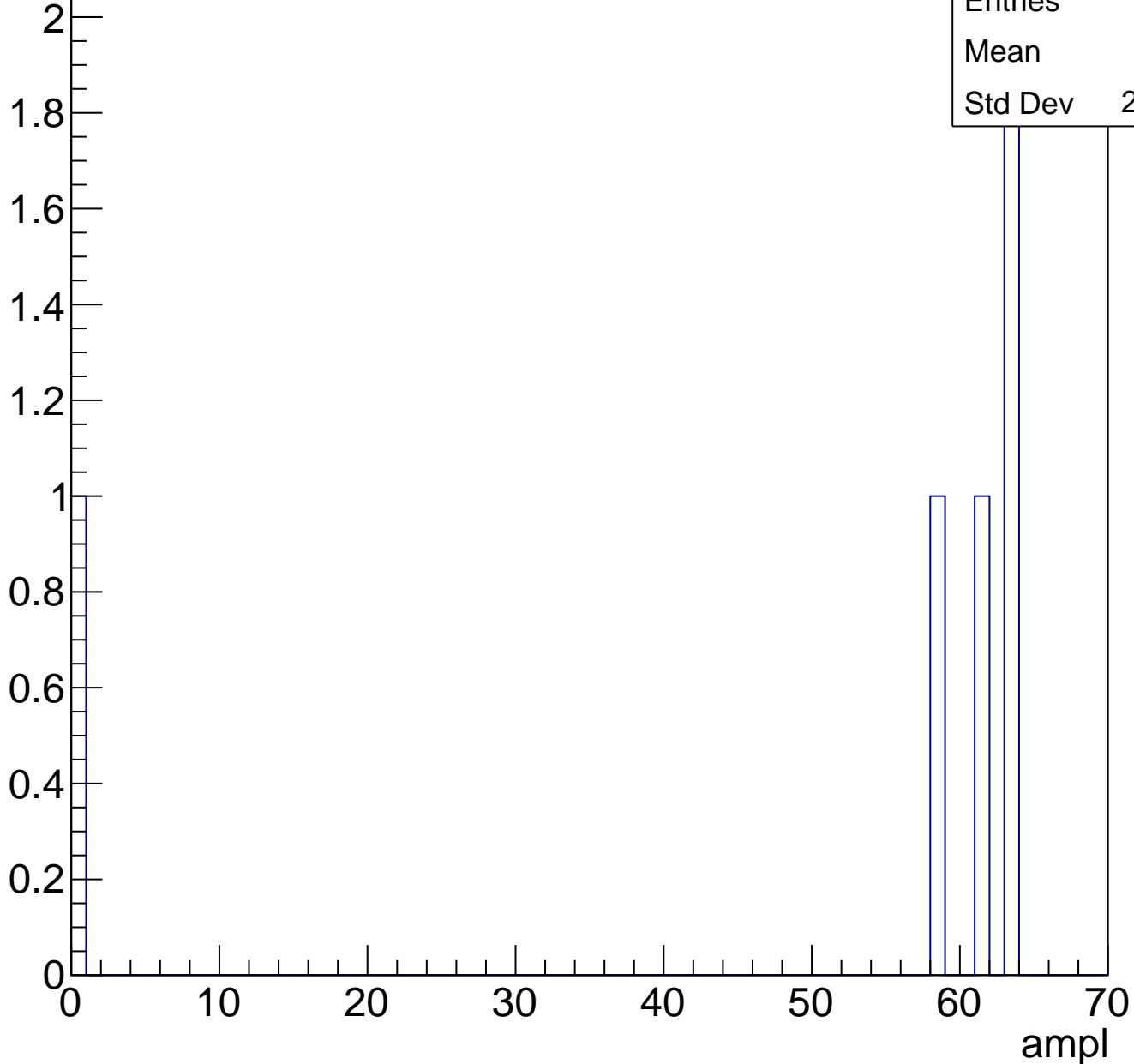
Entries	35
Mean	60.34
Std Dev	2.069



# B1L103S, U26-ch123, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry





# B1L103S, U26-ch123, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

18  
16  
14  
12  
10  
8  
6  
4  
2  
0

Entries	19
Mean	0
Std Dev	0

ampl

# B1L103S, U26-ch124, adc0

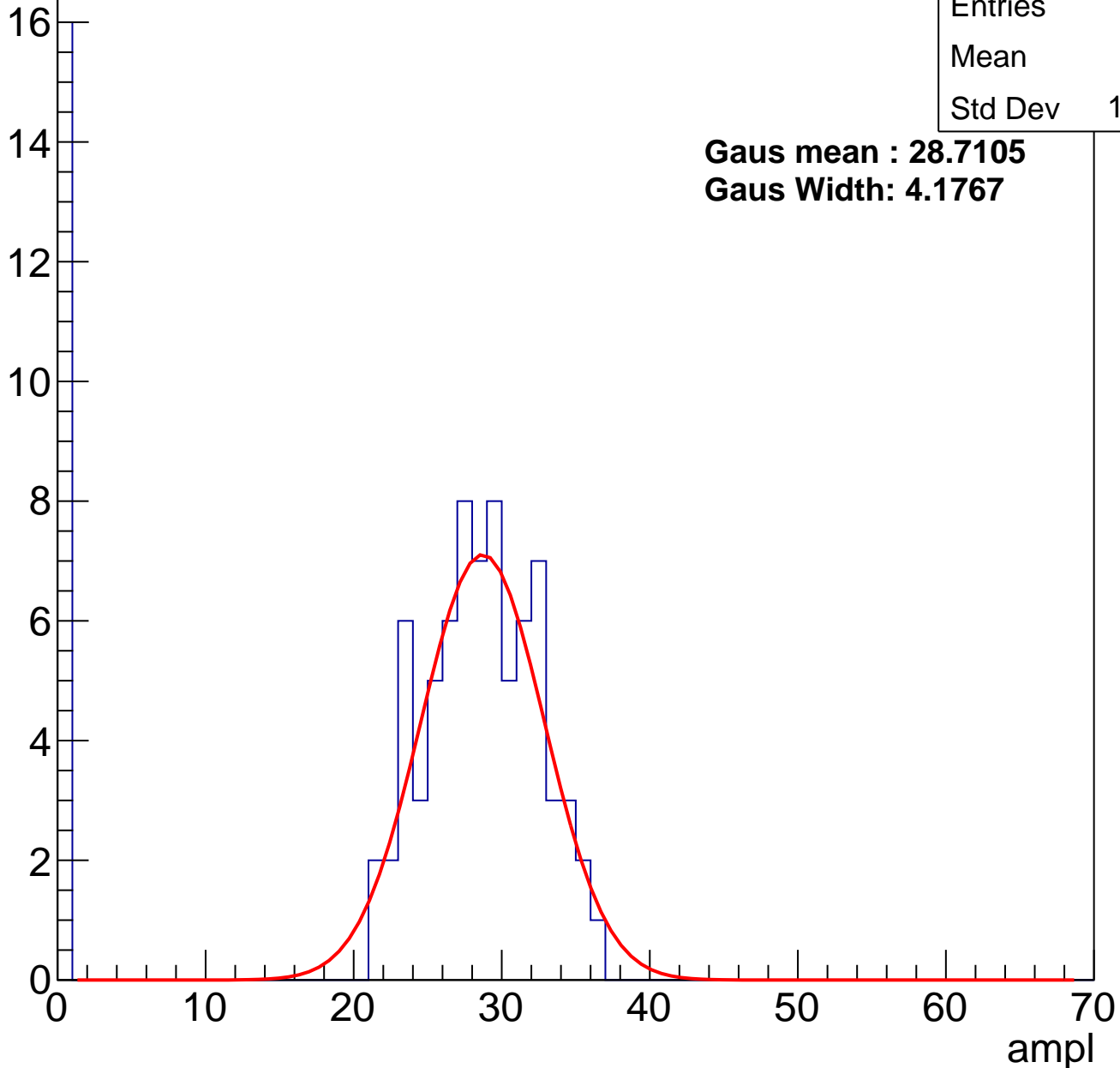
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	90
Mean	23.2
Std Dev	11.28

**Gaus mean : 28.7105**

**Gaus Width: 4.1767**

Entry



# B1L103S, U26-ch124, adc1

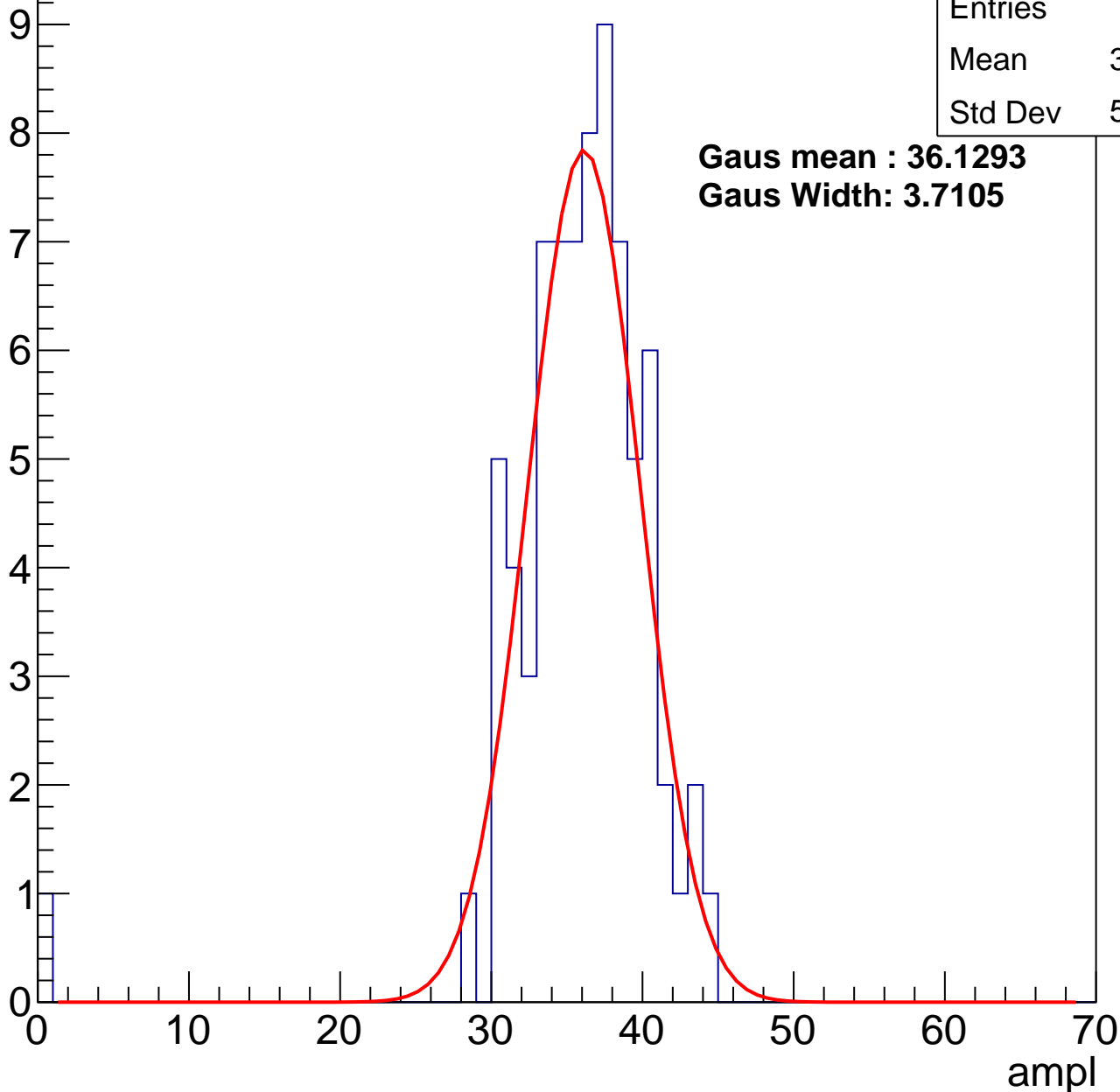
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	76
Mean	35.37
Std Dev	5.358

**Gaus mean : 36.1293**

**Gaus Width: 3.7105**



# B1L103S, U26-ch124, adc2

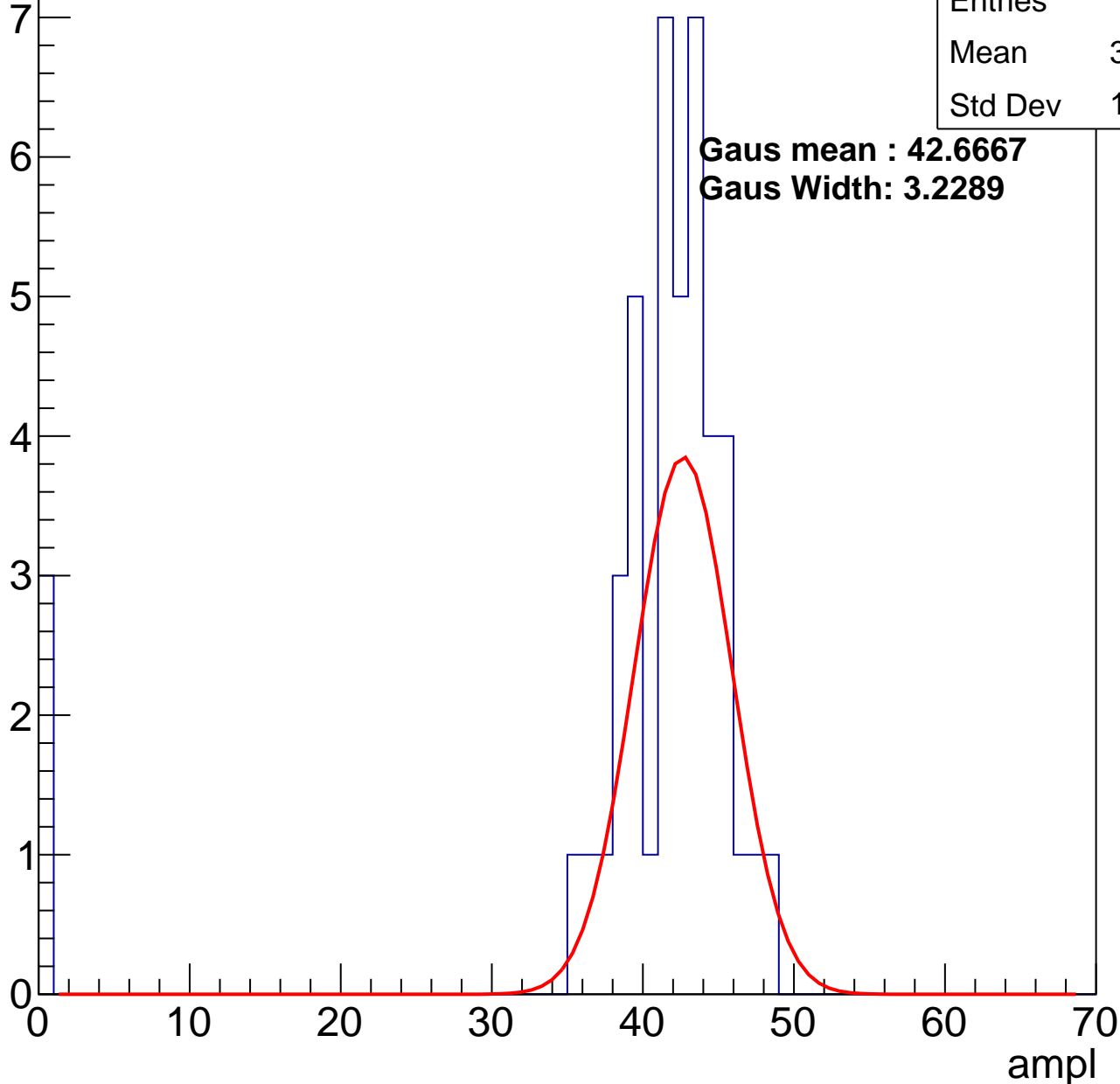
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	45
Mean	38.93
Std Dev	10.77

**Gaus mean : 42.6667**

**Gaus Width: 3.2289**



# B1L103S, U26-ch124, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	103
Mean	43.35
Std Dev	15.45

Entry

10

8

6

4

2

0

0

10

20

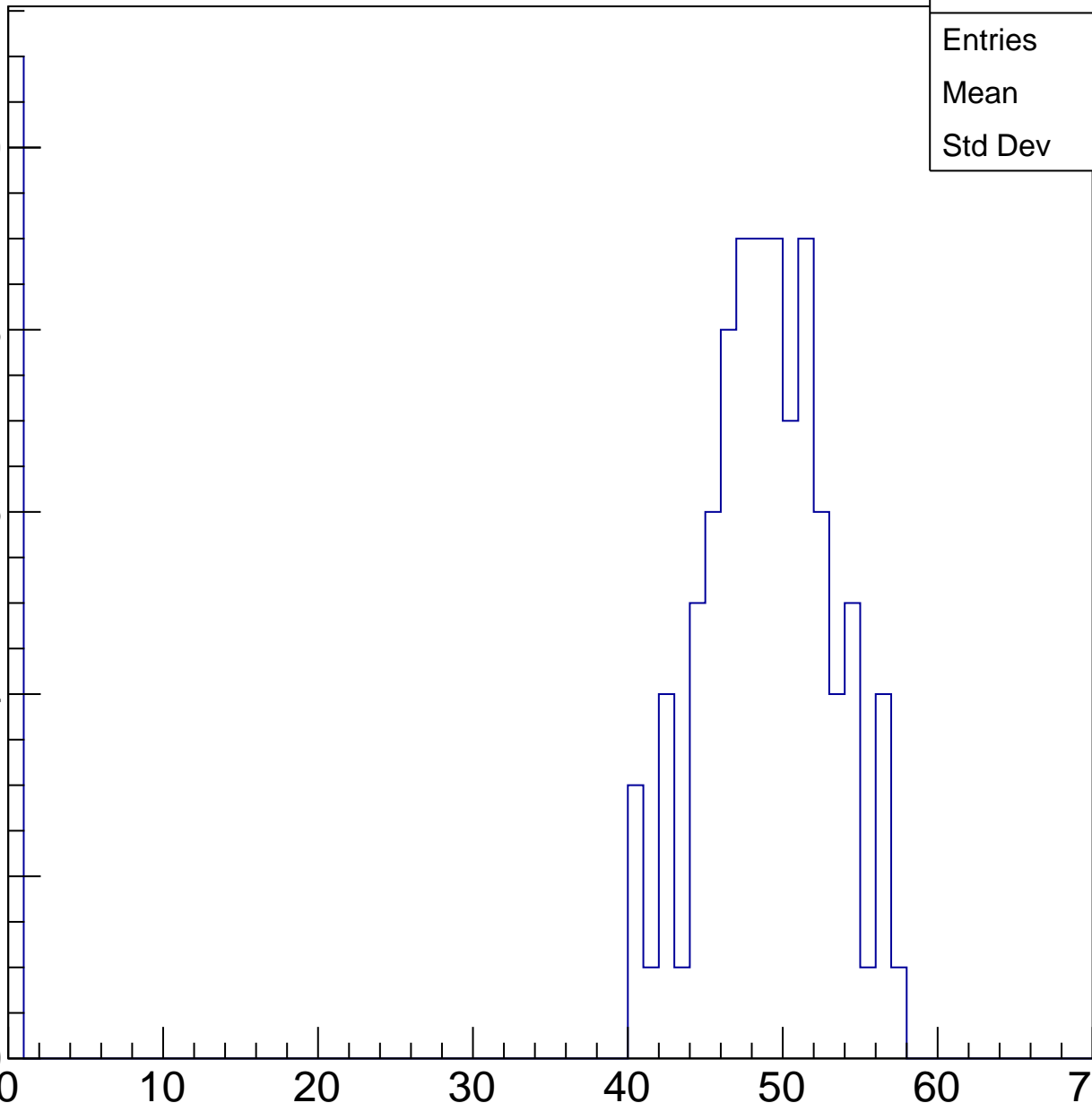
30

40

50

60

ampl

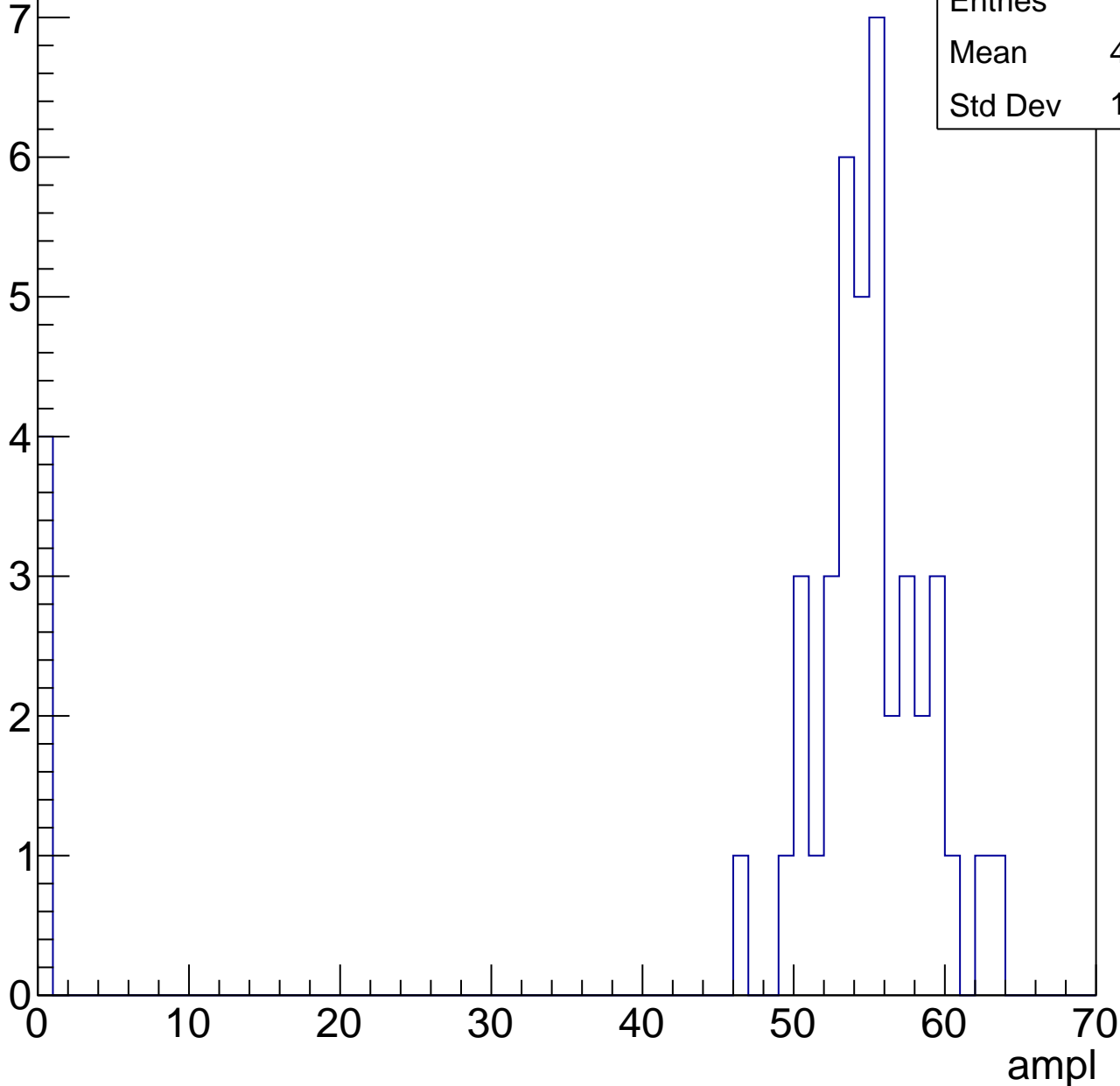


# B1L103S, U26-ch124, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	44
Mean	49.68
Std Dev	16.05

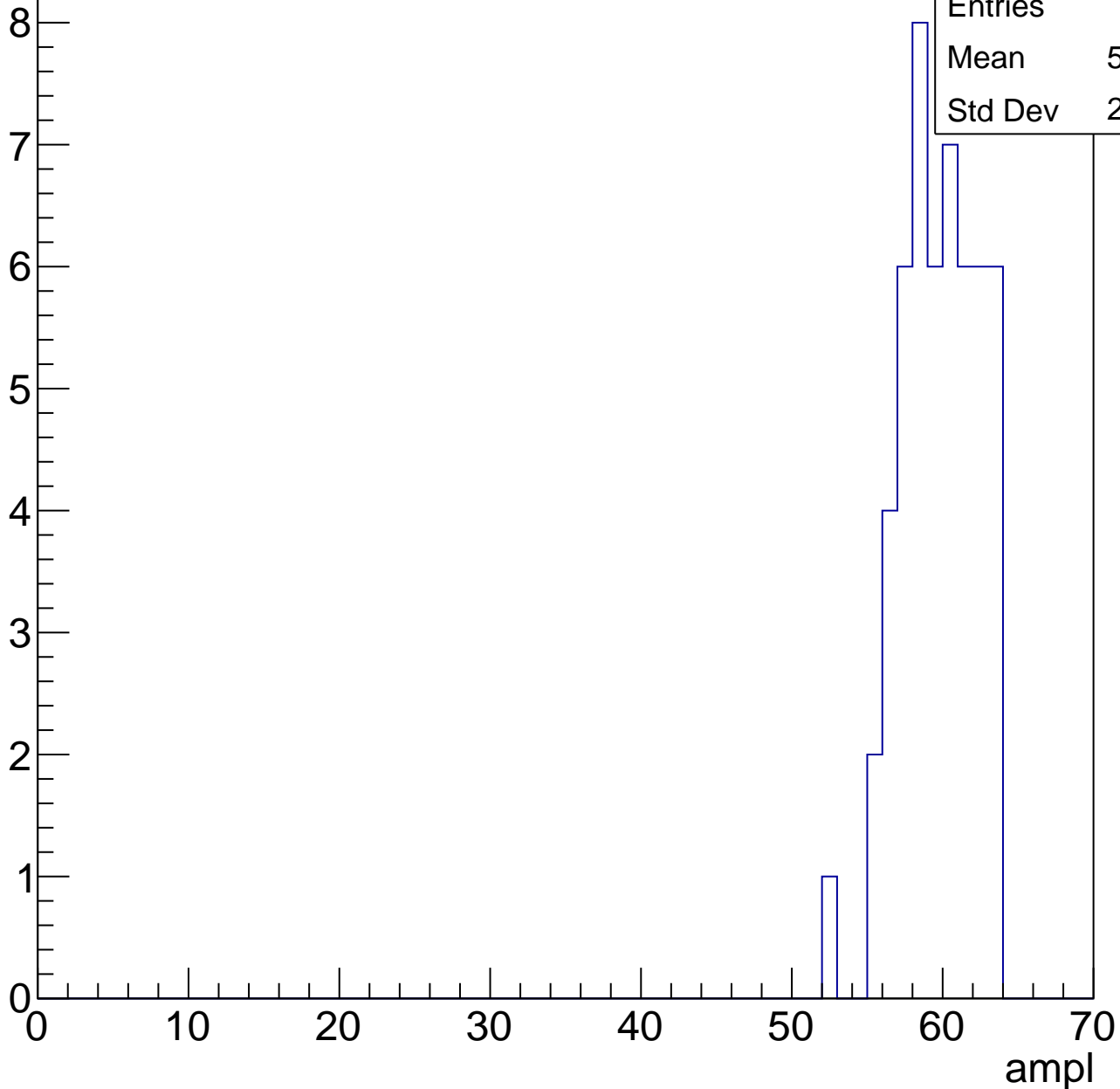


# B1L103S, U26-ch124, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

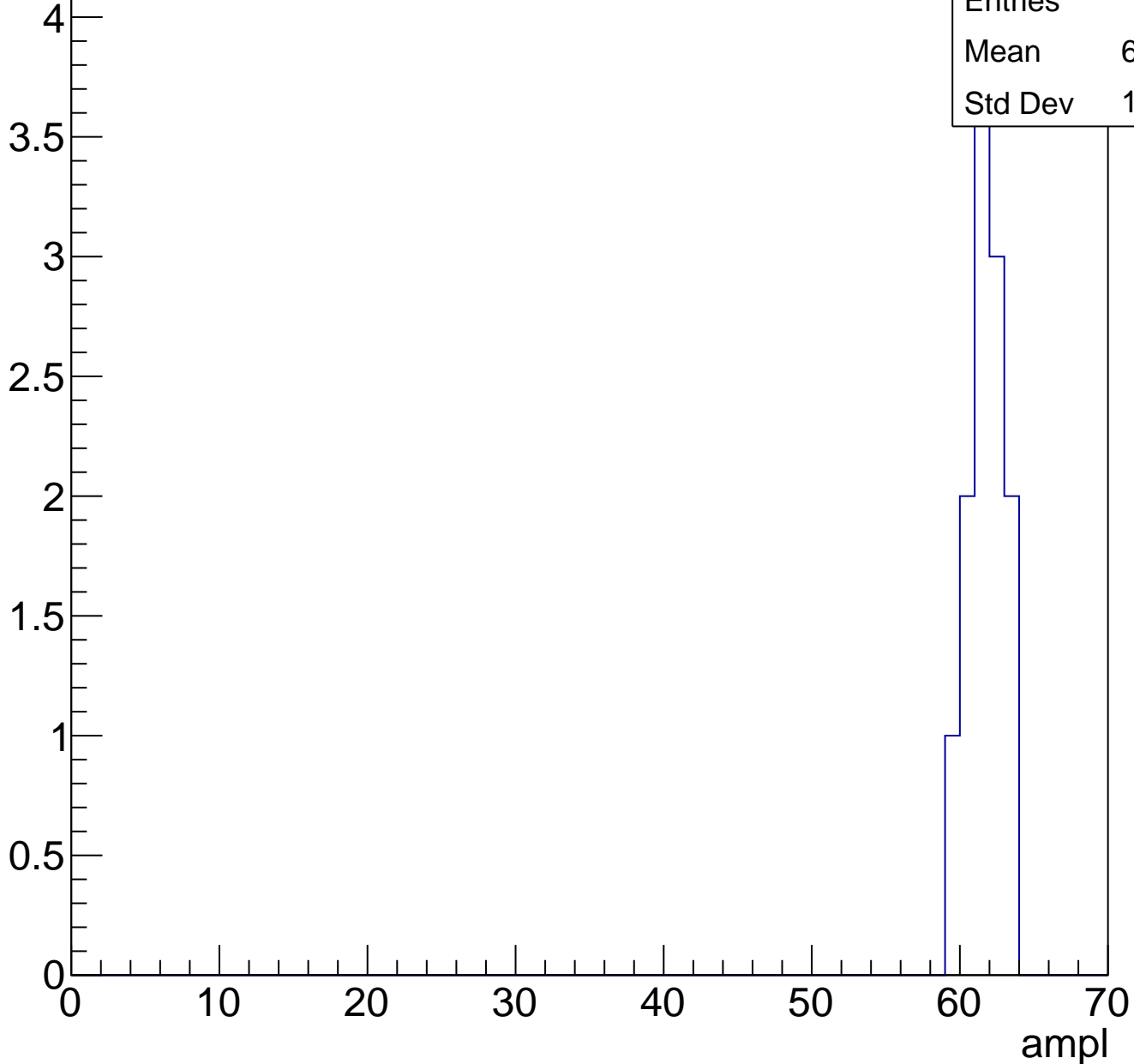
Entries	52
Mean	59.27
Std Dev	2.505



# B1L103S, U26-ch124, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

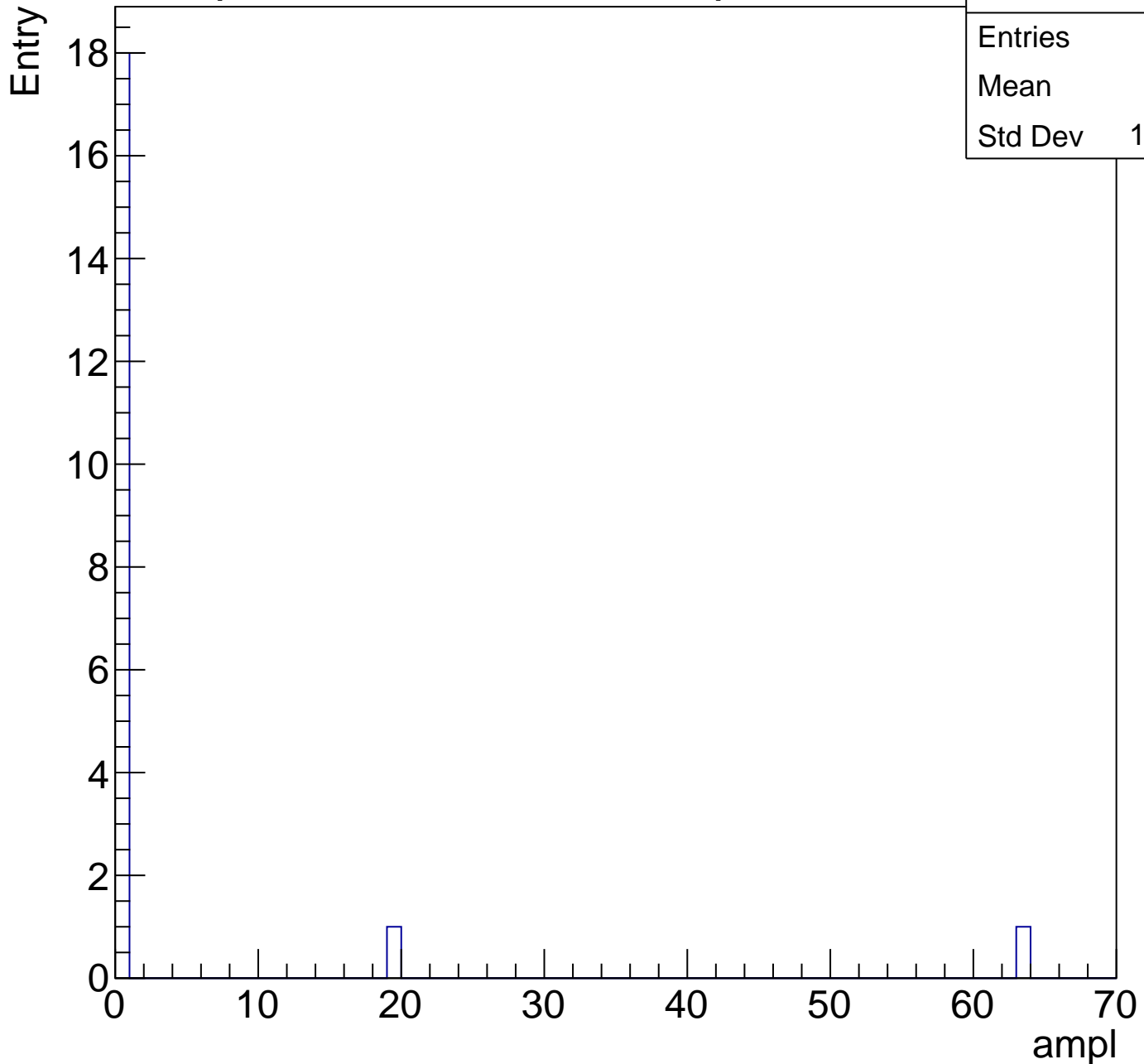




# B1L103S, U26-ch124, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	20
Mean	4.1
Std Dev	14.13



# B1L103S, U26-ch125, adc0

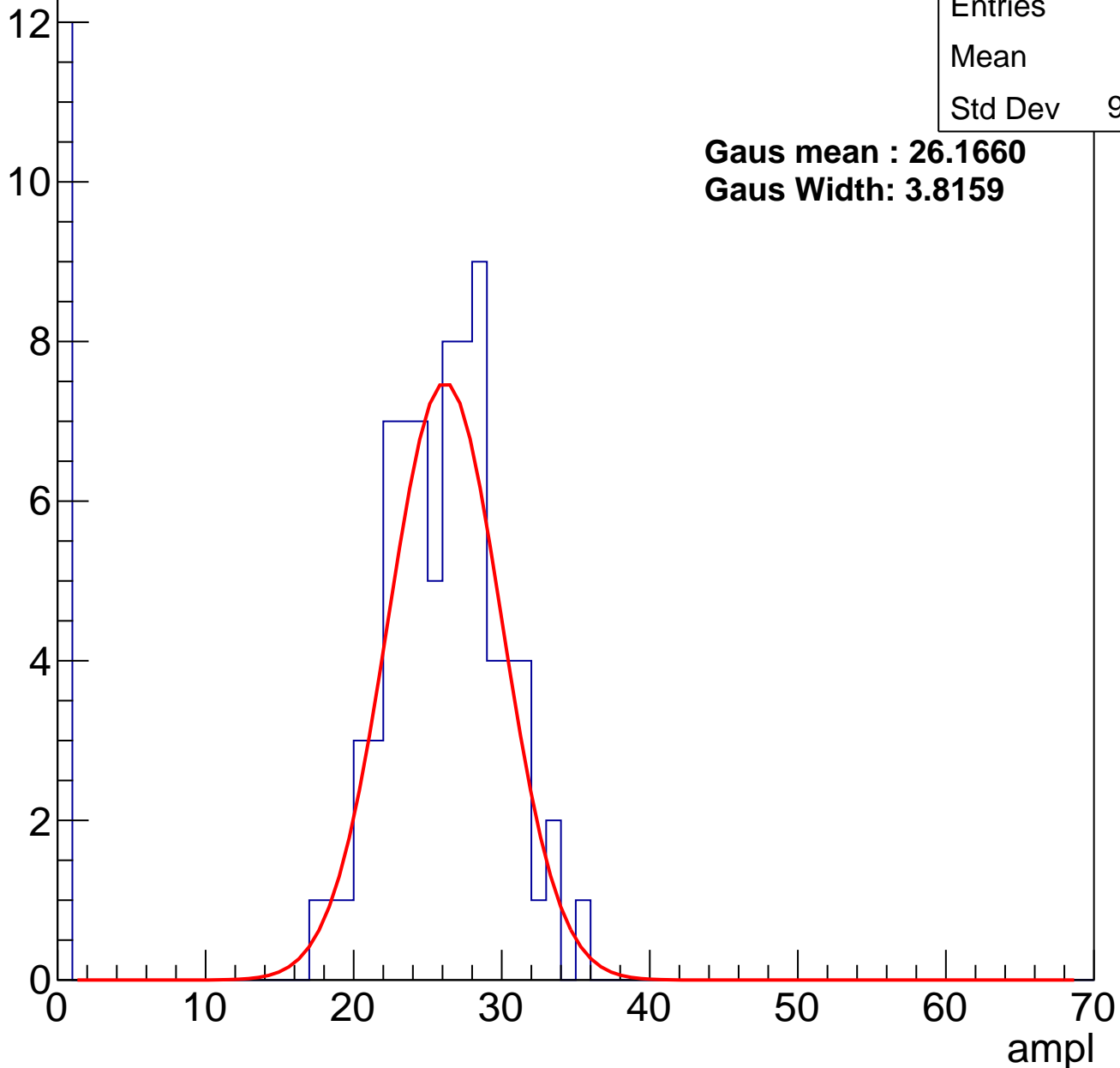
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	88
Mean	22.2
Std Dev	9.468

**Gaus mean : 26.1660**

**Gaus Width: 3.8159**

Entry



# B1L103S, U26-ch125, adc1

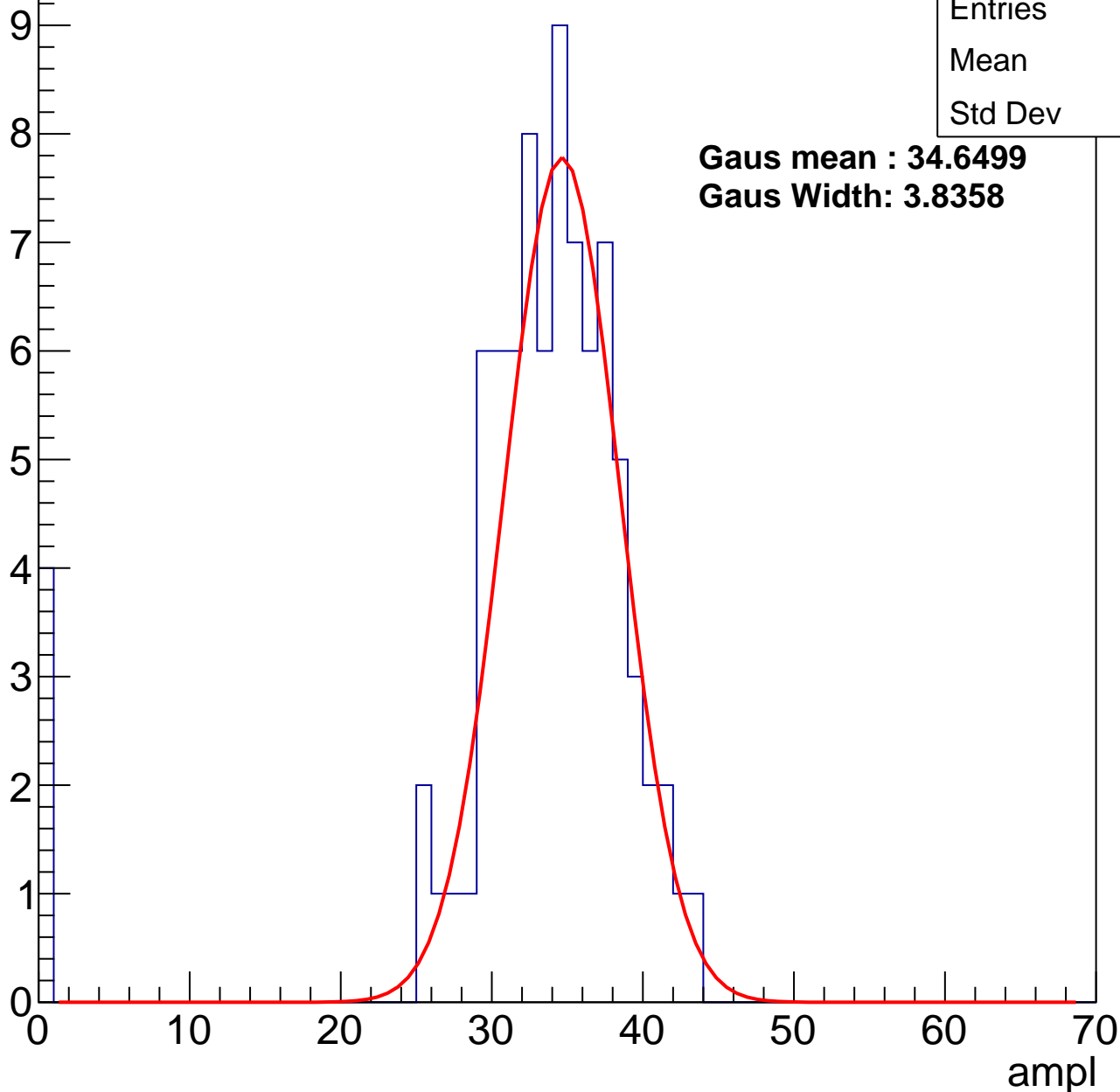
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	84
Mean	32.2
Std Dev	8.14

**Gaus mean : 34.6499**

**Gaus Width: 3.8358**



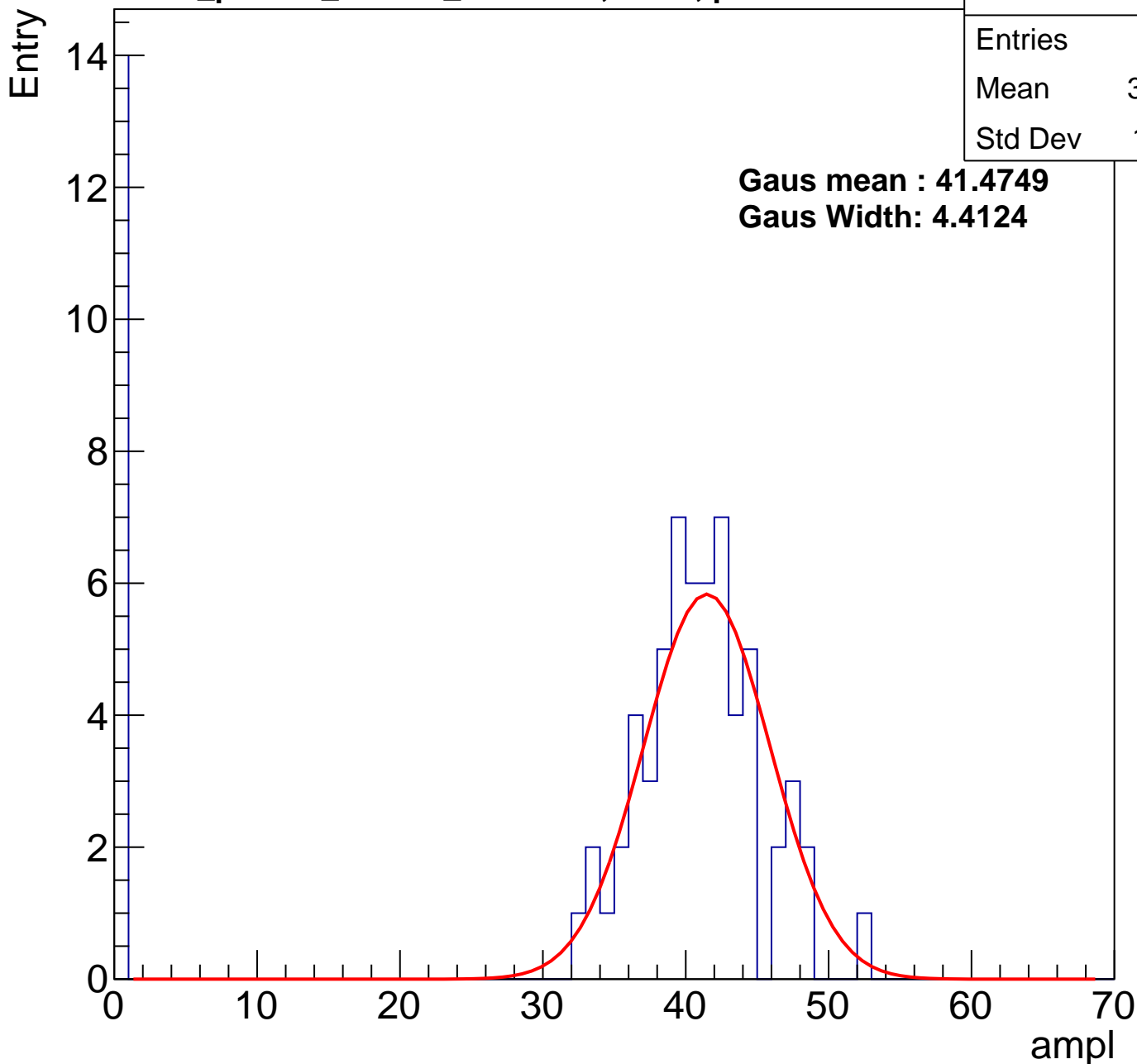
# B1L103S, U26-ch125, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	75
Mean	32.97
Std Dev	16.21

**Gaus mean : 41.4749**

**Gaus Width: 4.4124**

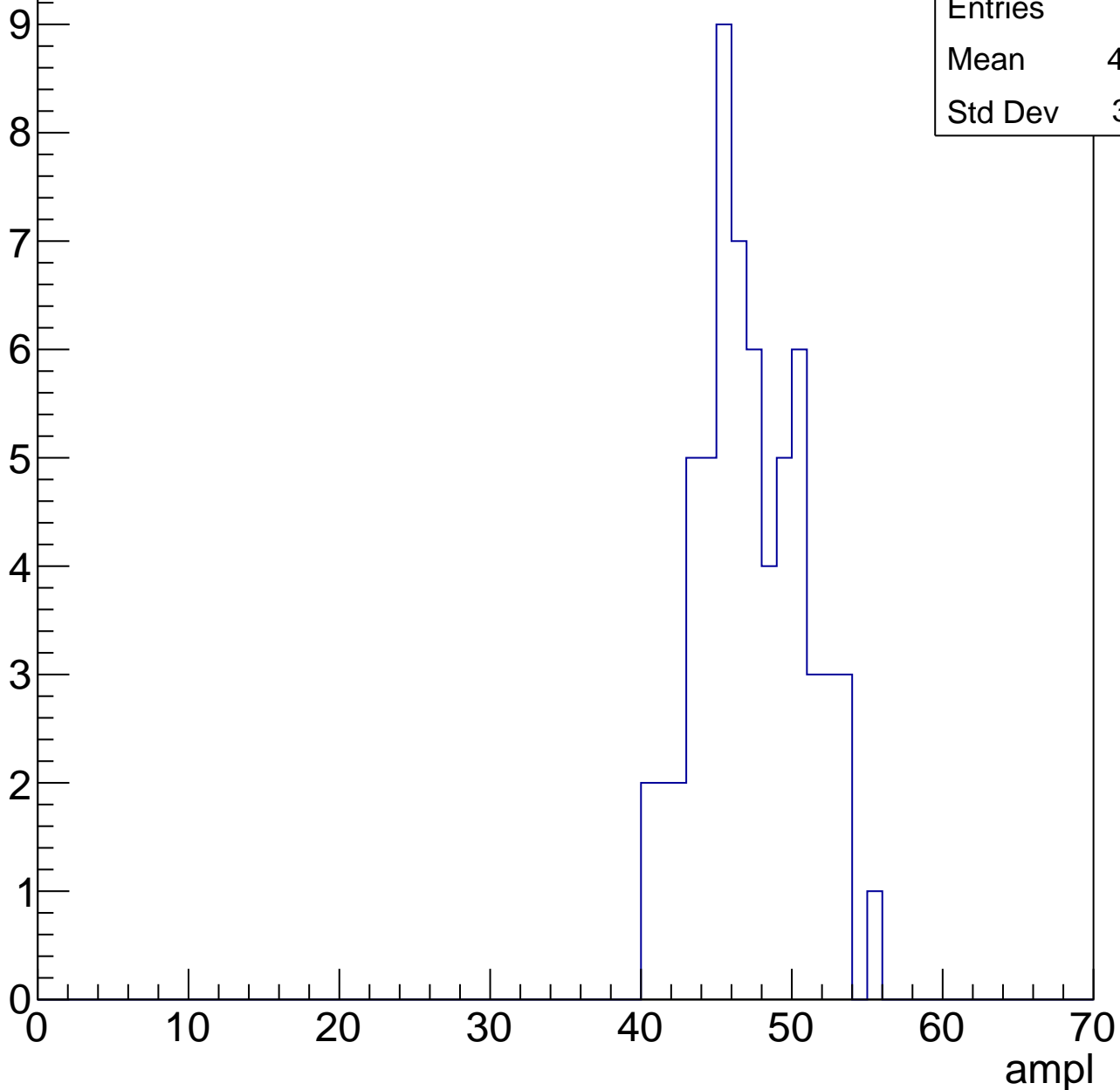


# B1L103S, U26-ch125, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	63
Mean	46.83
Std Dev	3.471

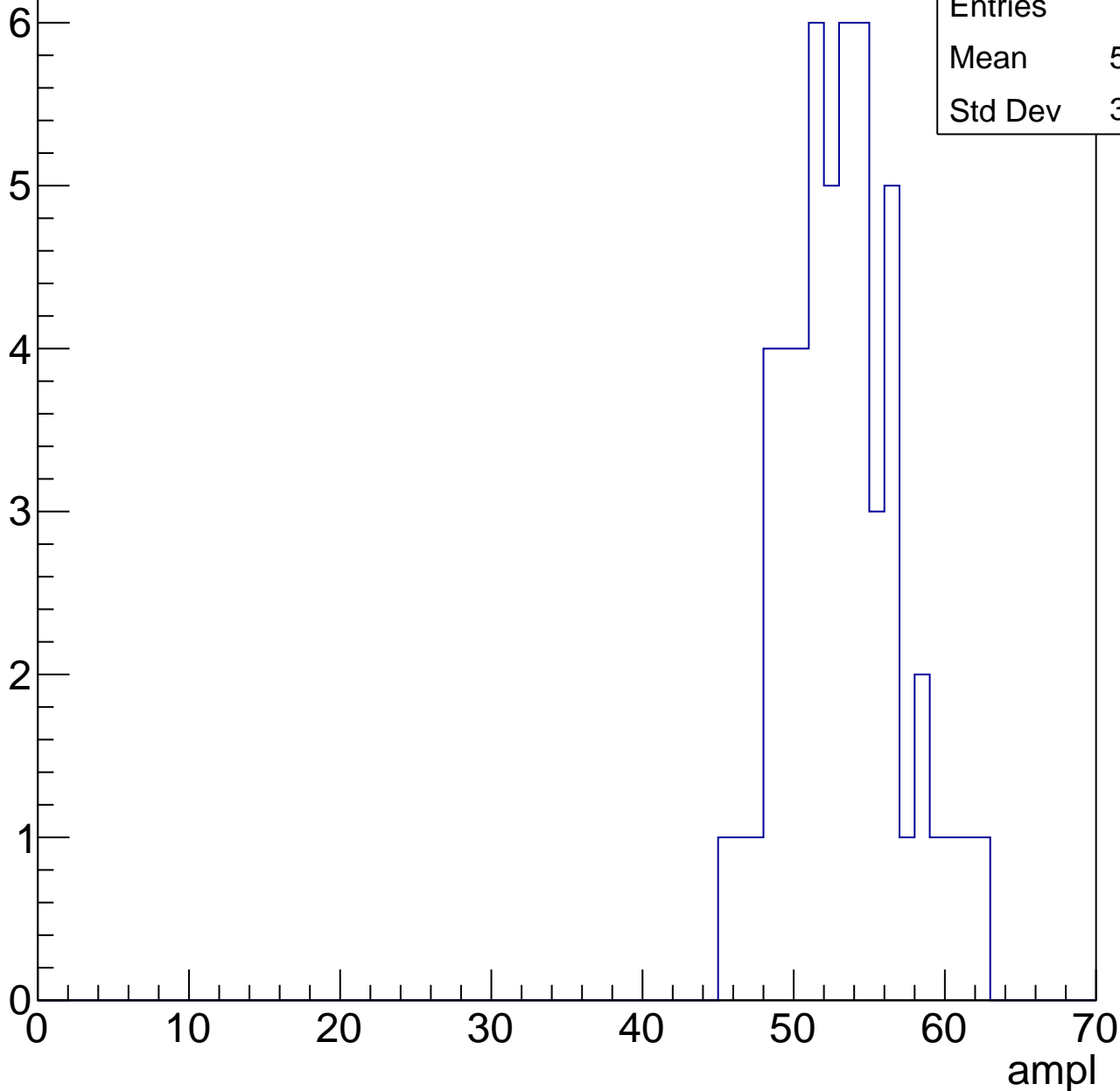


# B1L103S, U26-ch125, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	53
Mean	52.72
Std Dev	3.718

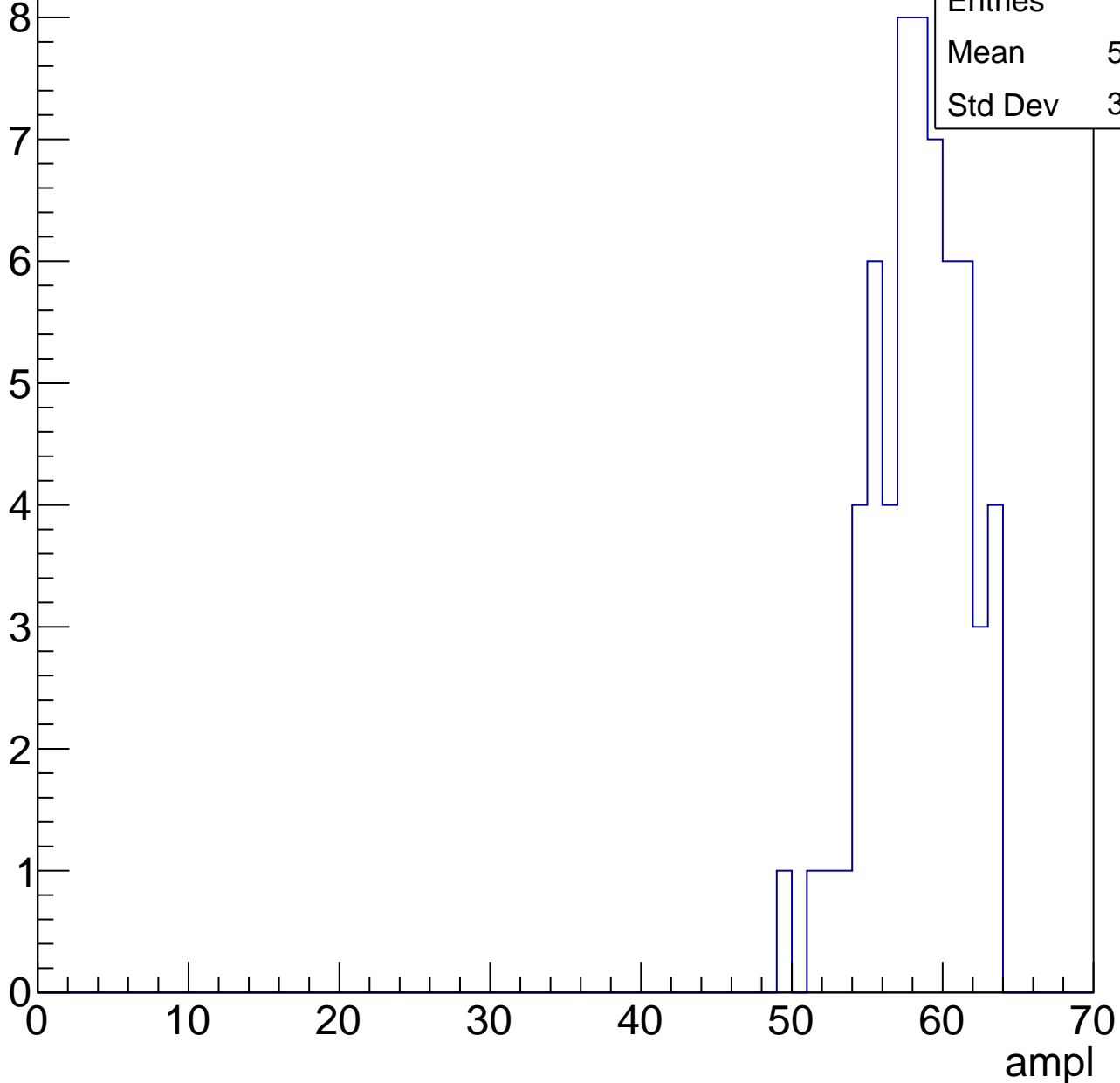


# B1L103S, U26-ch125, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	60
Mean	57.87
Std Dev	3.068

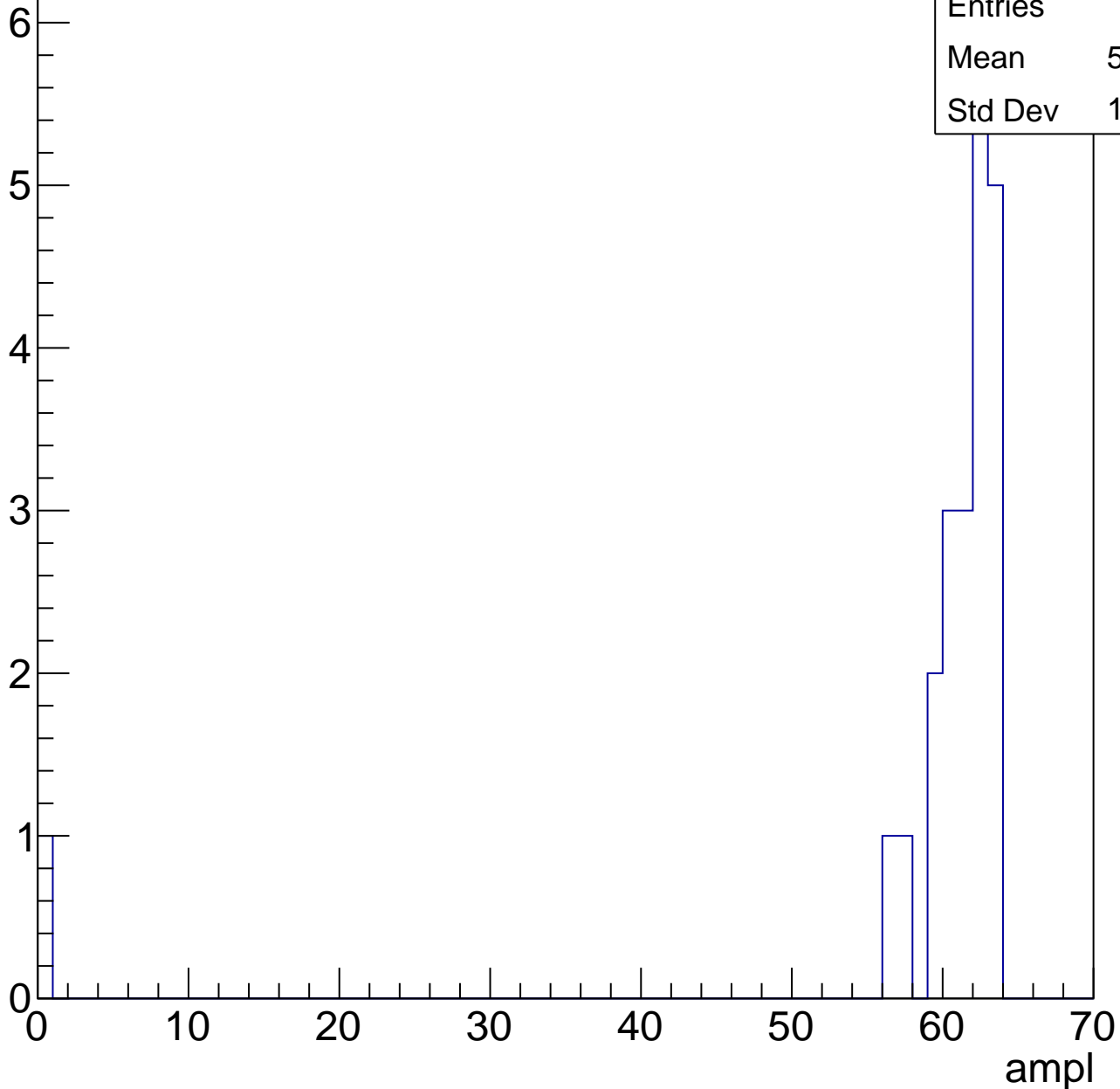


# B1L103S, U26-ch125, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	22
Mean	58.23
Std Dev	12.84





# B1L103S, U26-ch125, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	20
Mean	3.15
Std Dev	13.73

Entry



# B1L103S, U26-ch126, adc0

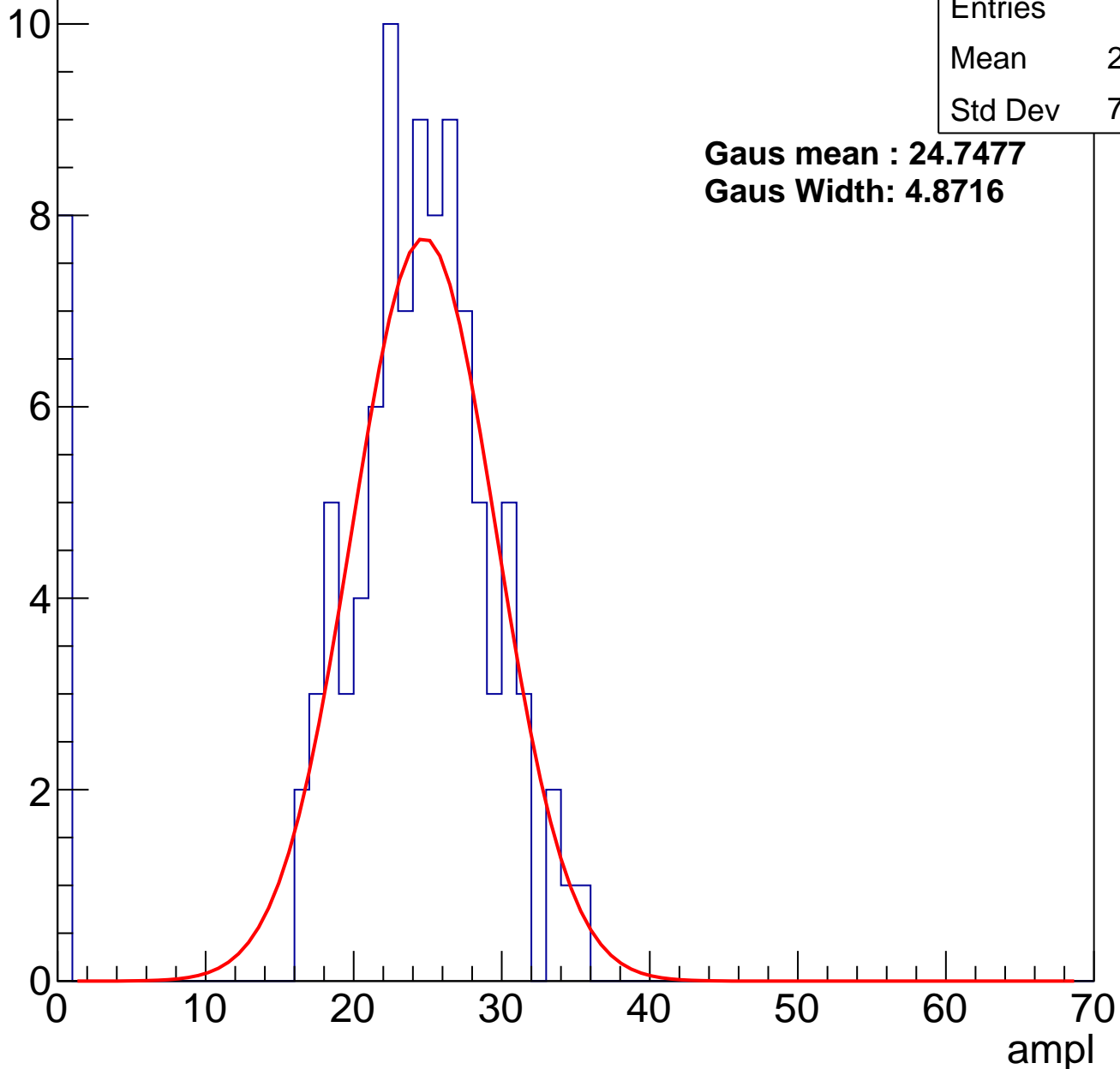
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	101
Mean	22.39
Std Dev	7.715

**Gaus mean : 24.7477**

**Gaus Width: 4.8716**

Entry



# B1L103S, U26-ch126, adc1

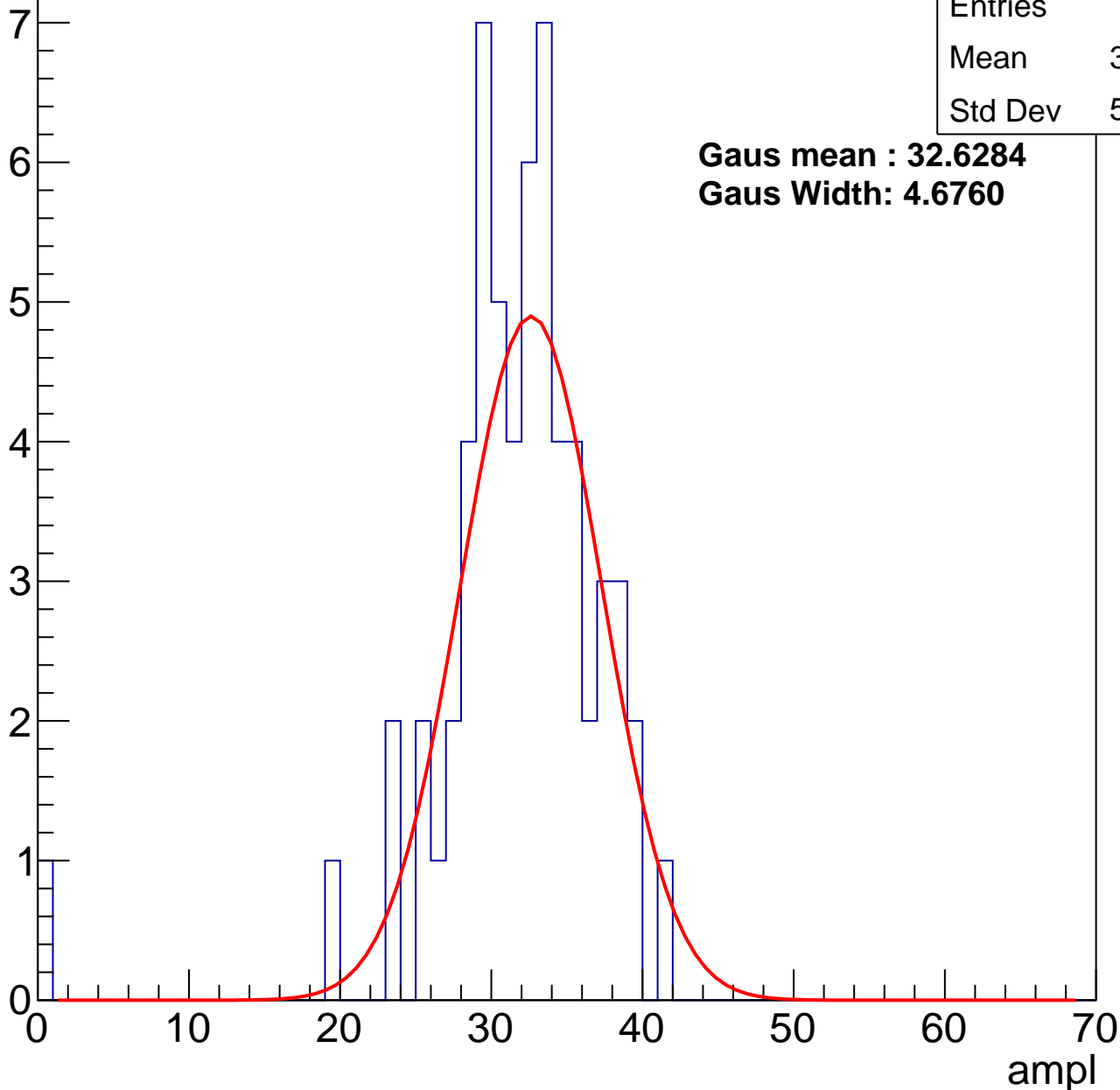
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	61
Mean	31.13
Std Dev	5.863

**Gaus mean : 32.6284**

**Gaus Width: 4.6760**



# B1L103S, U26-ch126, adc2

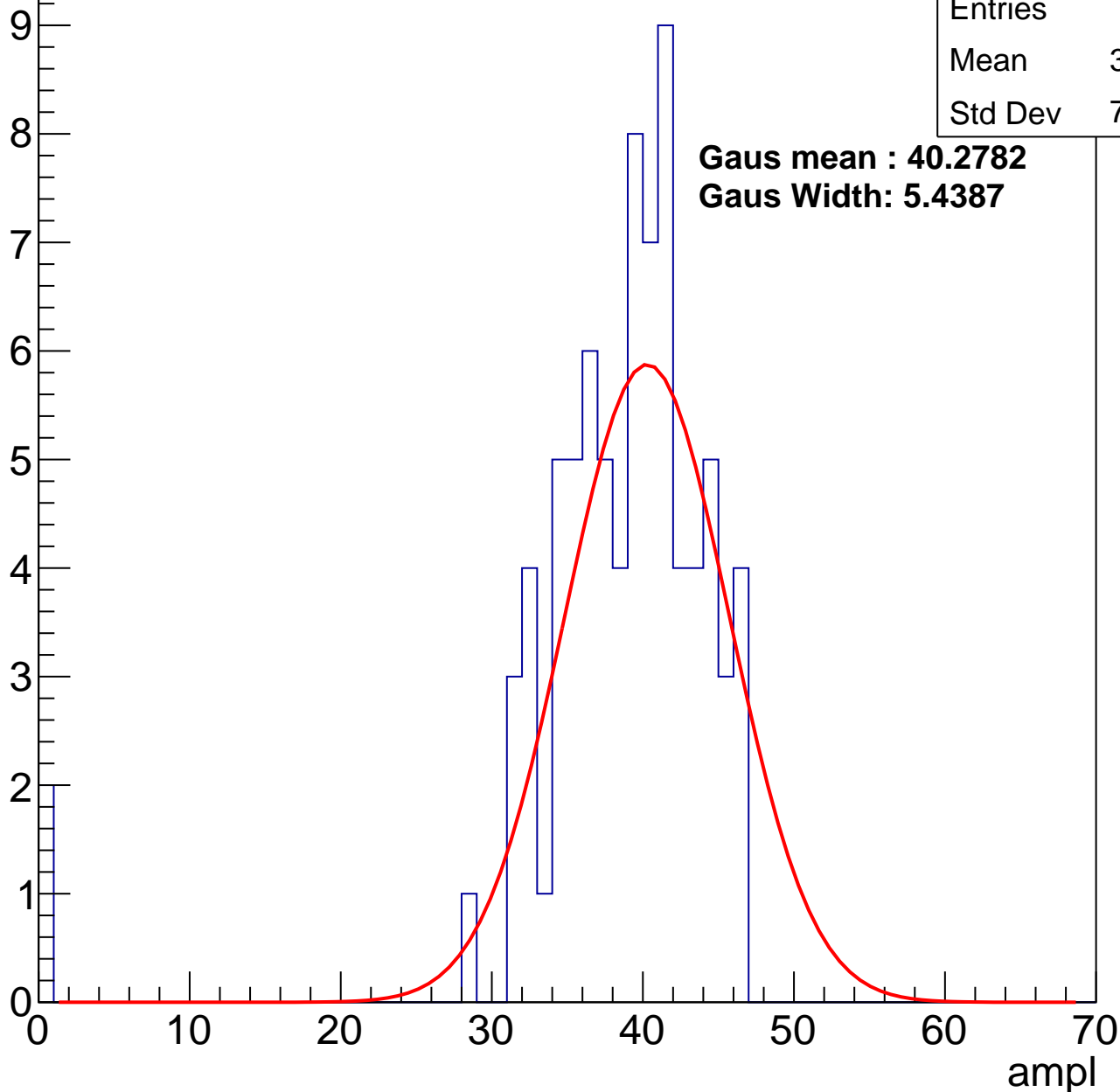
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	80
Mean	37.75
Std Dev	7.346

**Gaus mean : 40.2782**

**Gaus Width: 5.4387**

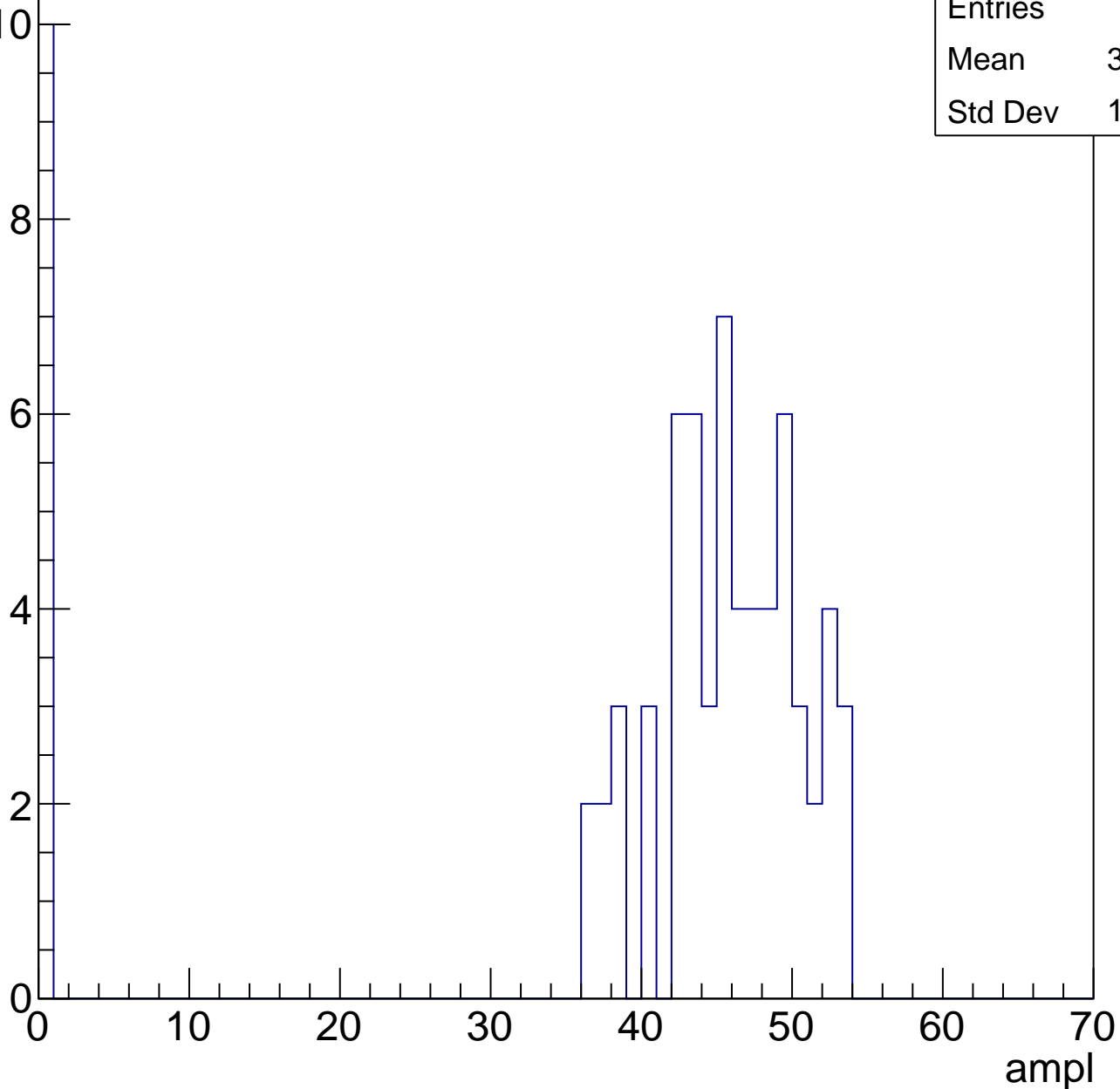


# B1L103S, U26-ch126, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	72
Mean	39.08
Std Dev	16.25

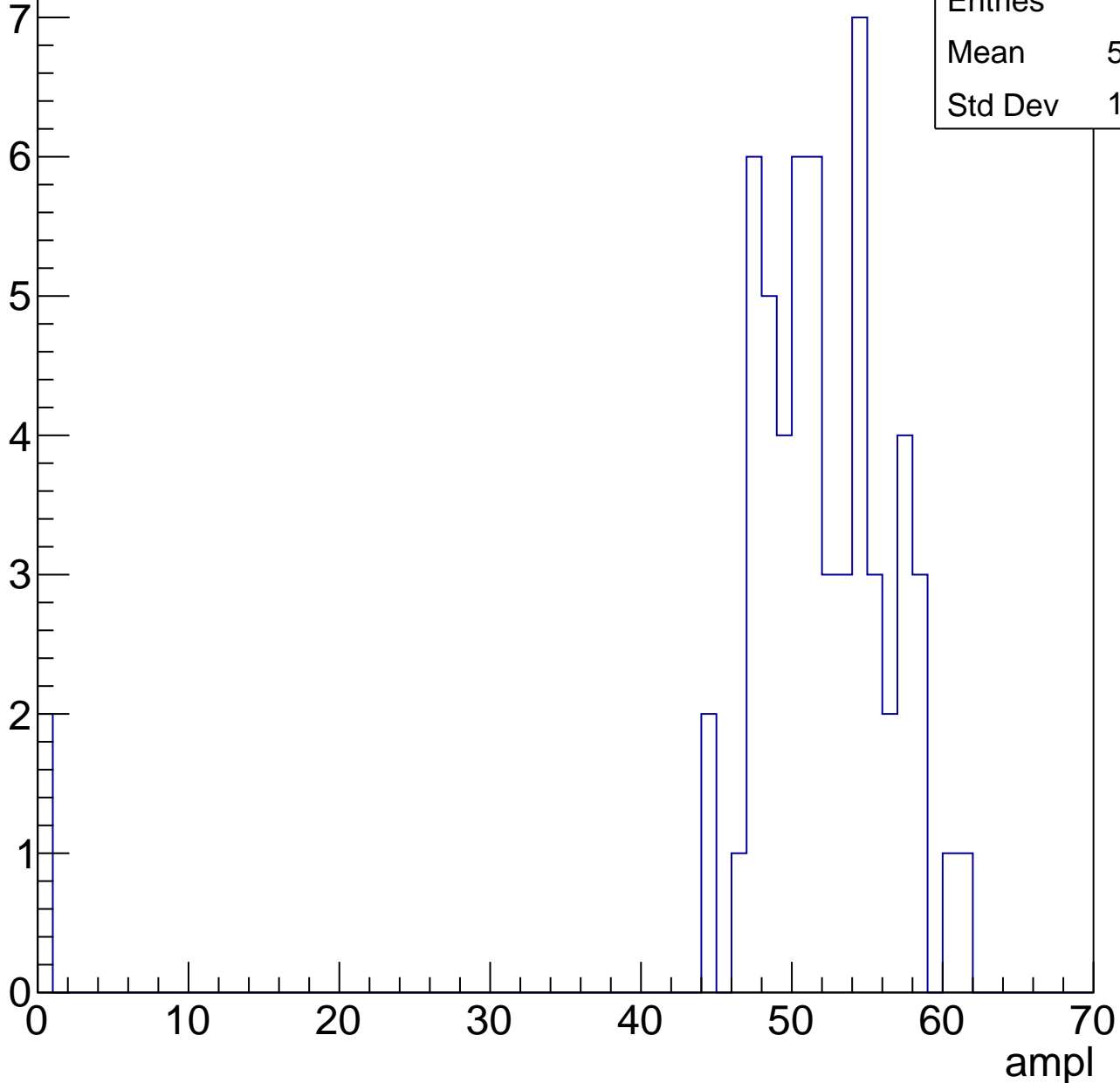


# B1L103S, U26-ch126, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	59
Mean	50.02
Std Dev	10.15

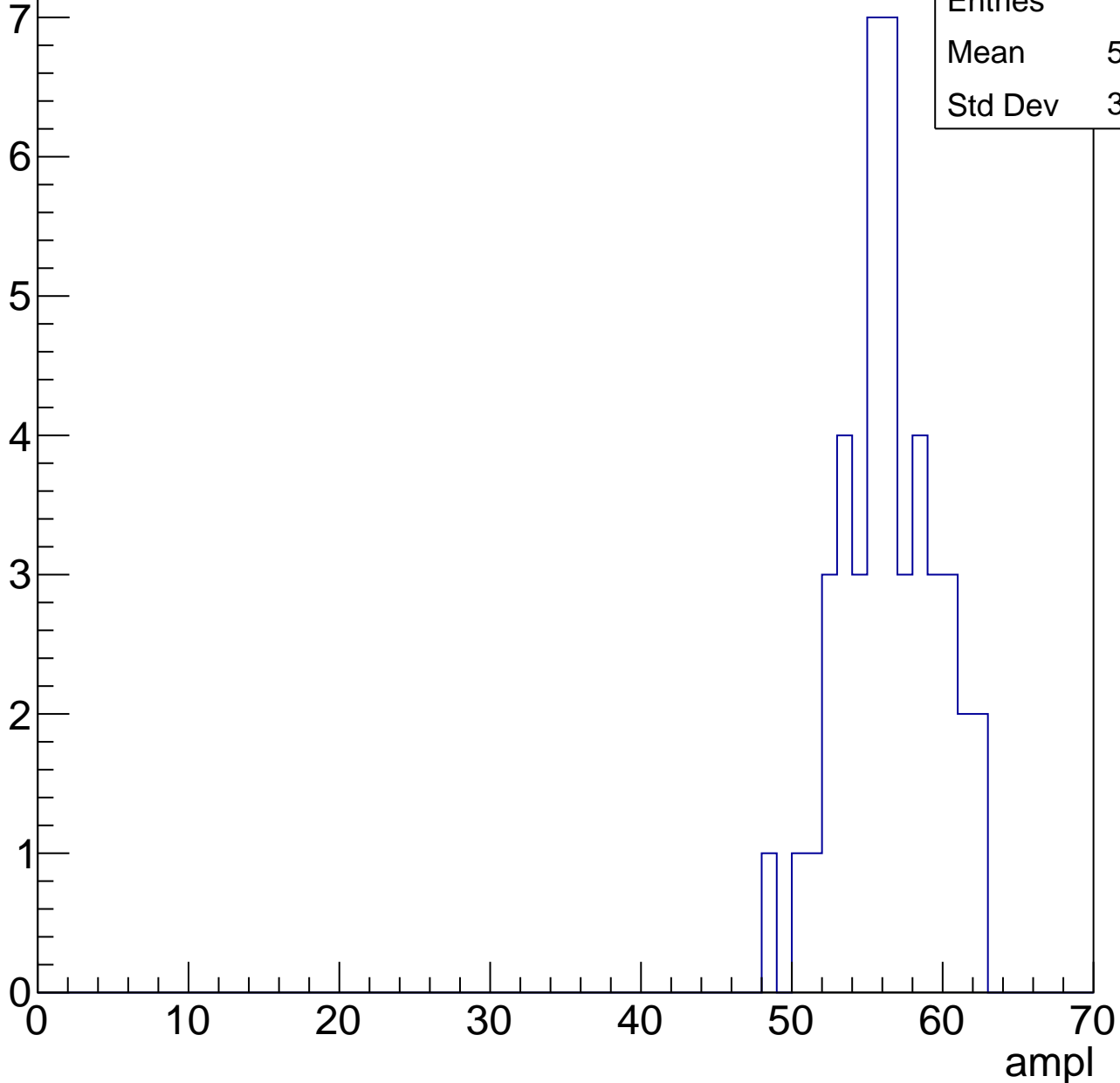


# B1L103S, U26-ch126, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	44
Mean	55.95
Std Dev	3.176

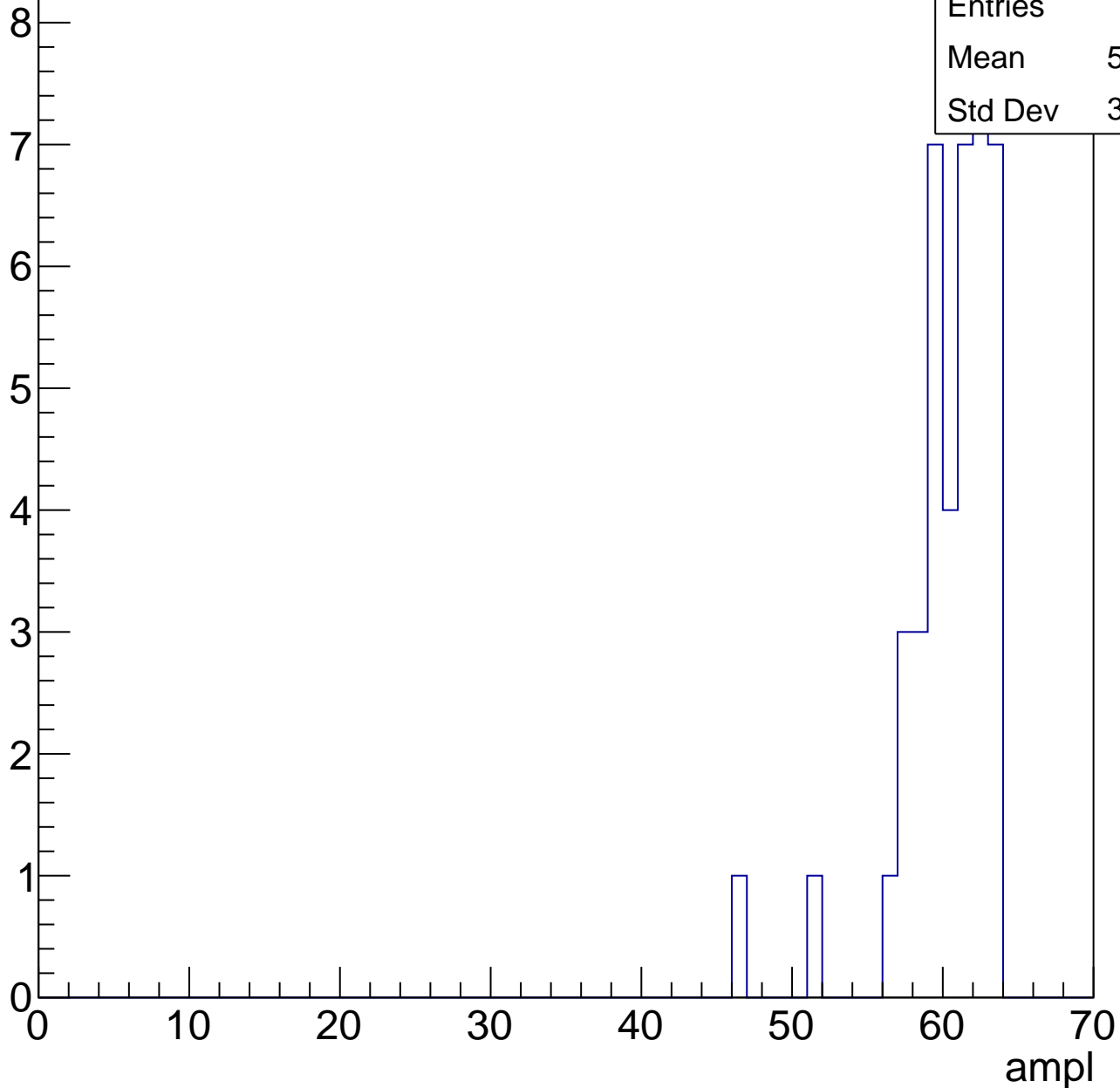


# B1L103S, U26-ch126, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	42
Mean	59.88
Std Dev	3.238

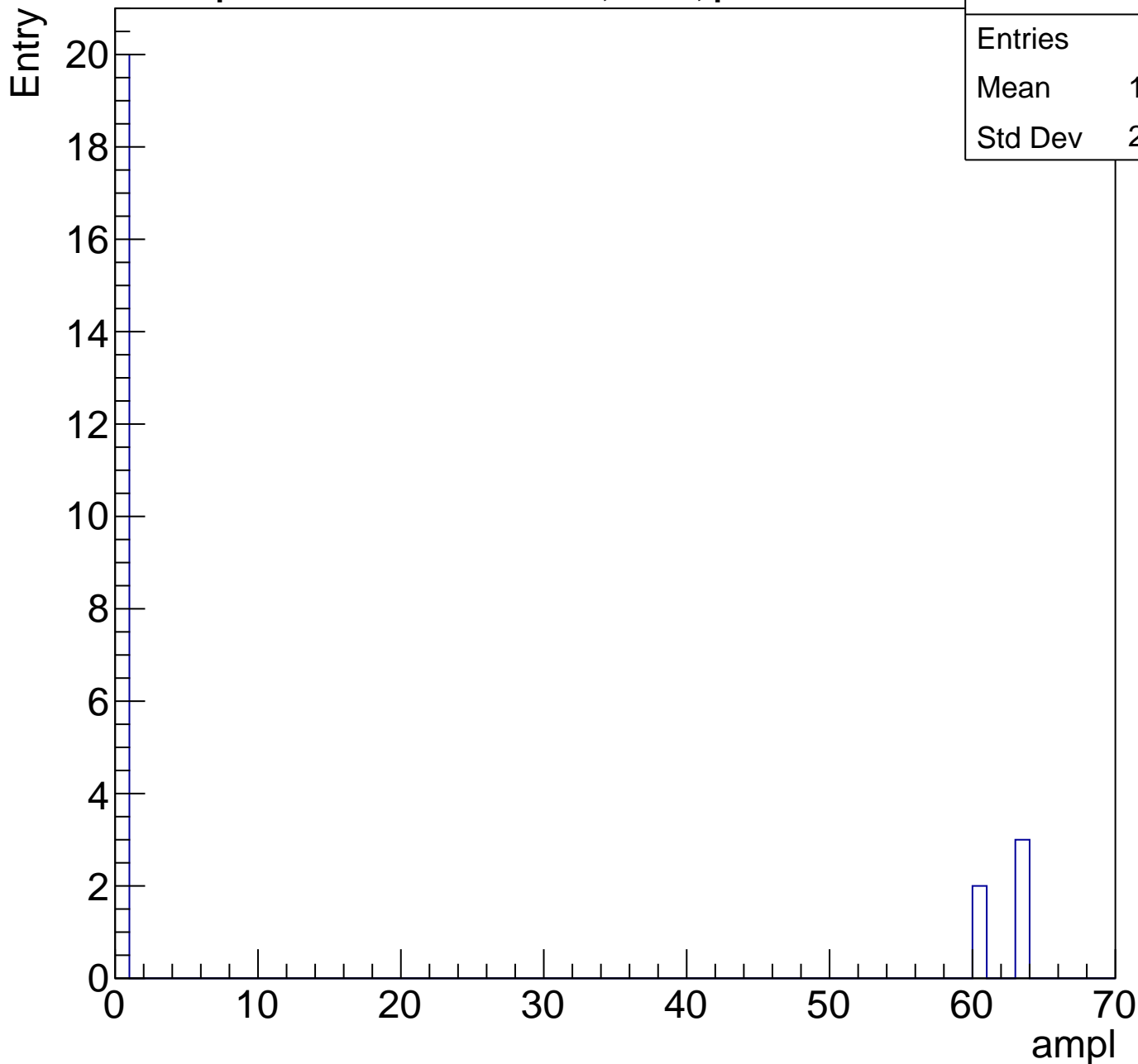




# B1L103S, U26-ch126, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	25
Mean	12.36
Std Dev	24.73



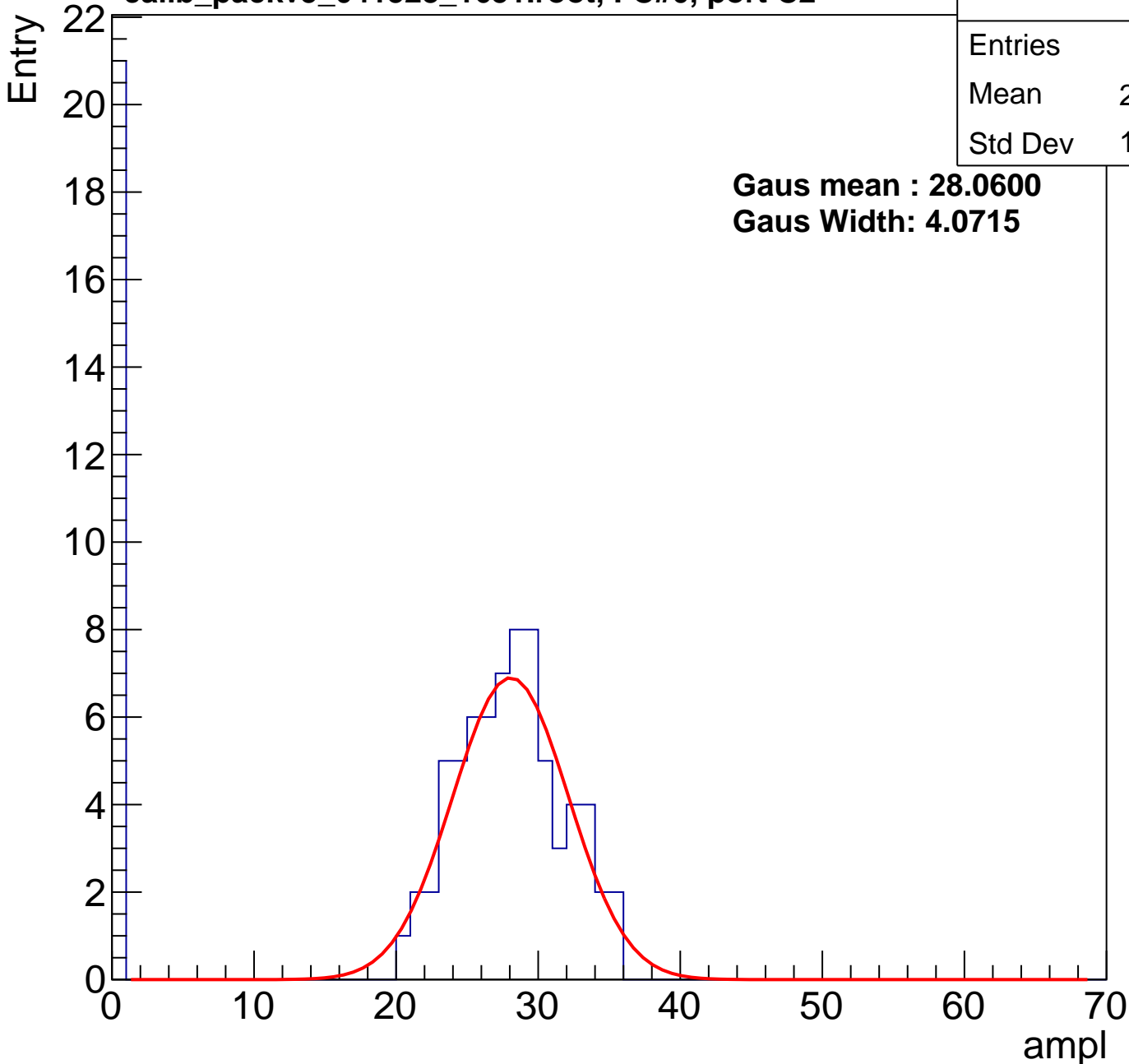
# B1L103S, U26-ch127, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	91
Mean	21.24
Std Dev	12.05

**Gaus mean : 28.0600**

**Gaus Width: 4.0715**



# B1L103S, U26-ch127, adc1

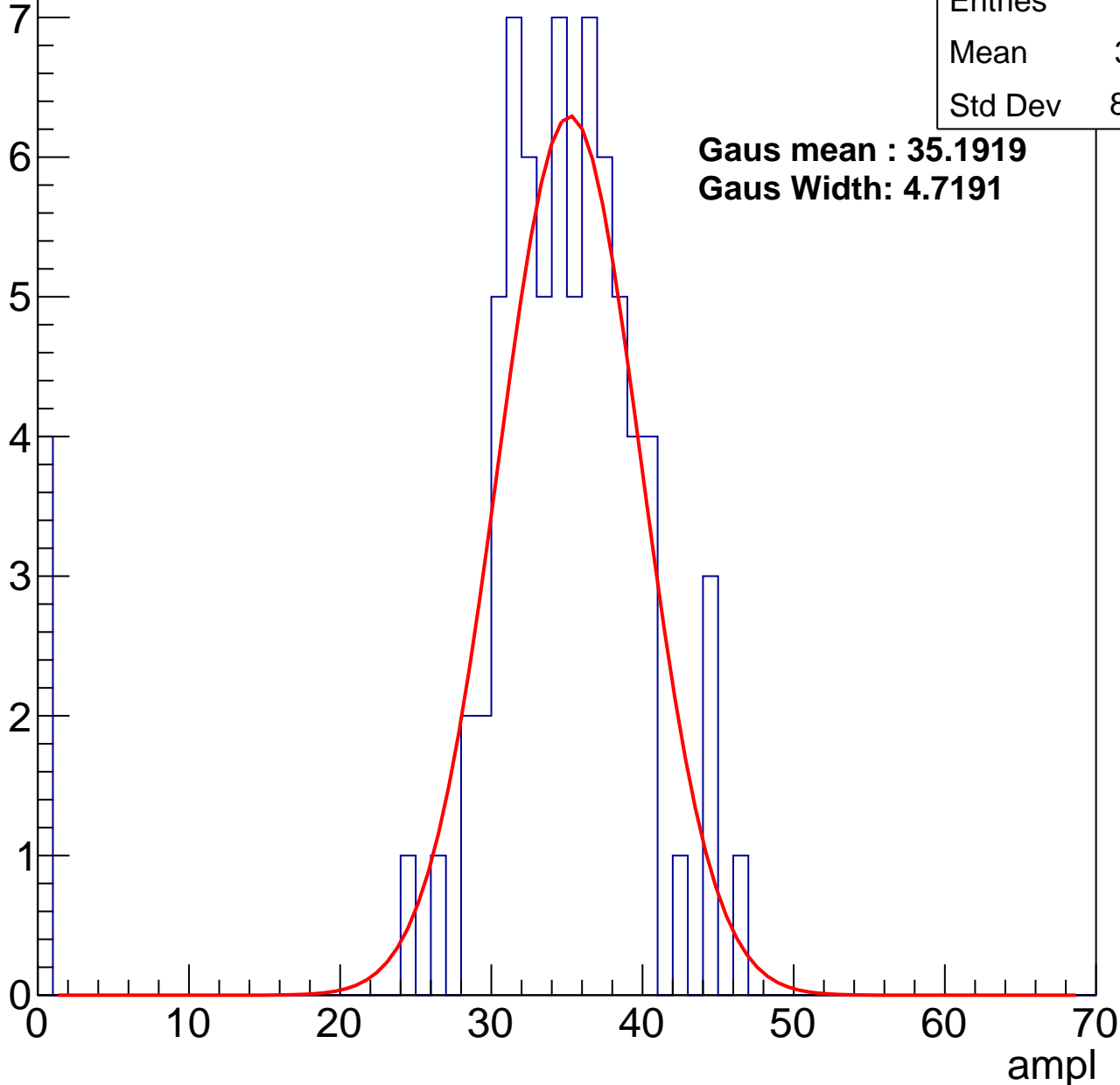
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	76
Mean	32.91
Std Dev	8.819

**Gaus mean : 35.1919**

**Gaus Width: 4.7191**



# B1L103S, U26-ch127, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	66
Mean	33.42
Std Dev	15.24

**Gaus mean : 40.1515**  
**Gaus Width: 3.1708**

Entry

10

8

6

4

2

0

0

10

20

30

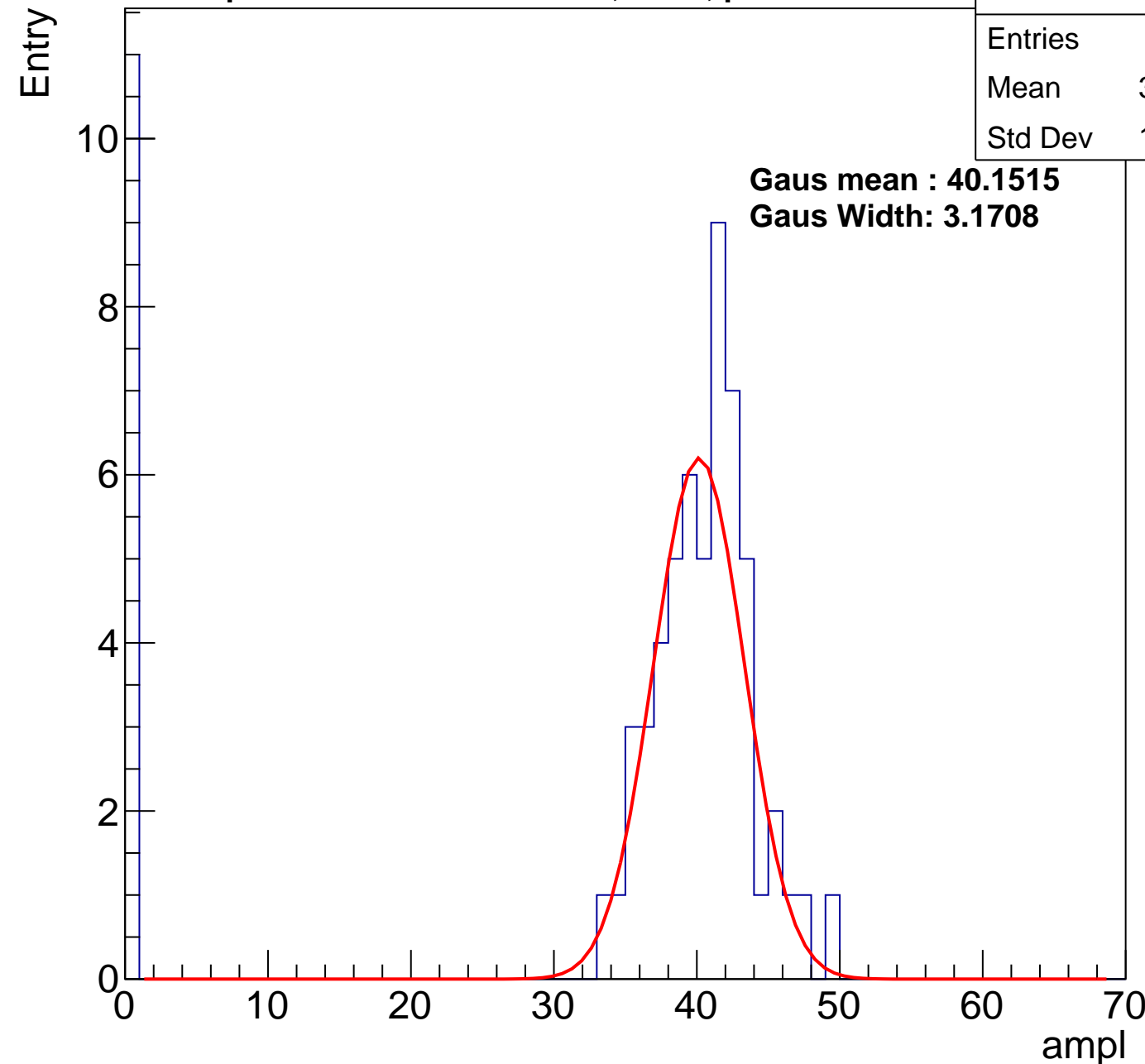
40

50

60

70

ampl

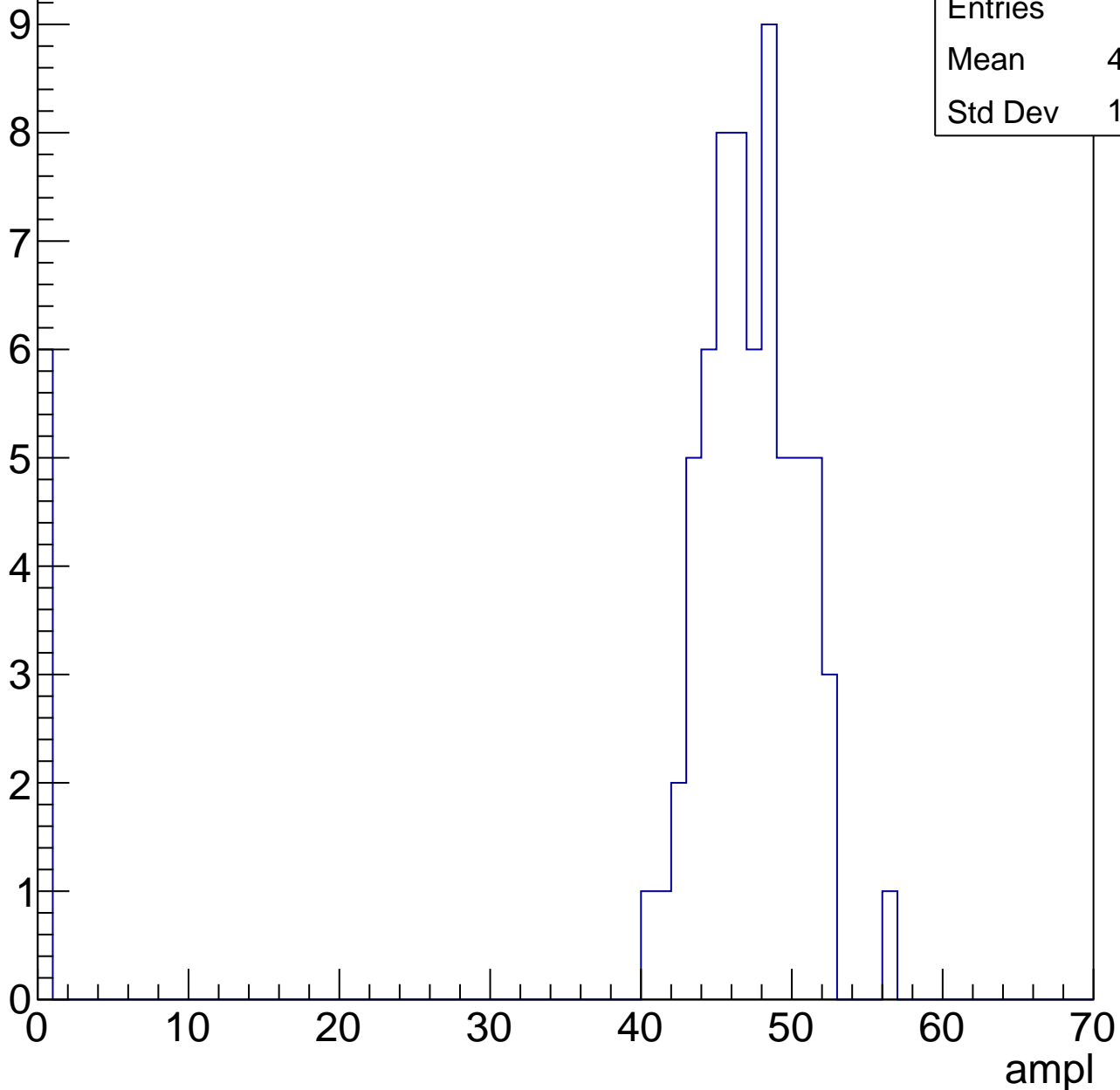


# B1L103S, U26-ch127, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

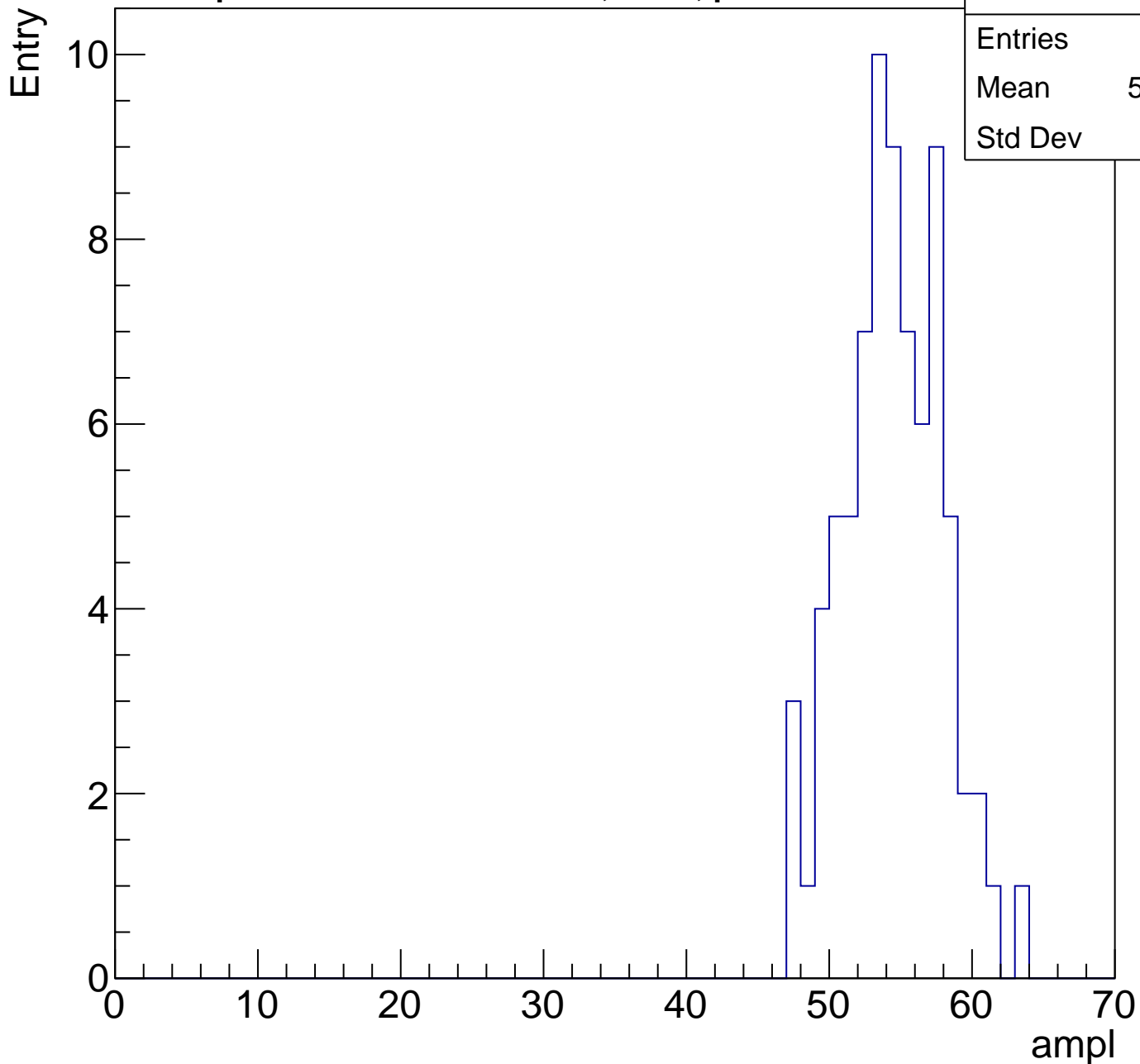
Entries	71
Mean	42.93
Std Dev	13.37



# B1L103S, U26-ch127, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	77
Mean	53.97
Std Dev	3.4

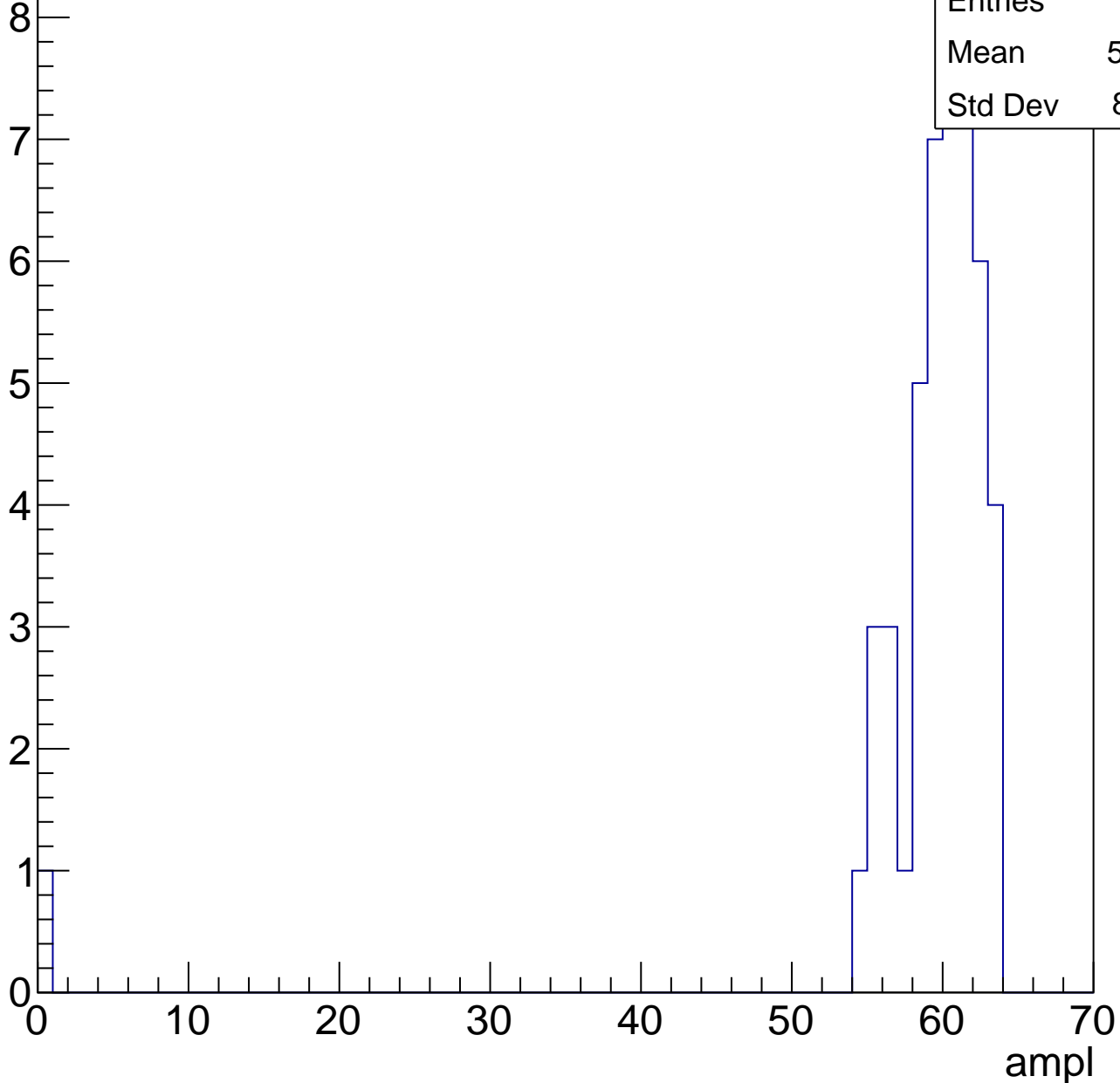


# B1L103S, U26-ch127, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	47
Mean	58.28
Std Dev	8.901

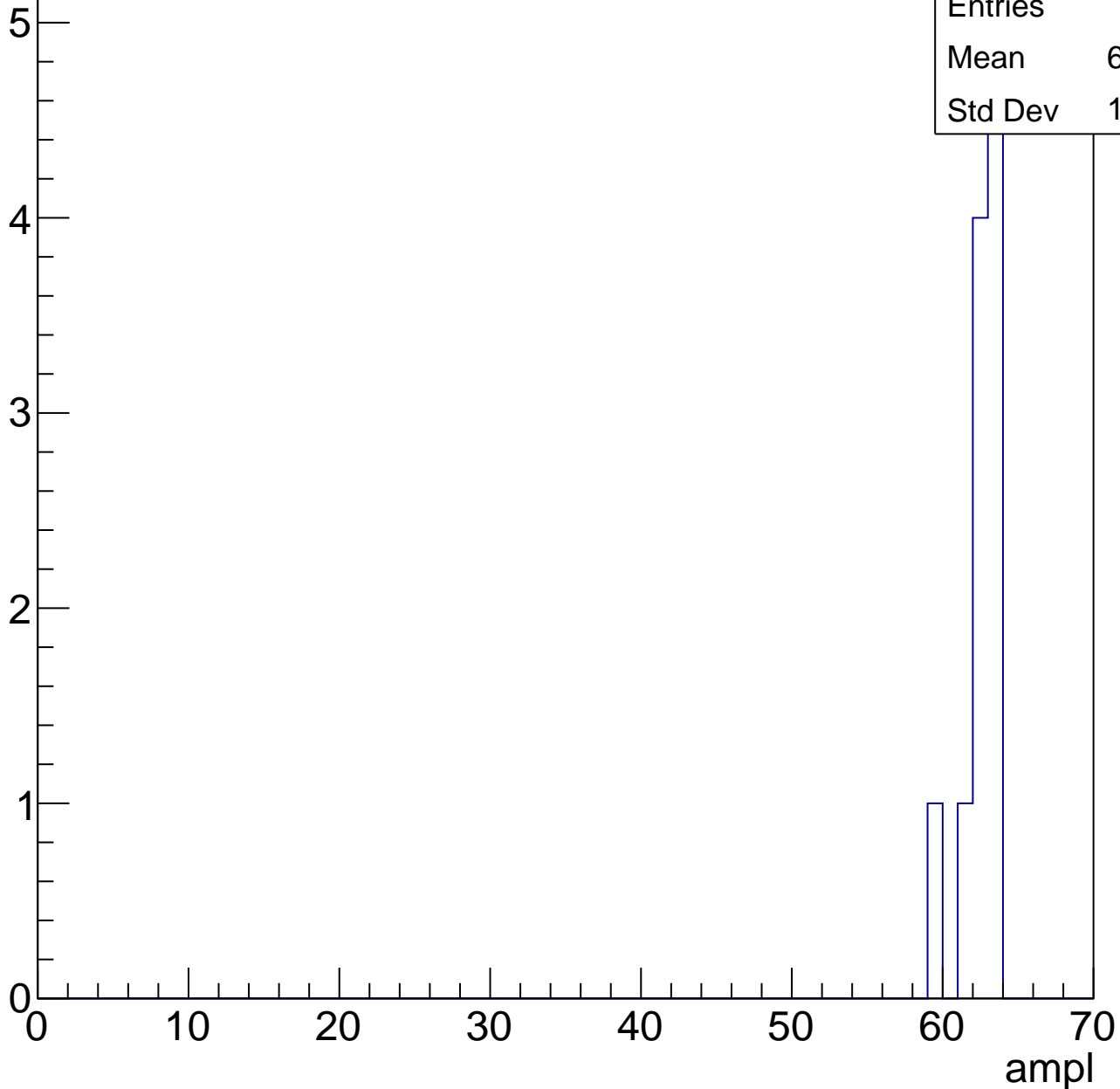


# B1L103S, U26-ch127, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	11
Mean	62.09
Std Dev	1.164



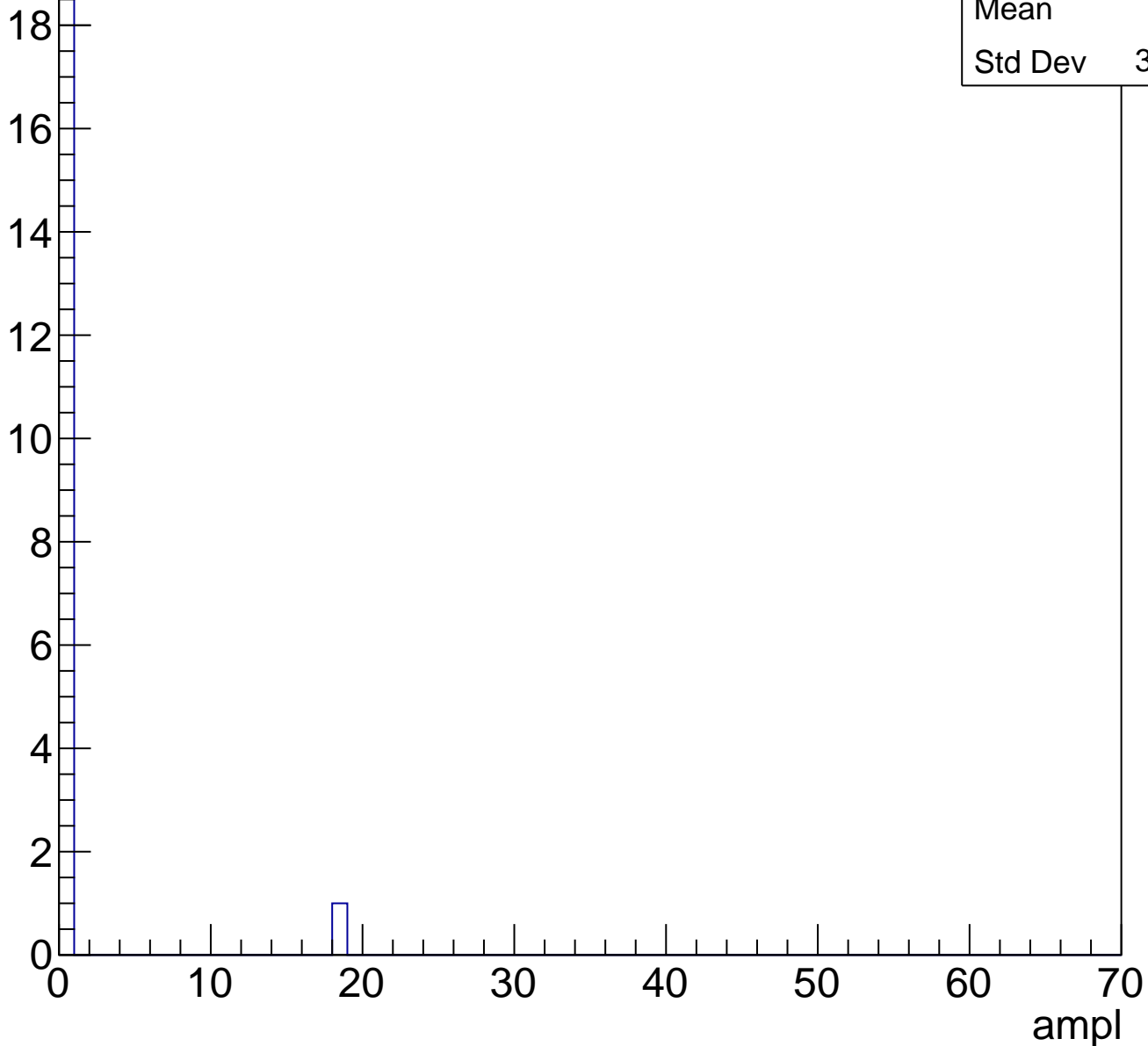


# B1L103S, U26-ch127, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	20
Mean	0.9
Std Dev	3.923

Entry



# B1L103S, U26-ch127, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	20
Mean	0.9
Std Dev	3.923

Entry

