

B1L003S, U4-ch0

calib_packv5_042523_0143.root, FC#13, port D2

Entries	357
Mean	45.48
Std Dev	10.71

Turn on : 28.6346

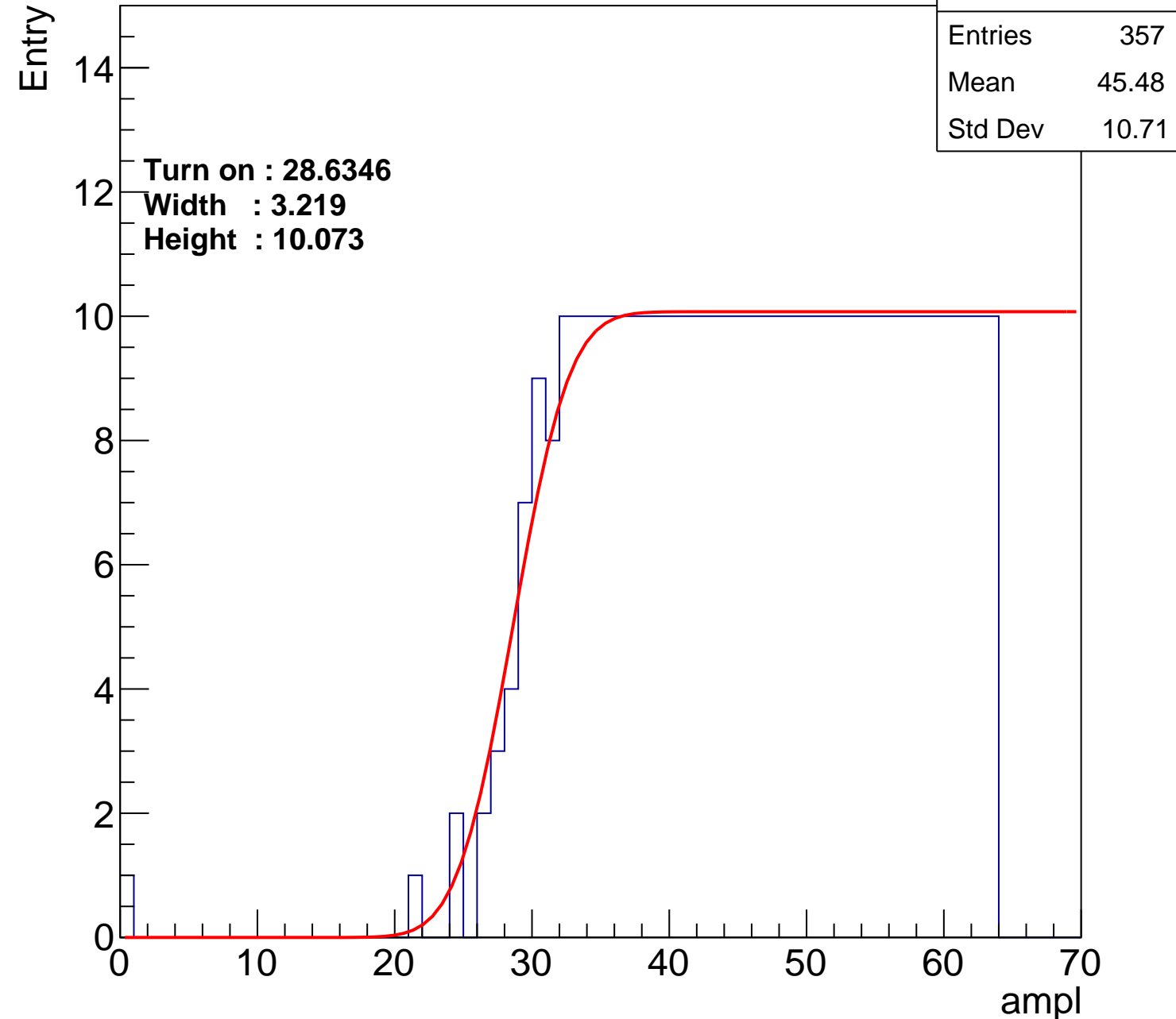
Width : 3.219

Height : 10.073

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U4-ch1

calib_packv5_042523_0143.root, FC#13, port D2

Entries	371
Mean	44.78
Std Dev	11.08

Turn on : 27.1150

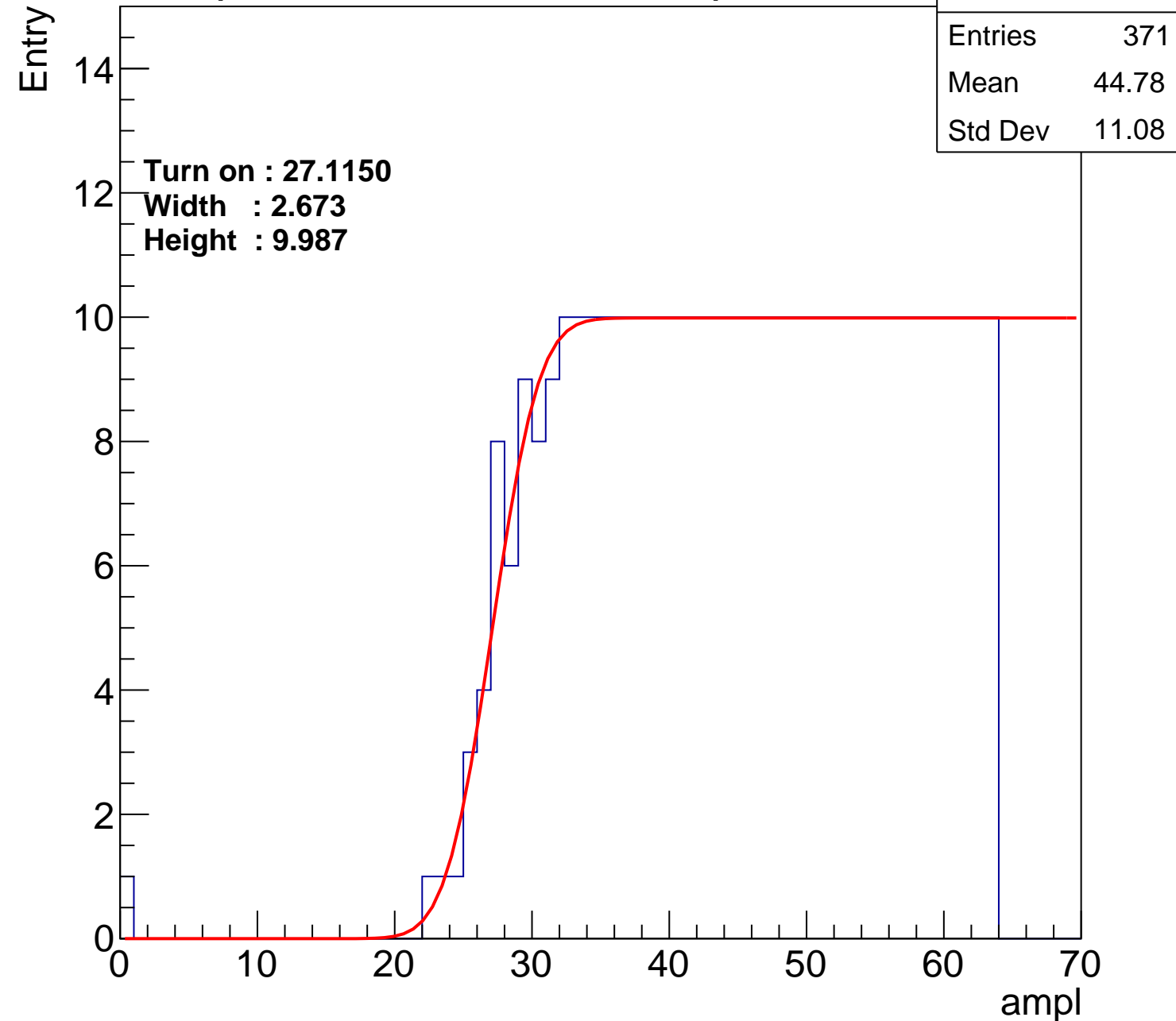
Width : 2.673

Height : 9.987

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U4-ch2

calib_packv5_042523_0143.root, FC#13, port D2

Entries	377
Mean	44.49
Std Dev	11.22

Turn on : 26.8784

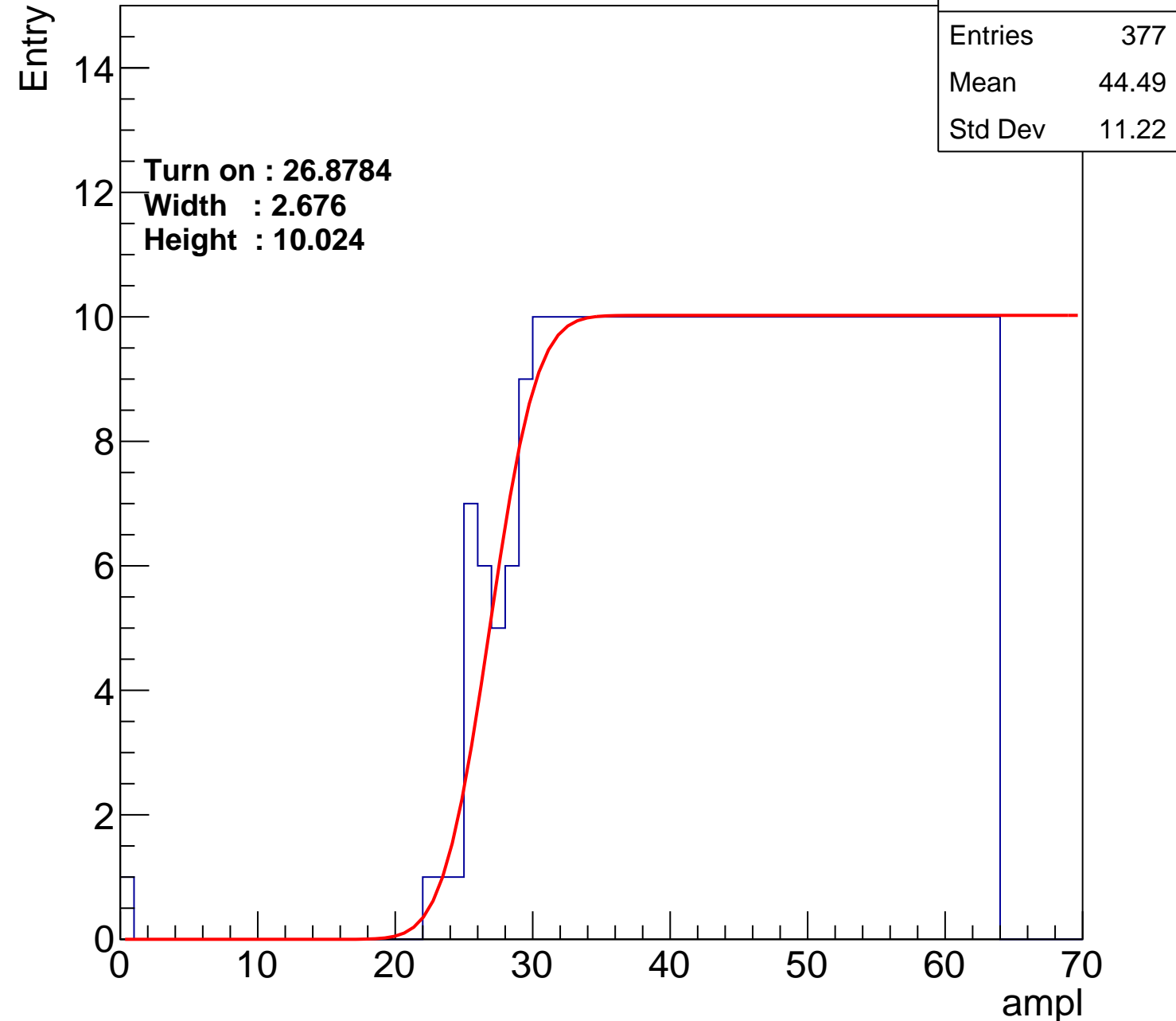
Width : 2.676

Height : 10.024

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U4-ch3

calib_packv5_042523_0143.root, FC#13, port D2

Entries	365
Mean	44.96
Std Dev	11.19

Turn on : 27.7430

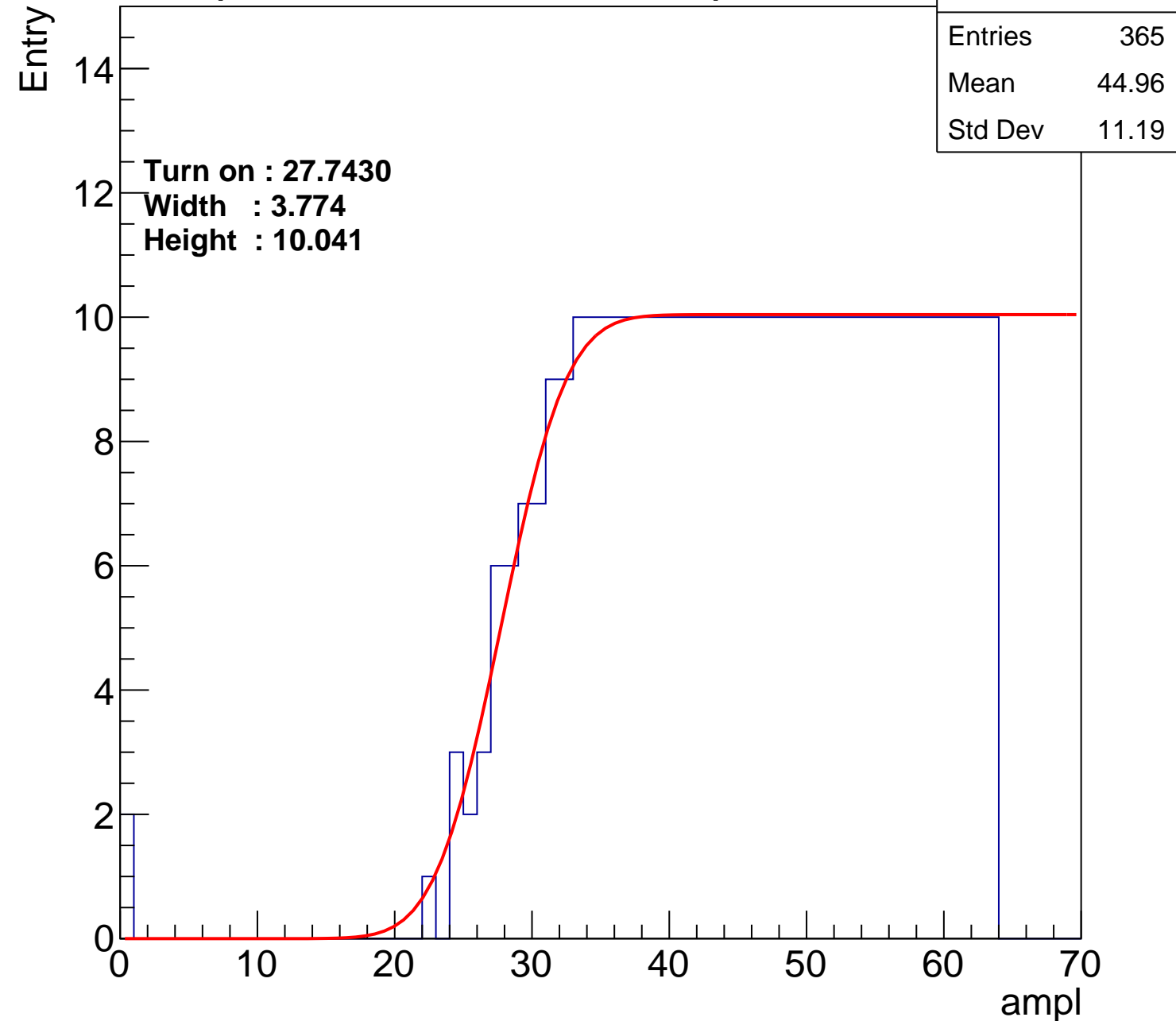
Width : 3.774

Height : 10.041

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U4-ch4

calib_packv5_042523_0143.root, FC#13, port D2

Entries	357
Mean	45.34
Std Dev	11.11

Turn on : 29.0176

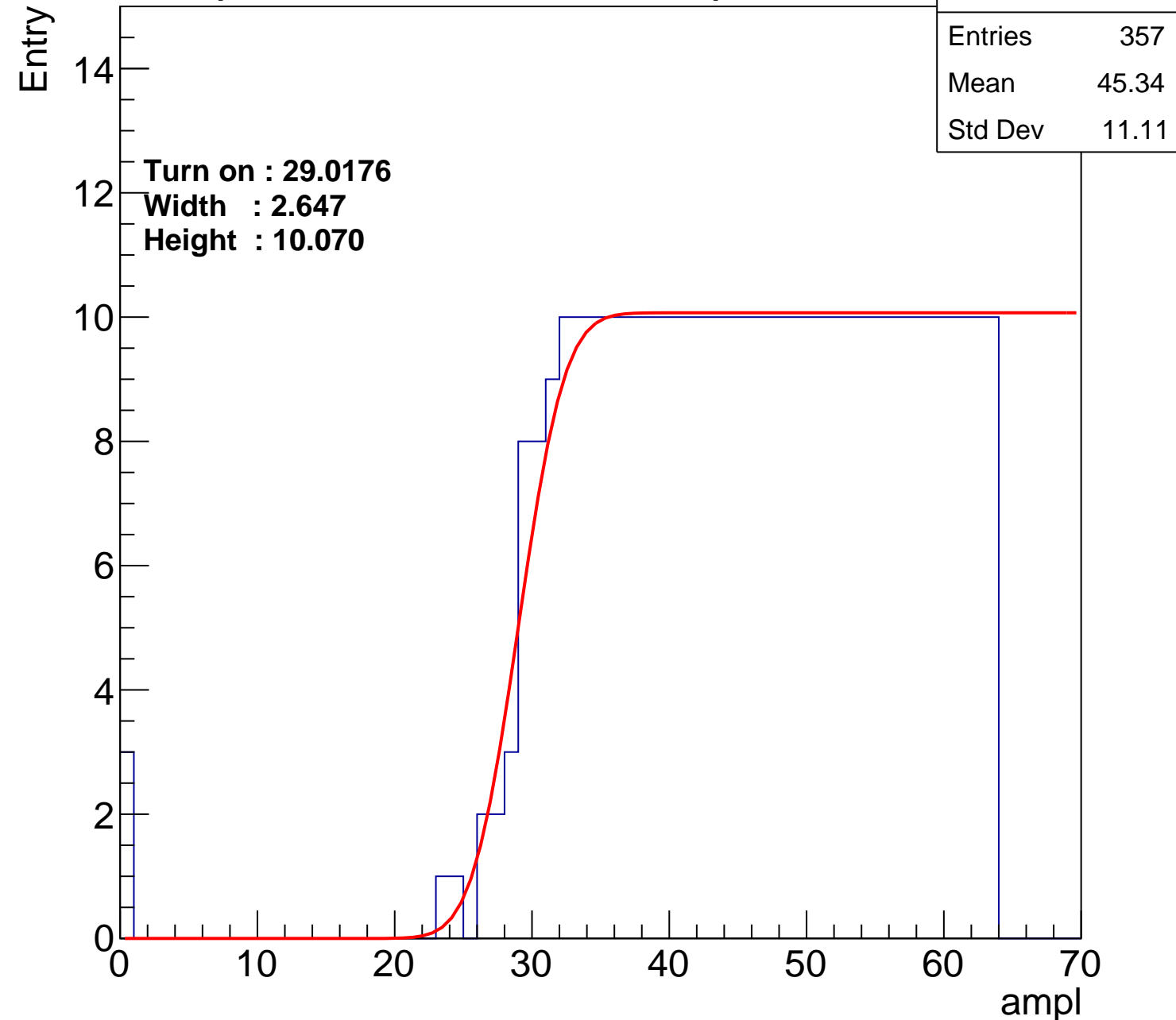
Width : 2.647

Height : 10.070

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U4-ch5

calib_packv5_042523_0143.root, FC#13, port D2

Entries	354
Mean	45.41
Std Dev	11.17

Turn on : 29.2057

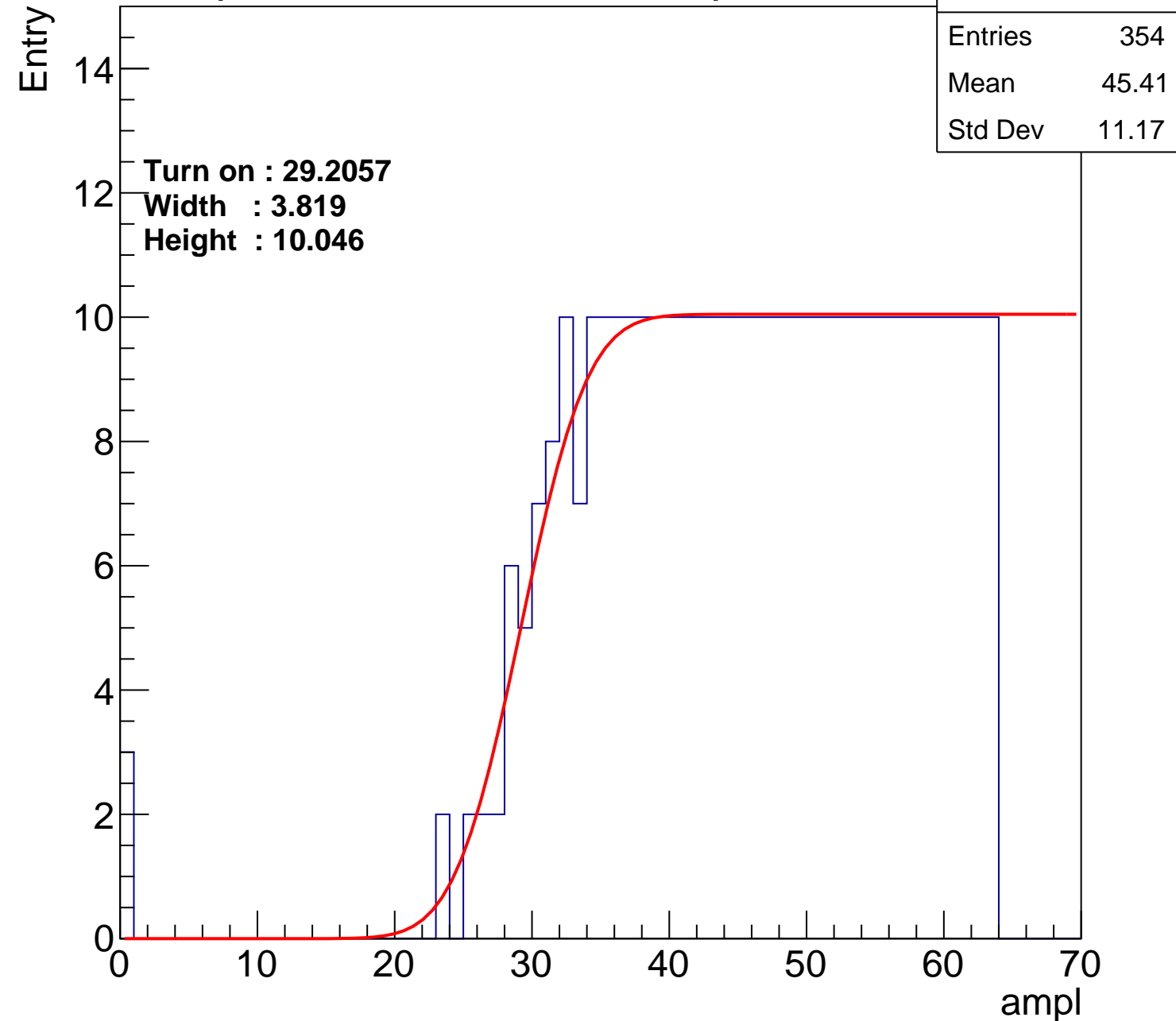
Width : 3.819

Height : 10.046

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U4-ch6

calib_packv5_042523_0143.root, FC#13, port D2

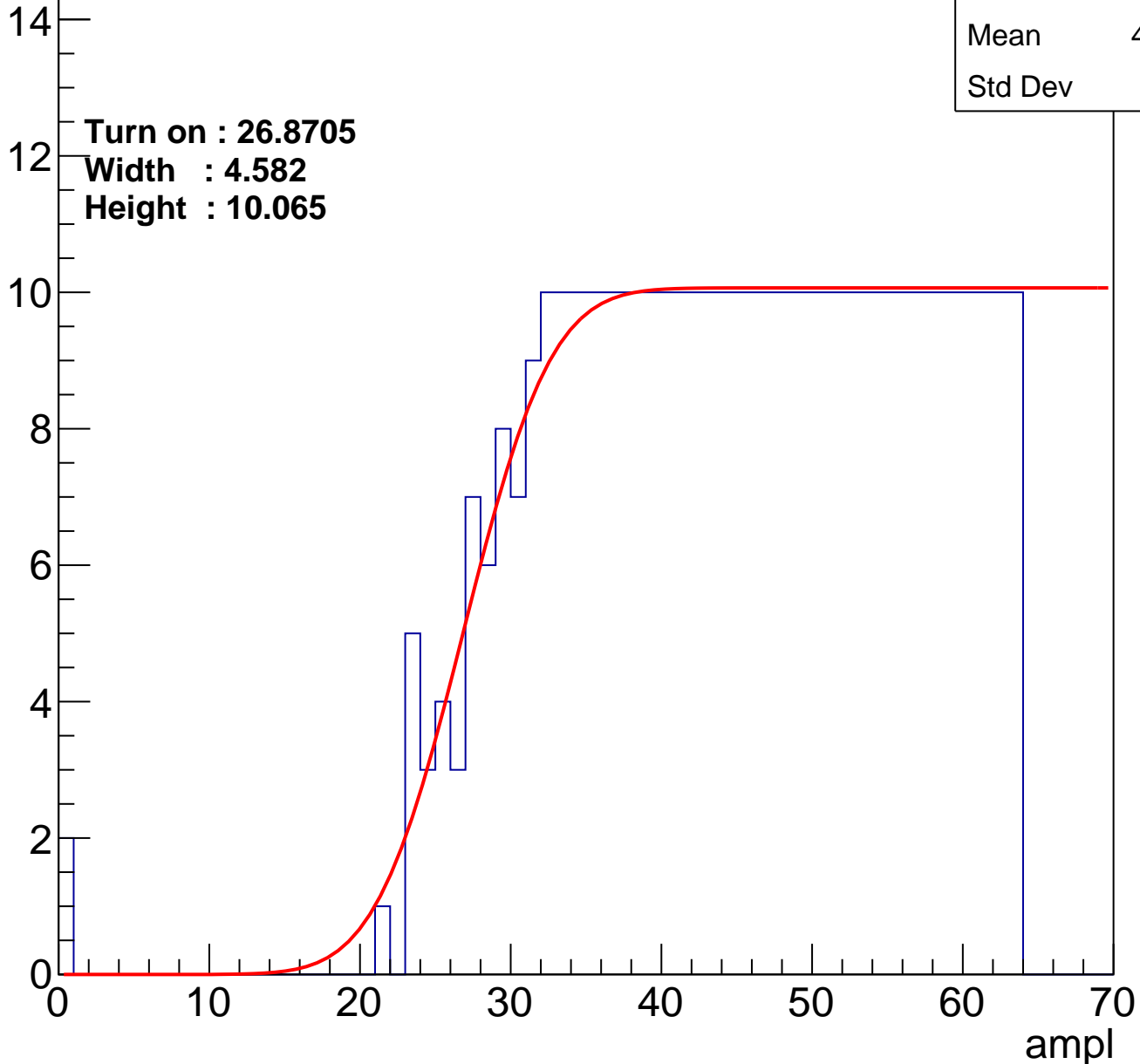
Entries	375
Mean	44.44
Std Dev	11.5

Turn on : 26.8705

Width : 4.582

Height : 10.065

Entry



B1L003S, U4-ch7

calib_packv5_042523_0143.root, FC#13, port D2

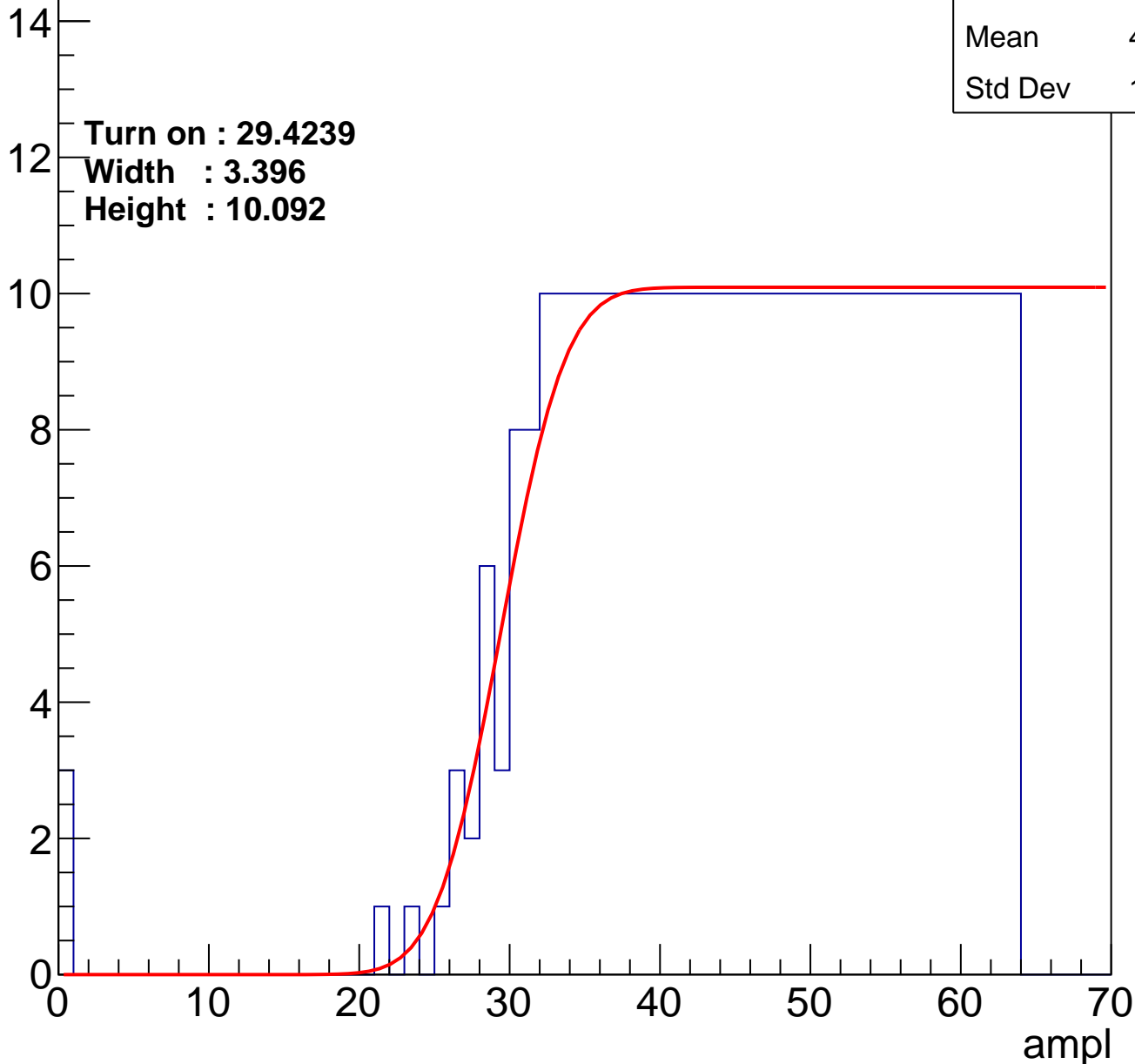
Entry

Entries	356
Mean	45.35
Std Dev	11.16

Turn on : 29.4239

Width : 3.396

Height : 10.092



B1L003S, U4-ch8

calib_packv5_042523_0143.root, FC#13, port D2

Entries	380
Mean	44.13
Std Dev	11.8

Turn on : 26.9946

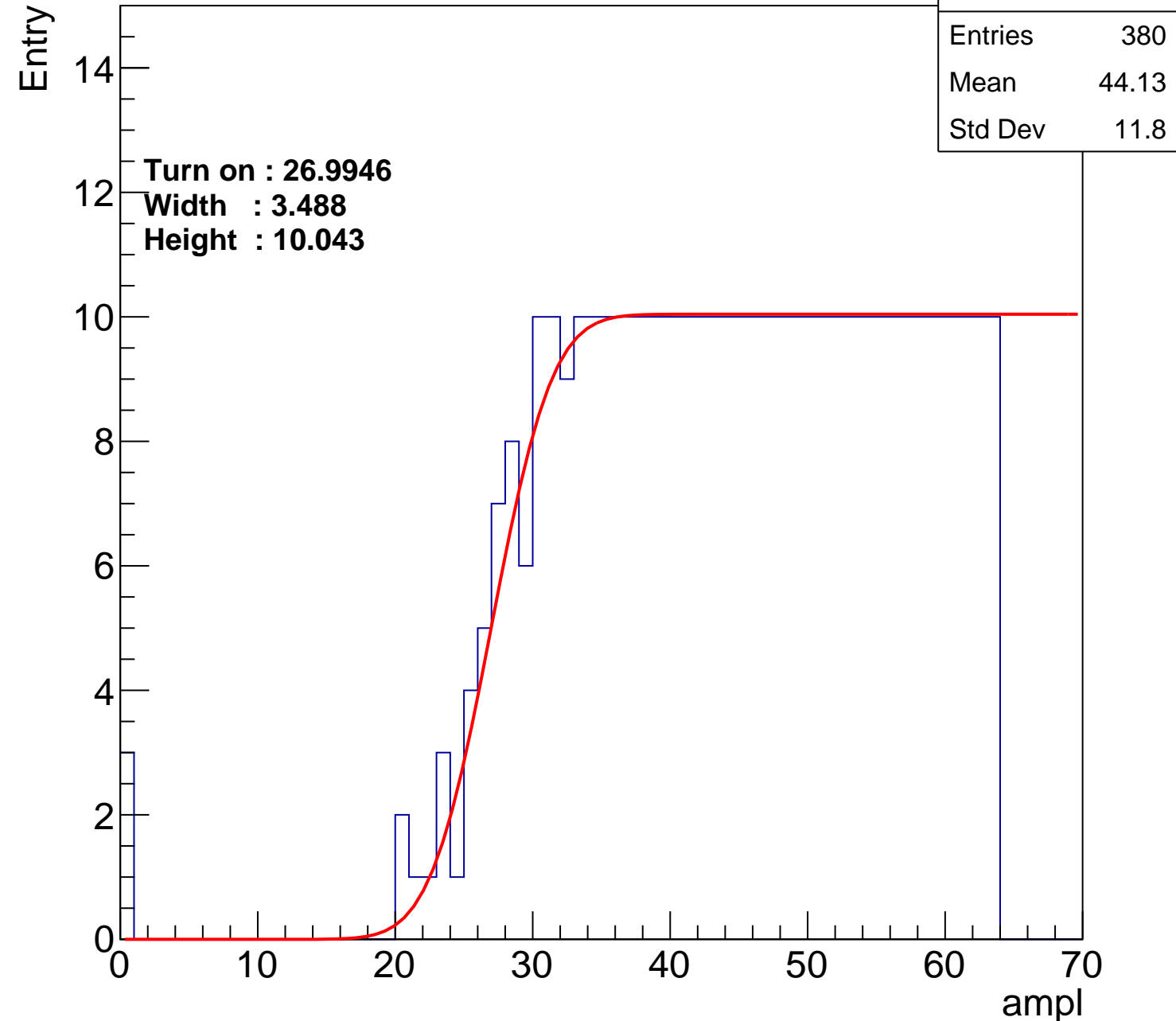
Width : 3.488

Height : 10.043

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U4-ch9

calib_packv5_042523_0143.root, FC#13, port D2

Entries	377
Mean	44.39
Std Dev	11.47

Turn on : 26.8102

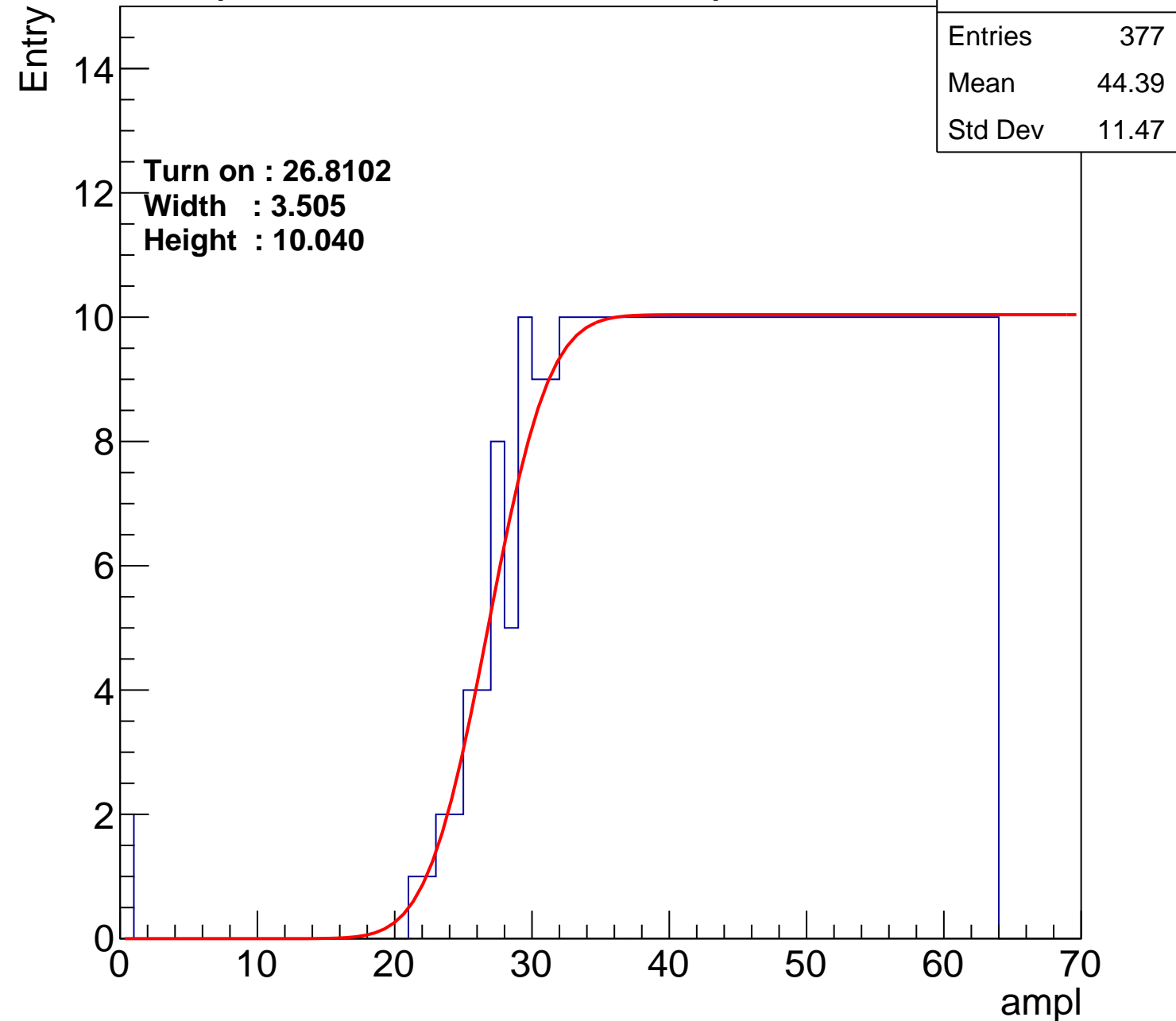
Width : 3.505

Height : 10.040

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U4-ch10

calib_packv5_042523_0143.root, FC#13, port D2

Entries	387
Mean	43.91
Std Dev	11.71

Turn on : 25.8923

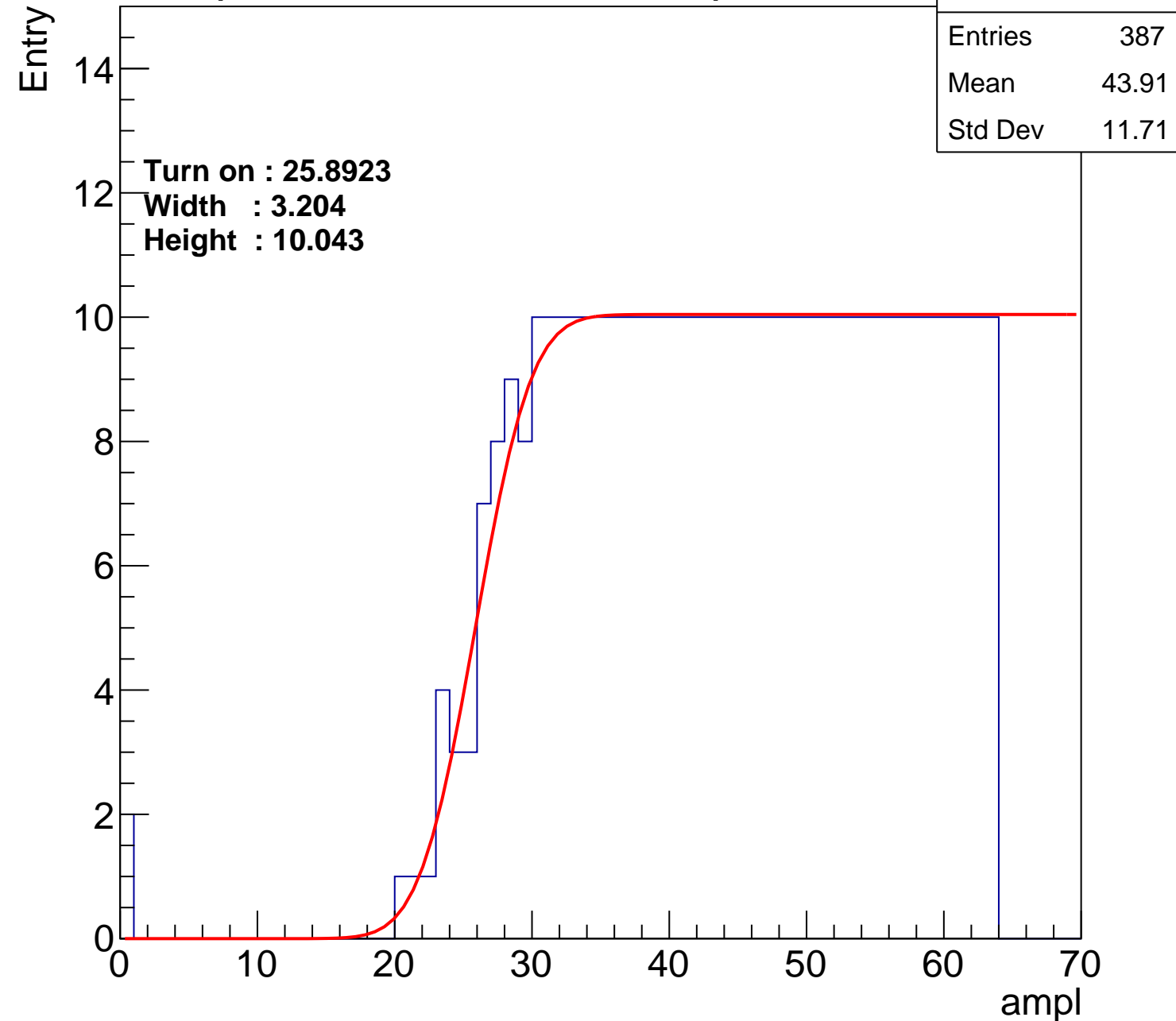
Width : 3.204

Height : 10.043

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U4-ch11

calib_packv5_042523_0143.root, FC#13, port D2

Entries	381
Mean	44.08
Std Dev	11.9

Turn on : 26.5951

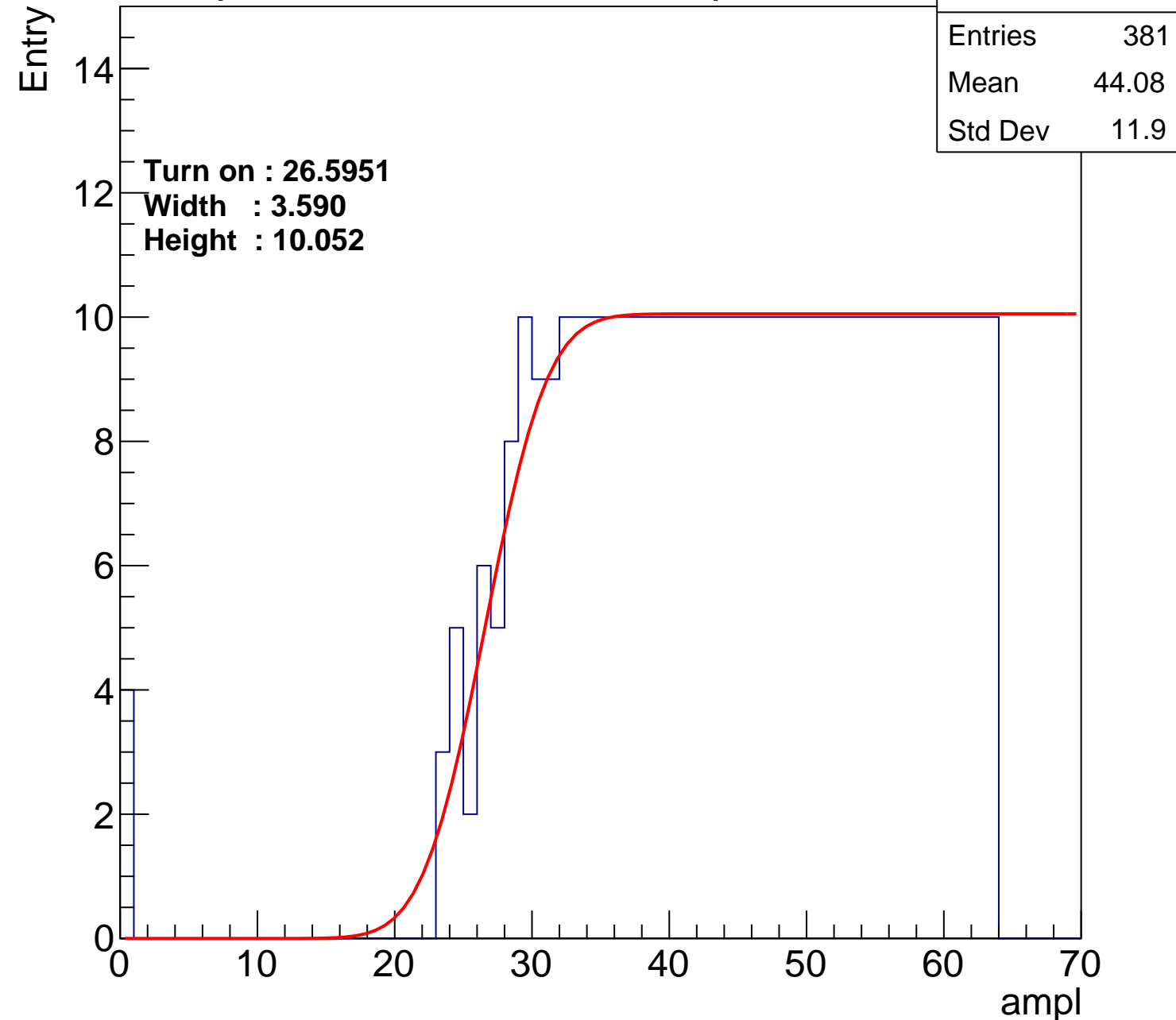
Width : 3.590

Height : 10.052

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U4-ch12

calib_packv5_042523_0143.root, FC#13, port D2

Entries	369
Mean	44.58
Std Dev	11.83

Turn on : 28.1931

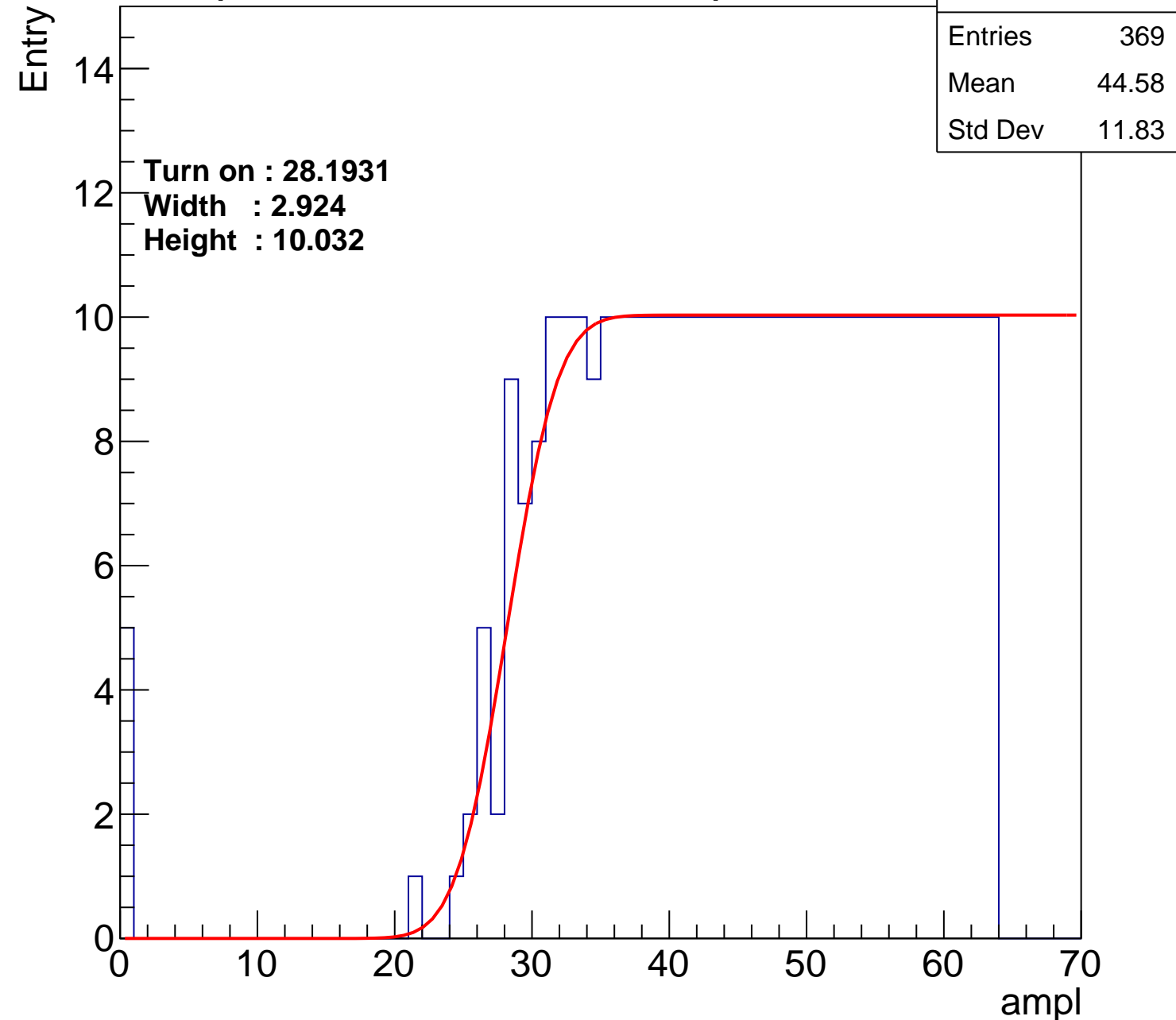
Width : 2.924

Height : 10.032

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U4-ch13

calib_packv5_042523_0143.root, FC#13, port D2

Entries	372
Mean	44.49
Std Dev	11.81

Turn on : 27.2615

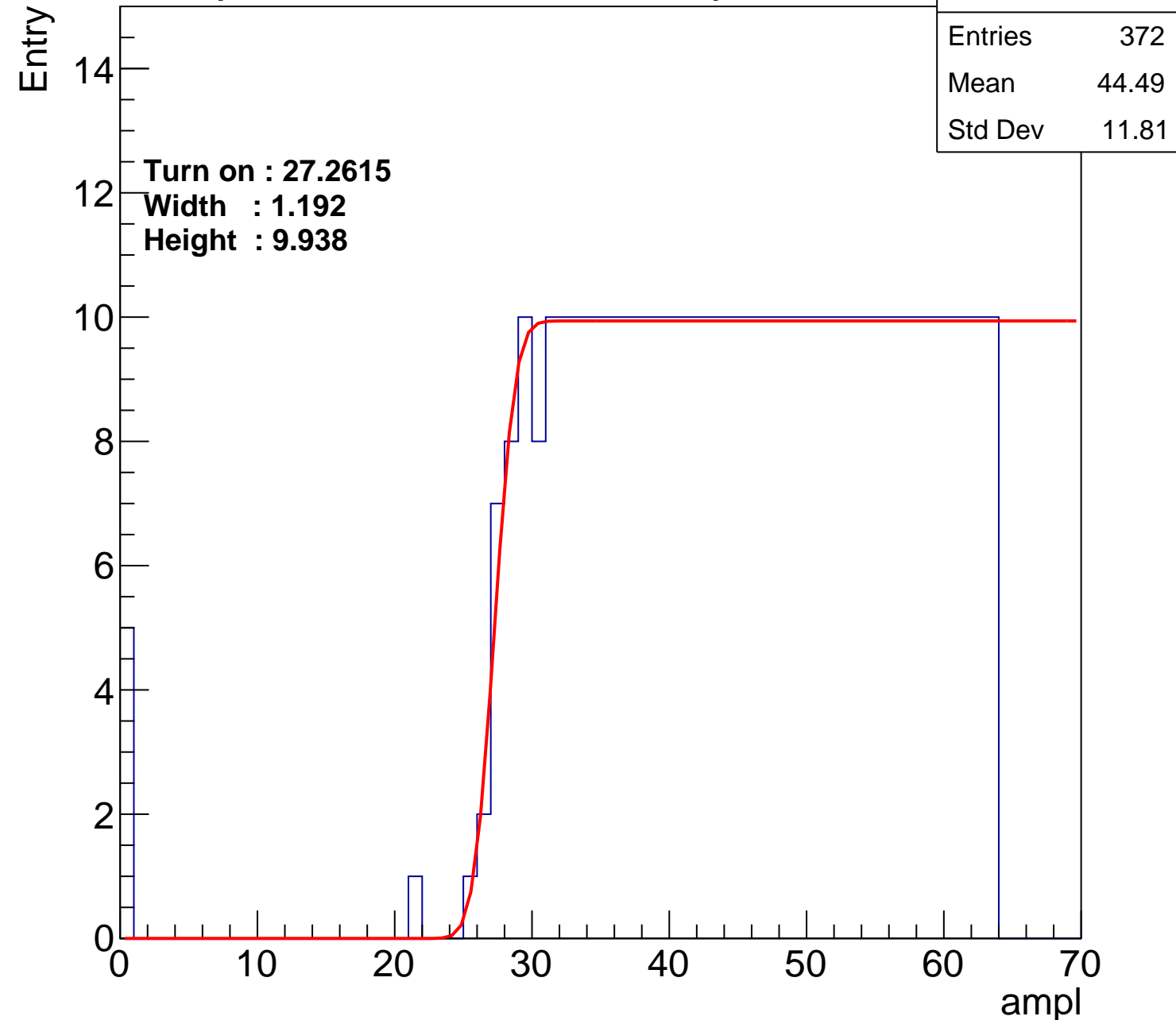
Width : 1.192

Height : 9.938

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U4-ch14

calib_packv5_042523_0143.root, FC#13, port D2

Entries	364
Mean	44.93
Std Dev	11.39

Turn on : 27.9752

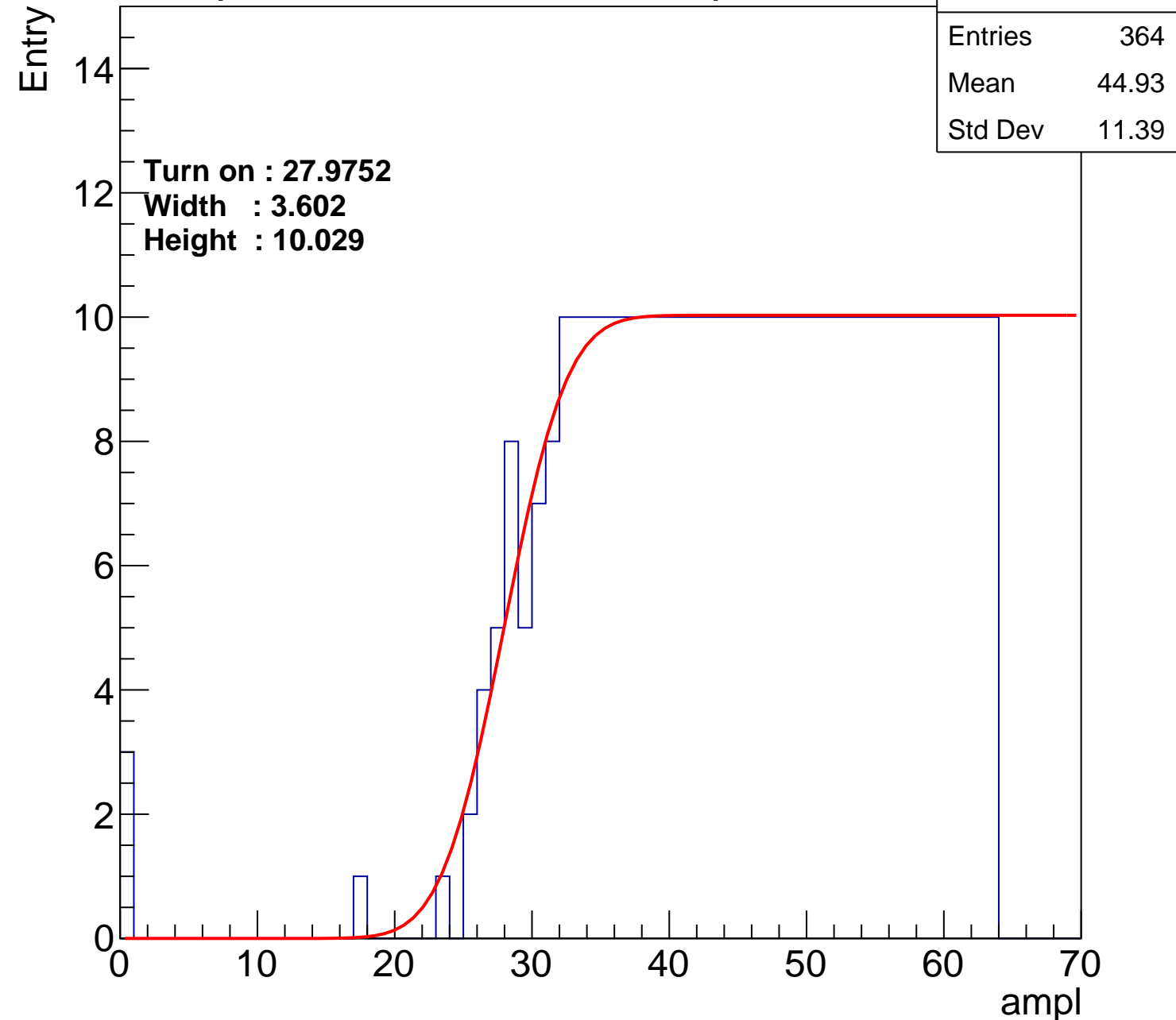
Width : 3.602

Height : 10.029

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U4-ch15

calib_packv5_042523_0143.root, FC#13, port D2

Entries	343
Mean	46.04
Std Dev	10.66

Turn on : 30.2716

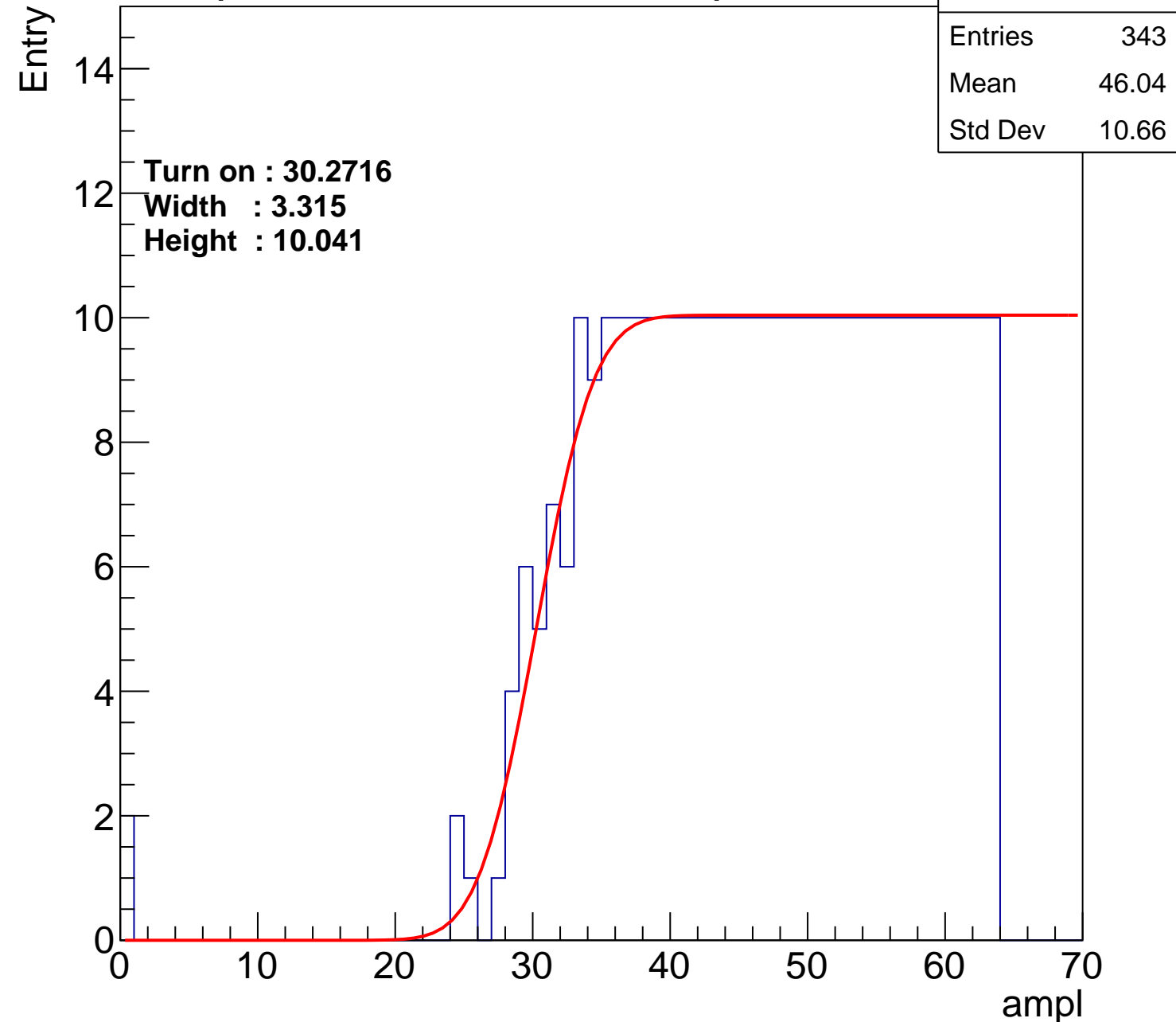
Width : 3.315

Height : 10.041

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U4-ch16

calib_packv5_042523_0143.root, FC#13, port D2

Entries	370
Mean	44.58
Std Dev	11.69

Turn on : 27.1520

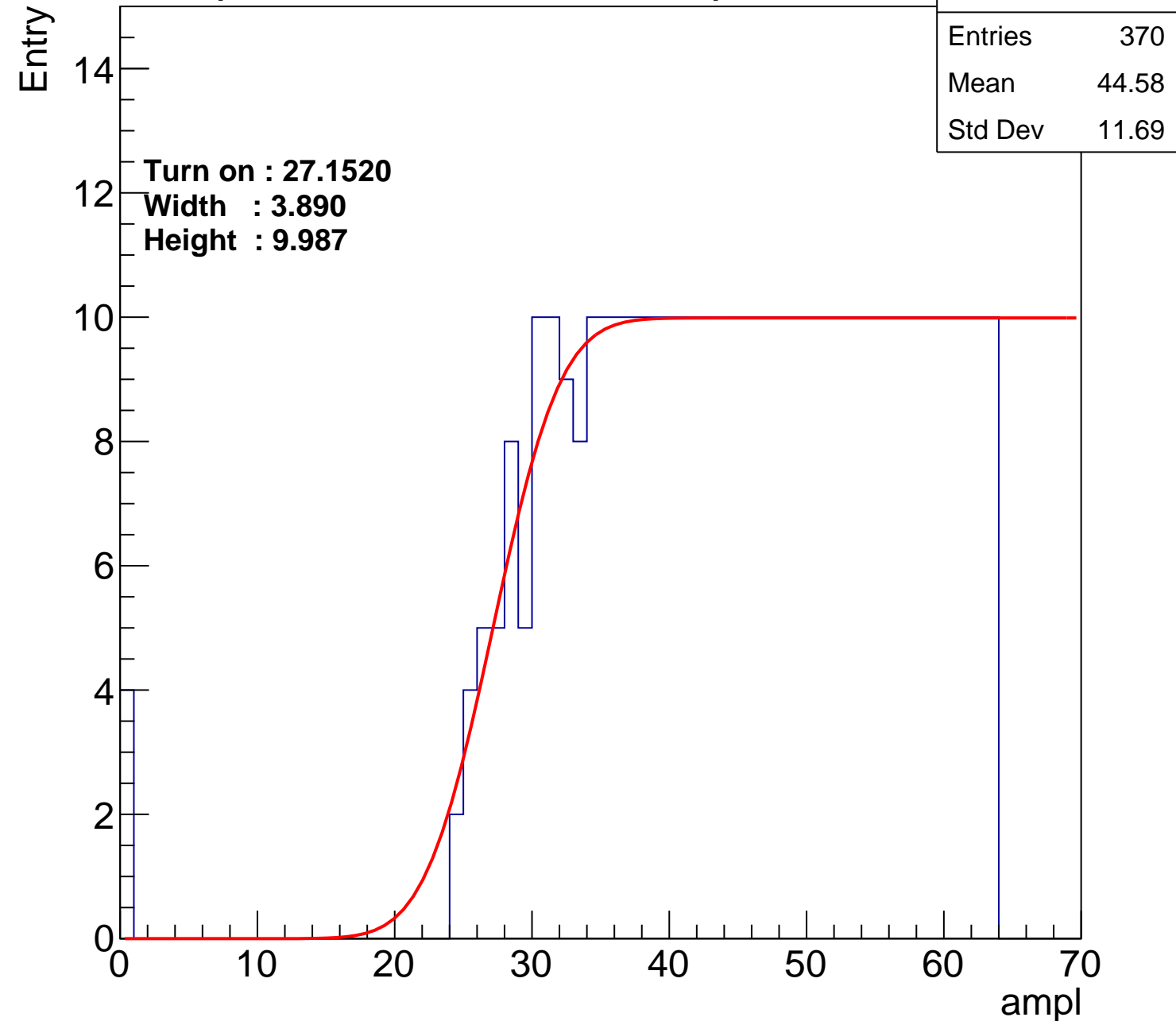
Width : 3.890

Height : 9.987

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U4-ch17

calib_packv5_042523_0143.root, FC#13, port D2

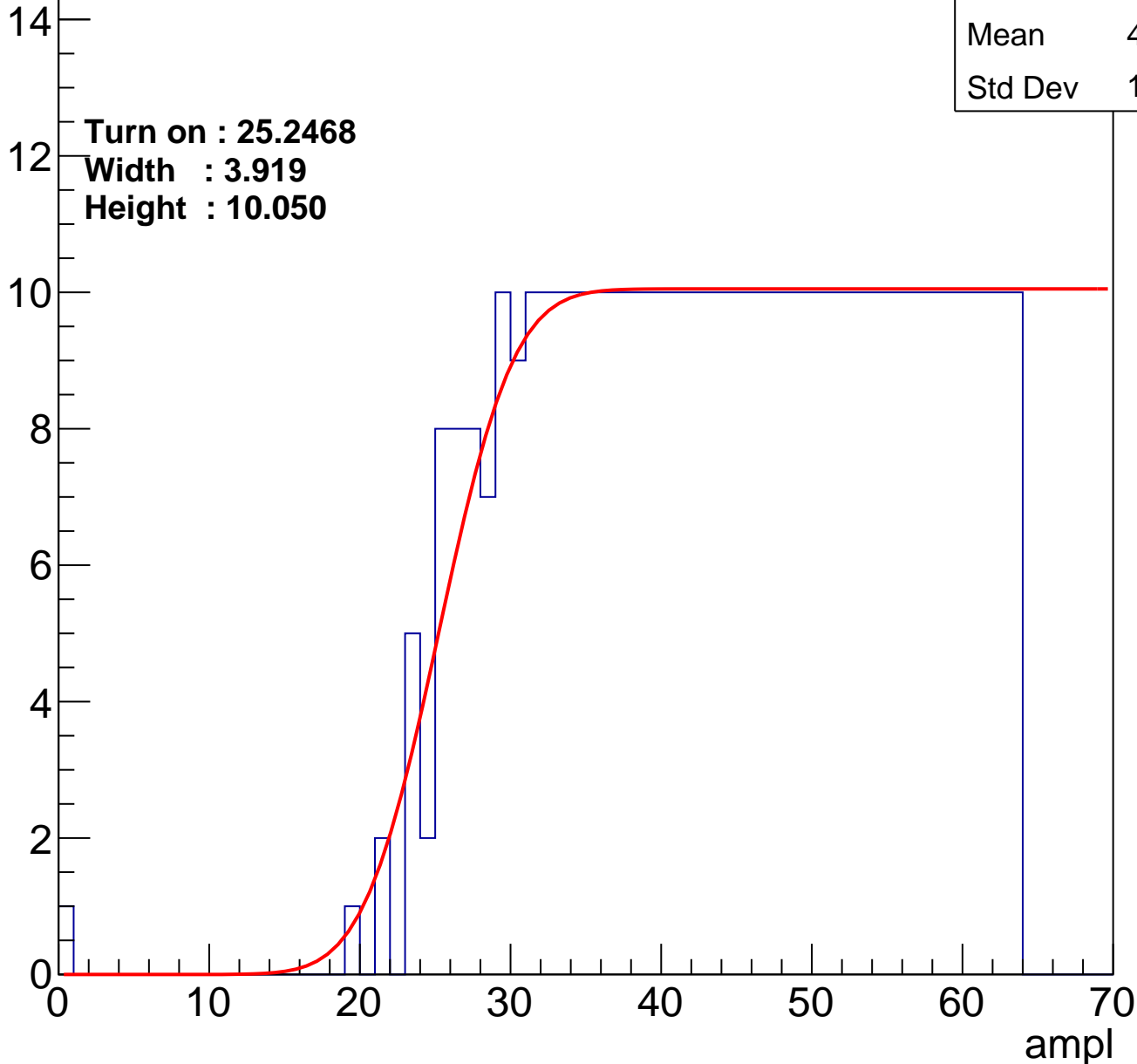
Entries	391
Mean	43.77
Std Dev	11.65

Turn on : 25.2468

Width : 3.919

Height : 10.050

Entry



B1L003S, U4-ch18

calib_packv5_042523_0143.root, FC#13, port D2

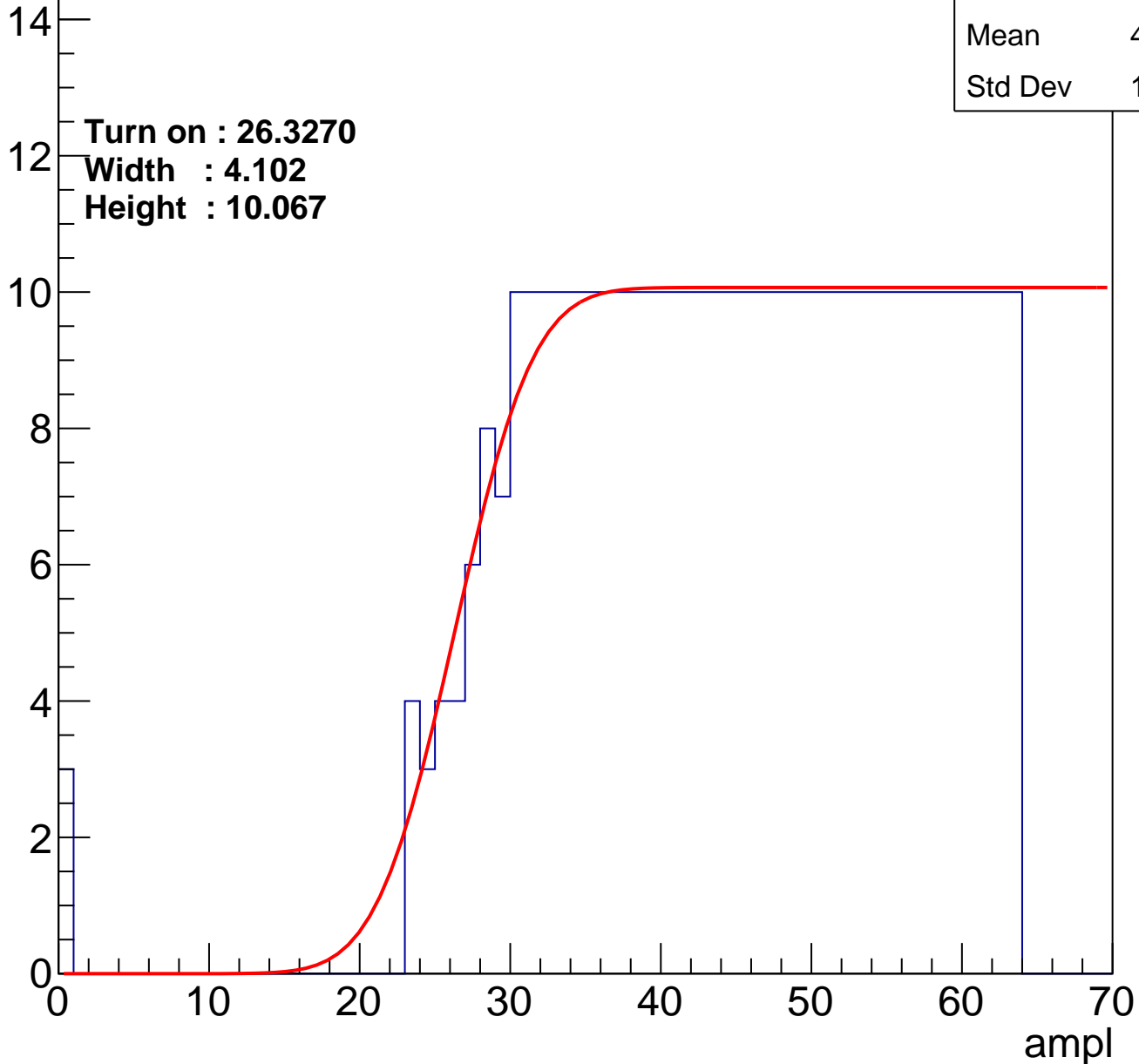
Entries	379
Mean	44.24
Std Dev	11.68

Turn on : 26.3270

Width : 4.102

Height : 10.067

Entry



B1L003S, U4-ch19

calib_packv5_042523_0143.root, FC#13, port D2

Entries	377
Mean	44.13
Std Dev	12.17

Turn on : 27.0640

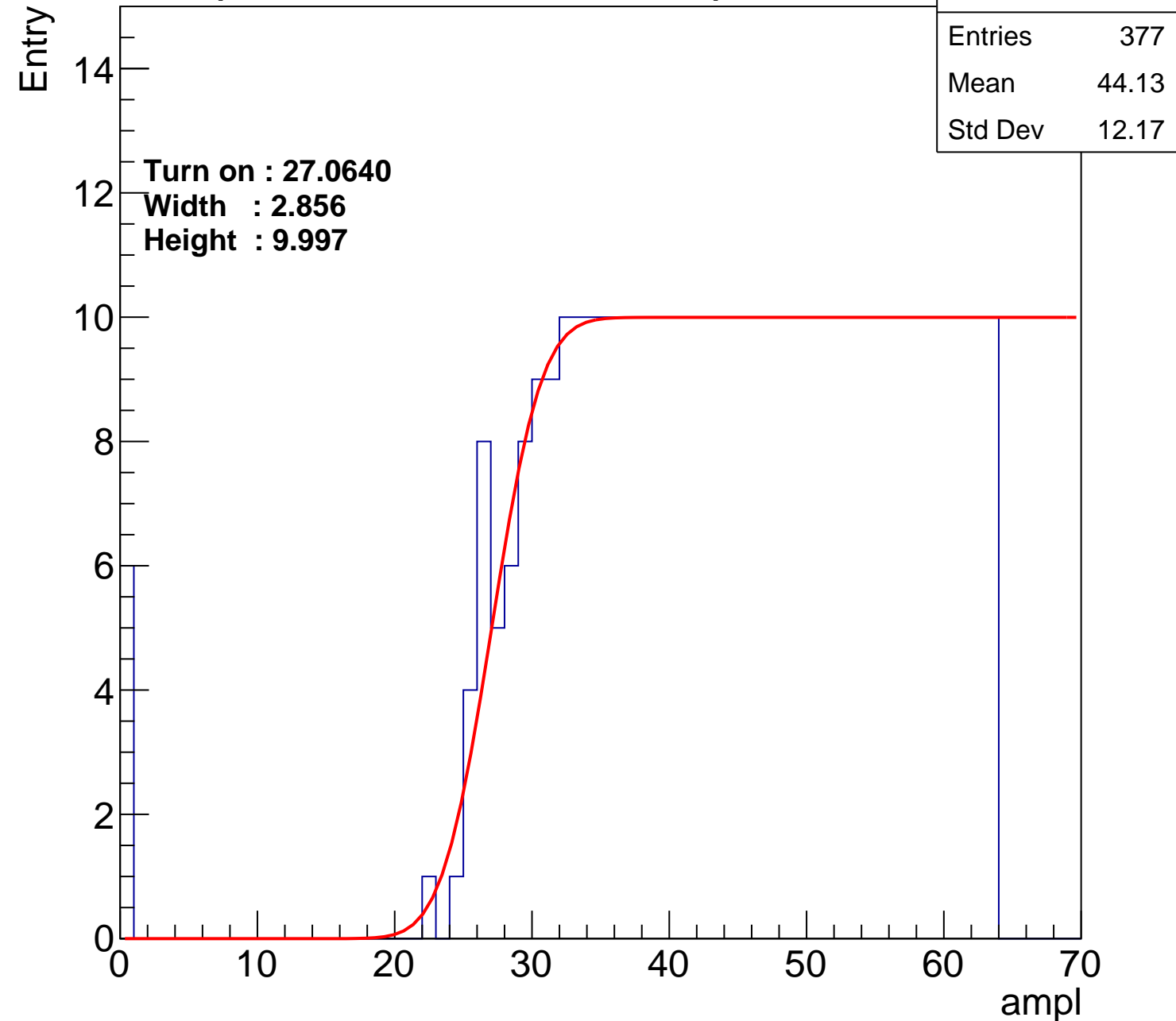
Width : 2.856

Height : 9.997

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U4-ch20

calib_packv5_042523_0143.root, FC#13, port D2

Entries	370
Mean	44.53
Std Dev	11.86

Turn on : 28.0419

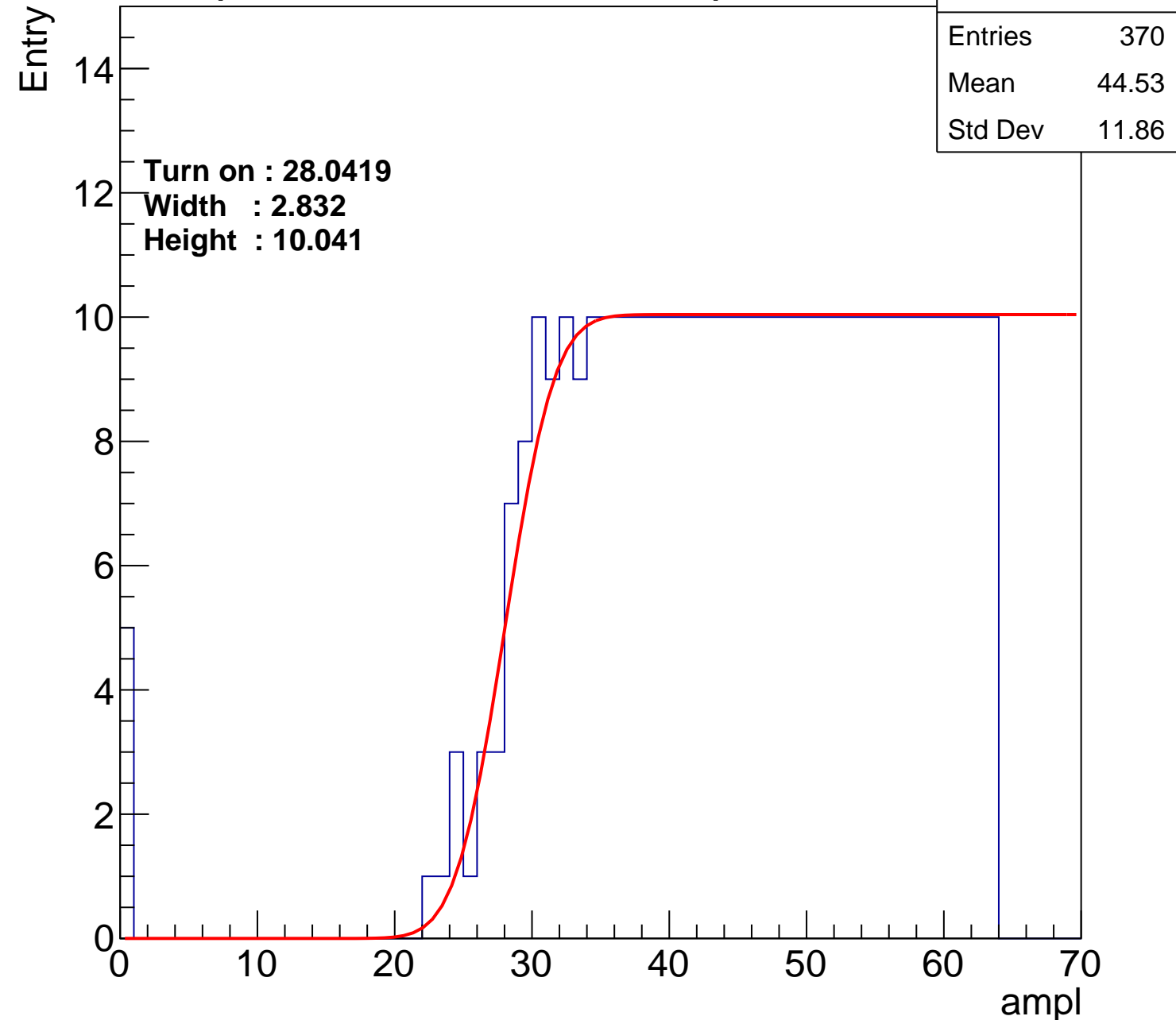
Width : 2.832

Height : 10.041

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U4-ch21

calib_packv5_042523_0143.root, FC#13, port D2

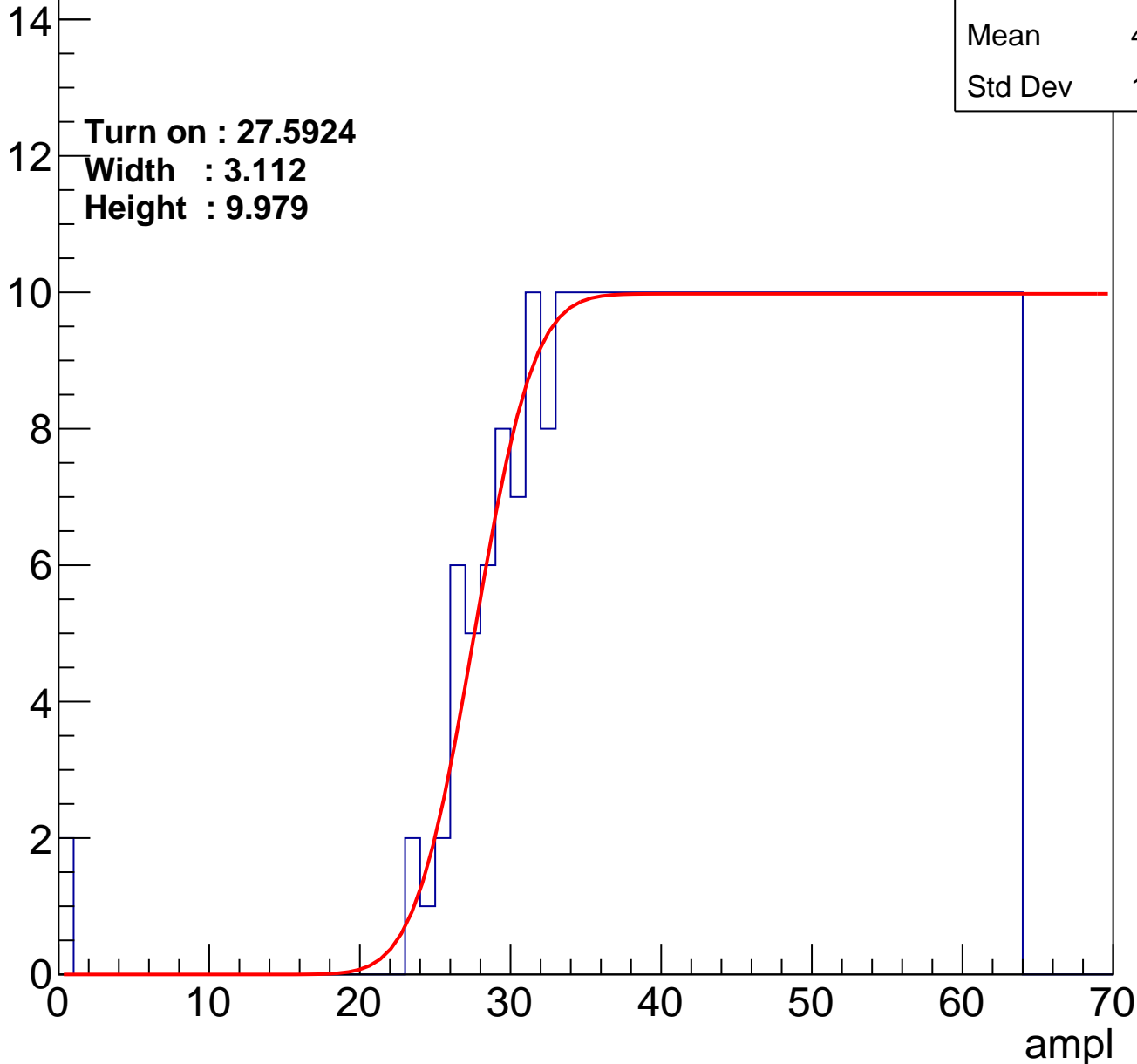
Entries	367
Mean	44.87
Std Dev	11.23

Turn on : 27.5924

Width : 3.112

Height : 9.979

Entry



B1L003S, U4-ch22

calib_packv5_042523_0143.root, FC#13, port D2

Entries	394
Mean	43.44
Std Dev	12.21

Turn on : 25.6021

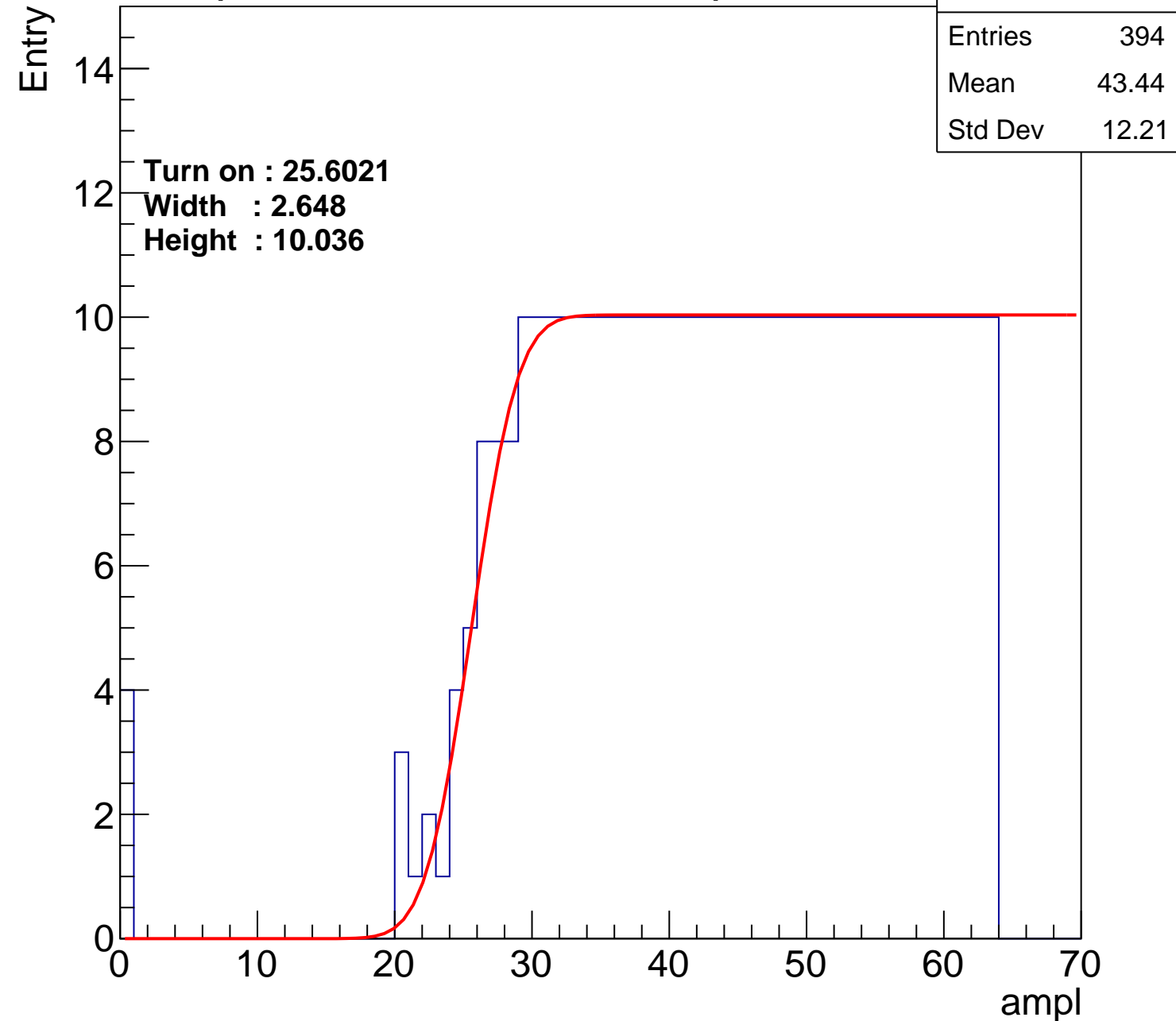
Width : 2.648

Height : 10.036

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U4-ch23

calib_packv5_042523_0143.root, FC#13, port D2

Entries	379
Mean	44.04
Std Dev	12.21

Turn on : 27.1972

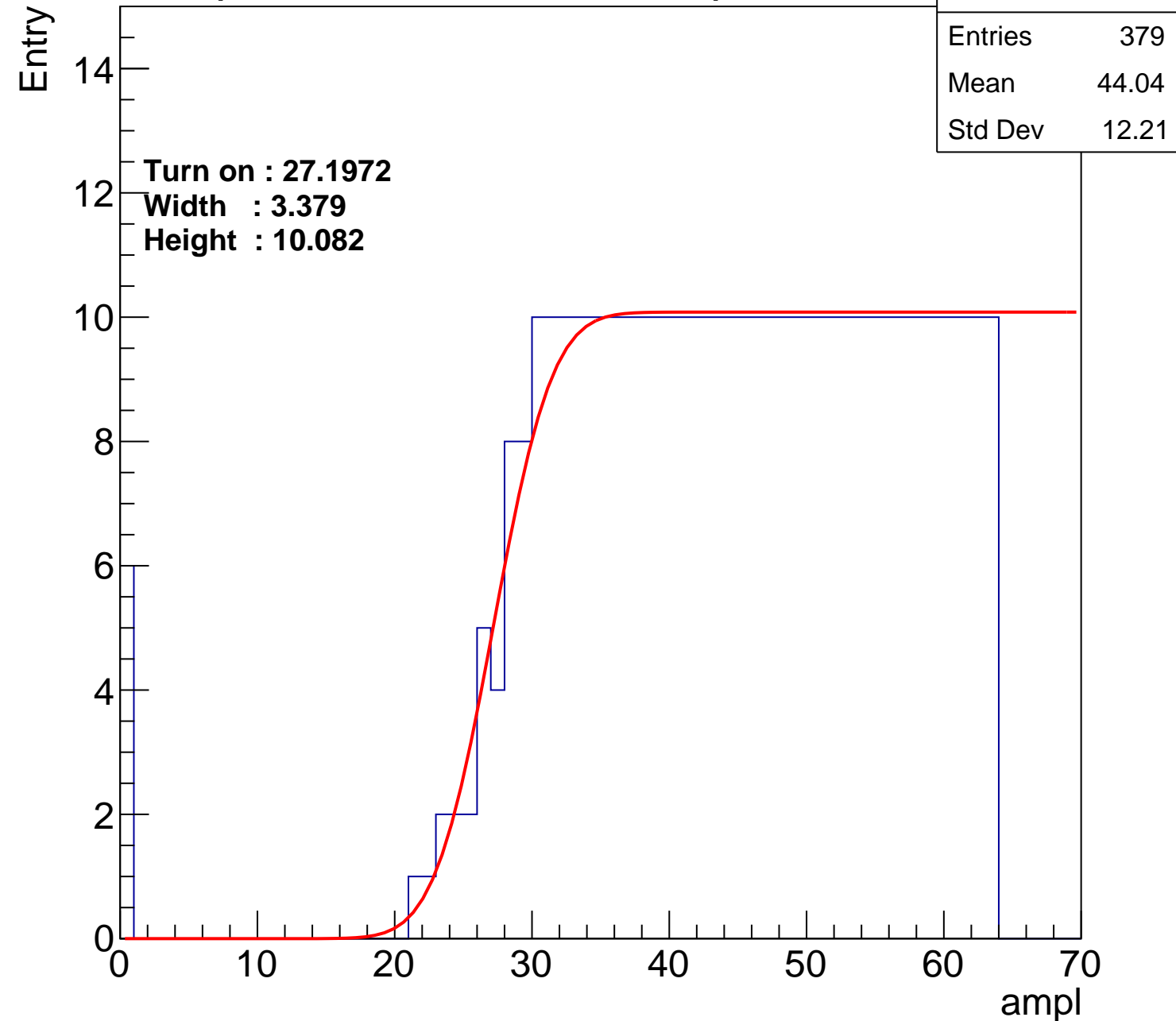
Width : 3.379

Height : 10.082

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U4-ch24

calib_packv5_042523_0143.root, FC#13, port D2

Entries	395
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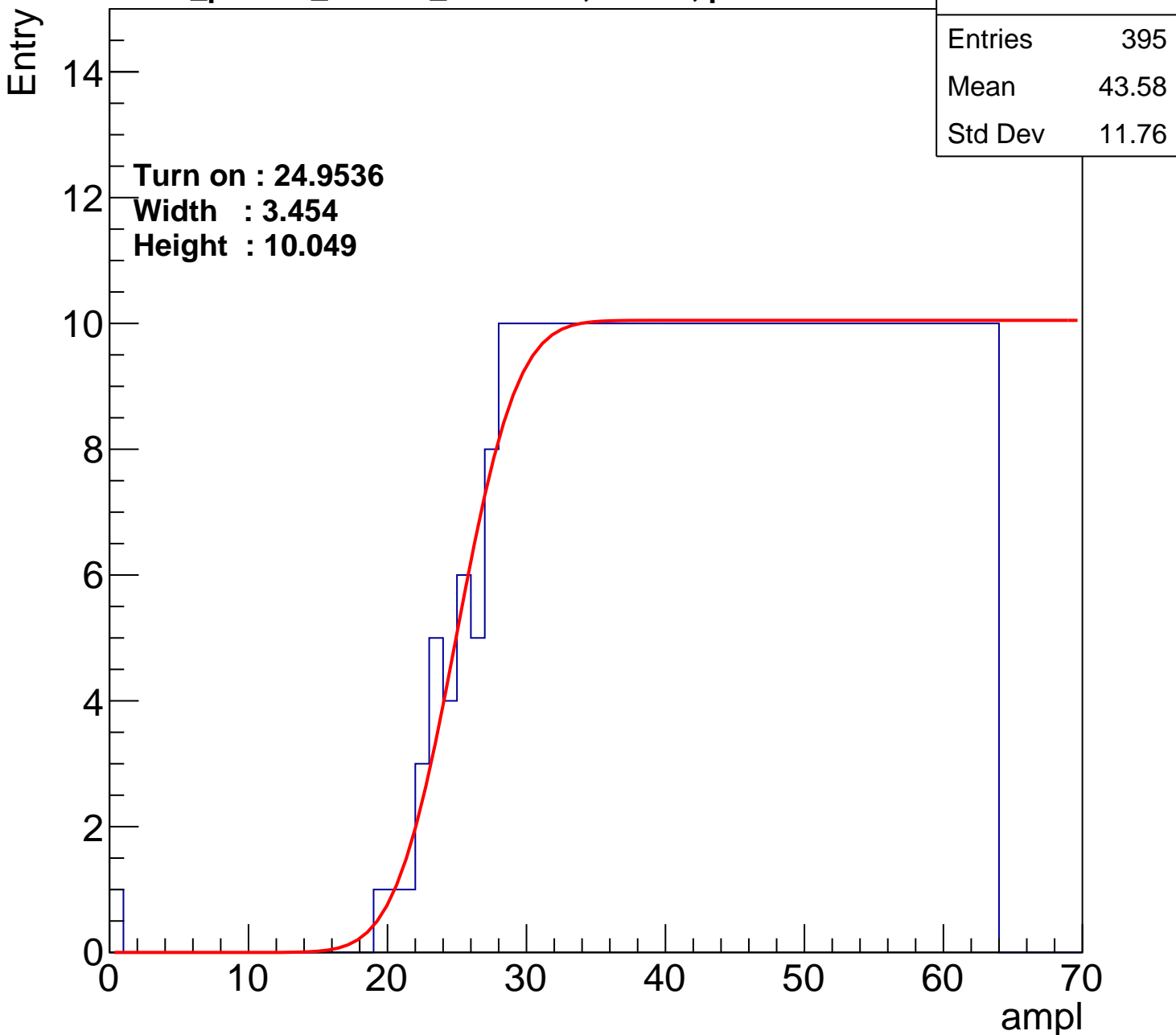
Mean	43.58
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Std Dev	11.76
---------	-------

Turn on : 24.9536

Width : 3.454

Height : 10.049



B1L003S, U4-ch25

calib_packv5_042523_0143.root, FC#13, port D2

Entries	354
Mean	45.55
Std Dev	10.85

Turn on : 30.0757

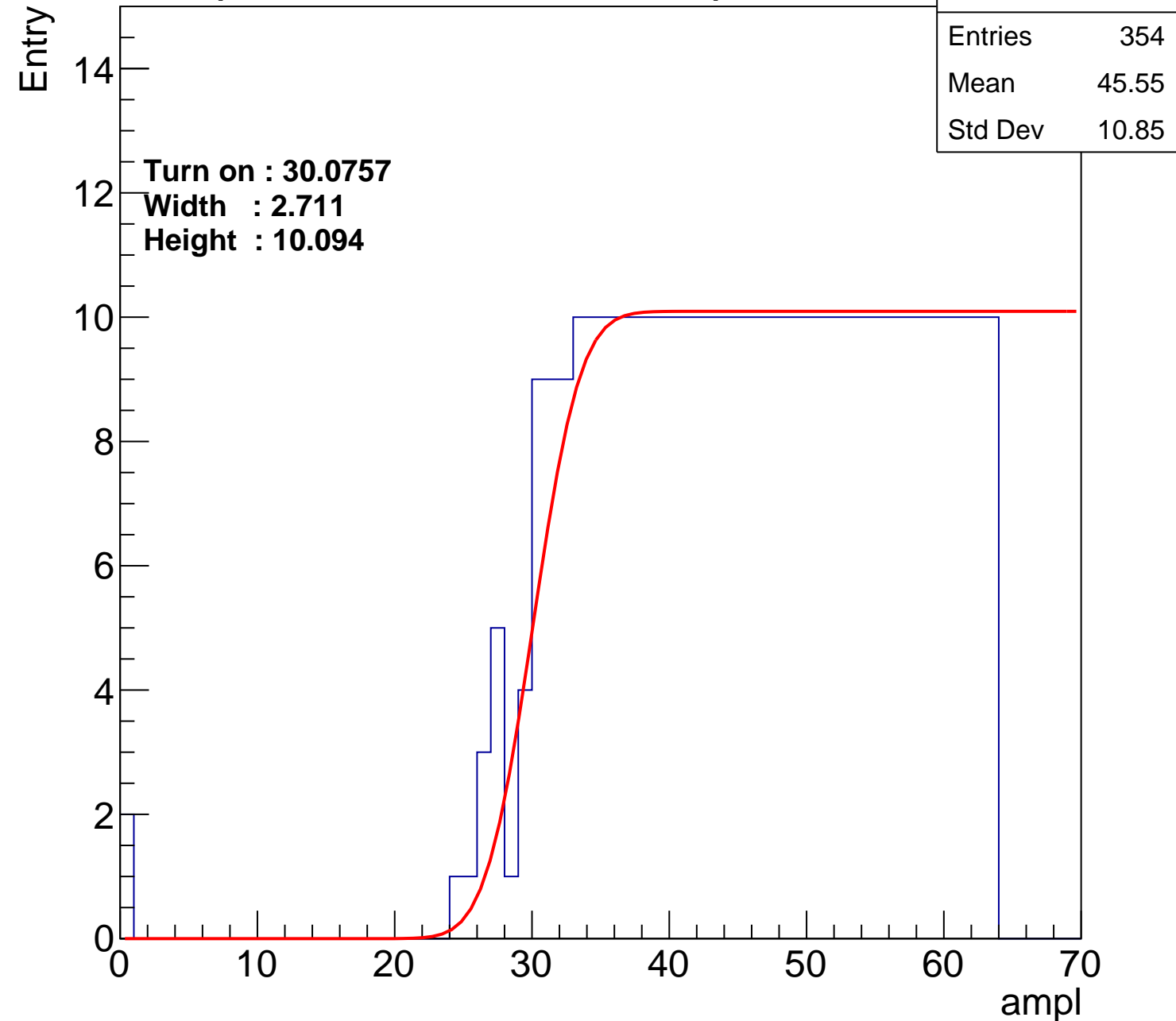
Width : 2.711

Height : 10.094

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U4-ch26

calib_packv5_042523_0143.root, FC#13, port D2

Entries	372
Mean	44.72
Std Dev	11.12

Turn on : 26.8817

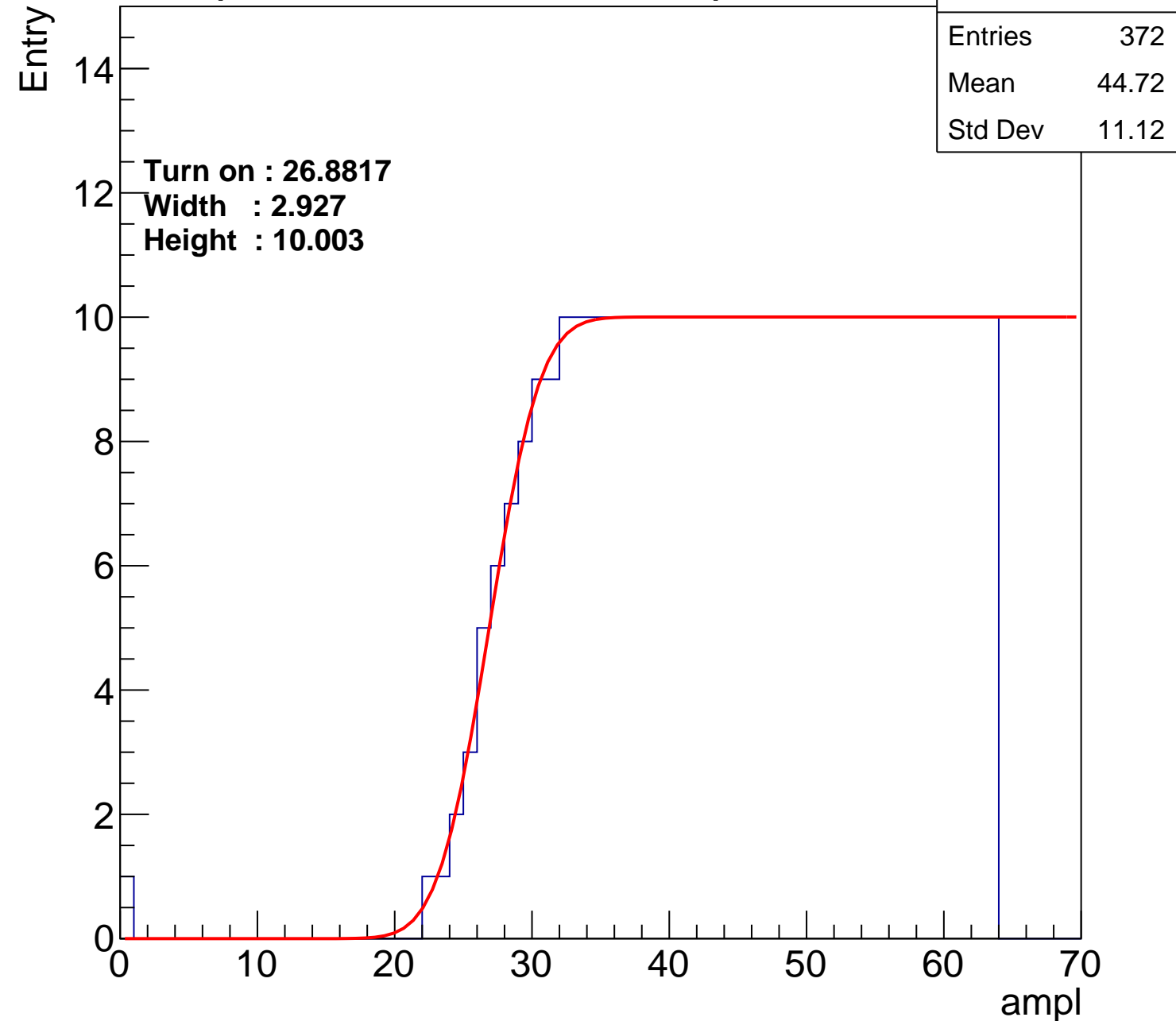
Width : 2.927

Height : 10.003

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U4-ch27

calib_packv5_042523_0143.root, FC#13, port D2

Entries	384
Mean	43.92
Std Dev	11.99

Turn on : 26.0921

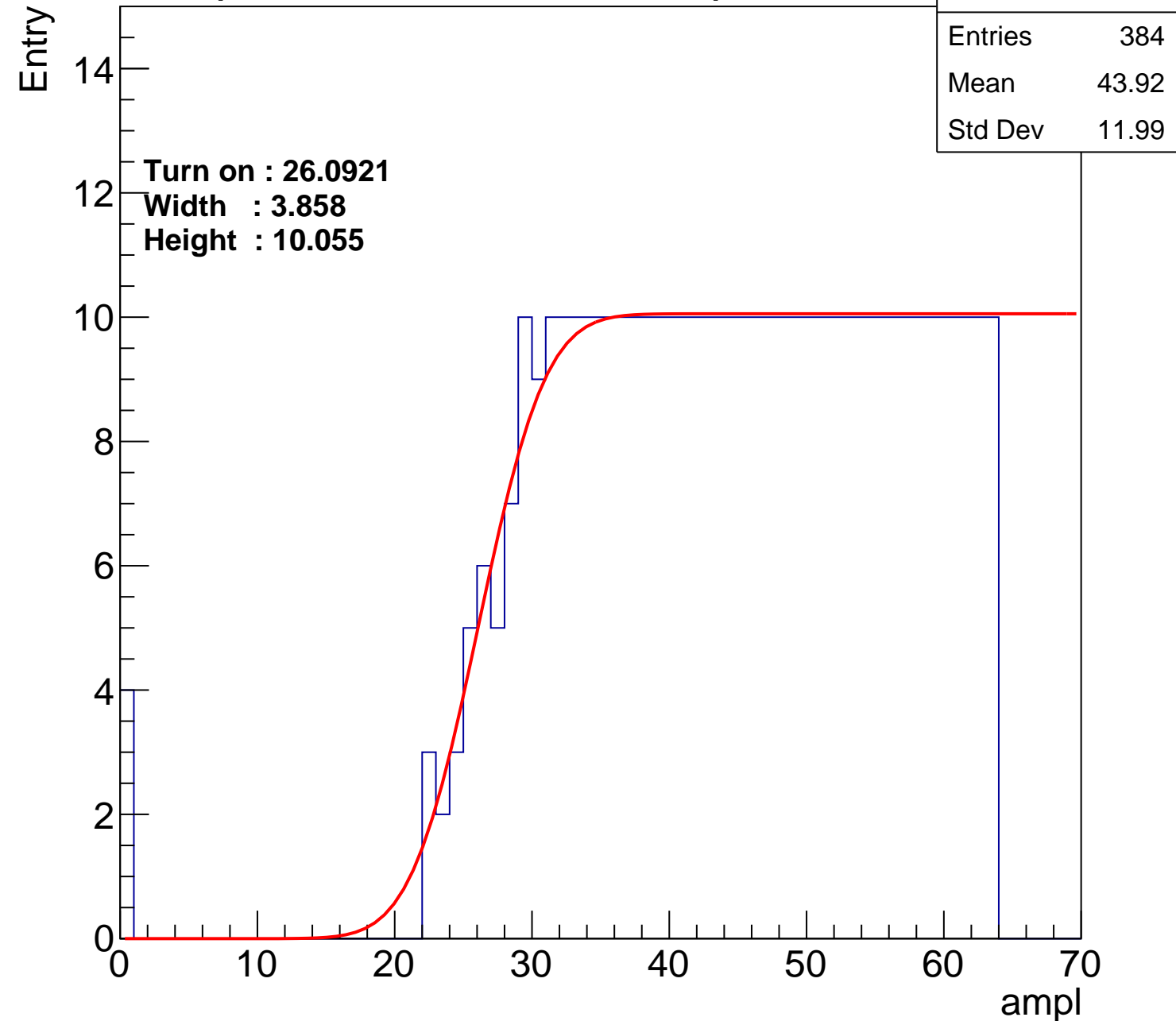
Width : 3.858

Height : 10.055

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U4-ch28

calib_packv5_042523_0143.root, FC#13, port D2

Entries	389
Mean	43.76
Std Dev	11.84

Turn on : 25.7177

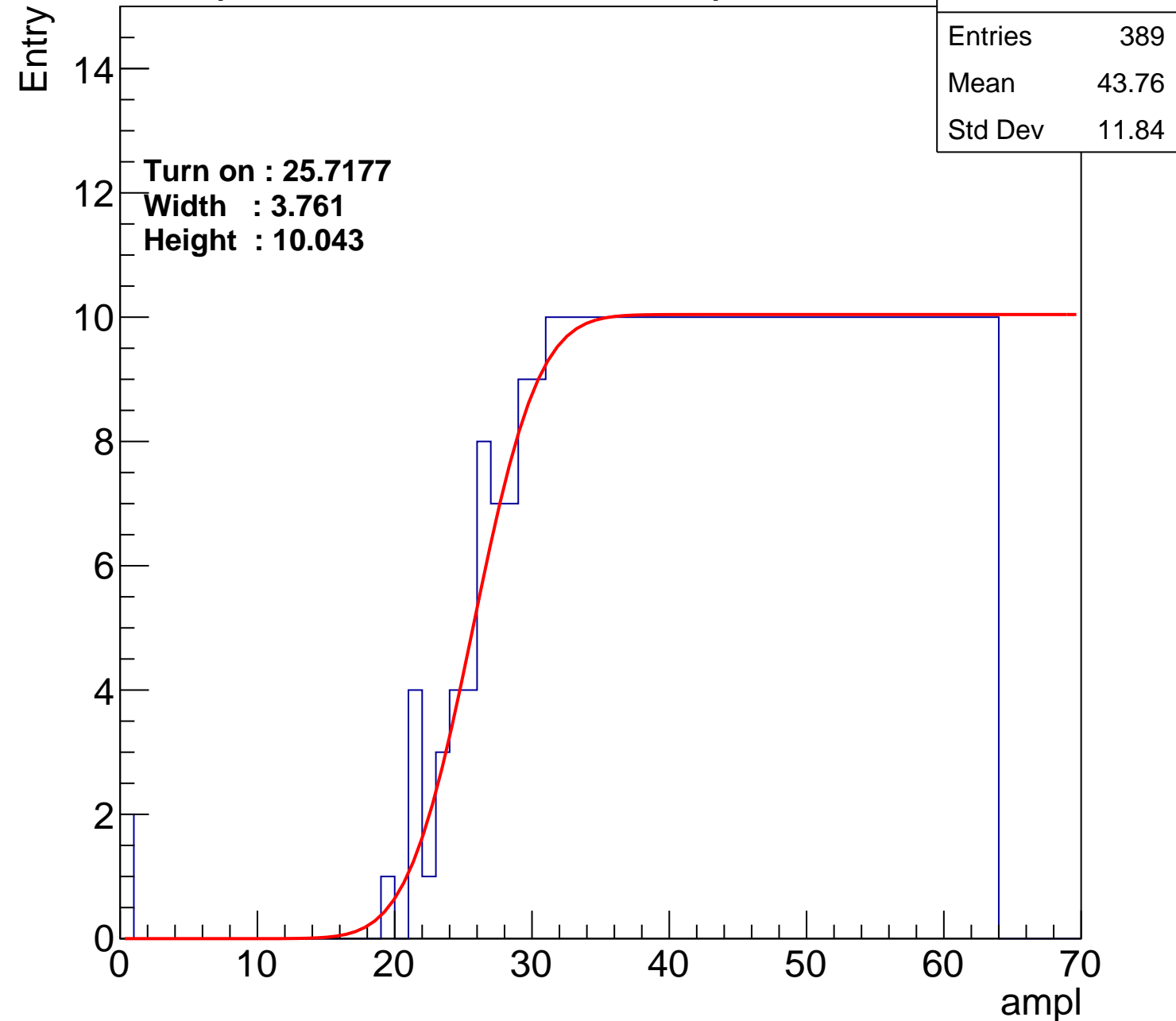
Width : 3.761

Height : 10.043

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U4-ch29

calib_packv5_042523_0143.root, FC#13, port D2

Entries	380
Mean	44.13
Std Dev	11.87

Turn on : 26.4424

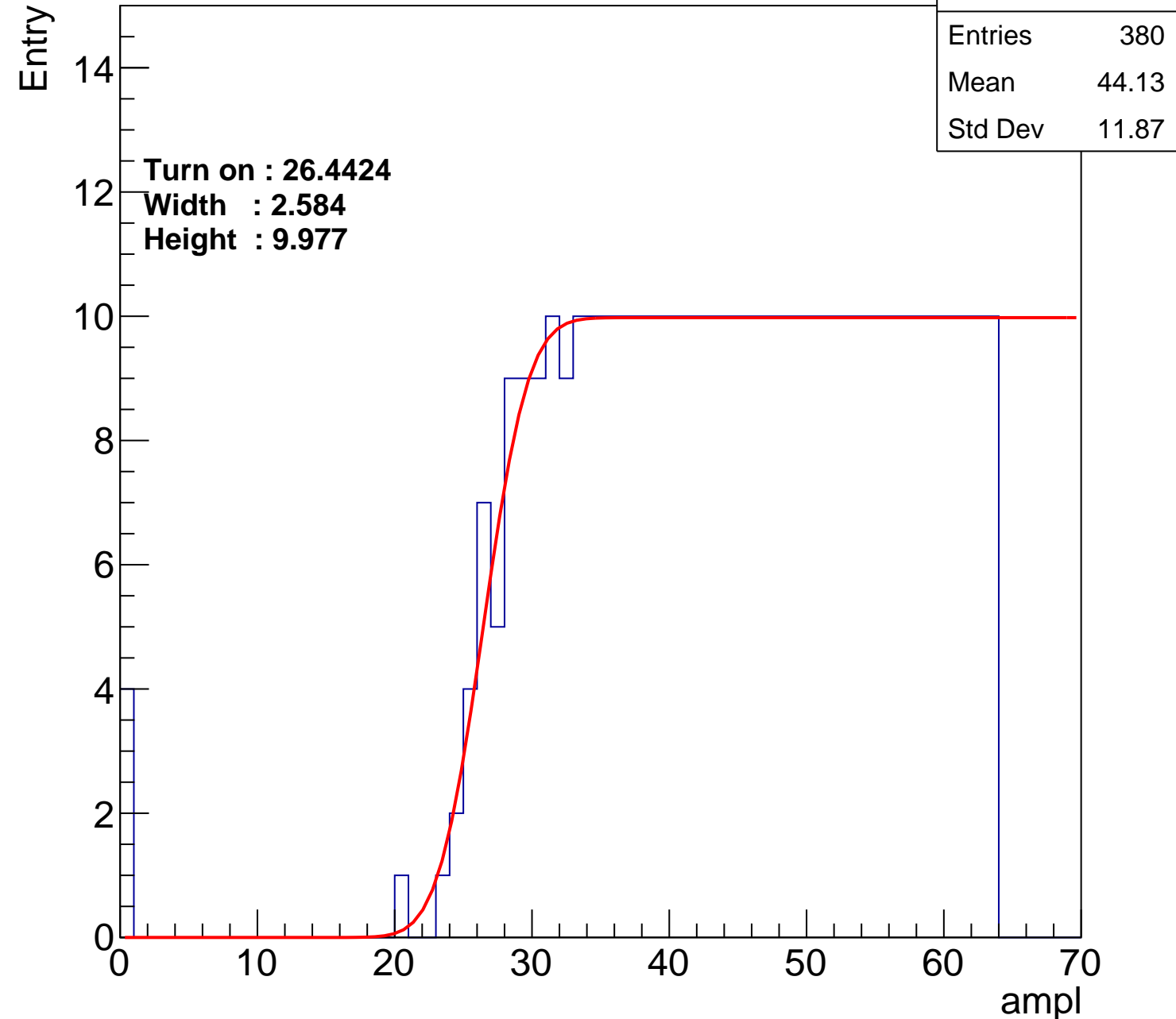
Width : 2.584

Height : 9.977

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U4-ch30

calib_packv5_042523_0143.root, FC#13, port D2

Entries	376
Mean	44.4
Std Dev	11.59

Turn on : 26.9547

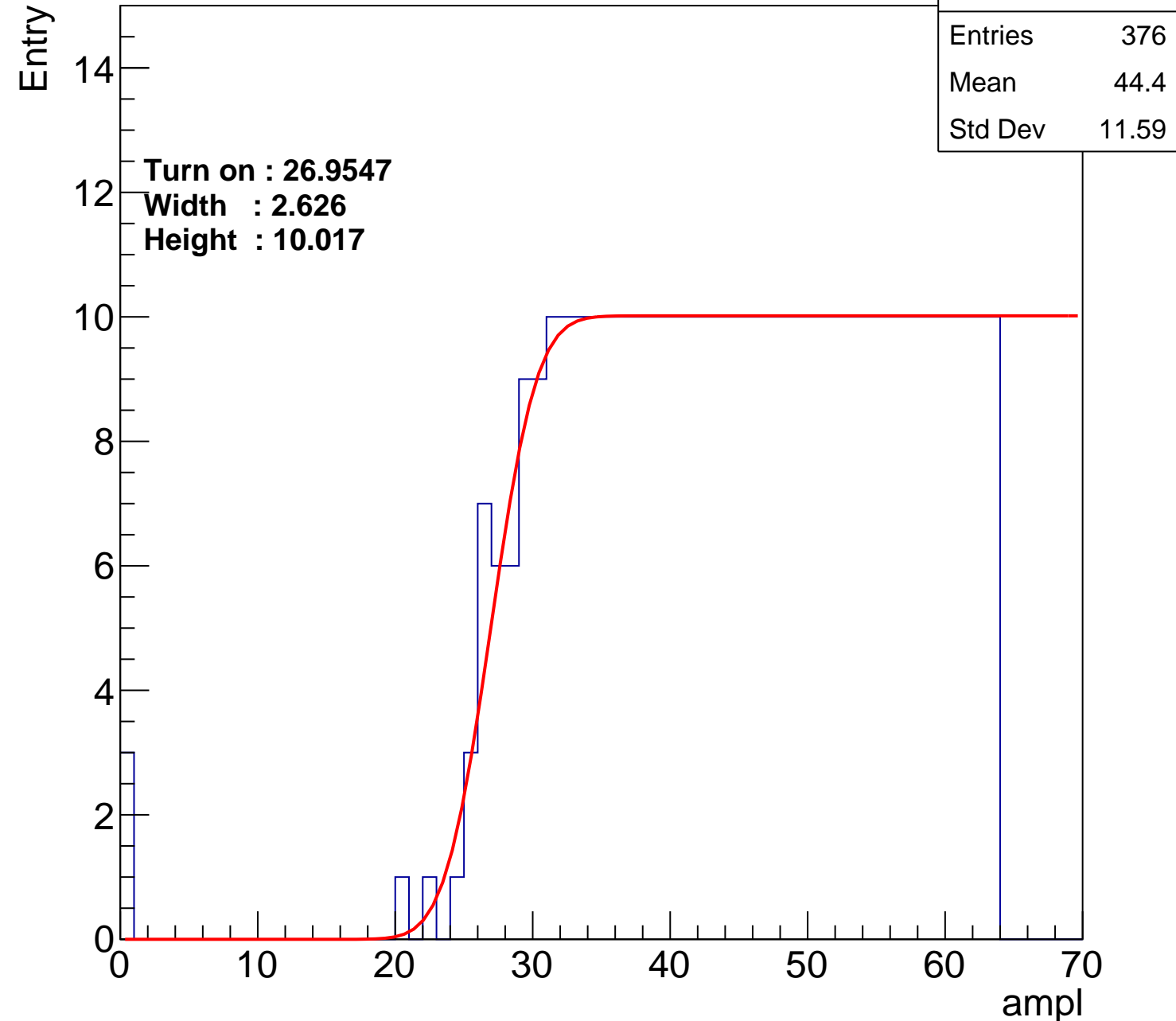
Width : 2.626

Height : 10.017

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U4-ch31

calib_packv5_042523_0143.root, FC#13, port D2

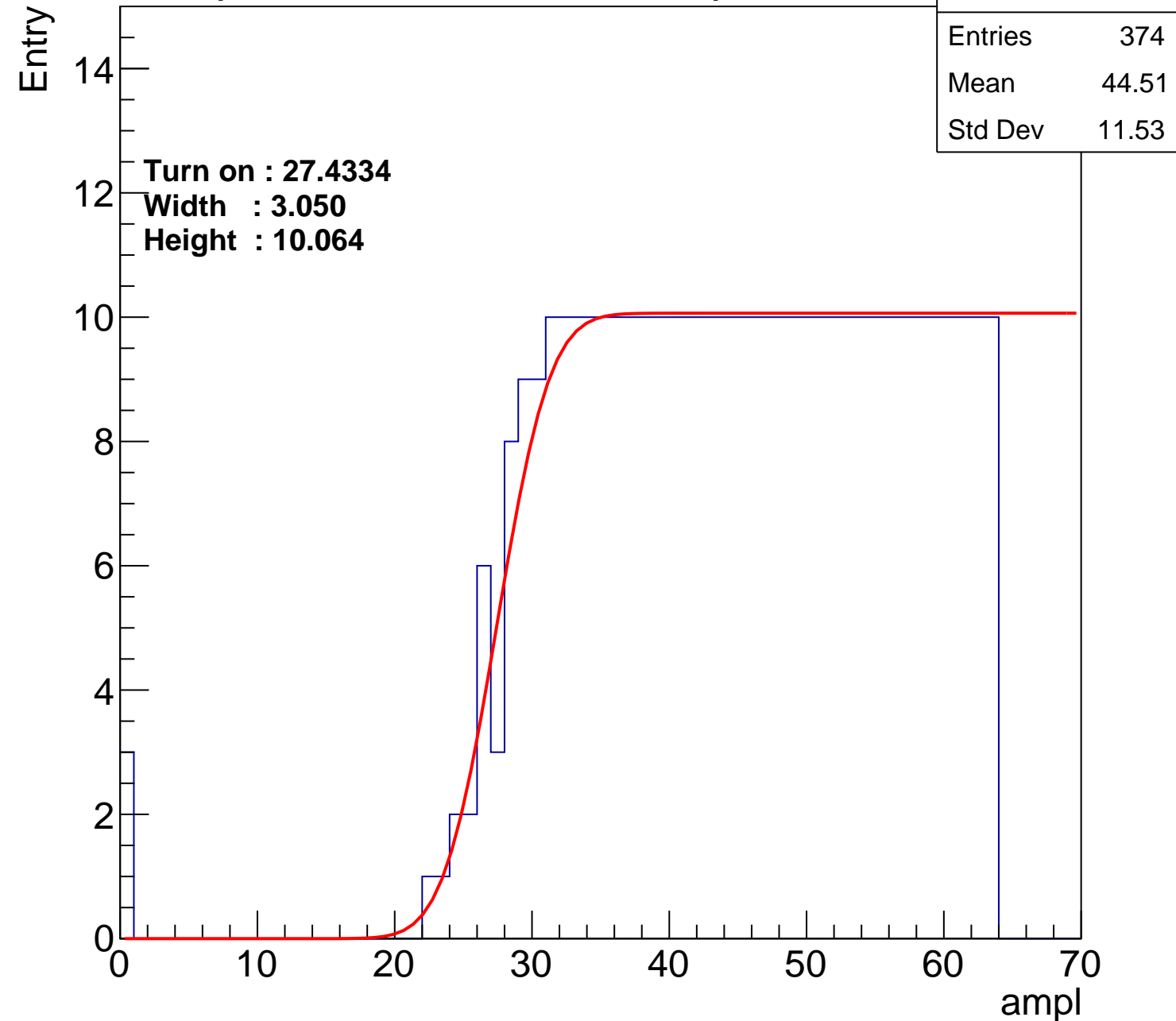
Entry

14
12
10
8
6
4
2
0

Turn on : 27.4334
Width : 3.050
Height : 10.064

Entries	374
Mean	44.51
Std Dev	11.53

ampl



B1L003S, U4-ch32

calib_packv5_042523_0143.root, FC#13, port D2

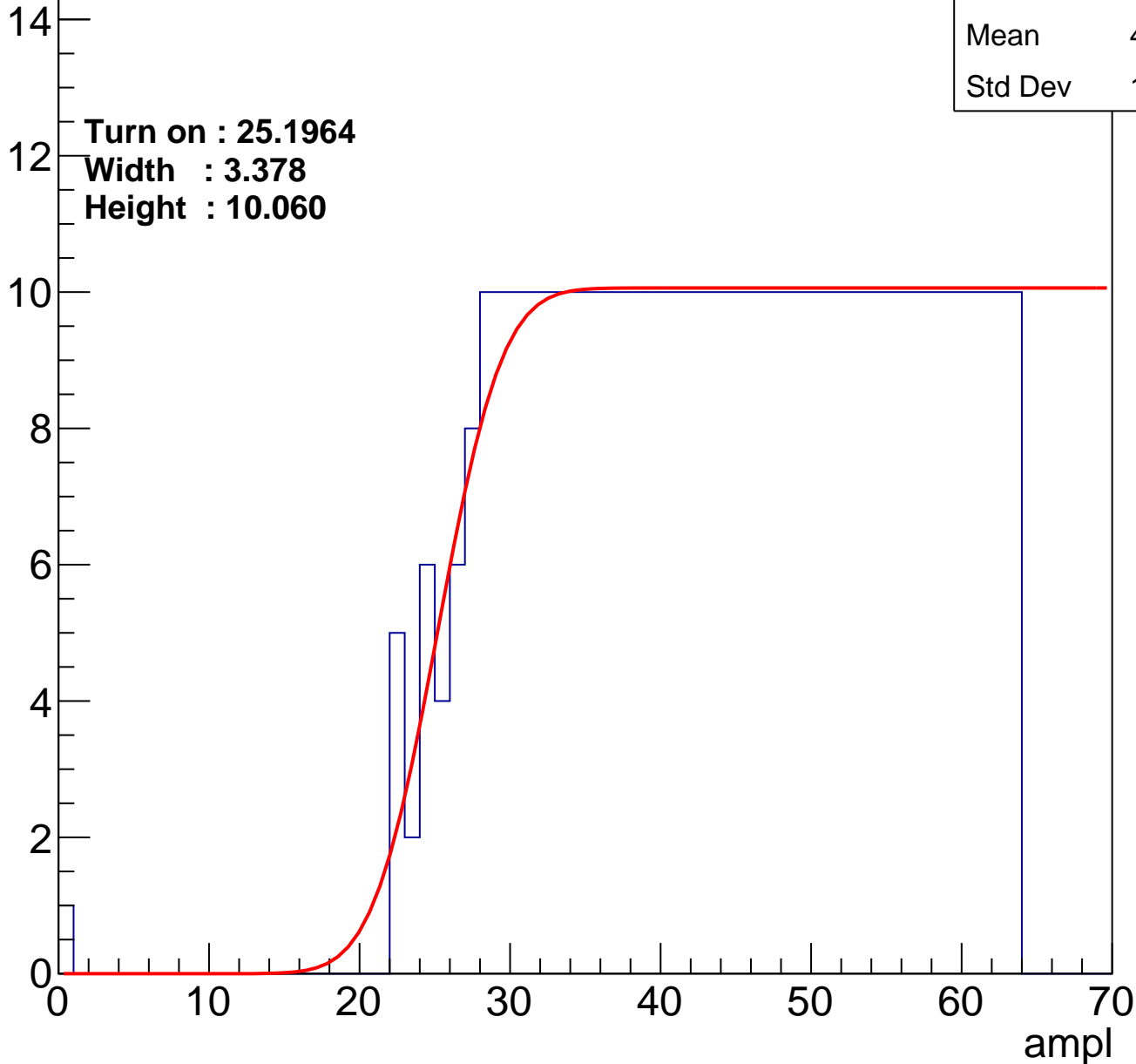
Entries	392
Mean	43.76
Std Dev	11.62

Turn on : 25.1964

Width : 3.378

Height : 10.060

Entry



B1L003S, U4-ch33

calib_packv5_042523_0143.root, FC#13, port D2

Entries	382
Mean	44.14
Std Dev	11.61

Turn on : 26.3412

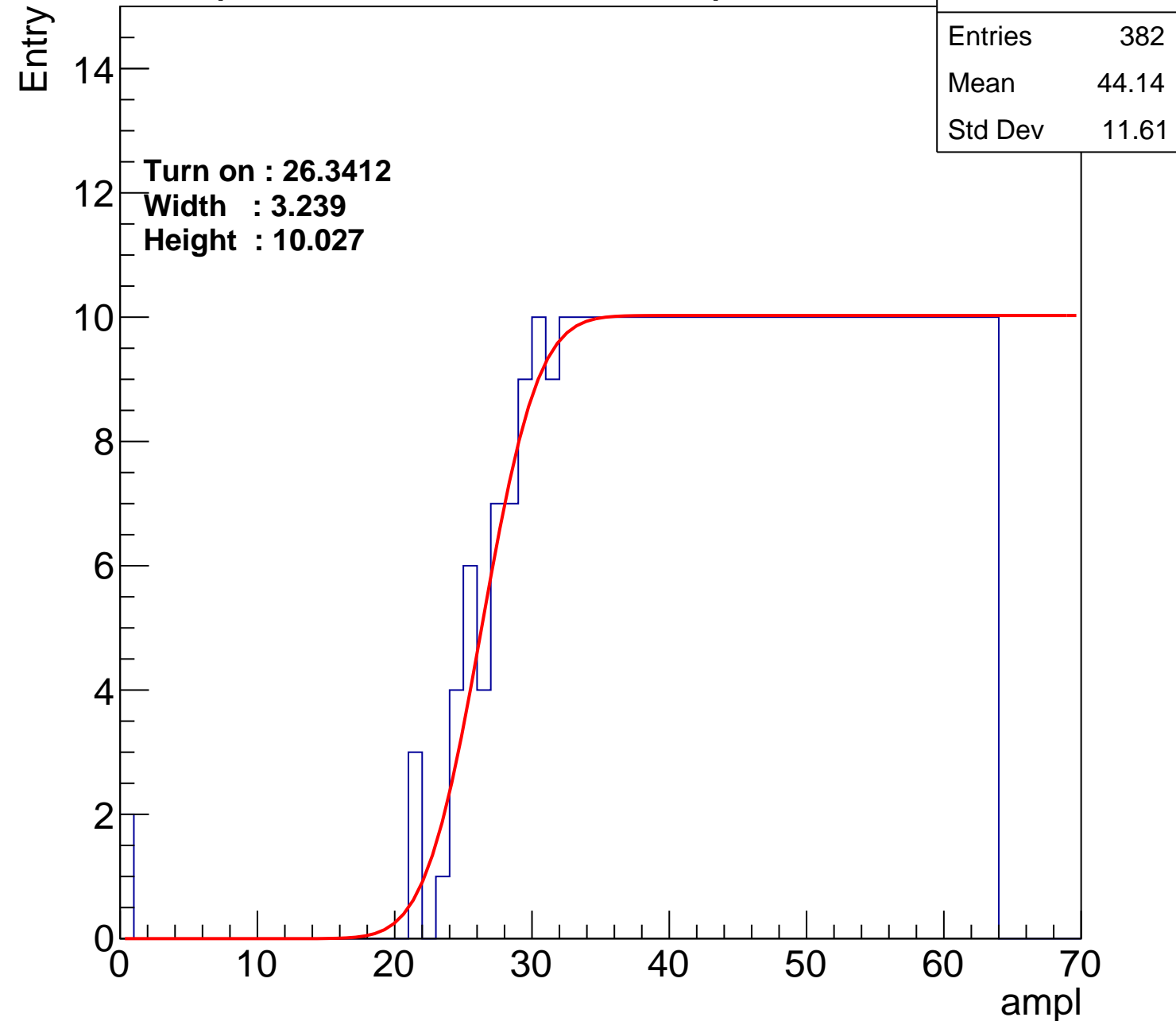
Width : 3.239

Height : 10.027

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U4-ch34

calib_packv5_042523_0143.root, FC#13, port D2

Entries	376
Mean	44.47
Std Dev	11.39

Turn on : 26.7027

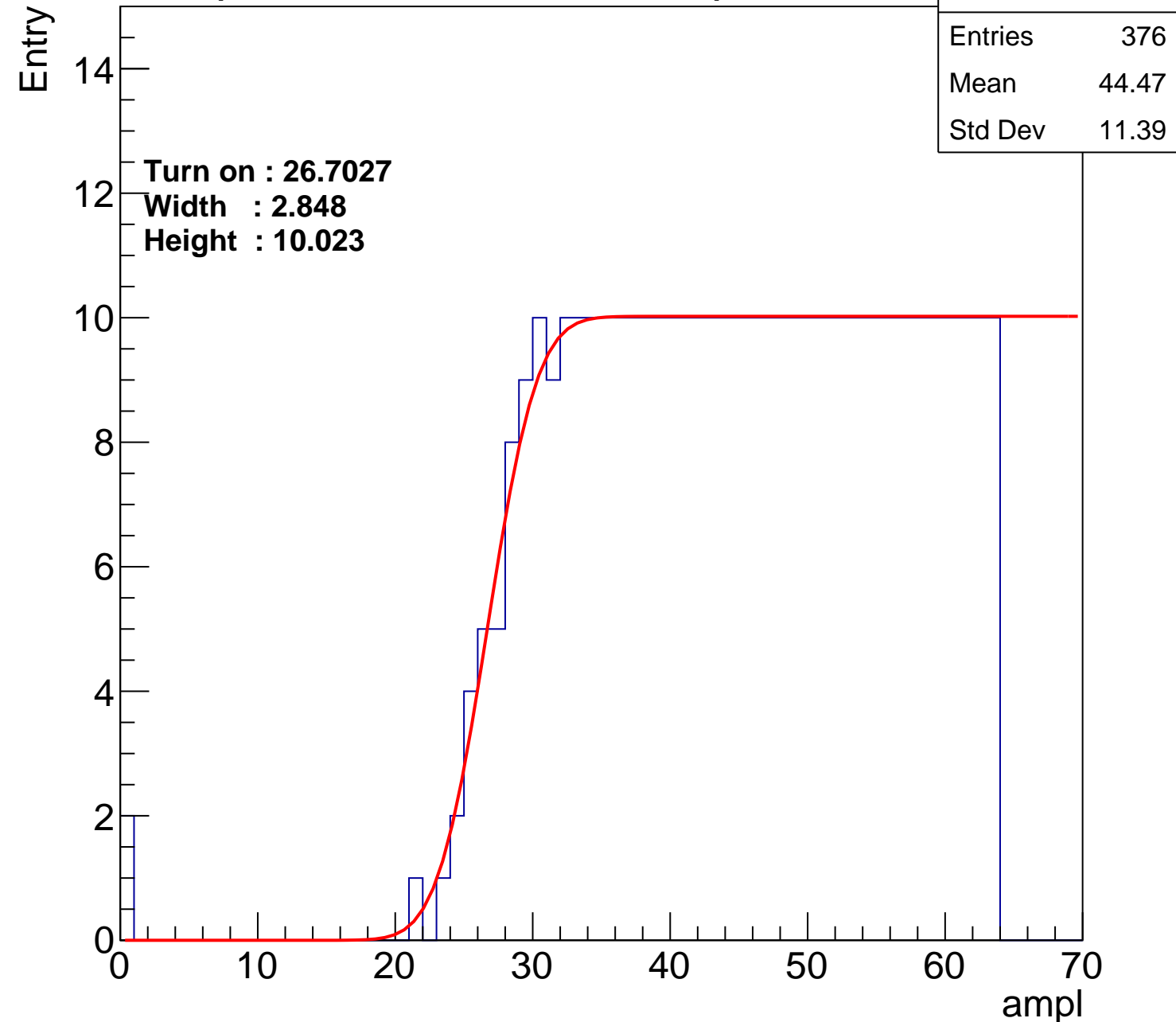
Width : 2.848

Height : 10.023

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U4-ch35

calib_packv5_042523_0143.root, FC#13, port D2

Entries	381
Mean	44.07
Std Dev	11.92

Turn on : 26.4719

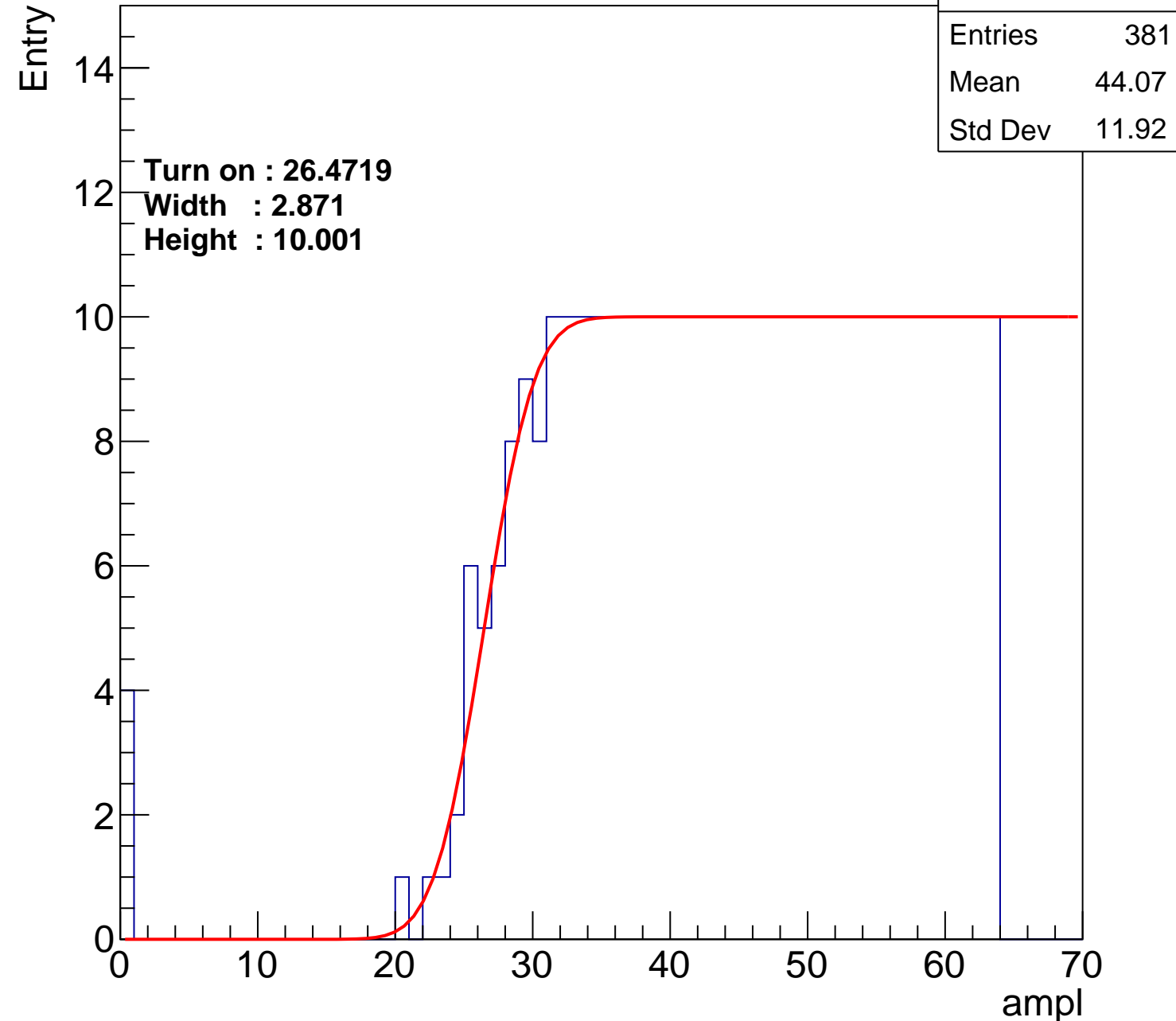
Width : 2.871

Height : 10.001

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U4-ch36

calib_packv5_042523_0143.root, FC#13, port D2

Entries	363
Mean	44.99
Std Dev	11.33

Turn on : 27.7551

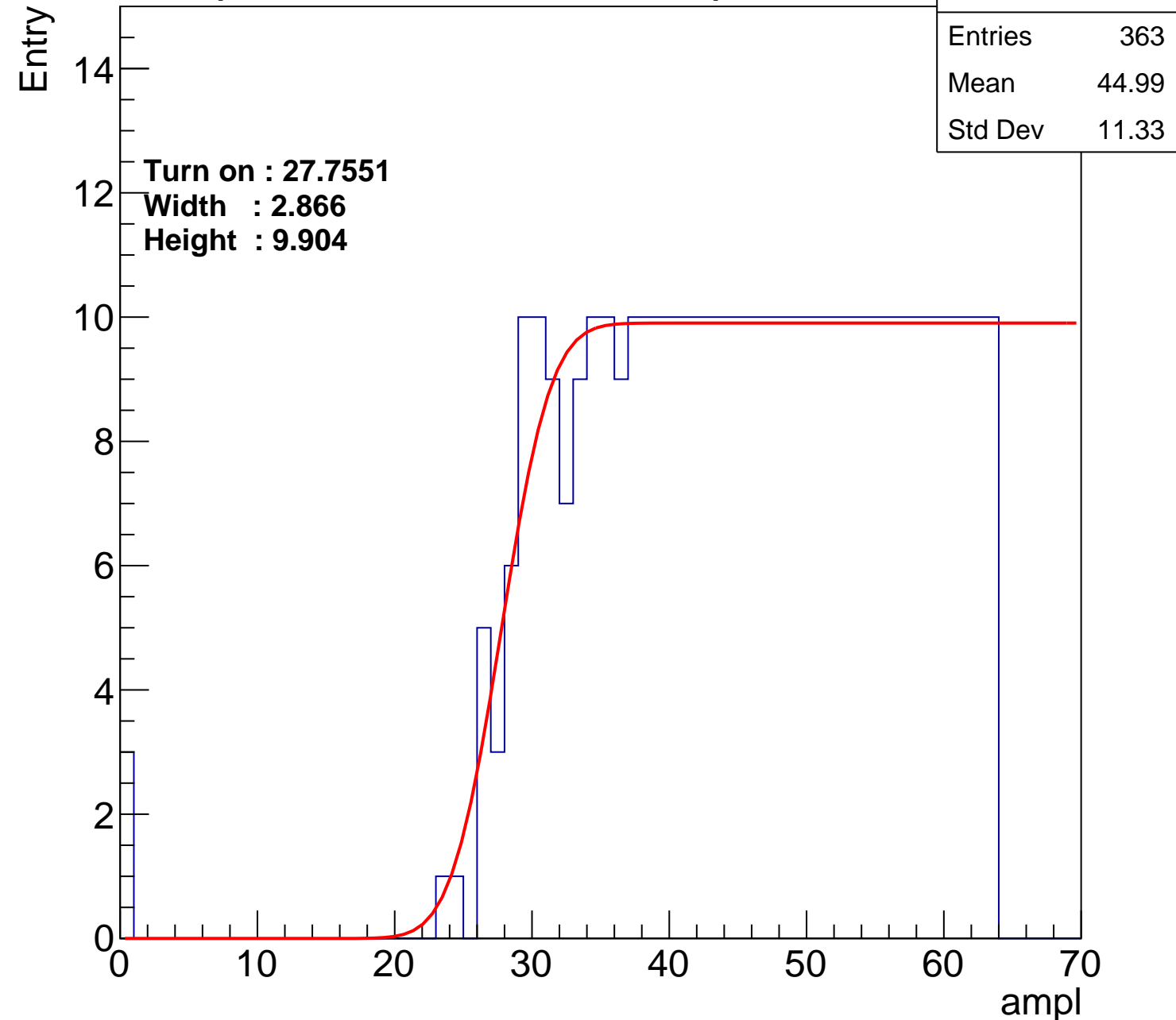
Width : 2.866

Height : 9.904

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U4-ch37

calib_packv5_042523_0143.root, FC#13, port D2

Entries	368
Mean	44.91
Std Dev	11.02

Turn on : 27.5302

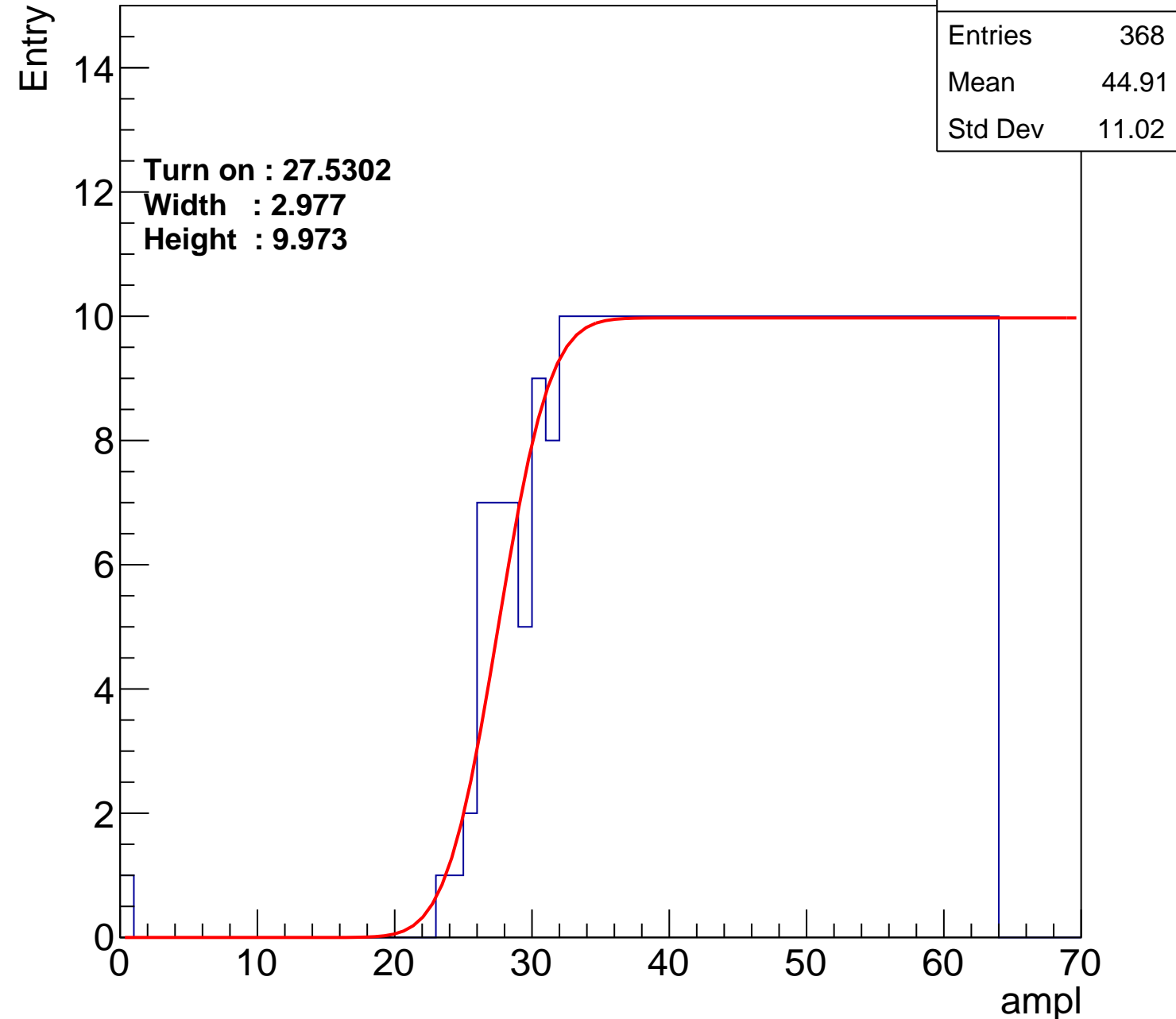
Width : 2.977

Height : 9.973

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U4-ch38

calib_packv5_042523_0143.root, FC#13, port D2

Entries	380
Mean	44.24
Std Dev	11.55

Turn on : 26.4482

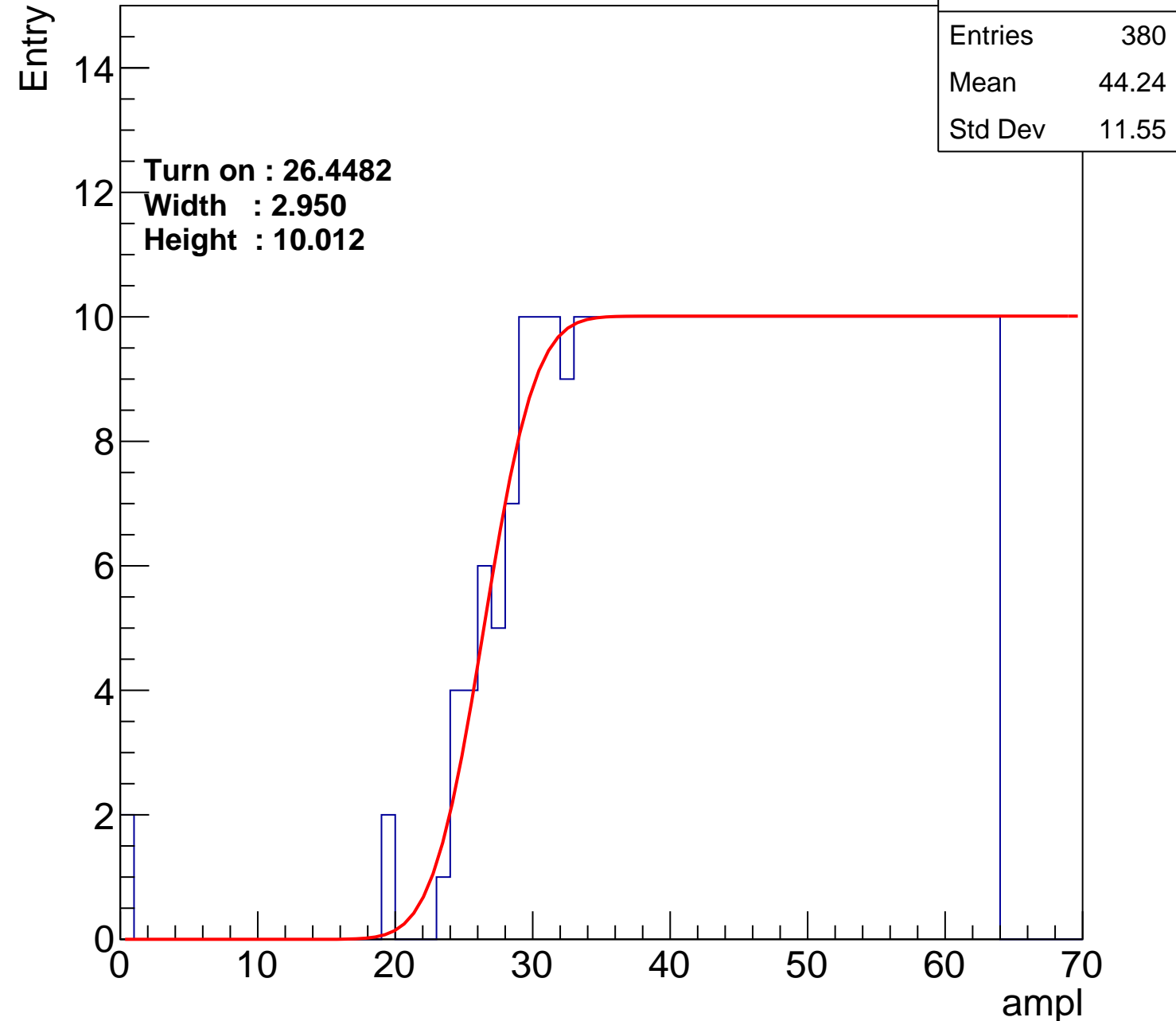
Width : 2.950

Height : 10.012

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U4-ch39

calib_packv5_042523_0143.root, FC#13, port D2

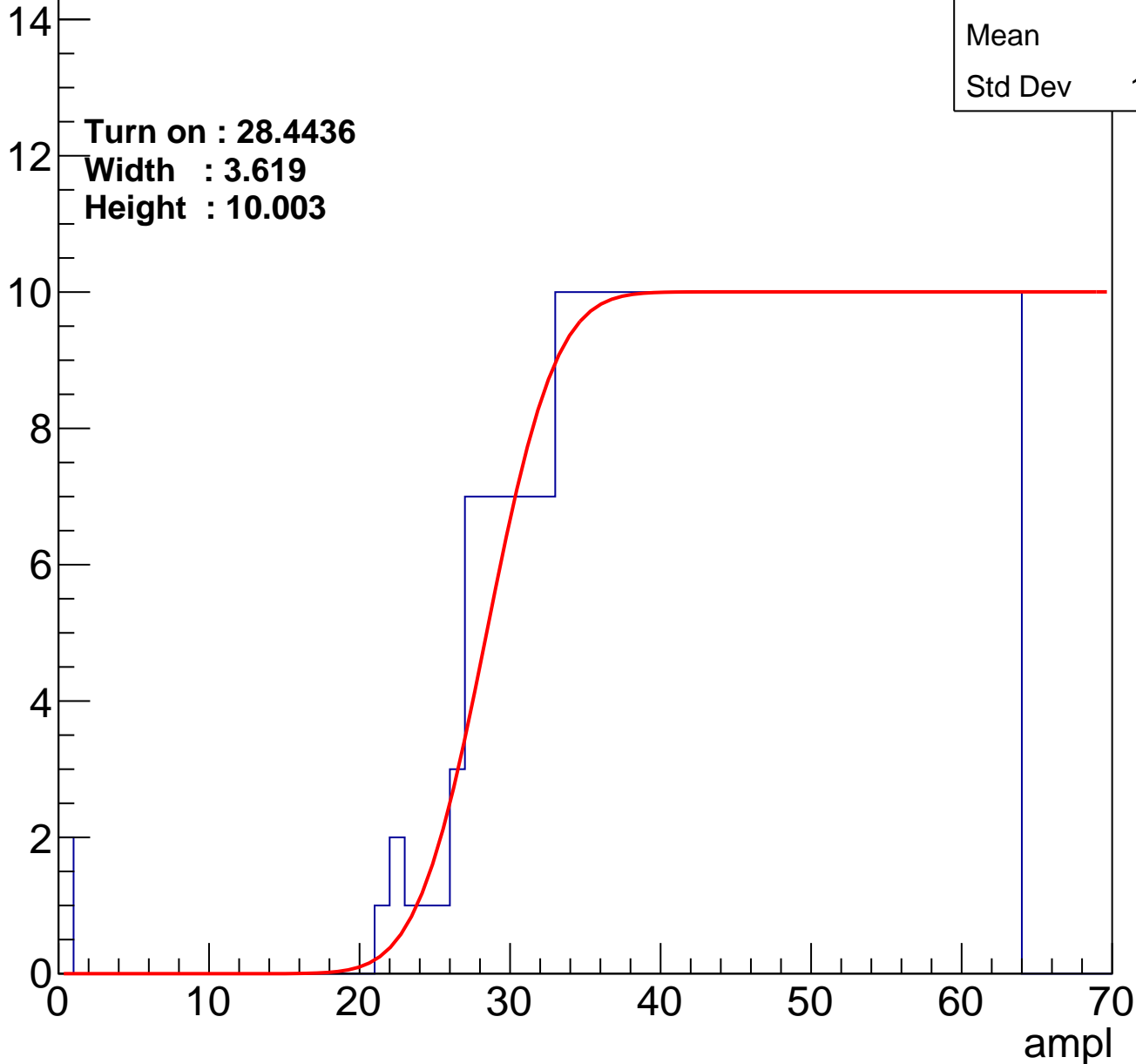
Entry

Entries	363
Mean	45
Std Dev	11.24

Turn on : 28.4436

Width : 3.619

Height : 10.003



B1L003S, U4-ch40

calib_packv5_042523_0143.root, FC#13, port D2

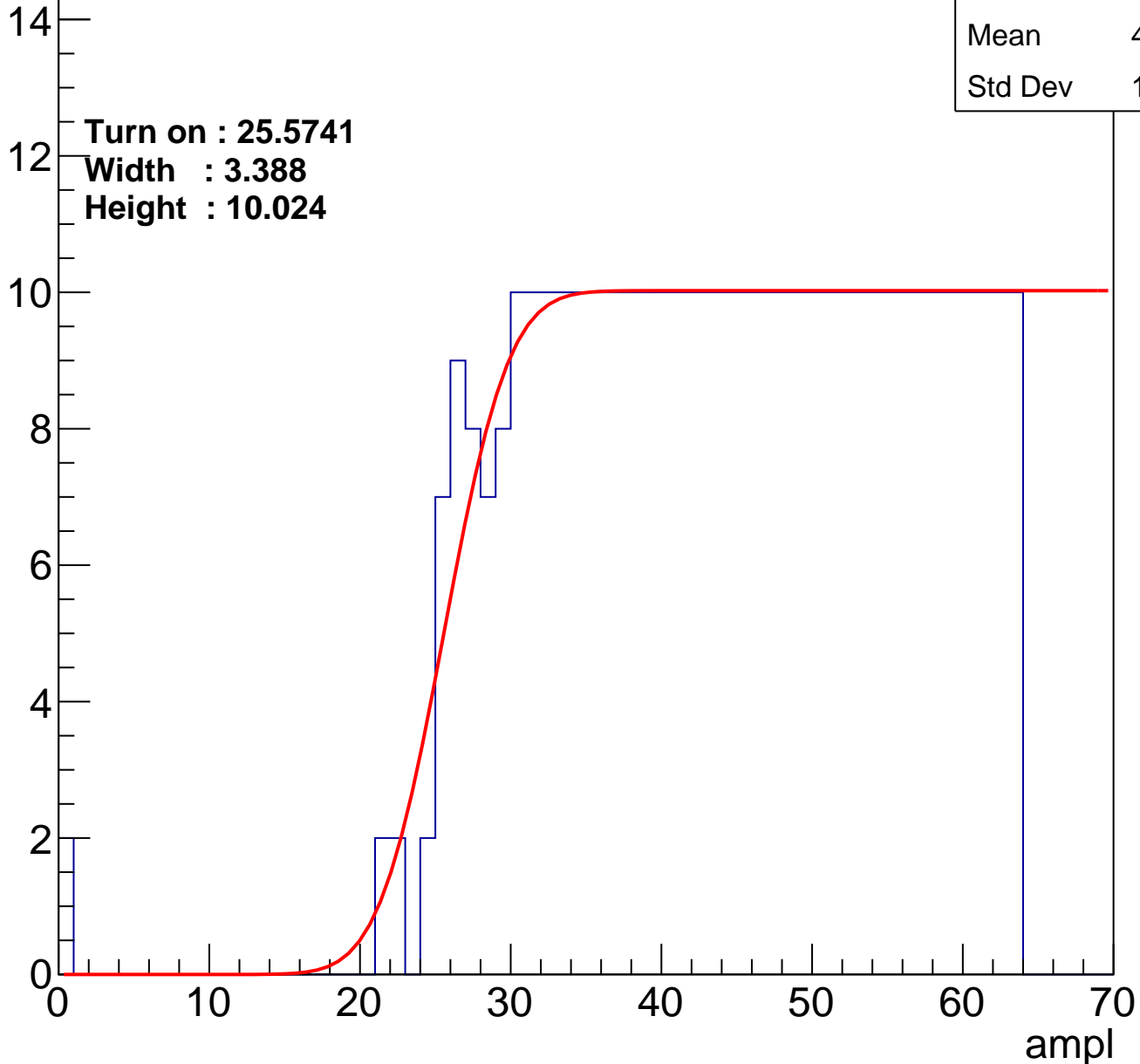
Entries	387
Mean	43.92
Std Dev	11.69

Turn on : 25.5741

Width : 3.388

Height : 10.024

Entry



B1L003S, U4-ch41

calib_packv5_042523_0143.root, FC#13, port D2

Entries	376
Mean	44.22
Std Dev	12.1

Turn on : 27.2988

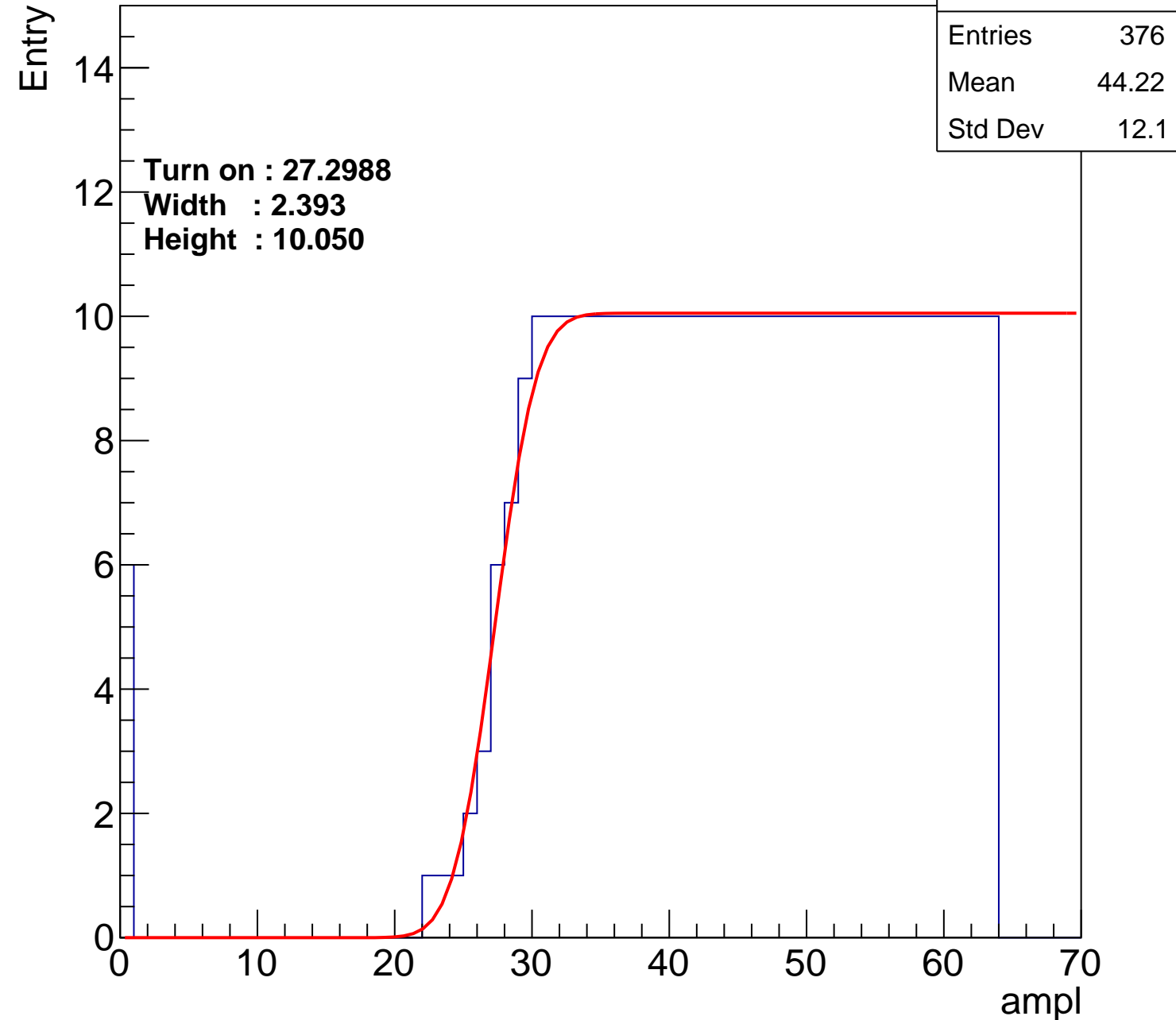
Width : 2.393

Height : 10.050

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U4-ch42

calib_packv5_042523_0143.root, FC#13, port D2

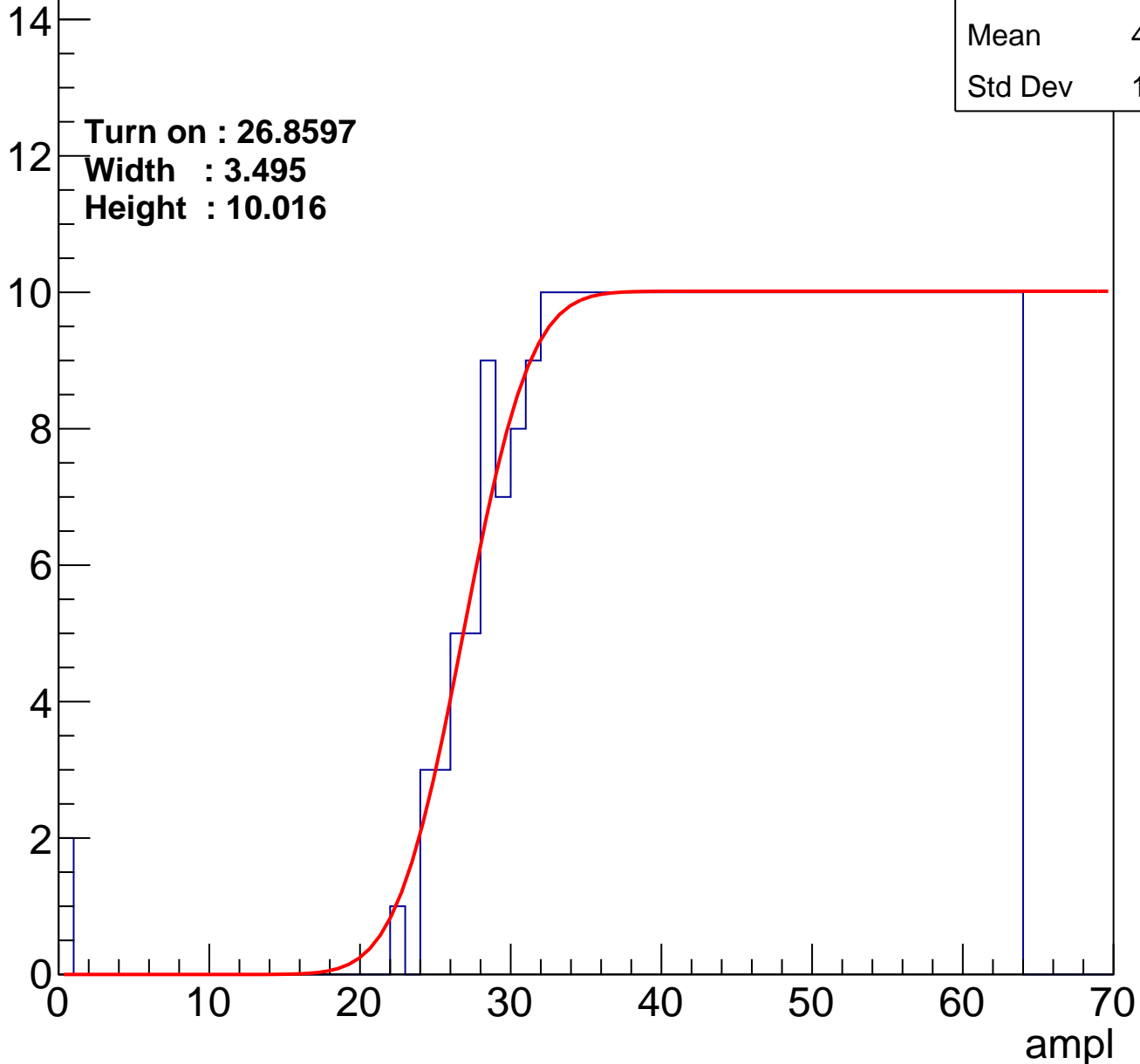
Entries	372
Mean	44.65
Std Dev	11.33

Turn on : 26.8597

Width : 3.495

Height : 10.016

Entry



B1L003S, U4-ch43

calib_packv5_042523_0143.root, FC#13, port D2

Entries	388
Mean	43.85
Std Dev	11.74

Turn on : 25.3170

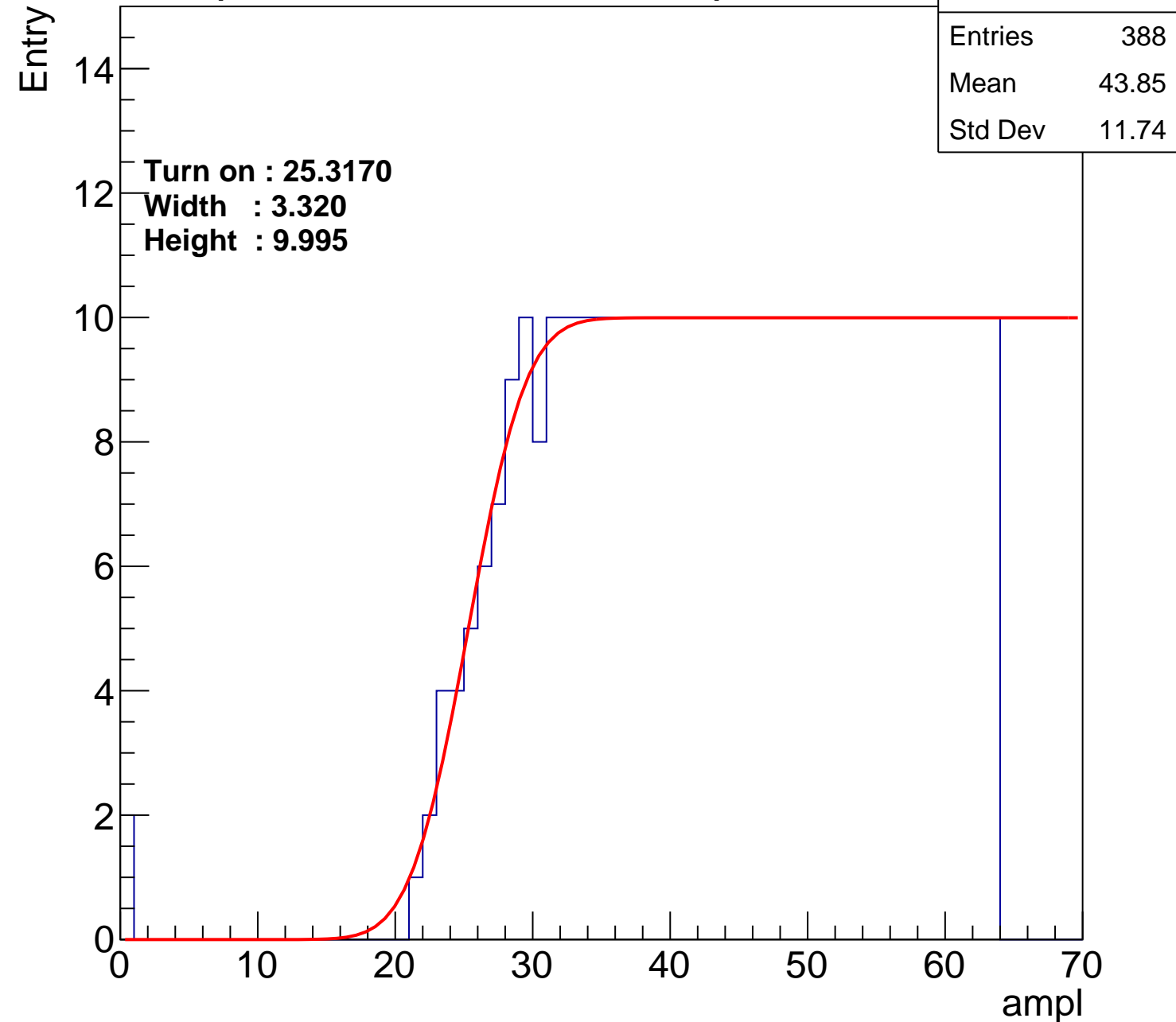
Width : 3.320

Height : 9.995

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U4-ch44

calib_packv5_042523_0143.root, FC#13, port D2

Entries	373
Mean	44.46
Std Dev	11.73

Turn on : 26.8258

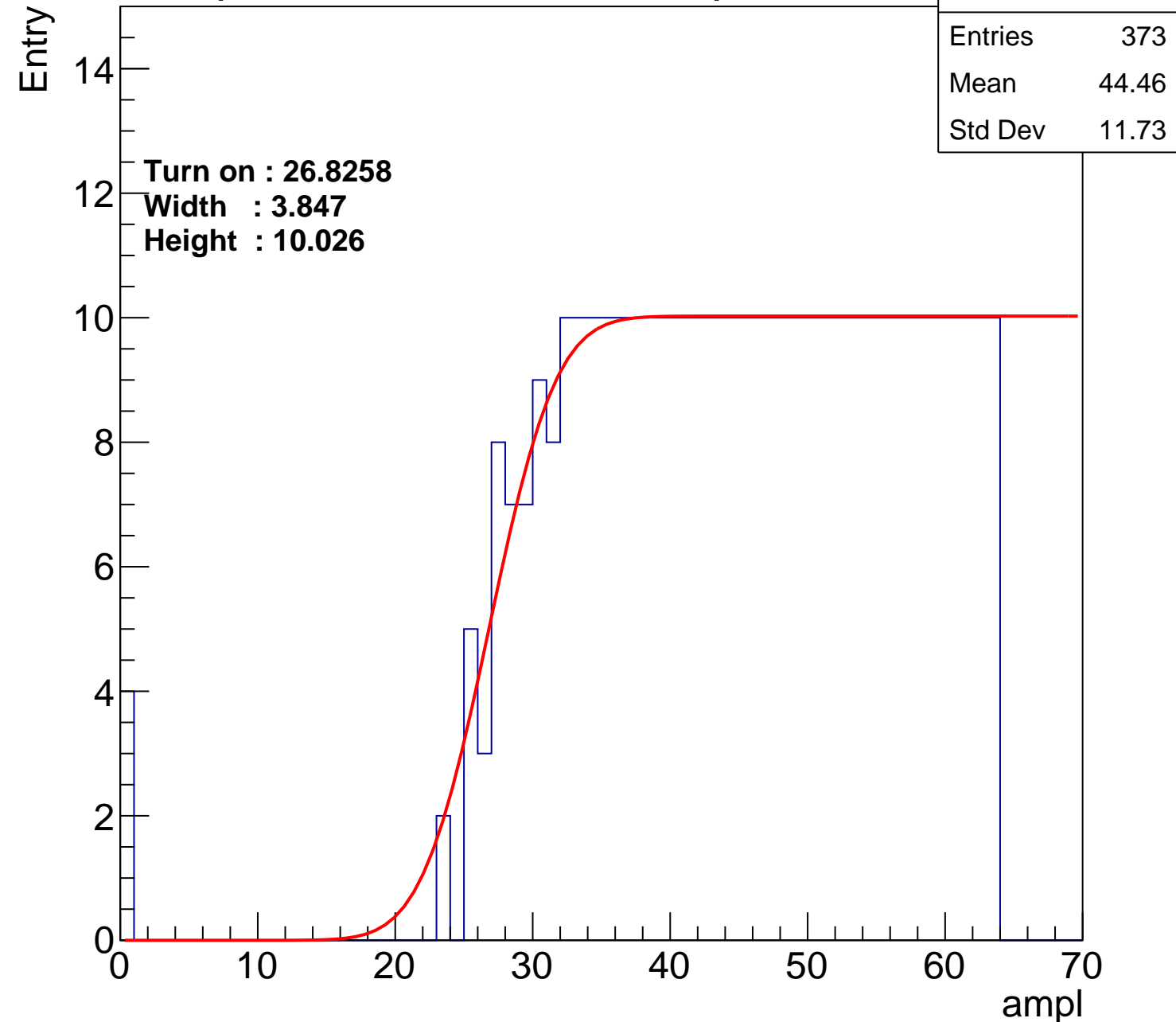
Width : 3.847

Height : 10.026

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U4-ch45

calib_packv5_042523_0143.root, FC#13, port D2

Entries	377
Mean	43.96
Std Dev	12.56

Turn on : 27.8279

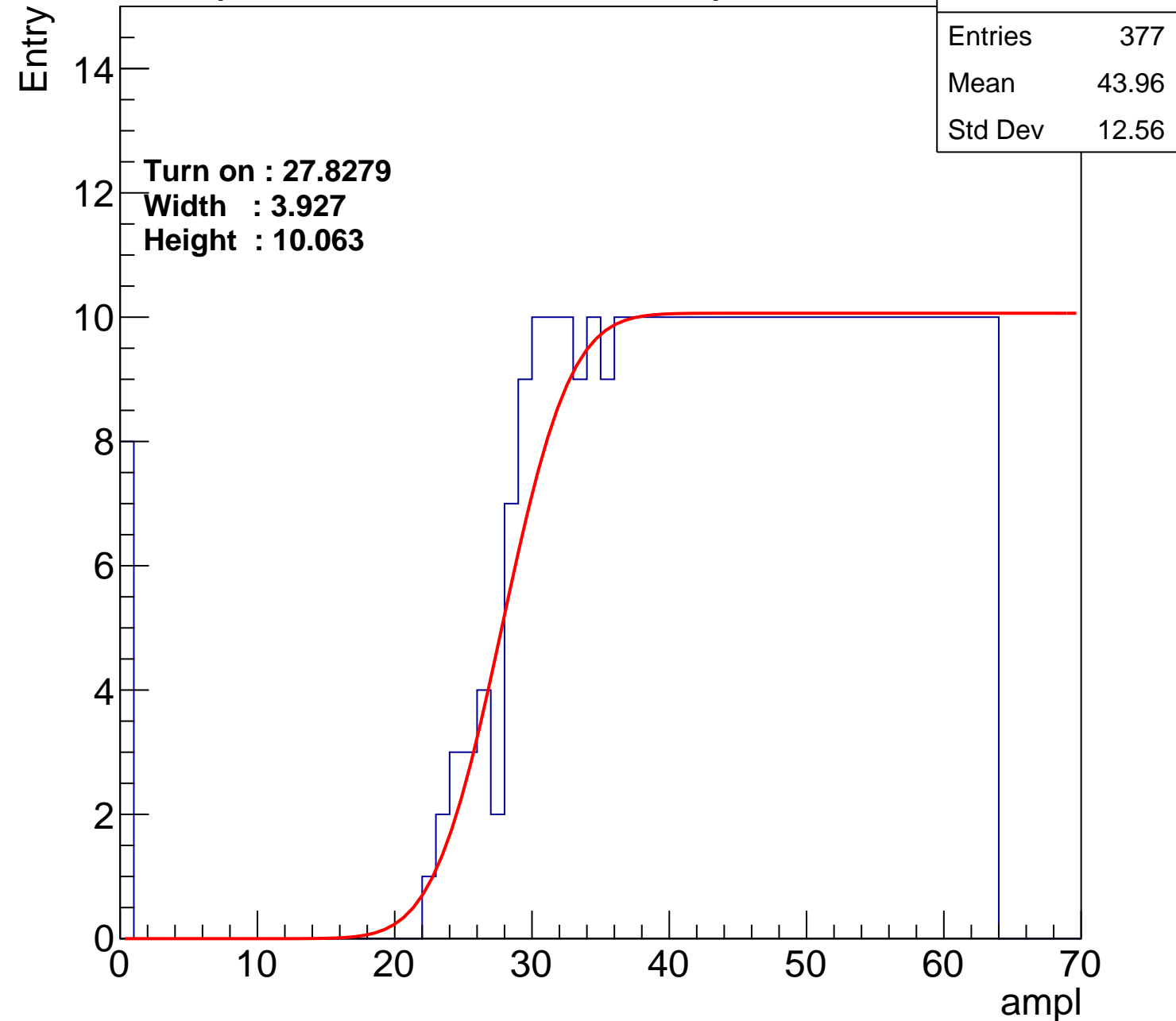
Width : 3.927

Height : 10.063

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U4-ch46

calib_packv5_042523_0143.root, FC#13, port D2

Entries	354
Mean	45.43
Std Dev	11.14

Turn on : 29.1542

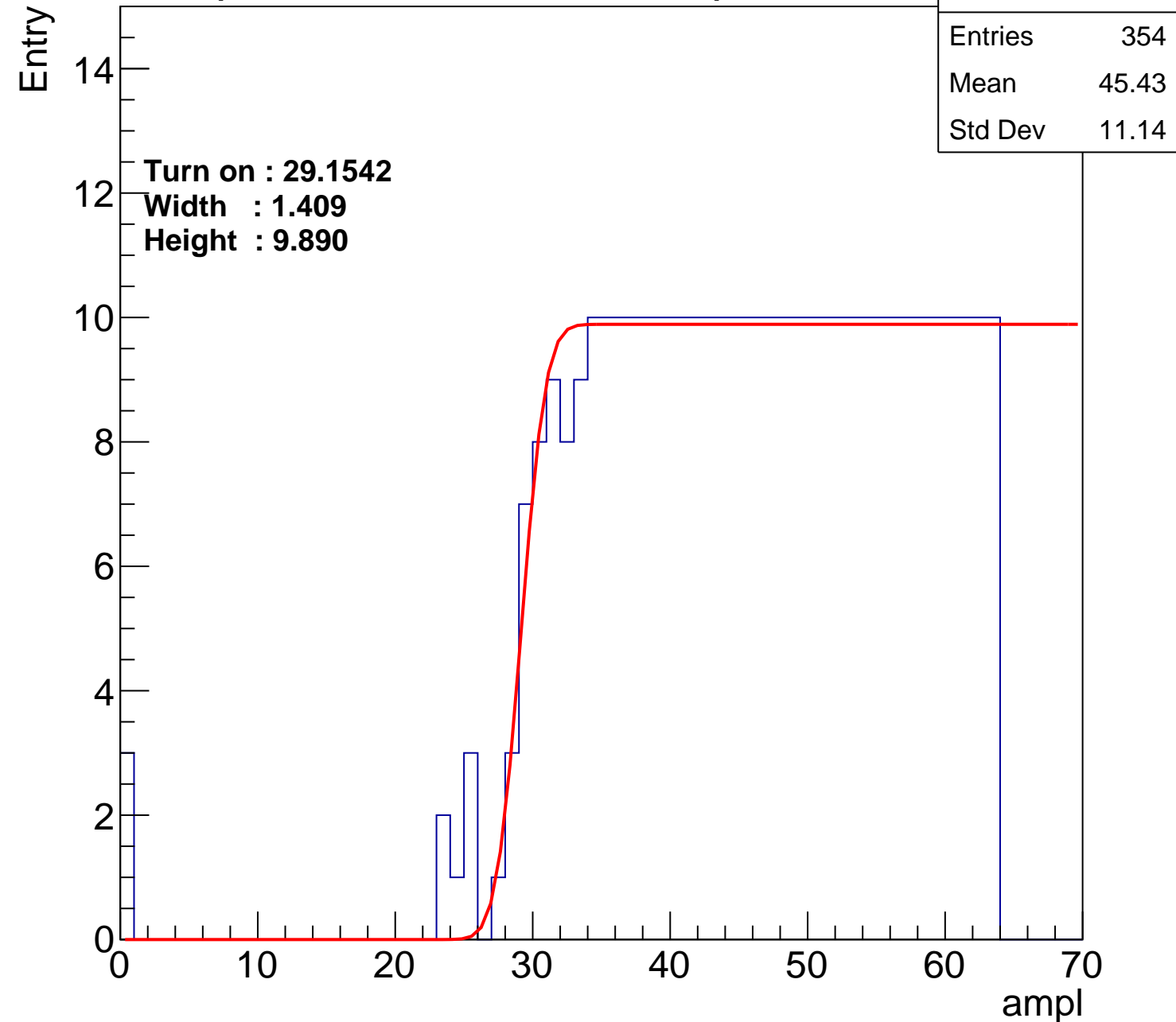
Width : 1.409

Height : 9.890

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U4-ch47

calib_packv5_042523_0143.root, FC#13, port D2

Entries	375
Mean	44.38
Std Dev	11.67

Turn on : 28.2199

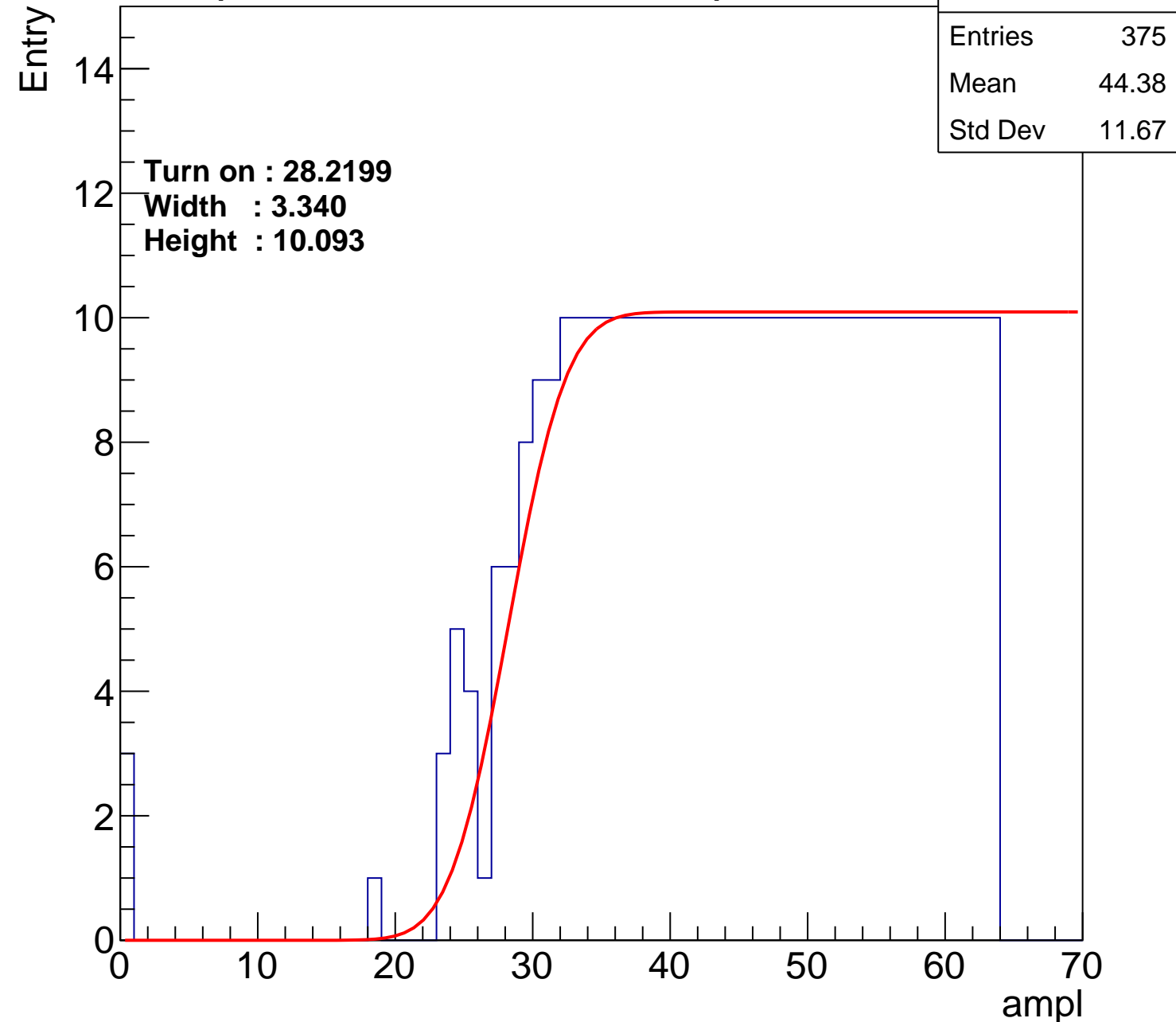
Width : 3.340

Height : 10.093

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U4-ch48

calib_packv5_042523_0143.root, FC#13, port D2

Entries	348
Mean	45.61
Std Dev	11.26

Turn on : 29.7157

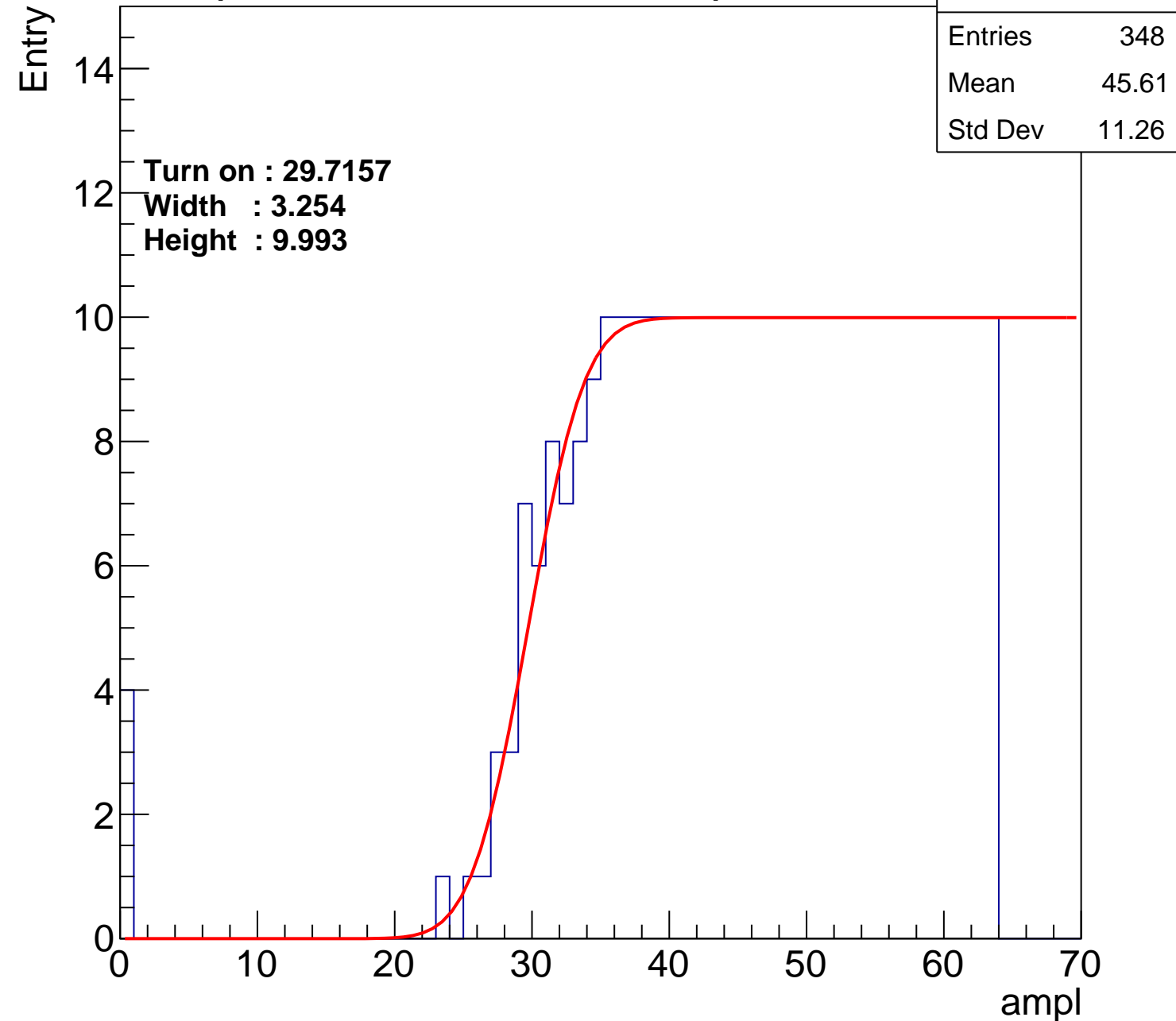
Width : 3.254

Height : 9.993

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U4-ch49

calib_packv5_042523_0143.root, FC#13, port D2

Entries	388
Mean	43.77
Std Dev	12.01

Turn on : 25.8386

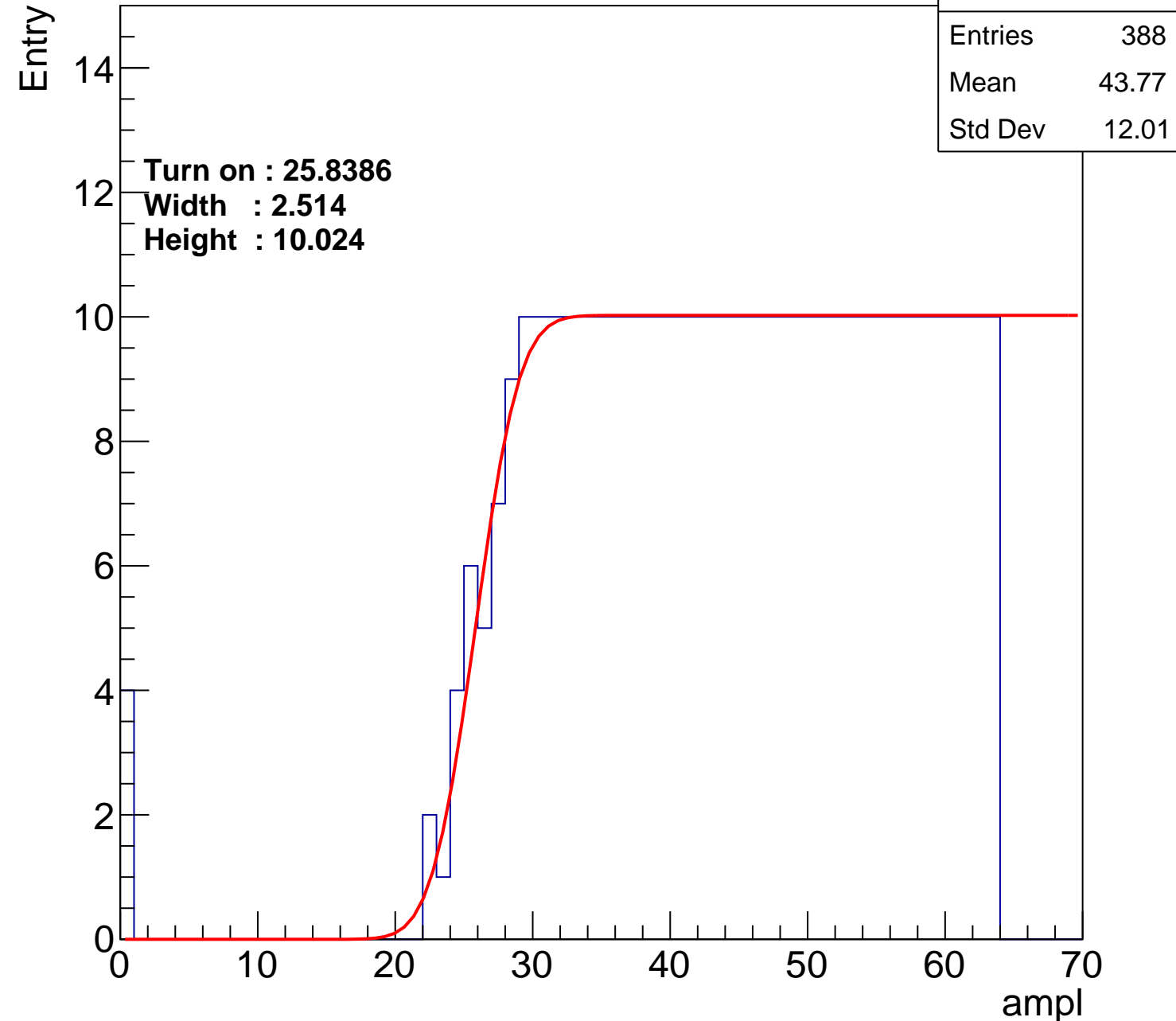
Width : 2.514

Height : 10.024

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U4-ch50

calib_packv5_042523_0143.root, FC#13, port D2

Entries	370
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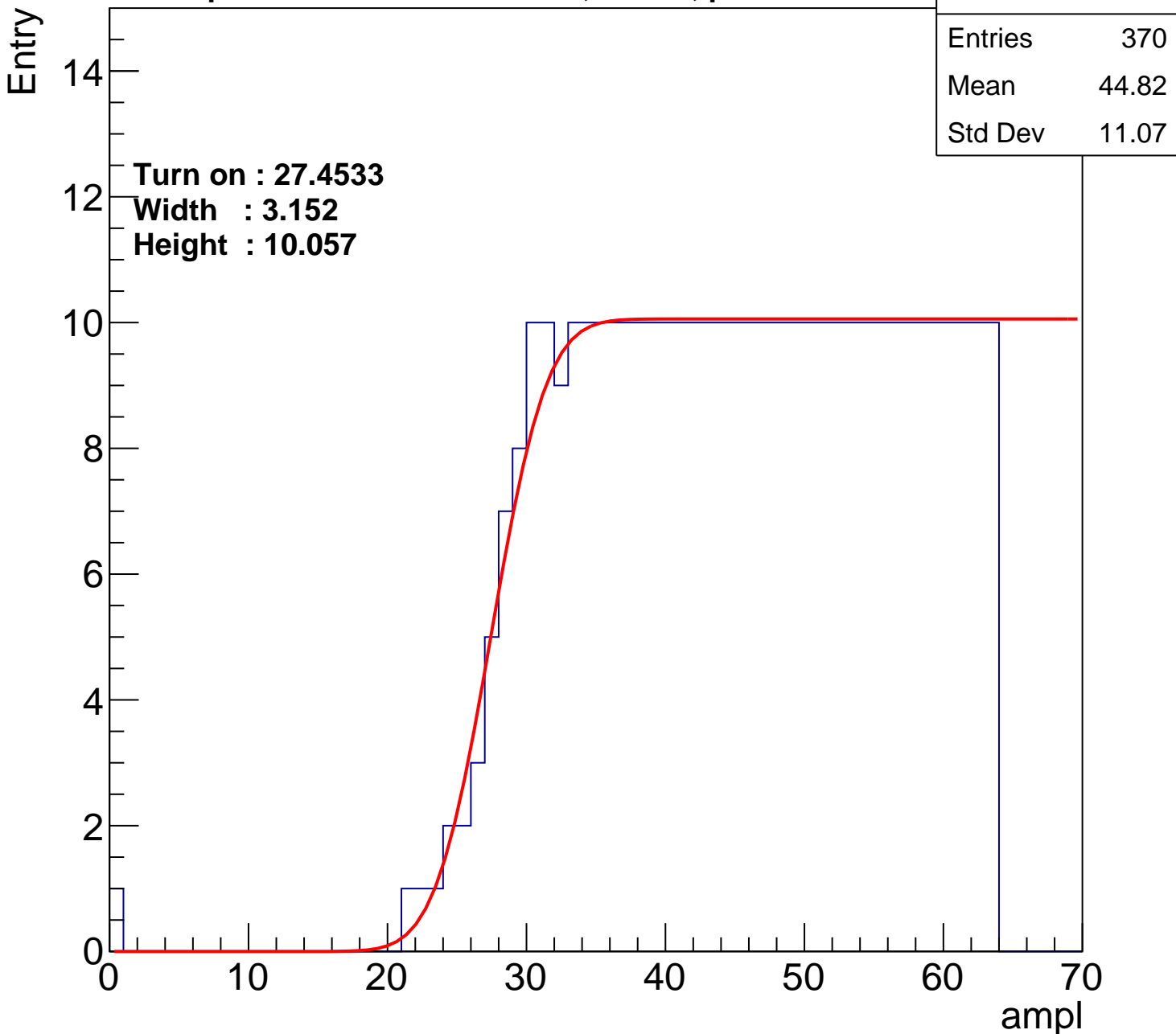
Mean	44.82
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Std Dev	11.07
---------	-------

Turn on : 27.4533

Width : 3.152

Height : 10.057



B1L003S, U4-ch51

calib_packv5_042523_0143.root, FC#13, port D2

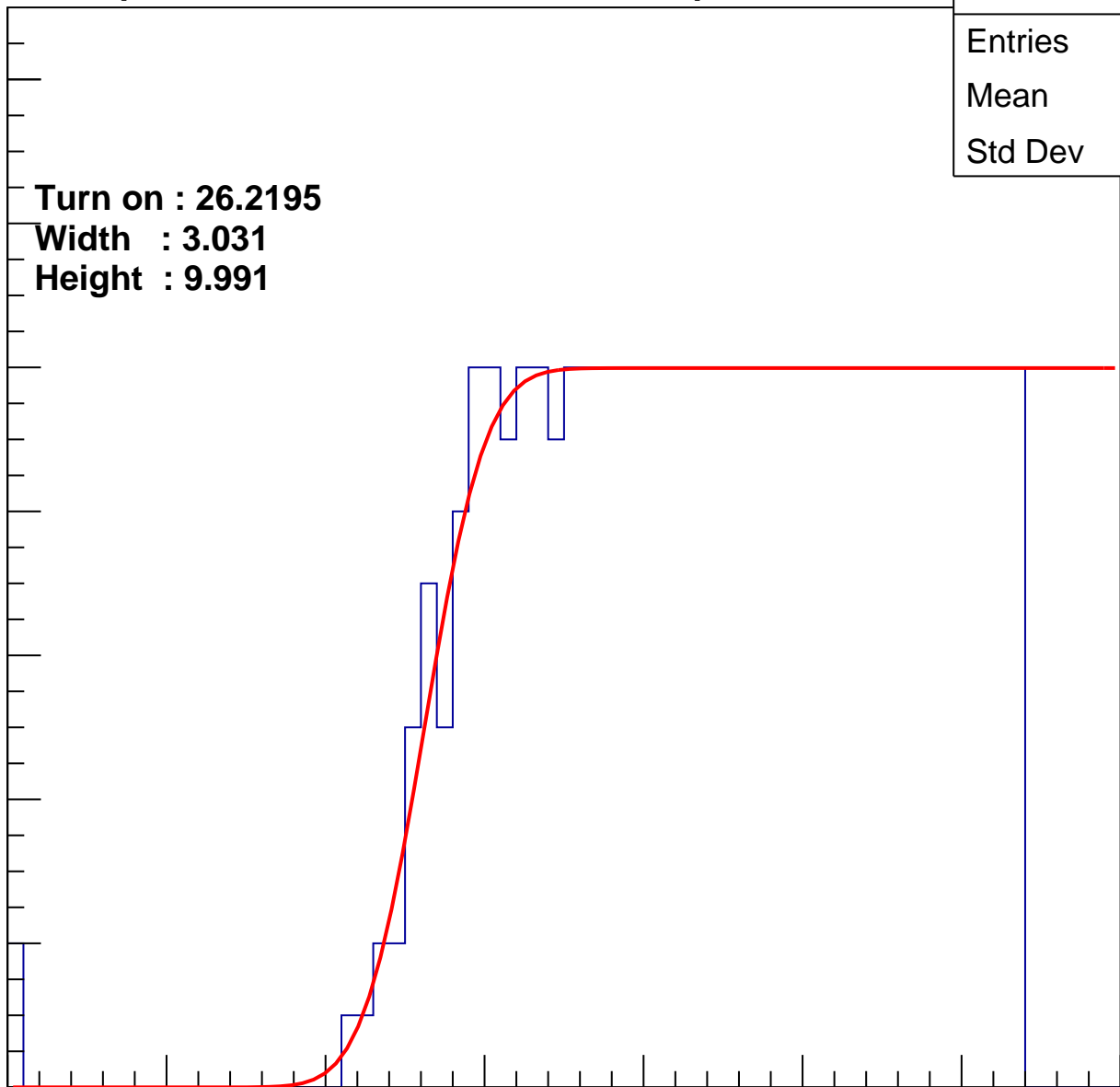
Entry

14
12
10
8
6
4
2
0

Turn on : 26.2195
Width : 3.031
Height : 9.991

Entries	381
Mean	44.19
Std Dev	11.56

ampl



B1L003S, U4-ch52

calib_packv5_042523_0143.root, FC#13, port D2

Entries	382
Mean	44.02
Std Dev	11.94

Turn on : 26.3694

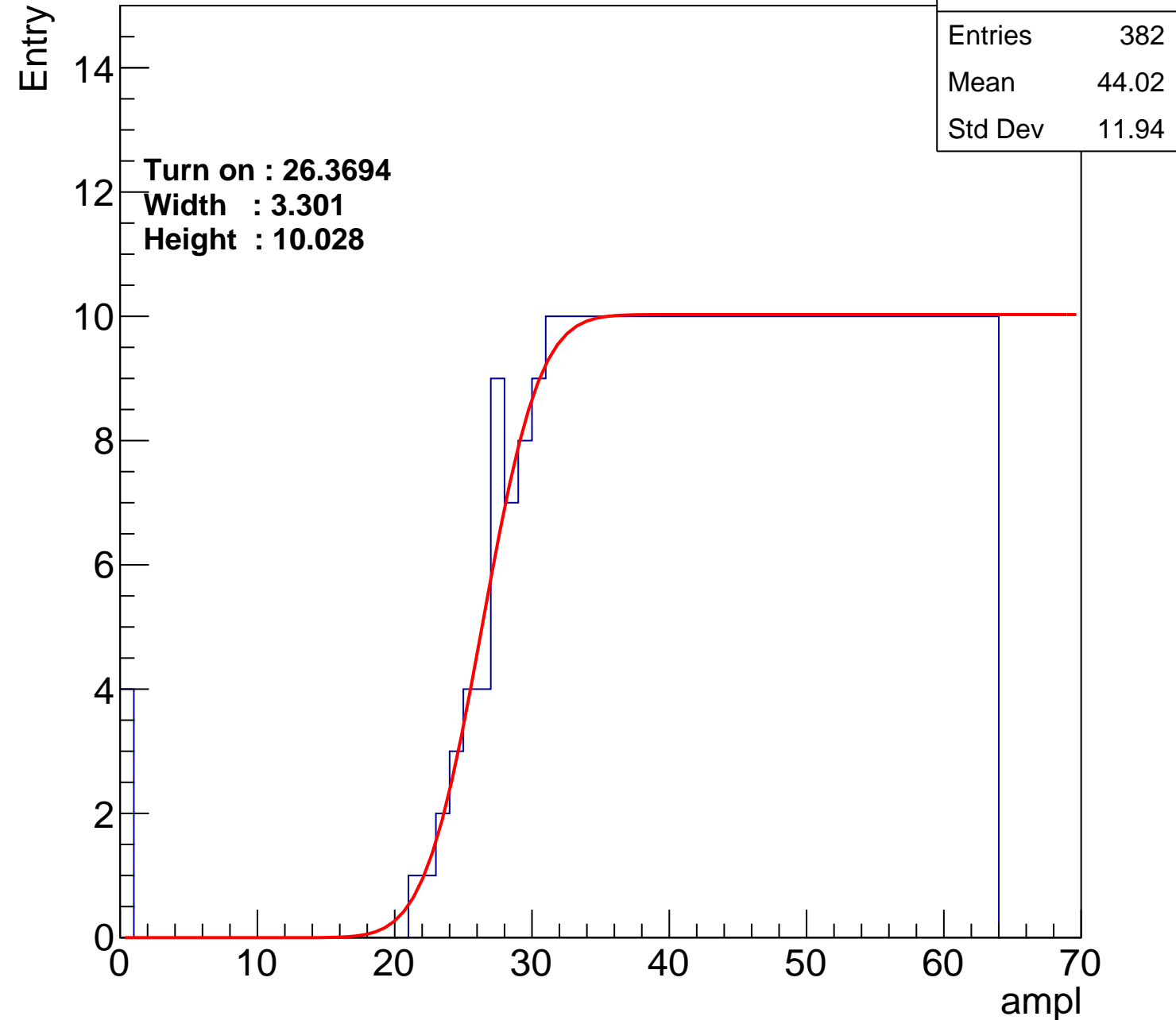
Width : 3.301

Height : 10.028

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U4-ch53

calib_packv5_042523_0143.root, FC#13, port D2

Entries	379
Mean	44.35
Std Dev	11.36

Turn on : 26.3840

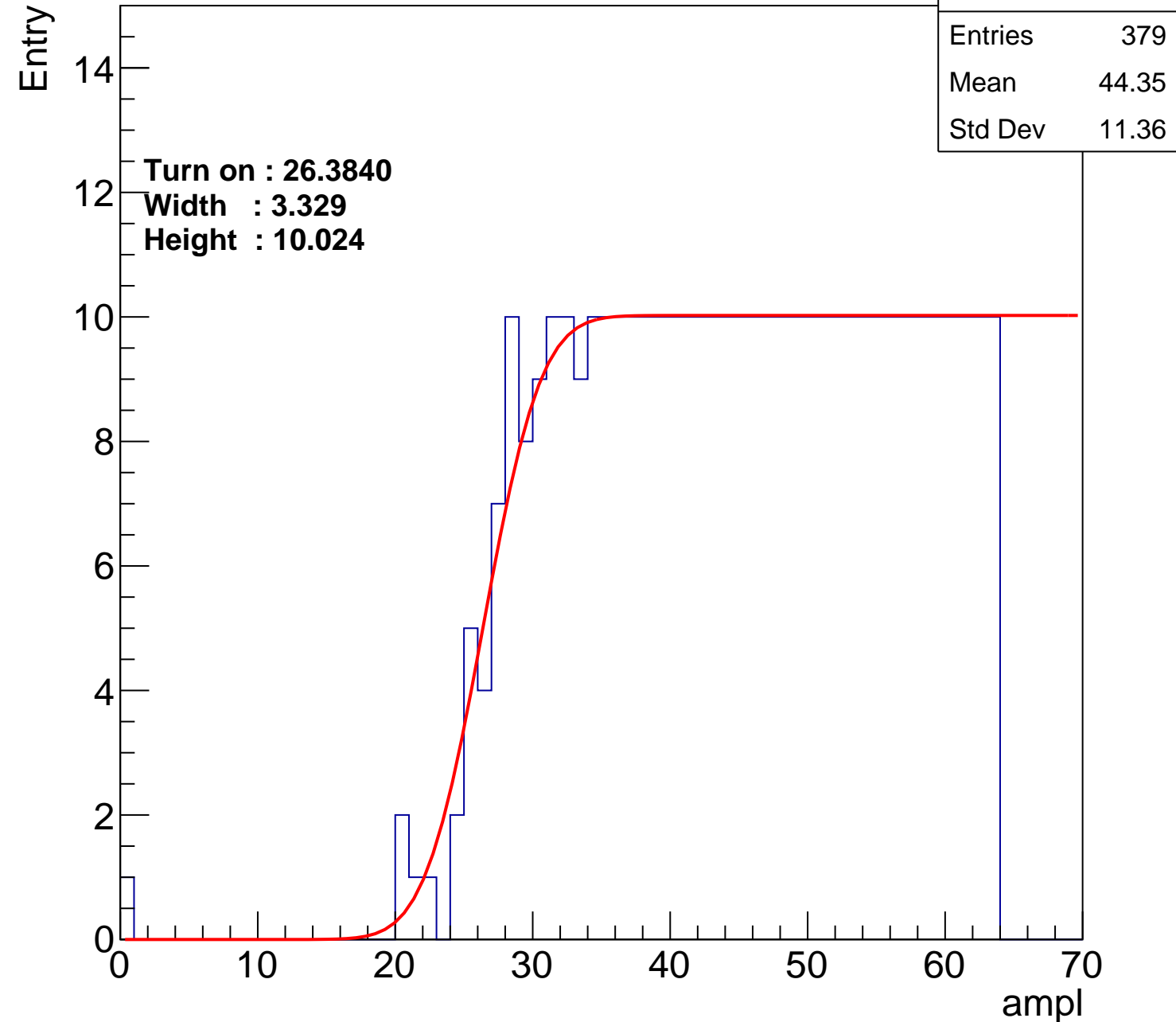
Width : 3.329

Height : 10.024

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U4-ch54

calib_packv5_042523_0143.root, FC#13, port D2

Entry

Entries 373

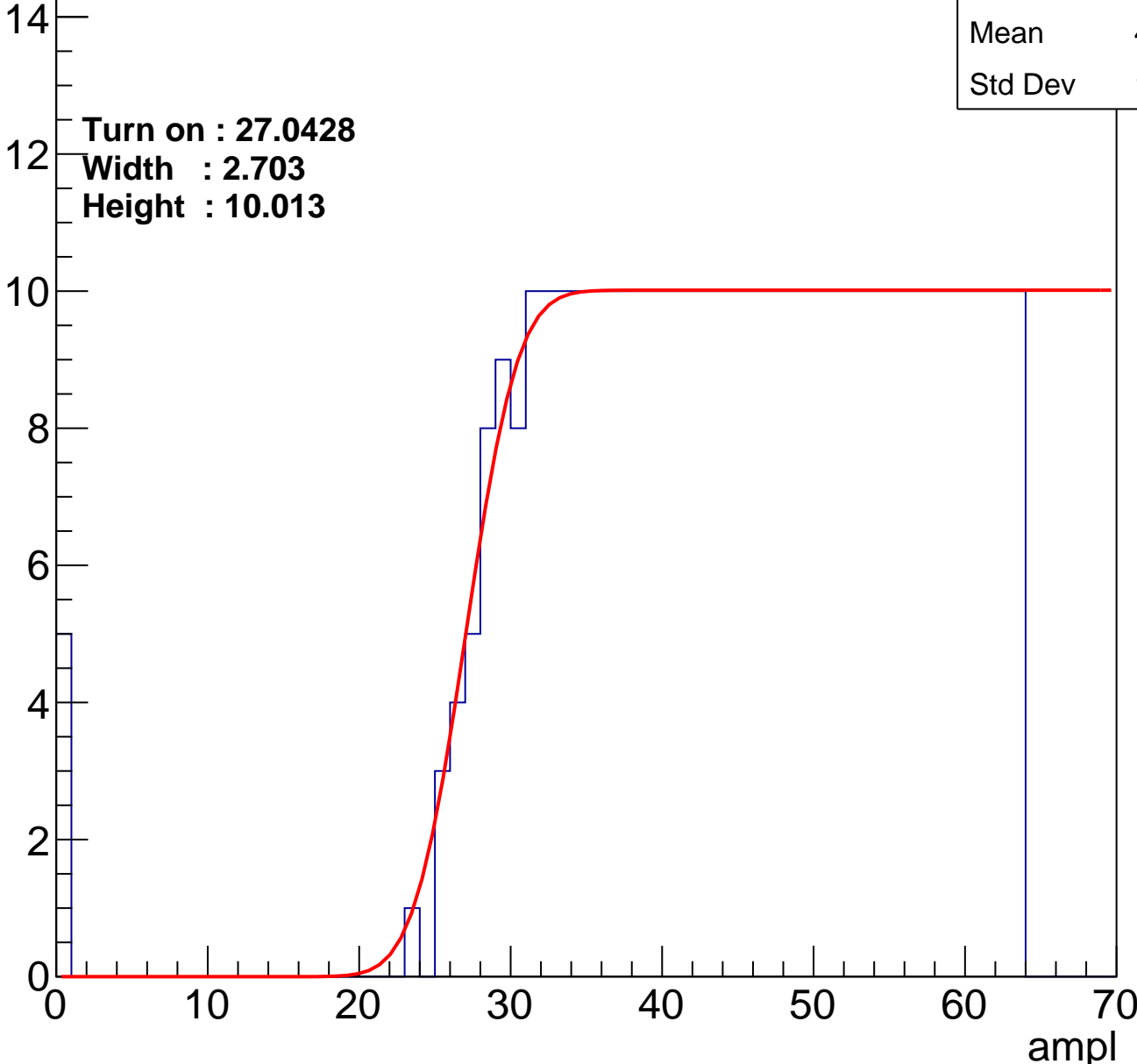
Mean 44.43

Std Dev 11.85

Turn on : 27.0428

Width : 2.703

Height : 10.013



B1L003S, U4-ch55

calib_packv5_042523_0143.root, FC#13, port D2

Entries	380
Mean	44.23
Std Dev	11.64

Turn on : 26.4185

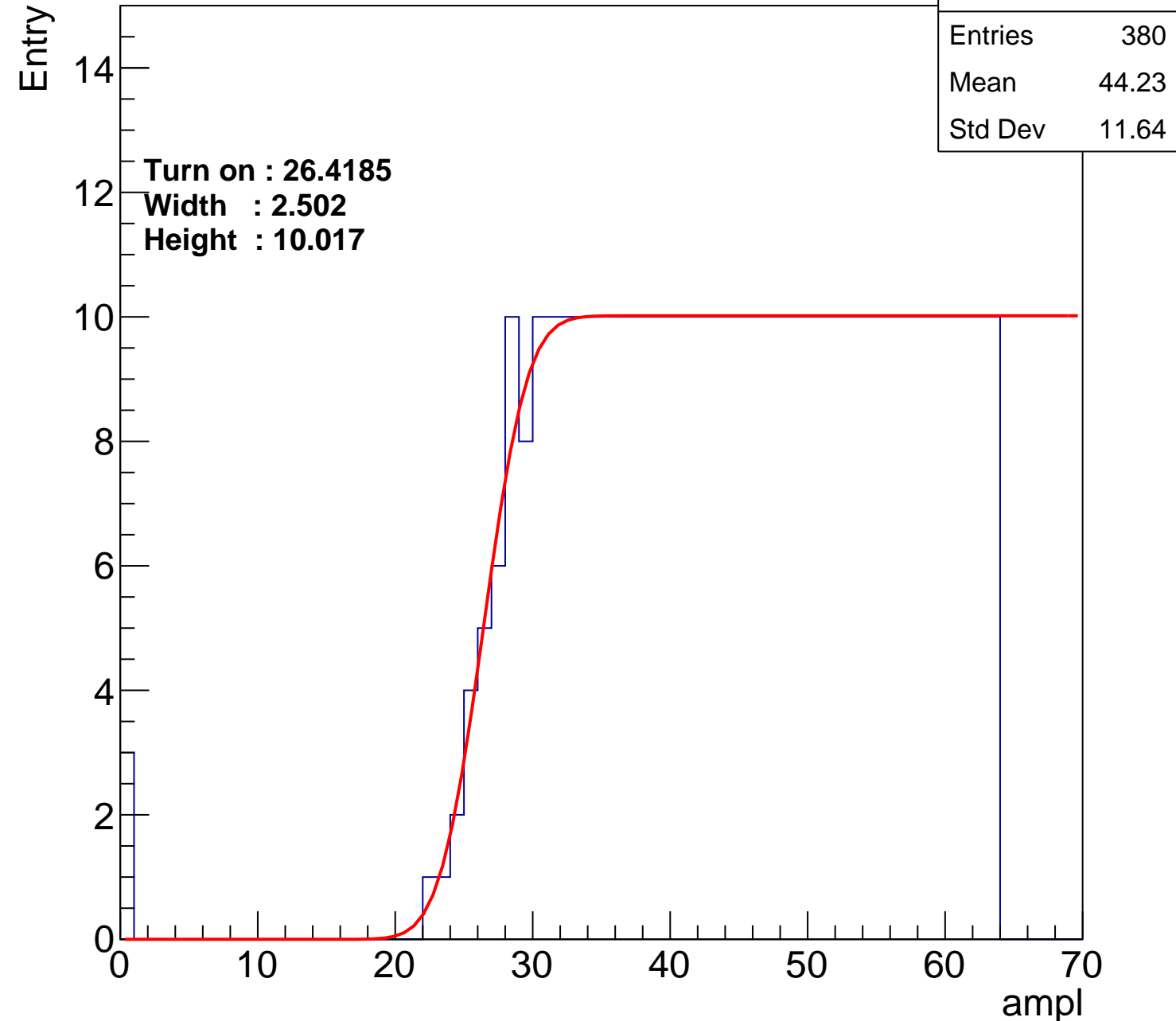
Width : 2.502

Height : 10.017

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U4-ch56

calib_packv5_042523_0143.root, FC#13, port D2

Entries	397
Mean	43.47
Std Dev	11.83

Turn on : 24.7337

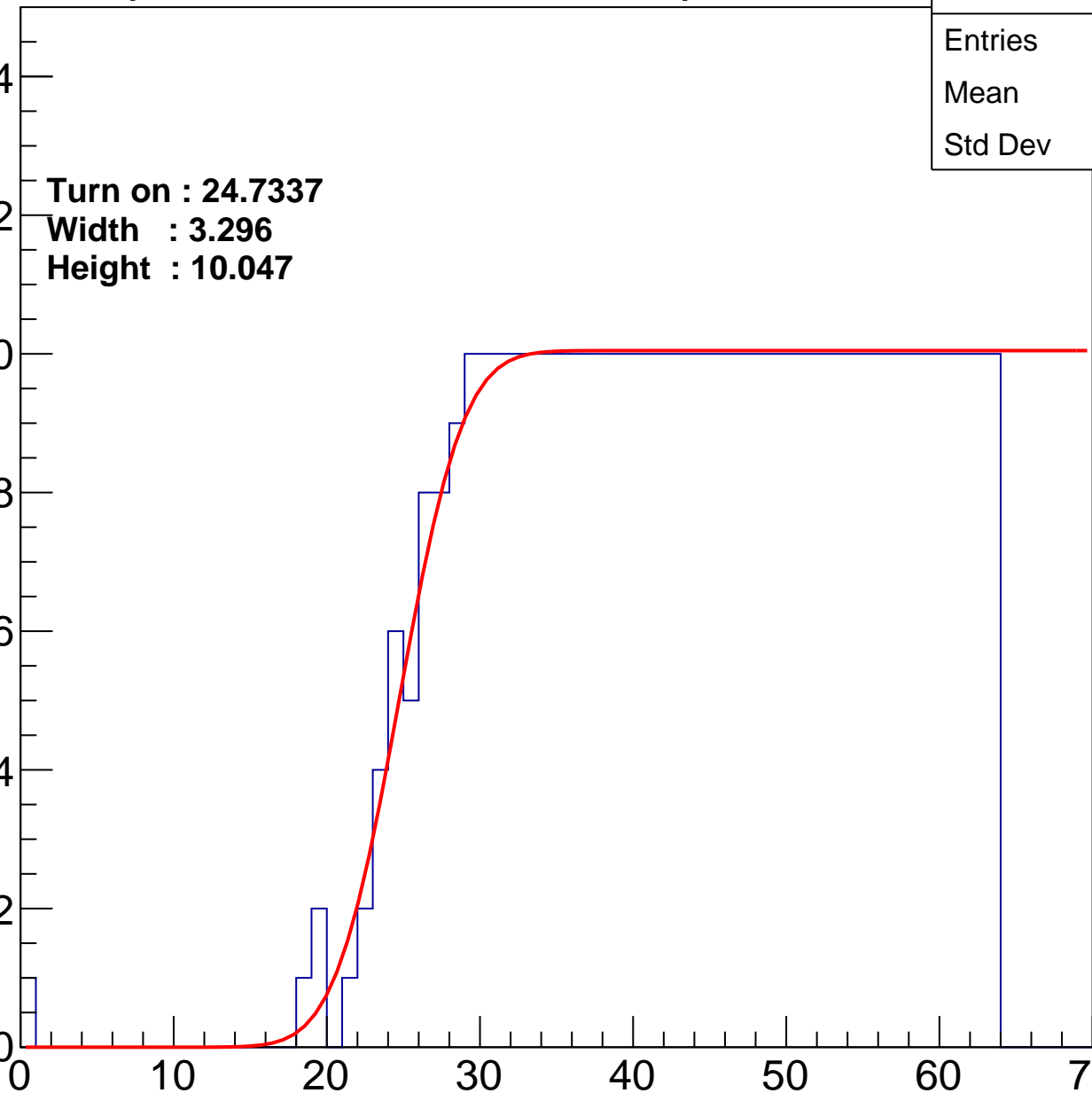
Width : 3.296

Height : 10.047

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U4-ch57

calib_packv5_042523_0143.root, FC#13, port D2

Entries	369
Mean	44.63
Std Dev	11.67

Turn on : 27.6335

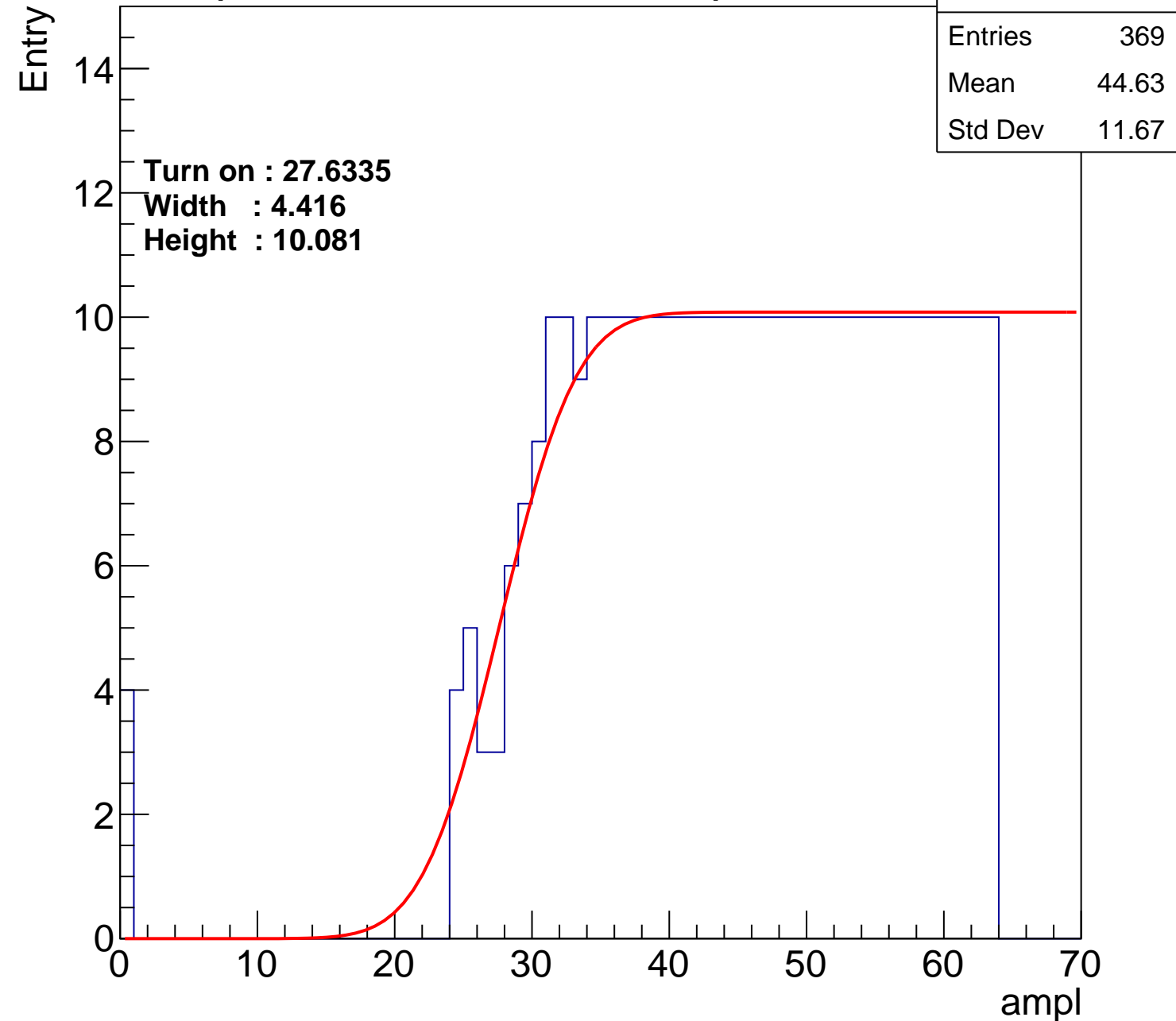
Width : 4.416

Height : 10.081

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U4-ch58

calib_packv5_042523_0143.root, FC#13, port D2

Entries	373
Mean	44.53
Std Dev	11.54

Turn on : 26.9027

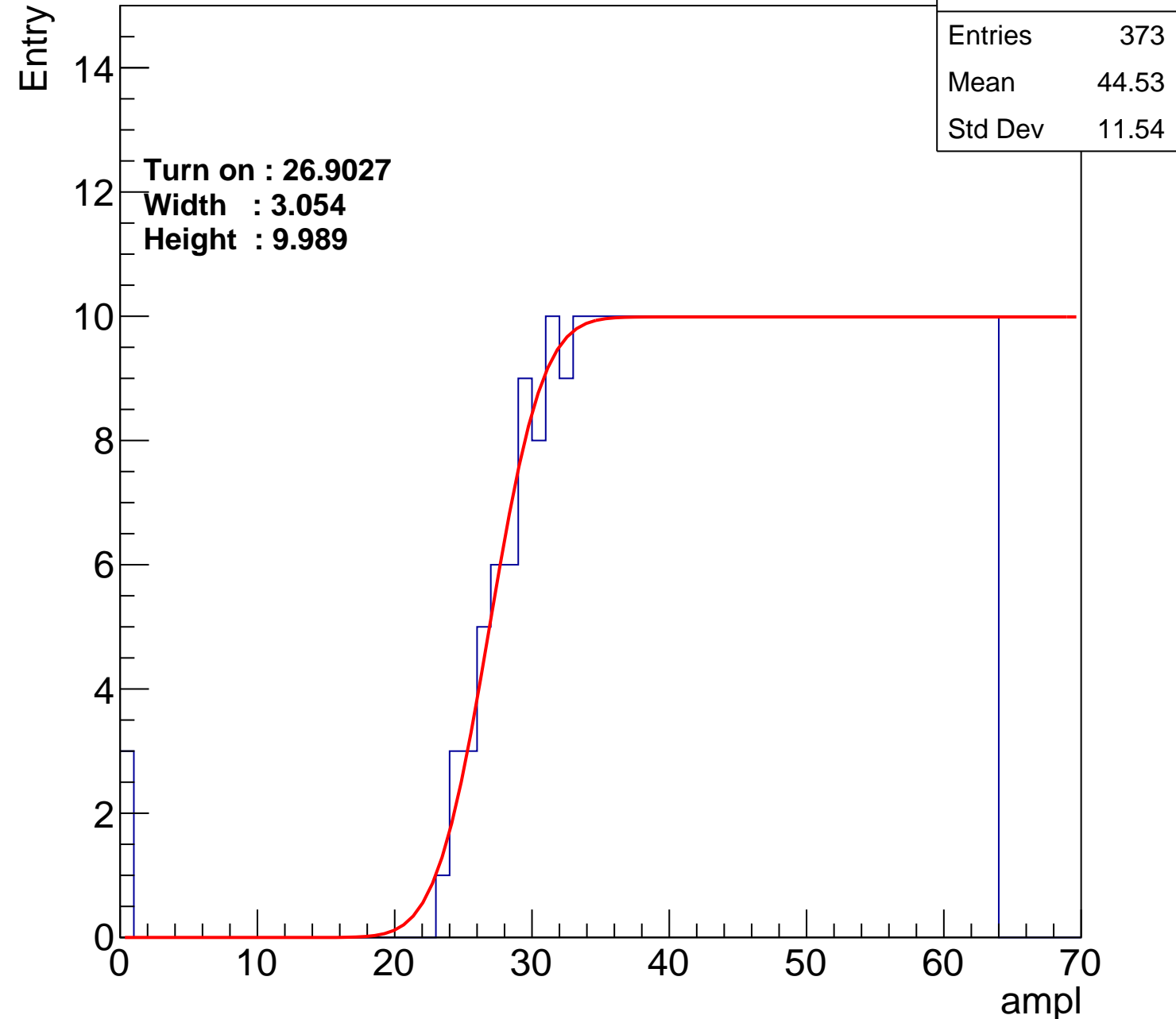
Width : 3.054

Height : 9.989

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U4-ch59

calib_packv5_042523_0143.root, FC#13, port D2

Entries	375
Mean	44.4
Std Dev	11.72

Turn on : 27.1898

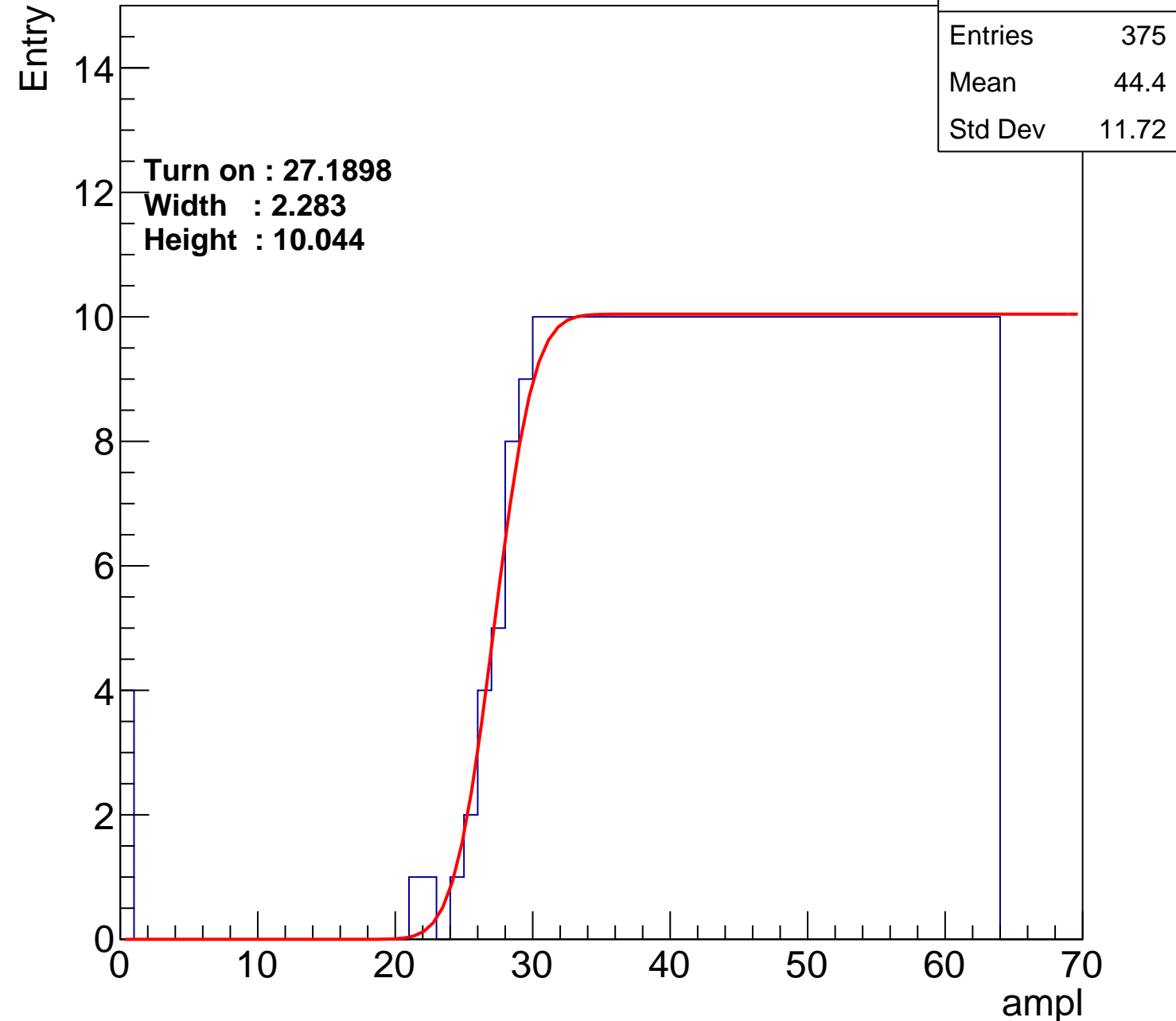
Width : 2.283

Height : 10.044

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U4-ch60

calib_packv5_042523_0143.root, FC#13, port D2

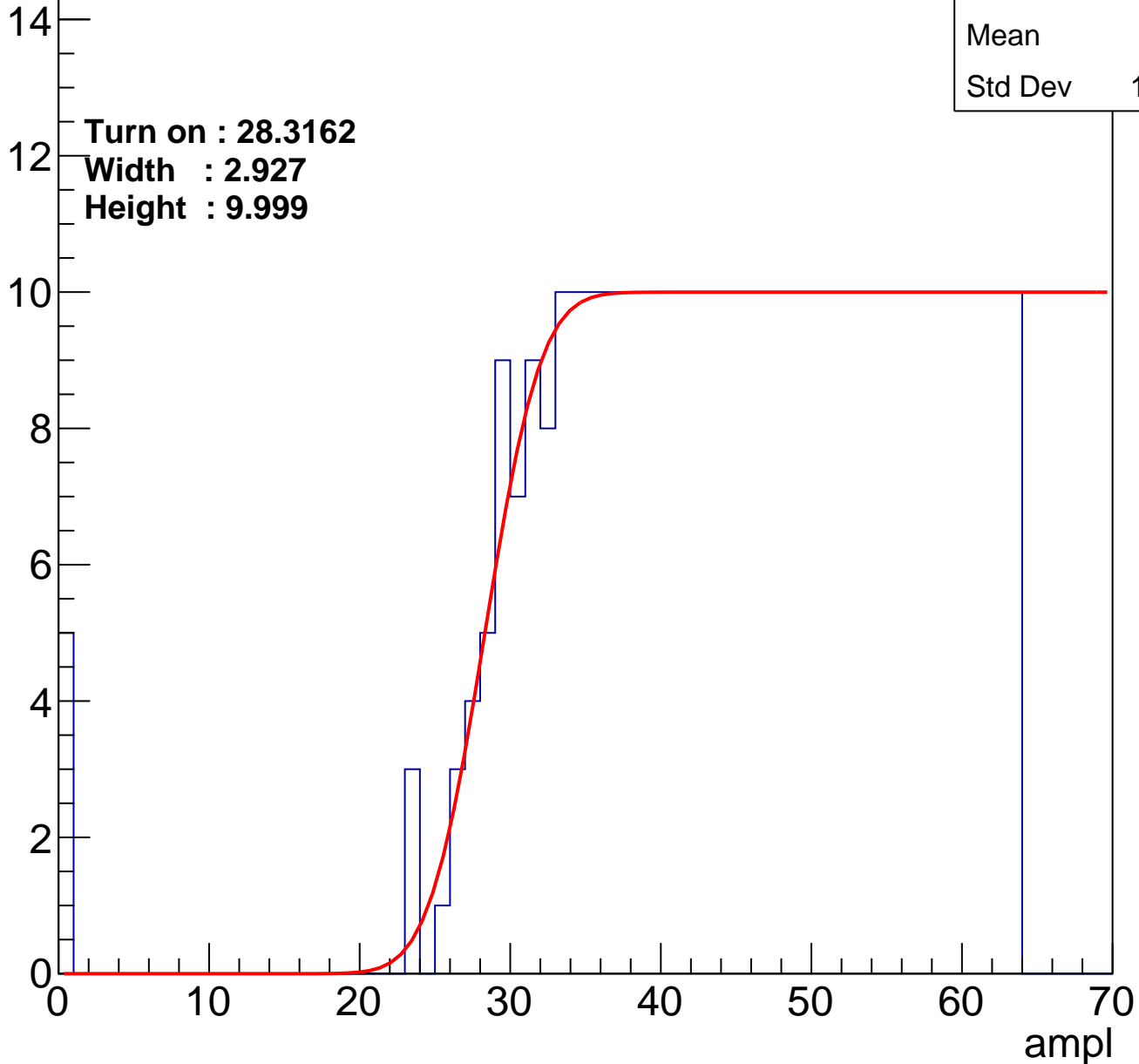
Entries	364
Mean	44.8
Std Dev	11.76

Turn on : 28.3162

Width : 2.927

Height : 9.999

Entry



B1L003S, U4-ch61

calib_packv5_042523_0143.root, FC#13, port D2

Entries	364
Mean	44.75
Std Dev	11.92

Turn on : 28.4646

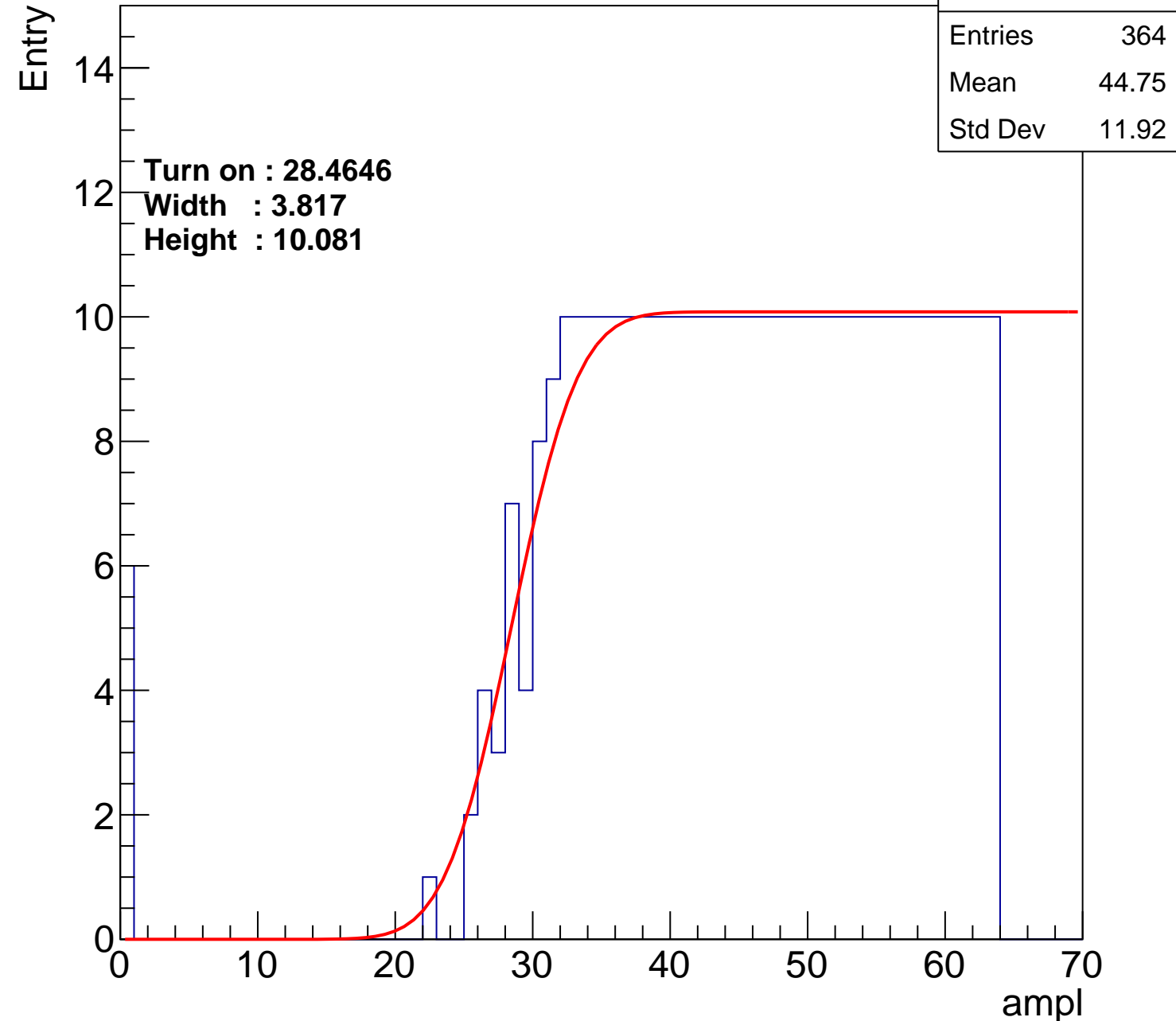
Width : 3.817

Height : 10.081

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U4-ch62

calib_packv5_042523_0143.root, FC#13, port D2

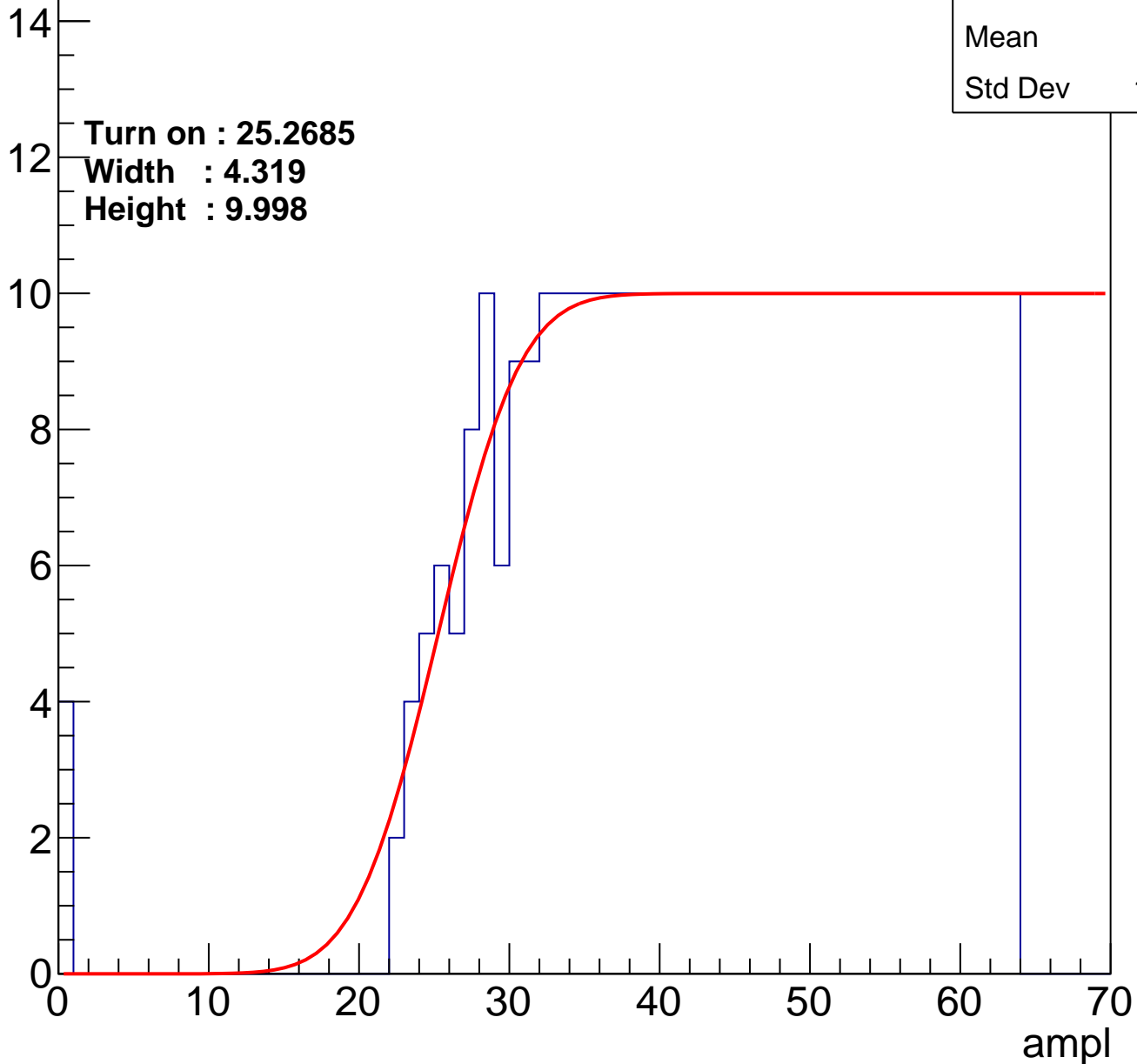
Entries	388
Mean	43.7
Std Dev	12.11

Turn on : 25.2685

Width : 4.319

Height : 9.998

Entry



B1L003S, U4-ch63

calib_packv5_042523_0143.root, FC#13, port D2

Entries	372
Mean	44.49
Std Dev	11.72

Turn on : 26.8185

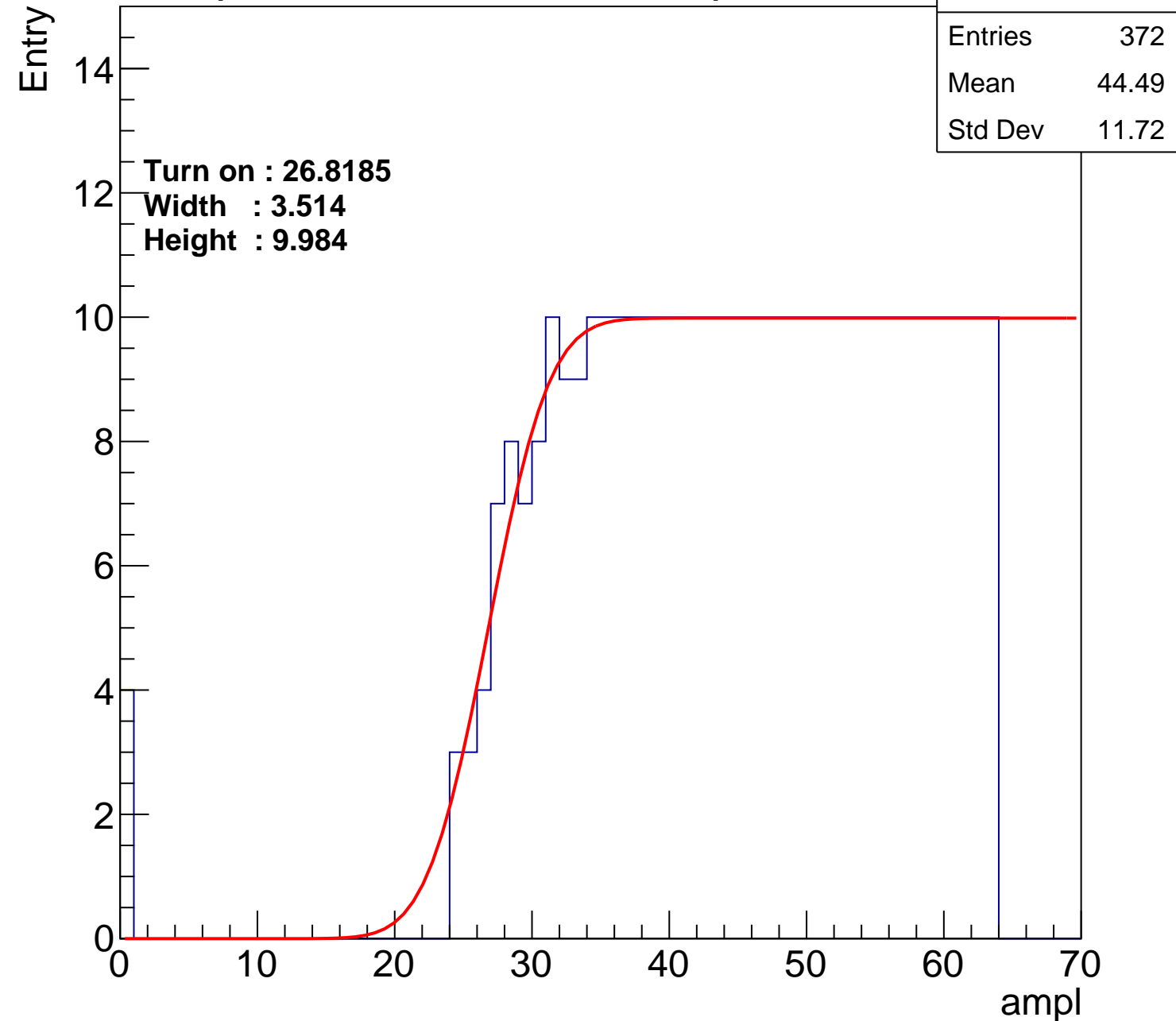
Width : 3.514

Height : 9.984

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U4-ch64

calib_packv5_042523_0143.root, FC#13, port D2

Entries	372
Mean	44.45
Std Dev	11.87

Turn on : 27.5785

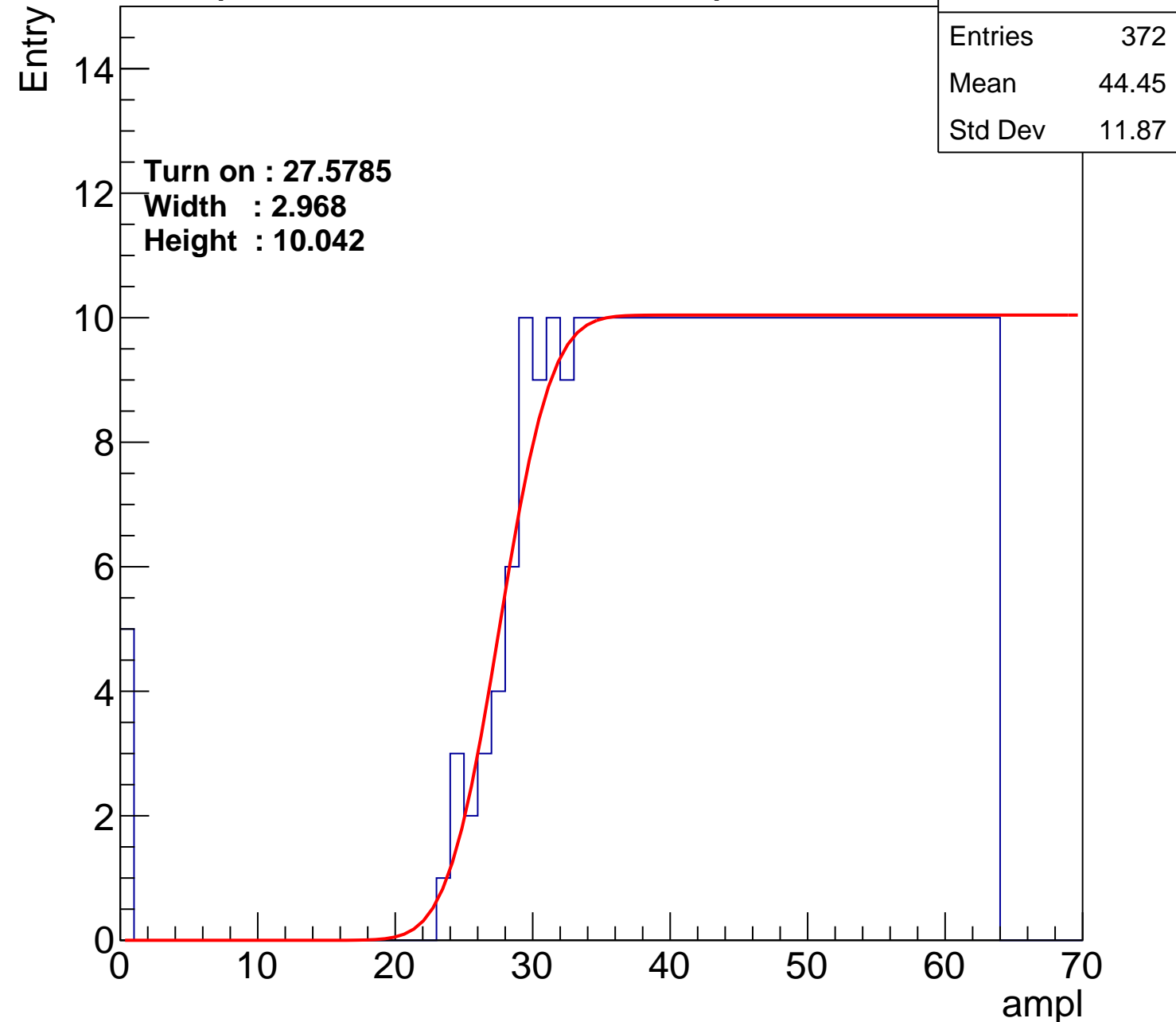
Width : 2.968

Height : 10.042

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U4-ch65

calib_packv5_042523_0143.root, FC#13, port D2

Entries	399
Mean	43.27
Std Dev	12.22

Turn on : 24.5325

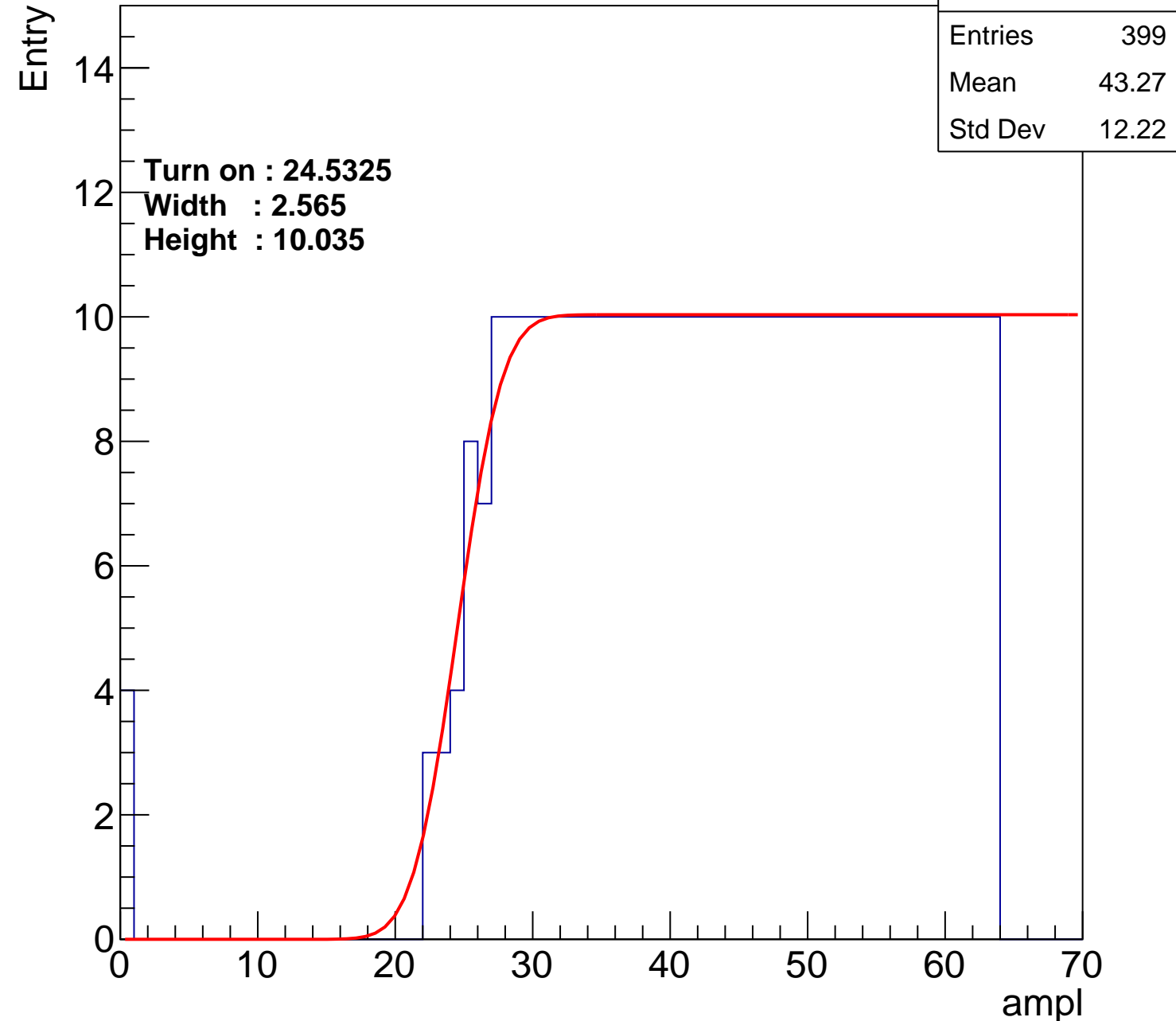
Width : 2.565

Height : 10.035

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U4-ch66

calib_packv5_042523_0143.root, FC#13, port D2

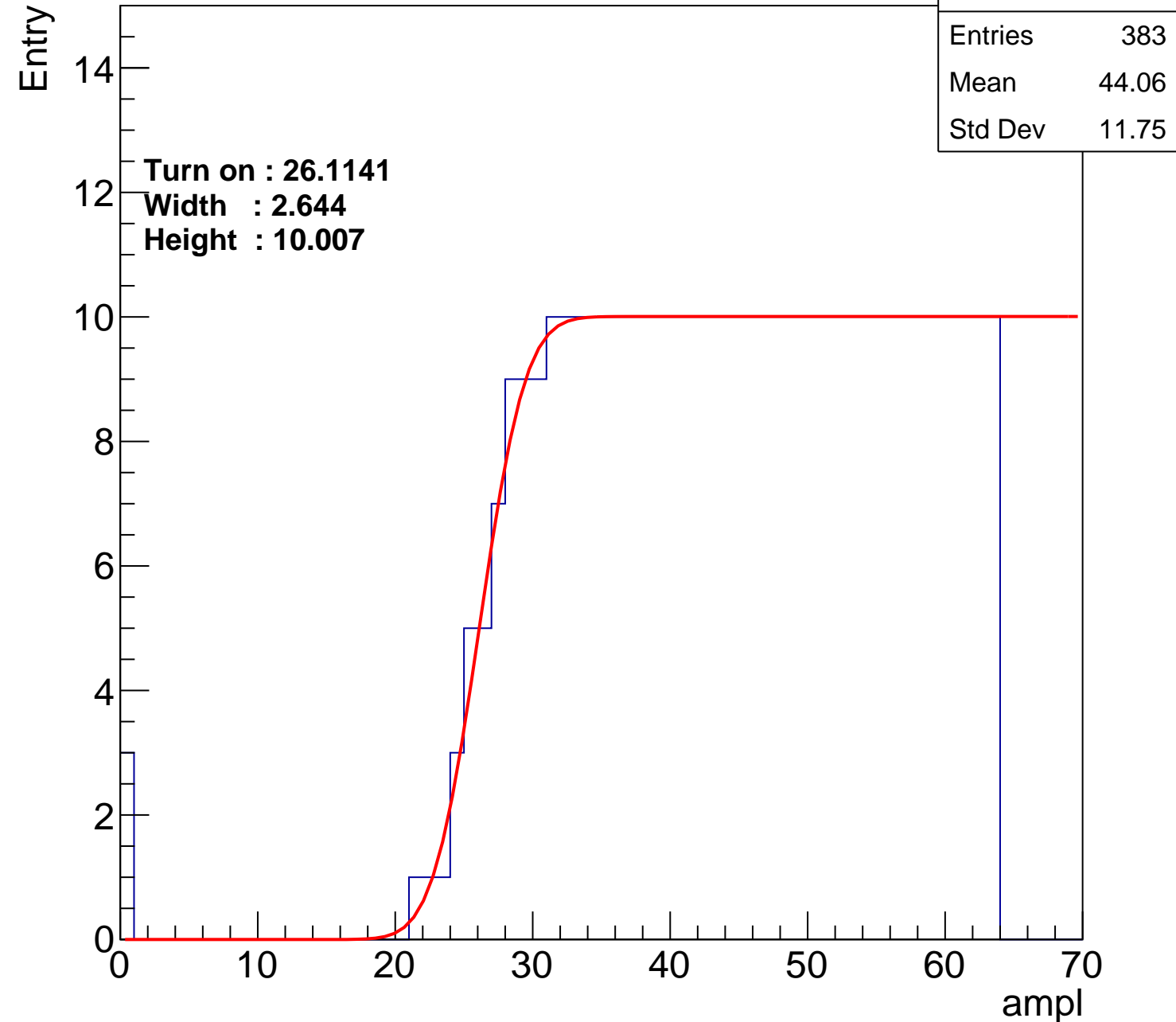
Entry

14
12
10
8
6
4
2
0

Turn on : 26.1141
Width : 2.644
Height : 10.007

Entries	383
Mean	44.06
Std Dev	11.75

ampl



B1L003S, U4-ch67

calib_packv5_042523_0143.root, FC#13, port D2

Entries	364
Mean	44.85
Std Dev	11.6

Turn on : 28.6995

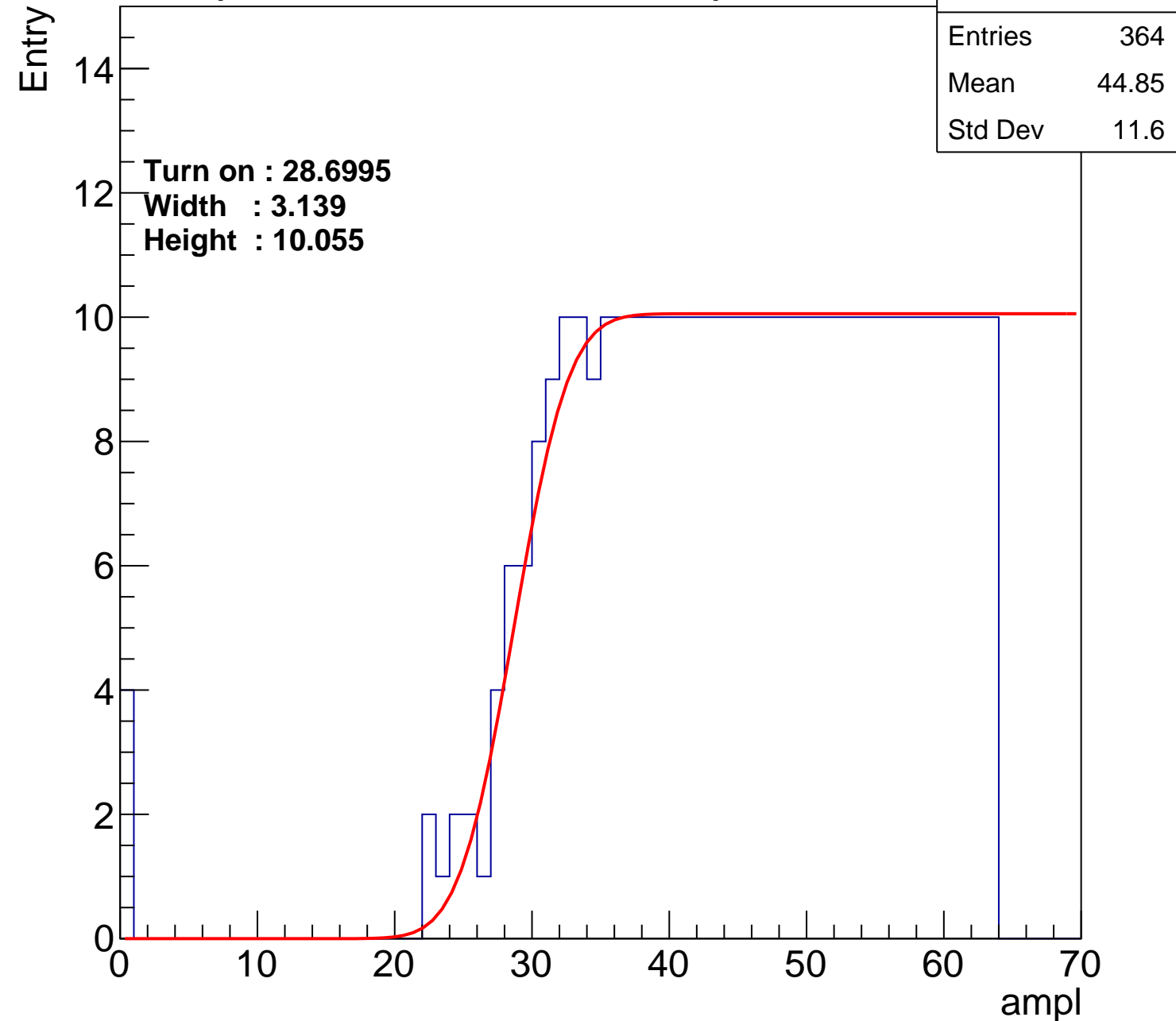
Width : 3.139

Height : 10.055

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U4-ch68

calib_packv5_042523_0143.root, FC#13, port D2

Entries	386
Mean	43.91
Std Dev	11.83

Turn on : 26.4591

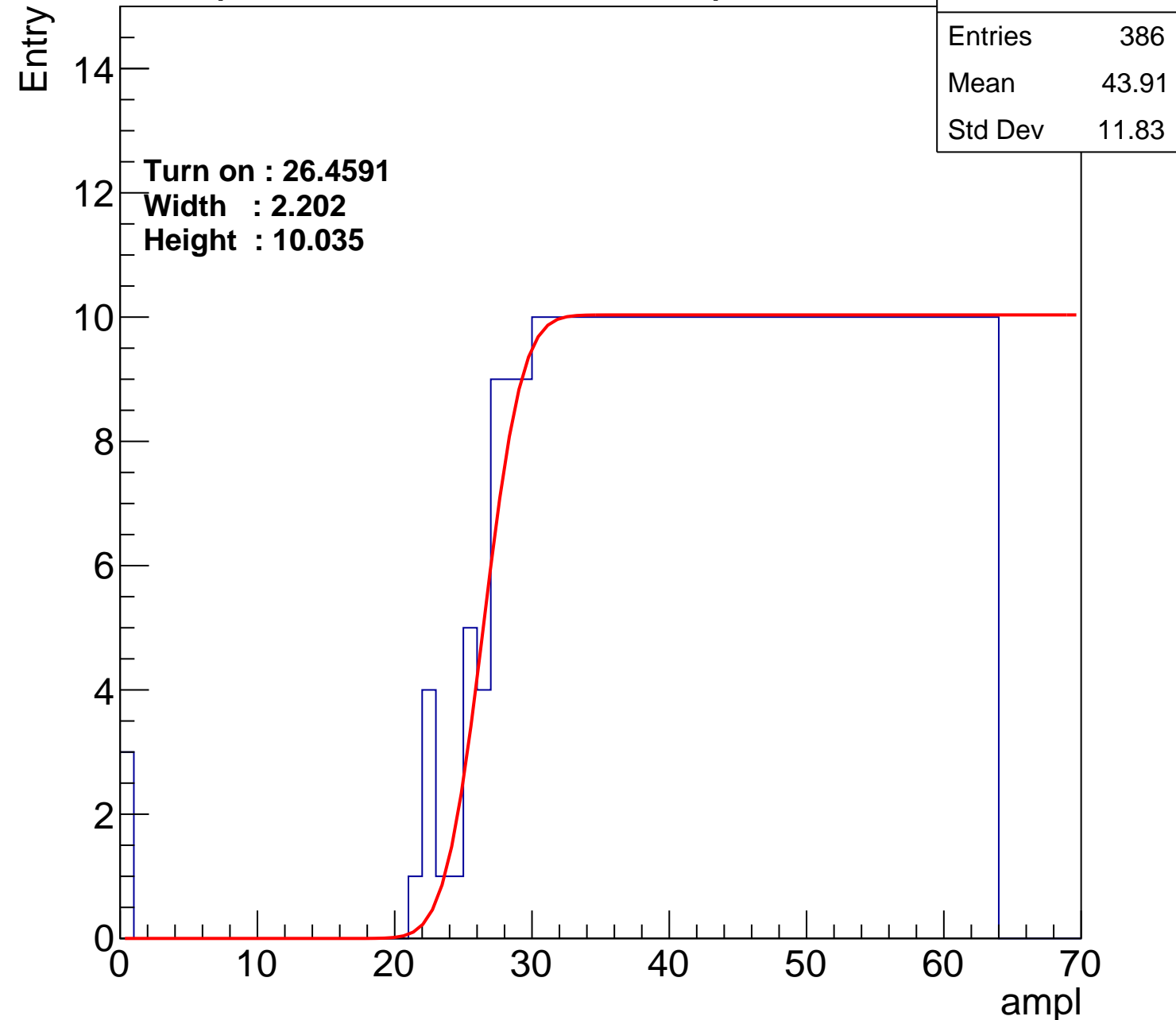
Width : 2.202

Height : 10.035

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U4-ch69

calib_packv5_042523_0143.root, FC#13, port D2

Entries	379
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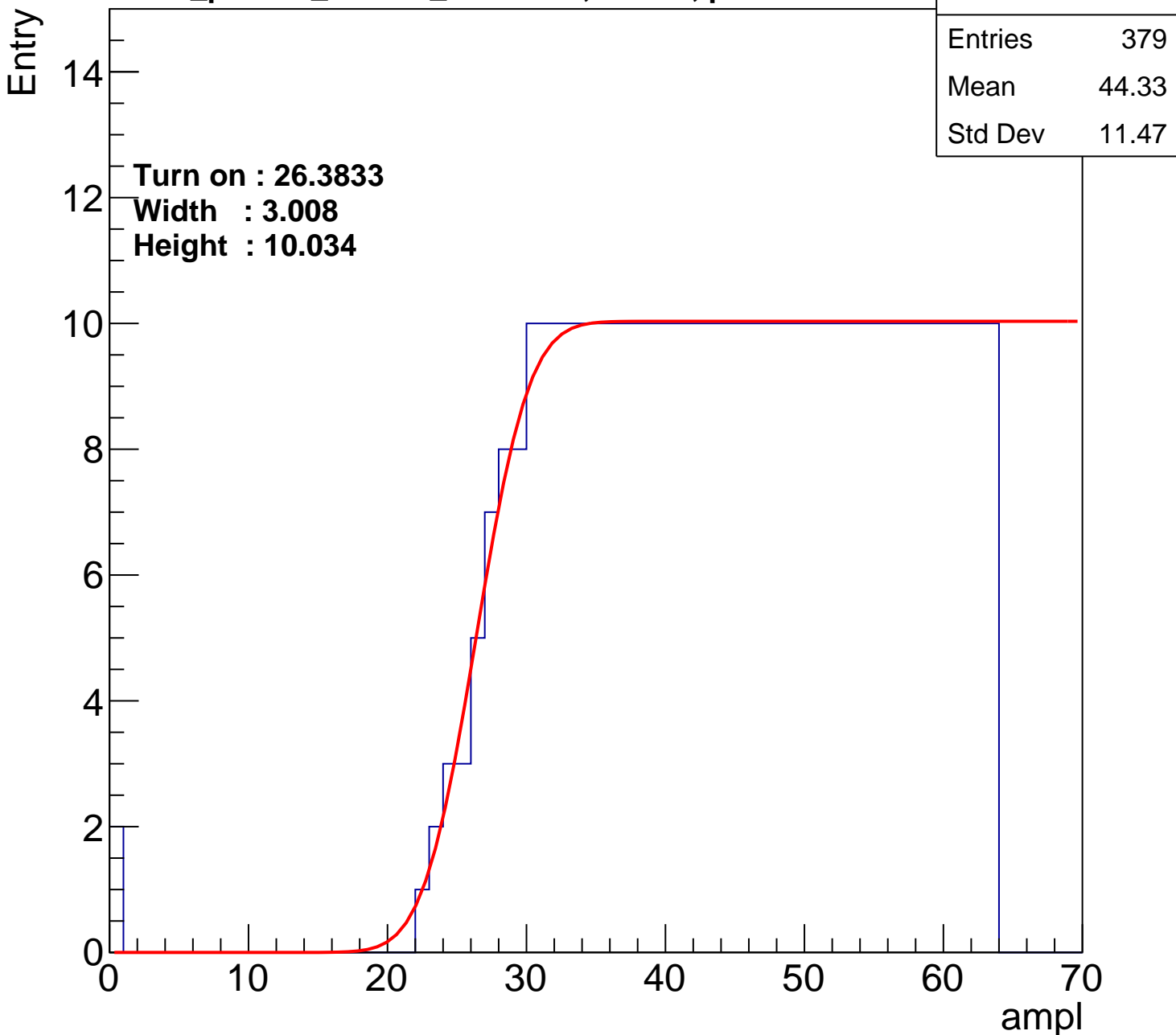
Mean	44.33
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Std Dev	11.47
---------	-------

Turn on : 26.3833

Width : 3.008

Height : 10.034



B1L003S, U4-ch70

calib_packv5_042523_0143.root, FC#13, port D2

Entries	385
Mean	43.88
Std Dev	11.92

Turn on : 26.0902

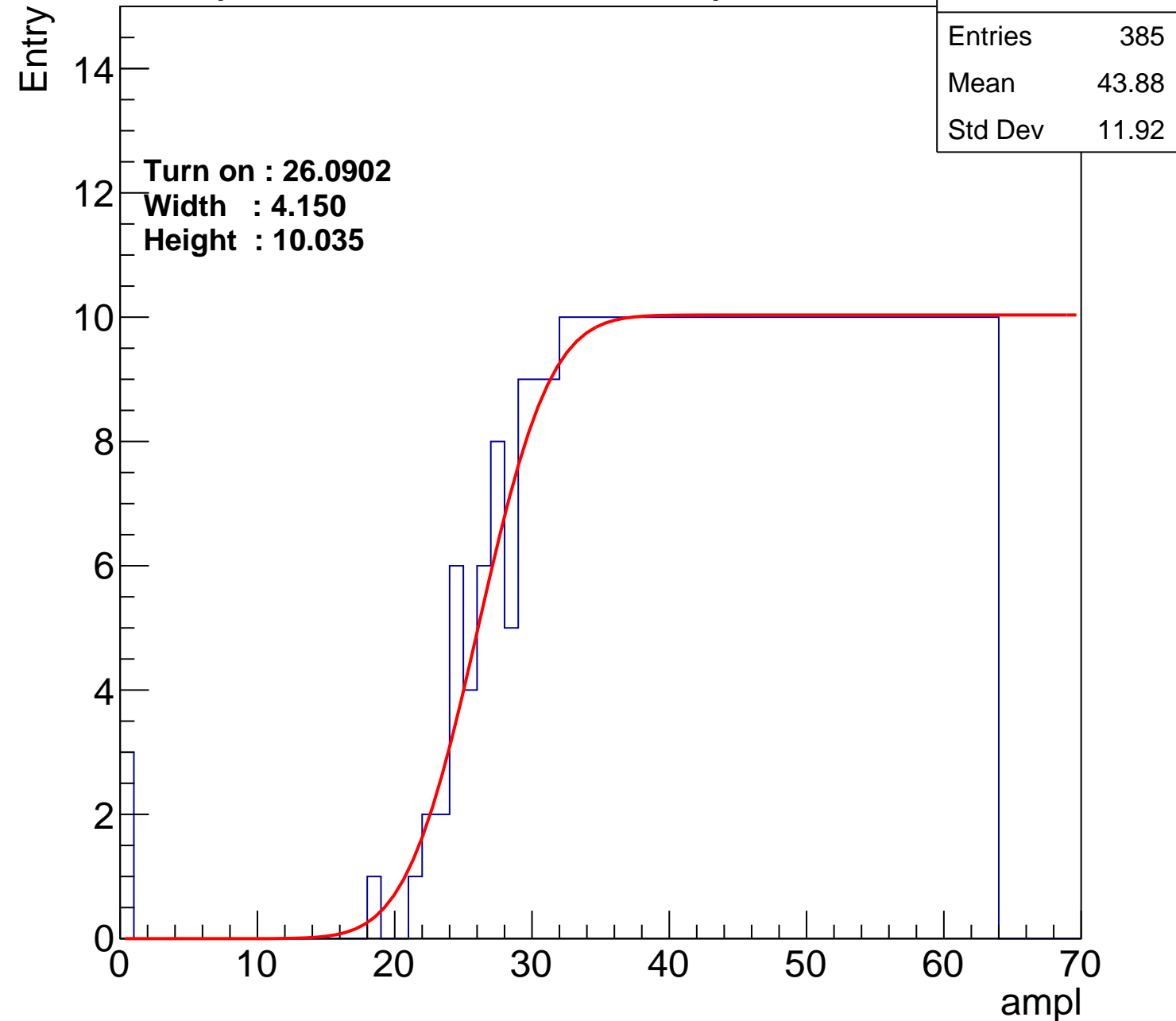
Width : 4.150

Height : 10.035

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U4-ch71

calib_packv5_042523_0143.root, FC#13, port D2

Entries	362
Mean	45.07
Std Dev	11.27

Turn on : 28.4284

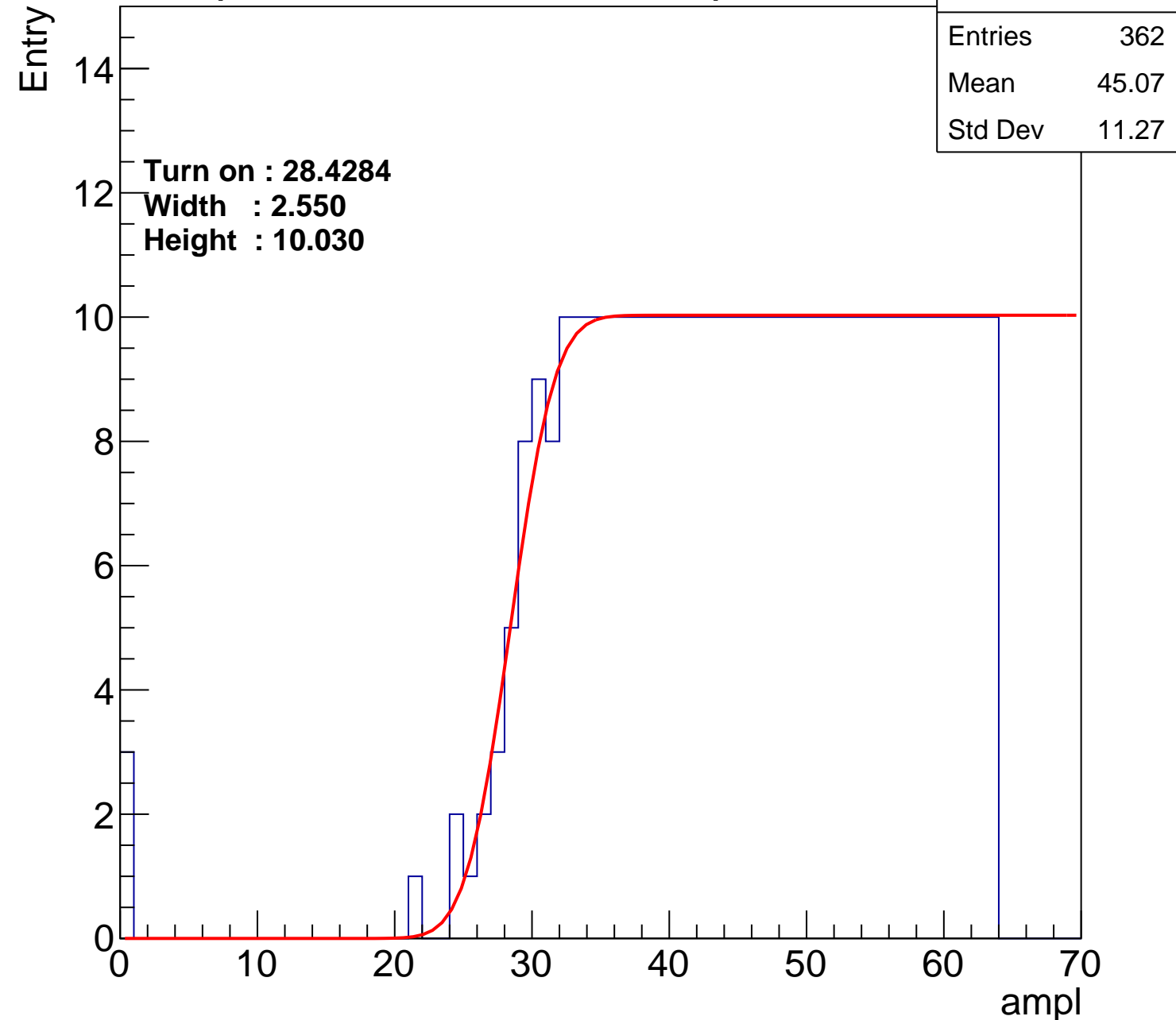
Width : 2.550

Height : 10.030

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U4-ch72

calib_packv5_042523_0143.root, FC#13, port D2

Entries	391
Mean	43.62
Std Dev	12.03

Turn on : 25.2712

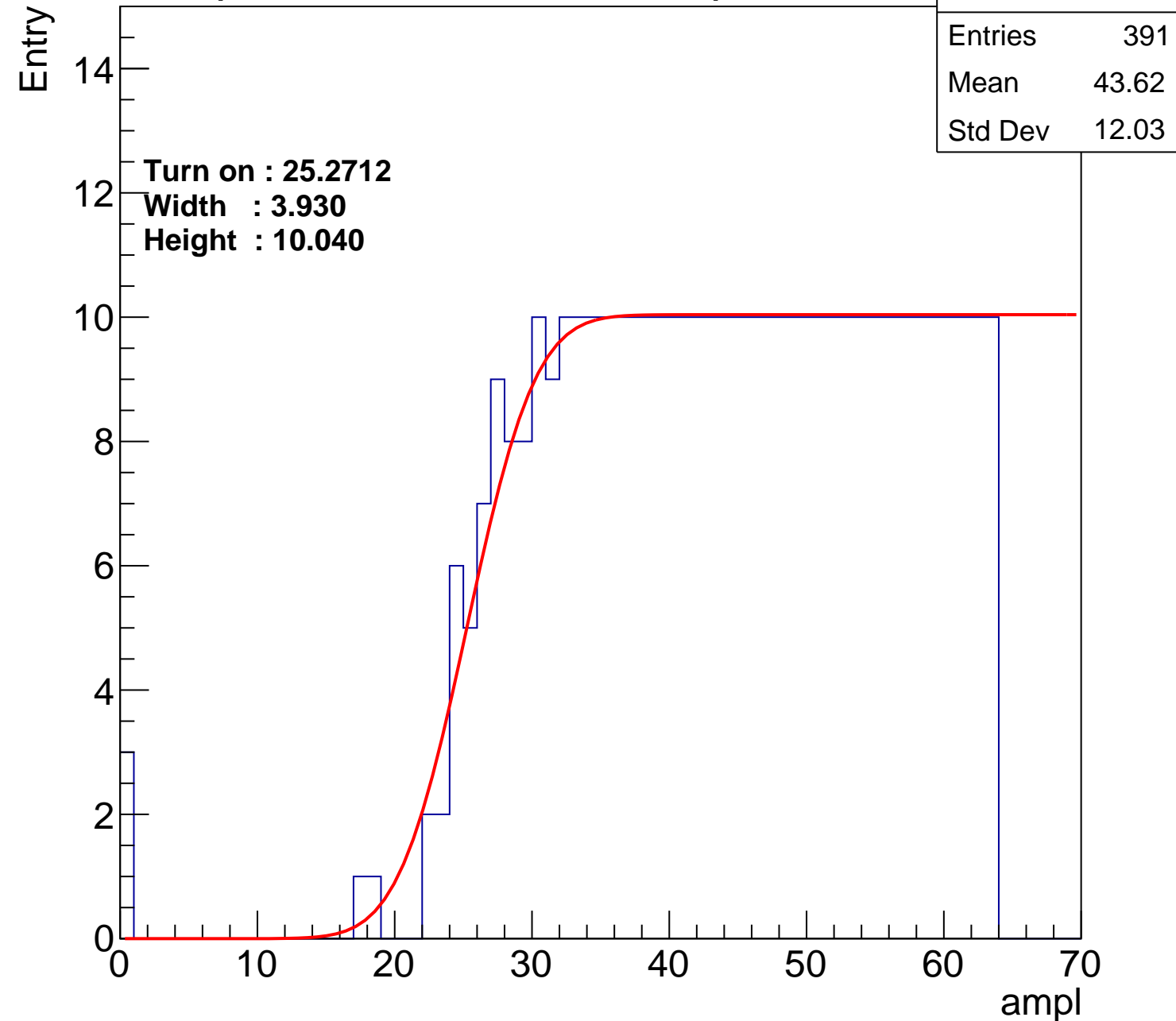
Width : 3.930

Height : 10.040

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U4-ch73

calib_packv5_042523_0143.root, FC#13, port D2

Entries	362
Mean	45.21
Std Dev	10.87

Turn on : 28.0021

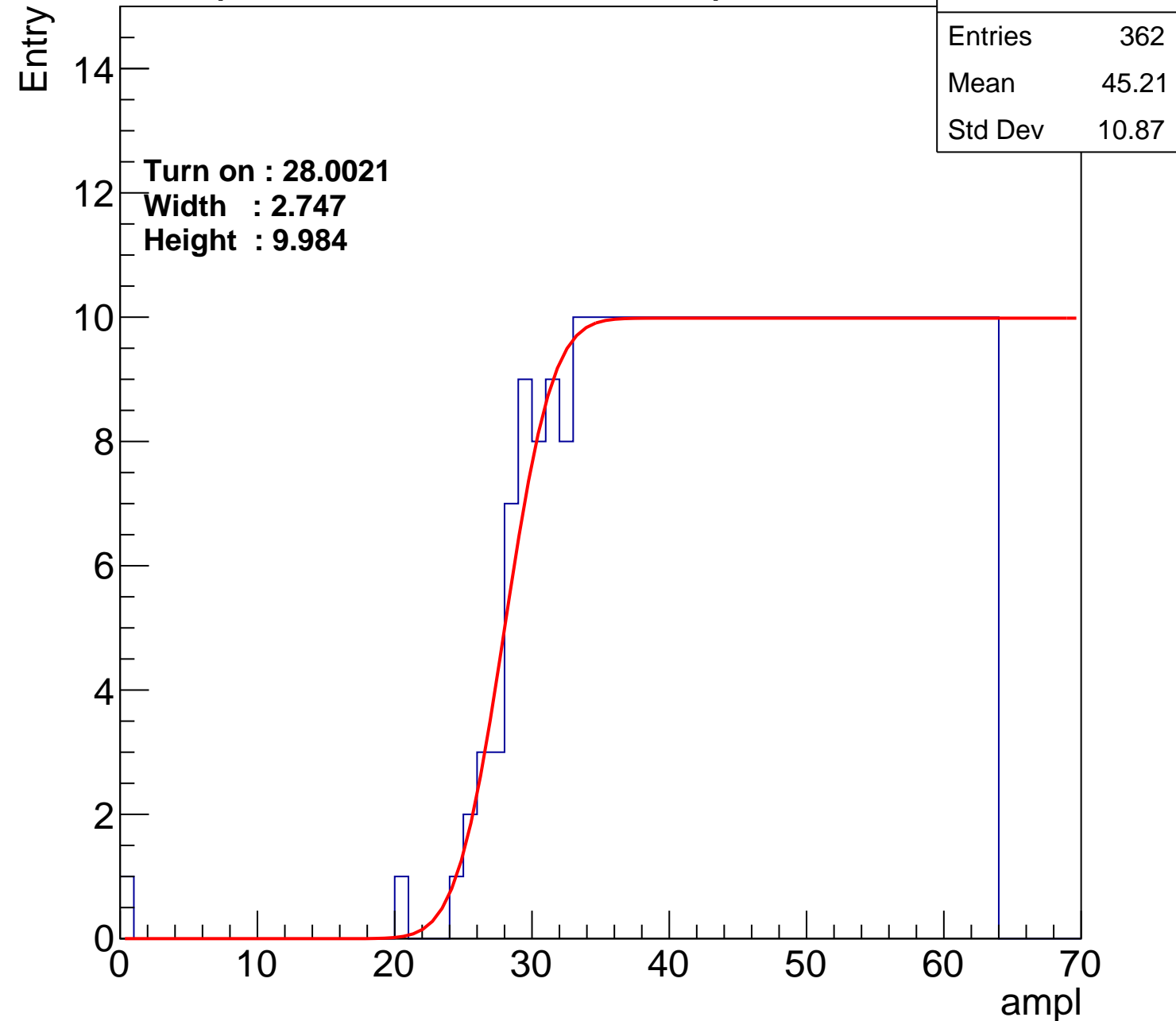
Width : 2.747

Height : 9.984

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U4-ch74

calib_packv5_042523_0143.root, FC#13, port D2

Entries	388
Mean	43.66
Std Dev	12.25

Turn on : 26.1461

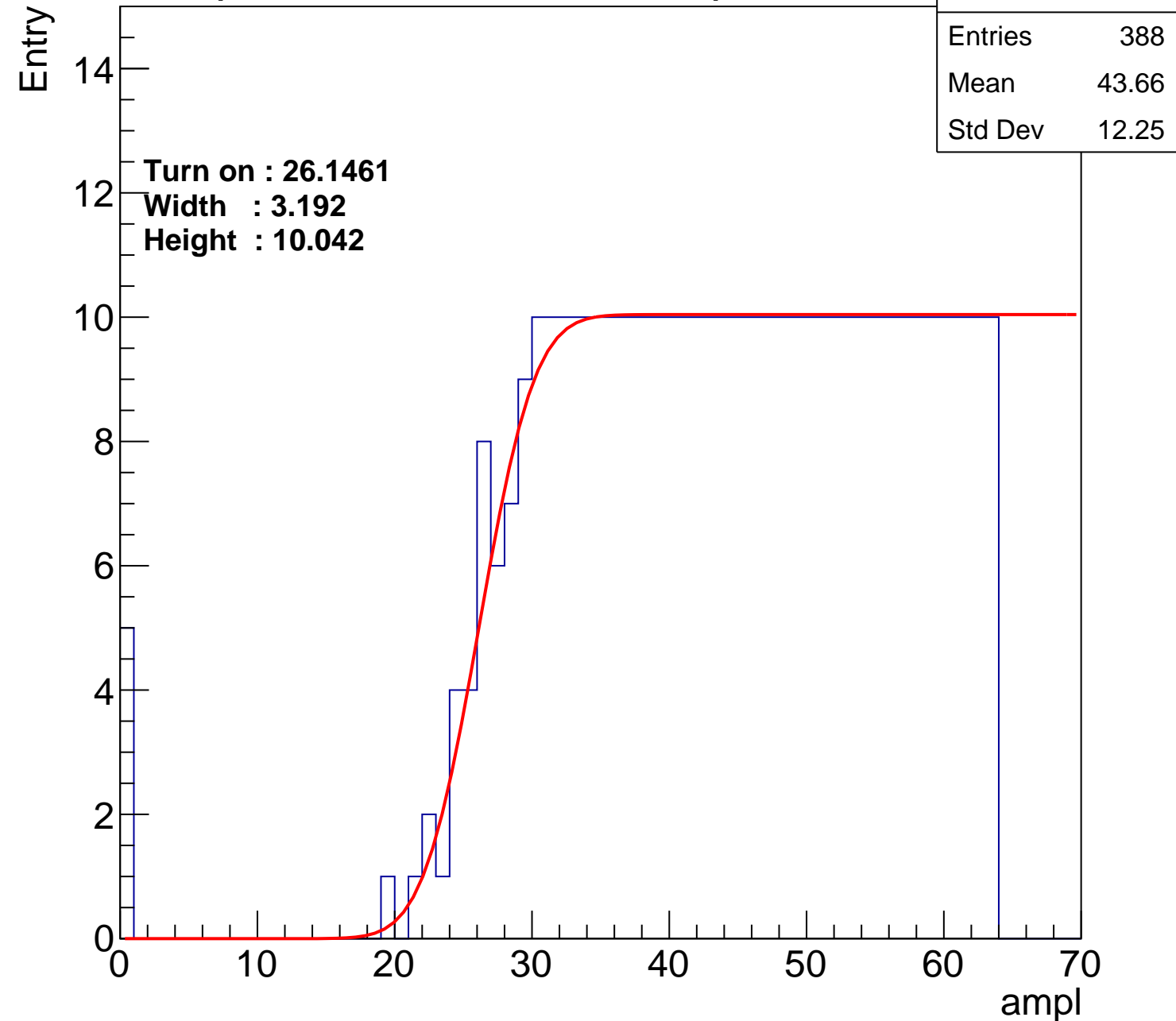
Width : 3.192

Height : 10.042

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U4-ch75

calib_packv5_042523_0143.root, FC#13, port D2

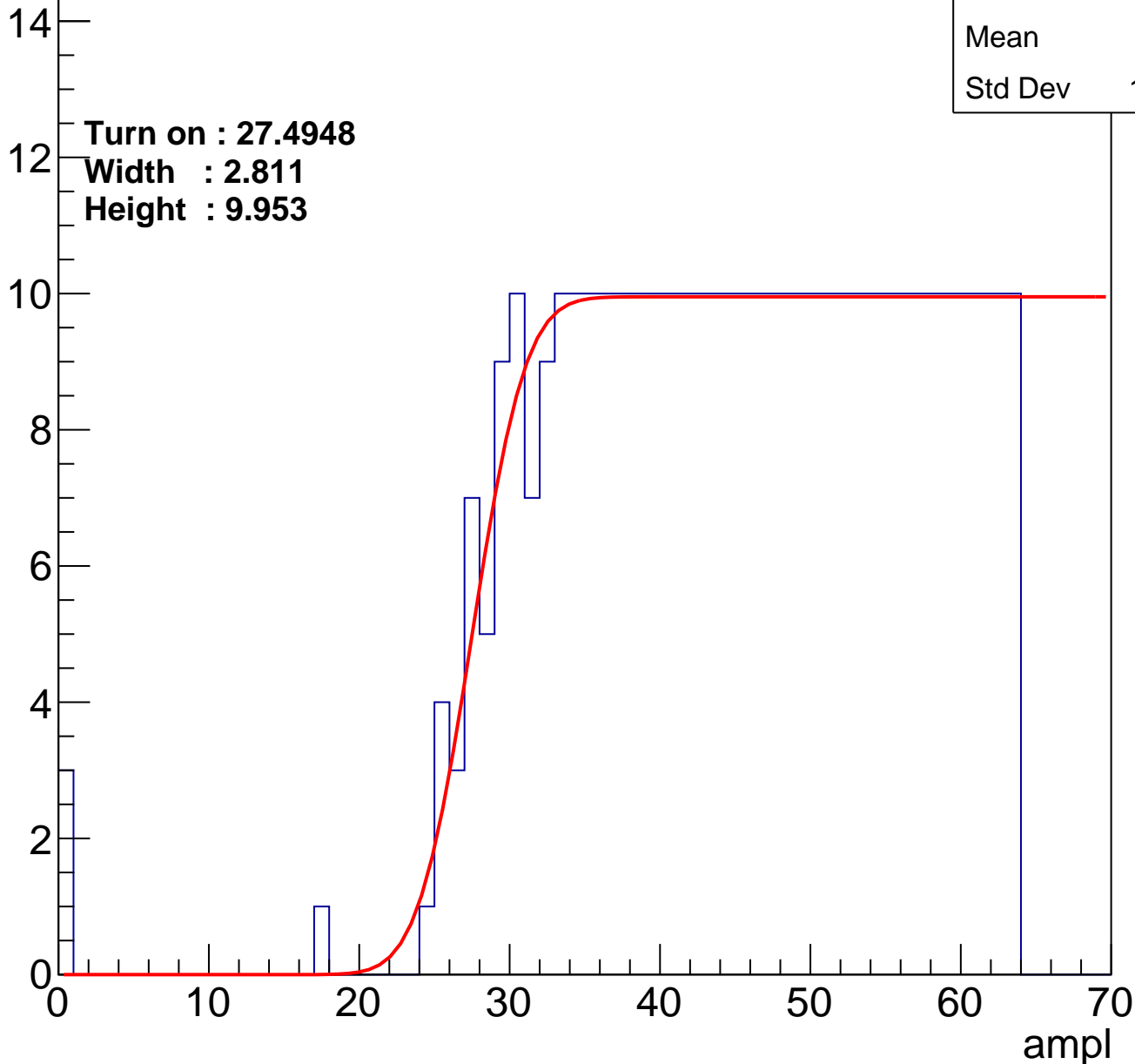
Entry

Entries	369
Mean	44.7
Std Dev	11.49

Turn on : 27.4948

Width : 2.811

Height : 9.953



B1L003S, U4-ch76

calib_packv5_042523_0143.root, FC#13, port D2

Entries	371
Mean	44.64
Std Dev	11.48

Turn on : 27.2958

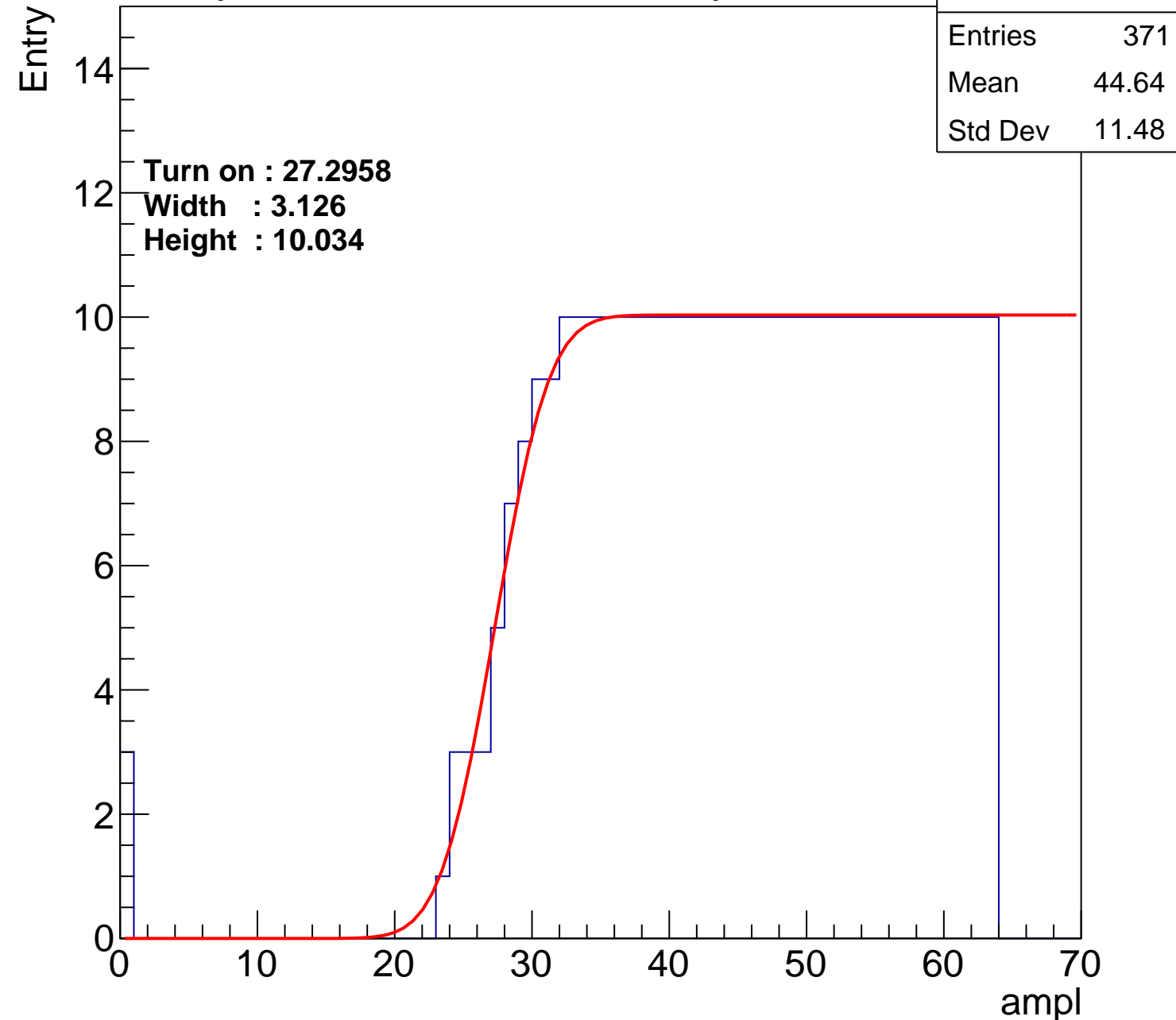
Width : 3.126

Height : 10.034

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U4-ch77

calib_packv5_042523_0143.root, FC#13, port D2

Entries	352
Mean	45.47
Std Dev	11.18

Turn on : 29.5682

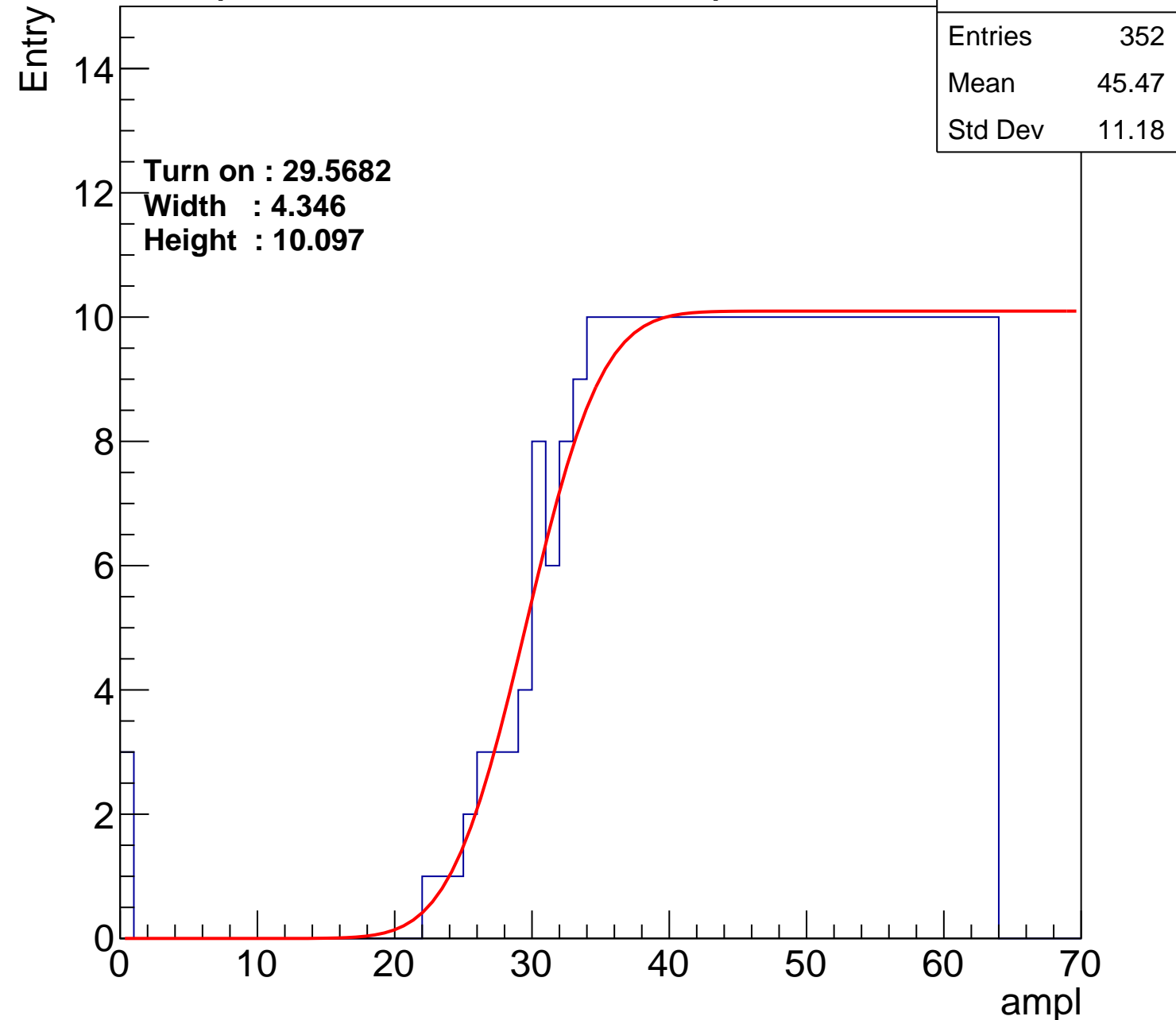
Width : 4.346

Height : 10.097

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U4-ch78

calib_packv5_042523_0143.root, FC#13, port D2

Entries	367
Mean	44.73
Std Dev	11.63

Turn on : 28.0437

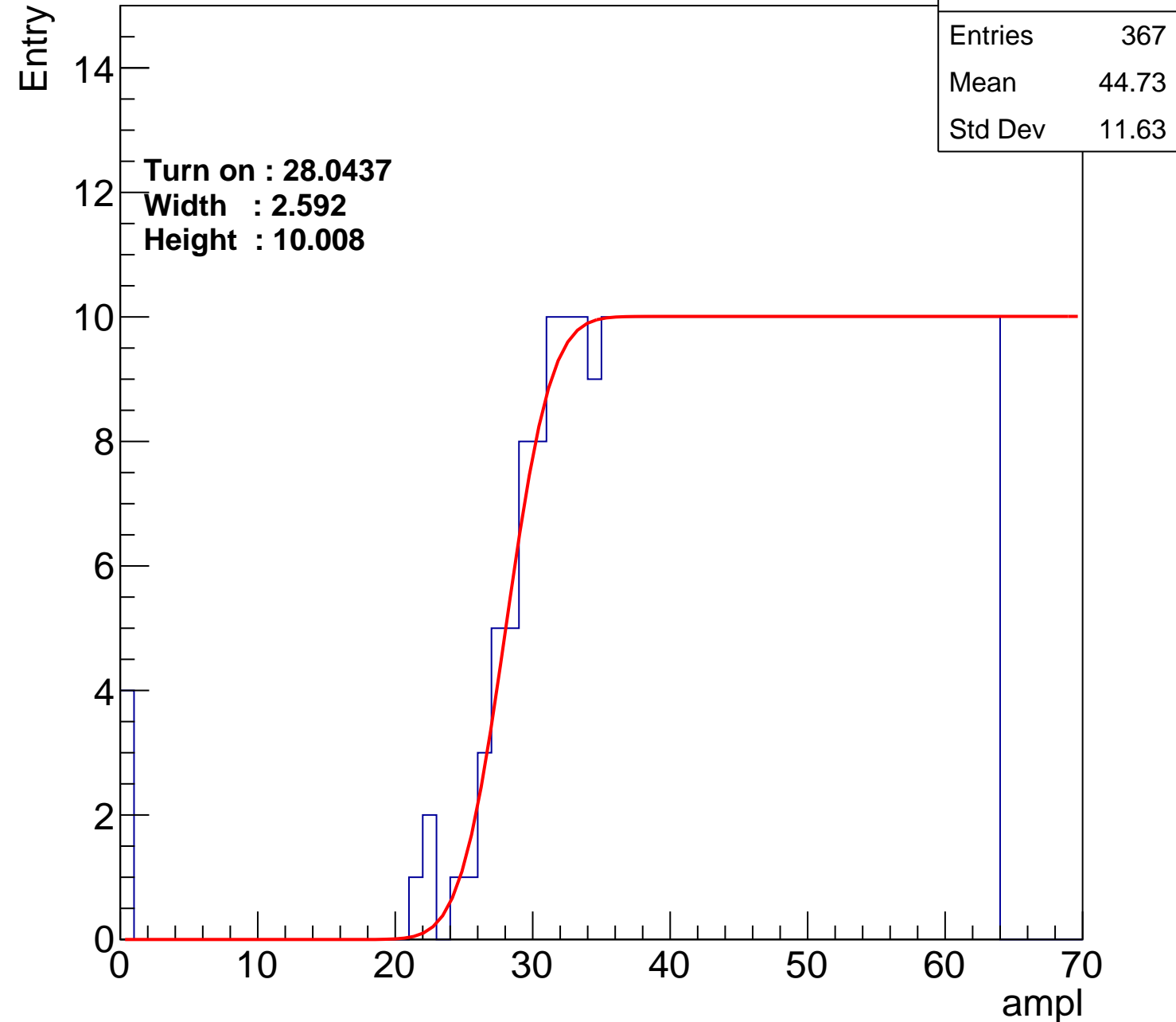
Width : 2.592

Height : 10.008

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U4-ch79

calib_packv5_042523_0143.root, FC#13, port D2

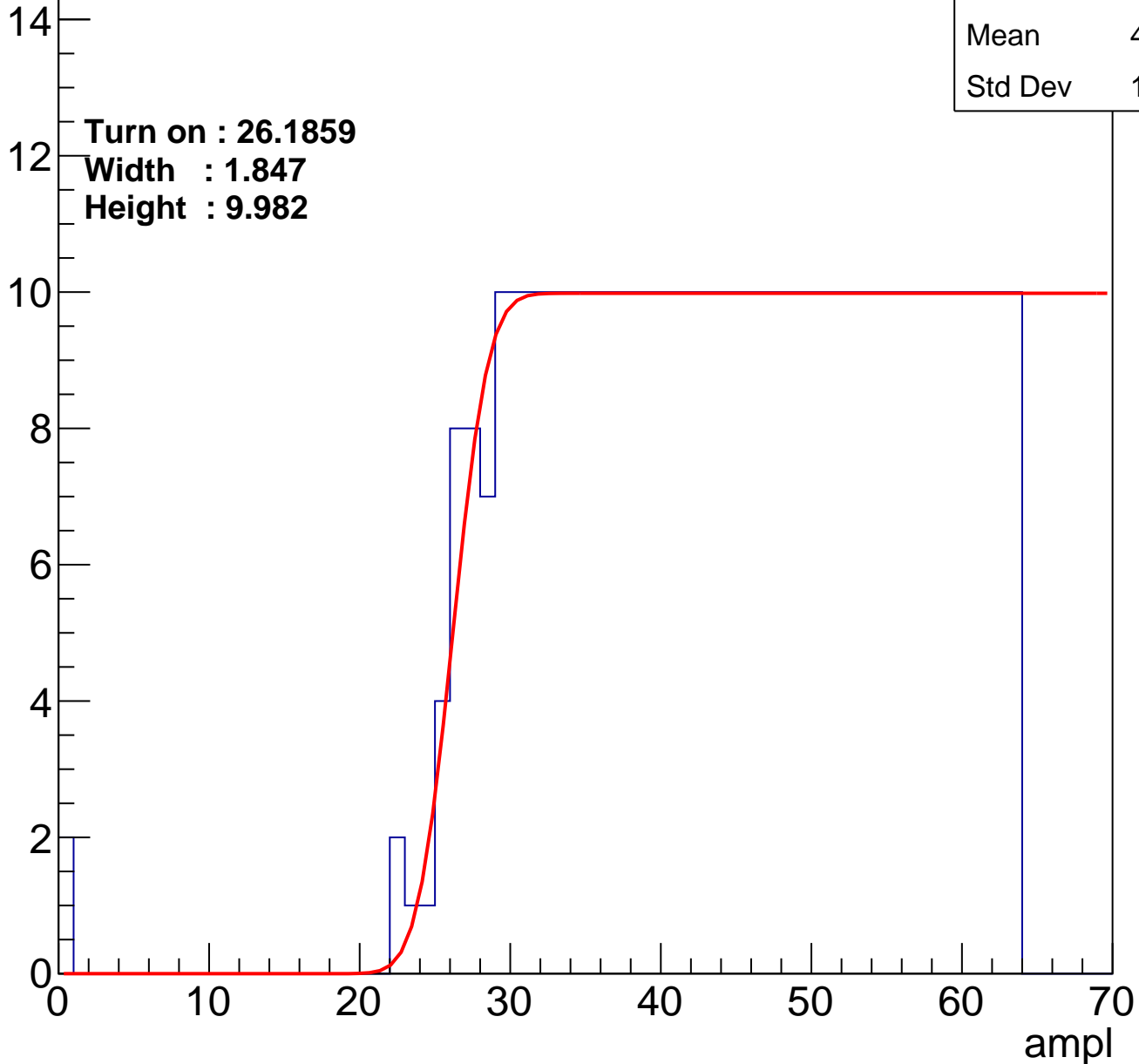
Entries	383
Mean	44.15
Std Dev	11.53

Turn on : 26.1859

Width : 1.847

Height : 9.982

Entry



B1L003S, U4-ch80

calib_packv5_042523_0143.root, FC#13, port D2

Entries	379
Mean	44.42
Std Dev	11.23

Turn on : 26.2679

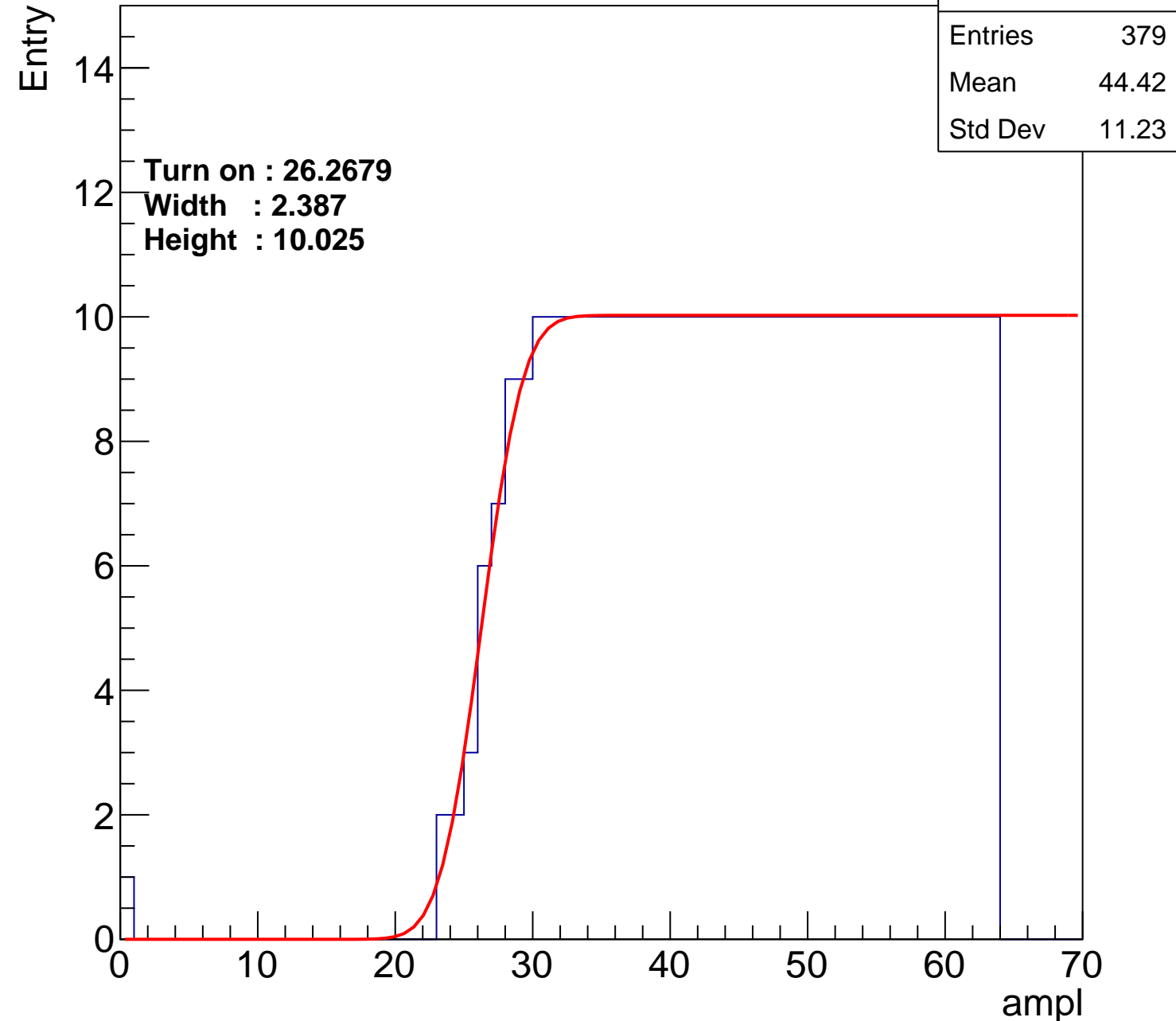
Width : 2.387

Height : 10.025

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U4-ch81

calib_packv5_042523_0143.root, FC#13, port D2

Entries	372
Mean	44.54
Std Dev	11.66

Turn on : 27.4577

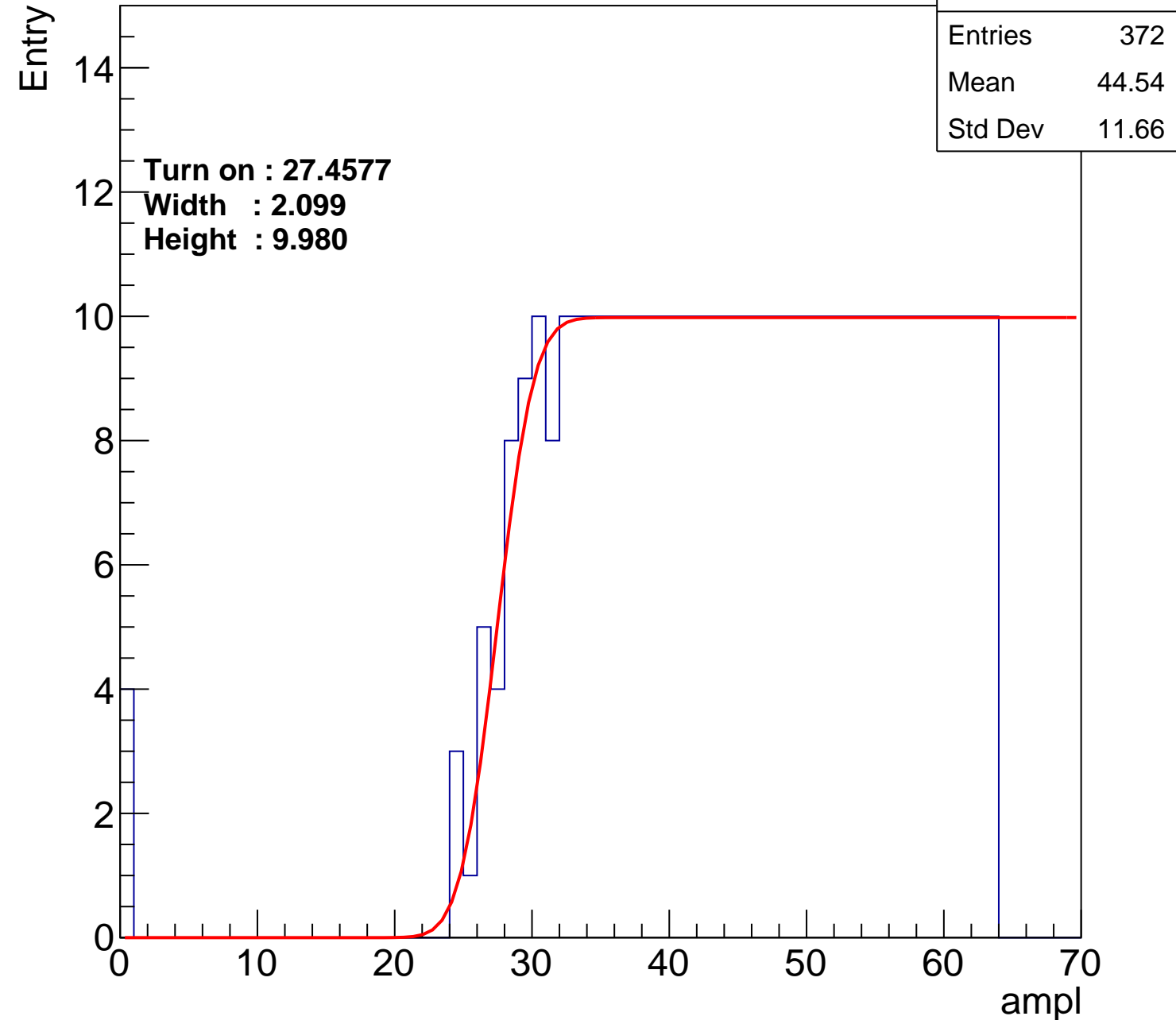
Width : 2.099

Height : 9.980

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U4-ch82

calib_packv5_042523_0143.root, FC#13, port D2

Entries	370
Mean	44.26
Std Dev	12.47

Turn on : 28.3831

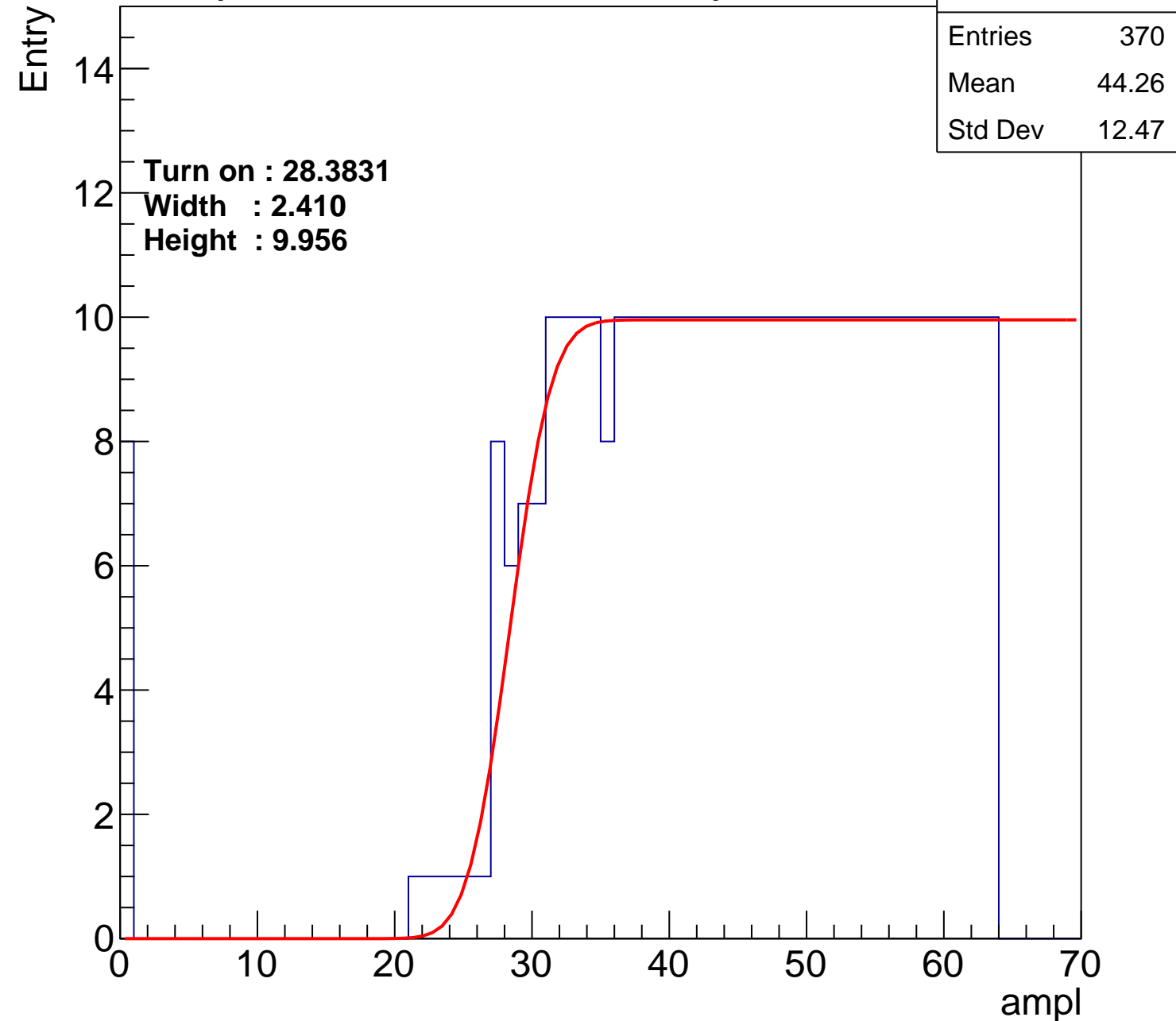
Width : 2.410

Height : 9.956

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U4-ch83

calib_packv5_042523_0143.root, FC#13, port D2

Entries	367
Mean	44.75
Std Dev	11.59

Turn on : 27.8783

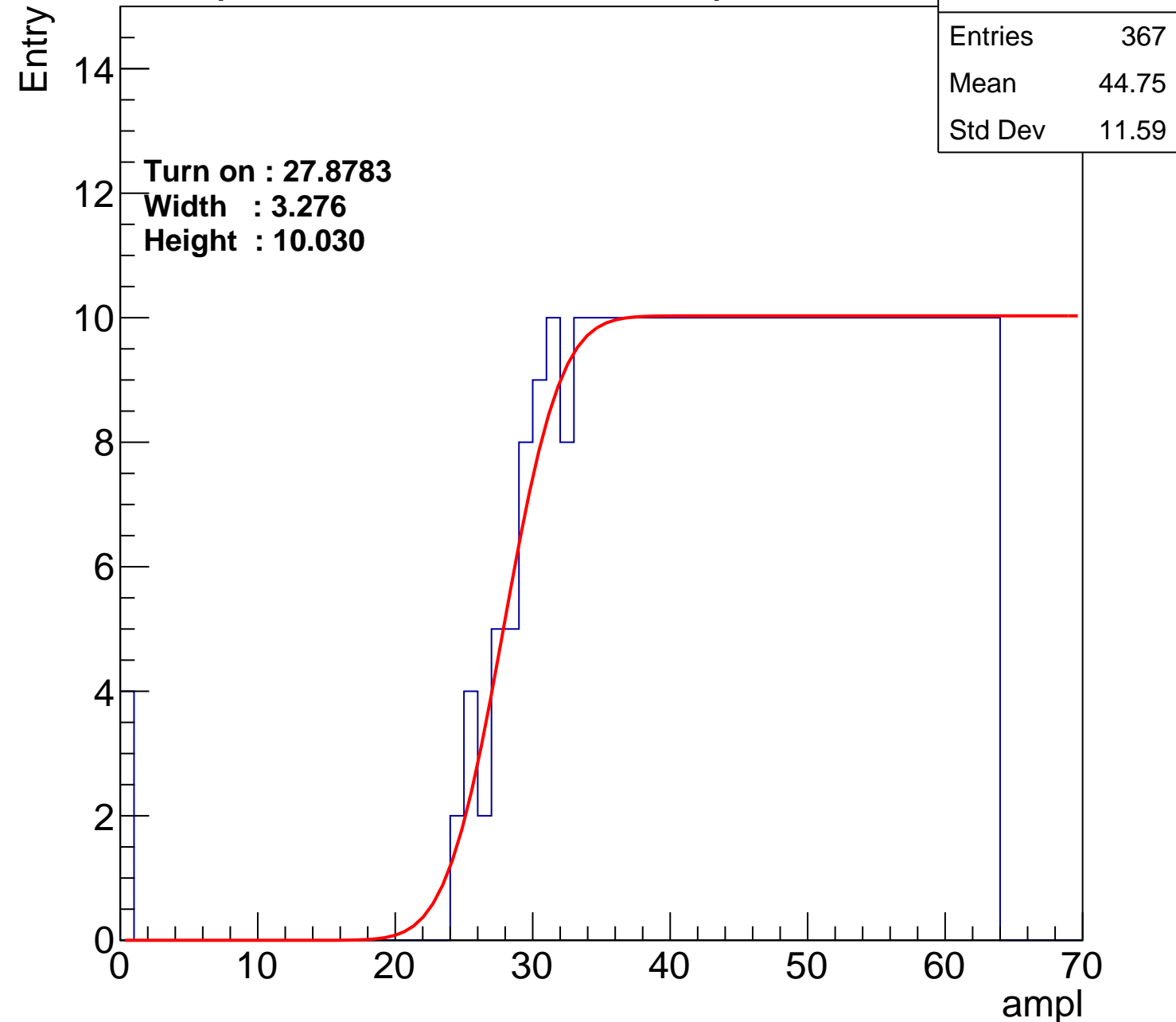
Width : 3.276

Height : 10.030

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U4-ch84

calib_packv5_042523_0143.root, FC#13, port D2

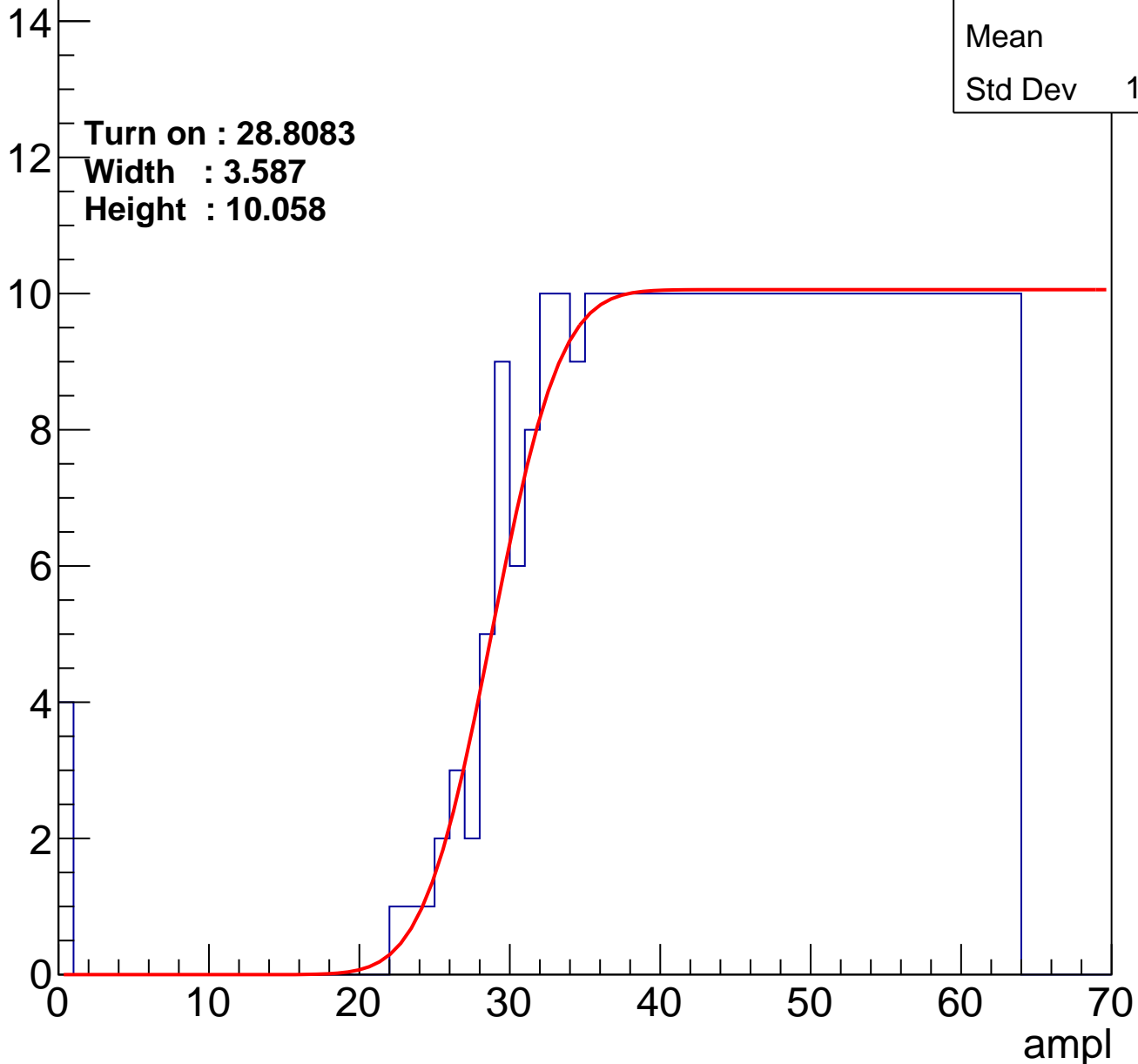
Entries	361
Mean	45
Std Dev	11.52

Turn on : 28.8083

Width : 3.587

Height : 10.058

Entry



B1L003S, U4-ch85

calib_packv5_042523_0143.root, FC#13, port D2

Entries	380
Mean	44.17
Std Dev	11.73

Turn on : 26.7815

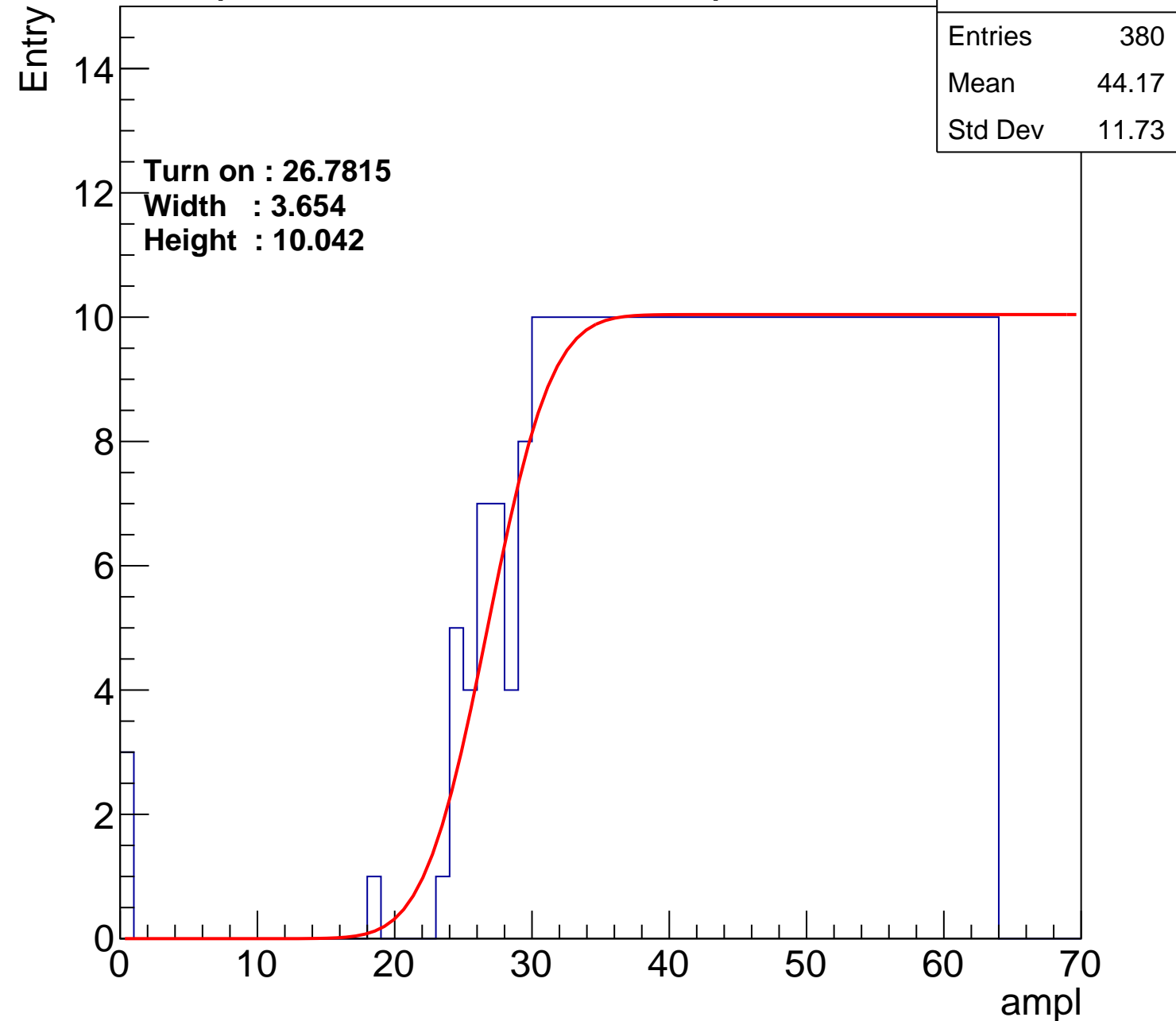
Width : 3.654

Height : 10.042

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U4-ch86

calib_packv5_042523_0143.root, FC#13, port D2

Entries	367
Mean	44.85
Std Dev	11.26

Turn on : 27.6778

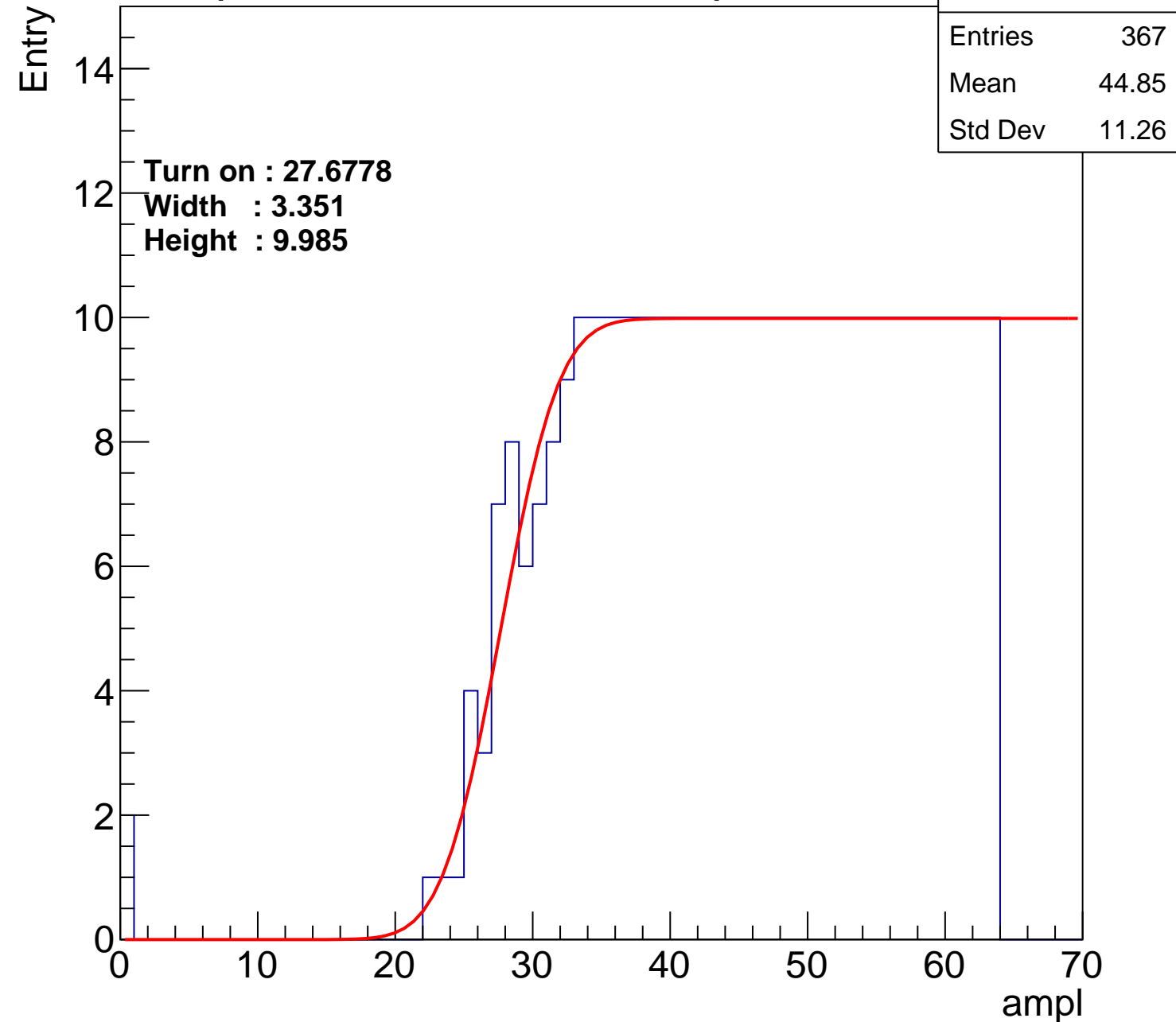
Width : 3.351

Height : 9.985

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U4-ch87

calib_packv5_042523_0143.root, FC#13, port D2

Entries	372
Mean	44.52
Std Dev	11.68

Turn on : 26.7326

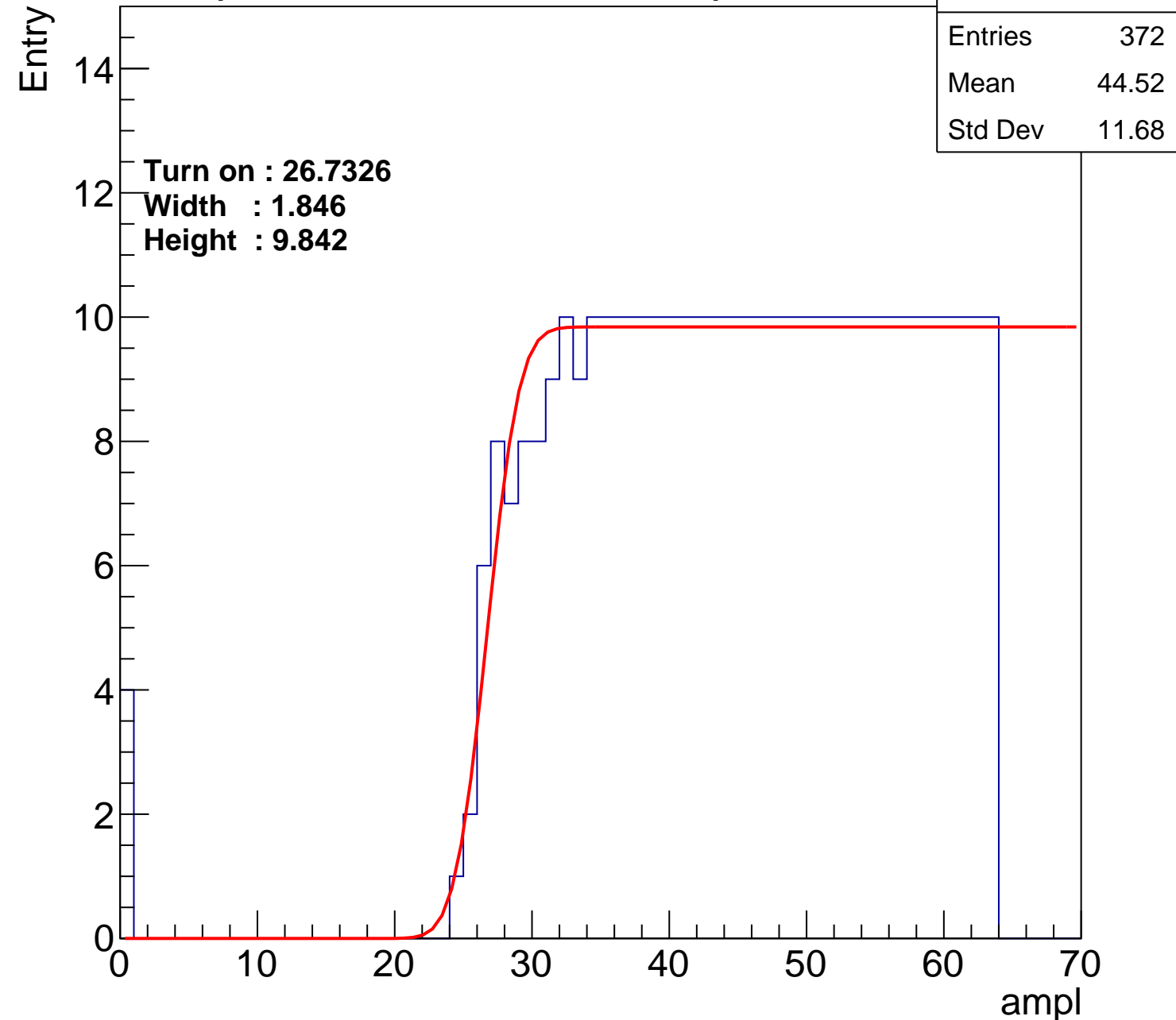
Width : 1.846

Height : 9.842

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U4-ch88

calib_packv5_042523_0143.root, FC#13, port D2

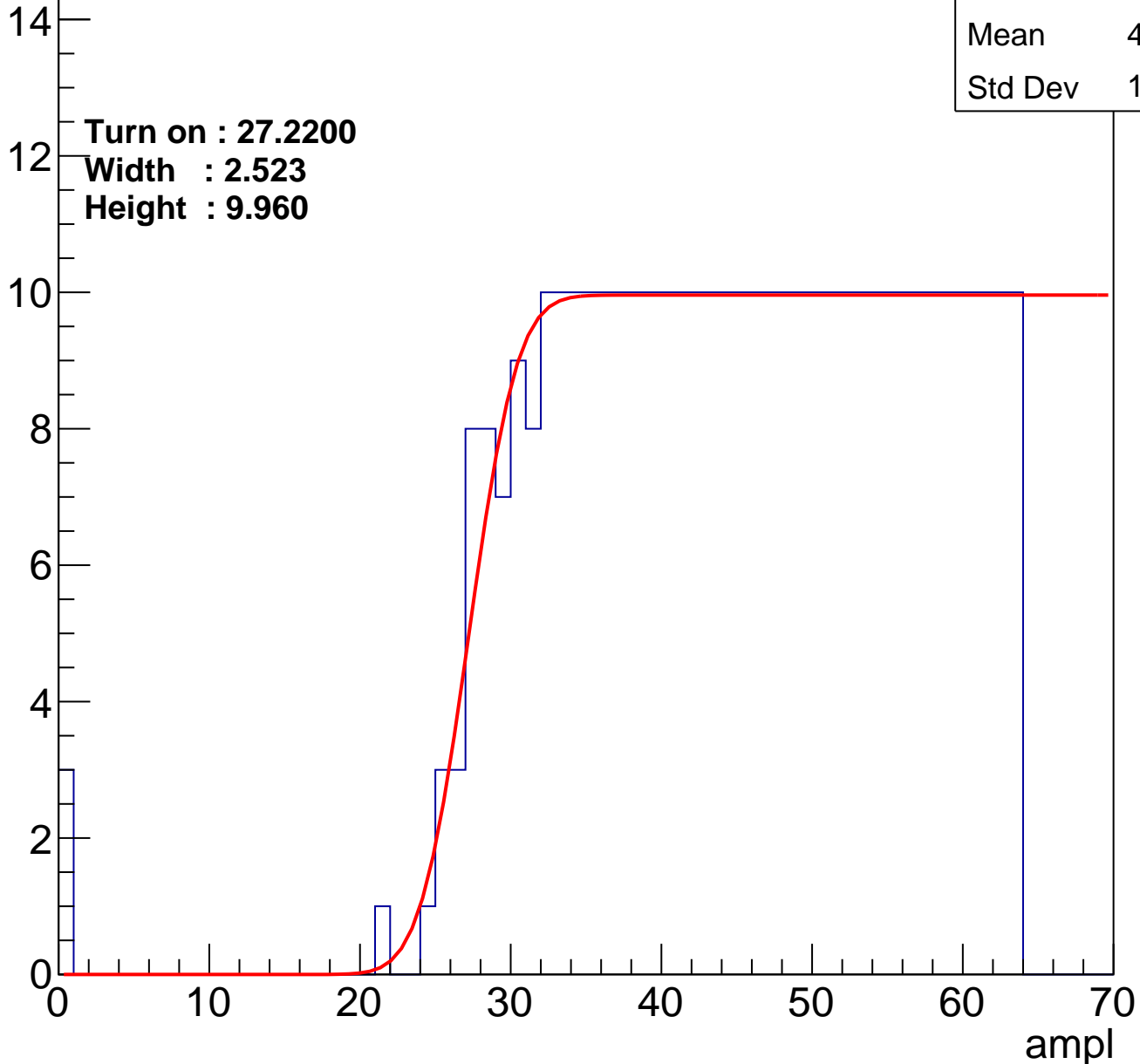
Entries	371
Mean	44.63
Std Dev	11.48

Turn on : 27.2200

Width : 2.523

Height : 9.960

Entry



B1L003S, U4-ch89

calib_packv5_042523_0143.root, FC#13, port D2

Entries	389
Mean	43.8
Std Dev	11.76

Turn on : 25.3088

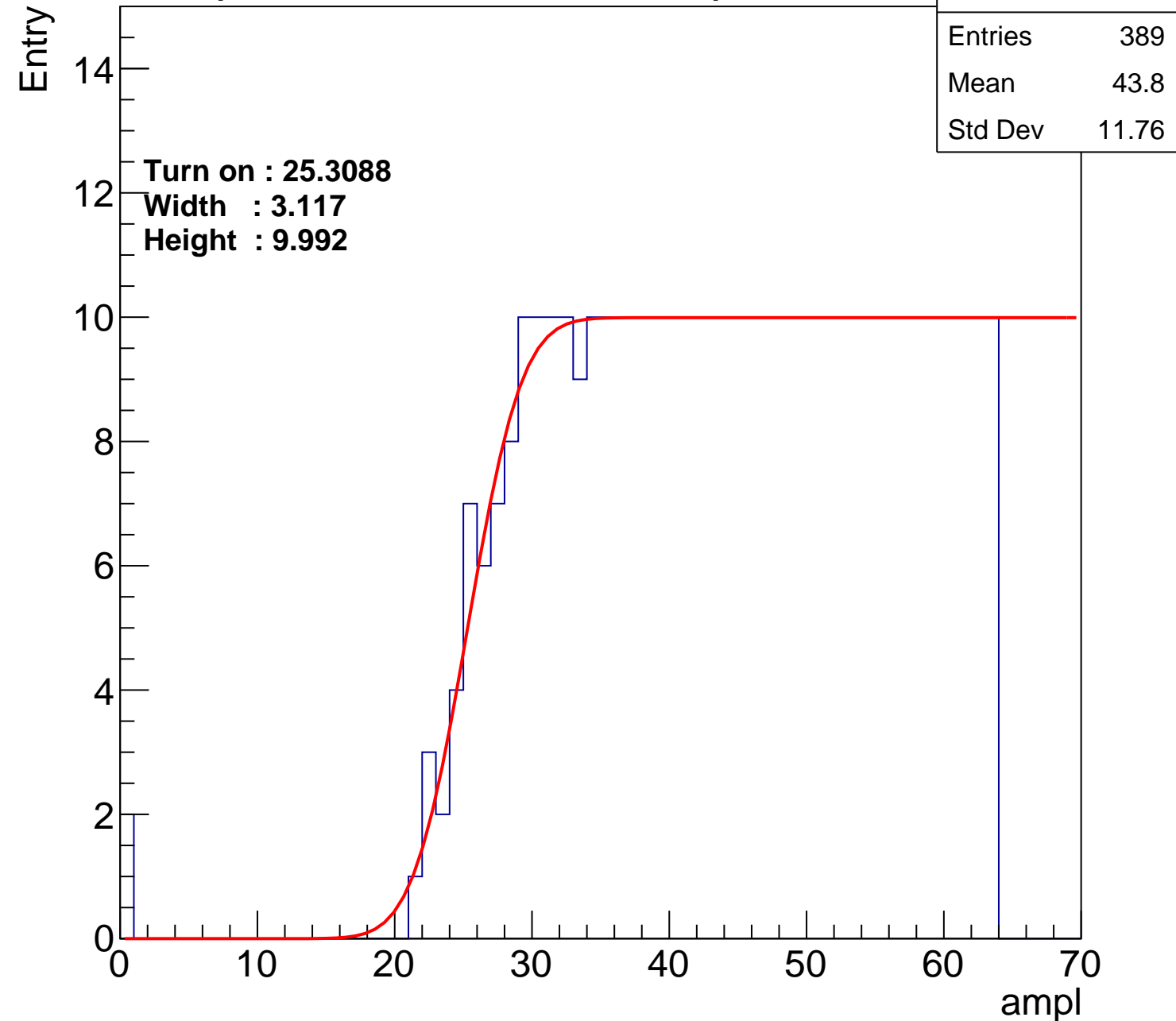
Width : 3.117

Height : 9.992

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U4-ch90

calib_packv5_042523_0143.root, FC#13, port D2

Entries	375
Mean	44.46
Std Dev	11.46

Turn on : 26.7232

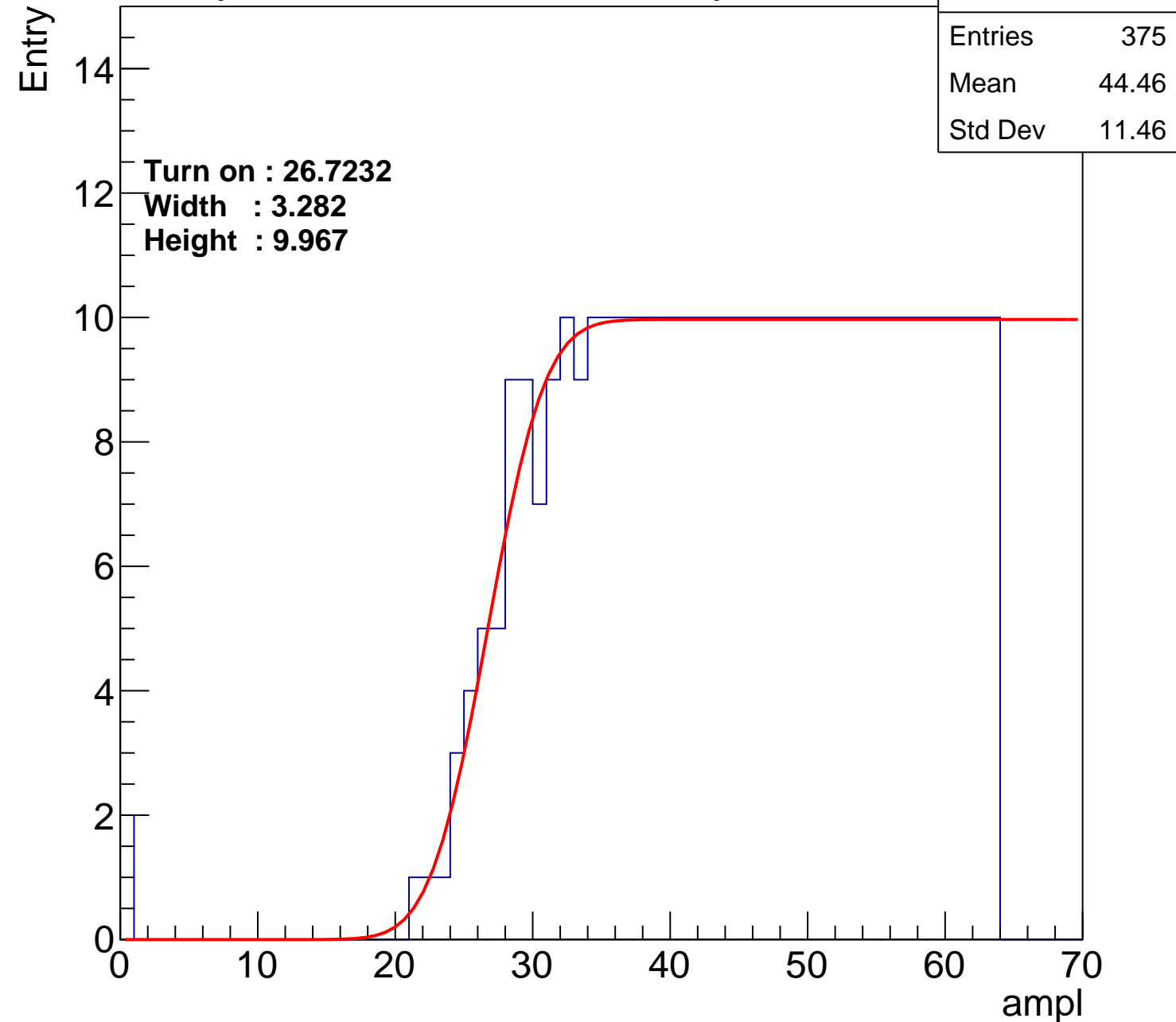
Width : 3.282

Height : 9.967

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U4-ch91

calib_packv5_042523_0143.root, FC#13, port D2

Entries	383
Mean	44.12
Std Dev	11.57

Turn on : 25.8591

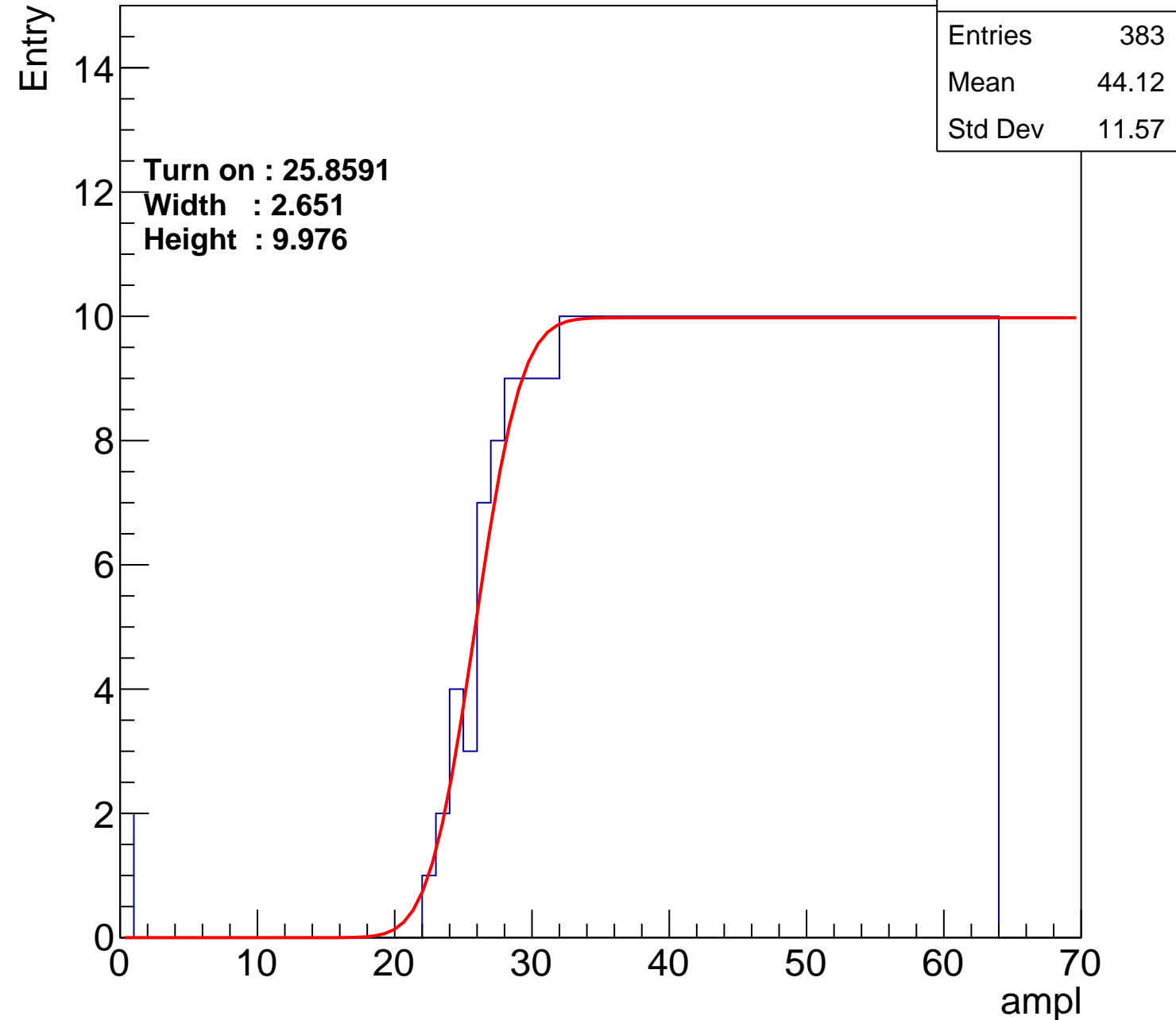
Width : 2.651

Height : 9.976

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U4-ch92

calib_packv5_042523_0143.root, FC#13, port D2

Entries	383
Mean	43.83
Std Dev	12.3

Turn on : 25.9155

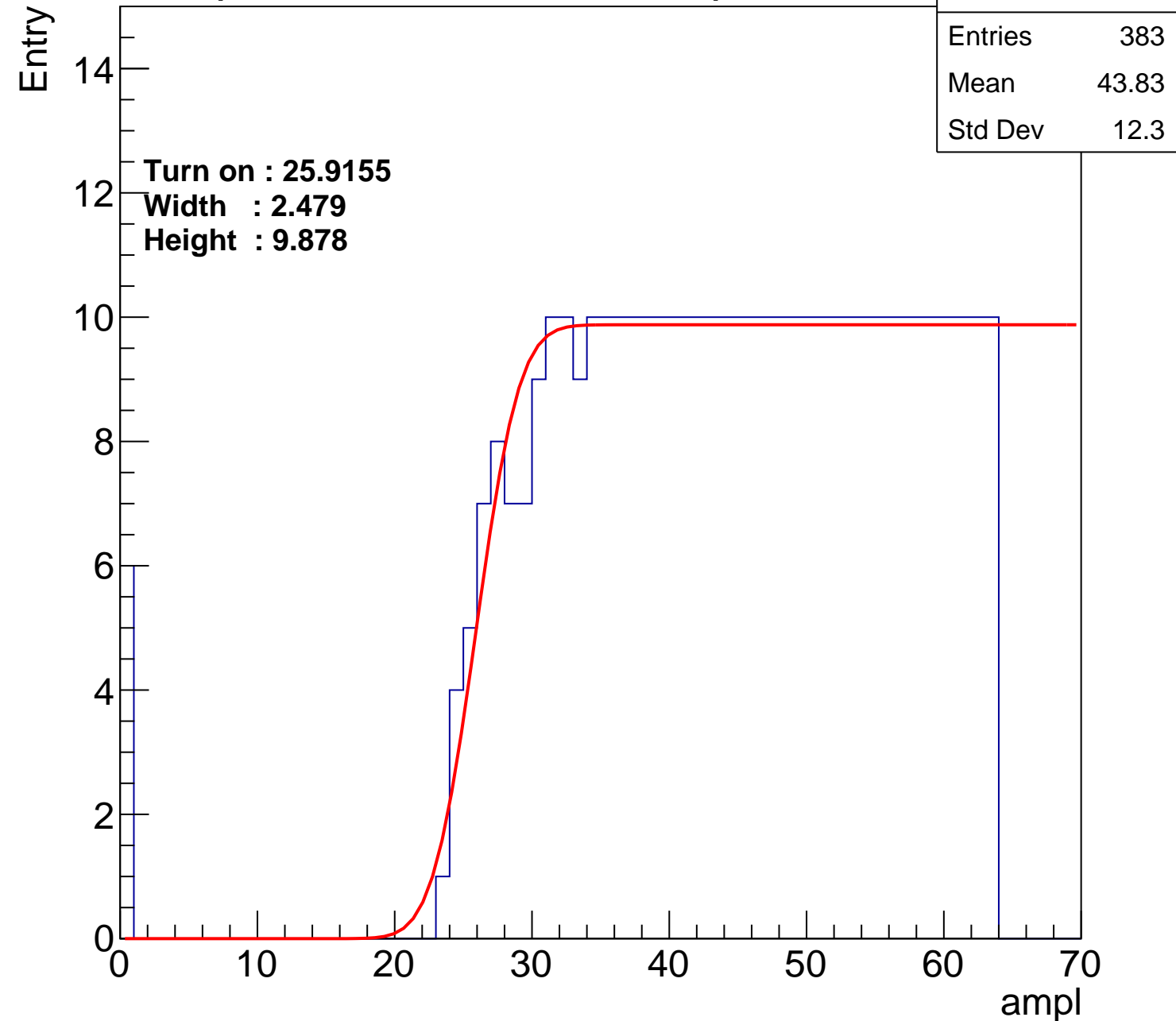
Width : 2.479

Height : 9.878

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U4-ch93

calib_packv5_042523_0143.root, FC#13, port D2

Entries	382
Mean	44.12
Std Dev	11.63

Turn on : 25.8496

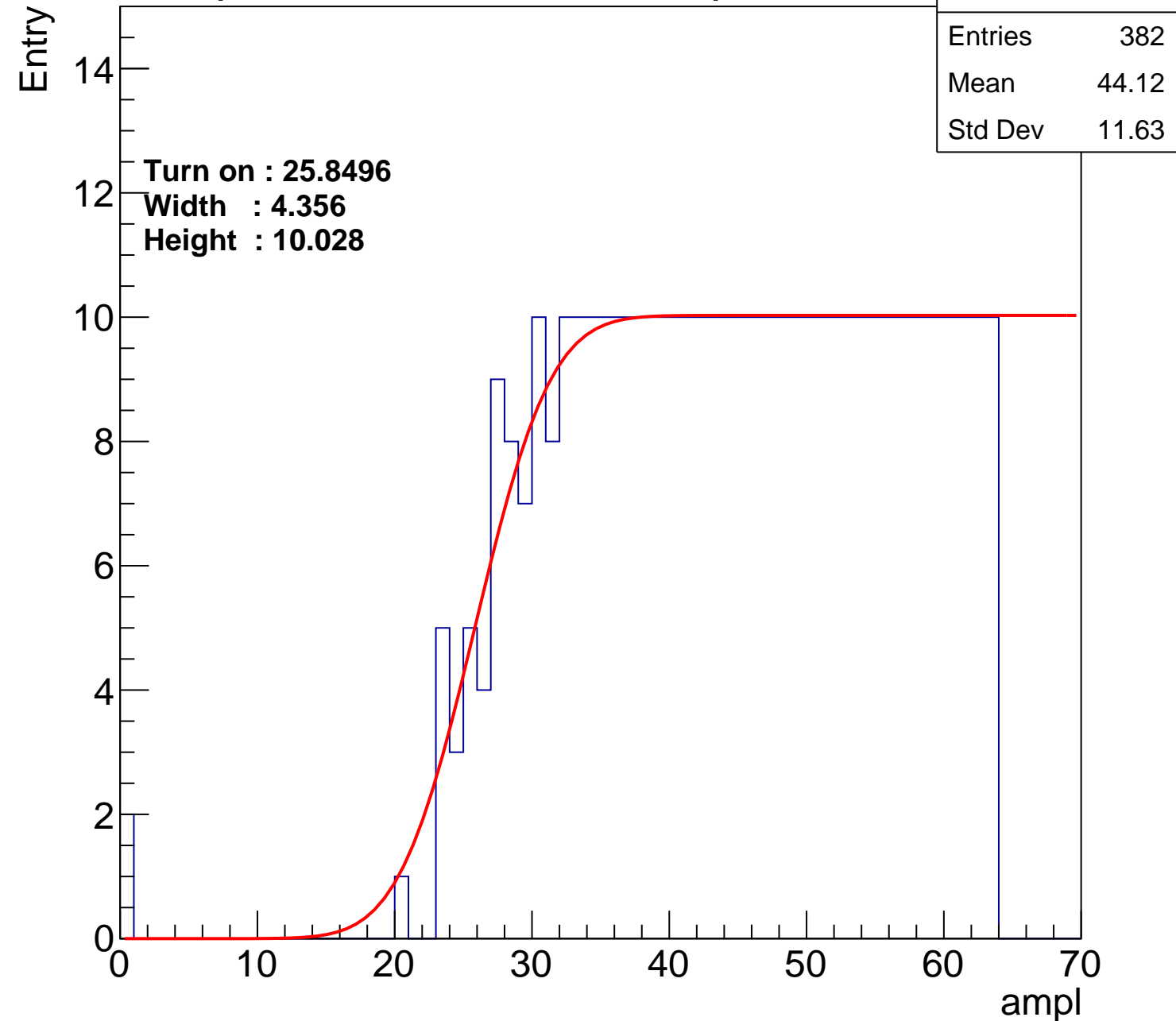
Width : 4.356

Height : 10.028

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U4-ch94

calib_packv5_042523_0143.root, FC#13, port D2

Entries	370
Mean	44.65
Std Dev	11.51

Turn on : 28.0127

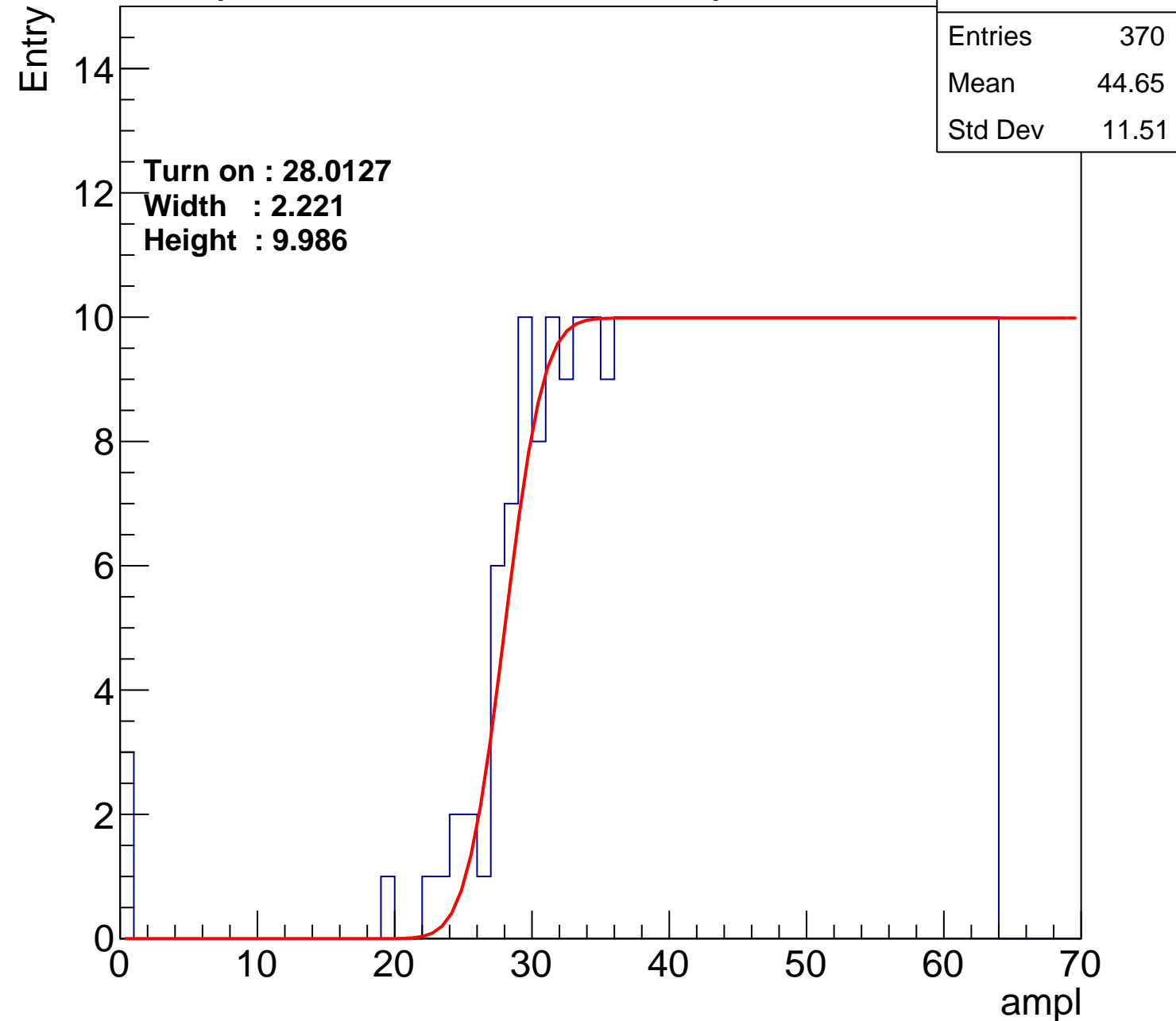
Width : 2.221

Height : 9.986

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U4-ch95

calib_packv5_042523_0143.root, FC#13, port D2

Entries	349
Mean	45.79
Std Dev	10.73

Turn on : 29.2041

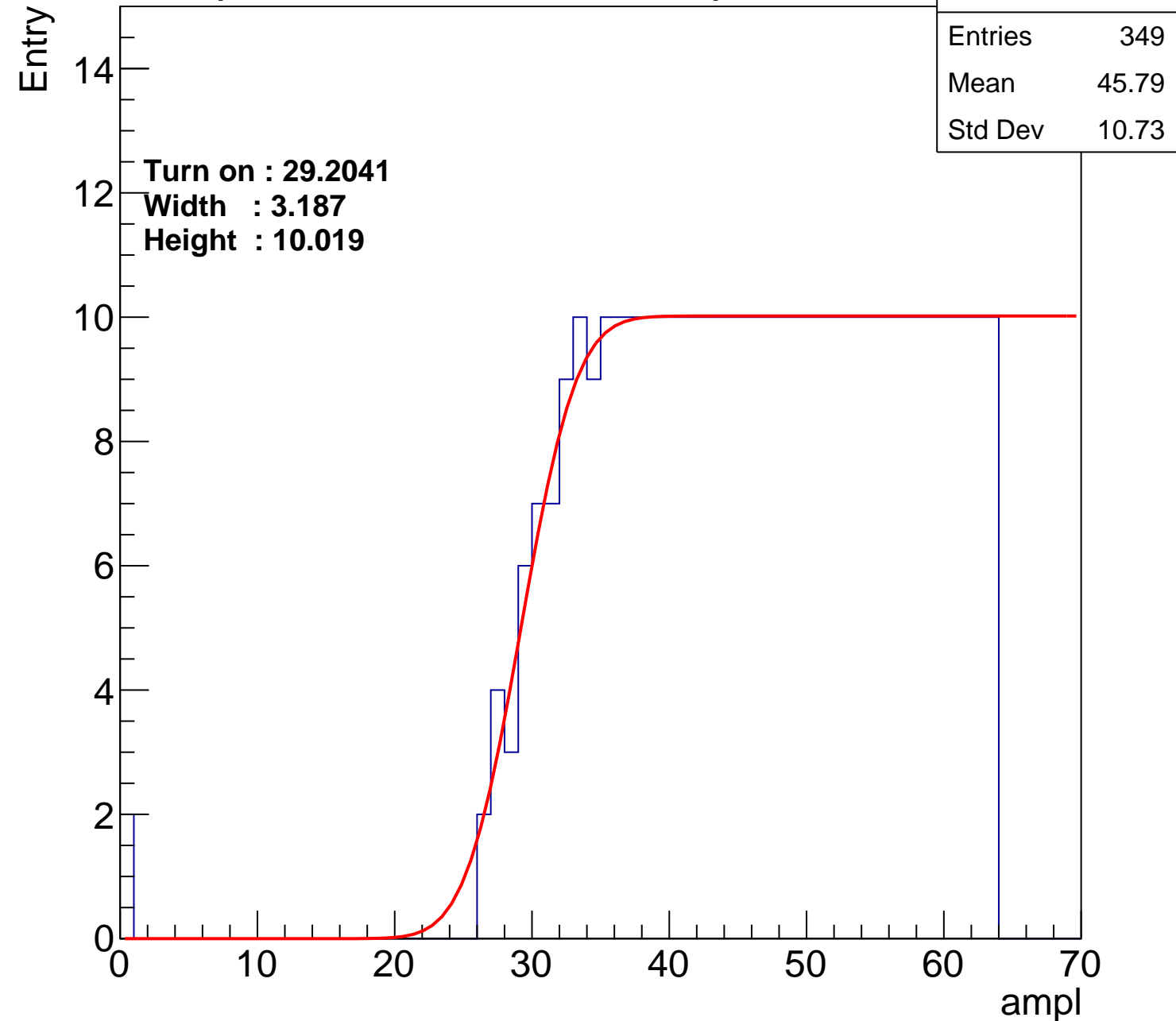
Width : 3.187

Height : 10.019

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U4-ch96

calib_packv5_042523_0143.root, FC#13, port D2

Entries	373
Mean	44.44
Std Dev	11.76

Turn on : 27.6876

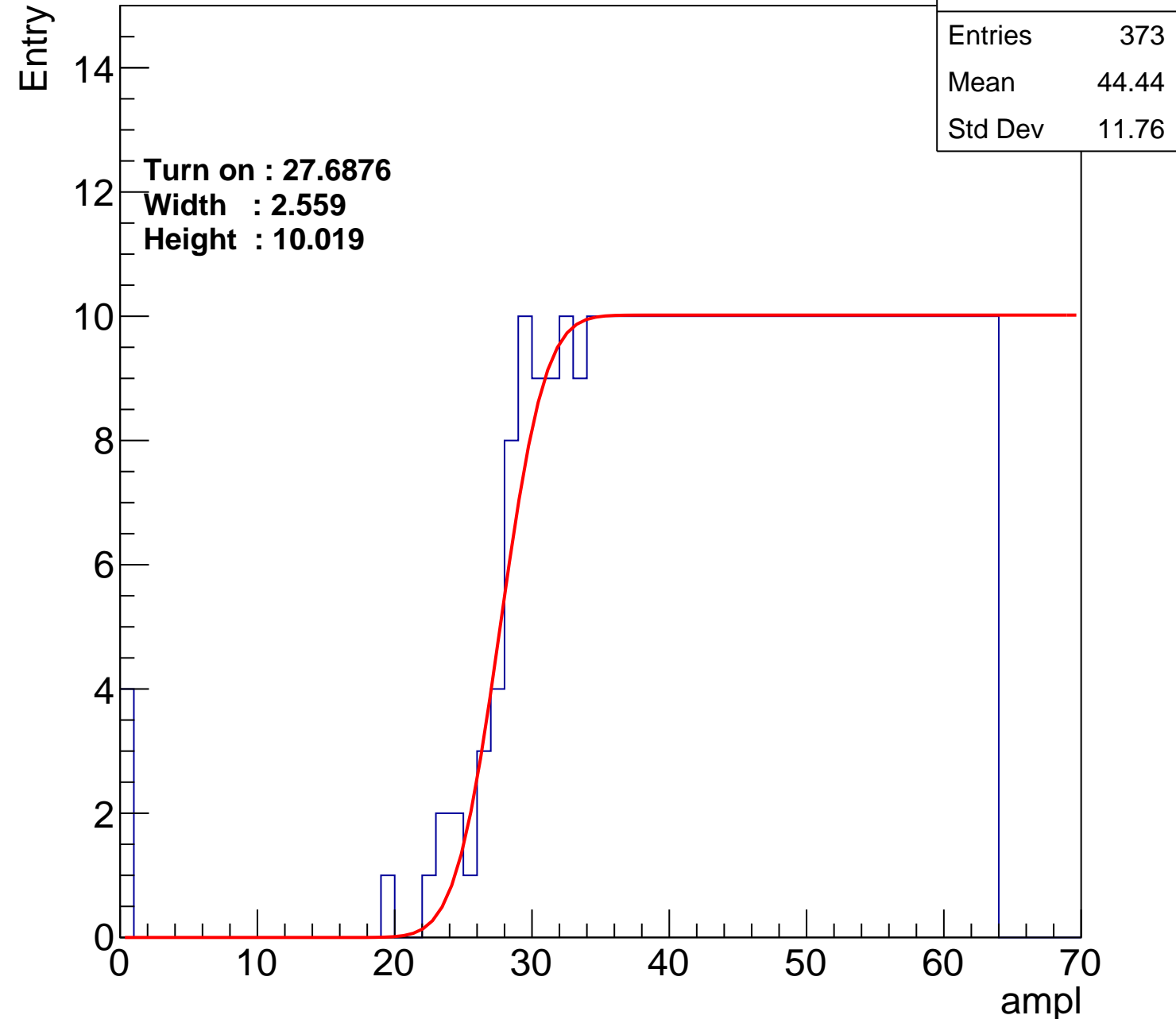
Width : 2.559

Height : 10.019

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U4-ch97

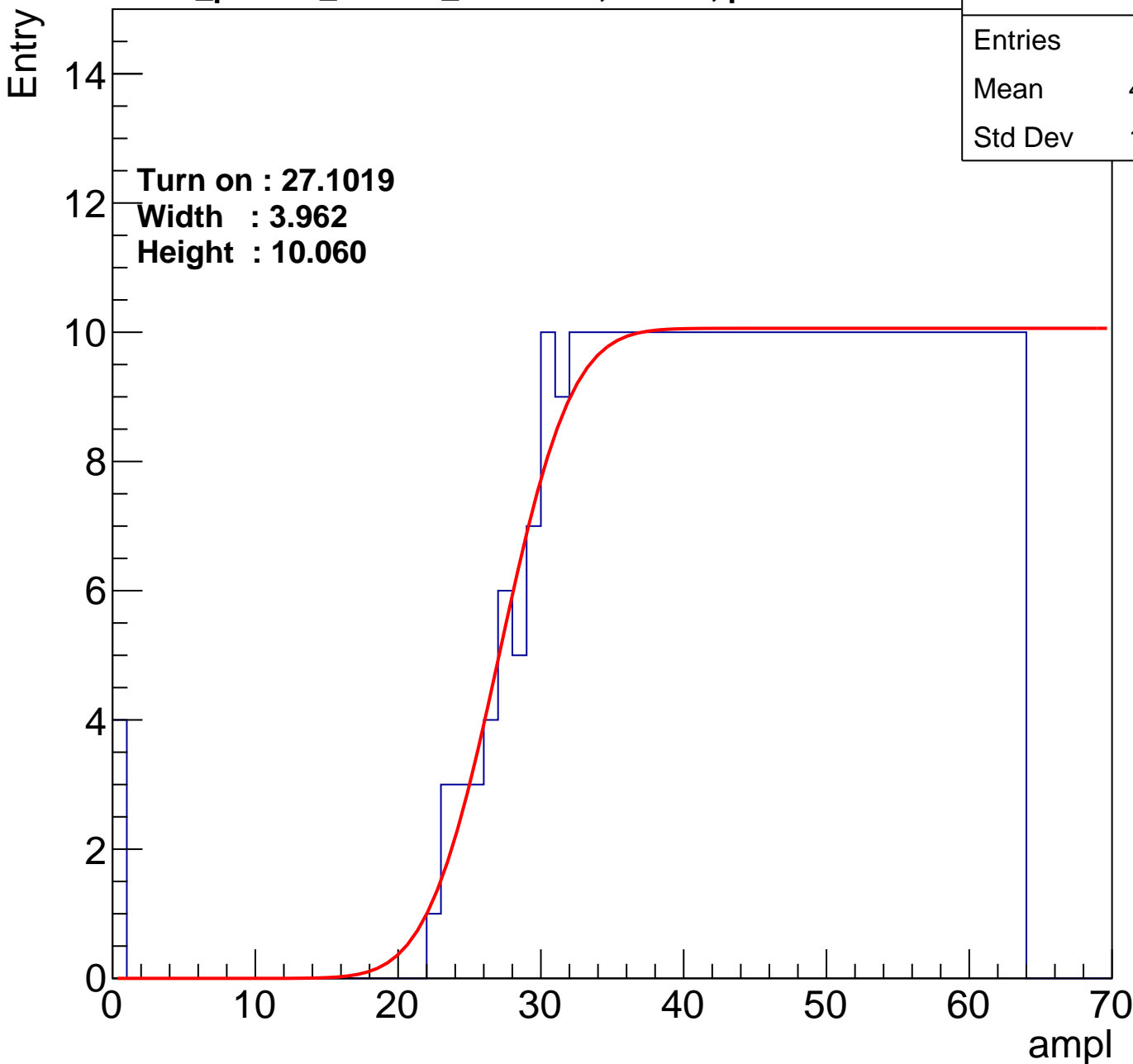
calib_packv5_042523_0143.root, FC#13, port D2

Turn on : 27.1019

Width : 3.962

Height : 10.060

Entries	375
Mean	44.34
Std Dev	11.82



B1L003S, U4-ch98

calib_packv5_042523_0143.root, FC#13, port D2

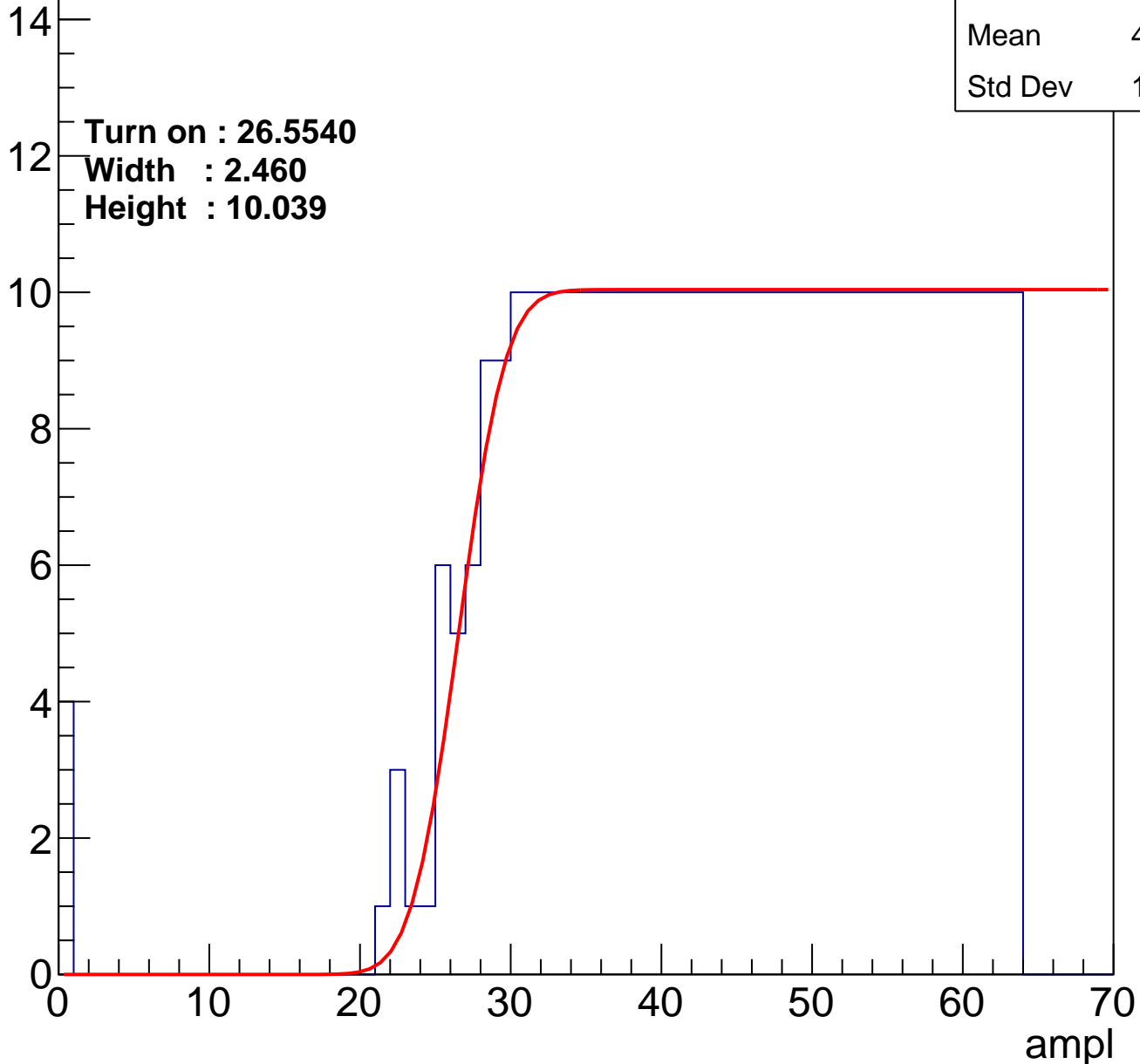
Entries	385
Mean	43.89
Std Dev	11.98

Turn on : 26.5540

Width : 2.460

Height : 10.039

Entry



B1L003S, U4-ch99

calib_packv5_042523_0143.root, FC#13, port D2

Entries	369
Mean	44.83
Std Dev	11.1

Turn on : 27.3325

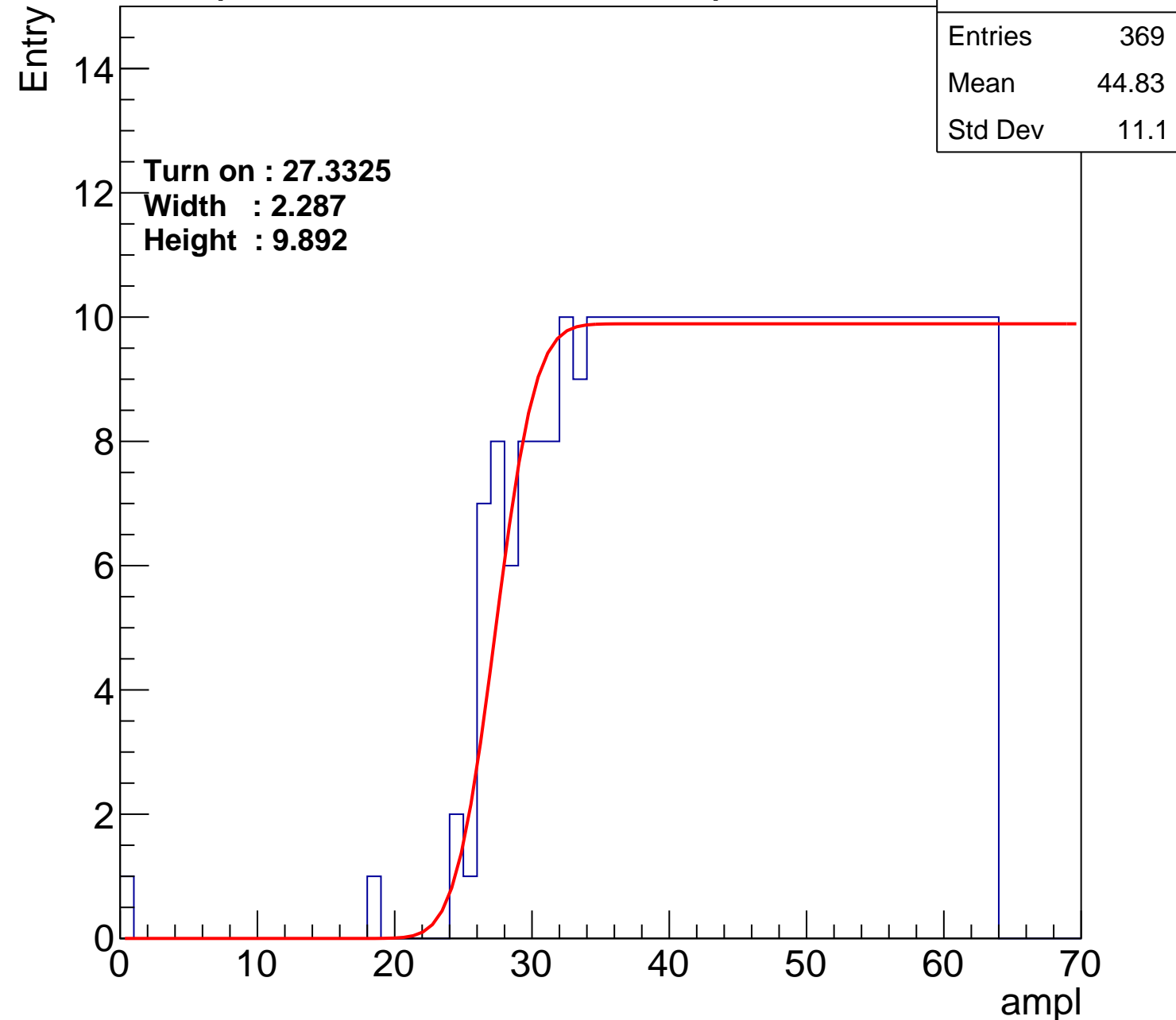
Width : 2.287

Height : 9.892

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U4-ch100

calib_packv5_042523_0143.root, FC#13, port D2

Entries	379
Mean	44.13
Std Dev	11.93

Turn on : 26.8861

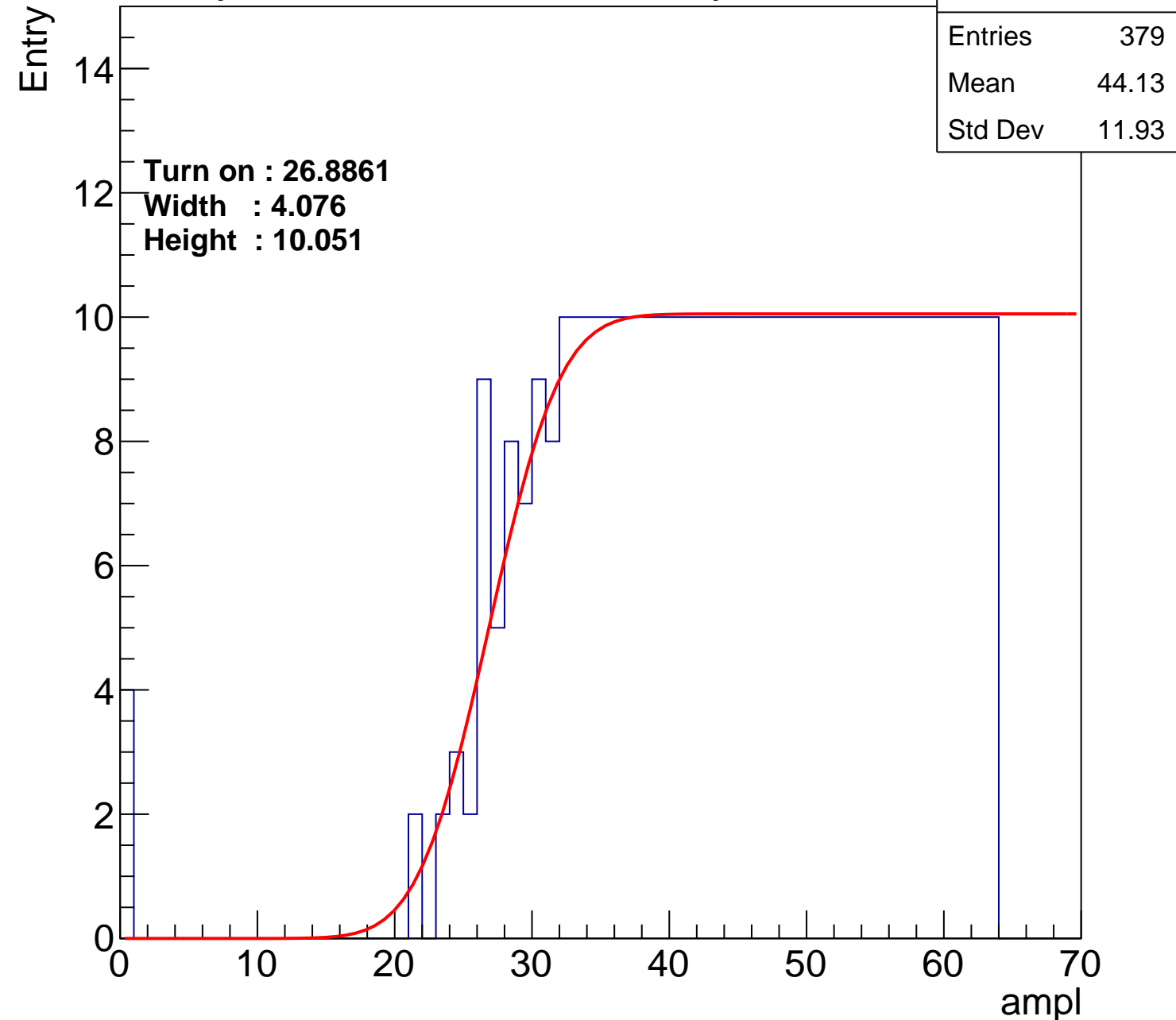
Width : 4.076

Height : 10.051

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U4-ch101

calib_packv5_042523_0143.root, FC#13, port D2

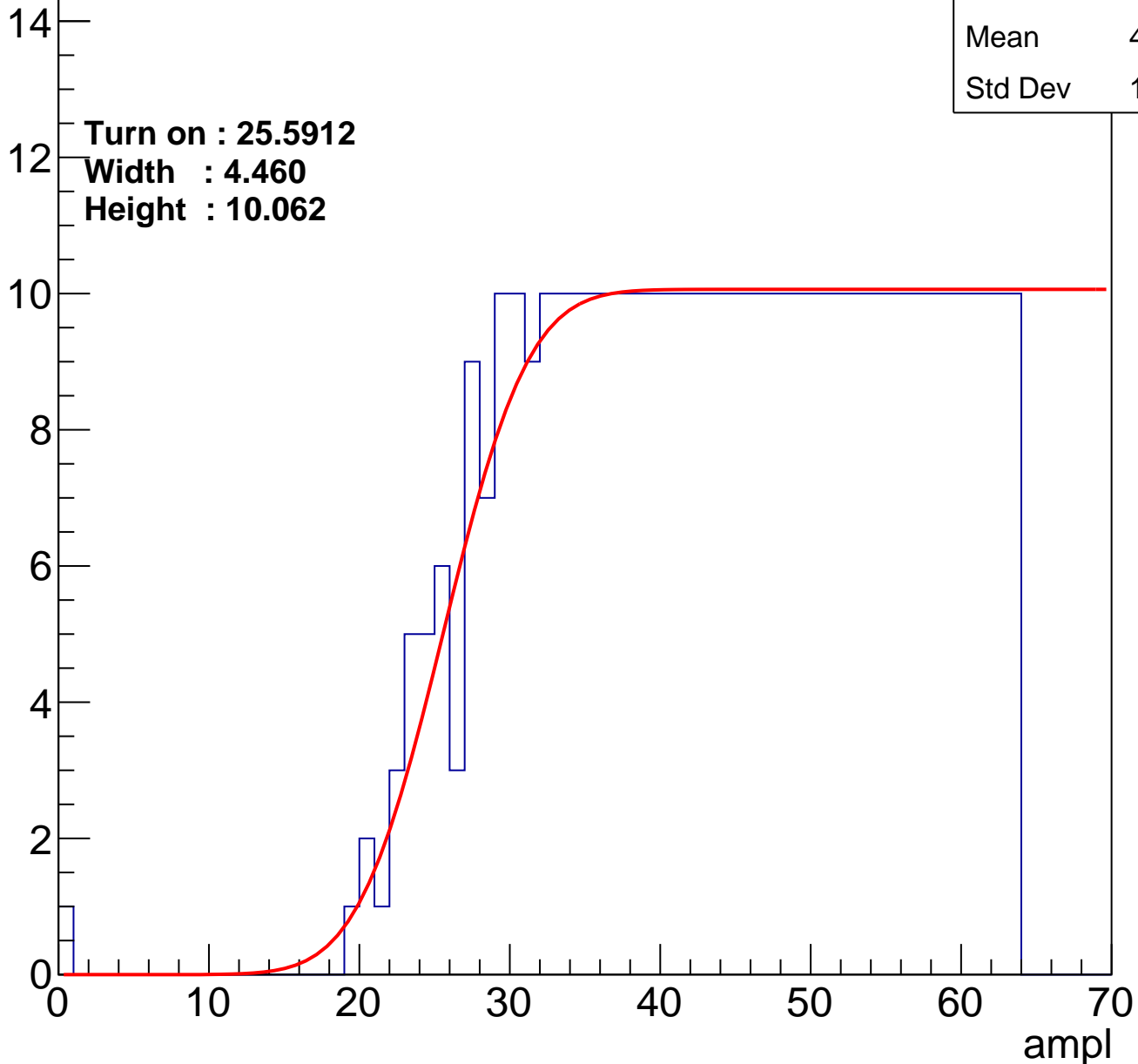
Entries	392
Mean	43.67
Std Dev	11.77

Turn on : 25.5912

Width : 4.460

Height : 10.062

Entry



B1L003S, U4-ch102

calib_packv5_042523_0143.root, FC#13, port D2

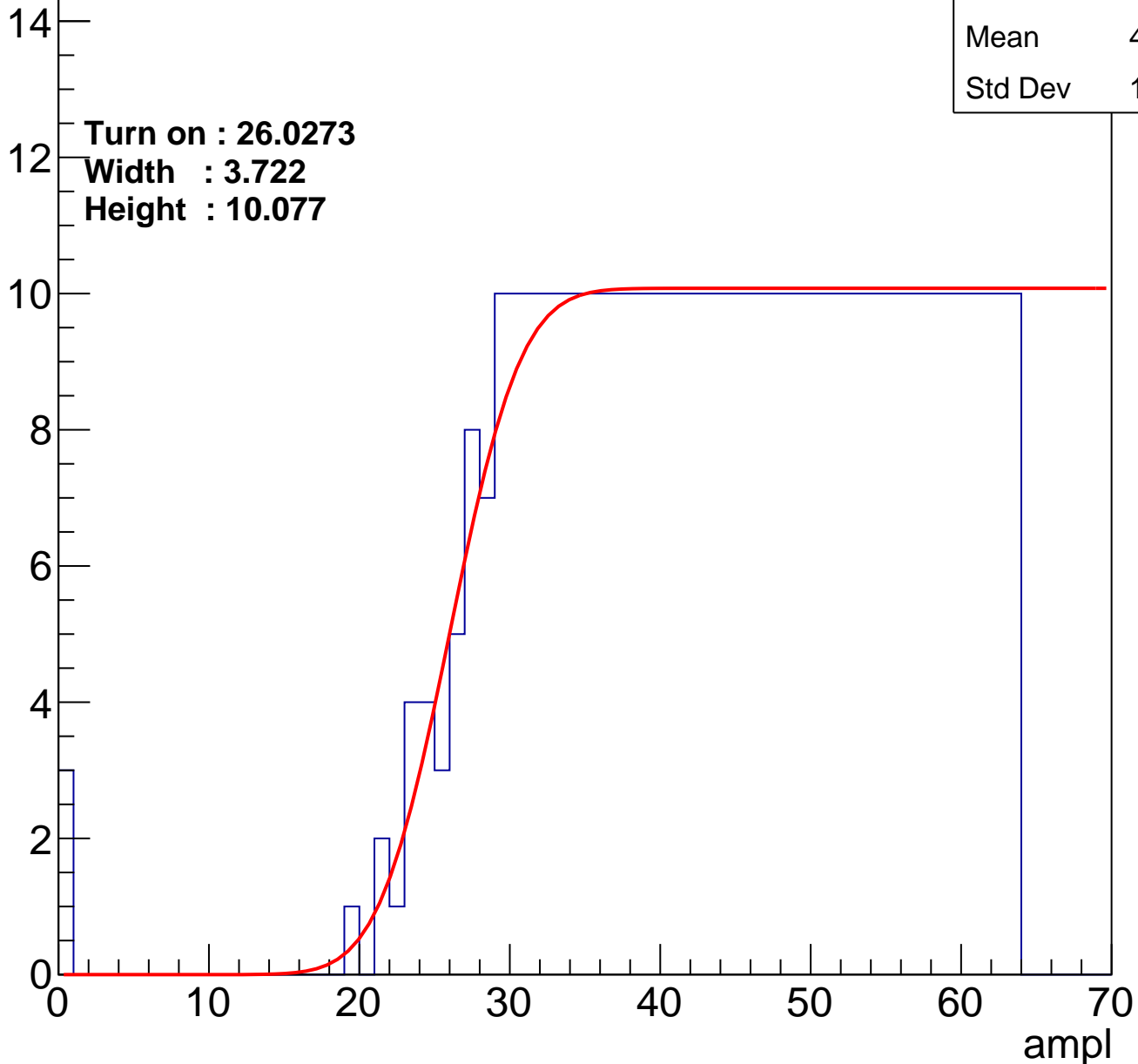
Entries	388
Mean	43.78
Std Dev	11.93

Turn on : 26.0273

Width : 3.722

Height : 10.077

Entry



B1L003S, U4-ch103

calib_packv5_042523_0143.root, FC#13, port D2

Entries	379
Mean	44.34
Std Dev	11.45

Turn on : 26.3853

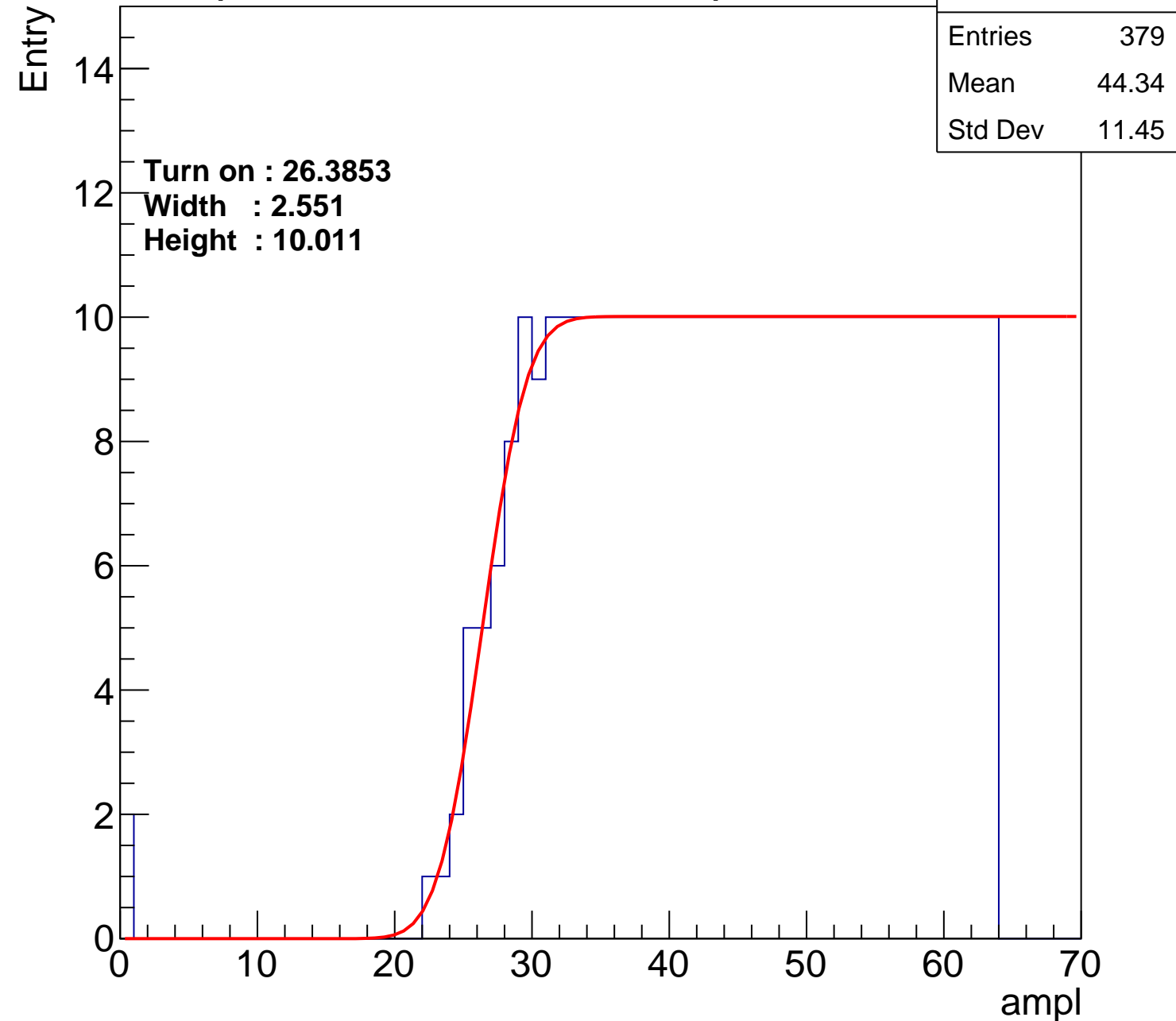
Width : 2.551

Height : 10.011

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U4-ch104

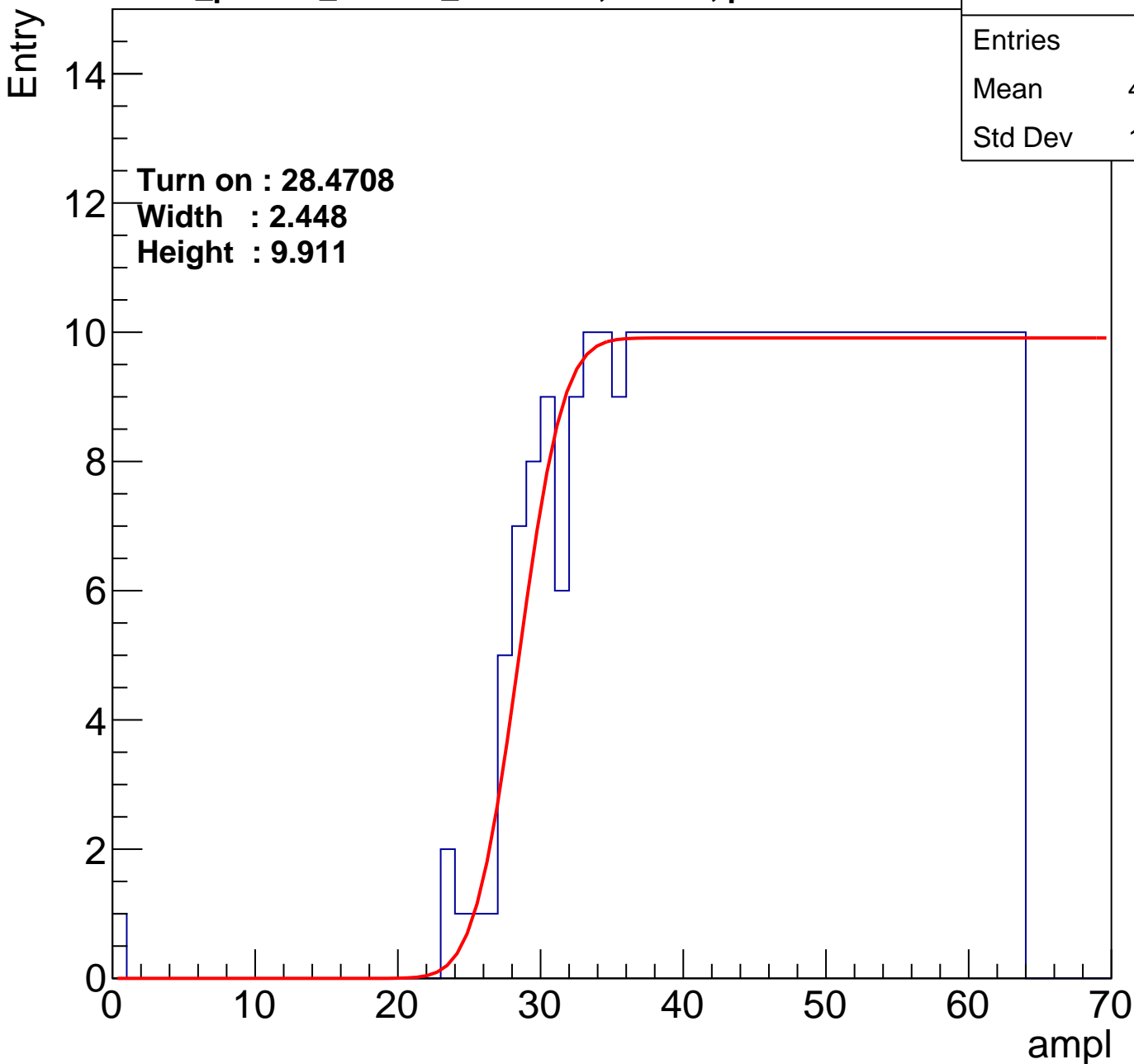
calib_packv5_042523_0143.root, FC#13, port D2

Entries	359
Mean	45.33
Std Dev	10.82

Turn on : 28.4708

Width : 2.448

Height : 9.911



B1L003S, U4-ch105

calib_packv5_042523_0143.root, FC#13, port D2

Entries	361
Mean	45.12
Std Dev	11.14

Turn on : 27.9376

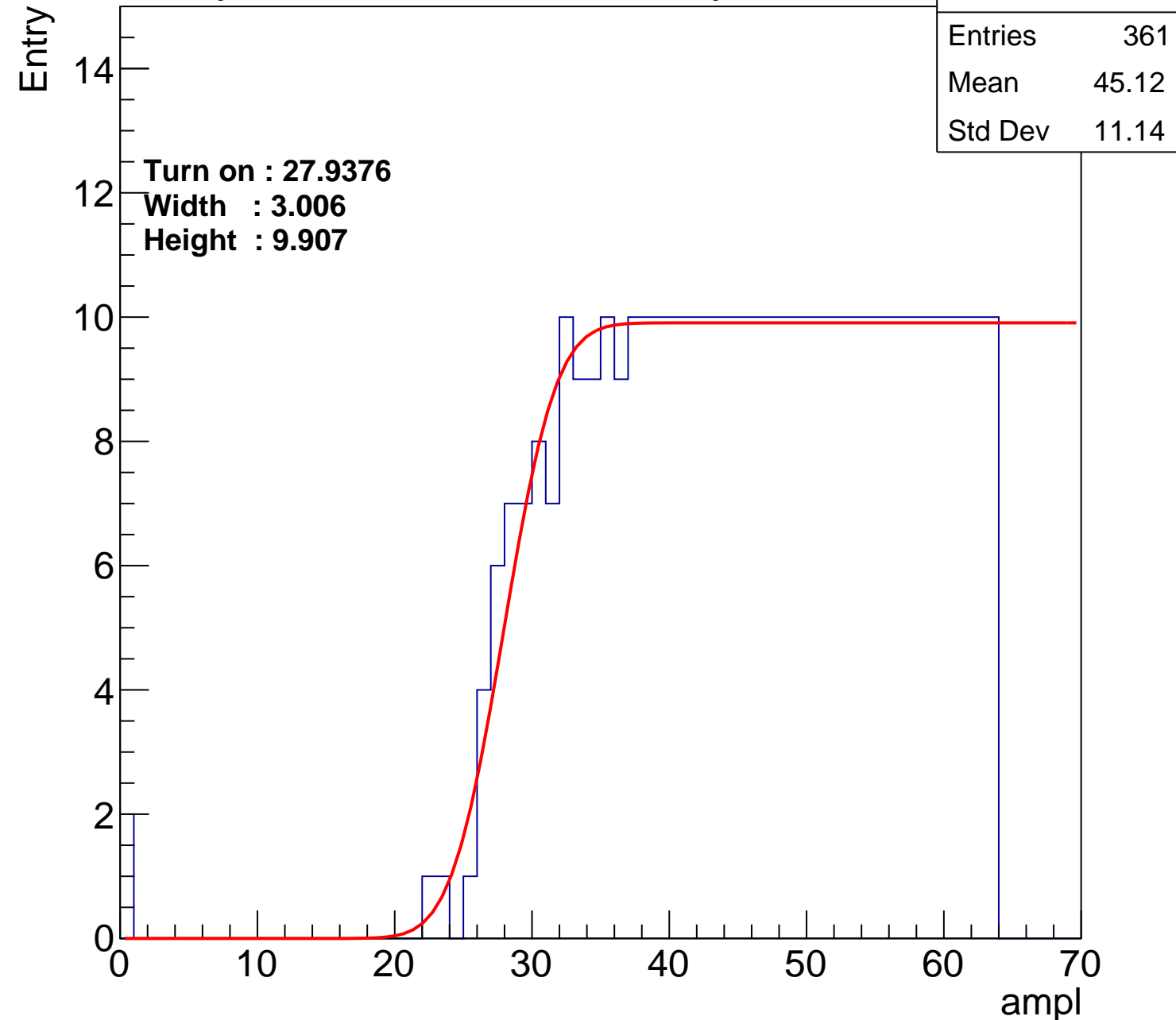
Width : 3.006

Height : 9.907

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U4-ch106

calib_packv5_042523_0143.root, FC#13, port D2

Entries	374
Mean	44.14
Std Dev	12.46

Turn on : 27.6073

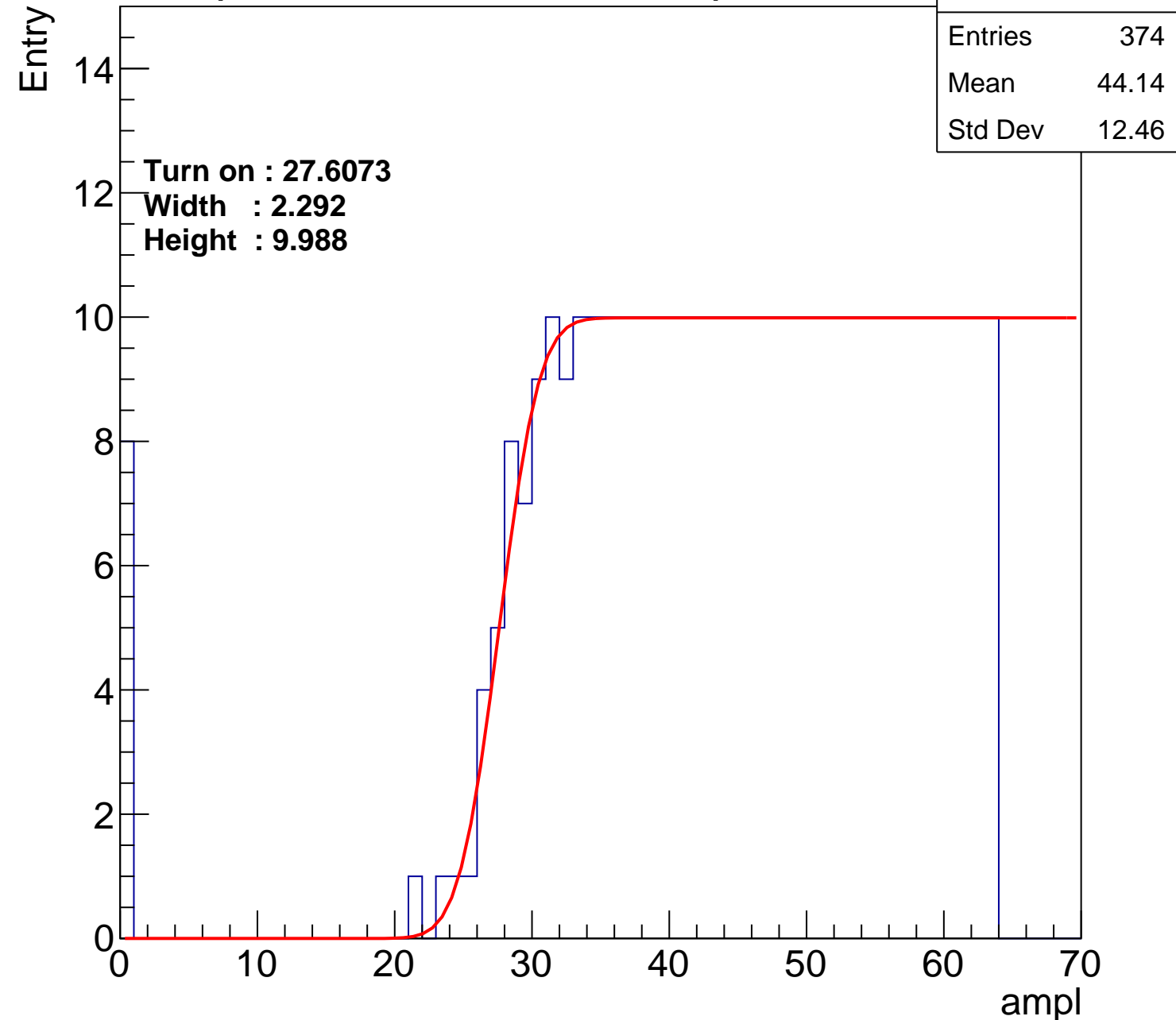
Width : 2.292

Height : 9.988

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U4-ch107

calib_packv5_042523_0143.root, FC#13, port D2

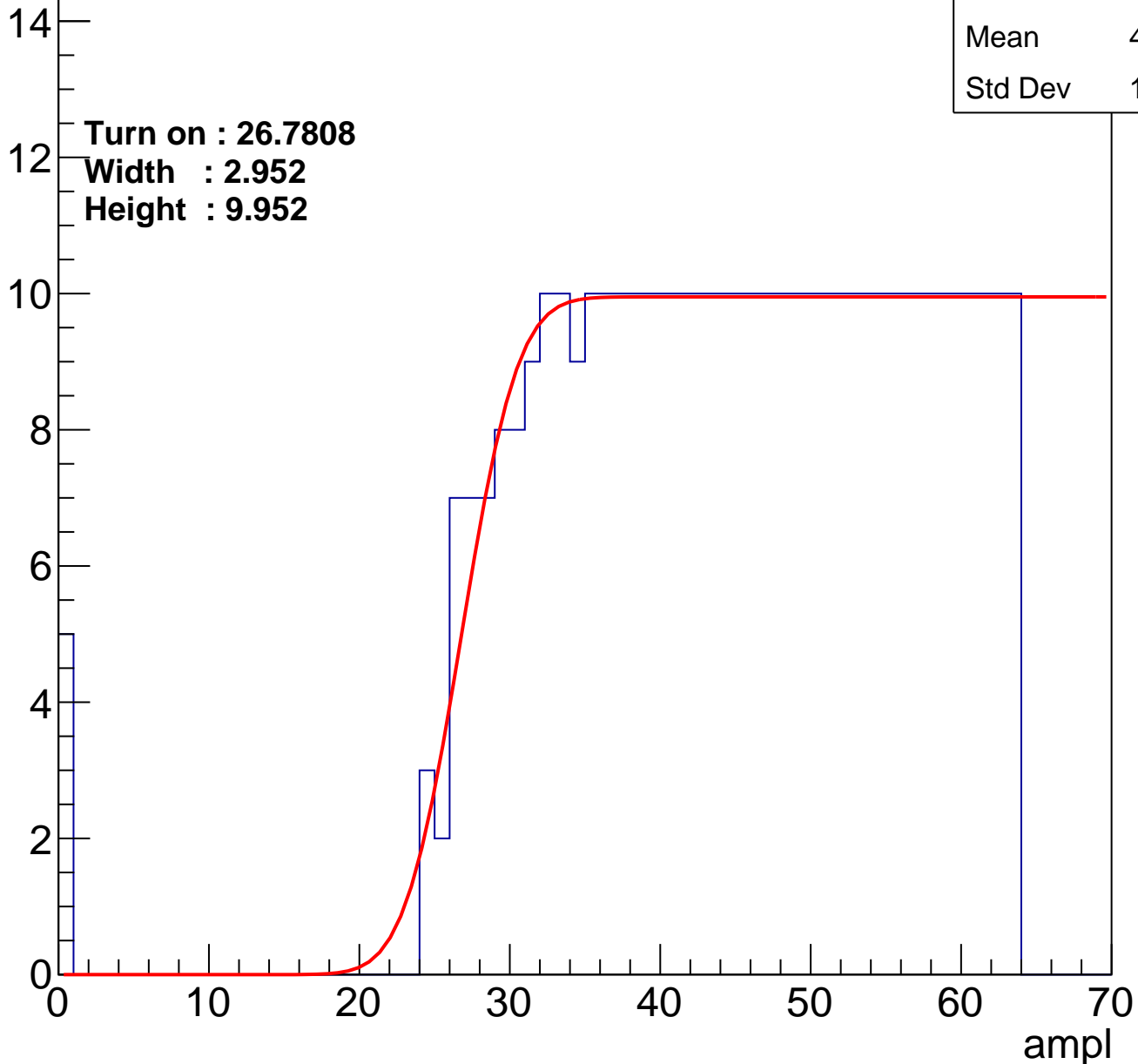
Entries	375
Mean	44.28
Std Dev	11.96

Turn on : 26.7808

Width : 2.952

Height : 9.952

Entry



B1L003S, U4-ch108

calib_packv5_042523_0143.root, FC#13, port D2

Entries	373
Mean	44.43
Std Dev	11.84

Turn on : 27.2864

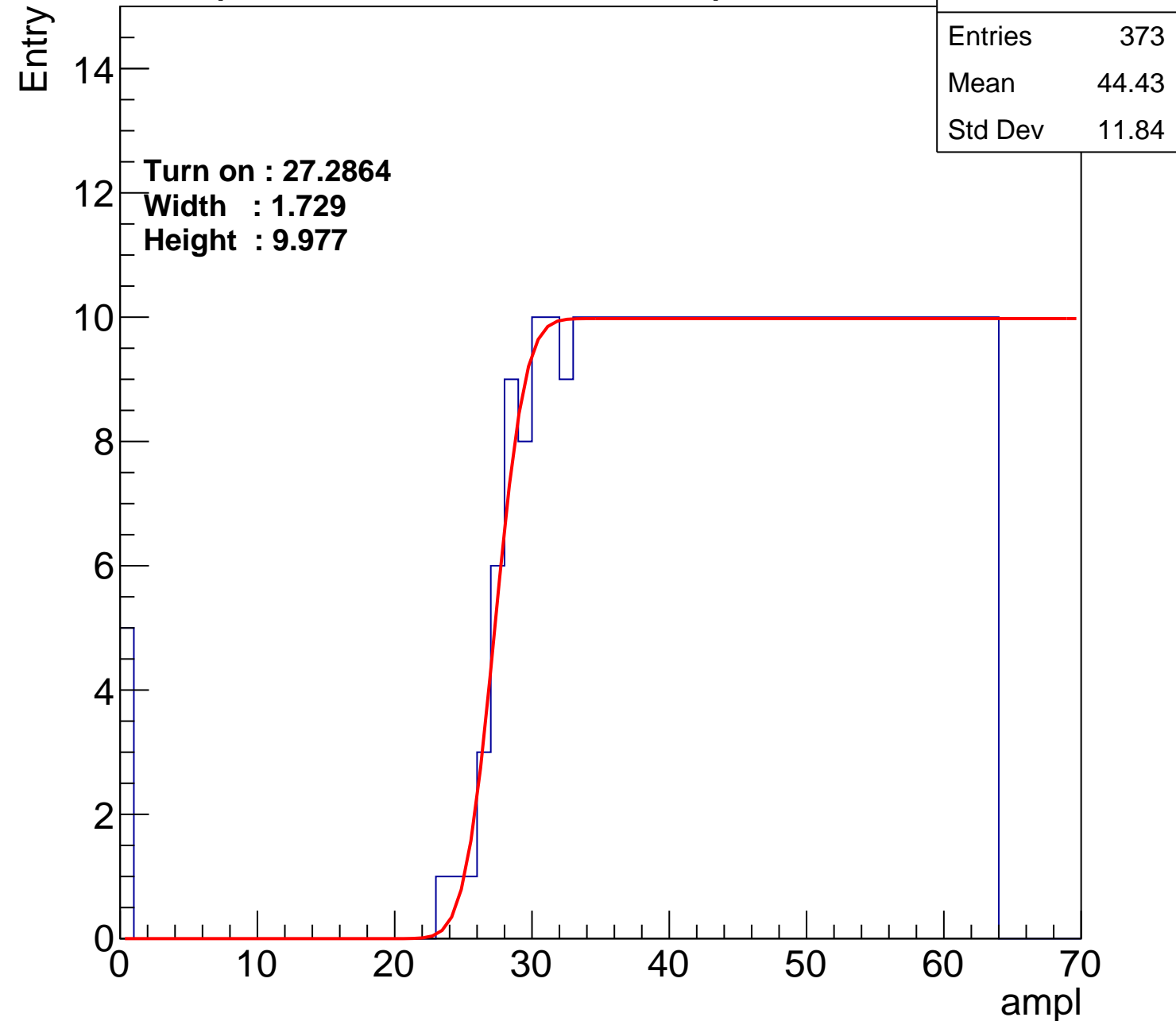
Width : 1.729

Height : 9.977

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U4-ch109

calib_packv5_042523_0143.root, FC#13, port D2

Entries	379
Mean	44.1
Std Dev	12.05

Turn on : 26.7542

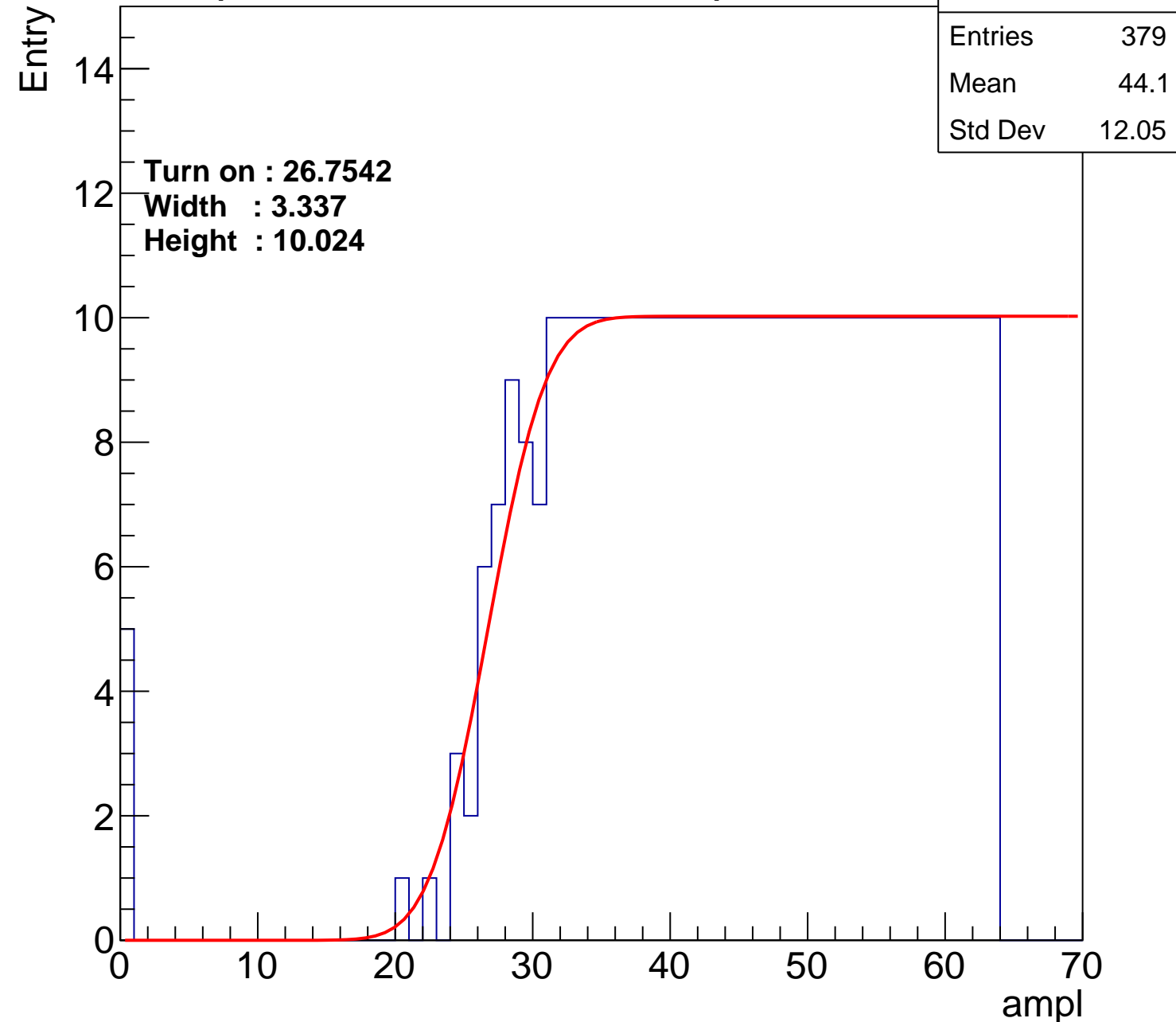
Width : 3.337

Height : 10.024

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U4-ch110

calib_packv5_042523_0143.root, FC#13, port D2

Entries	379
Mean	44.42
Std Dev	11.24

Turn on : 26.0654

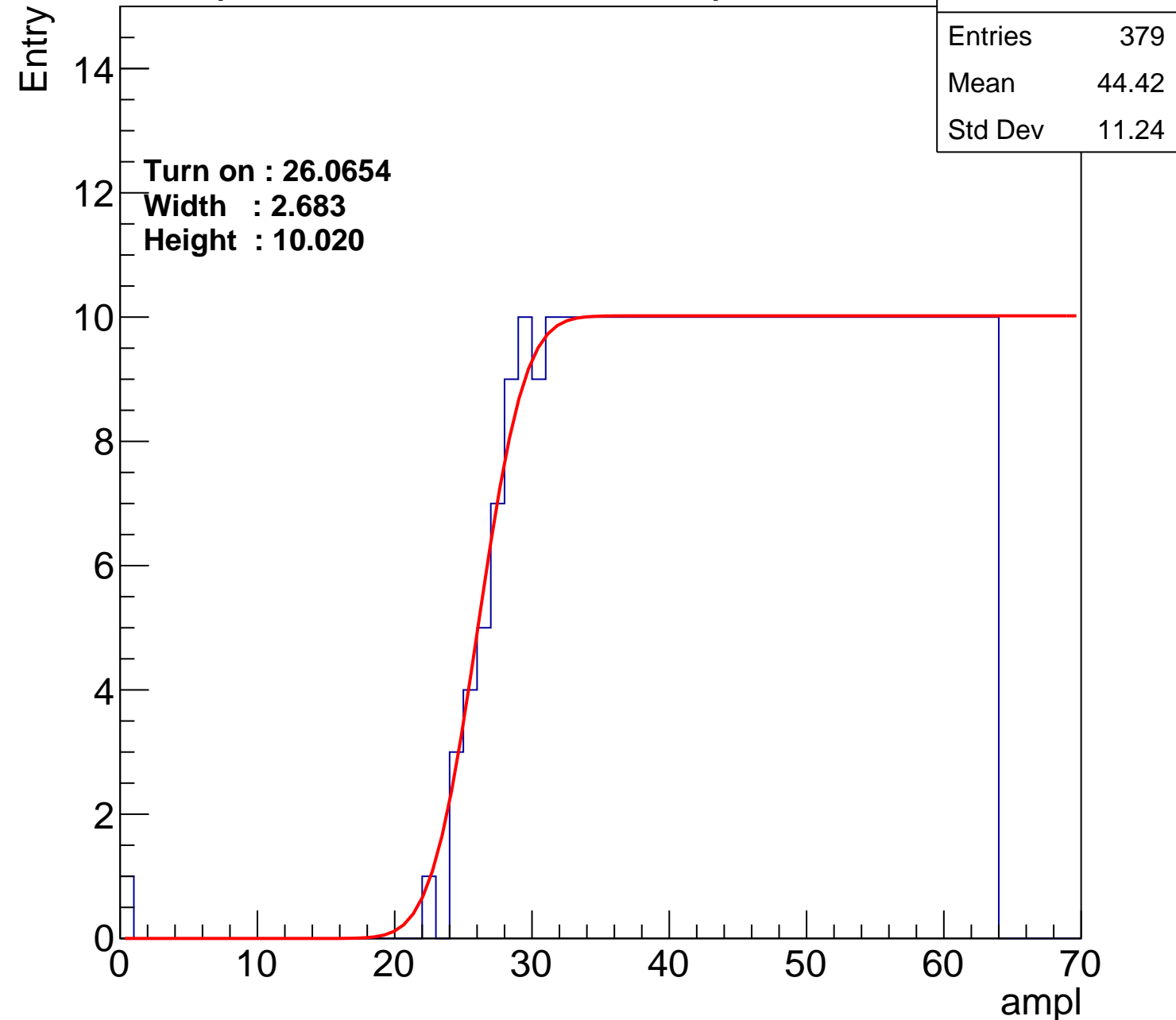
Width : 2.683

Height : 10.020

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U4-ch111

calib_packv5_042523_0143.root, FC#13, port D2

Entries	362
Mean	45.16
Std Dev	11.04

Turn on : 28.0293

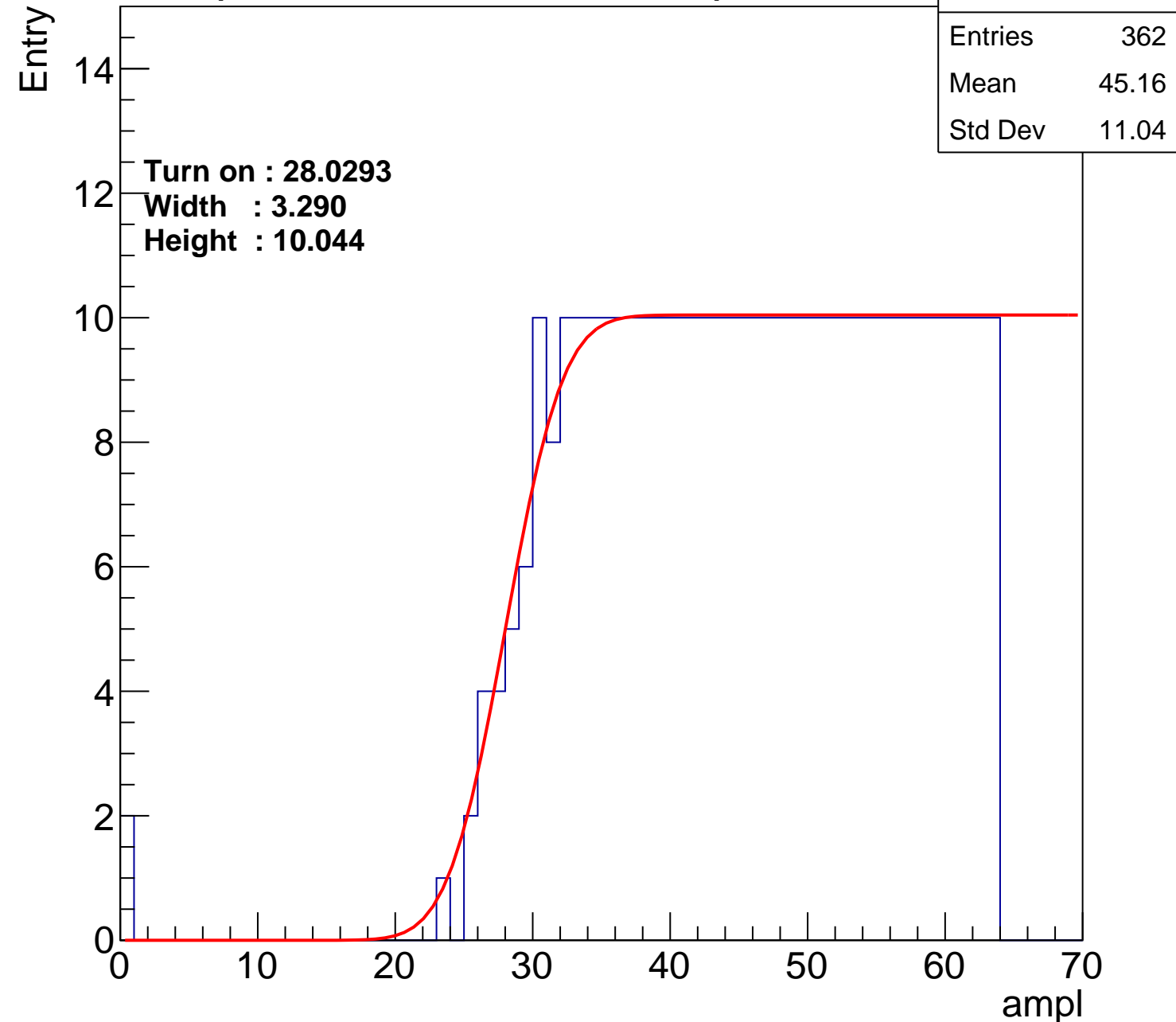
Width : 3.290

Height : 10.044

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U4-ch112

calib_packv5_042523_0143.root, FC#13, port D2

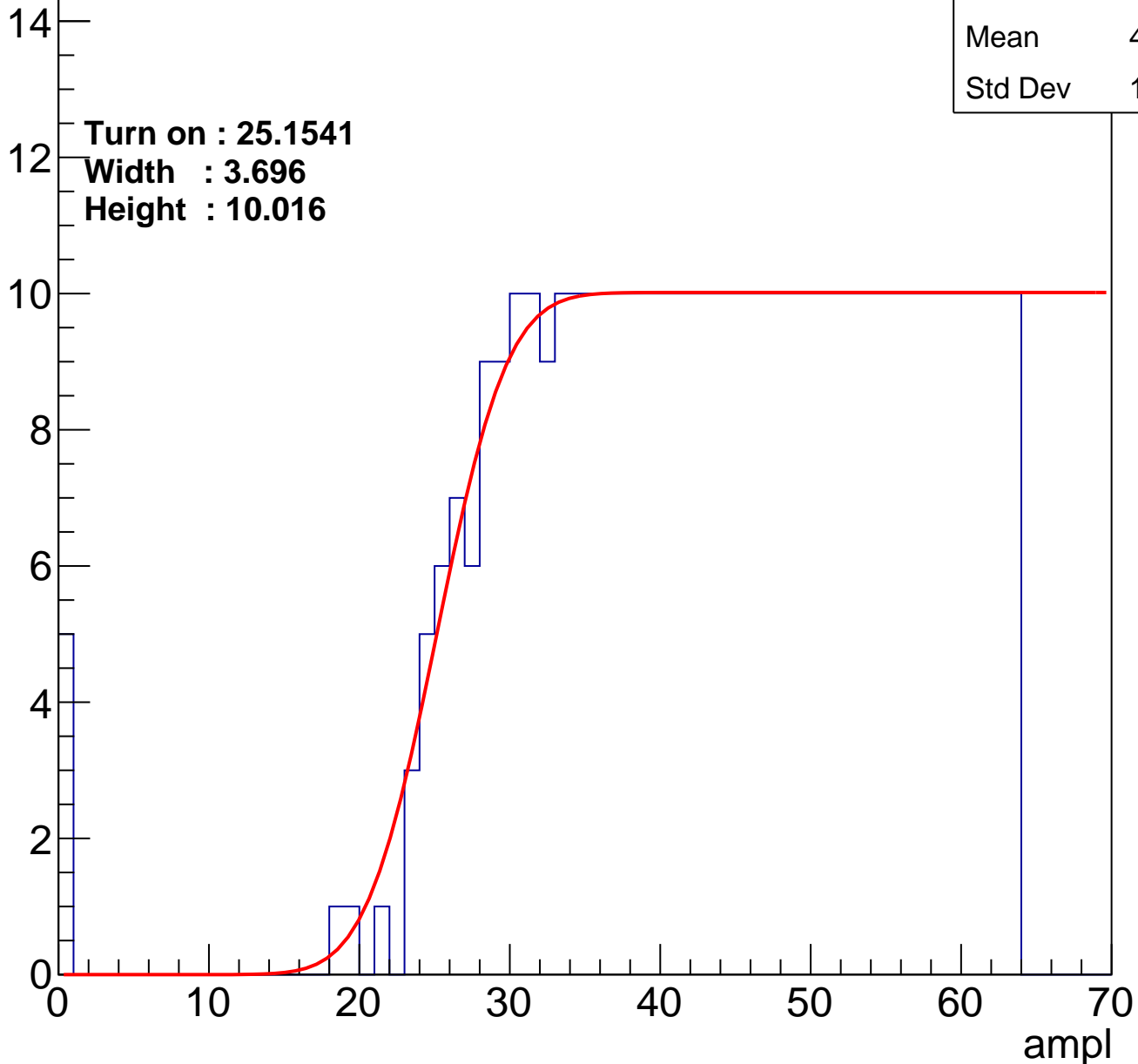
Entries	392
Mean	43.45
Std Dev	12.36

Turn on : 25.1541

Width : 3.696

Height : 10.016

Entry



B1L003S, U4-ch113

calib_packv5_042523_0143.root, FC#13, port D2

Entries	364
Mean	45.11
Std Dev	10.93

Turn on : 28.3333

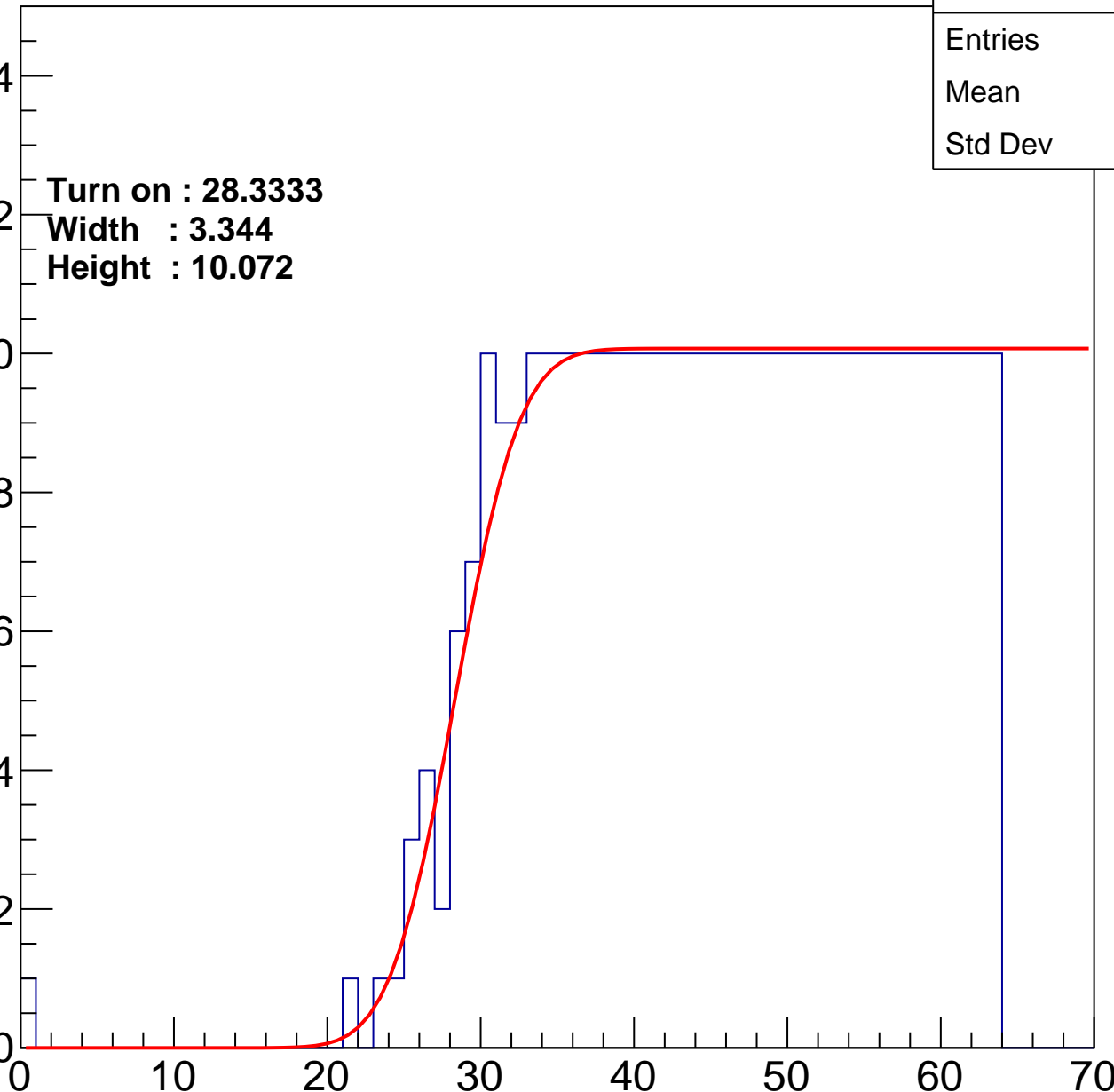
Width : 3.344

Height : 10.072

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U4-ch114

calib_packv5_042523_0143.root, FC#13, port D2

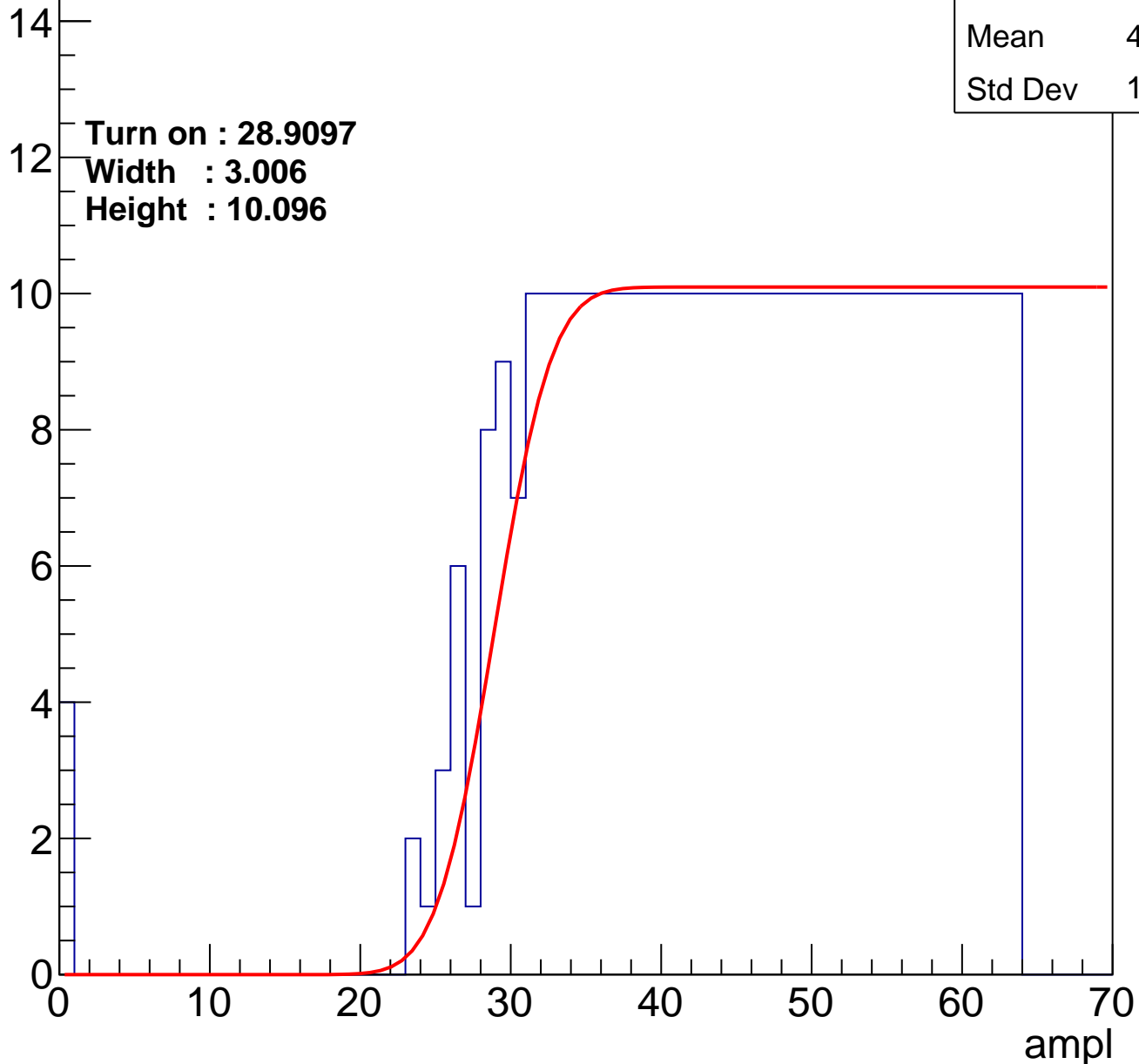
Entries	371
Mean	44.56
Std Dev	11.67

Turn on : 28.9097

Width : 3.006

Height : 10.096

Entry



B1L003S, U4-ch115

calib_packv5_042523_0143.root, FC#13, port D2

Entries	363
Mean	44.95
Std Dev	11.38

Turn on : 27.9394

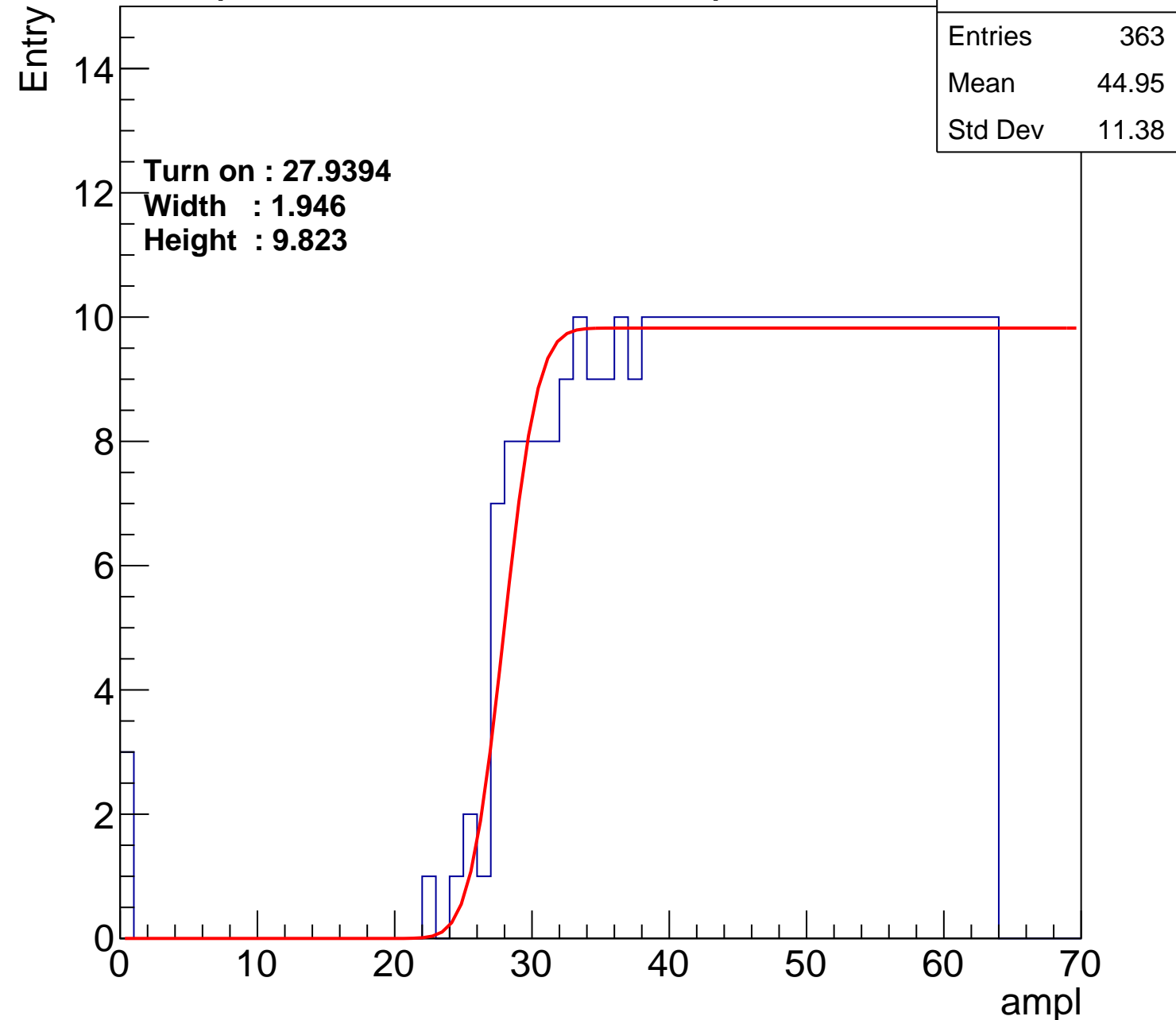
Width : 1.946

Height : 9.823

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U4-ch116

calib_packv5_042523_0143.root, FC#13, port D2

Entries	372
Mean	44.27
Std Dev	12.29

Turn on : 27.7184

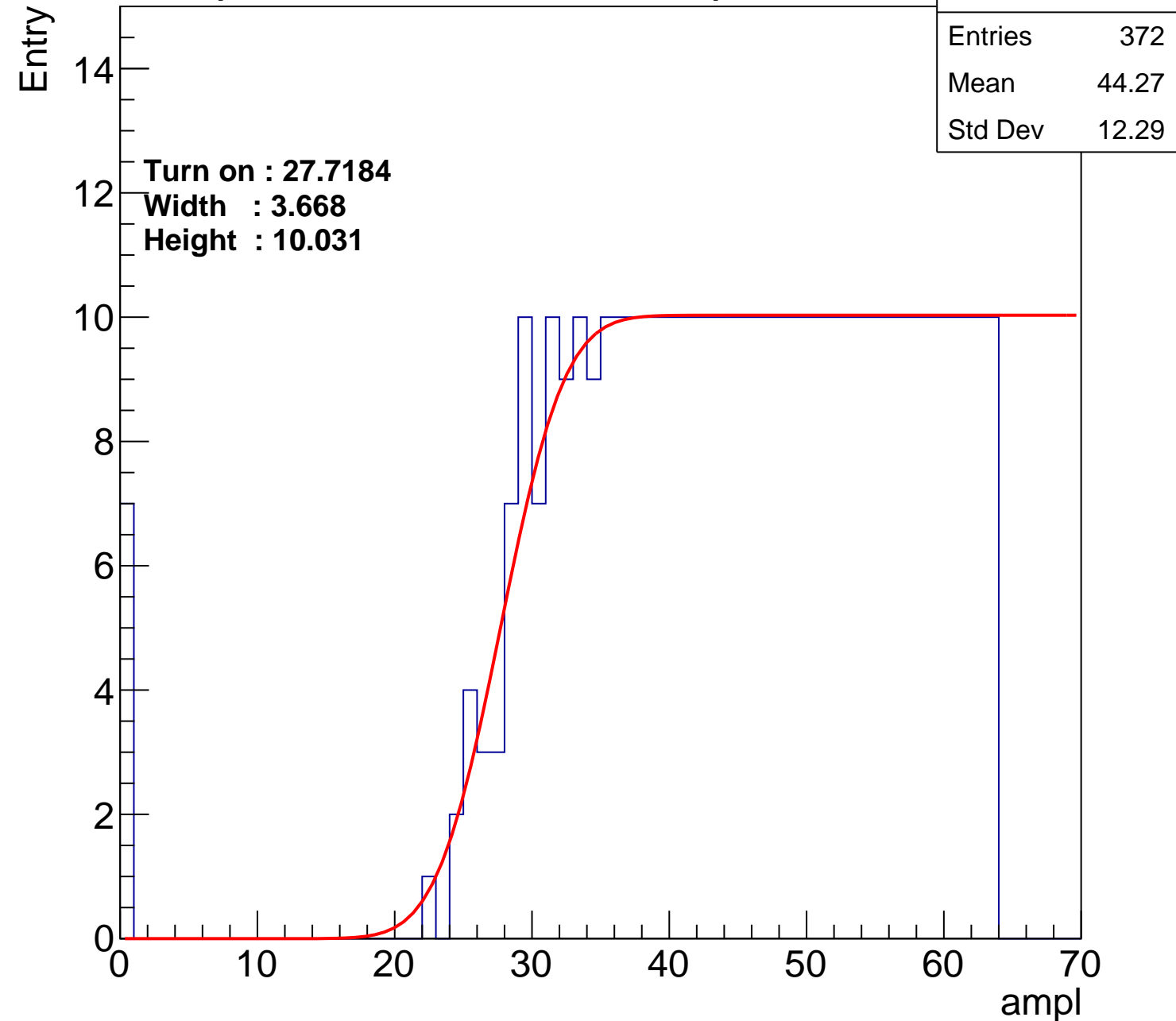
Width : 3.668

Height : 10.031

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U4-ch117

calib_packv5_042523_0143.root, FC#13, port D2

Entries	362
Mean	45.09
Std Dev	11.15

Turn on : 28.2366

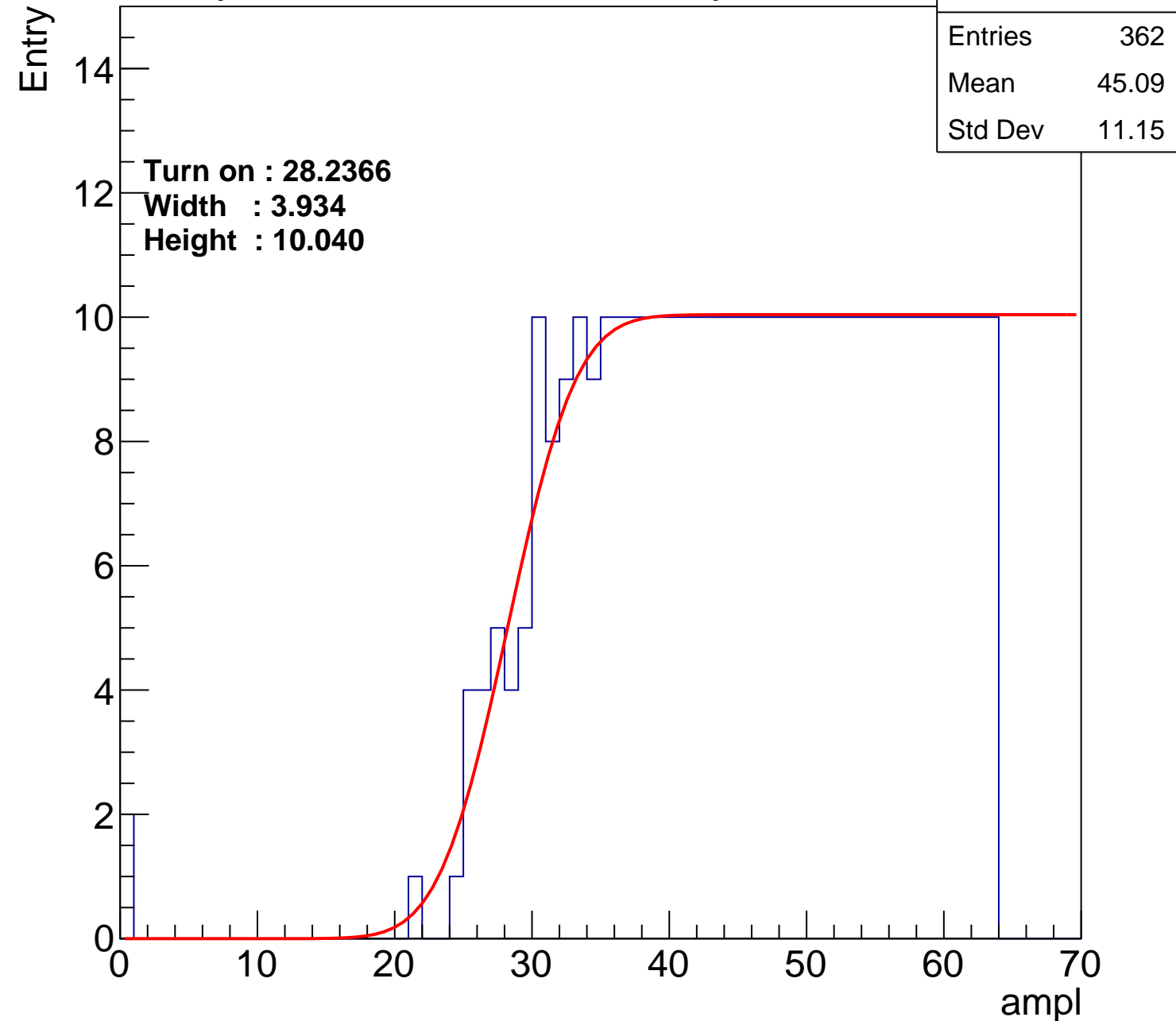
Width : 3.934

Height : 10.040

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U4-ch118

calib_packv5_042523_0143.root, FC#13, port D2

Entries	373
Mean	44.48
Std Dev	11.61

Turn on : 27.1405

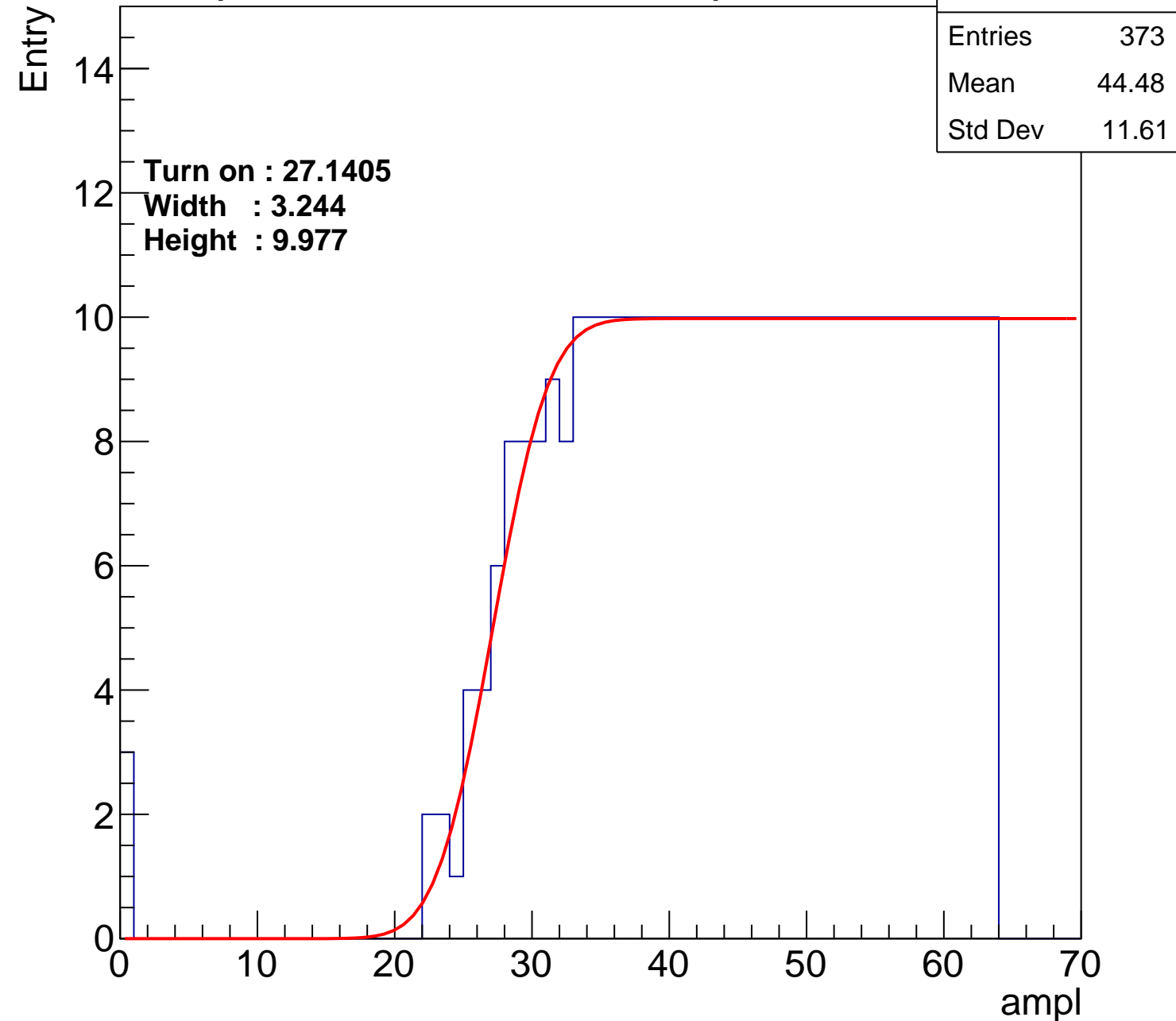
Width : 3.244

Height : 9.977

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U4-ch119

calib_packv5_042523_0143.root, FC#13, port D2

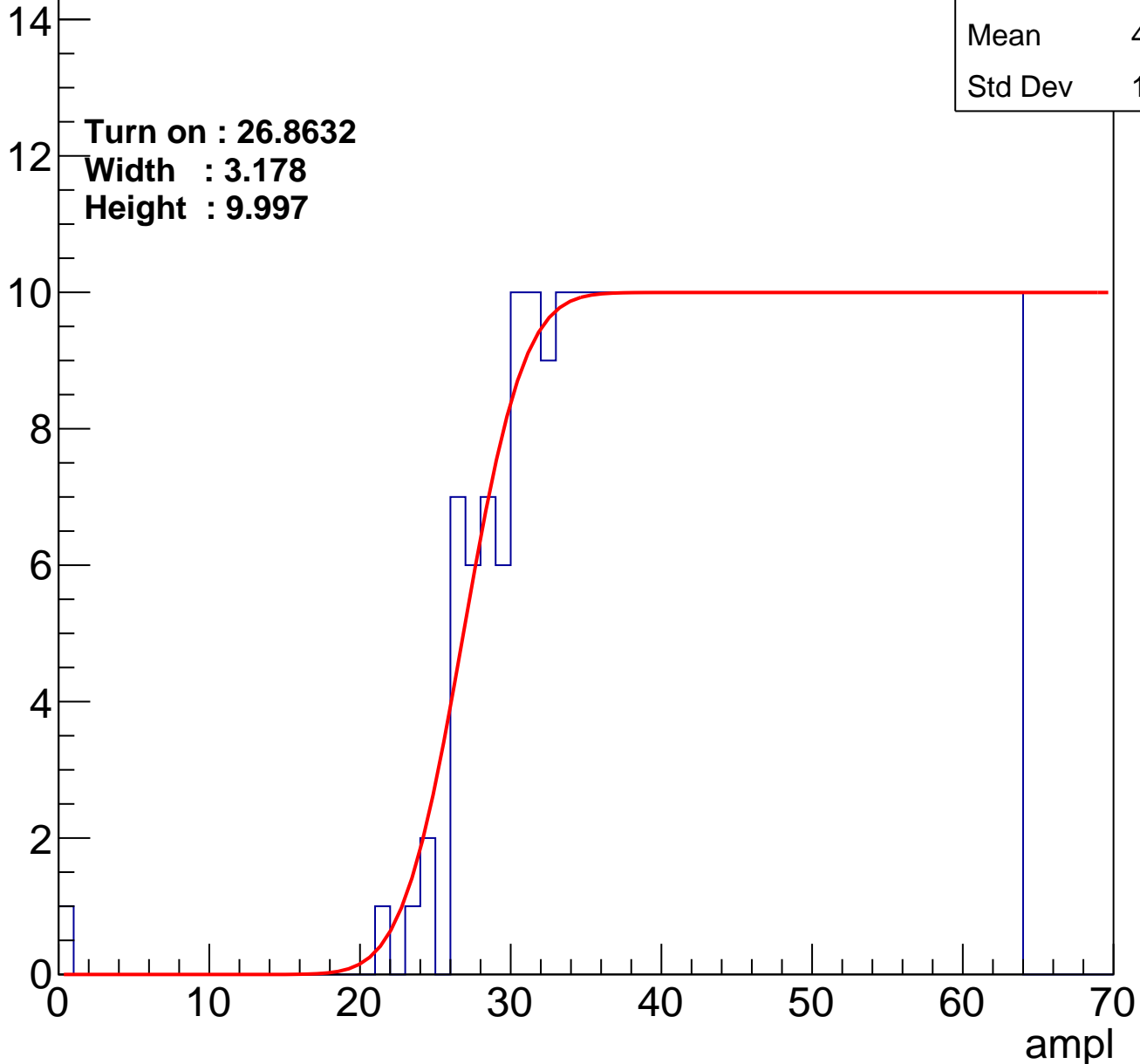
Entries	370
Mean	44.82
Std Dev	11.07

Turn on : 26.8632

Width : 3.178

Height : 9.997

Entry



calib_packv5_042523_0143.root, FC#13, port D2

calib_packv5_042523_0143.root, FC#13, port D2

Entries	354
Mean	45.54
Std Dev	10.85

Height : 9.908



14

12

10

8

6

4

2

0

0

10

20

30

40

50

60

ampl

B1L003S, U4-ch121

calib_packv5_042523_0143.root, FC#13, port D2

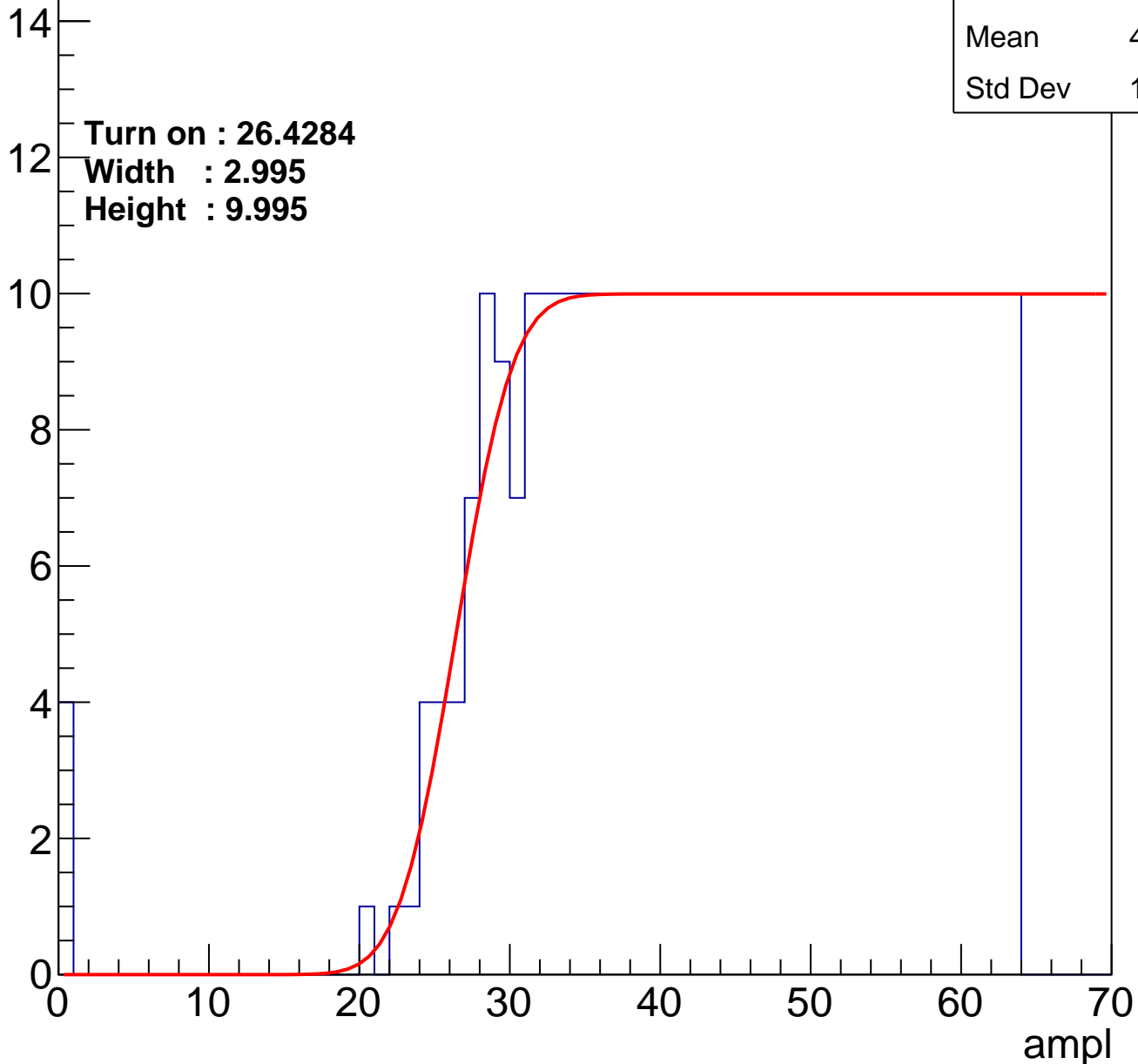
Entries	382
Mean	44.02
Std Dev	11.94

Turn on : 26.4284

Width : 2.995

Height : 9.995

Entry



B1L003S, U4-ch122

calib_packv5_042523_0143.root, FC#13, port D2

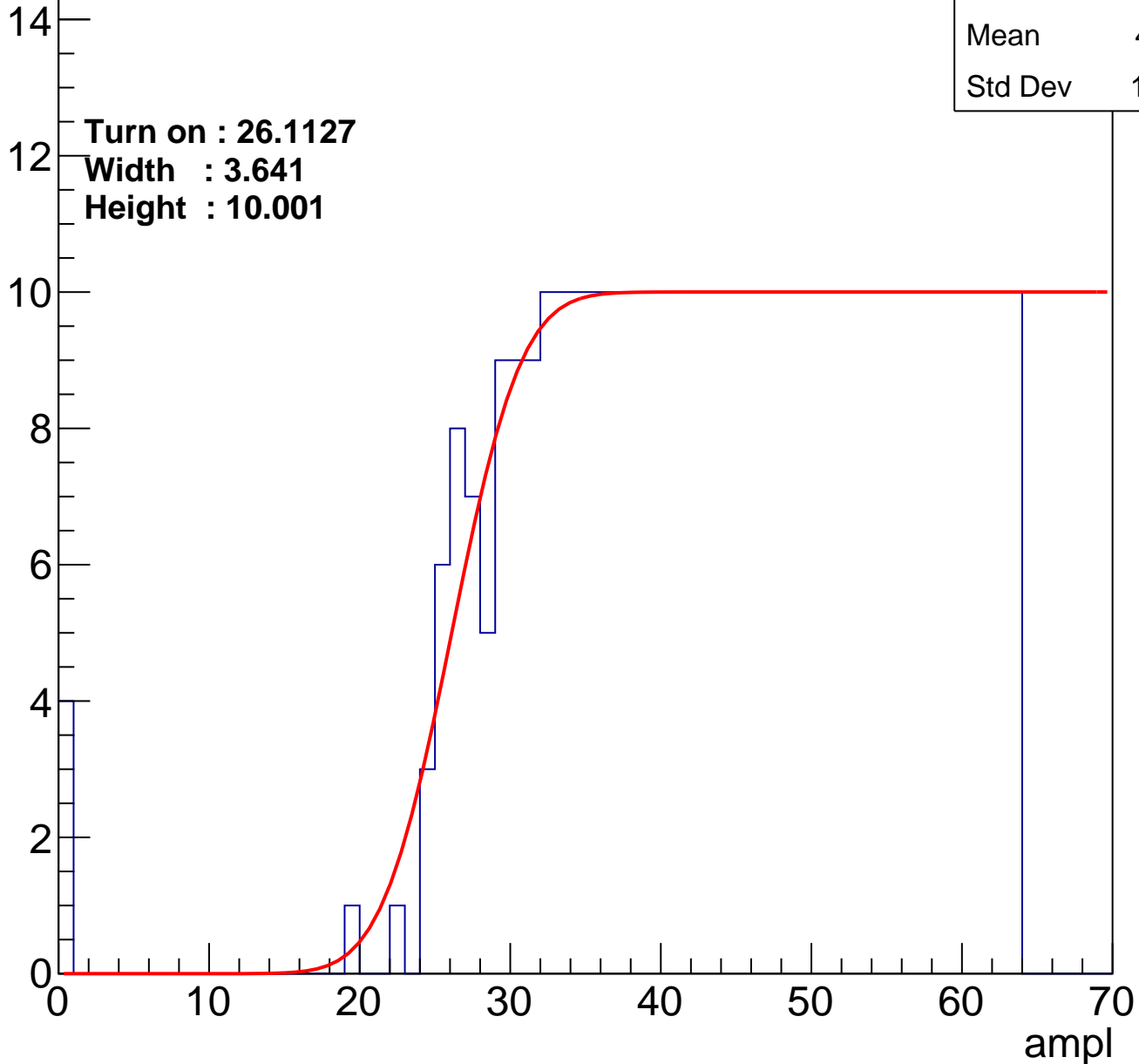
Entries	382
Mean	44.01
Std Dev	11.96

Turn on : 26.1127

Width : 3.641

Height : 10.001

Entry



B1L003S, U4-ch123

calib_packv5_042523_0143.root, FC#13, port D2

Entries	373
Mean	44.39
Std Dev	11.84

Turn on : 27.5636

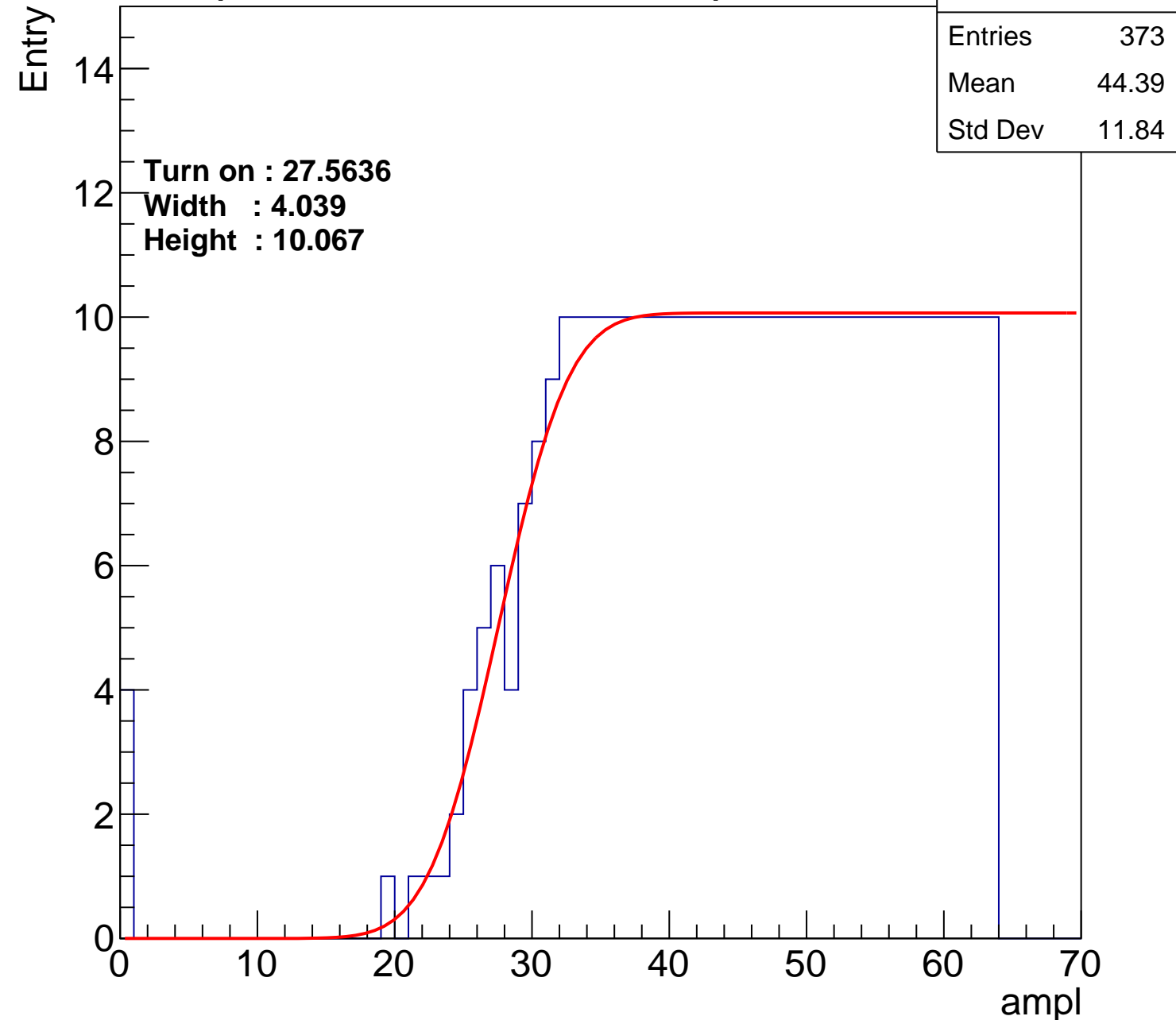
Width : 4.039

Height : 10.067

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U4-ch124

calib_packv5_042523_0143.root, FC#13, port D2

Entries	375
Mean	44.51
Std Dev	11.38

Turn on : 26.0743

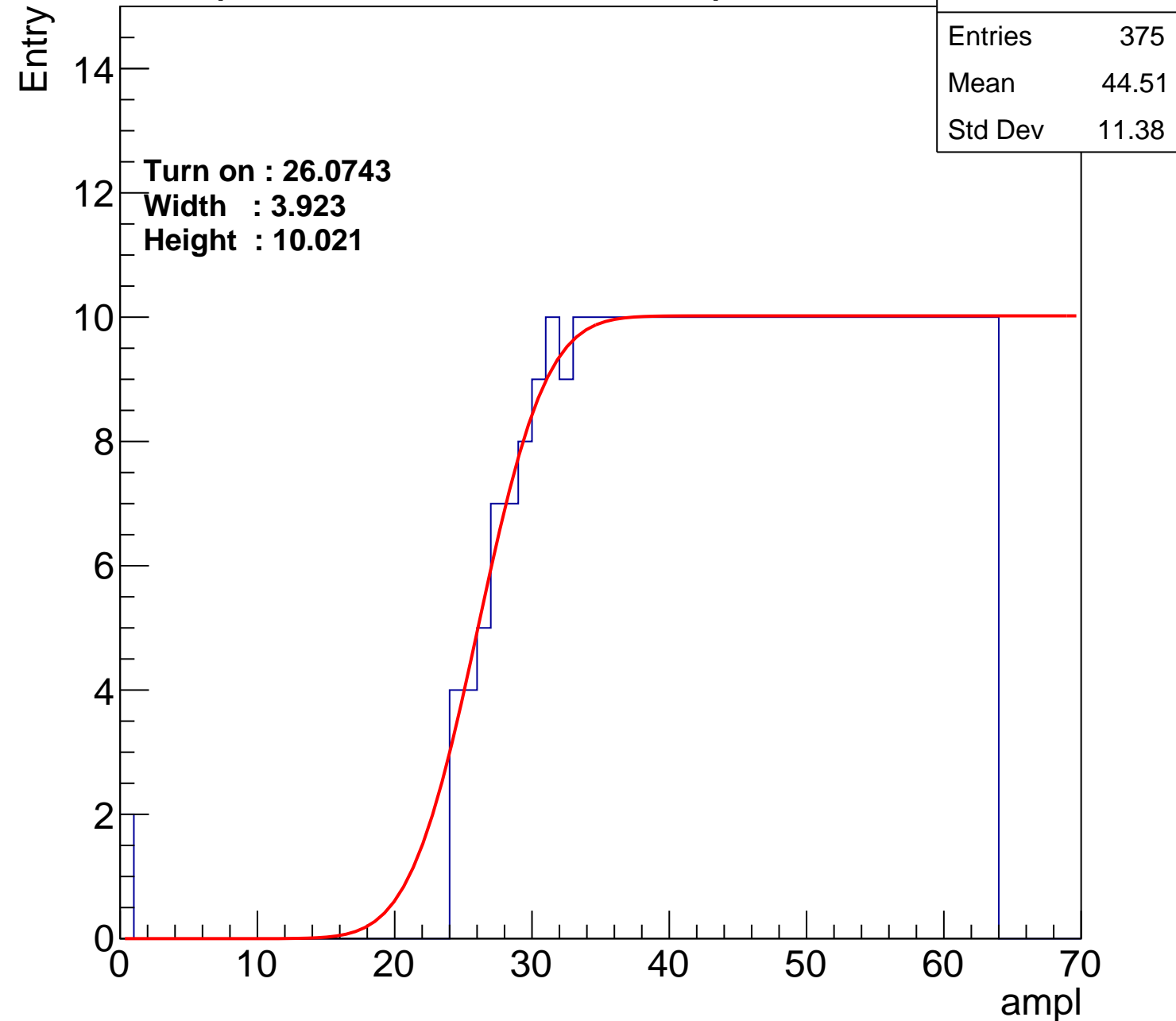
Width : 3.923

Height : 10.021

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U4-ch125

calib_packv5_042523_0143.root, FC#13, port D2

Entries	361
Mean	45.24
Std Dev	10.87

Turn on : 27.9661

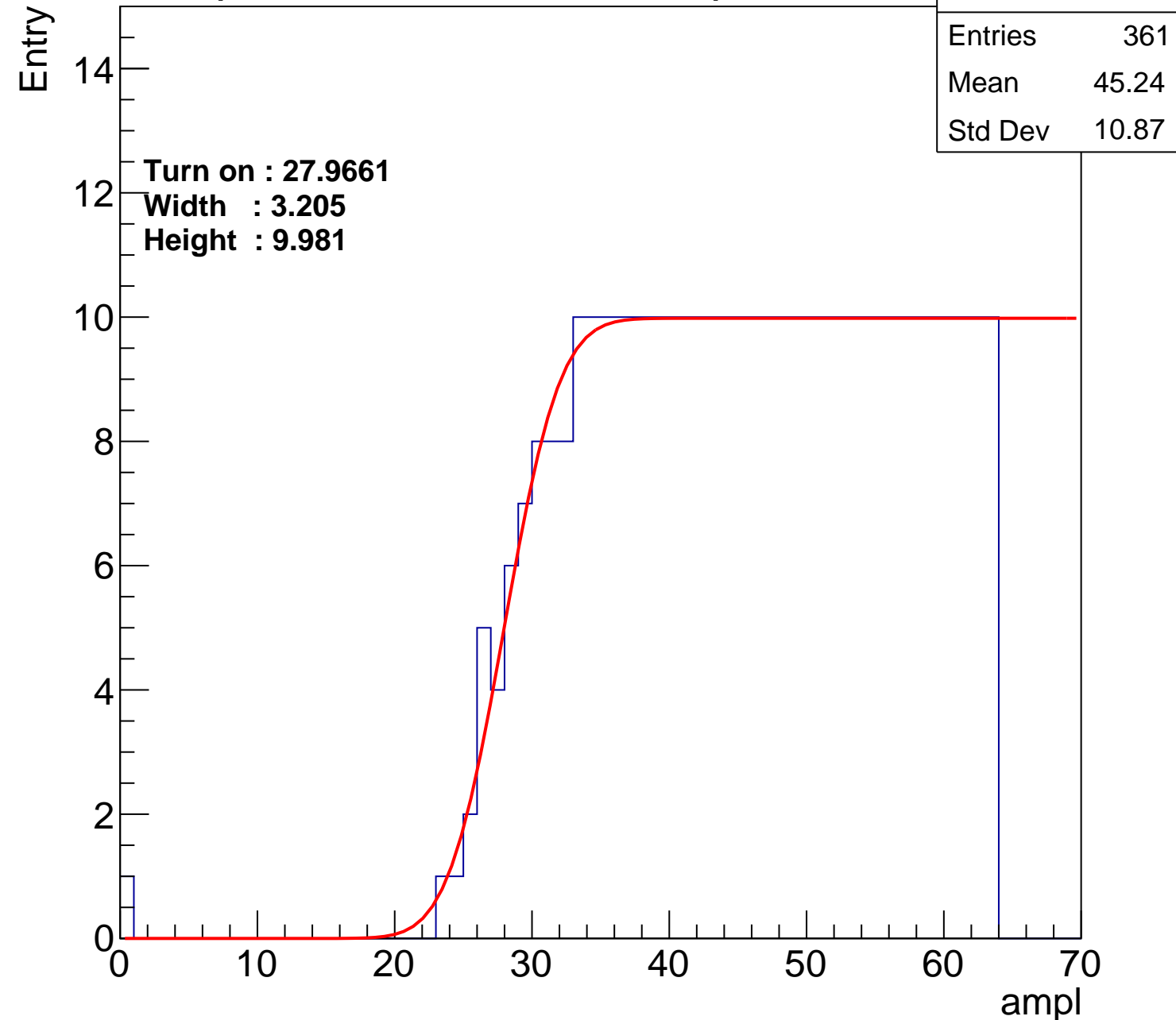
Width : 3.205

Height : 9.981

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U4-ch126

calib_packv5_042523_0143.root, FC#13, port D2

Entries	365
Mean	45
Std Dev	11.13

Turn on : 27.9068

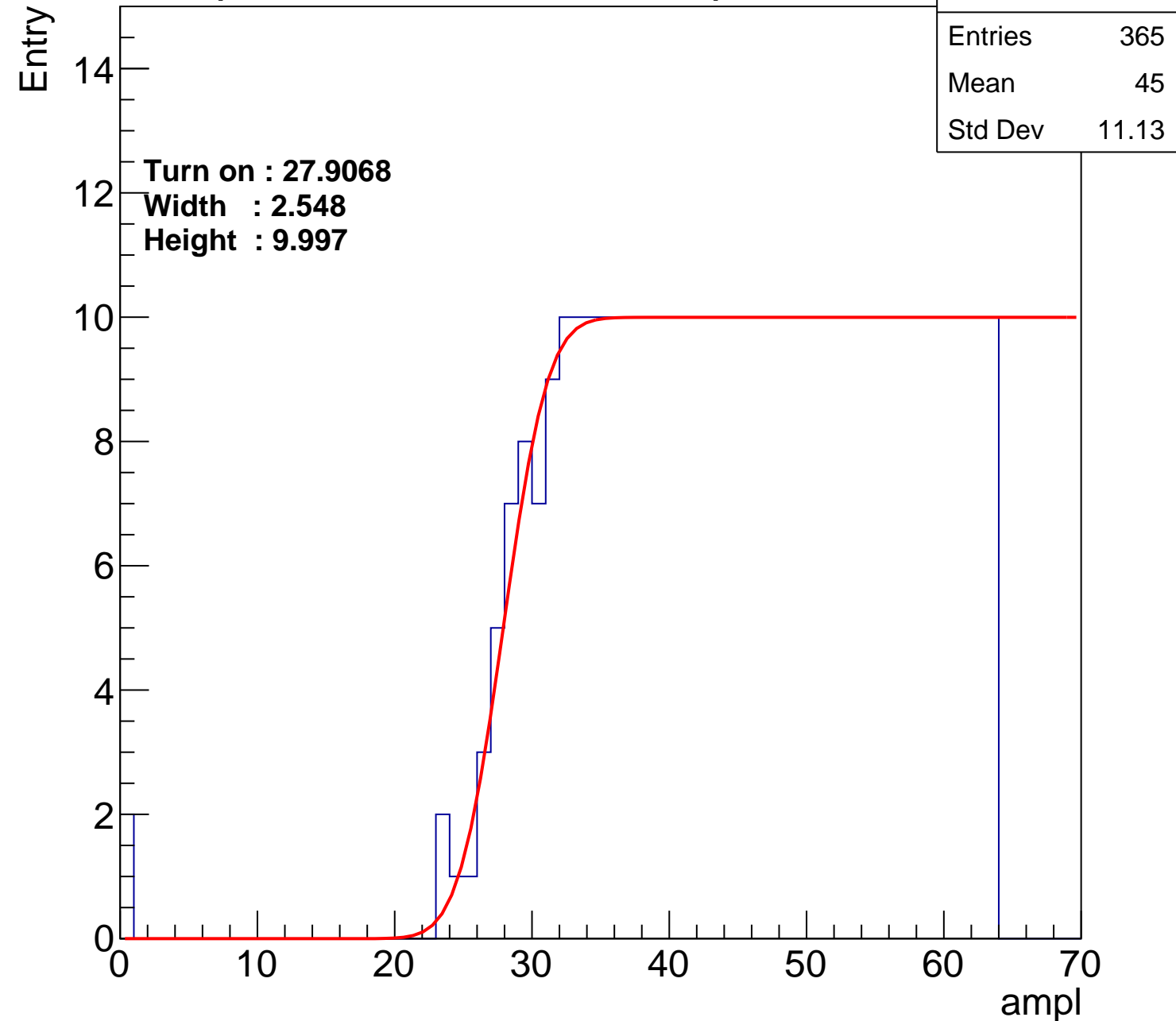
Width : 2.548

Height : 9.997

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U4-ch127

calib_packv5_042523_0143.root, FC#13, port D2

Entries	365
Mean	44.94
Std Dev	11.24

Turn on : 28.3677

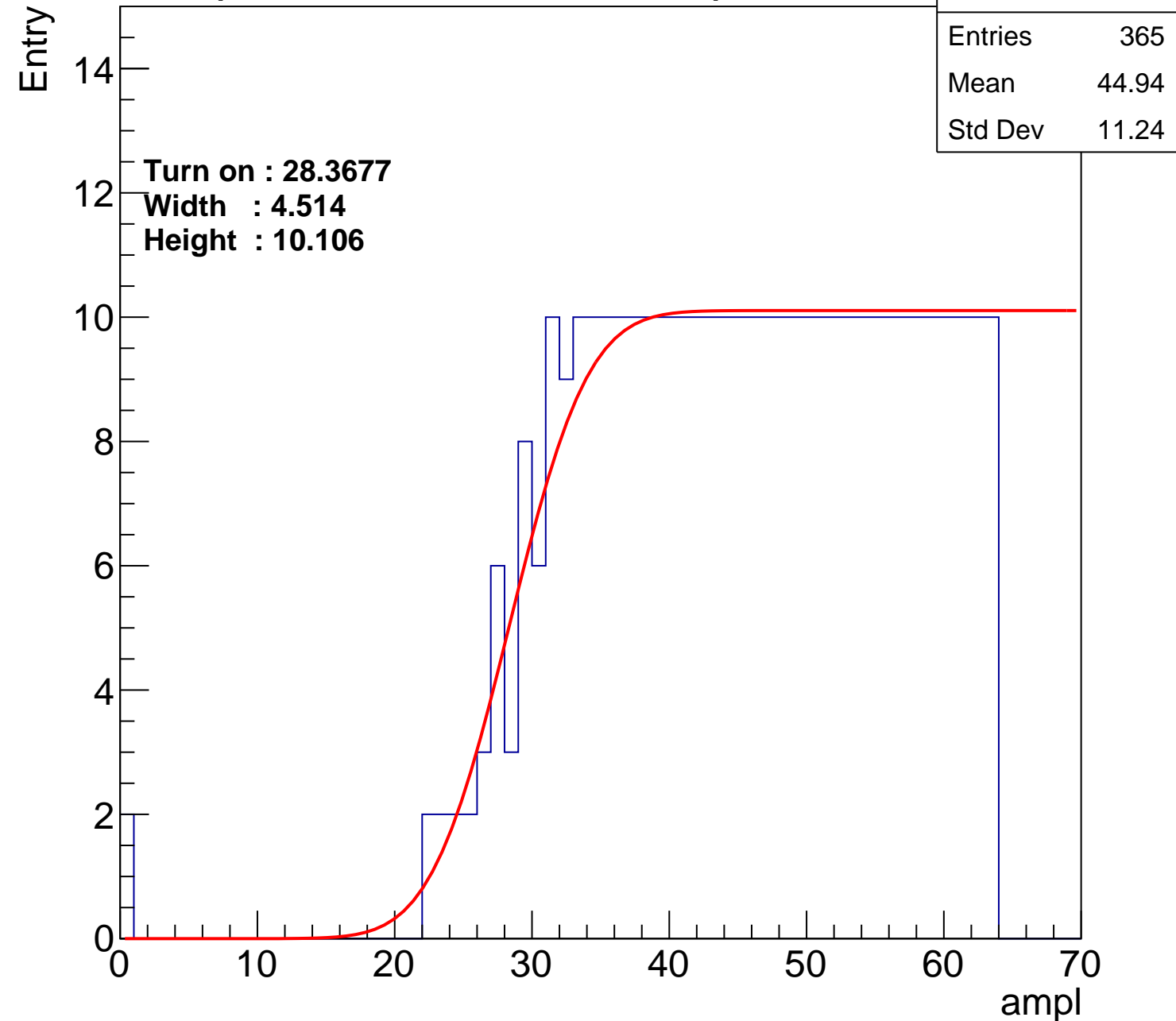
Width : 4.514

Height : 10.106

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U4-ch127

calib_packv5_042523_0143.root, FC#13, port D2

Entries	365
Mean	44.94
Std Dev	11.24

Turn on : 28.3677

Width : 4.514

Height : 10.106

Entry

14
12
10
8
6
4
2
0

ampl

