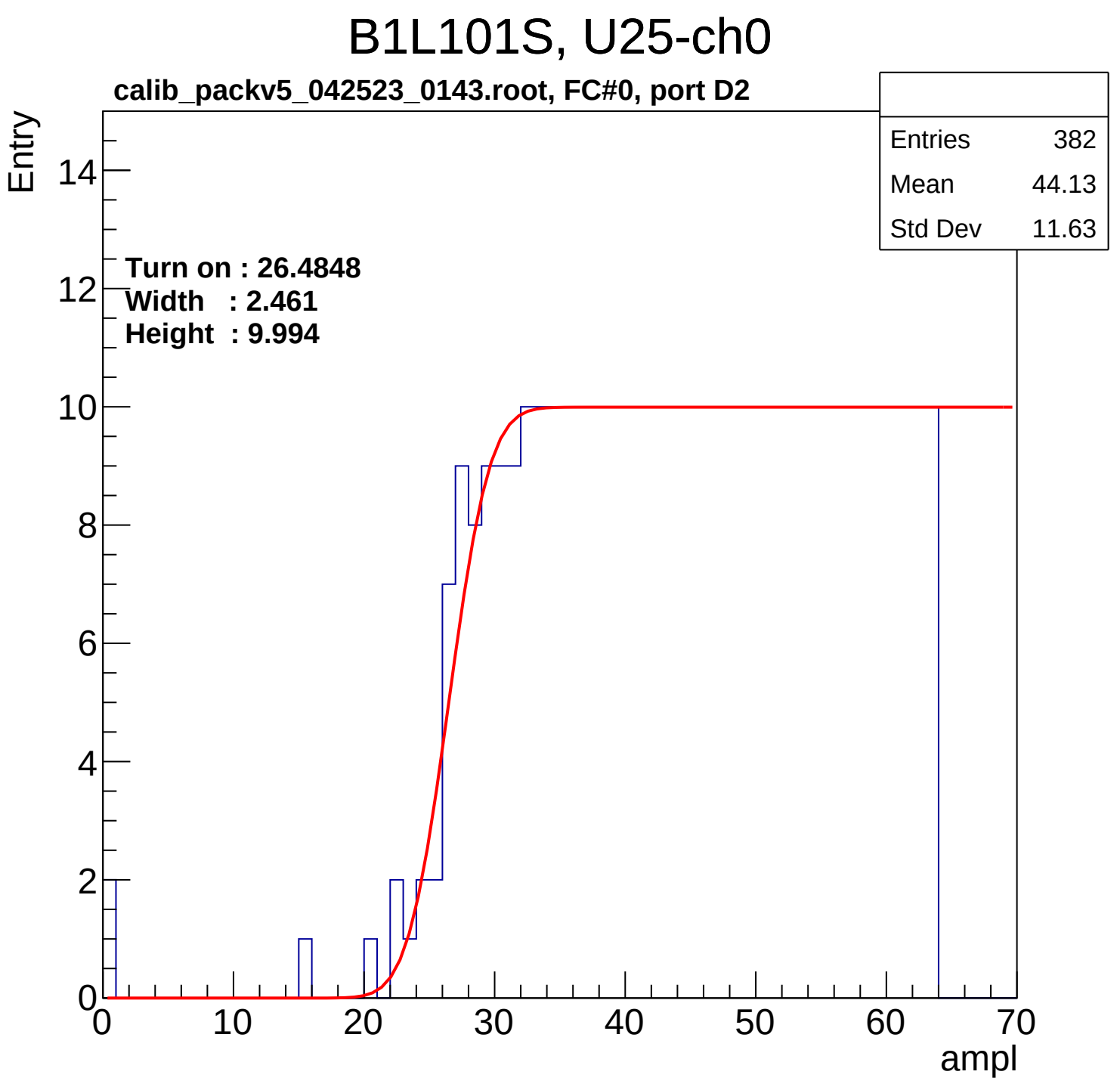
B1L101S, U25-ch0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 382
Mean 44.13
Std Dev 11.63
Turn on : 26.4848
Width : 2.461
Height : 9.994
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ampl
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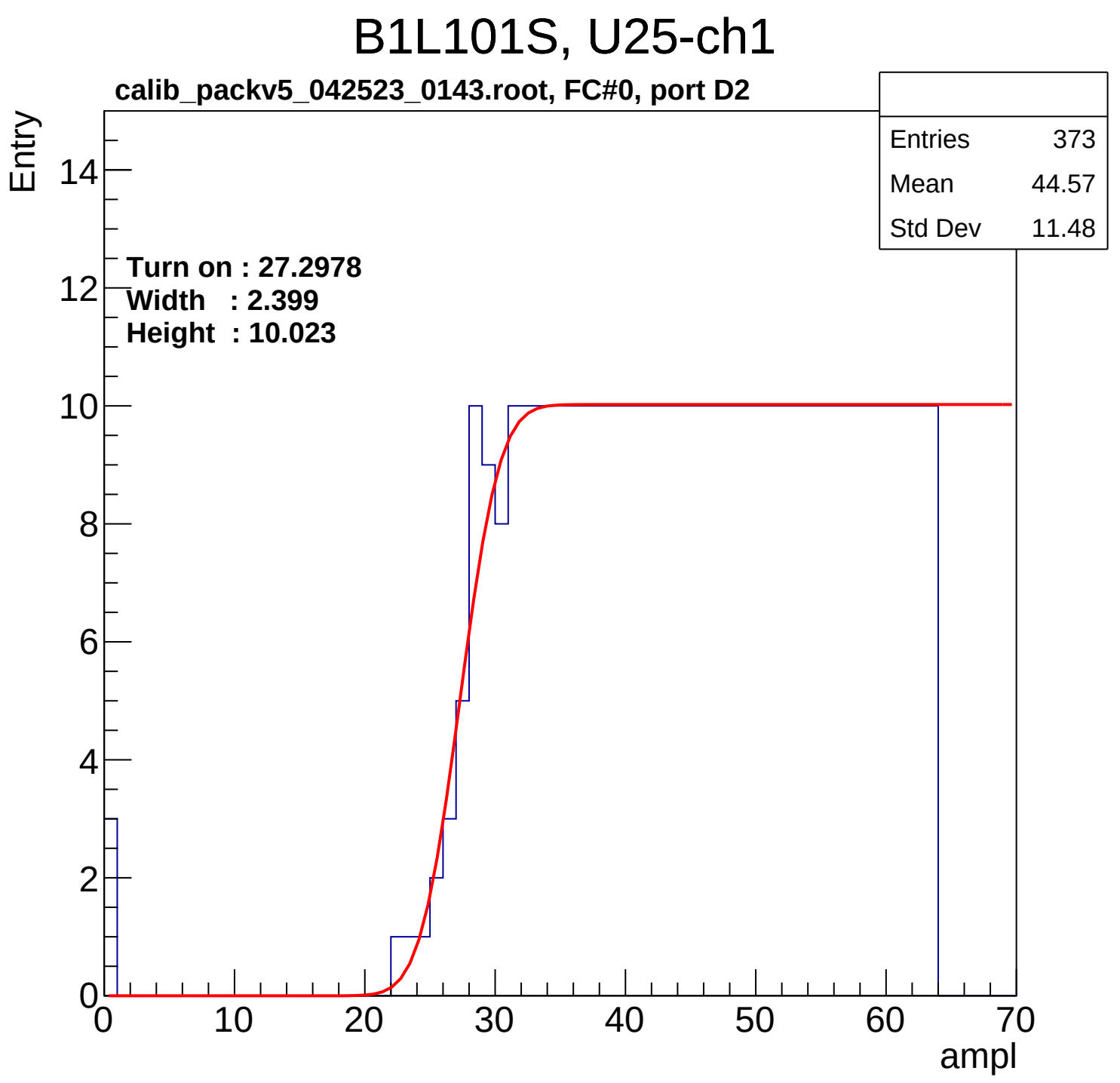
B1L101S, U25-ch1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 373
Mean 44.57
Std Dev 11.48
Turn on : 27.2978
Width : 2.399
Height : 10.023
Entry
ampl
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2
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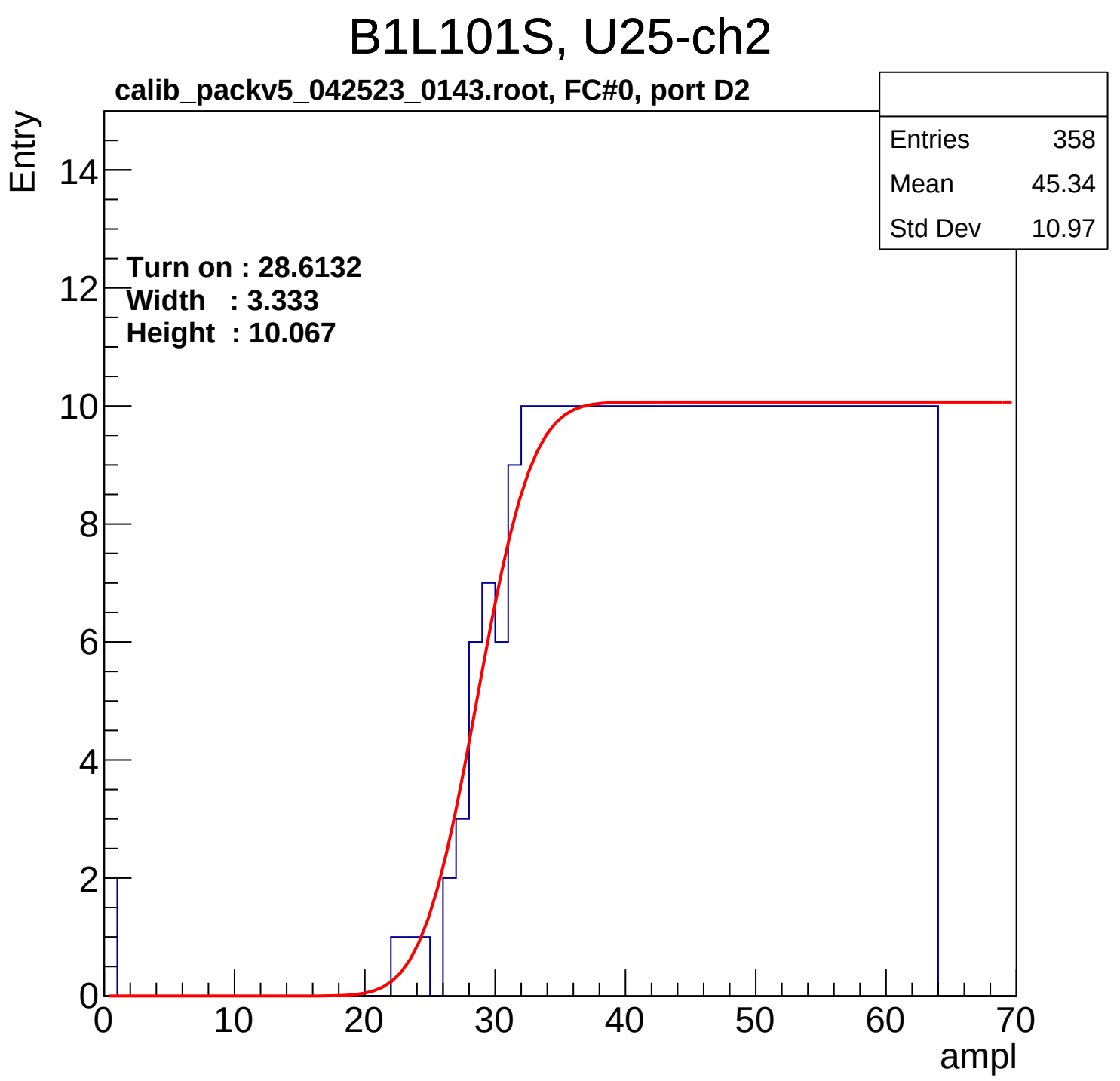
B1L101S, U25-ch2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 358
Mean 45.34
Std Dev 10.97
Turn on : 28.6132
Width : 3.333
Height : 10.067
Entry
ampl
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2
4
6
8
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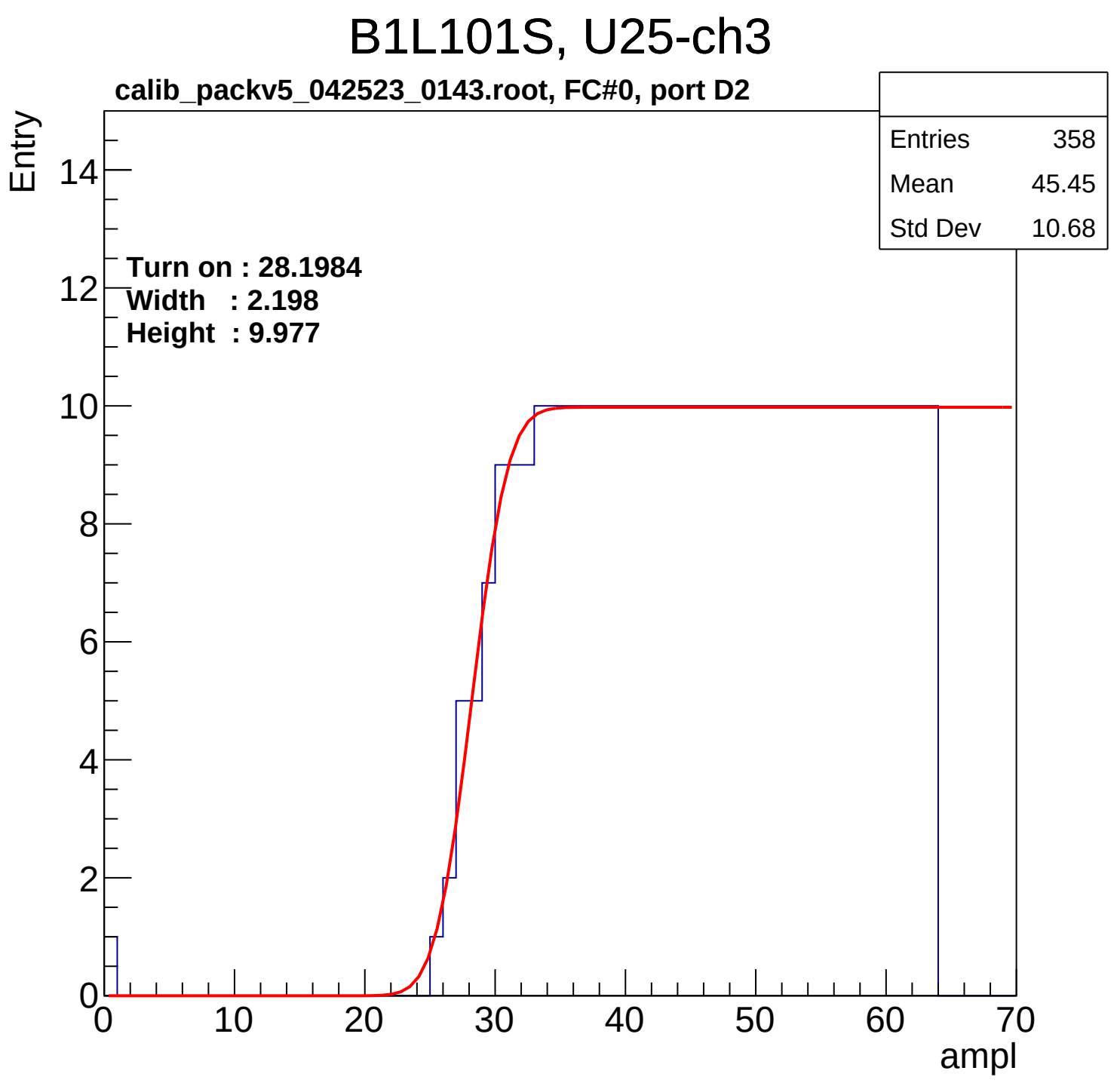
B1L101S, U25-ch3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 358
Mean 45.45
Std Dev 10.68
Turn on : 28.1984
Width : 2.198
Height : 9.977
Entry
ampl
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8
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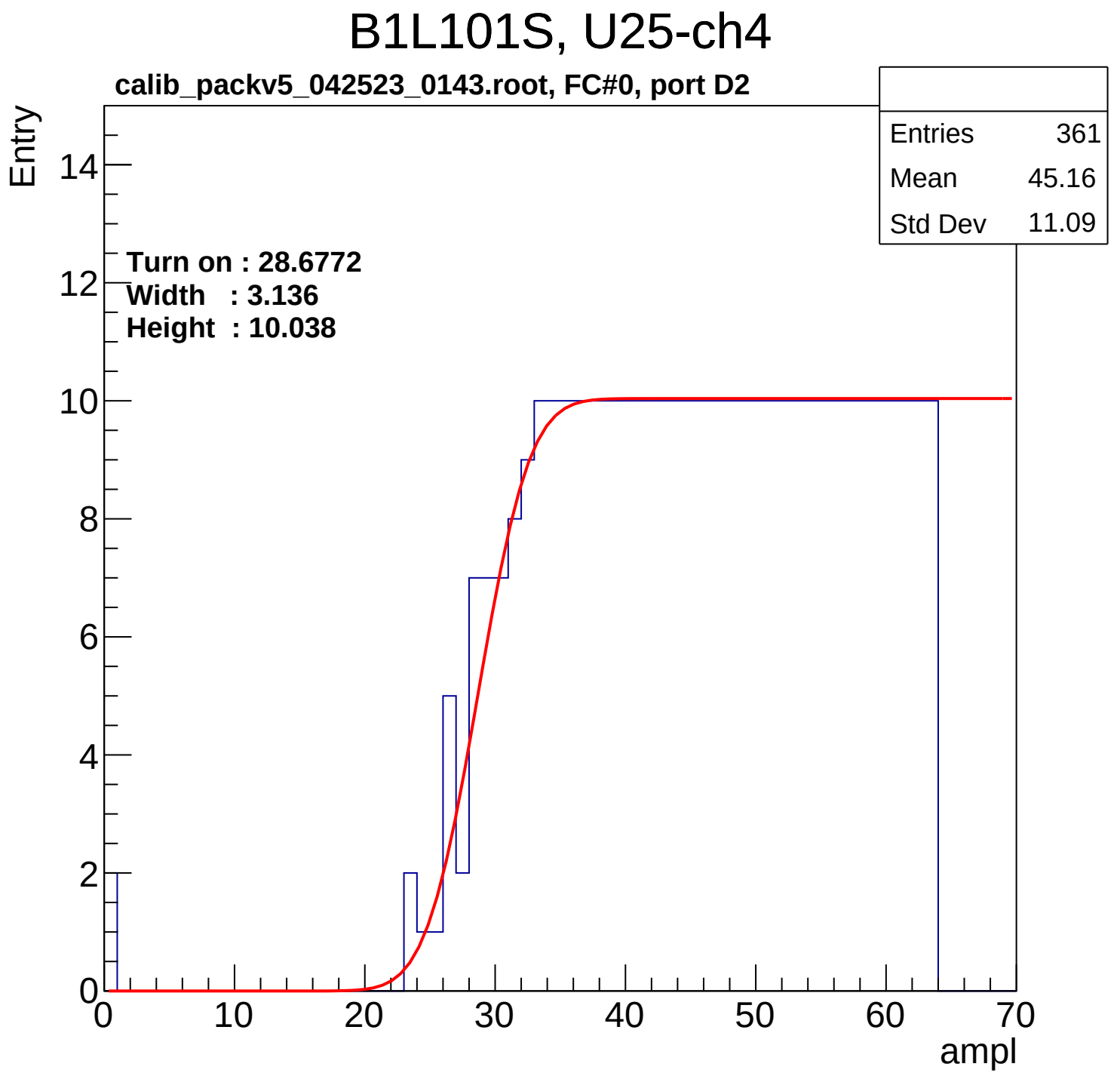
B1L101S, U25-ch4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 361
Mean 45.16
Std Dev 11.09
Turn on : 28.6772
Width : 3.136
Height : 10.038
Entry
ampl
0
2
4
6
8
10
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0
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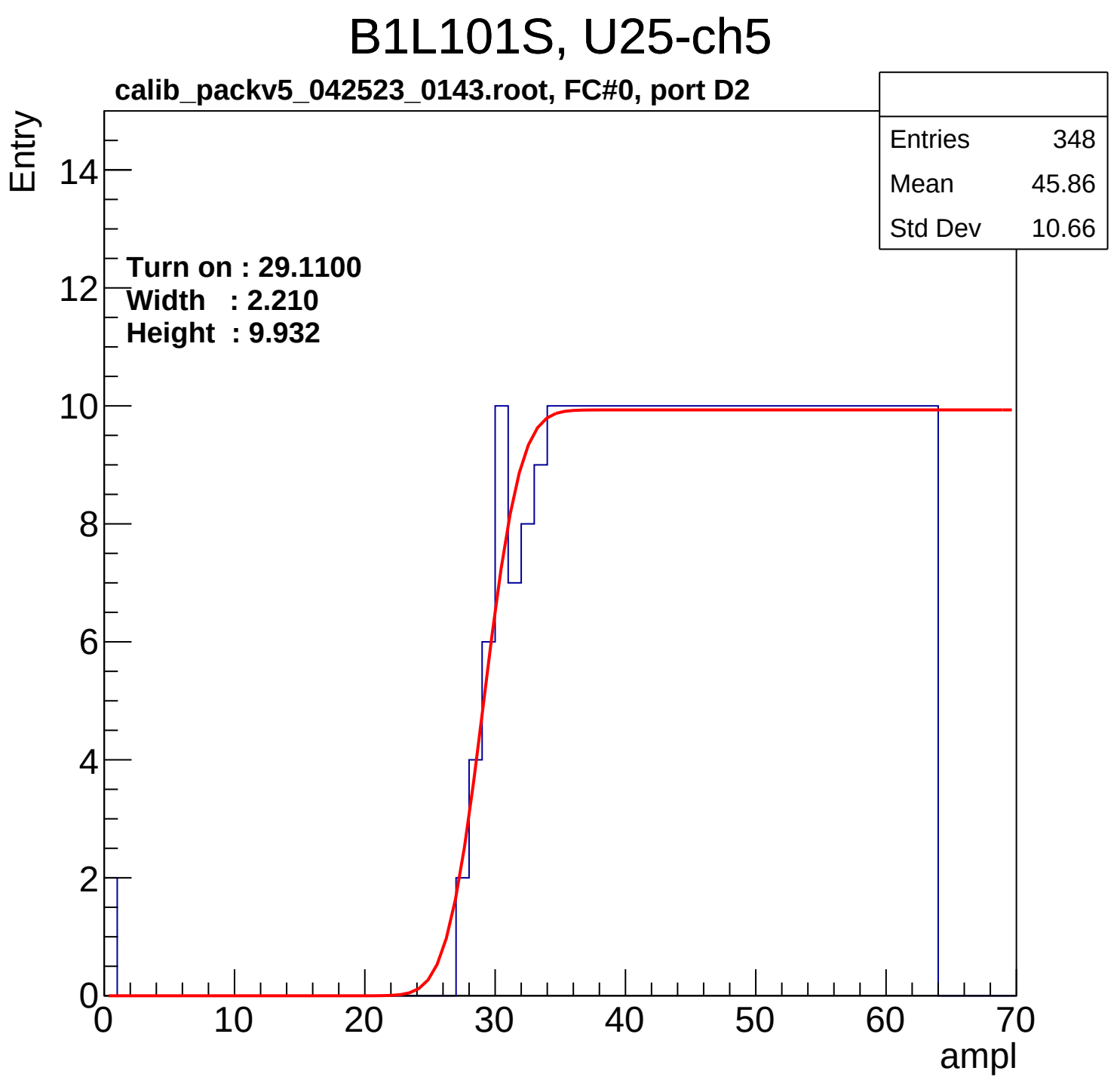
B1L101S, U25-ch5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 348
Mean 45.86
Std Dev 10.66
Turn on : 29.1100
Width : 2.210
Height : 9.932
Entry
ampl
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2
4
6
8
10
12
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0
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60
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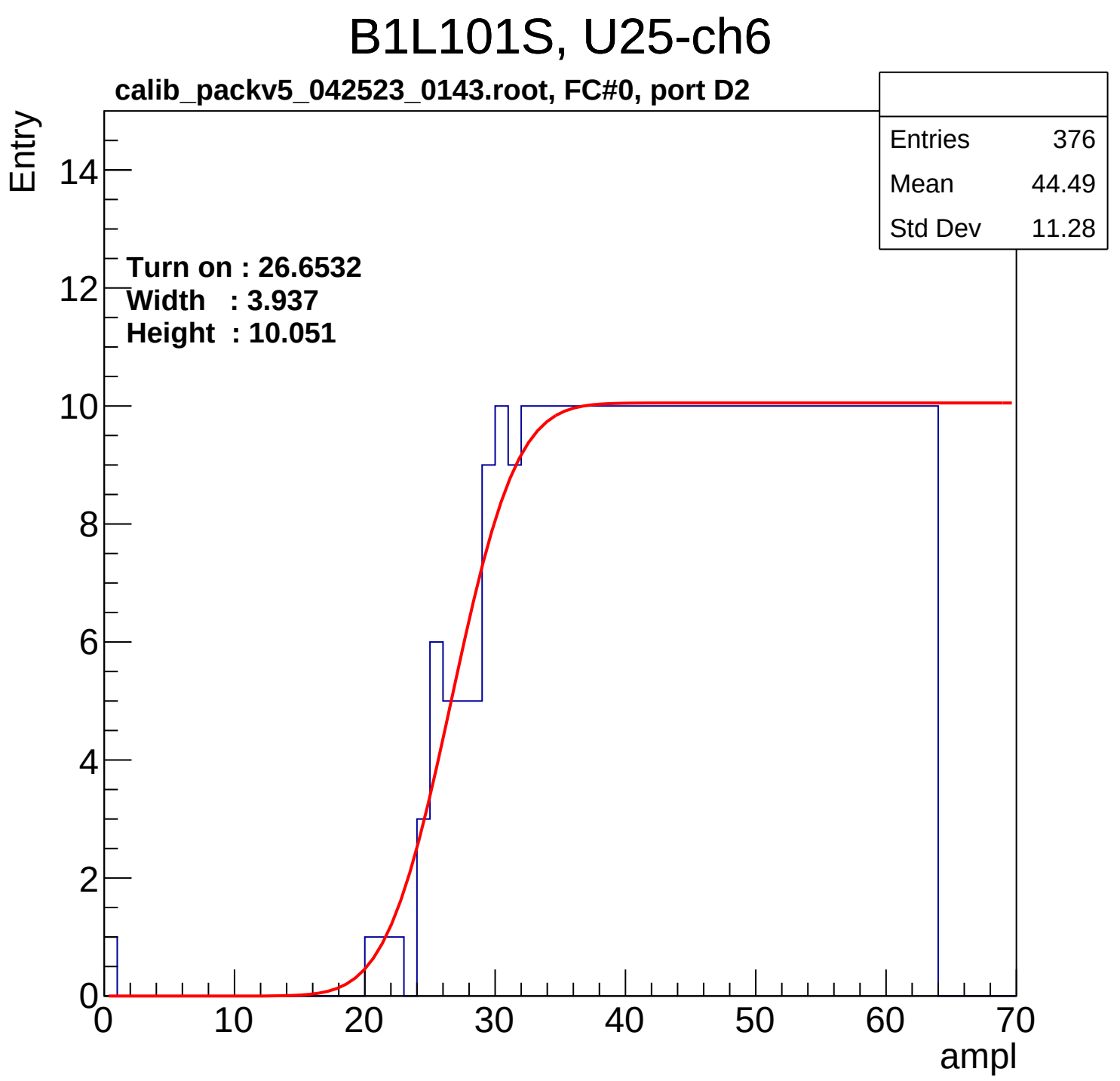
B1L101S, U25-ch6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 376
Mean 44.49
Std Dev 11.28
Turn on : 26.6532
Width : 3.937
Height : 10.051
Entry
ampl
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2
4
6
8
10
12
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0
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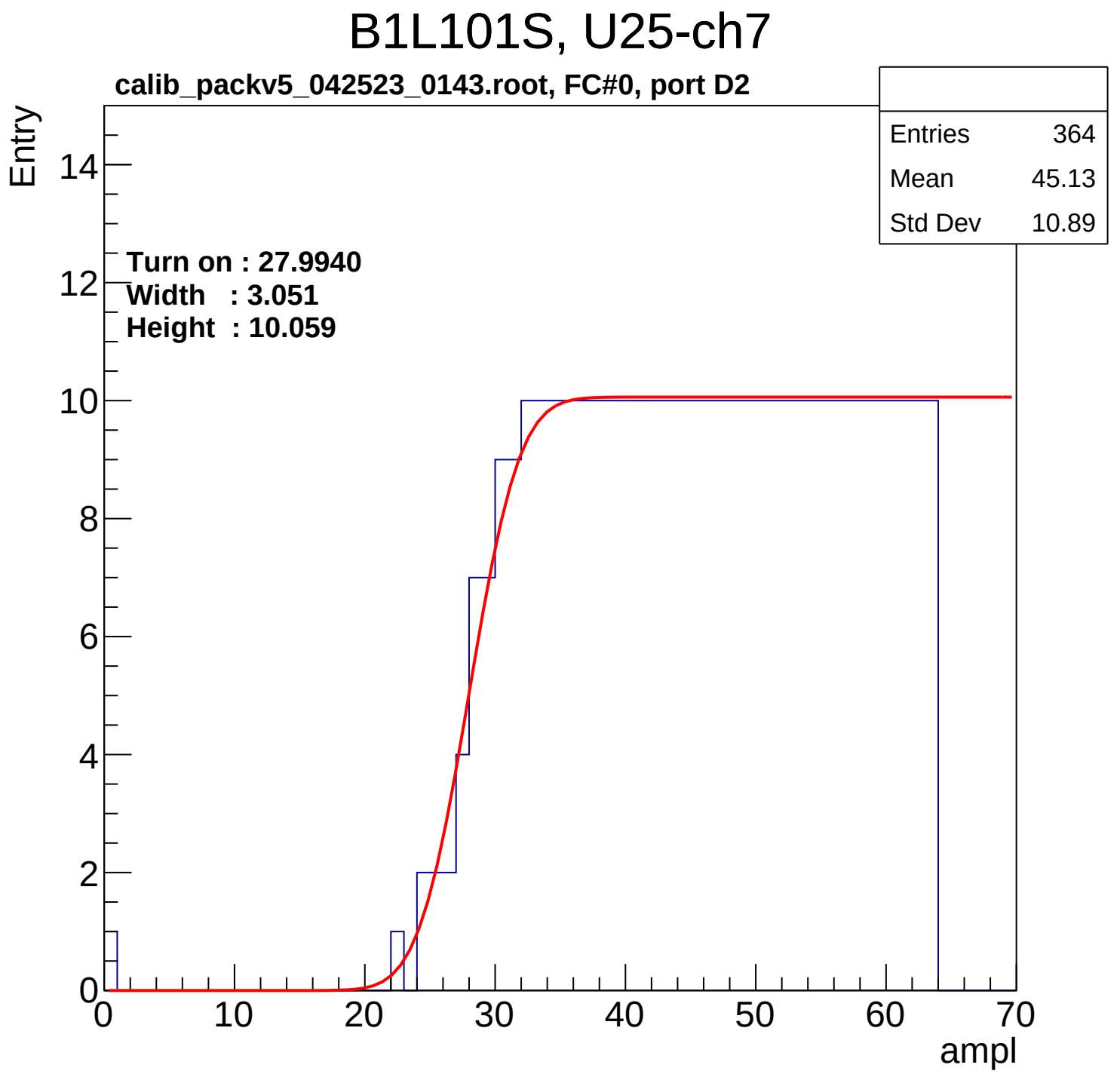
B1L101S, U25-ch7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 364
Mean 45.13
Std Dev 10.89
Turn on : 27.9940
Width : 3.051
Height : 10.059
Entry
ampl
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2
4
6
8
10
12
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0
10
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60
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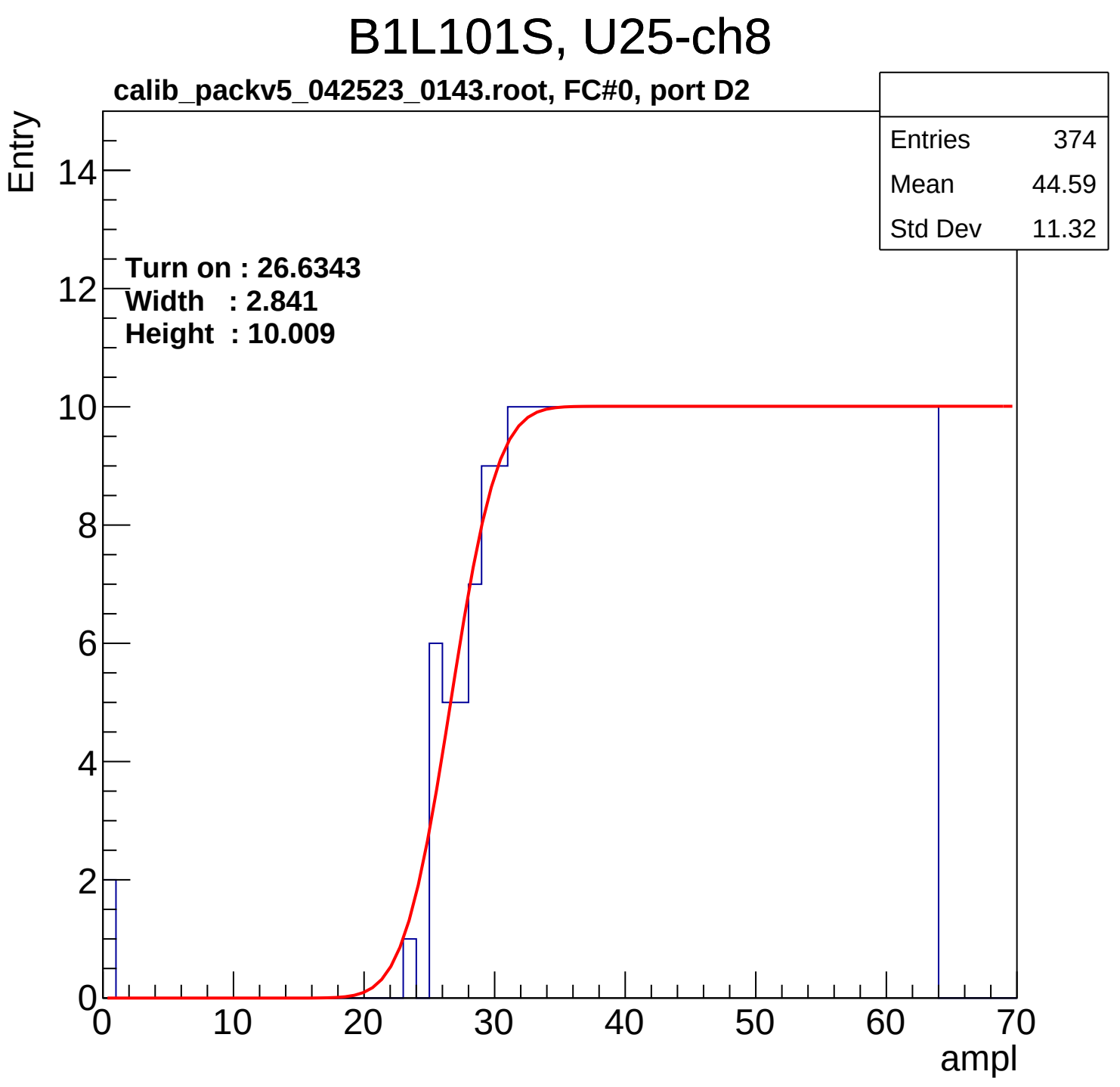
B1L101S, U25-ch8
calib_packv5_042523_0143.root, FC#0, port D2
Entries 374
Mean 44.59
Std Dev 11.32
Turn on : 26.6343
Width : 2.841
Height : 10.009
Entry
ampl
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4
6
8
10
12
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0
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20
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60
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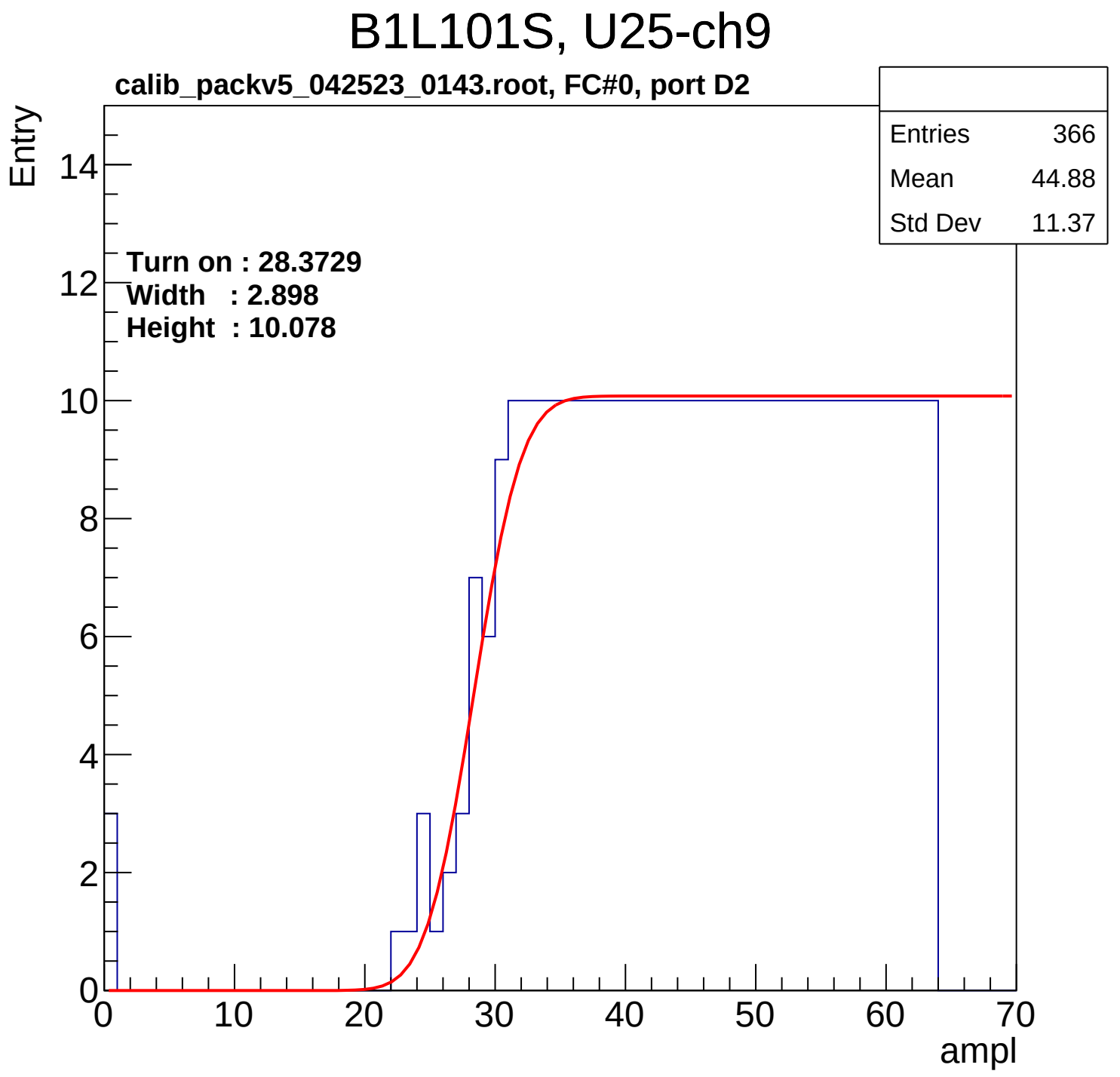
B1L101S, U25-ch9
calib_packv5_042523_0143.root, FC#0, port D2
Entries 366
Mean 44.88
Std Dev 11.37
Turn on : 28.3729
Width : 2.898
Height : 10.078
Entry
ampl
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2
4
6
8
10
12
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0
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20
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60
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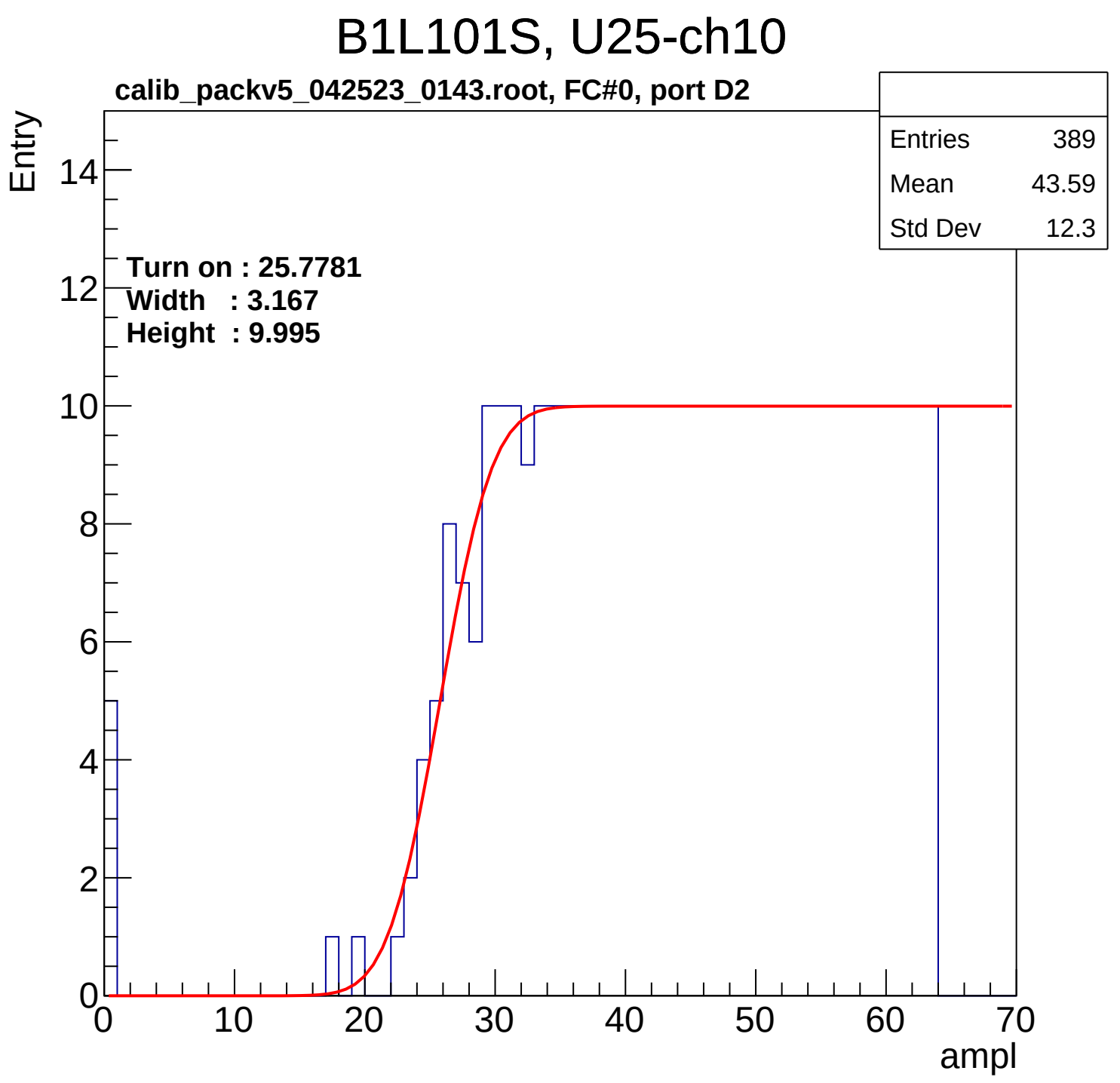
B1L101S, U25-ch10
calib_packv5_042523_0143.root, FC#0, port D2
Entries 389
Mean 43.59
Std Dev 12.3
Turn on : 25.7781
Width : 3.167
Height : 9.995
Entry
ampl
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2
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6
8
10
12
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0
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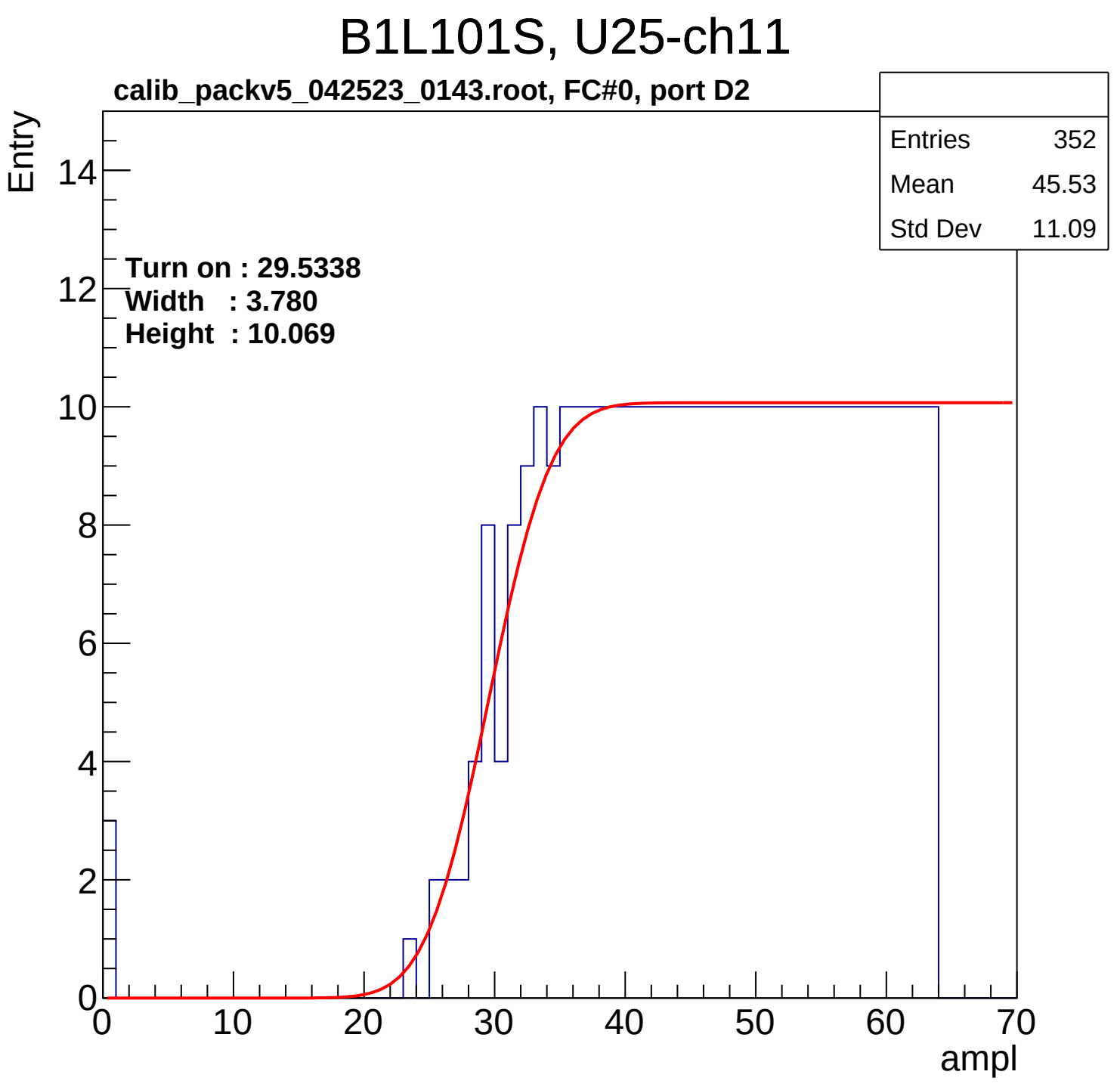
B1L101S, U25-ch11
calib_packv5_042523_0143.root, FC#0, port D2
Entries 352
Mean 45.53
Std Dev 11.09
Turn on : 29.5338
Width : 3.780
Height : 10.069
Entry
ampl
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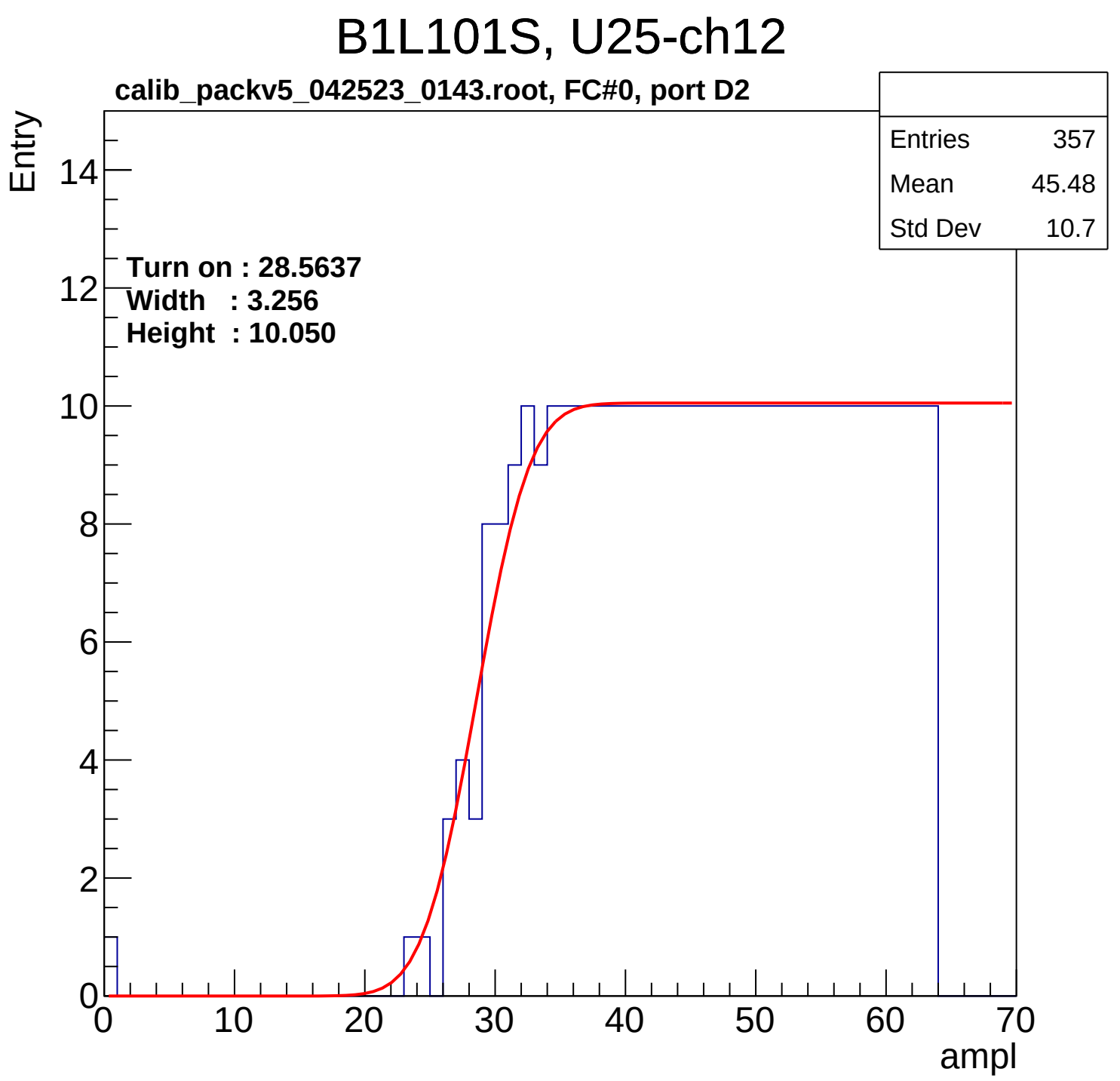
B1L101S, U25-ch12
calib_packv5_042523_0143.root, FC#0, port D2
Entries 357
Mean 45.48
Std Dev 10.7
Turn on : 28.5637
Width : 3.256
Height : 10.050
Entry
ampl
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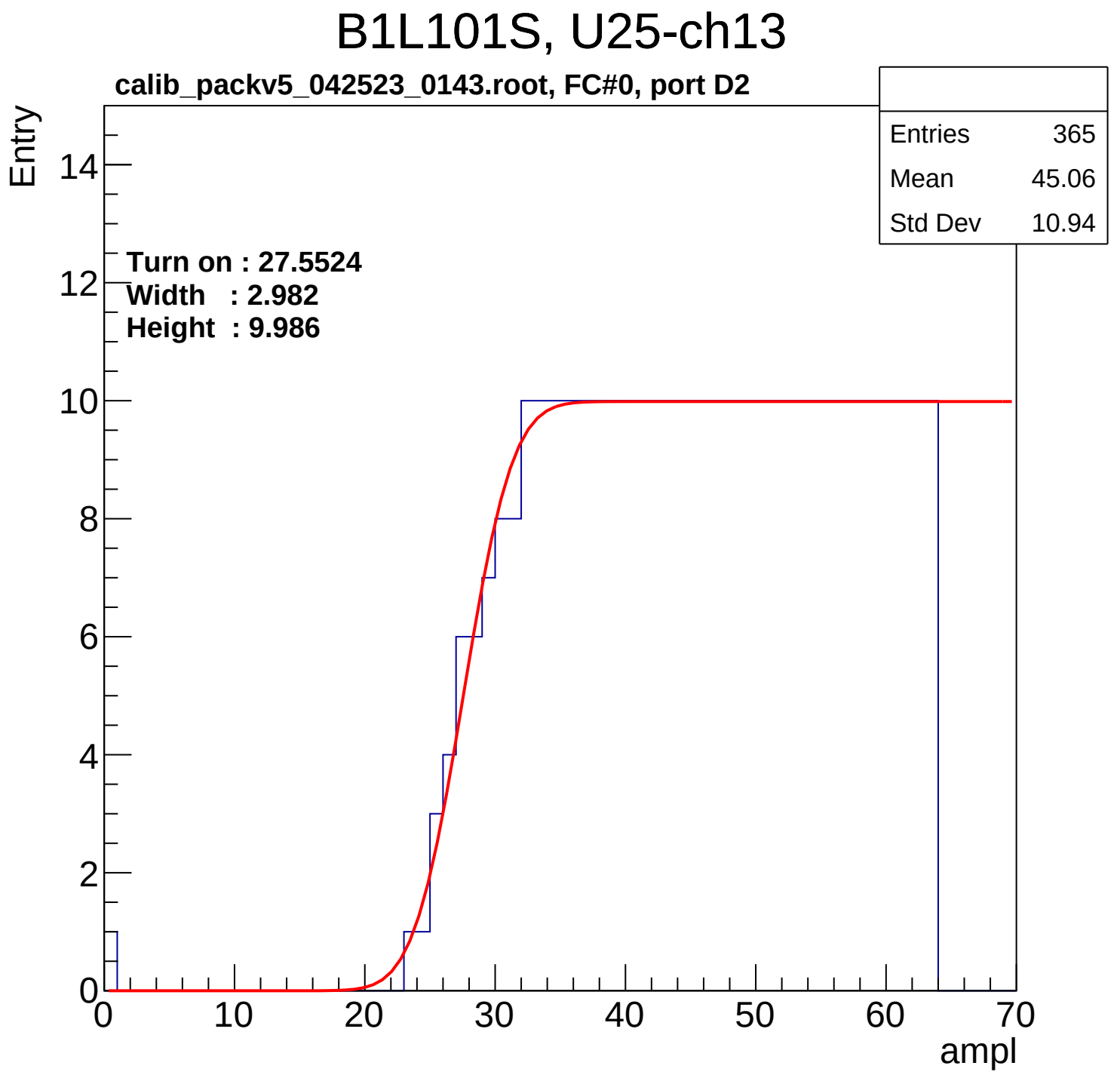
B1L101S, U25-ch13
calib_packv5_042523_0143.root, FC#0, port D2
Entries 365
Mean 45.06
Std Dev 10.94
Turn on : 27.5524
Width : 2.982
Height : 9.986
Entry
ampl
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6
8
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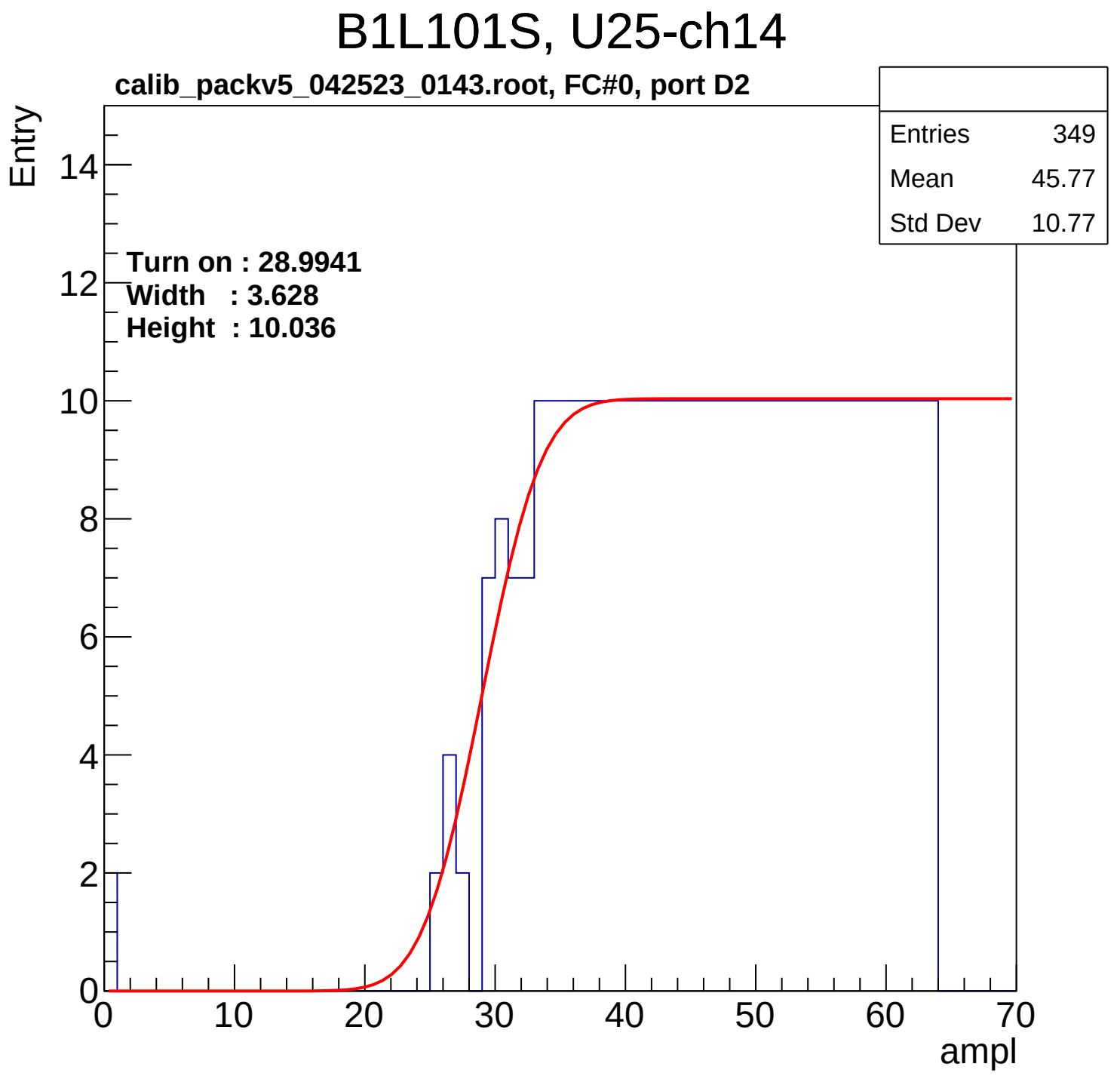
B1L101S, U25-ch14
calib_packv5_042523_0143.root, FC#0, port D2
Entries 349
Mean 45.77
Std Dev 10.77
Turn on : 28.9941
Width : 3.628
Height : 10.036
Entry
ampl
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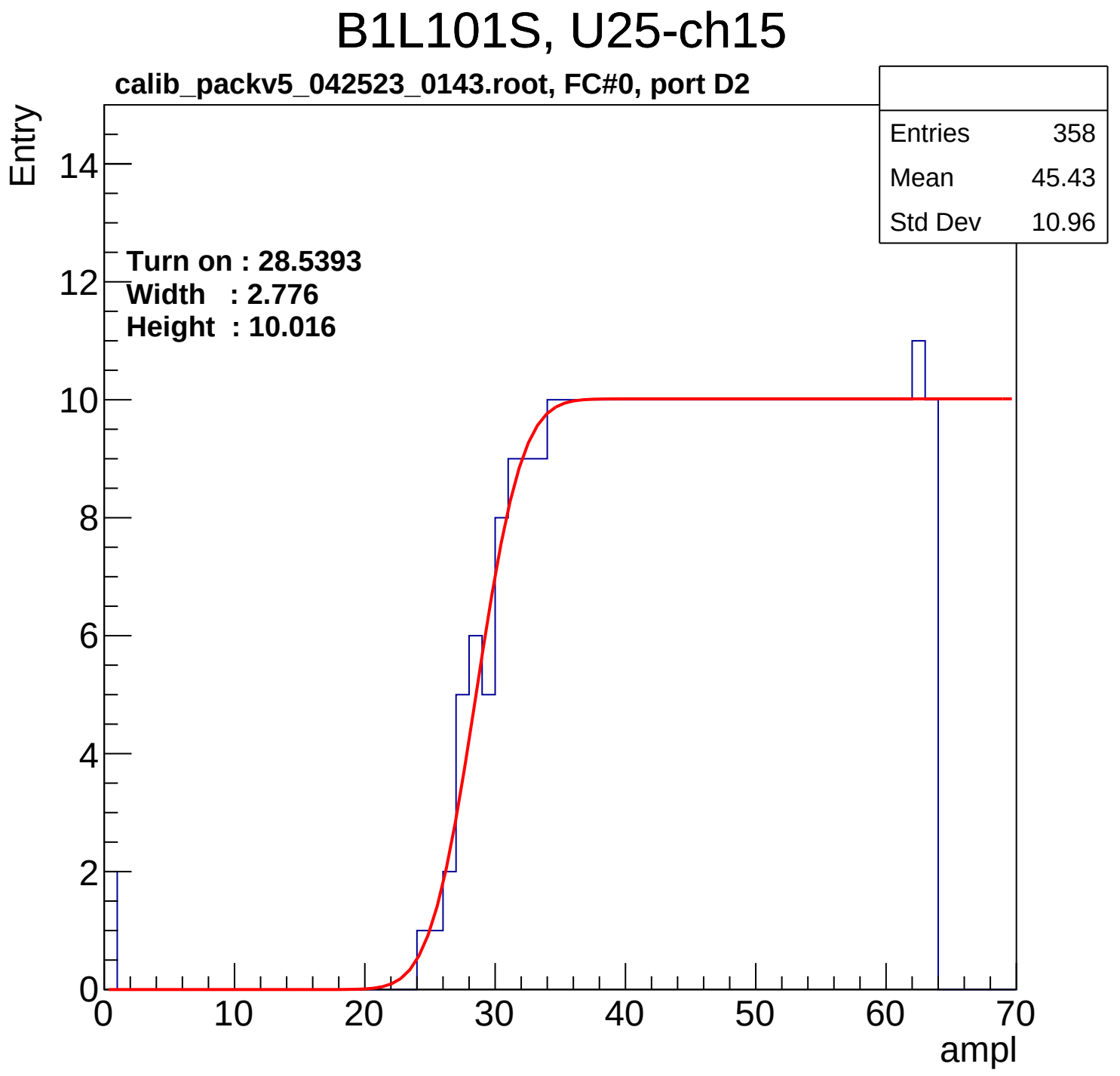
B1L101S, U25-ch15
calib_packv5_042523_0143.root, FC#0, port D2
Entries 358
Mean 45.43
Std Dev 10.96
Turn on : 28.5393
Width : 2.776
Height : 10.016
Entry
ampl
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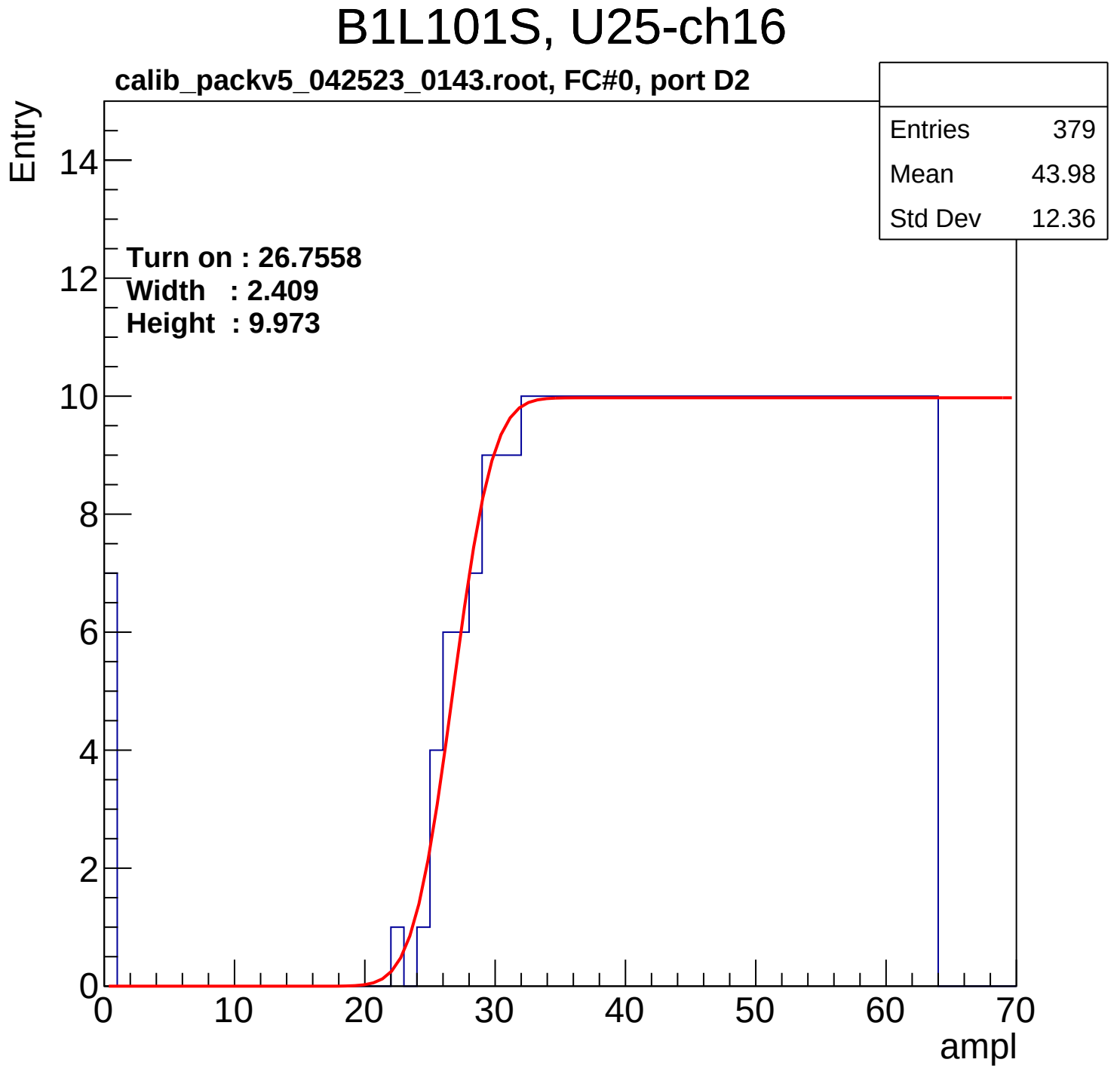
B1L101S, U25-ch16
calib_packv5_042523_0143.root, FC#0, port D2
Entries 379
Mean 43.98
Std Dev 12.36
Turn on : 26.7558
Width : 2.409
Height : 9.973
Entry
ampl
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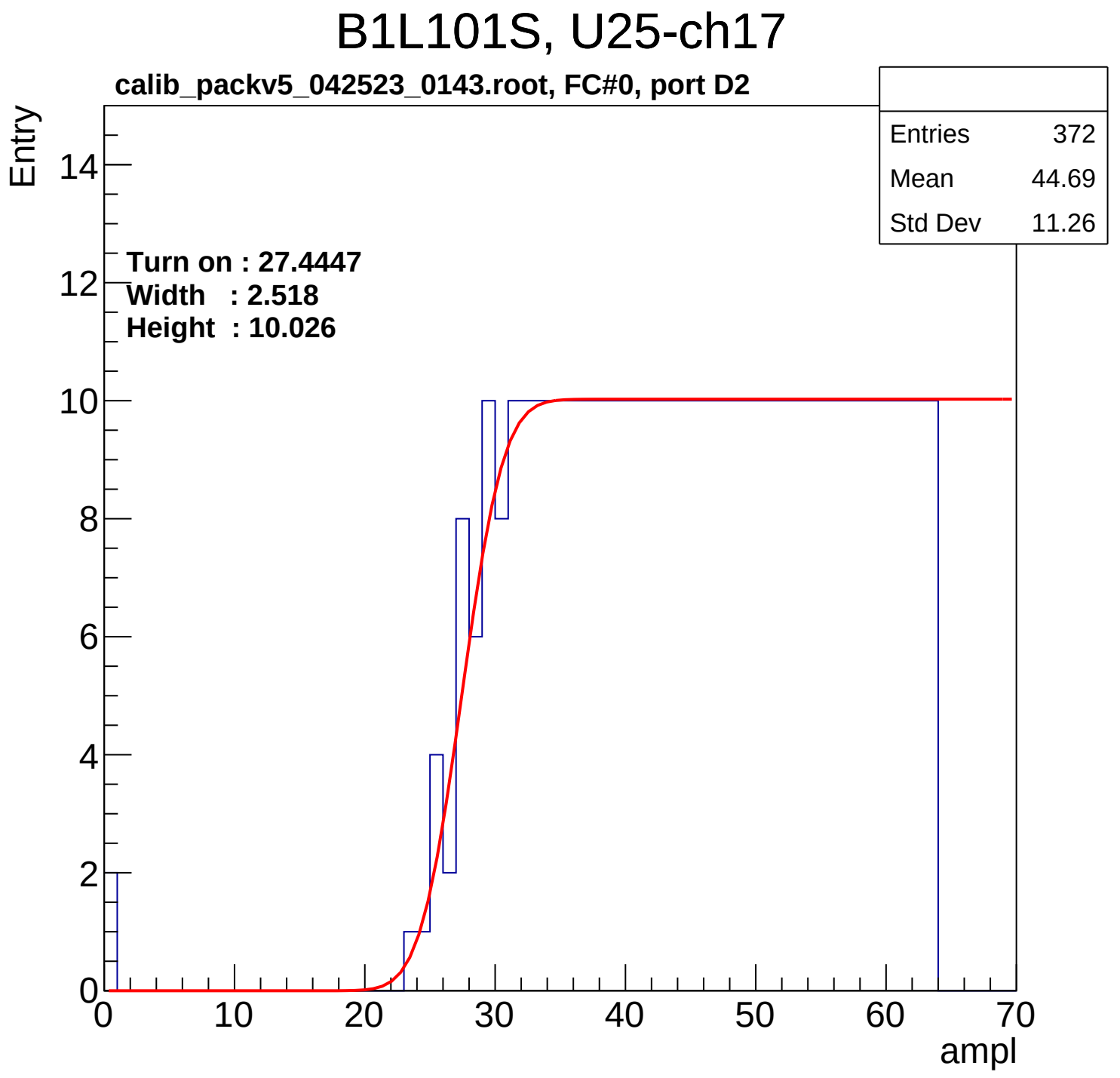
B1L101S, U25-ch17
calib_packv5_042523_0143.root, FC#0, port D2
Entries 372
Mean 44.69
Std Dev 11.26
Turn on : 27.4447
Width : 2.518
Height : 10.026
Entry
ampl
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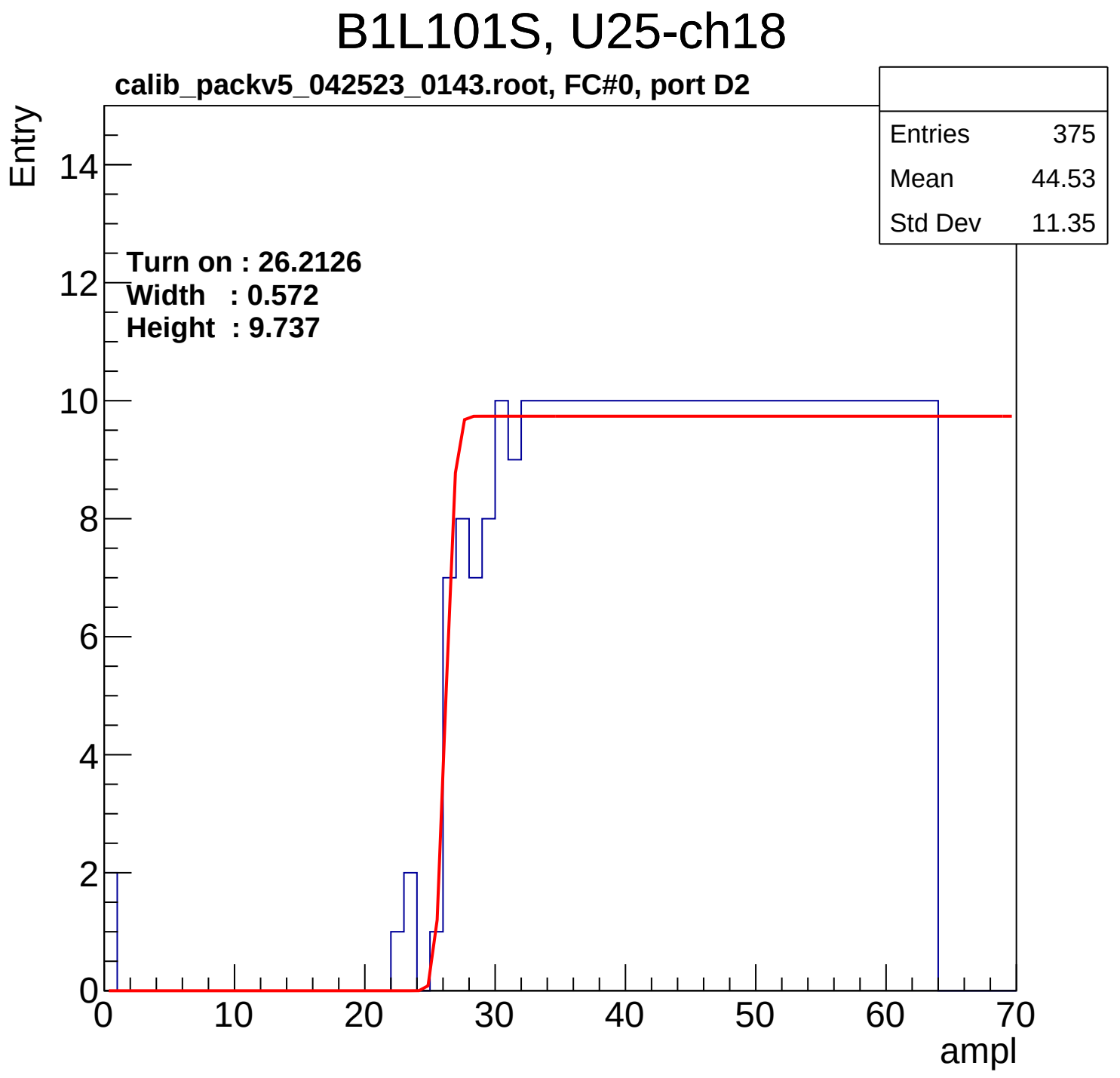
B1L101S, U25-ch18
calib_packv5_042523_0143.root, FC#0, port D2
Entries 375
Mean 44.53
Std Dev 11.35
Turn on : 26.2126
Width : 0.572
Height : 9.737
Entry
ampl
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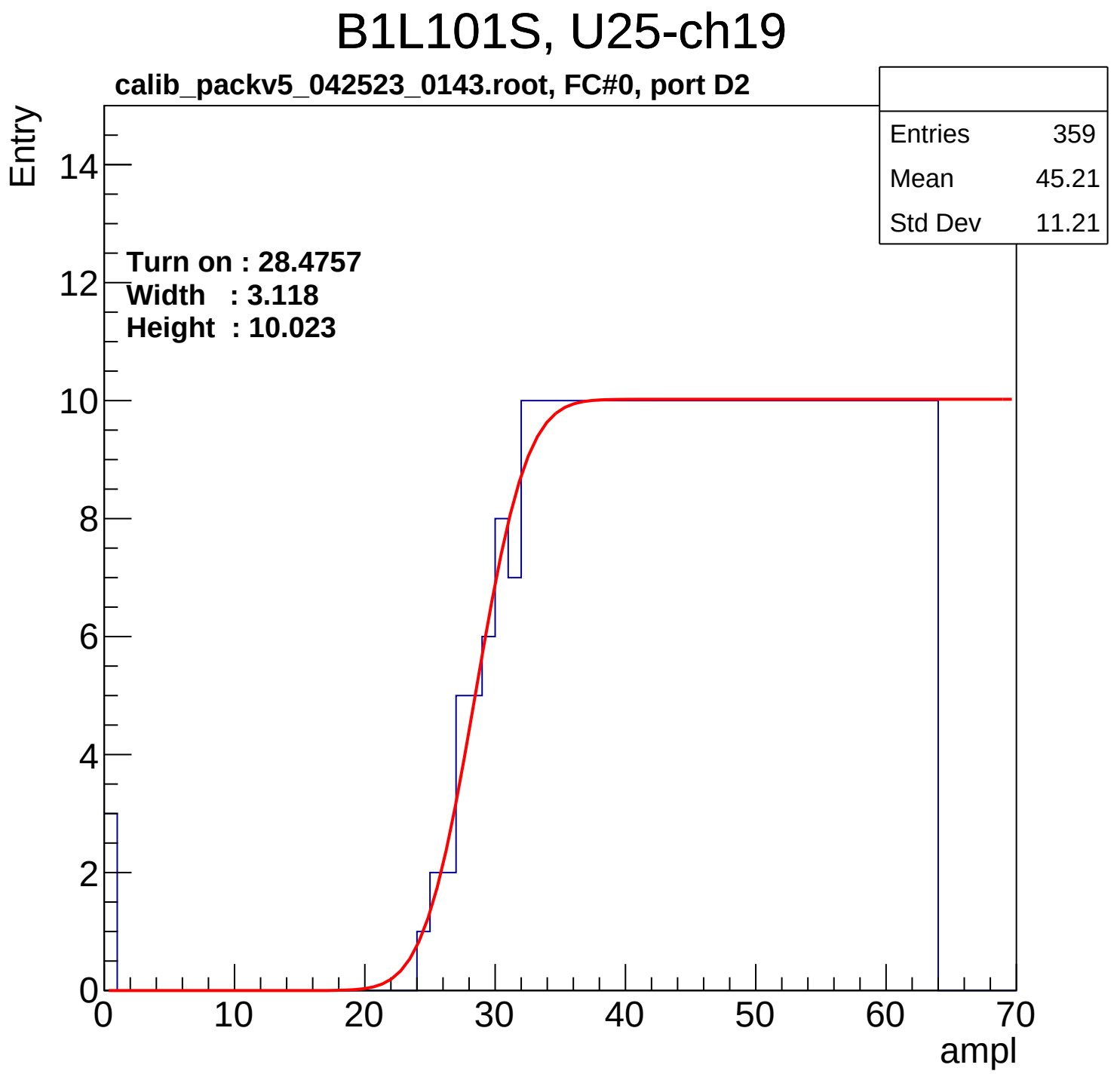
B1L101S, U25-ch19
calib_packv5_042523_0143.root, FC#0, port D2
Entries 359
Mean 45.21
Std Dev 11.21
Turn on : 28.4757
Width : 3.118
Height : 10.023
Entry
ampl
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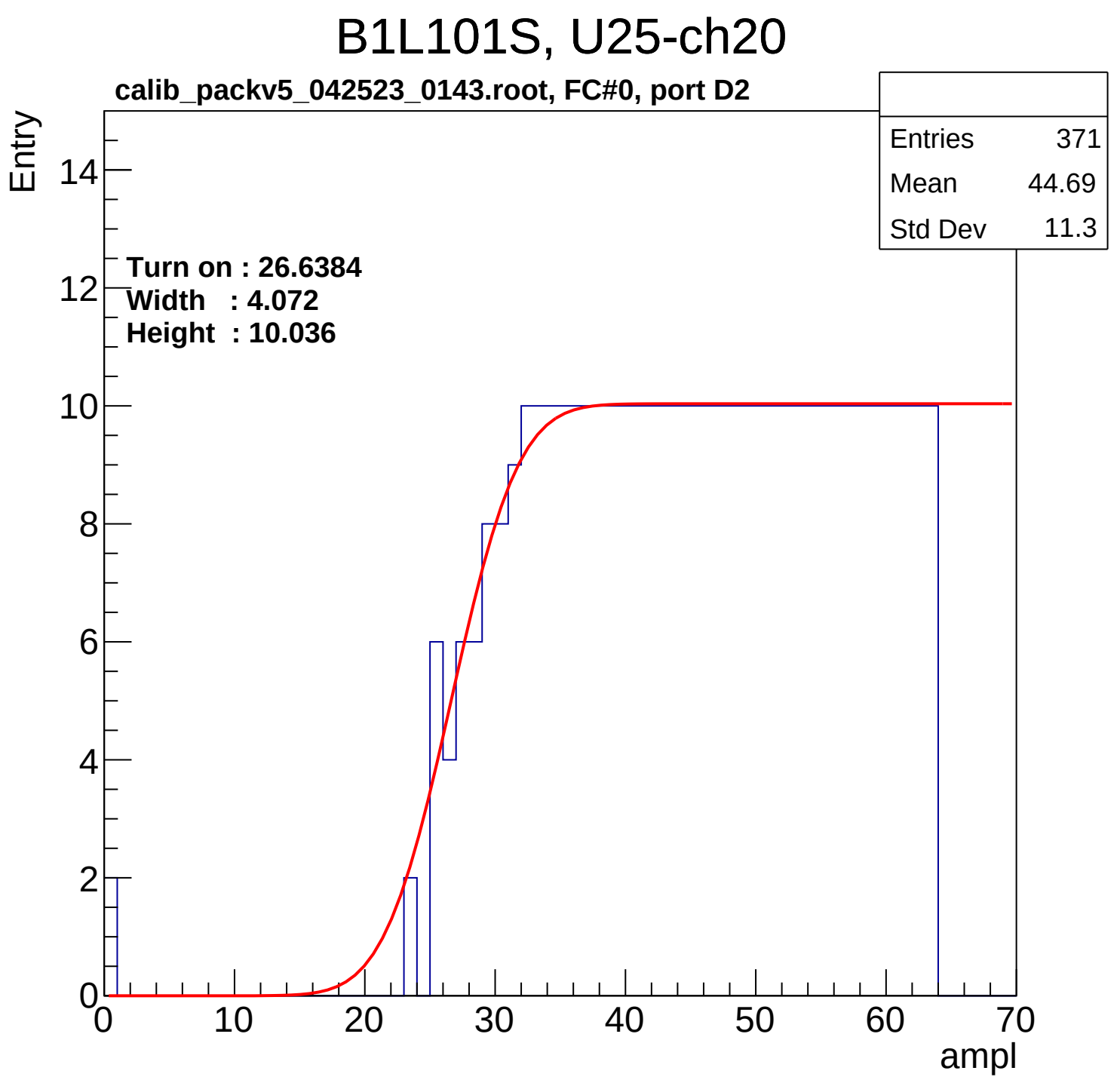
B1L101S, U25-ch20
calib_packv5_042523_0143.root, FC#0, port D2
Entries 371
Mean 44.69
Std Dev 11.3
Turn on : 26.6384
Width : 4.072
Height : 10.036
Entry
ampl
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8
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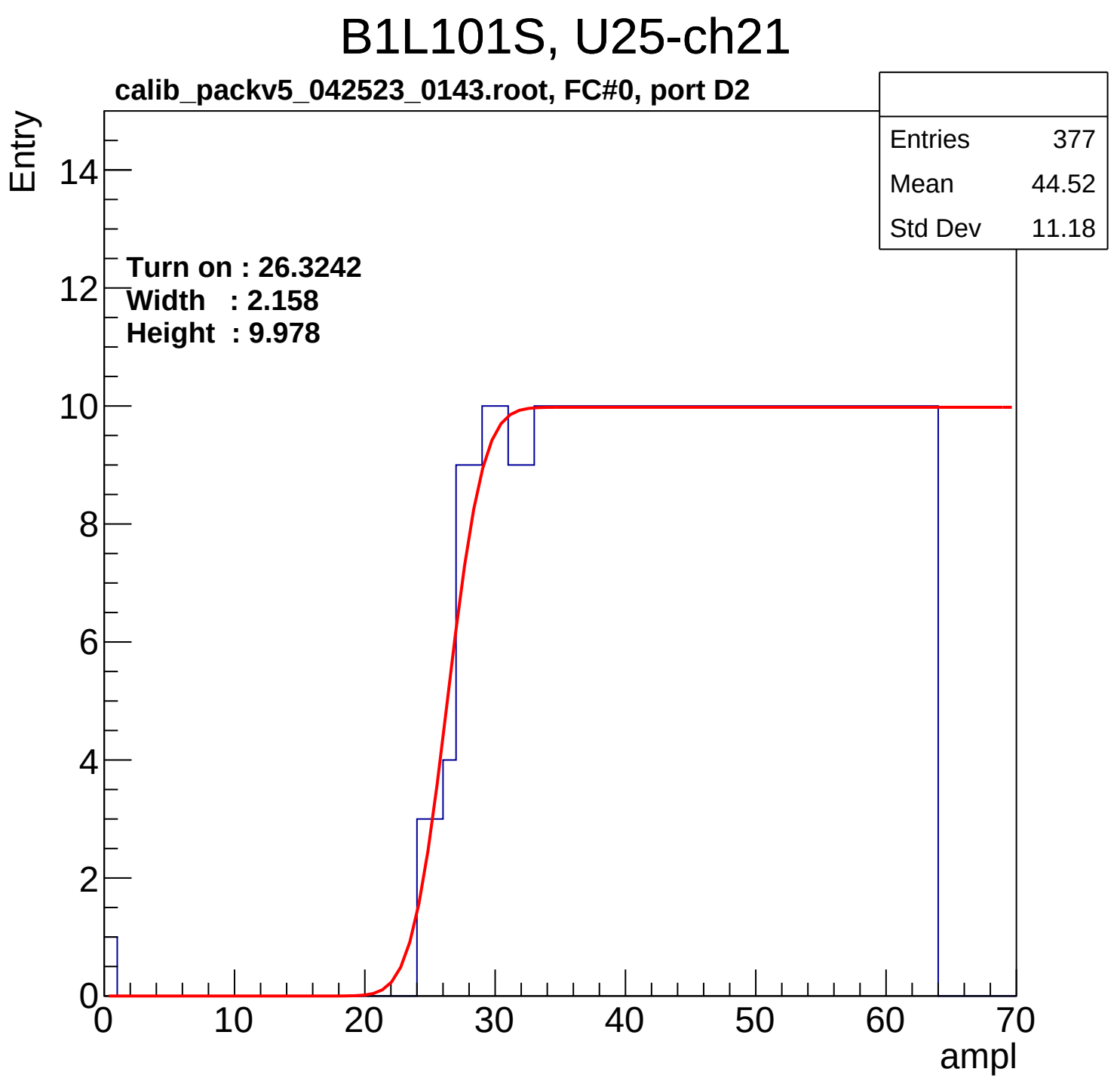
B1L101S, U25-ch21
calib_packv5_042523_0143.root, FC#0, port D2
Entries 377
Mean 44.52
Std Dev 11.18
Turn on : 26.3242
Width : 2.158
Height : 9.978
Entry
ampl
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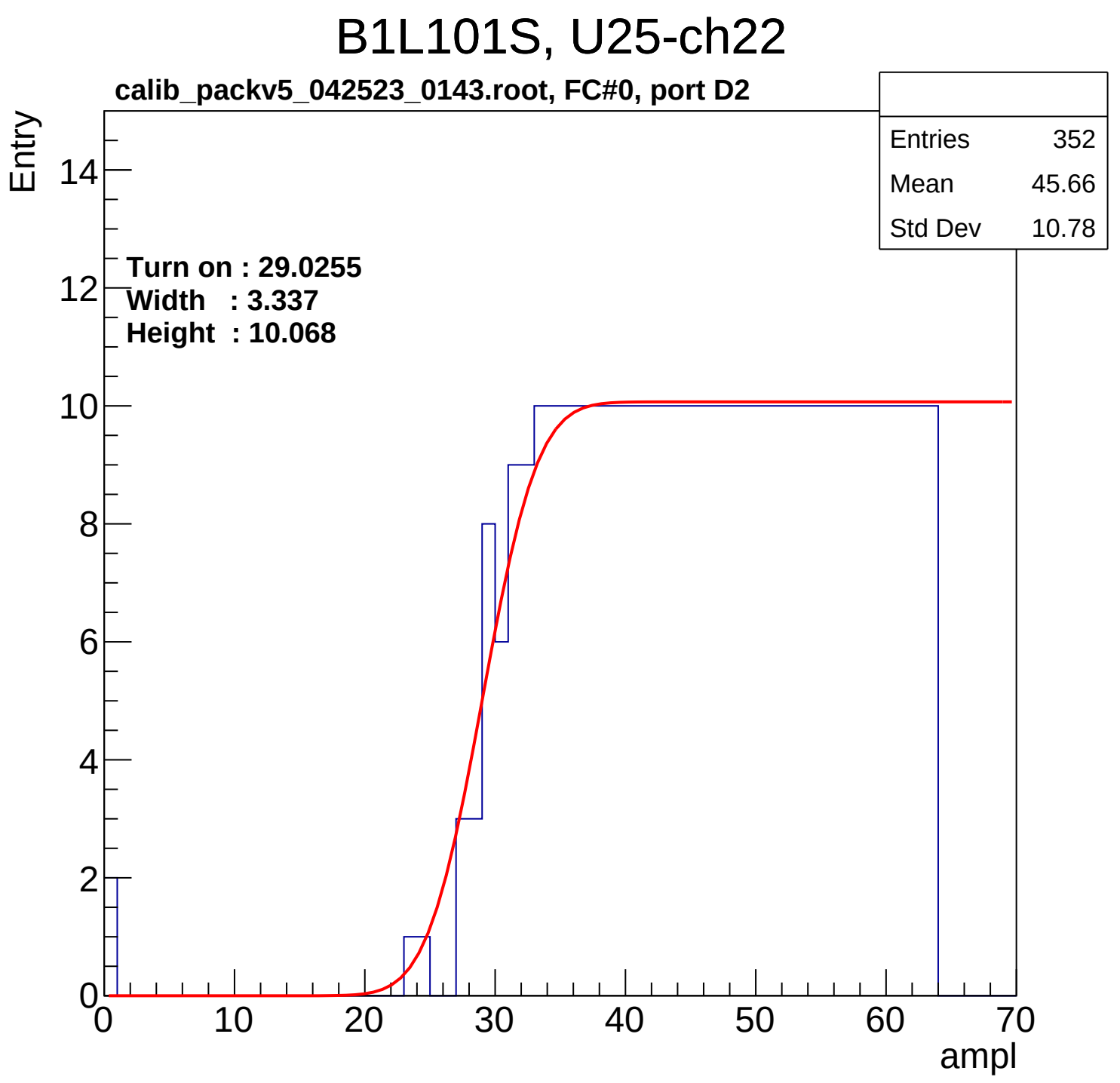
B1L101S, U25-ch22
calib_packv5_042523_0143.root, FC#0, port D2
Entries 352
Mean 45.66
Std Dev 10.78
Turn on : 29.0255
Width : 3.337
Height : 10.068
Entry
ampl
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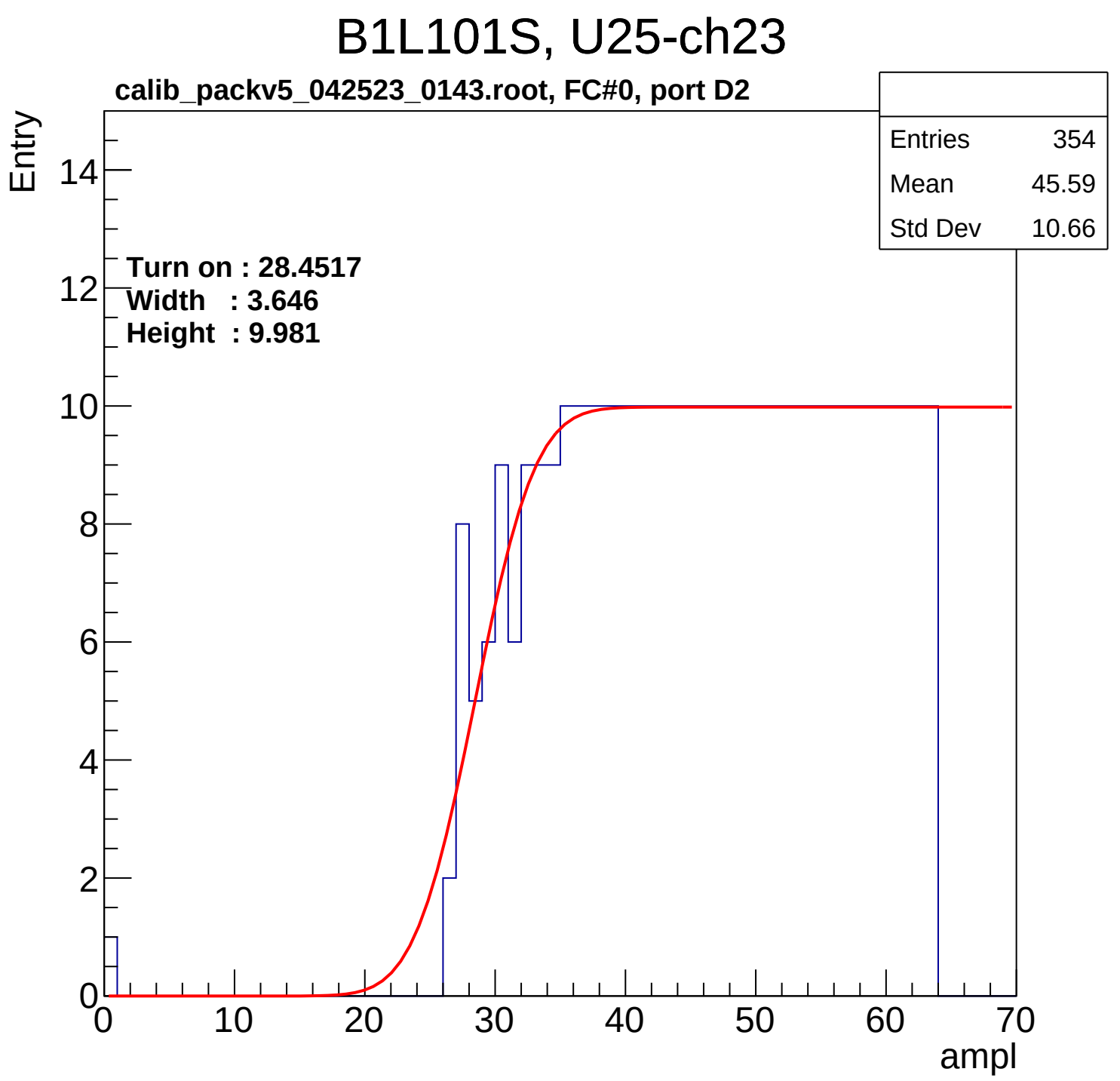
B1L101S, U25-ch23
calib_packv5_042523_0143.root, FC#0, port D2
Entries 354
Mean 45.59
Std Dev 10.66
Turn on : 28.4517
Width : 3.646
Height : 9.981
Entry
ampl
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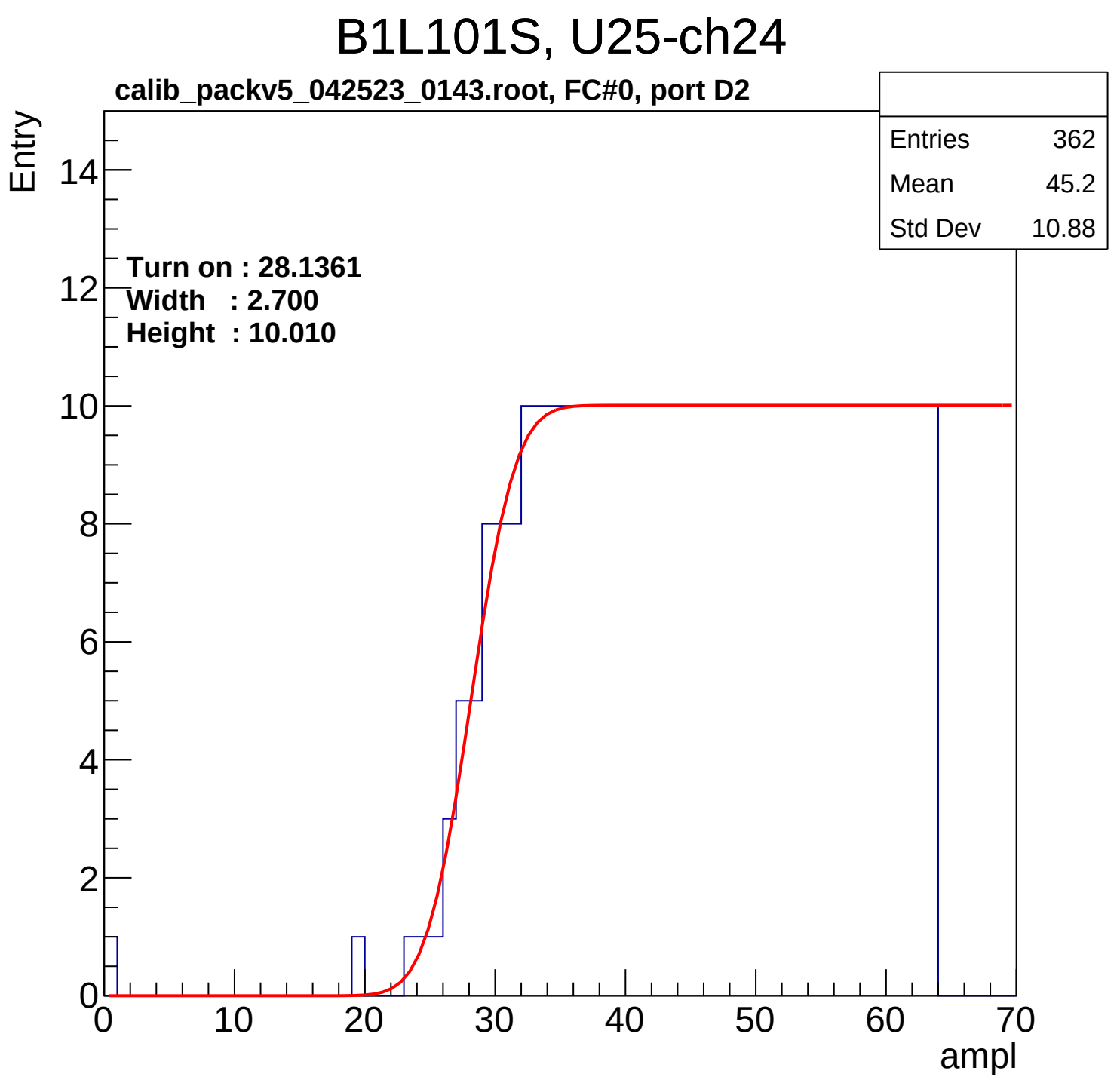
B1L101S, U25-ch24
calib_packv5_042523_0143.root, FC#0, port D2
Entries 362
Mean 45.2
Std Dev 10.88
Turn on : 28.1361
Width : 2.700
Height : 10.010
Entry
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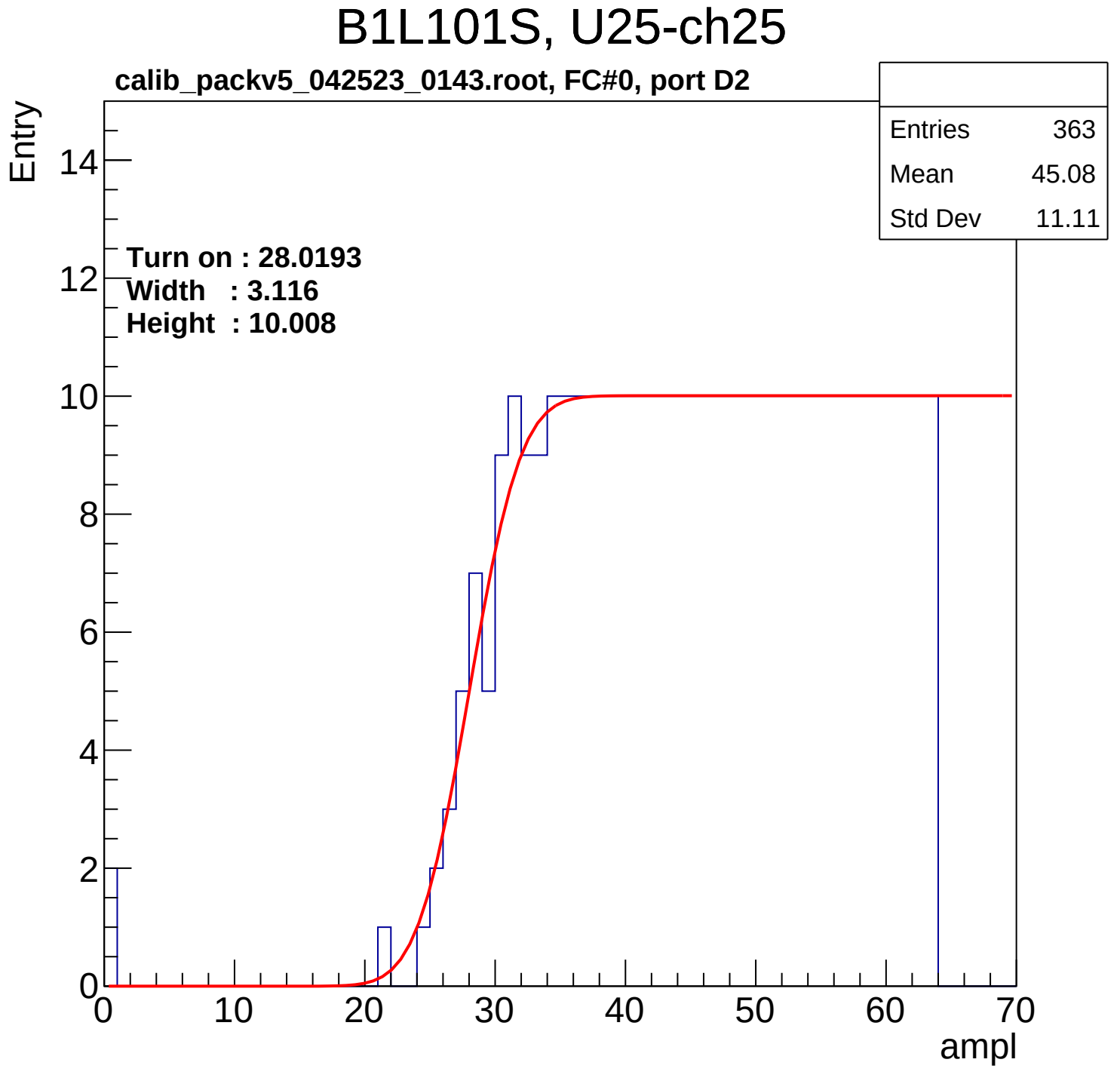
B1L101S, U25-ch25
calib_packv5_042523_0143.root, FC#0, port D2
Entries 363
Mean 45.08
Std Dev 11.11
Turn on : 28.0193
Width : 3.116
Height : 10.008
Entry
ampl
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8
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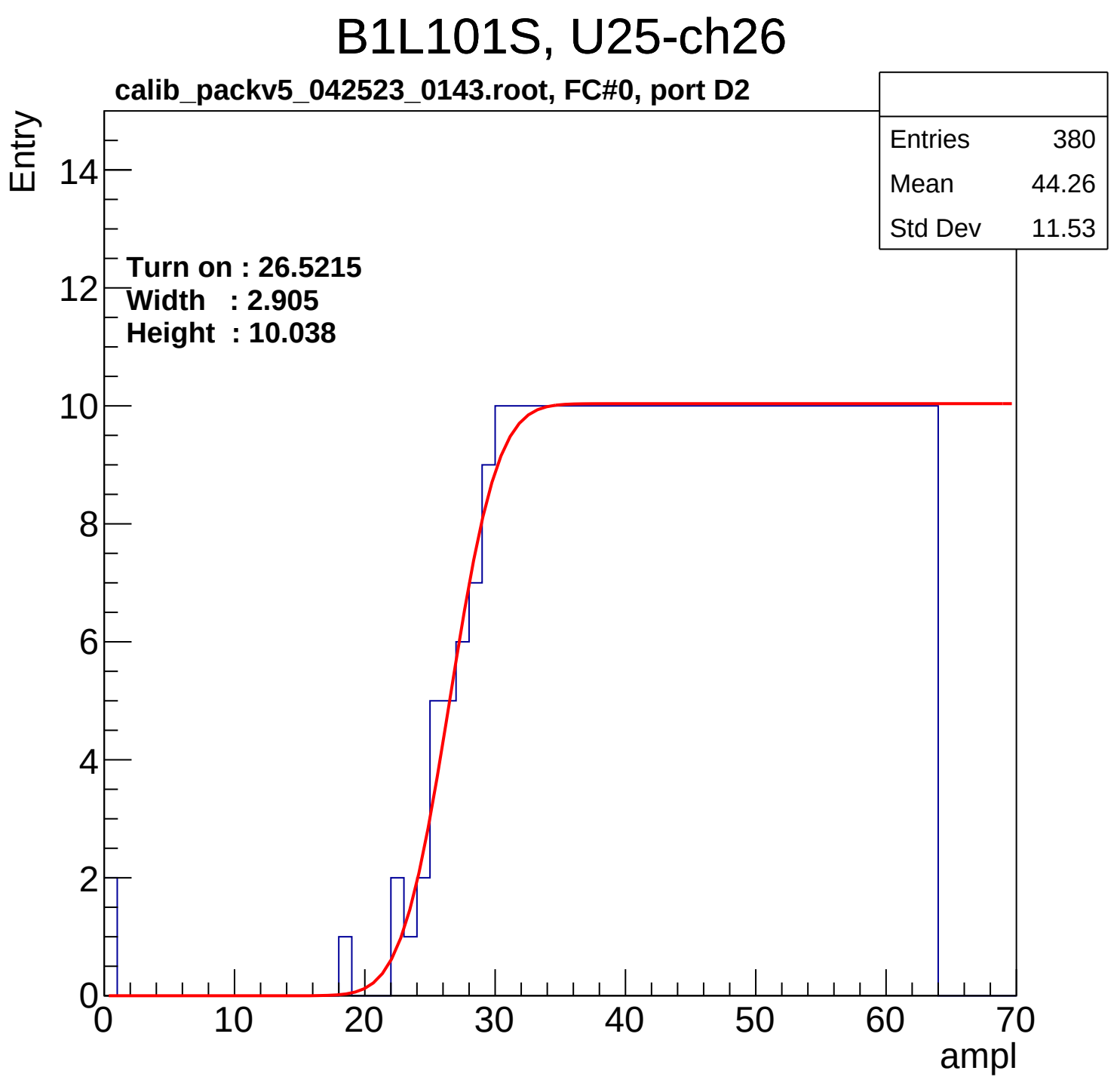
B1L101S, U25-ch26
calib_packv5_042523_0143.root, FC#0, port D2
Entries 380
Mean 44.26
Std Dev 11.53
Turn on : 26.5215
Width : 2.905
Height : 10.038
Entry
ampl
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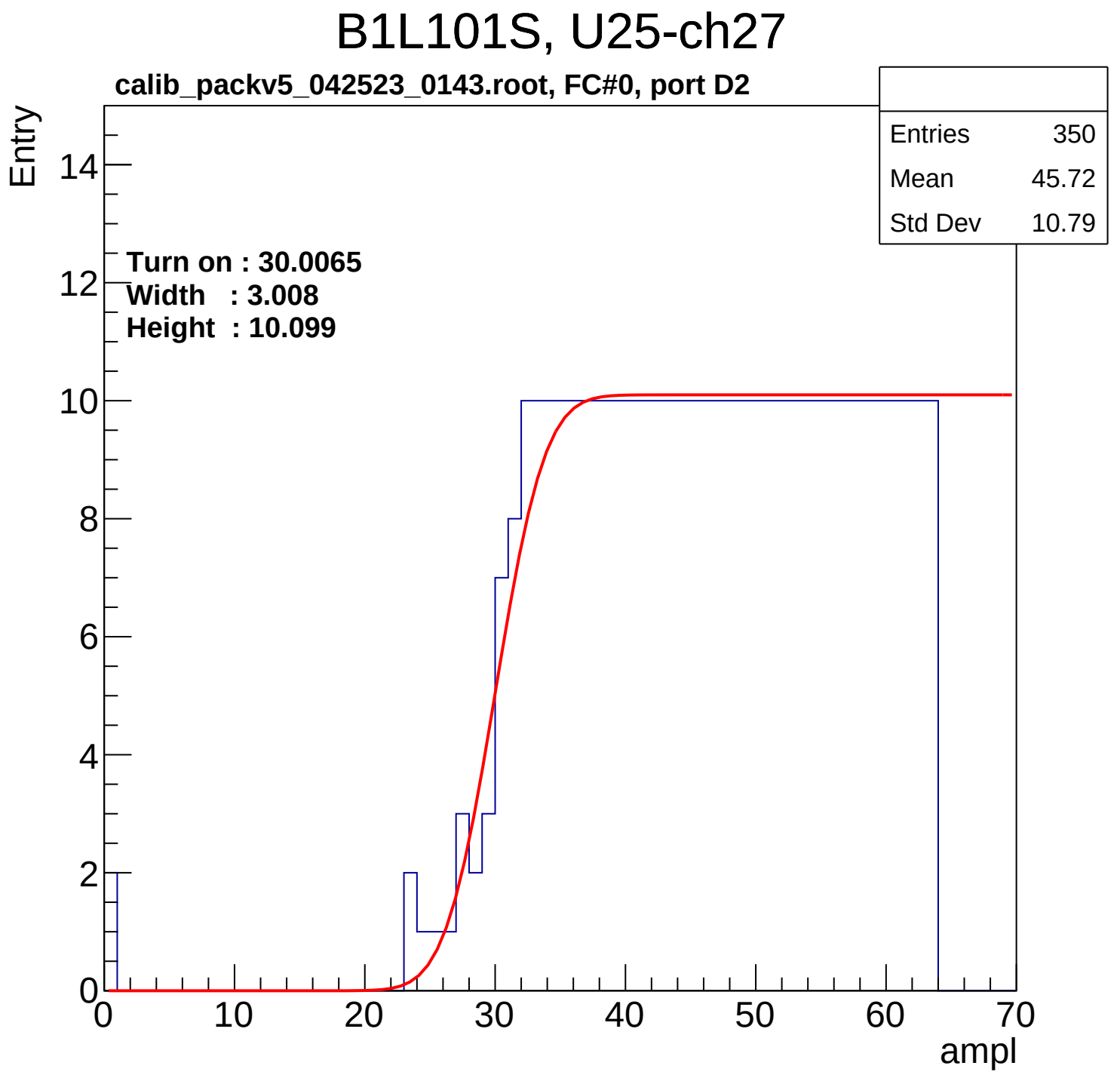
B1L101S, U25-ch27
calib_packv5_042523_0143.root, FC#0, port D2
Entries 350
Mean 45.72
Std Dev 10.79
Turn on : 30.0065
Width : 3.008
Height : 10.099
Entry
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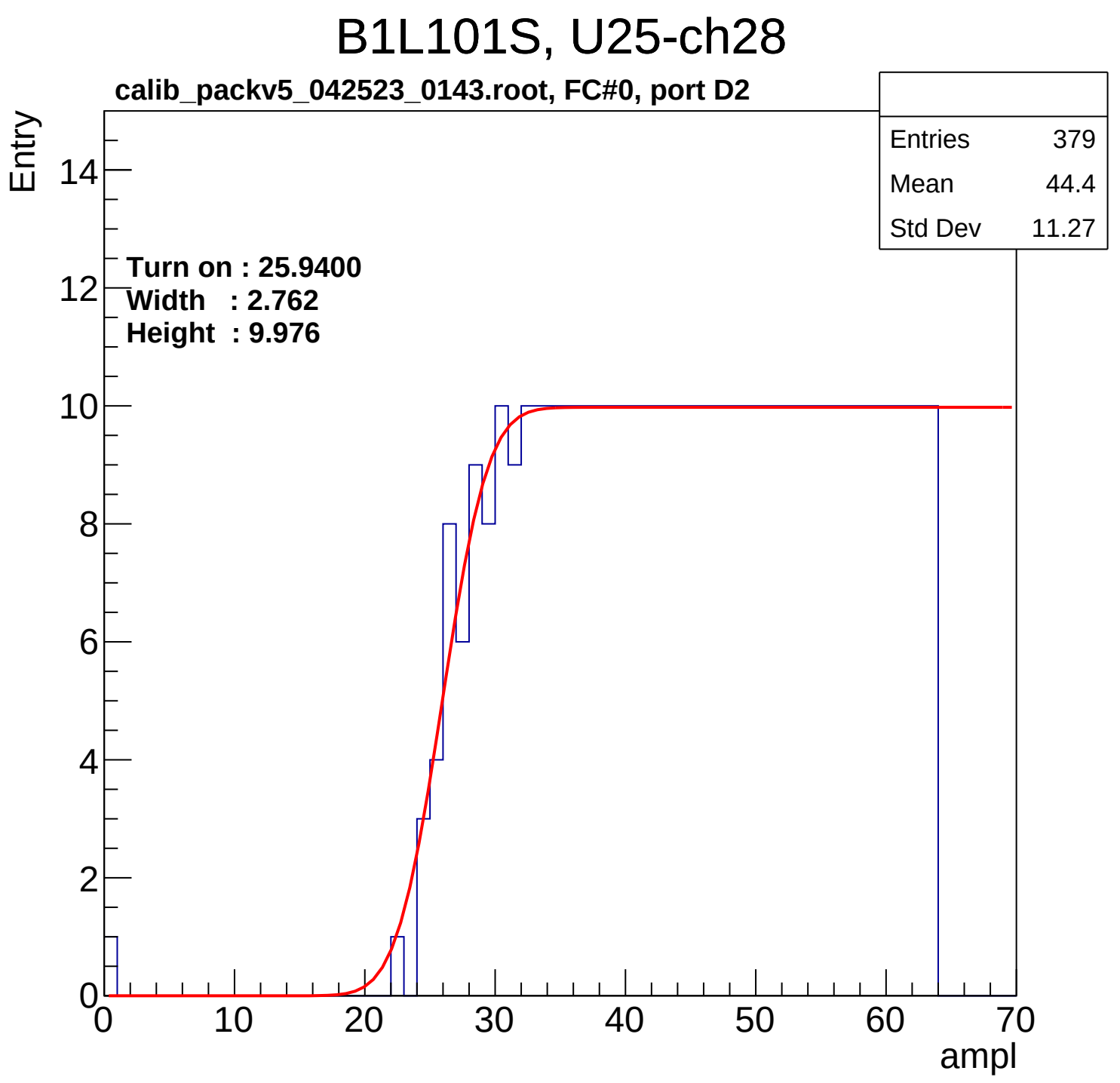
B1L101S, U25-ch28
calib_packv5_042523_0143.root, FC#0, port D2
Entries 379
Mean 44.4
Std Dev 11.27
Turn on : 25.9400
Width : 2.762
Height : 9.976
Entry
ampl
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6
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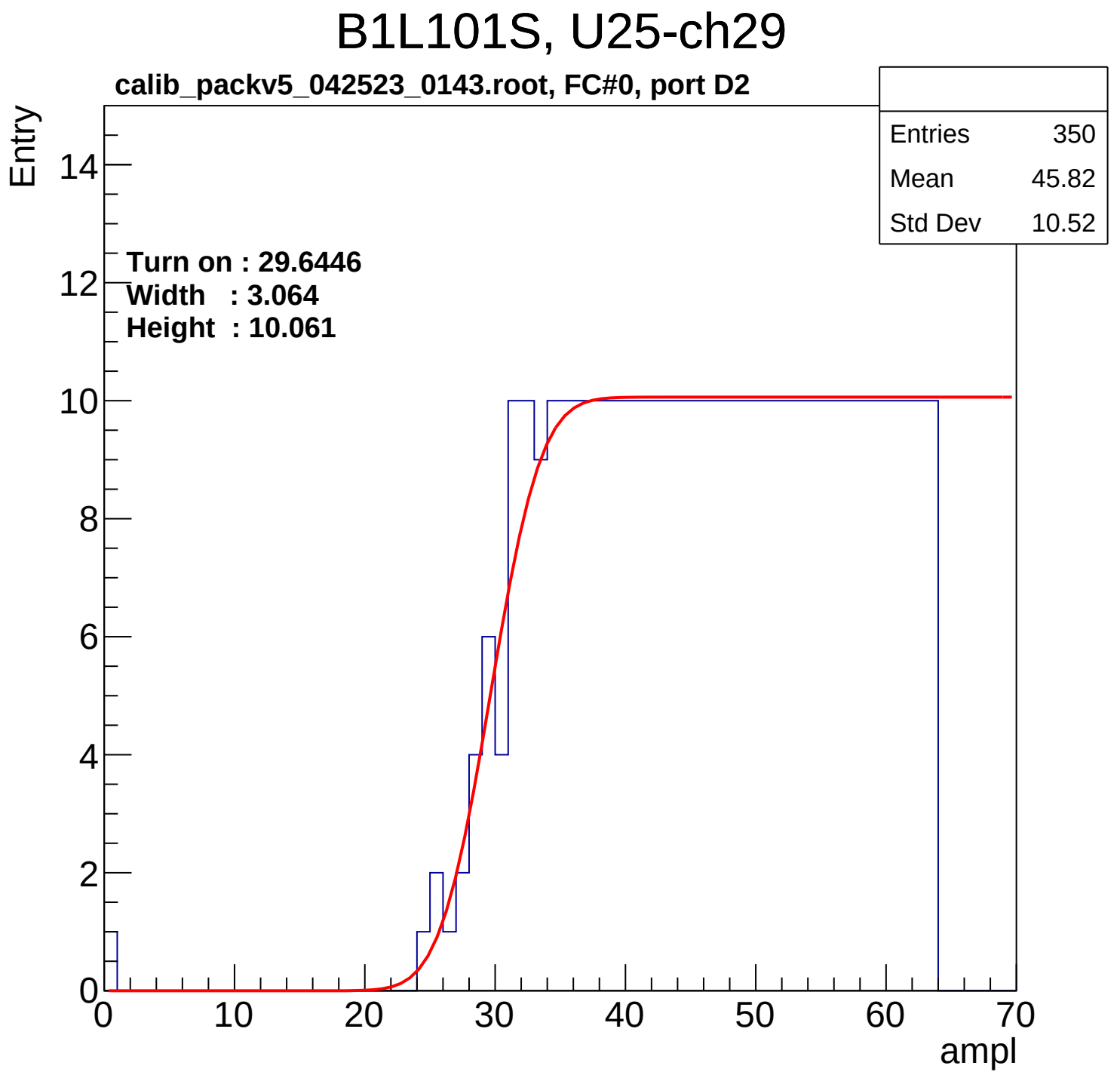
B1L101S, U25-ch29
calib_packv5_042523_0143.root, FC#0, port D2
Entries 350
Mean 45.82
Std Dev 10.52
Turn on : 29.6446
Width : 3.064
Height : 10.061
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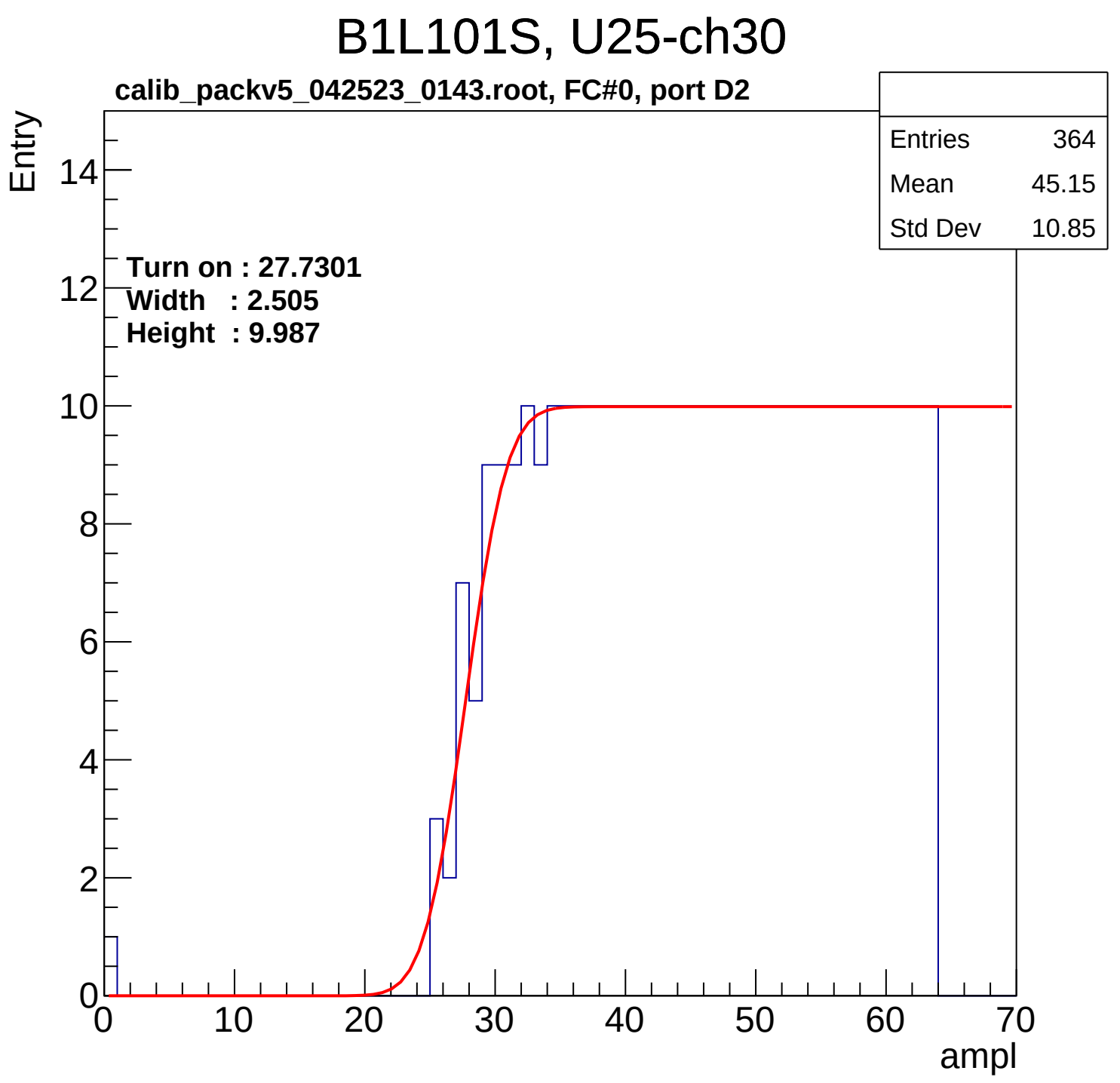
B1L101S, U25-ch30
calib_packv5_042523_0143.root, FC#0, port D2
Entries 364
Mean 45.15
Std Dev 10.85
Turn on : 27.7301
Width : 2.505
Height : 9.987
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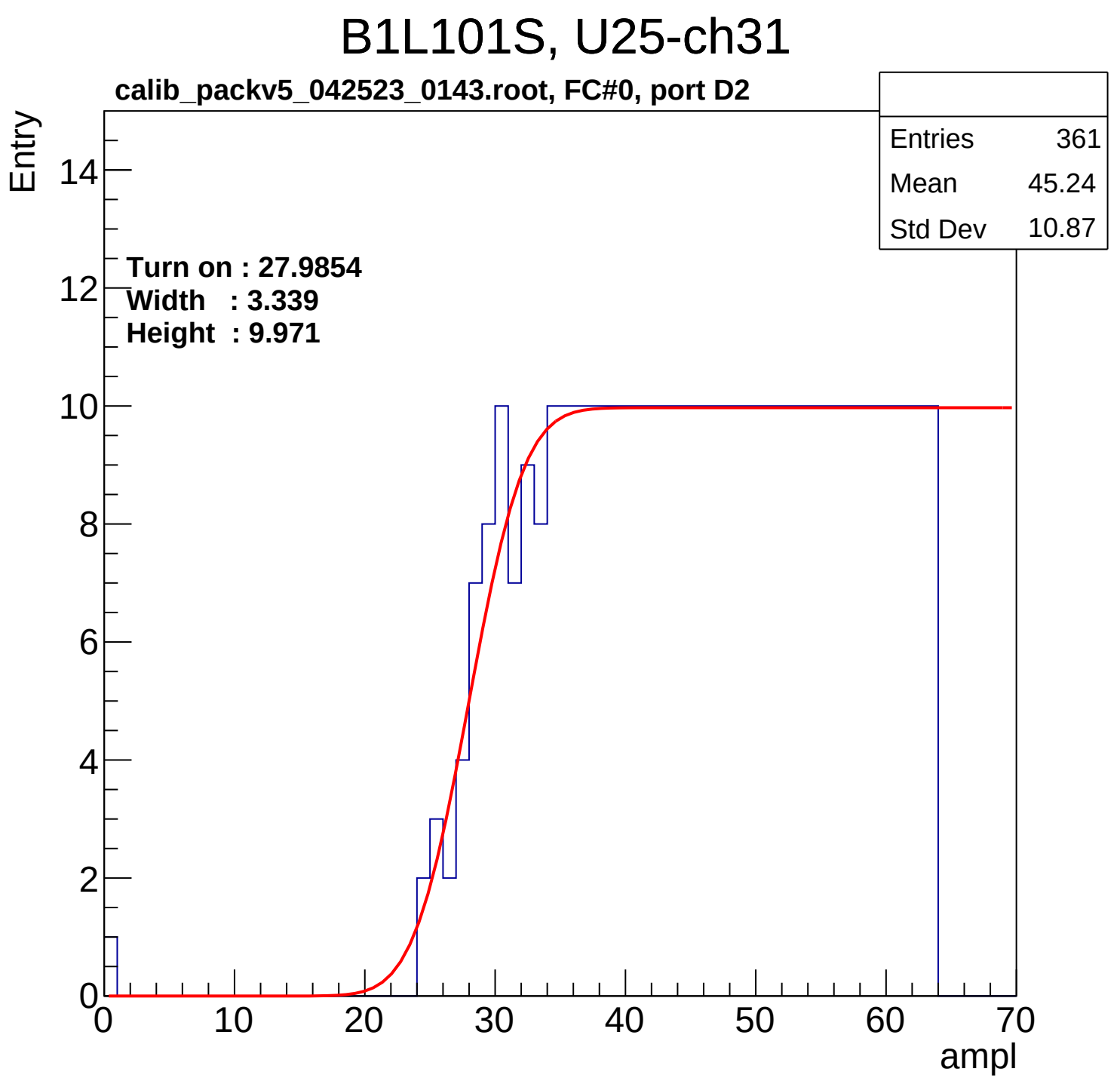
B1L101S, U25-ch31
calib_packv5_042523_0143.root, FC#0, port D2
Entries 361
Mean 45.24
Std Dev 10.87
Turn on : 27.9854
Width : 3.339
Height : 9.971
Entry
ampl
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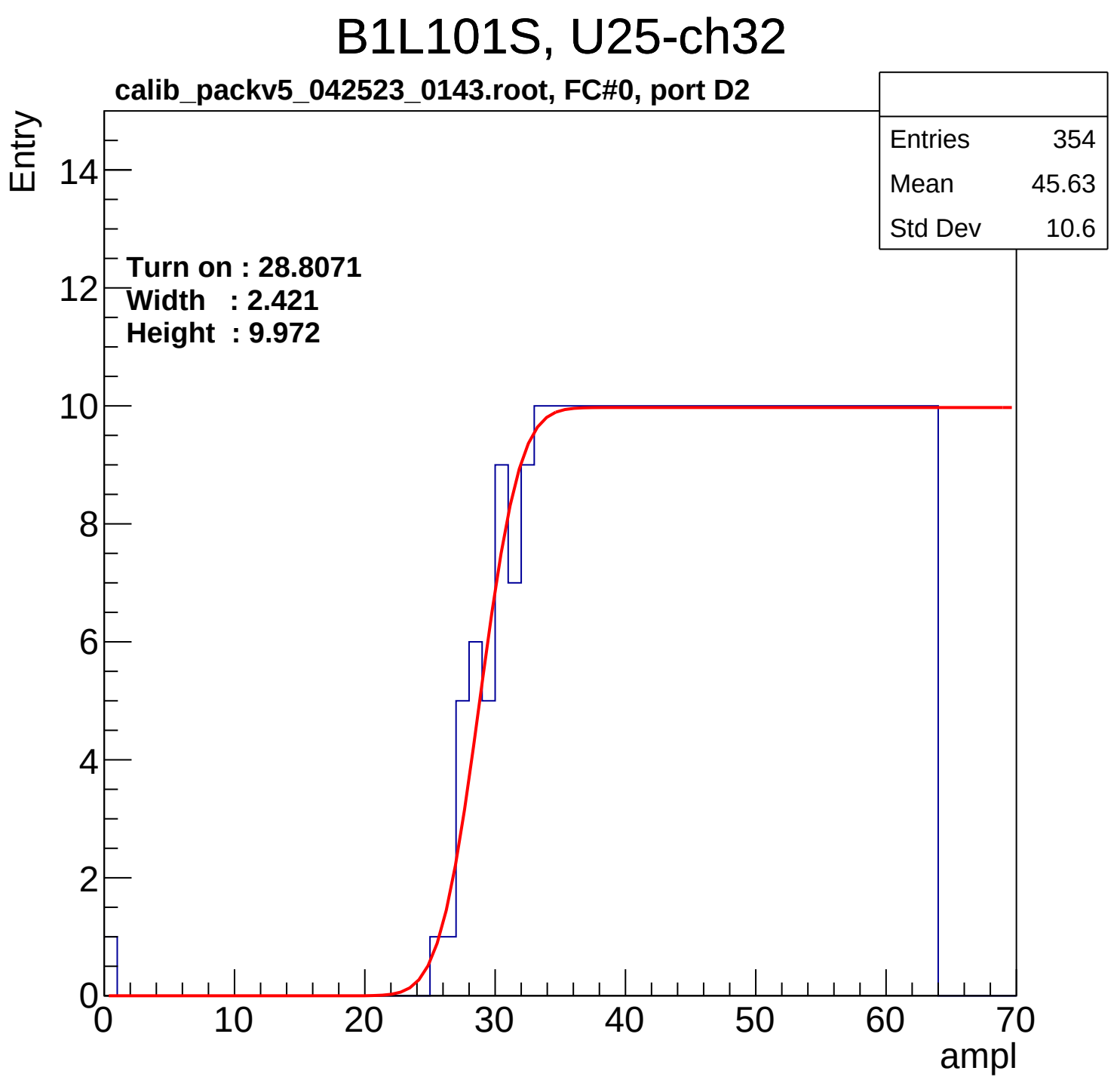
B1L101S, U25-ch32
calib_packv5_042523_0143.root, FC#0, port D2
Entries 354
Mean 45.63
Std Dev 10.6
Turn on : 28.8071
Width : 2.421
Height : 9.972
Entry
ampl
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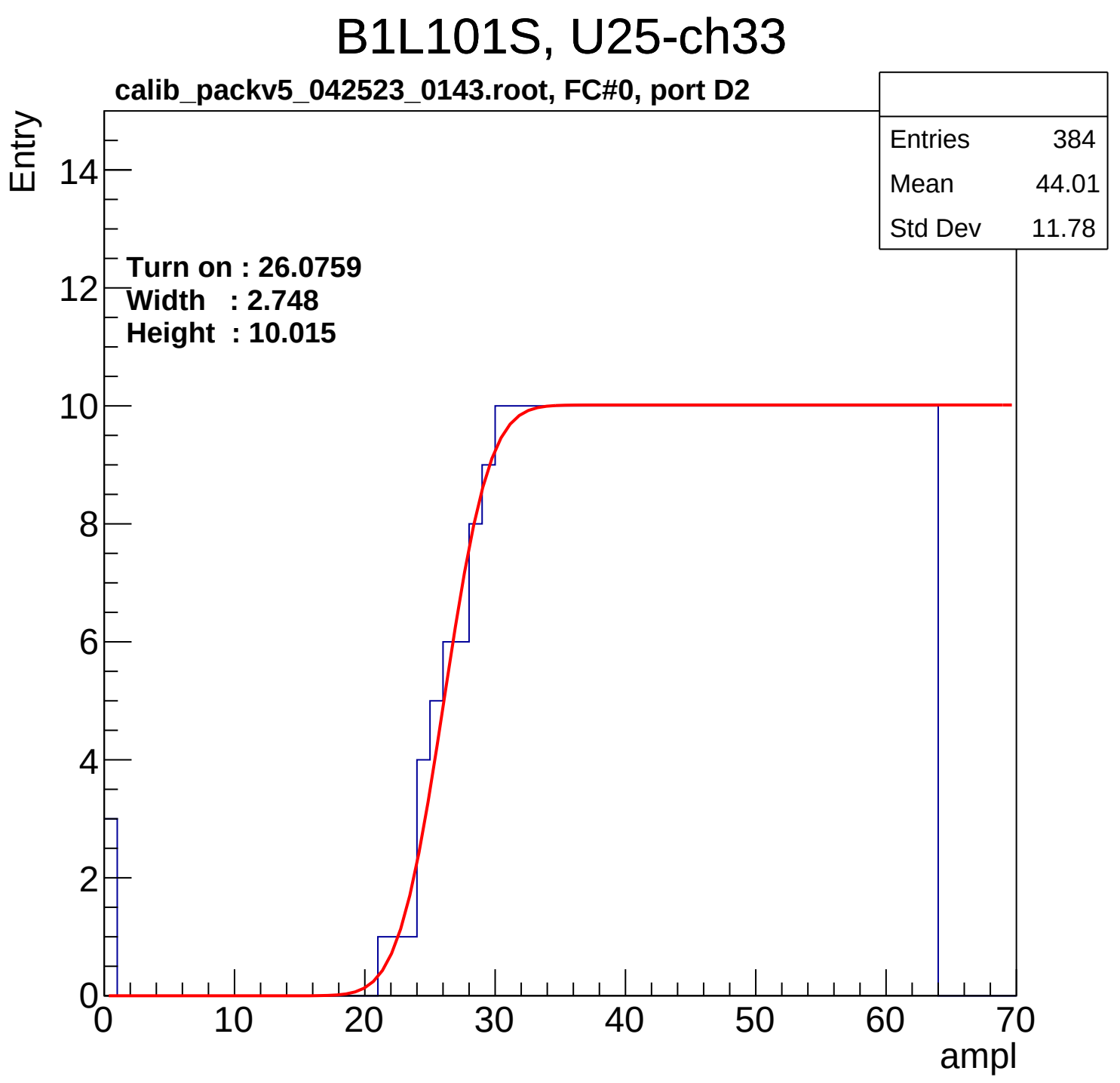
B1L101S, U25-ch33
calib_packv5_042523_0143.root, FC#0, port D2
Entries 384
Mean 44.01
Std Dev 11.78
Turn on : 26.0759
Width : 2.748
Height : 10.015
Entry
ampl
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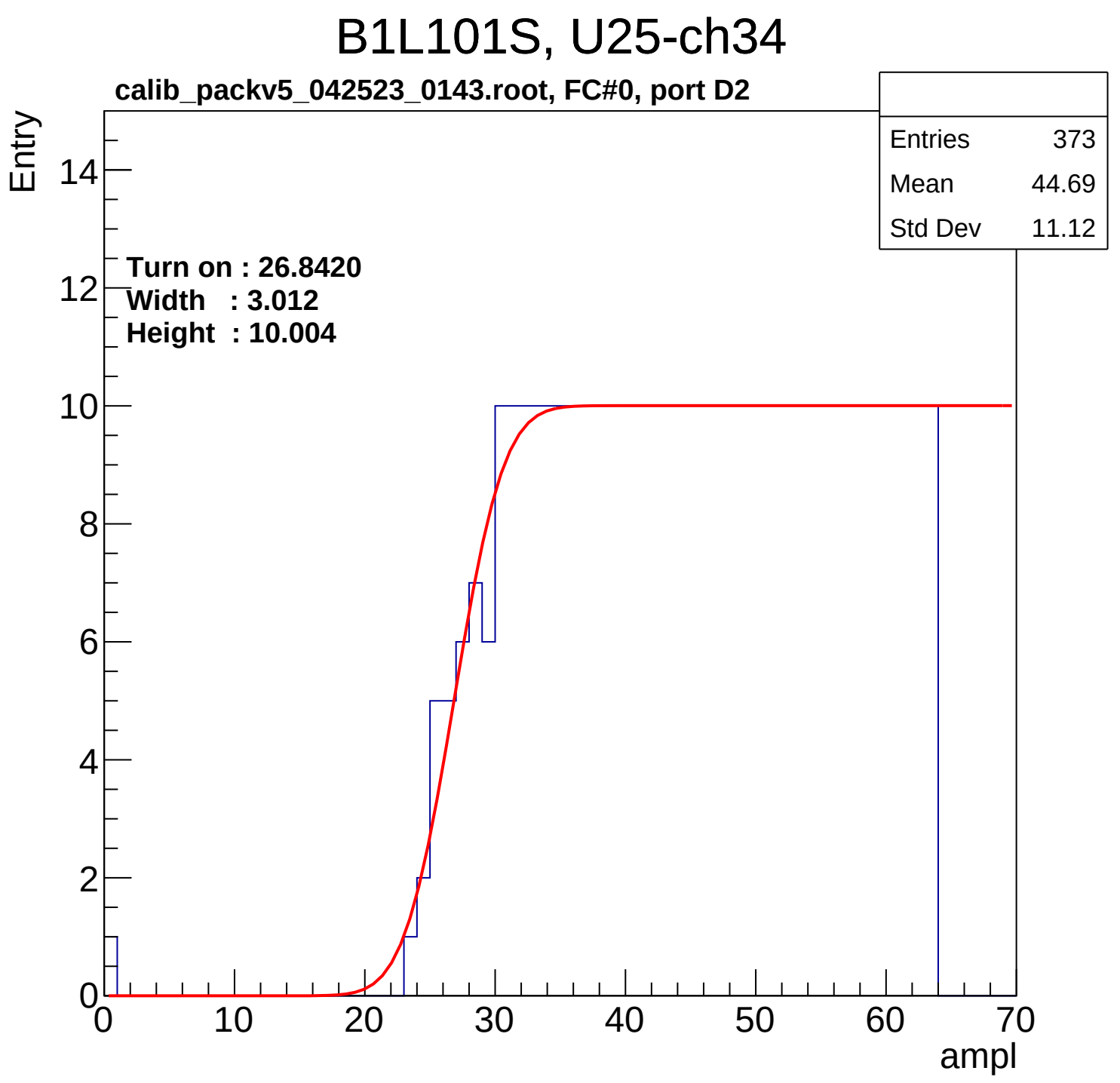
B1L101S, U25-ch34
calib_packv5_042523_0143.root, FC#0, port D2
Entries 373
Mean 44.69
Std Dev 11.12
Turn on : 26.8420
Width : 3.012
Height : 10.004
Entry
ampl
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6
8
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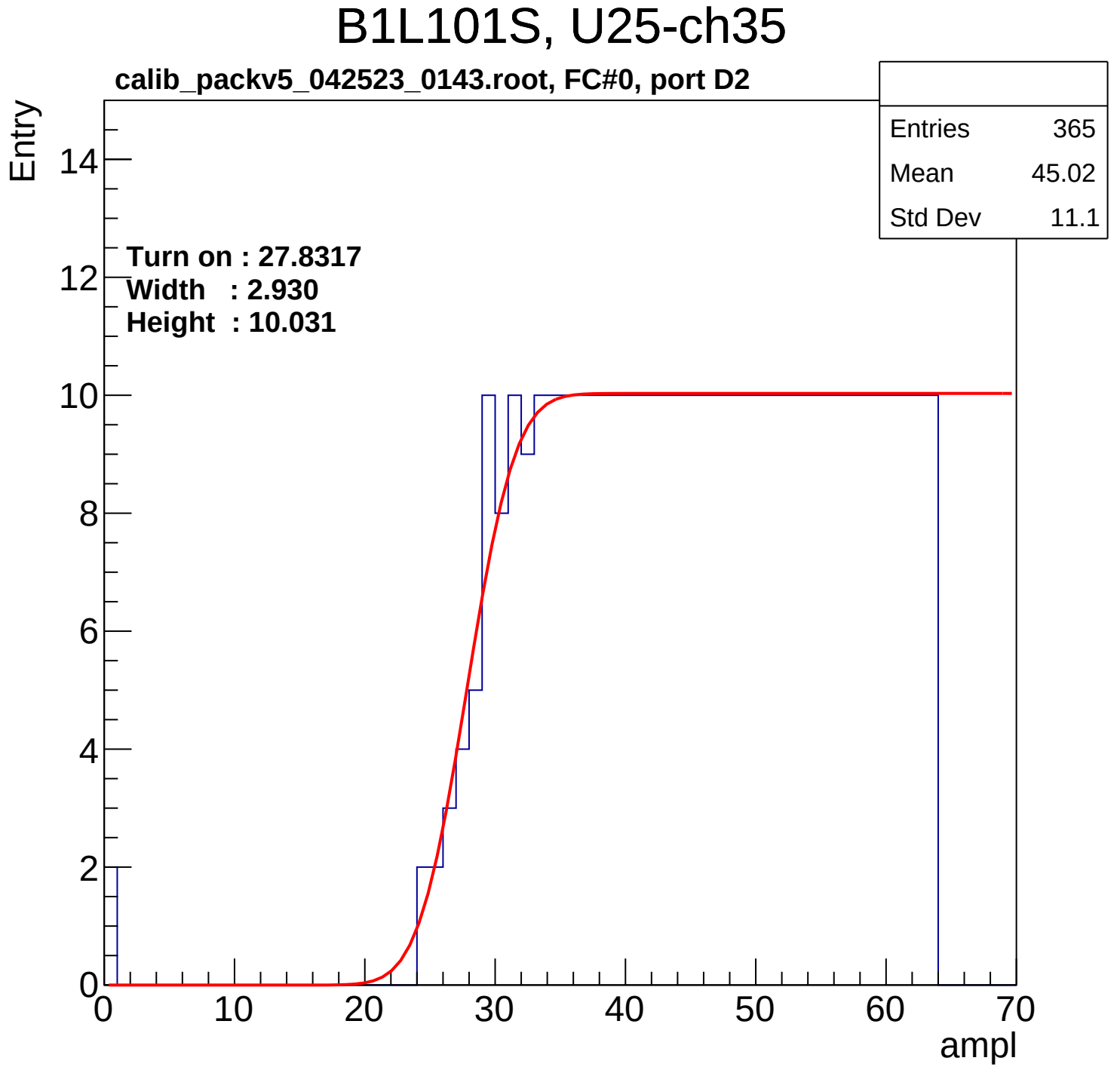
B1L101S, U25-ch35
calib_packv5_042523_0143.root, FC#0, port D2
Entries 365
Mean 45.02
Std Dev 11.1
Turn on : 27.8317
Width : 2.930
Height : 10.031
Entry
ampl
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6
8
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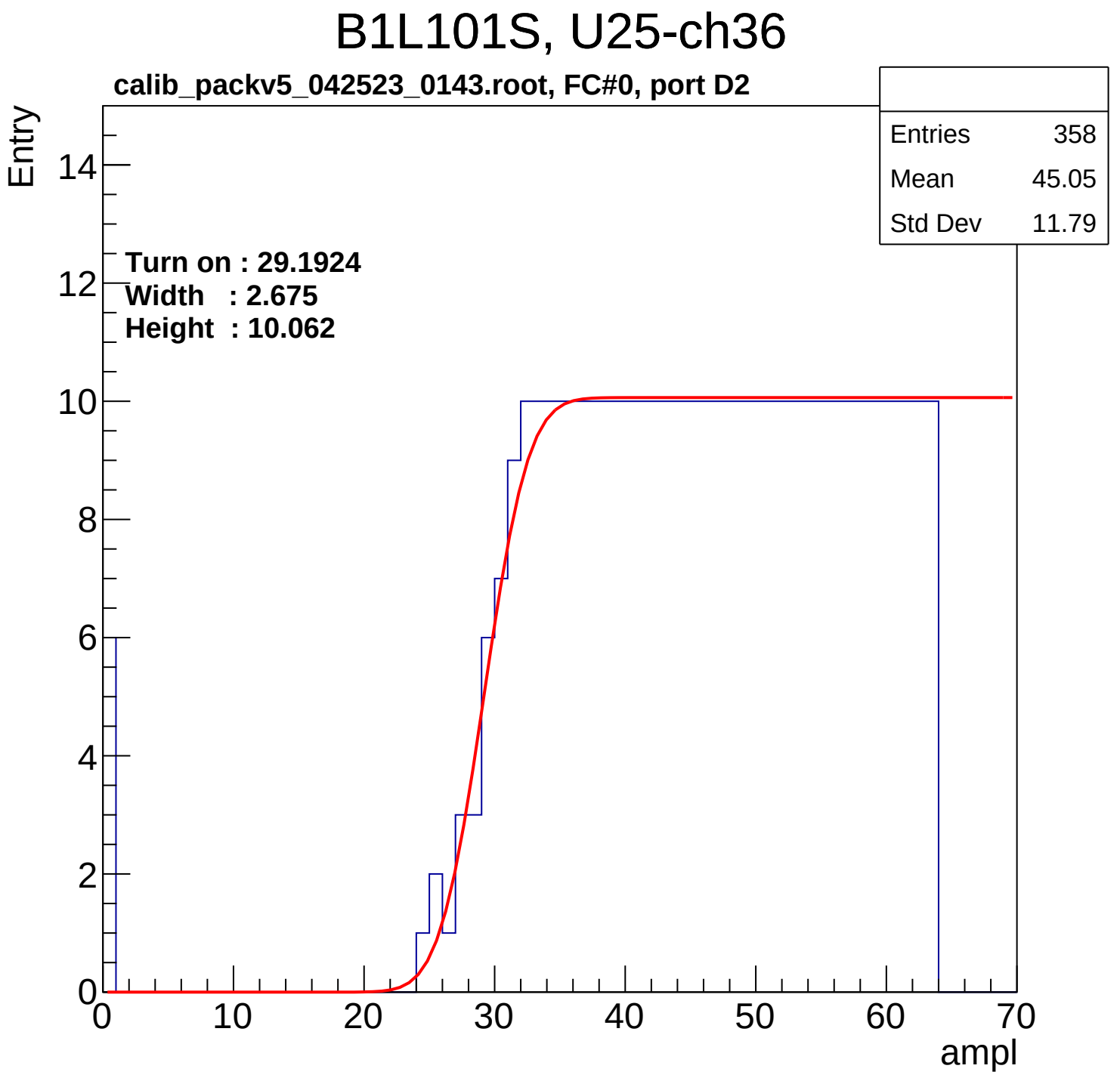
B1L101S, U25-ch36
calib_packv5_042523_0143.root, FC#0, port D2
Entries 358
Mean 45.05
Std Dev 11.79
Turn on : 29.1924
Width : 2.675
Height : 10.062
Entry
ampl
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6
8
10
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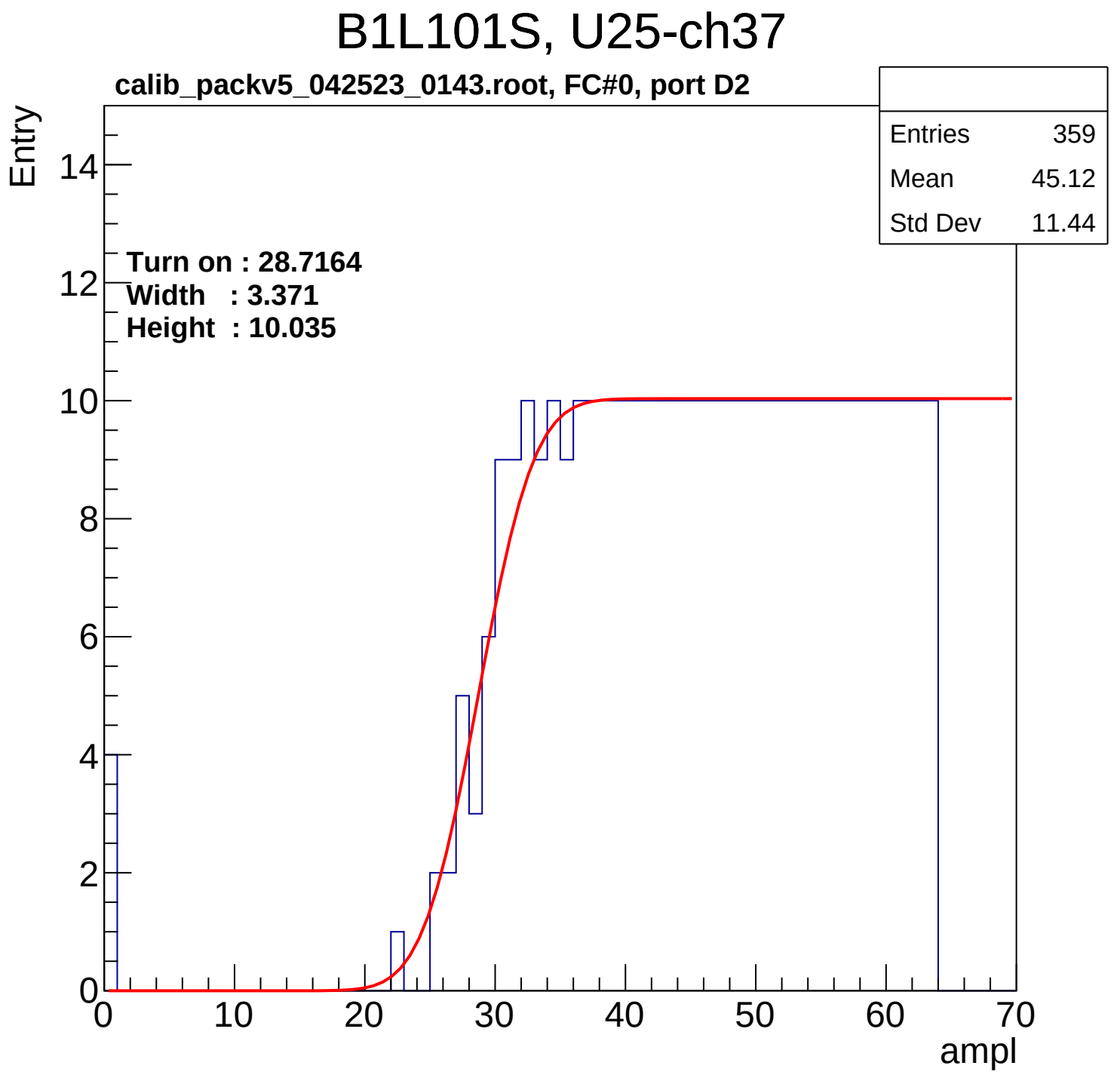
B1L101S, U25-ch37
calib_packv5_042523_0143.root, FC#0, port D2
Entries 359
Mean 45.12
Std Dev 11.44
Turn on : 28.7164
Width : 3.371
Height : 10.035
Entry
ampl
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2
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6
8
10
12
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0
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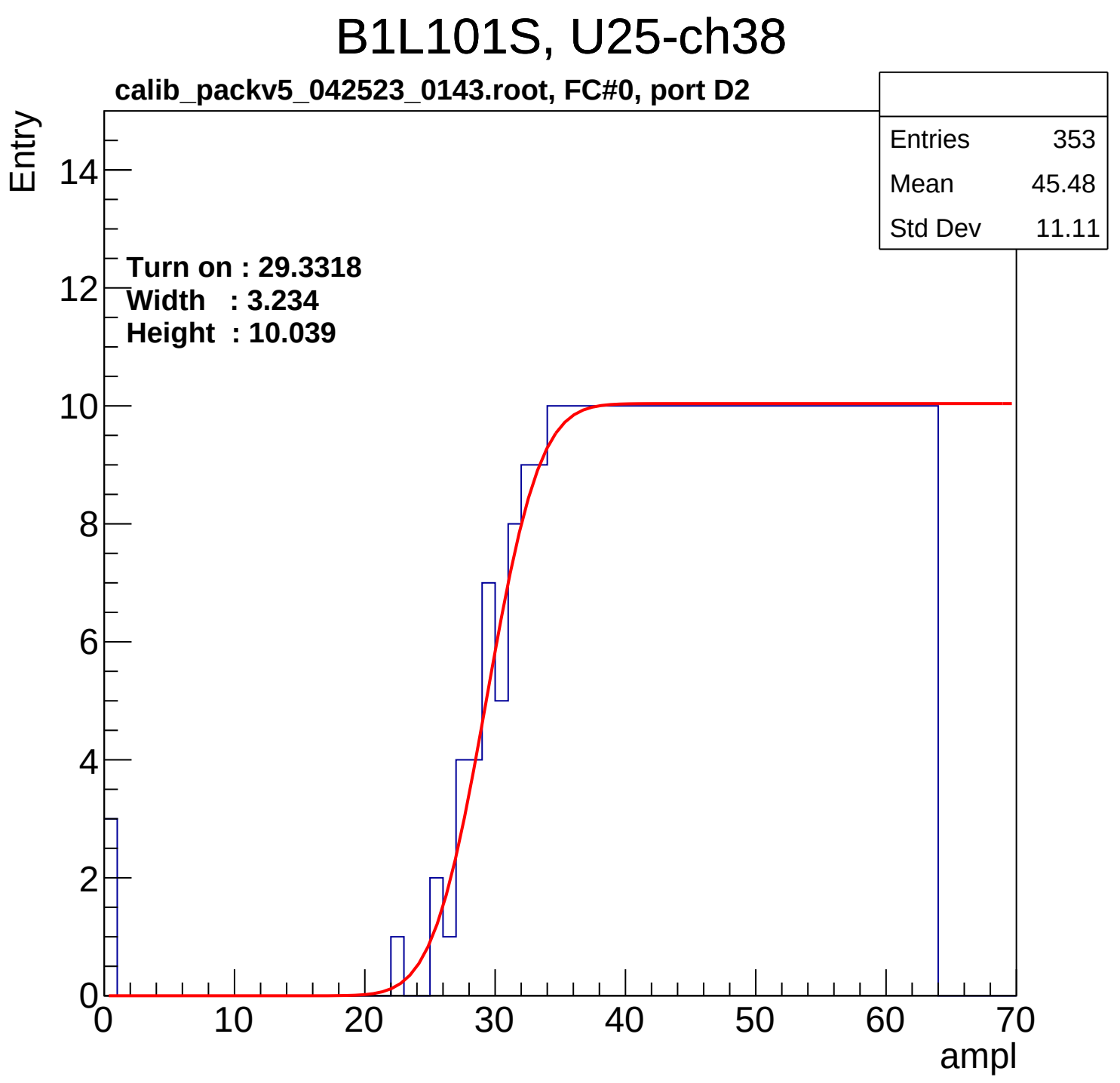
B1L101S, U25-ch38
calib_packv5_042523_0143.root, FC#0, port D2
Entries 353
Mean 45.48
Std Dev 11.11
Turn on : 29.3318
Width : 3.234
Height : 10.039
Entry
ampl
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6
8
10
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60
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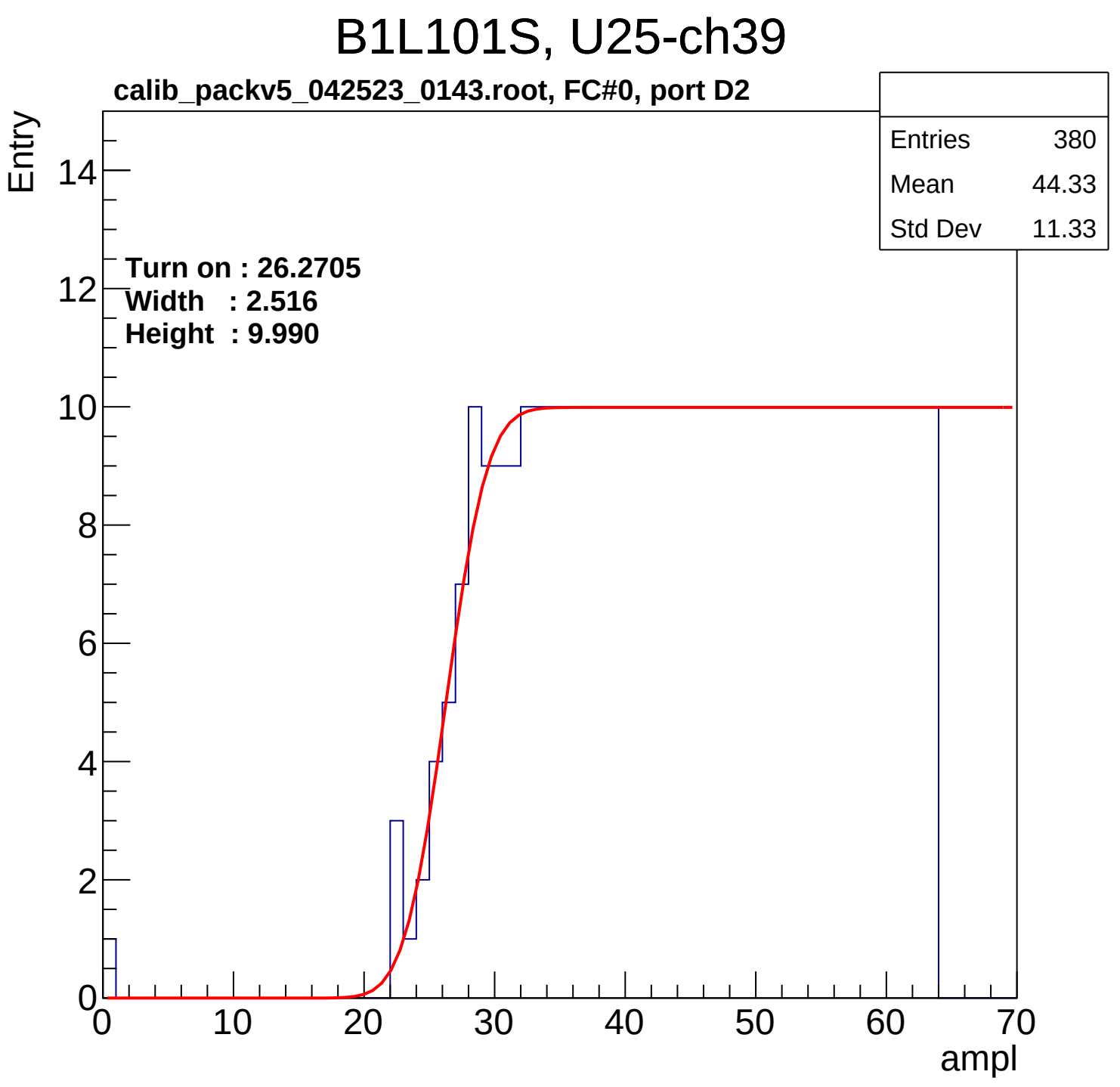
B1L101S, U25-ch39
calib_packv5_042523_0143.root, FC#0, port D2
Entries 380
Mean 44.33
Std Dev 11.33
Turn on : 26.2705
Width : 2.516
Height : 9.990
Entry
ampl
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6
8
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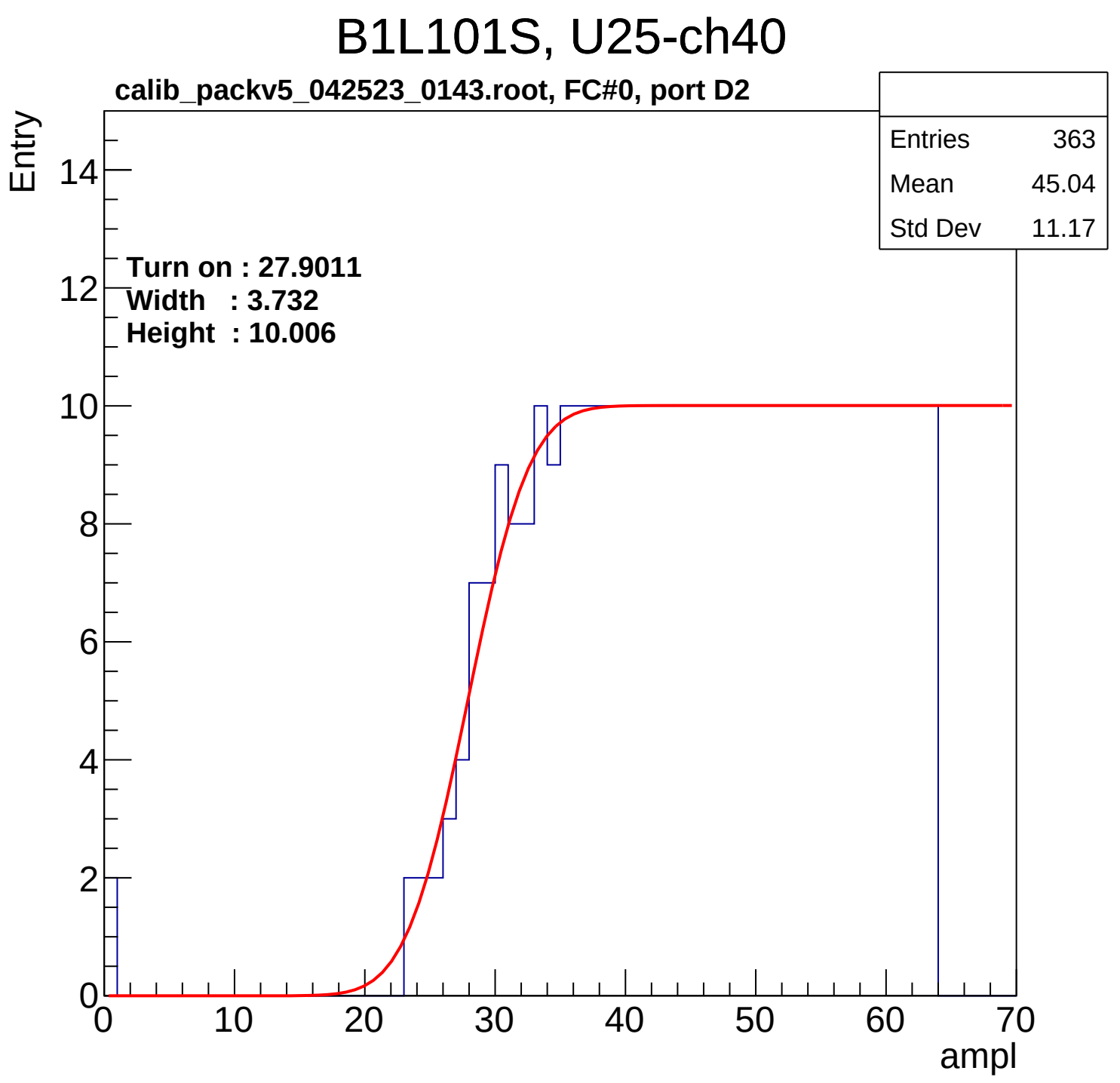
B1L101S, U25-ch40
calib_packv5_042523_0143.root, FC#0, port D2
Entries 363
Mean 45.04
Std Dev 11.17
Turn on : 27.9011
Width : 3.732
Height : 10.006
Entry
ampl
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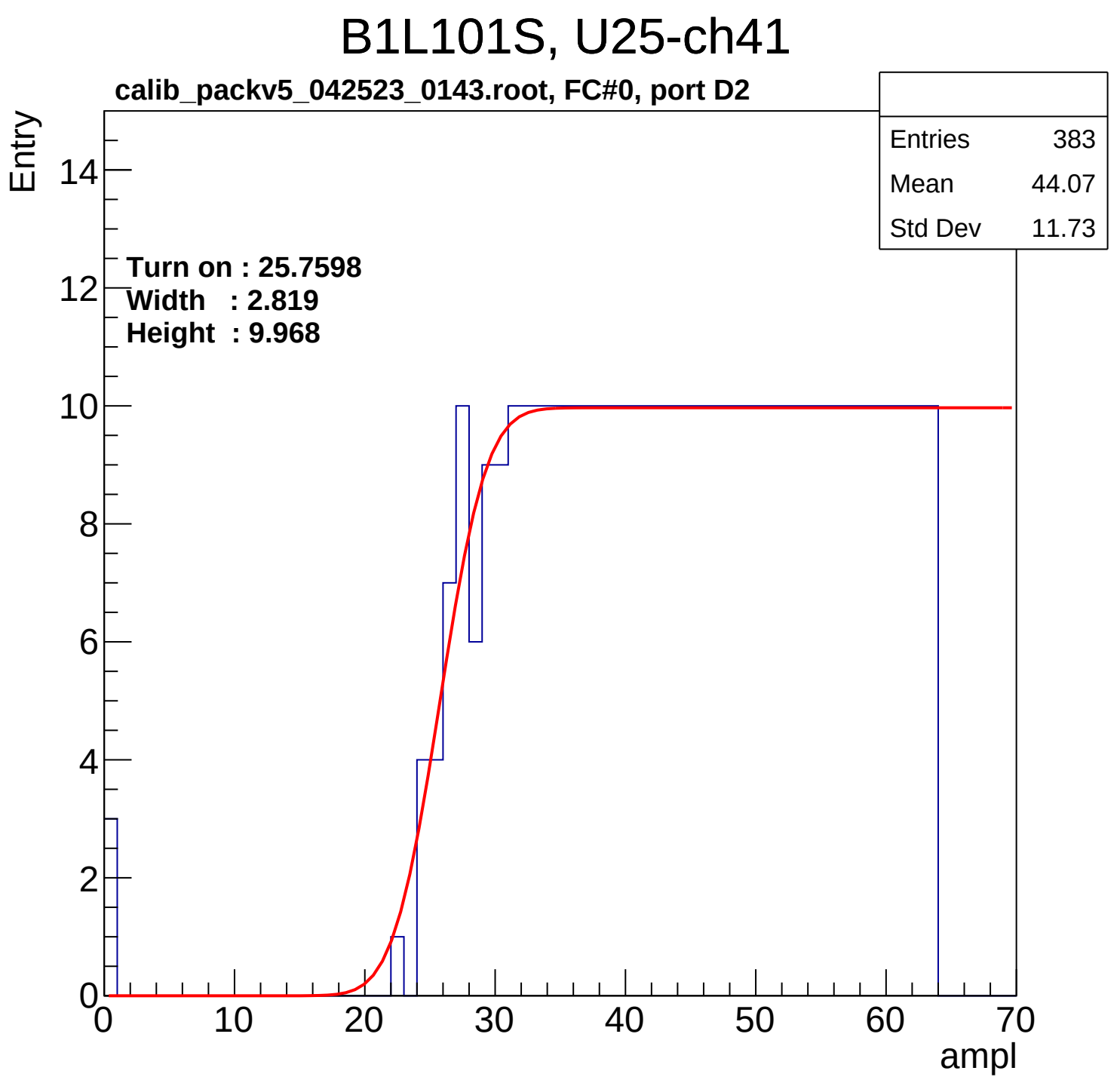
B1L101S, U25-ch41
calib_packv5_042523_0143.root, FC#0, port D2
Entries 383
Mean 44.07
Std Dev 11.73
Turn on : 25.7598
Width : 2.819
Height : 9.968
Entry
ampl
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6
8
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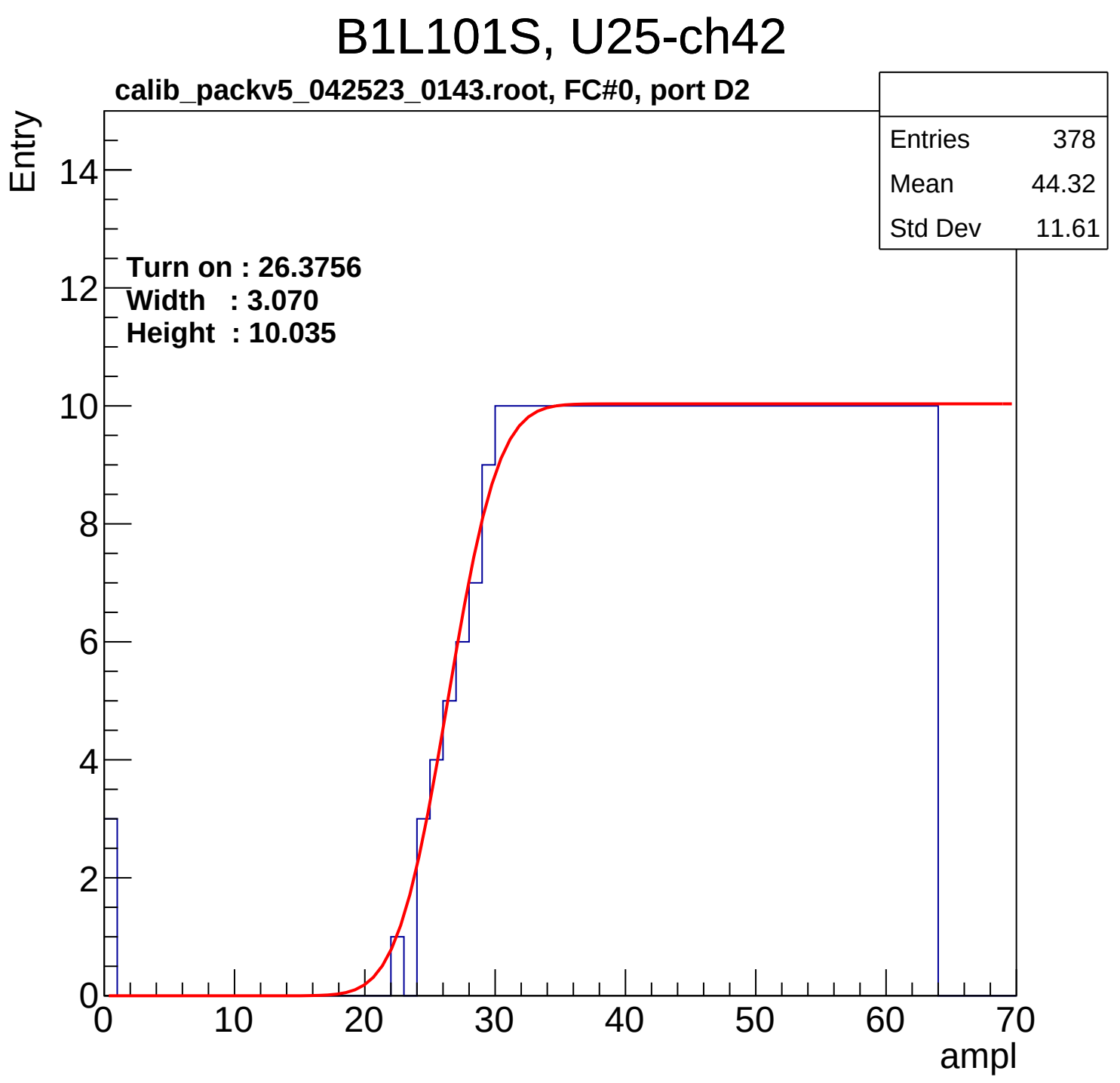
B1L101S, U25-ch42
calib_packv5_042523_0143.root, FC#0, port D2
Entries 378
Mean 44.32
Std Dev 11.61
Turn on : 26.3756
Width : 3.070
Height : 10.035
Entry
ampl
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6
8
10
12
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0
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60
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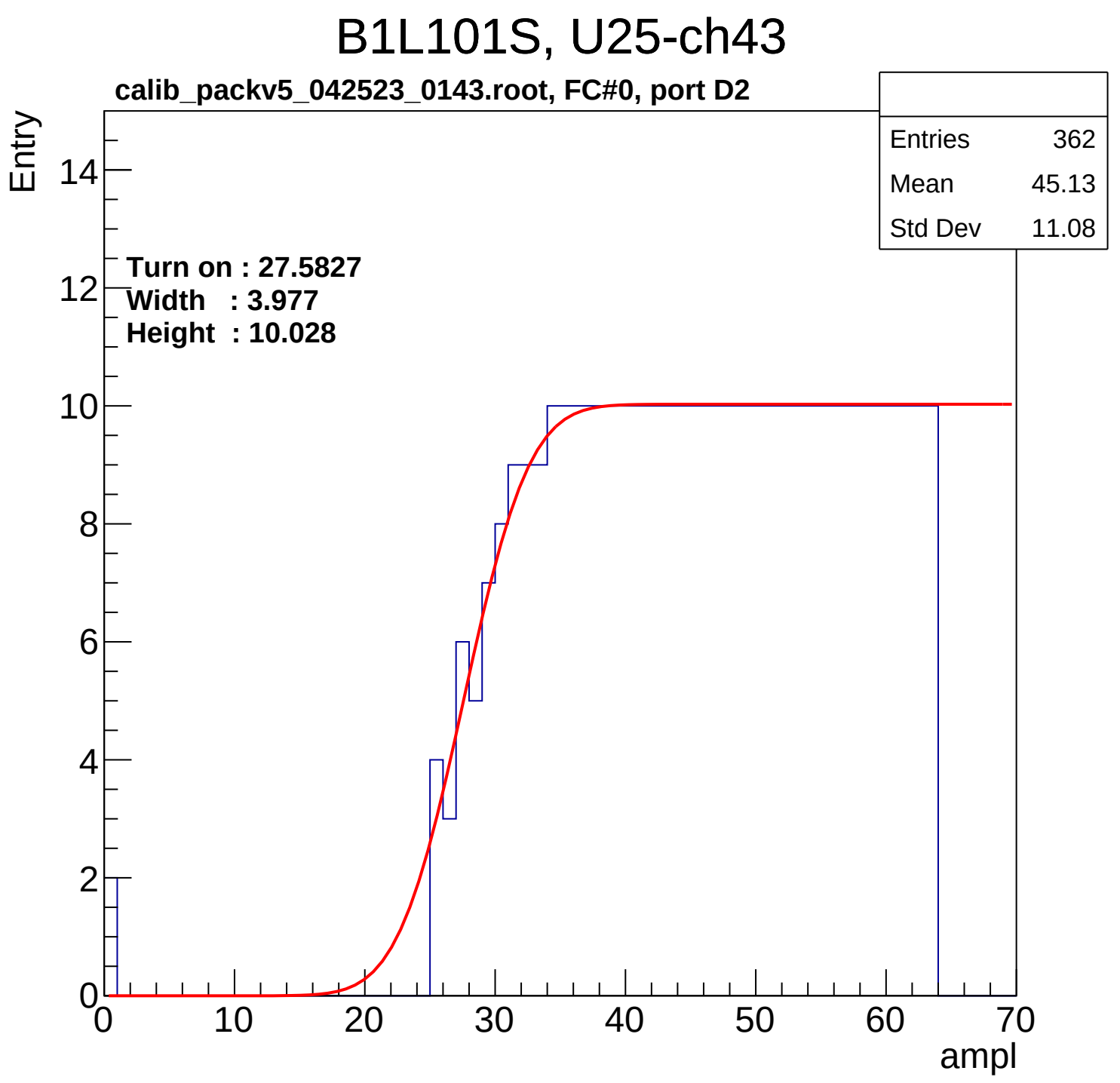
B1L101S, U25-ch43
calib_packv5_042523_0143.root, FC#0, port D2
Entries 362
Mean 45.13
Std Dev 11.08
Turn on : 27.5827
Width : 3.977
Height : 10.028
Entry
ampl
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6
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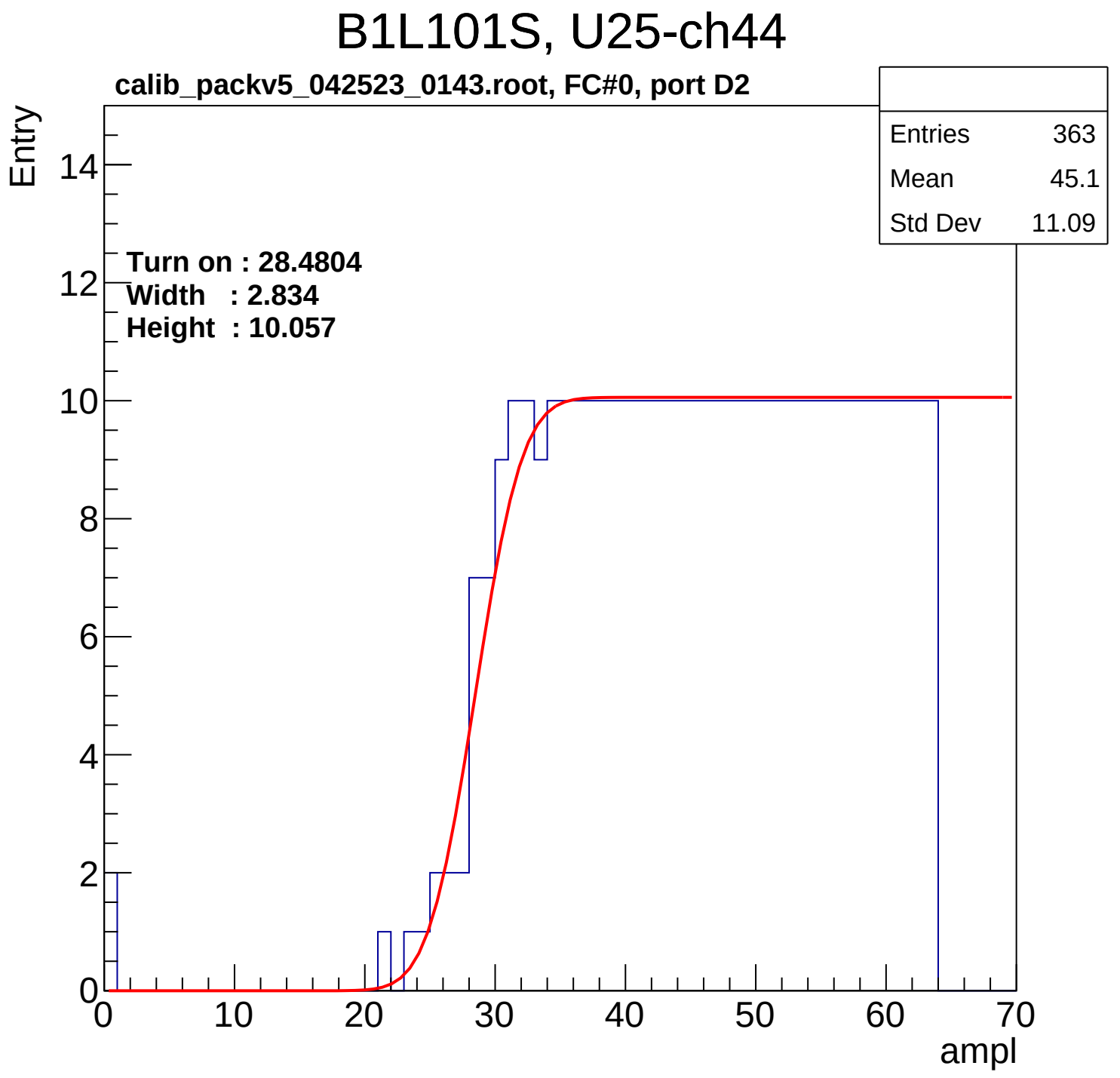
B1L101S, U25-ch44
calib_packv5_042523_0143.root, FC#0, port D2
Entries 363
Mean 45.1
Std Dev 11.09
Turn on : 28.4804
Width : 2.834
Height : 10.057
Entry
ampl
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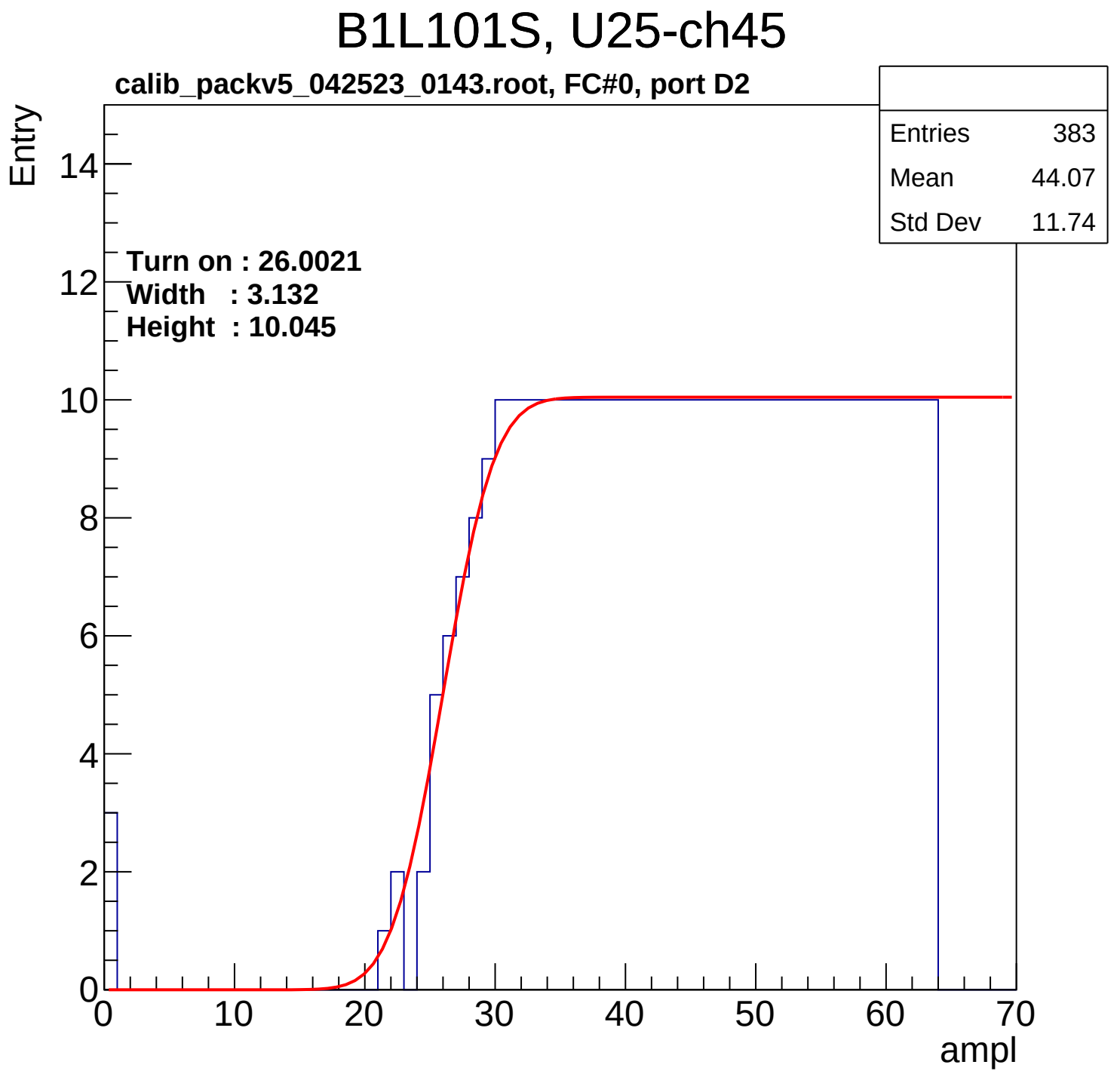
B1L101S, U25-ch45
calib_packv5_042523_0143.root, FC#0, port D2
Entries 383
Mean 44.07
Std Dev 11.74
Turn on : 26.0021
Width : 3.132
Height : 10.045
Entry
ampl
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8
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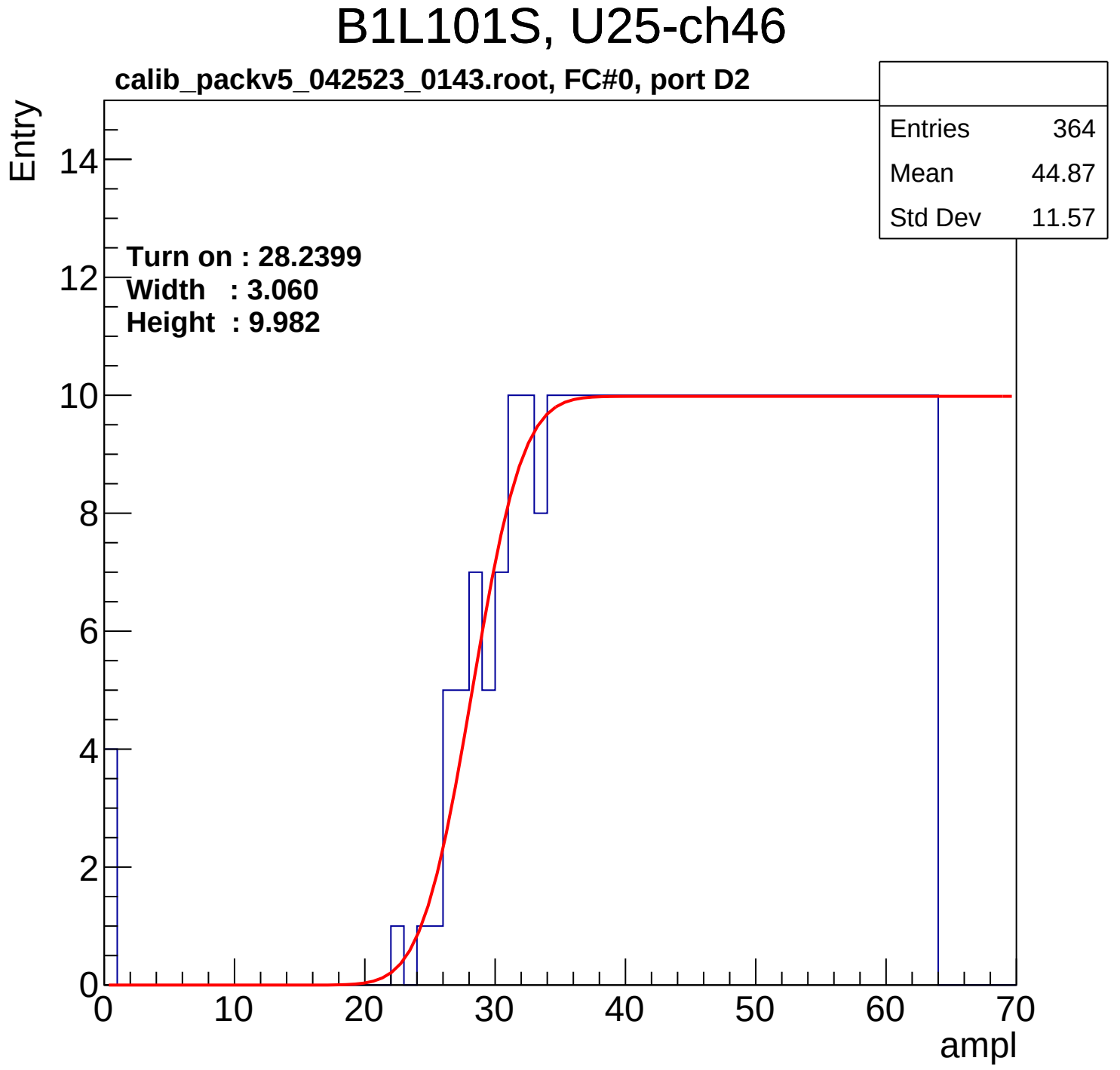
B1L101S, U25-ch46
calib_packv5_042523_0143.root, FC#0, port D2
Entries 364
Mean 44.87
Std Dev 11.57
Turn on : 28.2399
Width : 3.060
Height : 9.982
Entry
ampl
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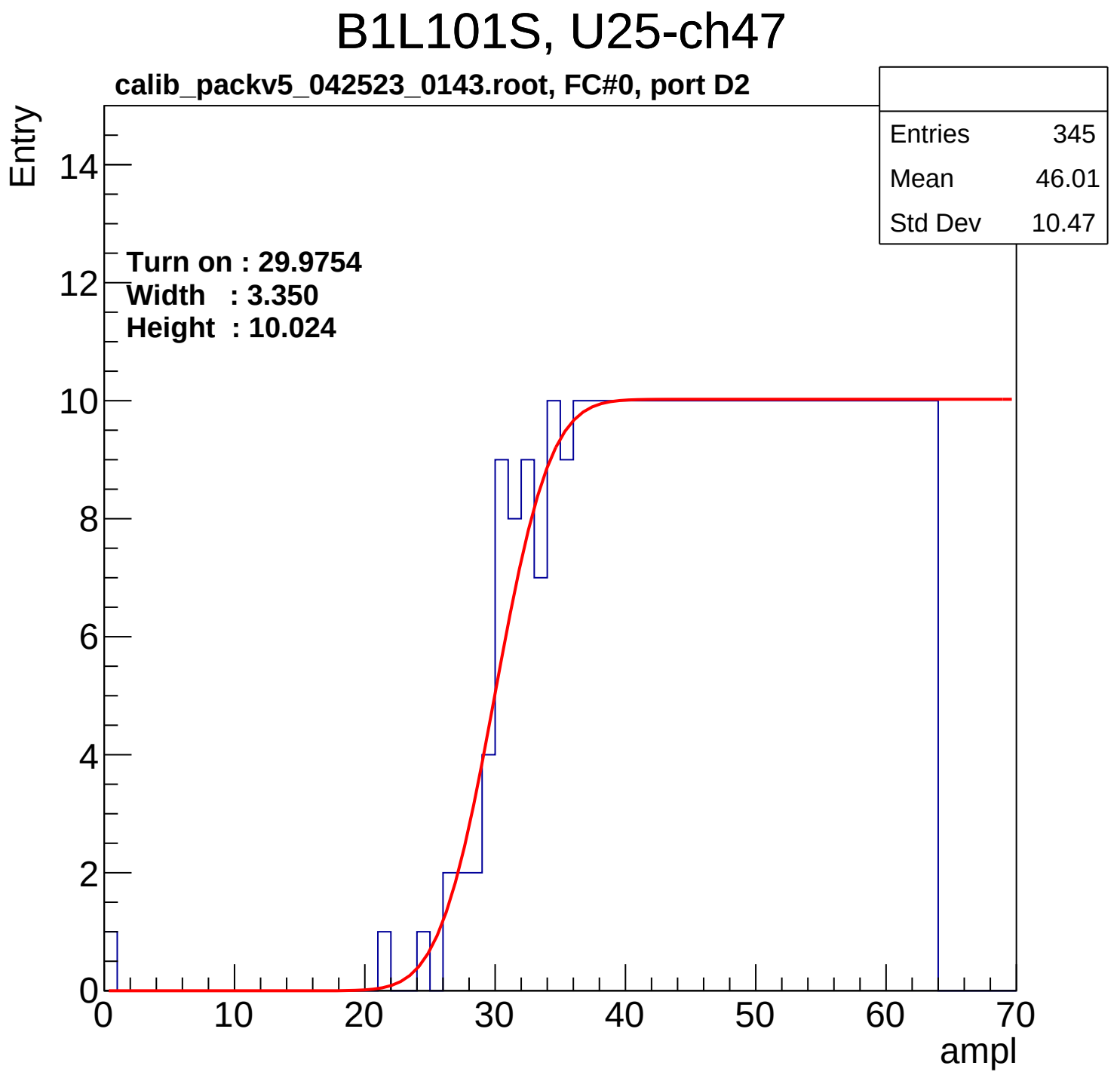
B1L101S, U25-ch47
calib_packv5_042523_0143.root, FC#0, port D2
Entries 345
Mean 46.01
Std Dev 10.47
Turn on : 29.9754
Width : 3.350
Height : 10.024
Entry
ampl
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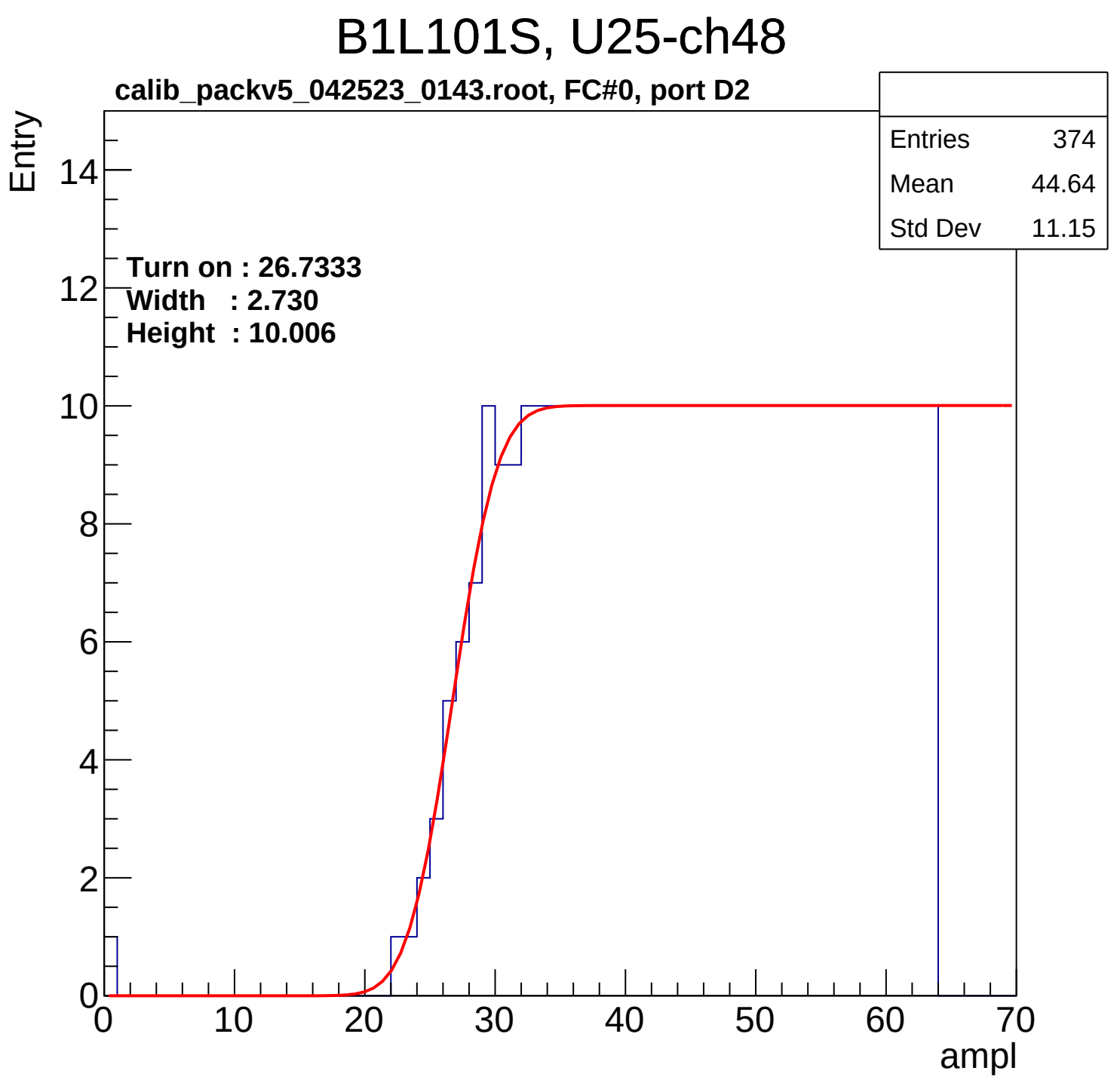
B1L101S, U25-ch48
calib_packv5_042523_0143.root, FC#0, port D2
Entries 374
Mean 44.64
Std Dev 11.15
Turn on : 26.7333
Width : 2.730
Height : 10.006
Entry
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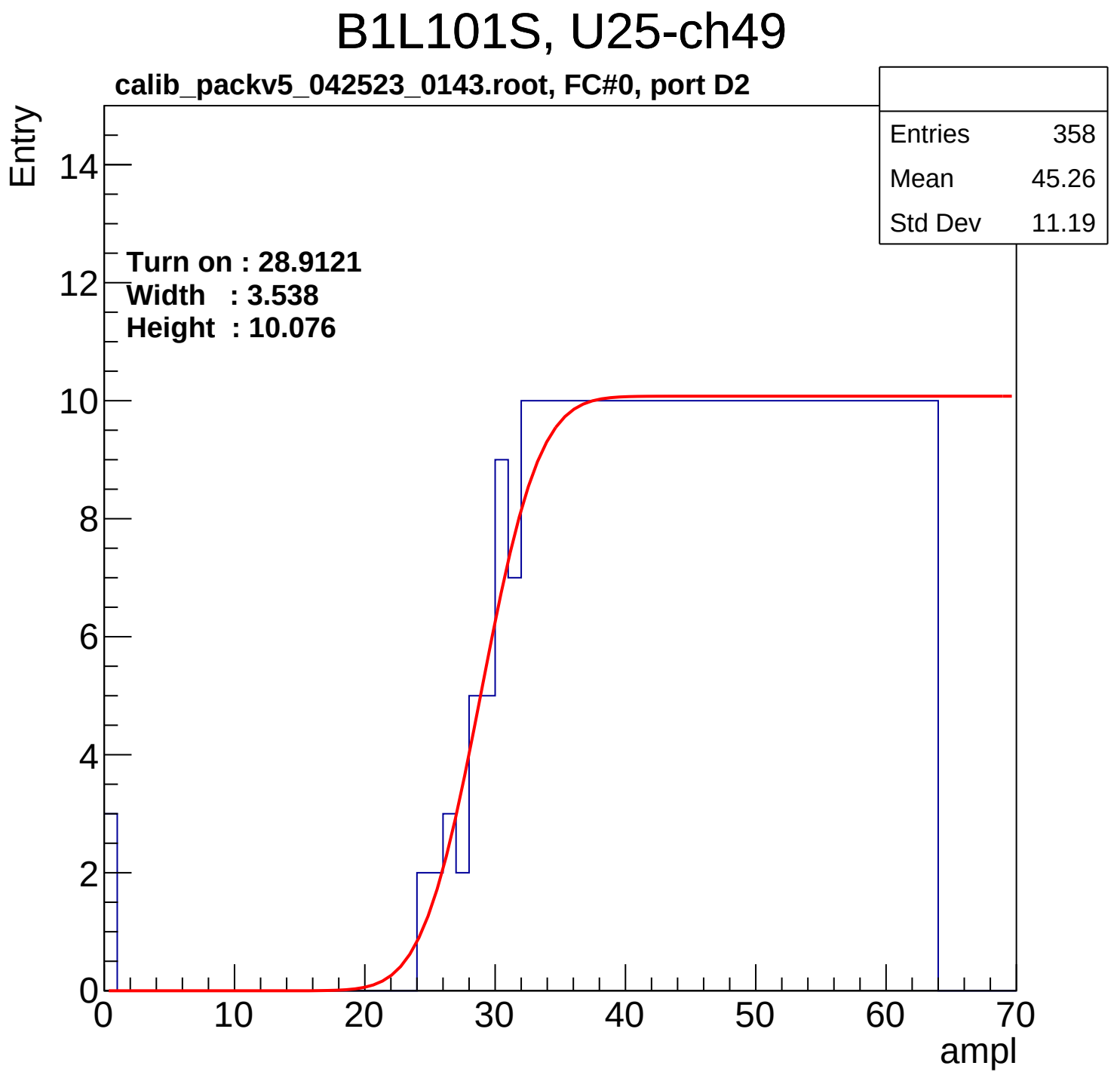
B1L101S, U25-ch49
calib_packv5_042523_0143.root, FC#0, port D2
Entries 358
Mean 45.26
Std Dev 11.19
Turn on : 28.9121
Width : 3.538
Height : 10.076
Entry
ampl
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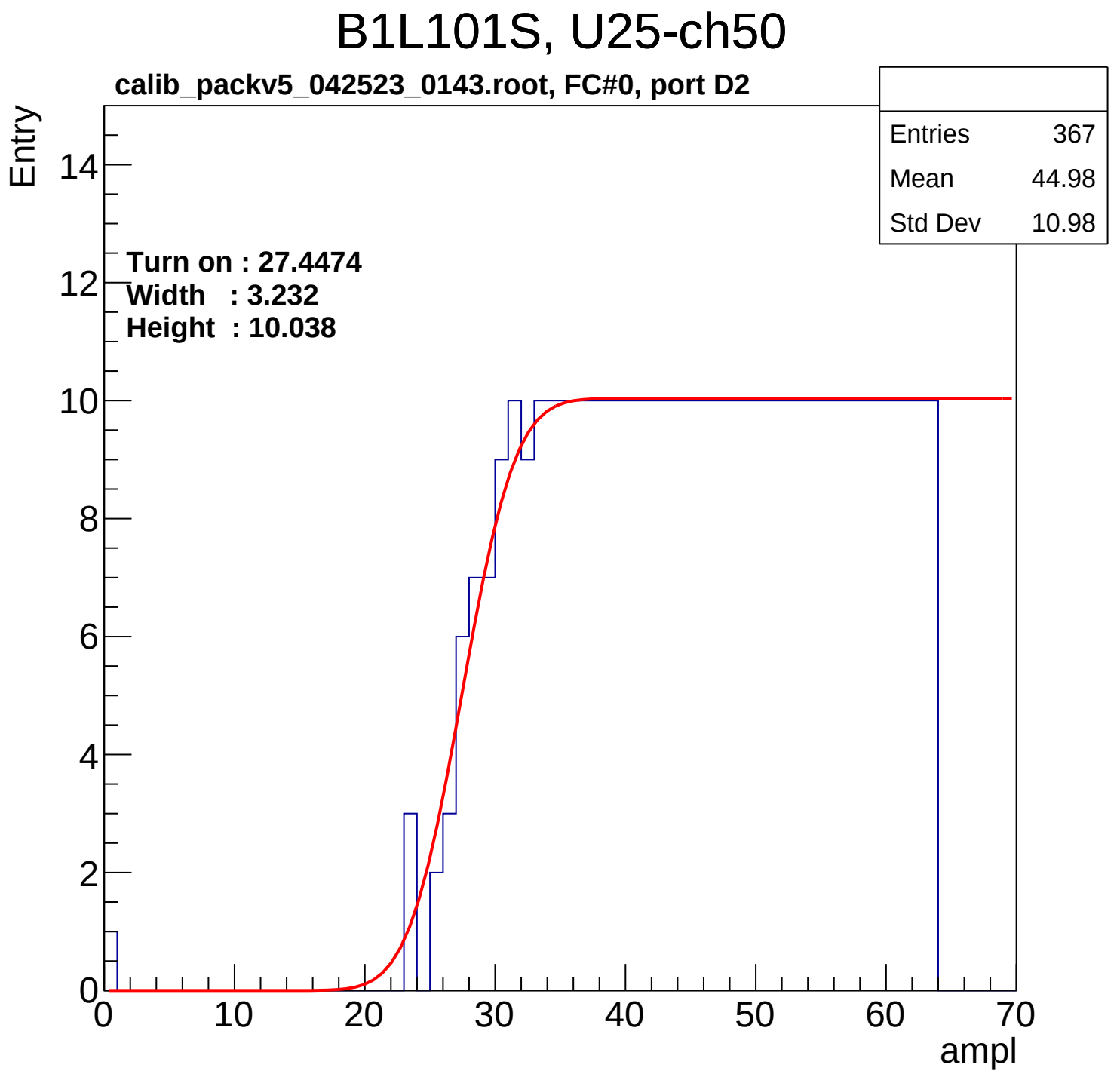
B1L101S, U25-ch50
calib_packv5_042523_0143.root, FC#0, port D2
Entries 367
Mean 44.98
Std Dev 10.98
Turn on : 27.4474
Width : 3.232
Height : 10.038
Entry
ampl
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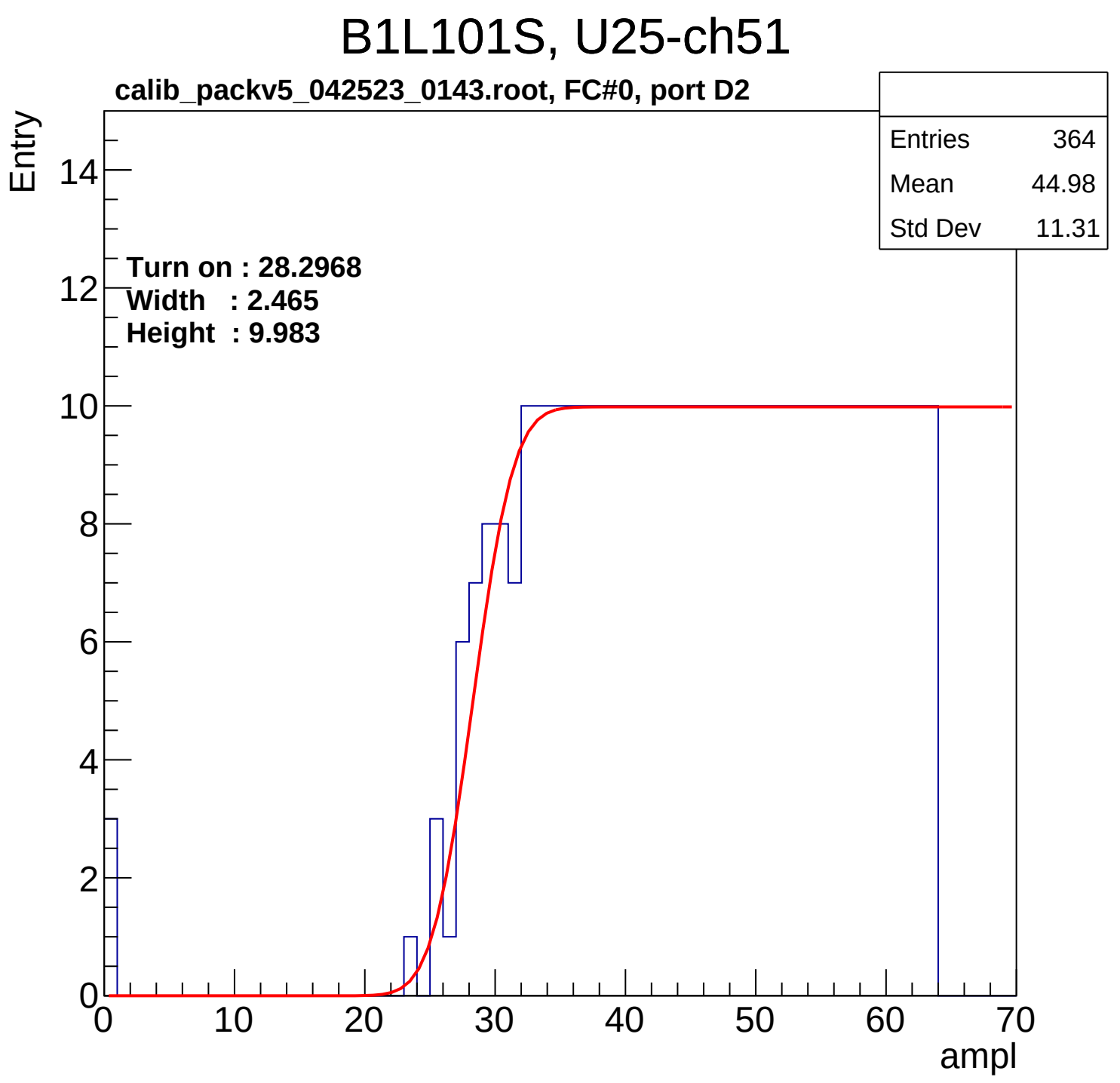
B1L101S, U25-ch51
calib_packv5_042523_0143.root, FC#0, port D2
Entries 364
Mean 44.98
Std Dev 11.31
Turn on : 28.2968
Width : 2.465
Height : 9.983
Entry
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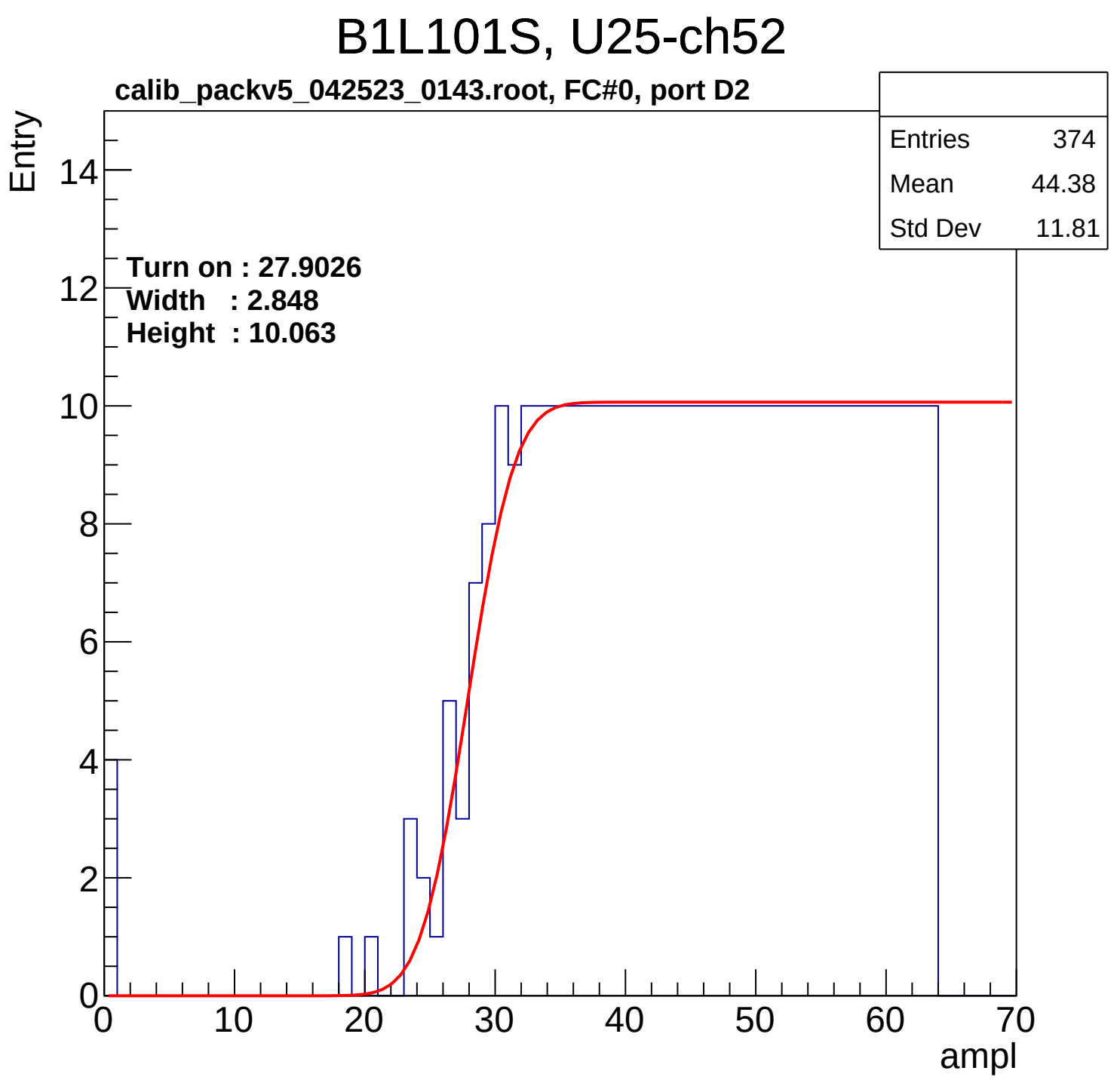
B1L101S, U25-ch52
calib_packv5_042523_0143.root, FC#0, port D2
Entries 374
Mean 44.38
Std Dev 11.81
Turn on : 27.9026
Width : 2.848
Height : 10.063
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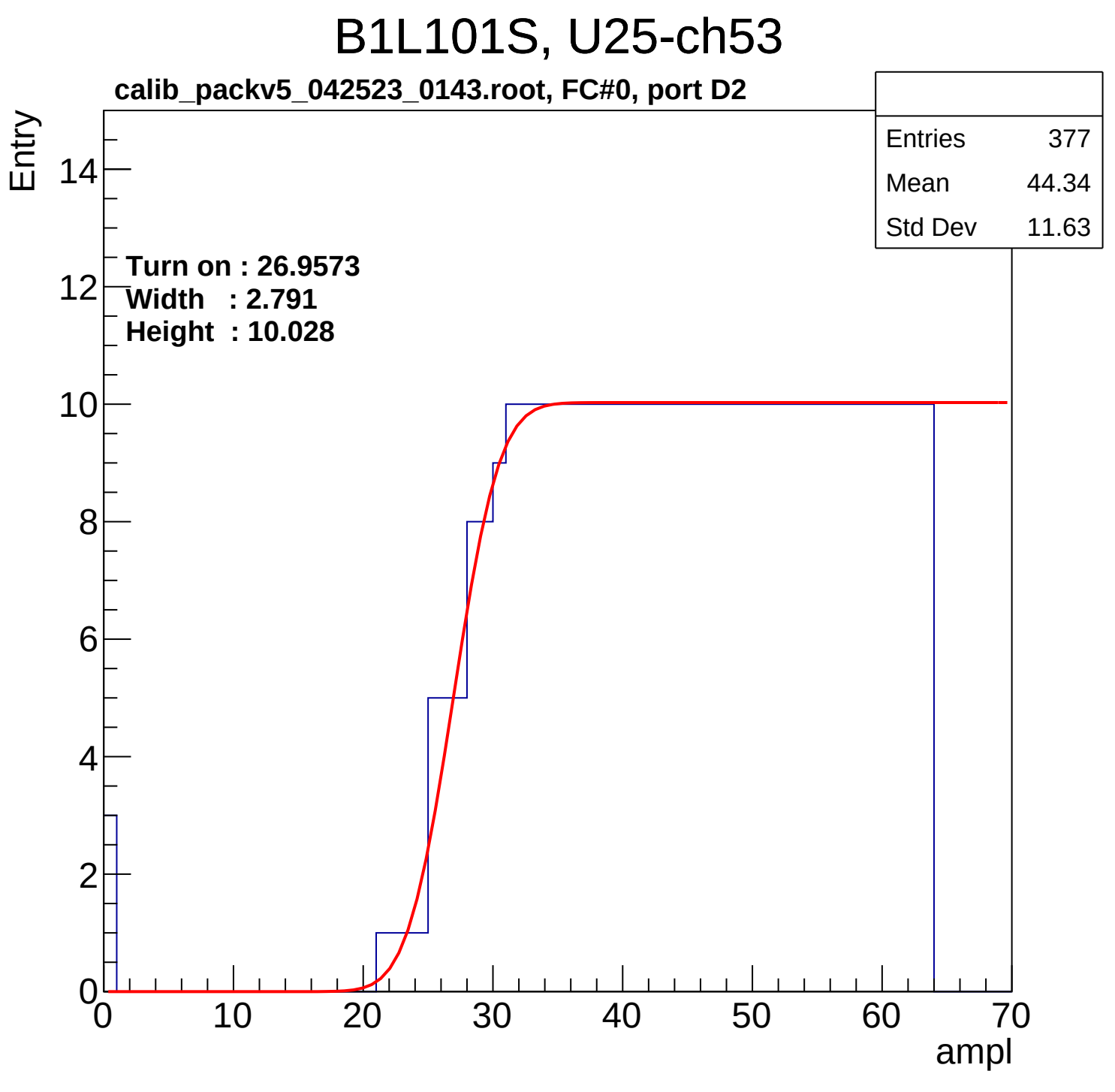
B1L101S, U25-ch53
calib_packv5_042523_0143.root, FC#0, port D2
Entries 377
Mean 44.34
Std Dev 11.63
Turn on : 26.9573
Width : 2.791
Height : 10.028
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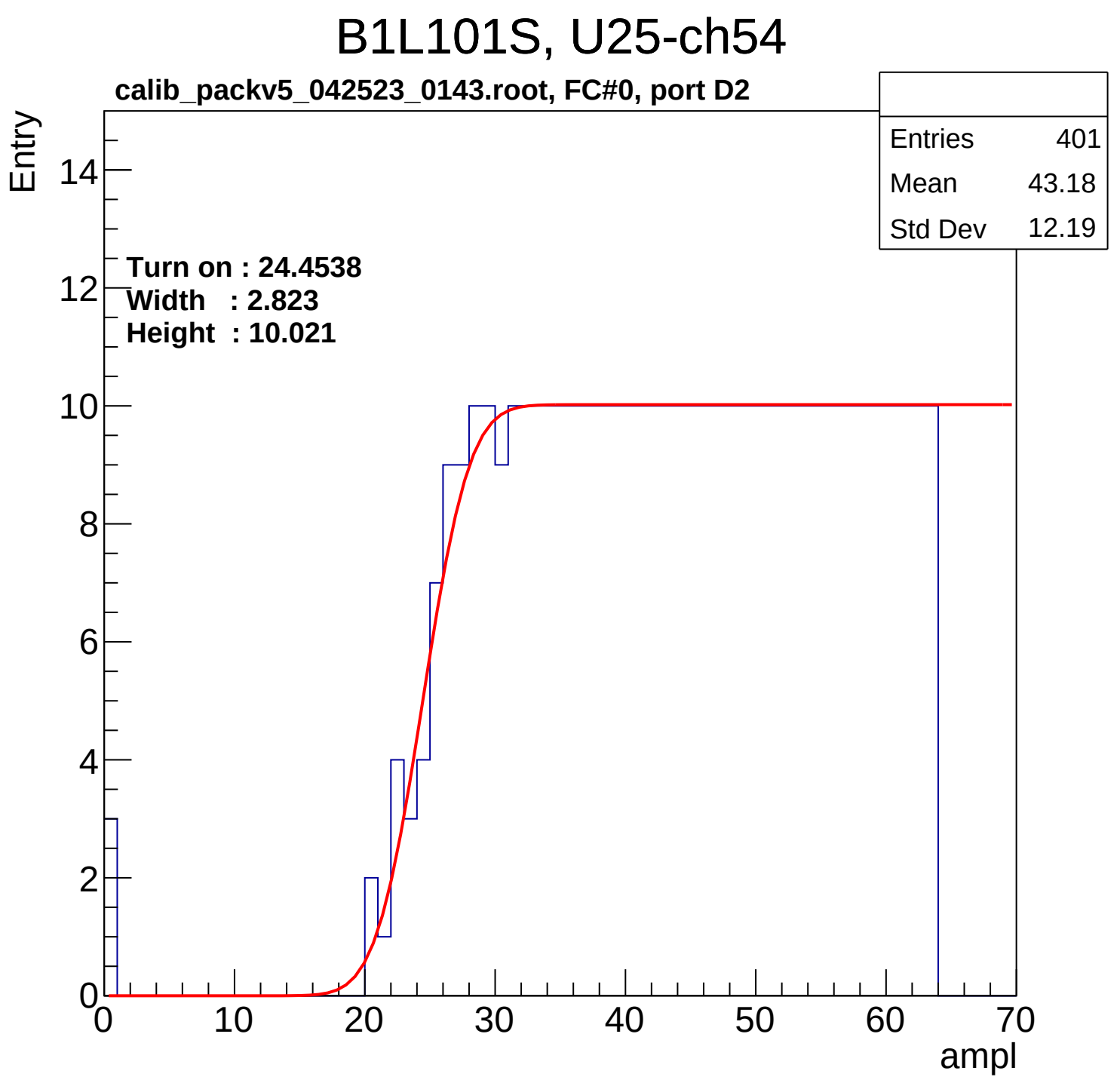
B1L101S, U25-ch54
calib_packv5_042523_0143.root, FC#0, port D2
Entries 401
Mean 43.18
Std Dev 12.19
Turn on : 24.4538
Width : 2.823
Height : 10.021
Entry
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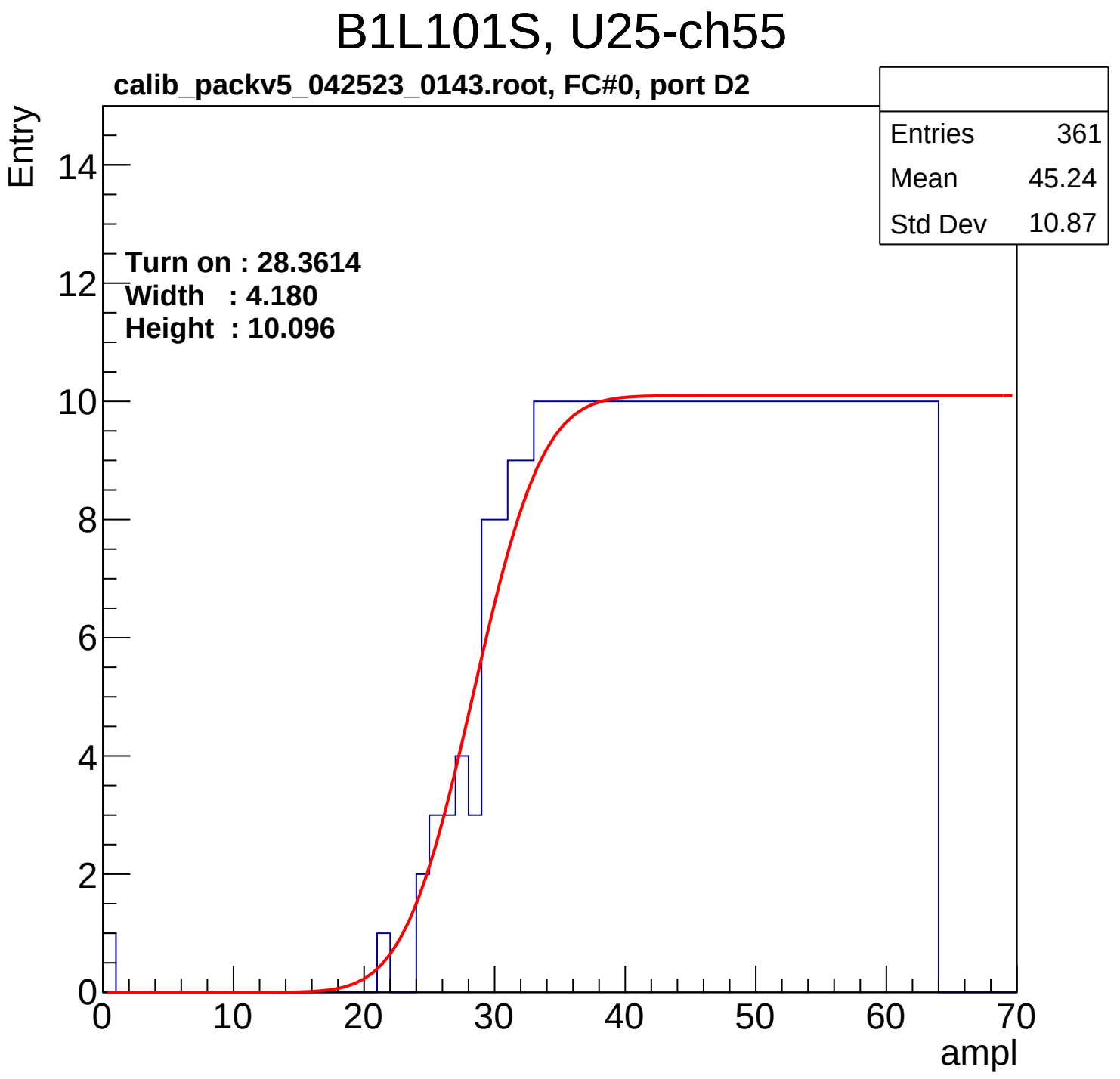
B1L101S, U25-ch55
calib_packv5_042523_0143.root, FC#0, port D2
Entries 361
Mean 45.24
Std Dev 10.87
Turn on : 28.3614
Width : 4.180
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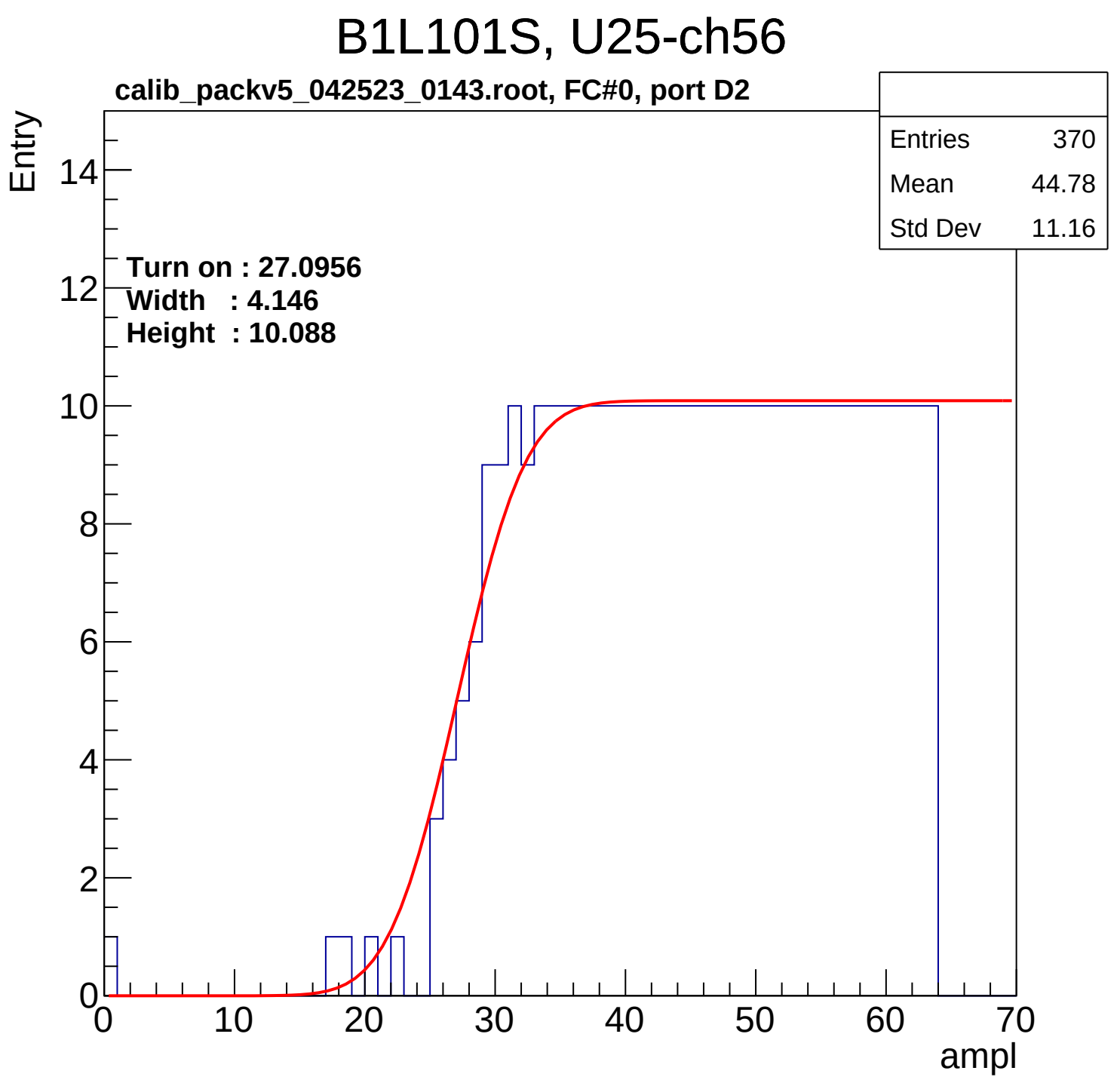
B1L101S, U25-ch56
calib_packv5_042523_0143.root, FC#0, port D2
Entries 370
Mean 44.78
Std Dev 11.16
Turn on : 27.0956
Width : 4.146
Height : 10.088
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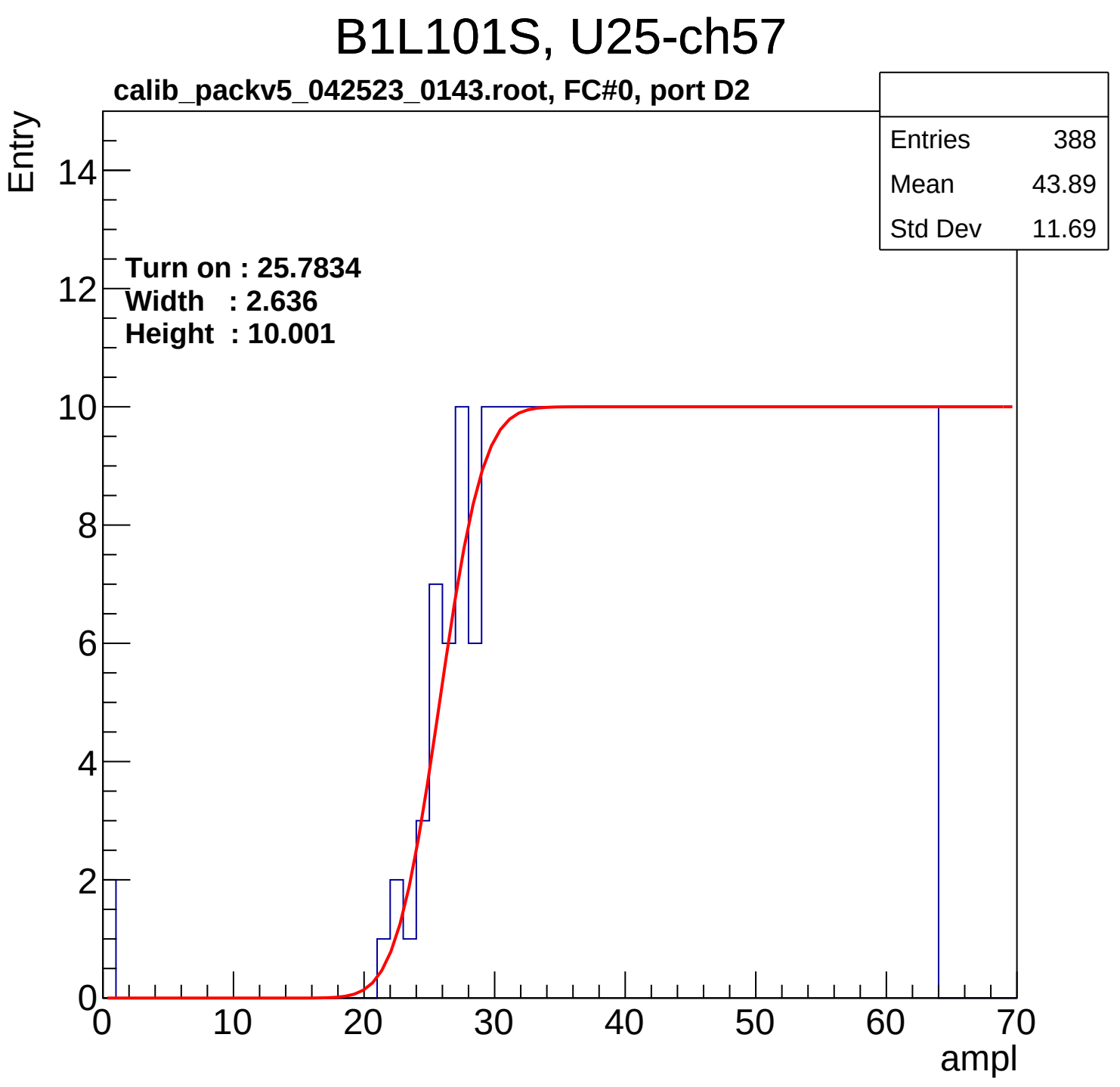
B1L101S, U25-ch57
calib_packv5_042523_0143.root, FC#0, port D2
Entries 388
Mean 43.89
Std Dev 11.69
Turn on : 25.7834
Width : 2.636
Height : 10.001
Entry
ampl
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4
6
8
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12
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10
20
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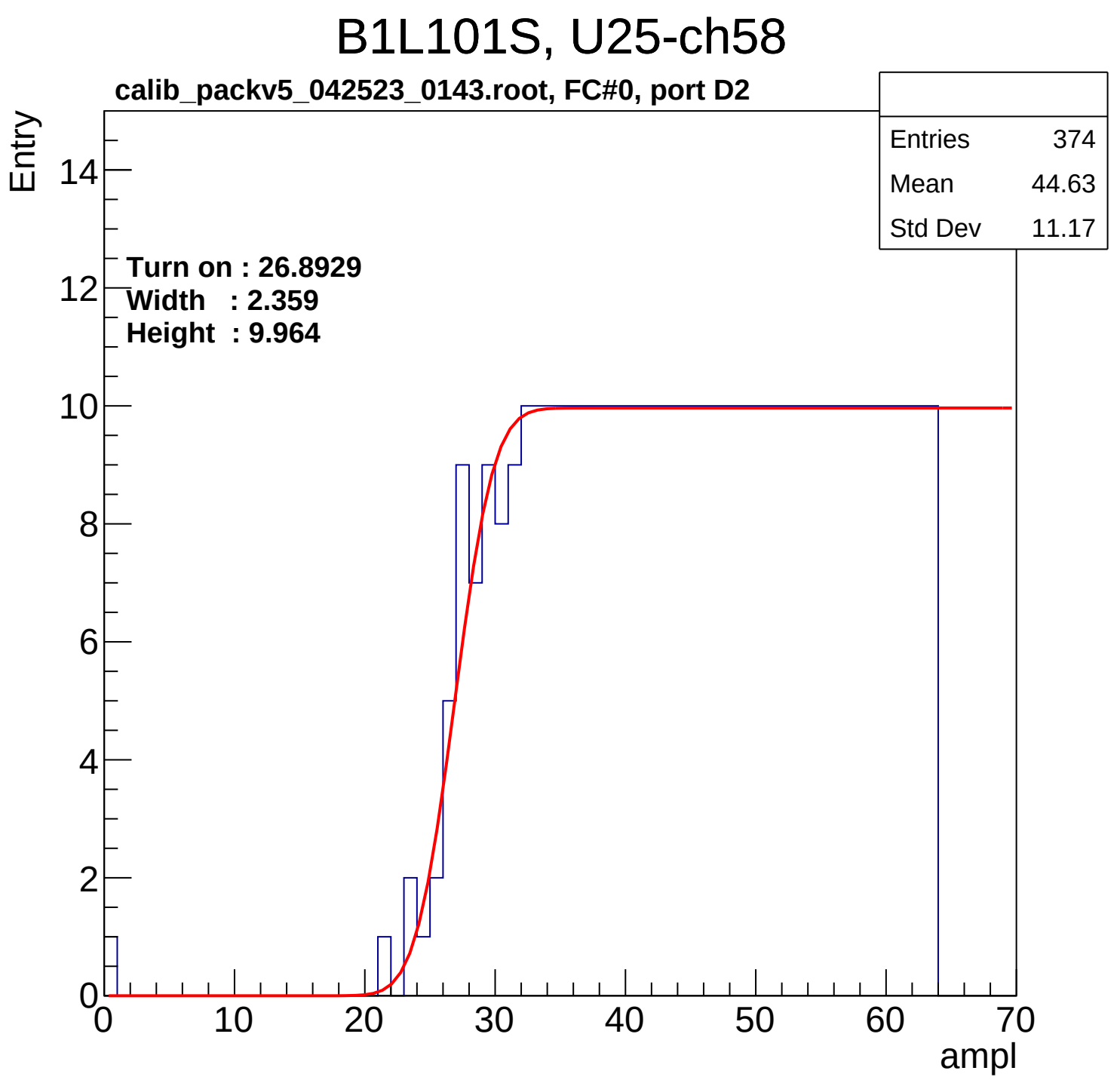
B1L101S, U25-ch58
calib_packv5_042523_0143.root, FC#0, port D2
Entries 374
Mean 44.63
Std Dev 11.17
Turn on : 26.8929
Width : 2.359
Height : 9.964
Entry
ampl
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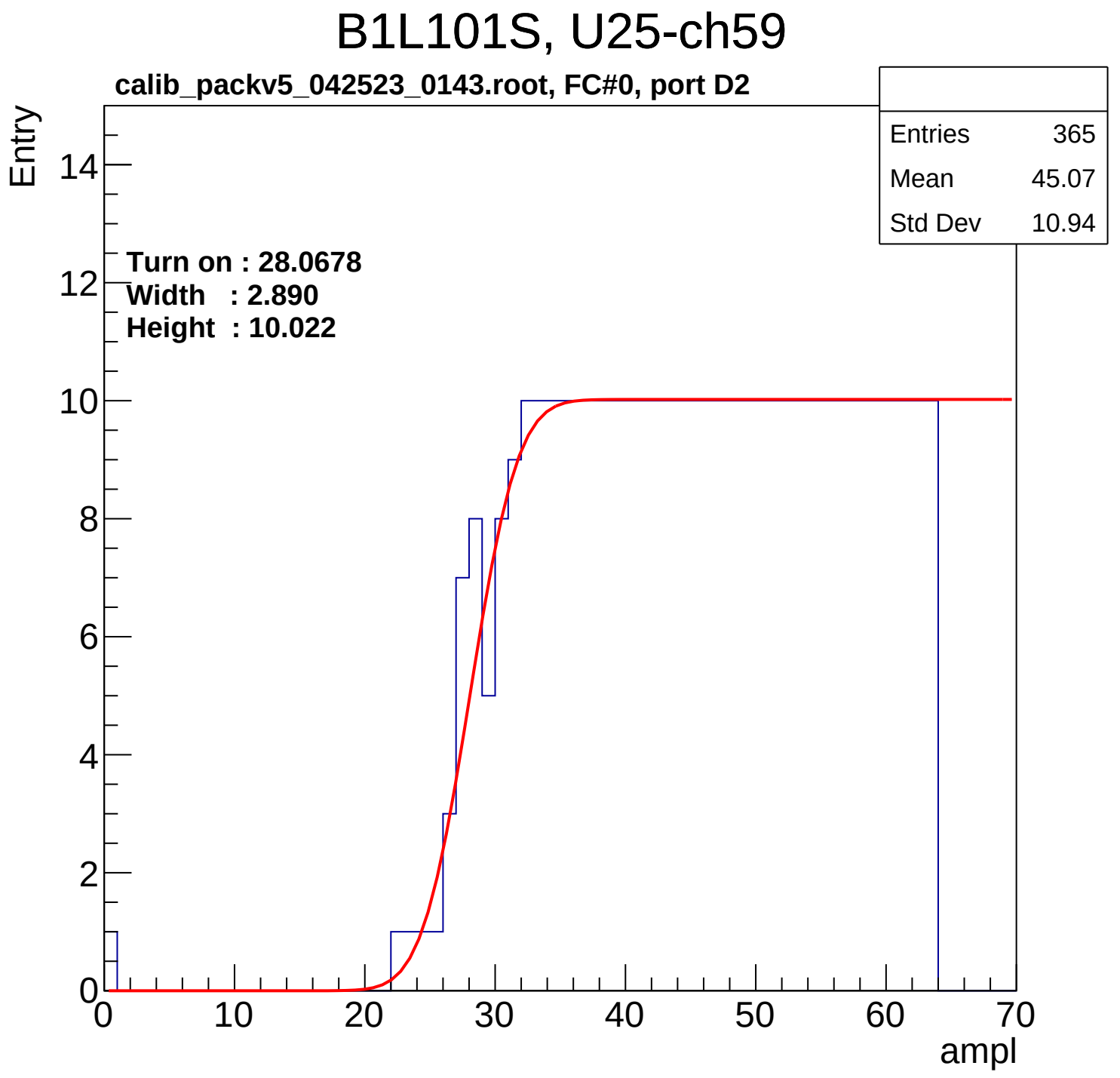
B1L101S, U25-ch59
calib_packv5_042523_0143.root, FC#0, port D2
Entries 365
Mean 45.07
Std Dev 10.94
Turn on : 28.0678
Width : 2.890
Height : 10.022
Entry
ampl
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2
4
6
8
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0
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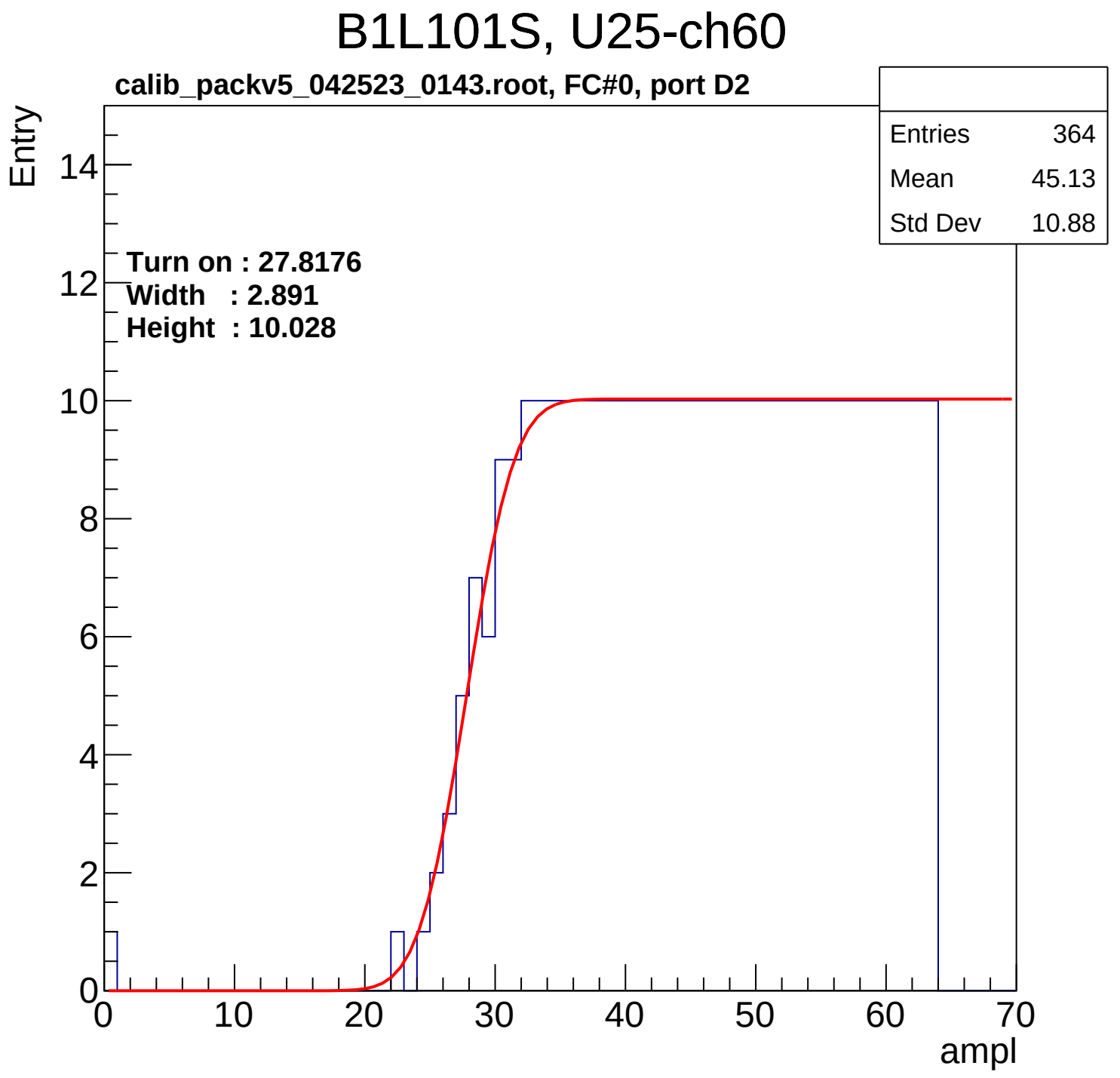
B1L101S, U25-ch60
calib_packv5_042523_0143.root, FC#0, port D2
Entries 364
Mean 45.13
Std Dev 10.88
Turn on : 27.8176
Width : 2.891
Height : 10.028
Entry
ampl
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2
4
6
8
10
12
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40
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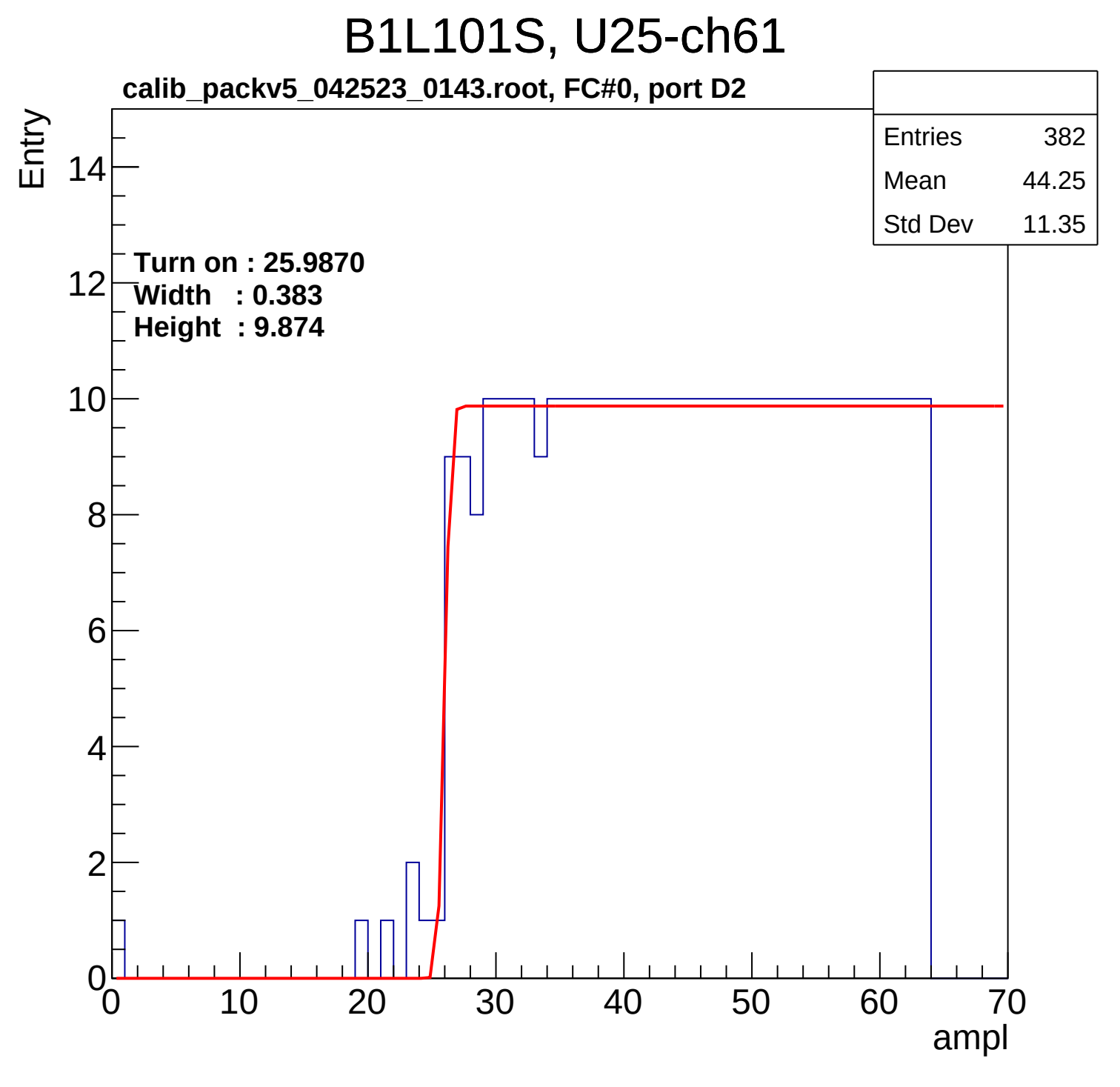
B1L101S, U25-ch61
calib_packv5_042523_0143.root, FC#0, port D2
Entries 382
Mean 44.25
Std Dev 11.35
Turn on : 25.9870
Width : 0.383
Height : 9.874
Entry
ampl
0
2
4
6
8
10
12
14
0
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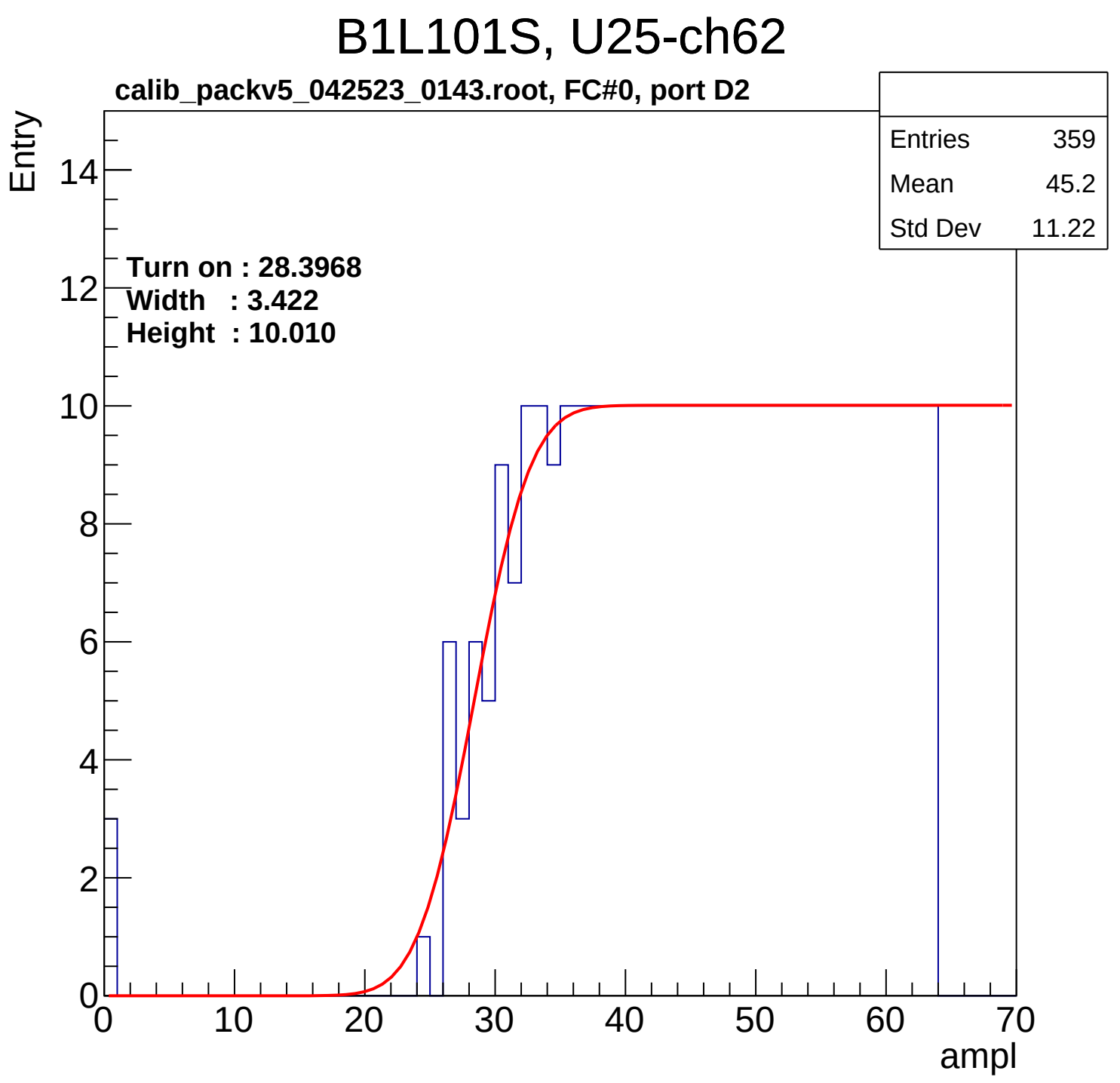
B1L101S, U25-ch62
calib_packv5_042523_0143.root, FC#0, port D2
Entries 359
Mean 45.2
Std Dev 11.22
Turn on : 28.3968
Width : 3.422
Height : 10.010
Entry
ampl
0
2
4
6
8
10
12
14
0
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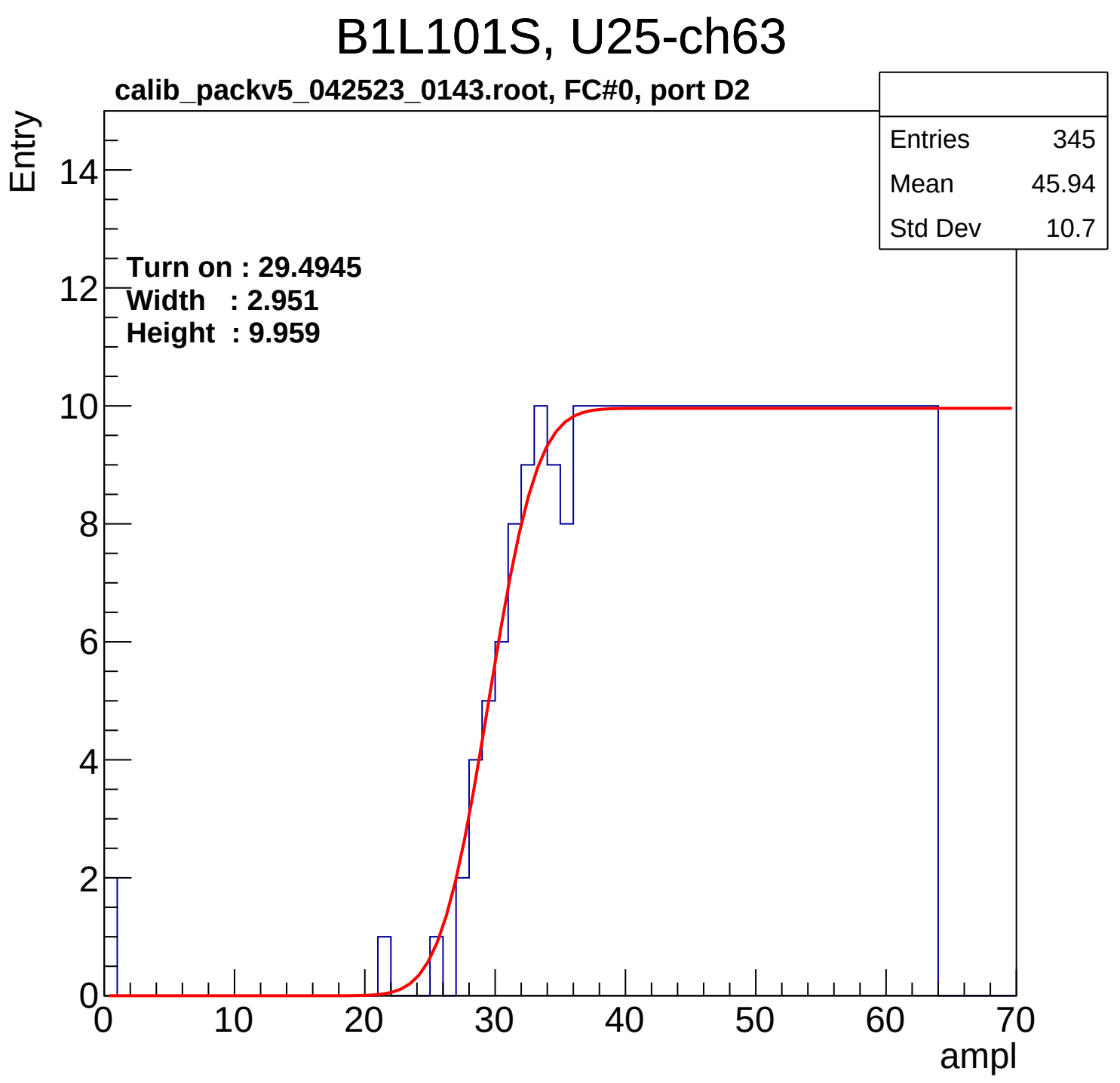
B1L101S, U25-ch63
calib_packv5_042523_0143.root, FC#0, port D2
Entries 345
Mean 45.94
Std Dev 10.7
Turn on : 29.4945
Width : 2.951
Height : 9.959
Entry
ampl
0
2
4
6
8
10
12
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0
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20
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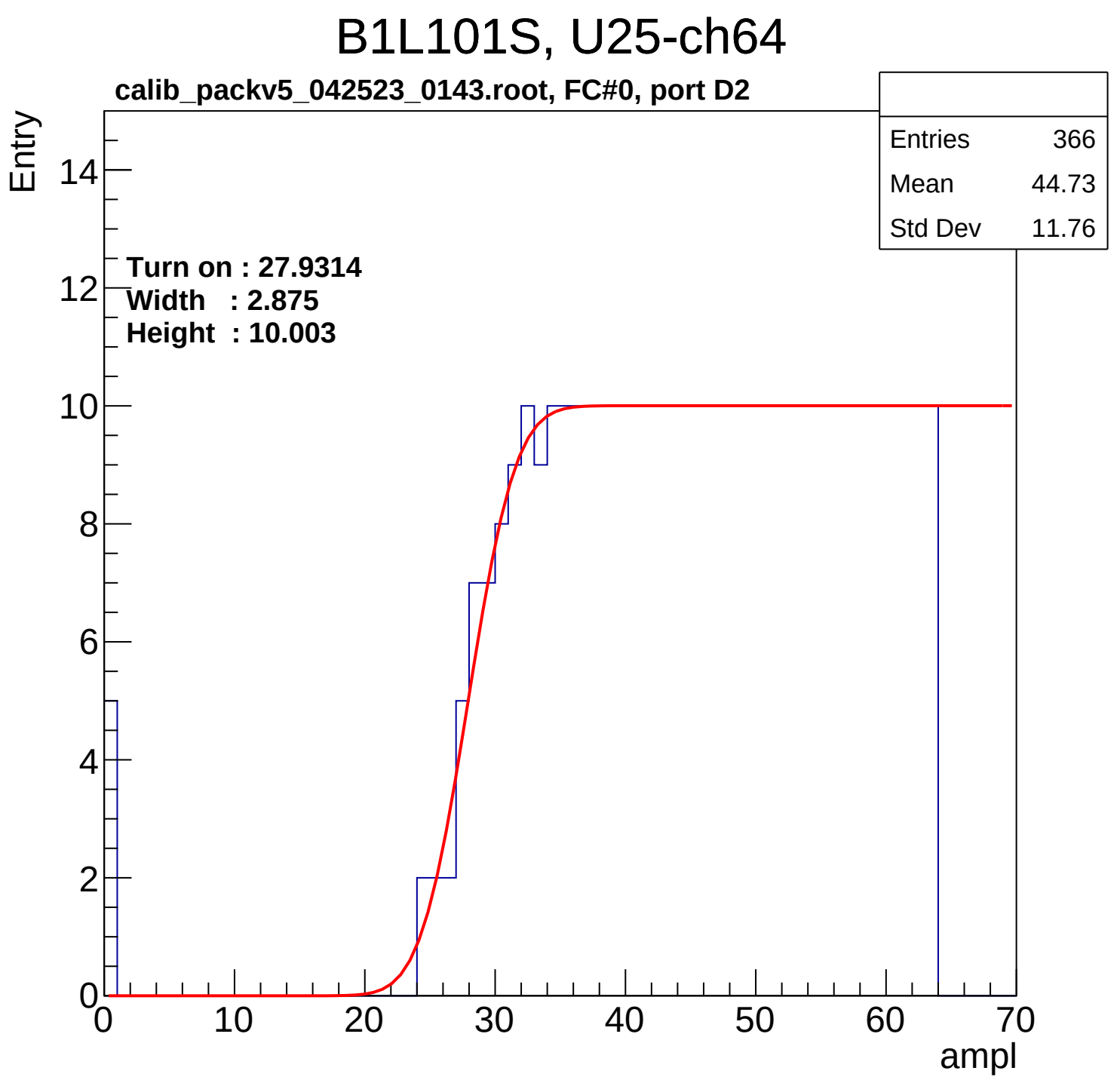
B1L101S, U25-ch64
calib_packv5_042523_0143.root, FC#0, port D2
Entries 366
Mean 44.73
Std Dev 11.76
Turn on : 27.9314
Width : 2.875
Height : 10.003
Entry
ampl
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2
4
6
8
10
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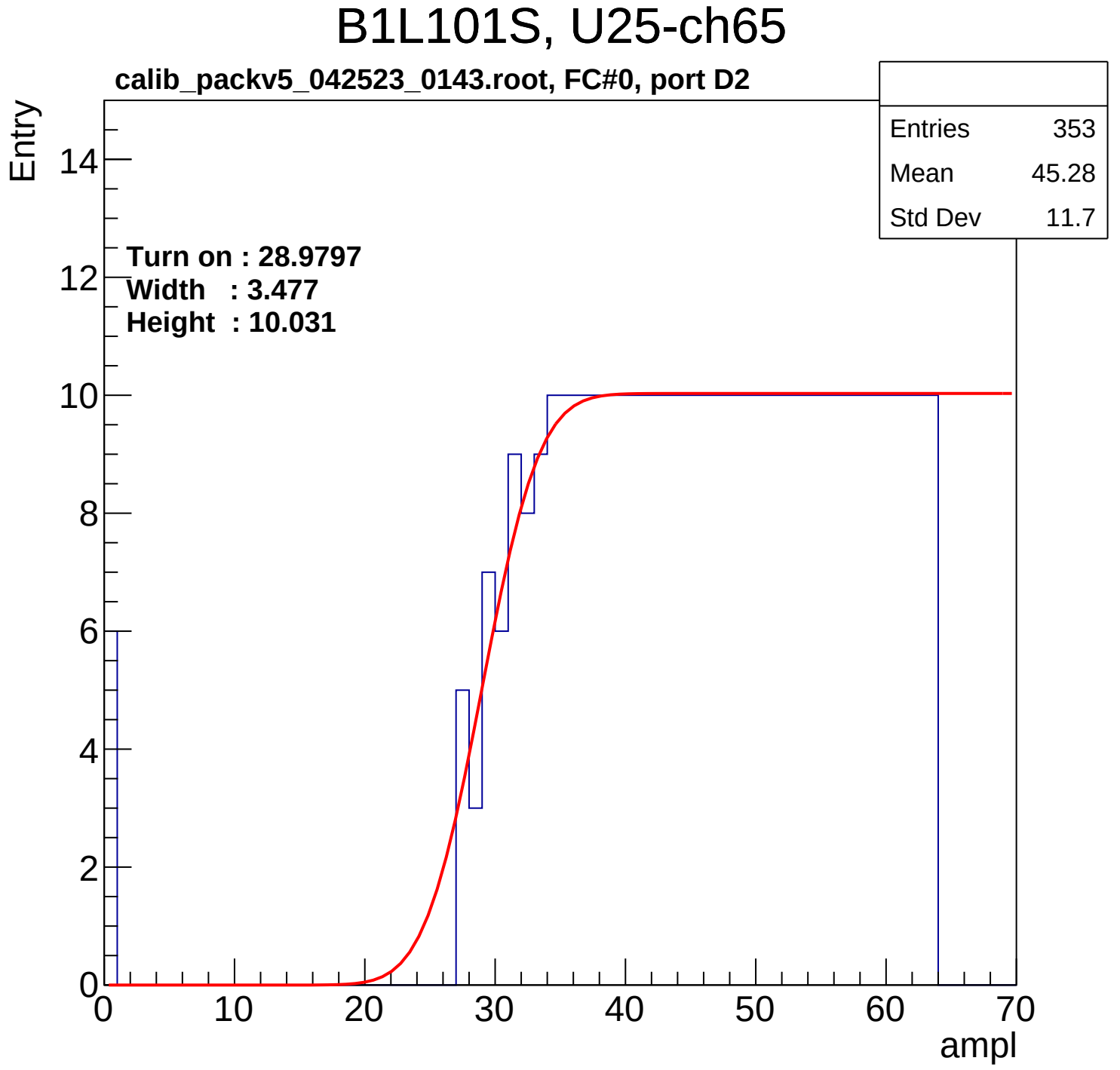
B1L101S, U25-ch65
calib_packv5_042523_0143.root, FC#0, port D2
Entries 353
Mean 45.28
Std Dev 11.7
Turn on : 28.9797
Width : 3.477
Height : 10.031
Entry
ampl
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2
4
6
8
10
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0
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60
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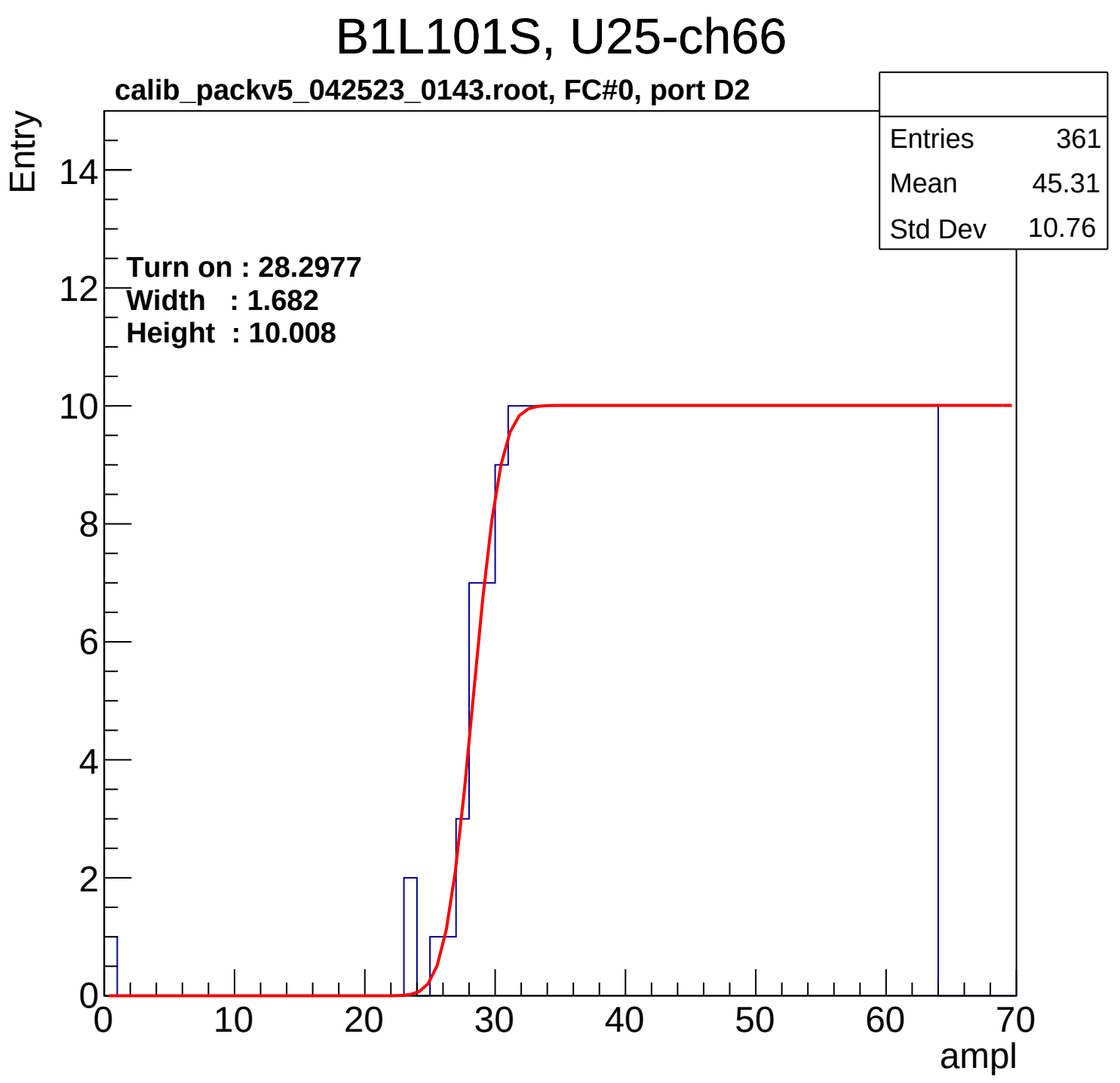
B1L101S, U25-ch66
calib_packv5_042523_0143.root, FC#0, port D2
Entries 361
Mean 45.31
Std Dev 10.76
Turn on : 28.2977
Width : 1.682
Height : 10.008
Entry
ampl
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2
4
6
8
10
12
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0
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60
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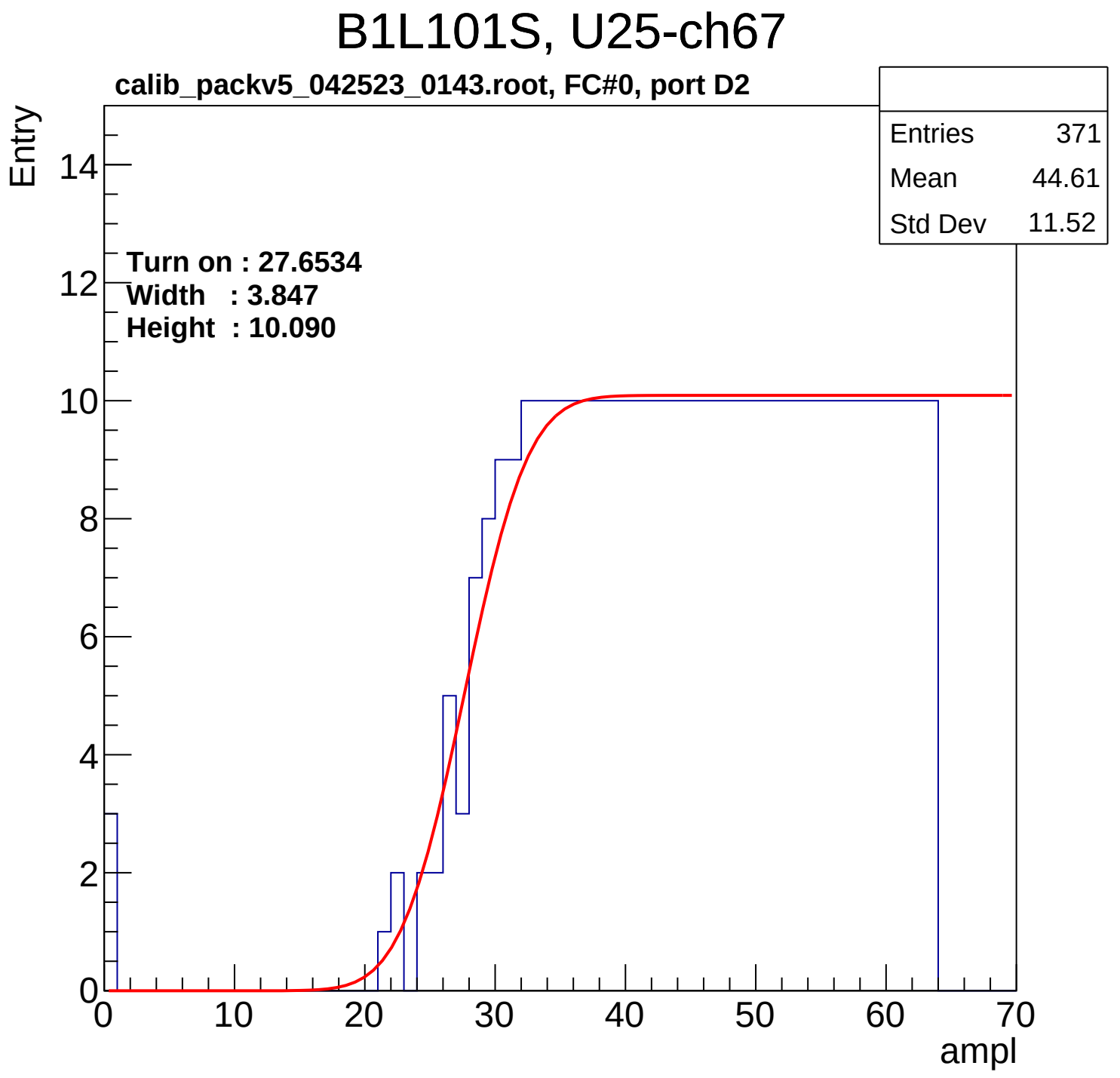
B1L101S, U25-ch67
calib_packv5_042523_0143.root, FC#0, port D2
Entries 371
Mean 44.61
Std Dev 11.52
Turn on : 27.6534
Width : 3.847
Height : 10.090
Entry
ampl
0
2
4
6
8
10
12
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0
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60
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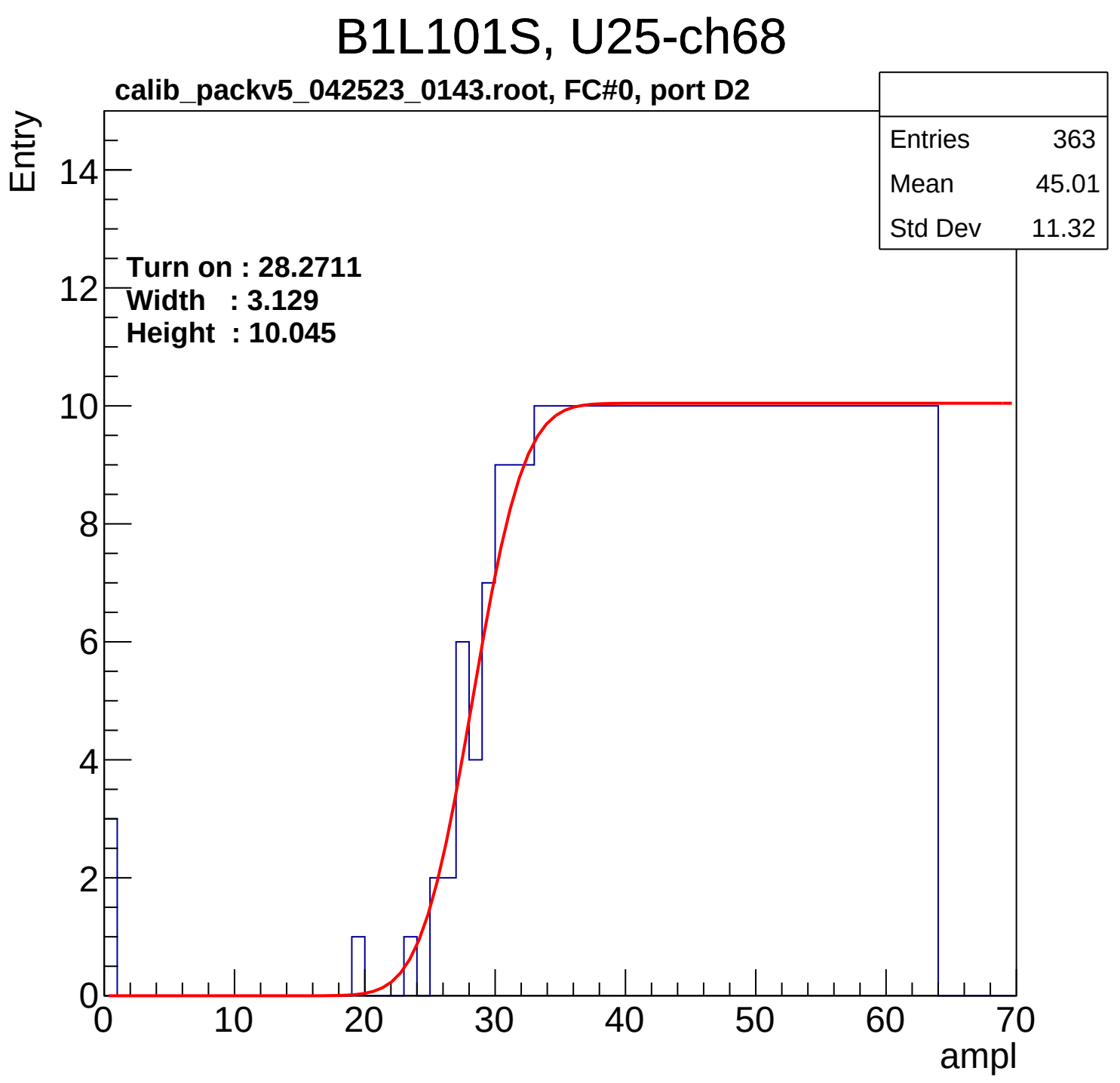
B1L101S, U25-ch68
calib_packv5_042523_0143.root, FC#0, port D2
Entries 363
Mean 45.01
Std Dev 11.32
Turn on : 28.2711
Width : 3.129
Height : 10.045
Entry
ampl
0
2
4
6
8
10
12
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0
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60
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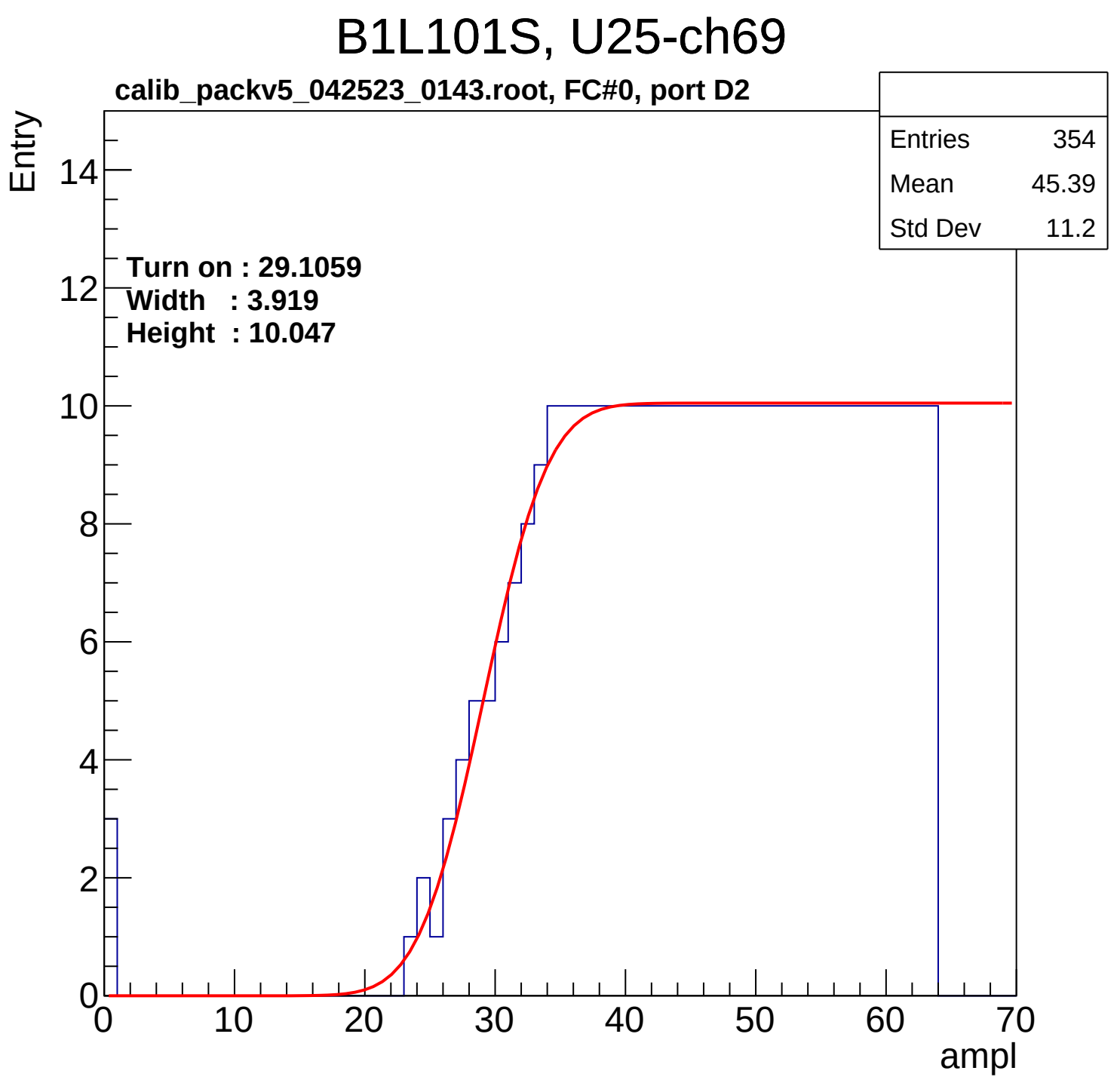
B1L101S, U25-ch69
calib_packv5_042523_0143.root, FC#0, port D2
Entries 354
Mean 45.39
Std Dev 11.2
Turn on : 29.1059
Width : 3.919
Height : 10.047
Entry
ampl
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2
4
6
8
10
12
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0
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20
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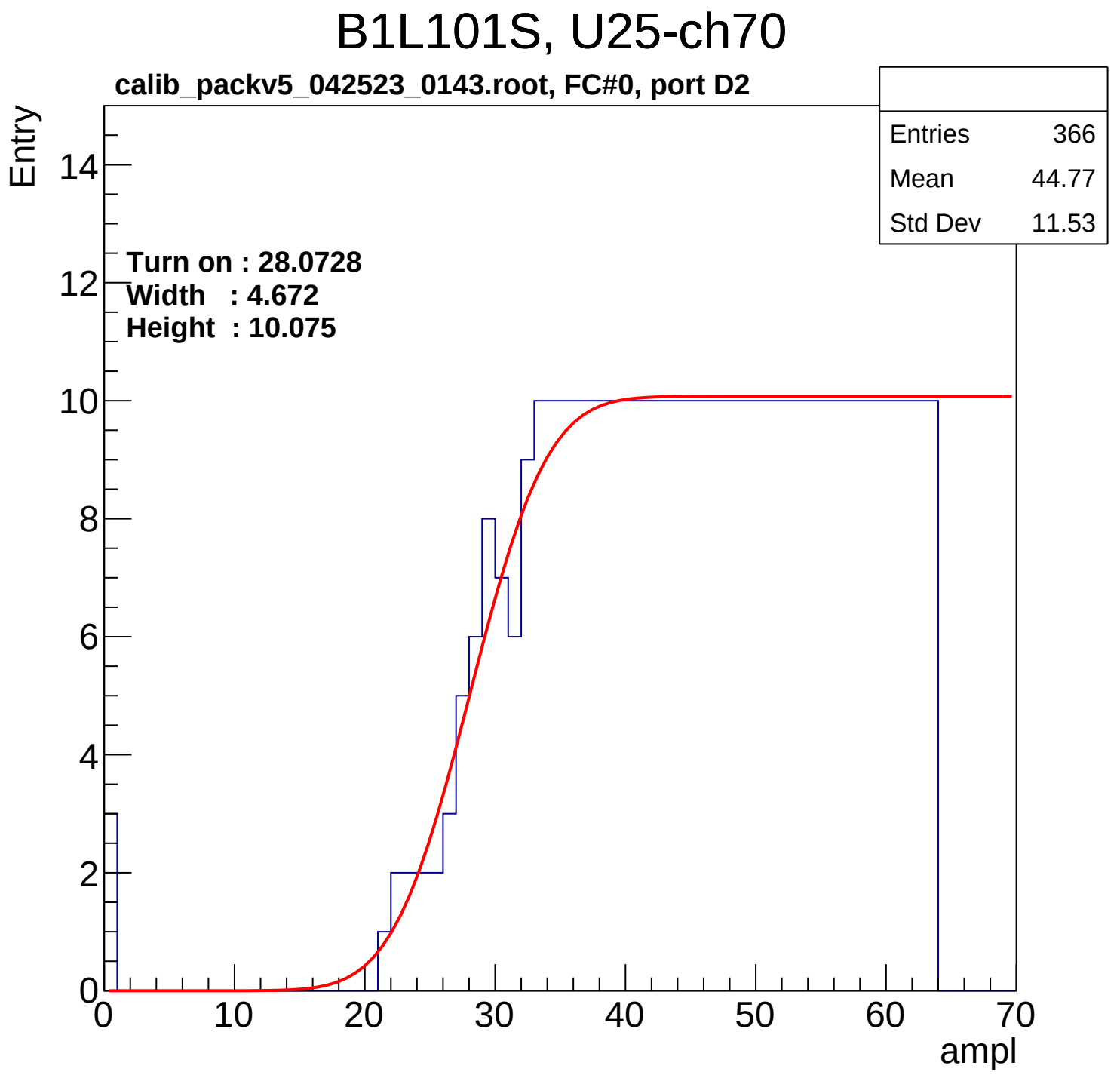
B1L101S, U25-ch70
calib_packv5_042523_0143.root, FC#0, port D2
Entries 366
Mean 44.77
Std Dev 11.53
Turn on : 28.0728
Width : 4.672
Height : 10.075
Entry
ampl
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6
8
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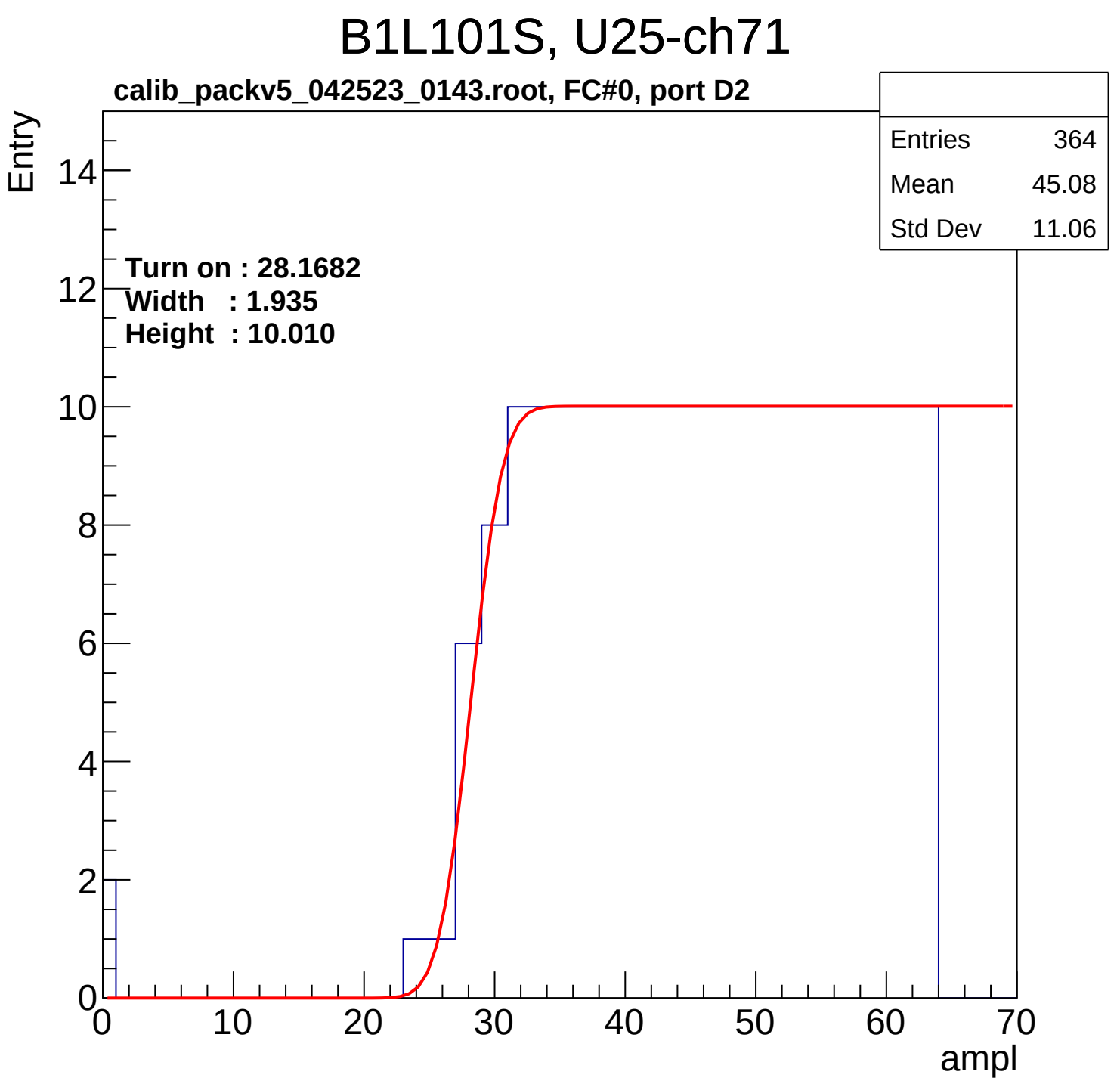
B1L101S, U25-ch71
calib_packv5_042523_0143.root, FC#0, port D2
Entries 364
Mean 45.08
Std Dev 11.06
Turn on : 28.1682
Width : 1.935
Height : 10.010
Entry
ampl
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2
4
6
8
10
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0
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20
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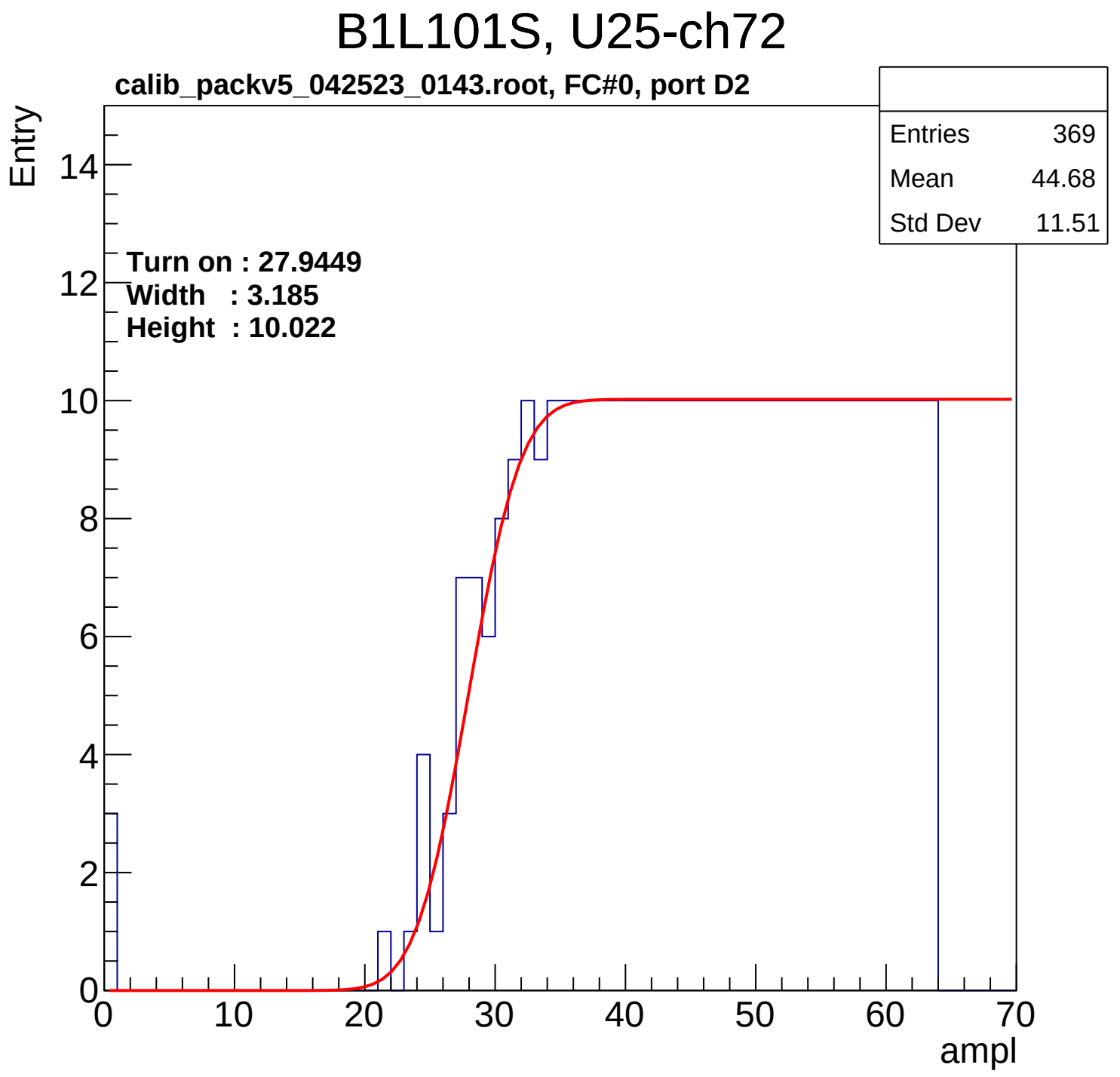
B1L101S, U25-ch72
calib_packv5_042523_0143.root, FC#0, port D2
Entries 369
Mean 44.68
Std Dev 11.51
Turn on : 27.9449
Width : 3.185
Height : 10.022
Entry
ampl
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2
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6
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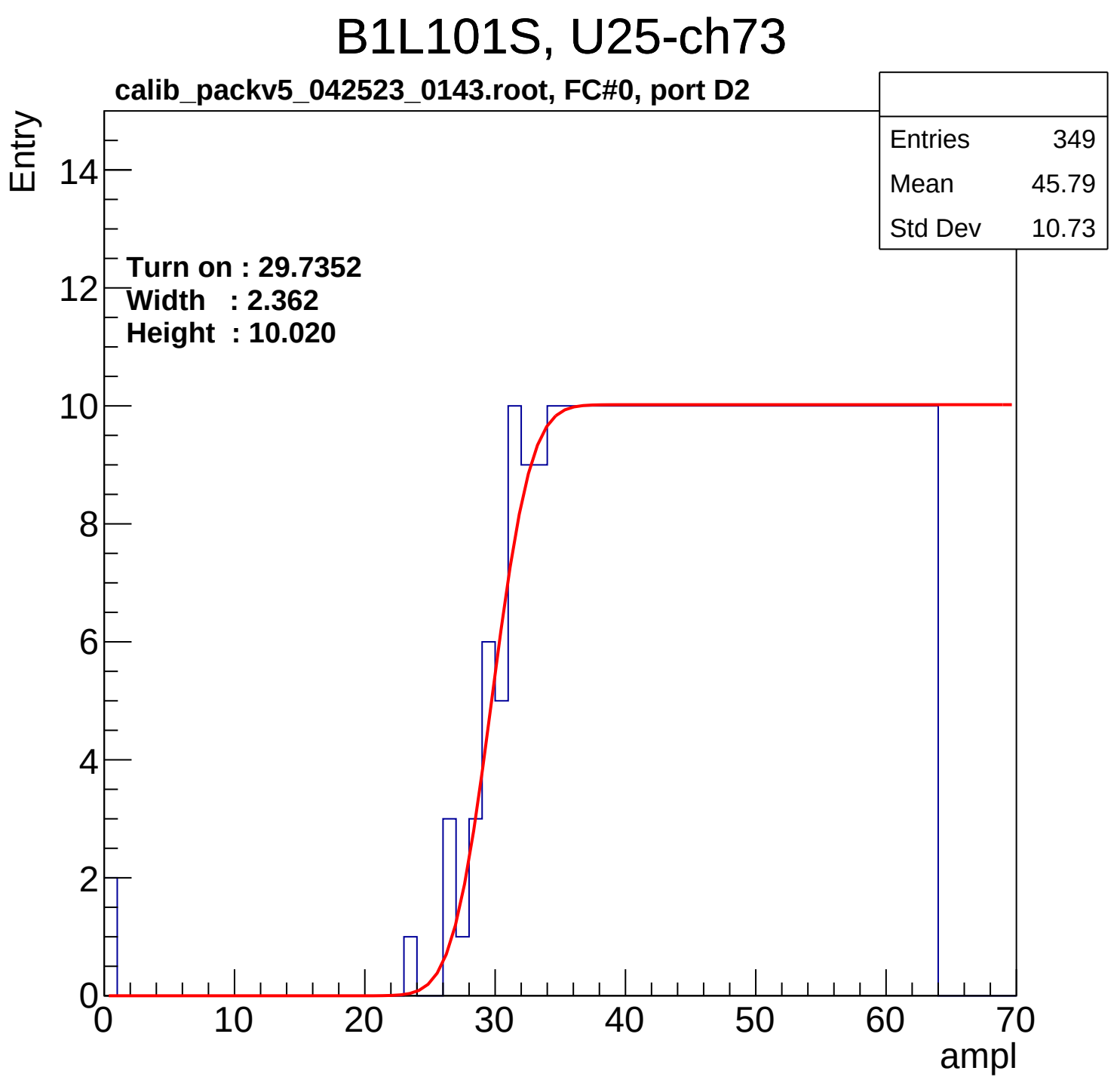
B1L101S, U25-ch73
calib_packv5_042523_0143.root, FC#0, port D2
Entries 349
Mean 45.79
Std Dev 10.73
Turn on : 29.7352
Width : 2.362
Height : 10.020
Entry
ampl
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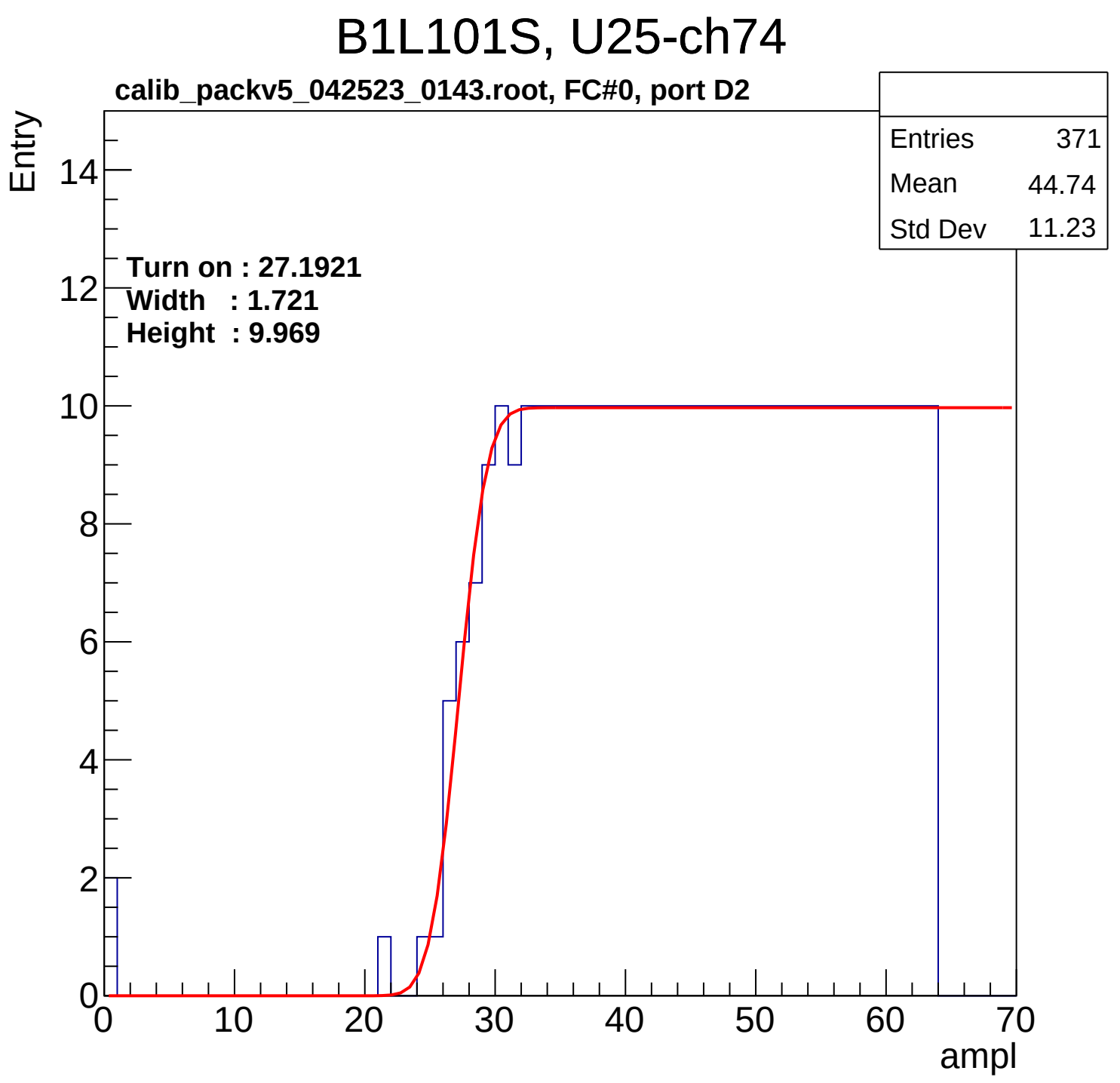
B1L101S, U25-ch74
calib_packv5_042523_0143.root, FC#0, port D2
Entries 371
Mean 44.74
Std Dev 11.23
Turn on : 27.1921
Width : 1.721
Height : 9.969
Entry
ampl
0
2
4
6
8
10
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0
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60
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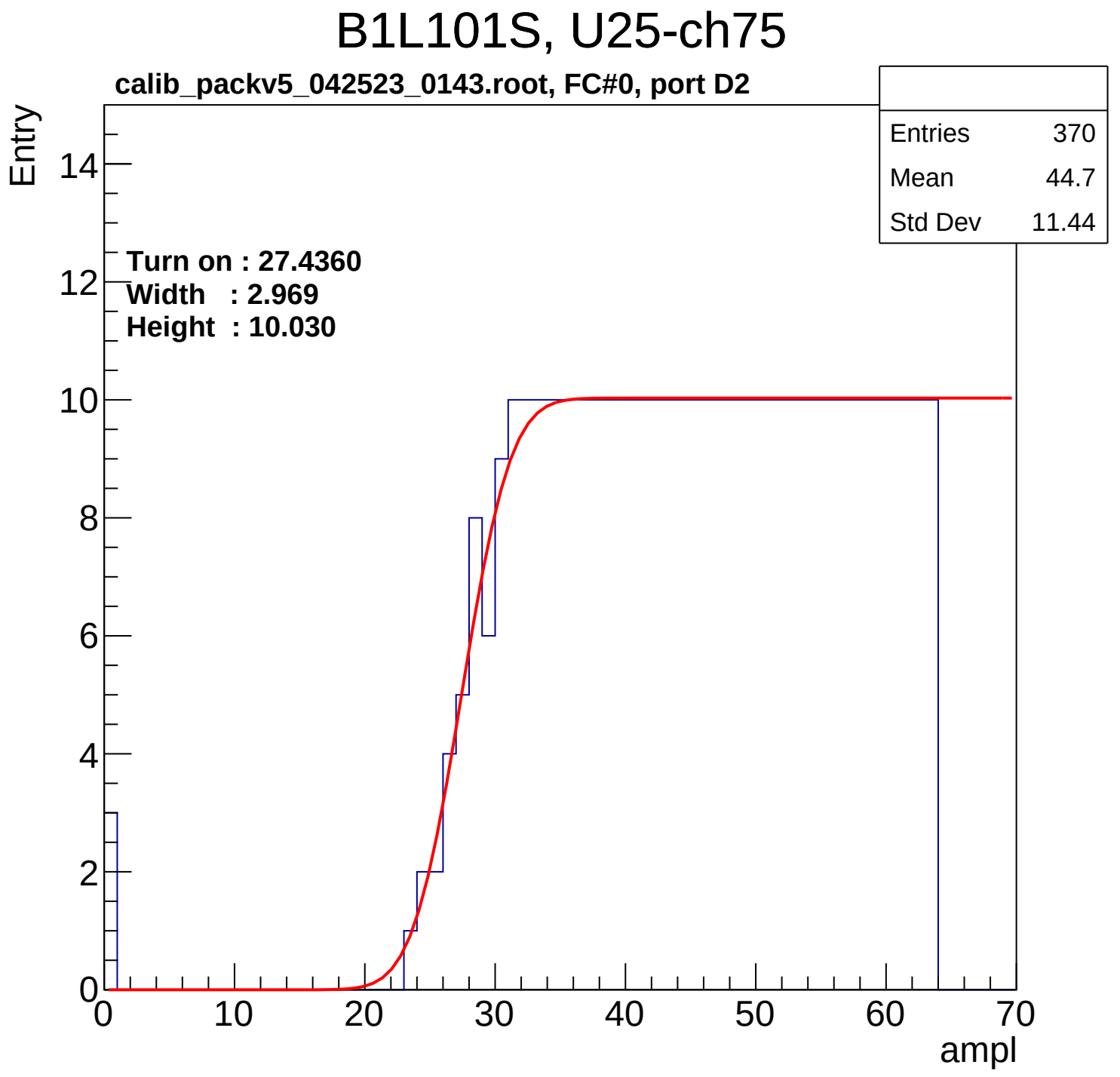
B1L101S, U25-ch75
calib_packv5_042523_0143.root, FC#0, port D2
Entries 370
Mean 44.7
Std Dev 11.44
Turn on : 27.4360
Width : 2.969
Height : 10.030
Entry
ampl
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4
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10
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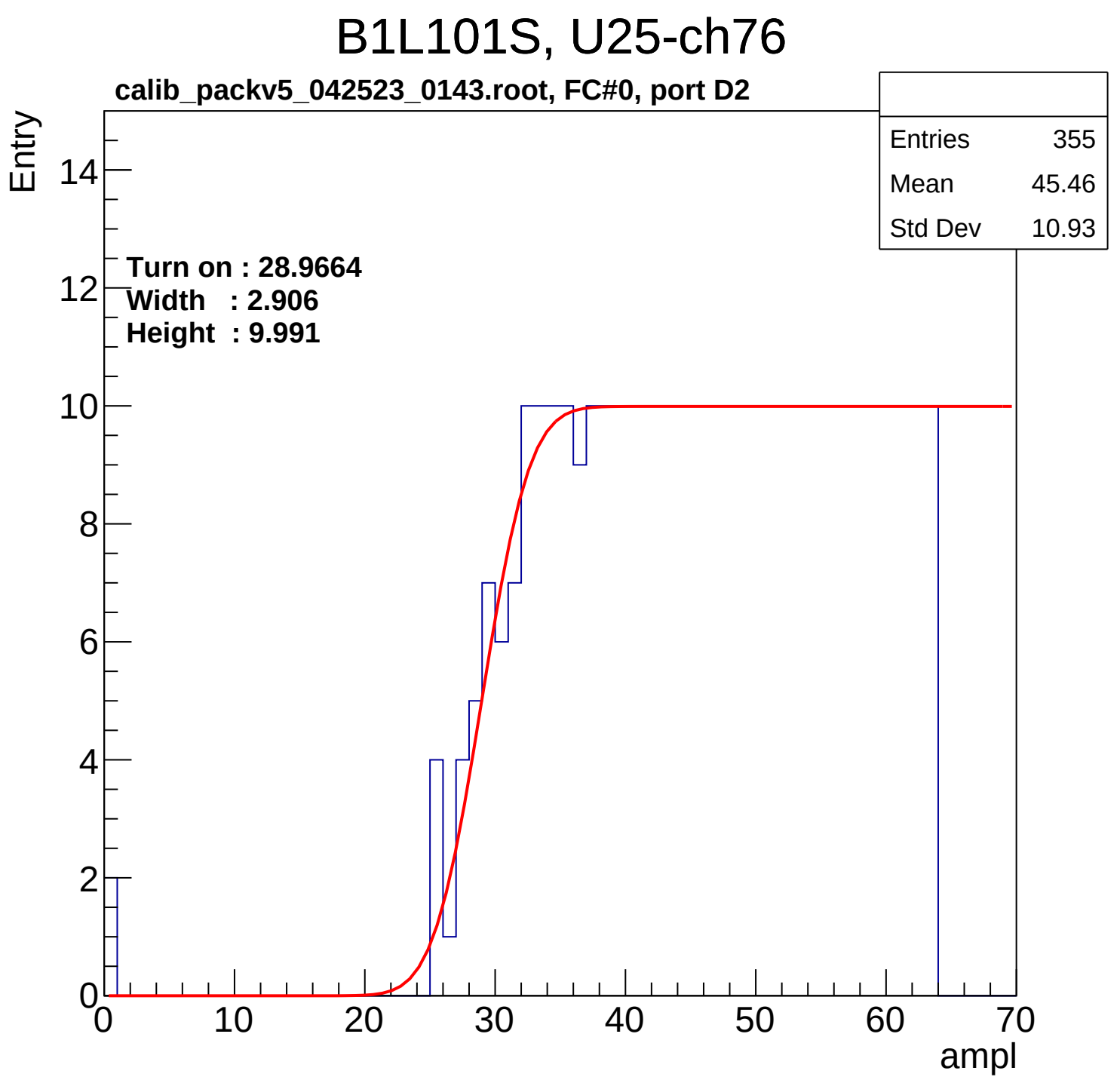
B1L101S, U25-ch76
calib_packv5_042523_0143.root, FC#0, port D2
Entries 355
Mean 45.46
Std Dev 10.93
Turn on : 28.9664
Width : 2.906
Height : 9.991
Entry
ampl
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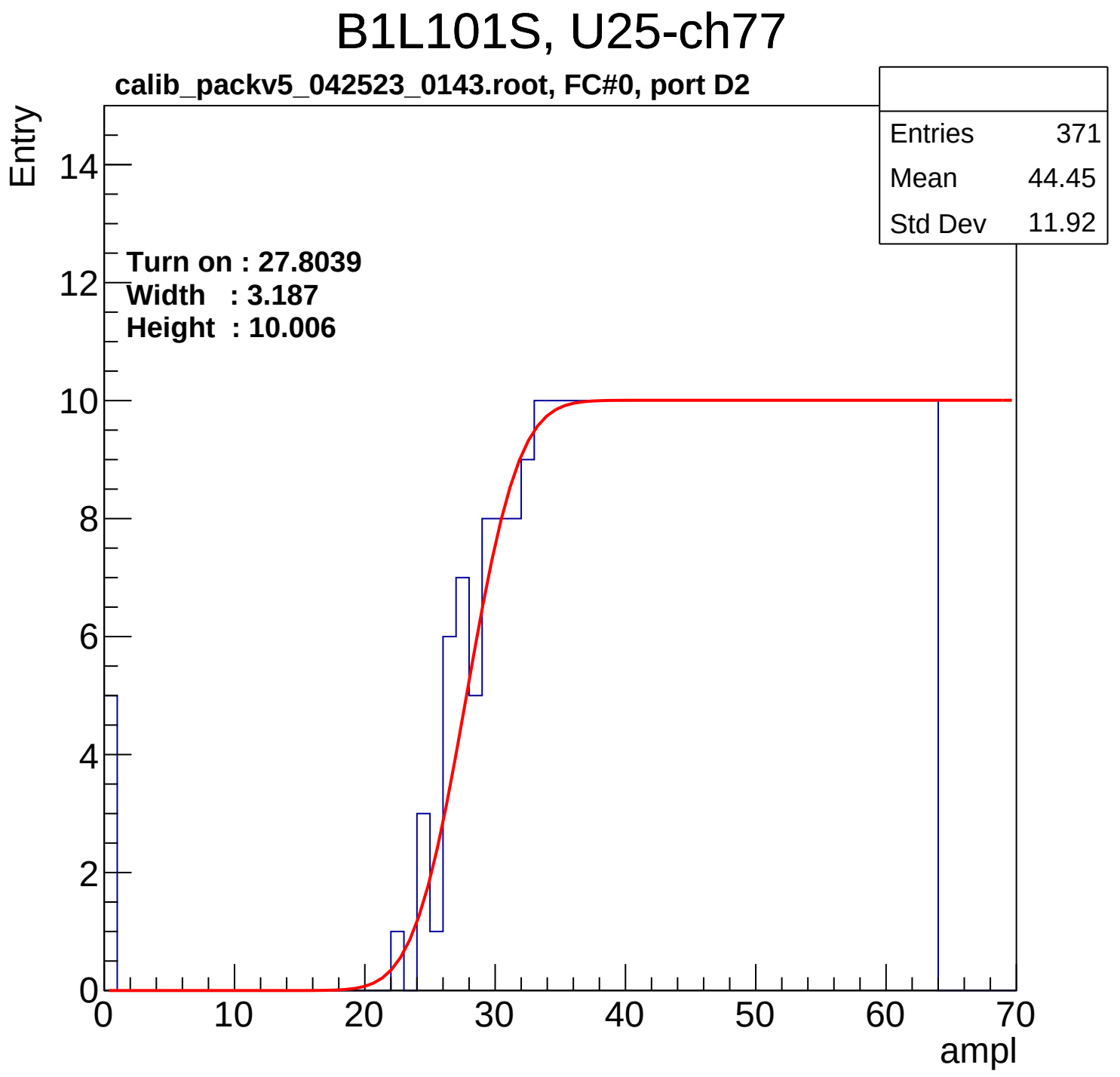
B1L101S, U25-ch77
calib_packv5_042523_0143.root, FC#0, port D2
Entries 371
Mean 44.45
Std Dev 11.92
Turn on : 27.8039
Width : 3.187
Height : 10.006
Entry
ampl
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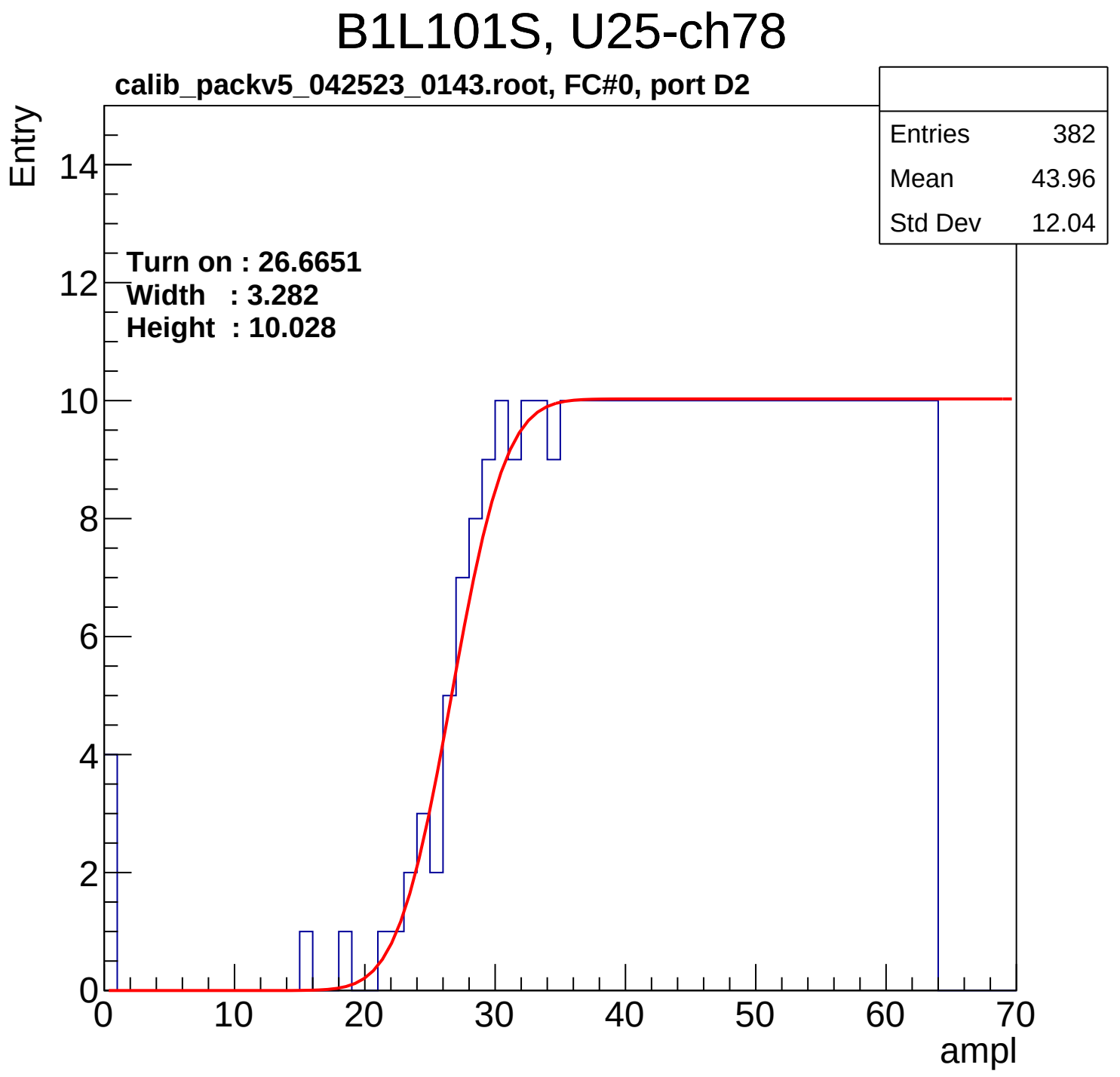
B1L101S, U25-ch78
calib_packv5_042523_0143.root, FC#0, port D2
Entries 382
Mean 43.96
Std Dev 12.04
Turn on : 26.6651
Width : 3.282
Height : 10.028
Entry
ampl
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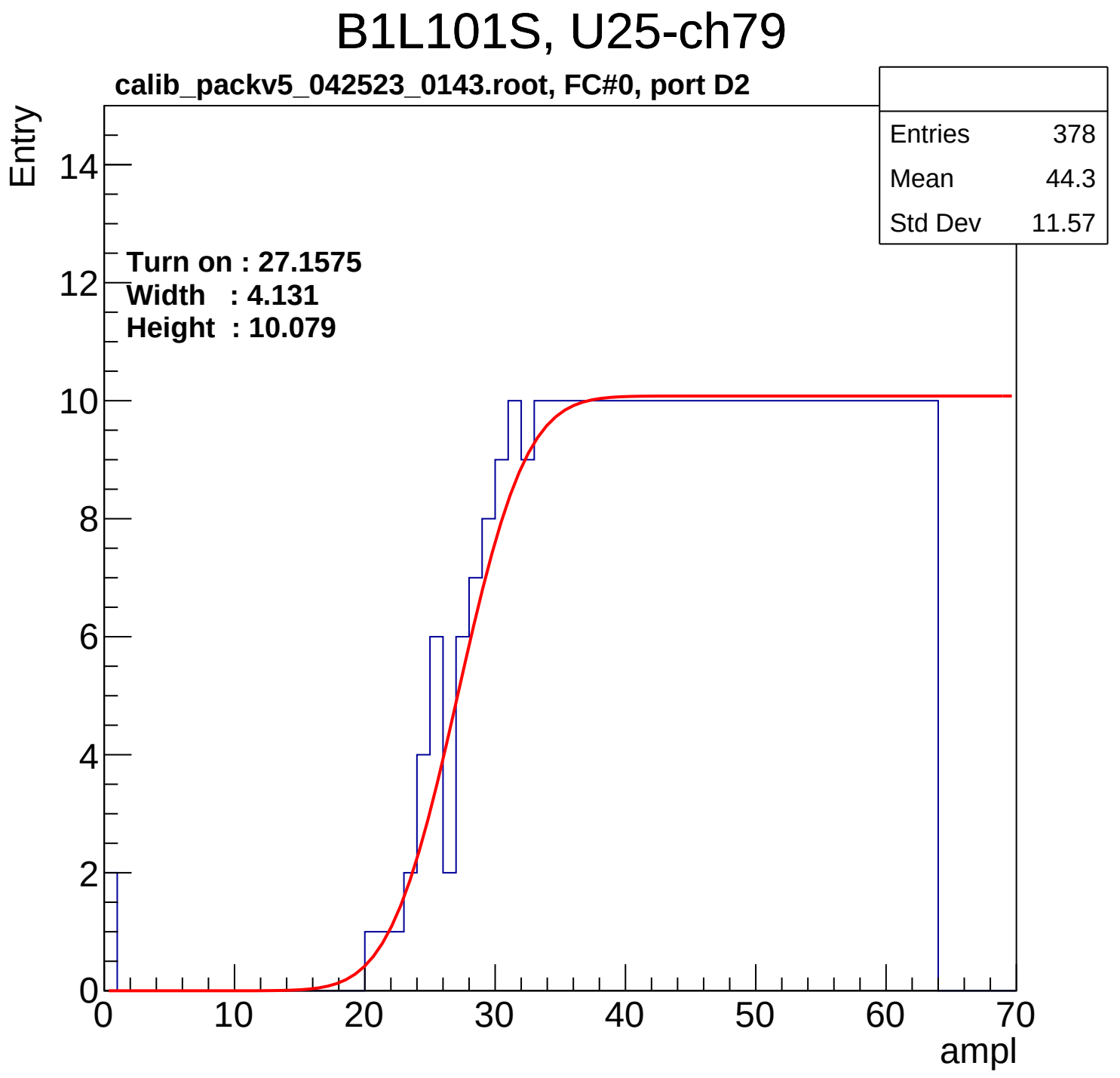
B1L101S, U25-ch79
calib_packv5_042523_0143.root, FC#0, port D2
Entries 378
Mean 44.3
Std Dev 11.57
Turn on : 27.1575
Width : 4.131
Height : 10.079
Entry
ampl
0
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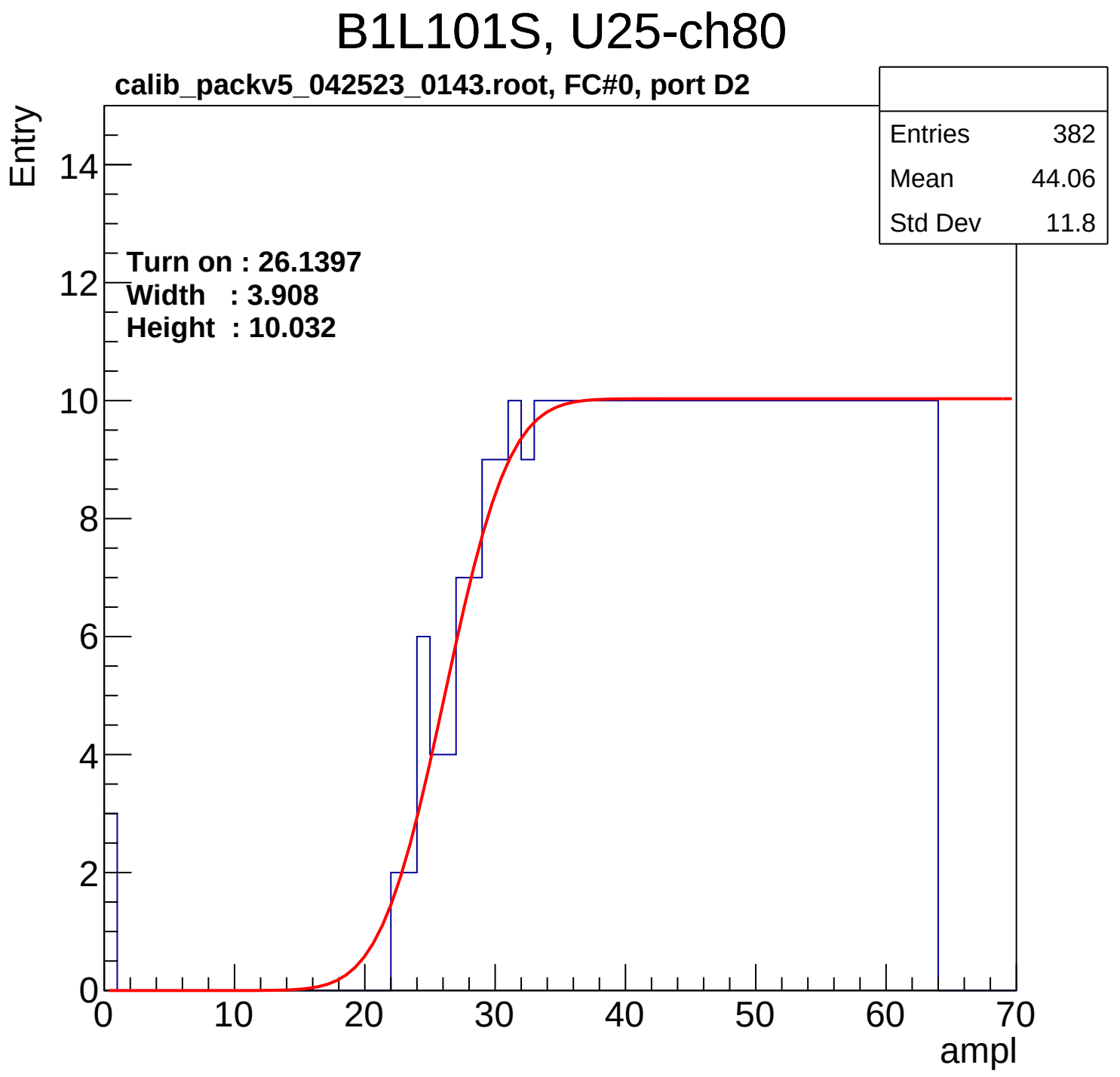
B1L101S, U25-ch80
calib_packv5_042523_0143.root, FC#0, port D2
Entries 382
Mean 44.06
Std Dev 11.8
Turn on : 26.1397
Width : 3.908
Height : 10.032
Entry
ampl
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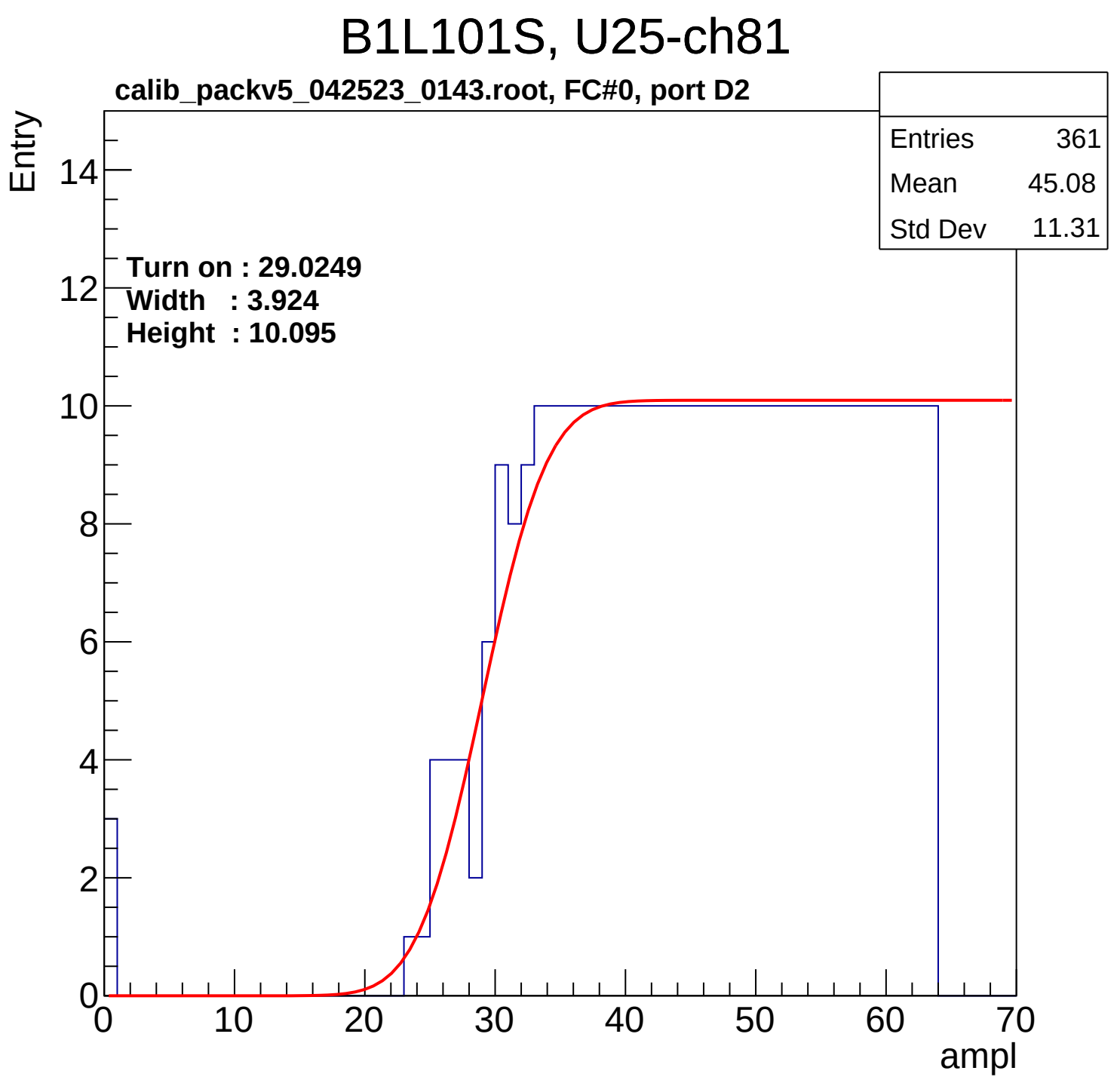
B1L101S, U25-ch81
calib_packv5_042523_0143.root, FC#0, port D2
Entries 361
Mean 45.08
Std Dev 11.31
Turn on : 29.0249
Width : 3.924
Height : 10.095
Entry
ampl
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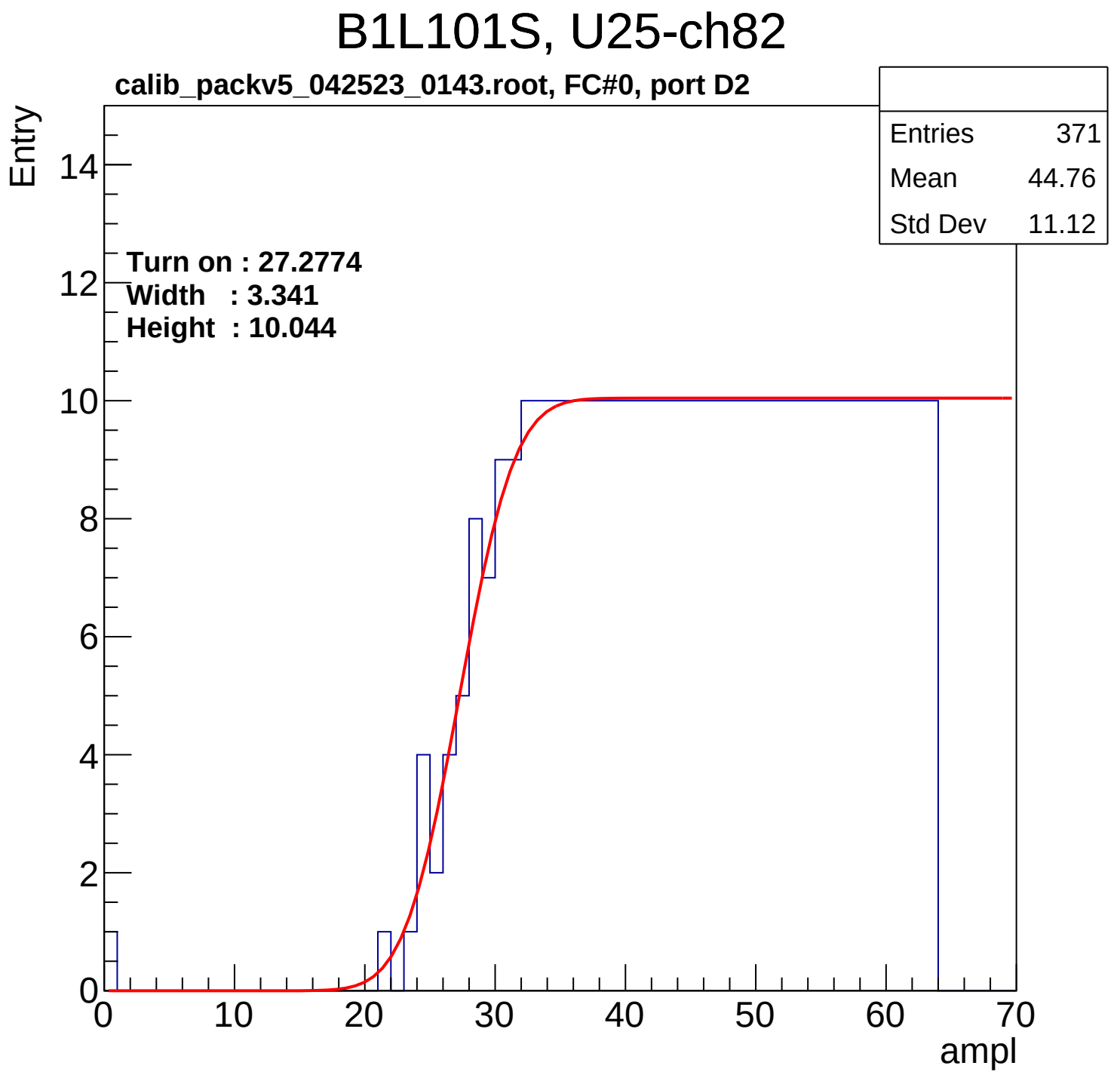
B1L101S, U25-ch82
calib_packv5_042523_0143.root, FC#0, port D2
Entries 371
Mean 44.76
Std Dev 11.12
Turn on : 27.2774
Width : 3.341
Height : 10.044
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ampl
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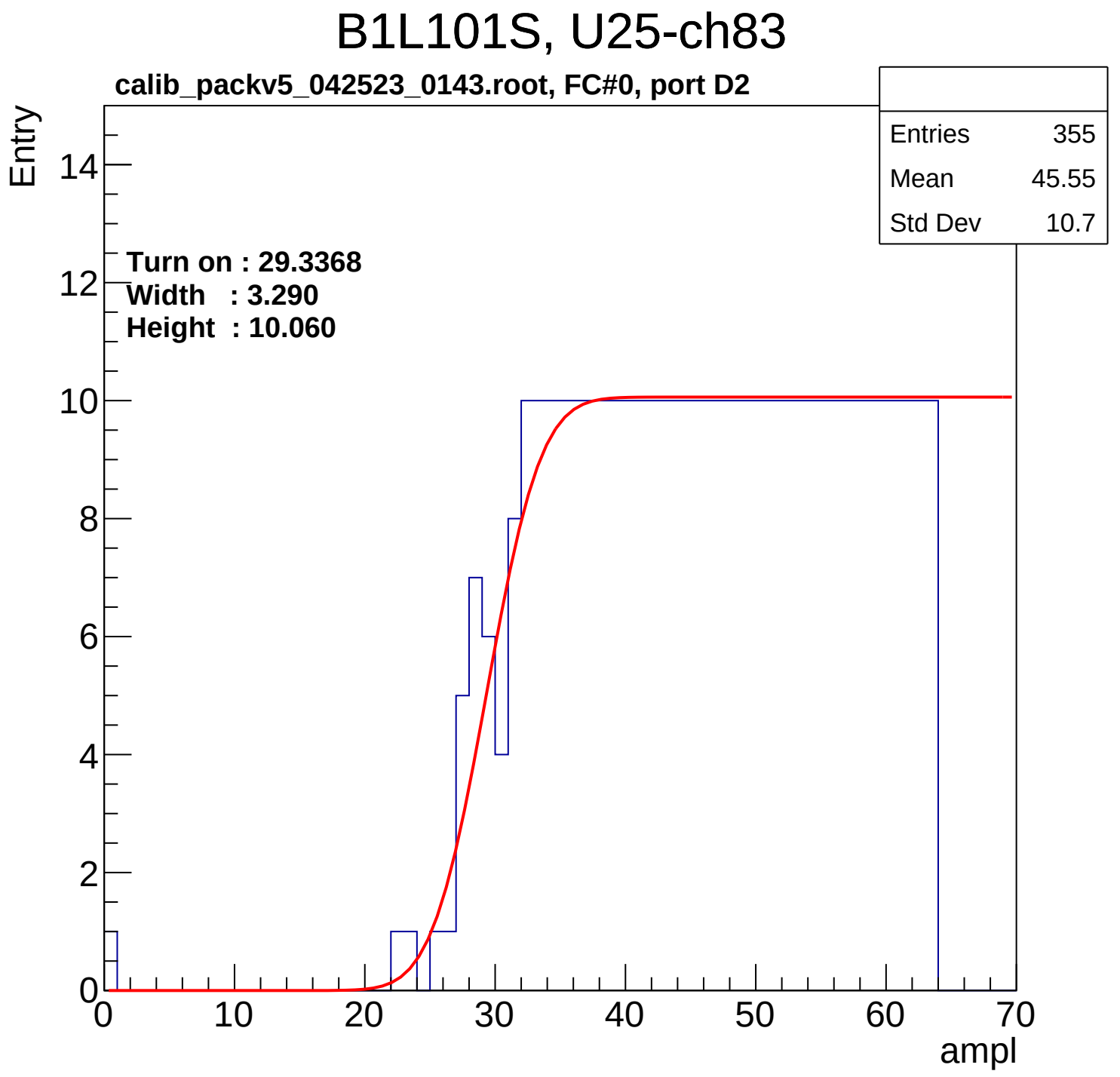
B1L101S, U25-ch83
calib_packv5_042523_0143.root, FC#0, port D2
Entries 355
Mean 45.55
Std Dev 10.7
Turn on : 29.3368
Width : 3.290
Height : 10.060
Entry
ampl
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6
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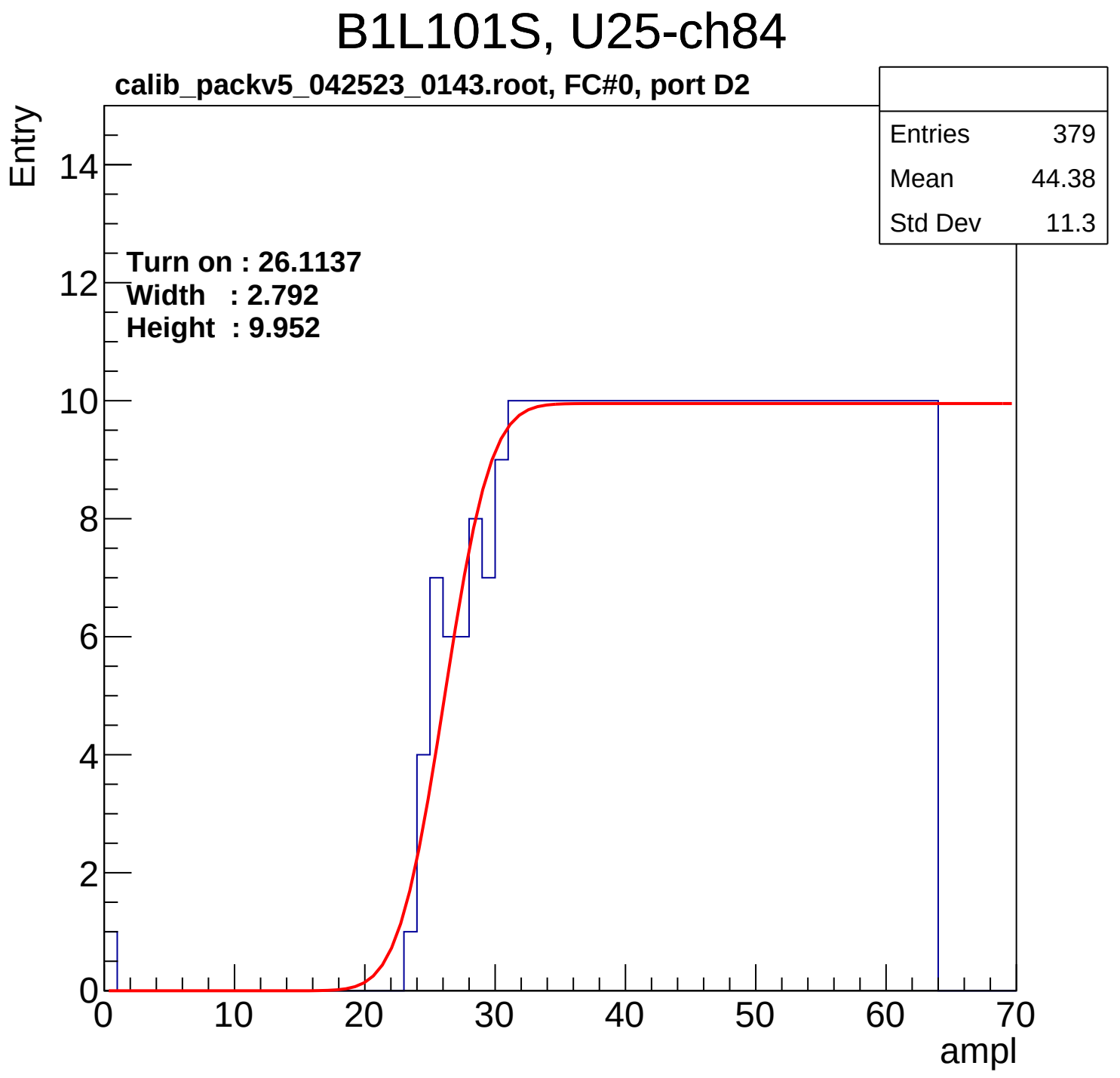
B1L101S, U25-ch84
calib_packv5_042523_0143.root, FC#0, port D2
Entries 379
Mean 44.38
Std Dev 11.3
Turn on : 26.1137
Width : 2.792
Height : 9.952
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ampl
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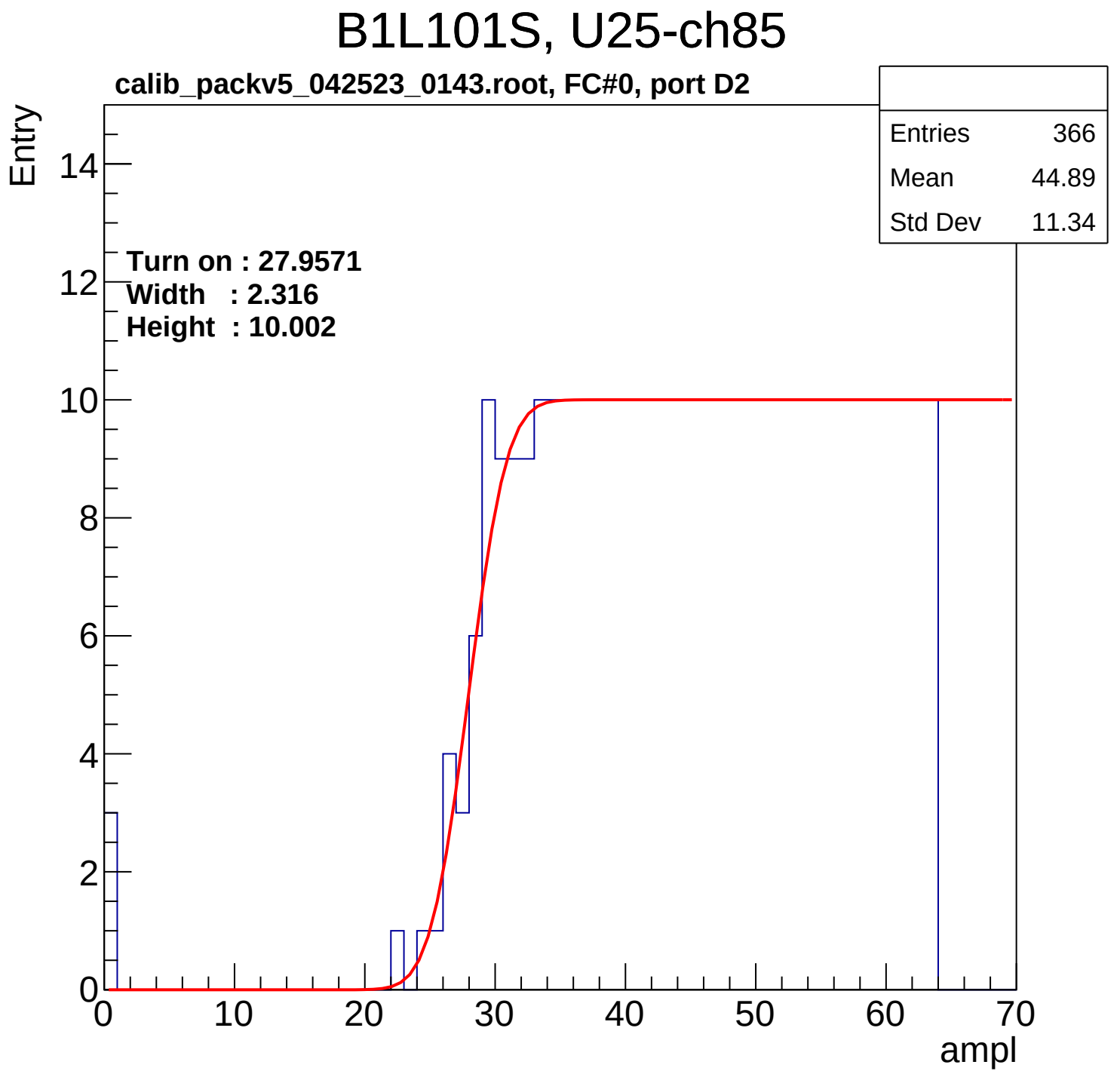
B1L101S, U25-ch85
calib_packv5_042523_0143.root, FC#0, port D2
Entries 366
Mean 44.89
Std Dev 11.34
Turn on : 27.9571
Width : 2.316
Height : 10.002
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ampl
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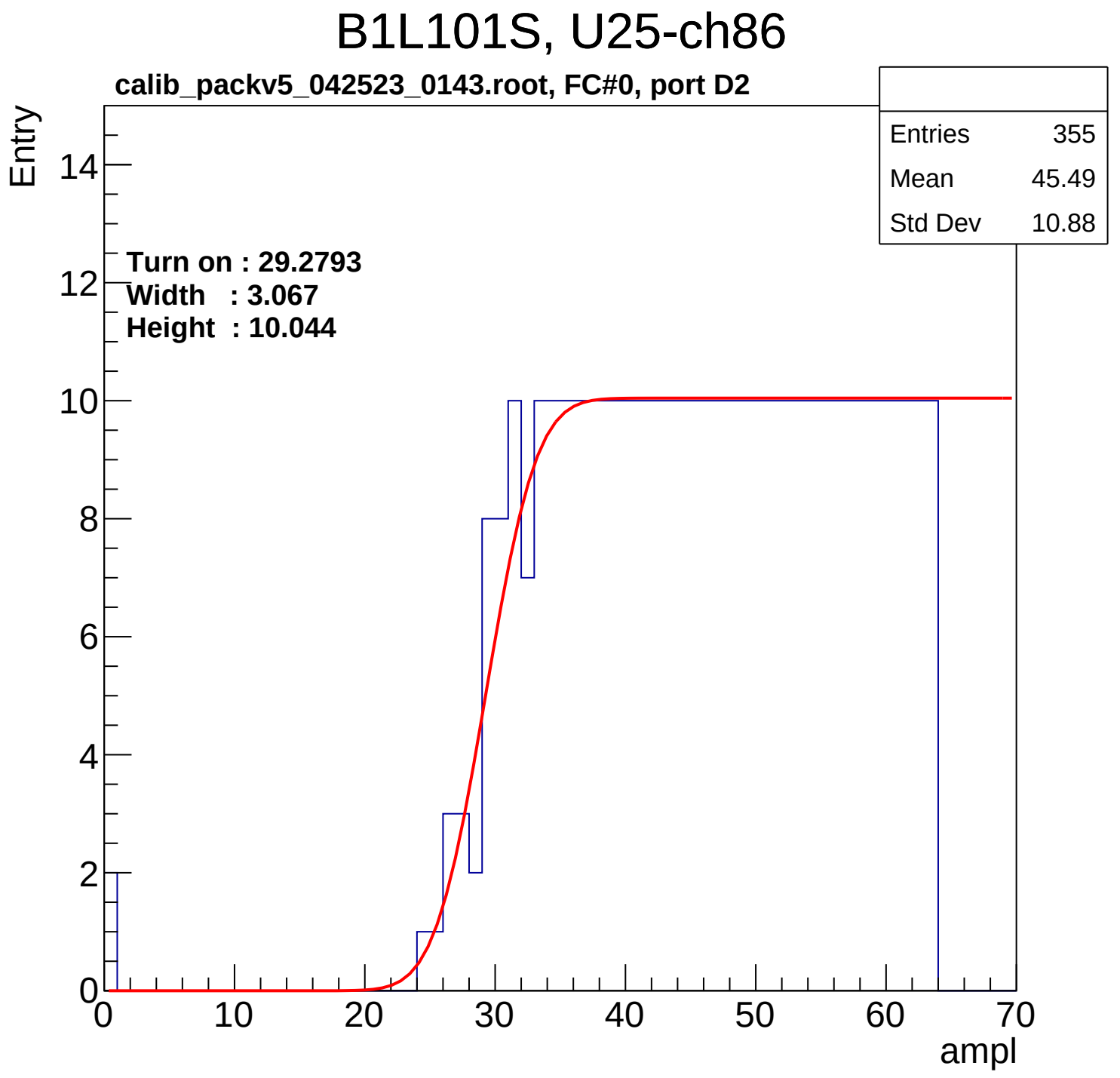
B1L101S, U25-ch86
calib_packv5_042523_0143.root, FC#0, port D2
Entries 355
Mean 45.49
Std Dev 10.88
Turn on : 29.2793
Width : 3.067
Height : 10.044
Entry
ampl
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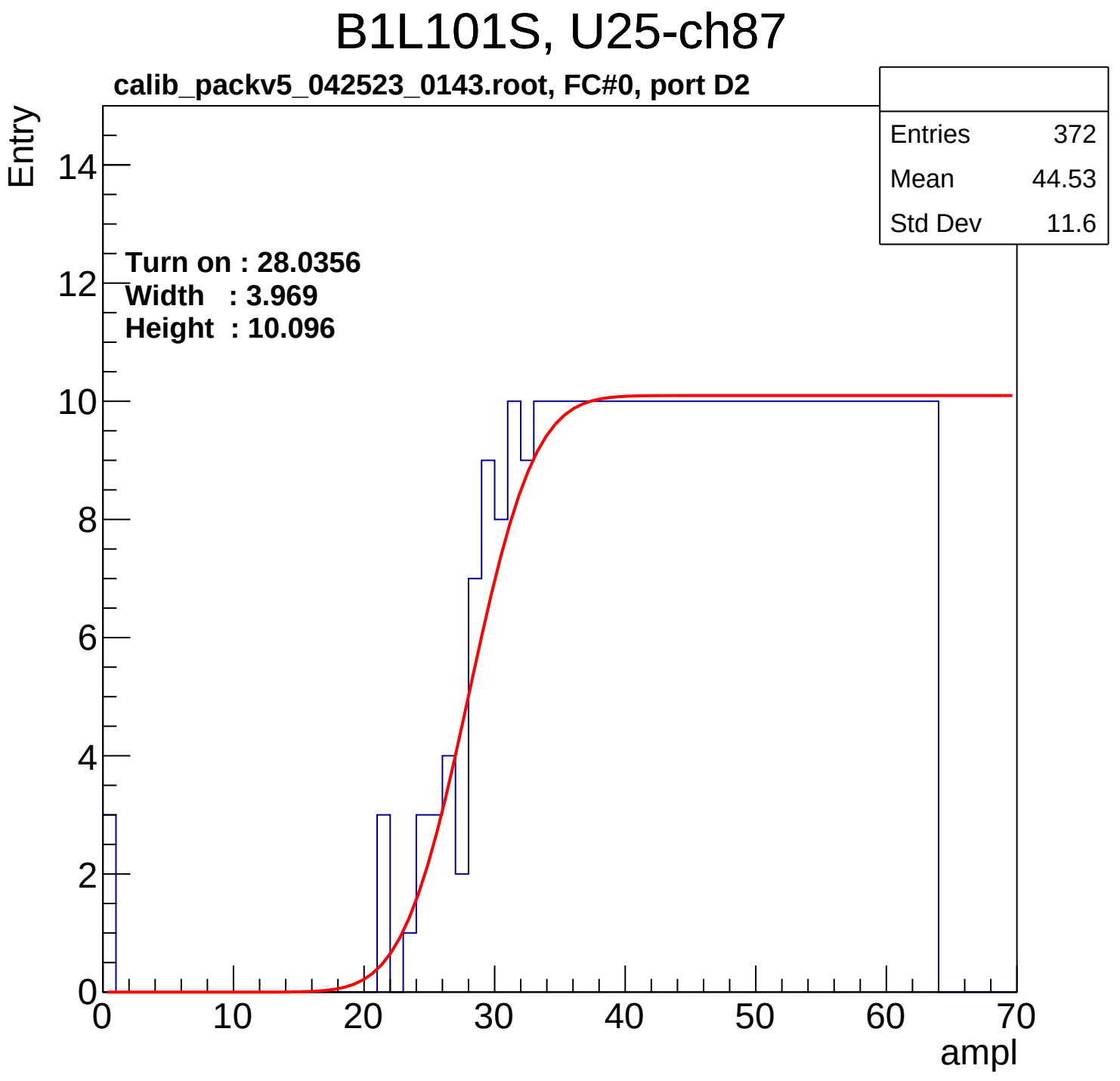
B1L101S, U25-ch87
calib_packv5_042523_0143.root, FC#0, port D2
Entries 372
Mean 44.53
Std Dev 11.6
Turn on : 28.0356
Width : 3.969
Height : 10.096
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ampl
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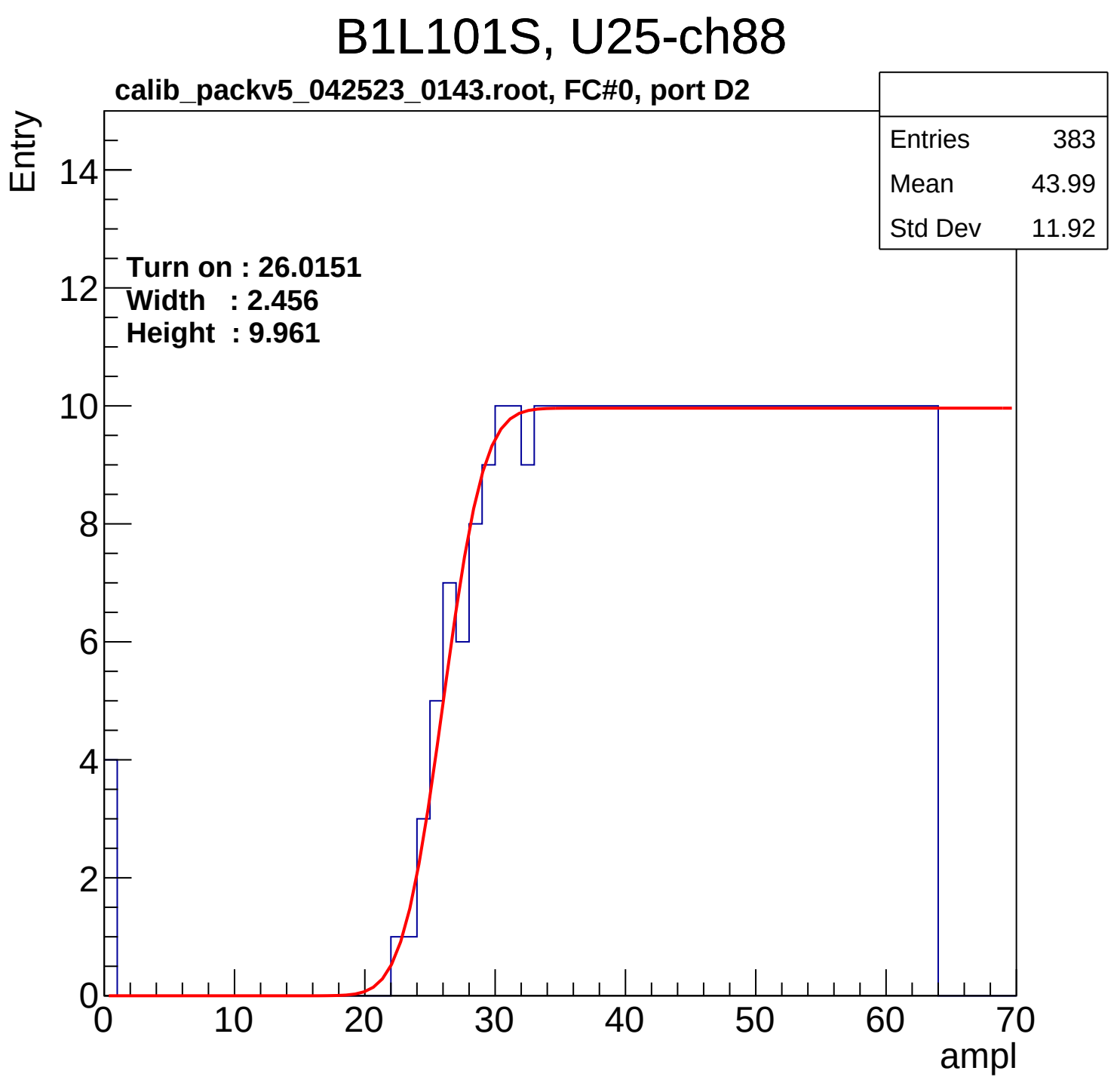
B1L101S, U25-ch88
calib_packv5_042523_0143.root, FC#0, port D2
Entries 383
Mean 43.99
Std Dev 11.92
Turn on : 26.0151
Width : 2.456
Height : 9.961
Entry
ampl
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2
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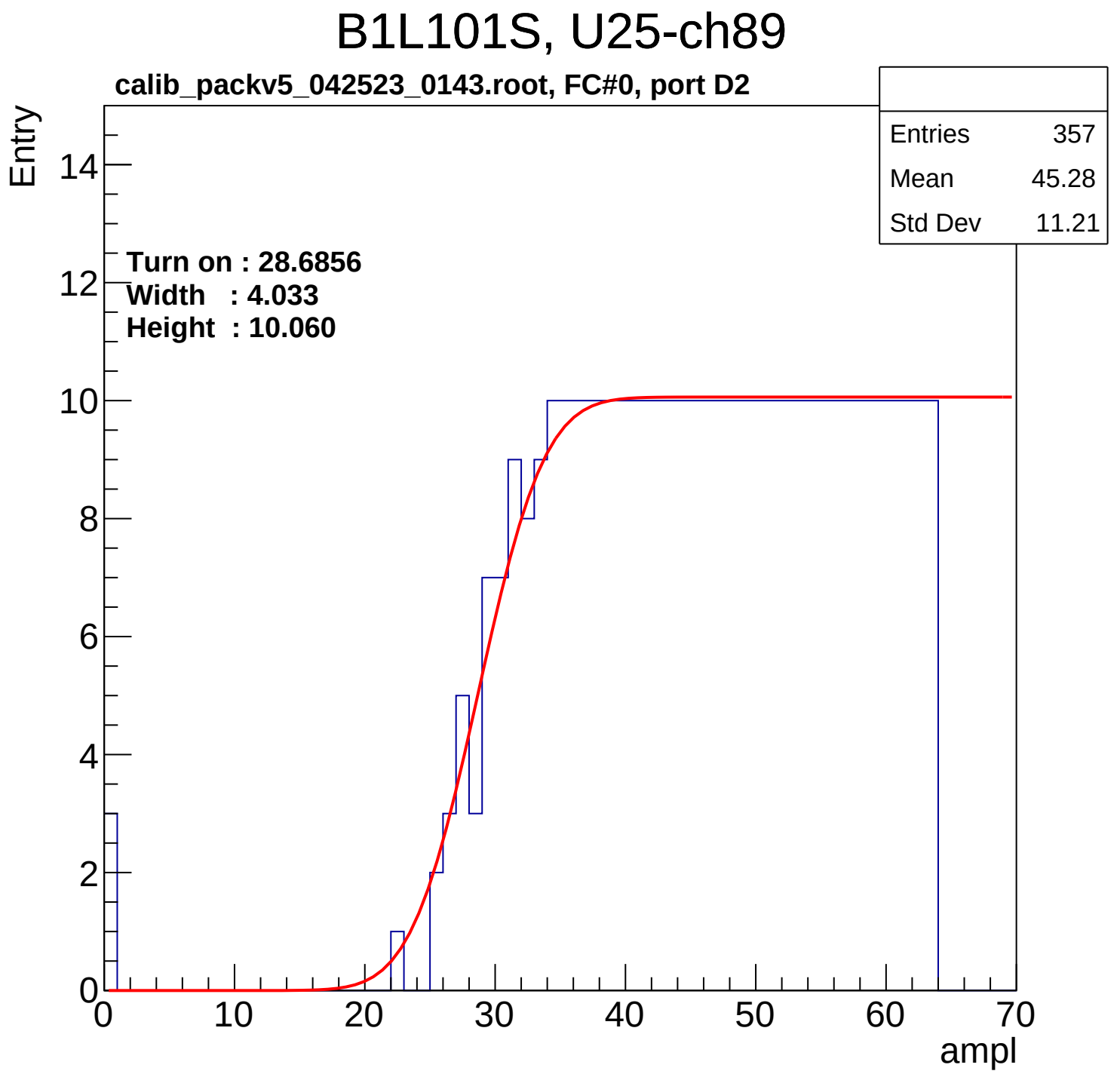
B1L101S, U25-ch89
calib_packv5_042523_0143.root, FC#0, port D2
Entries 357
Mean 45.28
Std Dev 11.21
Turn on : 28.6856
Width : 4.033
Height : 10.060
Entry
ampl
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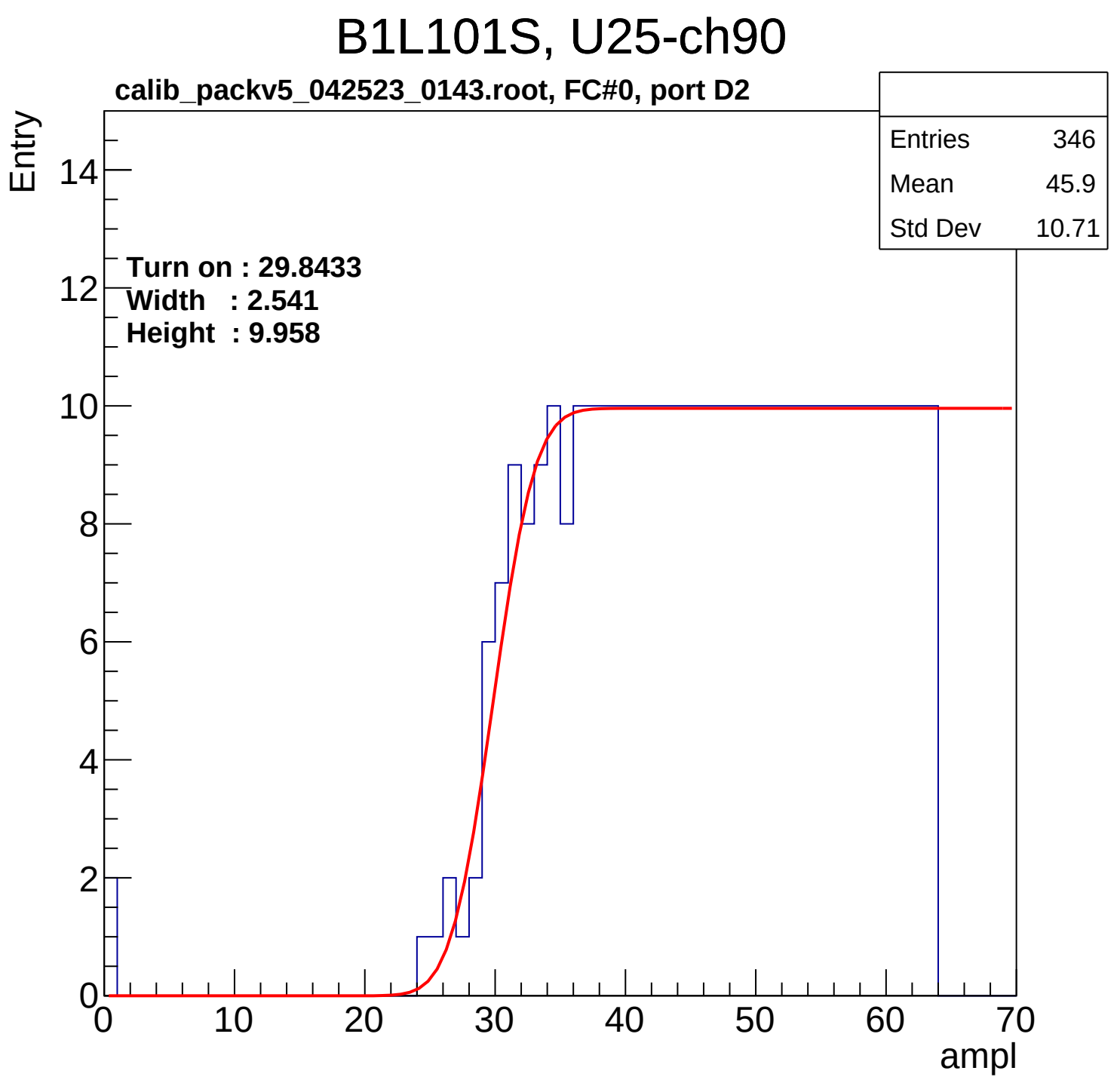
B1L101S, U25-ch90
calib_packv5_042523_0143.root, FC#0, port D2
Entries 346
Mean 45.9
Std Dev 10.71
Turn on : 29.8433
Width : 2.541
Height : 9.958
Entry
ampl
0
2
4
6
8
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0
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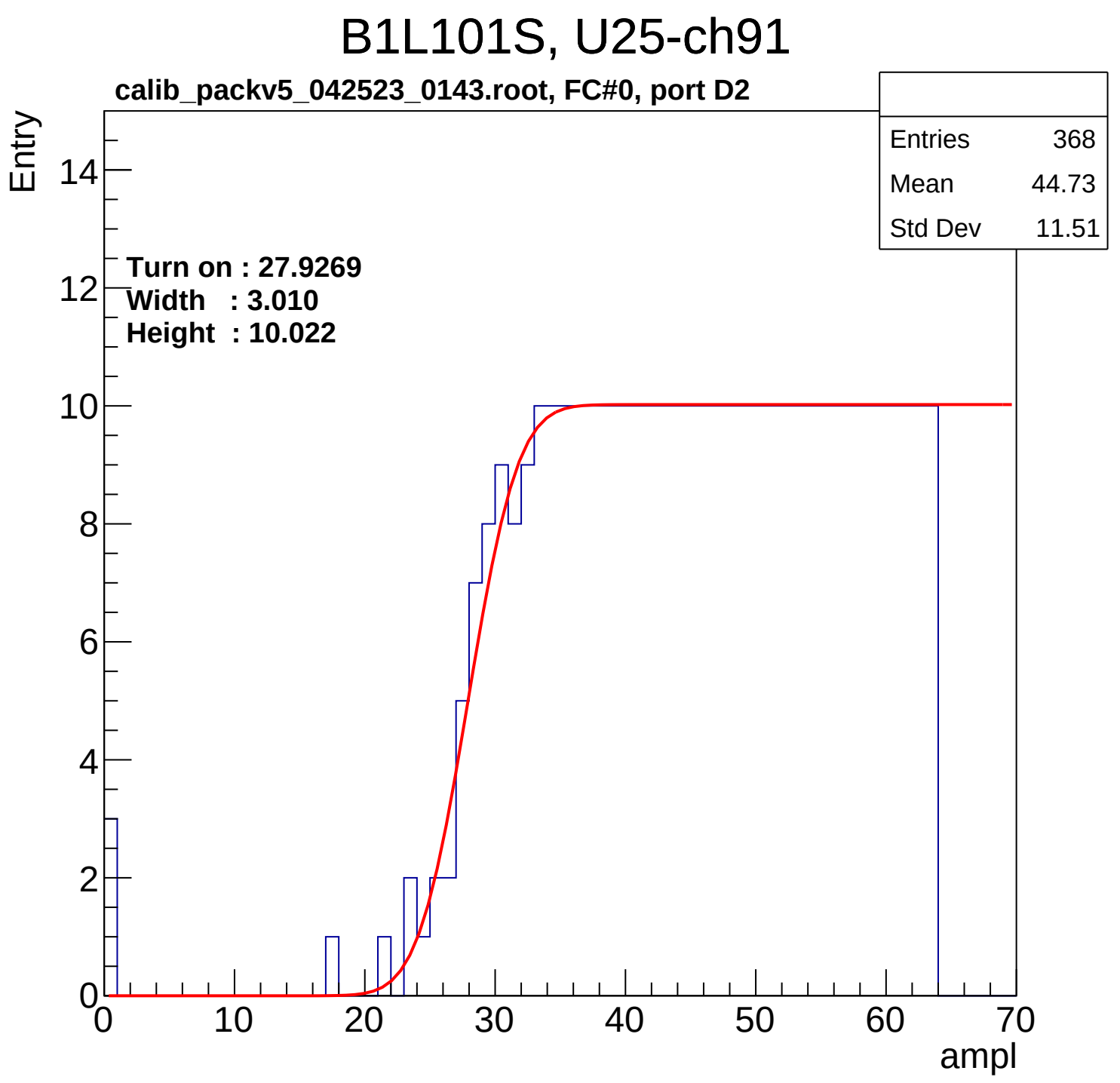
B1L101S, U25-ch91
calib_packv5_042523_0143.root, FC#0, port D2
Entries 368
Mean 44.73
Std Dev 11.51
Turn on : 27.9269
Width : 3.010
Height : 10.022
Entry
ampl
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2
4
6
8
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12
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0
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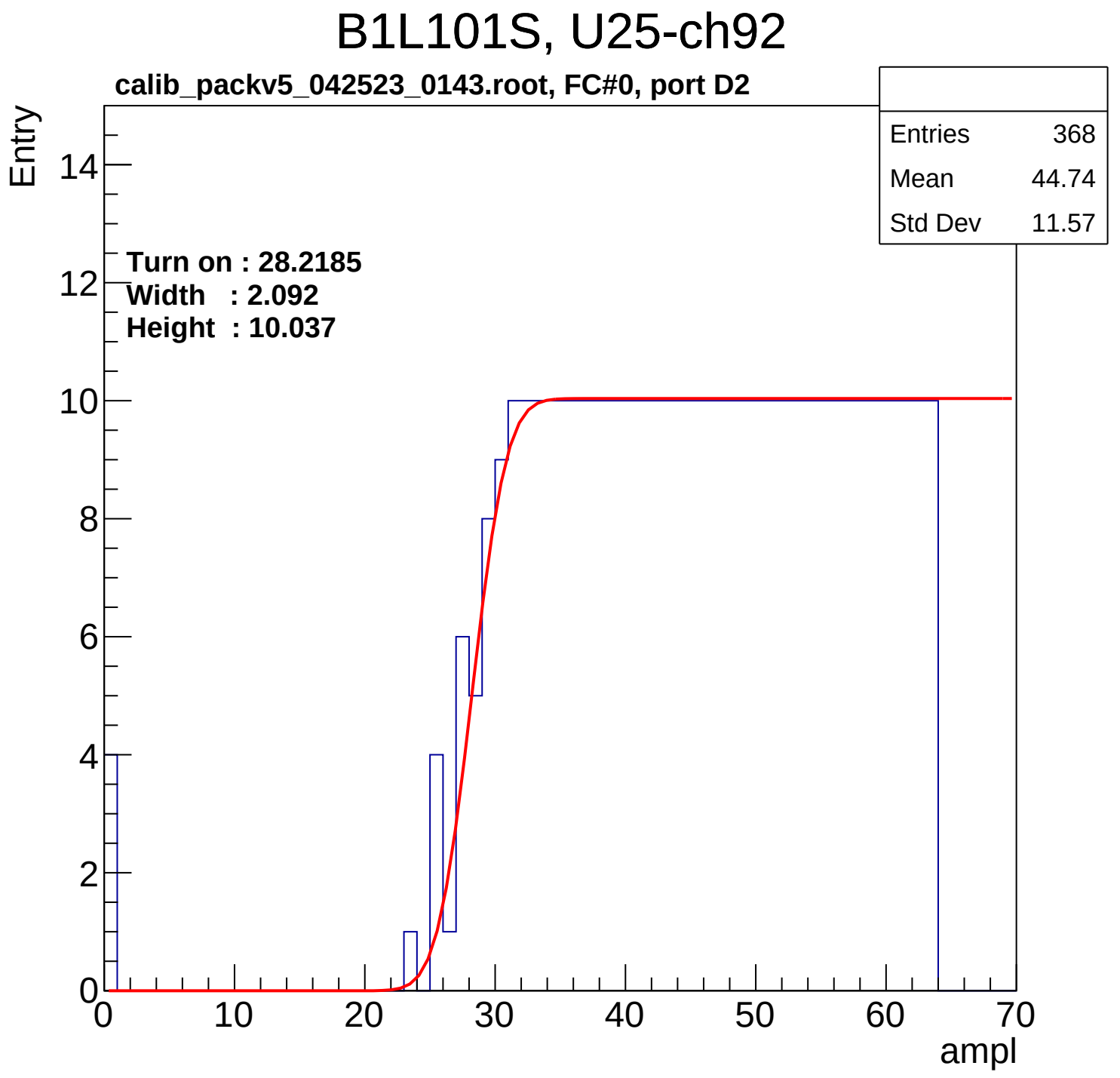
B1L101S, U25-ch92
calib_packv5_042523_0143.root, FC#0, port D2
Entries 368
Mean 44.74
Std Dev 11.57
Turn on : 28.2185
Width : 2.092
Height : 10.037
Entry
ampl
0
2
4
6
8
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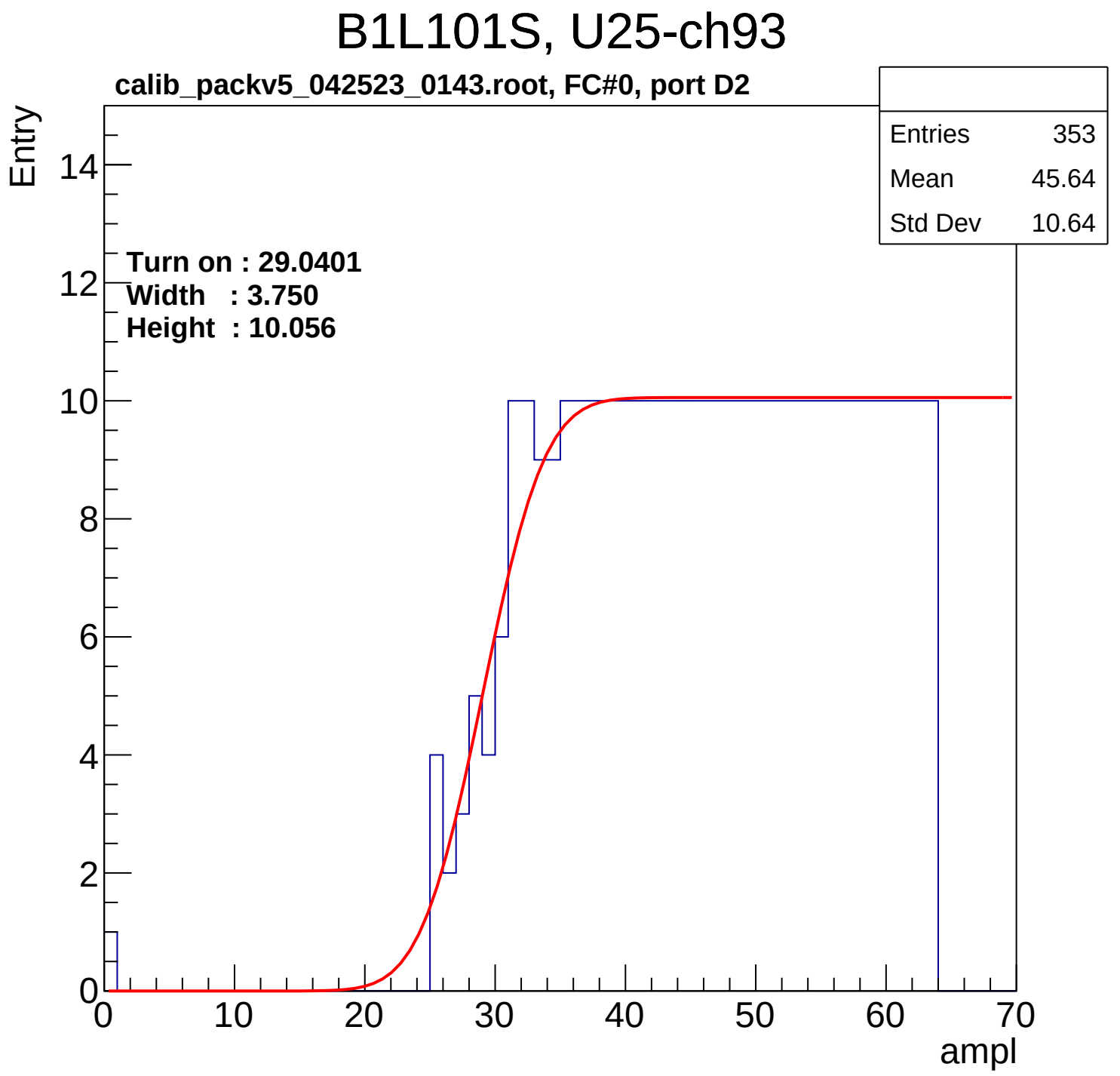
B1L101S, U25-ch93
calib_packv5_042523_0143.root, FC#0, port D2
Entries 353
Mean 45.64
Std Dev 10.64
Turn on : 29.0401
Width : 3.750
Height : 10.056
Entry
ampl
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4
6
8
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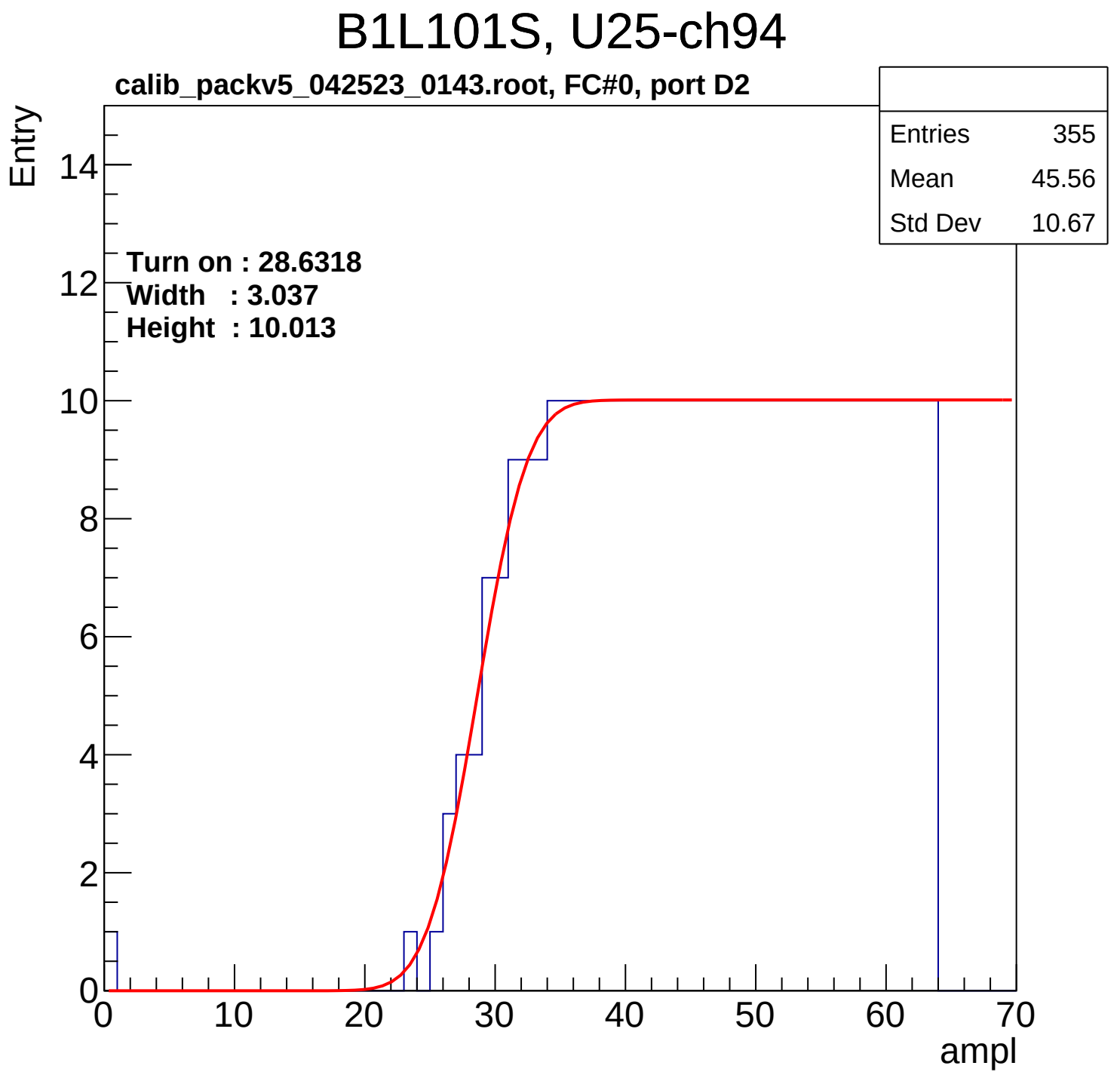
B1L101S, U25-ch94
calib_packv5_042523_0143.root, FC#0, port D2
Entries 355
Mean 45.56
Std Dev 10.67
Turn on : 28.6318
Width : 3.037
Height : 10.013
Entry
ampl
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2
4
6
8
10
12
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0
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60
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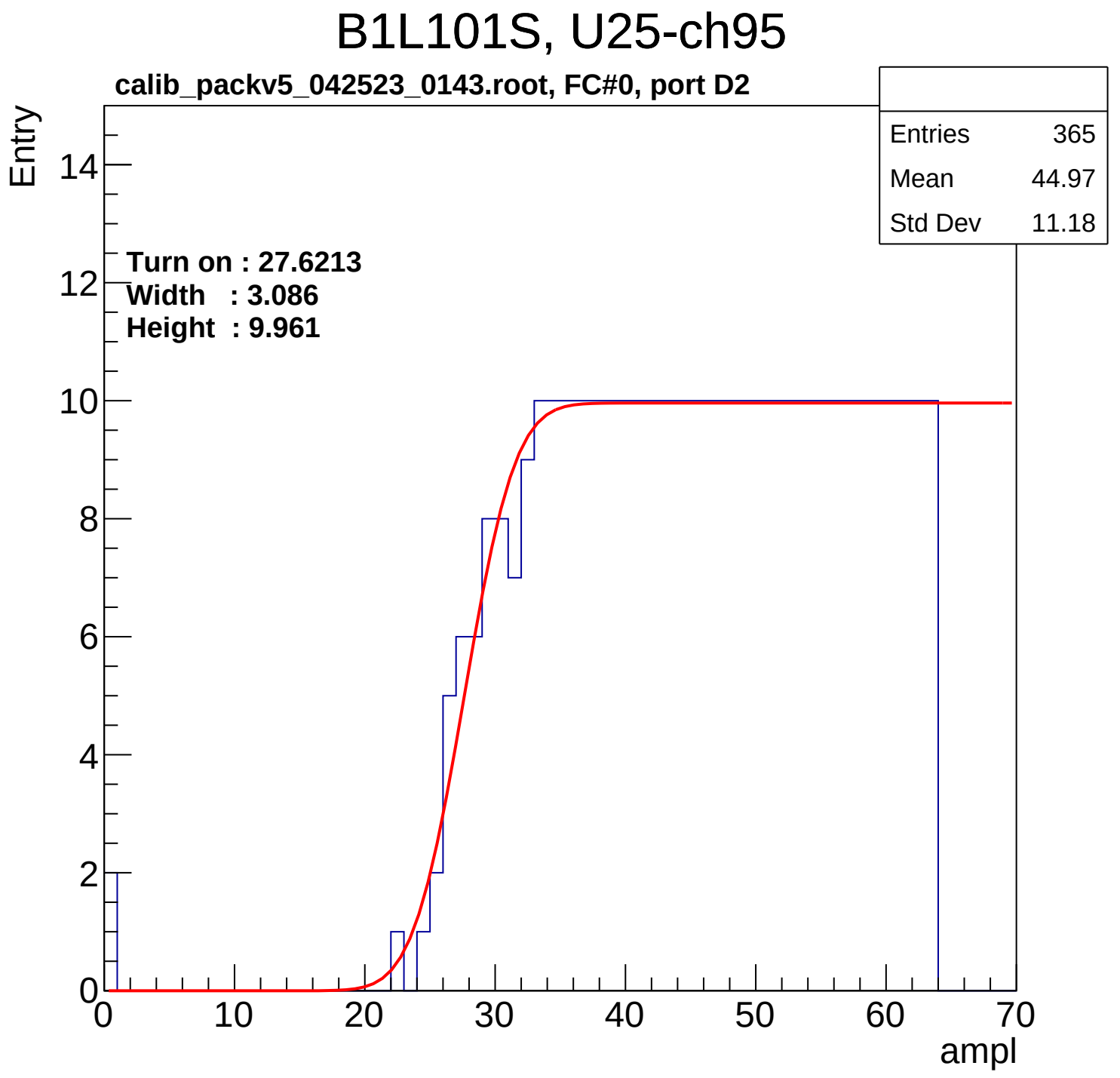
B1L101S, U25-ch95
calib_packv5_042523_0143.root, FC#0, port D2
Entries 365
Mean 44.97
Std Dev 11.18
Turn on : 27.6213
Width : 3.086
Height : 9.961
Entry
ampl
0
2
4
6
8
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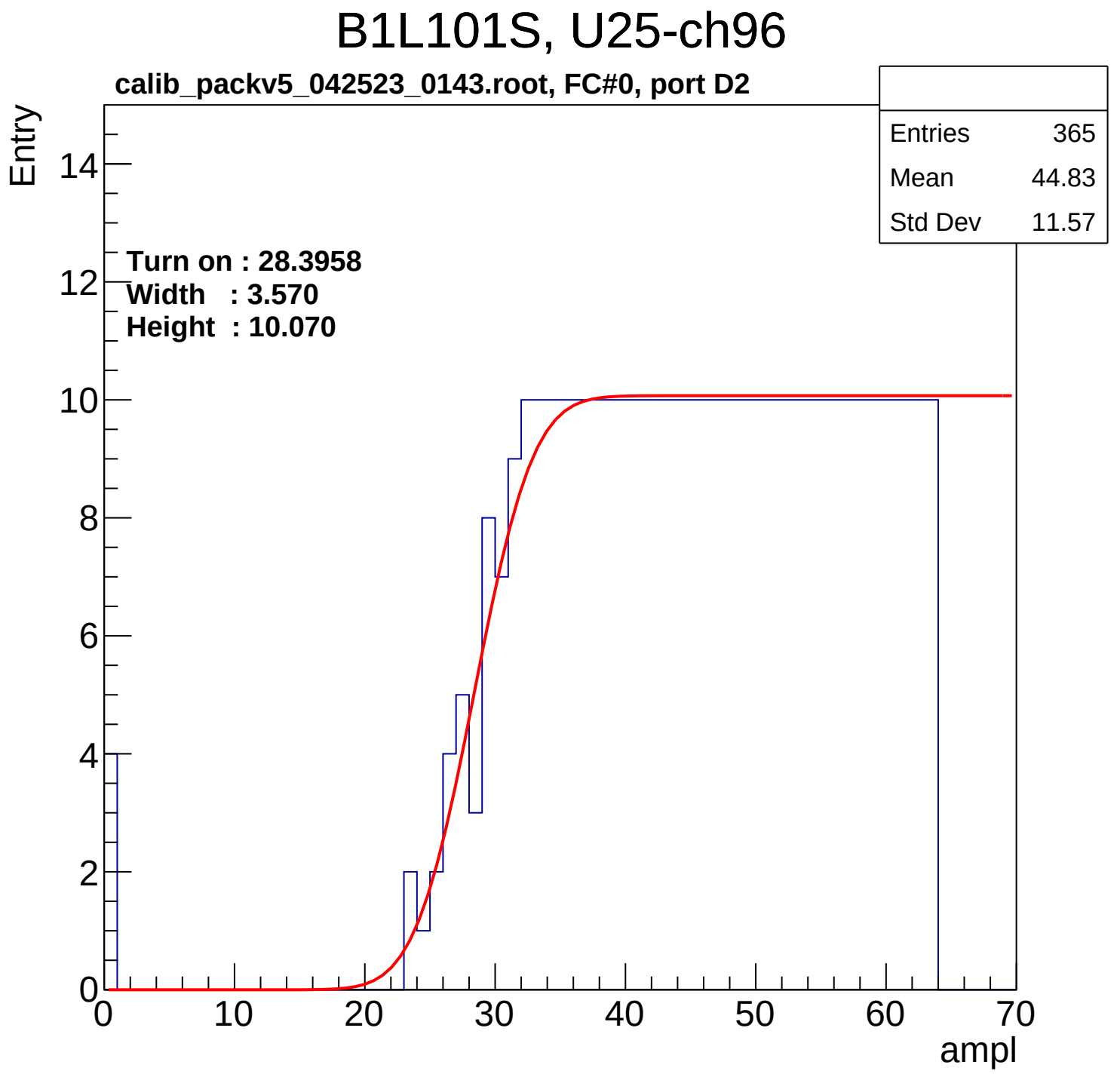
B1L101S, U25-ch96
calib_packv5_042523_0143.root, FC#0, port D2
Entries 365
Mean 44.83
Std Dev 11.57
Turn on : 28.3958
Width : 3.570
Height : 10.070
Entry
ampl
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6
8
10
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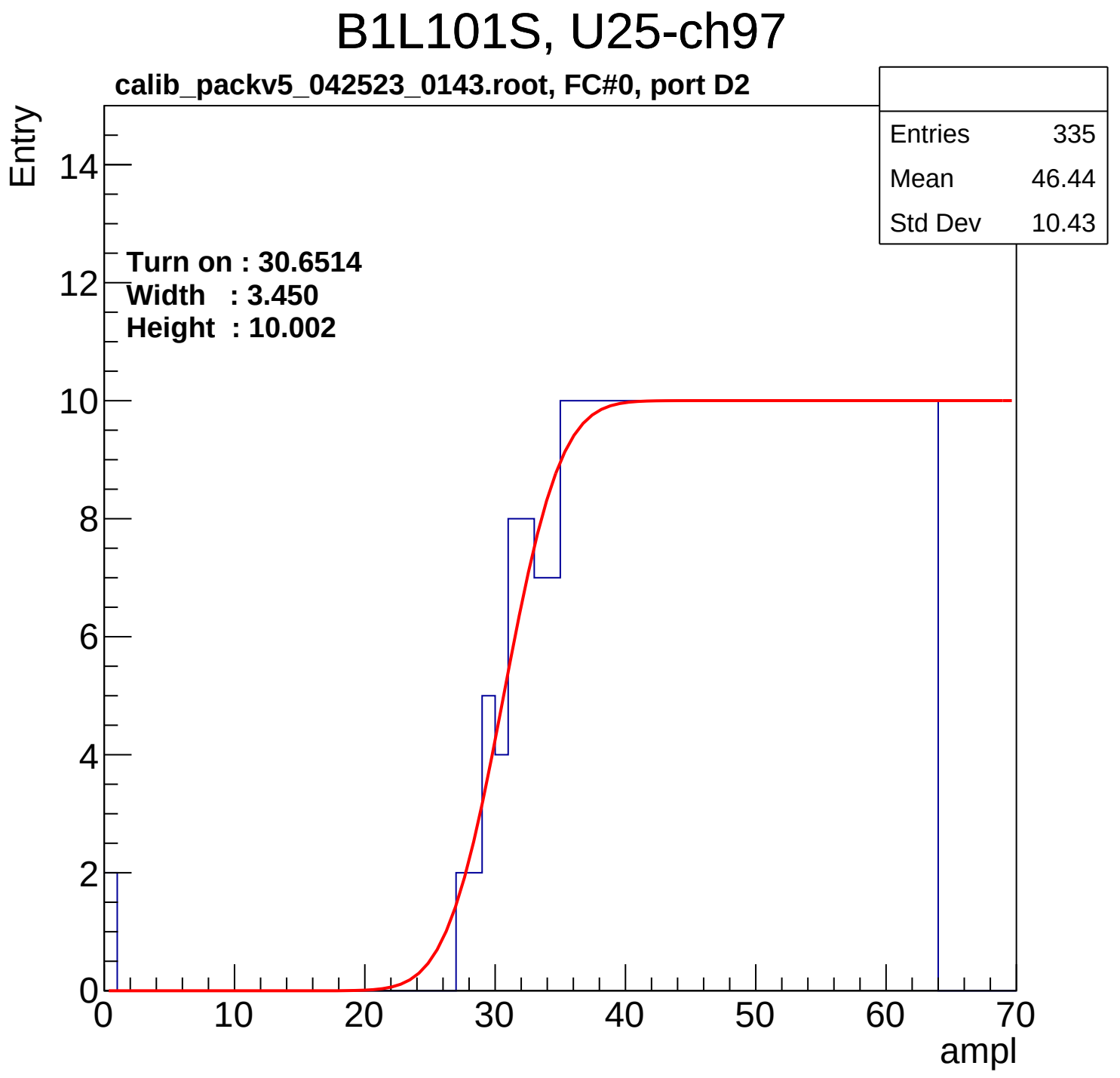
B1L101S, U25-ch97
calib_packv5_042523_0143.root, FC#0, port D2
Entries 335
Mean 46.44
Std Dev 10.43
Turn on : 30.6514
Width : 3.450
Height : 10.002
Entry
ampl
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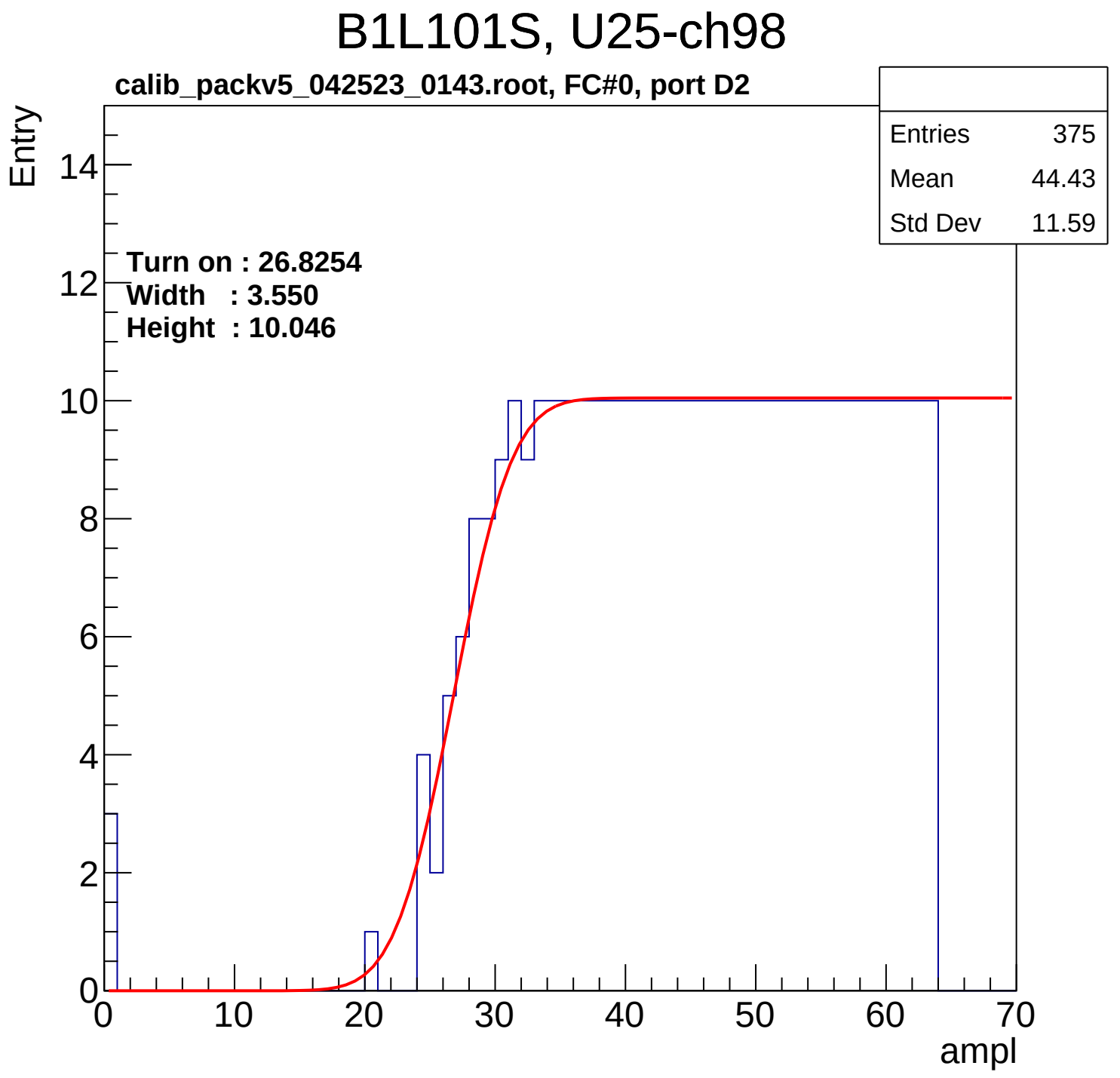
B1L101S, U25-ch98
calib_packv5_042523_0143.root, FC#0, port D2
Entries 375
Mean 44.43
Std Dev 11.59
Turn on : 26.8254
Width : 3.550
Height : 10.046
Entry
ampl
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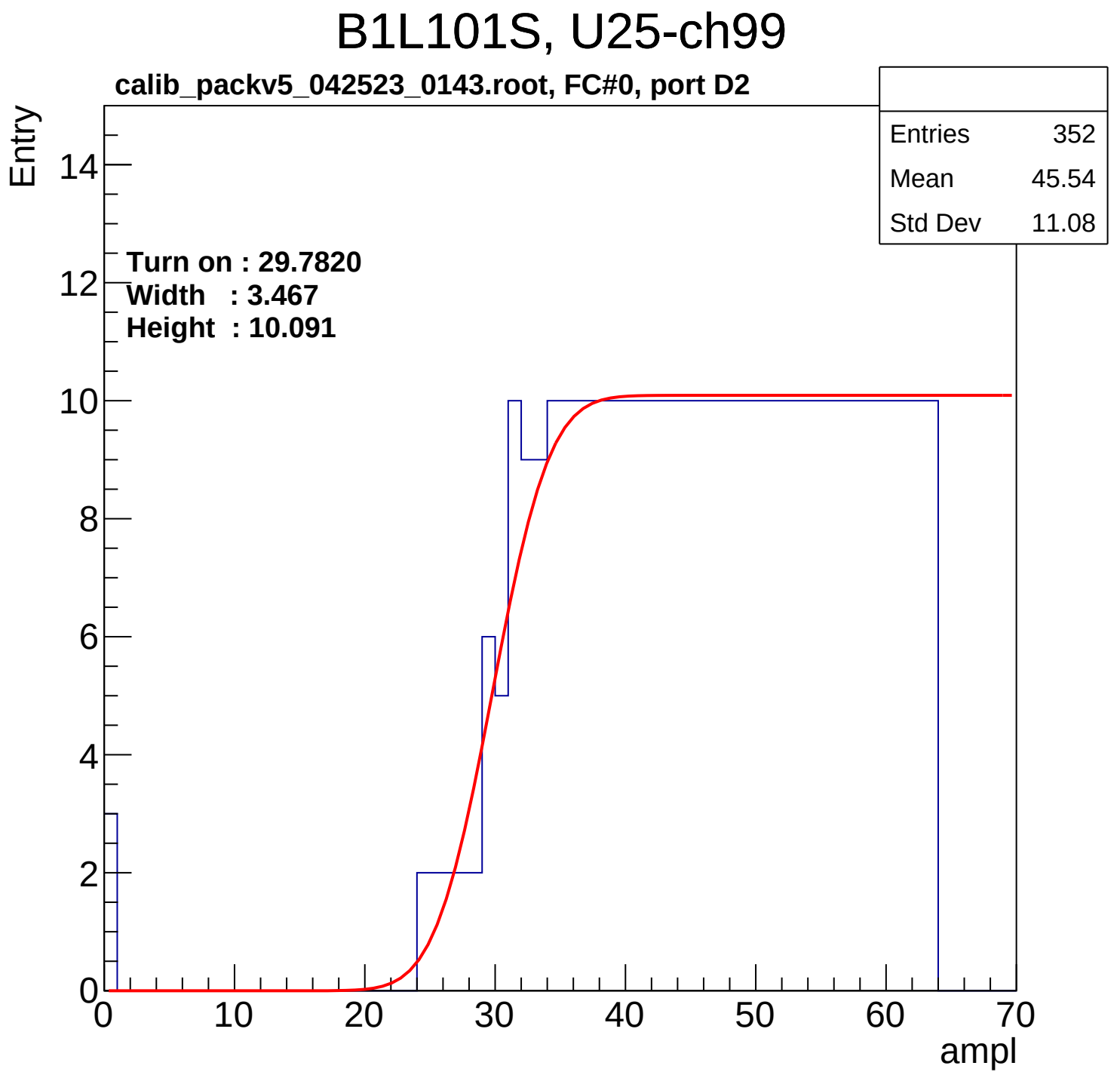
B1L101S, U25-ch99
calib_packv5_042523_0143.root, FC#0, port D2
Entries 352
Mean 45.54
Std Dev 11.08
Turn on : 29.7820
Width : 3.467
Height : 10.091
Entry
ampl
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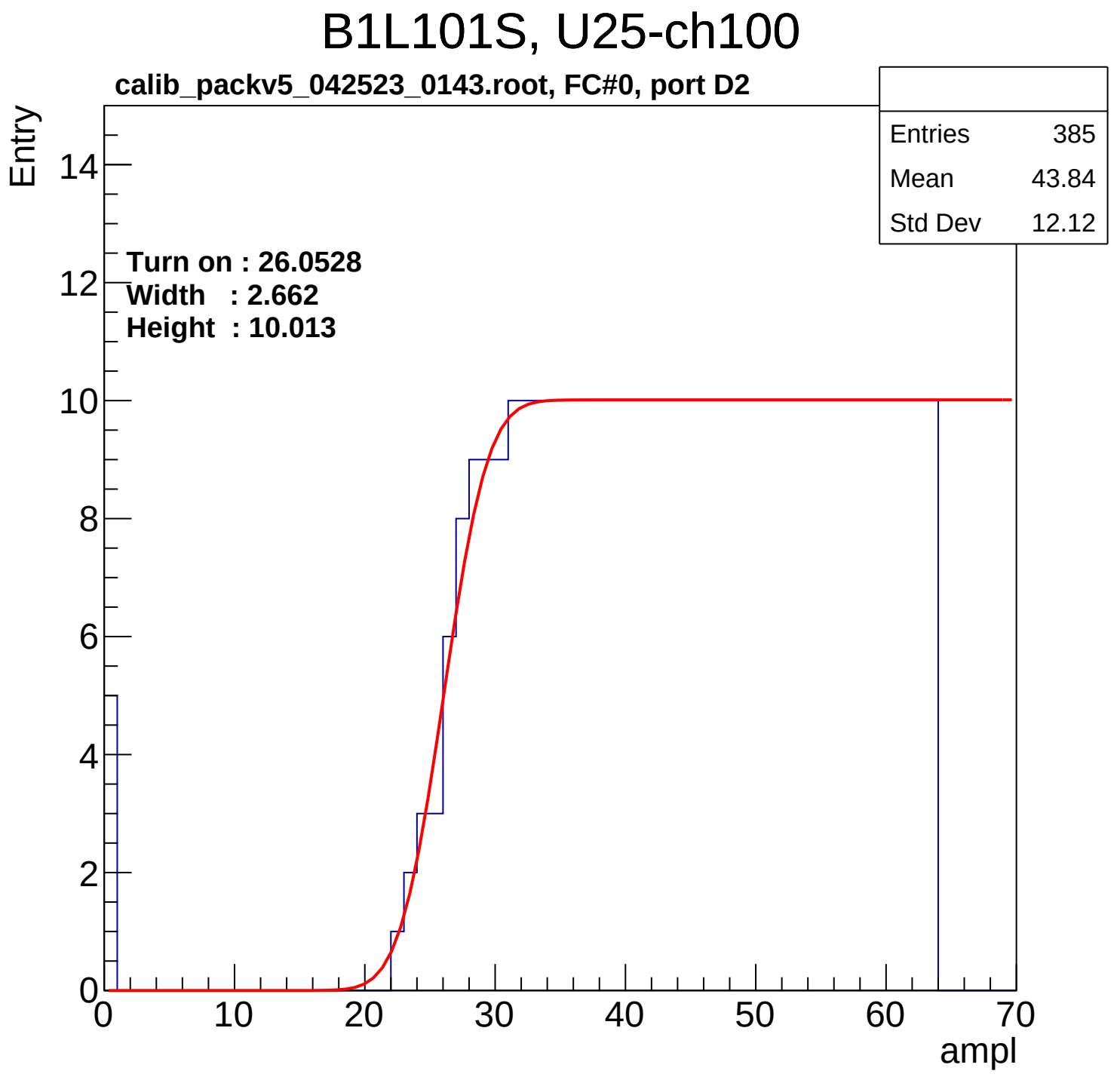
B1L101S, U25-ch100
calib_packv5_042523_0143.root, FC#0, port D2
Entries 385
Mean 43.84
Std Dev 12.12
Turn on : 26.0528
Width : 2.662
Height : 10.013
Entry
ampl
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6
8
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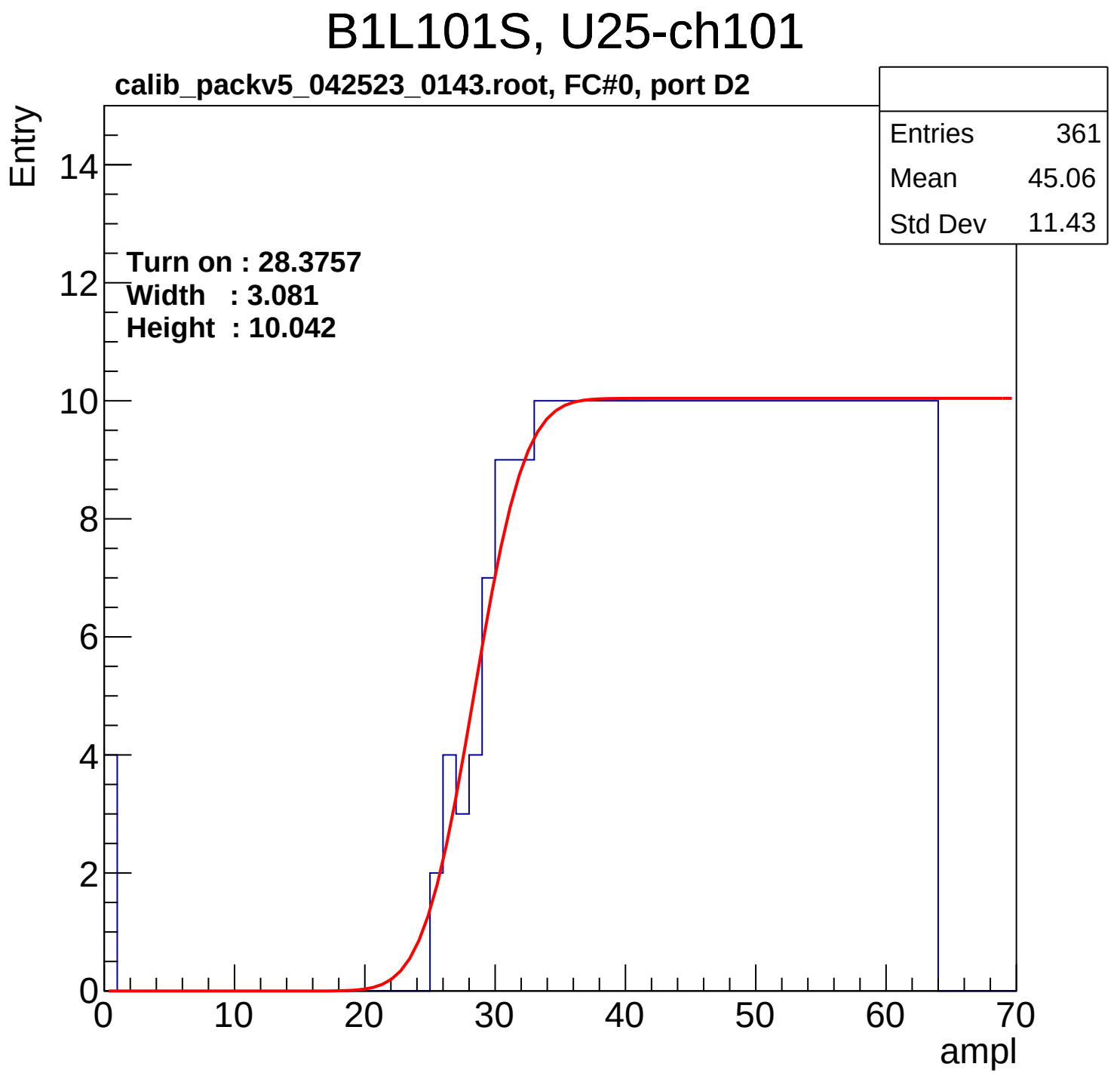
B1L101S, U25-ch101
calib_packv5_042523_0143.root, FC#0, port D2
Entries 361
Mean 45.06
Std Dev 11.43
Turn on : 28.3757
Width : 3.081
Height : 10.042
Entry
ampl
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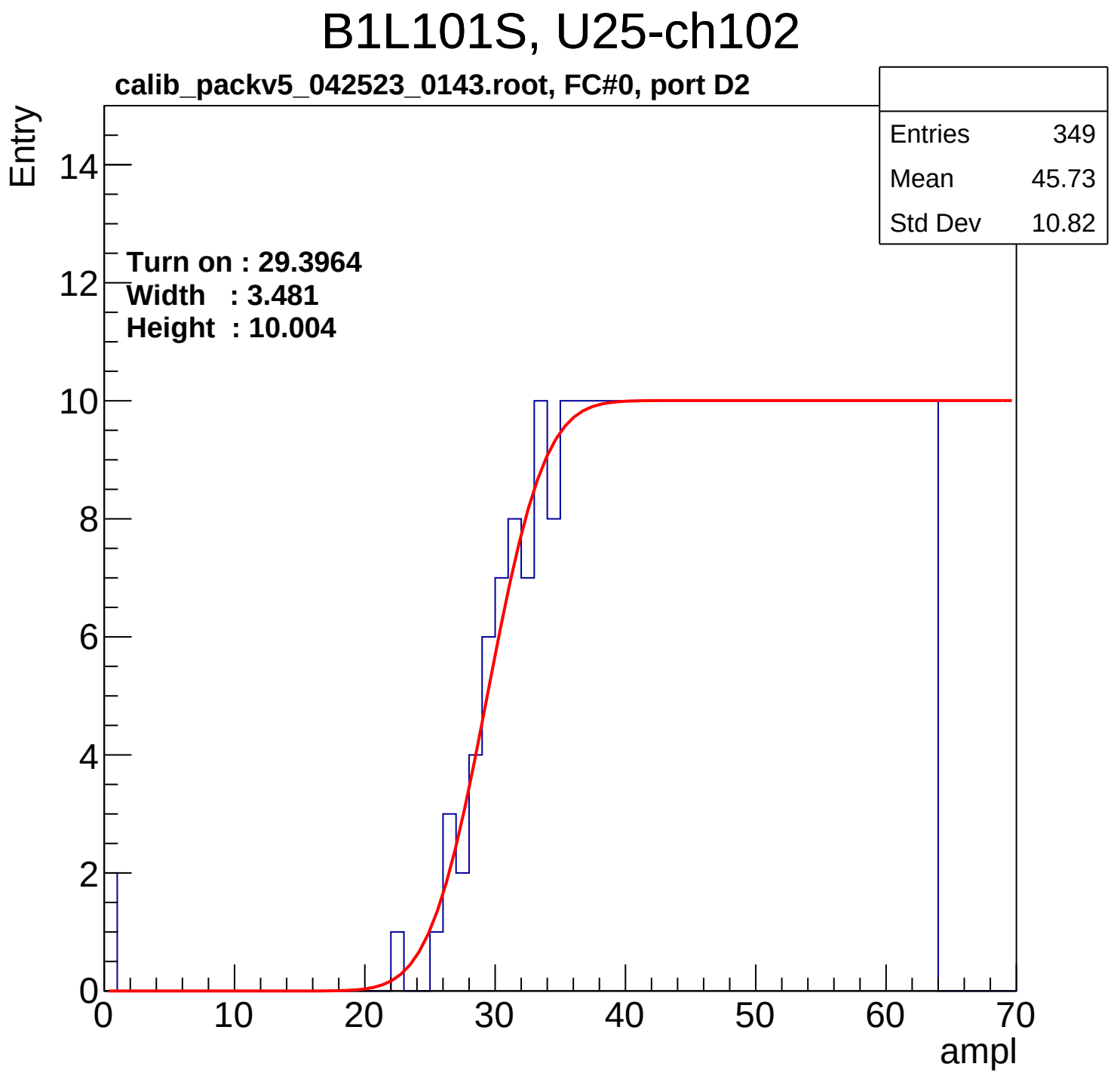
B1L101S, U25-ch102
calib_packv5_042523_0143.root, FC#0, port D2
Entries 349
Mean 45.73
Std Dev 10.82
Turn on : 29.3964
Width : 3.481
Height : 10.004
Entry
ampl
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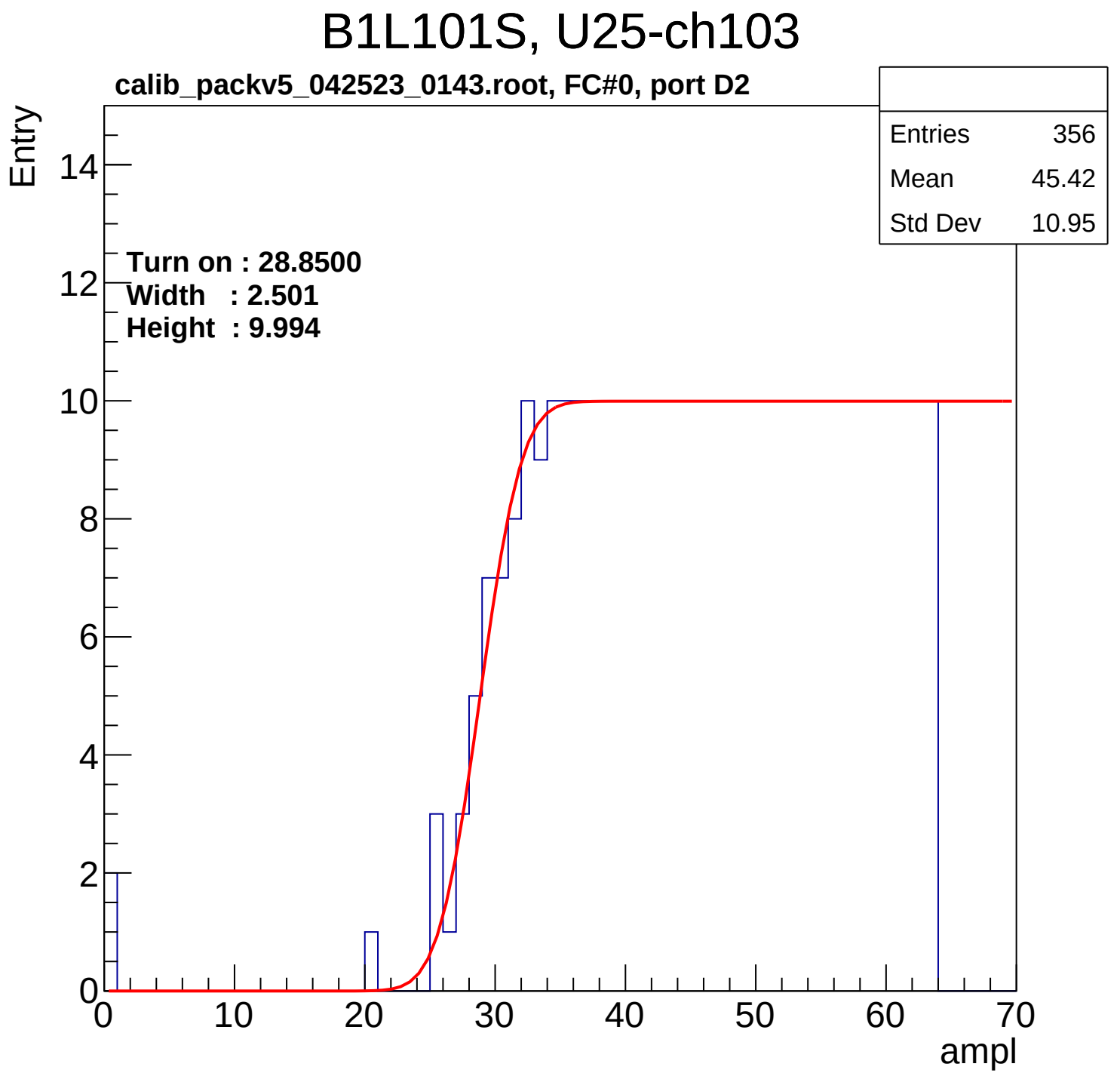
B1L101S, U25-ch103
calib_packv5_042523_0143.root, FC#0, port D2
Entries 356
Mean 45.42
Std Dev 10.95
Turn on : 28.8500
Width : 2.501
Height : 9.994
Entry
ampl
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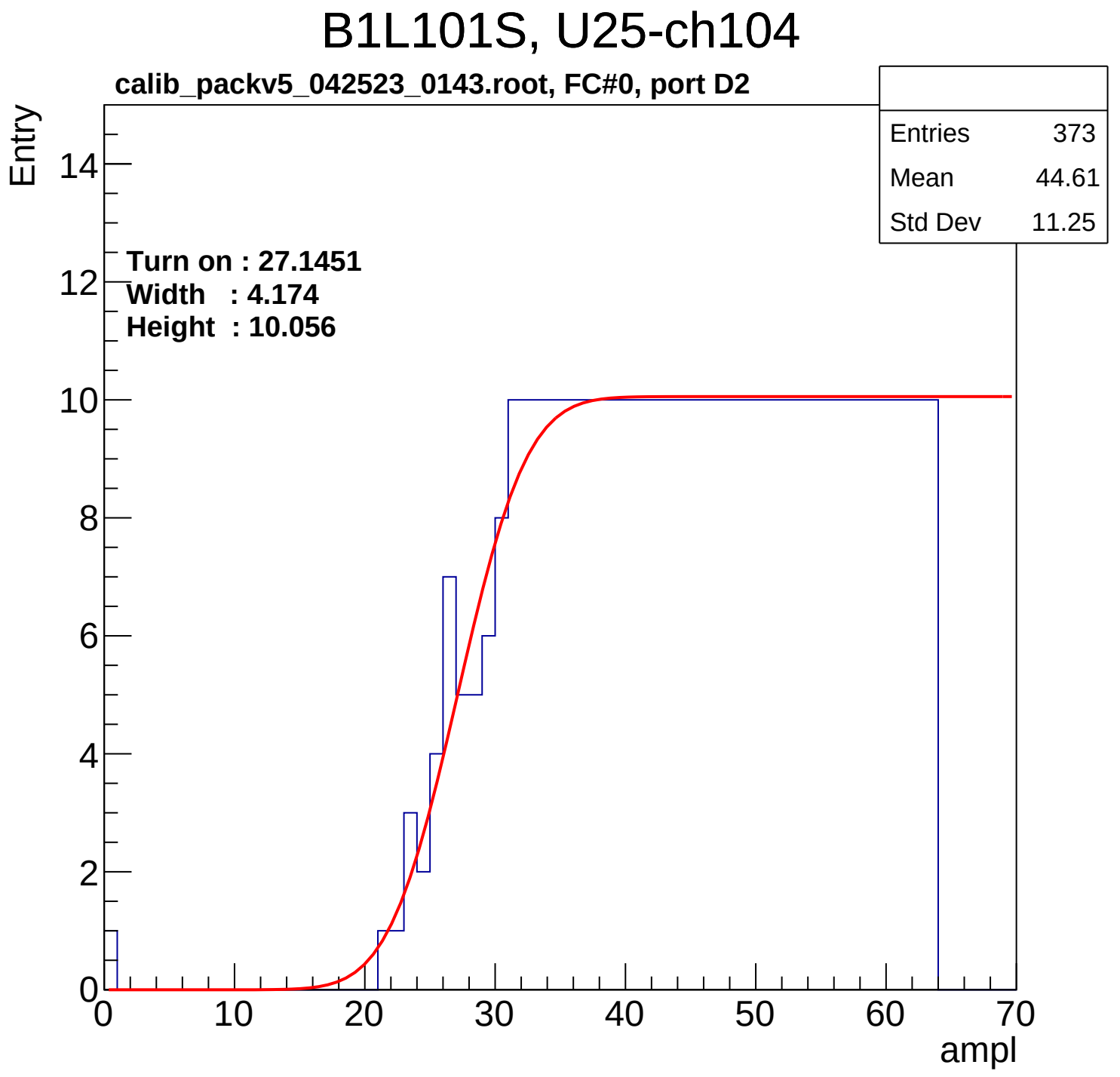
B1L101S, U25-ch104
calib_packv5_042523_0143.root, FC#0, port D2
Entries 373
Mean 44.61
Std Dev 11.25
Turn on : 27.1451
Width : 4.174
Height : 10.056
Entry
ampl
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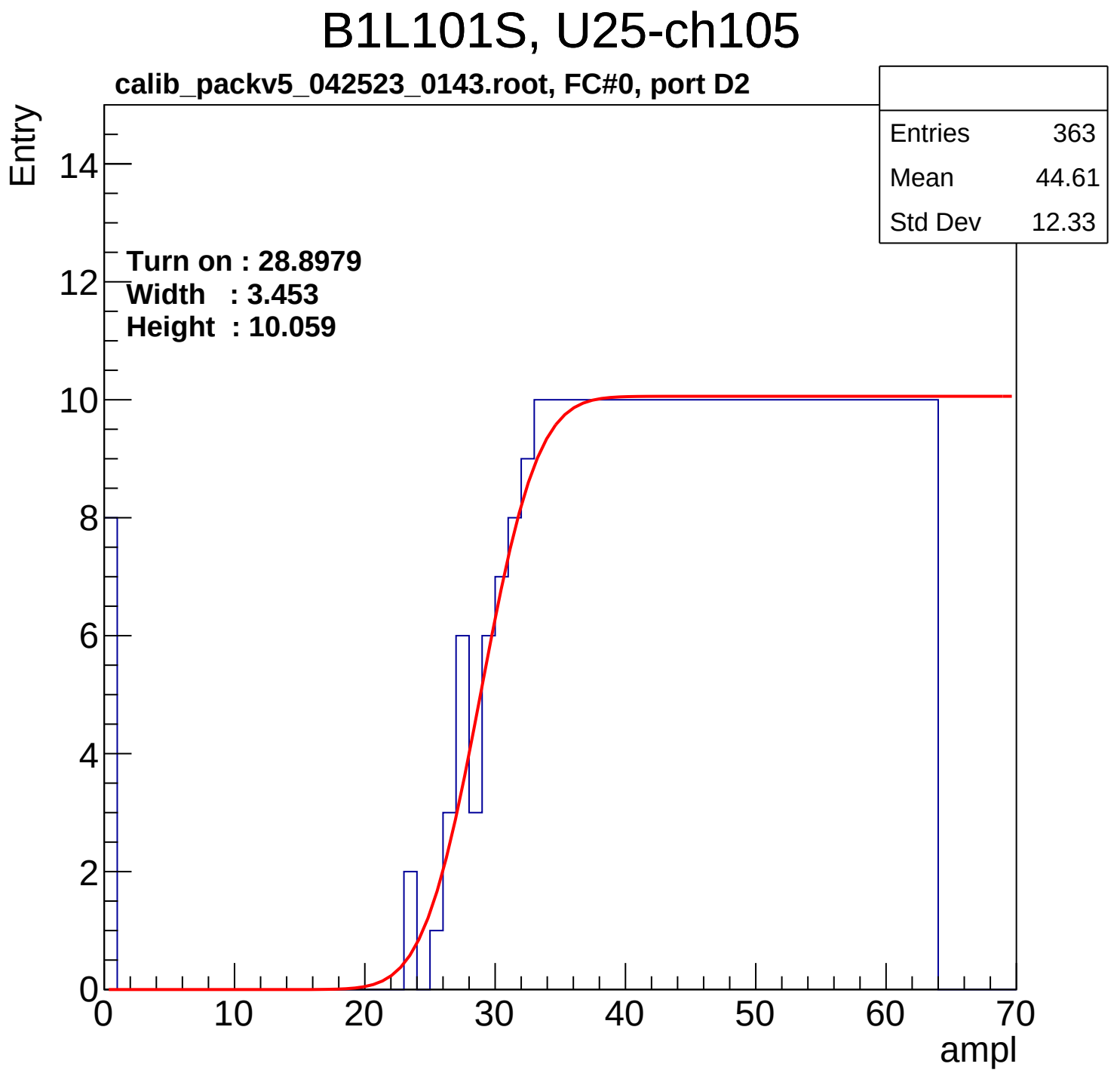
B1L101S, U25-ch105
calib_packv5_042523_0143.root, FC#0, port D2
Entries 363
Mean 44.61
Std Dev 12.33
Turn on : 28.8979
Width : 3.453
Height : 10.059
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ampl
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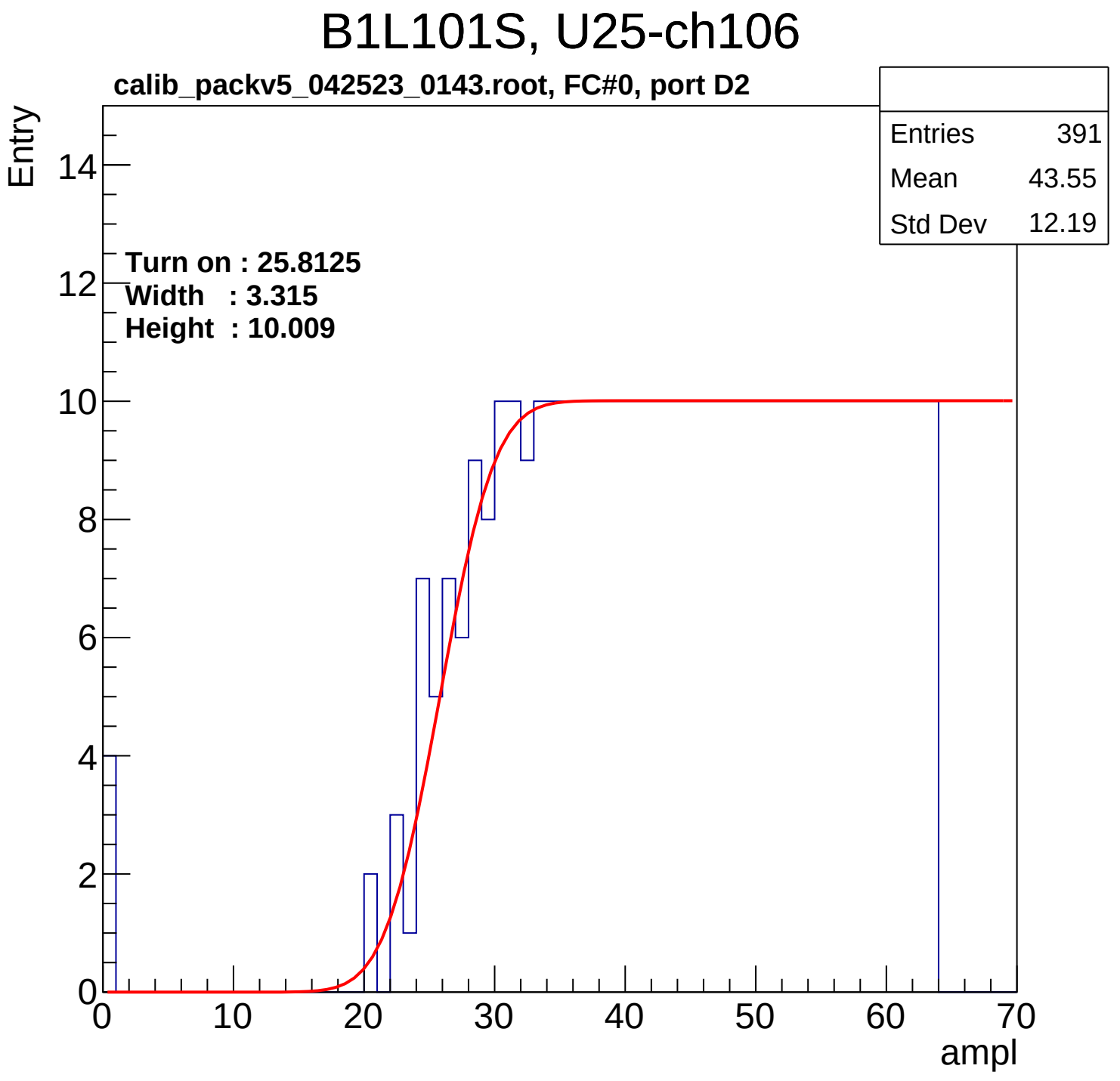
B1L101S, U25-ch106
calib_packv5_042523_0143.root, FC#0, port D2
Entries 391
Mean 43.55
Std Dev 12.19
Turn on : 25.8125
Width : 3.315
Height : 10.009
Entry
ampl
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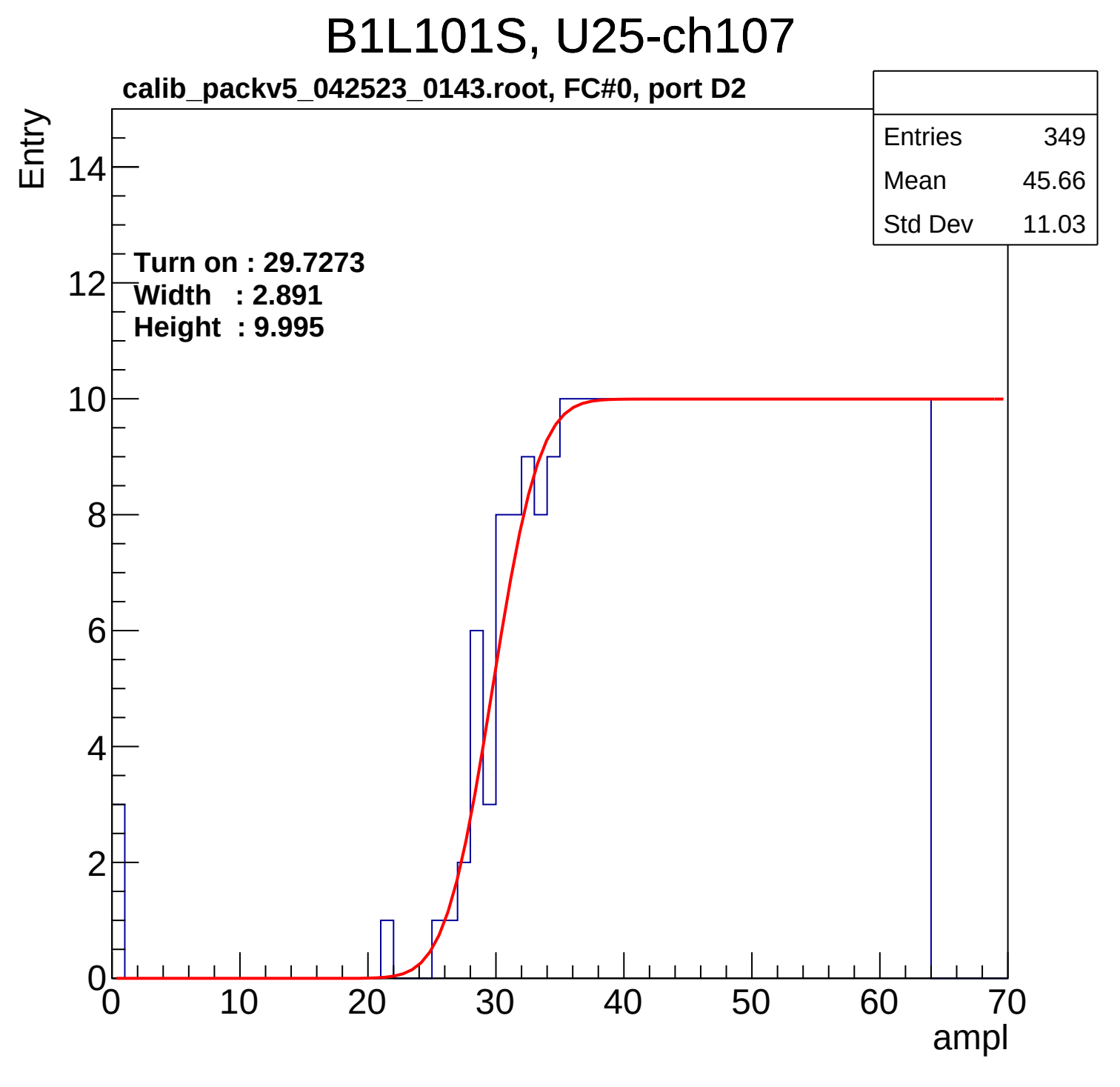
B1L101S, U25-ch107
calib_packv5_042523_0143.root, FC#0, port D2
Entries 349
Mean 45.66
Std Dev 11.03
Turn on : 29.7273
Width : 2.891
Height : 9.995
Entry
ampl
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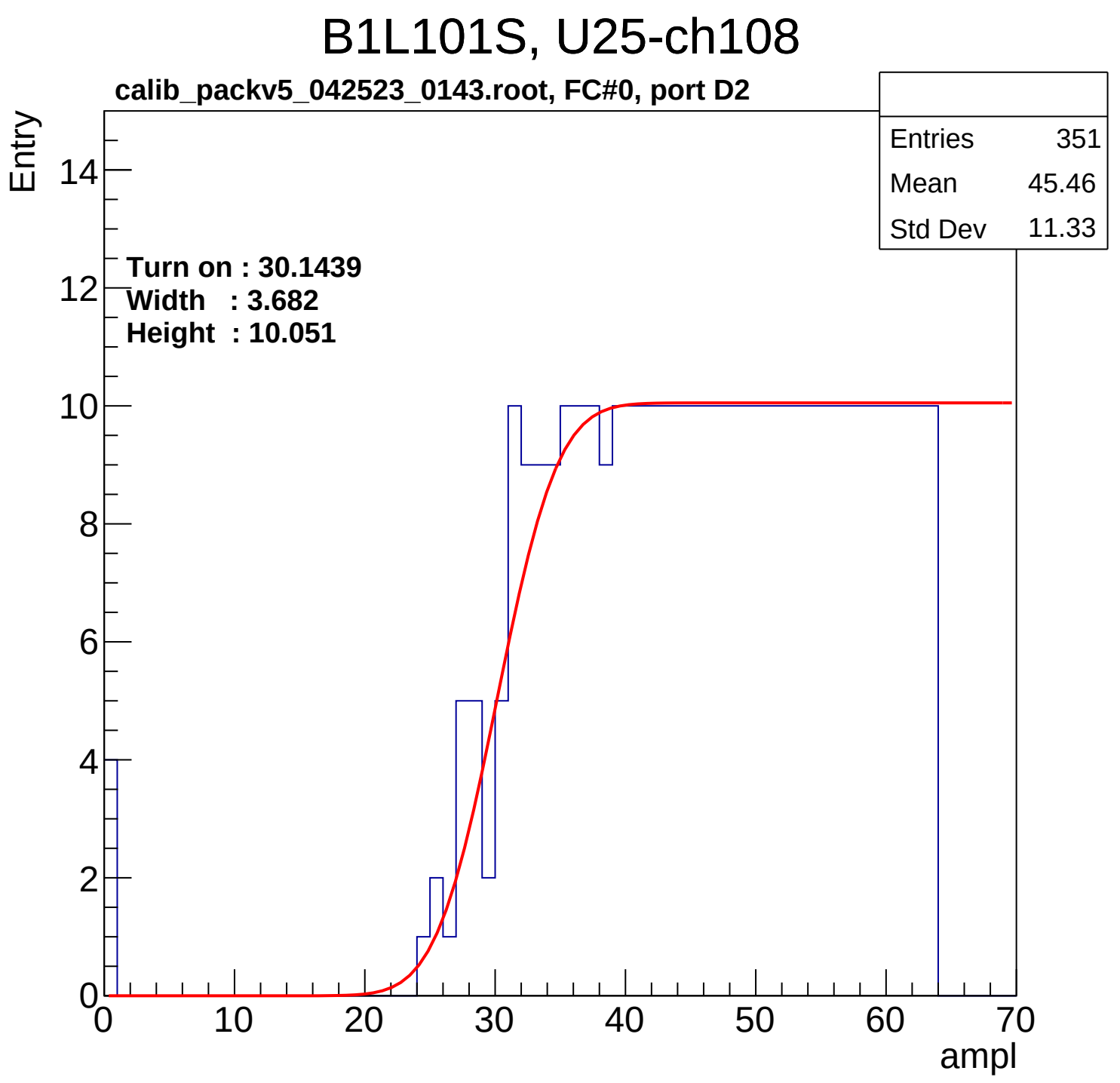
B1L101S, U25-ch108
calib_packv5_042523_0143.root, FC#0, port D2
Entries 351
Mean 45.46
Std Dev 11.33
Turn on : 30.1439
Width : 3.682
Height : 10.051
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ampl
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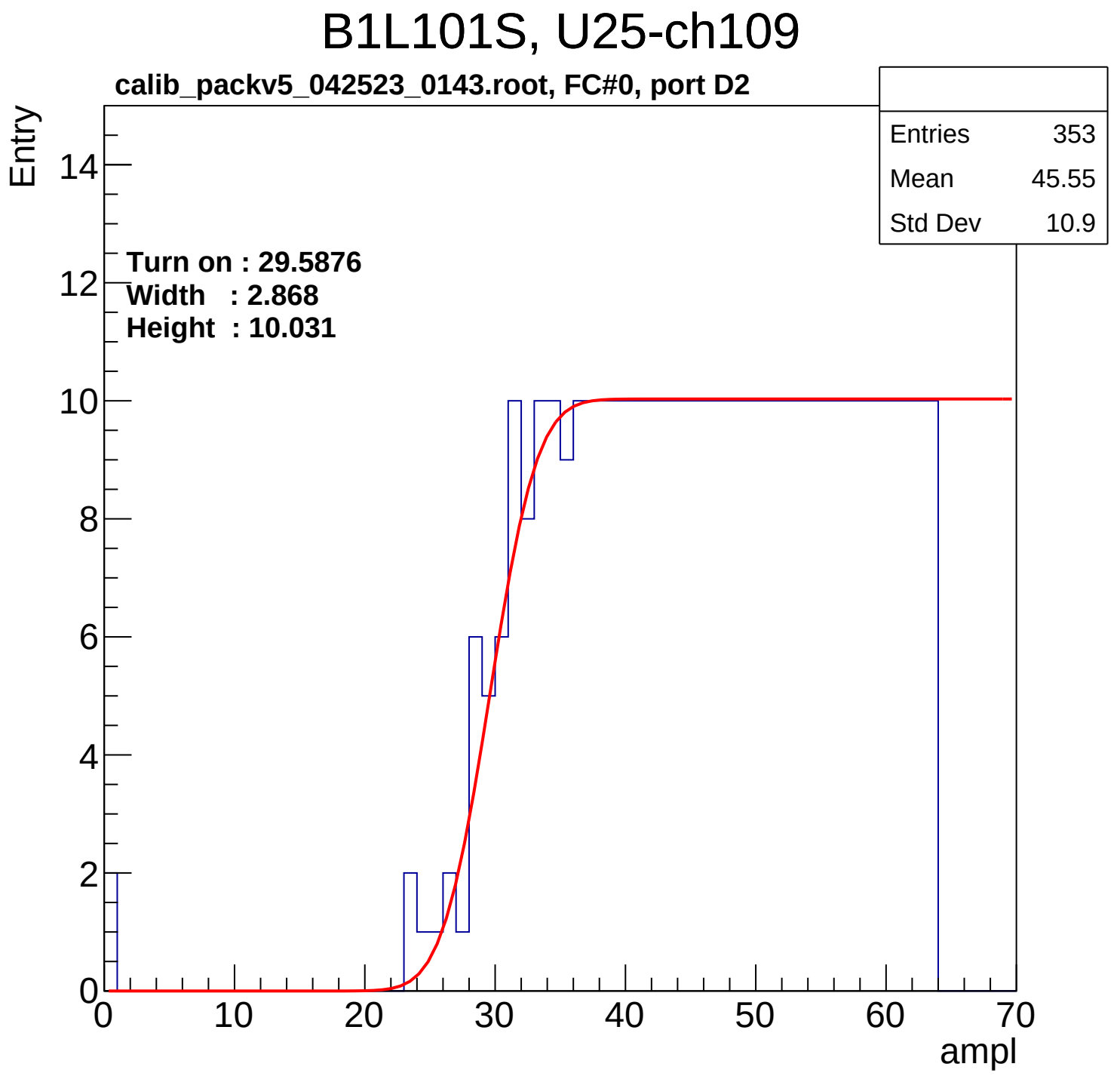
B1L101S, U25-ch109
calib_packv5_042523_0143.root, FC#0, port D2
Entries 353
Mean 45.55
Std Dev 10.9
Turn on : 29.5876
Width : 2.868
Height : 10.031
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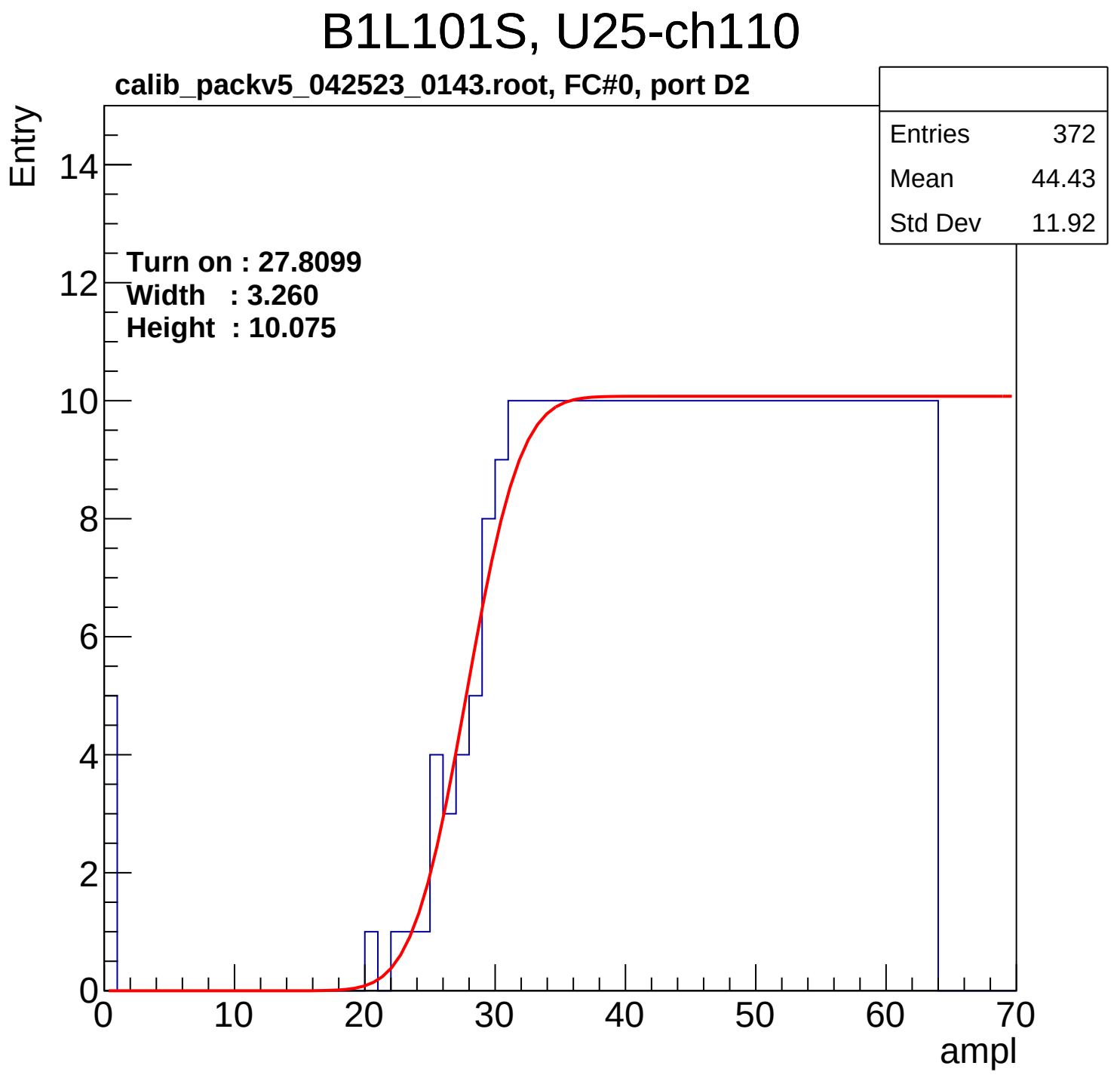
B1L101S, U25-ch110
calib_packv5_042523_0143.root, FC#0, port D2
Entries 372
Mean 44.43
Std Dev 11.92
Turn on : 27.8099
Width : 3.260
Height : 10.075
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ampl
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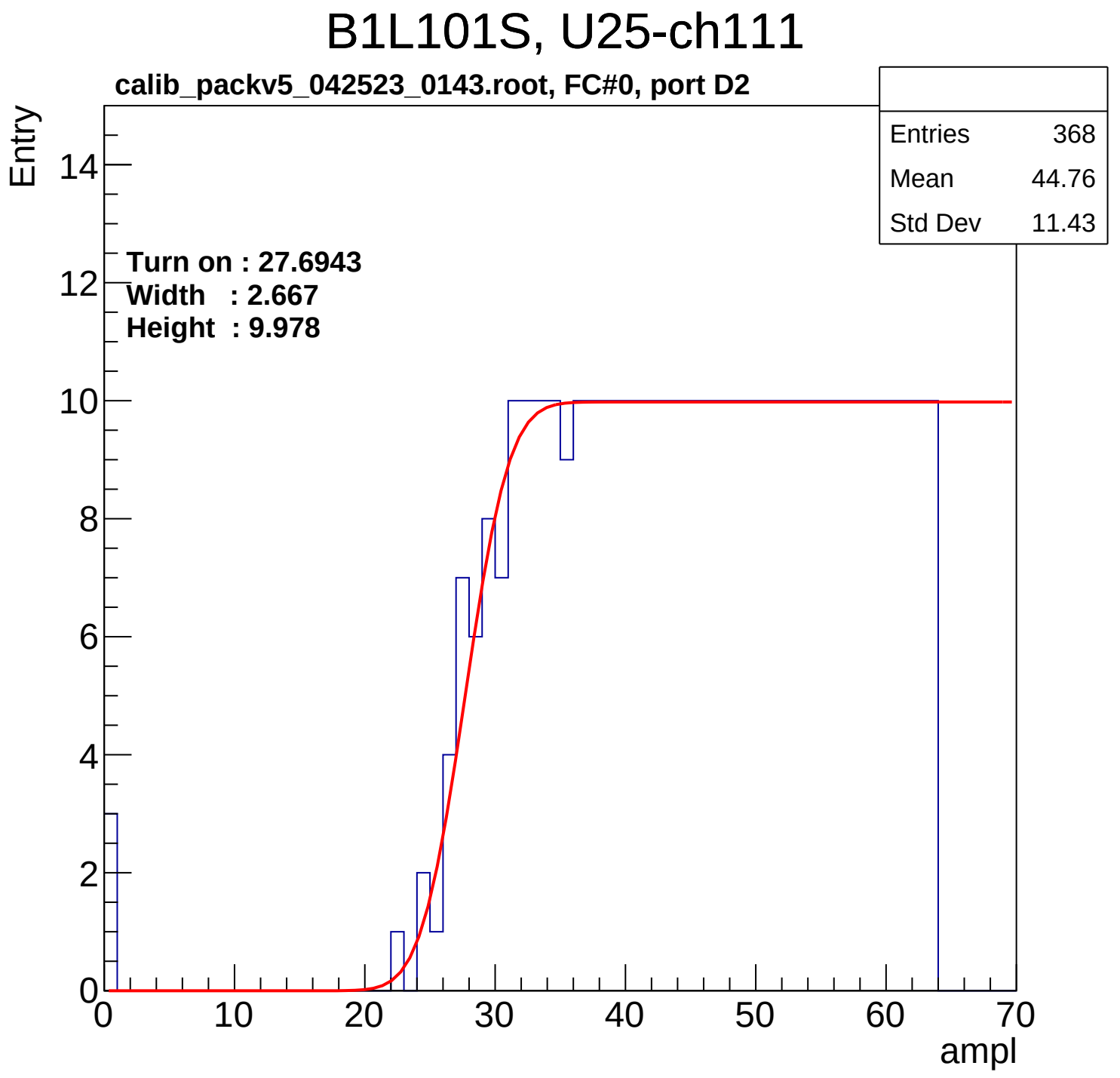
B1L101S, U25-ch111
calib_packv5_042523_0143.root, FC#0, port D2
Entries 368
Mean 44.76
Std Dev 11.43
Turn on : 27.6943
Width : 2.667
Height : 9.978
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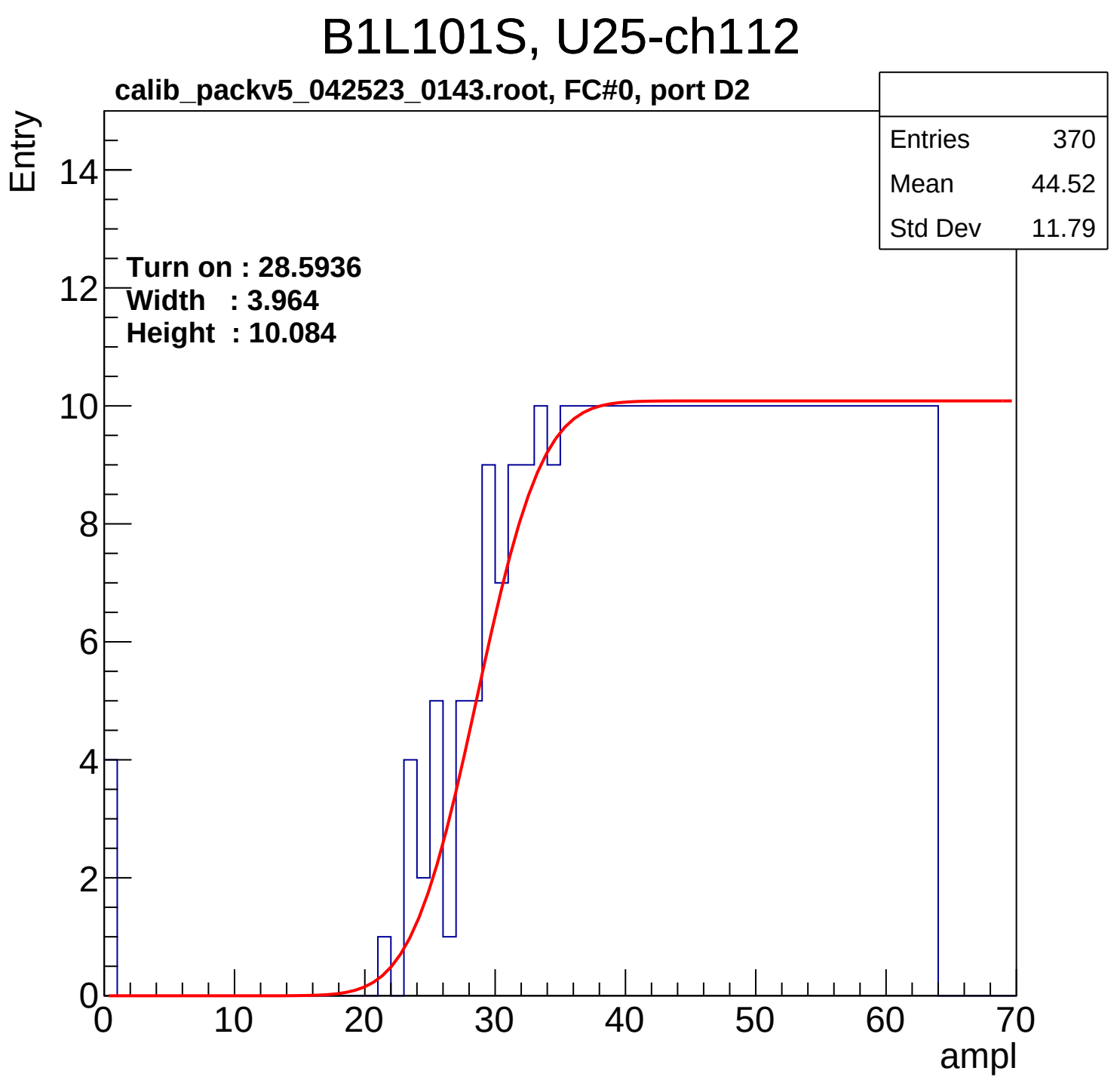
B1L101S, U25-ch112
calib_packv5_042523_0143.root, FC#0, port D2
Entries 370
Mean 44.52
Std Dev 11.79
Turn on : 28.5936
Width : 3.964
Height : 10.084
Entry
ampl
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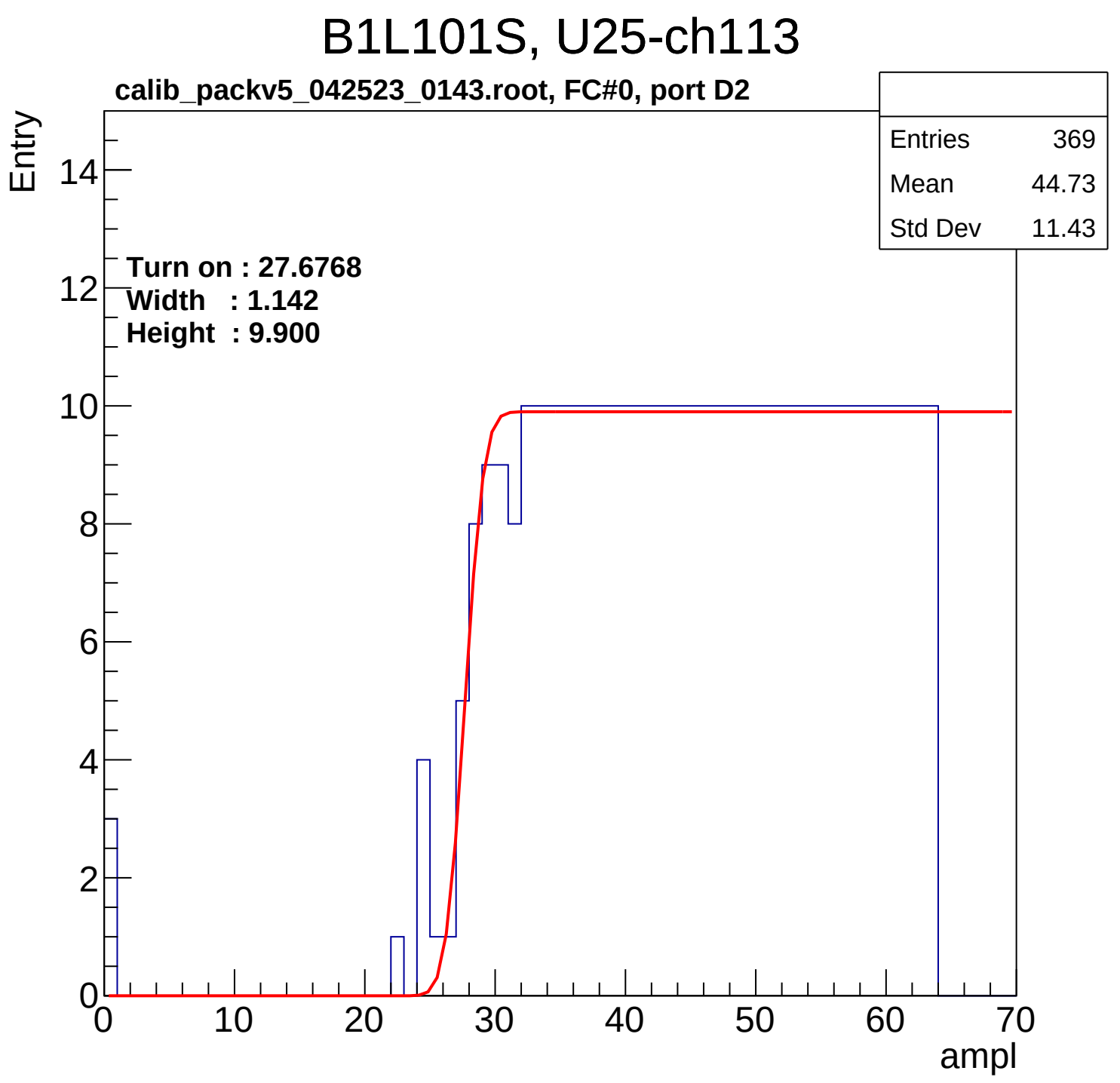
B1L101S, U25-ch113
calib_packv5_042523_0143.root, FC#0, port D2
Entries 369
Mean 44.73
Std Dev 11.43
Turn on : 27.6768
Width : 1.142
Height : 9.900
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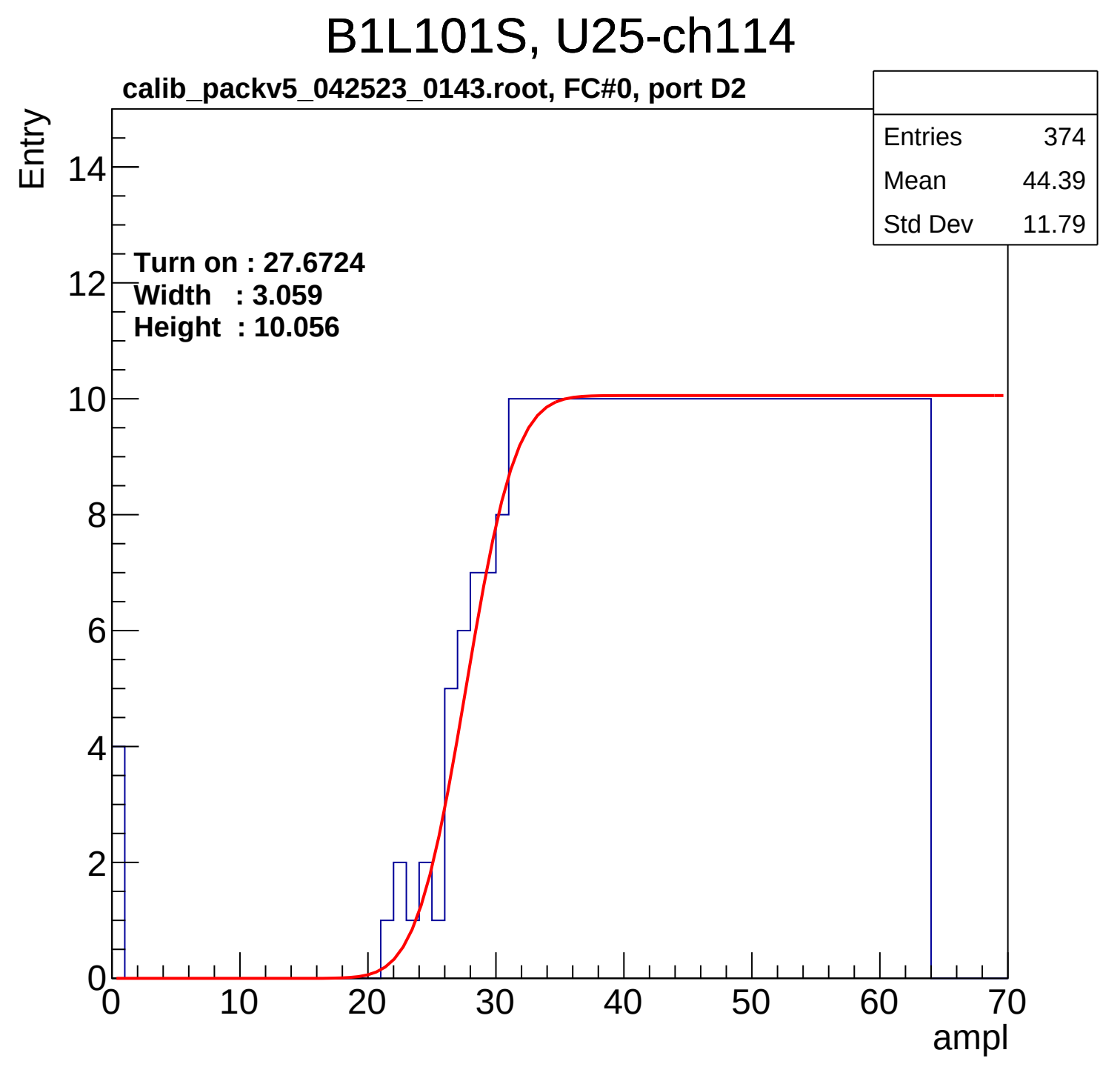
B1L101S, U25-ch114
calib_packv5_042523_0143.root, FC#0, port D2
Entries 374
Mean 44.39
Std Dev 11.79
Turn on : 27.6724
Width : 3.059
Height : 10.056
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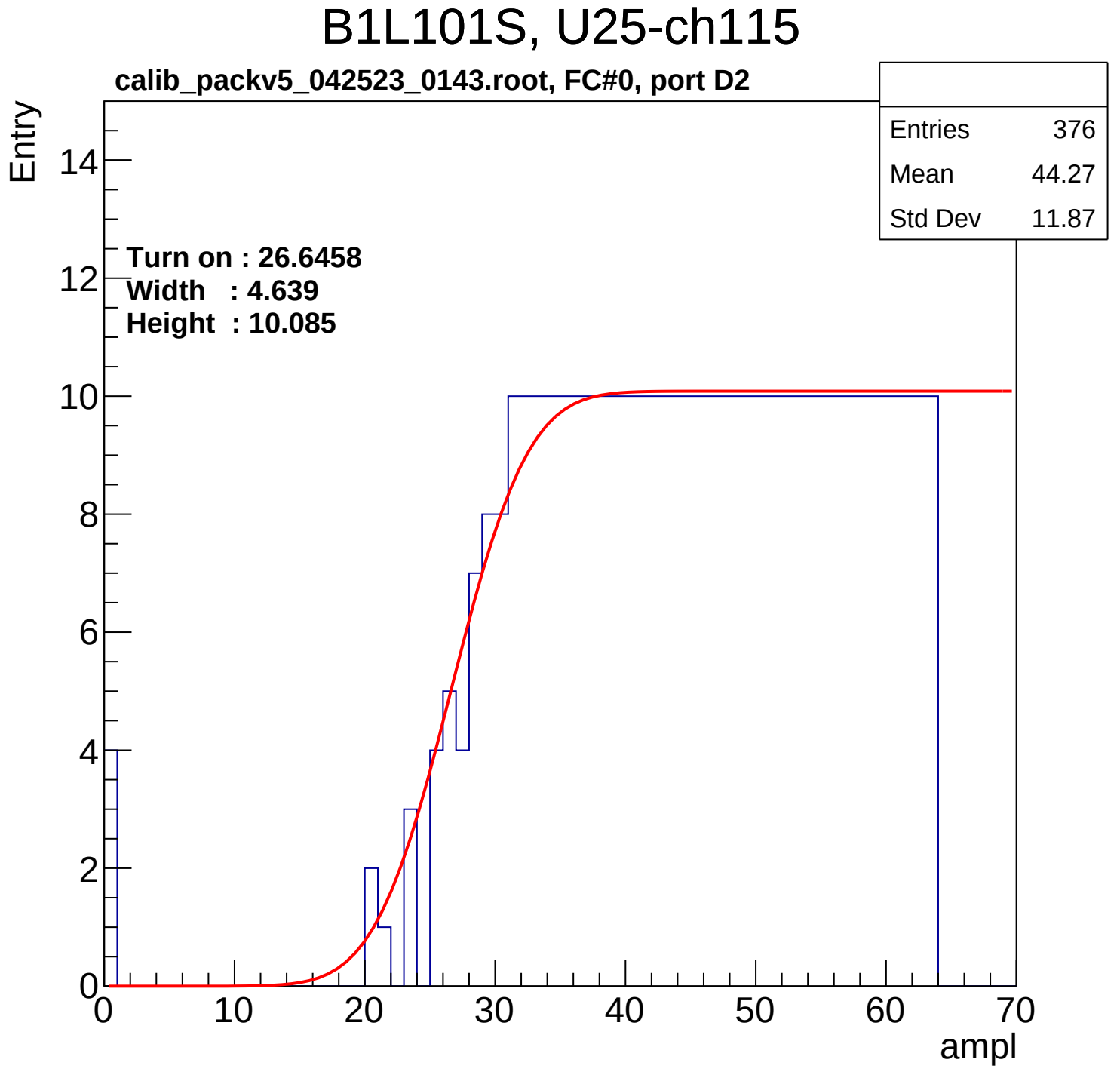
B1L101S, U25-ch115
calib_packv5_042523_0143.root, FC#0, port D2
Entries 376
Mean 44.27
Std Dev 11.87
Turn on : 26.6458
Width : 4.639
Height : 10.085
Entry
ampl
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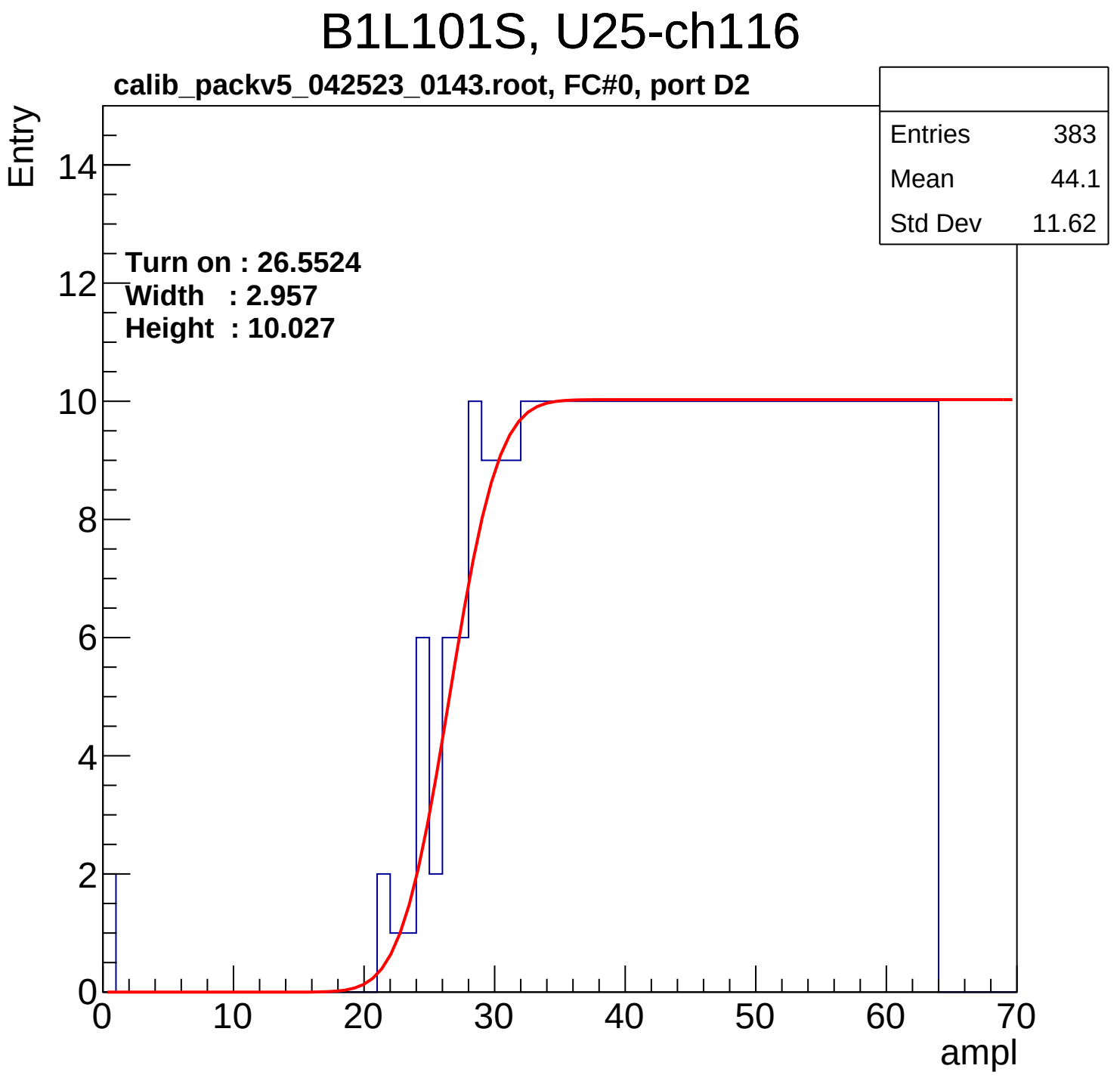
B1L101S, U25-ch116
calib_packv5_042523_0143.root, FC#0, port D2
Entries 383
Mean 44.1
Std Dev 11.62
Turn on : 26.5524
Width : 2.957
Height : 10.027
Entry
ampl
0
2
4
6
8
10
12
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0
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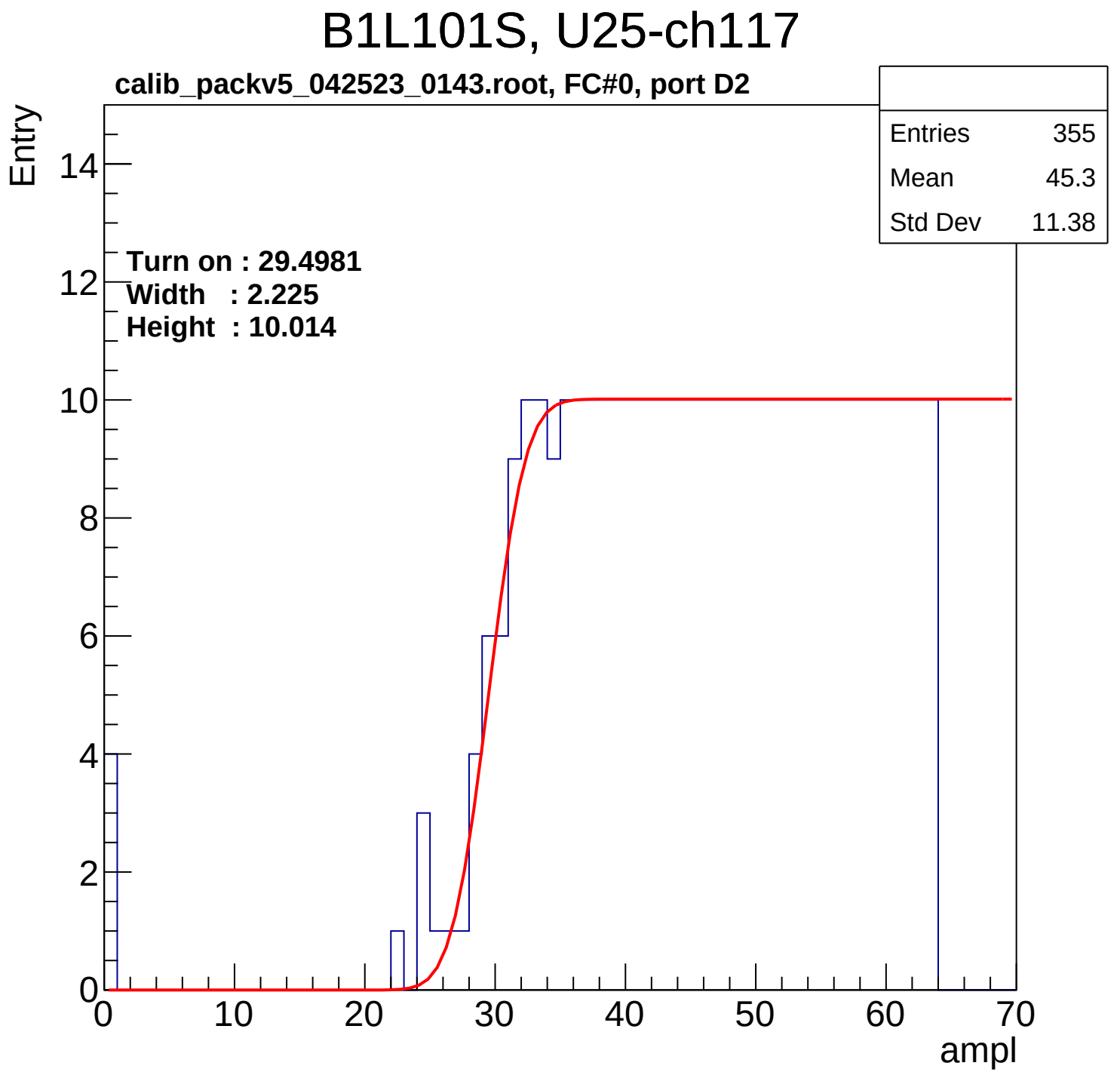
B1L101S, U25-ch117
calib_packv5_042523_0143.root, FC#0, port D2
Entries 355
Mean 45.3
Std Dev 11.38
Turn on : 29.4981
Width : 2.225
Height : 10.014
Entry
ampl
0
2
4
6
8
10
12
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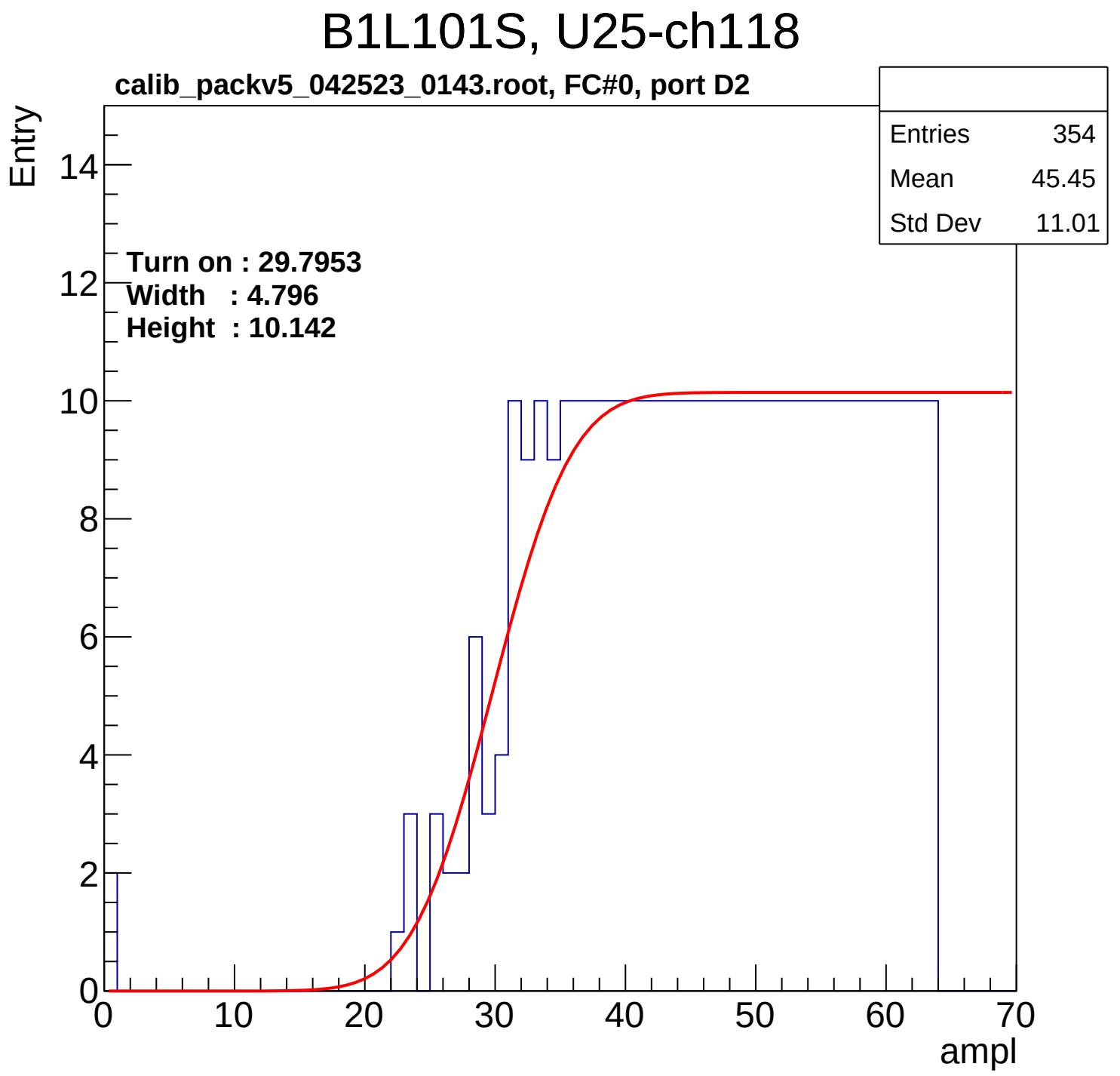
B1L101S, U25-ch118
calib_packv5_042523_0143.root, FC#0, port D2
Entries 354
Mean 45.45
Std Dev 11.01
Turn on : 29.7953
Width : 4.796
Height : 10.142
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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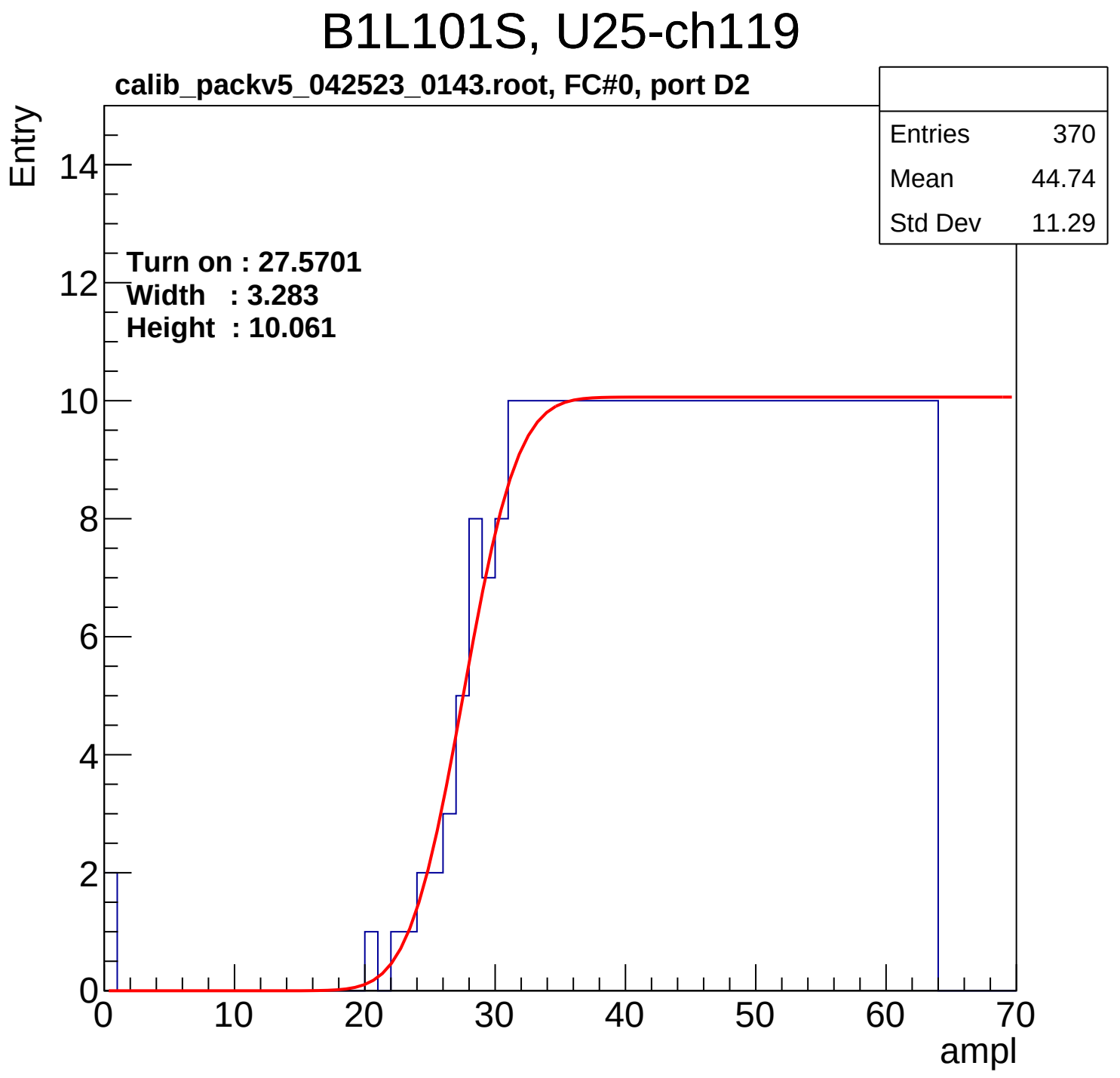
B1L101S, U25-ch119
calib_packv5_042523_0143.root, FC#0, port D2
Entries 370
Mean 44.74
Std Dev 11.29
Turn on : 27.5701
Width : 3.283
Height : 10.061
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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40
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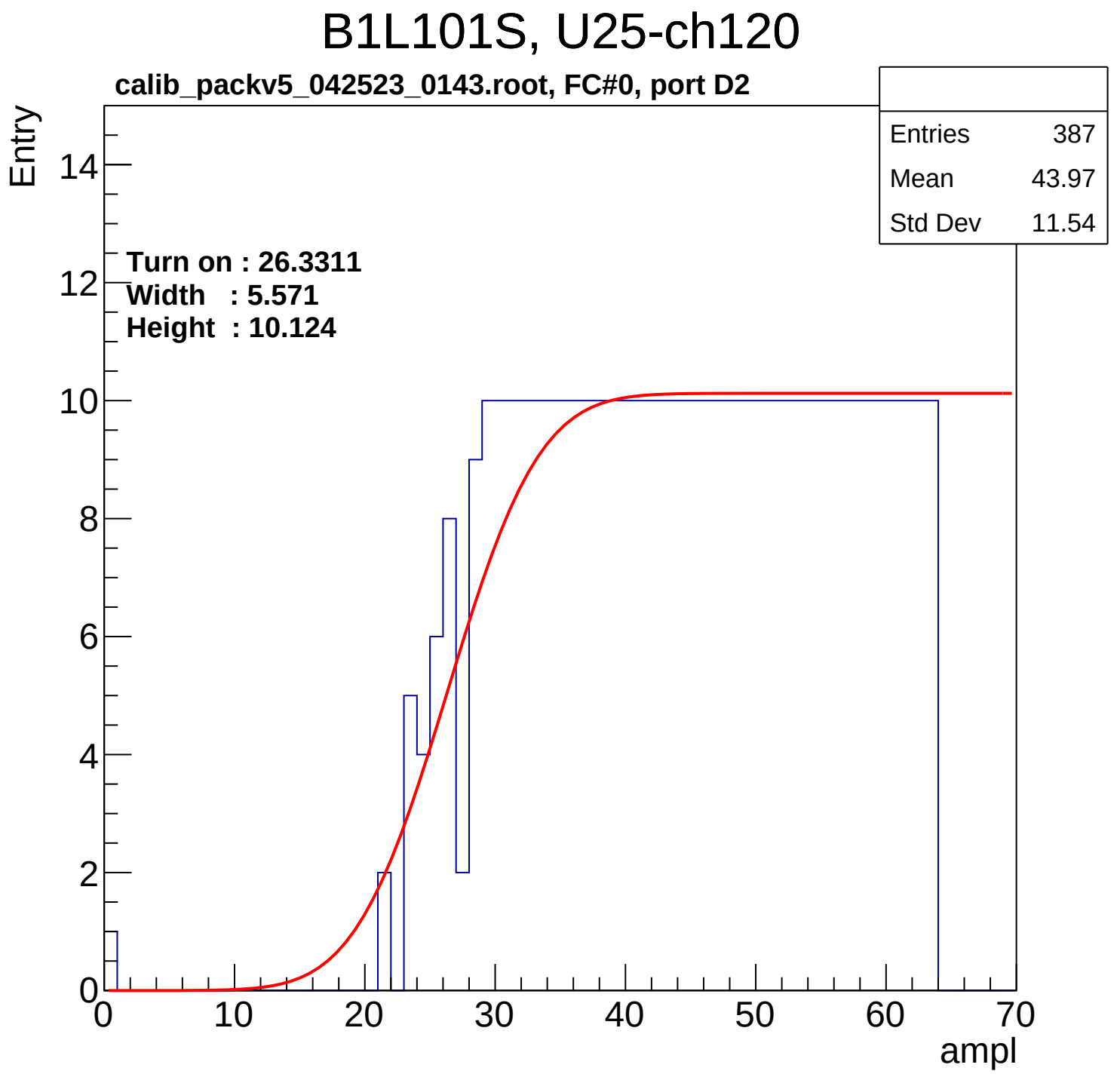
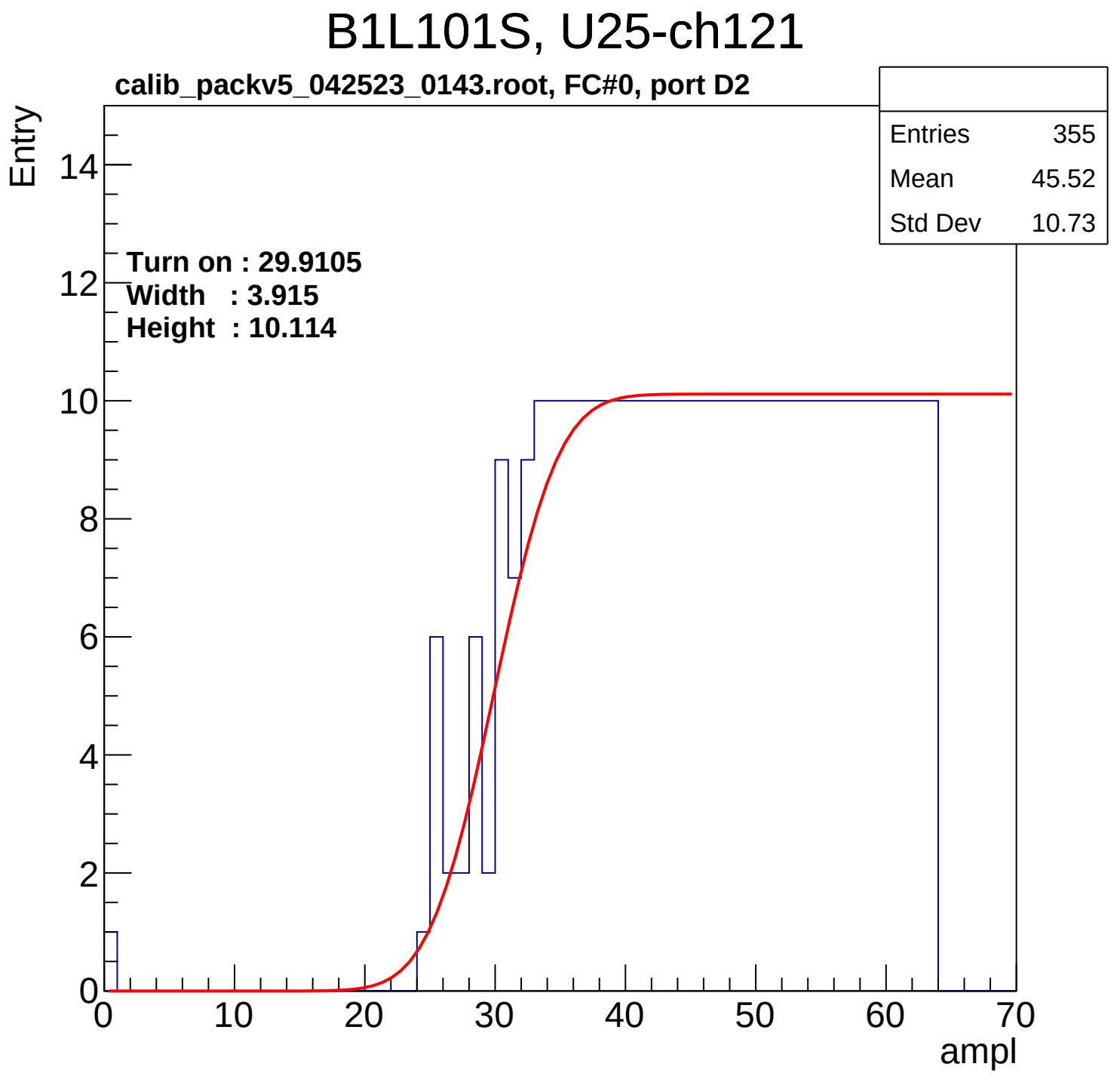
60
70


B1L101S, U25-ch120
calib_packv5_042523_0143.root, FC#0, port D2
Entries 387
Mean 43.97
Std Dev 11.54
Turn on : 26.3311
Width : 5.571
Height : 10.124
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L101S, U25-ch121
calib_packv5_042523_0143.root, FC#0, port D2
Entries 355
Mean 45.52
Std Dev 10.73
Turn on : 29.9105
Width : 3.915
Height : 10.114
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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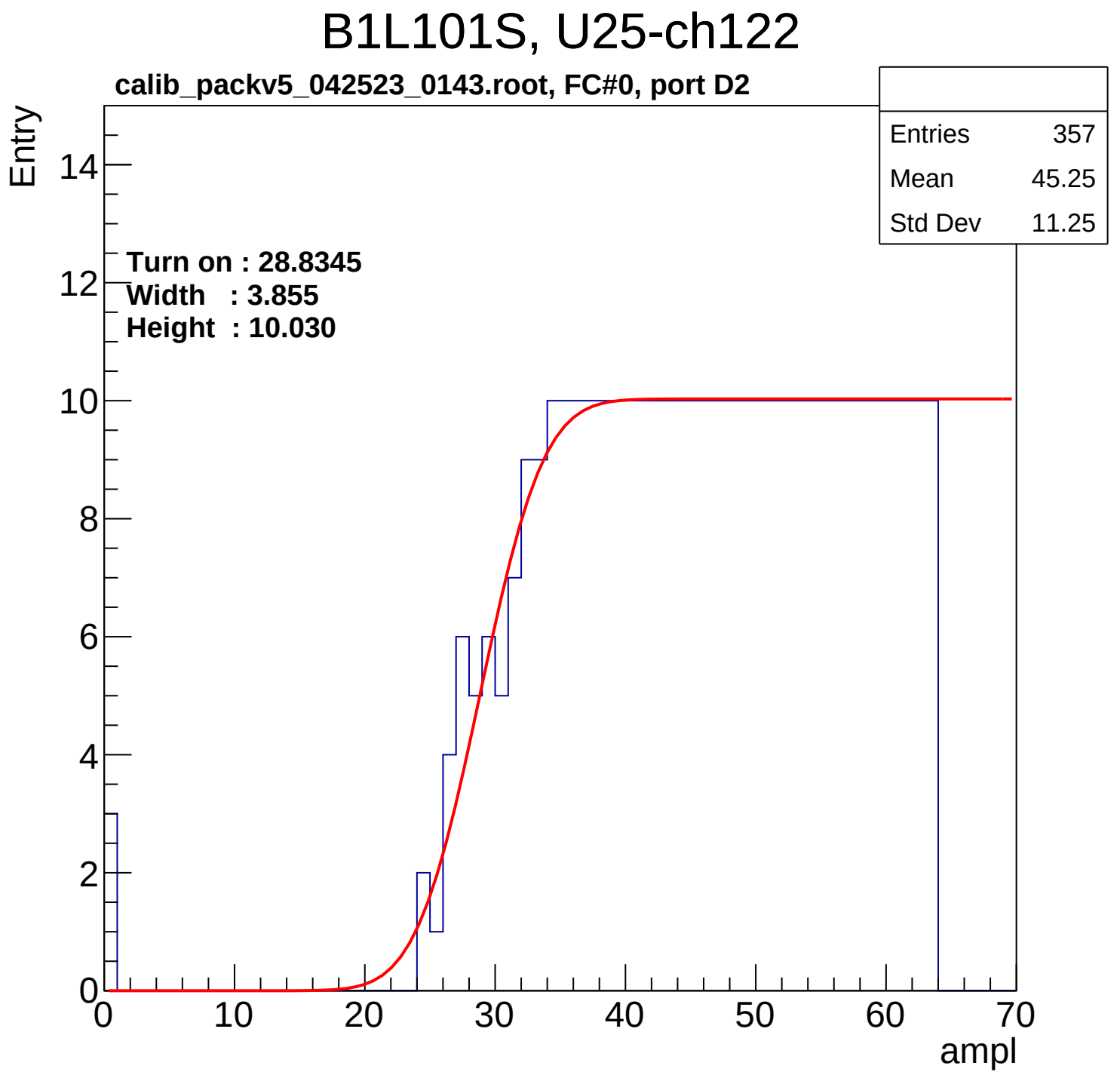
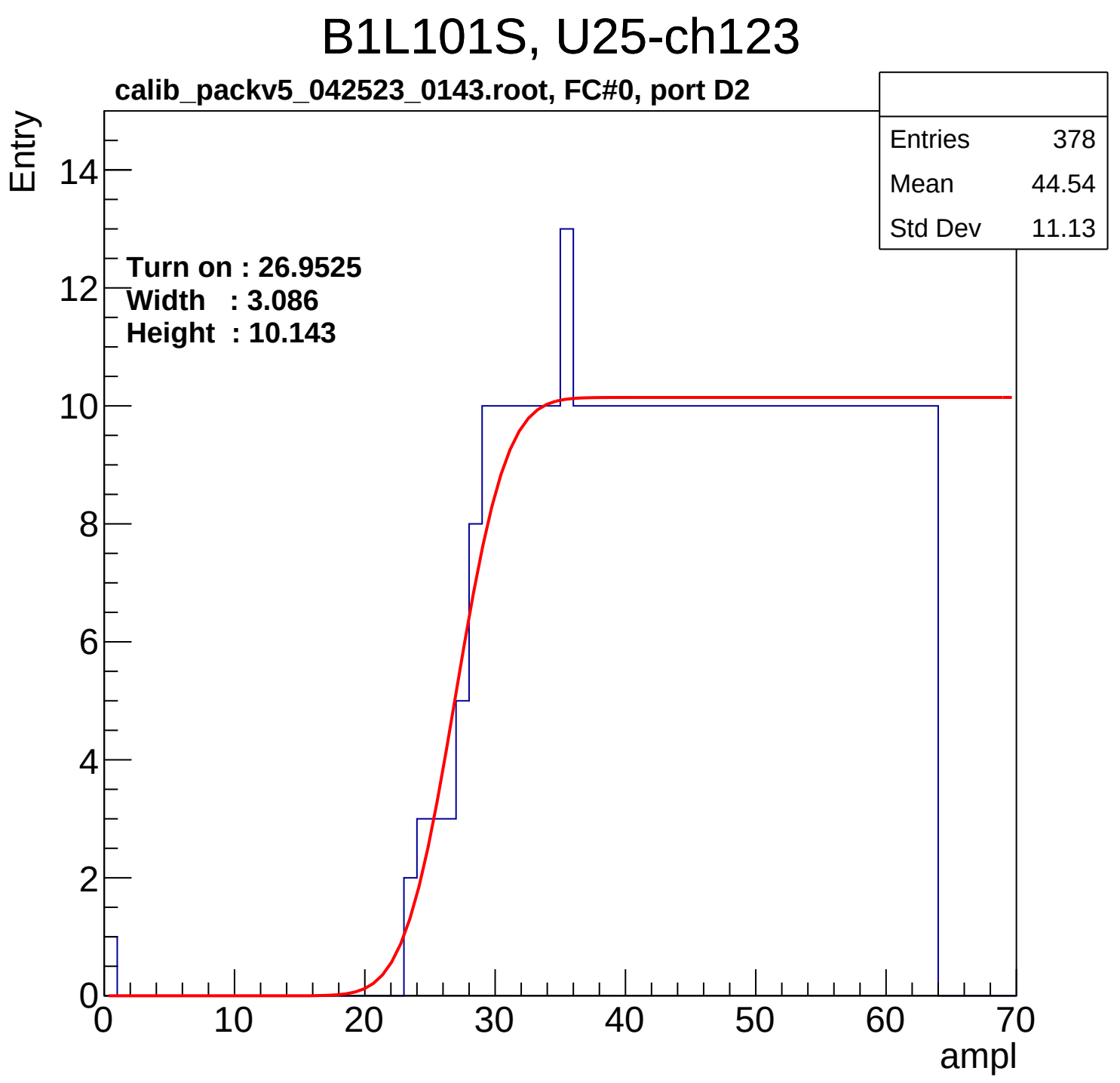
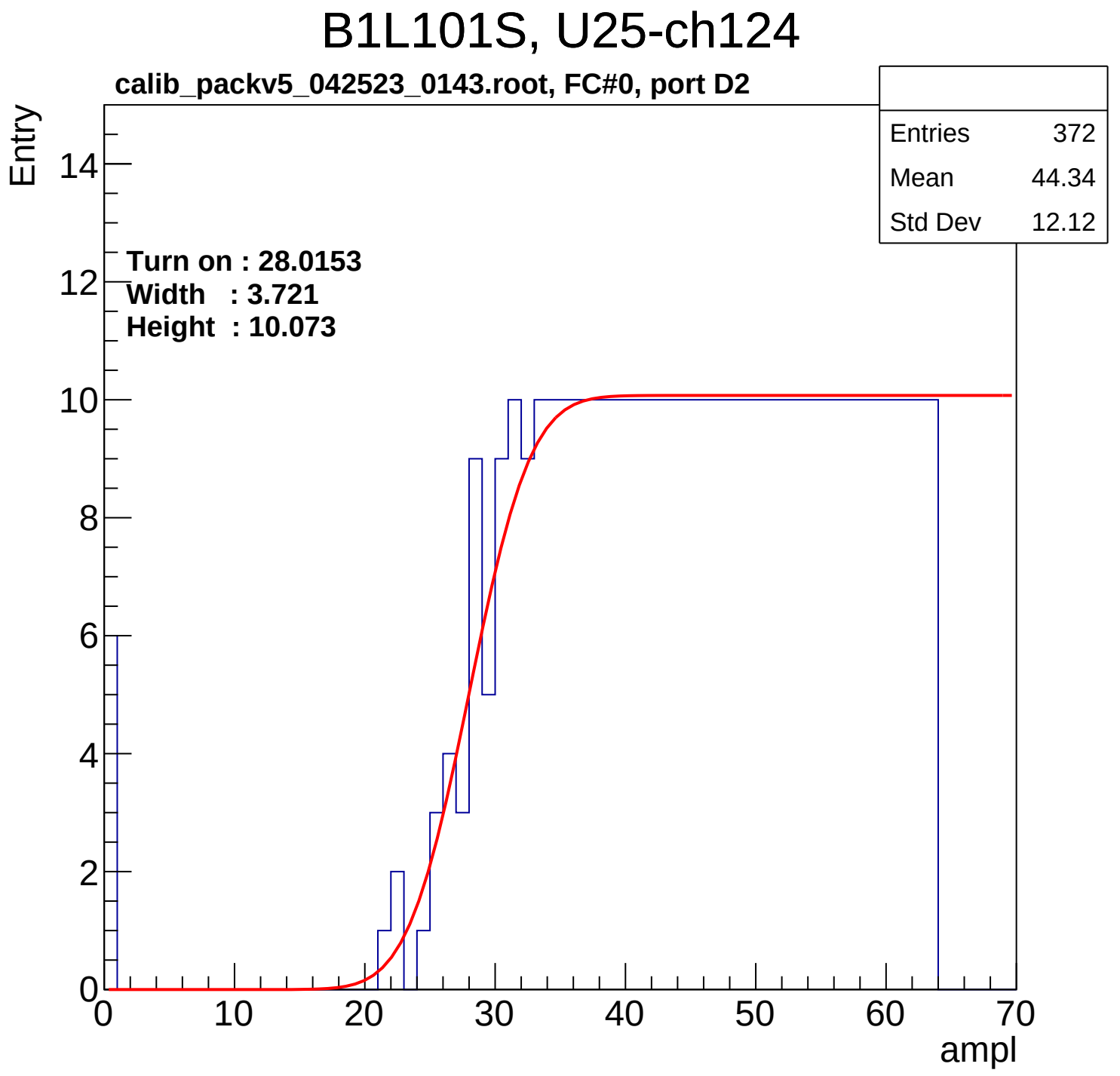
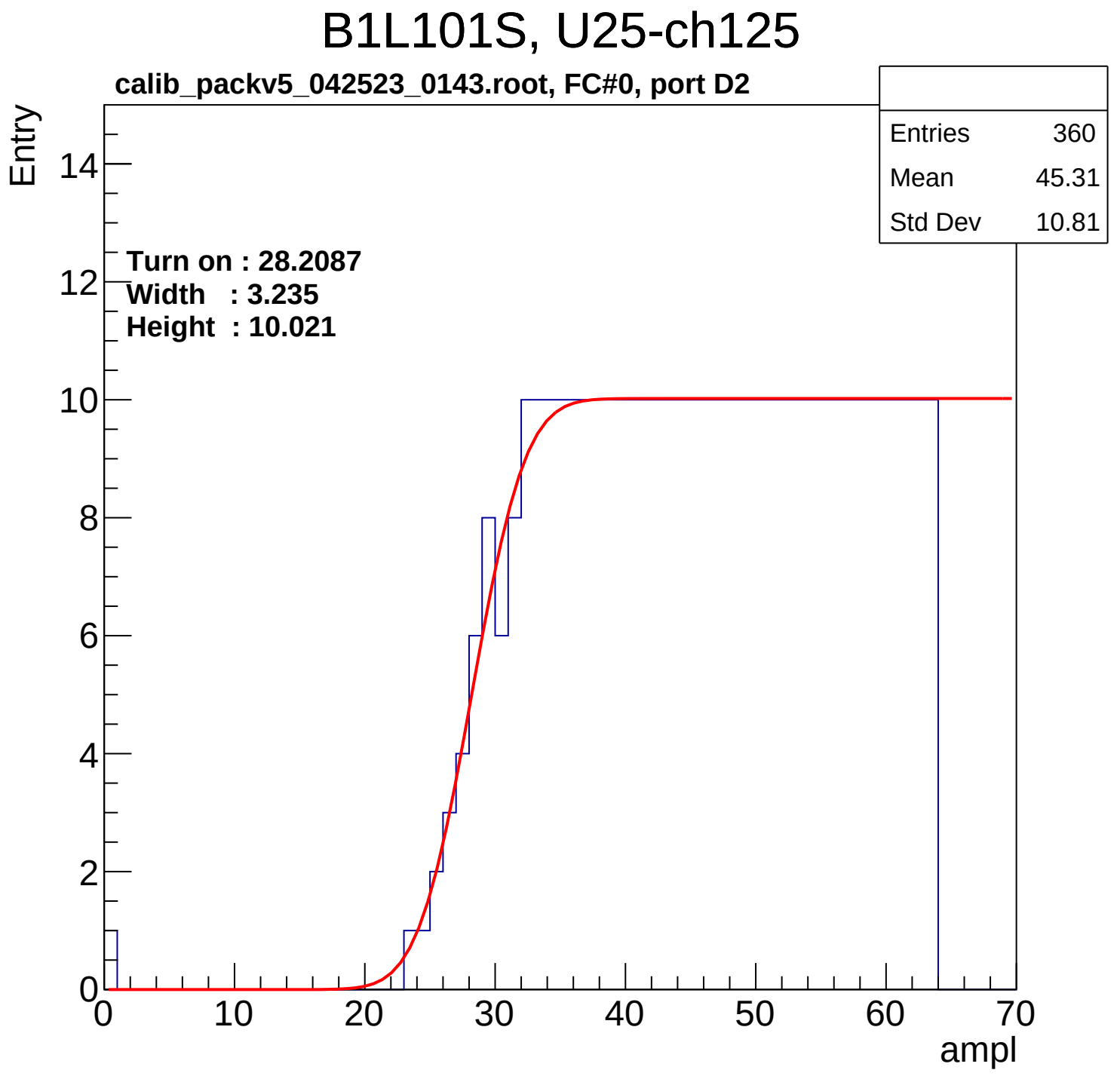
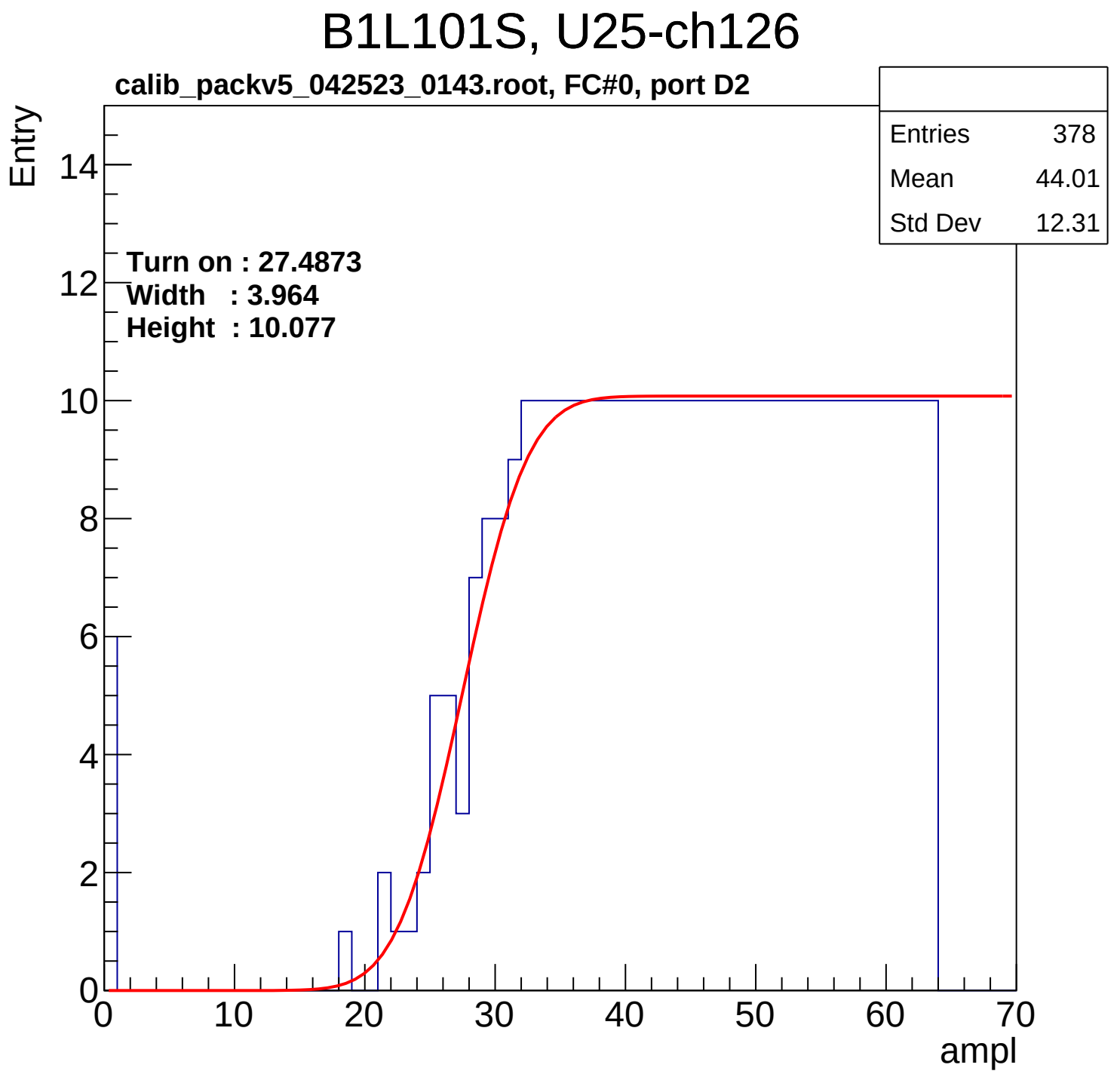

B1L101S, U25-ch122
calib_packv5_042523_0143.root, FC#0, port D2
Entries 357
Mean 45.25
Std Dev 11.25
Turn on : 28.8345
Width : 3.855
Height : 10.030
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L101S, U25-ch123
calib_packv5_042523_0143.root, FC#0, port D2
Entries 378
Mean 44.54
Std Dev 11.13
Turn on : 26.9525
Width : 3.086
Height : 10.143
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L101S, U25-ch124
calib_packv5_042523_0143.root, FC#0, port D2
Entries 372
Mean 44.34
Std Dev 12.12
Turn on : 28.0153
Width : 3.721
Height : 10.073
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L101S, U25-ch125
calib_packv5_042523_0143.root, FC#0, port D2
Entries 360
Mean 45.31
Std Dev 10.81
Turn on : 28.2087
Width : 3.235
Height : 10.021
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L101S, U25-ch126
calib_packv5_042523_0143.root, FC#0, port D2
Entries 378
Mean 44.01
Std Dev 12.31
Turn on : 27.4873
Width : 3.964
Height : 10.077
Entry
ampl
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2
4
6
8
10
12
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0
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20
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60
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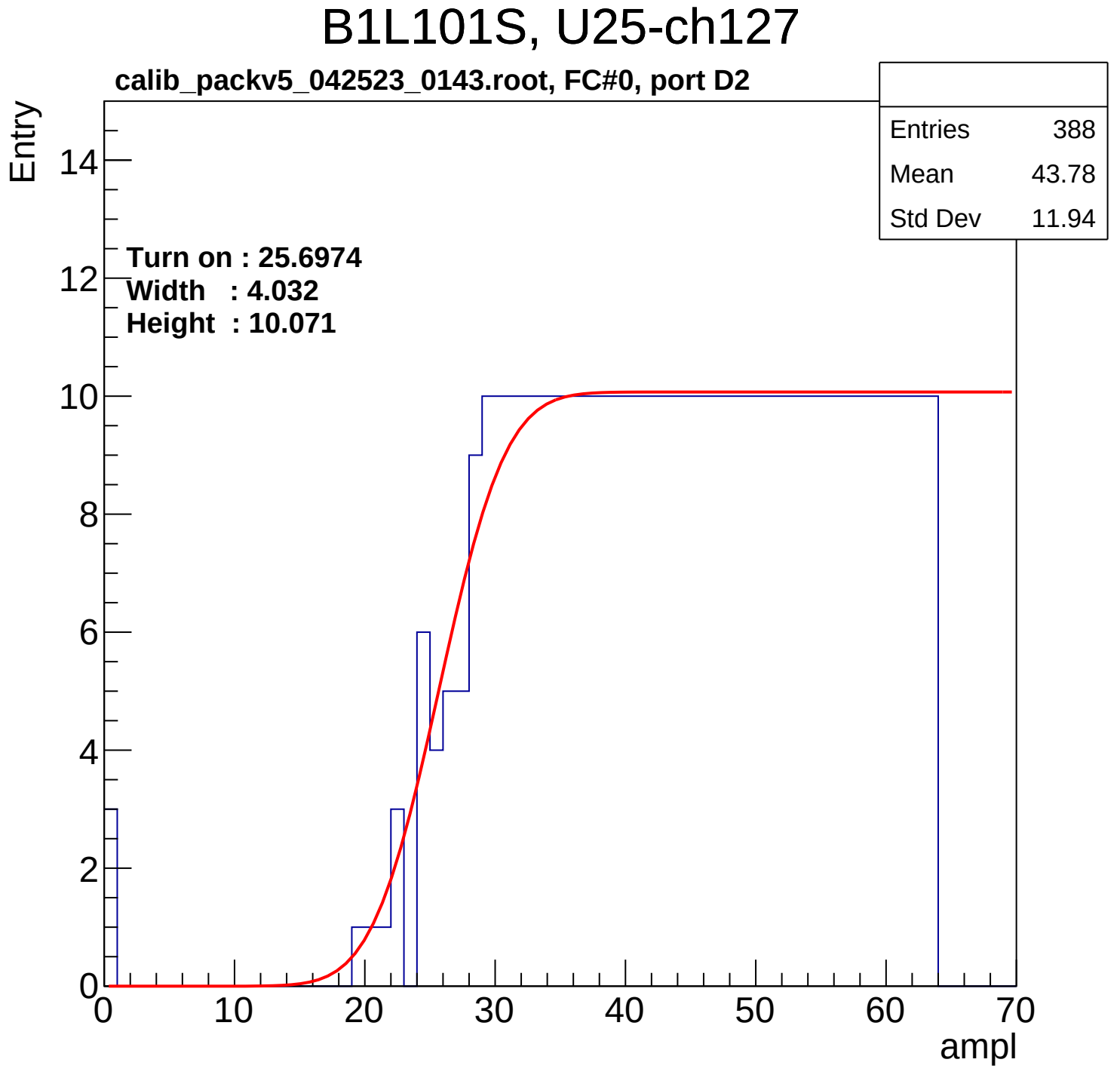
B1L101S, U25-ch127
calib_packv5_042523_0143.root, FC#0, port D2
Entries 388
Mean 43.78
Std Dev 11.94
Turn on : 25.6974
Width : 4.032
Height : 10.071
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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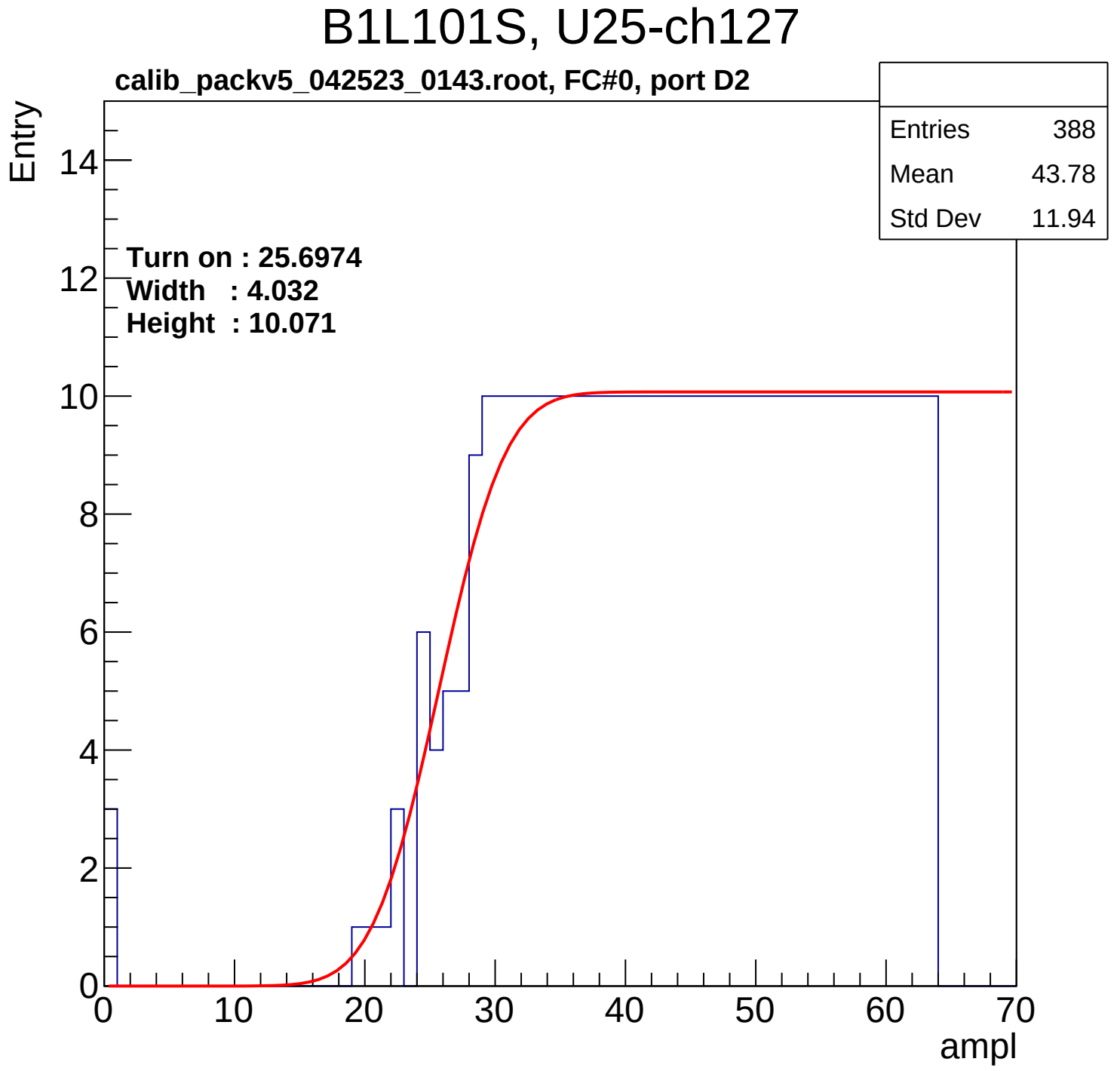
B1L101S, U25-ch127
calib_packv5_042523_0143.root, FC#0, port D2
Entries 388
Mean 43.78
Std Dev 11.94
Turn on : 25.6974
Width : 4.032
Height : 10.071
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70