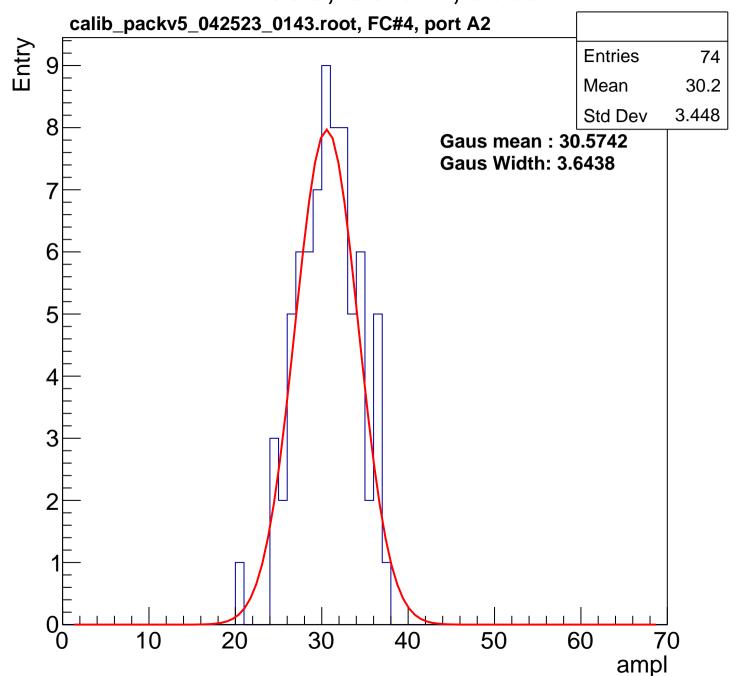
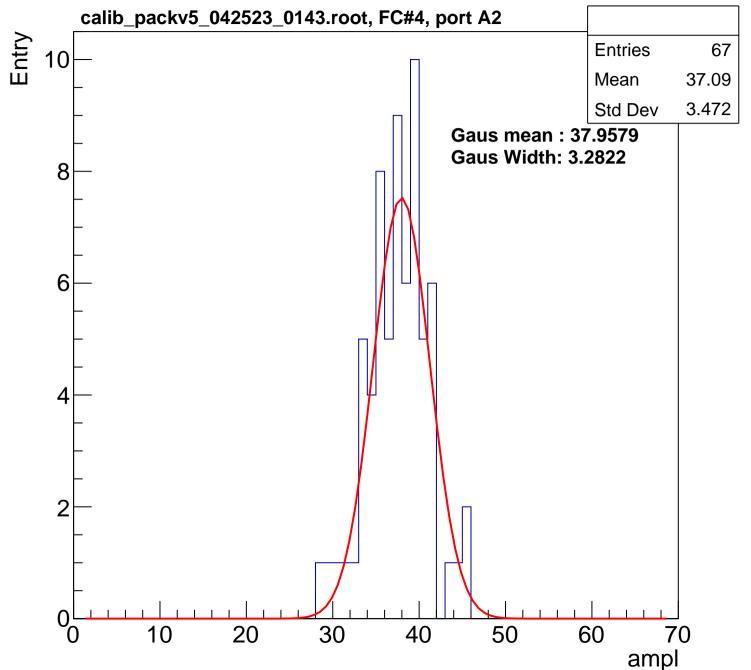
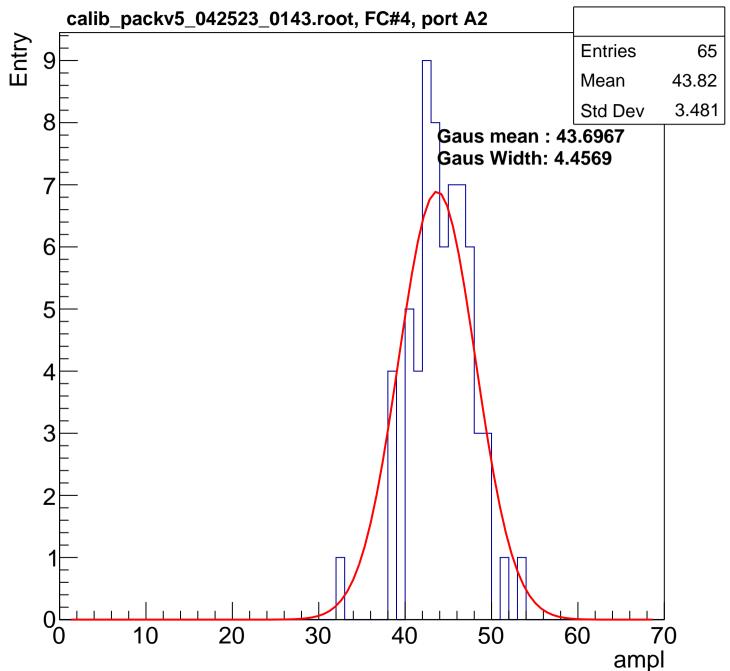
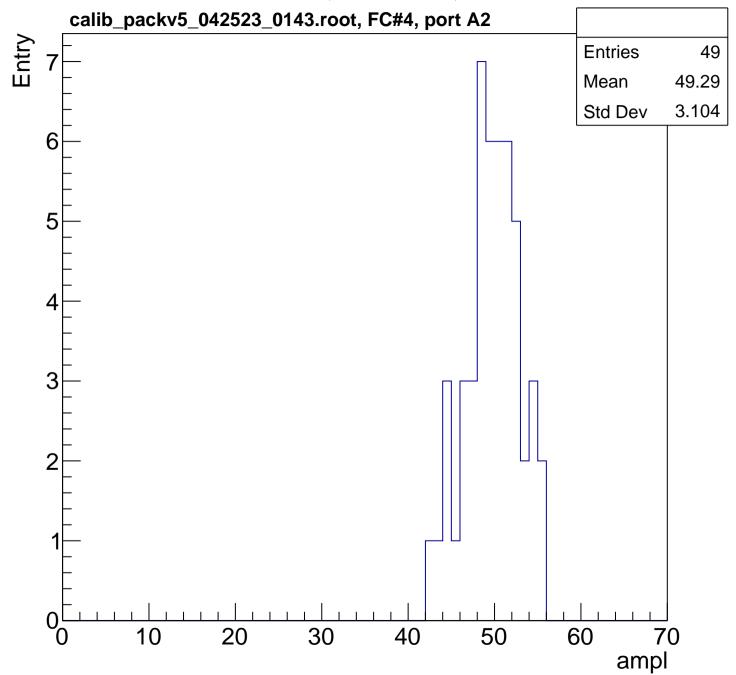


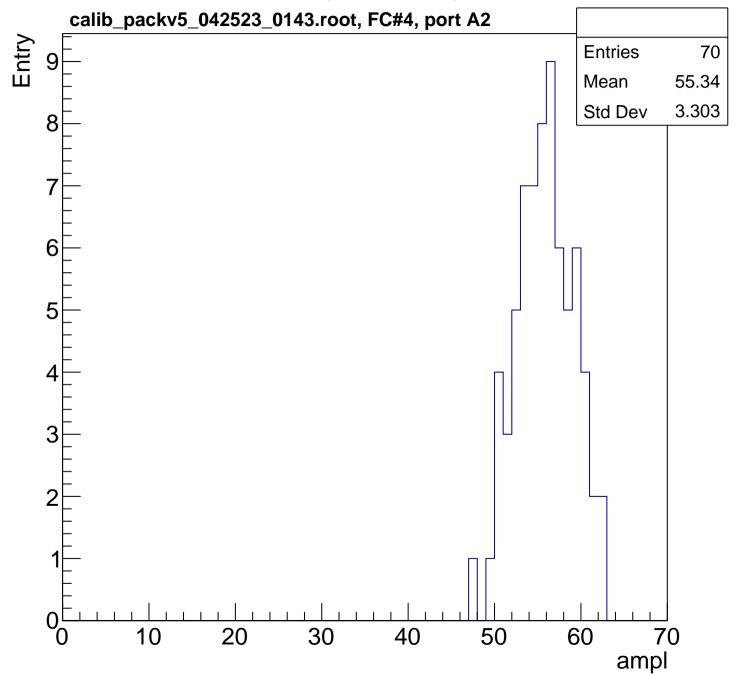
B1L100S, U8-ch0, adc7 calib_packv5_042523_0143.root, FC#4, port A2 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

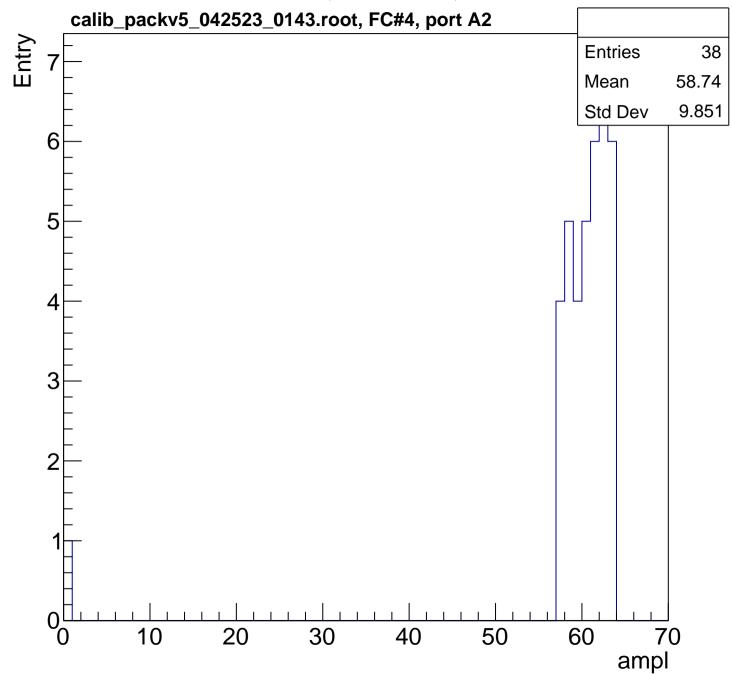


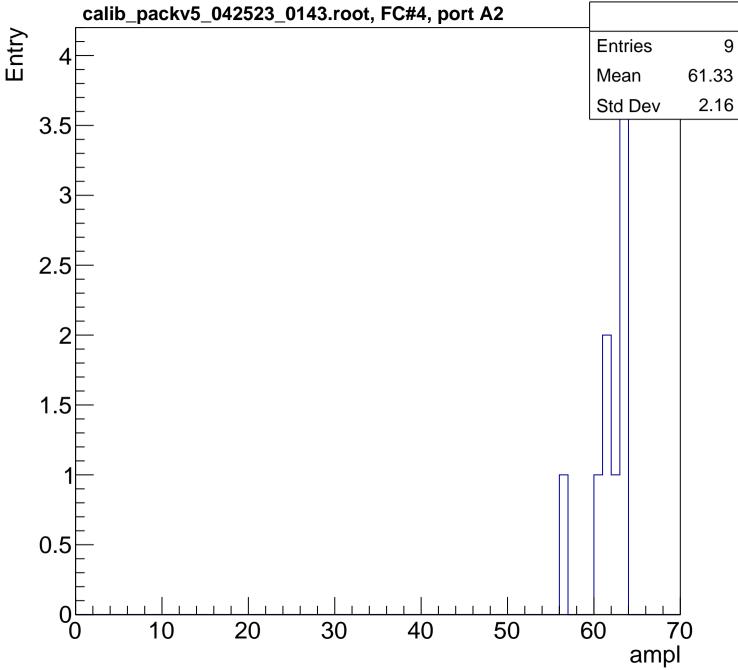


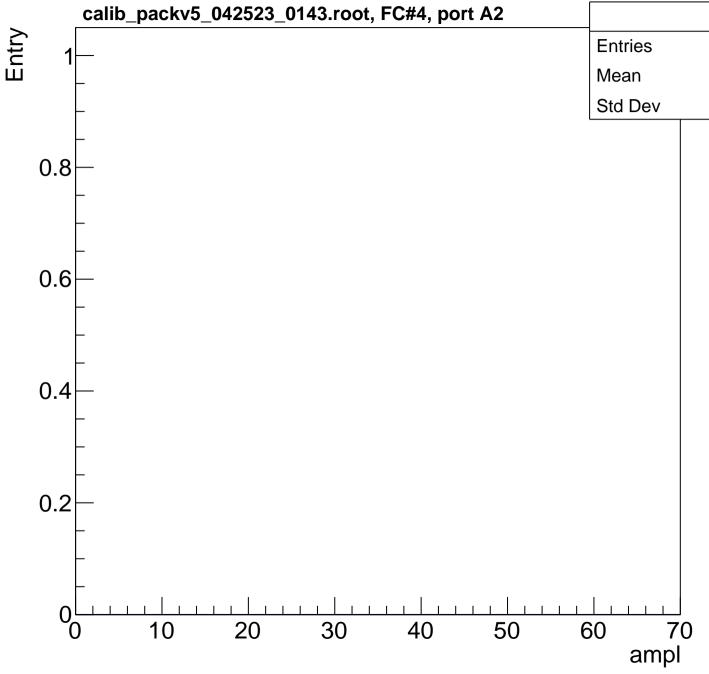


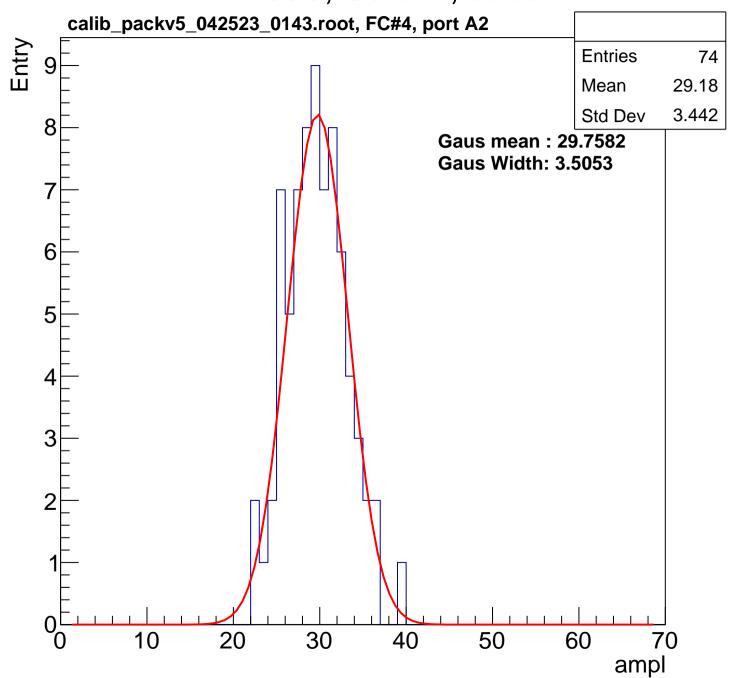


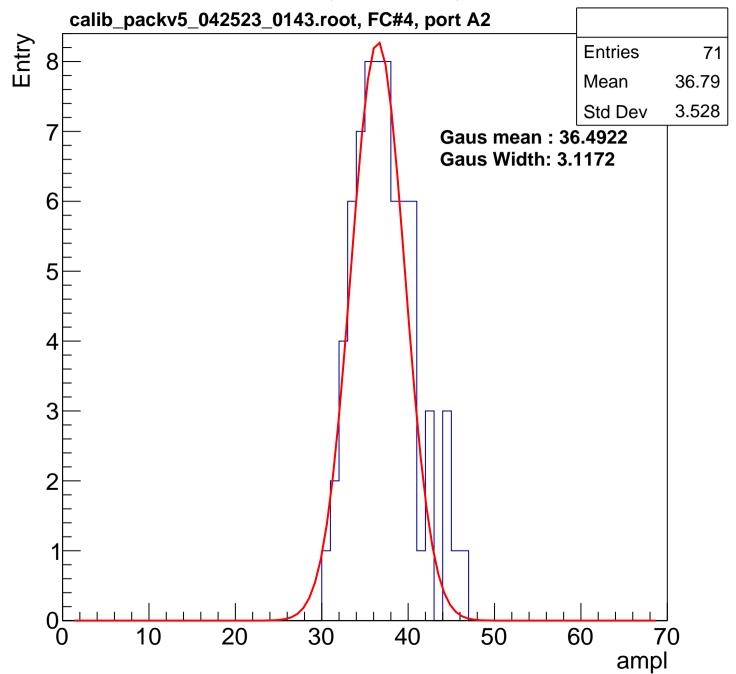


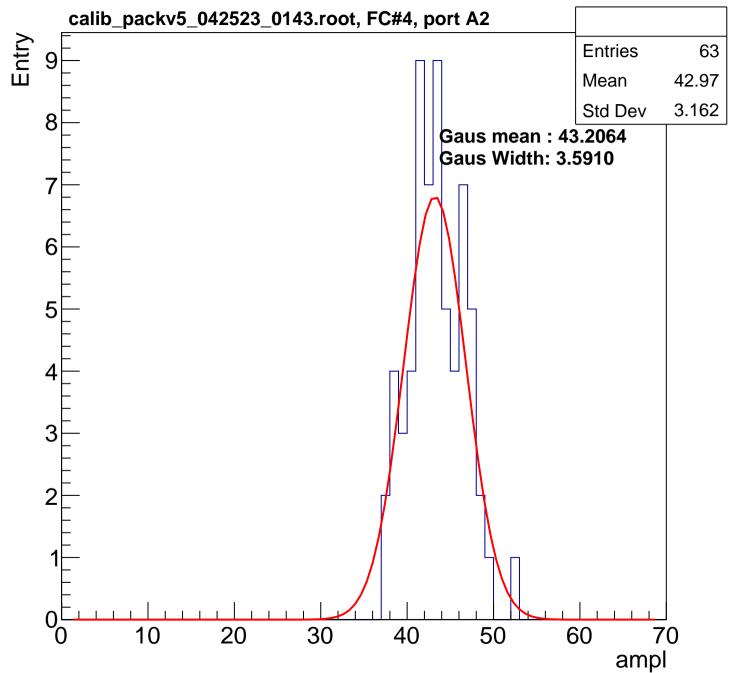


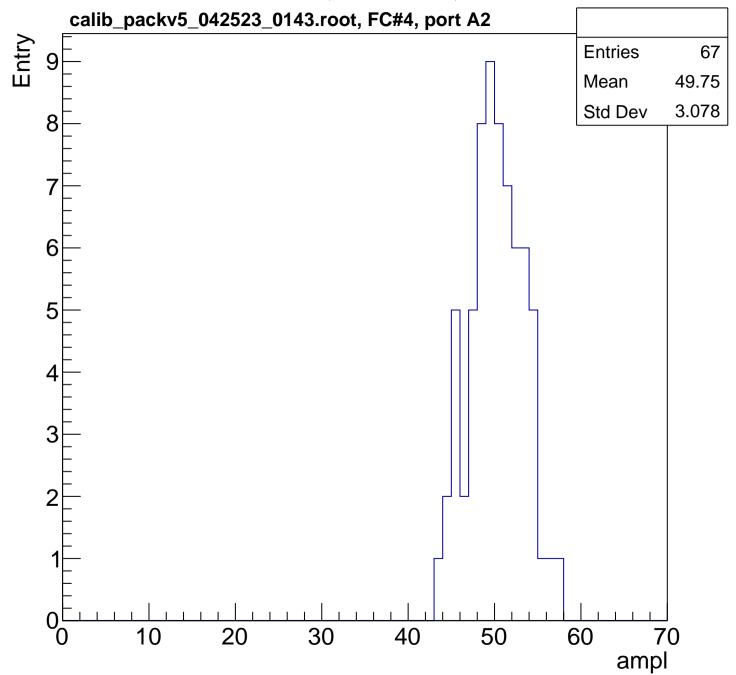


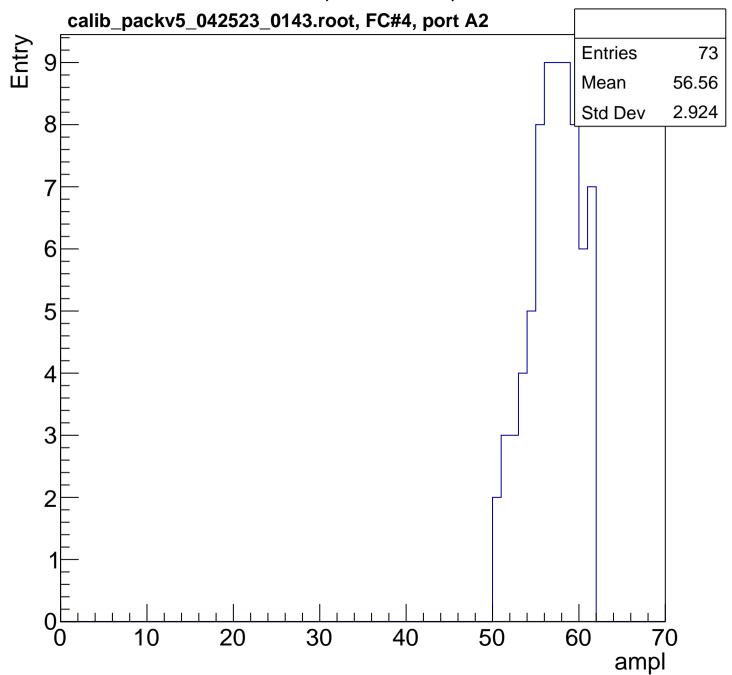


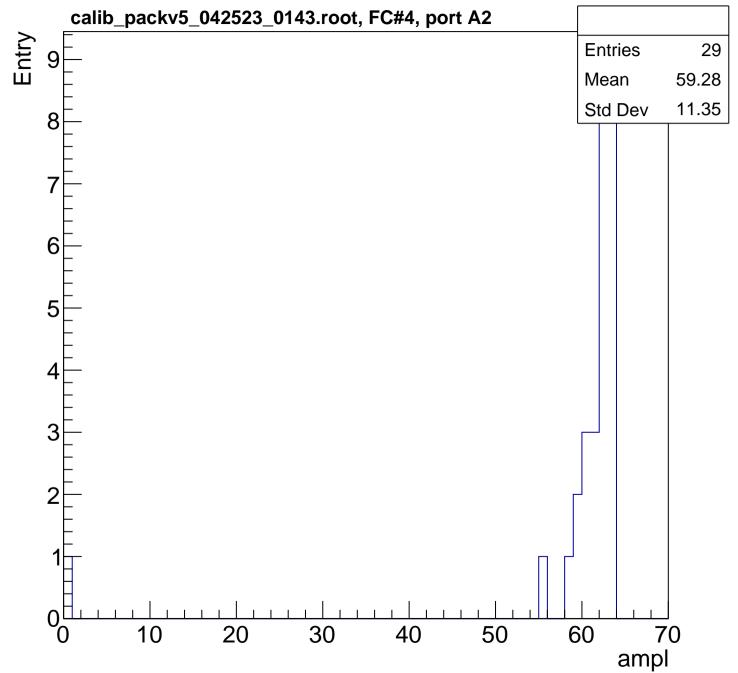


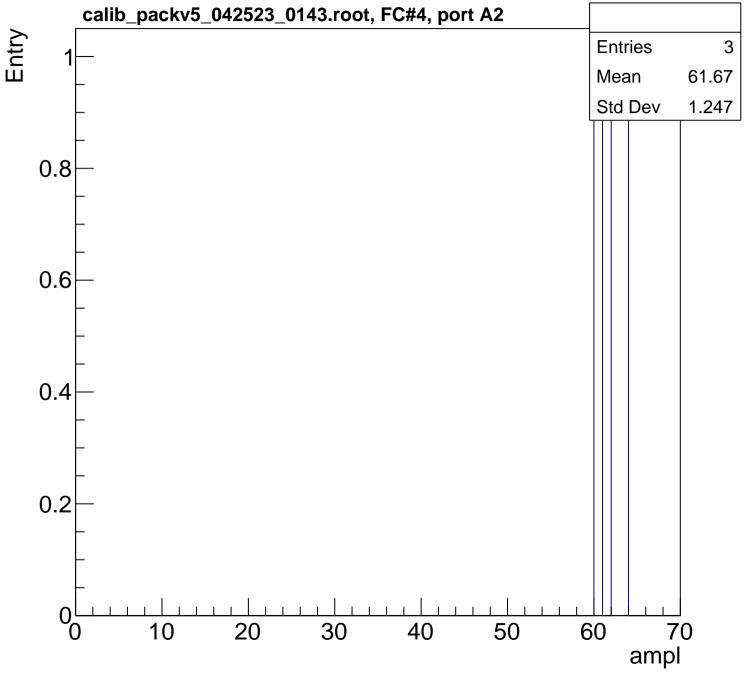




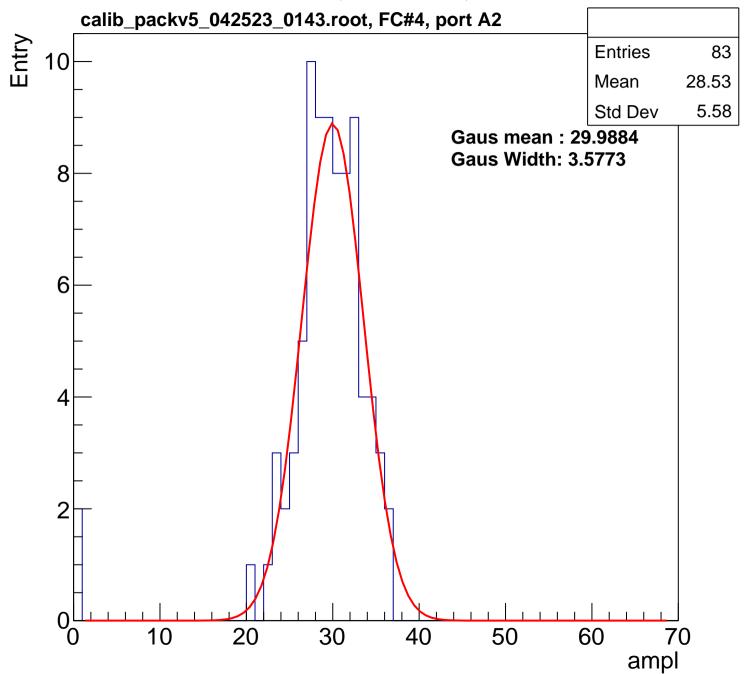


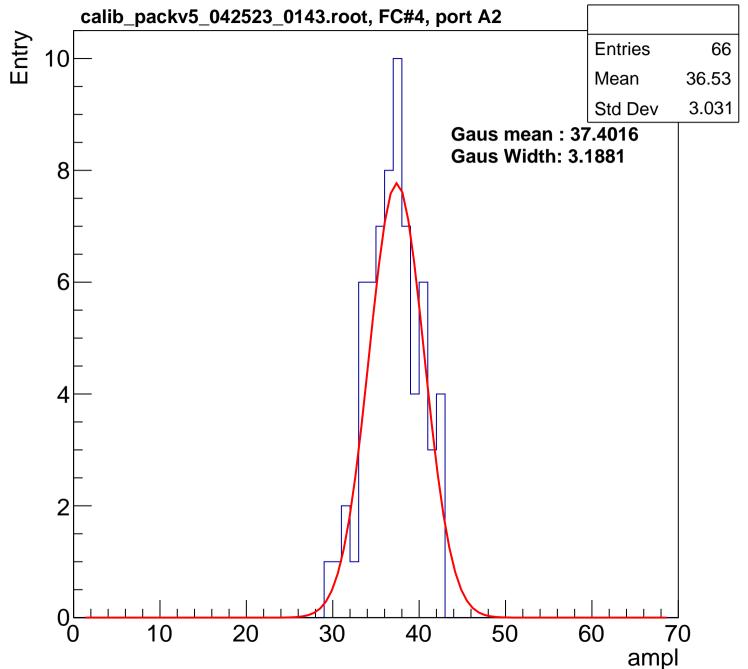


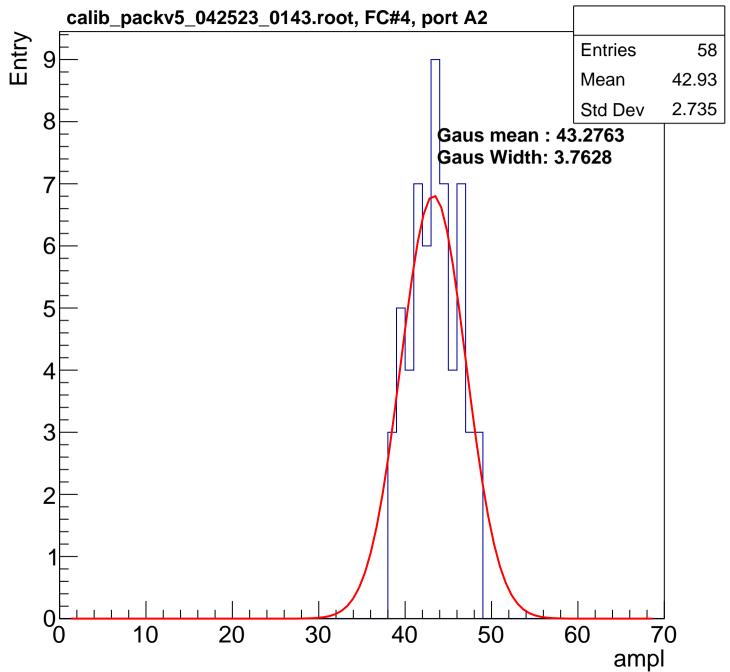


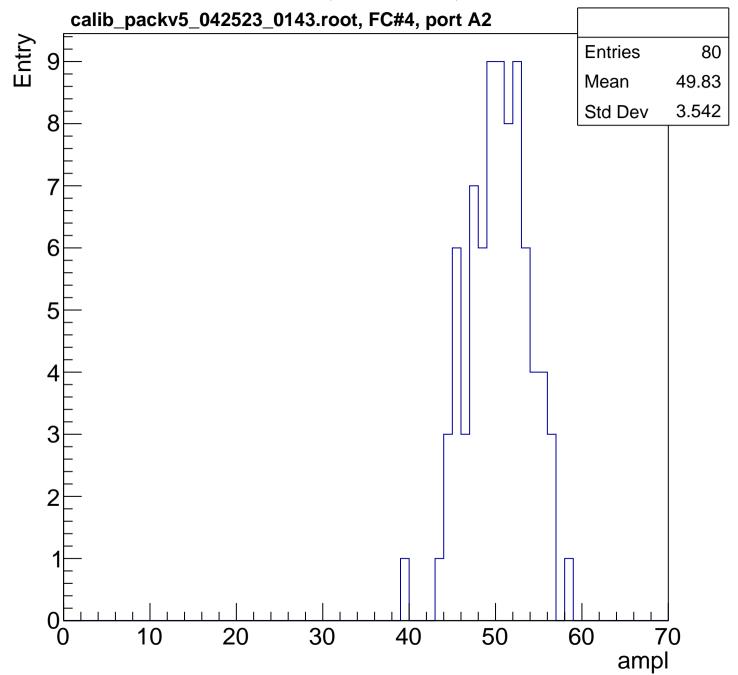


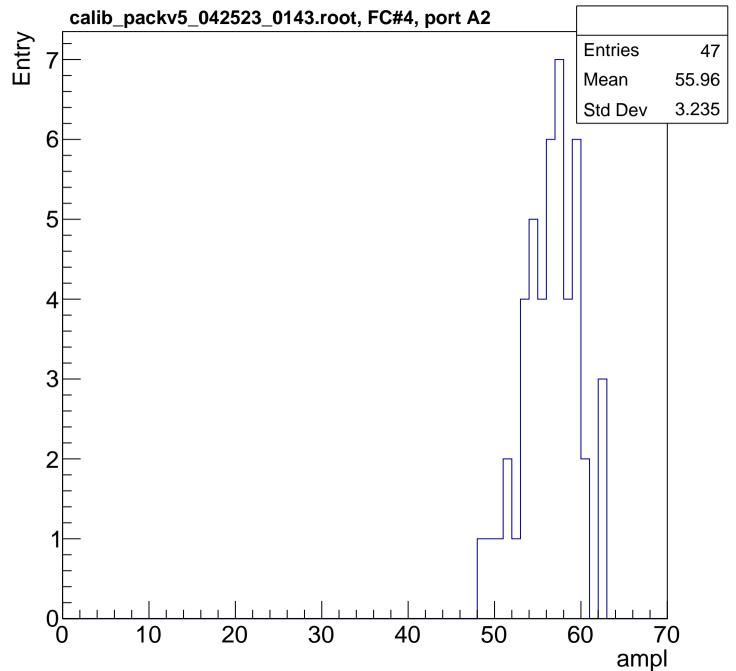
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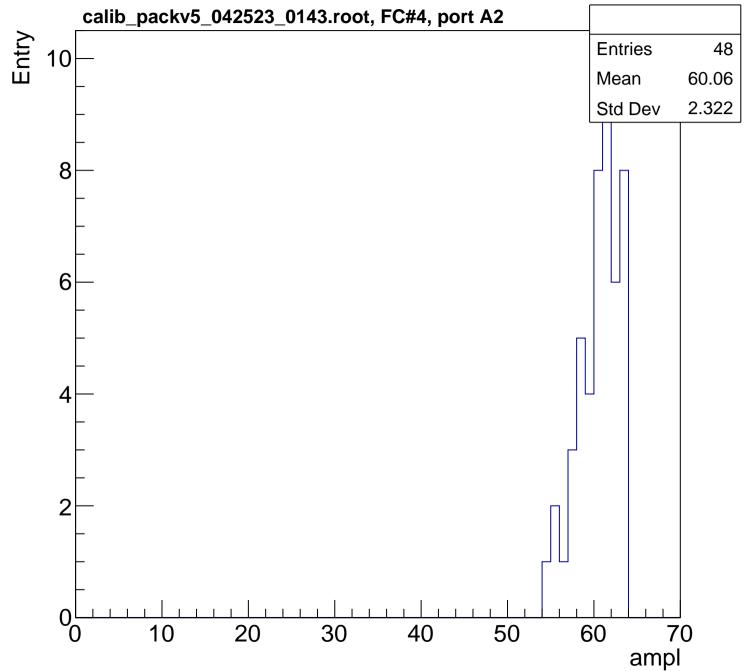


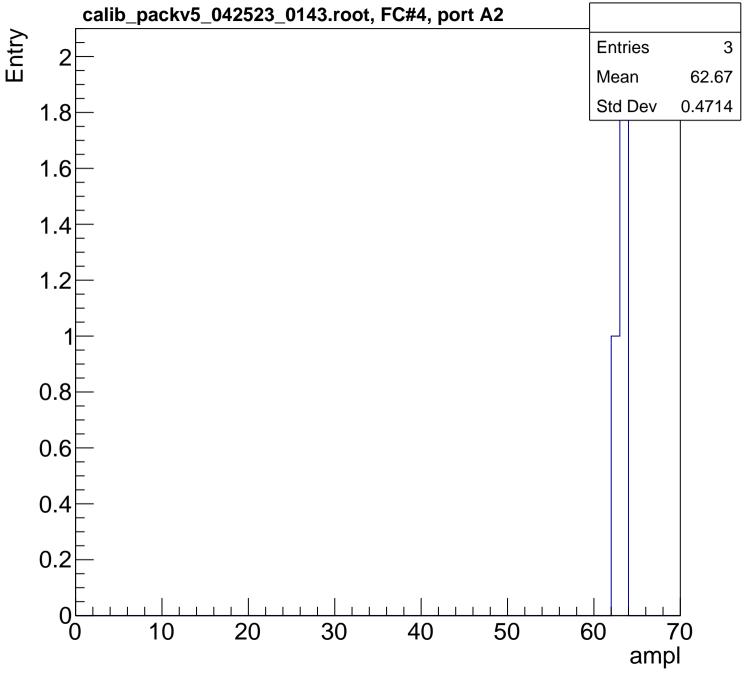




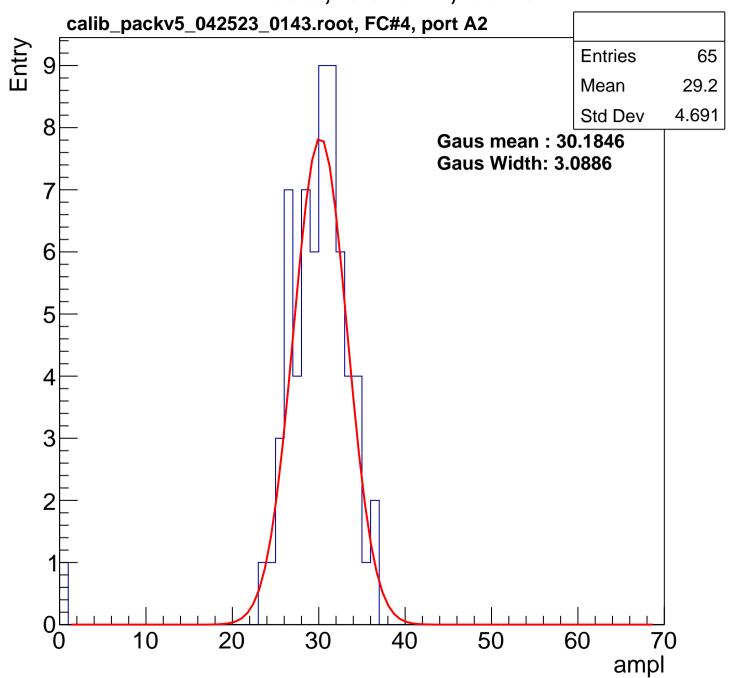


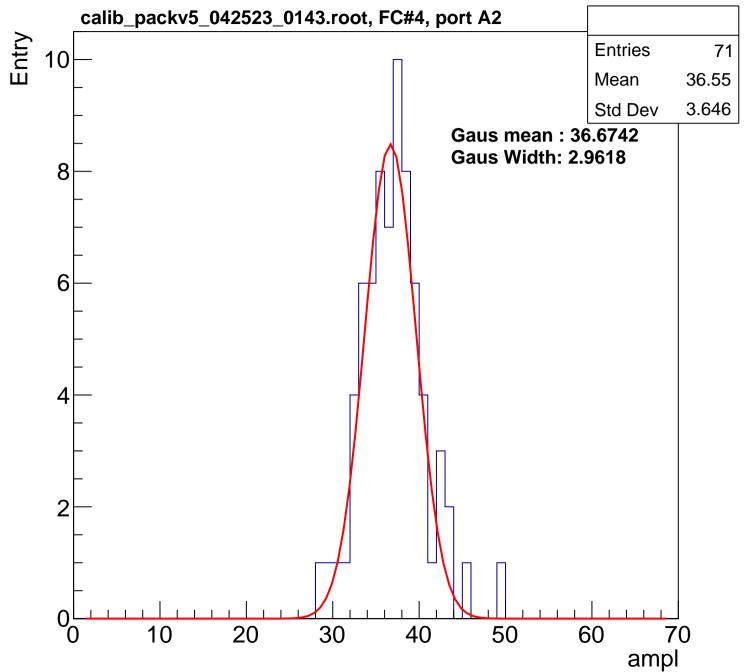


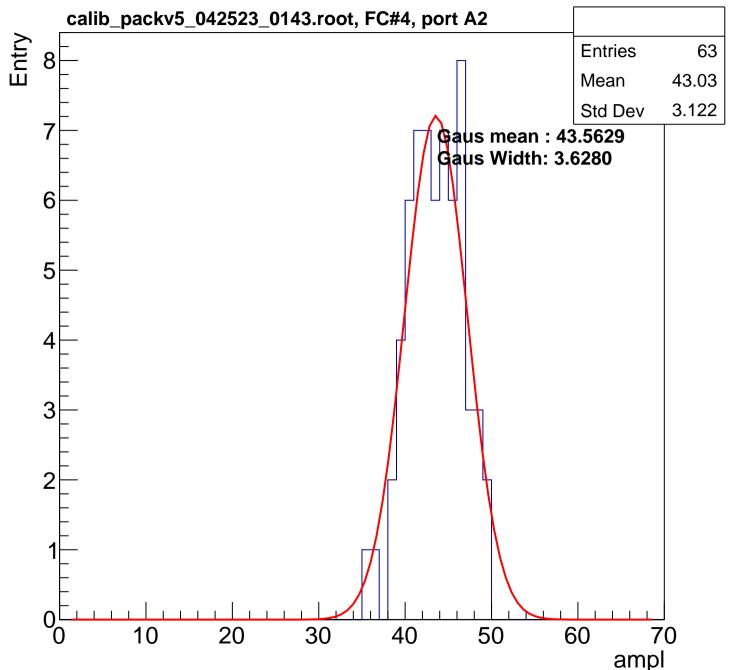


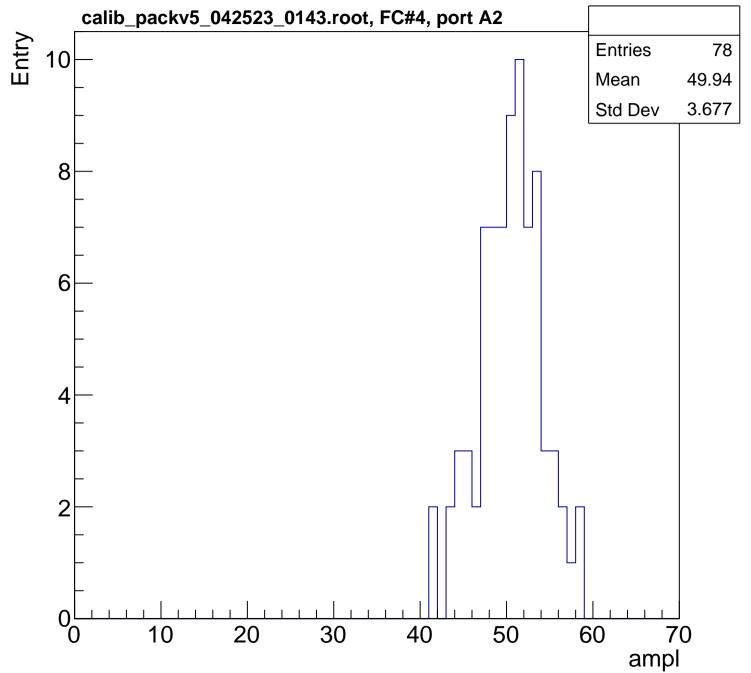


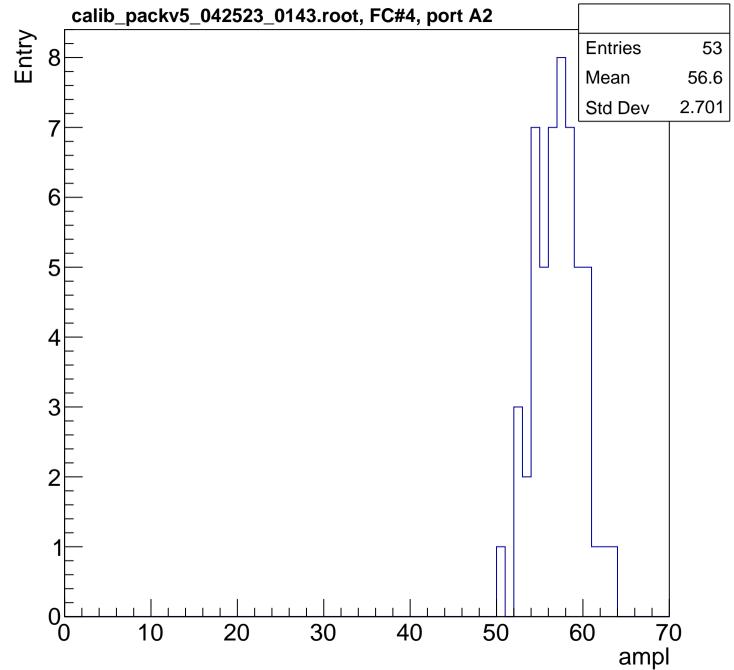
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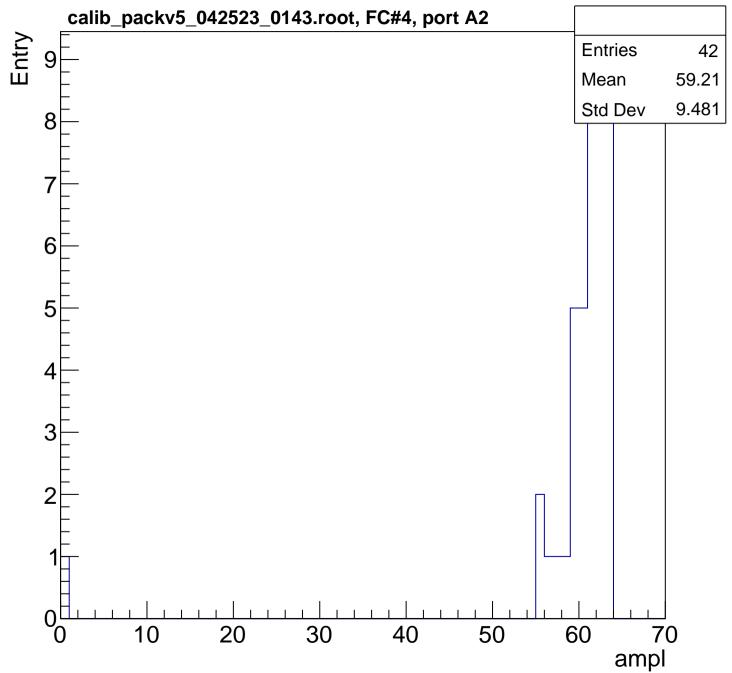


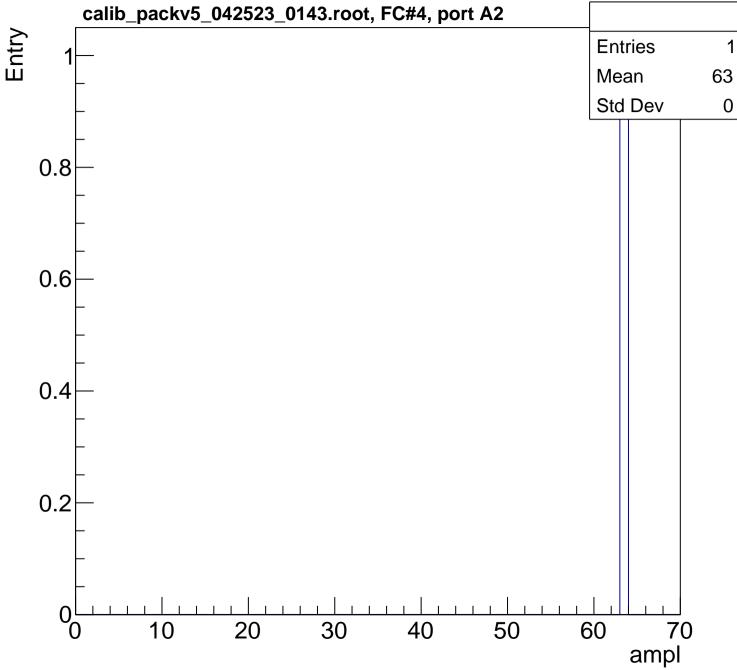




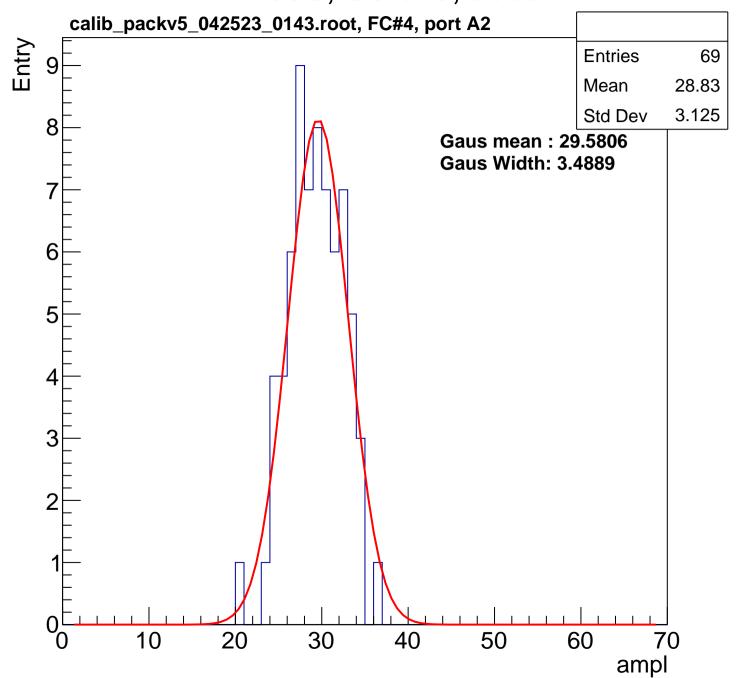


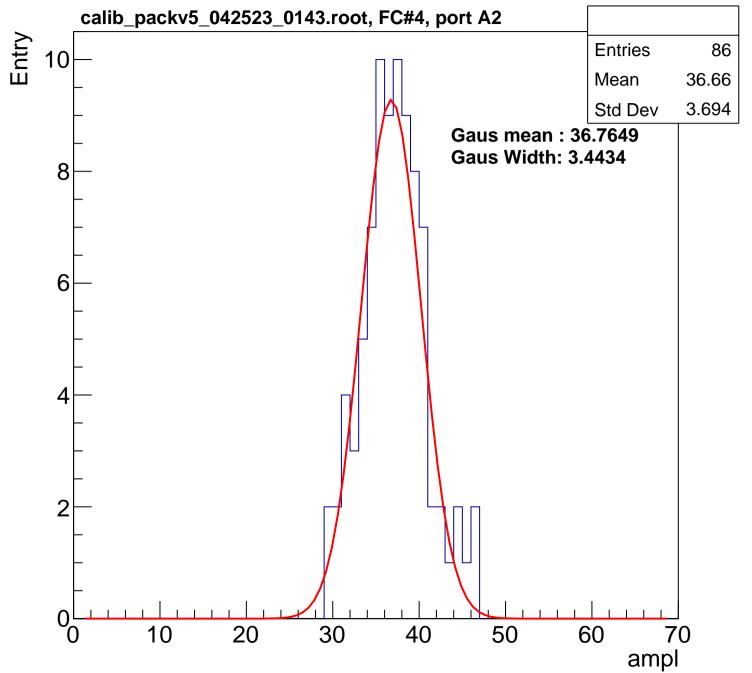


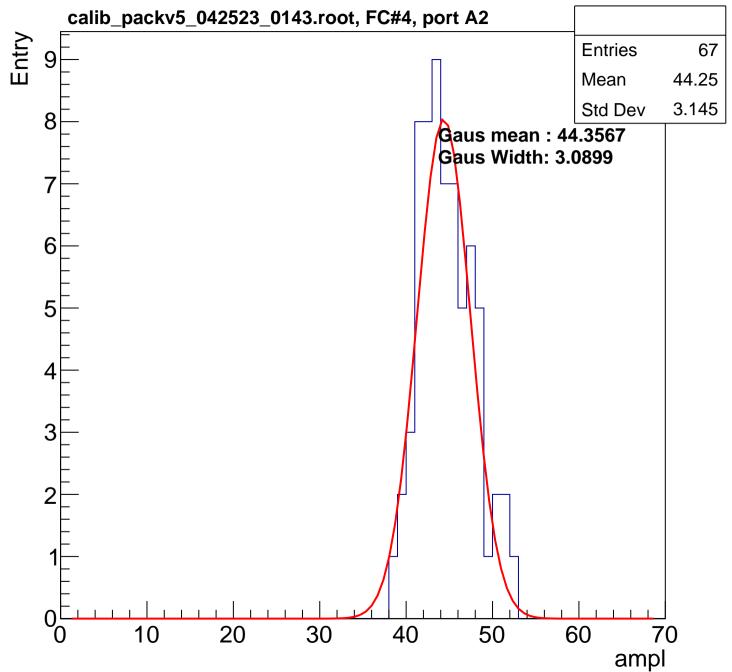


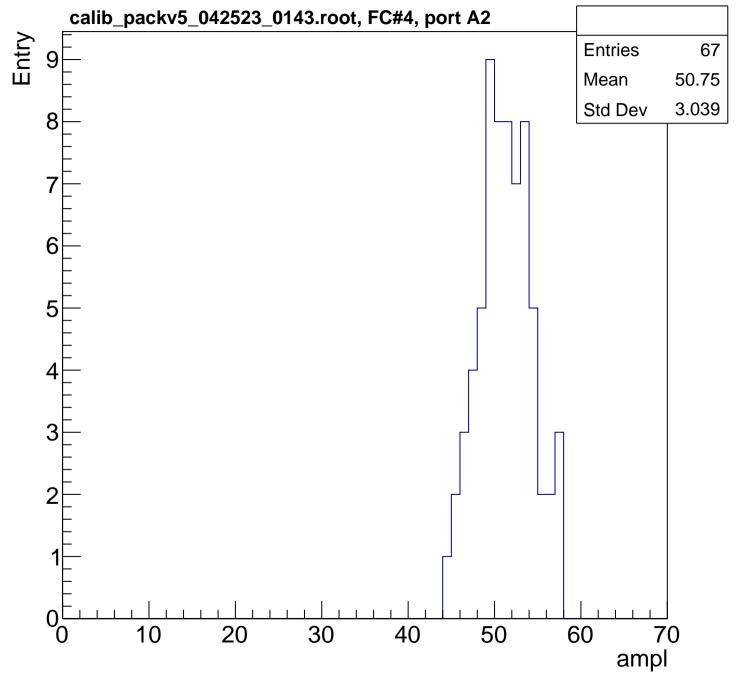


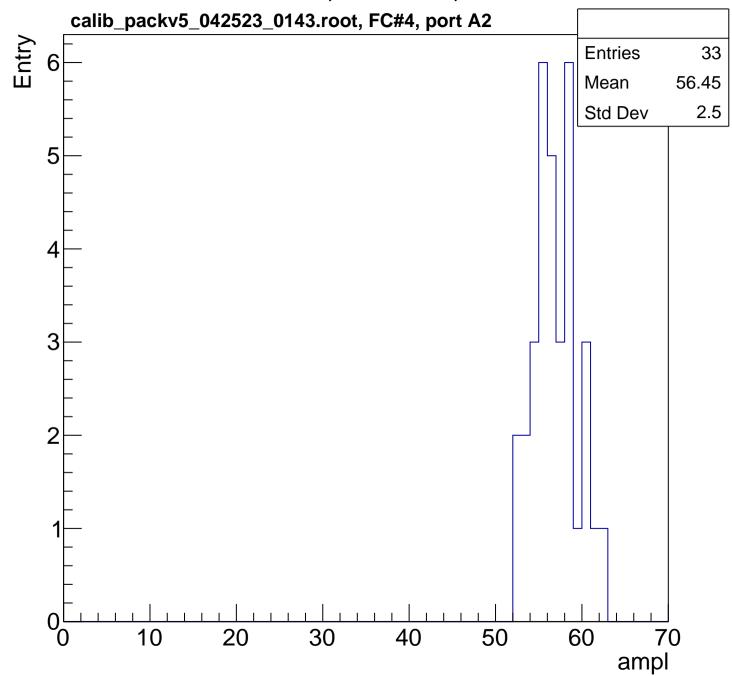
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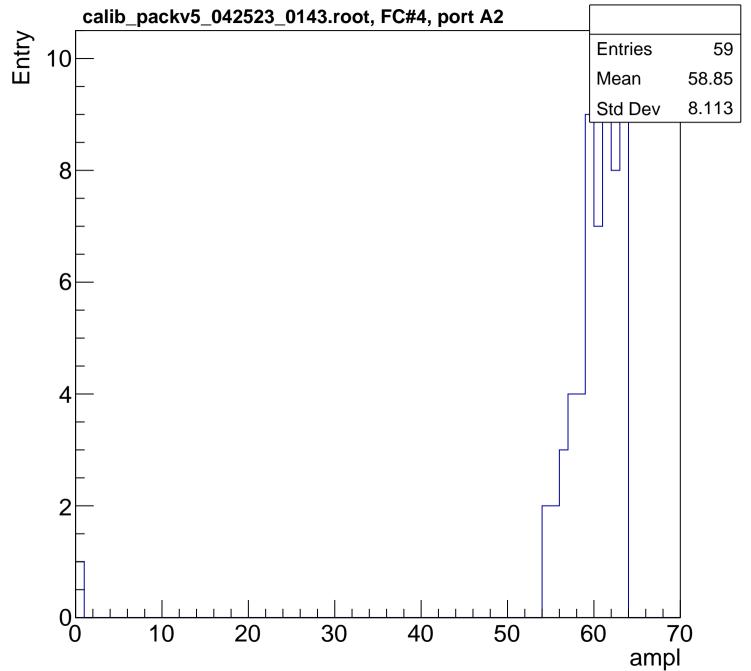




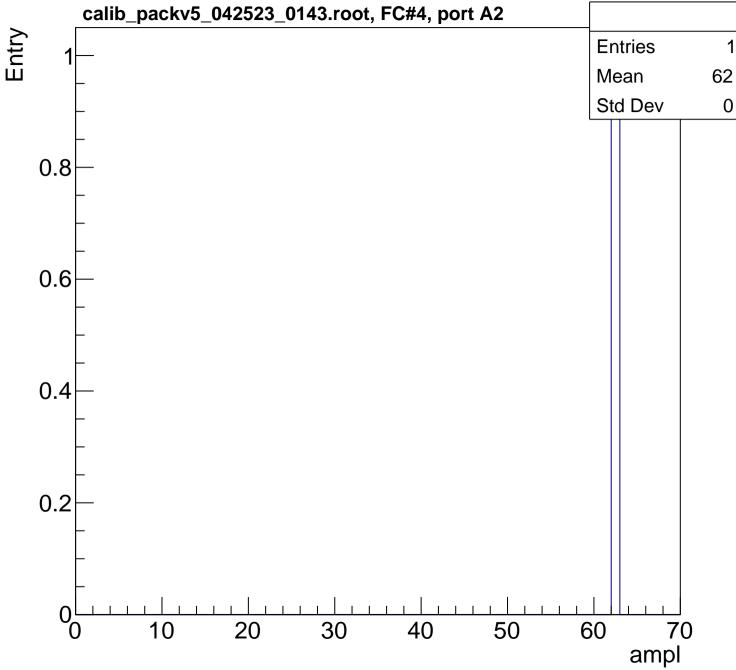


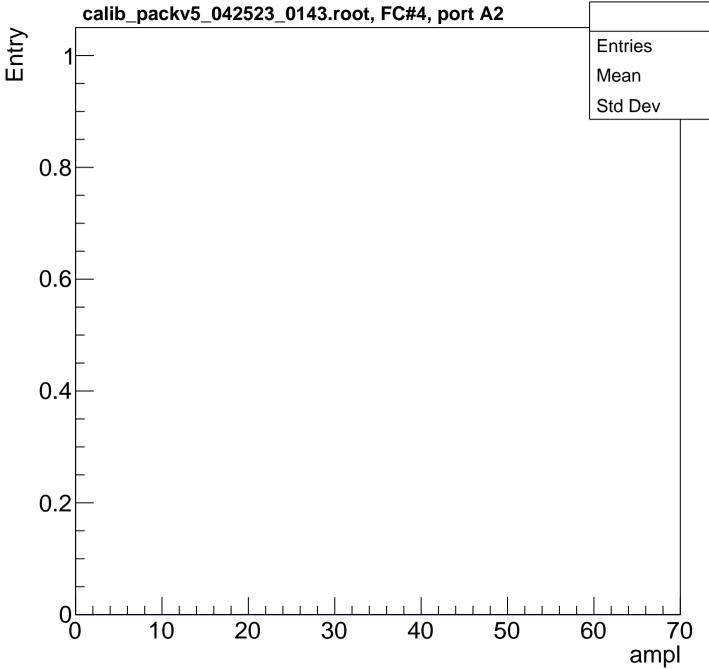


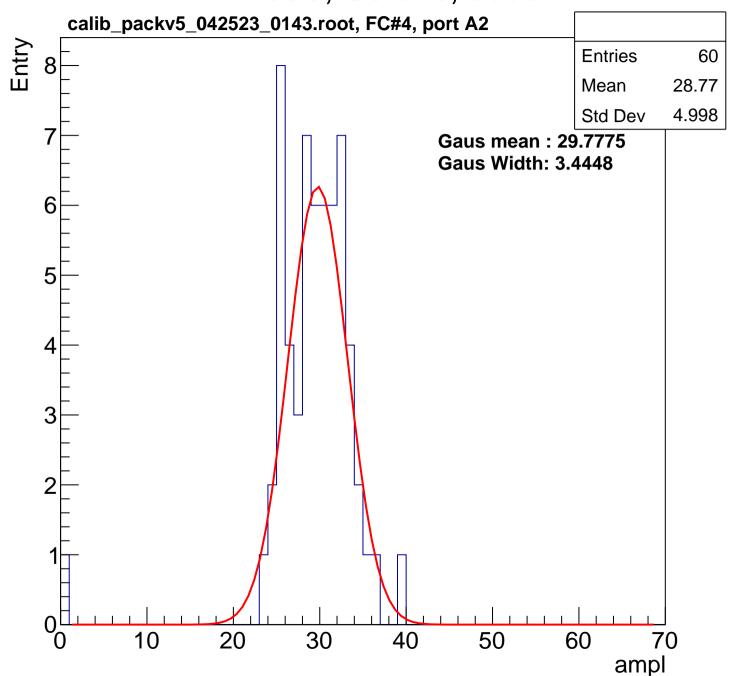


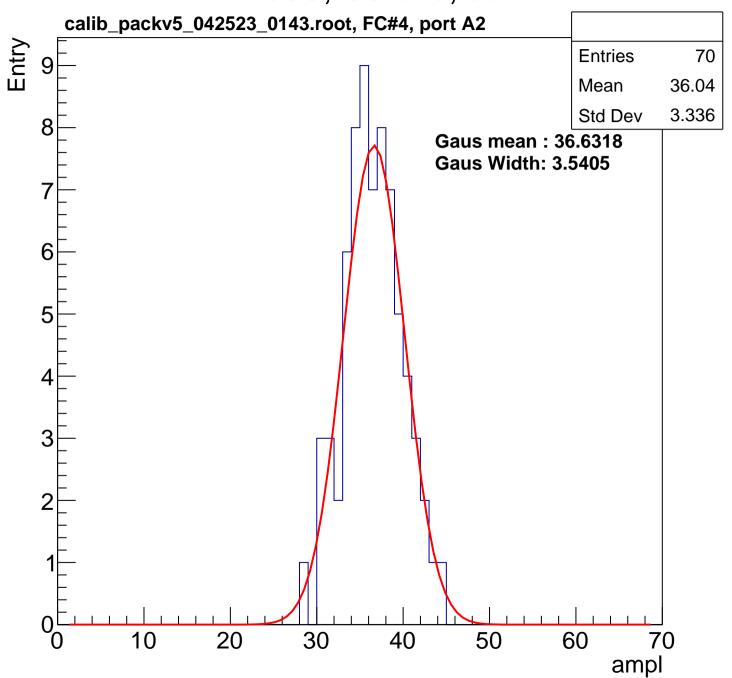


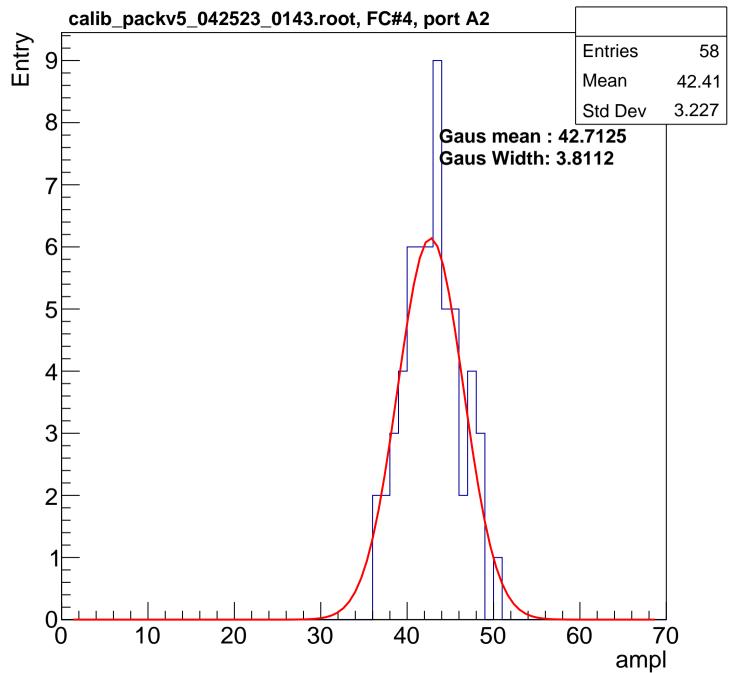
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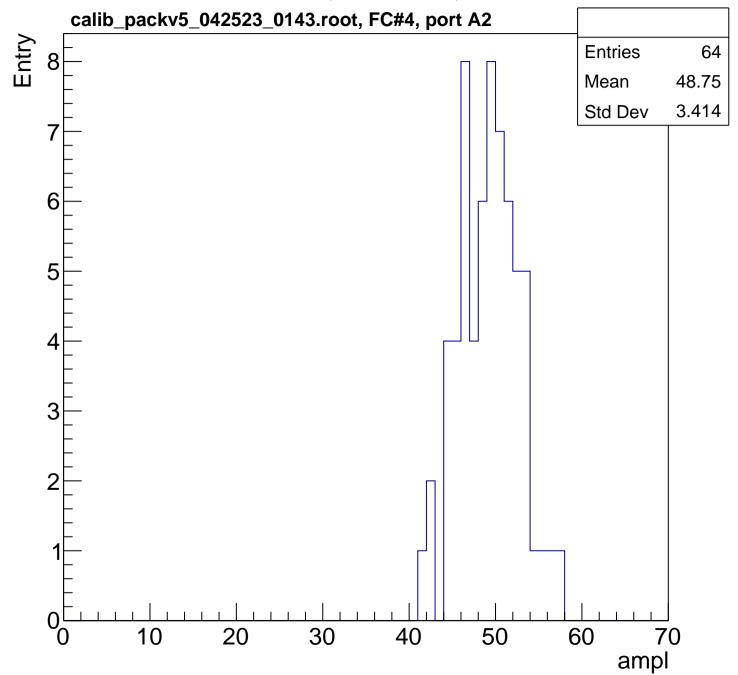


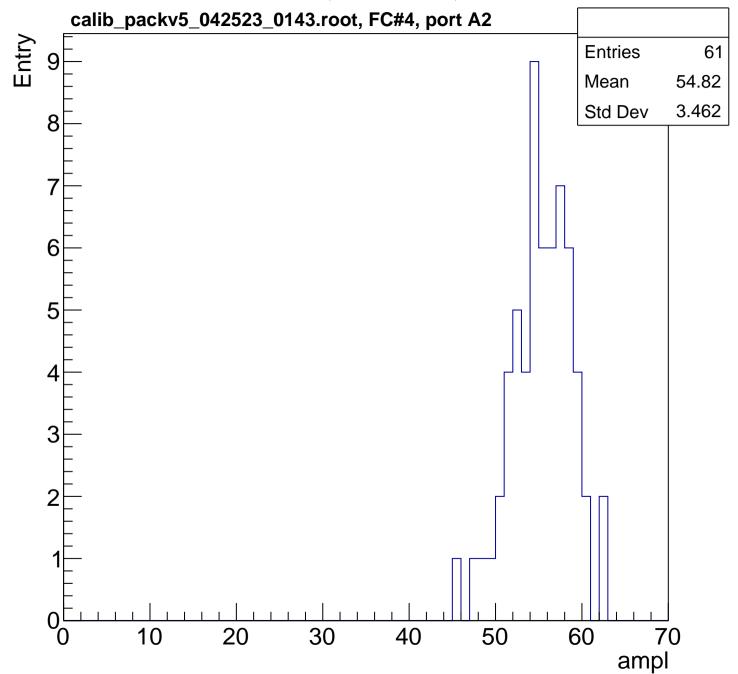


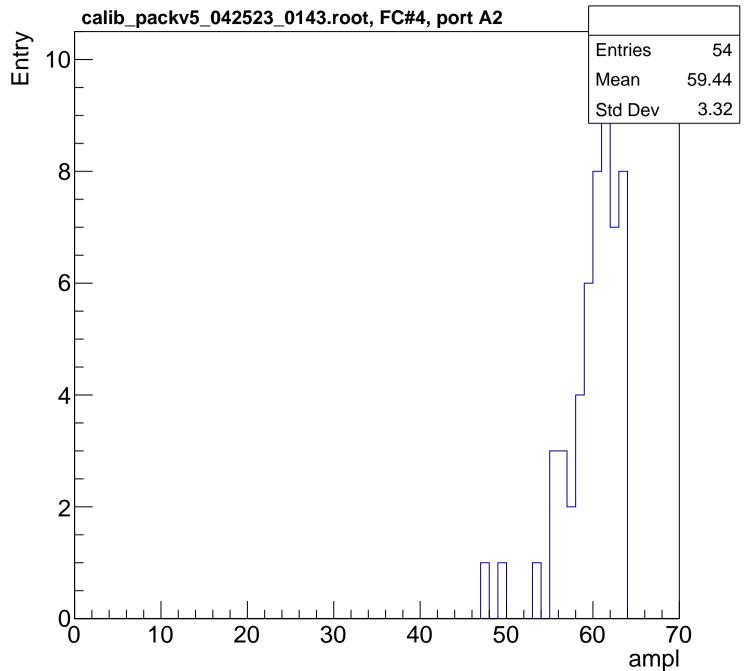


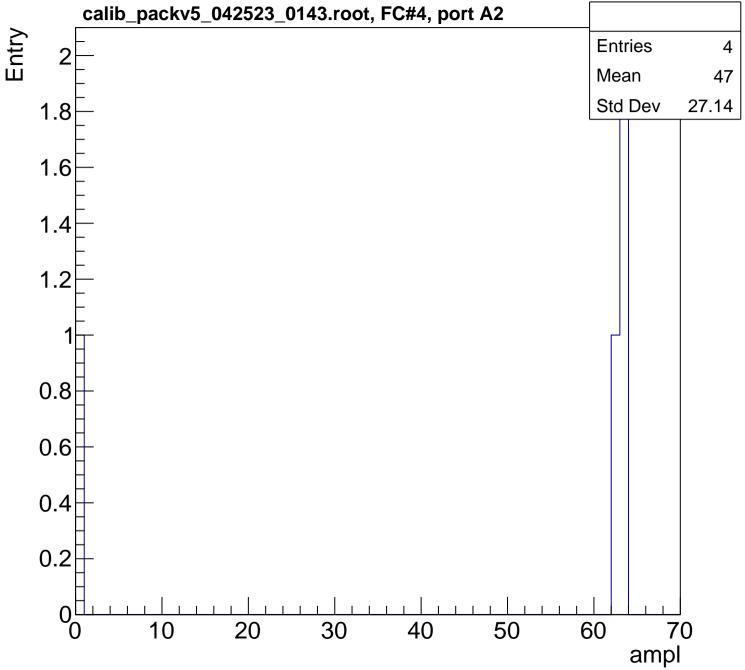




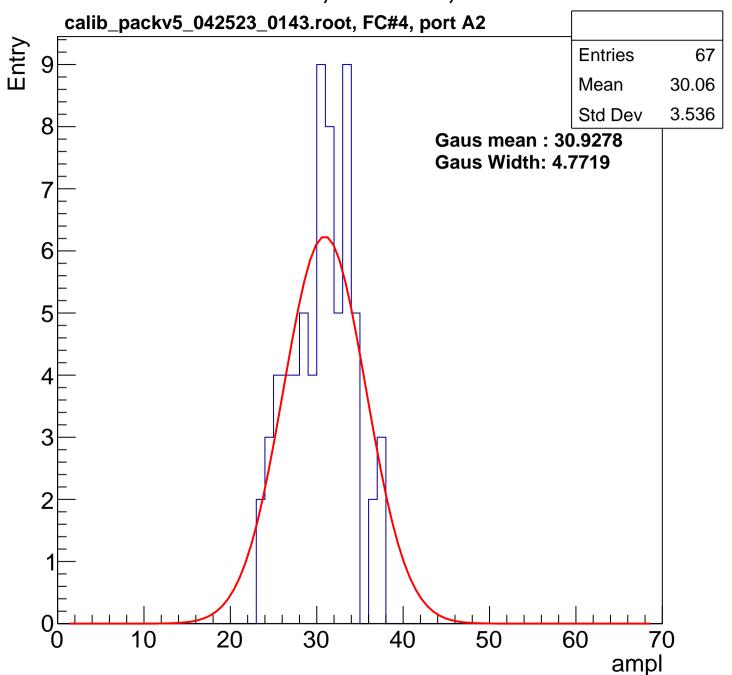


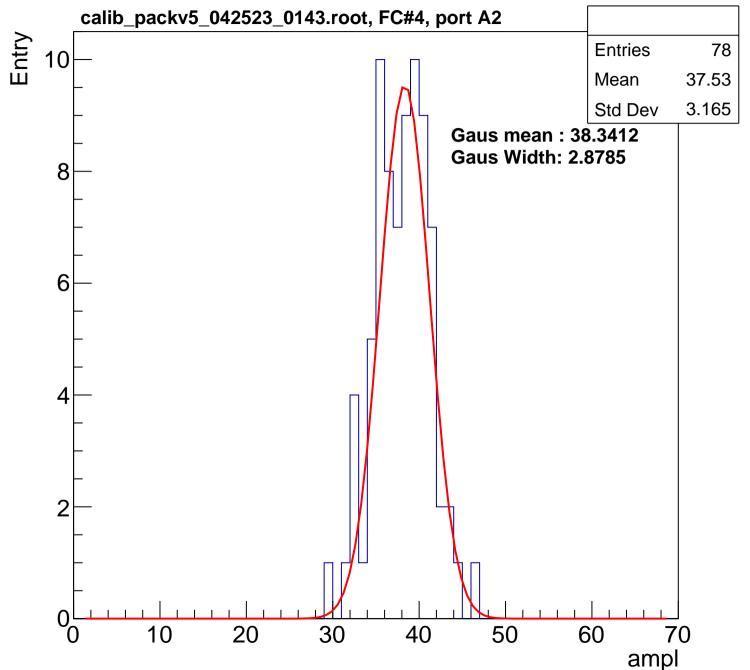


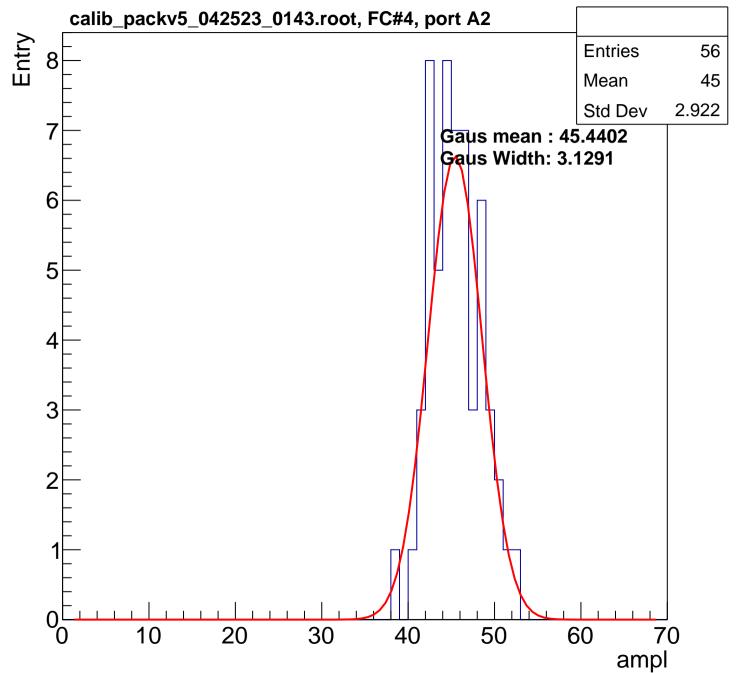


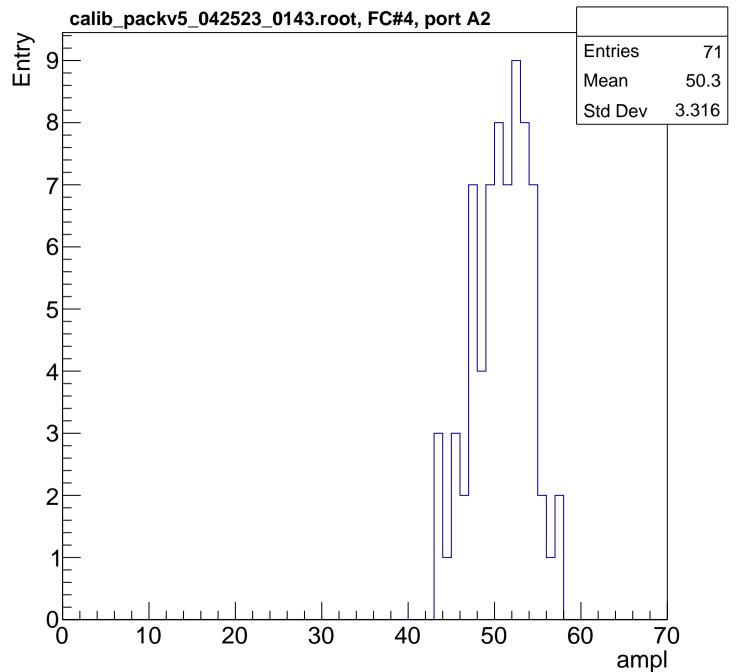


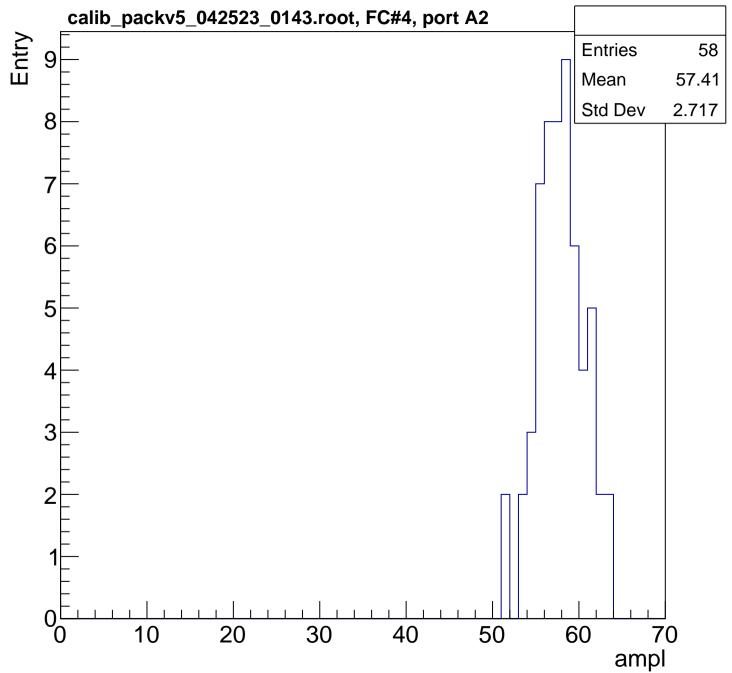
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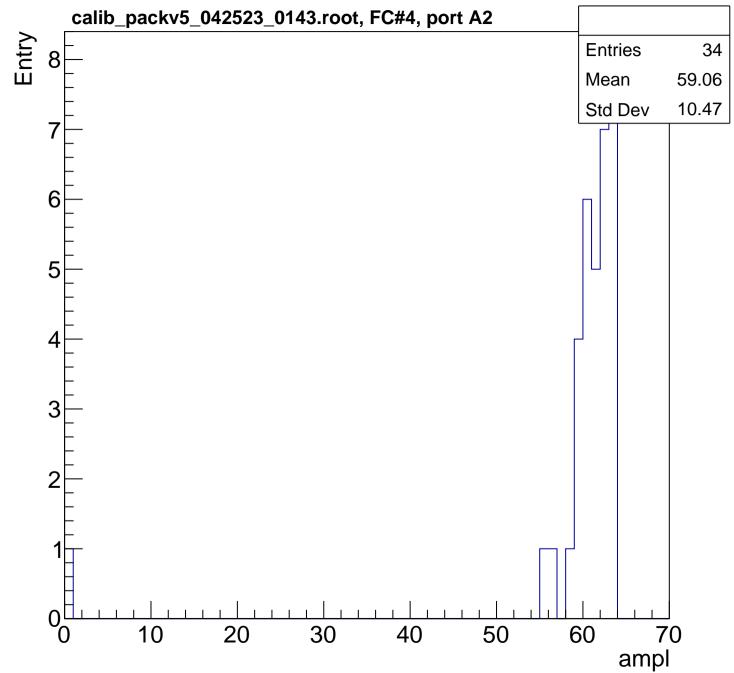




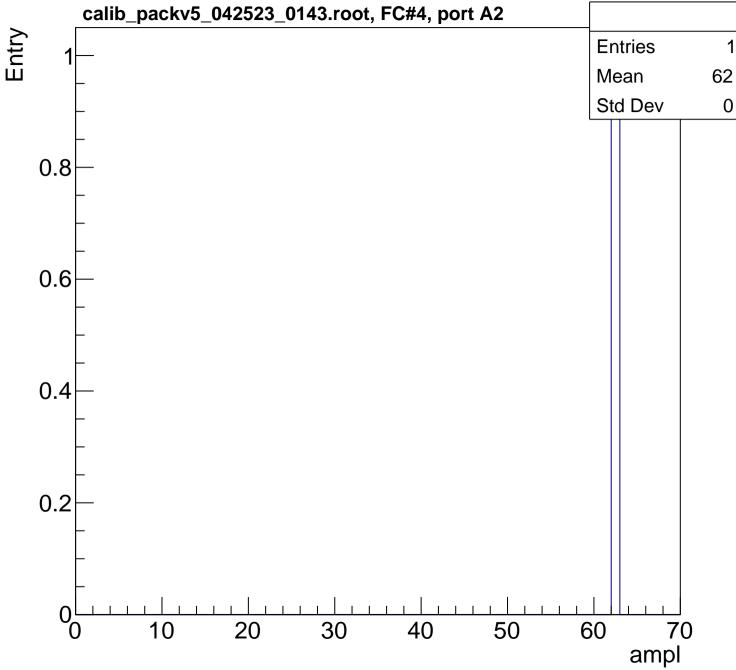




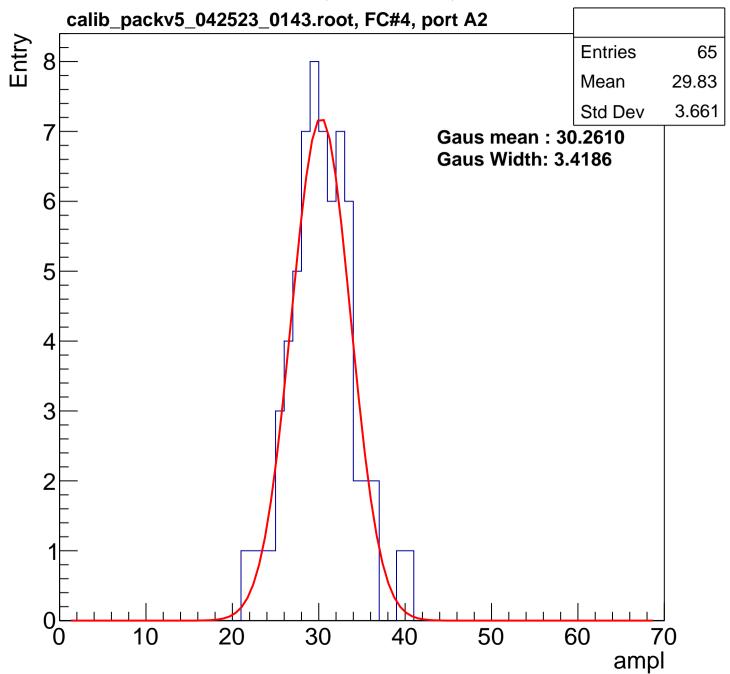


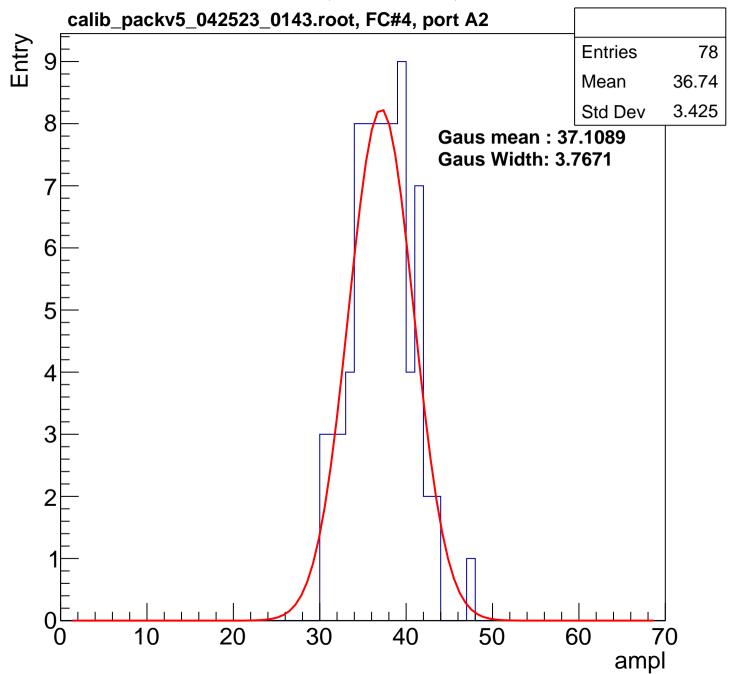


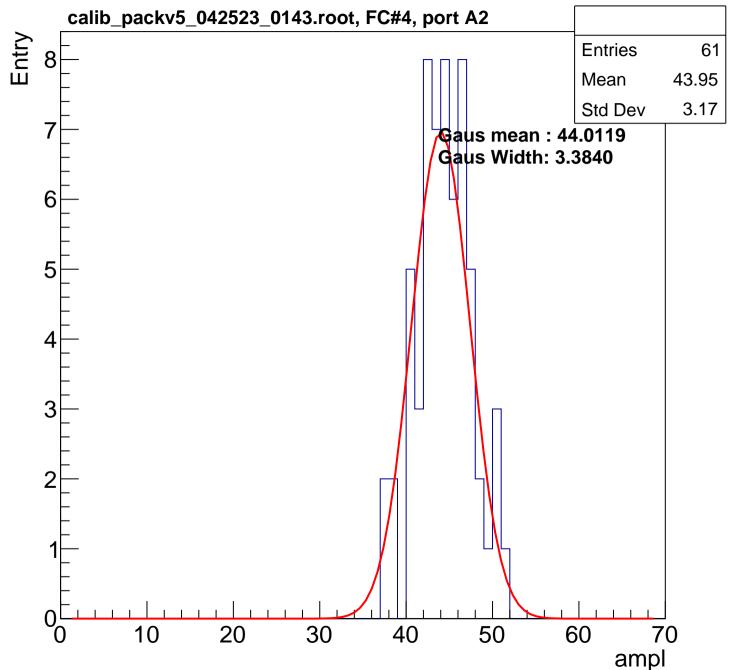
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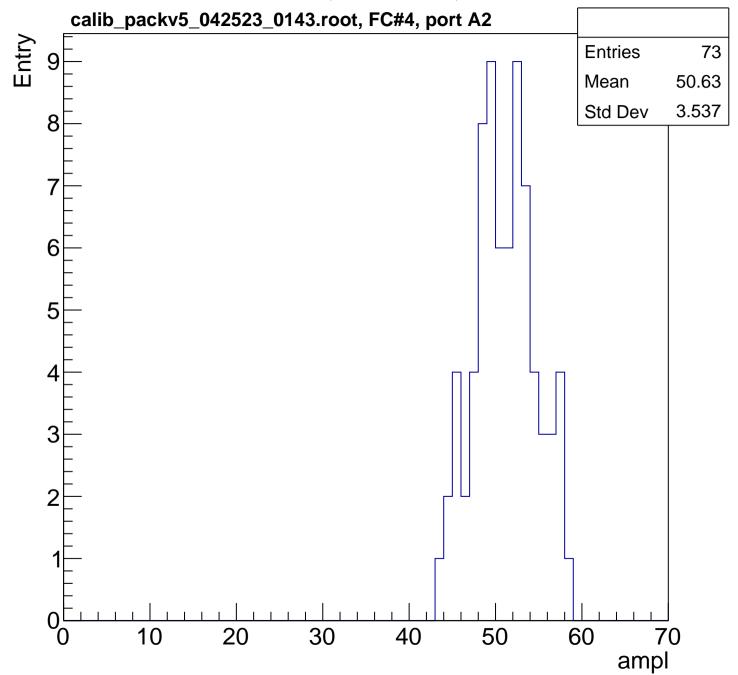


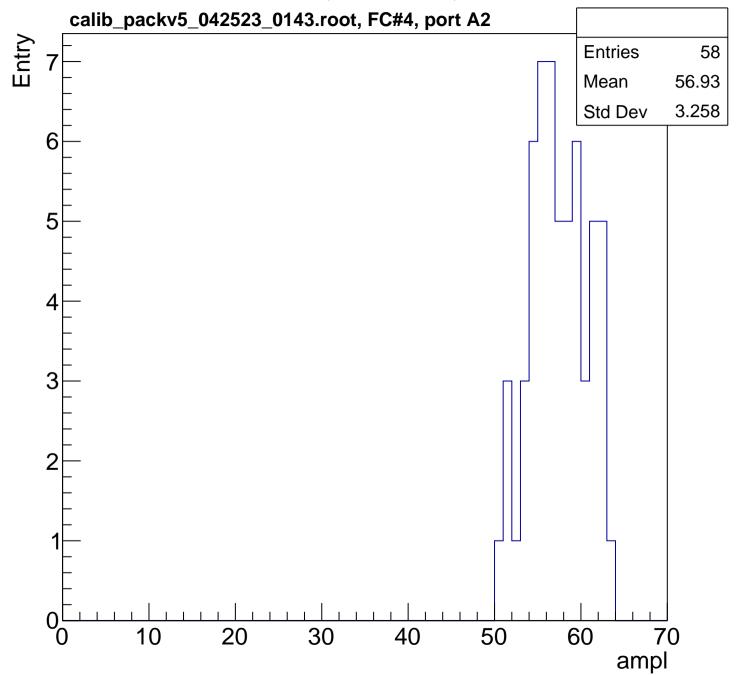
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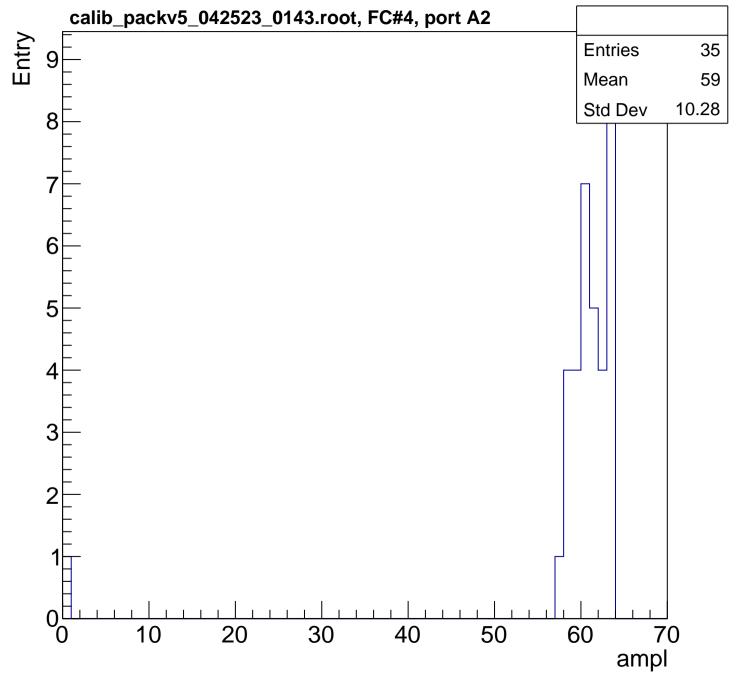


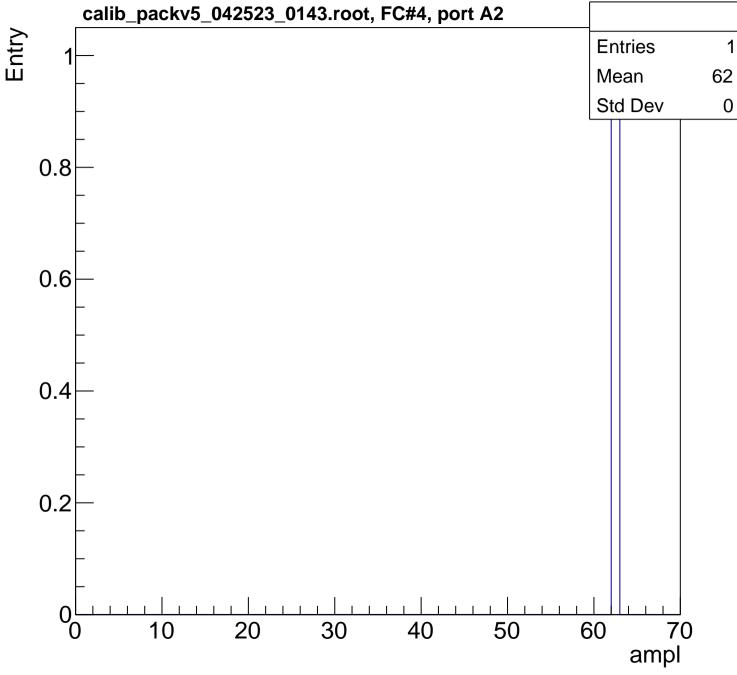


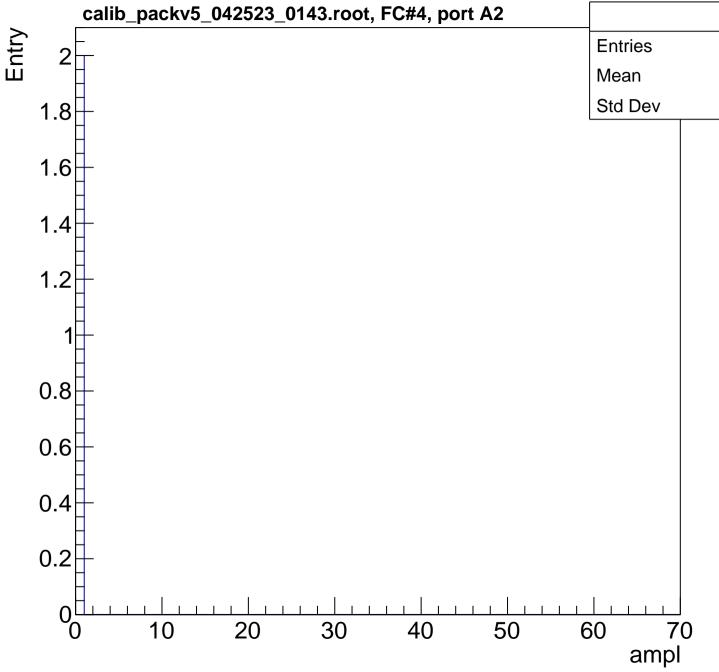


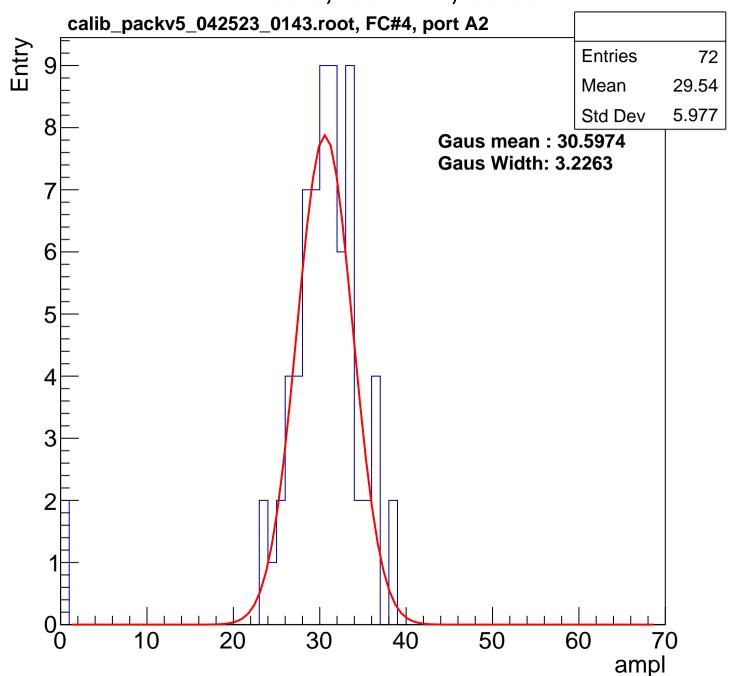


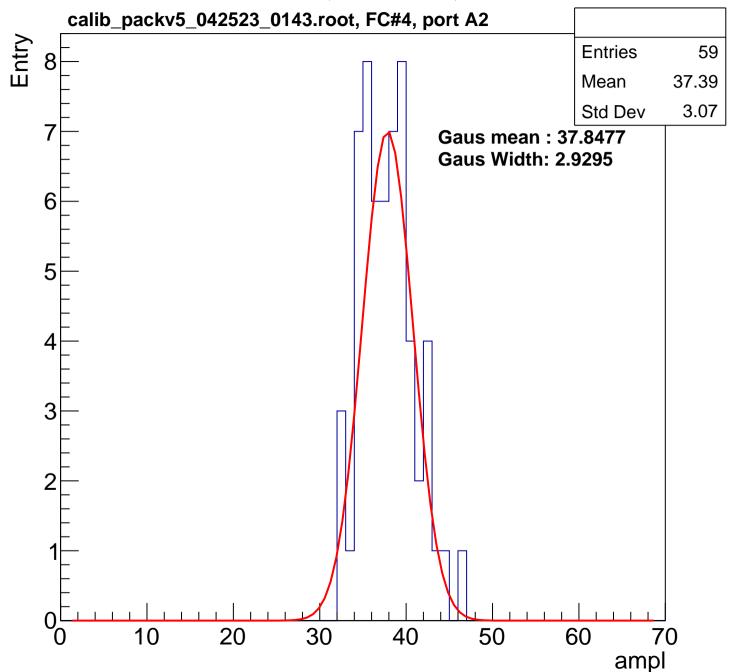


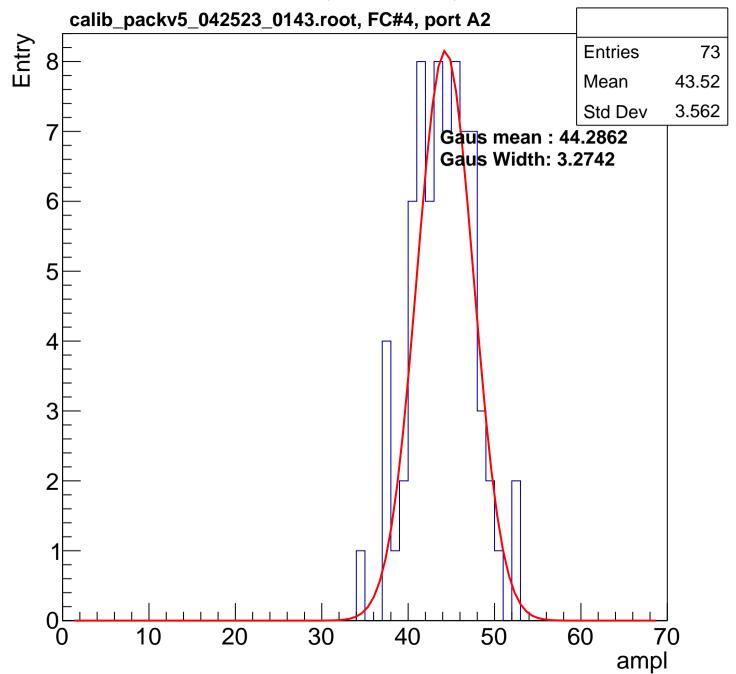


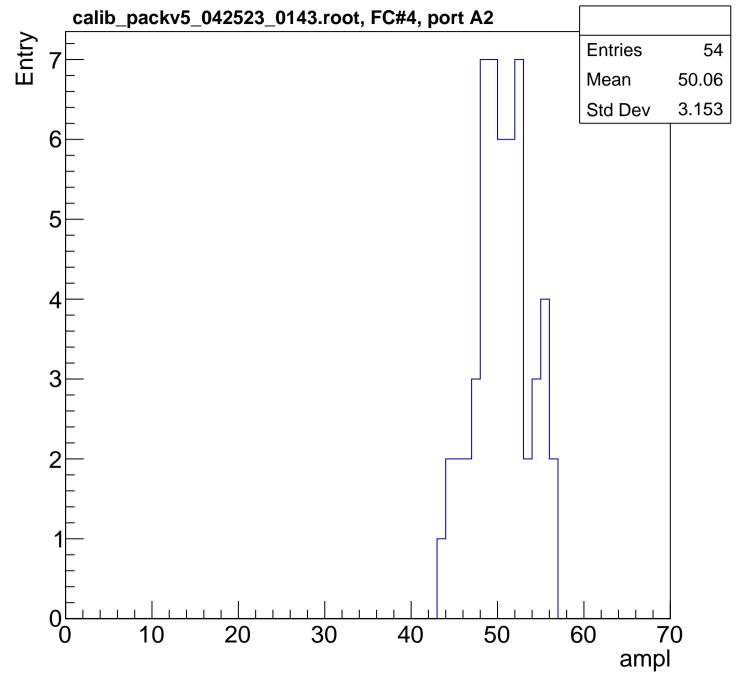


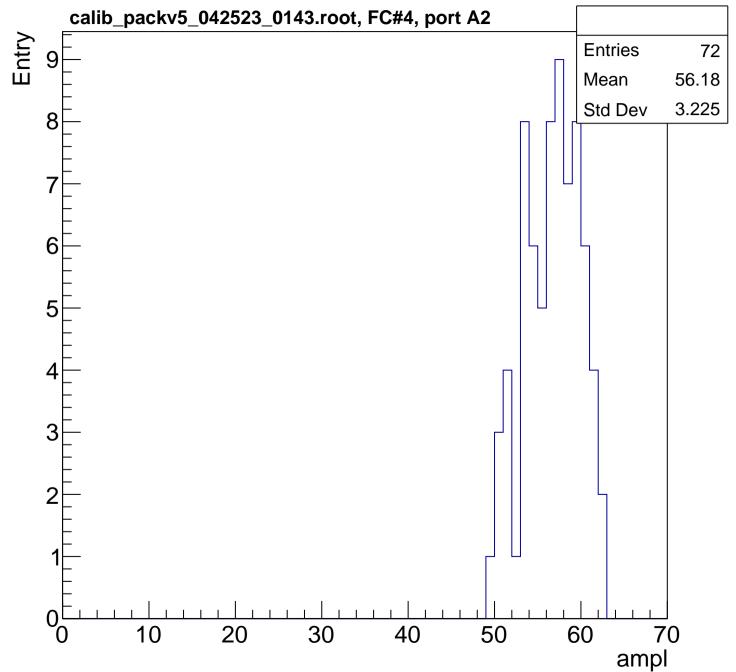


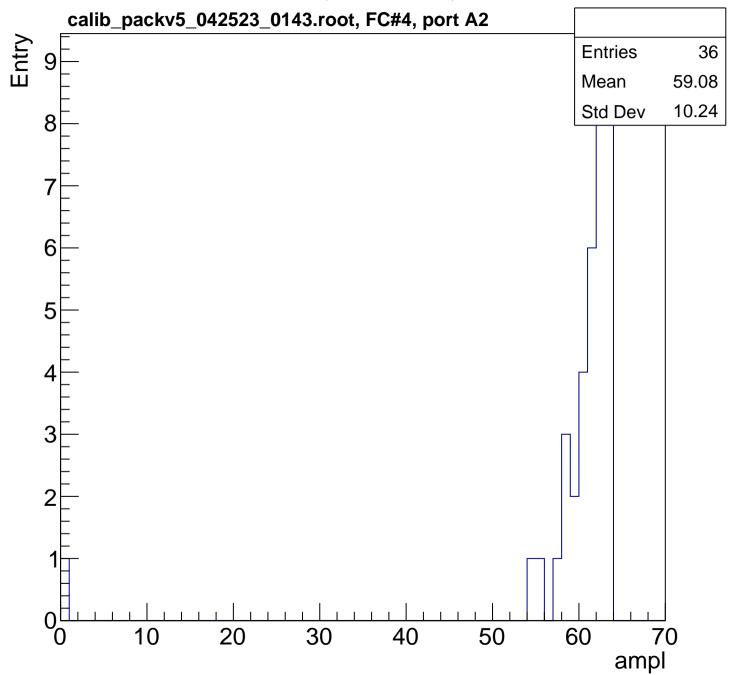


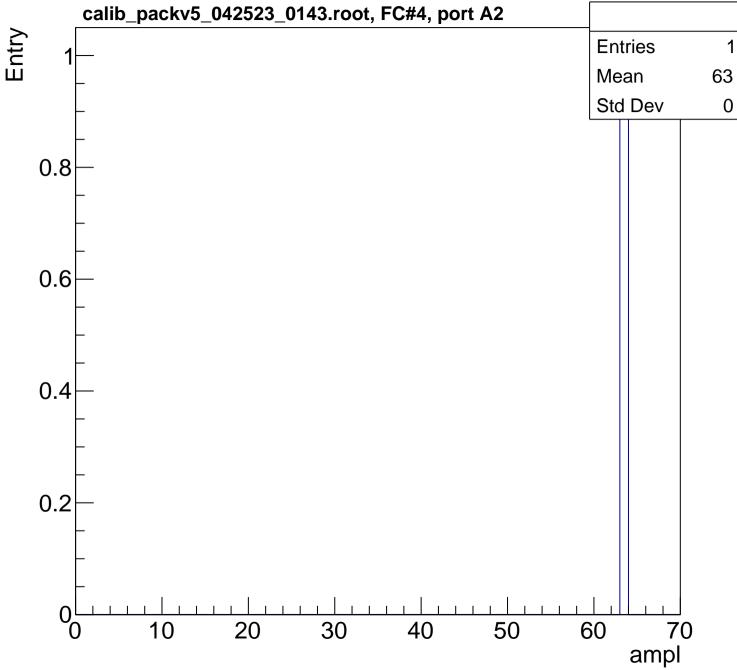


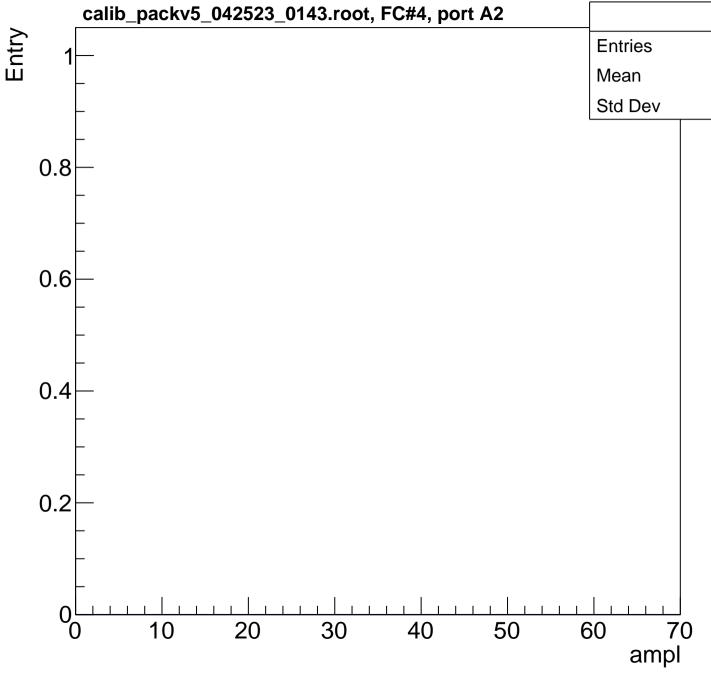


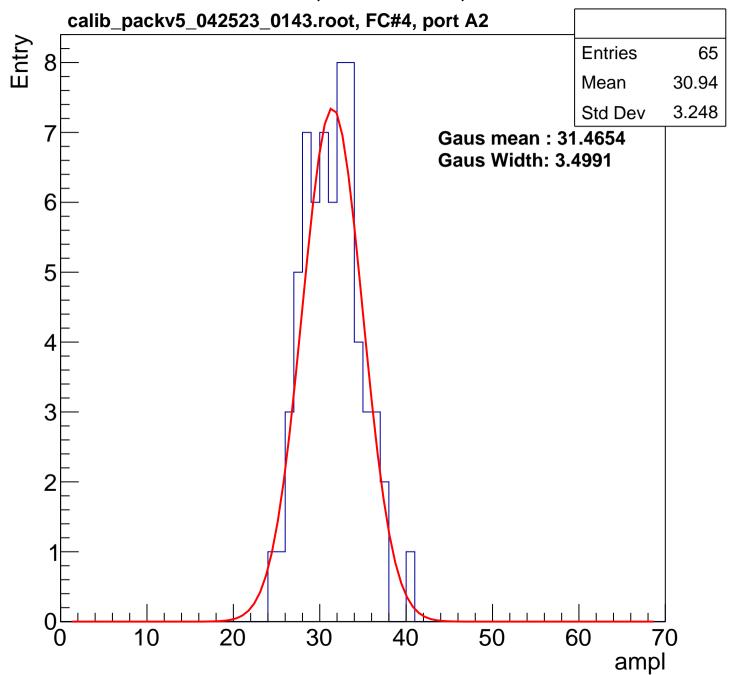


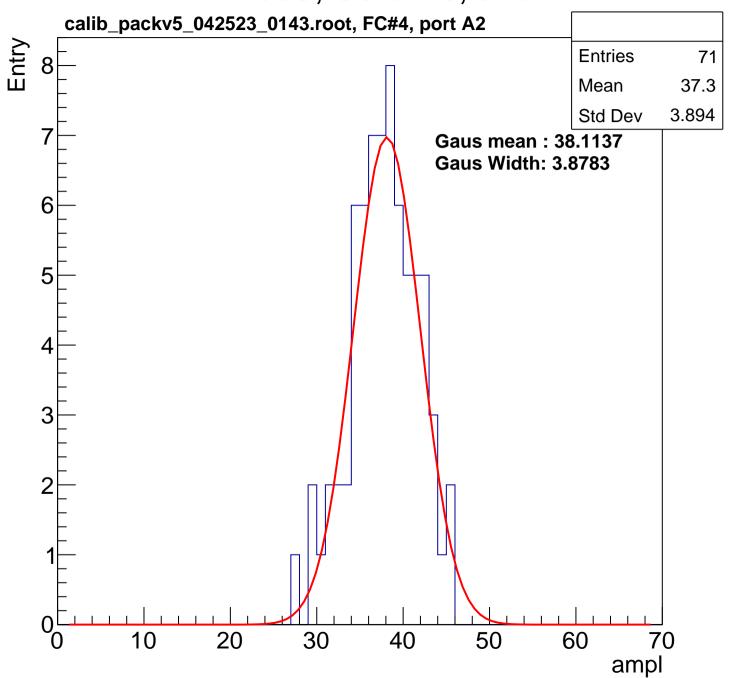


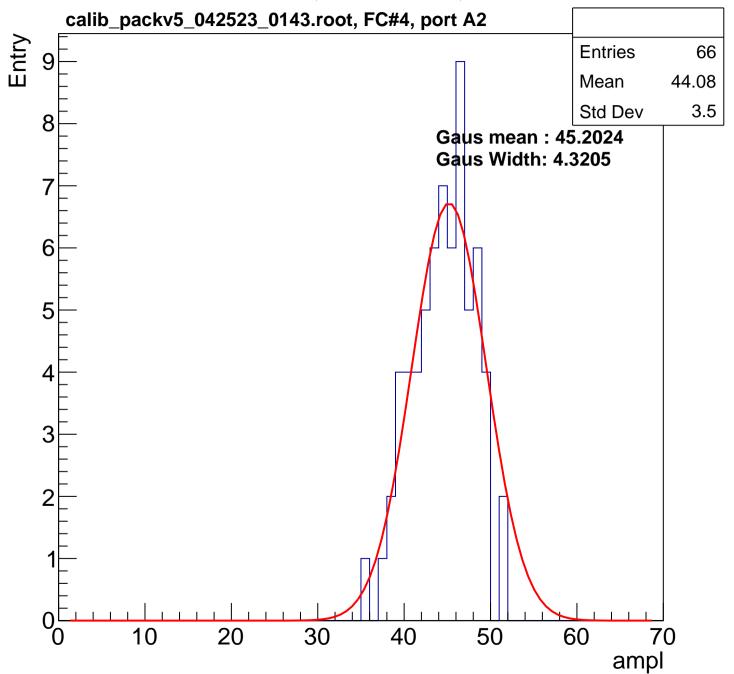


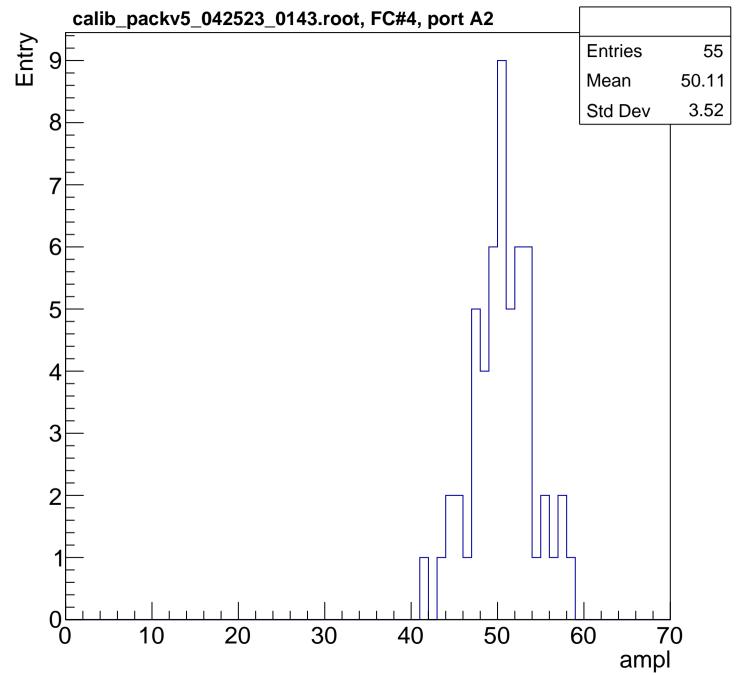


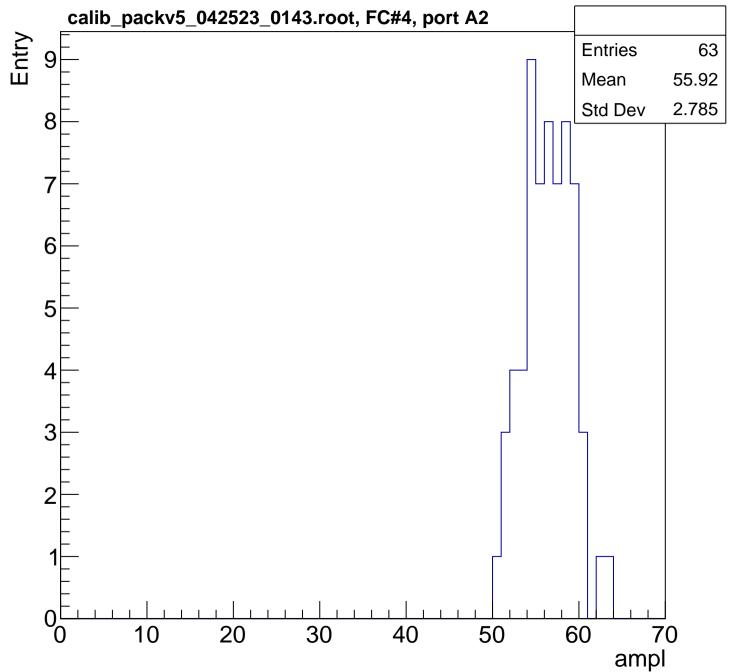


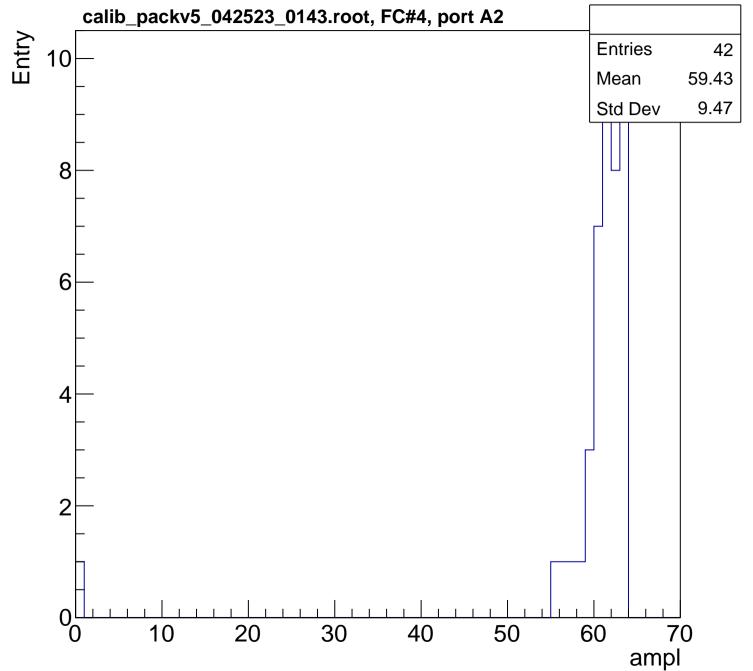


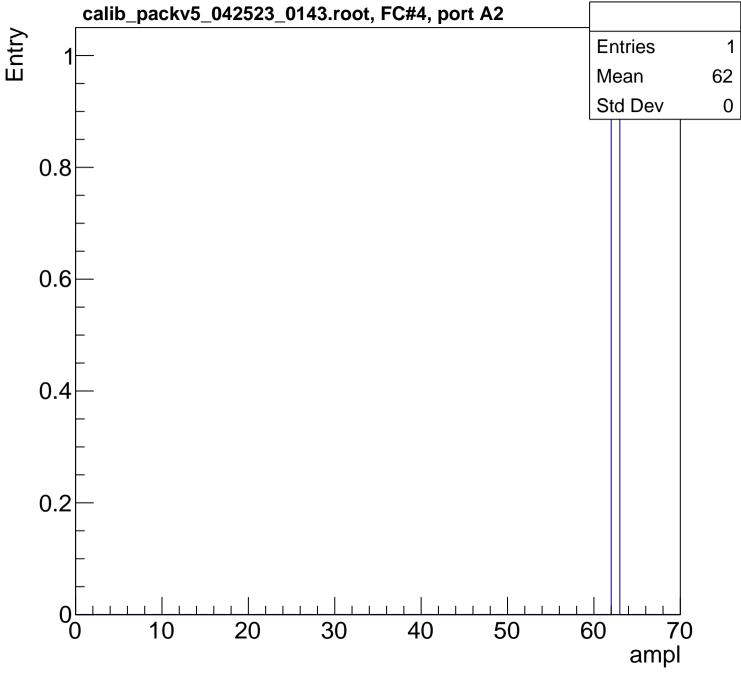






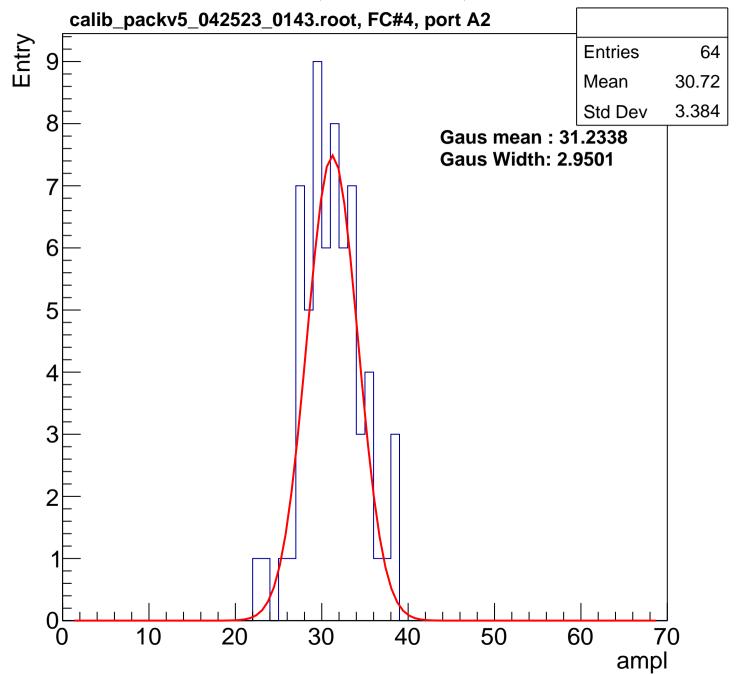


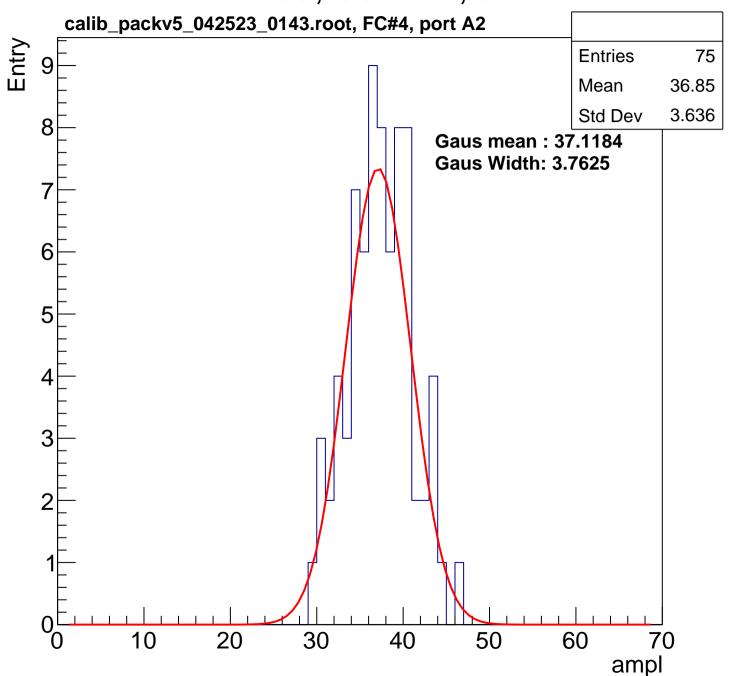


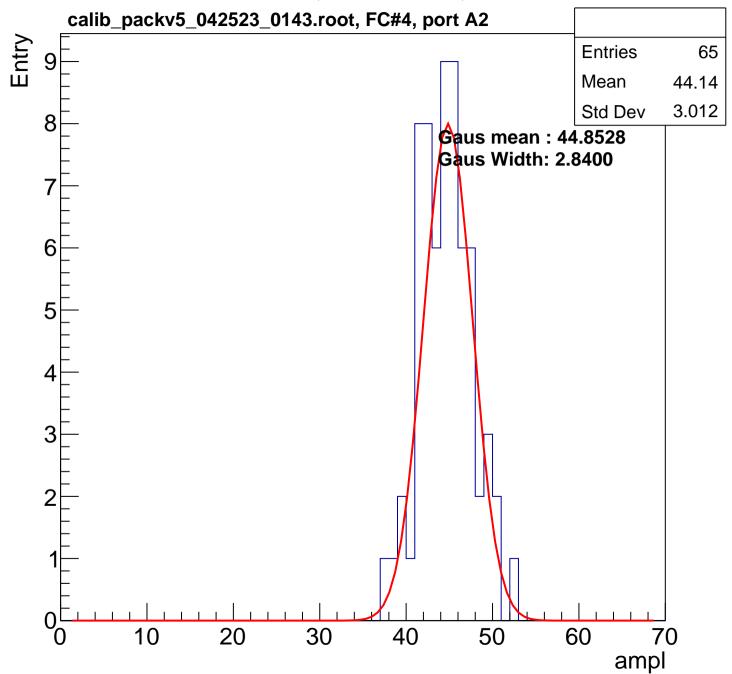


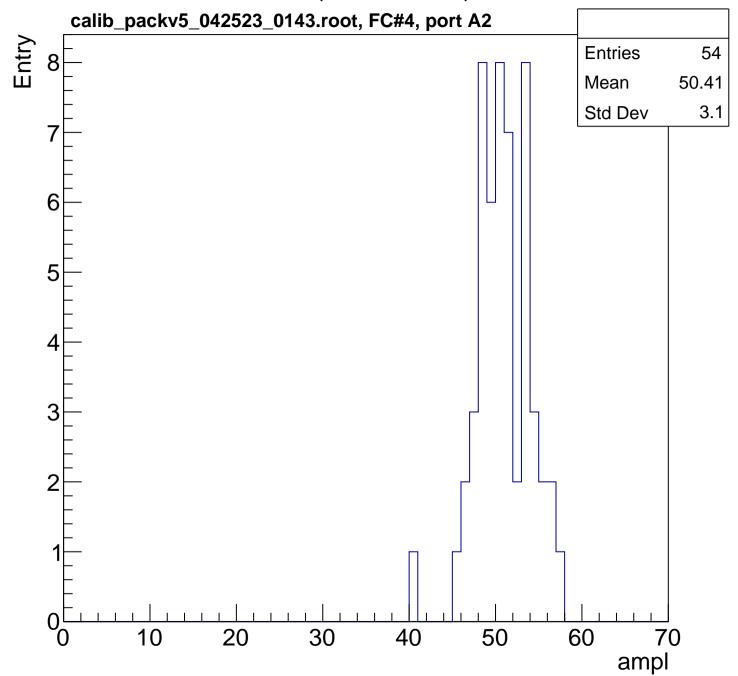
B1L100S, U8-ch10, adc7 calib_packv5_042523_0143.root, FC#4, port A2 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70

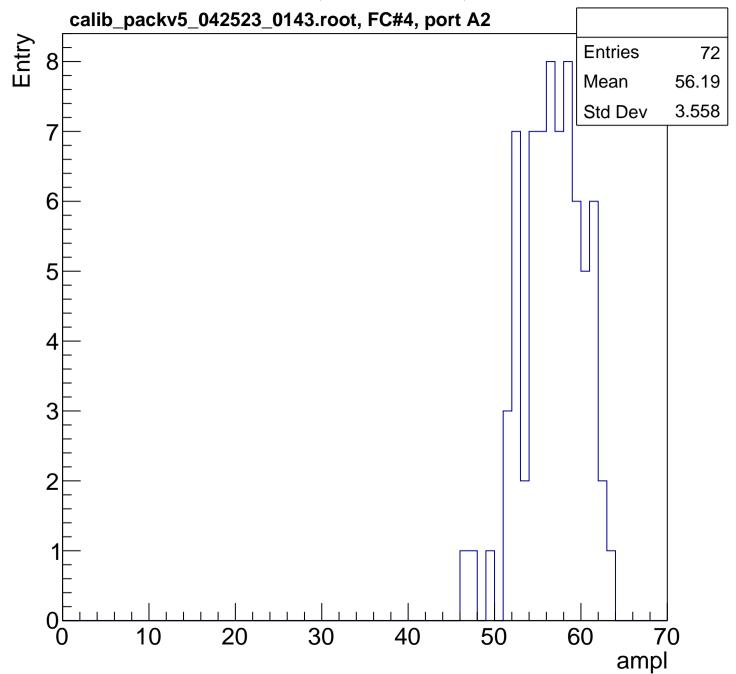
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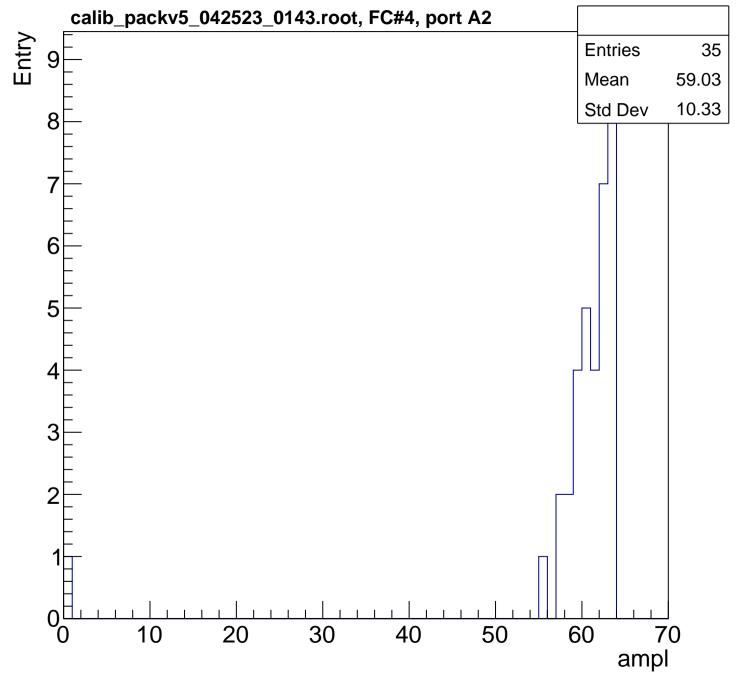




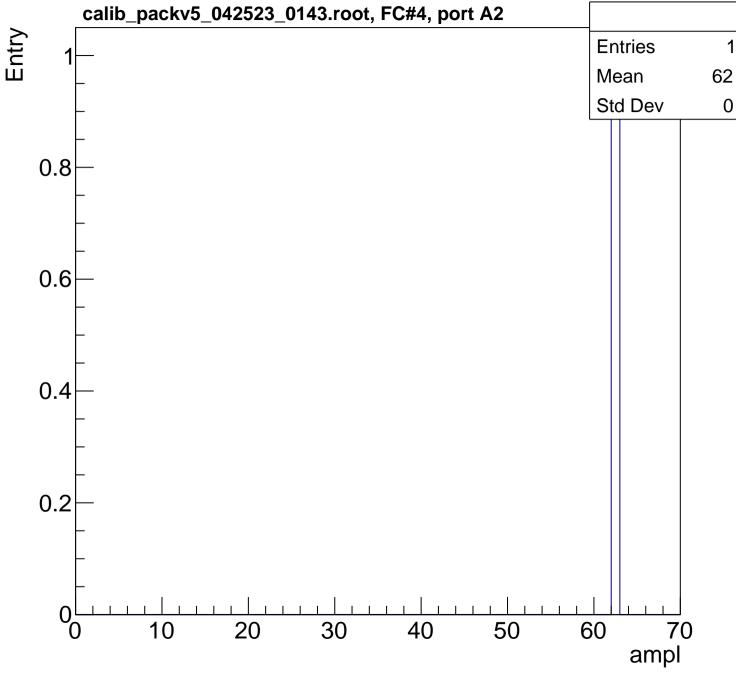


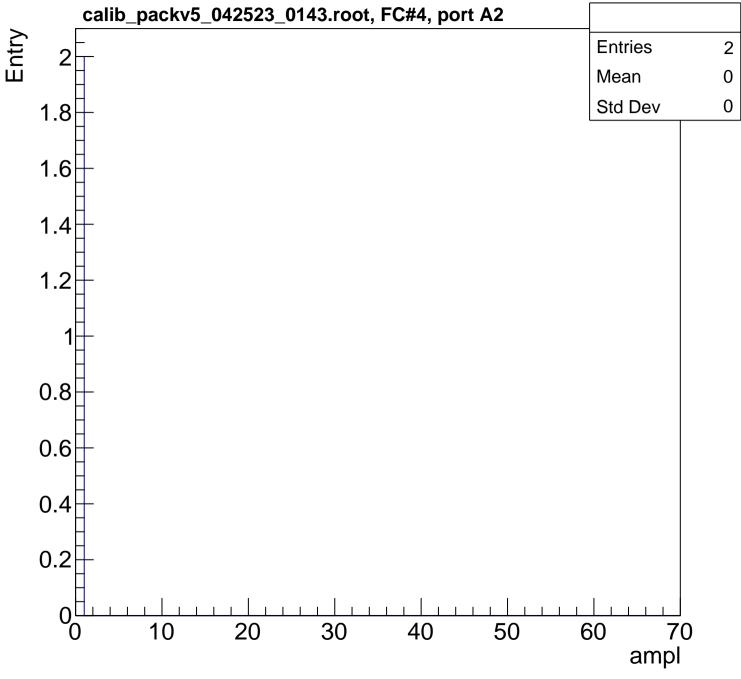


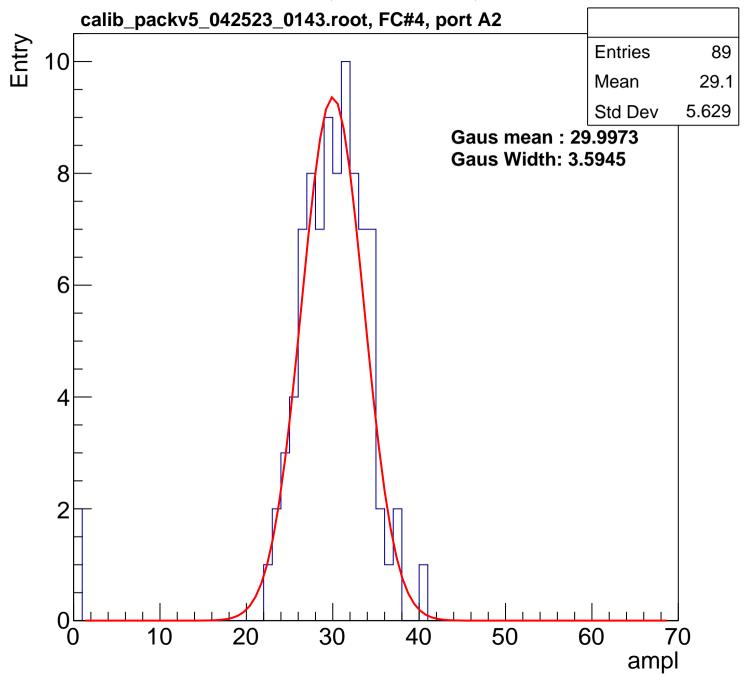


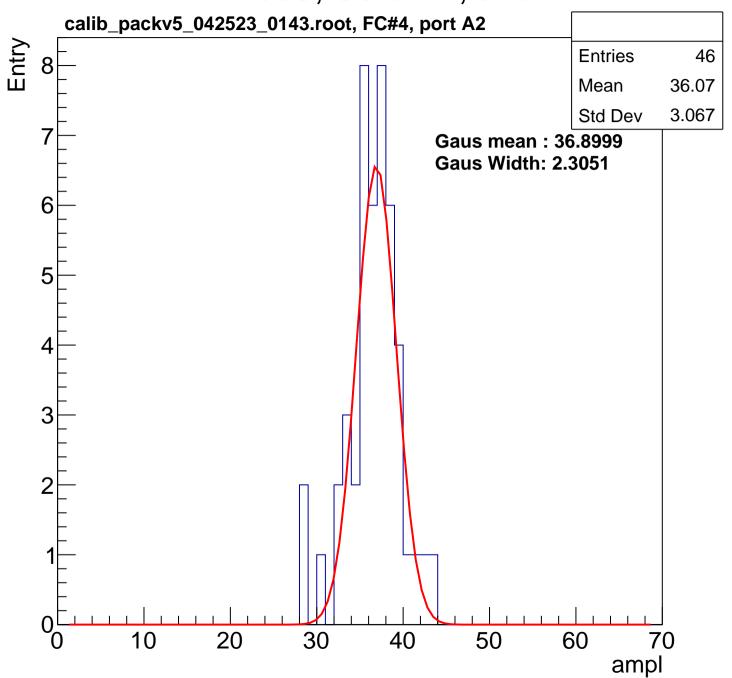


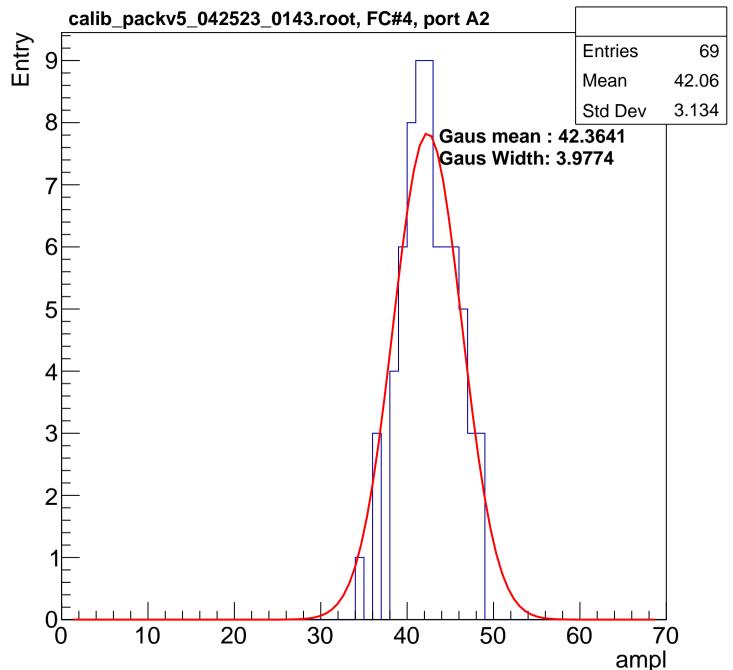
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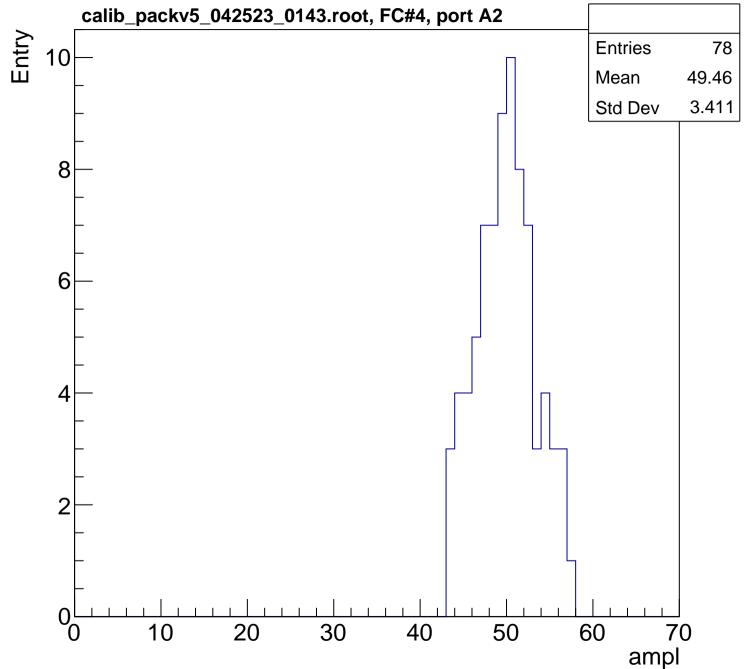


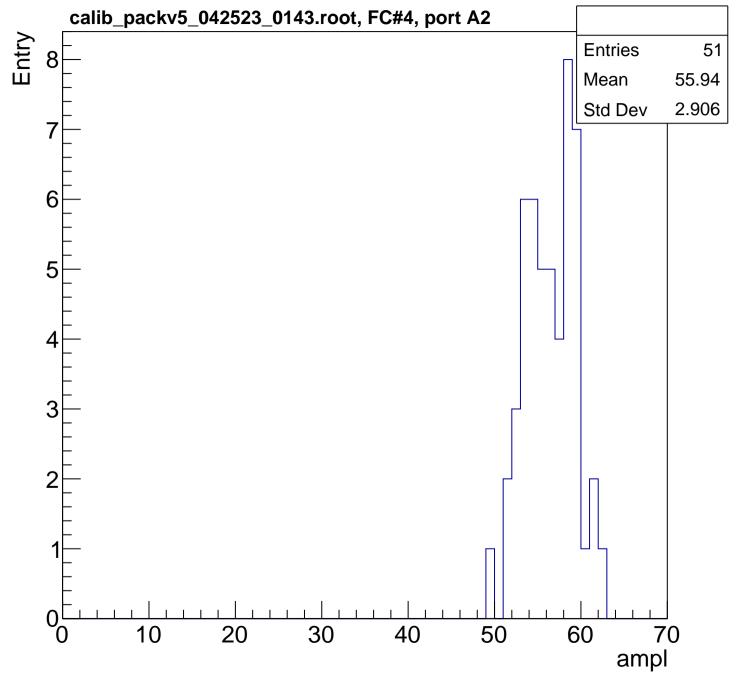


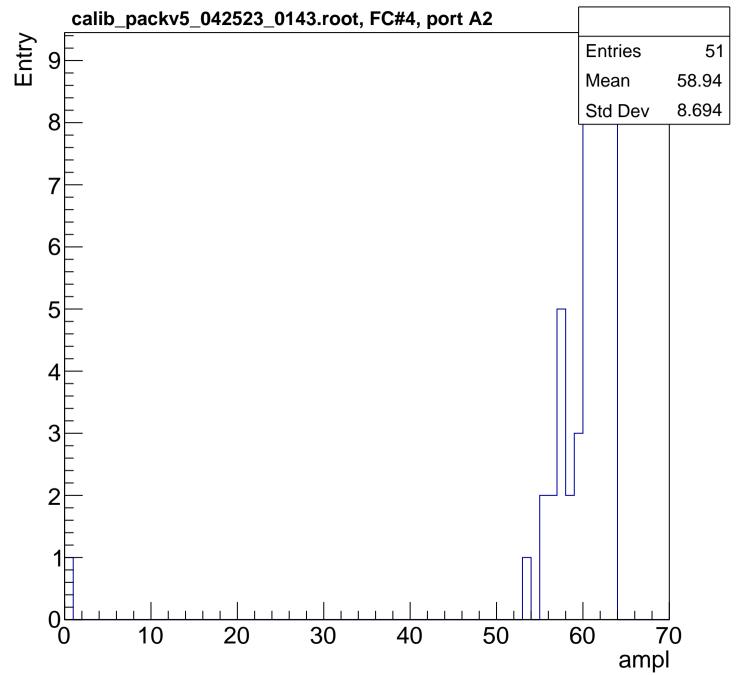


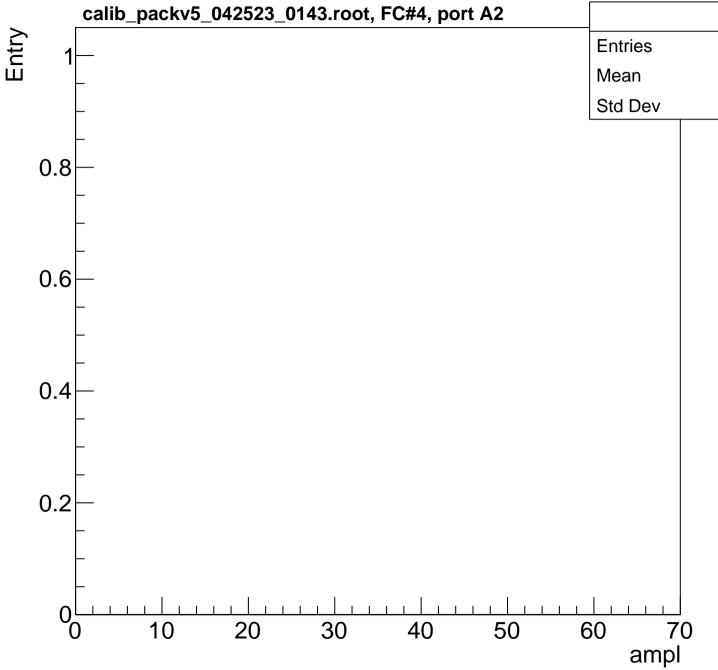


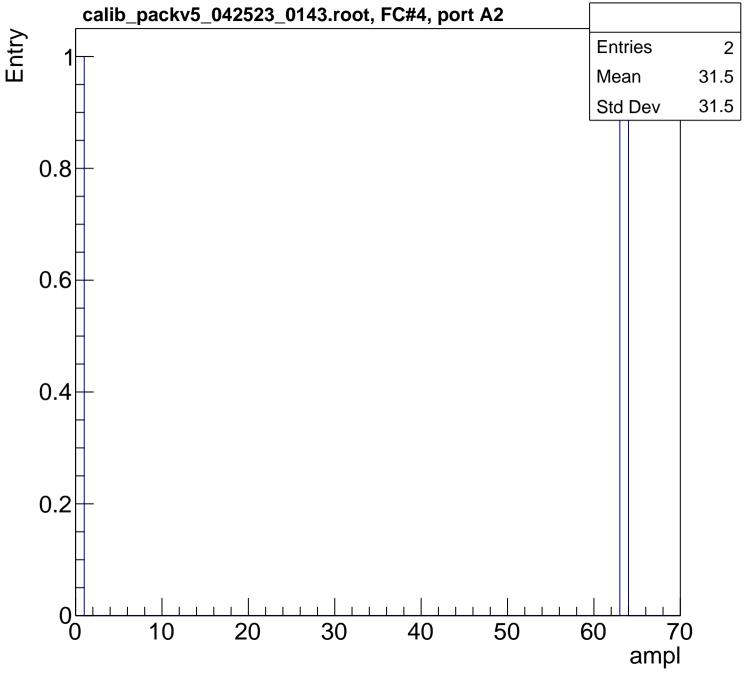


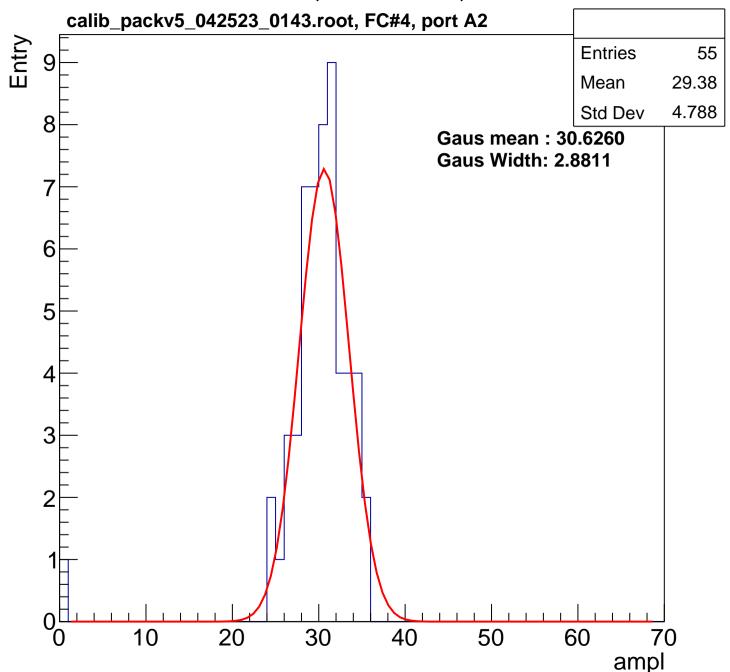


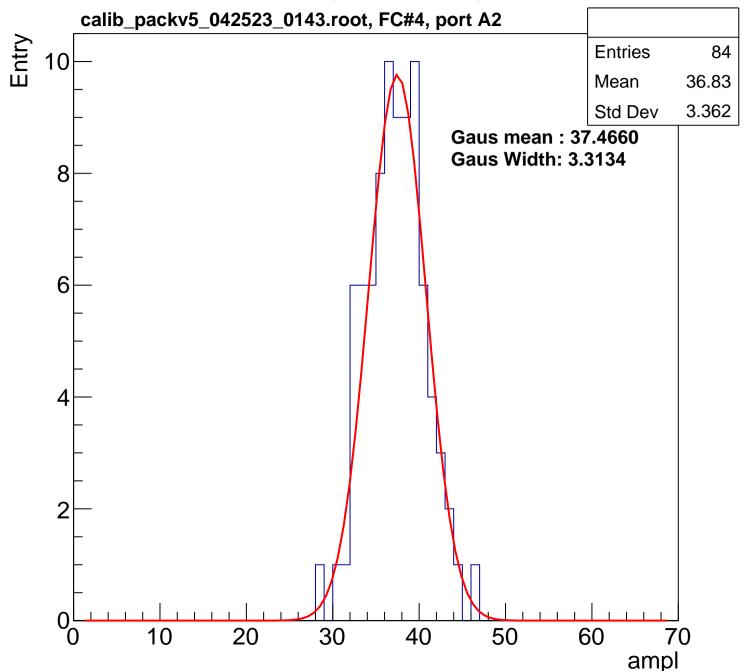


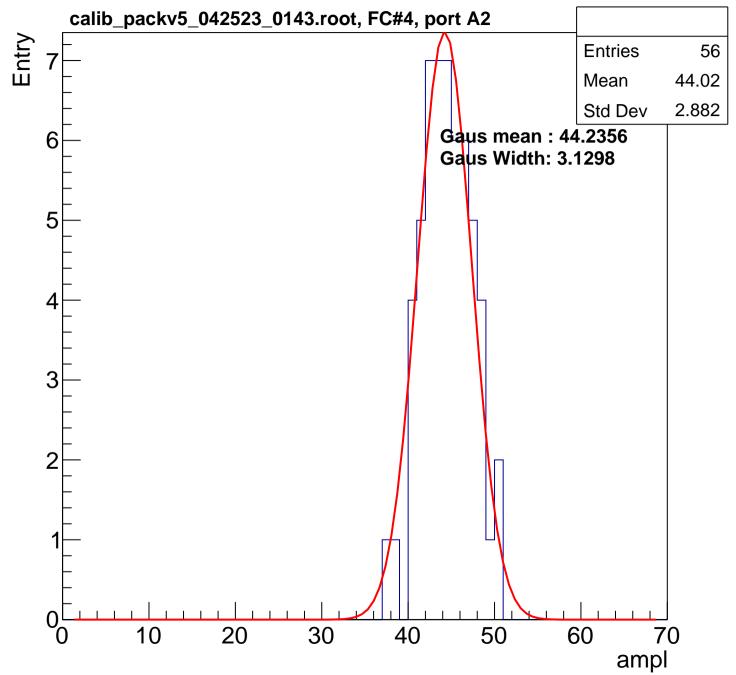


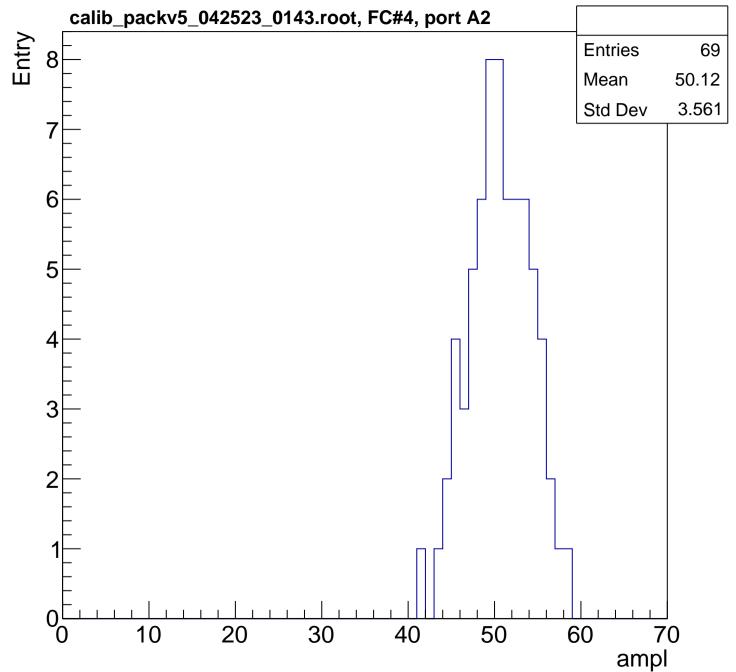


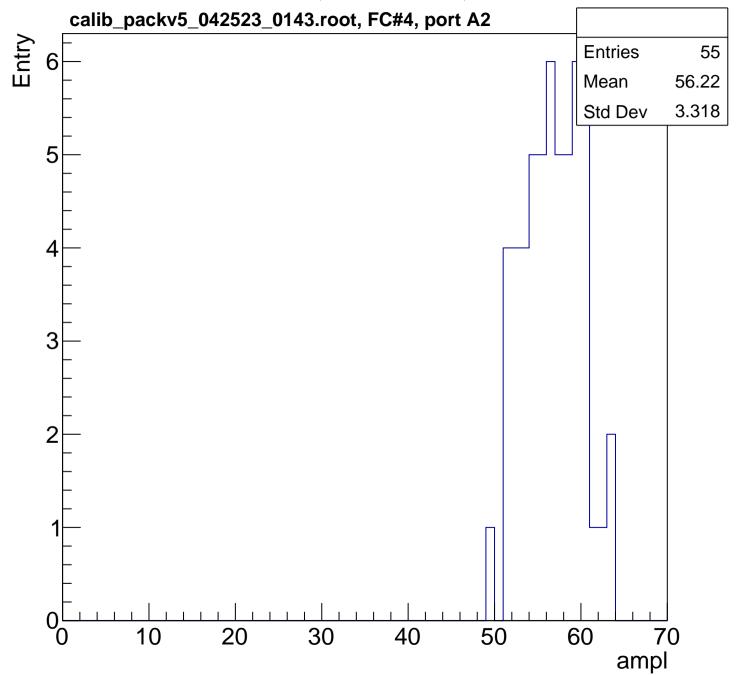


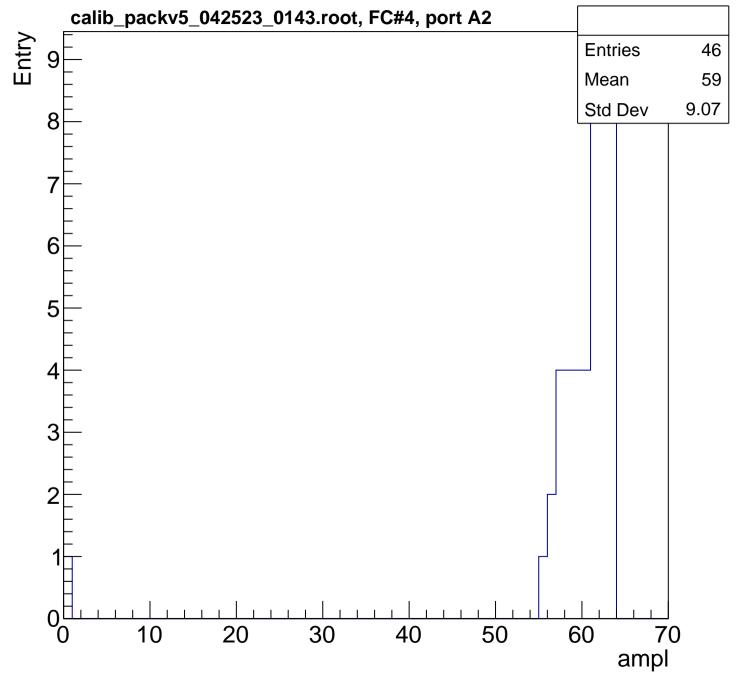


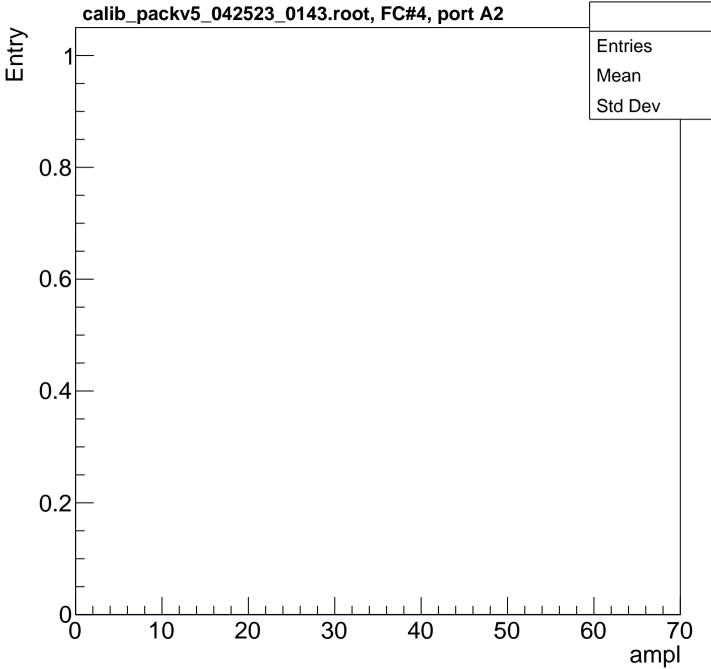




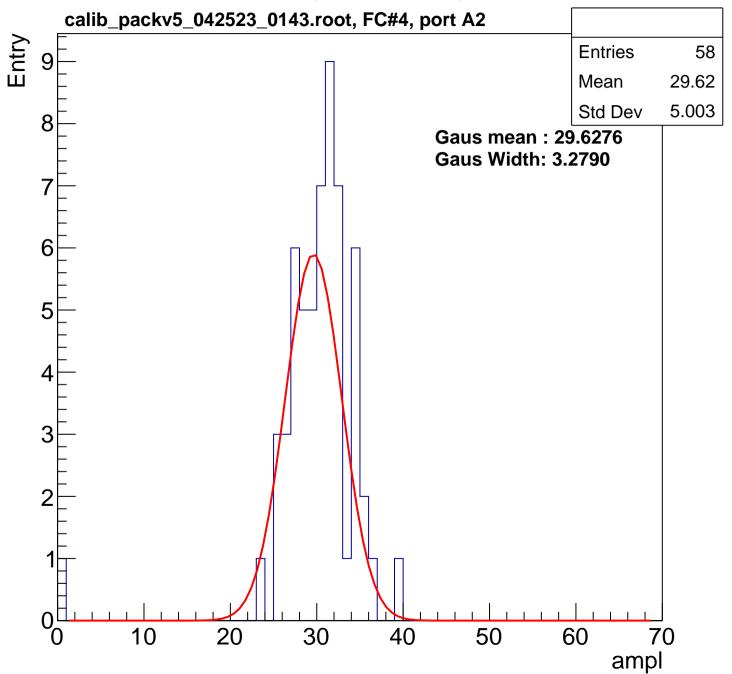


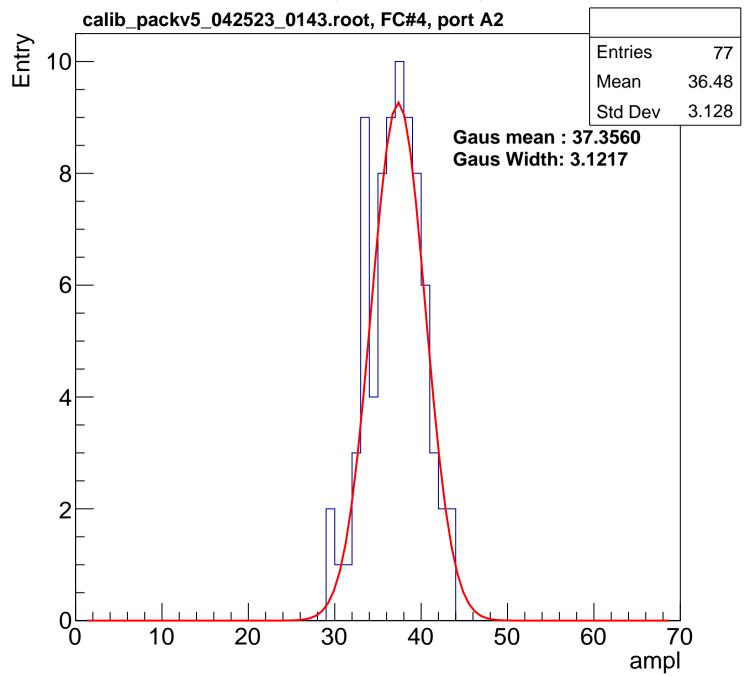


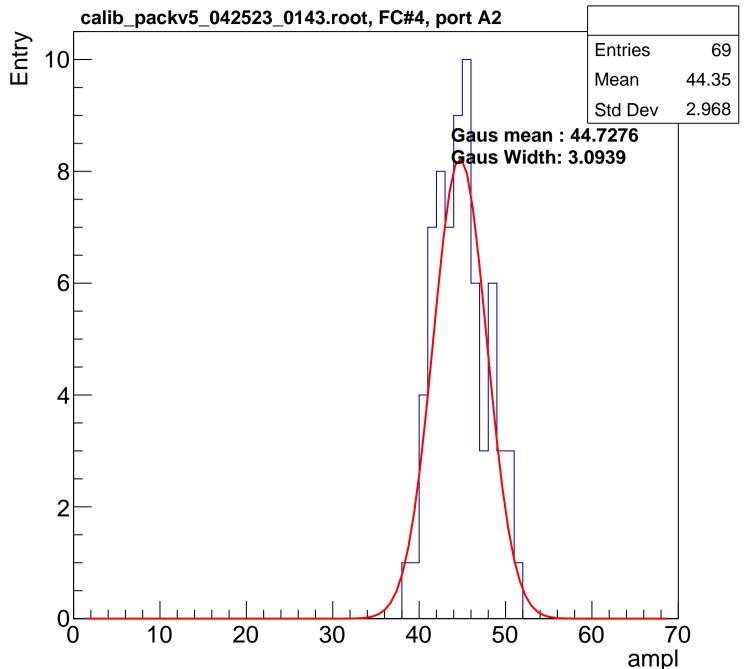


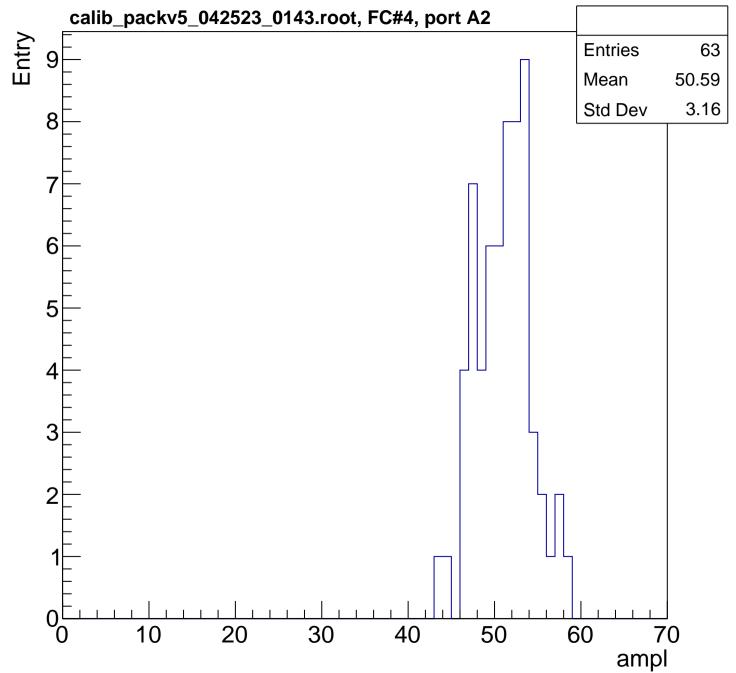


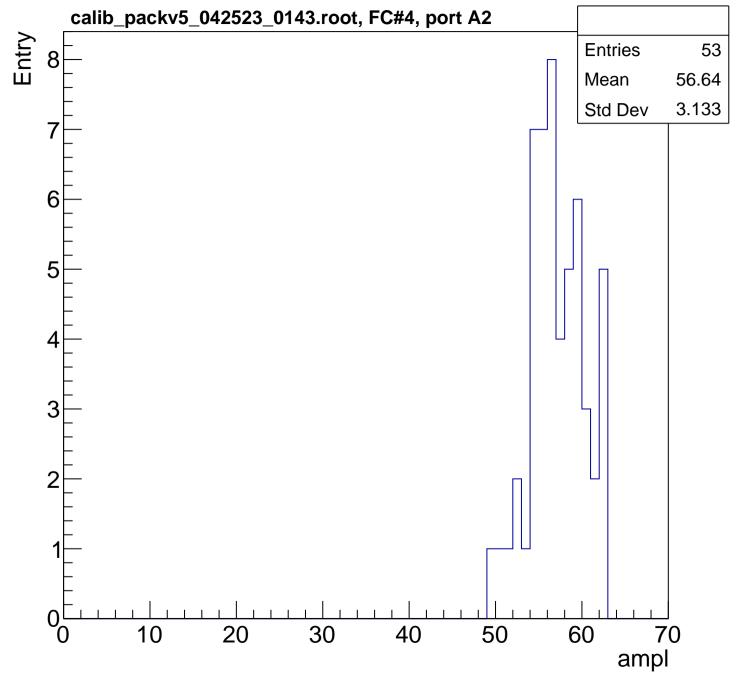
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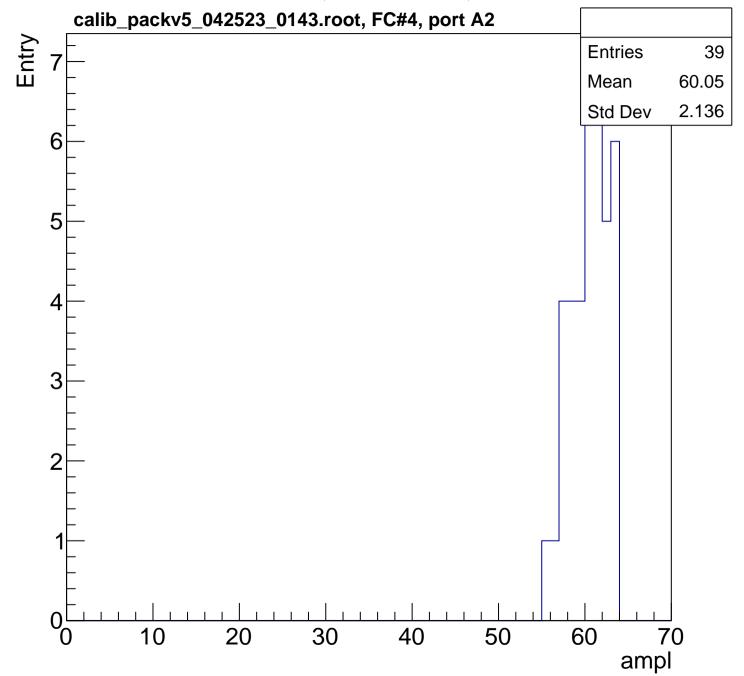


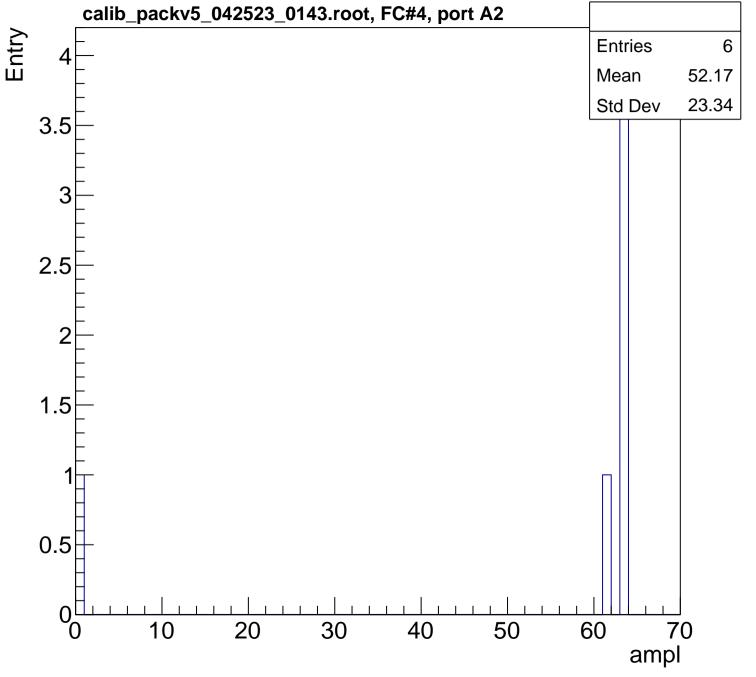


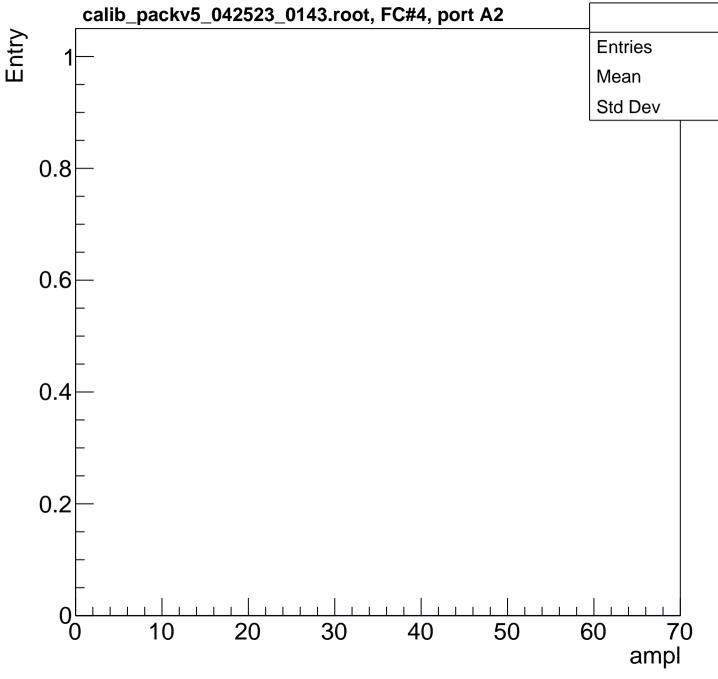


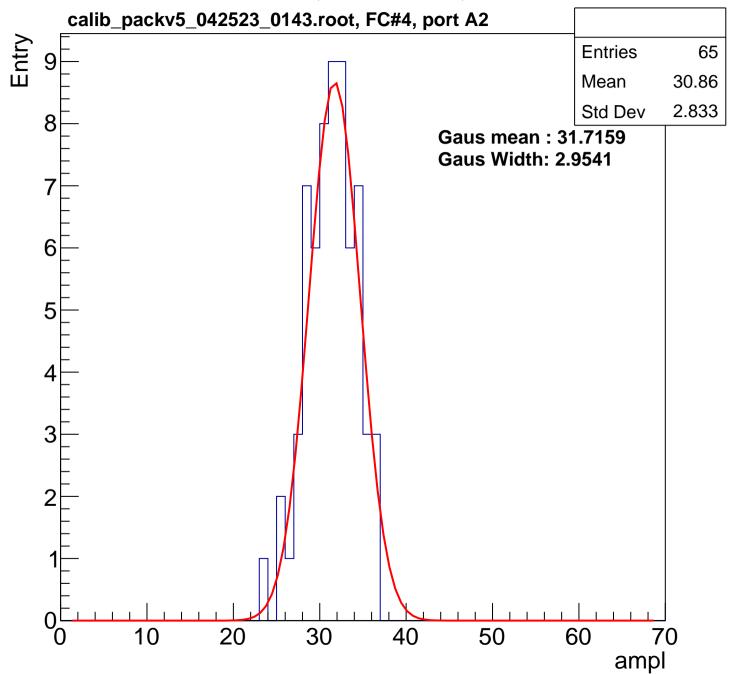


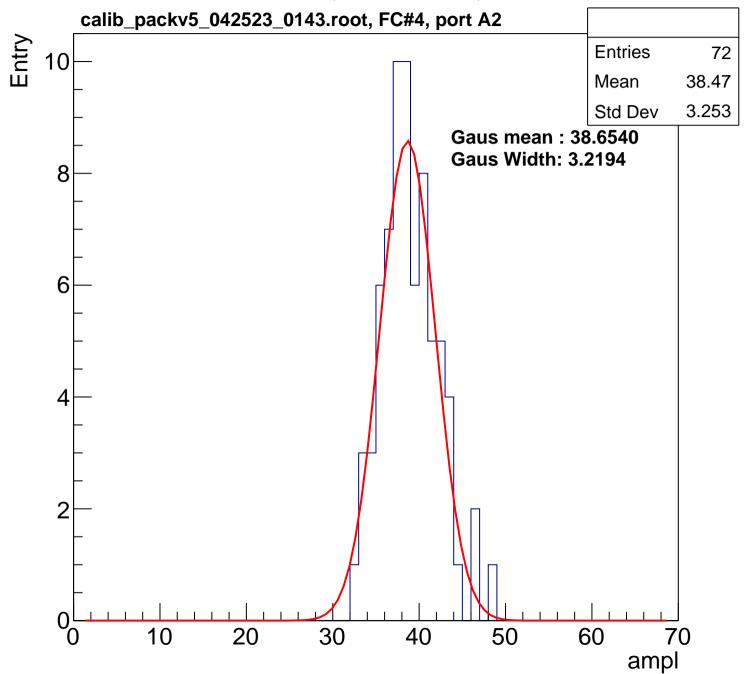


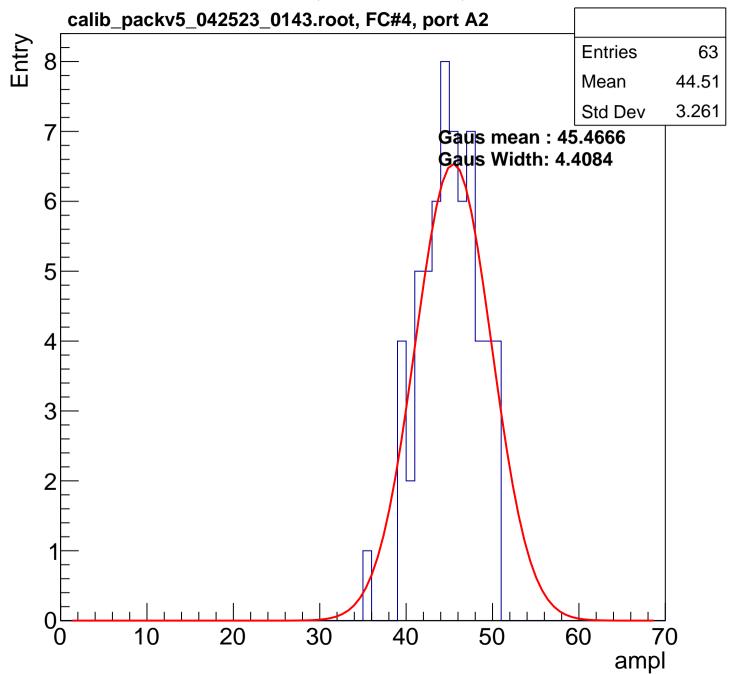


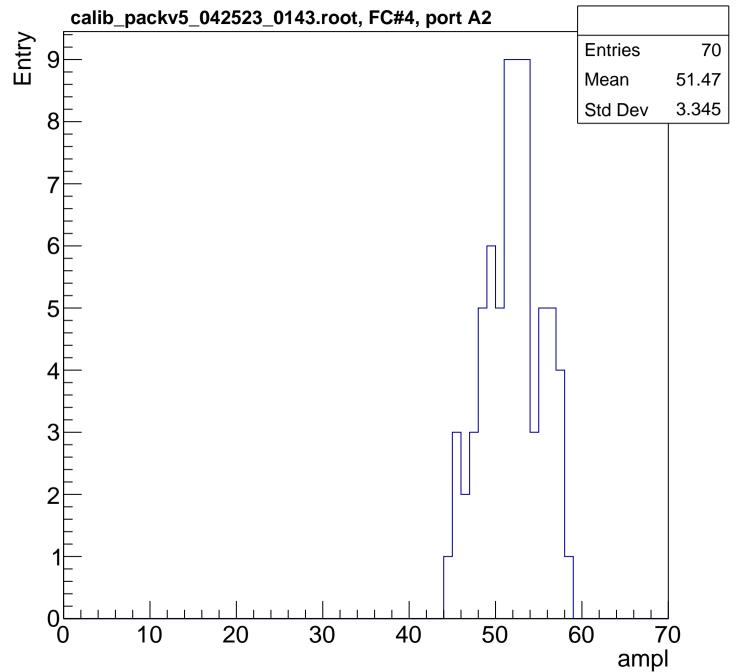


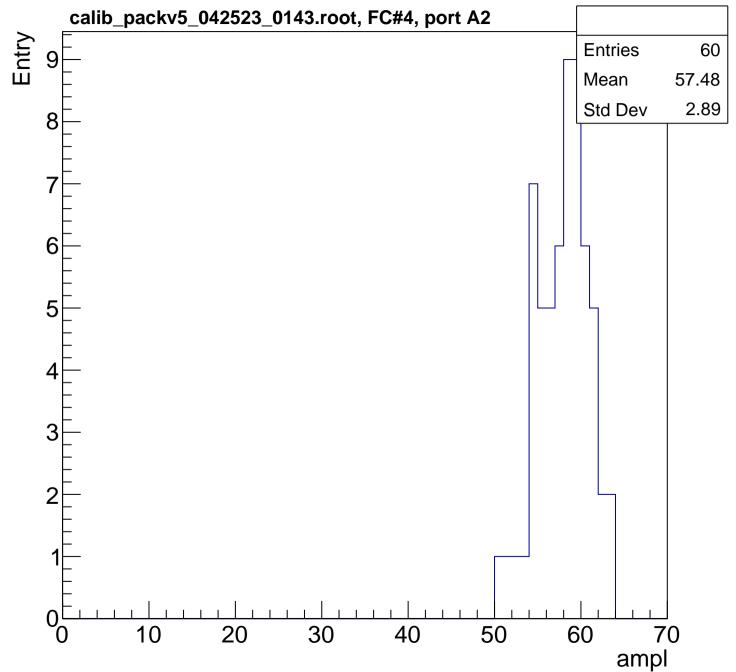


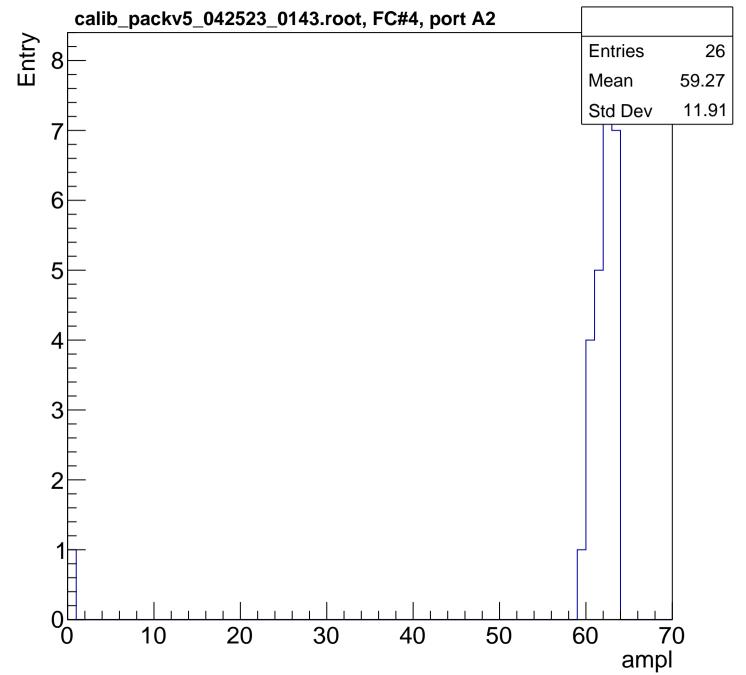


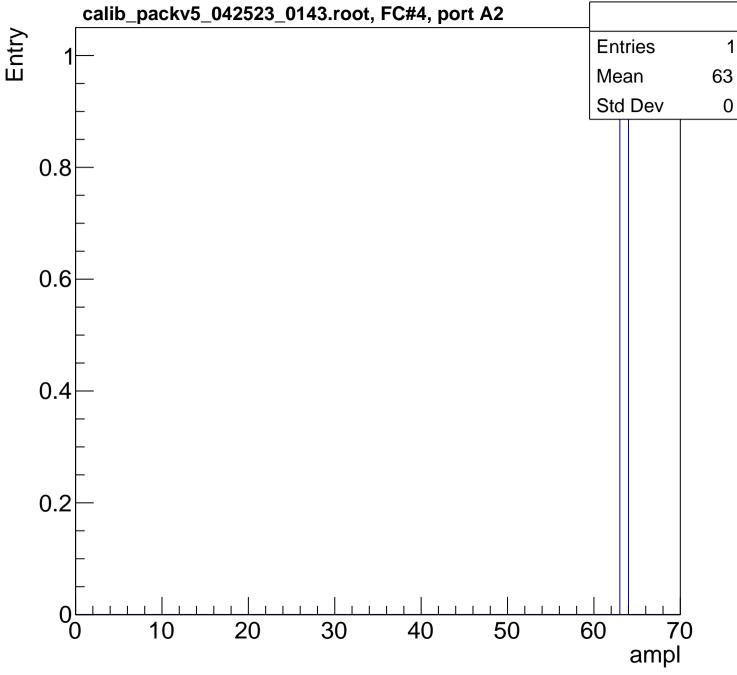


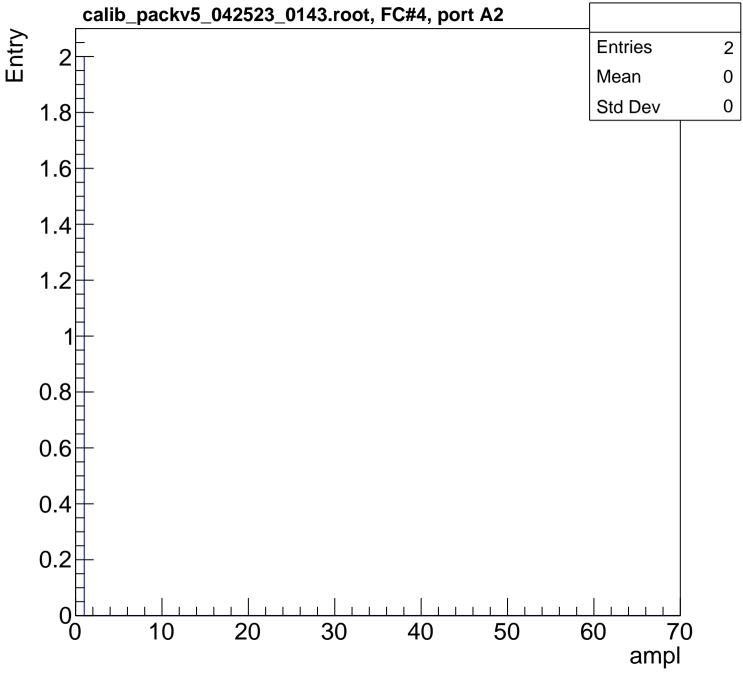


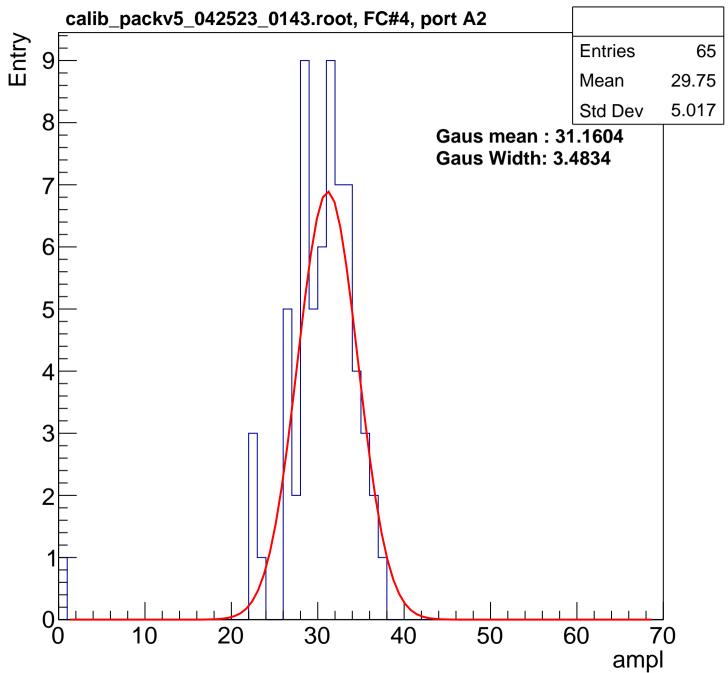


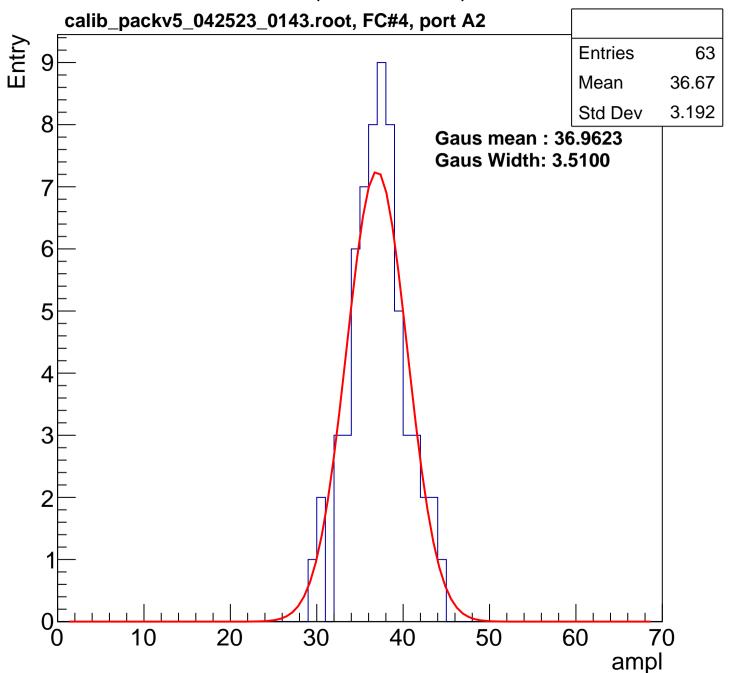


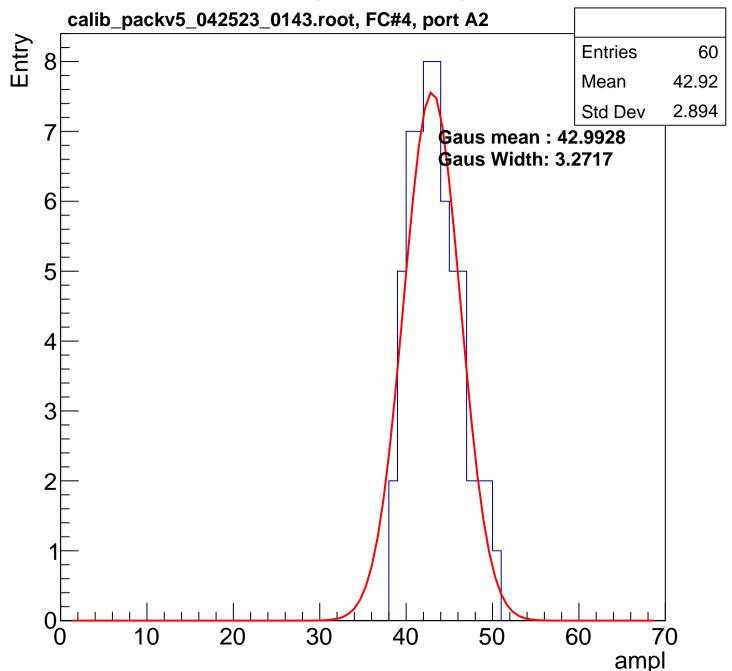


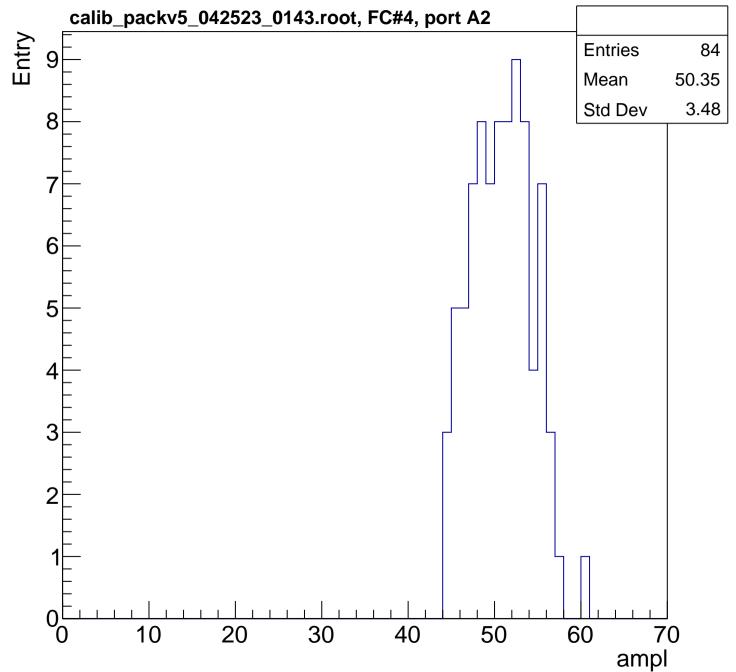


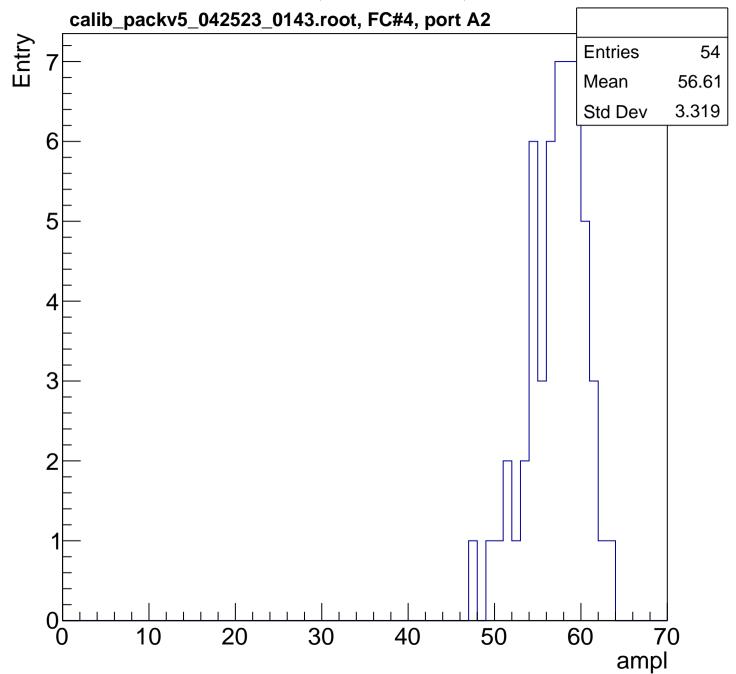


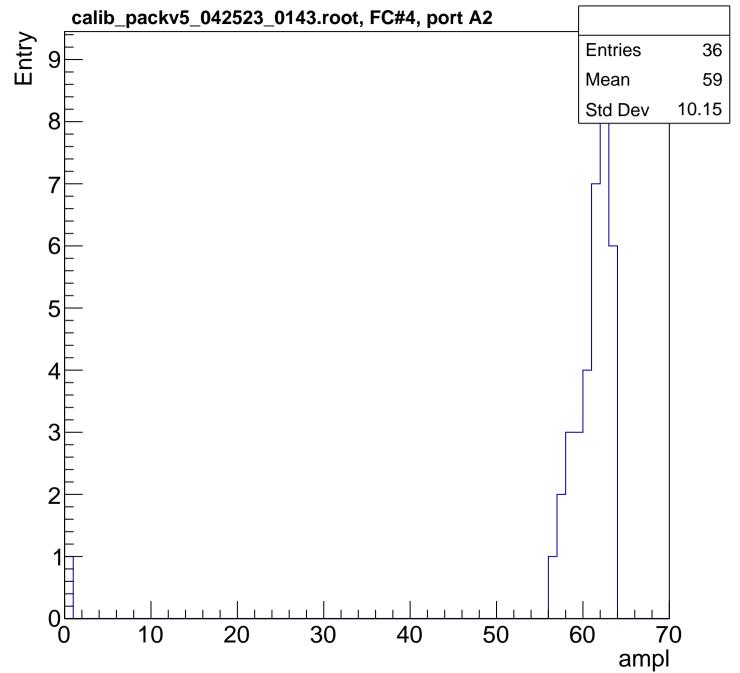


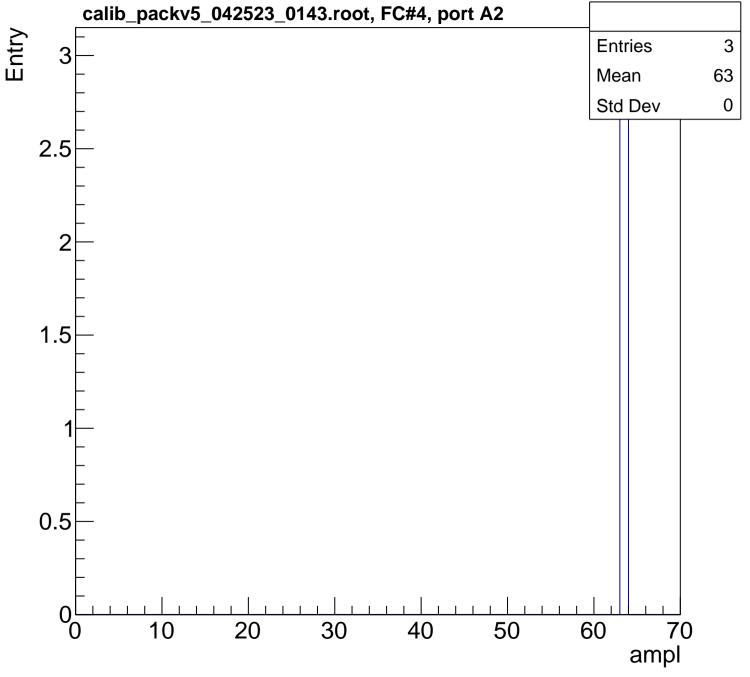


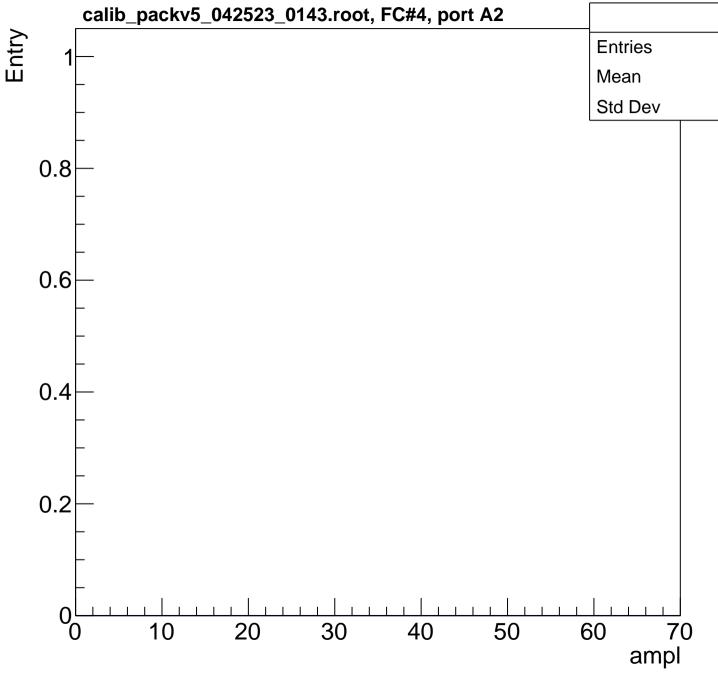


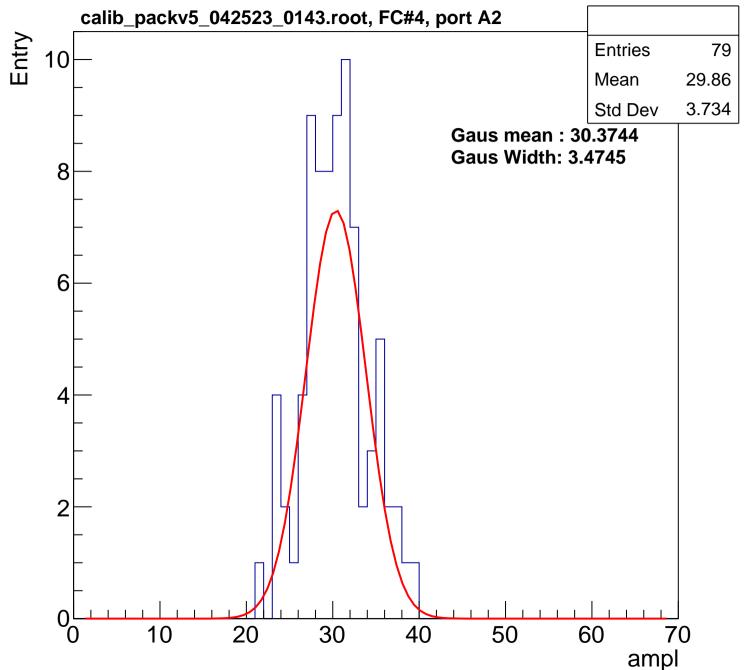


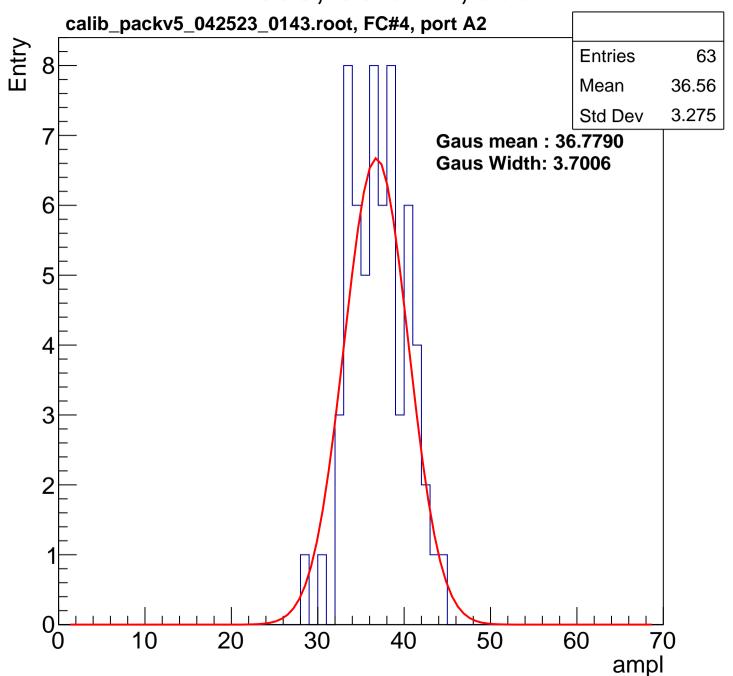


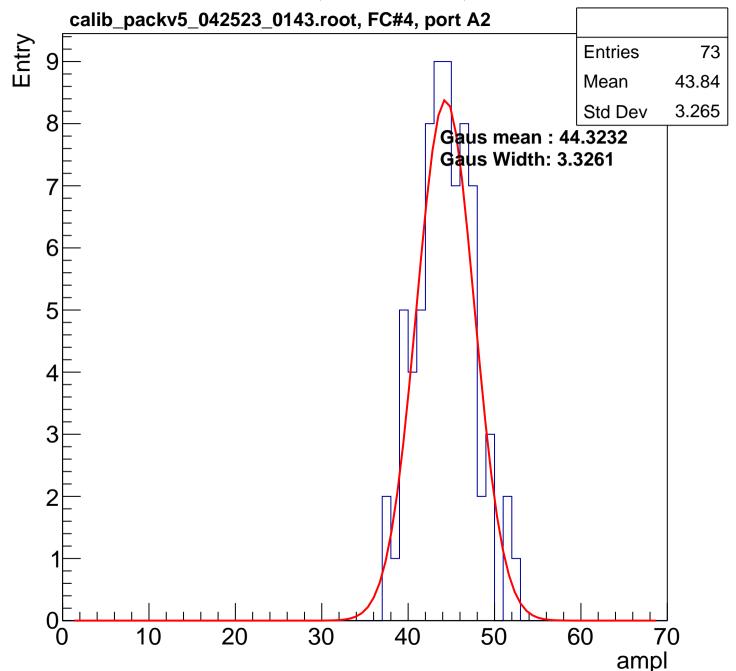




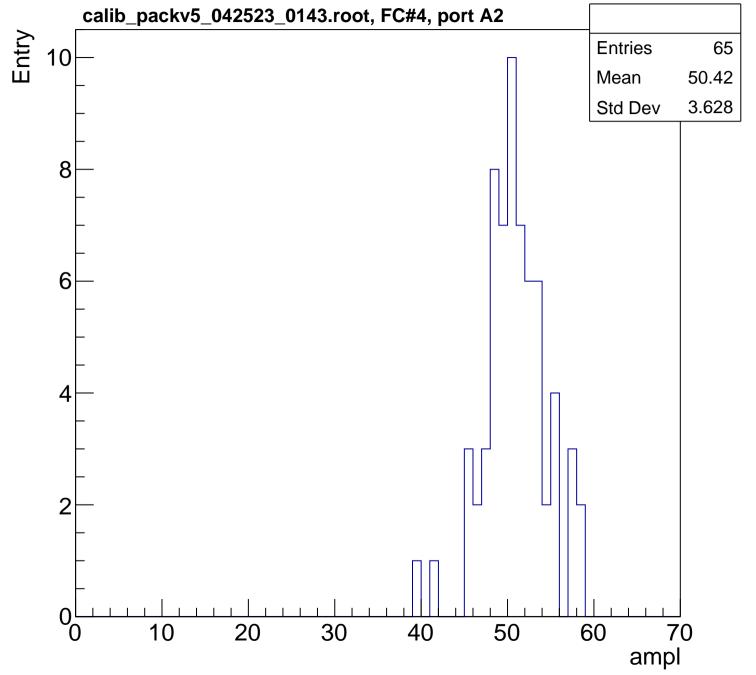


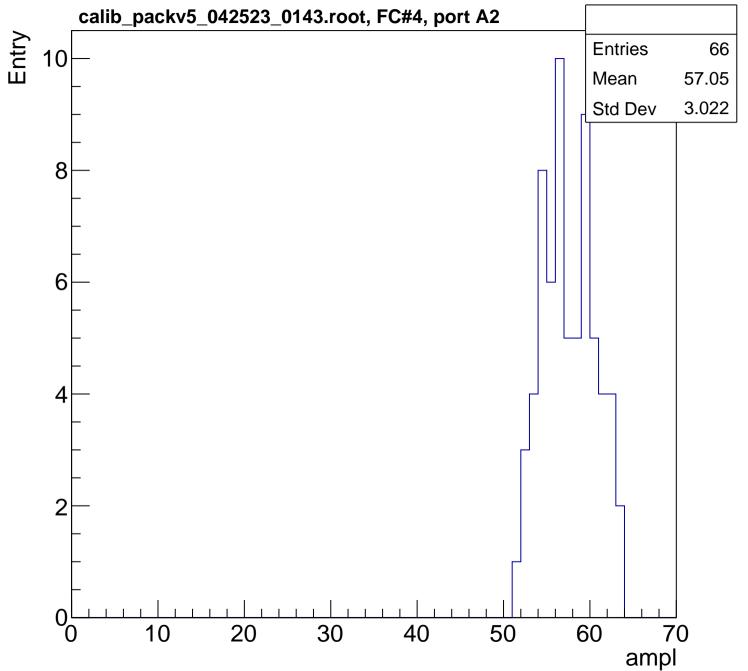


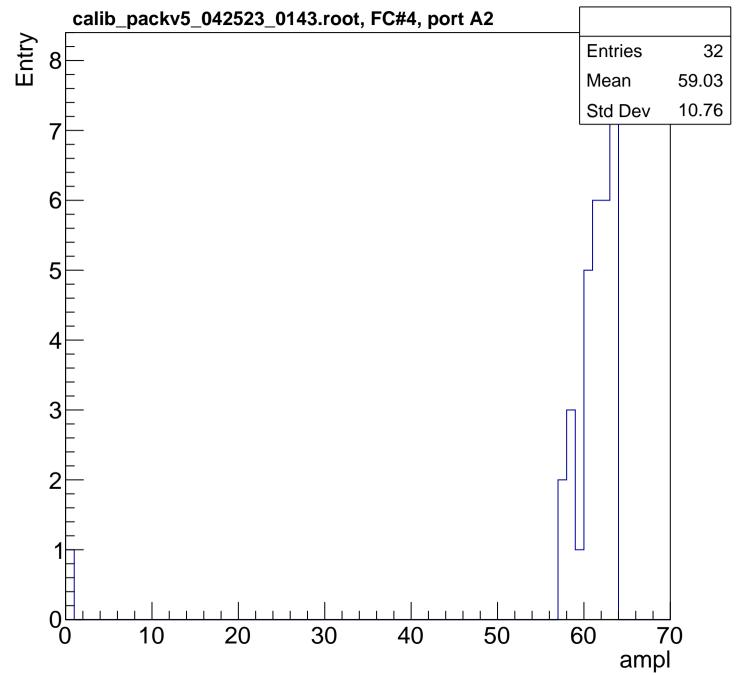


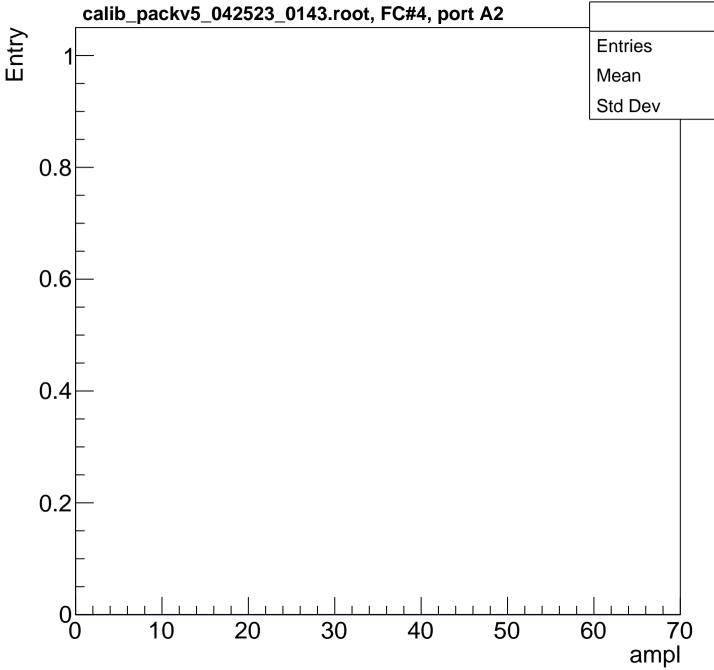


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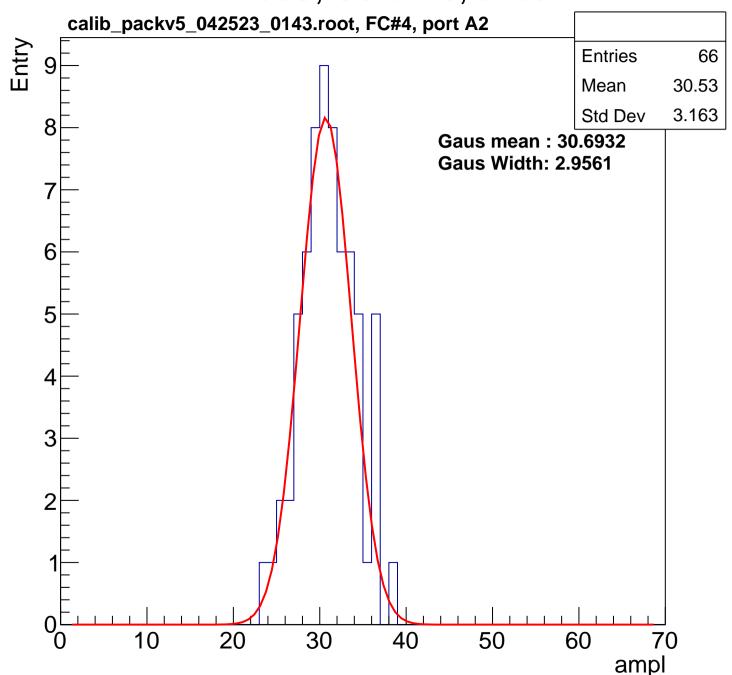


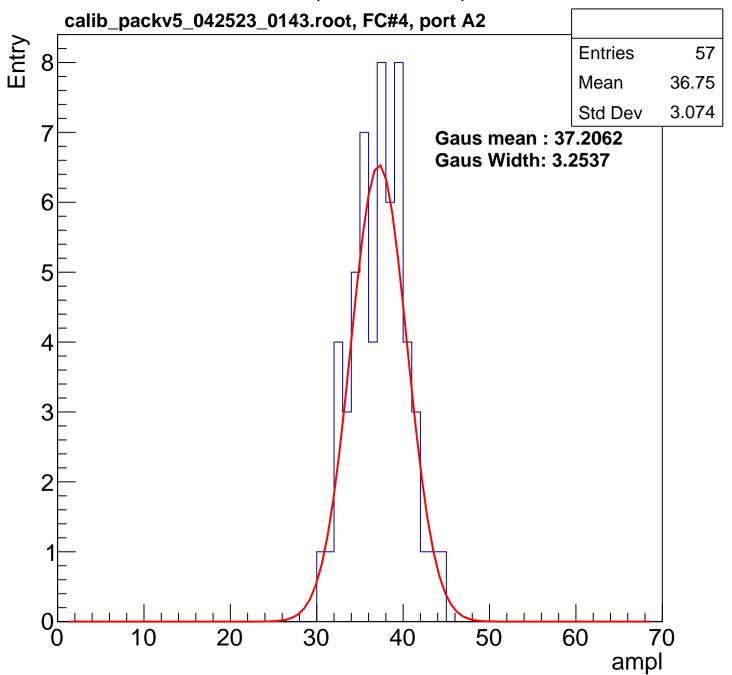


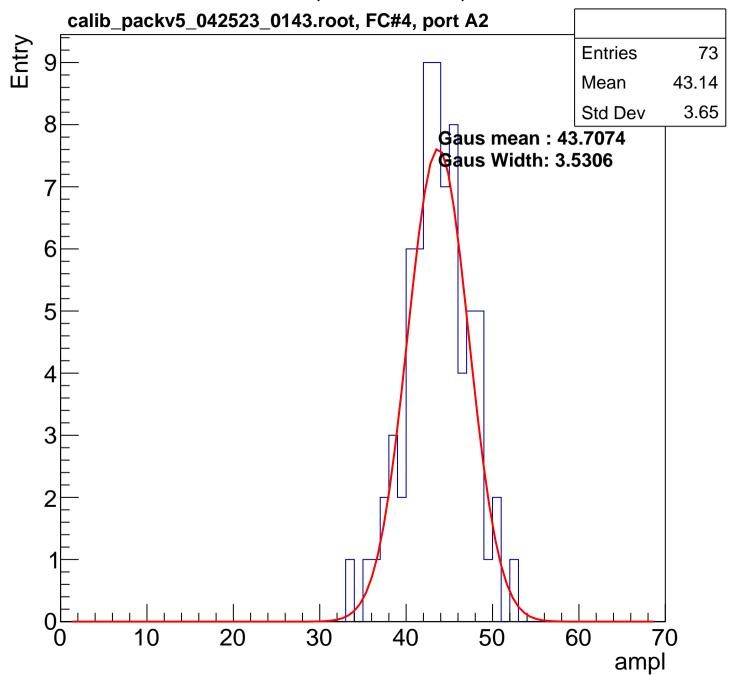


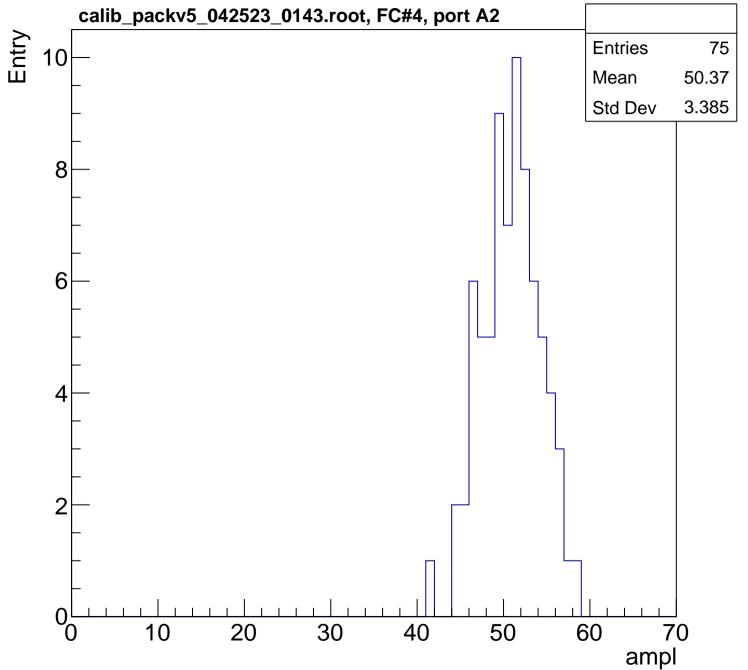


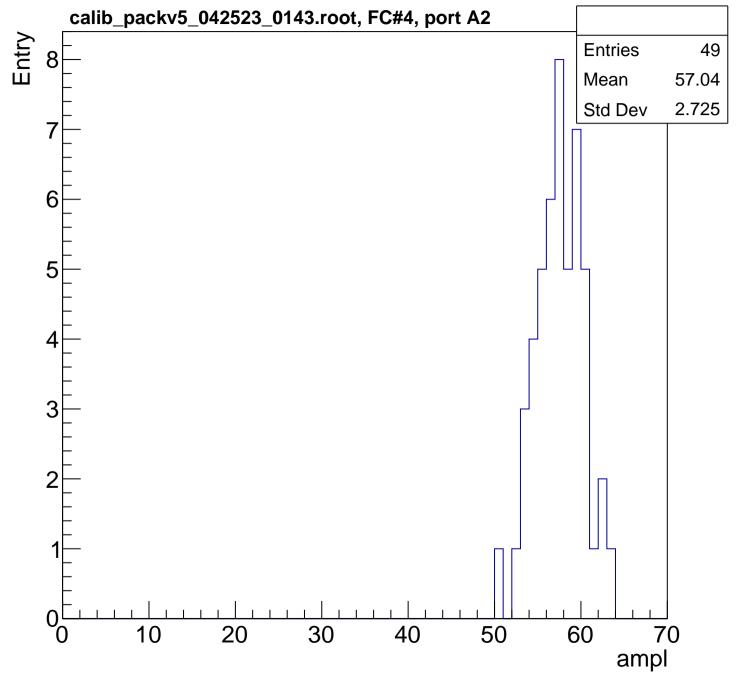


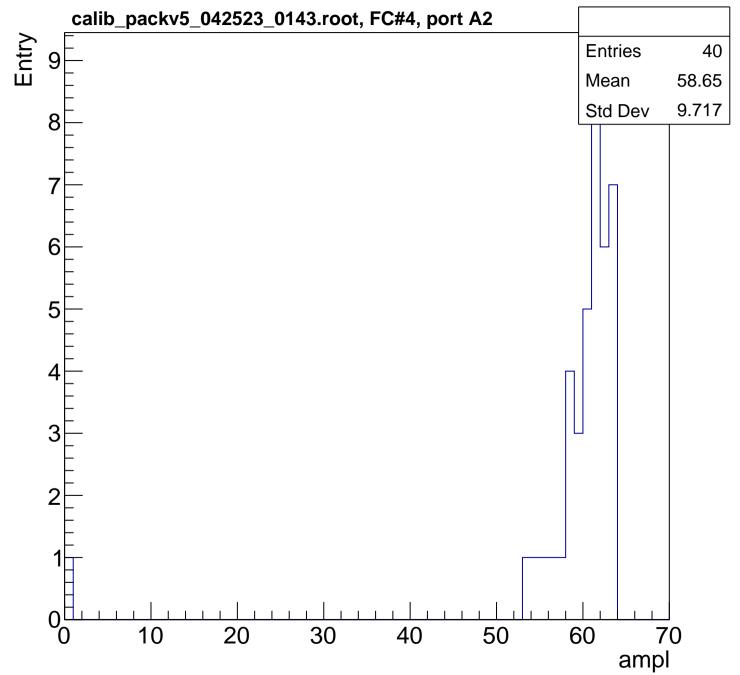


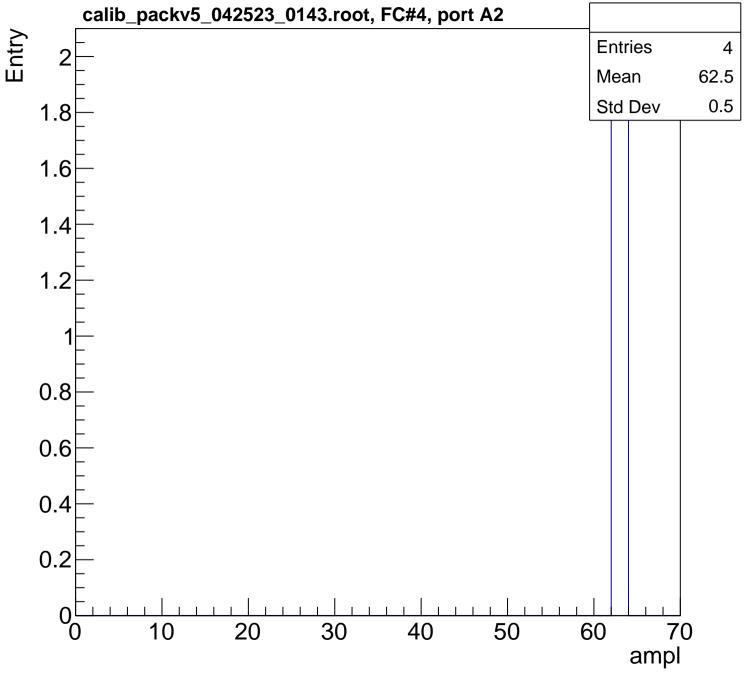




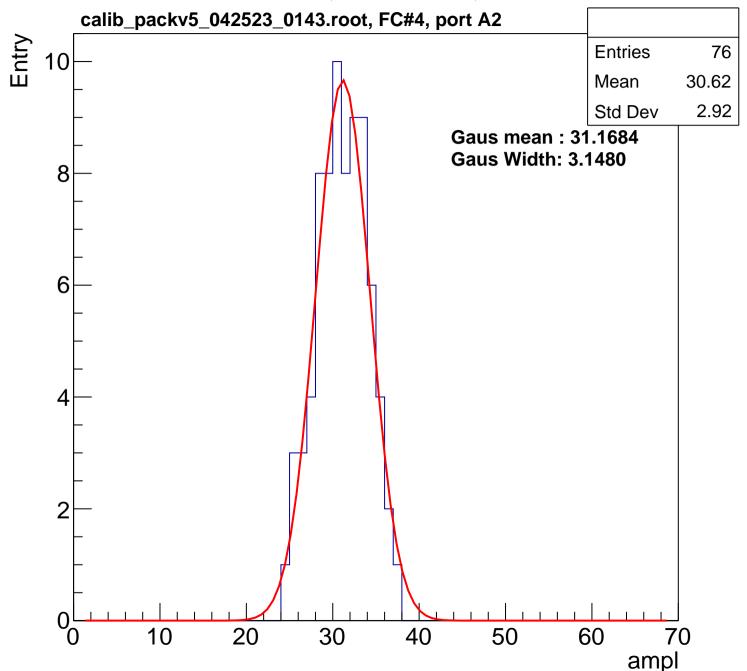


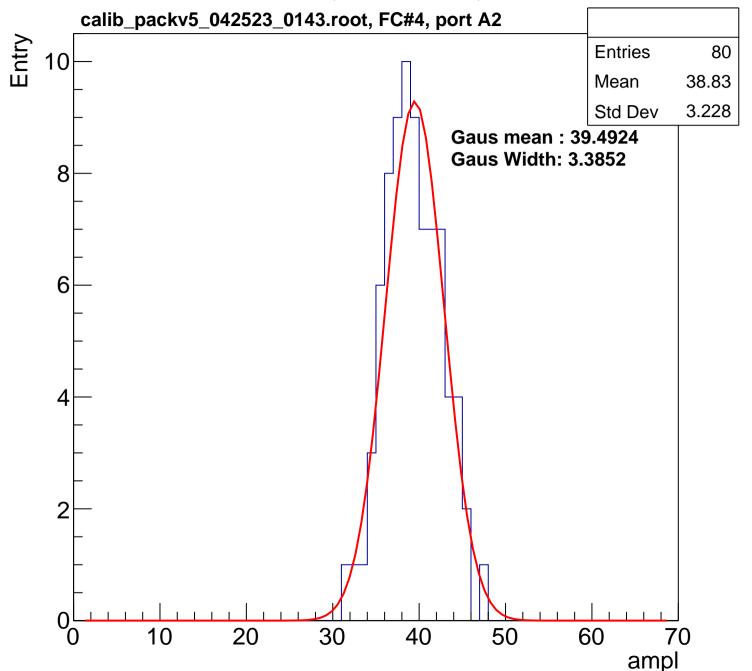


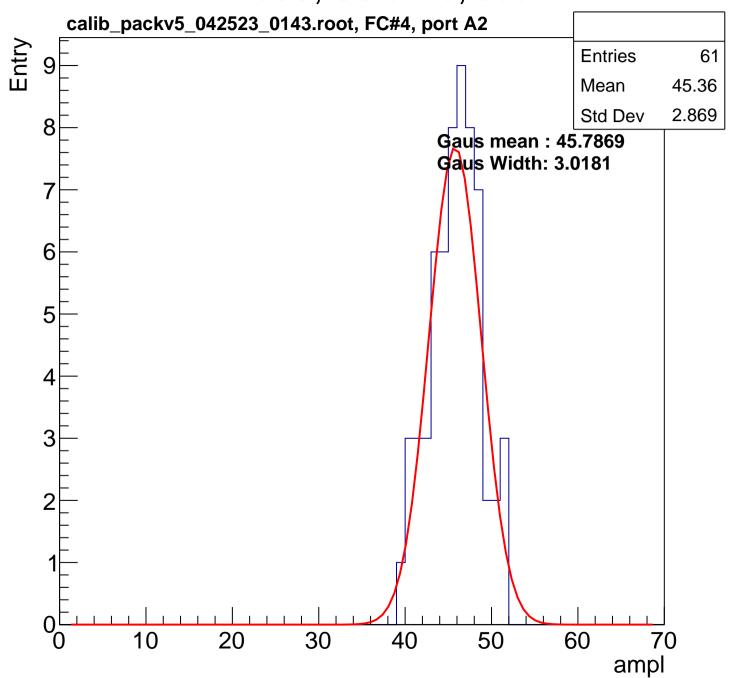


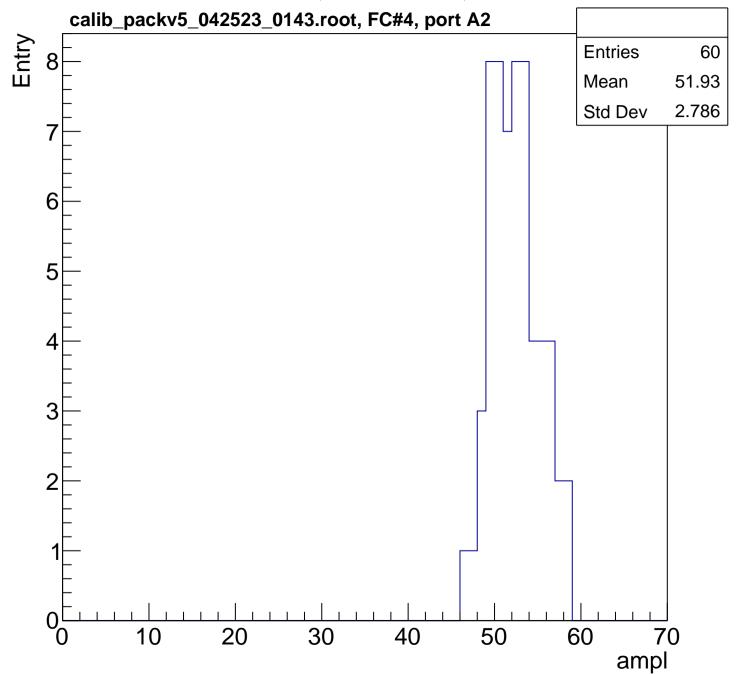


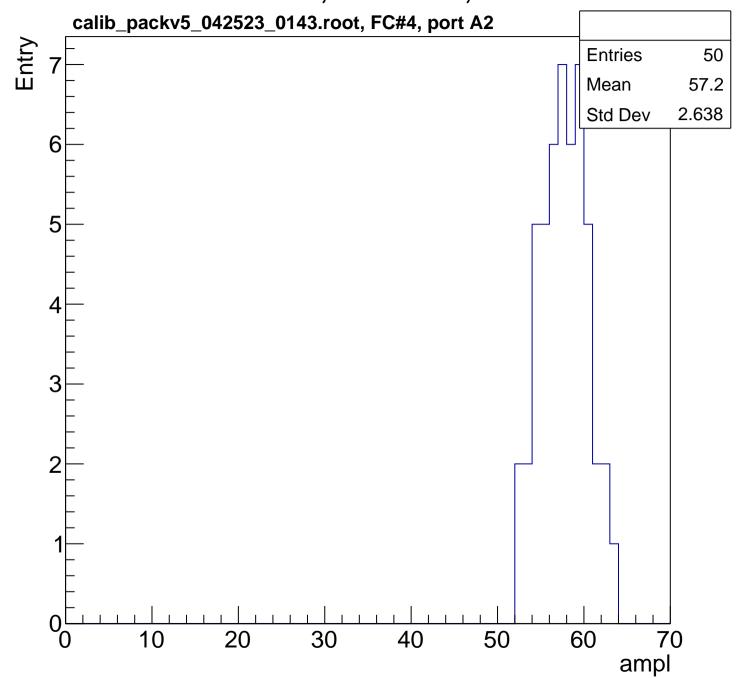


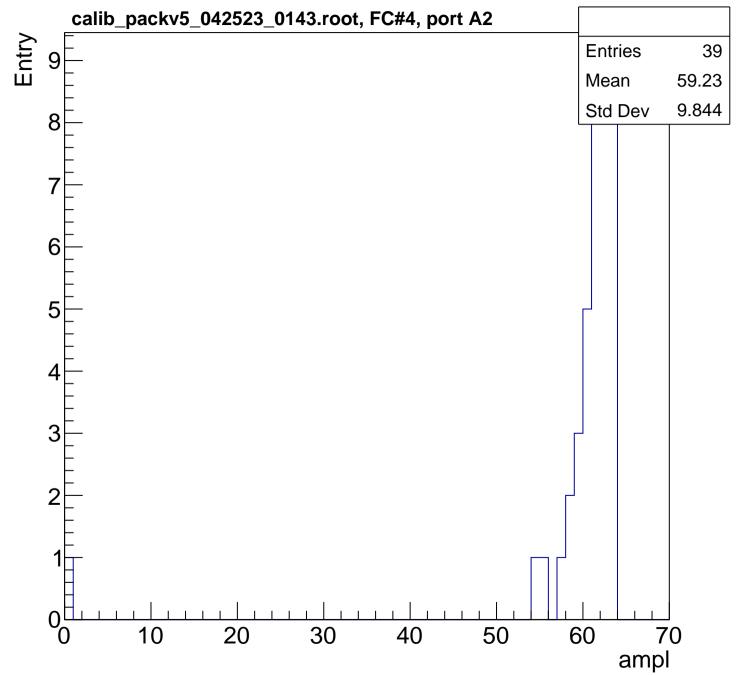


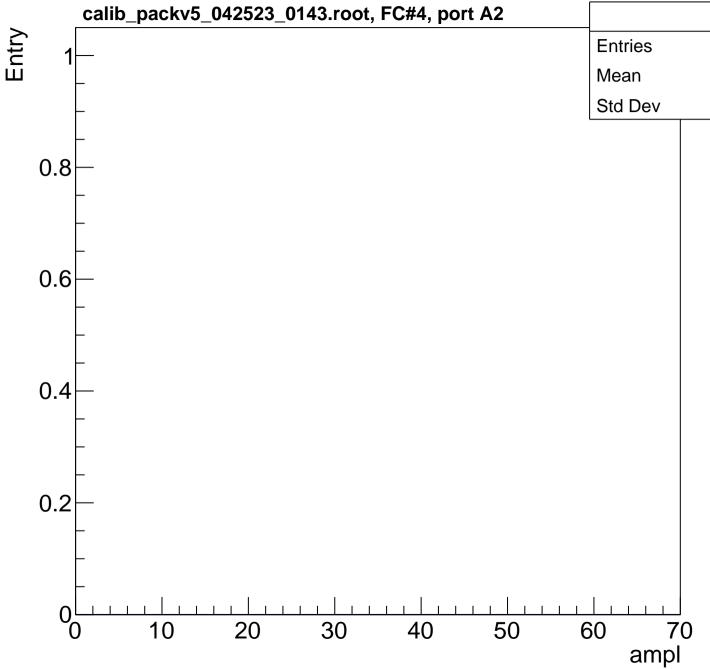






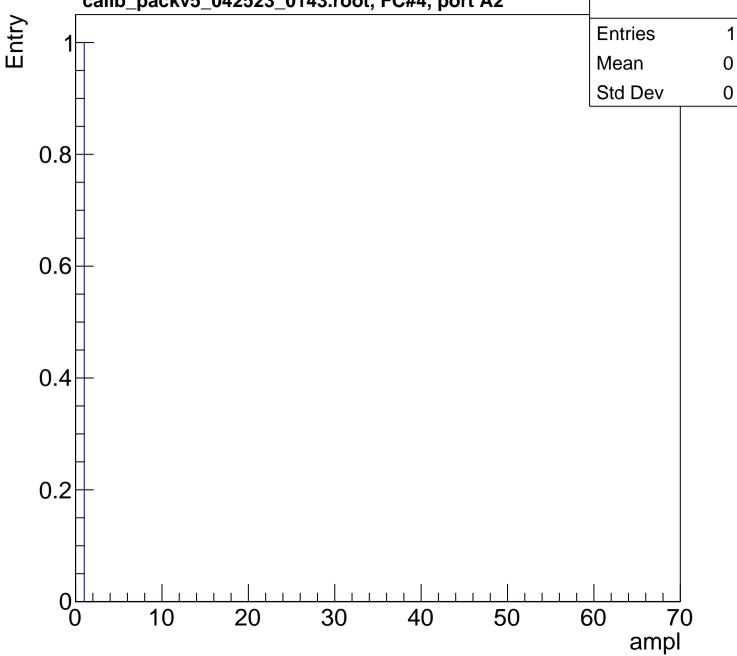


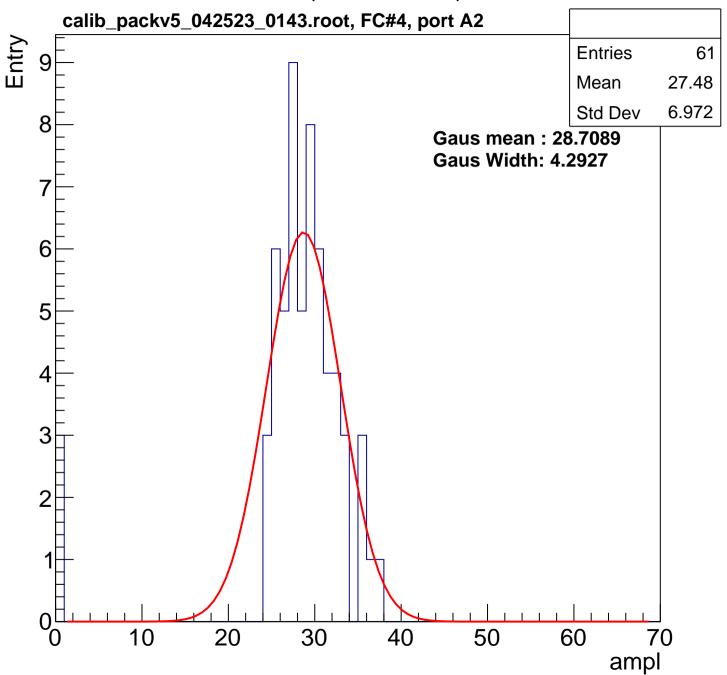


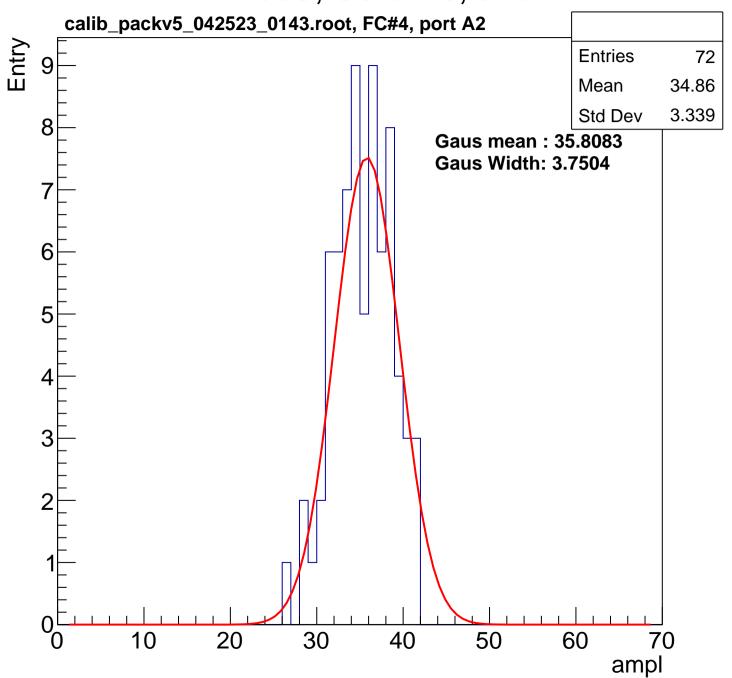


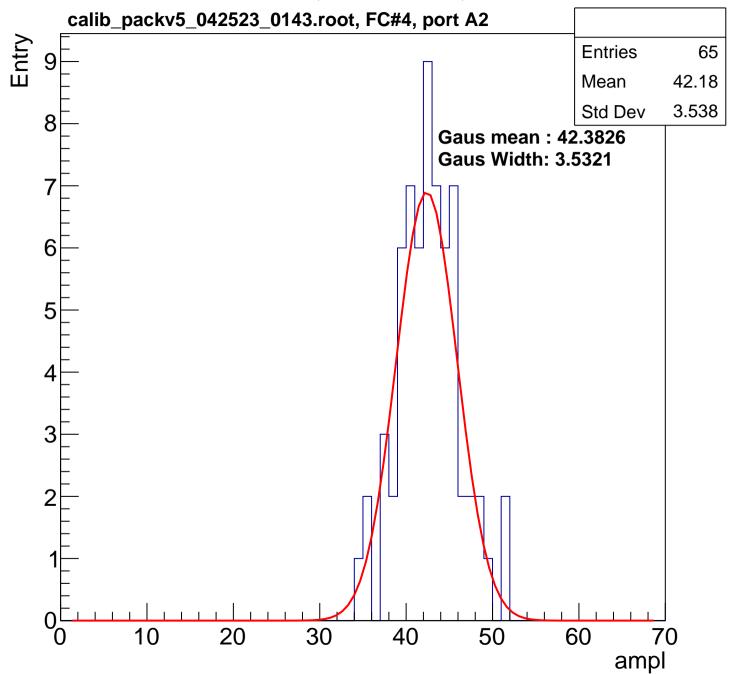
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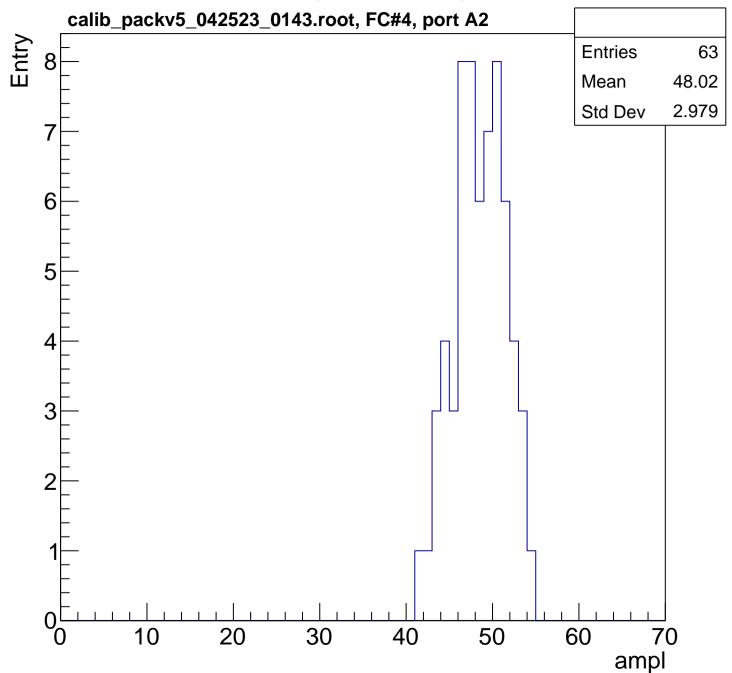
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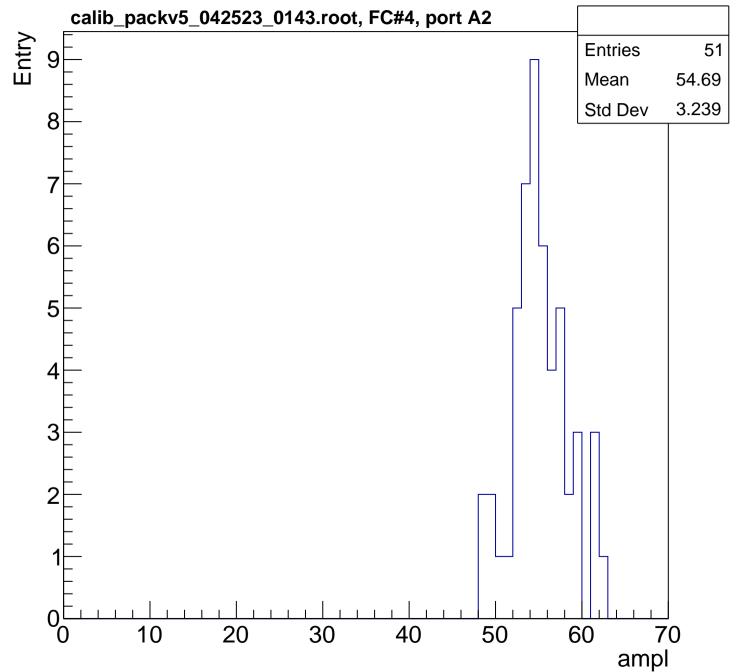


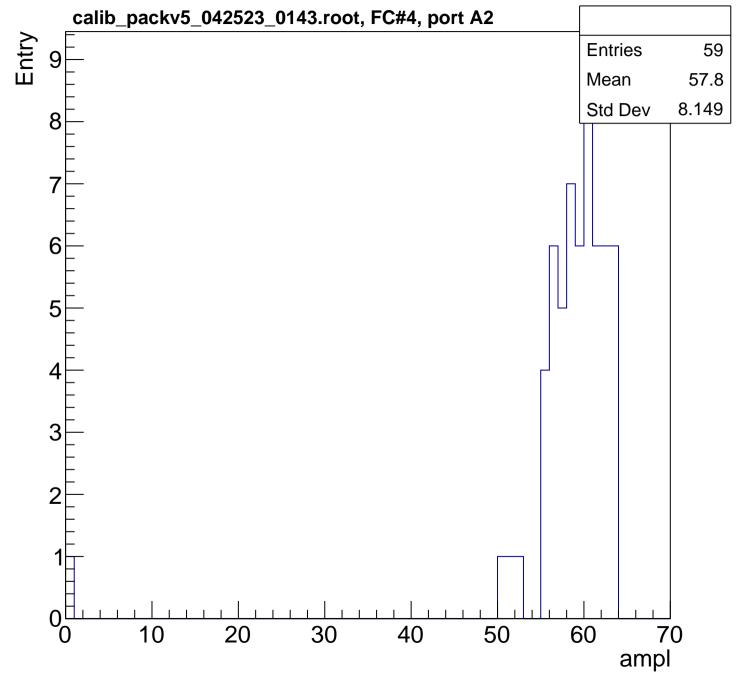


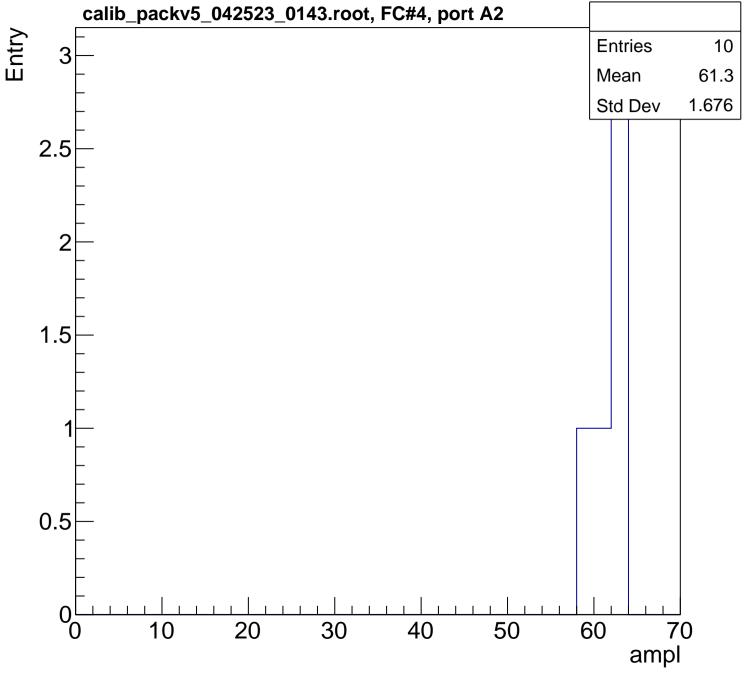


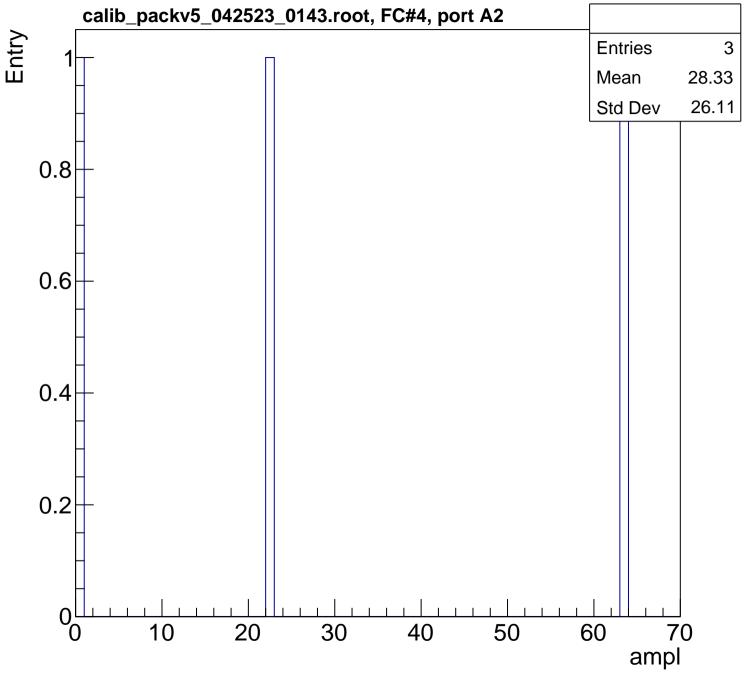


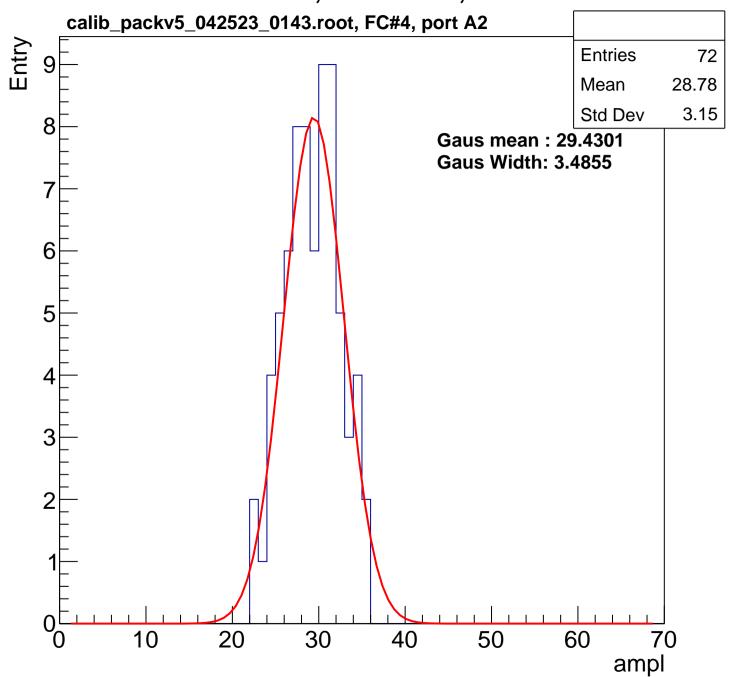


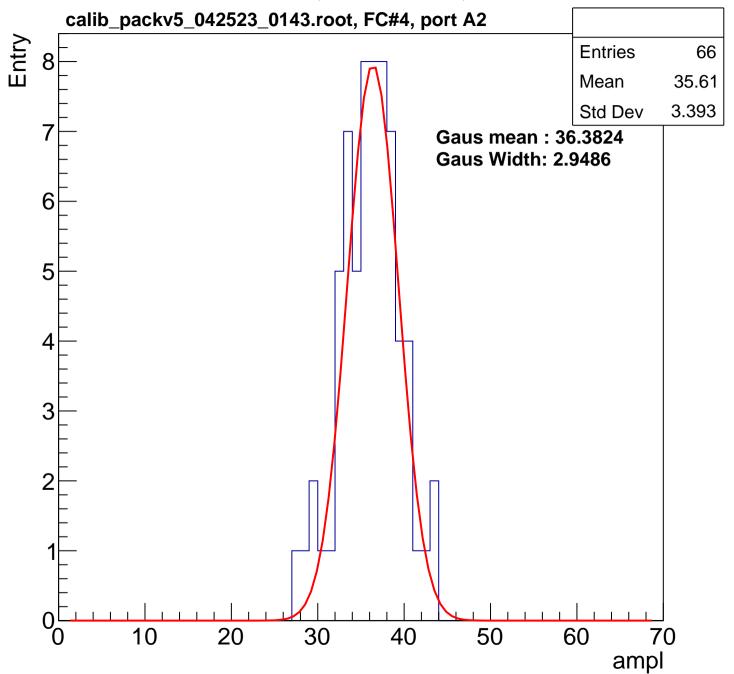


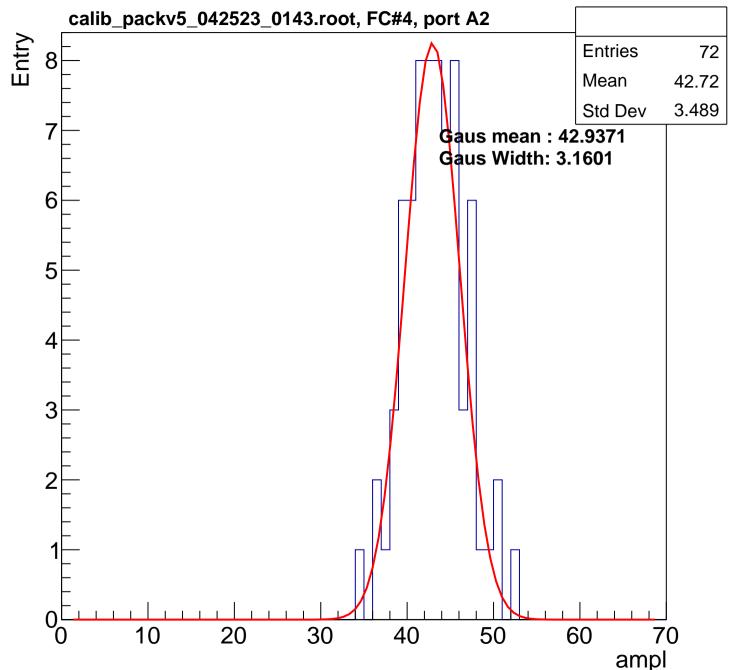


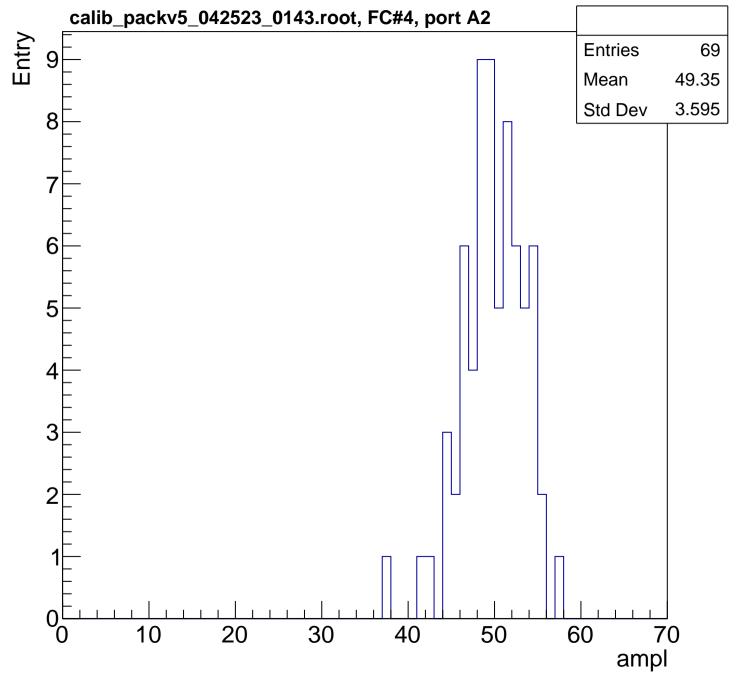


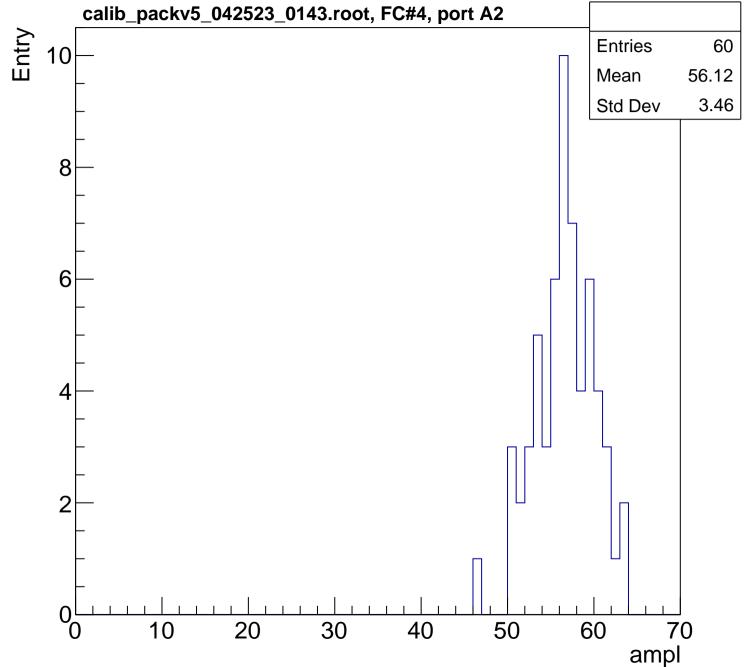


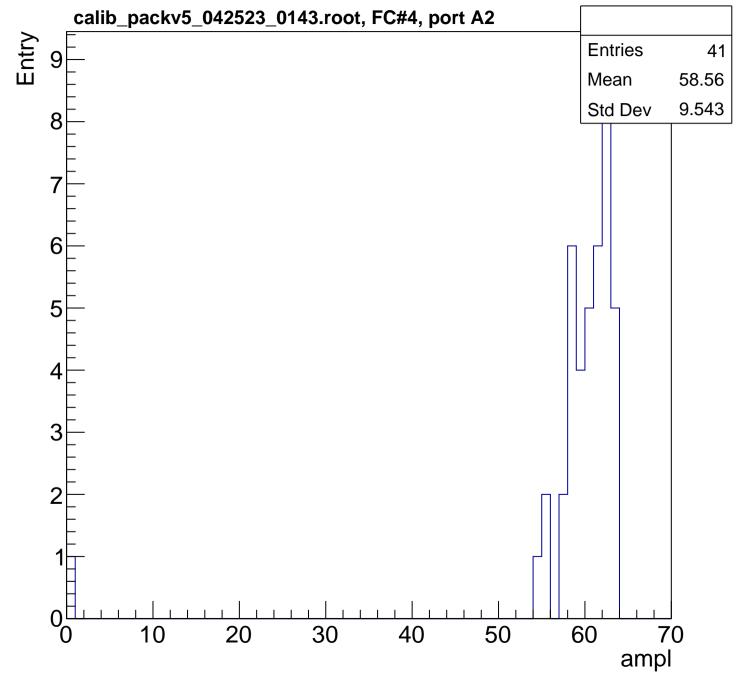


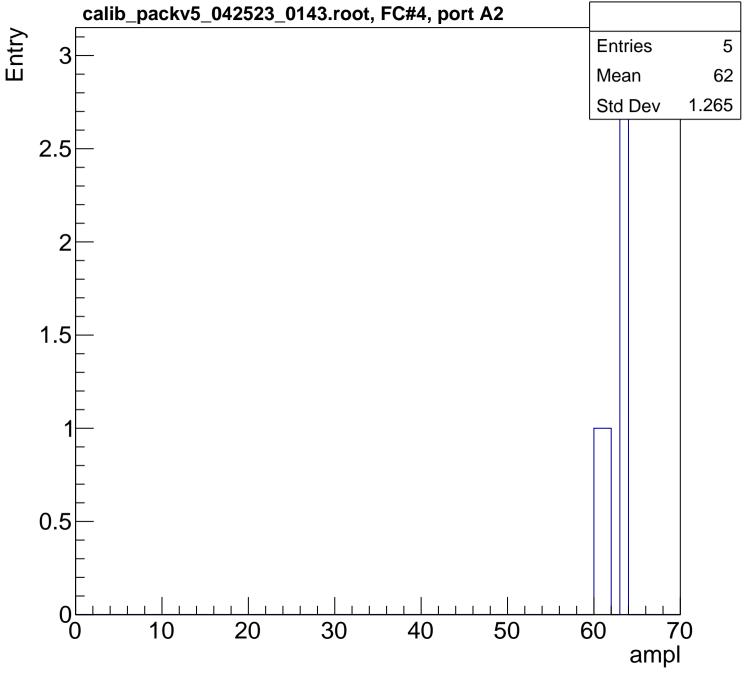


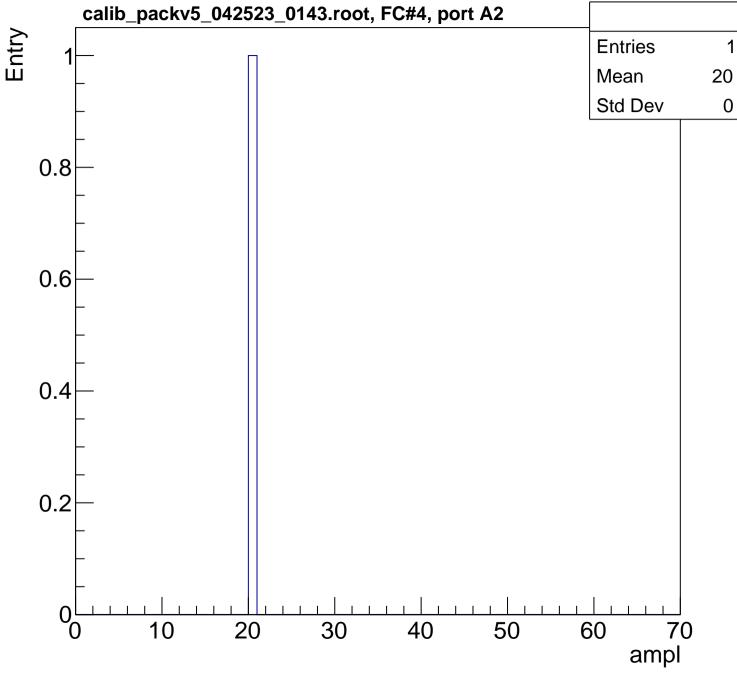


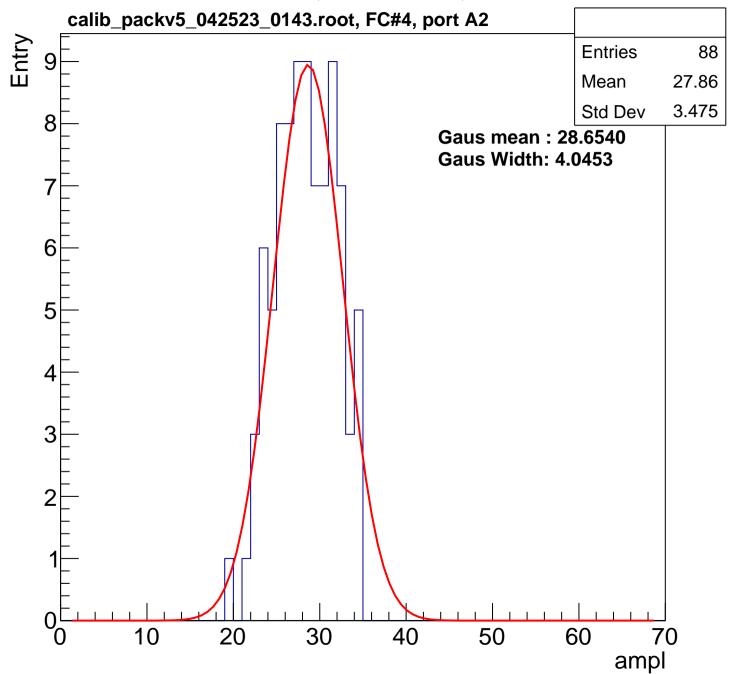


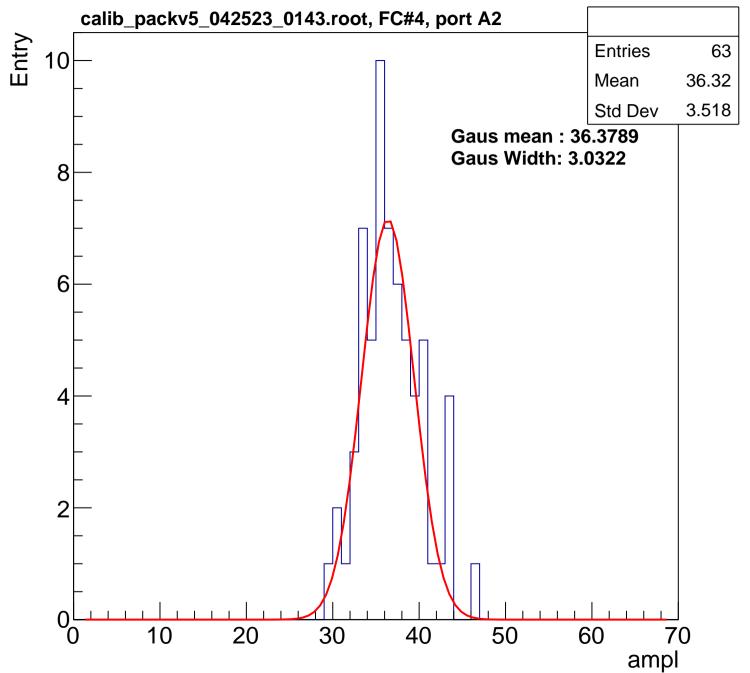


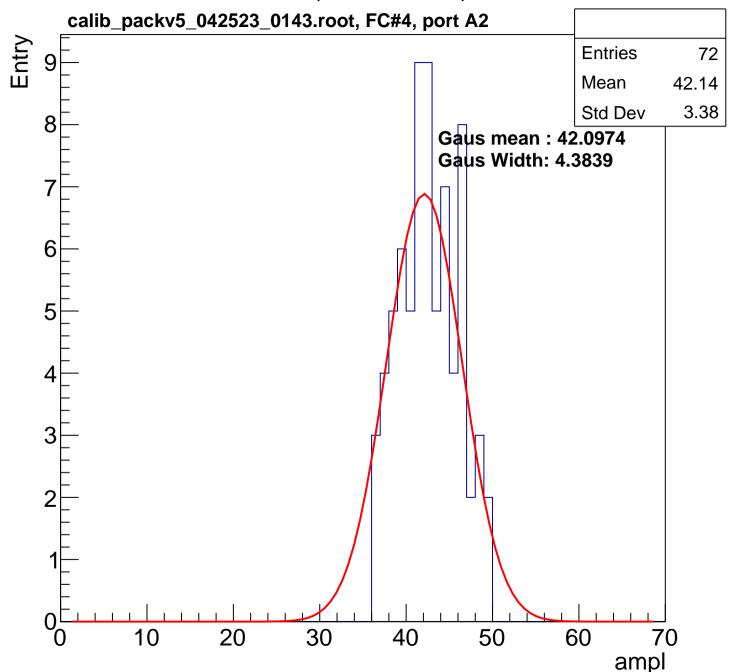


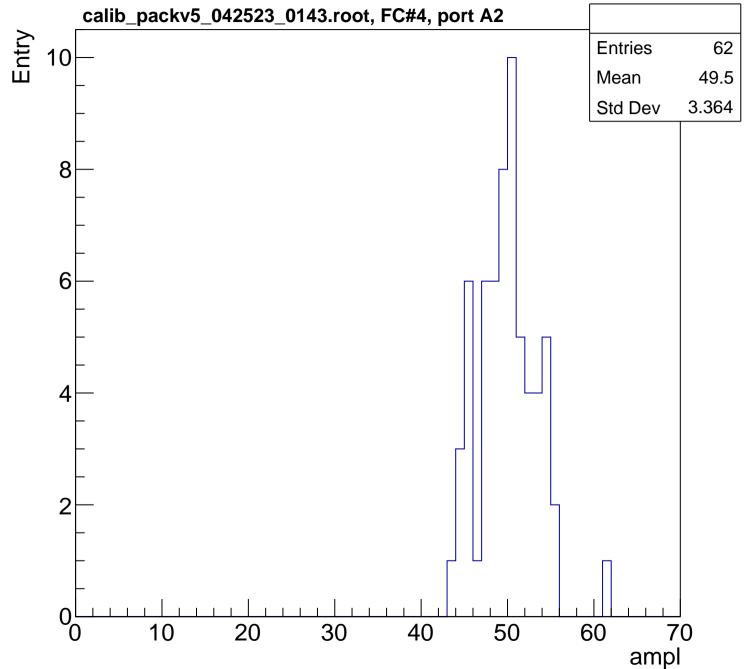


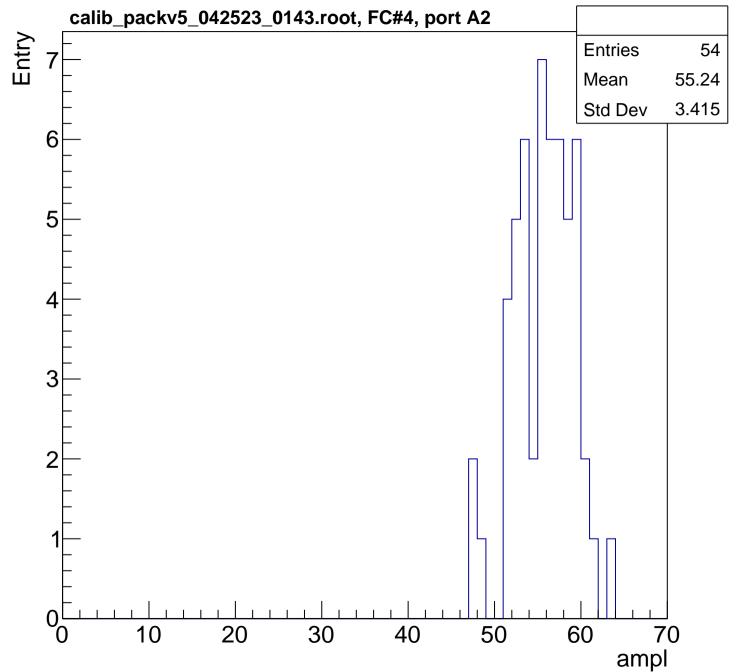


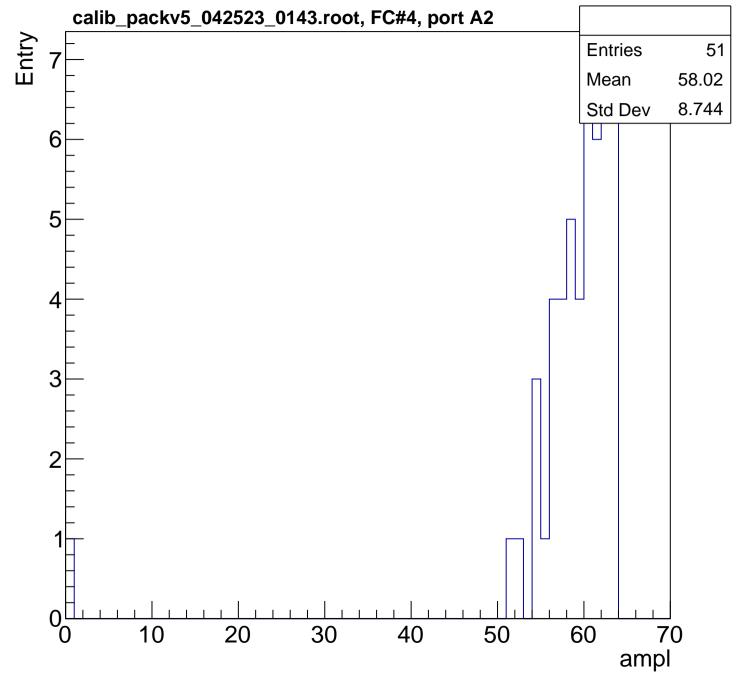


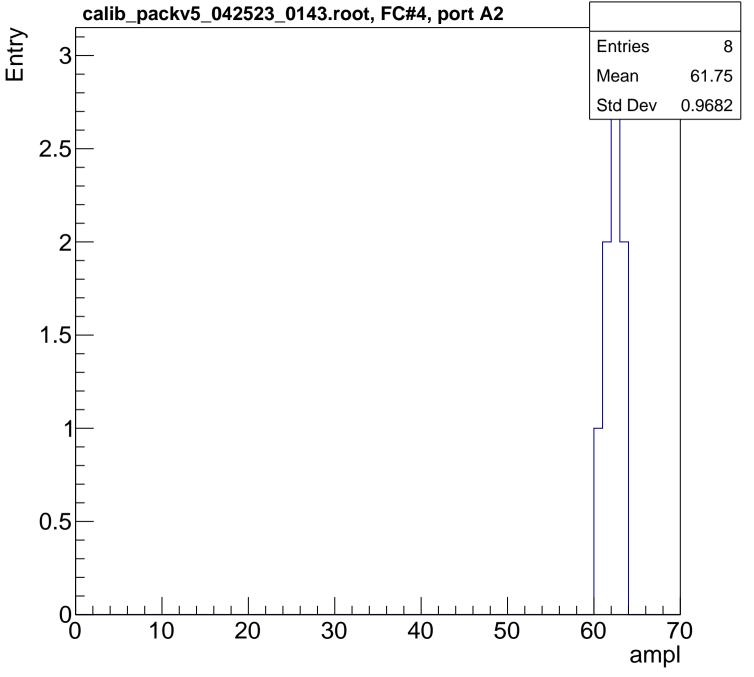




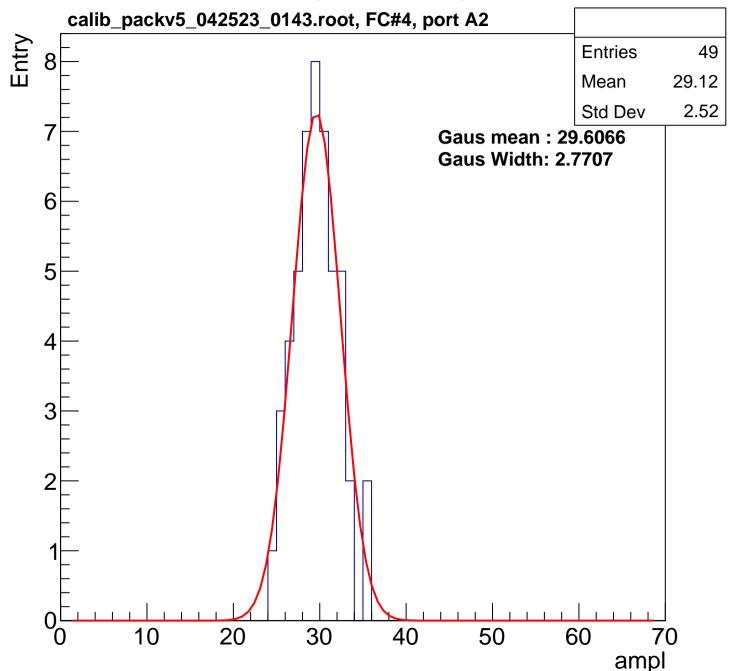


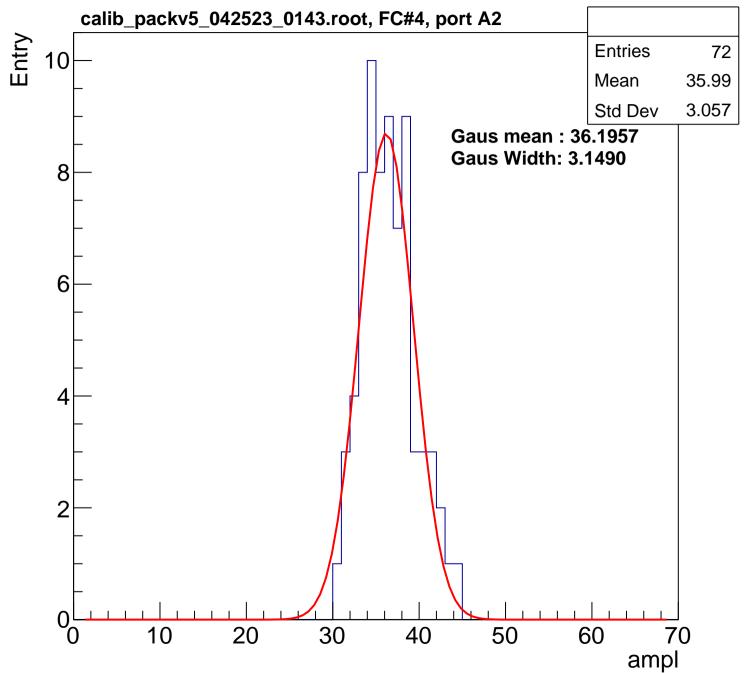


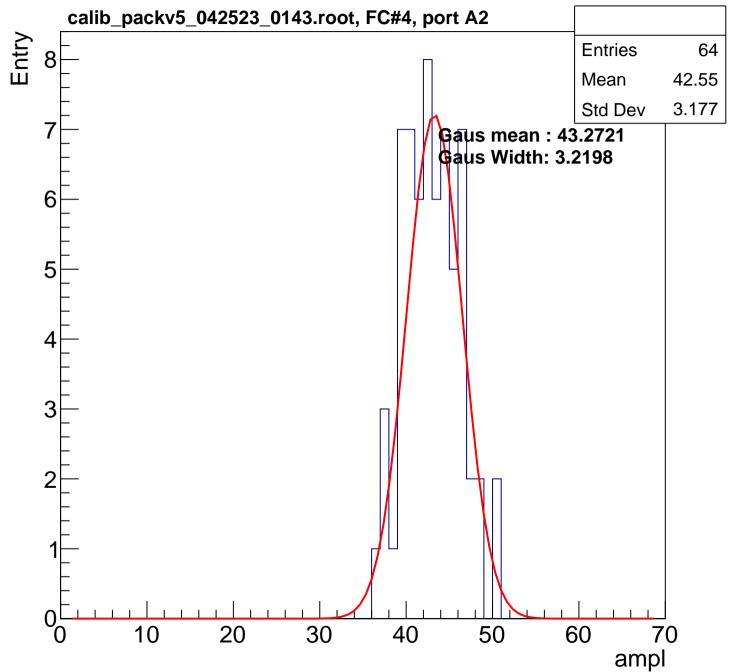


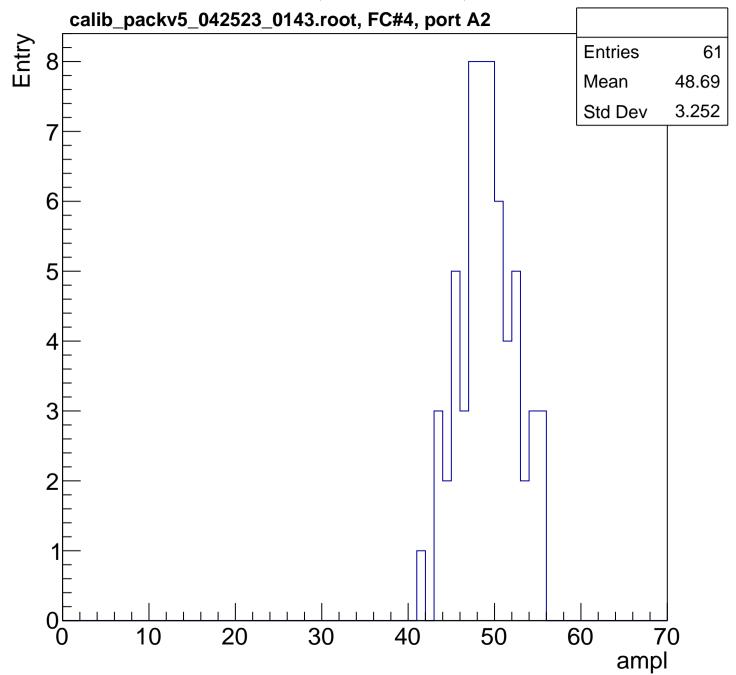


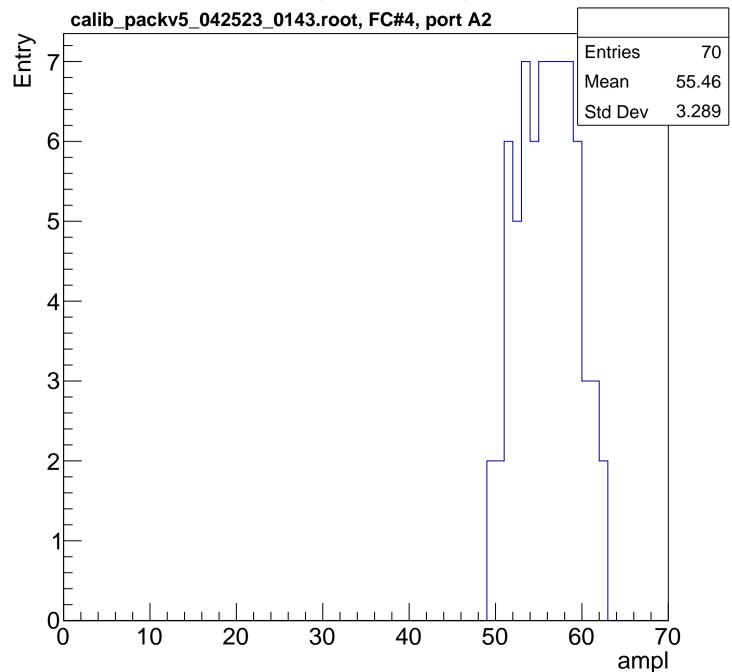


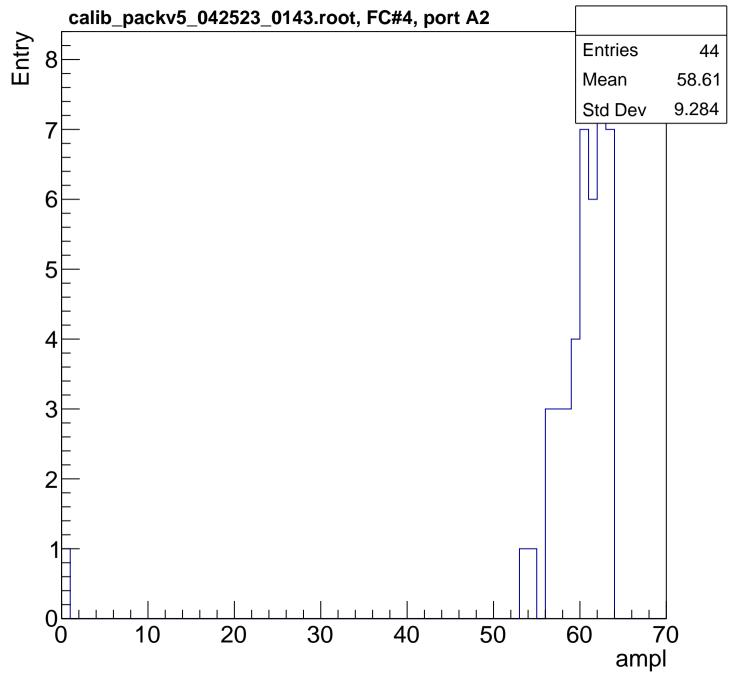


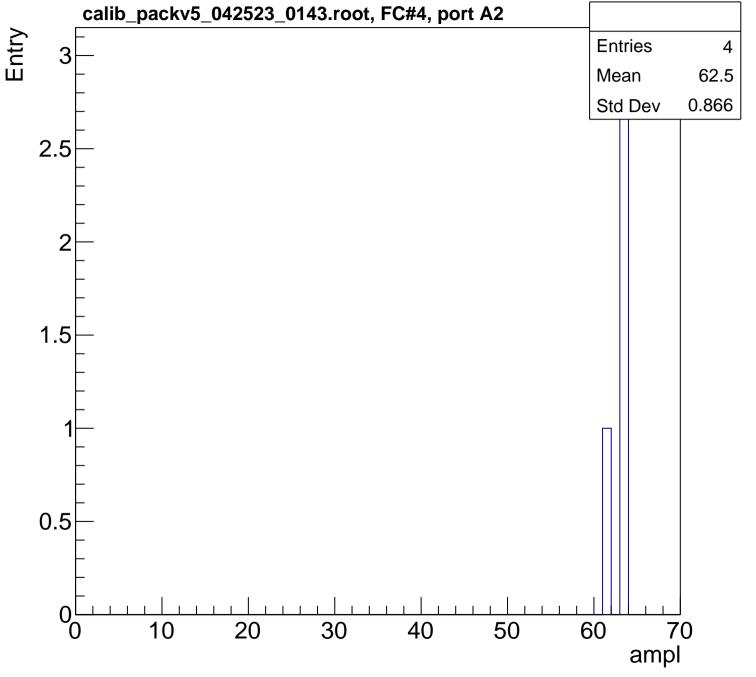




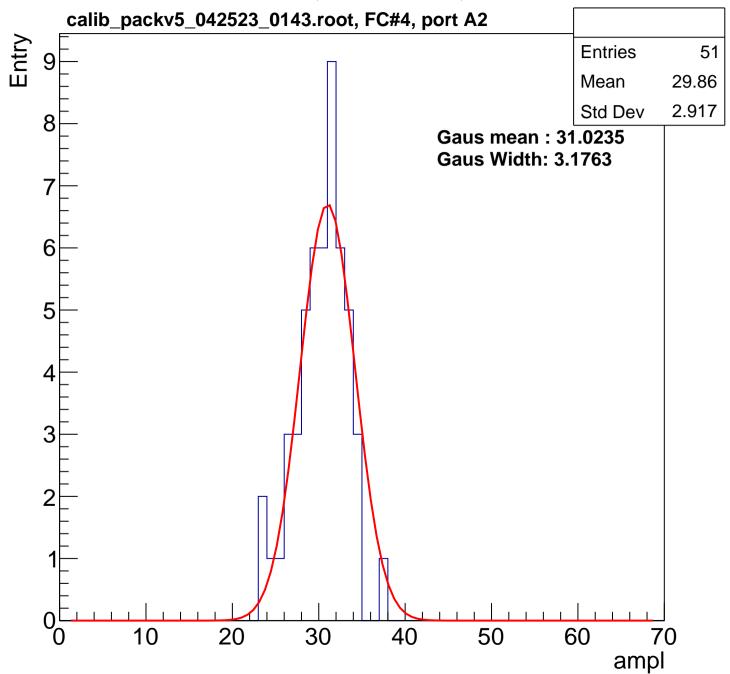


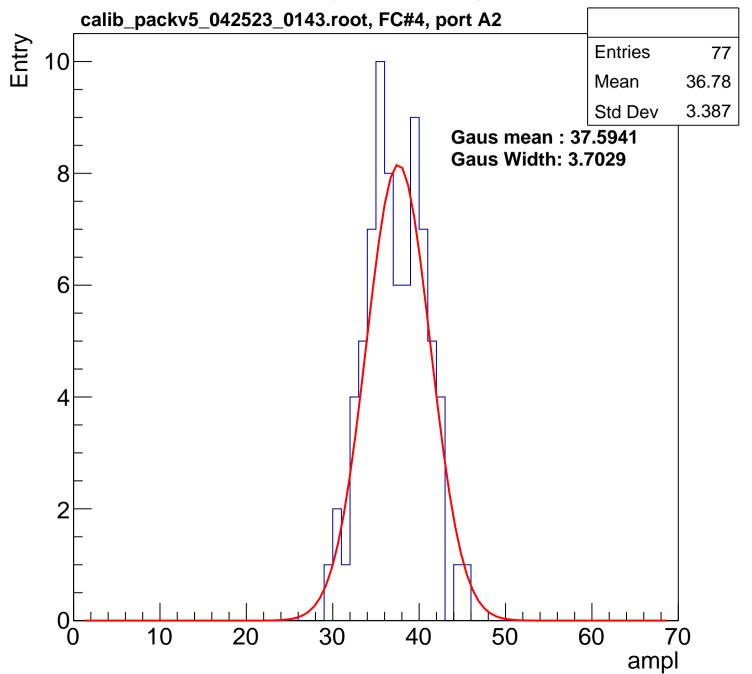


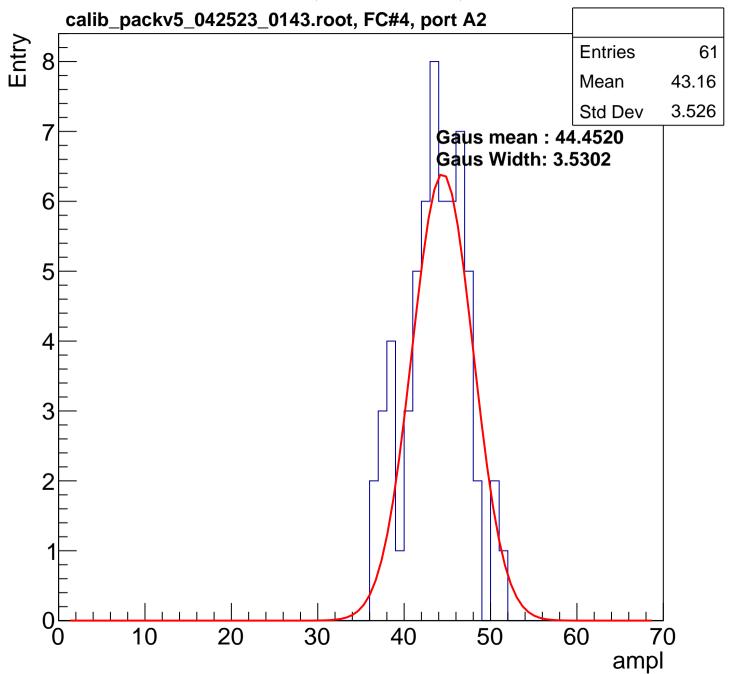


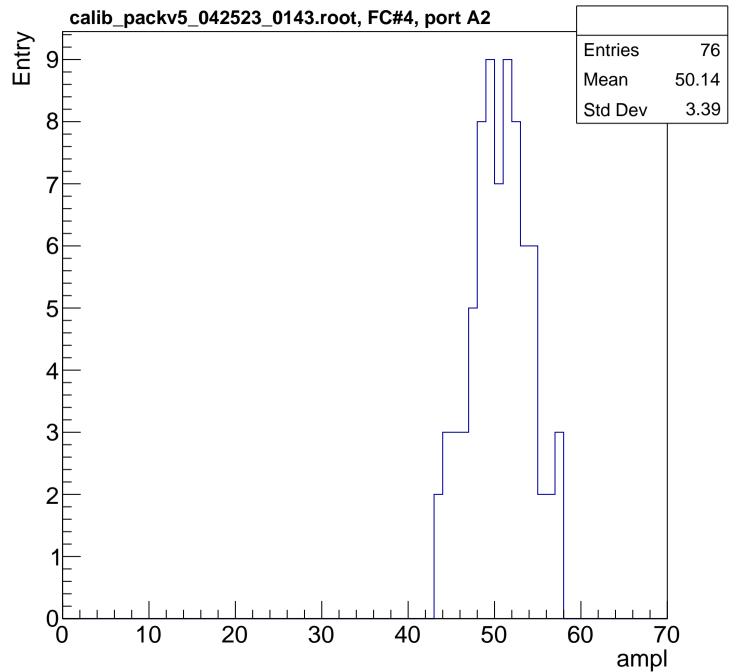


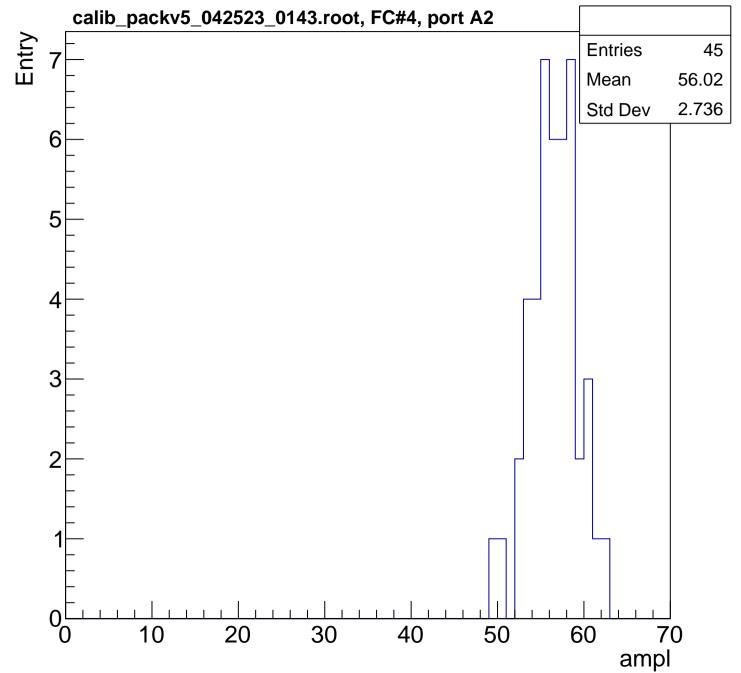


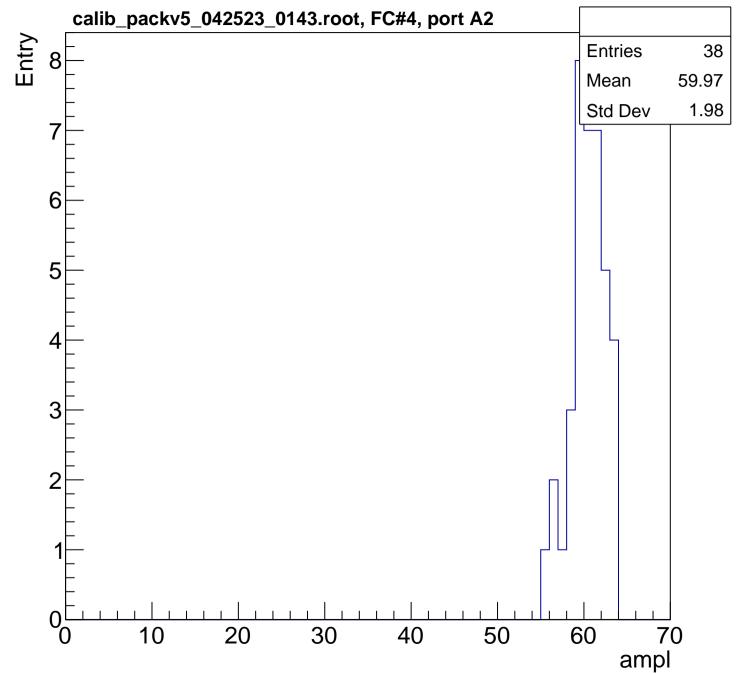


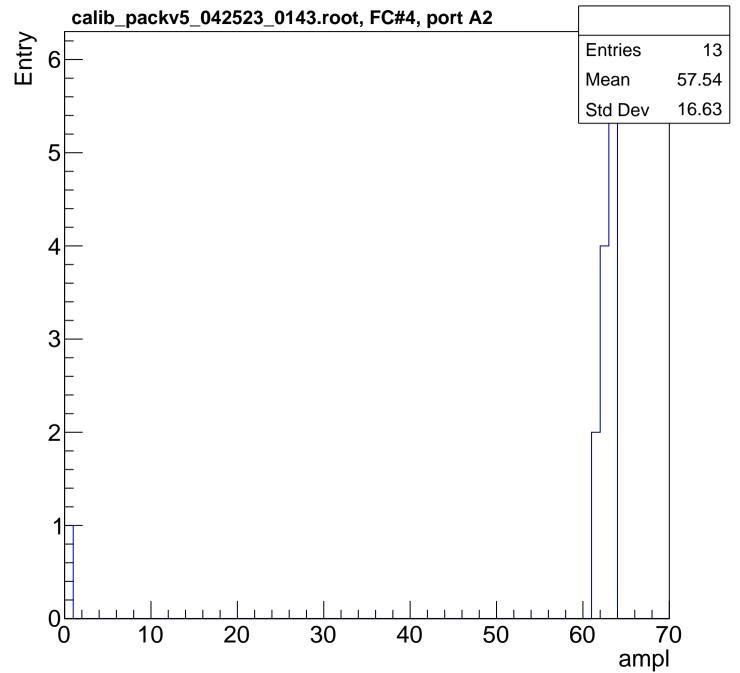




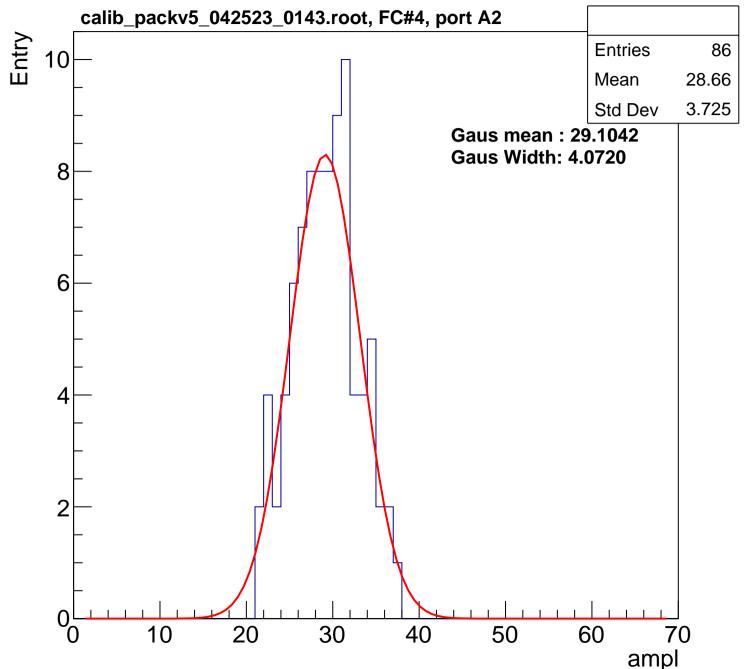


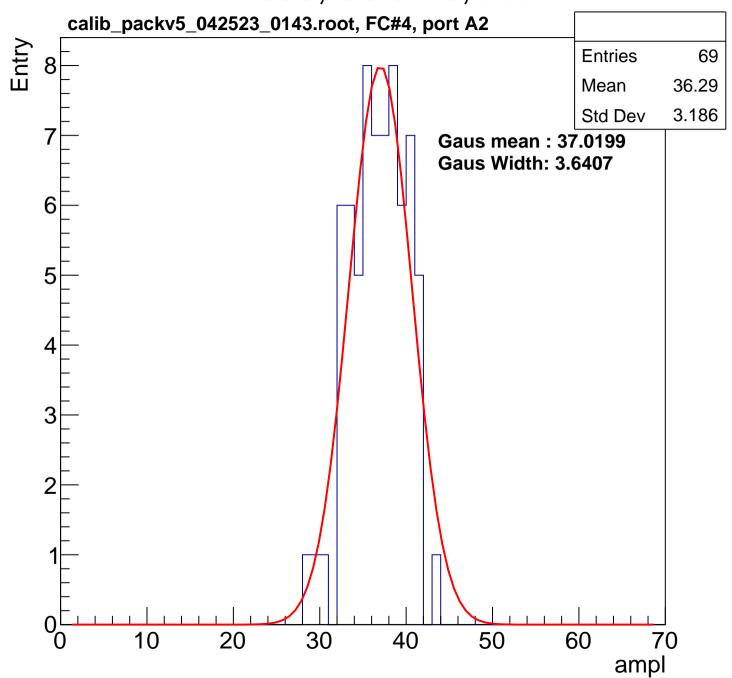


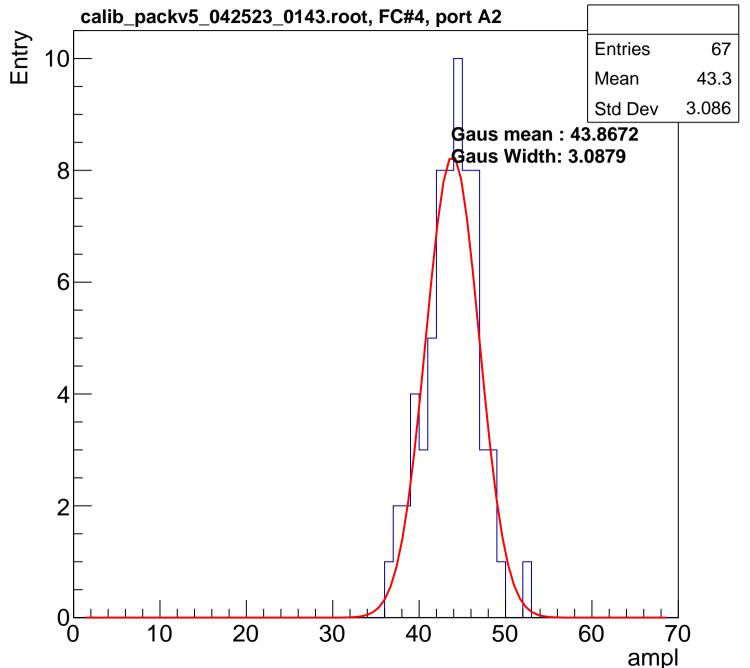


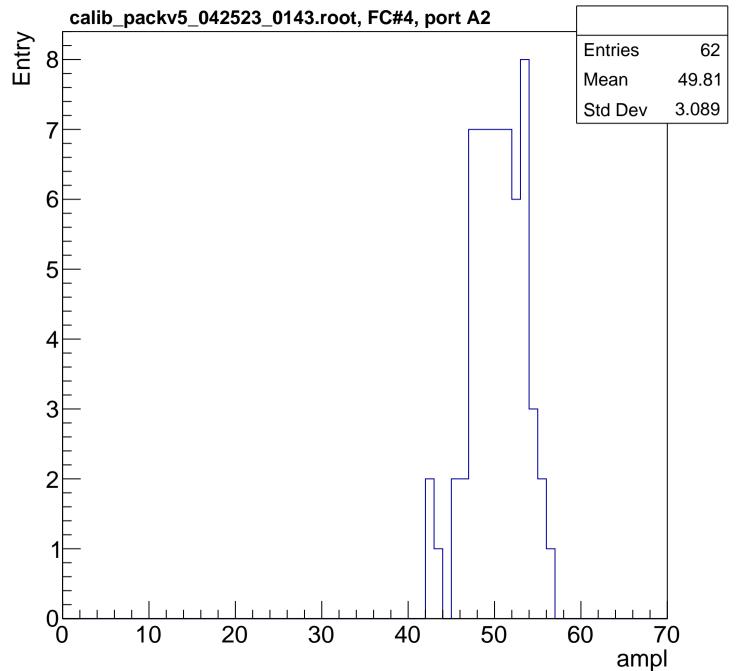


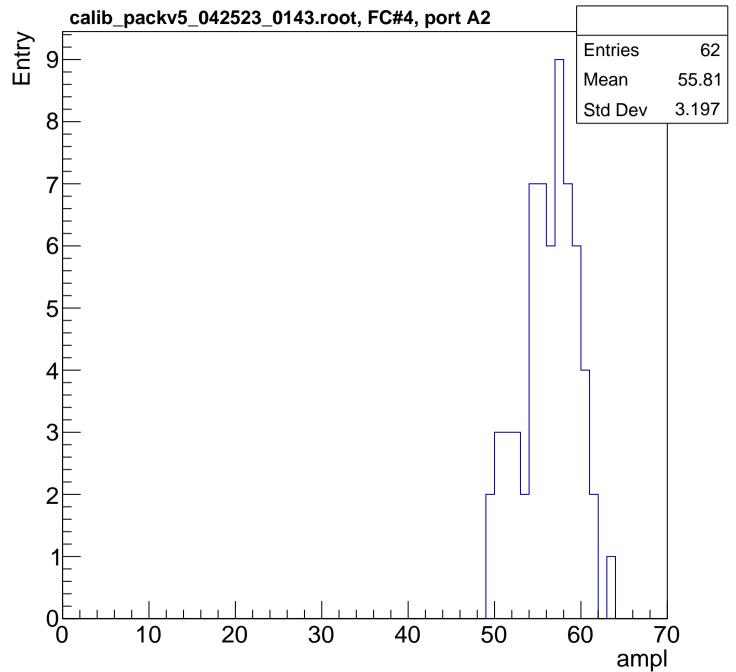


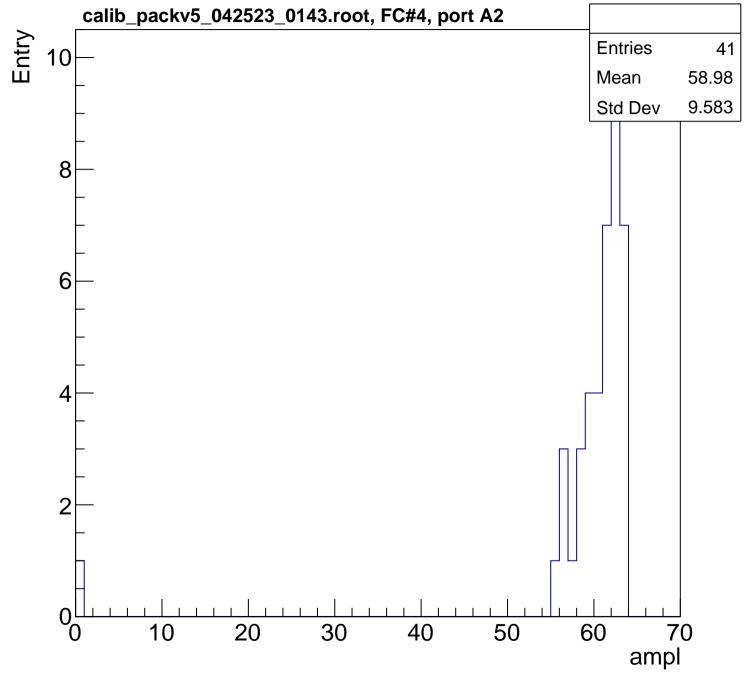


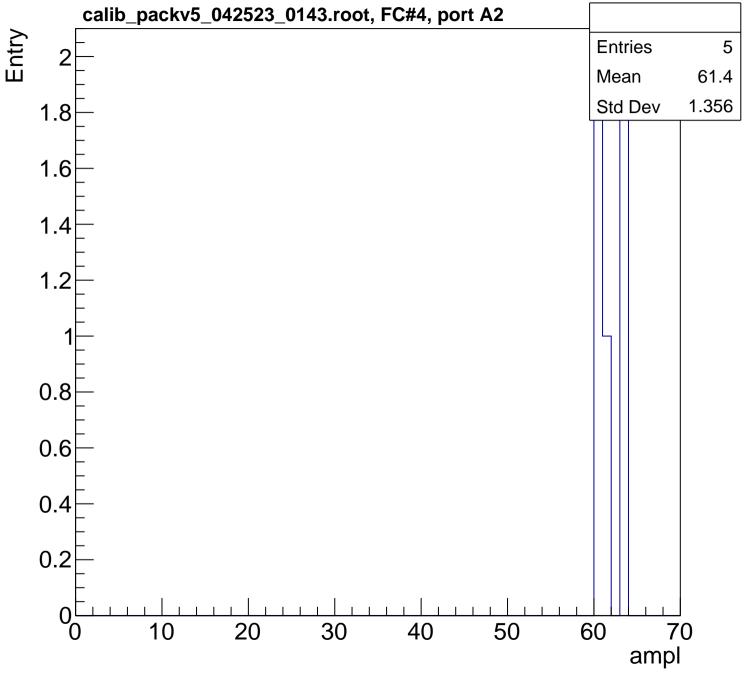




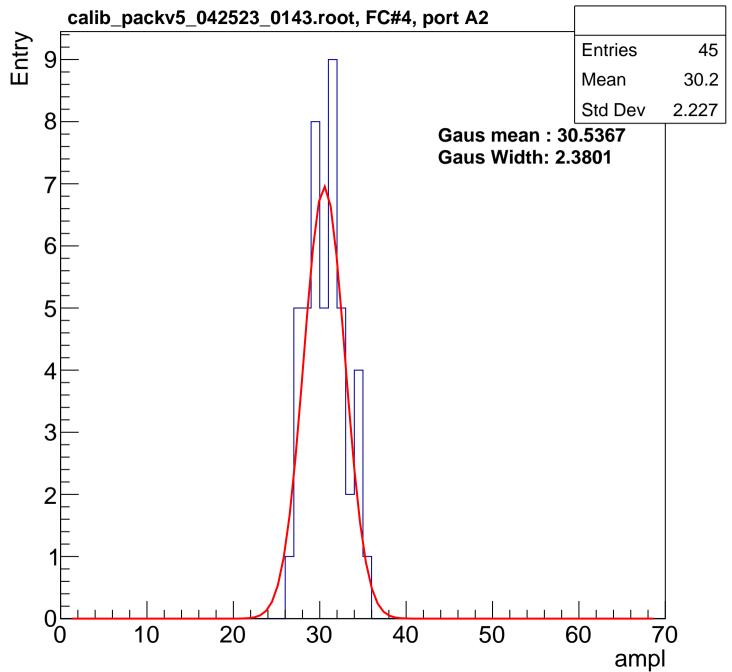


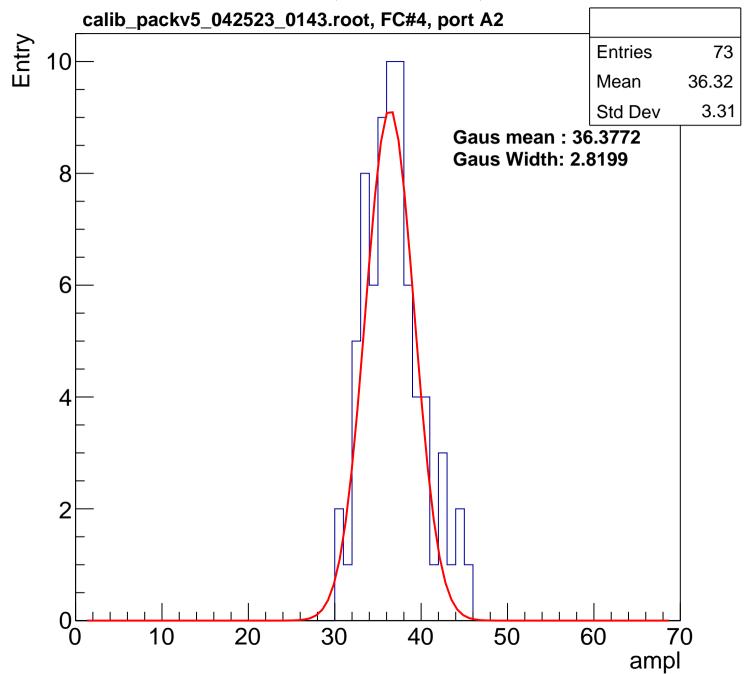


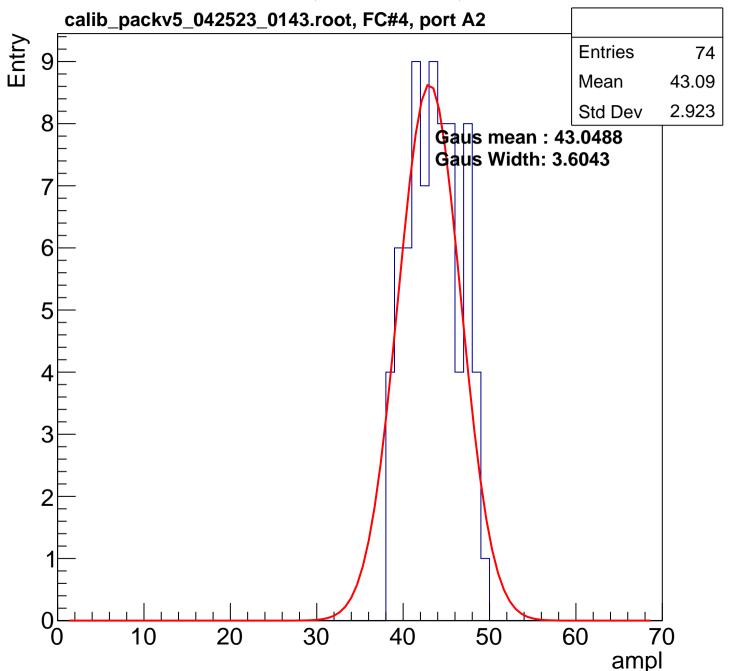


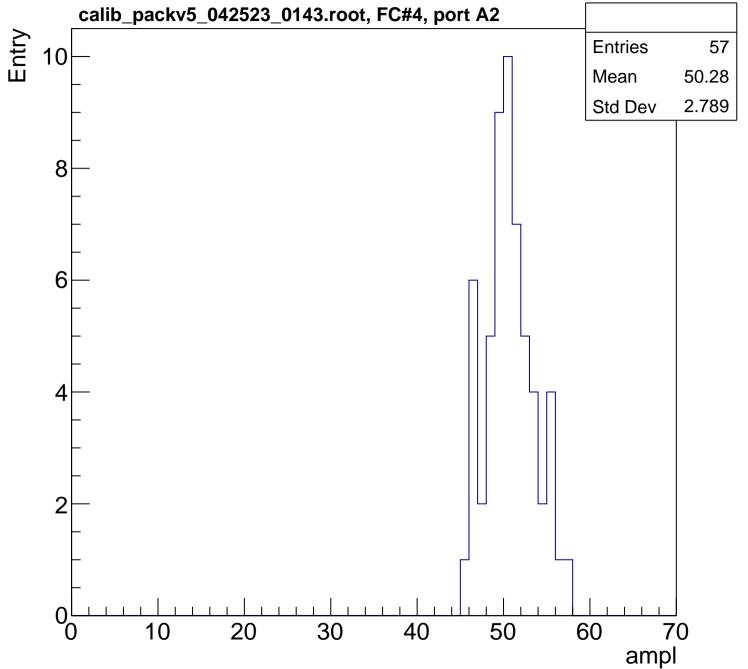


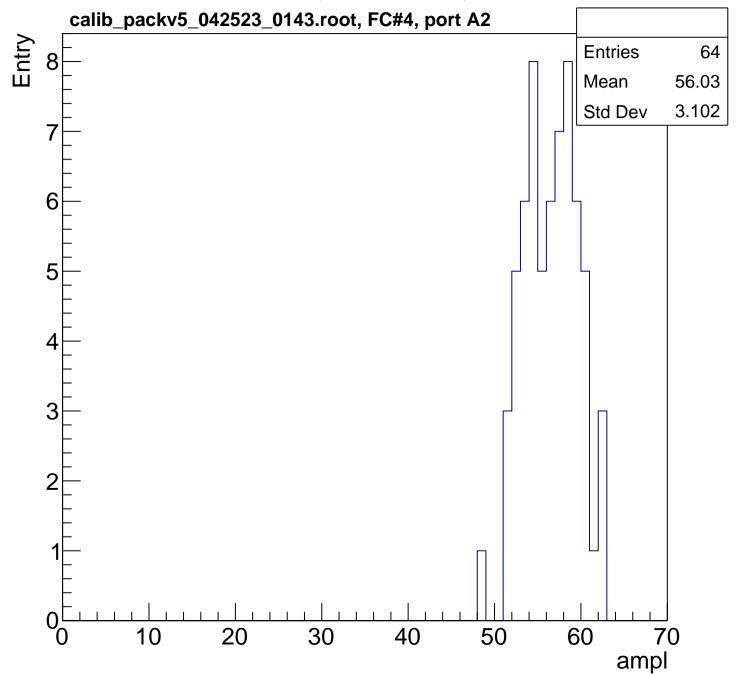


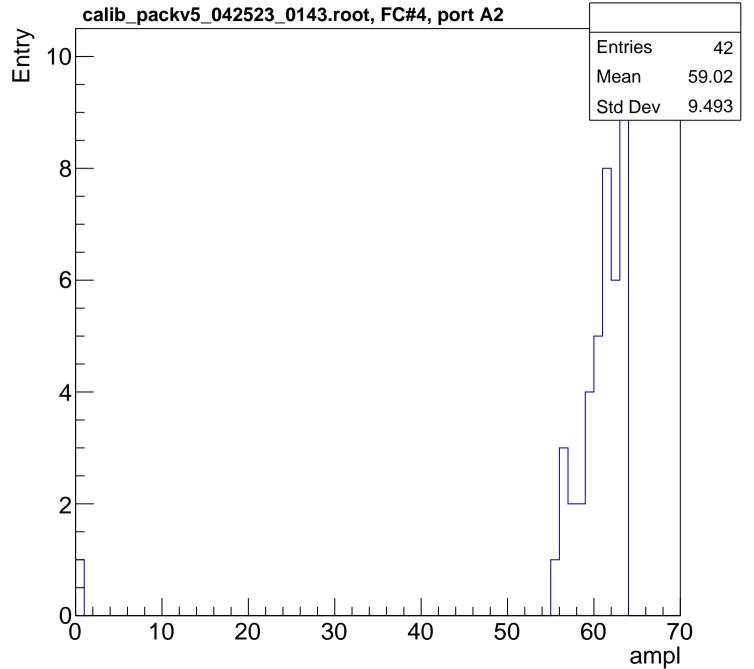


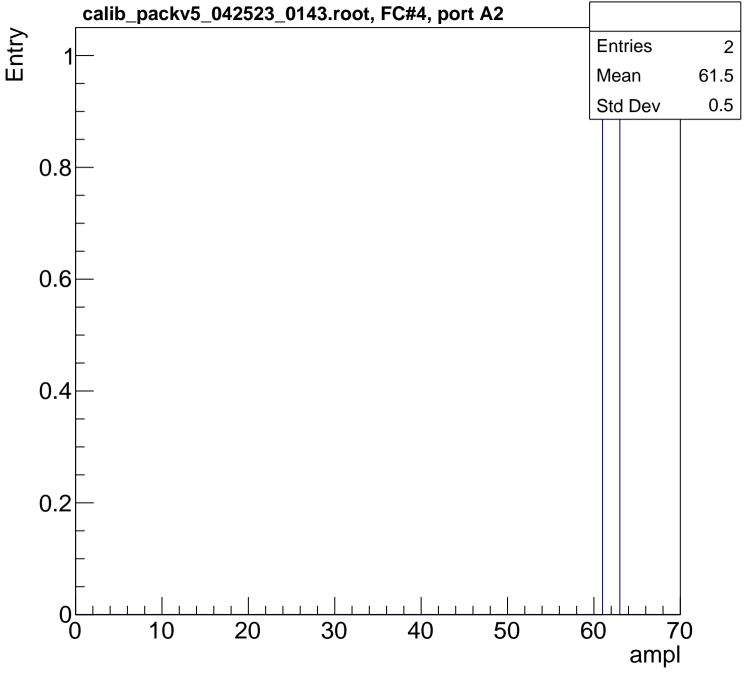


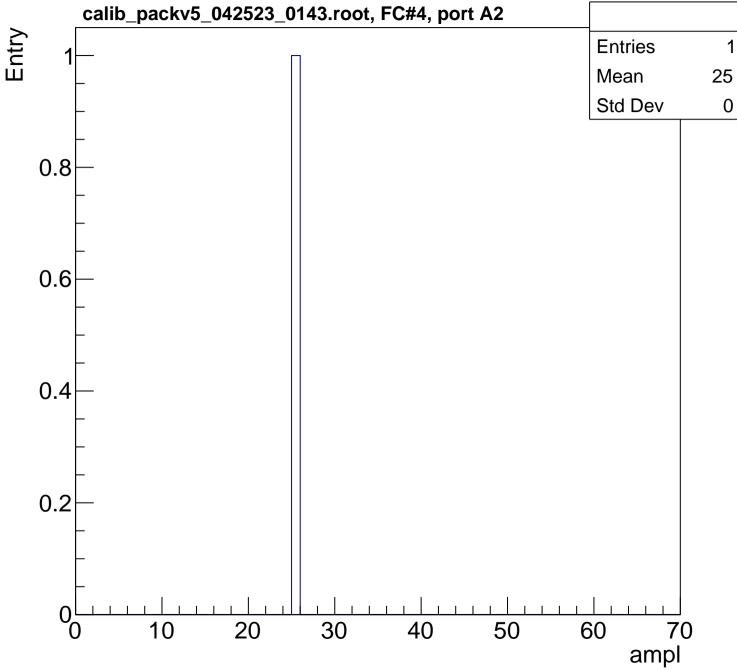


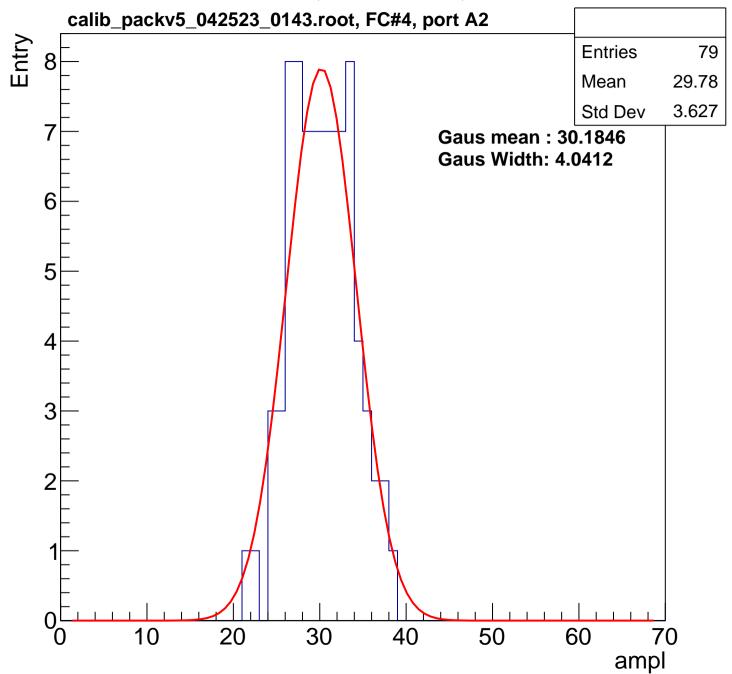


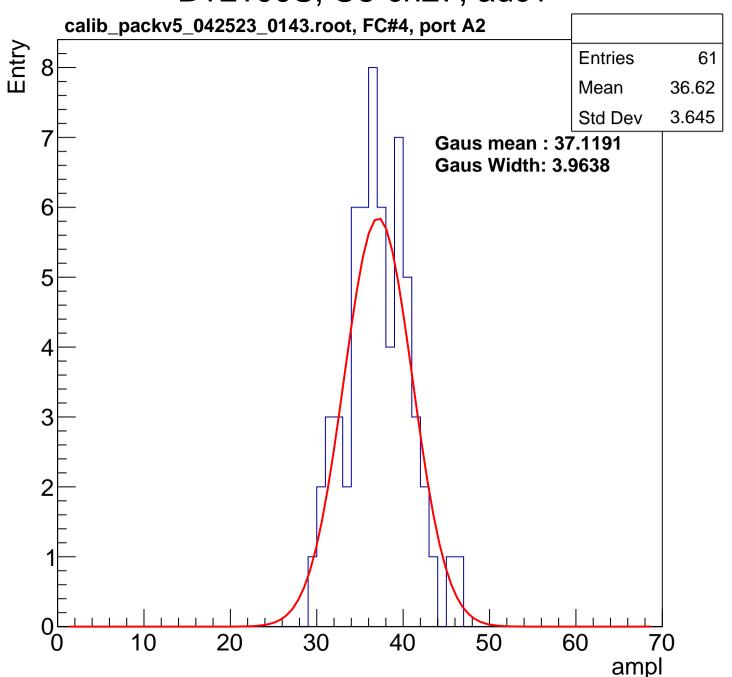


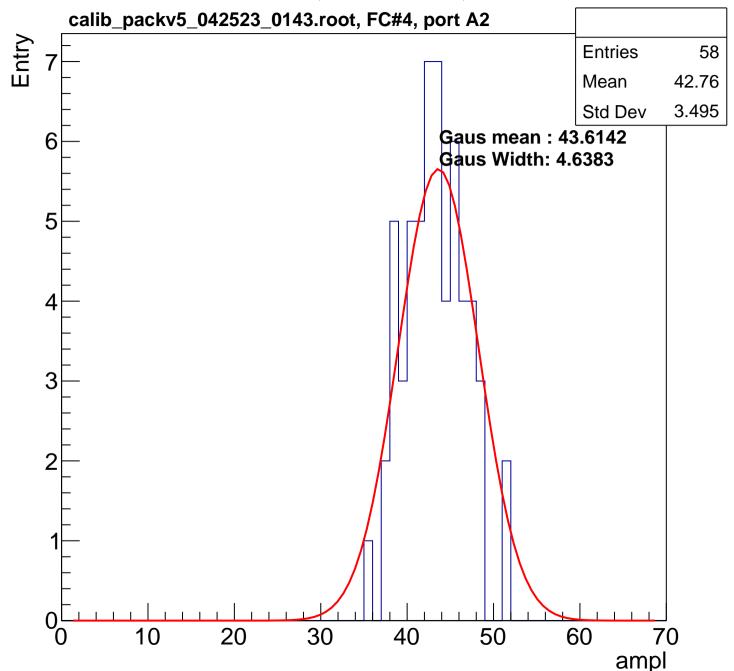


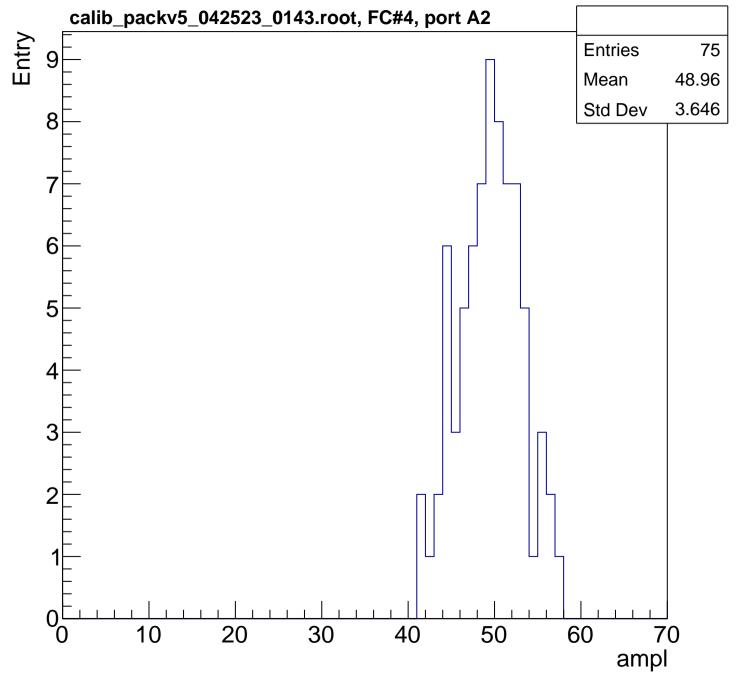


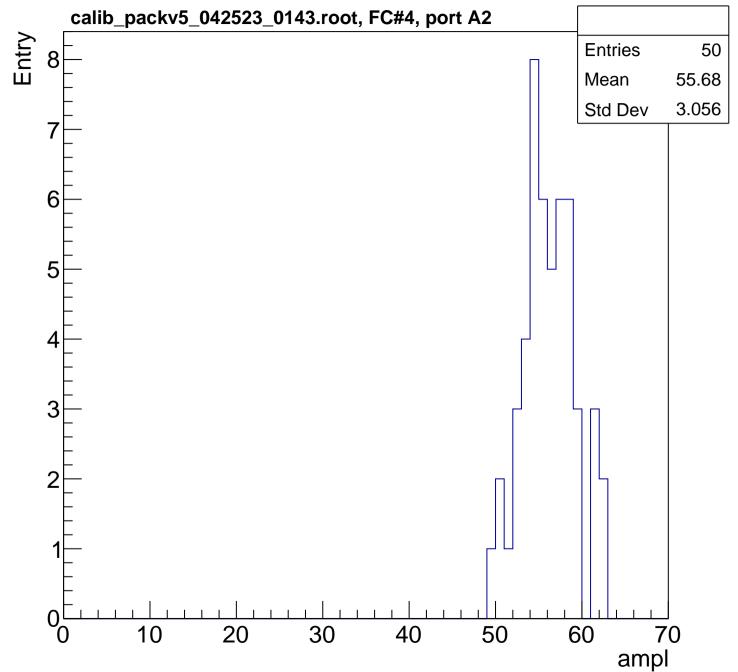


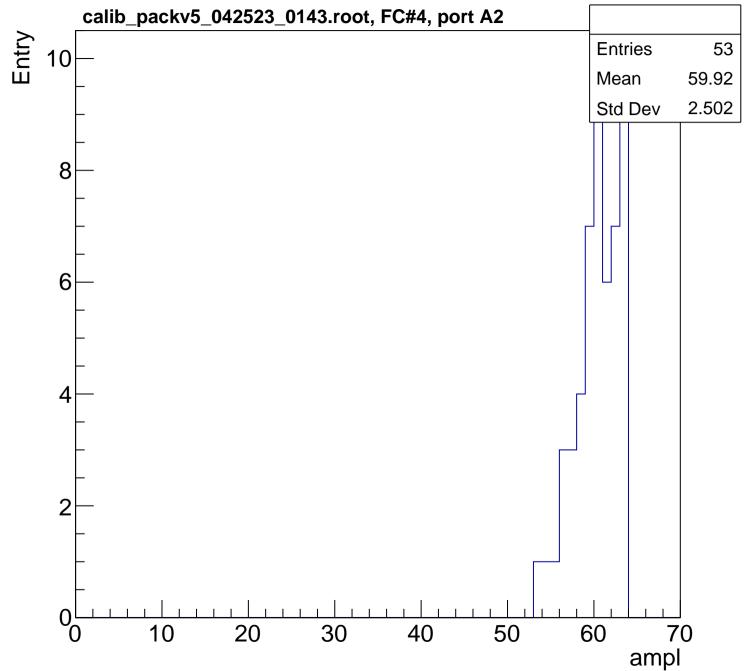


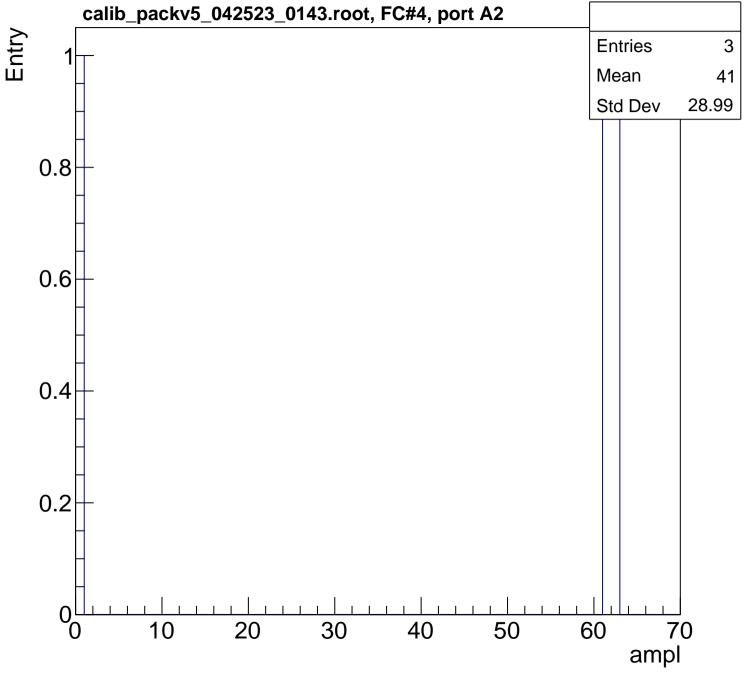




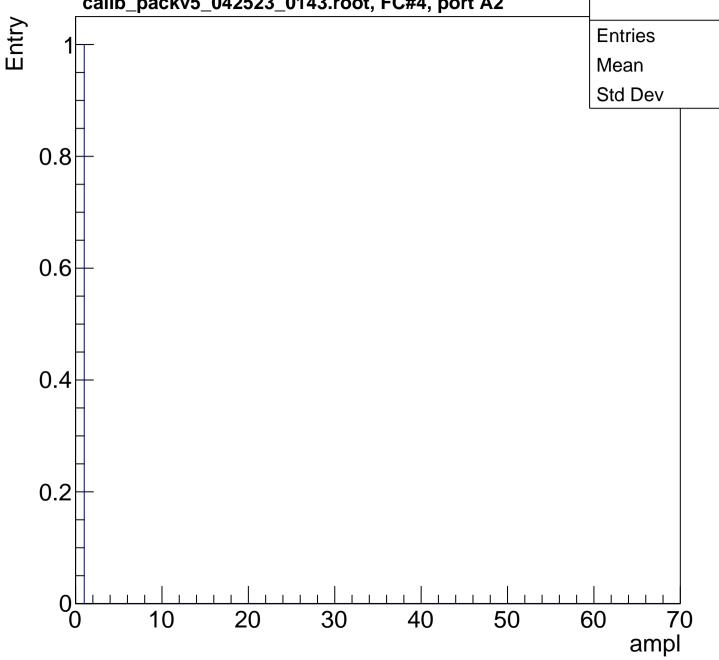


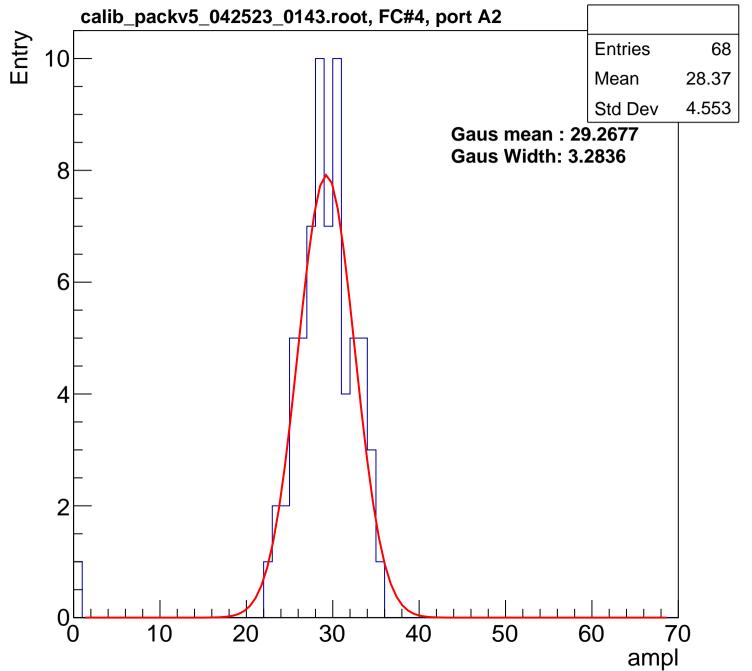


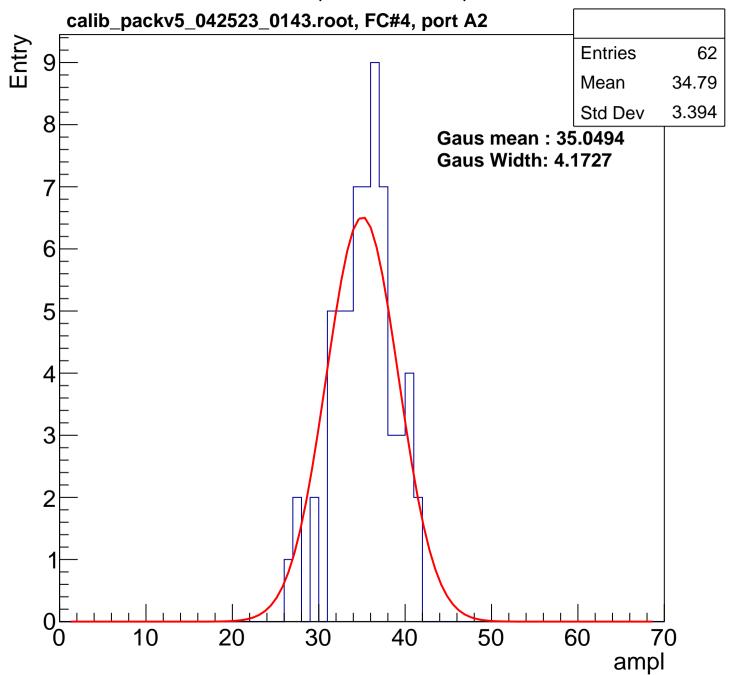


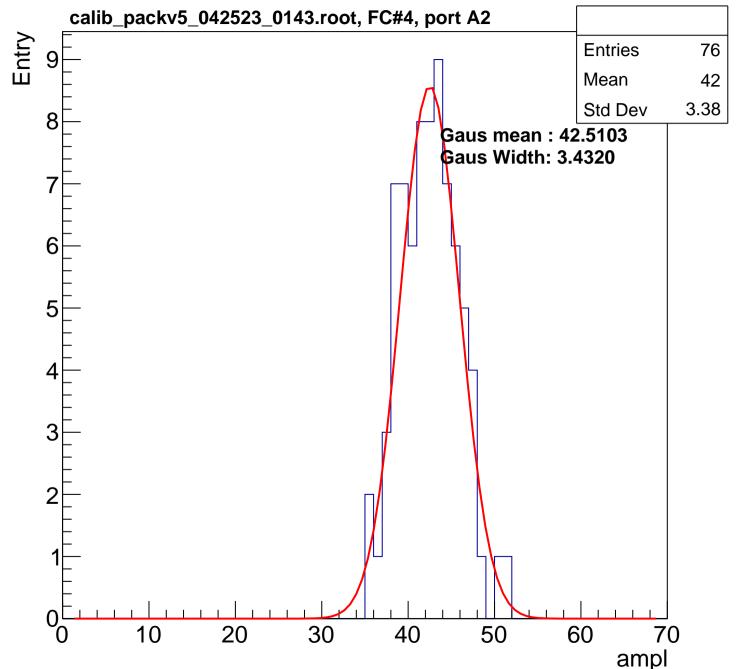


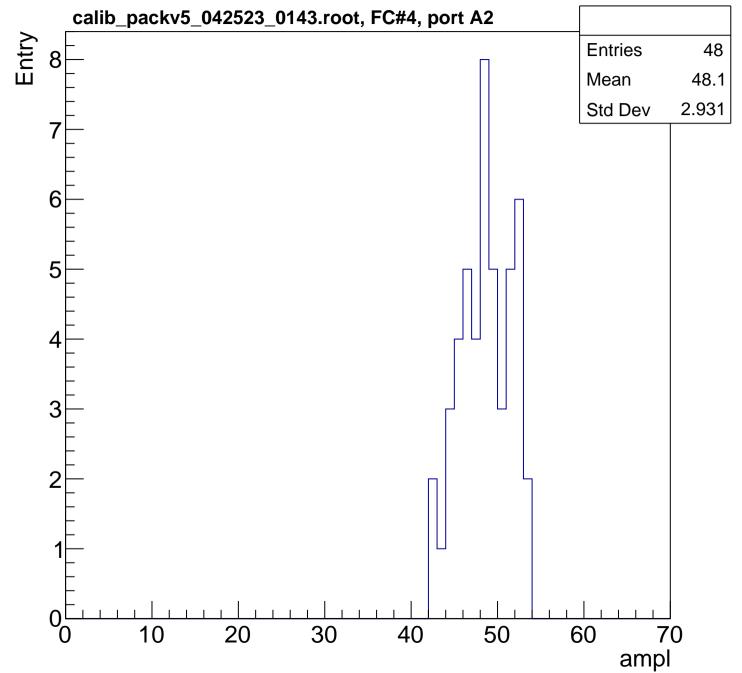
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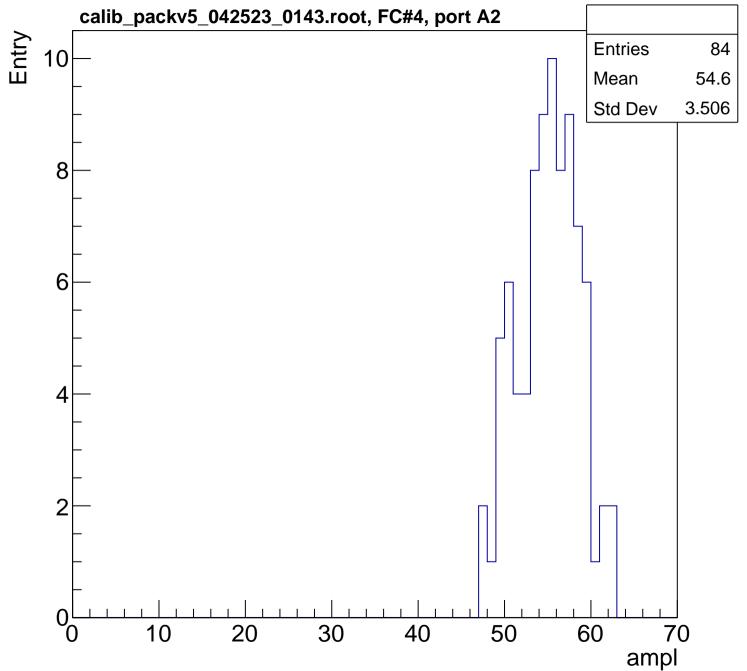


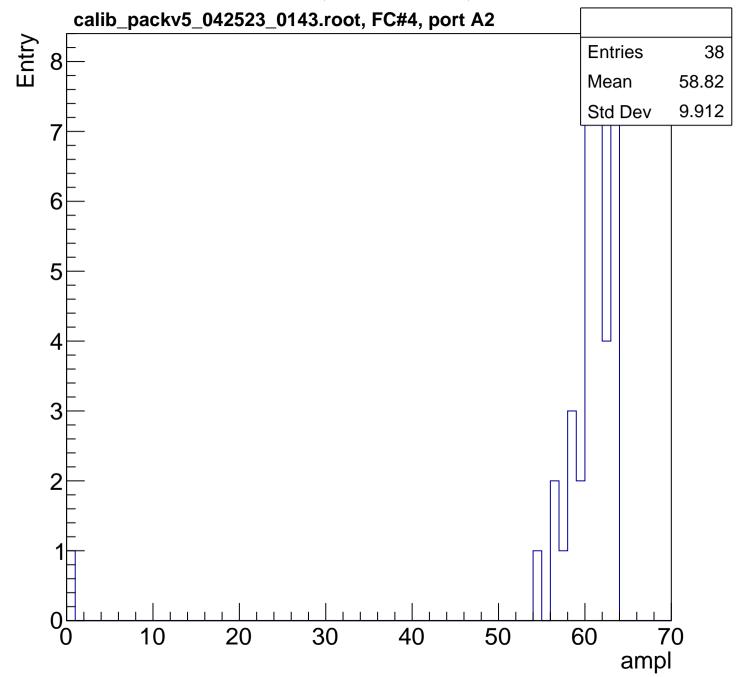


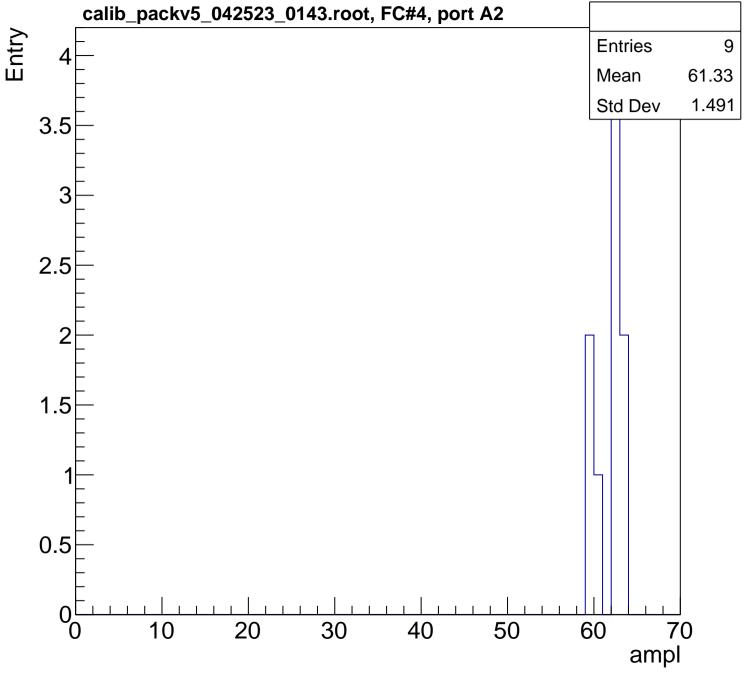


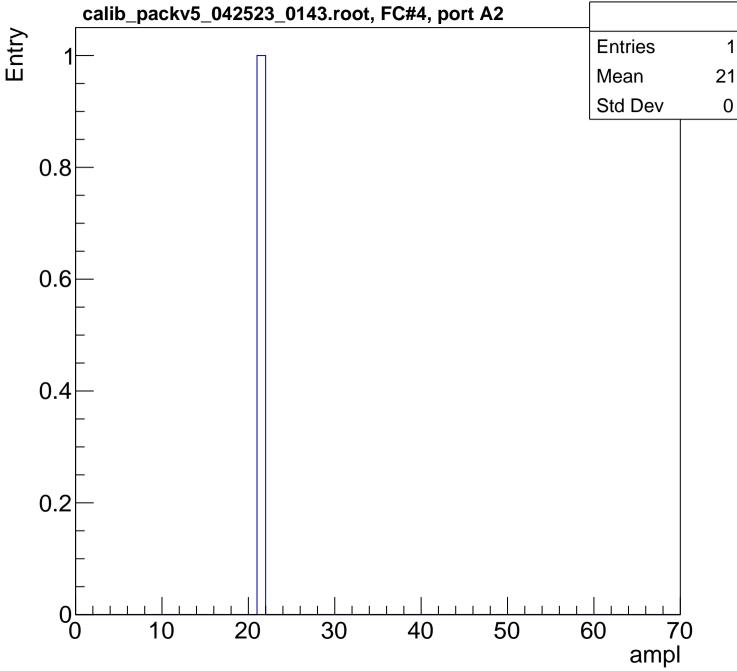


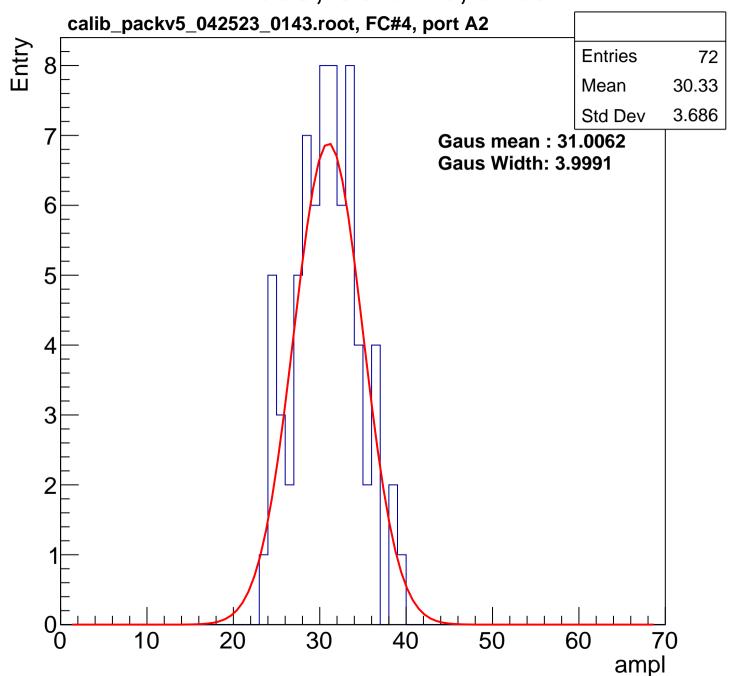


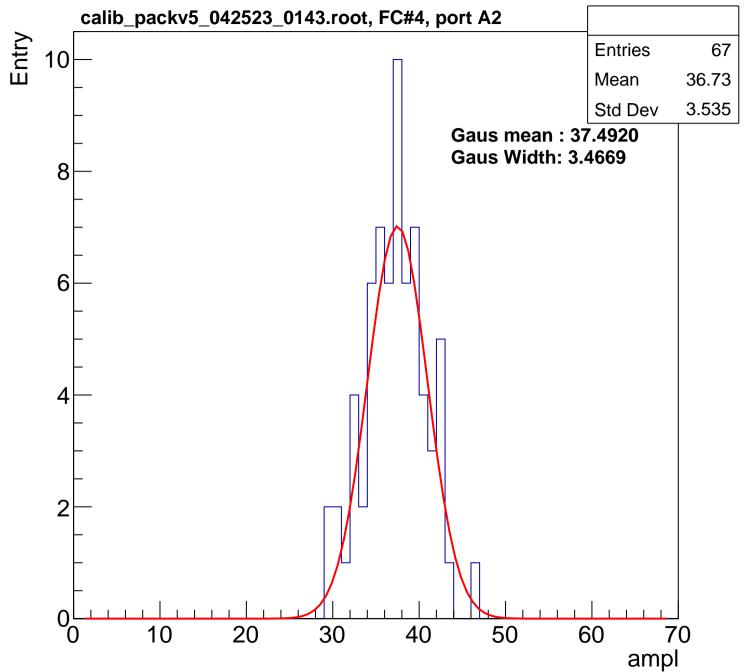


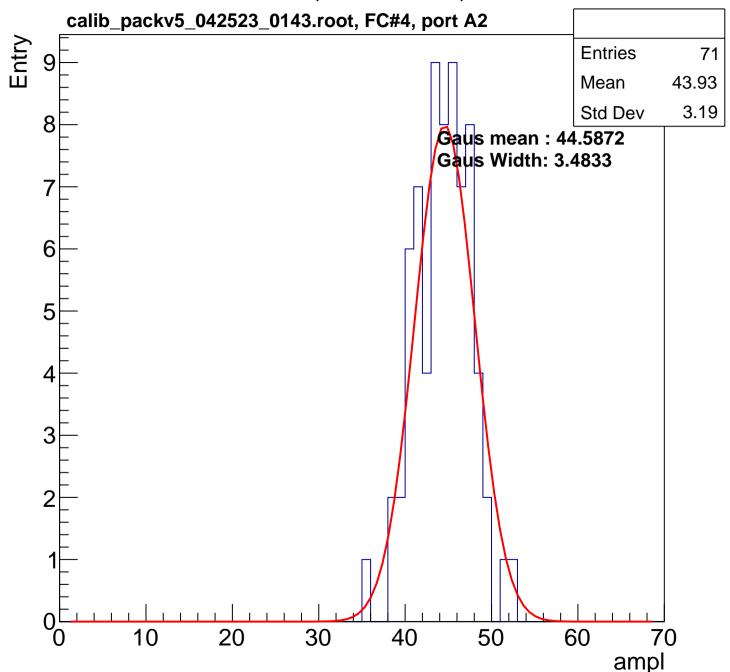


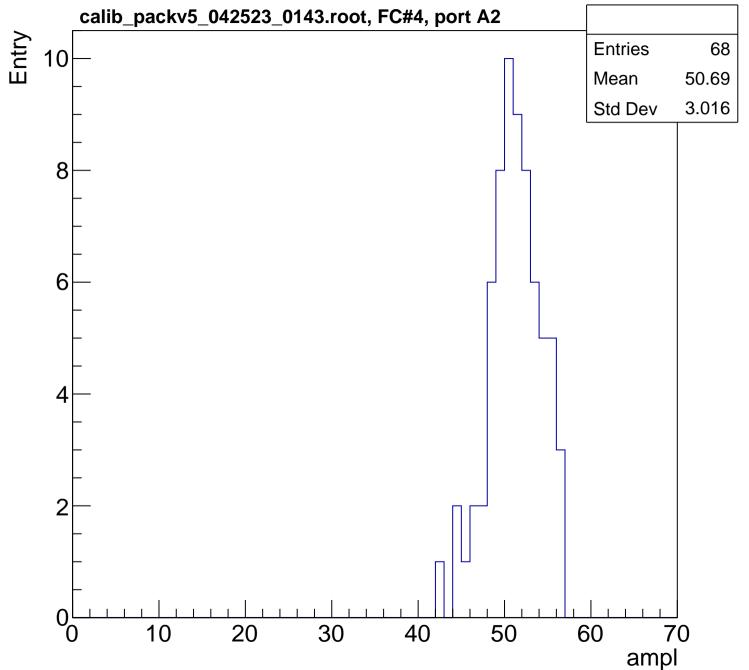


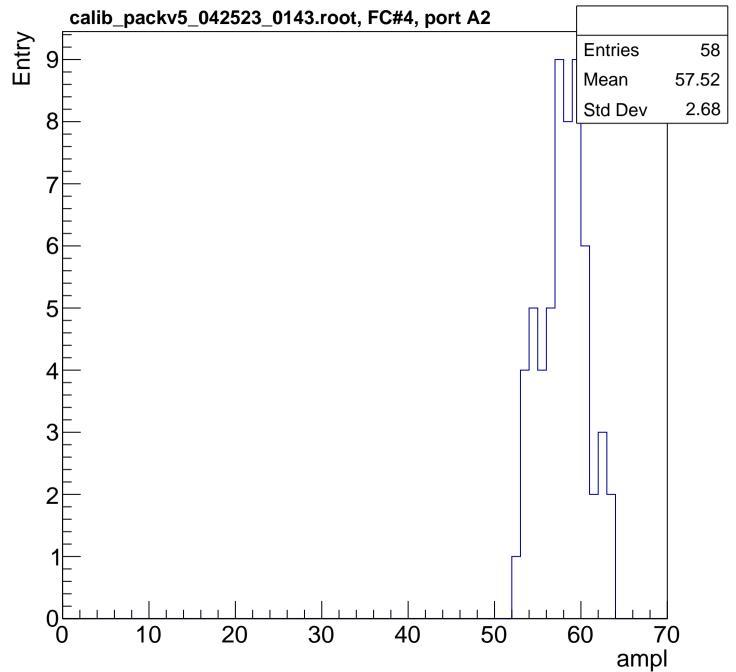


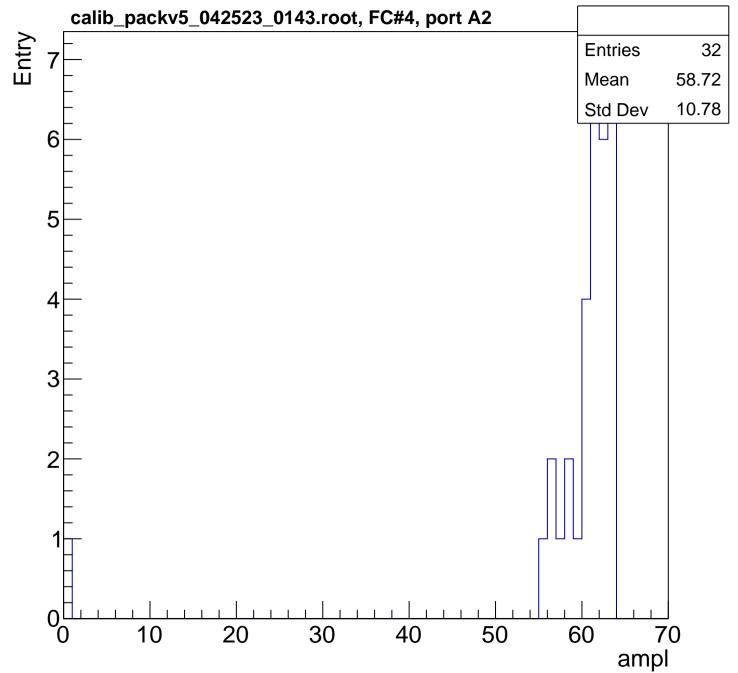


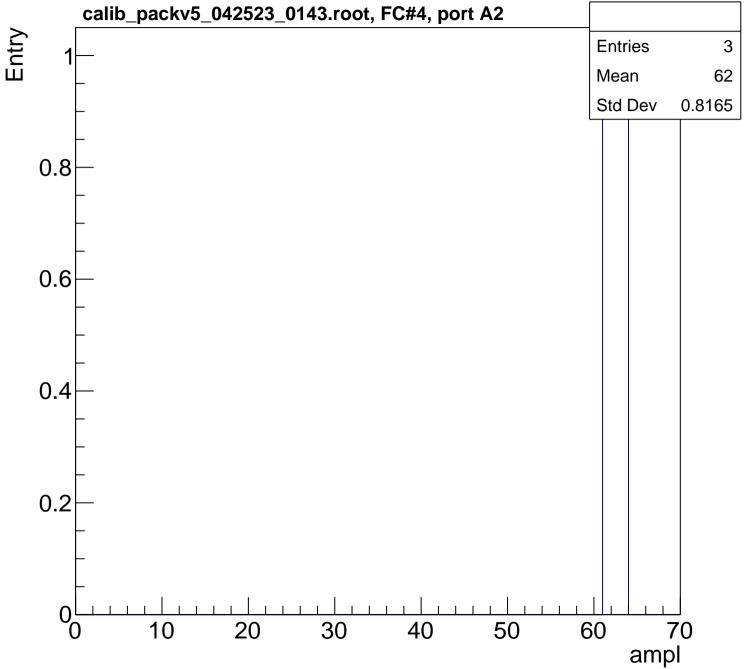


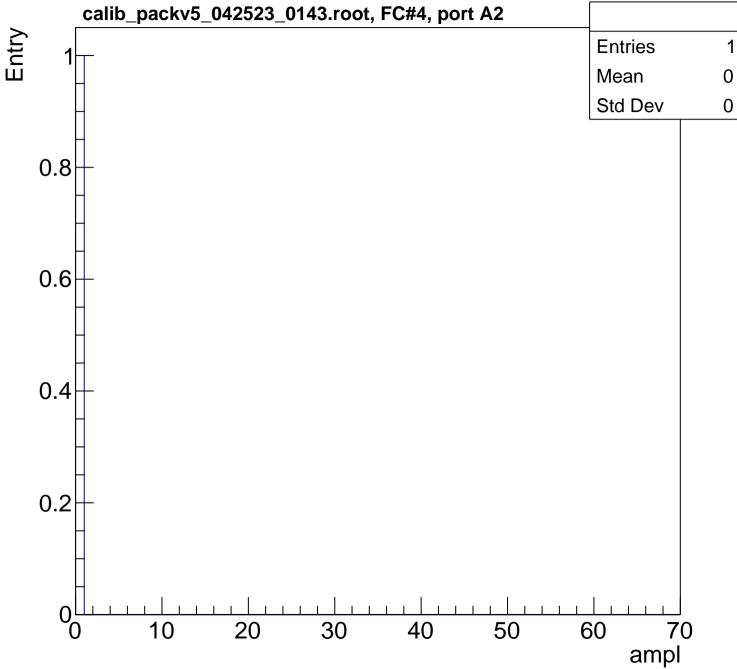


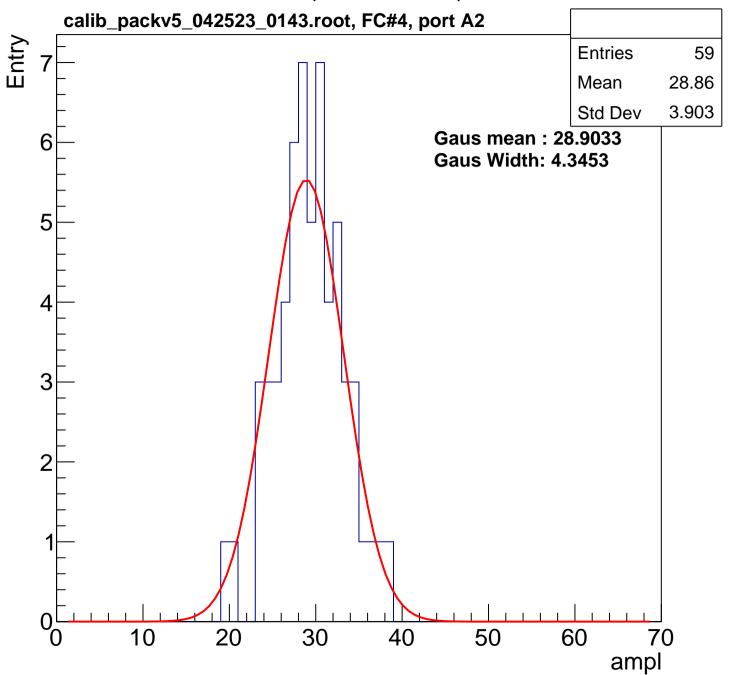


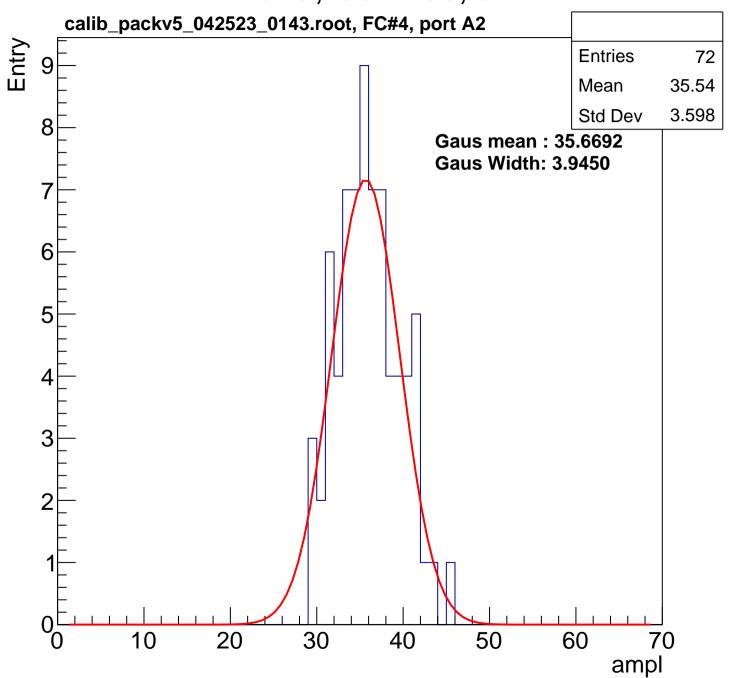


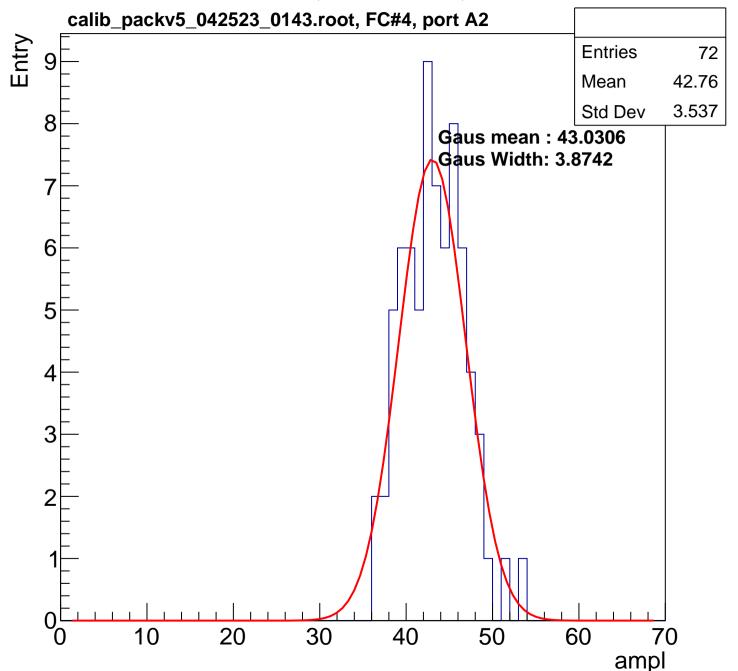


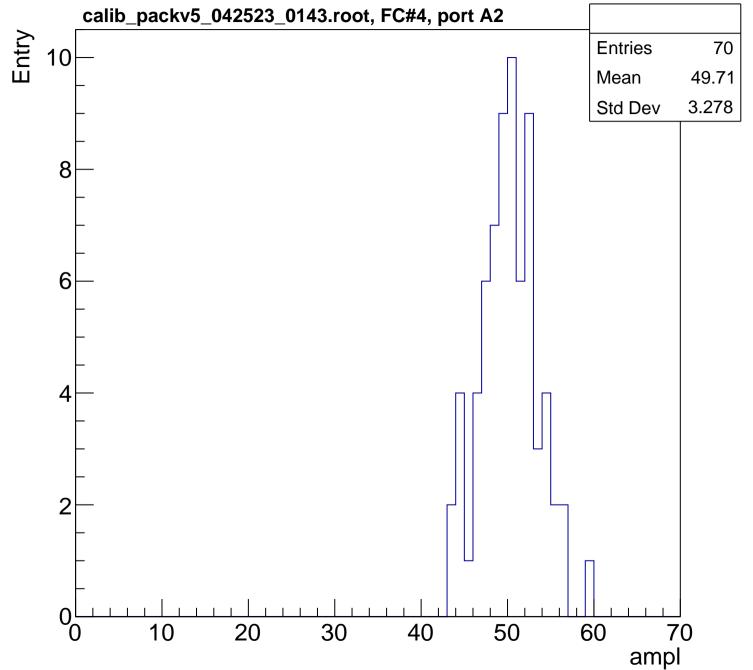


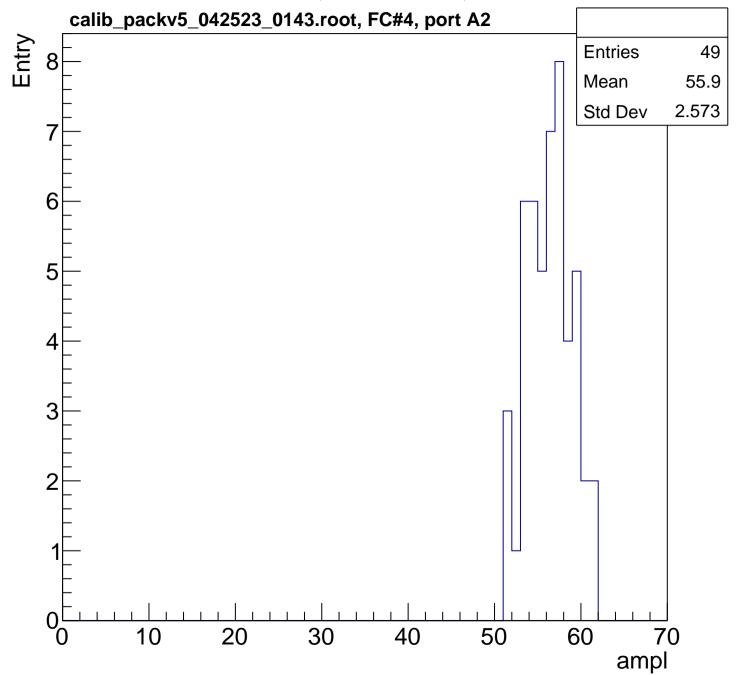


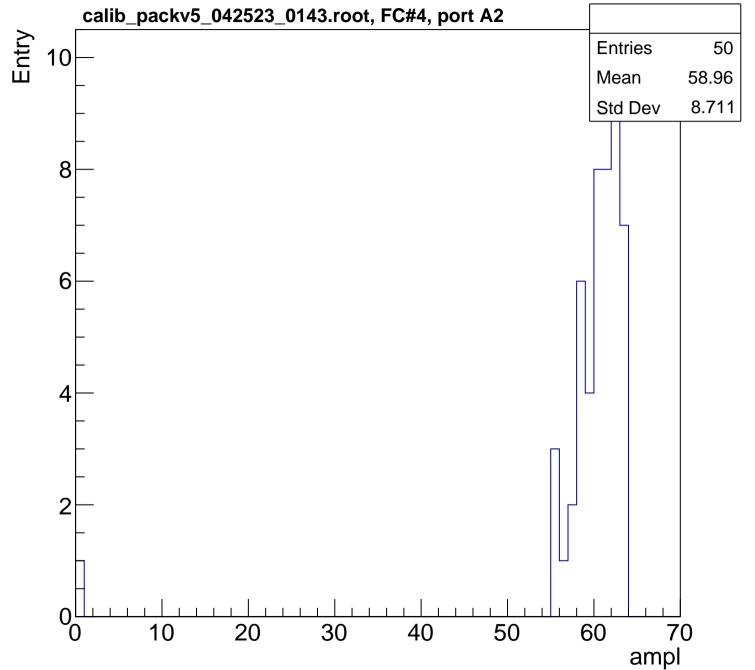


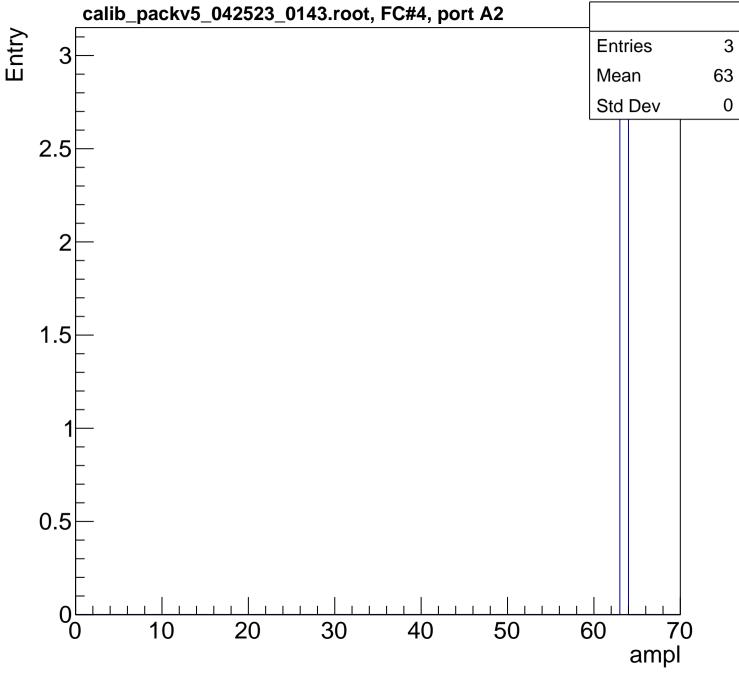




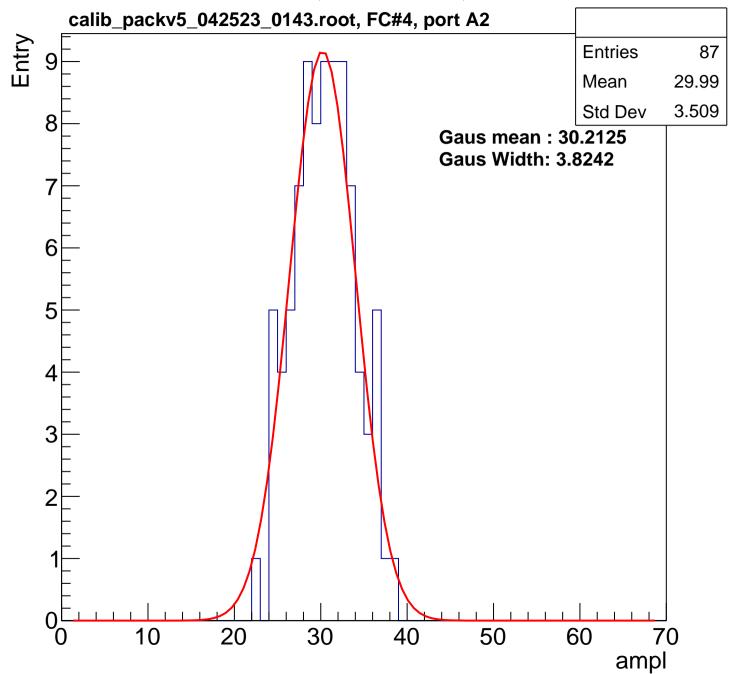


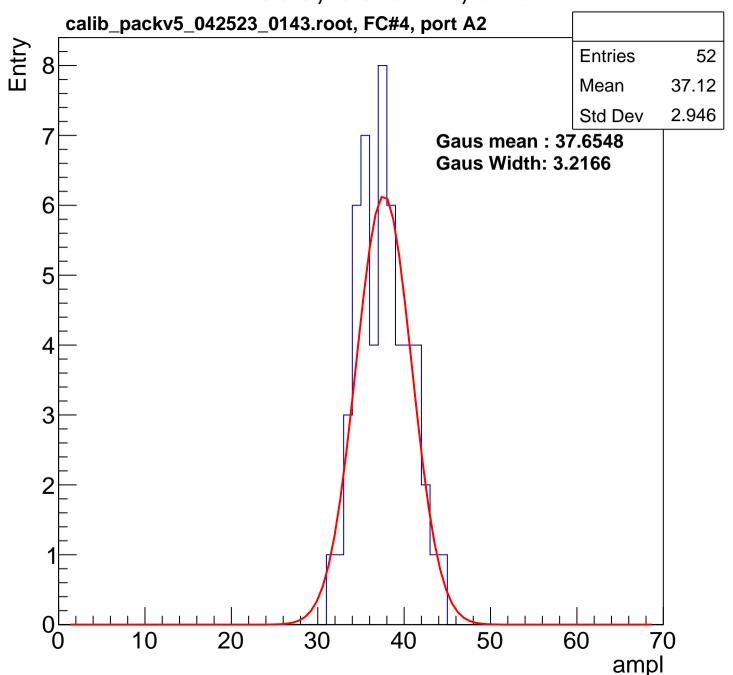


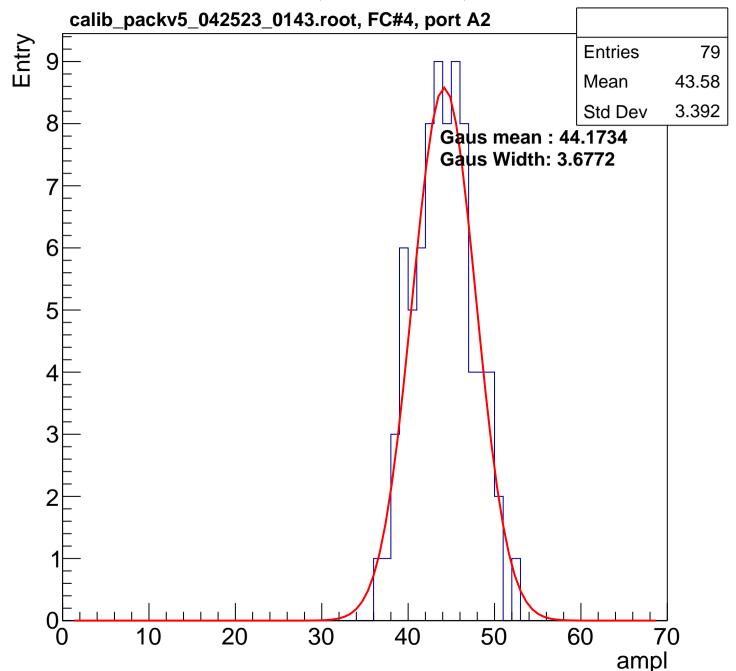


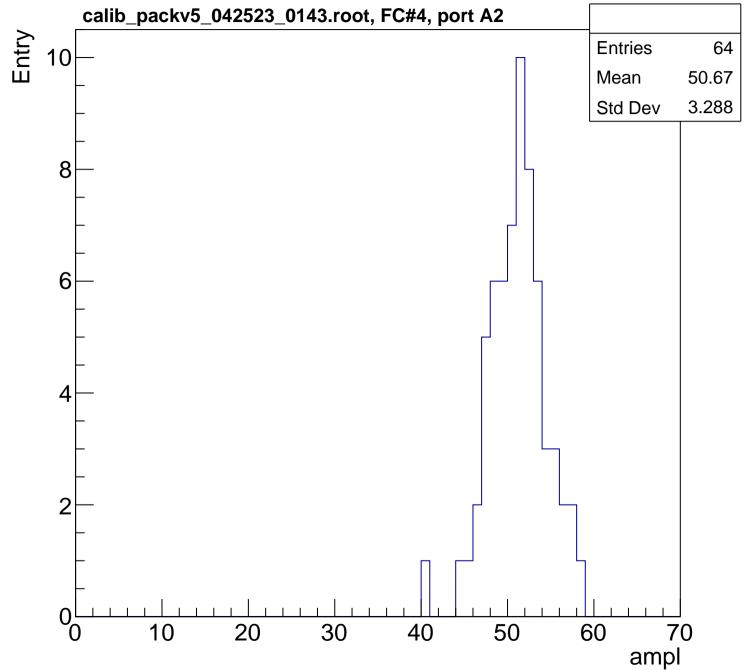


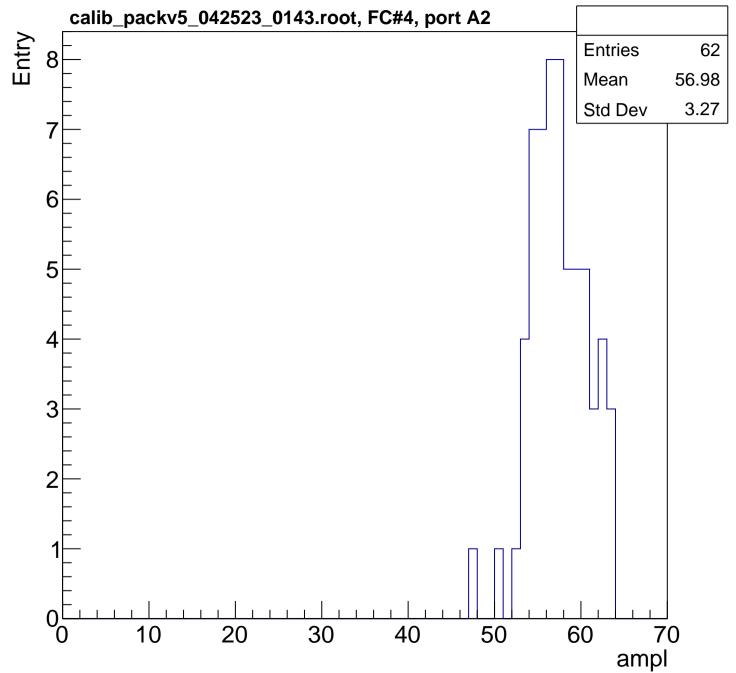


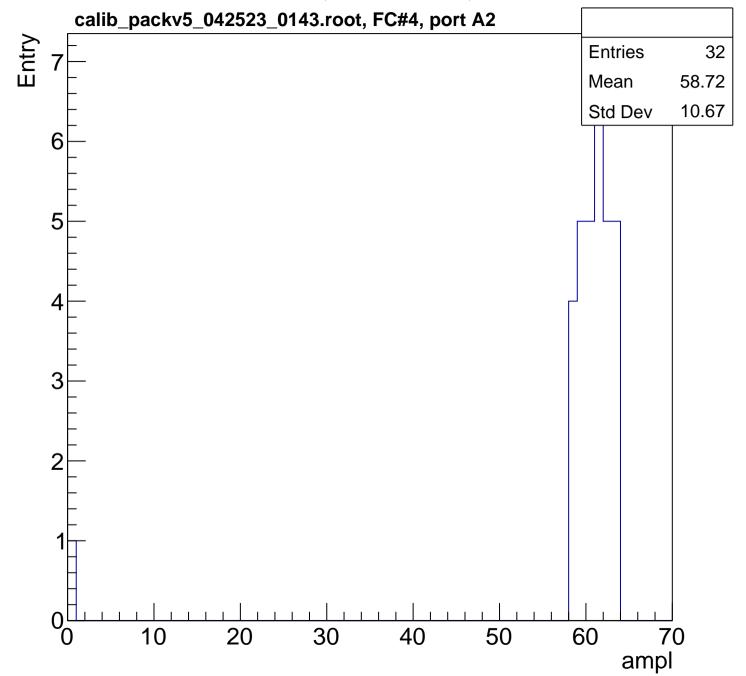


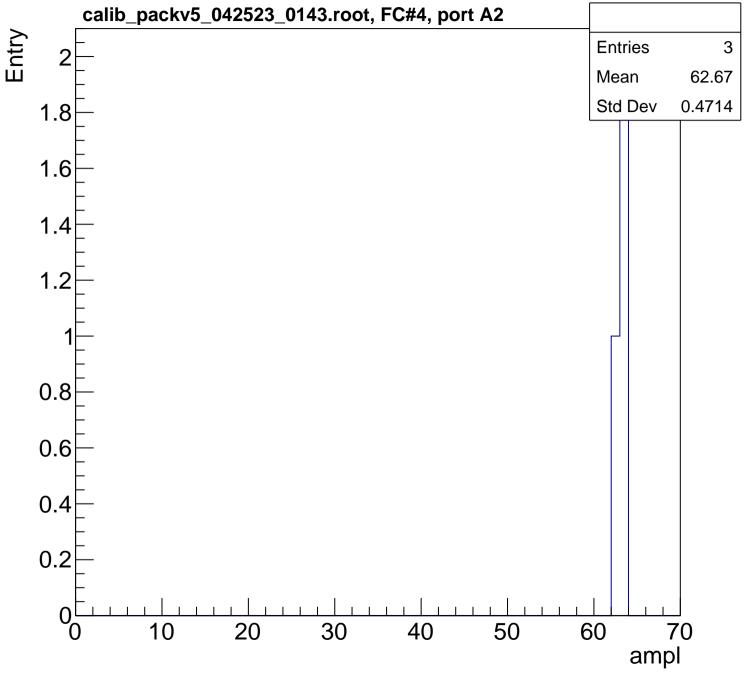




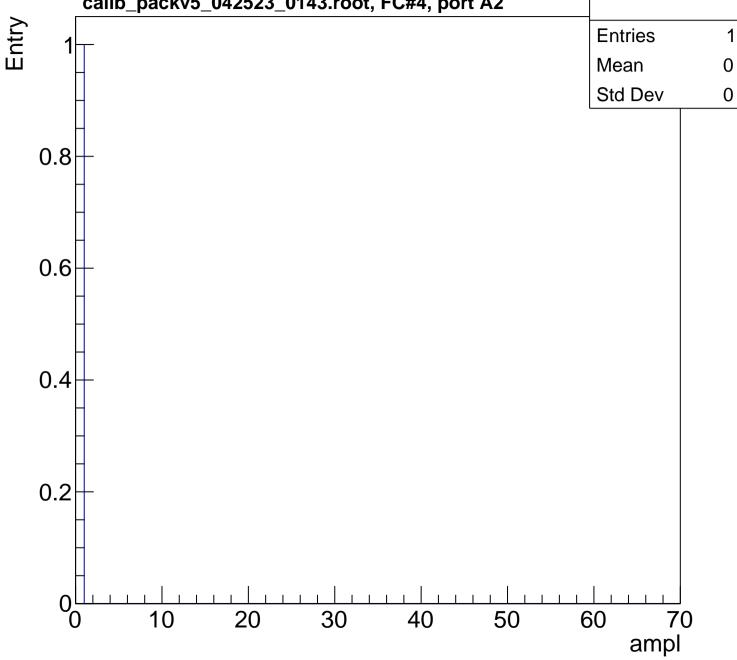


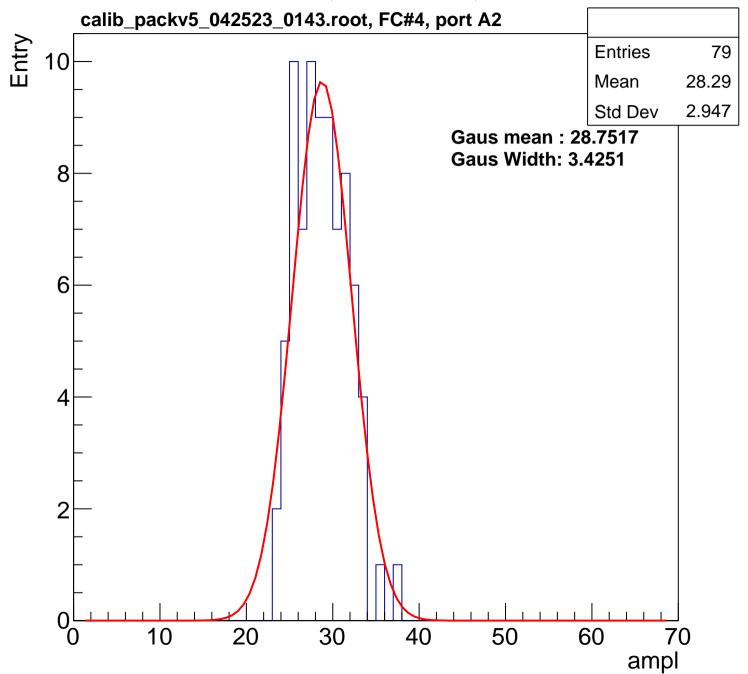


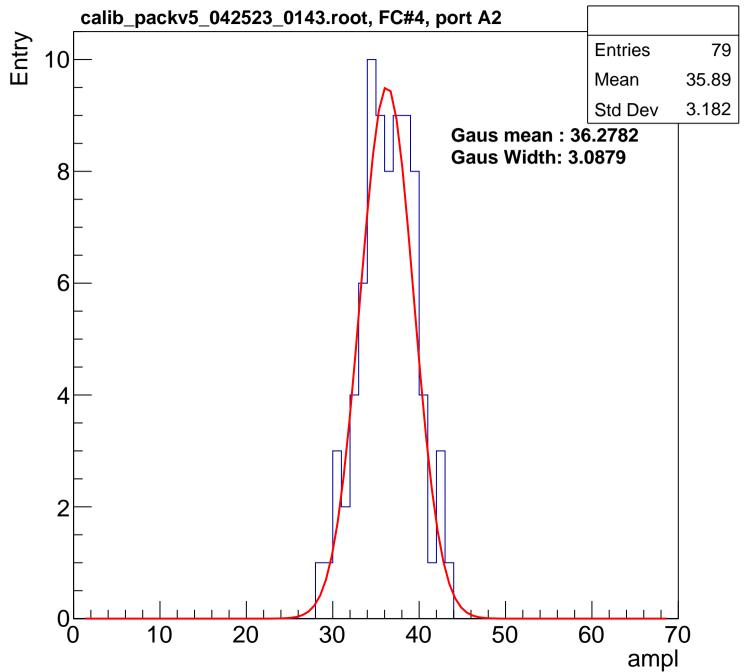


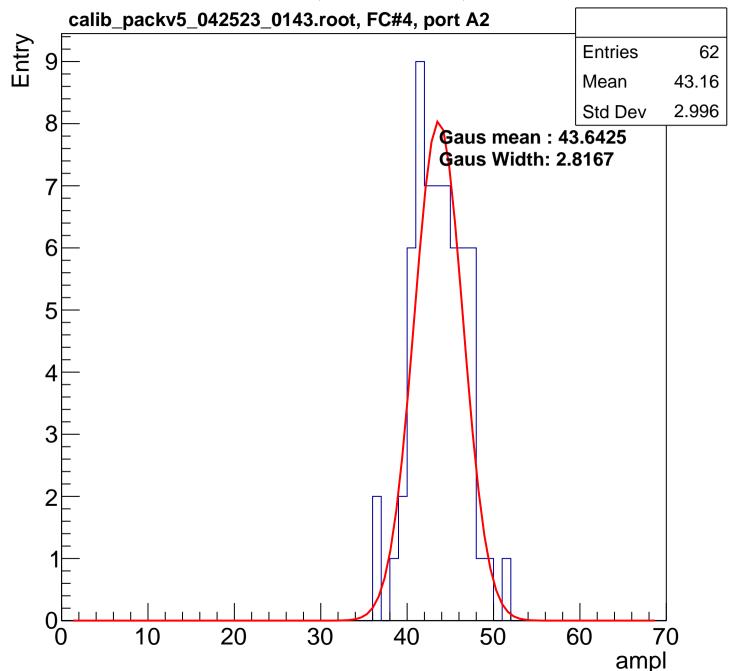


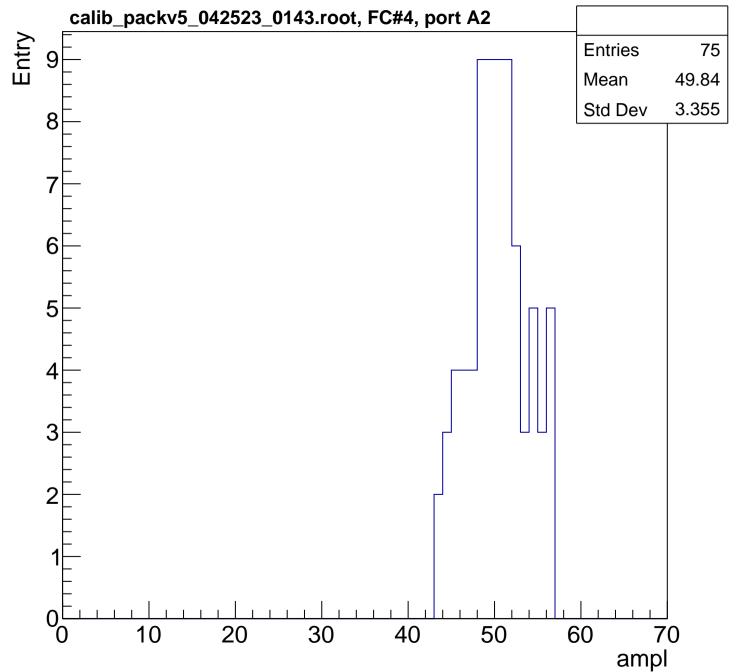
B1L100S, U8-ch31, adc7 calib_packv5_042523_0143.root, FC#4, port A2

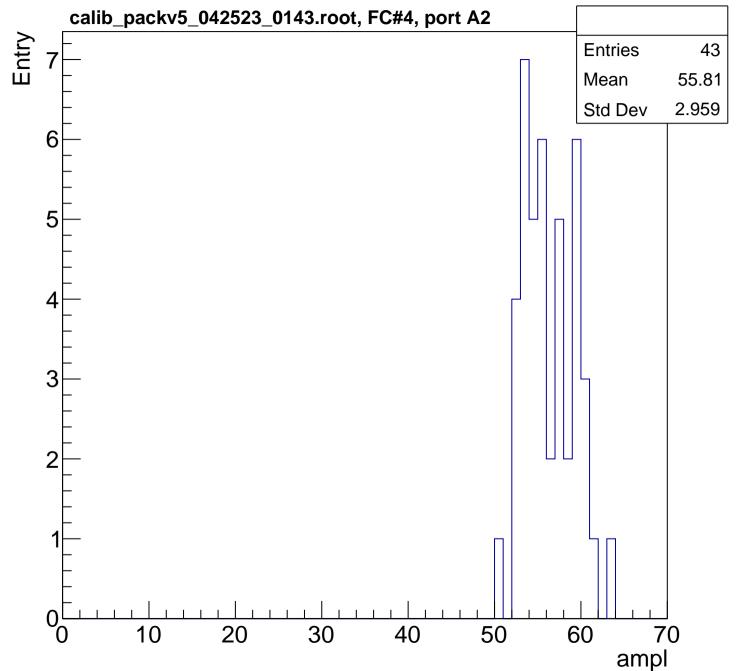


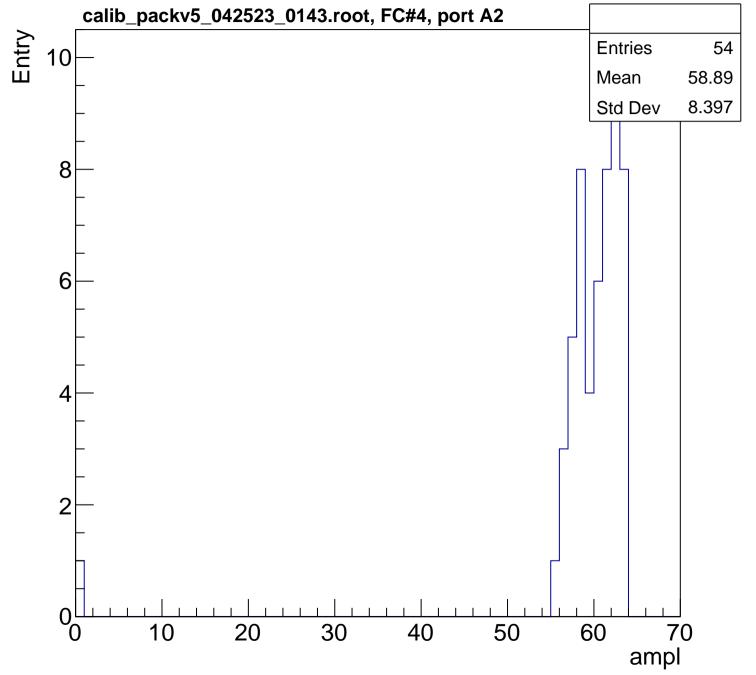


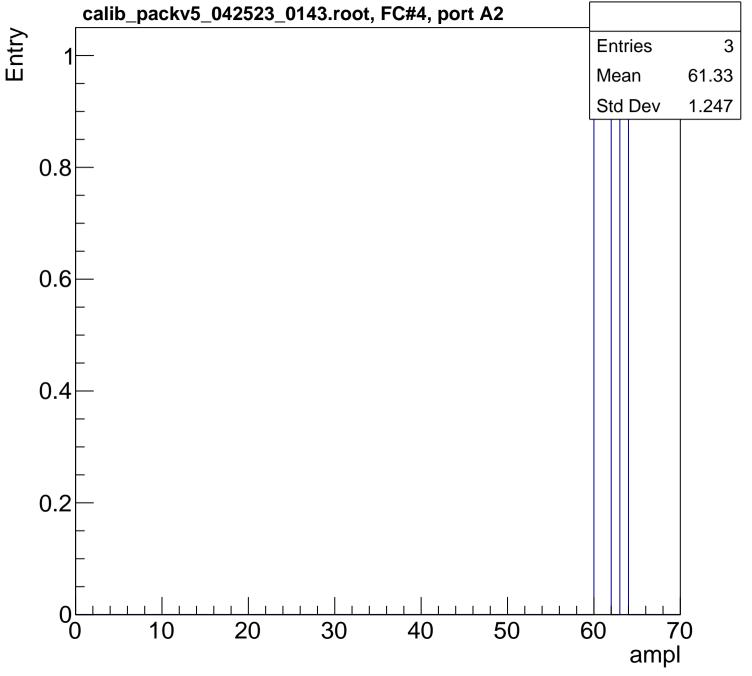


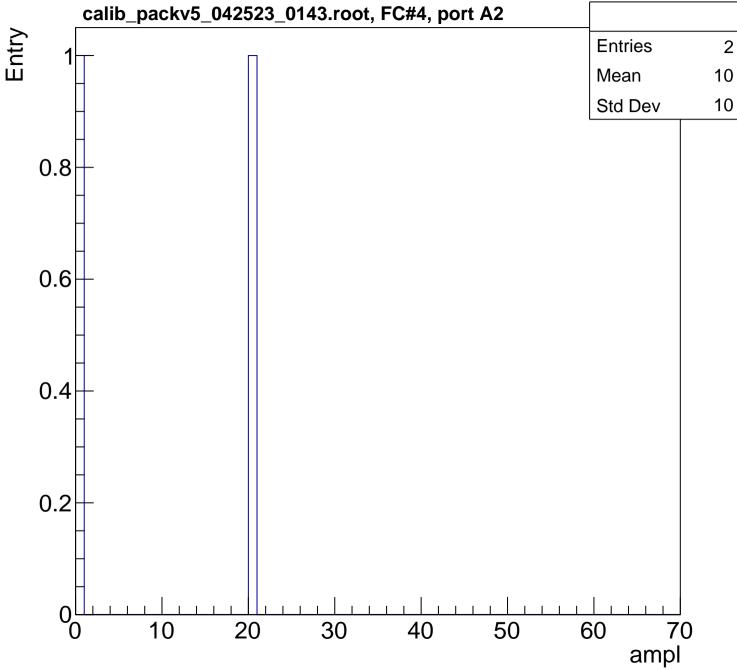


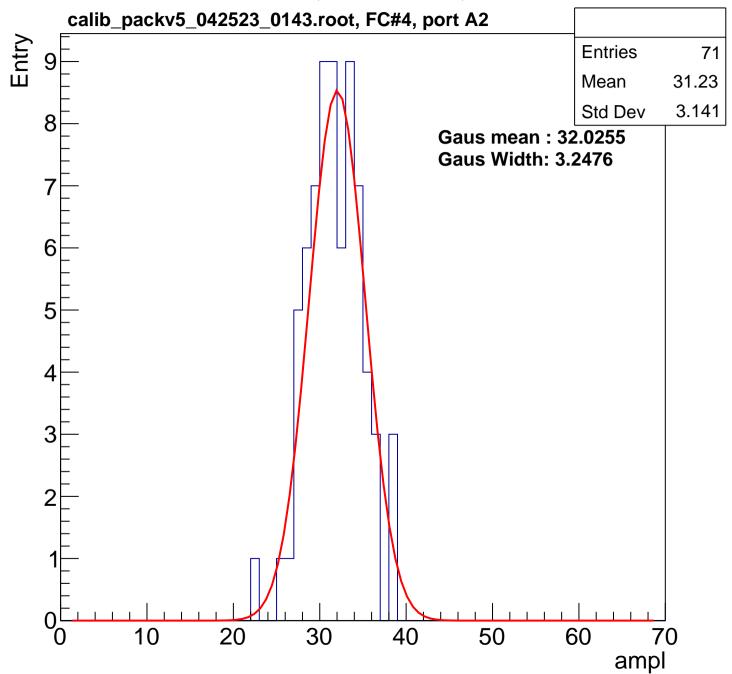


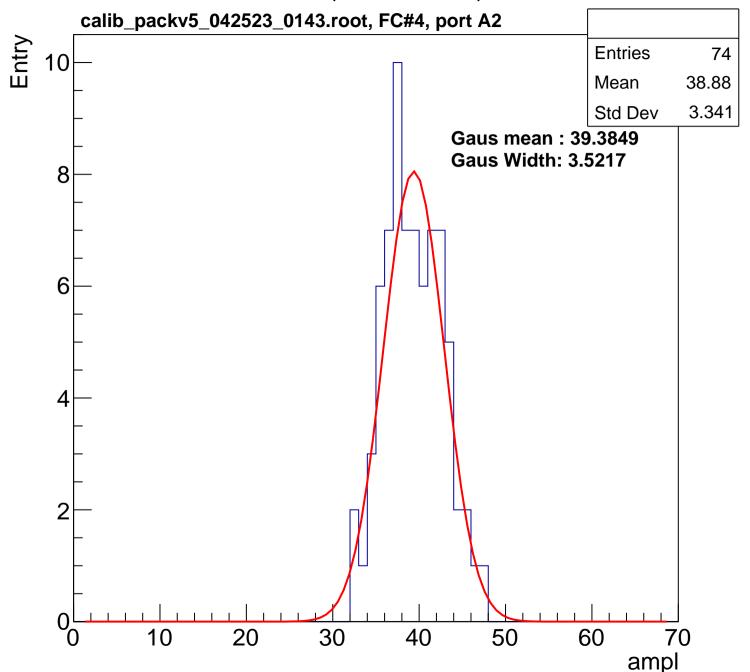


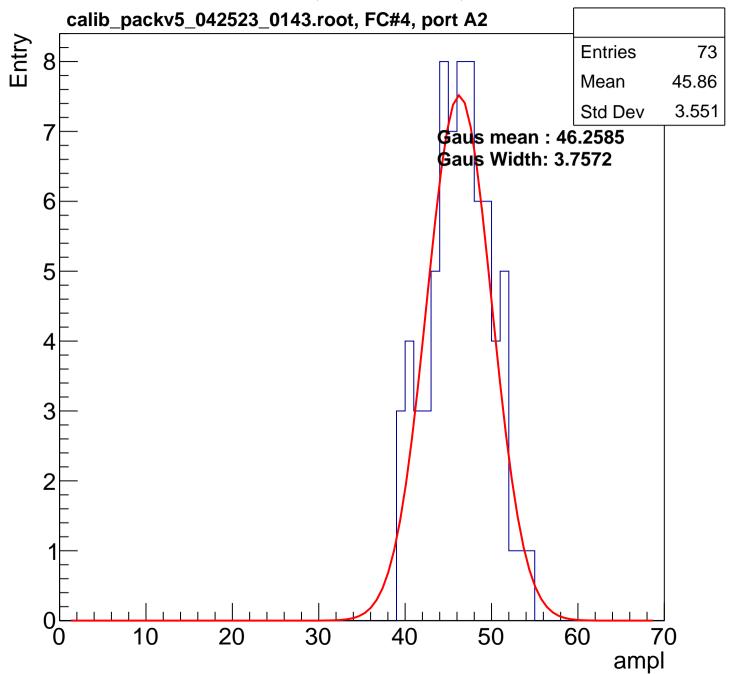


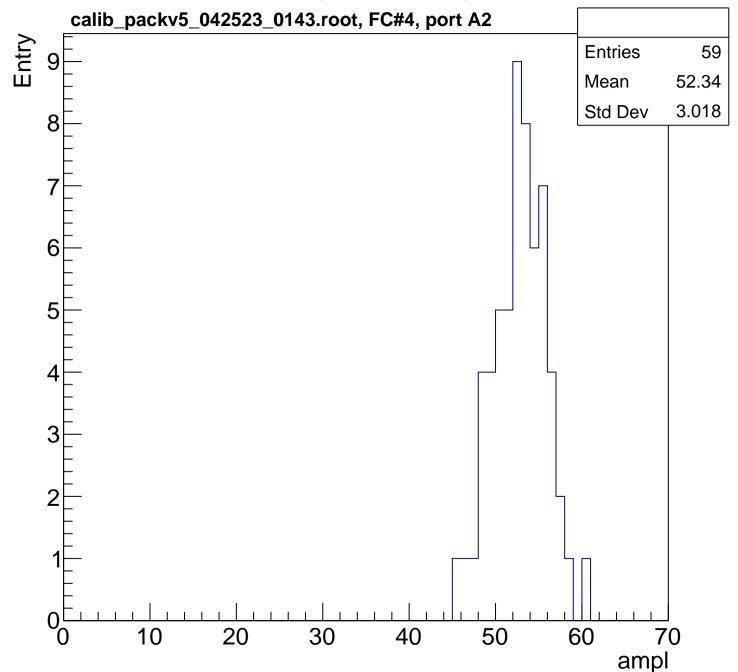


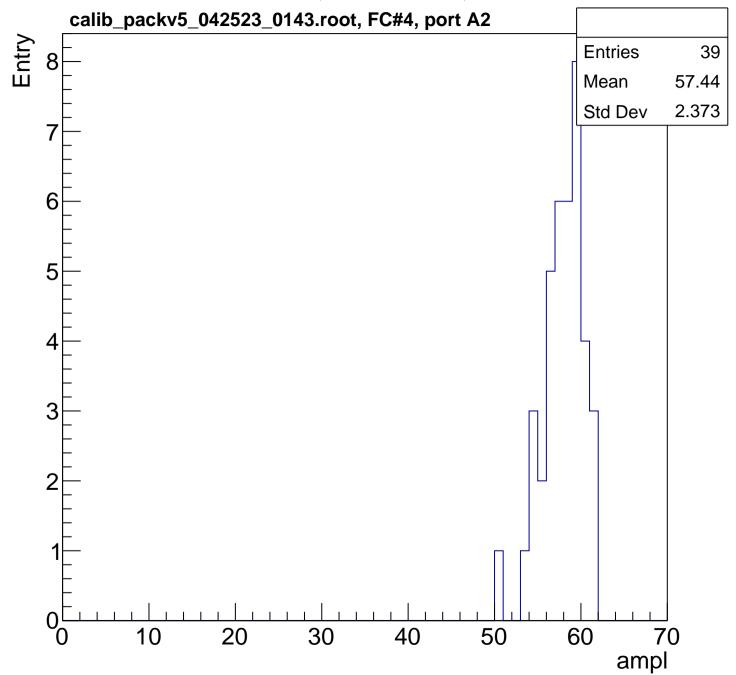


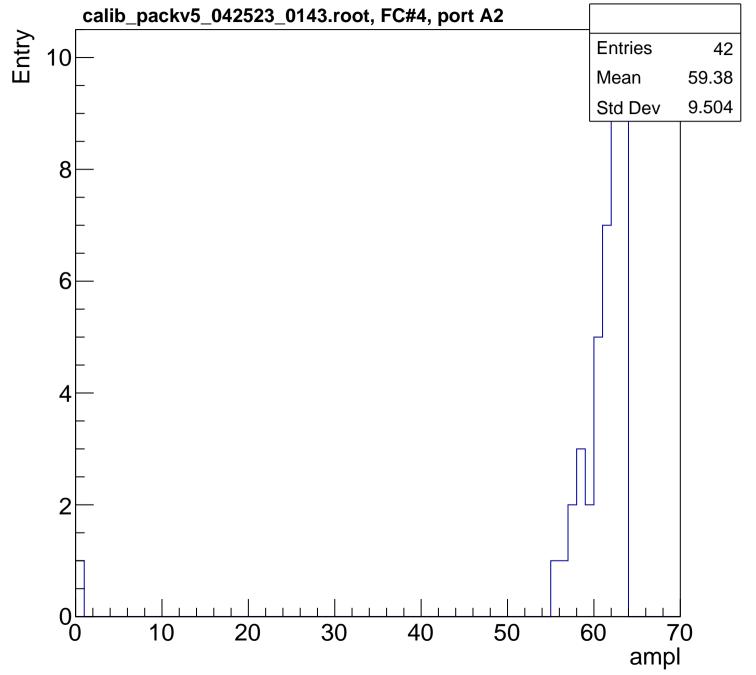


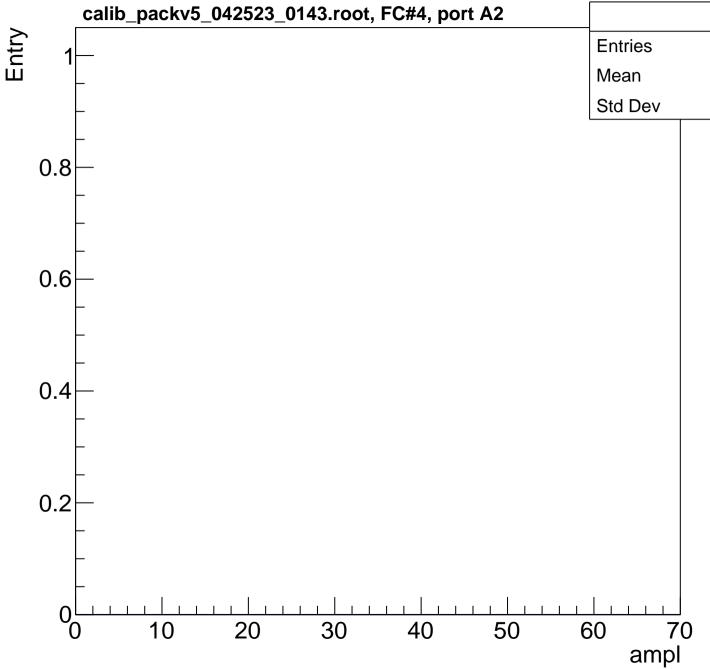


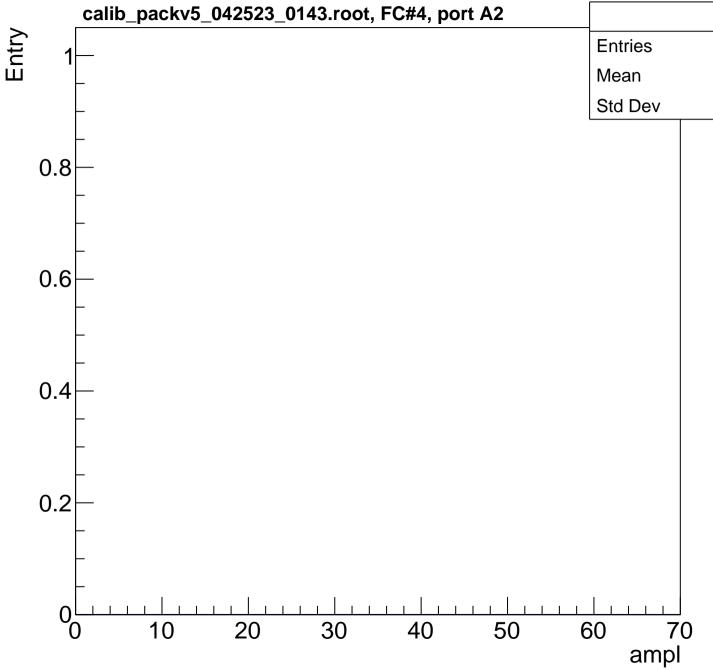


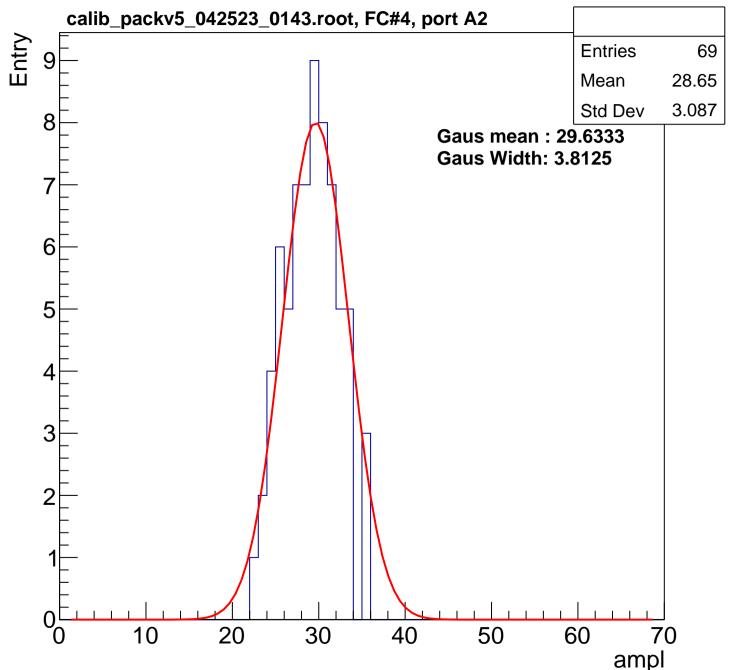


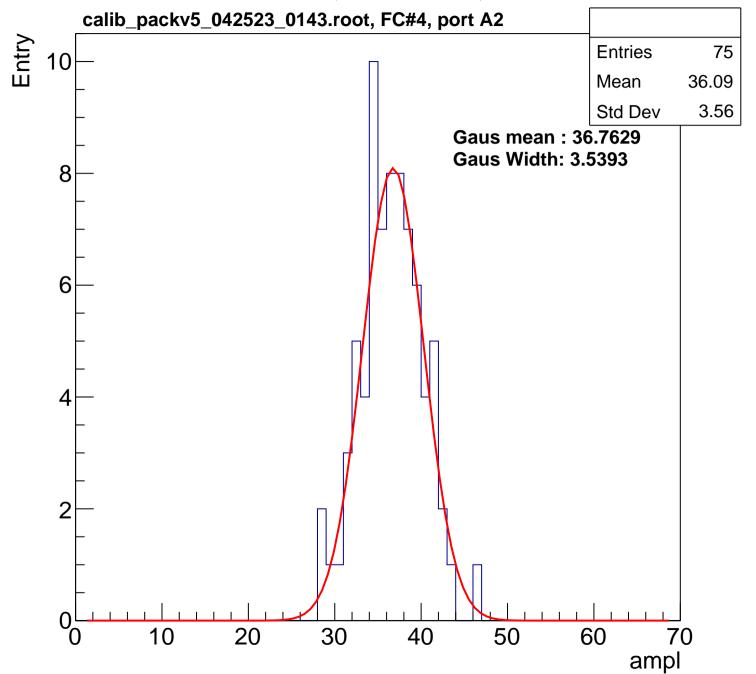


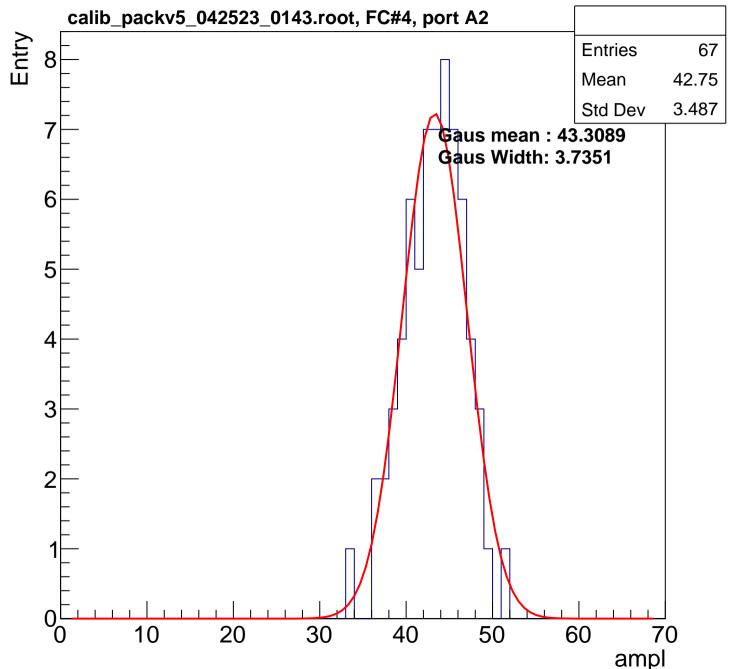


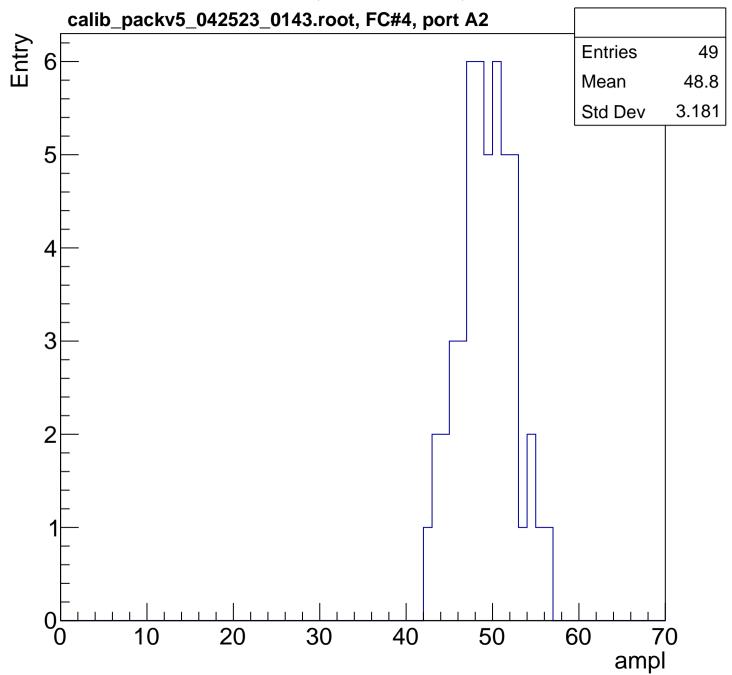


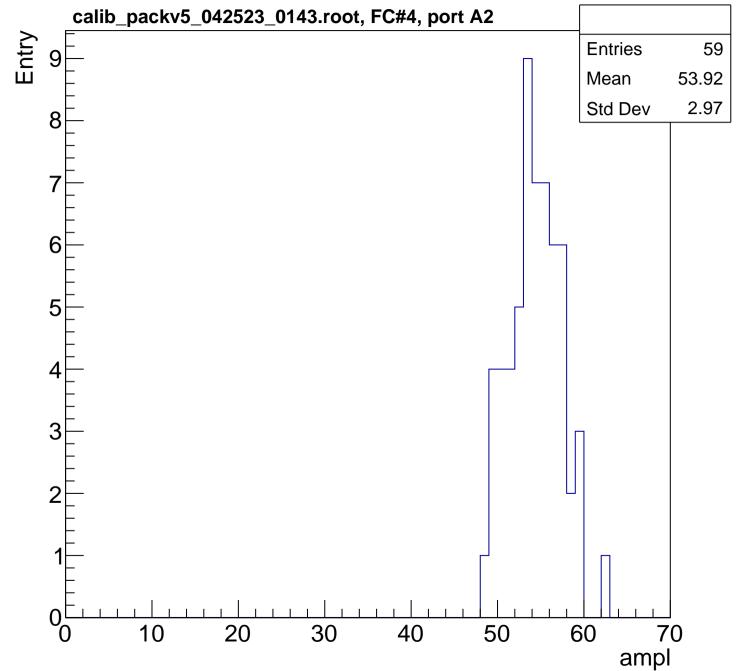


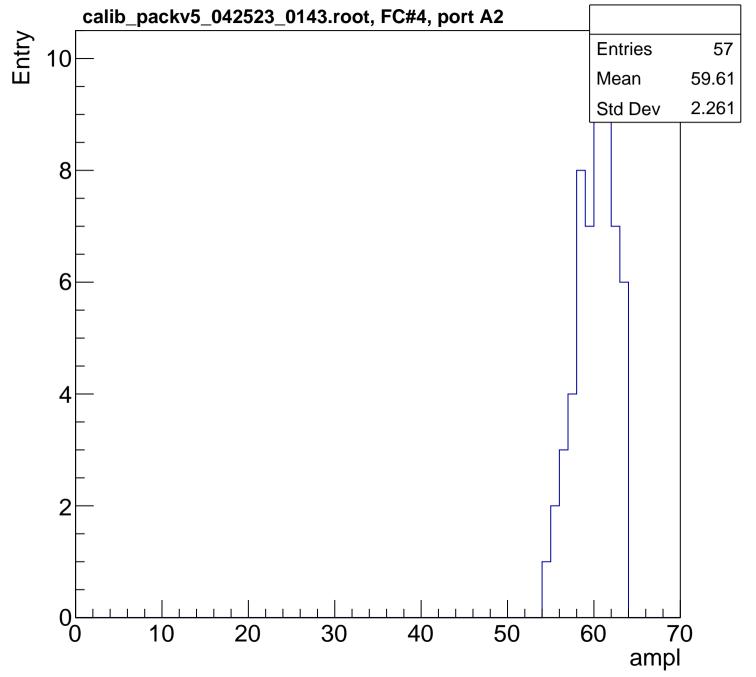


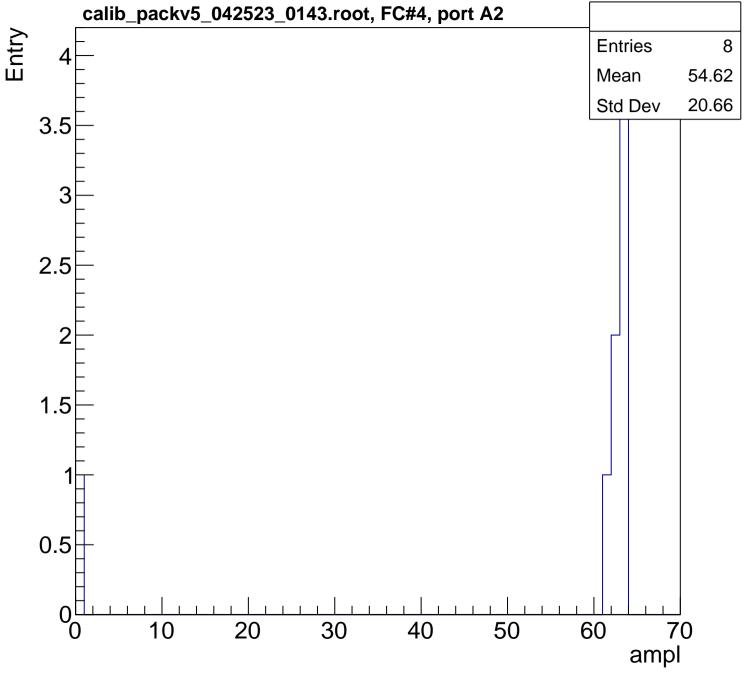




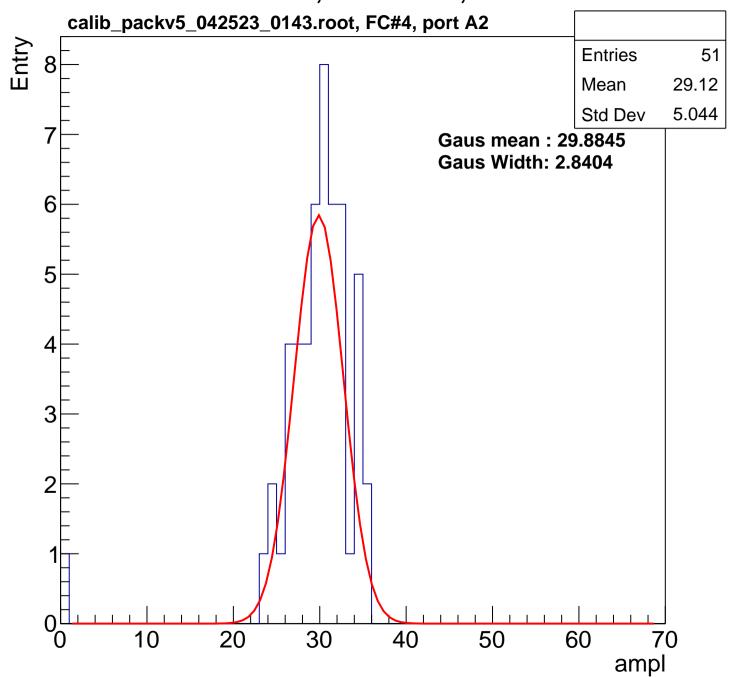


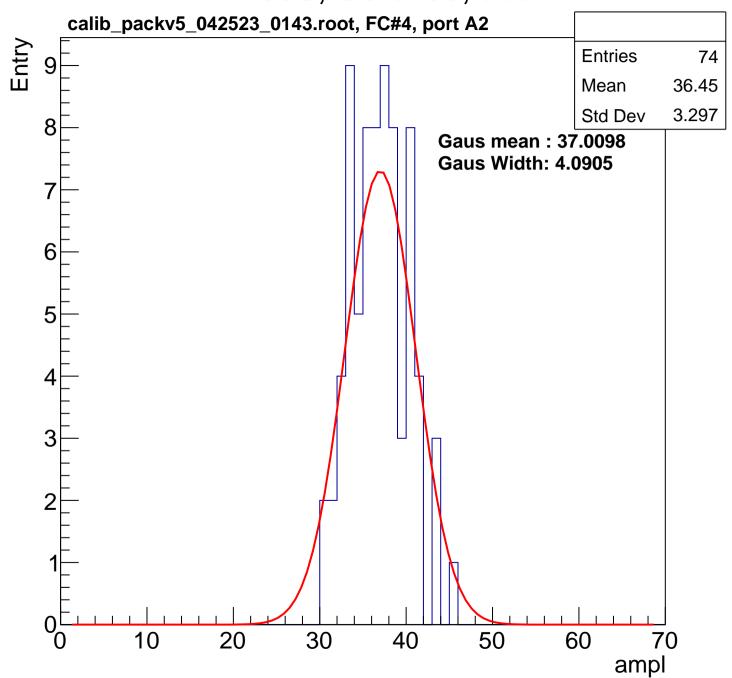


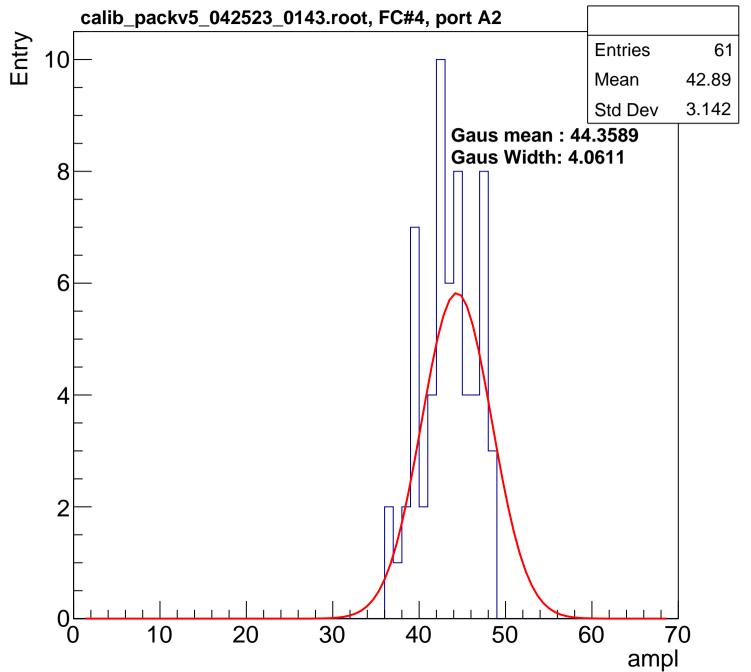


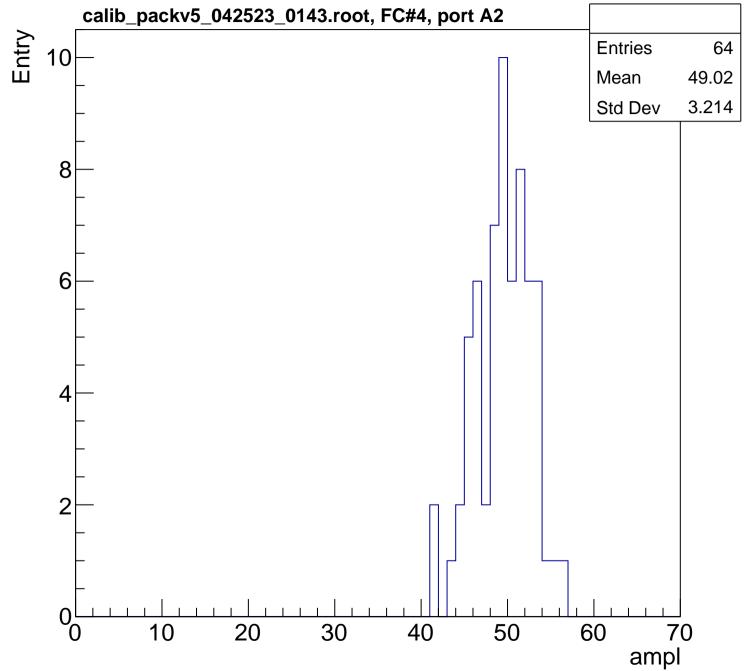


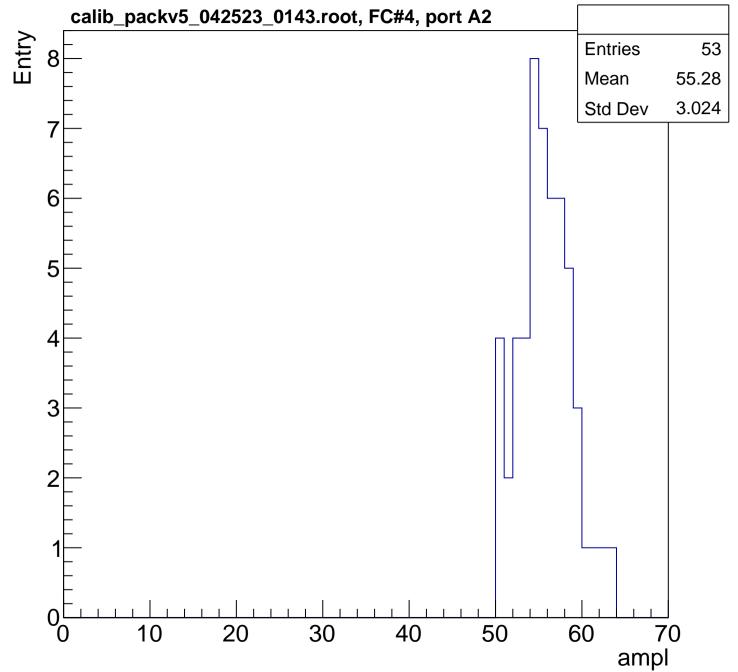


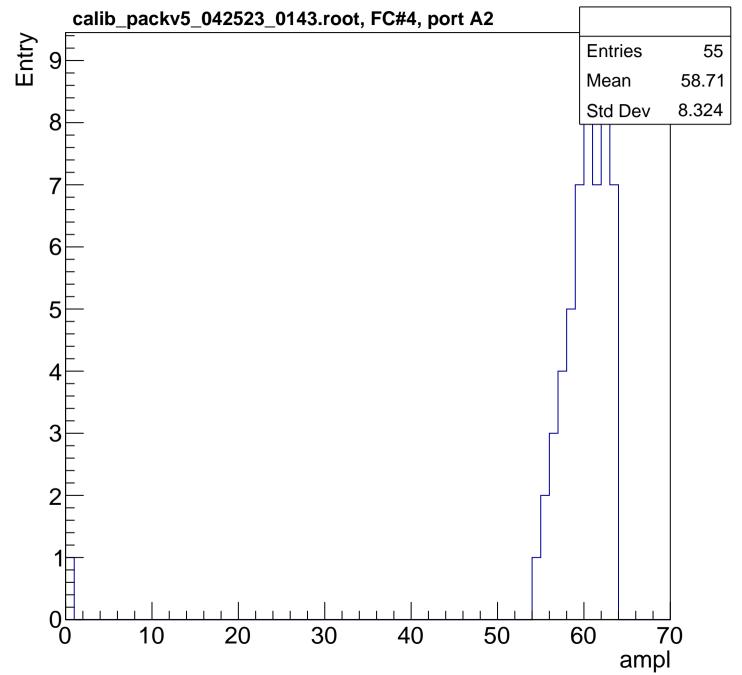


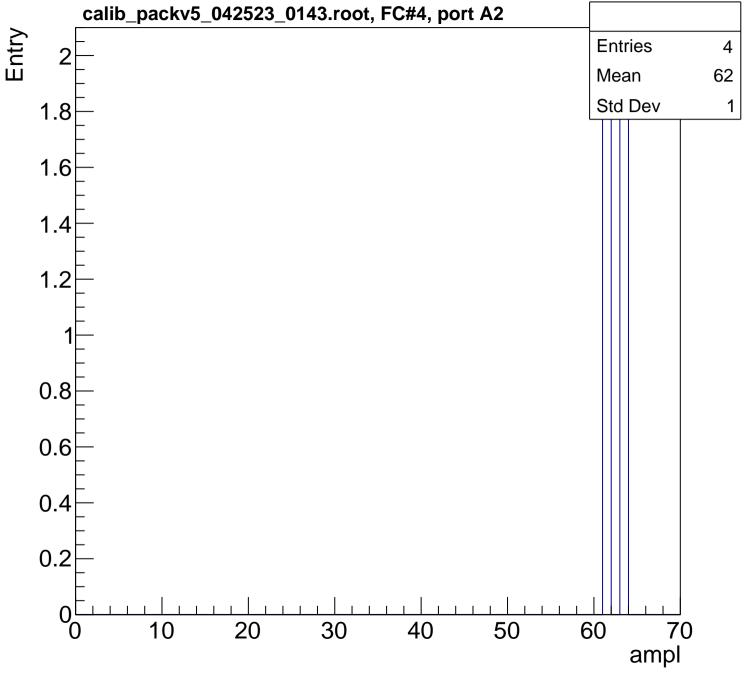


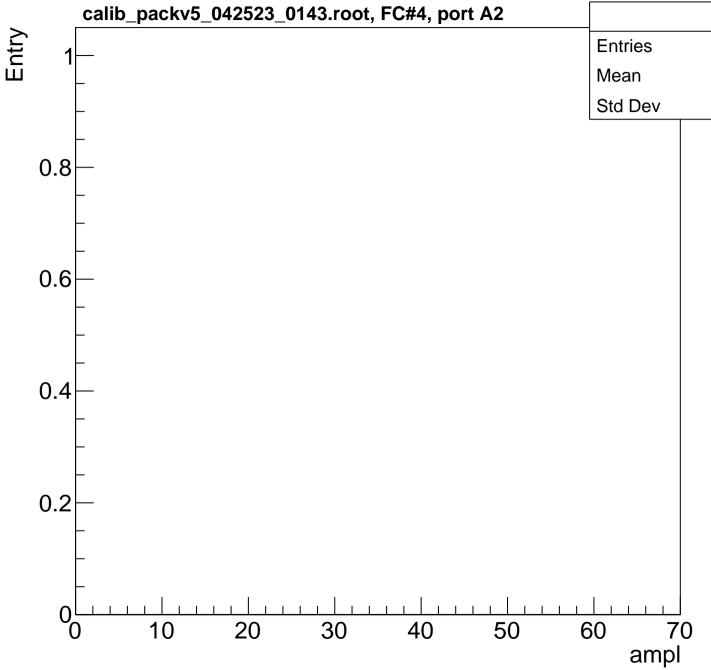


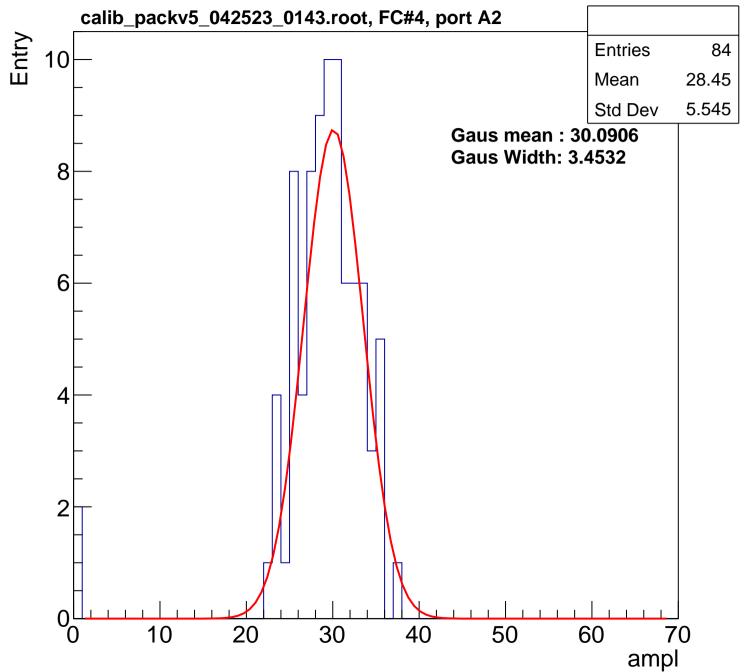


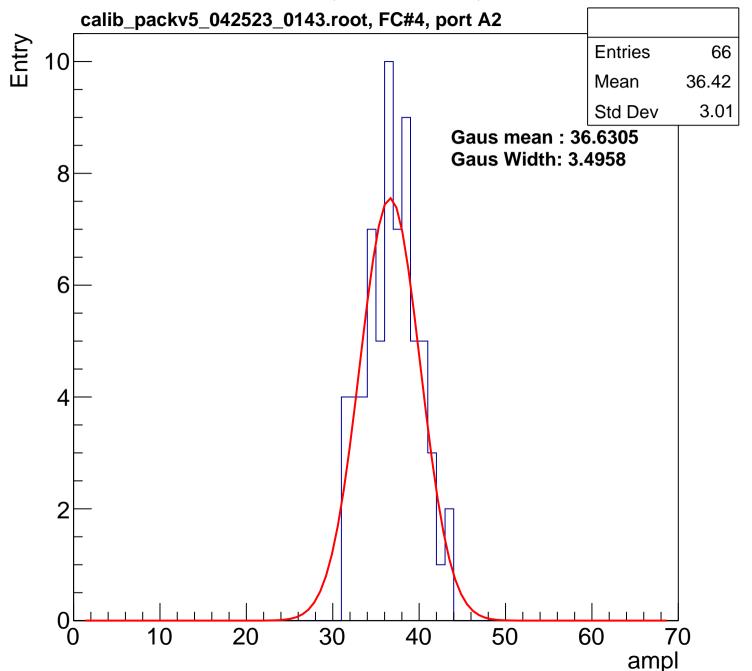


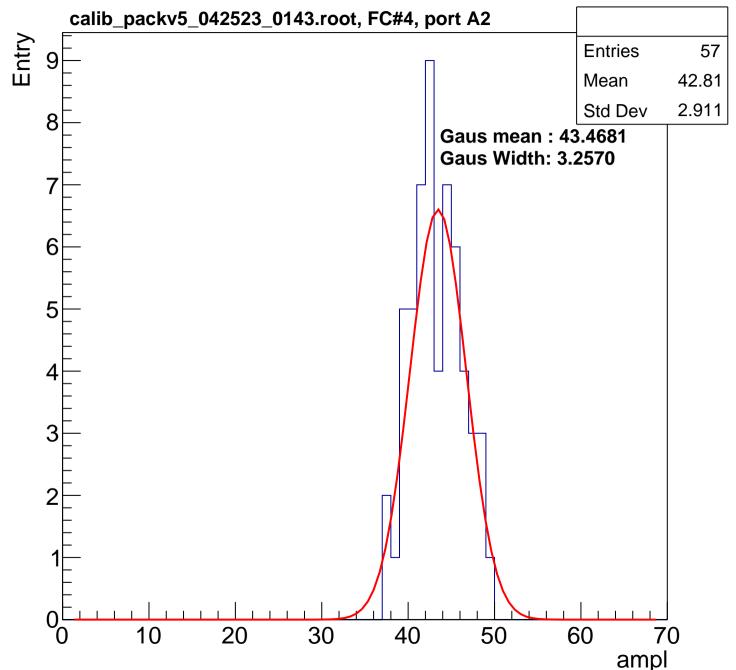


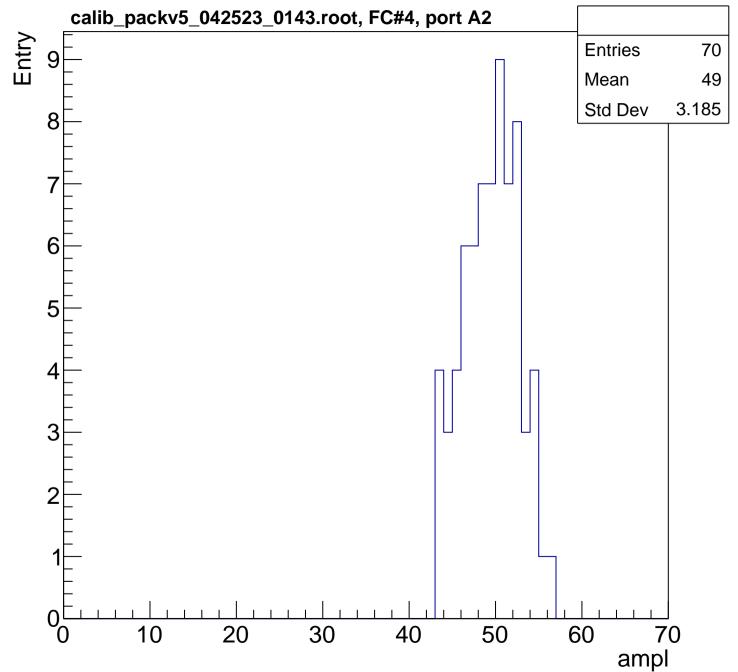


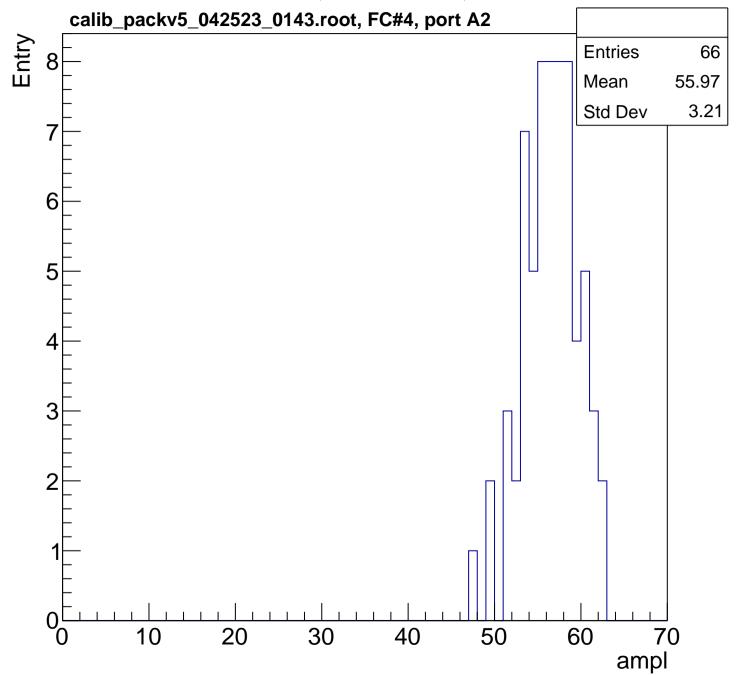


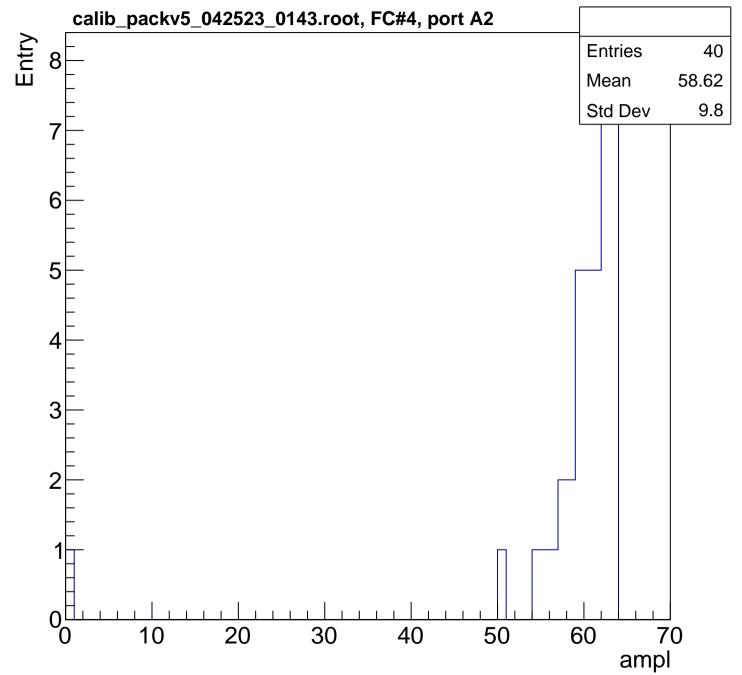


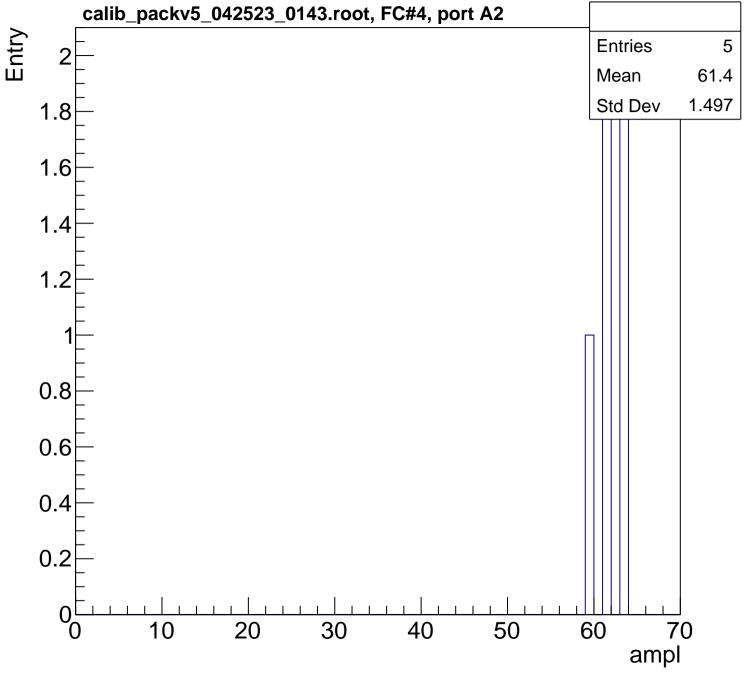












B1L100S, U8-ch36, adc7 calib_packv5_042523_0143.root, FC#4, port A2 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2

30

40

50

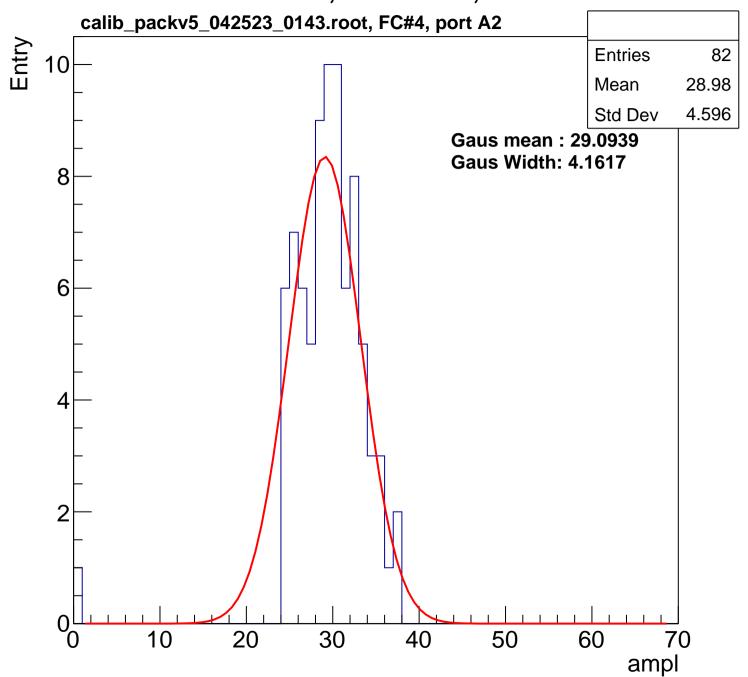
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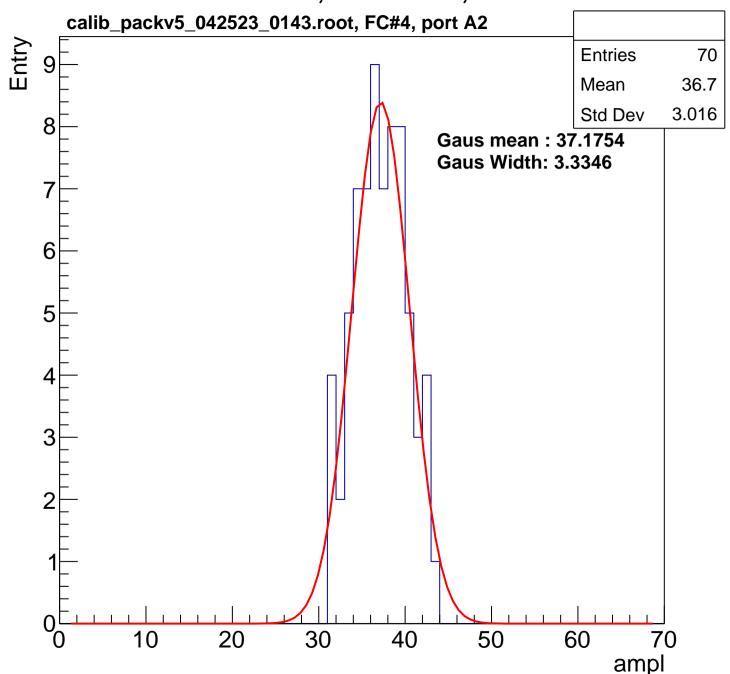
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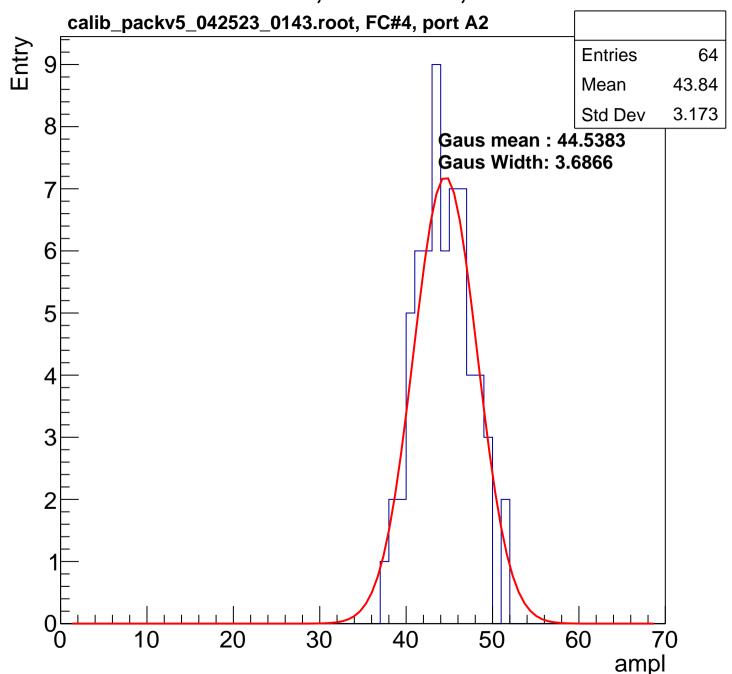
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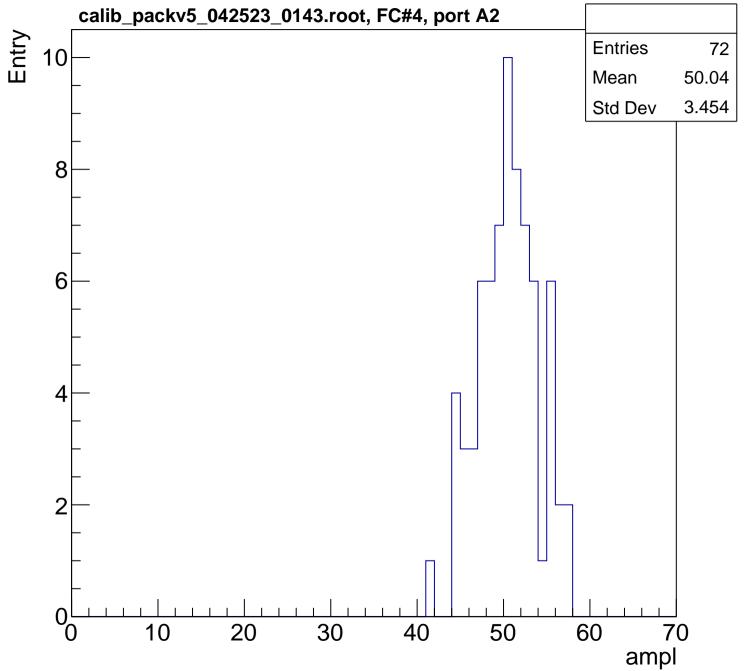
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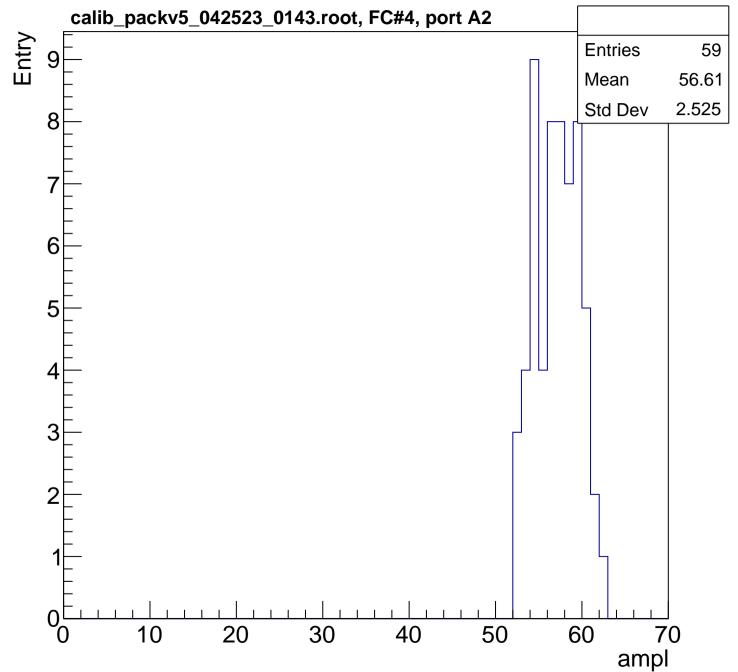
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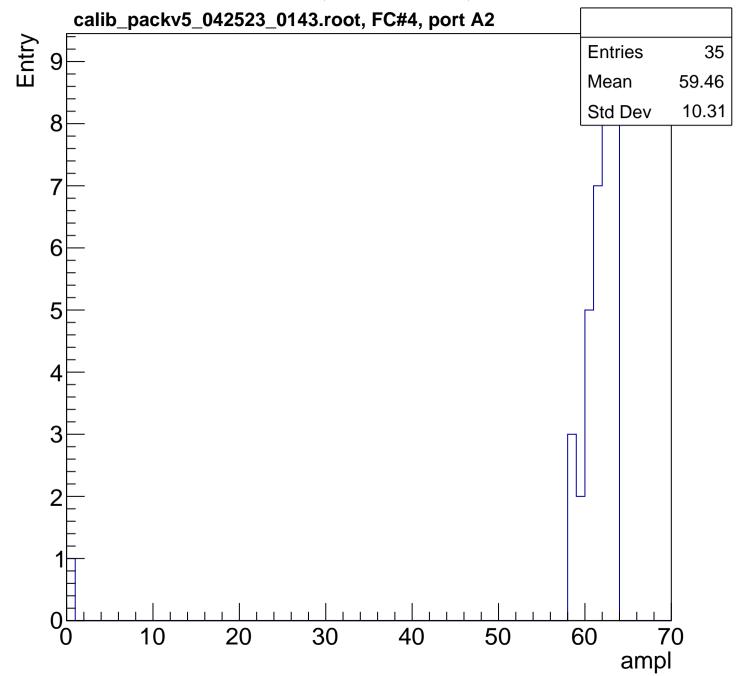


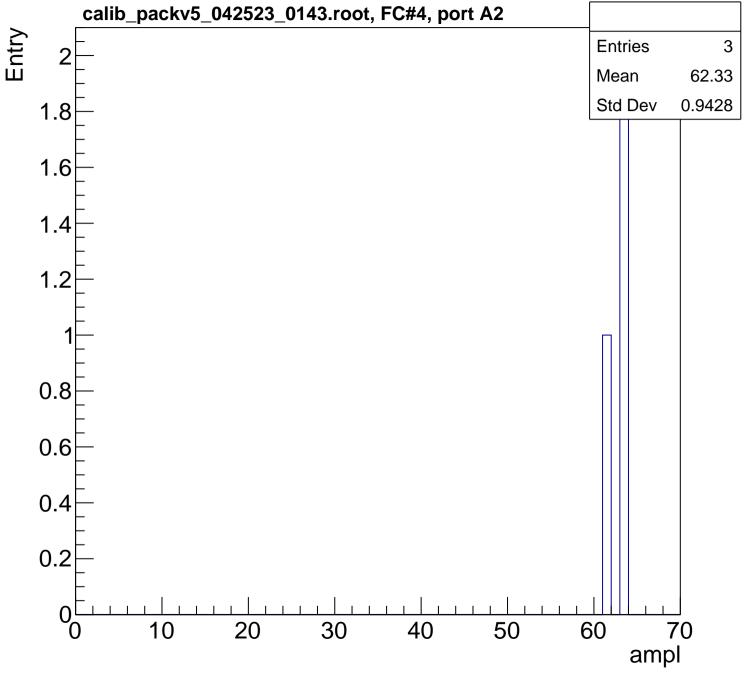




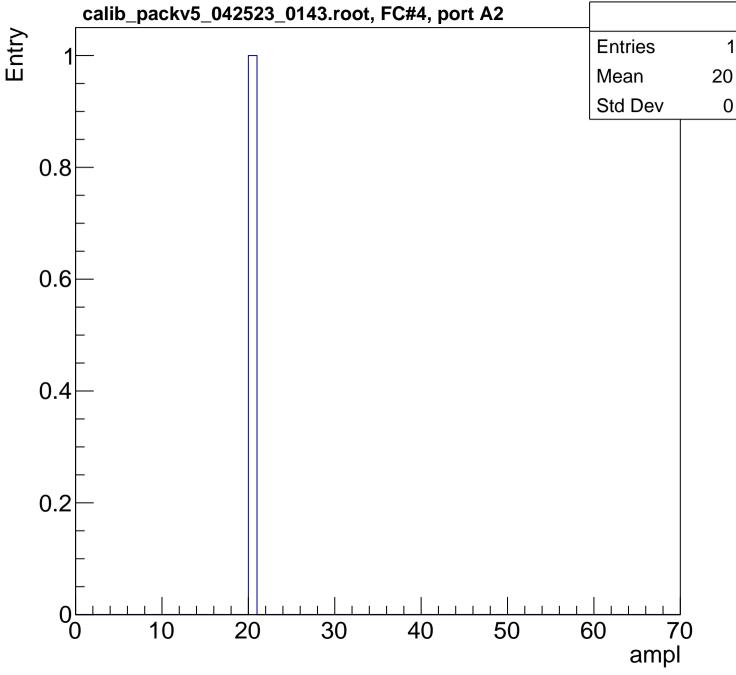


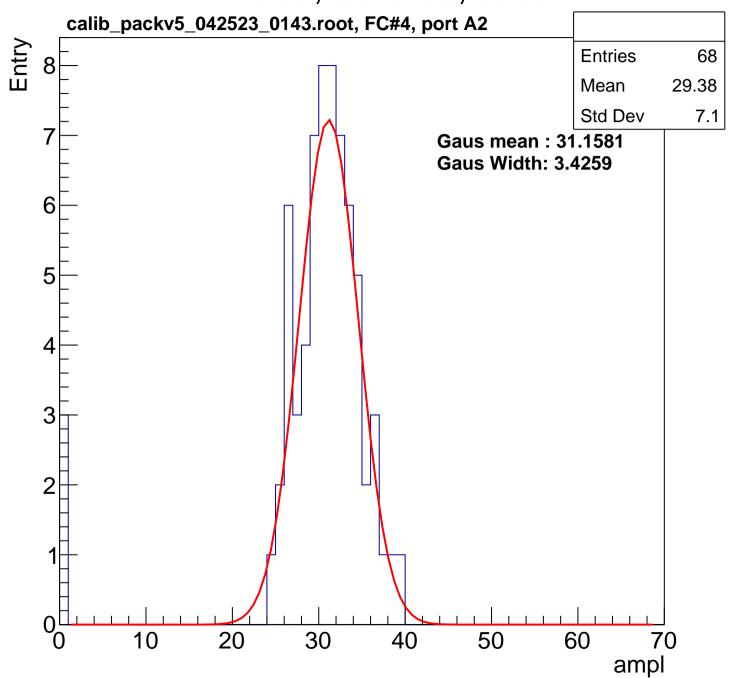


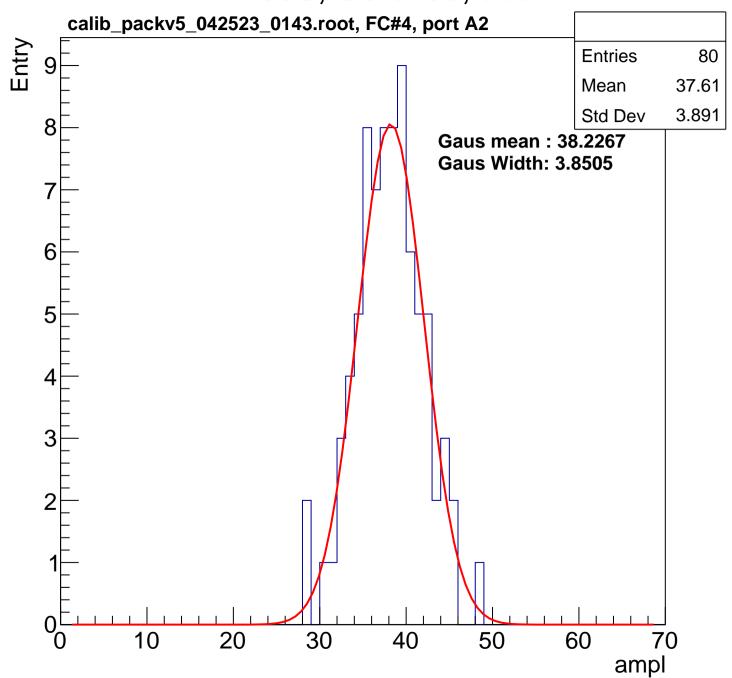


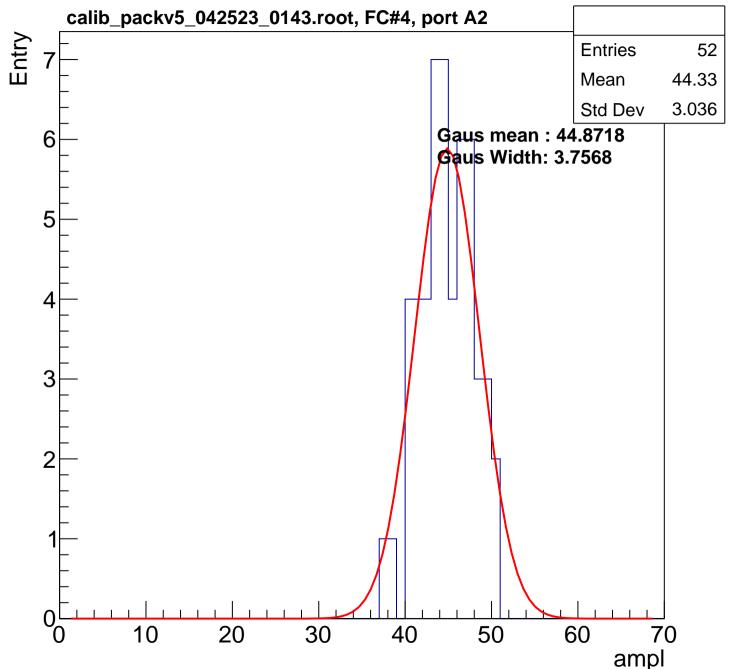


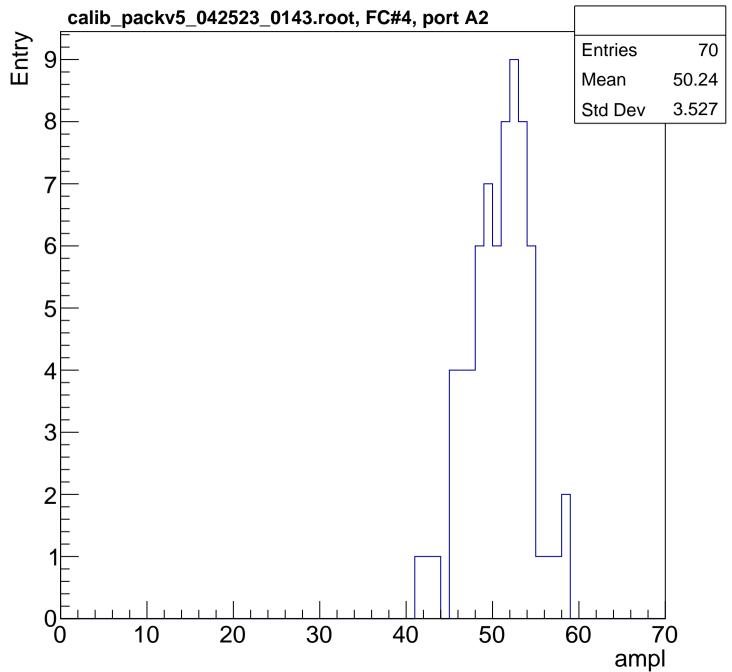
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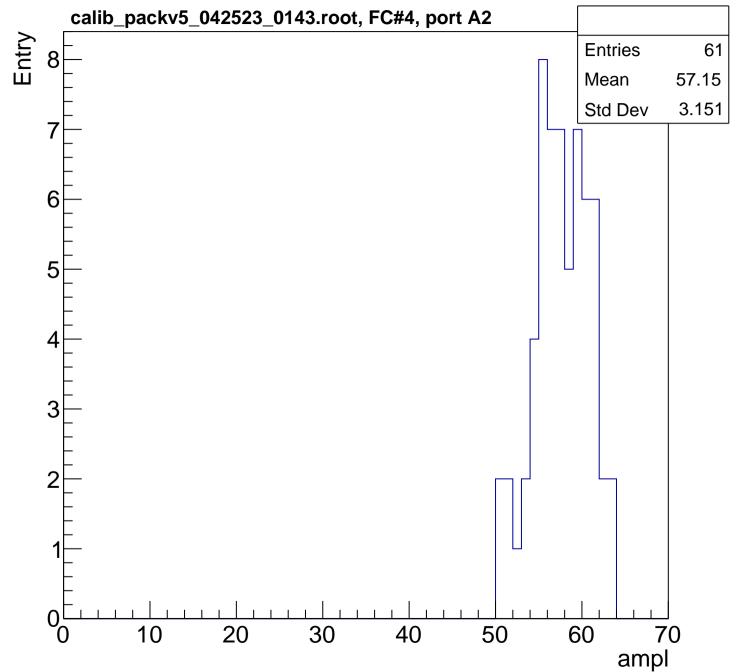


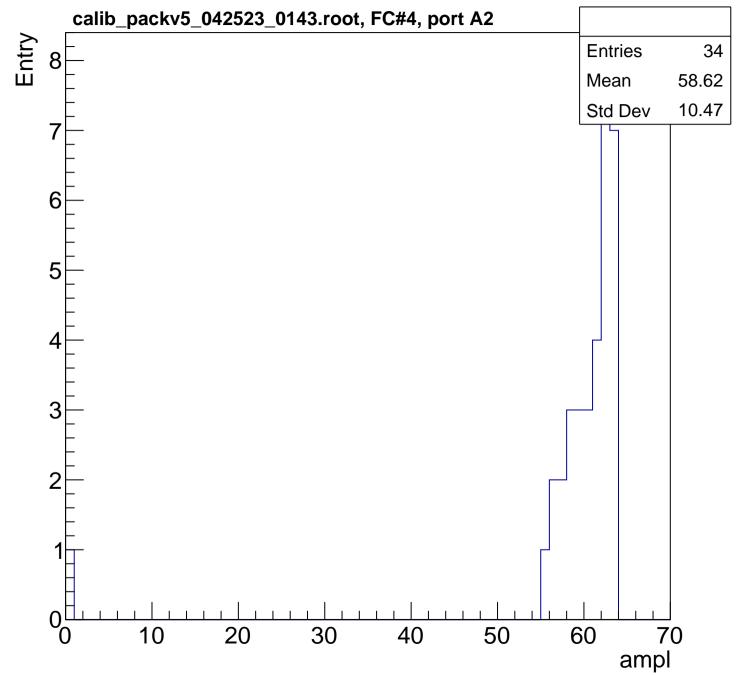


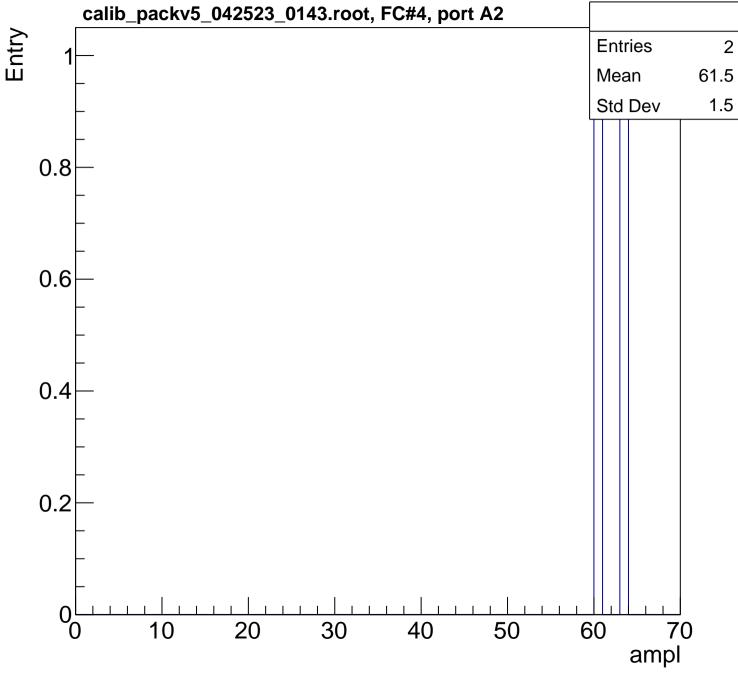




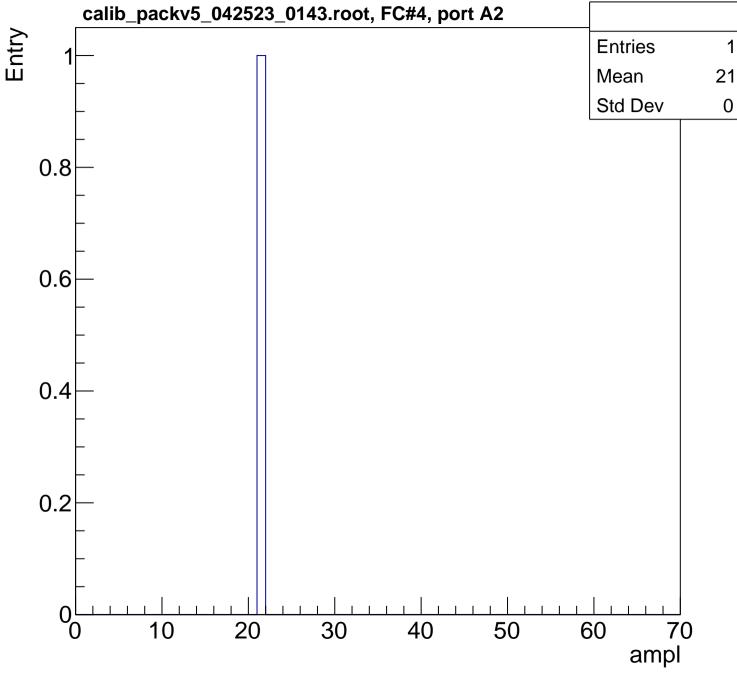


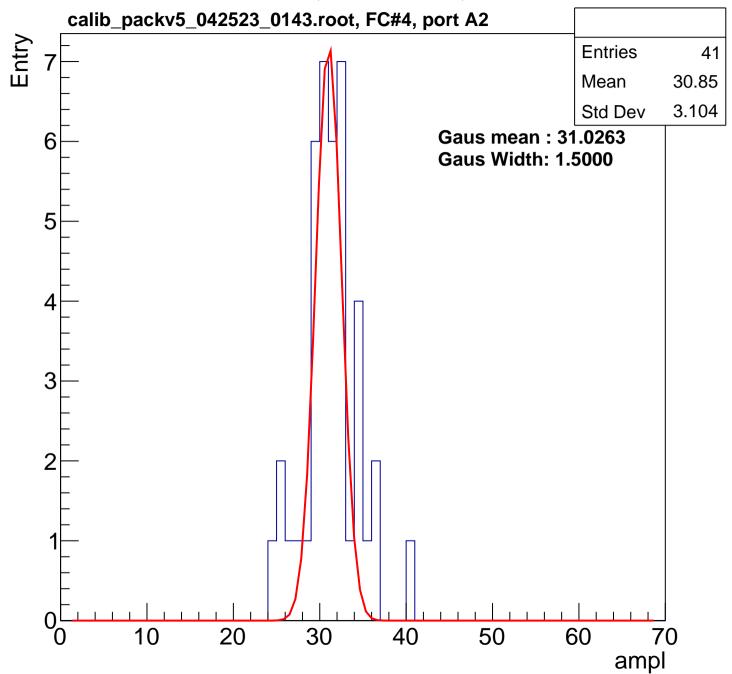


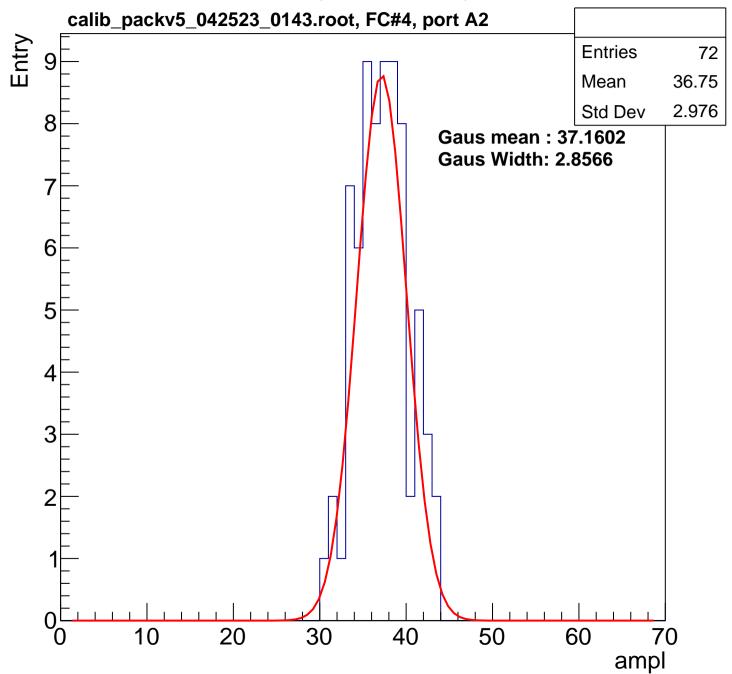


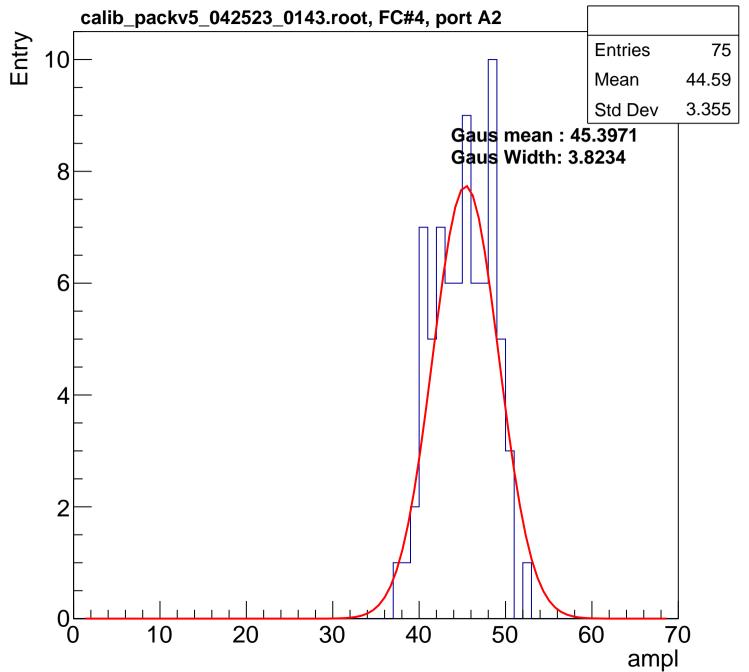


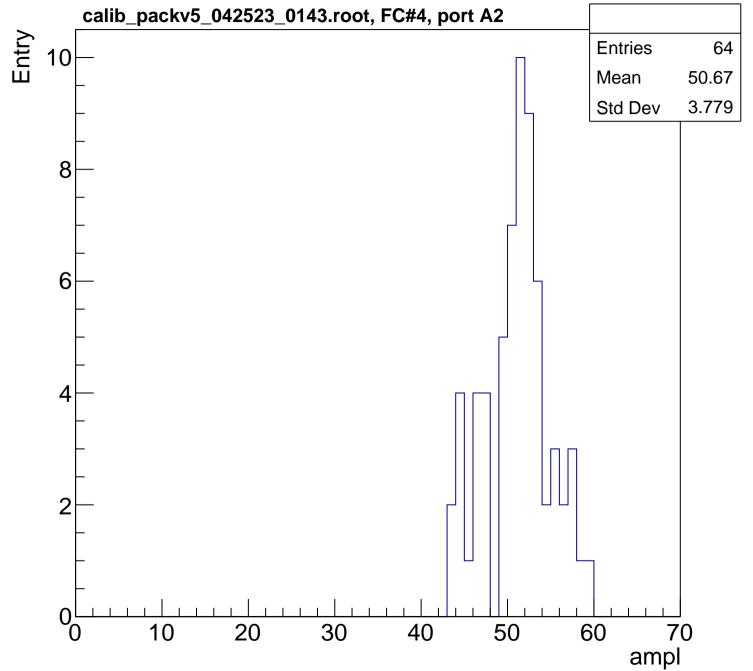
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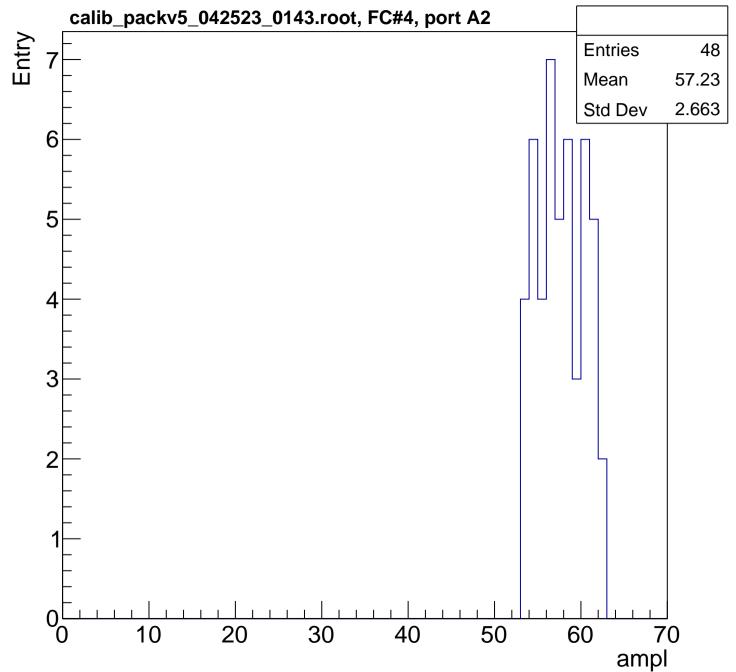


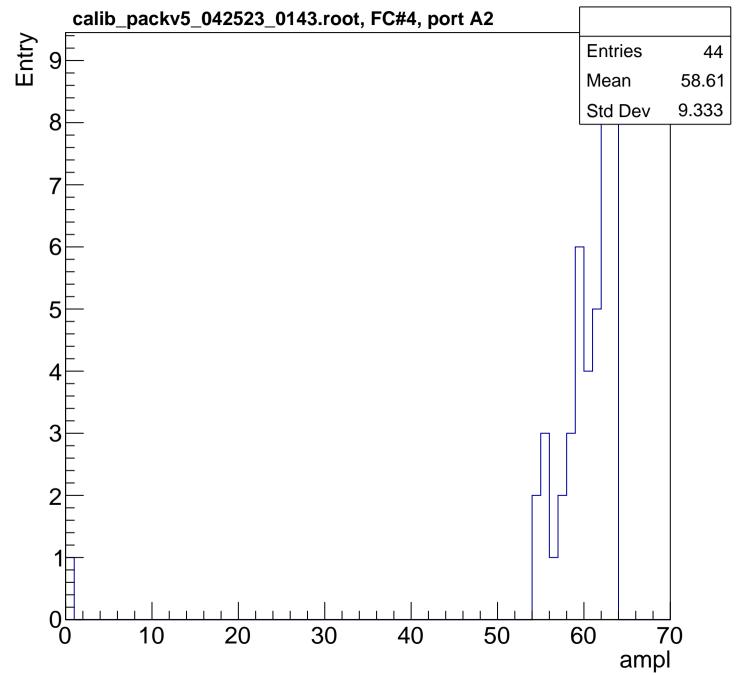


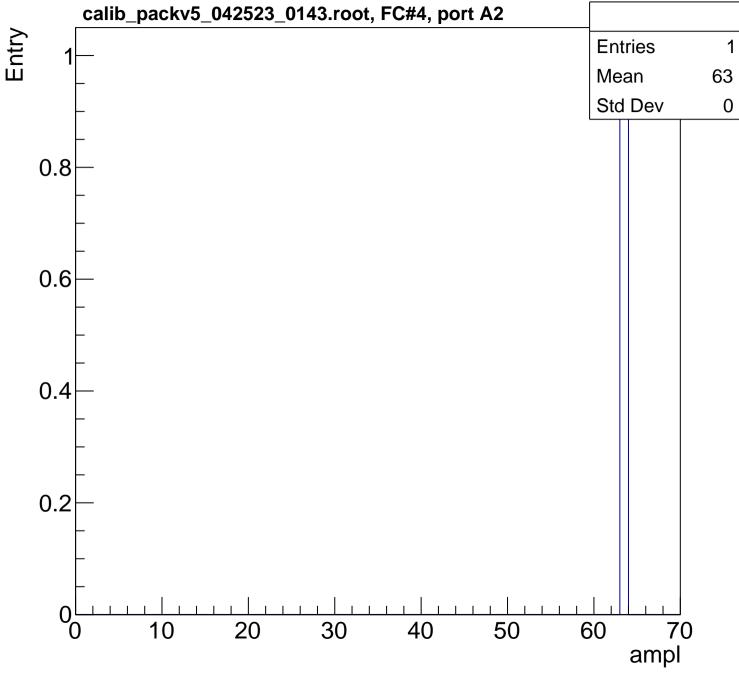




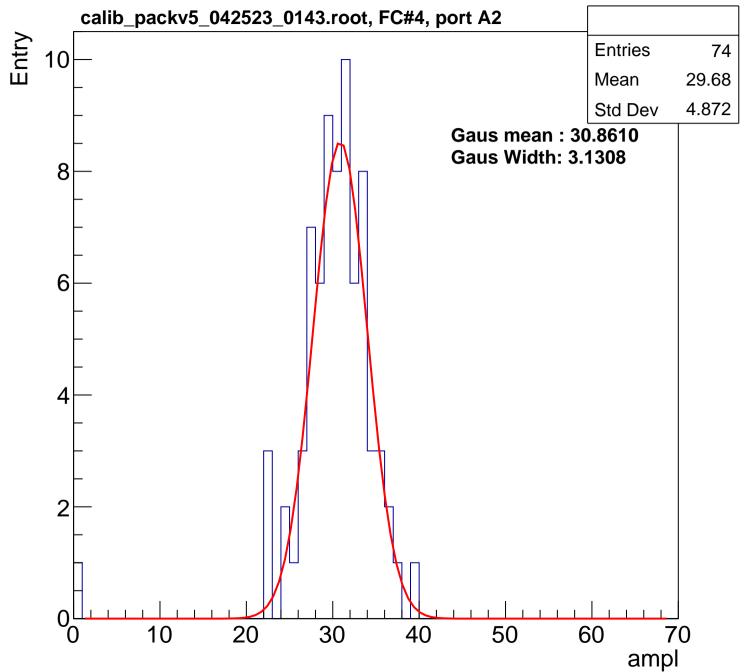


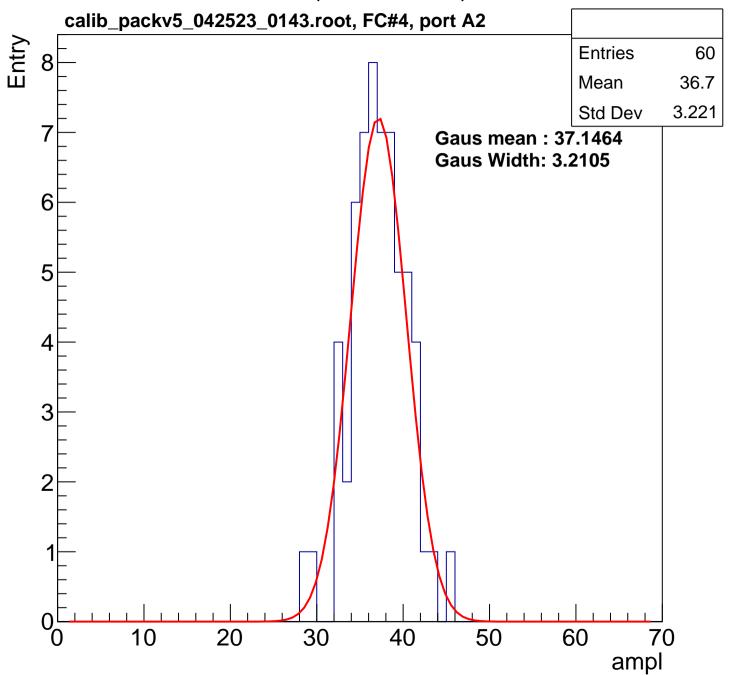


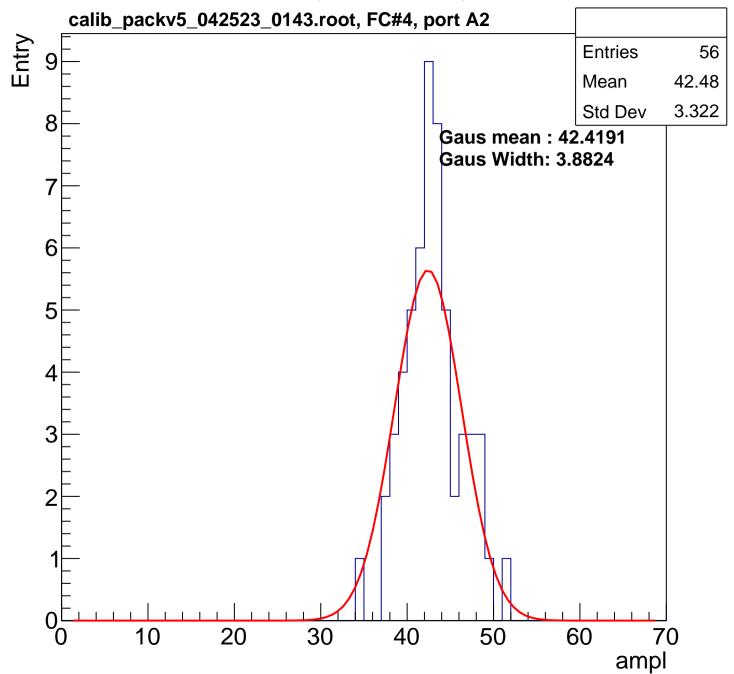


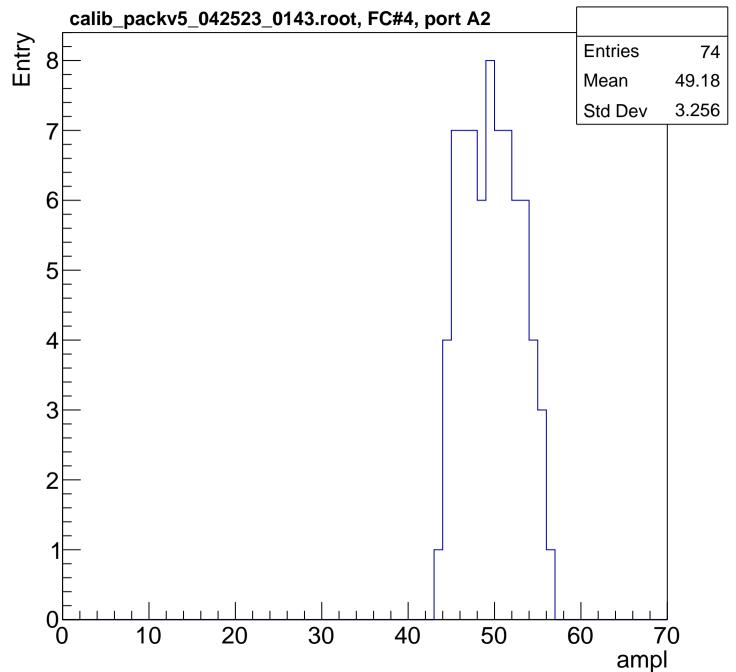


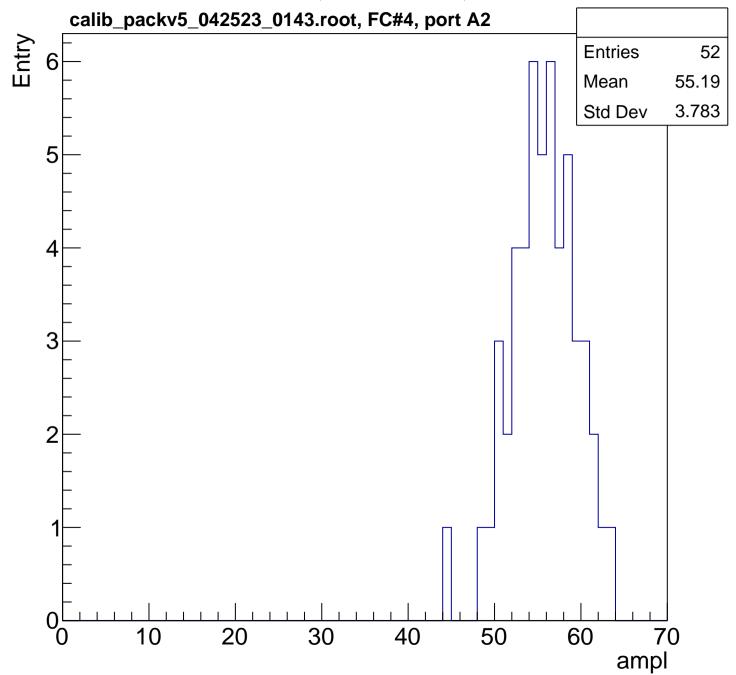


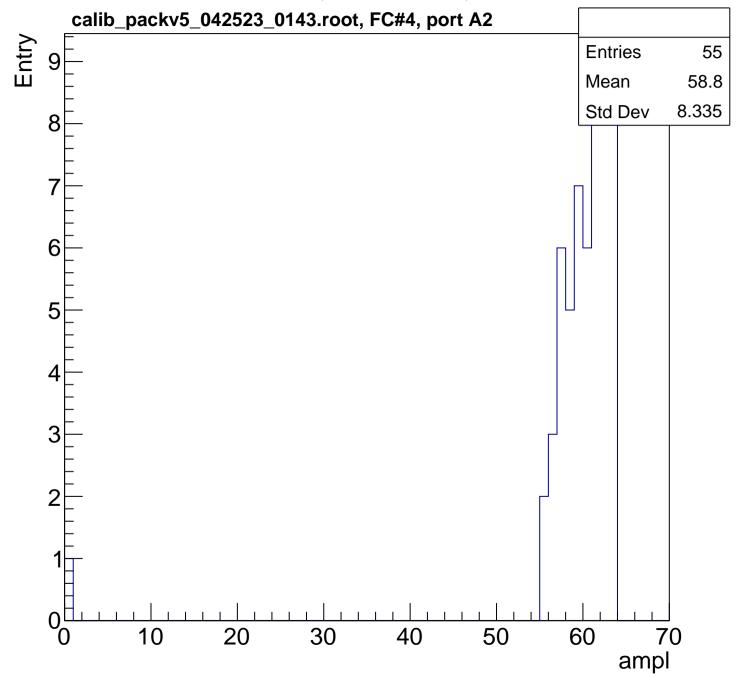


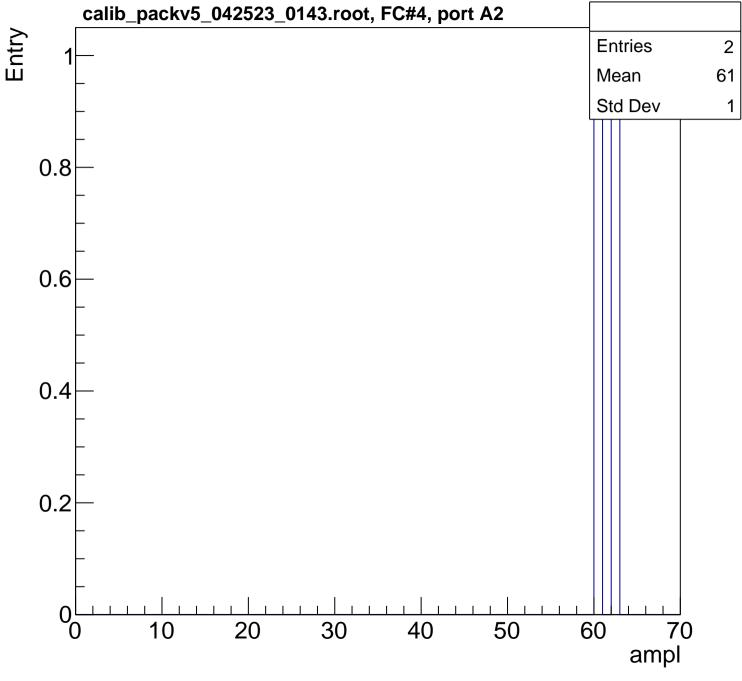




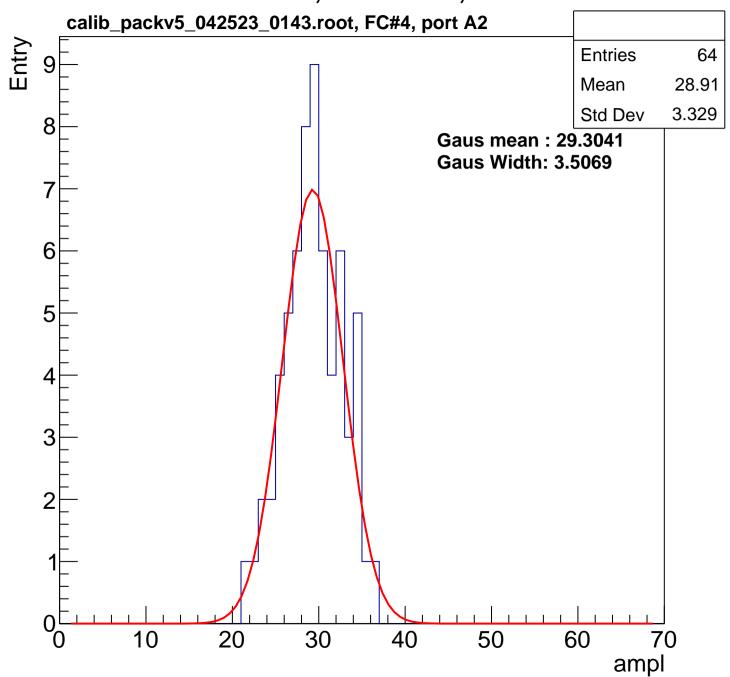


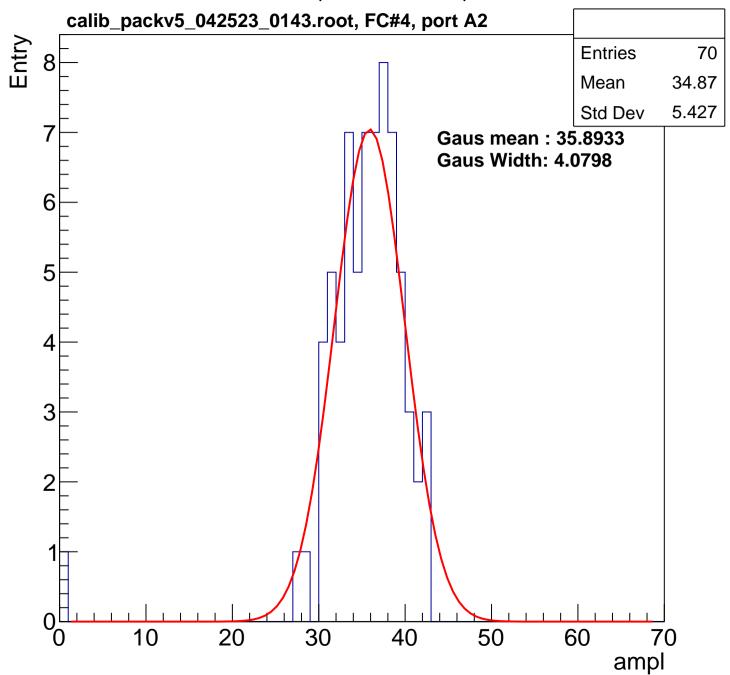


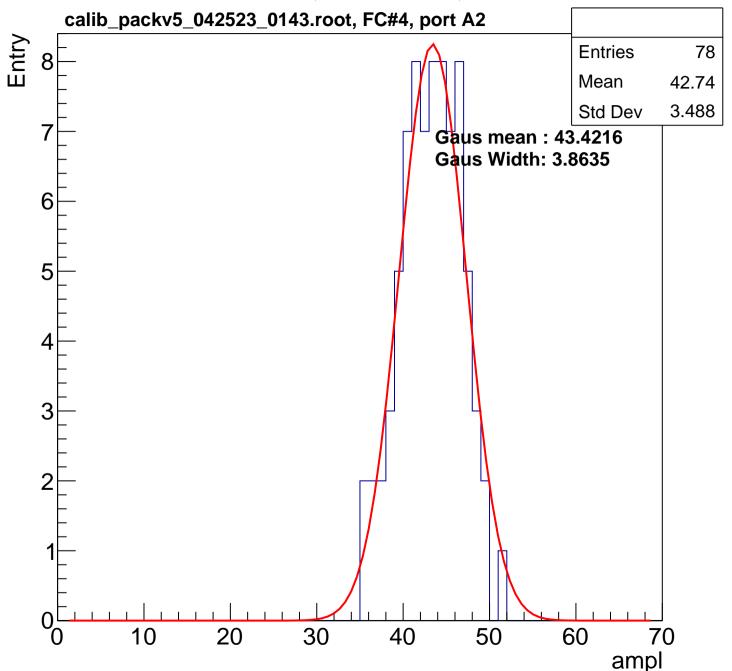


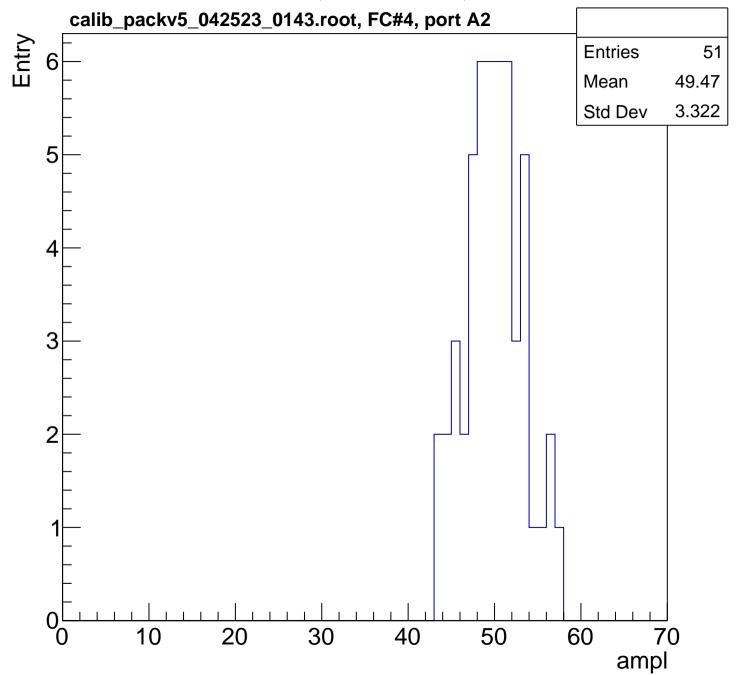


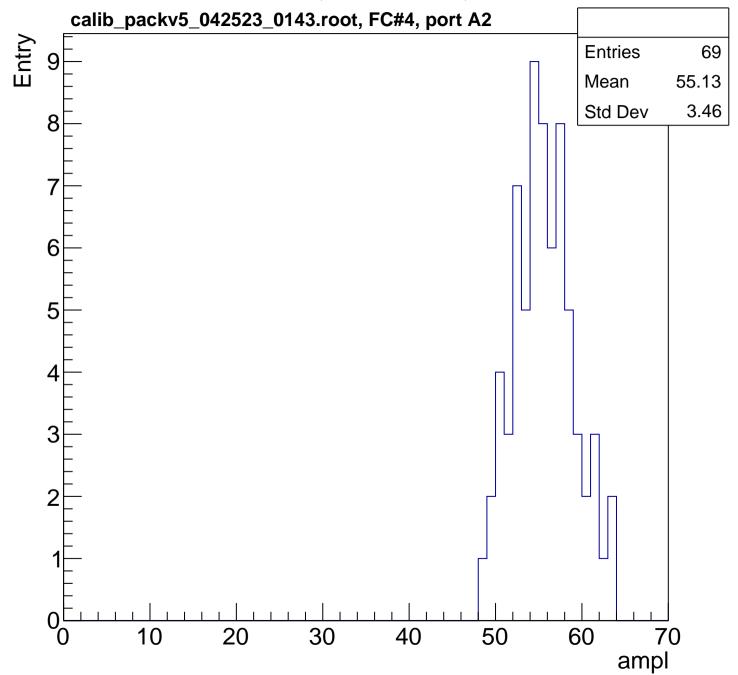
B1L100S, U8-ch40, adc7 calib_packv5_042523_0143.root, FC#4, port A2 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

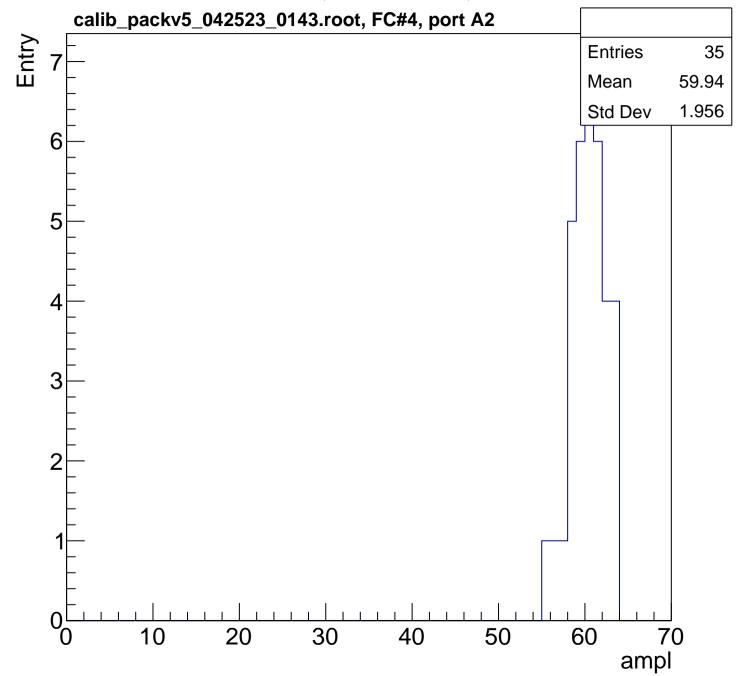


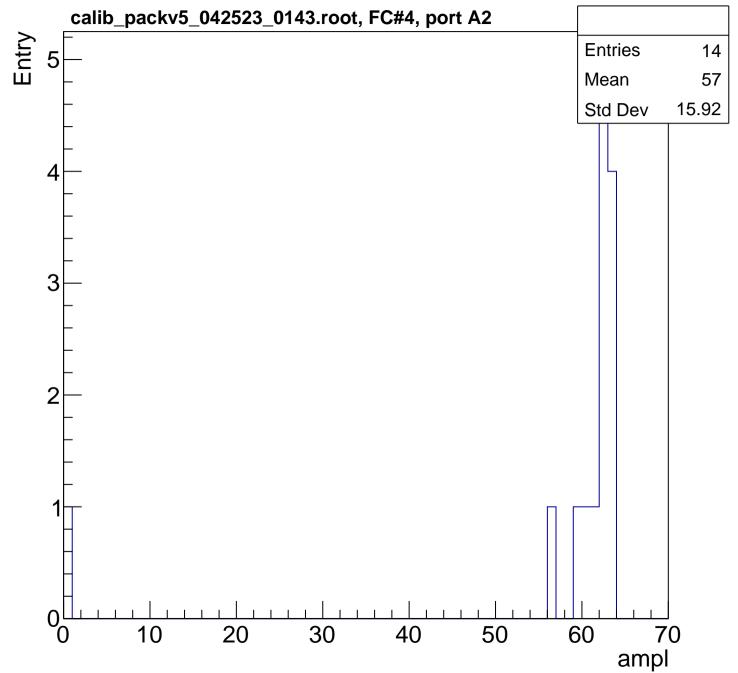




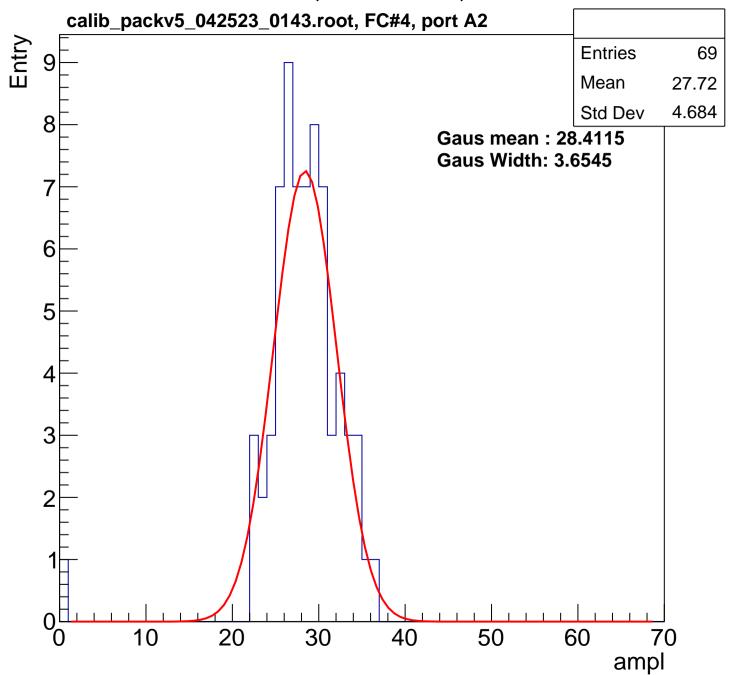


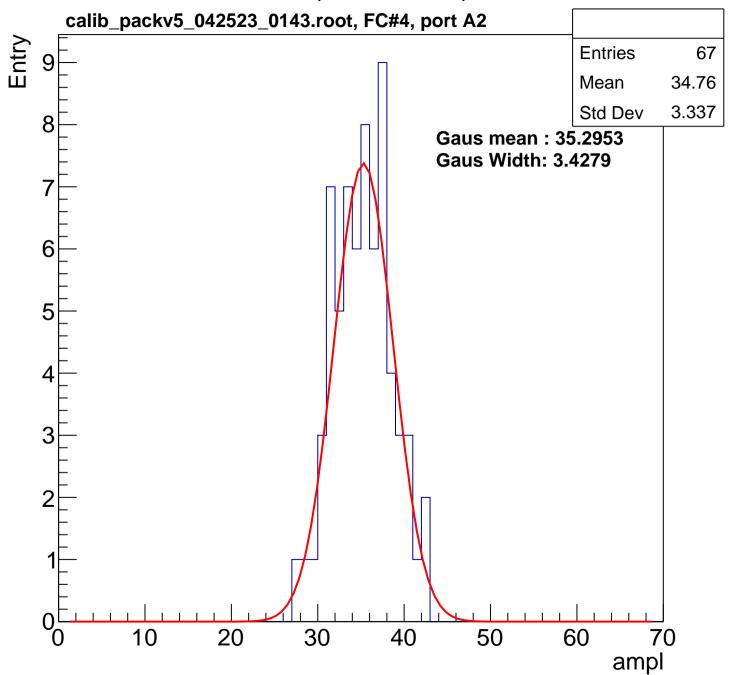


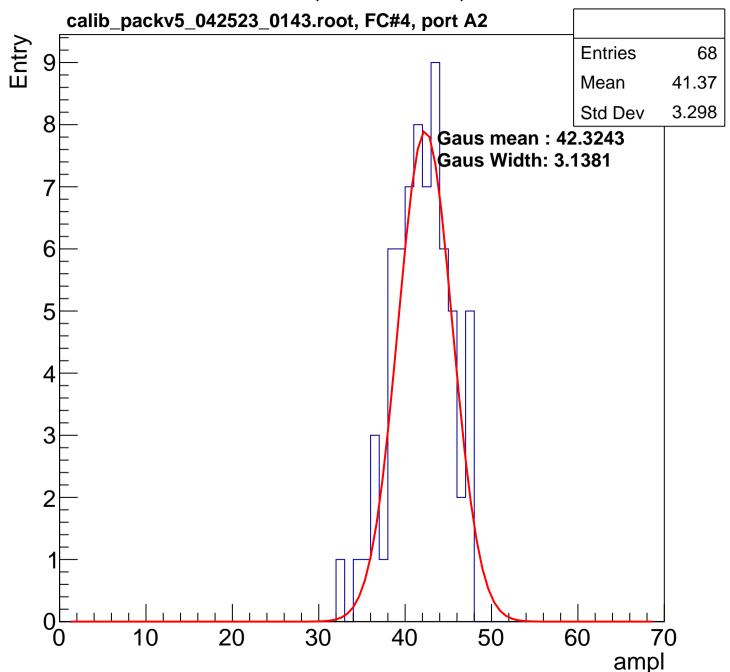


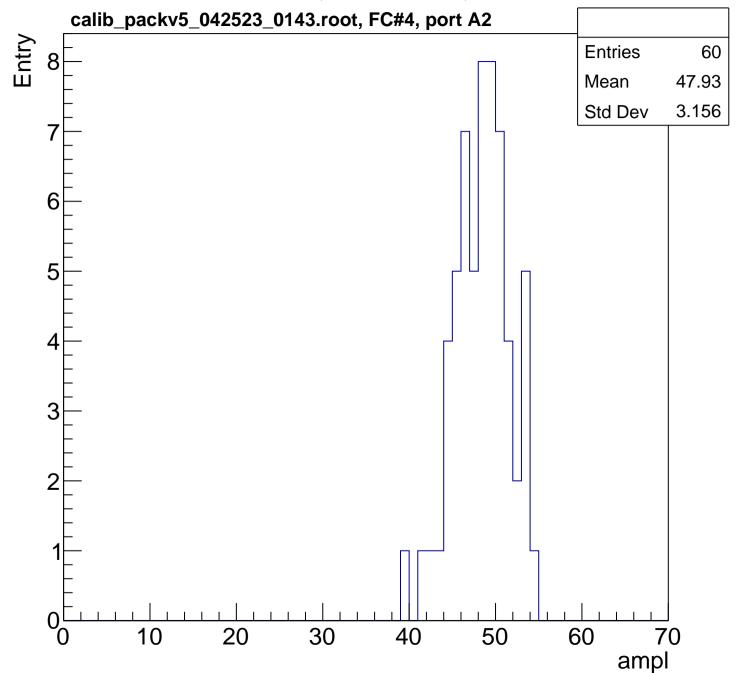


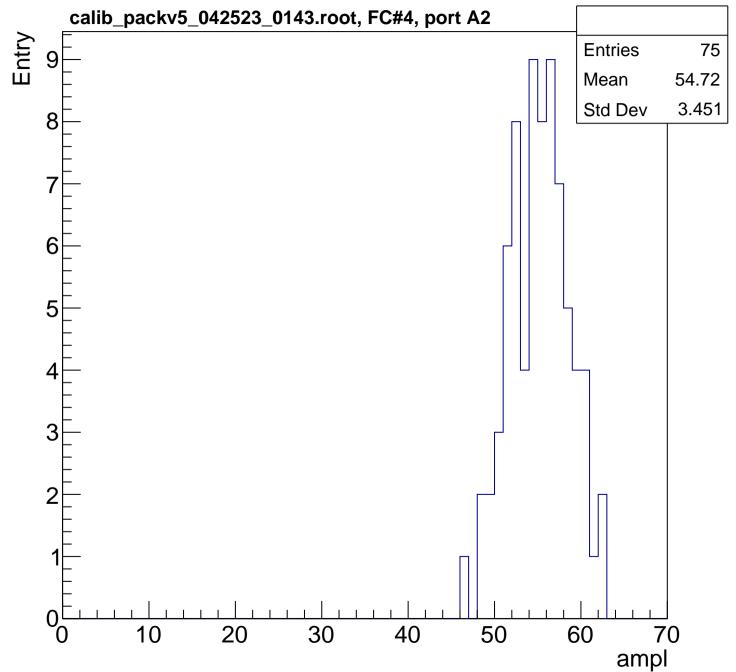
B1L100S, U8-ch41, adc7 calib_packv5_042523_0143.root, FC#4, port A2 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

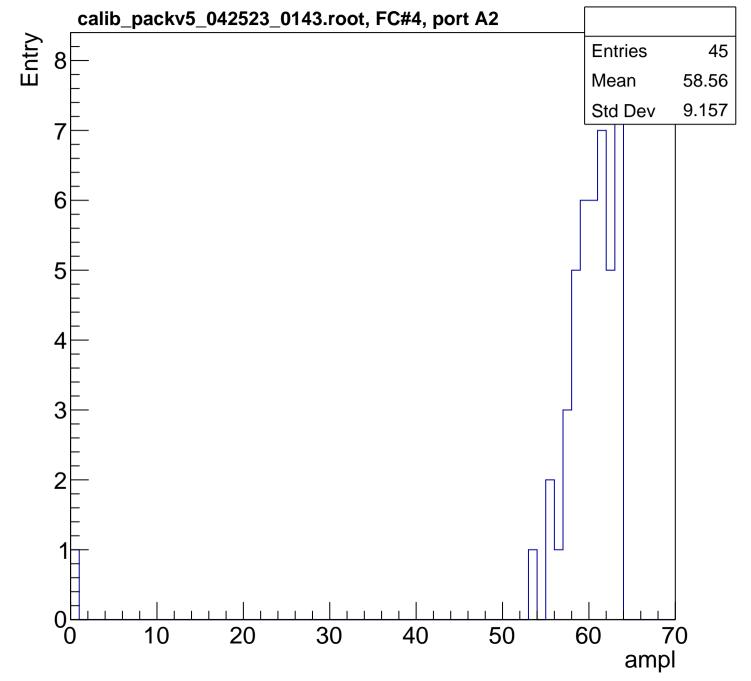


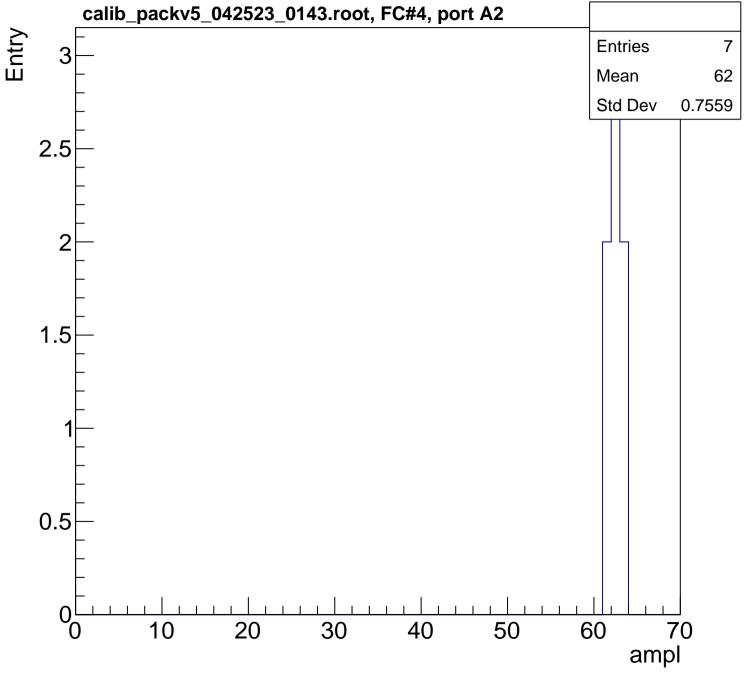




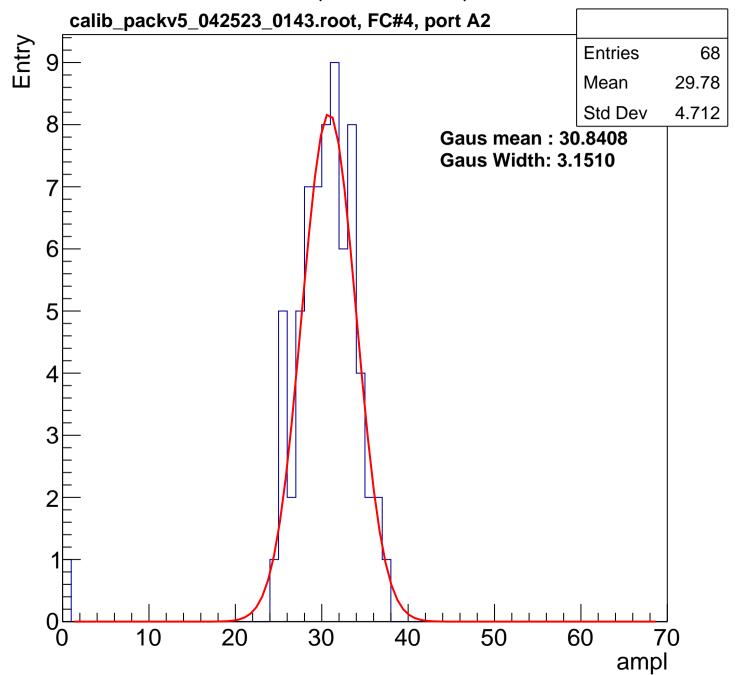


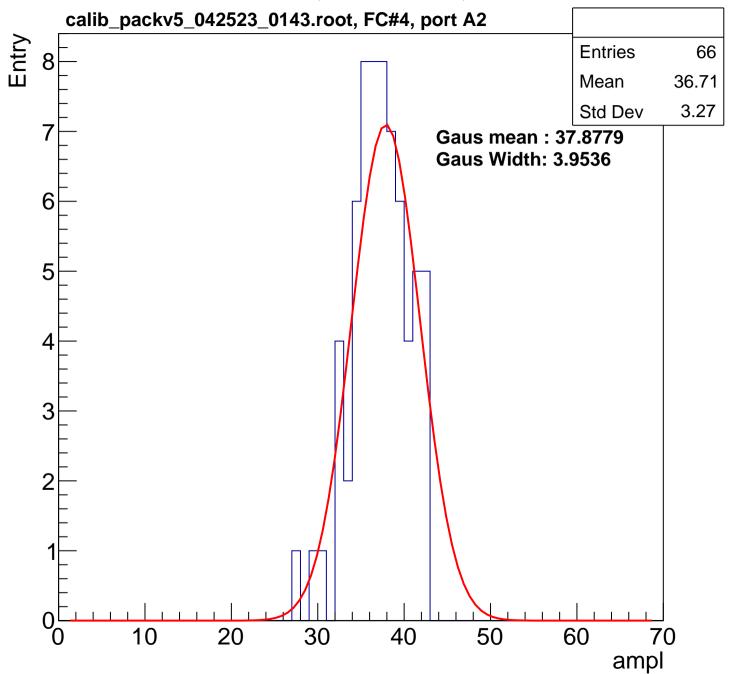


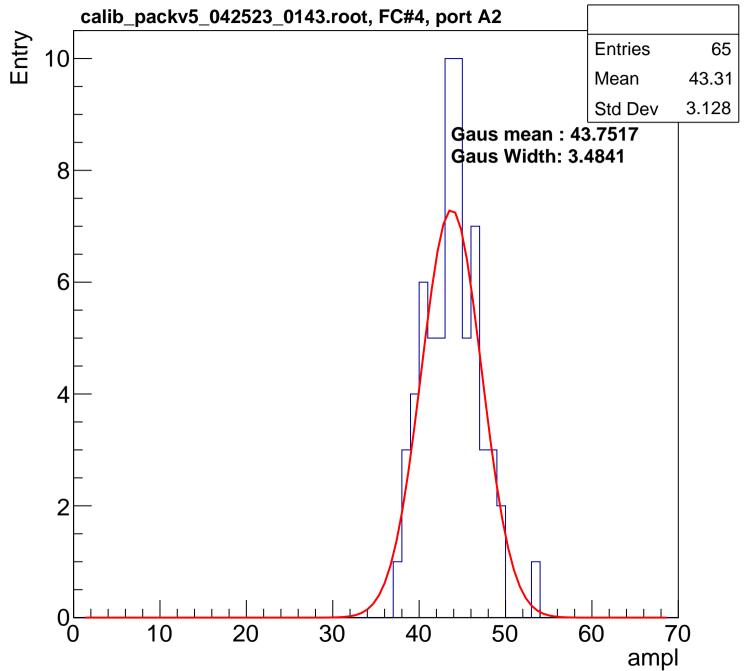


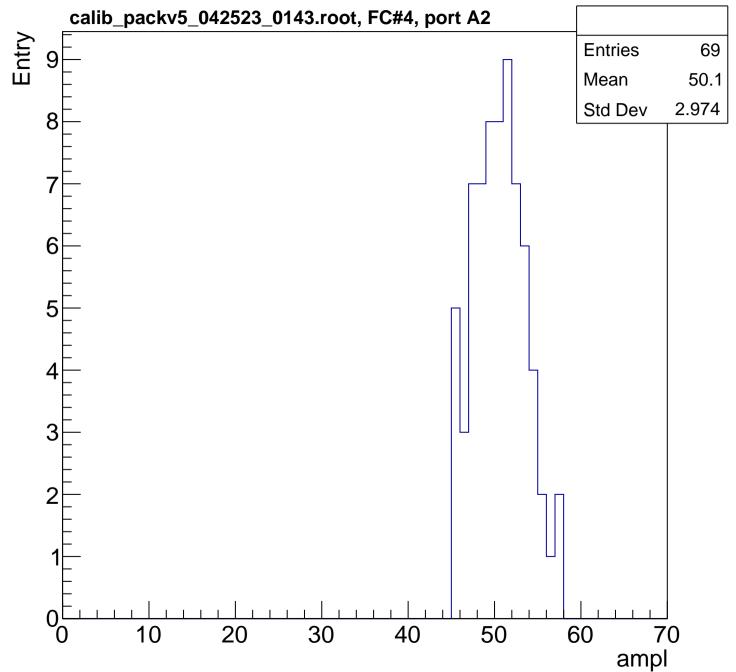


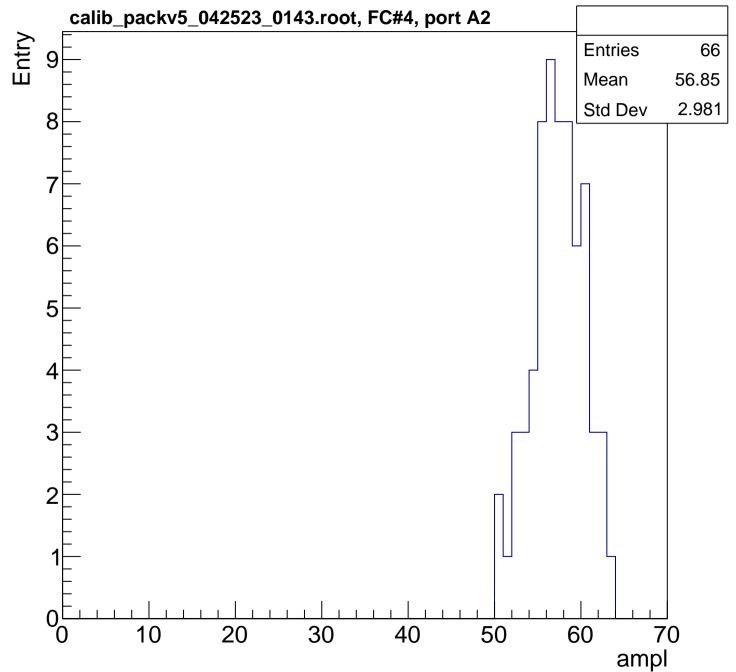
B1L100S, U8-ch42, adc7 calib_packv5_042523_0143.root, FC#4, port A2 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

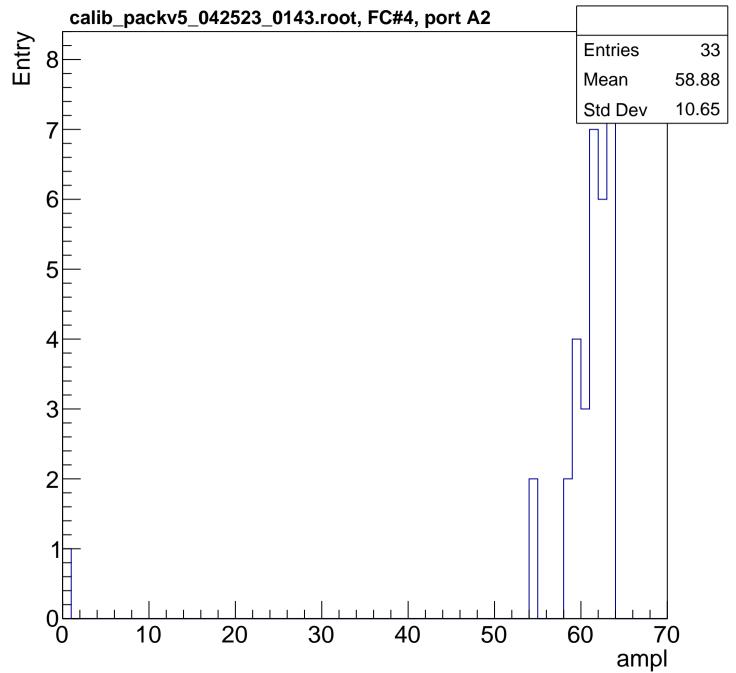


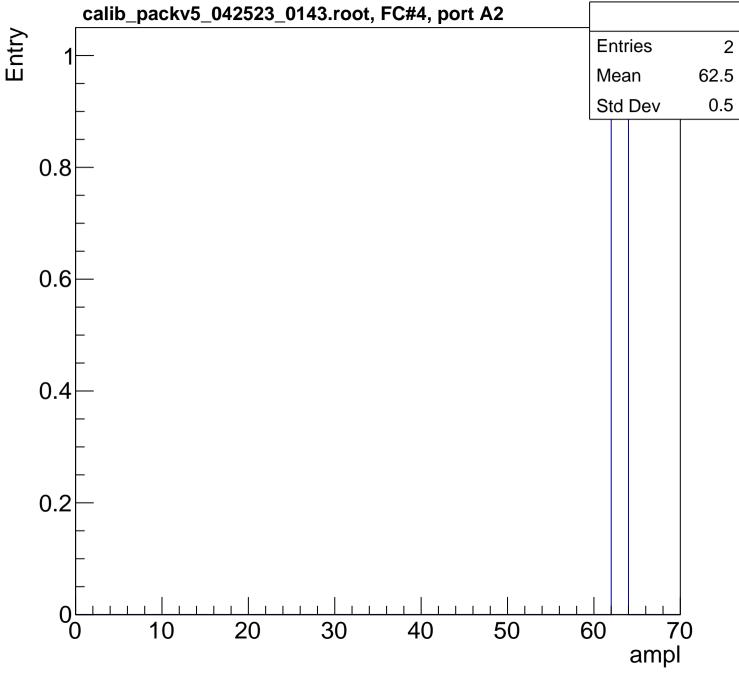


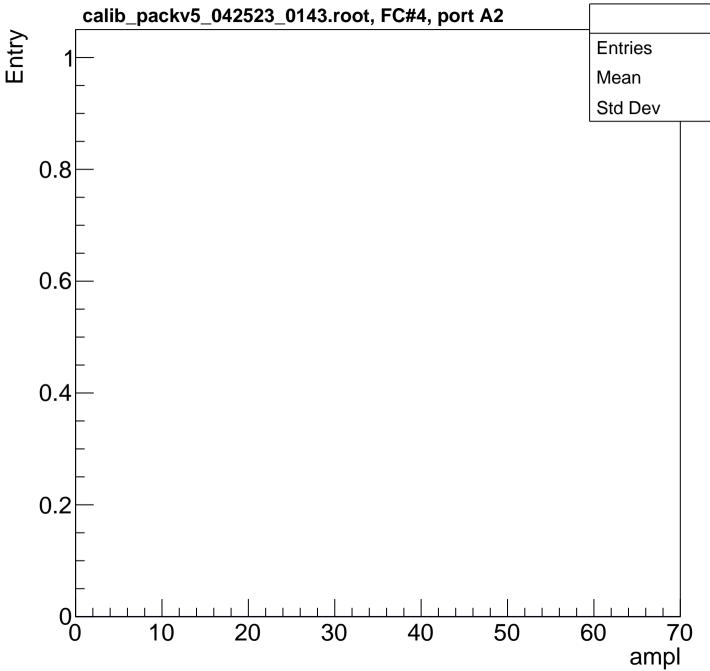


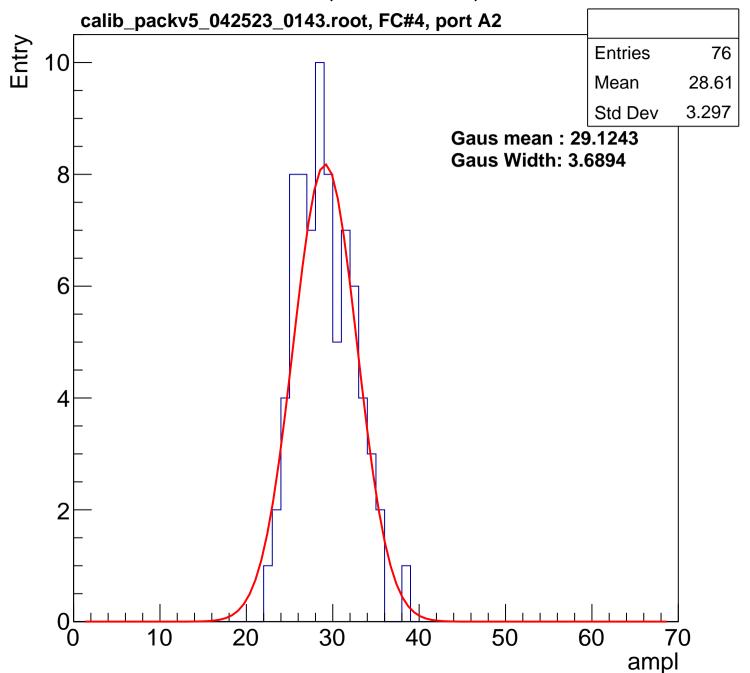


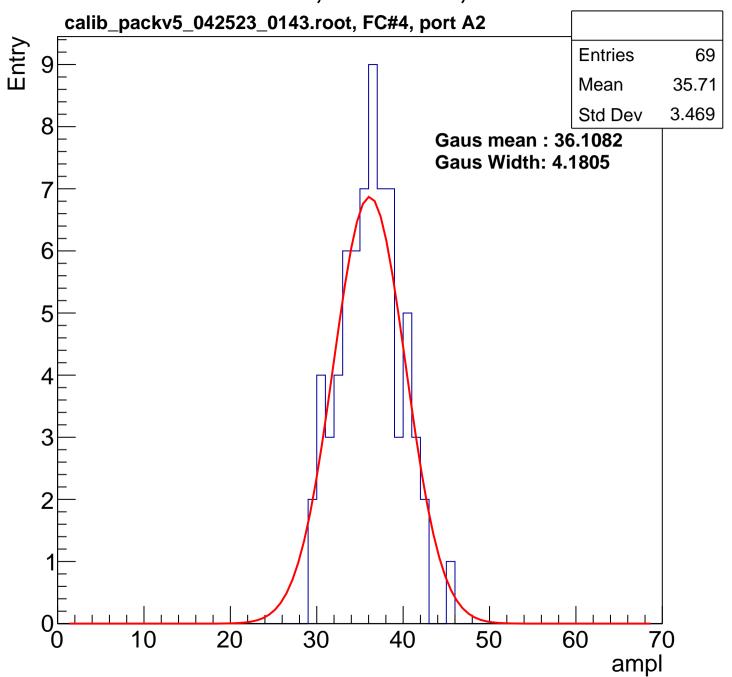


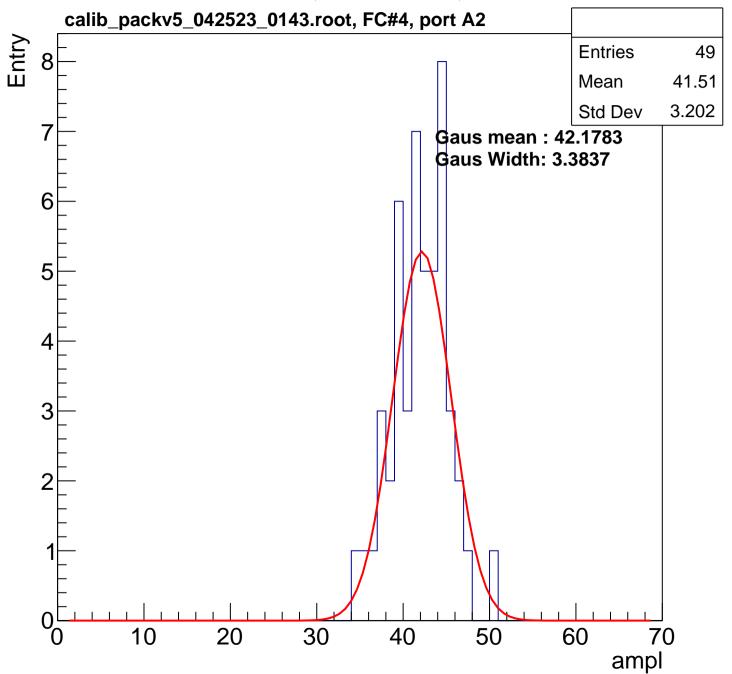


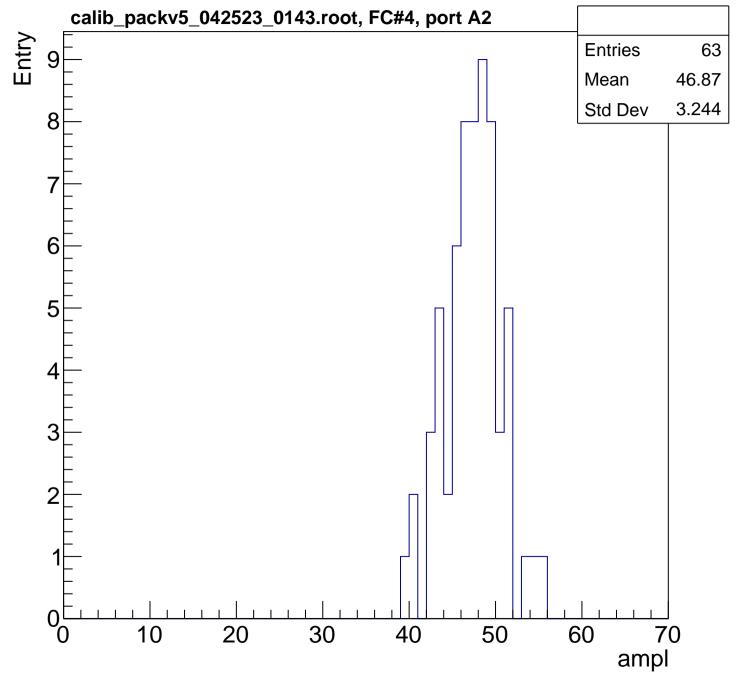


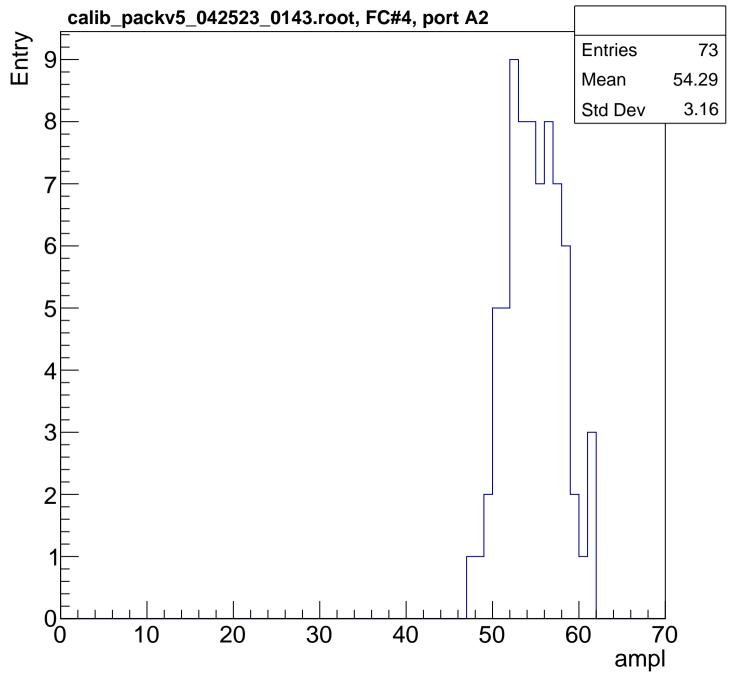


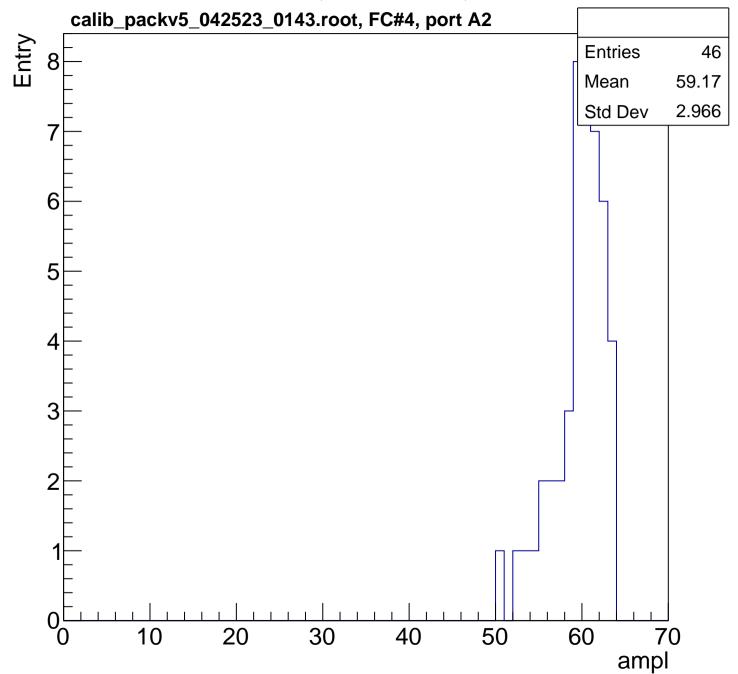


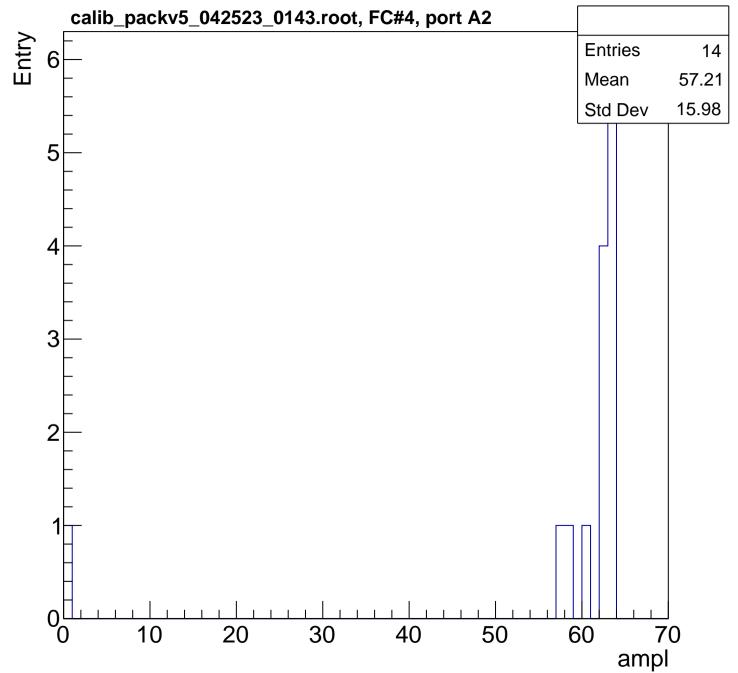


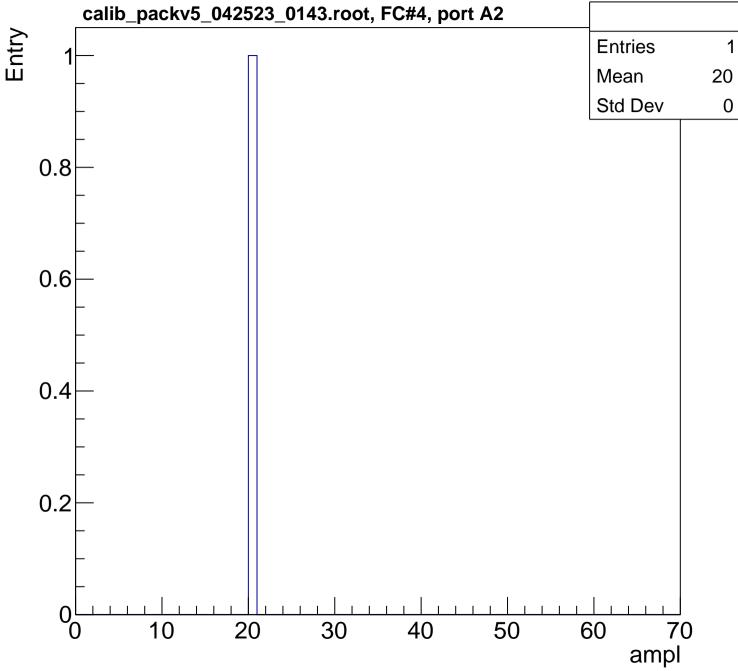


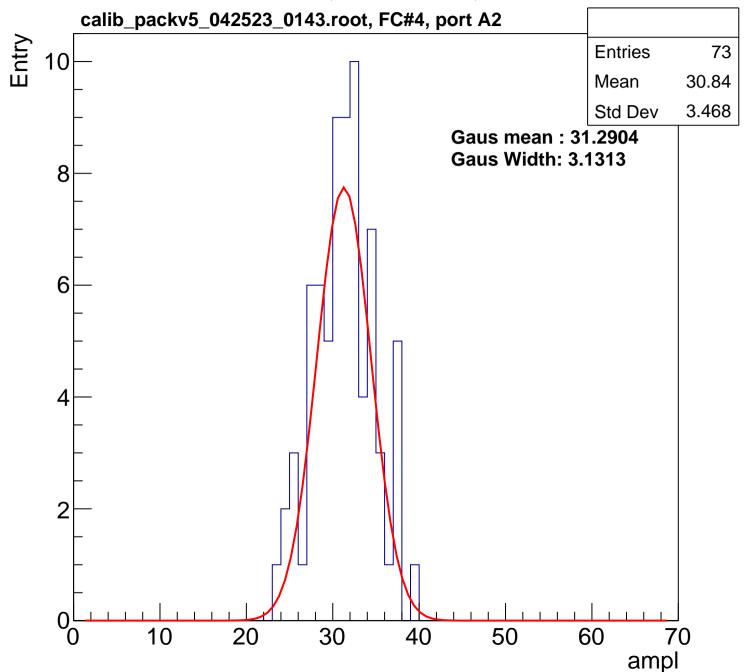


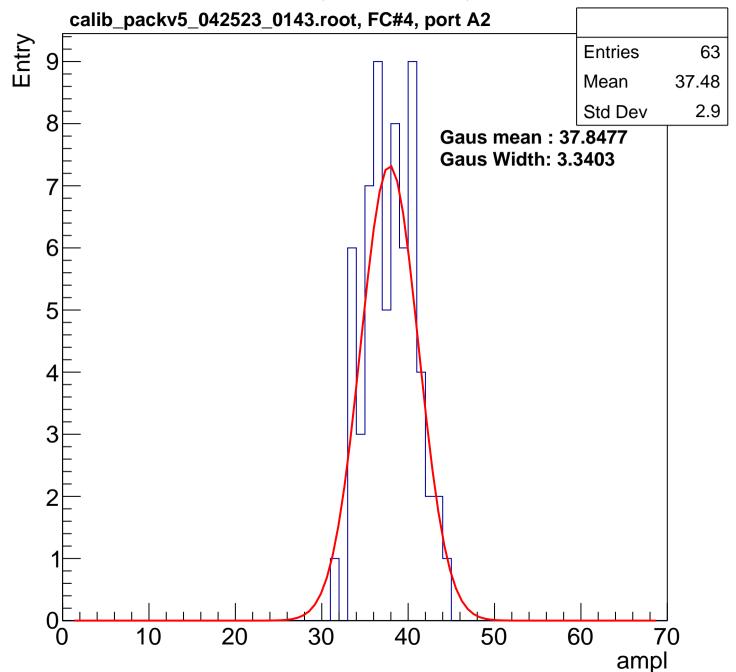


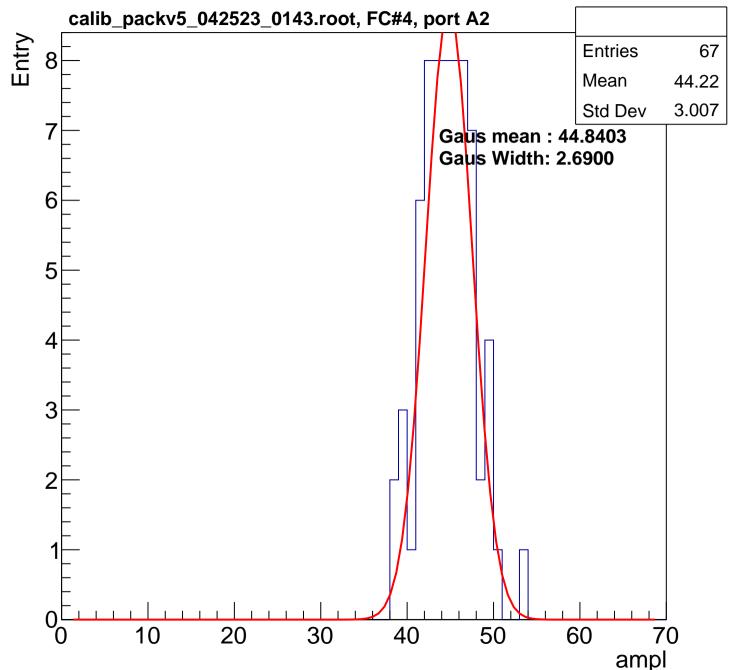


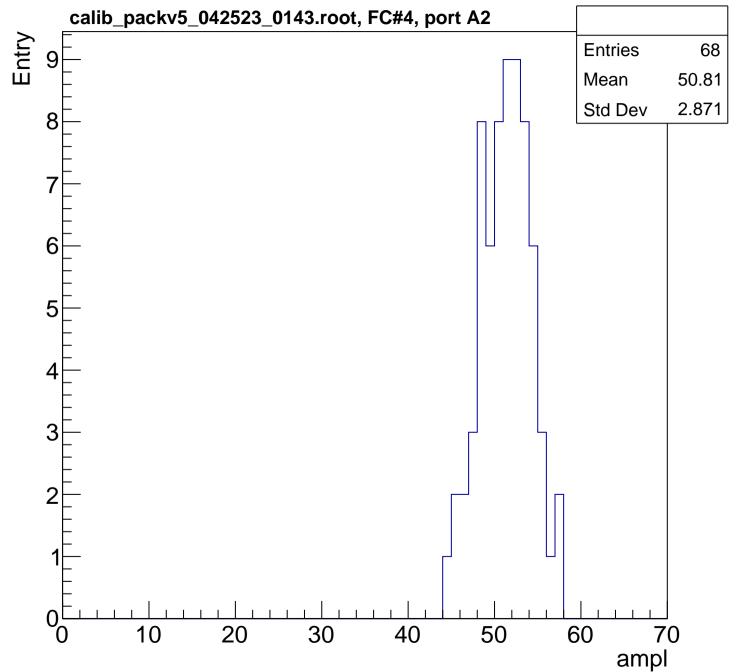


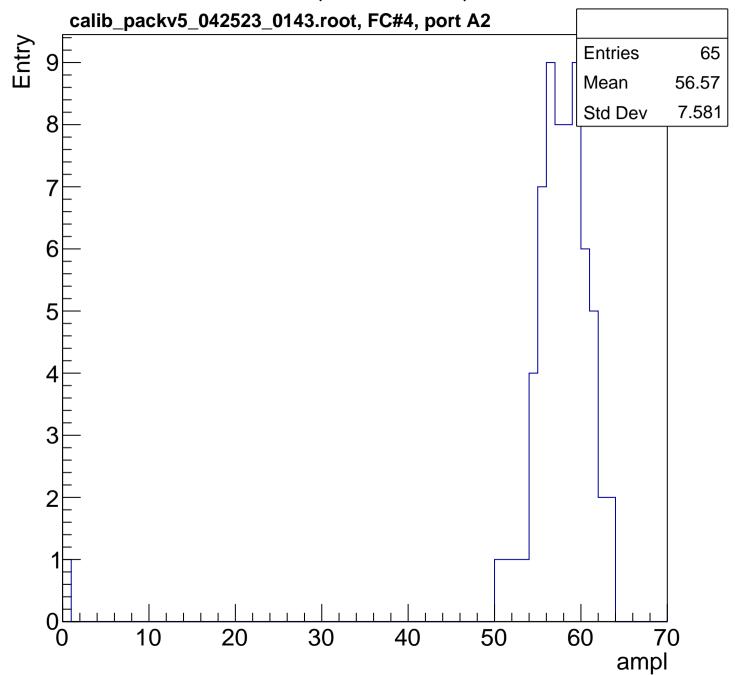


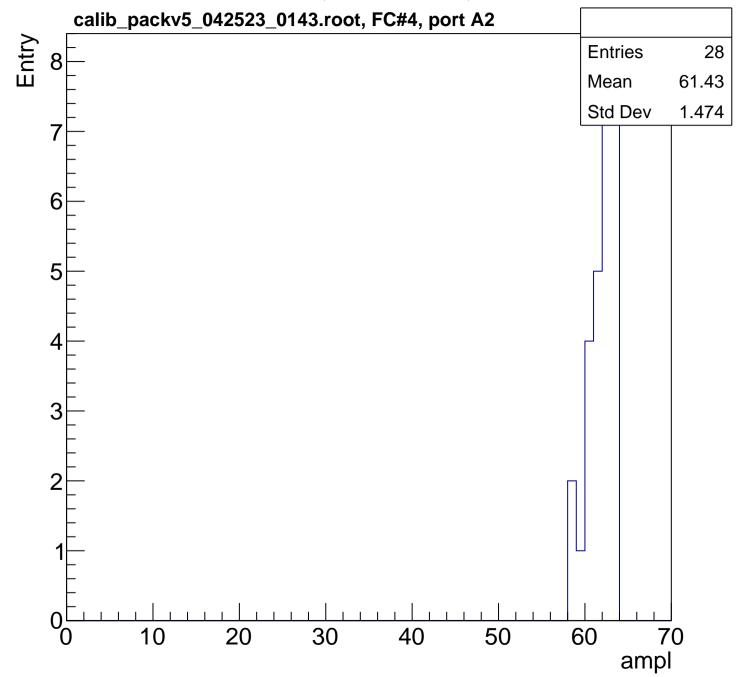


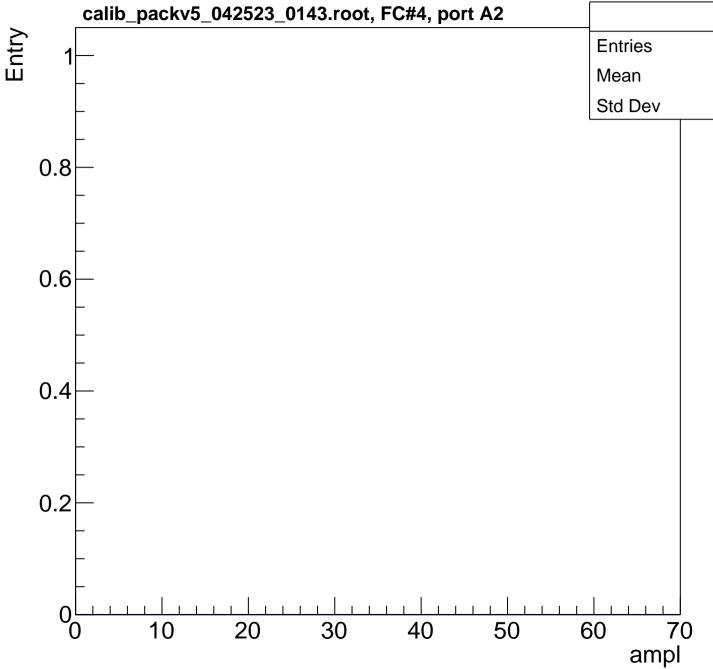




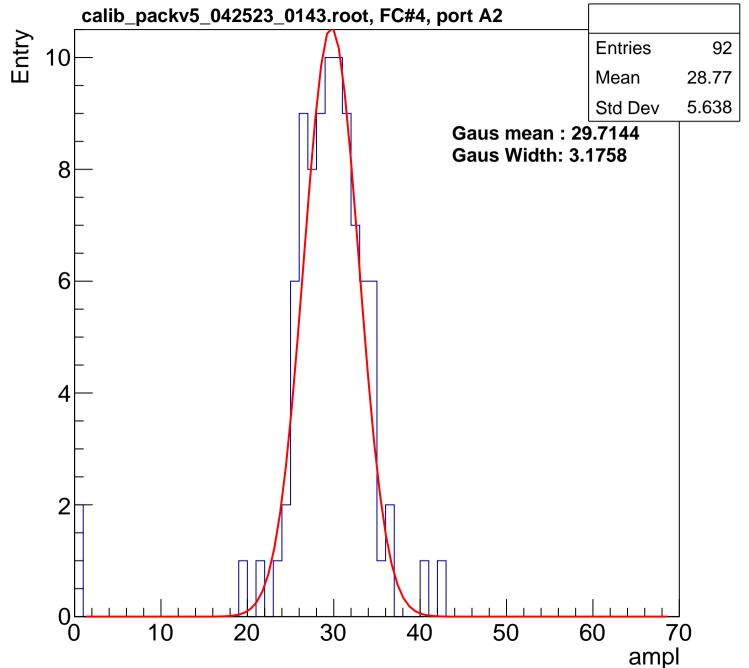


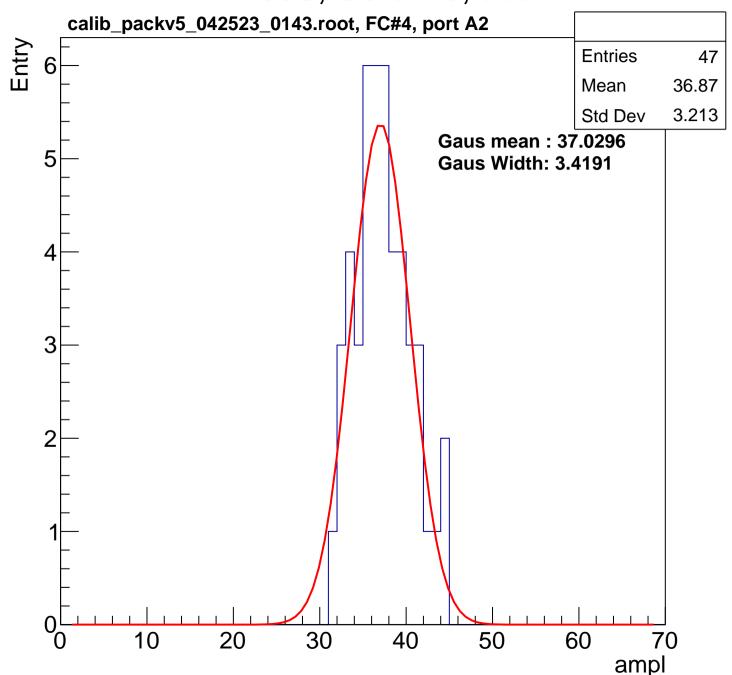


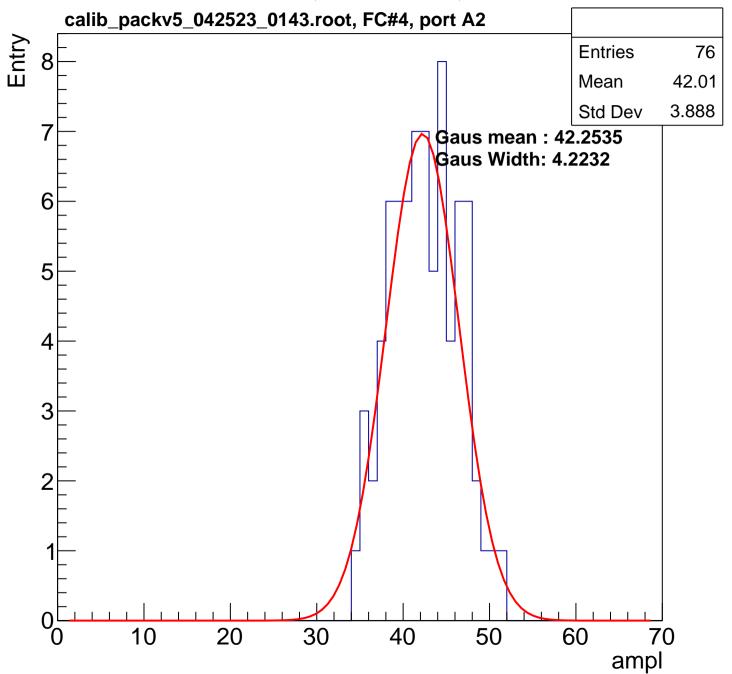


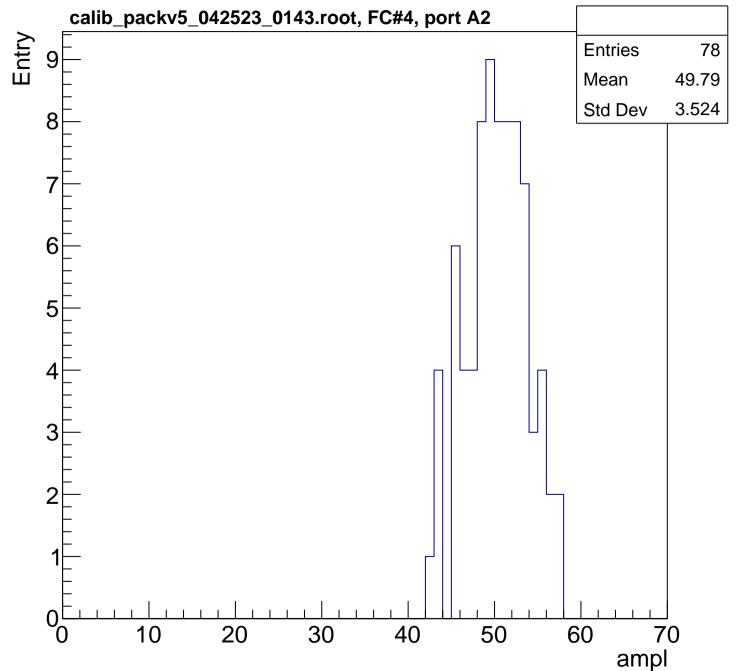


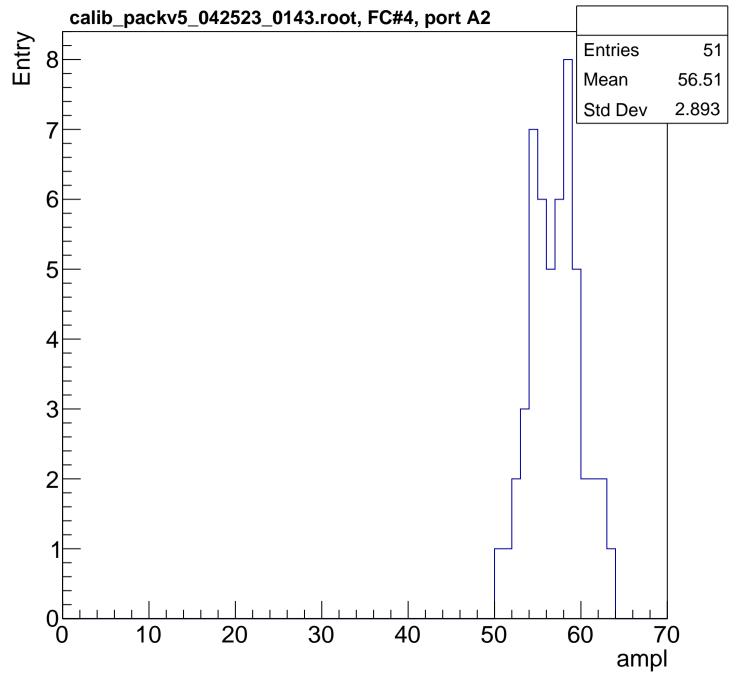


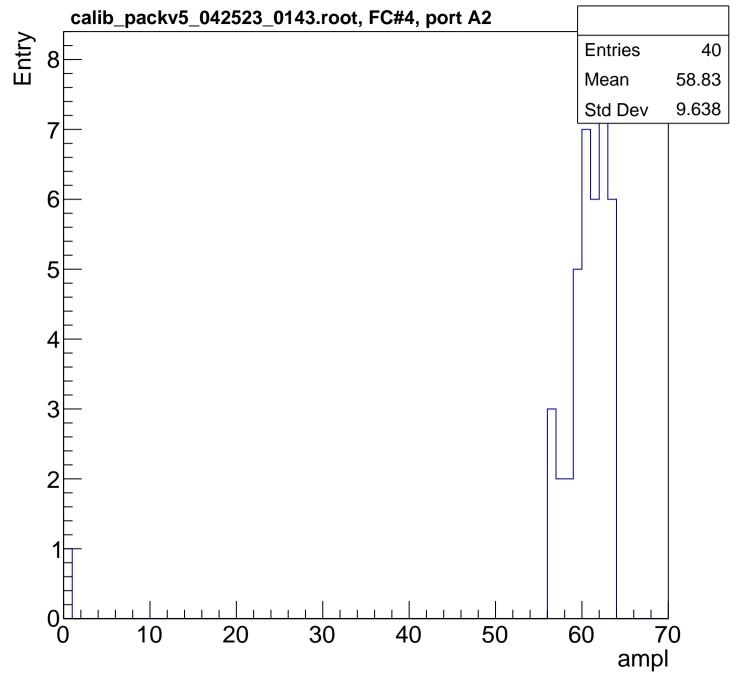


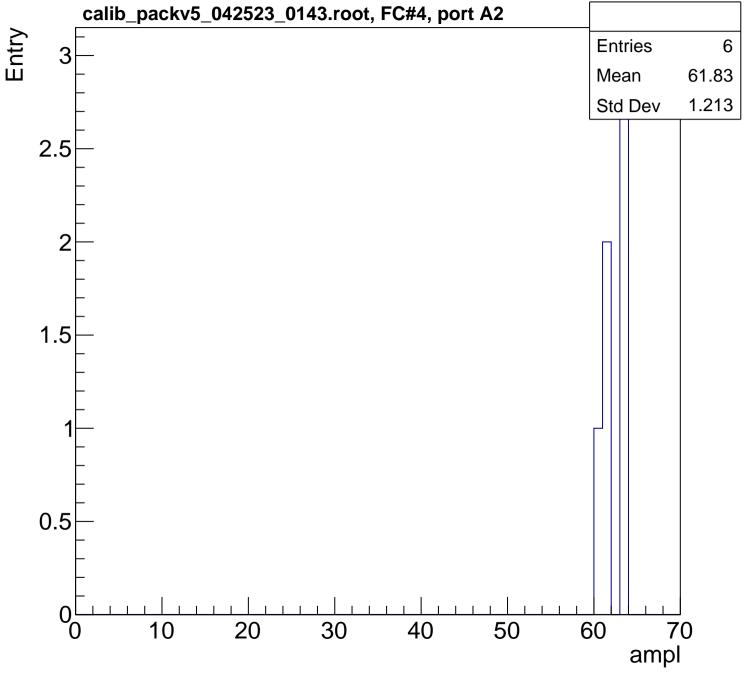




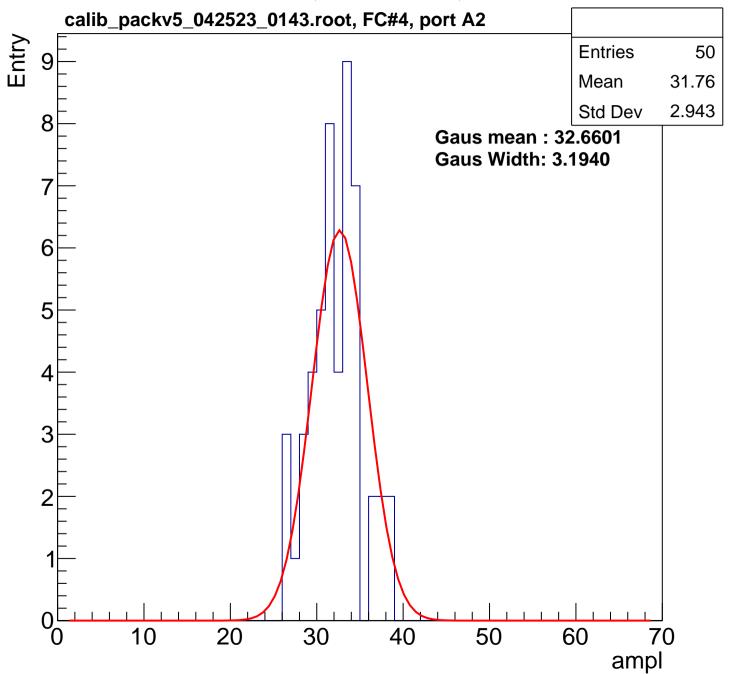


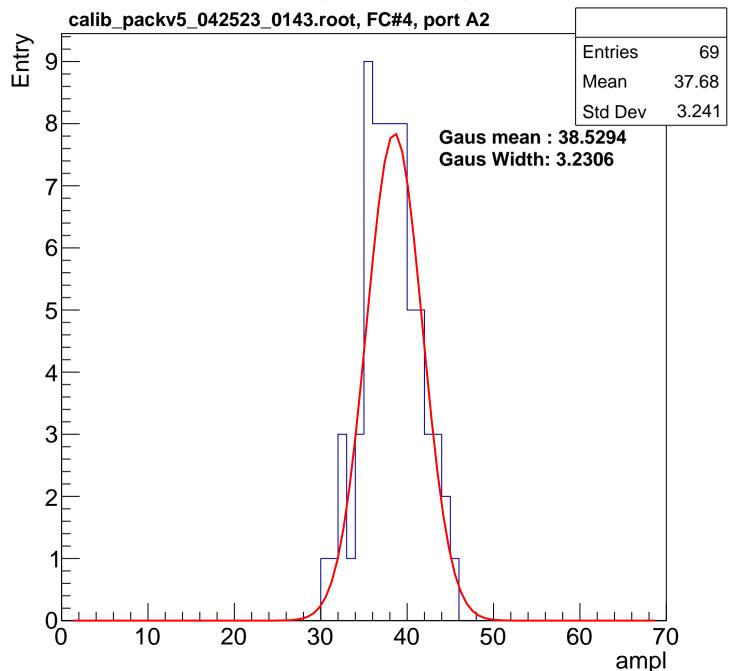


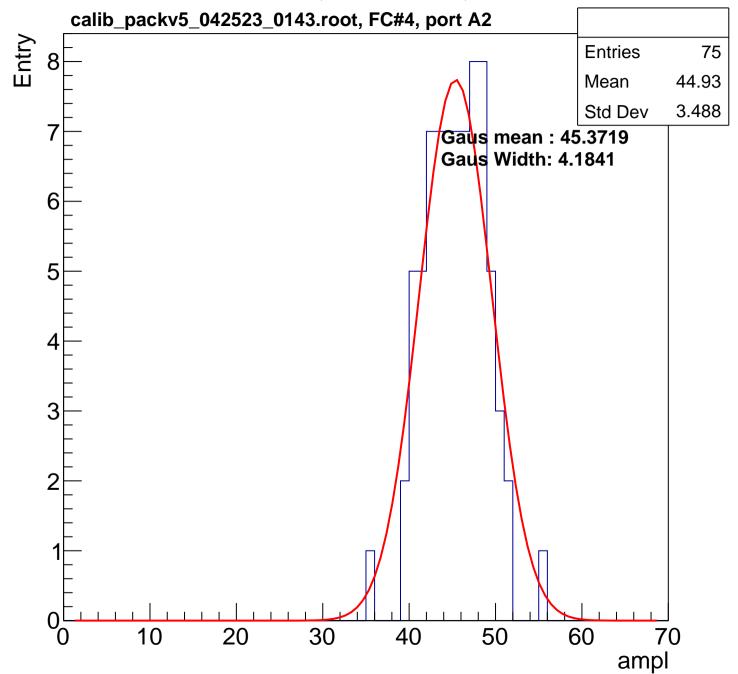


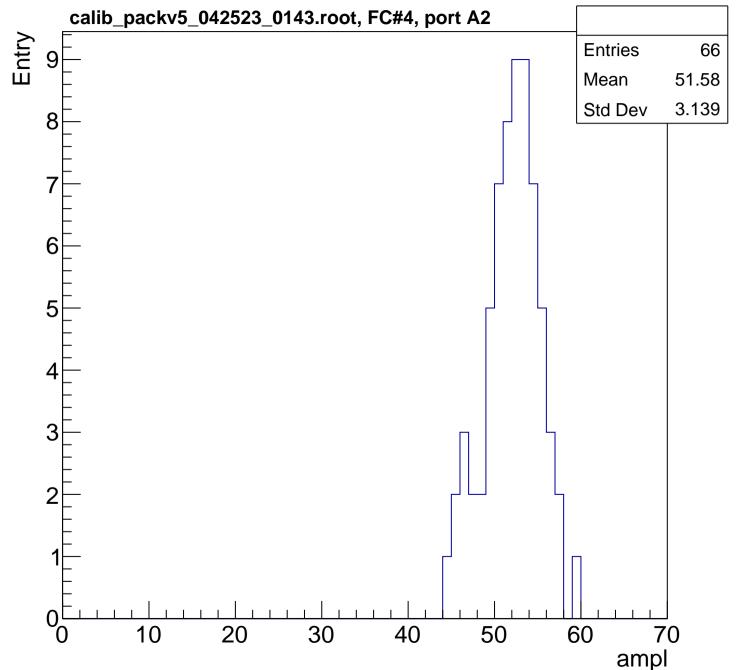


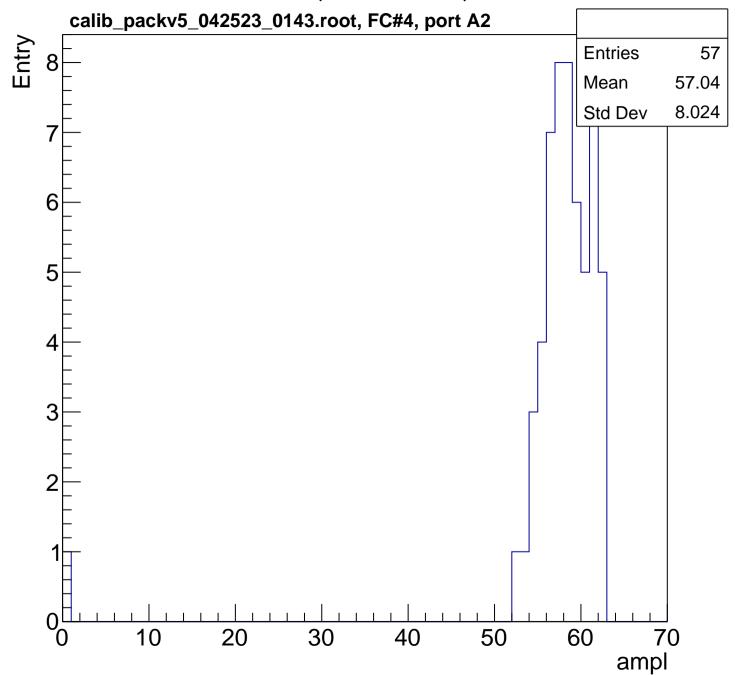
B1L100S, U8-ch46, adc7 calib_packv5_042523_0143.root, FC#4, port A2 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

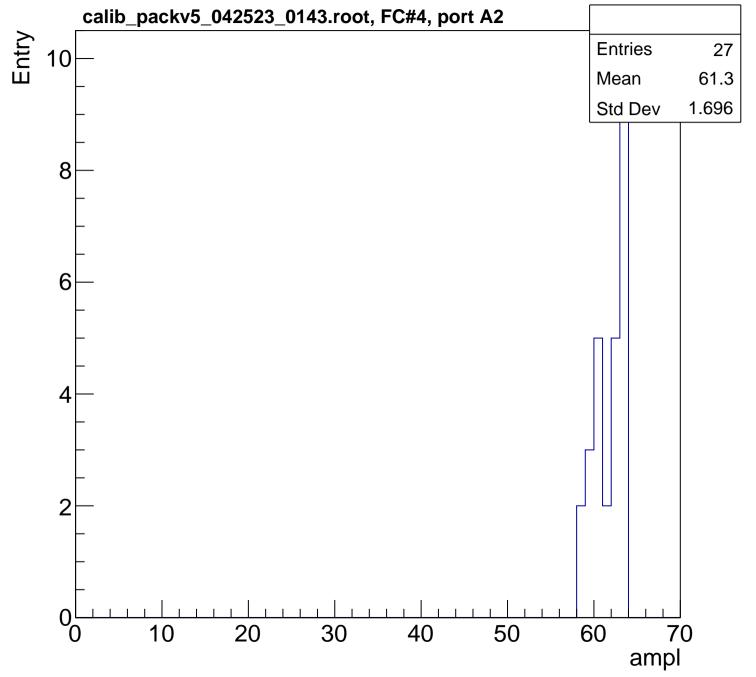


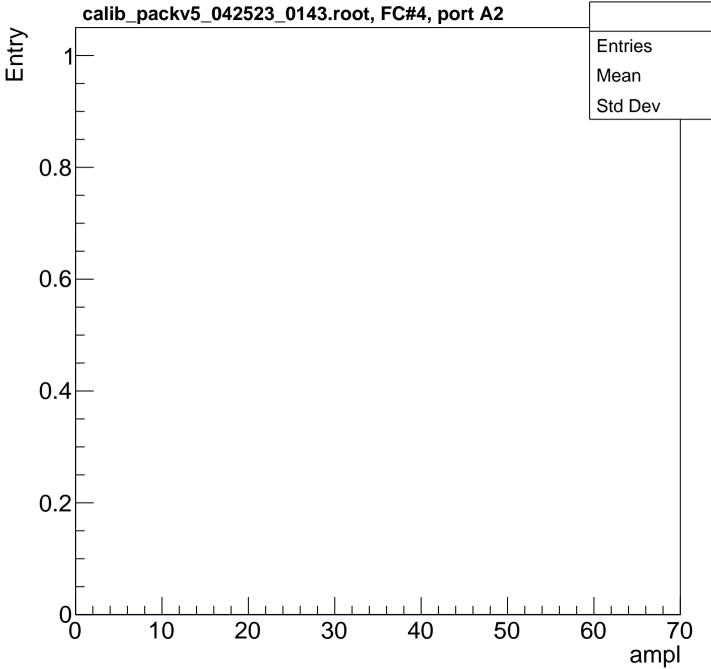


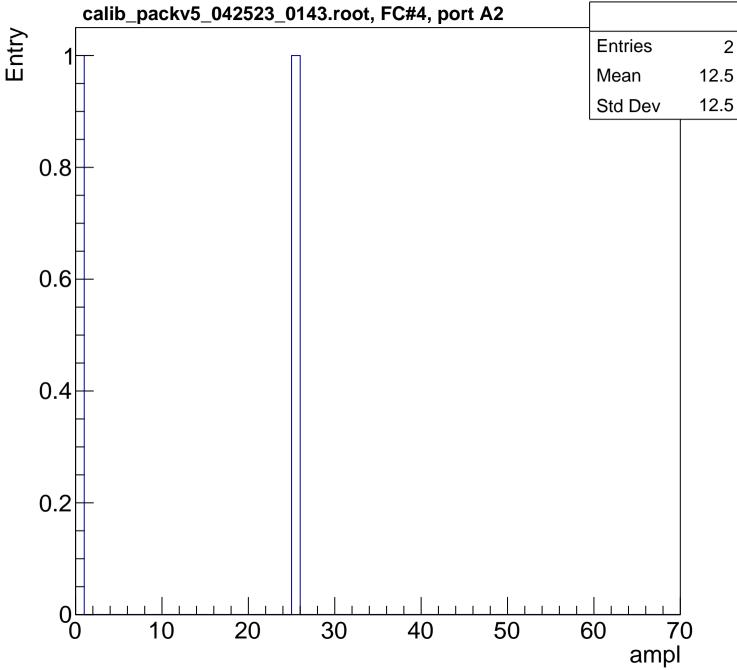


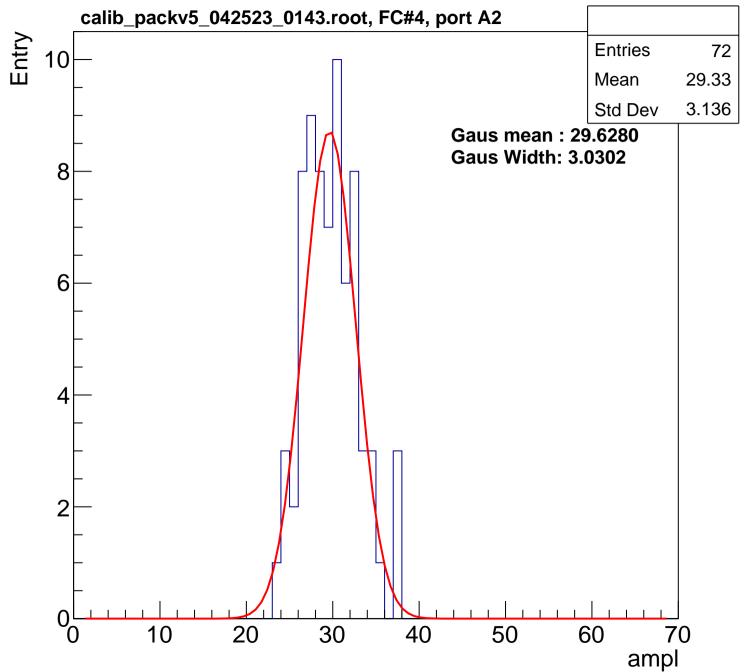


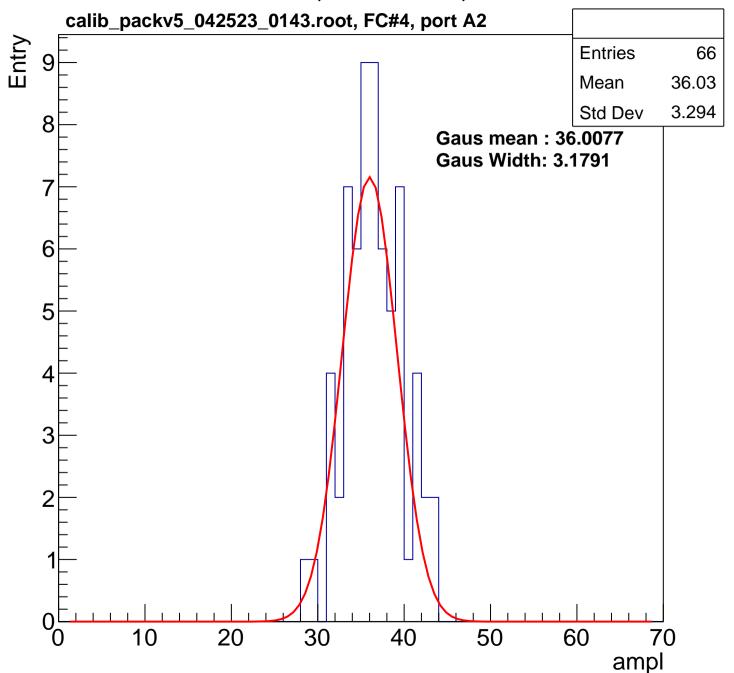


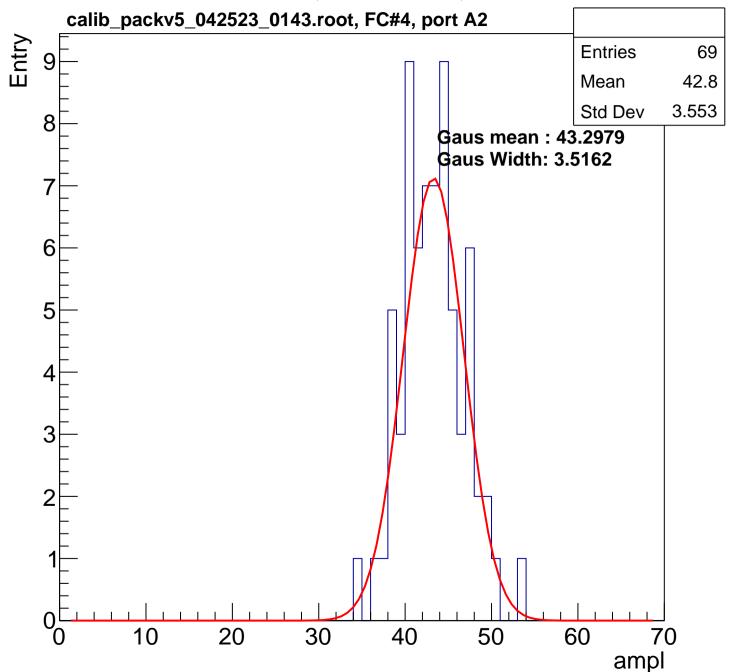


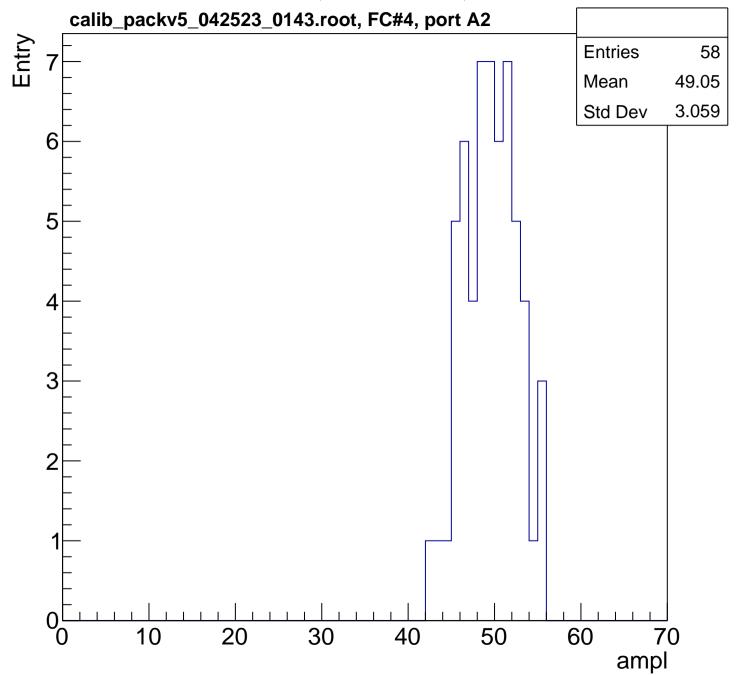


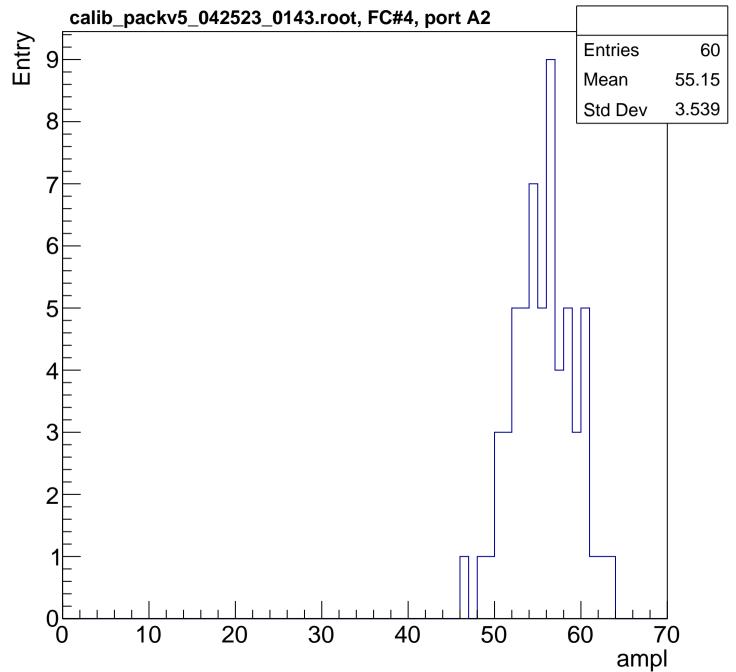


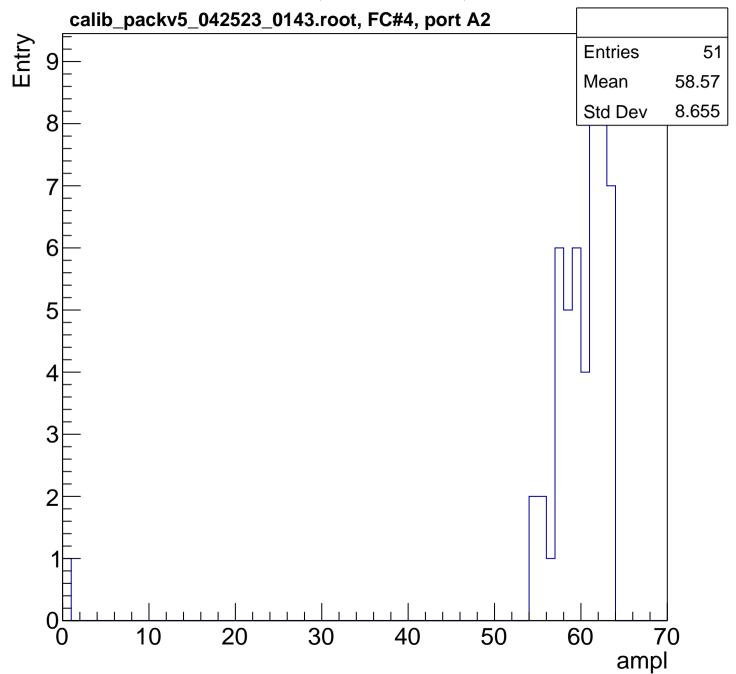


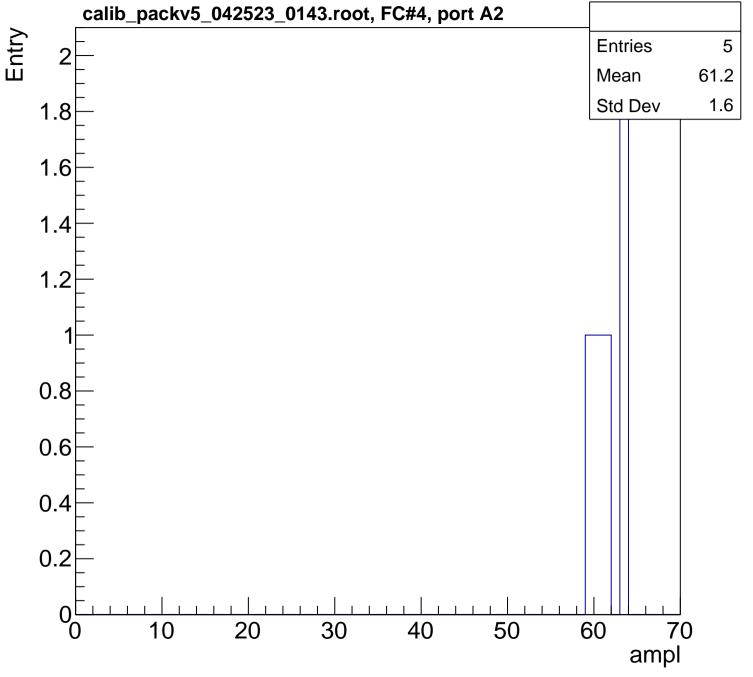


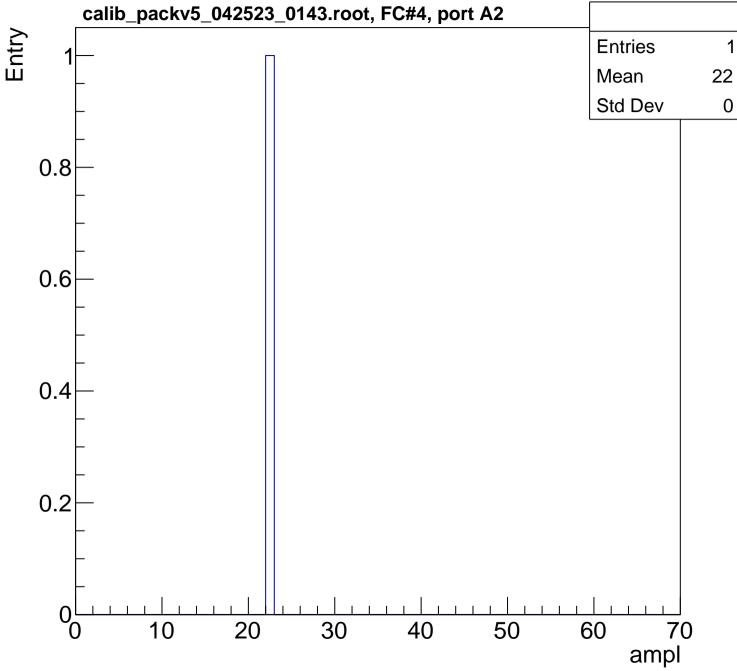


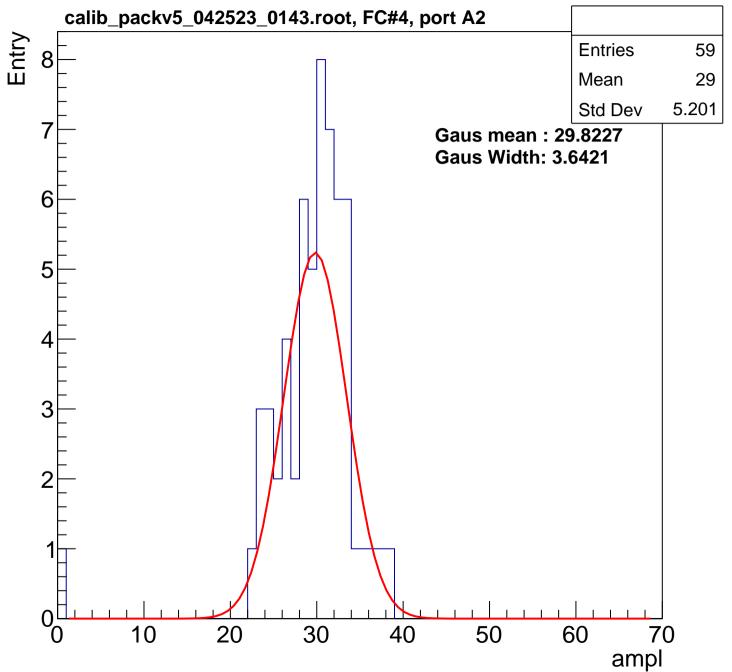


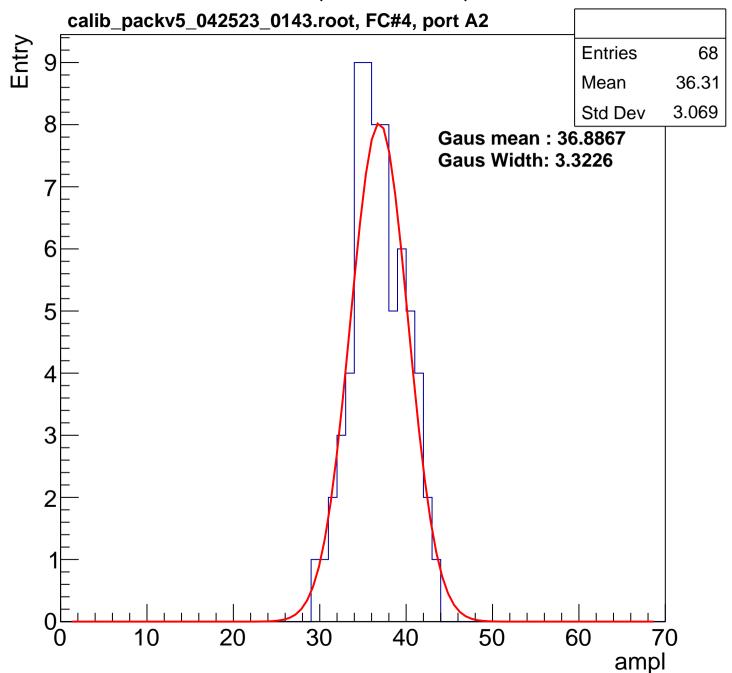


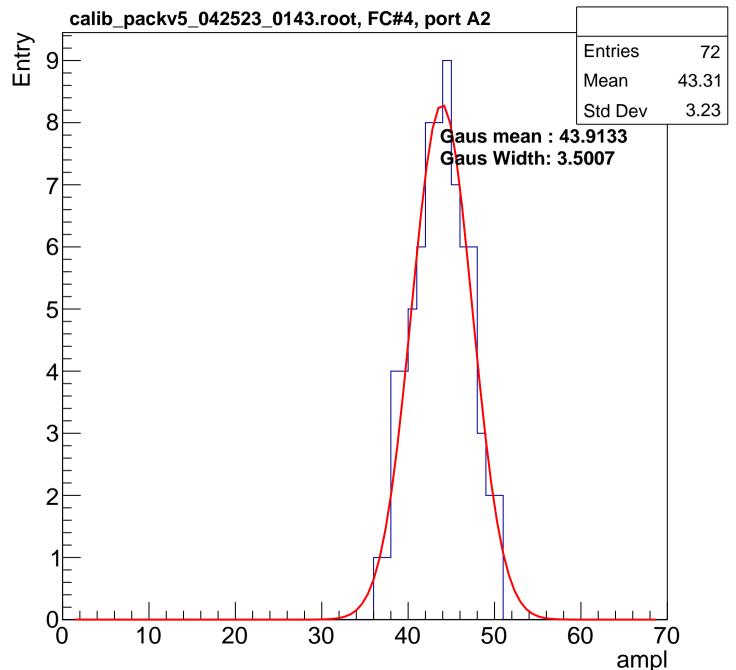


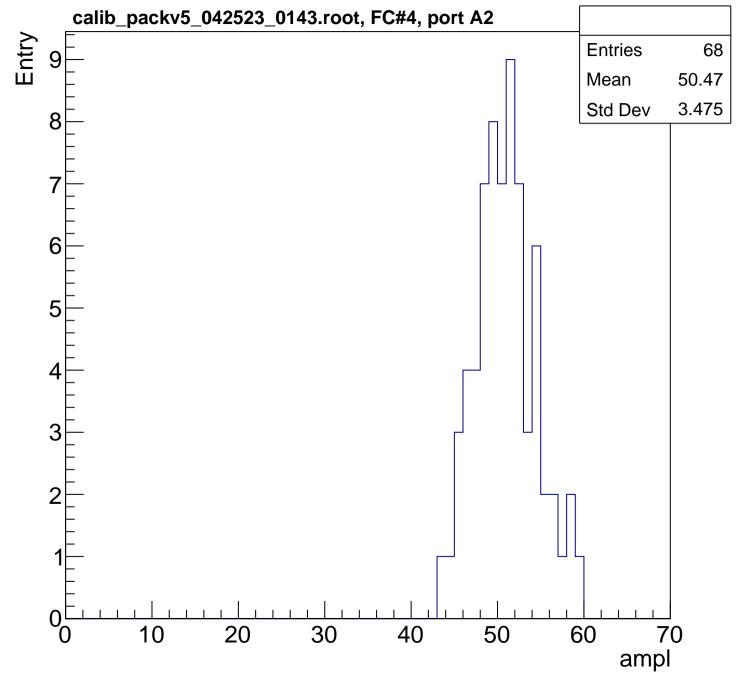


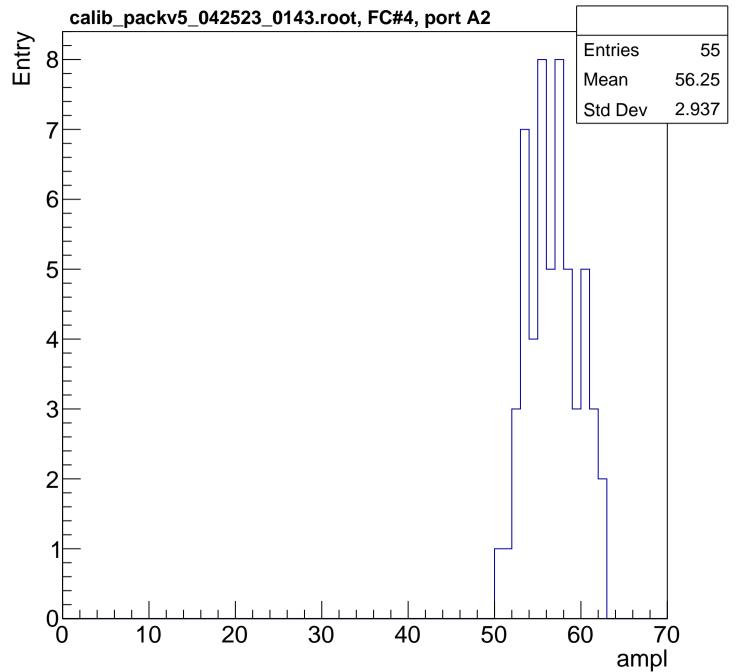


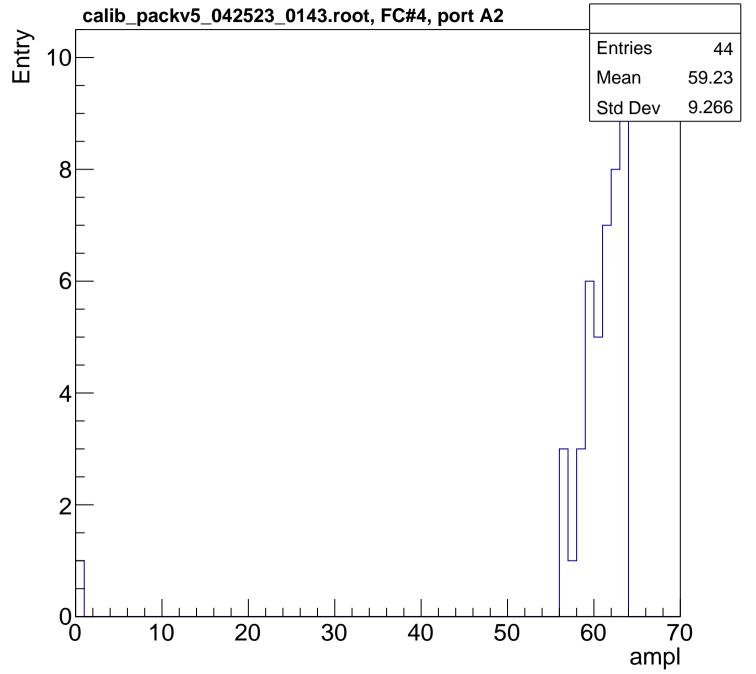


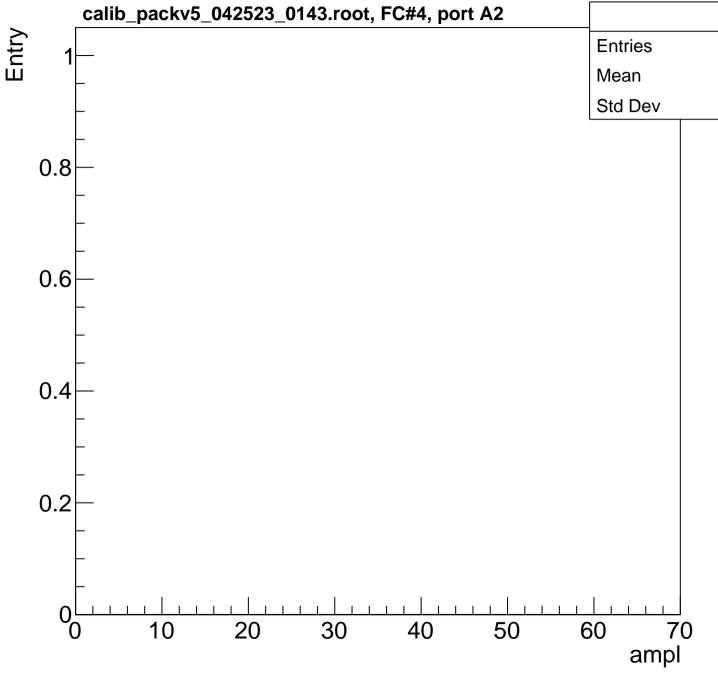




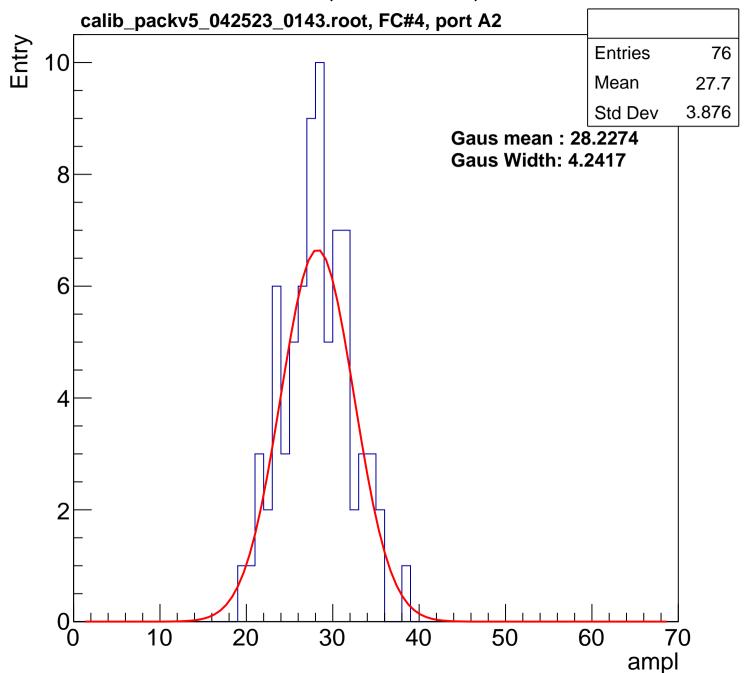


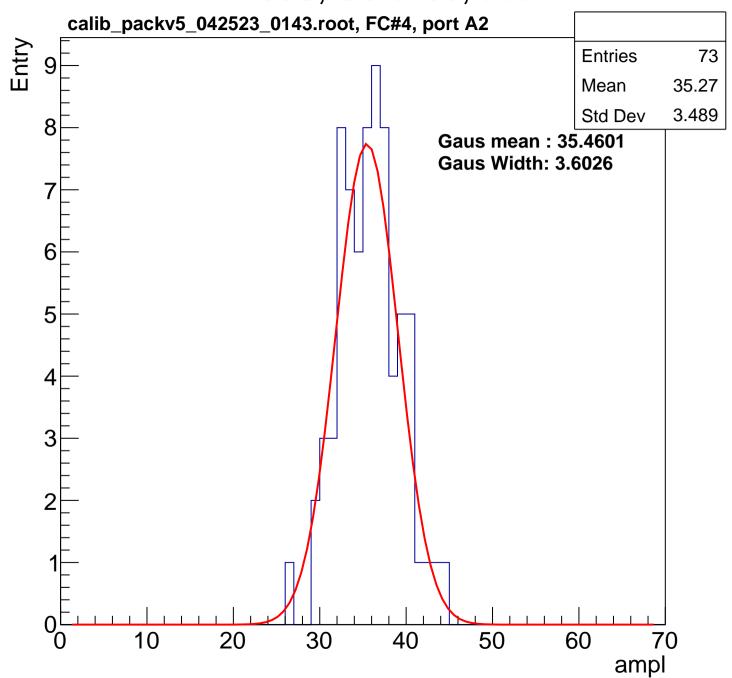


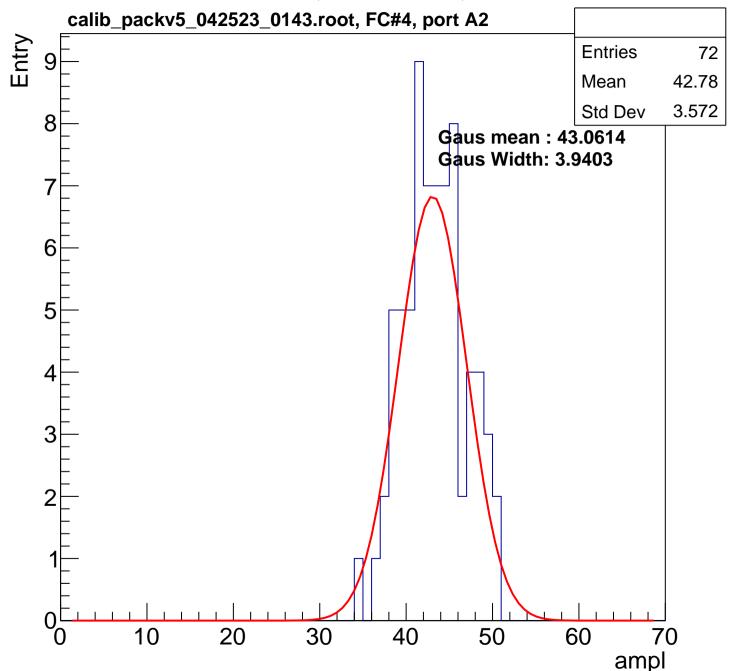


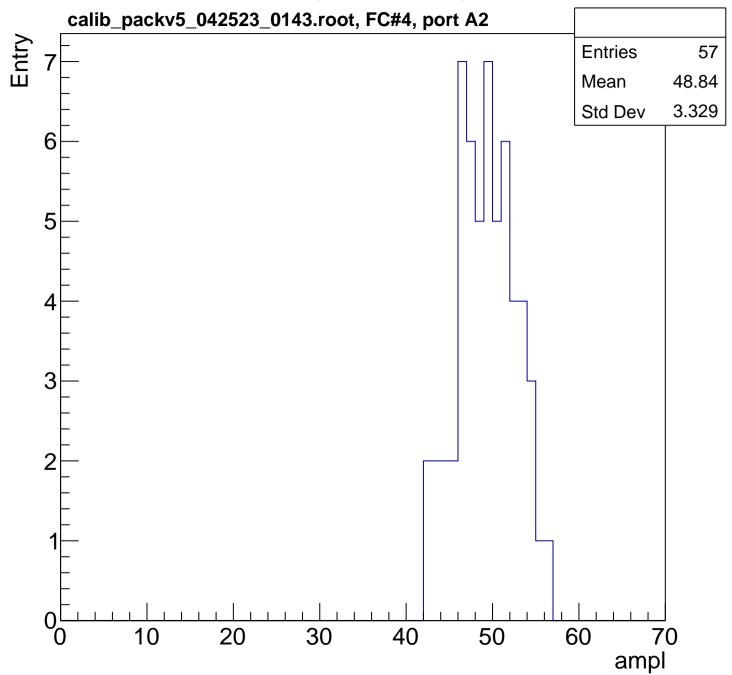


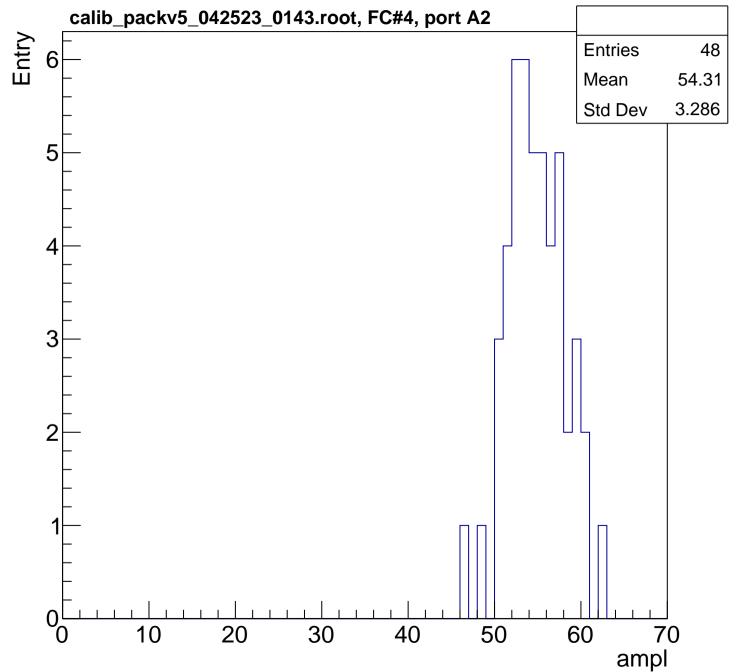
B1L100S, U8-ch49, adc7 calib_packv5_042523_0143.root, FC#4, port A2 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

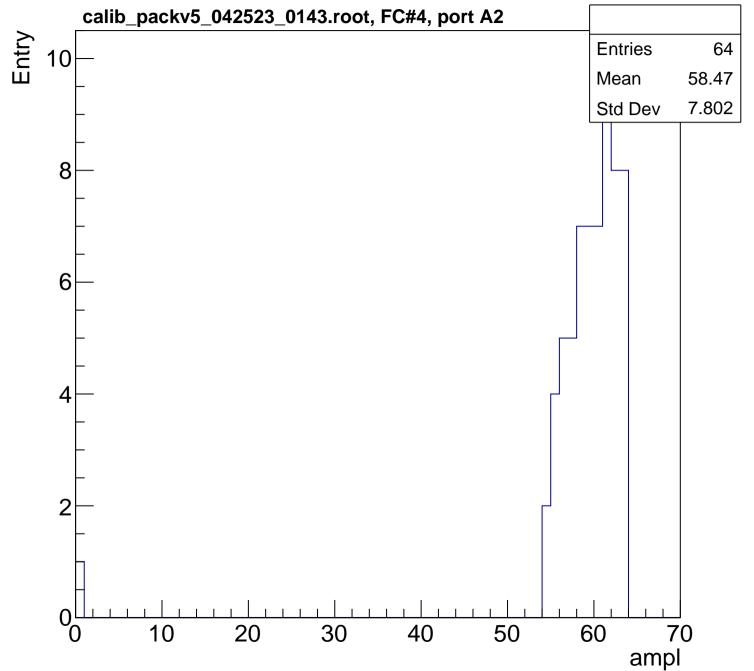


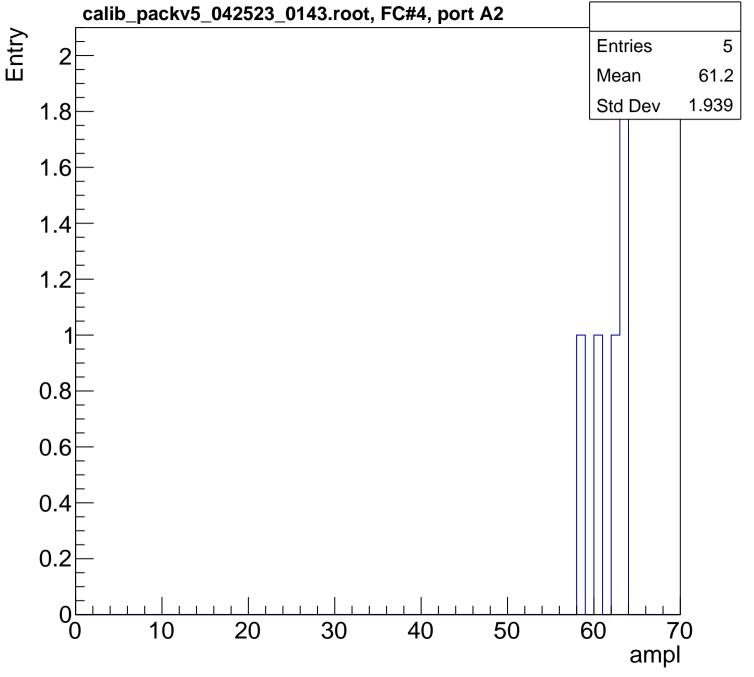




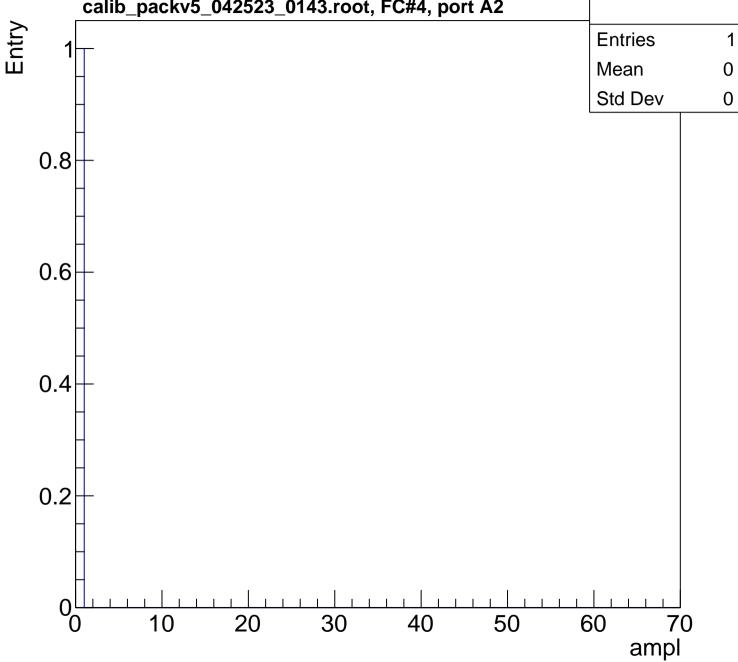


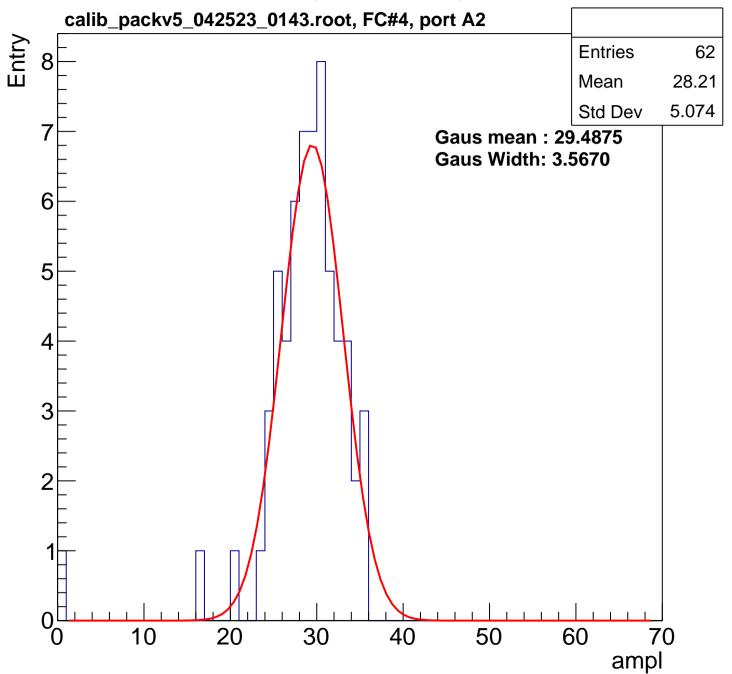


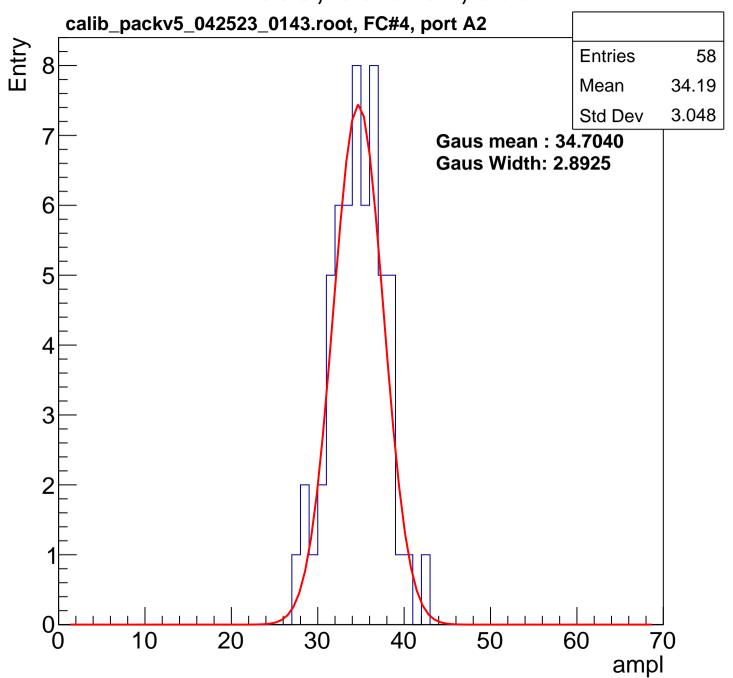


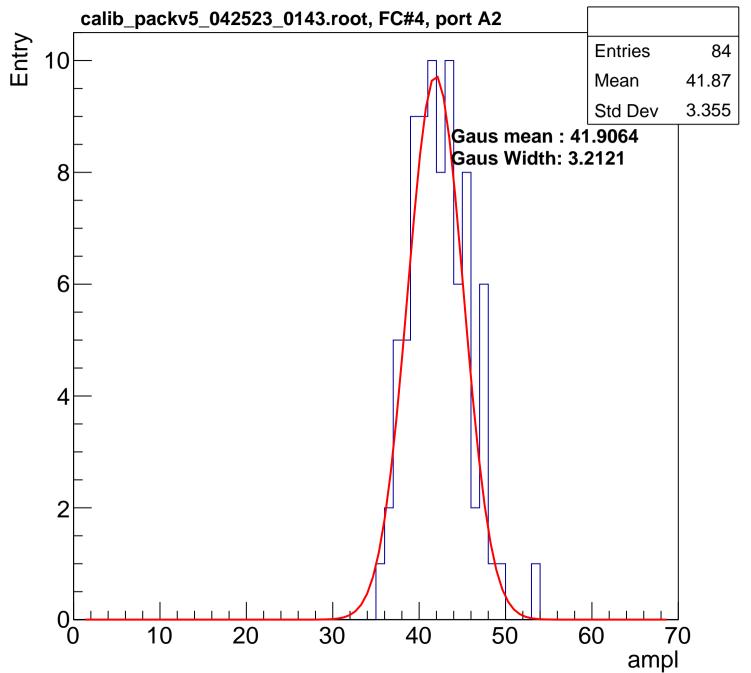


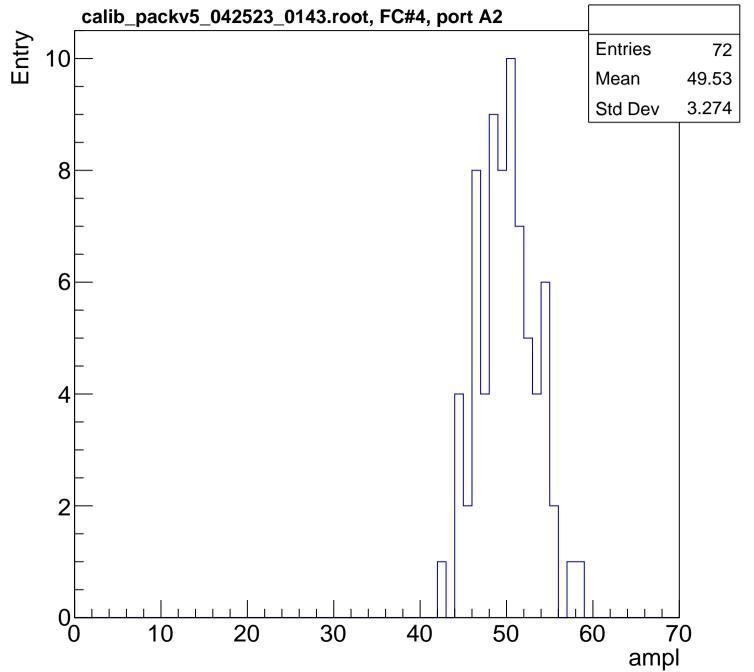
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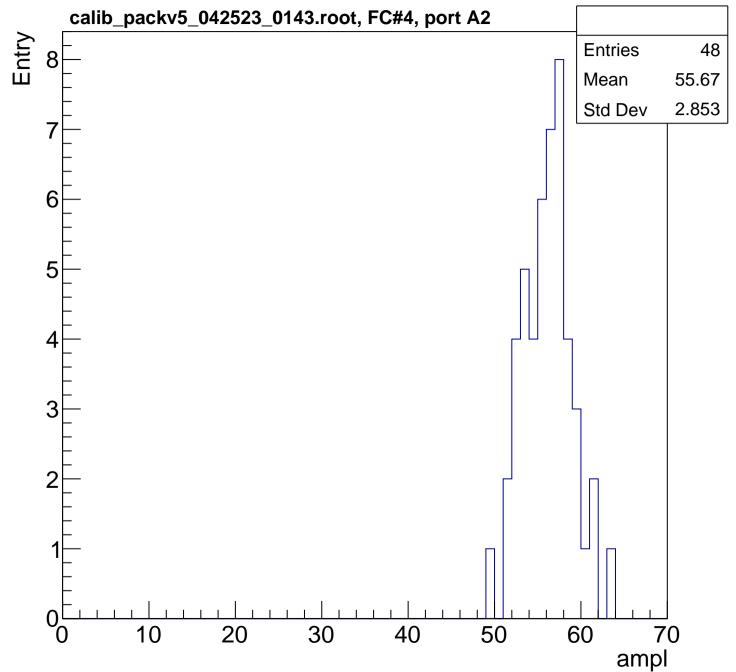


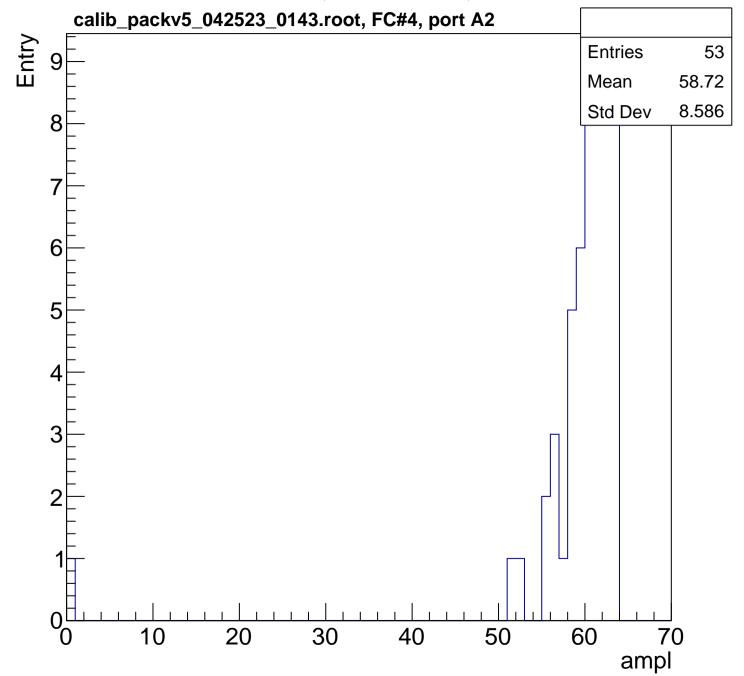


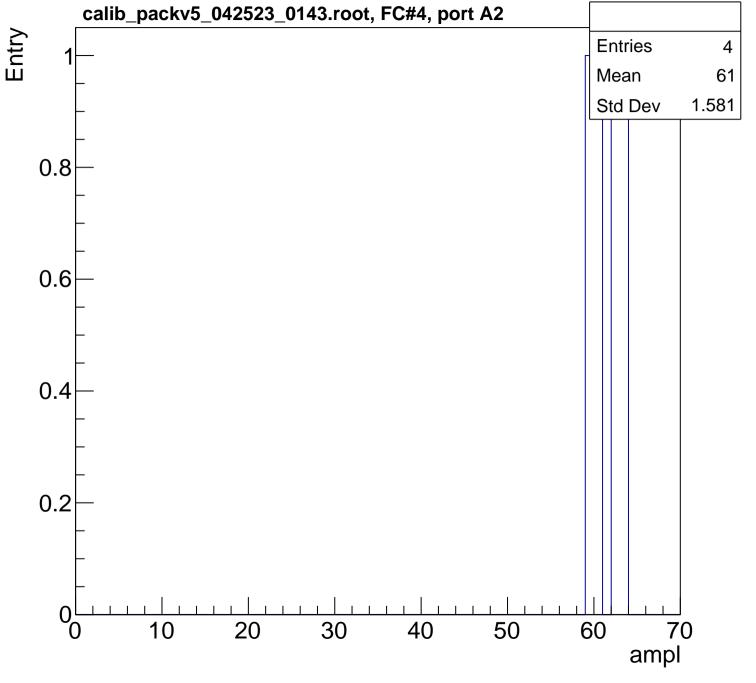


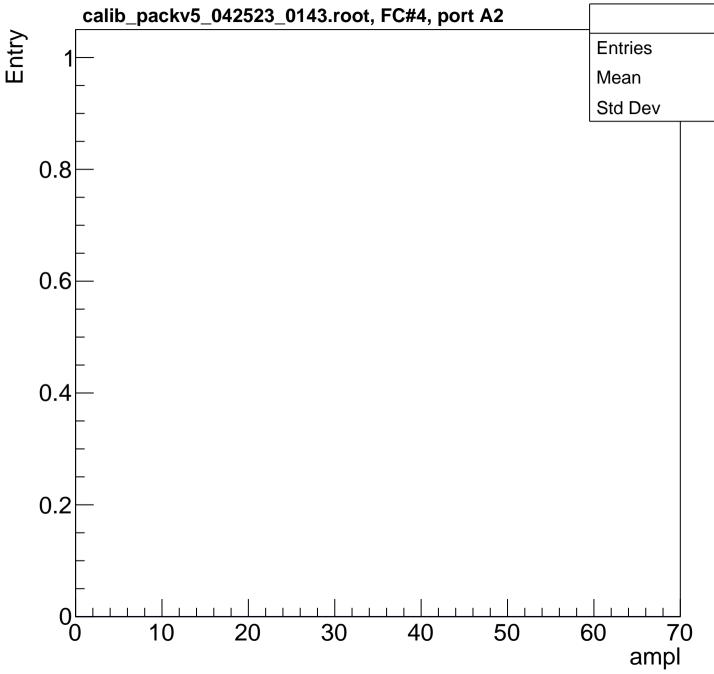


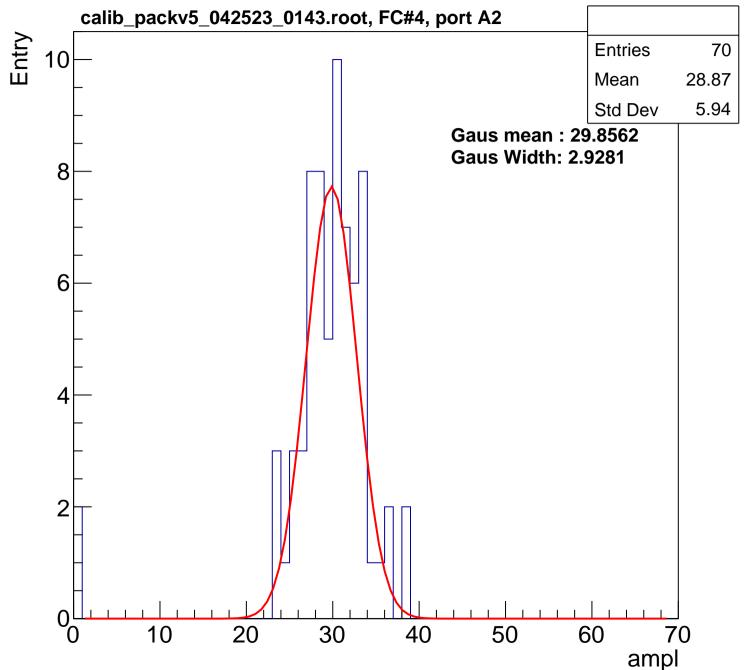


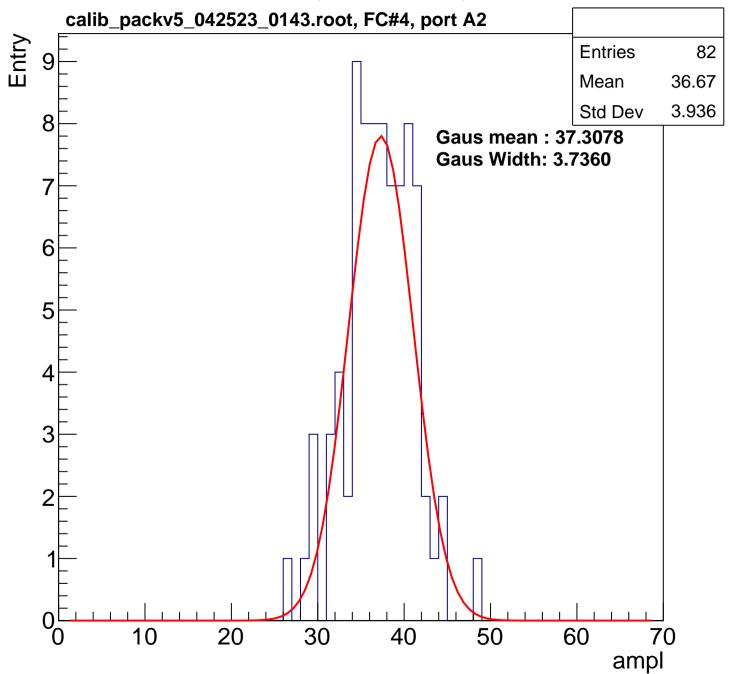


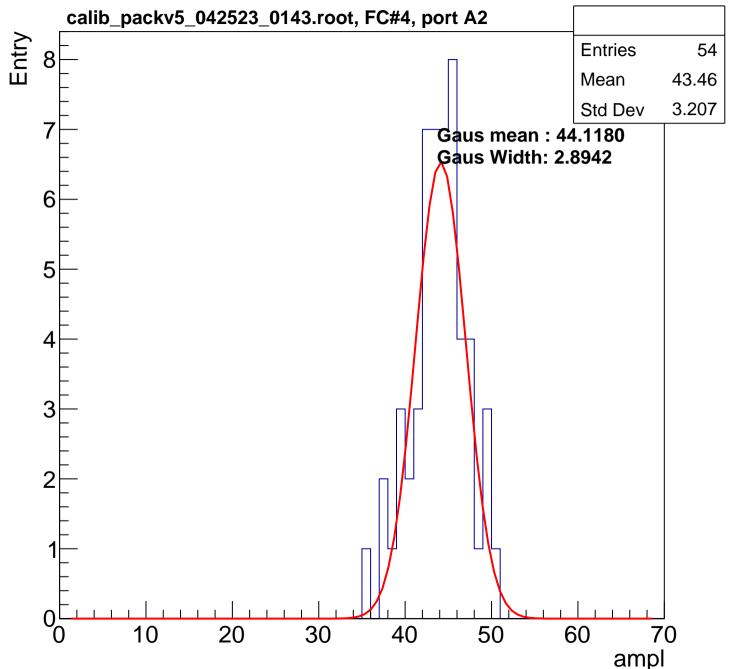


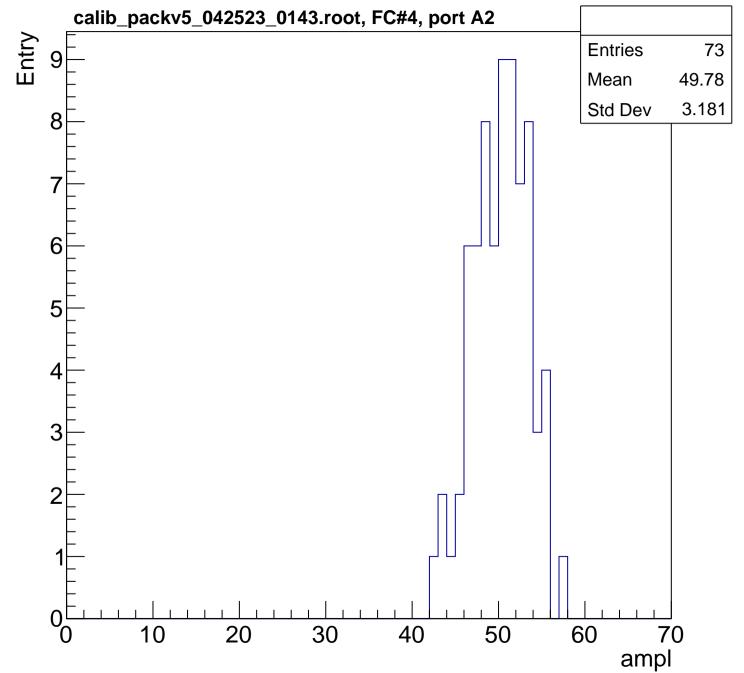


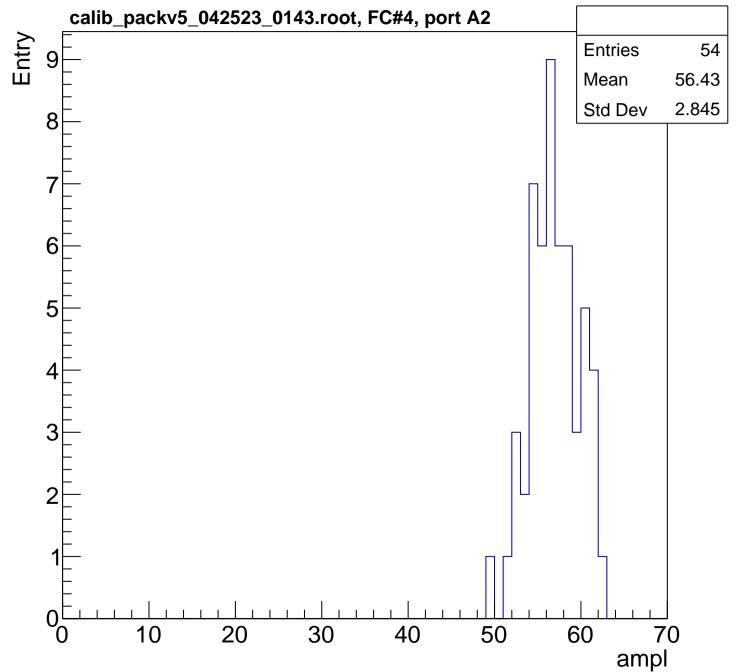


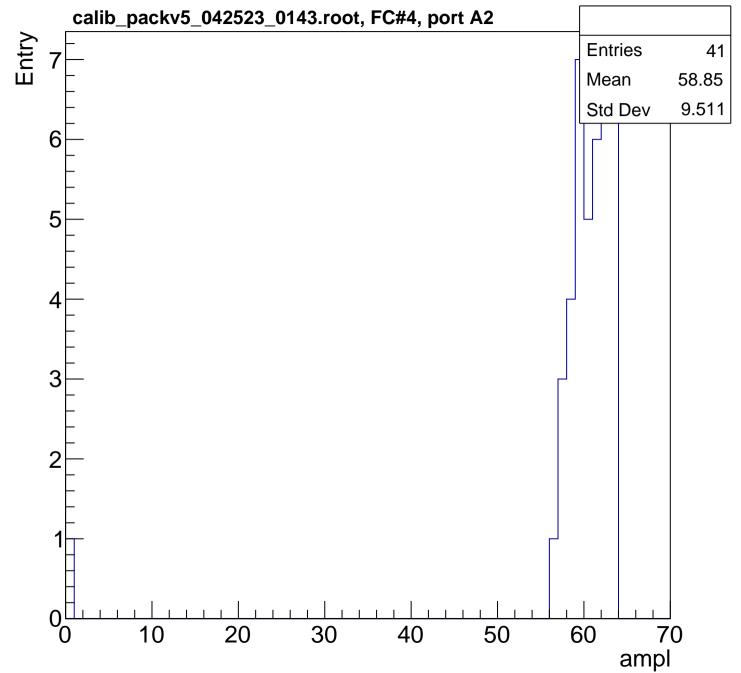


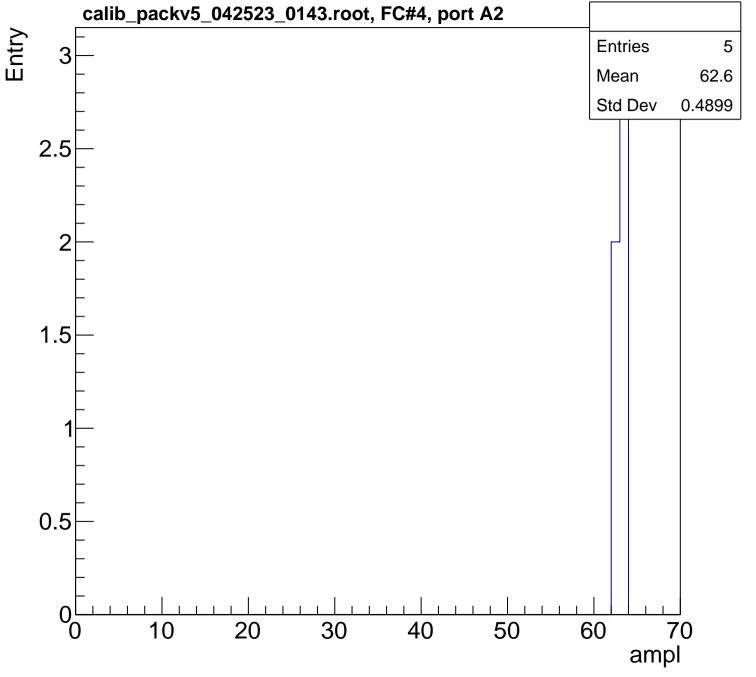


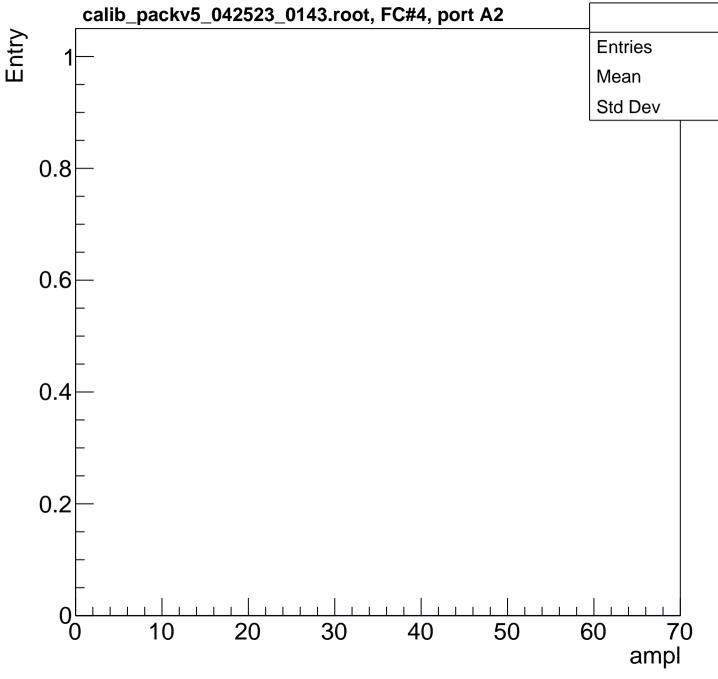


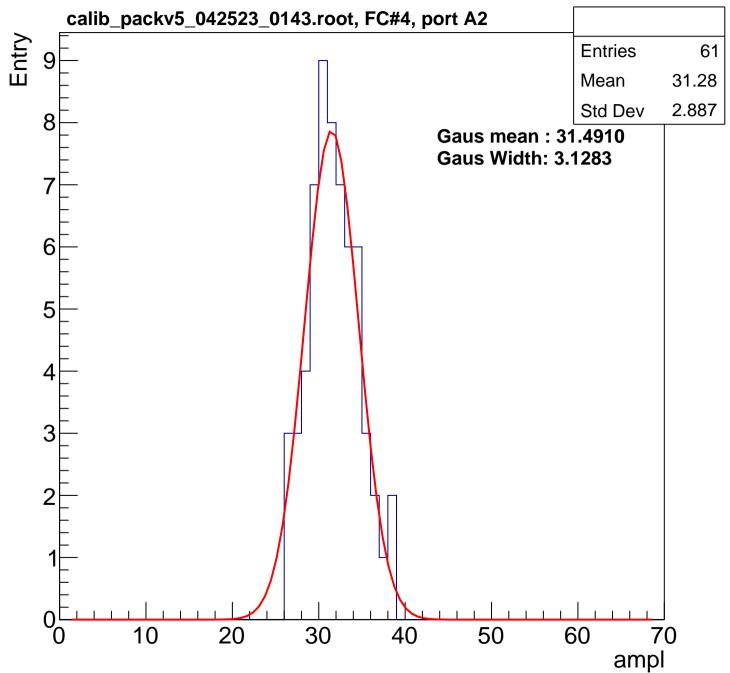


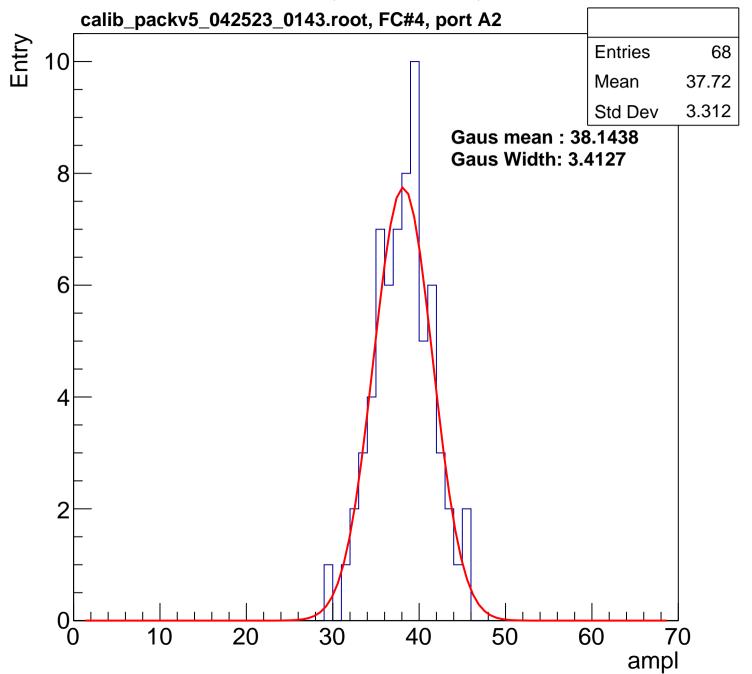


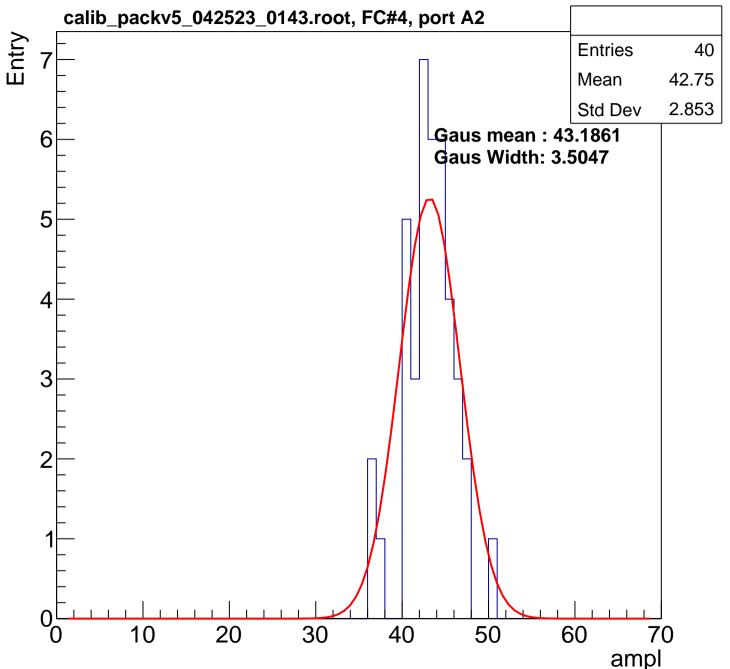


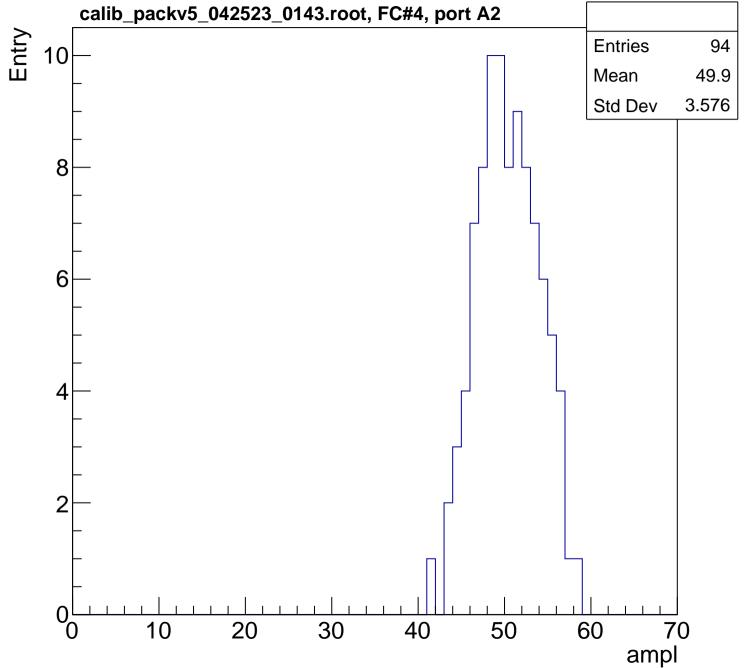


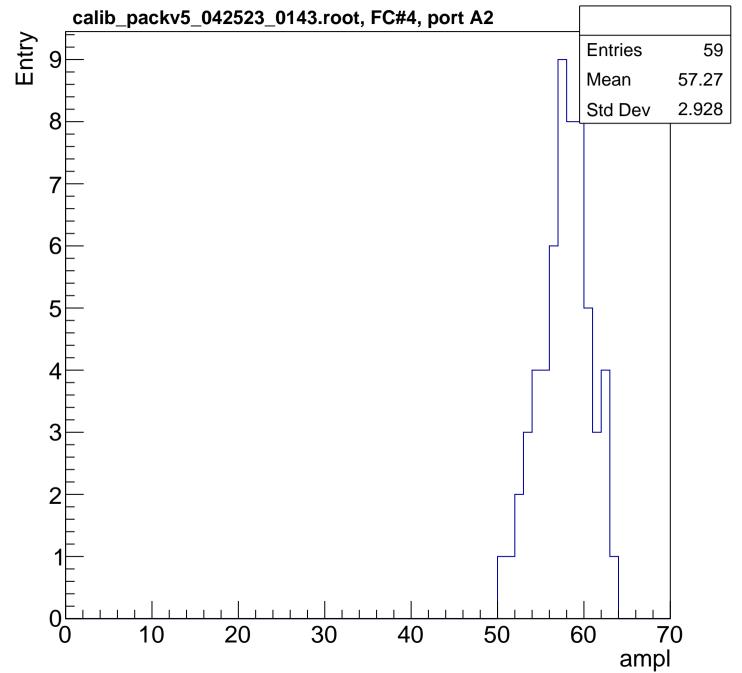


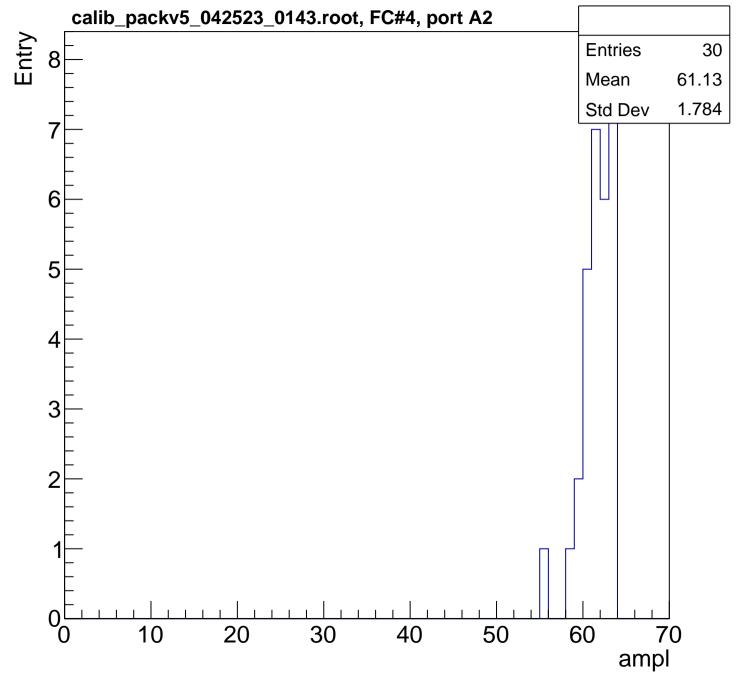


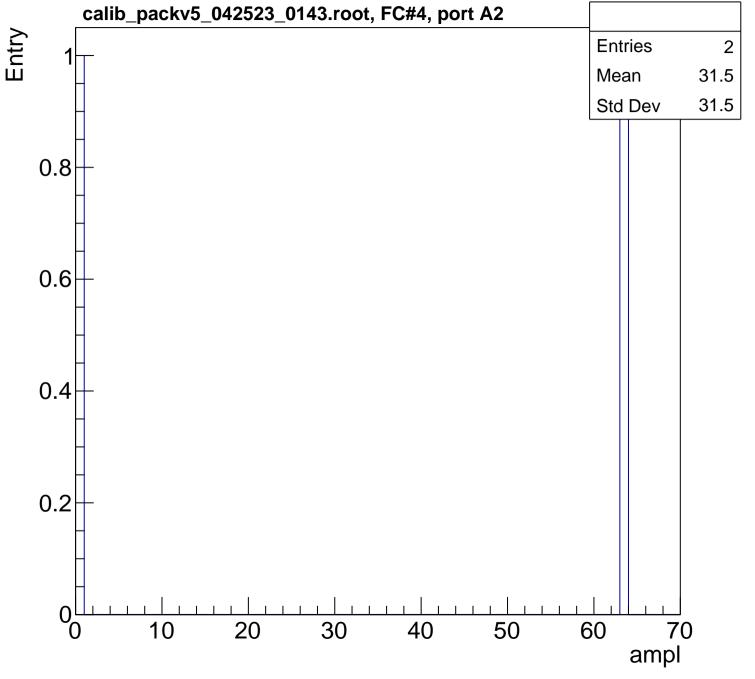


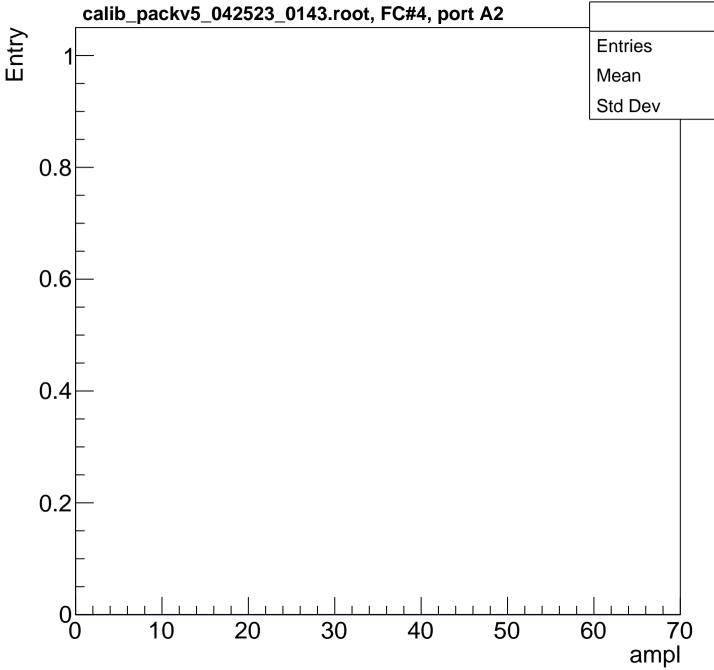


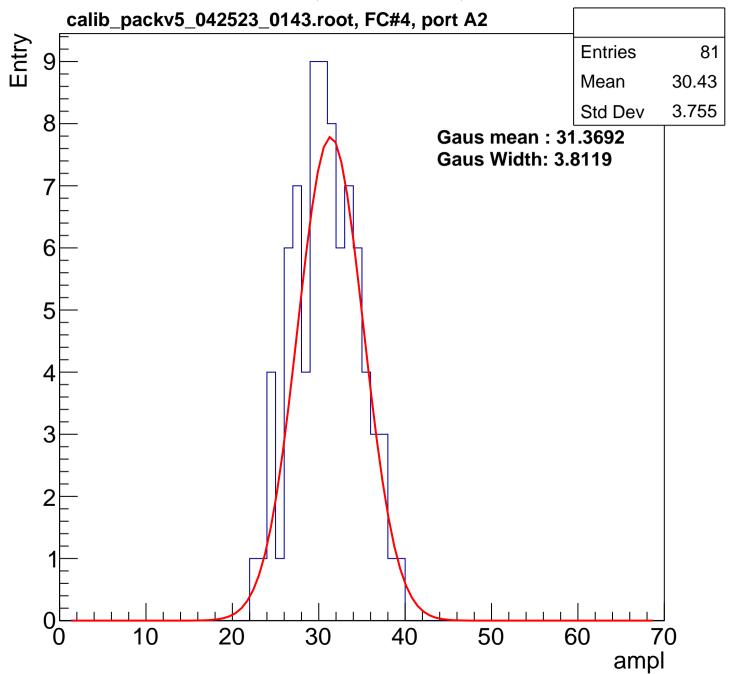


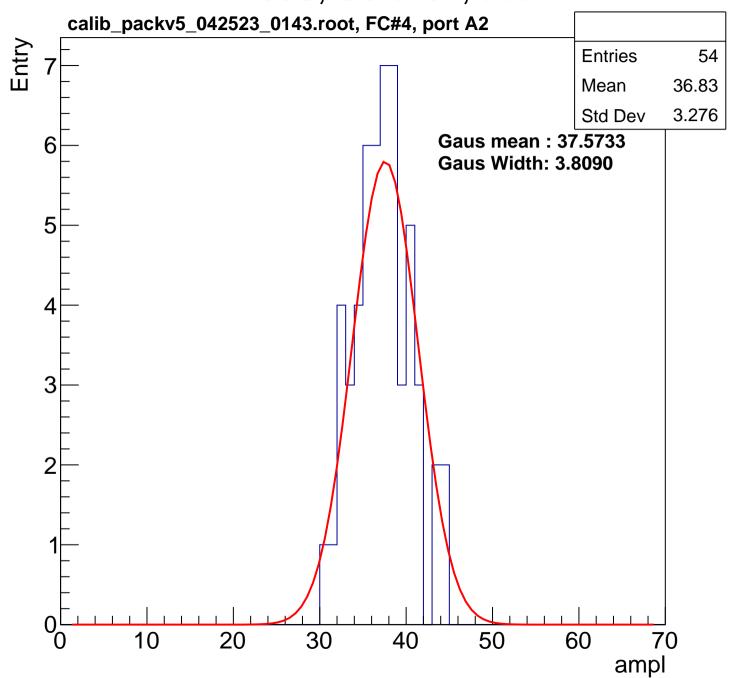


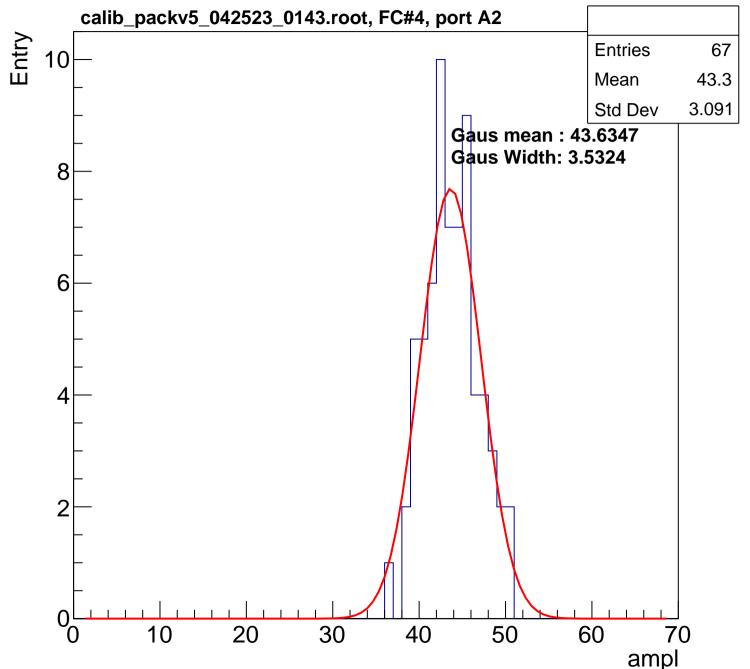


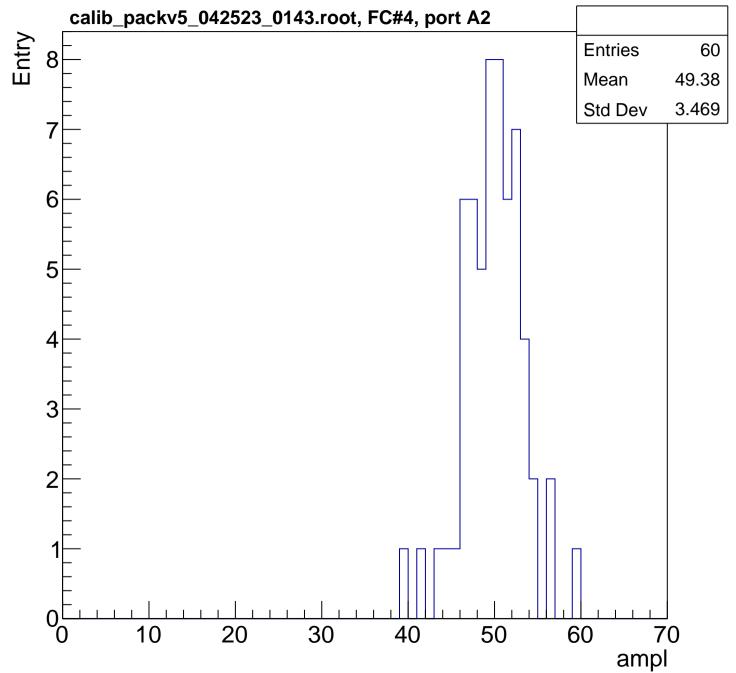


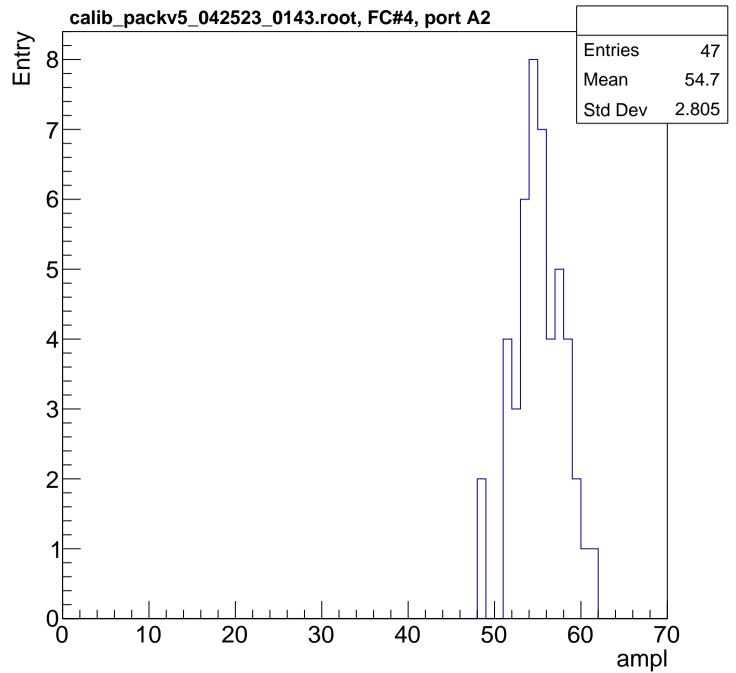


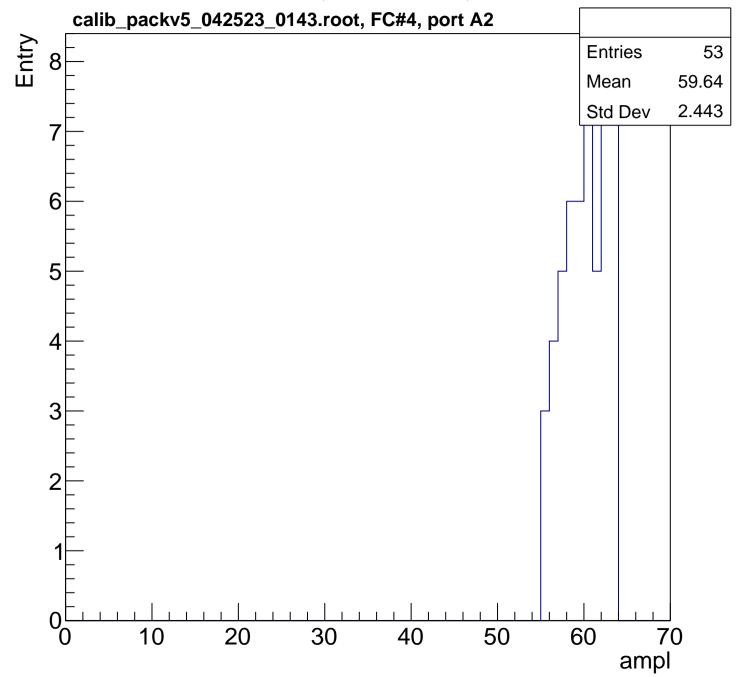


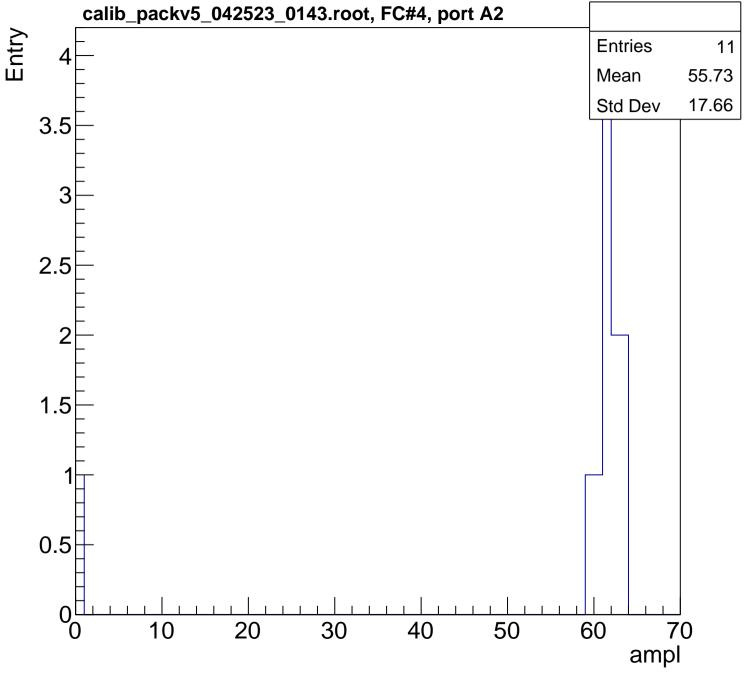




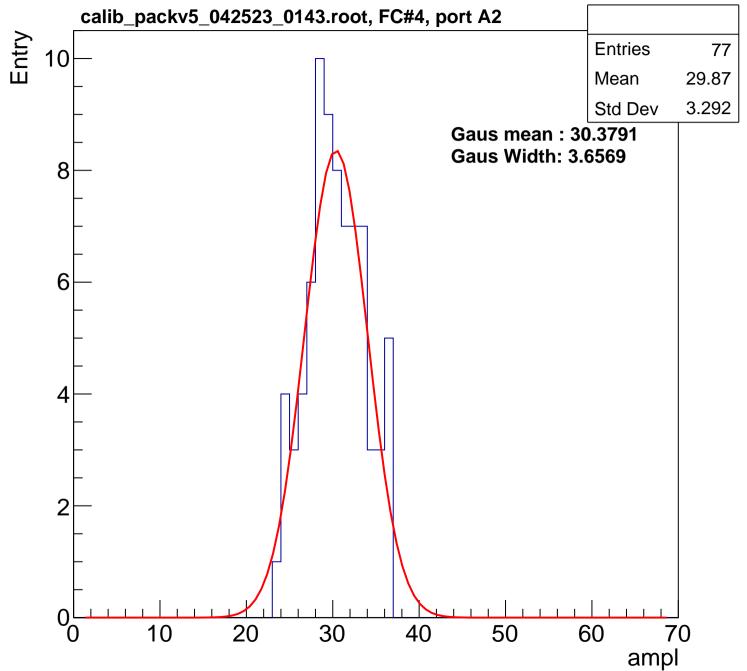


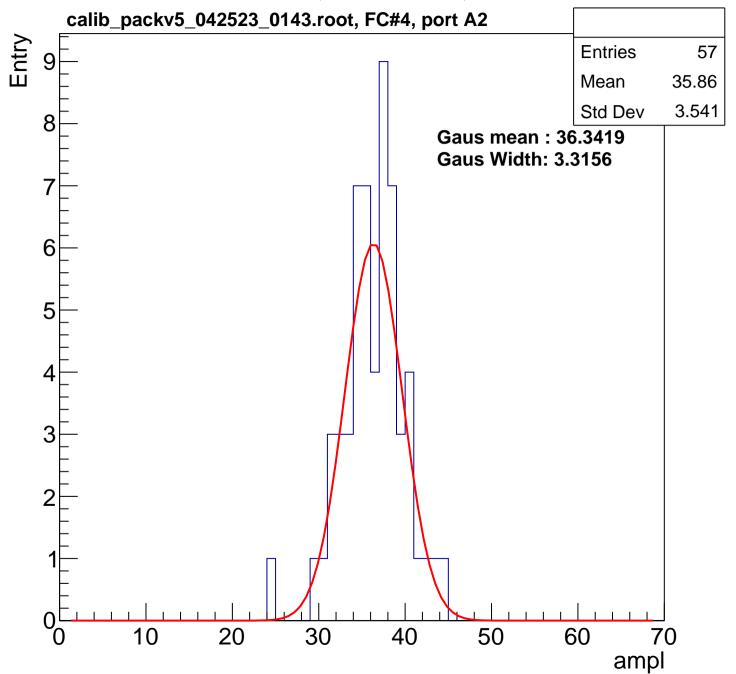


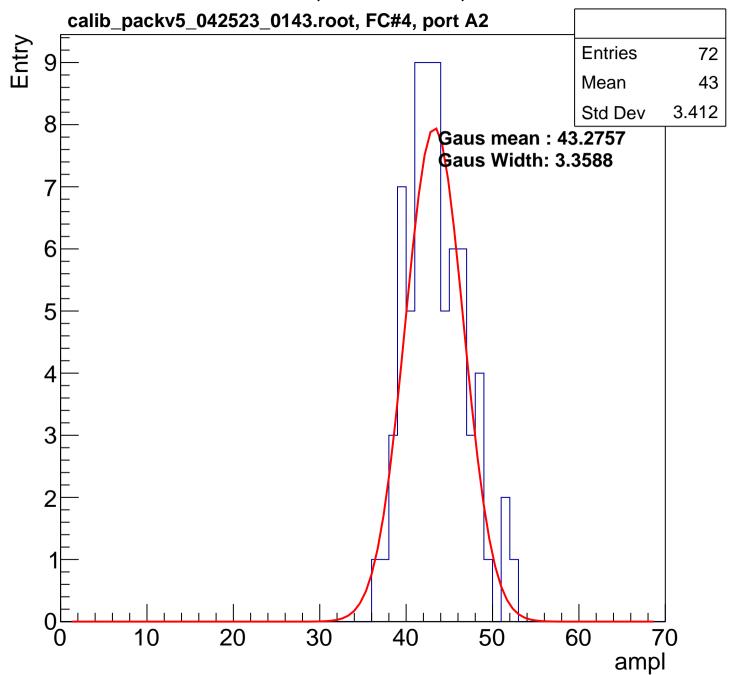


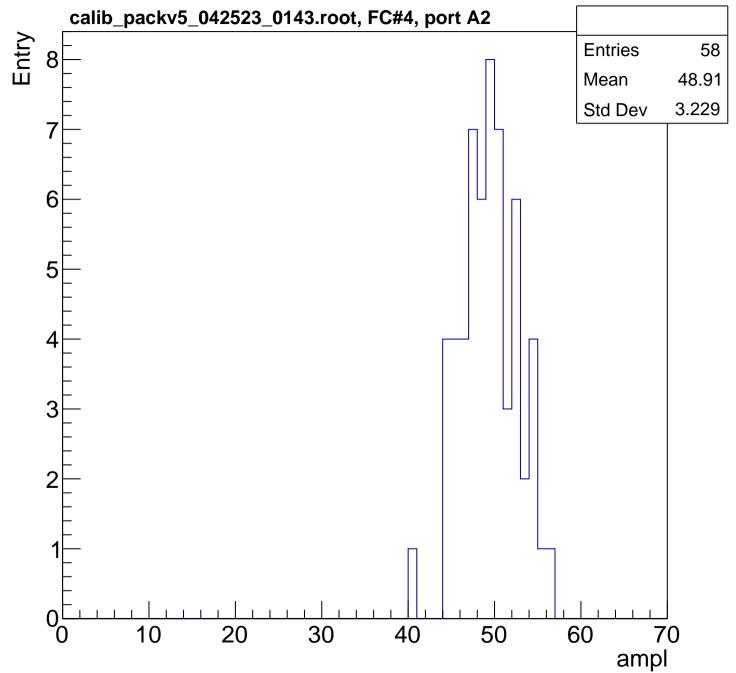


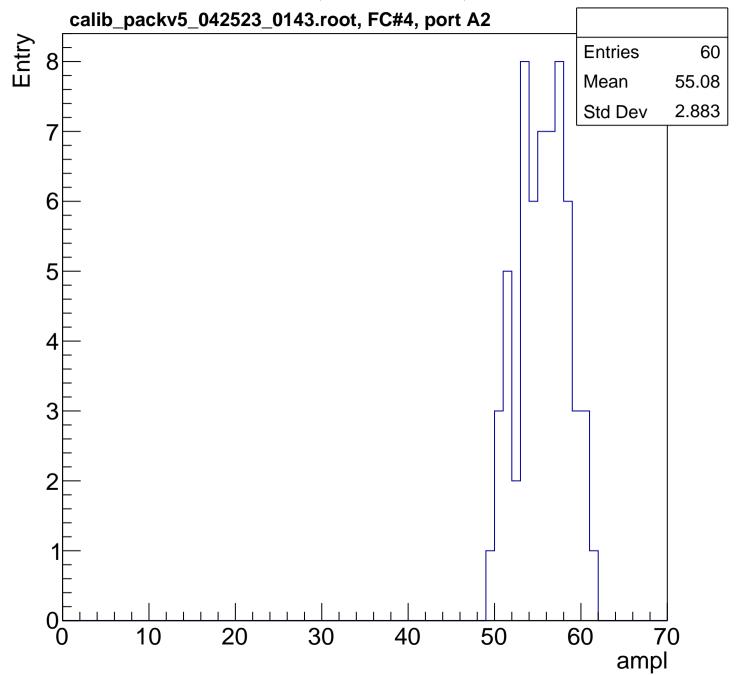


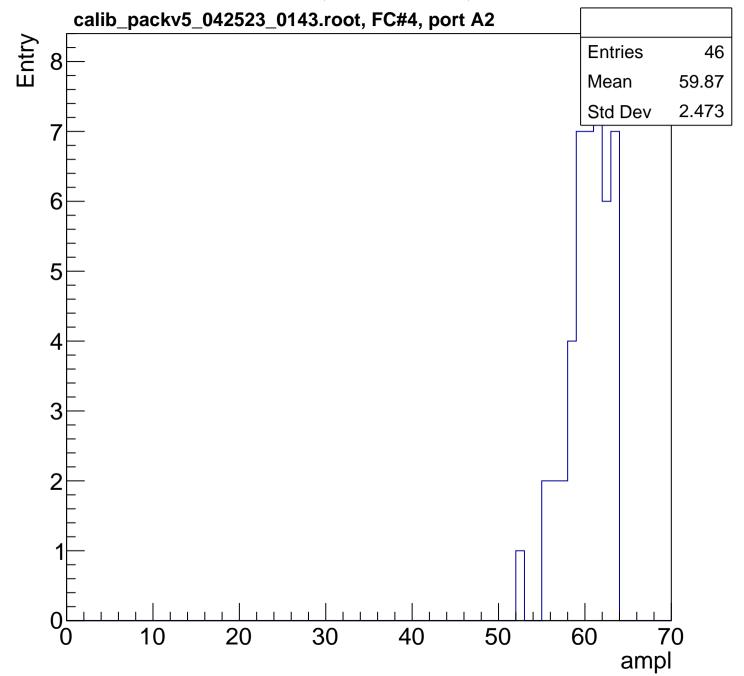


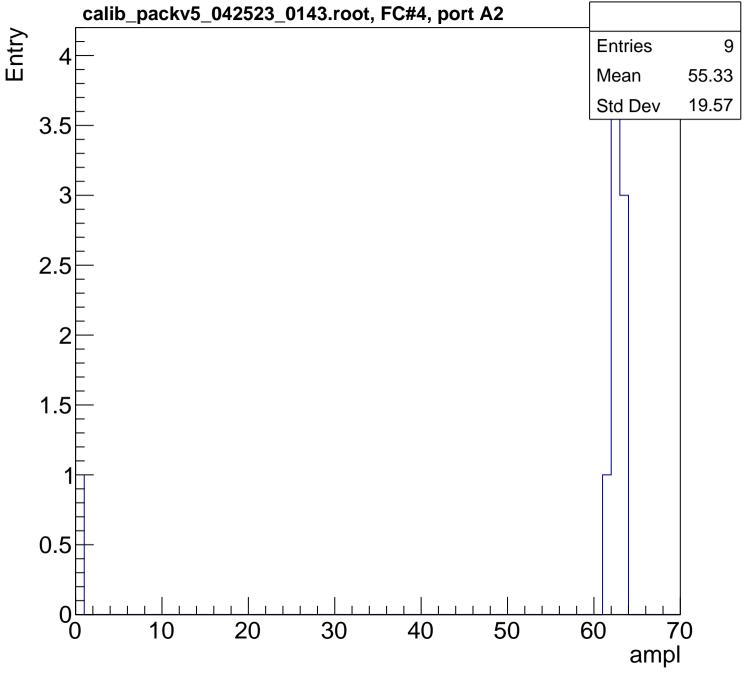




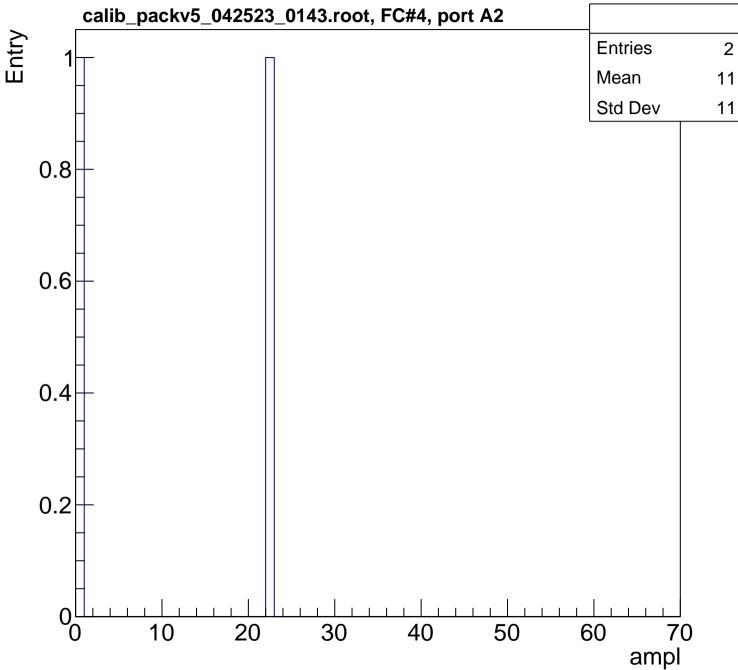


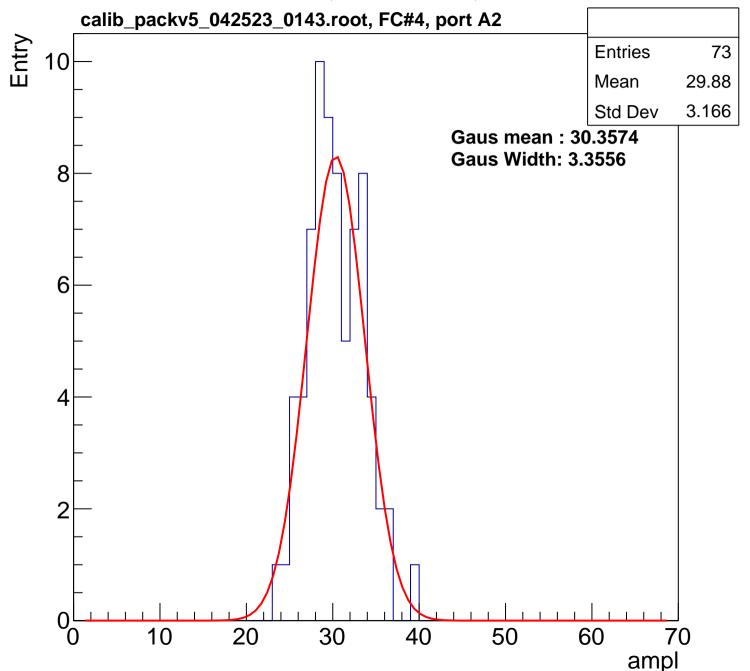


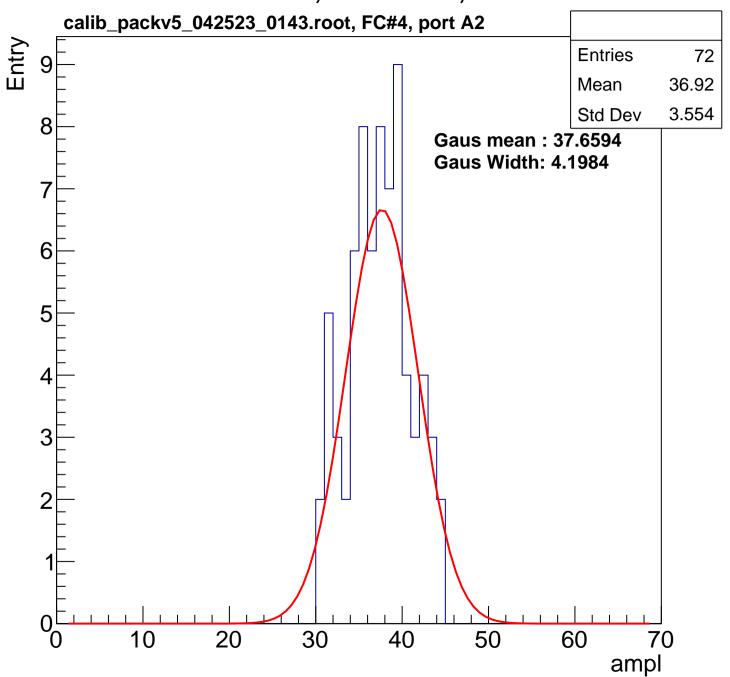


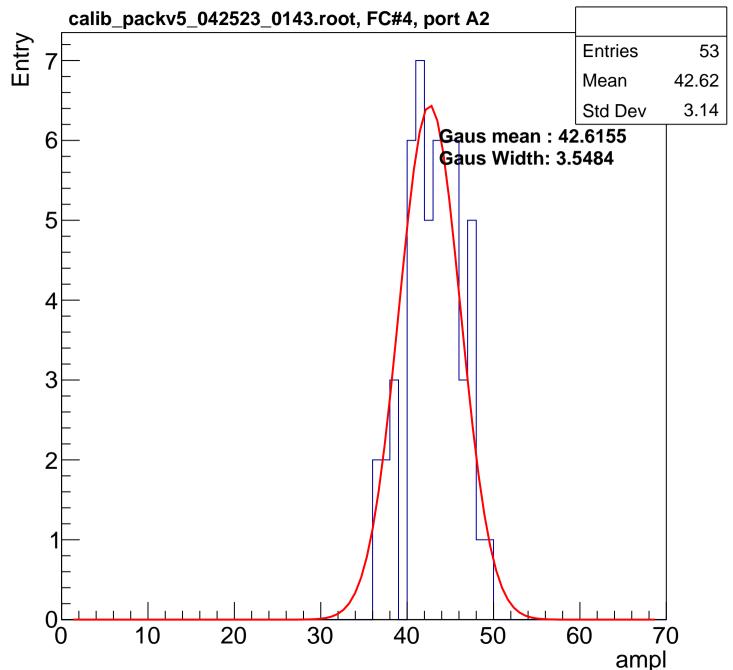


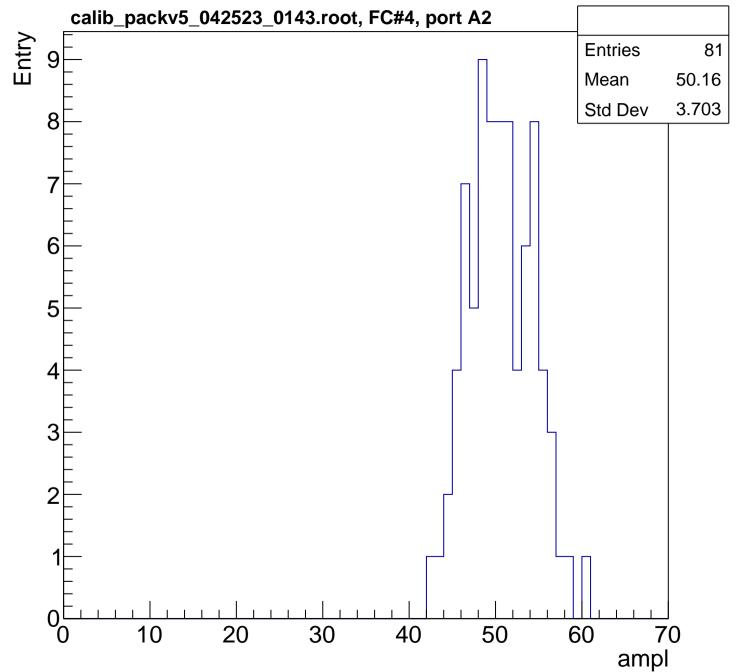
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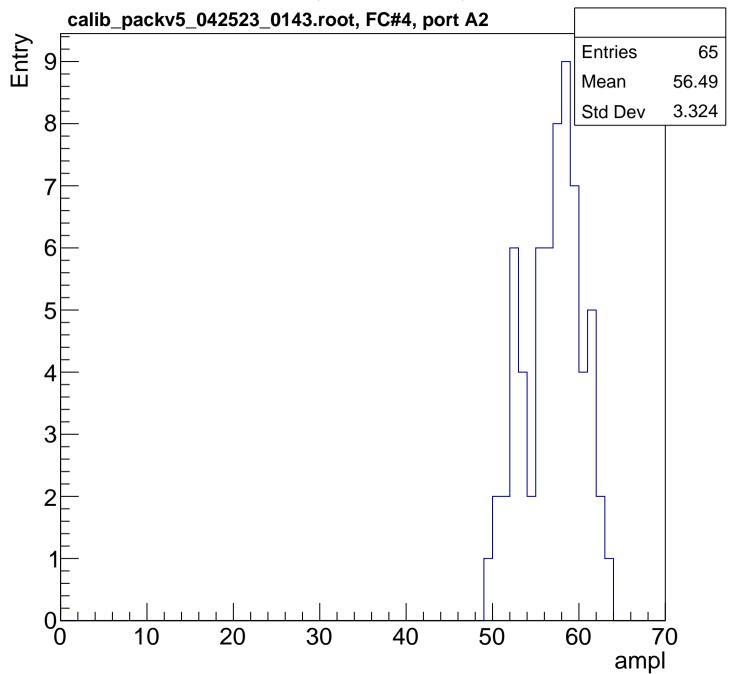


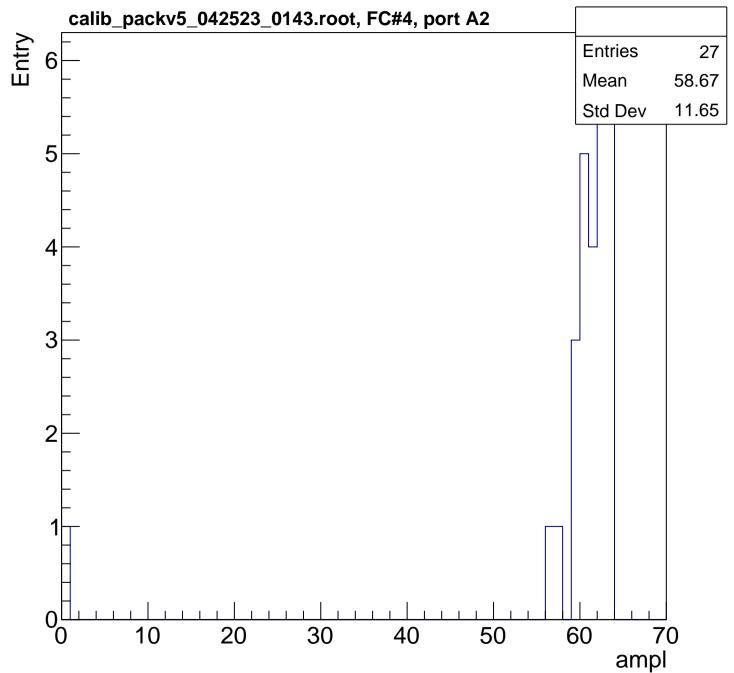


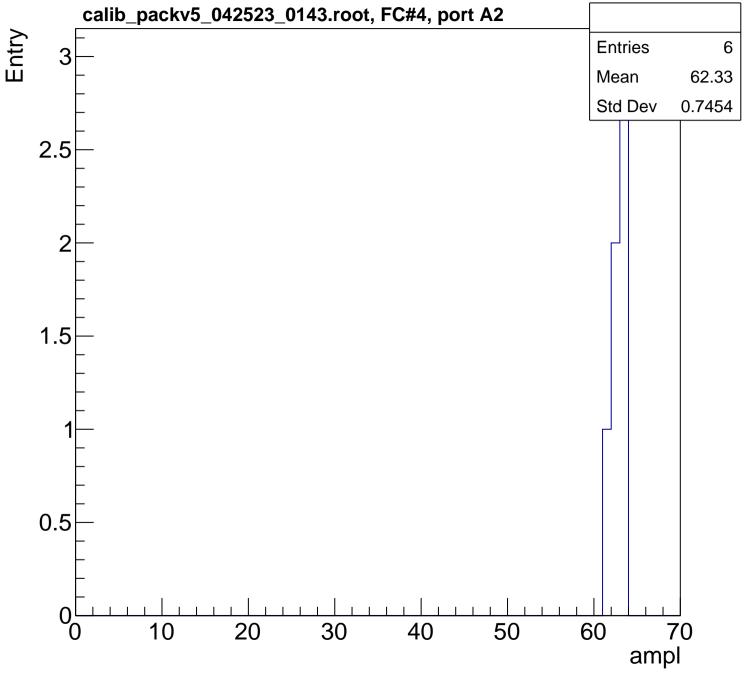


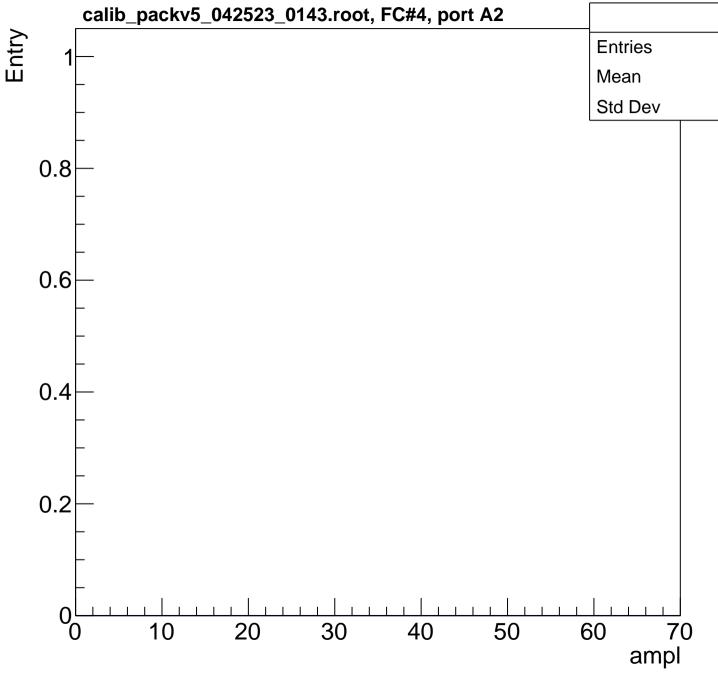


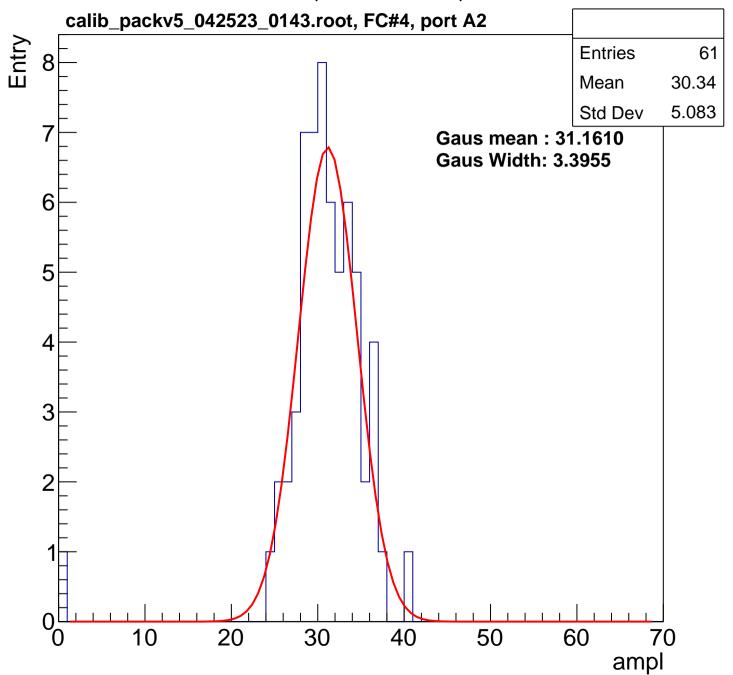


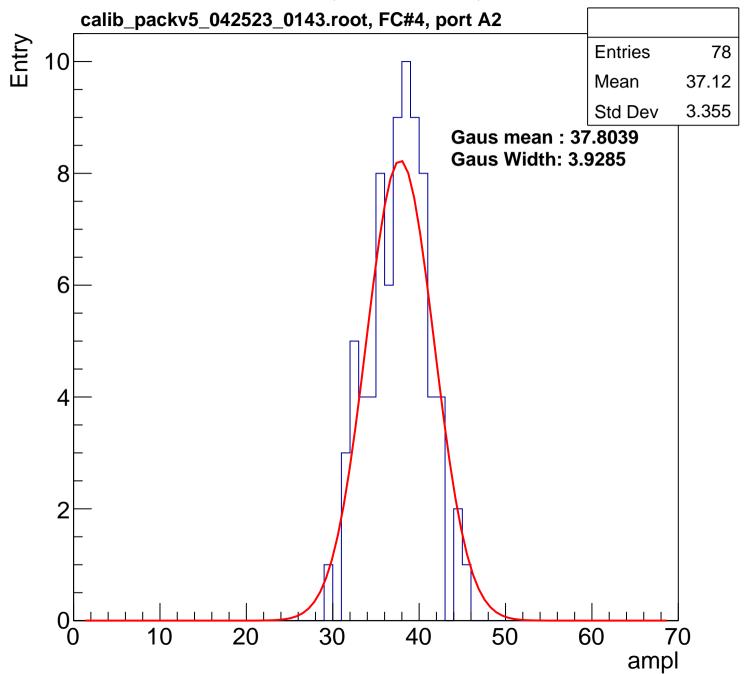


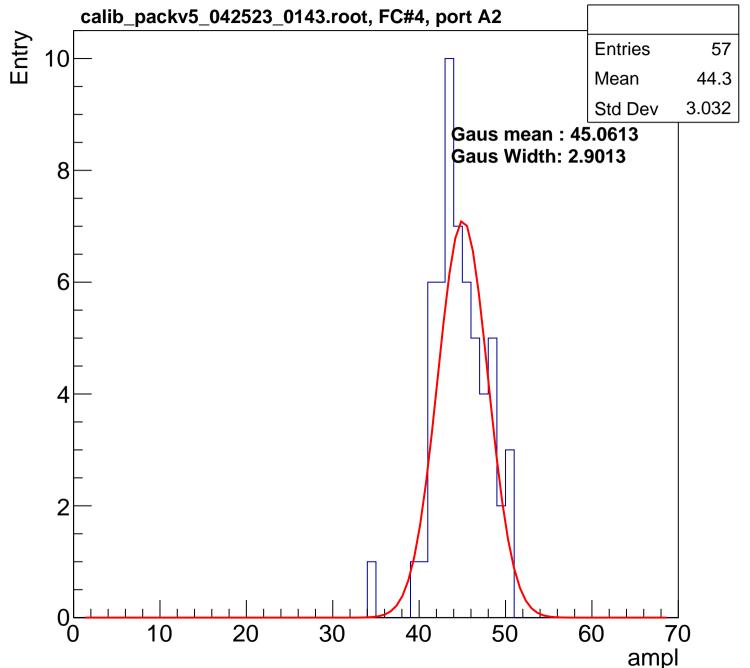


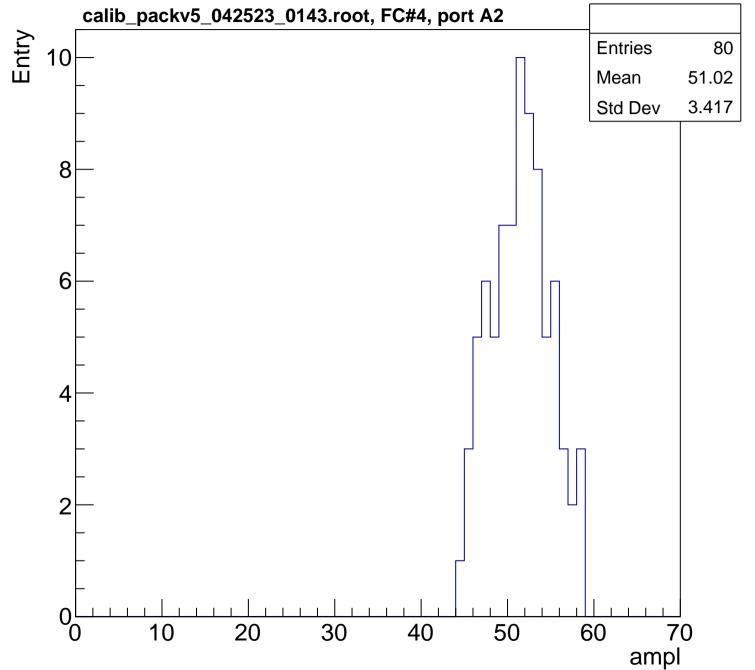


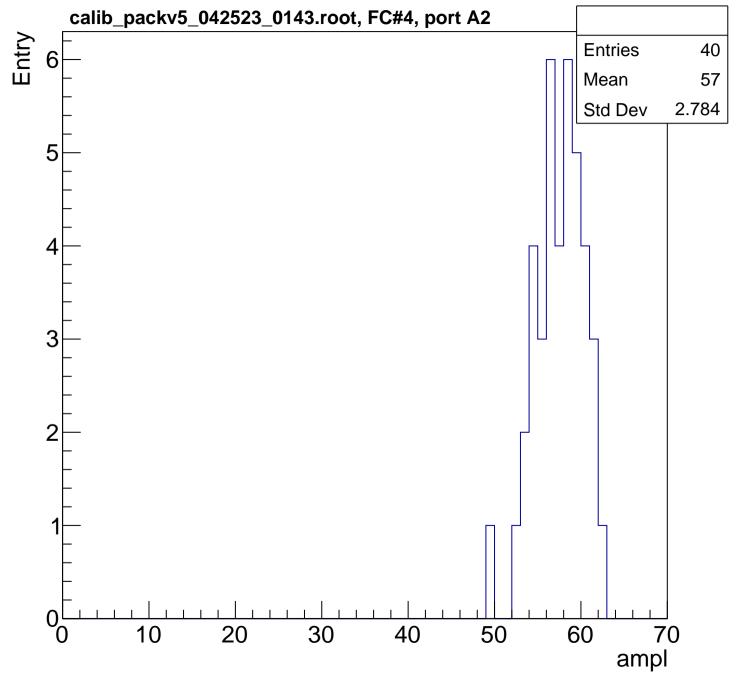


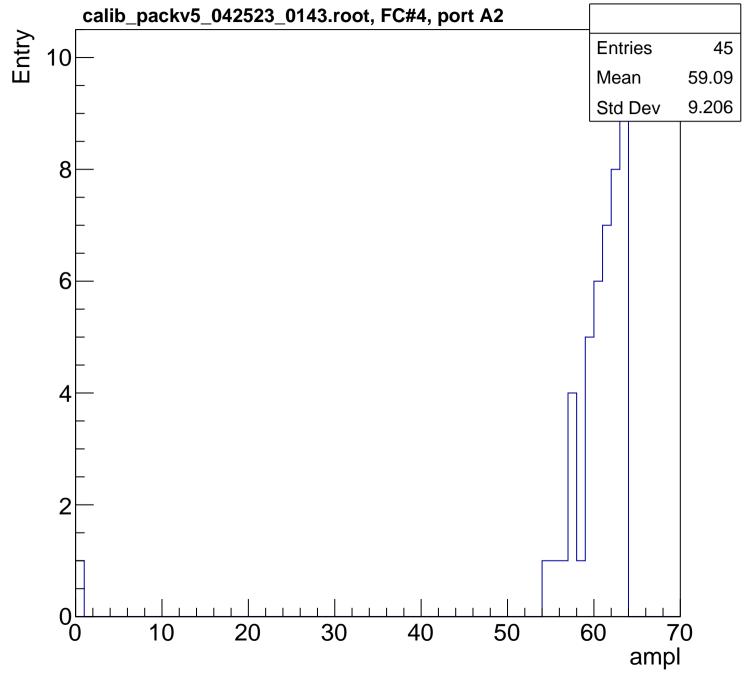


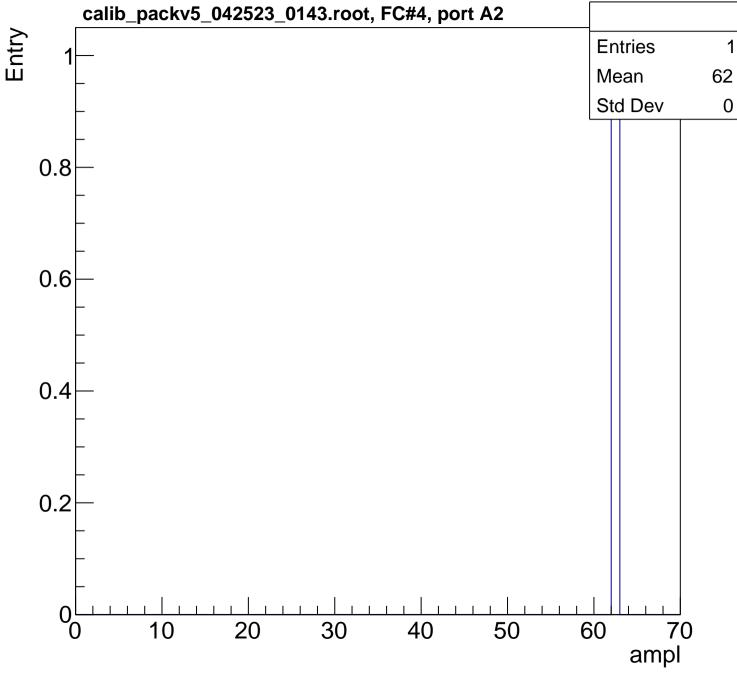




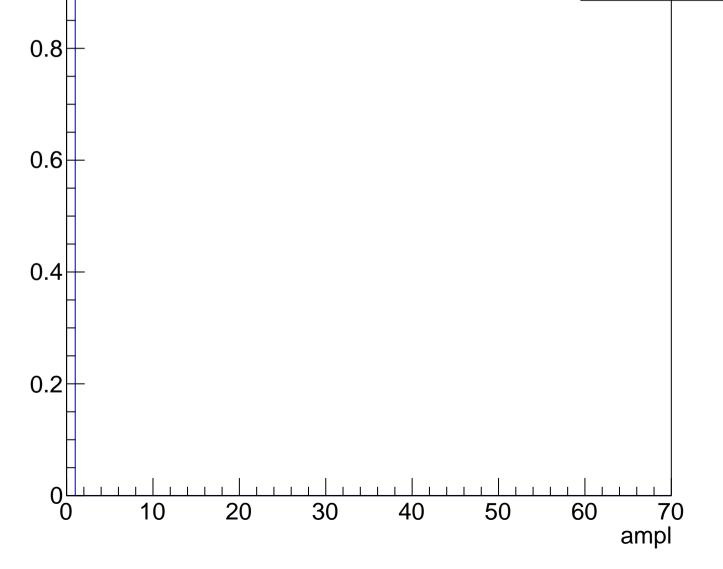


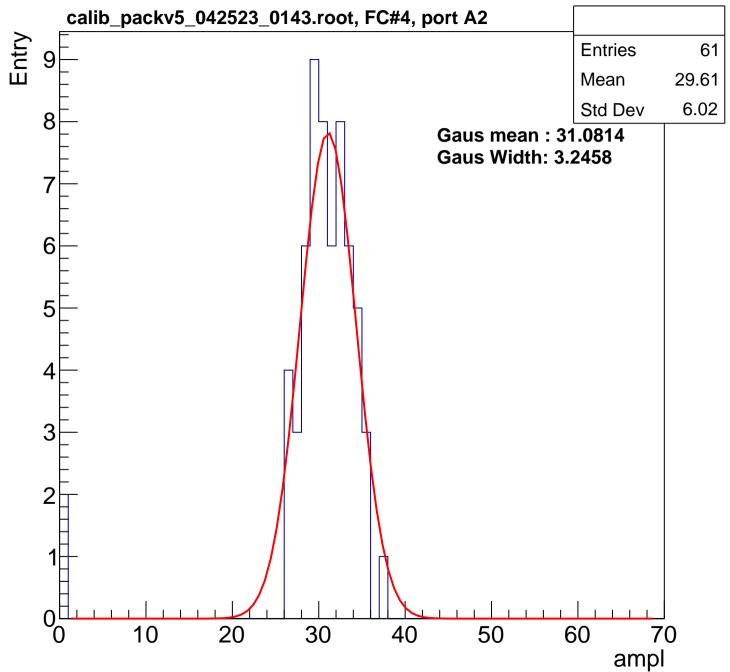


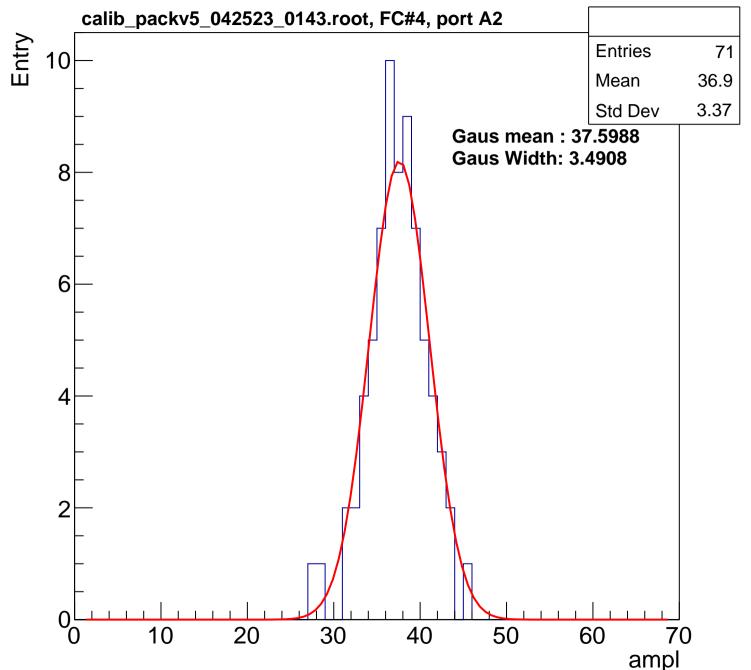


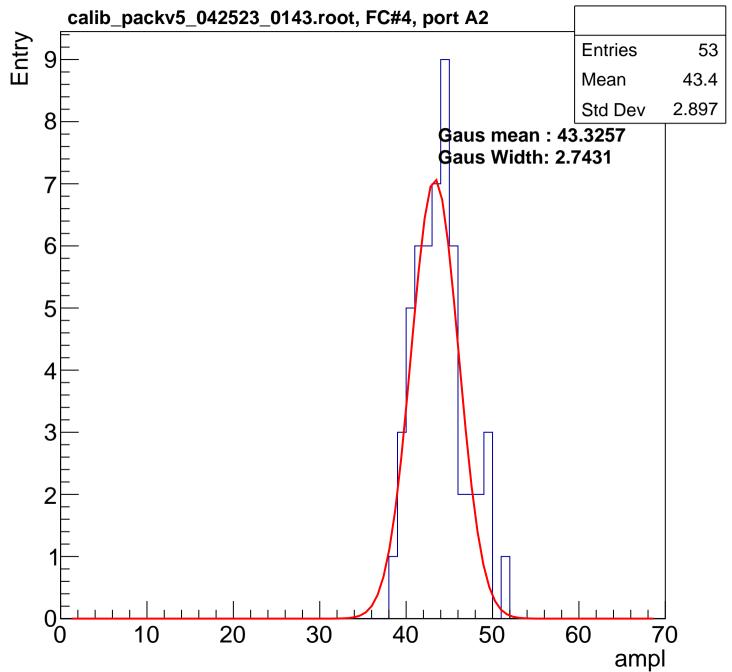


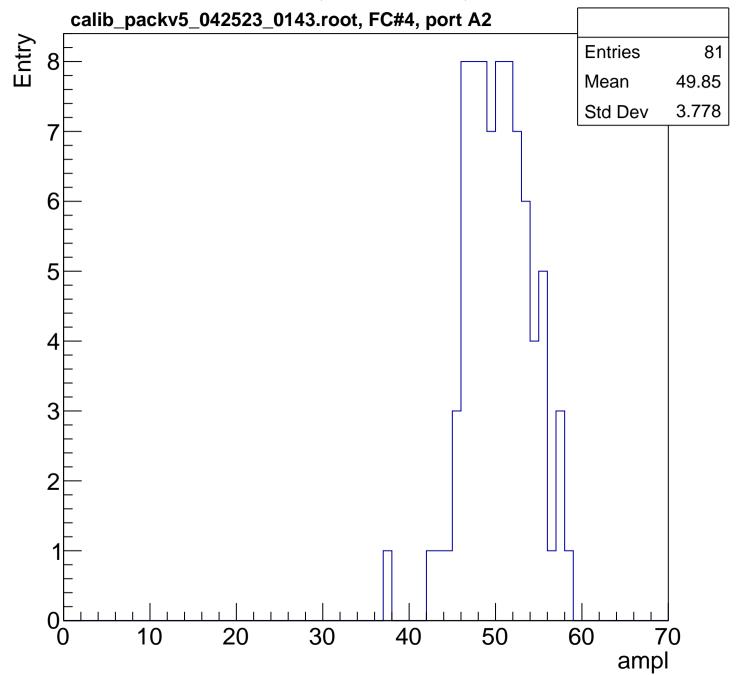
B1L100S, U8-ch57, adc7 calib_packv5_042523_0143.root, FC#4, port A2 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2

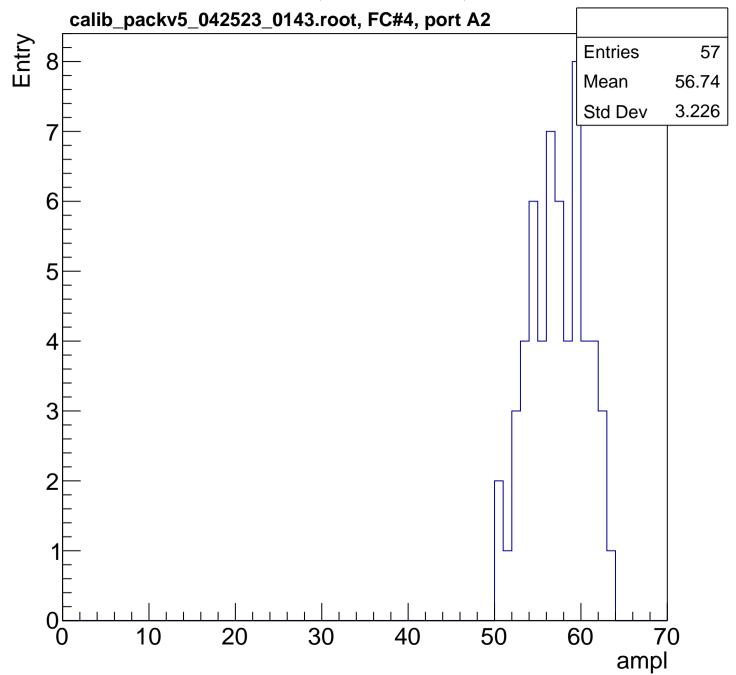


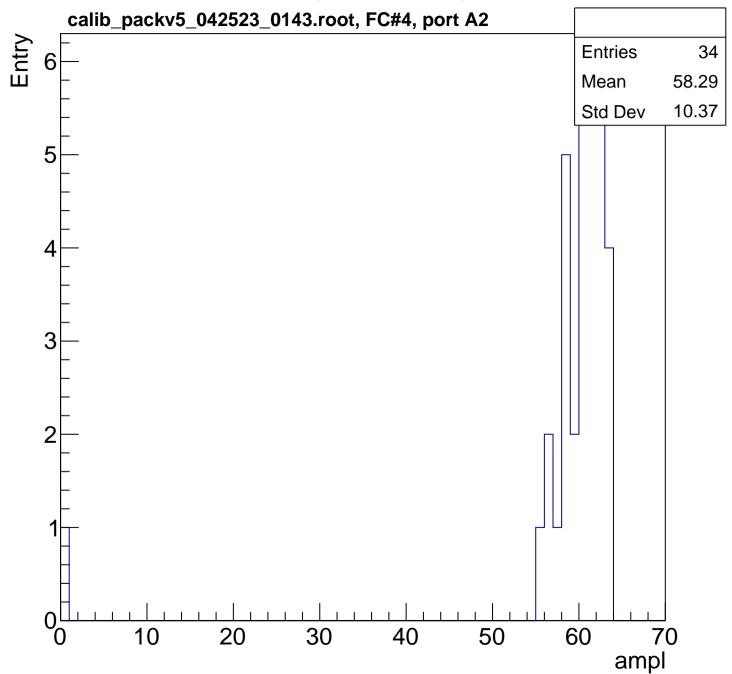


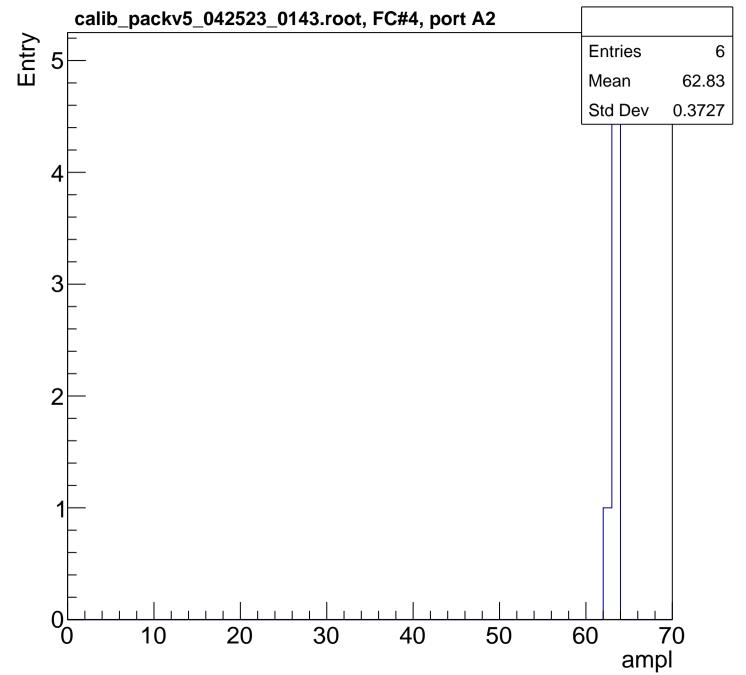




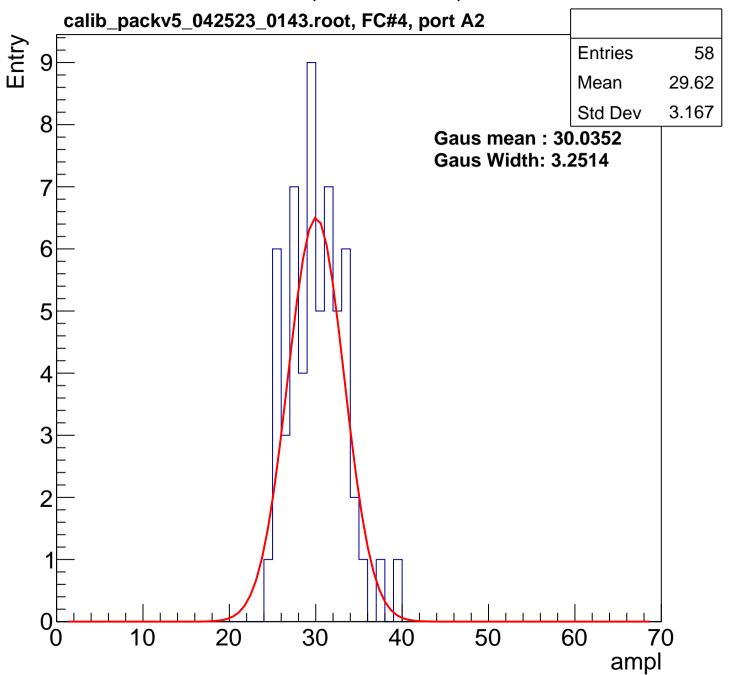


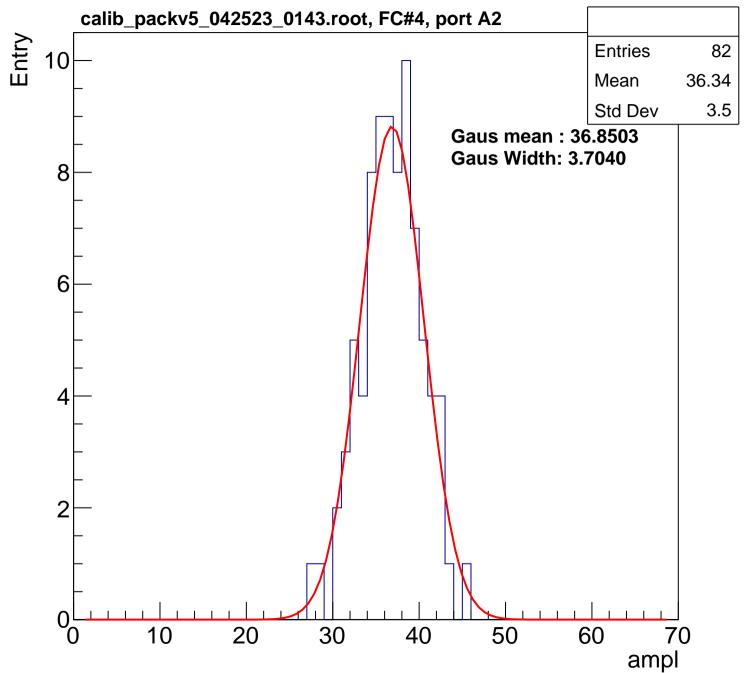


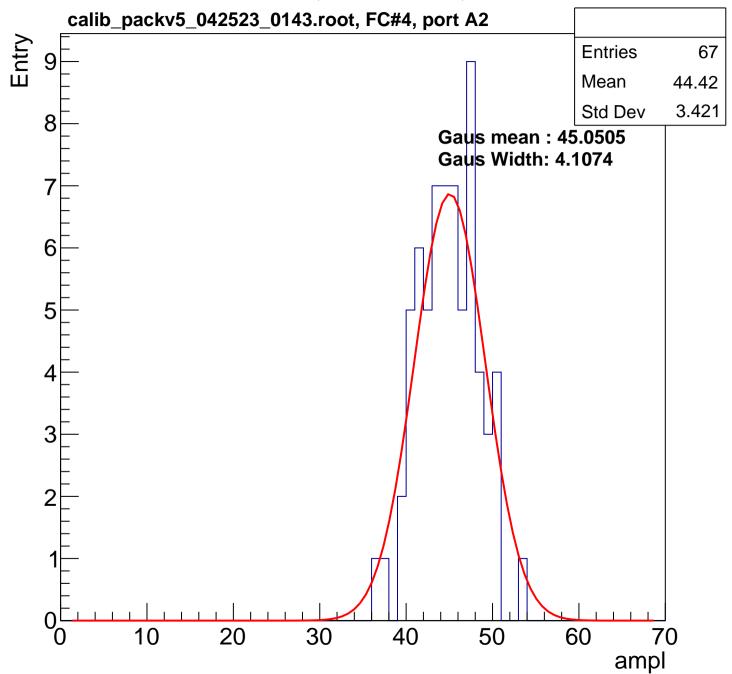


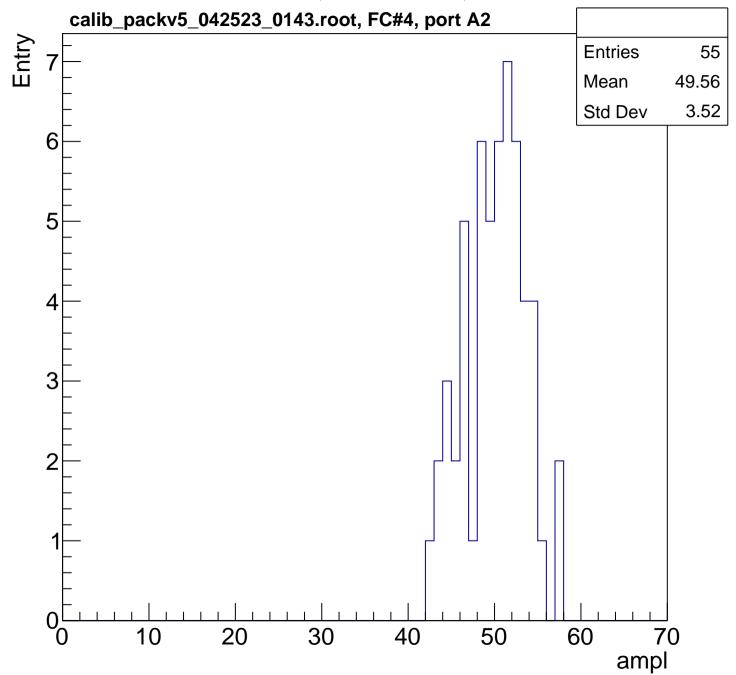


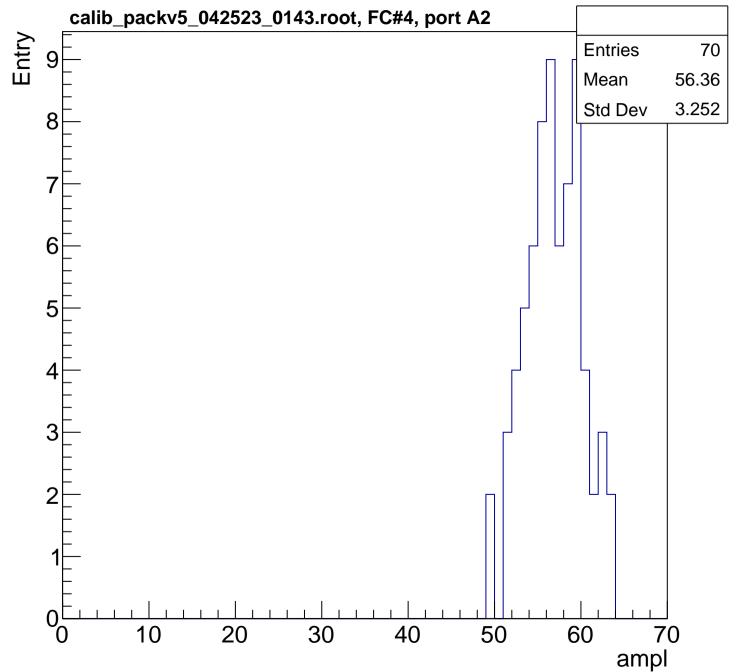


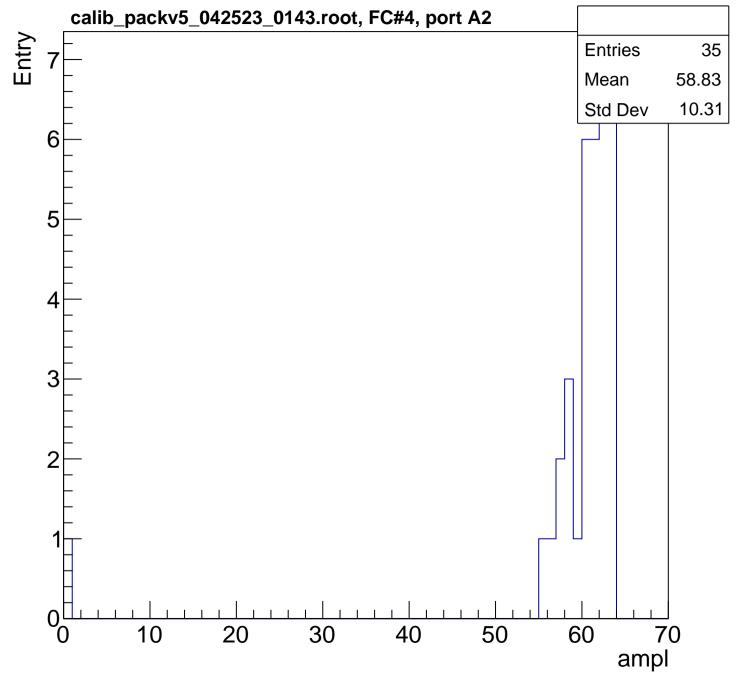


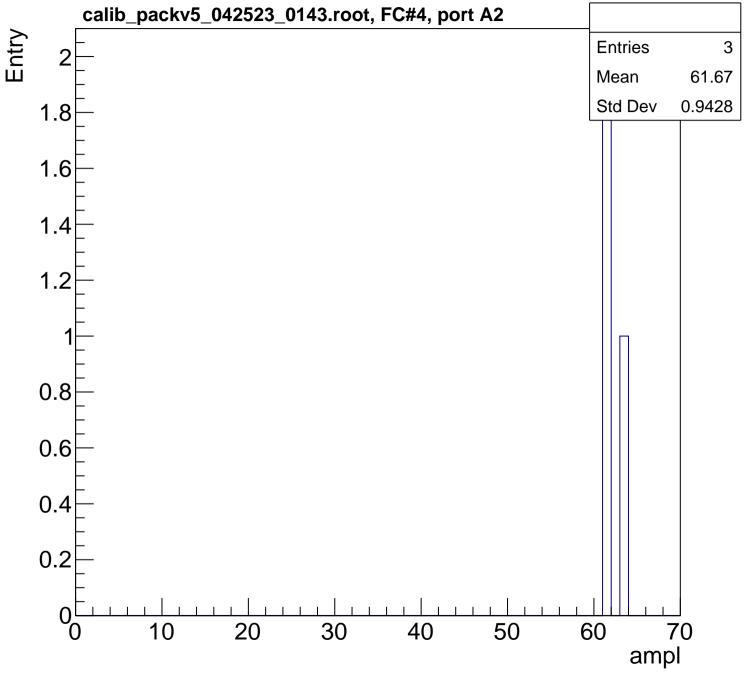




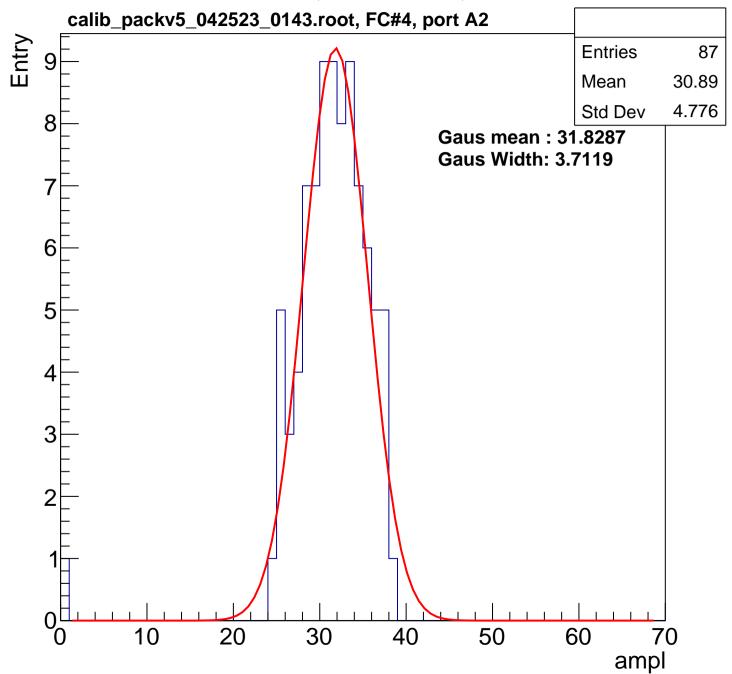


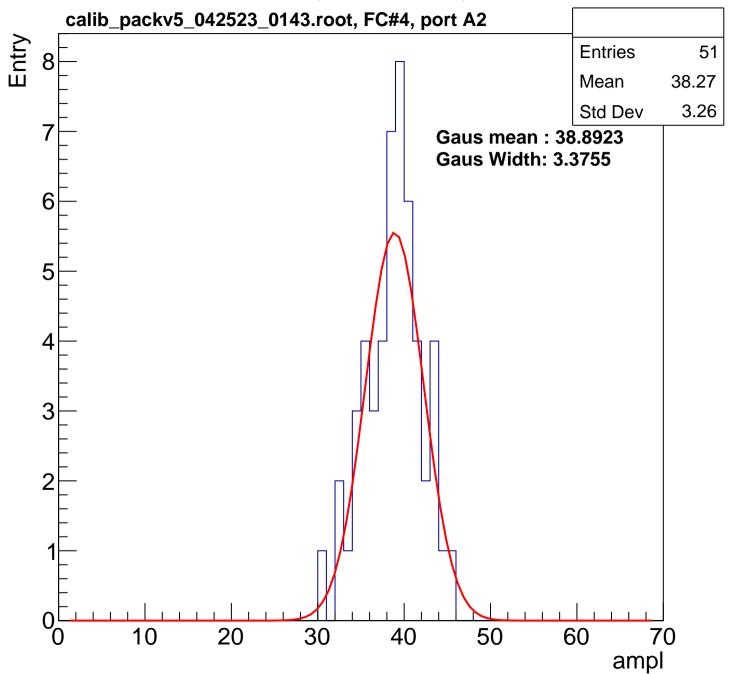


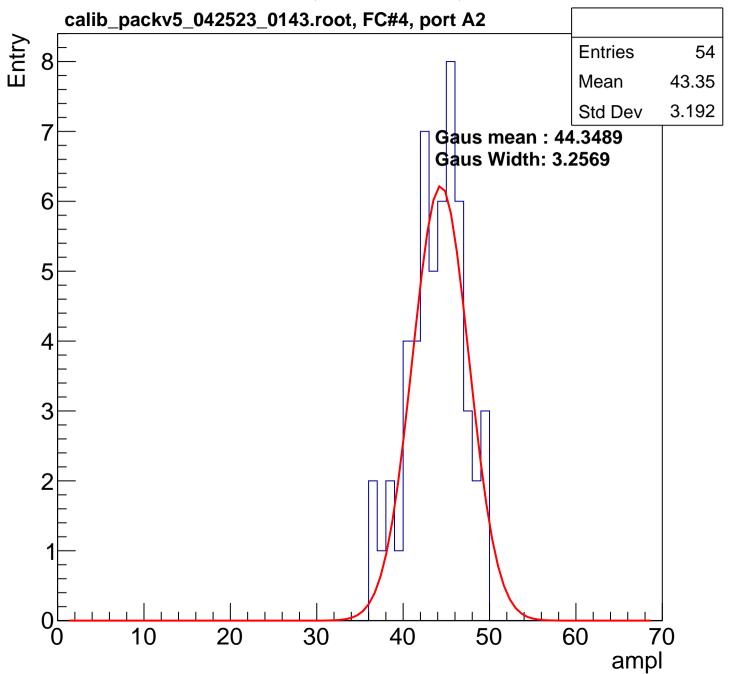




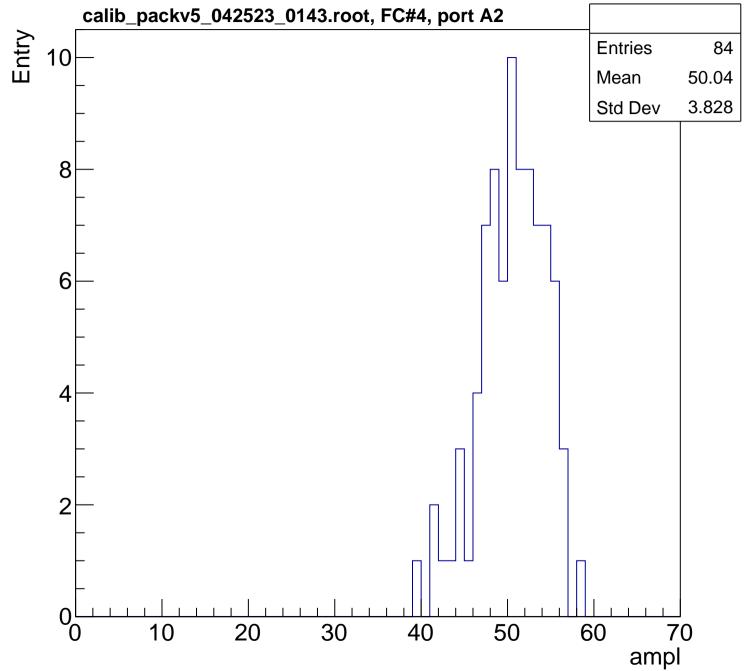


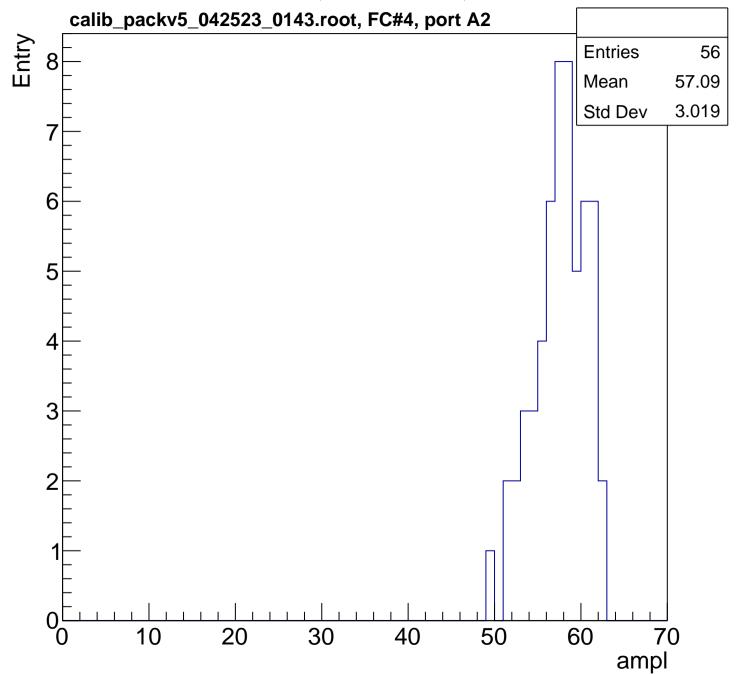


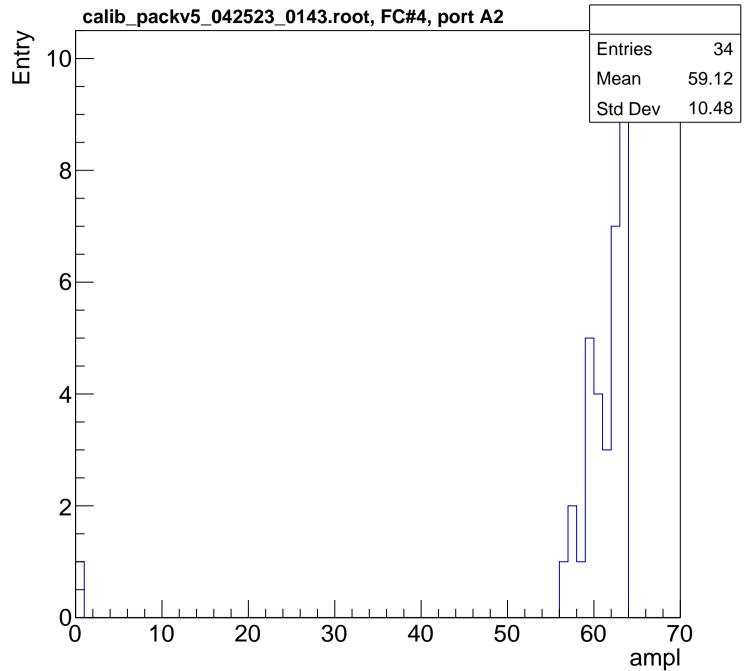


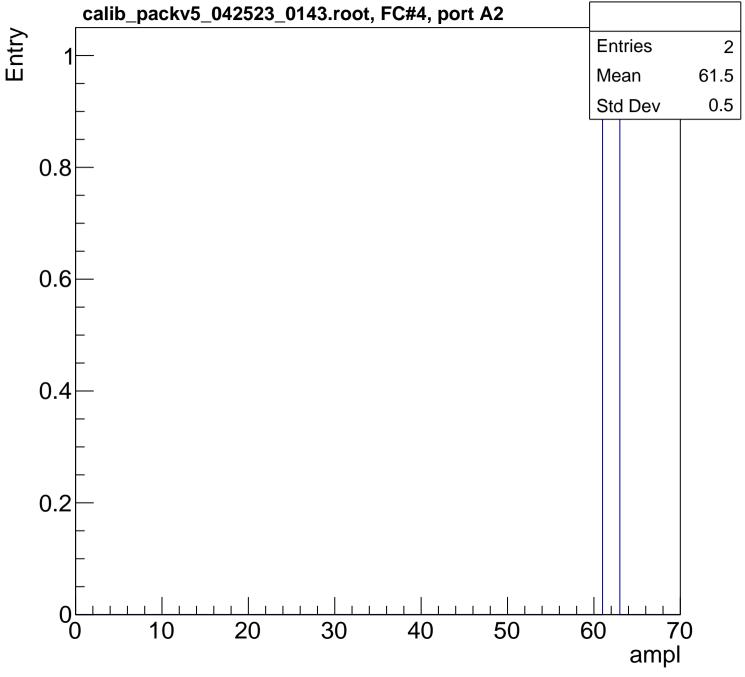


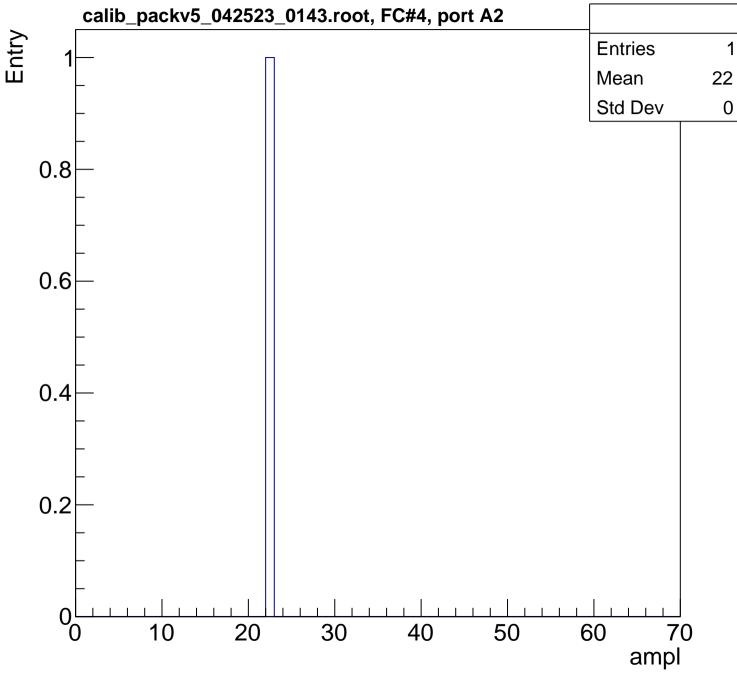
B1L100S, U8-ch60, adc3

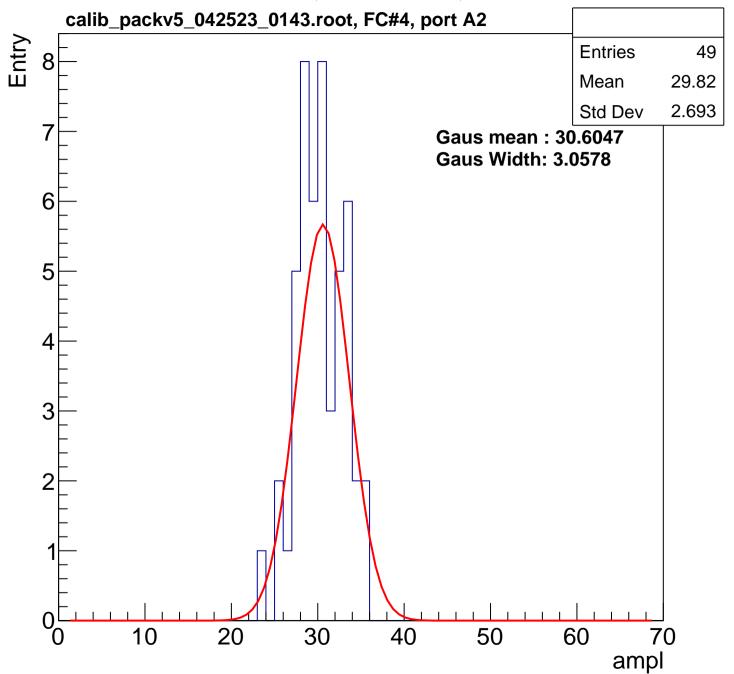


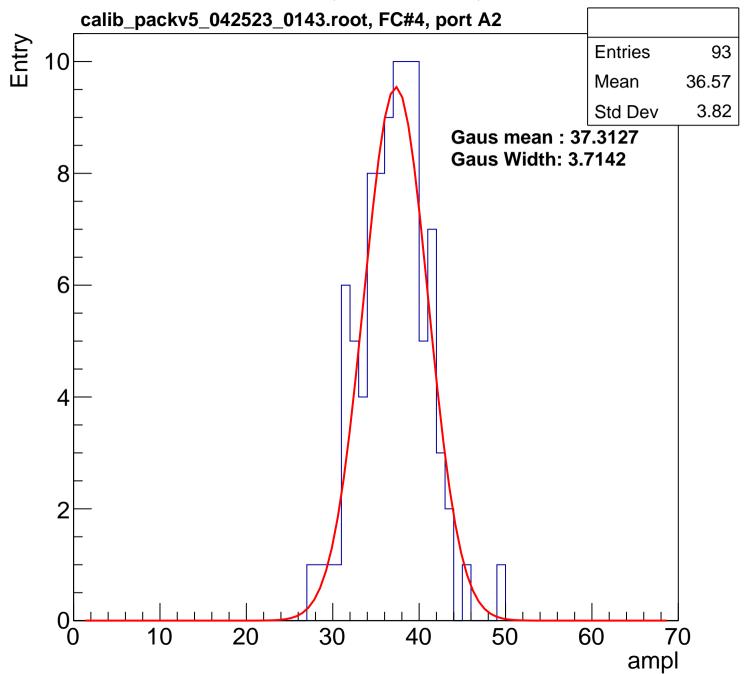


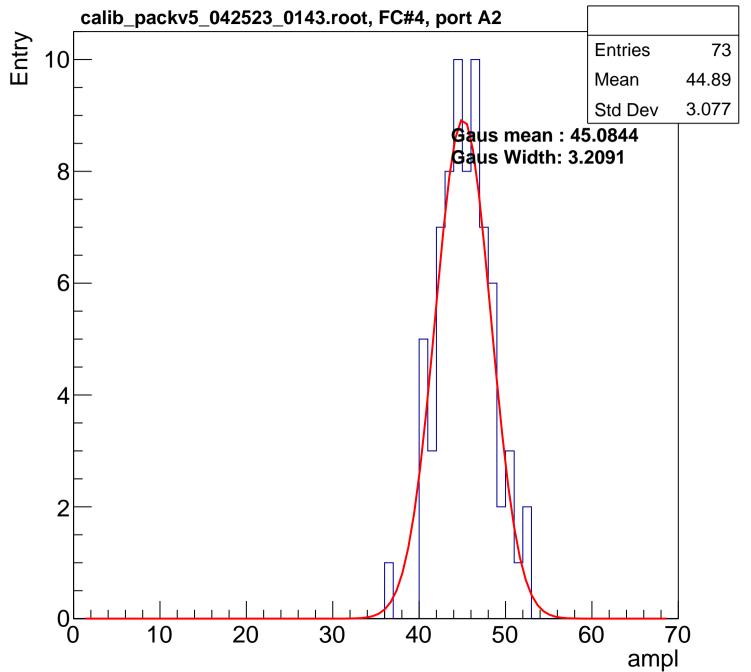


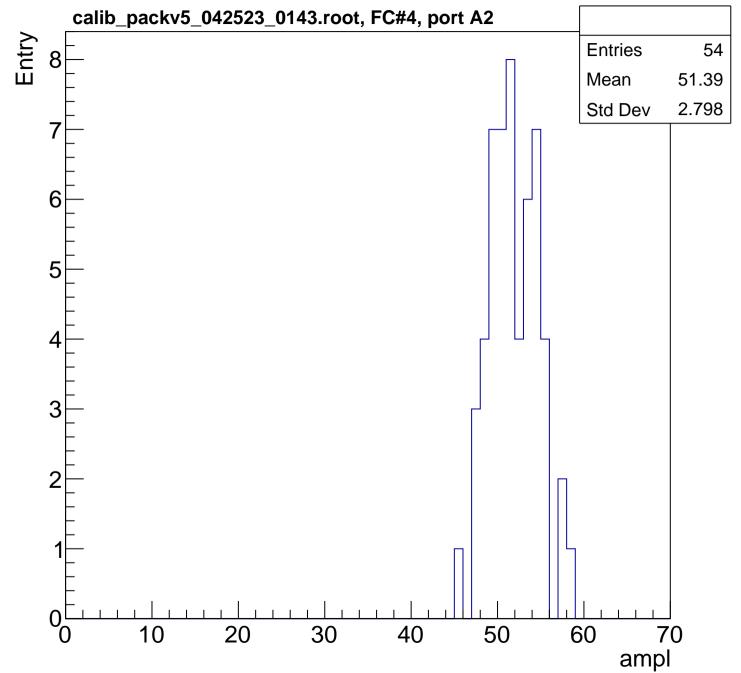


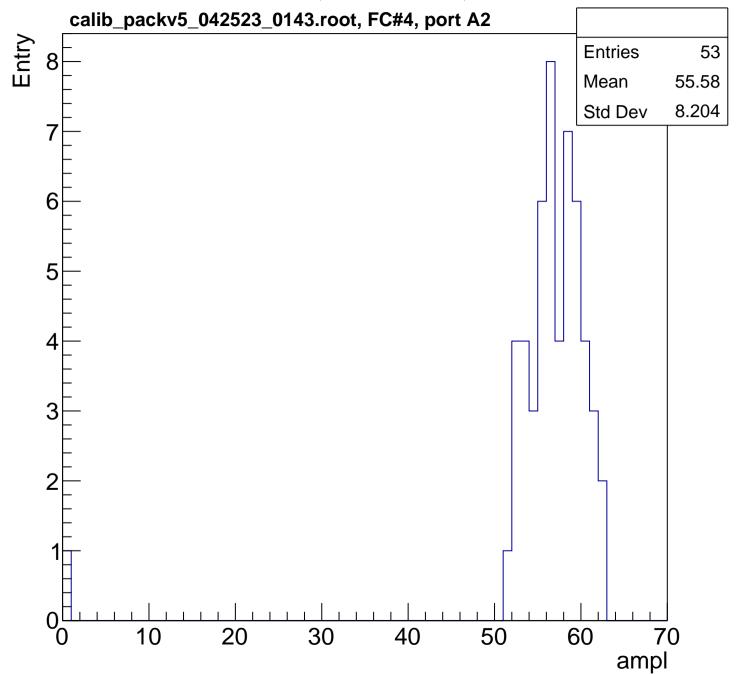


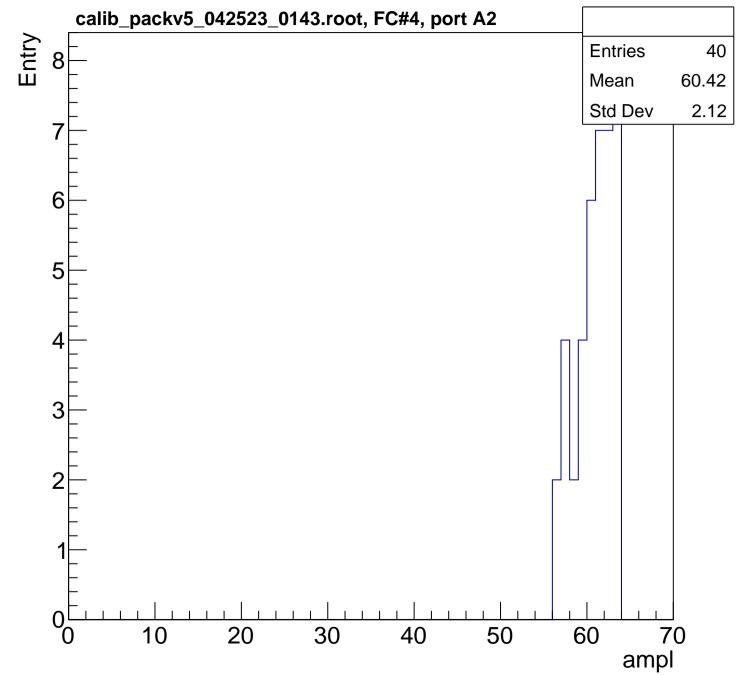






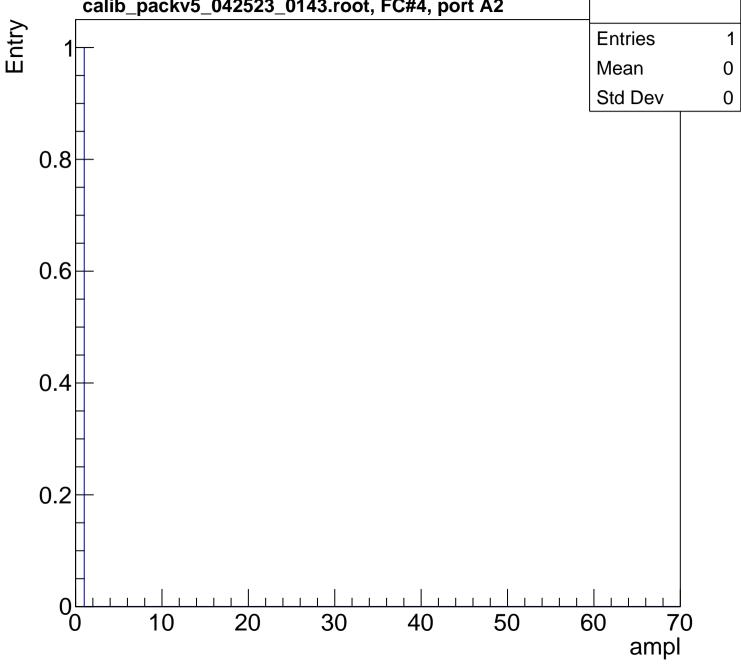


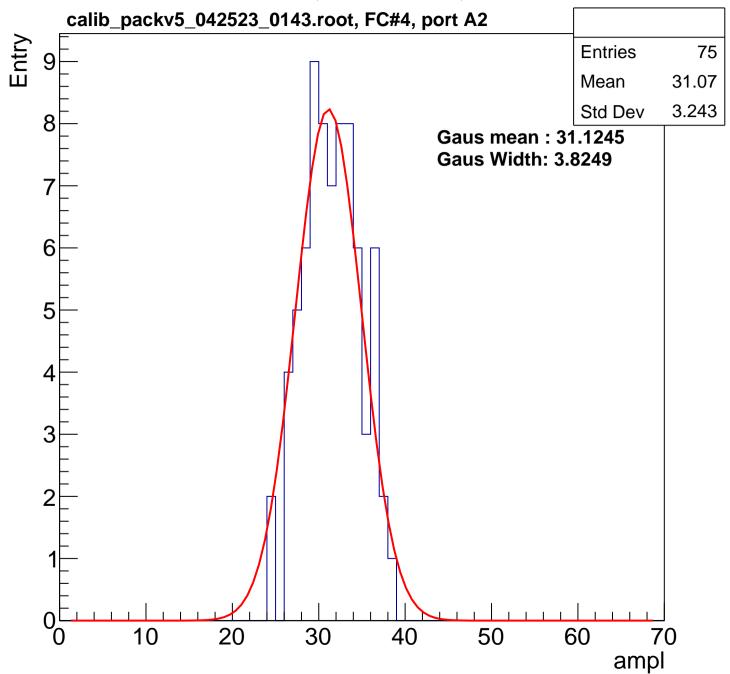


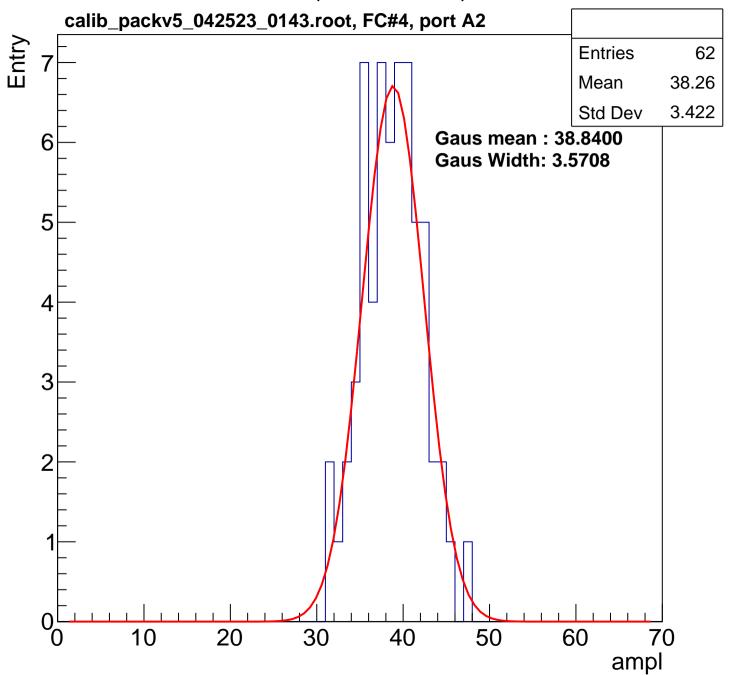


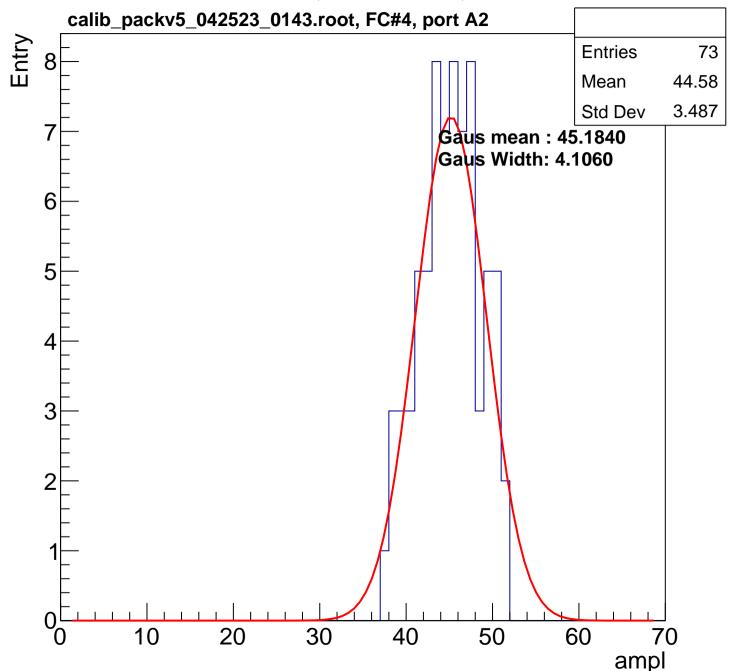


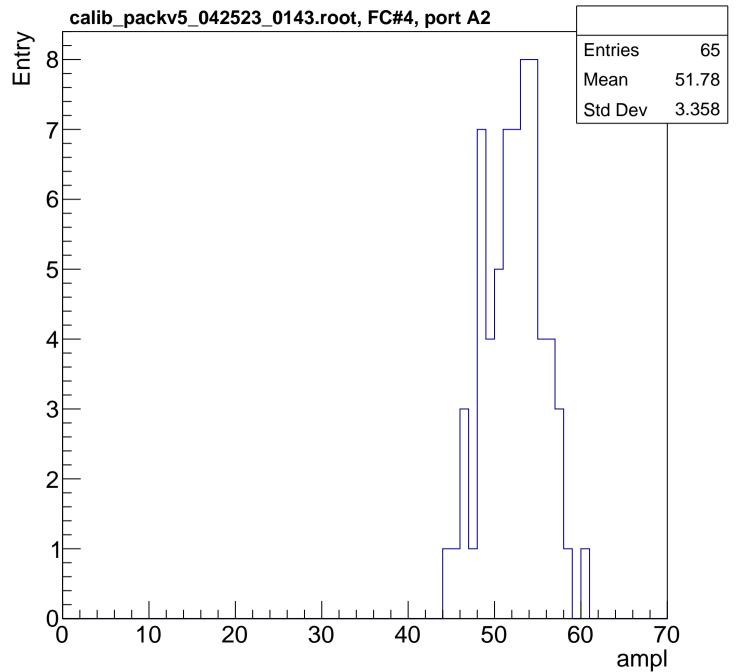
B1L100S, U8-ch61, adc7 calib_packv5_042523_0143.root, FC#4, port A2

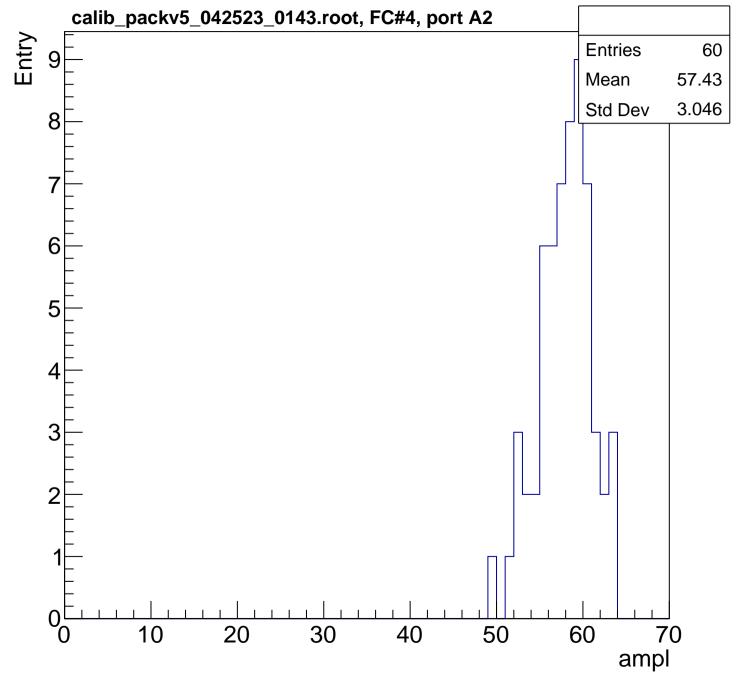


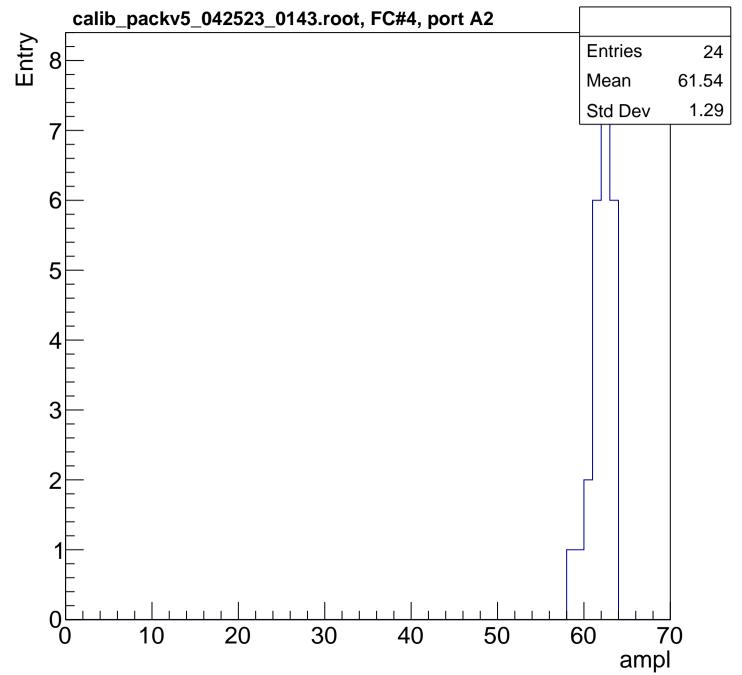


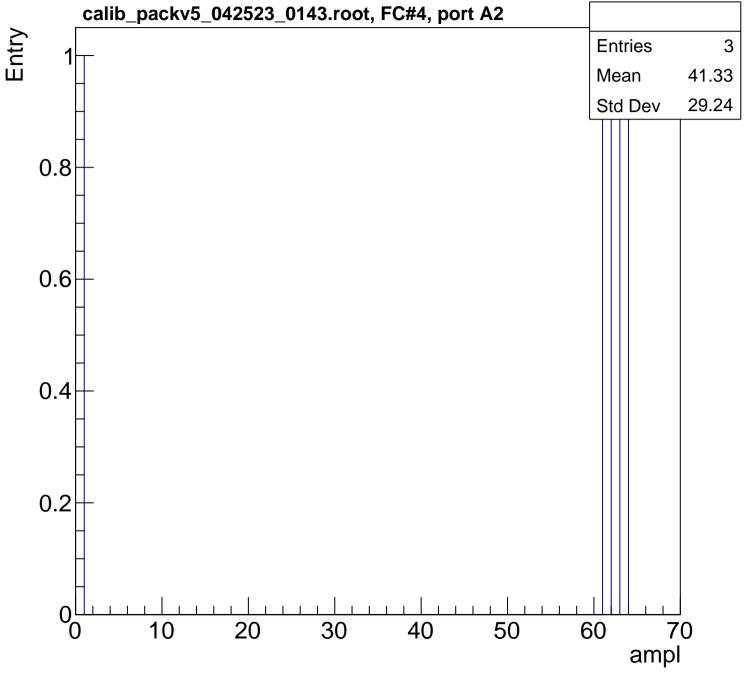


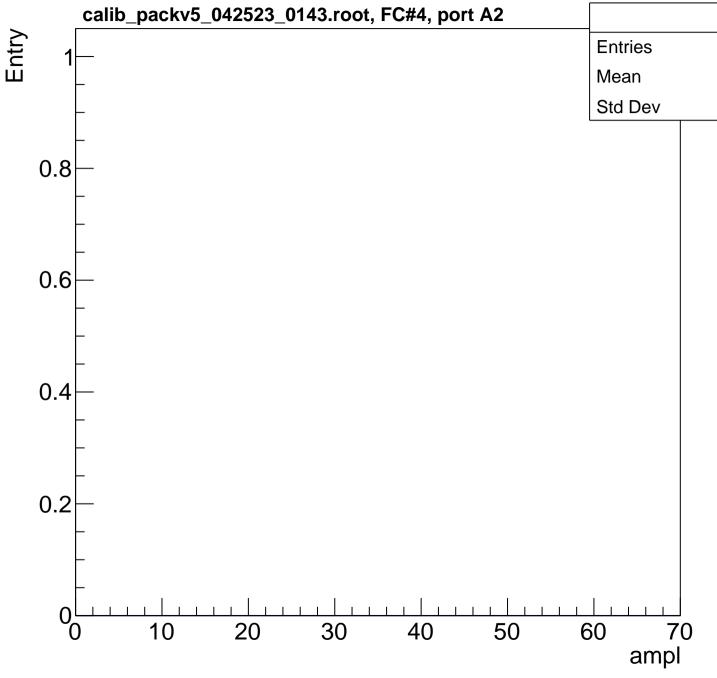


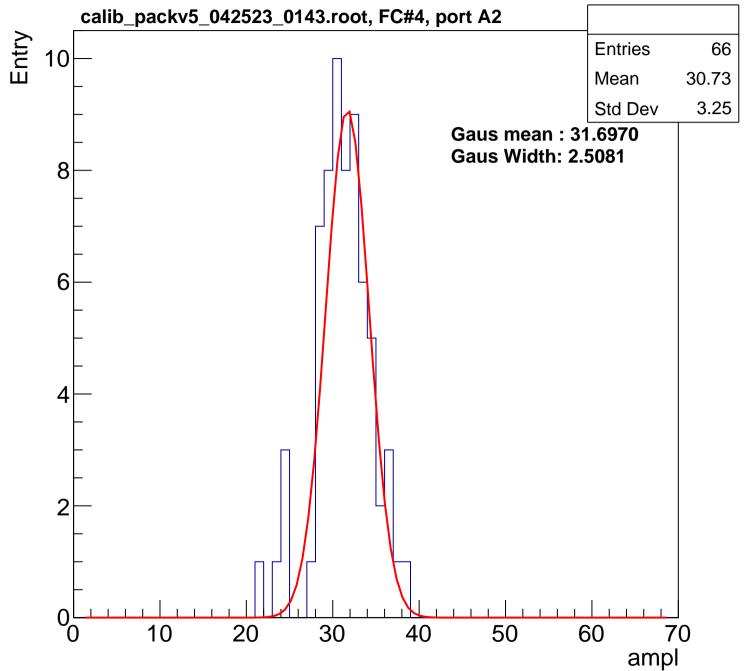


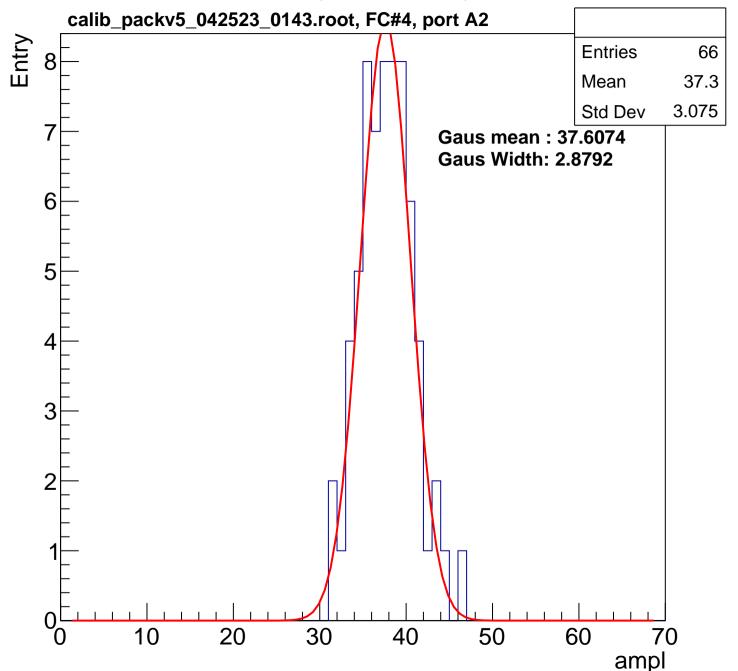


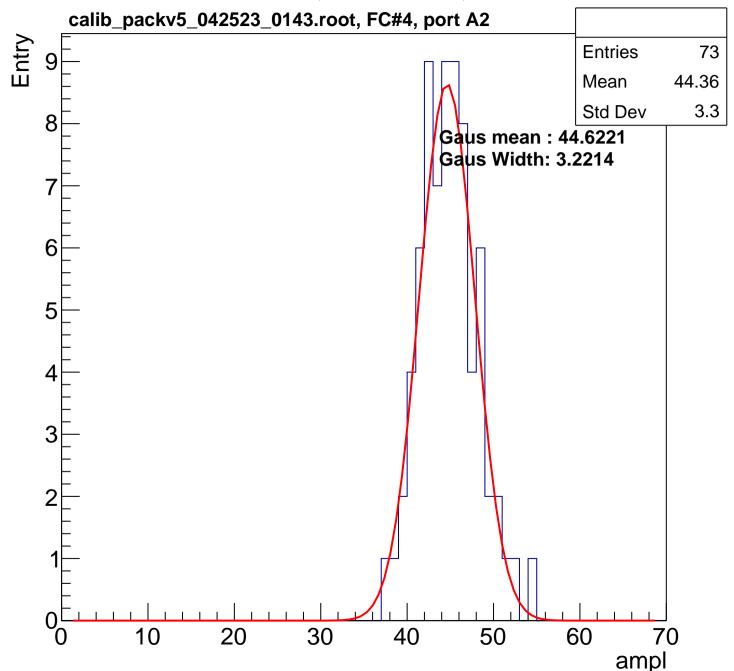


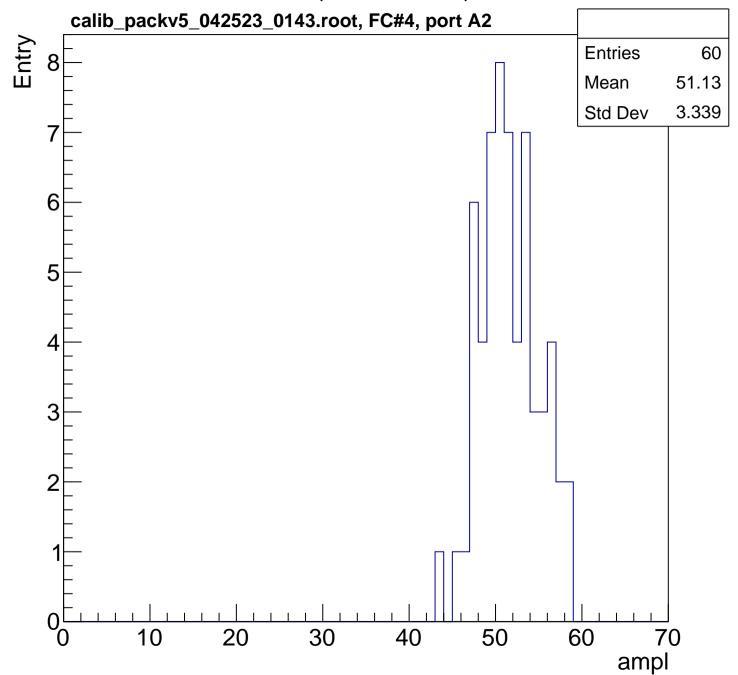


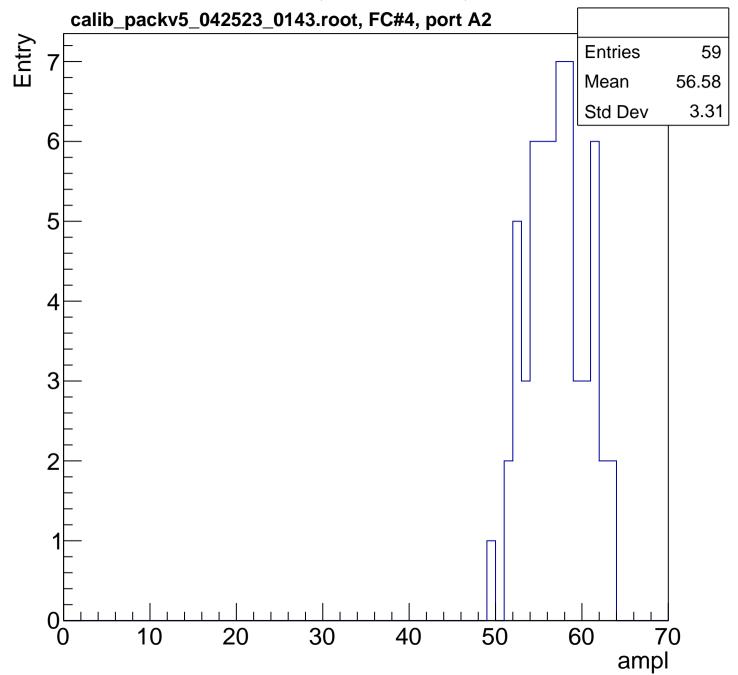


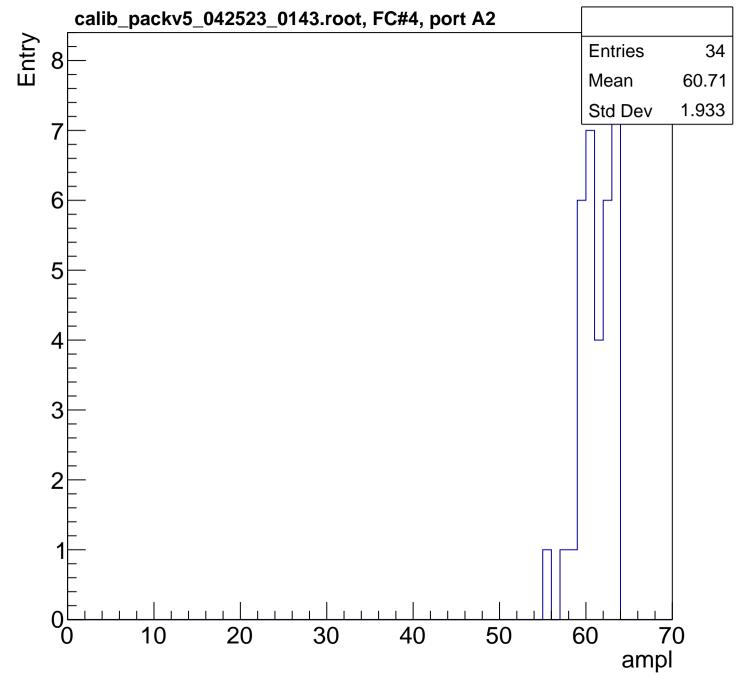


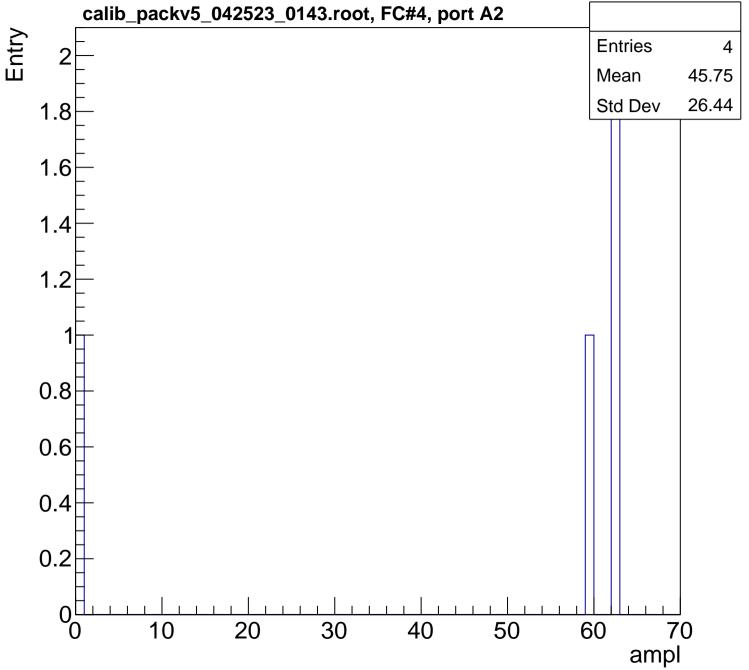




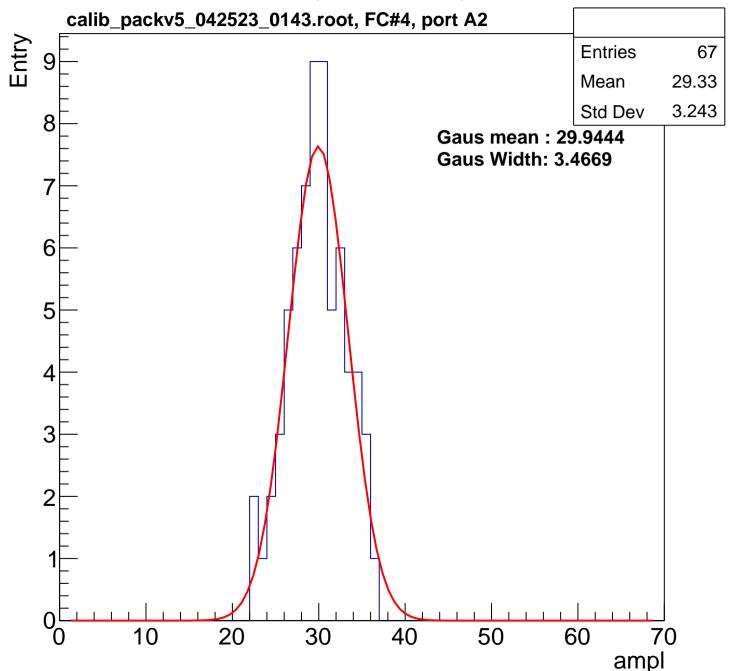


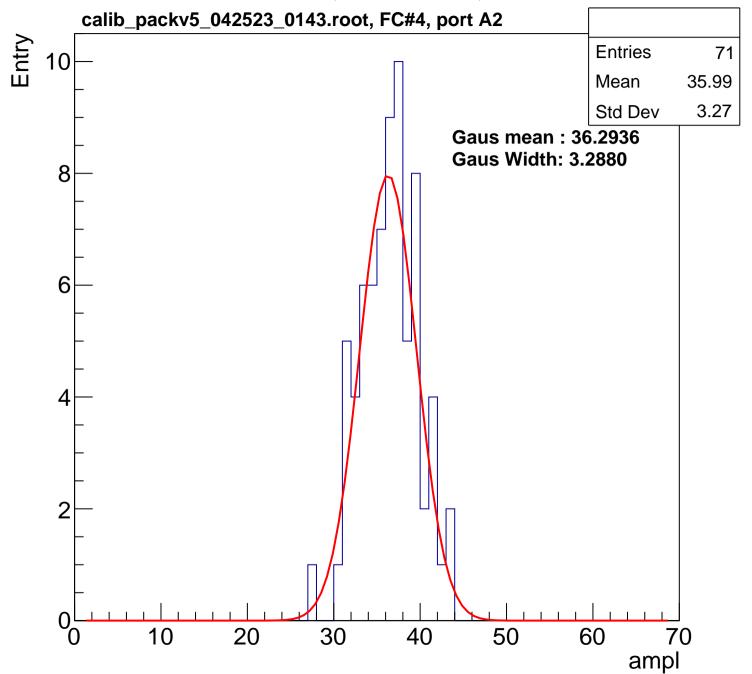


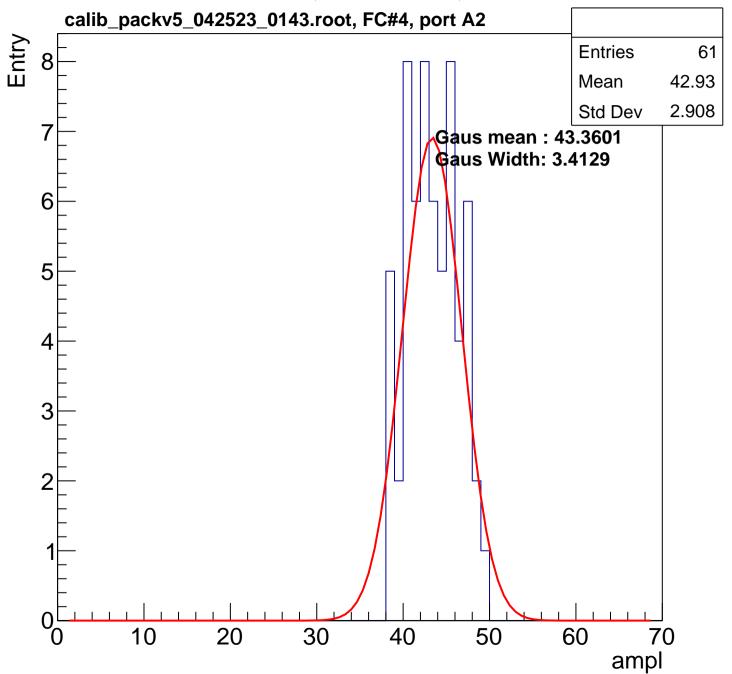


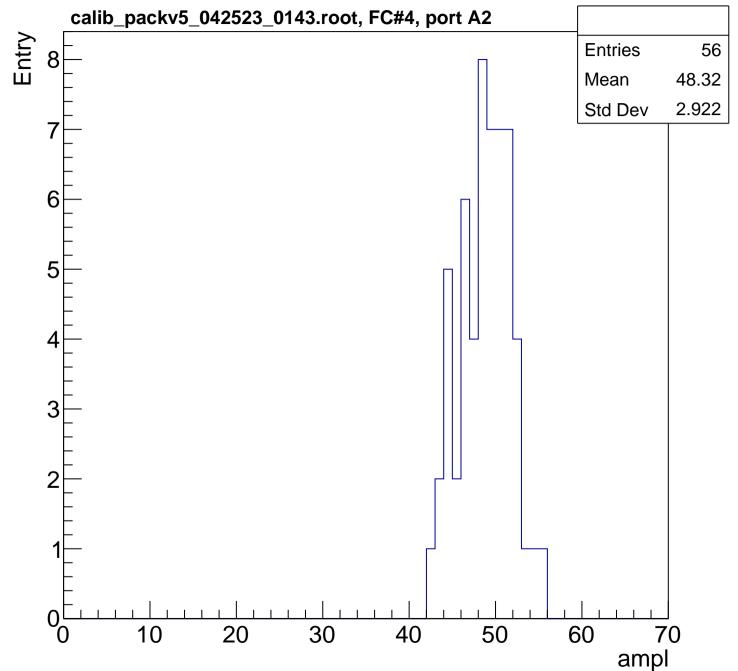


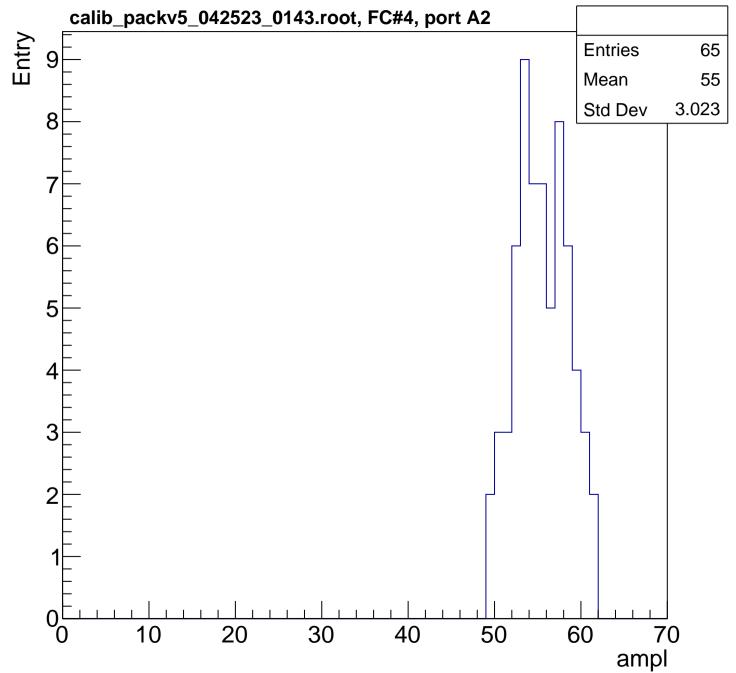


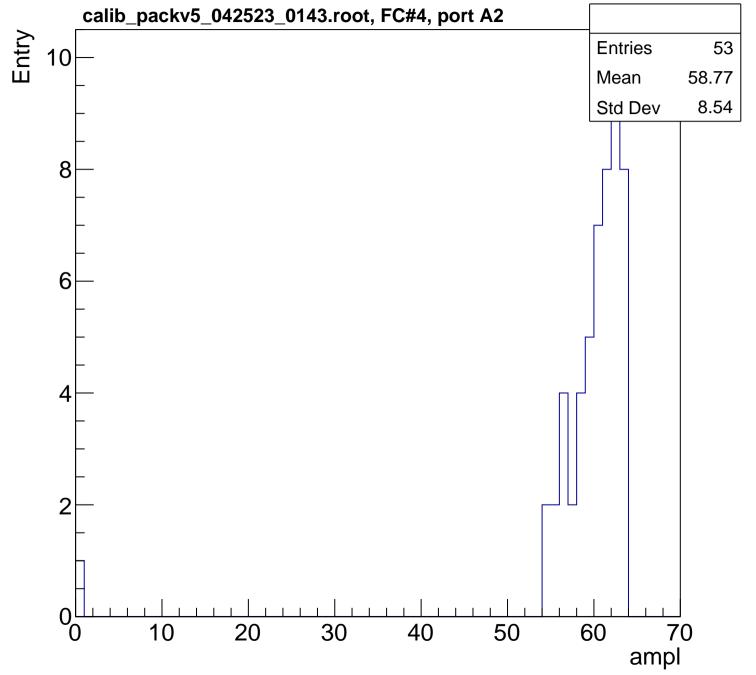


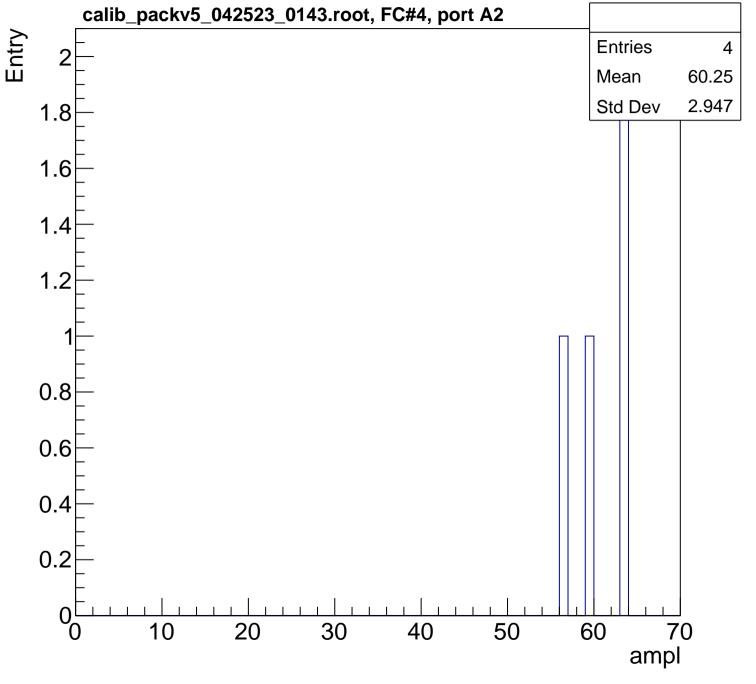


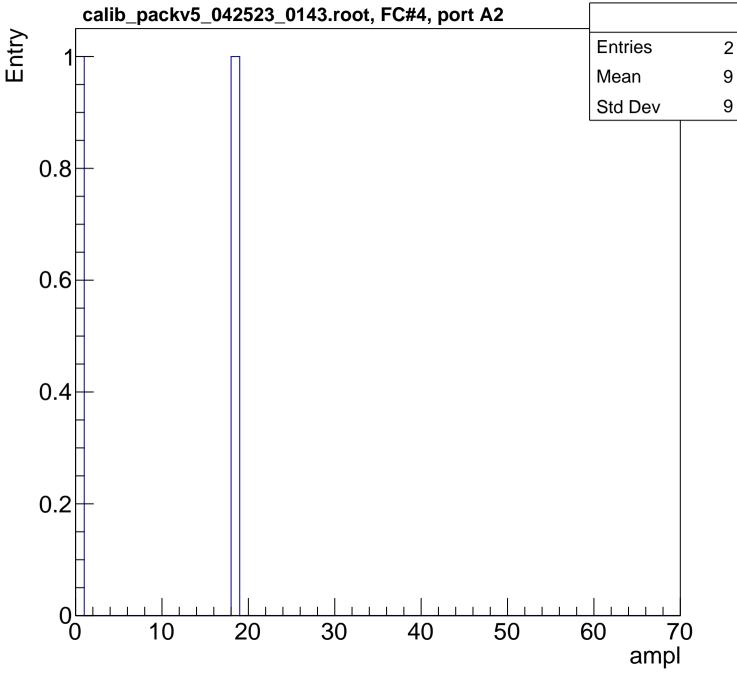


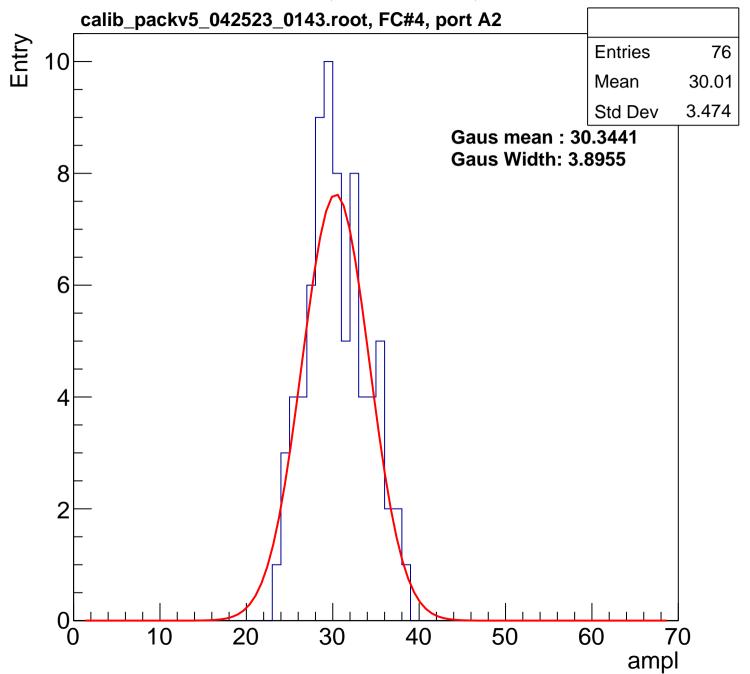


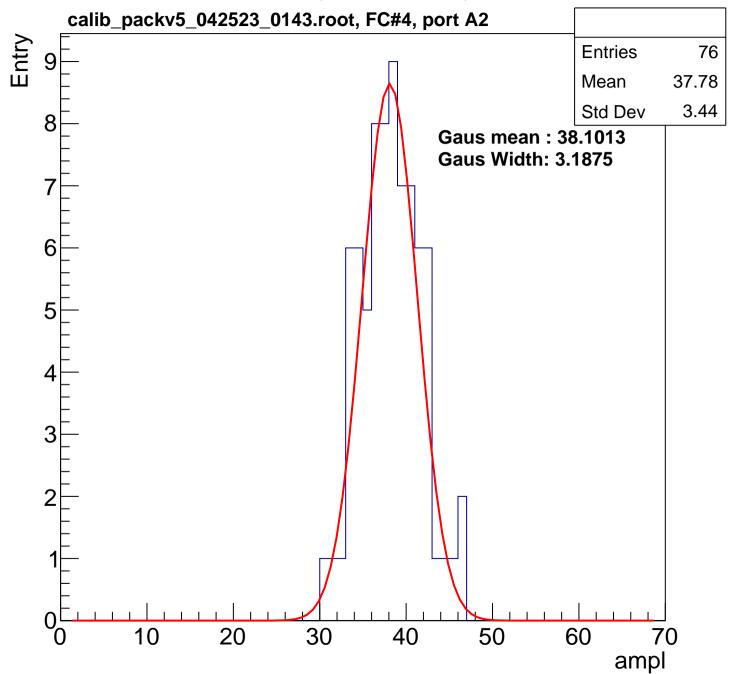


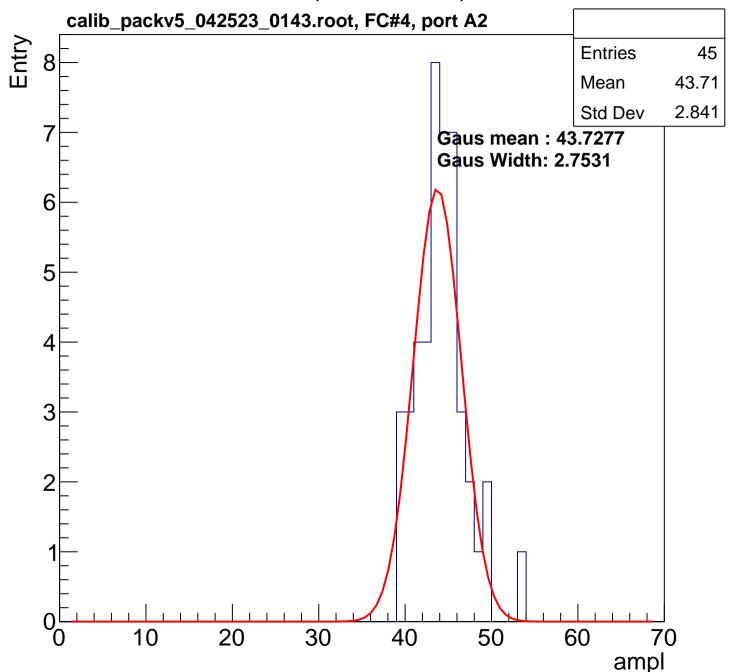


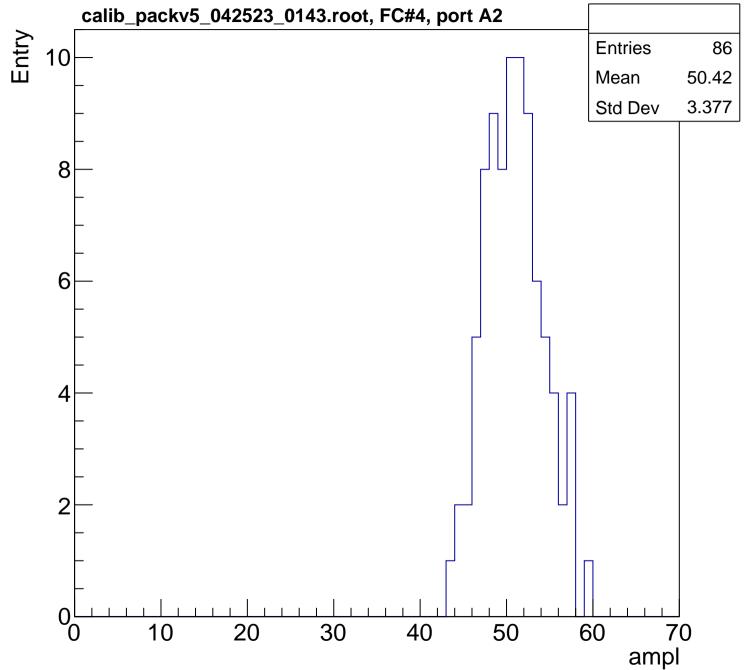


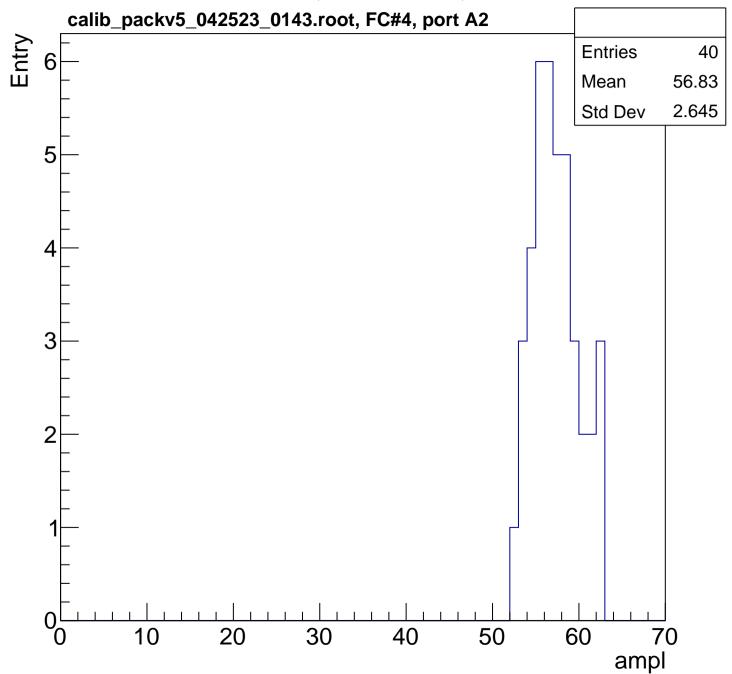


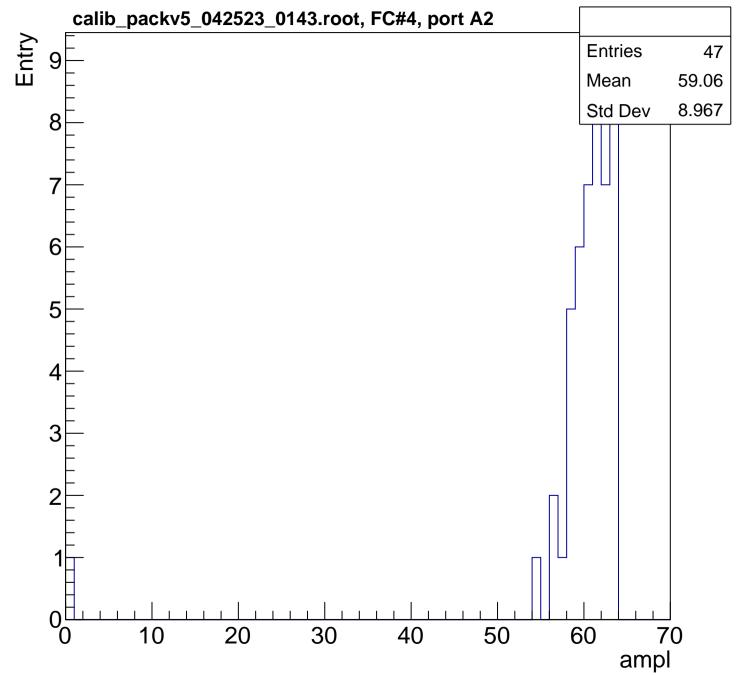


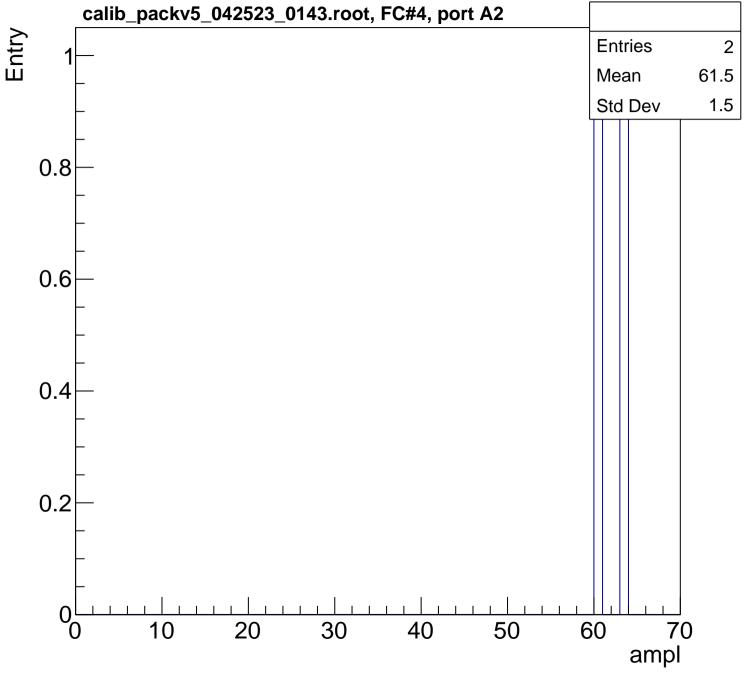




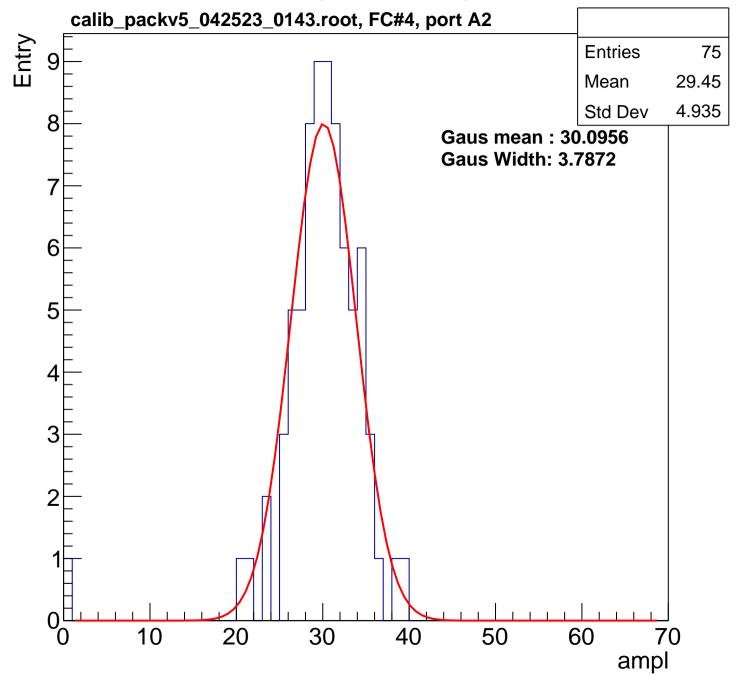


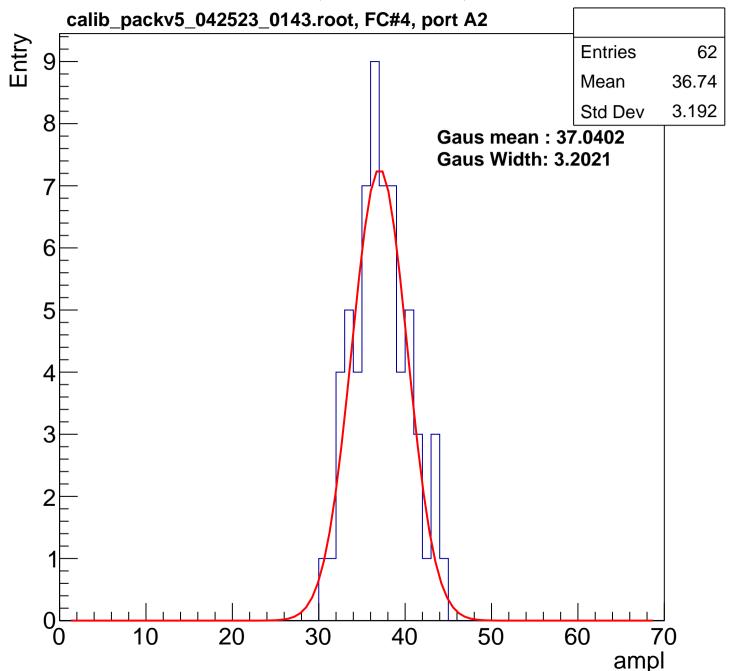


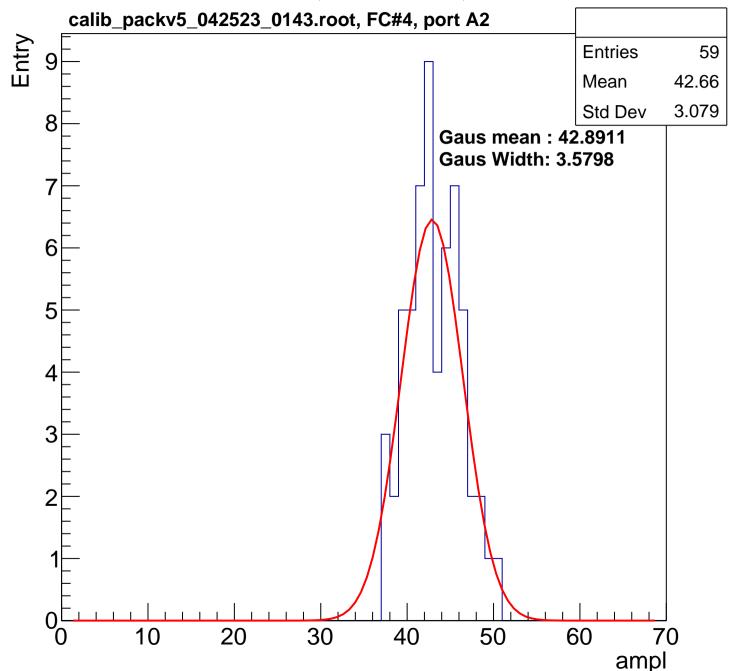


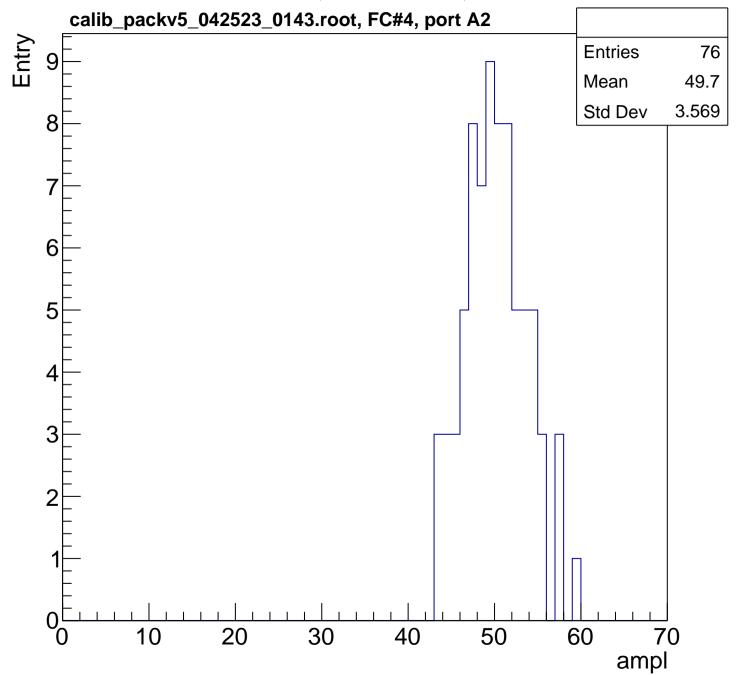


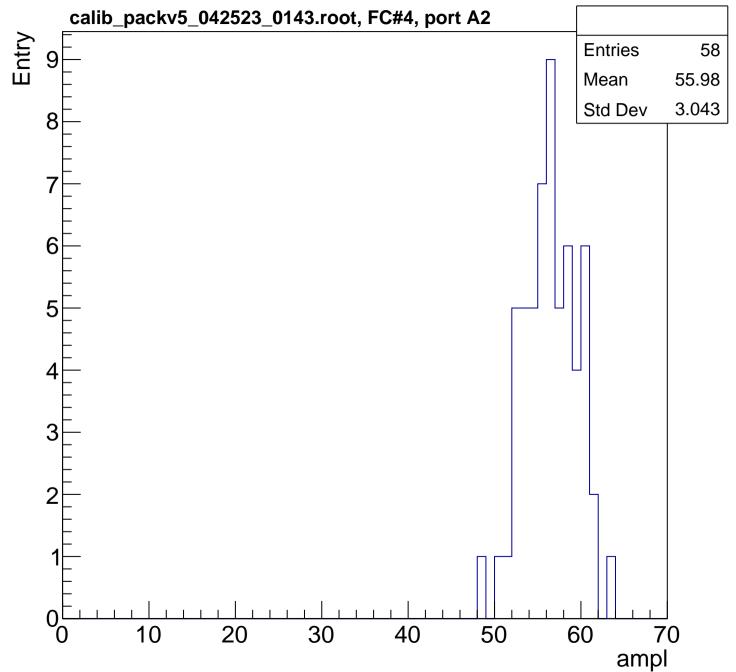


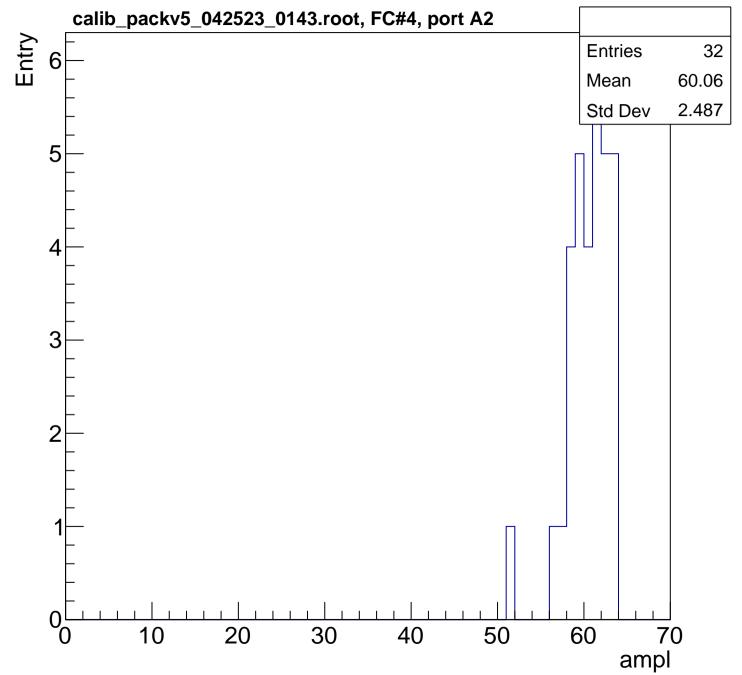


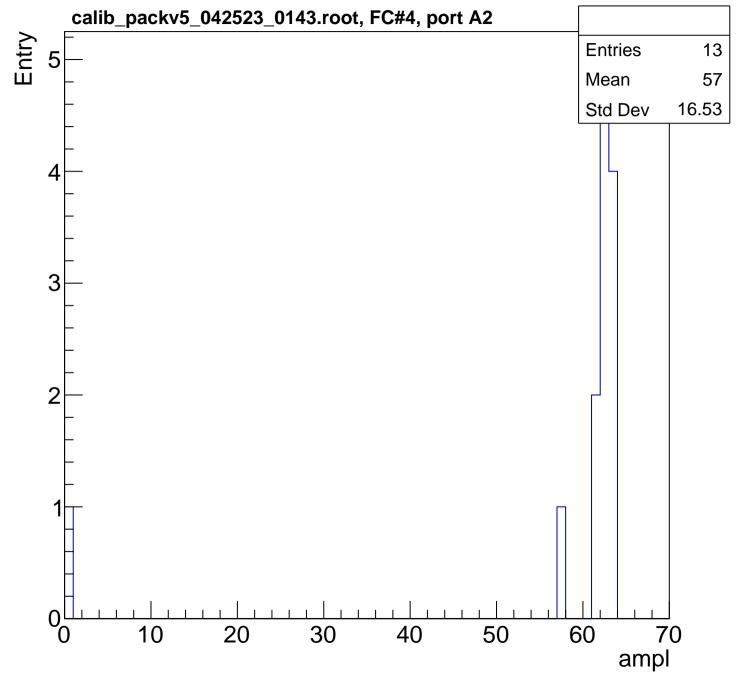




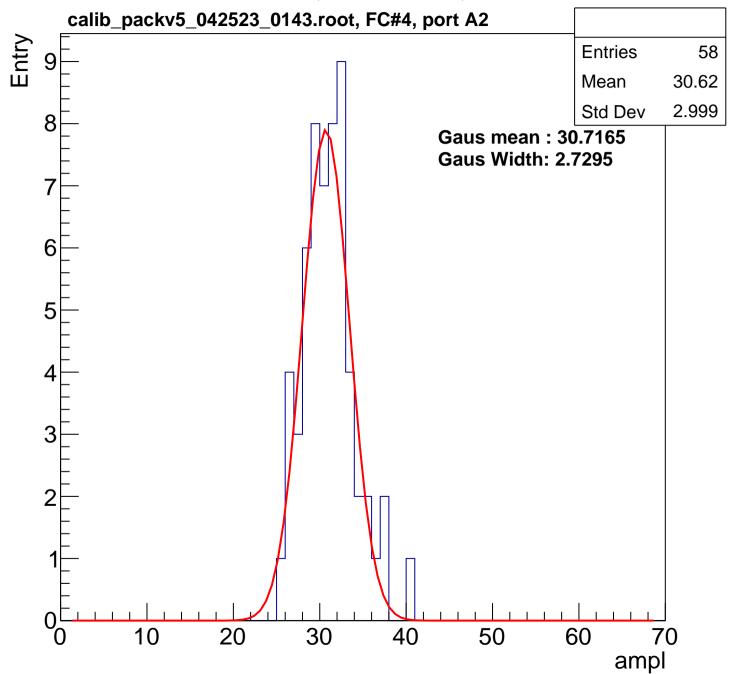


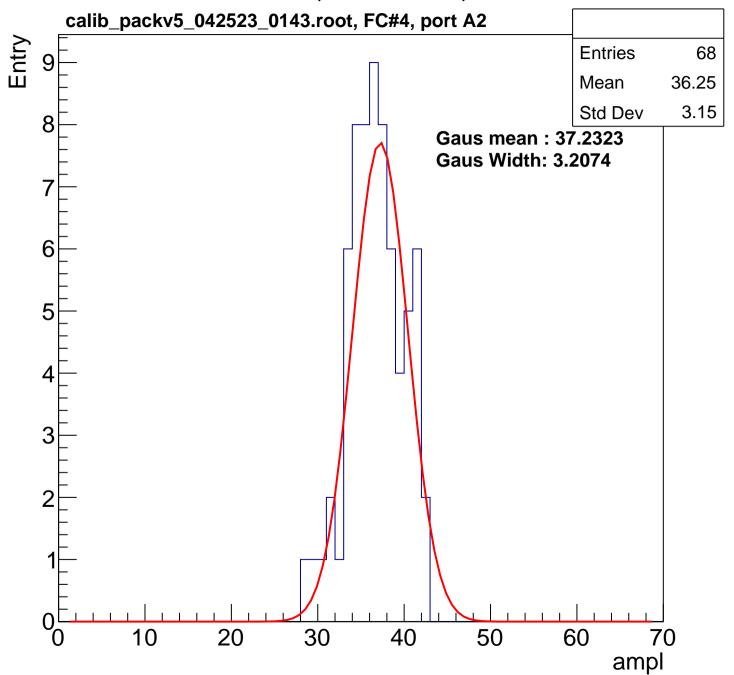


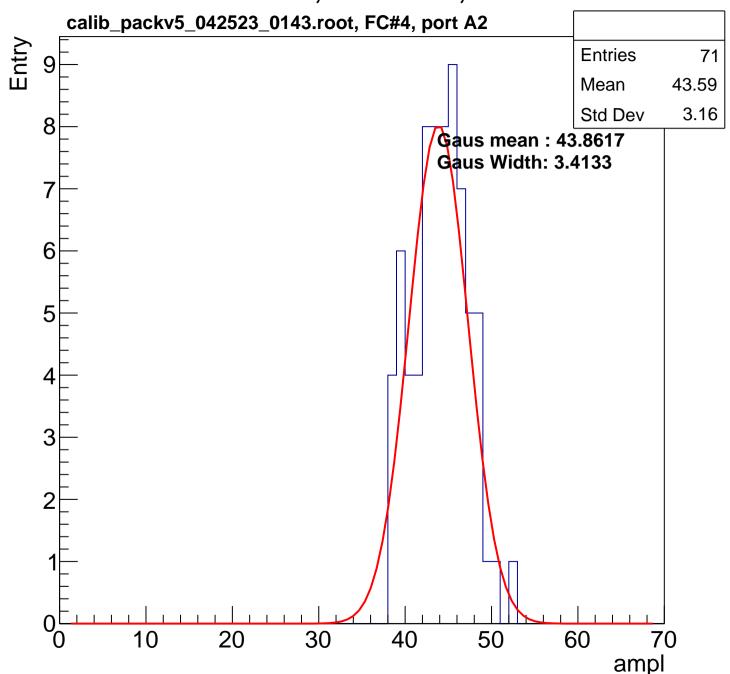


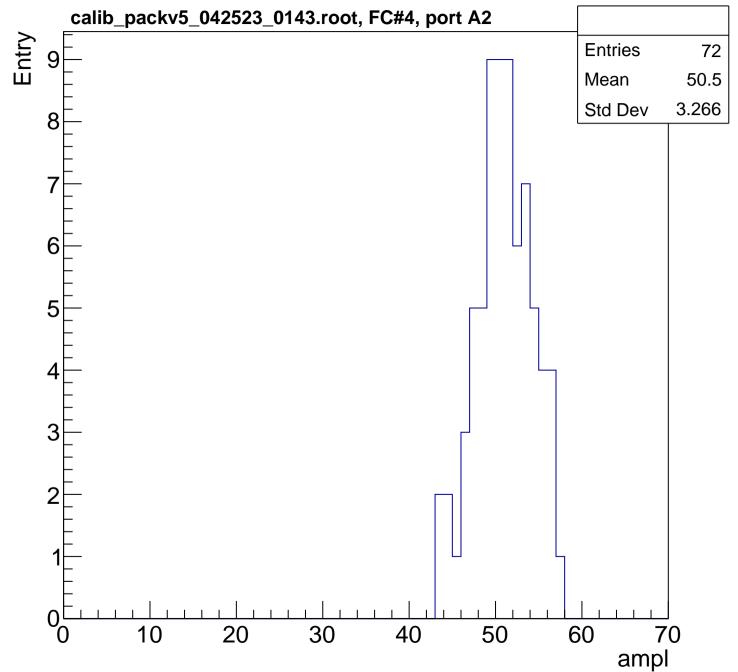


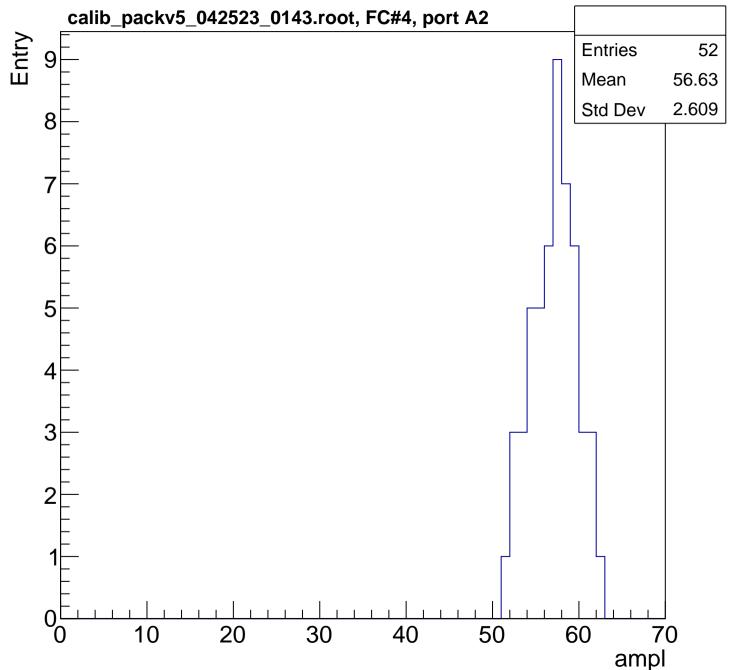
B1L100S, U8-ch66, adc7 calib_packv5_042523_0143.root, FC#4, port A2 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

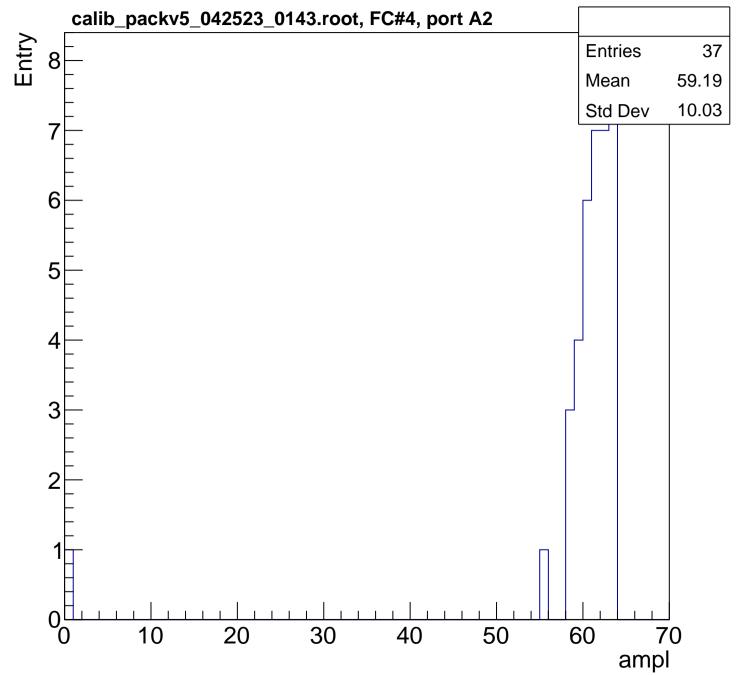


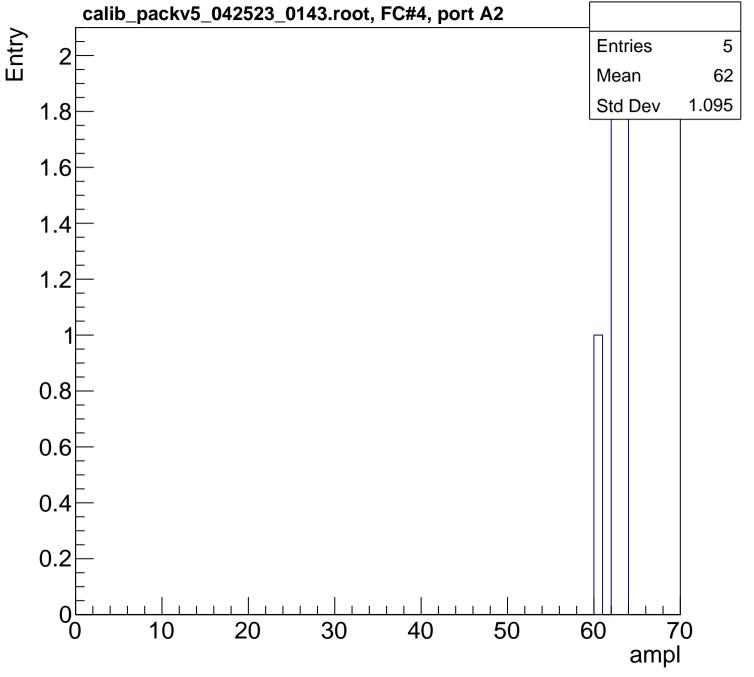




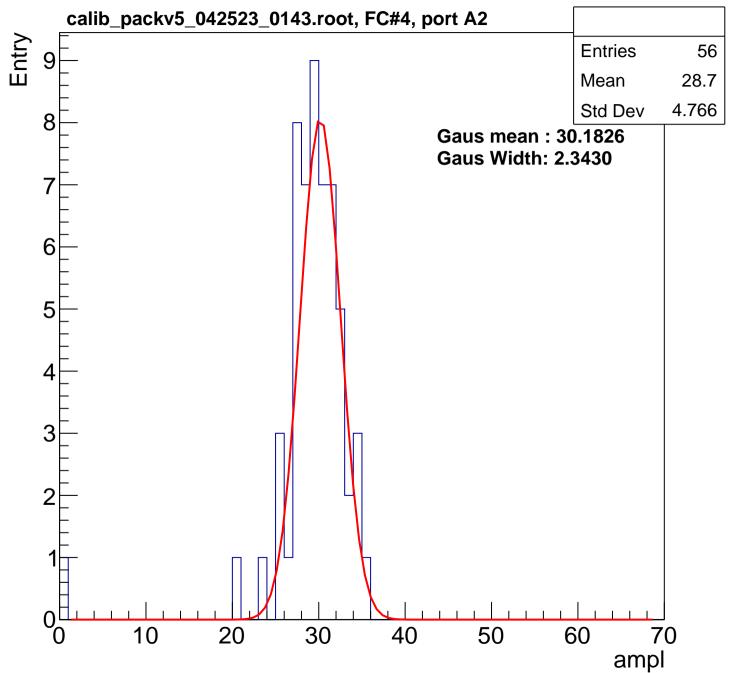


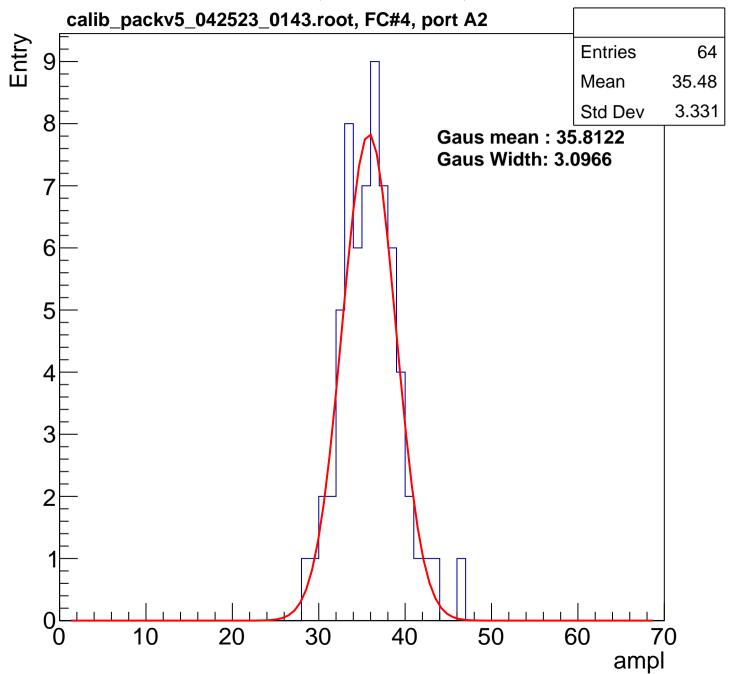


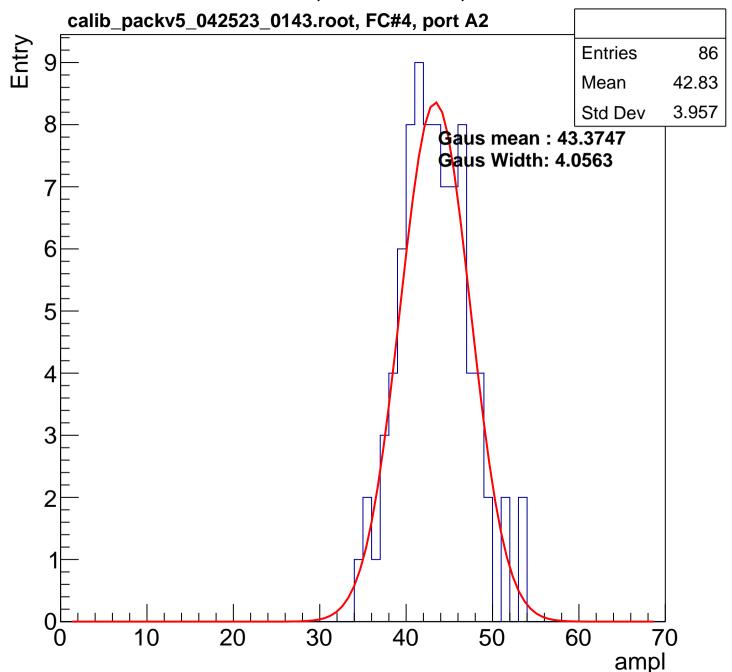


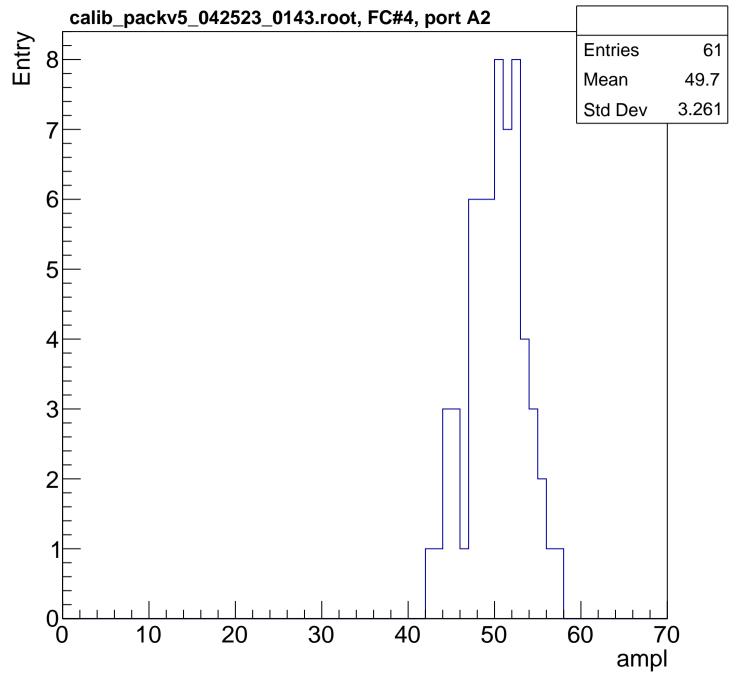


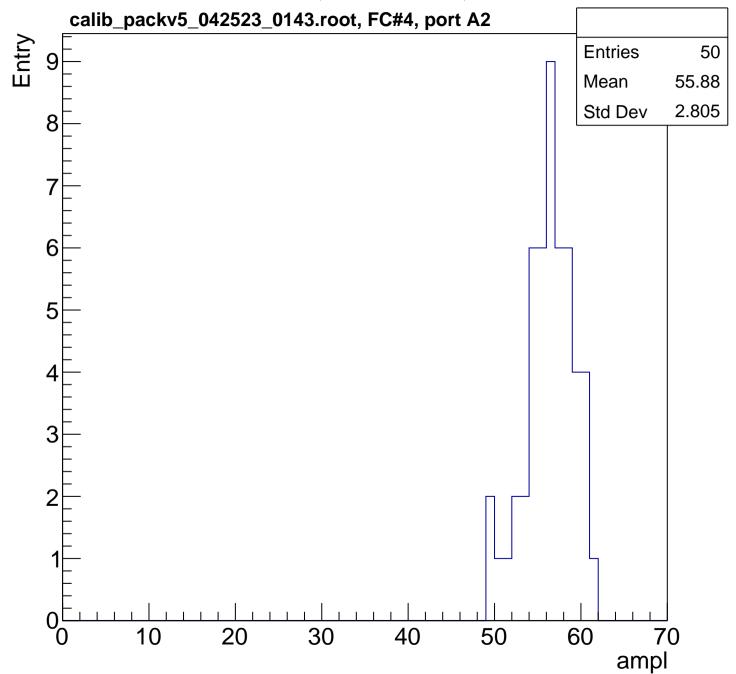


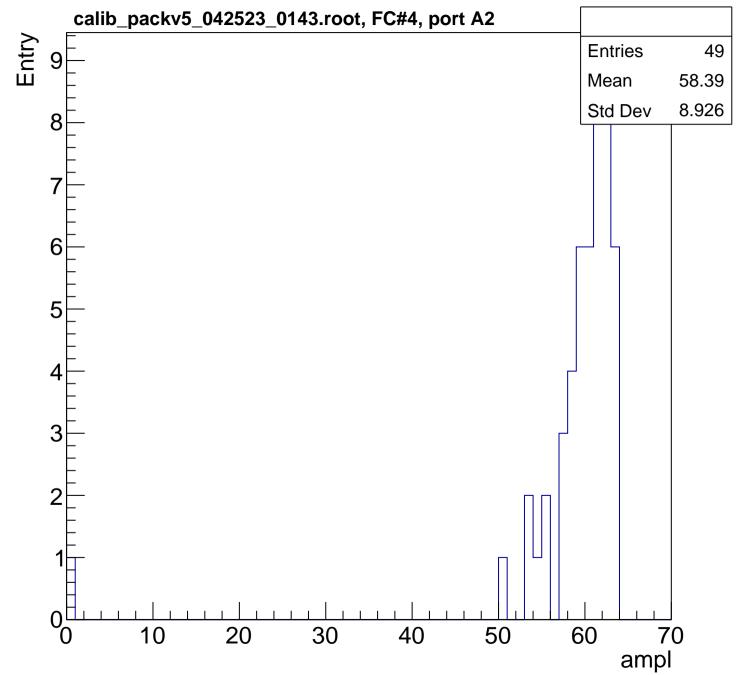


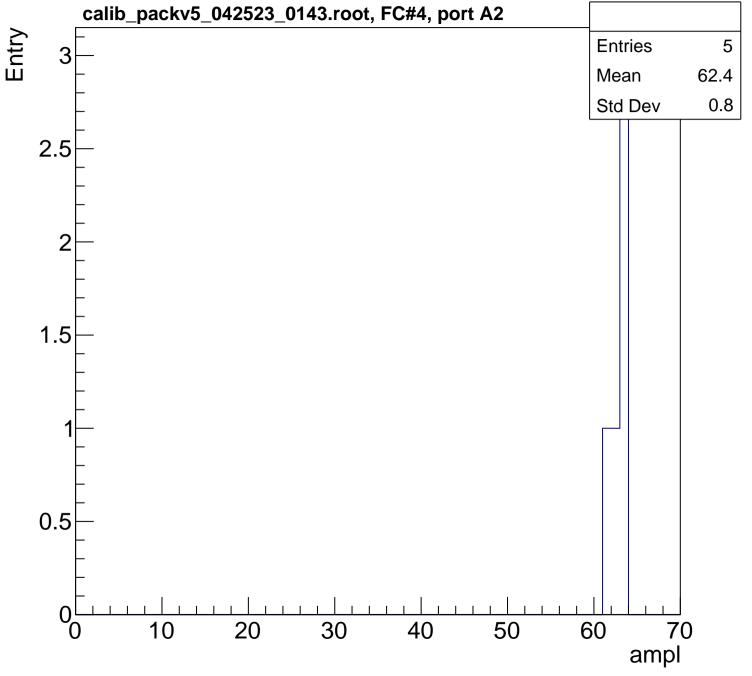


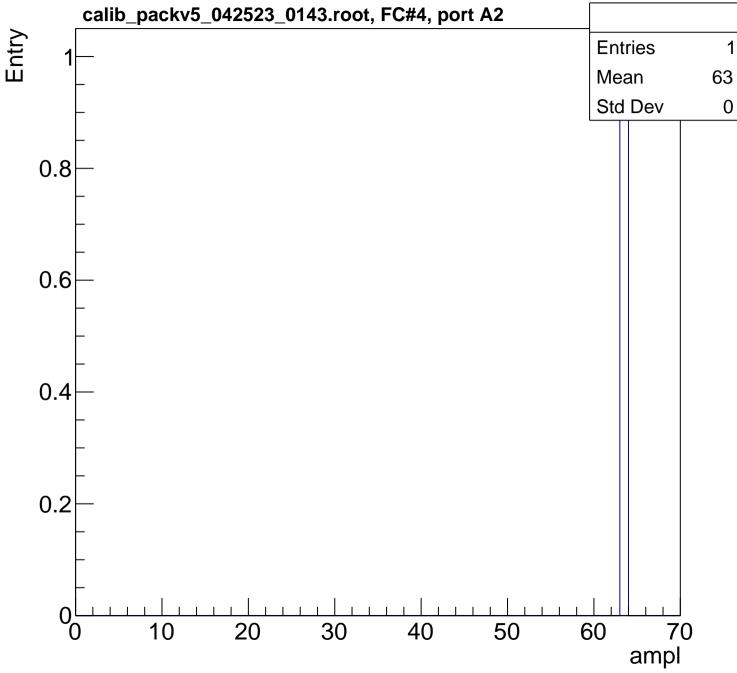


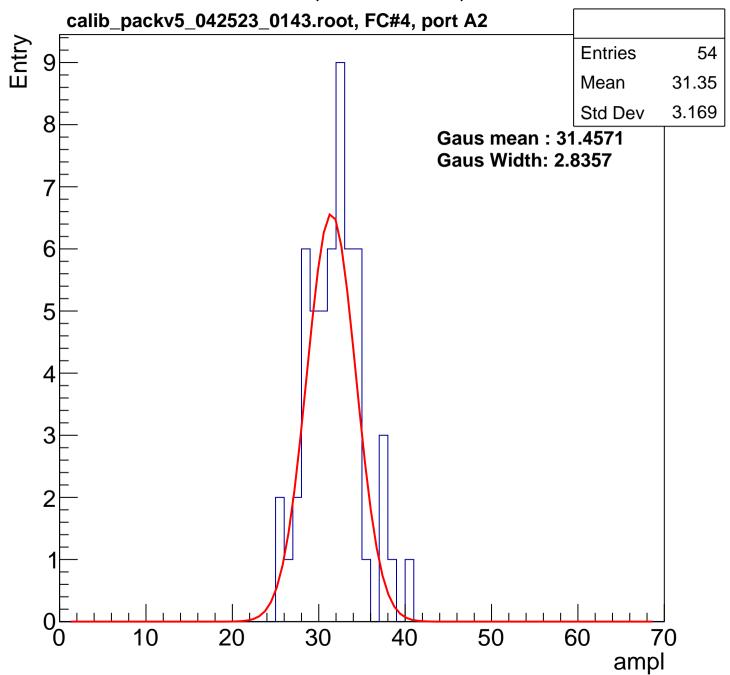


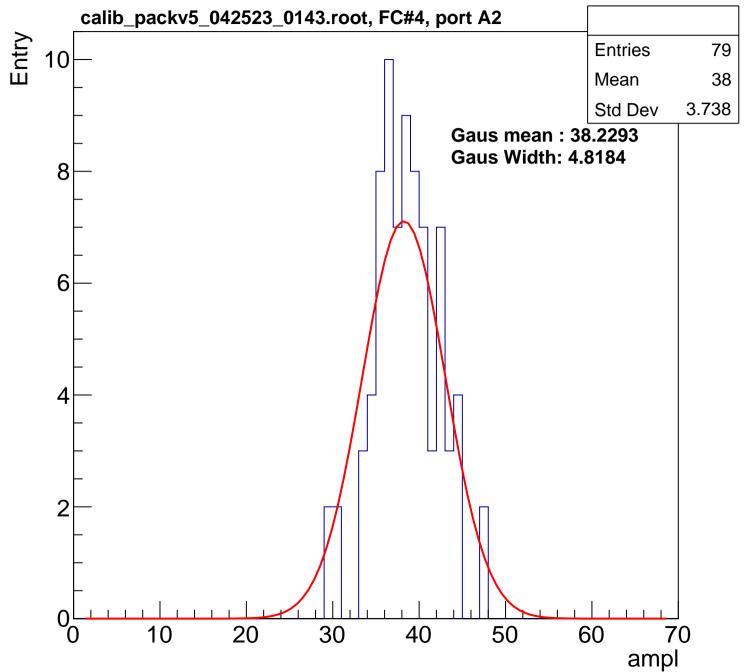


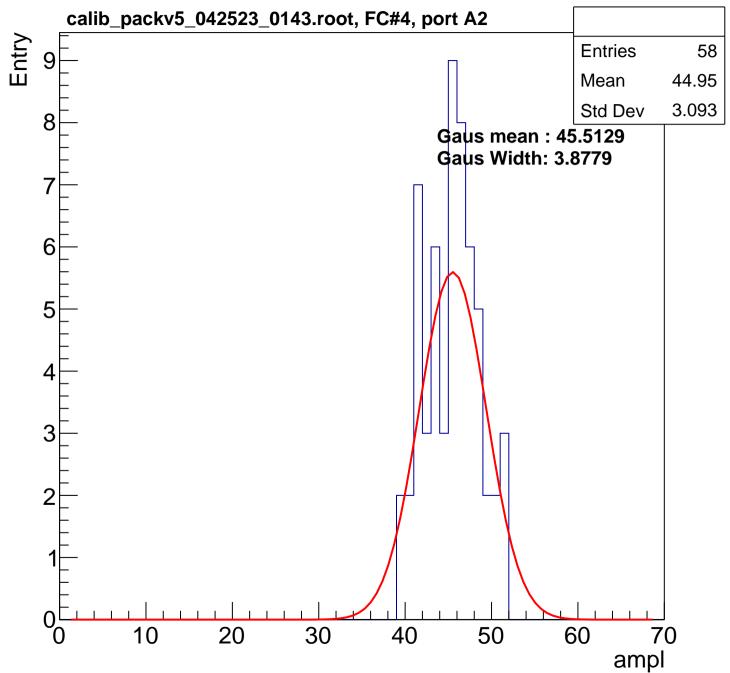


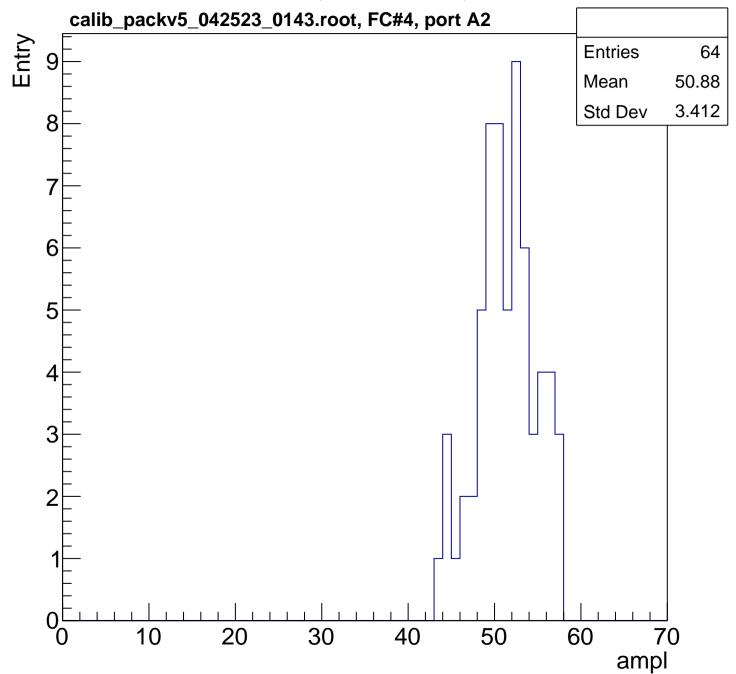


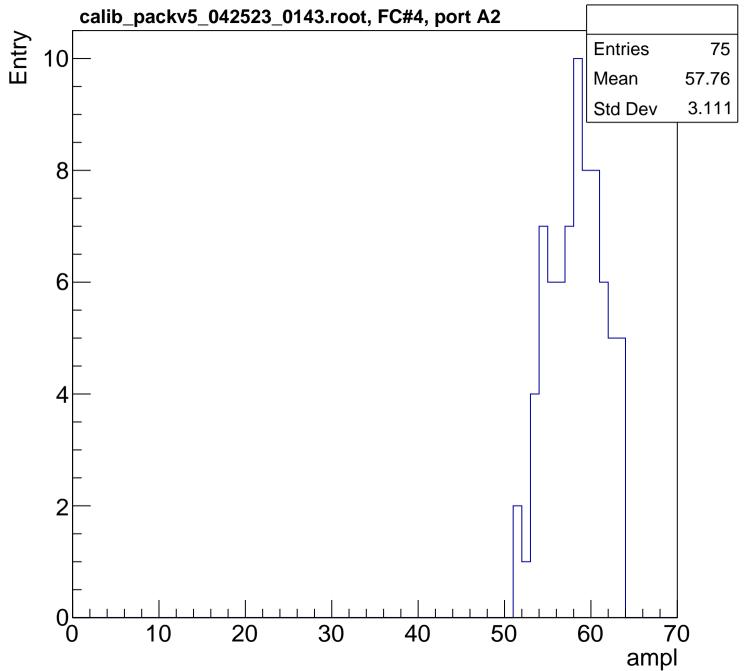


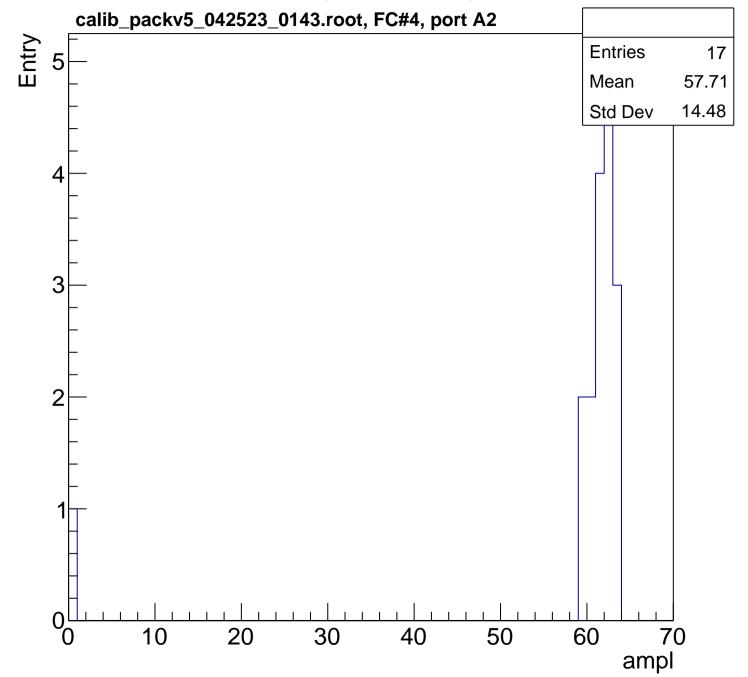


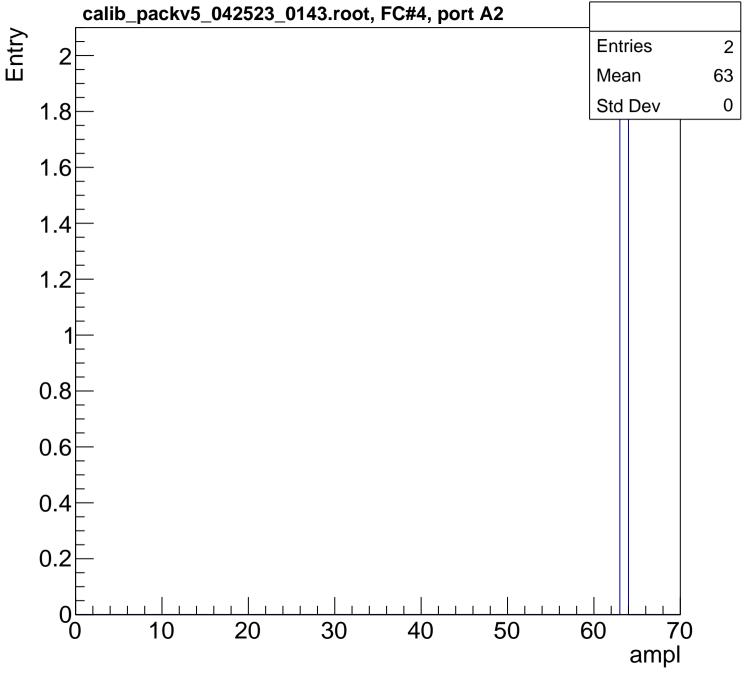


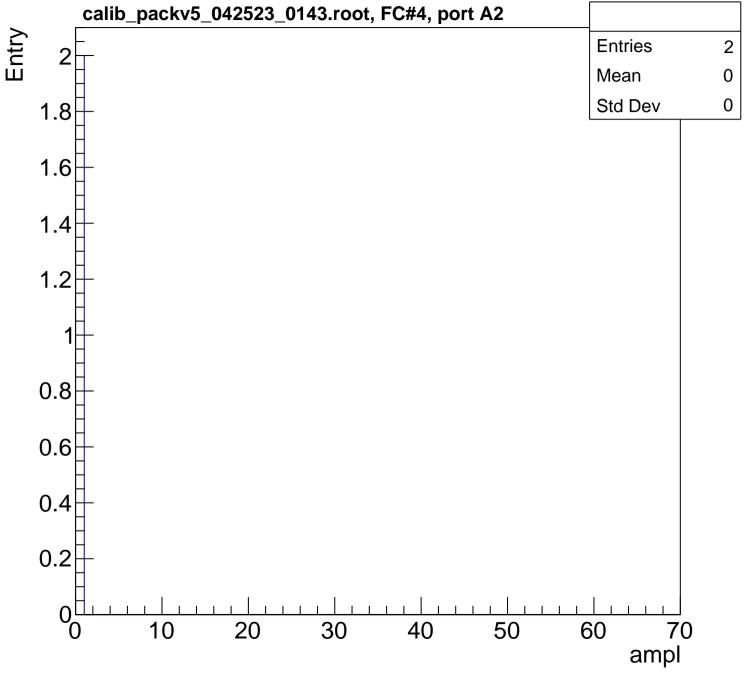


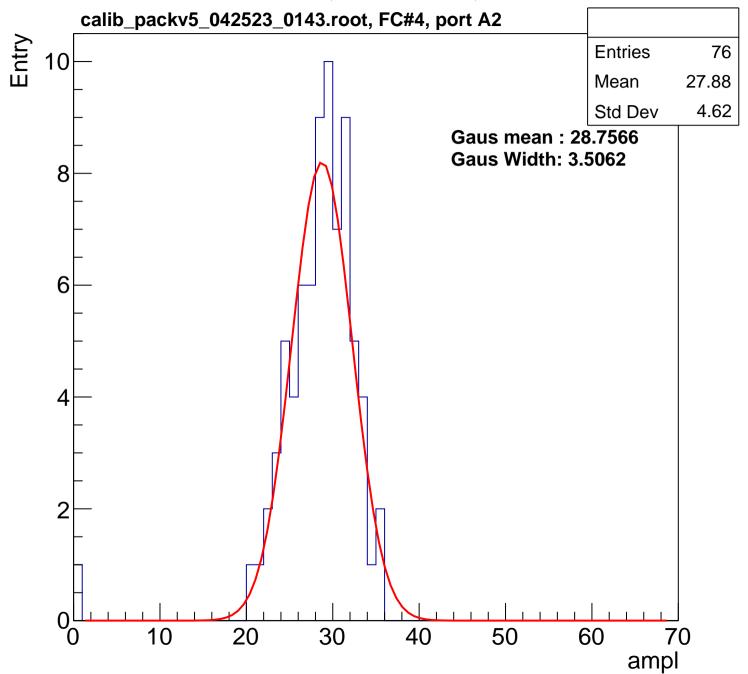


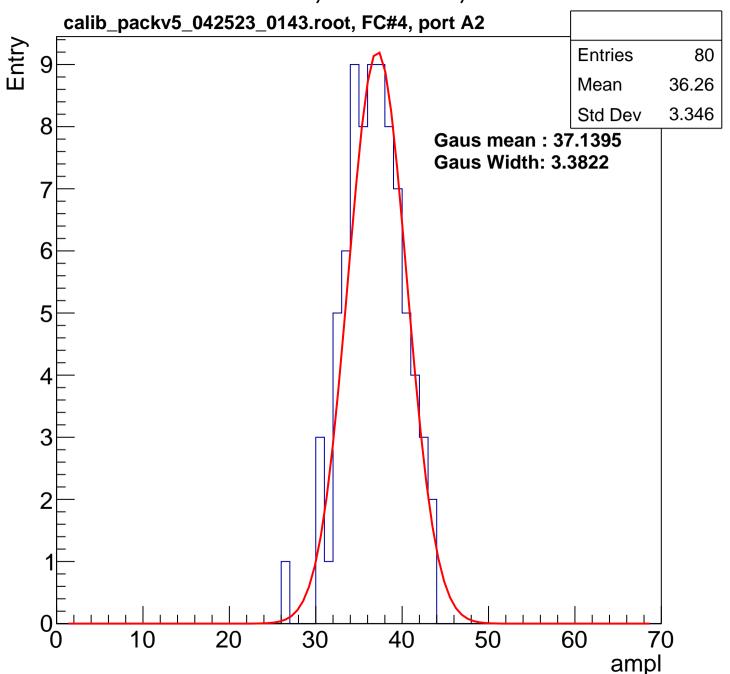


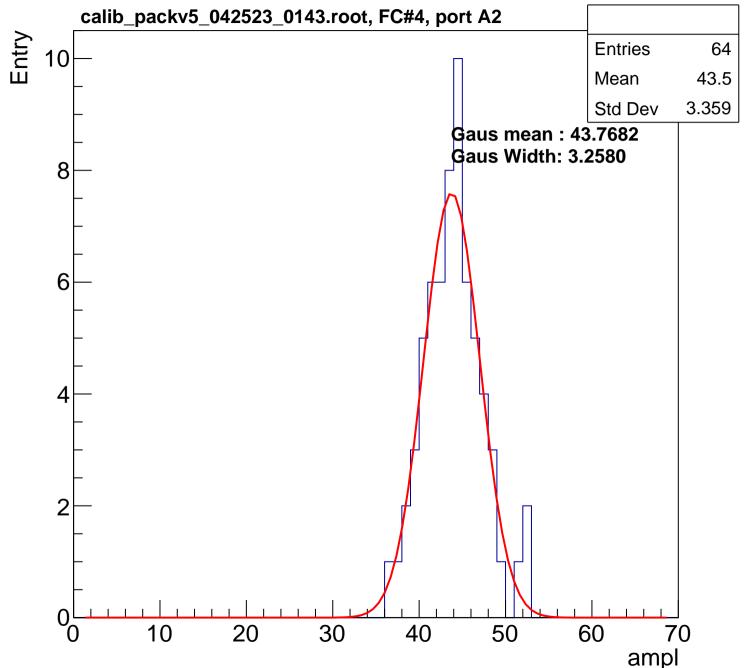


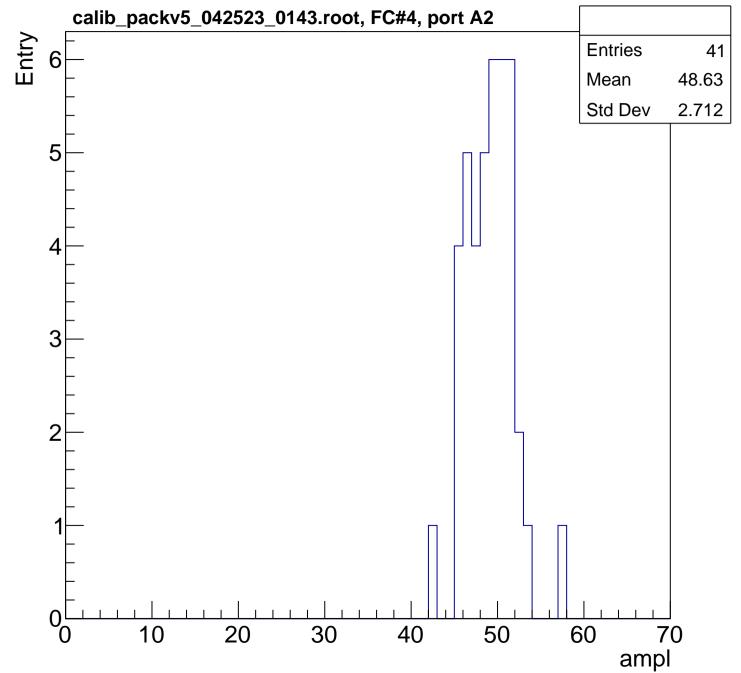


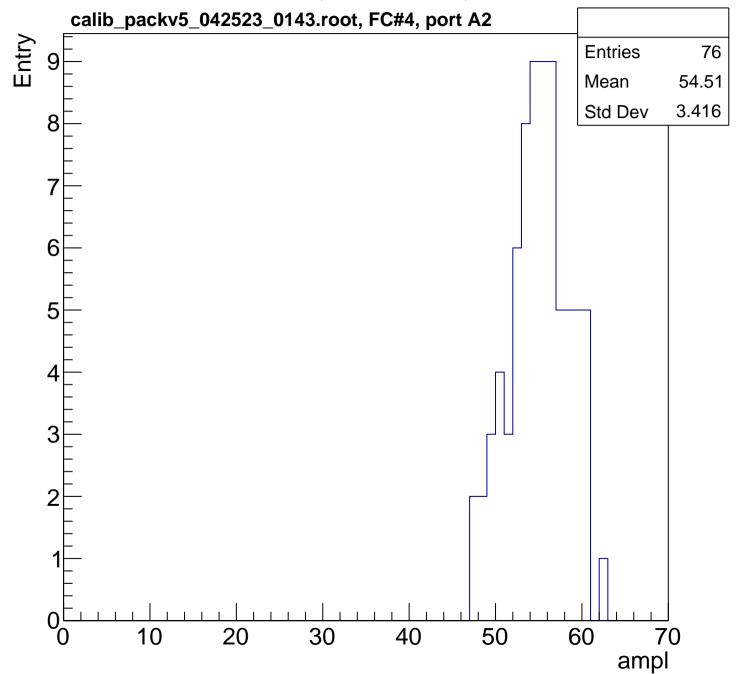


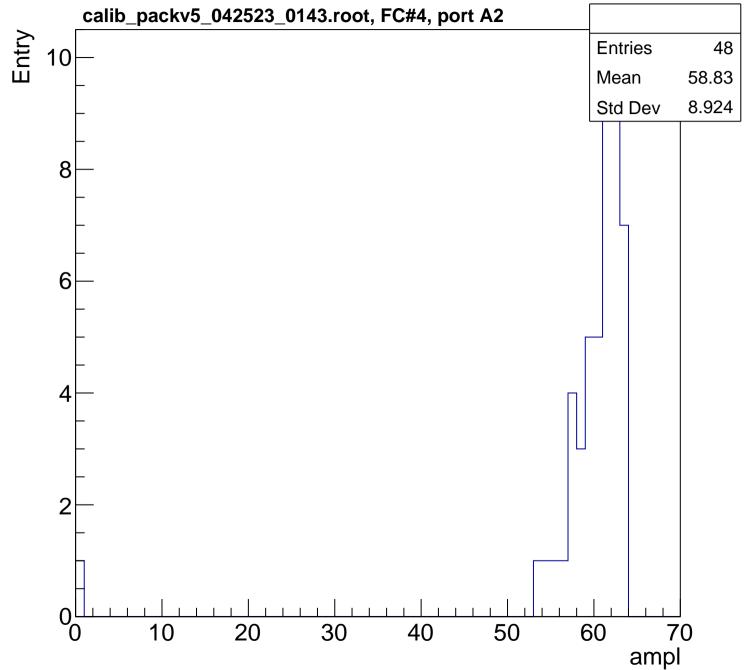


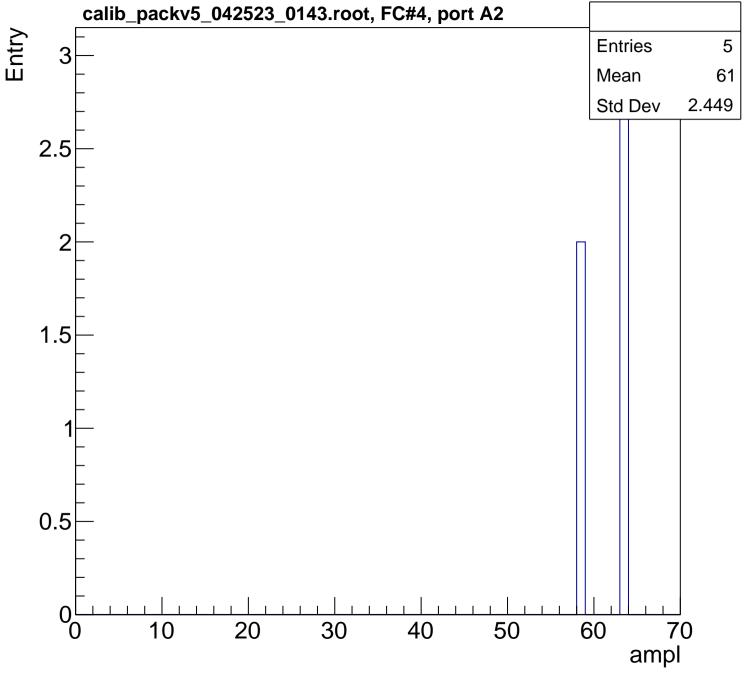




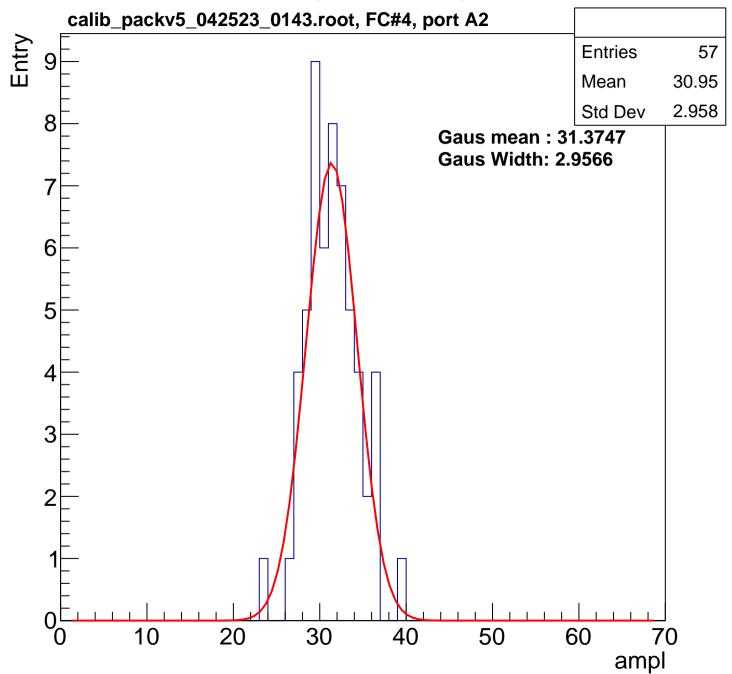


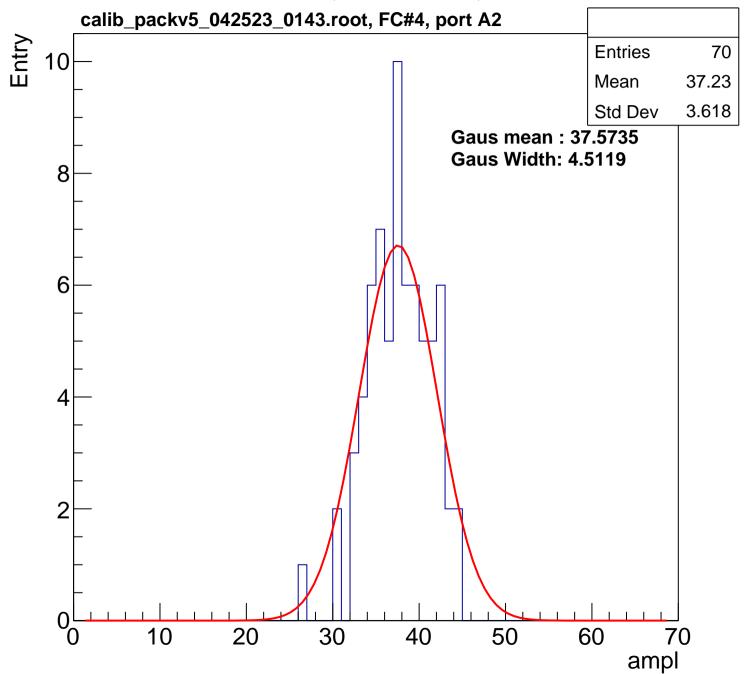


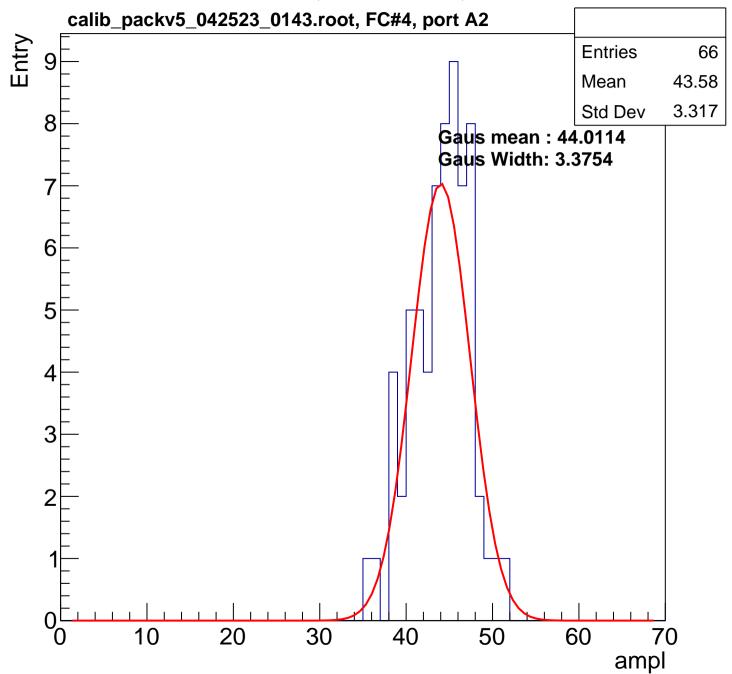


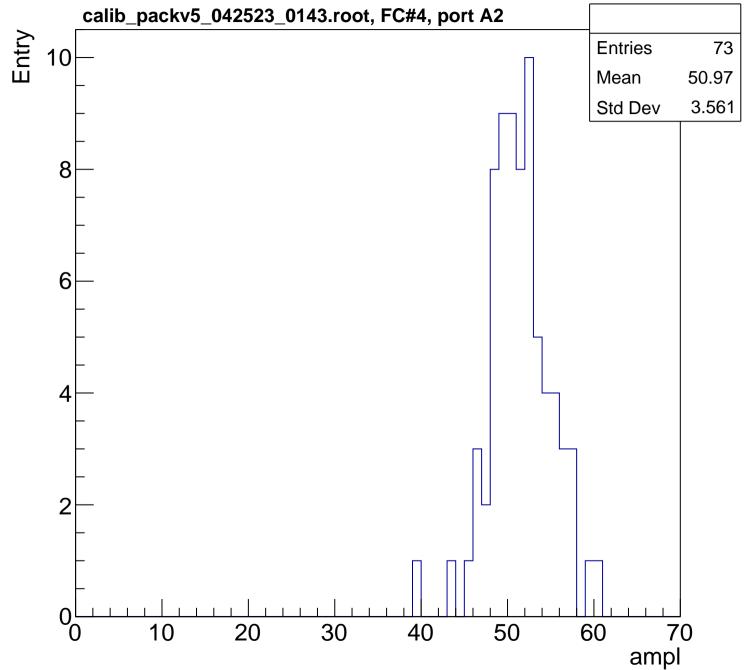


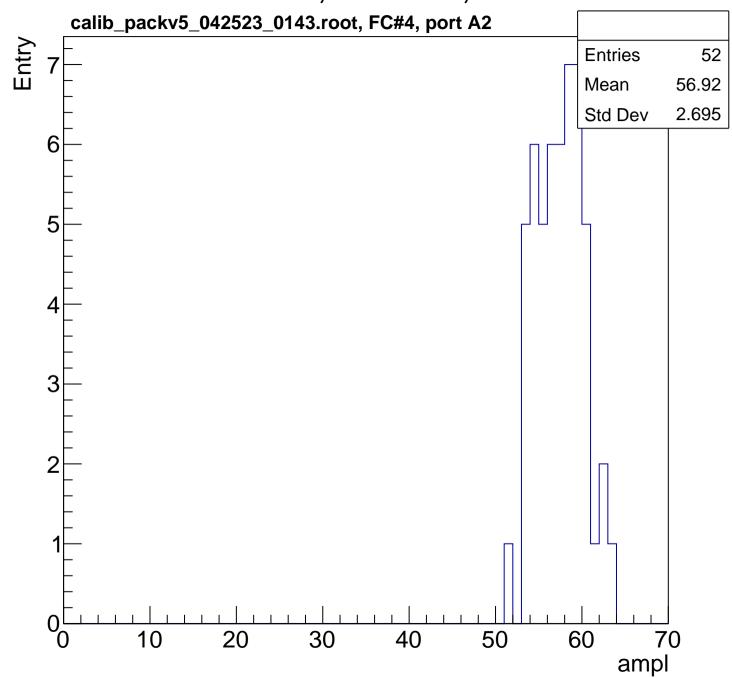


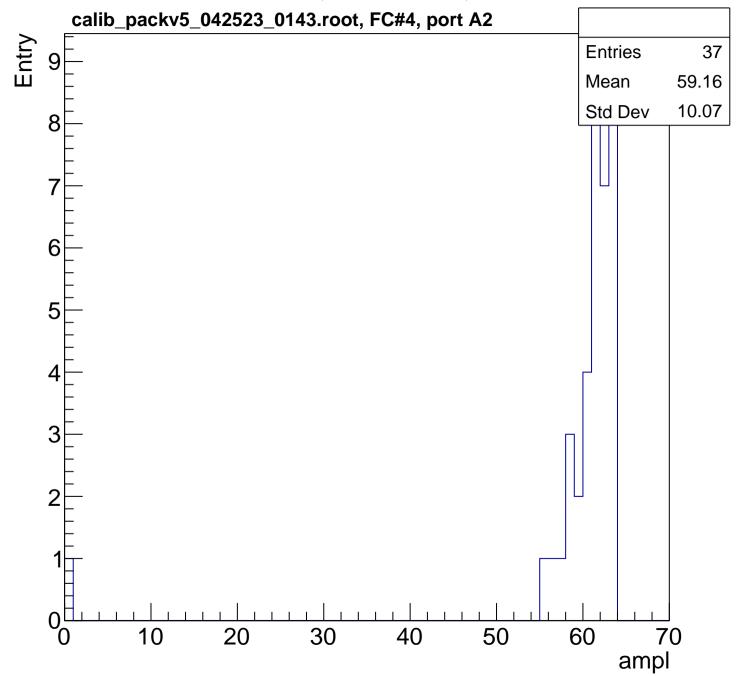


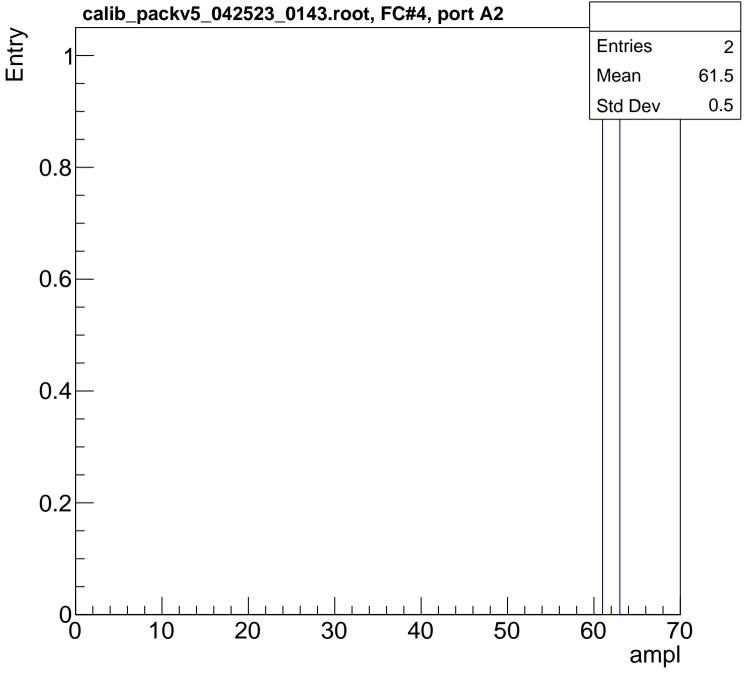




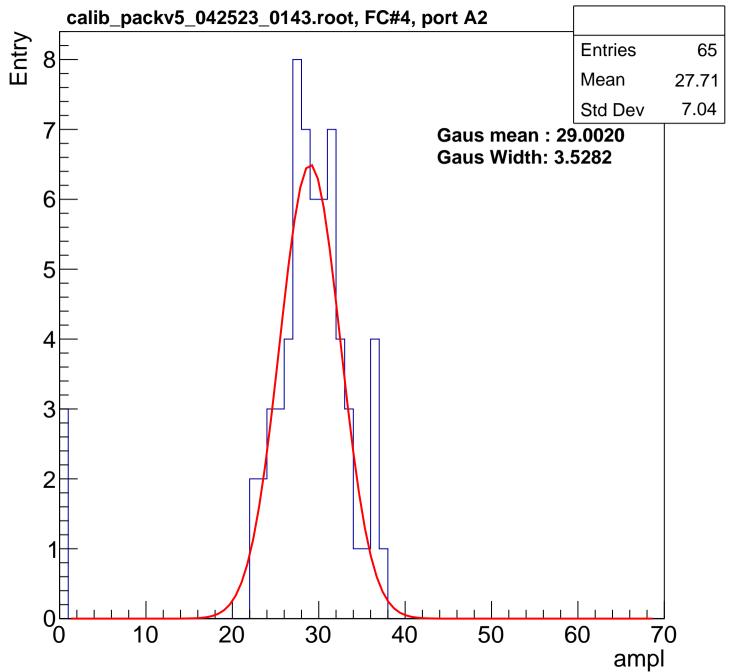


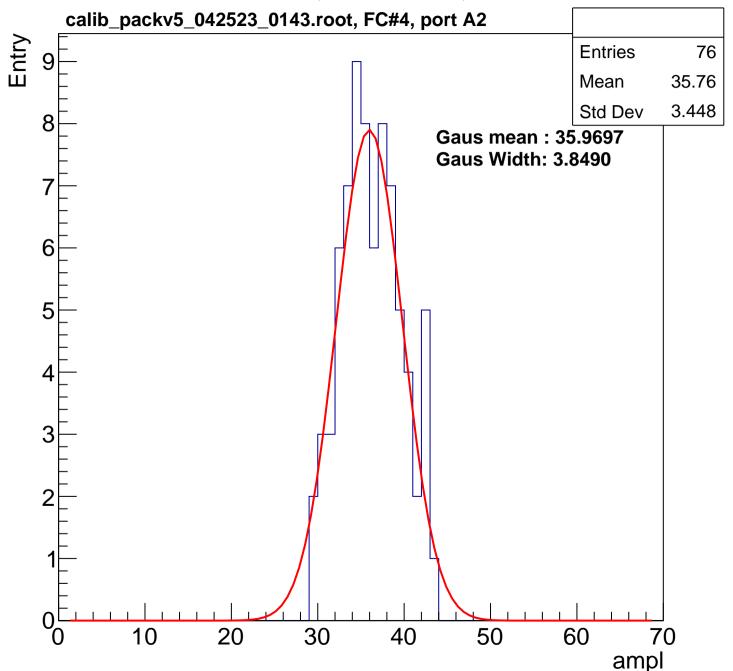


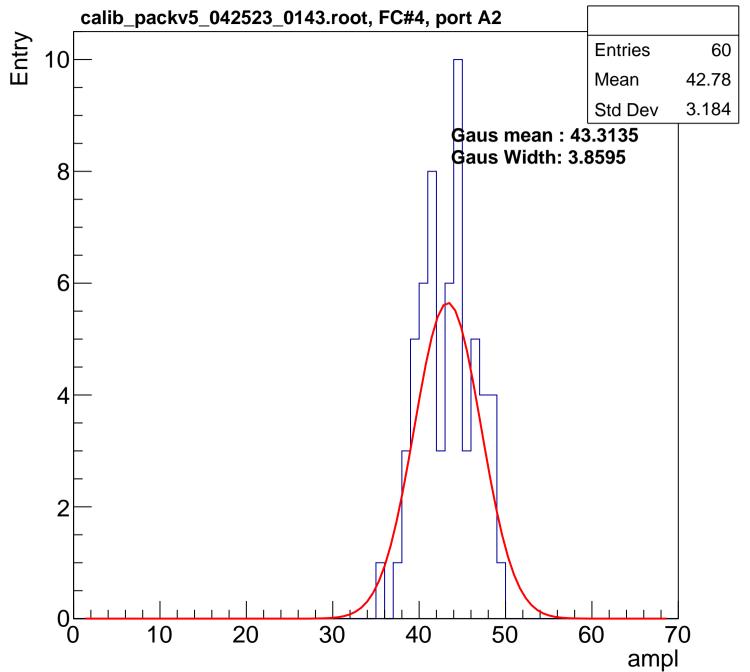


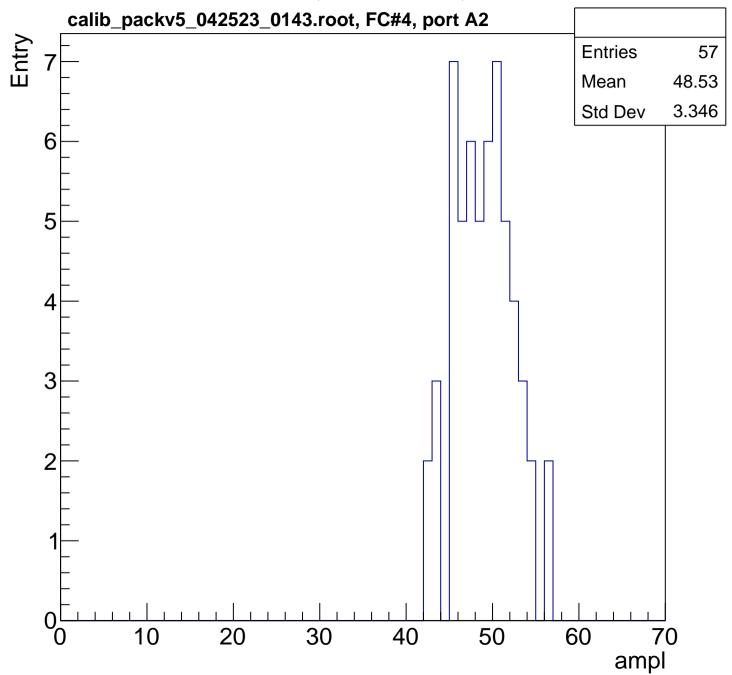


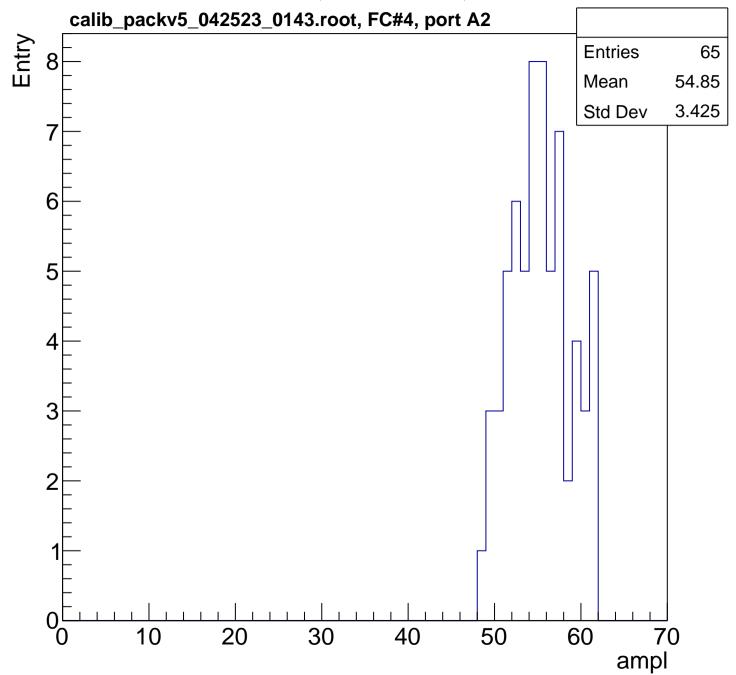


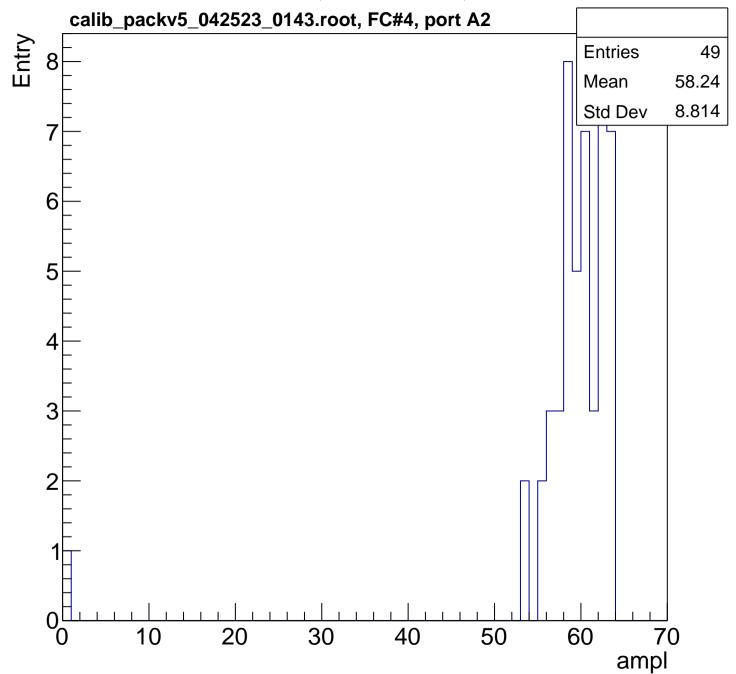


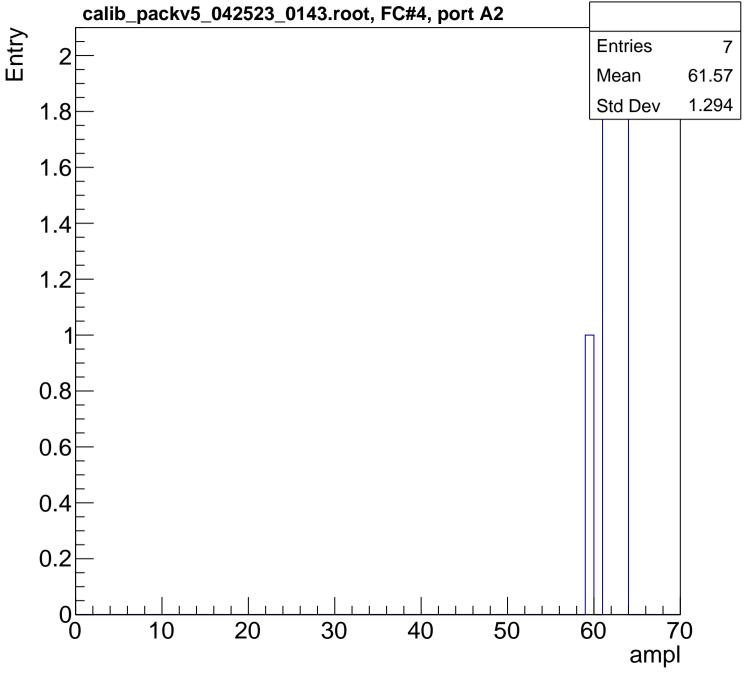


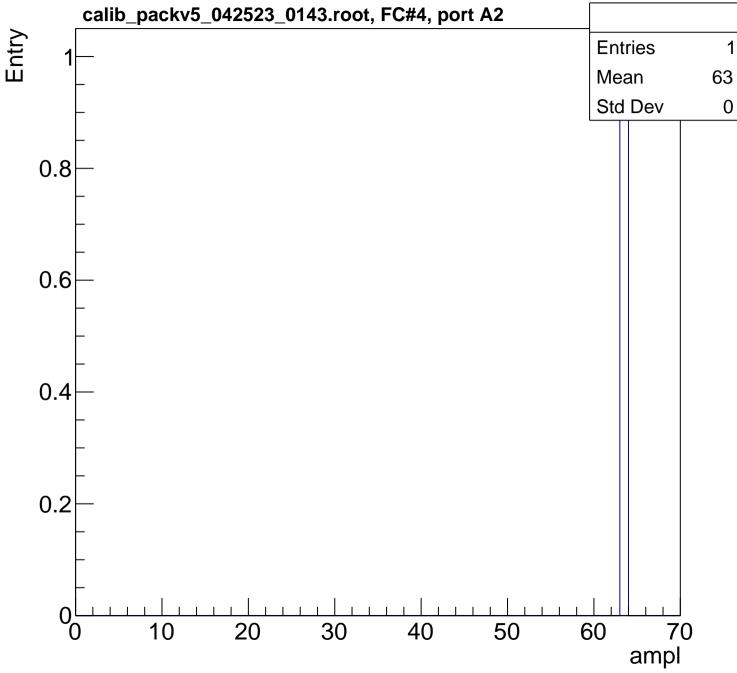


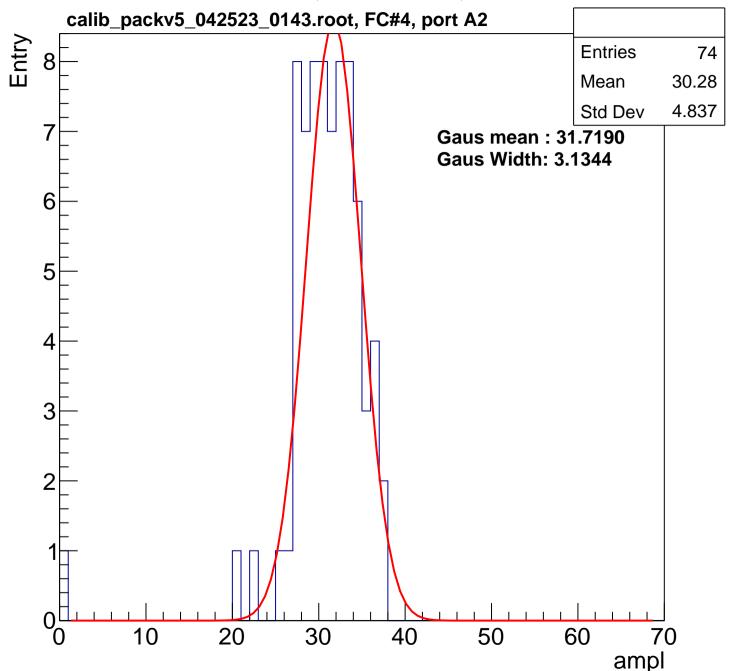


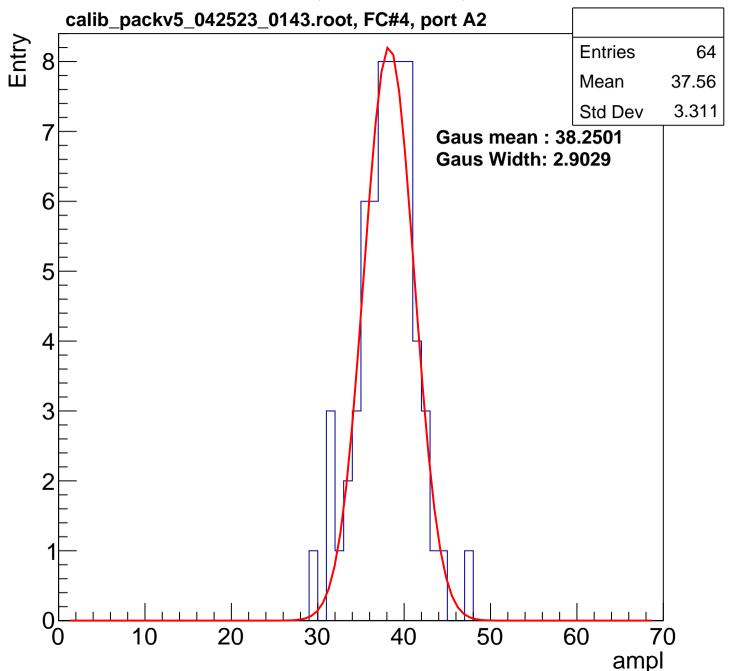


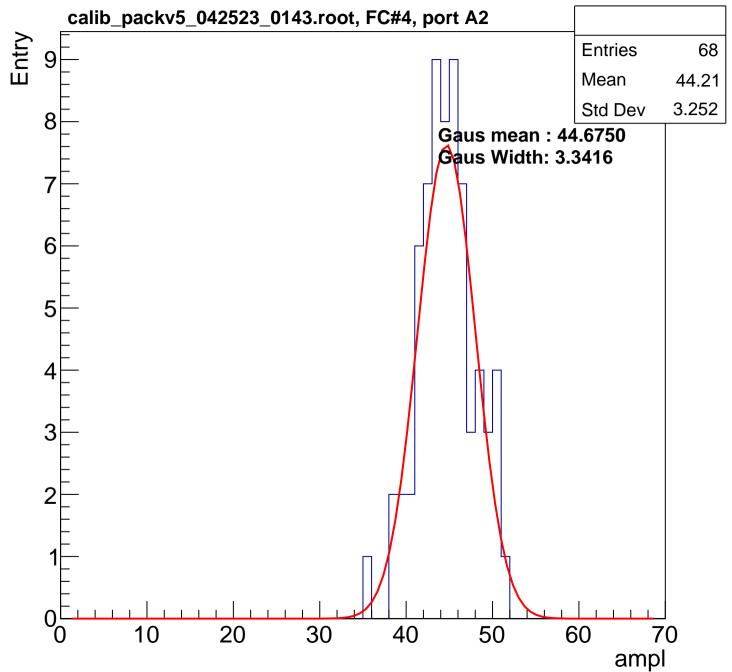


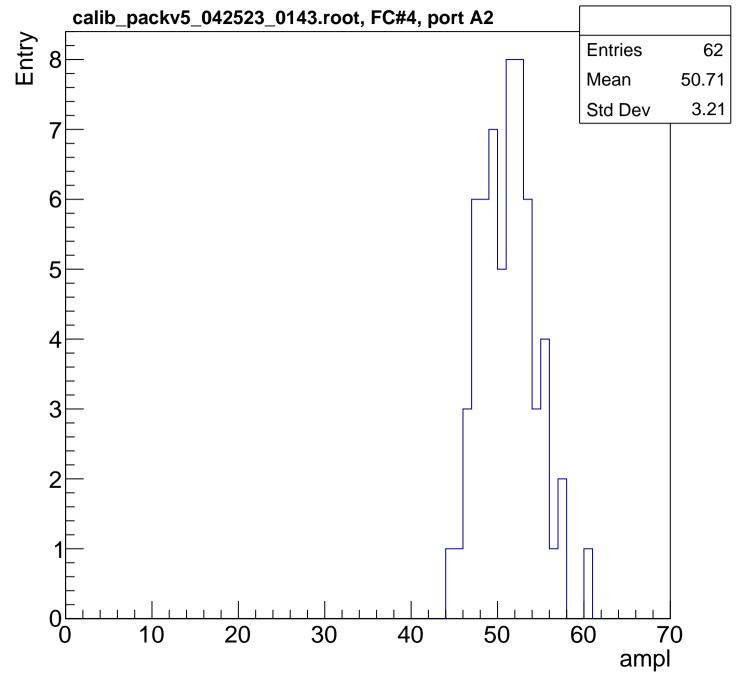


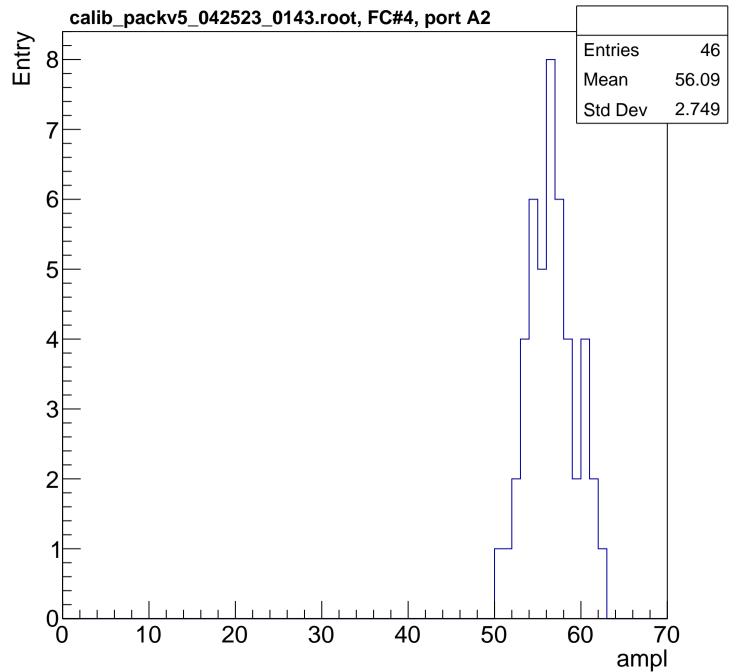


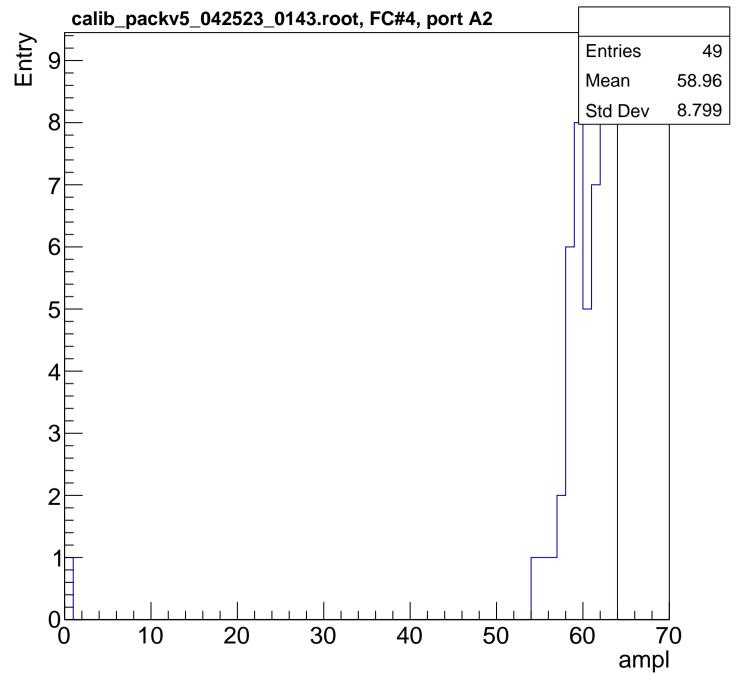


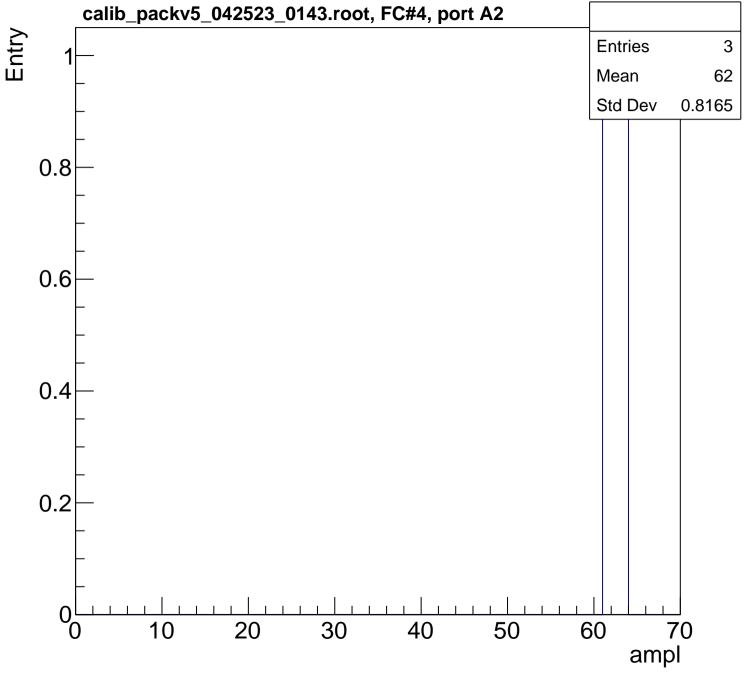




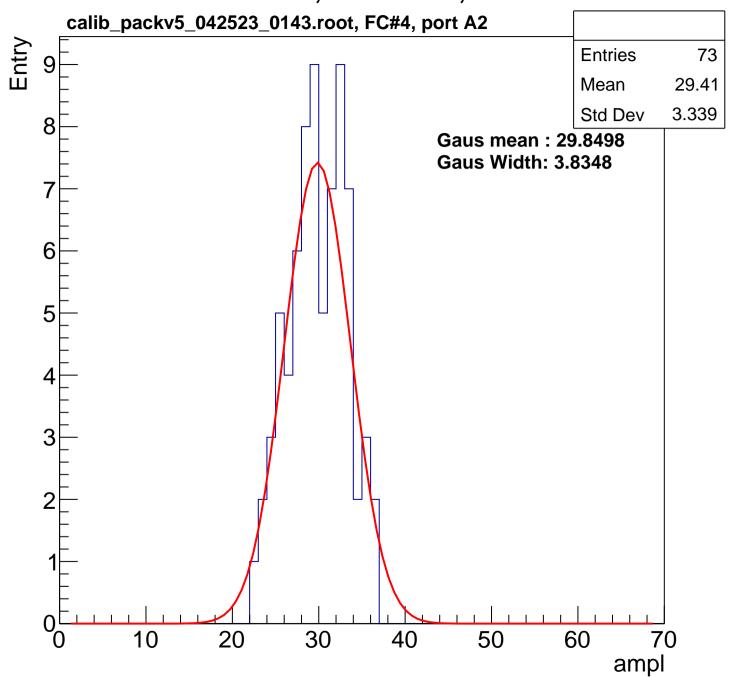


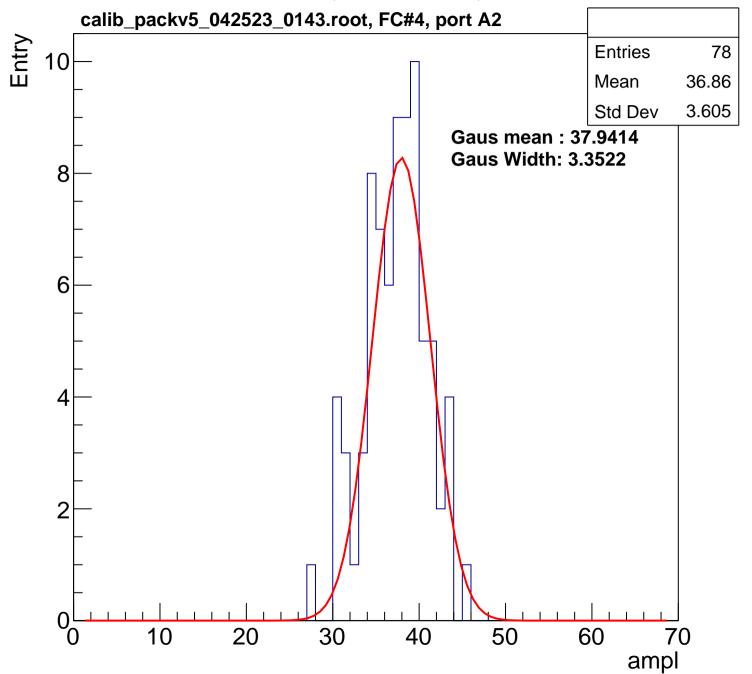


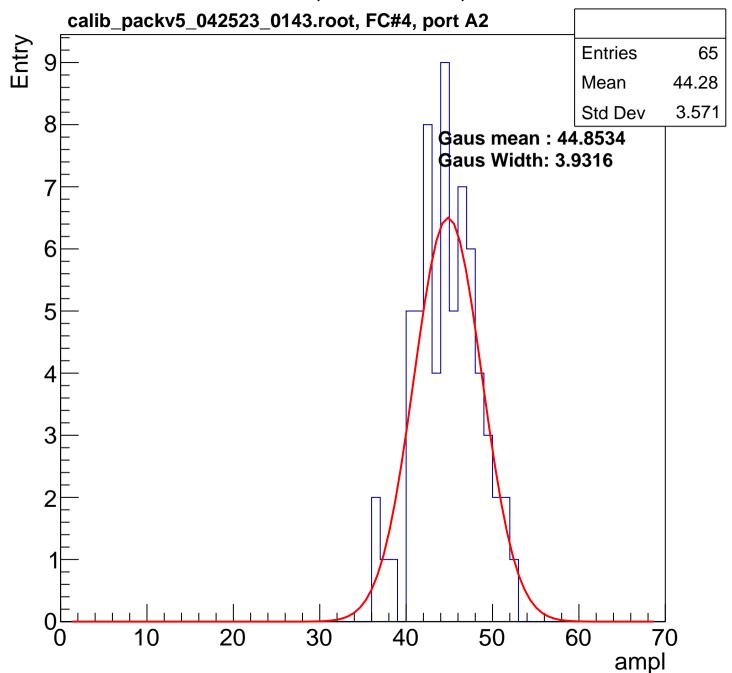


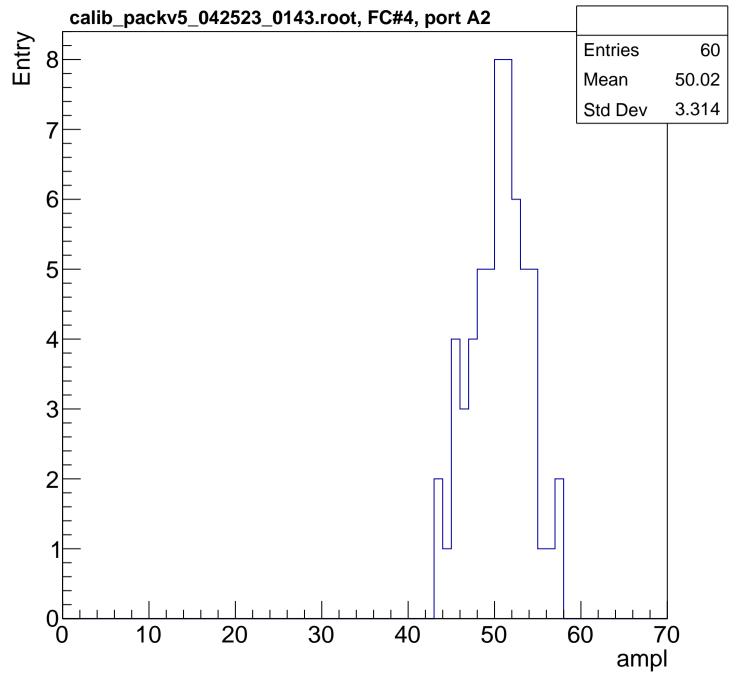


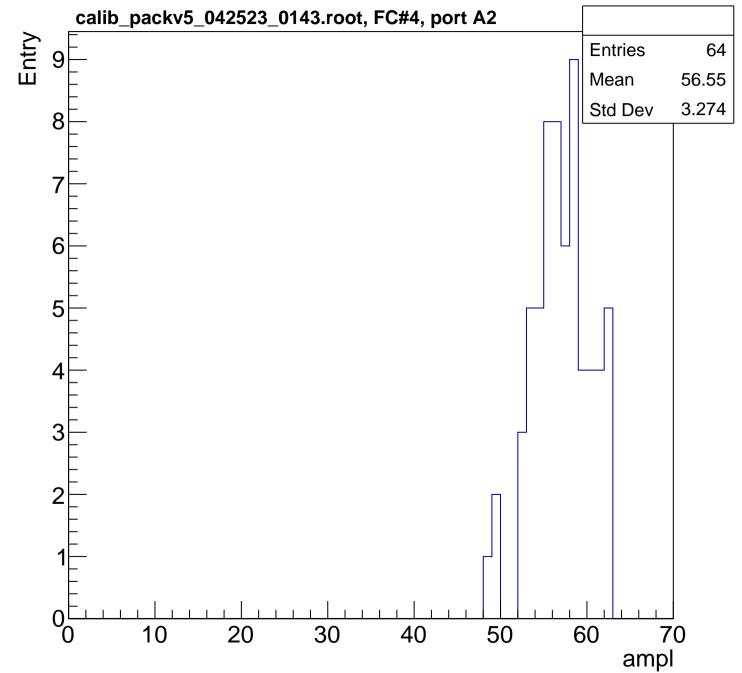
B1L100S, U8-ch73, adc7 calib_packv5_042523_0143.root, FC#4, port A2 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

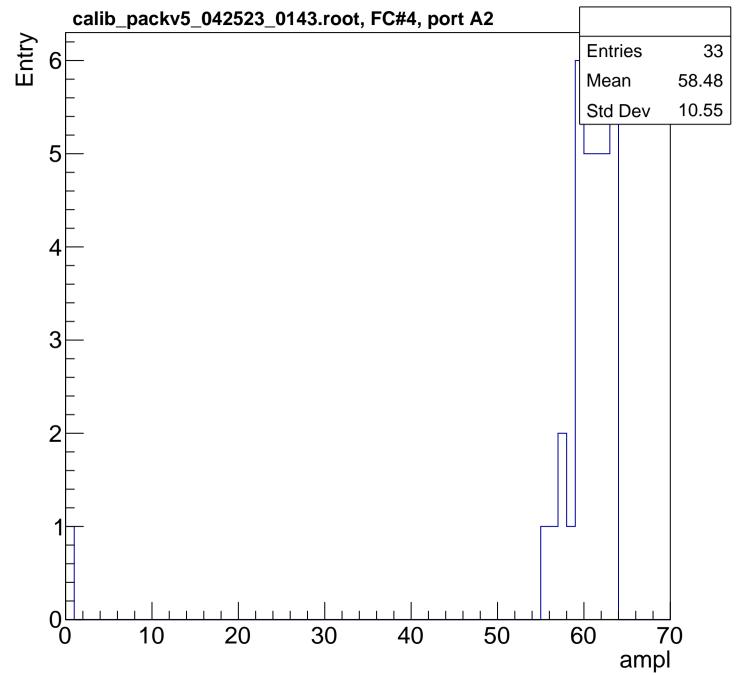


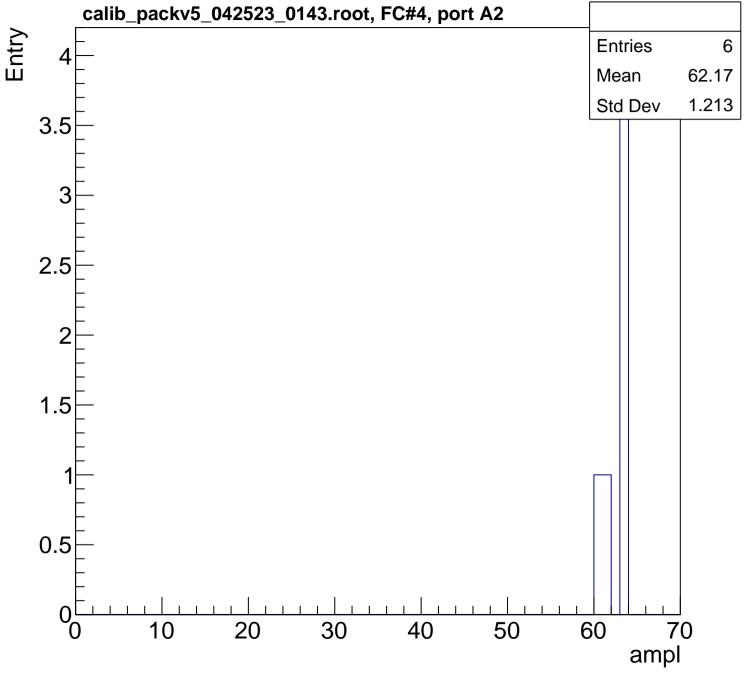


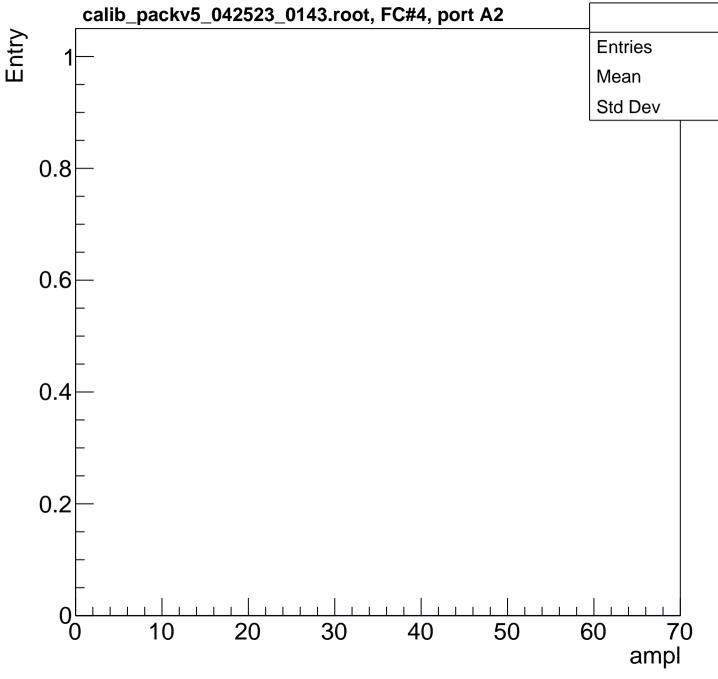


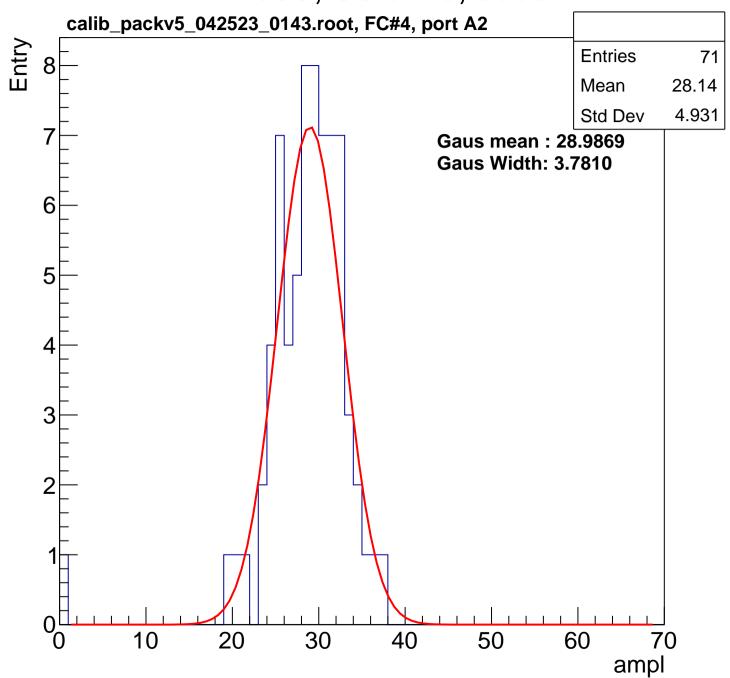


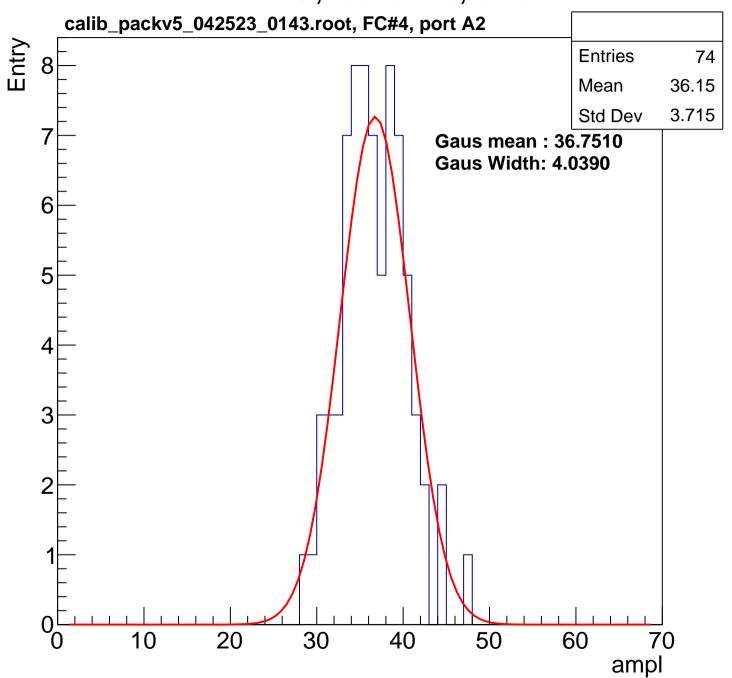


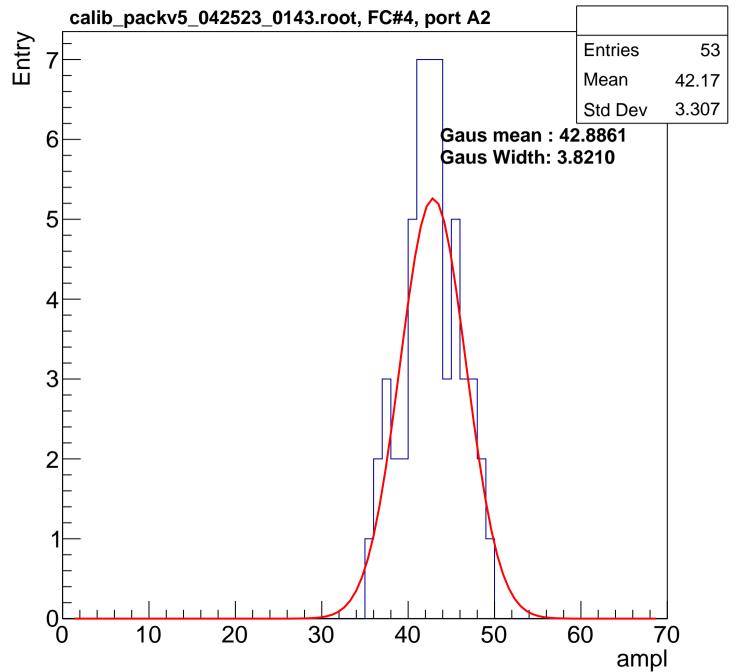


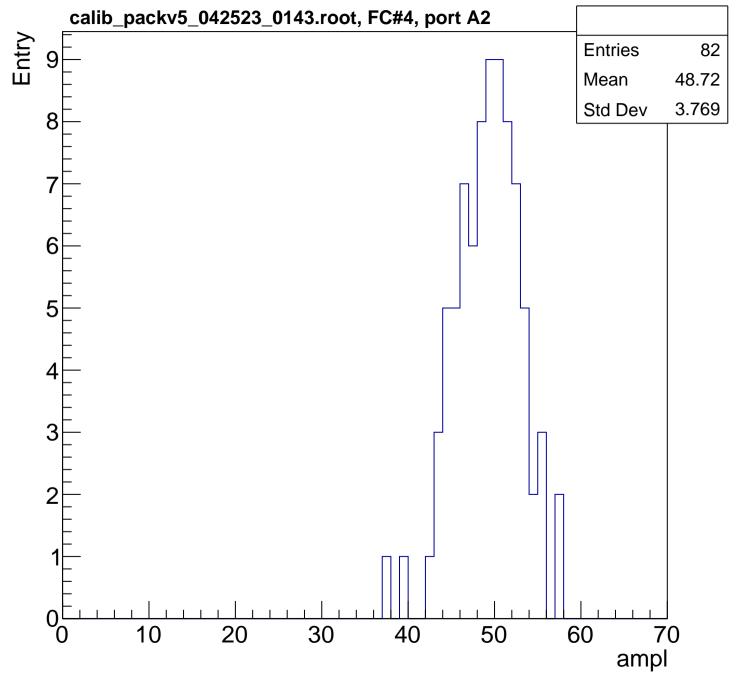


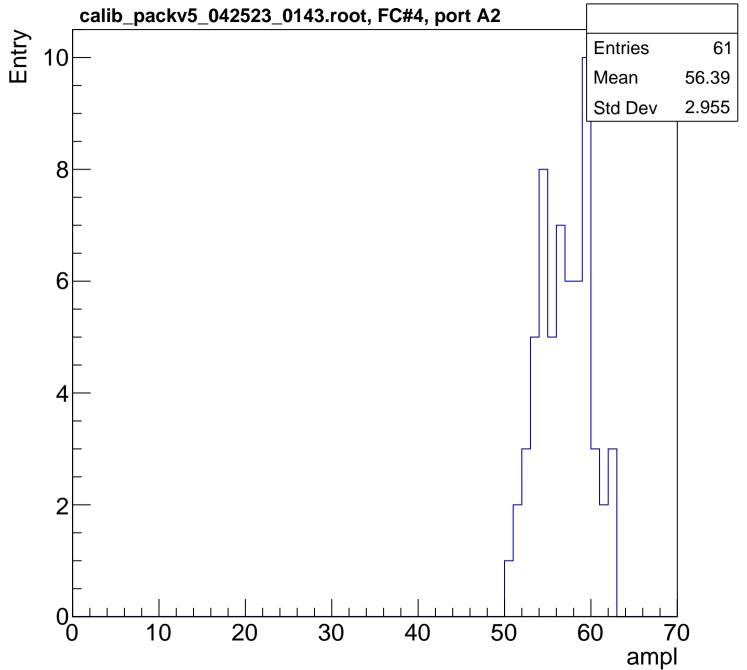


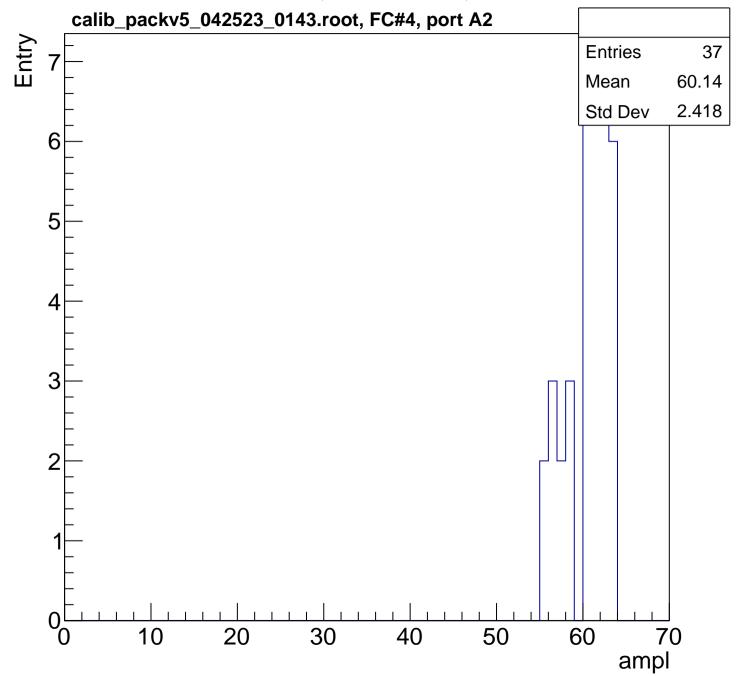


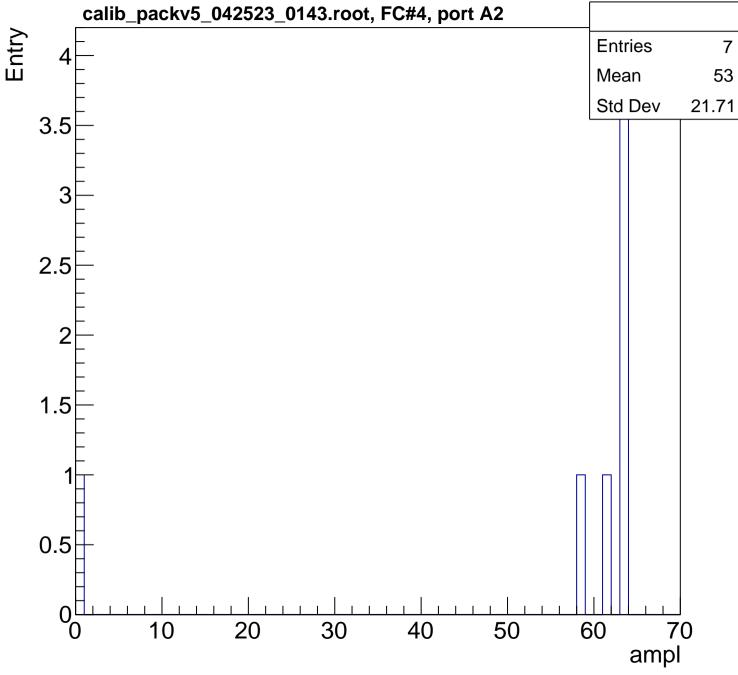




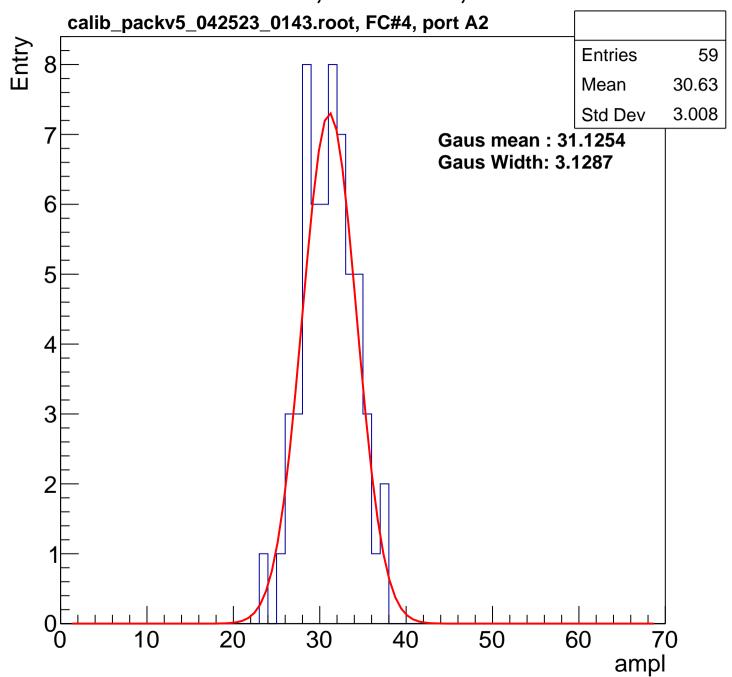


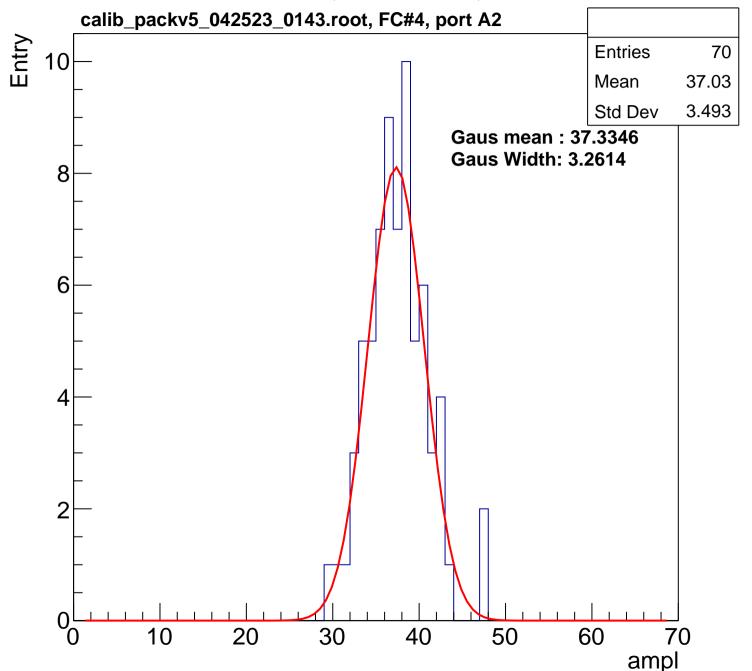


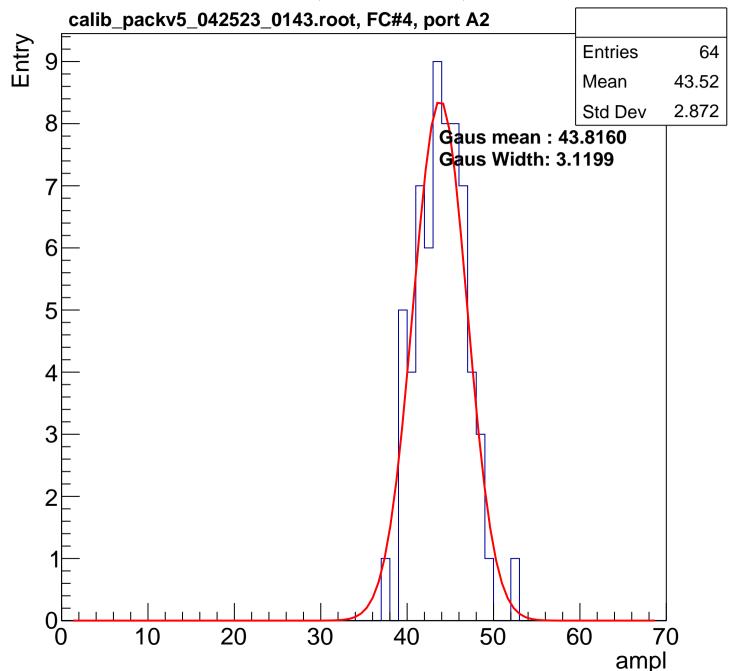


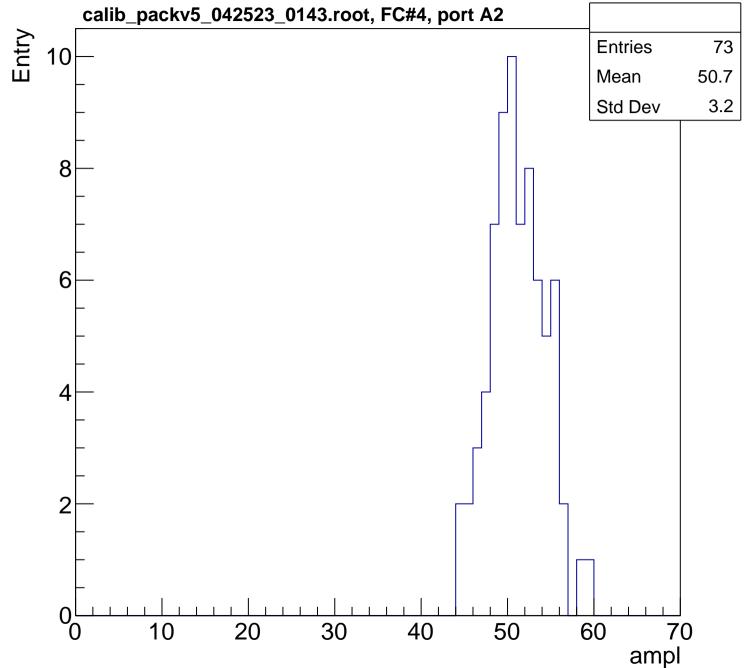


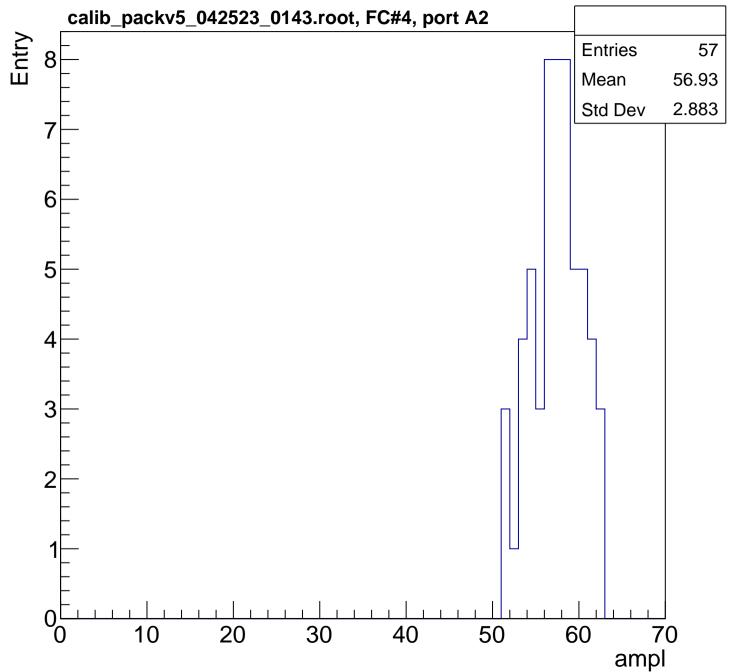


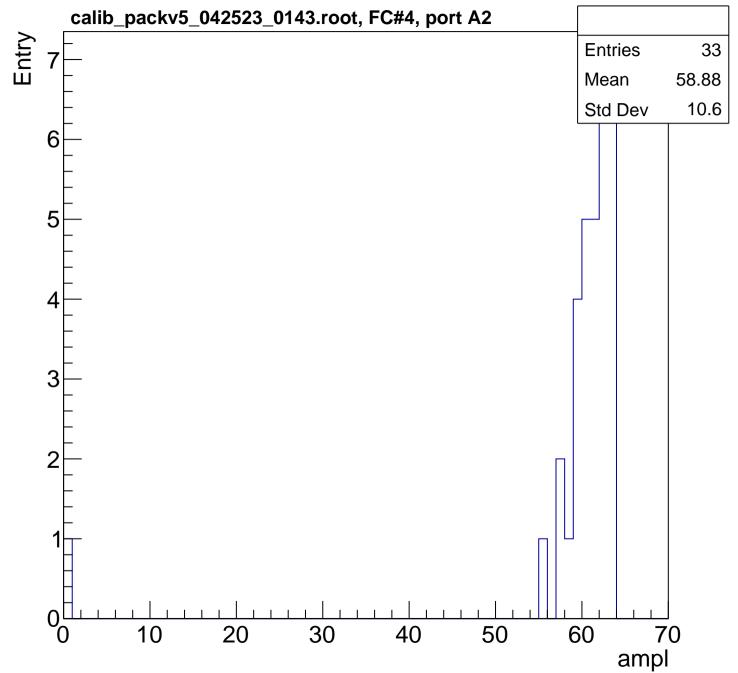


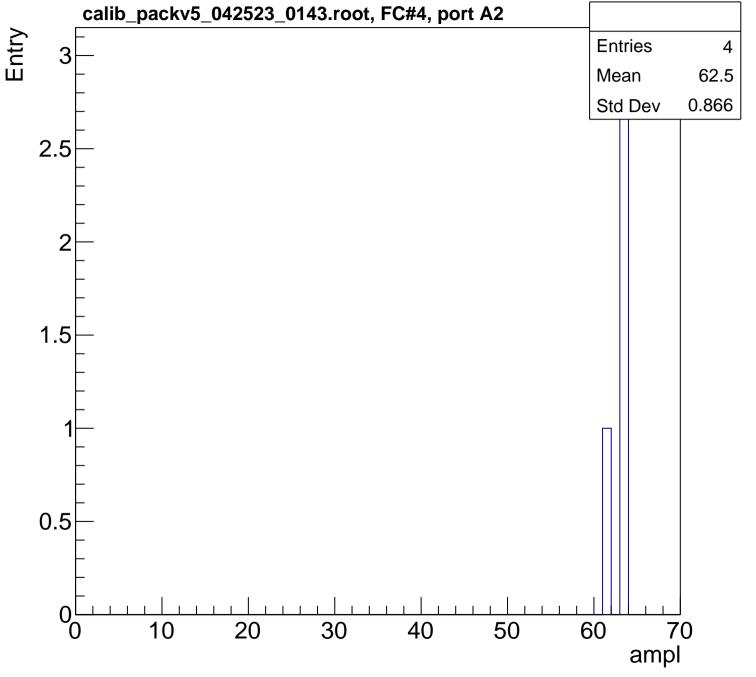


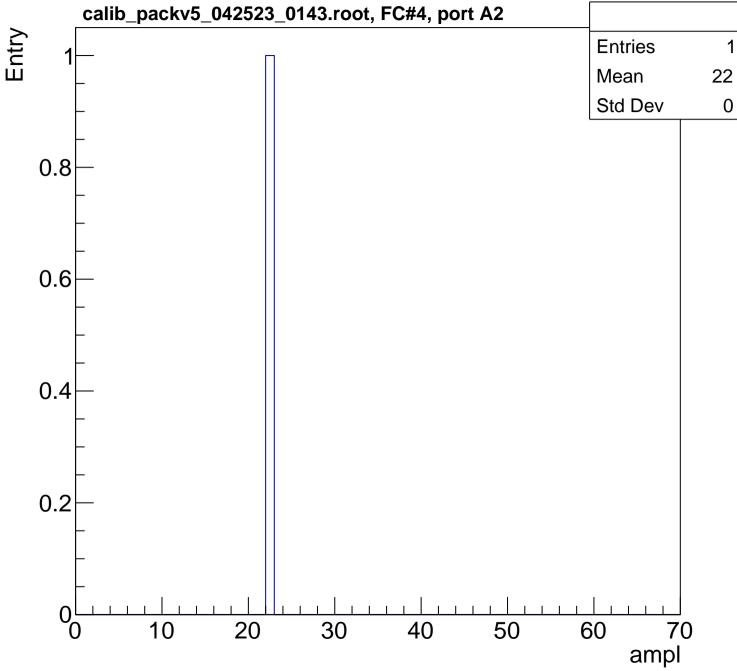


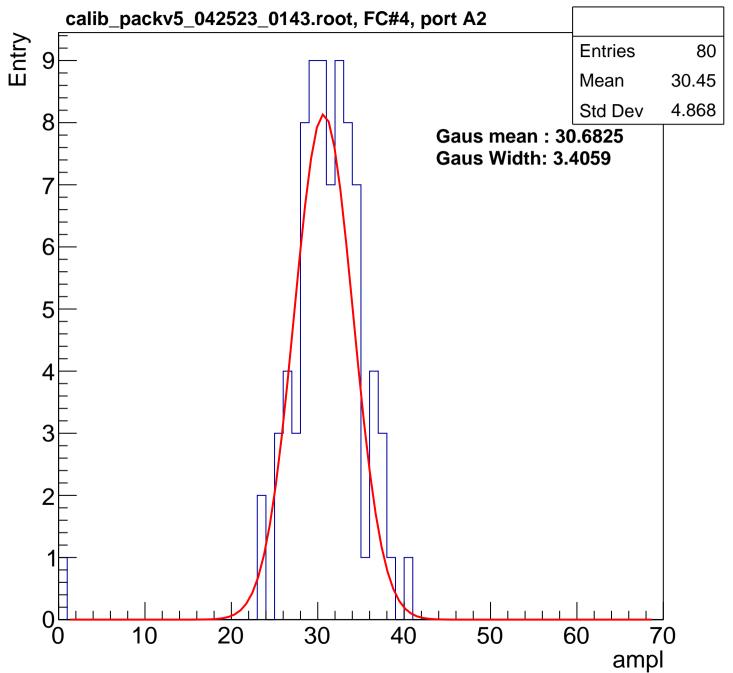


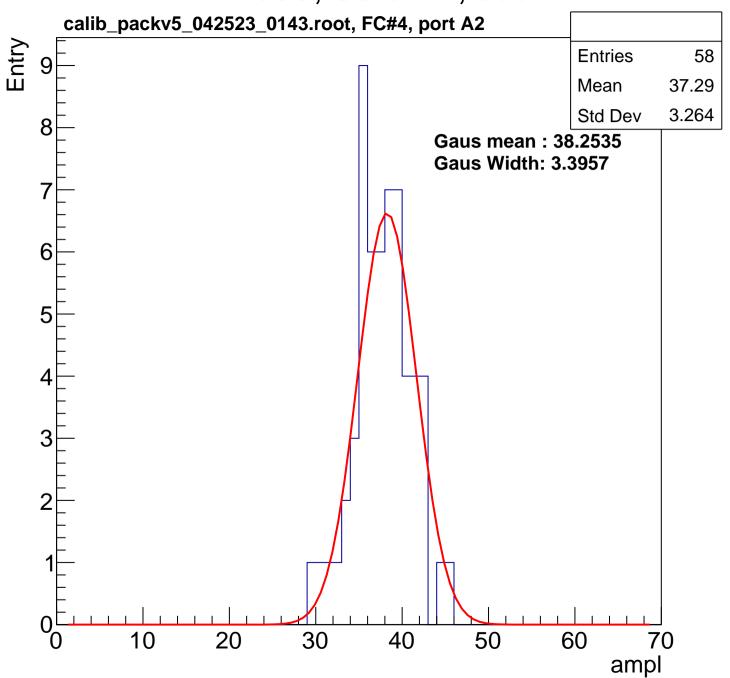


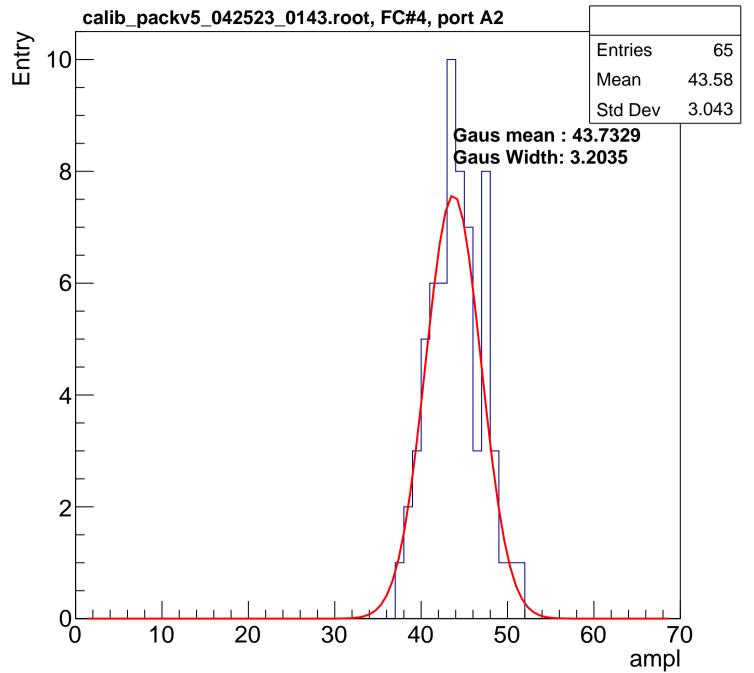


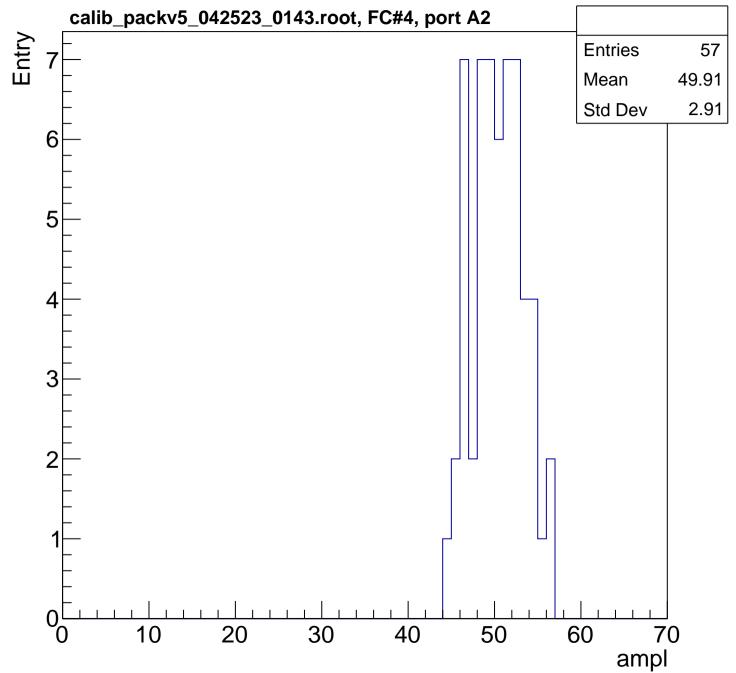


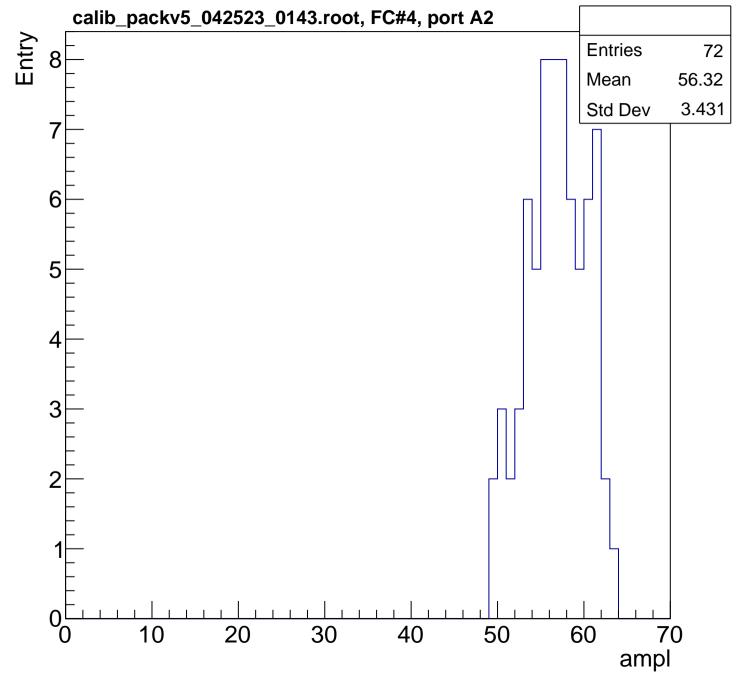


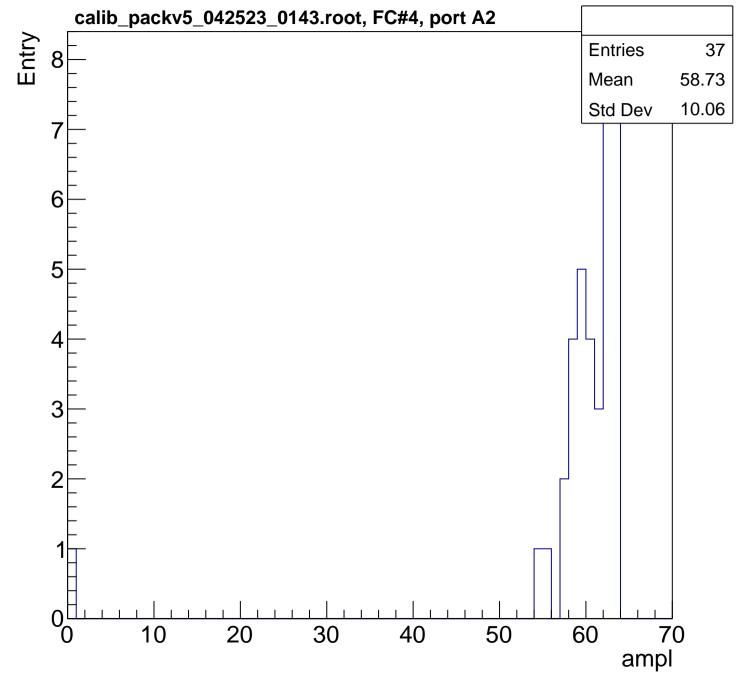


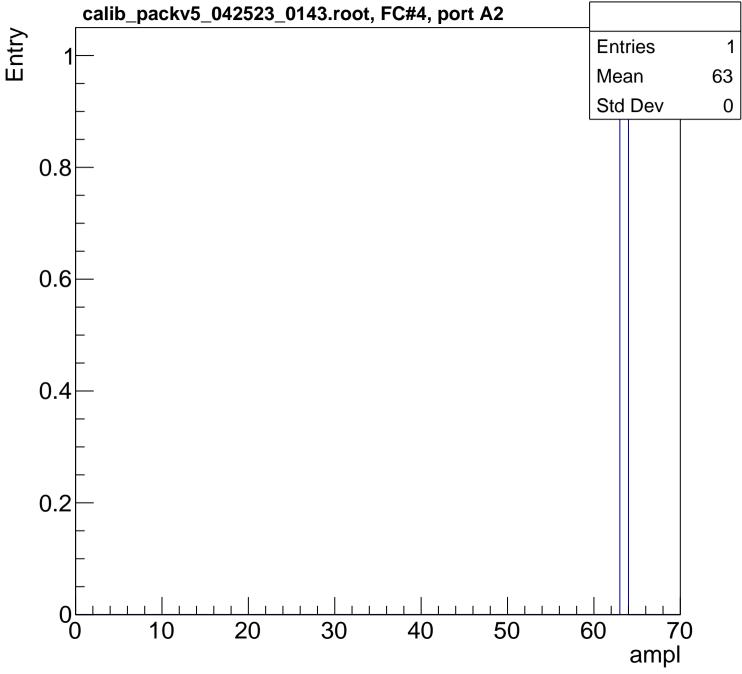


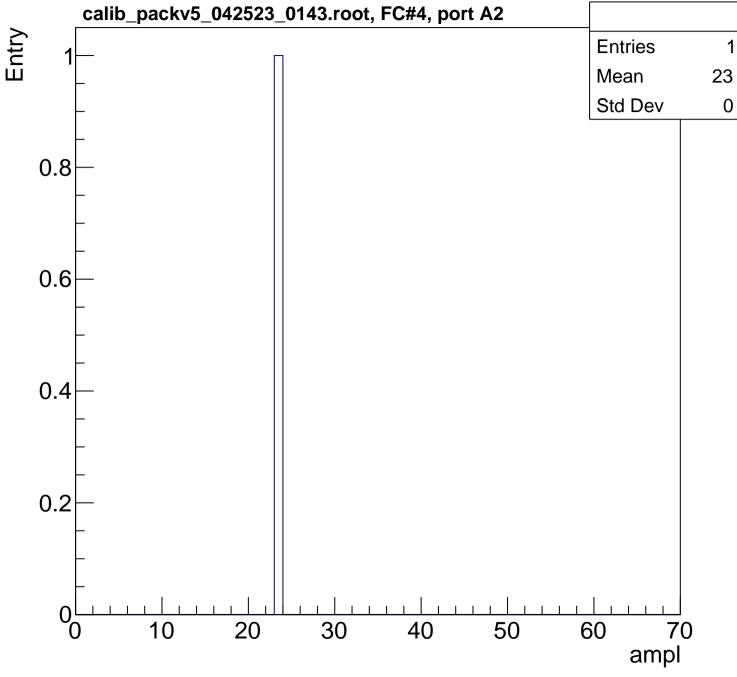


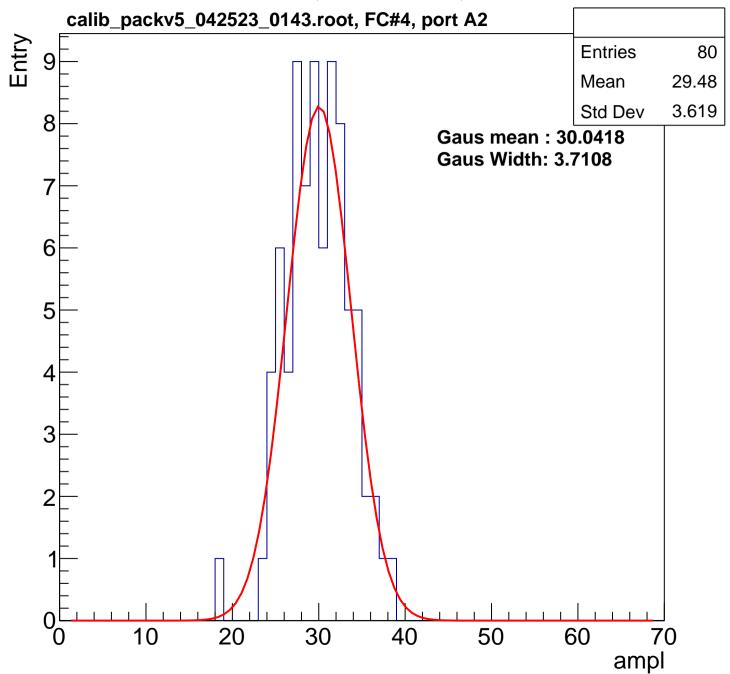


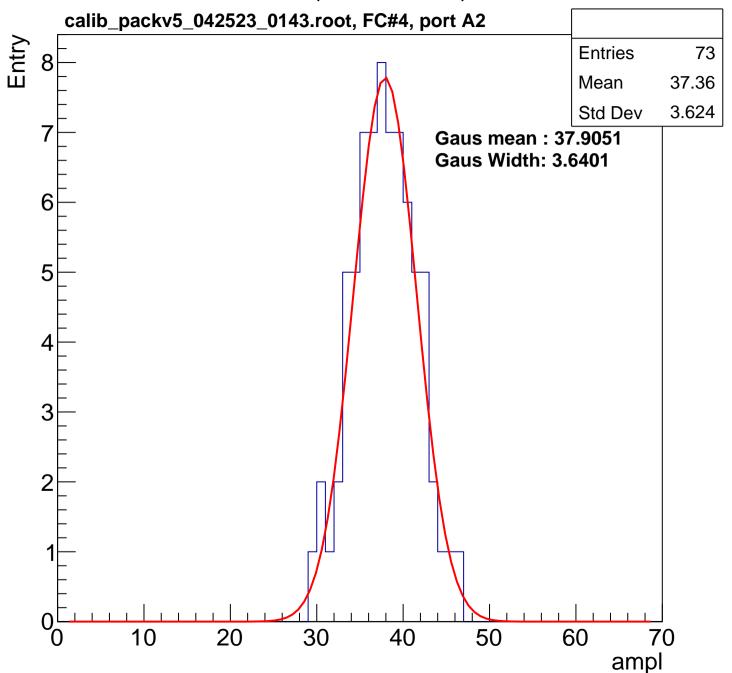


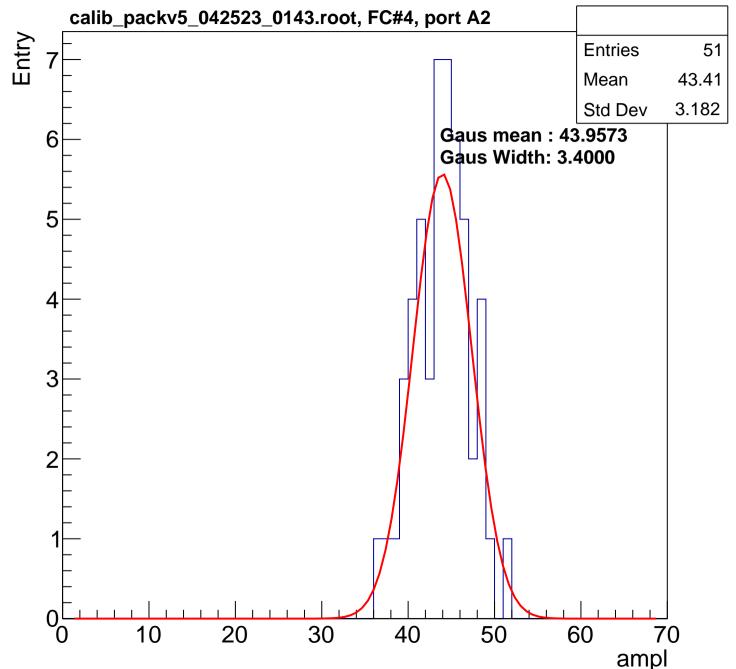


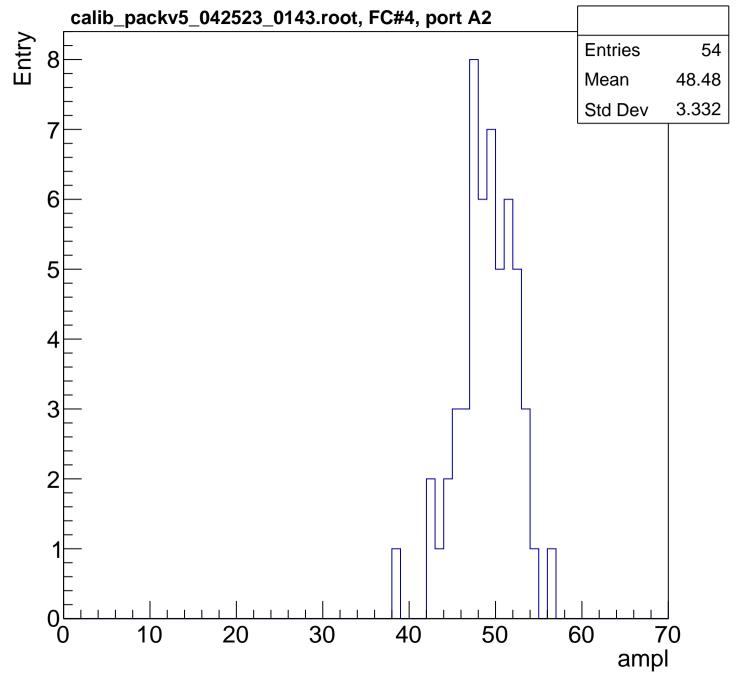


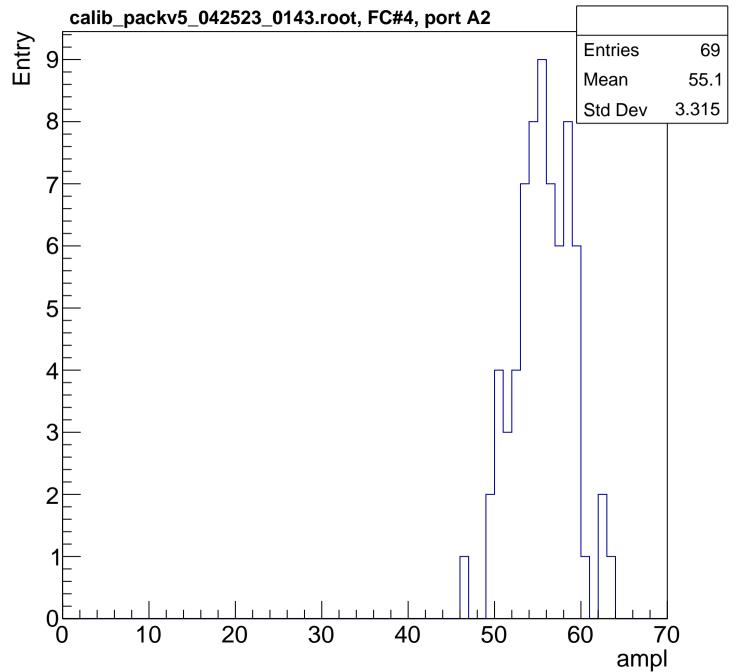


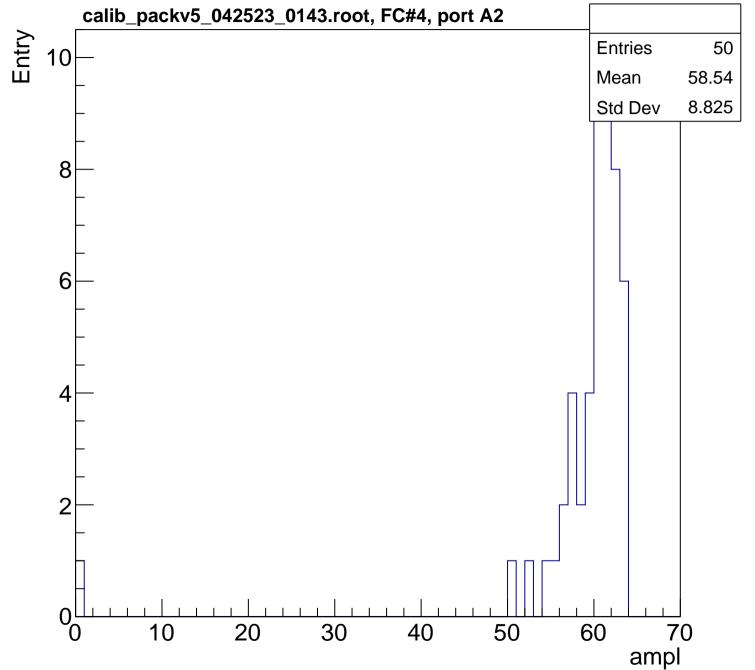


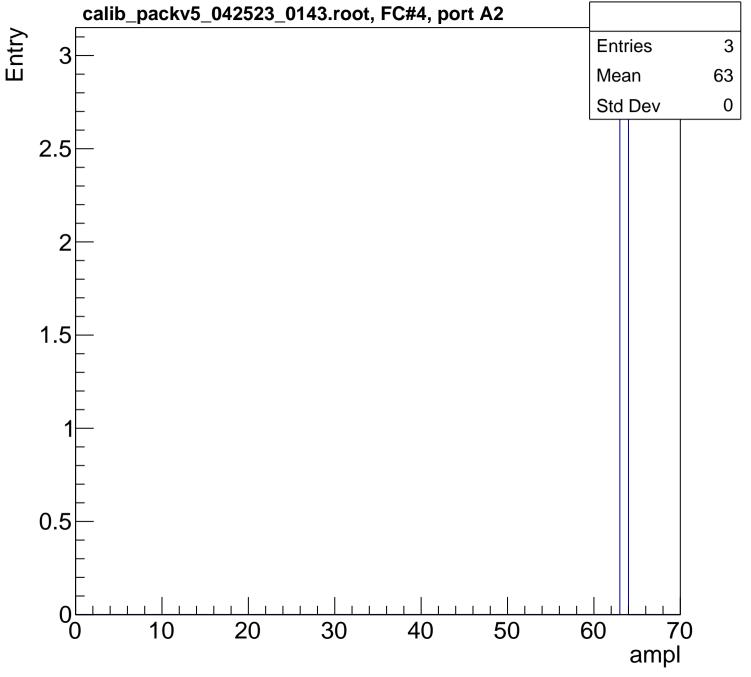




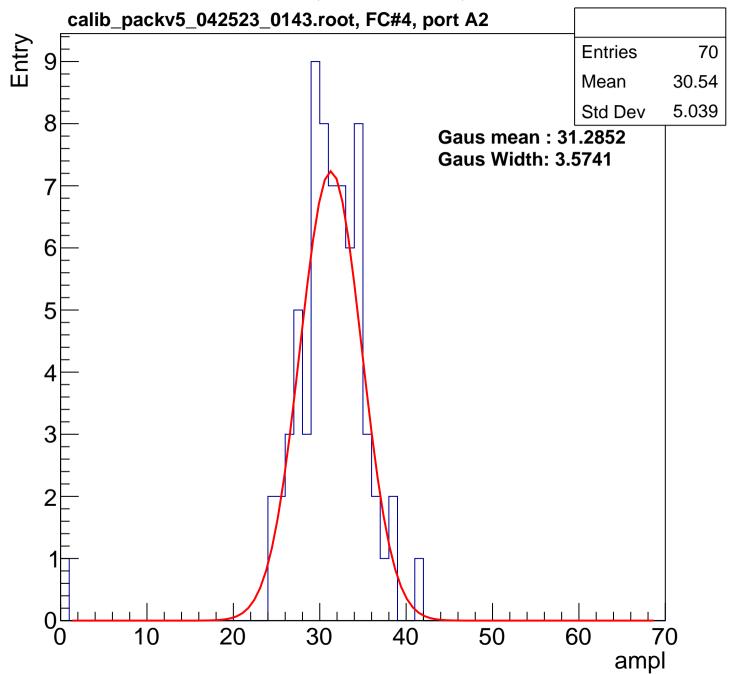


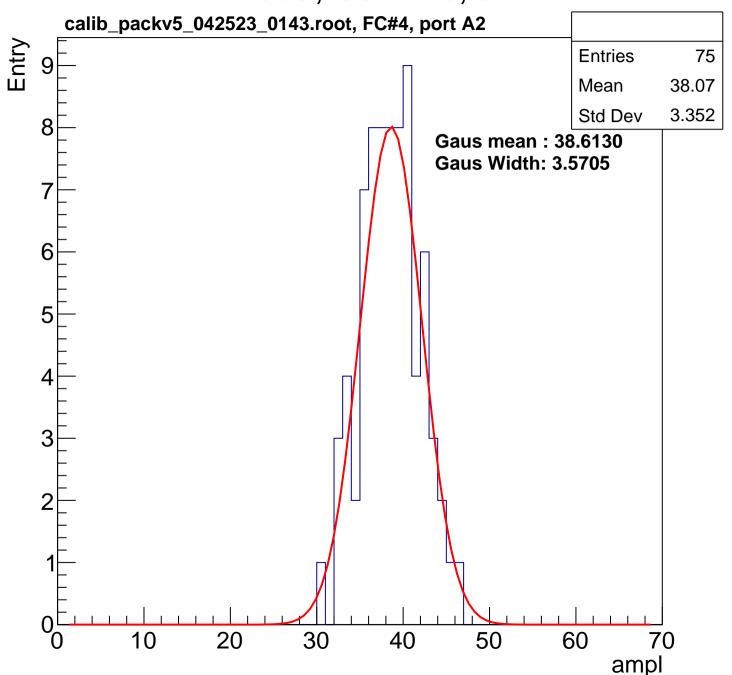


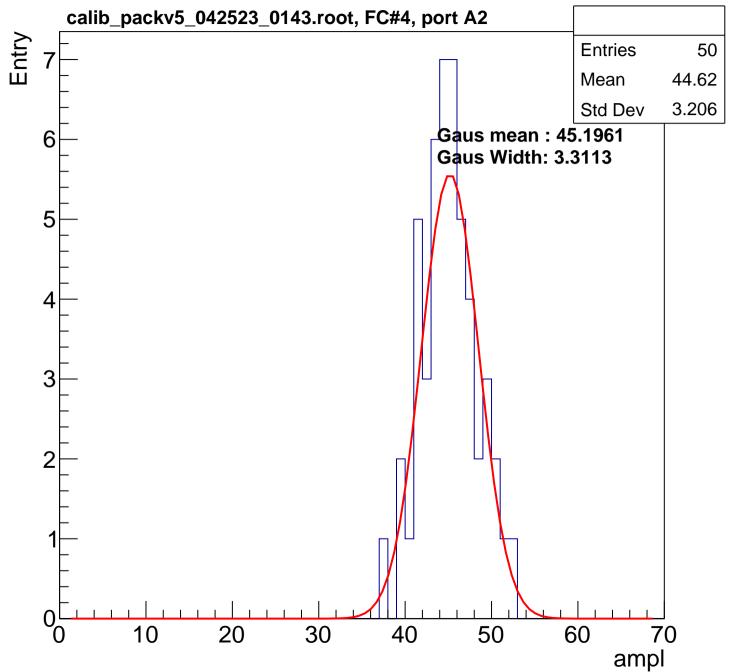


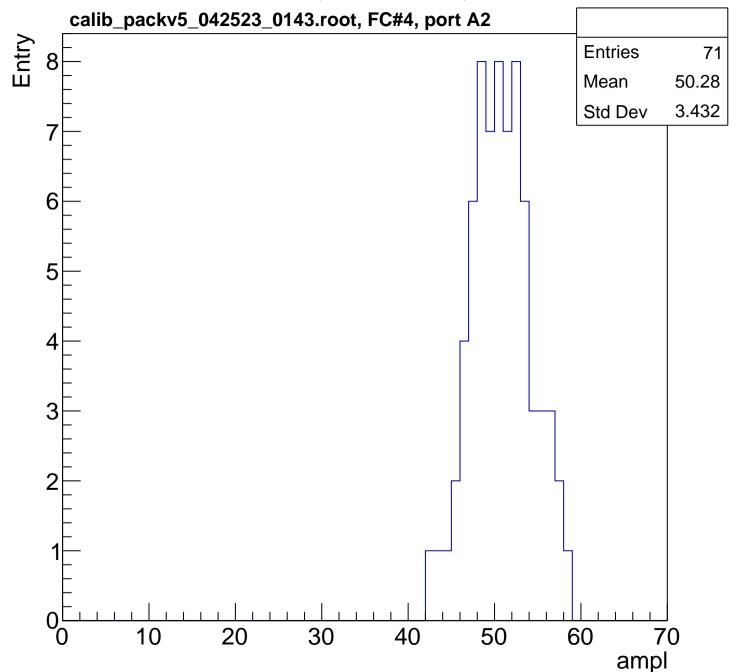


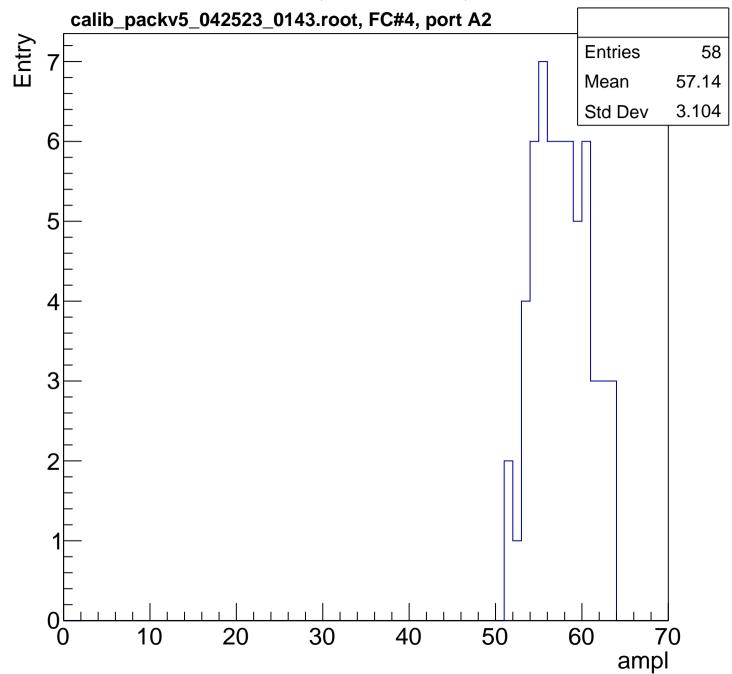
B1L100S, U8-ch78, adc7 calib_packv5_042523_0143.root, FC#4, port A2 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

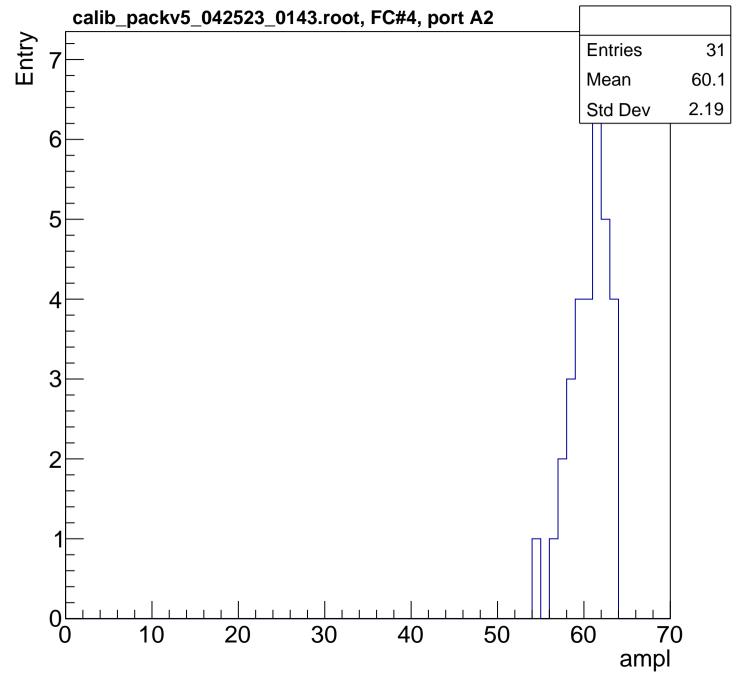


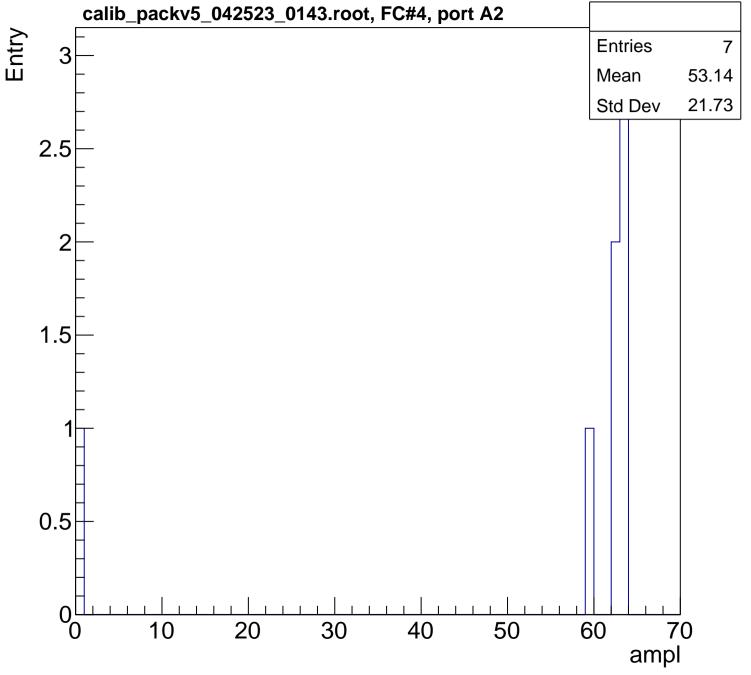










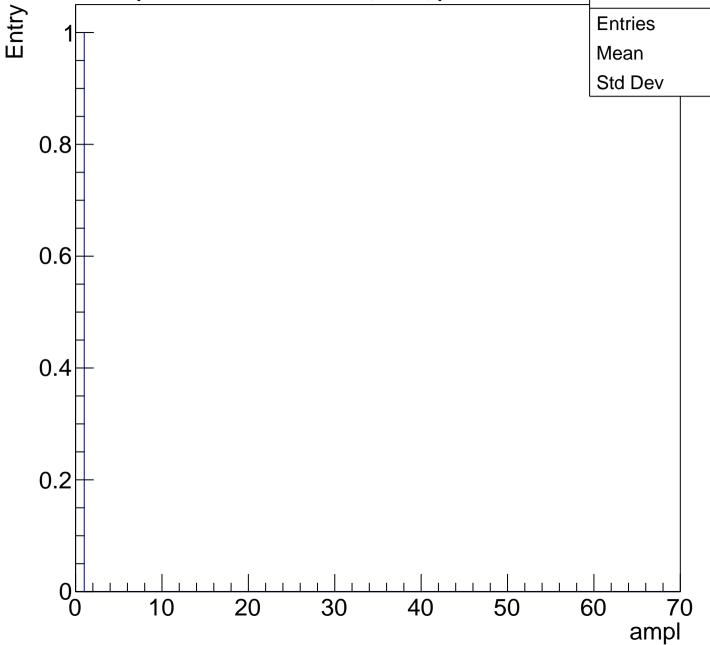


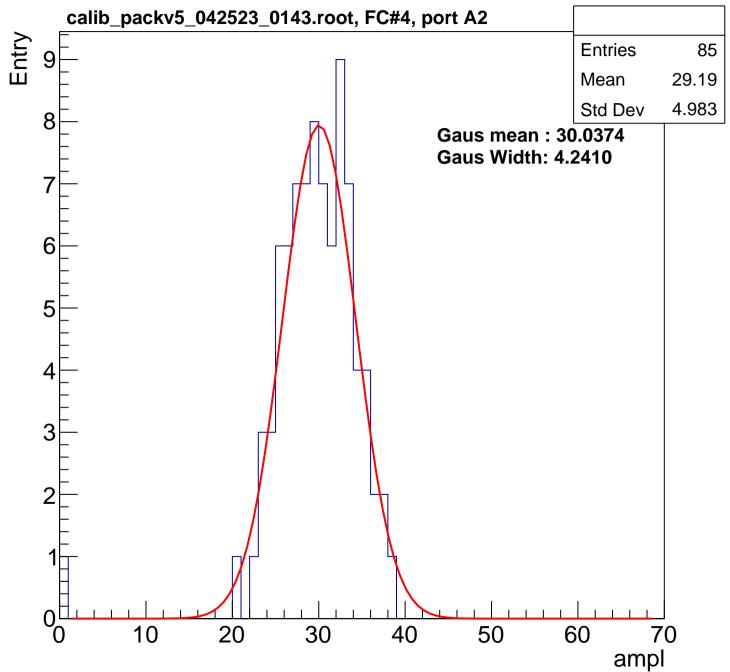
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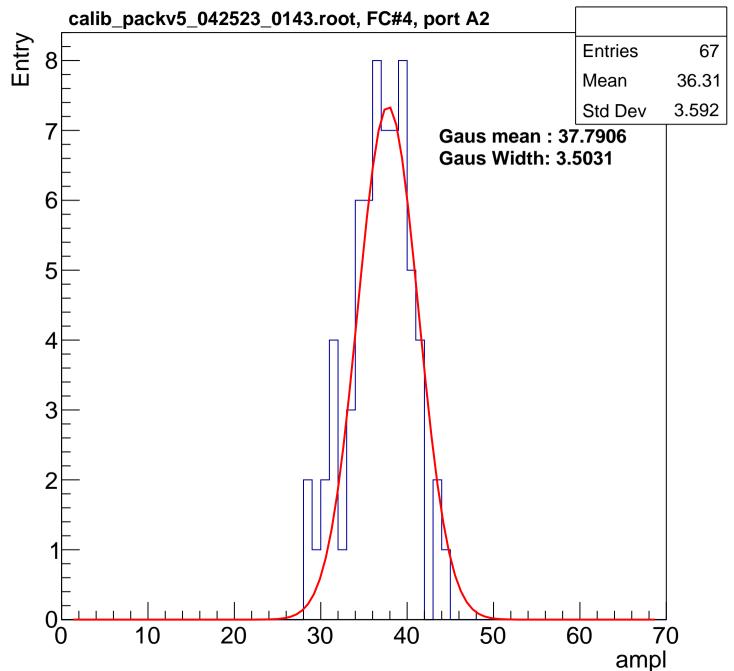
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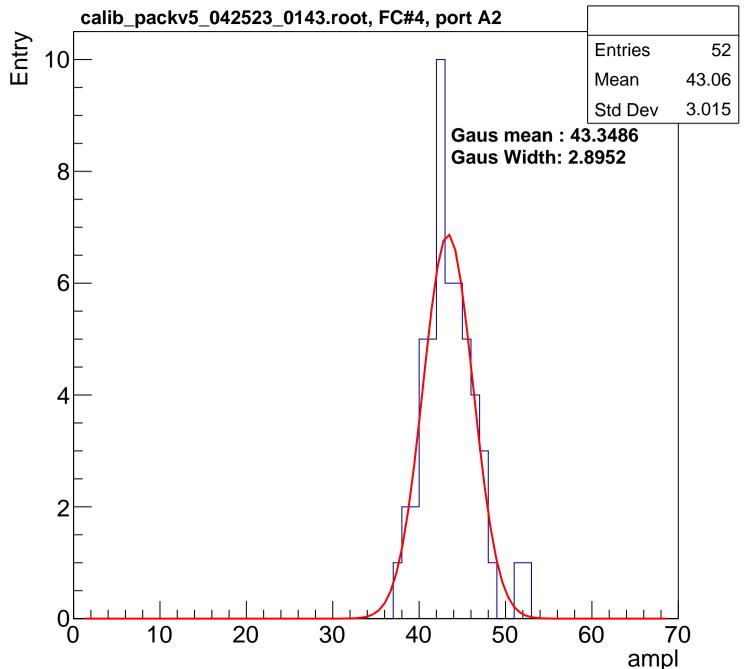
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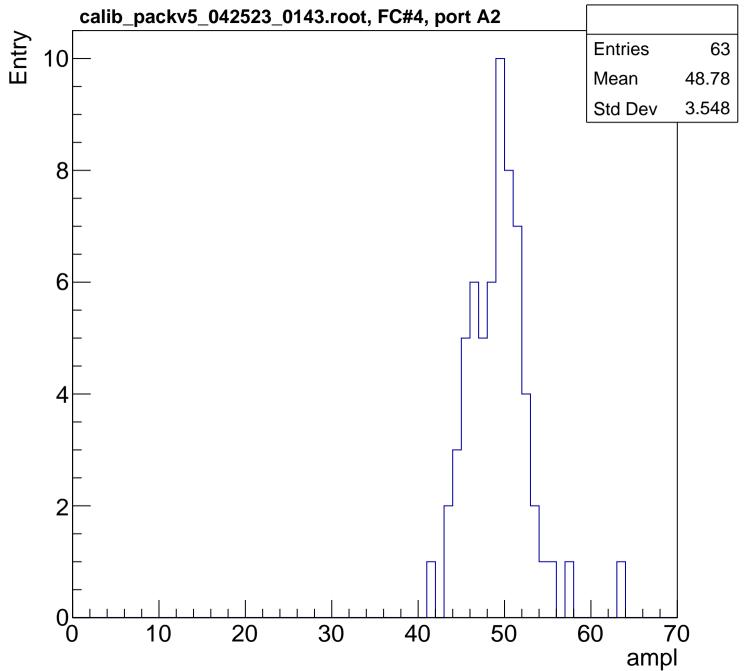
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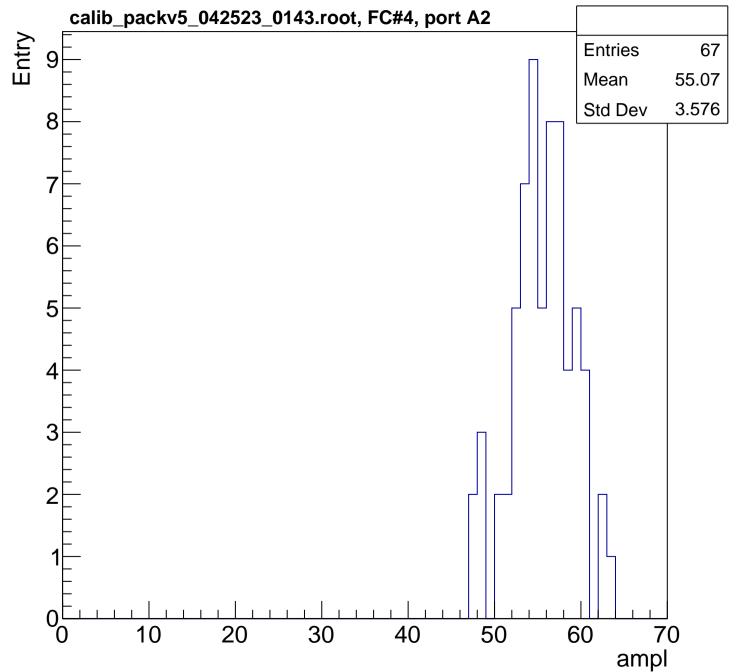


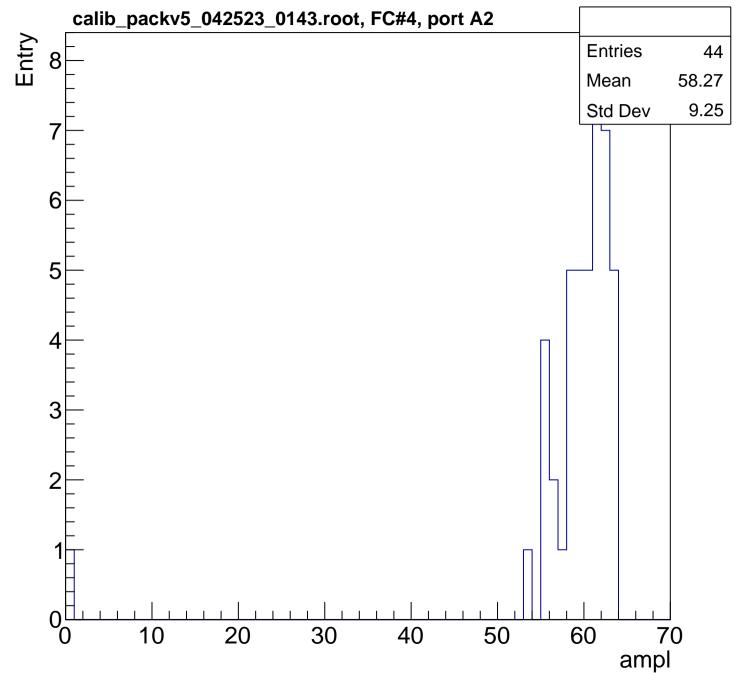


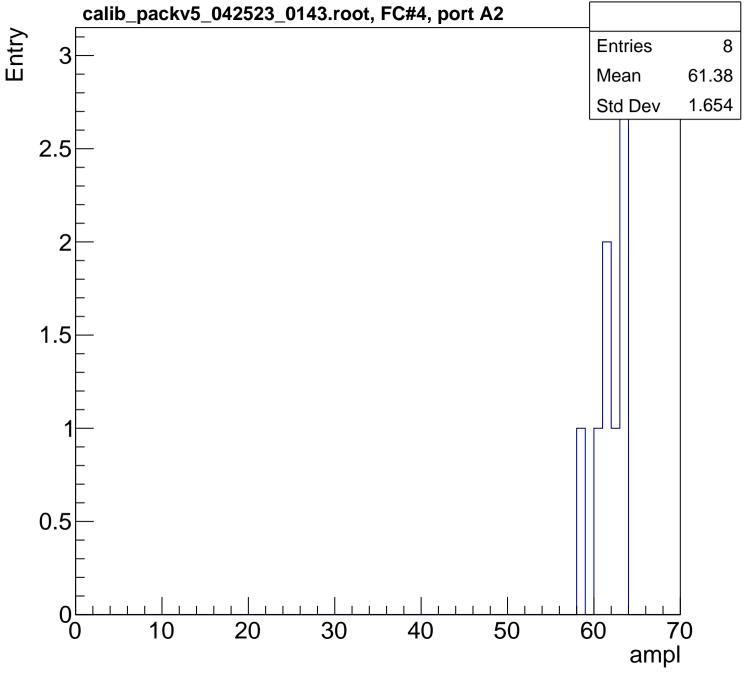


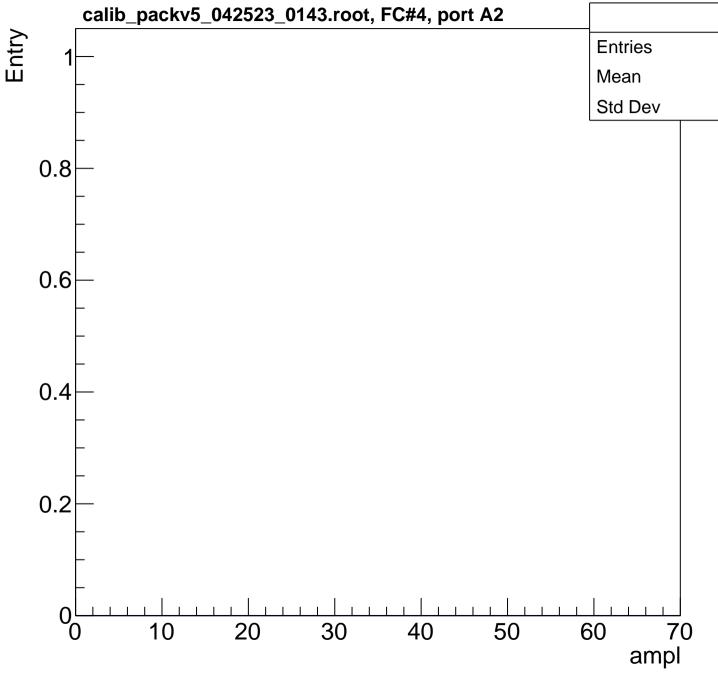


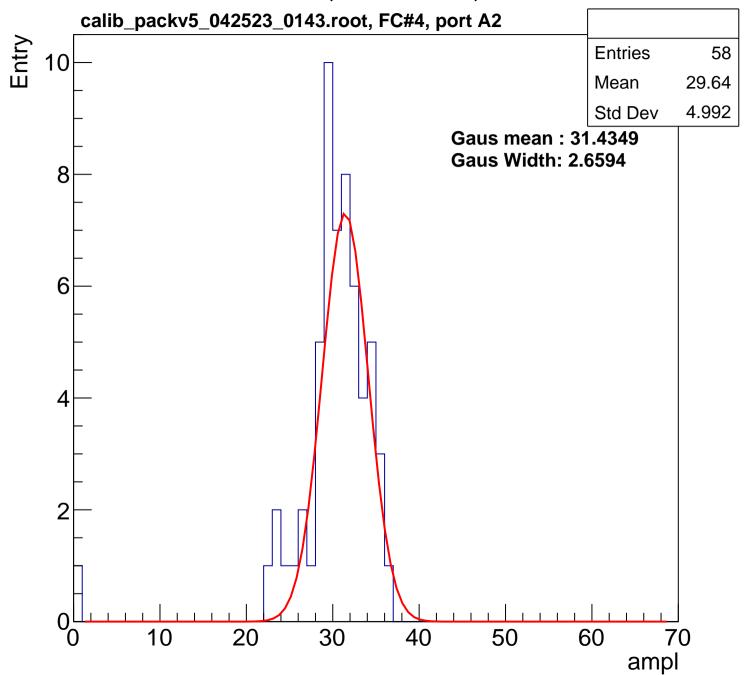


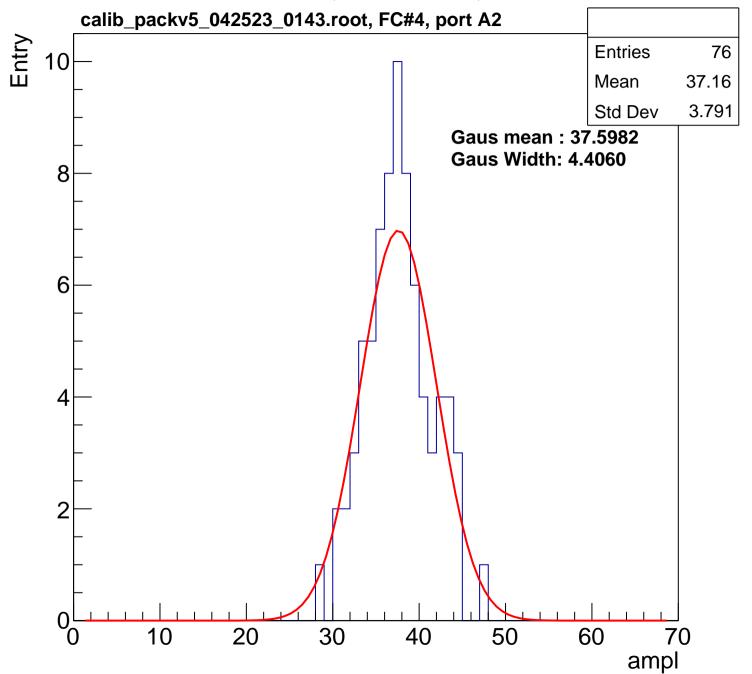


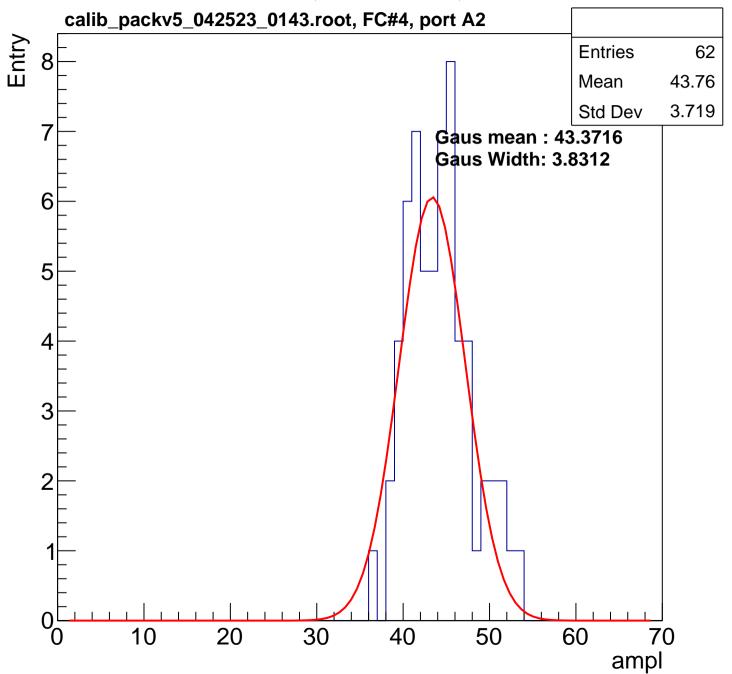


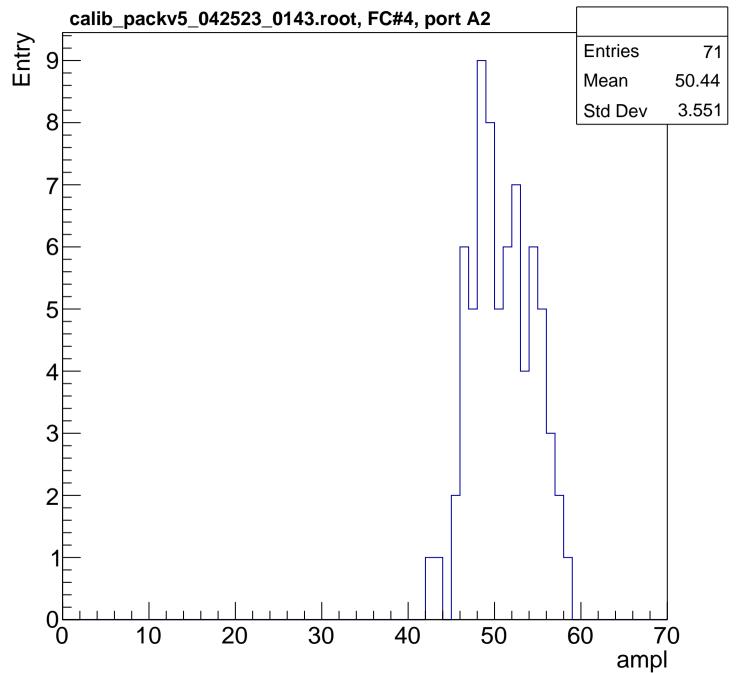


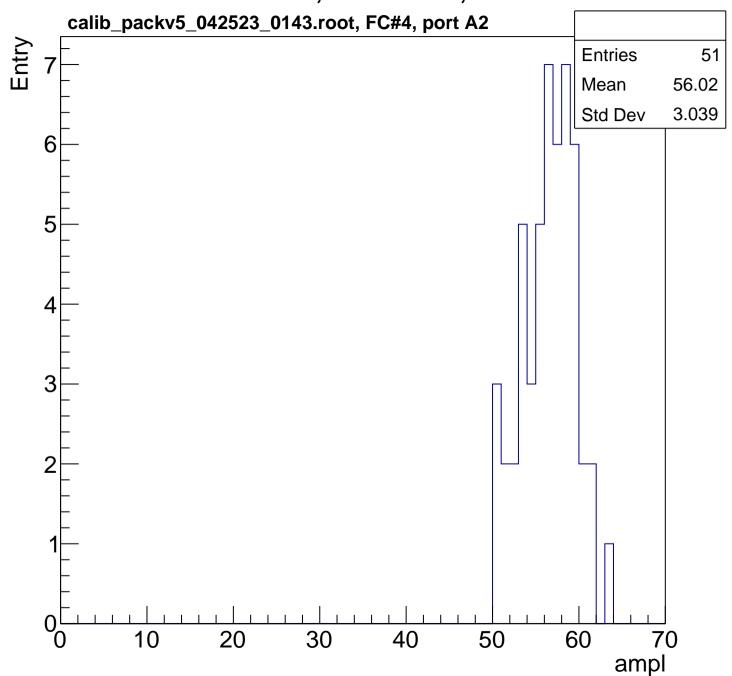


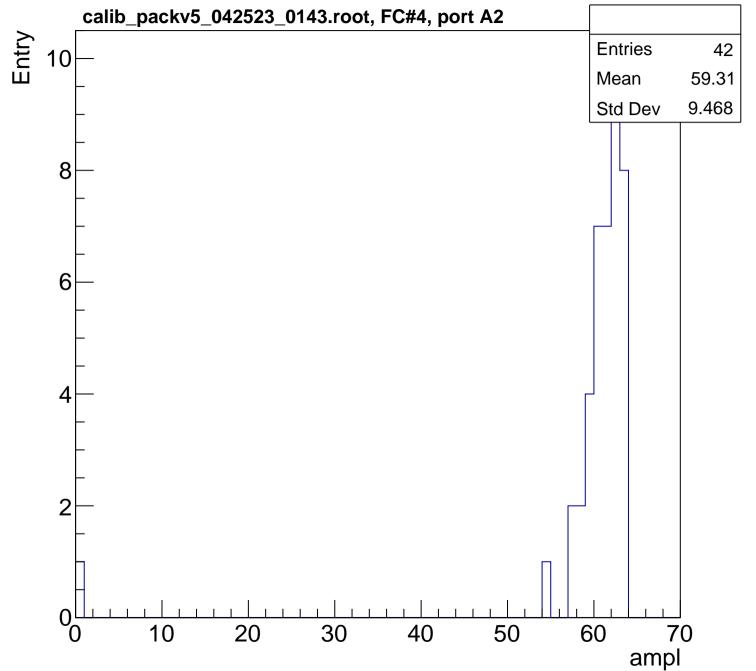


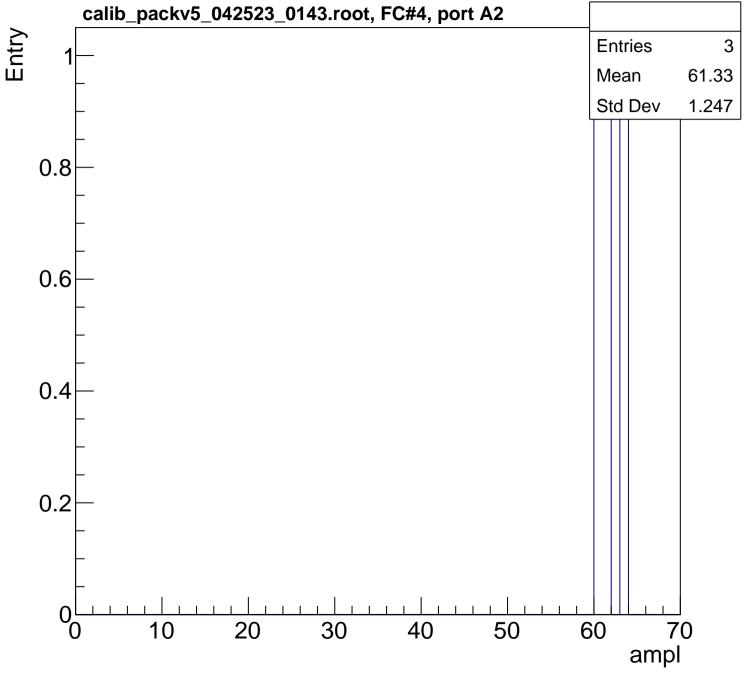




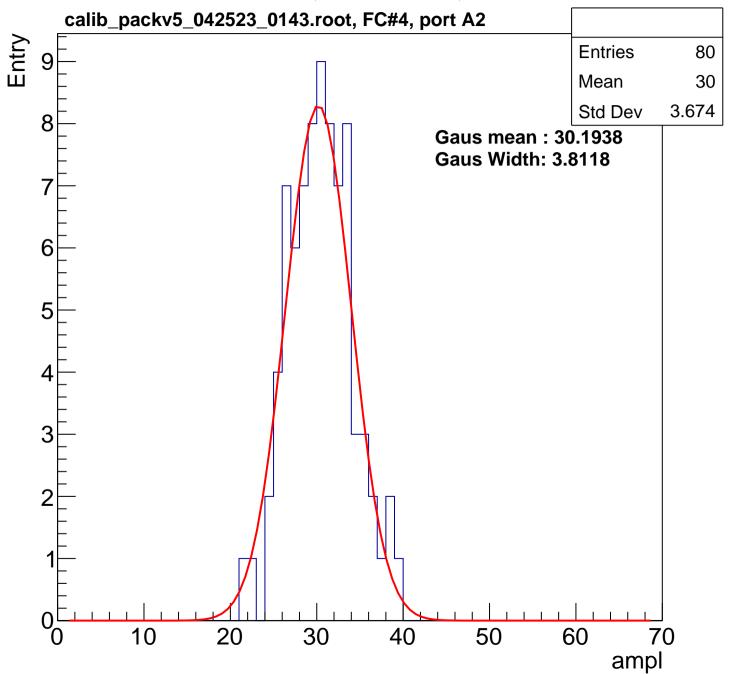


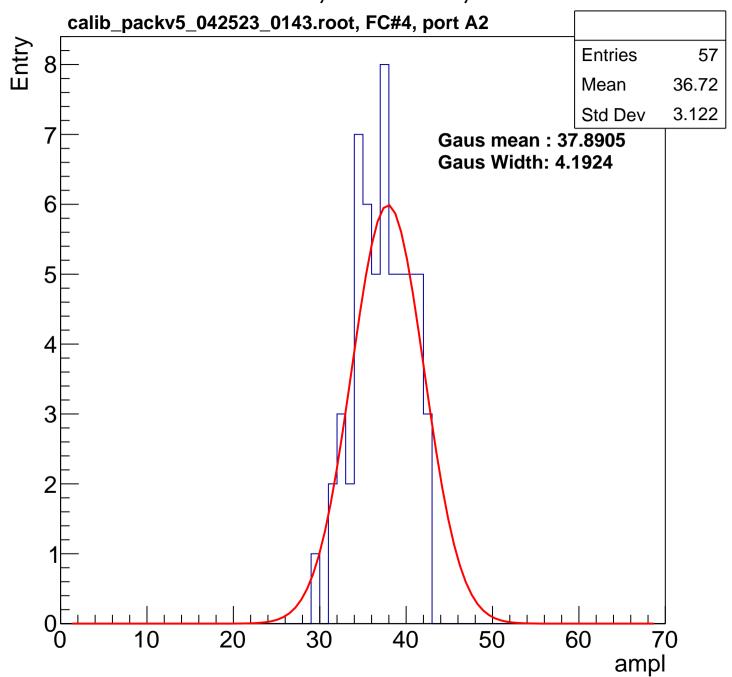


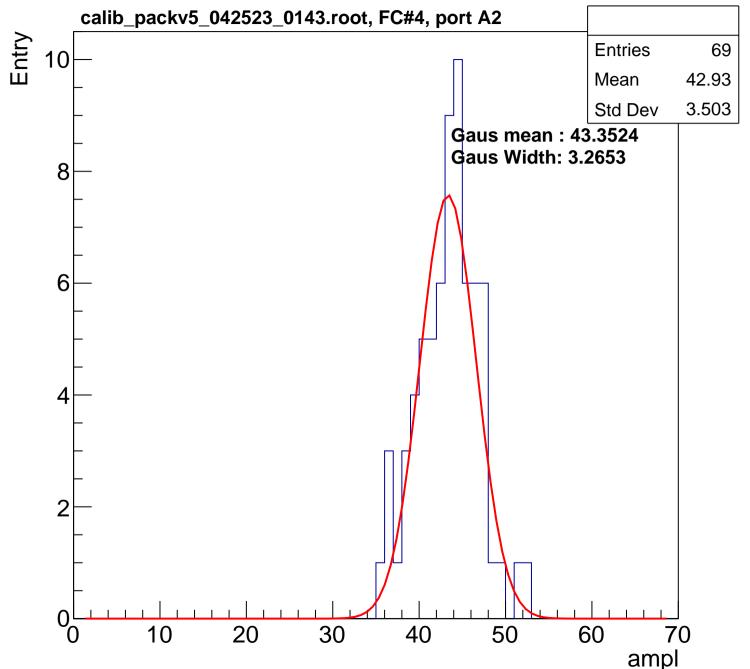


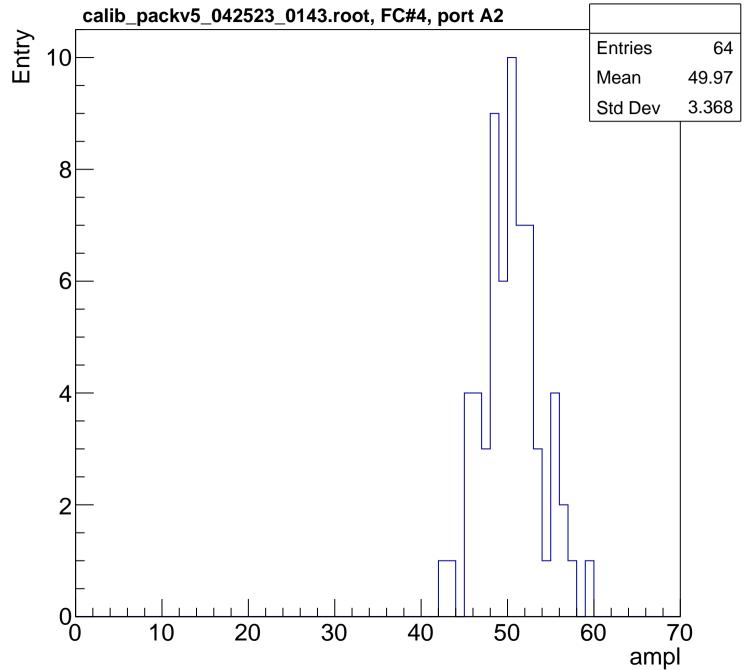


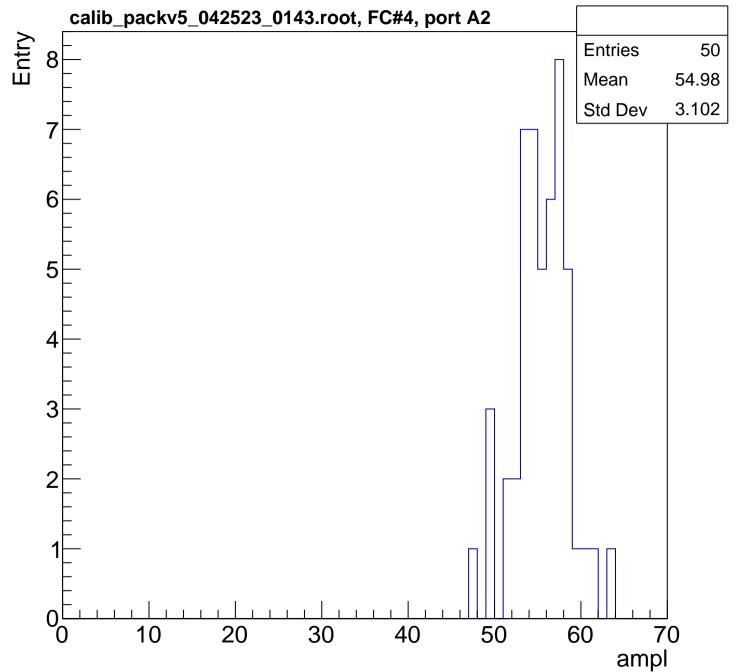


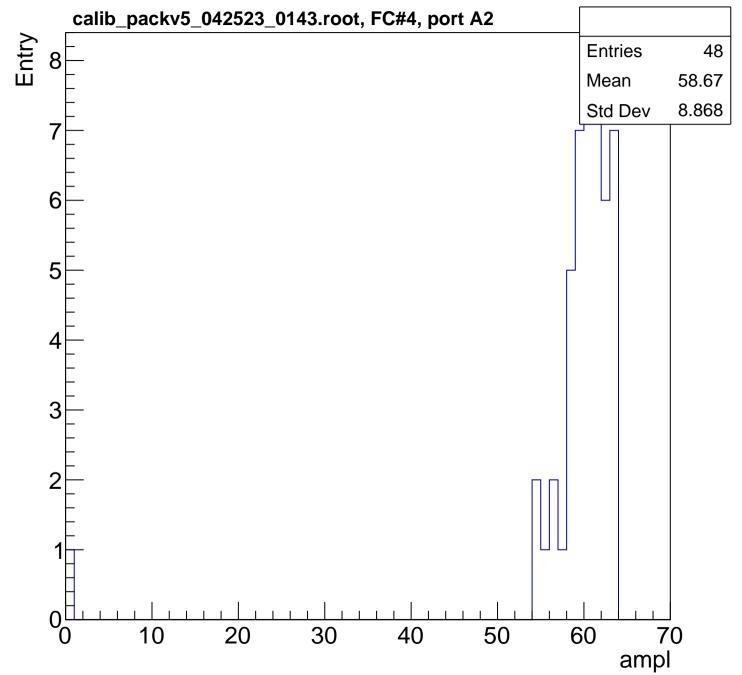


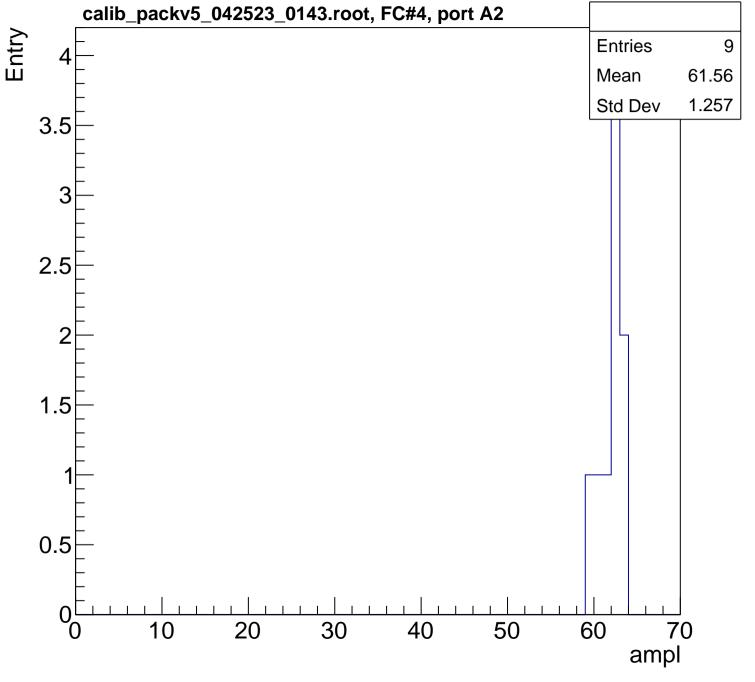












B1L100S, U8-ch82, adc7 calib_packv5_042523_0143.root, FC#4, port A2 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2

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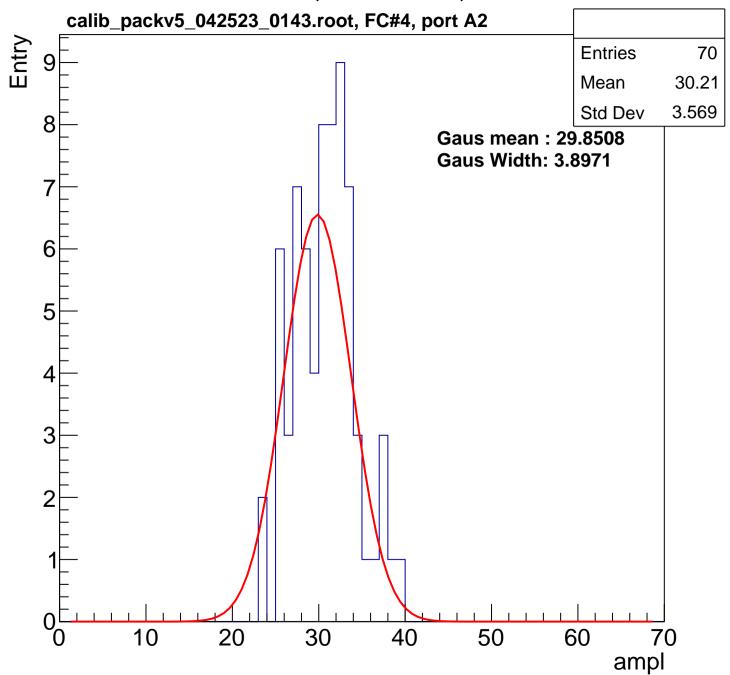
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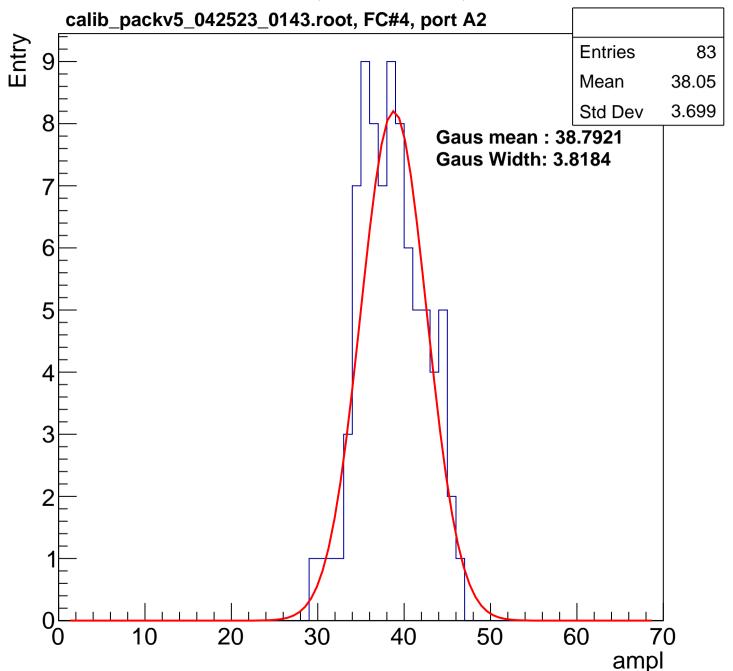
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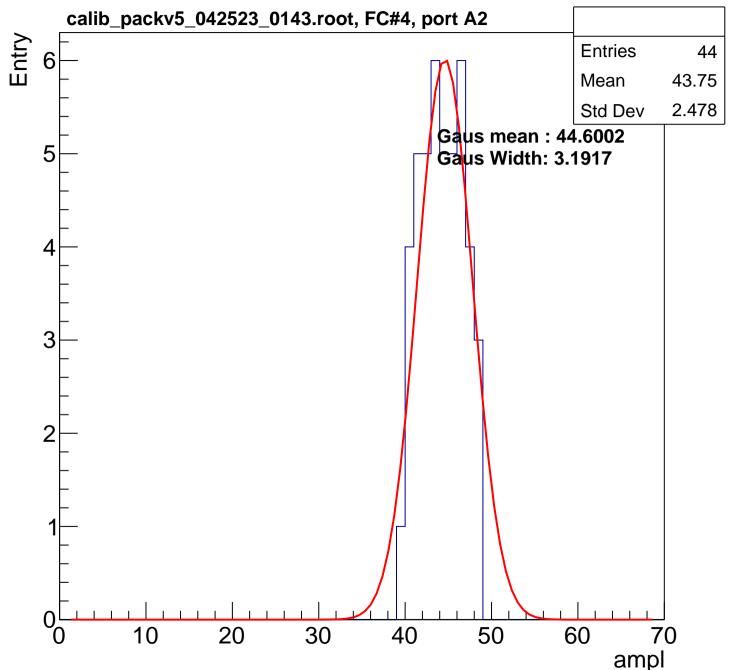
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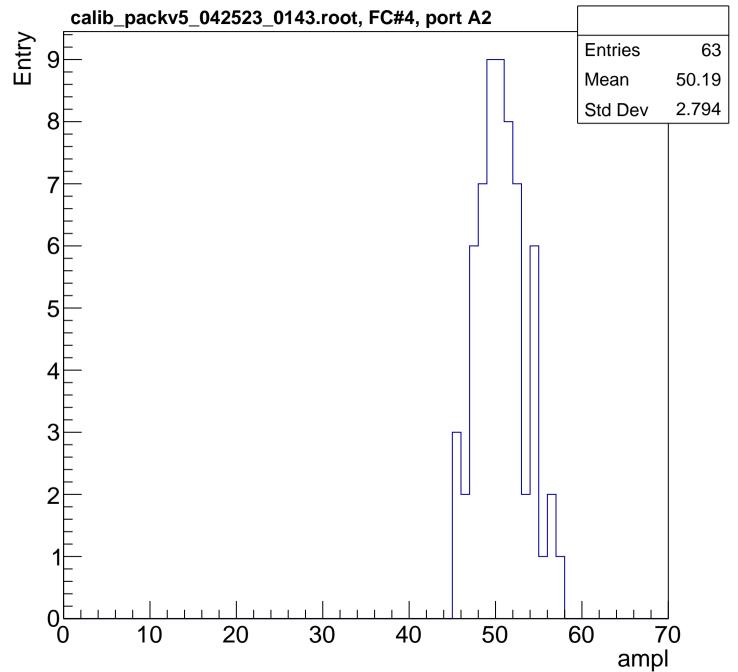
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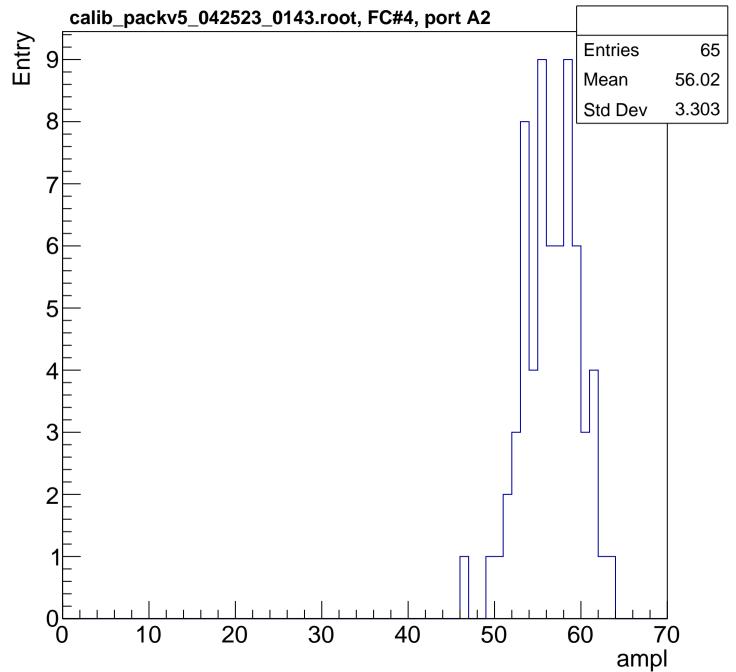
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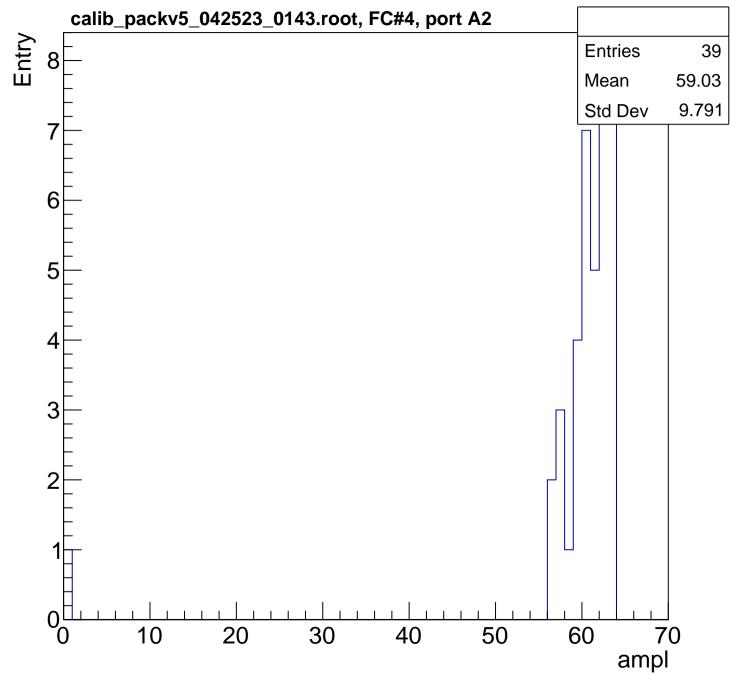


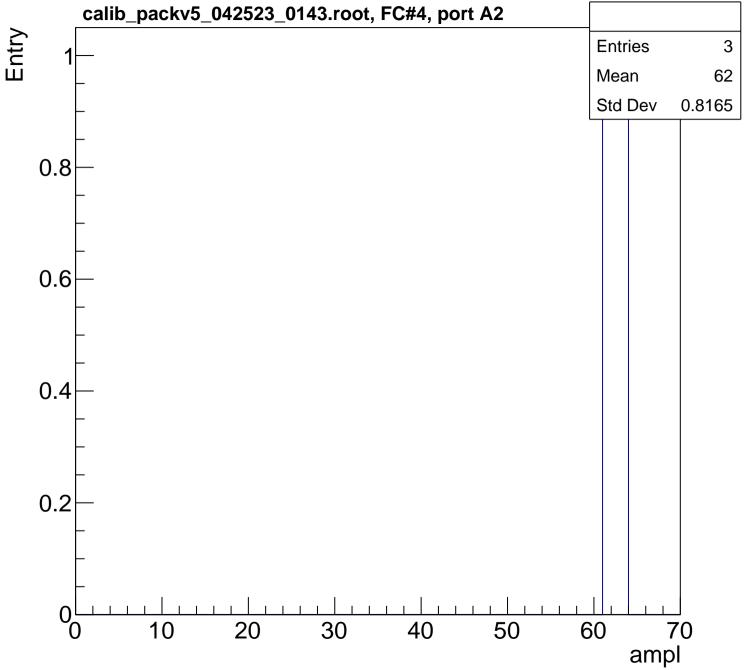


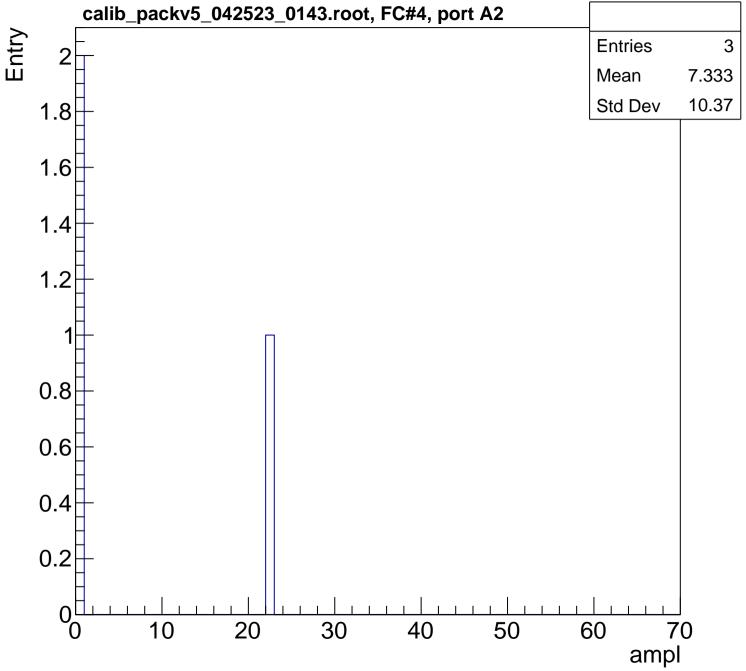


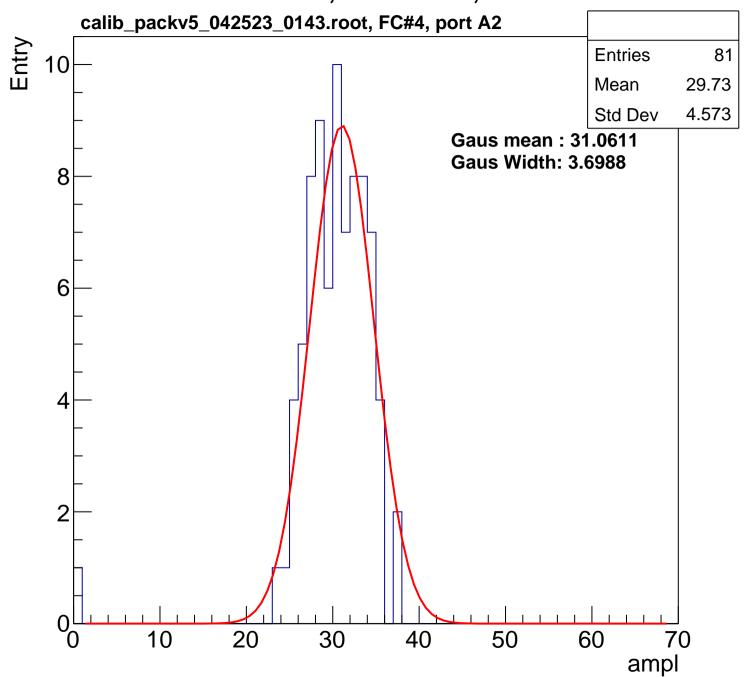


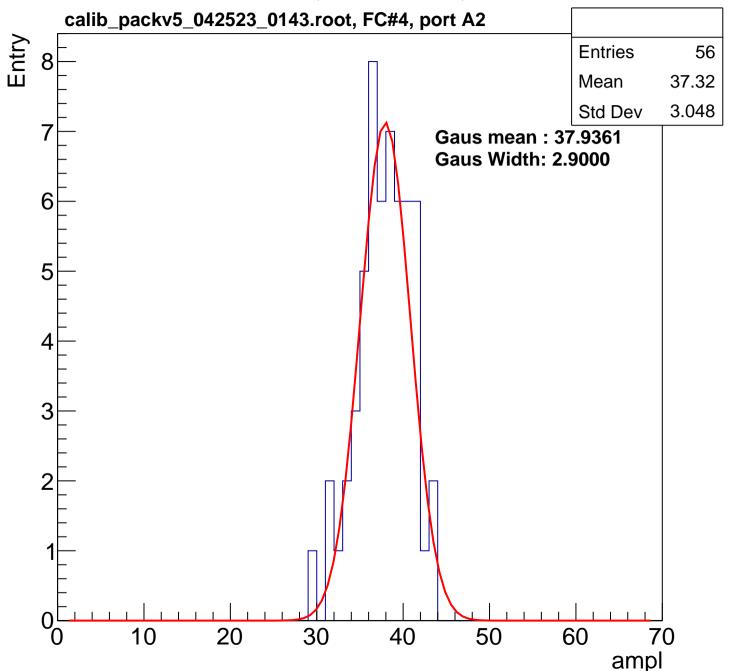


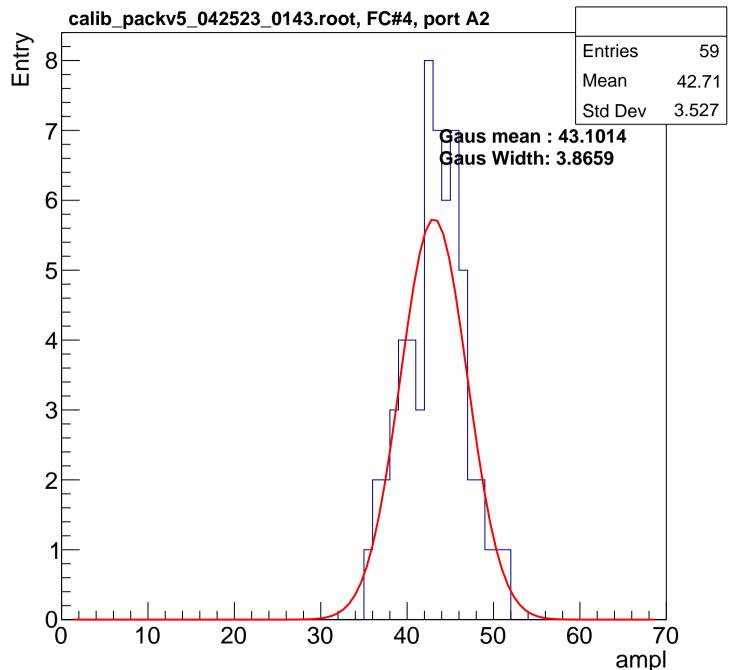


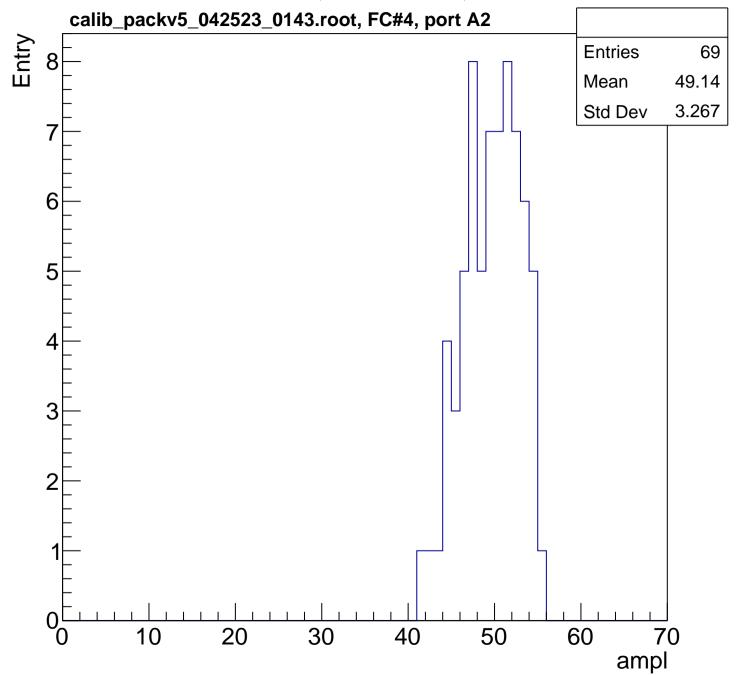


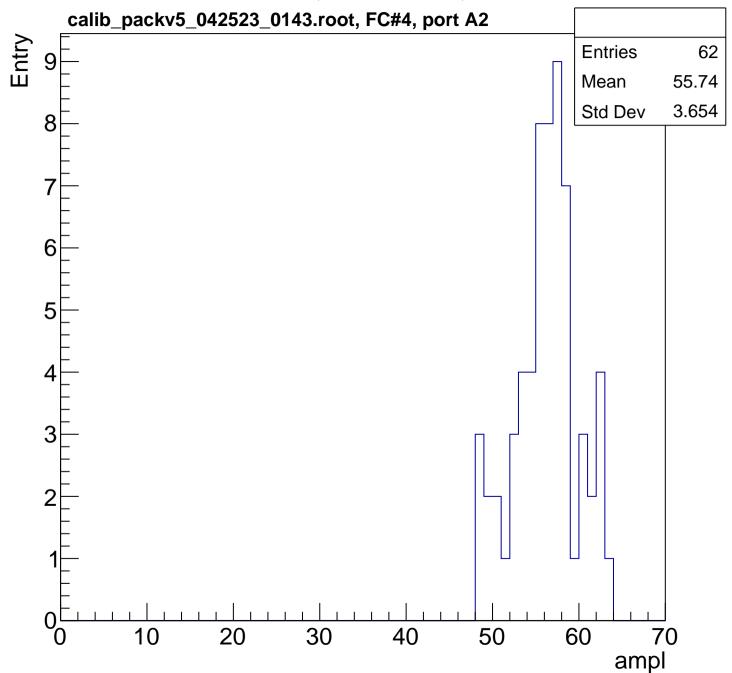


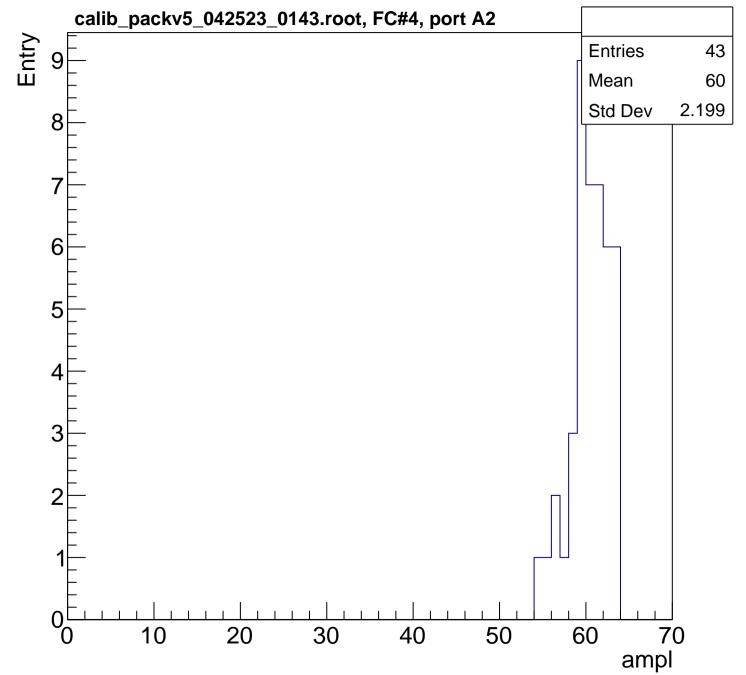


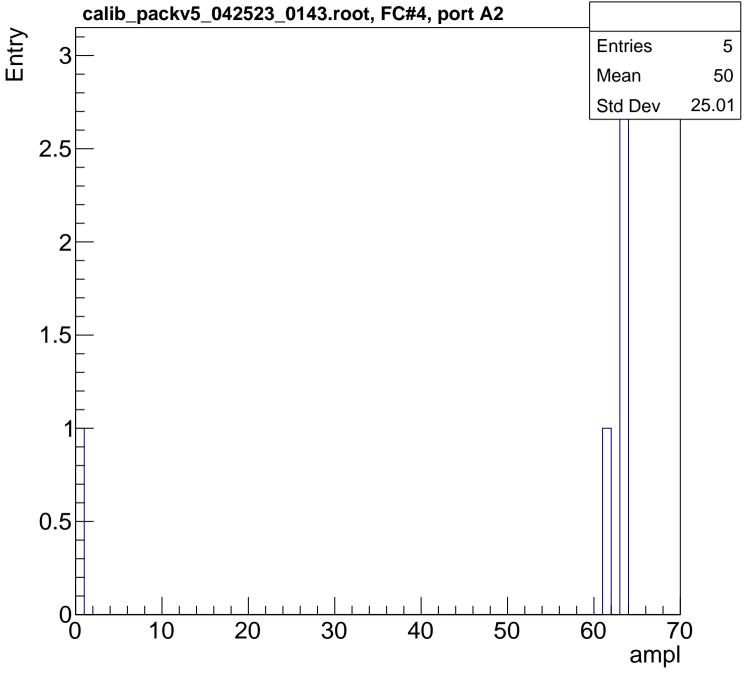


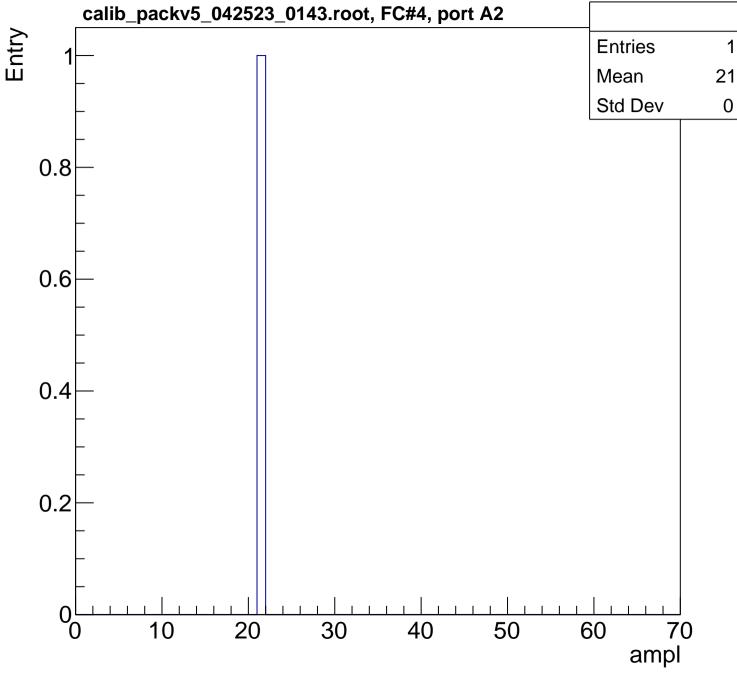


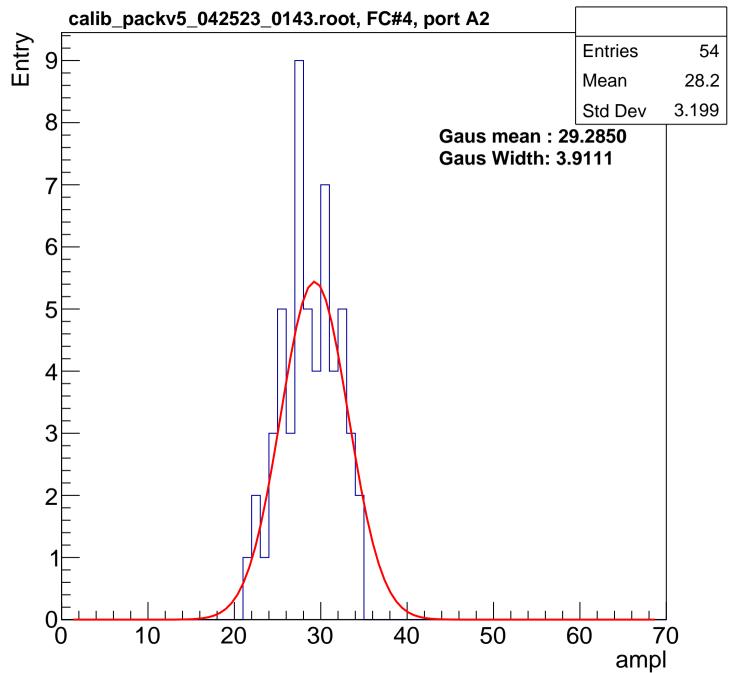


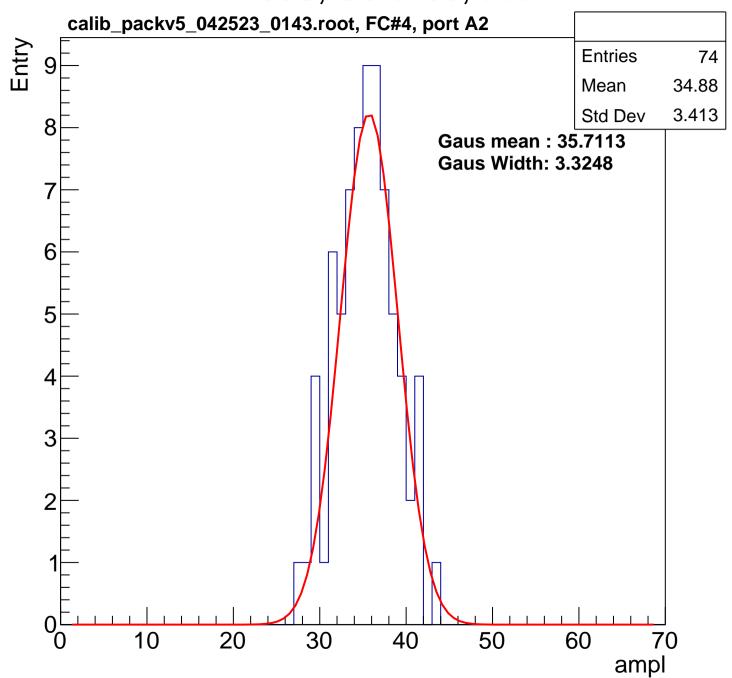


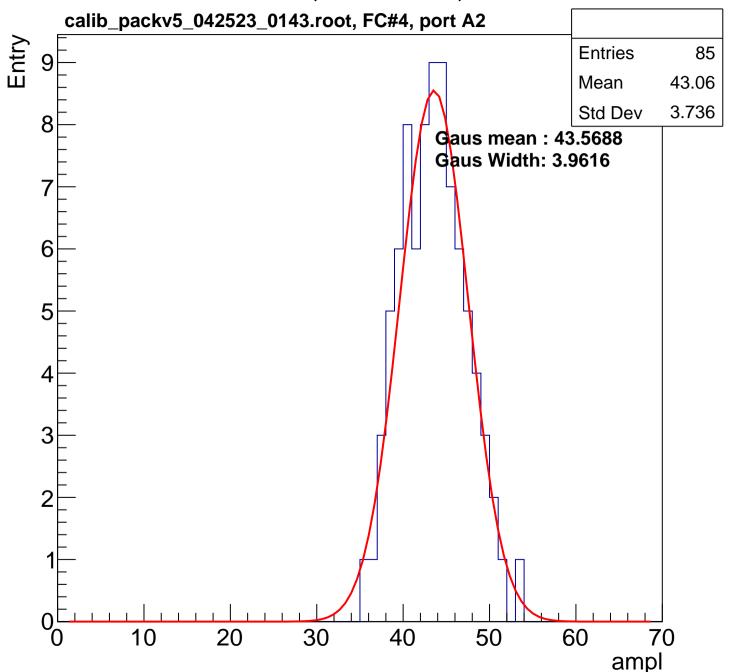


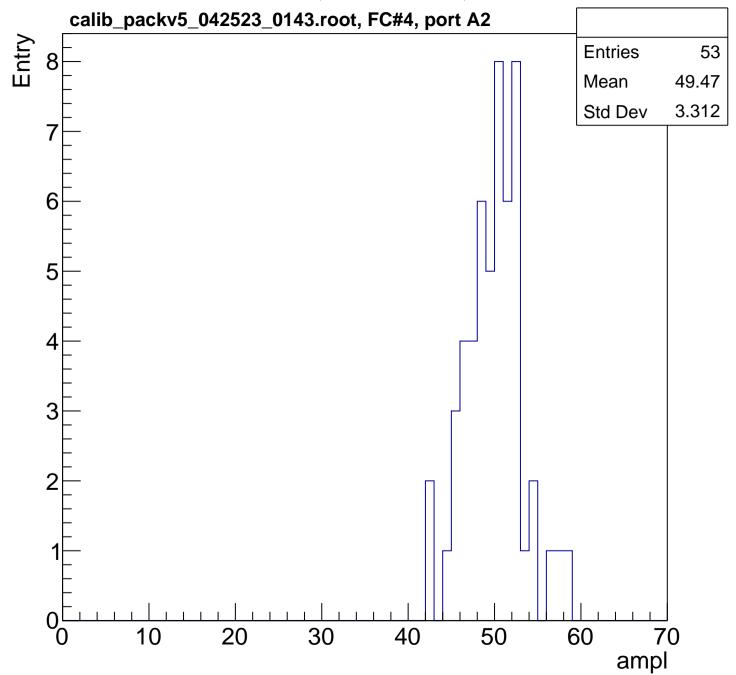


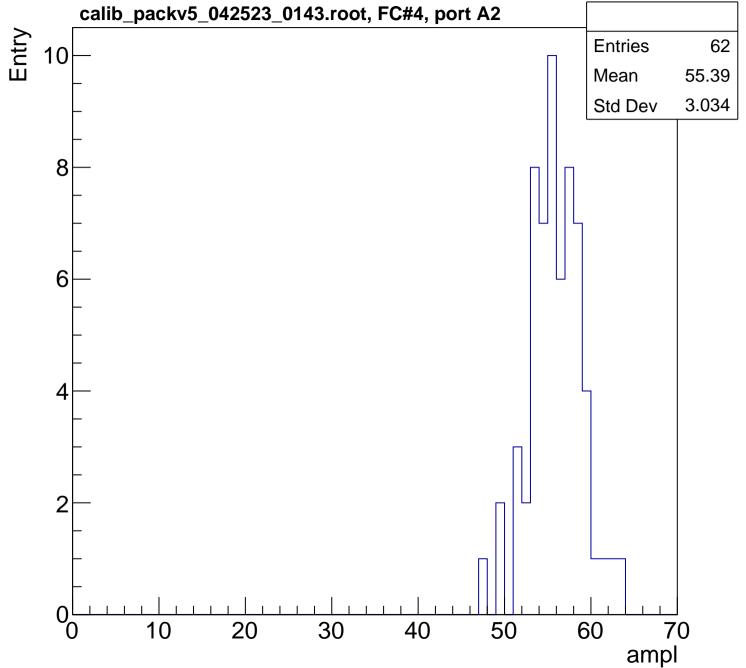


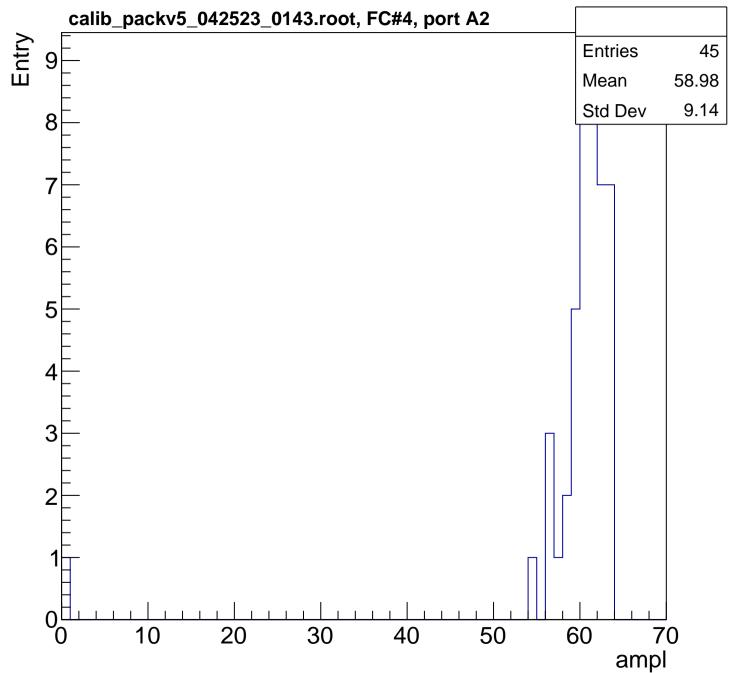


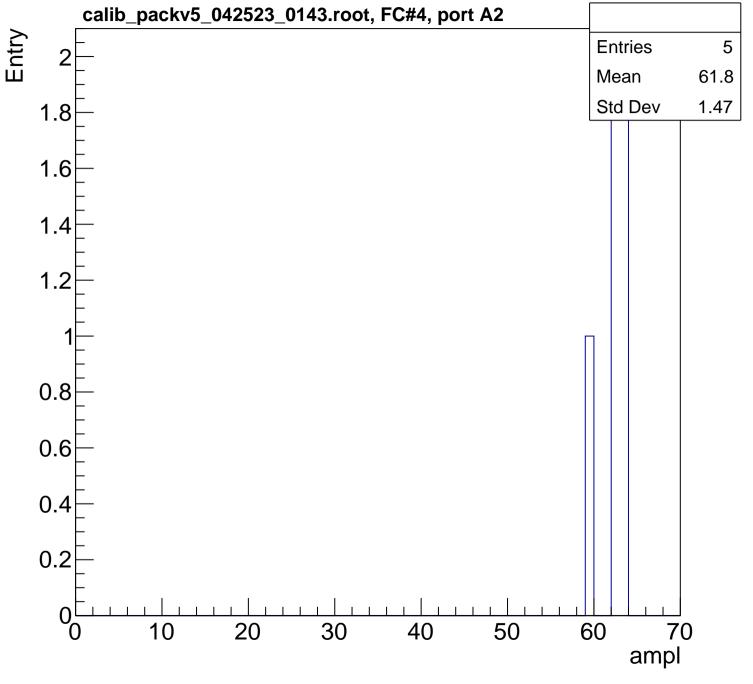












B1L100S, U8-ch85, adc7 calib_packv5_042523_0143.root, FC#4, port A2 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2

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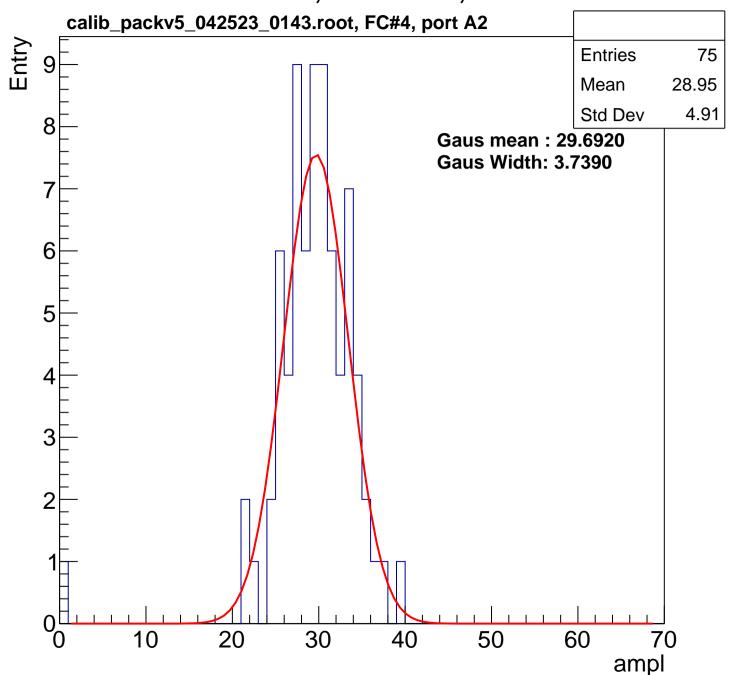
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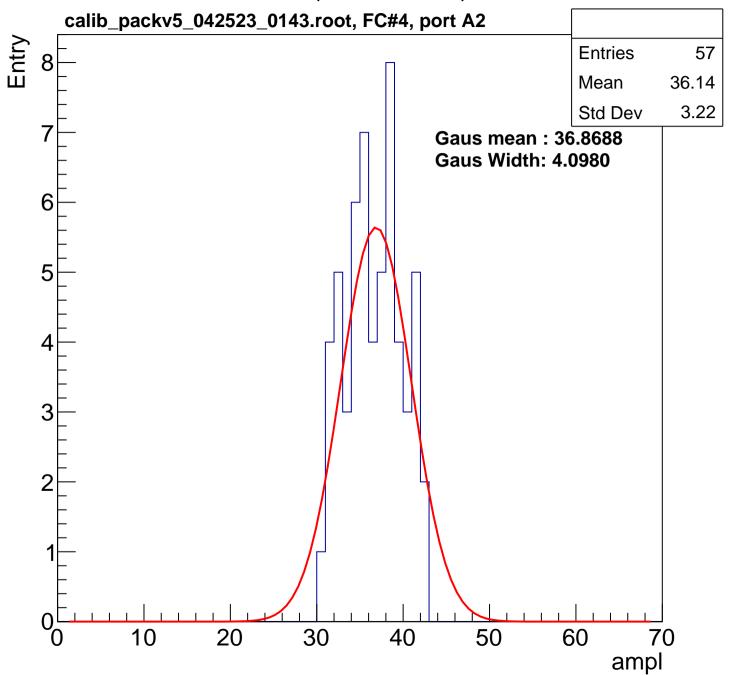
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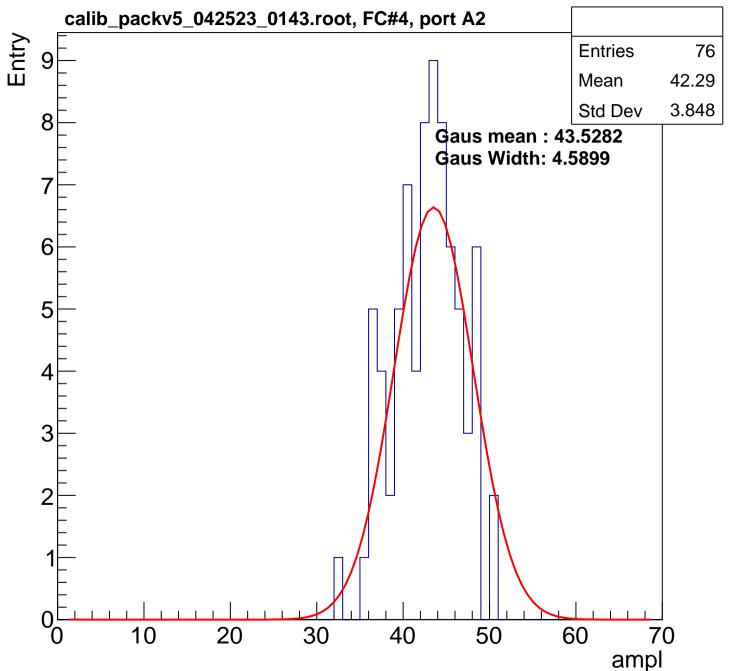
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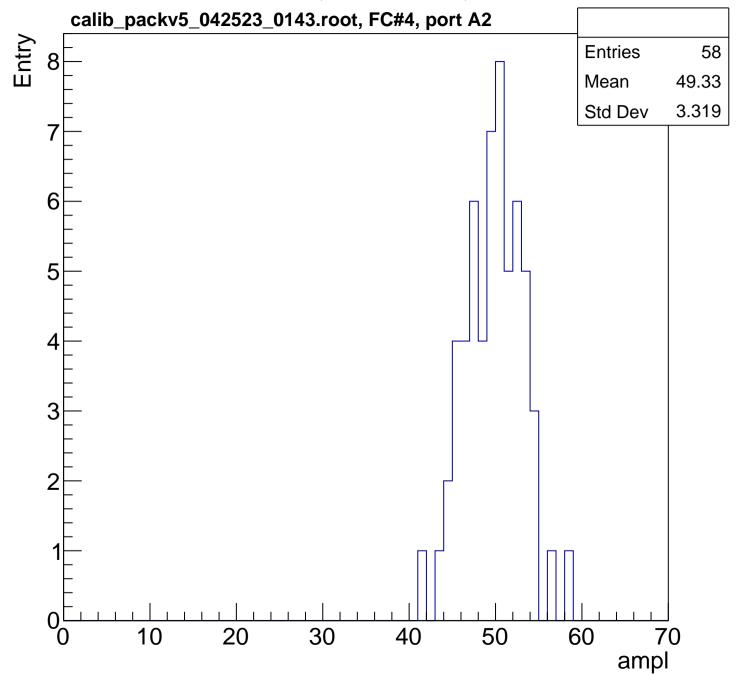
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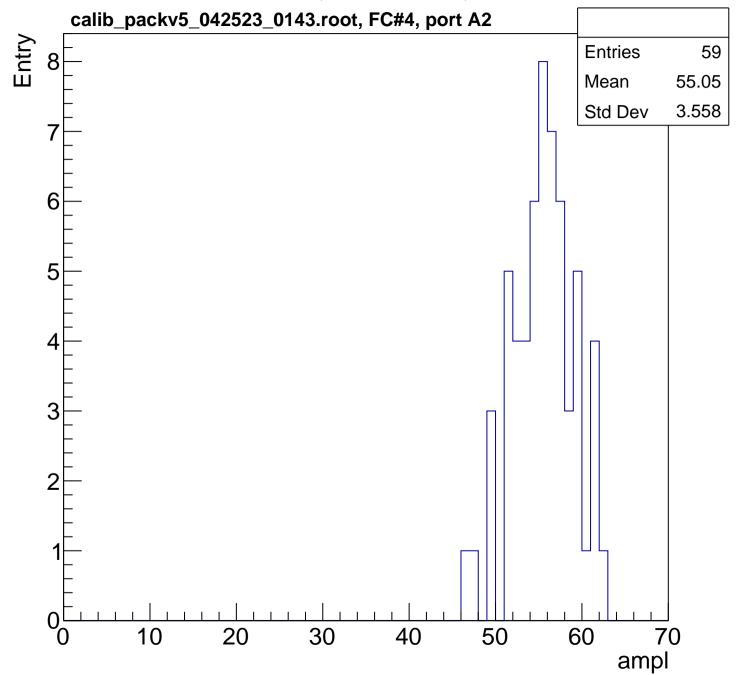
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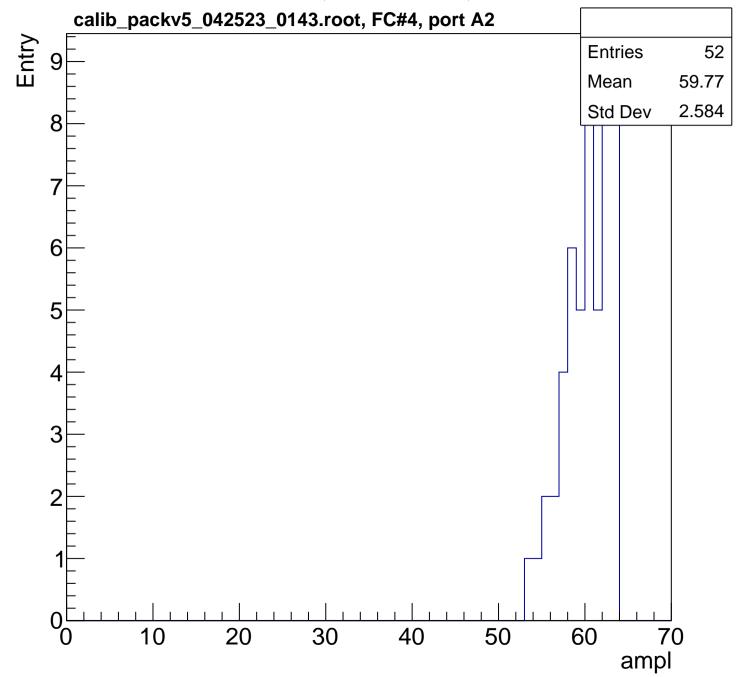


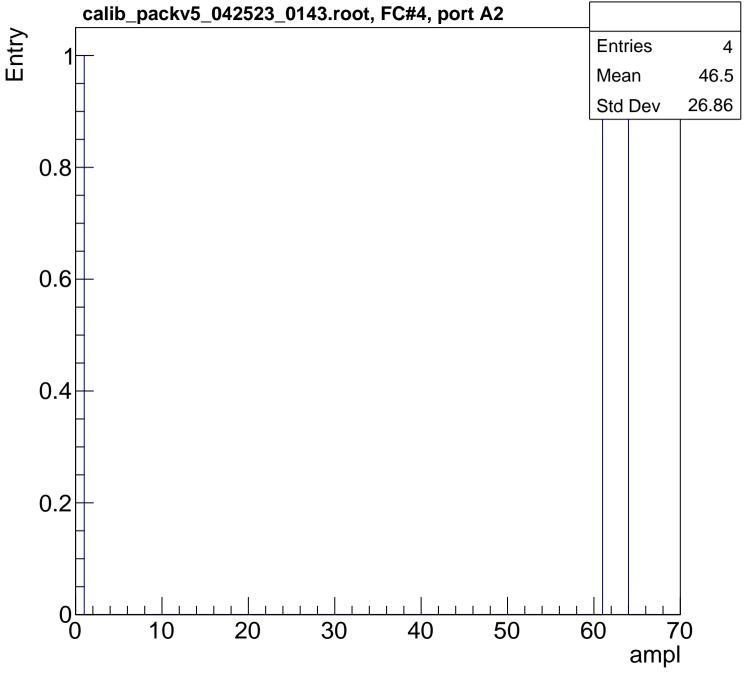




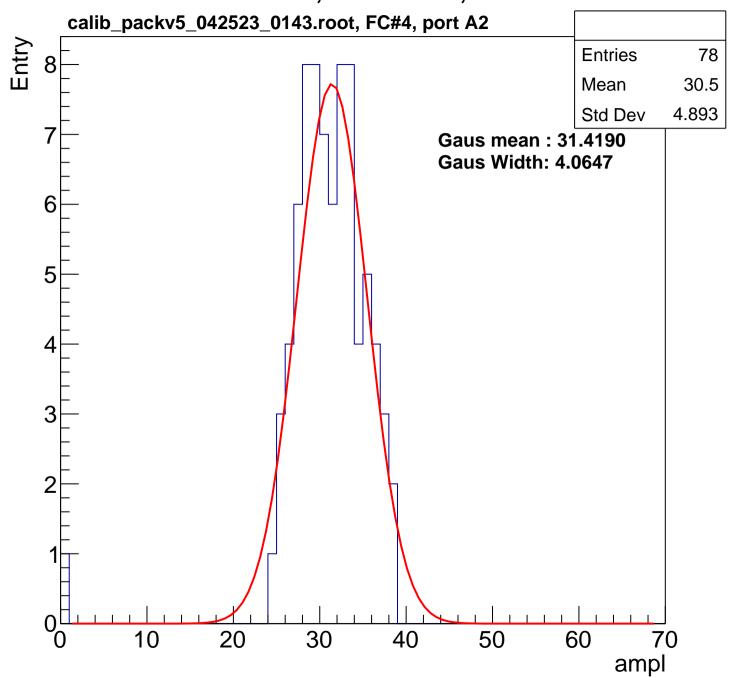


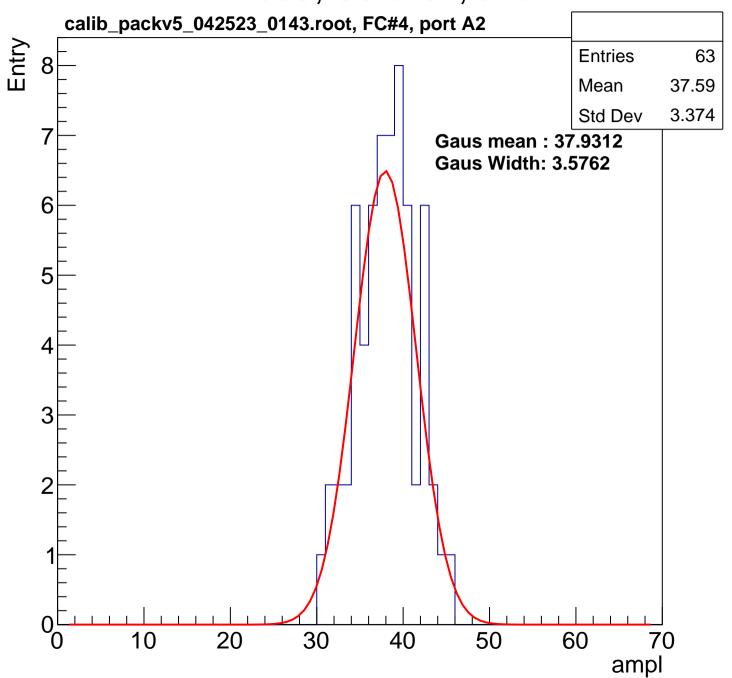


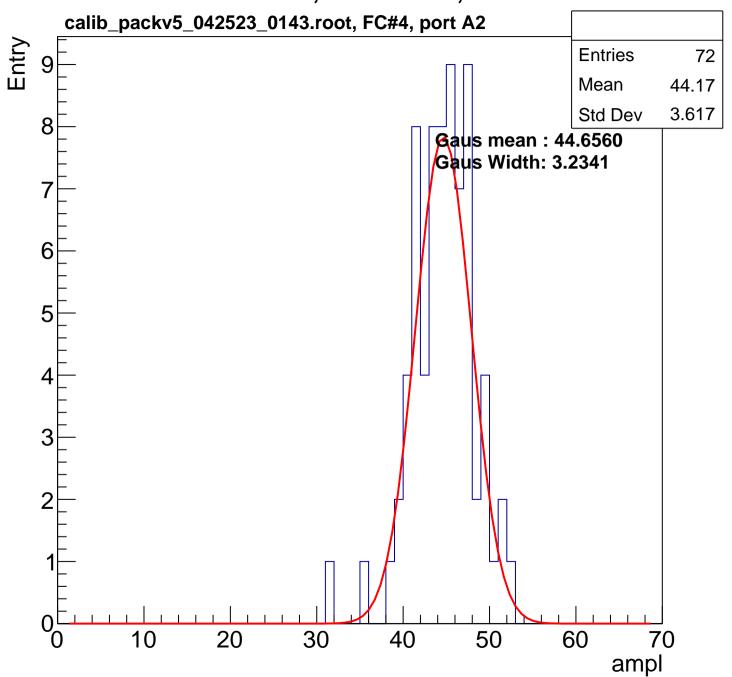


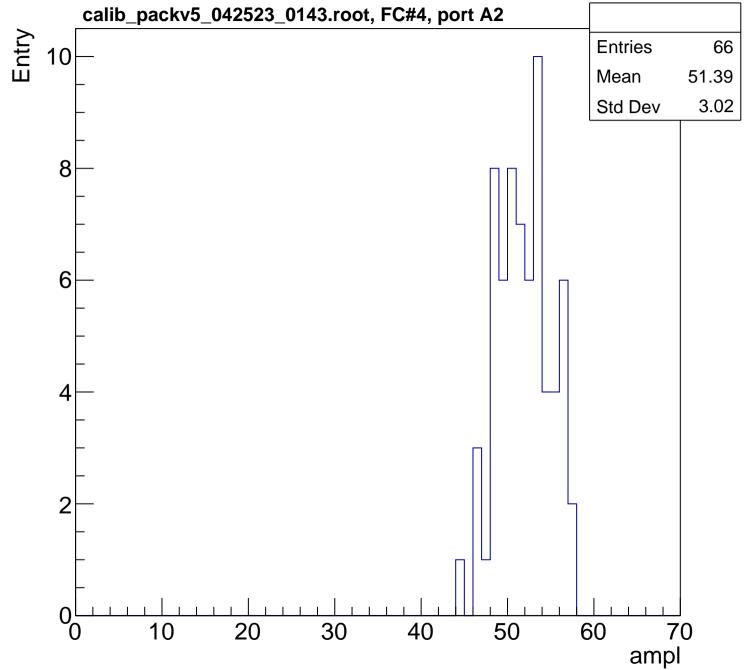


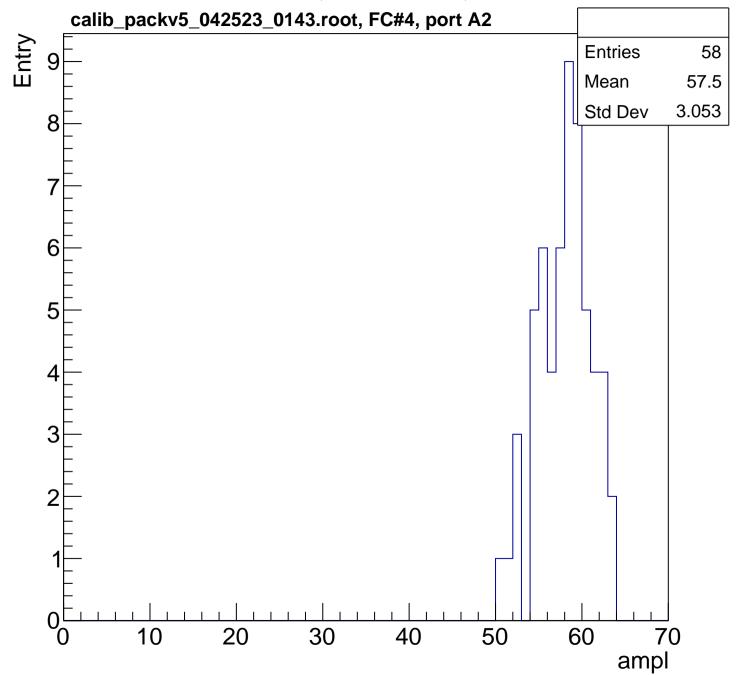


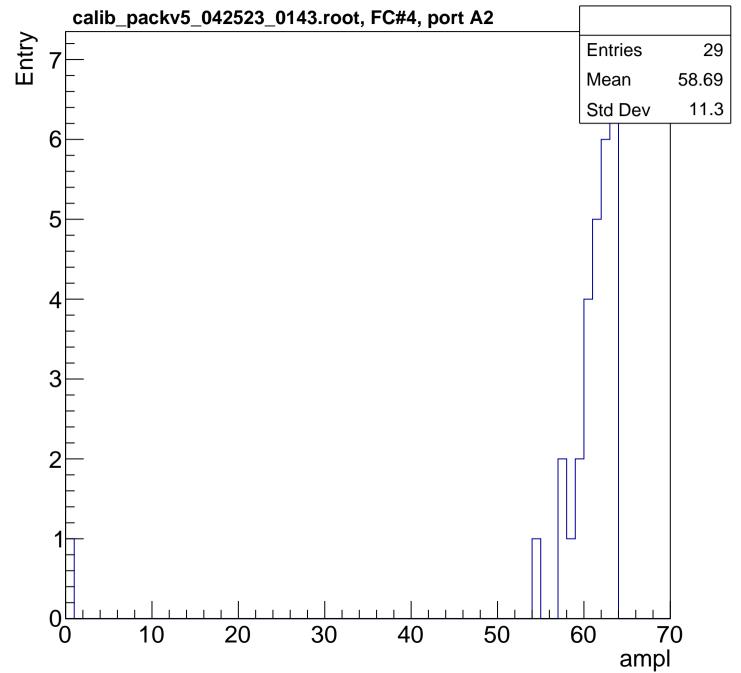


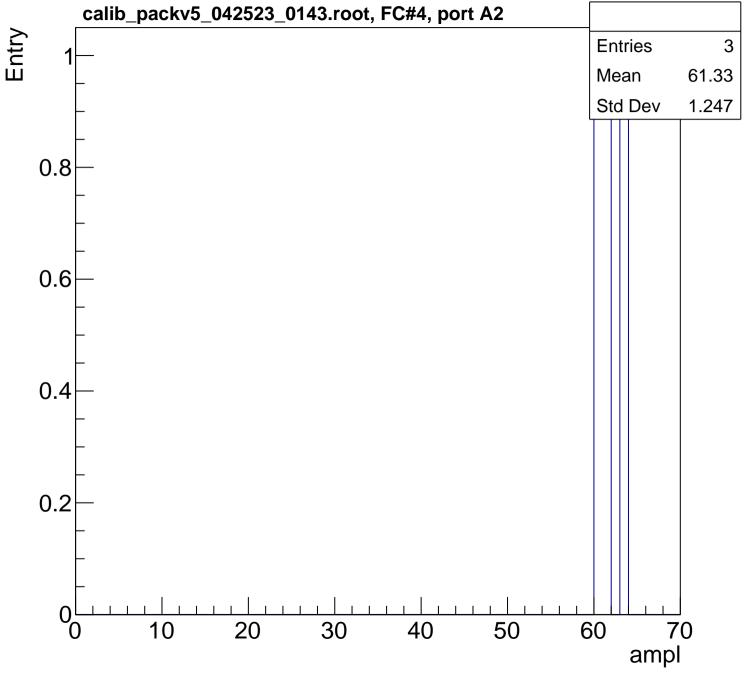


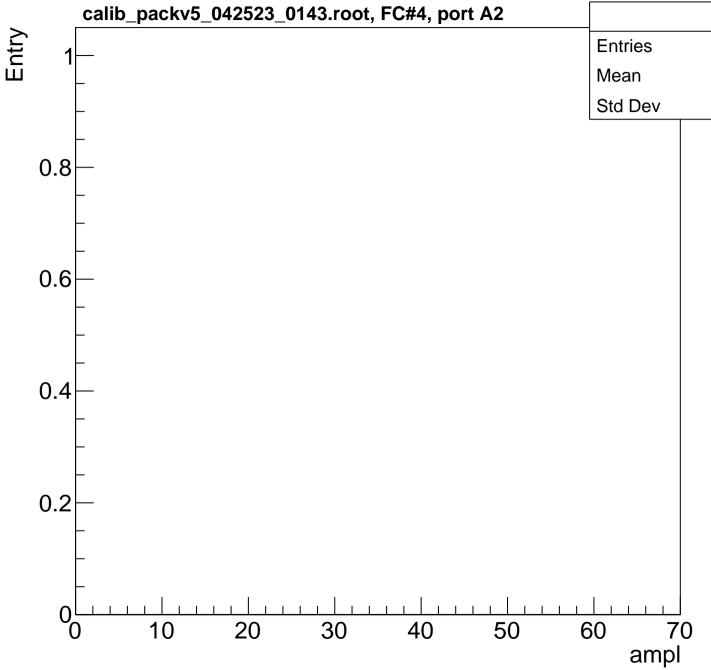


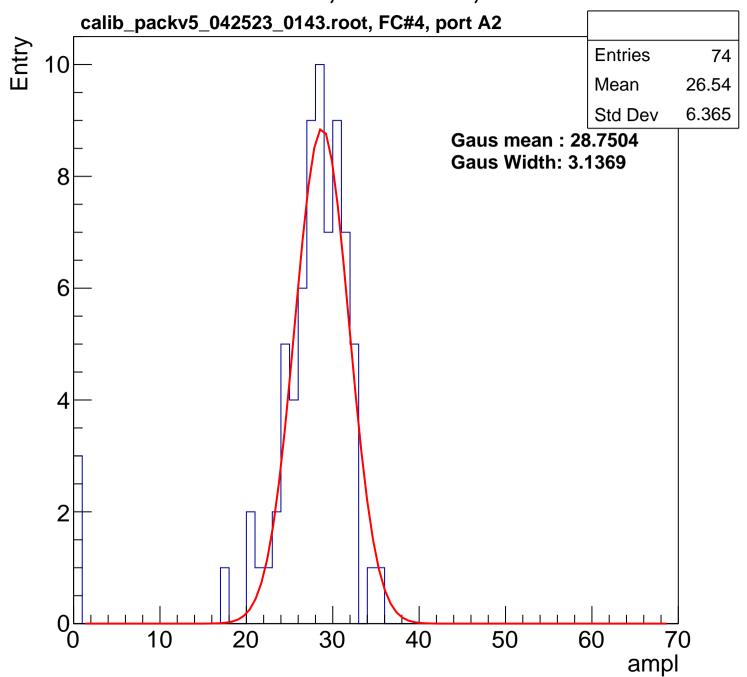


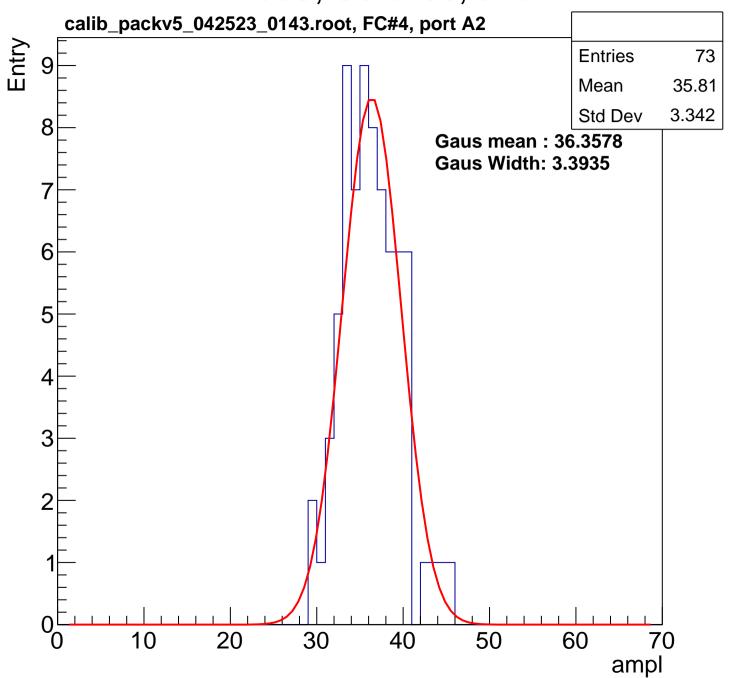


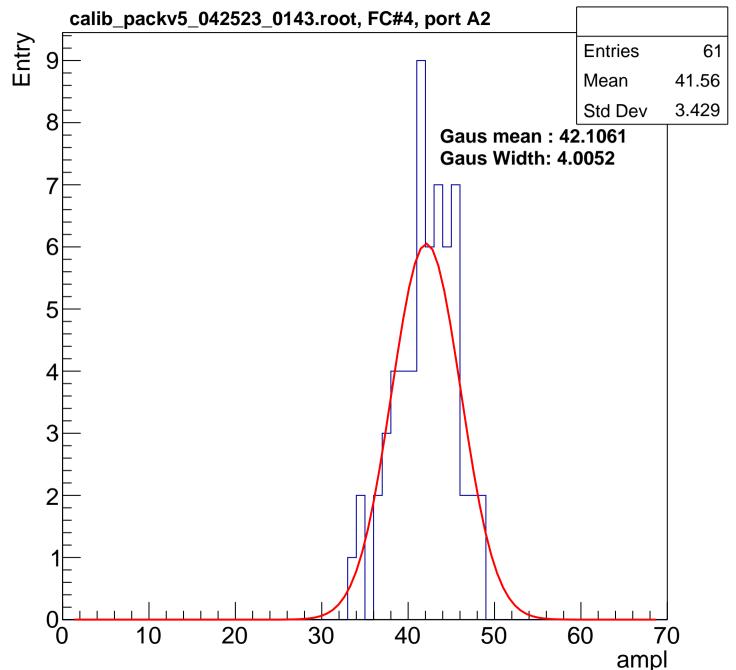


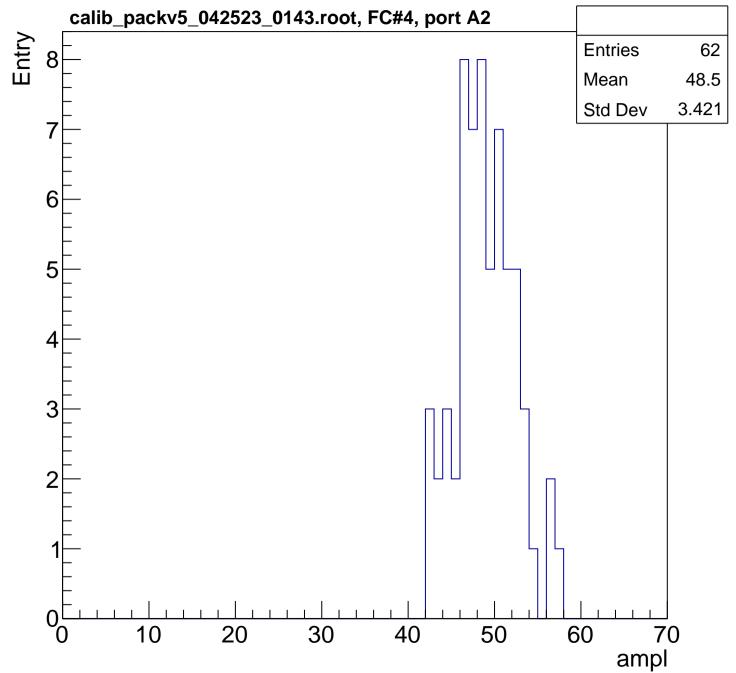


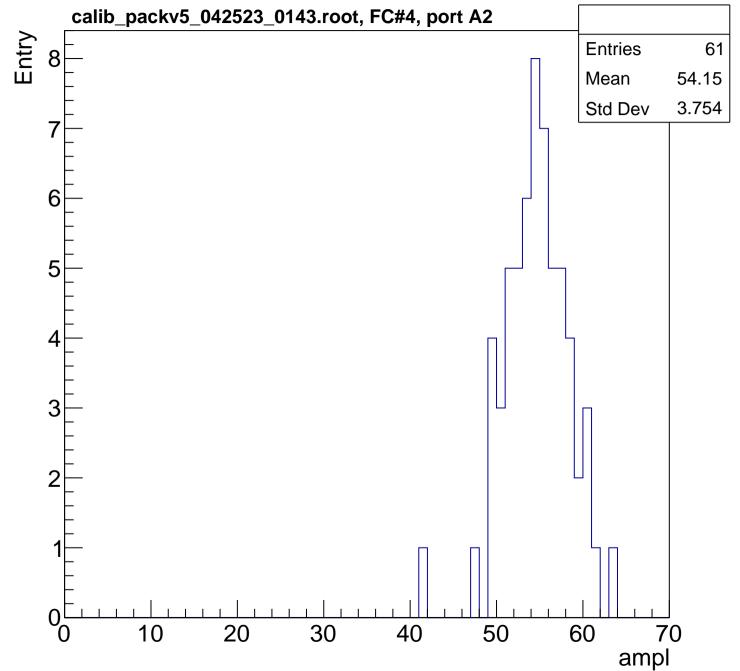


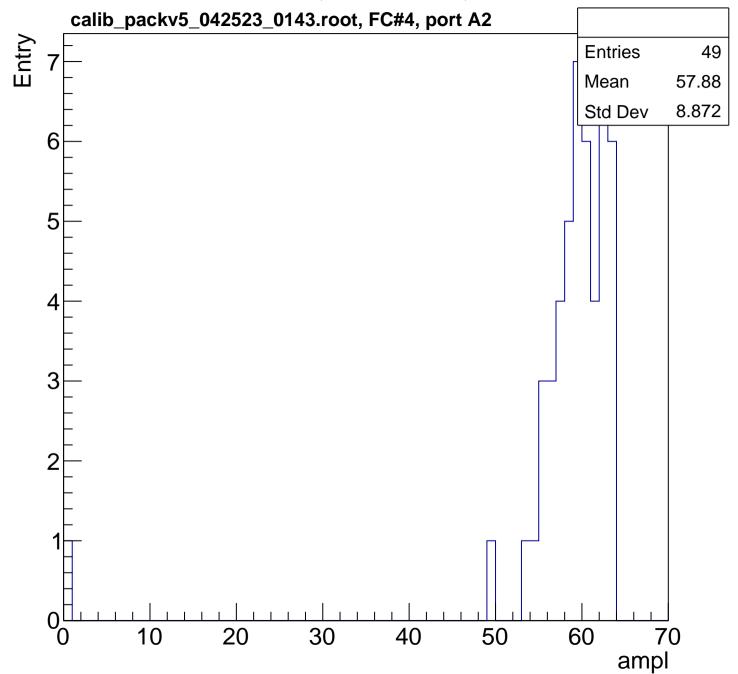


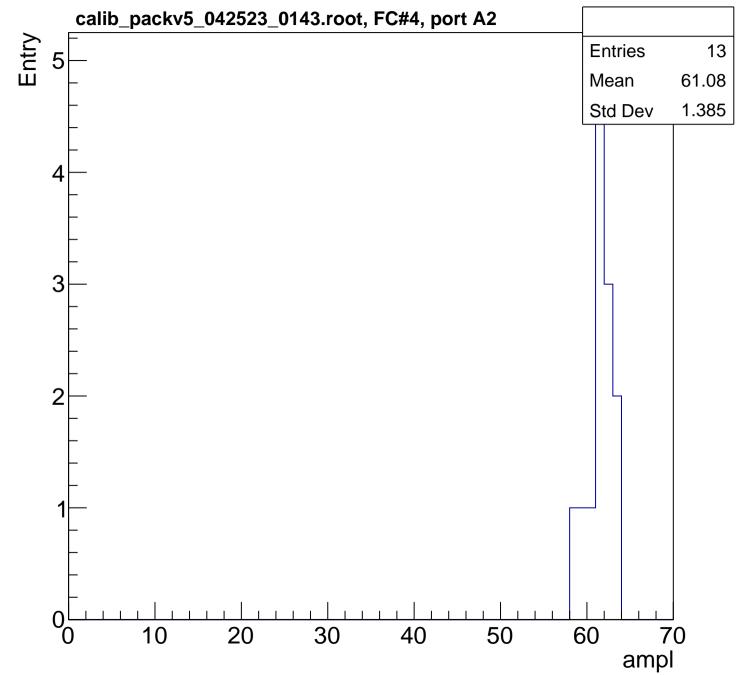


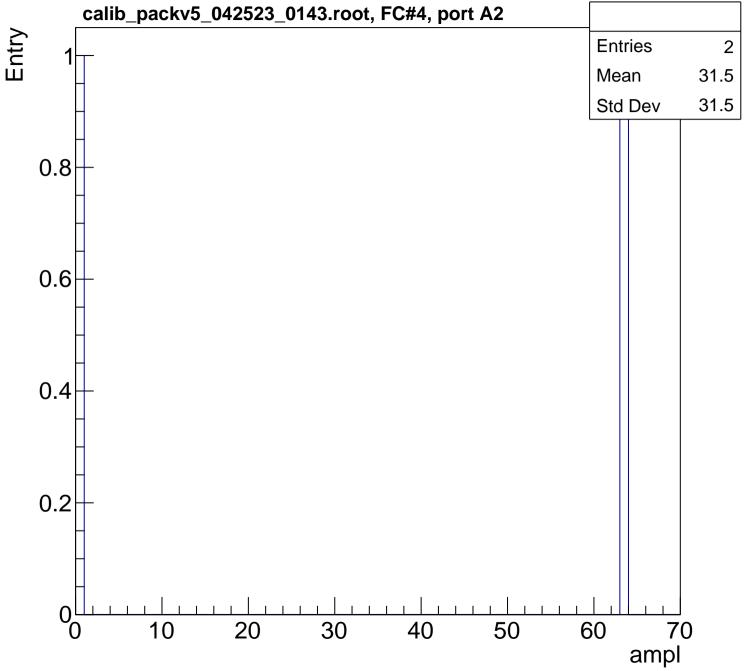


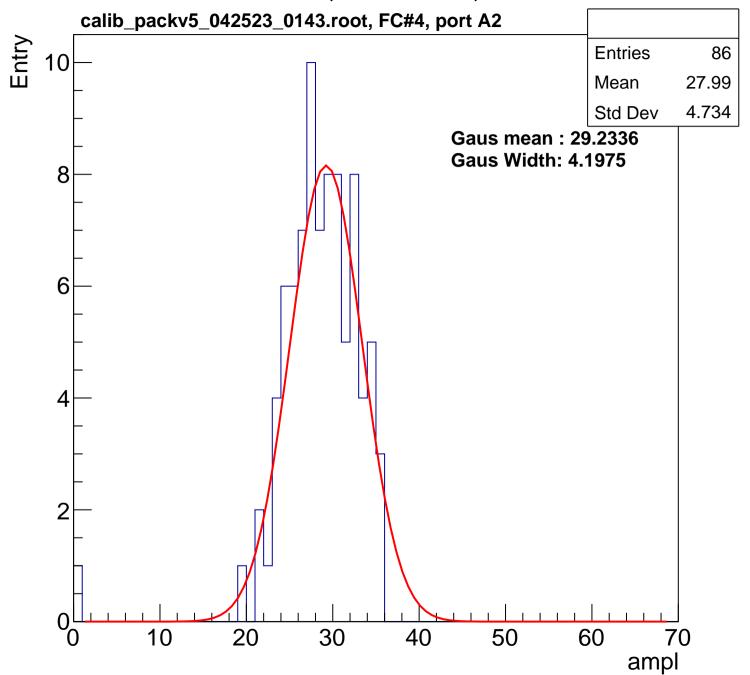


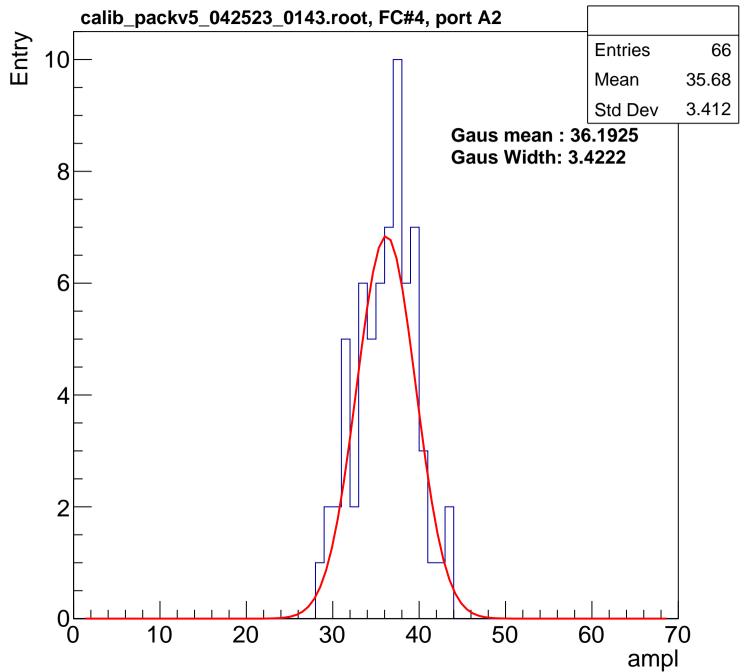


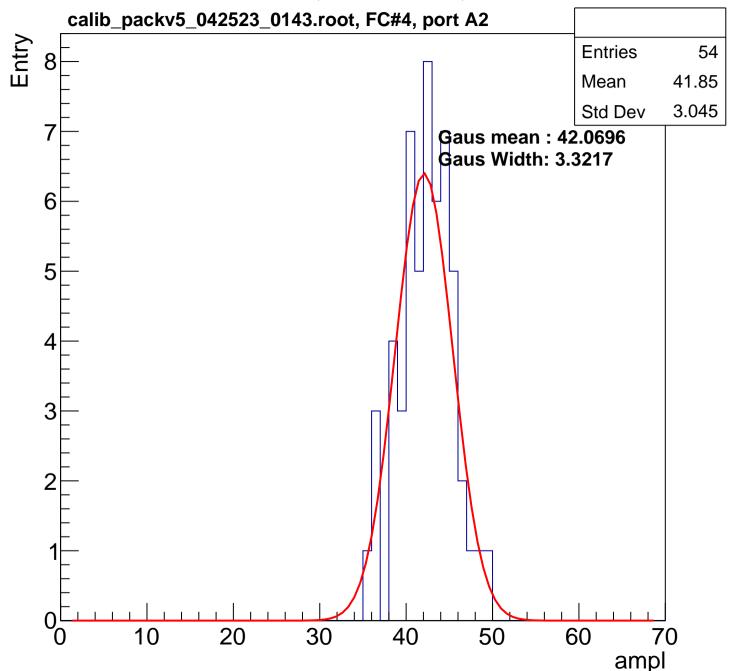


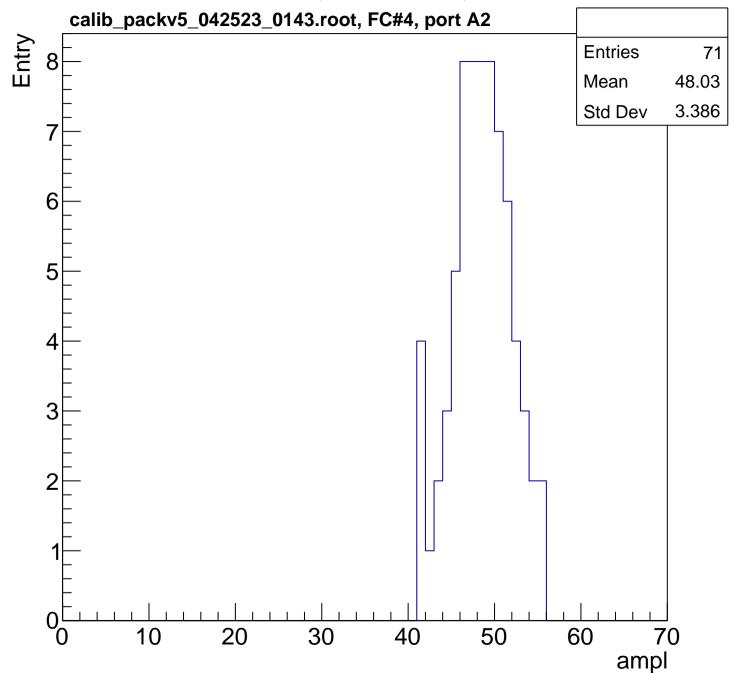


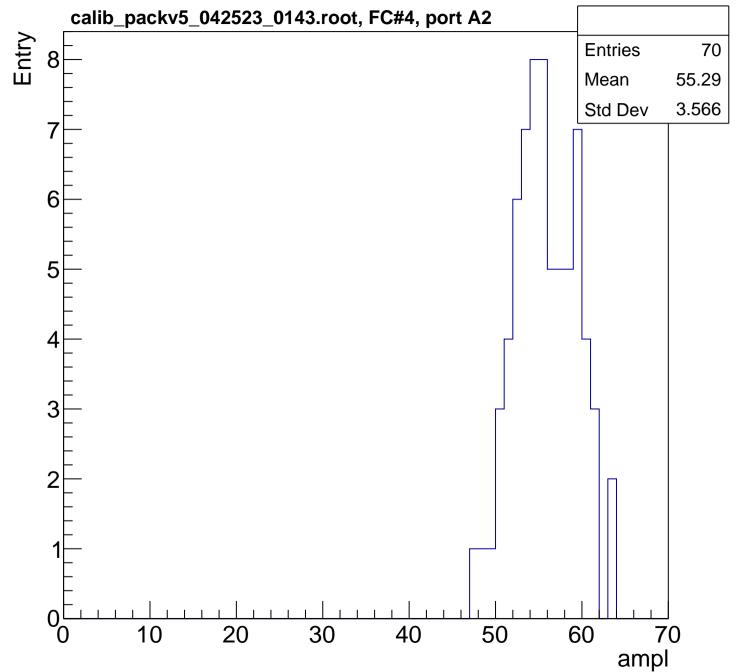


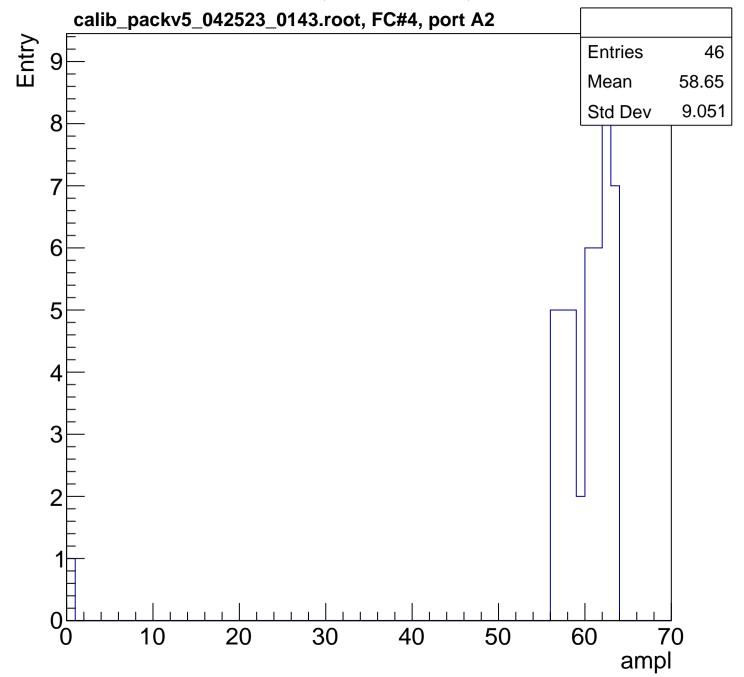


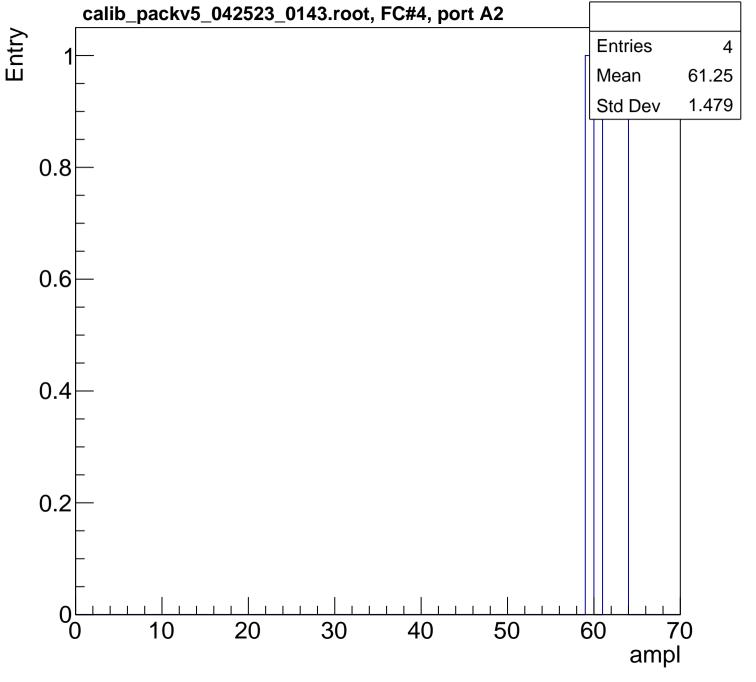


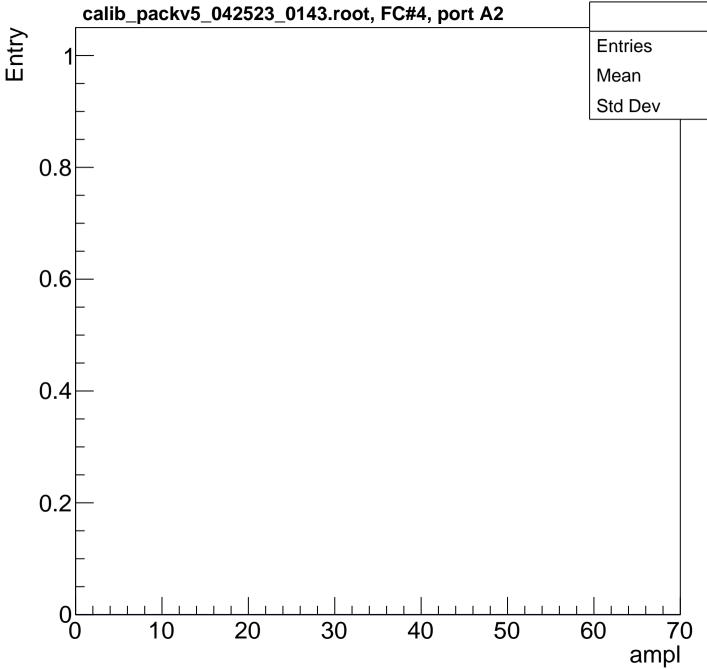


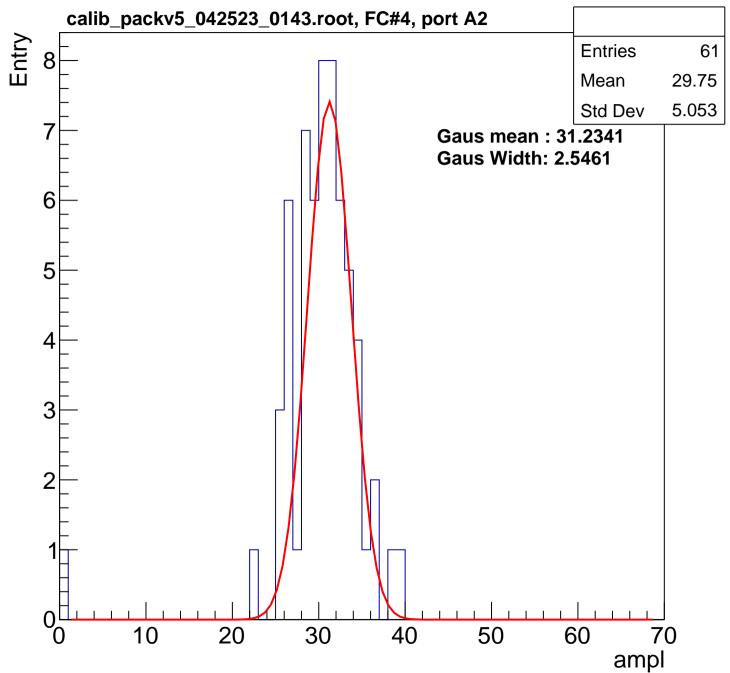


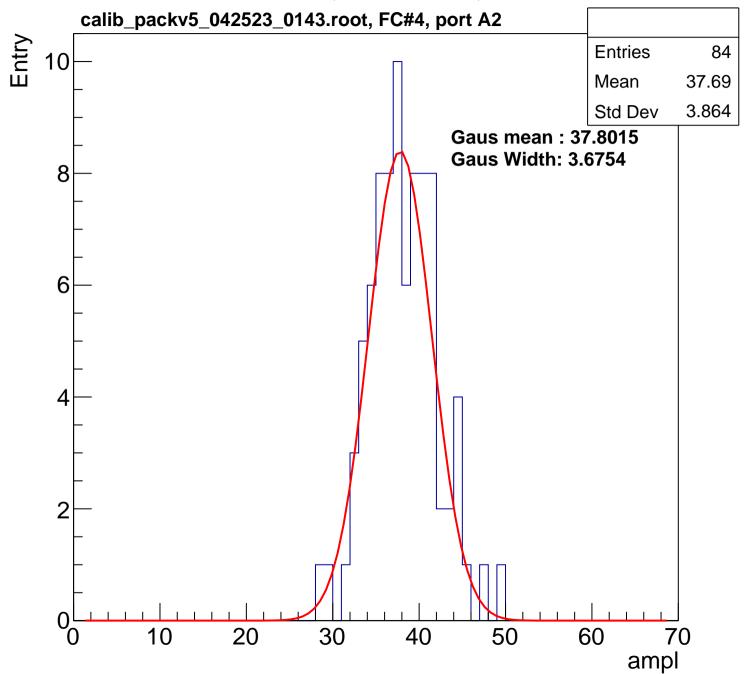


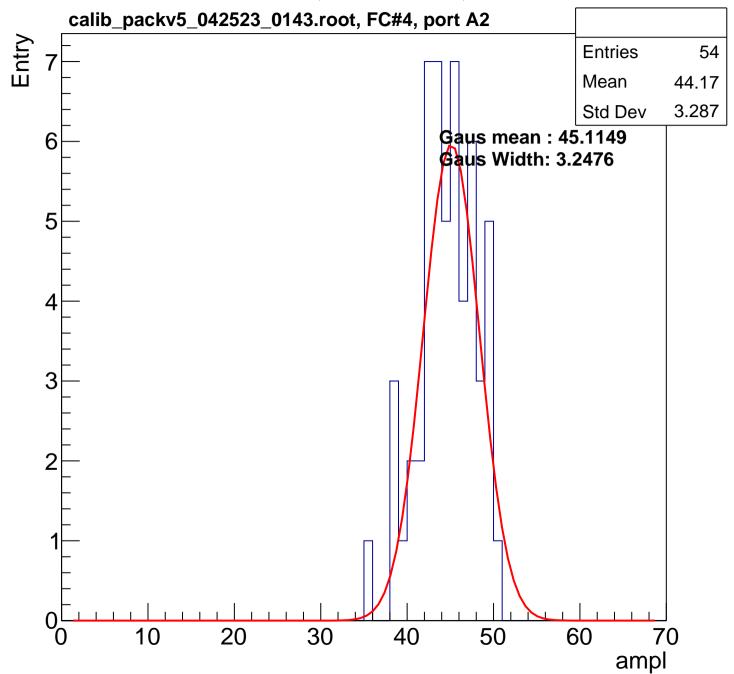


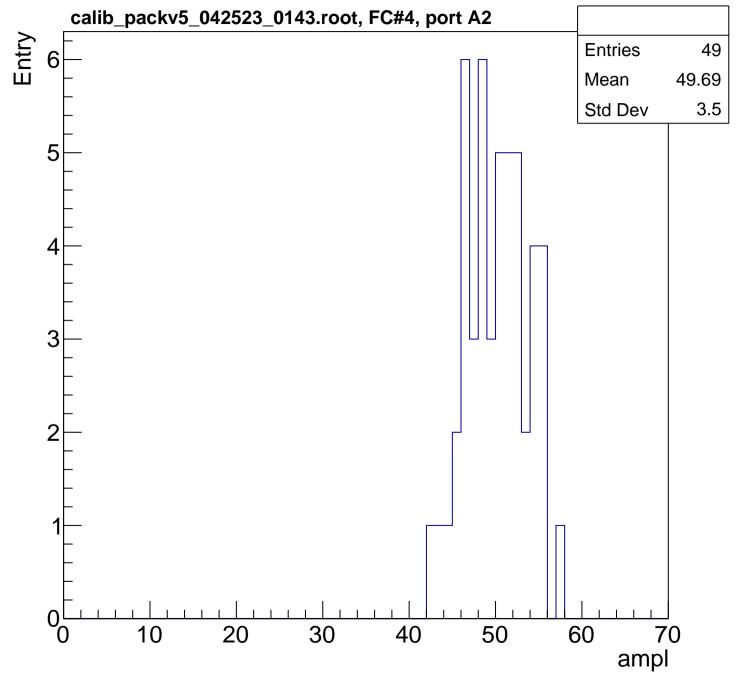


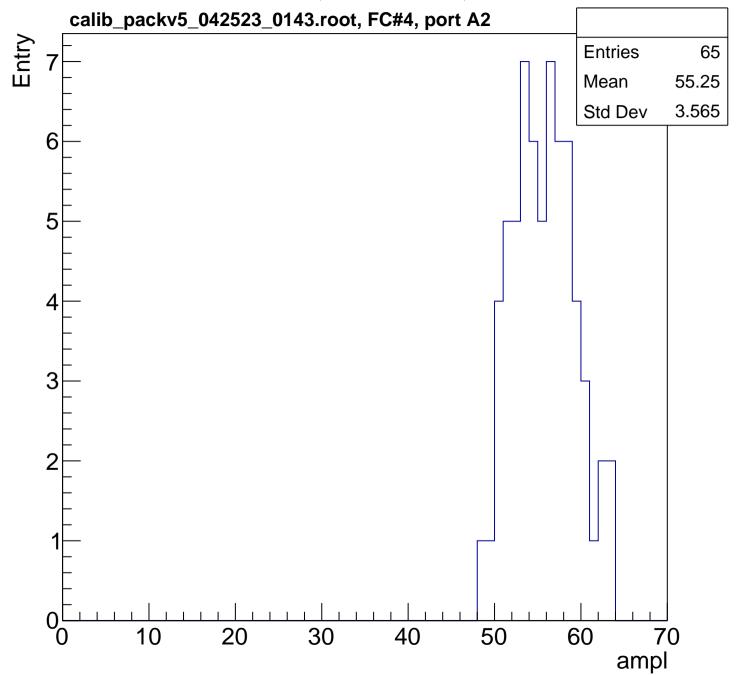


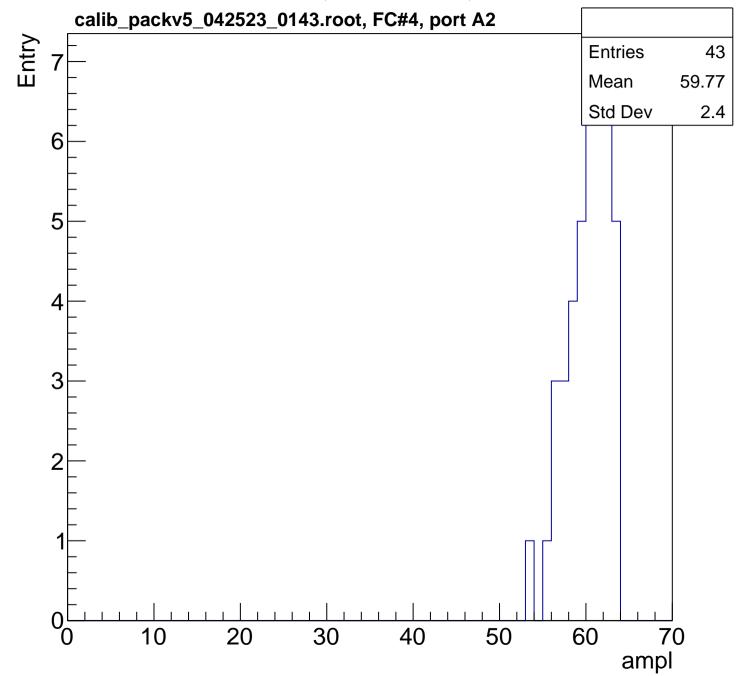


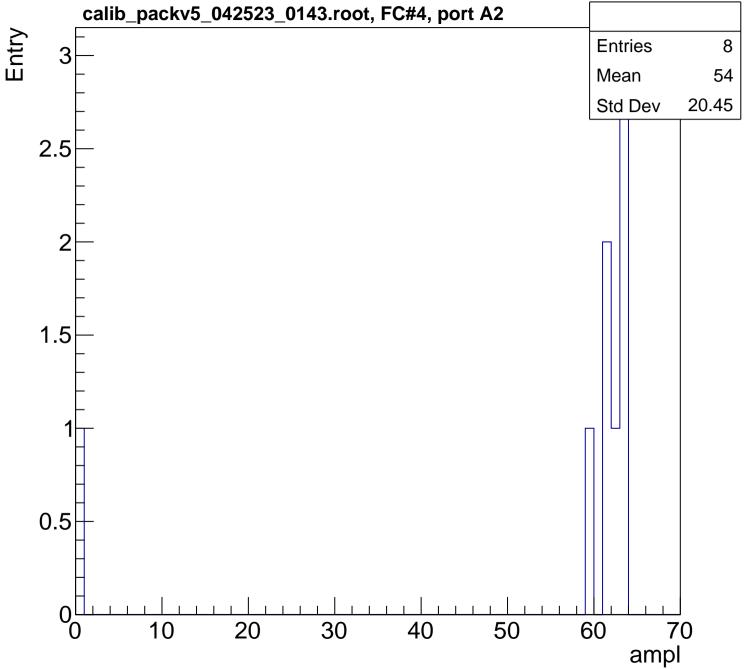


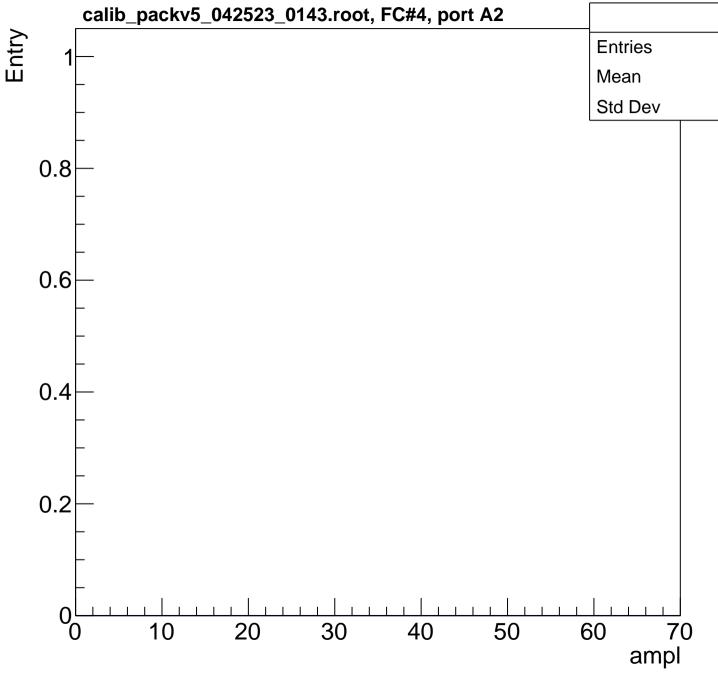


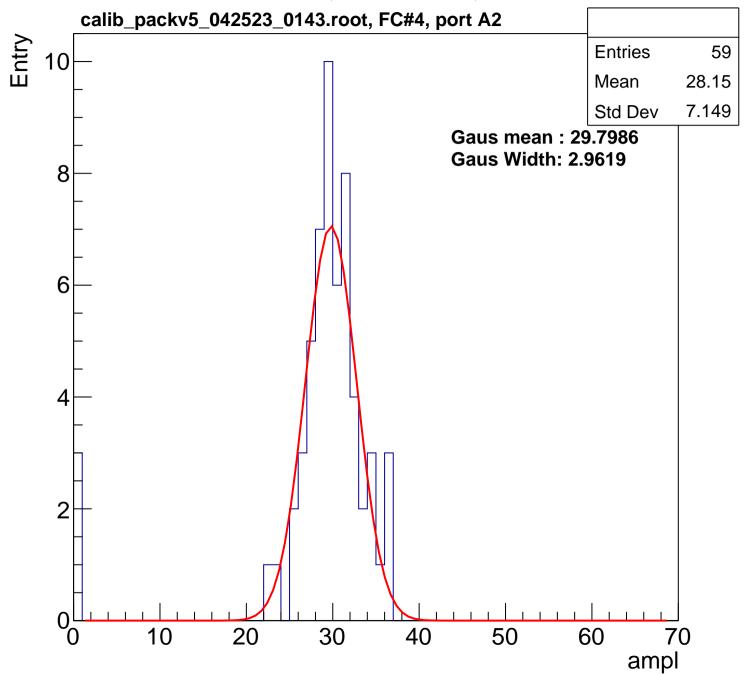


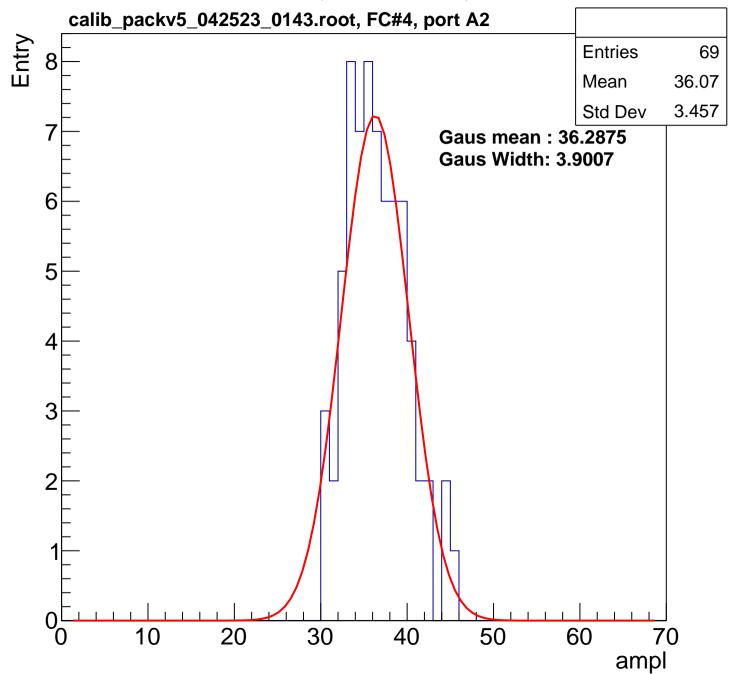


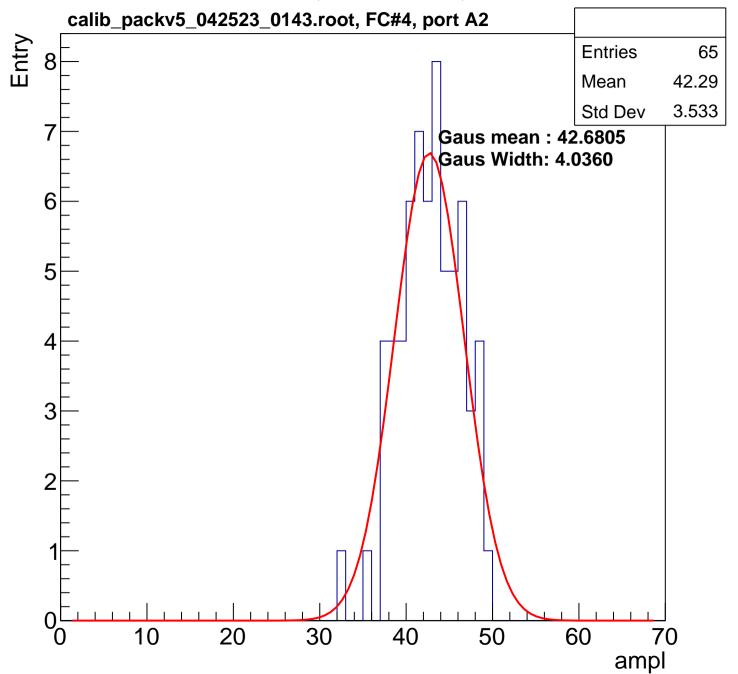


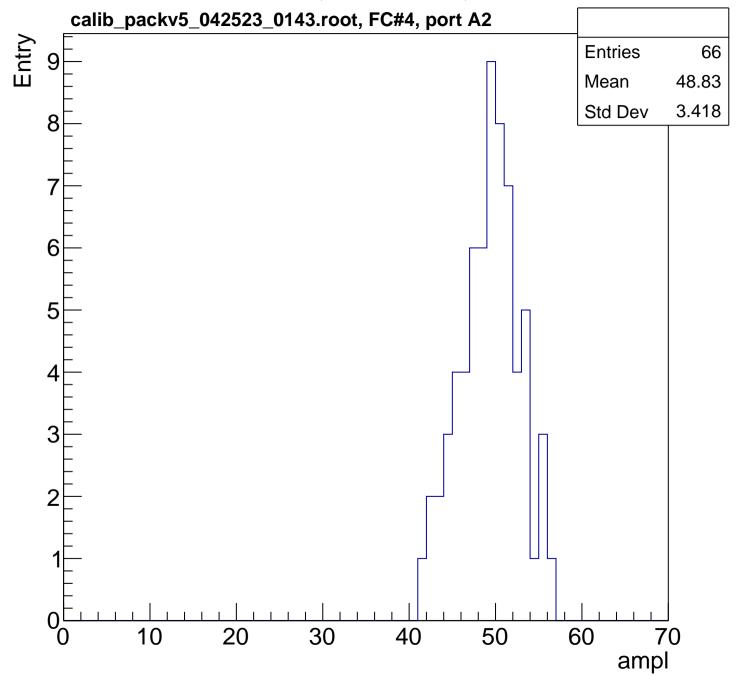


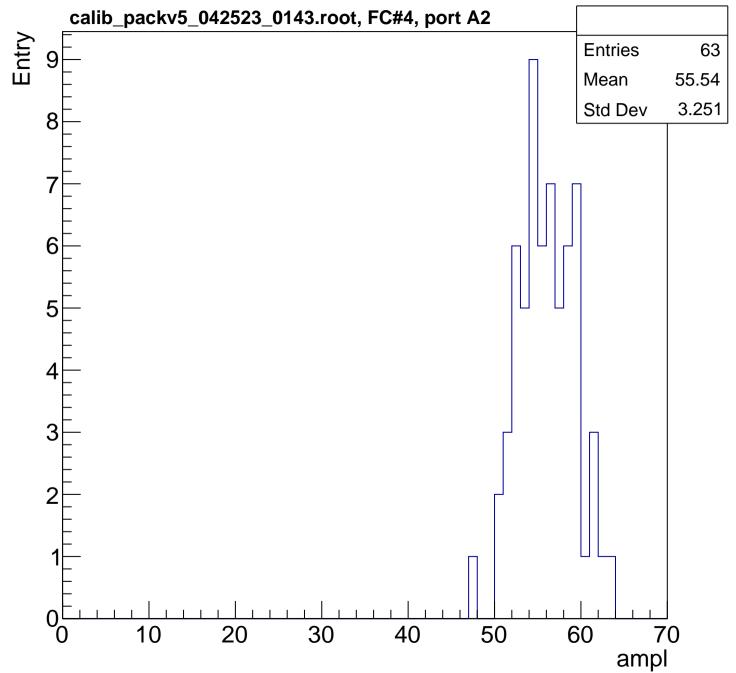


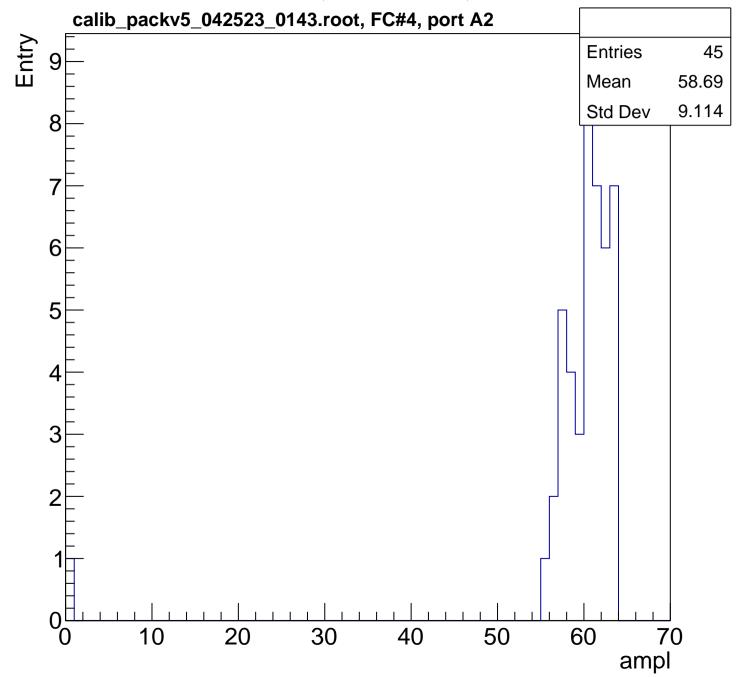


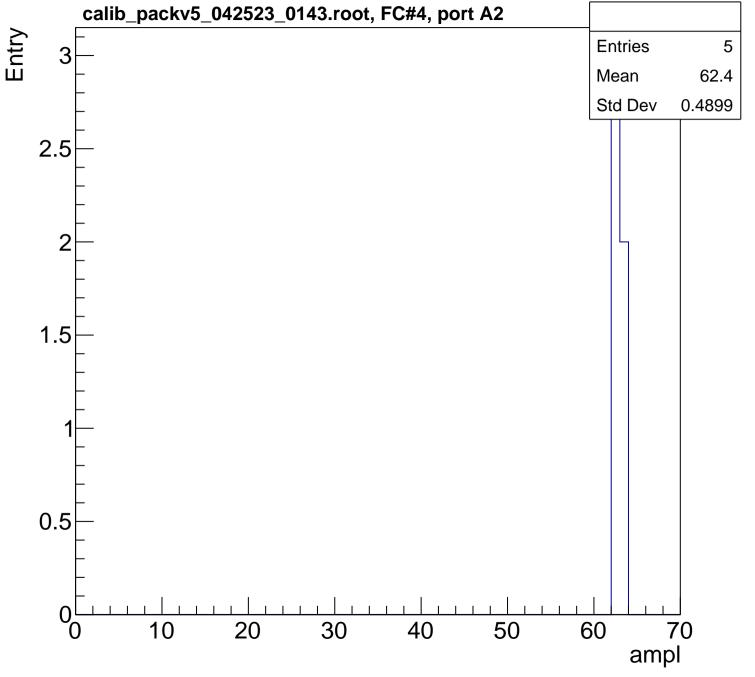












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