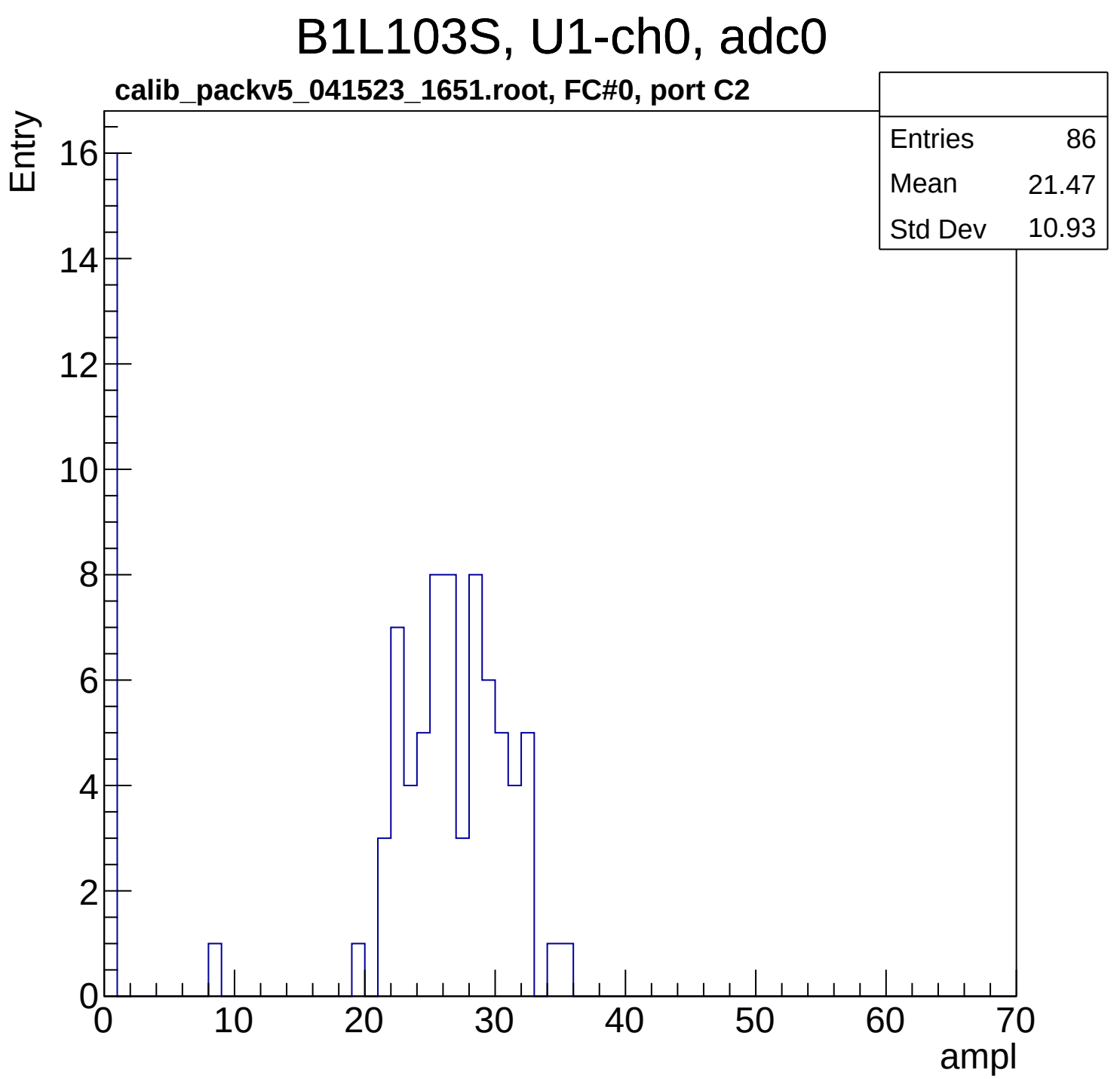
B1L103S, U1-ch0, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 21.47
Std Dev 10.93
Entry
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6
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16
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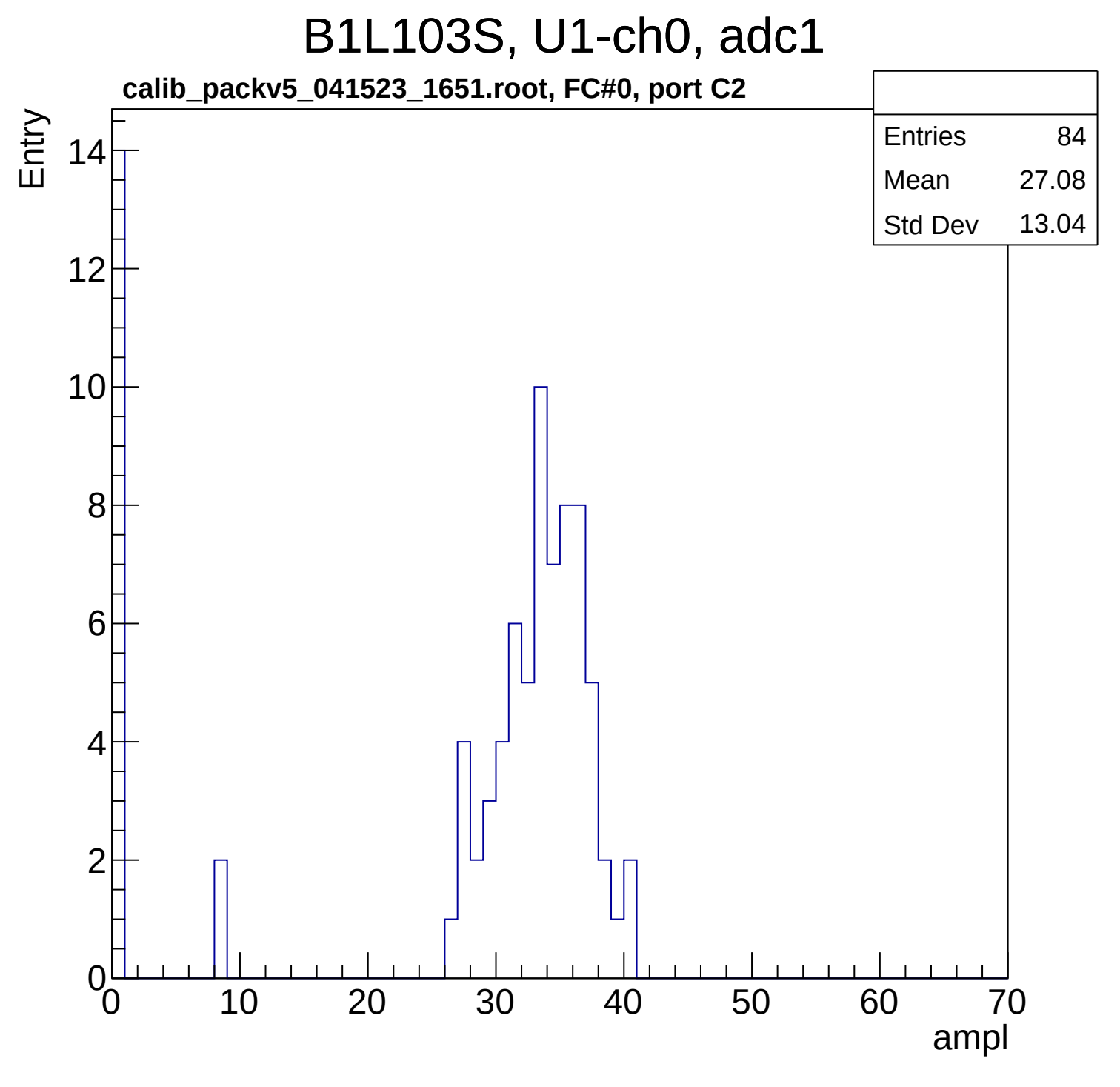
70
ampl


B1L103S, U1-ch0, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 27.08
Std Dev 13.04
Entry
ampl
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4
6
8
10
12
14
0
10
20
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40
50
60
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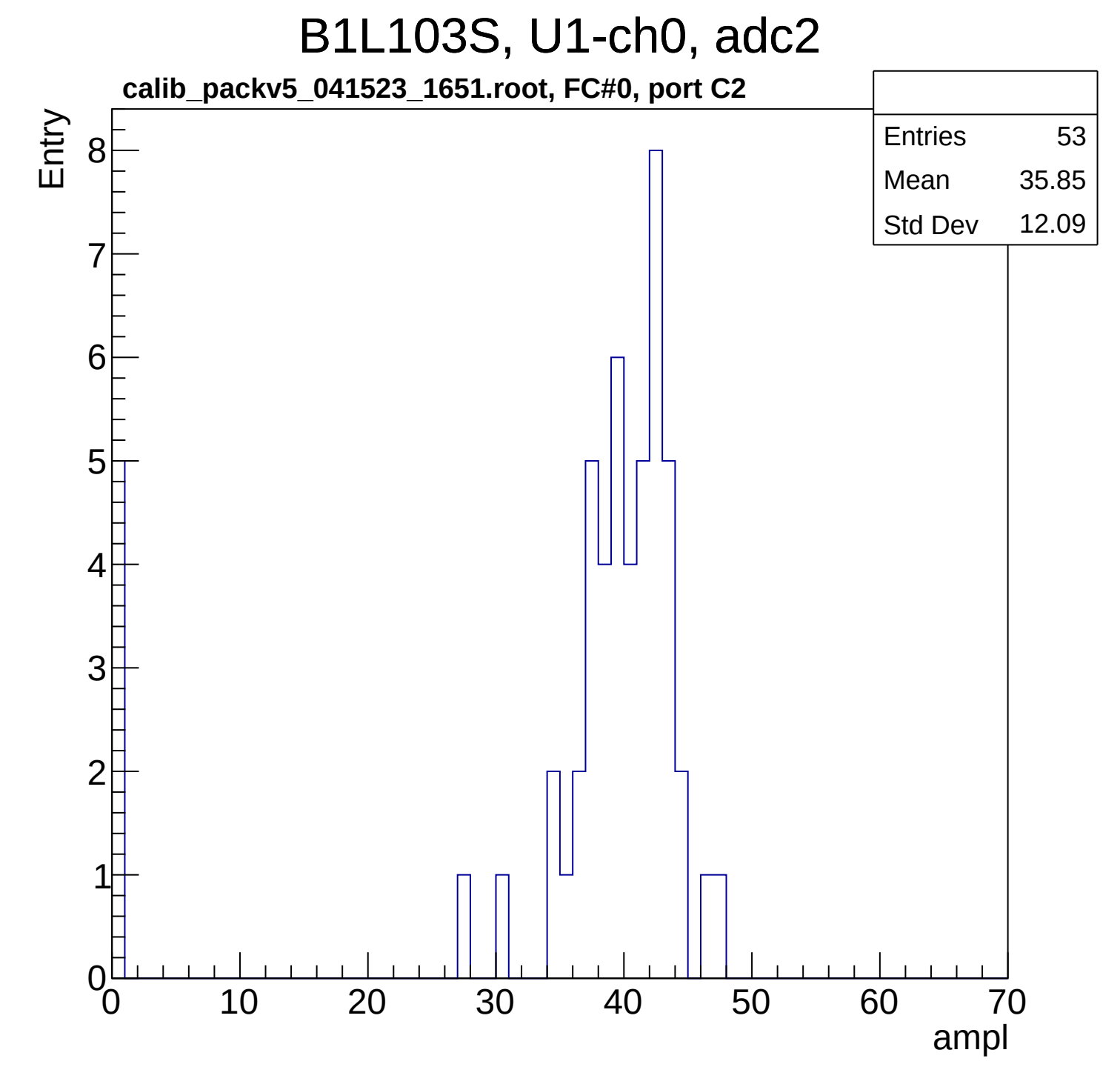
B1L103S, U1-ch0, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 35.85
Std Dev 12.09
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
30
40
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60
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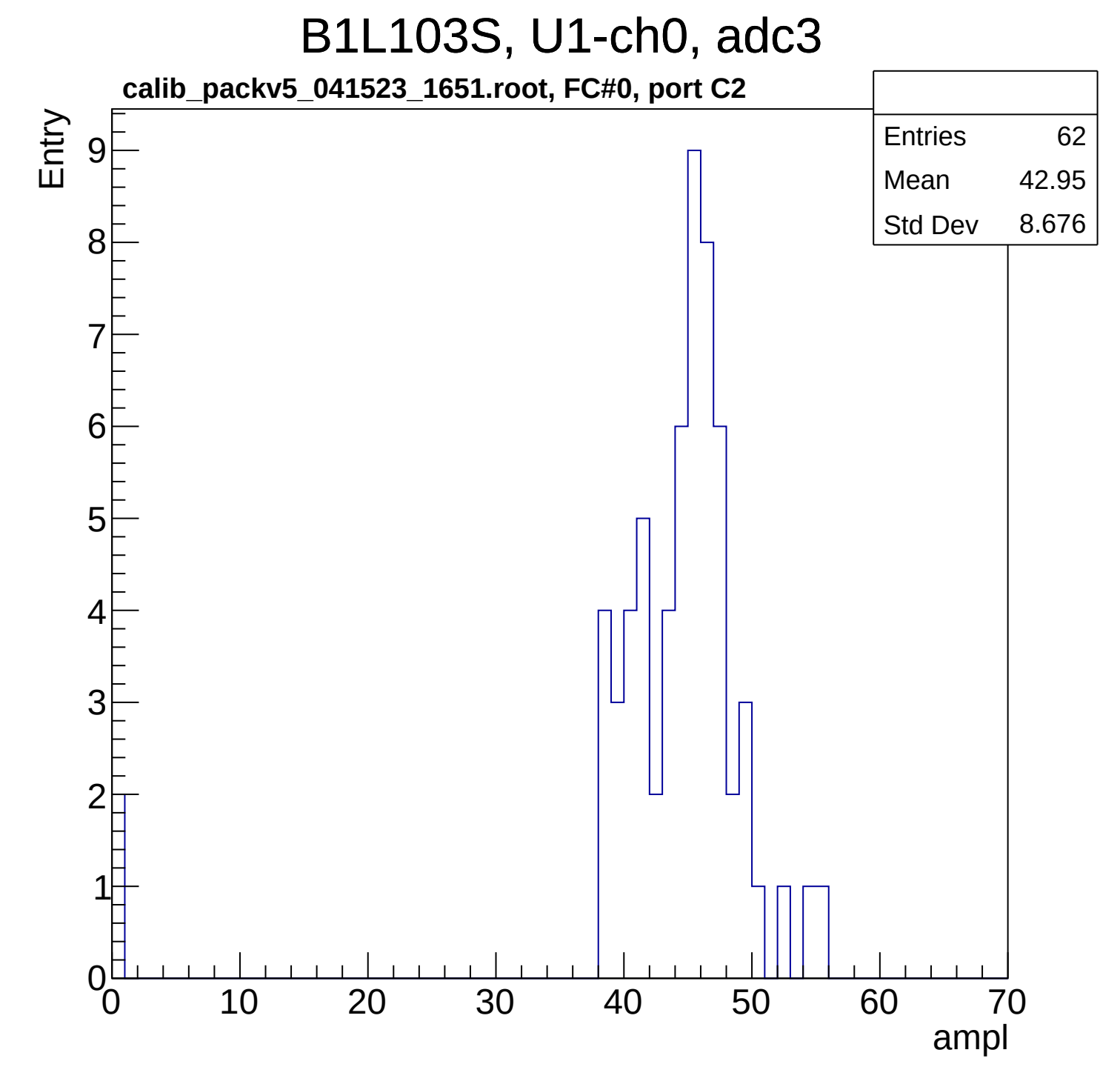
B1L103S, U1-ch0, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 42.95
Std Dev 8.676
Entry
ampl
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3
4
5
6
7
8
9
0
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60
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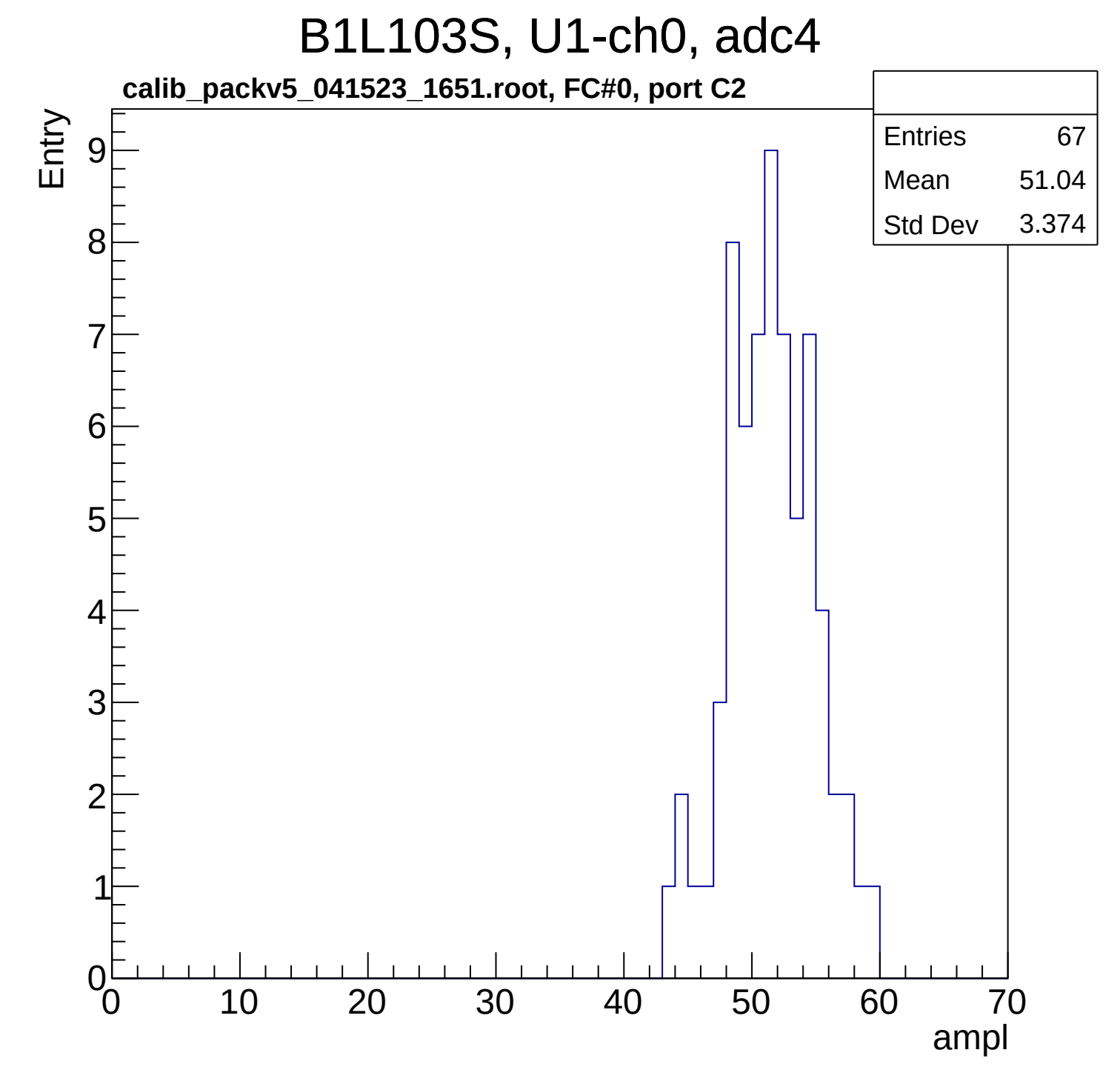
B1L103S, U1-ch0, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 51.04
Std Dev 3.374
Entry
ampl
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3
4
5
6
7
8
9
0
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40
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60
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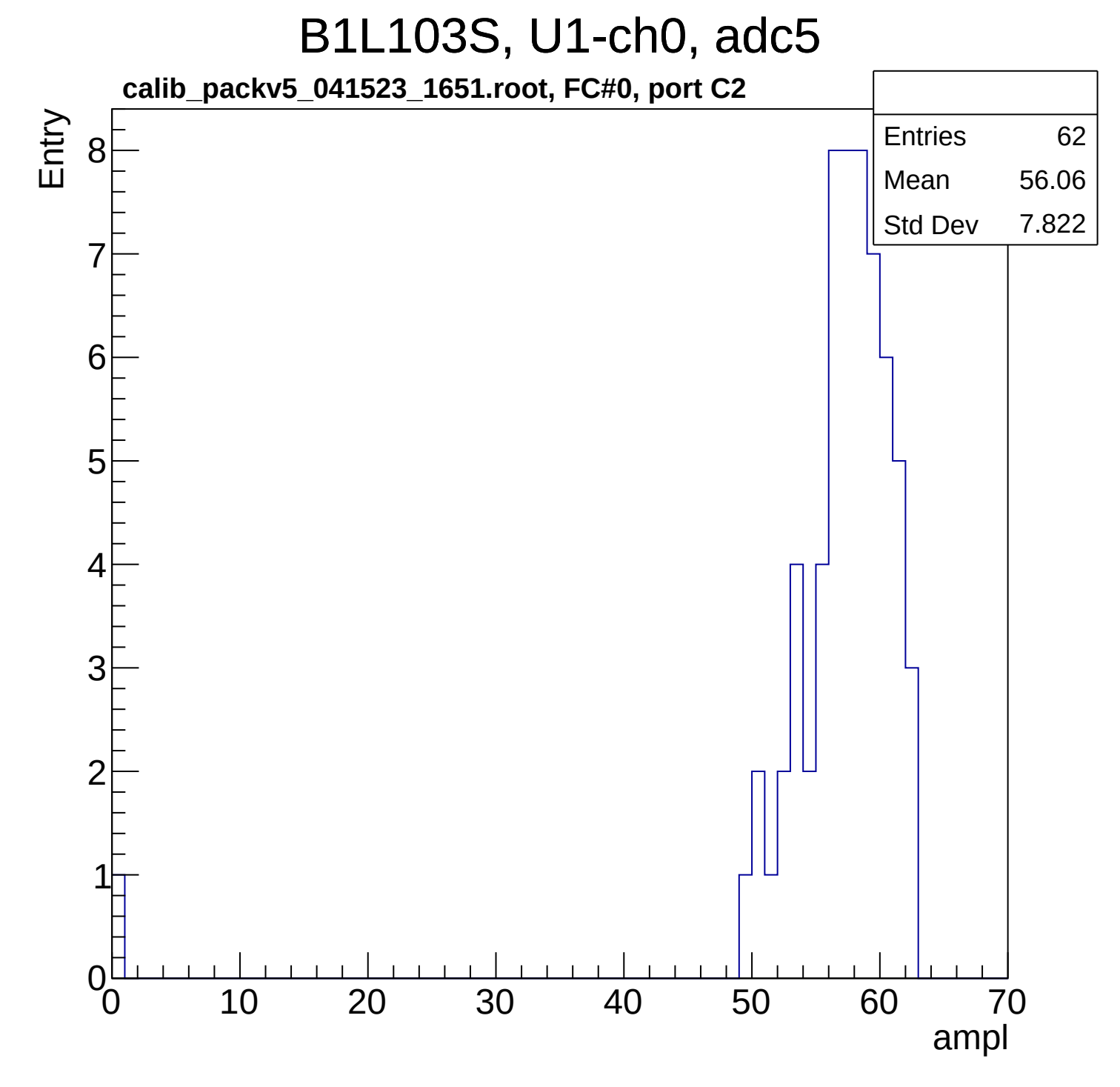
B1L103S, U1-ch0, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 56.06
Std Dev 7.822
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
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40
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60
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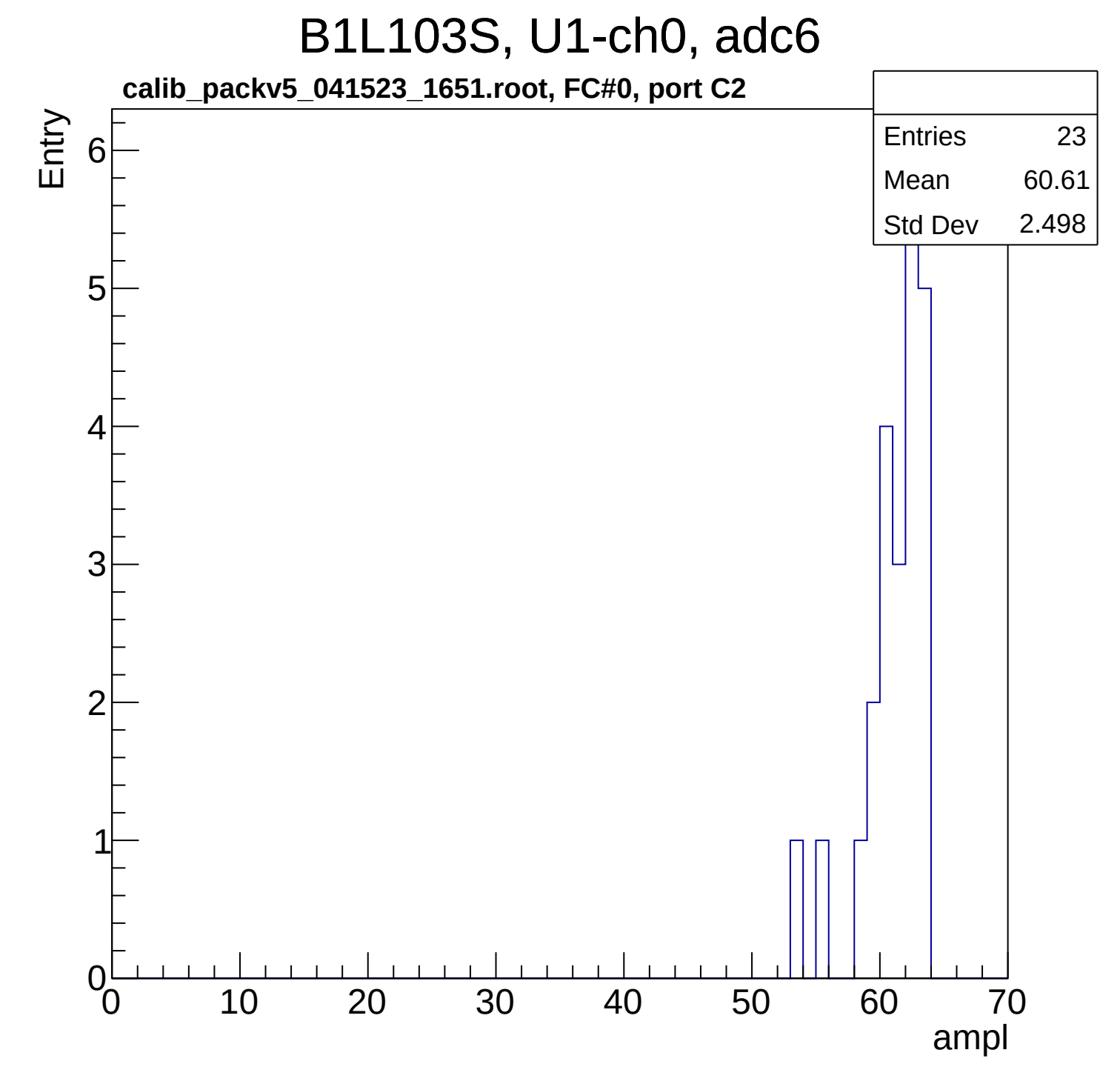
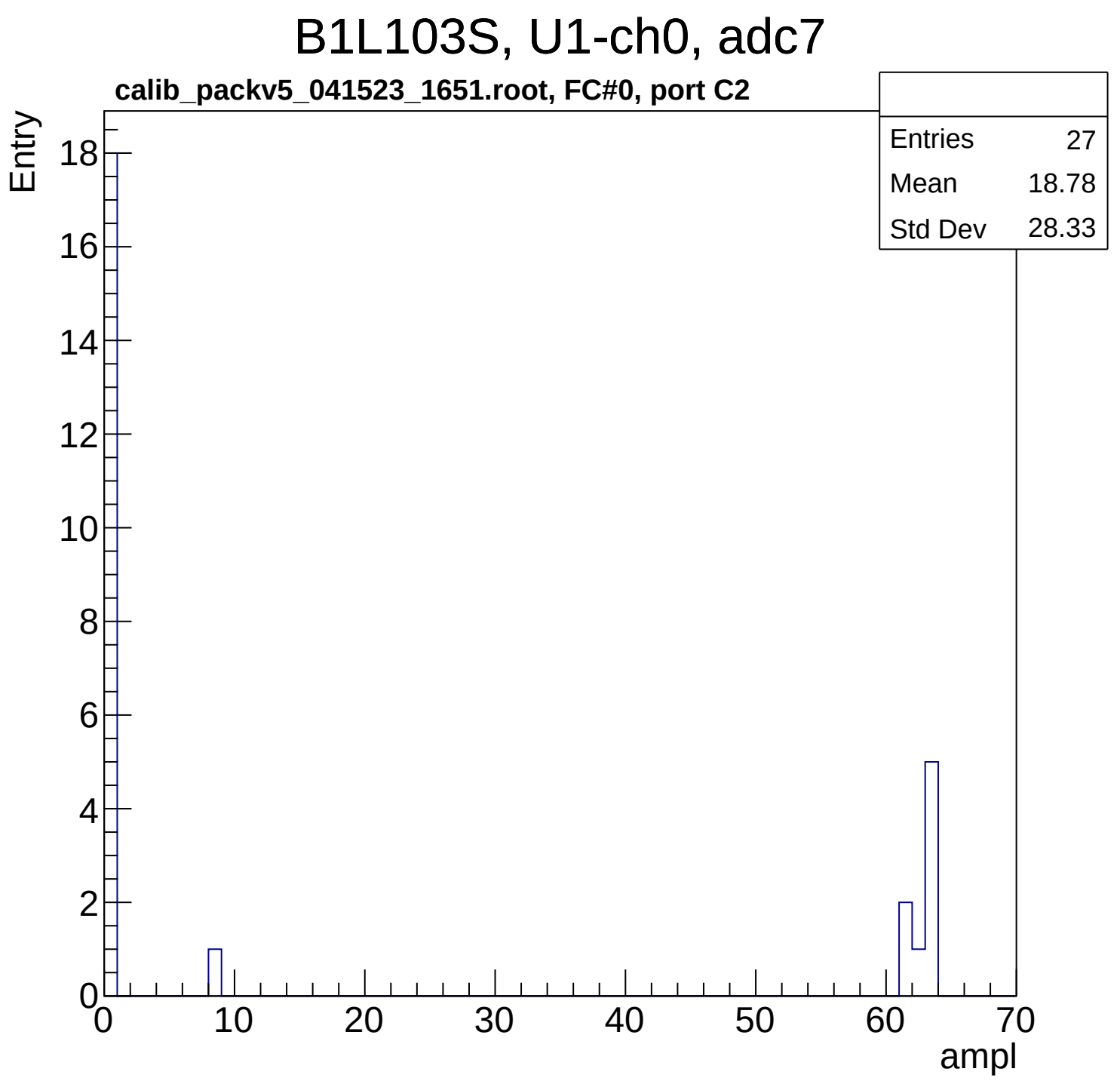

B1L103S, U1-ch0, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 23
Mean 60.61
Std Dev 2.498
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U1-ch0, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 27
Mean 18.78
Std Dev 28.33
Entry
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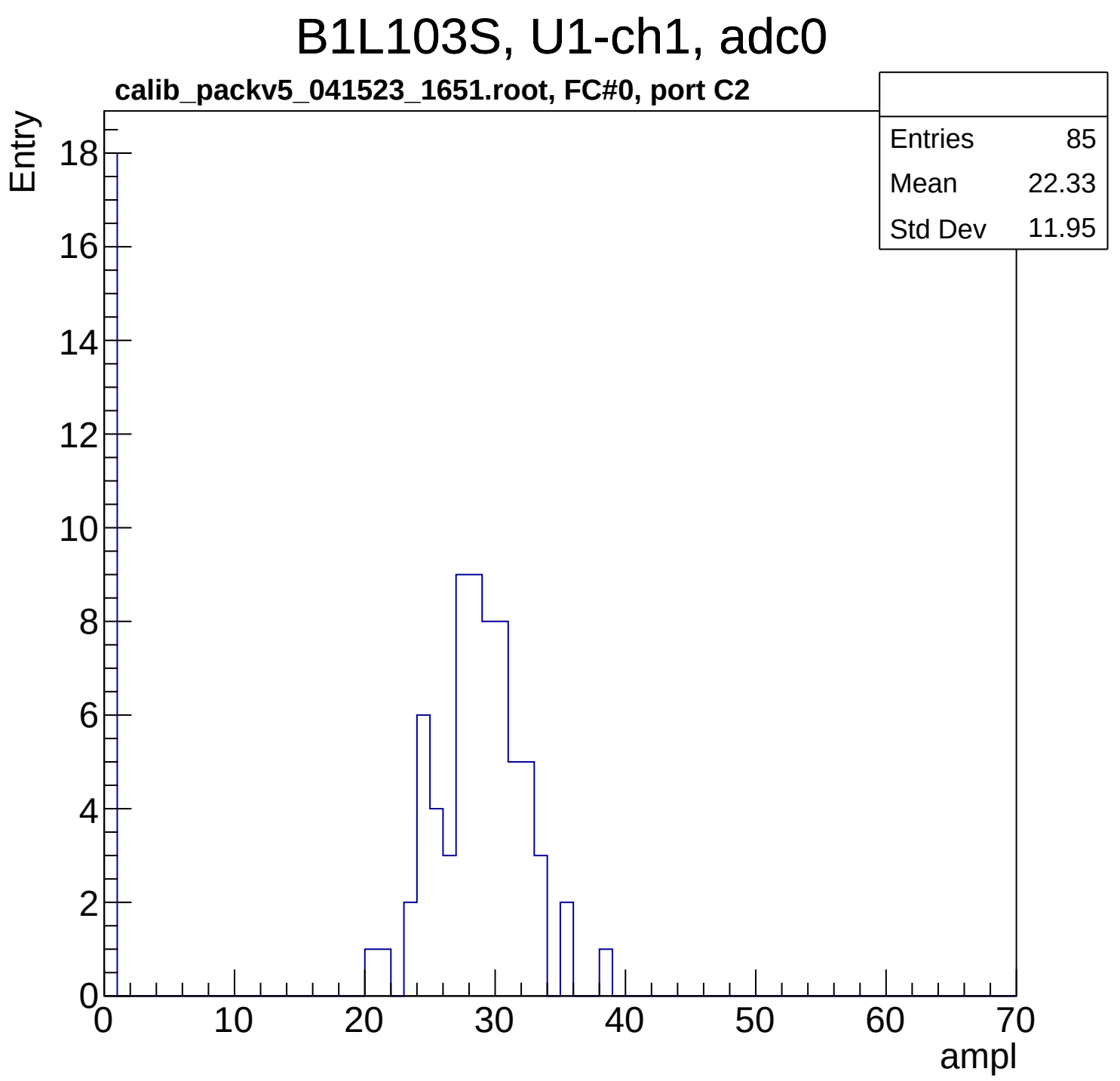
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch1, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 22.33
Std Dev 11.95
Entry
ampl
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4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
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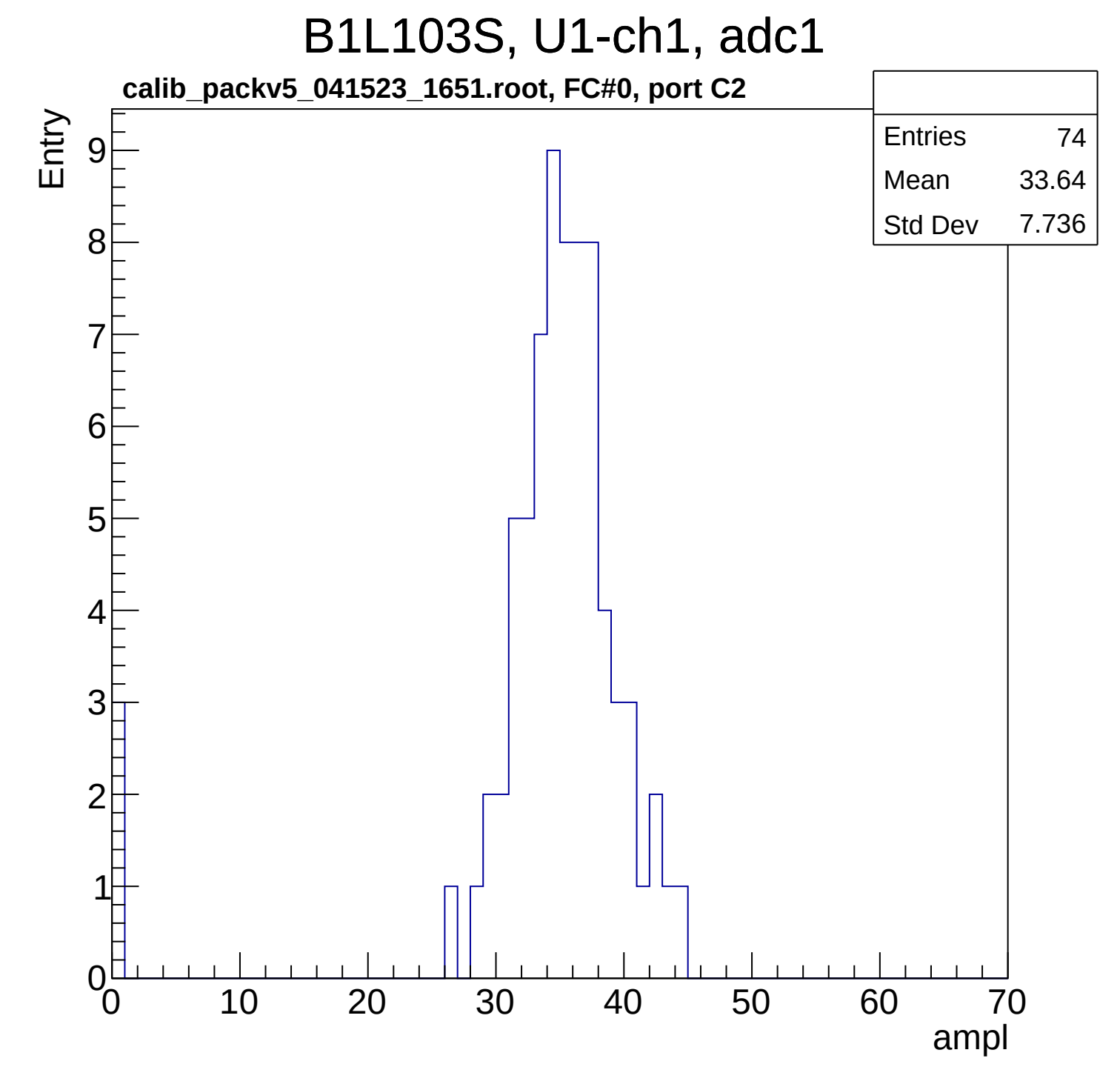
B1L103S, U1-ch1, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 33.64
Std Dev 7.736
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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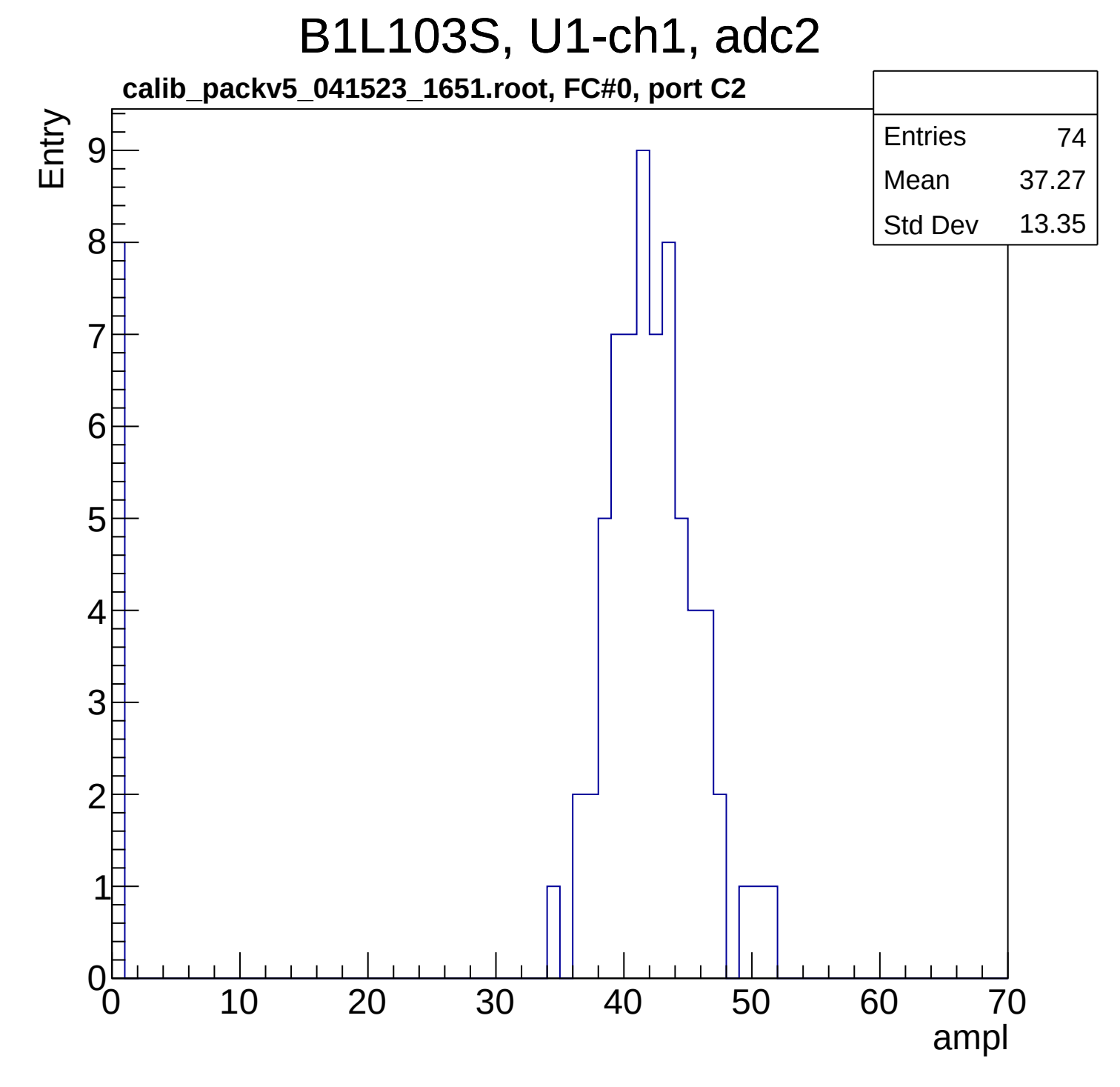
B1L103S, U1-ch1, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 37.27
Std Dev 13.35
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
30
40
50
60
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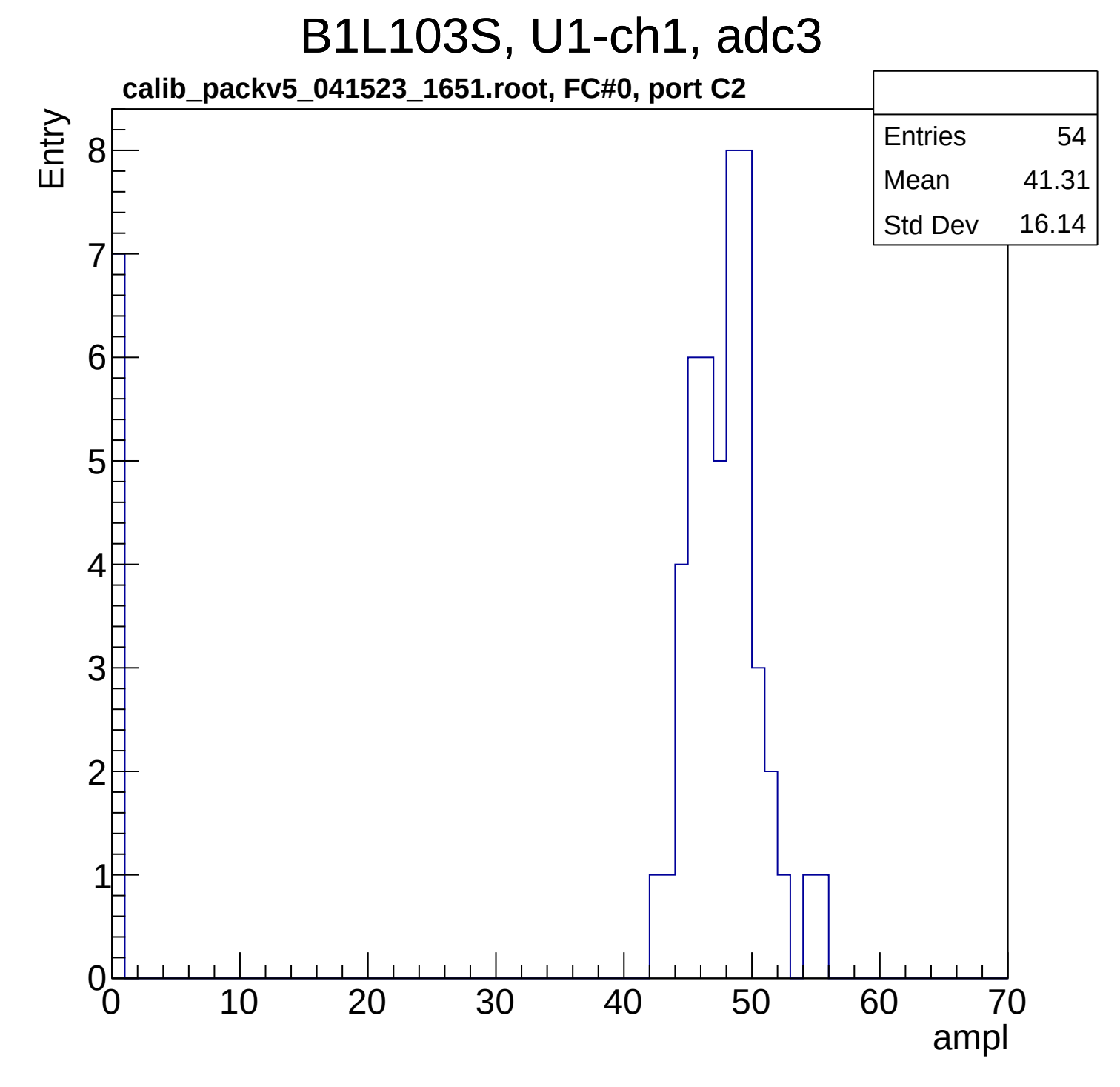
B1L103S, U1-ch1, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 41.31
Std Dev 16.14
Entry
ampl
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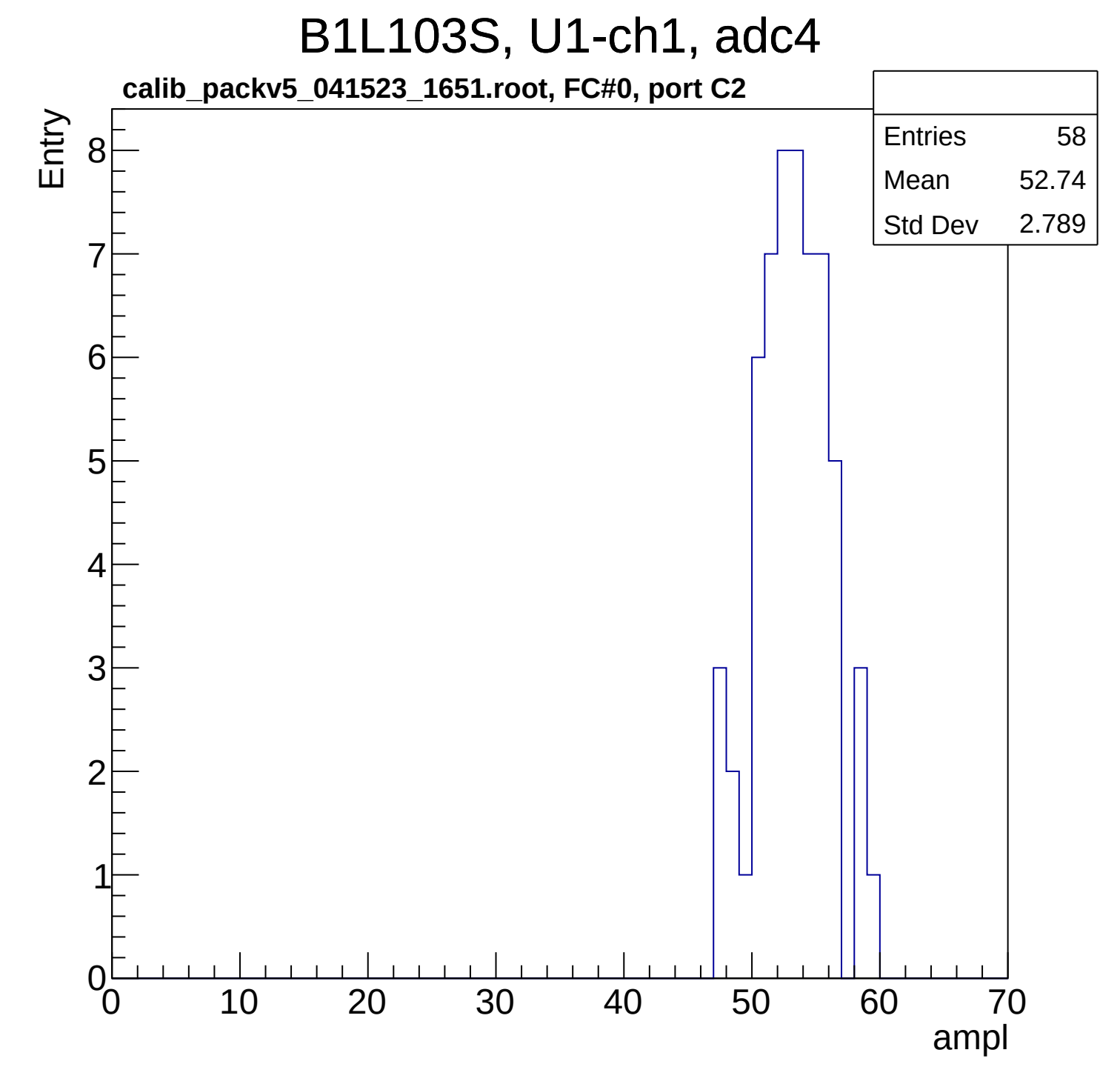
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U1-ch1, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 52.74
Std Dev 2.789
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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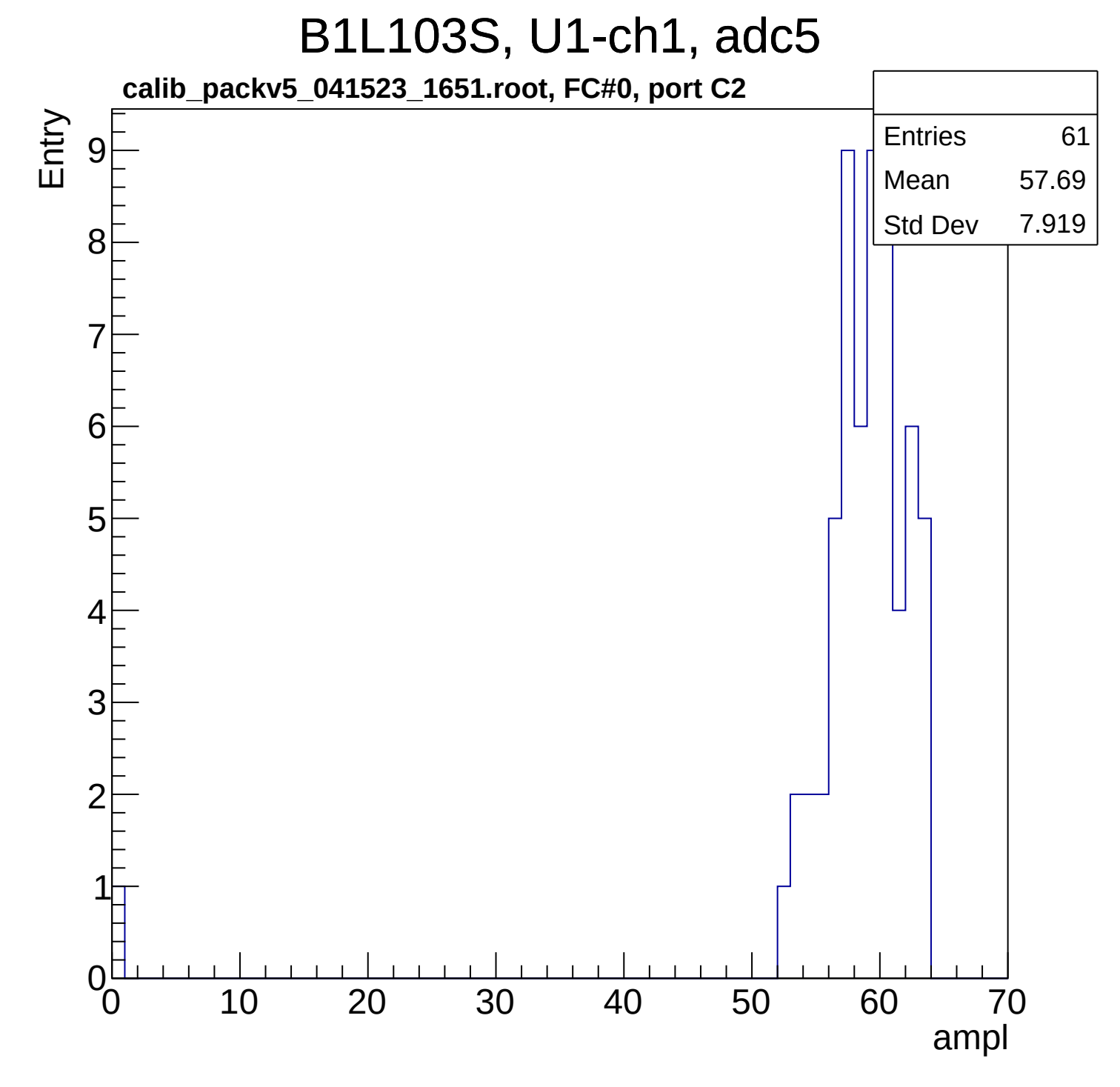
B1L103S, U1-ch1, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 57.69
Std Dev 7.919
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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40
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60
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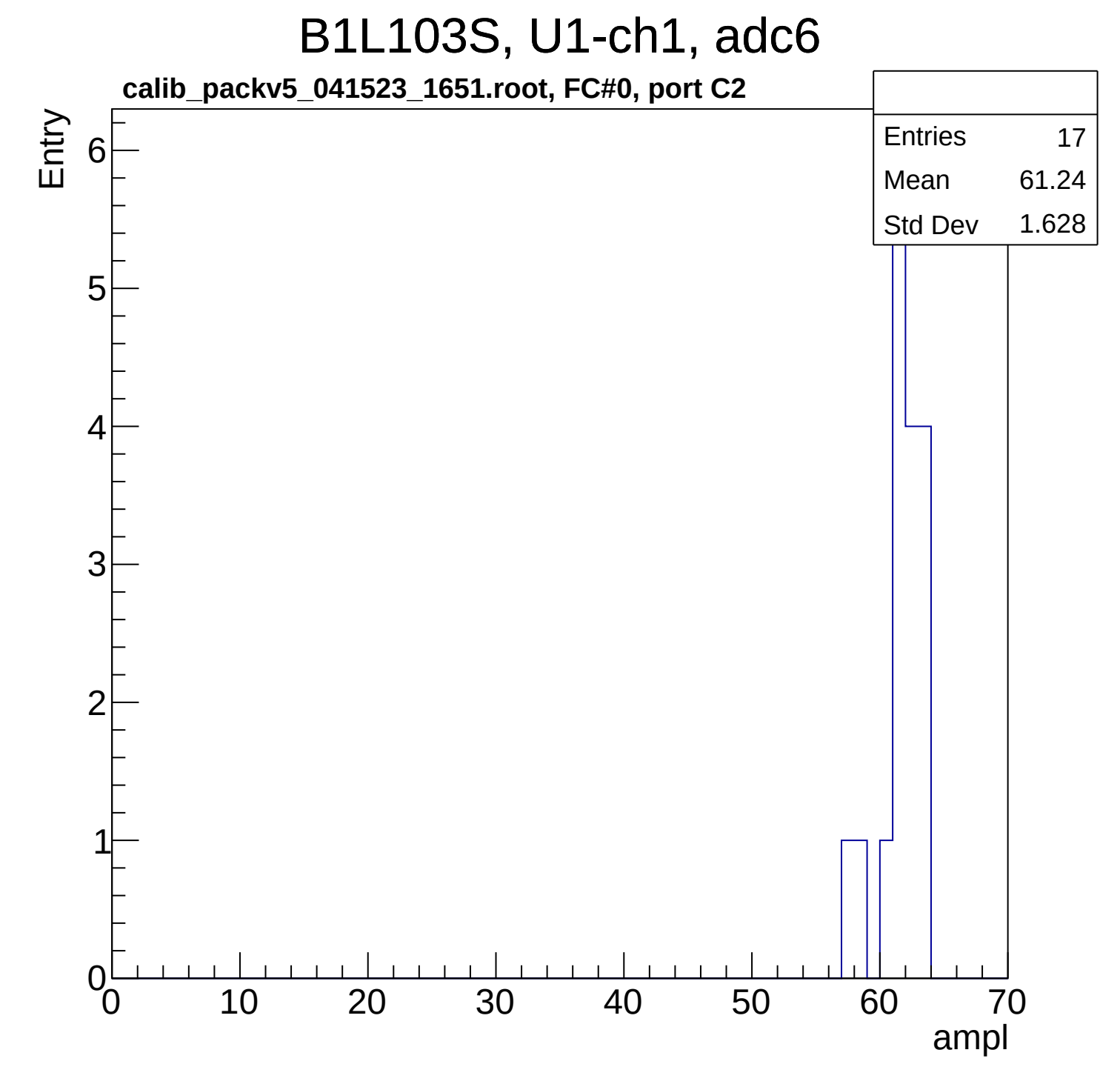
B1L103S, U1-ch1, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 17
Mean 61.24
Std Dev 1.628
Entry
ampl
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2
3
4
5
6
0
10
20
30
40
50
60
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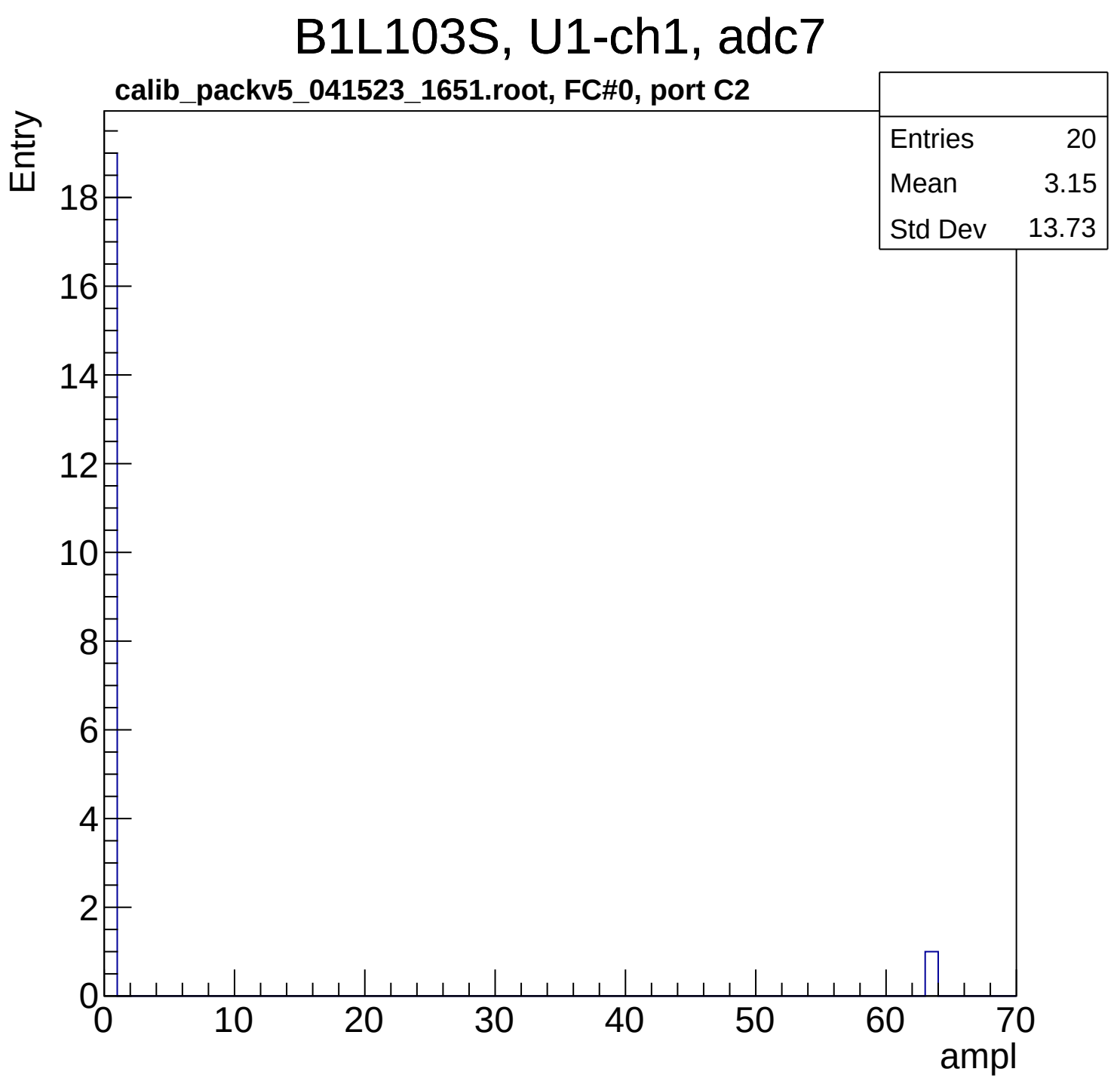
B1L103S, U1-ch1, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
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2
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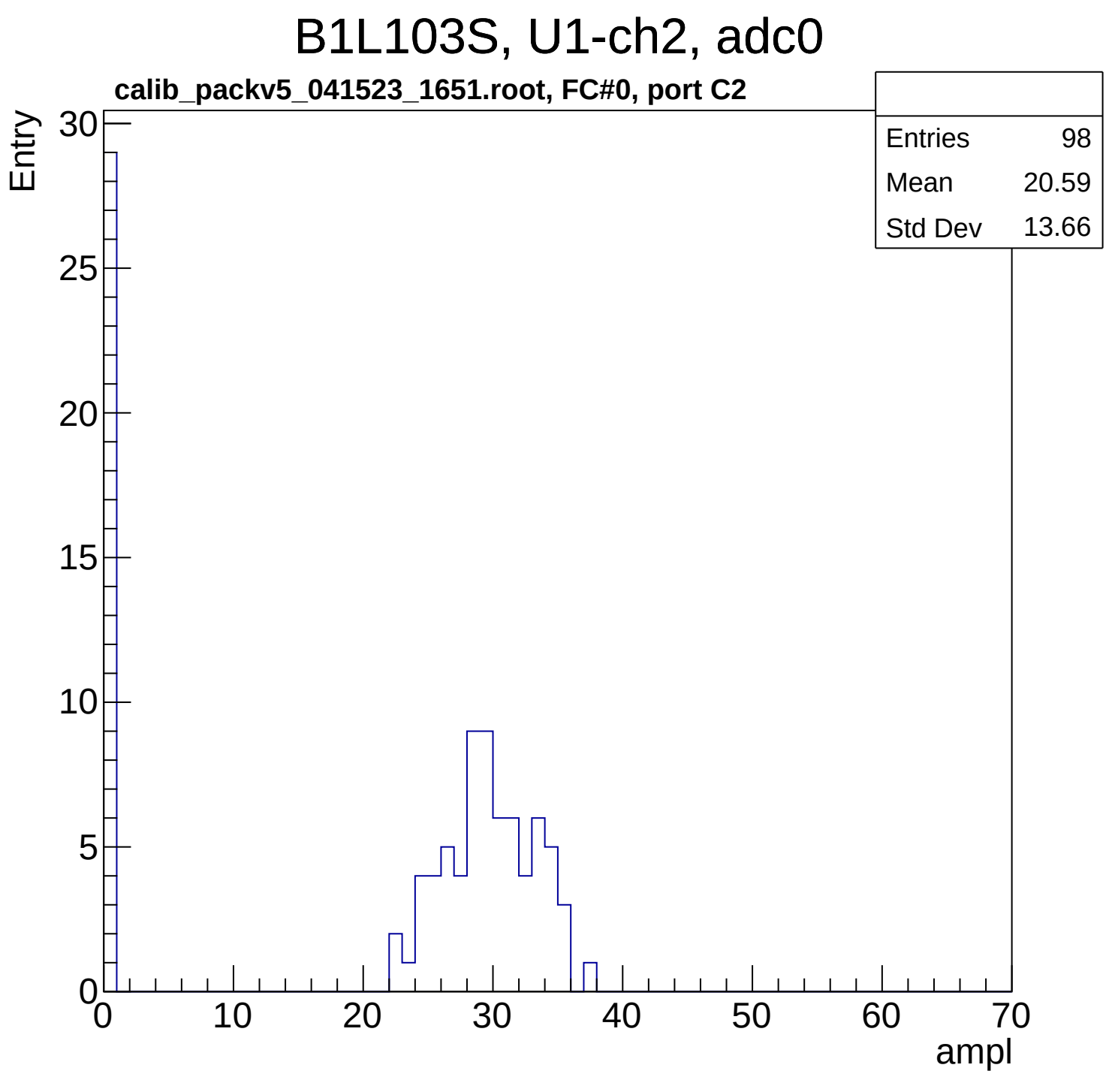
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch2, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 98
Mean 20.59
Std Dev 13.66
Entry
ampl
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10
15
20
25
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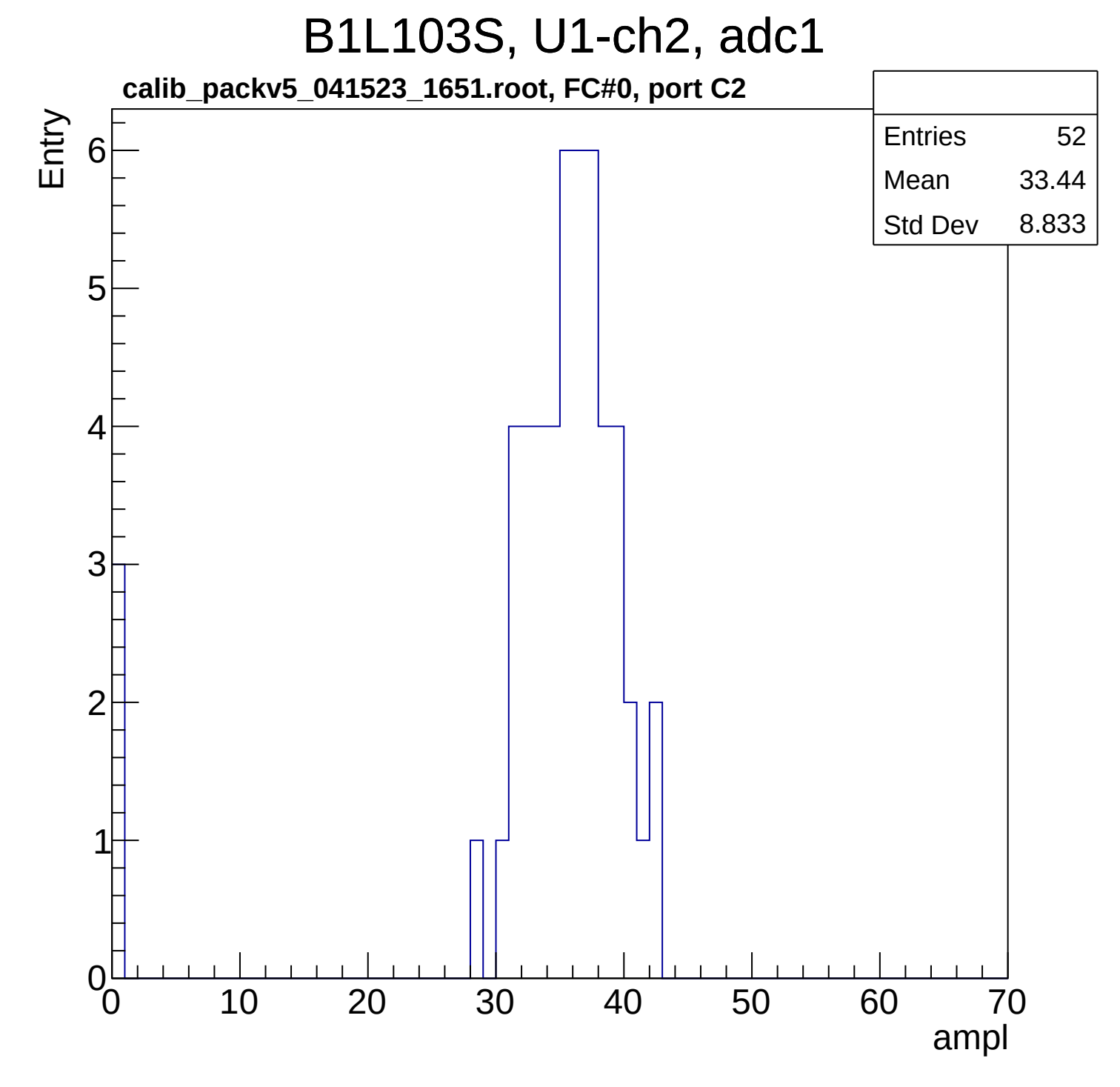
0
10
20
30
40
50
60
70


B1L103S, U1-ch2, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 33.44
Std Dev 8.833
Entry
ampl
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0
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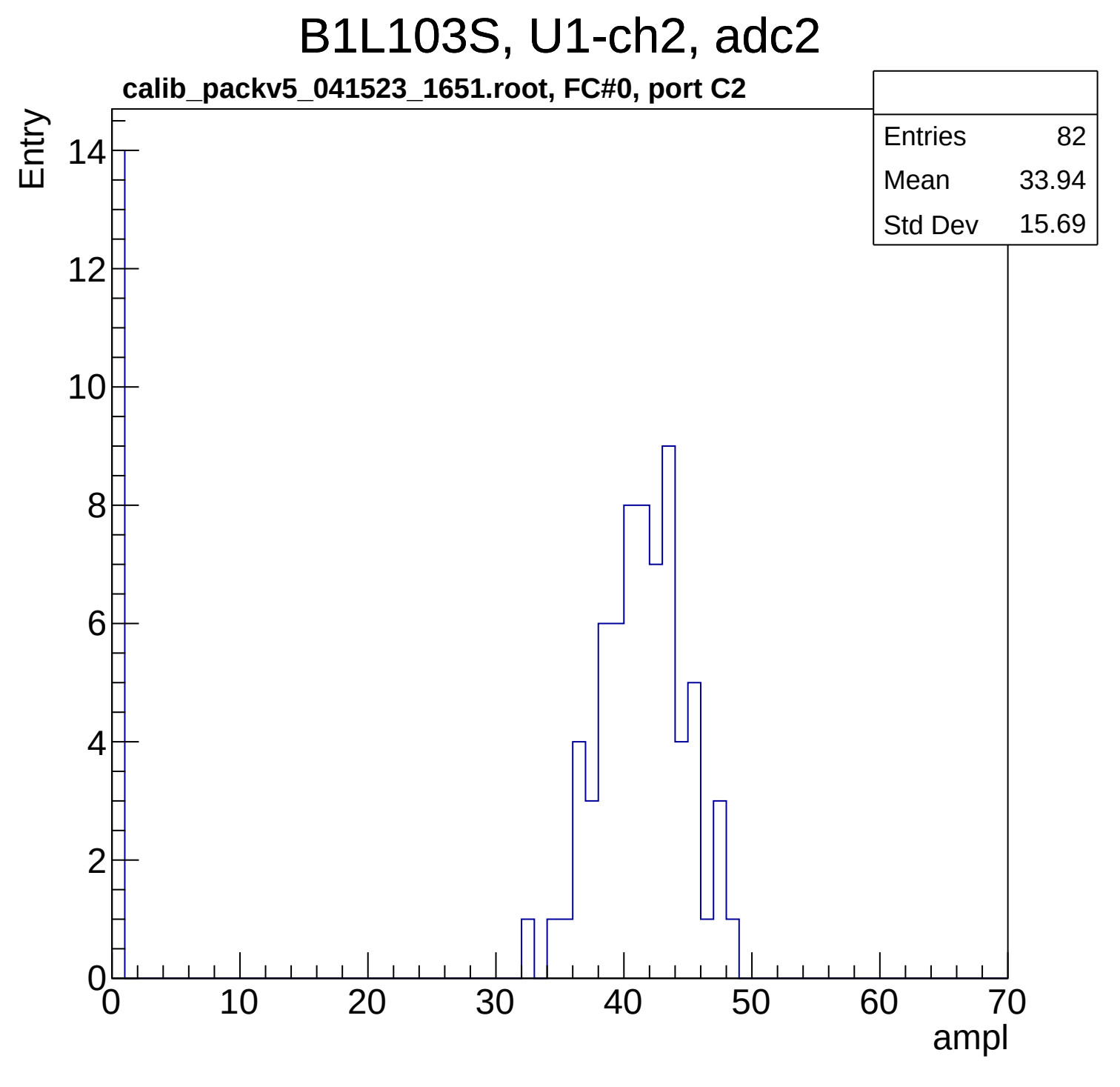
40
50
60
70


B1L103S, U1-ch2, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 33.94
Std Dev 15.69
Entry
ampl
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2
4
6
8
10
12
14
0
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20
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40
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60
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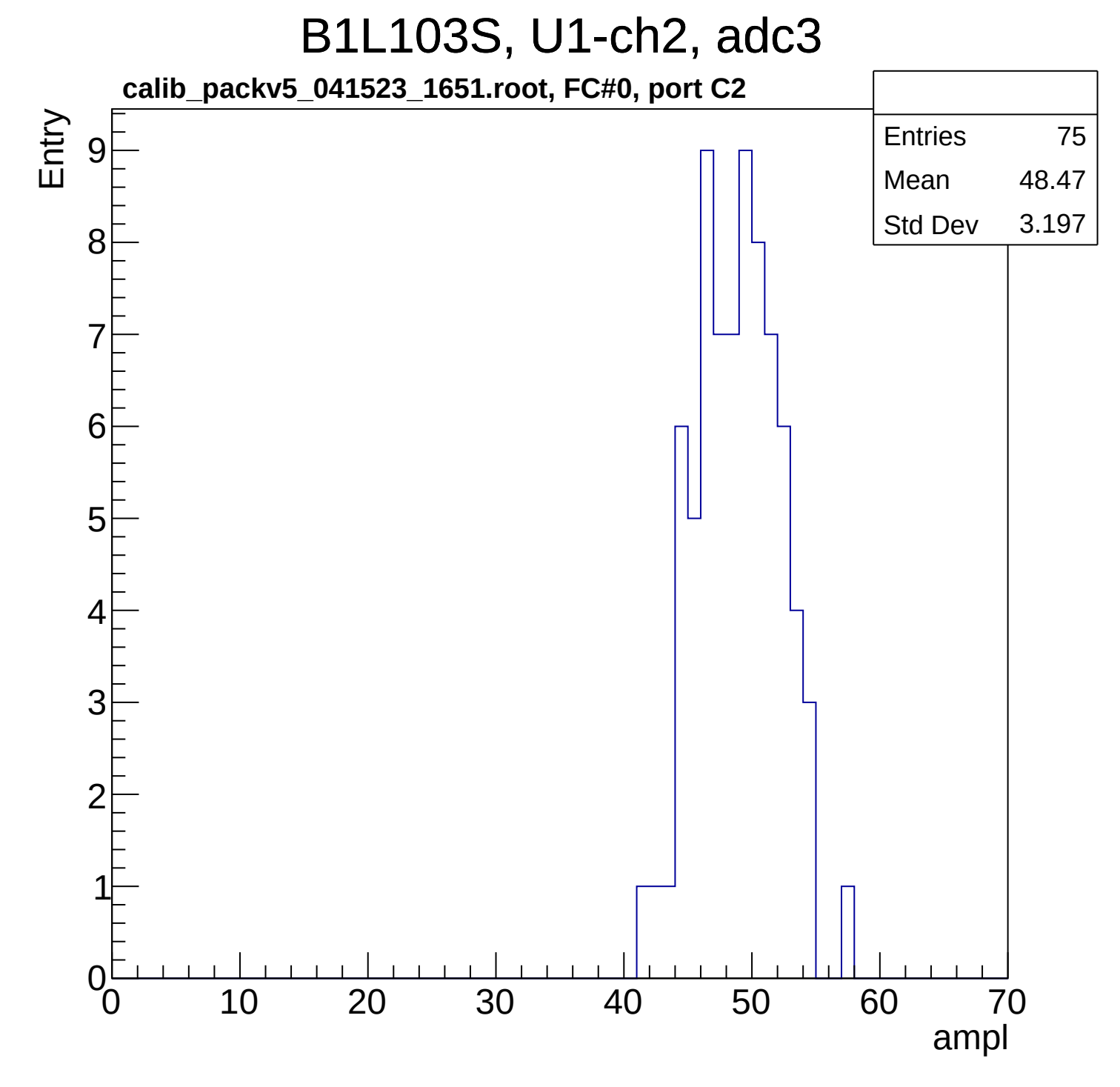
B1L103S, U1-ch2, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 48.47
Std Dev 3.197
Entry
ampl
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3
4
5
6
7
8
9
0
10
20
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40
50
60
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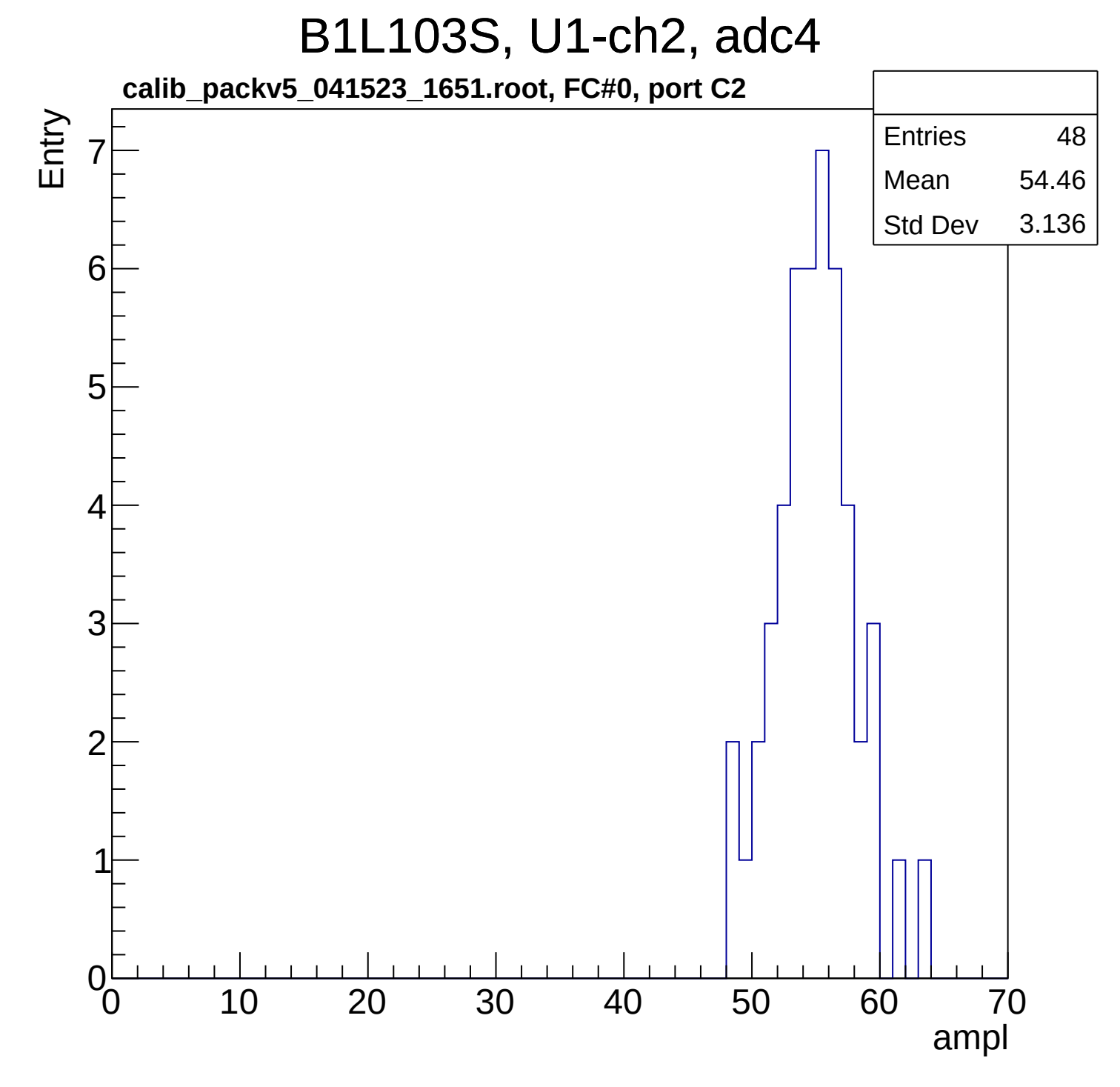
B1L103S, U1-ch2, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 54.46
Std Dev 3.136
Entry
ampl
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0
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60
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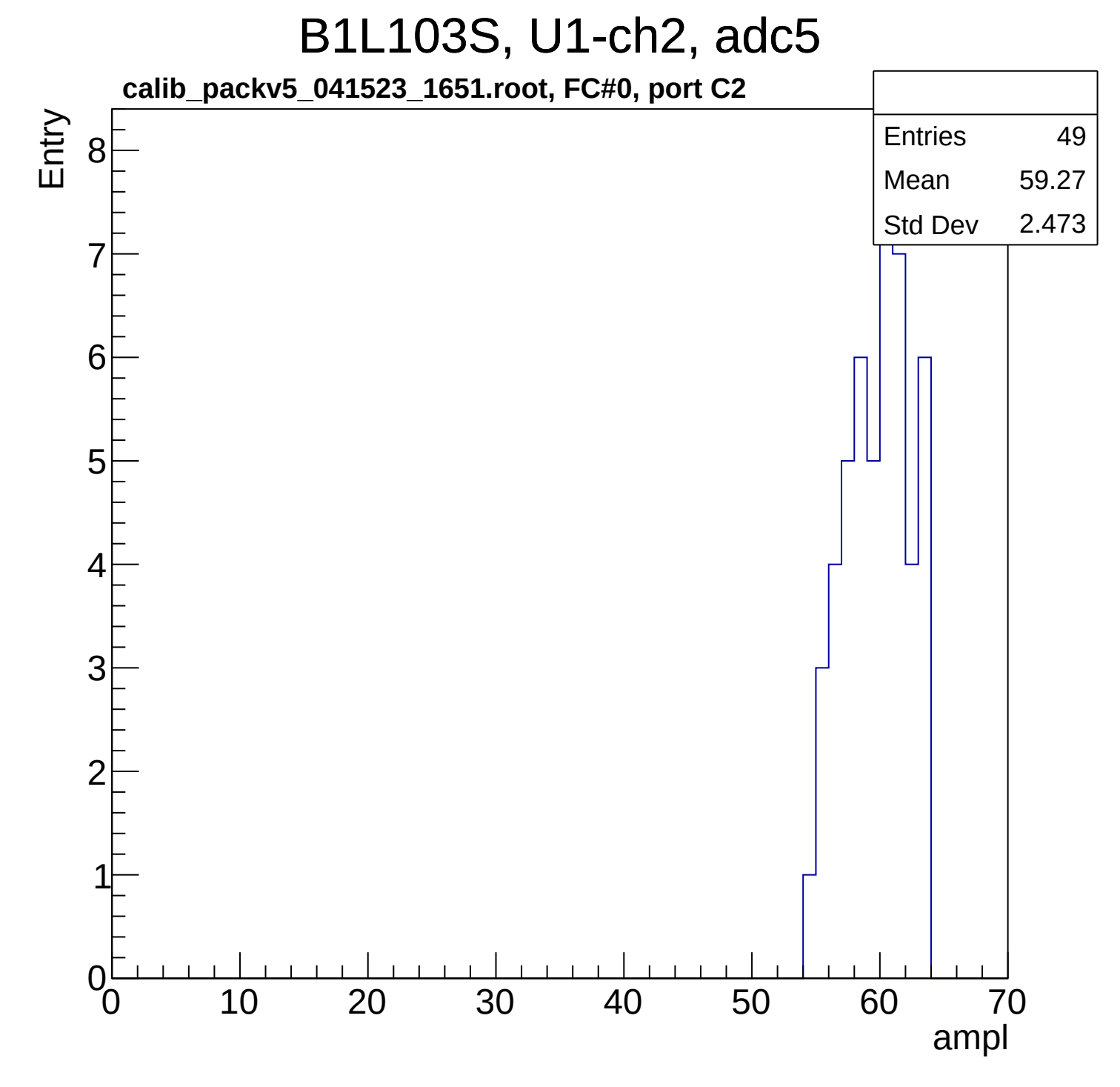
B1L103S, U1-ch2, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 59.27
Std Dev 2.473
Entry
ampl
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4
5
6
7
8
0
10
20
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40
50
60
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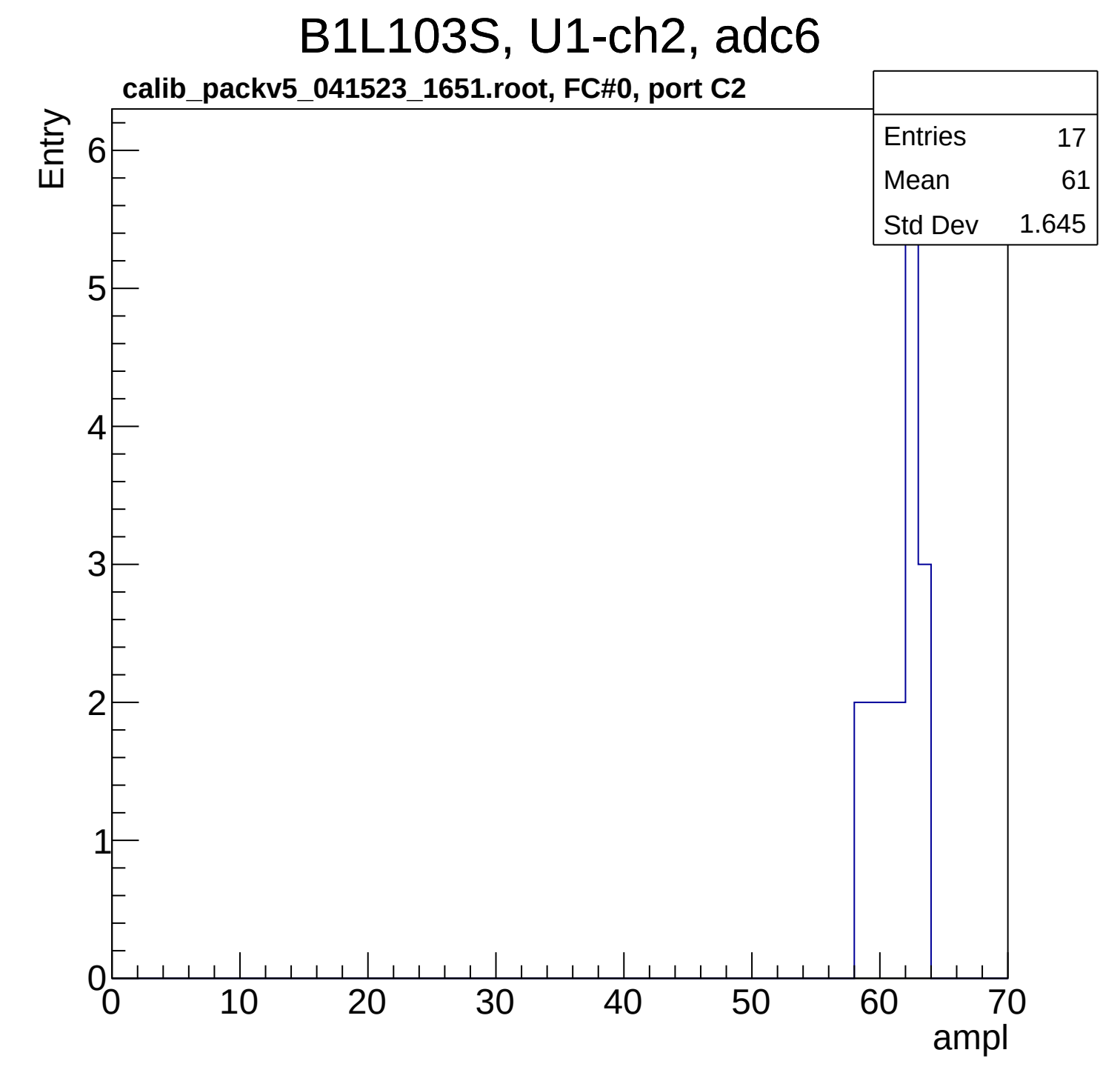
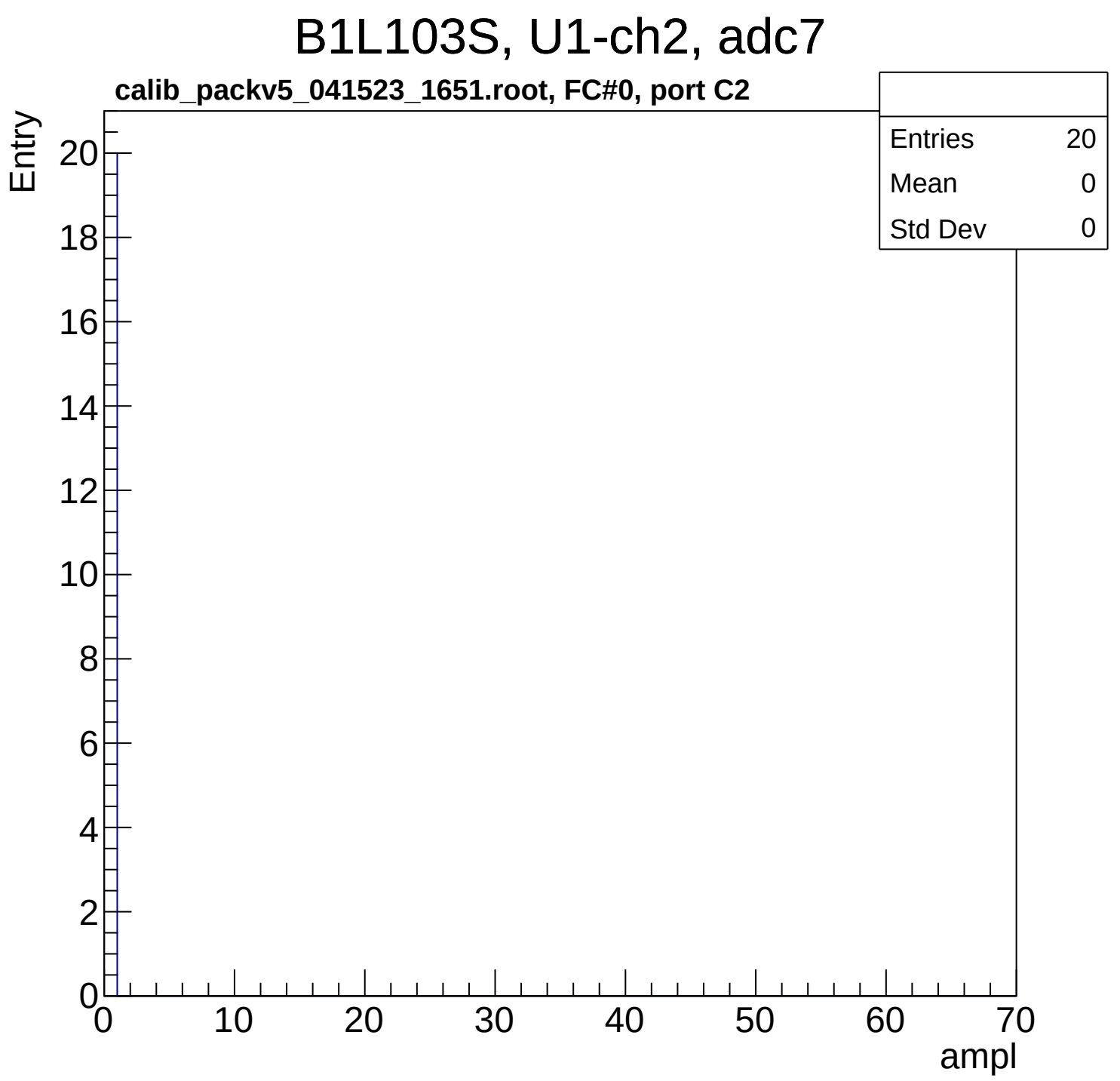

B1L103S, U1-ch2, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 17
Mean 61
Std Dev 1.645
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U1-ch2, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 0
Std Dev 0
Entry
0
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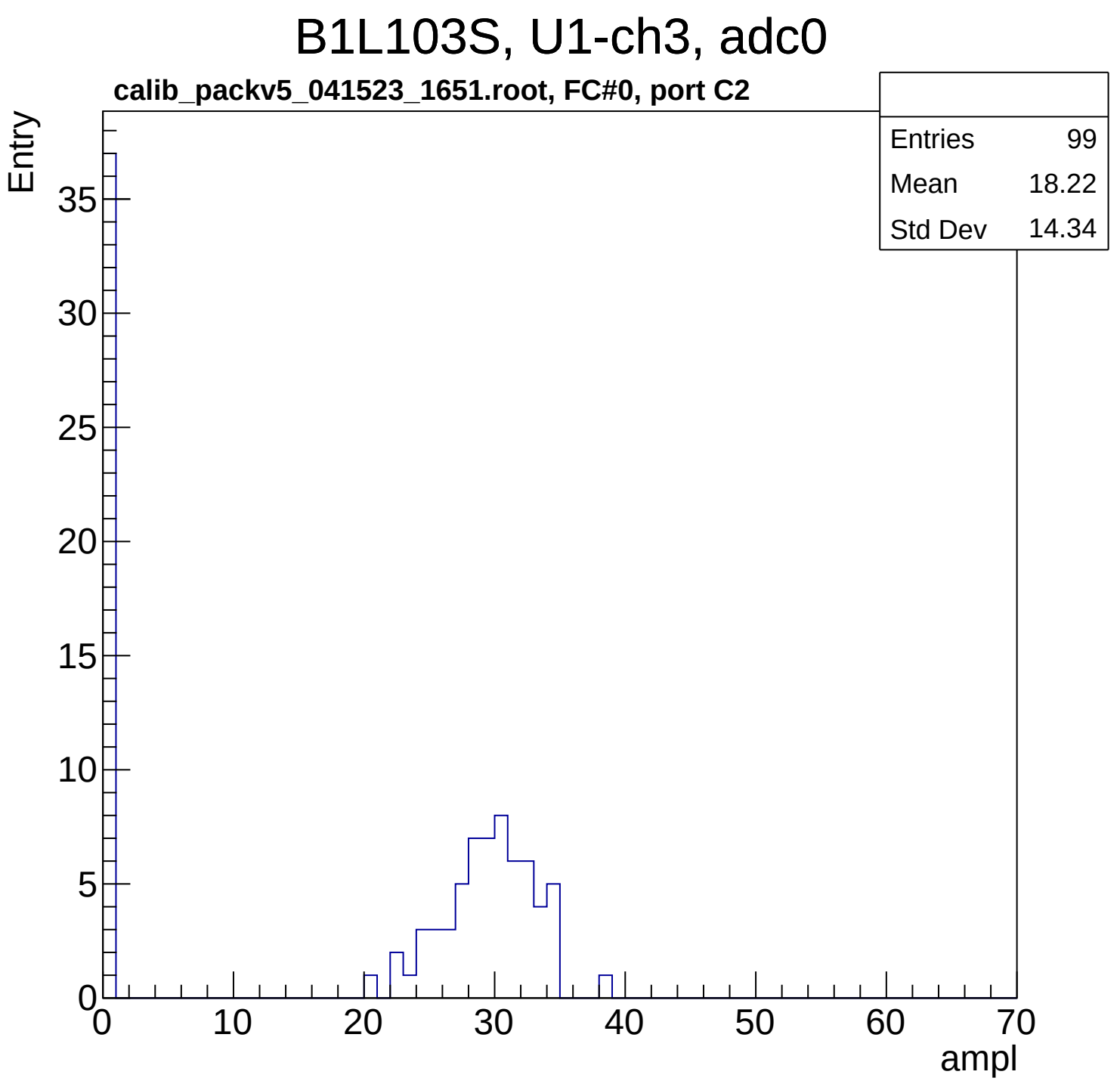
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch3, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 99
Mean 18.22
Std Dev 14.34
Entry
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25
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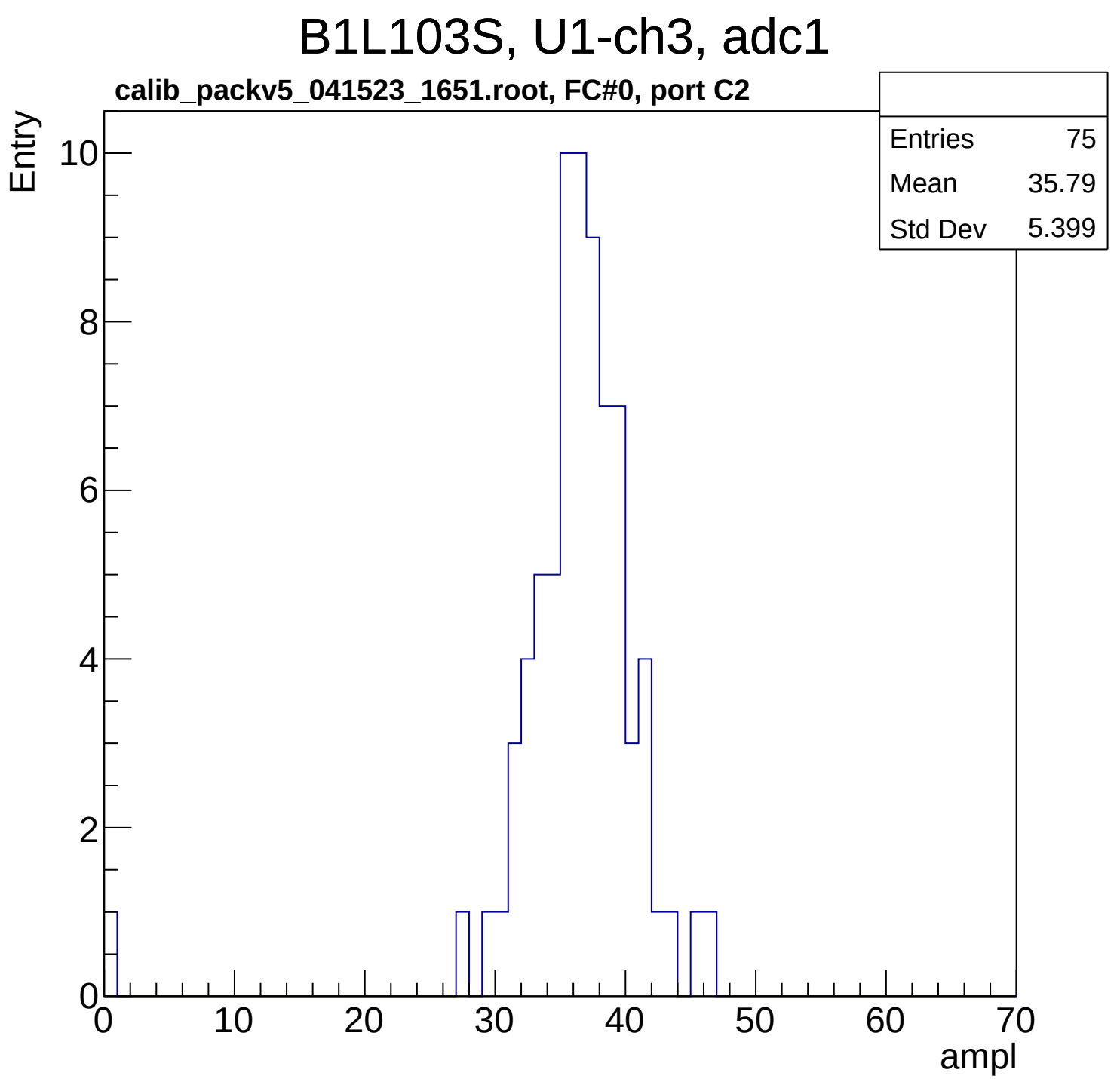
40
50
60
70
ampl


B1L103S, U1-ch3, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 35.79
Std Dev 5.399
Entry
ampl
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4
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0
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40
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60
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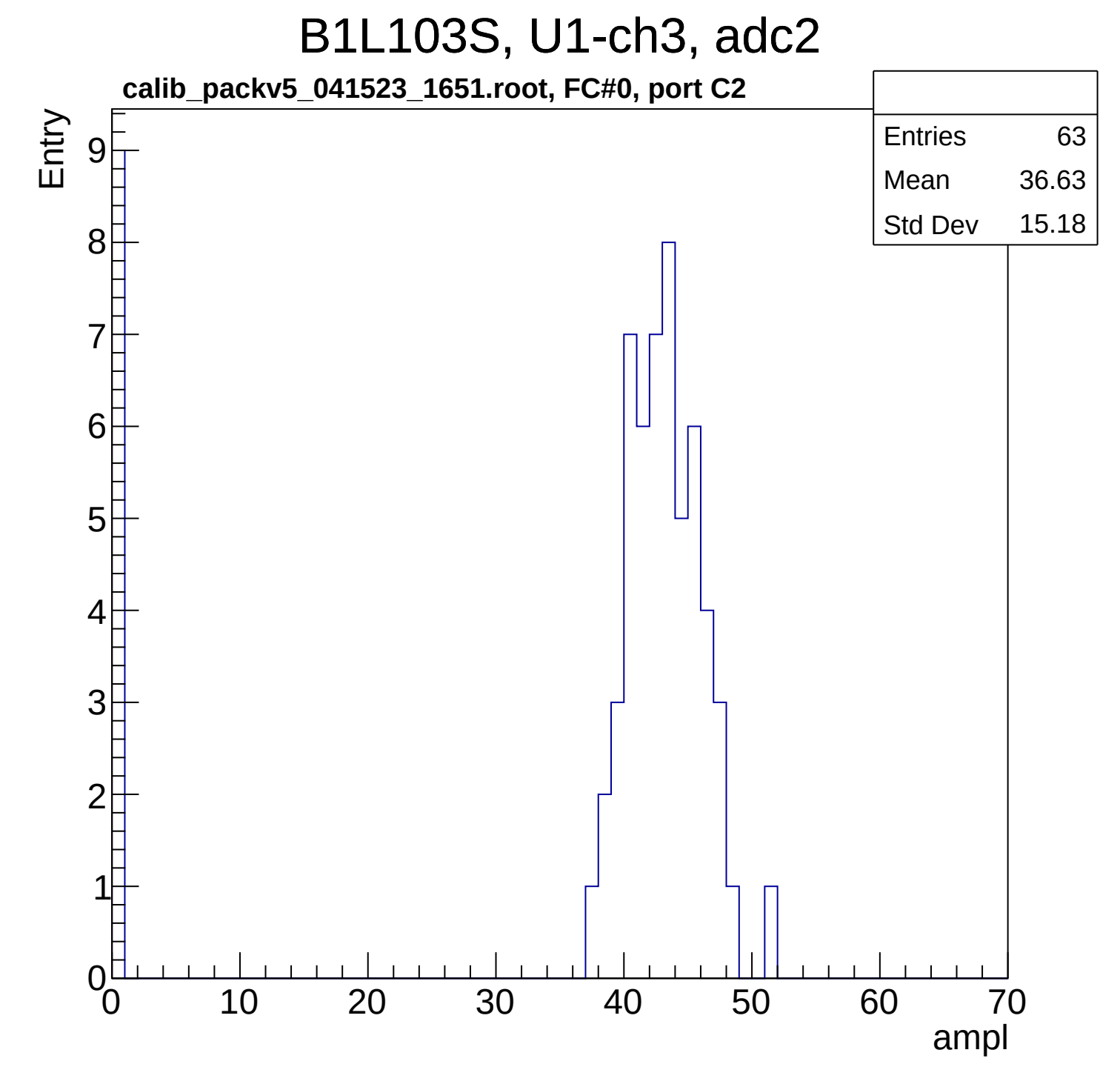
B1L103S, U1-ch3, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 36.63
Std Dev 15.18
Entry
ampl
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3
4
5
6
7
8
9
0
10
20
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40
50
60
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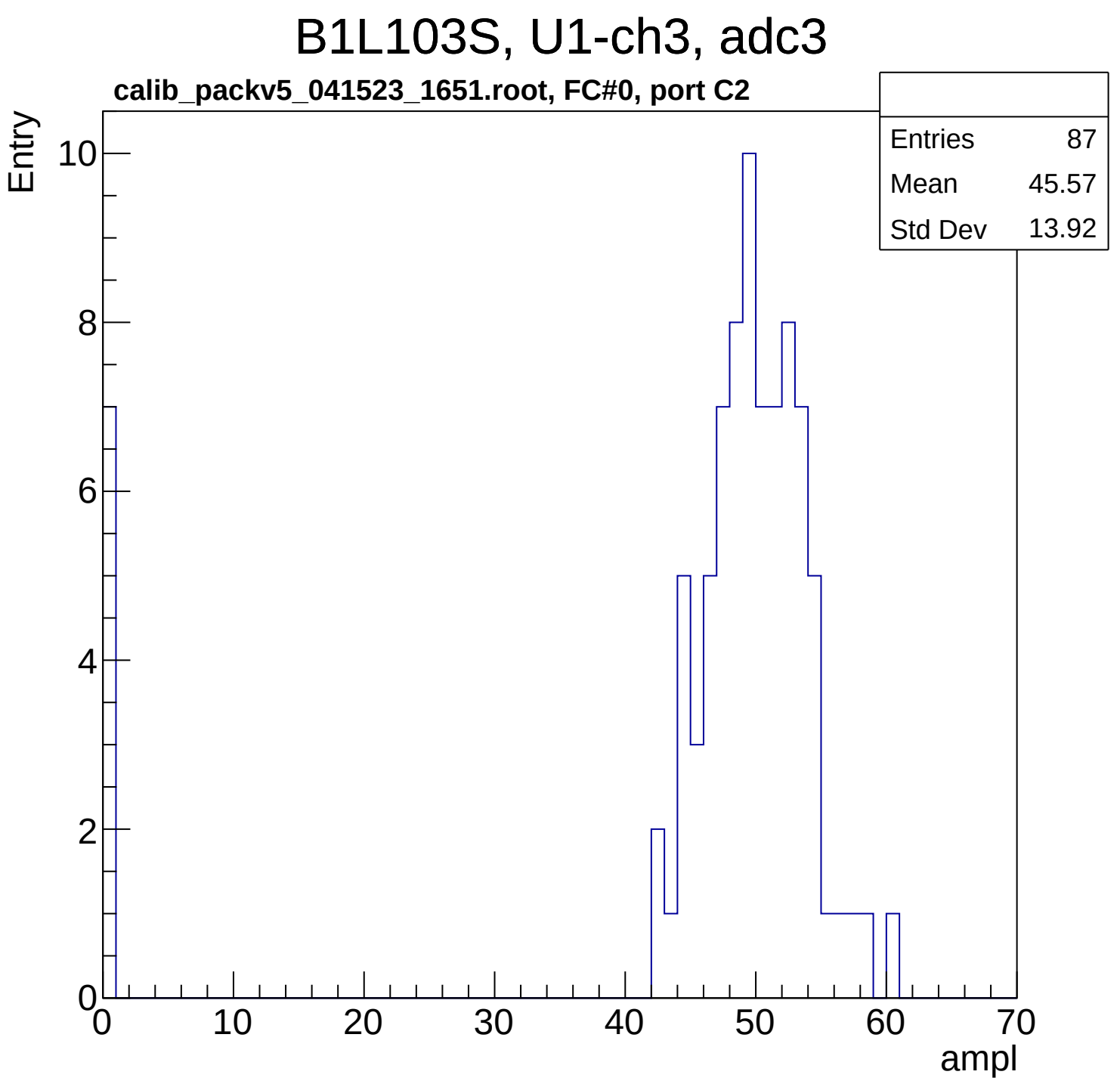
B1L103S, U1-ch3, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 87
Mean 45.57
Std Dev 13.92
Entry
ampl
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4
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8
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0
10
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40
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60
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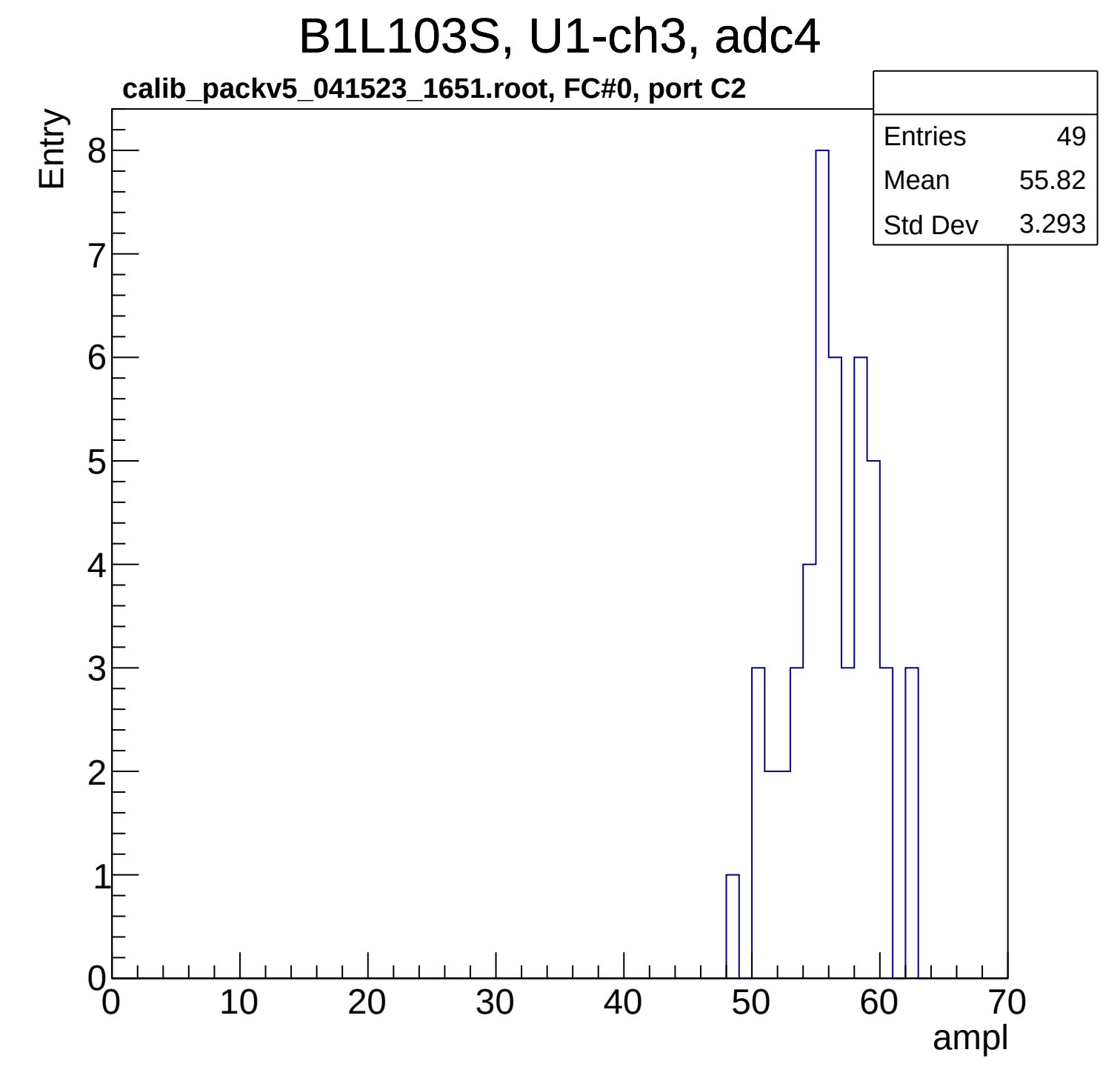
B1L103S, U1-ch3, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 55.82
Std Dev 3.293
Entry
ampl
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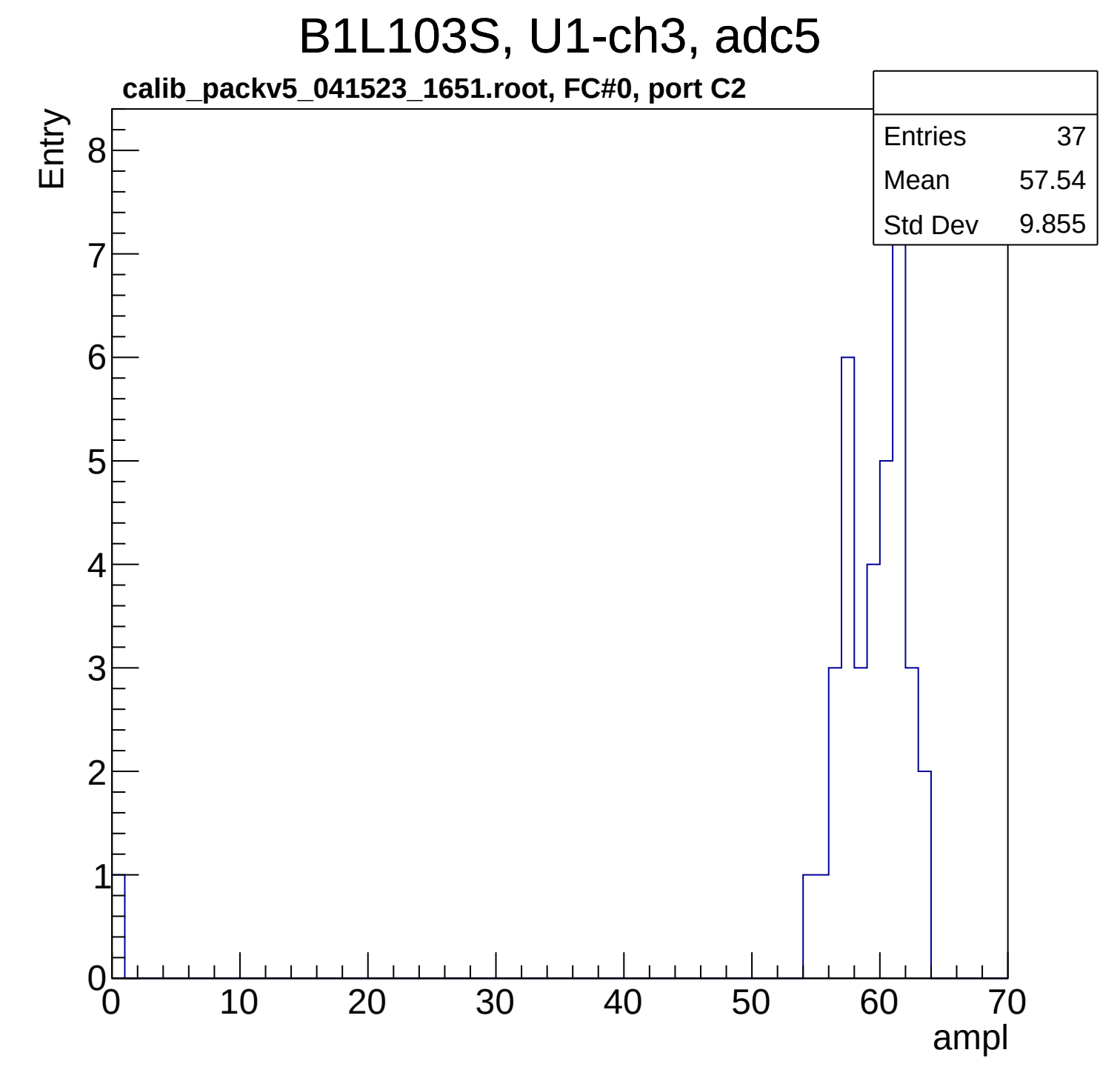
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U1-ch3, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 37
Mean 57.54
Std Dev 9.855
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
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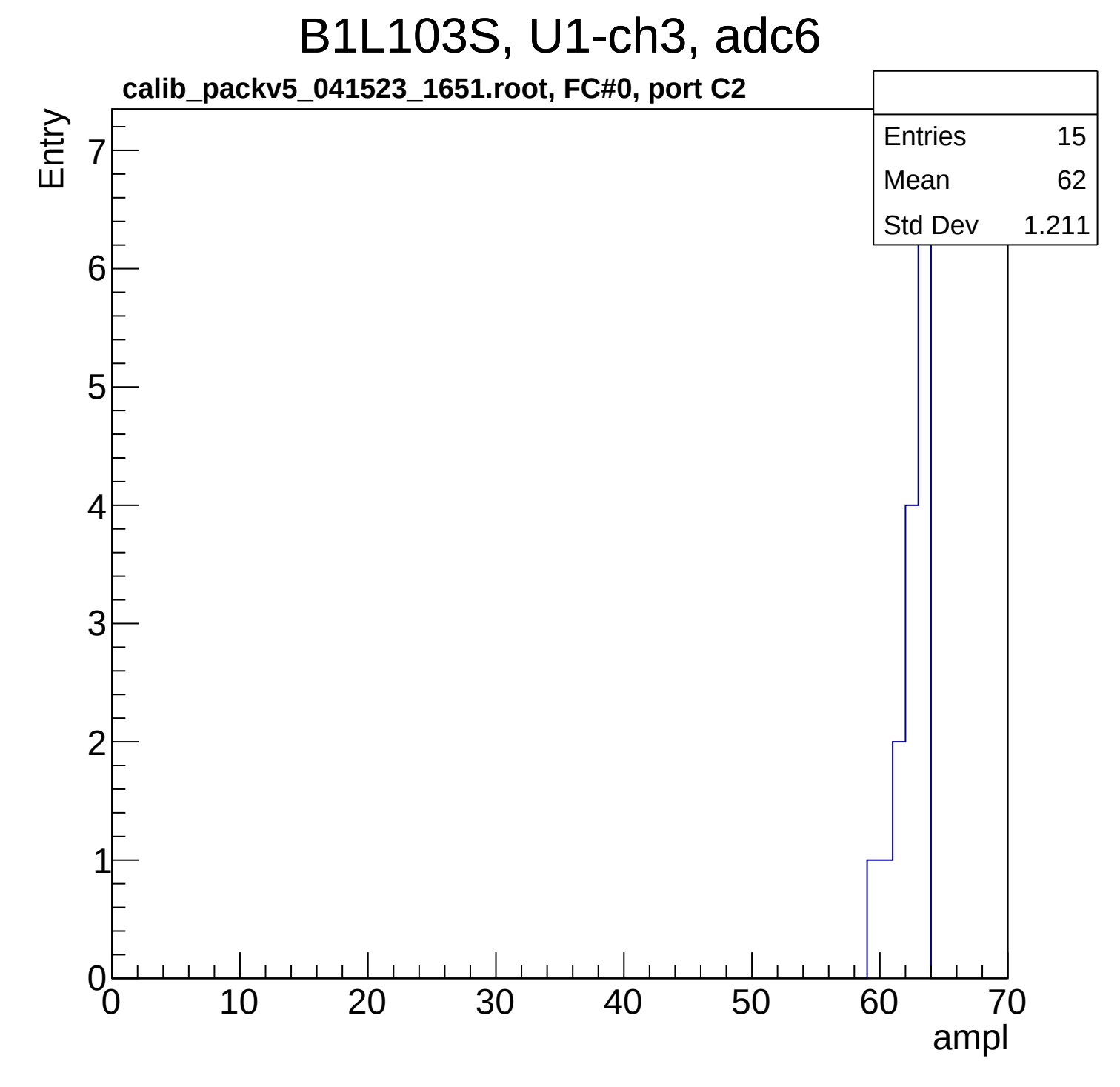
60
70


B1L103S, U1-ch3, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 15
Mean 62
Std Dev 1.211
Entry
ampl
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1
2
3
4
5
6
7
0
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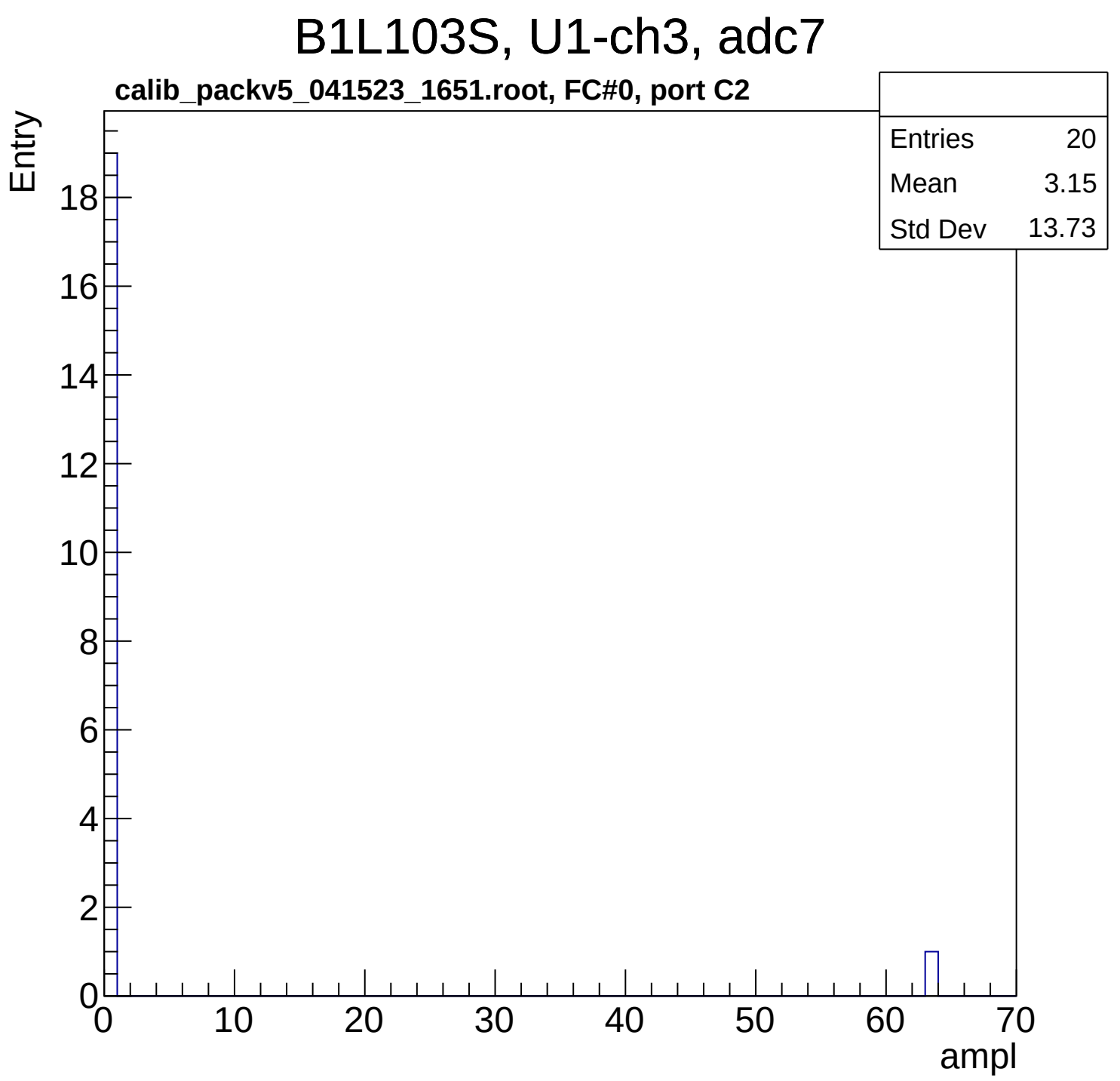
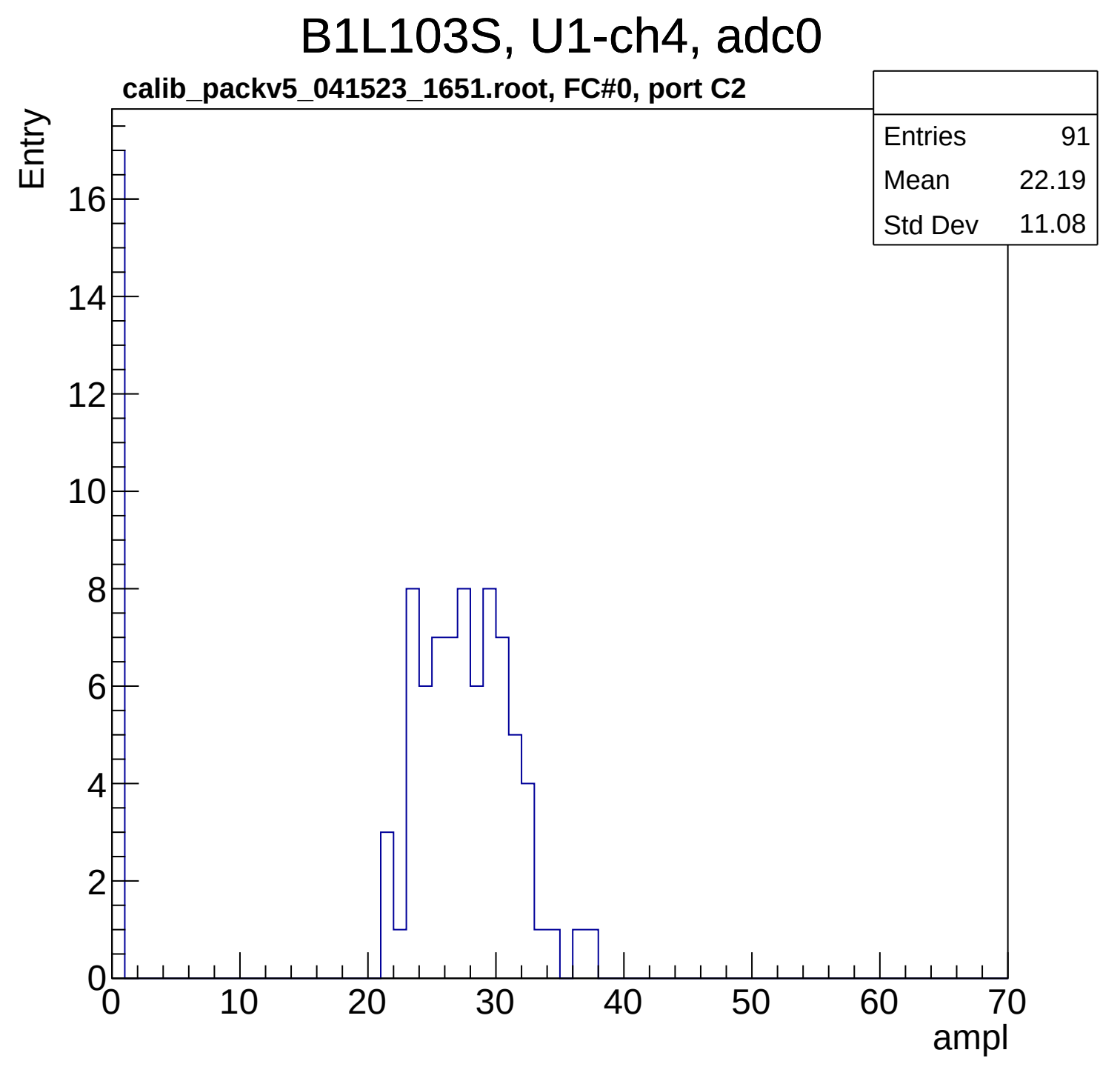
40
50
60
70


B1L103S, U1-ch3, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch4, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 91
Mean 22.19
Std Dev 11.08
Entry
0
2
4
6
8
10
12
14
16
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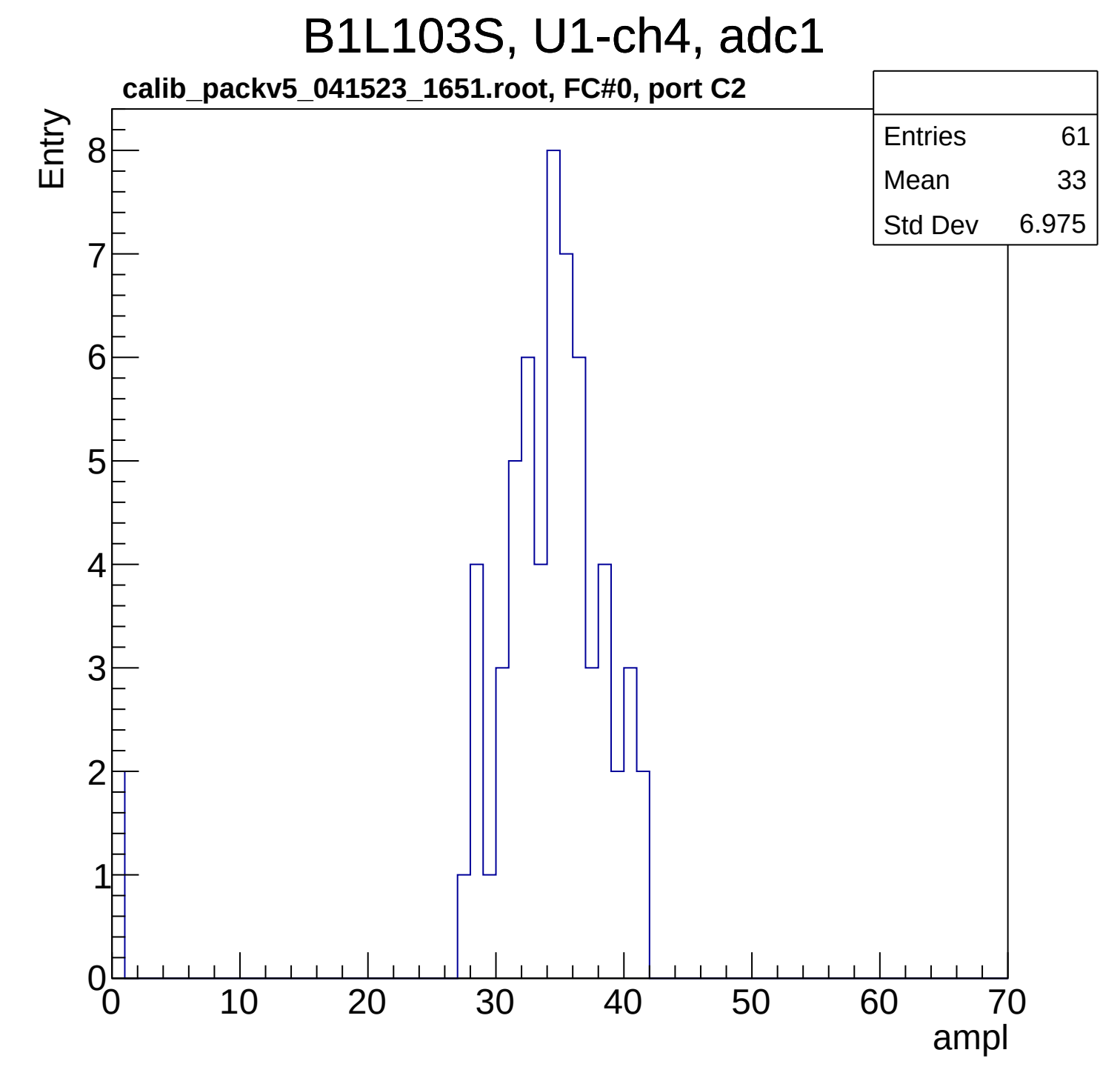
ampl


B1L103S, U1-ch4, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 33
Std Dev 6.975
Entry
ampl
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2
3
4
5
6
7
8
0
10
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40
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60
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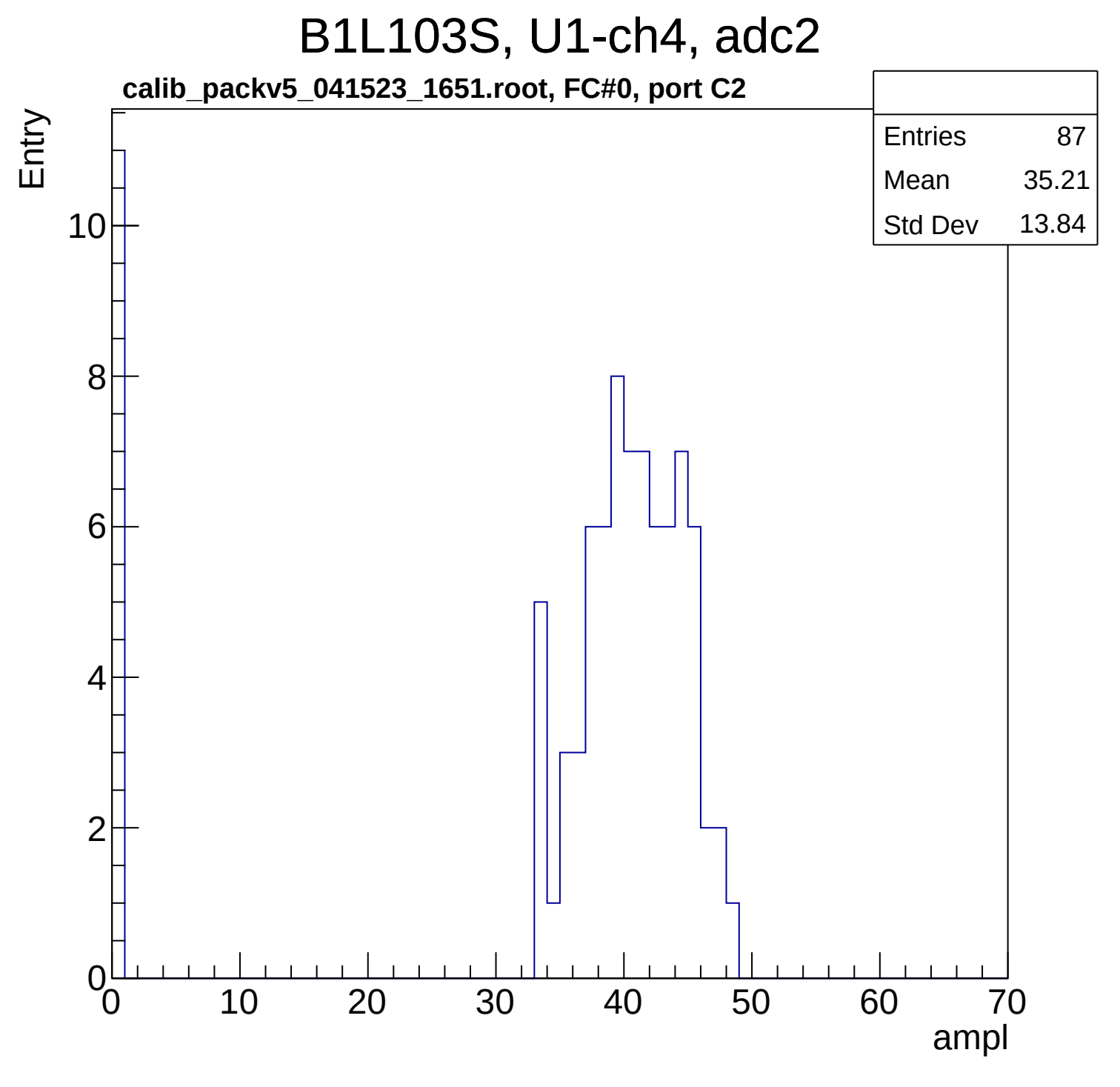
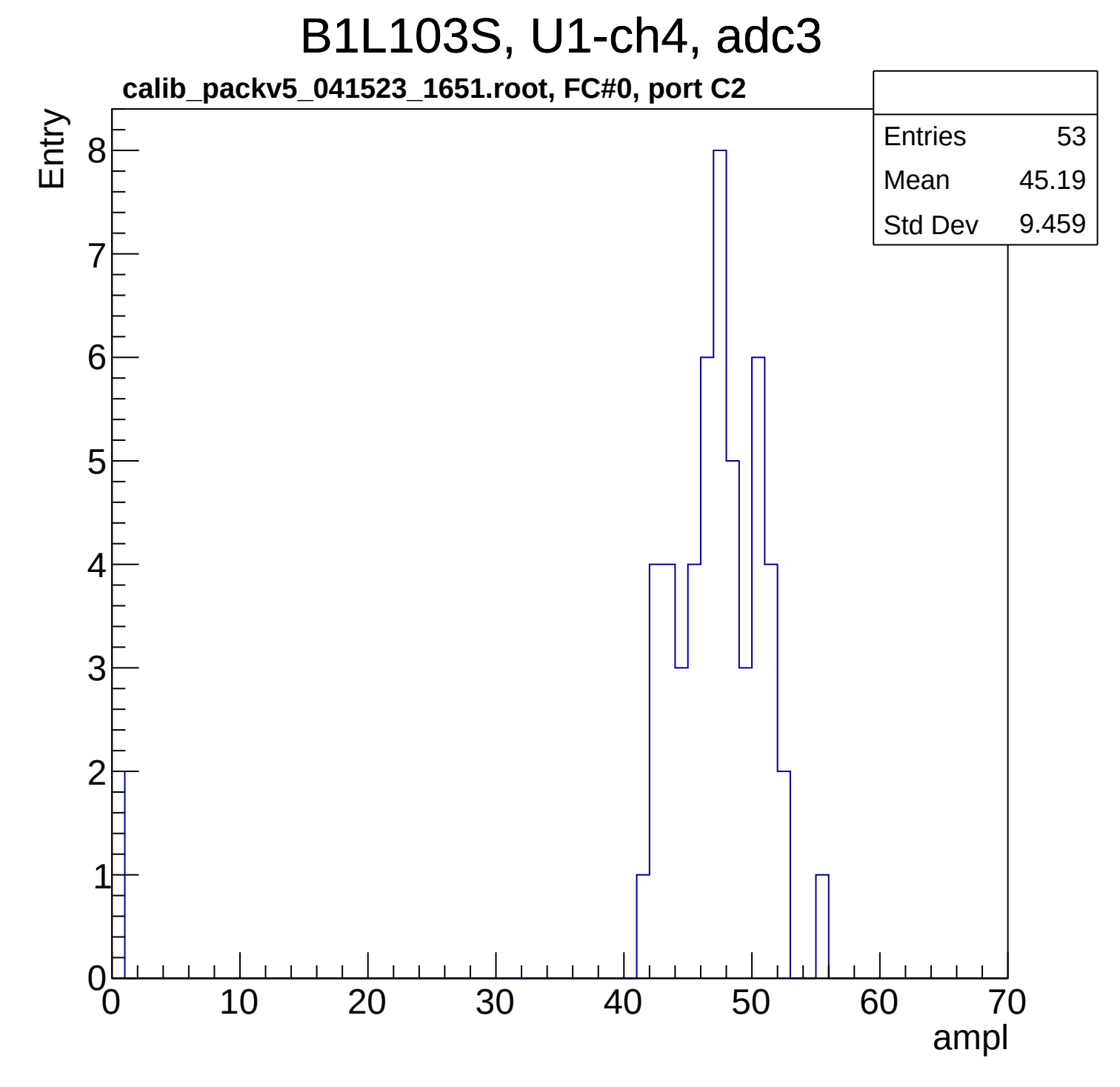

B1L103S, U1-ch4, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 87
Mean 35.21
Std Dev 13.84
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch4, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 45.19
Std Dev 9.459
Entry
ampl
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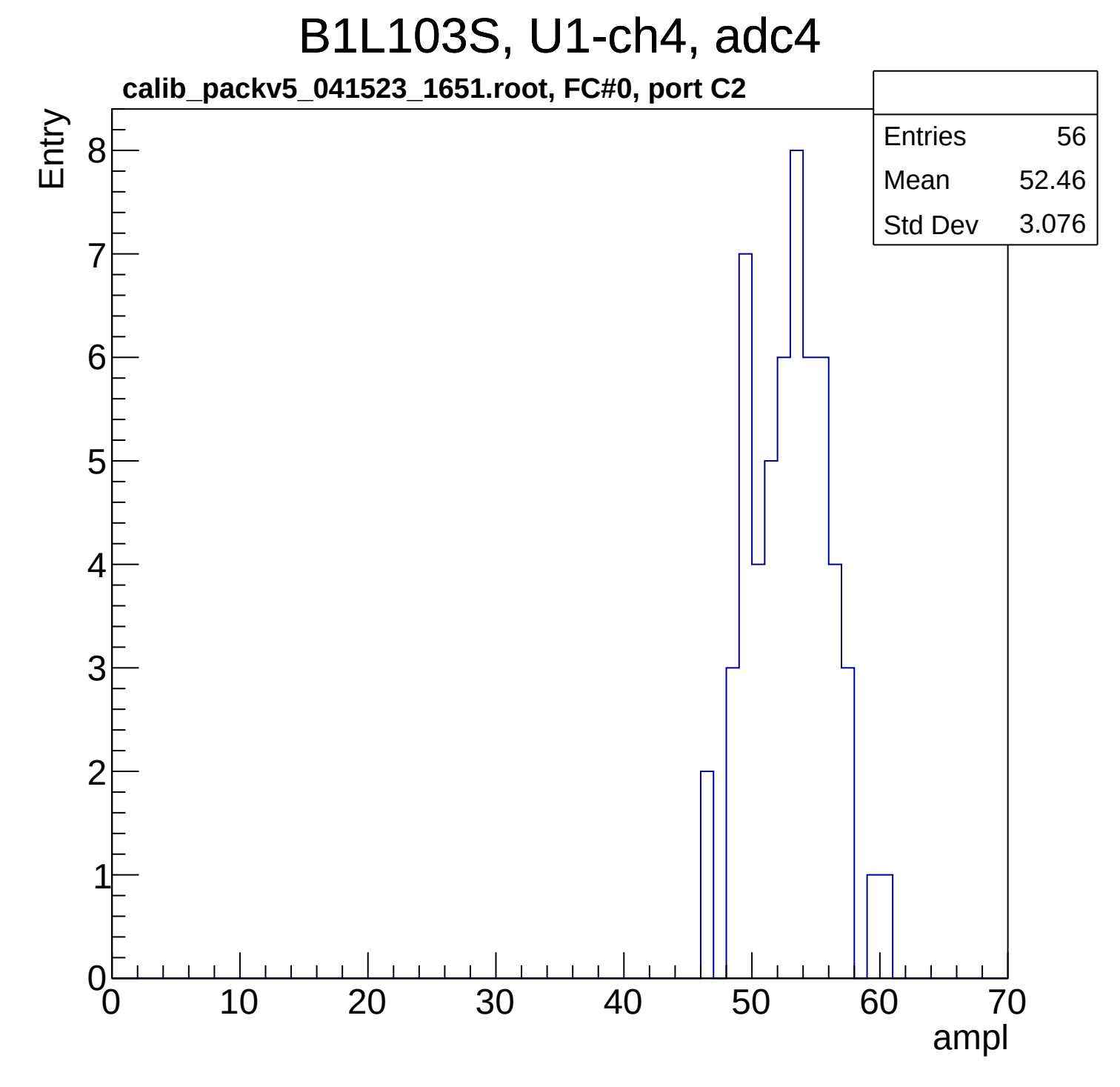
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U1-ch4, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 52.46
Std Dev 3.076
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
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40
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60
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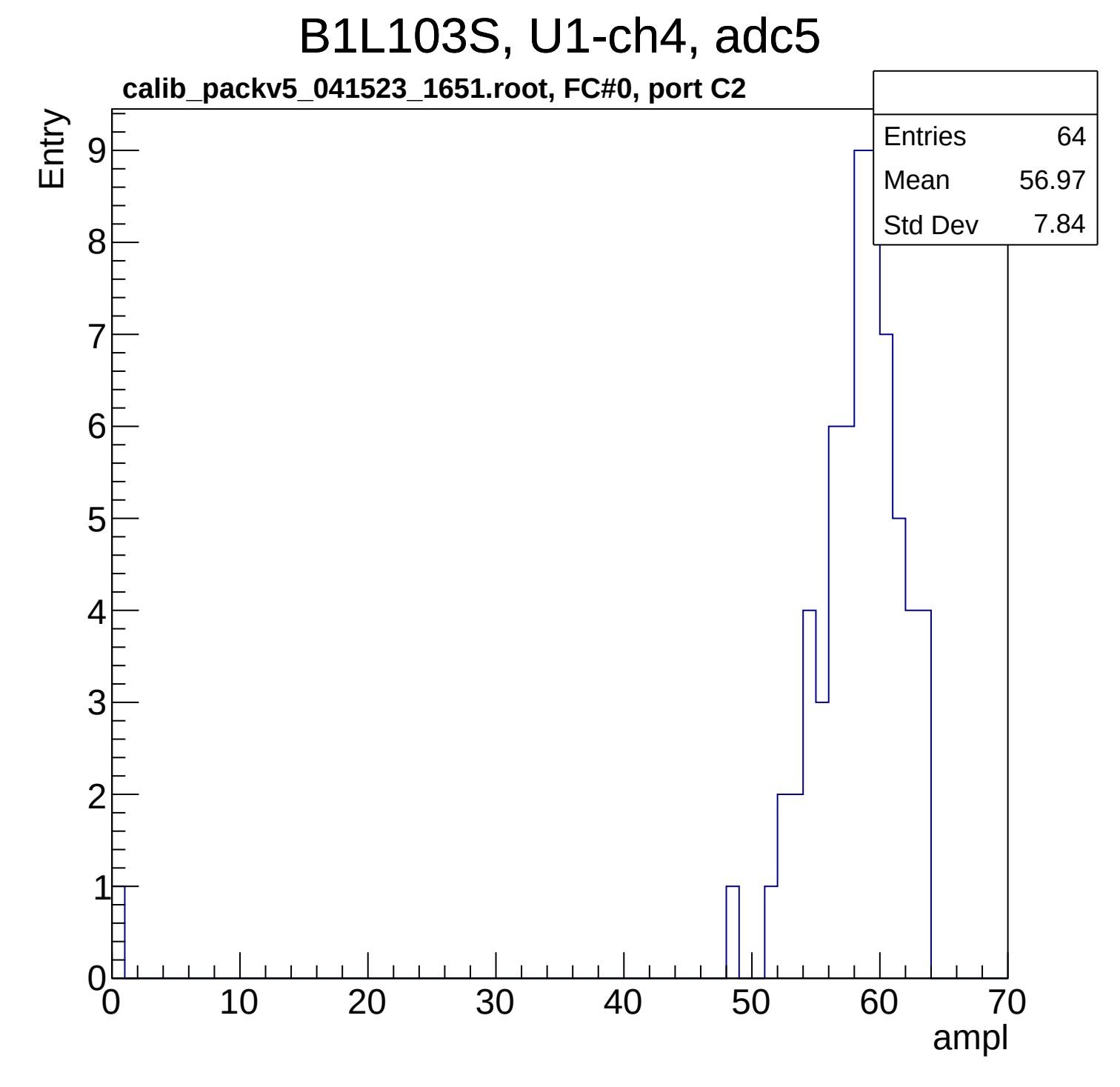
B1L103S, U1-ch4, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 56.97
Std Dev 7.84
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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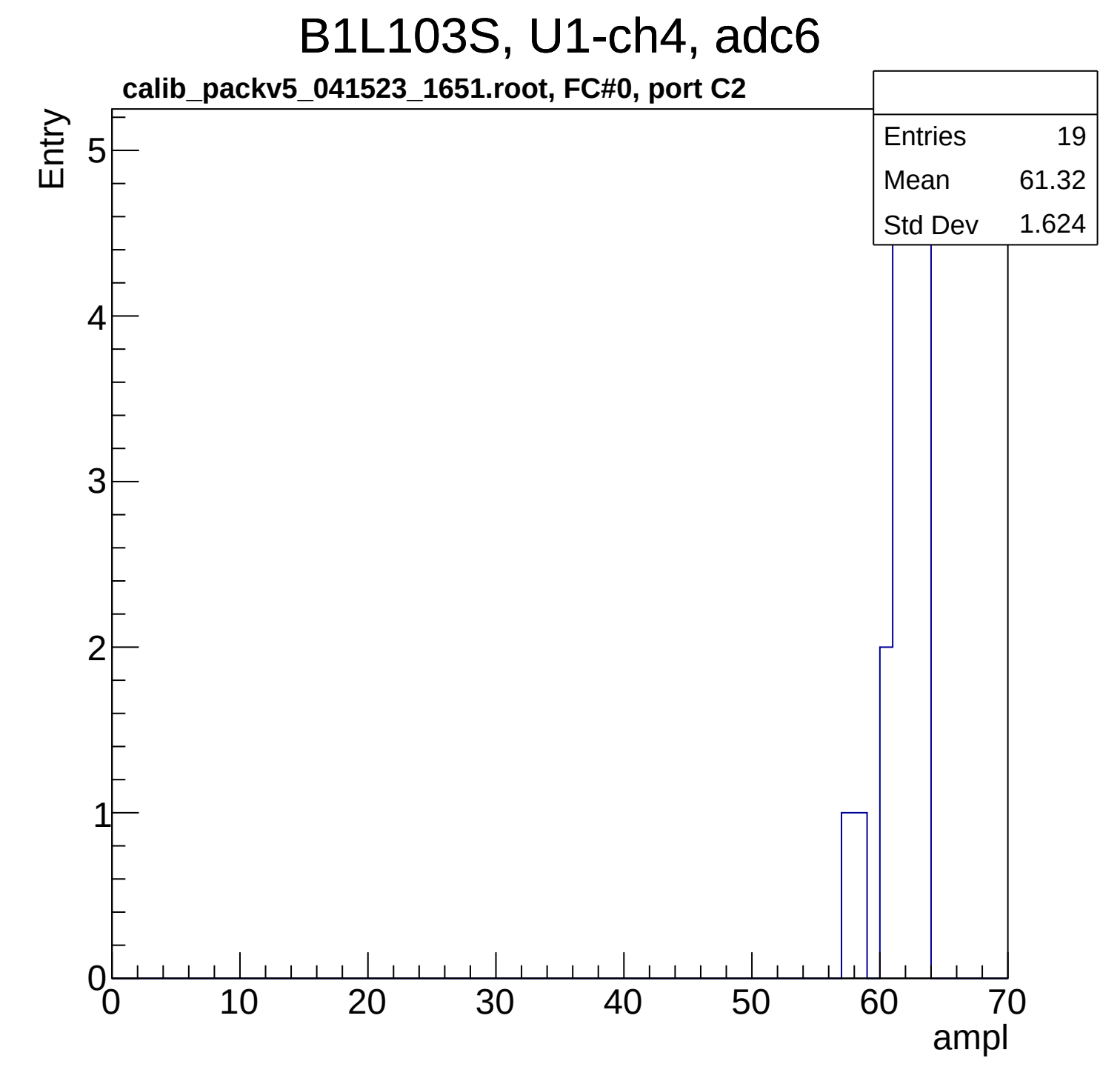
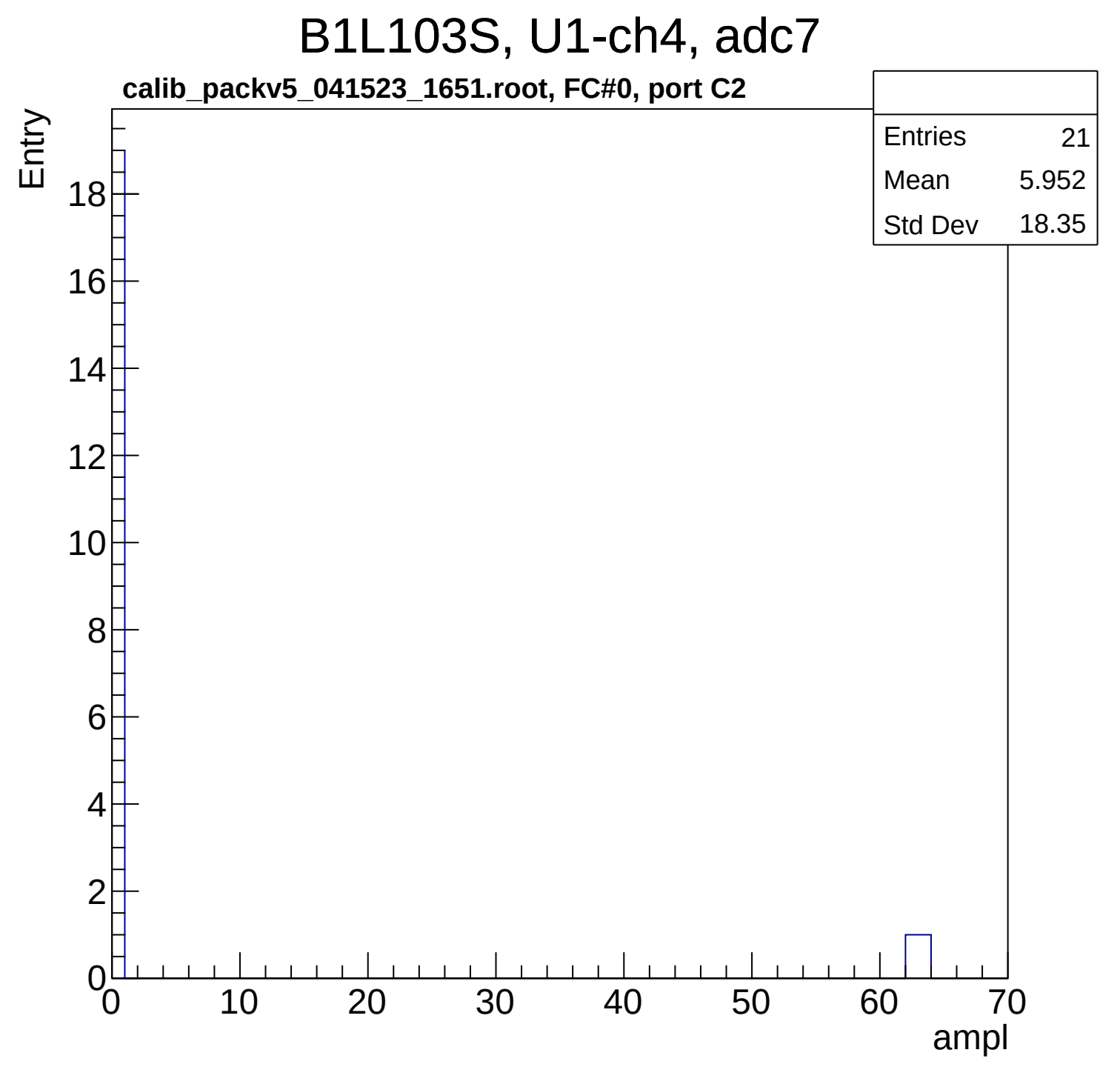
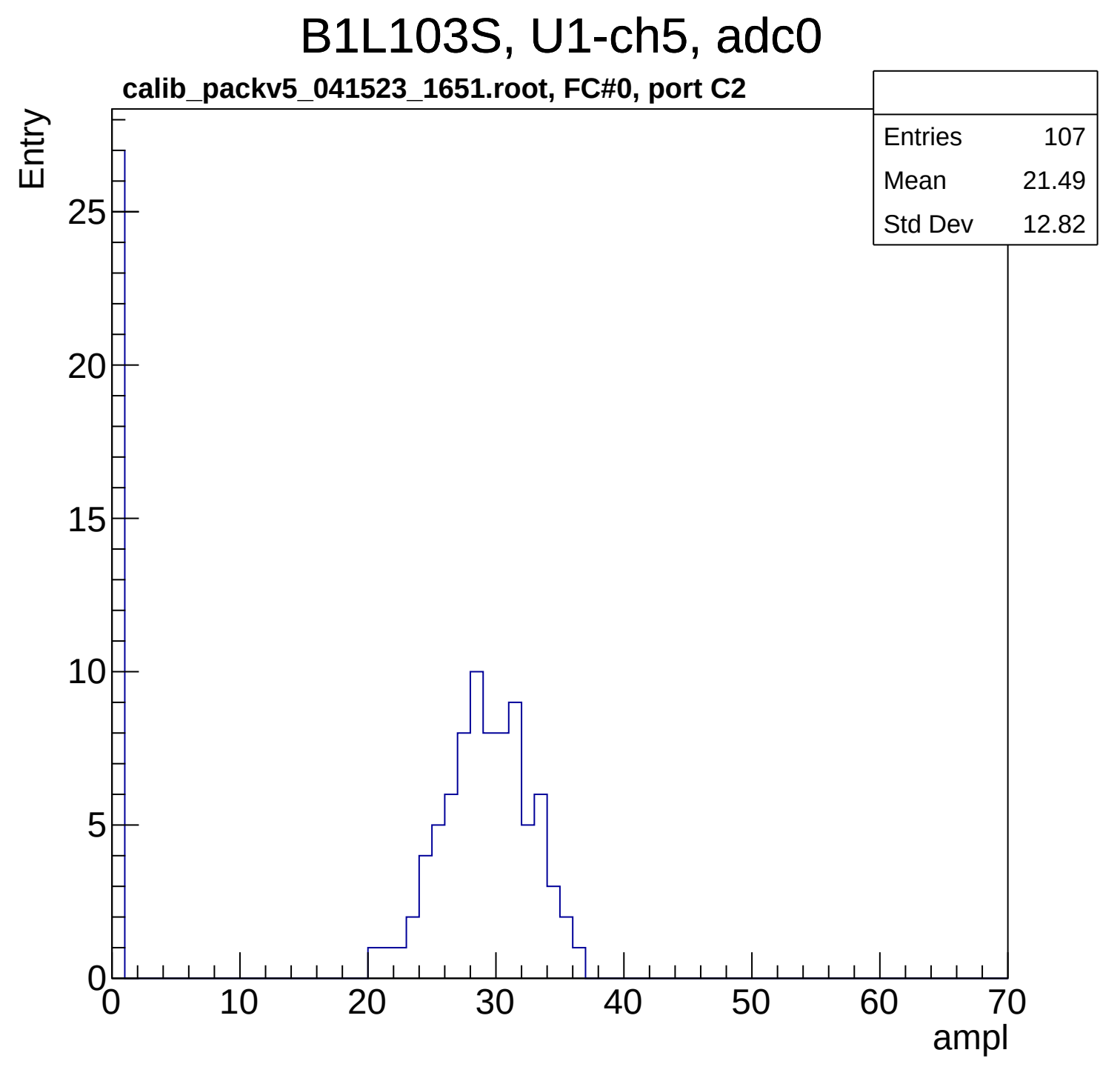
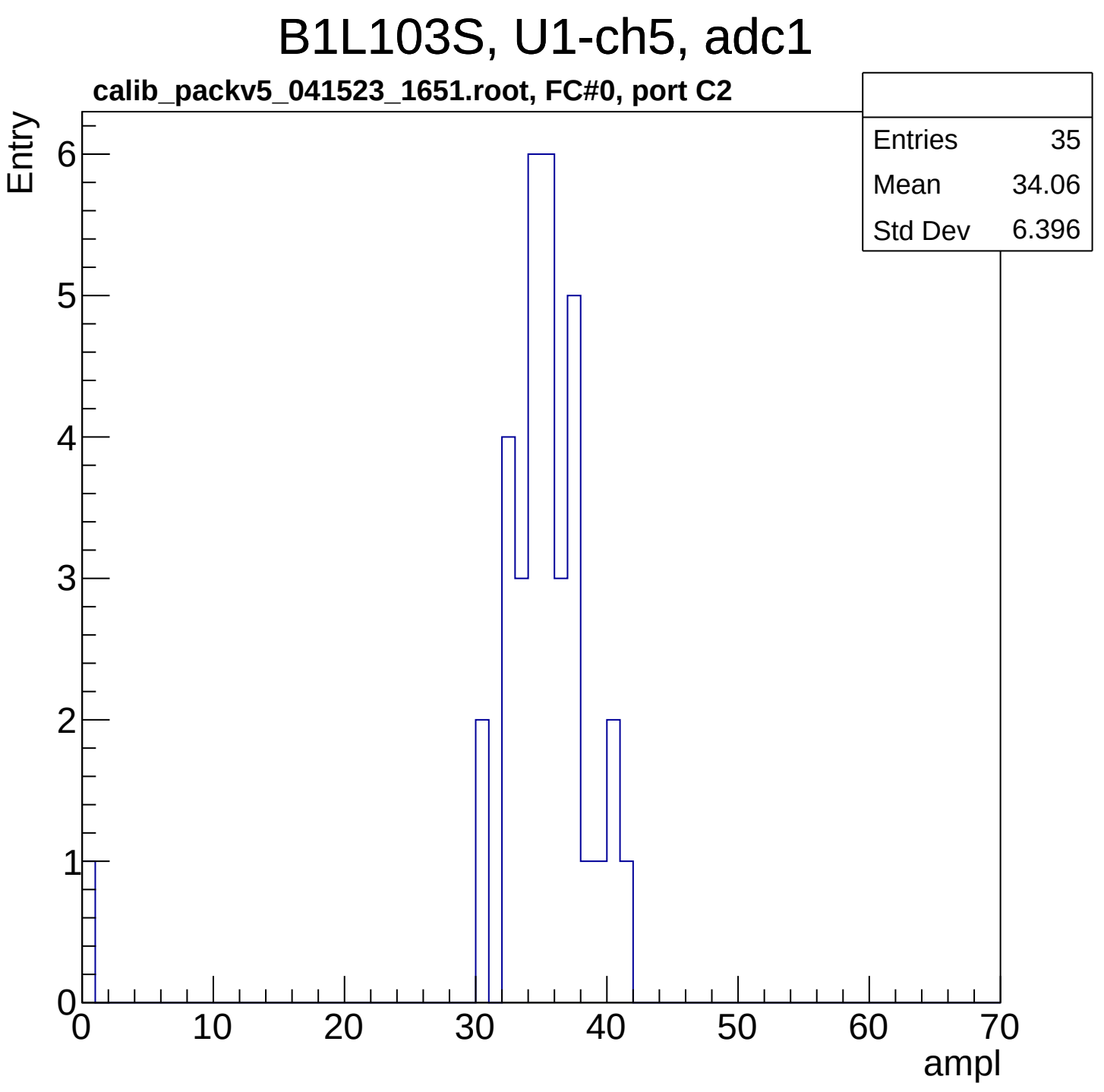
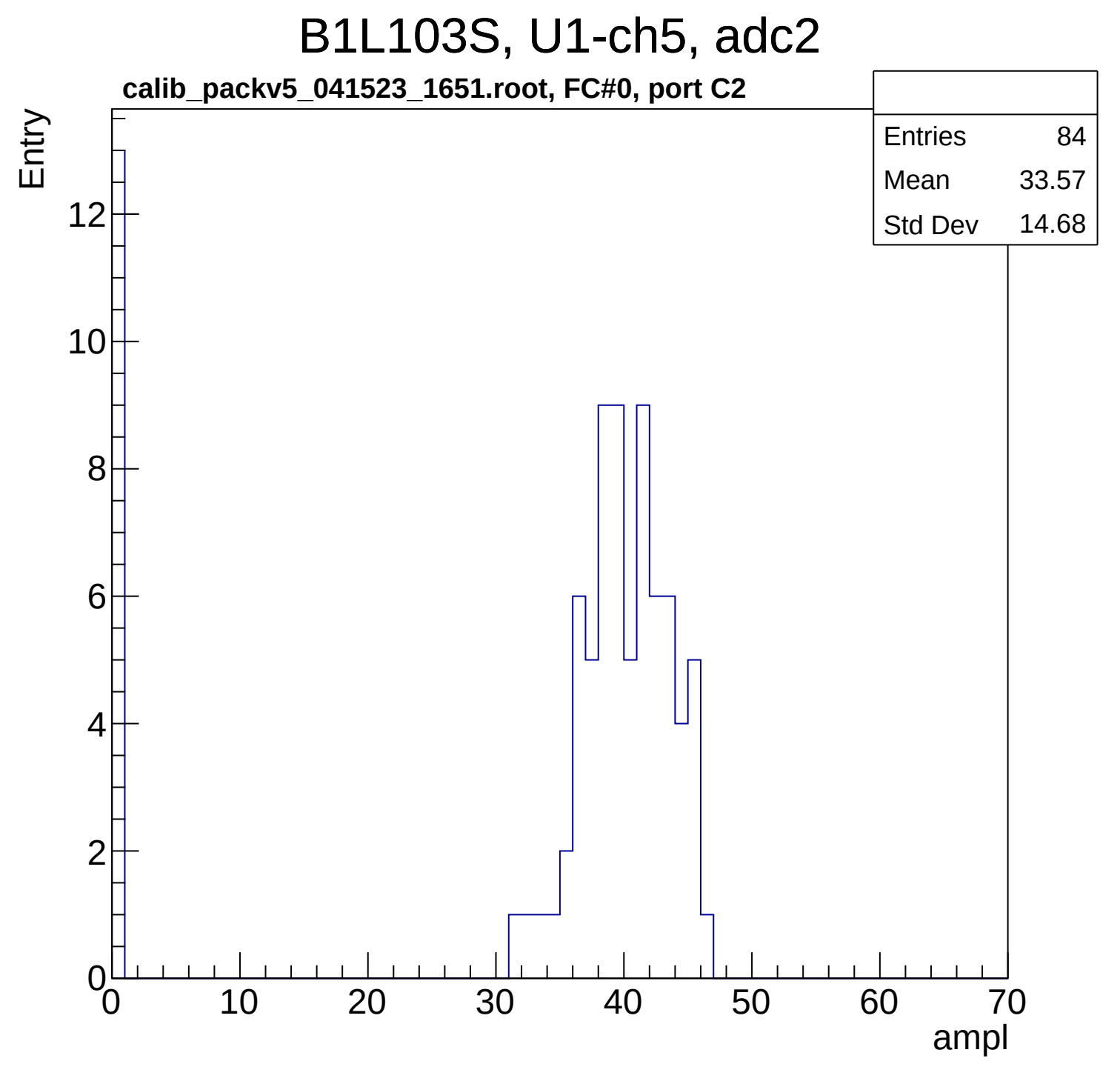

B1L103S, U1-ch4, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 61.32
Std Dev 1.624
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U1-ch4, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 5.952
Std Dev 18.35
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch5, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 107
Mean 21.49
Std Dev 12.82
Entry
0
5
10
15
20
25
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch5, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 35
Mean 34.06
Std Dev 6.396
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch5, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 33.57
Std Dev 14.68
Entry
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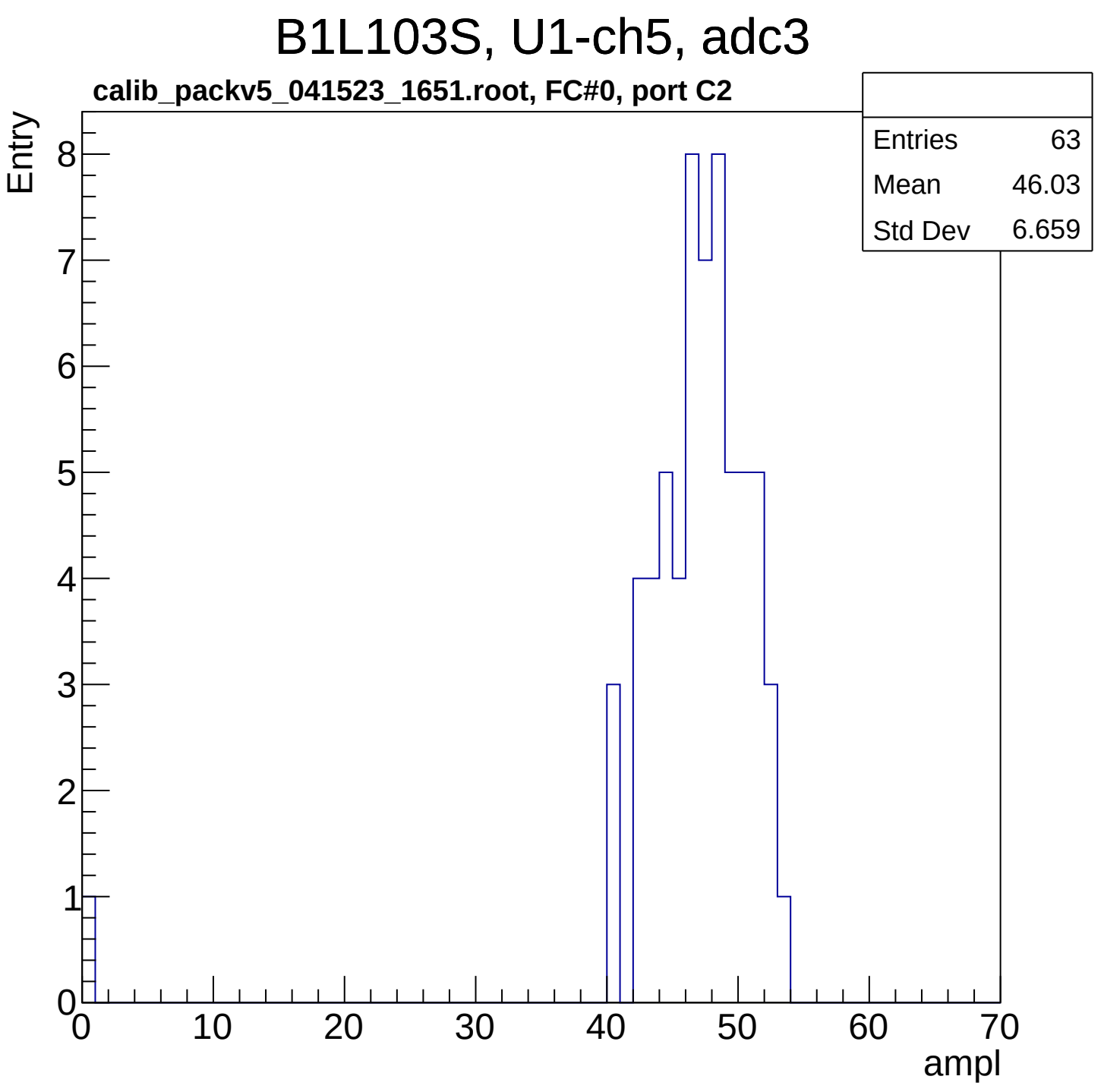
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch5, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 46.03
Std Dev 6.659
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
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40
50
60
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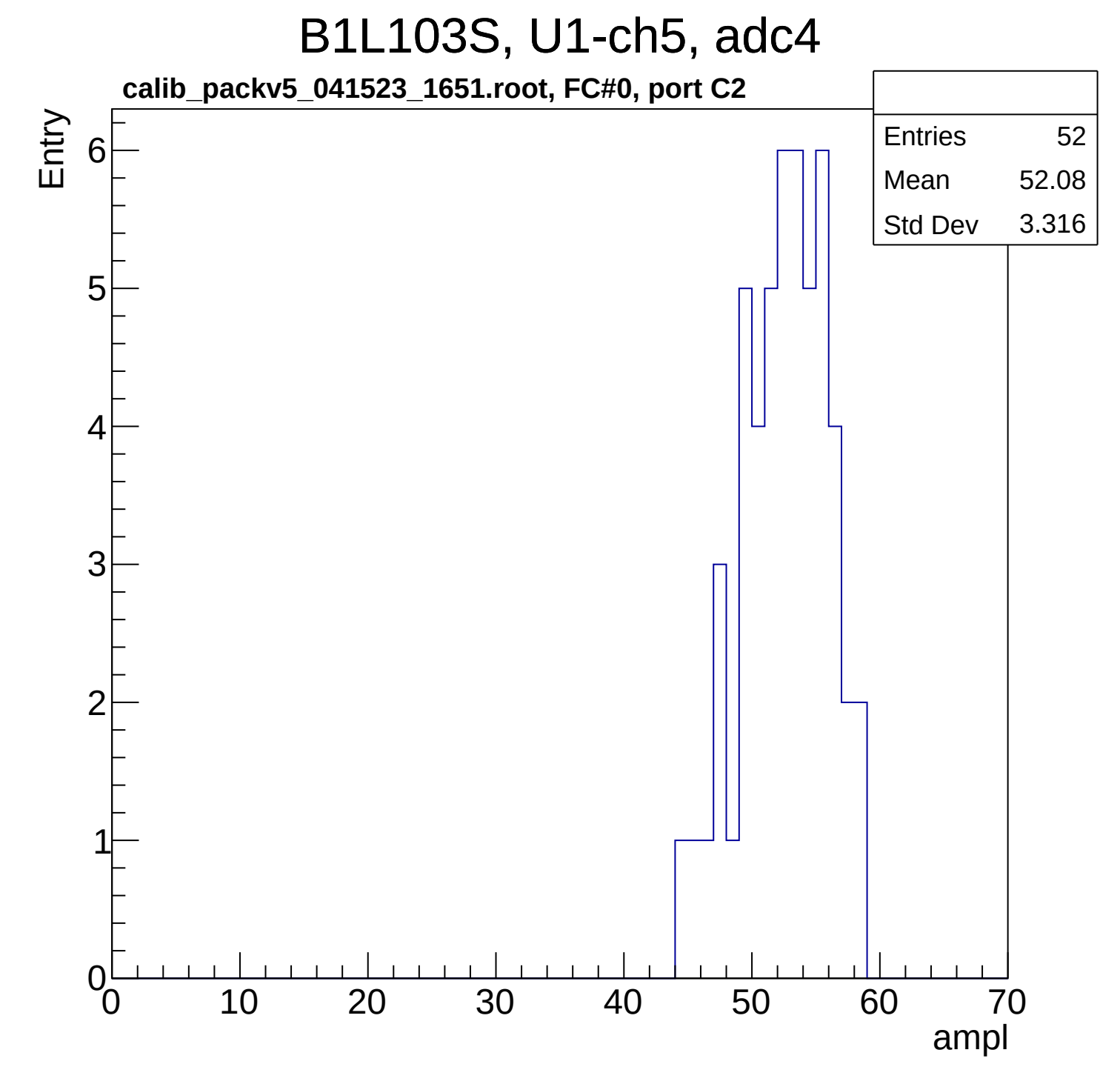
B1L103S, U1-ch5, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 52.08
Std Dev 3.316
Entry
ampl
0
1
2
3
4
5
6
0
10
20
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40
50
60
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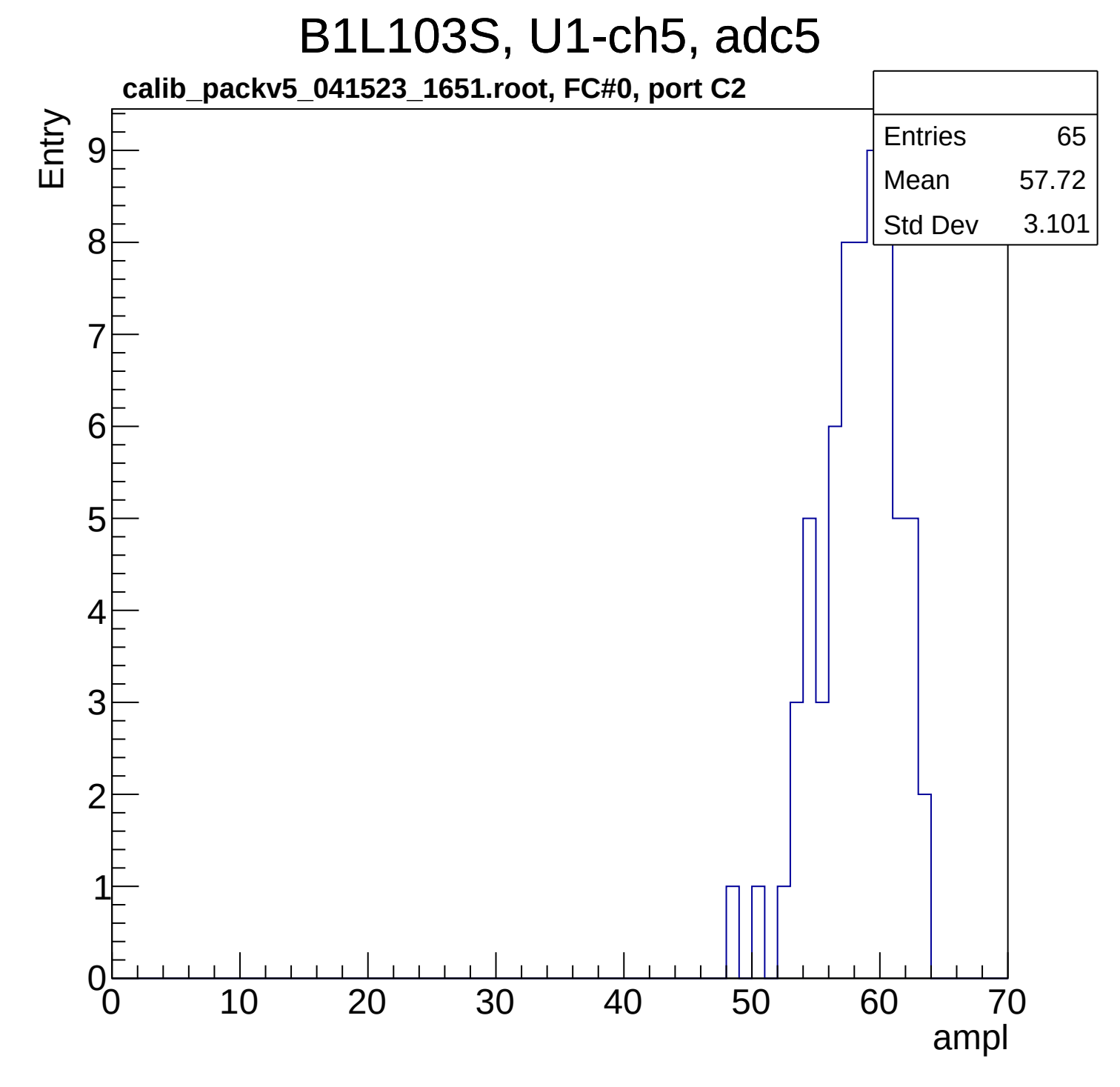
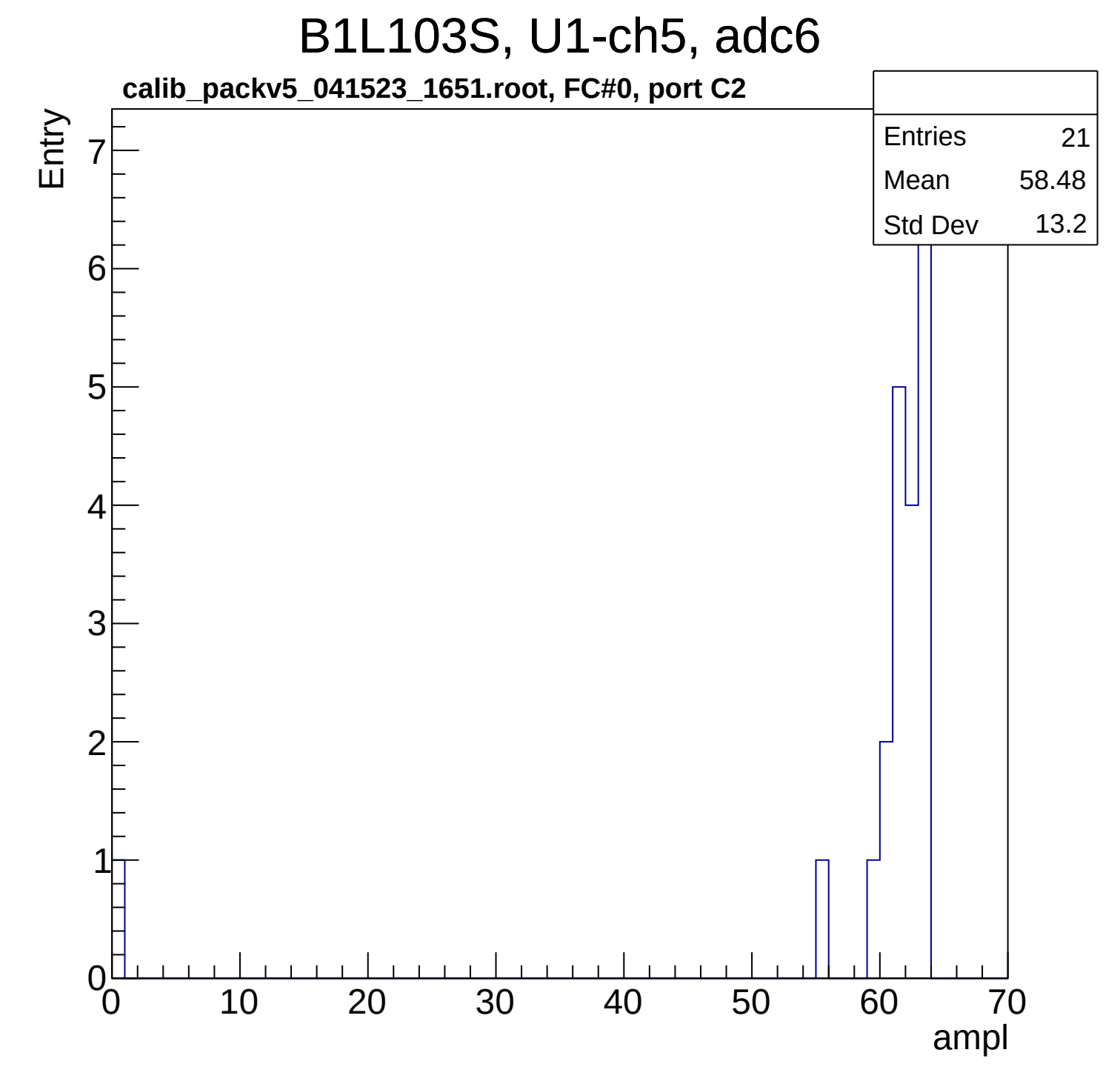

B1L103S, U1-ch5, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 57.72
Std Dev 3.101
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U1-ch5, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 58.48
Std Dev 13.2
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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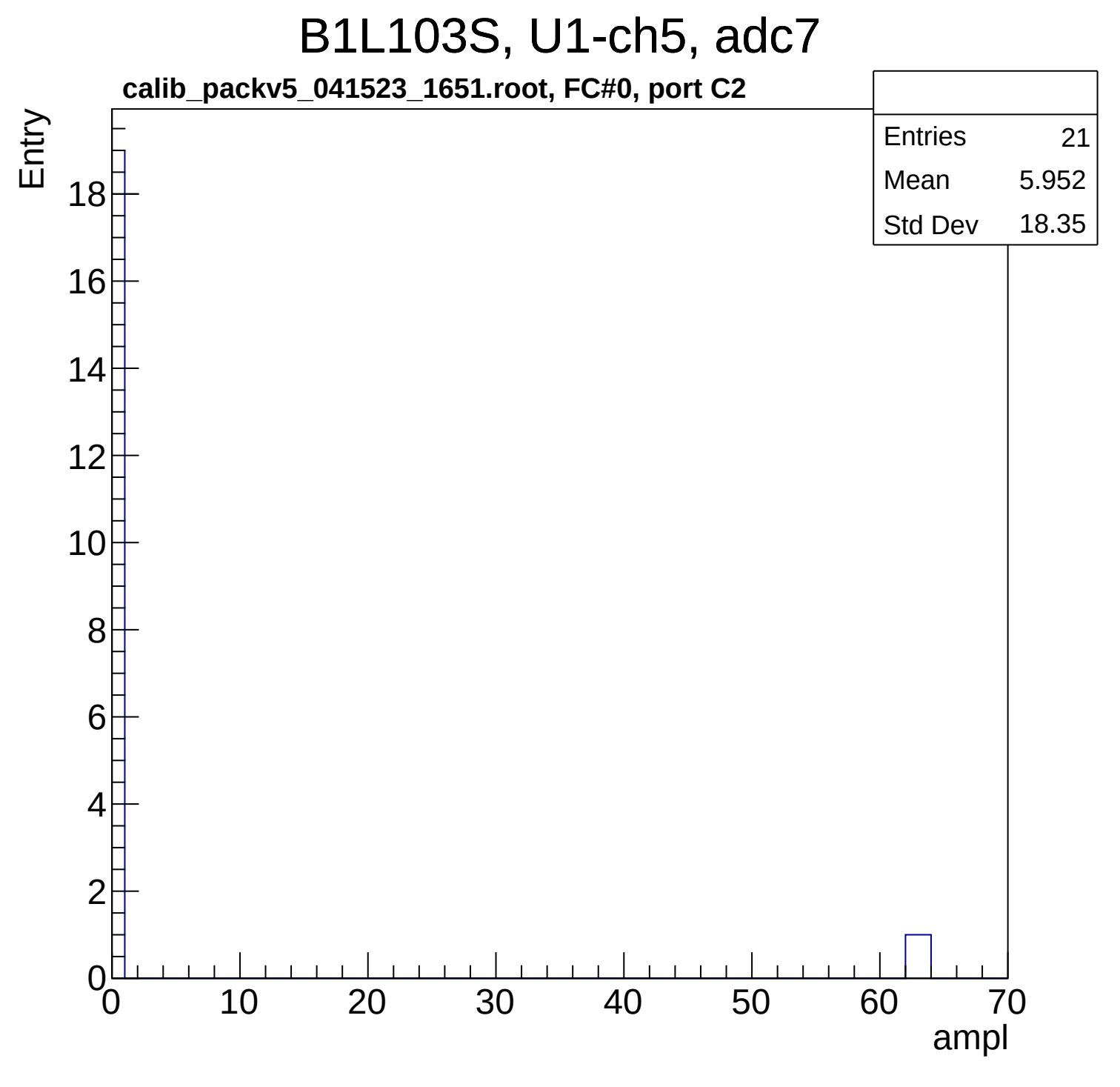
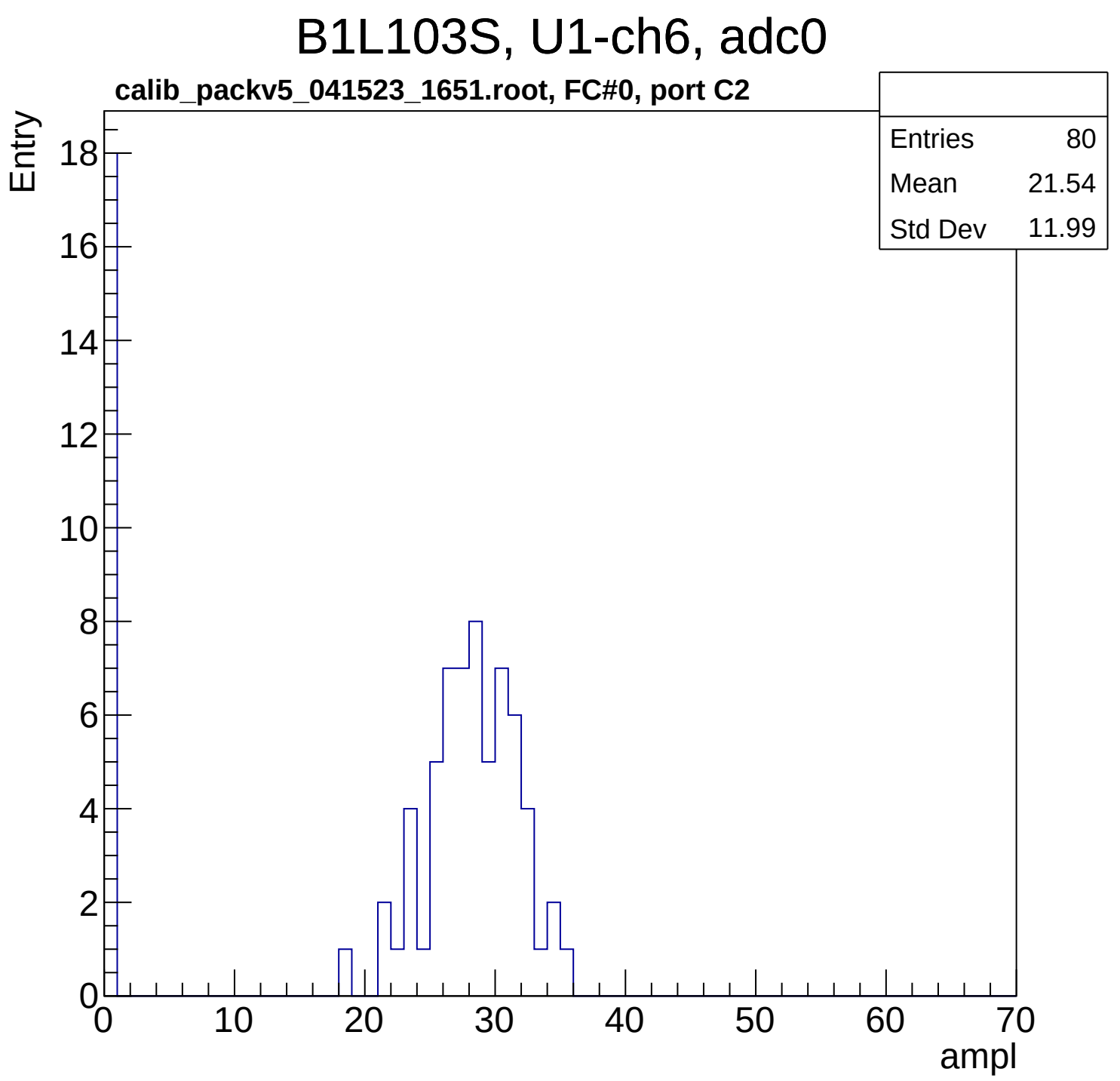

B1L103S, U1-ch5, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 5.952
Std Dev 18.35
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch6, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 21.54
Std Dev 11.99
Entry
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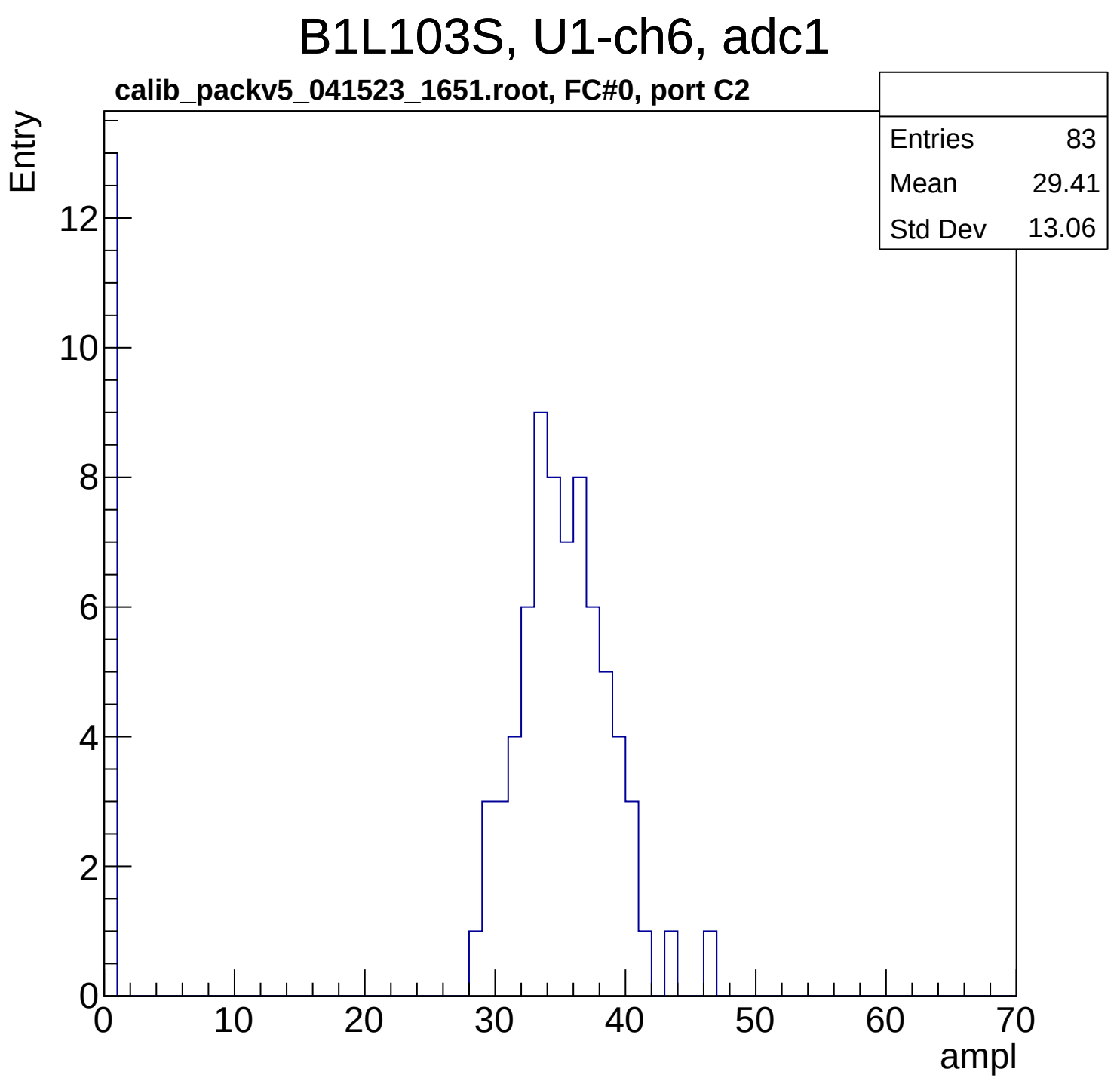
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch6, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 29.41
Std Dev 13.06
Entry
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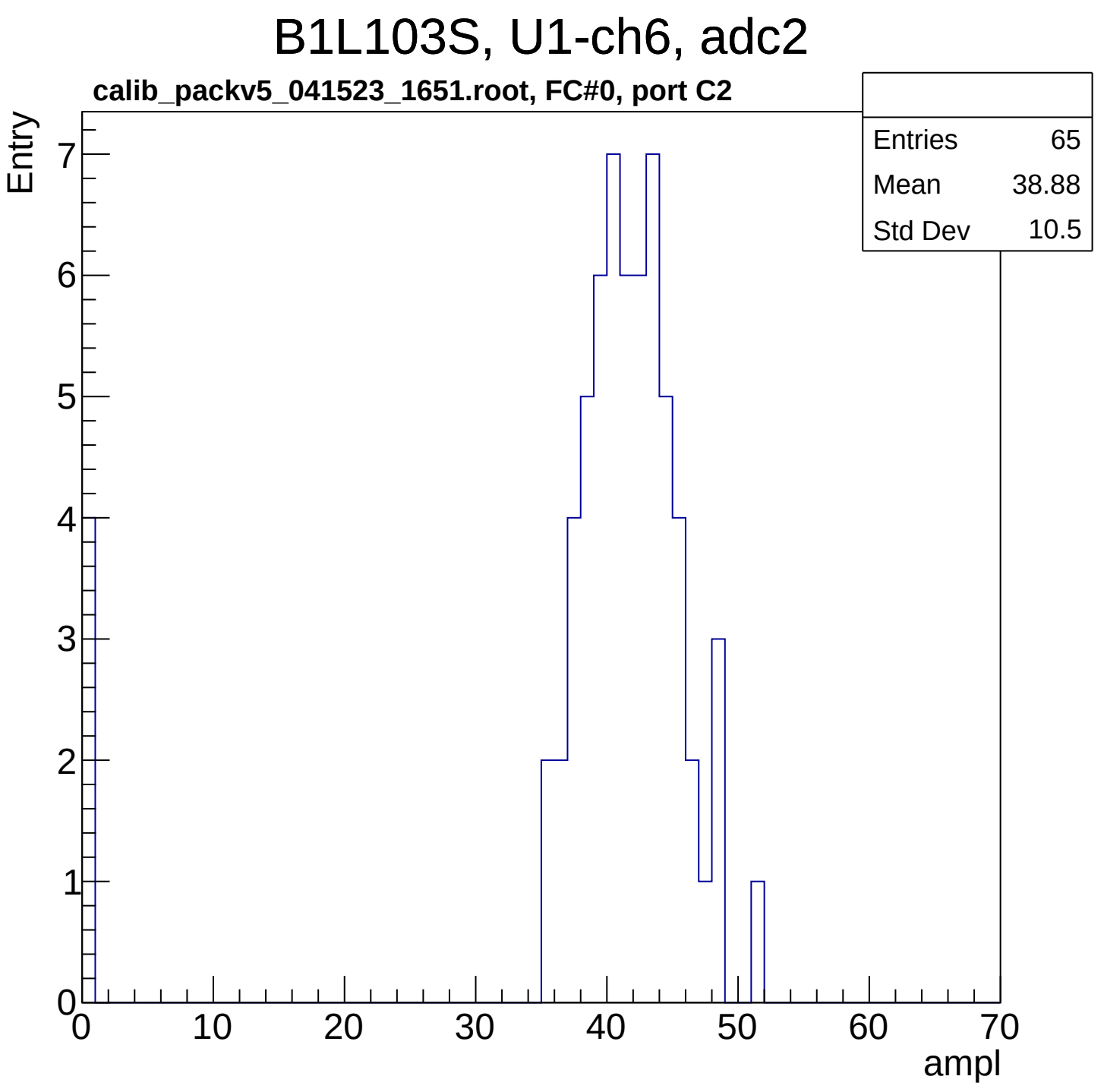
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch6, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 38.88
Std Dev 10.5
Entry
ampl
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1
2
3
4
5
6
7
0
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20
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40
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60
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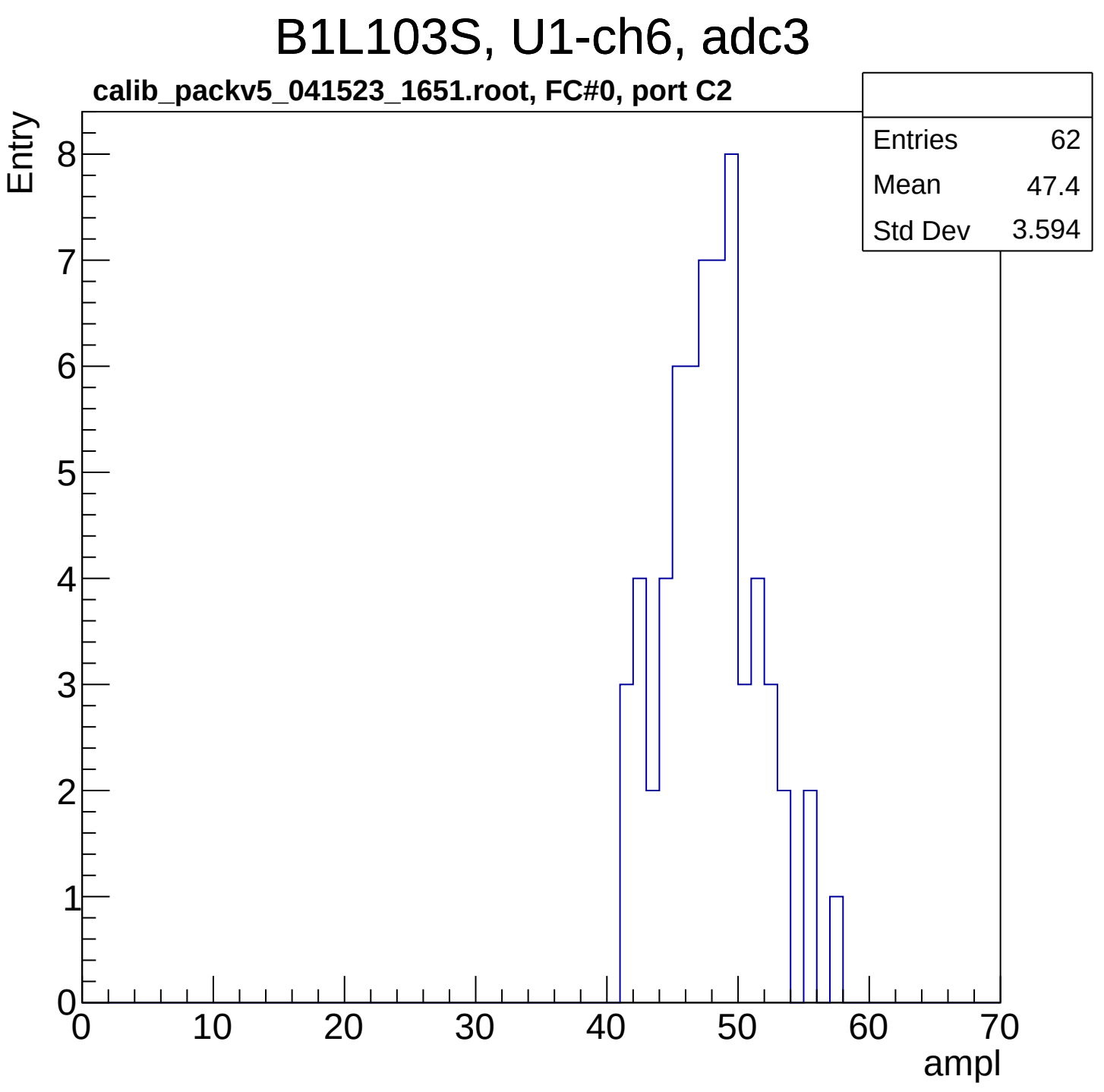
B1L103S, U1-ch6, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 47.4
Std Dev 3.594
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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40
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60
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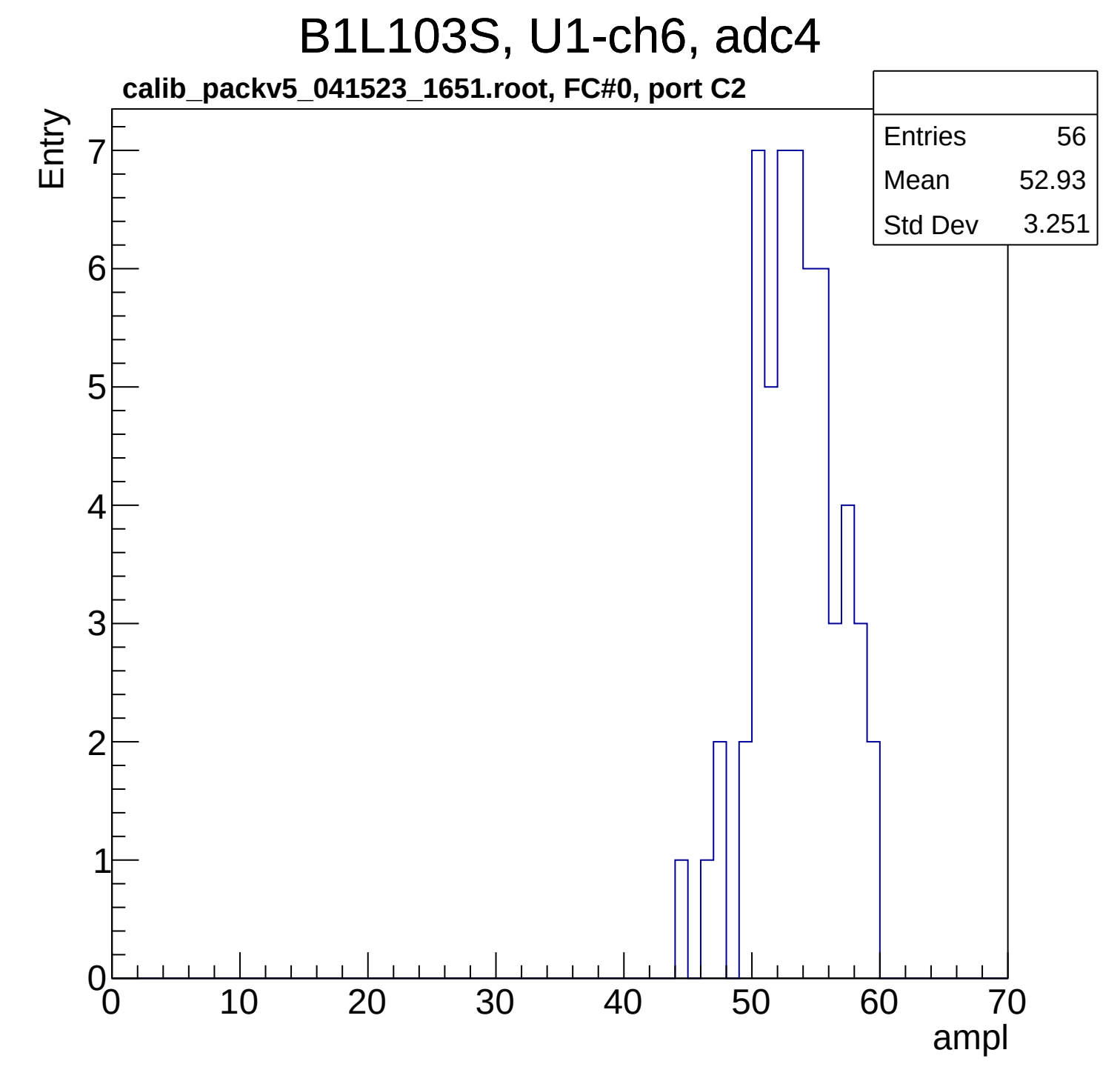
B1L103S, U1-ch6, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 52.93
Std Dev 3.251
Entry
ampl
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3
4
5
6
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0
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60
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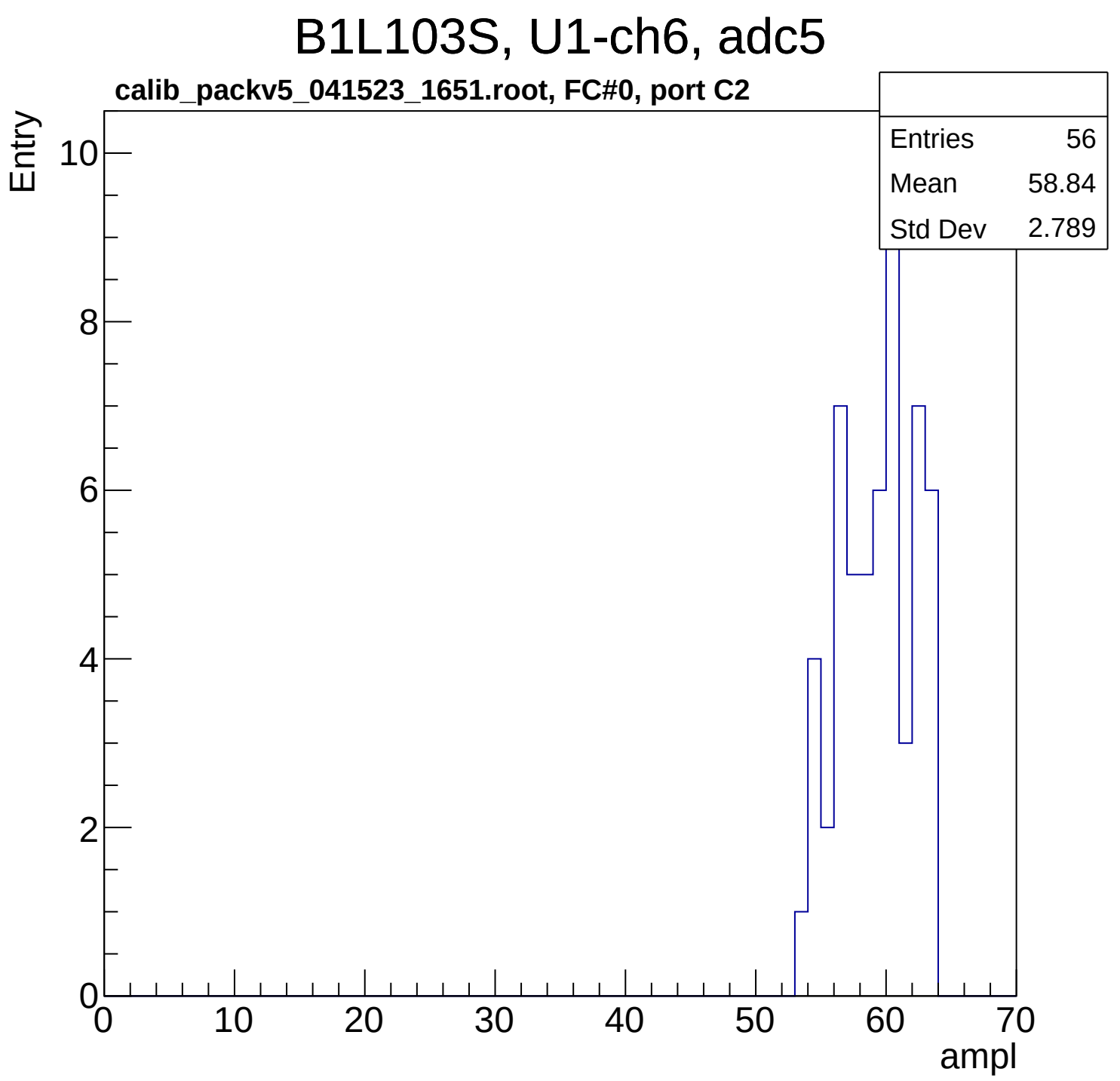
B1L103S, U1-ch6, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 58.84
Std Dev 2.789
Entry
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2
4
6
8
10
0
10
20
30
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50
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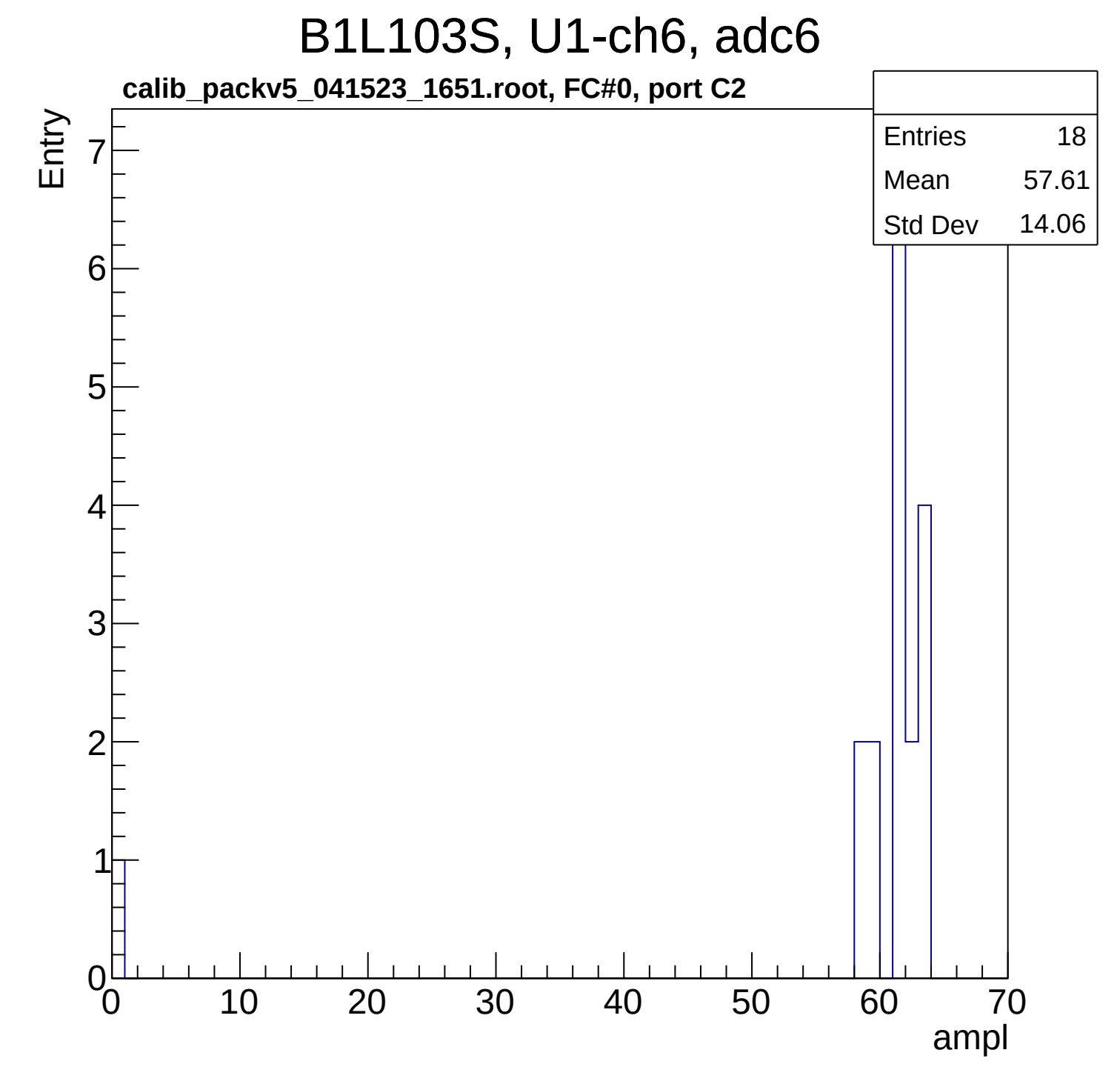
70
ampl


B1L103S, U1-ch6, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 57.61
Std Dev 14.06
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
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40
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60
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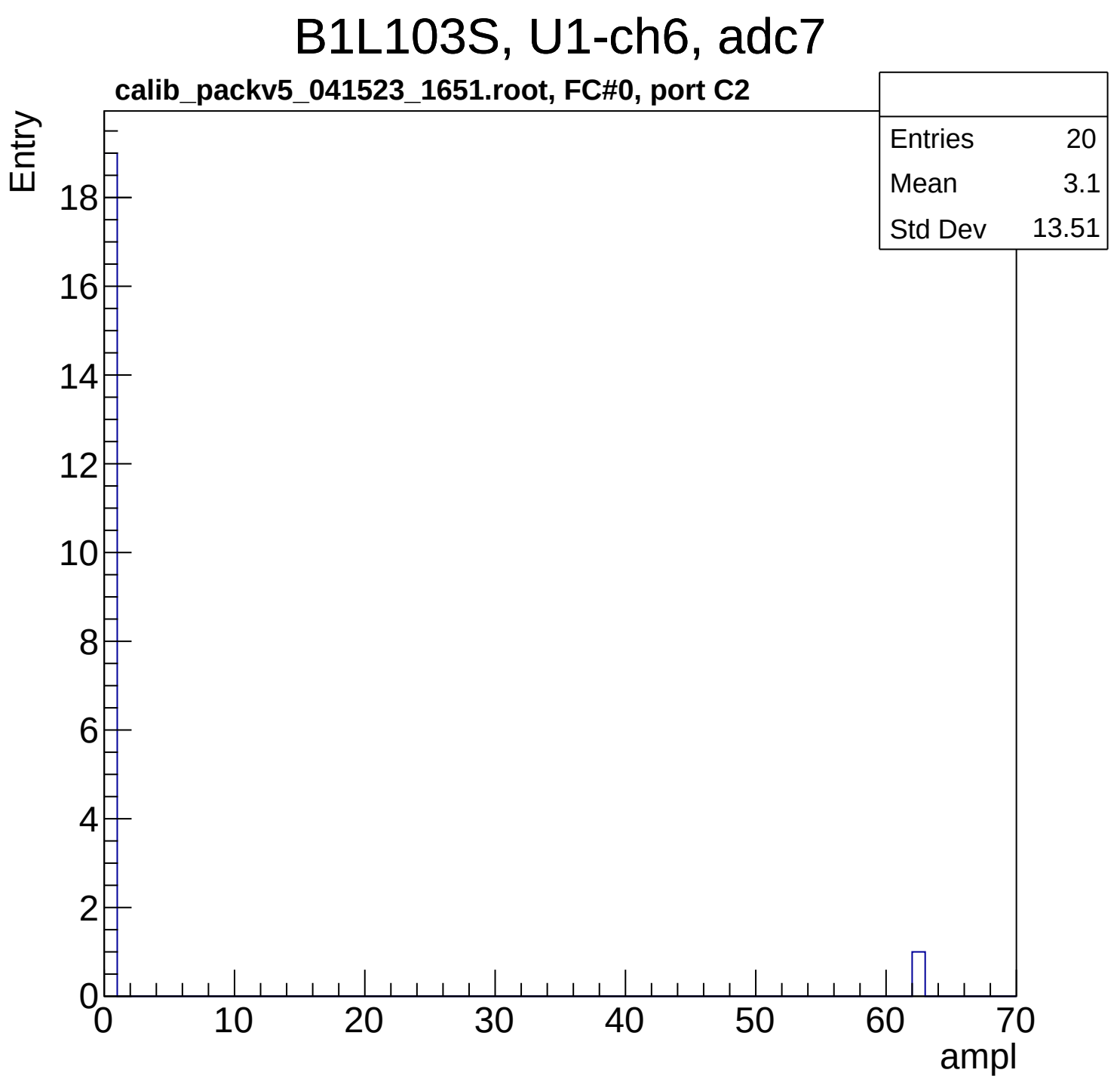
B1L103S, U1-ch6, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.1
Std Dev 13.51
Entry
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6
8
10
12
14
16
18
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10
20
30
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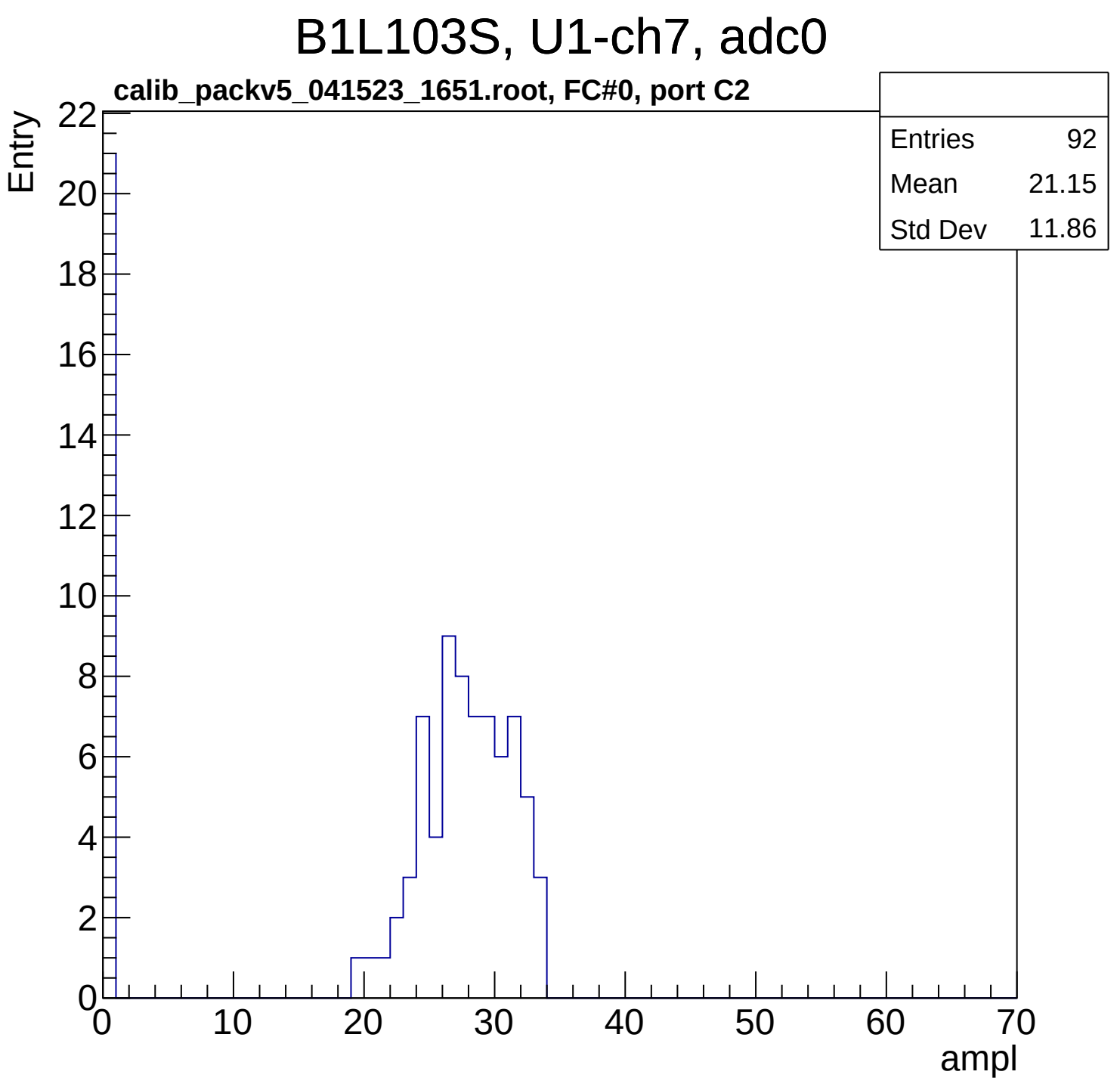
70
ampl


B1L103S, U1-ch7, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 92
Mean 21.15
Std Dev 11.86
Entry
ampl
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8
10
12
14
16
18
20
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0
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40
50
60
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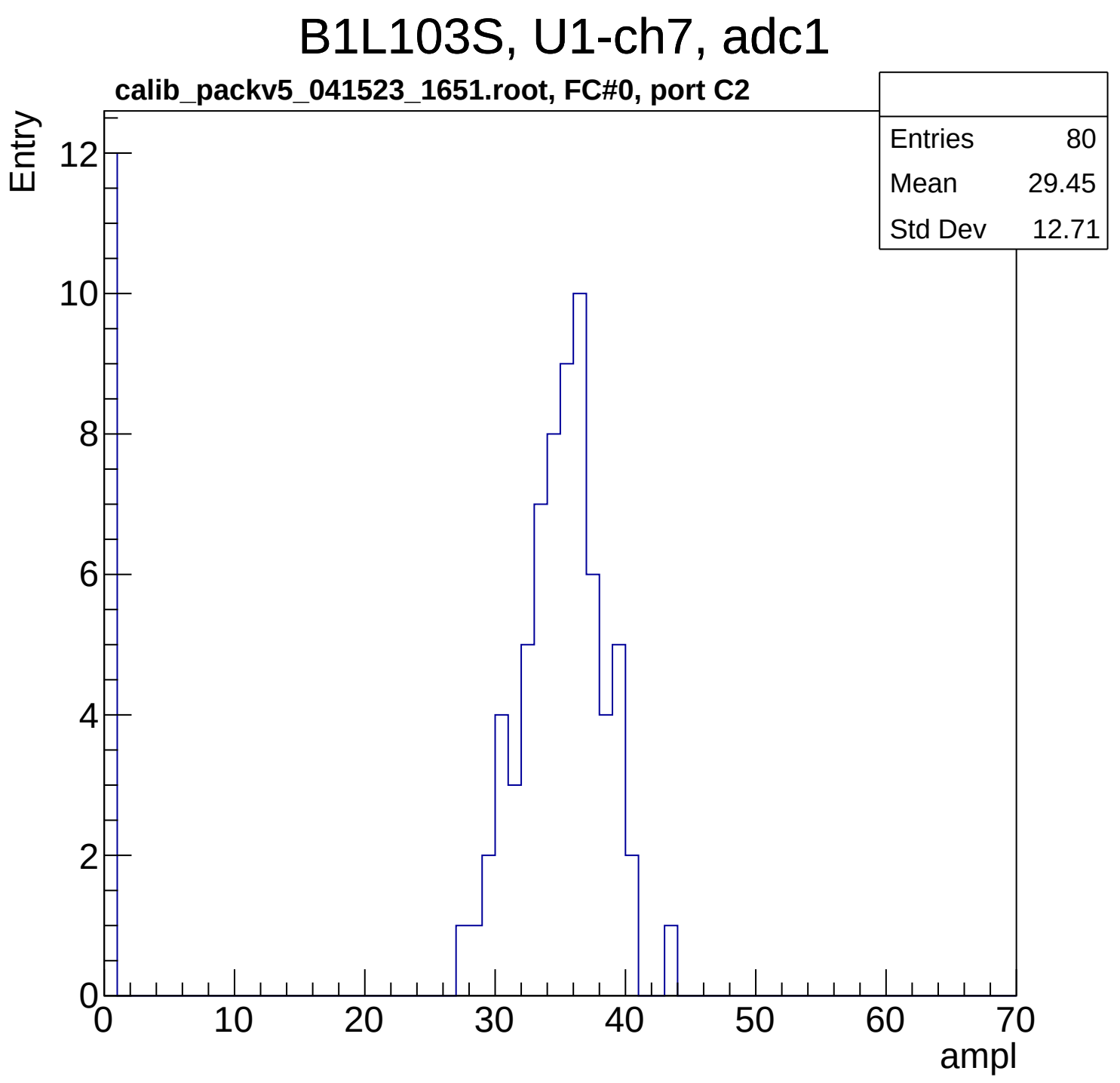
B1L103S, U1-ch7, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 29.45
Std Dev 12.71
Entry
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8
10
12
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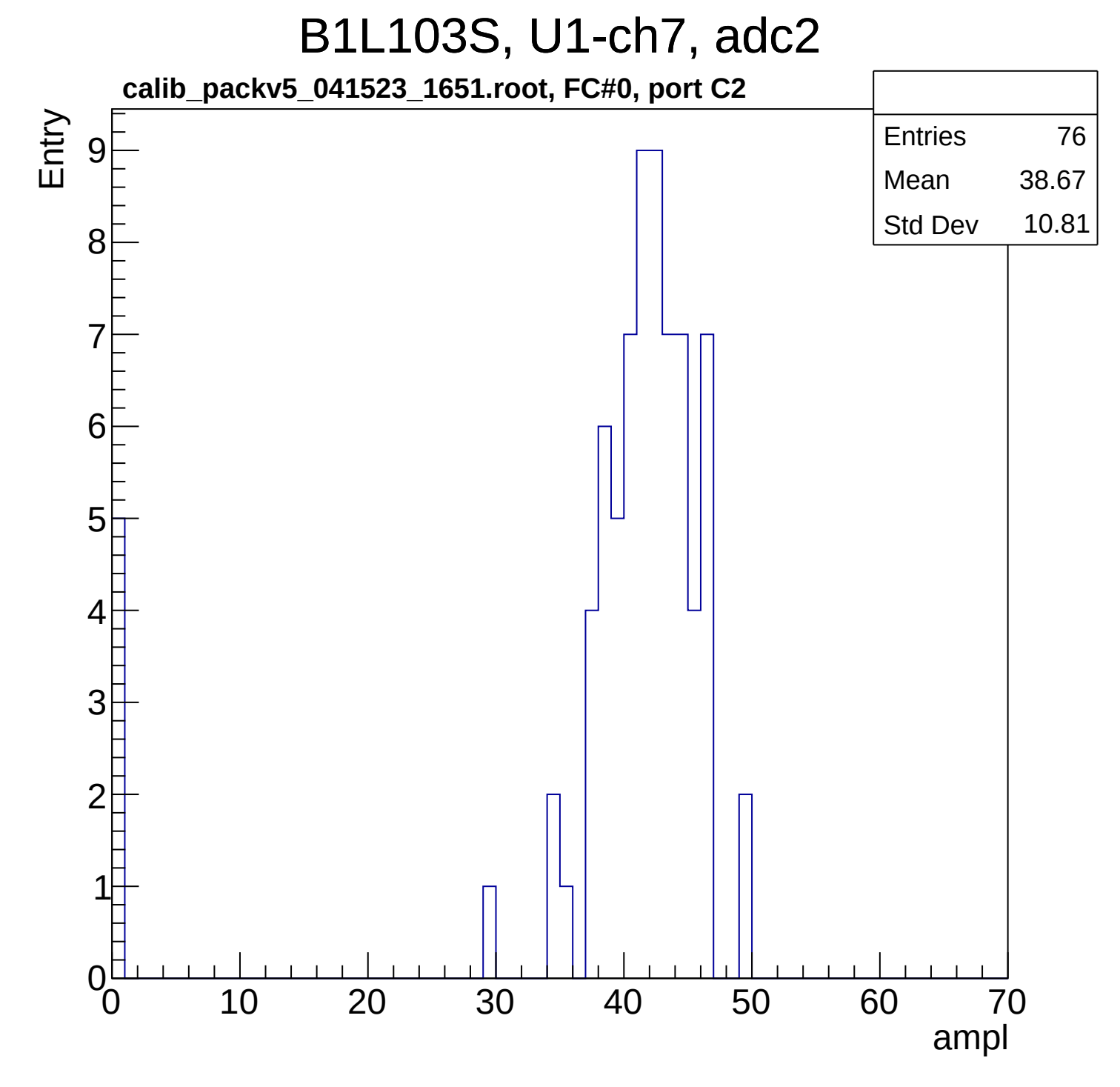
70
ampl


B1L103S, U1-ch7, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 38.67
Std Dev 10.81
Entry
ampl
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3
4
5
6
7
8
9
0
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40
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60
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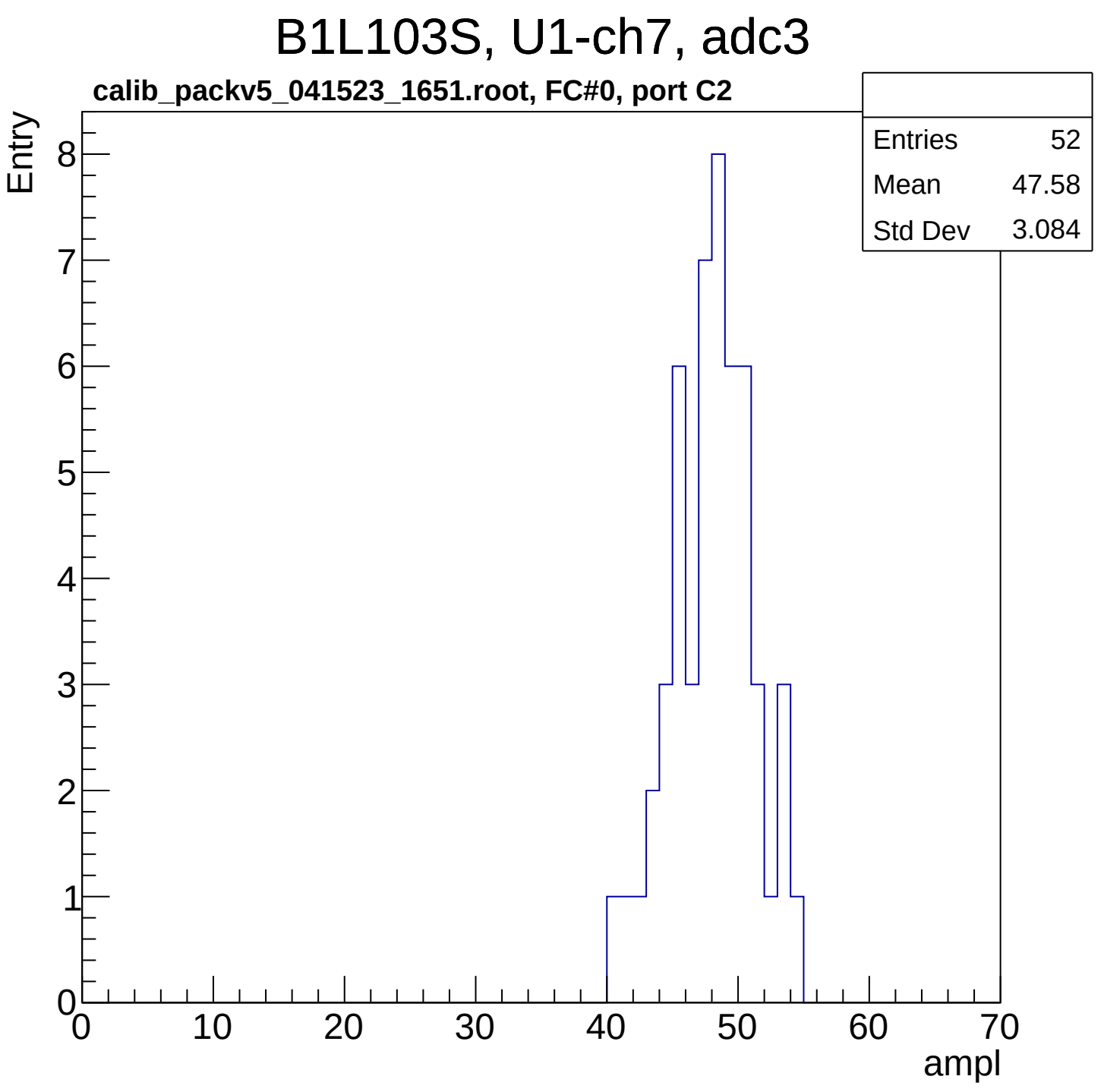
B1L103S, U1-ch7, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 47.58
Std Dev 3.084
Entry
ampl
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2
3
4
5
6
7
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0
10
20
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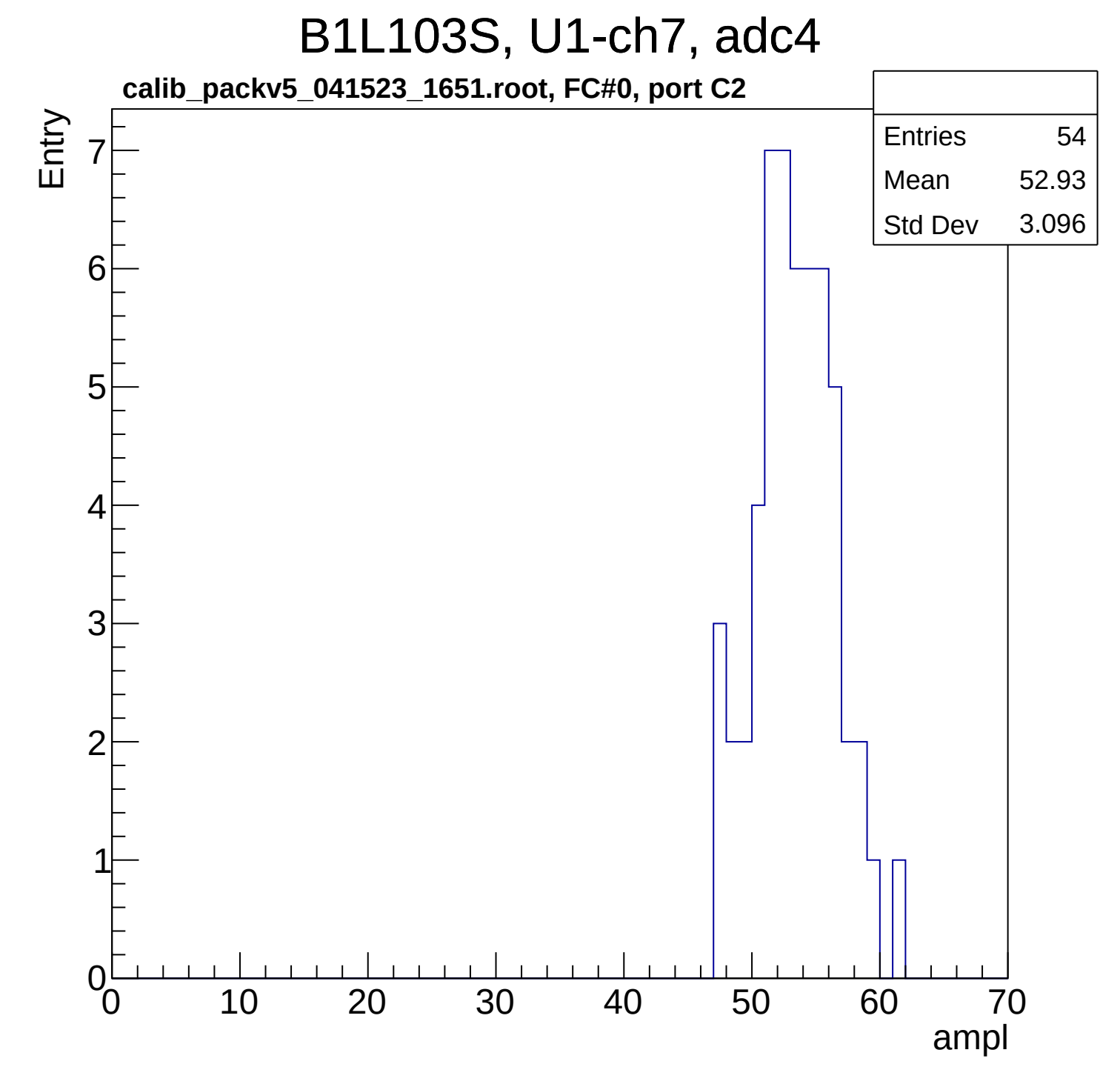
40
50
60
70


B1L103S, U1-ch7, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 52.93
Std Dev 3.096
Entry
ampl
0
1
2
3
4
5
6
7
0
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40
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60
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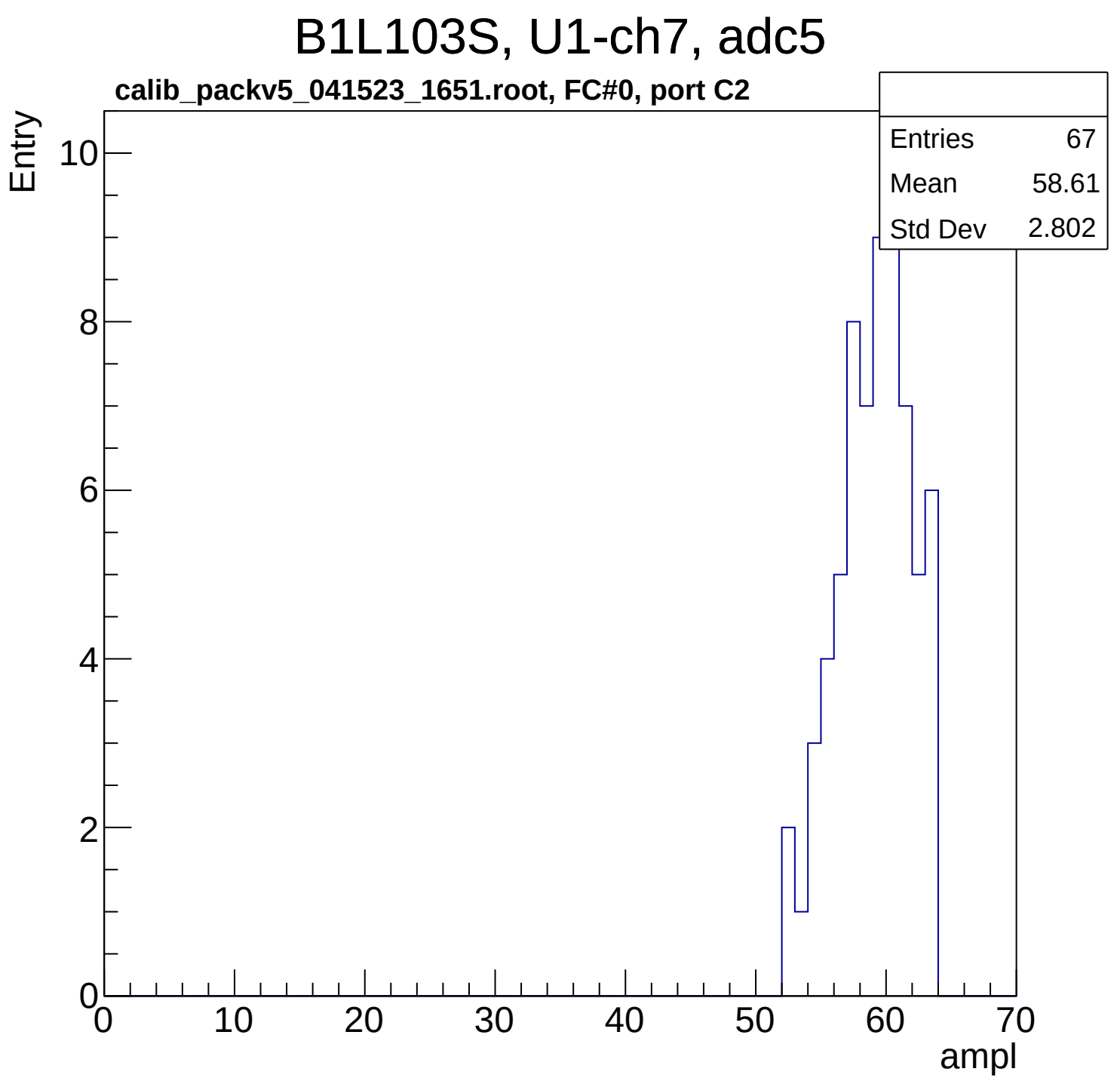
B1L103S, U1-ch7, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 58.61
Std Dev 2.802
Entry
ampl
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2
4
6
8
10
0
10
20
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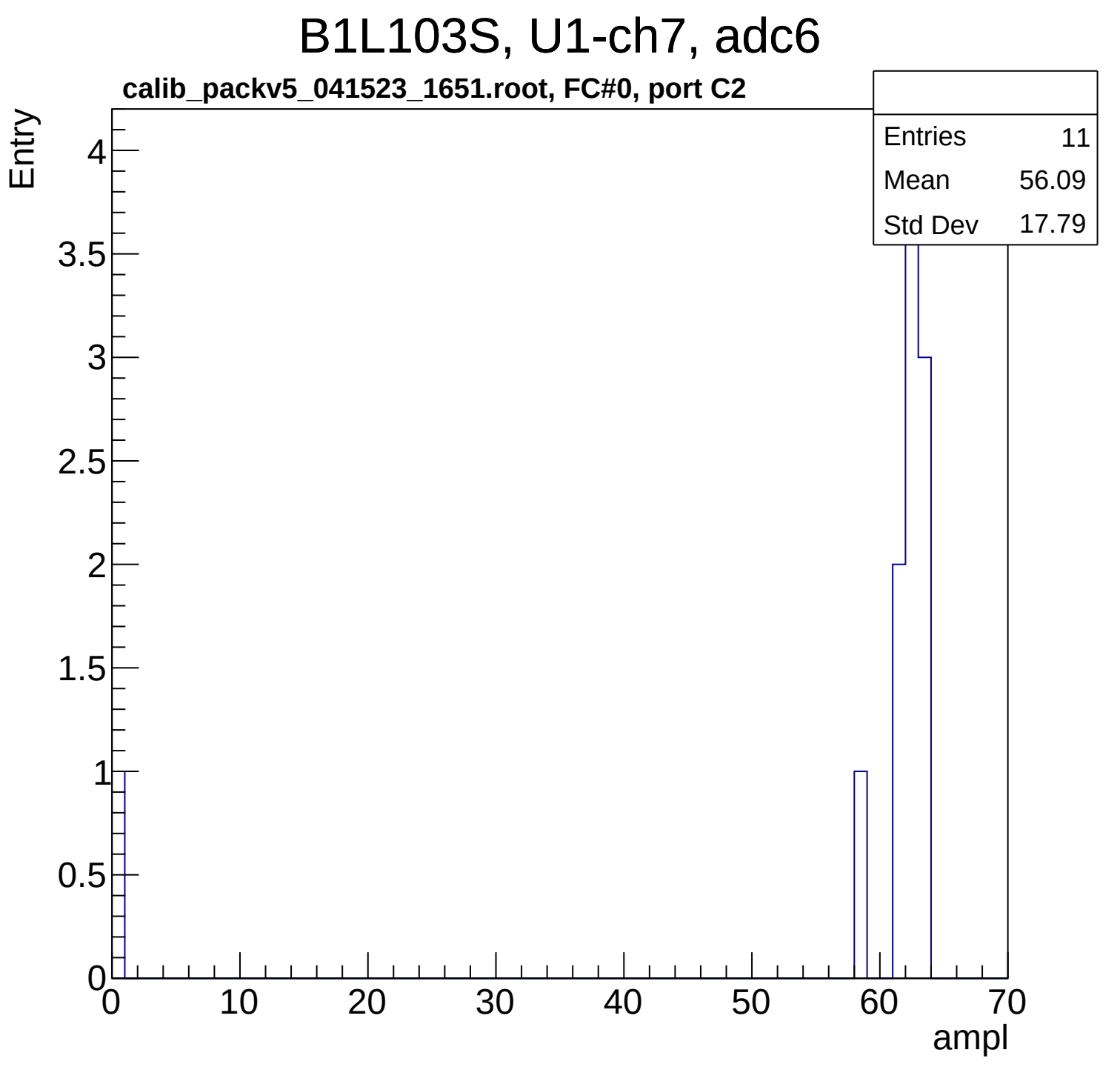
50
60
70


B1L103S, U1-ch7, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 56.09
Std Dev 17.79
Entry
ampl
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1.5
2
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3
3.5
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0
10
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40
50
60
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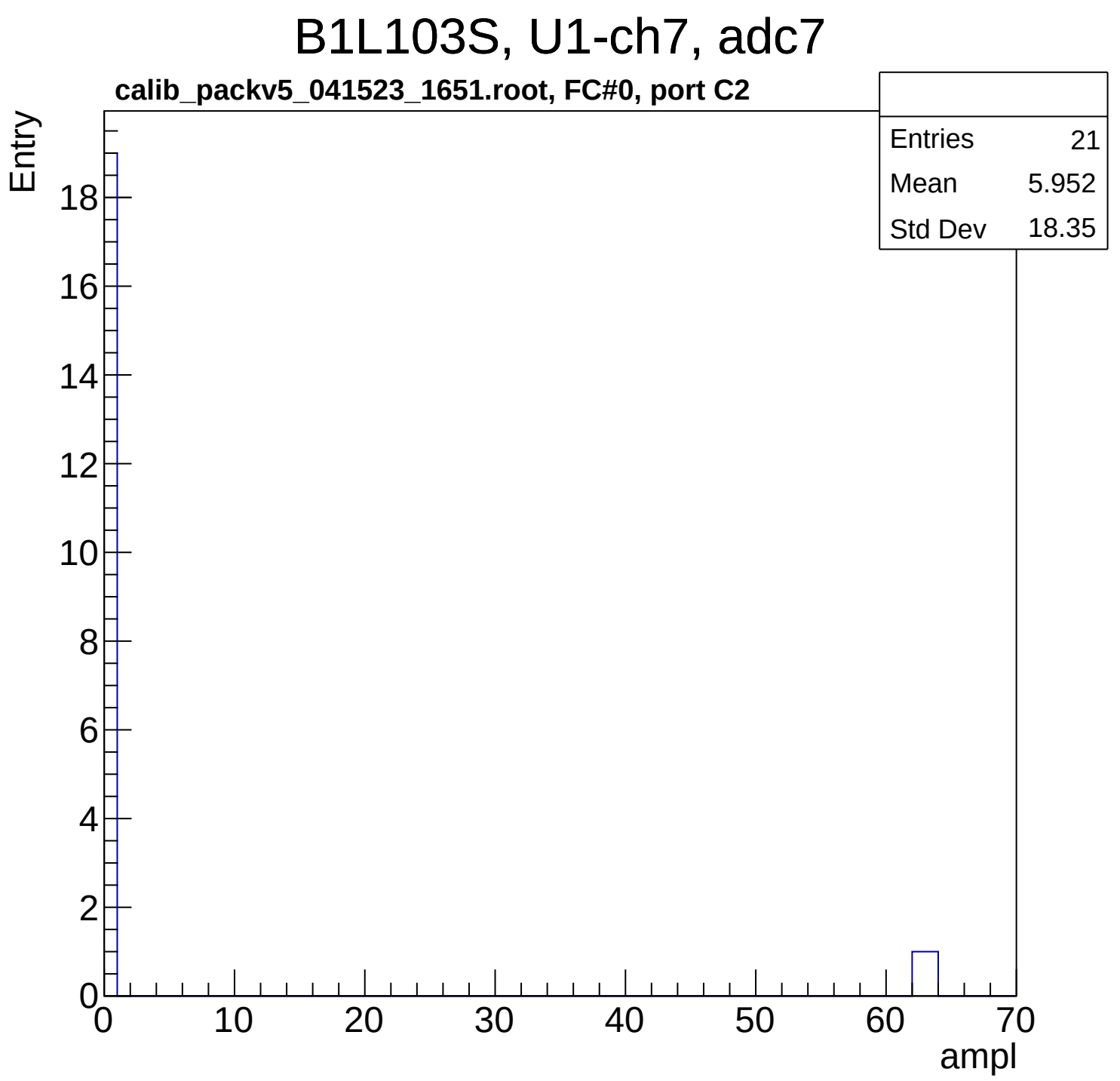
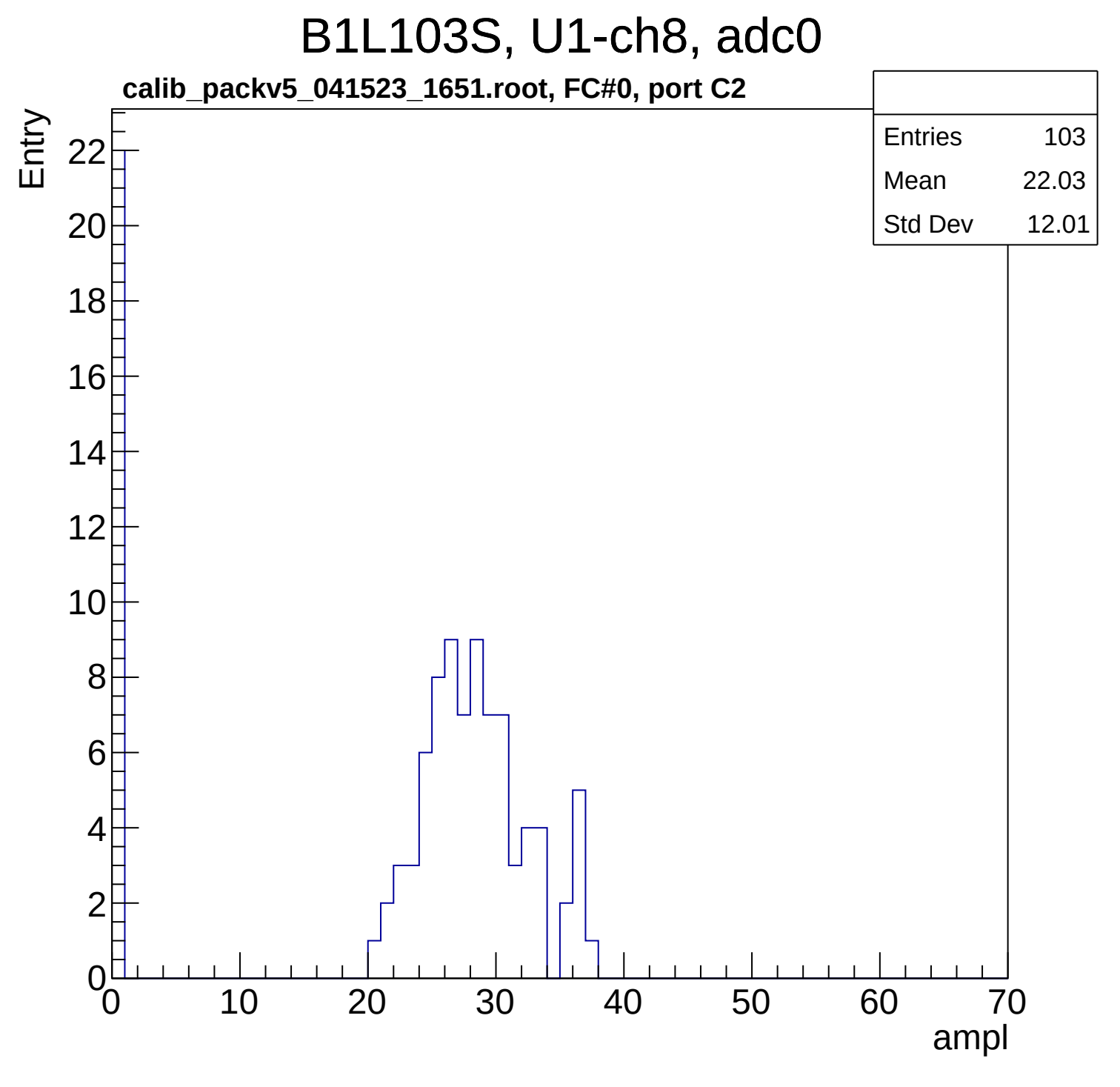

B1L103S, U1-ch7, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 5.952
Std Dev 18.35
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch8, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 103
Mean 22.03
Std Dev 12.01
Entry
ampl
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8
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16
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60
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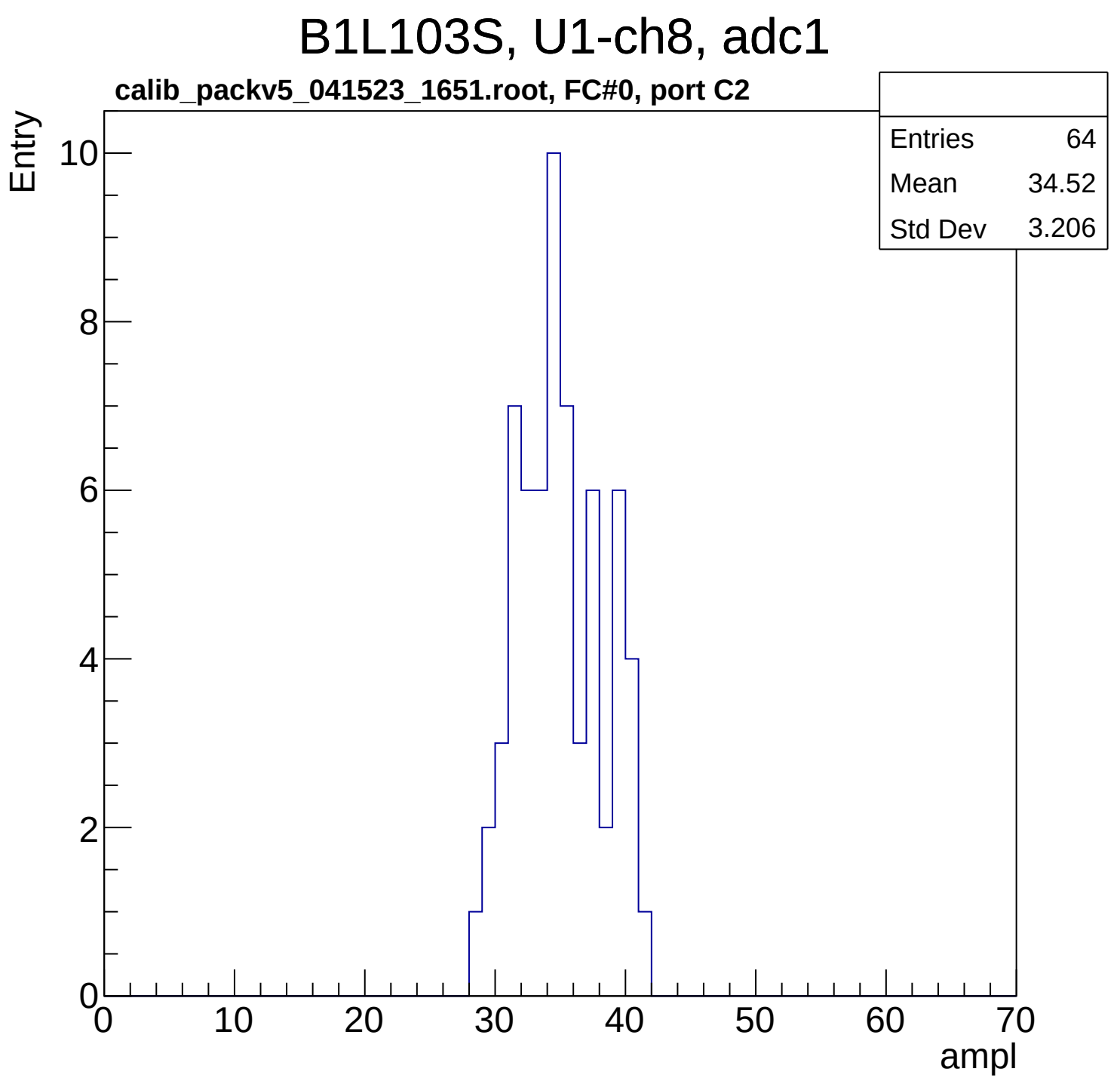
B1L103S, U1-ch8, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 34.52
Std Dev 3.206
Entry
ampl
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0
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40
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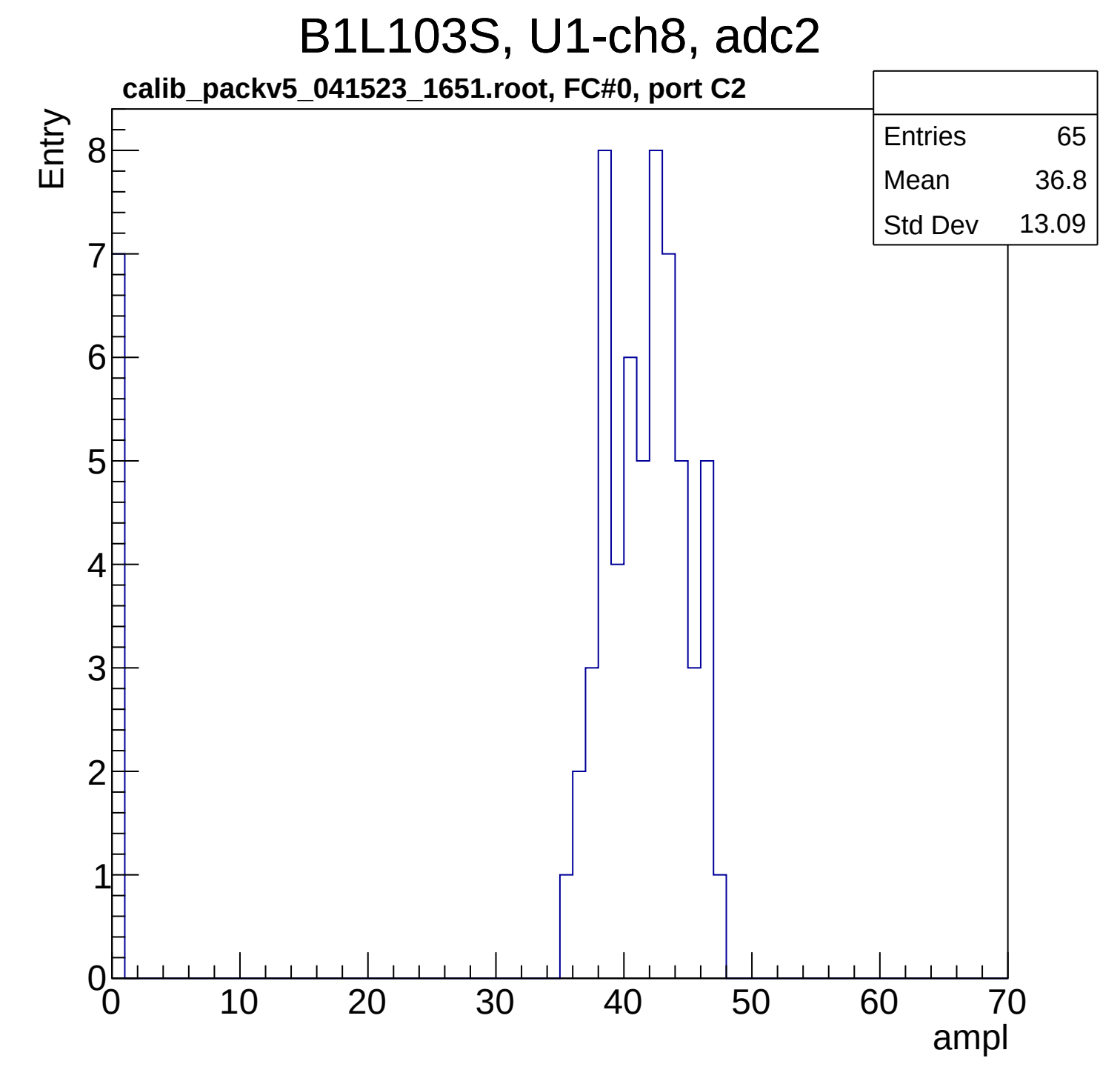
60
70


B1L103S, U1-ch8, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 36.8
Std Dev 13.09
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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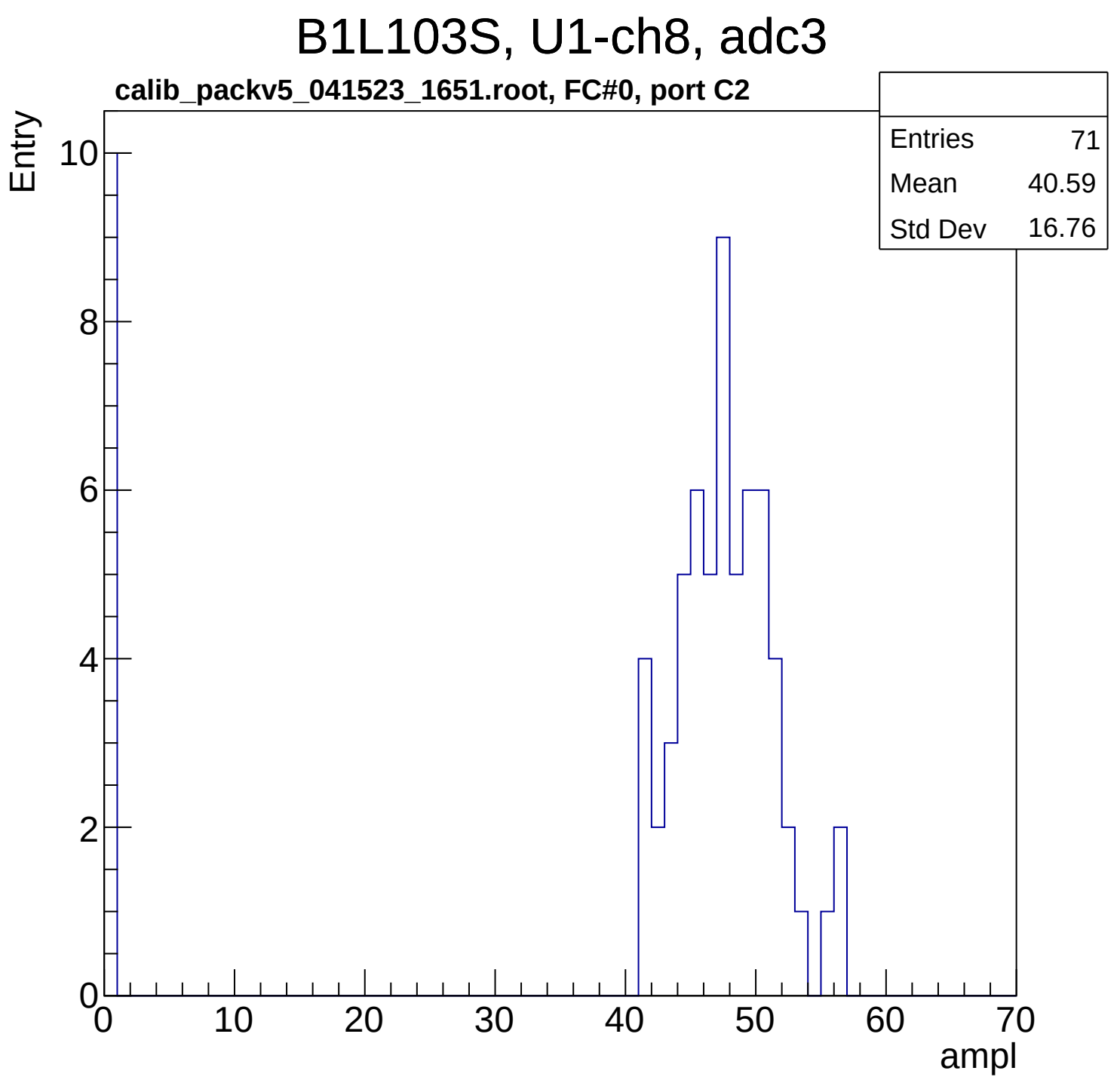
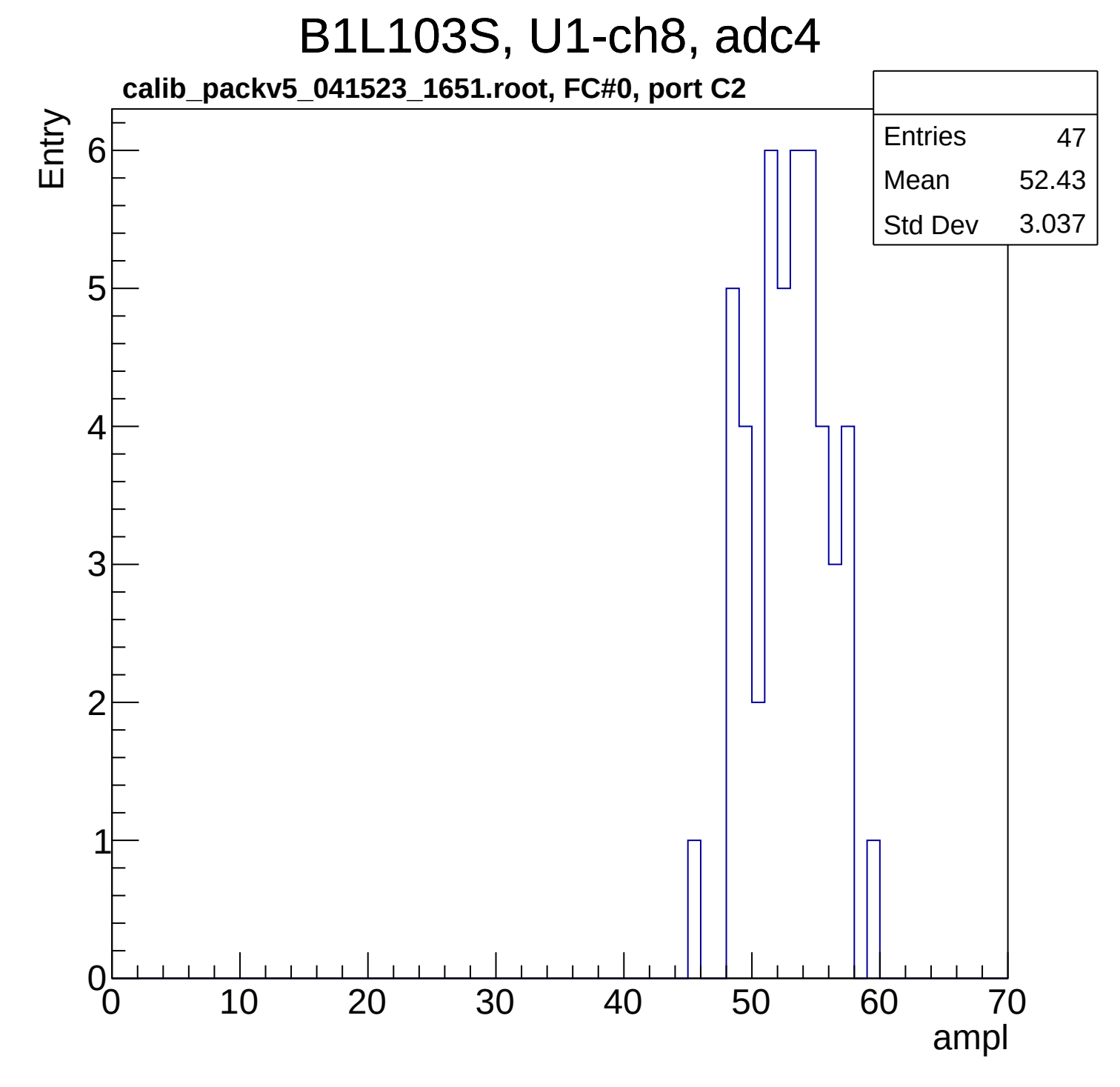

B1L103S, U1-ch8, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 40.59
Std Dev 16.76
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U1-ch8, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 52.43
Std Dev 3.037
Entry
ampl
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1
2
3
4
5
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0
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20
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40
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60
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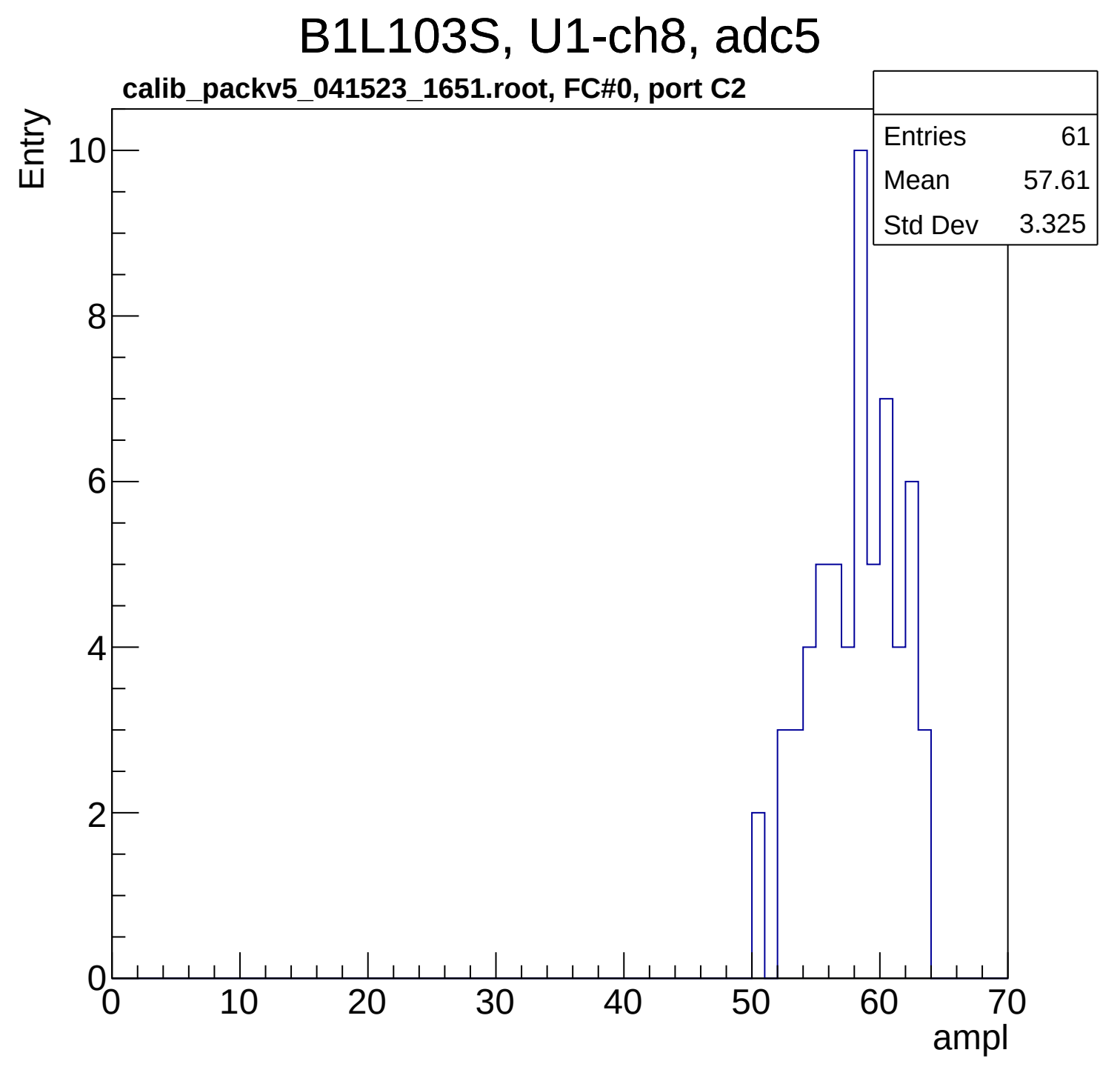
B1L103S, U1-ch8, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 57.61
Std Dev 3.325
Entry
ampl
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4
6
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0
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40
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60
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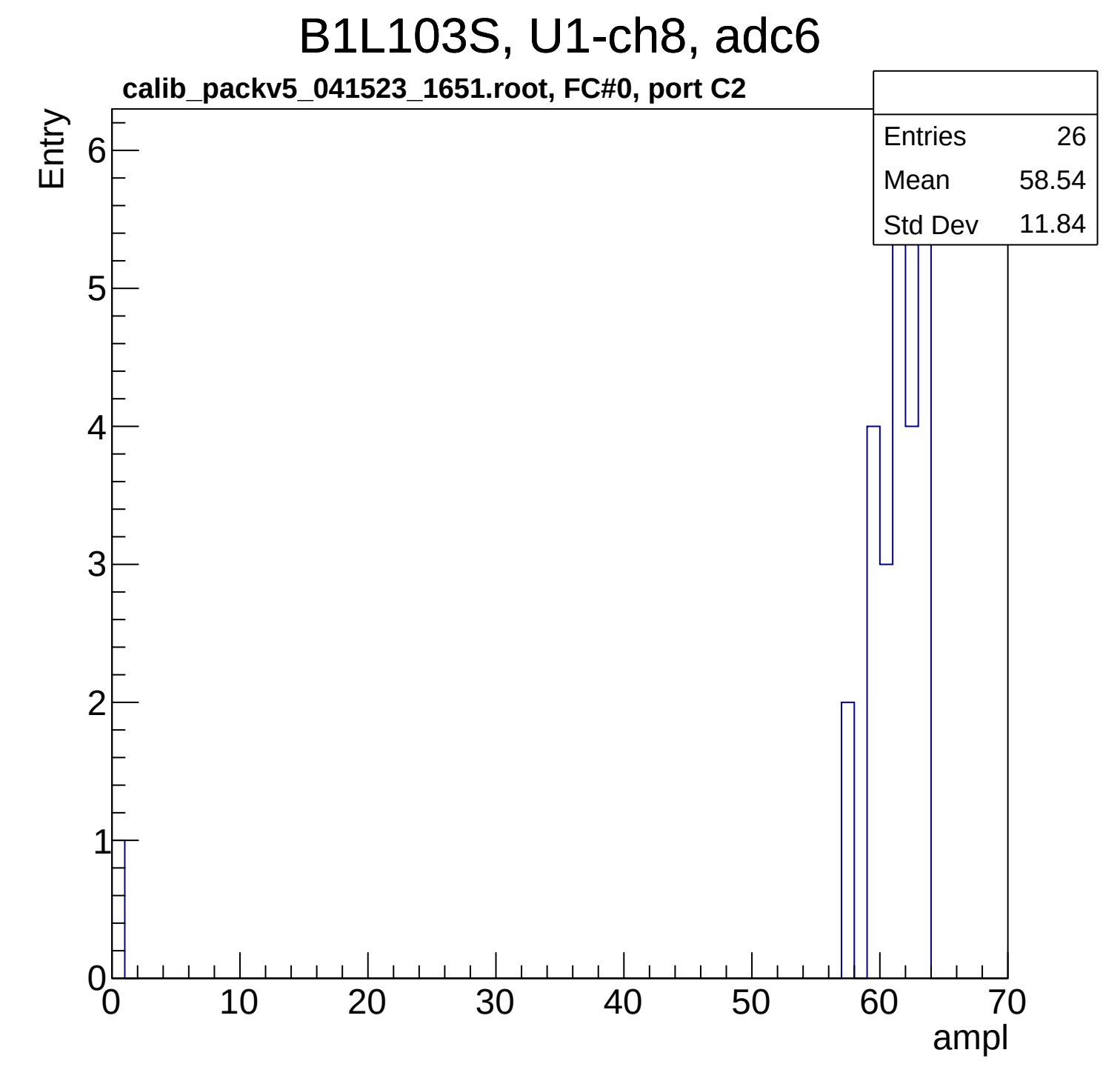
B1L103S, U1-ch8, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 26
Mean 58.54
Std Dev 11.84
Entry
ampl
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1
2
3
4
5
6
0
10
20
30
40
50
60
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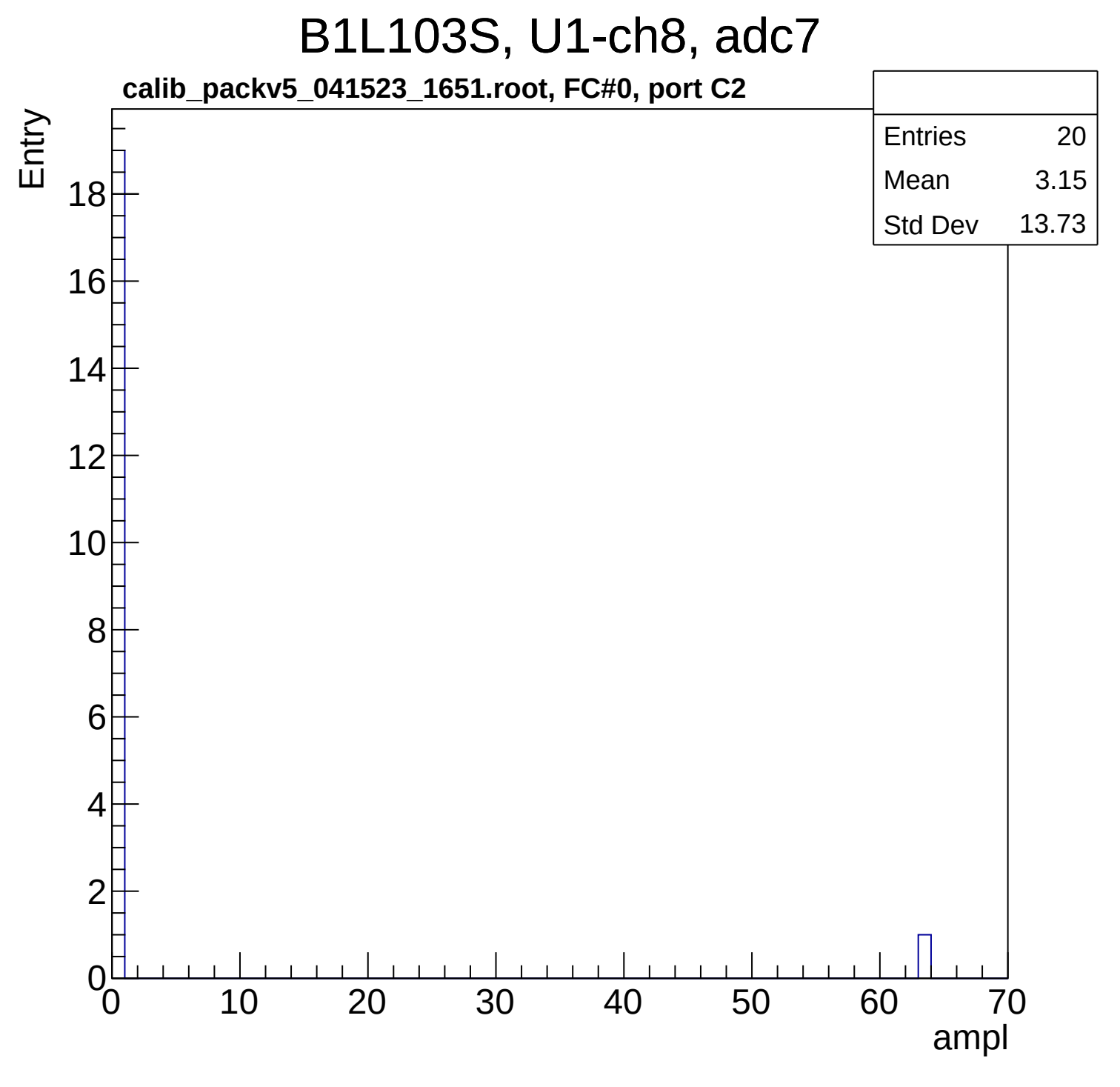
B1L103S, U1-ch8, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
0
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6
8
10
12
14
16
18
0
10
20
30
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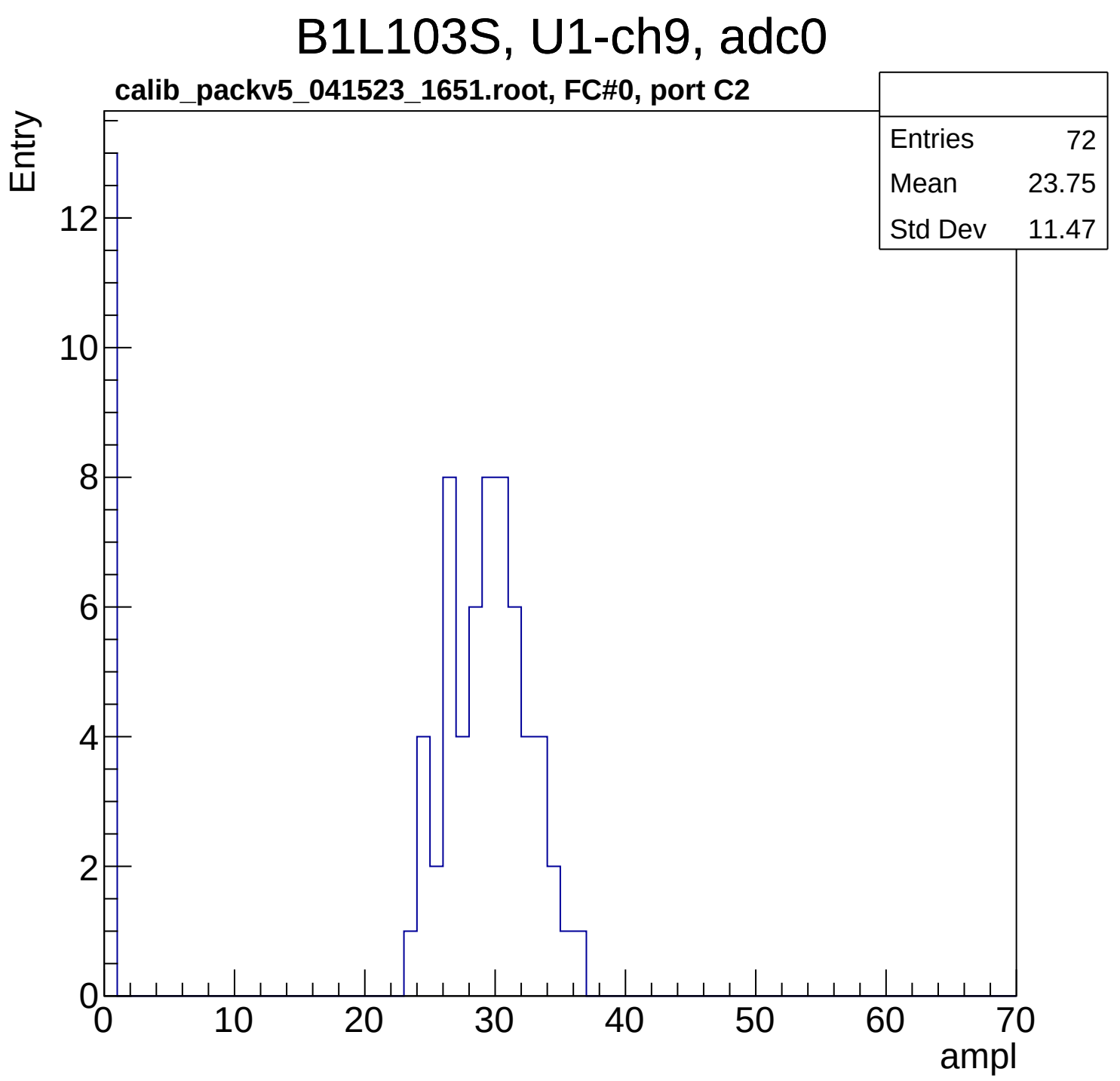
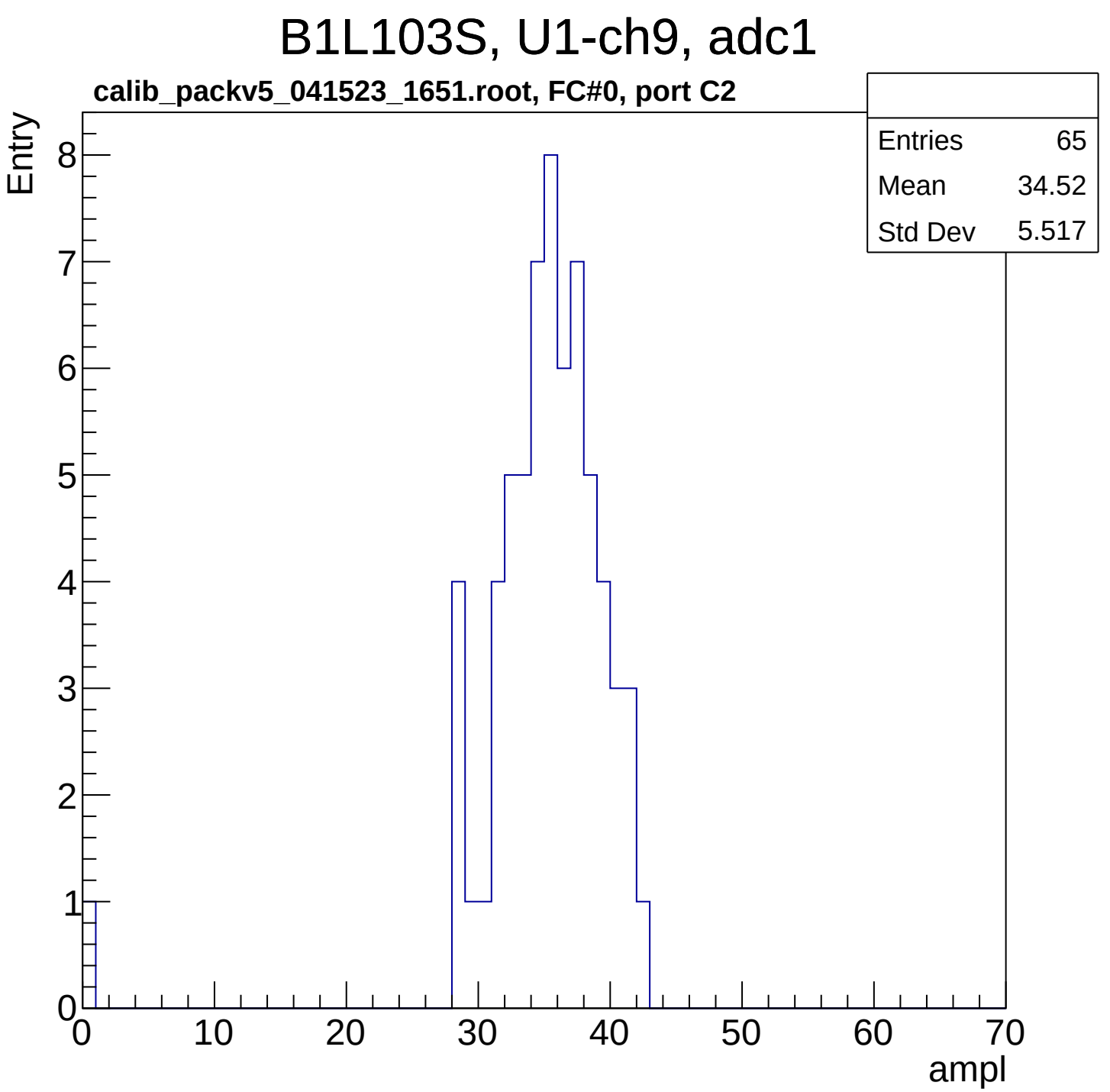
50
60
70
ampl


B1L103S, U1-ch9, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 23.75
Std Dev 11.47
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch9, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 34.52
Std Dev 5.517
Entry
ampl
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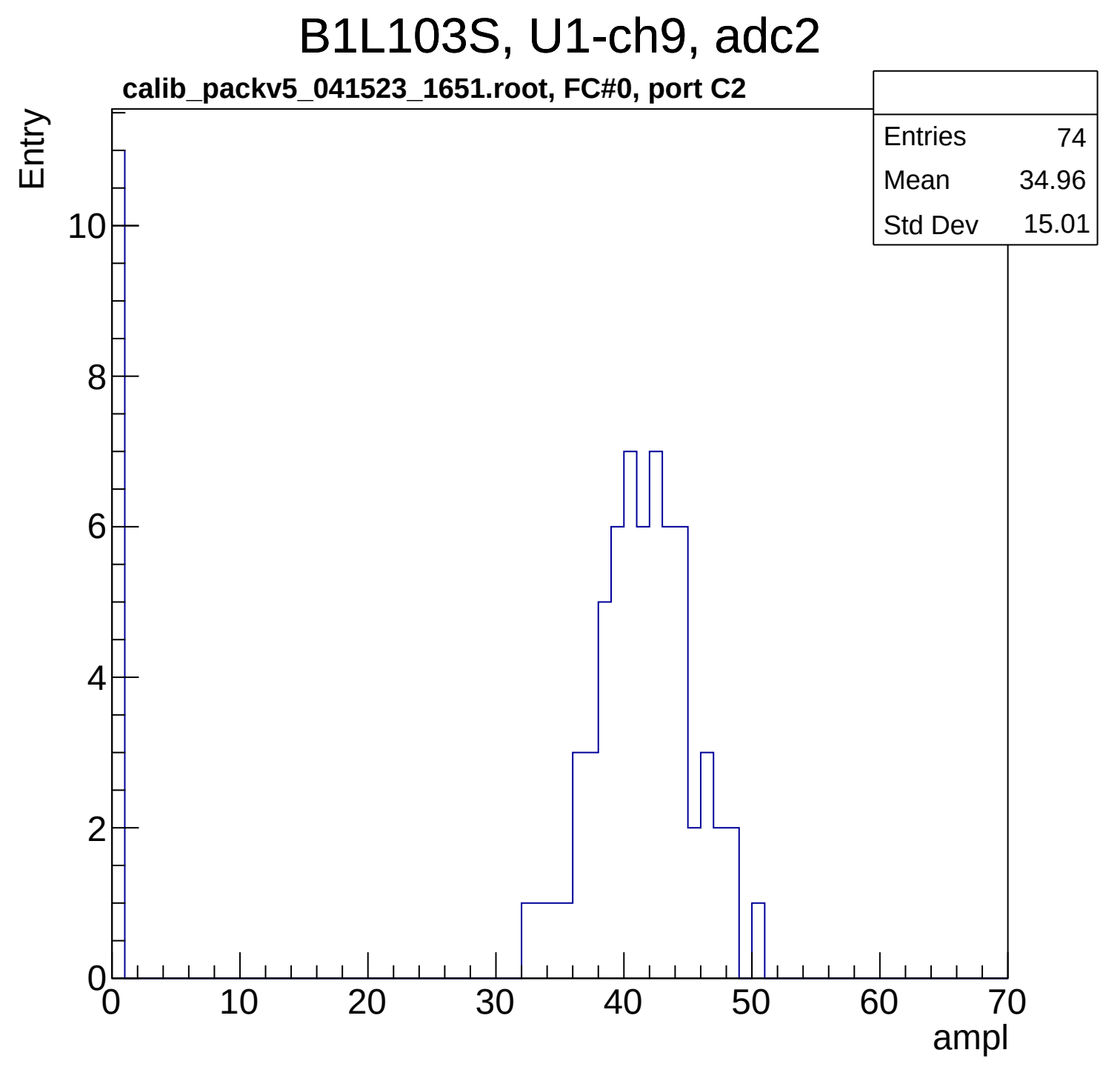
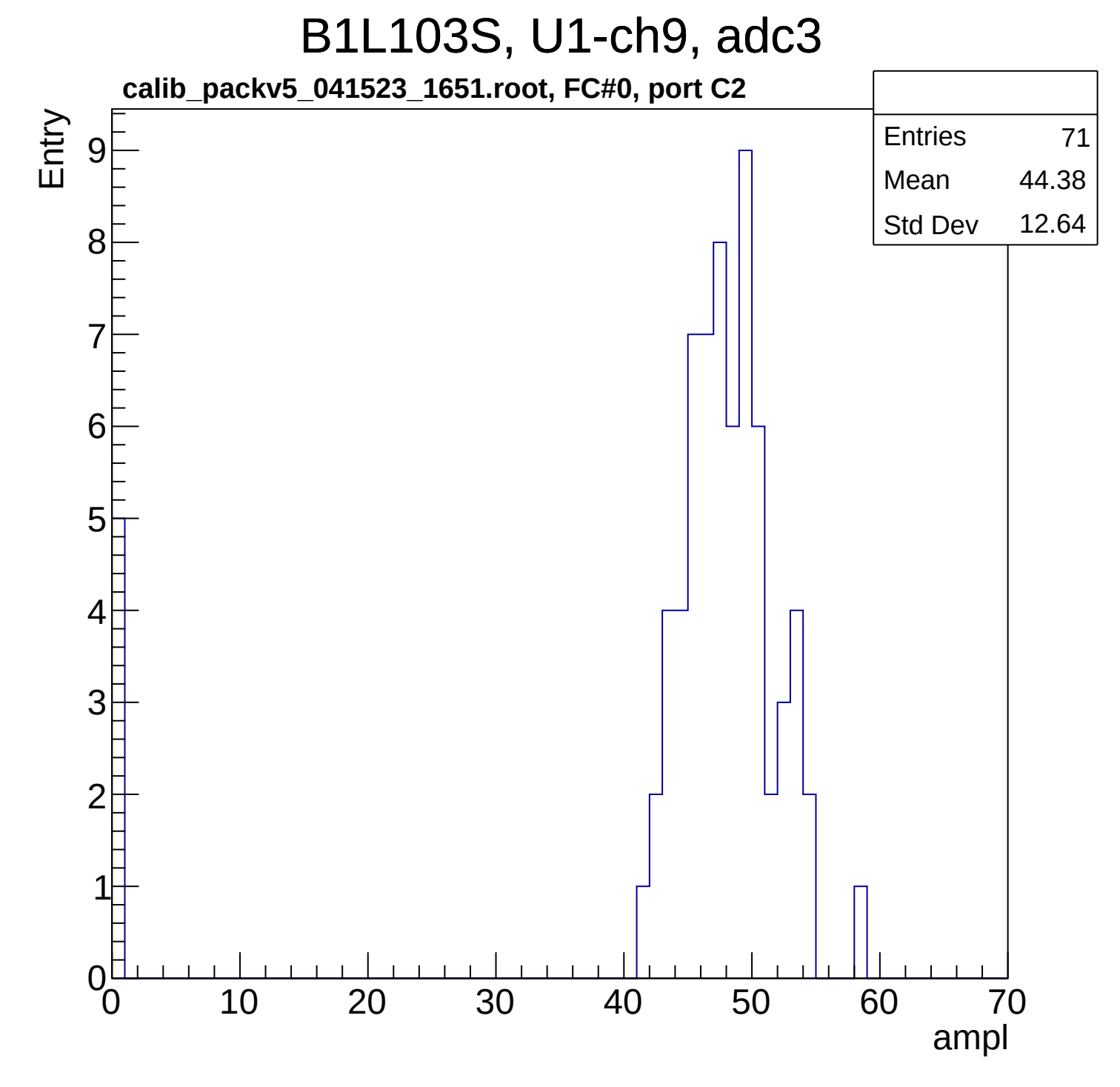
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U1-ch9, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 34.96
Std Dev 15.01
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch9, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 44.38
Std Dev 12.64
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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40
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60
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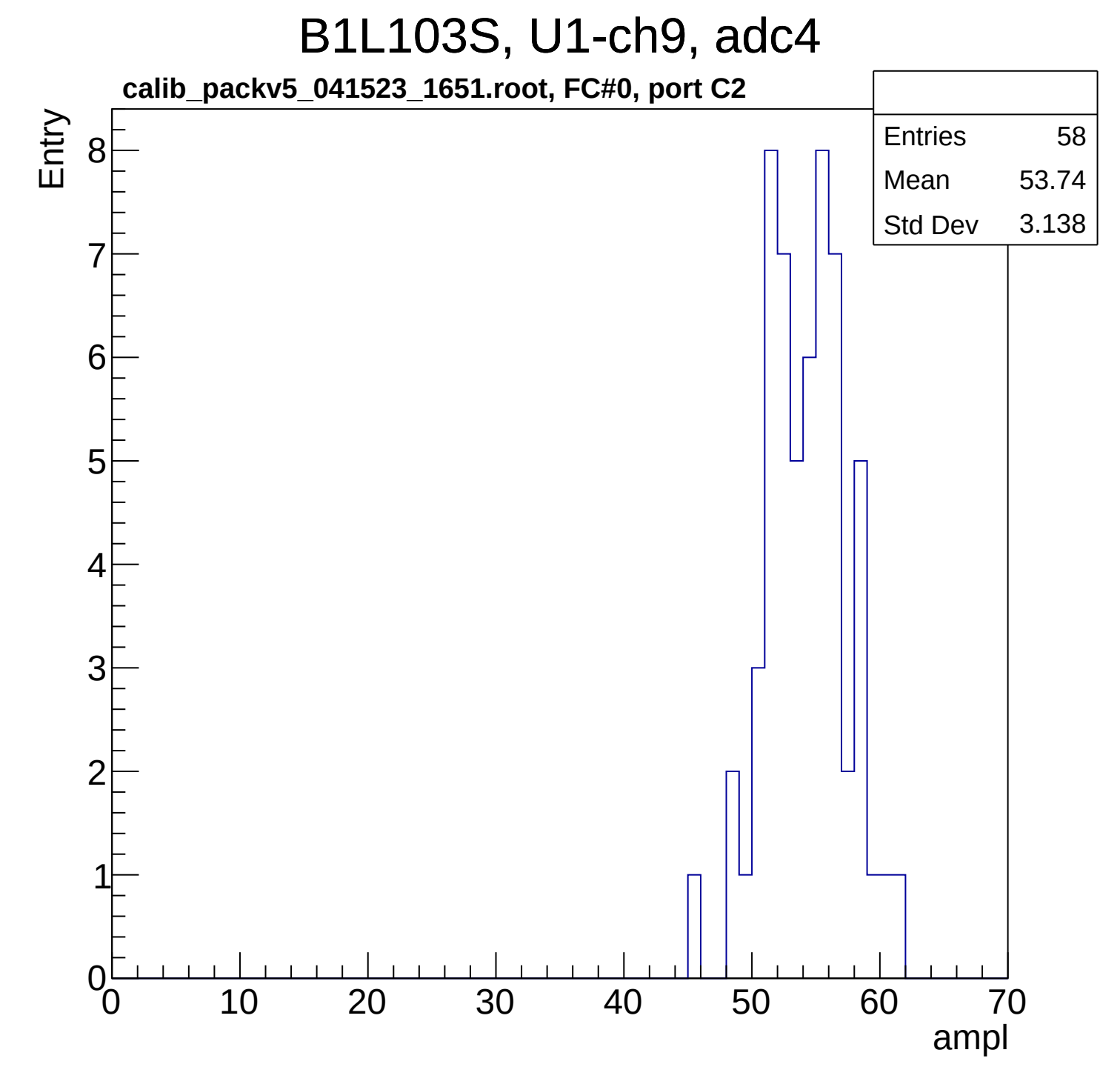
B1L103S, U1-ch9, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 53.74
Std Dev 3.138
Entry
ampl
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2
3
4
5
6
7
8
0
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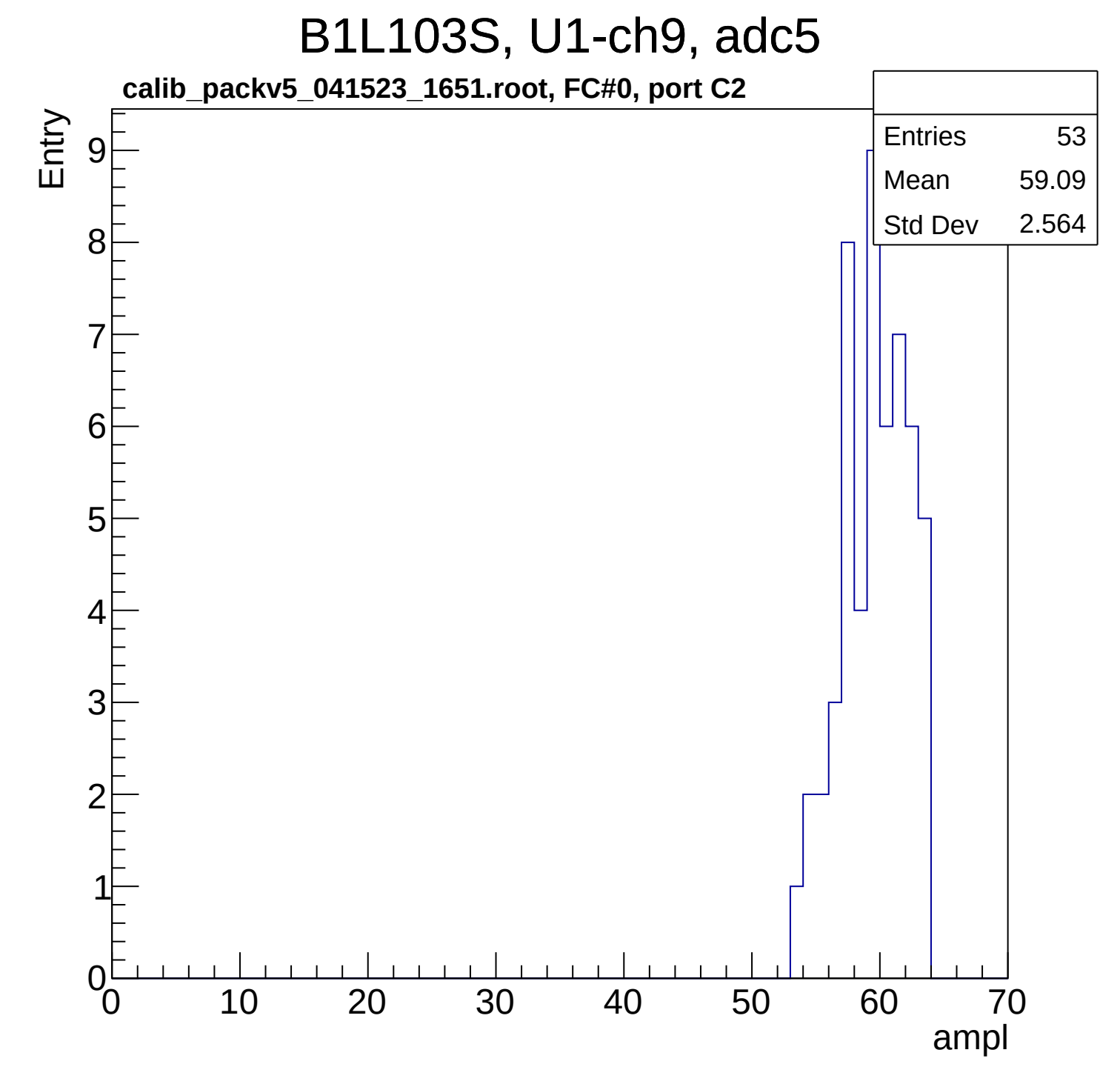
B1L103S, U1-ch9, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 59.09
Std Dev 2.564
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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60
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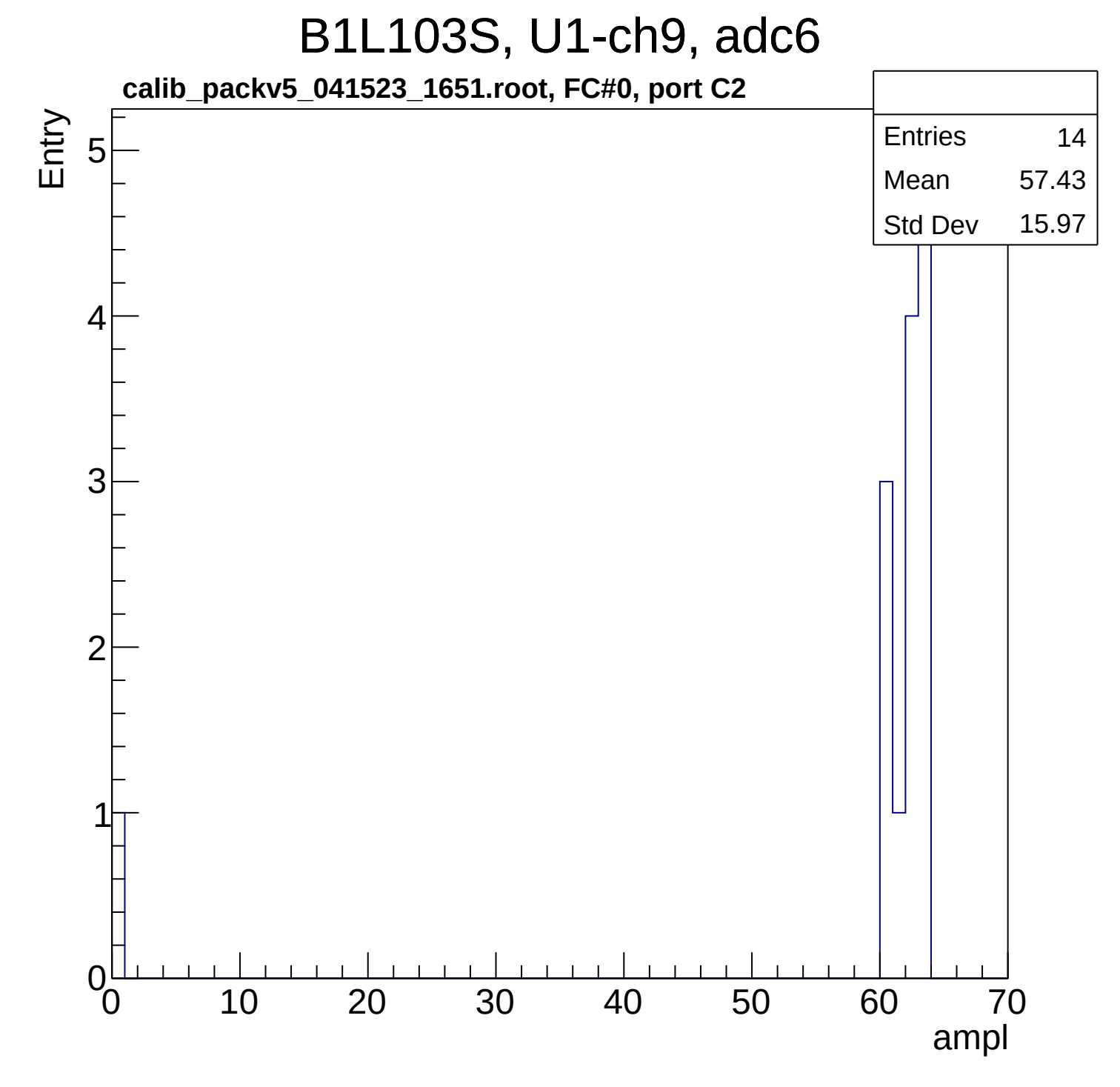
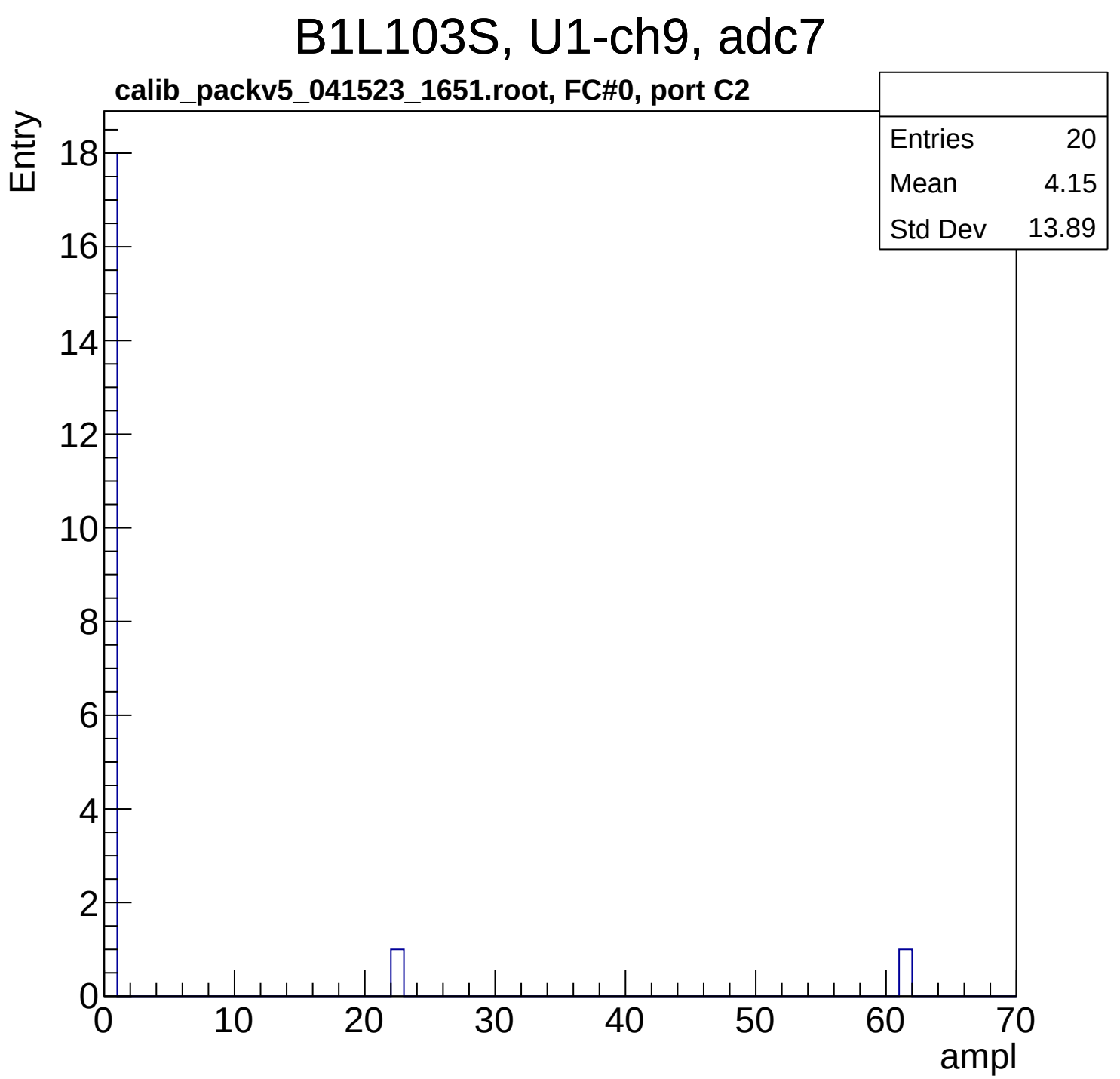
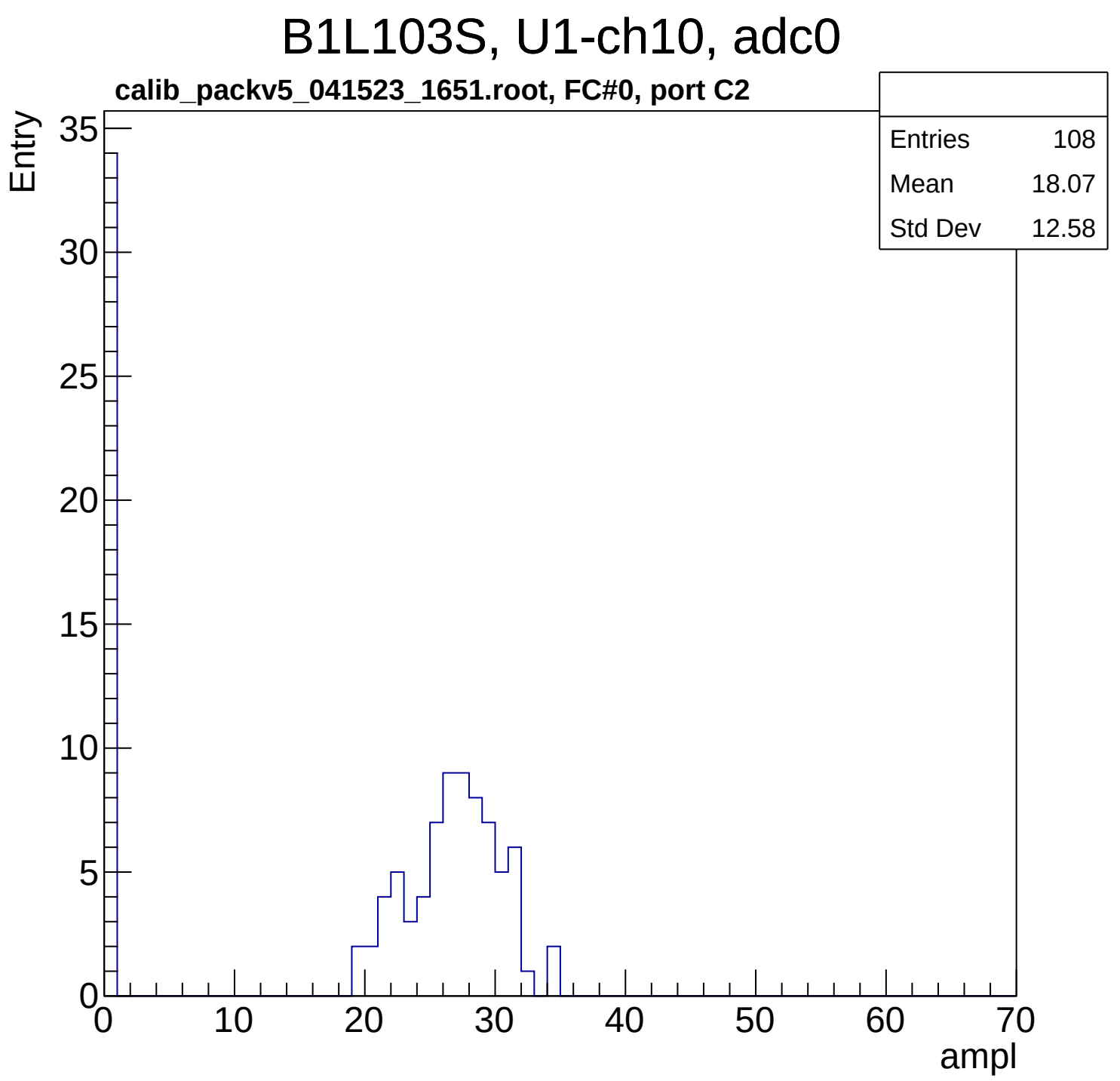

B1L103S, U1-ch9, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 14
Mean 57.43
Std Dev 15.97
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U1-ch9, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 4.15
Std Dev 13.89
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch10, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 108
Mean 18.07
Std Dev 12.58
Entry
ampl
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5
10
15
20
25
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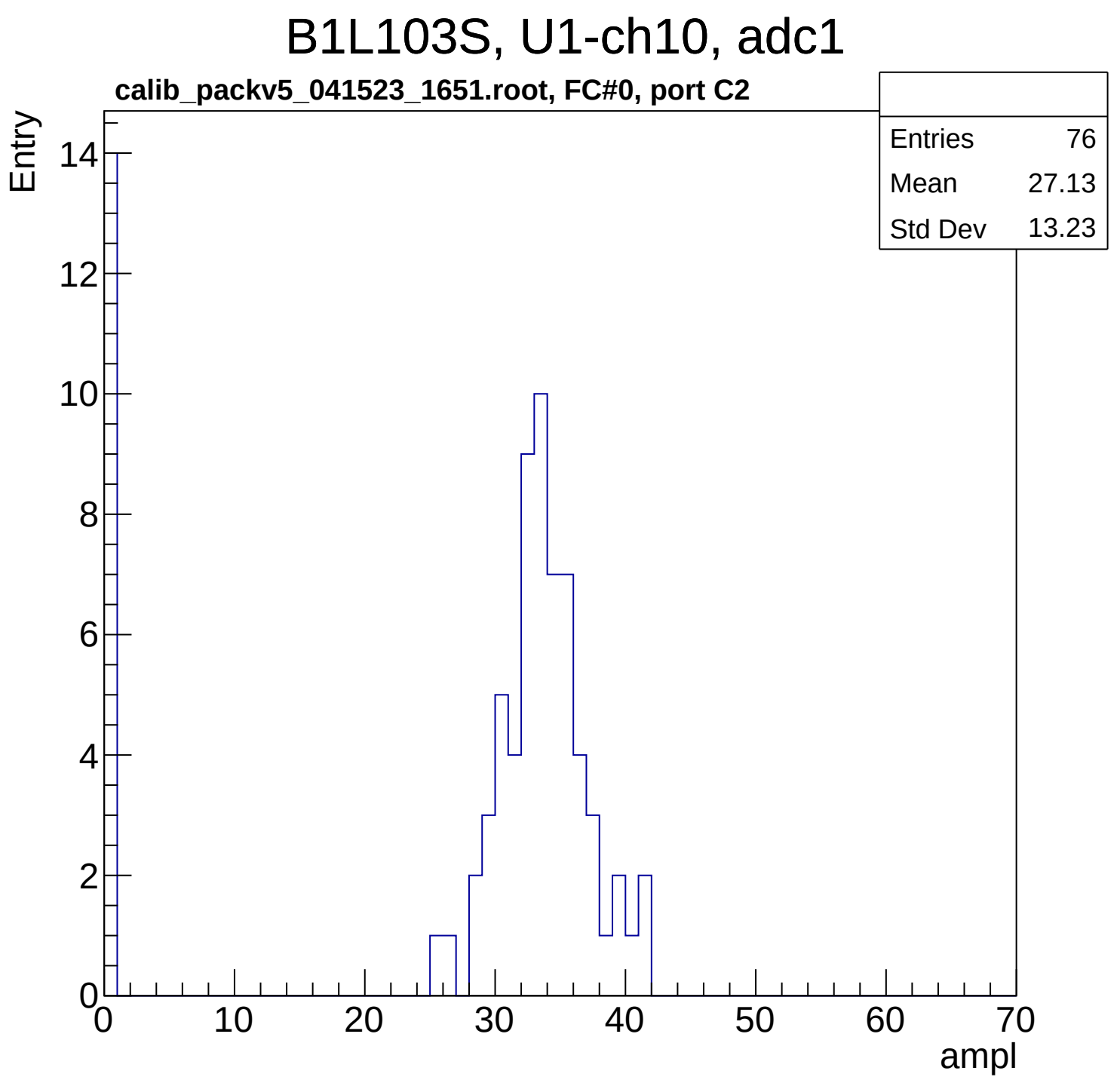
35
0
10
20
30
40
50
60
70


B1L103S, U1-ch10, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 27.13
Std Dev 13.23
Entry
ampl
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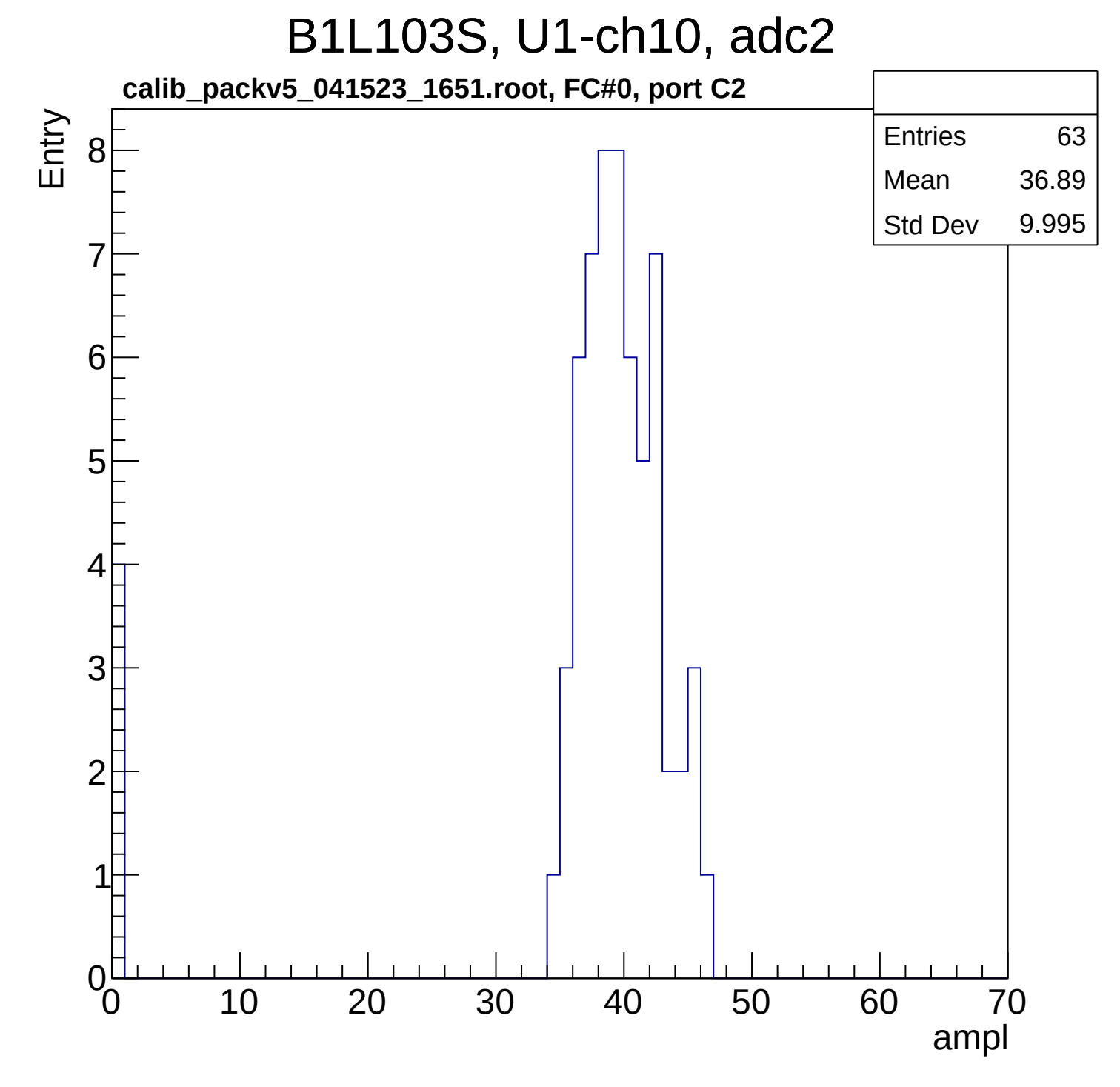
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L103S, U1-ch10, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 36.89
Std Dev 9.995
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
30
40
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60
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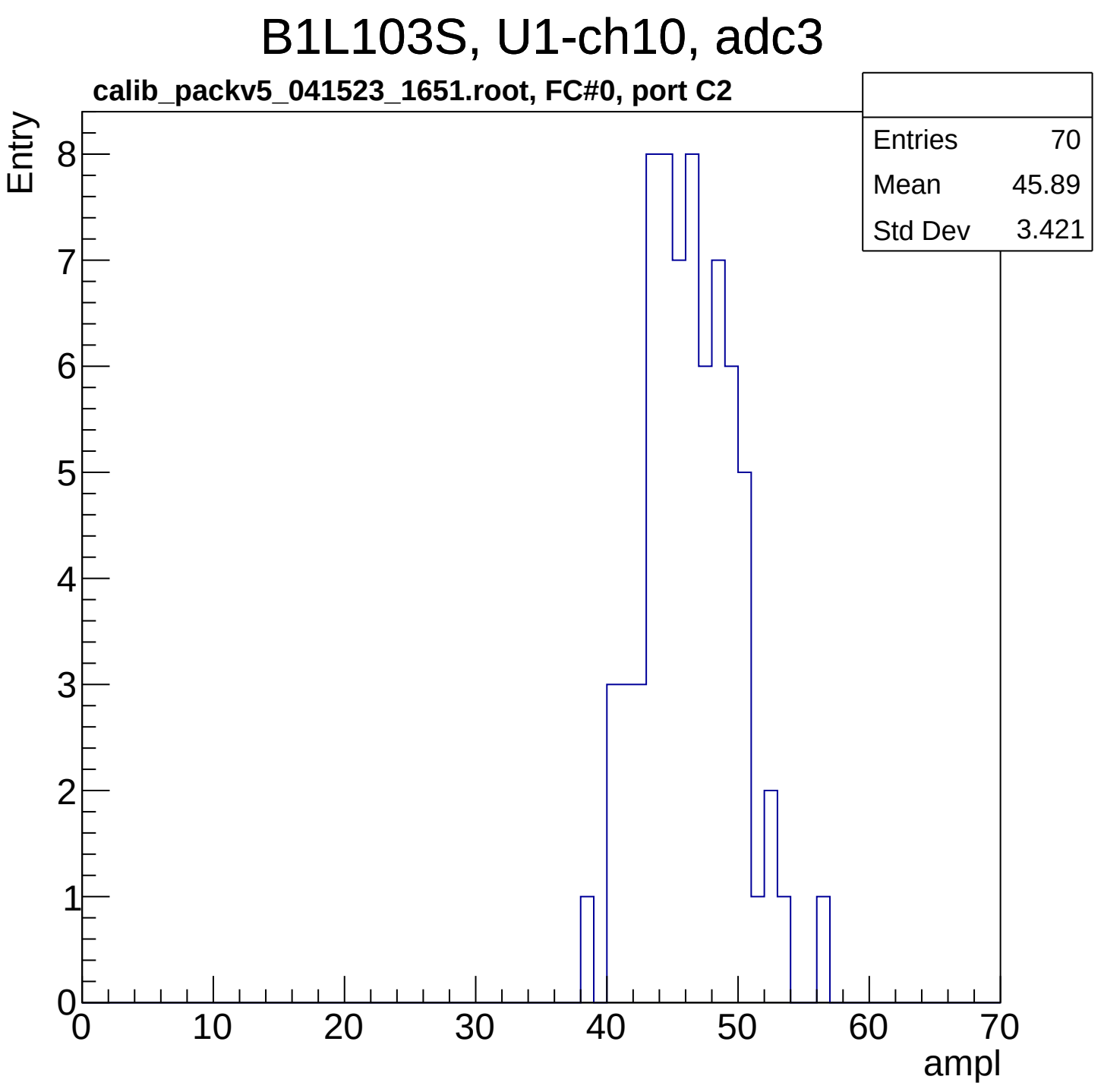
B1L103S, U1-ch10, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 45.89
Std Dev 3.421
Entry
ampl
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2
3
4
5
6
7
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0
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60
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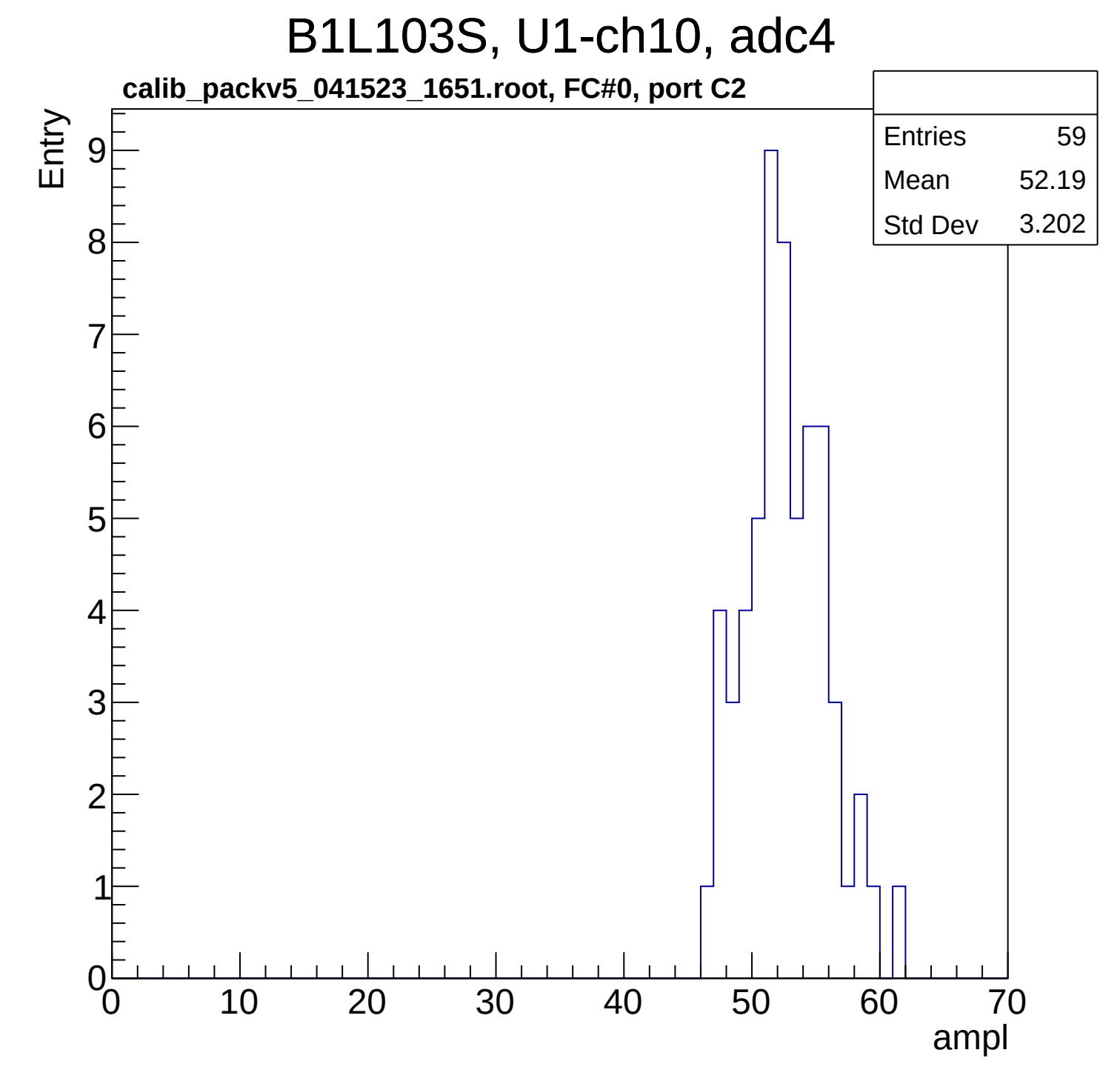
B1L103S, U1-ch10, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 52.19
Std Dev 3.202
Entry
ampl
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2
3
4
5
6
7
8
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0
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40
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60
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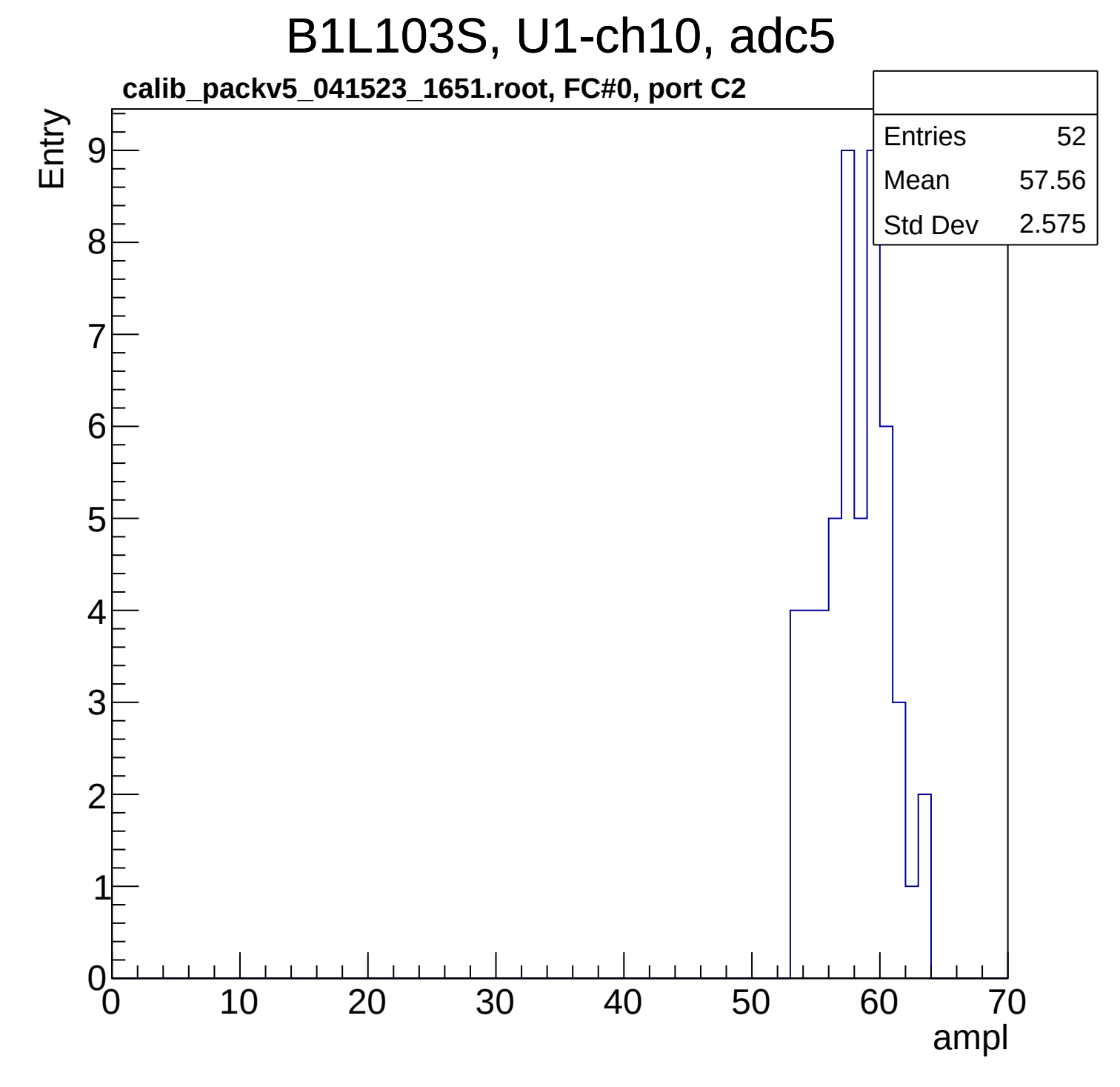
B1L103S, U1-ch10, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 57.56
Std Dev 2.575
Entry
ampl
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2
3
4
5
6
7
8
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0
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20
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60
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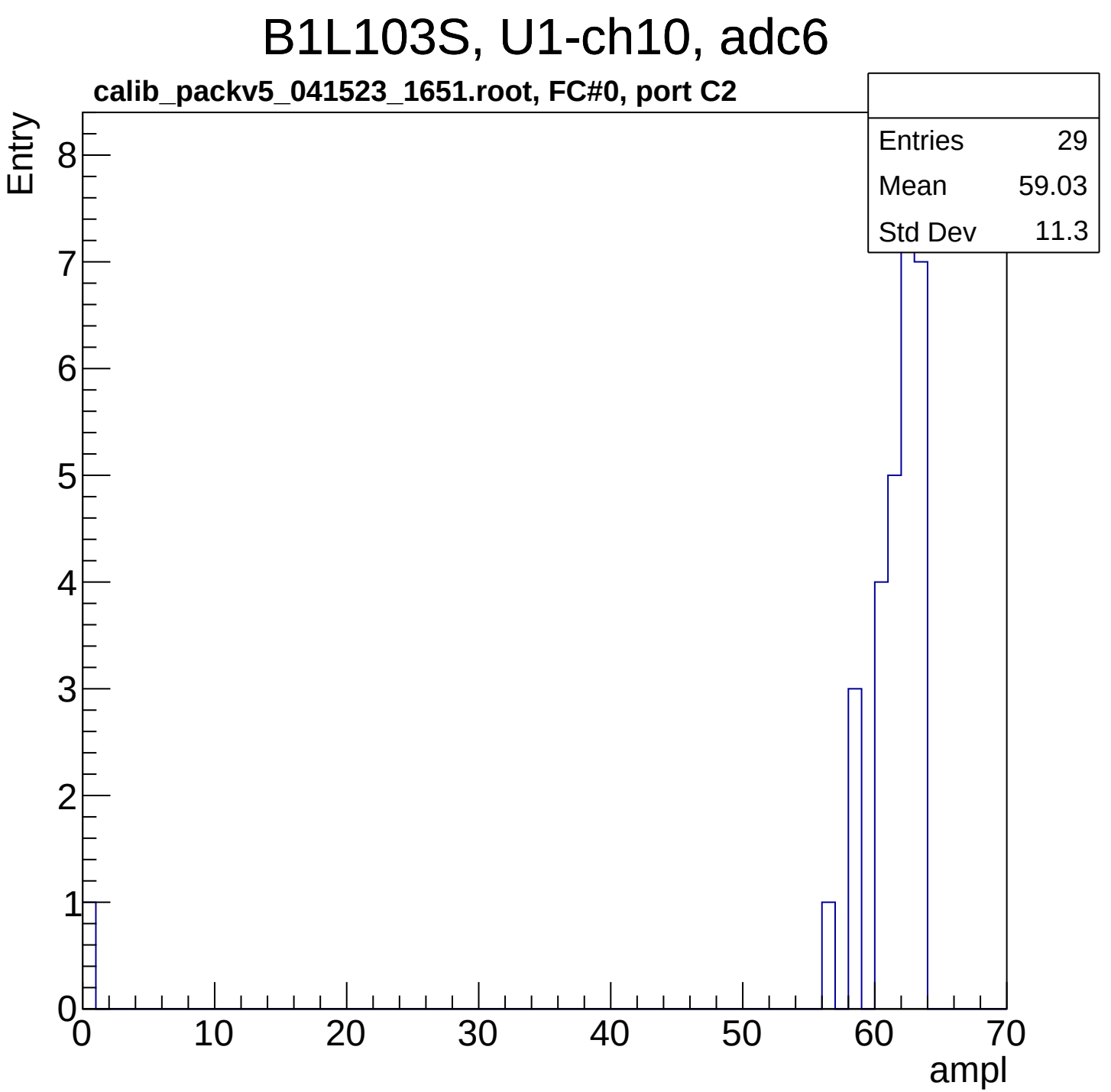
B1L103S, U1-ch10, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 29
Mean 59.03
Std Dev 11.3
Entry
ampl
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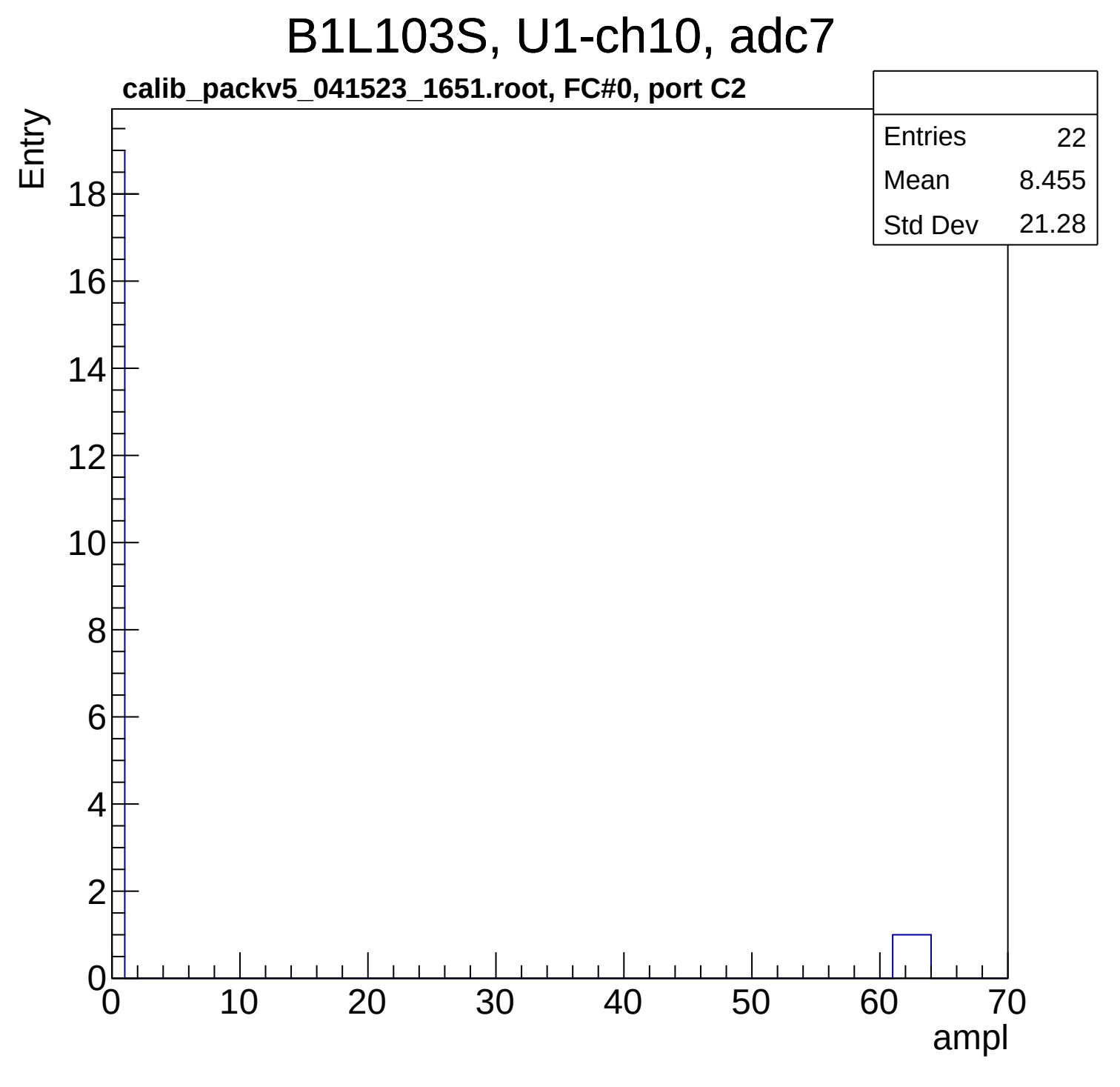
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U1-ch10, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 8.455
Std Dev 21.28
Entry
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6
8
10
12
14
16
18
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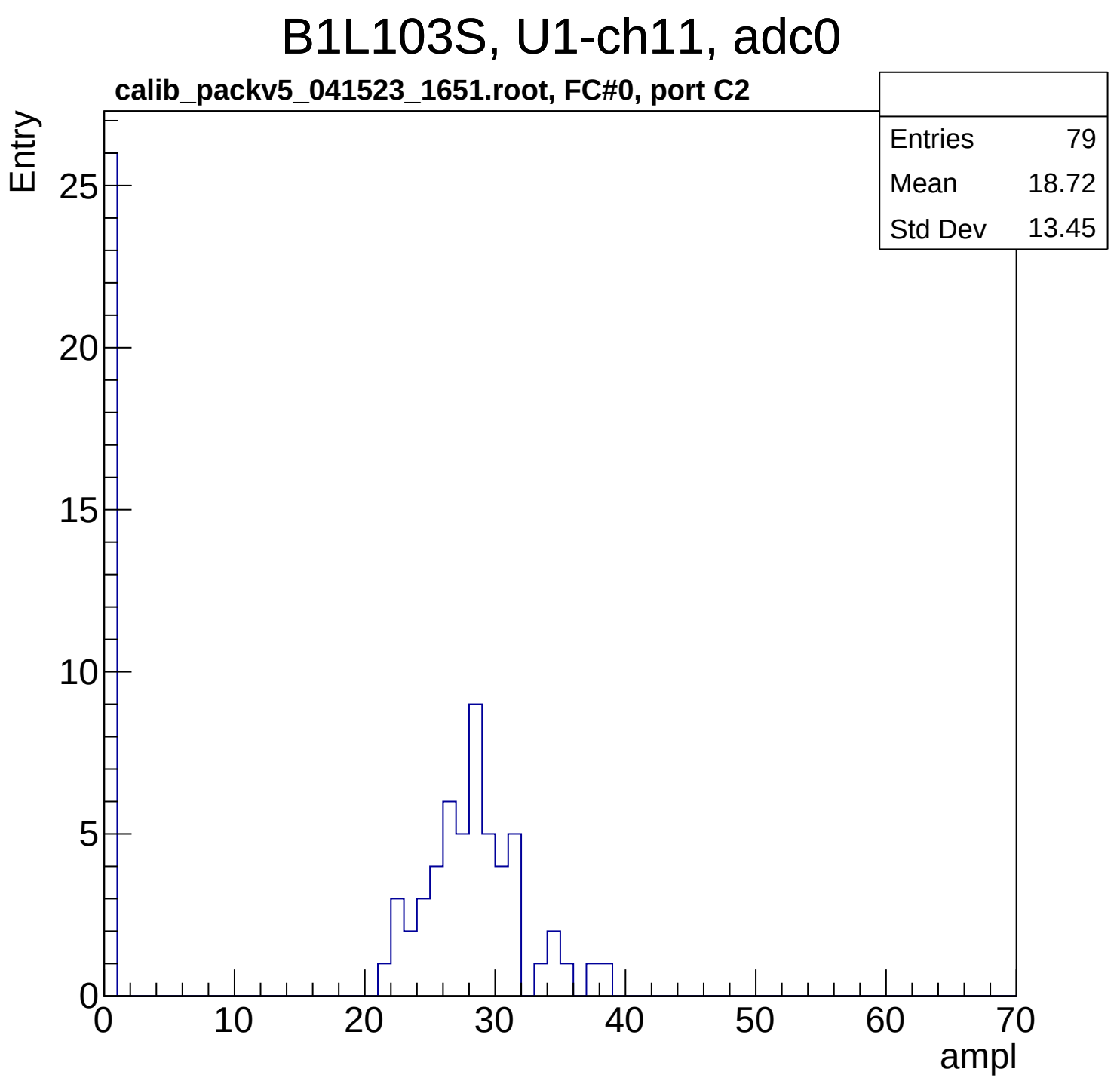
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch11, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 18.72
Std Dev 13.45
Entry
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10
15
20
25
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10
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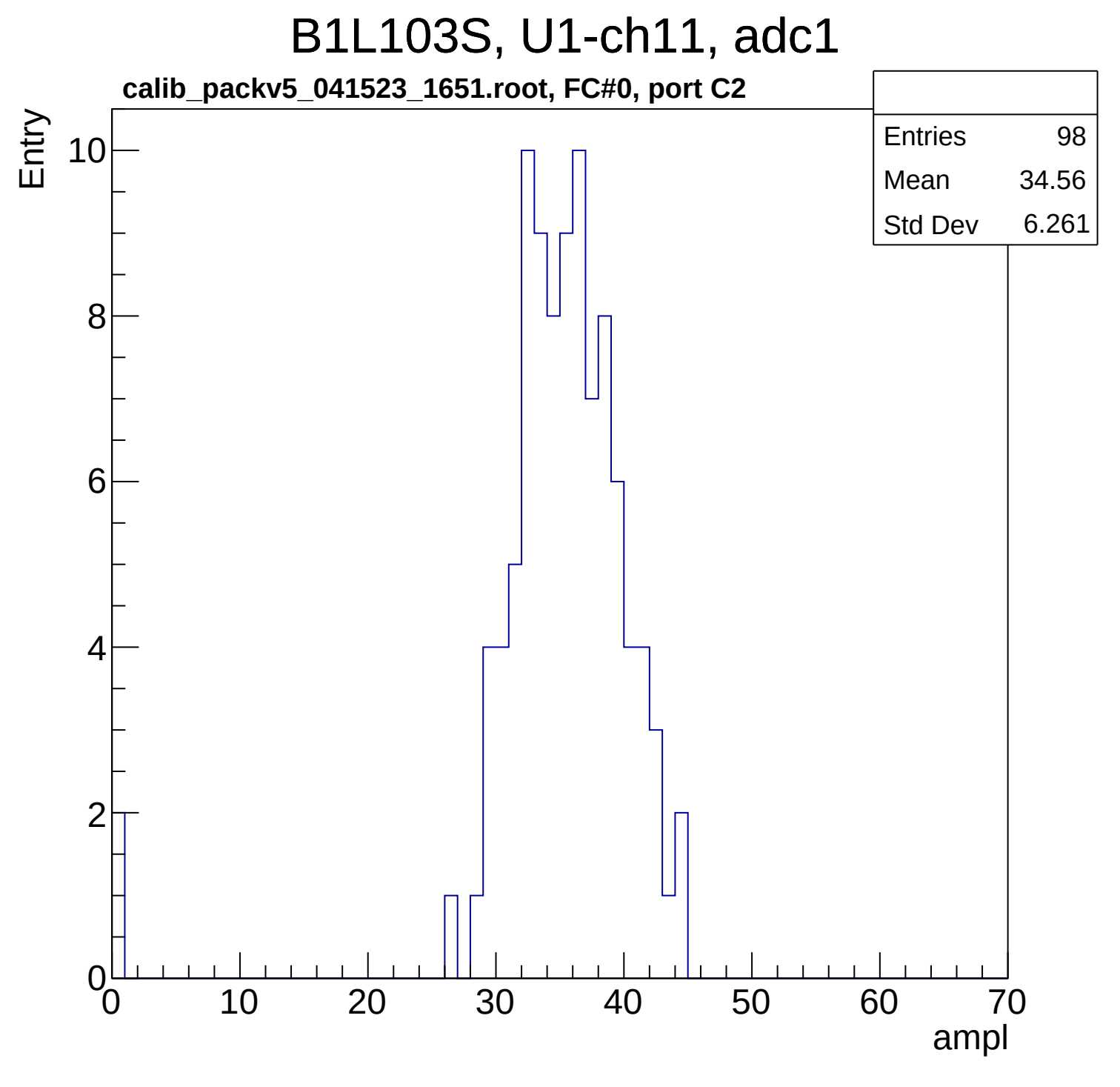
50
60
70
ampl


B1L103S, U1-ch11, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 98
Mean 34.56
Std Dev 6.261
Entry
ampl
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4
6
8
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0
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20
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50
60
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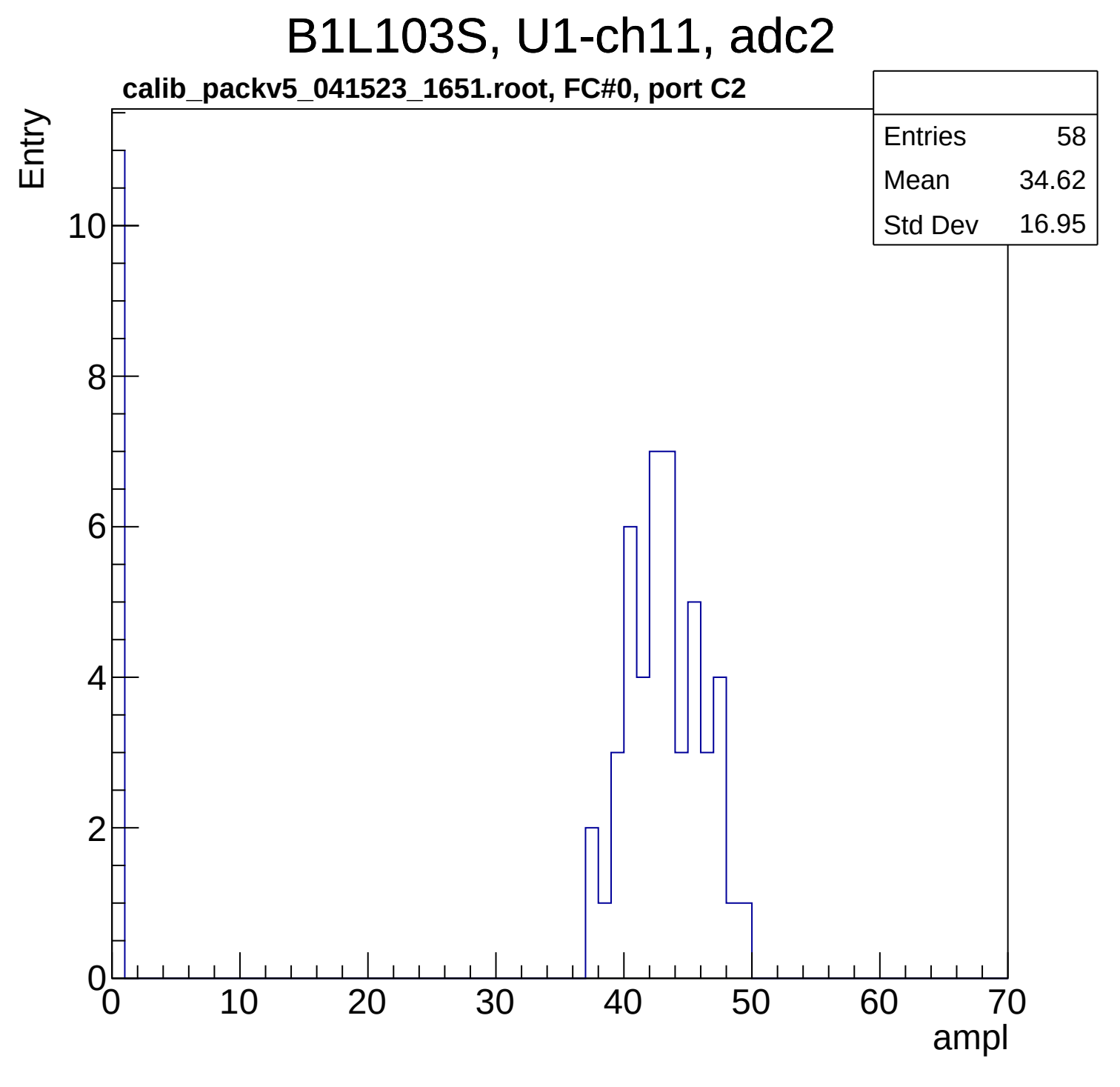
B1L103S, U1-ch11, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 34.62
Std Dev 16.95
Entry
0
2
4
6
8
10
0
10
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30
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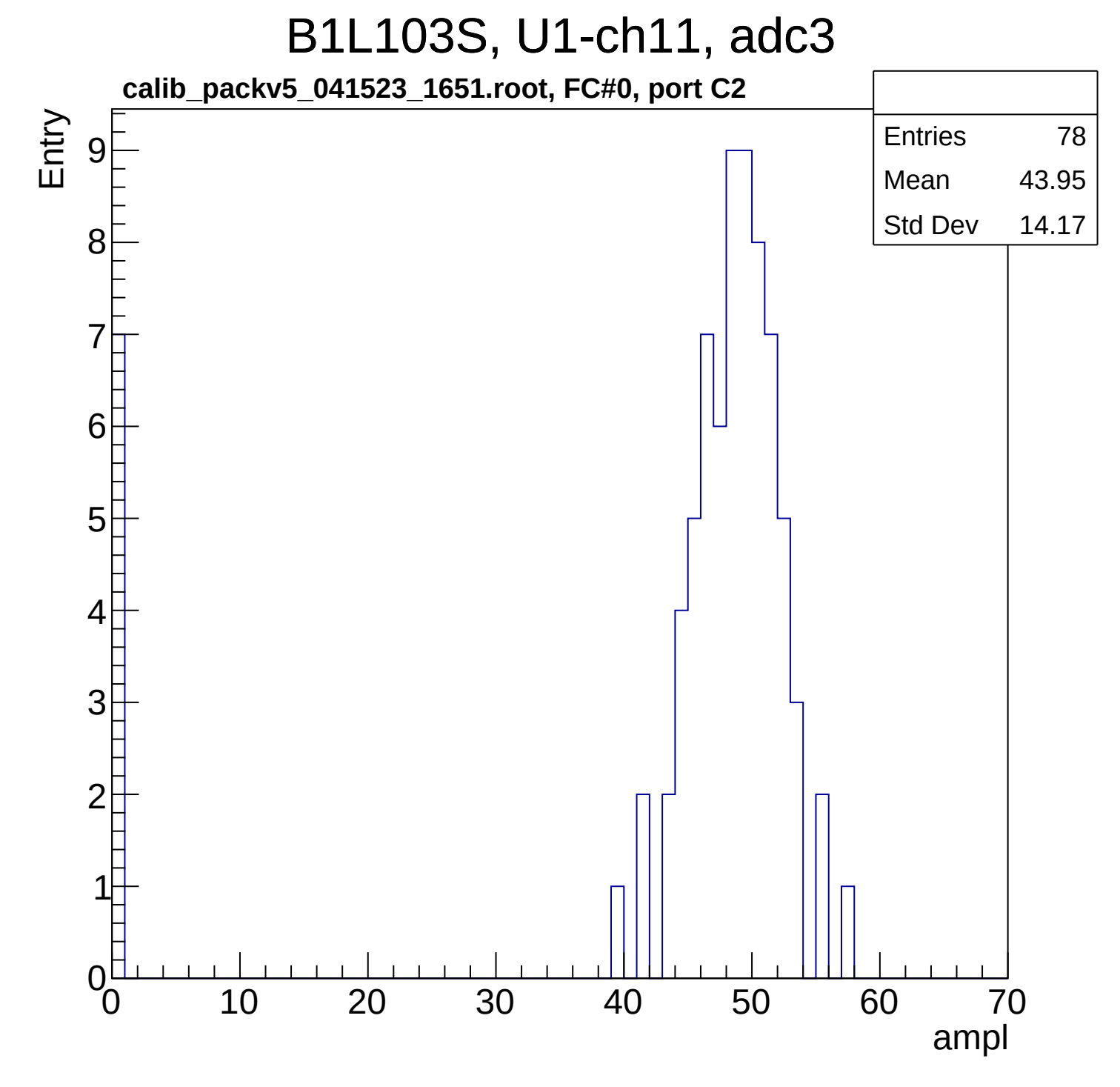
50
60
70
ampl


B1L103S, U1-ch11, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 43.95
Std Dev 14.17
Entry
ampl
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2
3
4
5
6
7
8
9
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60
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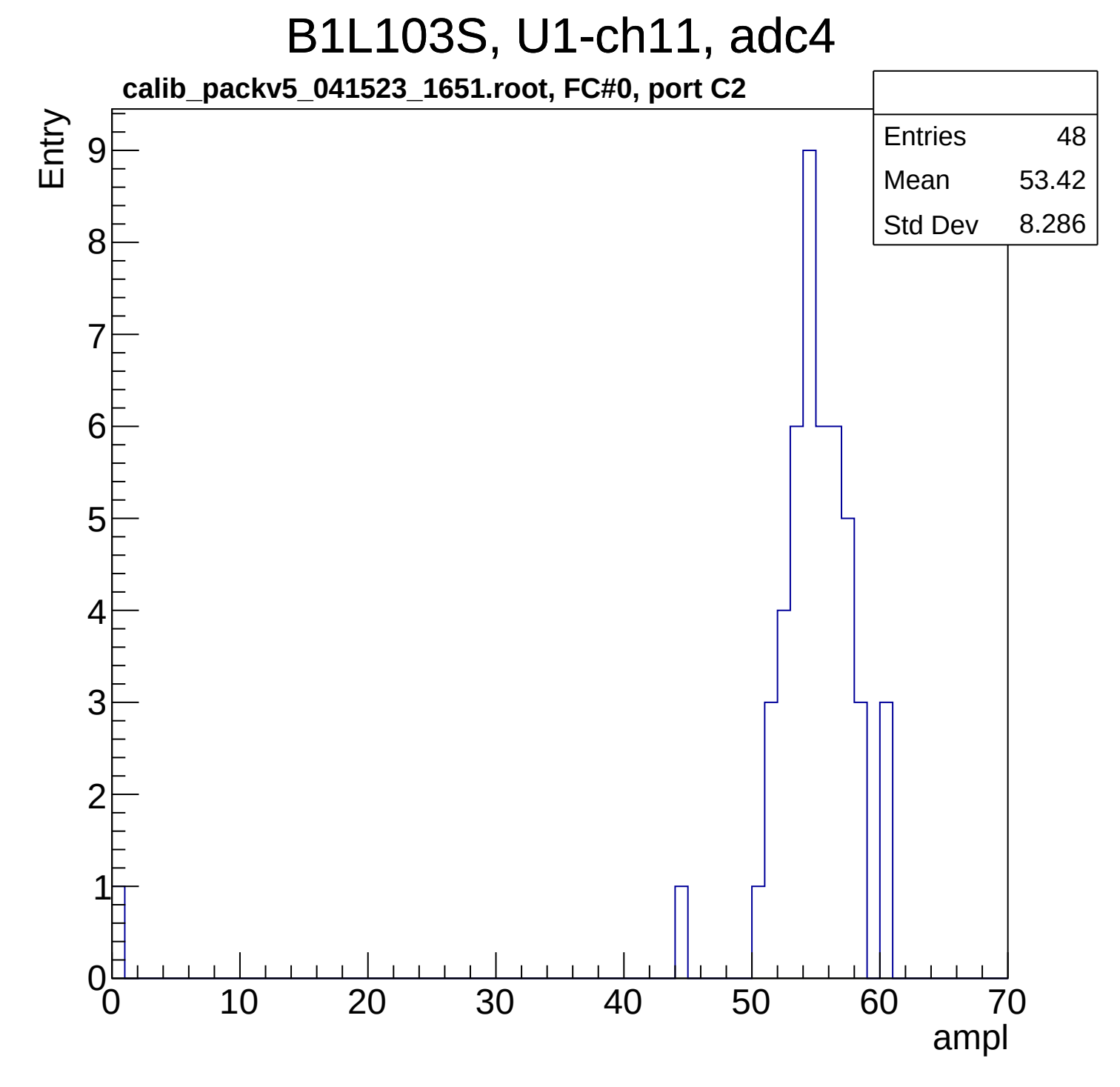
B1L103S, U1-ch11, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 53.42
Std Dev 8.286
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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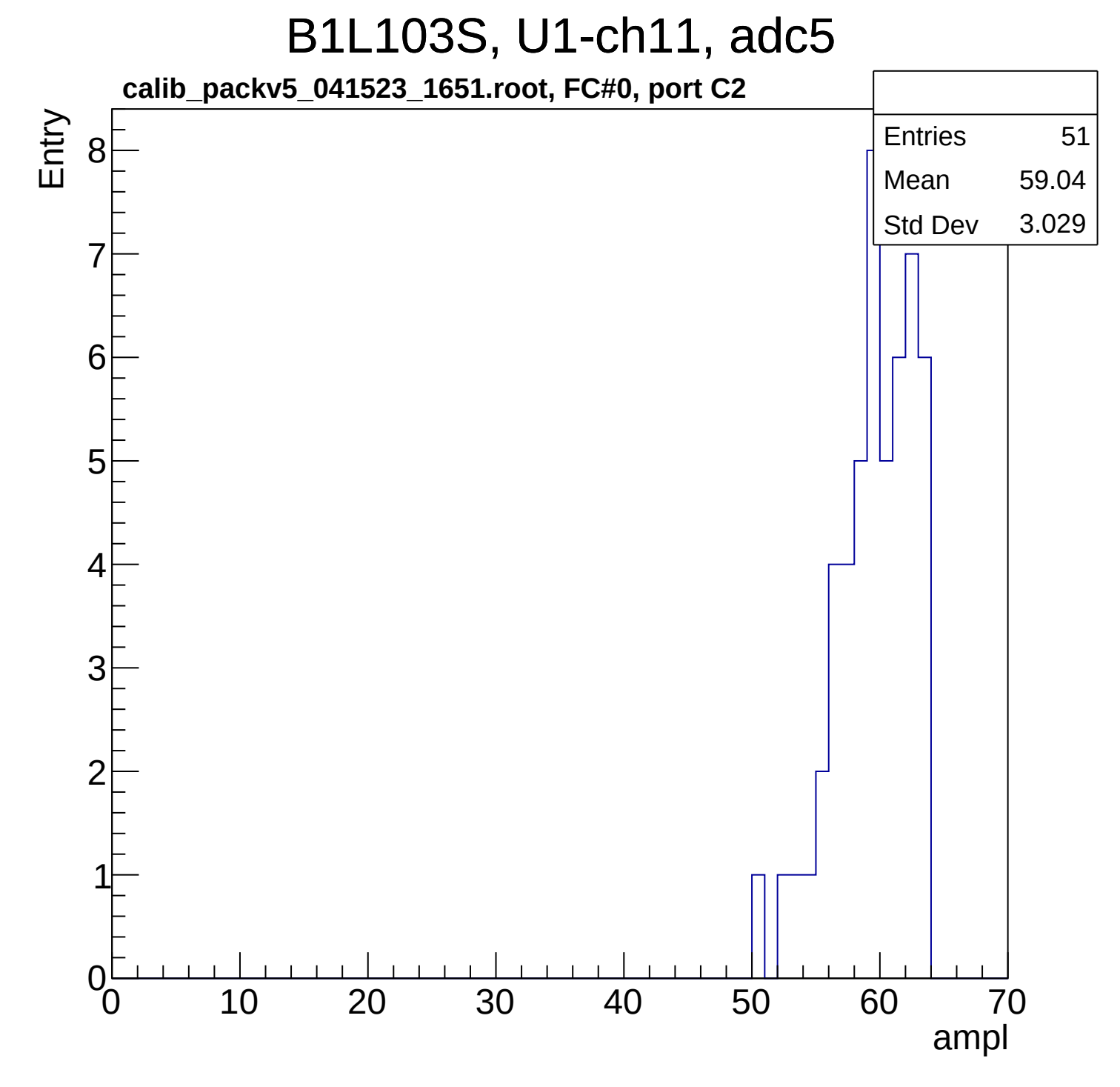
40
50
60
70


B1L103S, U1-ch11, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 59.04
Std Dev 3.029
Entry
ampl
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1
2
3
4
5
6
7
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0
10
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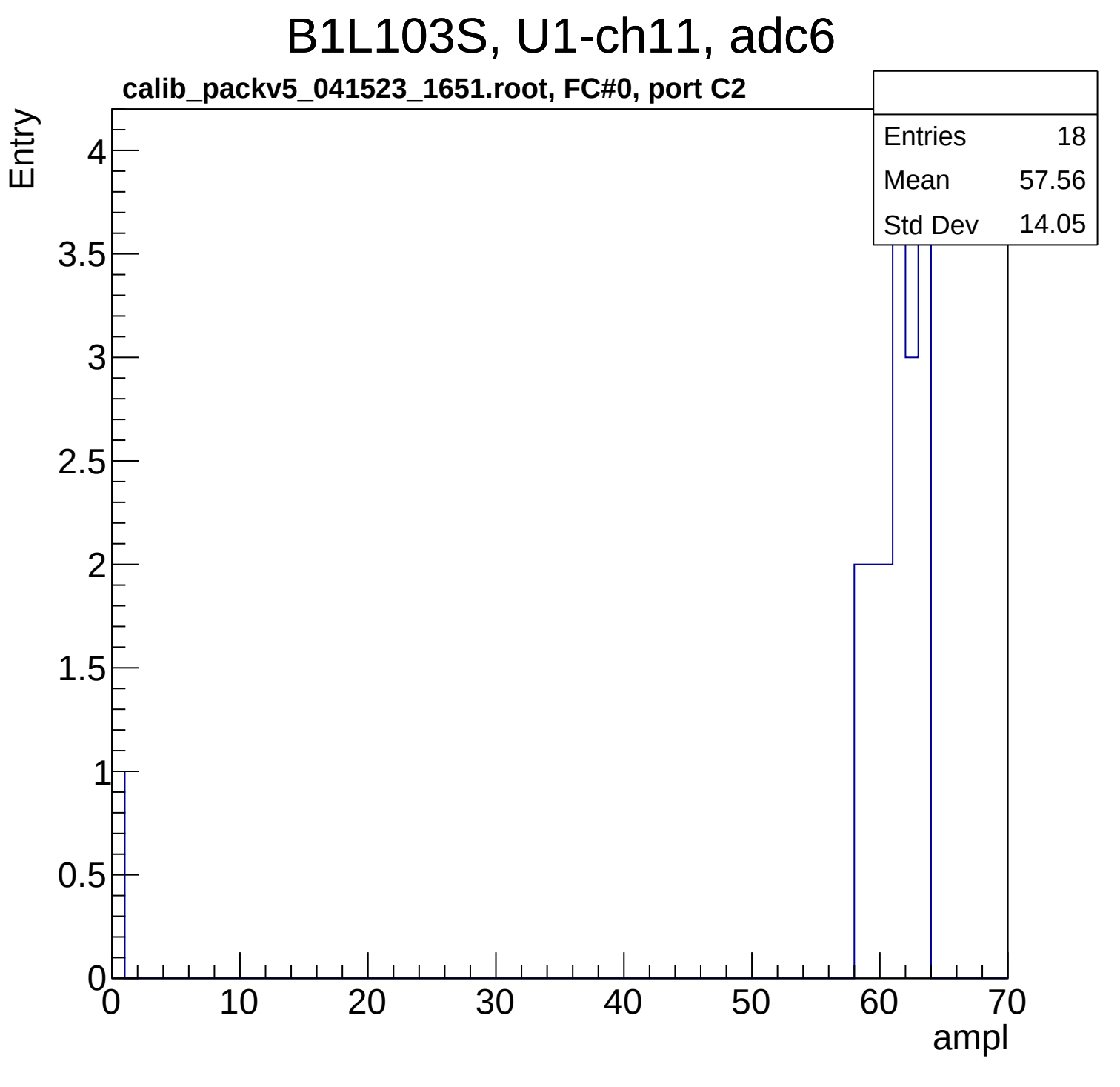
50
60
70


B1L103S, U1-ch11, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 57.56
Std Dev 14.05
Entry
ampl
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1
1.5
2
2.5
3
3.5
4
0
10
20
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40
50
60
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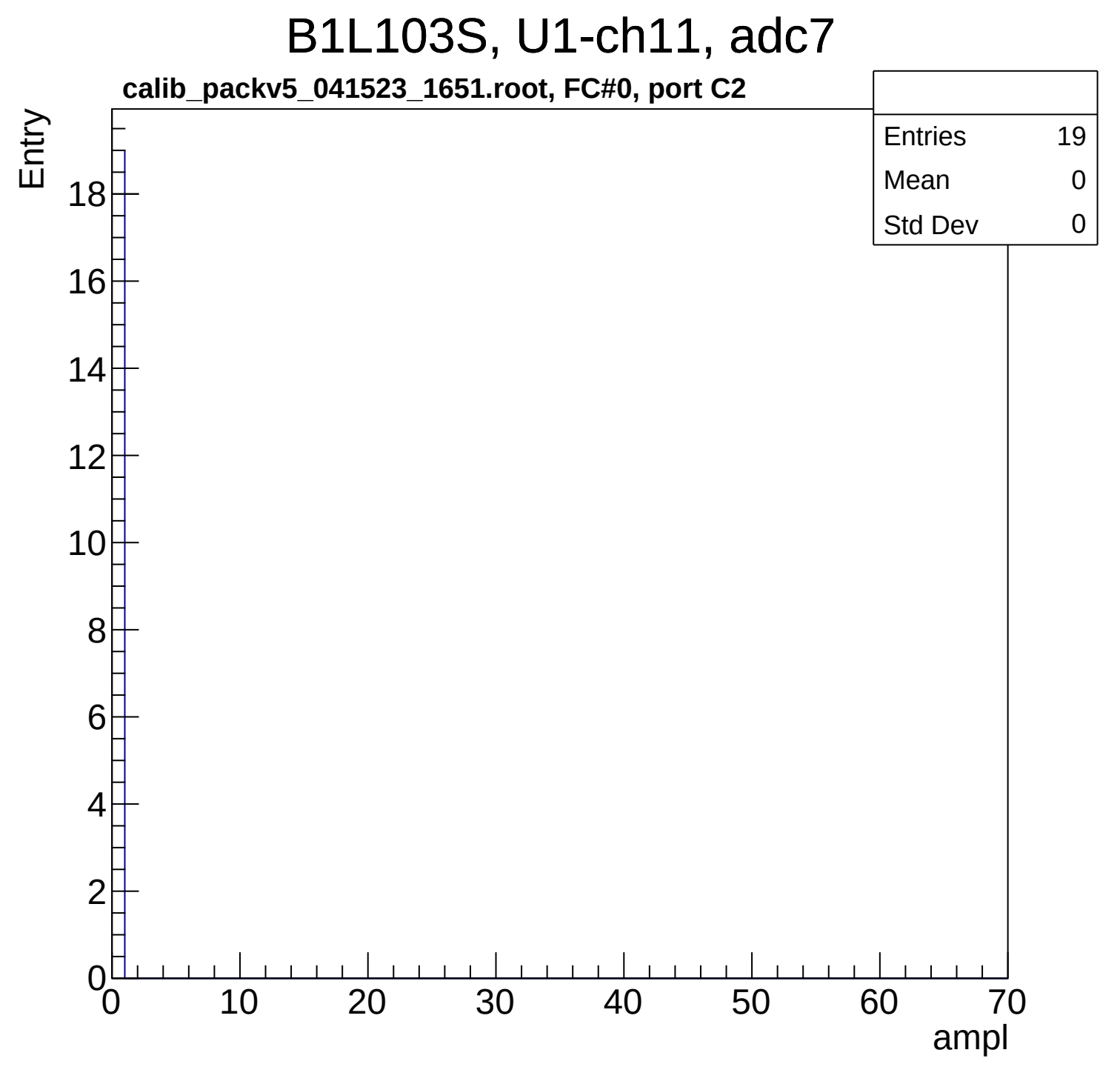
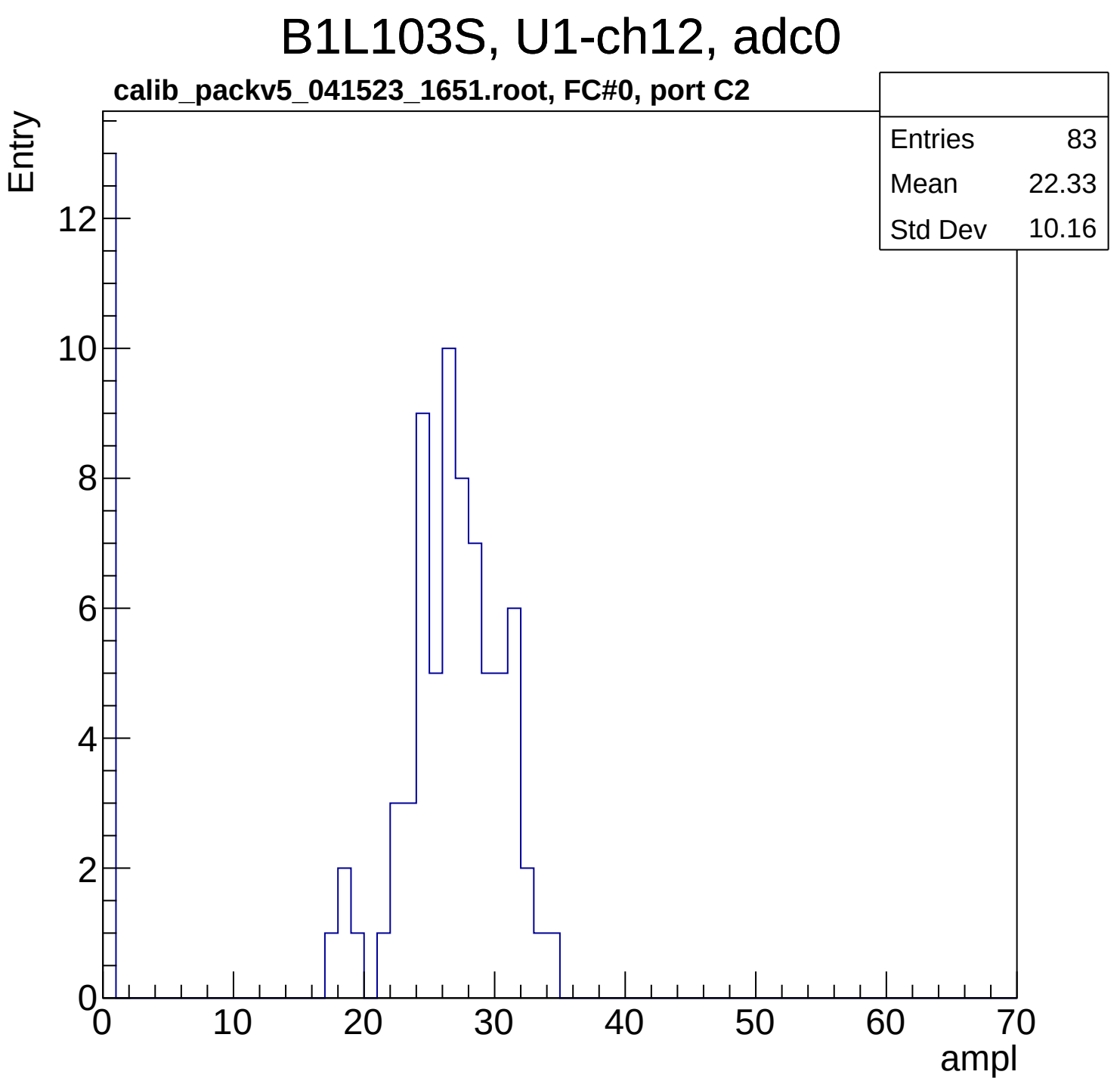

B1L103S, U1-ch11, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch12, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 22.33
Std Dev 10.16
Entry
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2
4
6
8
10
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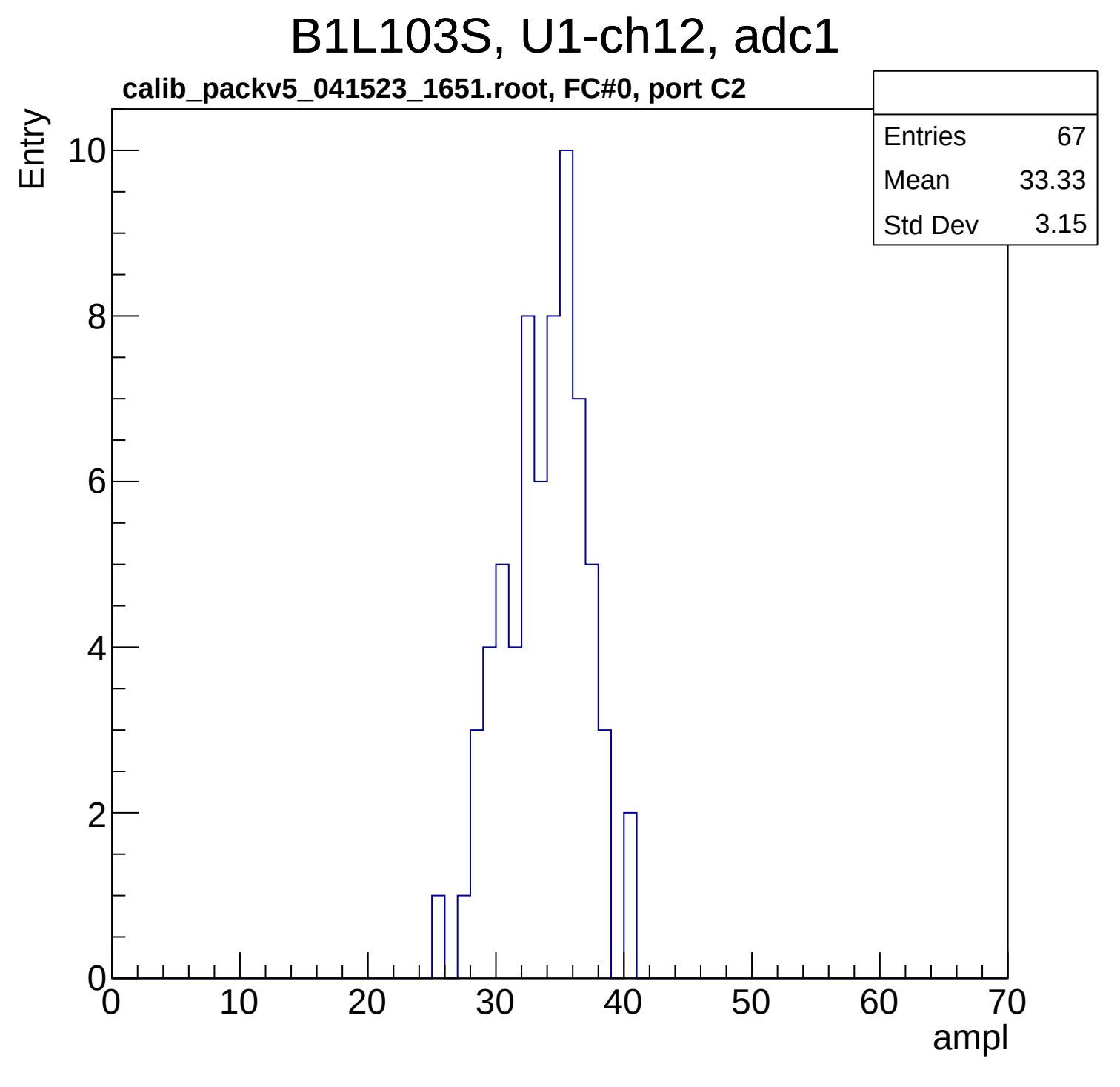
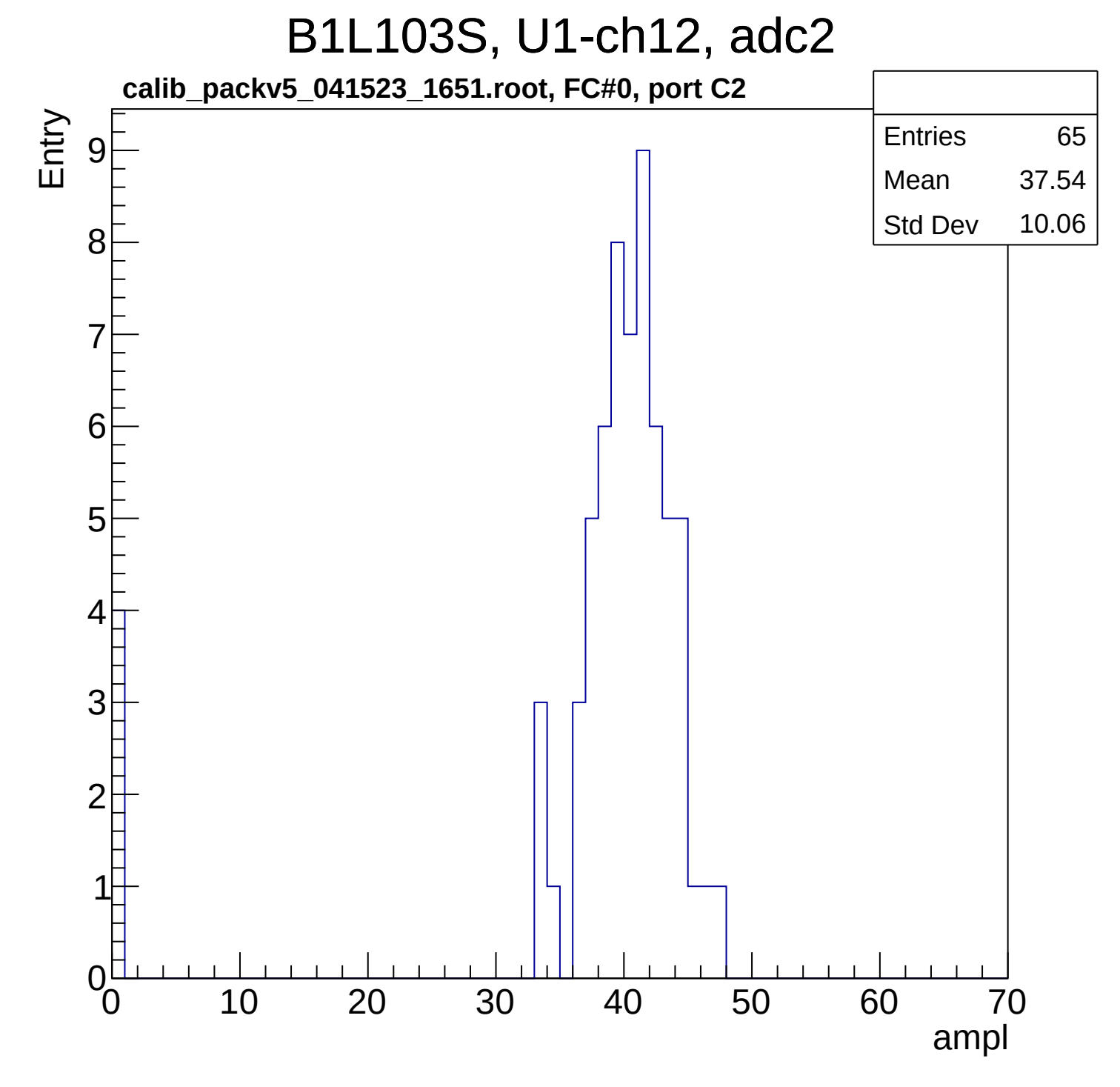
70
ampl


B1L103S, U1-ch12, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 33.33
Std Dev 3.15
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U1-ch12, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 37.54
Std Dev 10.06
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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60
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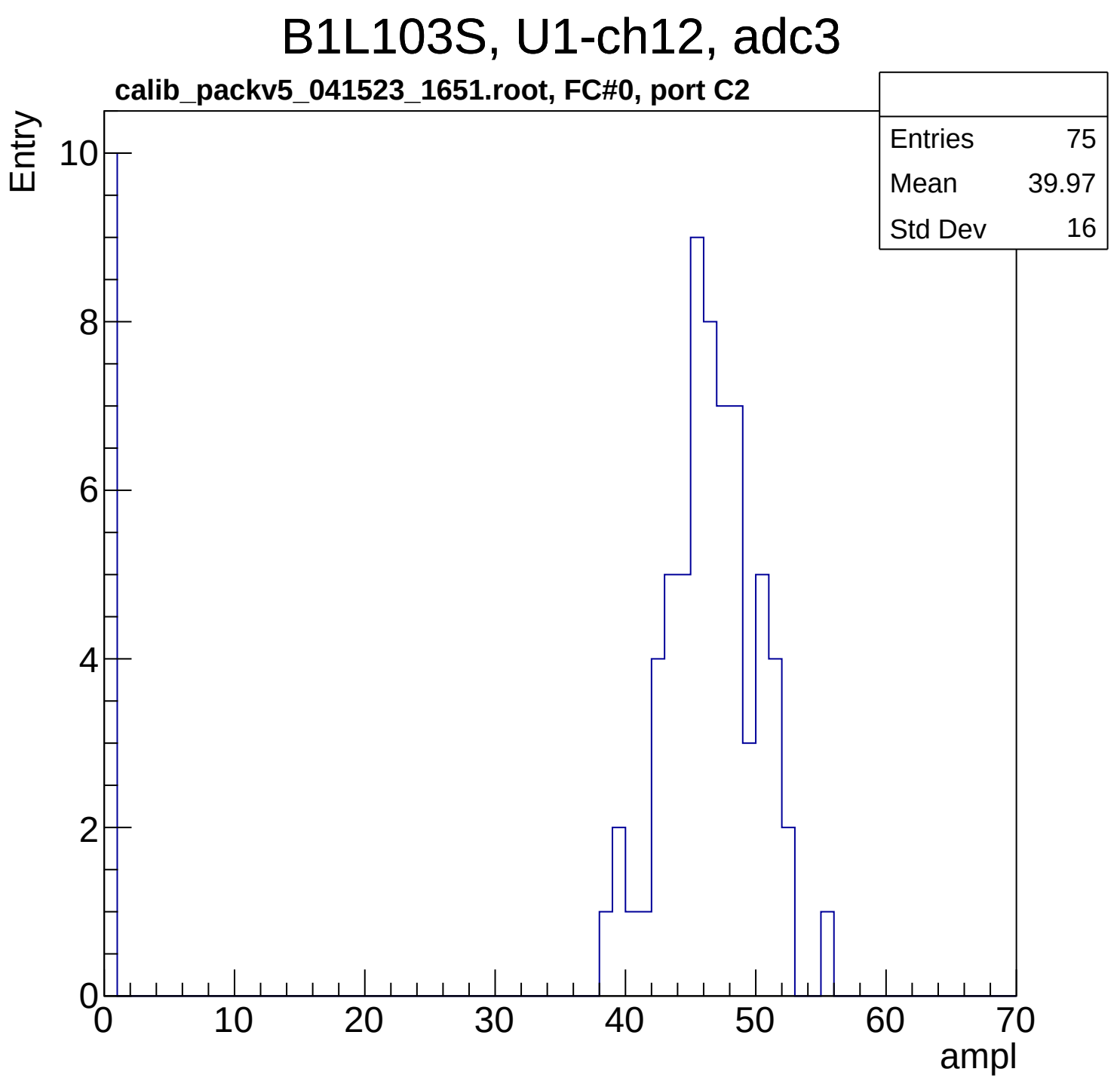
B1L103S, U1-ch12, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 39.97
Std Dev 16
Entry
ampl
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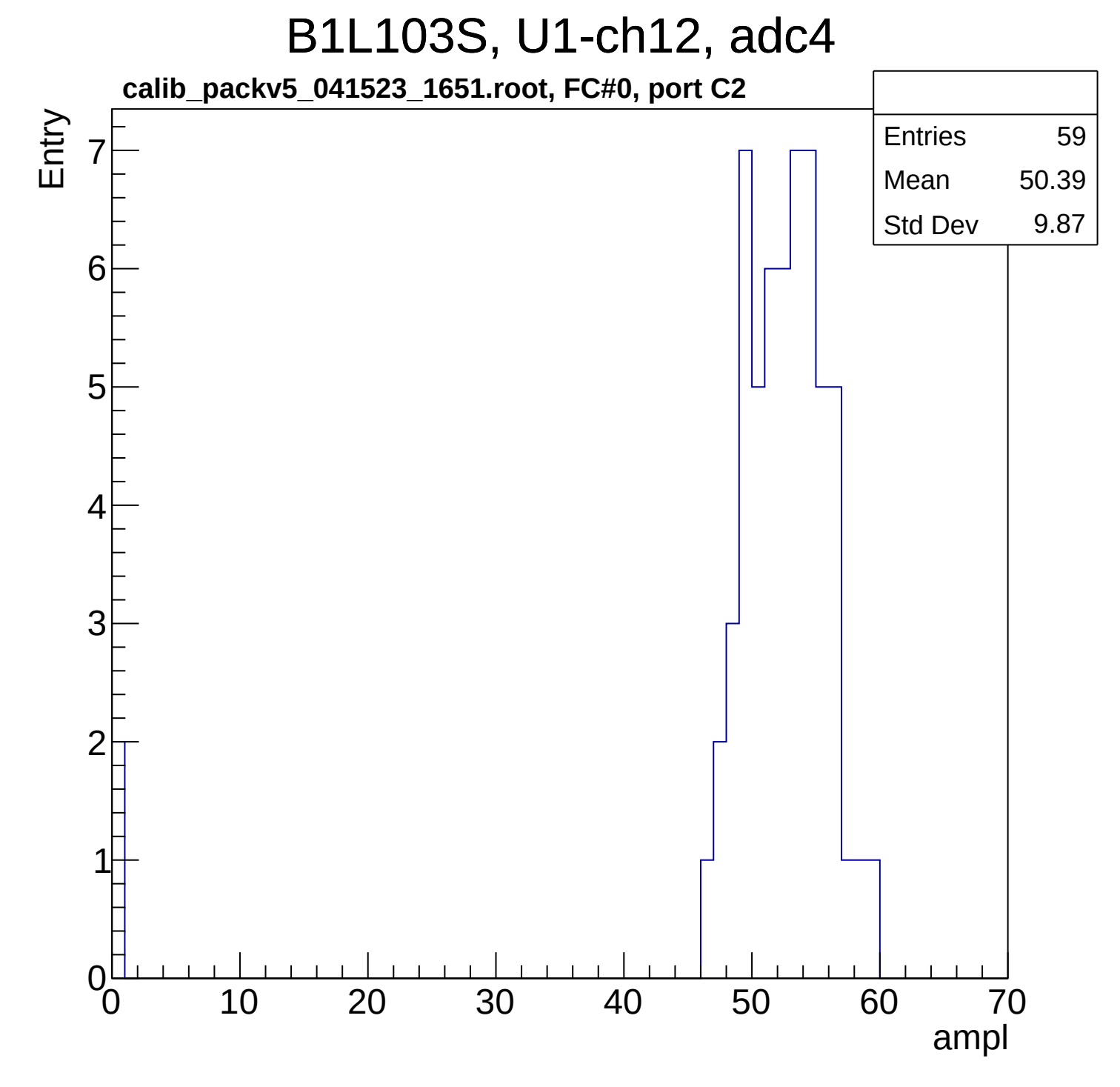
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U1-ch12, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 50.39
Std Dev 9.87
Entry
ampl
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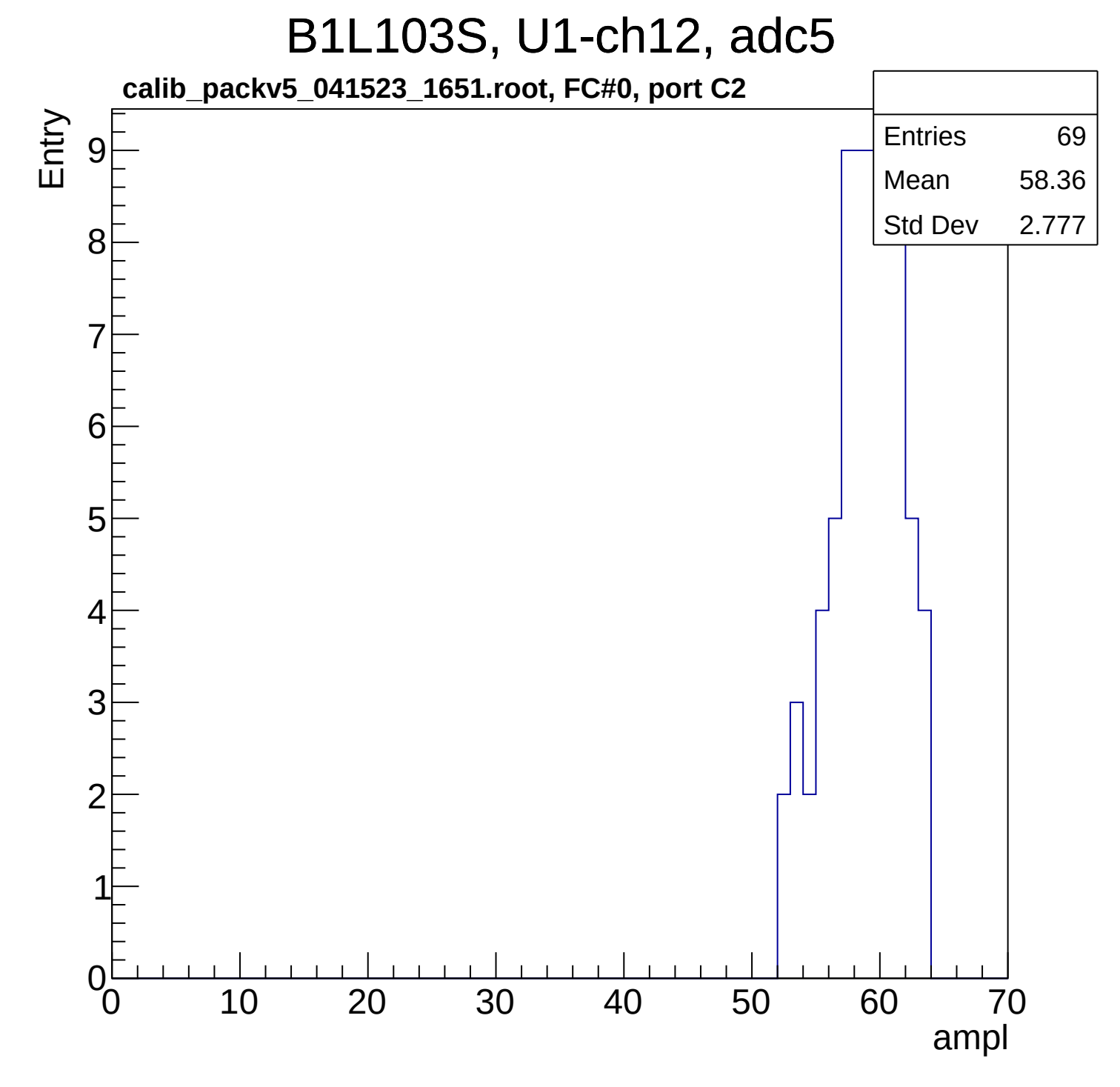
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U1-ch12, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 58.36
Std Dev 2.777
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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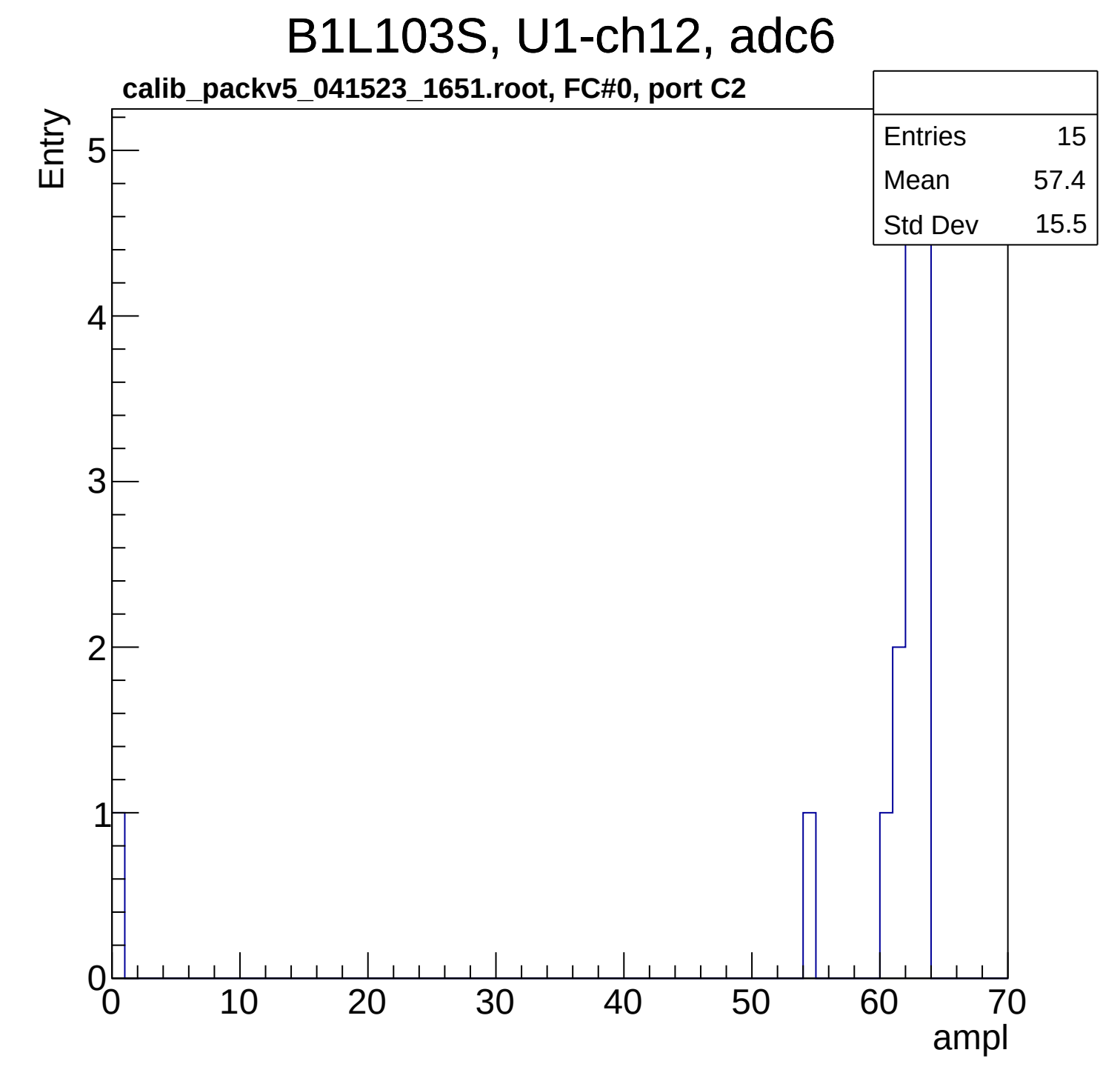
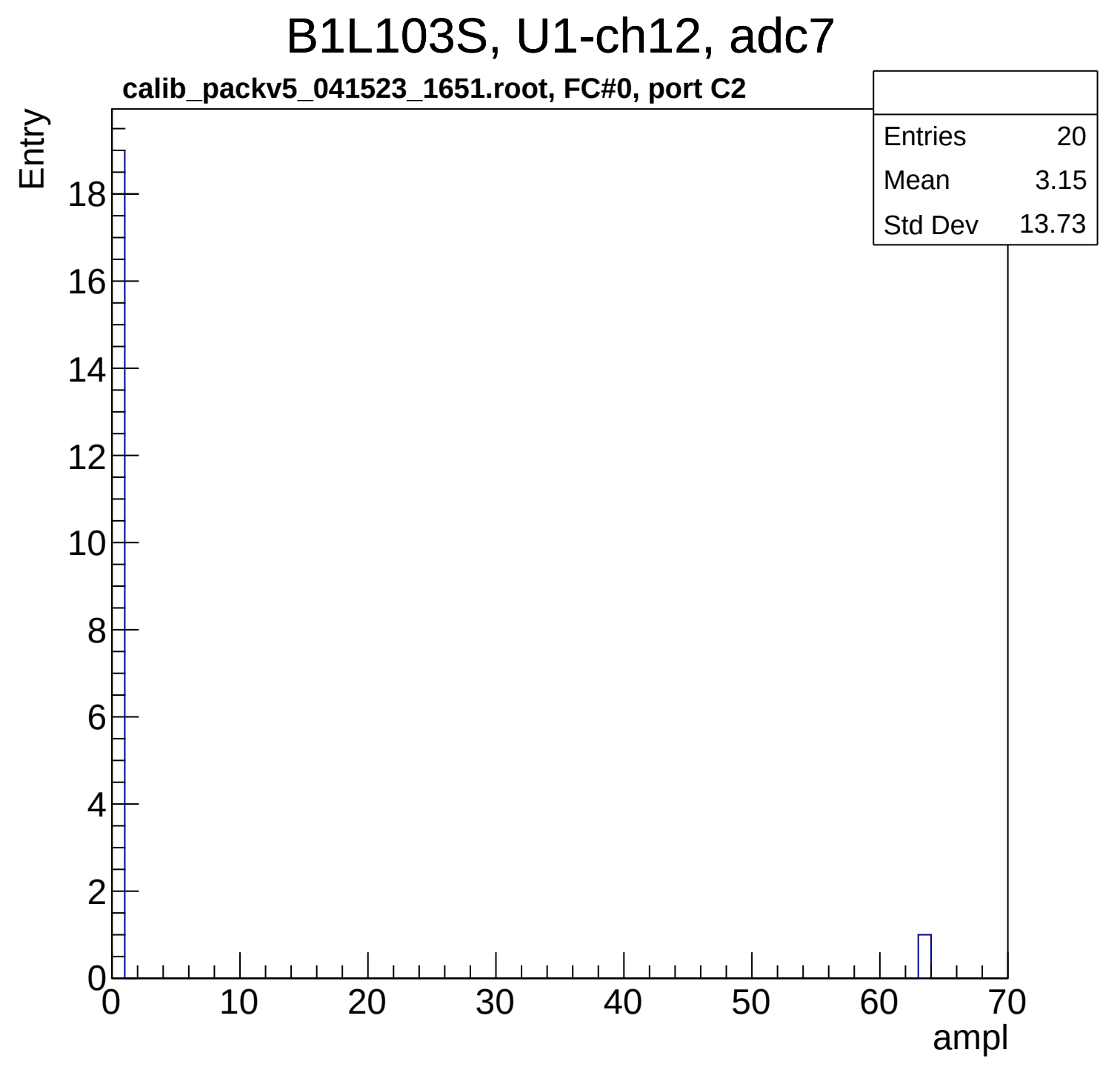
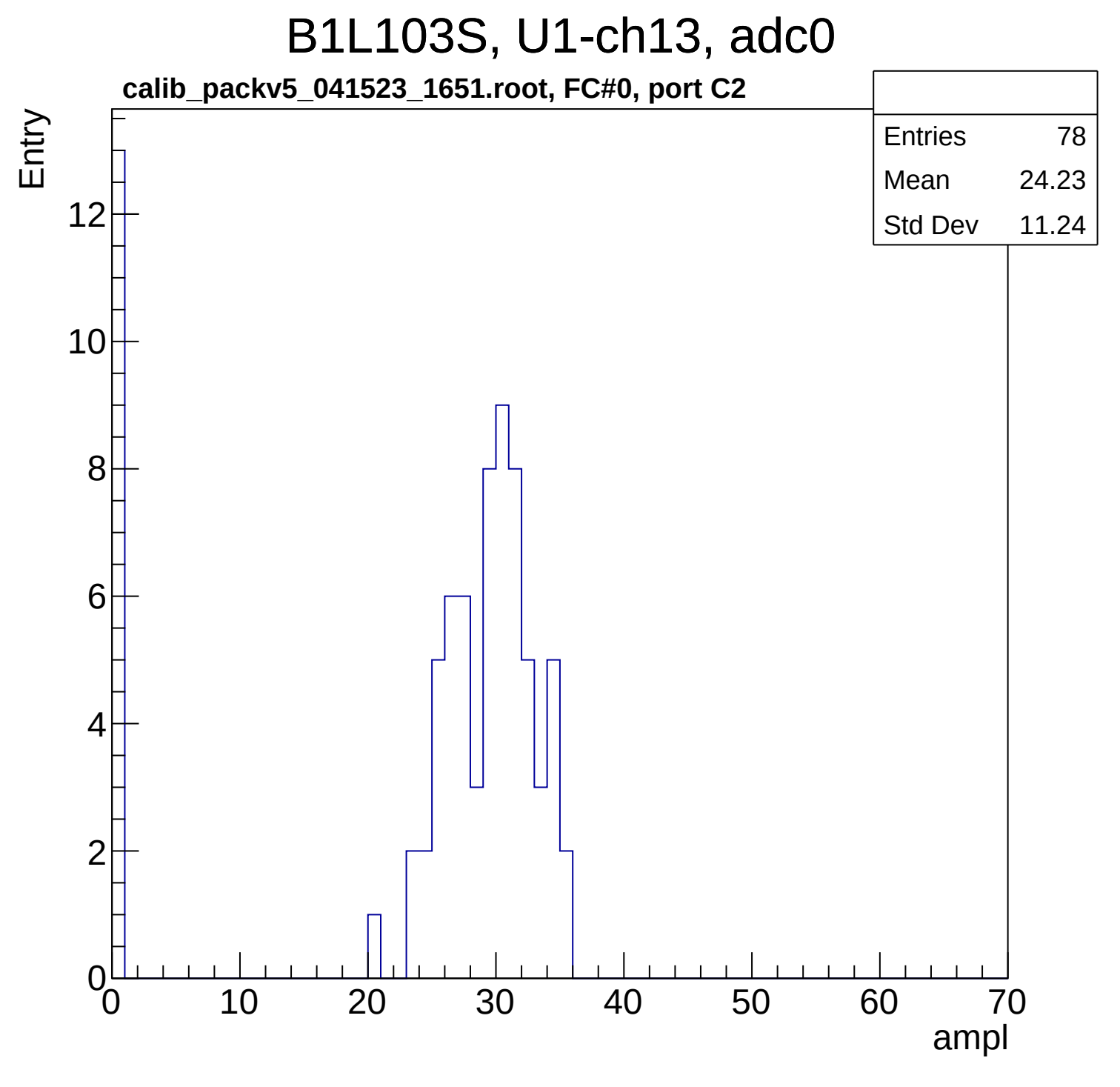

B1L103S, U1-ch12, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 15
Mean 57.4
Std Dev 15.5
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch12, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch13, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 24.23
Std Dev 11.24
Entry
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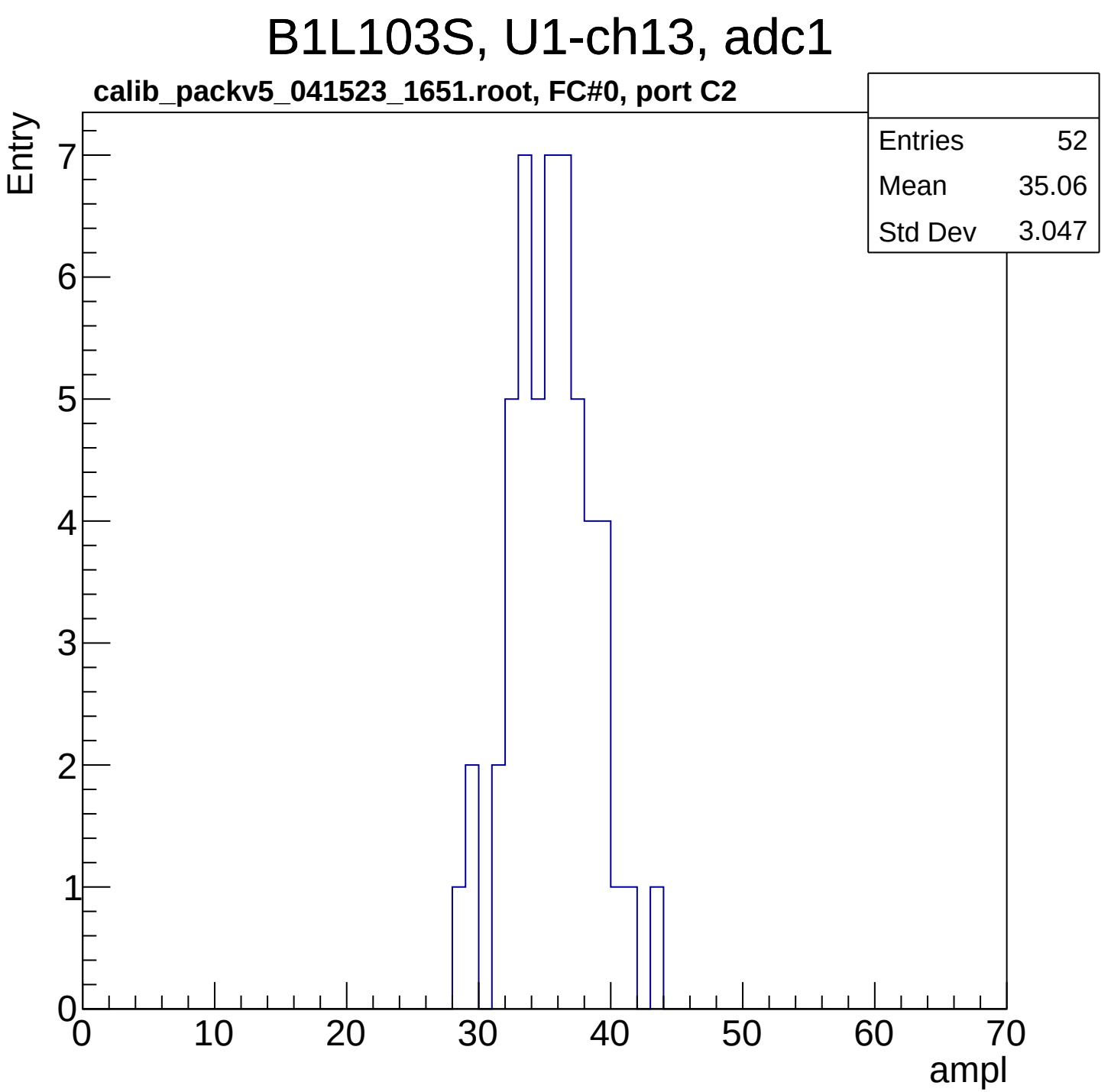
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch13, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 35.06
Std Dev 3.047
Entry
ampl
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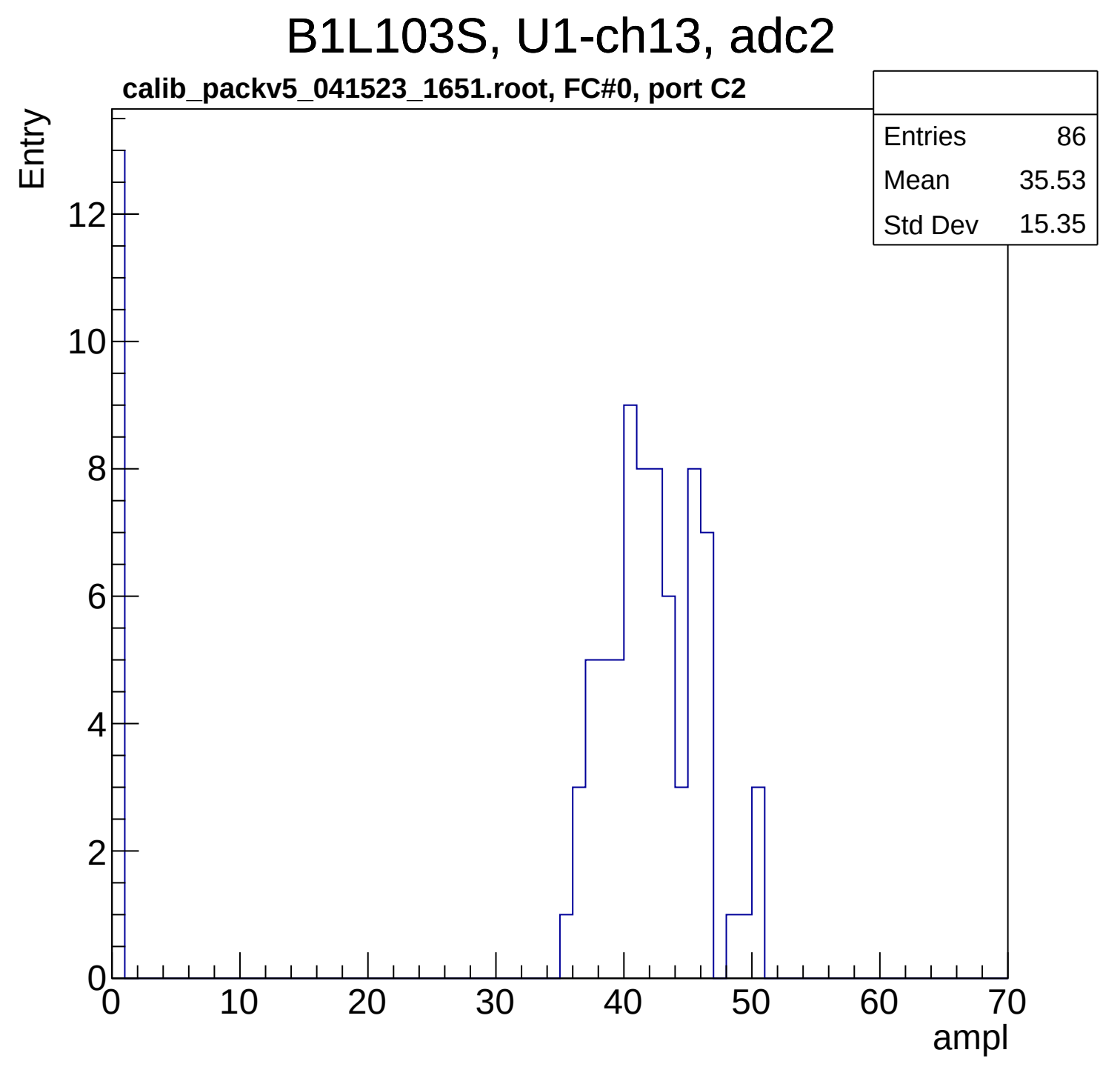
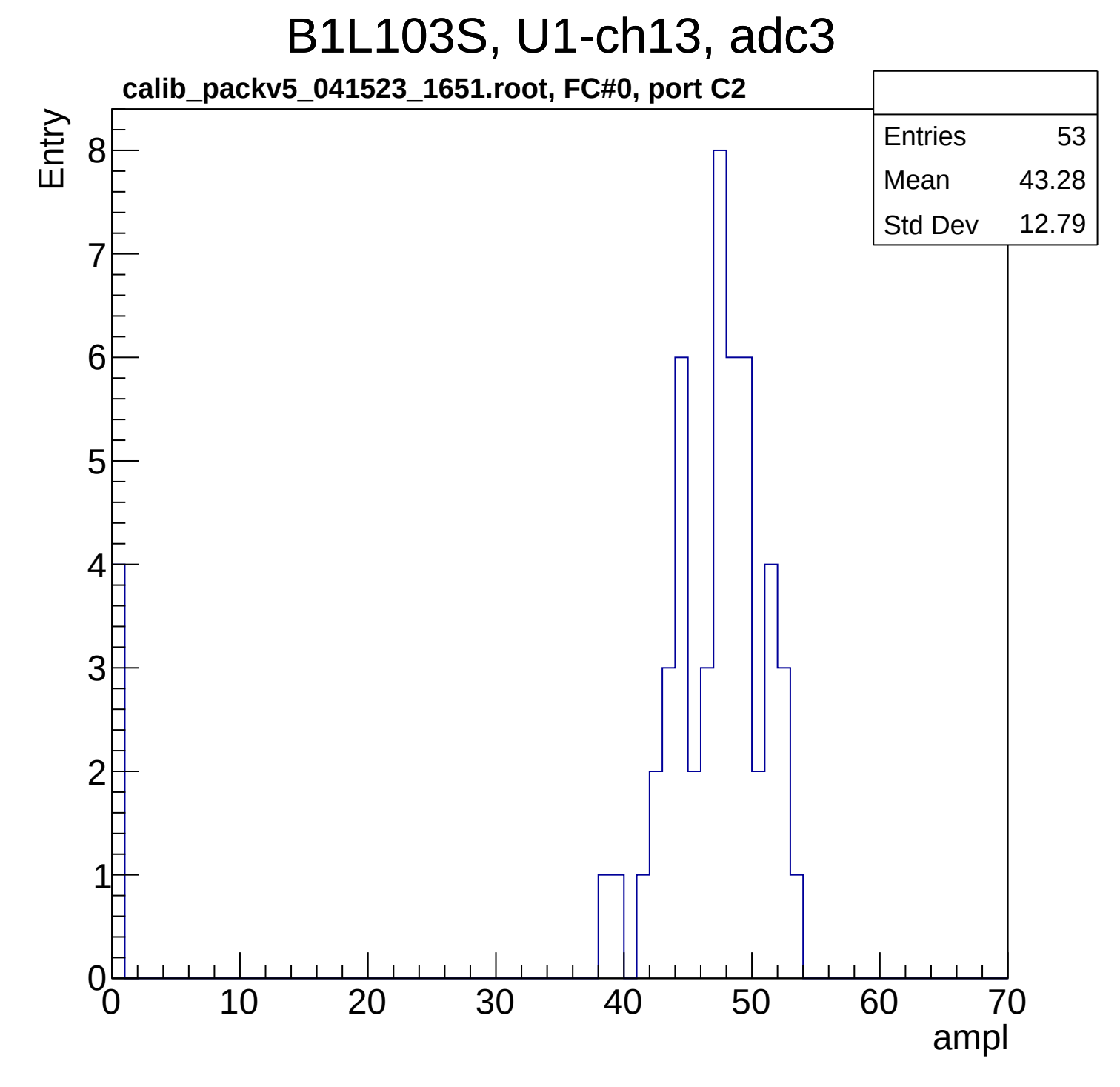
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U1-ch13, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 35.53
Std Dev 15.35
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch13, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 43.28
Std Dev 12.79
Entry
ampl
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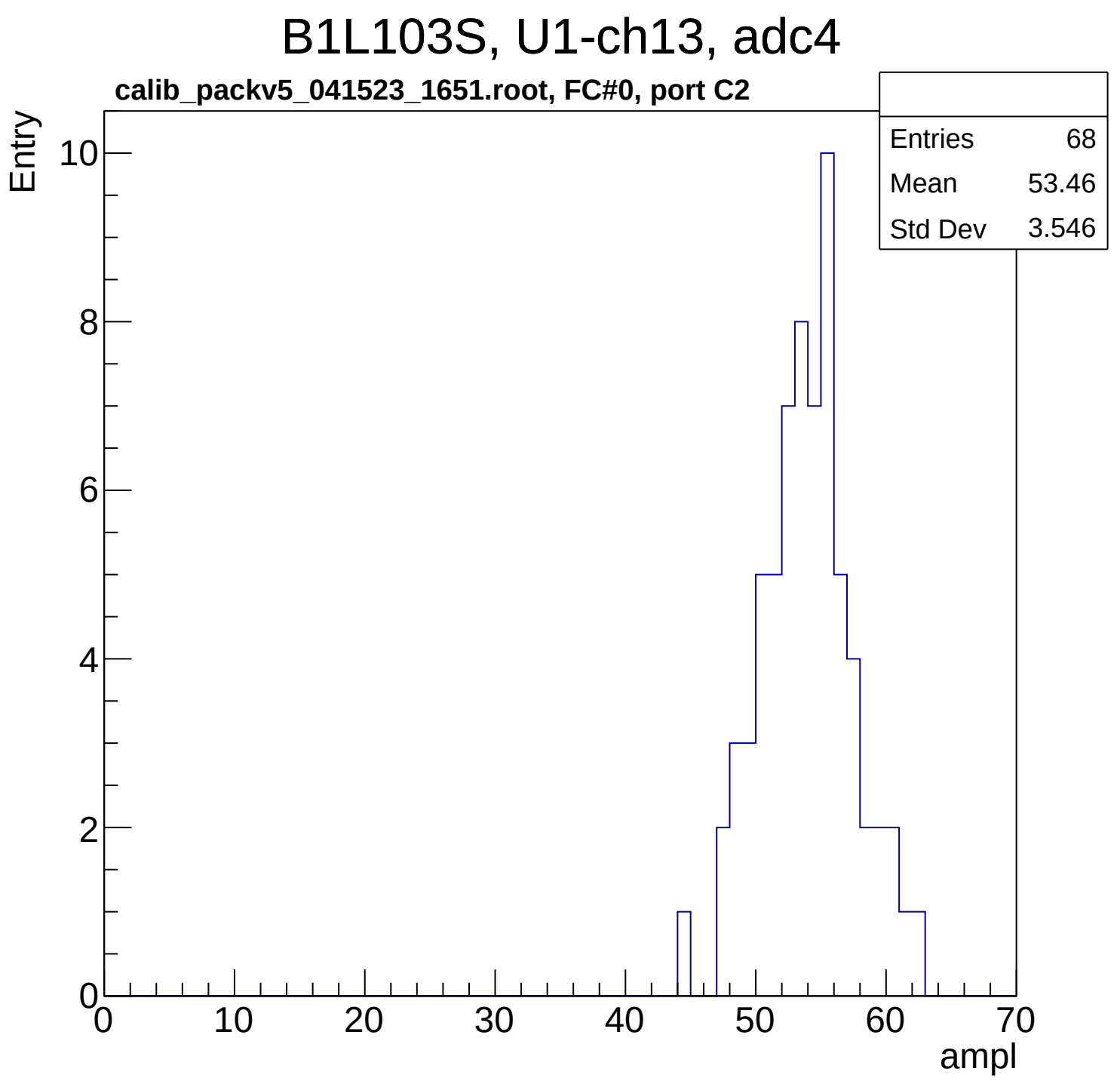
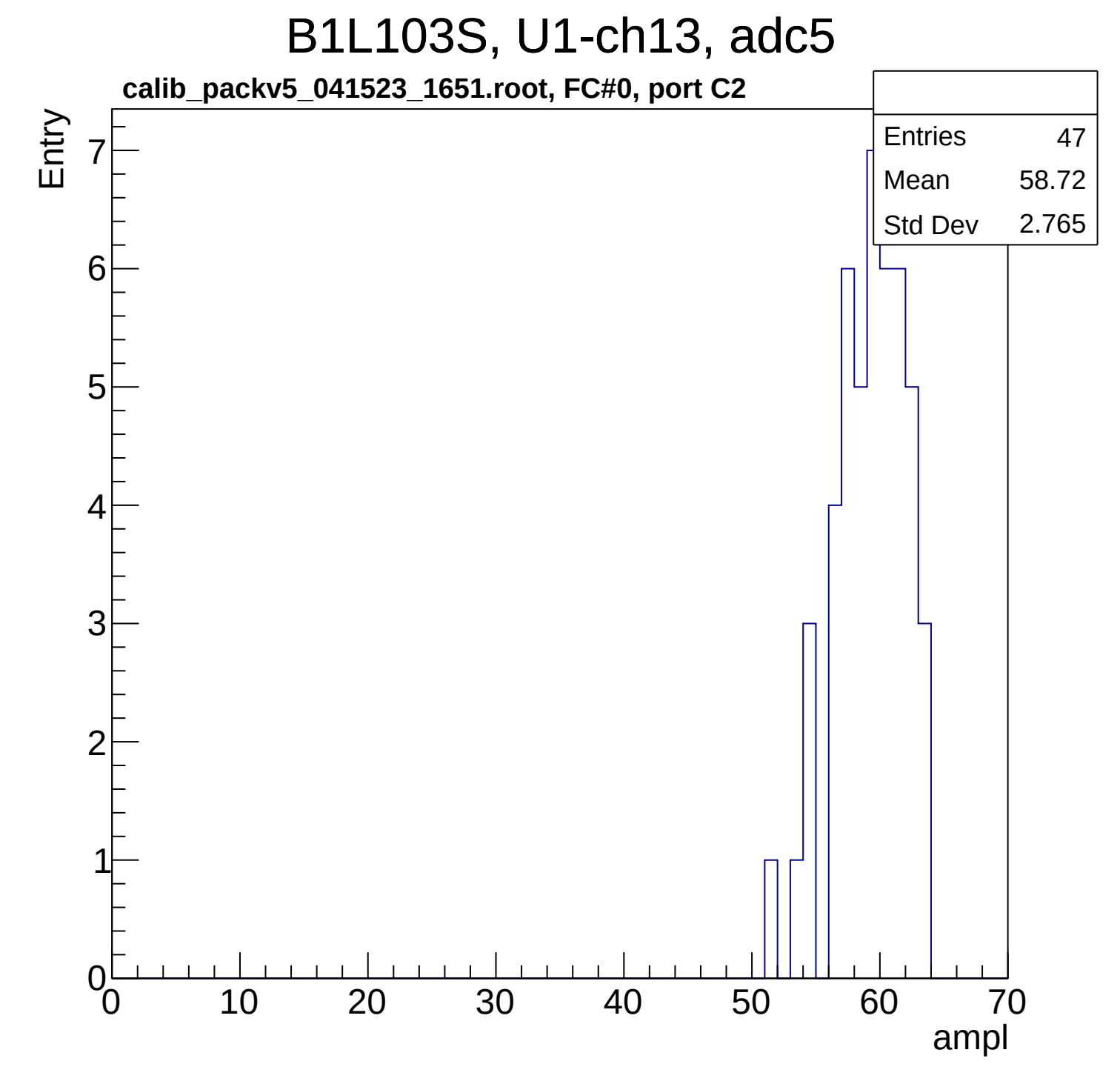
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U1-ch13, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 53.46
Std Dev 3.546
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U1-ch13, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 58.72
Std Dev 2.765
Entry
ampl
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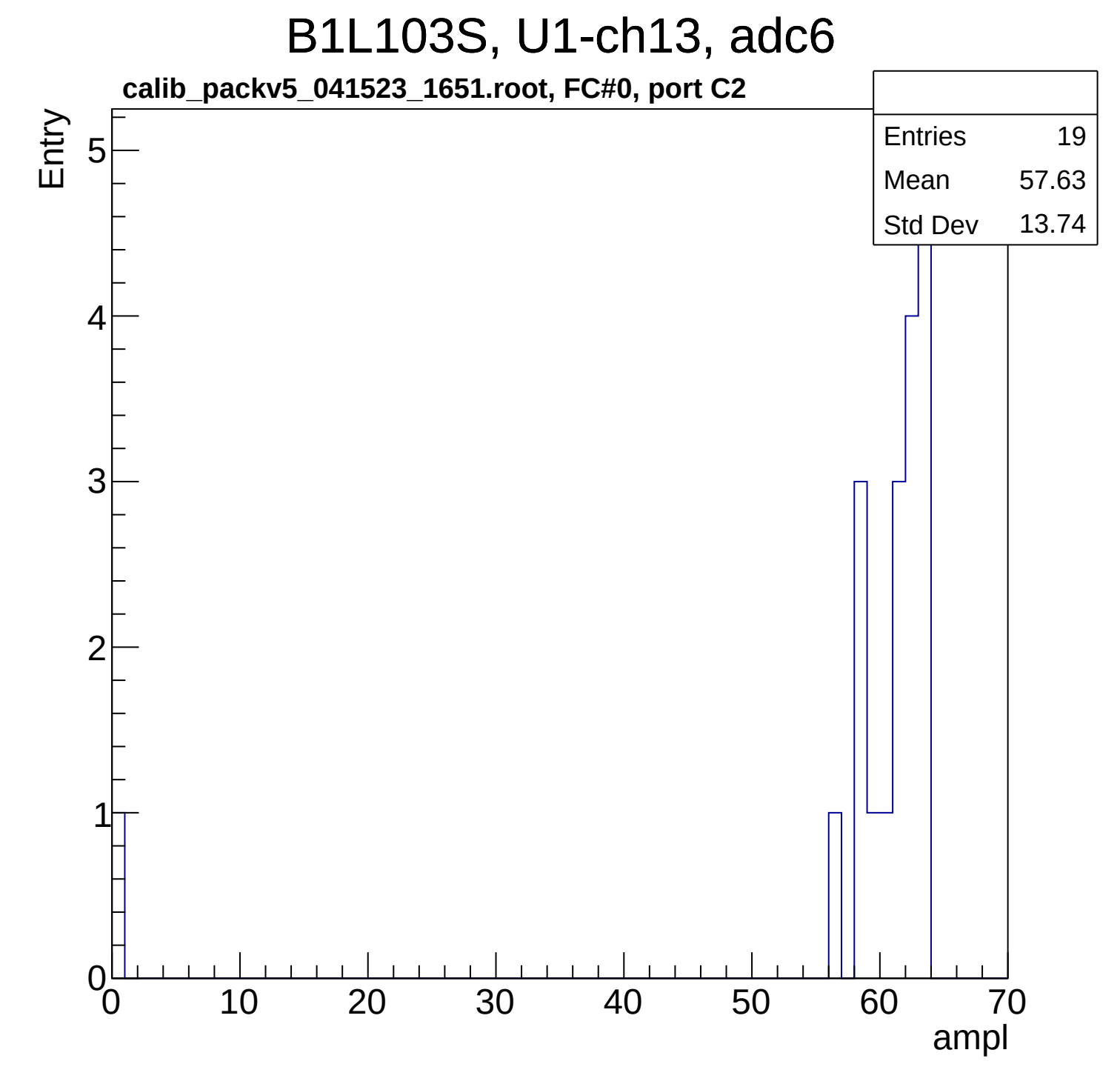
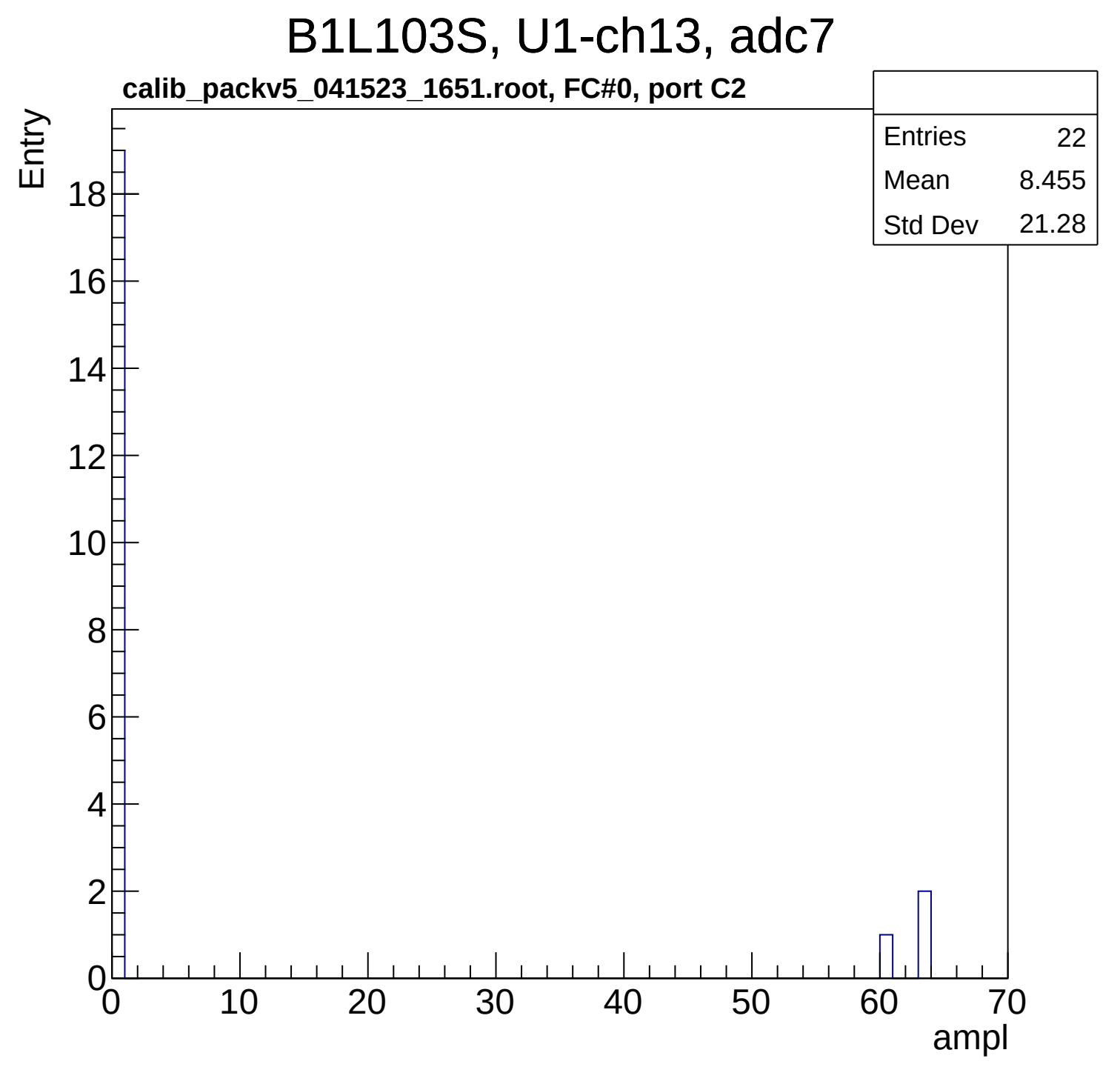
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U1-ch13, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 57.63
Std Dev 13.74
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U1-ch13, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 8.455
Std Dev 21.28
Entry
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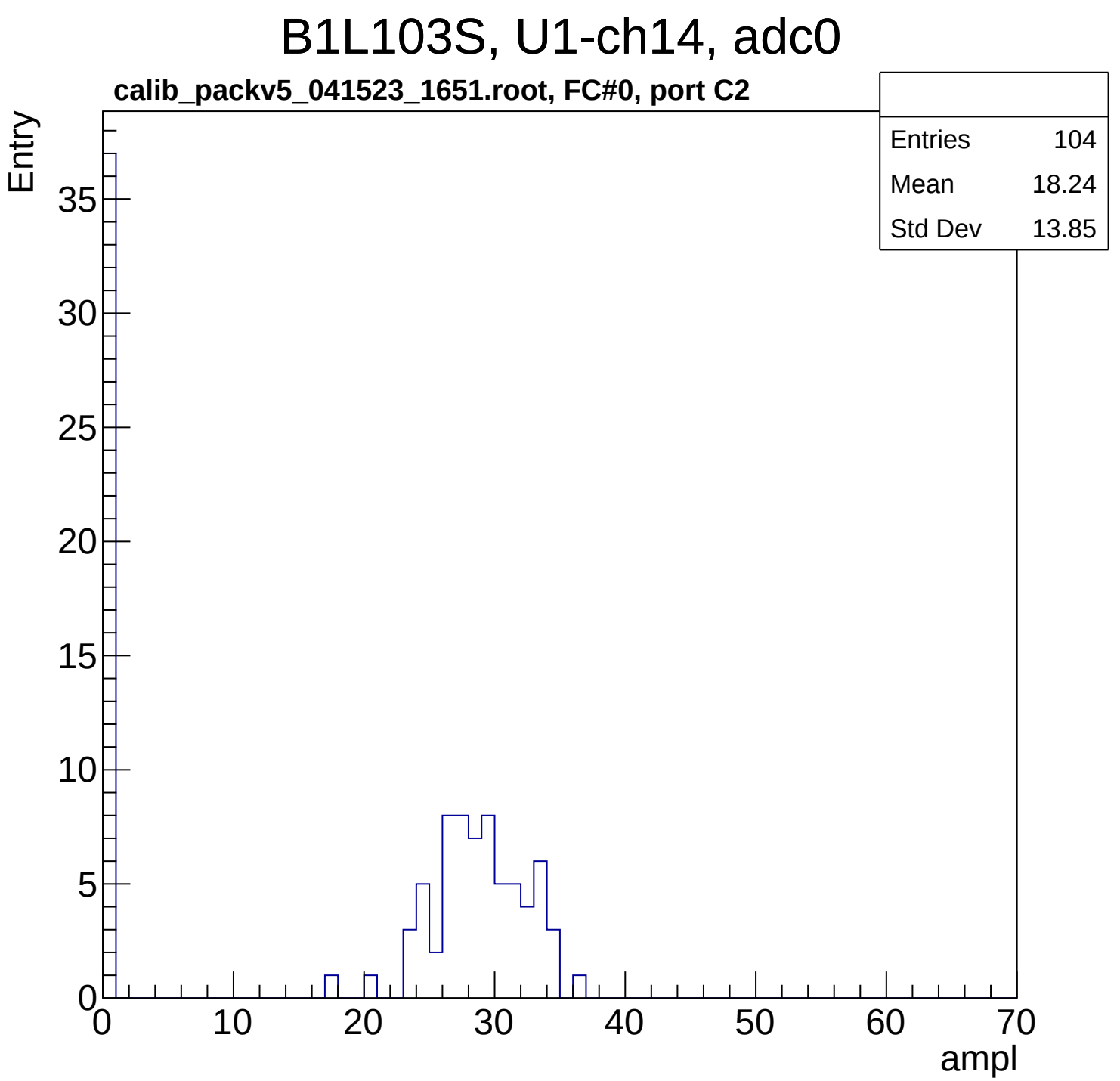
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch14, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 104
Mean 18.24
Std Dev 13.85
Entry
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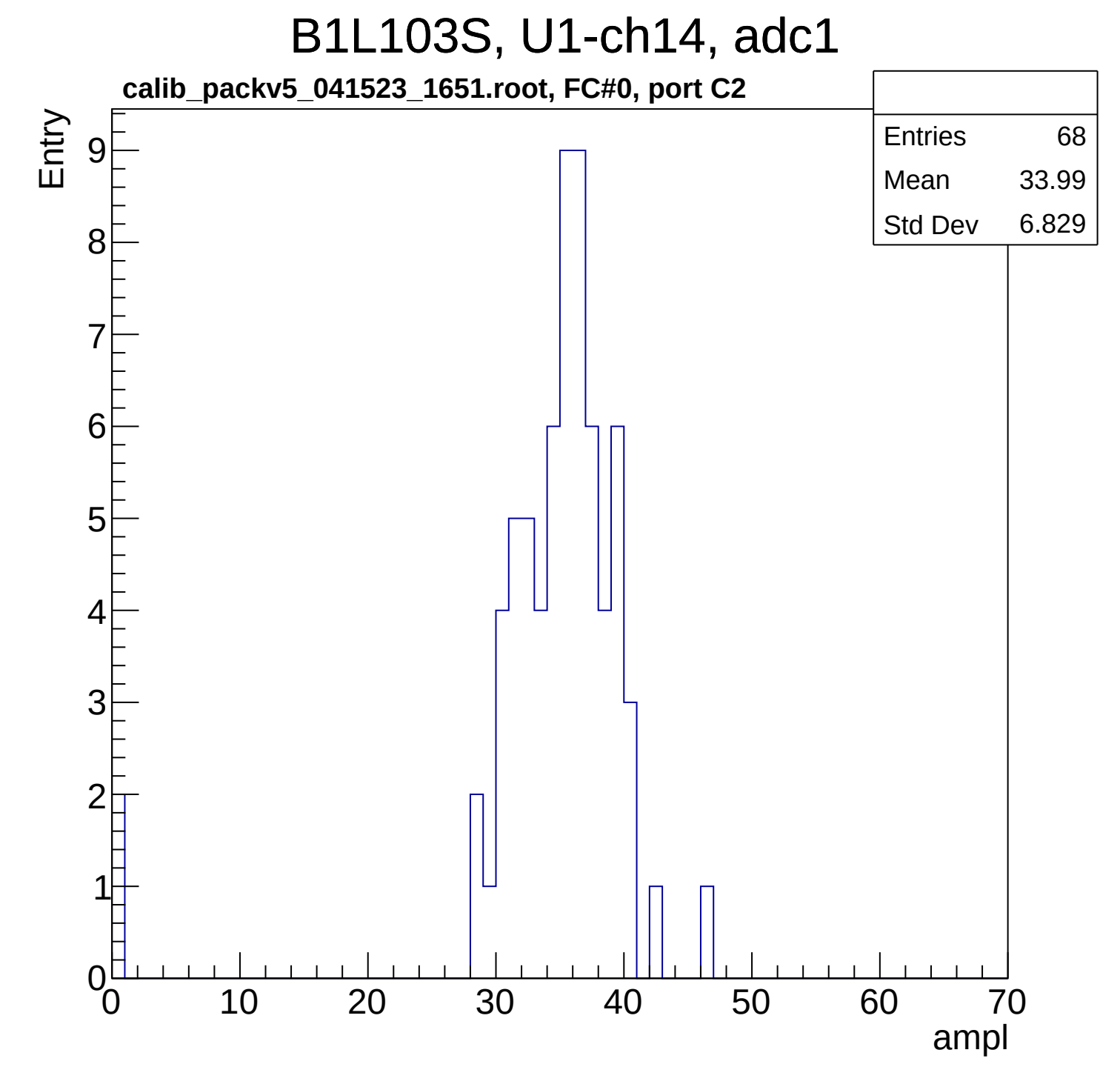
5
10
15
20
25
30
35
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch14, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 33.99
Std Dev 6.829
Entry
ampl
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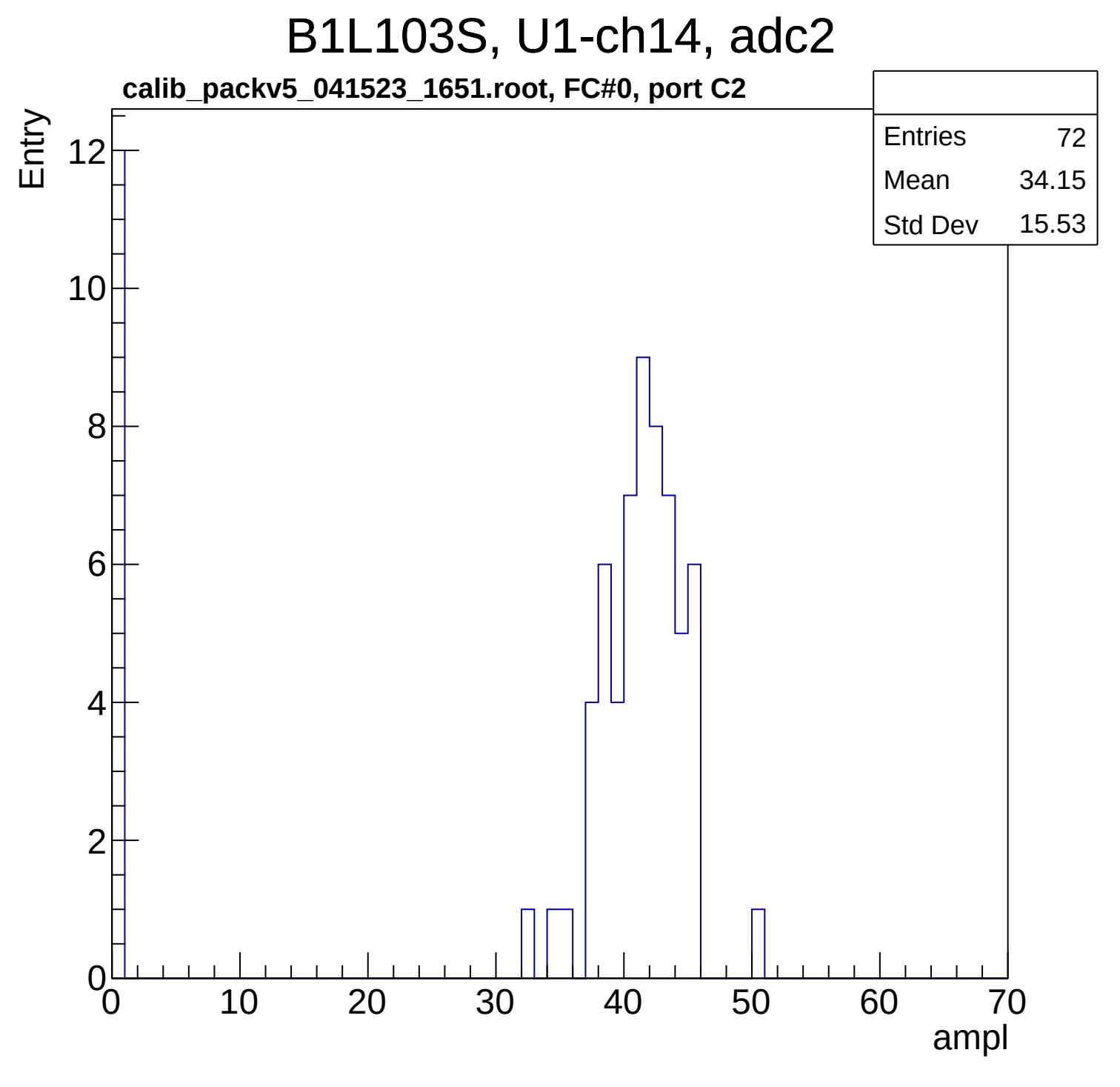
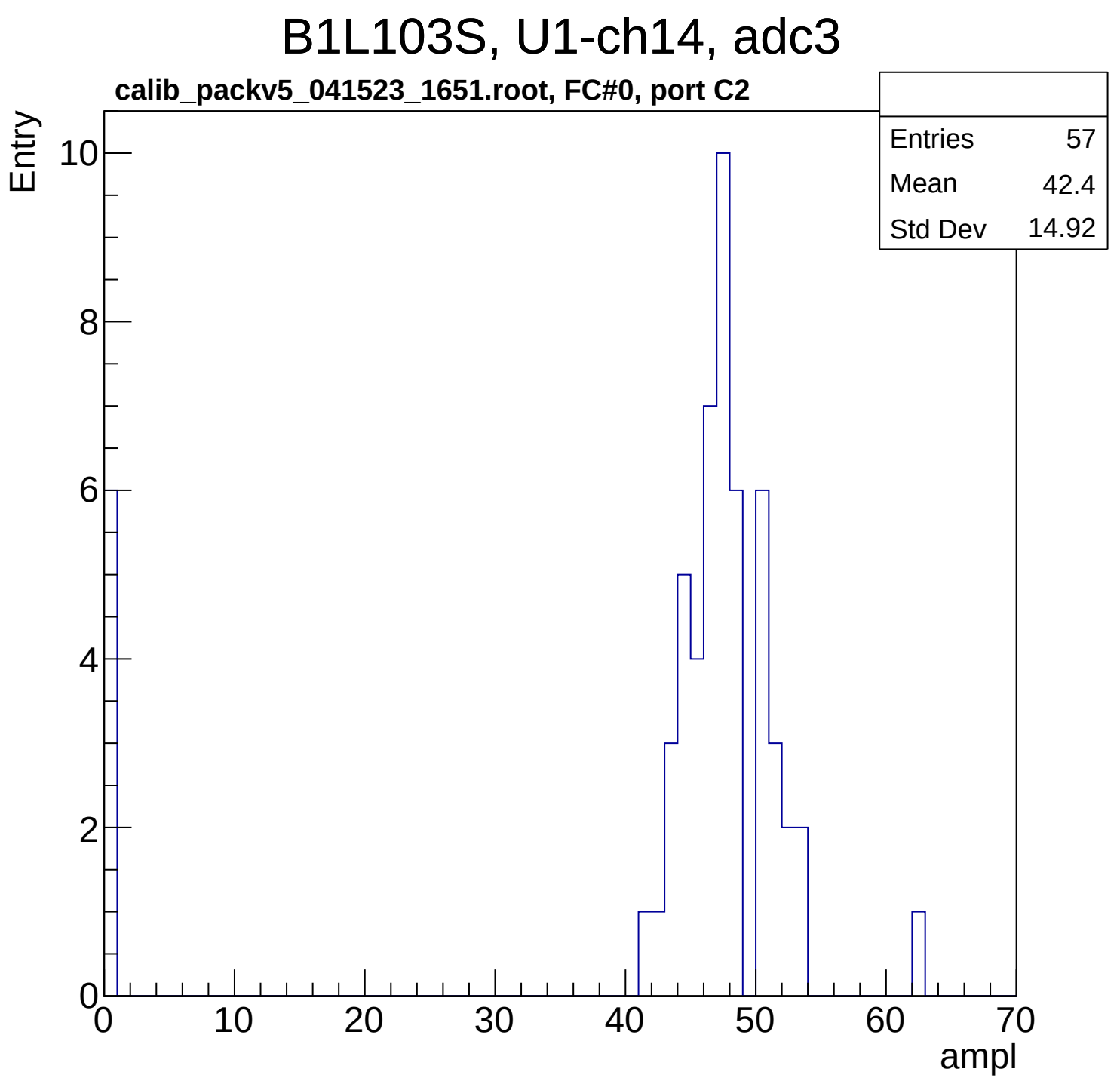
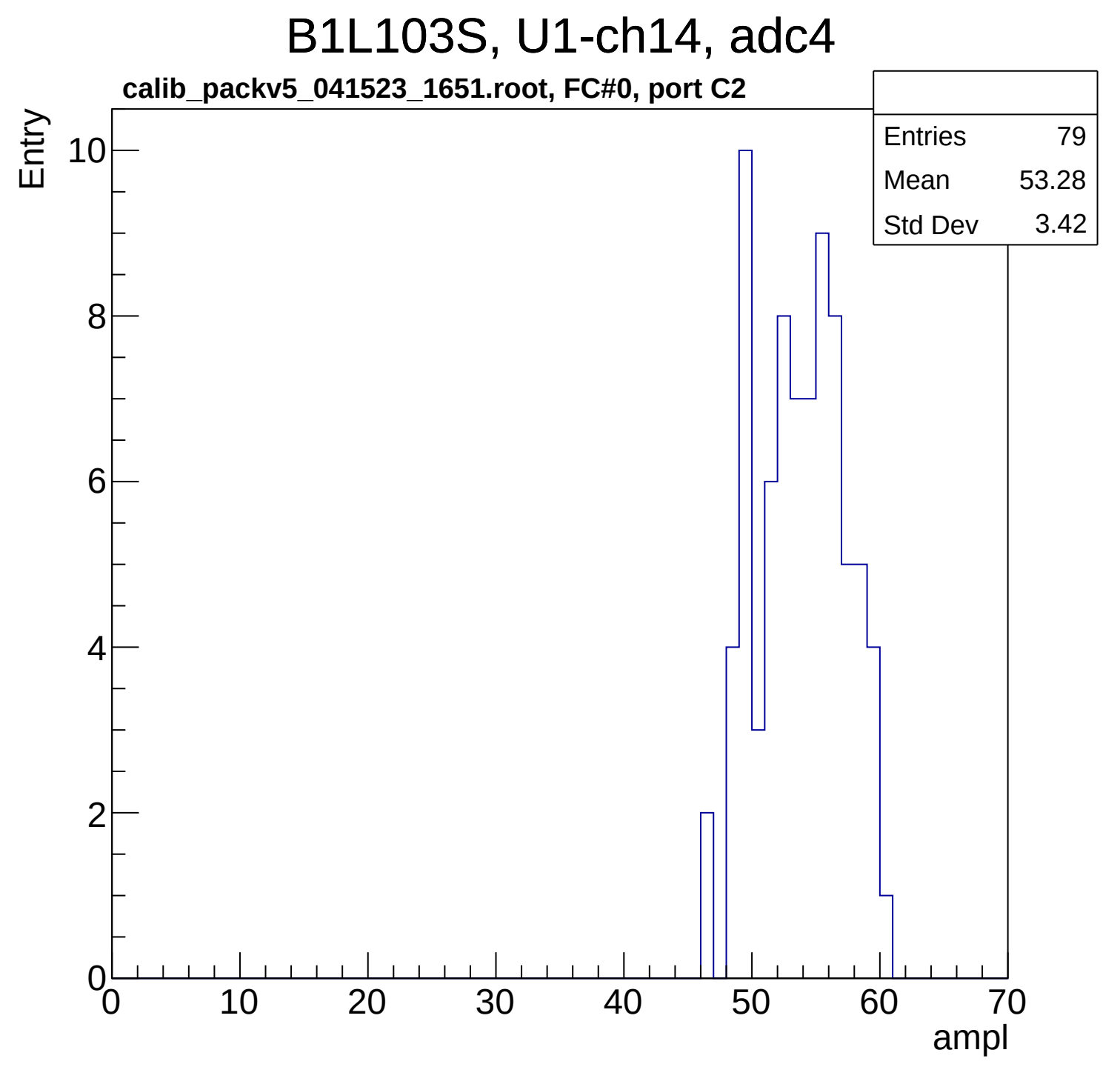
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U1-ch14, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 34.15
Std Dev 15.53
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch14, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 42.4
Std Dev 14.92
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch14, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 53.28
Std Dev 3.42
Entry
ampl
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2
4
6
8
10
0
10
20
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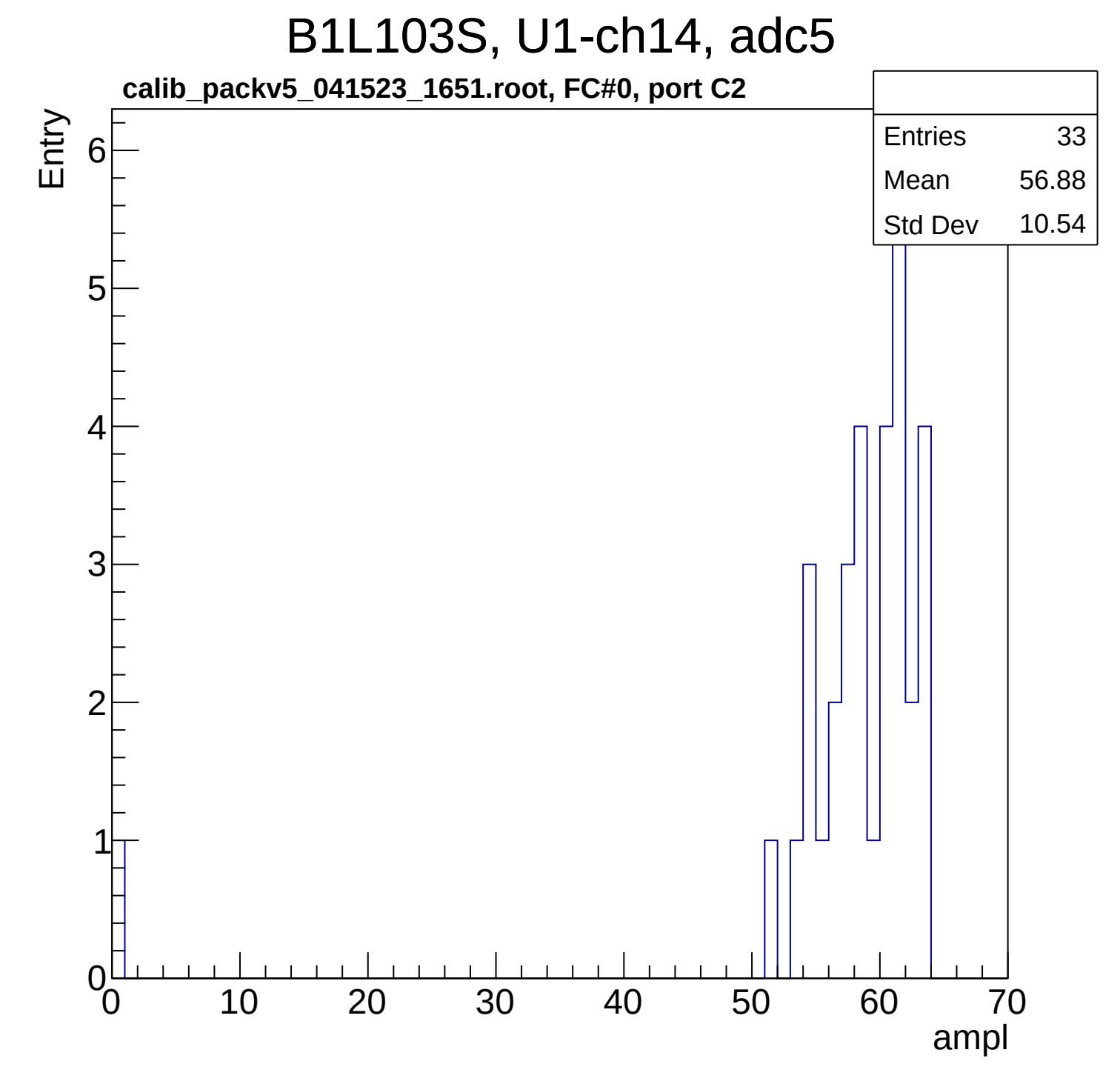
40
50
60
70


B1L103S, U1-ch14, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 33
Mean 56.88
Std Dev 10.54
Entry
ampl
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1
2
3
4
5
6
0
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20
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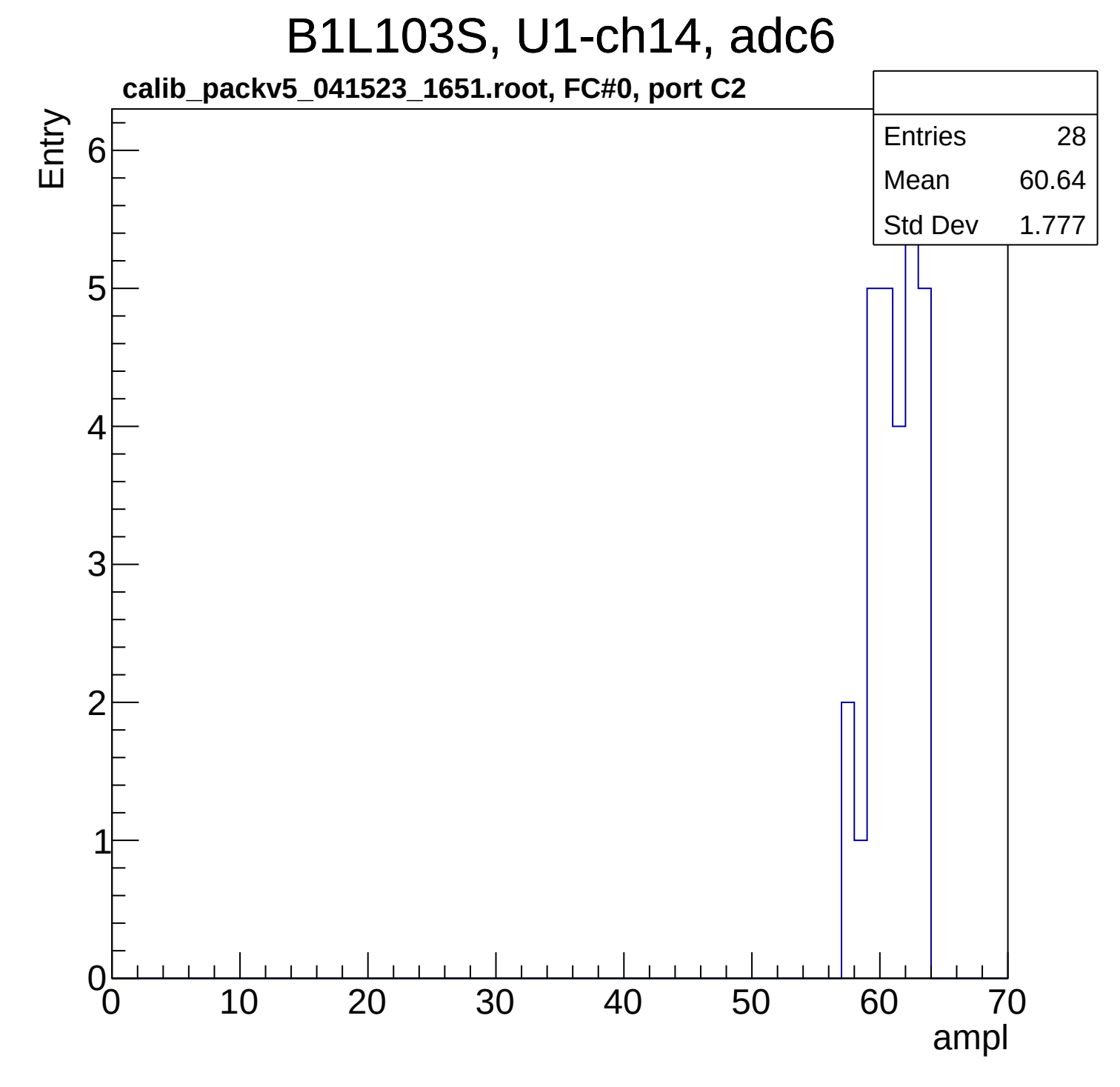
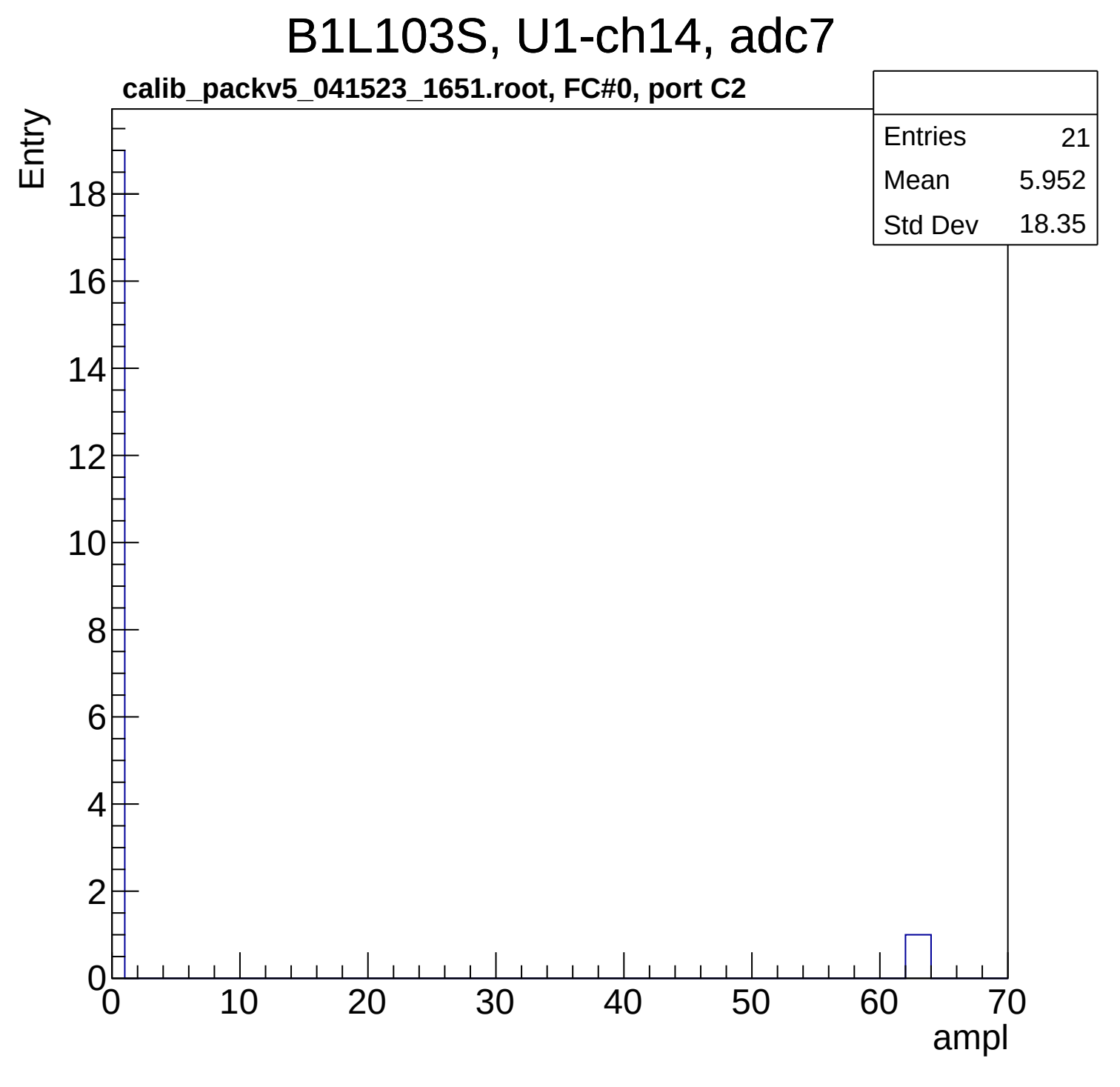
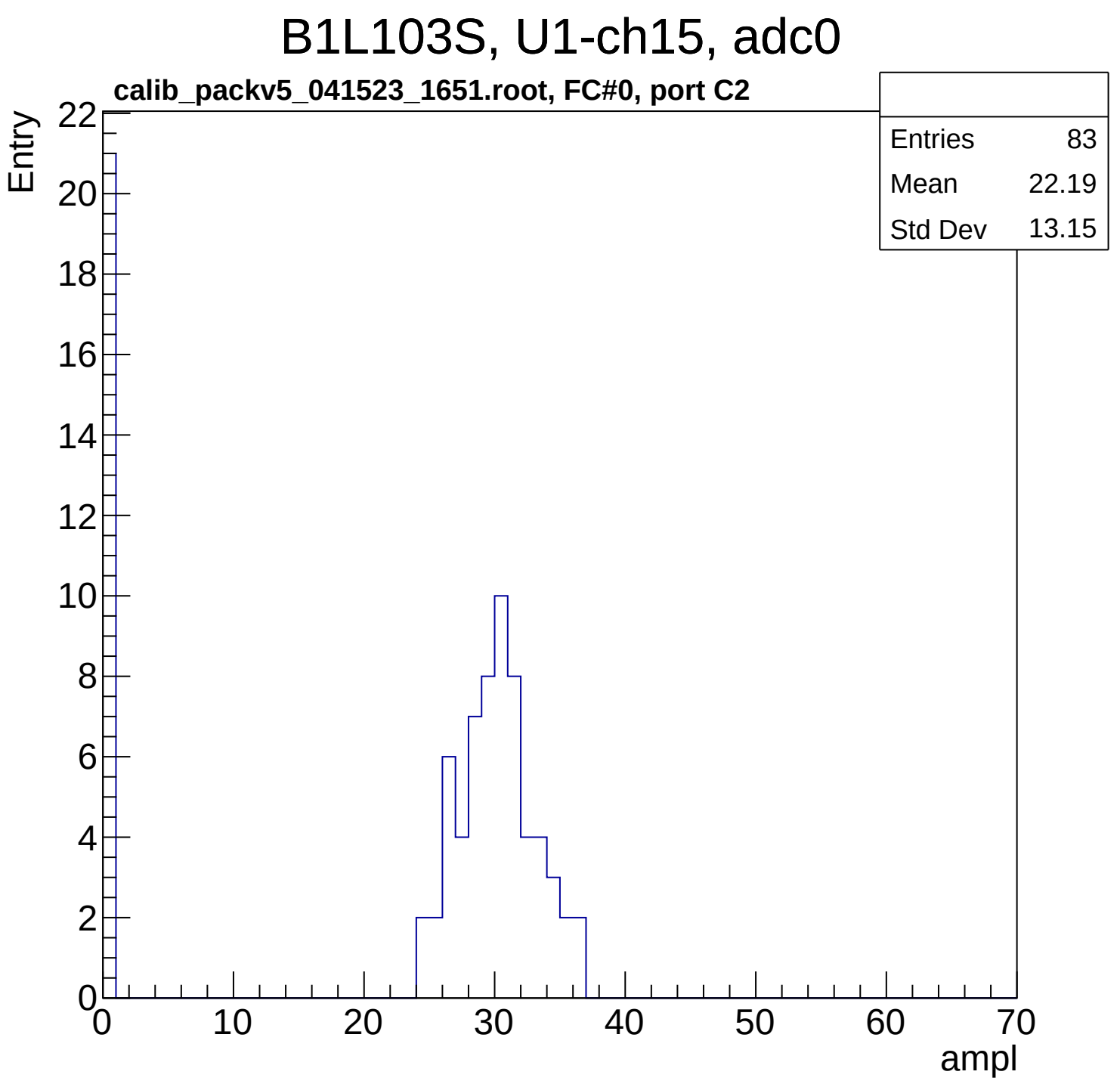
40
50
60
70


B1L103S, U1-ch14, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 28
Mean 60.64
Std Dev 1.777
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U1-ch14, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 5.952
Std Dev 18.35
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch15, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 22.19
Std Dev 13.15
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
22
0
10
20
30
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60
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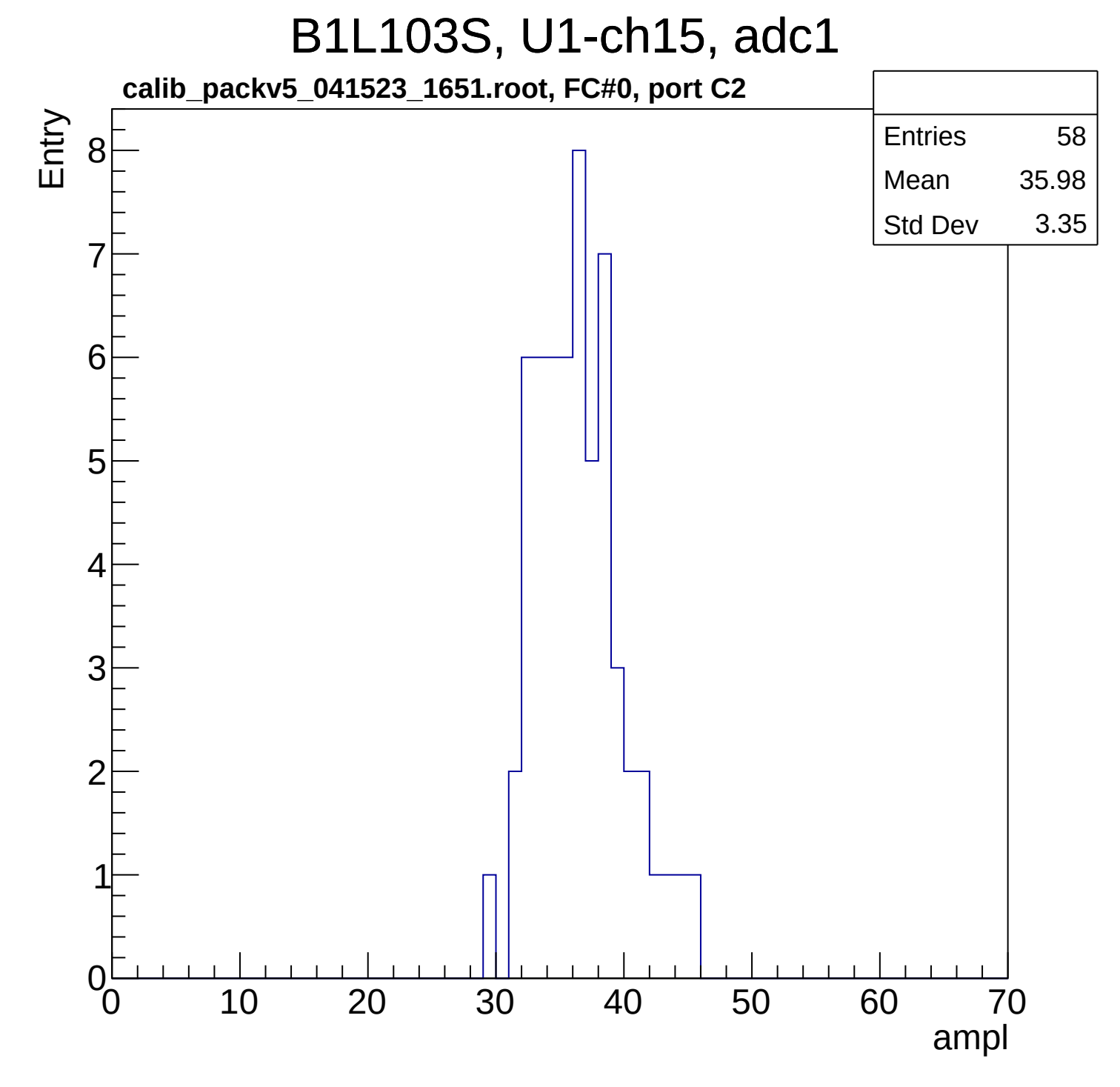
B1L103S, U1-ch15, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 35.98
Std Dev 3.35
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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60
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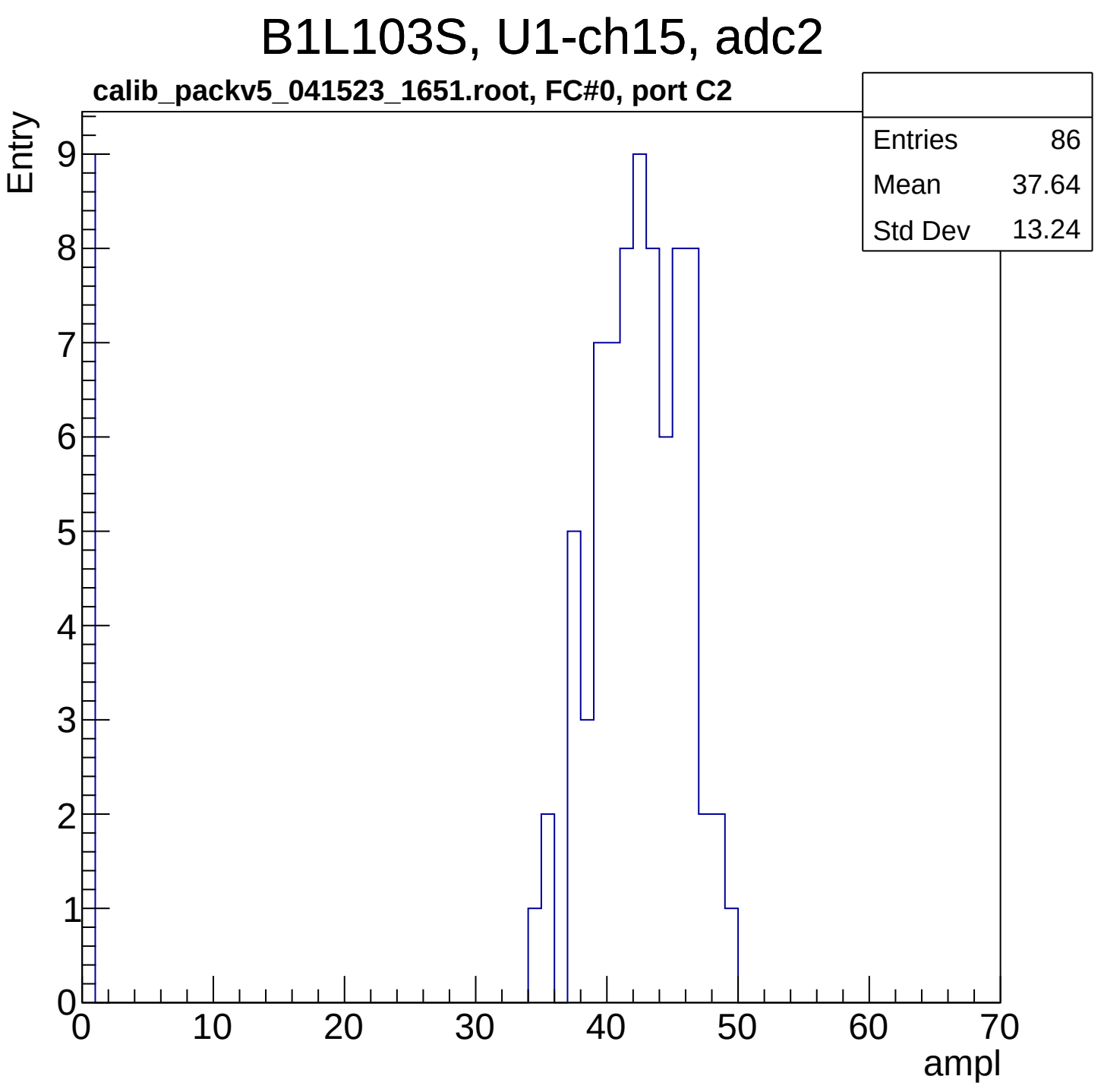
B1L103S, U1-ch15, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 37.64
Std Dev 13.24
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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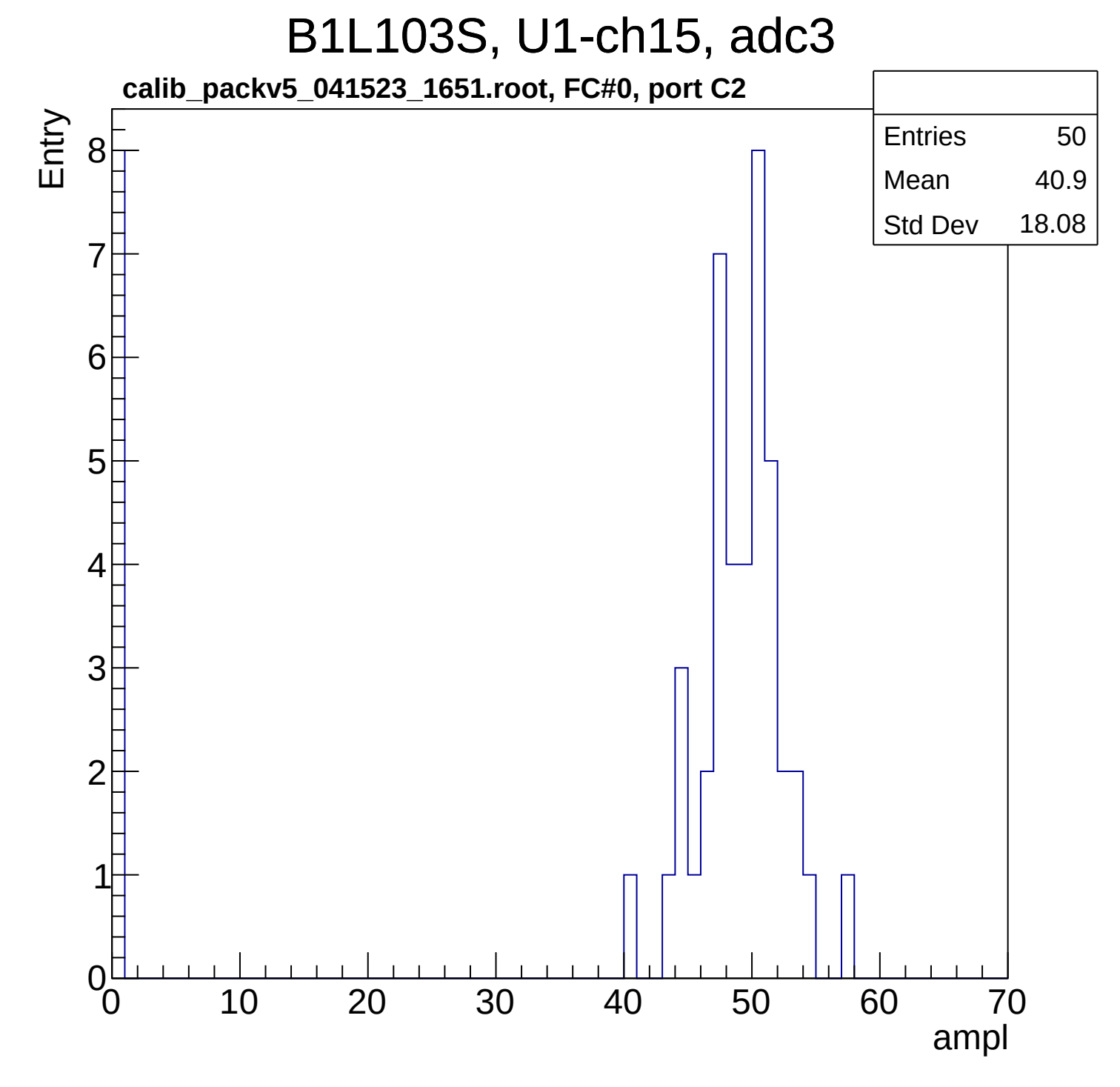
B1L103S, U1-ch15, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 40.9
Std Dev 18.08
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
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60
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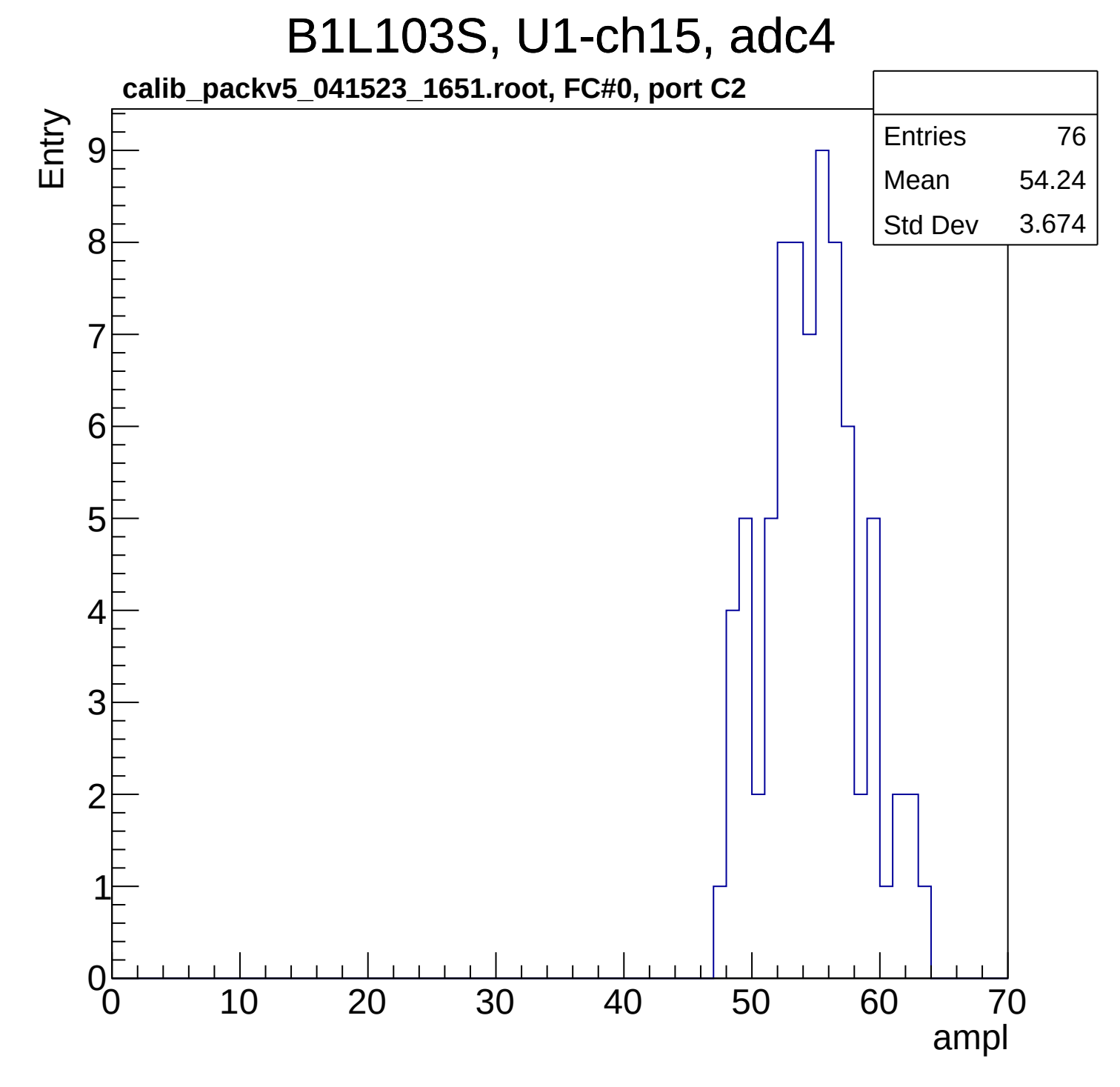
B1L103S, U1-ch15, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 54.24
Std Dev 3.674
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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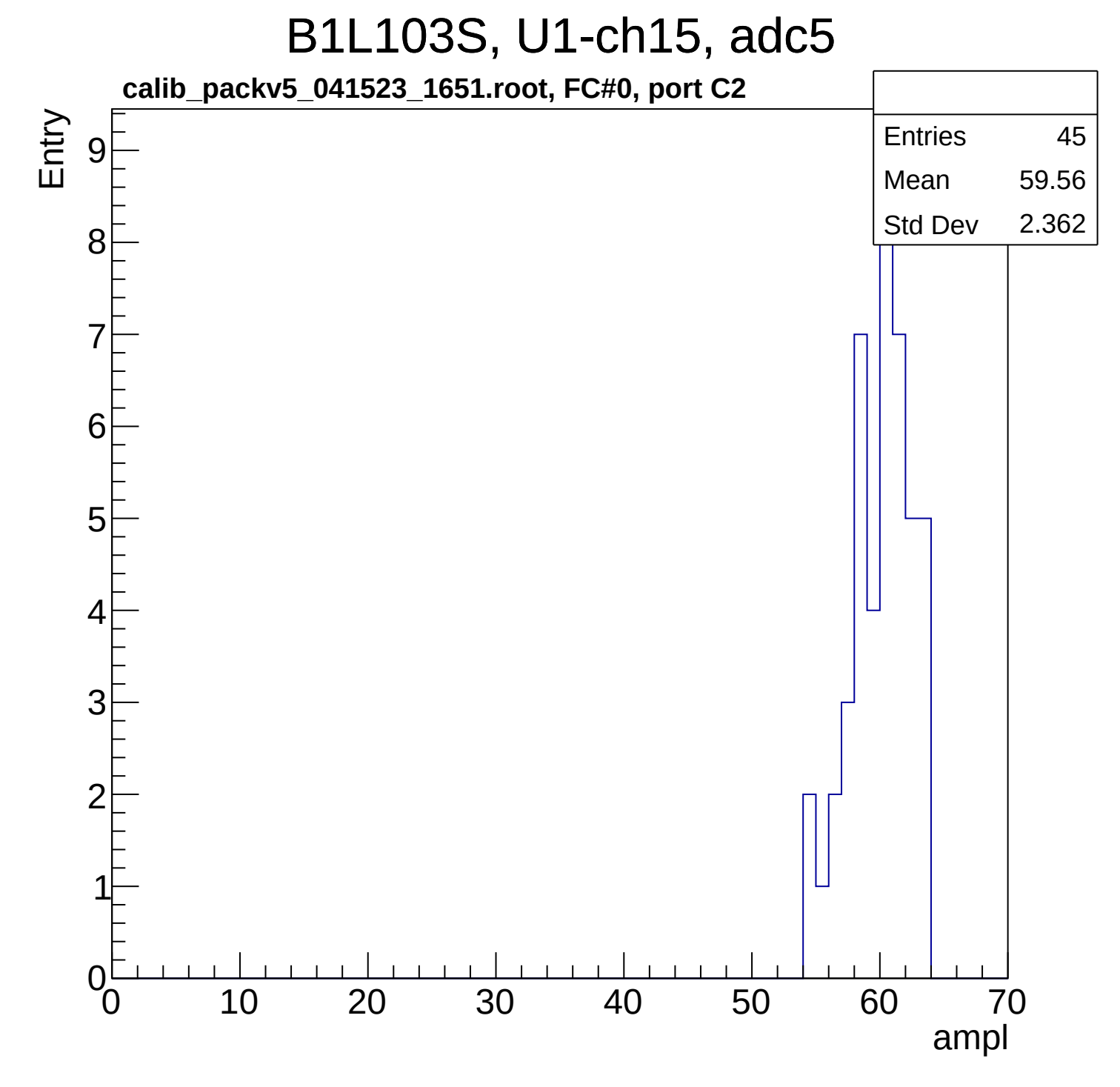
B1L103S, U1-ch15, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 59.56
Std Dev 2.362
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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60
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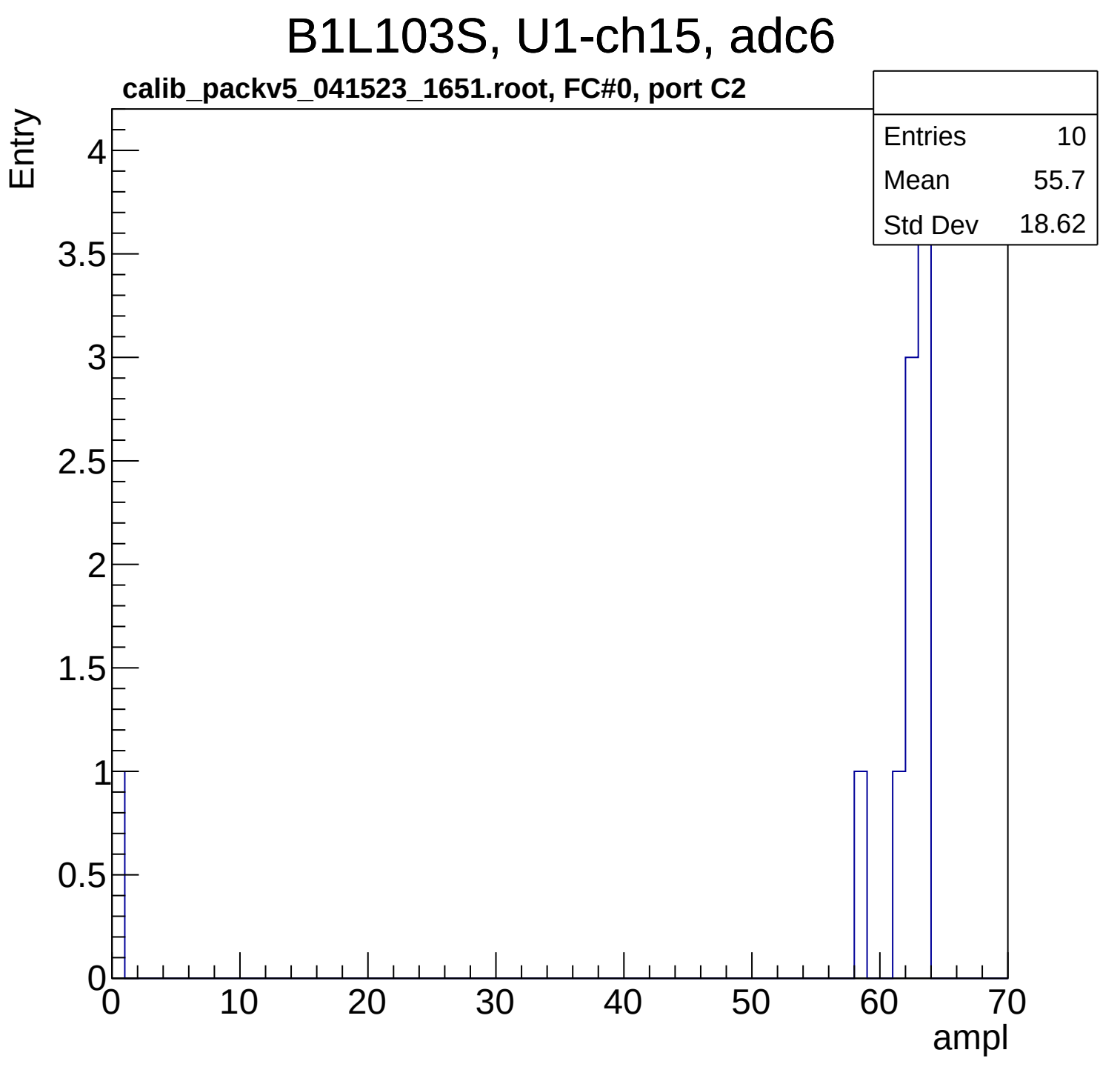
B1L103S, U1-ch15, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 55.7
Std Dev 18.62
Entry
ampl
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0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
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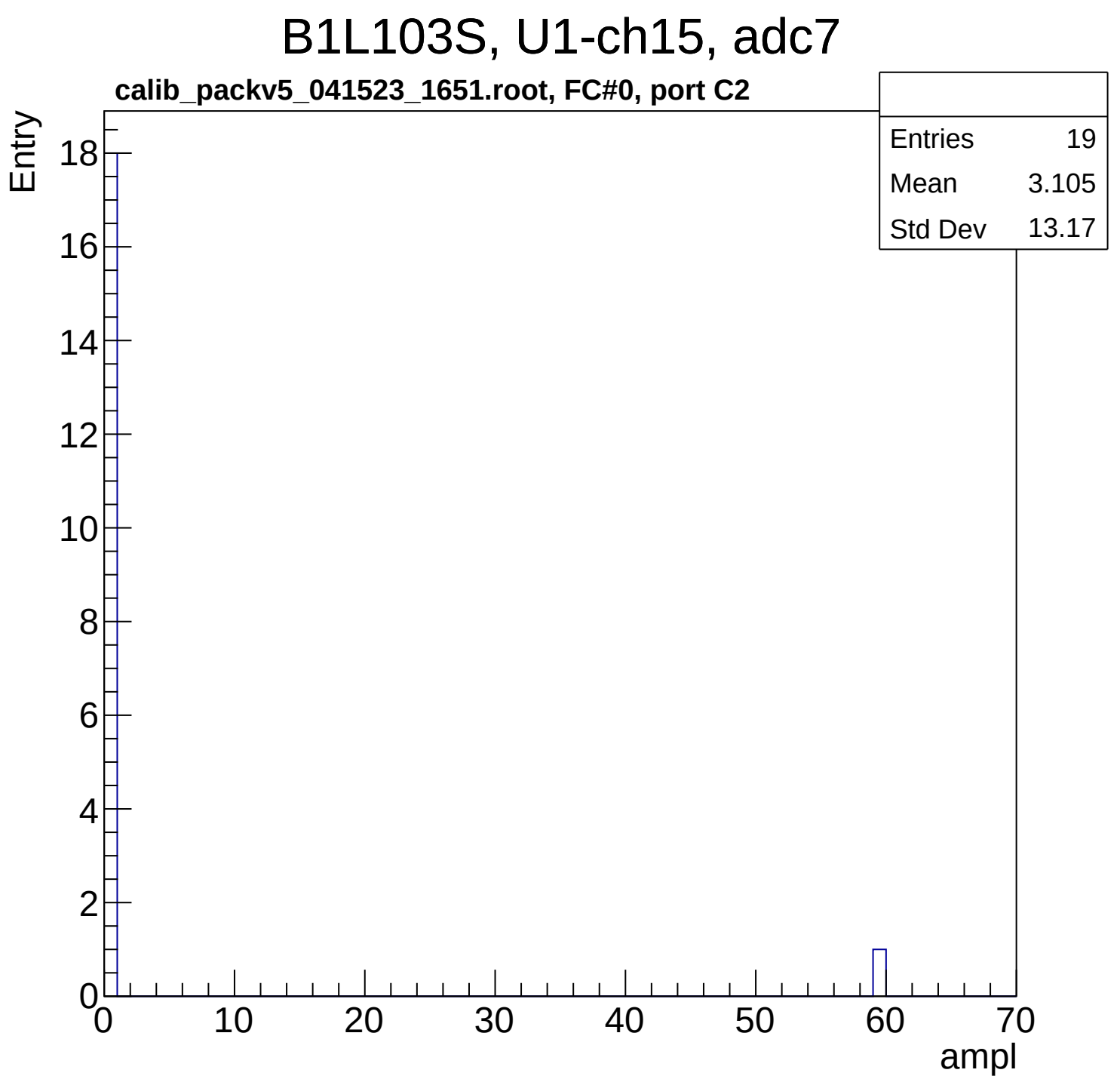
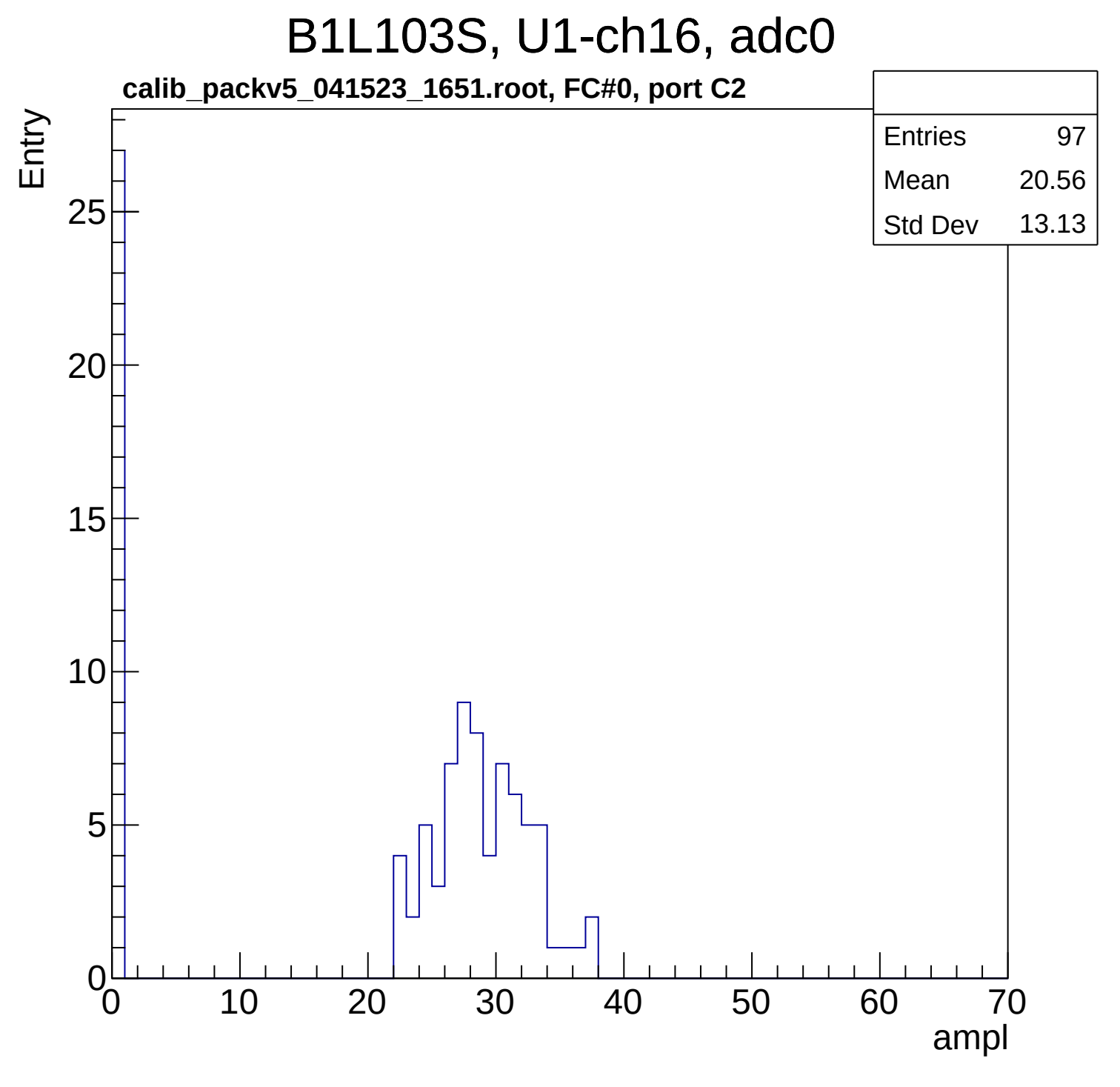
40
50
60
70


B1L103S, U1-ch15, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 3.105
Std Dev 13.17
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch16, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 97
Mean 20.56
Std Dev 13.13
Entry
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10
15
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25
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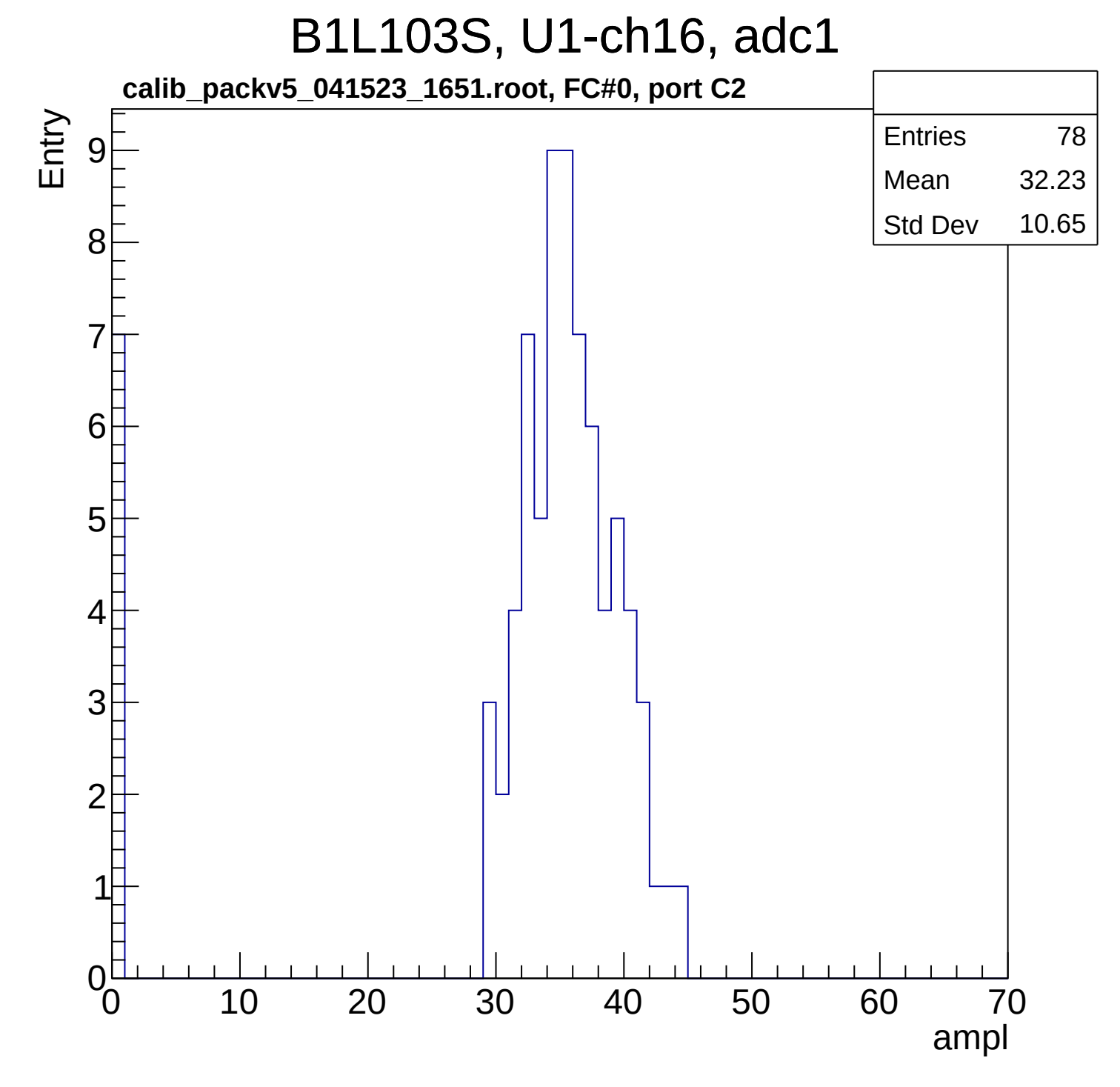
70
ampl


B1L103S, U1-ch16, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 32.23
Std Dev 10.65
Entry
ampl
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3
4
5
6
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60
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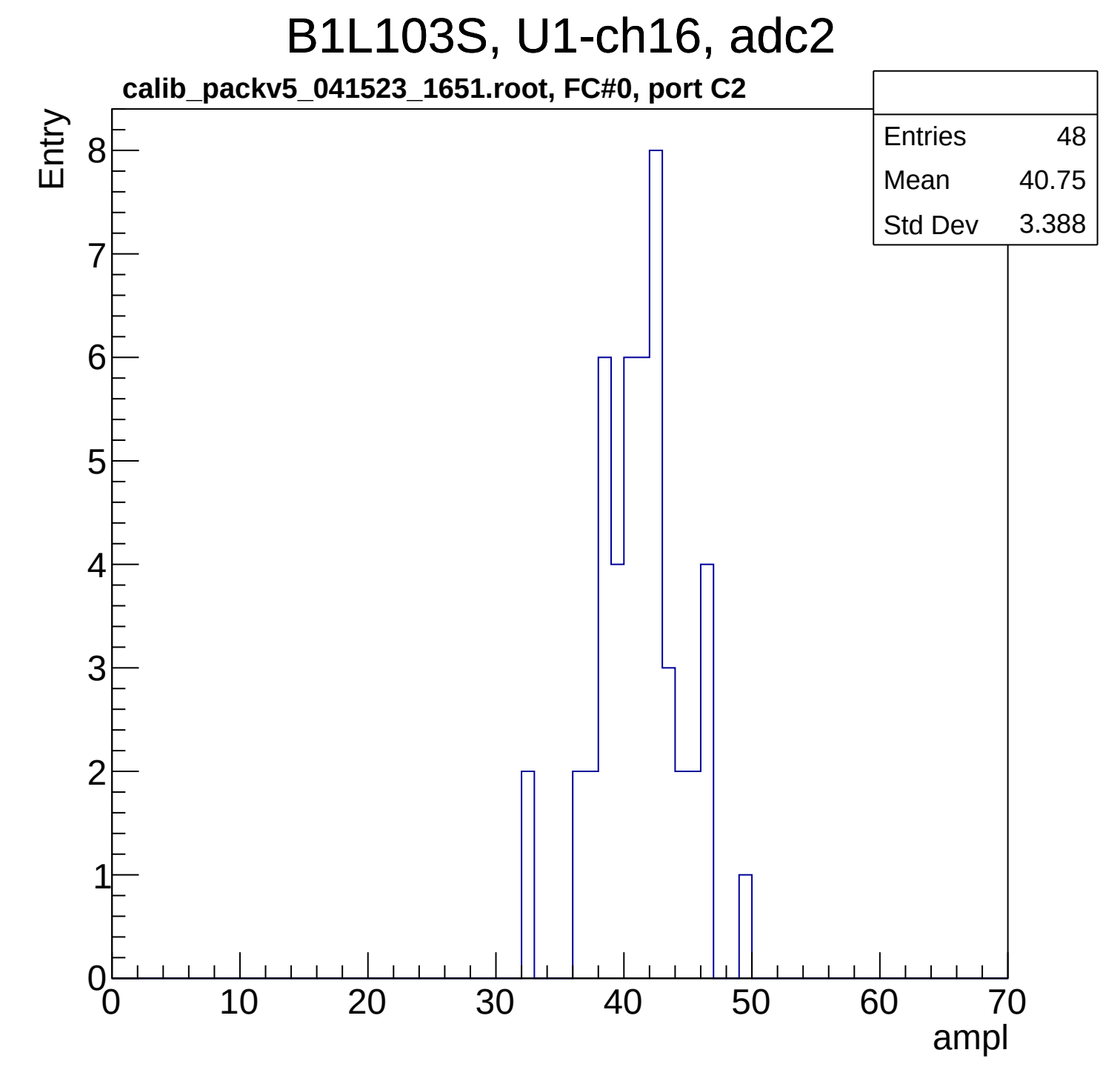
B1L103S, U1-ch16, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 40.75
Std Dev 3.388
Entry
ampl
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5
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7
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0
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40
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60
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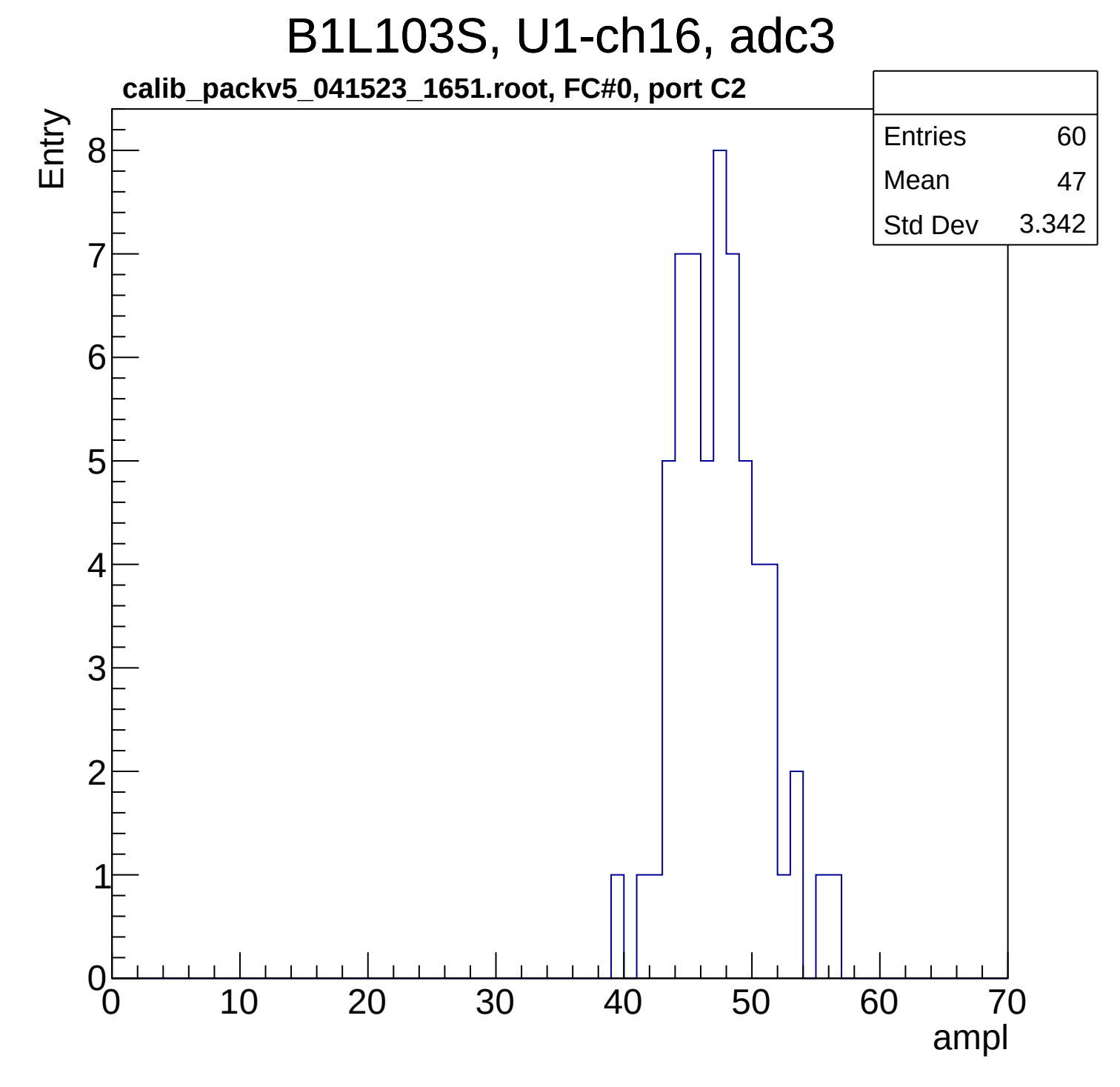
B1L103S, U1-ch16, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 47
Std Dev 3.342
Entry
ampl
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3
4
5
6
7
8
0
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20
30
40
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60
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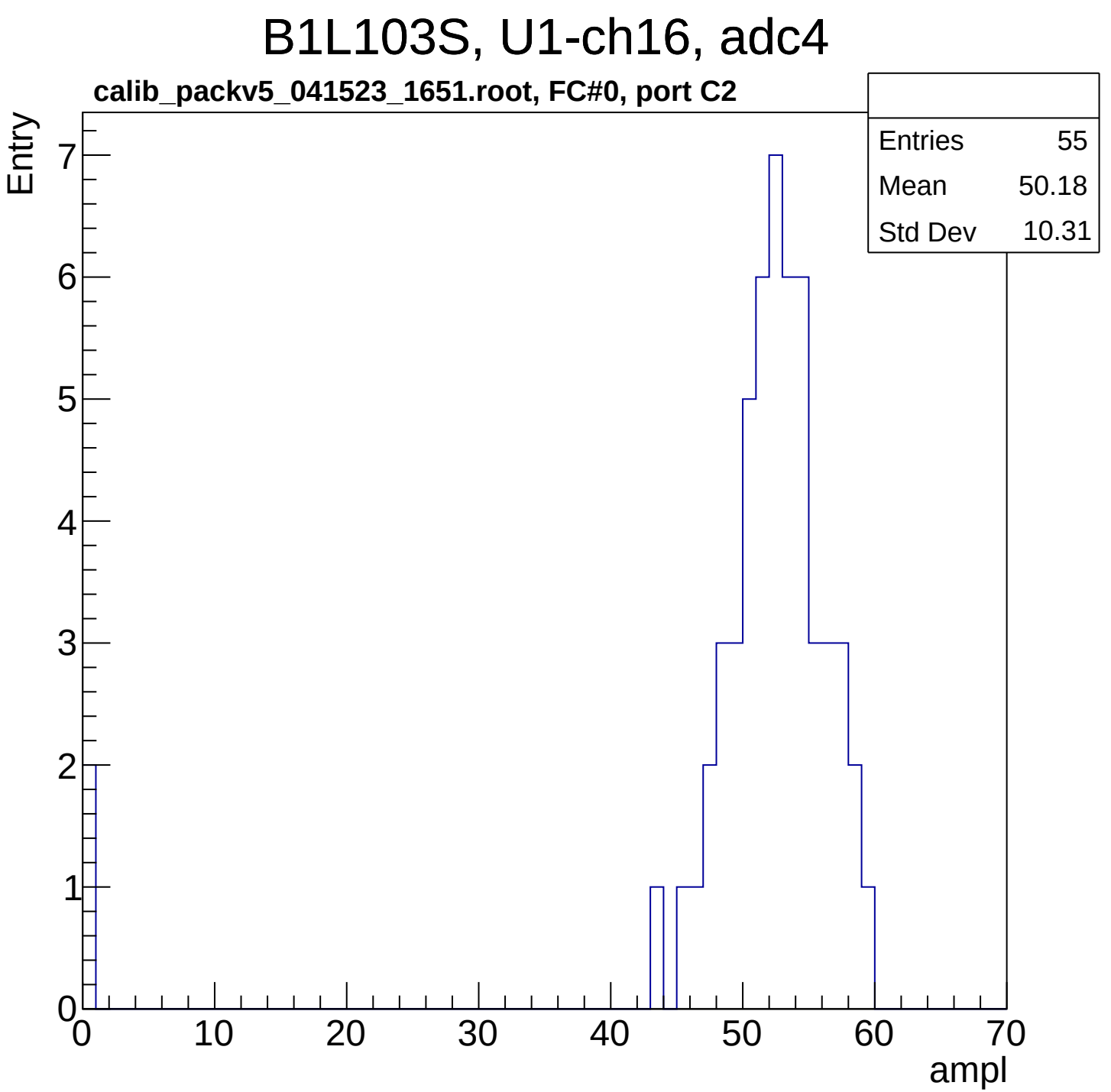
B1L103S, U1-ch16, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 50.18
Std Dev 10.31
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
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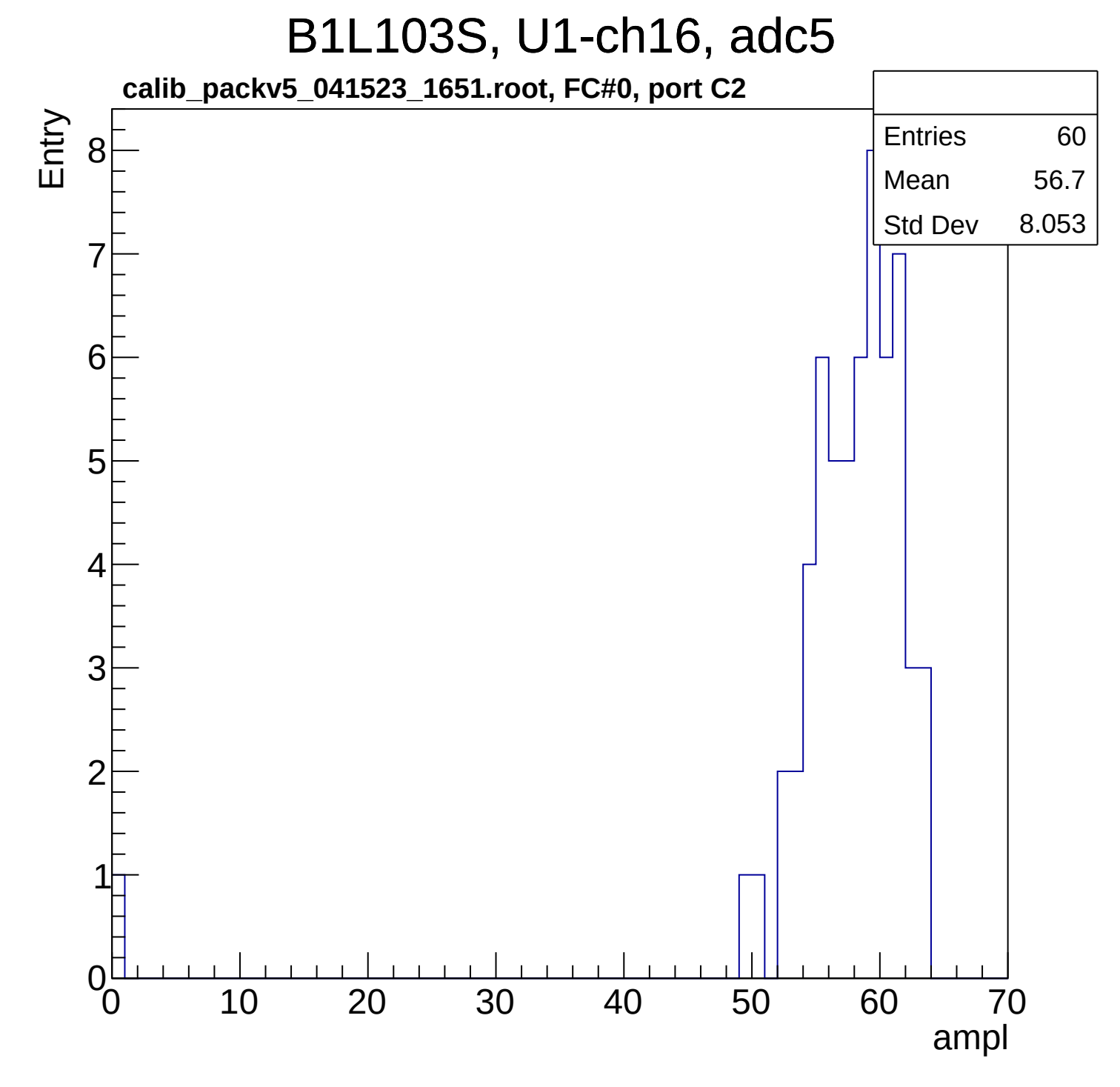
40
50
60
70


B1L103S, U1-ch16, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 56.7
Std Dev 8.053
Entry
ampl
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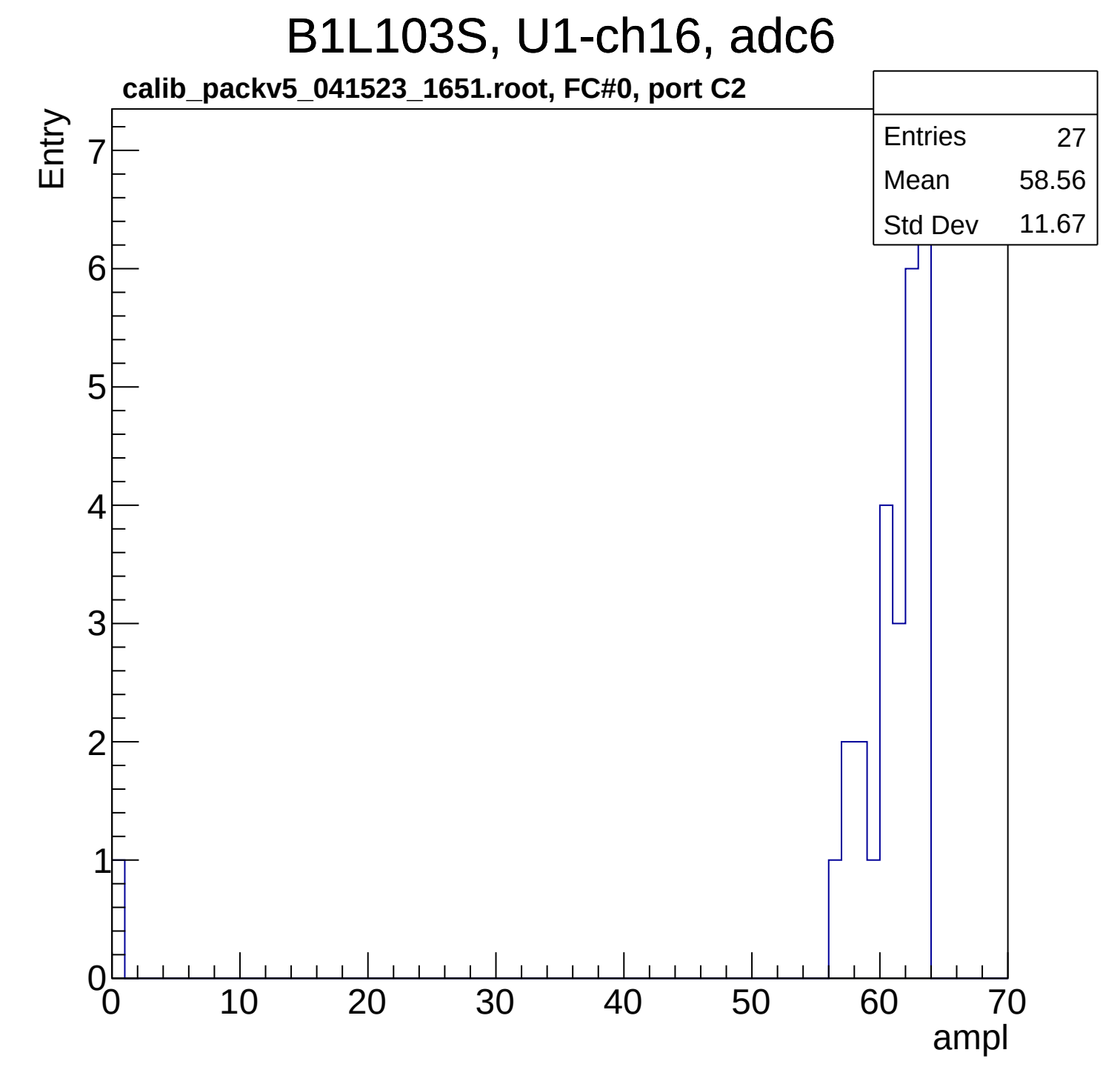
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U1-ch16, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 27
Mean 58.56
Std Dev 11.67
Entry
ampl
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4
5
6
7
0
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20
30
40
50
60
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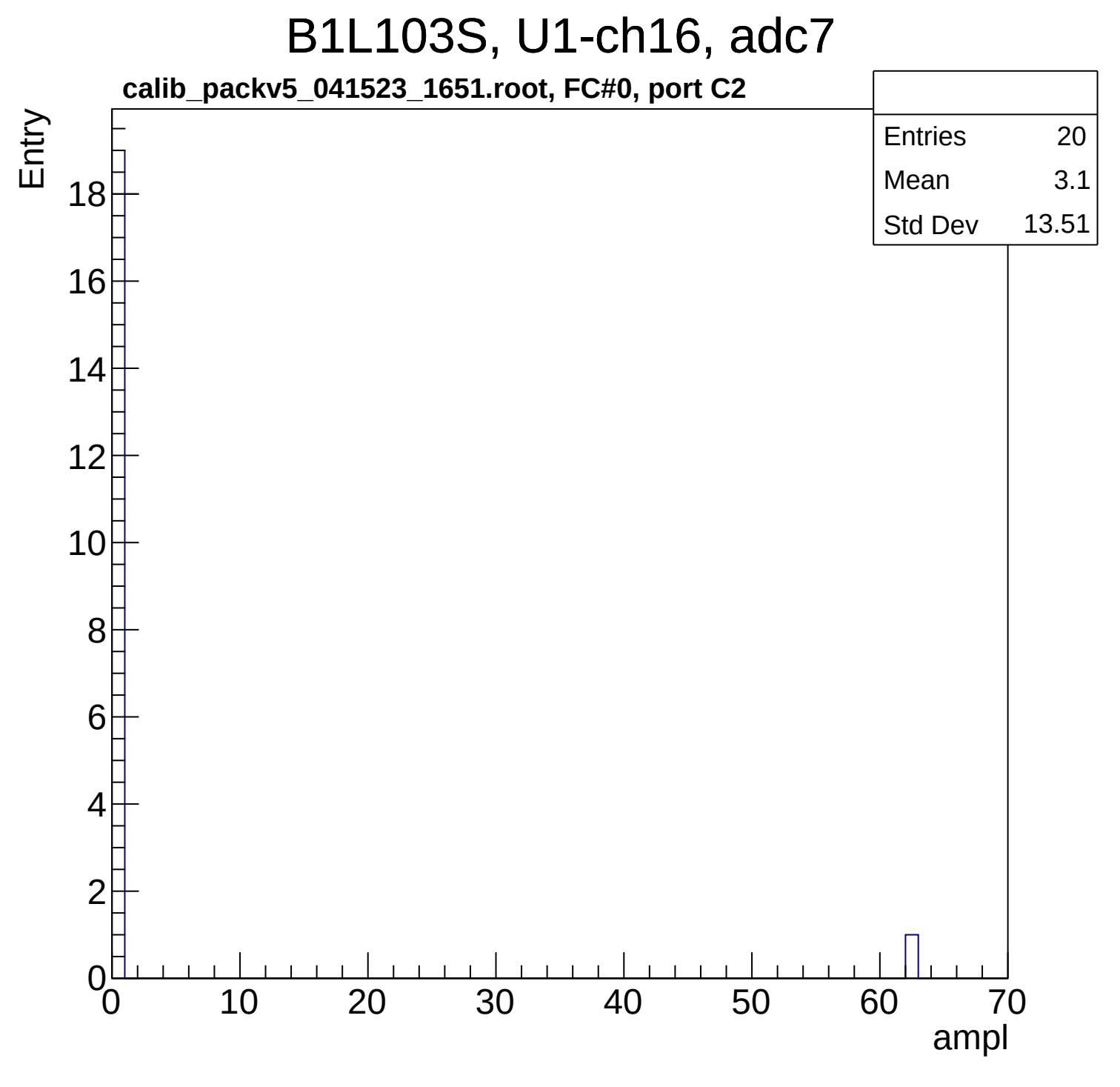
B1L103S, U1-ch16, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.1
Std Dev 13.51
Entry
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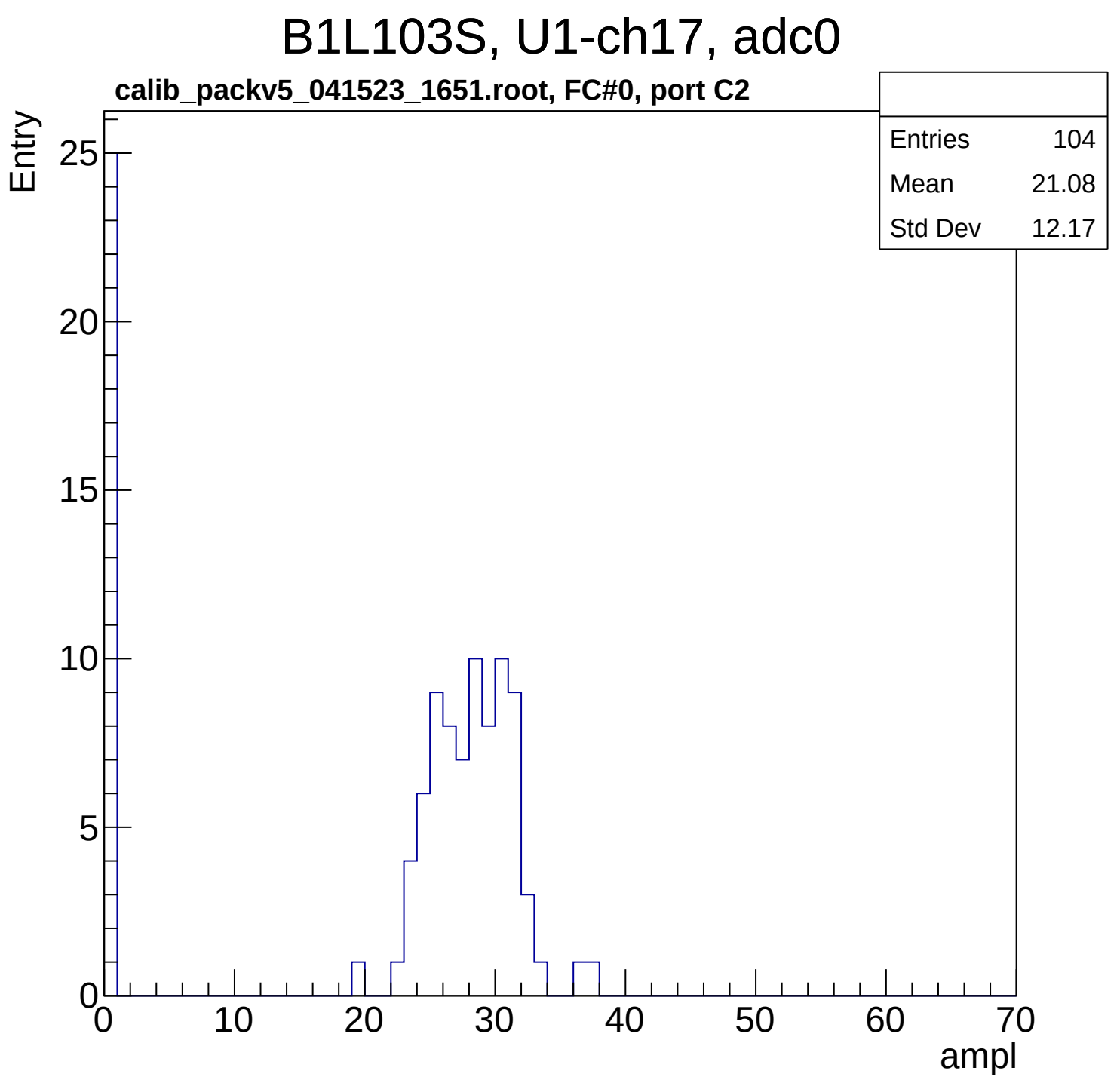
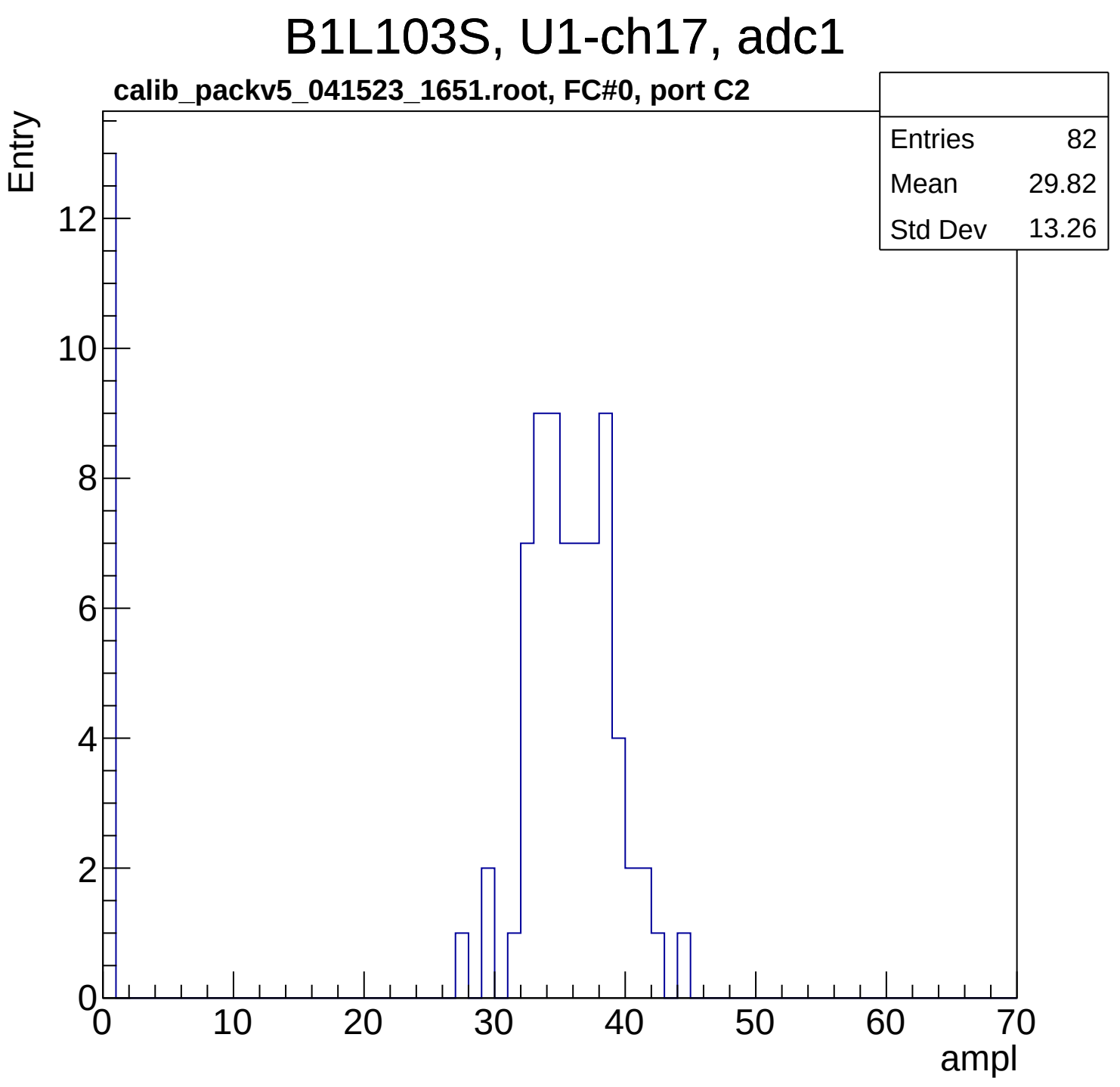
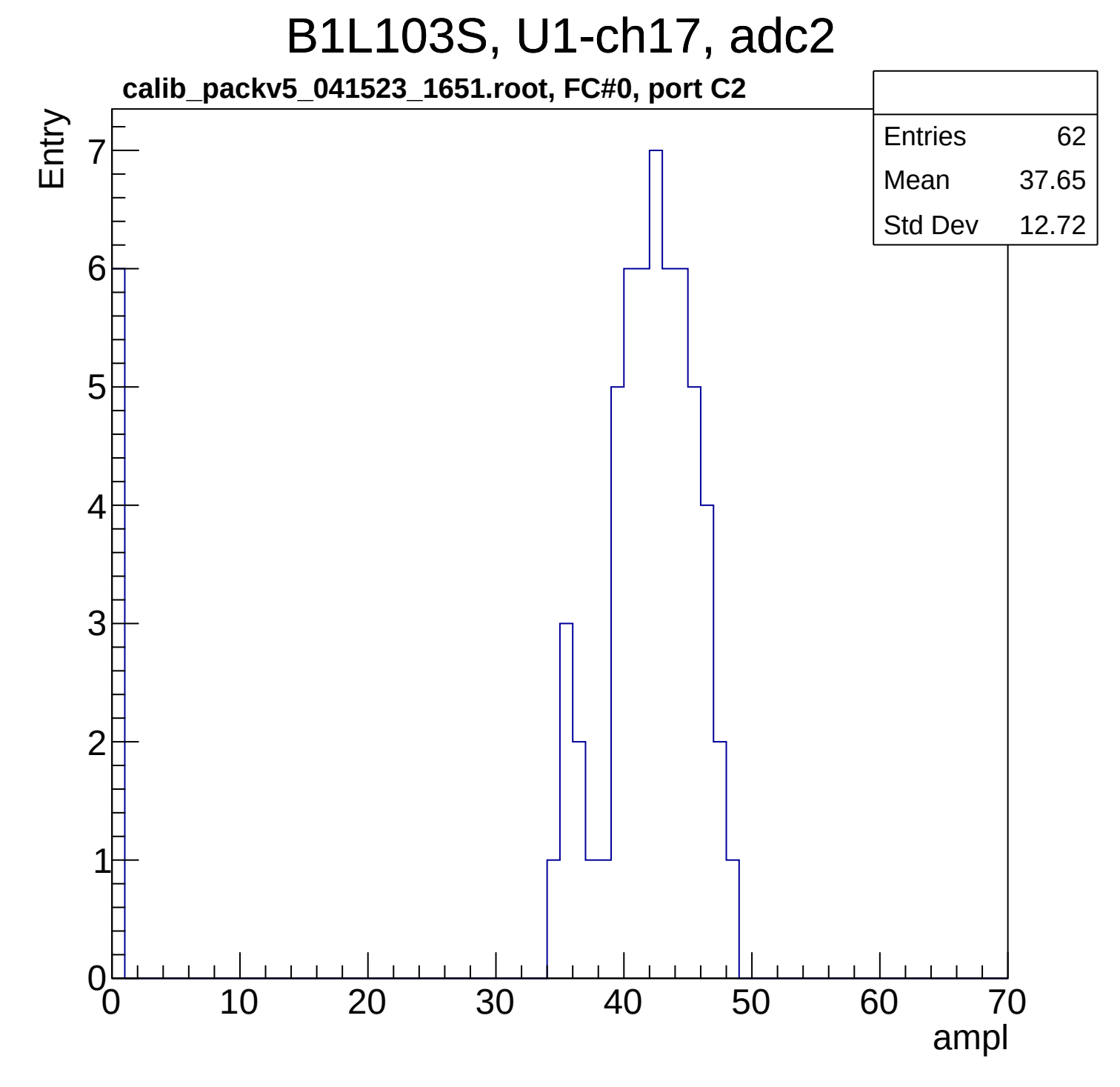
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch17, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 104
Mean 21.08
Std Dev 12.17
Entry
0
5
10
15
20
25
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch17, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 29.82
Std Dev 13.26
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch17, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 37.65
Std Dev 12.72
Entry
ampl
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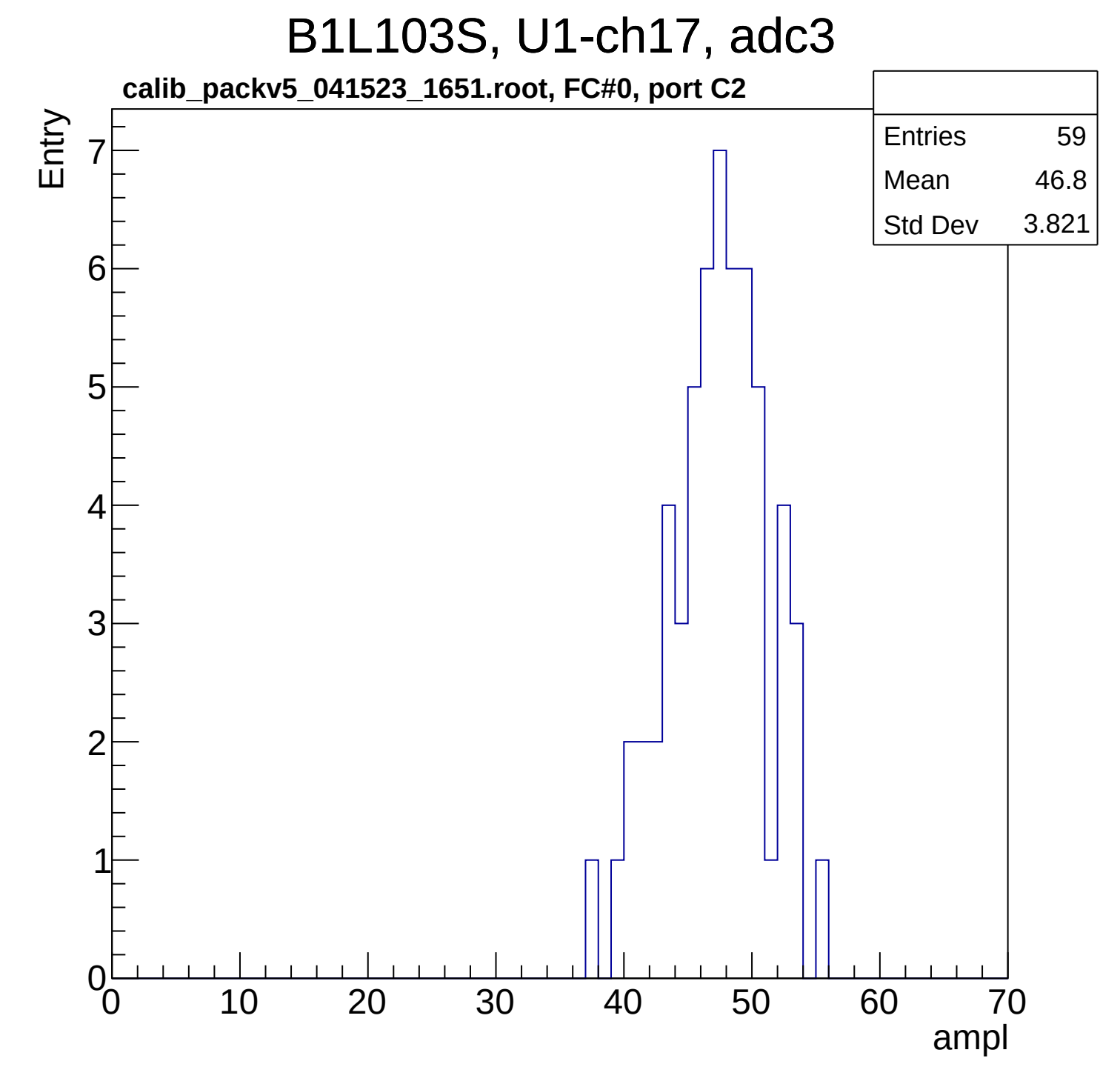
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U1-ch17, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 46.8
Std Dev 3.821
Entry
ampl
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2
3
4
5
6
7
0
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20
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40
50
60
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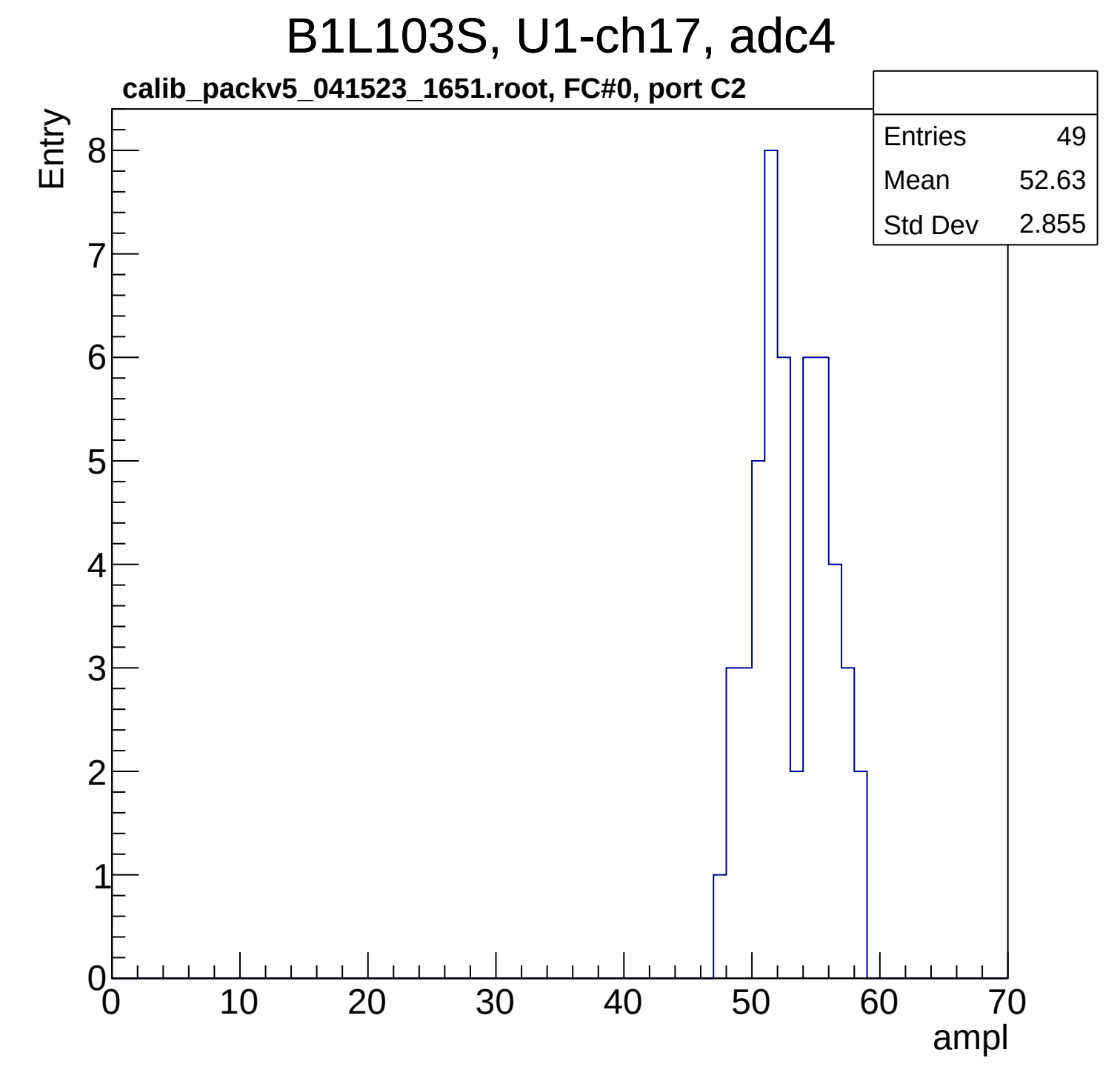
B1L103S, U1-ch17, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 52.63
Std Dev 2.855
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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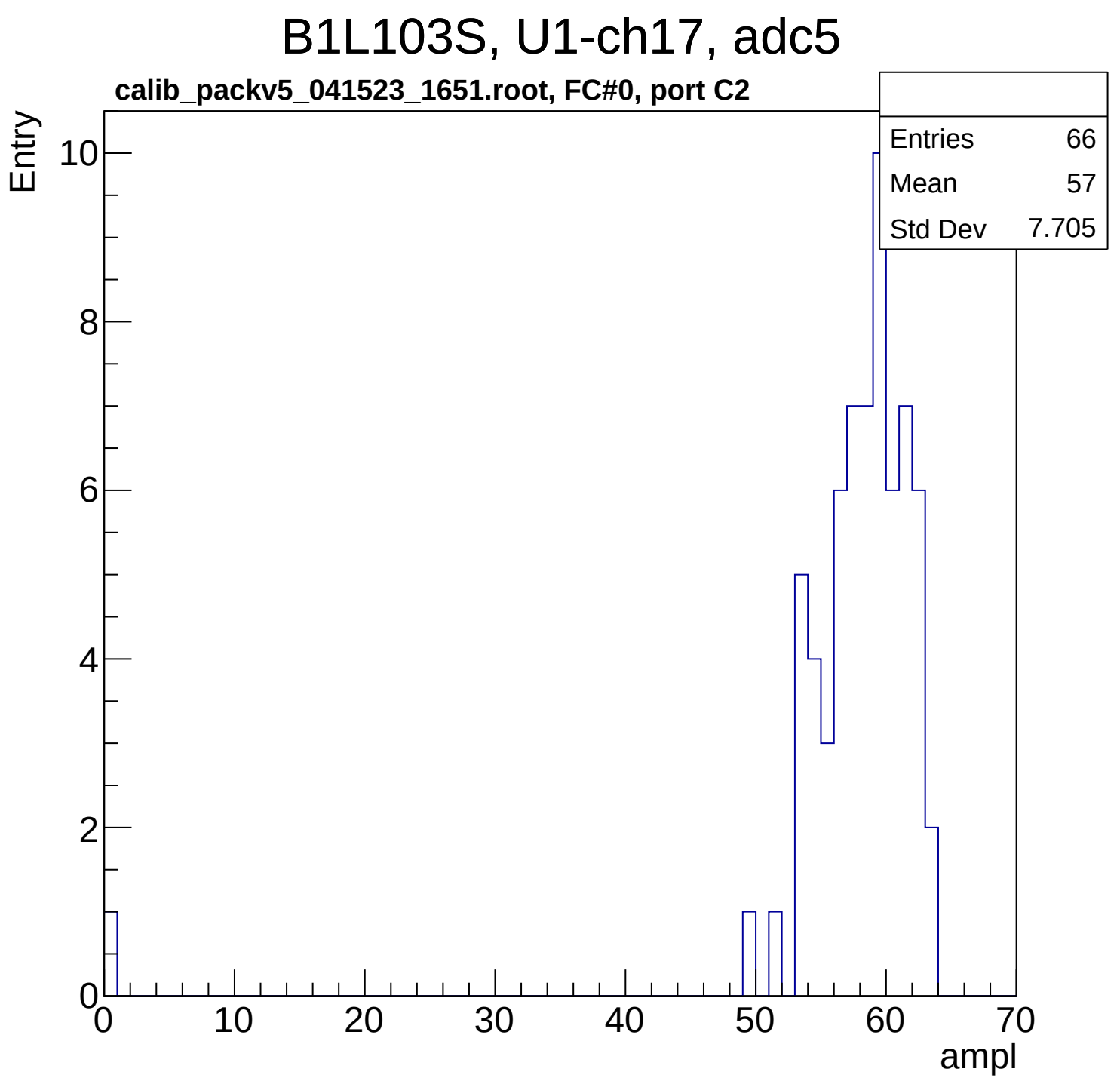
B1L103S, U1-ch17, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 57
Std Dev 7.705
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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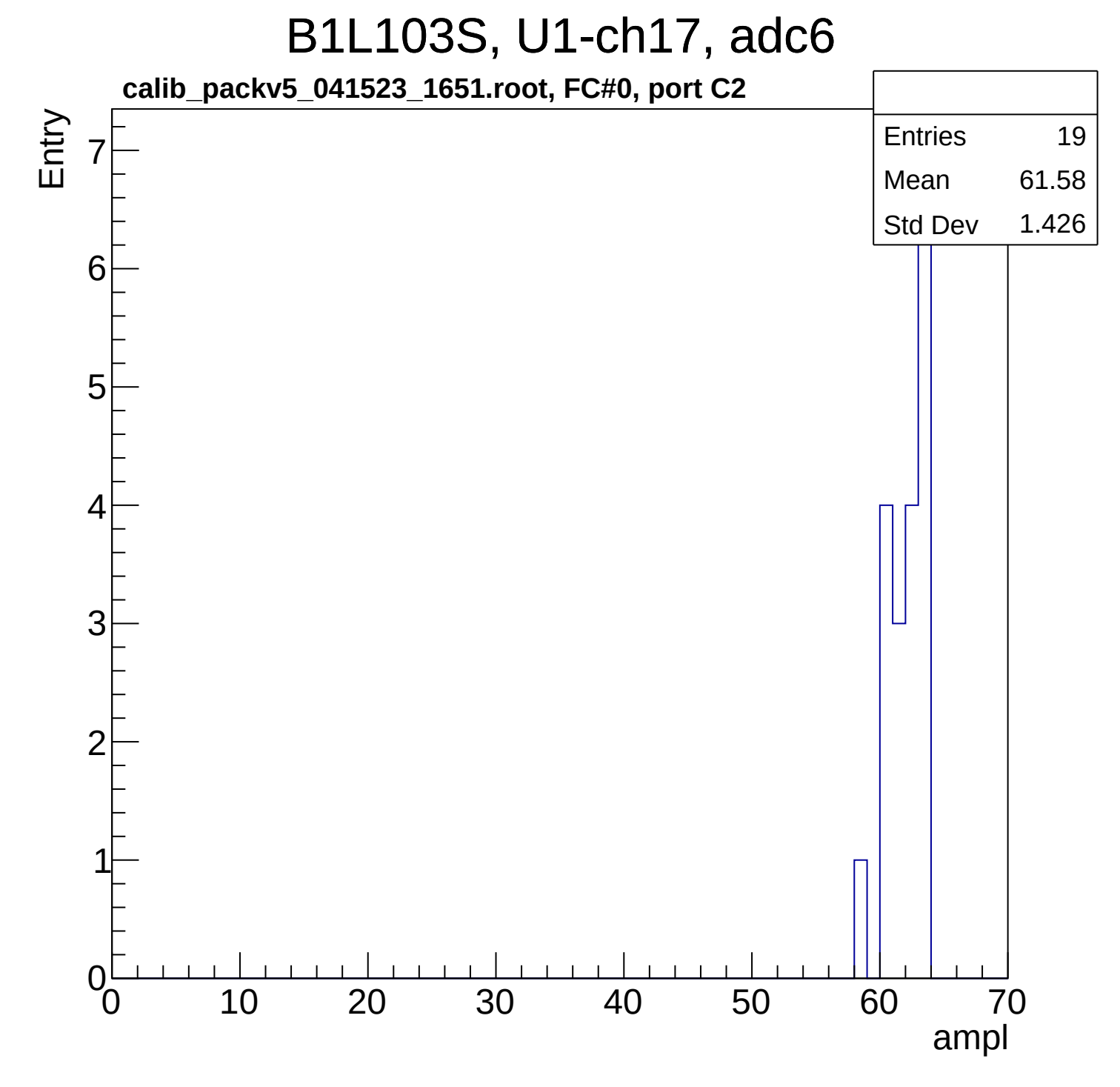
B1L103S, U1-ch17, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 61.58
Std Dev 1.426
Entry
ampl
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2
3
4
5
6
7
0
10
20
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40
50
60
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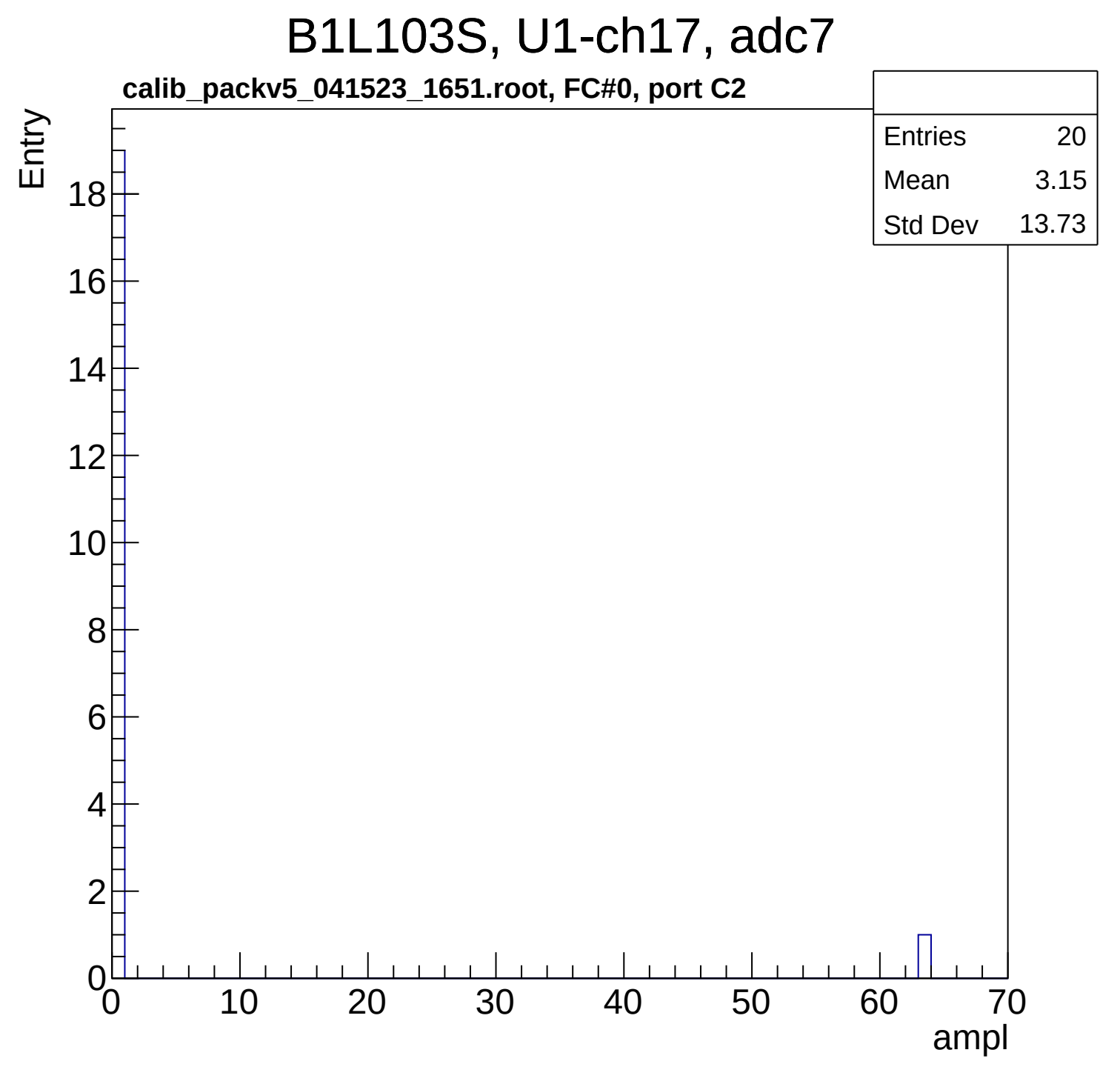
B1L103S, U1-ch17, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
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6
8
10
12
14
16
18
0
10
20
30
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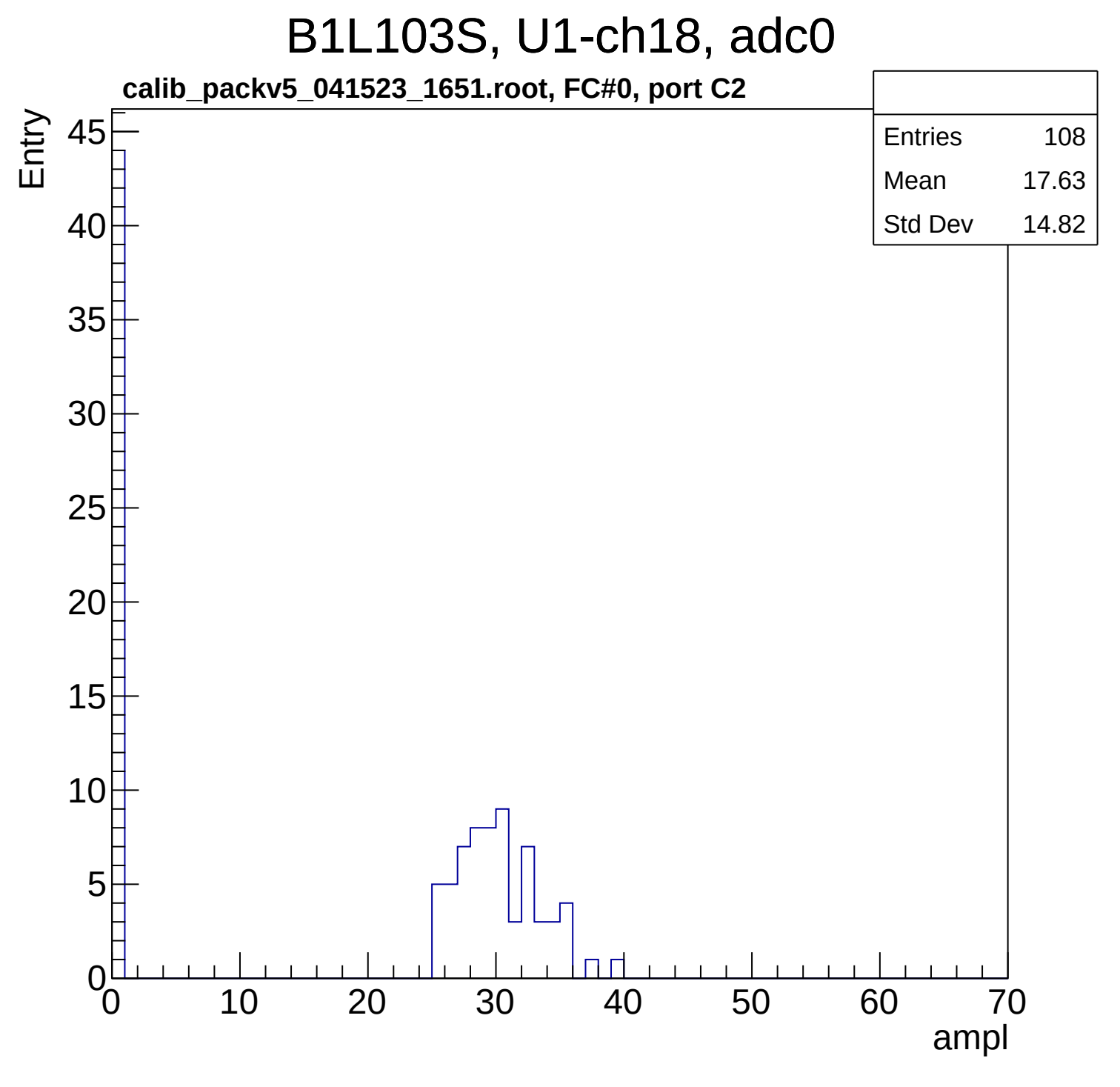
50
60
70
ampl


B1L103S, U1-ch18, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 108
Mean 17.63
Std Dev 14.82
Entry
ampl
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10
15
20
25
30
35
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0
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20
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40
50
60
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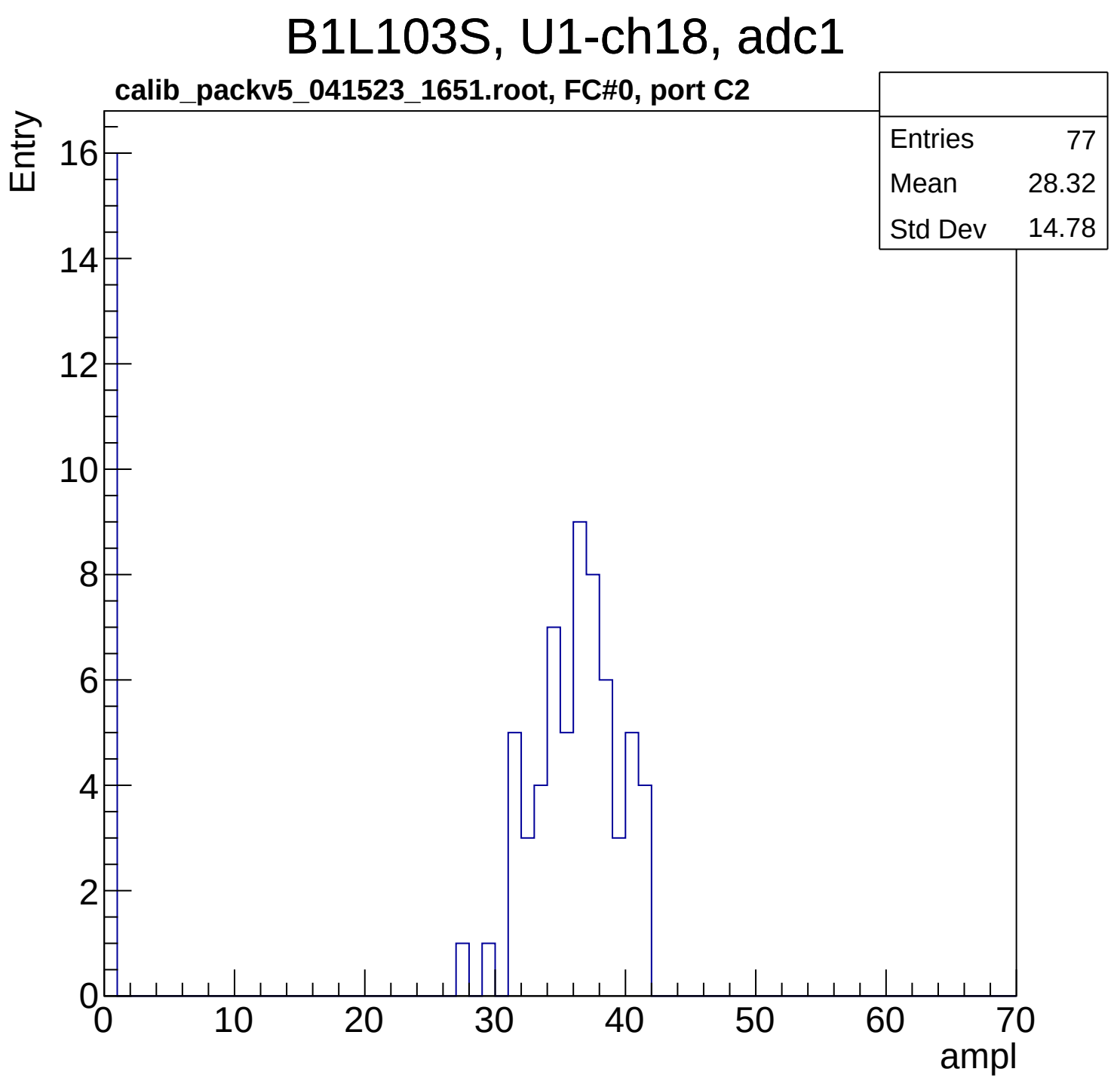
B1L103S, U1-ch18, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 28.32
Std Dev 14.78
Entry
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4
6
8
10
12
14
16
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10
20
30
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50
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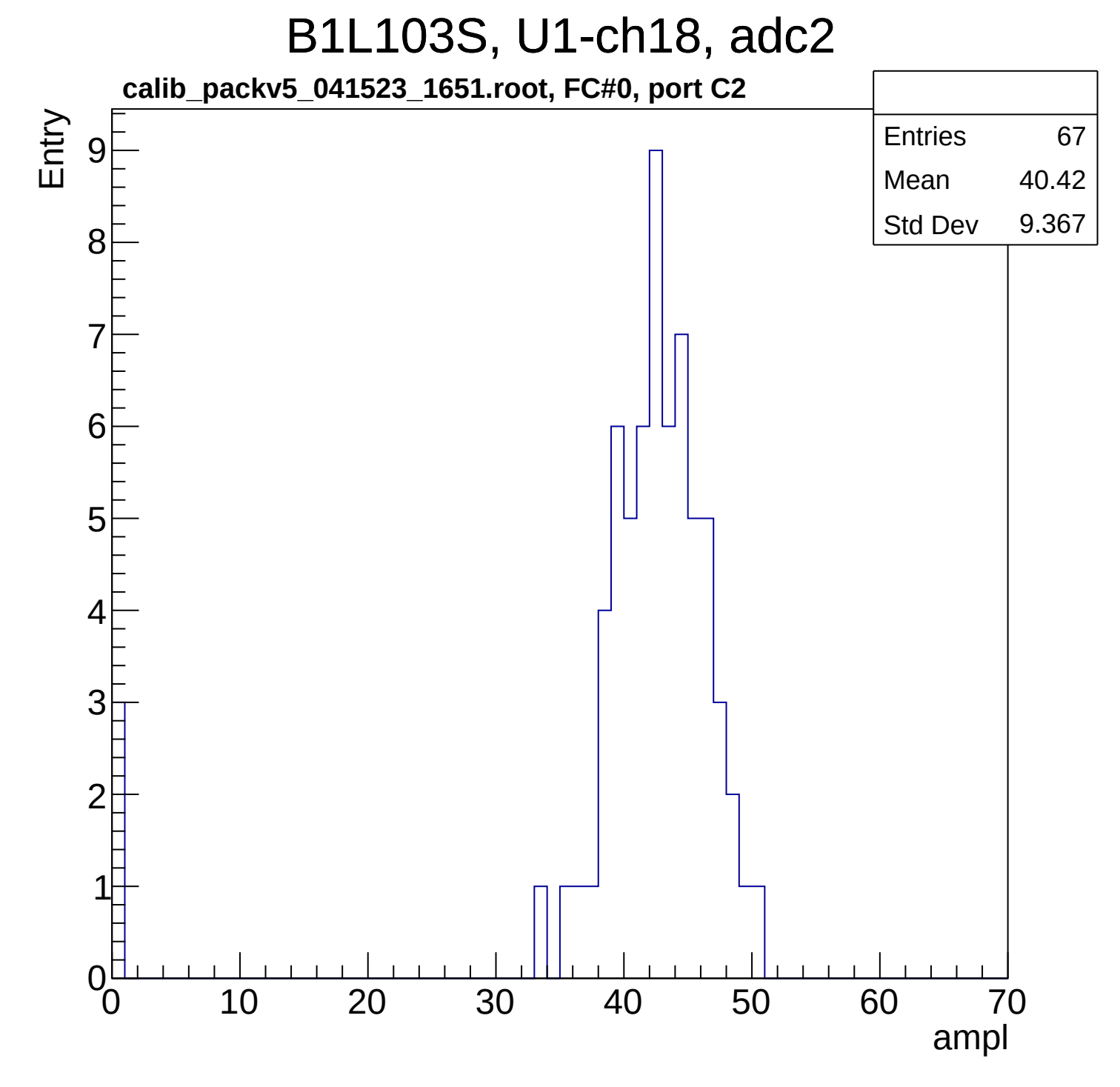
70
ampl


B1L103S, U1-ch18, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 40.42
Std Dev 9.367
Entry
ampl
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5
6
7
8
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0
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60
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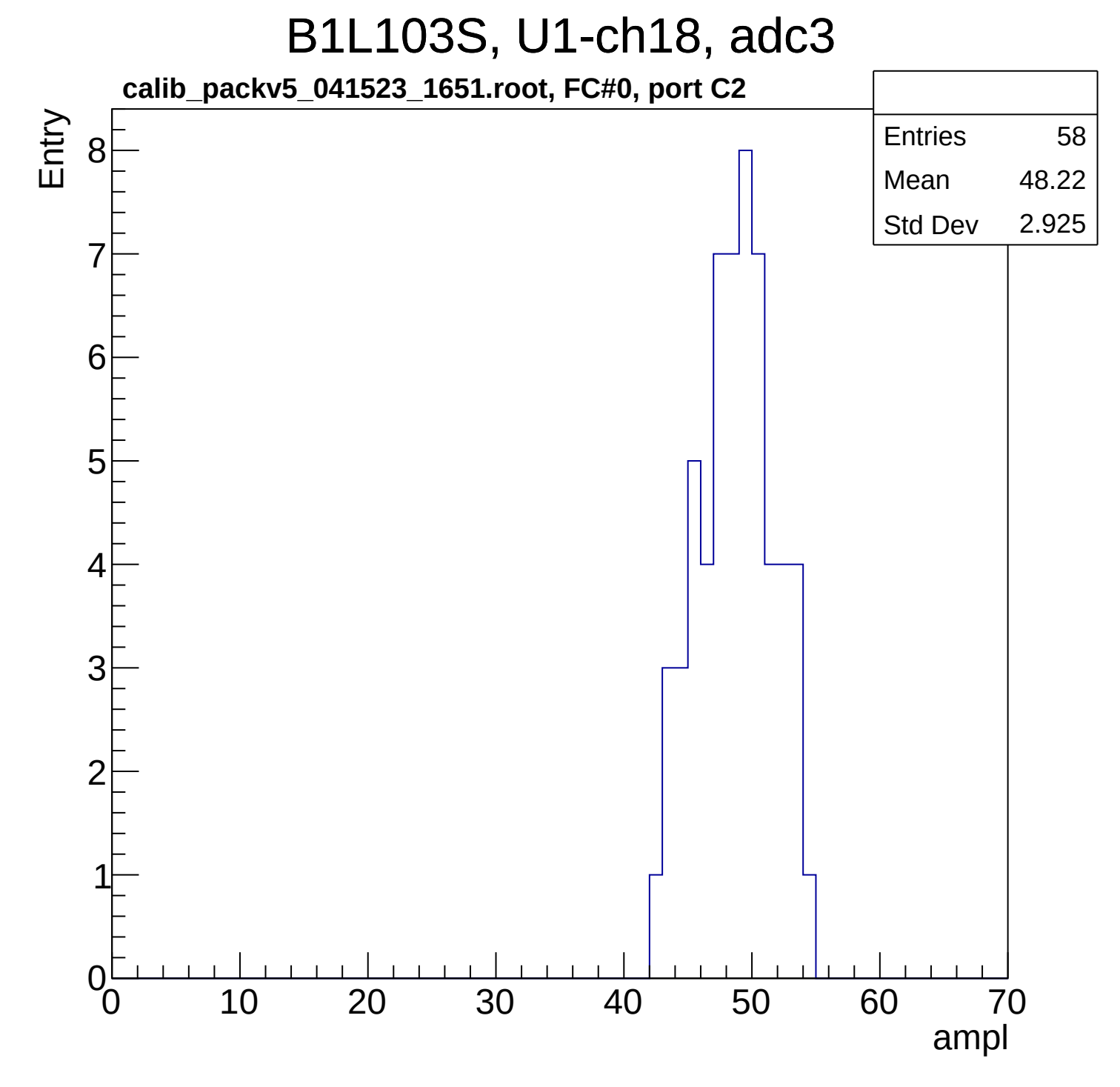
B1L103S, U1-ch18, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 48.22
Std Dev 2.925
Entry
ampl
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2
3
4
5
6
7
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60
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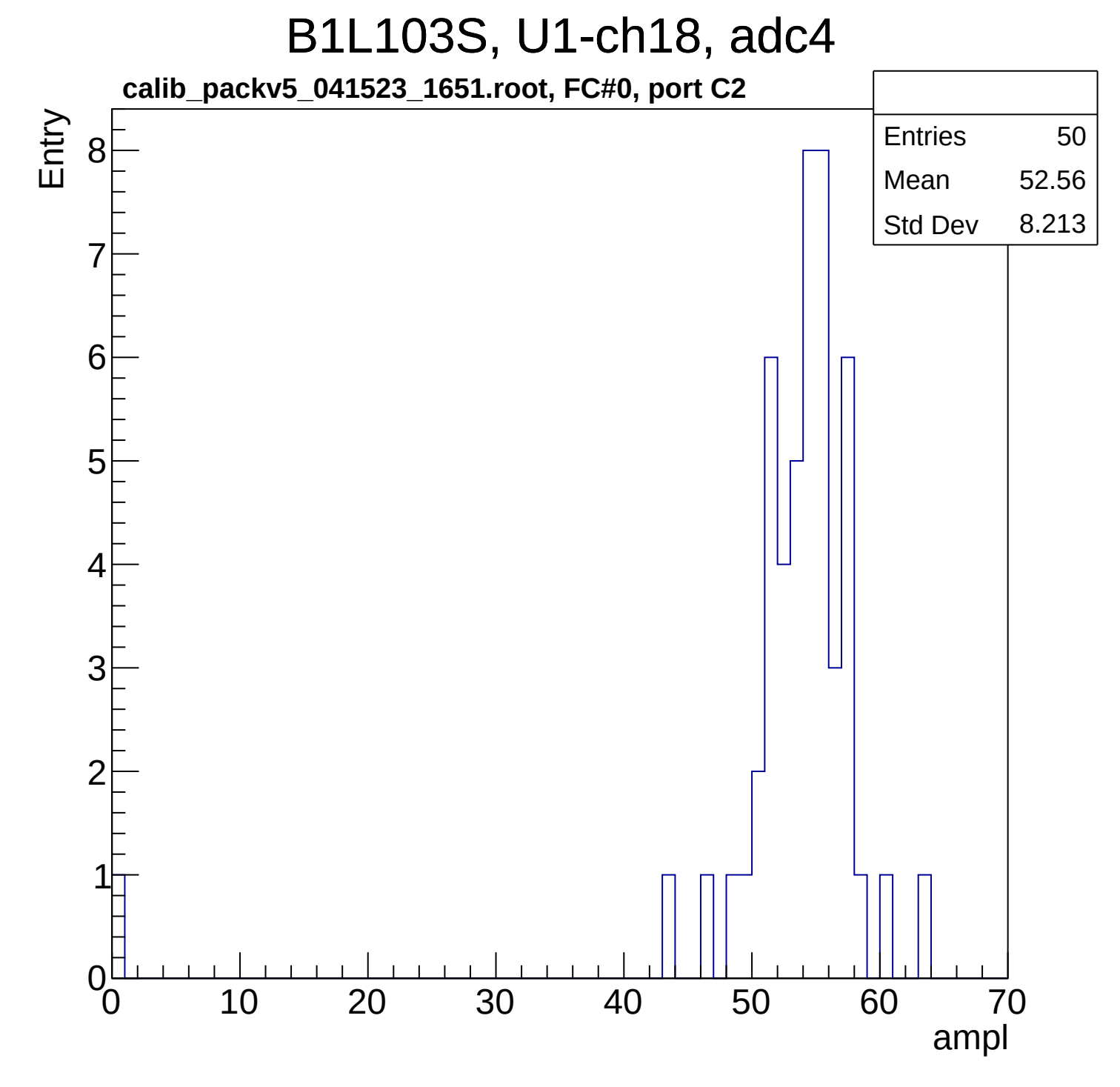
B1L103S, U1-ch18, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 52.56
Std Dev 8.213
Entry
ampl
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2
3
4
5
6
7
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0
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60
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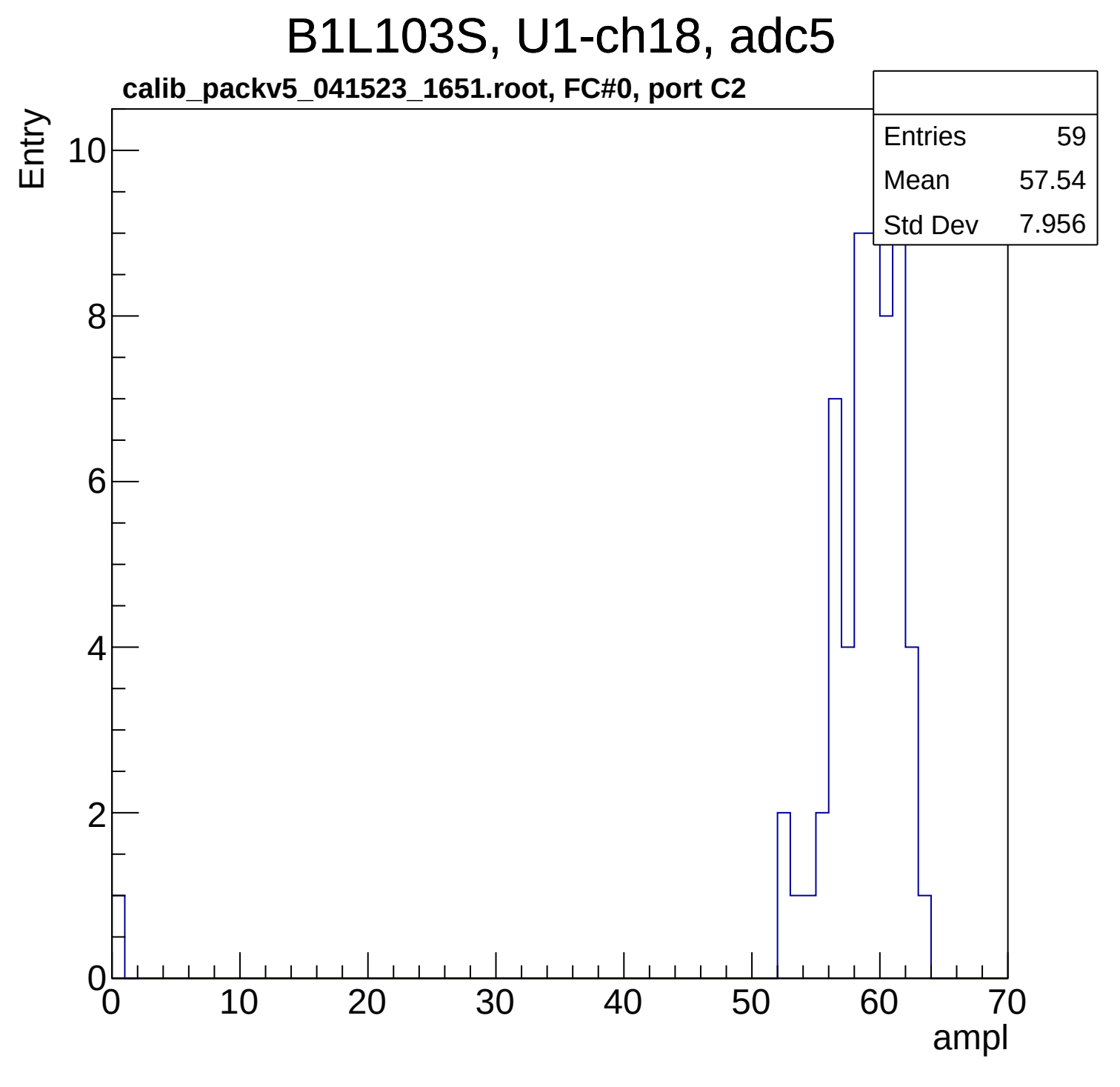
B1L103S, U1-ch18, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 57.54
Std Dev 7.956
Entry
ampl
0
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4
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8
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0
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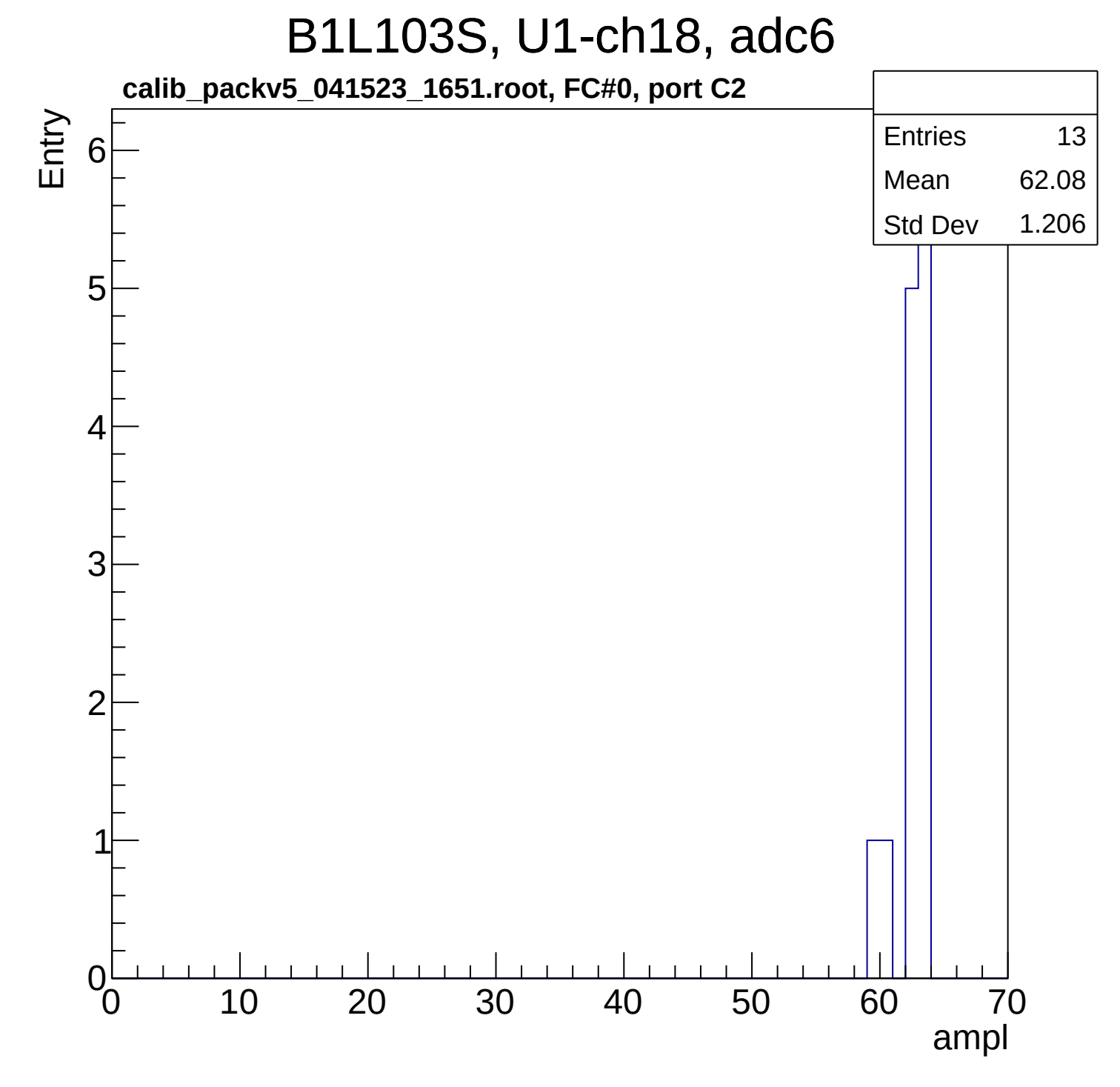
B1L103S, U1-ch18, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 13
Mean 62.08
Std Dev 1.206
Entry
ampl
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3
4
5
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0
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50
60
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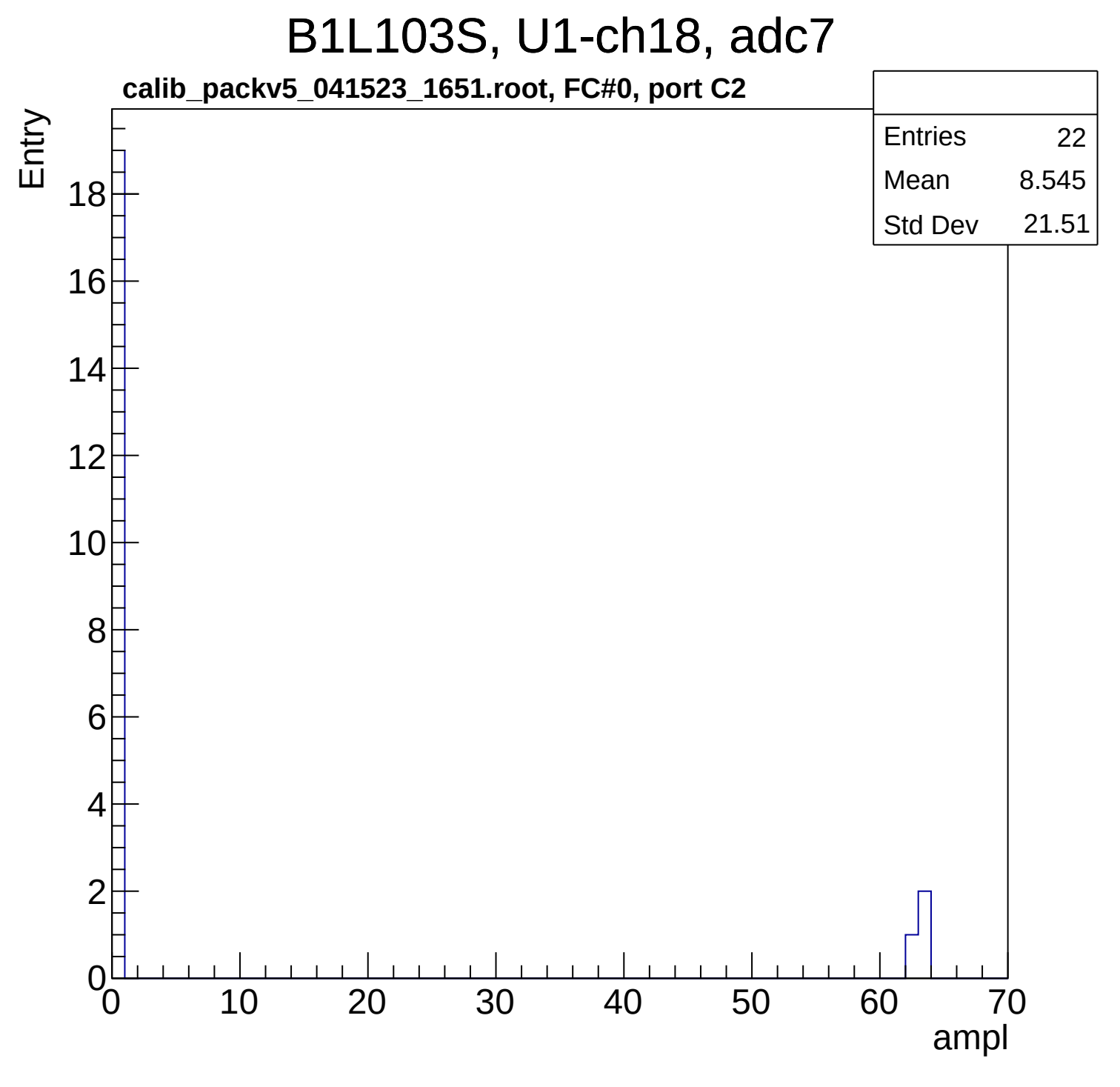
B1L103S, U1-ch18, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 8.545
Std Dev 21.51
Entry
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8
10
12
14
16
18
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10
20
30
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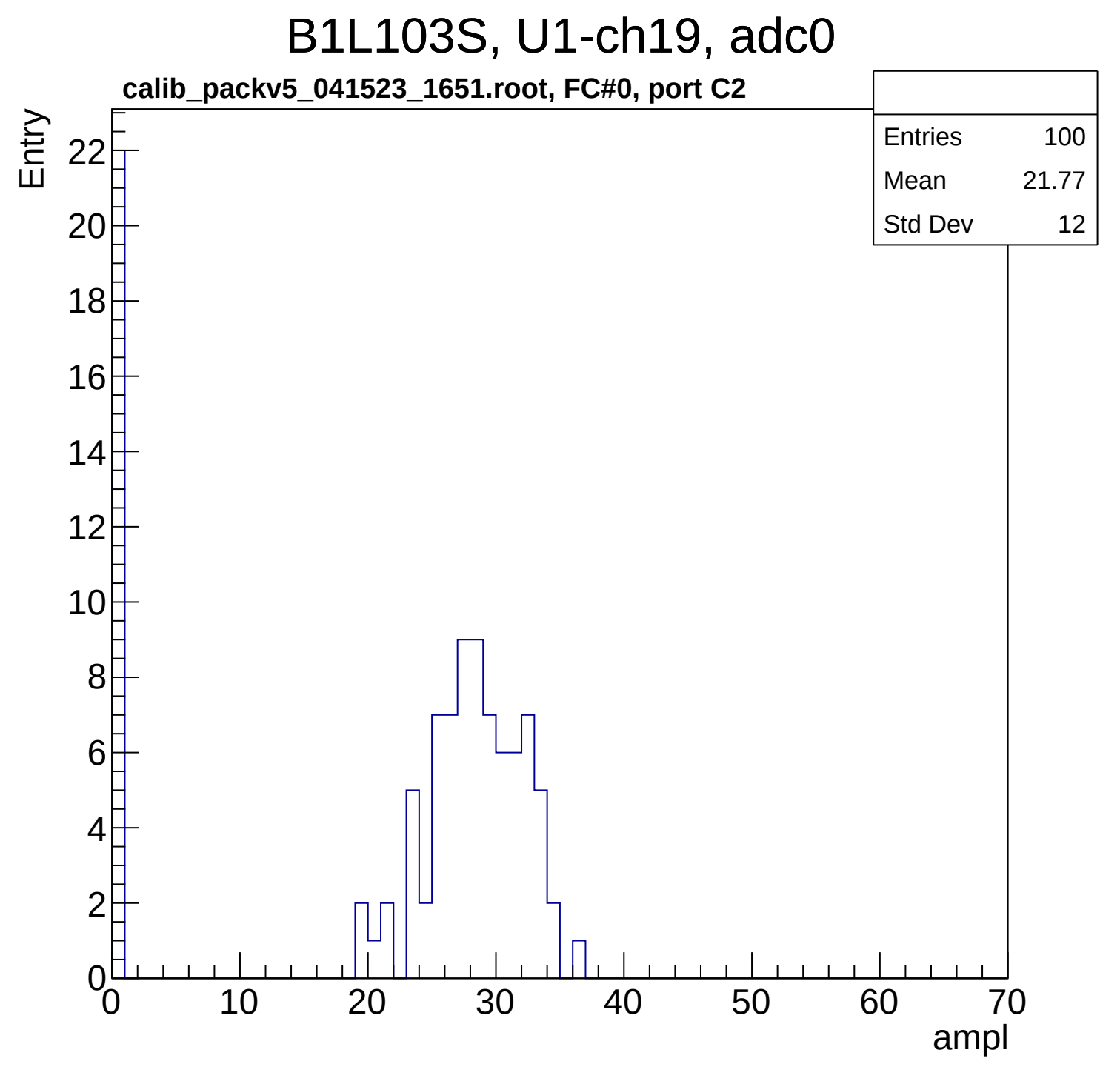
60
70
ampl


B1L103S, U1-ch19, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 100
Mean 21.77
Std Dev 12
Entry
ampl
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6
8
10
12
14
16
18
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60
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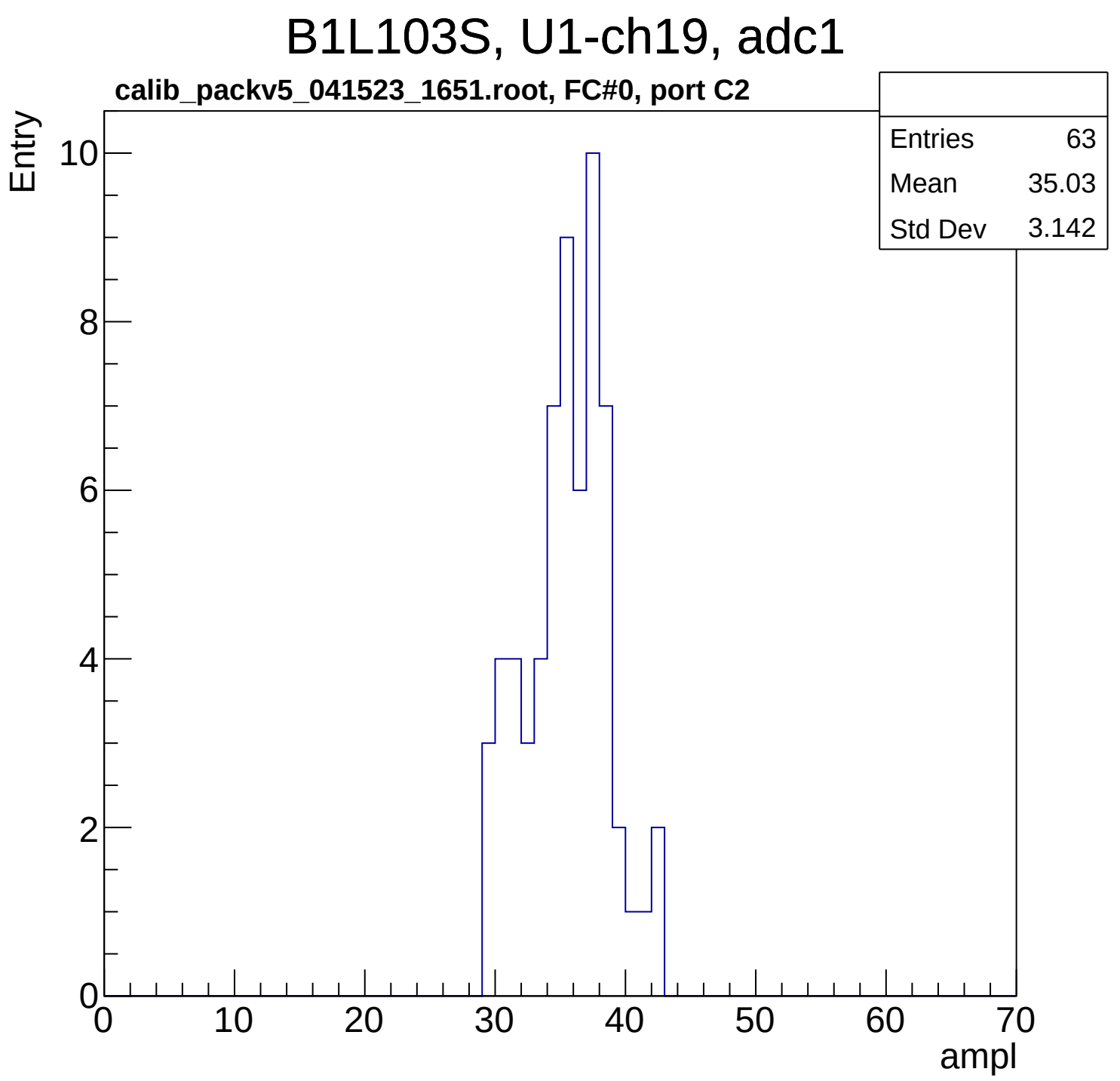
B1L103S, U1-ch19, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 35.03
Std Dev 3.142
Entry
ampl
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4
6
8
10
0
10
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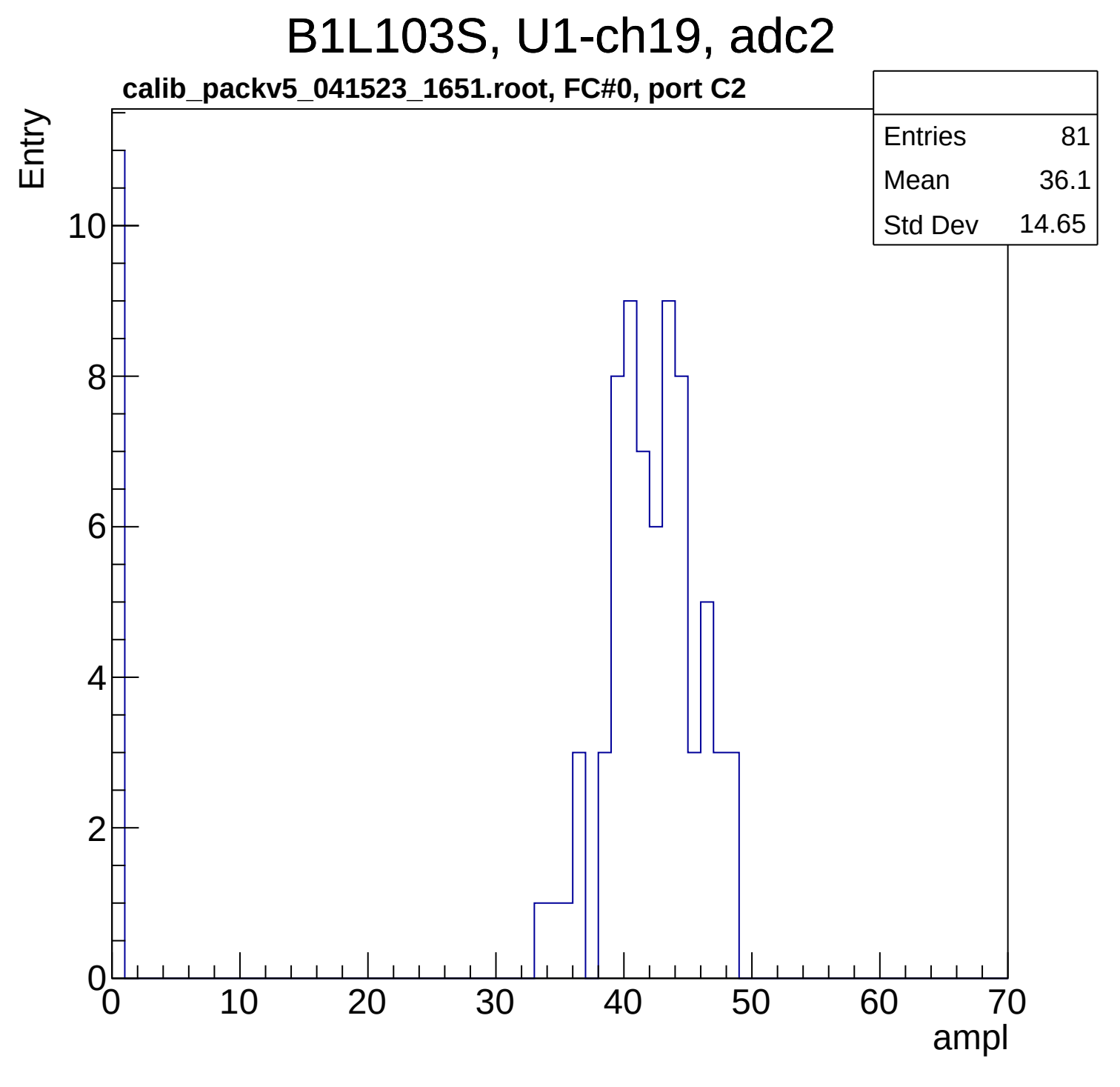
50
60
70


B1L103S, U1-ch19, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 36.1
Std Dev 14.65
Entry
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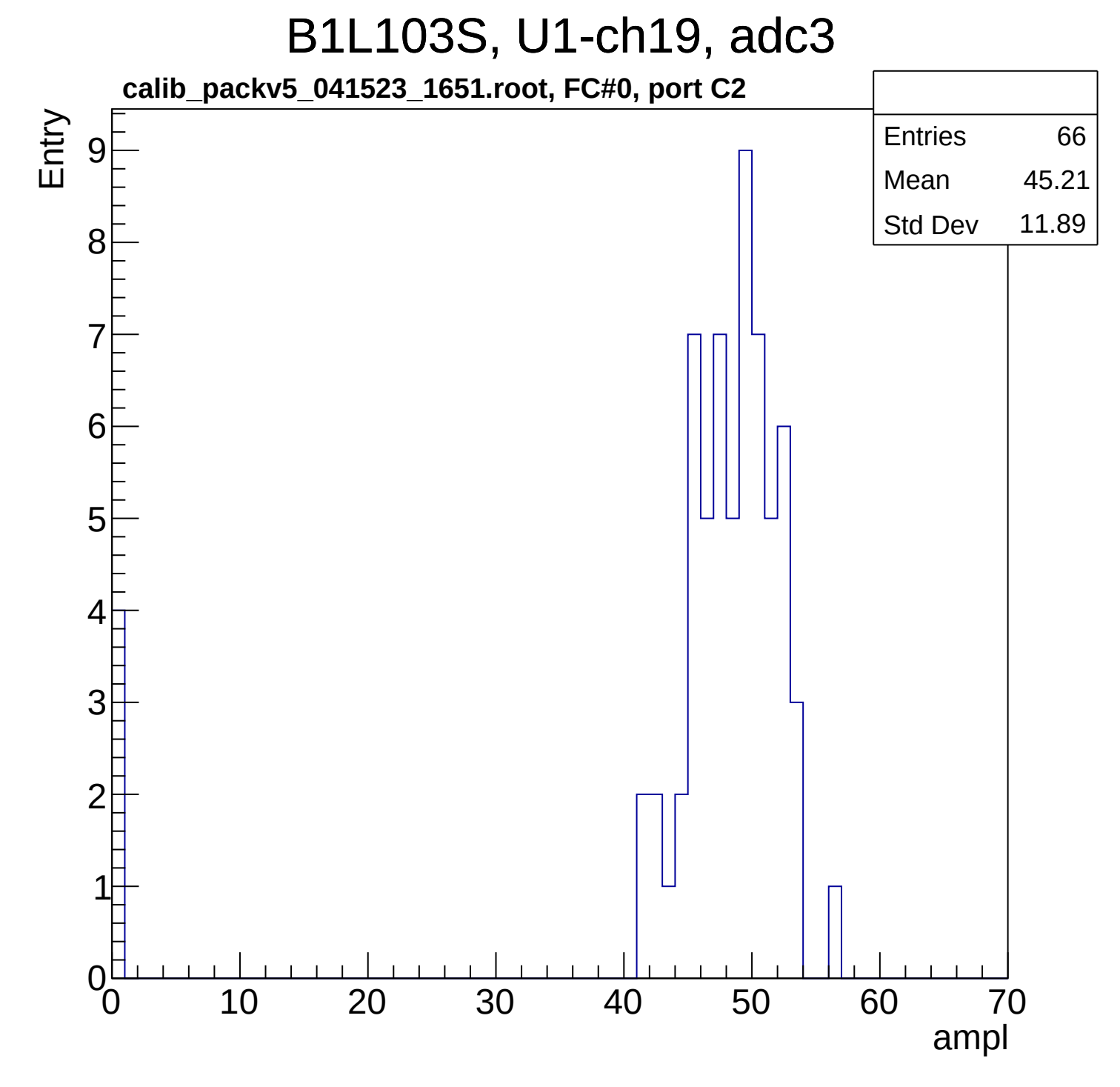
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch19, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 45.21
Std Dev 11.89
Entry
ampl
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2
3
4
5
6
7
8
9
0
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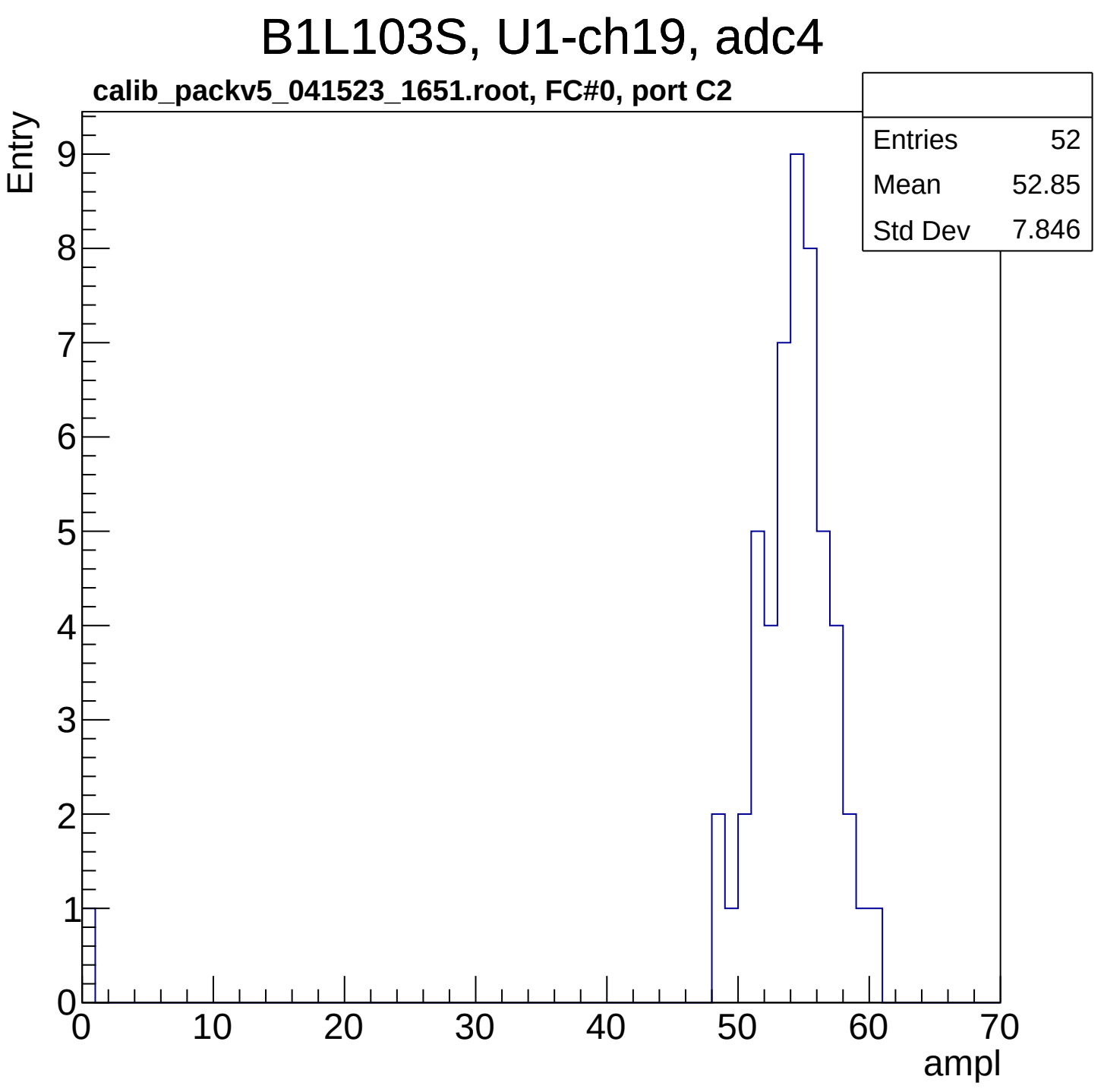
B1L103S, U1-ch19, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 52.85
Std Dev 7.846
Entry
ampl
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2
3
4
5
6
7
8
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0
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40
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60
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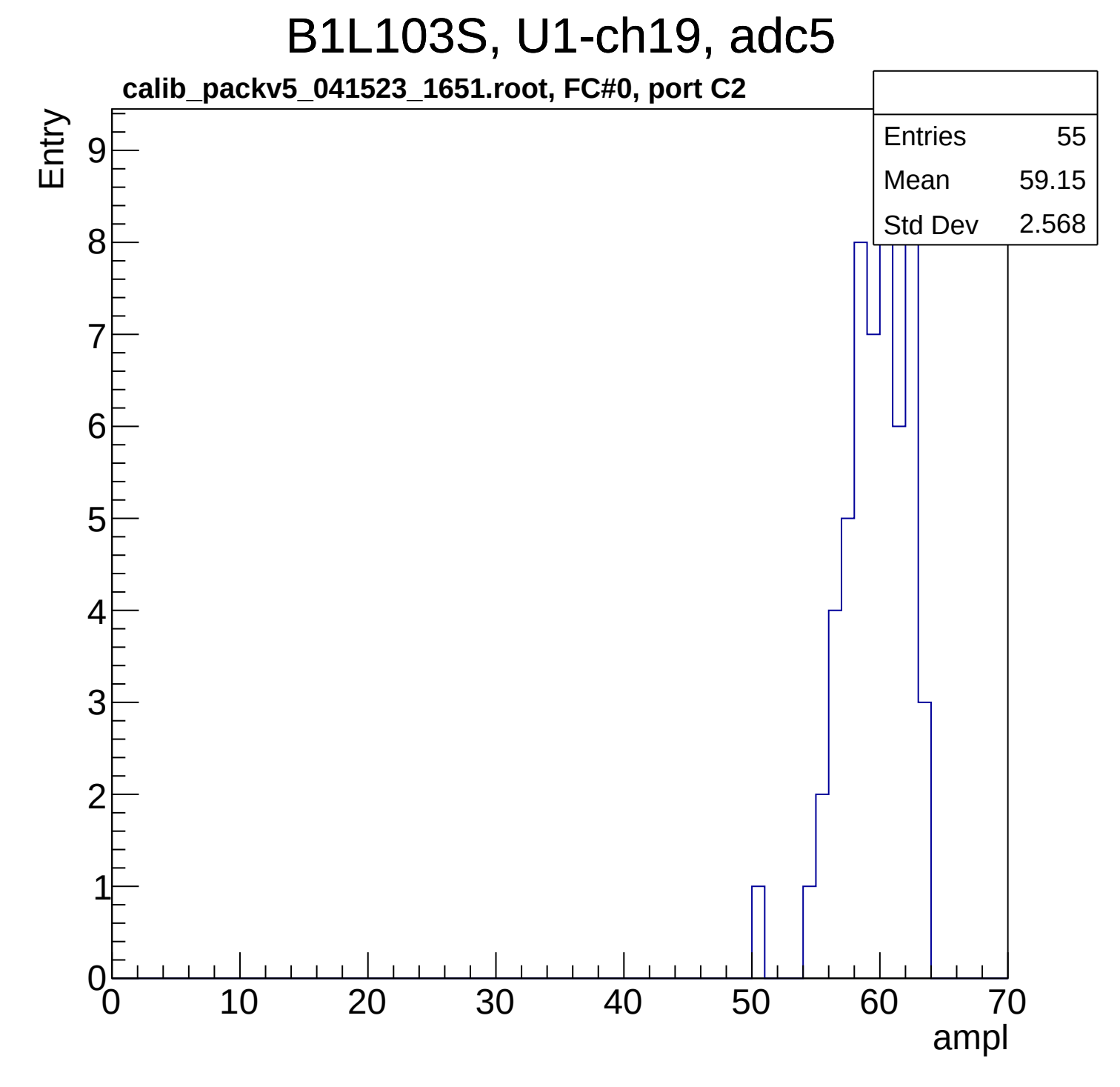
B1L103S, U1-ch19, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 59.15
Std Dev 2.568
Entry
ampl
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3
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5
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7
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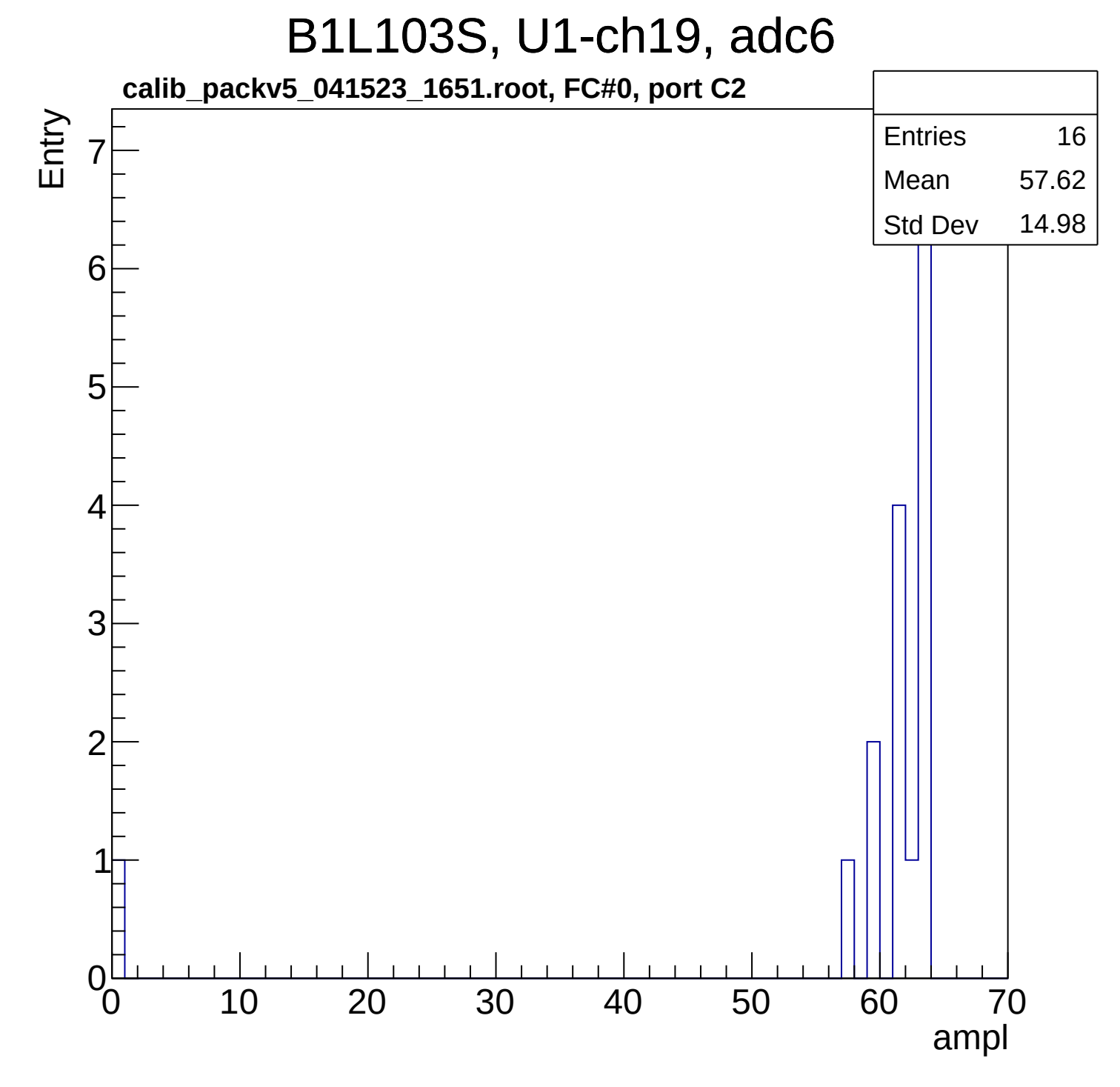
B1L103S, U1-ch19, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 16
Mean 57.62
Std Dev 14.98
Entry
ampl
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7
0
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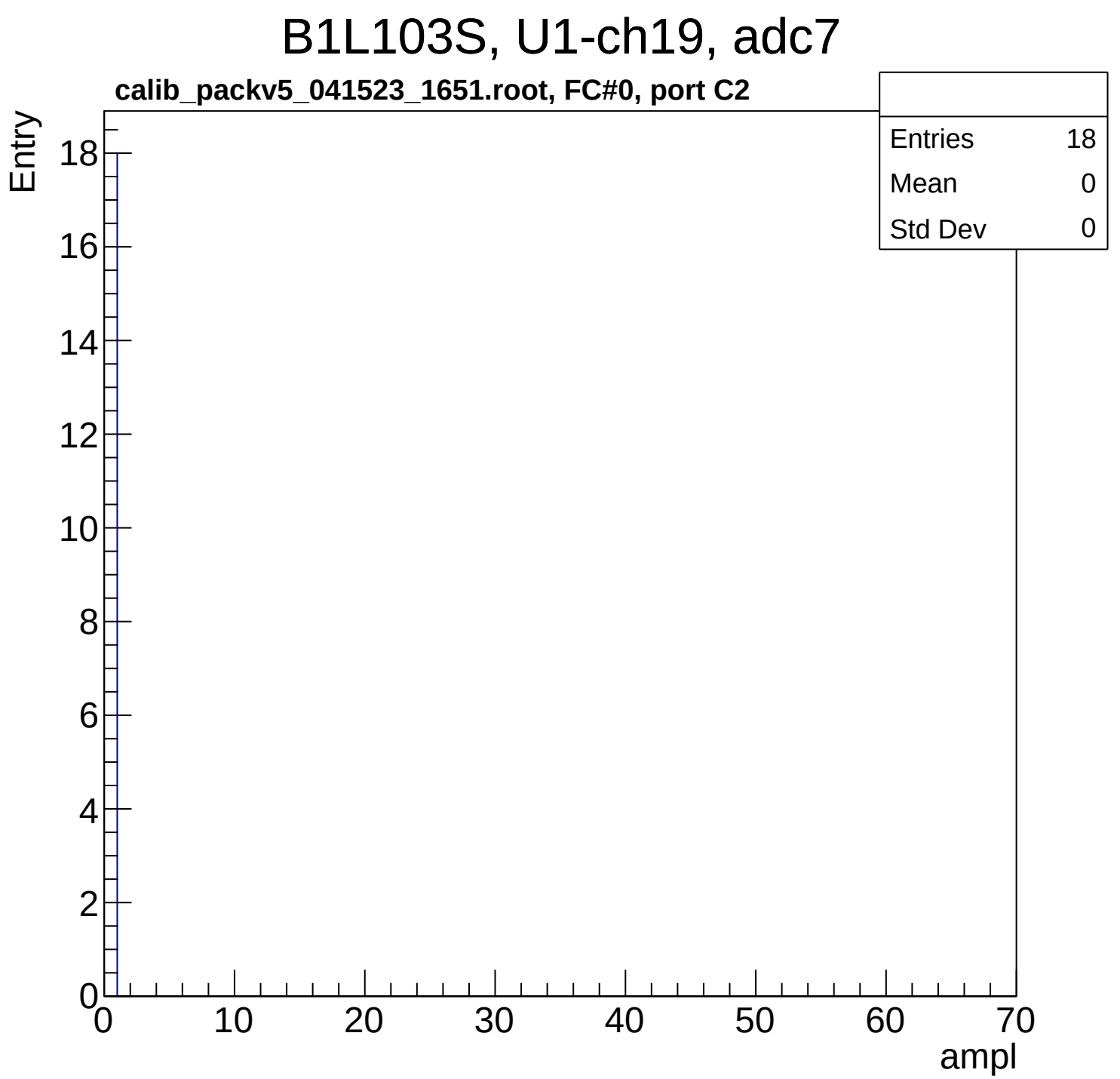
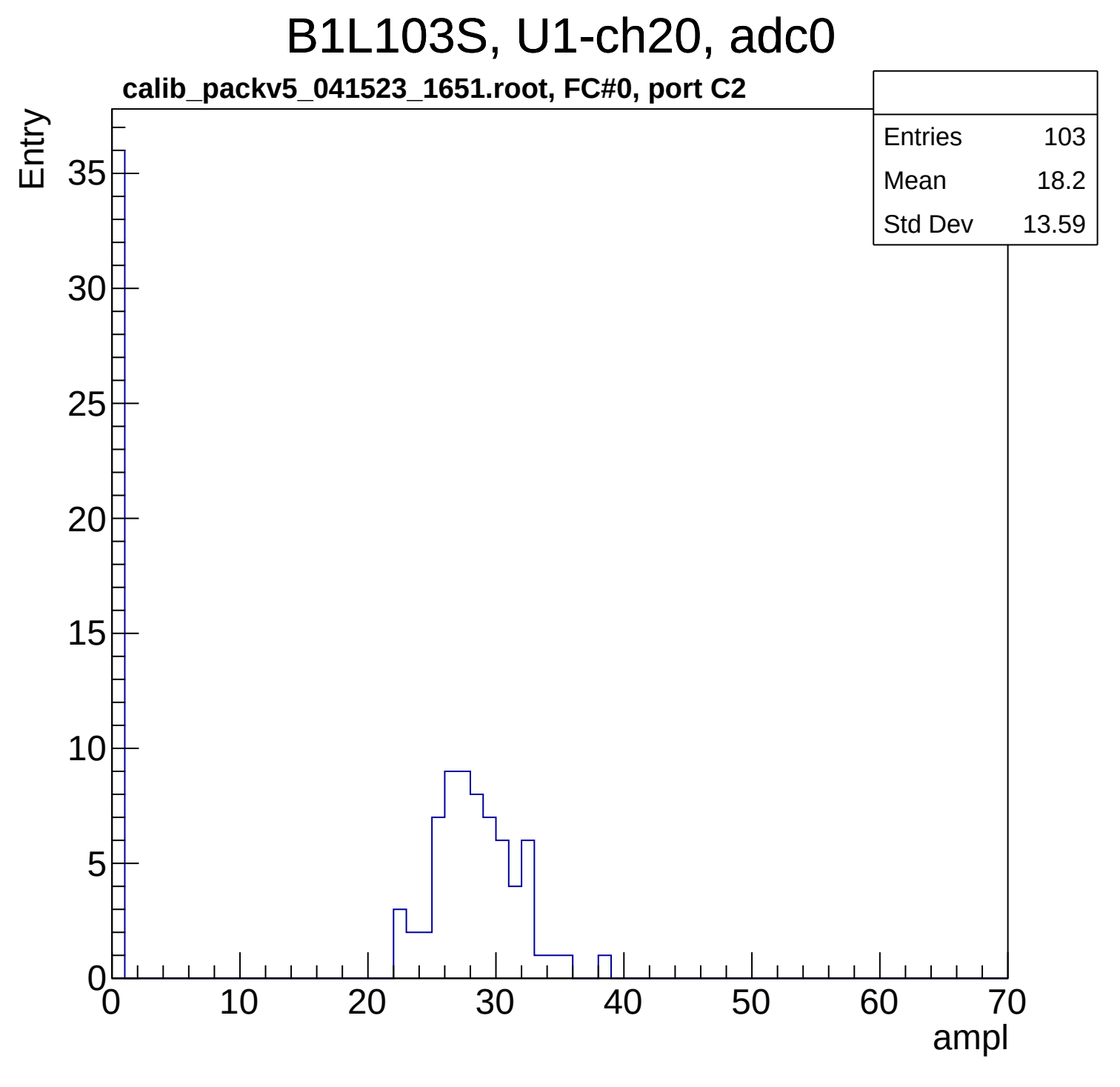

B1L103S, U1-ch19, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch20, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 103
Mean 18.2
Std Dev 13.59
Entry
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5
10
15
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25
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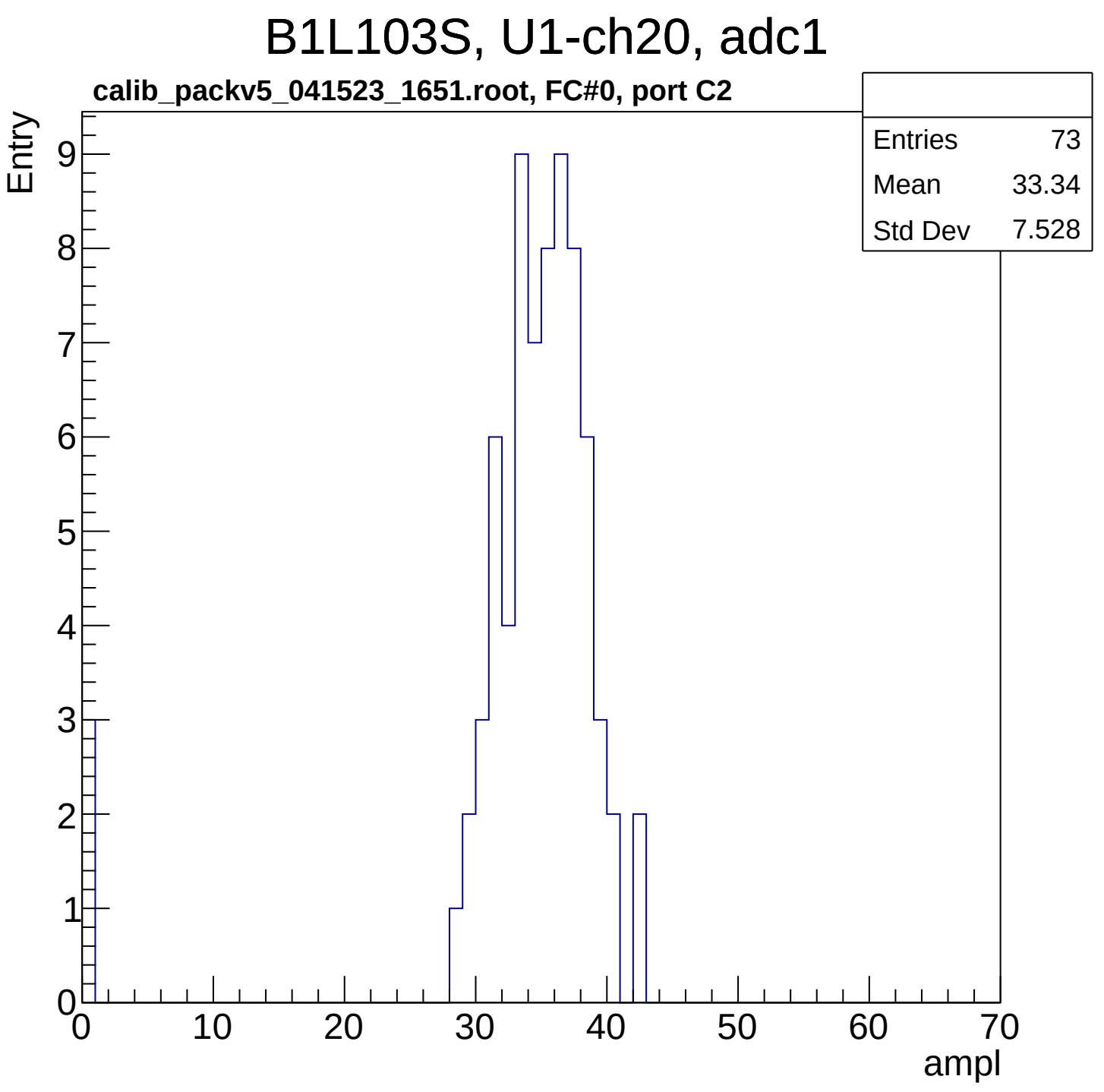
ampl


B1L103S, U1-ch20, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 33.34
Std Dev 7.528
Entry
ampl
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3
4
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6
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8
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0
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60
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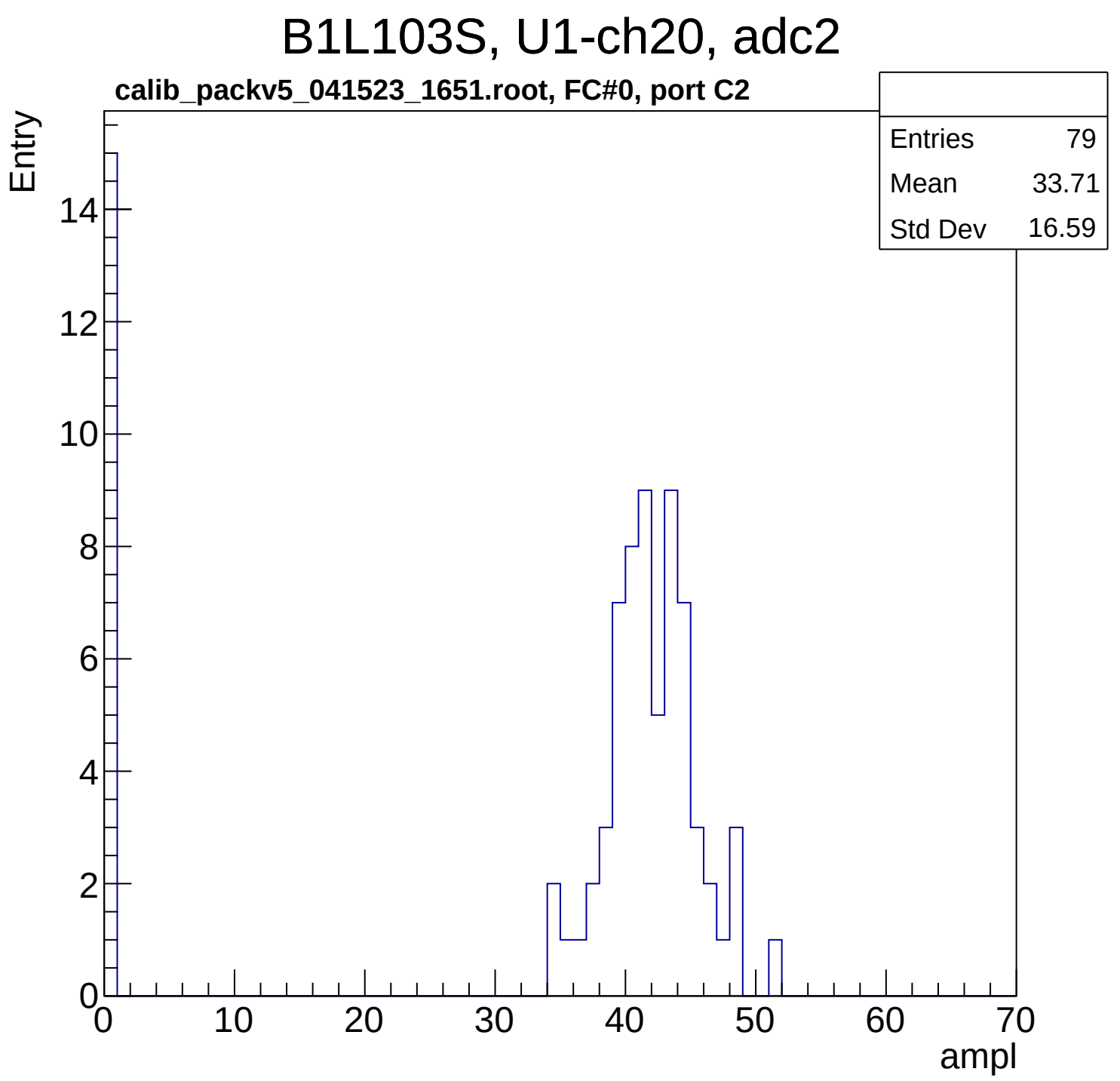
B1L103S, U1-ch20, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 33.71
Std Dev 16.59
Entry
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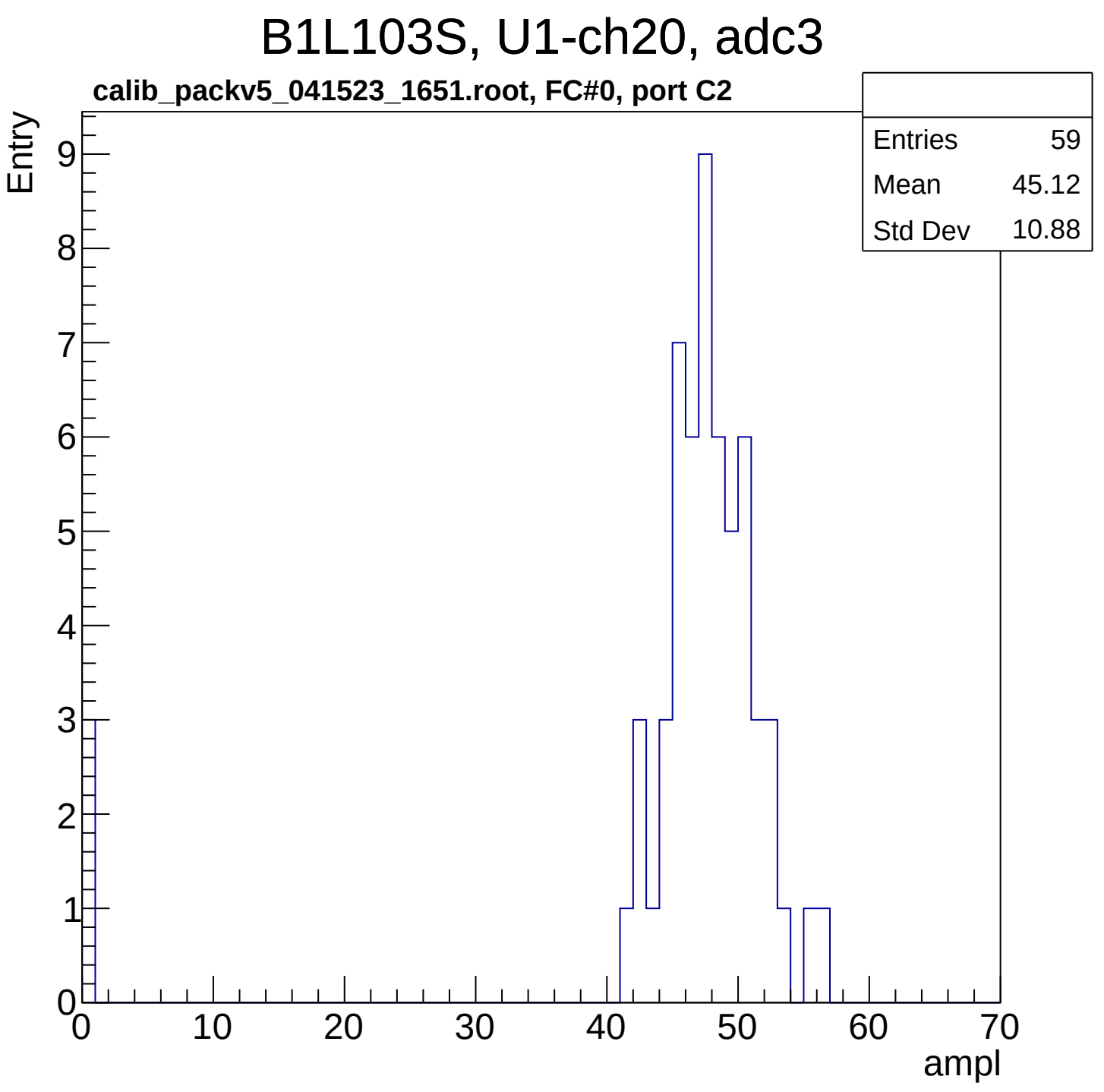
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch20, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 45.12
Std Dev 10.88
Entry
ampl
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2
3
4
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6
7
8
9
0
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20
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60
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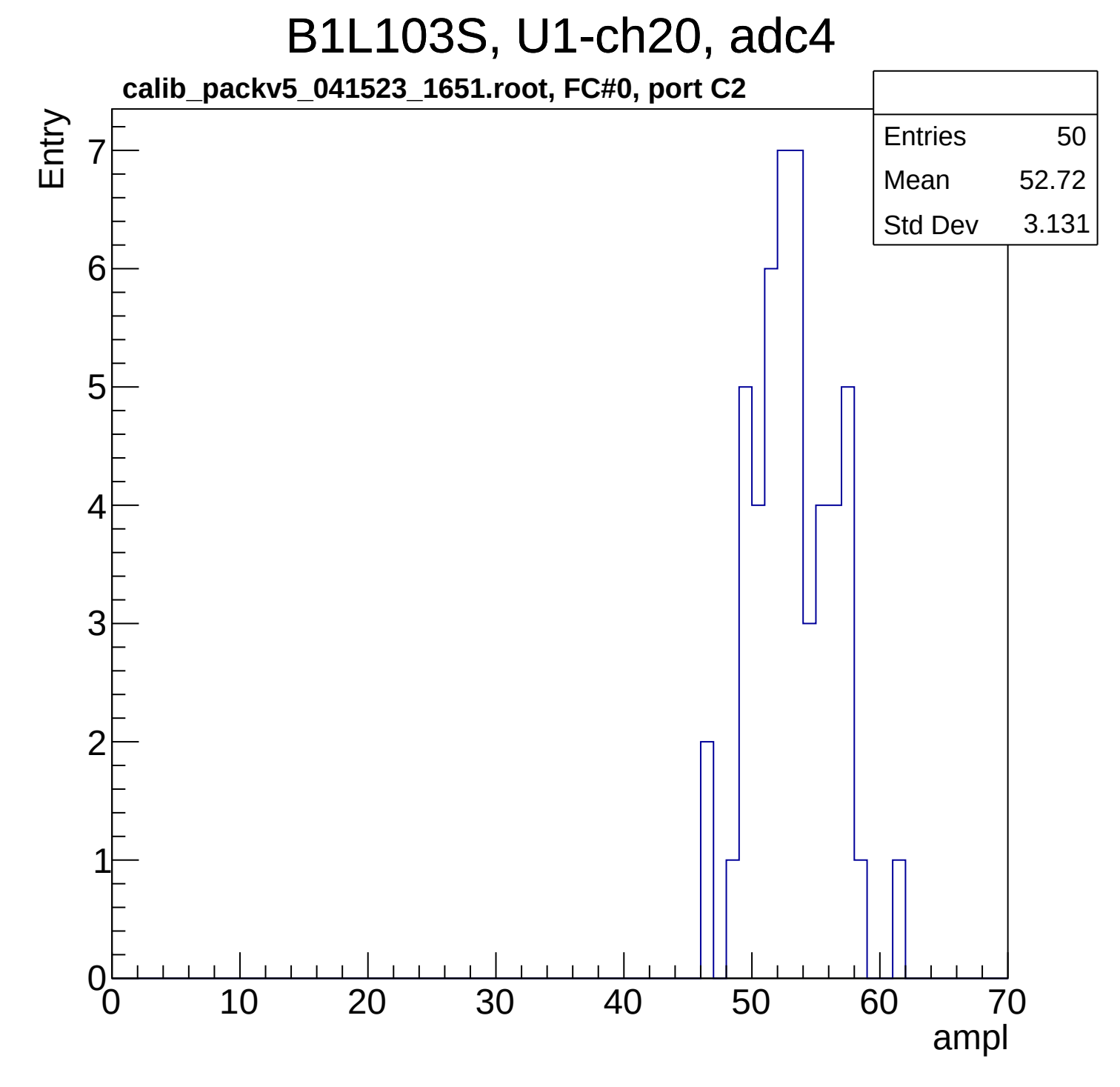
B1L103S, U1-ch20, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 52.72
Std Dev 3.131
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
30
40
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60
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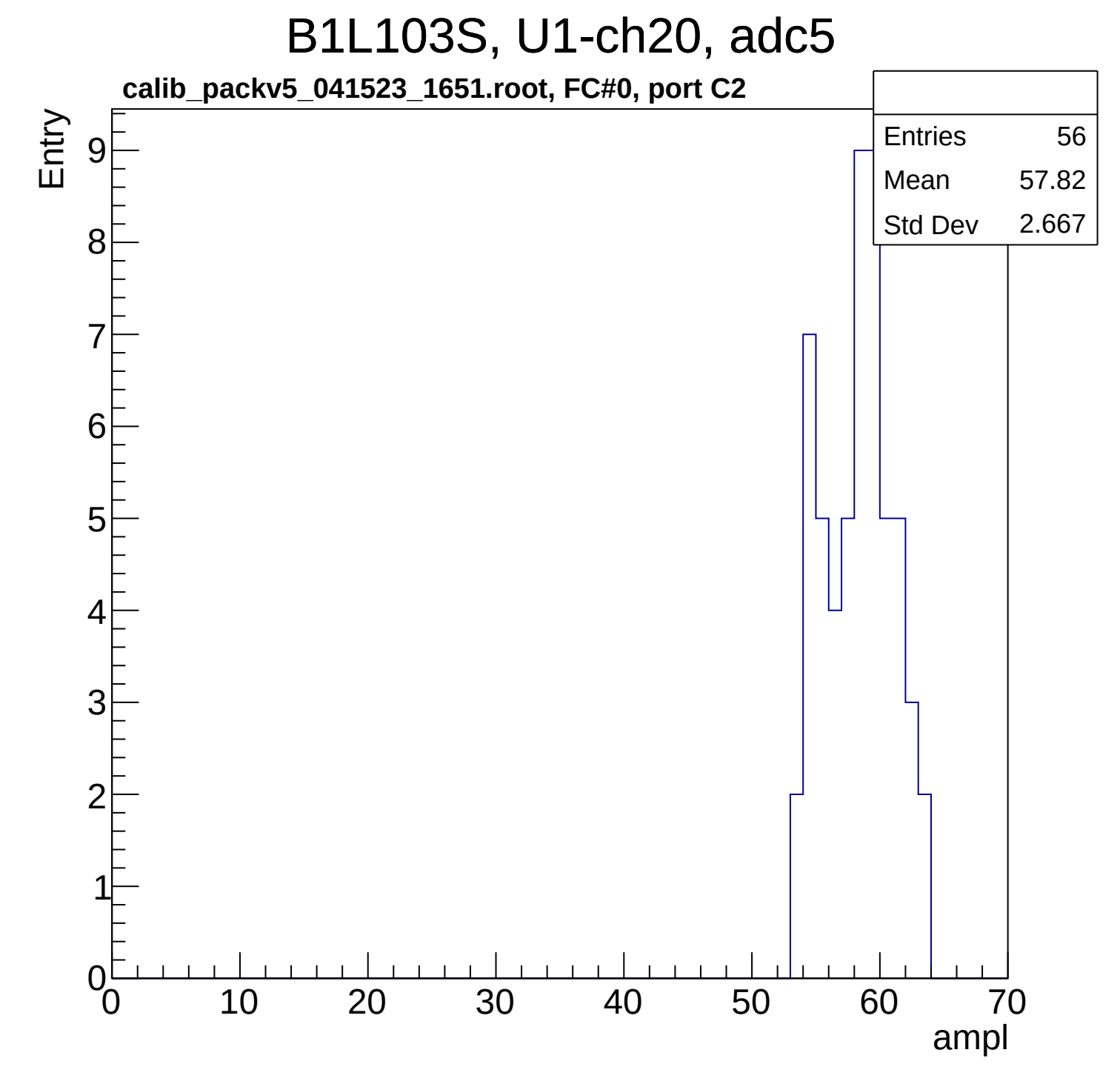
B1L103S, U1-ch20, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 57.82
Std Dev 2.667
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
50
60
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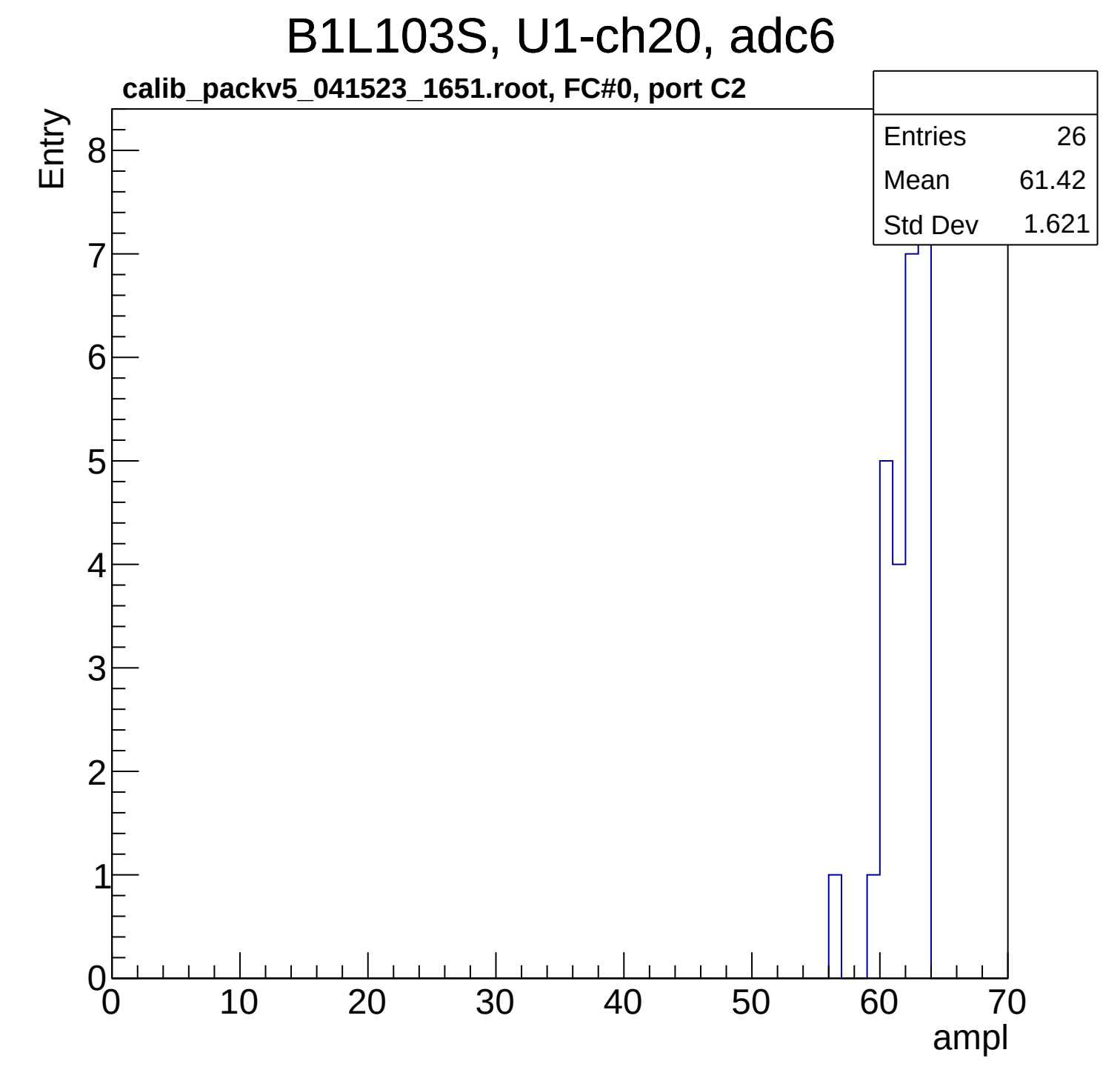
B1L103S, U1-ch20, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 26
Mean 61.42
Std Dev 1.621
Entry
ampl
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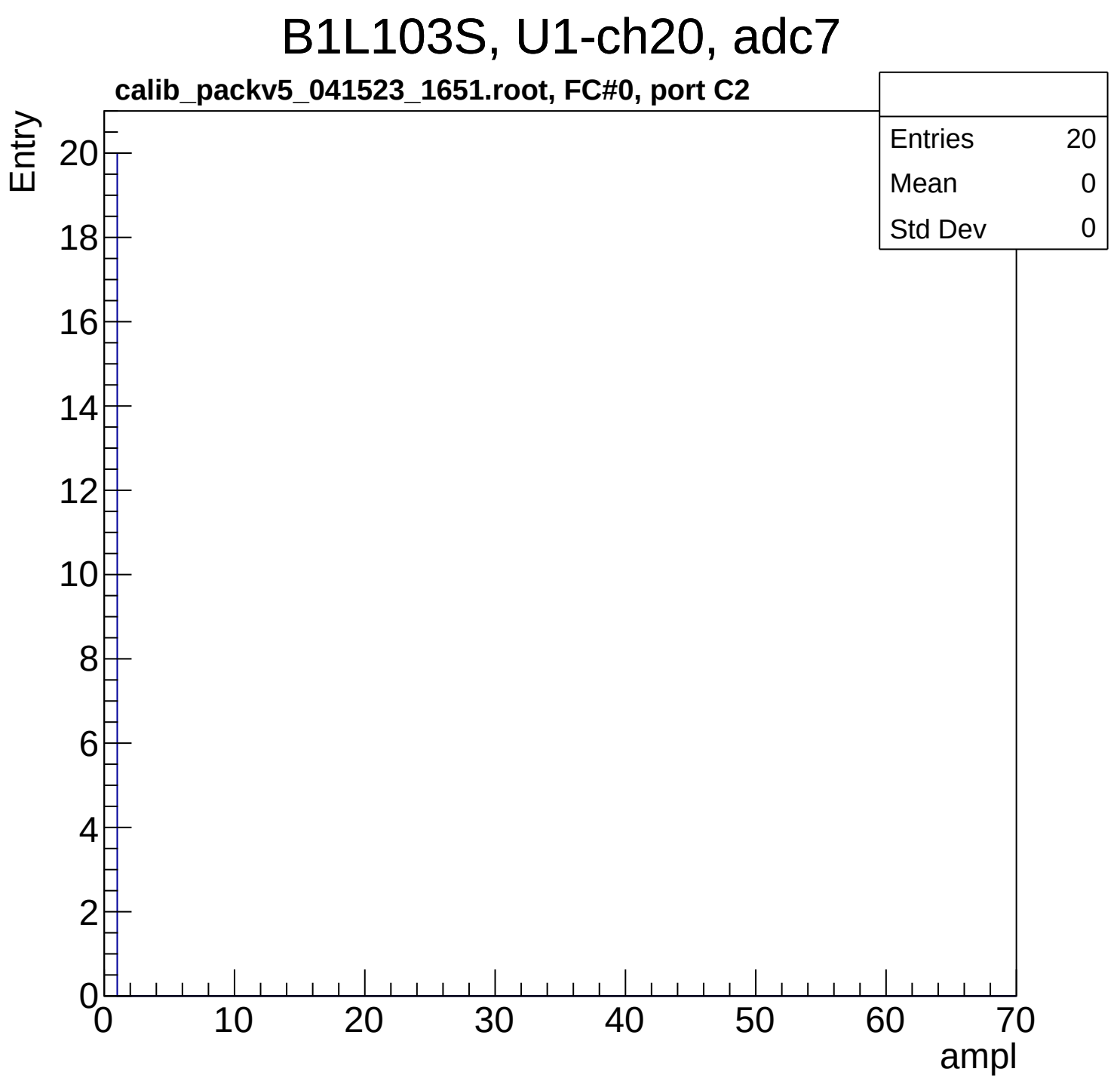
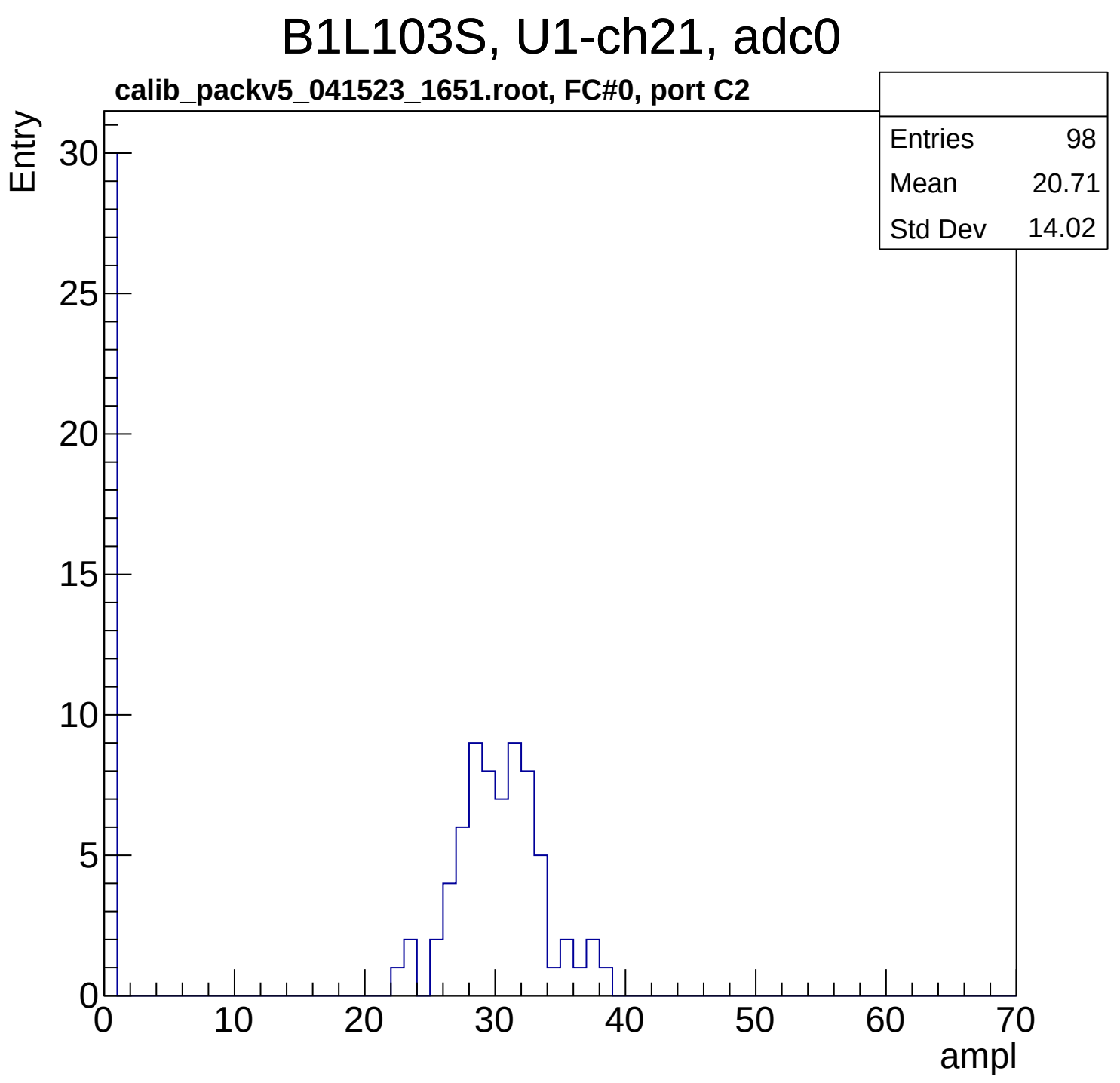
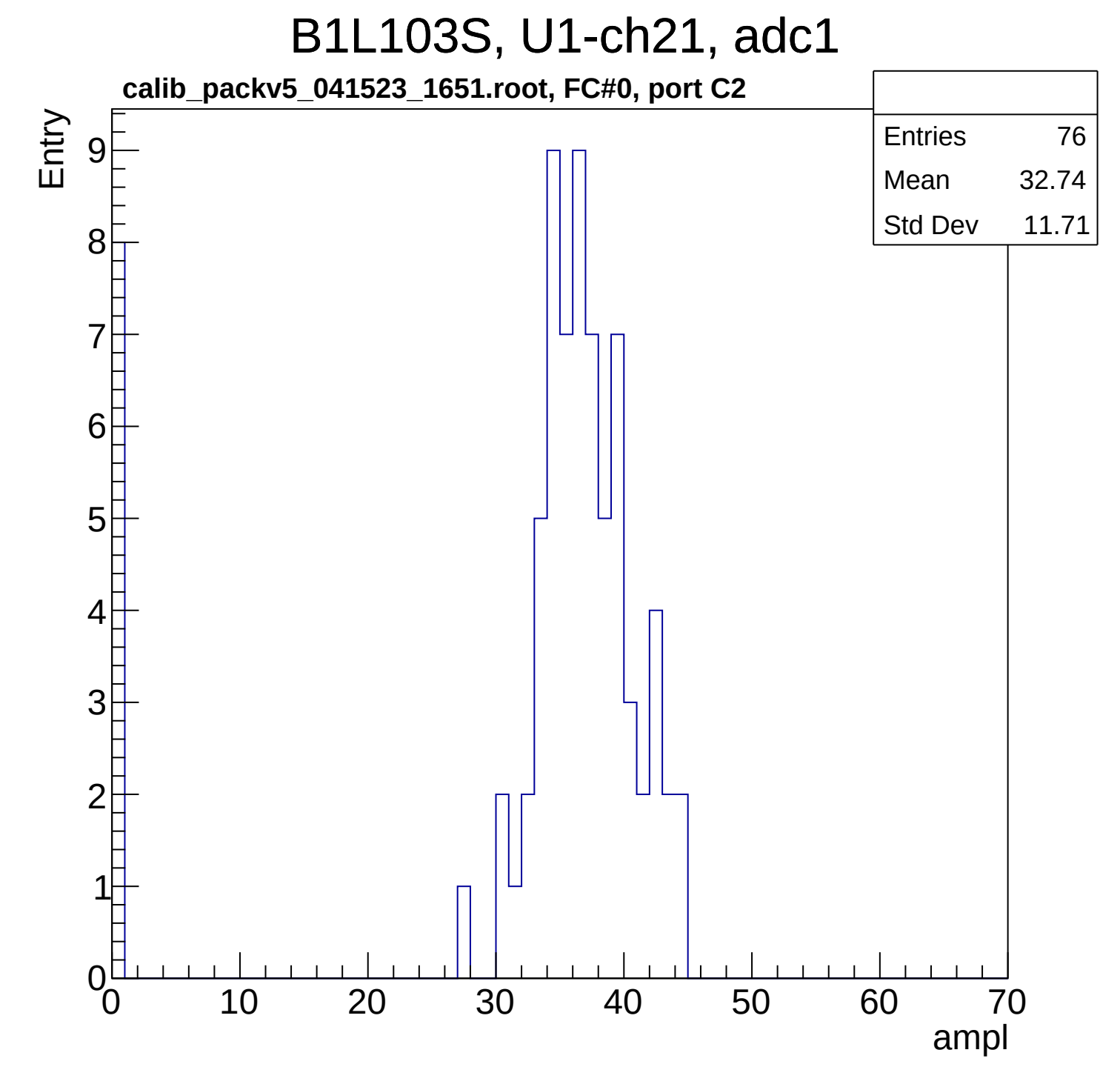
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U1-ch20, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch21, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 98
Mean 20.71
Std Dev 14.02
Entry
0
5
10
15
20
25
30
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch21, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 32.74
Std Dev 11.71
Entry
ampl
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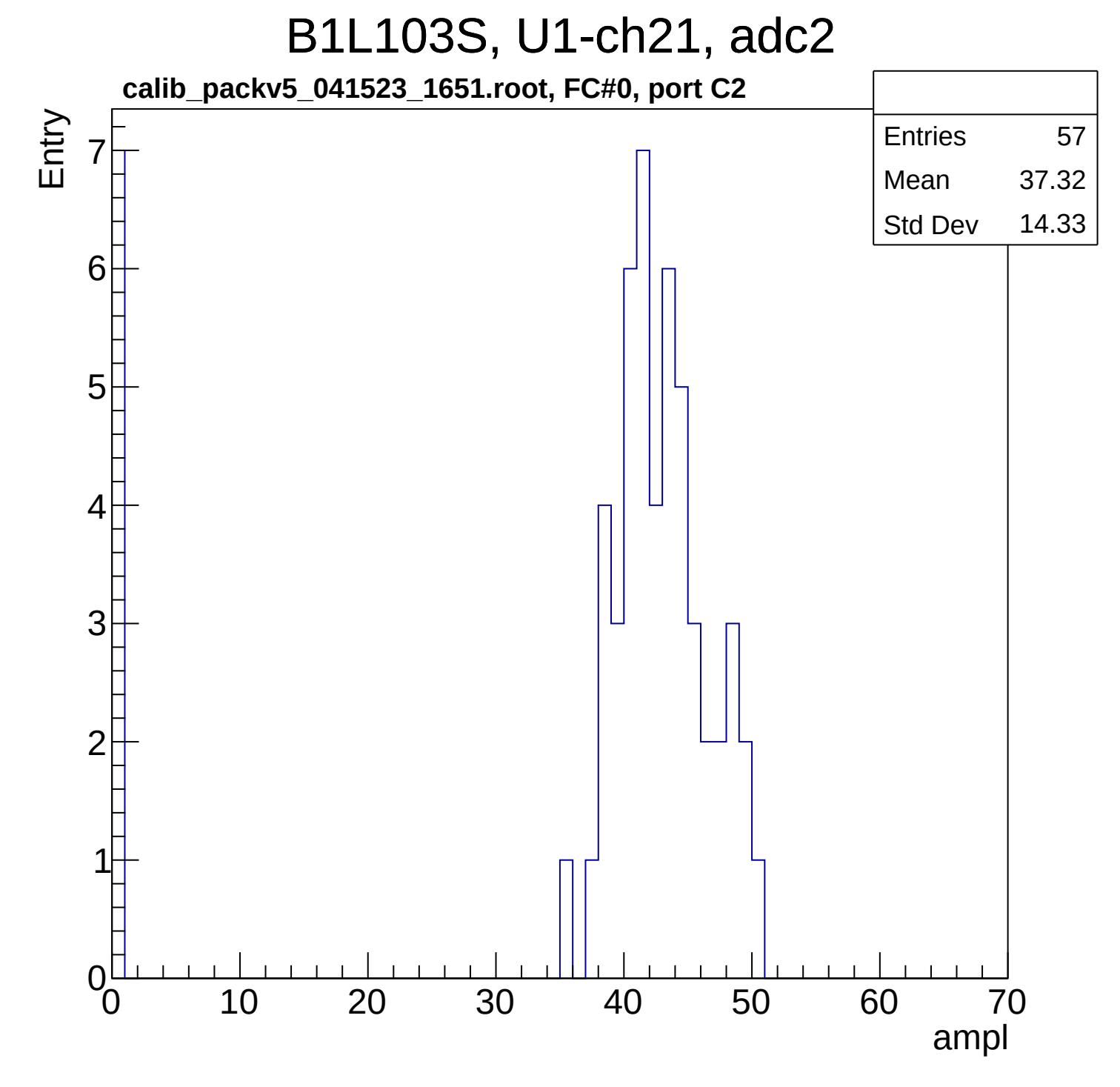
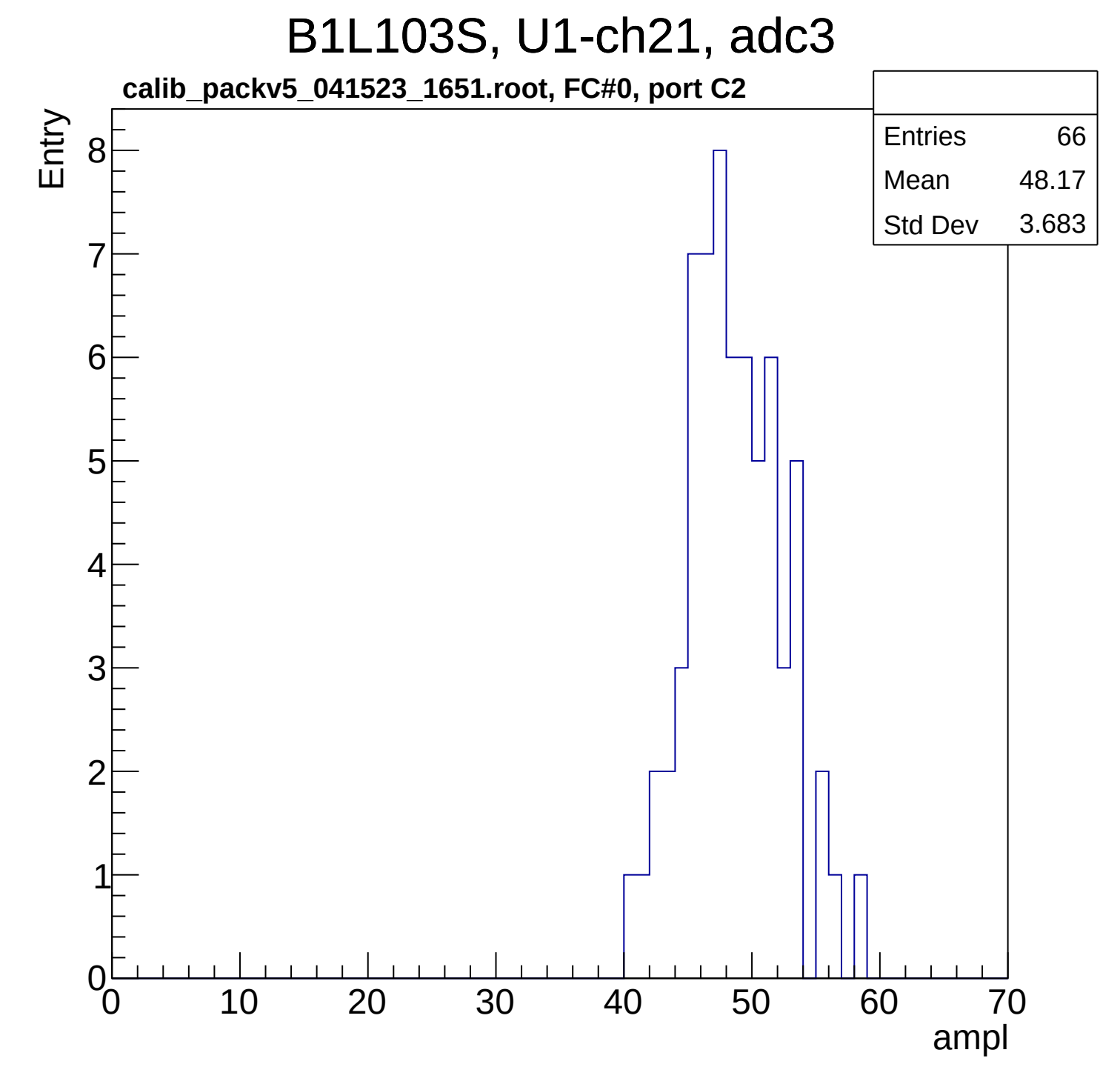
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U1-ch21, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 37.32
Std Dev 14.33
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U1-ch21, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 48.17
Std Dev 3.683
Entry
ampl
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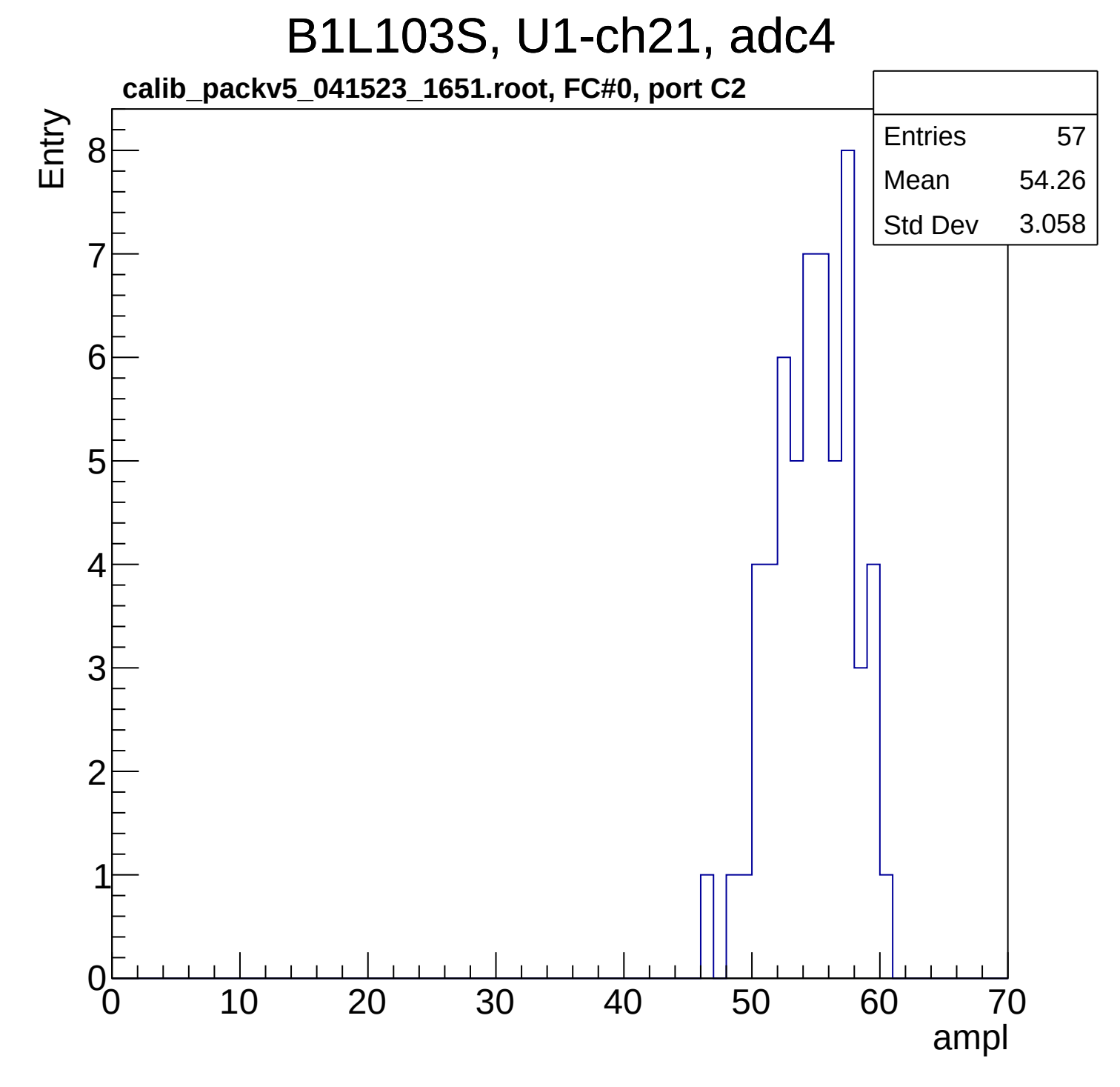
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U1-ch21, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 54.26
Std Dev 3.058
Entry
ampl
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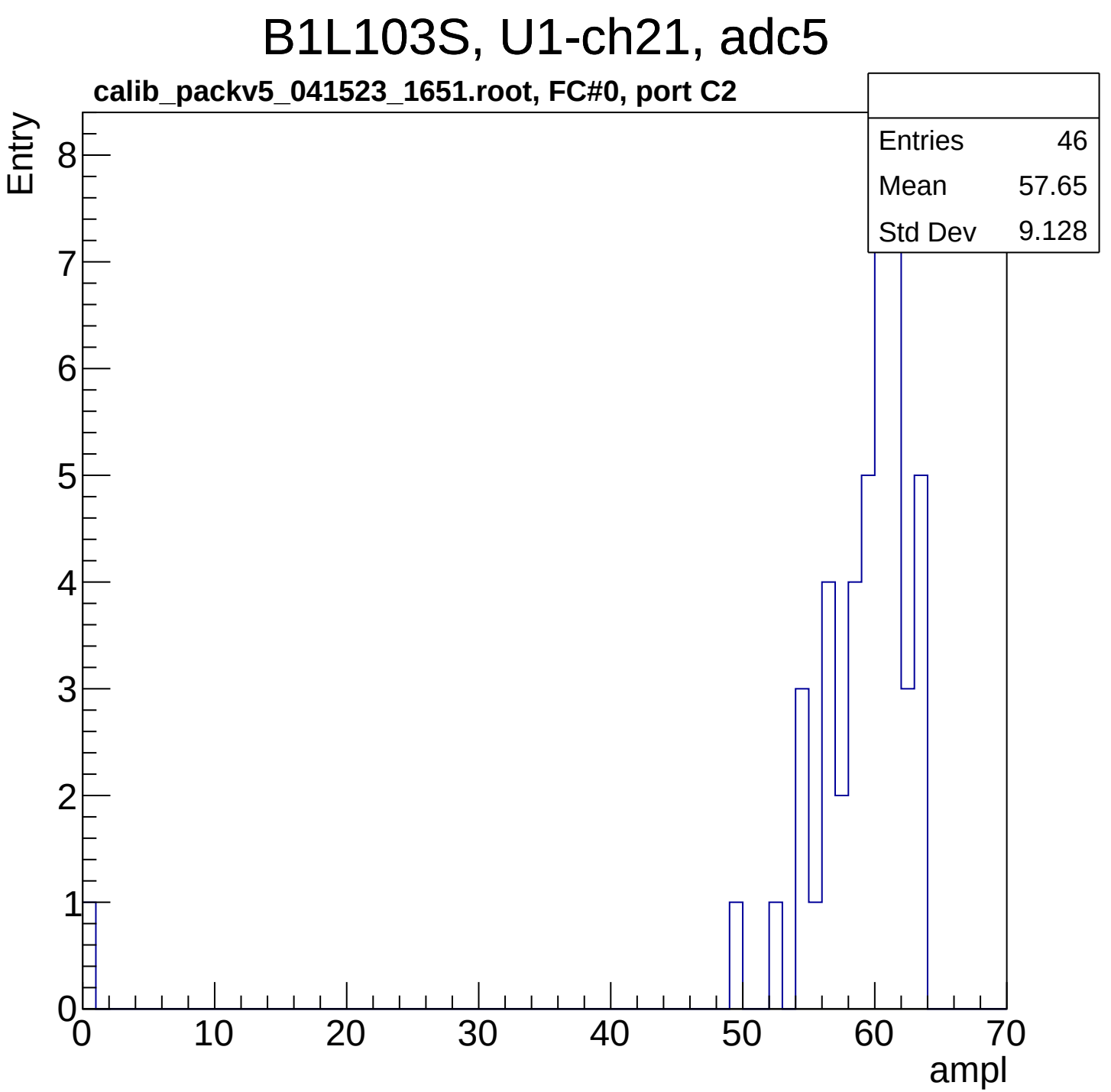
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U1-ch21, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 57.65
Std Dev 9.128
Entry
ampl
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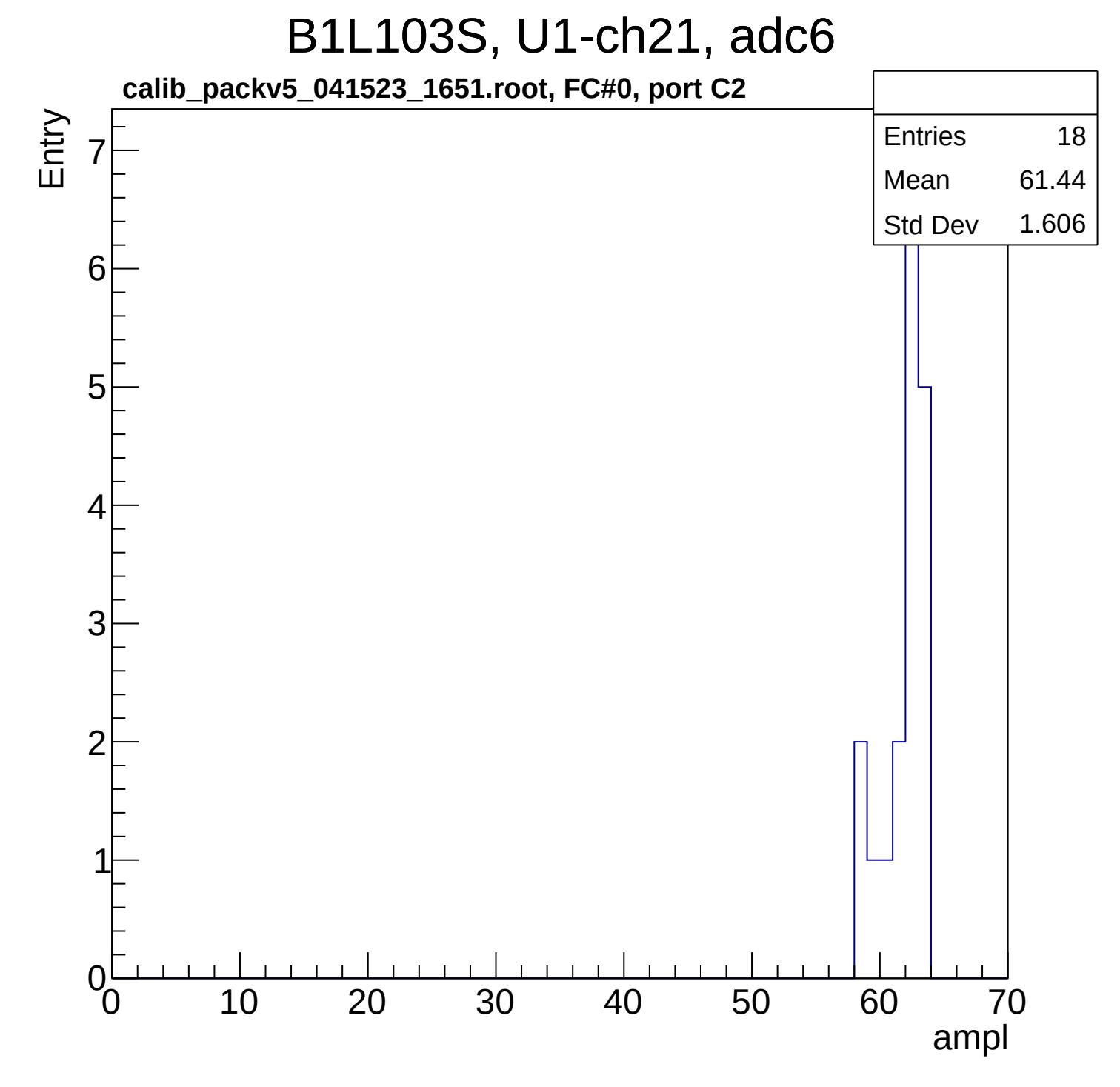
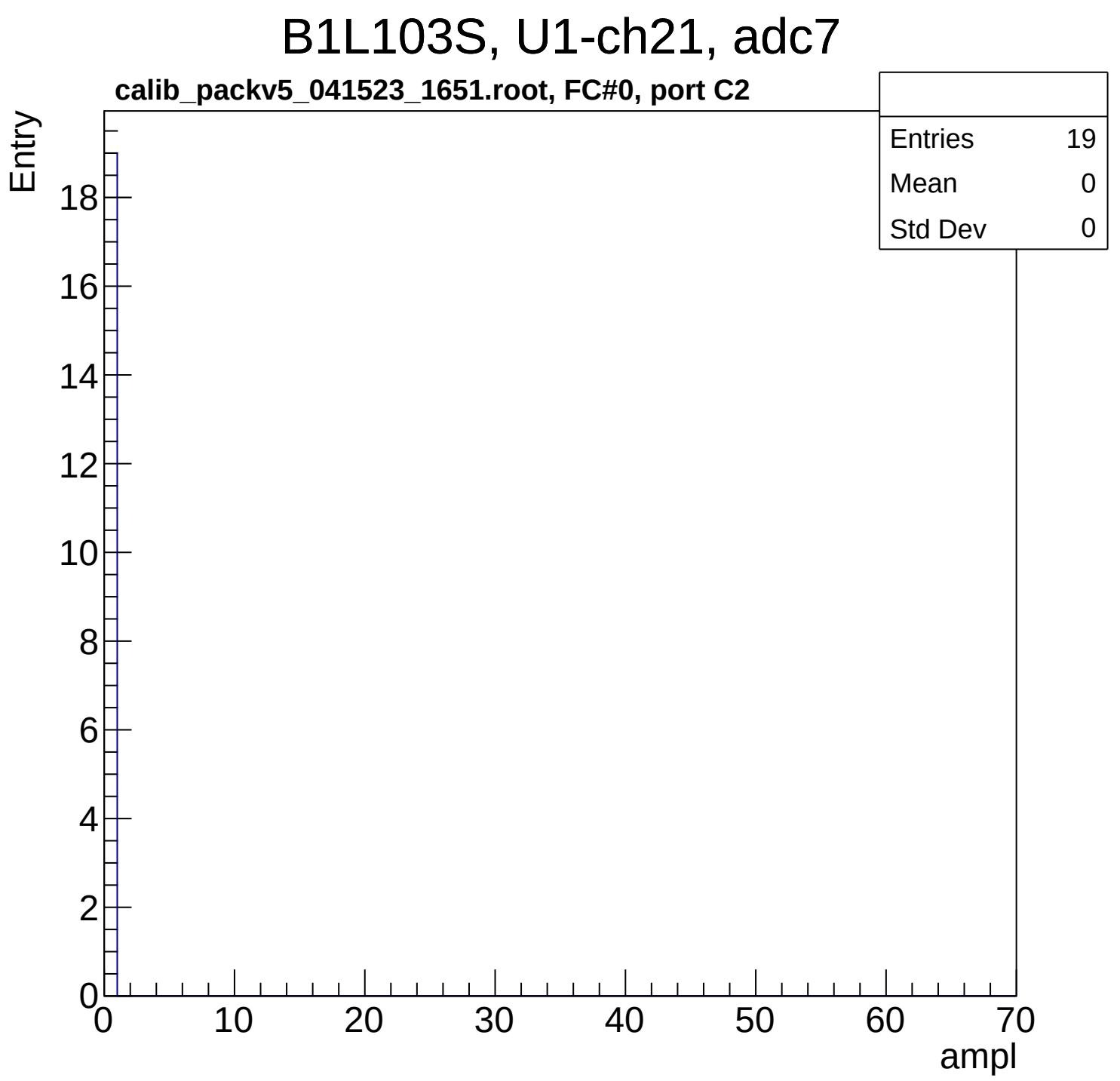
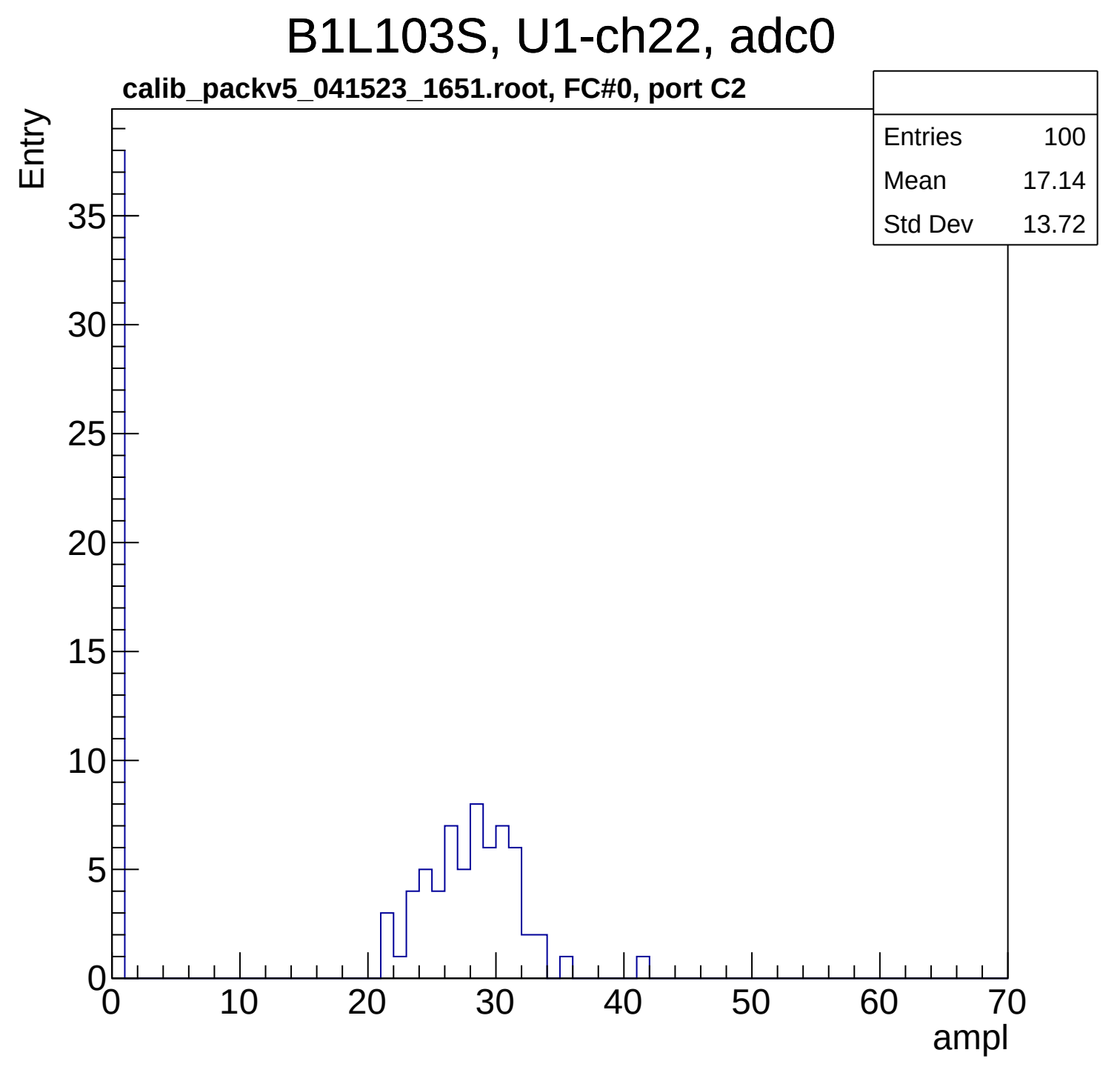
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U1-ch21, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 61.44
Std Dev 1.606
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U1-ch21, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch22, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 100
Mean 17.14
Std Dev 13.72
Entry
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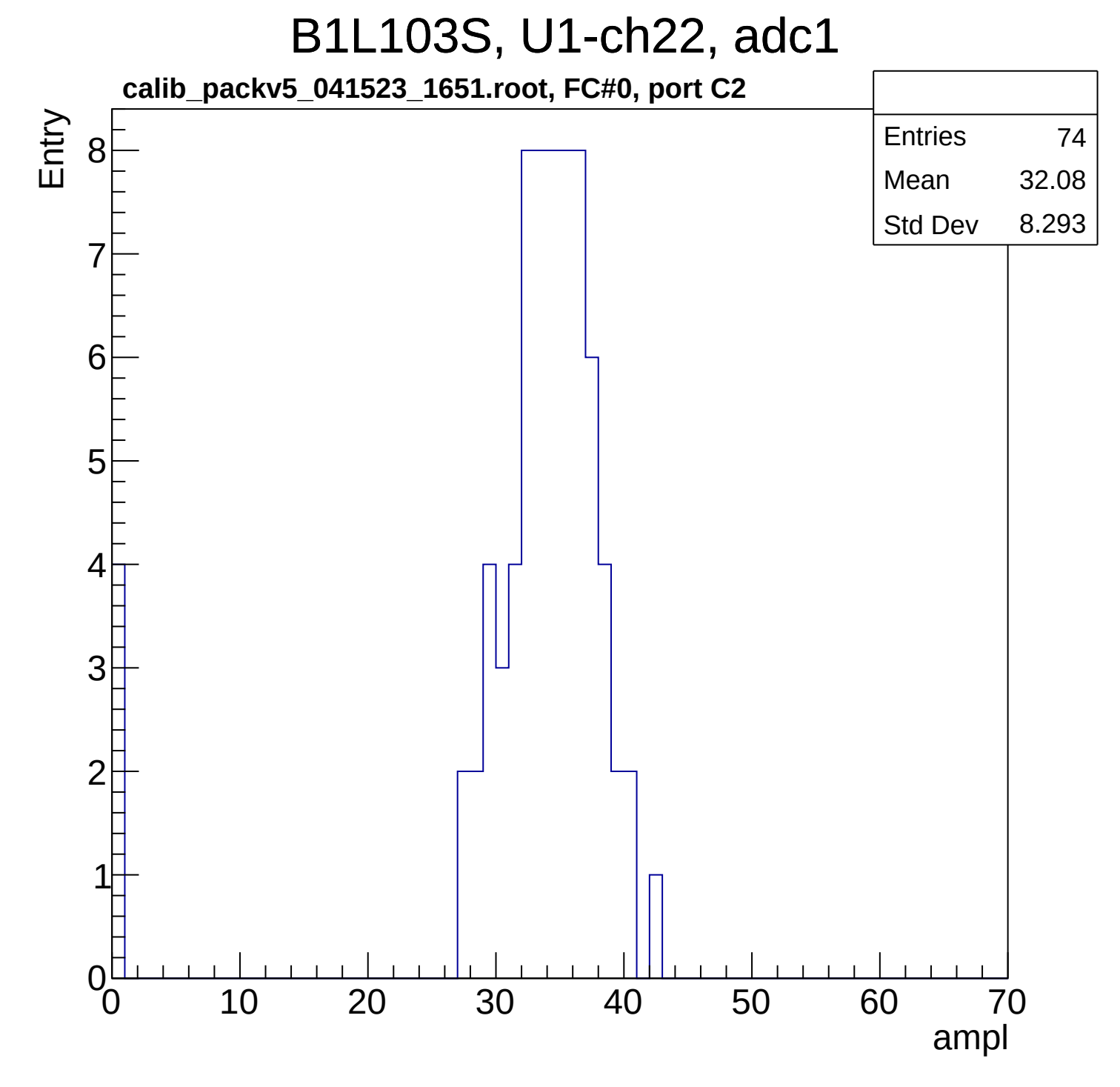
5
10
15
20
25
30
35
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch22, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 32.08
Std Dev 8.293
Entry
ampl
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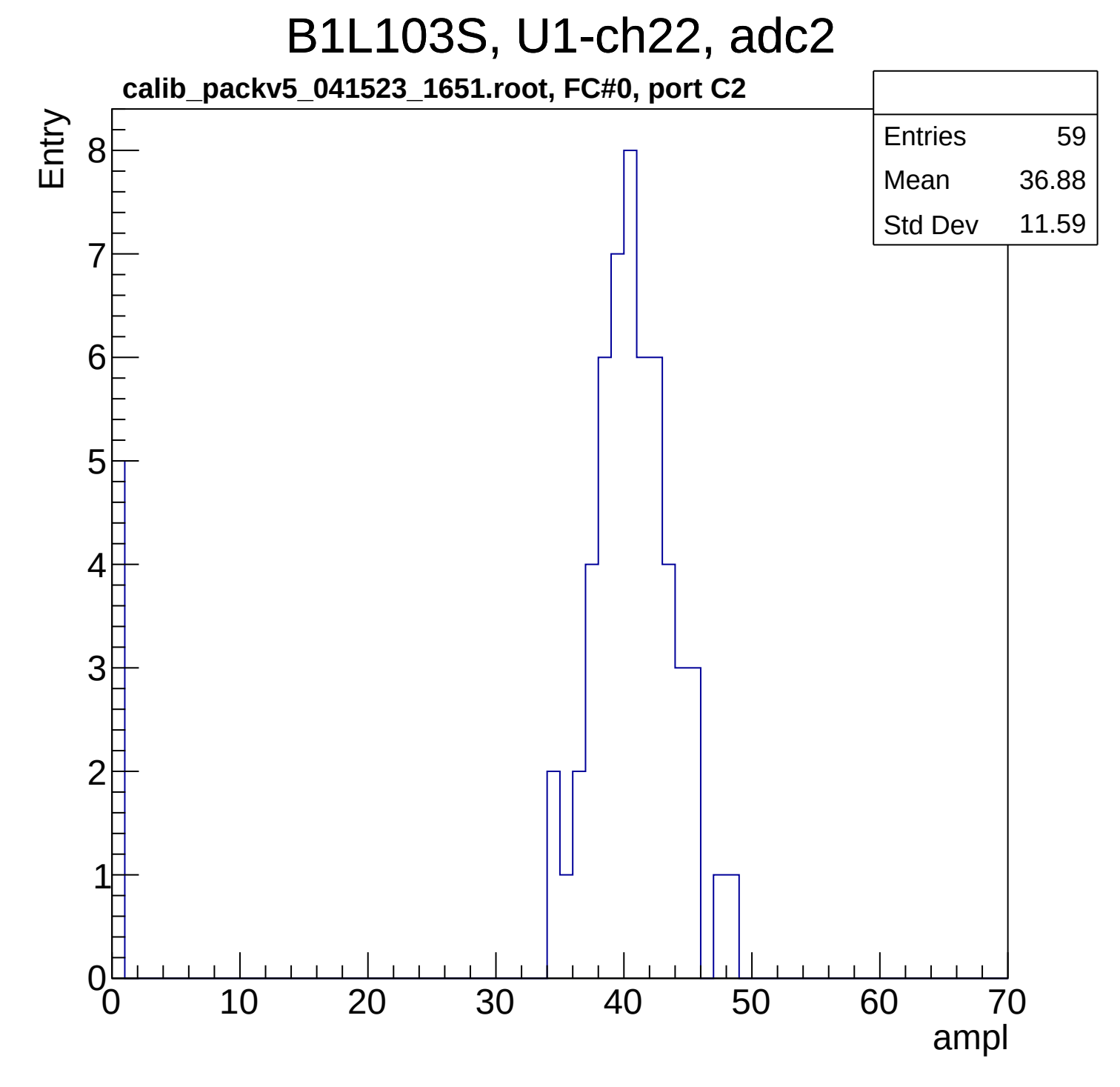
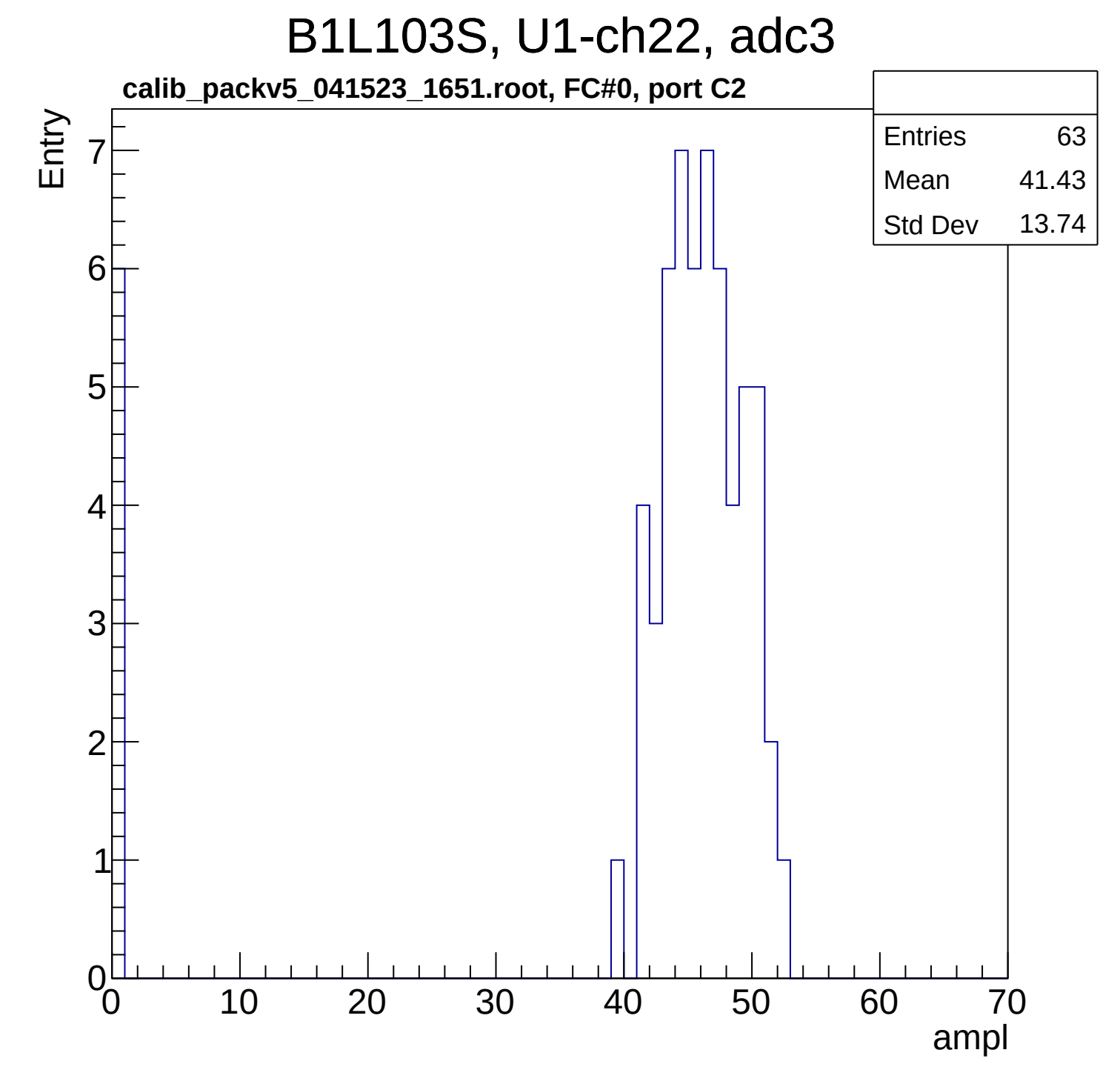
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U1-ch22, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 36.88
Std Dev 11.59
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U1-ch22, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 41.43
Std Dev 13.74
Entry
ampl
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2
3
4
5
6
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0
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20
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50
60
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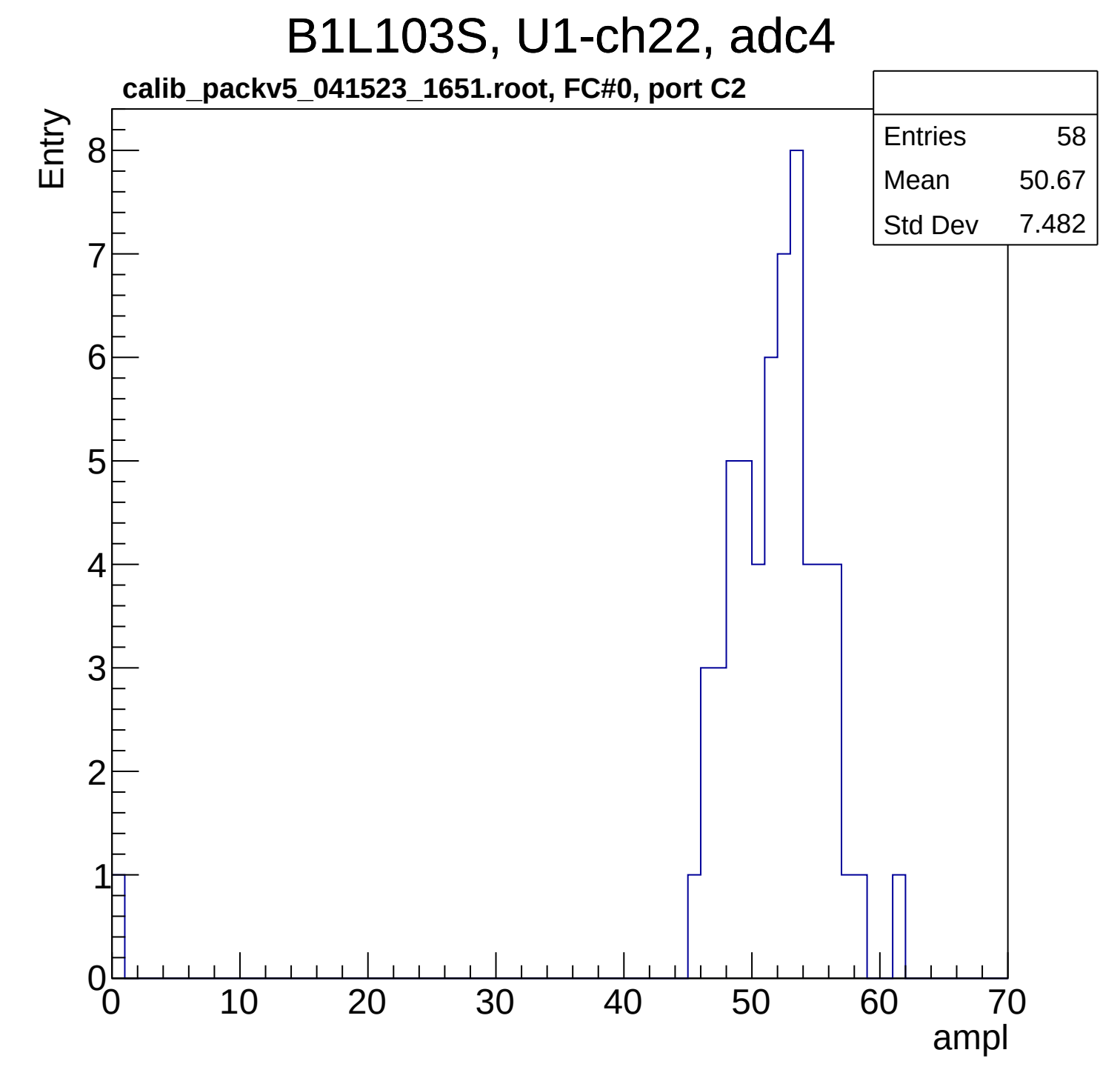
B1L103S, U1-ch22, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 50.67
Std Dev 7.482
Entry
ampl
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2
3
4
5
6
7
8
0
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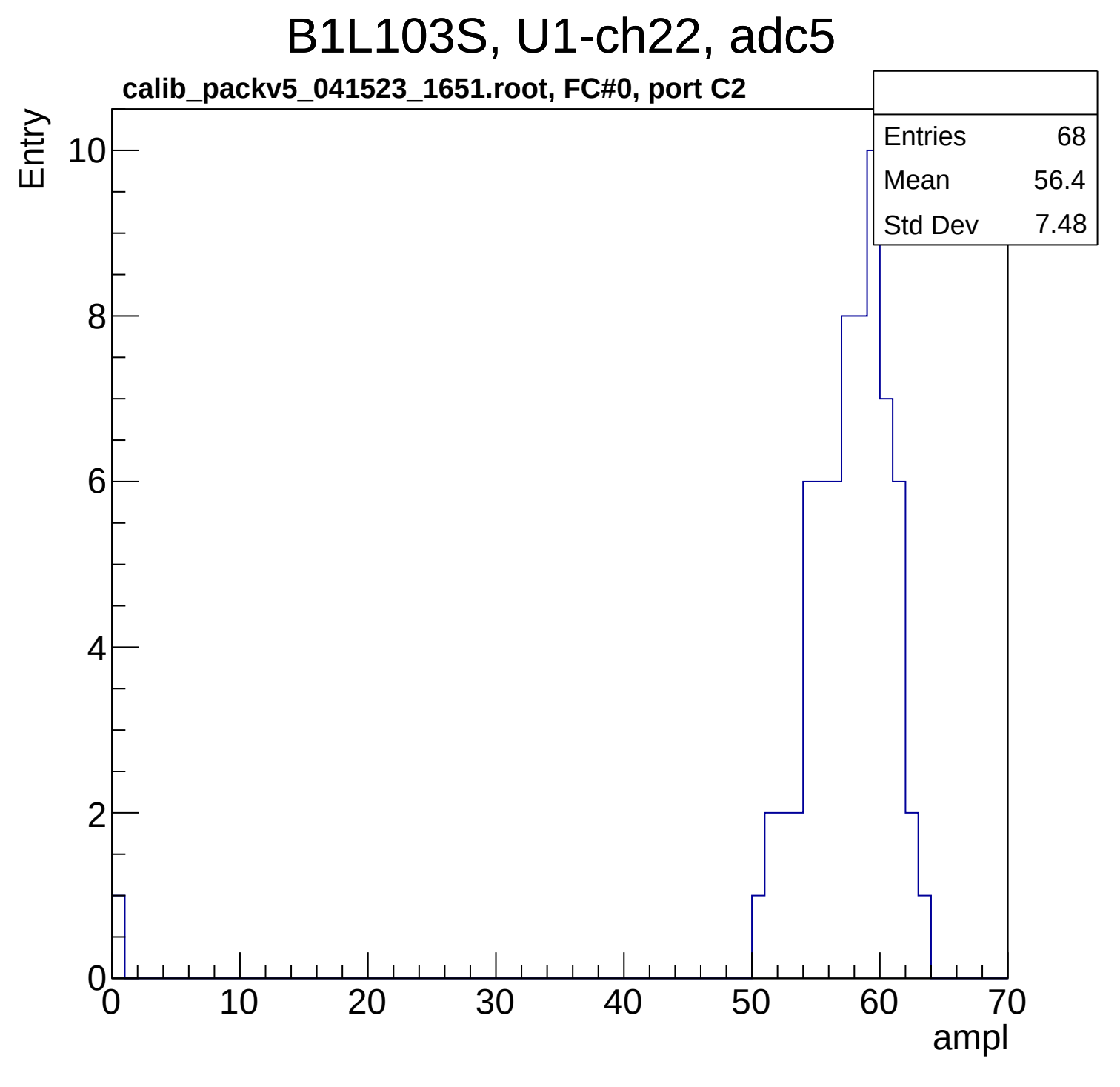
20
30
40
50
60
70


B1L103S, U1-ch22, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 56.4
Std Dev 7.48
Entry
ampl
0
2
4
6
8
10
0
10
20
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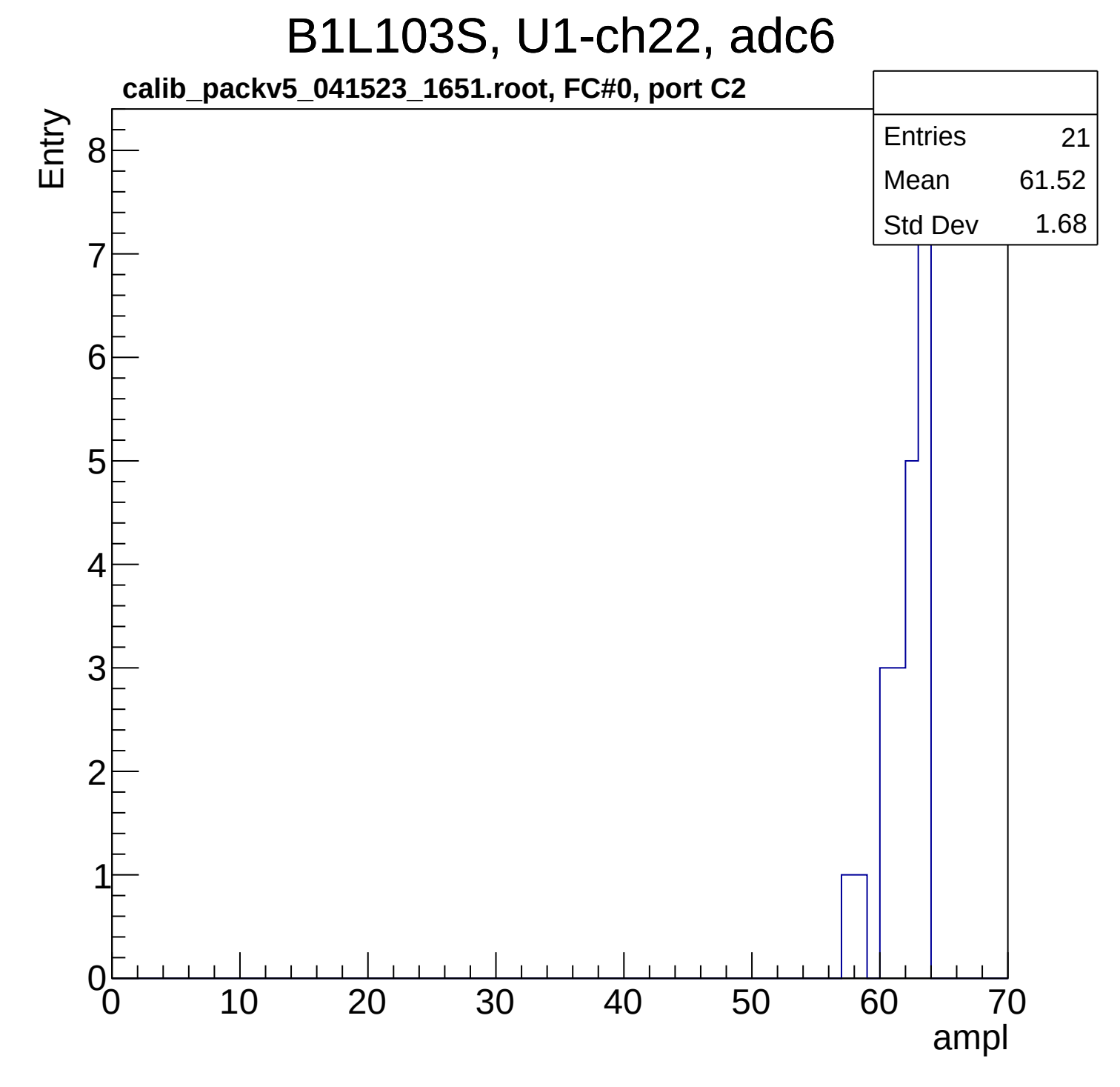
40
50
60
70


B1L103S, U1-ch22, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 61.52
Std Dev 1.68
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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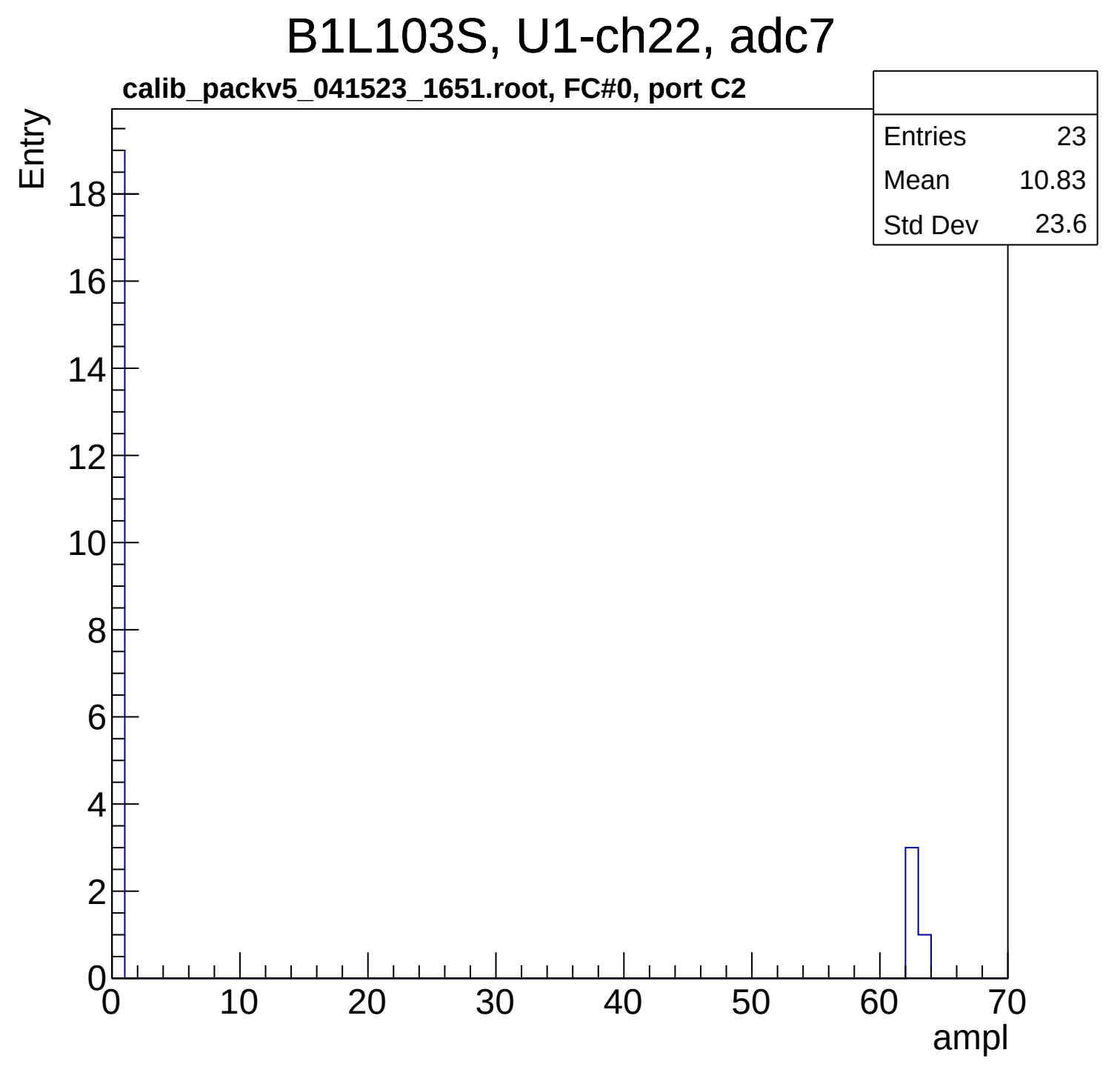
40
50
60
70


B1L103S, U1-ch22, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 23
Mean 10.83
Std Dev 23.6
Entry
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6
8
10
12
14
16
18
0
10
20
30
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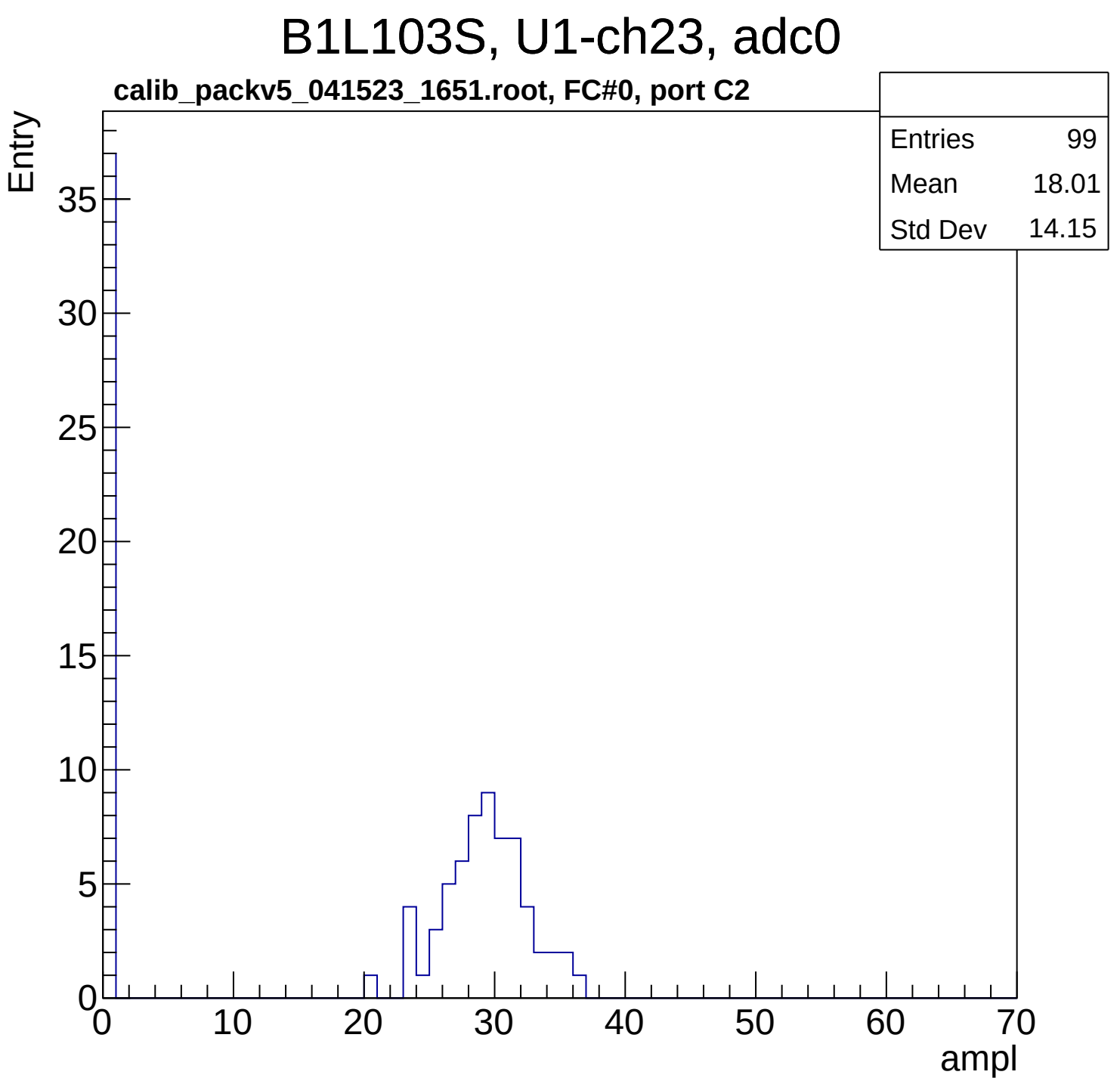
50
60
70
ampl


B1L103S, U1-ch23, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 99
Mean 18.01
Std Dev 14.15
Entry
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5
10
15
20
25
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10
20
30
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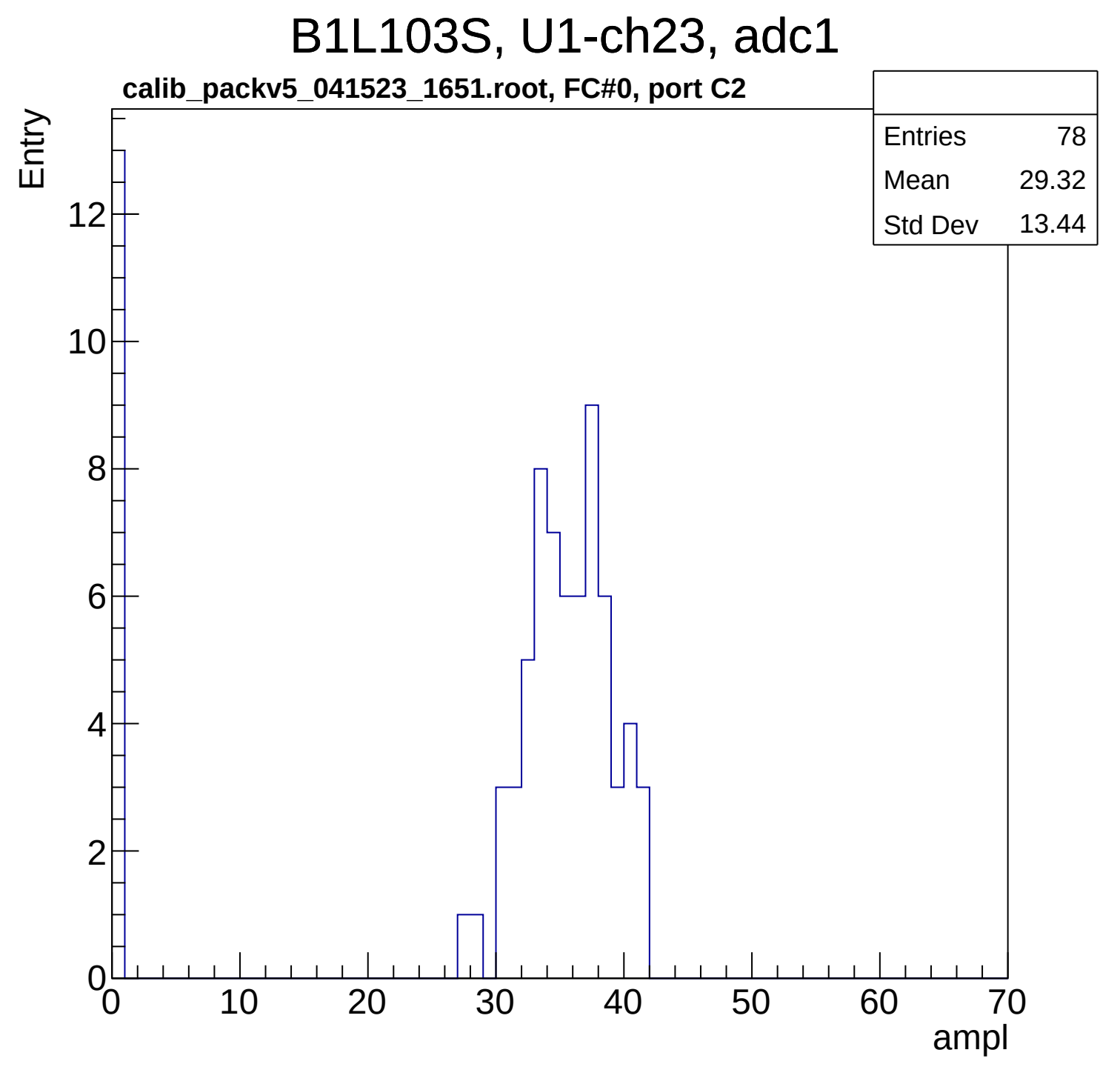
60
70
ampl


B1L103S, U1-ch23, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 29.32
Std Dev 13.44
Entry
ampl
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2
4
6
8
10
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0
10
20
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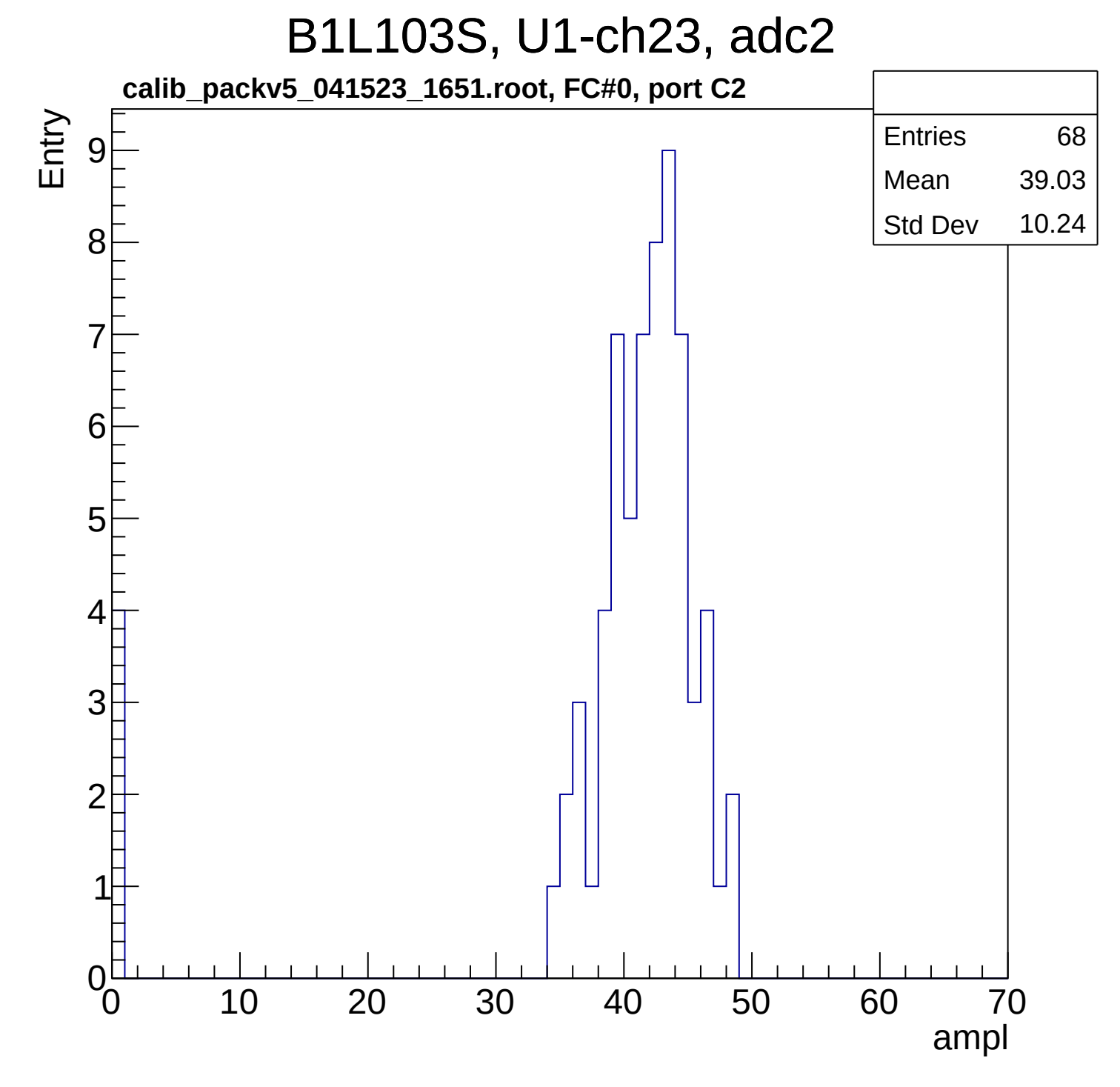
40
50
60
70


B1L103S, U1-ch23, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 39.03
Std Dev 10.24
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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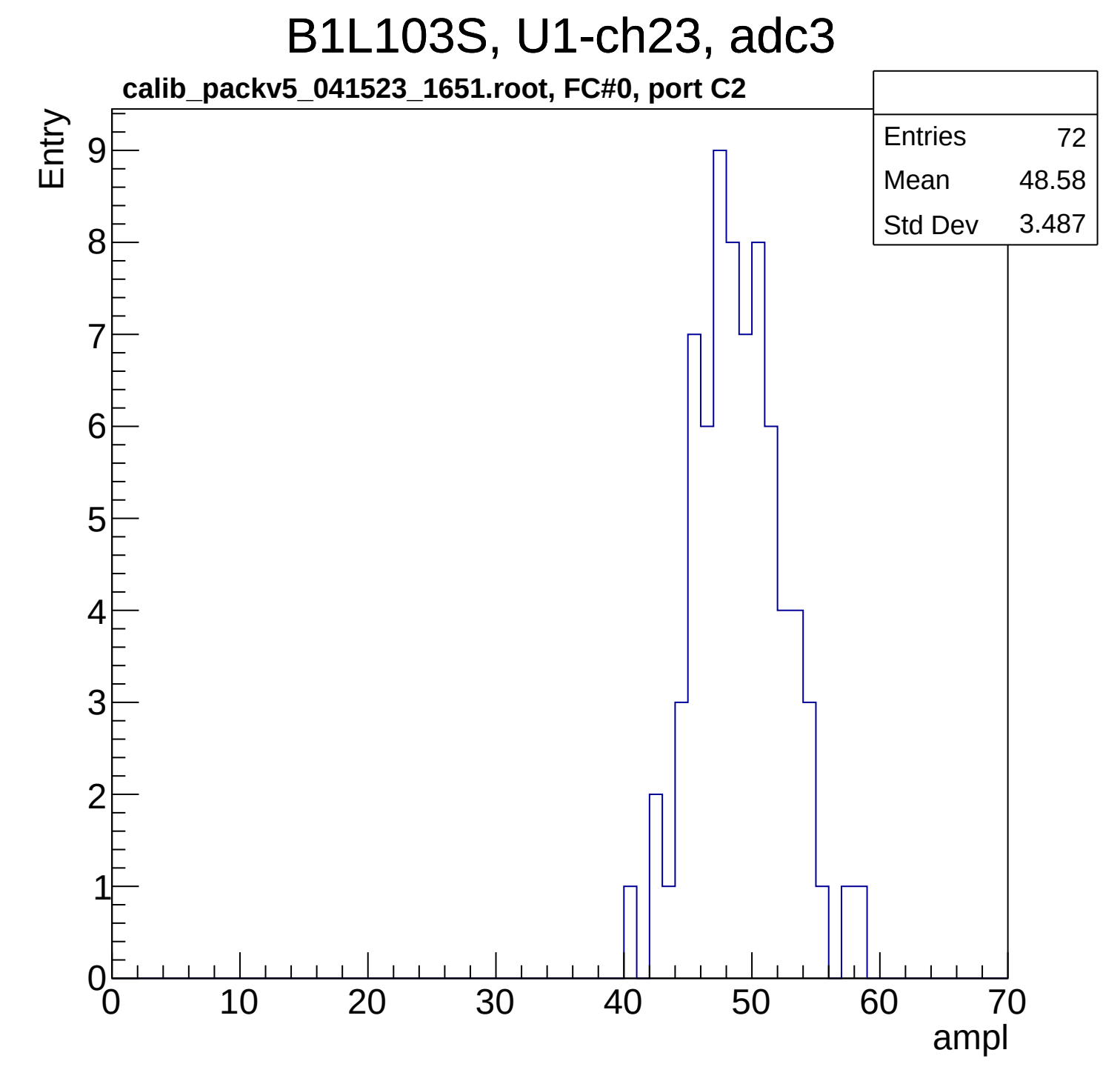
60
70


B1L103S, U1-ch23, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 48.58
Std Dev 3.487
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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40
50
60
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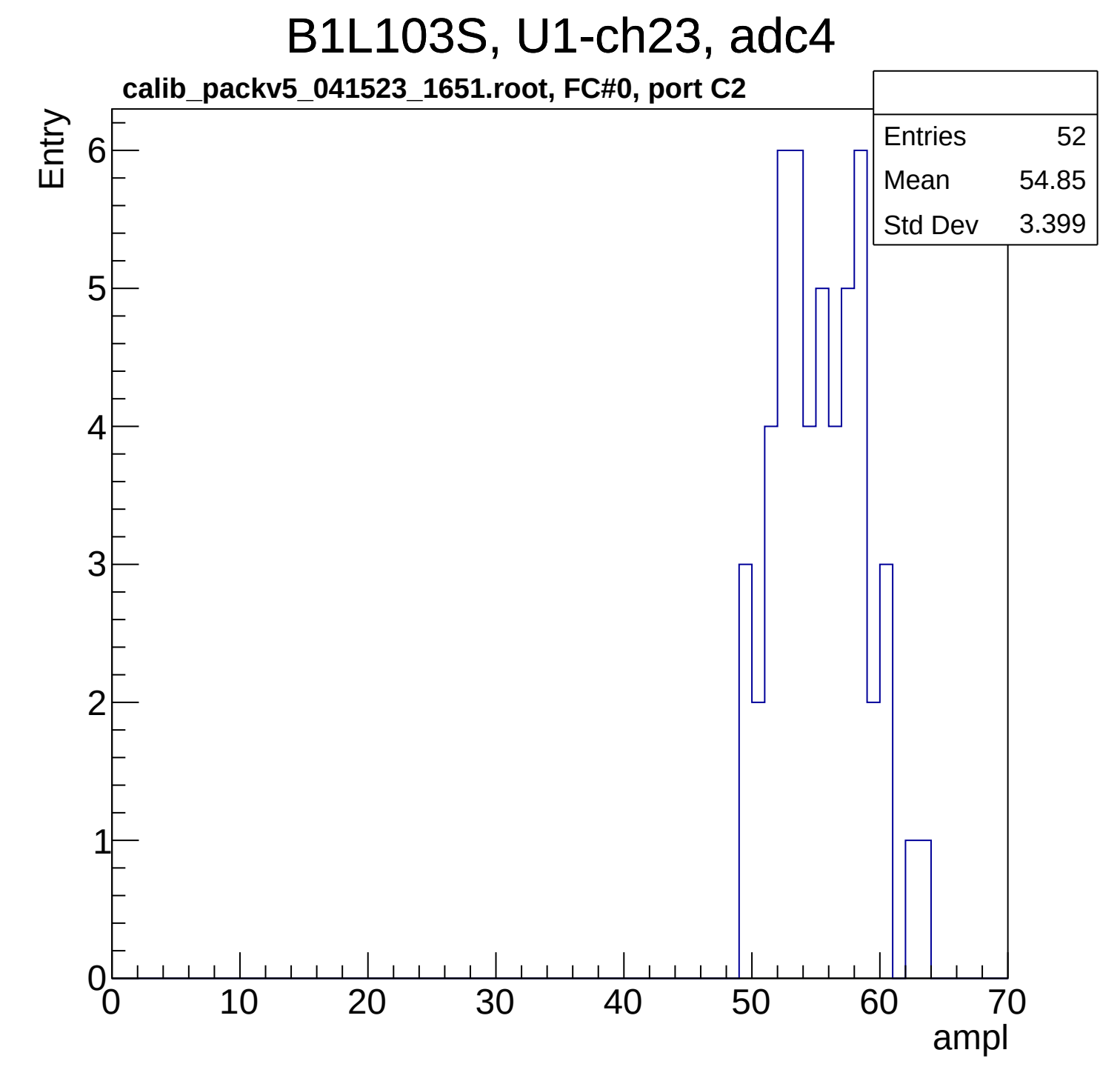
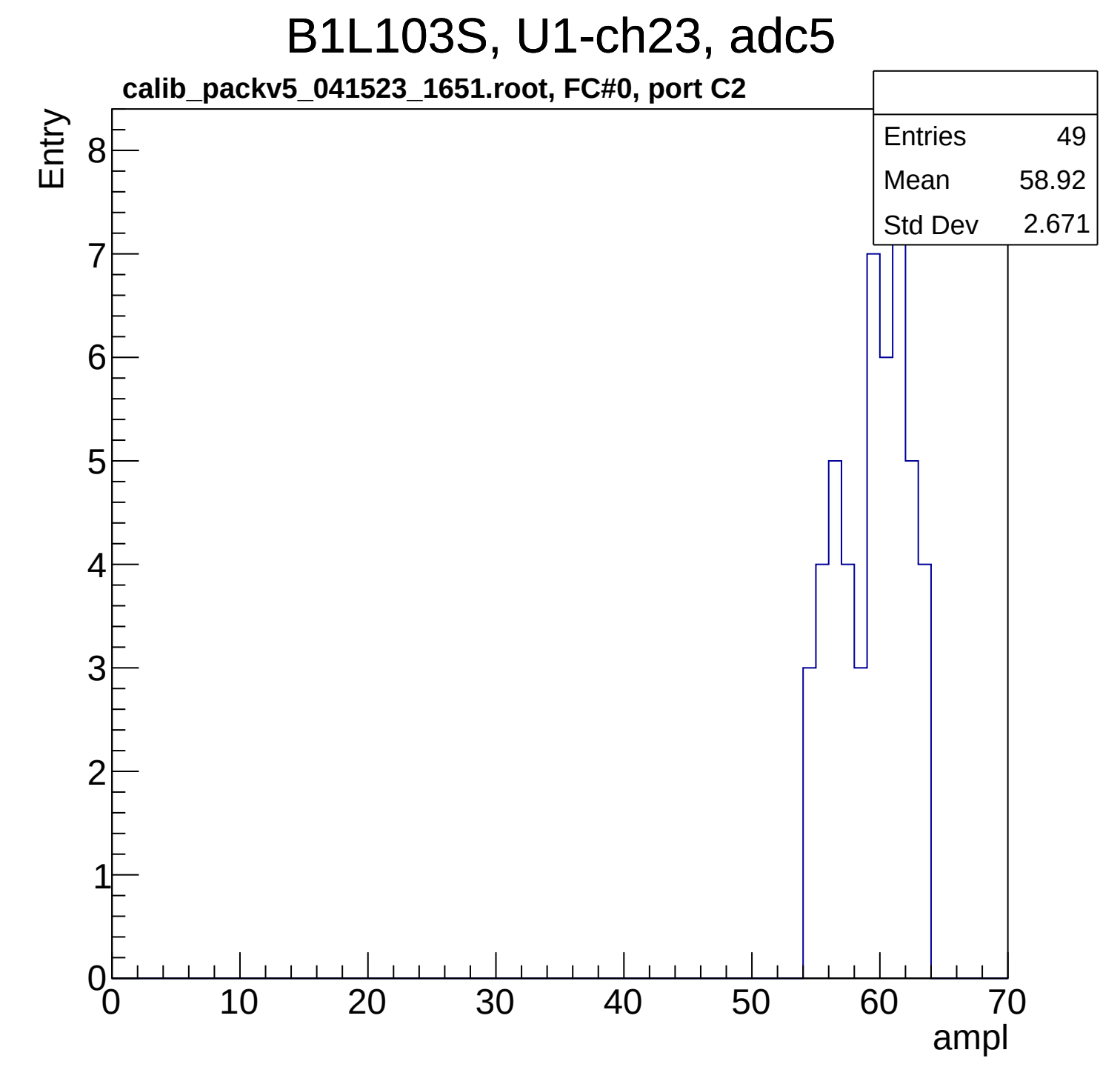

B1L103S, U1-ch23, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 54.85
Std Dev 3.399
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U1-ch23, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 58.92
Std Dev 2.671
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
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30
40
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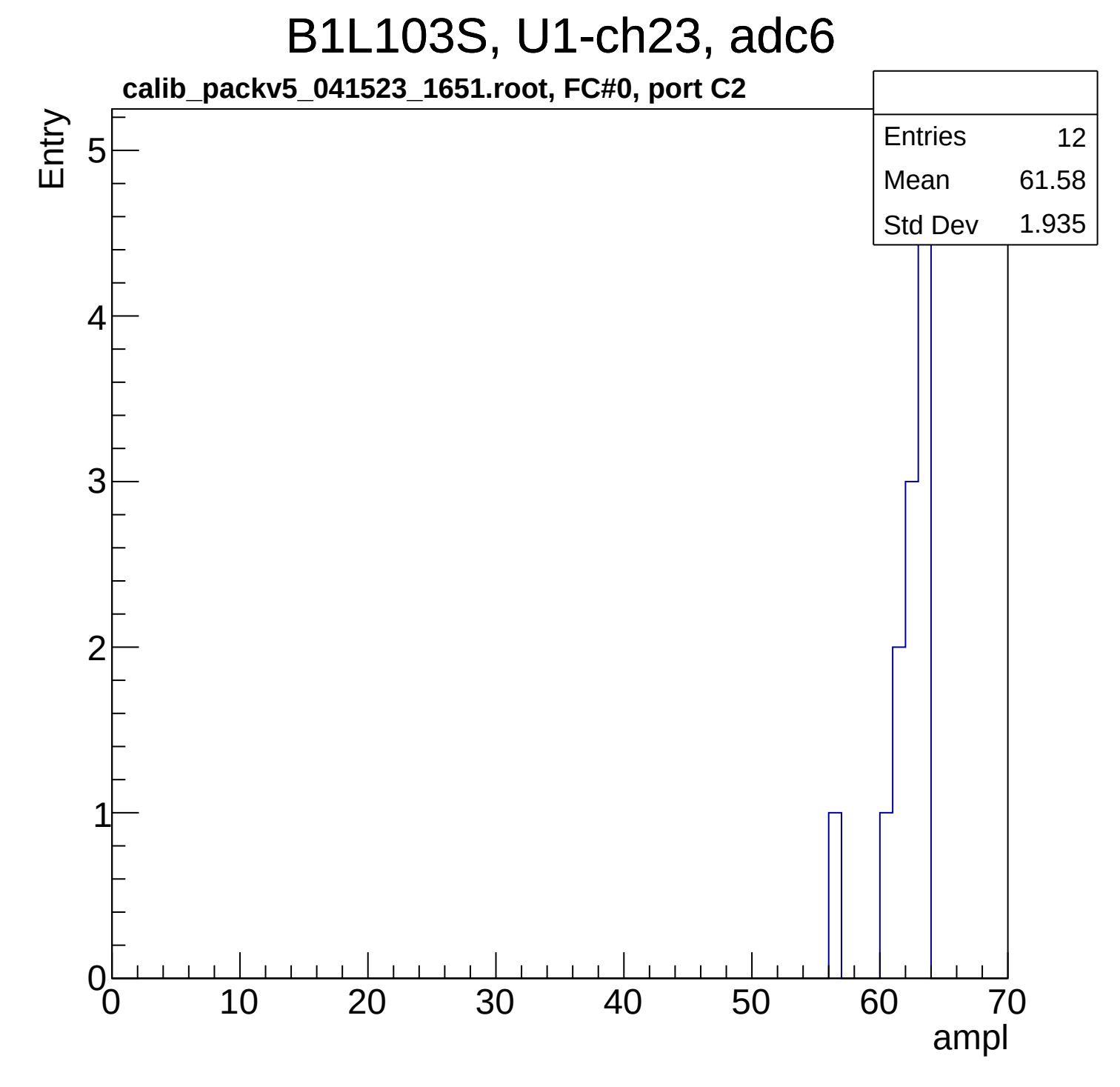
60
70


B1L103S, U1-ch23, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 61.58
Std Dev 1.935
Entry
ampl
0
1
2
3
4
5
0
10
20
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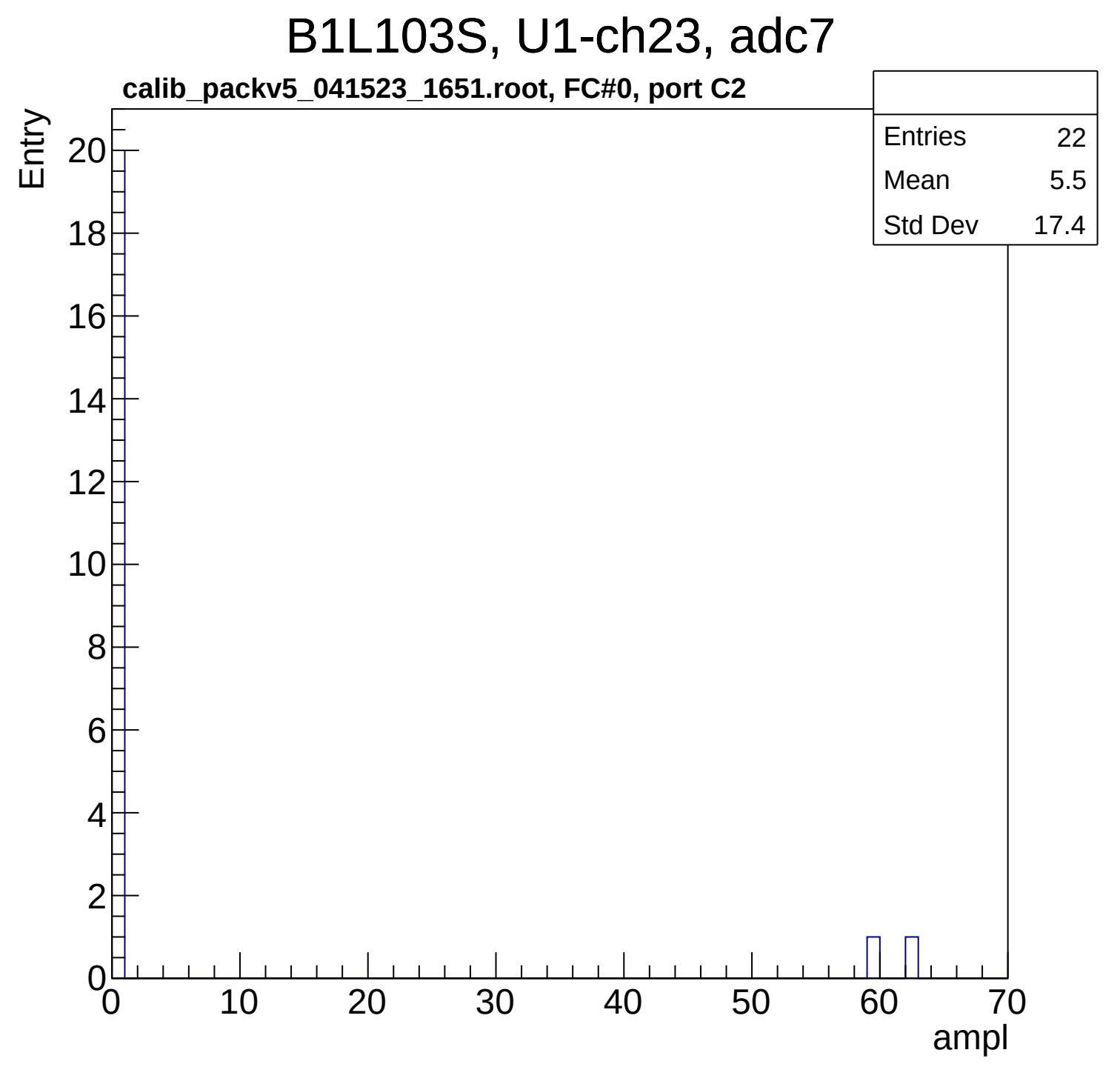
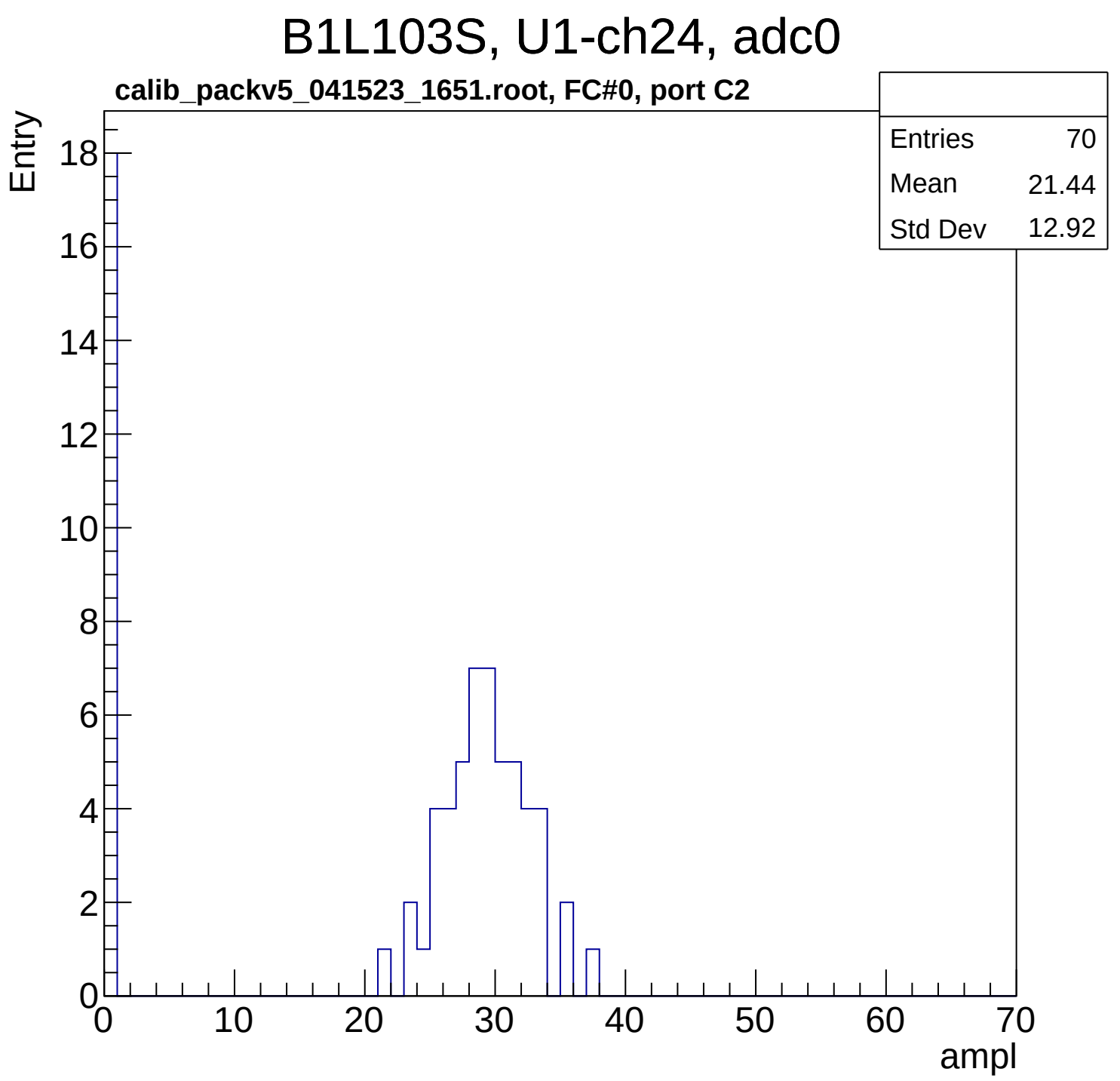
60
70


B1L103S, U1-ch23, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 5.5
Std Dev 17.4
Entry
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch24, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 21.44
Std Dev 12.92
Entry
0
2
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6
8
10
12
14
16
18
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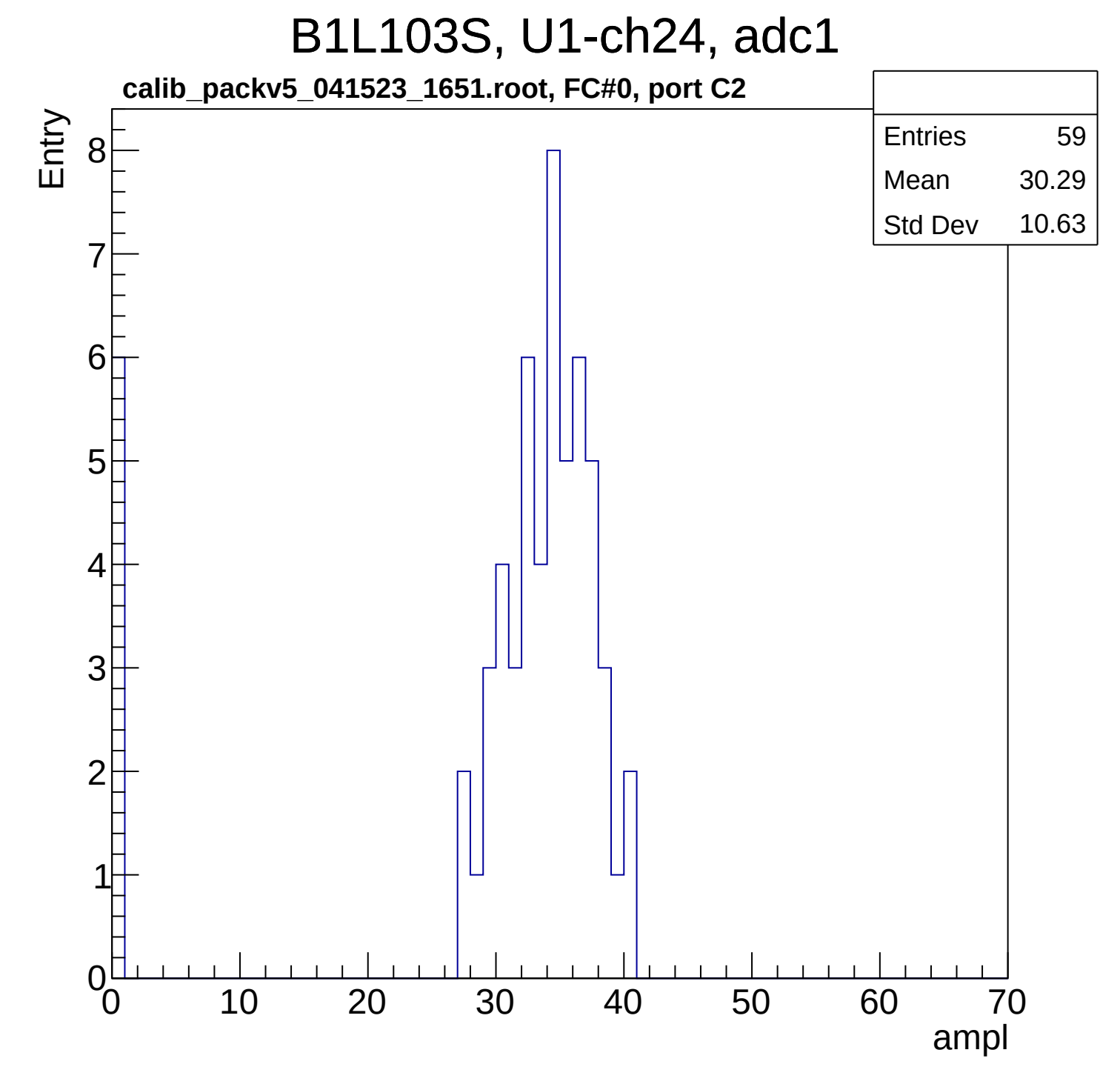
ampl


B1L103S, U1-ch24, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 30.29
Std Dev 10.63
Entry
ampl
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2
3
4
5
6
7
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0
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20
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40
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60
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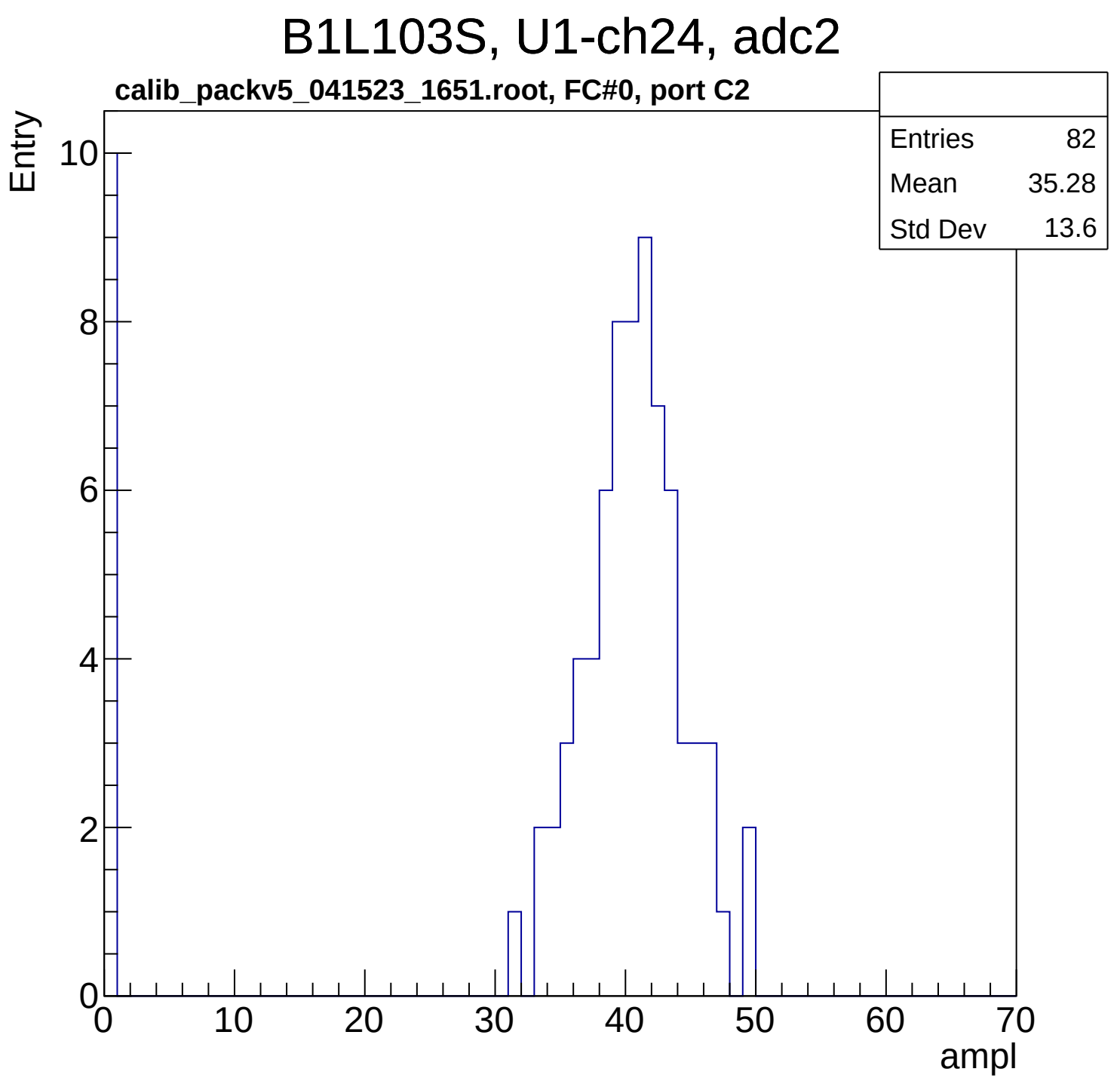
B1L103S, U1-ch24, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 35.28
Std Dev 13.6
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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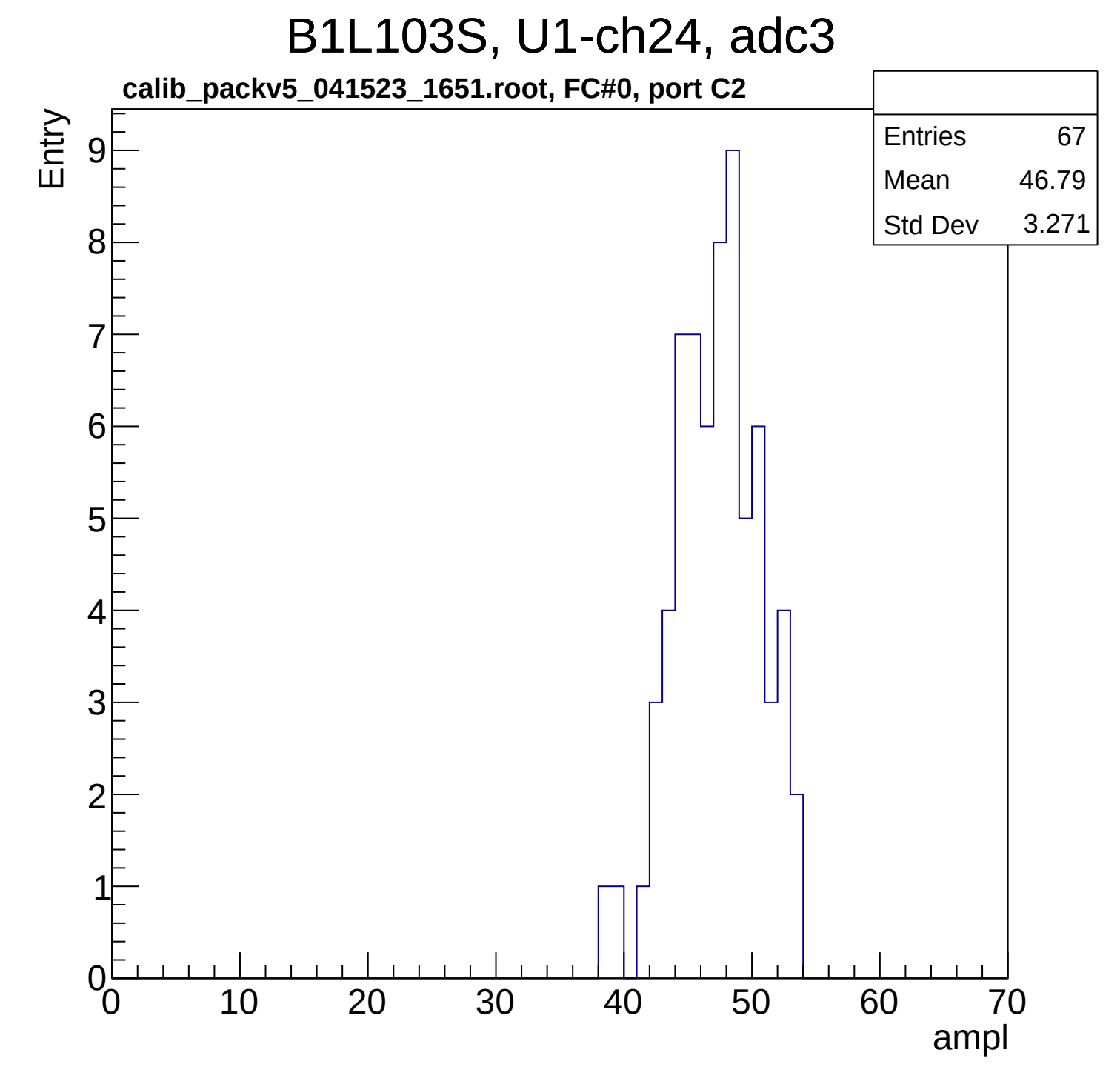
B1L103S, U1-ch24, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 46.79
Std Dev 3.271
Entry
ampl
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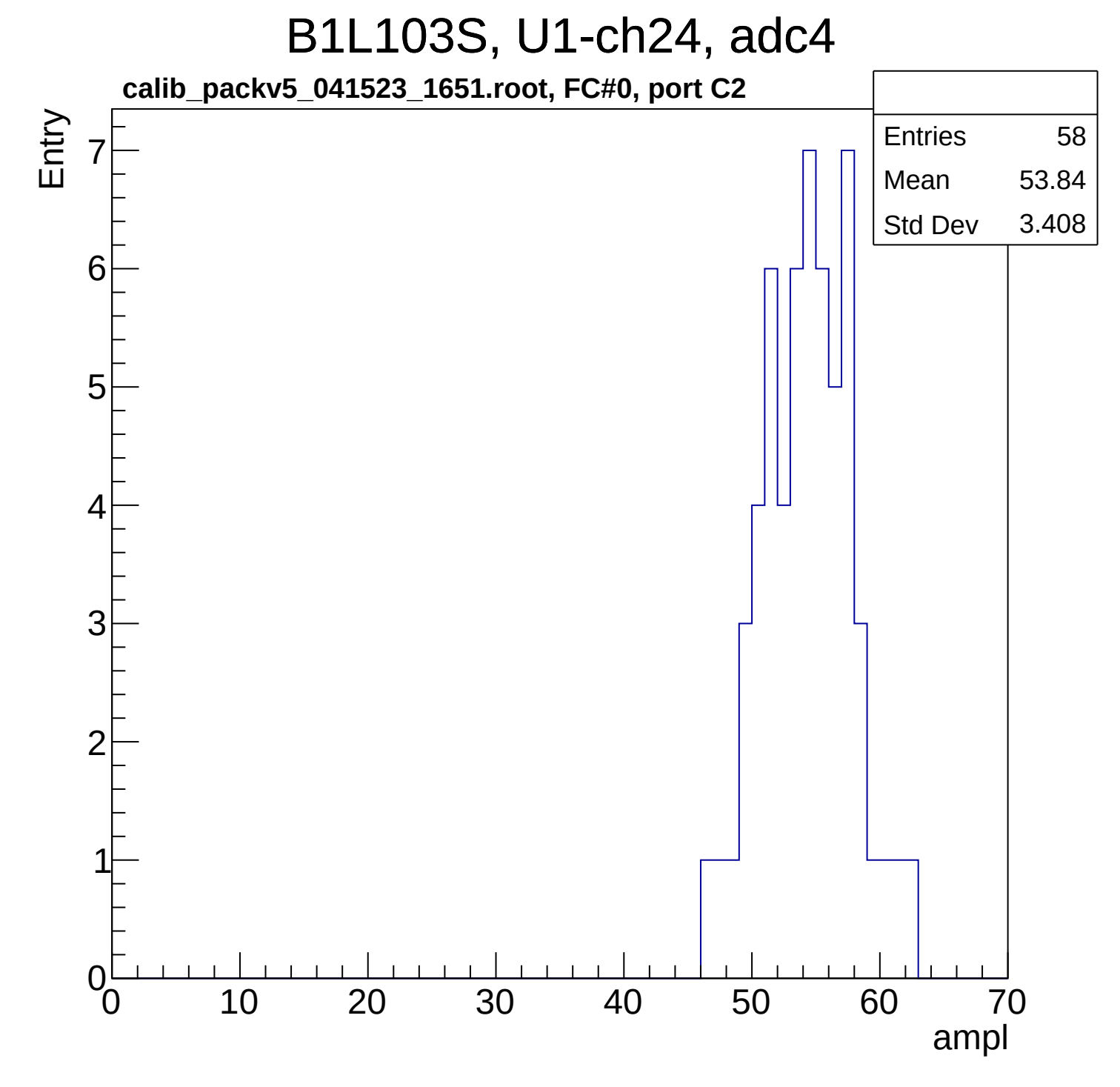
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U1-ch24, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 53.84
Std Dev 3.408
Entry
ampl
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1
2
3
4
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6
7
0
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20
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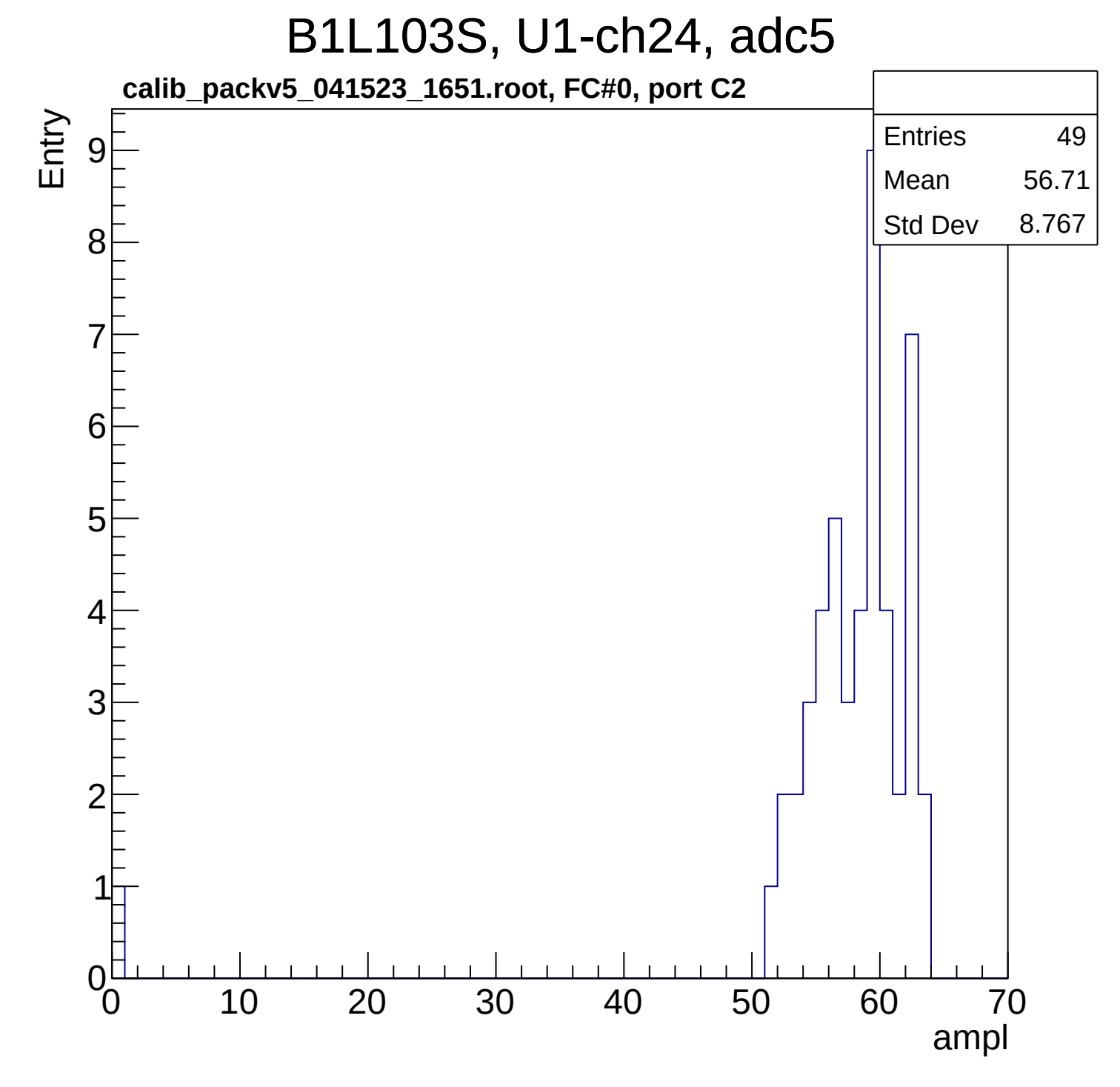
40
50
60
70


B1L103S, U1-ch24, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 56.71
Std Dev 8.767
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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40
50
60
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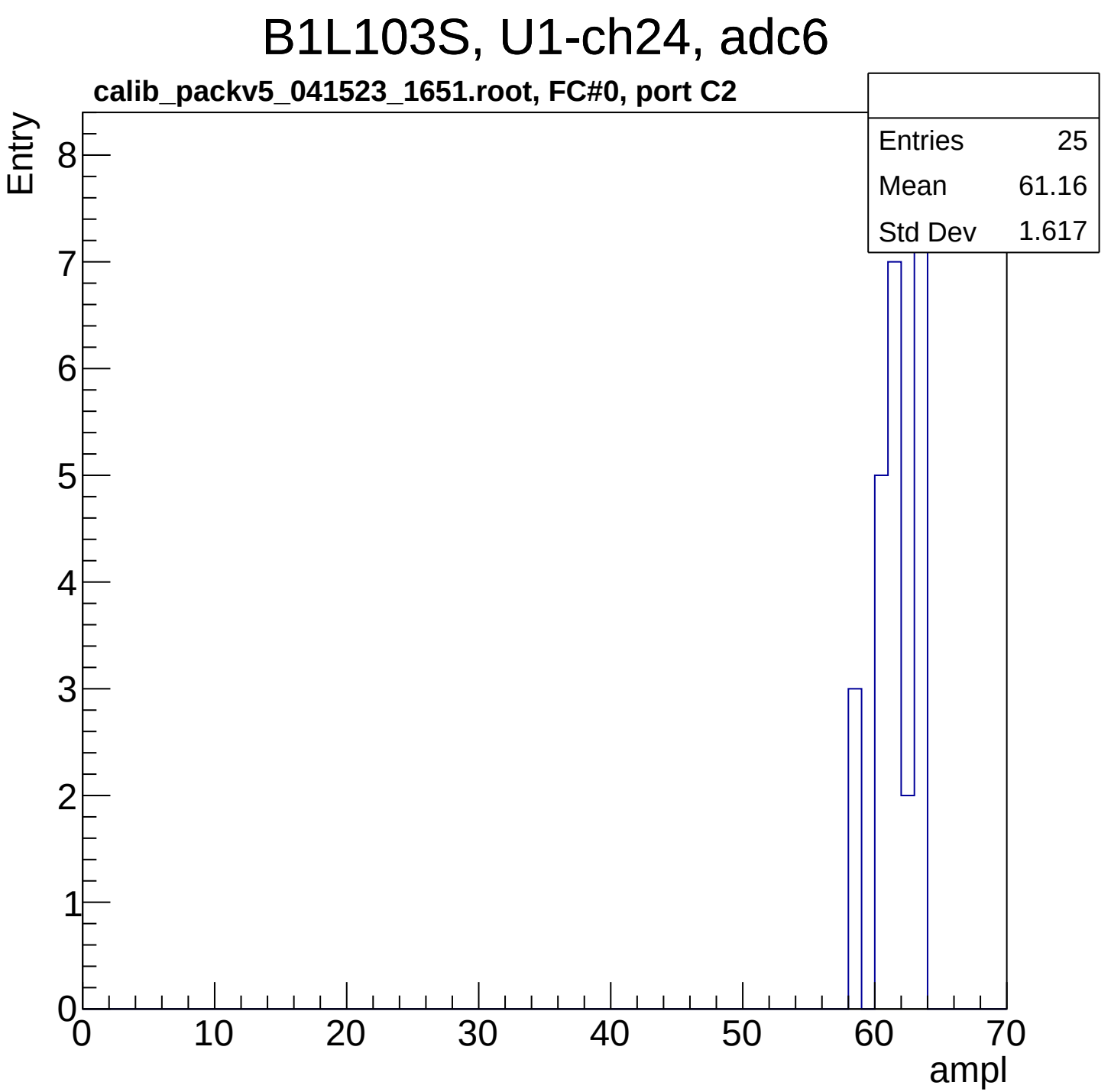
B1L103S, U1-ch24, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 25
Mean 61.16
Std Dev 1.617
Entry
ampl
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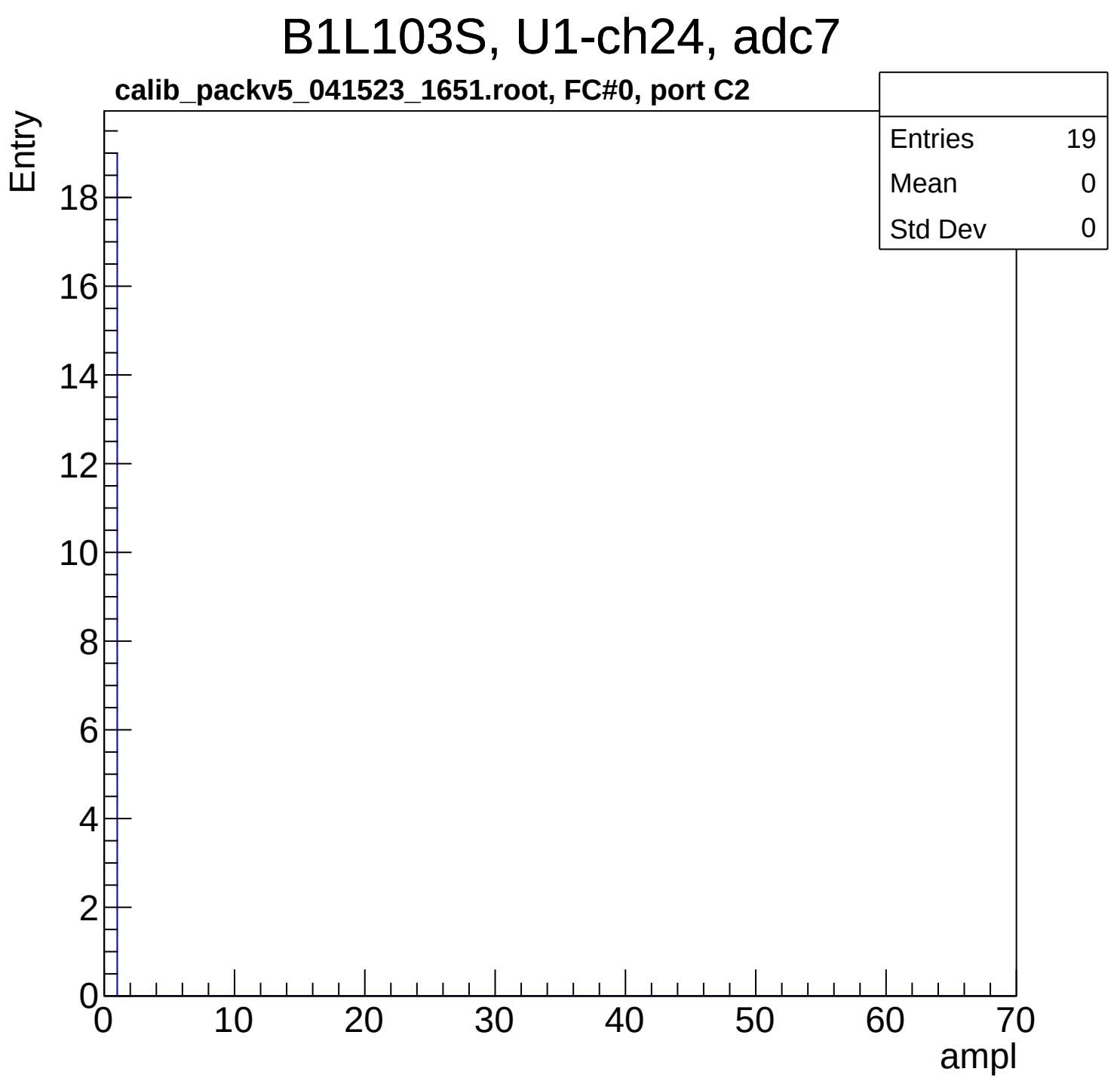
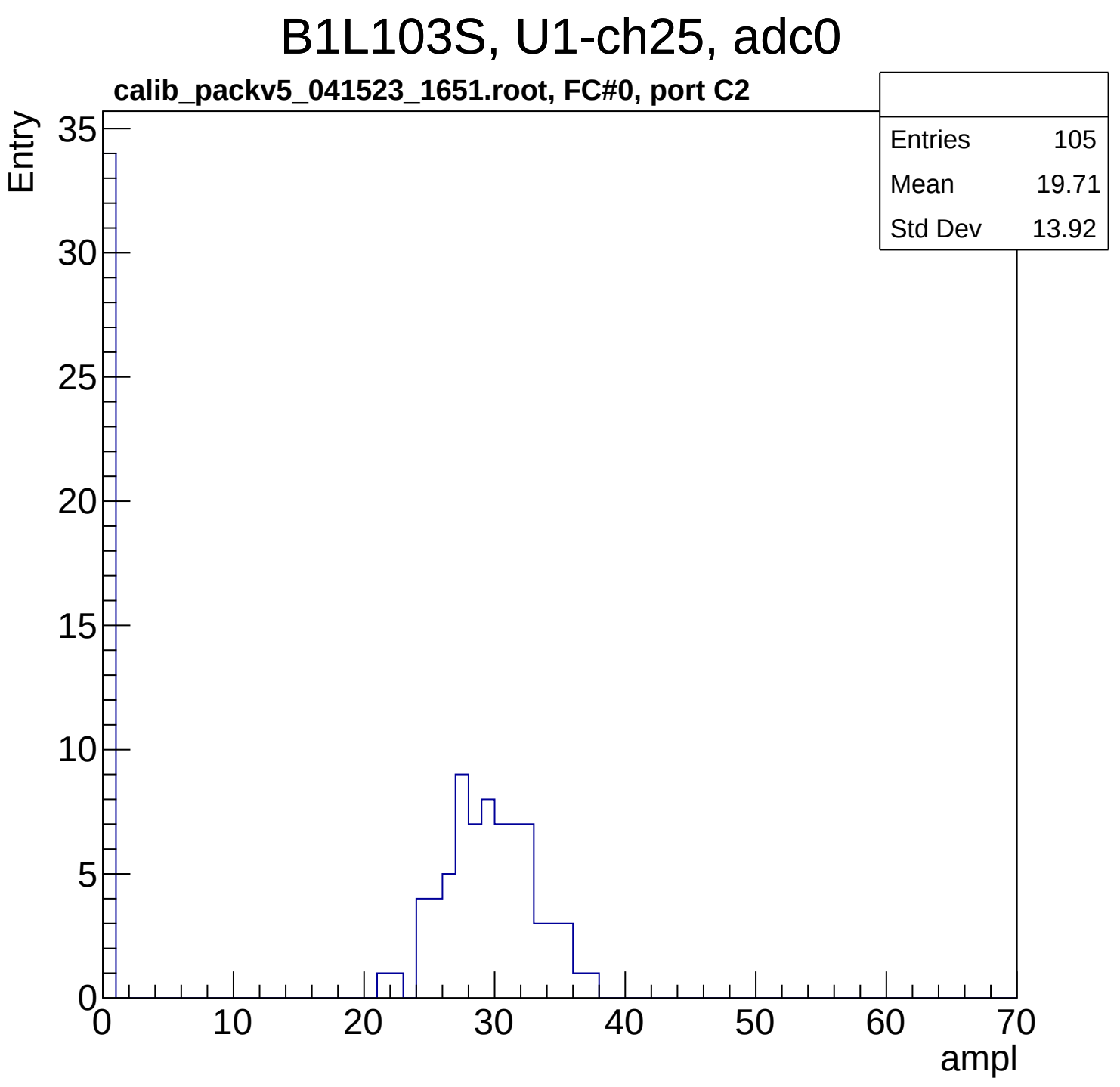
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U1-ch24, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch25, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 105
Mean 19.71
Std Dev 13.92
Entry
ampl
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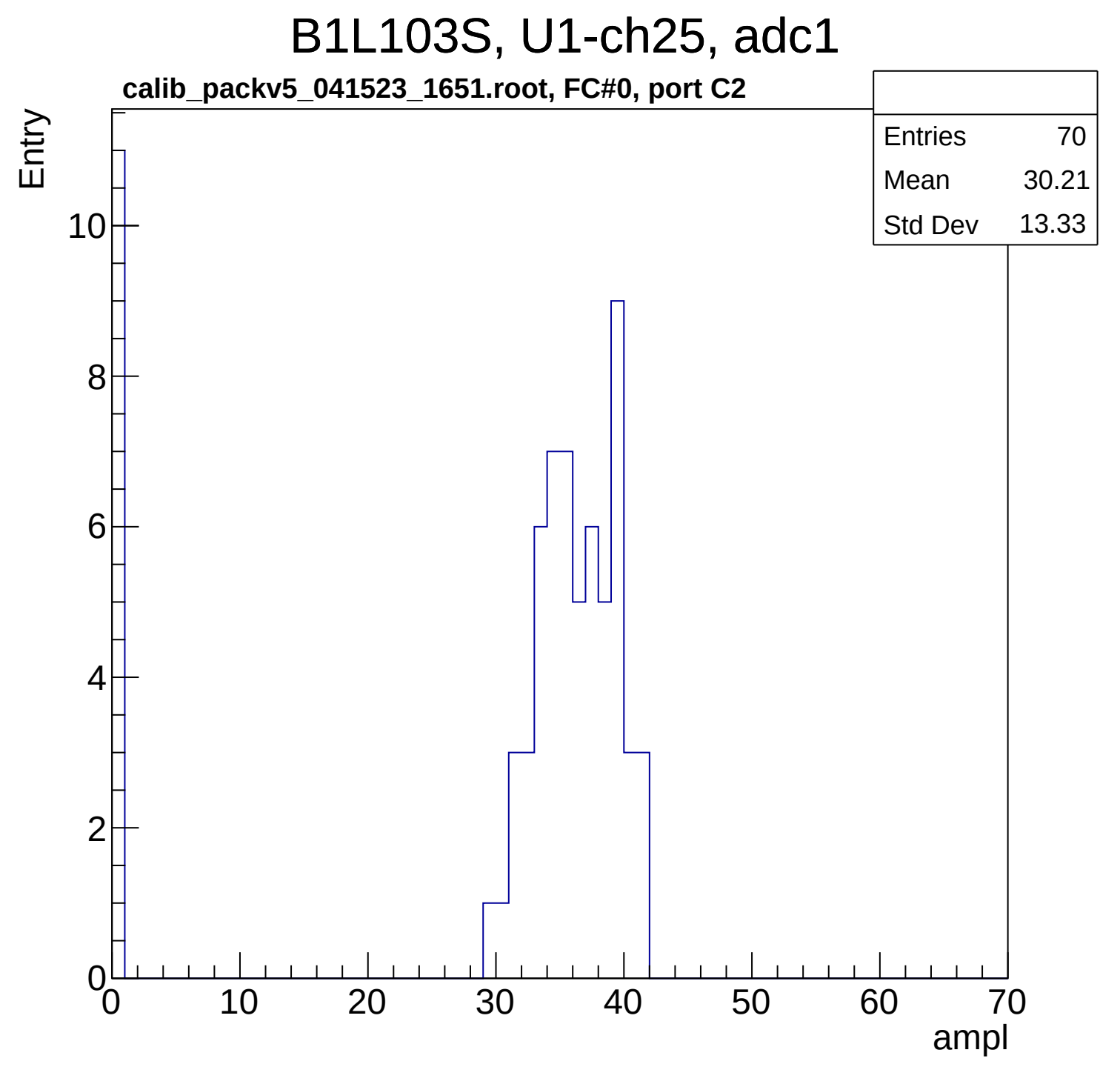
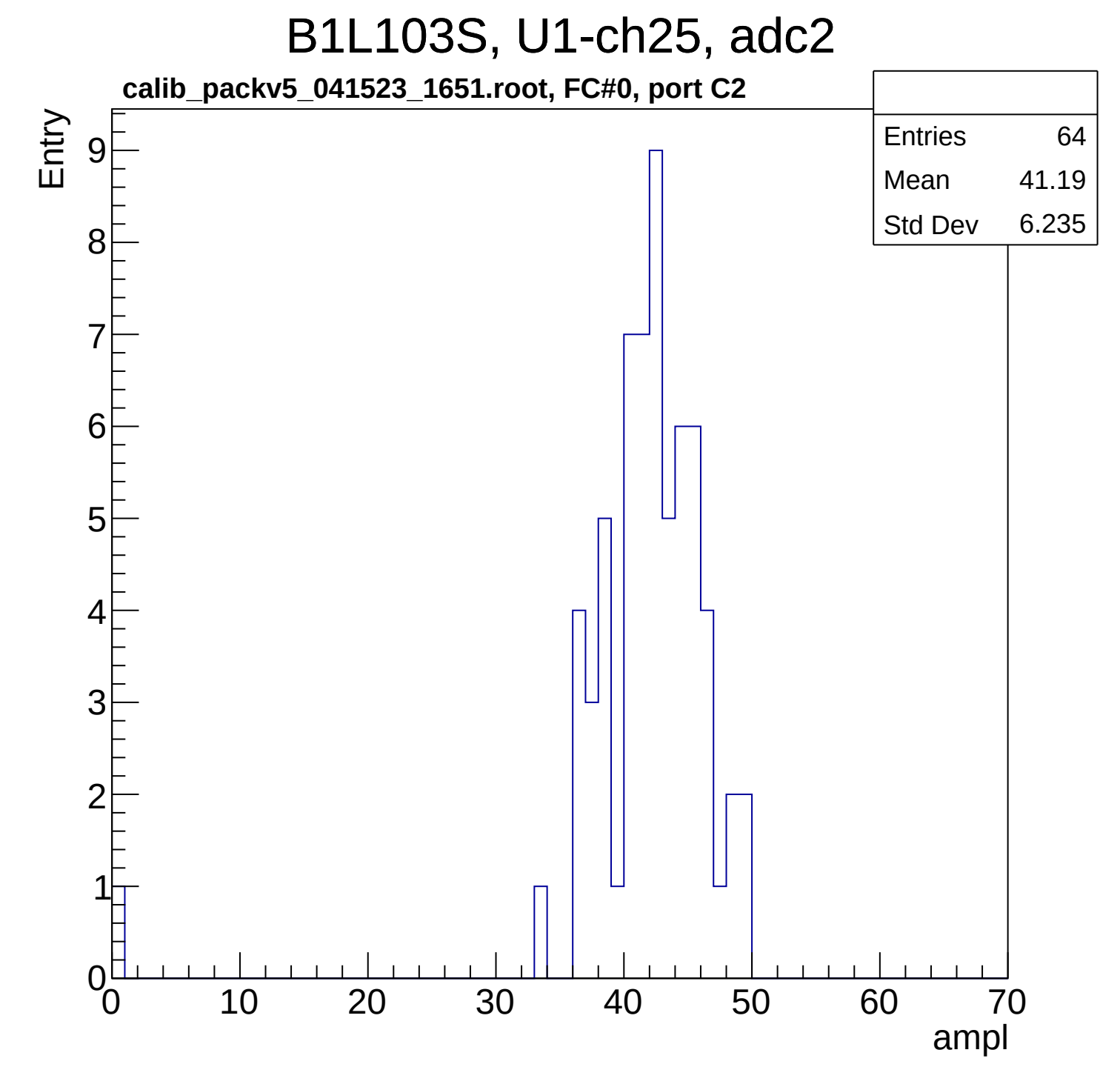
5
10
15
20
25
30
35
0
10
20
30
40
50
60
70


B1L103S, U1-ch25, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 30.21
Std Dev 13.33
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch25, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 41.19
Std Dev 6.235
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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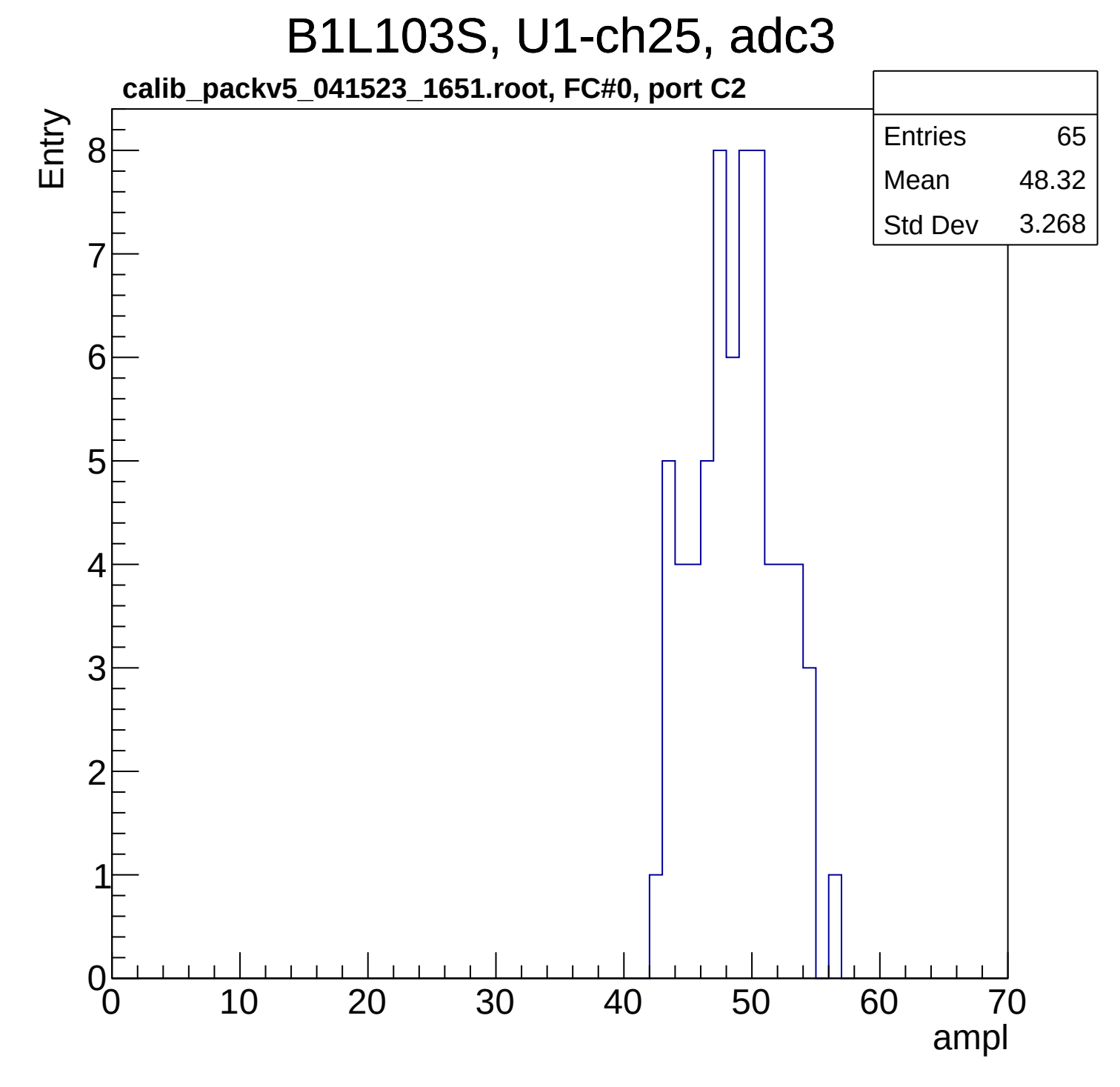
40
50
60
70


B1L103S, U1-ch25, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 48.32
Std Dev 3.268
Entry
ampl
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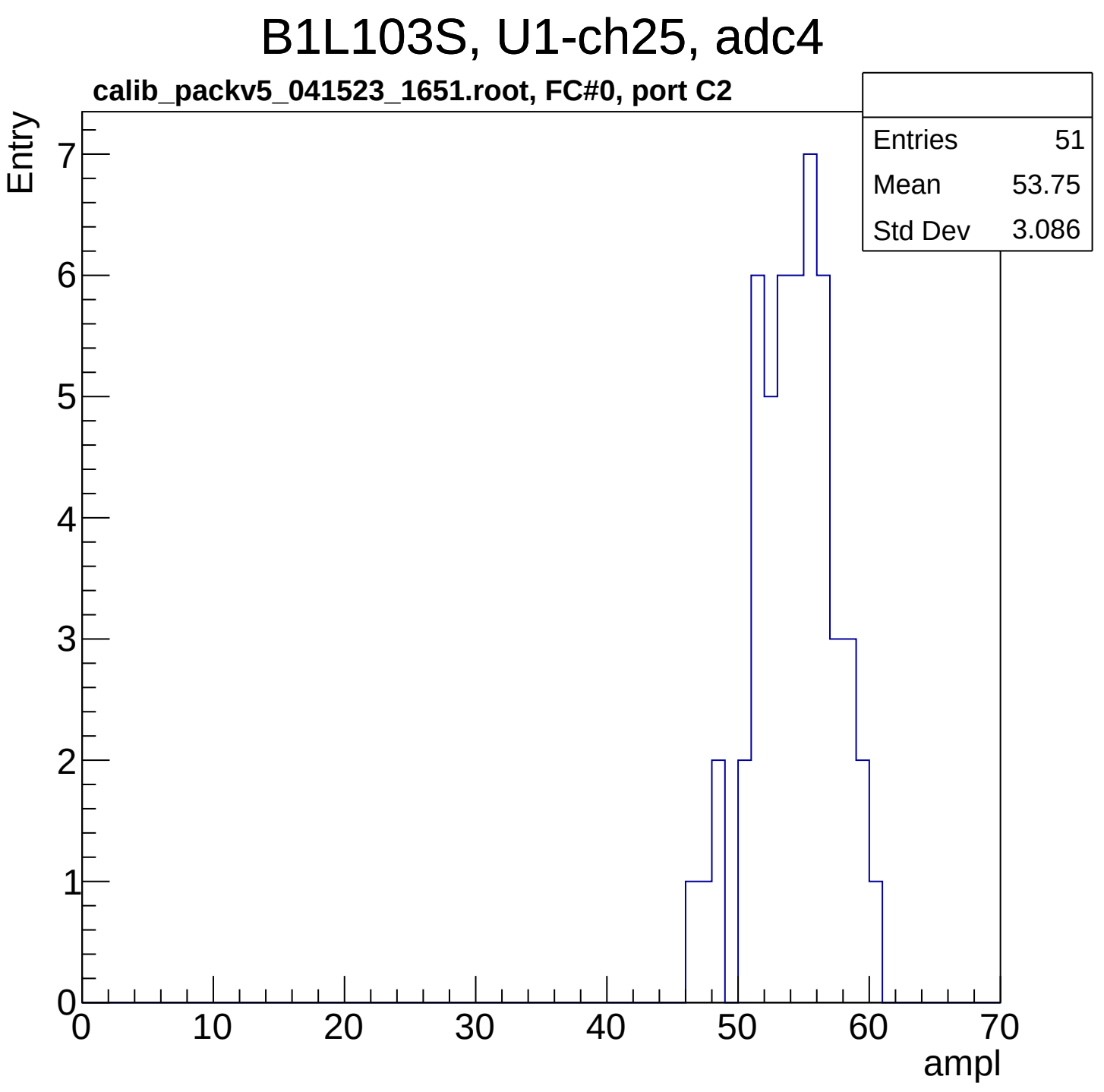
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U1-ch25, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 53.75
Std Dev 3.086
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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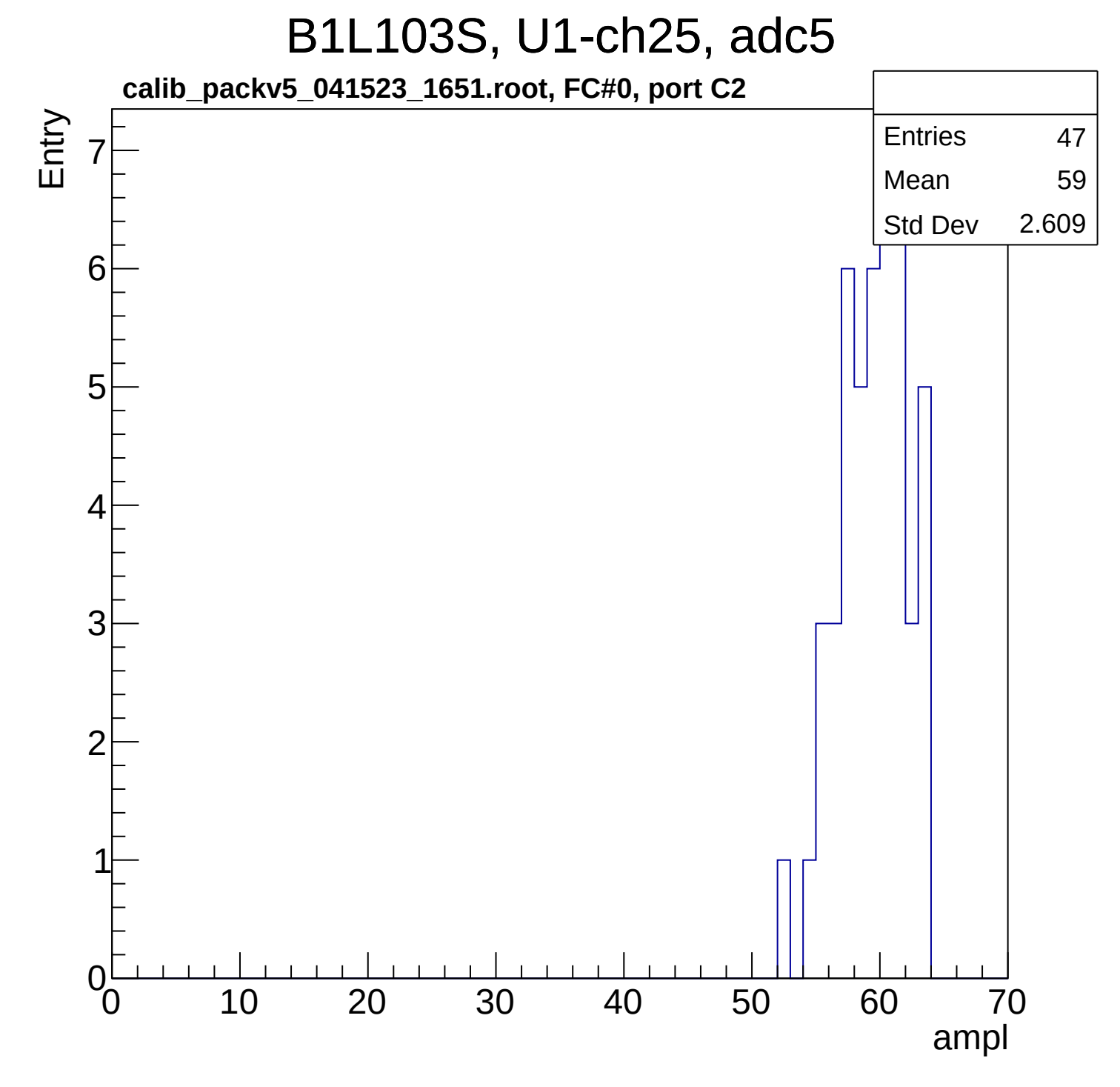
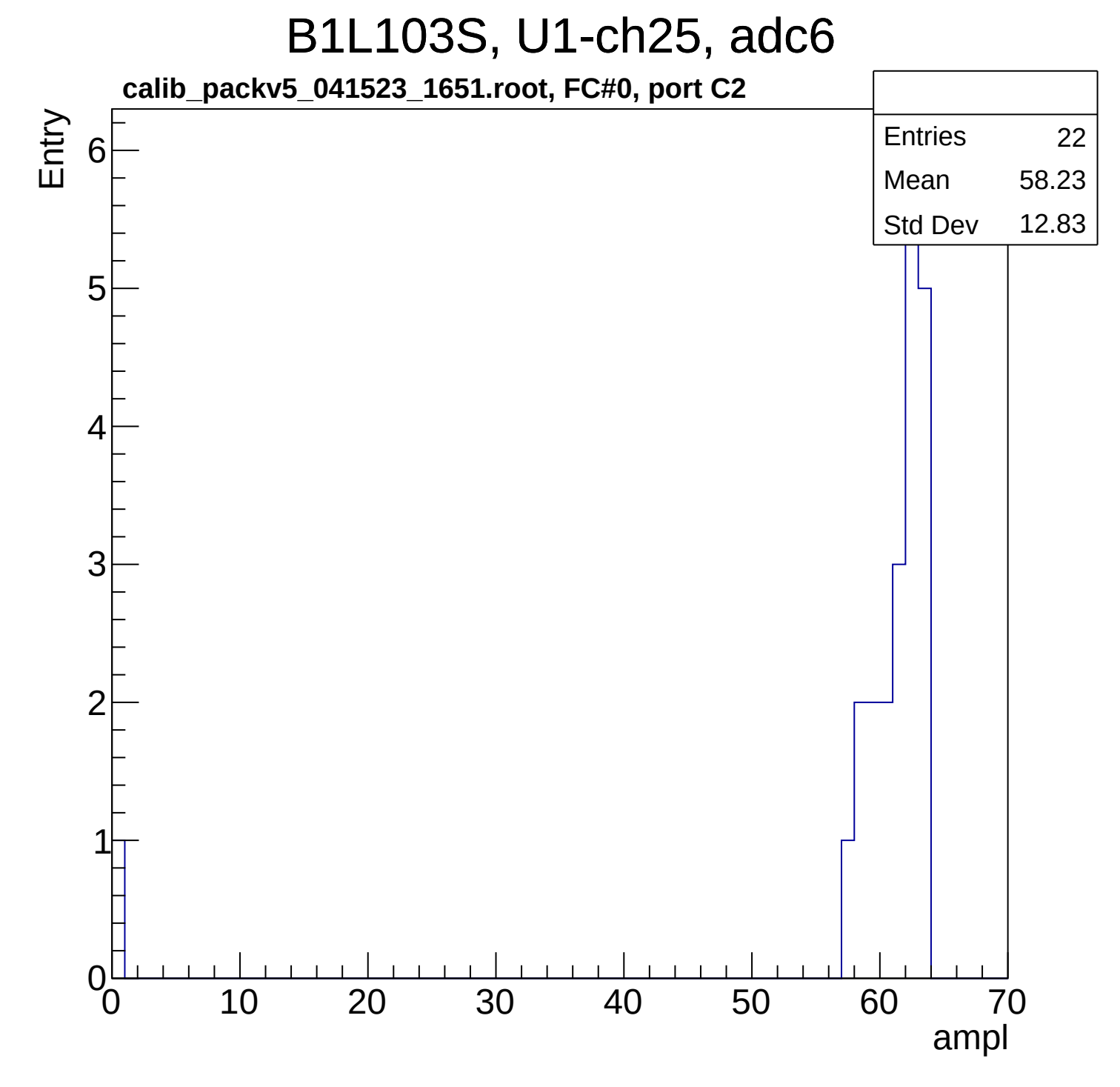
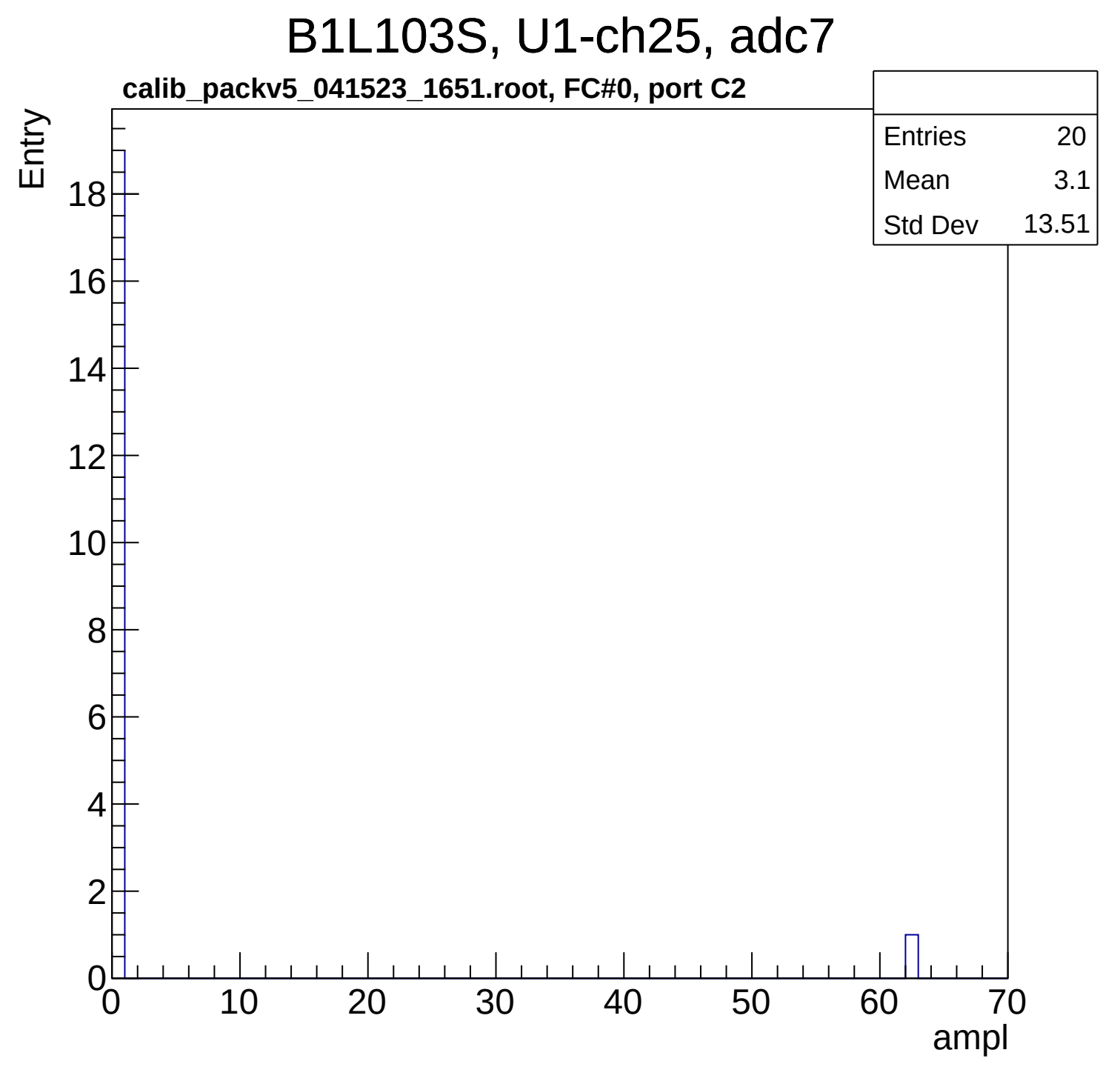

B1L103S, U1-ch25, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 59
Std Dev 2.609
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U1-ch25, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 58.23
Std Dev 12.83
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch25, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.1
Std Dev 13.51
Entry
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6
8
10
12
14
16
18
0
10
20
30
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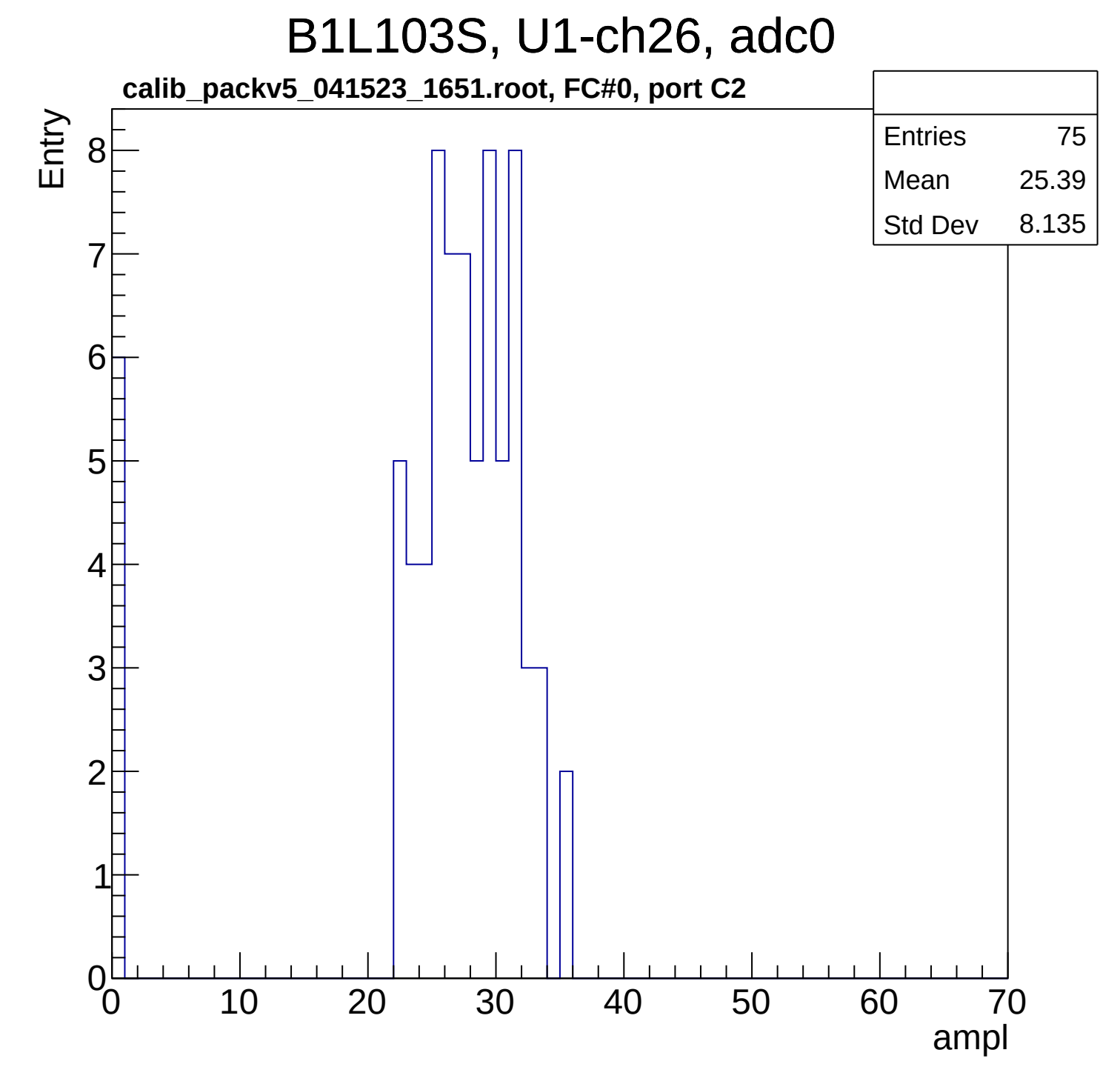
50
60
70
ampl


B1L103S, U1-ch26, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 25.39
Std Dev 8.135
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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60
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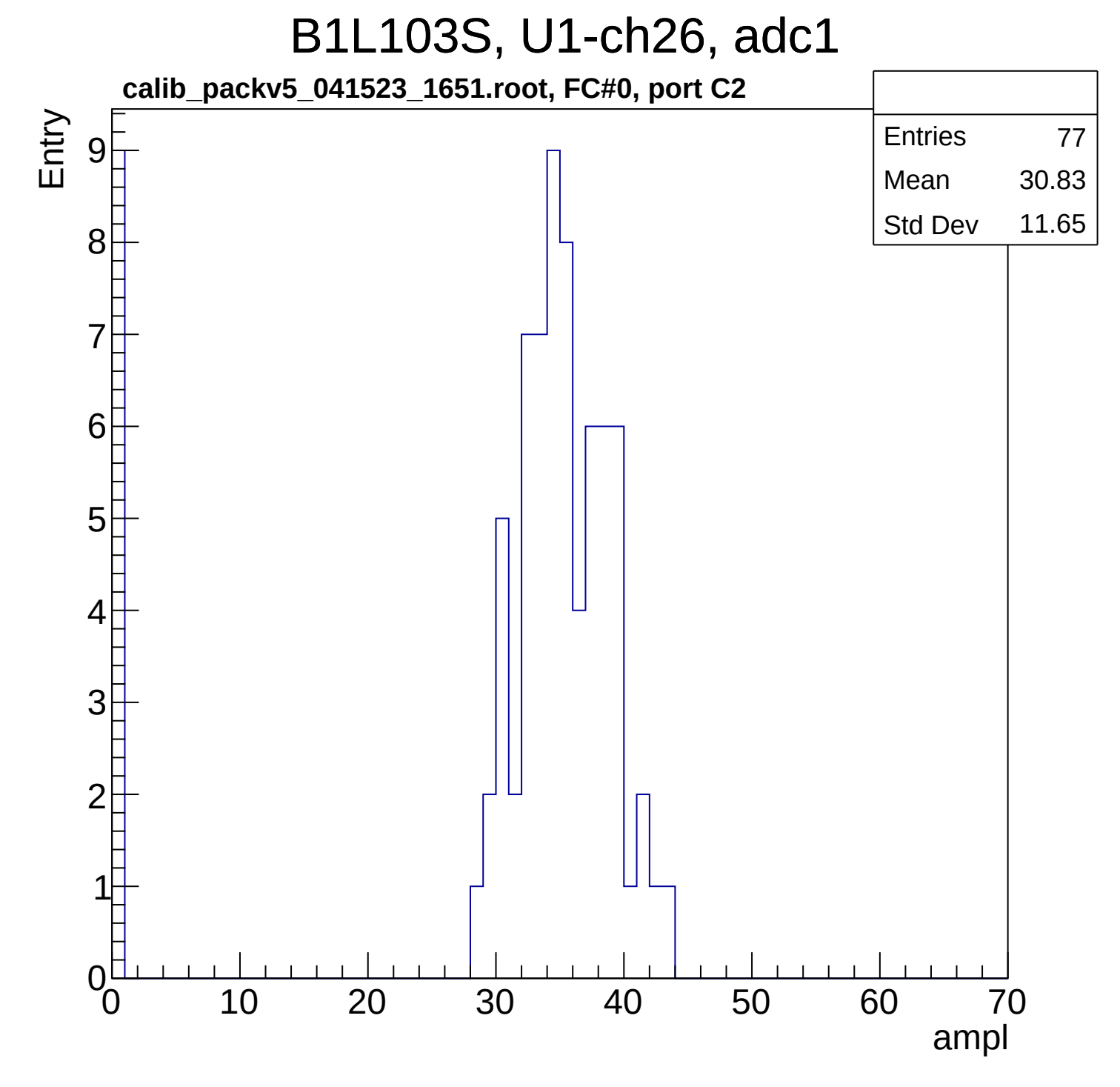
B1L103S, U1-ch26, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 30.83
Std Dev 11.65
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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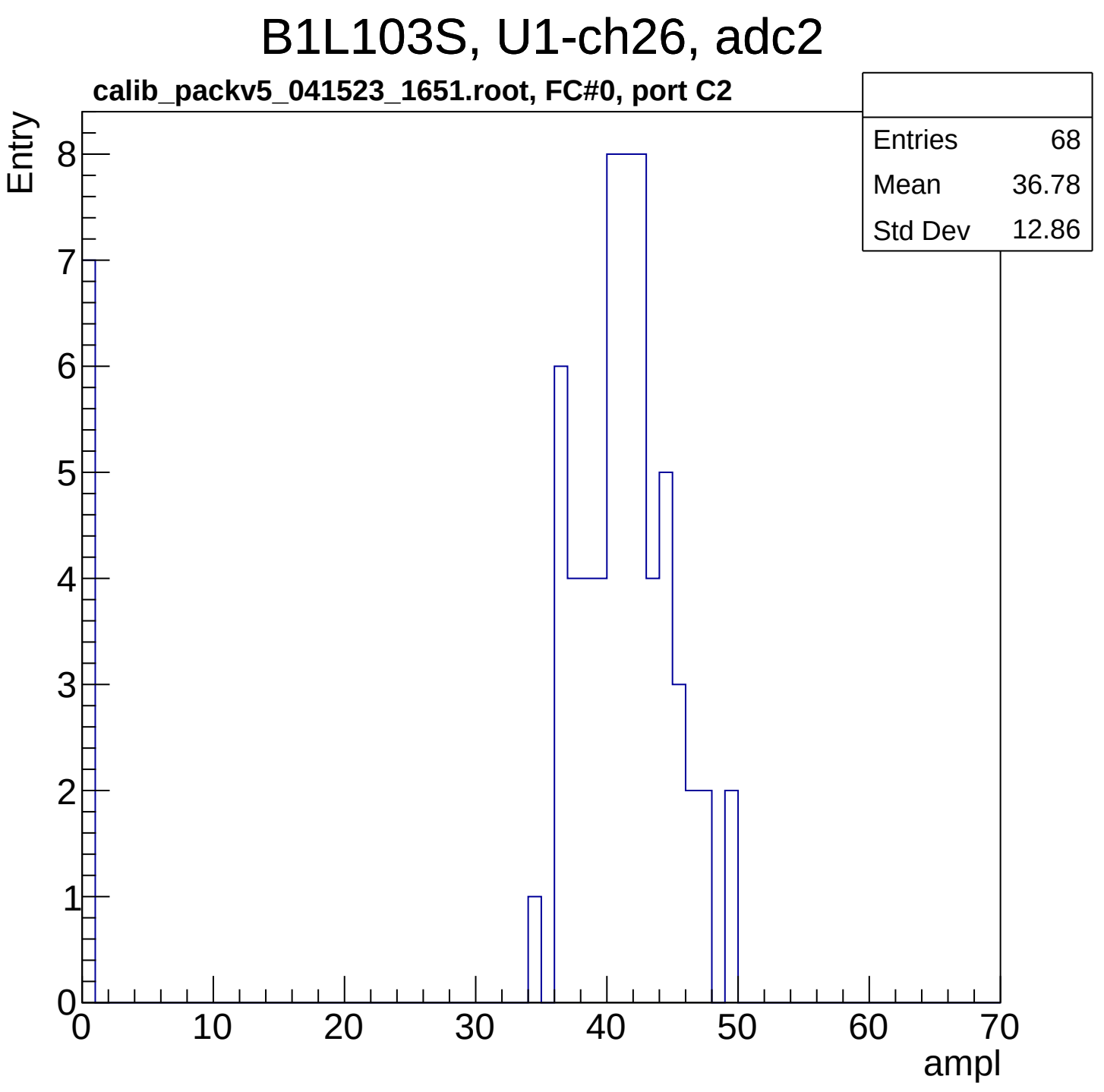
40
50
60
70


B1L103S, U1-ch26, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 36.78
Std Dev 12.86
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
30
40
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60
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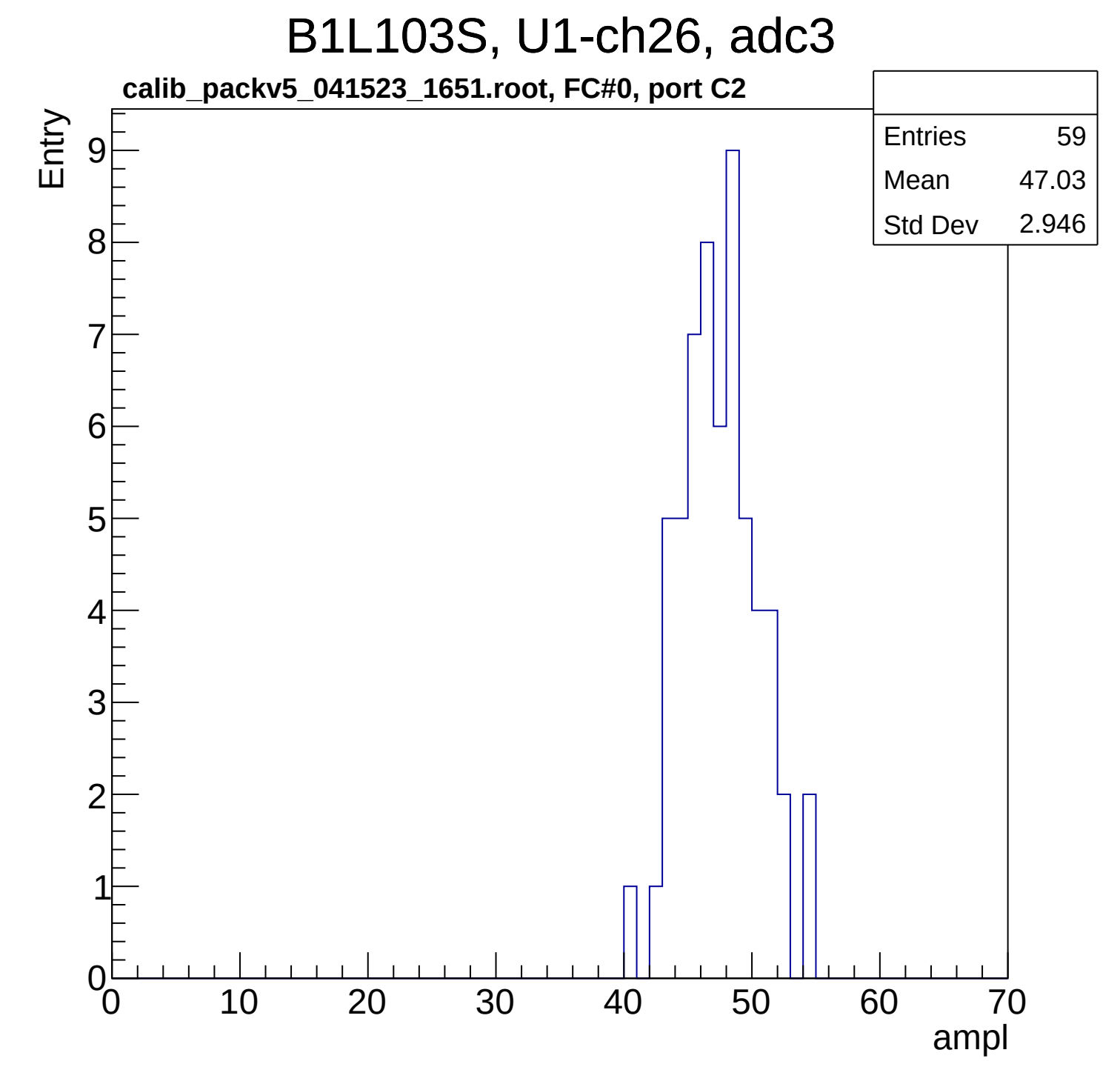
B1L103S, U1-ch26, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 47.03
Std Dev 2.946
Entry
ampl
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2
3
4
5
6
7
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0
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60
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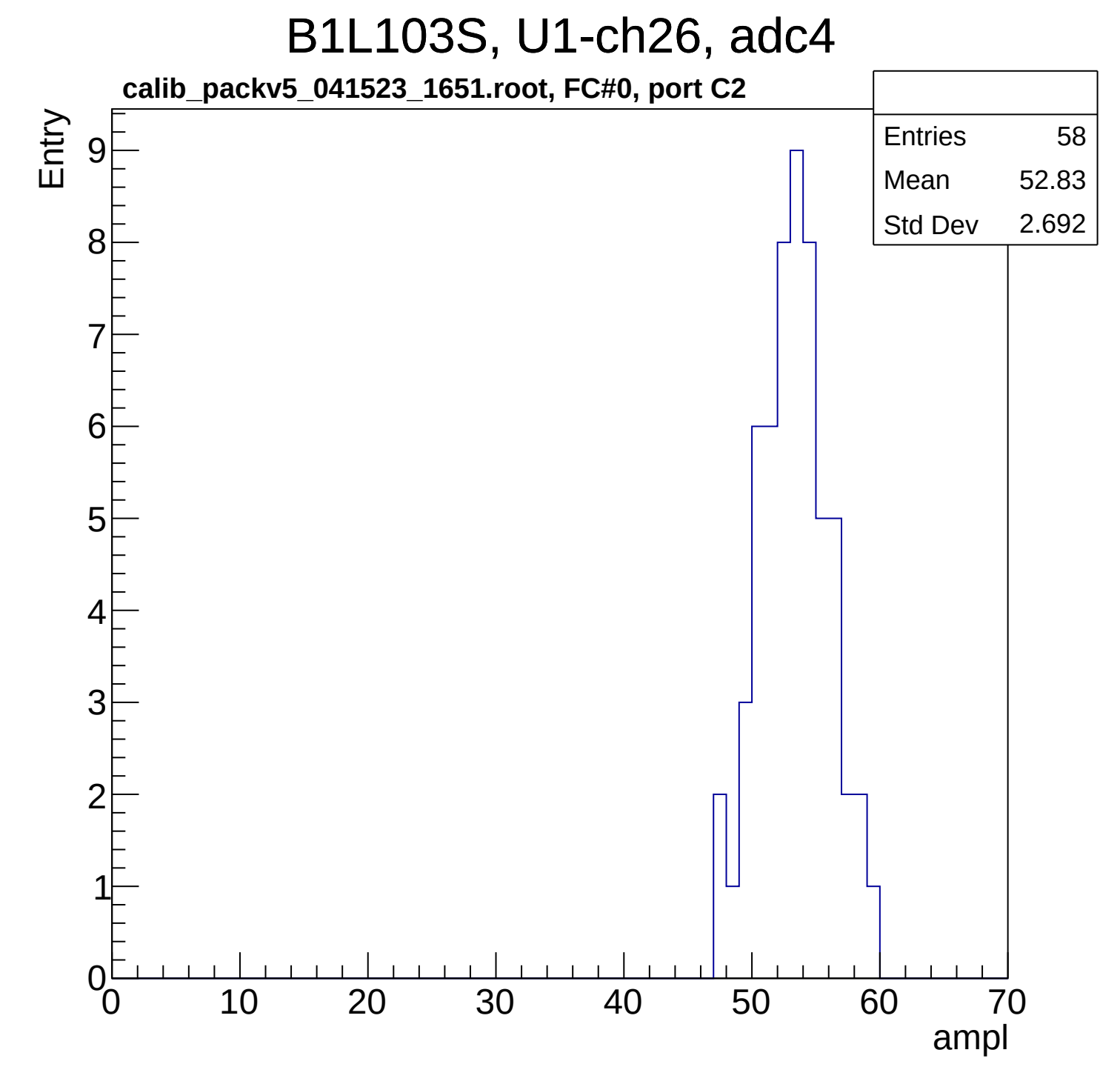
B1L103S, U1-ch26, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 52.83
Std Dev 2.692
Entry
ampl
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2
3
4
5
6
7
8
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0
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60
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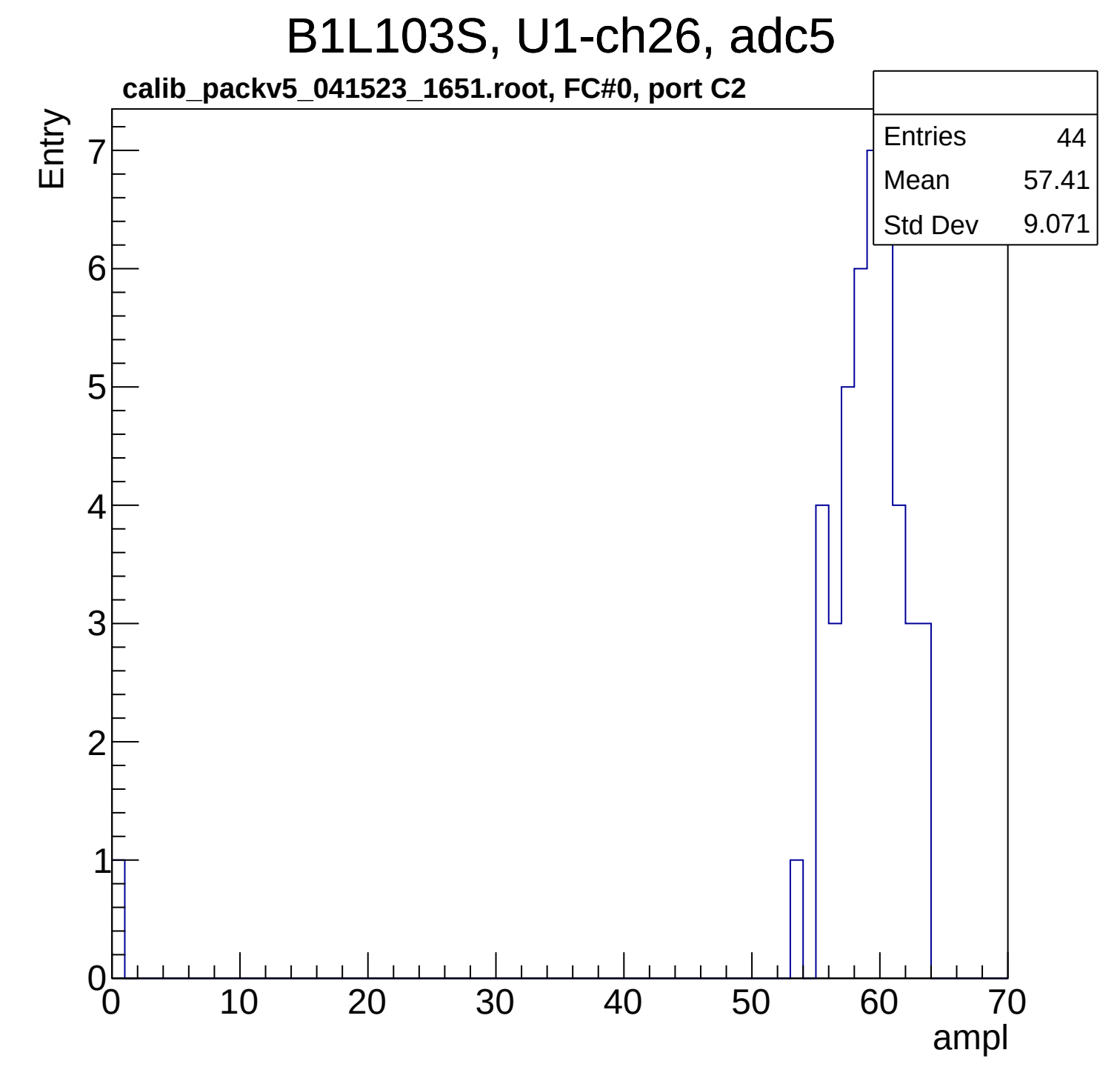
B1L103S, U1-ch26, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 57.41
Std Dev 9.071
Entry
ampl
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4
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6
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0
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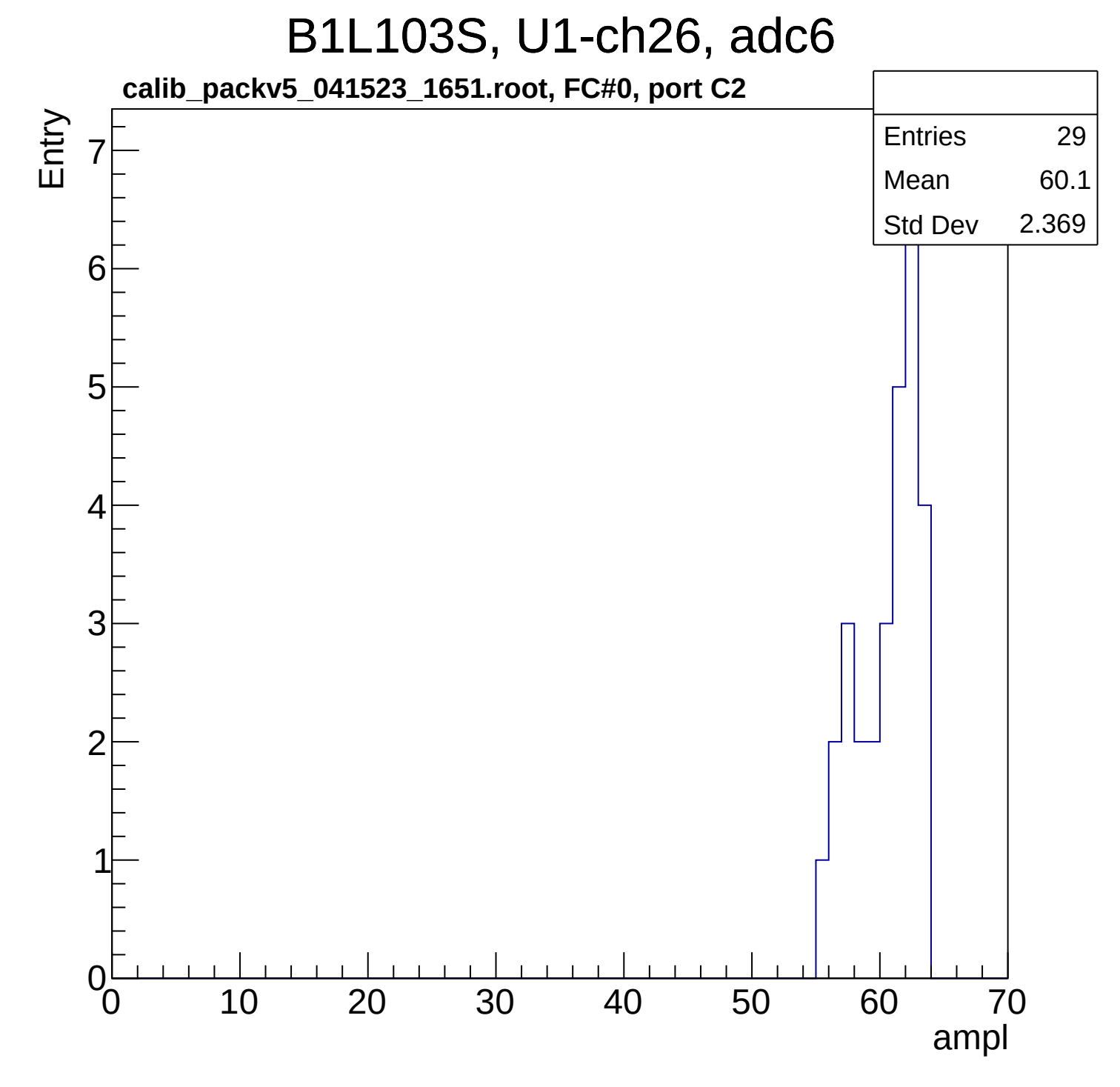
B1L103S, U1-ch26, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 29
Mean 60.1
Std Dev 2.369
Entry
ampl
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4
5
6
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0
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20
30
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50
60
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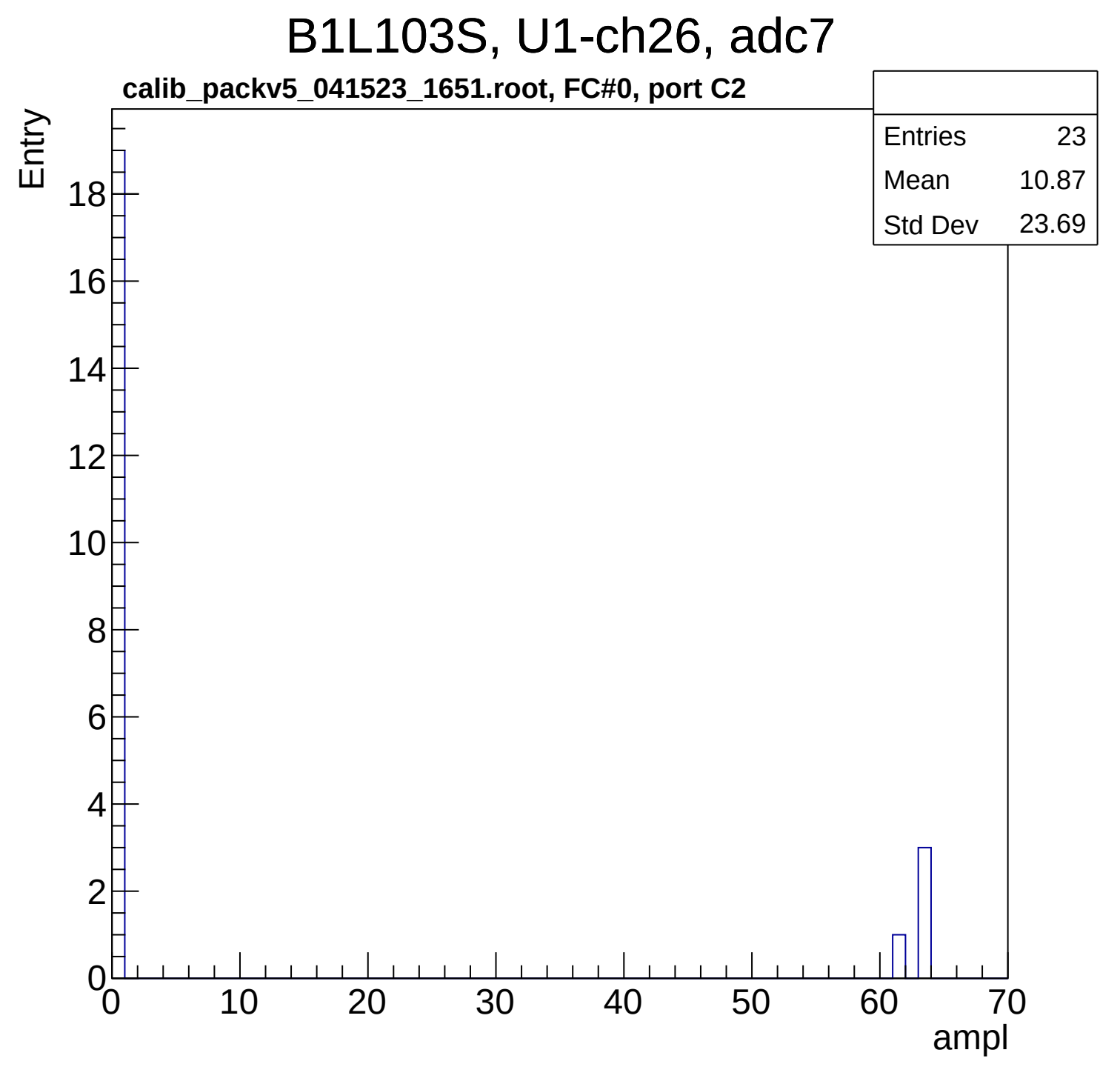
B1L103S, U1-ch26, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 23
Mean 10.87
Std Dev 23.69
Entry
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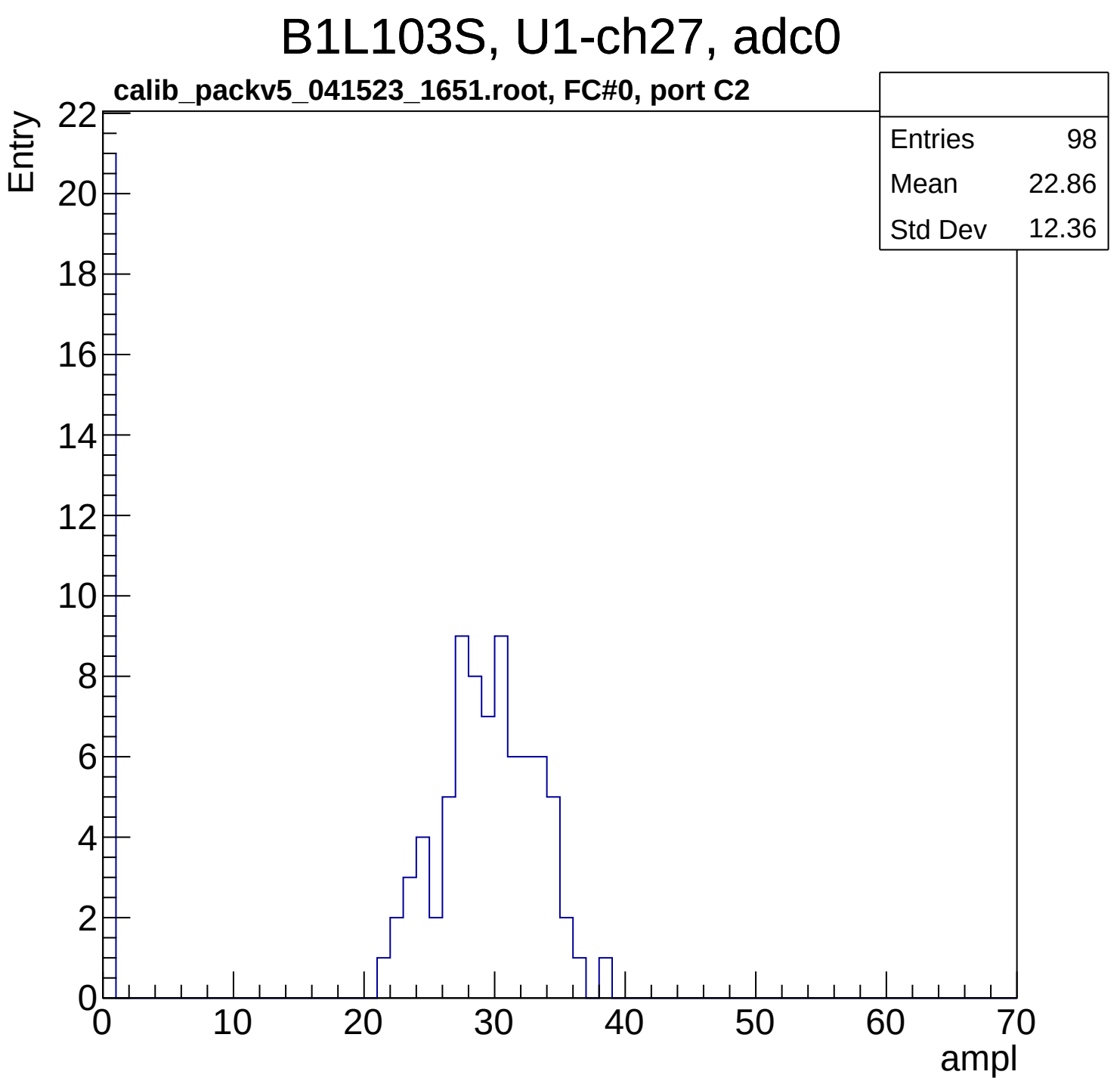
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch27, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 98
Mean 22.86
Std Dev 12.36
Entry
ampl
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8
10
12
14
16
18
20
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0
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60
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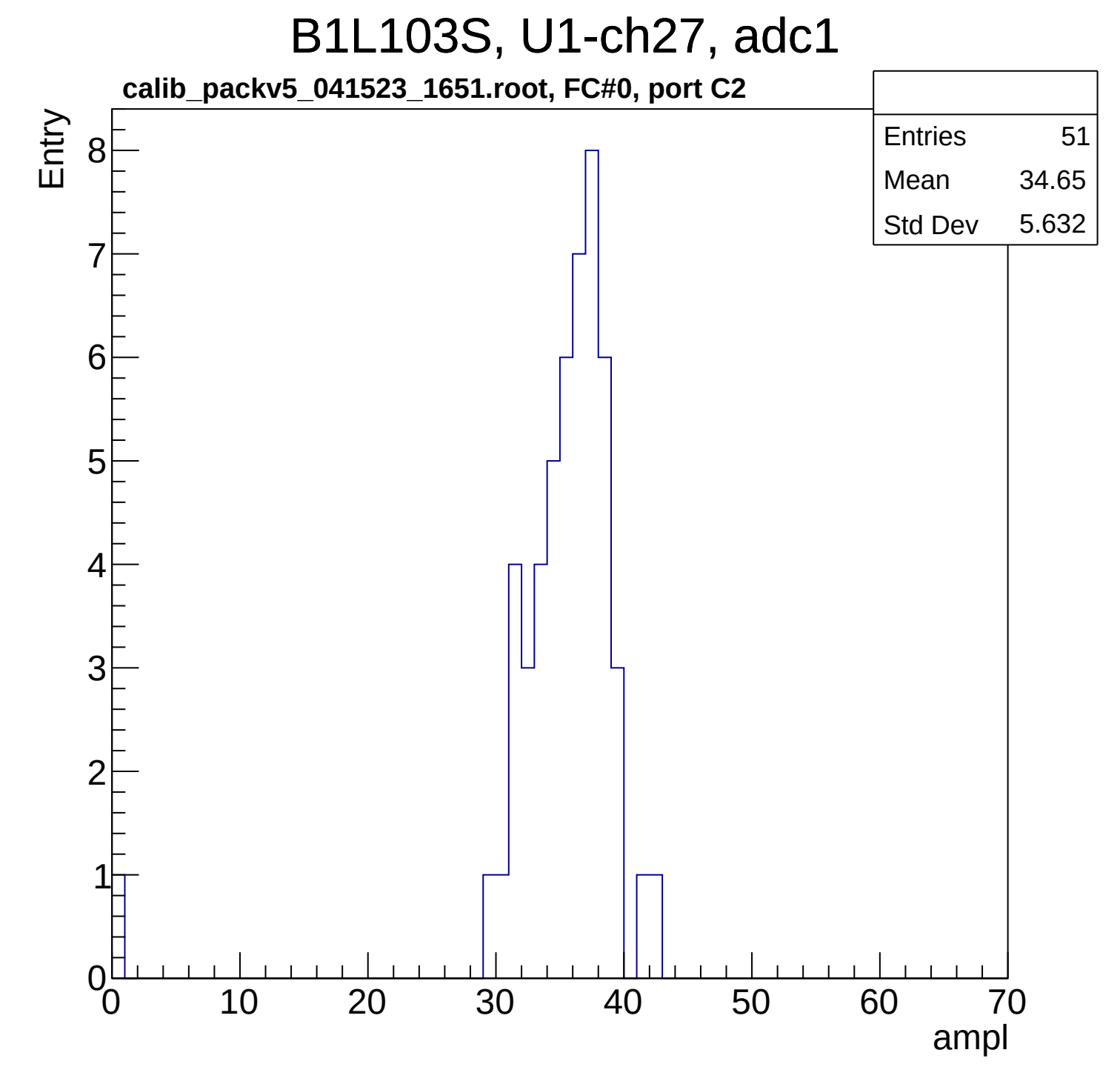
B1L103S, U1-ch27, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 34.65
Std Dev 5.632
Entry
ampl
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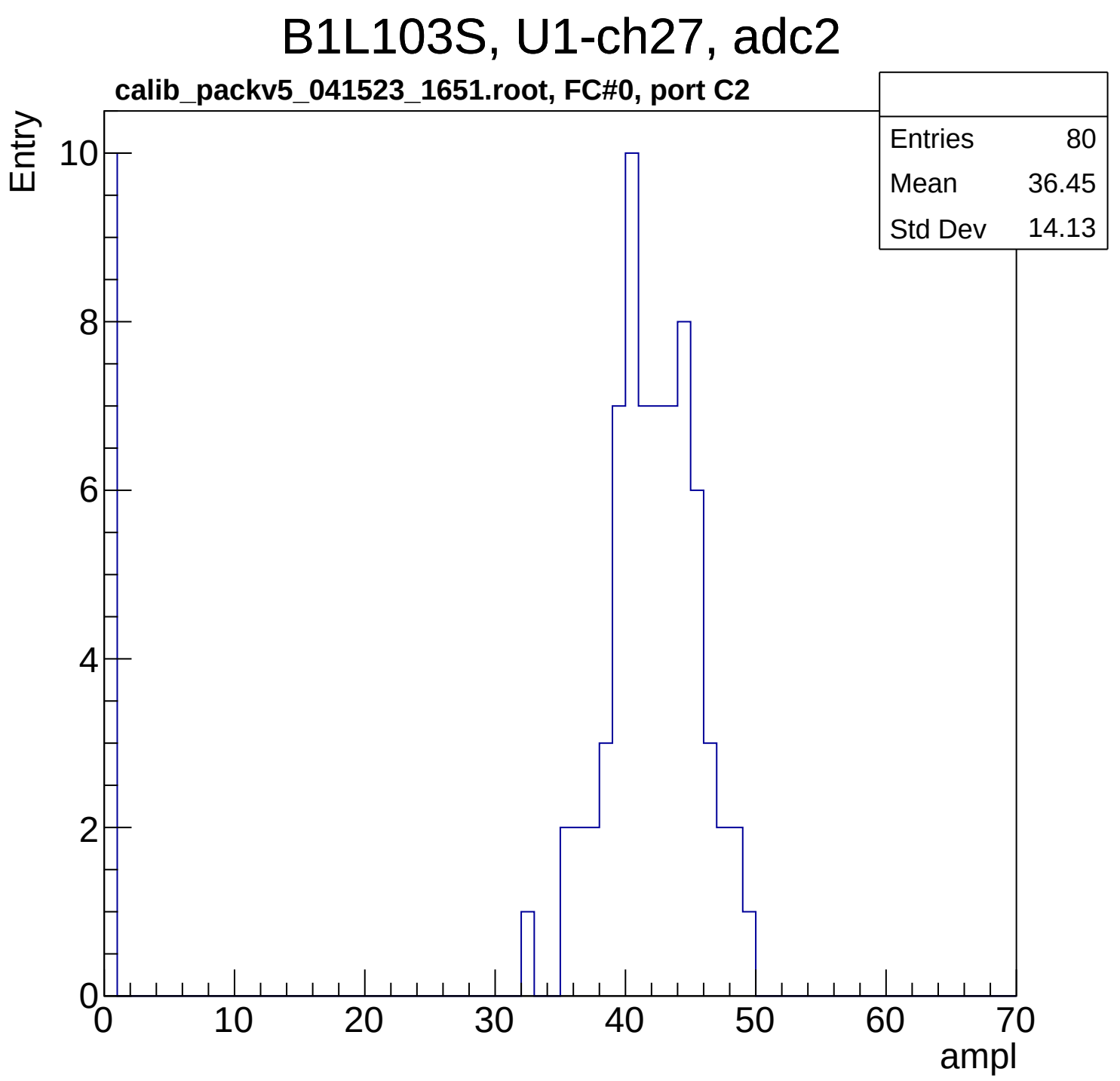
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U1-ch27, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 36.45
Std Dev 14.13
Entry
ampl
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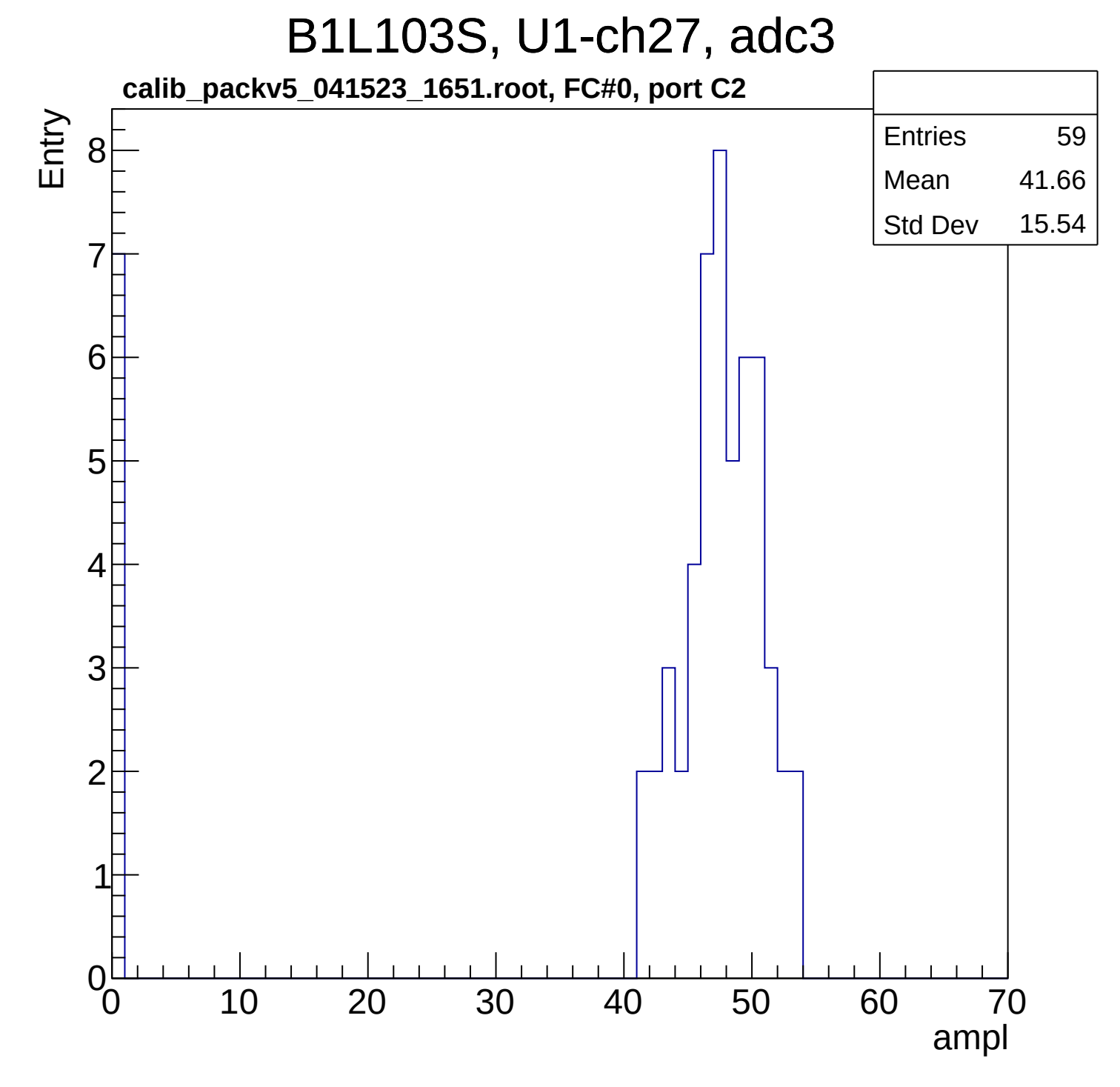
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U1-ch27, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 41.66
Std Dev 15.54
Entry
ampl
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4
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7
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0
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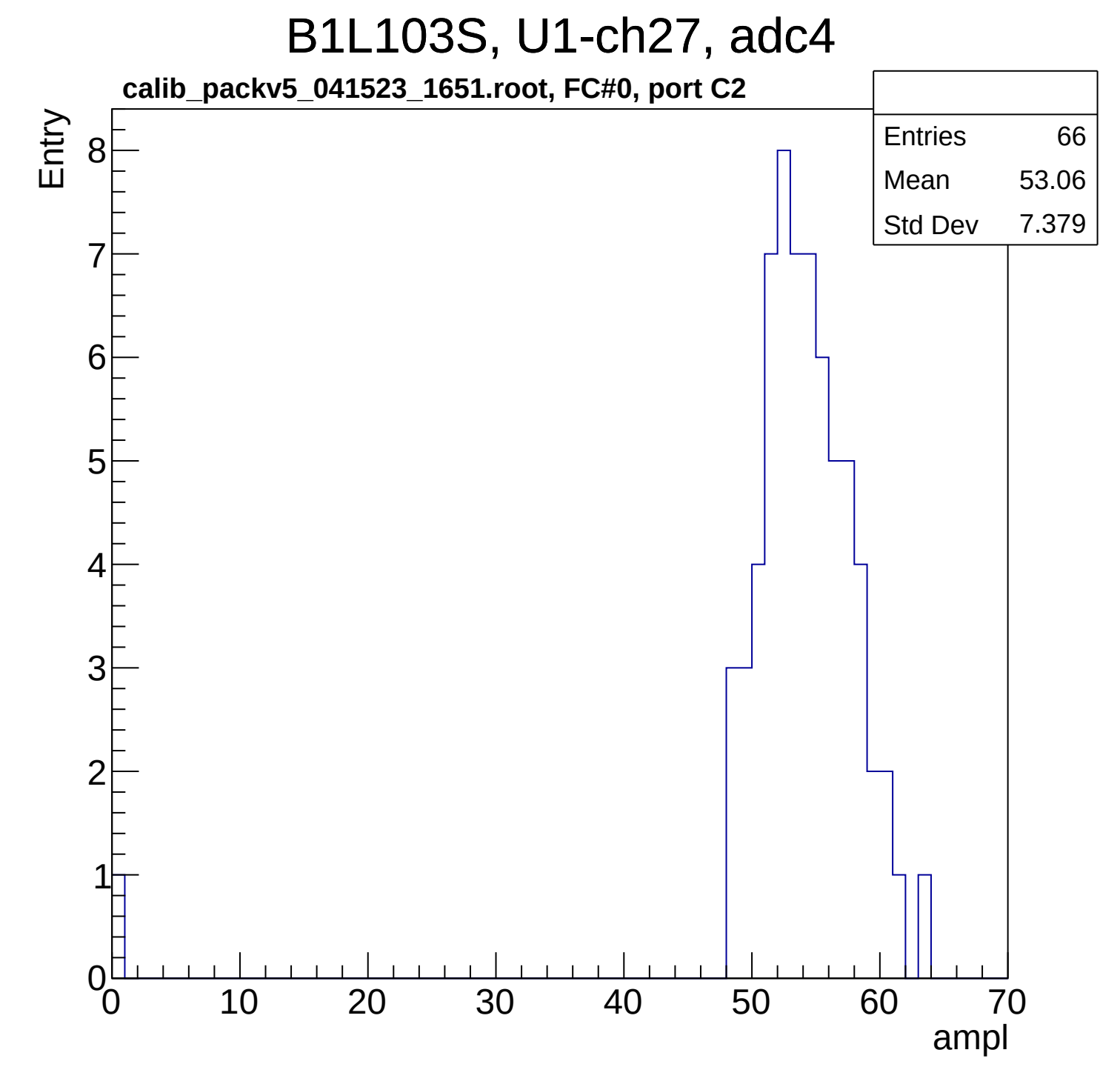
B1L103S, U1-ch27, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 53.06
Std Dev 7.379
Entry
ampl
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2
3
4
5
6
7
8
0
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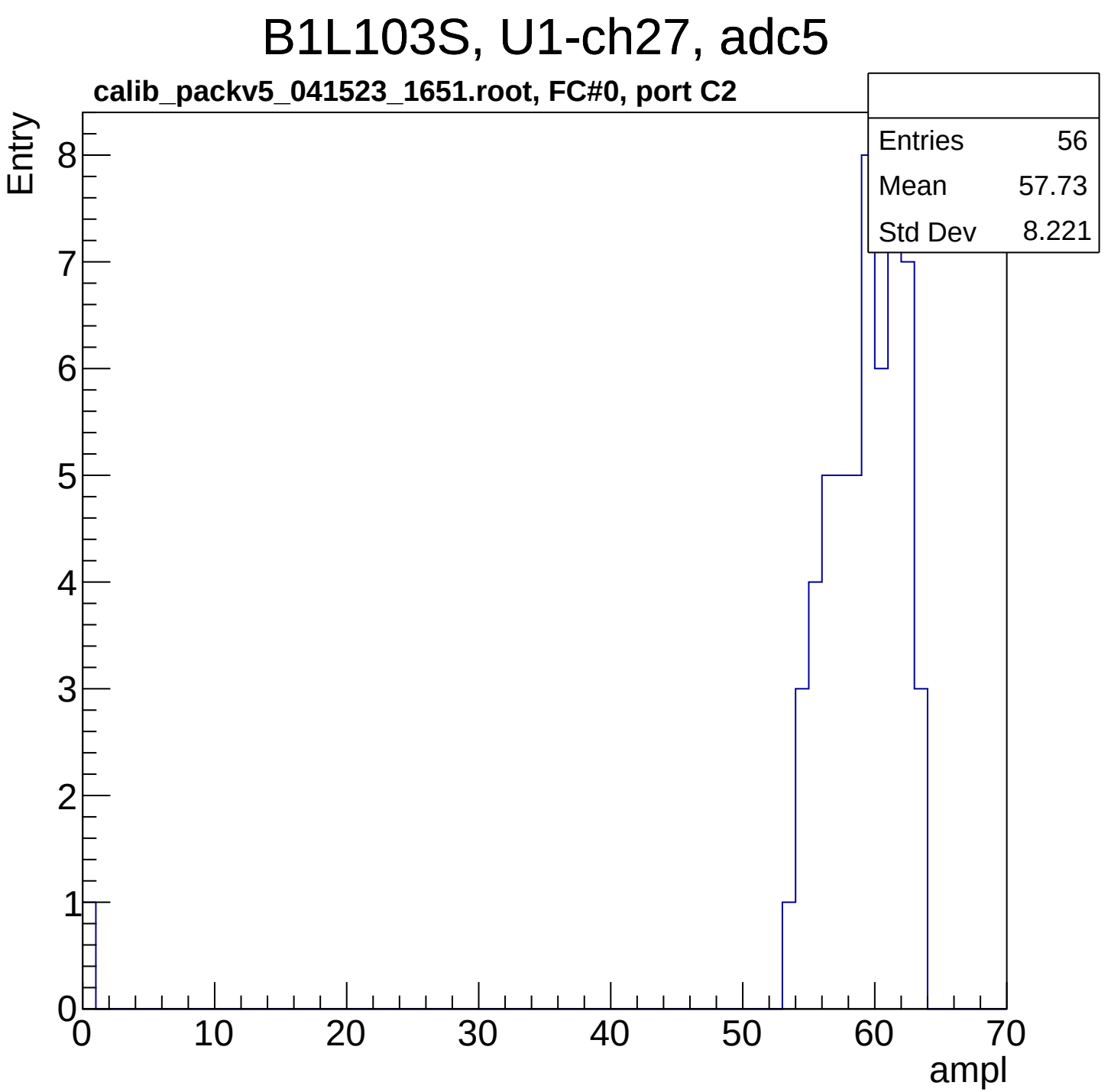
20
30
40
50
60
70


B1L103S, U1-ch27, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 57.73
Std Dev 8.221
Entry
ampl
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2
3
4
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6
7
8
0
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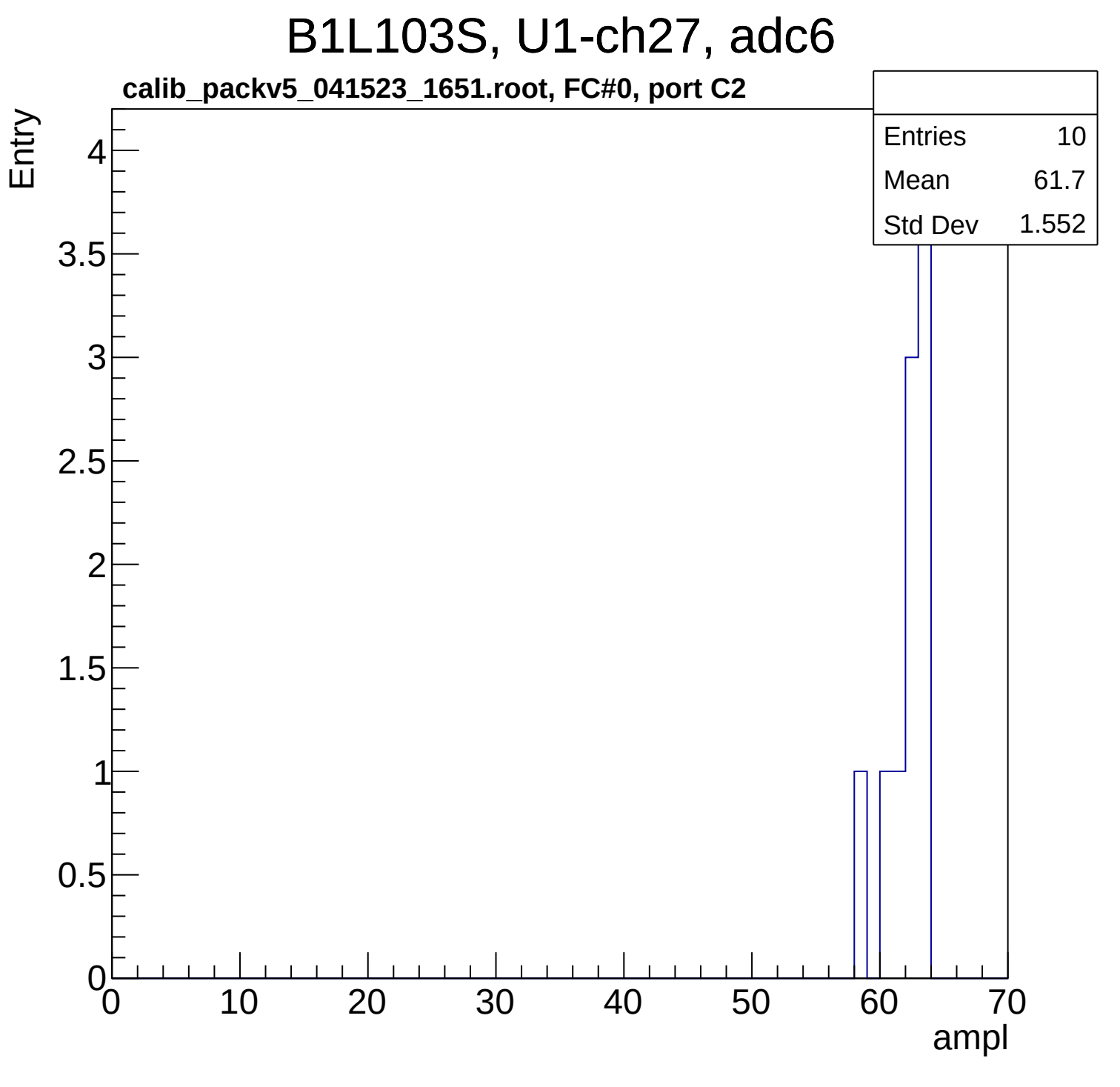
60
70


B1L103S, U1-ch27, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 61.7
Std Dev 1.552
Entry
ampl
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1.5
2
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3.5
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0
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40
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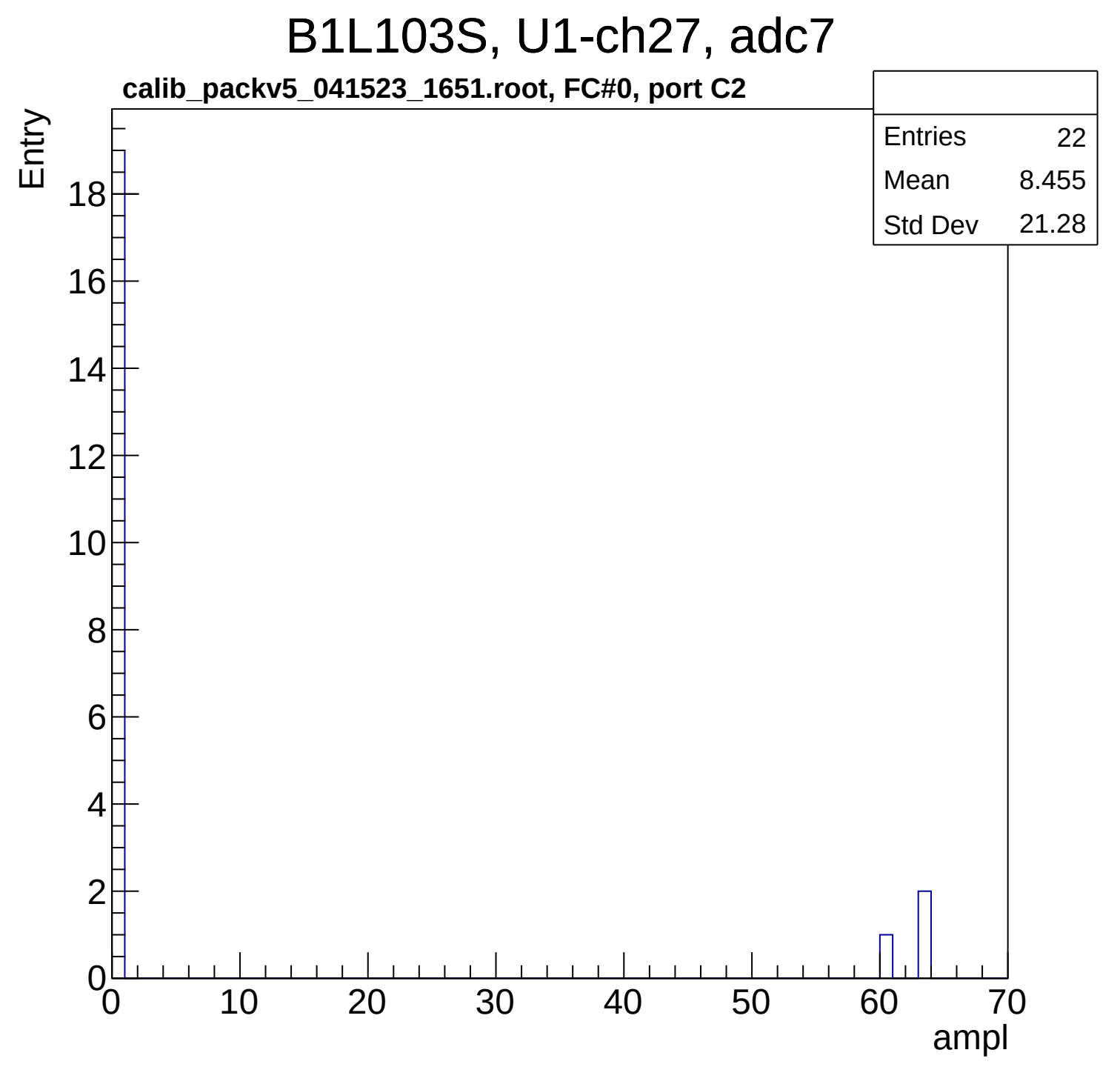
60
70


B1L103S, U1-ch27, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 8.455
Std Dev 21.28
Entry
0
2
4
6
8
10
12
14
16
18
0
10
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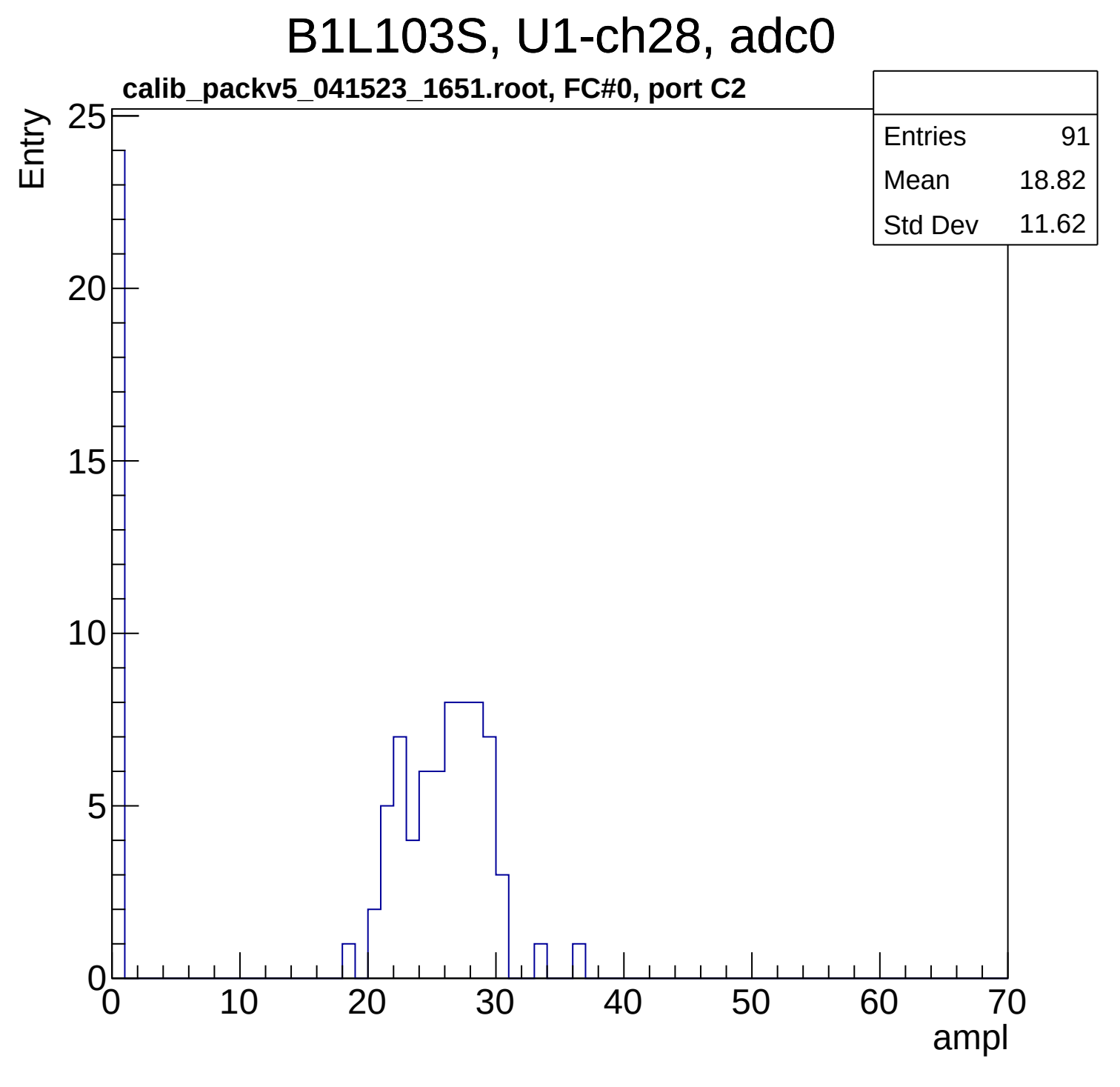
50
60
70
ampl


B1L103S, U1-ch28, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 91
Mean 18.82
Std Dev 11.62
Entry
ampl
0
5
10
15
20
25
0
10
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40
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60
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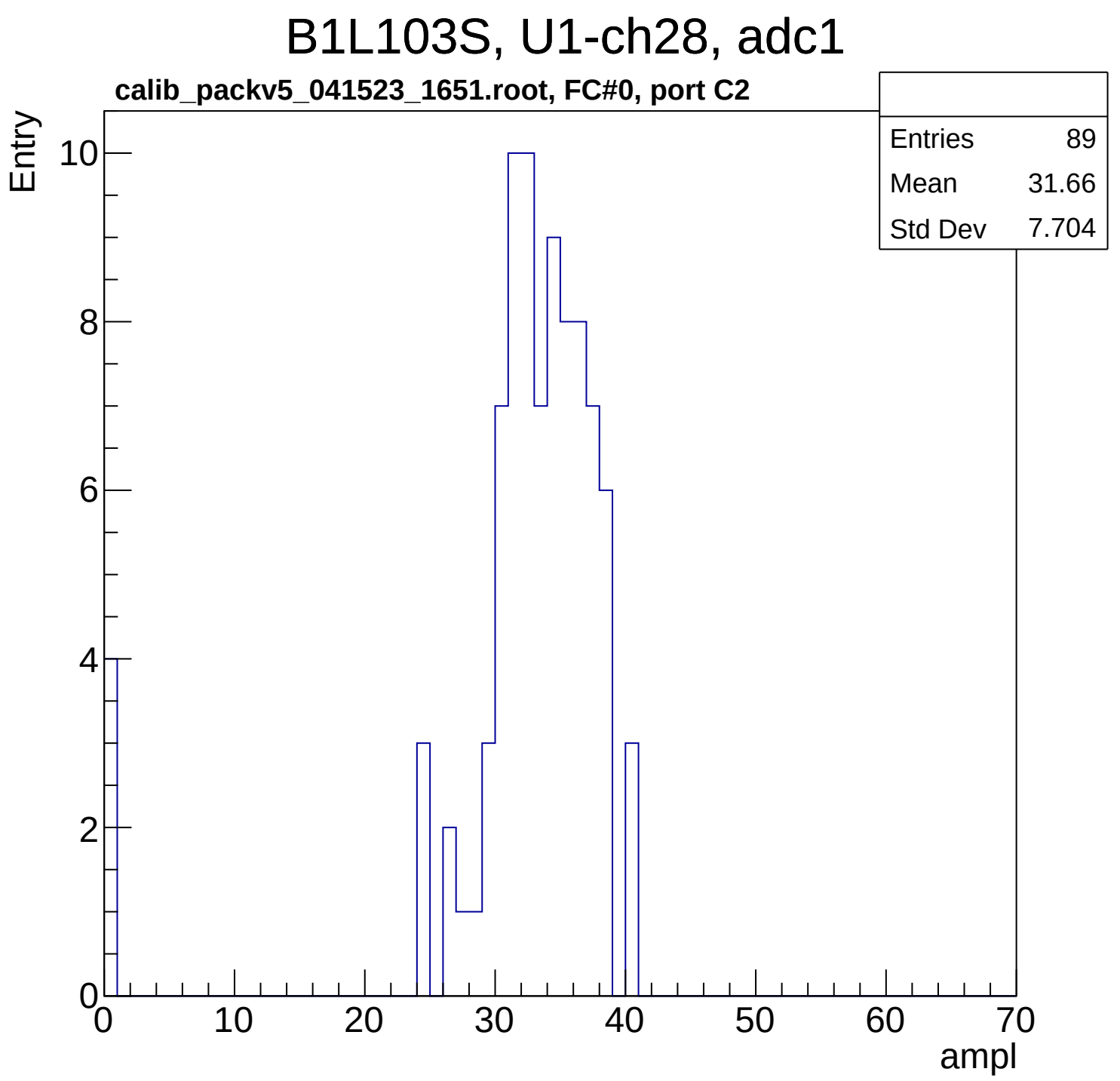
B1L103S, U1-ch28, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 89
Mean 31.66
Std Dev 7.704
Entry
ampl
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2
4
6
8
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0
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20
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40
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60
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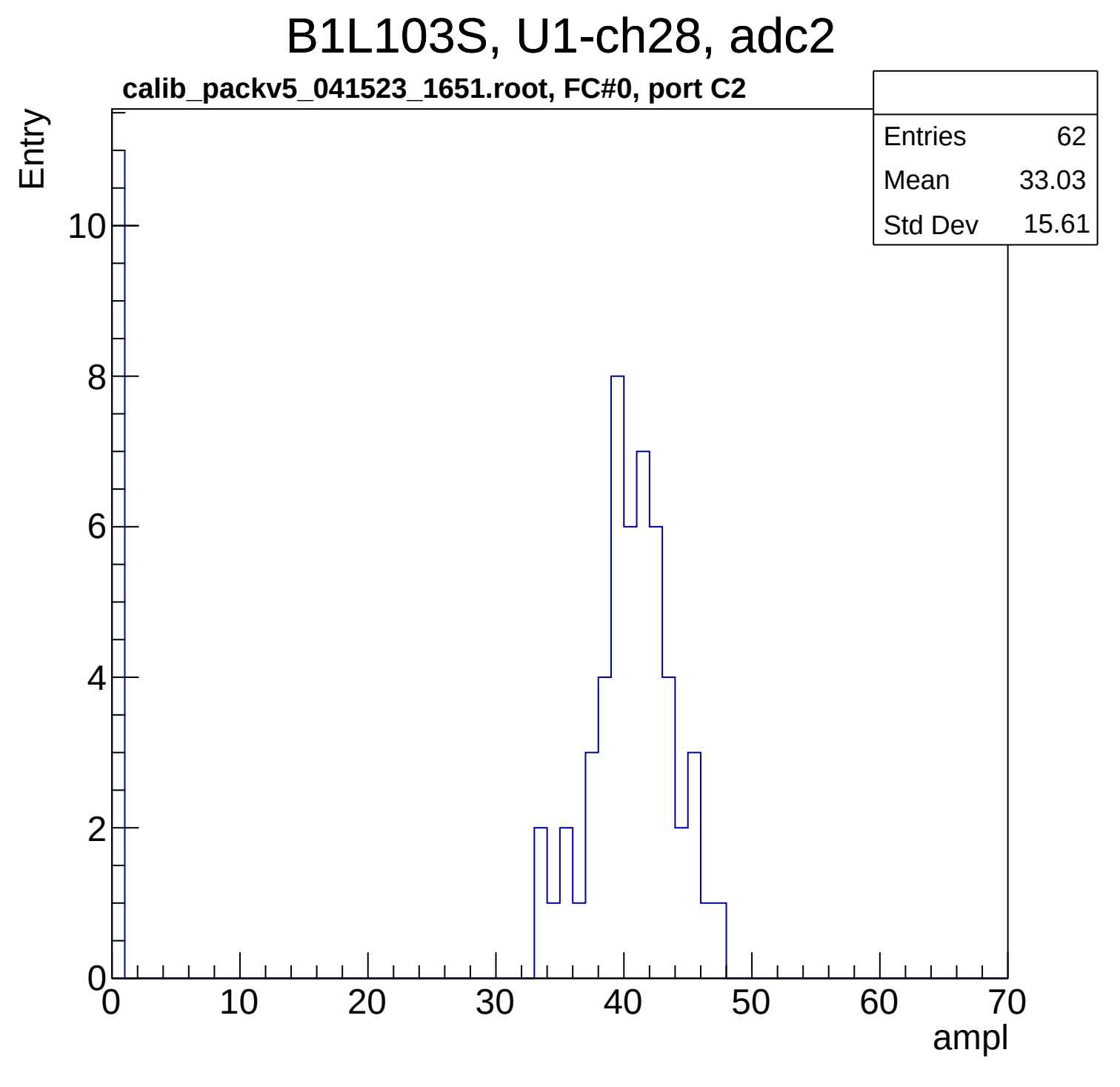
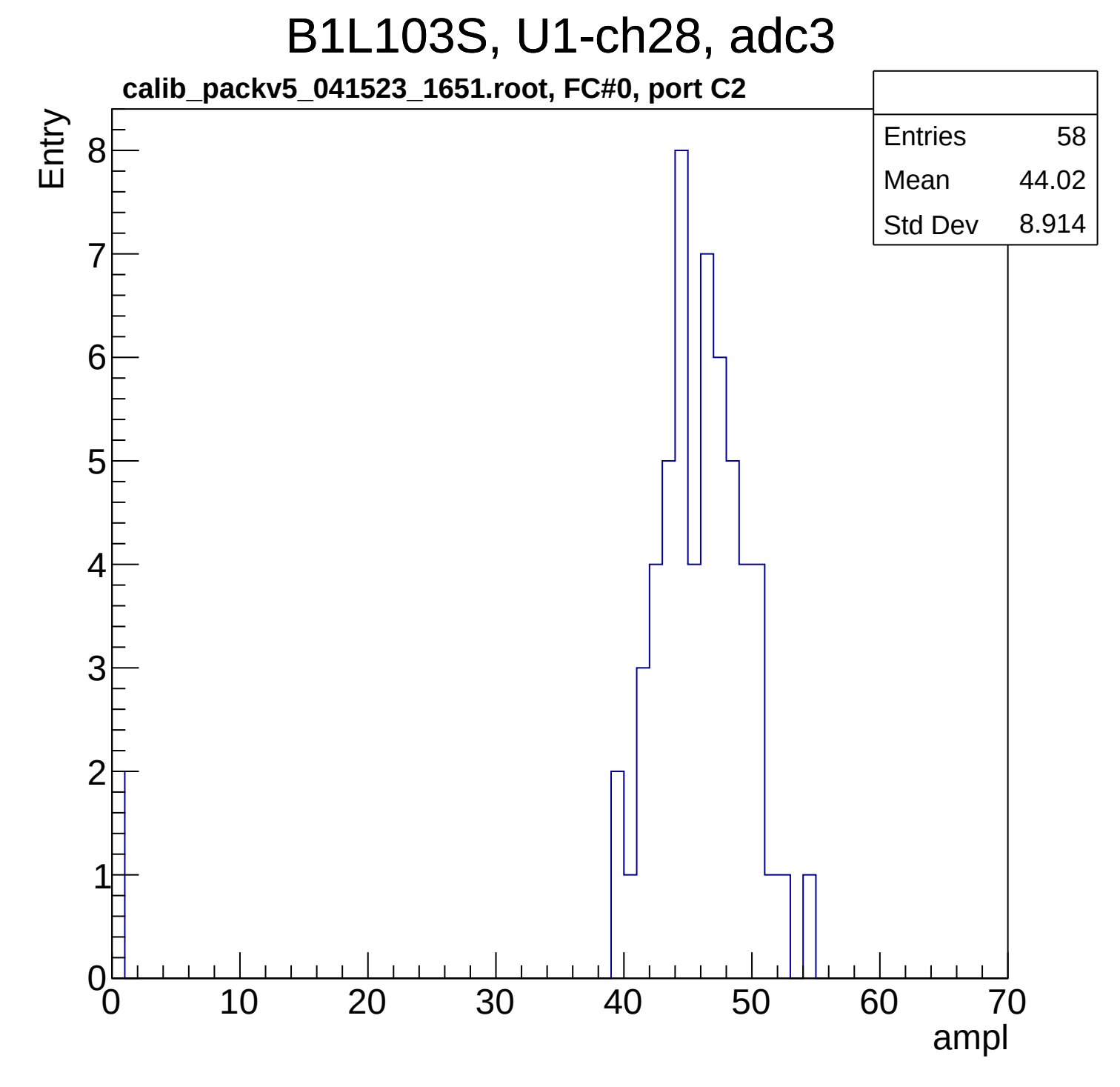

B1L103S, U1-ch28, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 33.03
Std Dev 15.61
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch28, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 44.02
Std Dev 8.914
Entry
ampl
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2
3
4
5
6
7
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0
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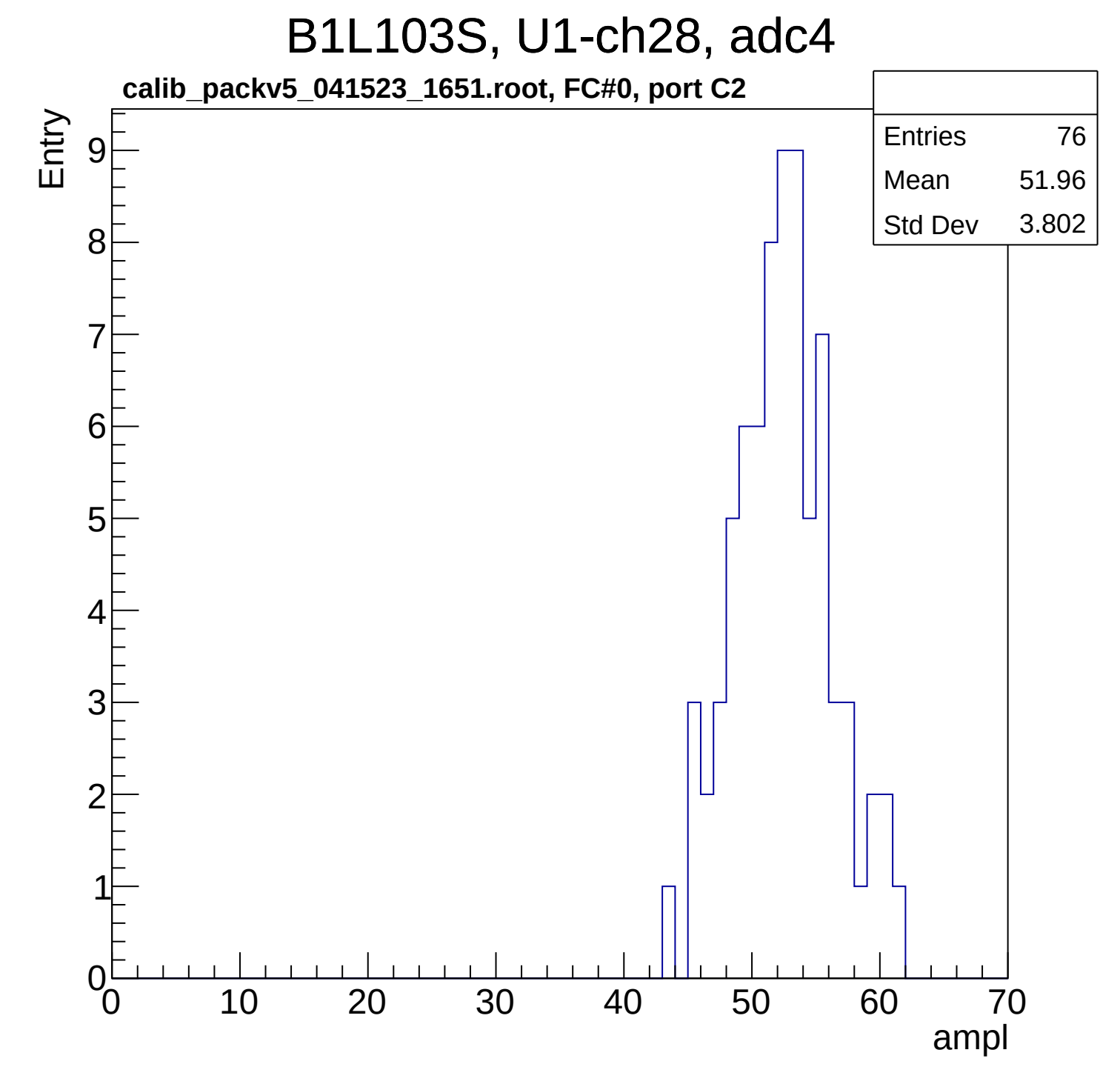
60
70


B1L103S, U1-ch28, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 51.96
Std Dev 3.802
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
50
60
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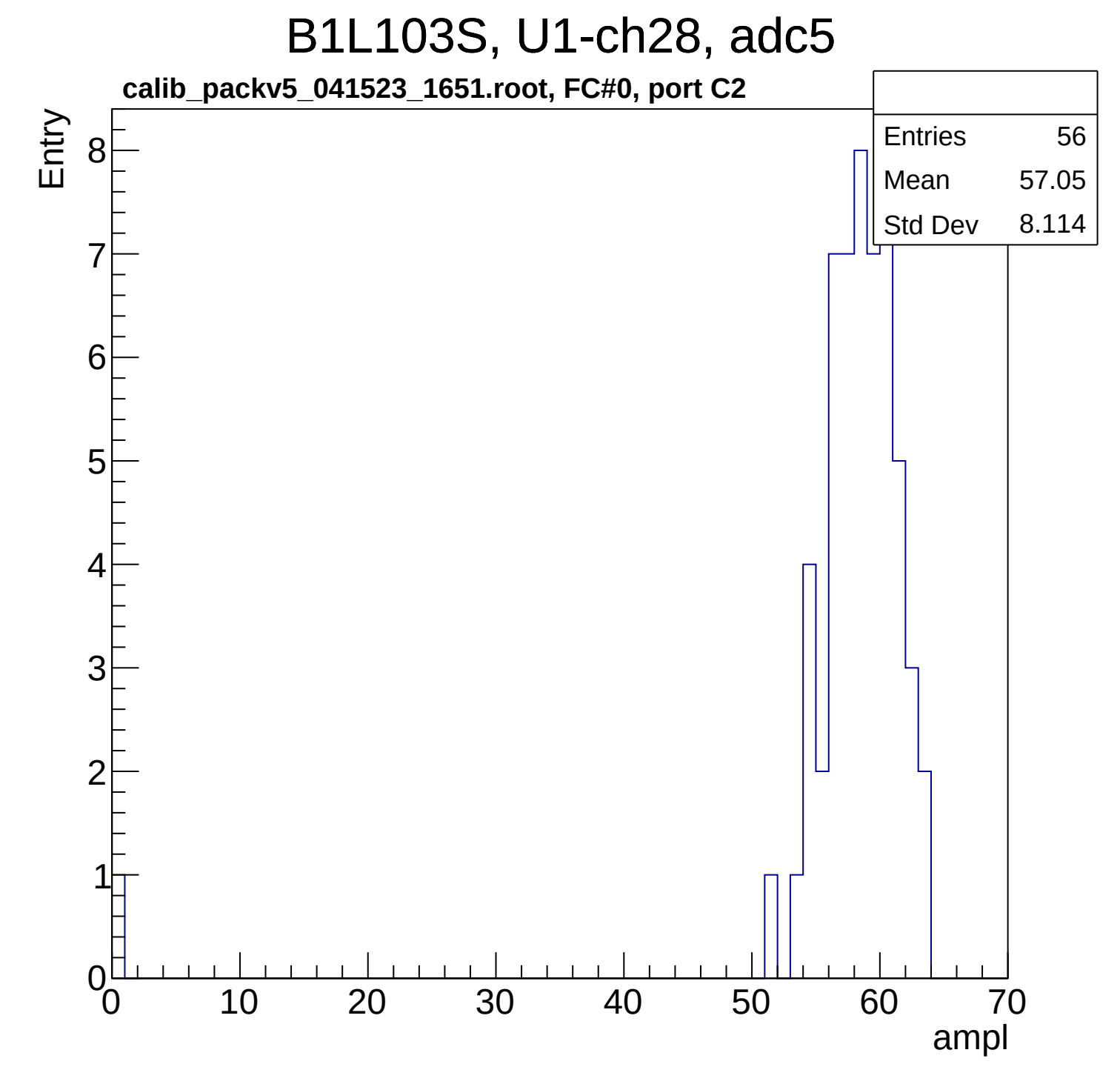
B1L103S, U1-ch28, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 57.05
Std Dev 8.114
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
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60
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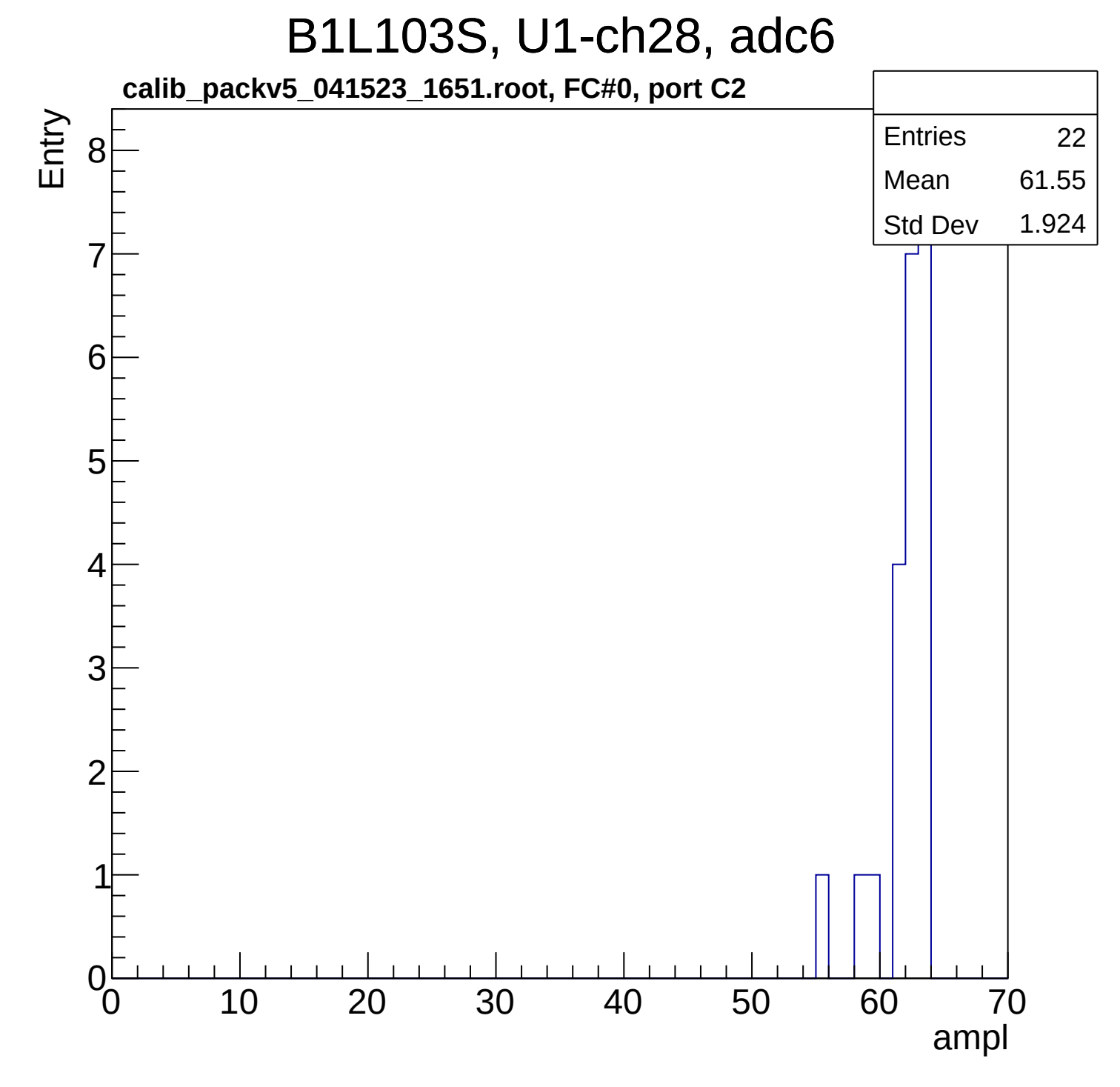
B1L103S, U1-ch28, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 61.55
Std Dev 1.924
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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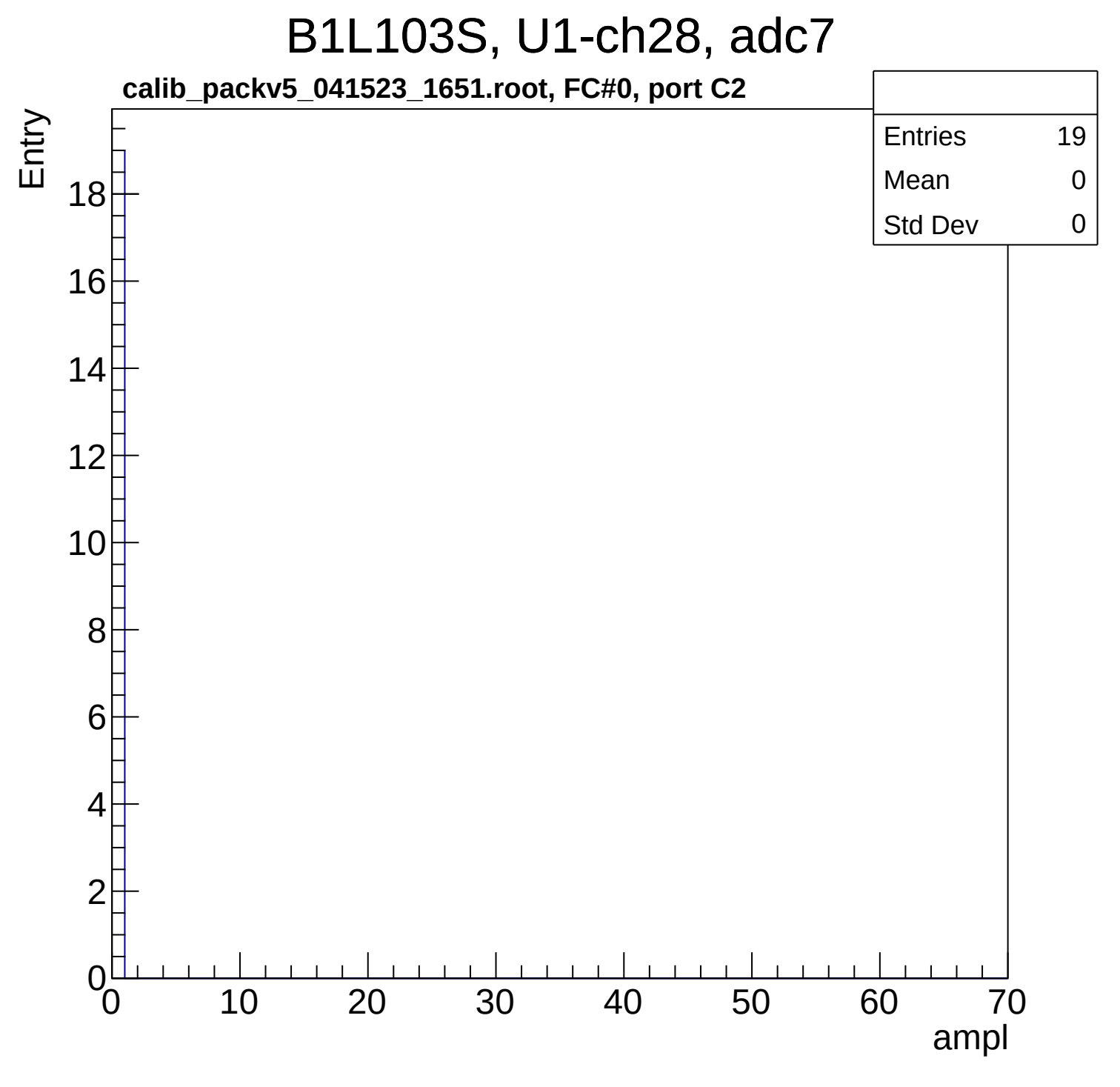
B1L103S, U1-ch28, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
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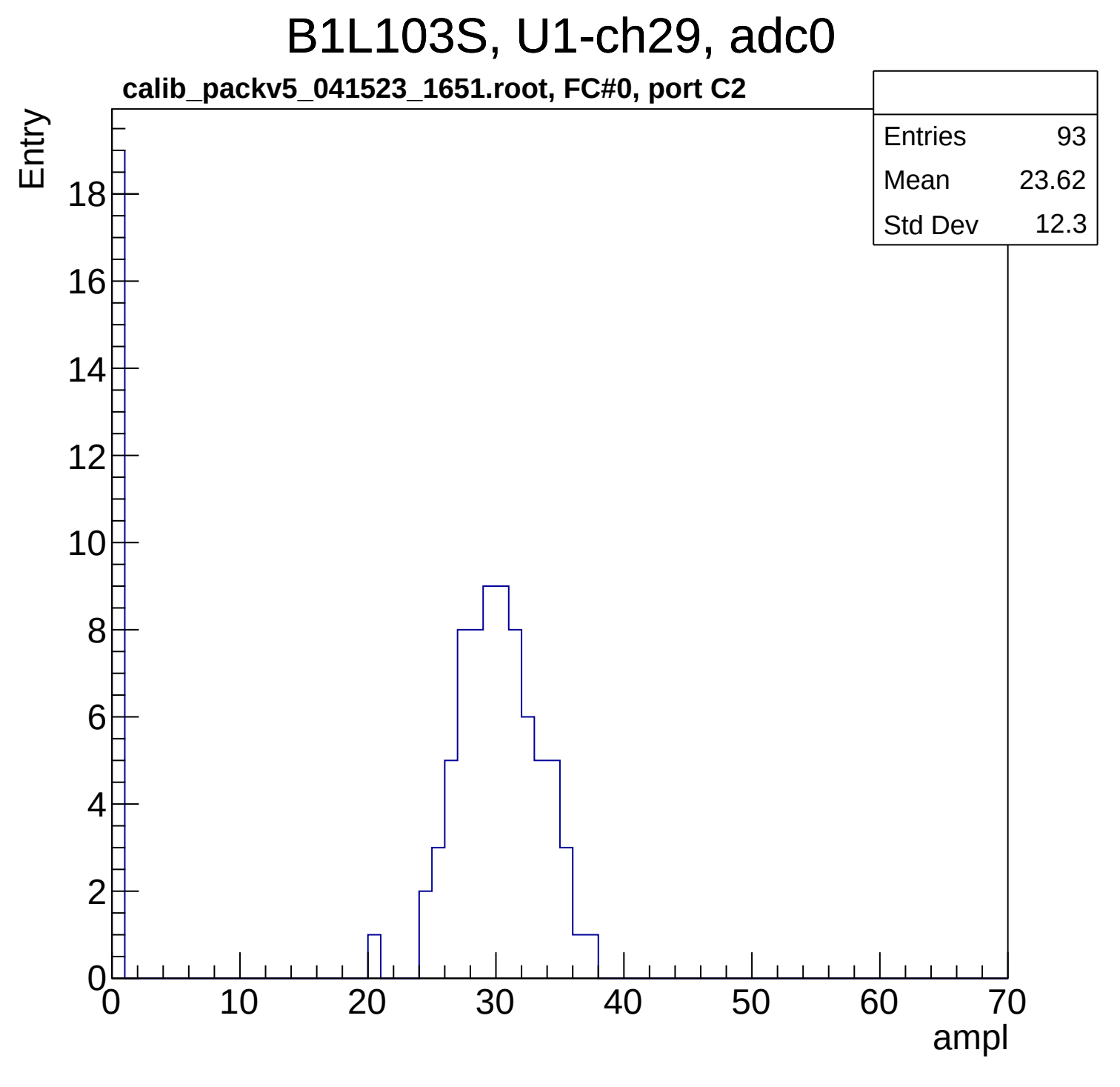
50
60
70
ampl


B1L103S, U1-ch29, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 93
Mean 23.62
Std Dev 12.3
Entry
ampl
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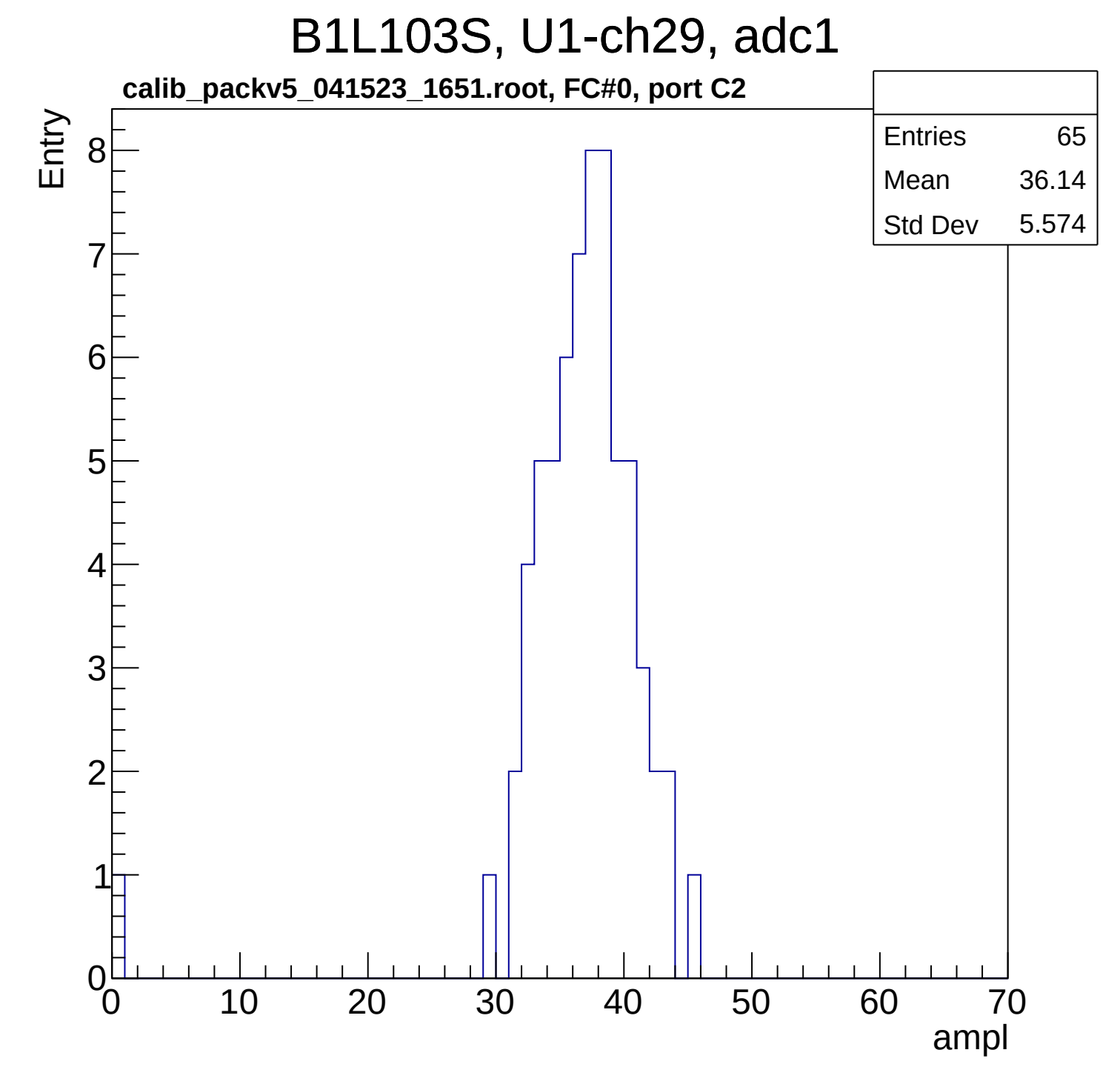
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70


B1L103S, U1-ch29, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 36.14
Std Dev 5.574
Entry
ampl
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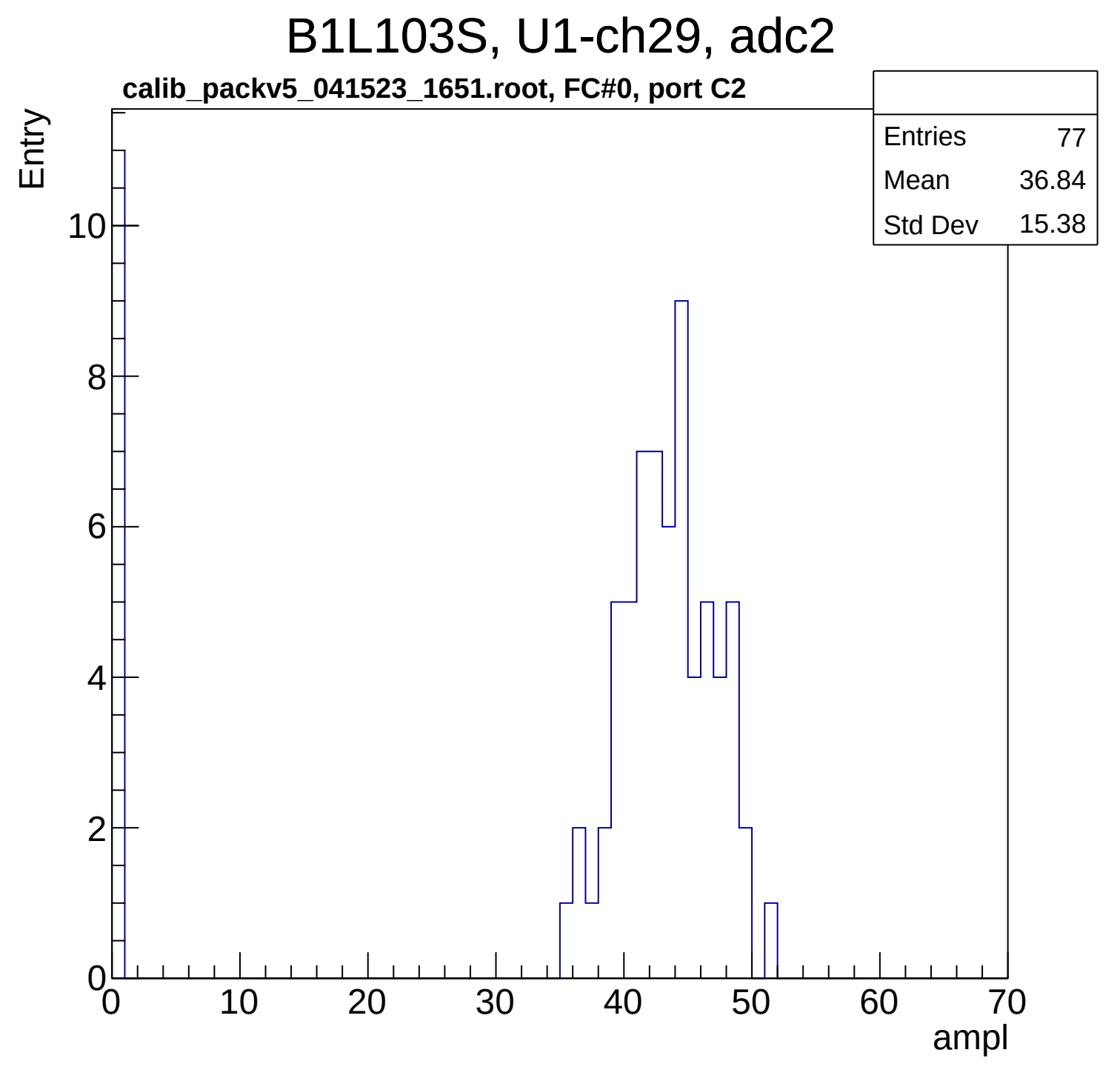
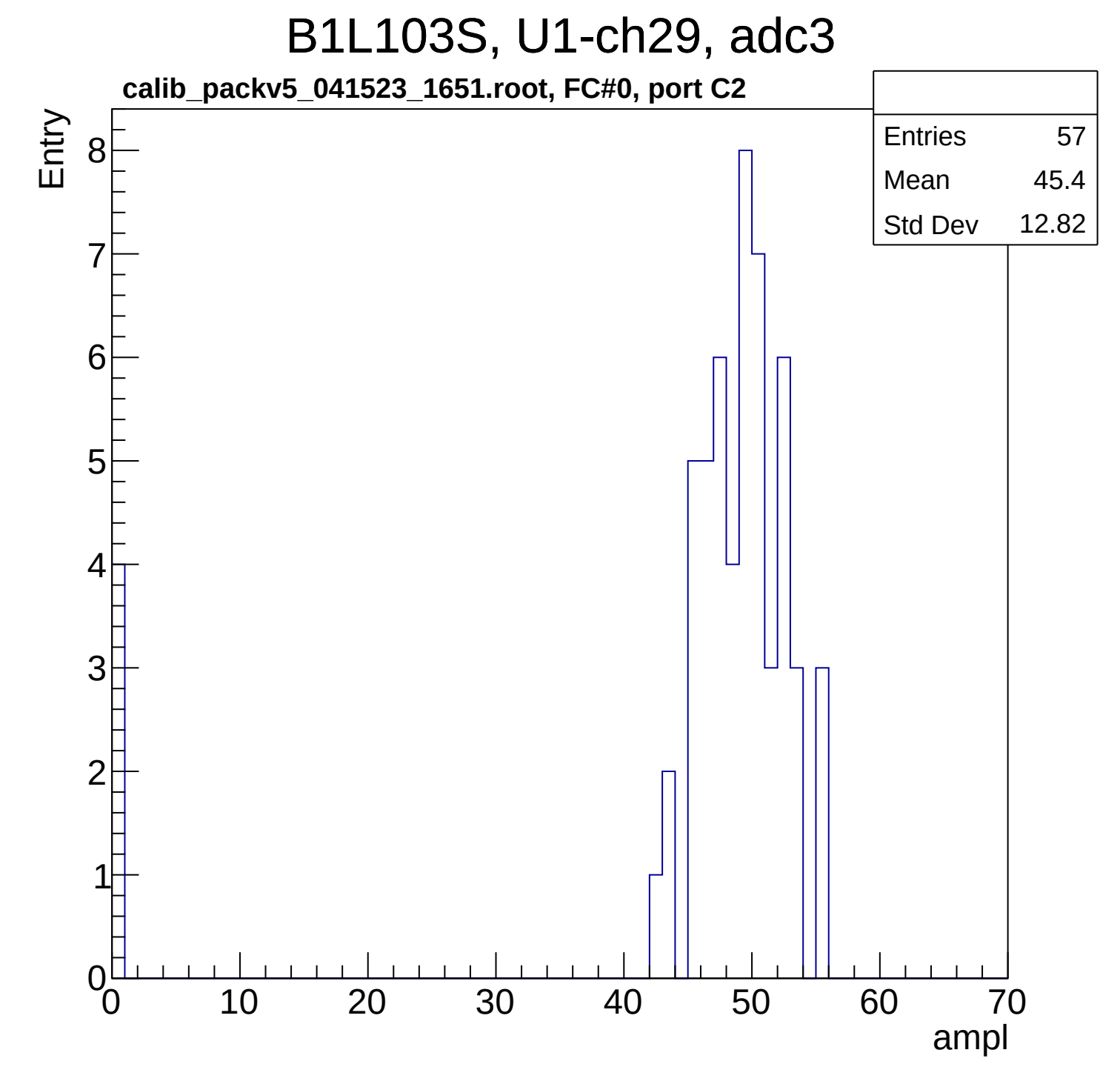
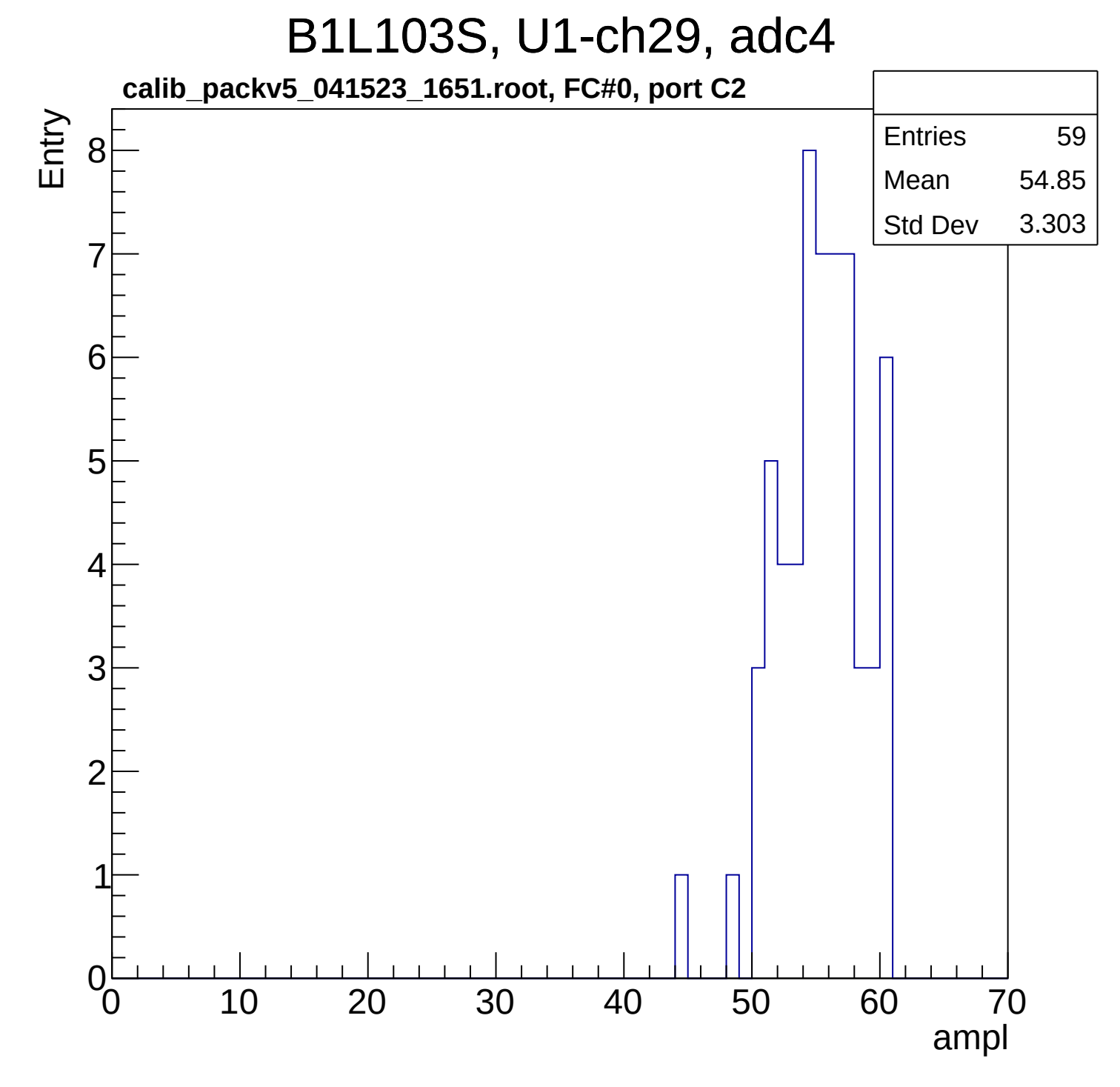
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U1-ch29, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 36.84
Std Dev 15.38
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch29, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 45.4
Std Dev 12.82
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U1-ch29, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 54.85
Std Dev 3.303
Entry
ampl
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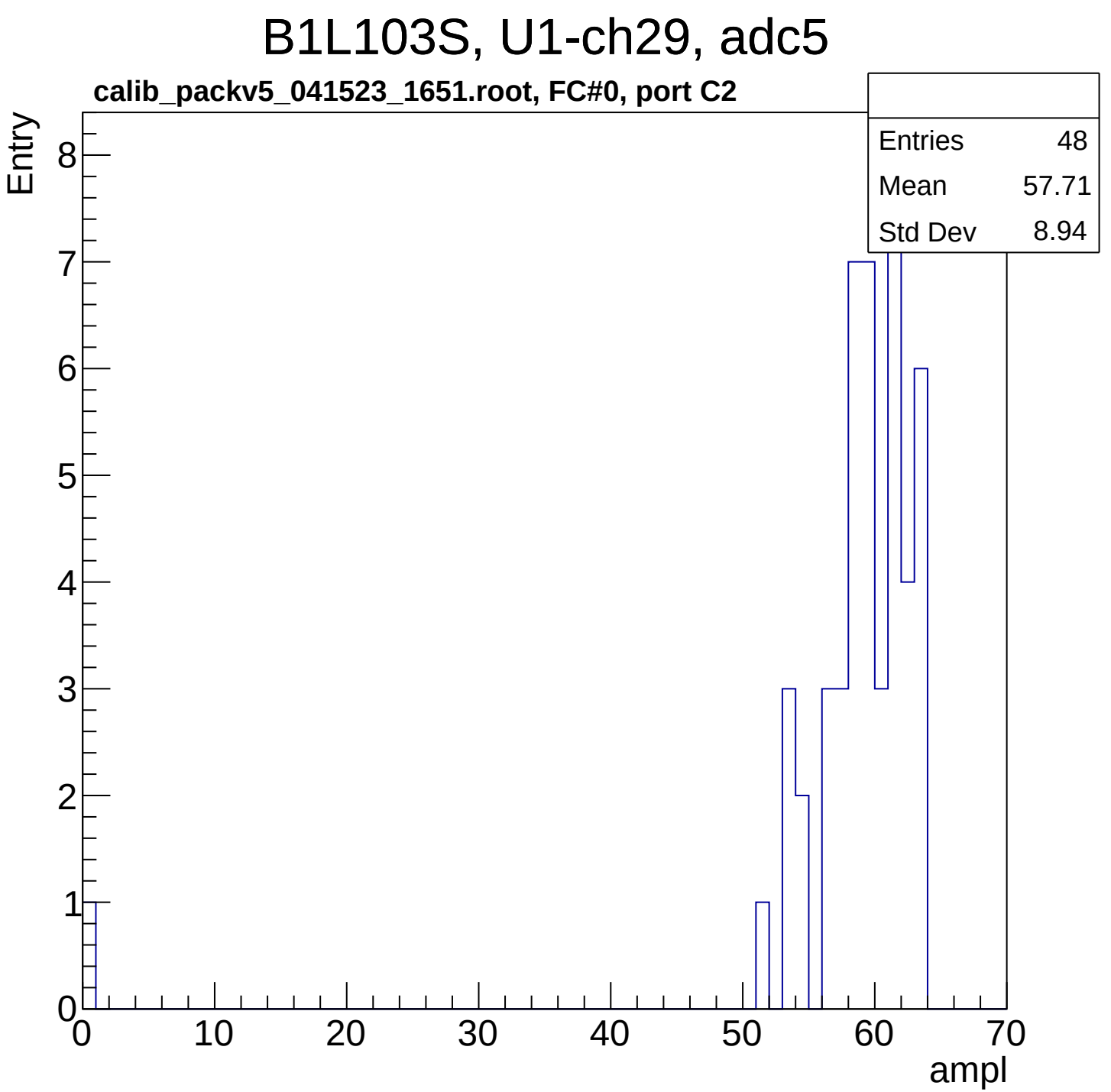
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U1-ch29, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 57.71
Std Dev 8.94
Entry
ampl
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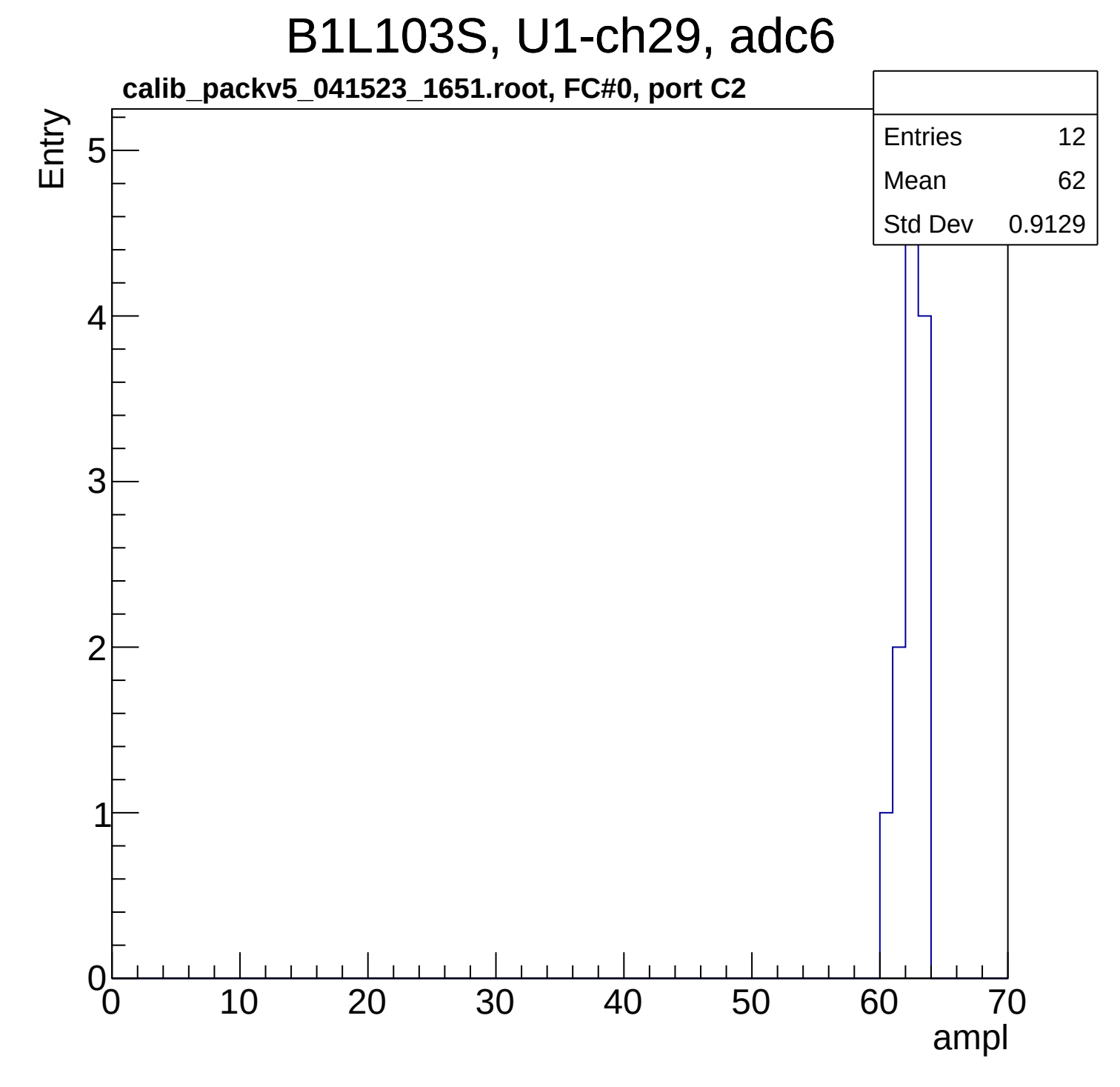
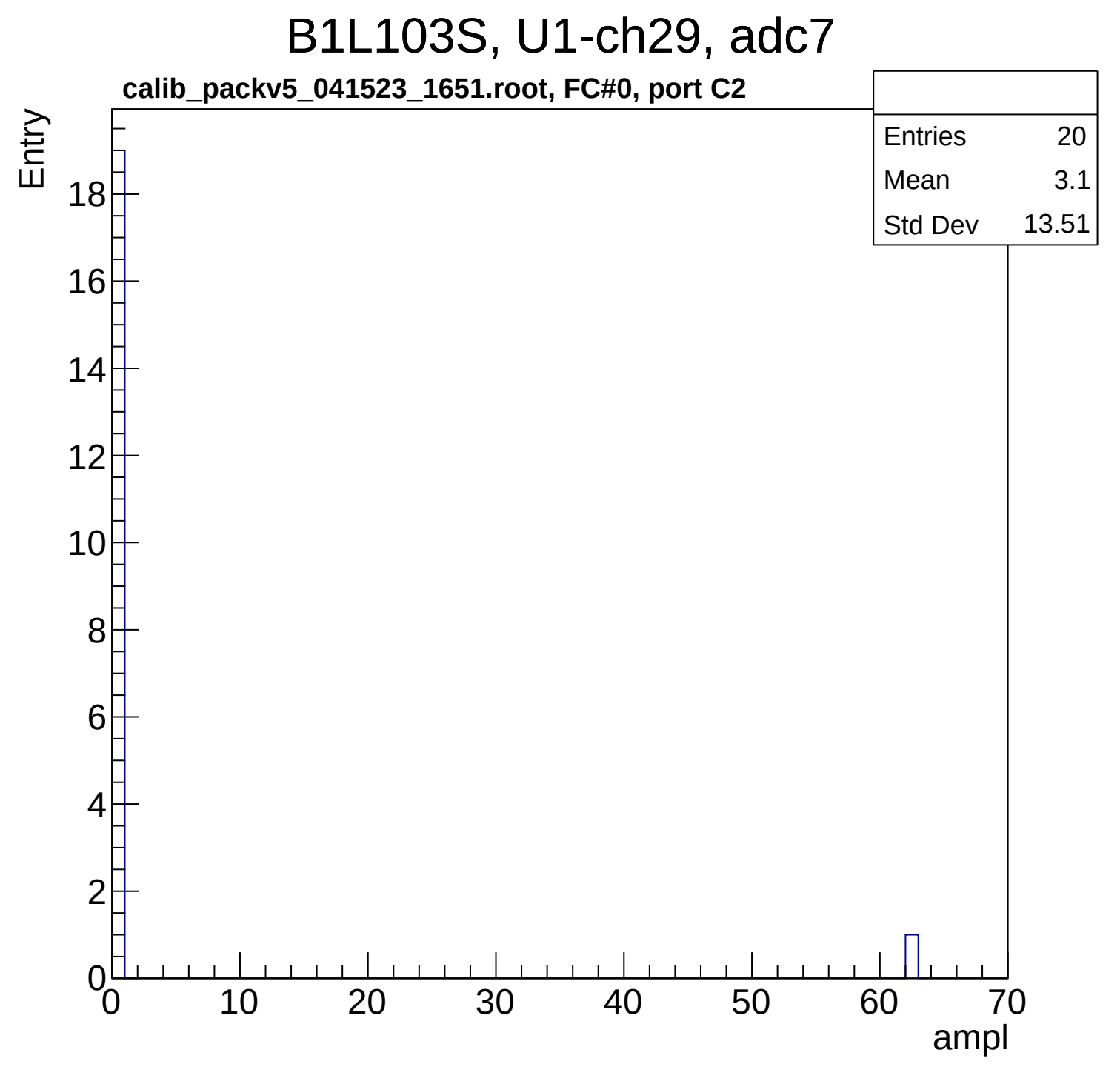
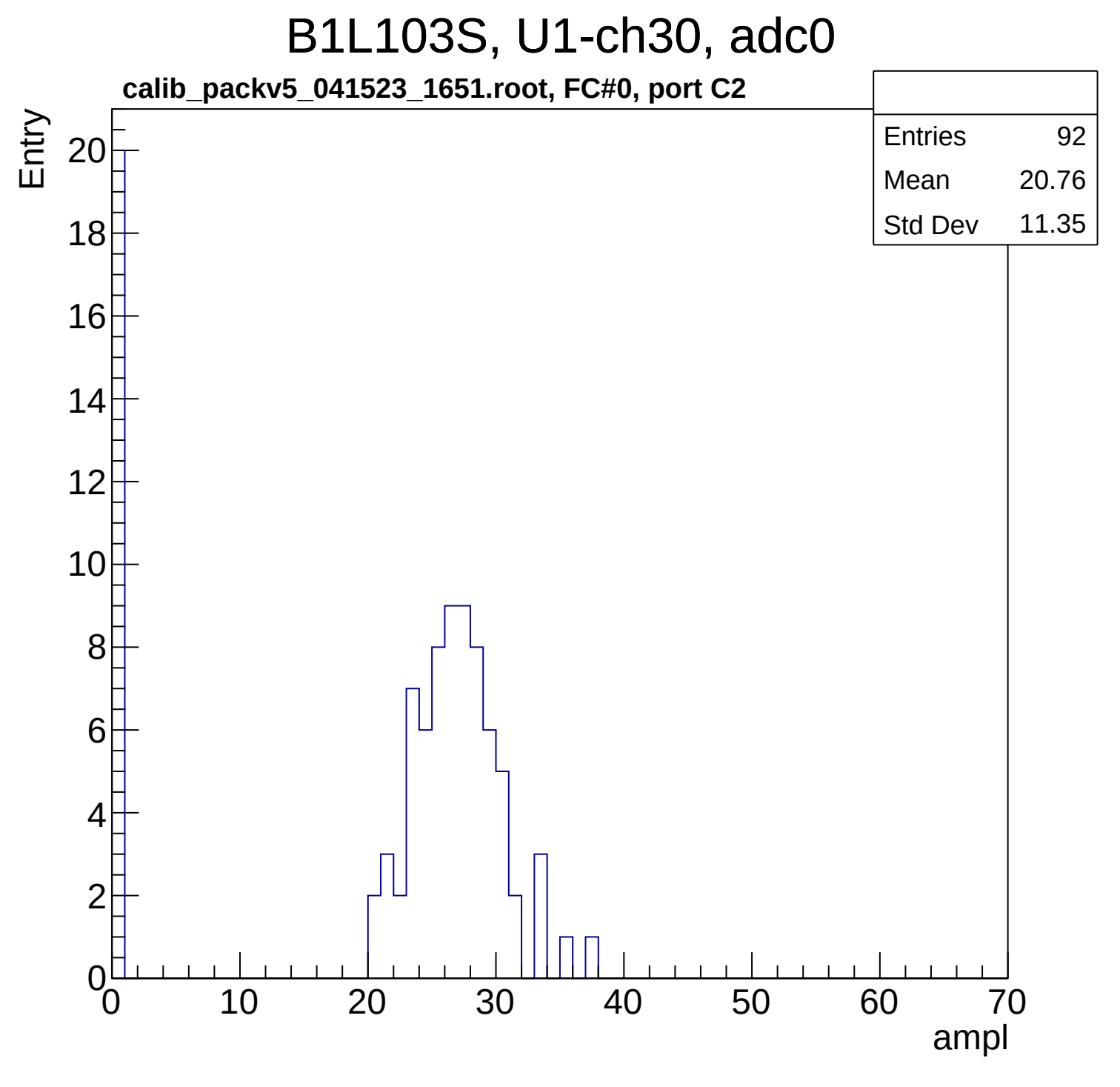
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U1-ch29, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 62
Std Dev 0.9129
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch29, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.1
Std Dev 13.51
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch30, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 92
Mean 20.76
Std Dev 11.35
Entry
ampl
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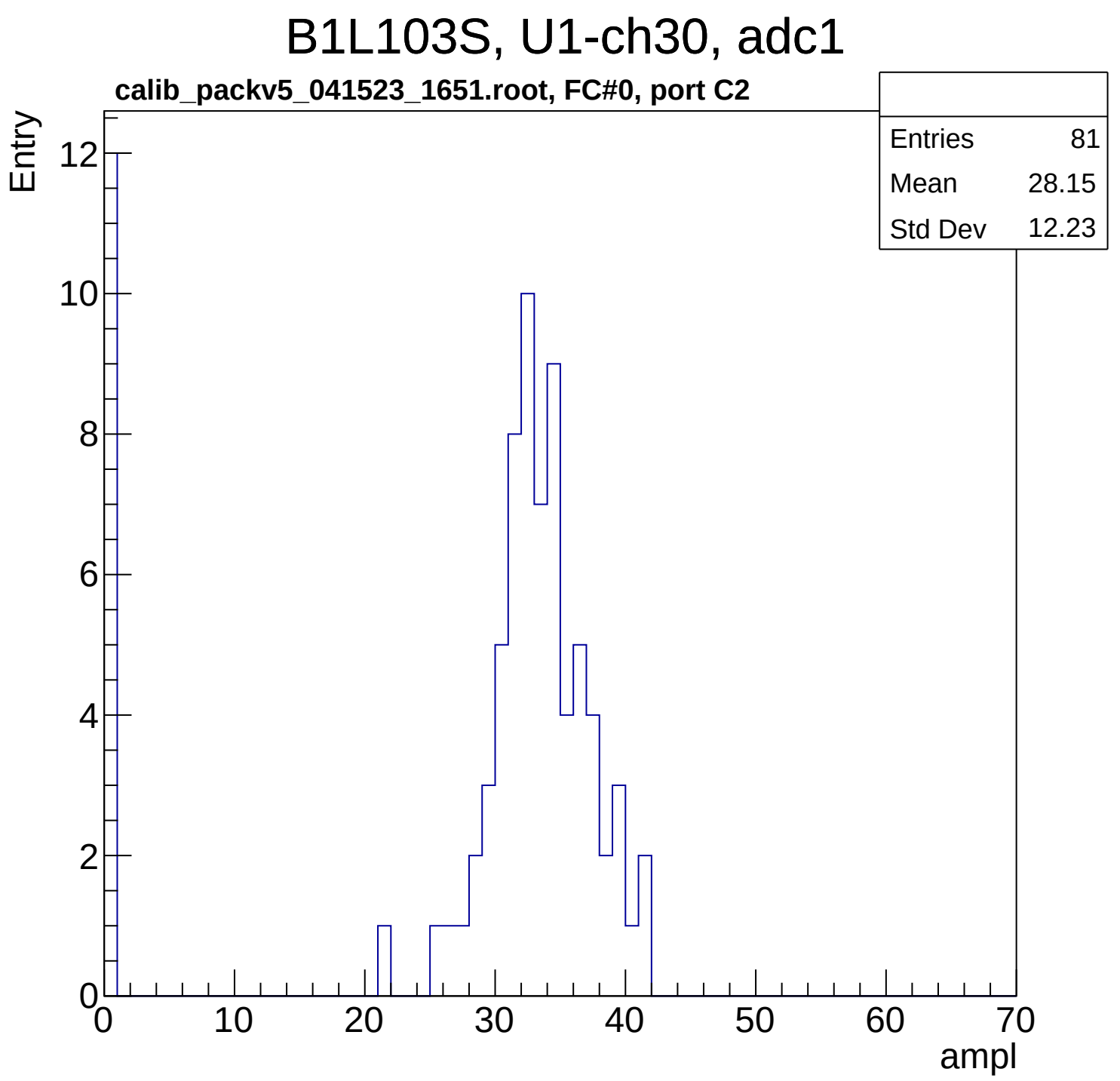
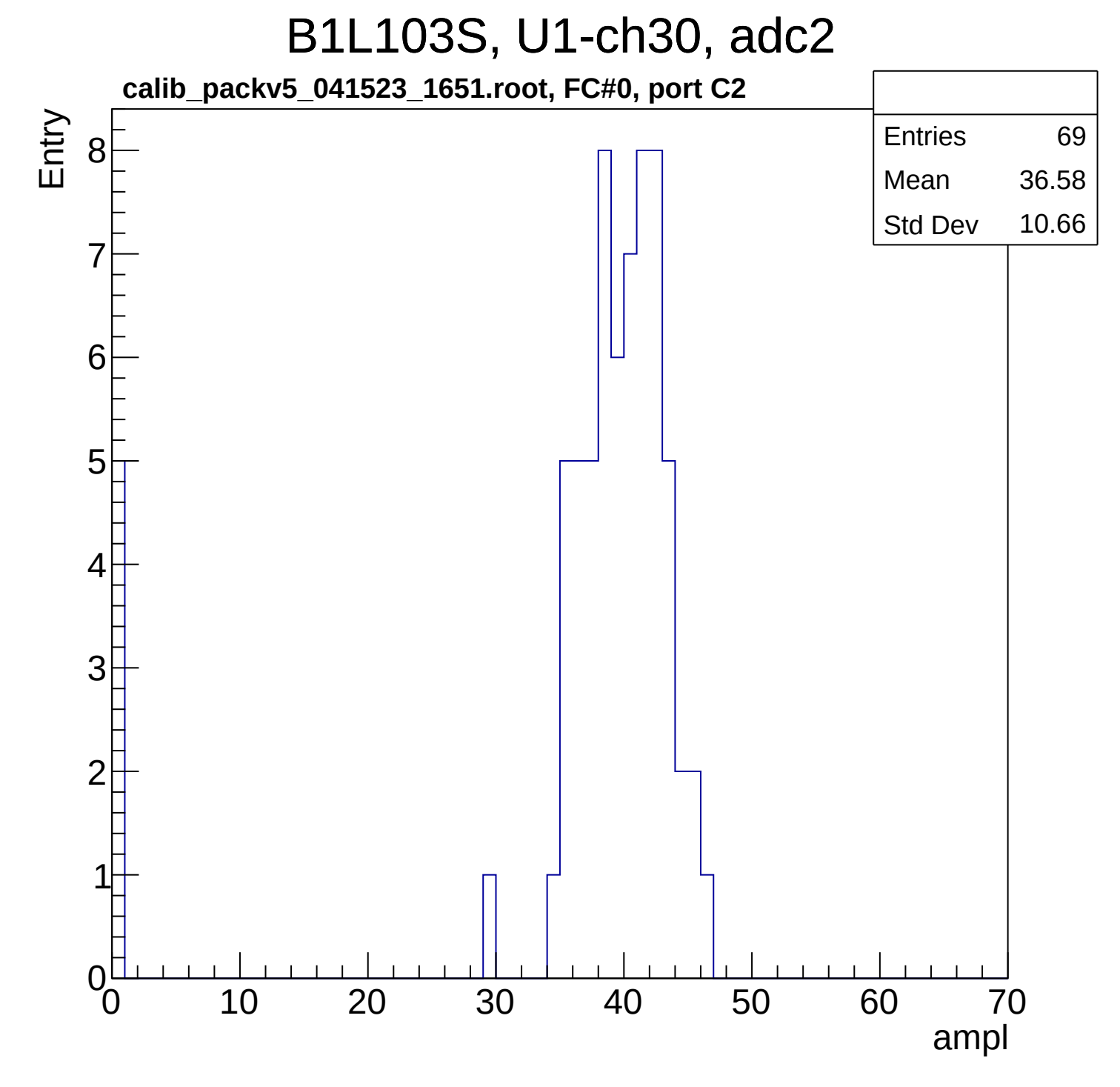
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70


B1L103S, U1-ch30, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 28.15
Std Dev 12.23
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch30, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 36.58
Std Dev 10.66
Entry
ampl
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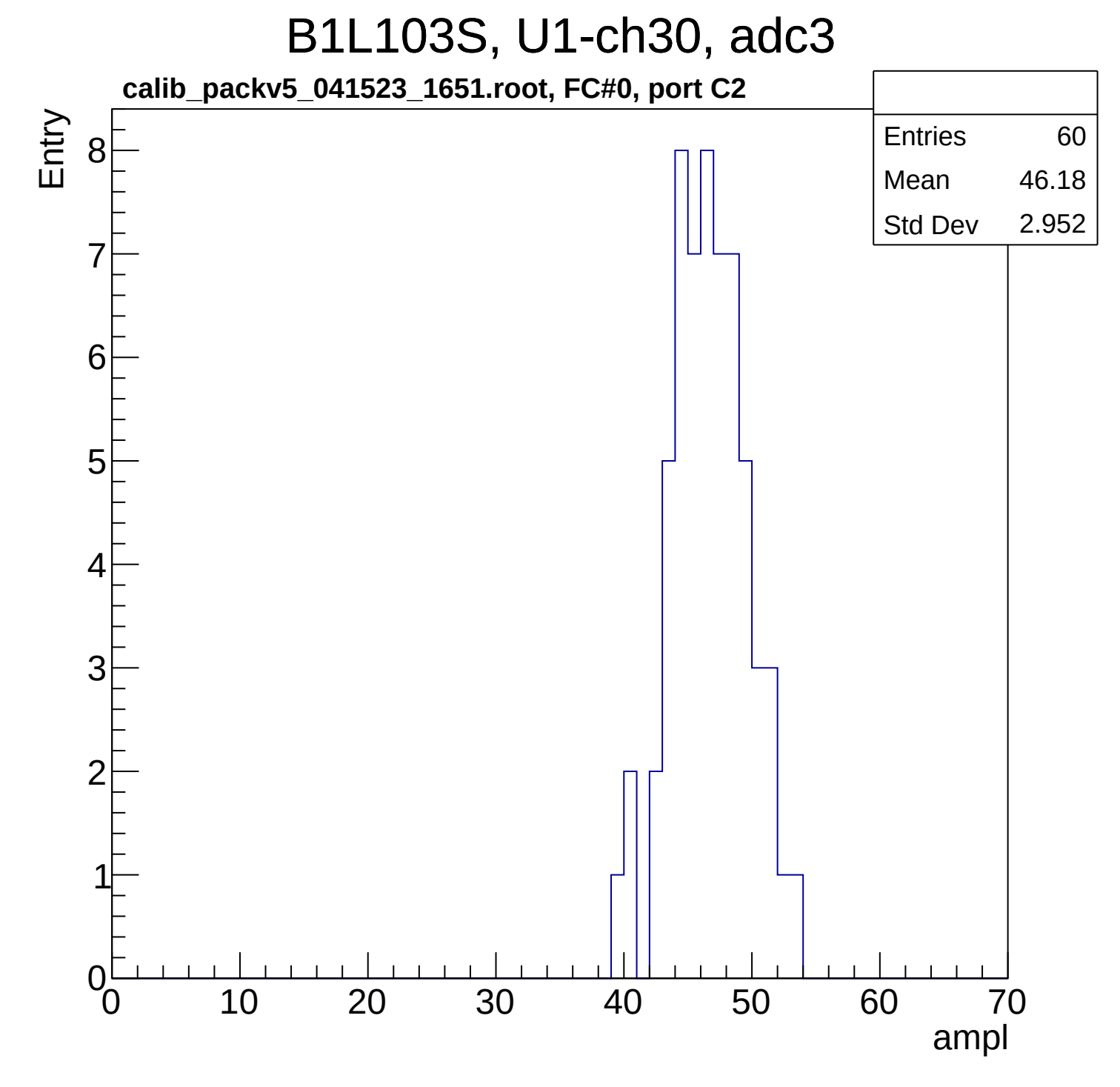
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U1-ch30, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 46.18
Std Dev 2.952
Entry
ampl
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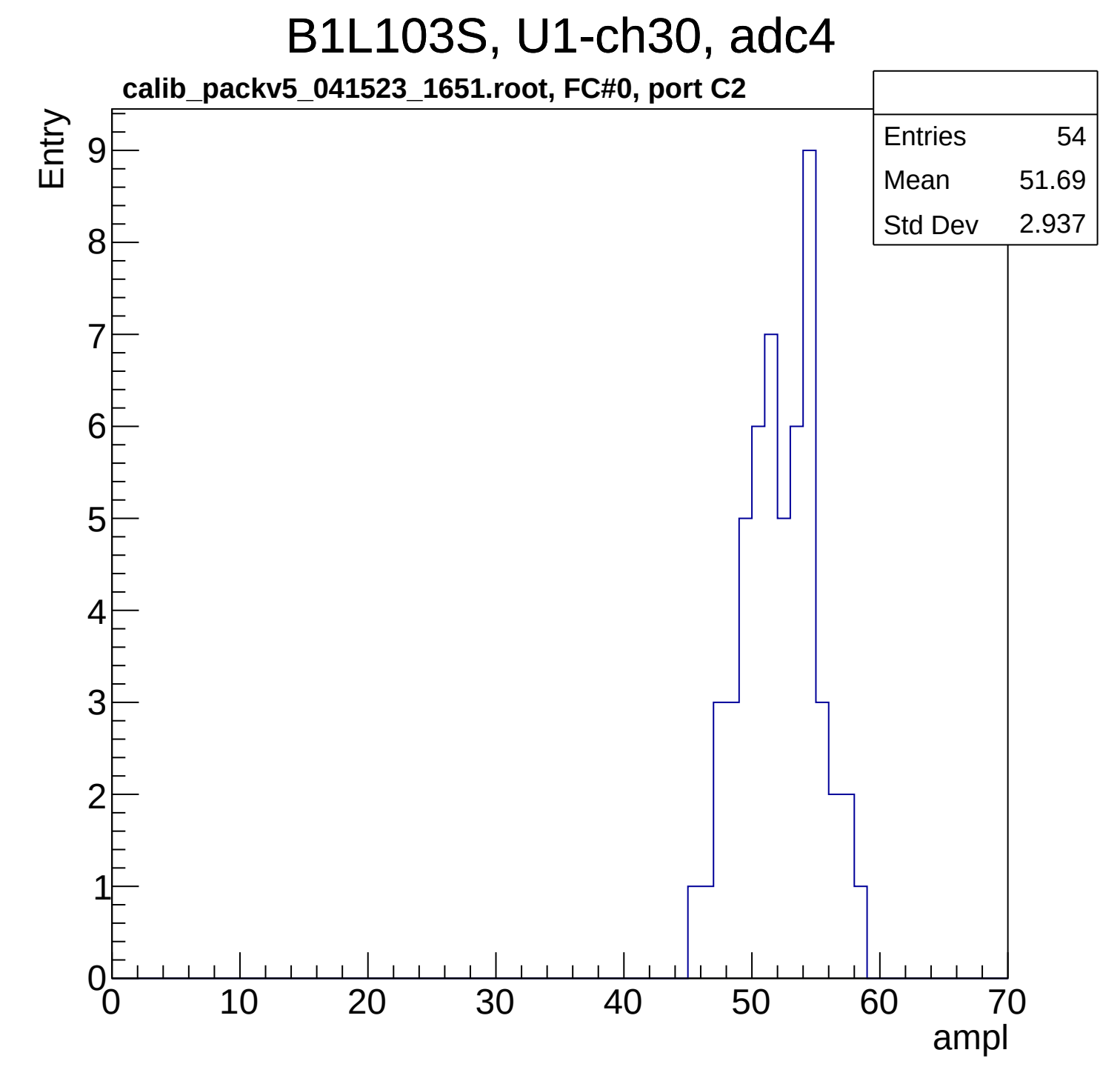
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U1-ch30, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 51.69
Std Dev 2.937
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
50
60
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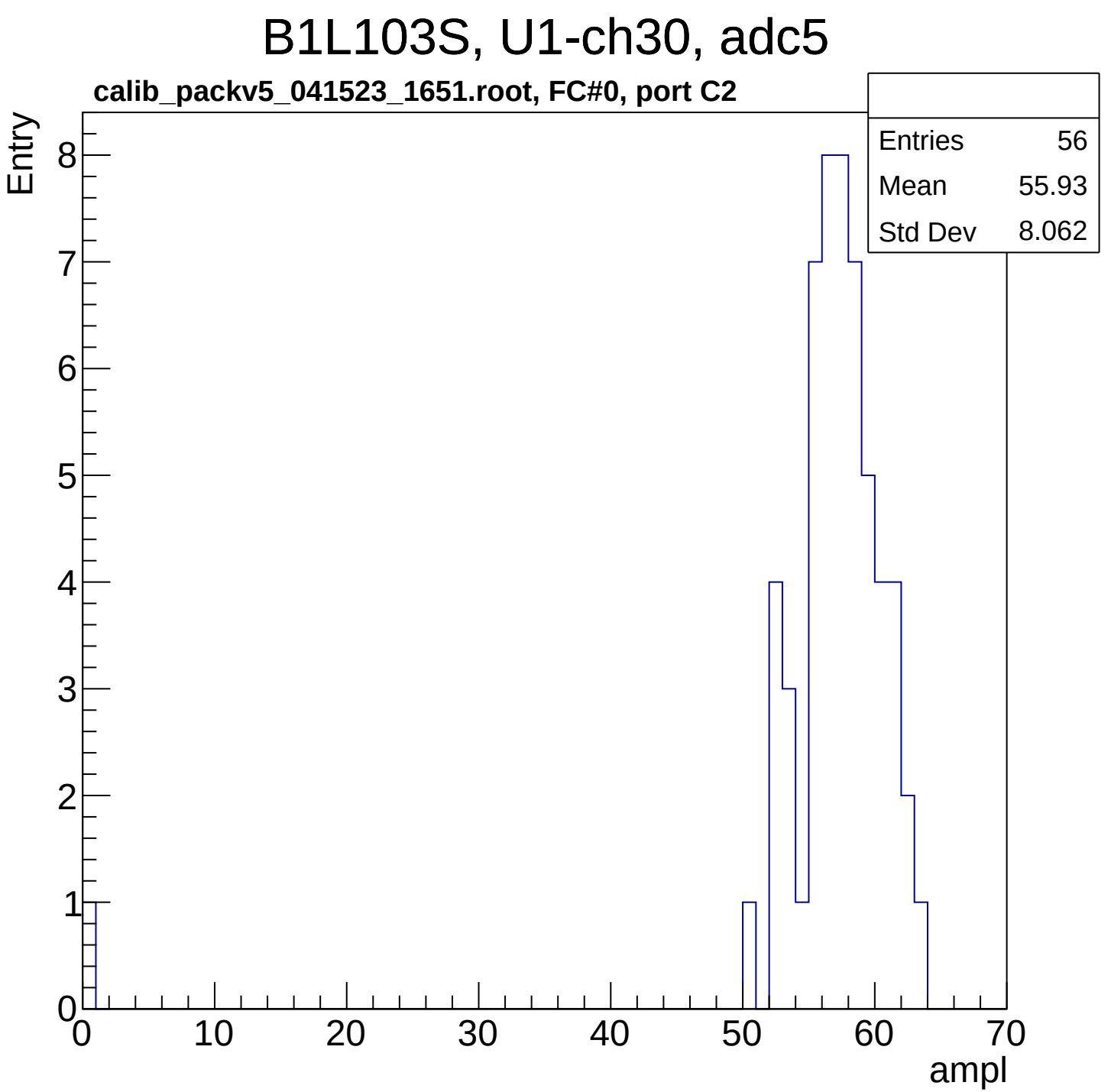
B1L103S, U1-ch30, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 55.93
Std Dev 8.062
Entry
ampl
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2
3
4
5
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7
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0
10
20
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40
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60
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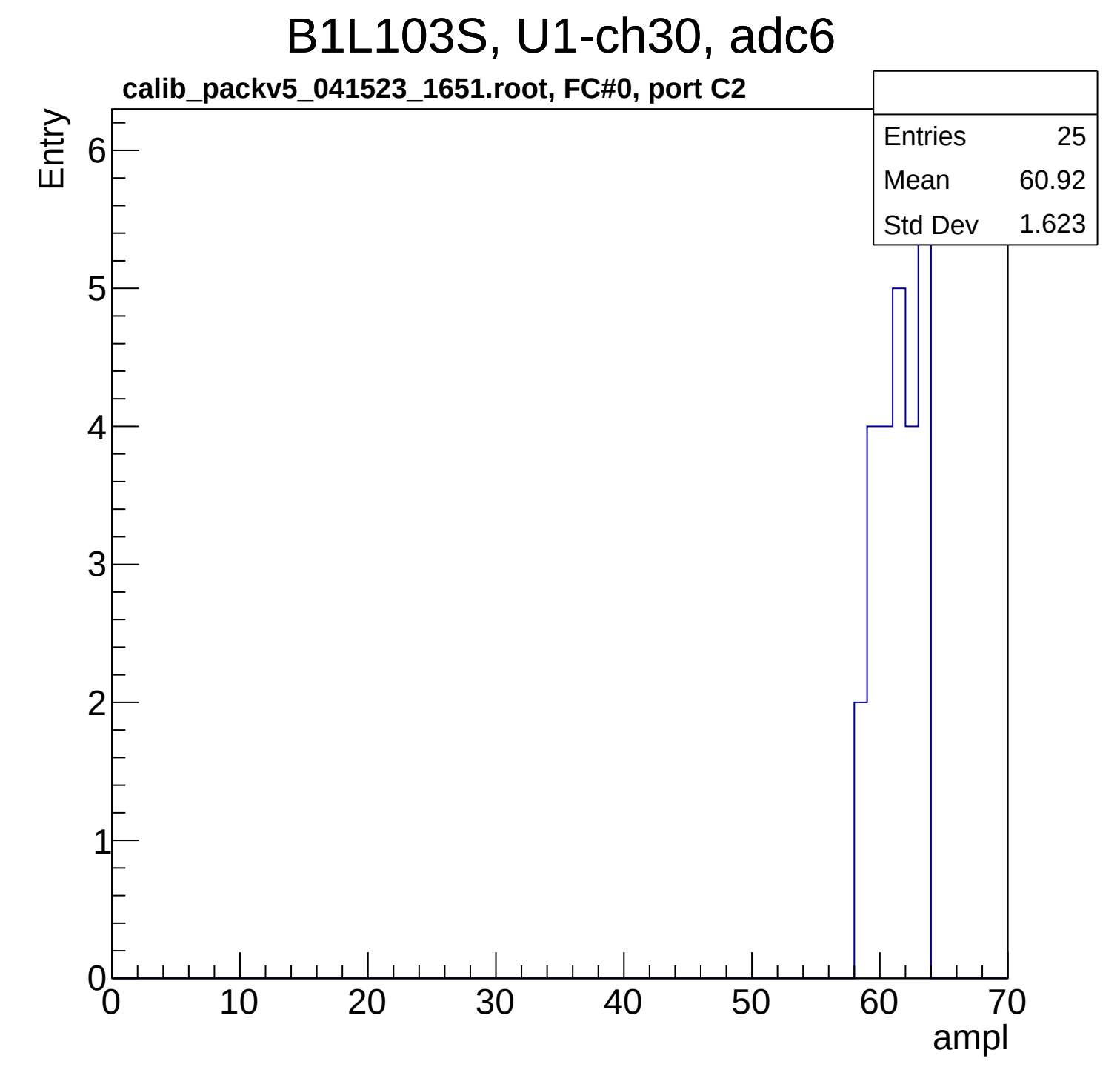
B1L103S, U1-ch30, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 25
Mean 60.92
Std Dev 1.623
Entry
ampl
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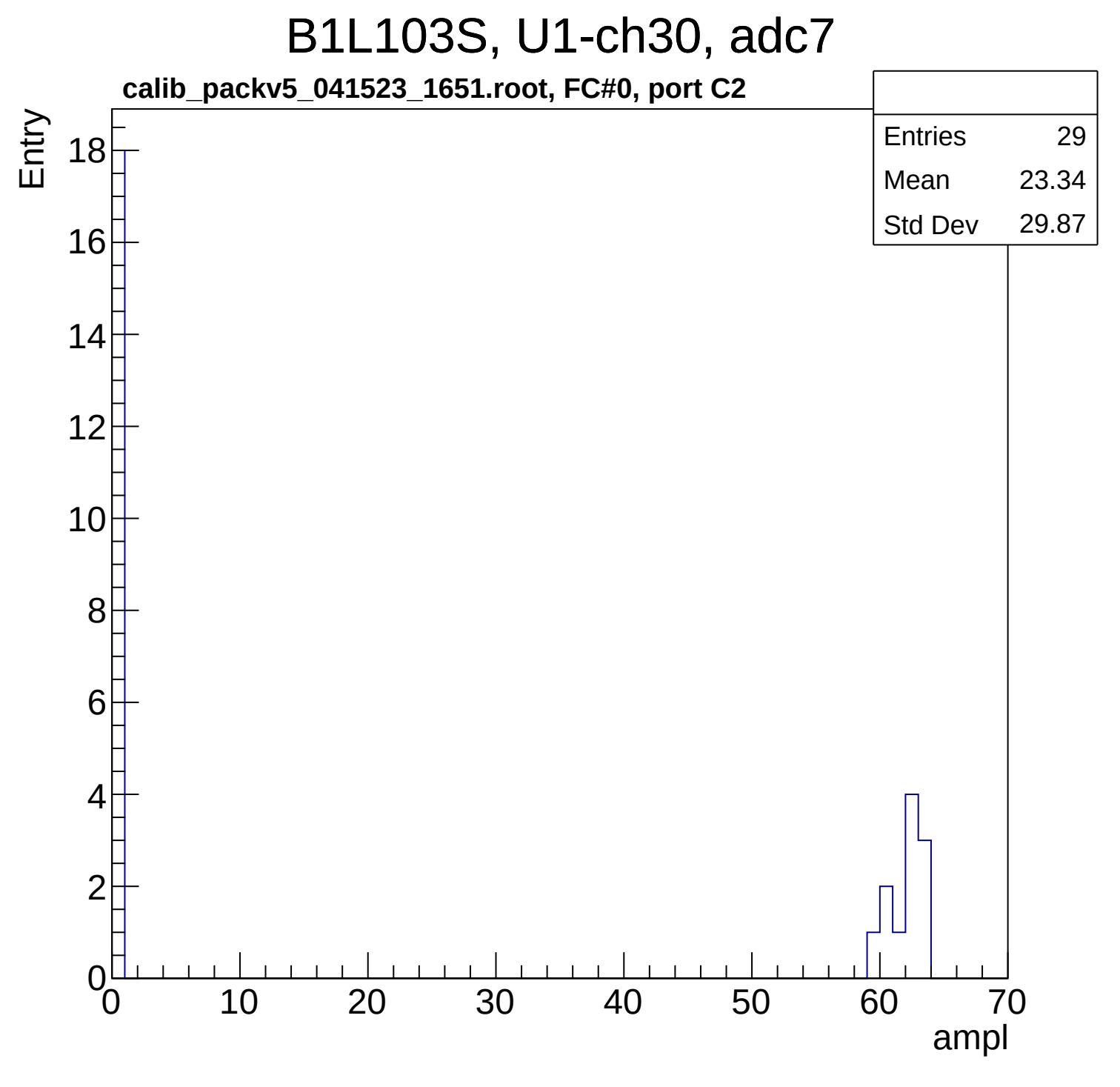
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U1-ch30, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 29
Mean 23.34
Std Dev 29.87
Entry
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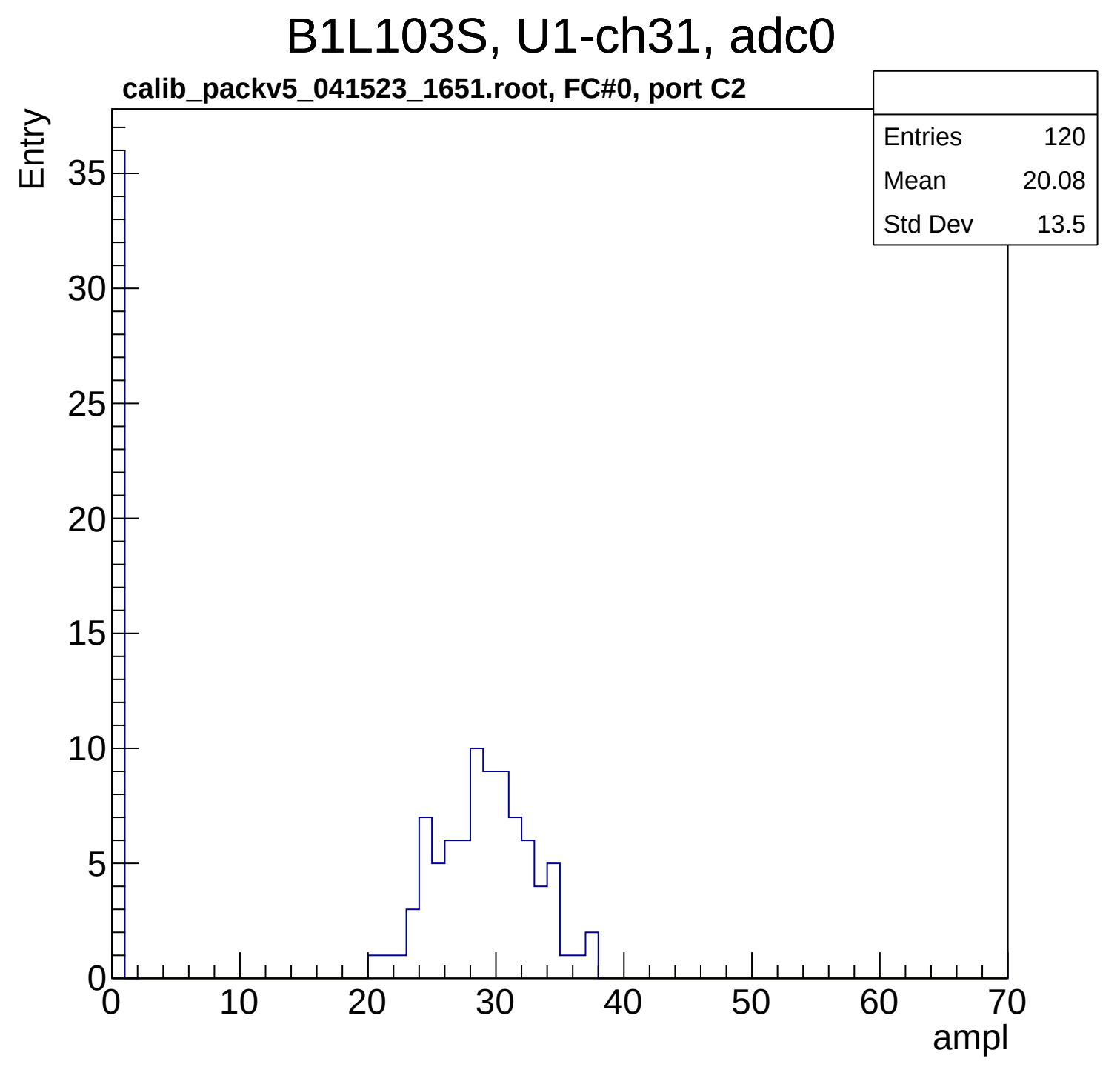
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch31, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 120
Mean 20.08
Std Dev 13.5
Entry
ampl
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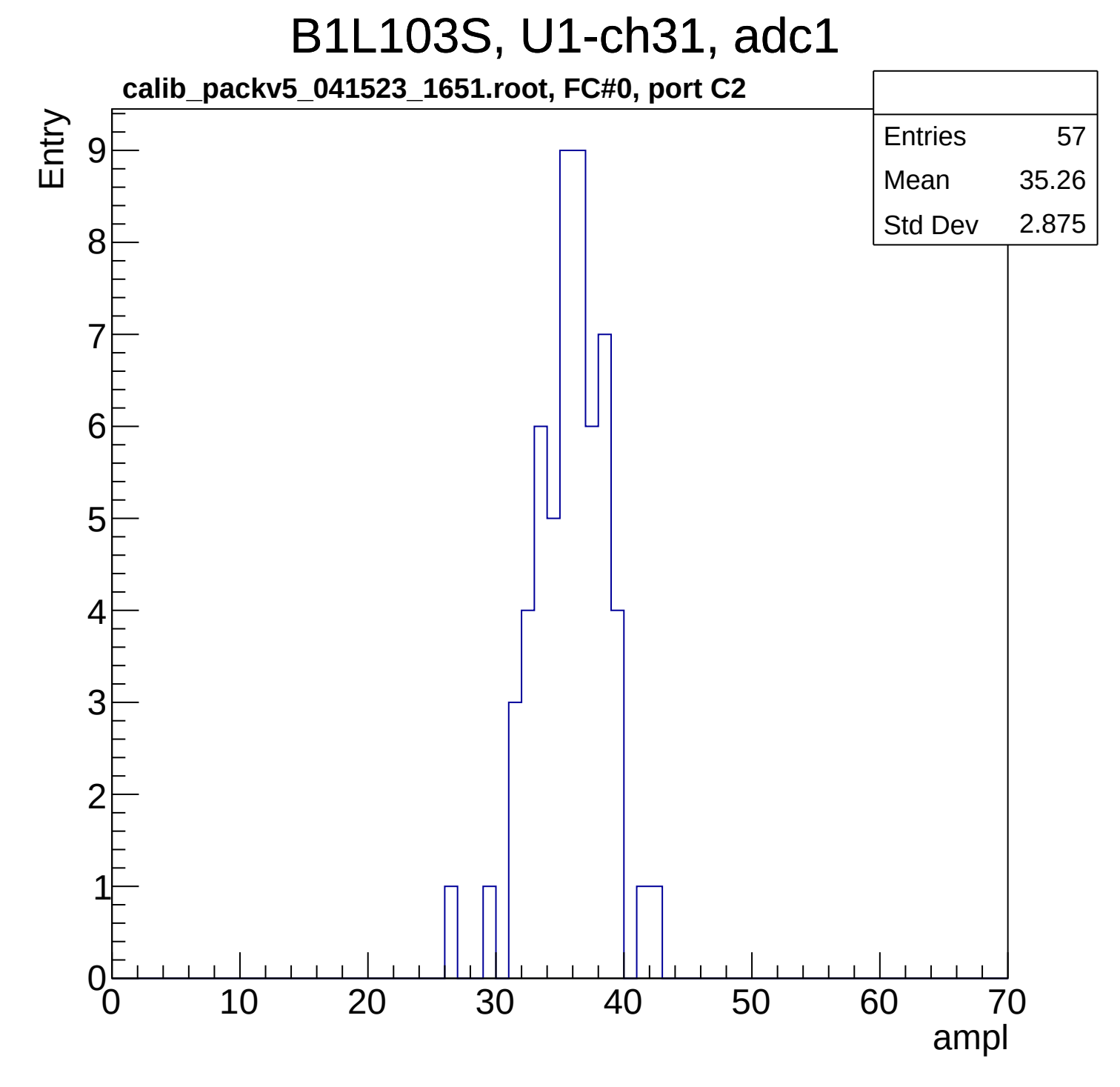
5
10
15
20
25
30
35
0
10
20
30
40
50
60
70


B1L103S, U1-ch31, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 35.26
Std Dev 2.875
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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60
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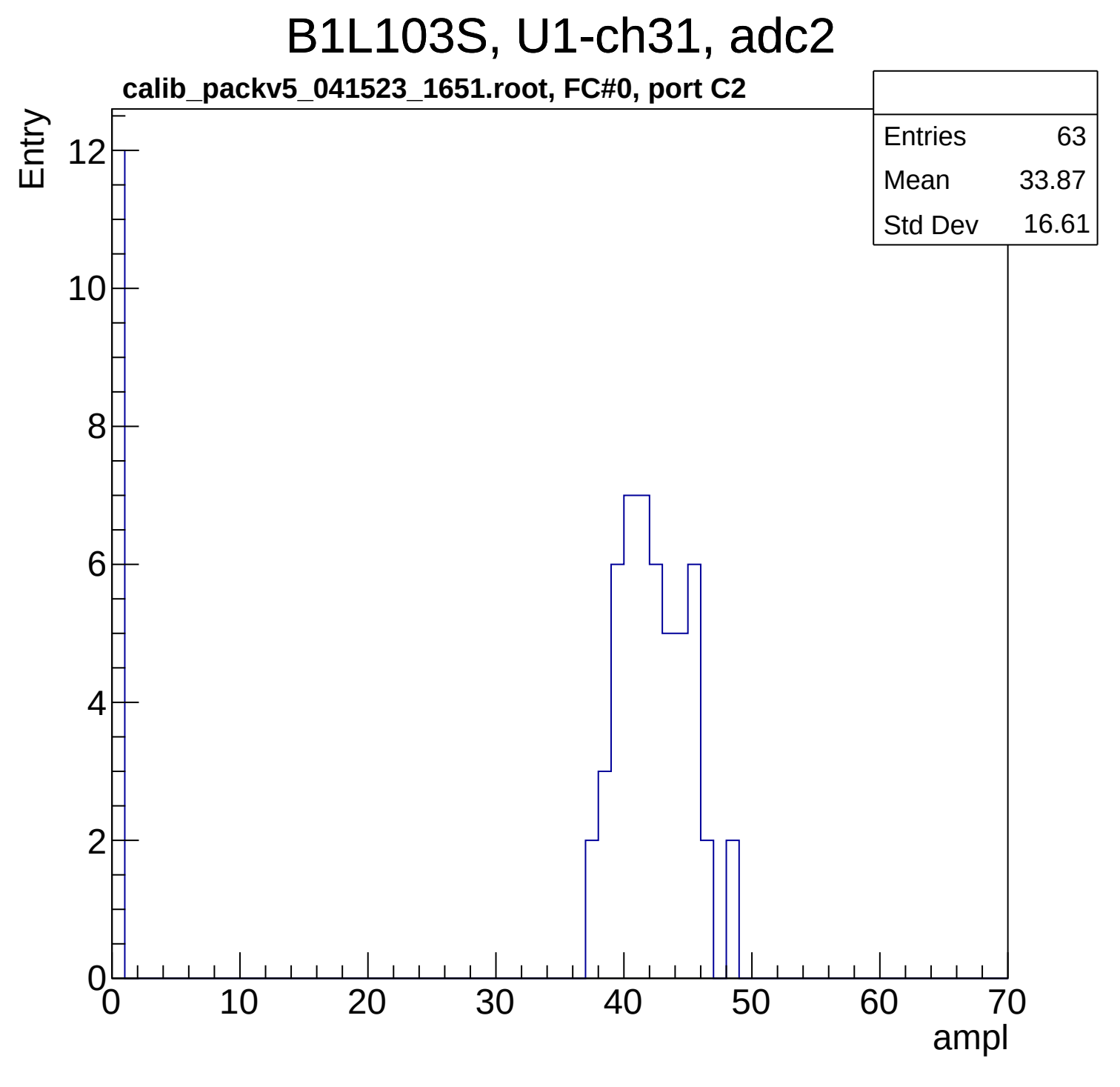
B1L103S, U1-ch31, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 33.87
Std Dev 16.61
Entry
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4
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10
12
0
10
20
30
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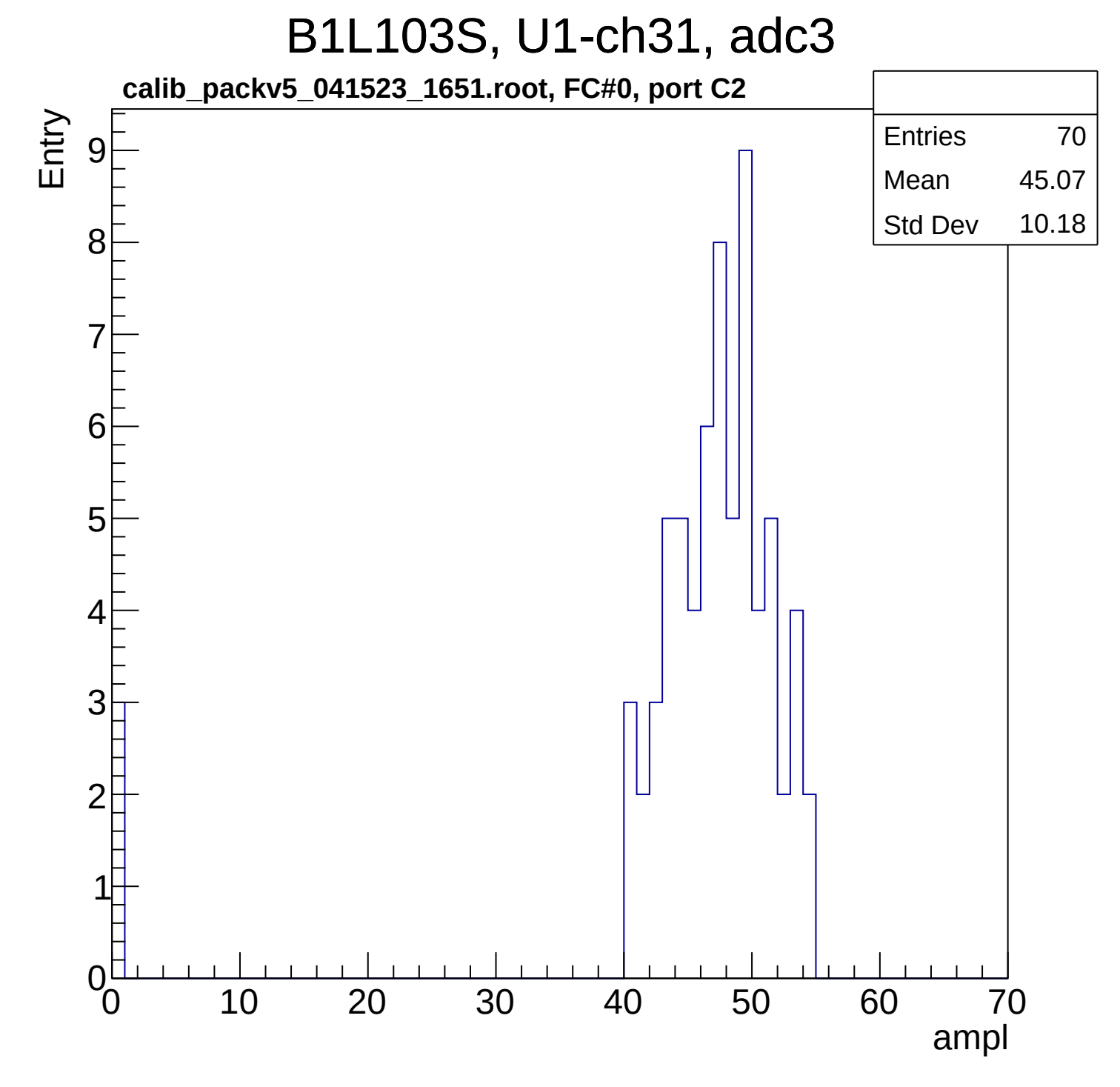
50
60
70
ampl


B1L103S, U1-ch31, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 45.07
Std Dev 10.18
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
50
60
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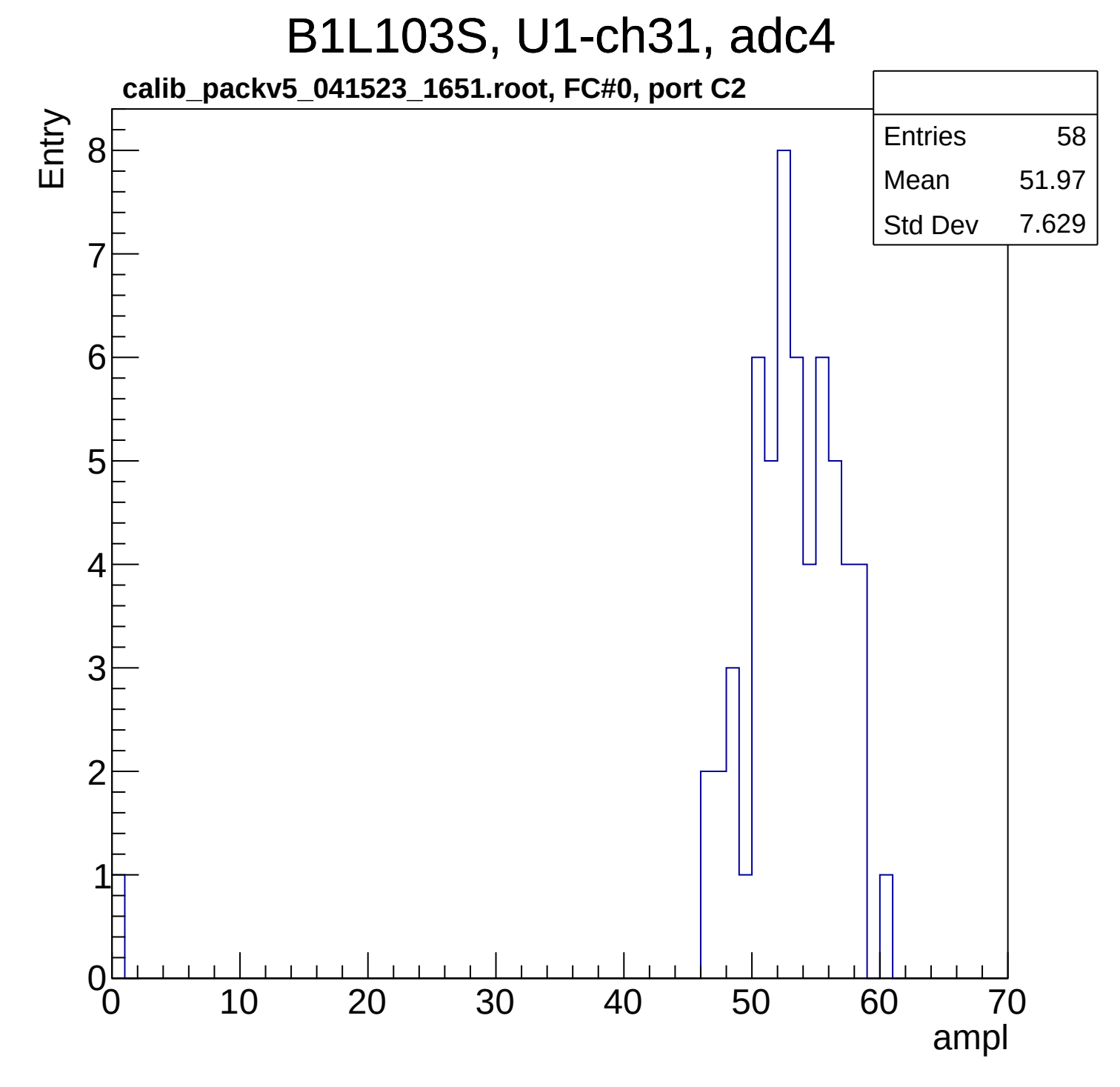
B1L103S, U1-ch31, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 51.97
Std Dev 7.629
Entry
ampl
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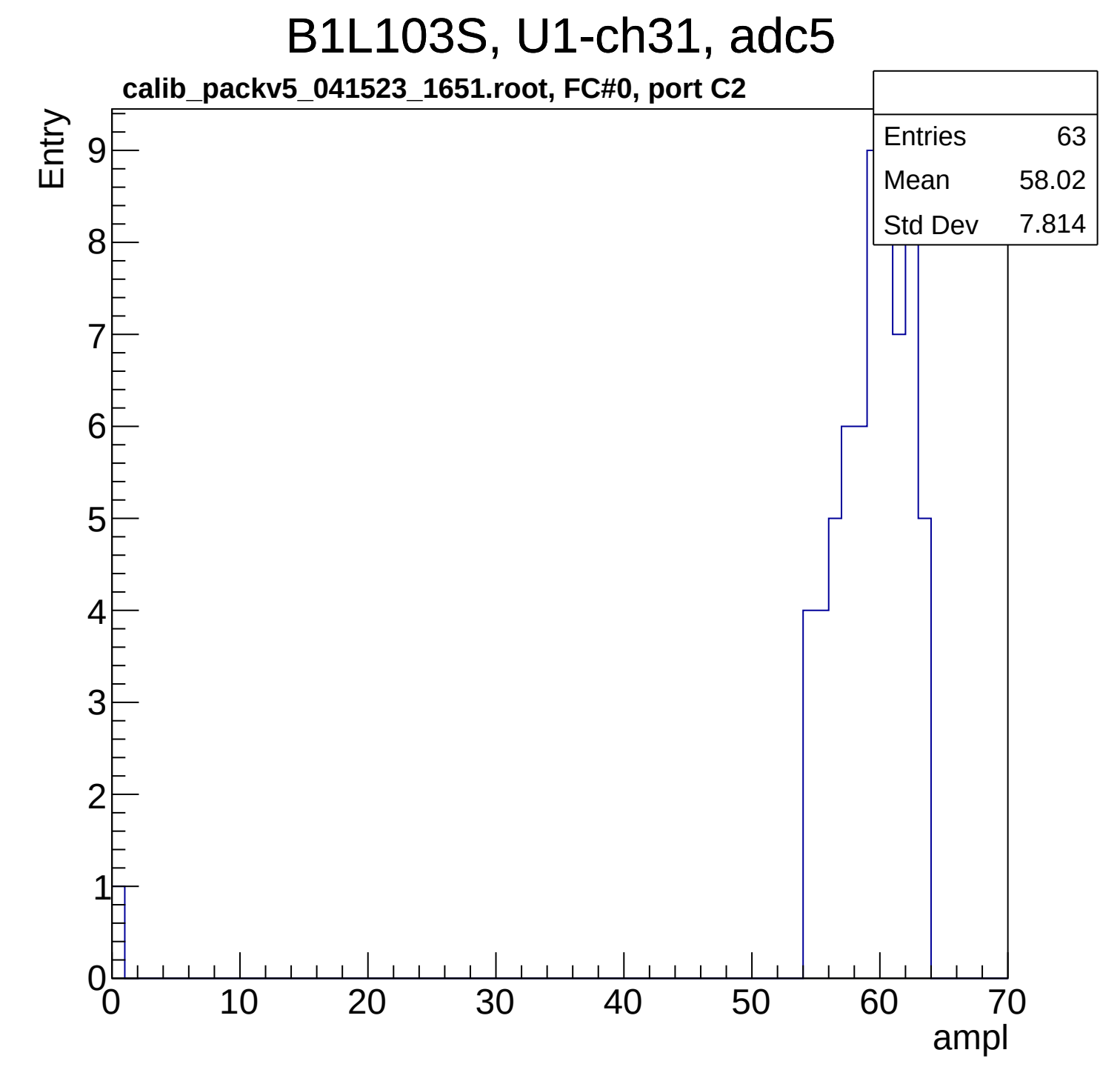
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U1-ch31, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 58.02
Std Dev 7.814
Entry
ampl
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3
4
5
6
7
8
9
0
10
20
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50
60
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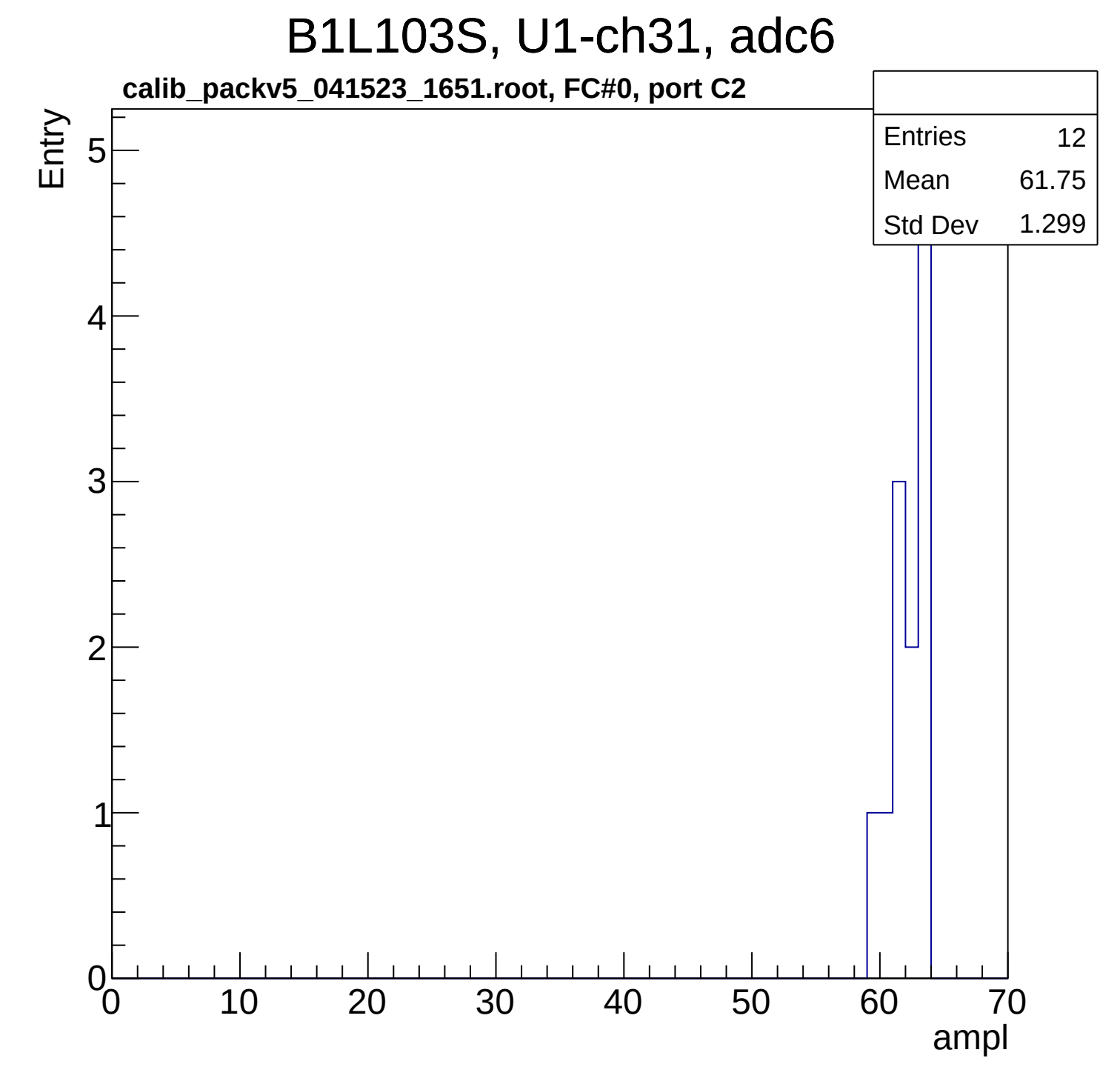
B1L103S, U1-ch31, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 61.75
Std Dev 1.299
Entry
ampl
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2
3
4
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0
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20
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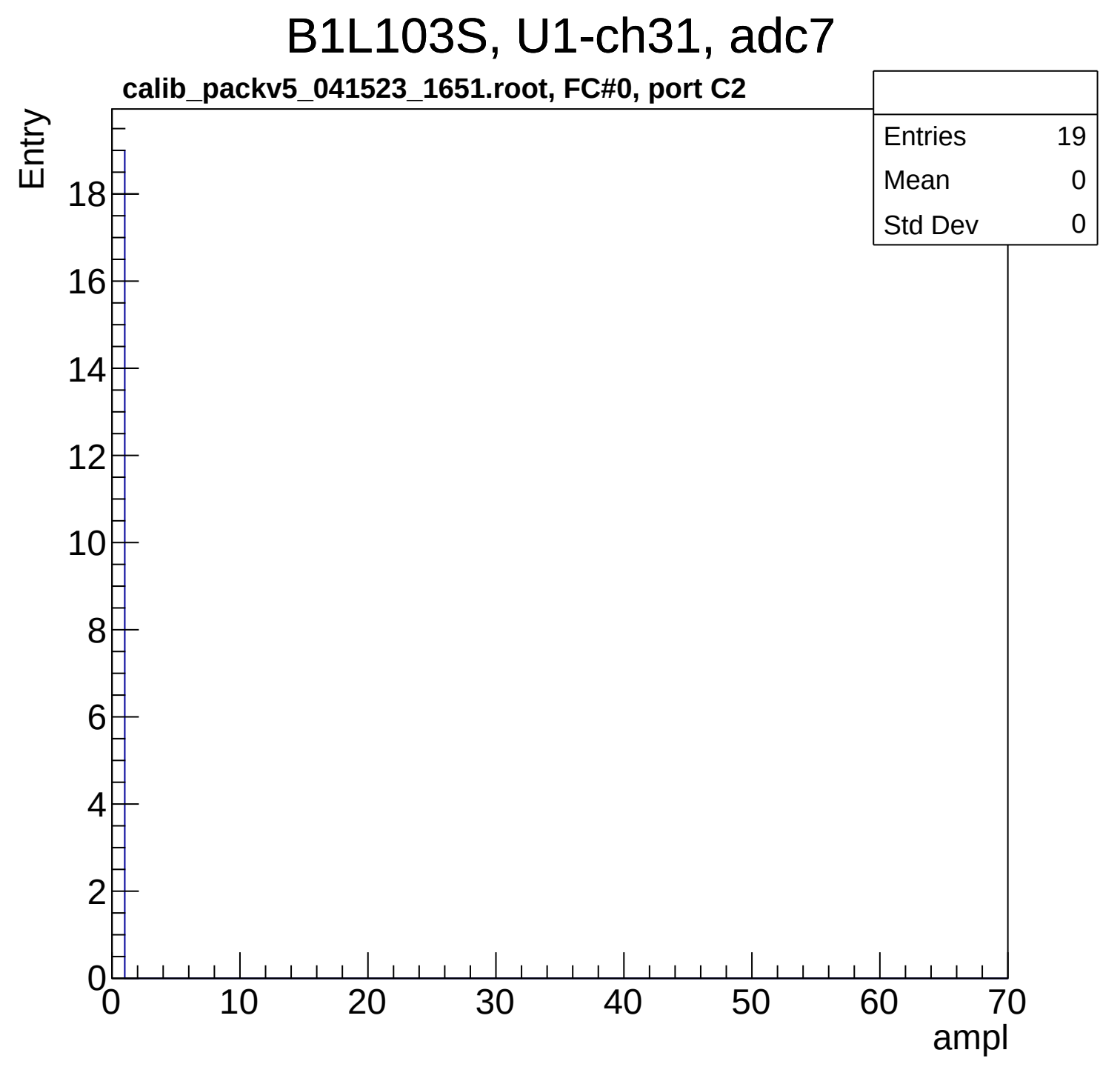
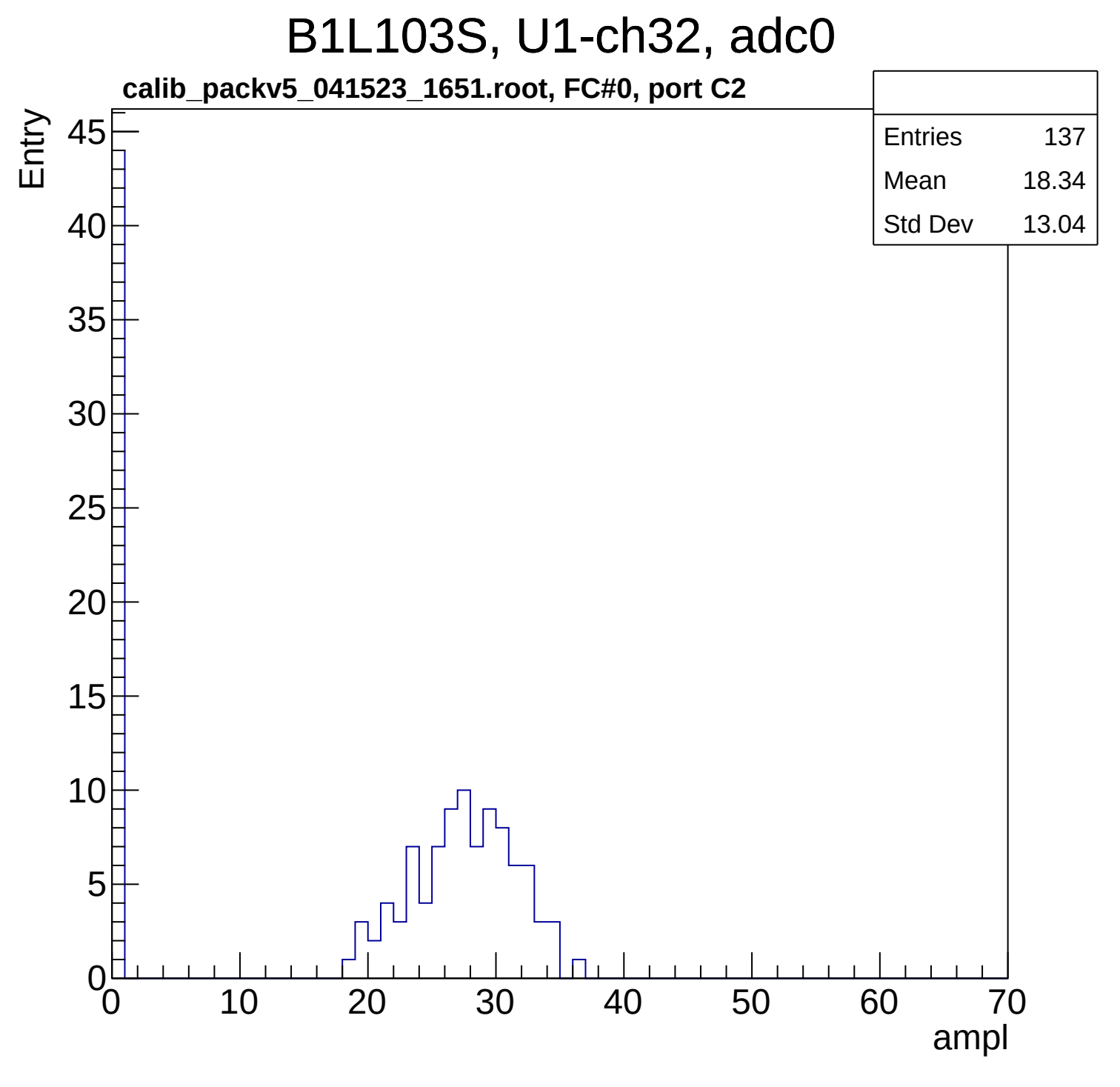
40
50
60
70


B1L103S, U1-ch31, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch32, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 137
Mean 18.34
Std Dev 13.04
Entry
ampl
0
5
10
15
20
25
30
35
40
45
0
10
20
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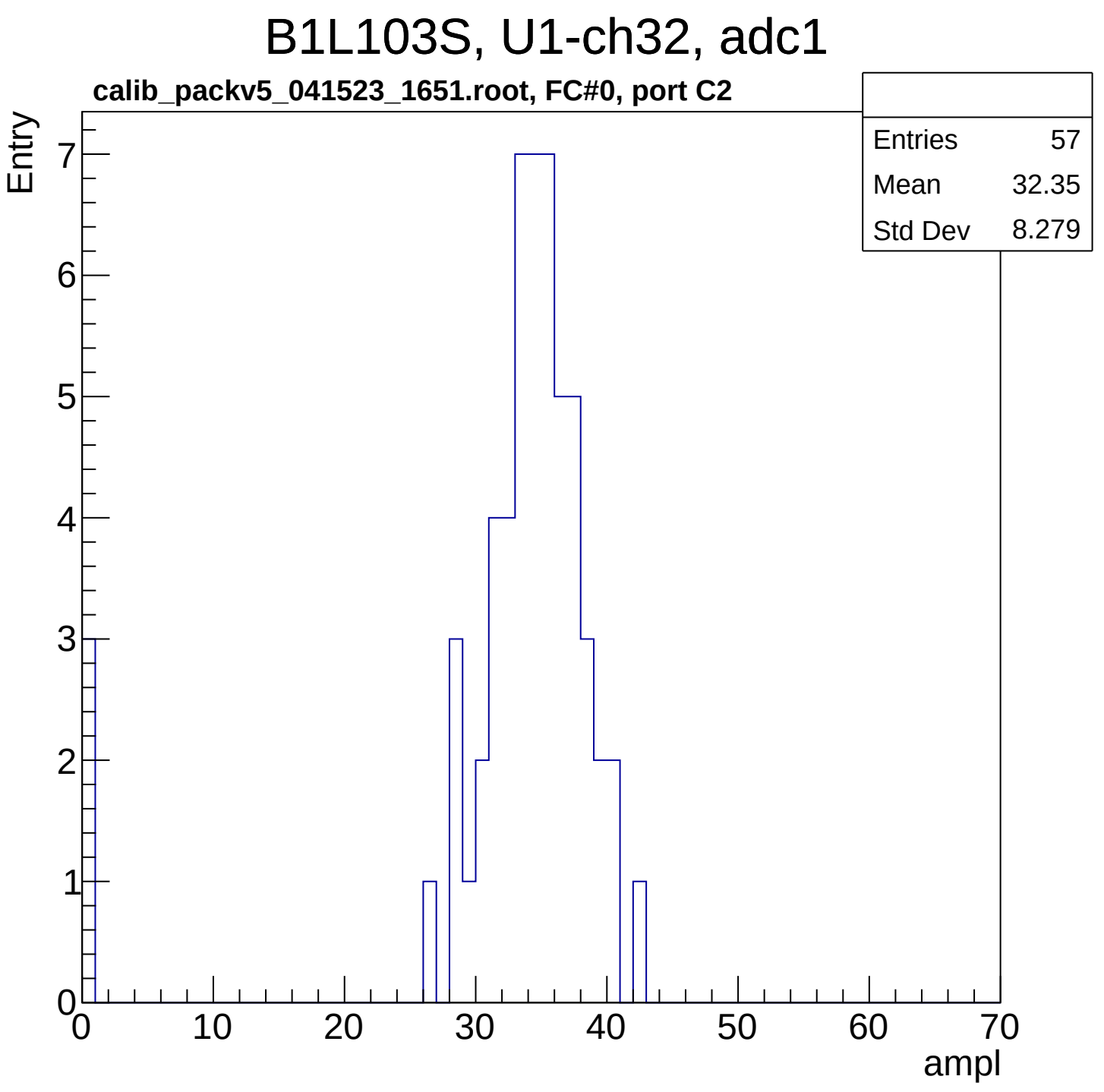
40
50
60
70


B1L103S, U1-ch32, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 32.35
Std Dev 8.279
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
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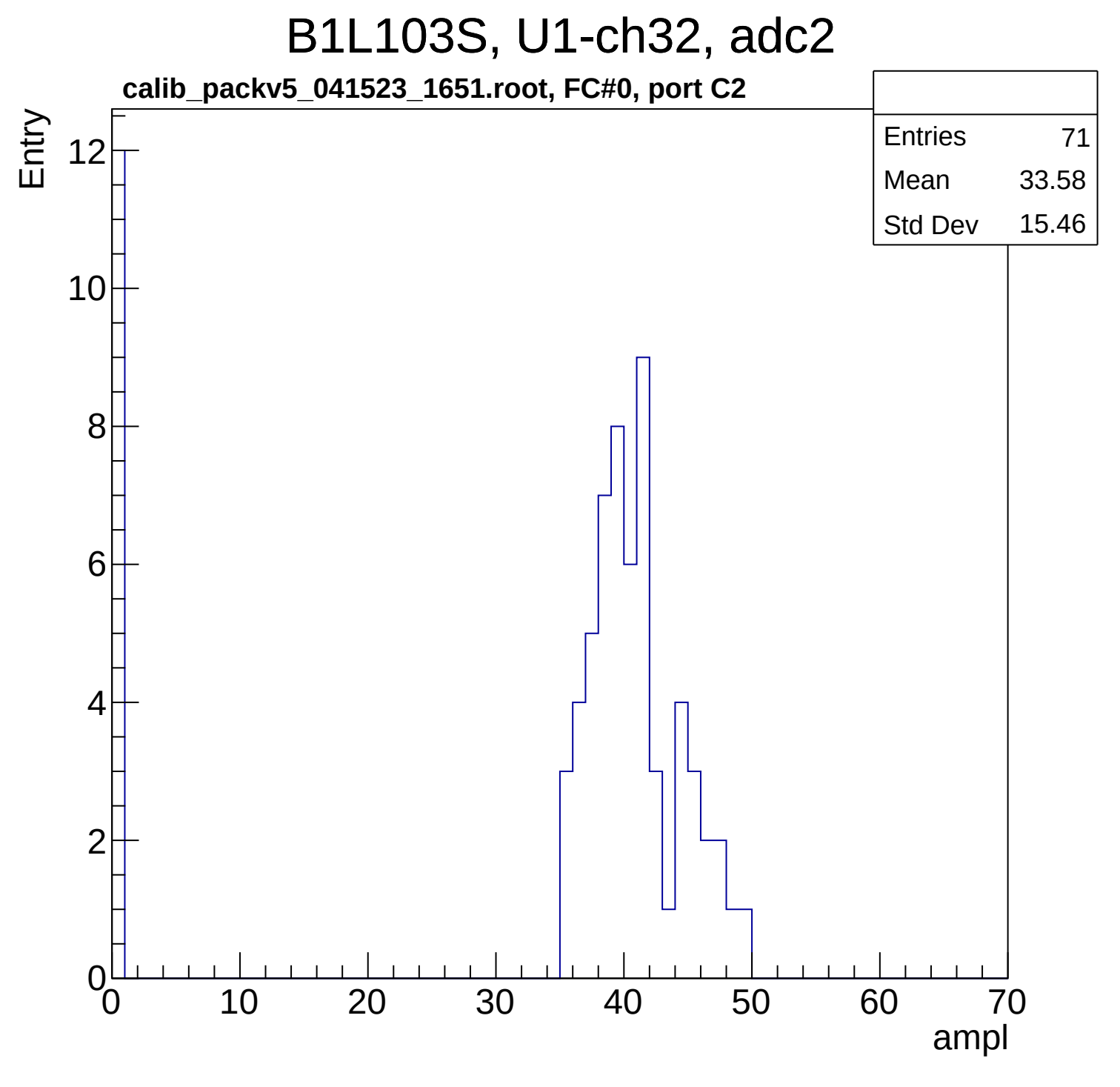
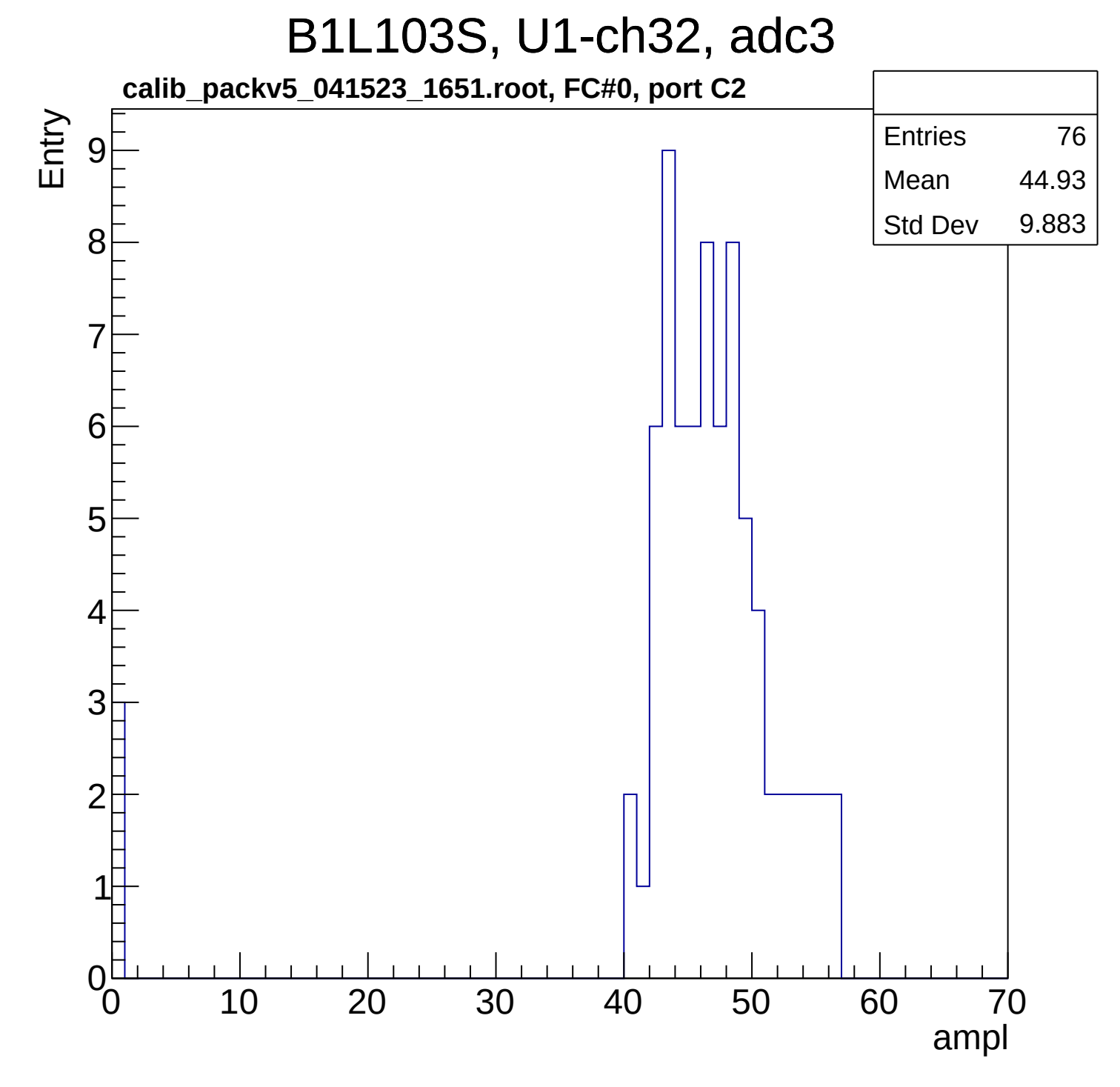
40
50
60
70


B1L103S, U1-ch32, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 33.58
Std Dev 15.46
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch32, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 44.93
Std Dev 9.883
Entry
ampl
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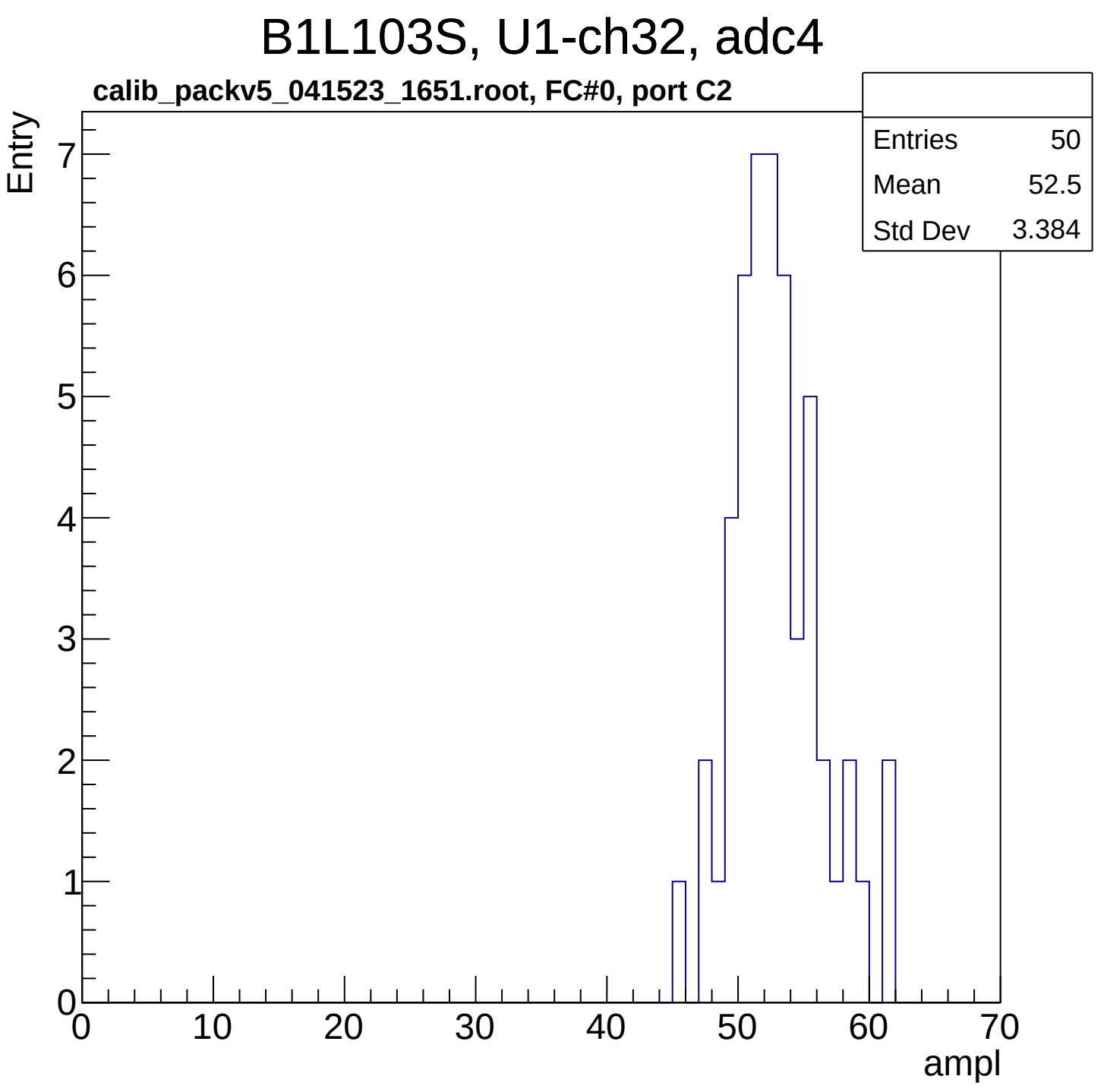
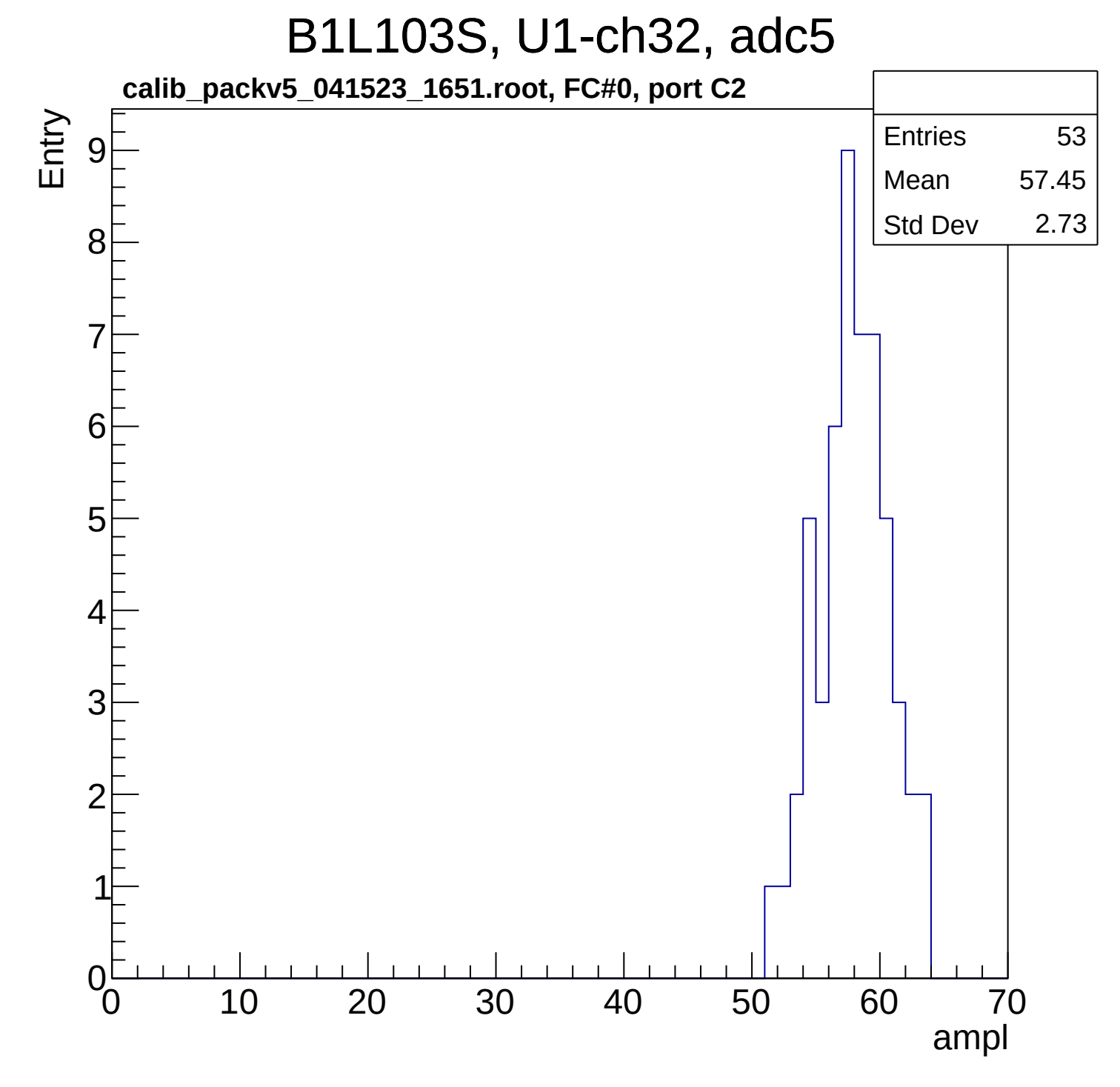
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U1-ch32, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 52.5
Std Dev 3.384
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U1-ch32, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 57.45
Std Dev 2.73
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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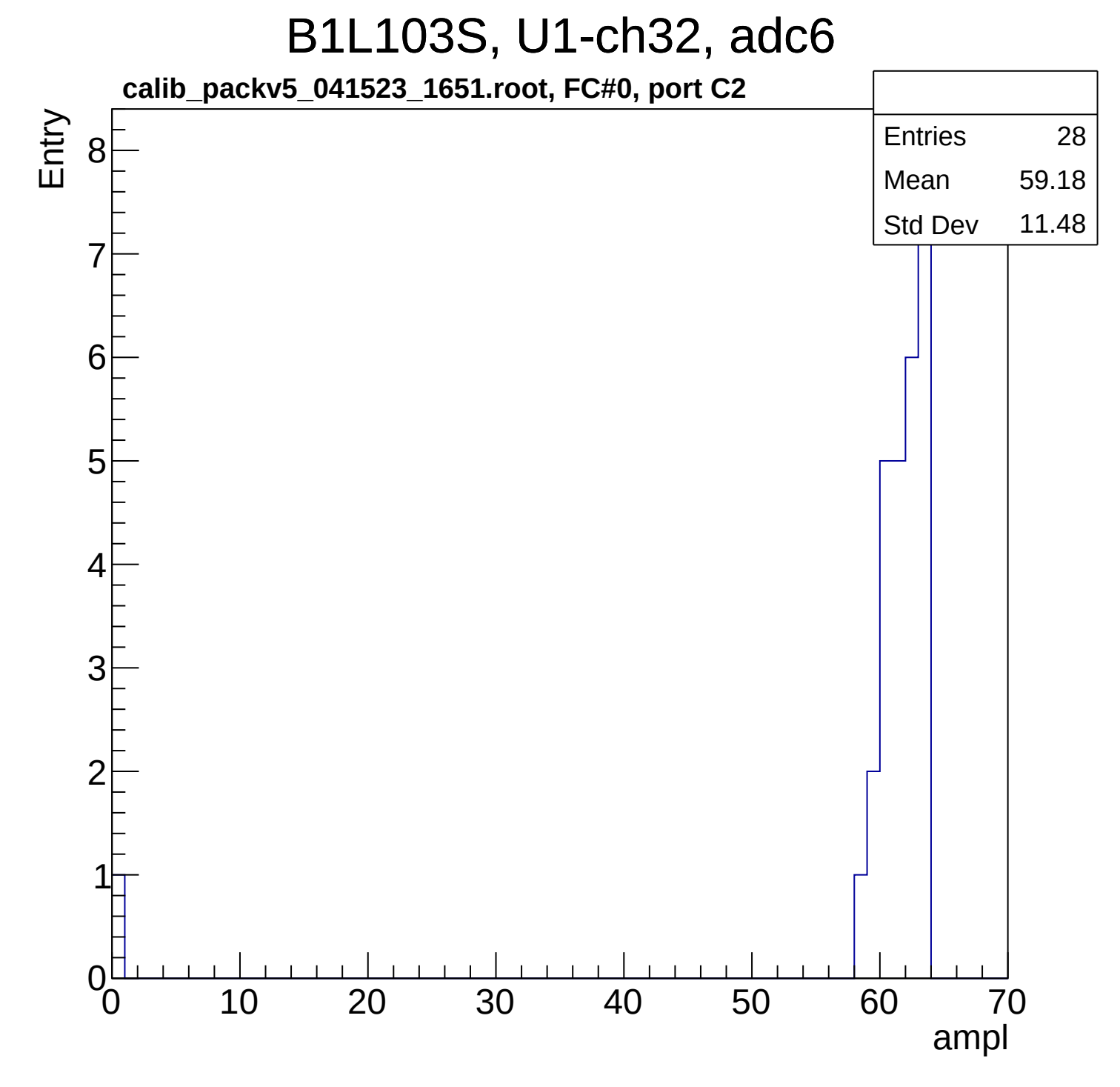
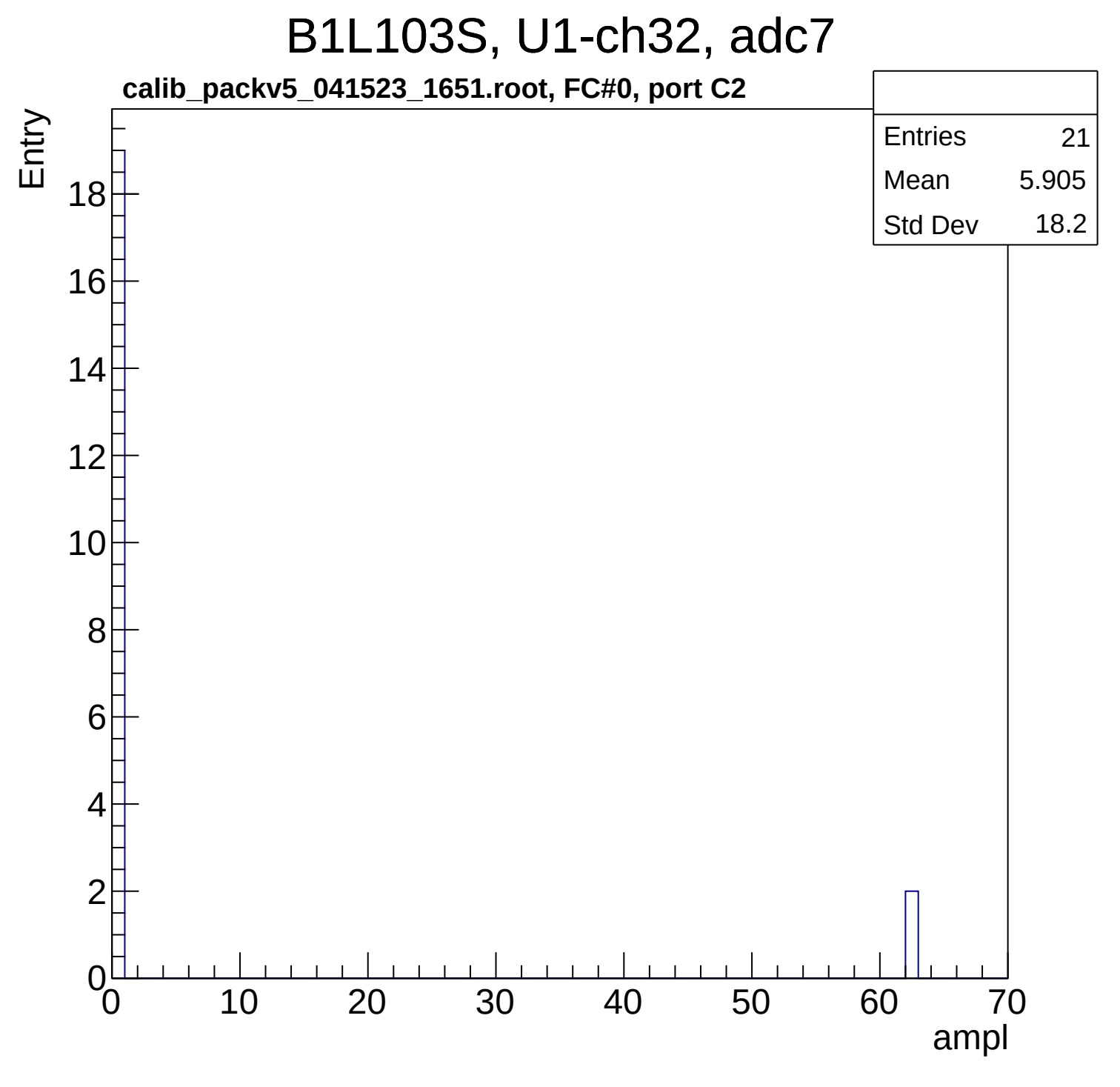
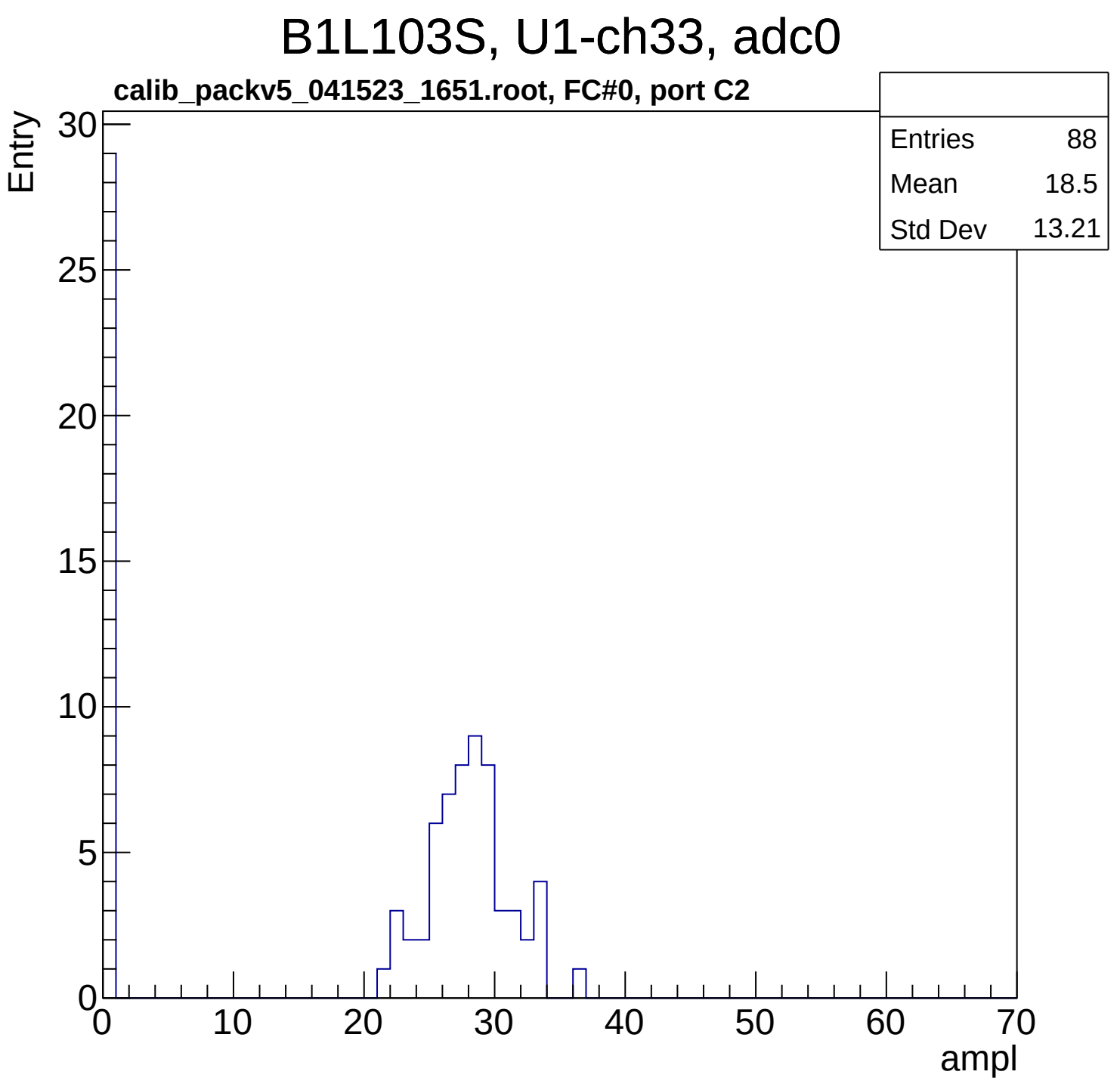
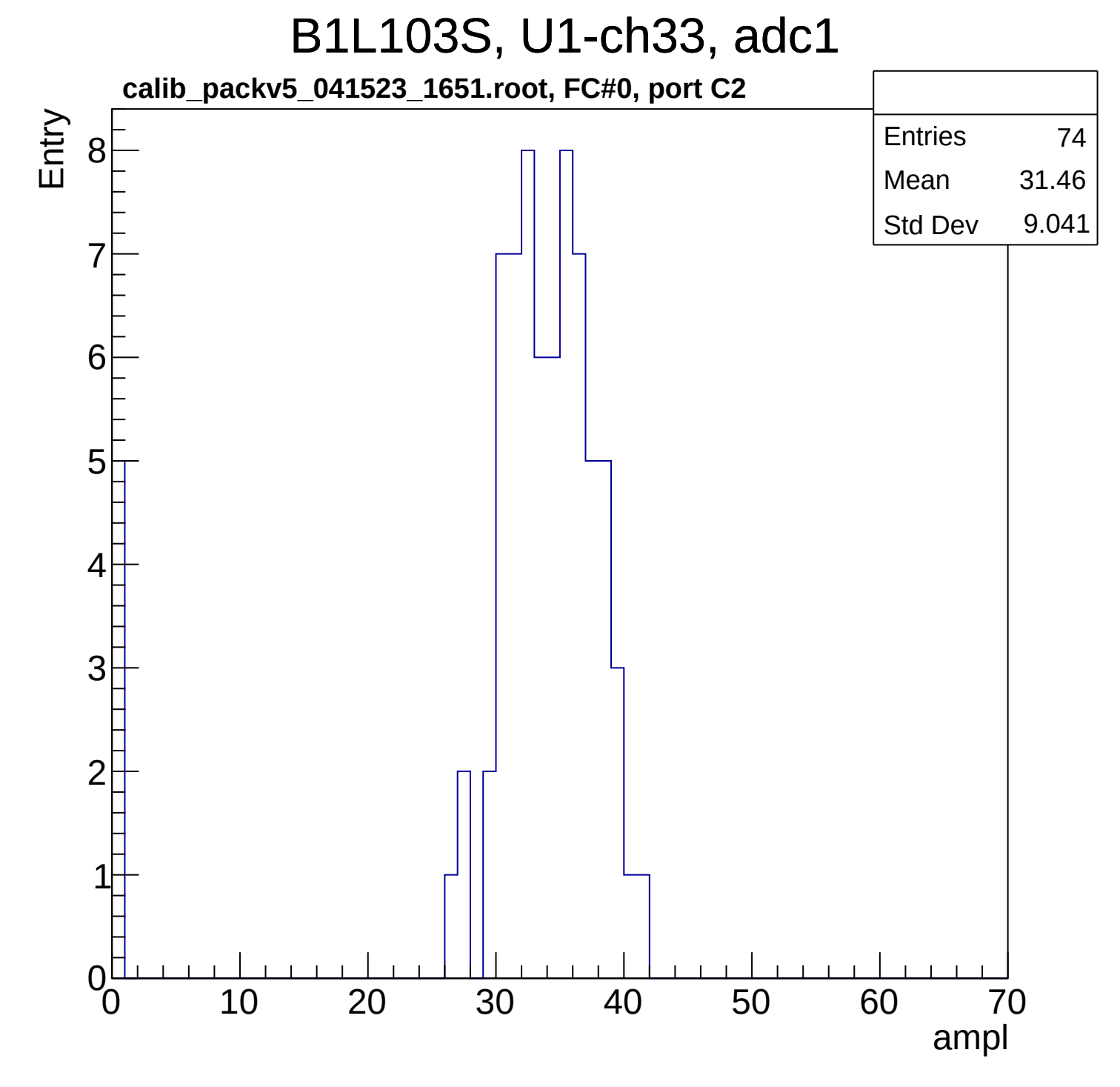
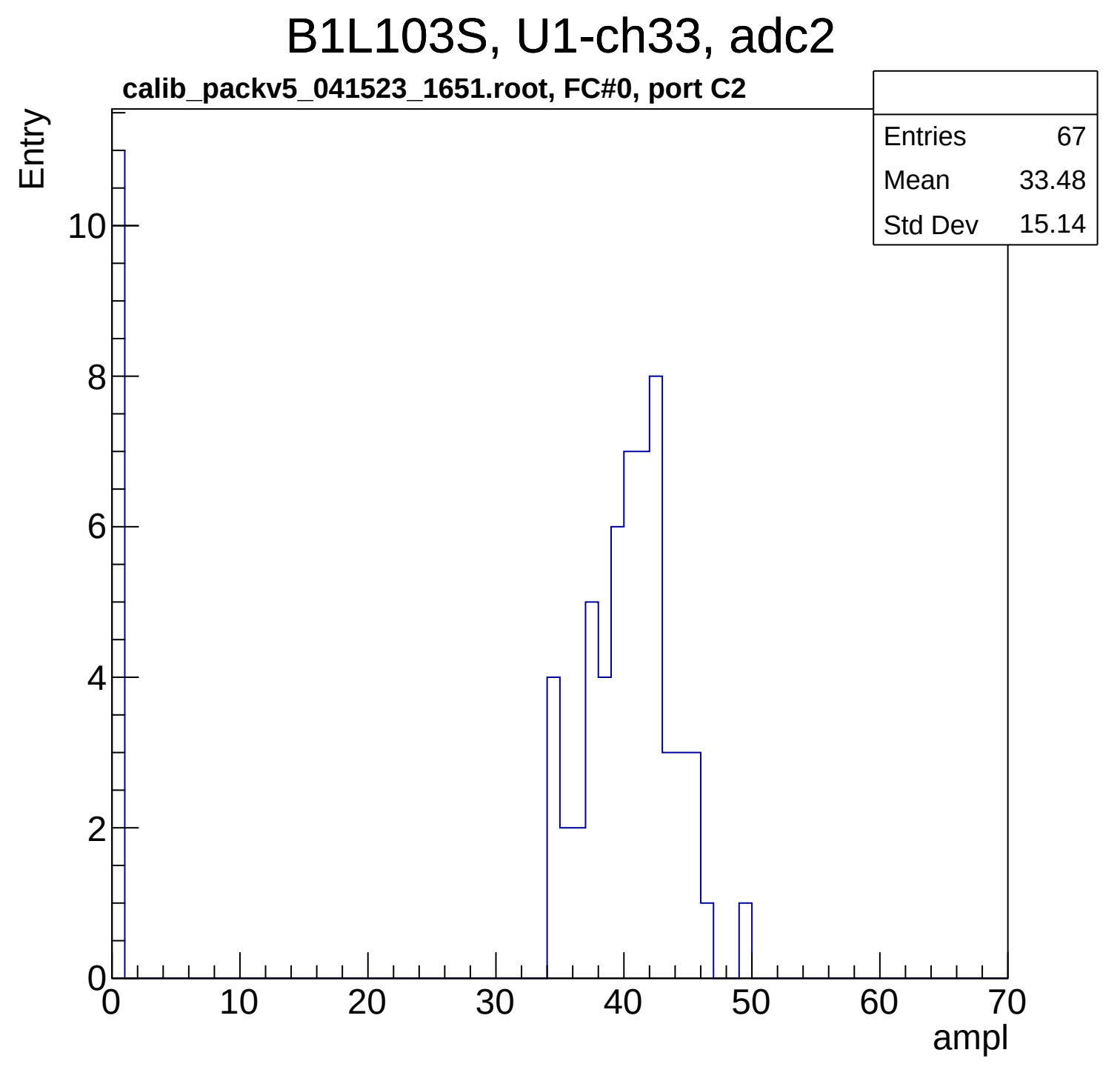
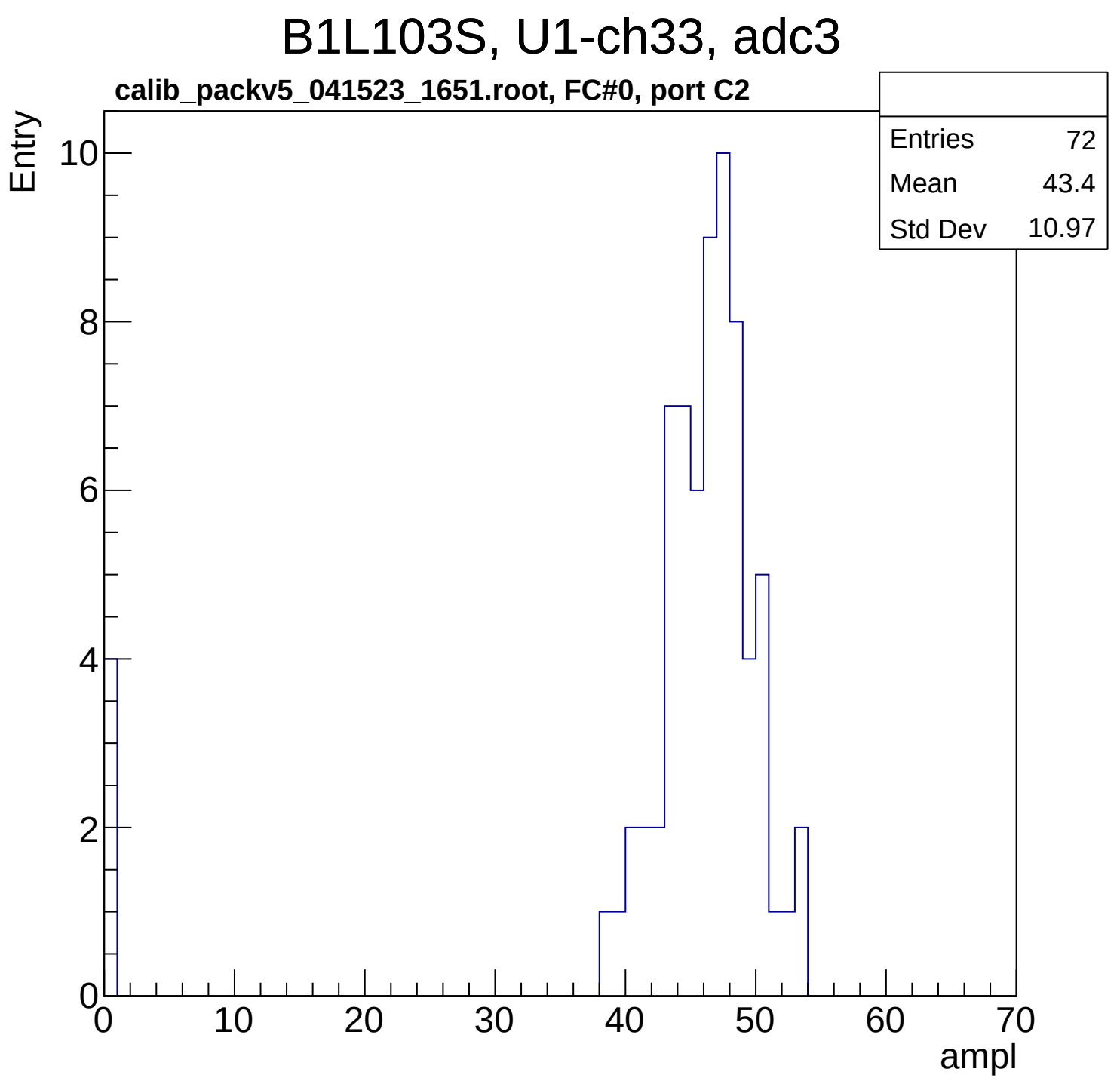

B1L103S, U1-ch32, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 28
Mean 59.18
Std Dev 11.48
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

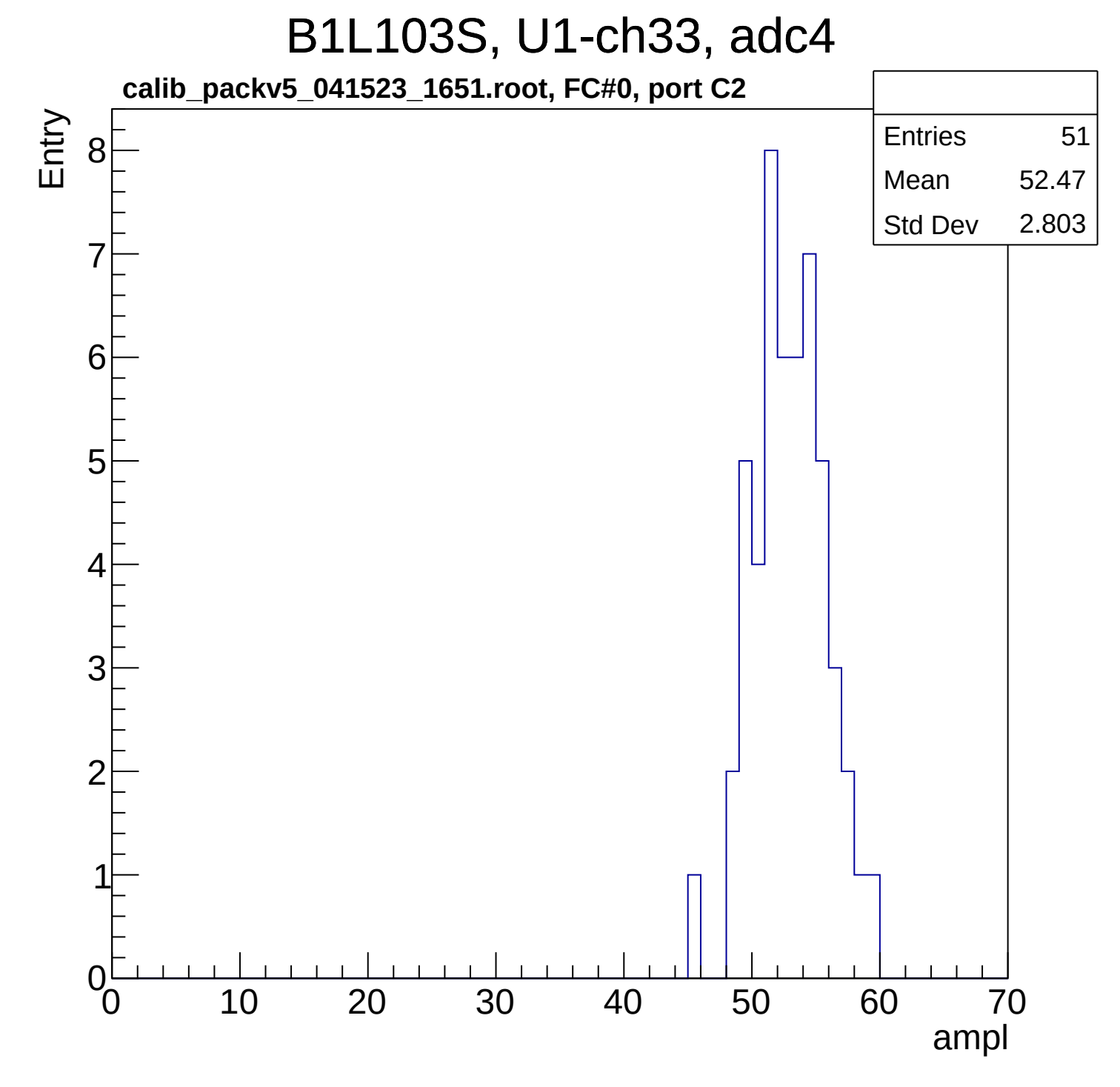

B1L103S, U1-ch32, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 5.905
Std Dev 18.2
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

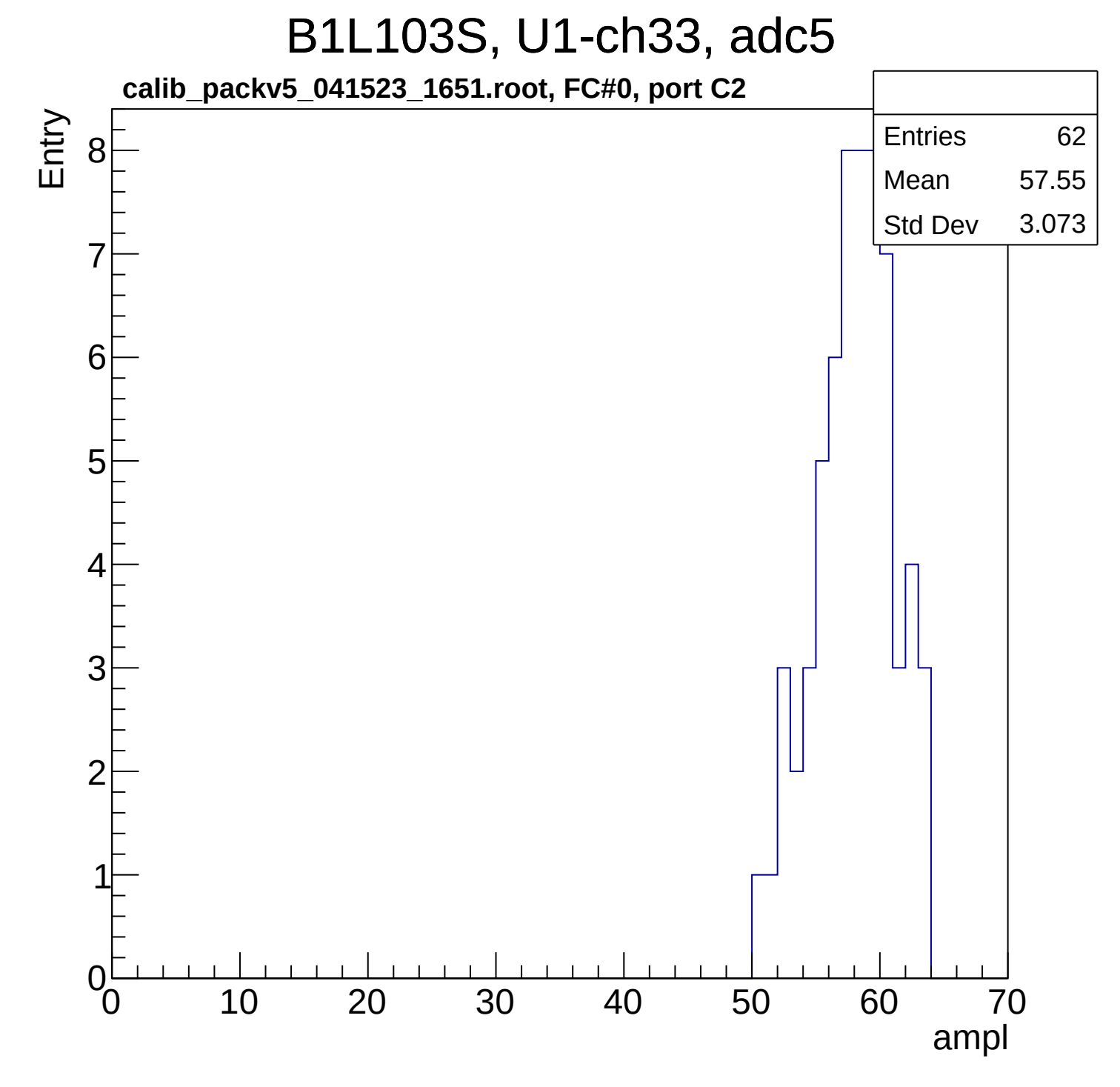

B1L103S, U1-ch33, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 88
Mean 18.5
Std Dev 13.21
Entry
ampl
0
5
10
15
20
25
30
0
10
20
30
40
50
60
70


B1L103S, U1-ch33, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 31.46
Std Dev 9.041
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U1-ch33, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 33.48
Std Dev 15.14
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch33, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 43.4
Std Dev 10.97
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch33, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 52.47
Std Dev 2.803
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U1-ch33, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 57.55
Std Dev 3.073
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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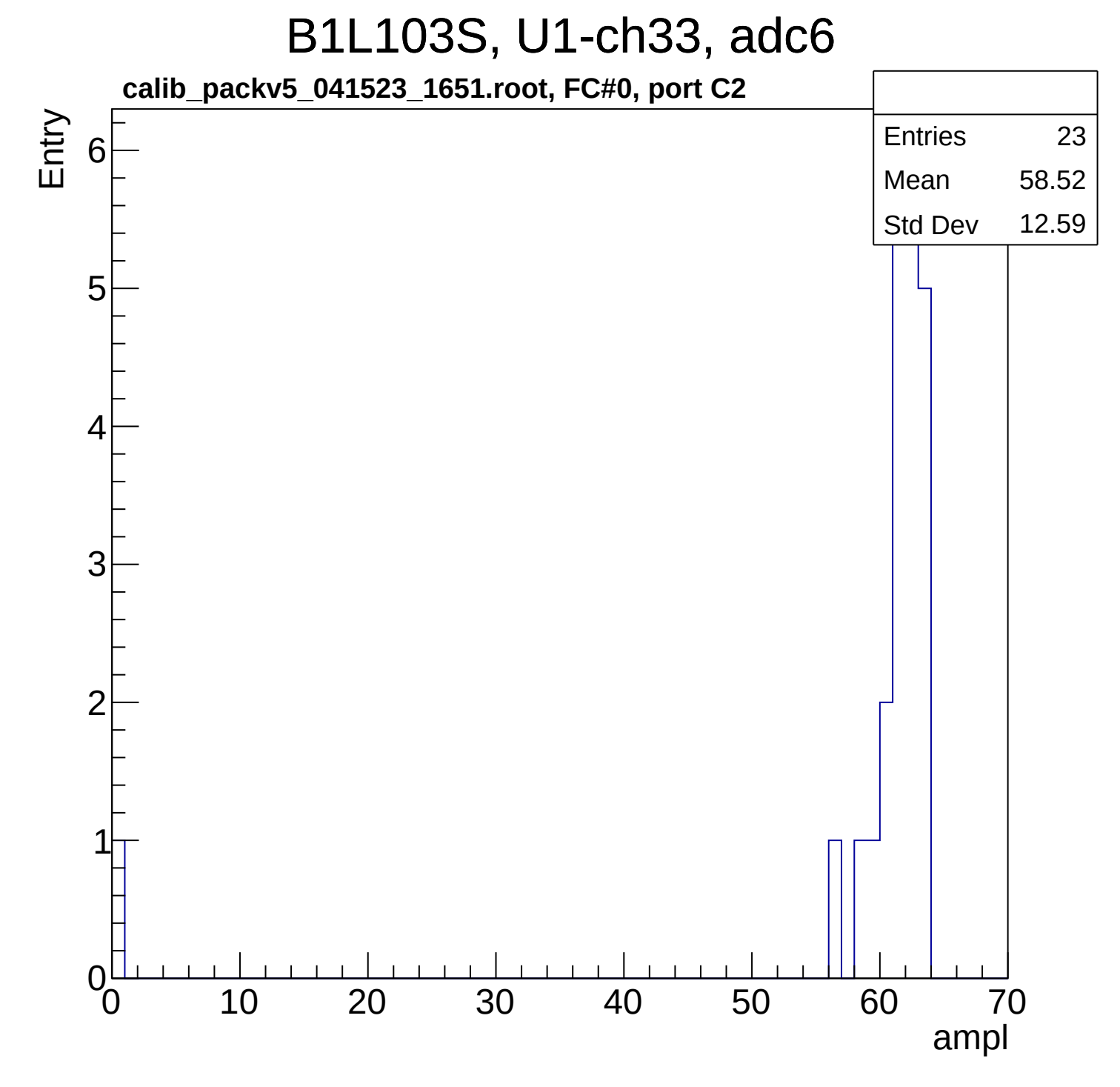
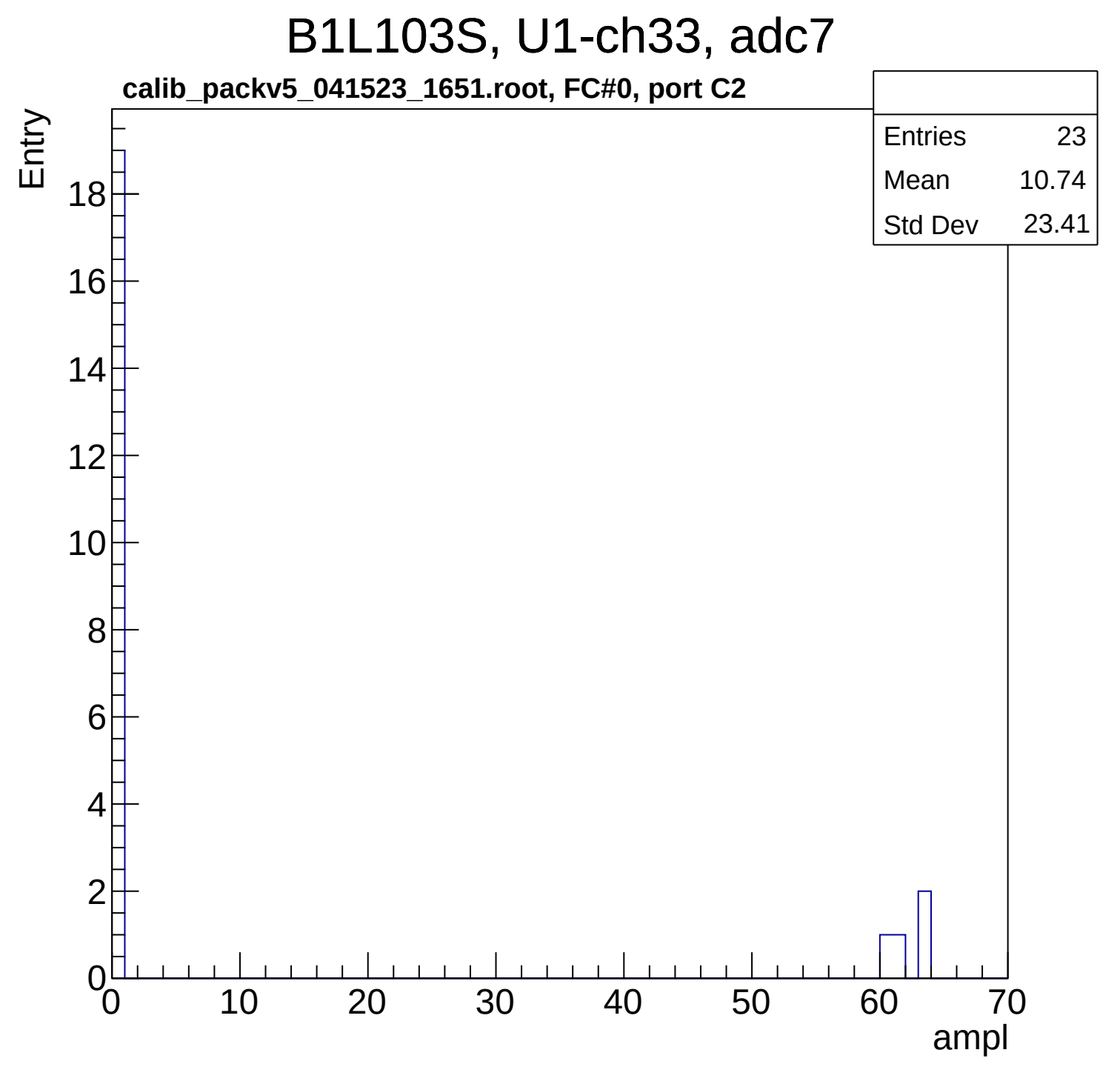
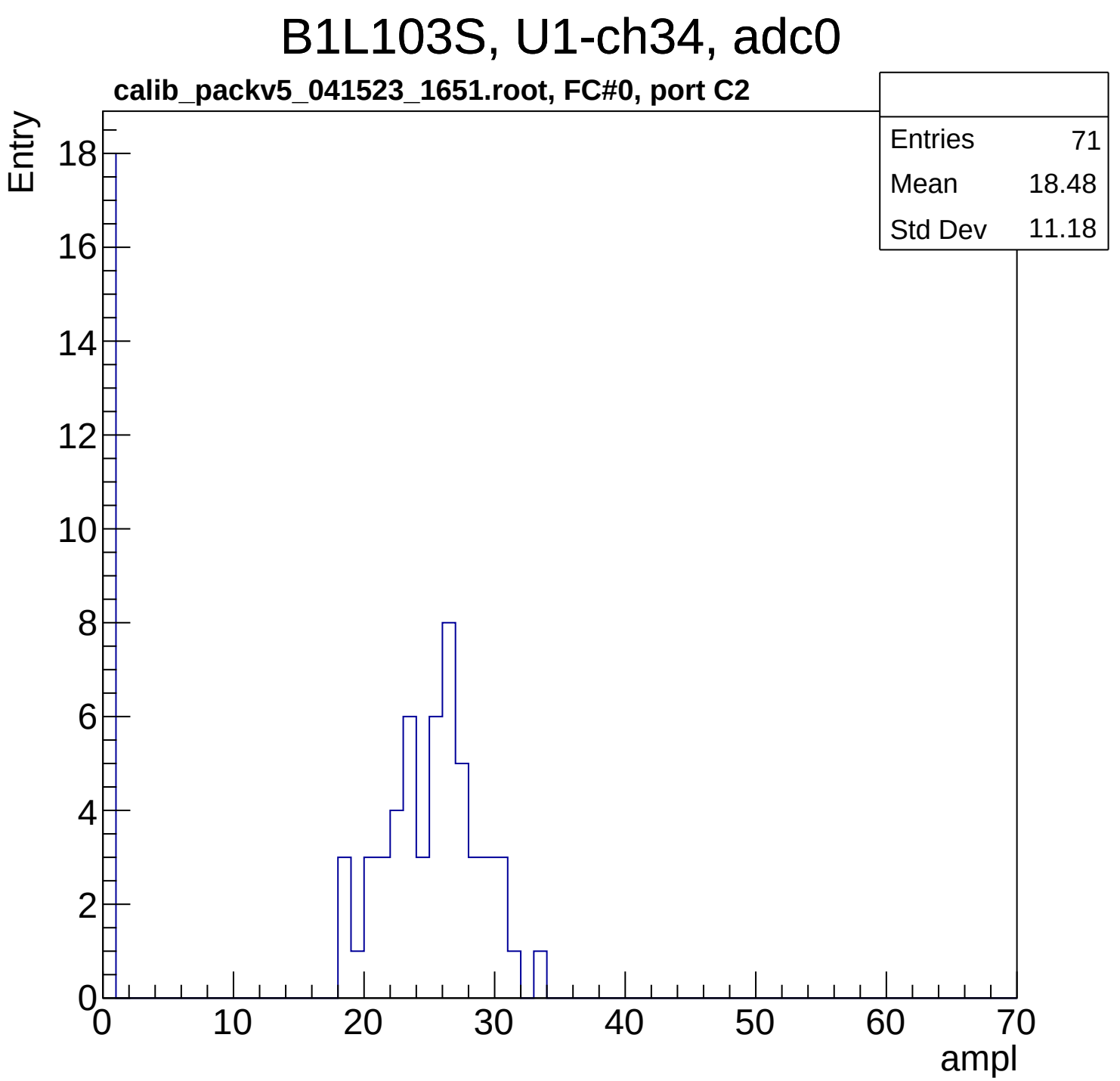
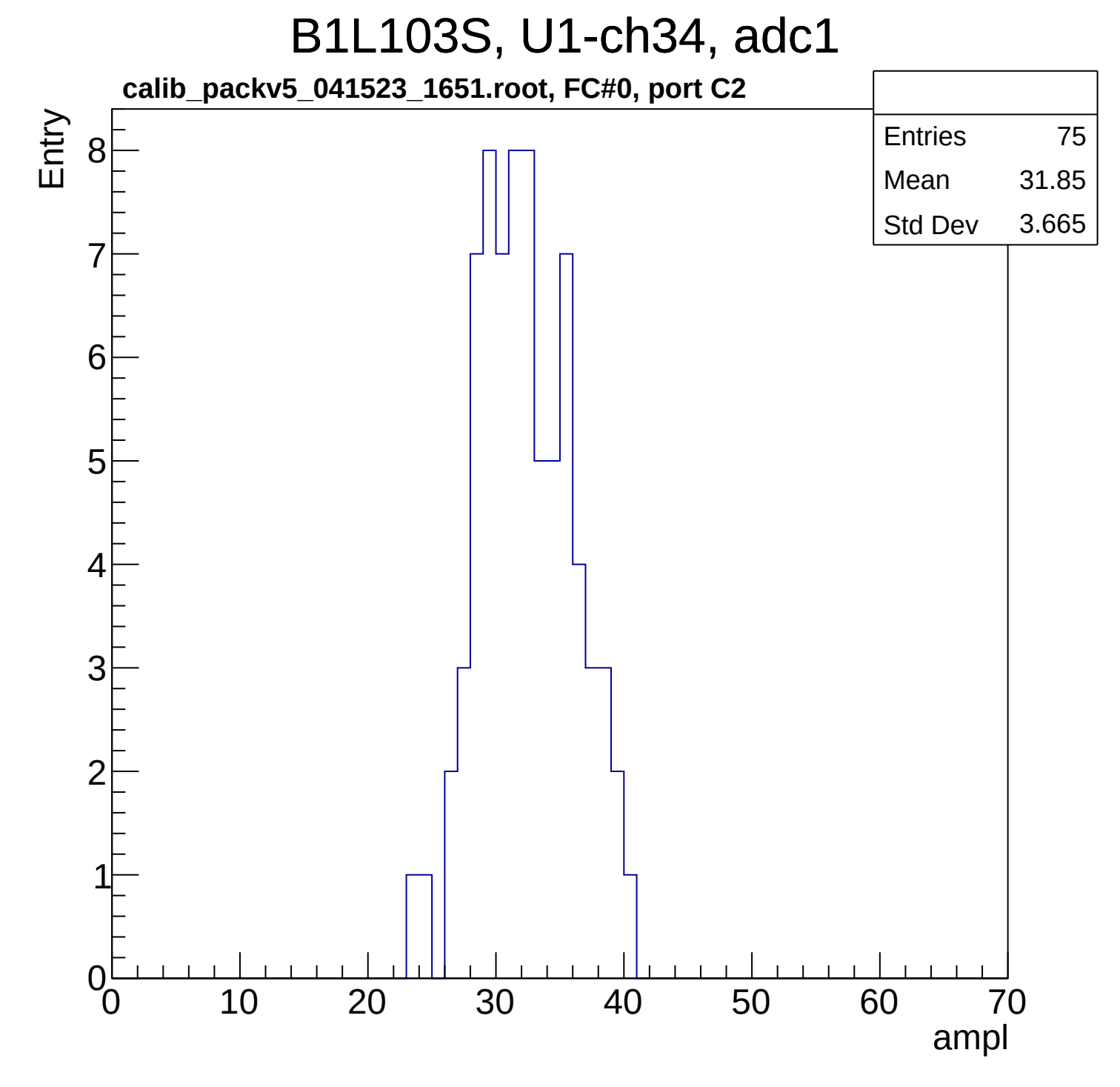

B1L103S, U1-ch33, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 23
Mean 58.52
Std Dev 12.59
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U1-ch33, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 23
Mean 10.74
Std Dev 23.41
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch34, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 18.48
Std Dev 11.18
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch34, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 31.85
Std Dev 3.665
Entry
ampl
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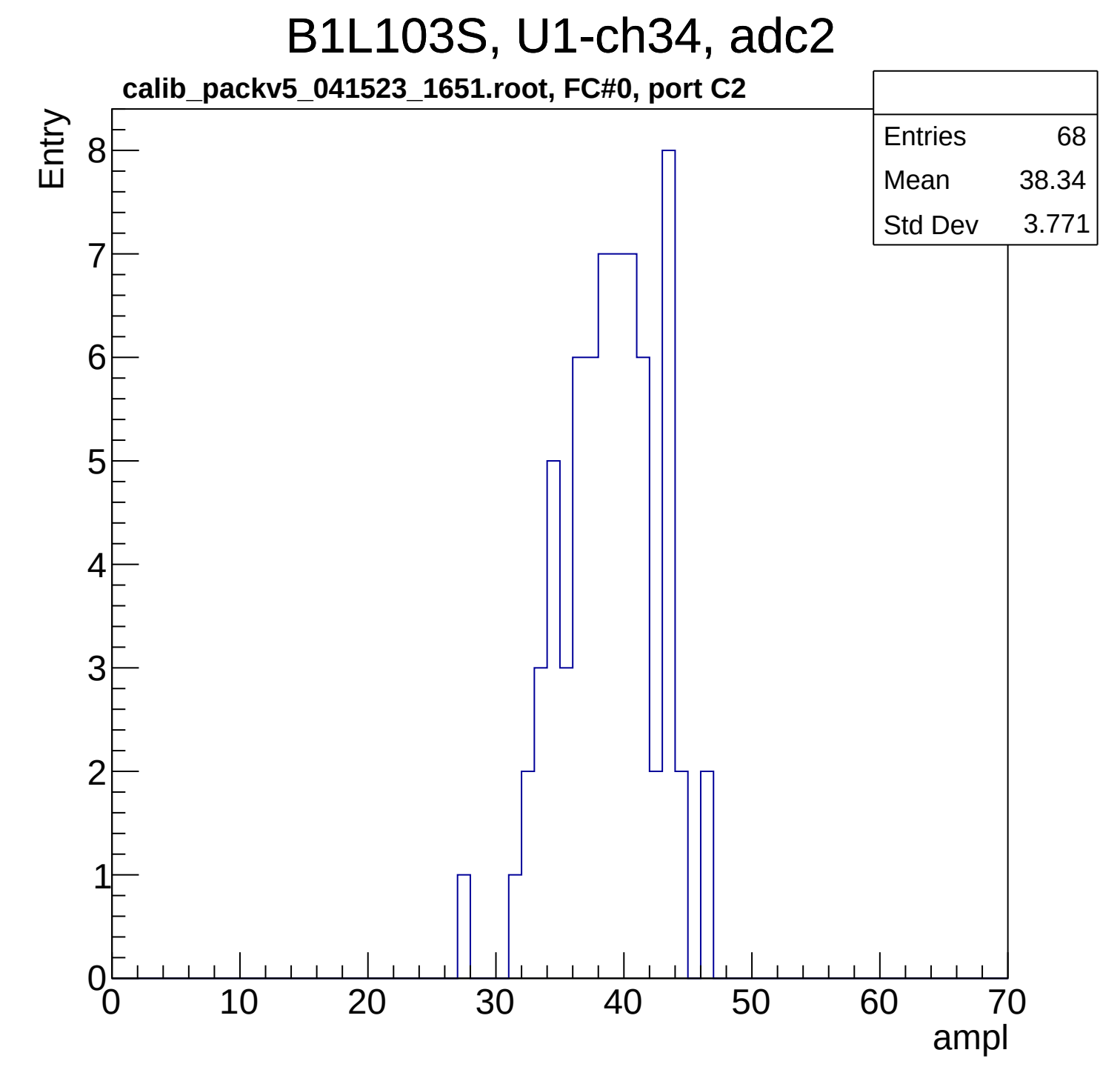
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U1-ch34, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 38.34
Std Dev 3.771
Entry
ampl
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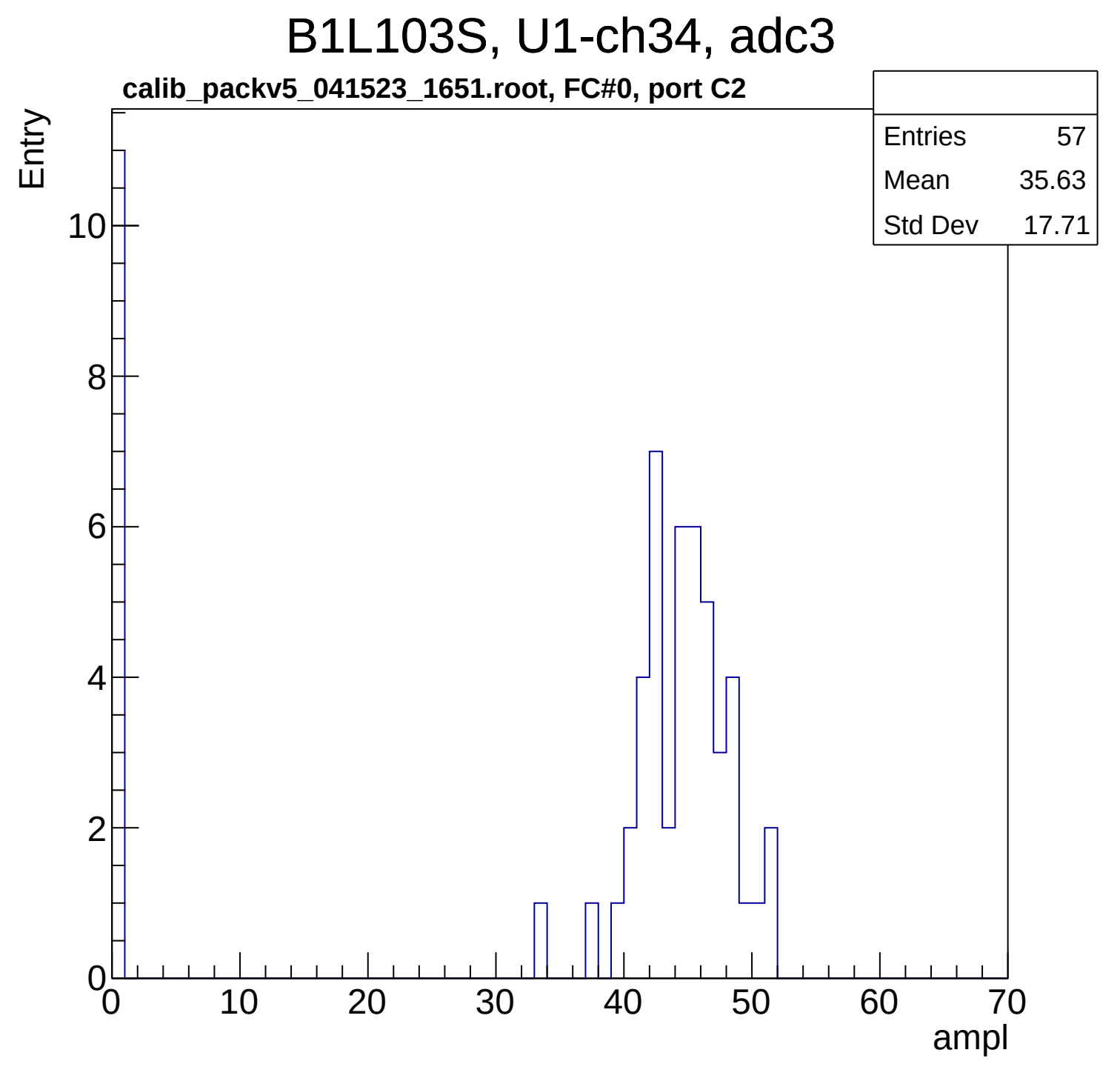
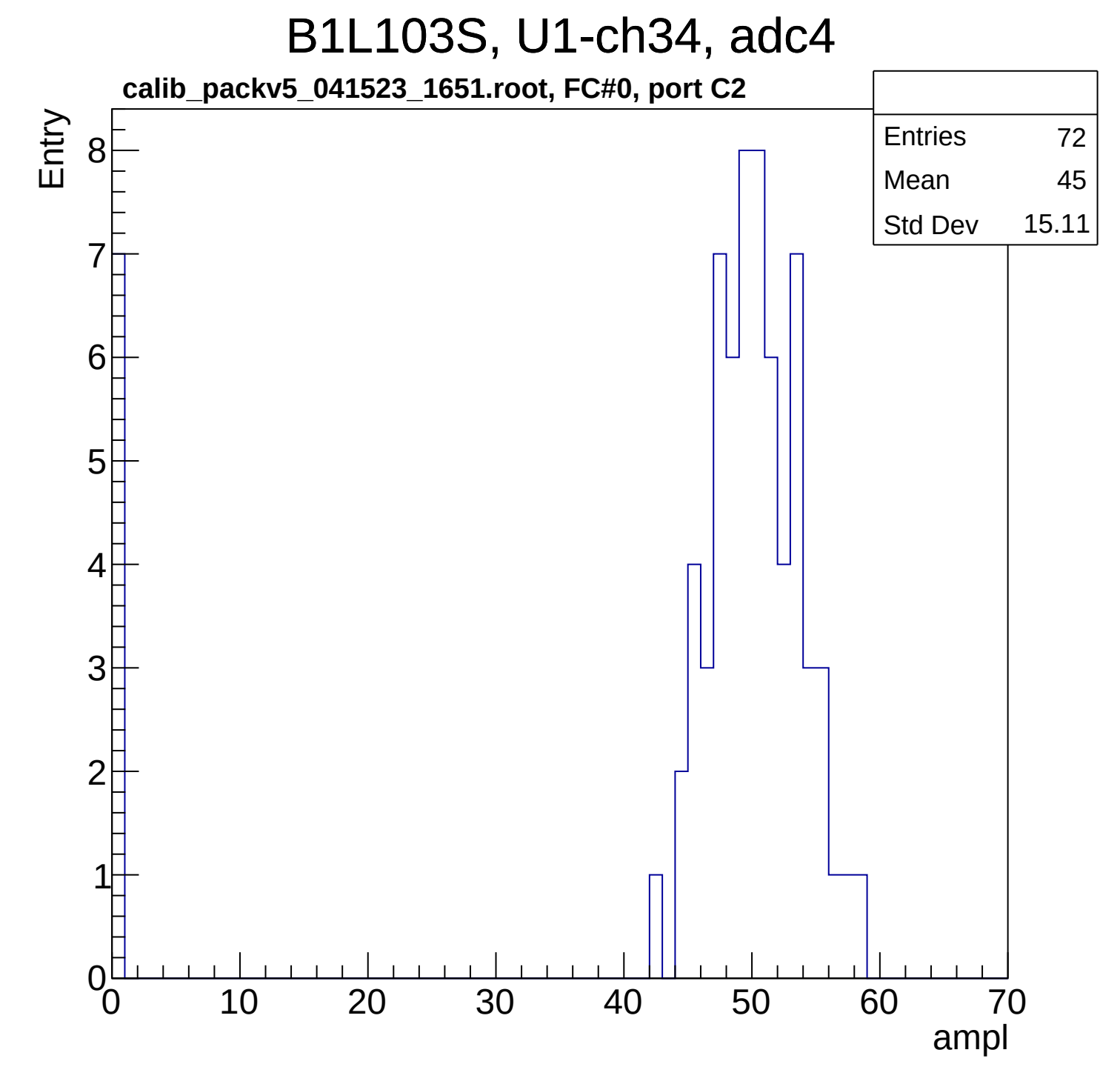
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U1-ch34, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 35.63
Std Dev 17.71
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch34, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 45
Std Dev 15.11
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
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60
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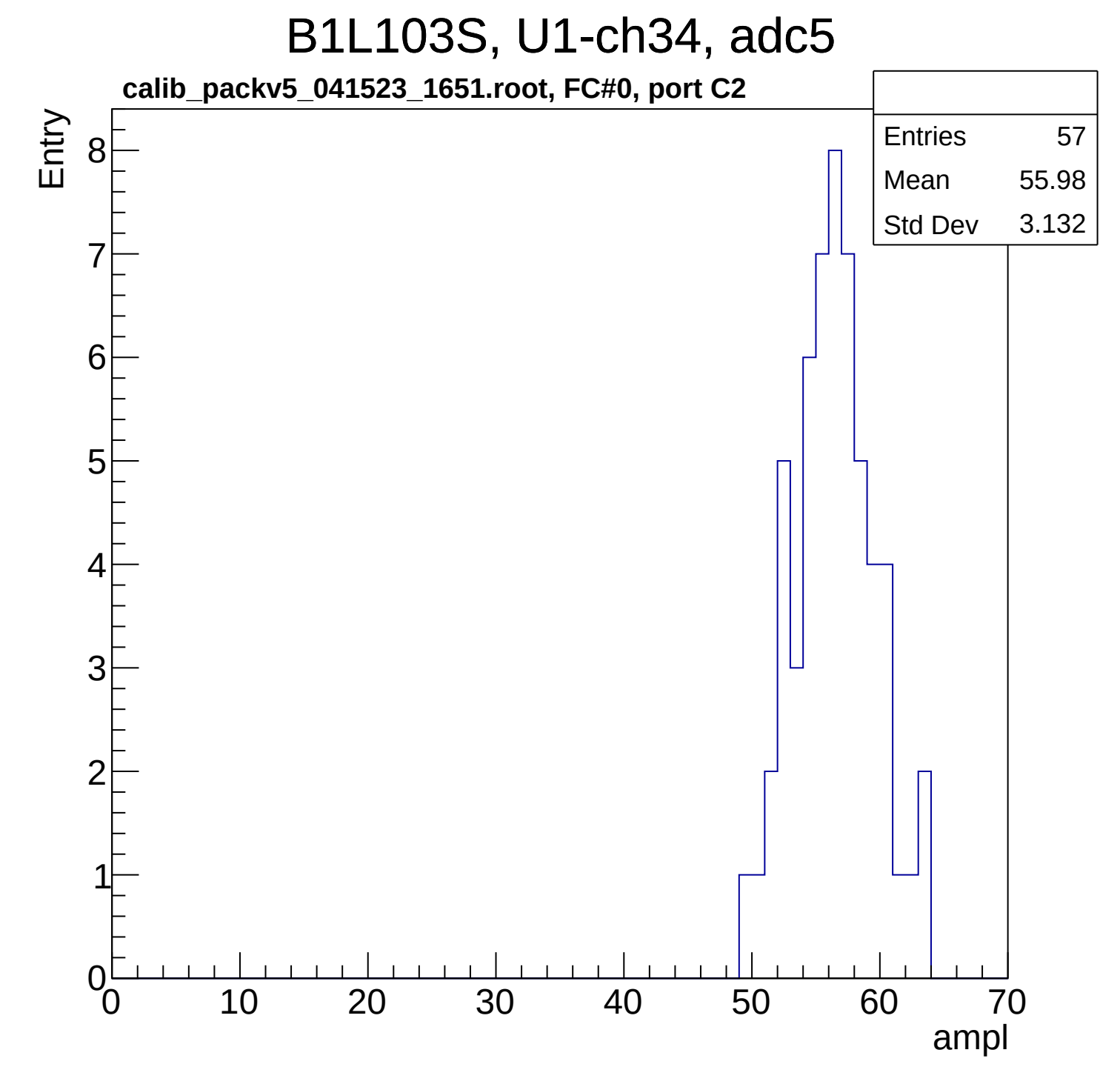
B1L103S, U1-ch34, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 55.98
Std Dev 3.132
Entry
ampl
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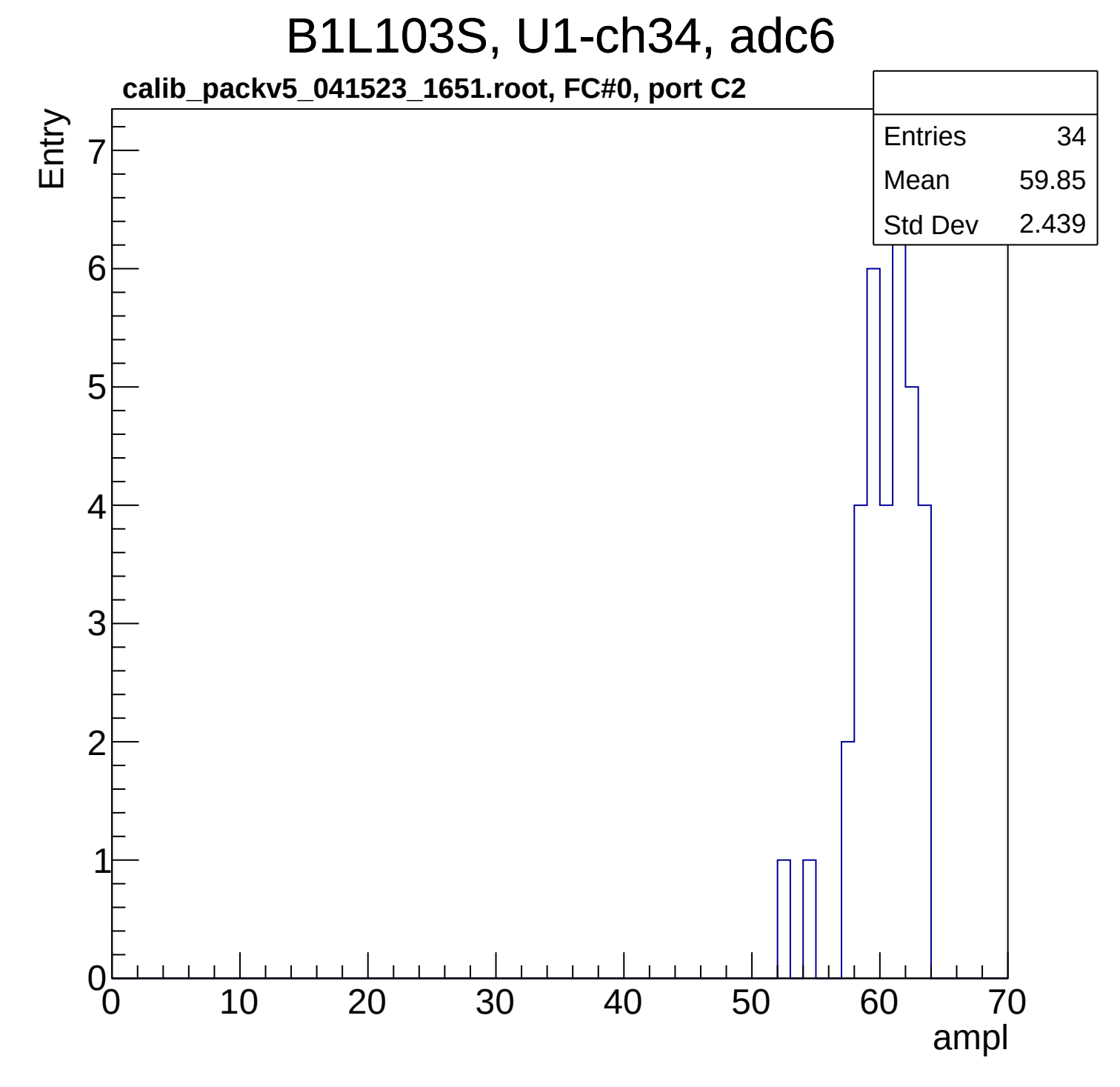
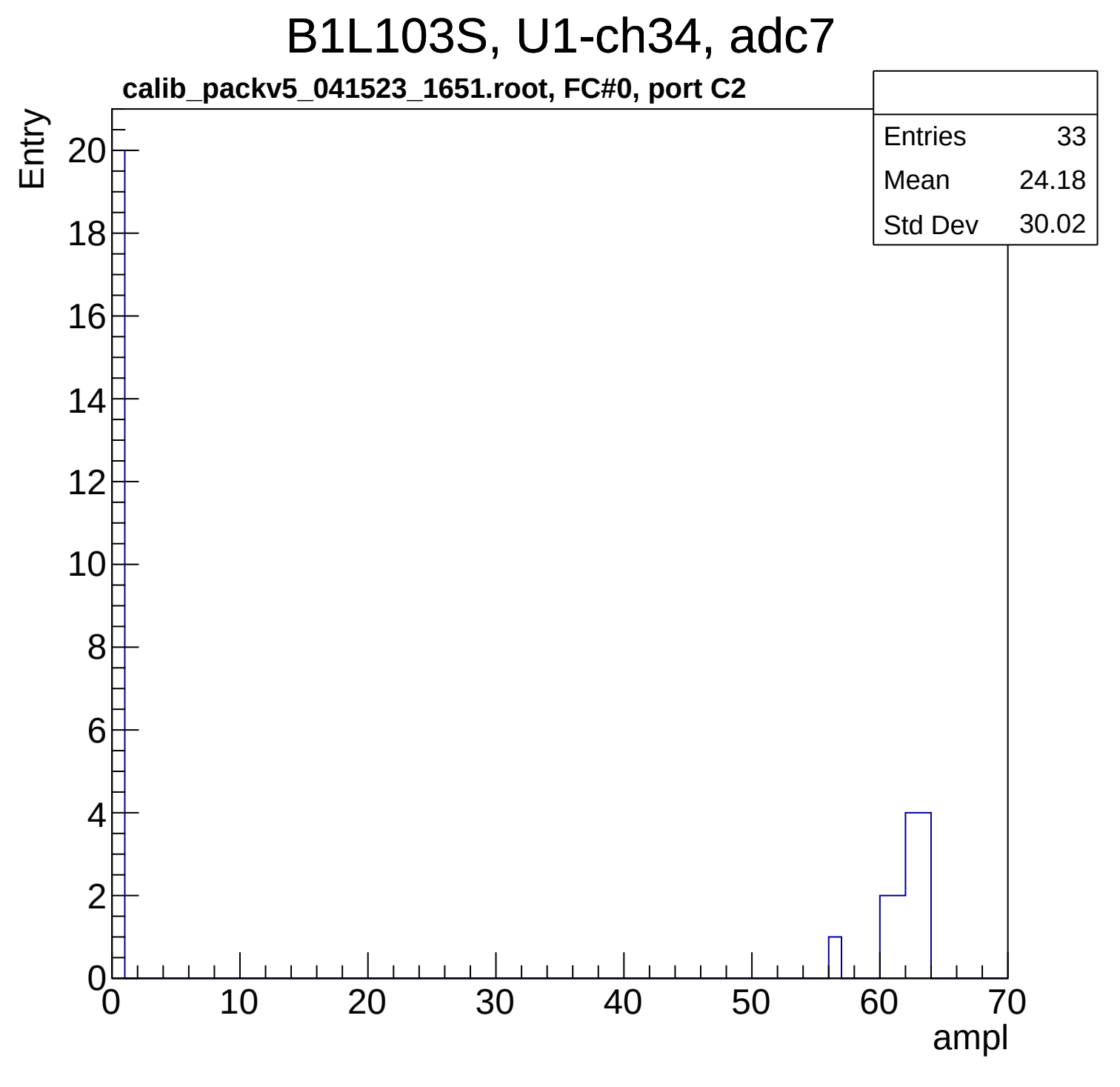
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U1-ch34, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 34
Mean 59.85
Std Dev 2.439
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U1-ch34, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 33
Mean 24.18
Std Dev 30.02
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
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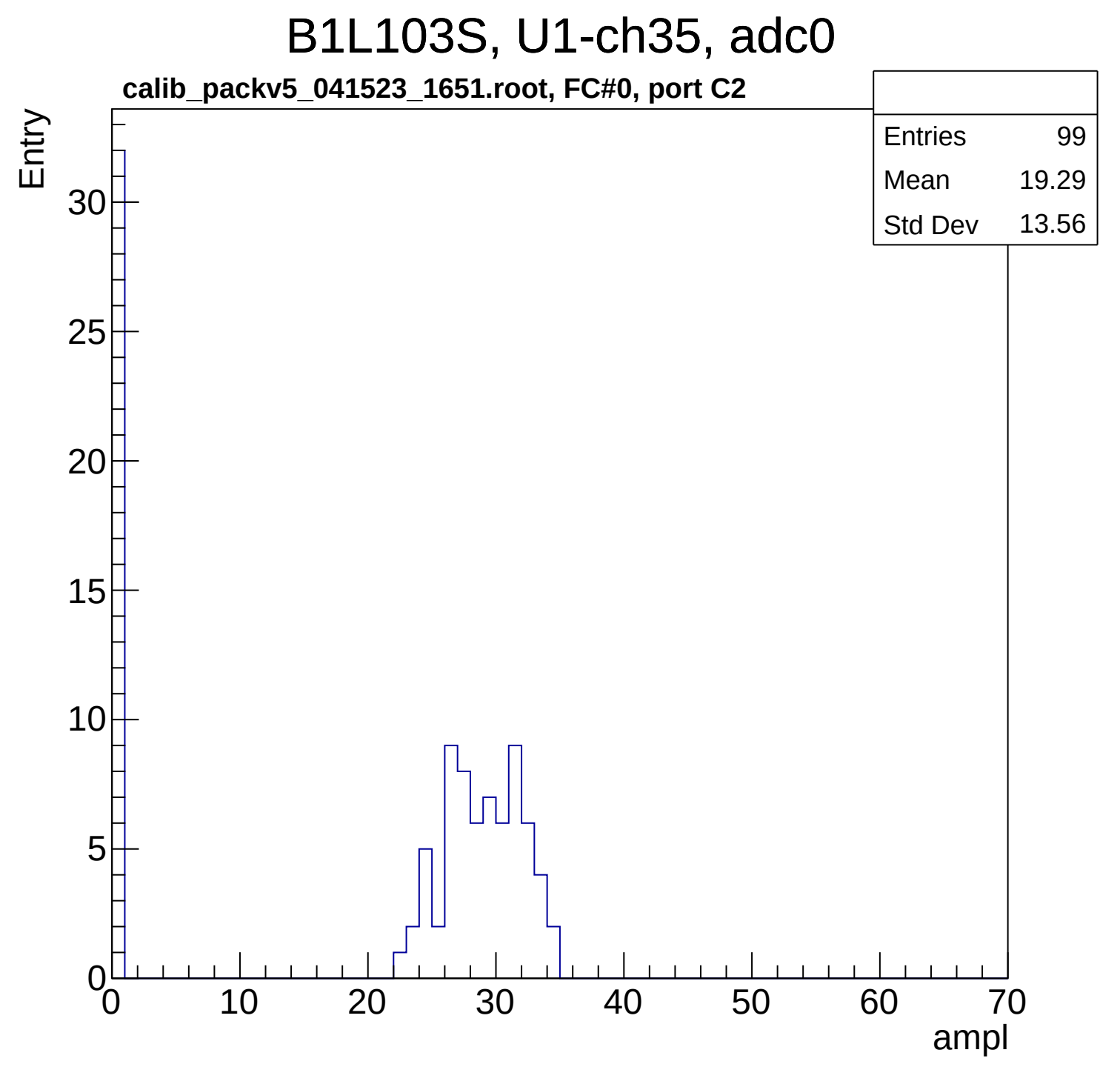
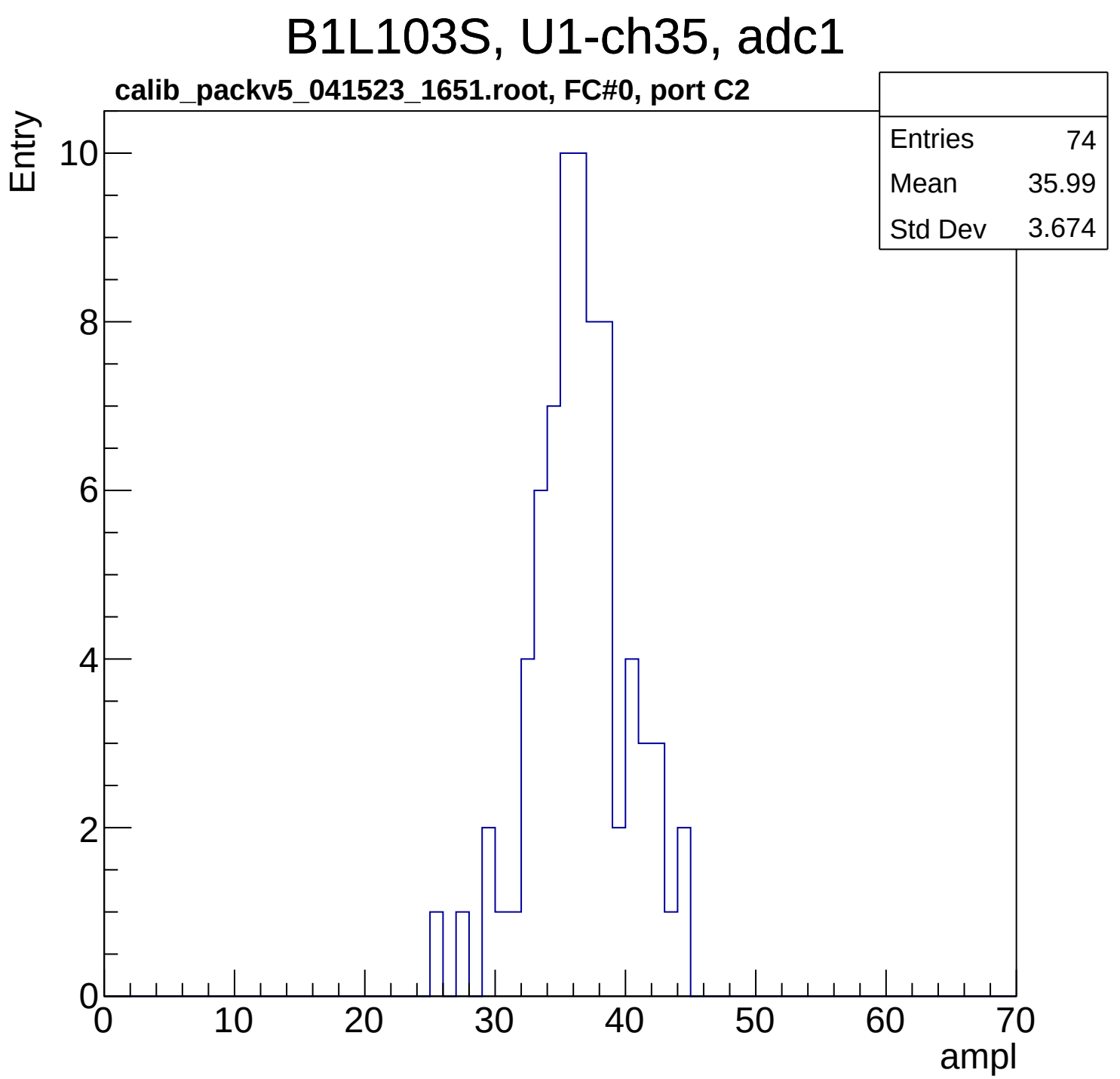
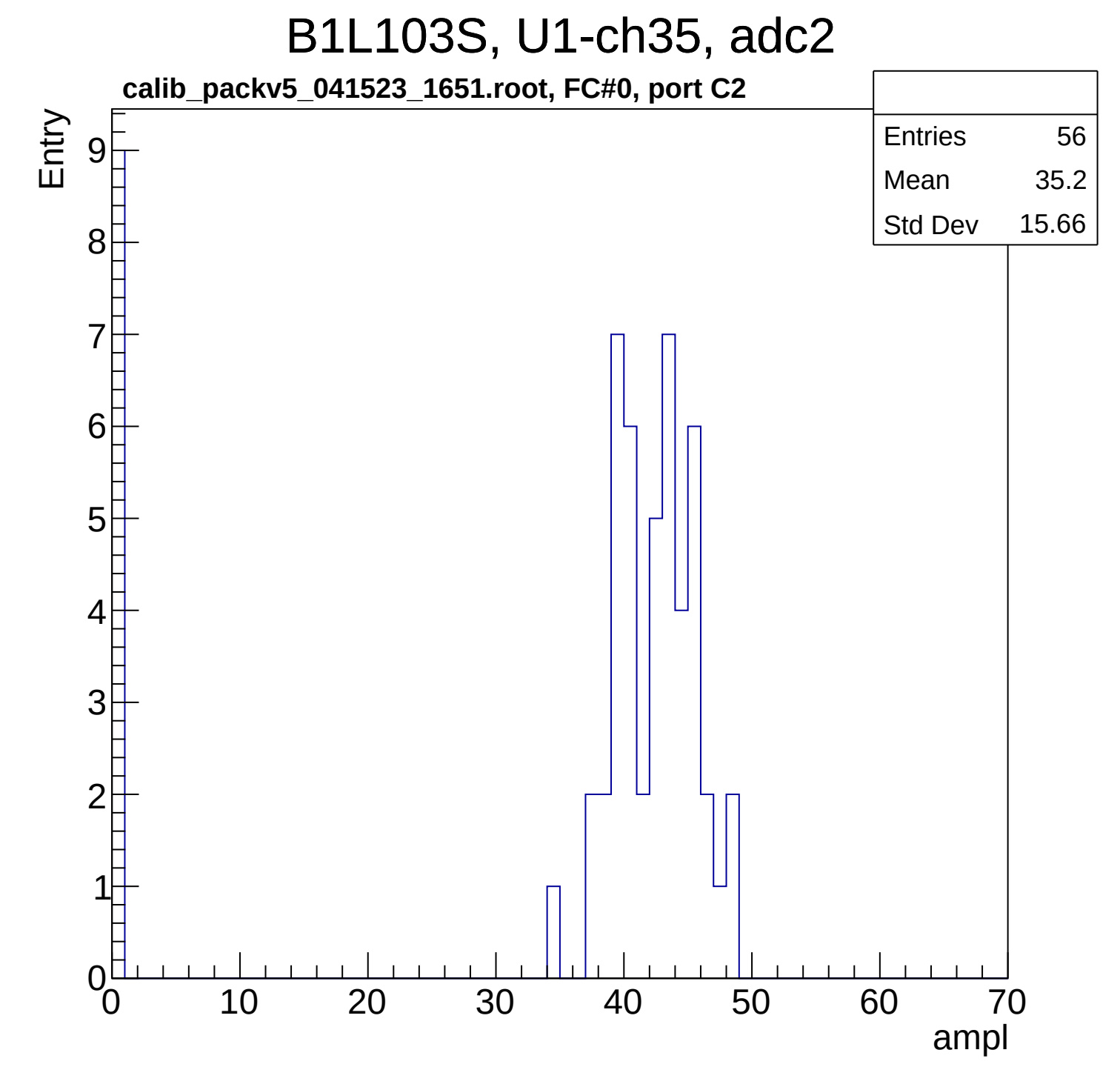
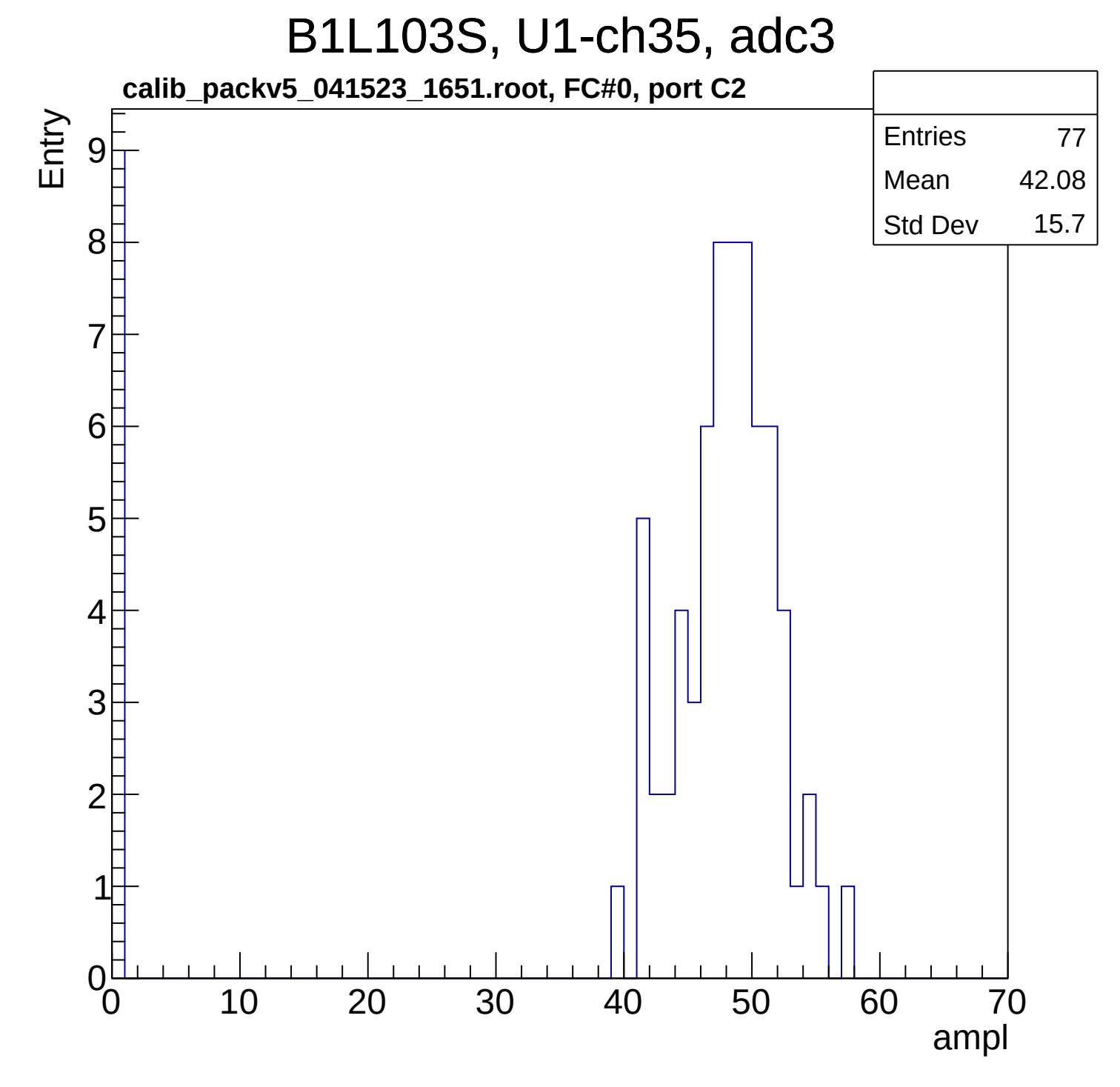
20
30
40
50
60
70


B1L103S, U1-ch35, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 99
Mean 19.29
Std Dev 13.56
Entry
ampl
0
5
10
15
20
25
30
0
10
20
30
40
50
60
70


B1L103S, U1-ch35, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 35.99
Std Dev 3.674
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U1-ch35, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 35.2
Std Dev 15.66
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U1-ch35, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 42.08
Std Dev 15.7
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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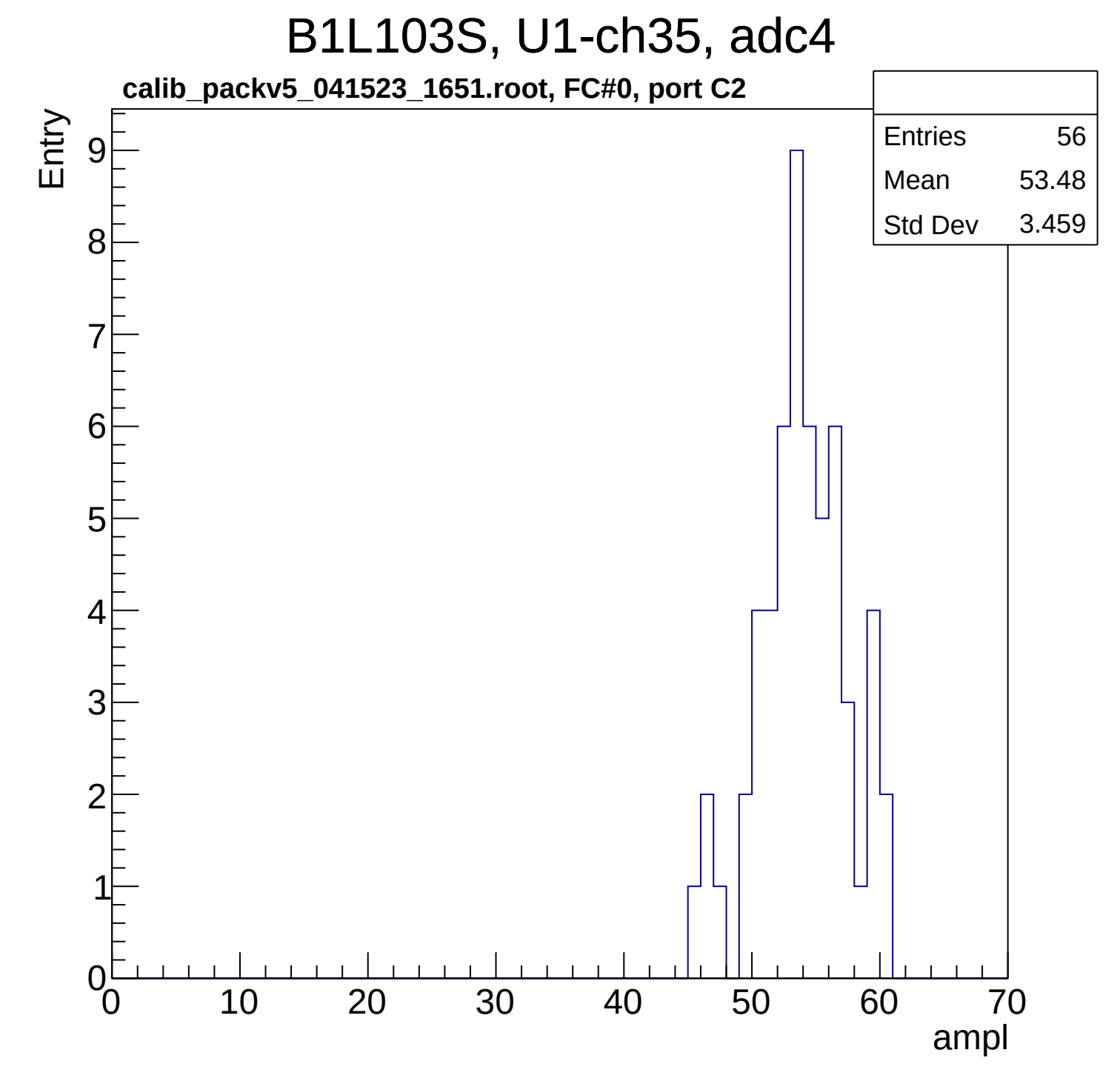
40
50
60
70


B1L103S, U1-ch35, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 53.48
Std Dev 3.459
Entry
ampl
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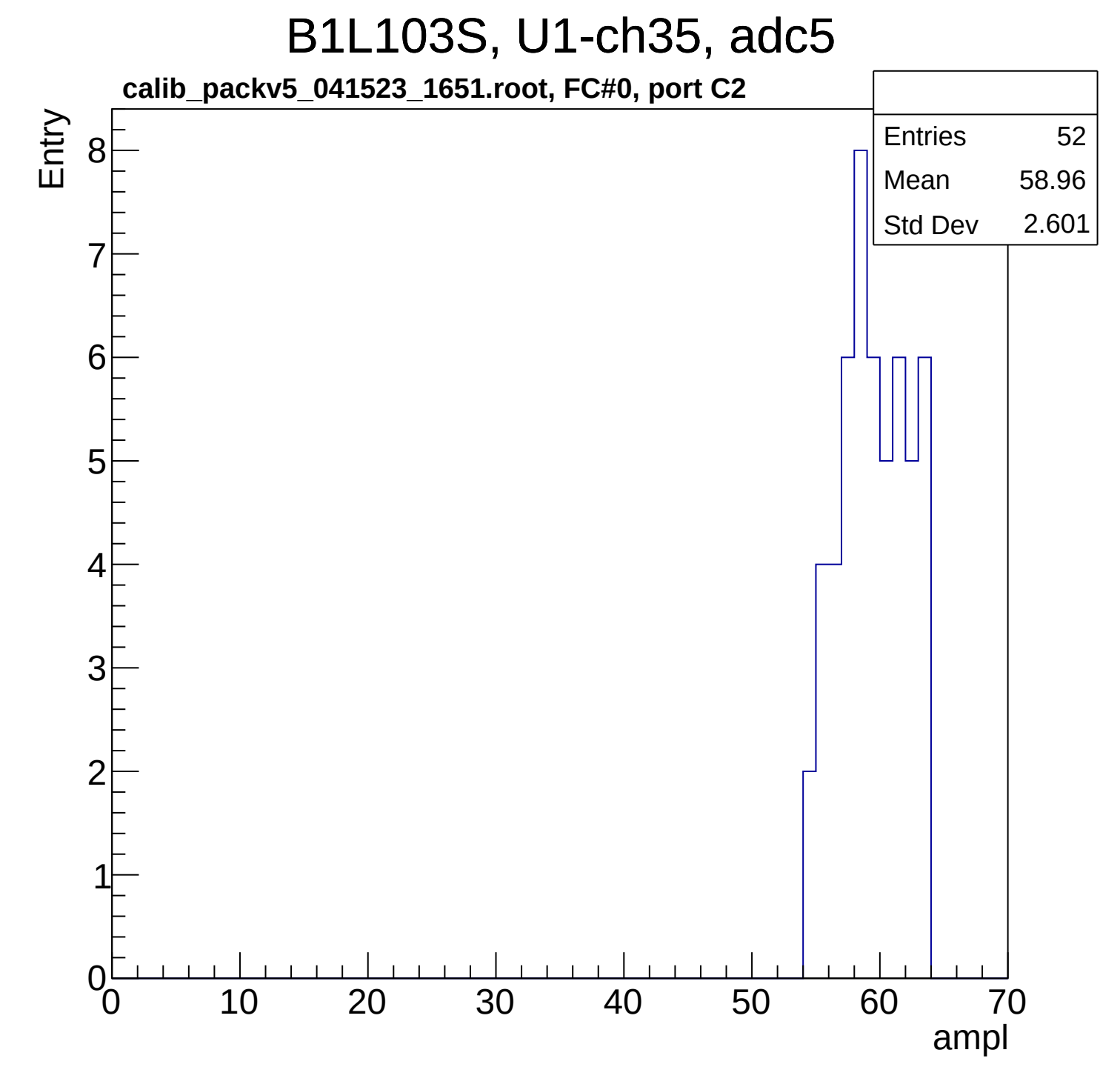
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U1-ch35, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 58.96
Std Dev 2.601
Entry
ampl
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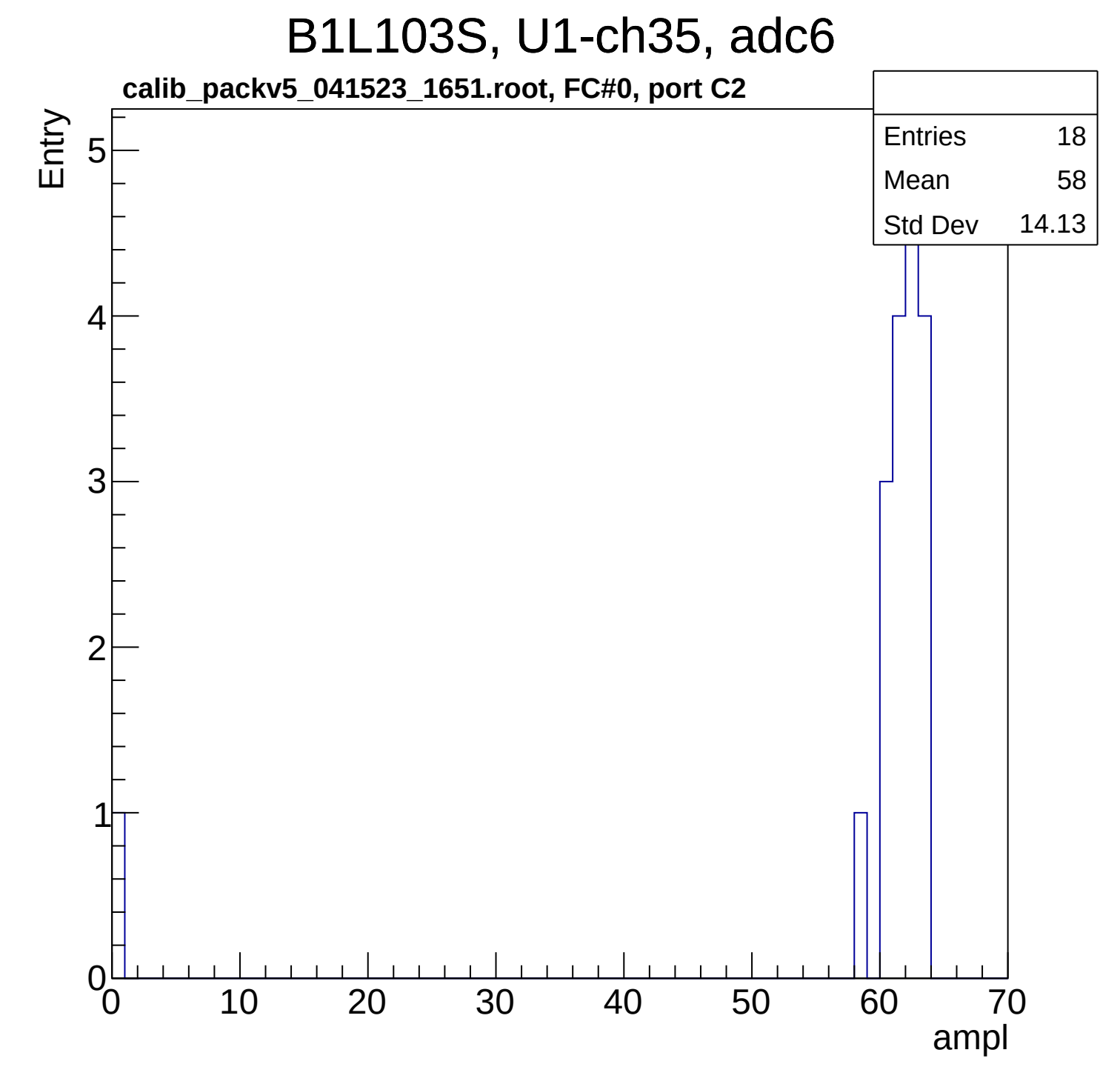
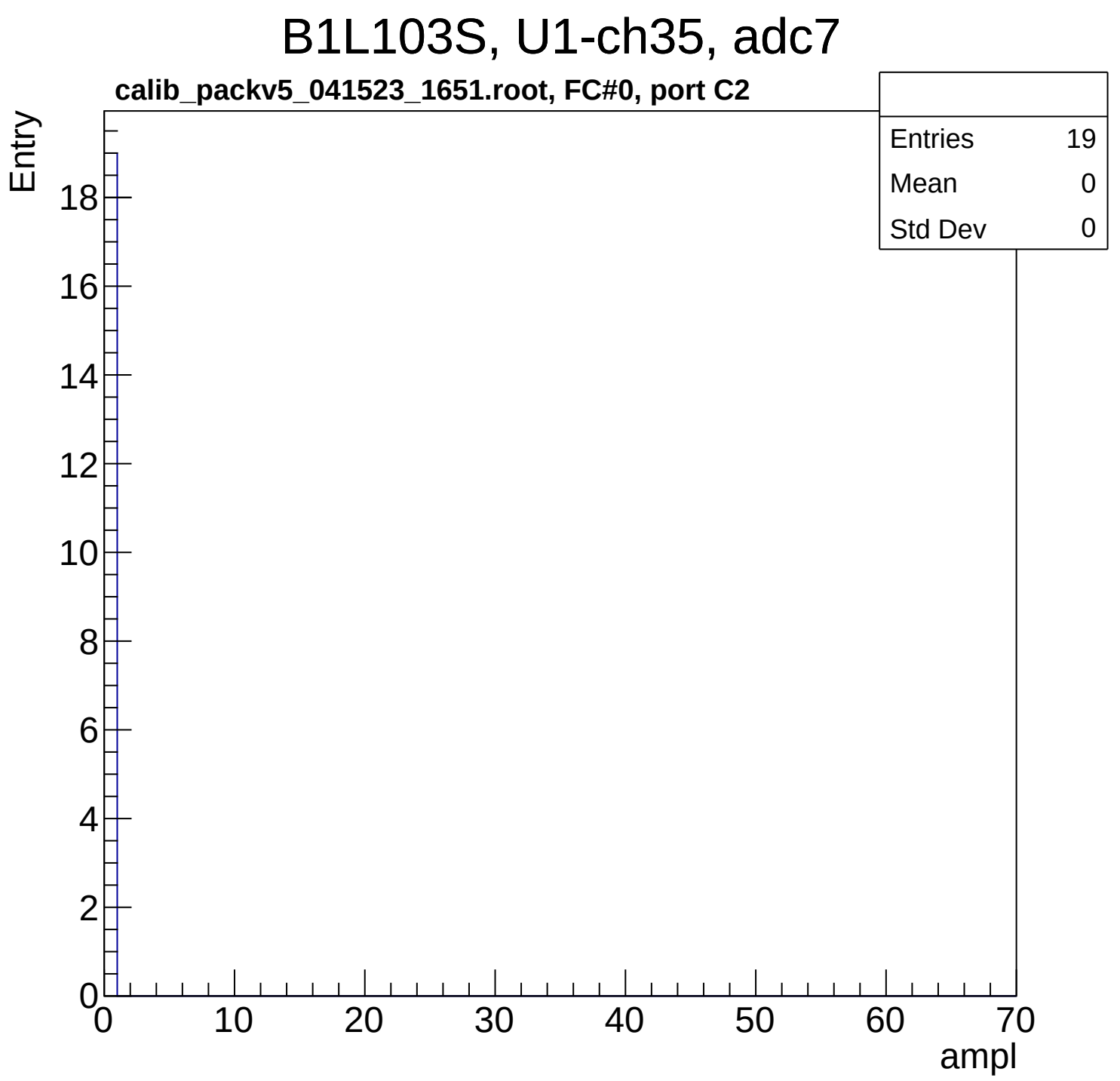
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U1-ch35, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 58
Std Dev 14.13
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U1-ch35, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
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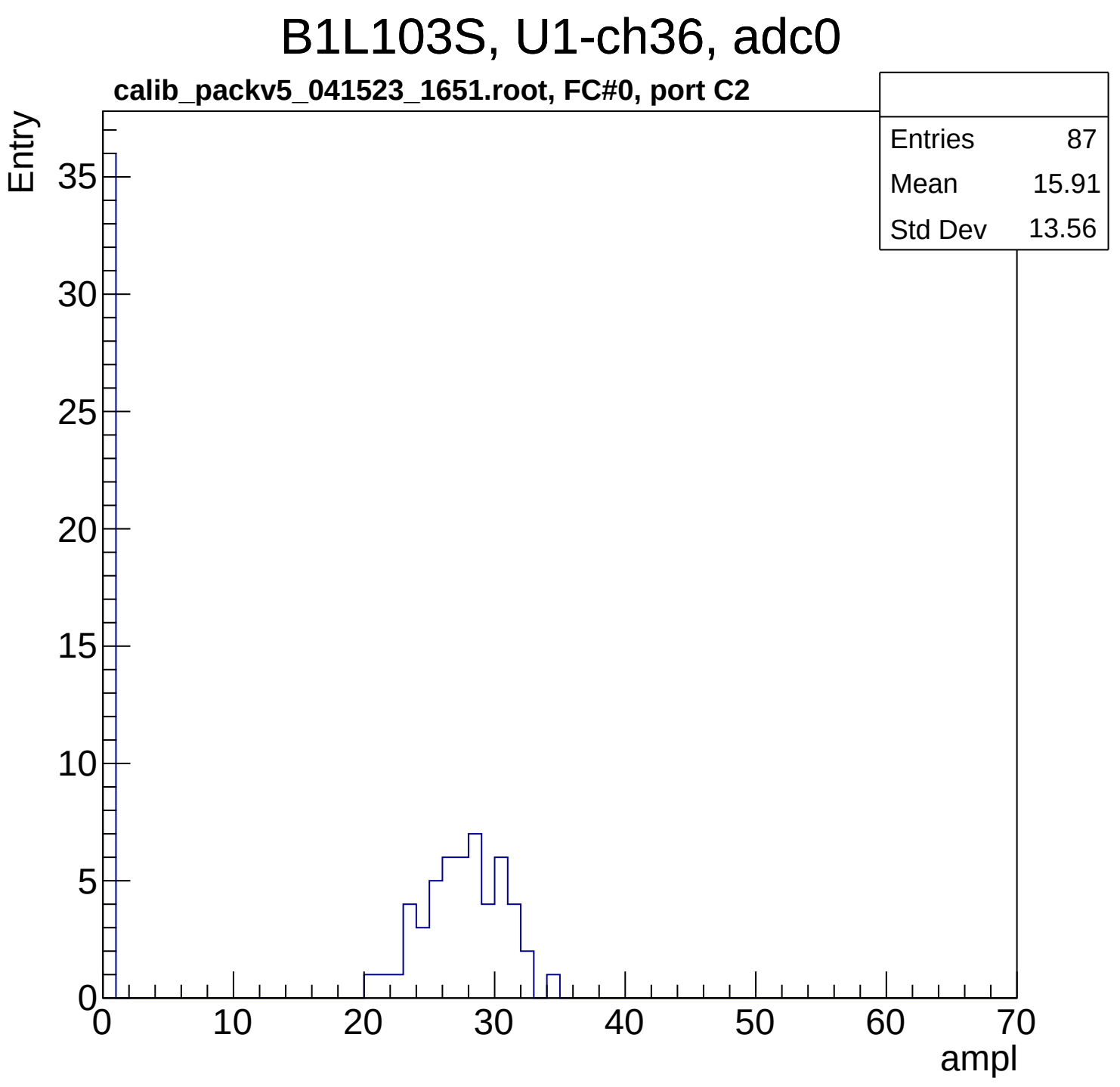
50
60
70
ampl


B1L103S, U1-ch36, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 87
Mean 15.91
Std Dev 13.56
Entry
0
5
10
15
20
25
30
35
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10
20
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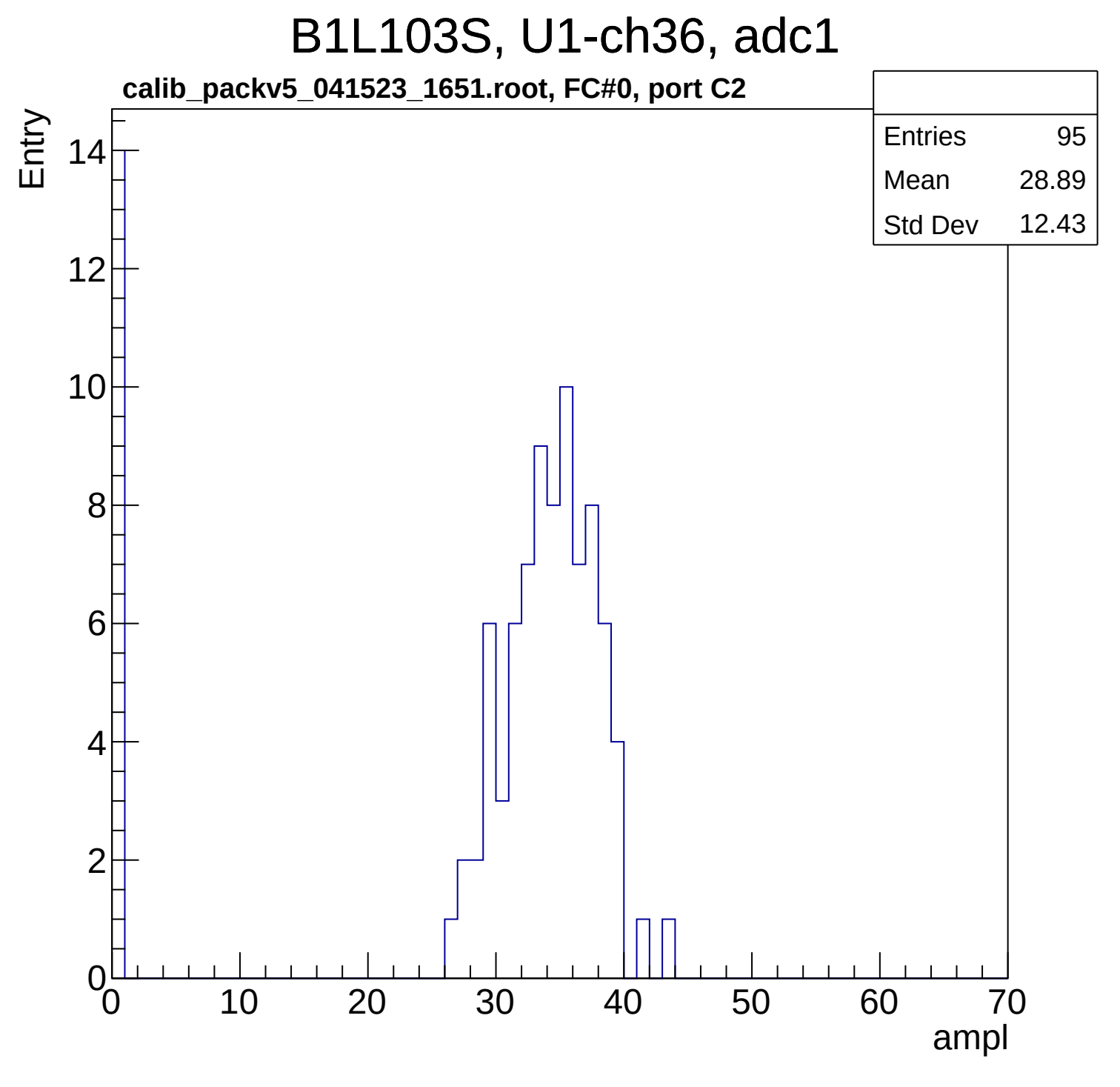
50
60
70
ampl


B1L103S, U1-ch36, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 95
Mean 28.89
Std Dev 12.43
Entry
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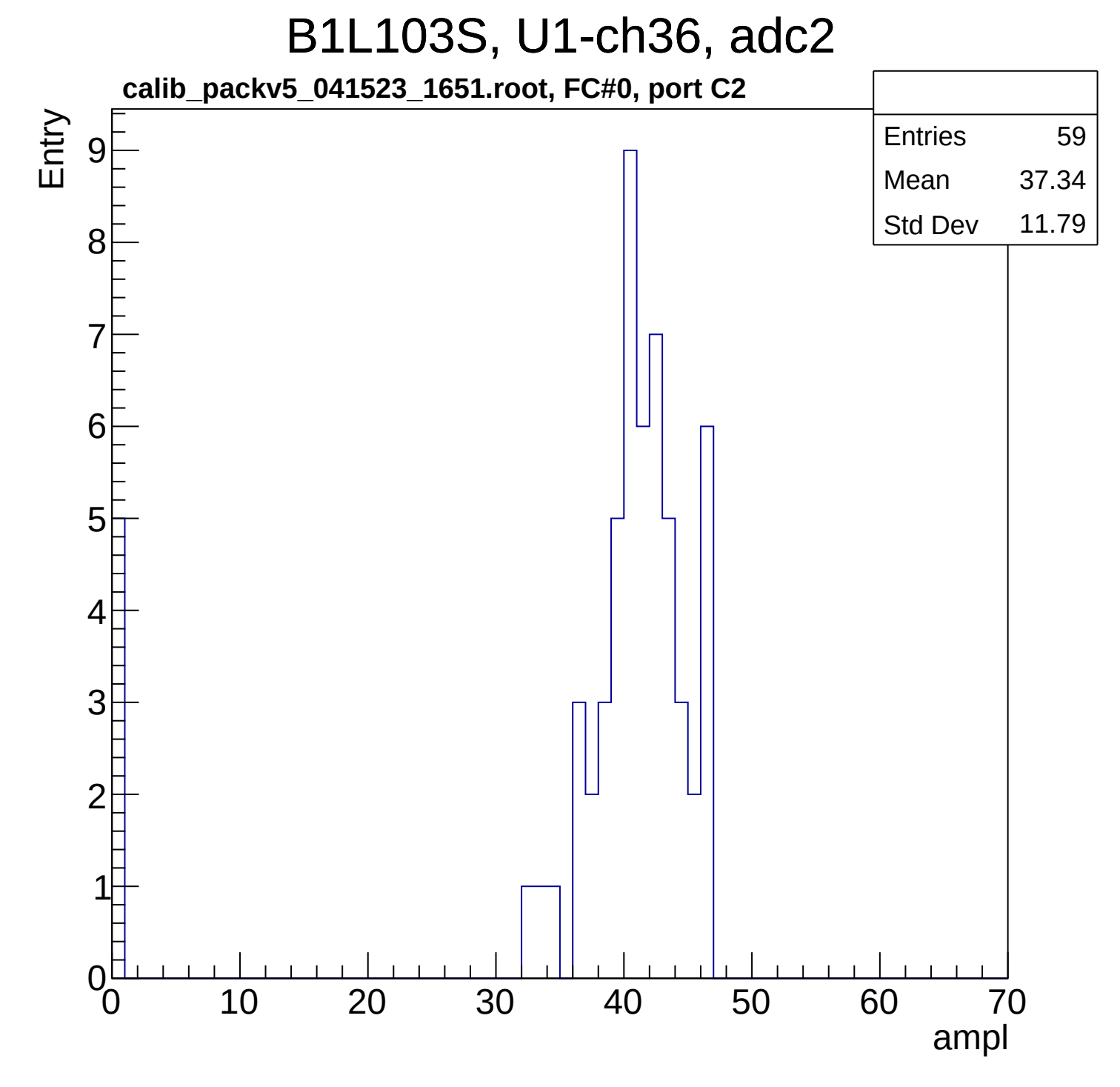
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch36, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 37.34
Std Dev 11.79
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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30
40
50
60
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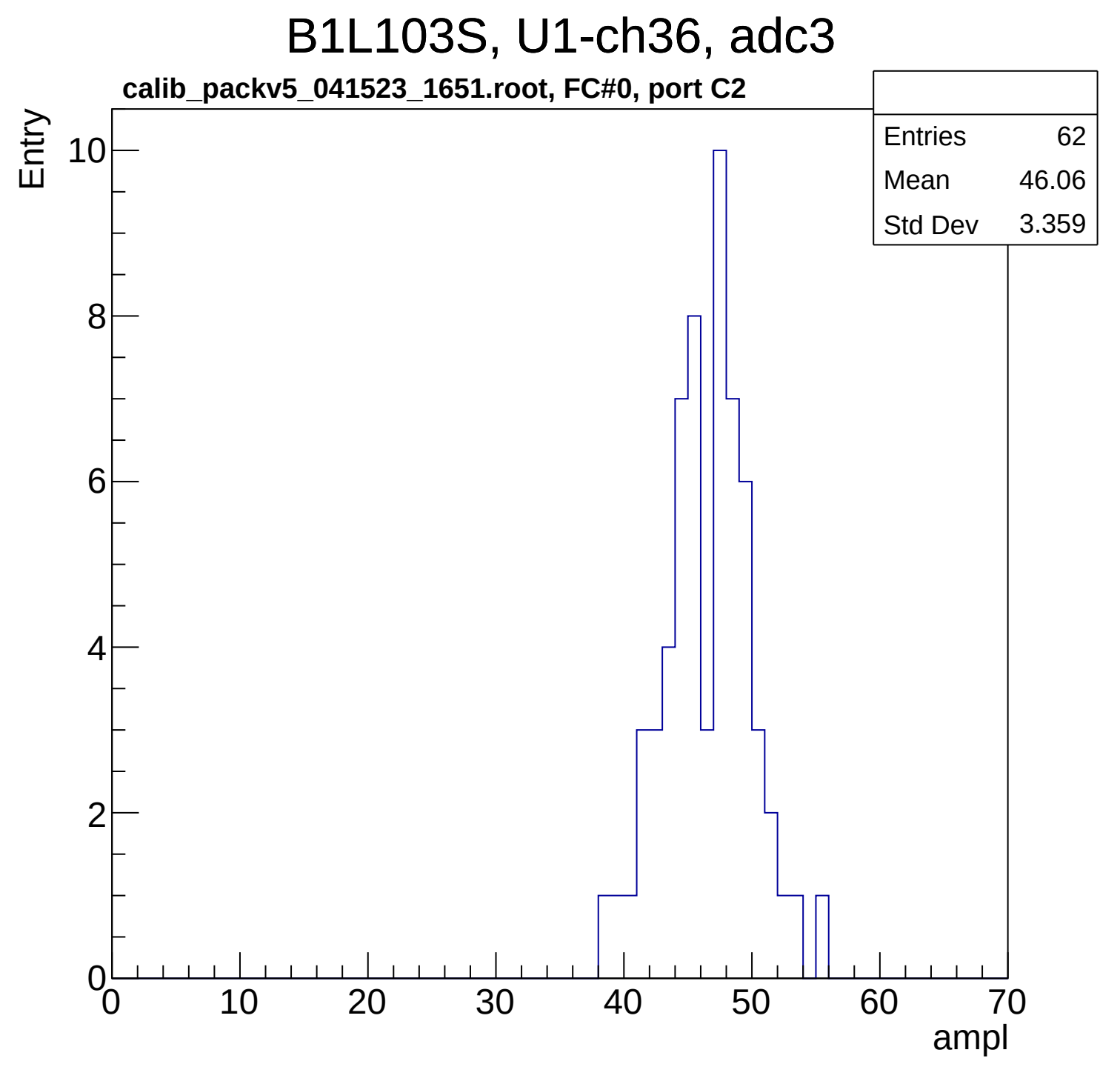
B1L103S, U1-ch36, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 46.06
Std Dev 3.359
Entry
ampl
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4
6
8
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0
10
20
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40
50
60
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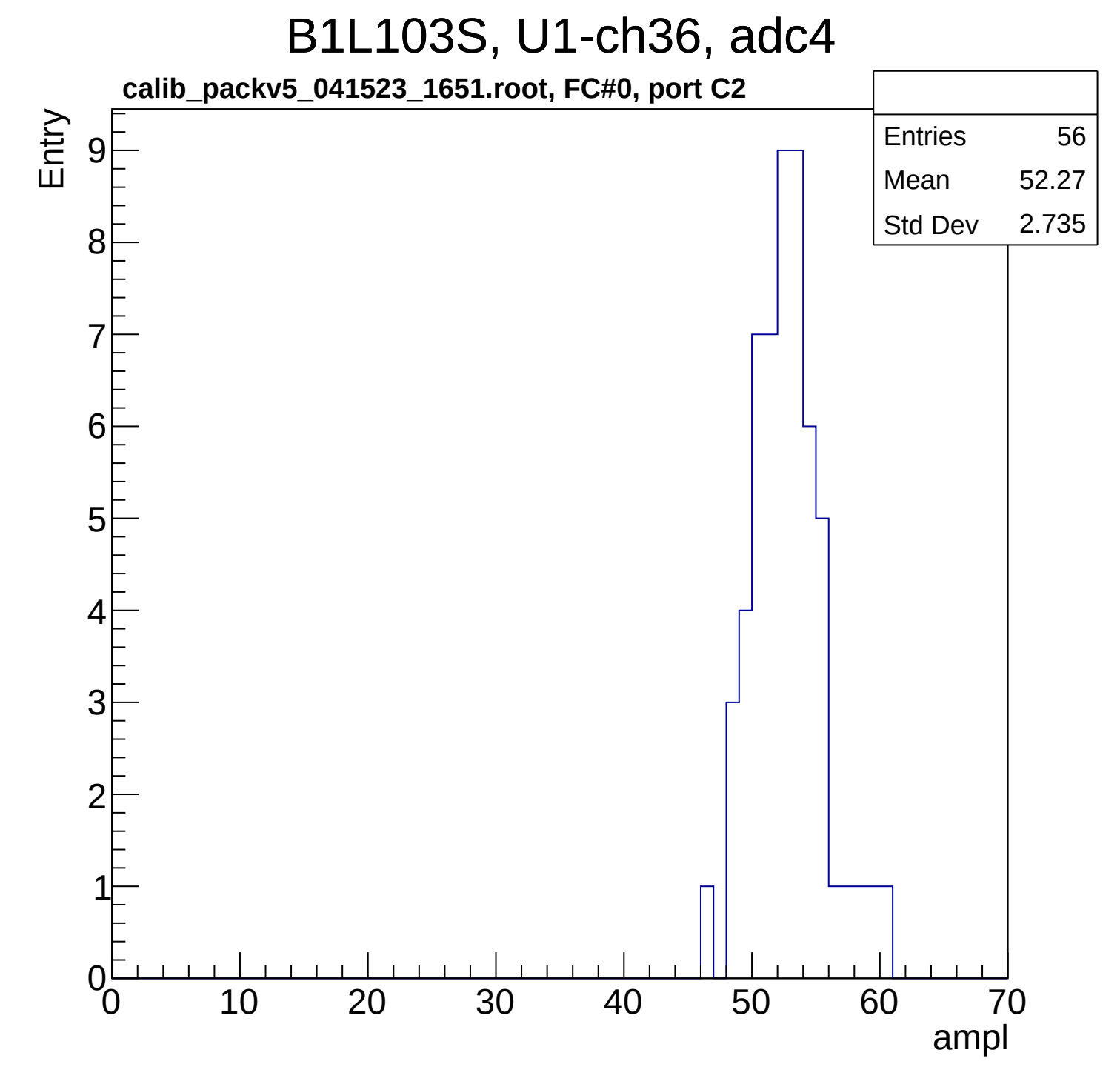
B1L103S, U1-ch36, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 52.27
Std Dev 2.735
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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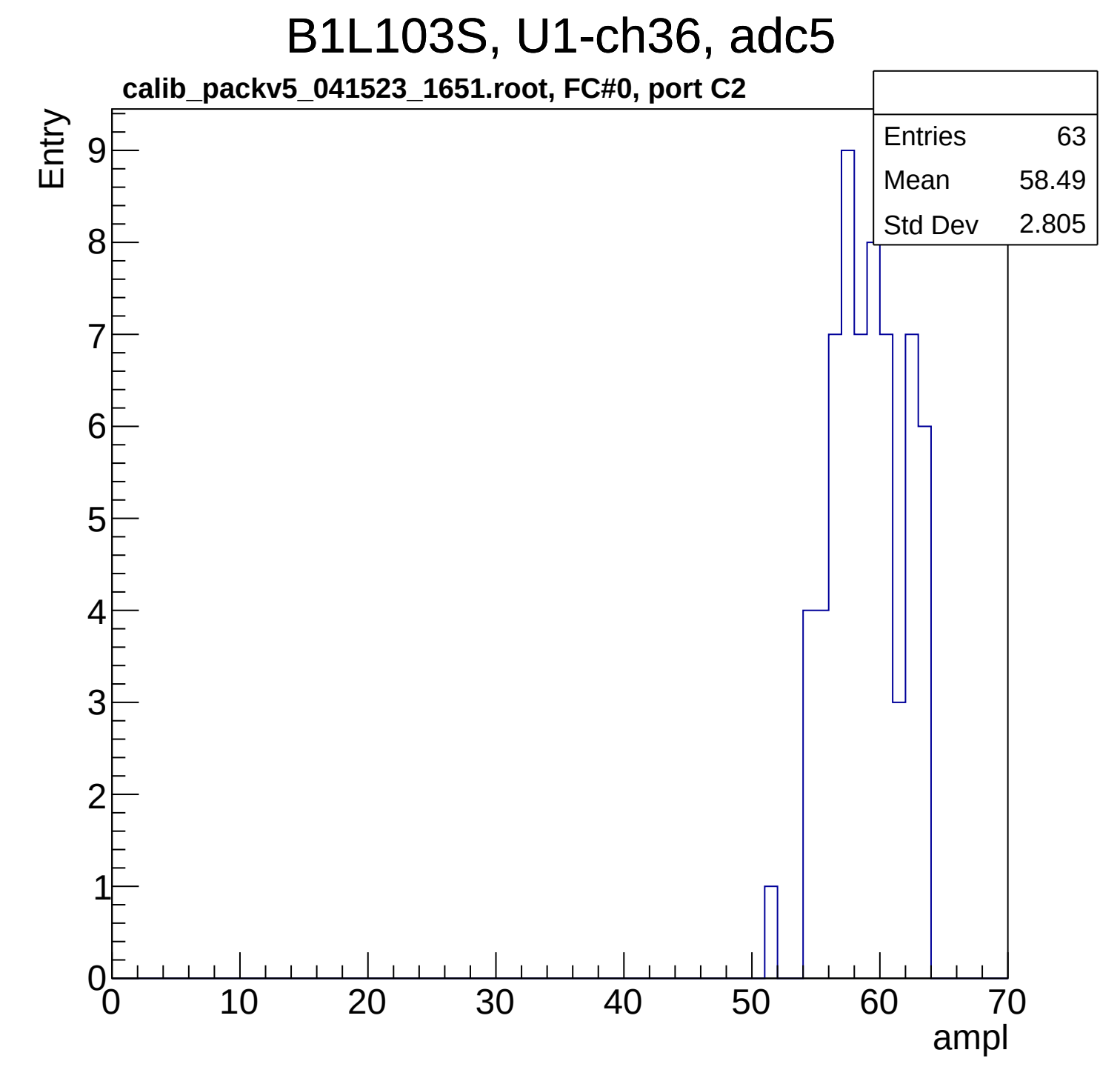
B1L103S, U1-ch36, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 58.49
Std Dev 2.805
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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40
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60
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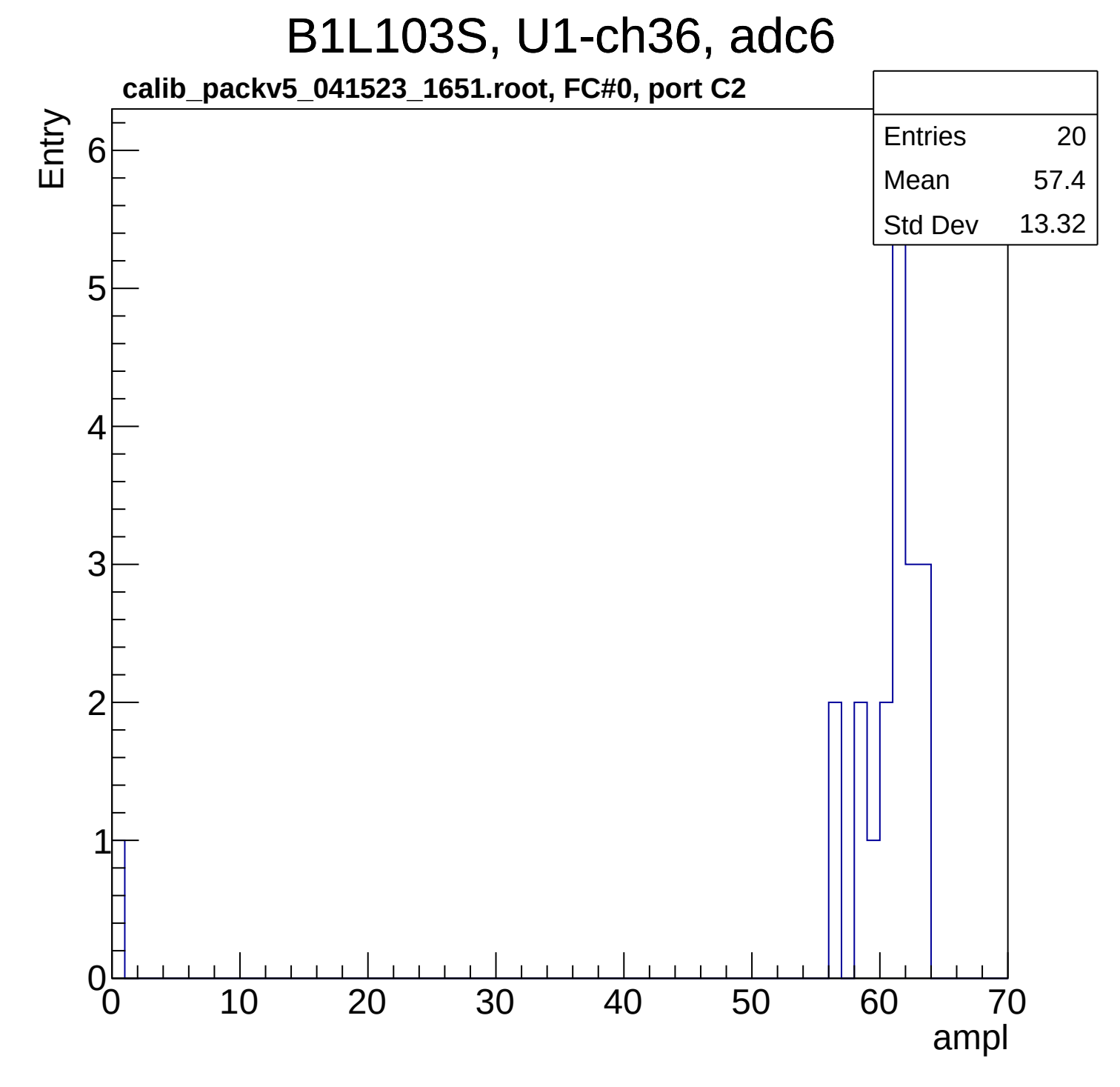
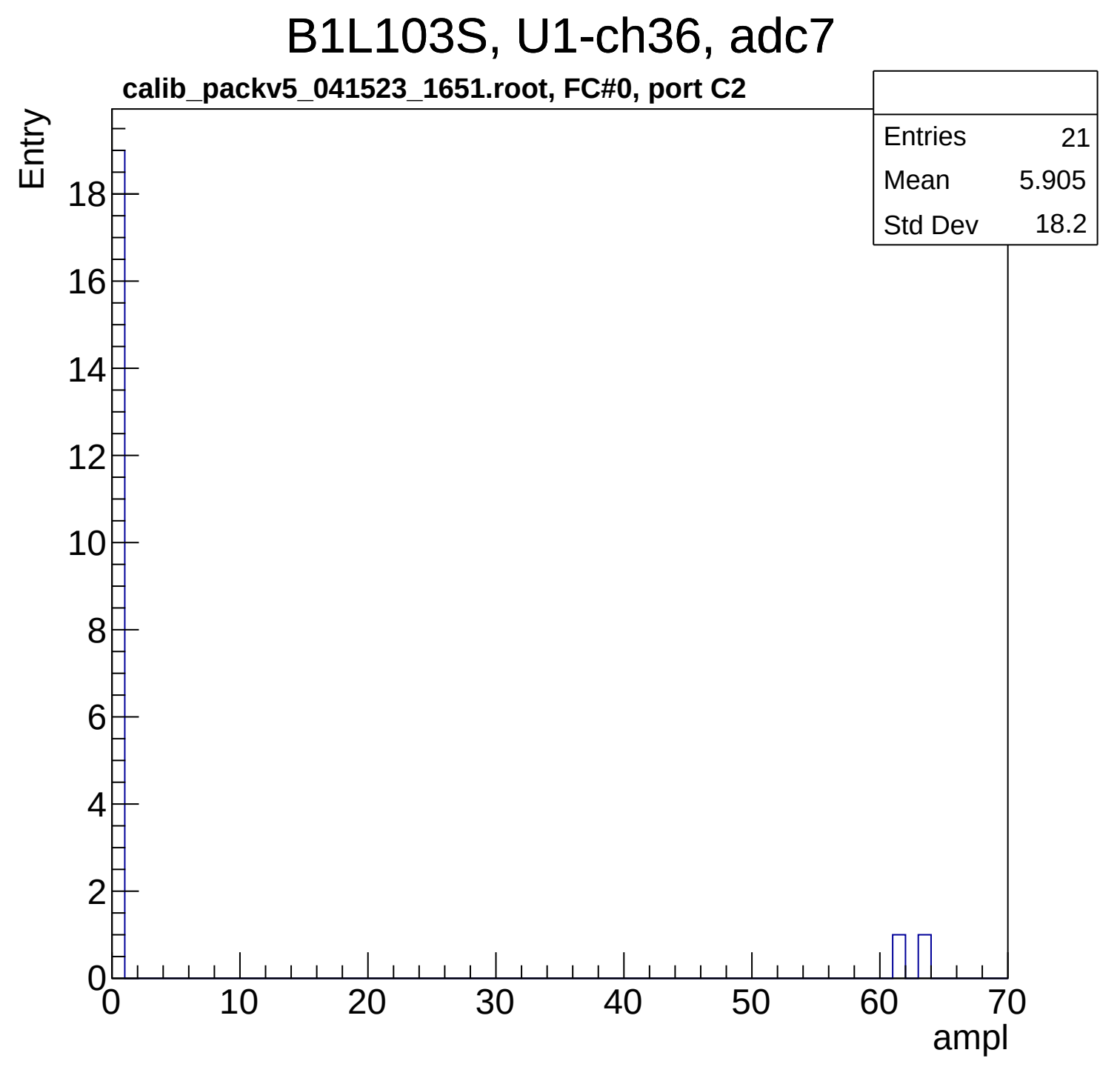

B1L103S, U1-ch36, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 57.4
Std Dev 13.32
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U1-ch36, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 5.905
Std Dev 18.2
Entry
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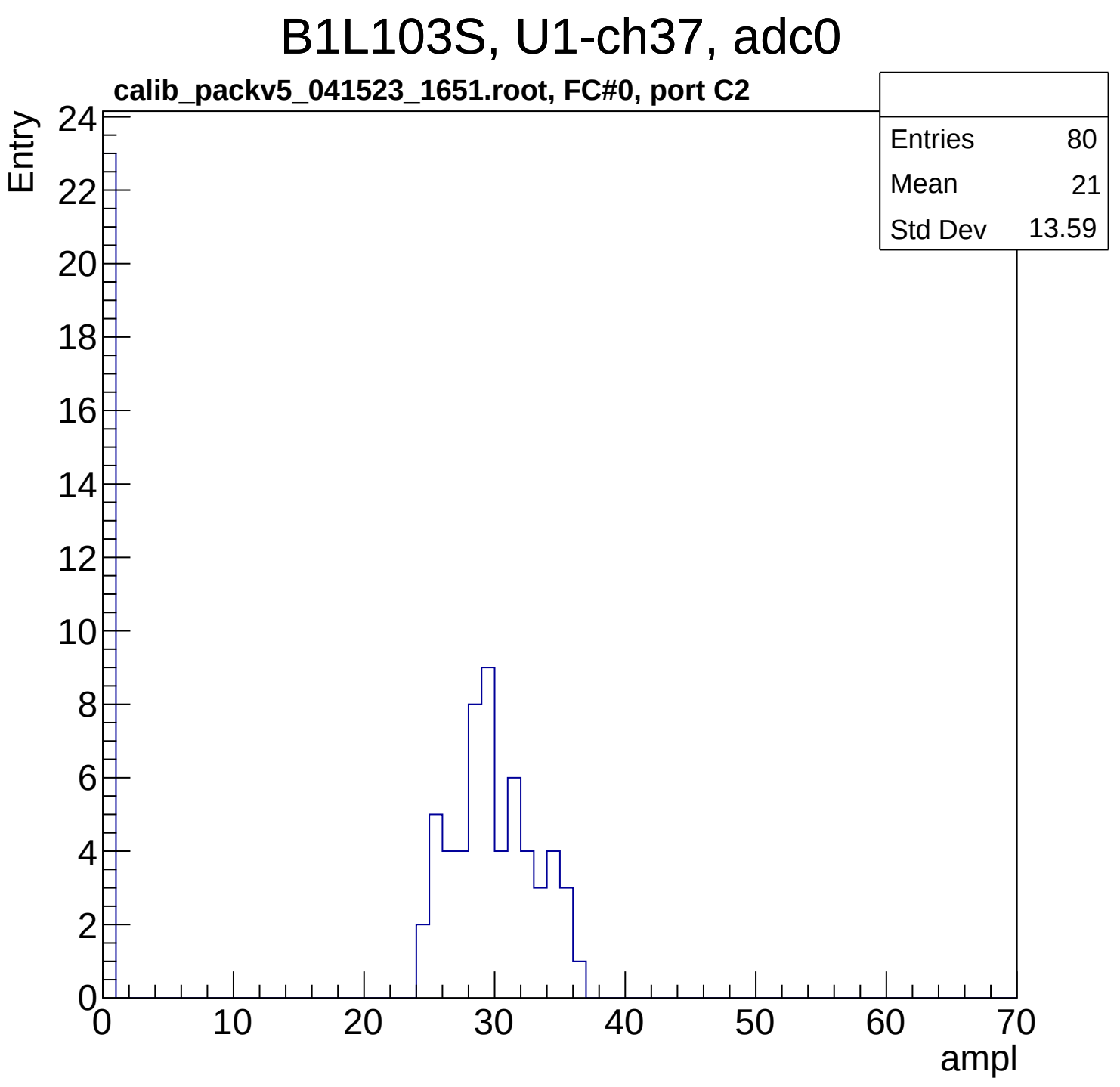
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch37, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 21
Std Dev 13.59
Entry
ampl
0
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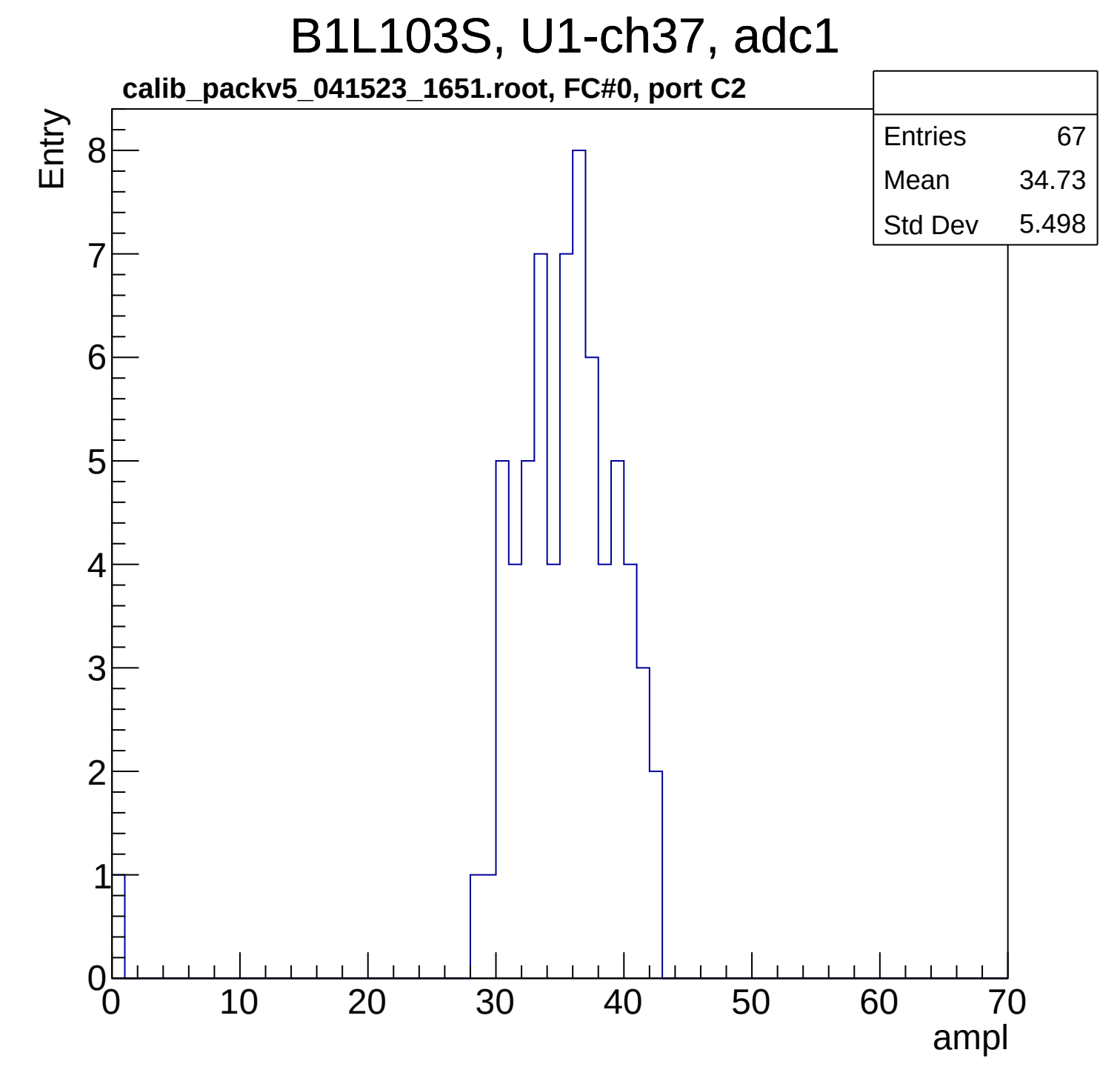
6
8
10
12
14
16
18
20
22
24
0
10
20
30
40
50
60
70


B1L103S, U1-ch37, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 34.73
Std Dev 5.498
Entry
ampl
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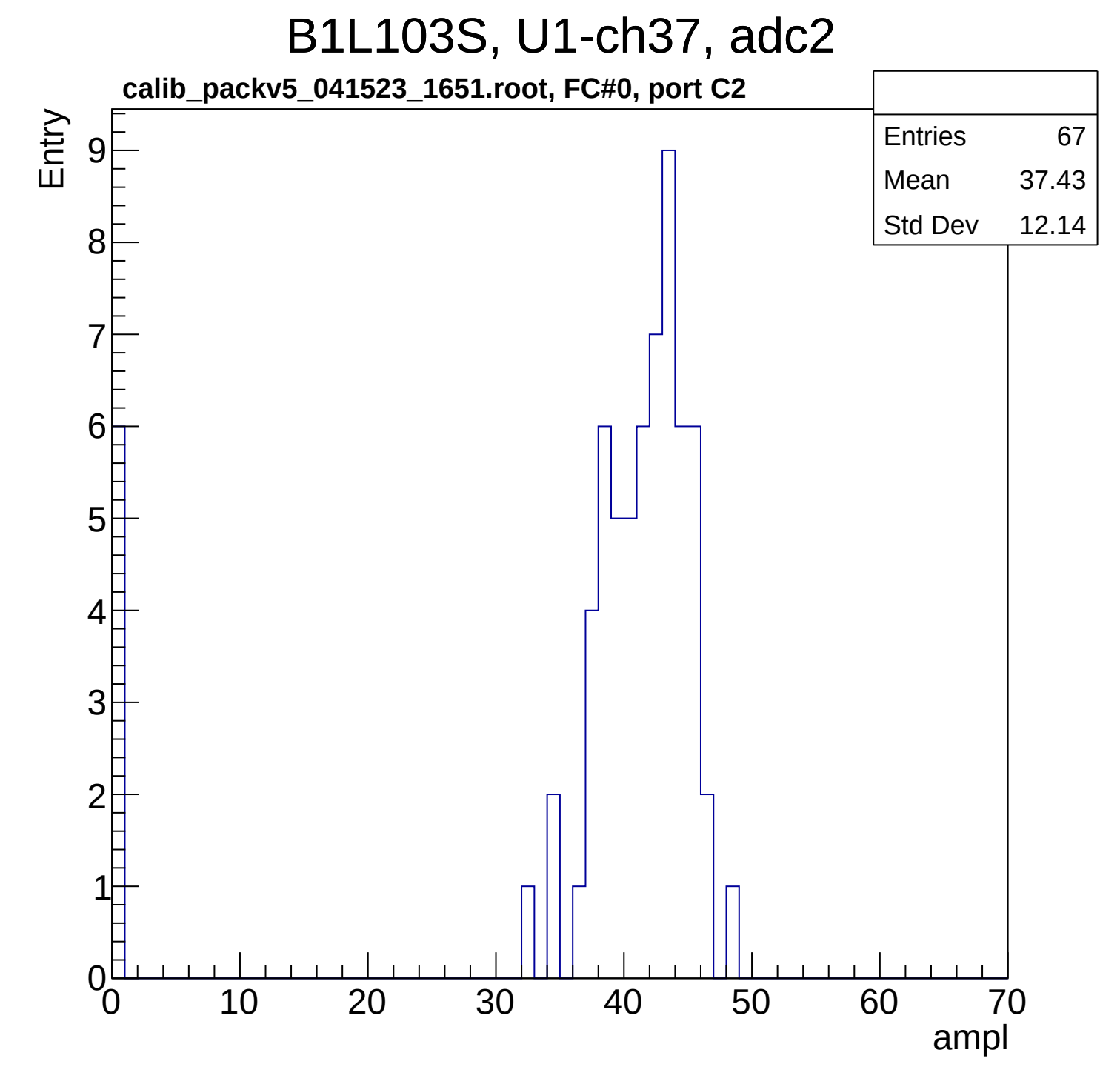
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U1-ch37, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 37.43
Std Dev 12.14
Entry
ampl
0
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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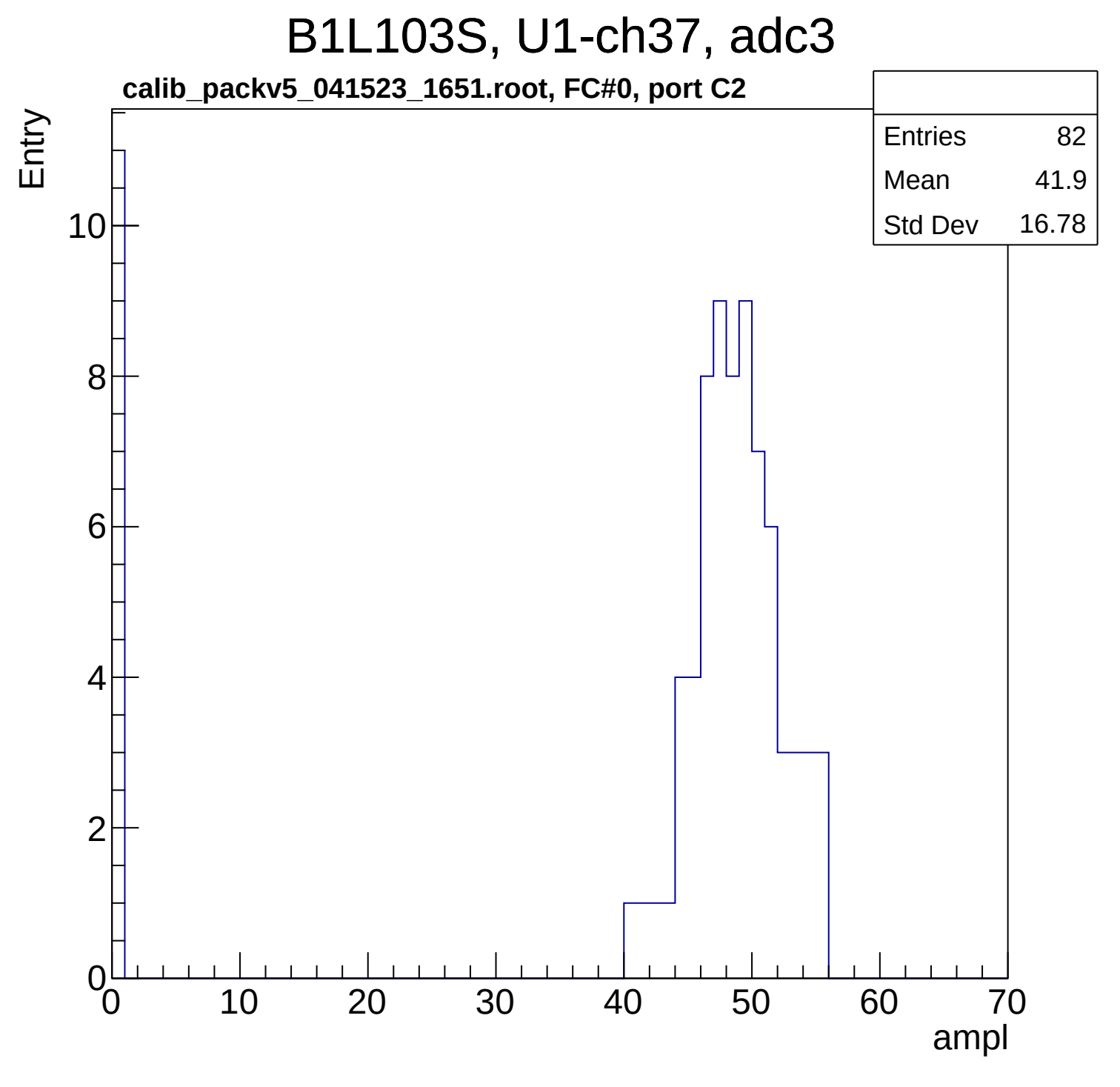
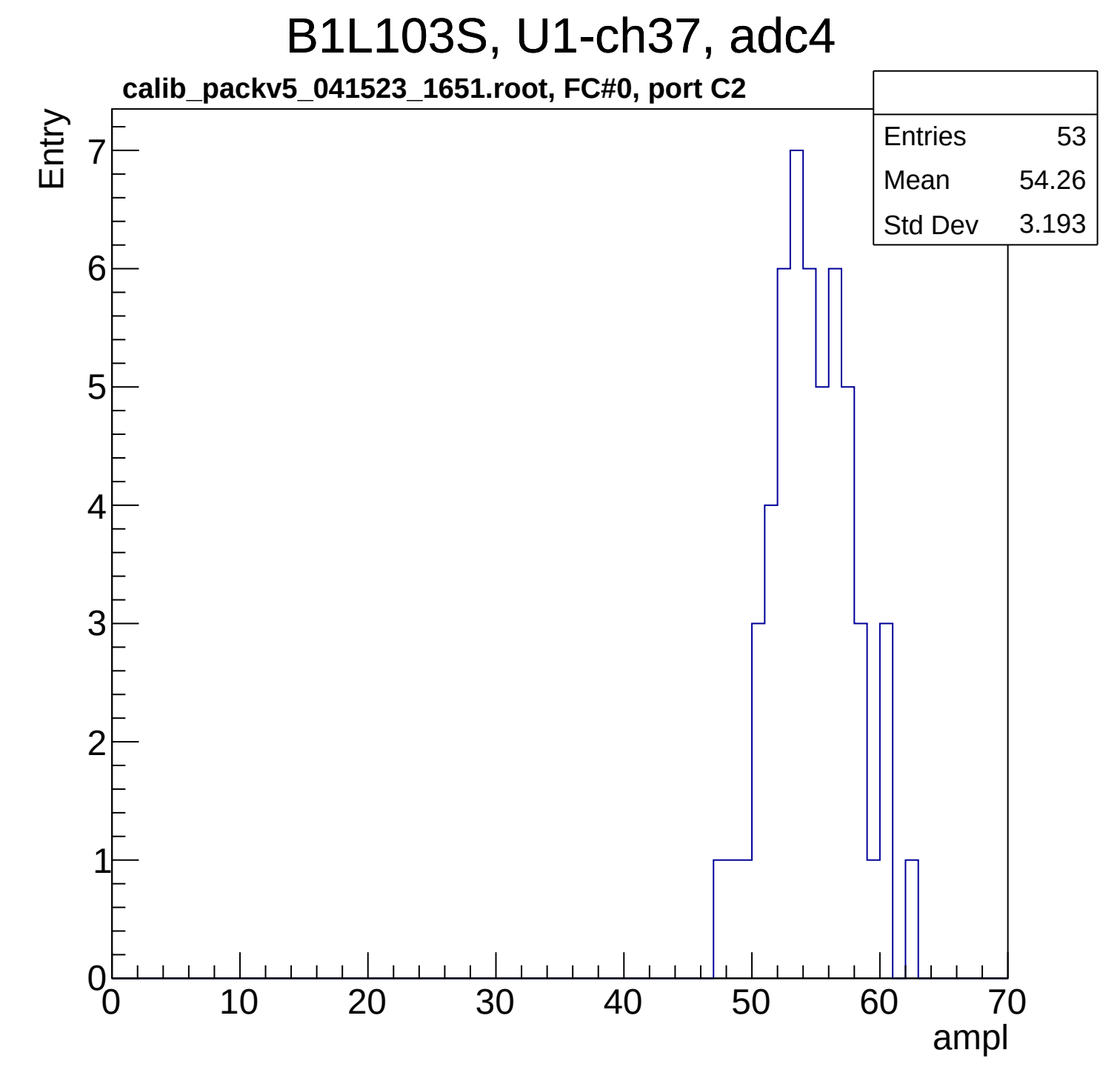
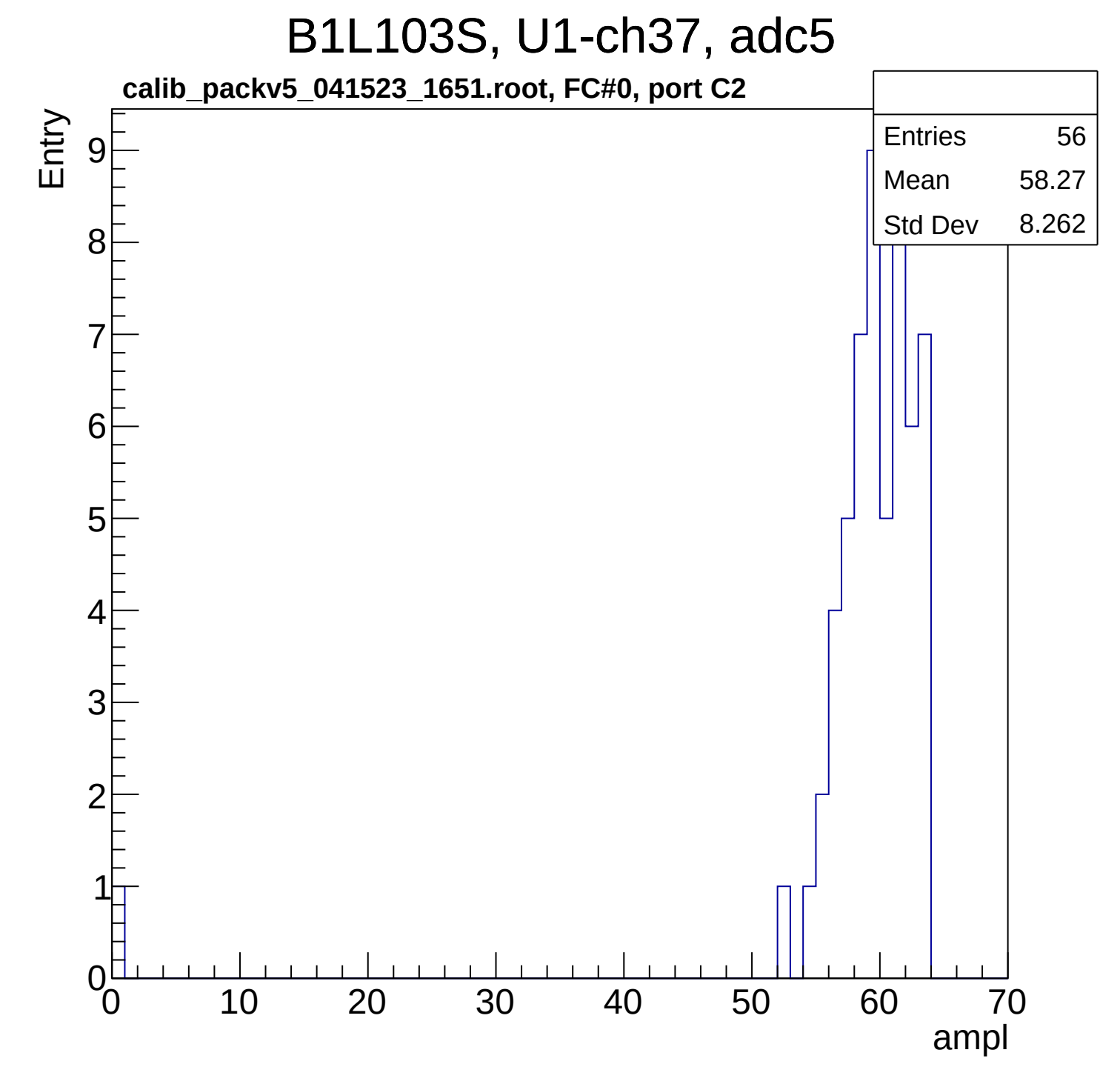

B1L103S, U1-ch37, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 41.9
Std Dev 16.78
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch37, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 54.26
Std Dev 3.193
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U1-ch37, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 58.27
Std Dev 8.262
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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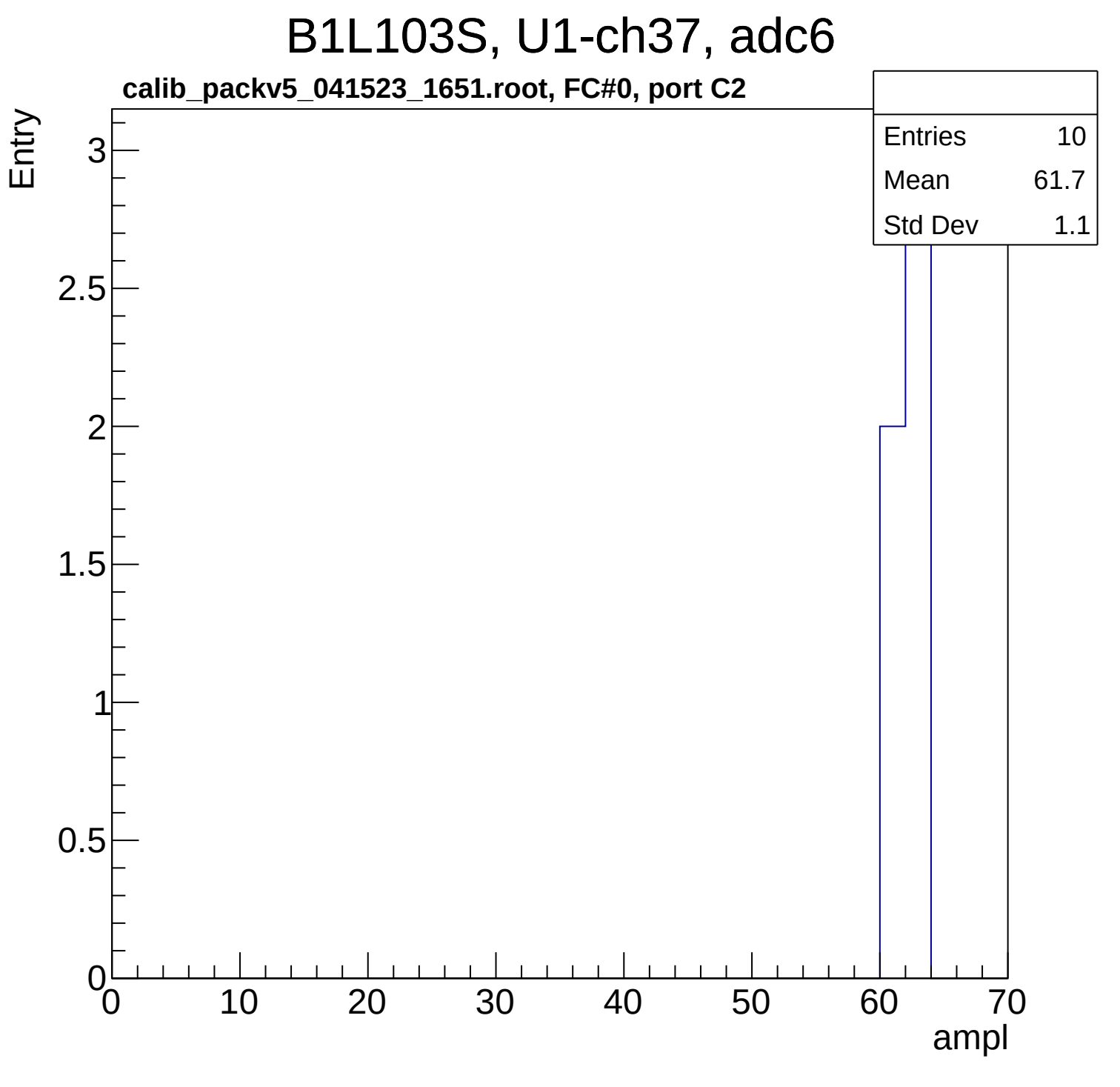
B1L103S, U1-ch37, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 61.7
Std Dev 1.1
Entry
ampl
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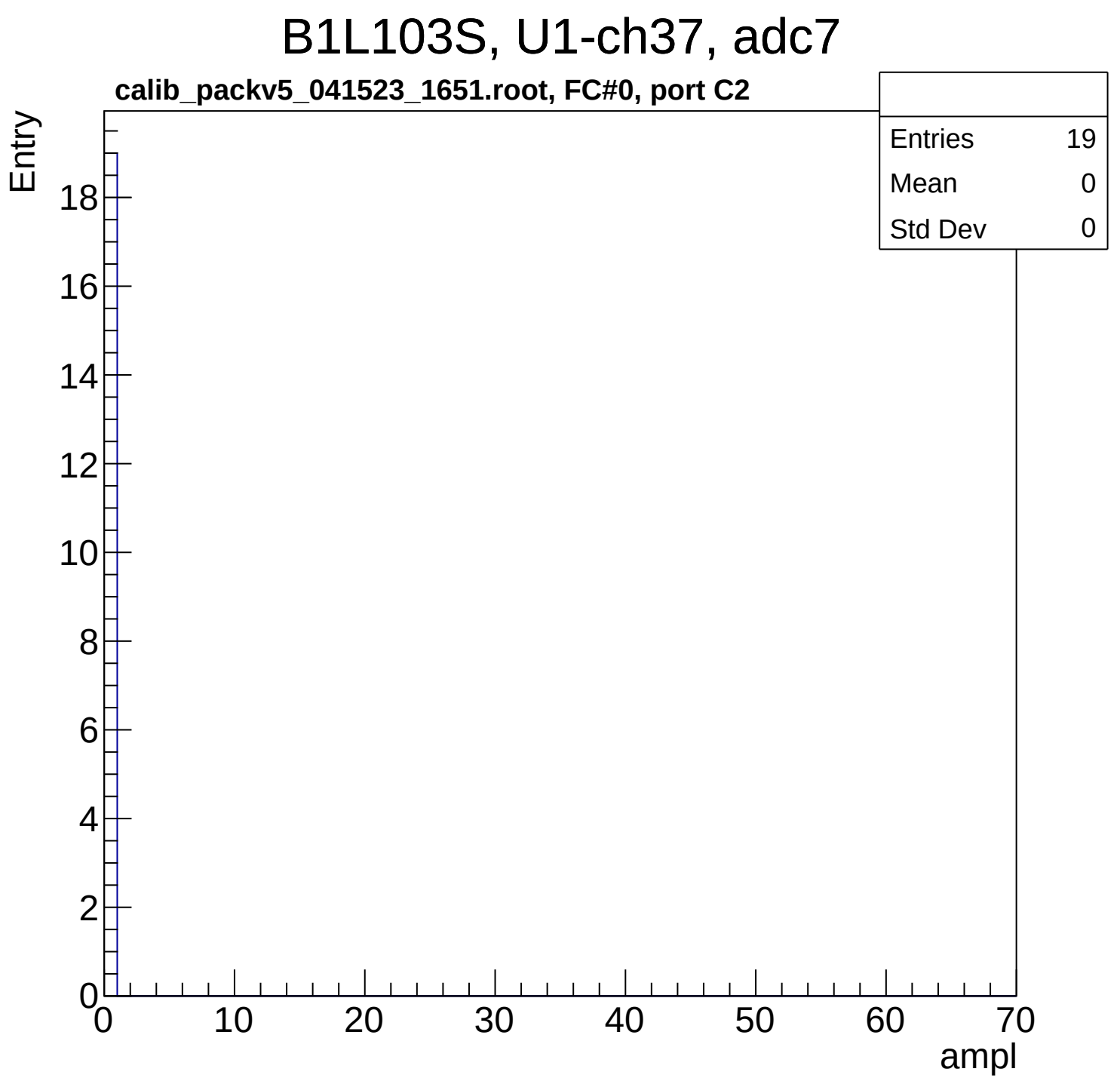
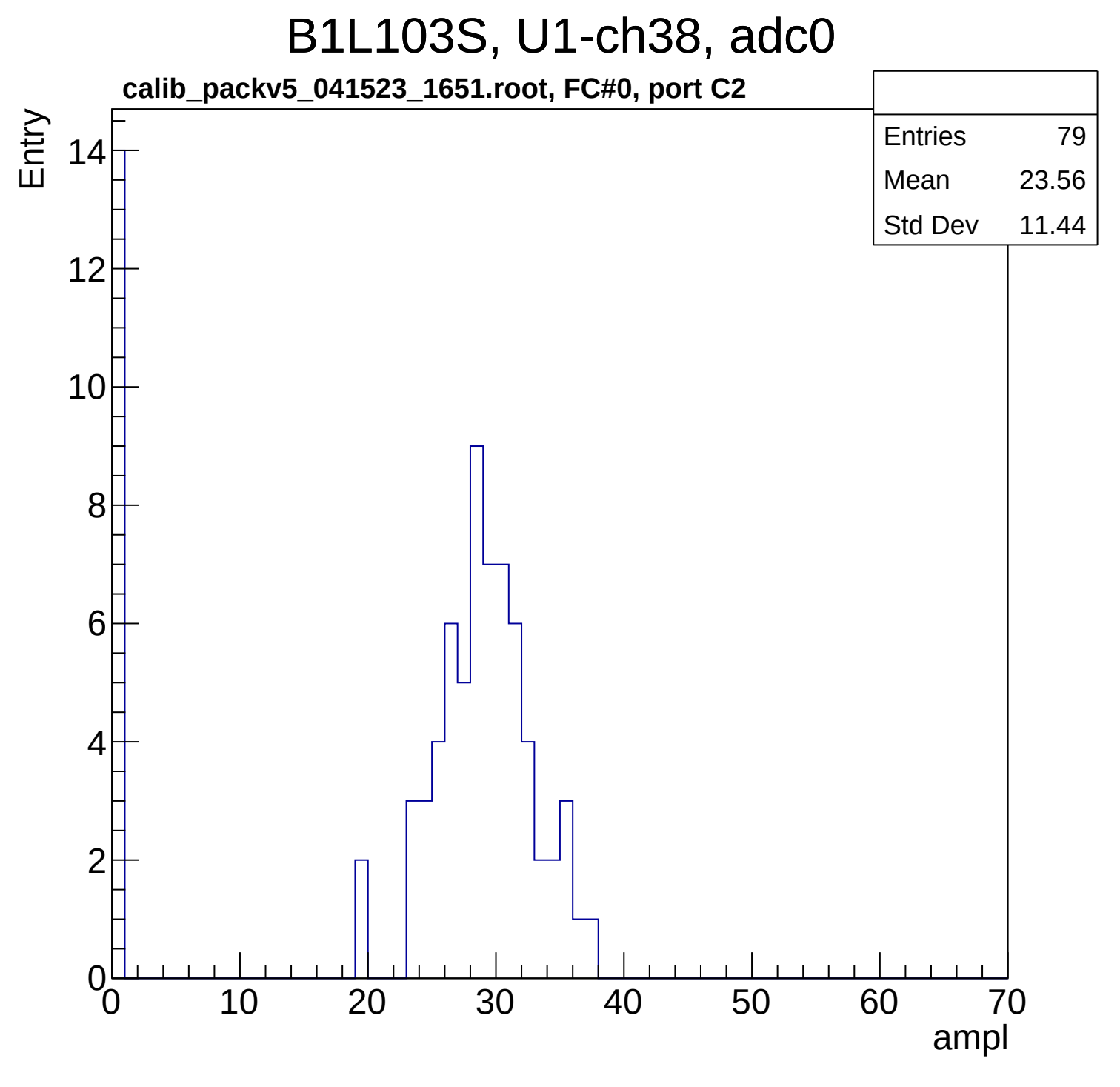
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U1-ch37, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch38, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 23.56
Std Dev 11.44
Entry
ampl
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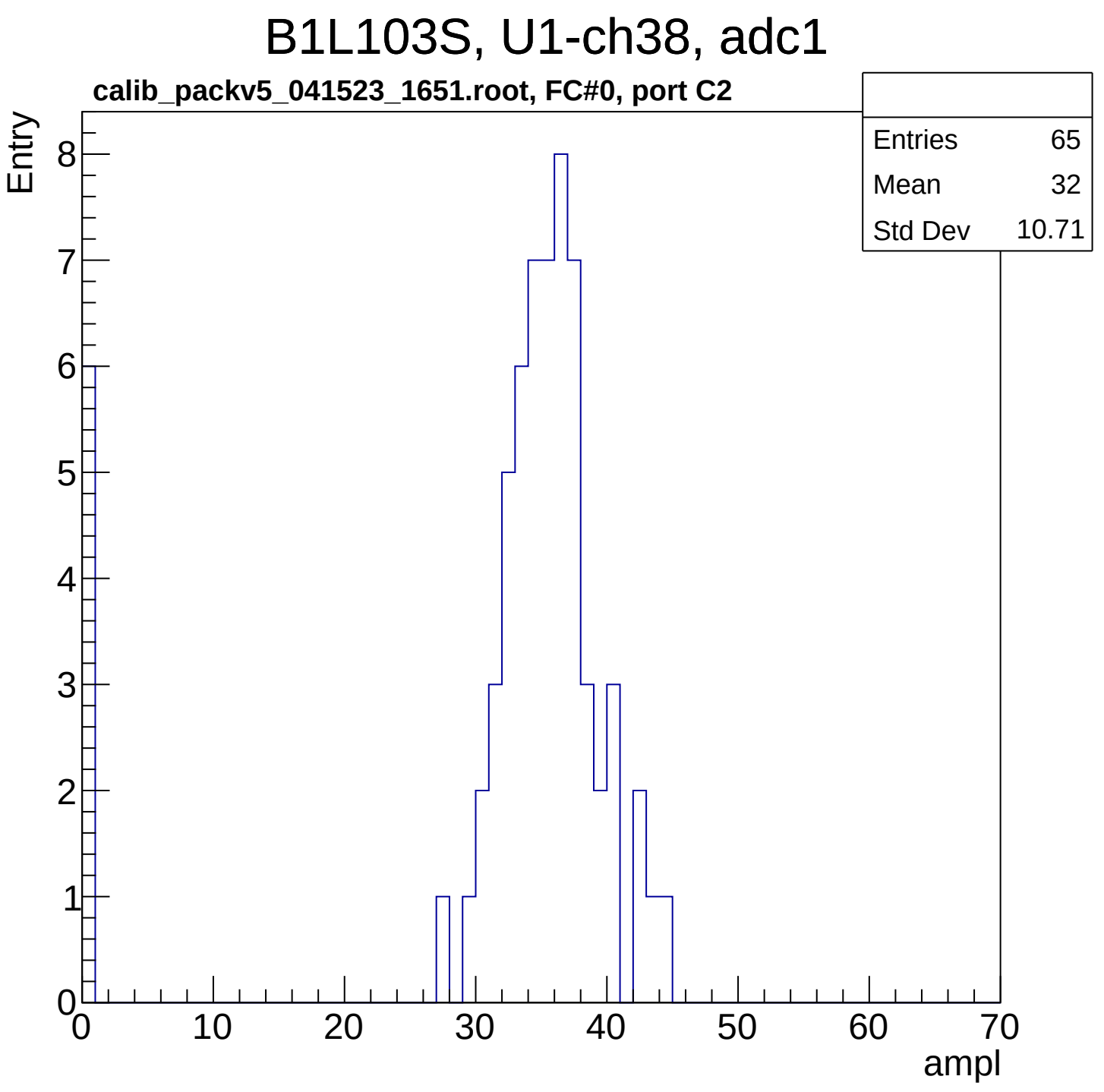
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L103S, U1-ch38, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 32
Std Dev 10.71
Entry
ampl
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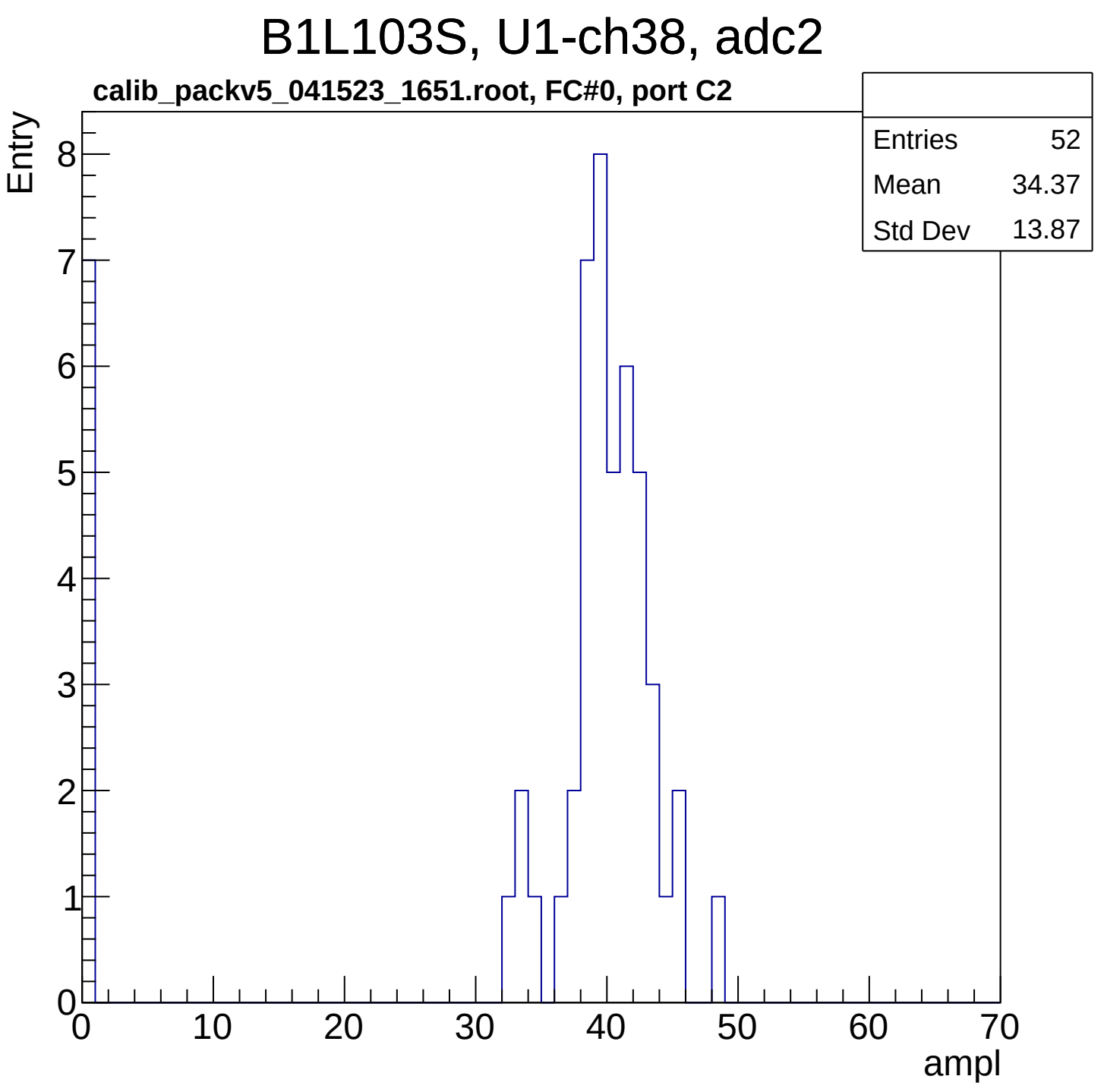
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U1-ch38, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 34.37
Std Dev 13.87
Entry
ampl
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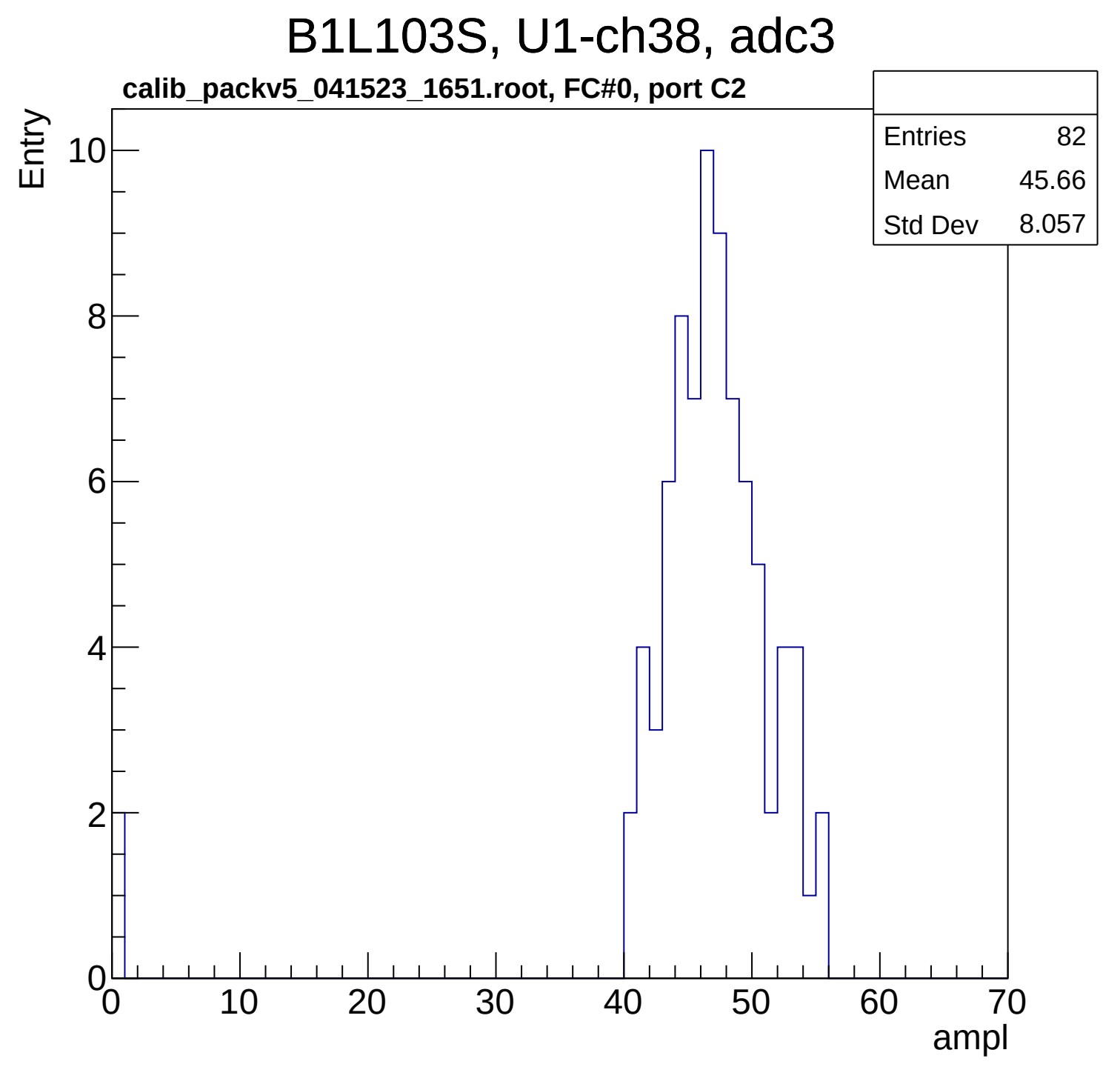
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U1-ch38, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 45.66
Std Dev 8.057
Entry
ampl
0
2
4
6
8
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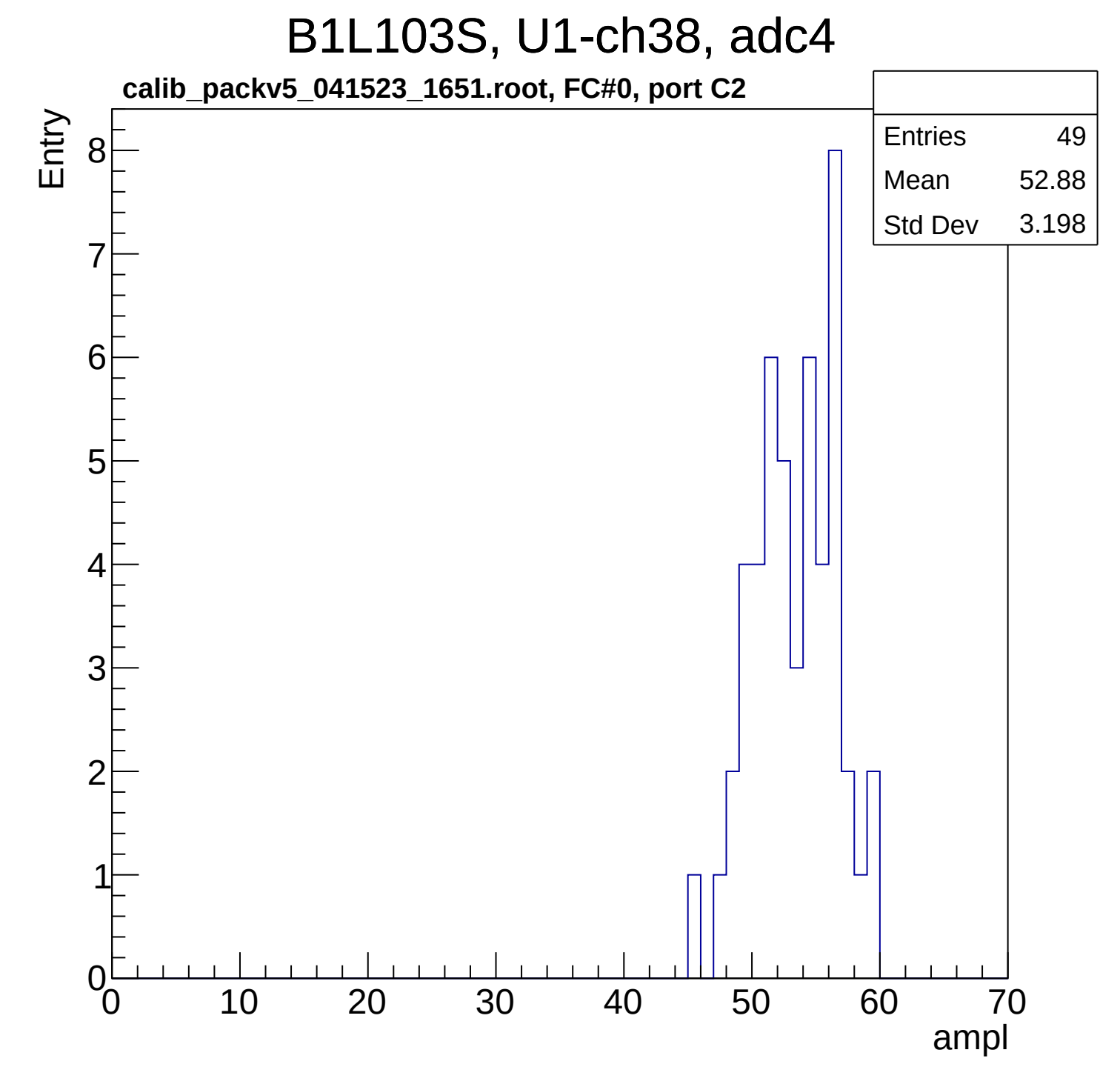
0
10
20
30
40
50
60
70


B1L103S, U1-ch38, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 52.88
Std Dev 3.198
Entry
ampl
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2
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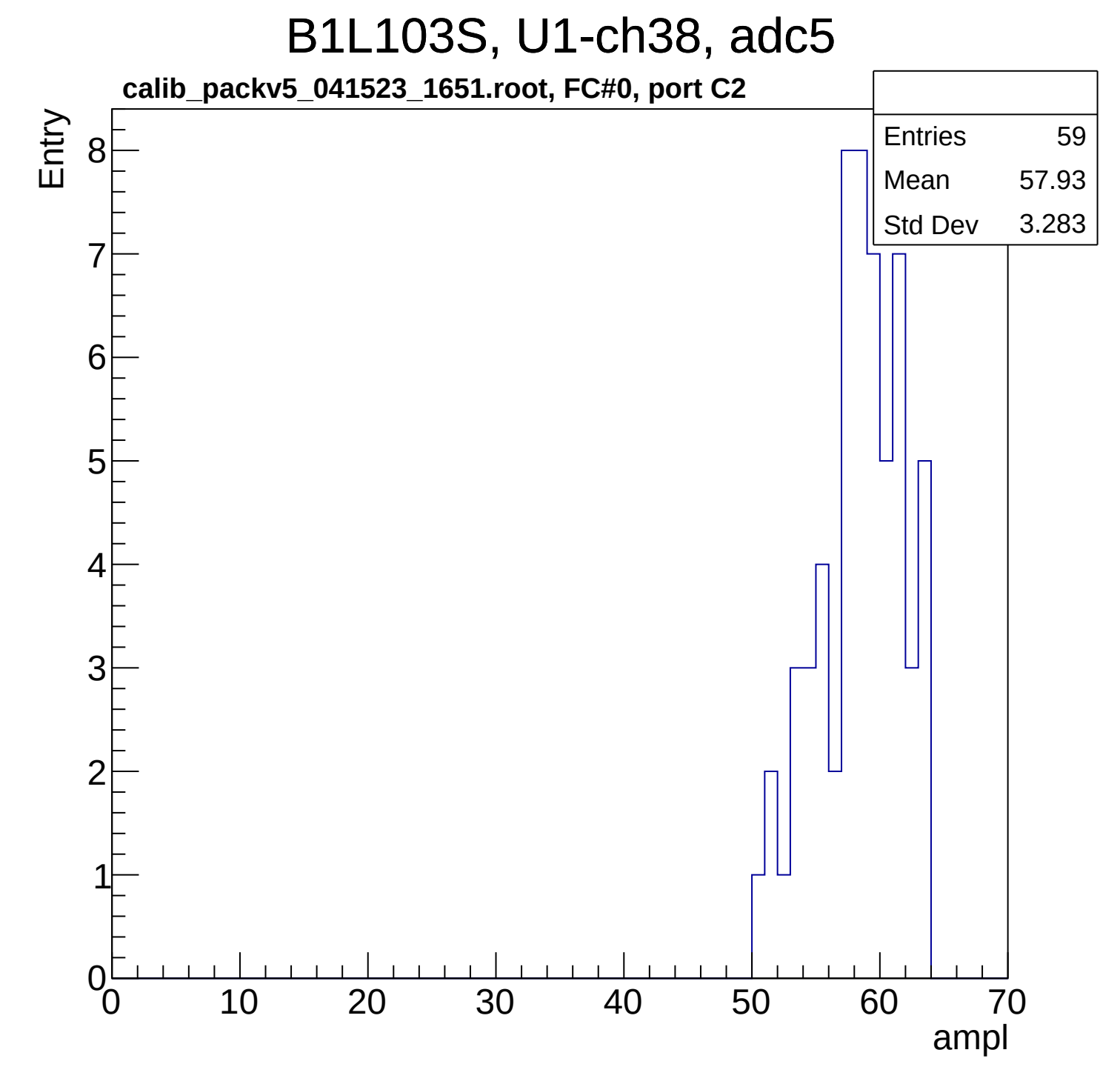
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U1-ch38, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 57.93
Std Dev 3.283
Entry
ampl
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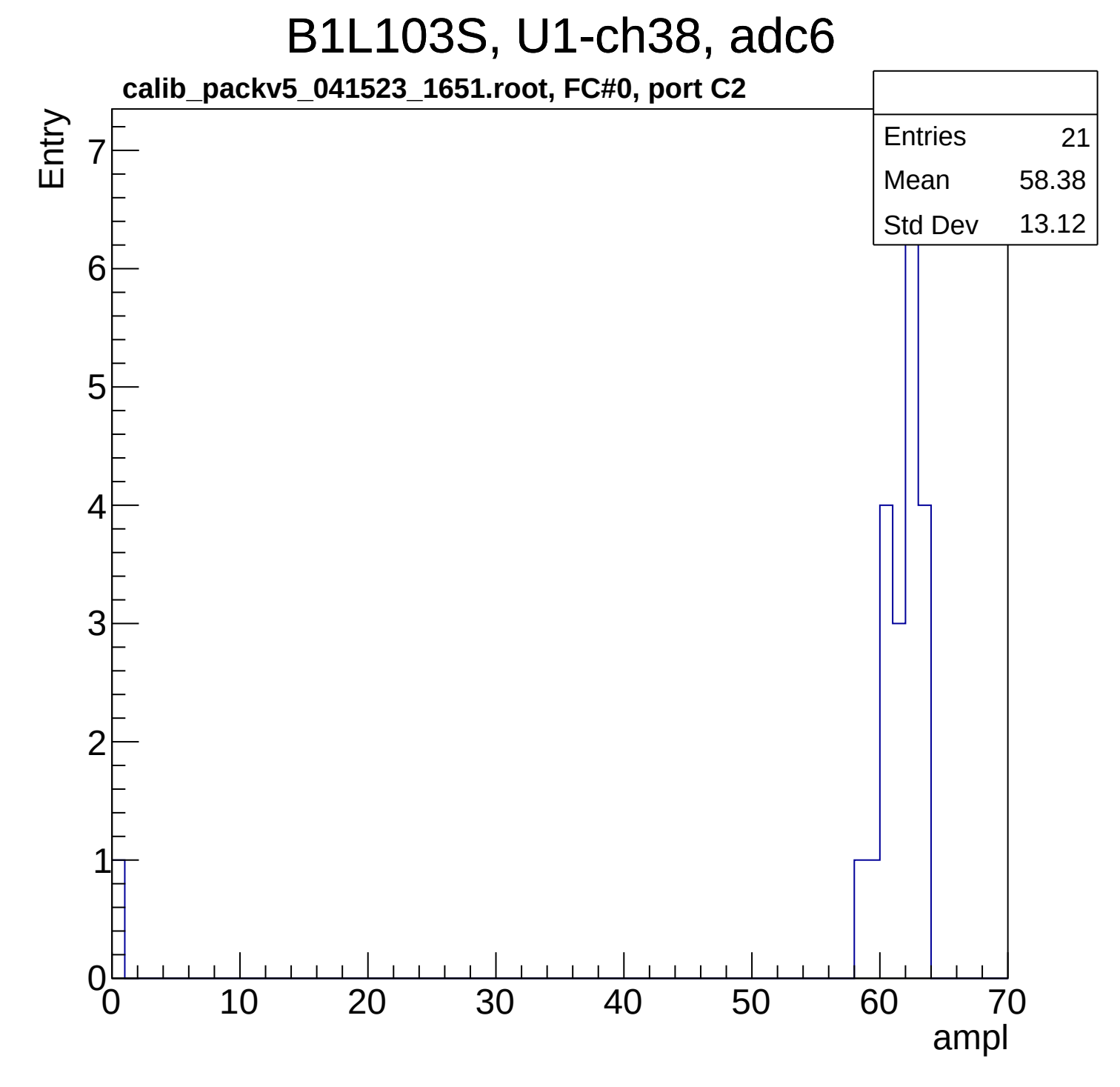
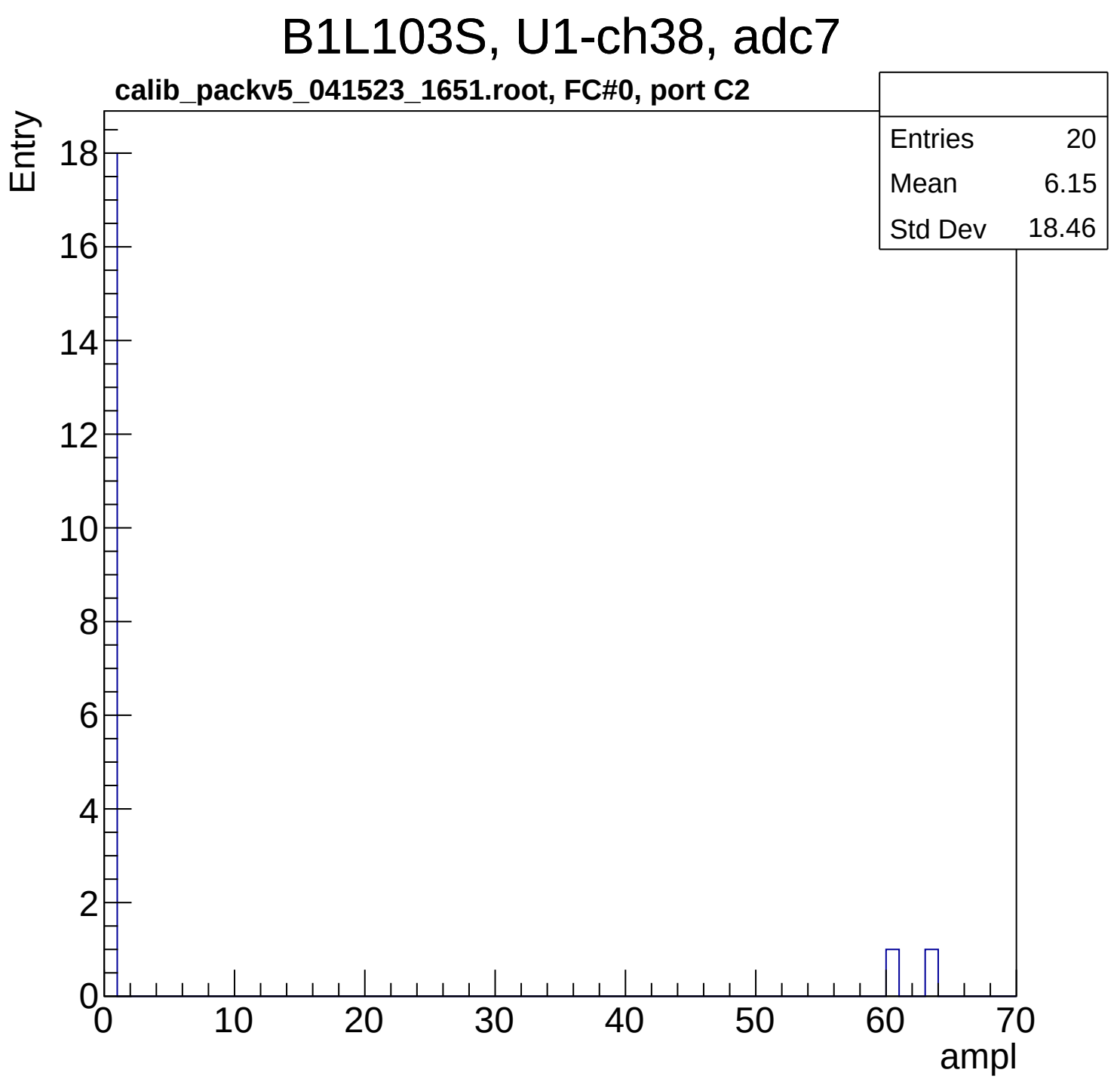
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U1-ch38, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 58.38
Std Dev 13.12
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U1-ch38, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 6.15
Std Dev 18.46
Entry
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10
12
14
16
18
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10
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30
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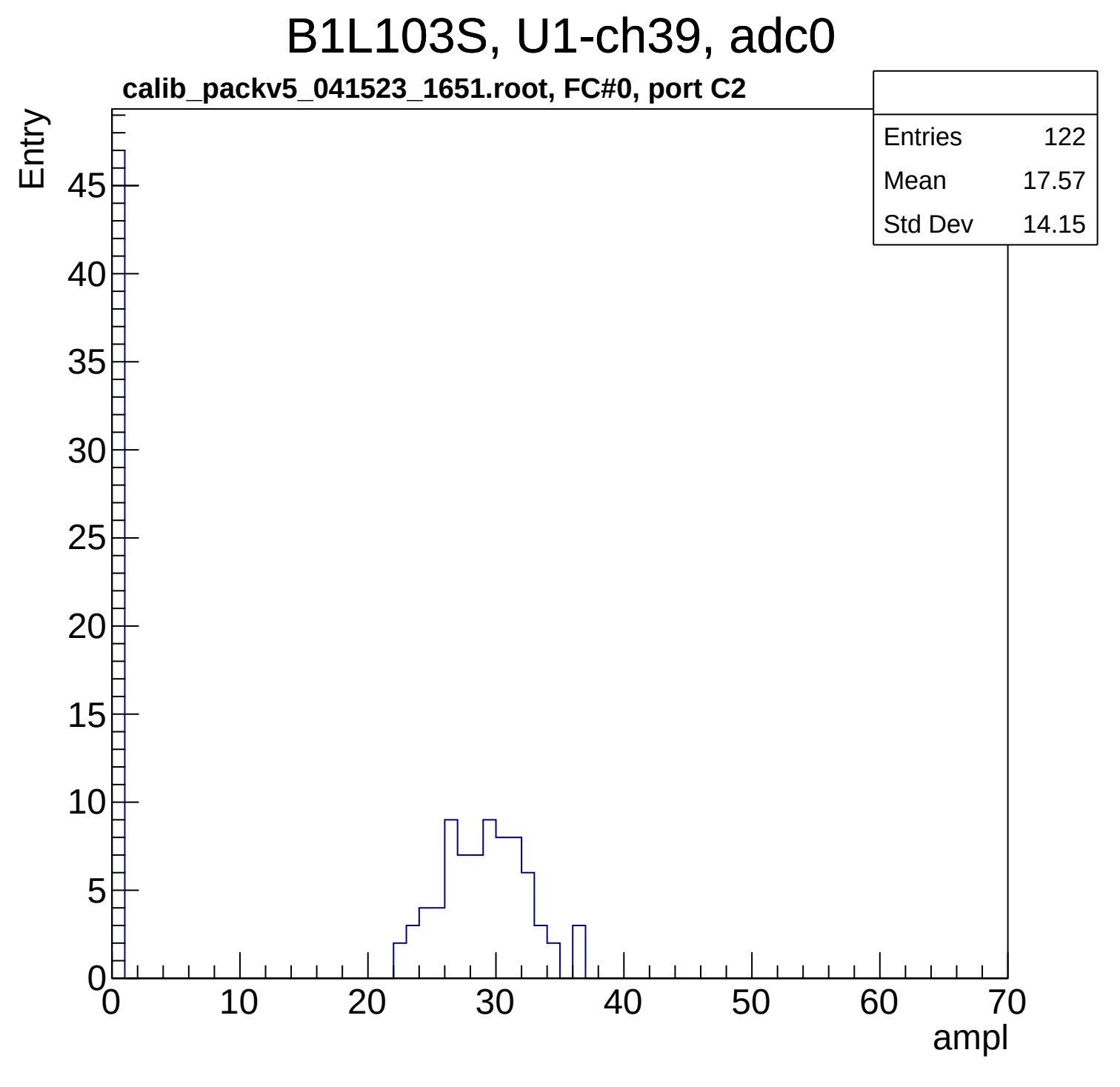
50
60
70
ampl


B1L103S, U1-ch39, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 122
Mean 17.57
Std Dev 14.15
Entry
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15
20
25
30
35
40
45
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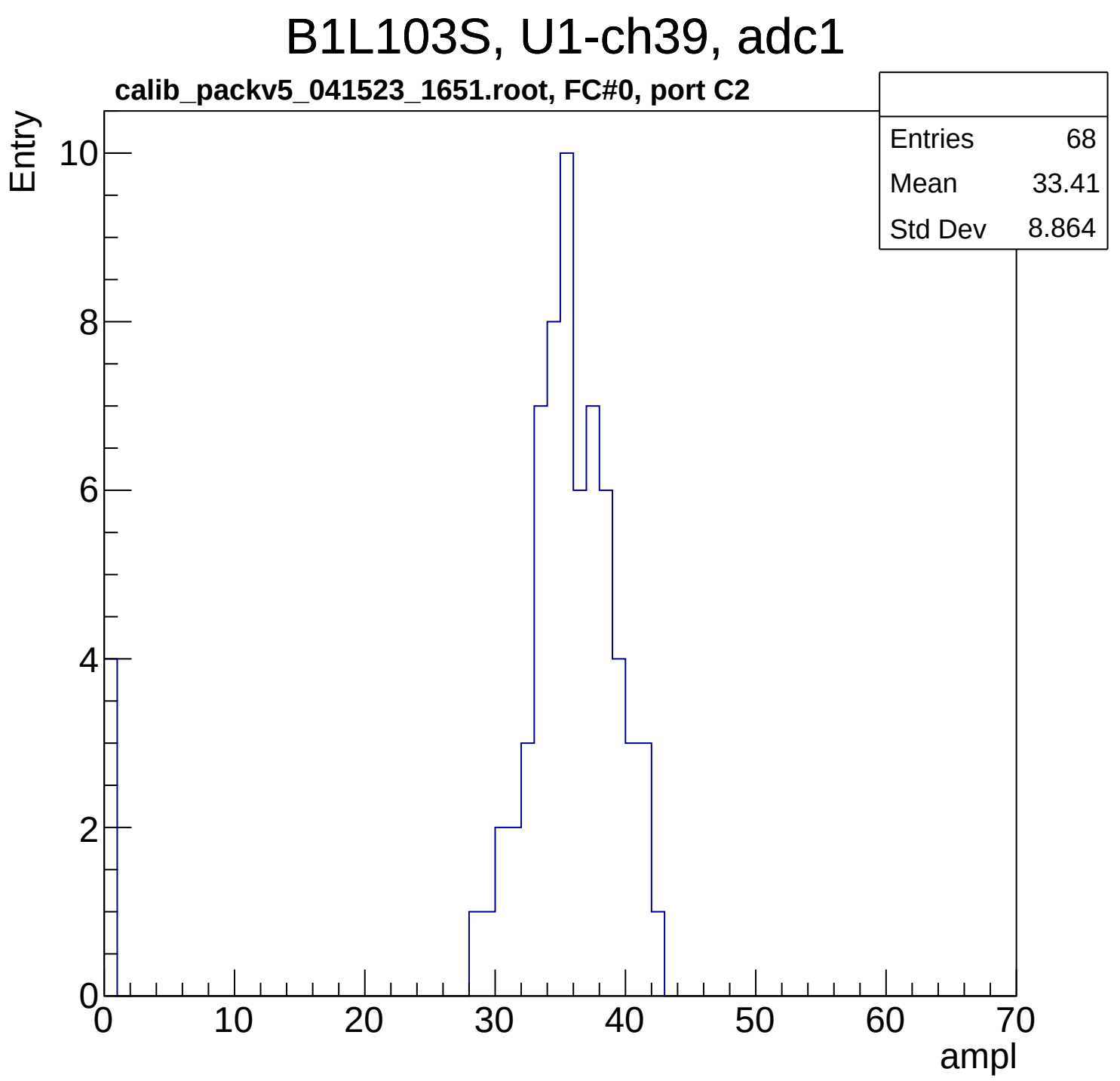
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch39, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 33.41
Std Dev 8.864
Entry
ampl
0
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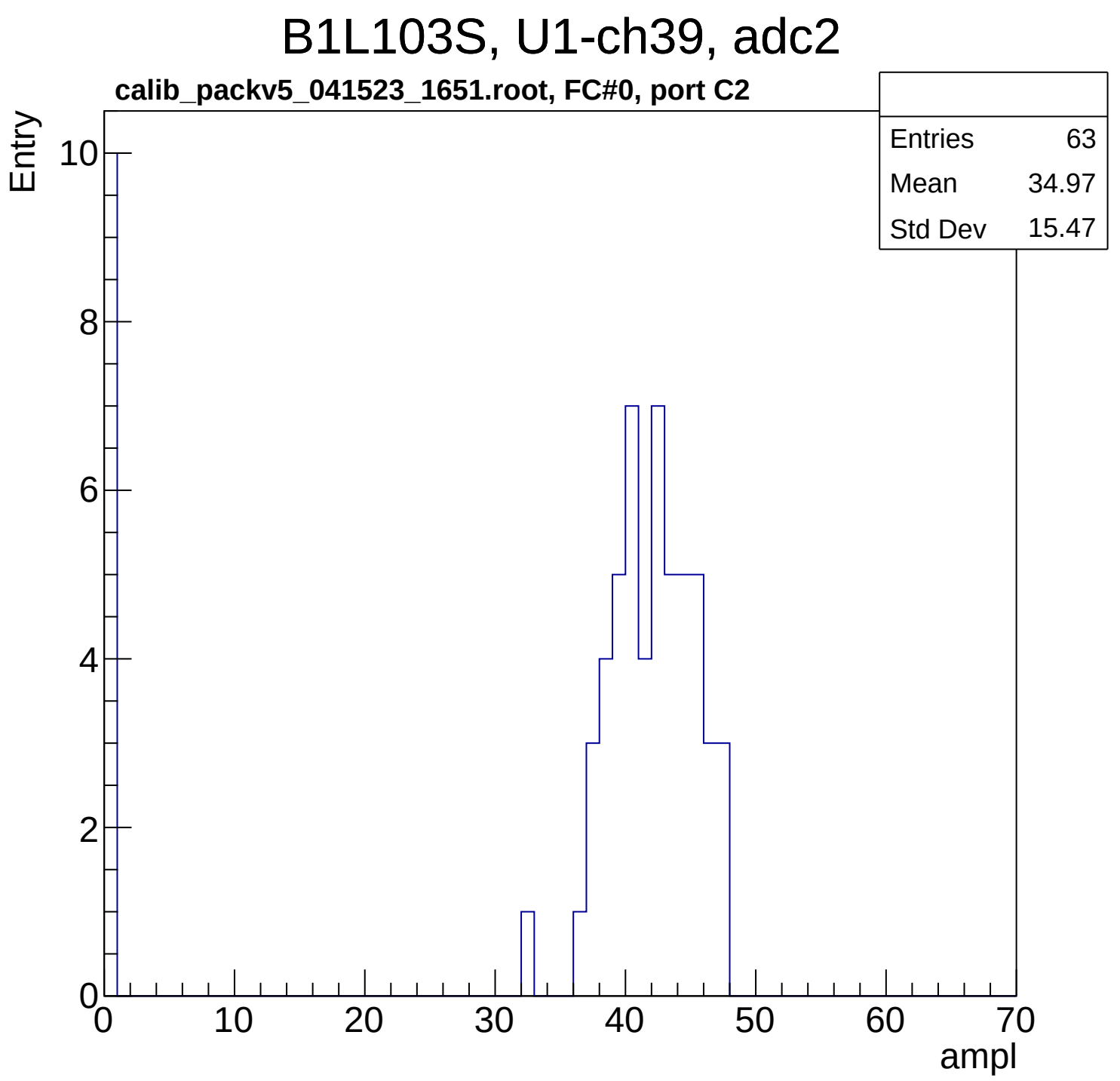
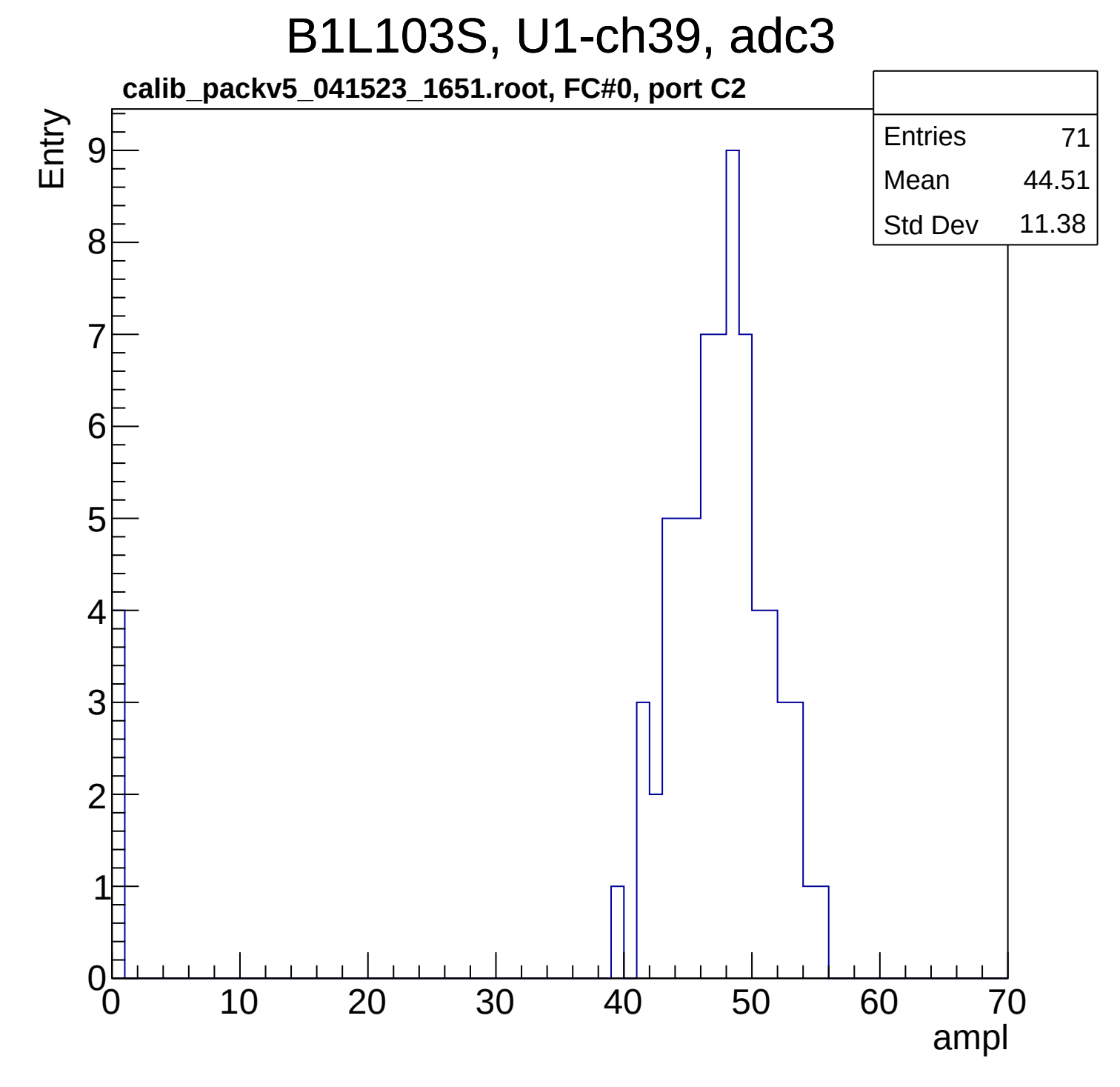
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U1-ch39, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 34.97
Std Dev 15.47
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch39, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 44.51
Std Dev 11.38
Entry
ampl
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2
3
4
5
6
7
8
9
0
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40
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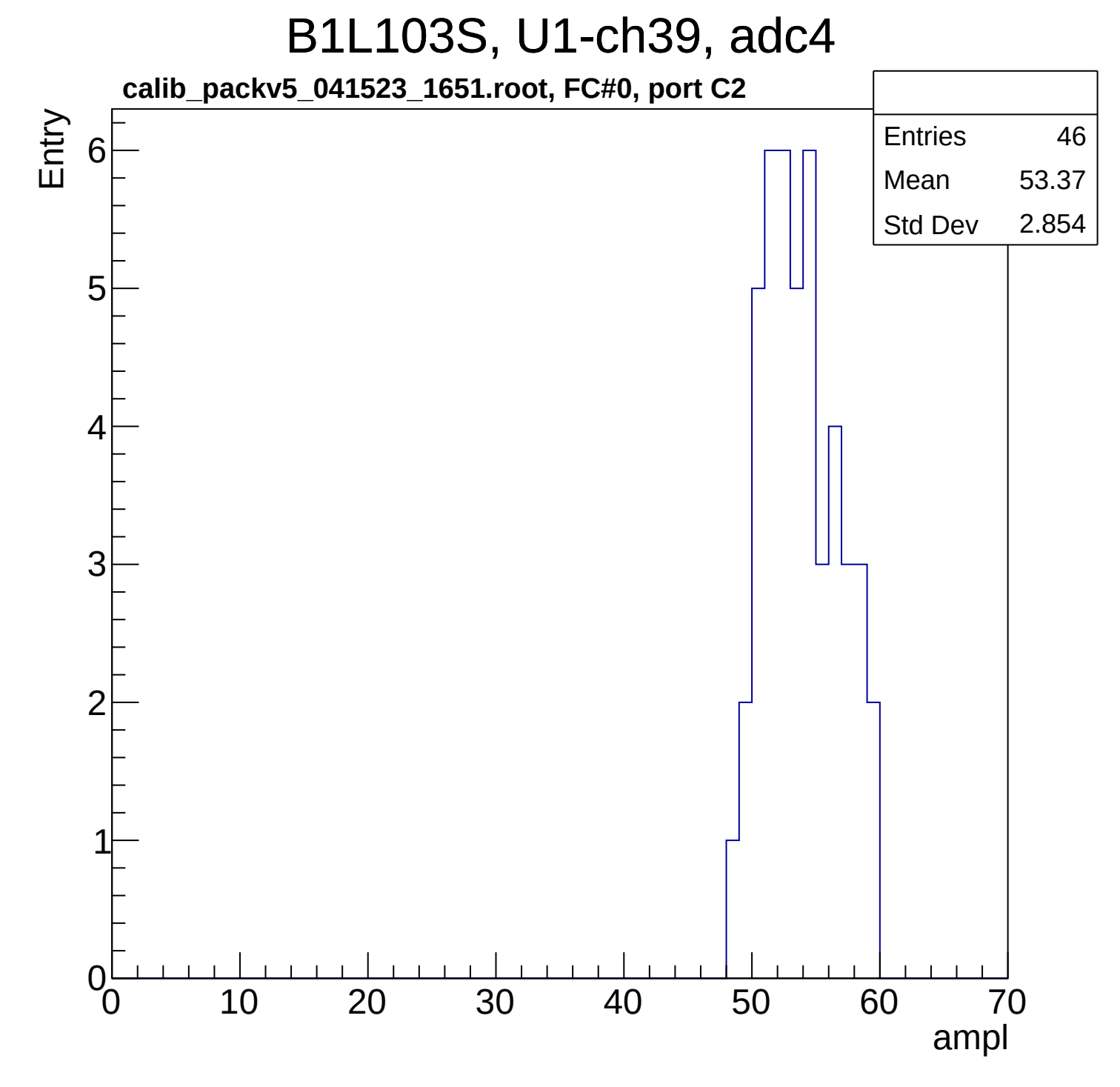
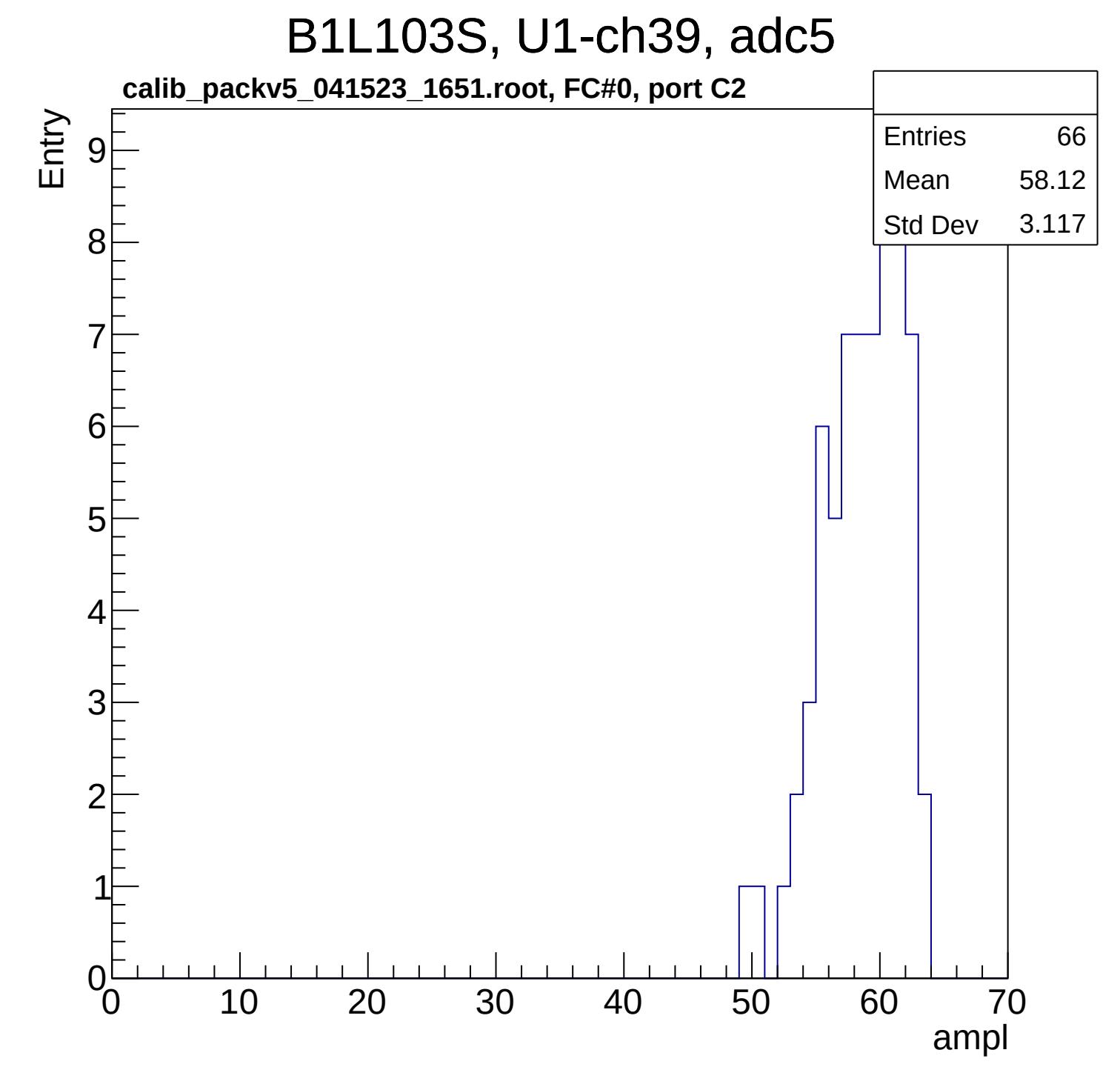
60
70


B1L103S, U1-ch39, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 53.37
Std Dev 2.854
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U1-ch39, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 58.12
Std Dev 3.117
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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40
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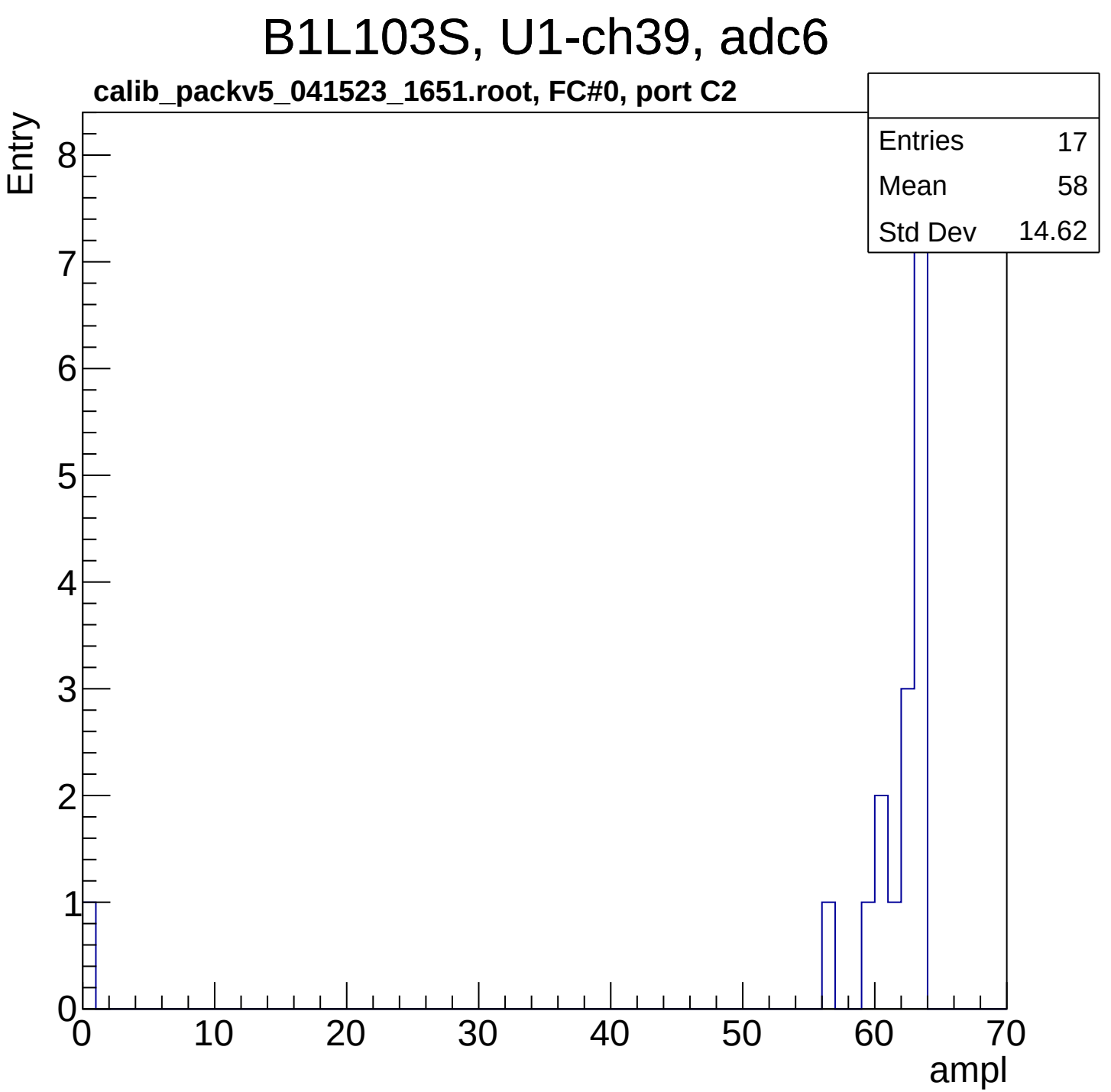
B1L103S, U1-ch39, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 17
Mean 58
Std Dev 14.62
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
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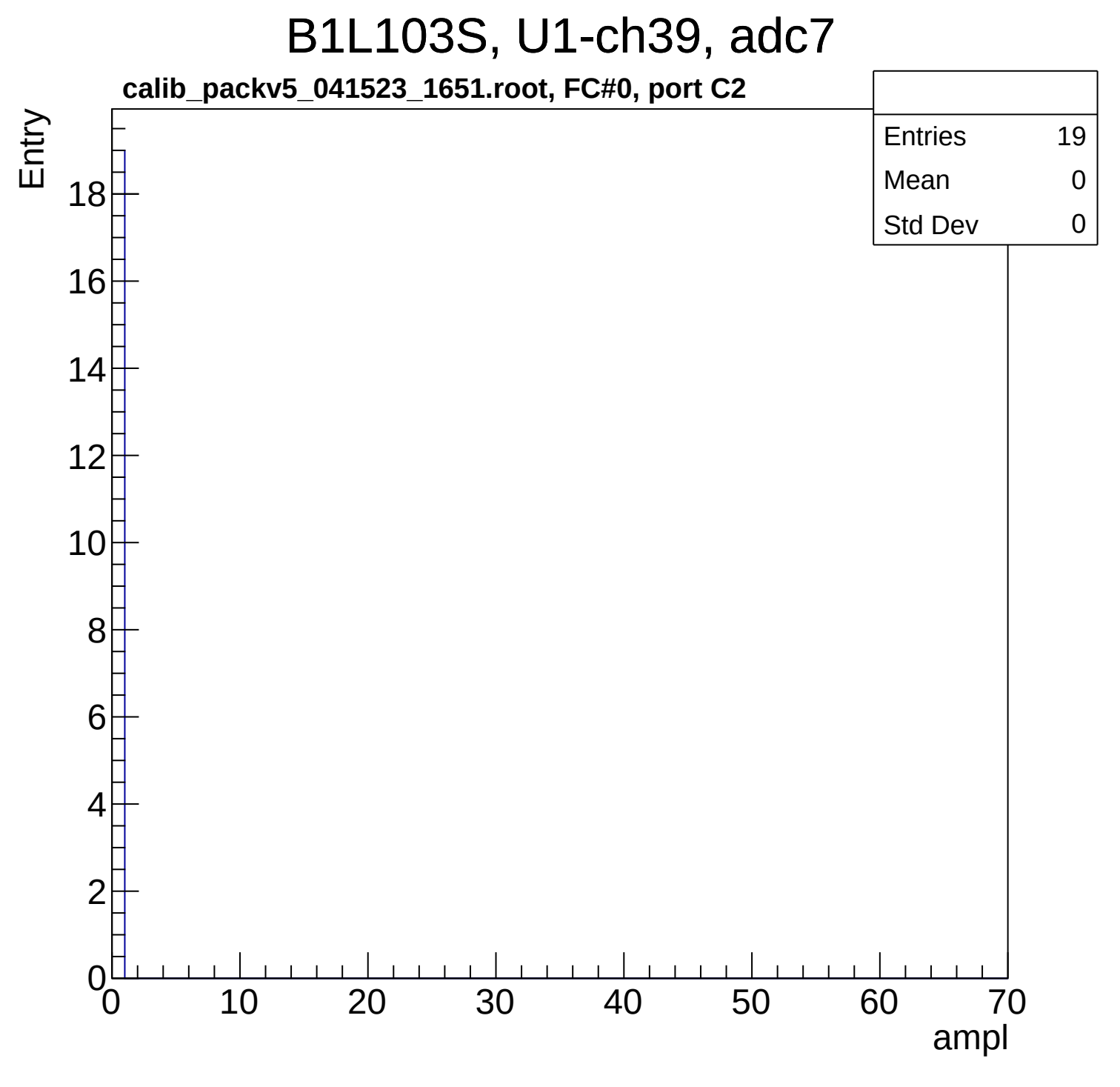
40
50
60
70


B1L103S, U1-ch39, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
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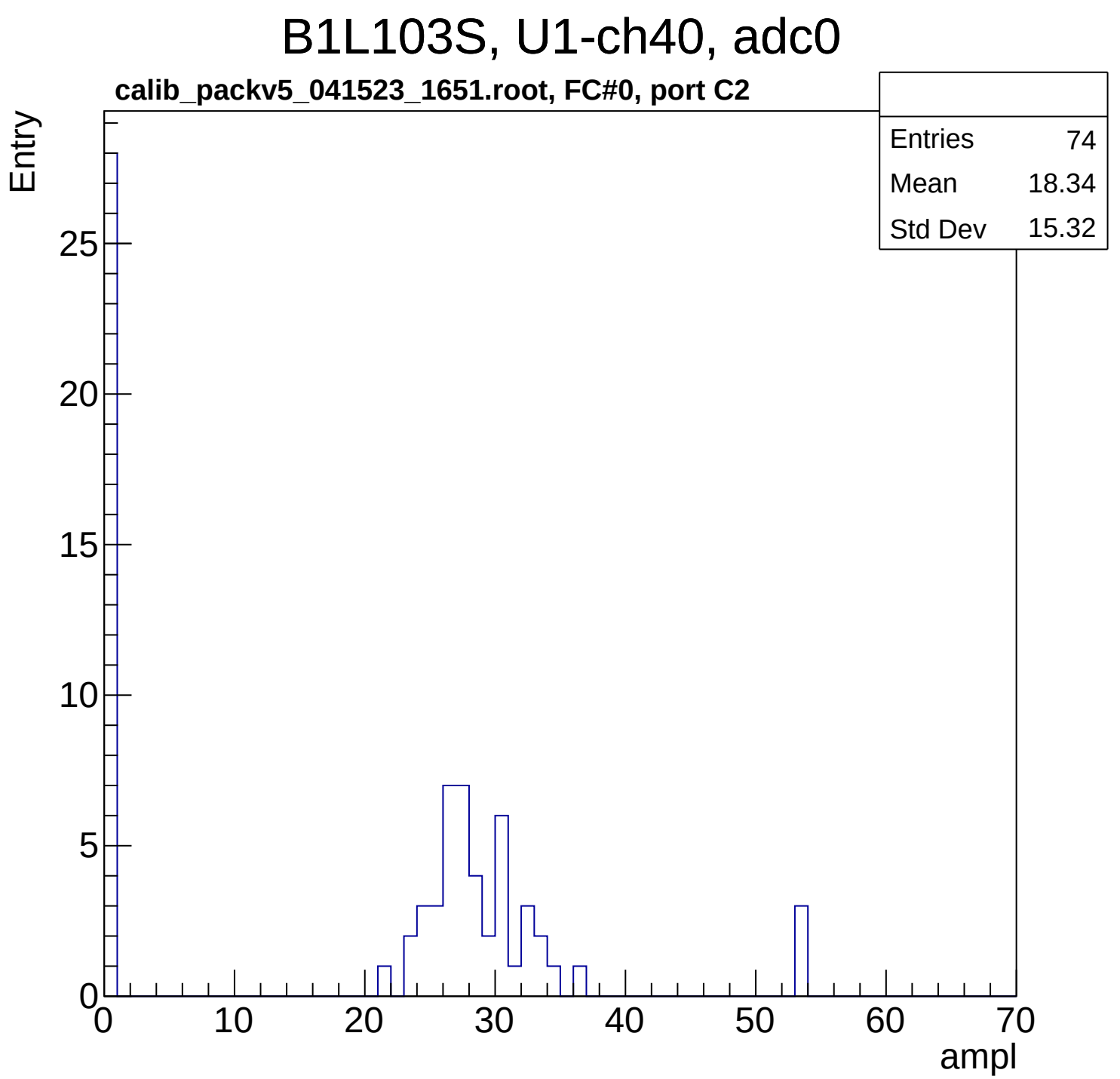
70
ampl


B1L103S, U1-ch40, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 18.34
Std Dev 15.32
Entry
0
5
10
15
20
25
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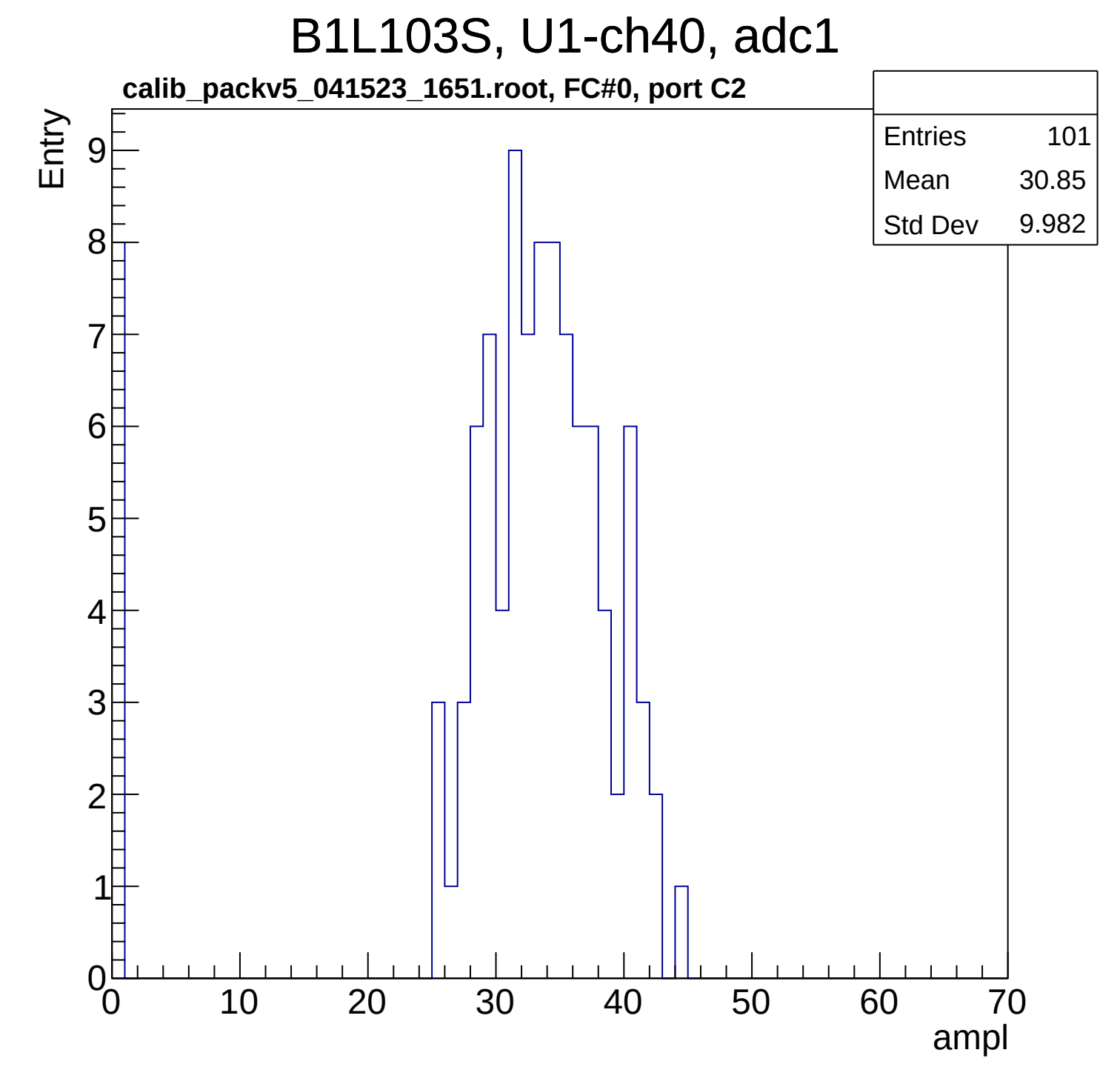
70
ampl


B1L103S, U1-ch40, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 101
Mean 30.85
Std Dev 9.982
Entry
ampl
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3
4
5
6
7
8
9
0
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60
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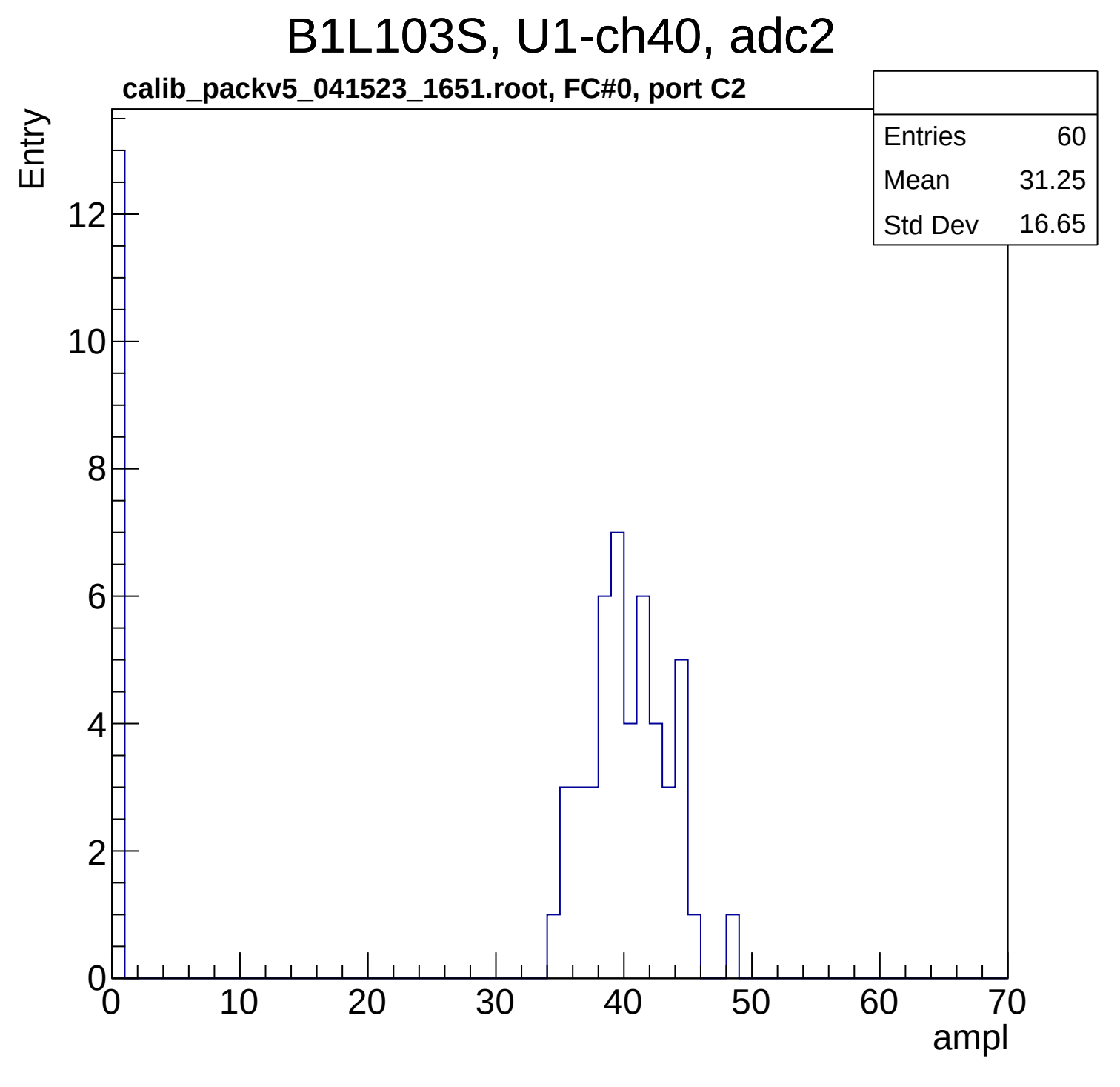
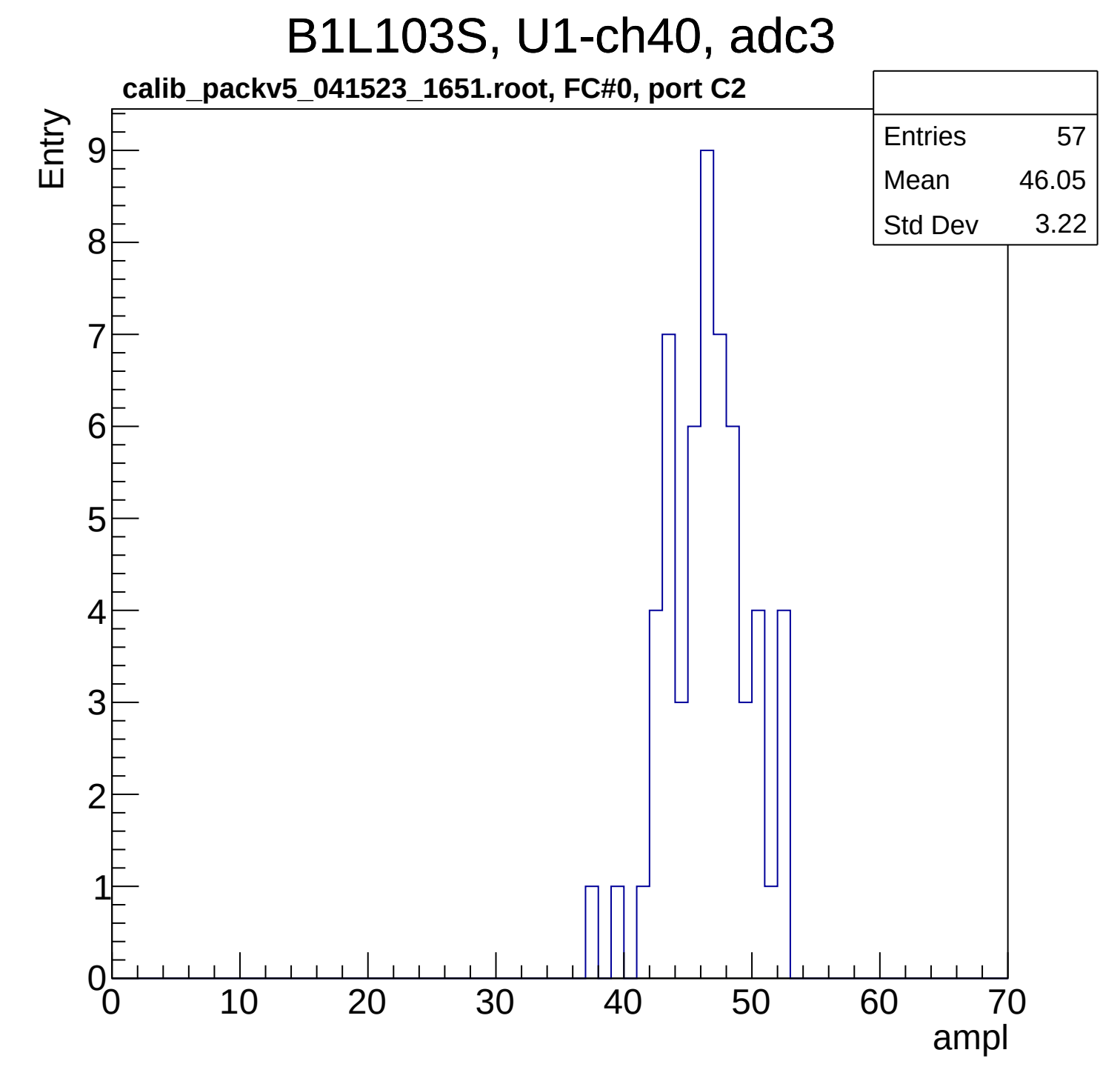

B1L103S, U1-ch40, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 31.25
Std Dev 16.65
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch40, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 46.05
Std Dev 3.22
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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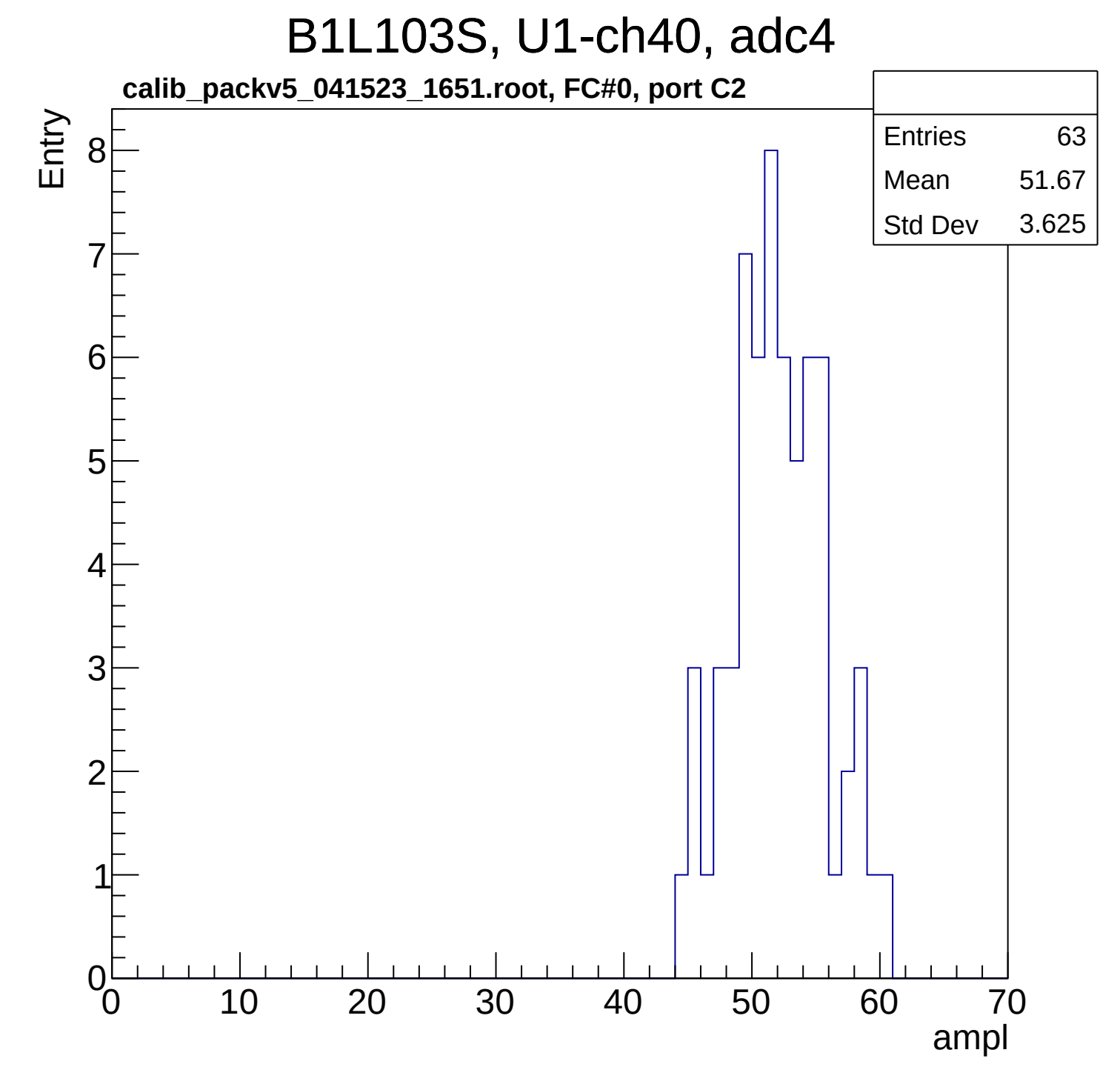
B1L103S, U1-ch40, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 51.67
Std Dev 3.625
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
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40
50
60
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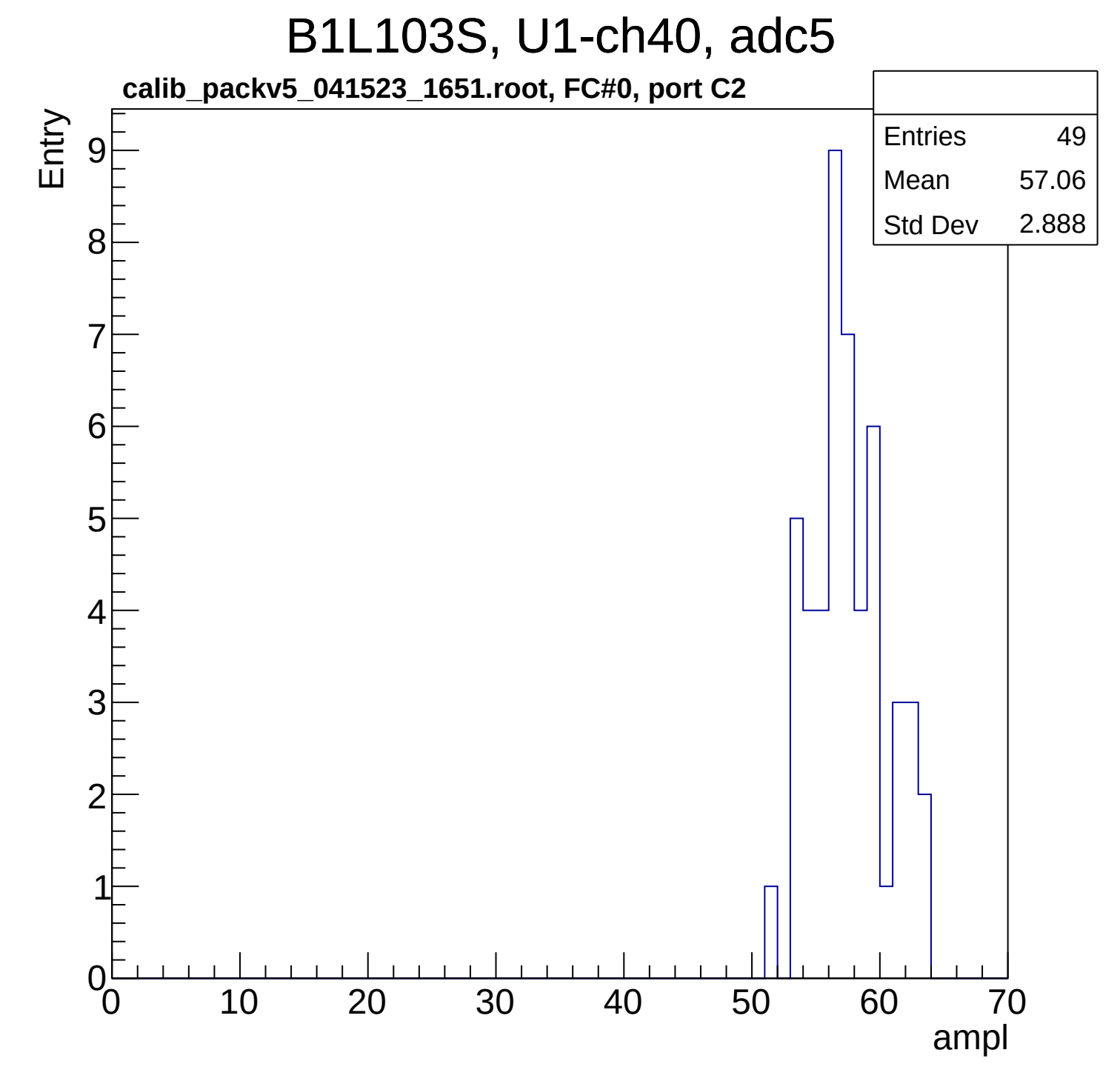
B1L103S, U1-ch40, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 57.06
Std Dev 2.888
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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60
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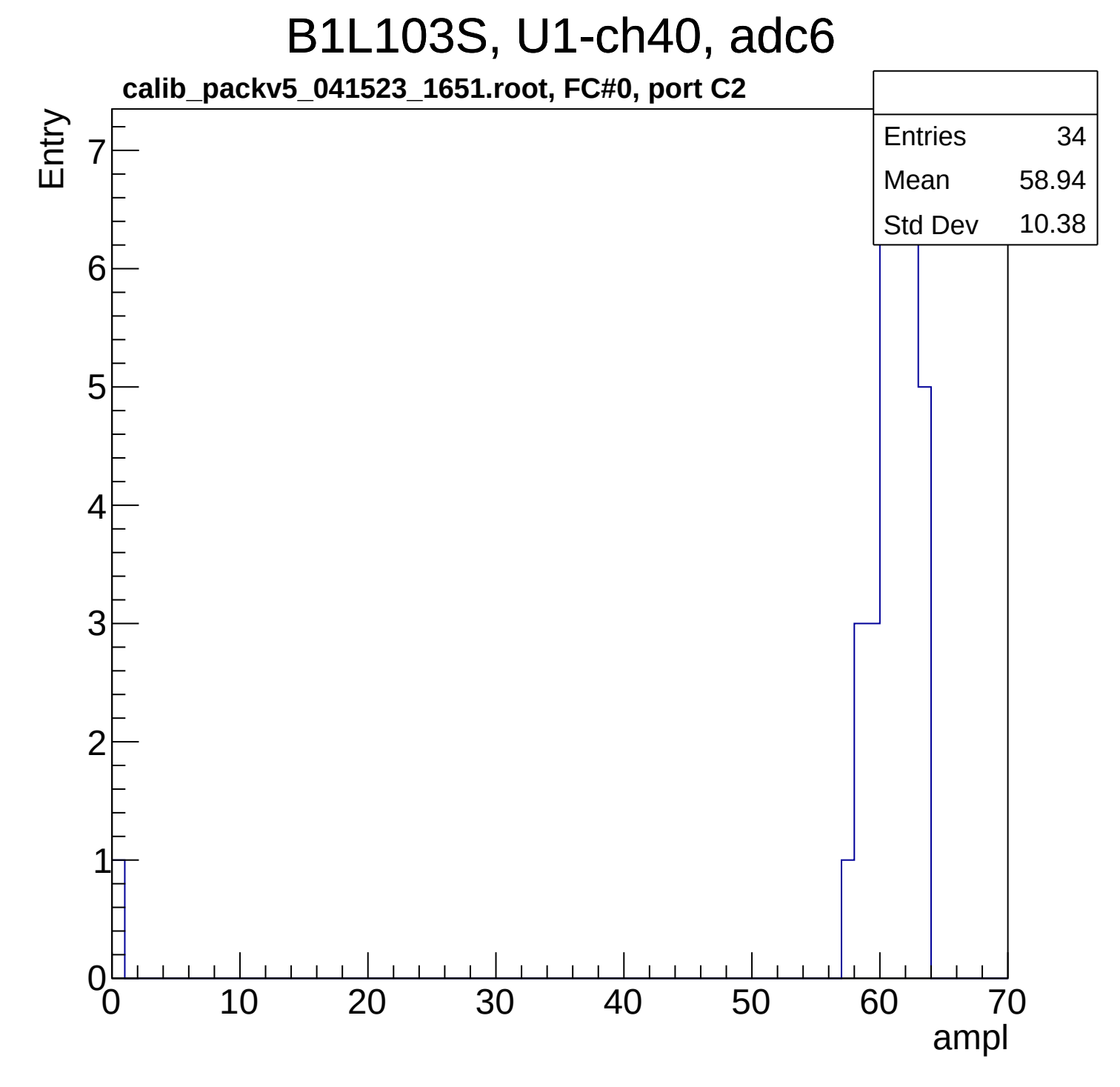
B1L103S, U1-ch40, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 34
Mean 58.94
Std Dev 10.38
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
30
40
50
60
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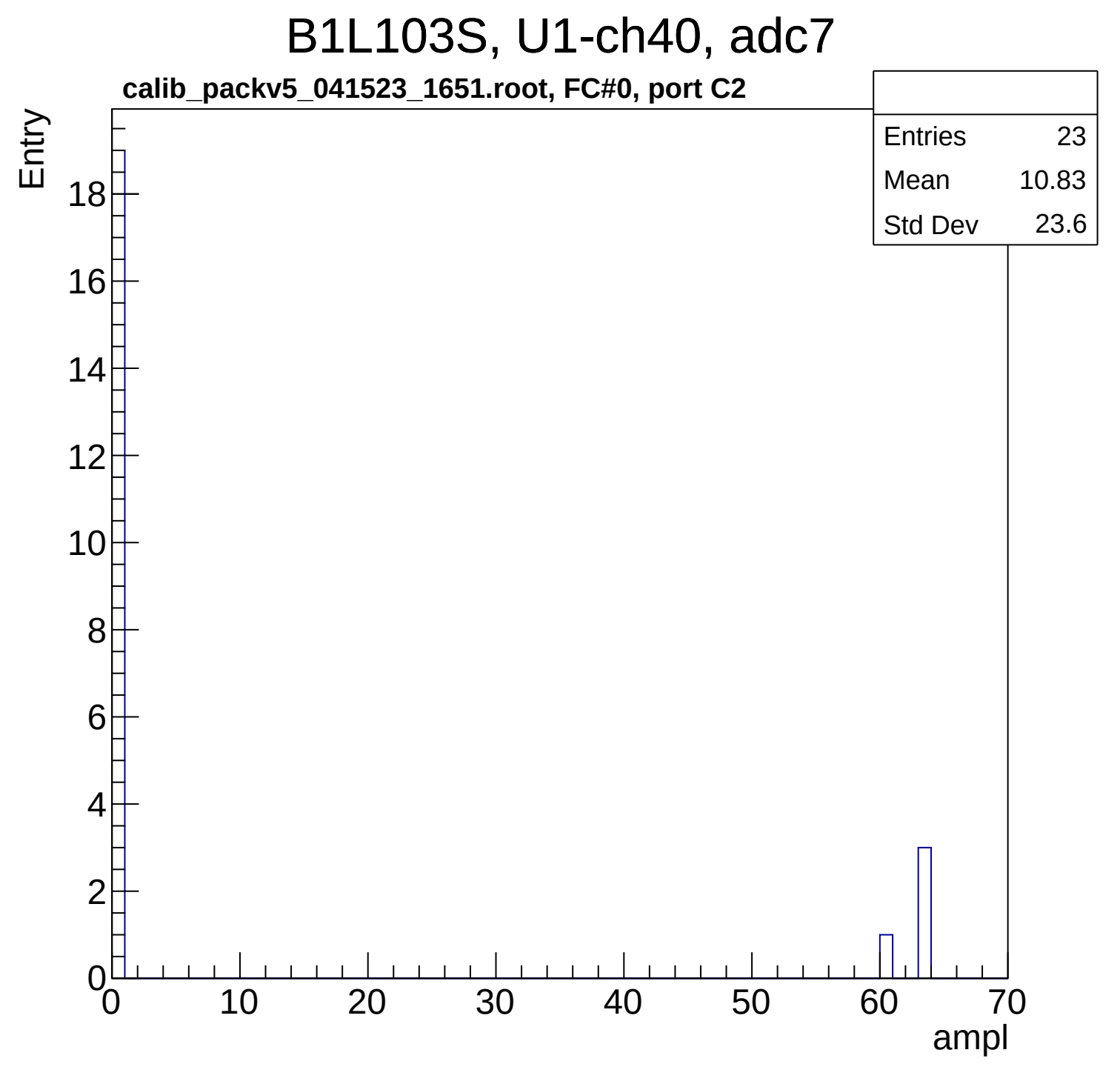
B1L103S, U1-ch40, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 23
Mean 10.83
Std Dev 23.6
Entry
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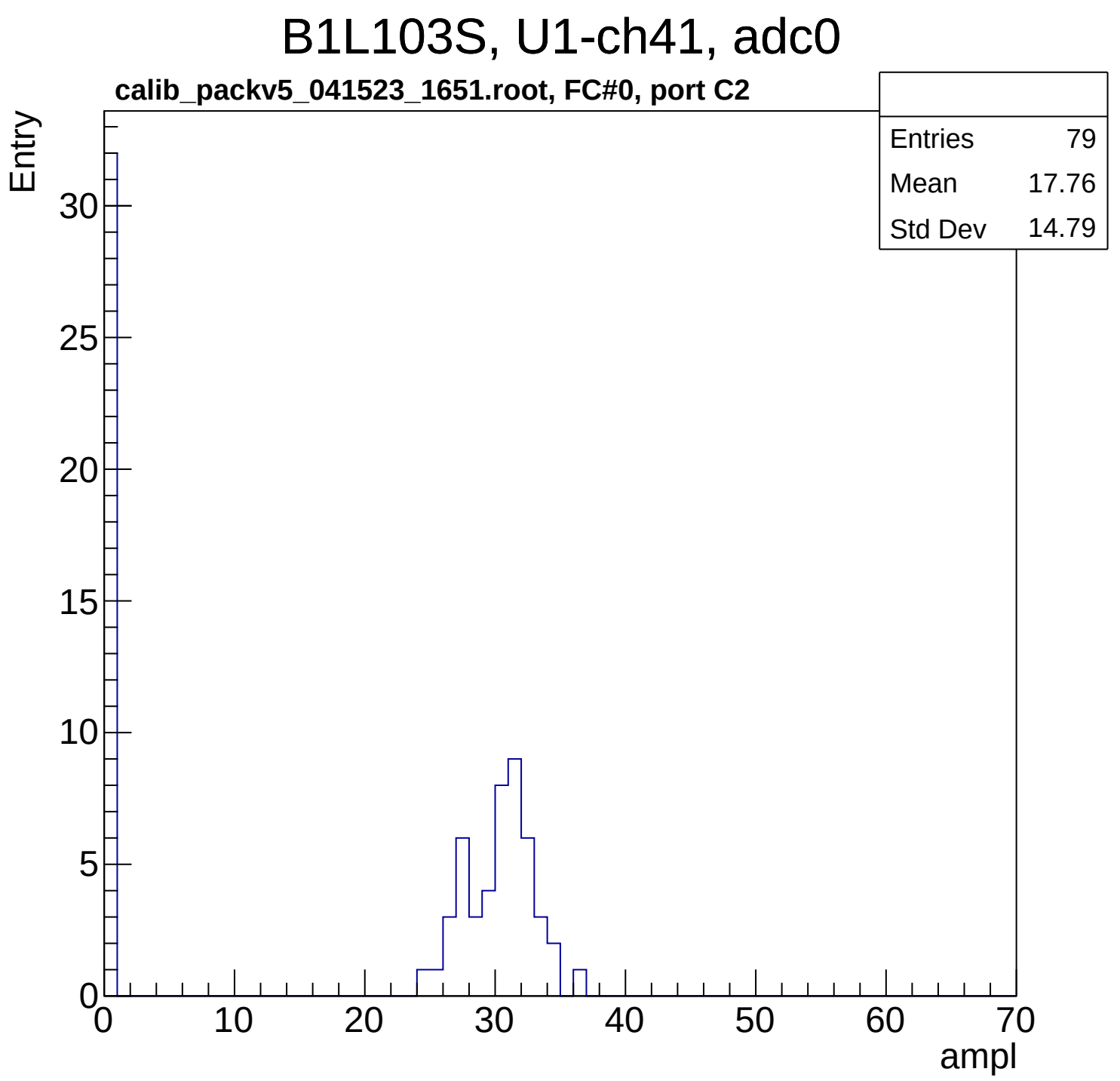
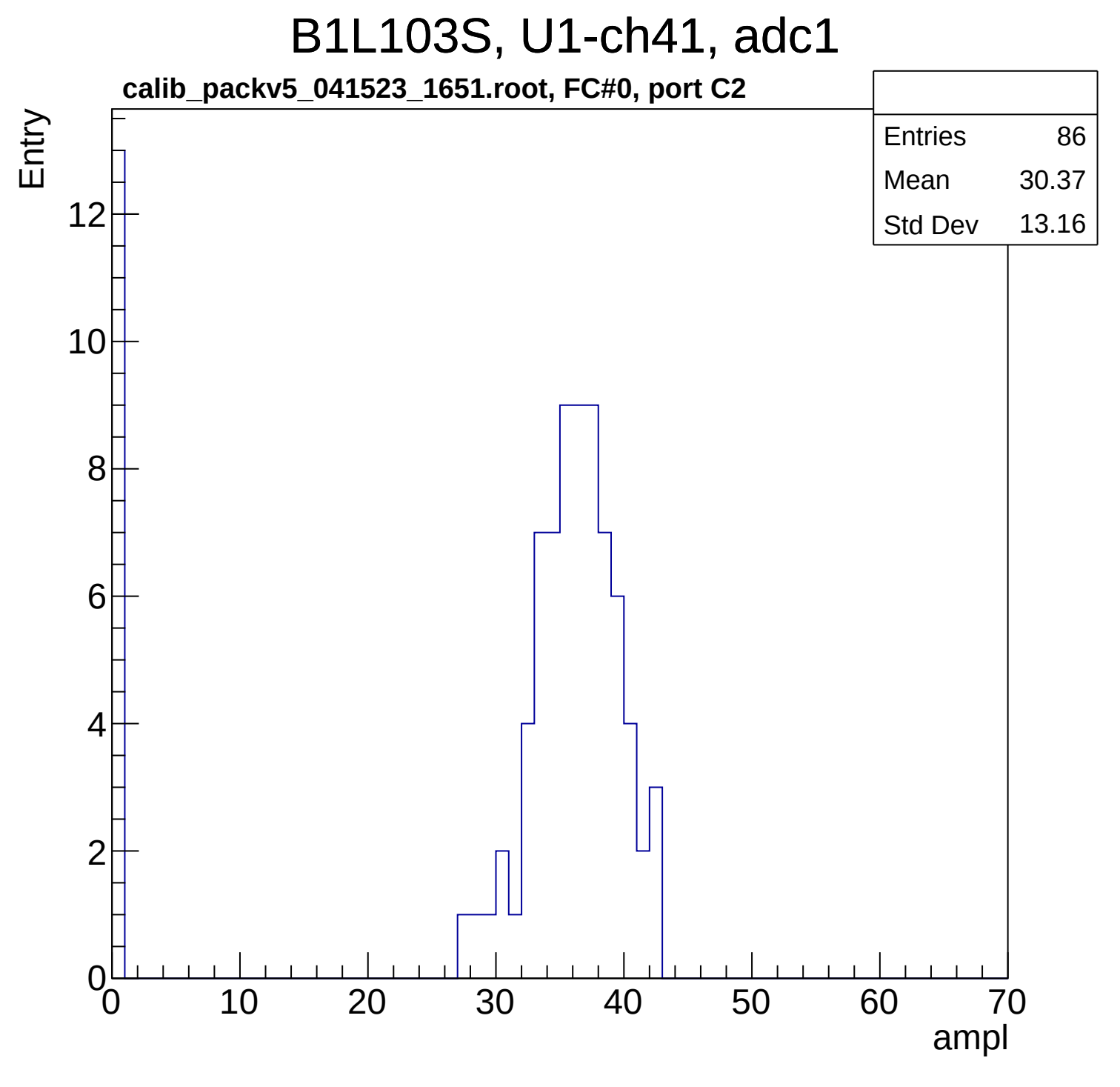
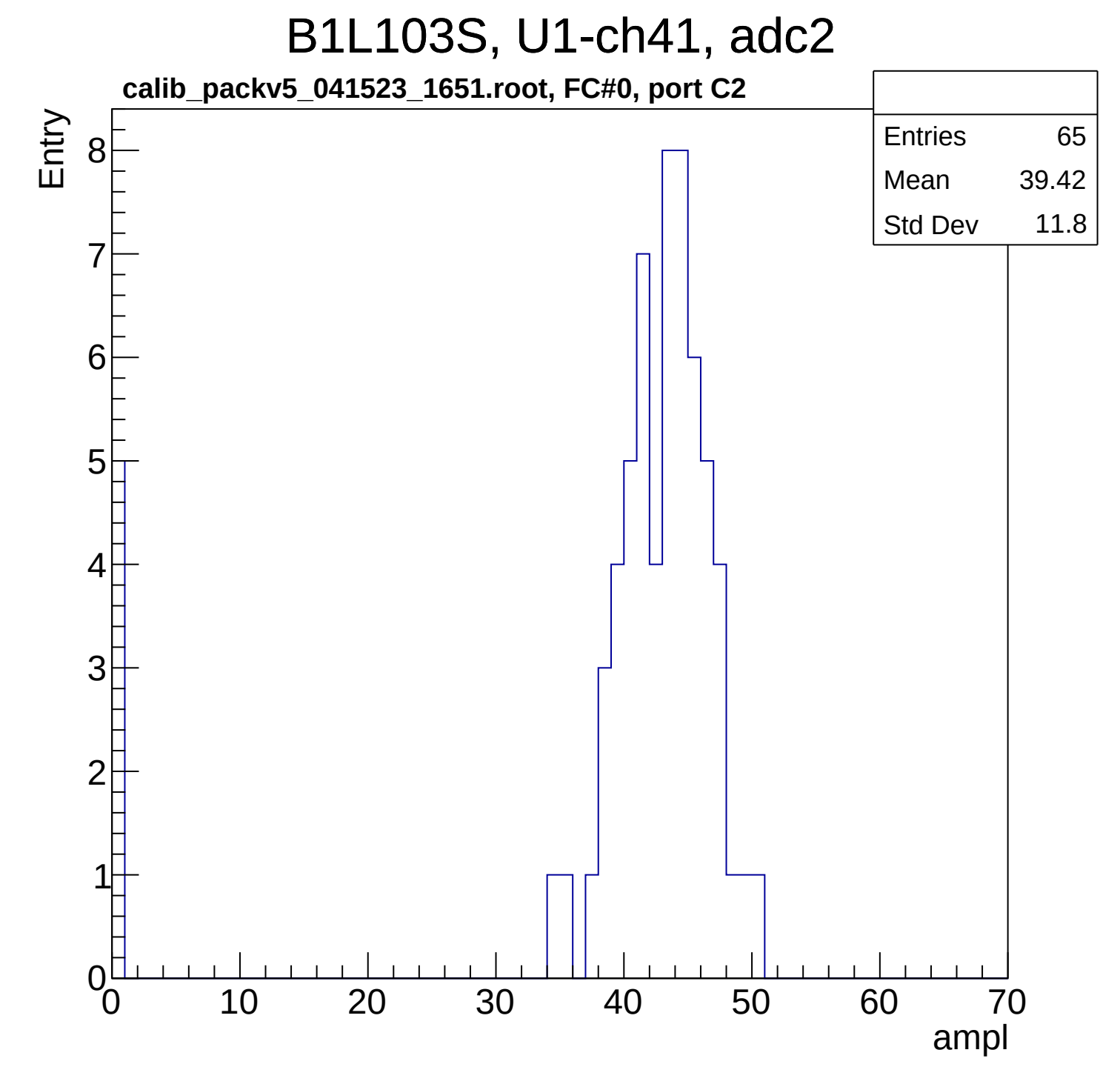
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch41, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 17.76
Std Dev 14.79
Entry
0
5
10
15
20
25
30
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch41, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 30.37
Std Dev 13.16
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70


B1L103S, U1-ch41, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 39.42
Std Dev 11.8
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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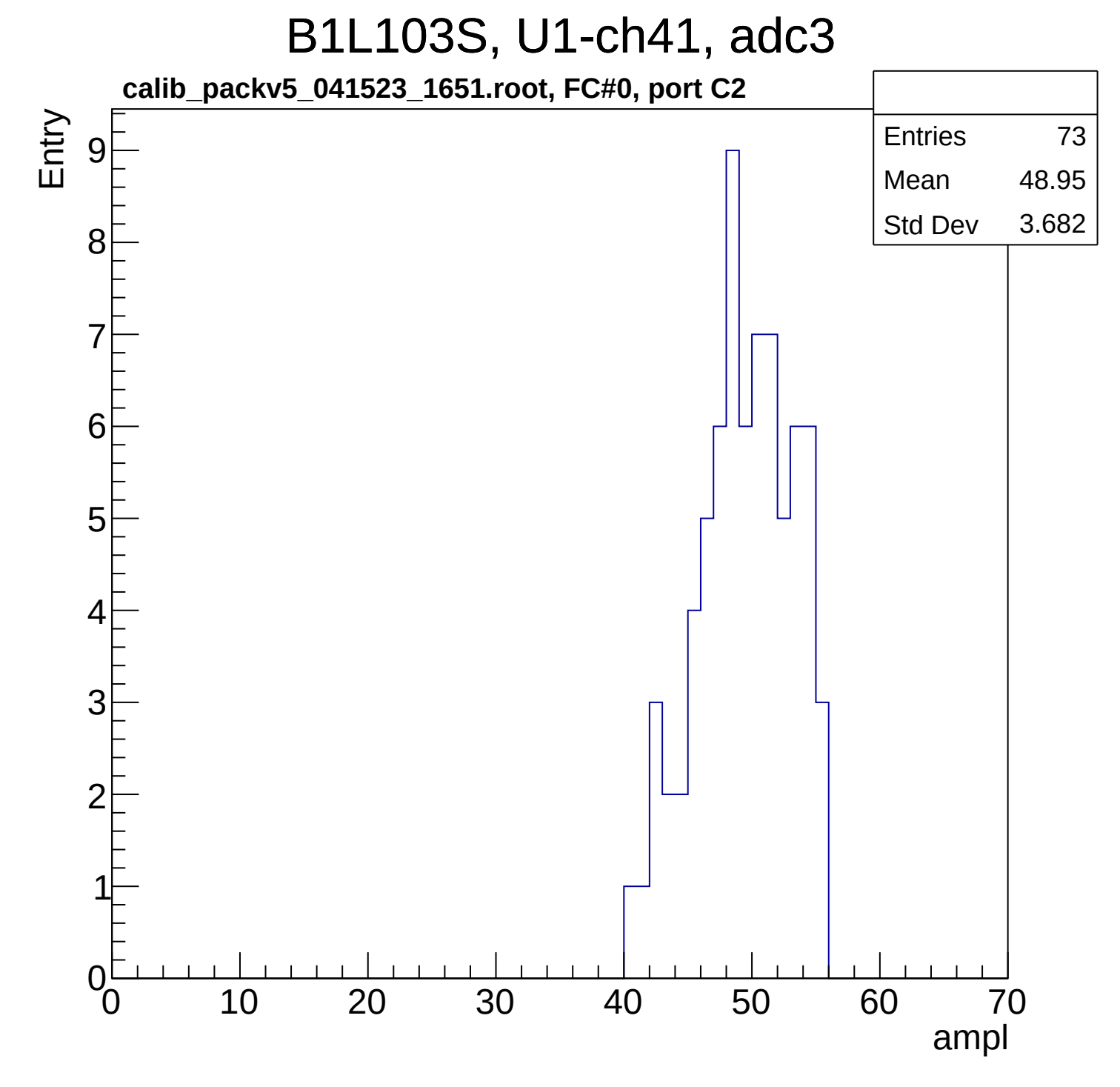
B1L103S, U1-ch41, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 48.95
Std Dev 3.682
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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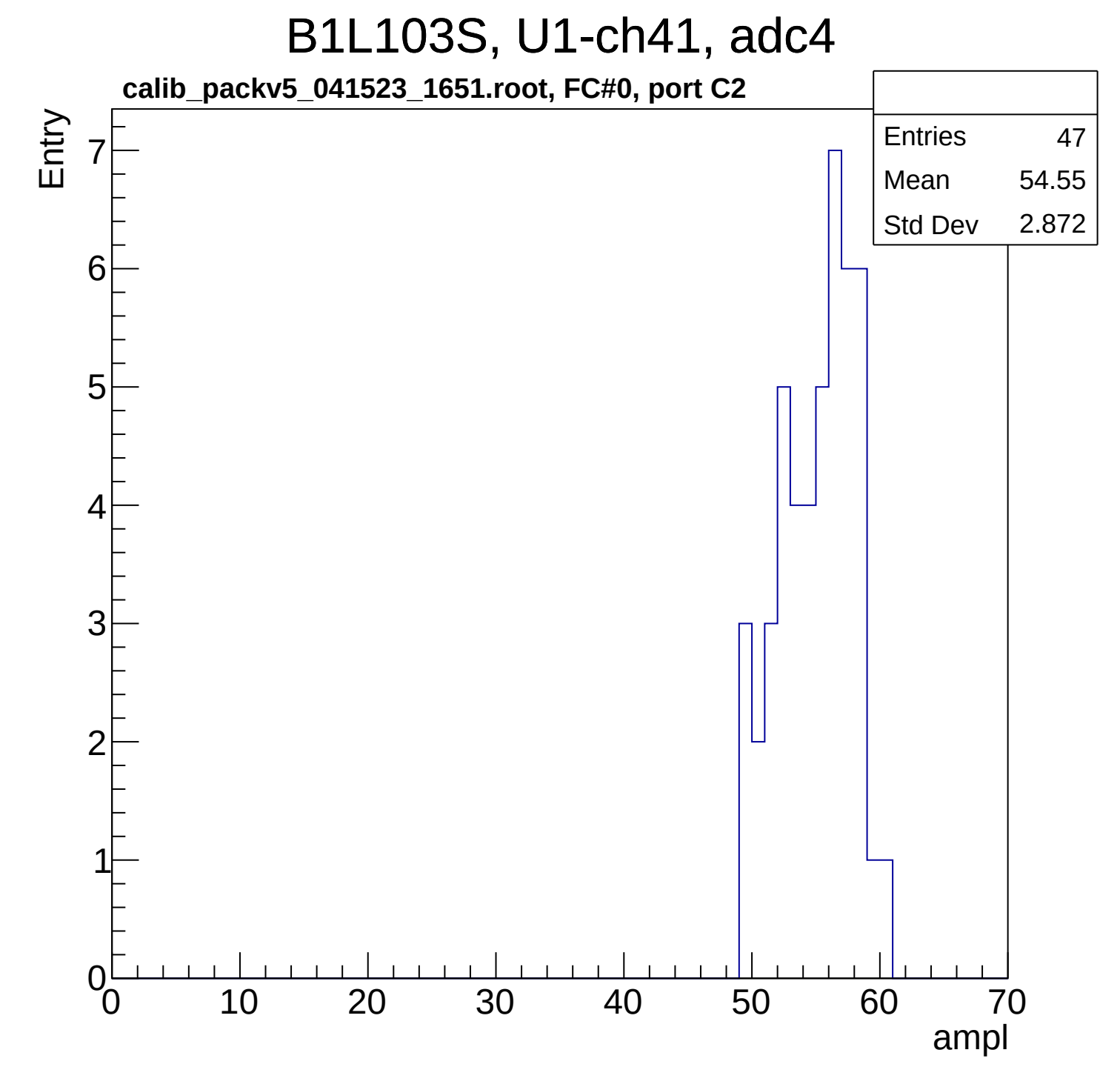
B1L103S, U1-ch41, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 54.55
Std Dev 2.872
Entry
ampl
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1
2
3
4
5
6
7
0
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20
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40
50
60
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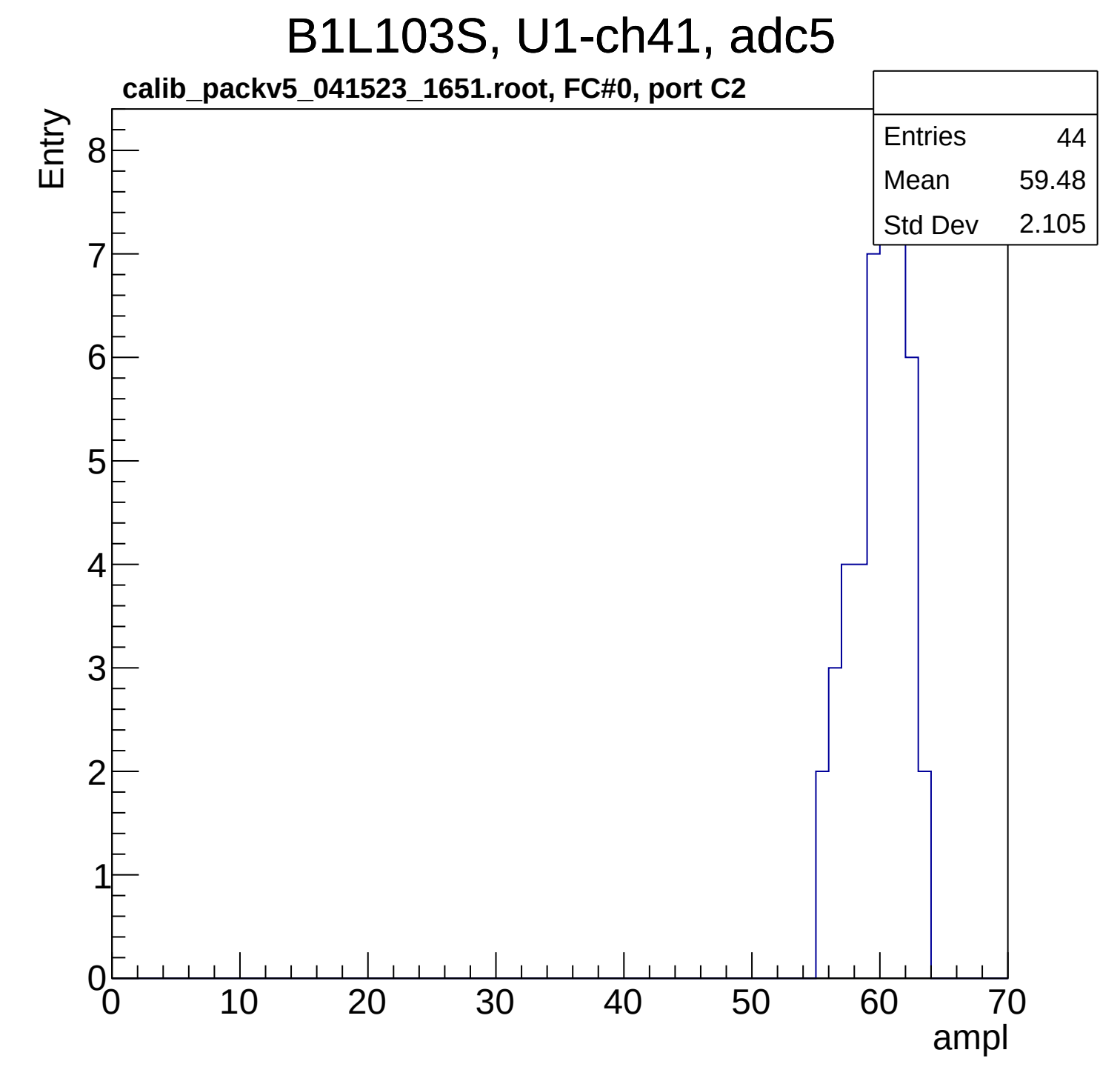
B1L103S, U1-ch41, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 59.48
Std Dev 2.105
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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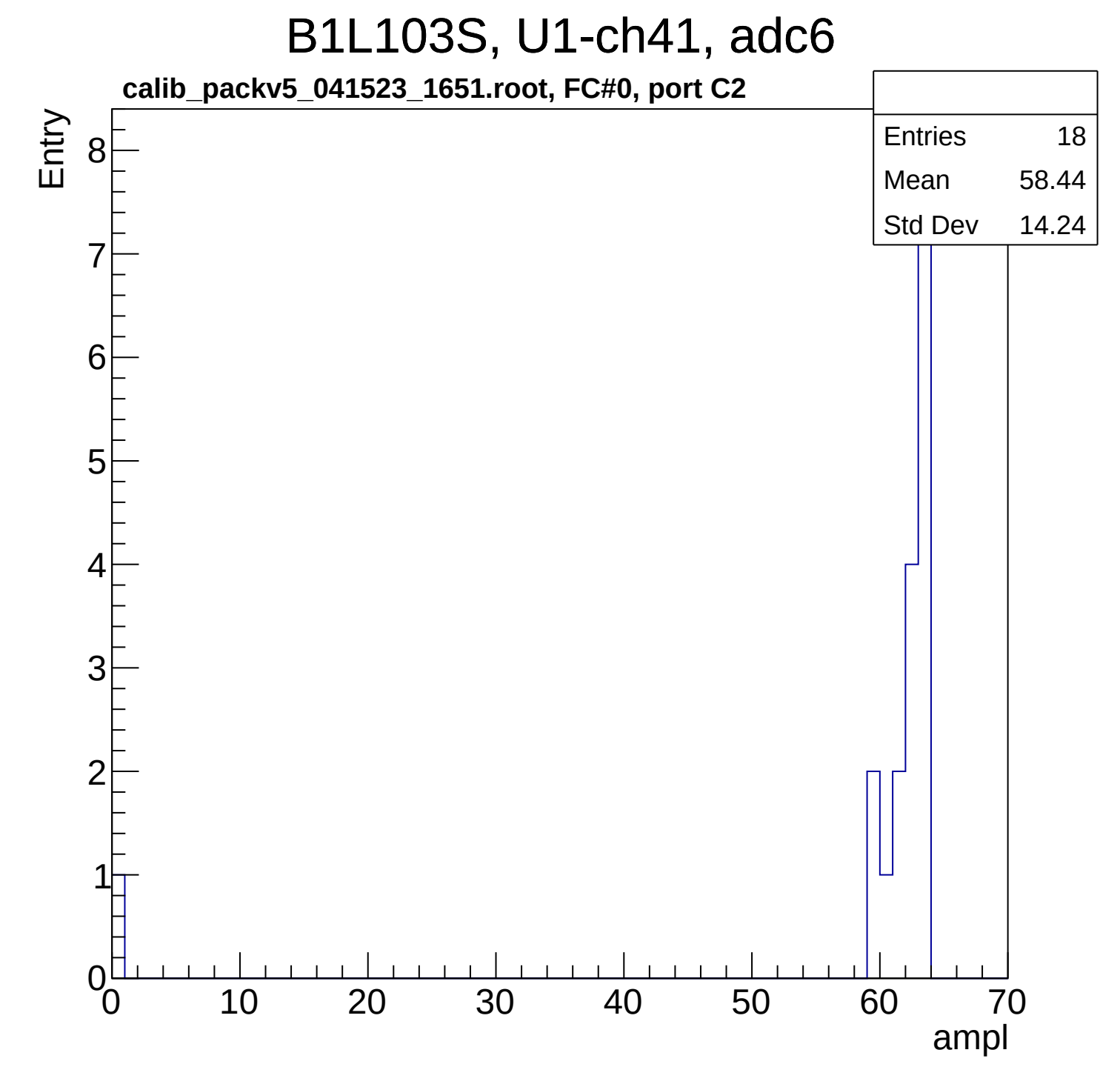
B1L103S, U1-ch41, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 58.44
Std Dev 14.24
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
30
40
50
60
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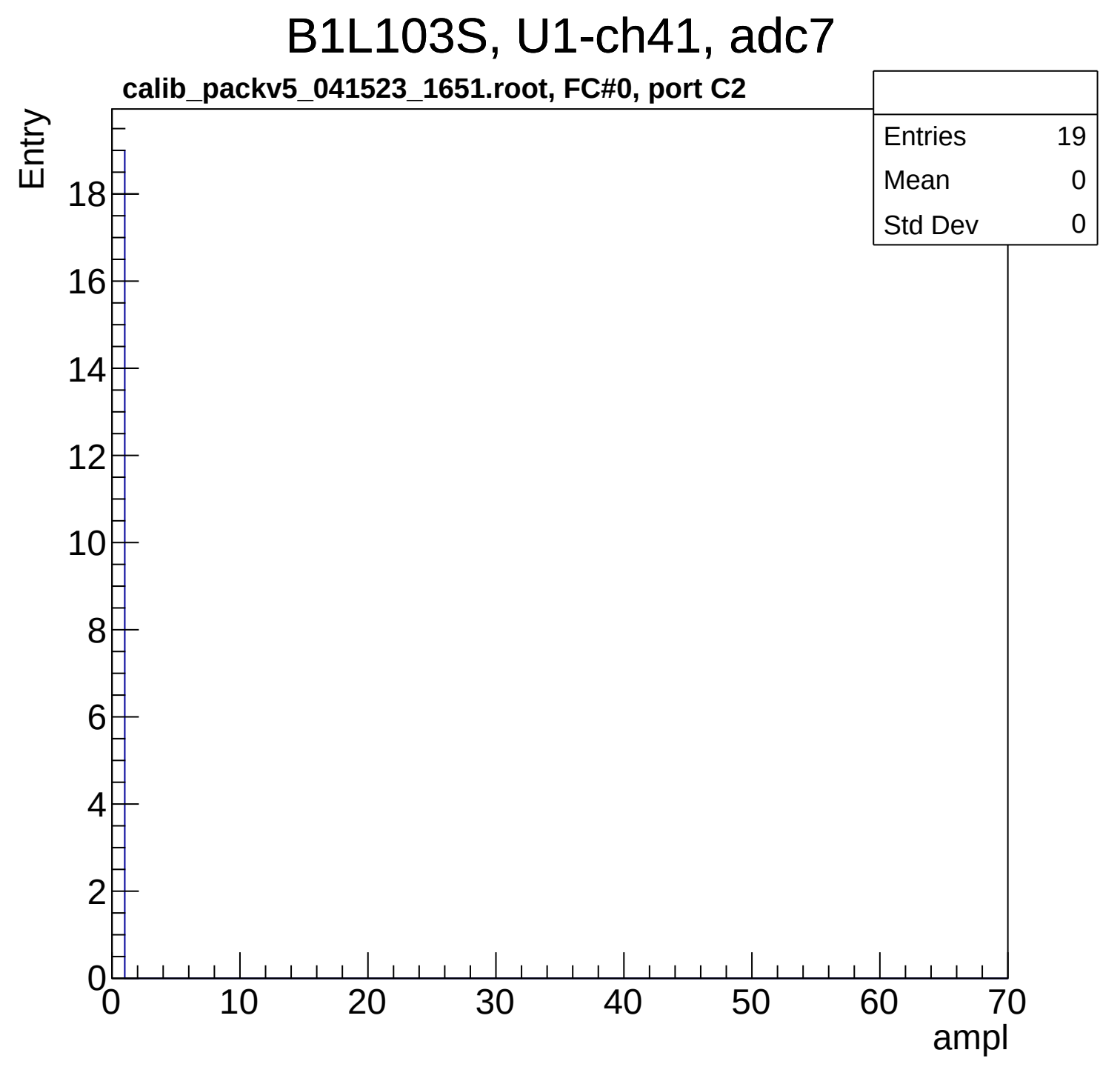
B1L103S, U1-ch41, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
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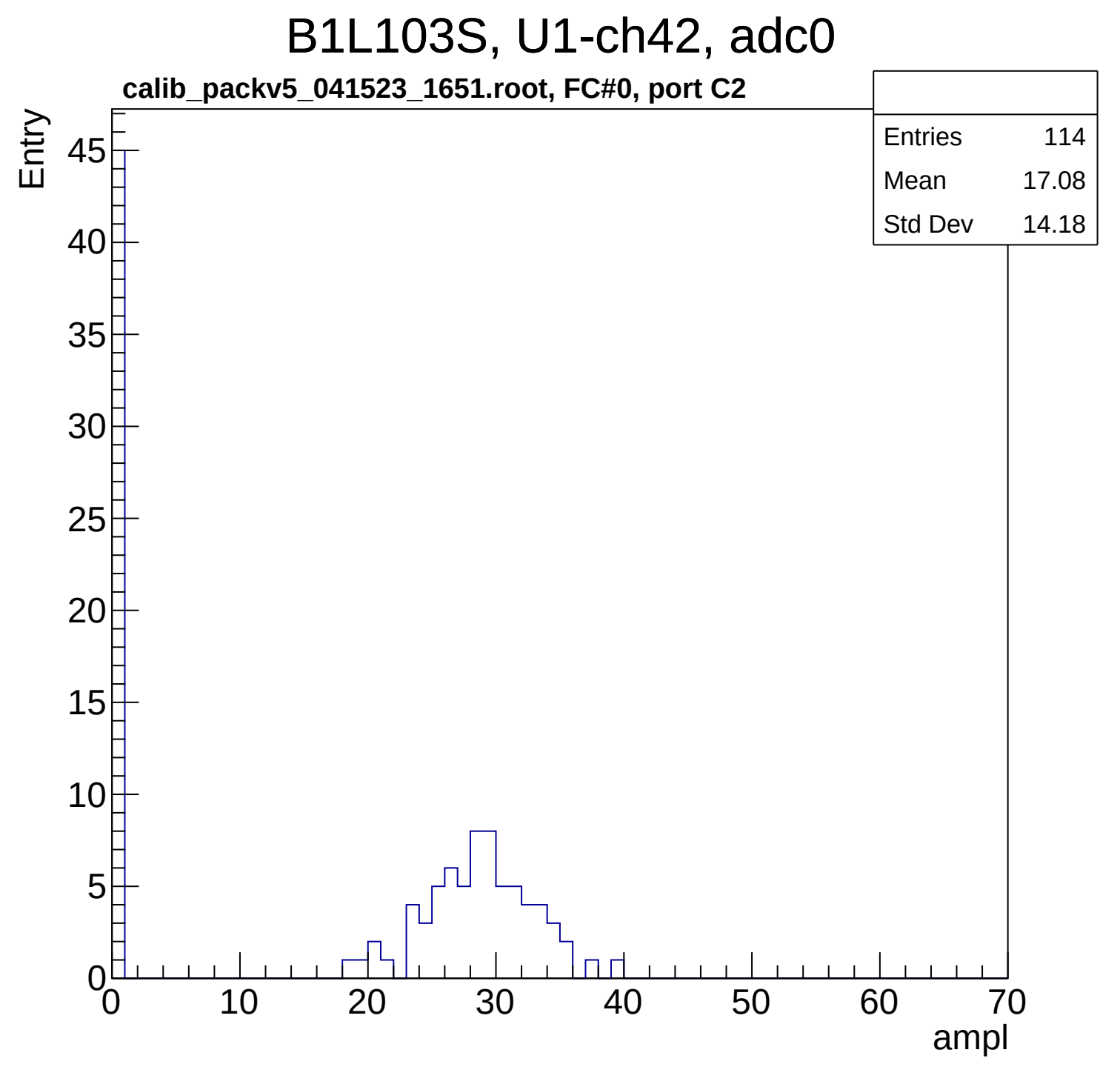
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch42, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 114
Mean 17.08
Std Dev 14.18
Entry
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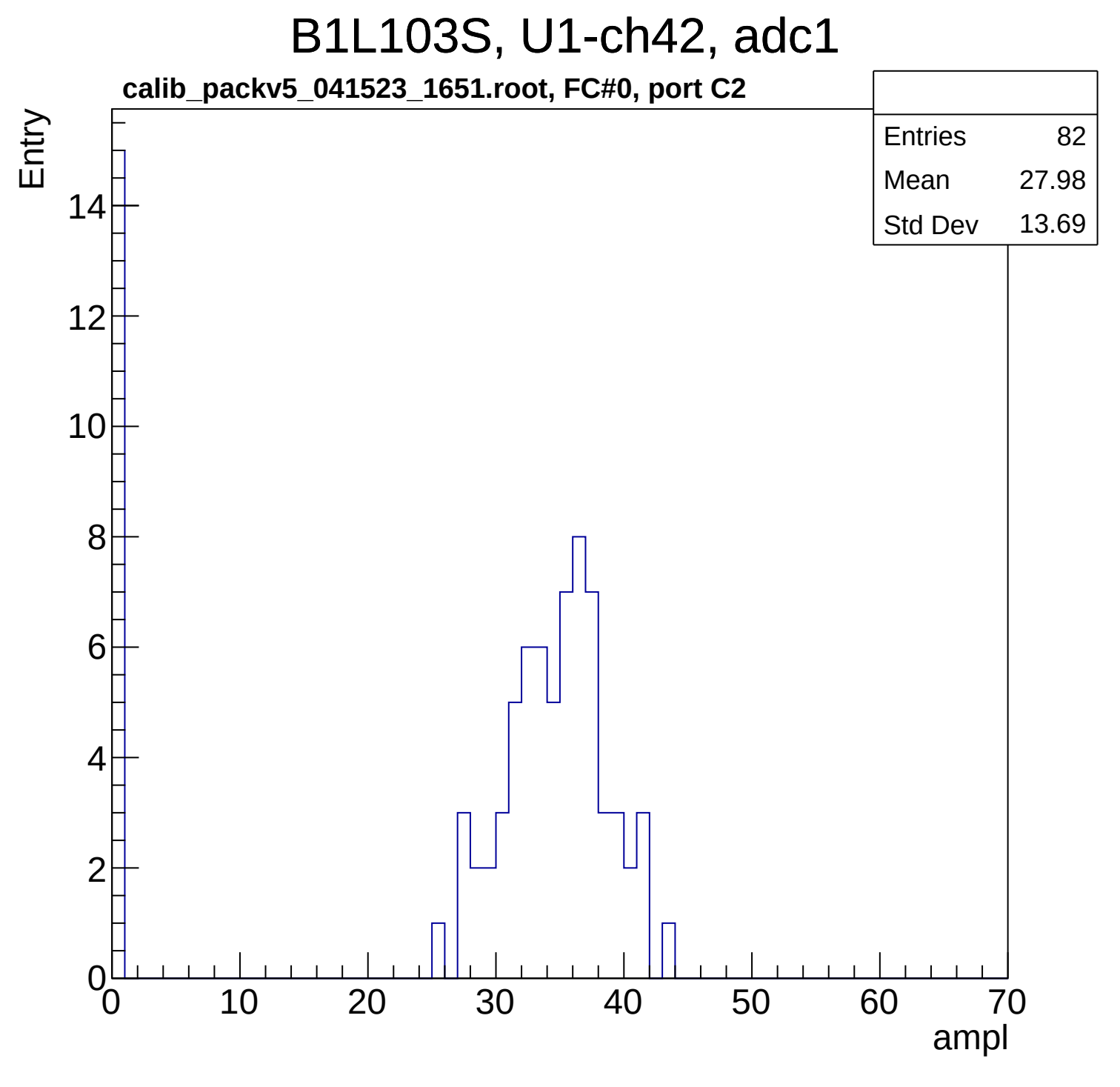
5
10
15
20
25
30
35
40
45
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch42, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 27.98
Std Dev 13.69
Entry
ampl
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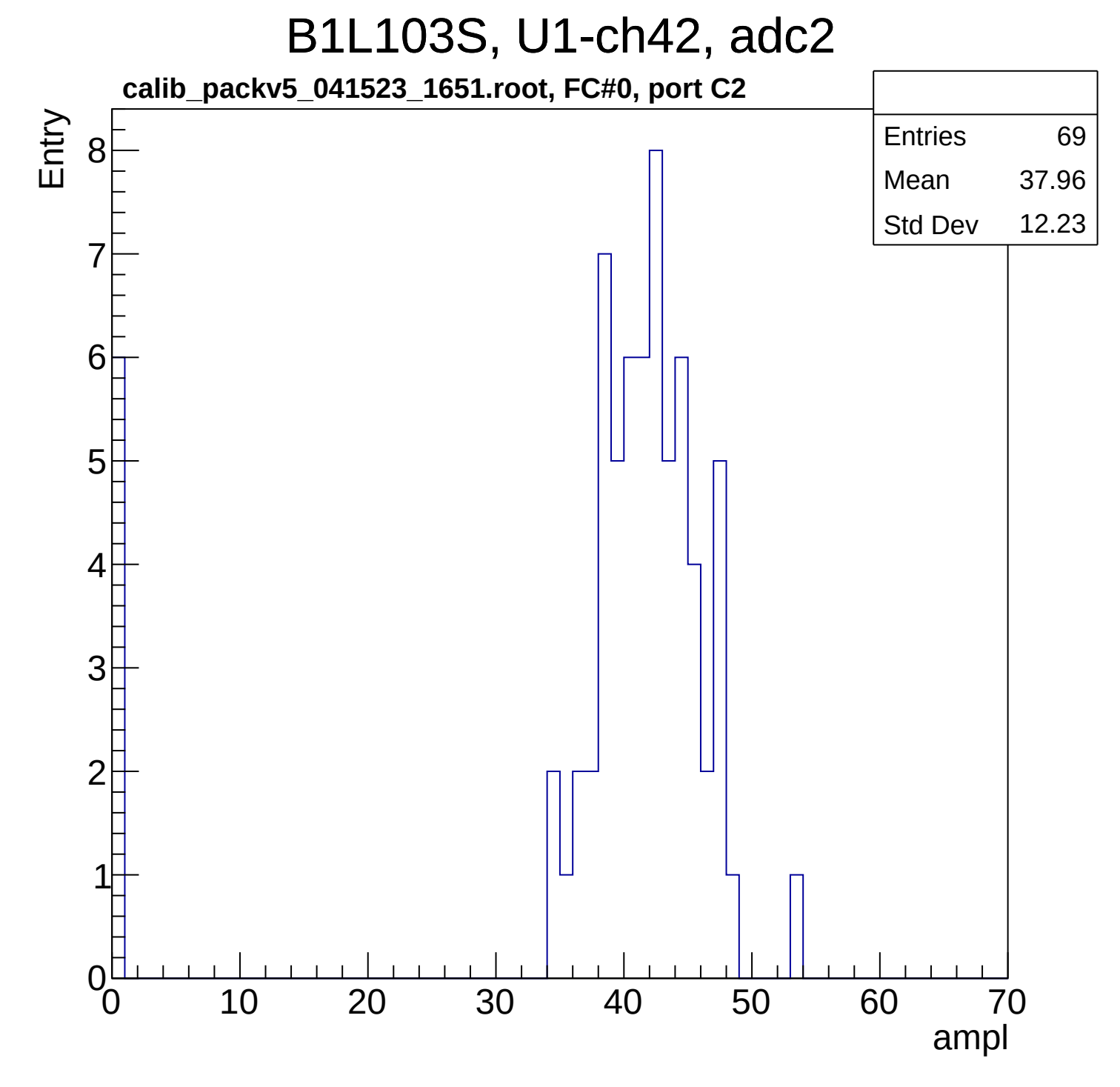
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L103S, U1-ch42, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 37.96
Std Dev 12.23
Entry
ampl
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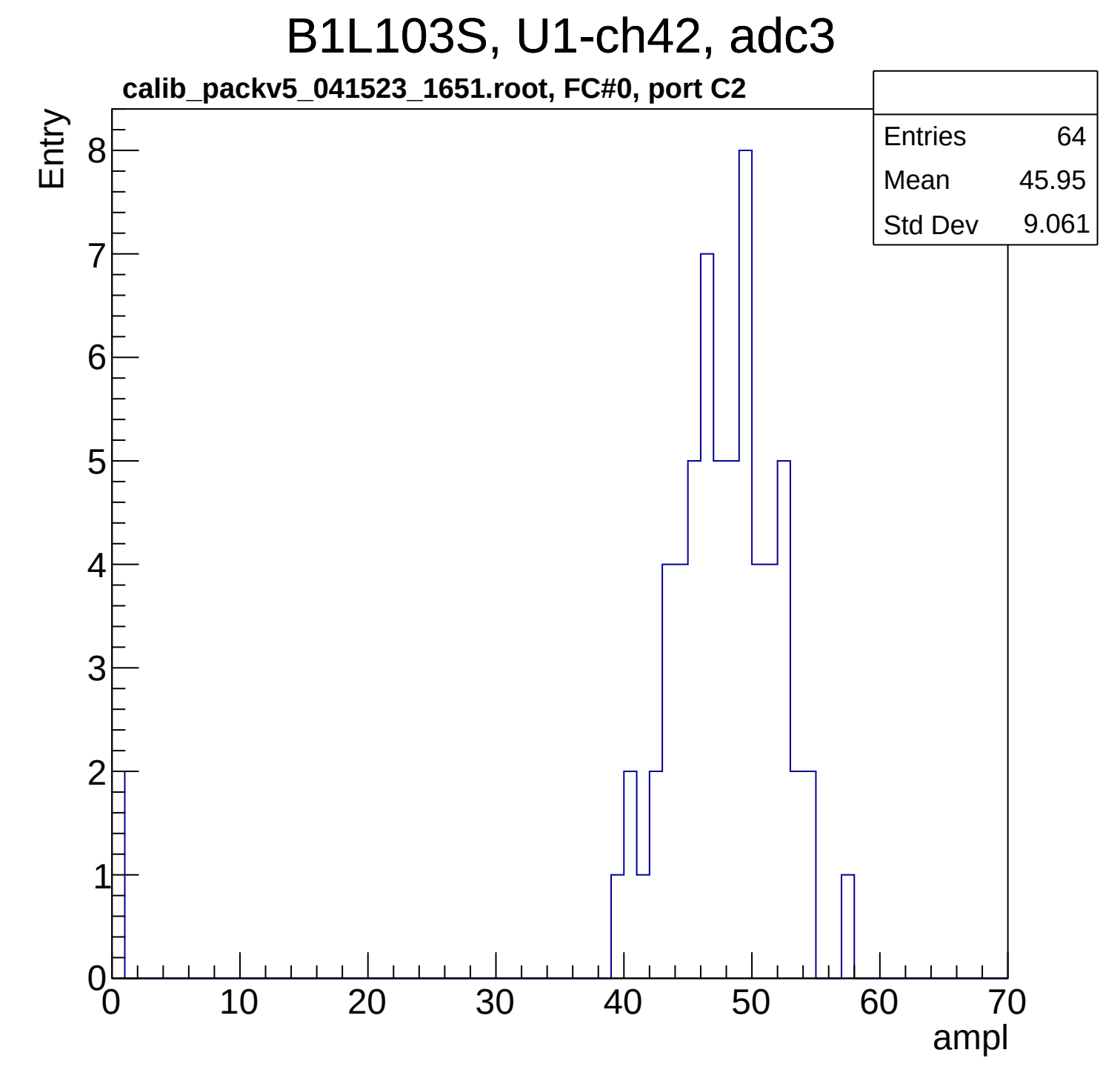
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U1-ch42, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 45.95
Std Dev 9.061
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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60
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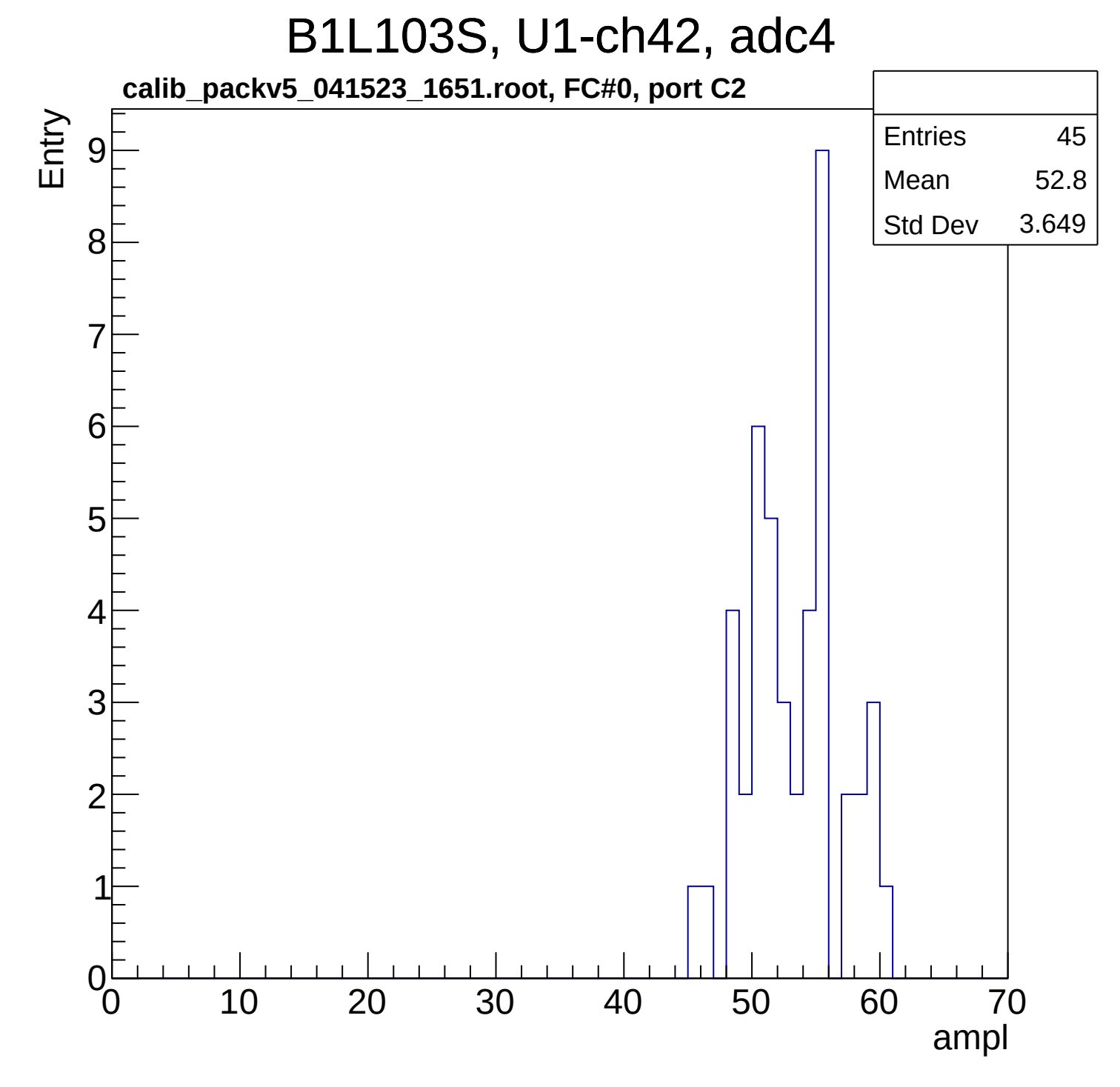
B1L103S, U1-ch42, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 52.8
Std Dev 3.649
Entry
ampl
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3
4
5
6
7
8
9
0
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20
30
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50
60
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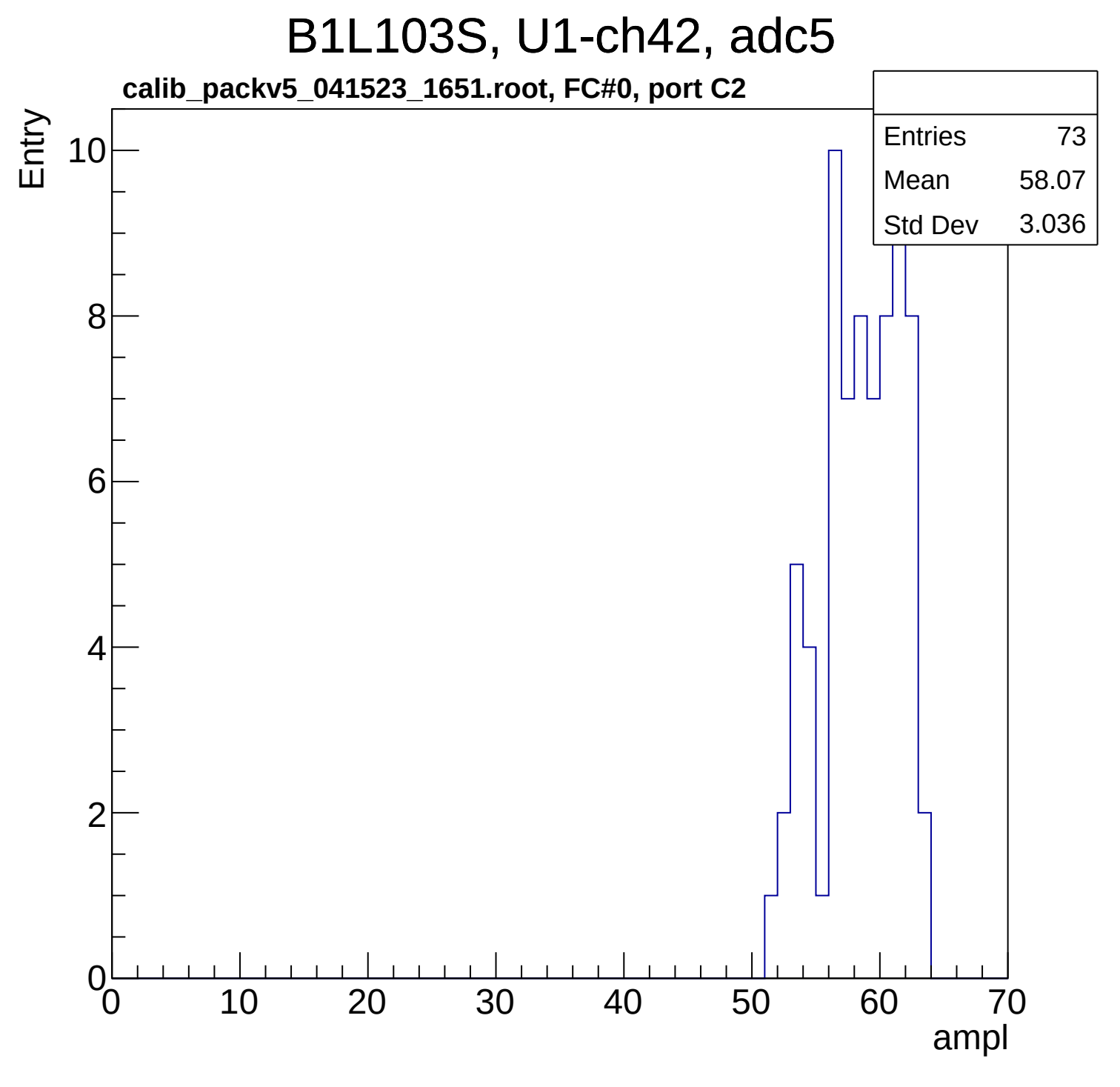
B1L103S, U1-ch42, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 58.07
Std Dev 3.036
Entry
ampl
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2
4
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0
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20
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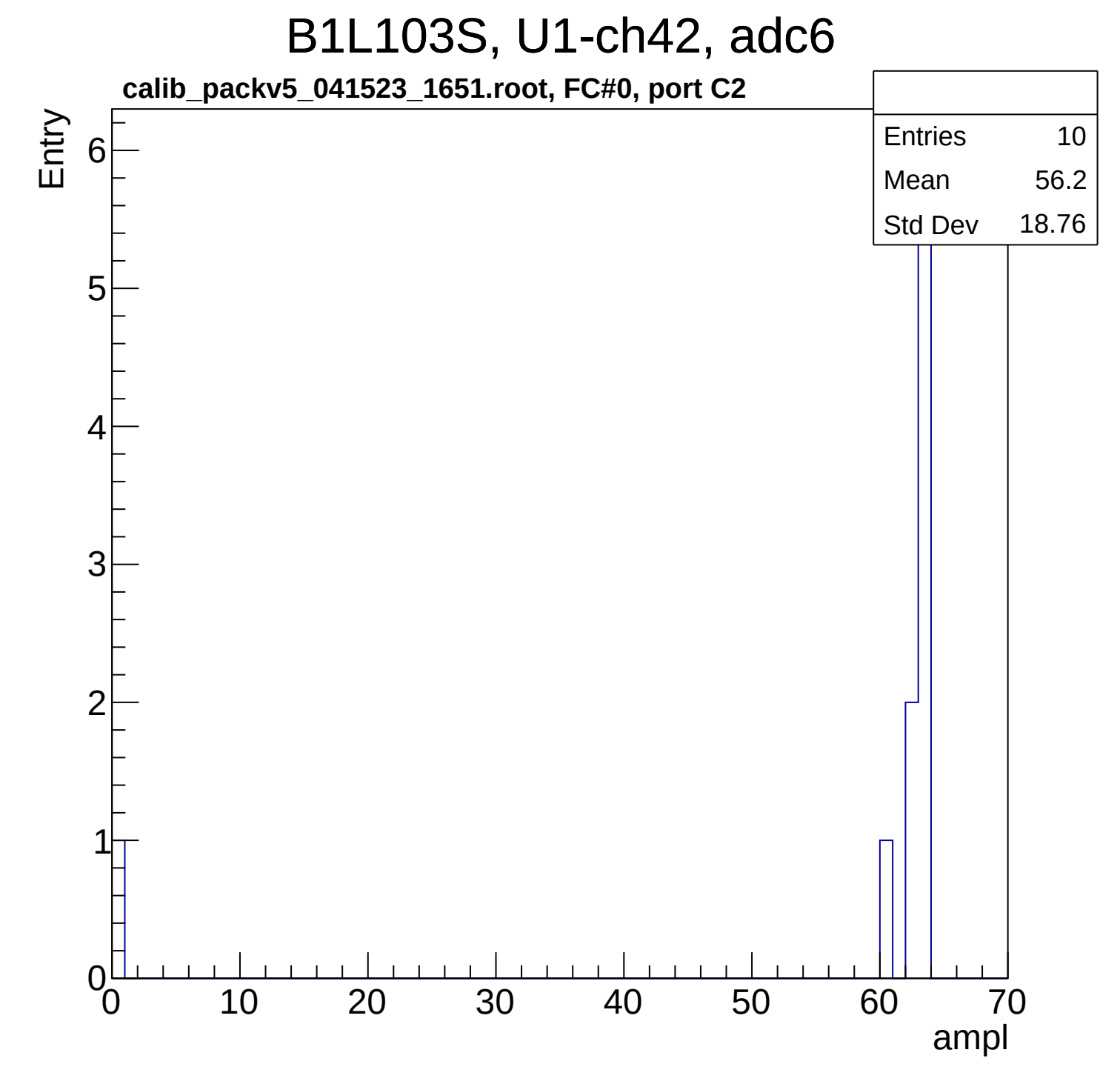
40
50
60
70


B1L103S, U1-ch42, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 56.2
Std Dev 18.76
Entry
ampl
0
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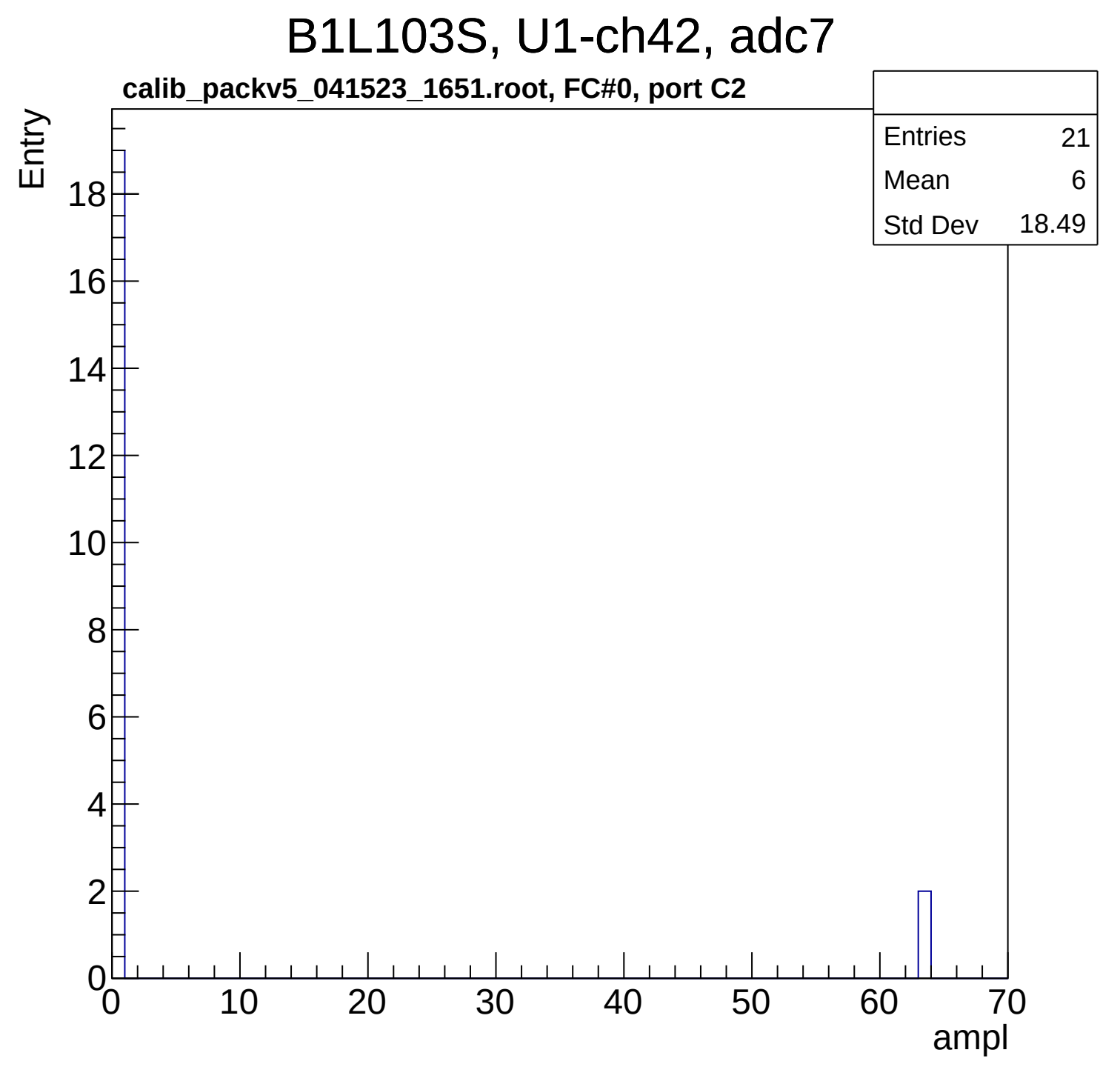
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U1-ch42, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 6
Std Dev 18.49
Entry
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6
8
10
12
14
16
18
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10
20
30
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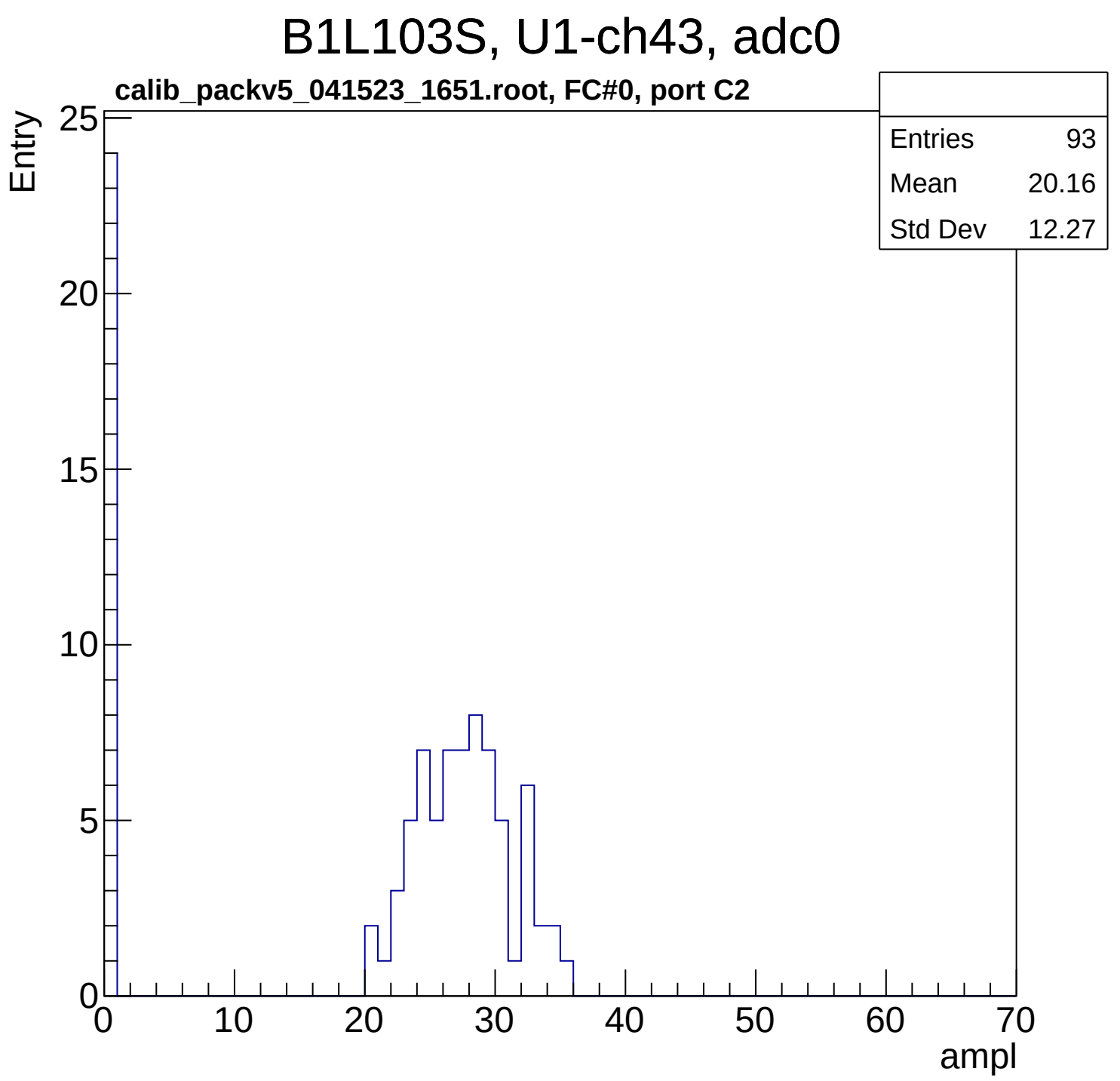
50
60
70
ampl


B1L103S, U1-ch43, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 93
Mean 20.16
Std Dev 12.27
Entry
ampl
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5
10
15
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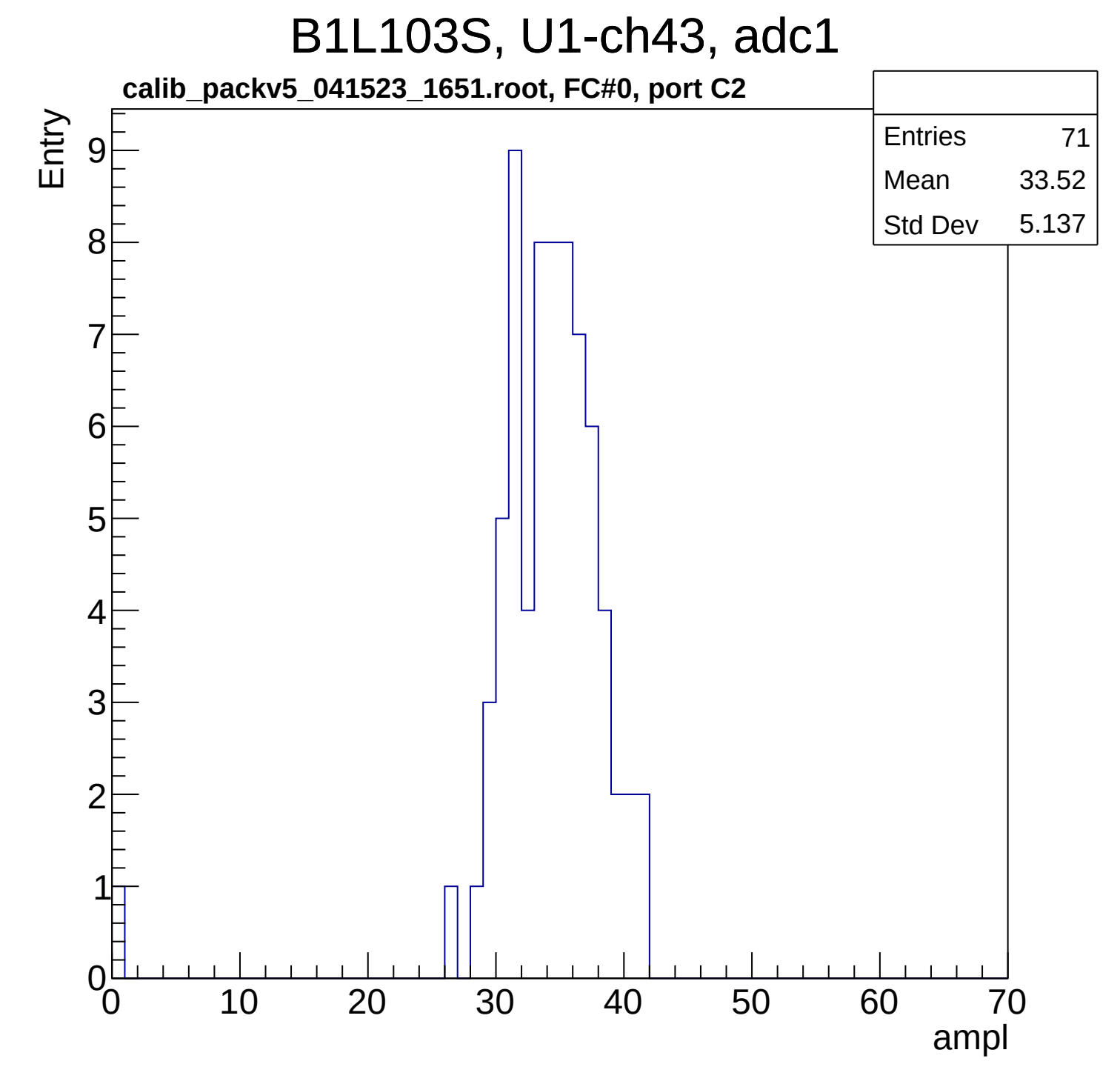
25
0
10
20
30
40
50
60
70


B1L103S, U1-ch43, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 33.52
Std Dev 5.137
Entry
ampl
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2
3
4
5
6
7
8
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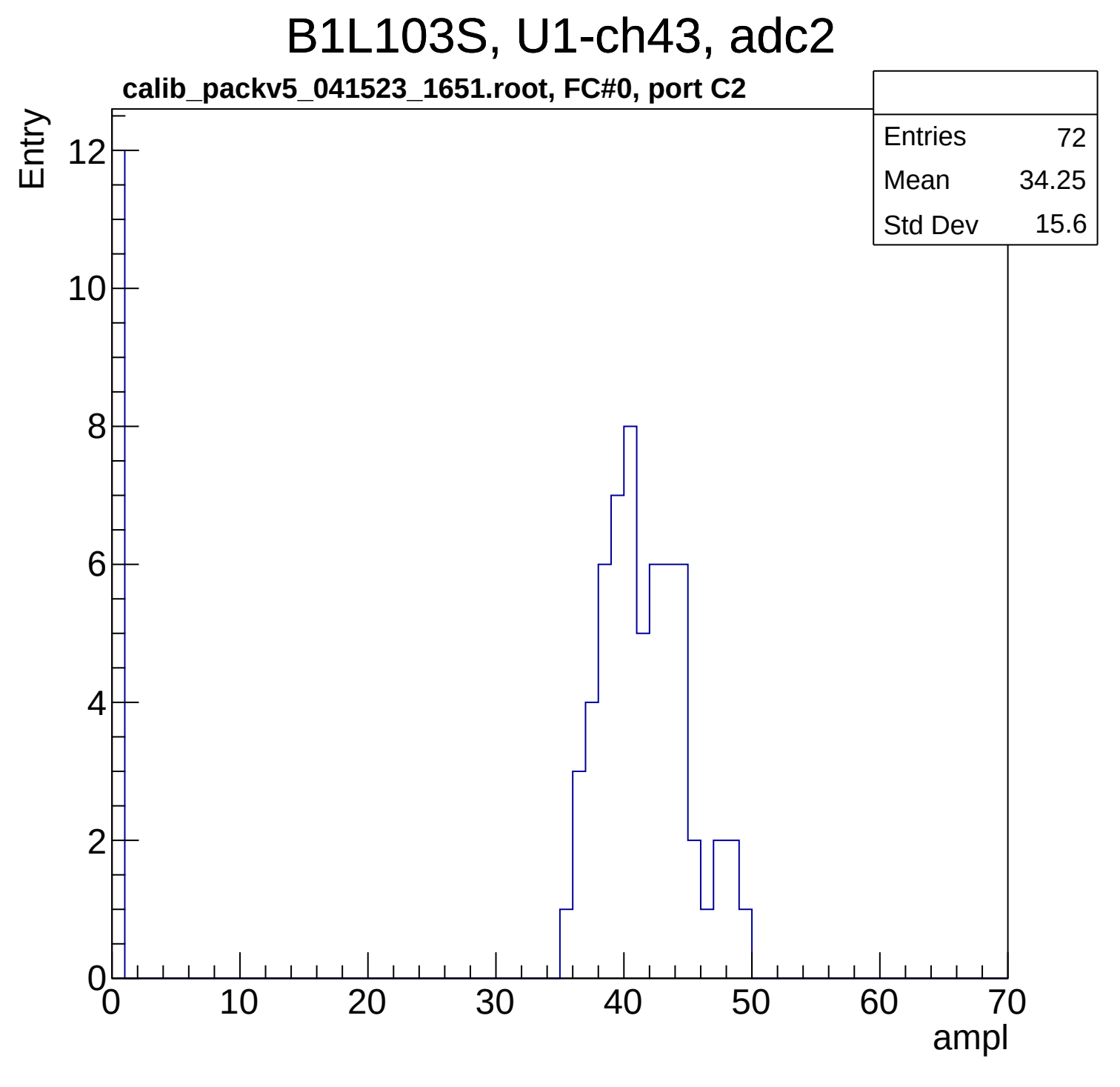
0
10
20
30
40
50
60
70


B1L103S, U1-ch43, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 34.25
Std Dev 15.6
Entry
0
2
4
6
8
10
12
0
10
20
30
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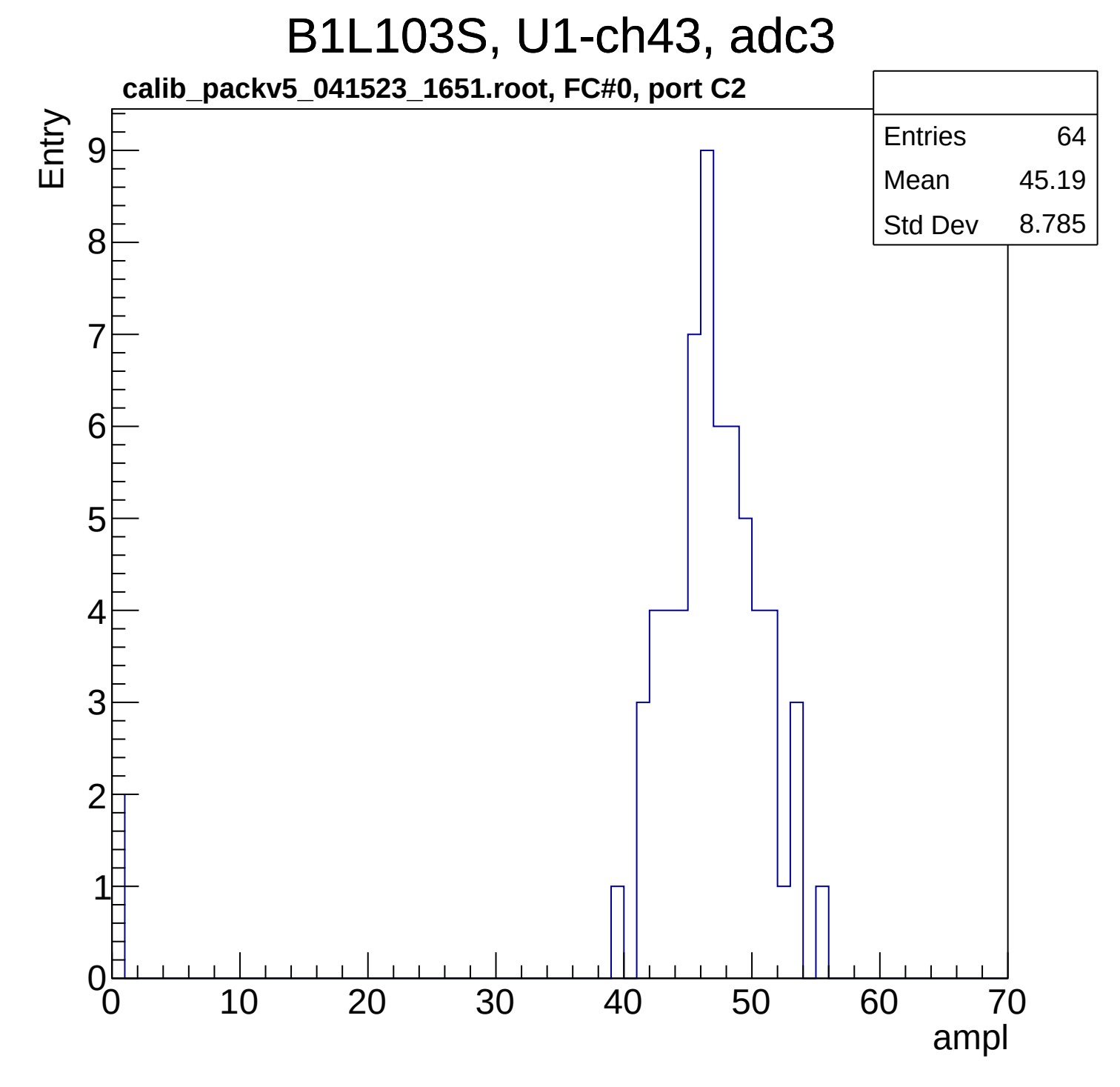
50
60
70
ampl


B1L103S, U1-ch43, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 45.19
Std Dev 8.785
Entry
ampl
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7
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0
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40
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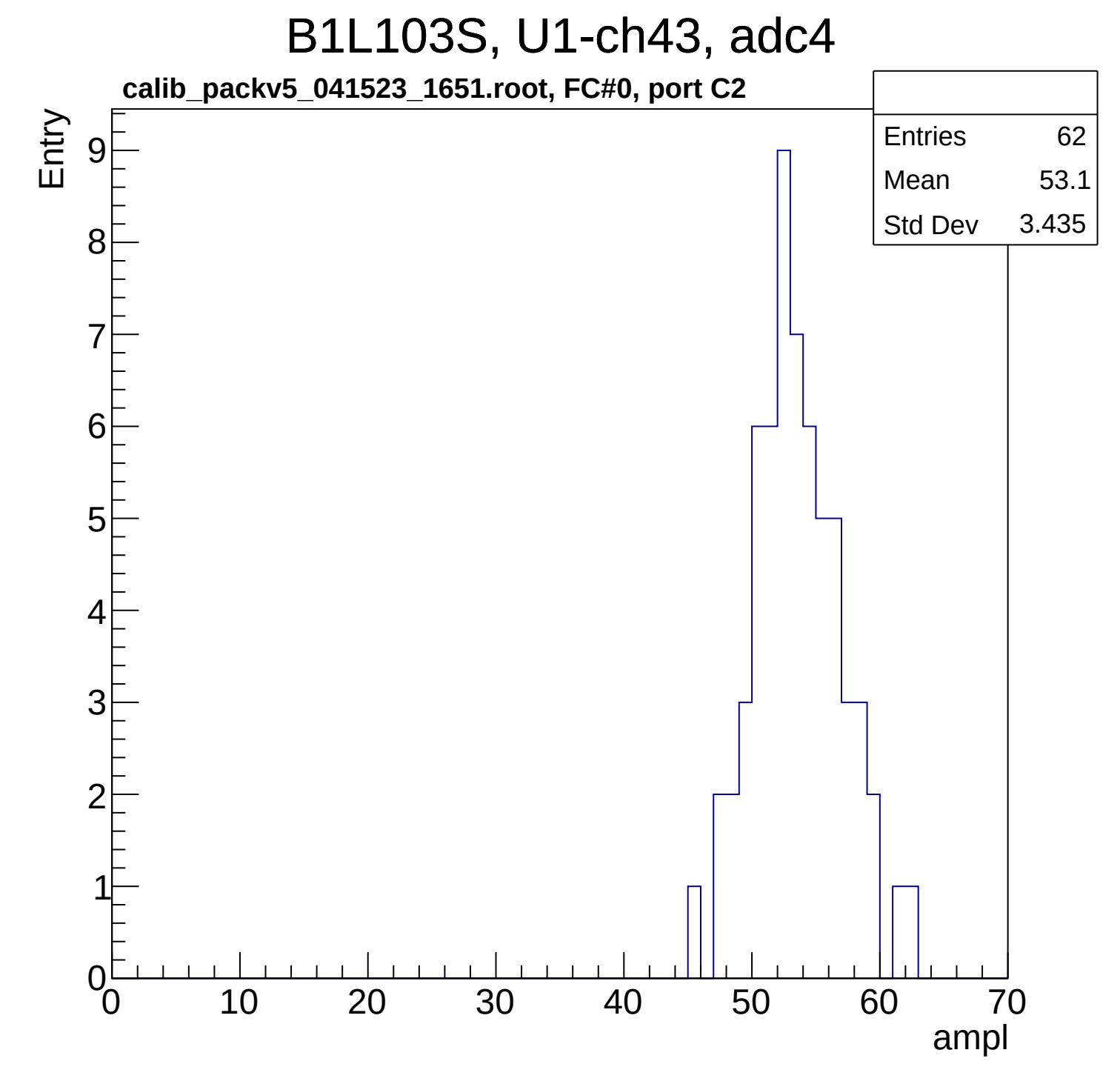
60
70


B1L103S, U1-ch43, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 53.1
Std Dev 3.435
Entry
ampl
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2
3
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5
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7
8
9
0
10
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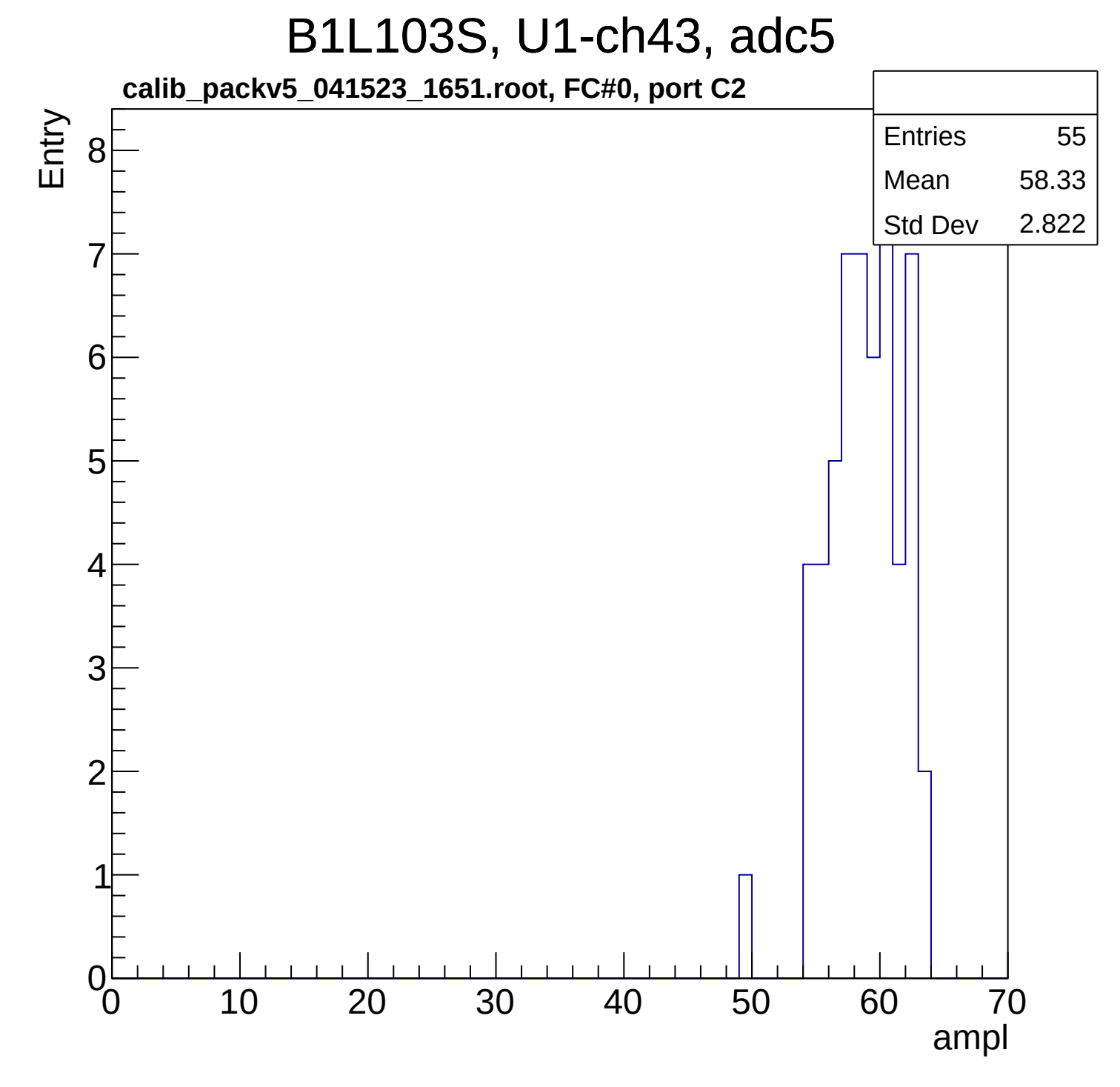
40
50
60
70


B1L103S, U1-ch43, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 58.33
Std Dev 2.822
Entry
ampl
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5
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7
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60
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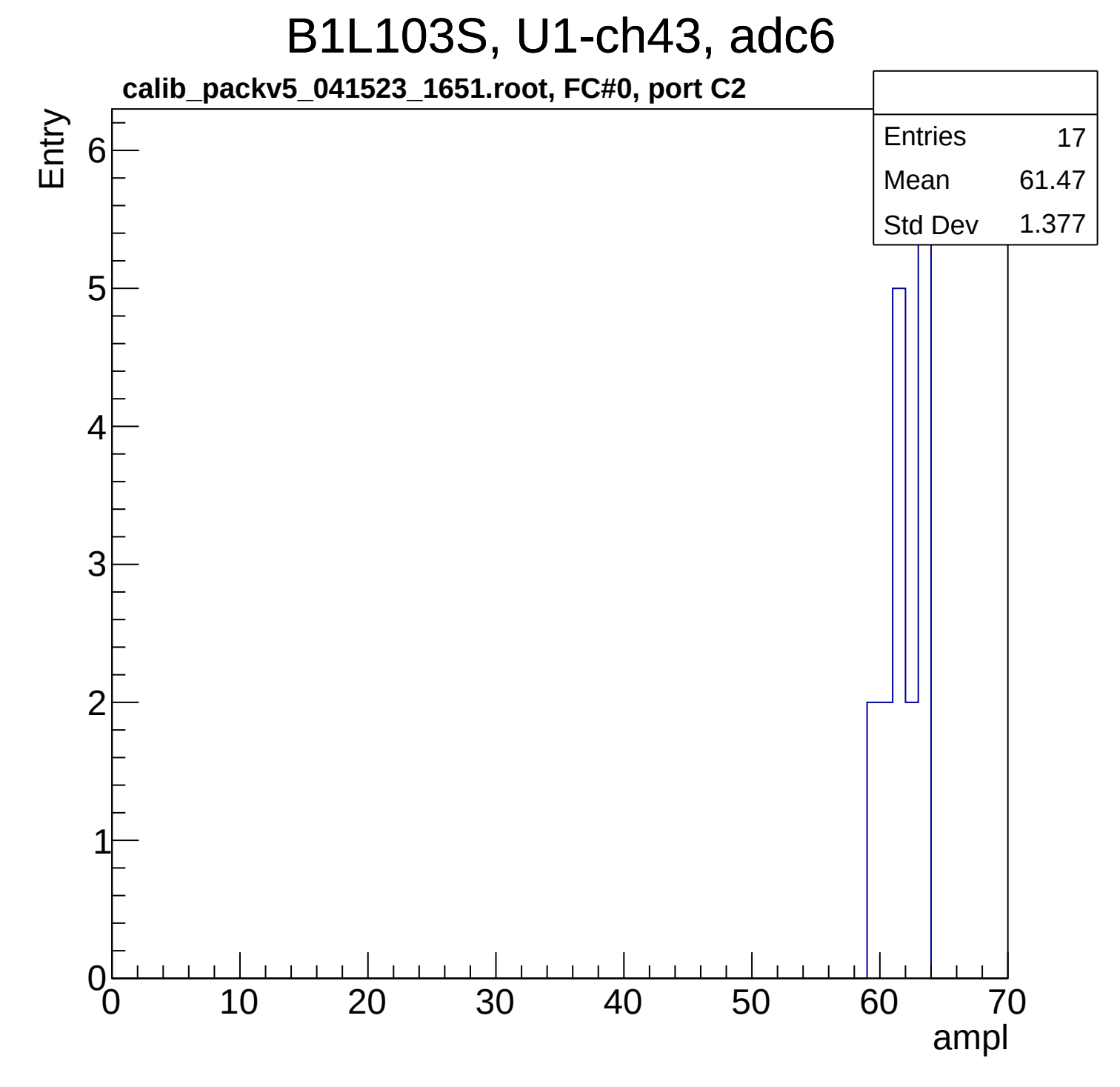
B1L103S, U1-ch43, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 17
Mean 61.47
Std Dev 1.377
Entry
ampl
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5
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0
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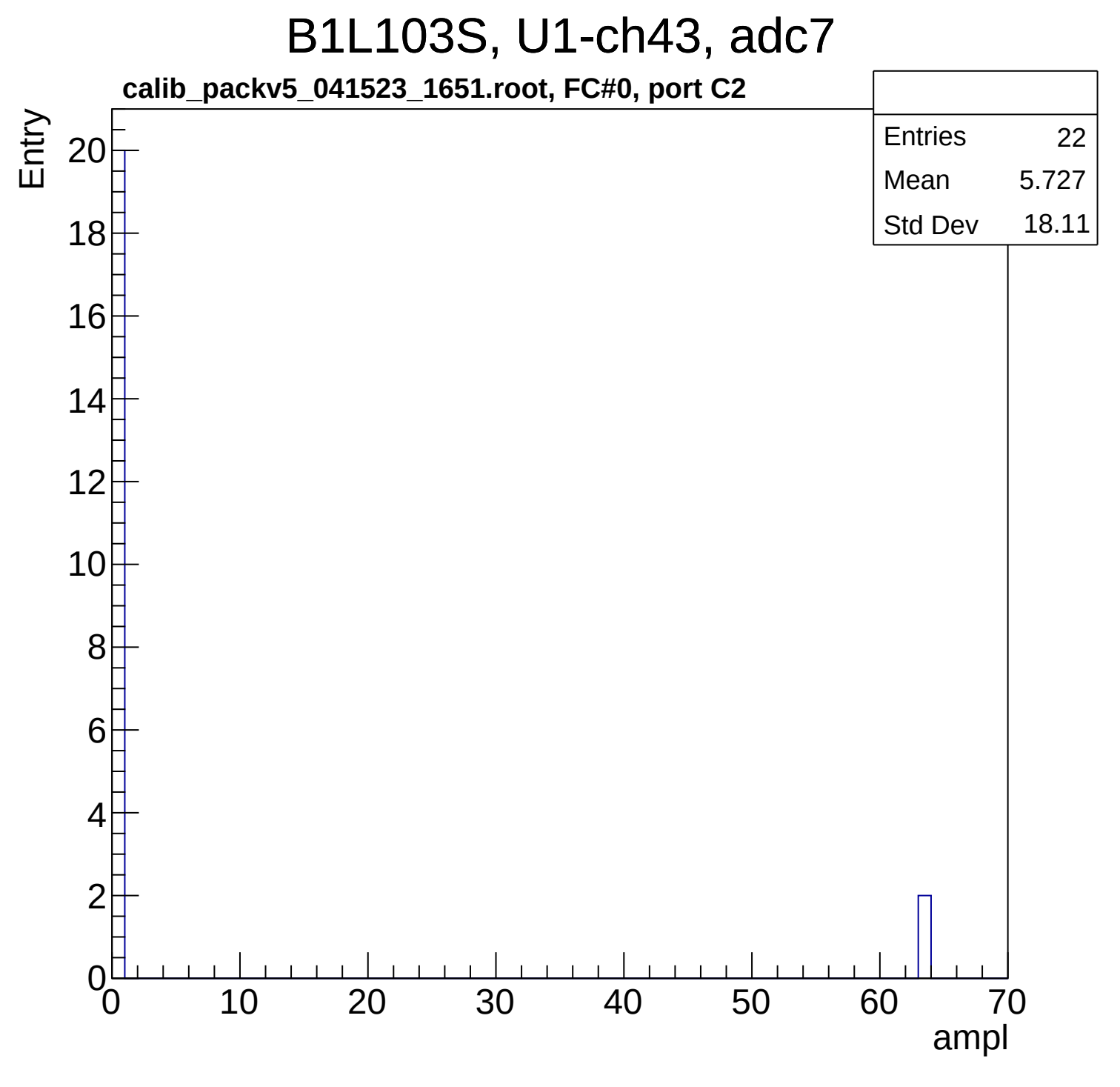
20
30
40
50
60
70


B1L103S, U1-ch43, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 5.727
Std Dev 18.11
Entry
0
2
4
6
8
10
12
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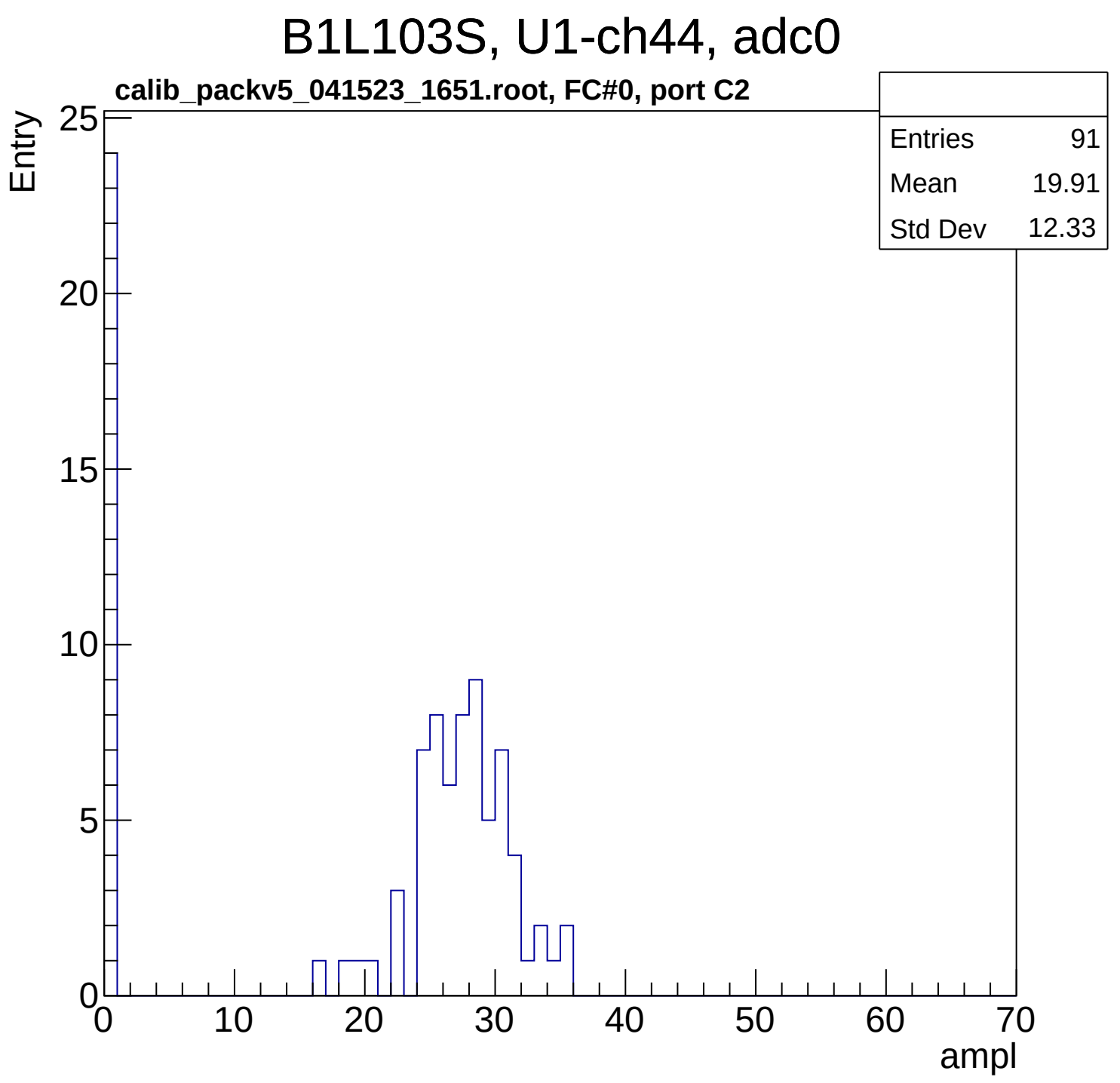
16
18
20
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch44, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 91
Mean 19.91
Std Dev 12.33
Entry
ampl
0
5
10
15
20
25
0
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30
40
50
60
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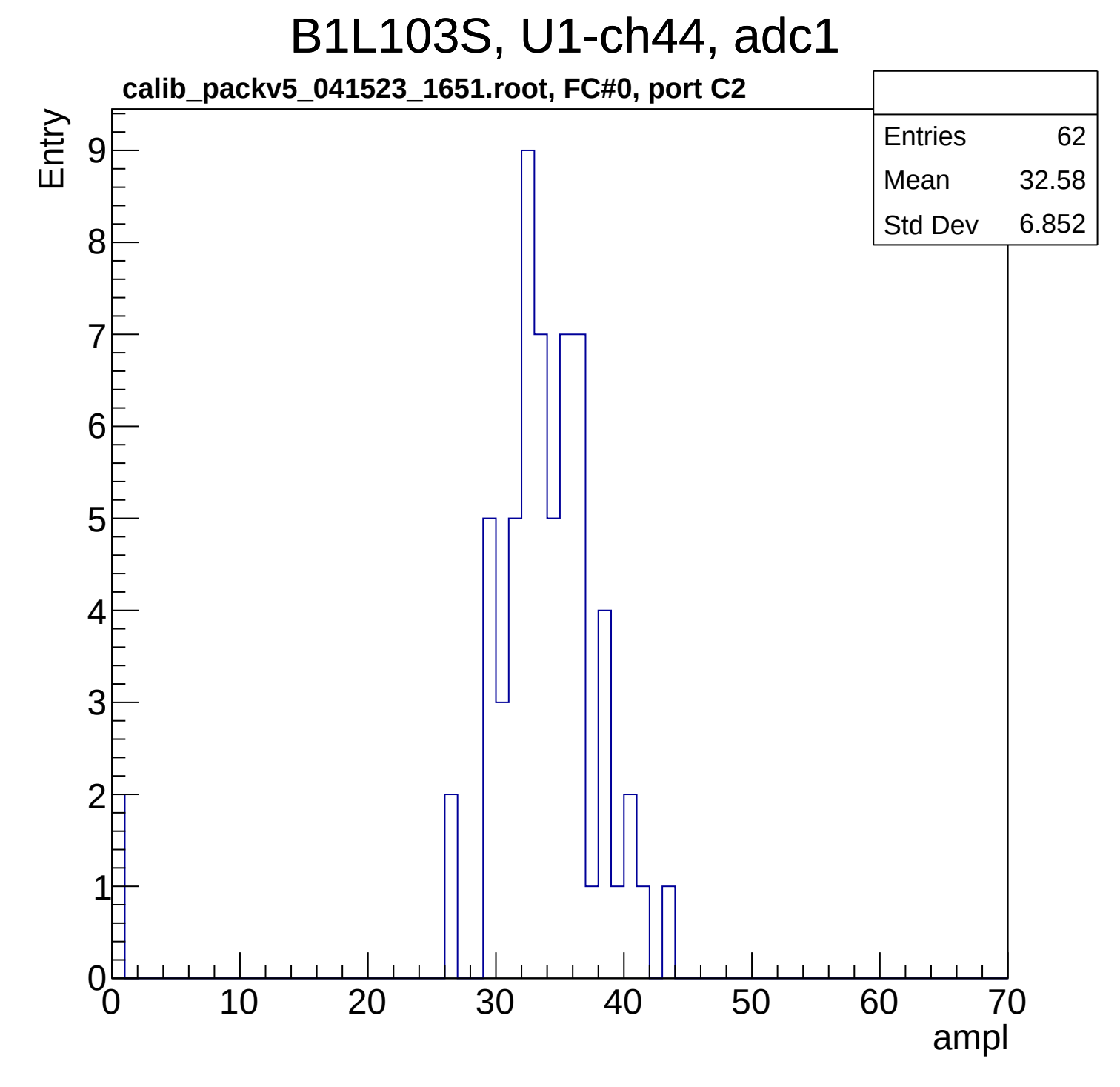
B1L103S, U1-ch44, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 32.58
Std Dev 6.852
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
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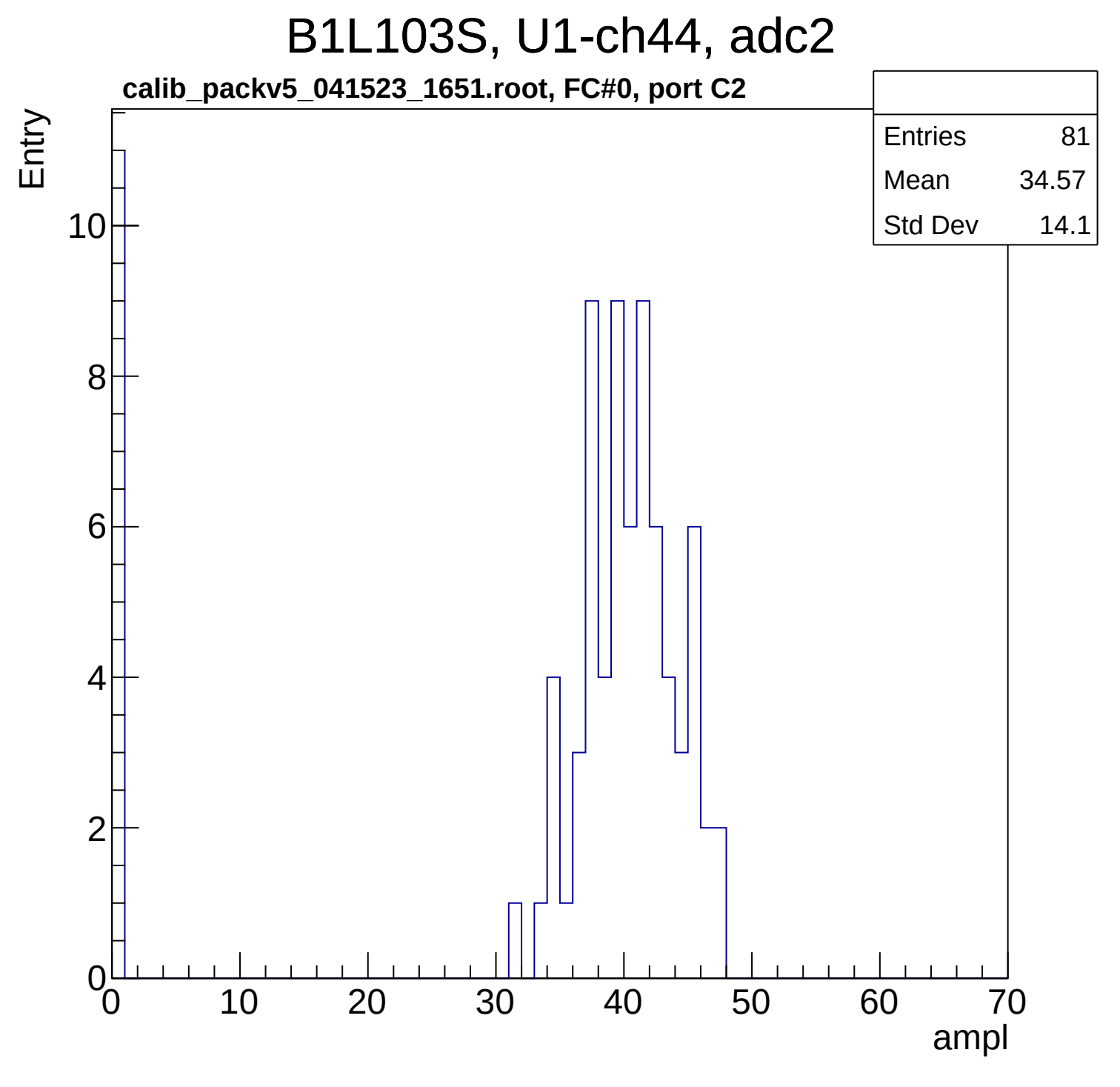
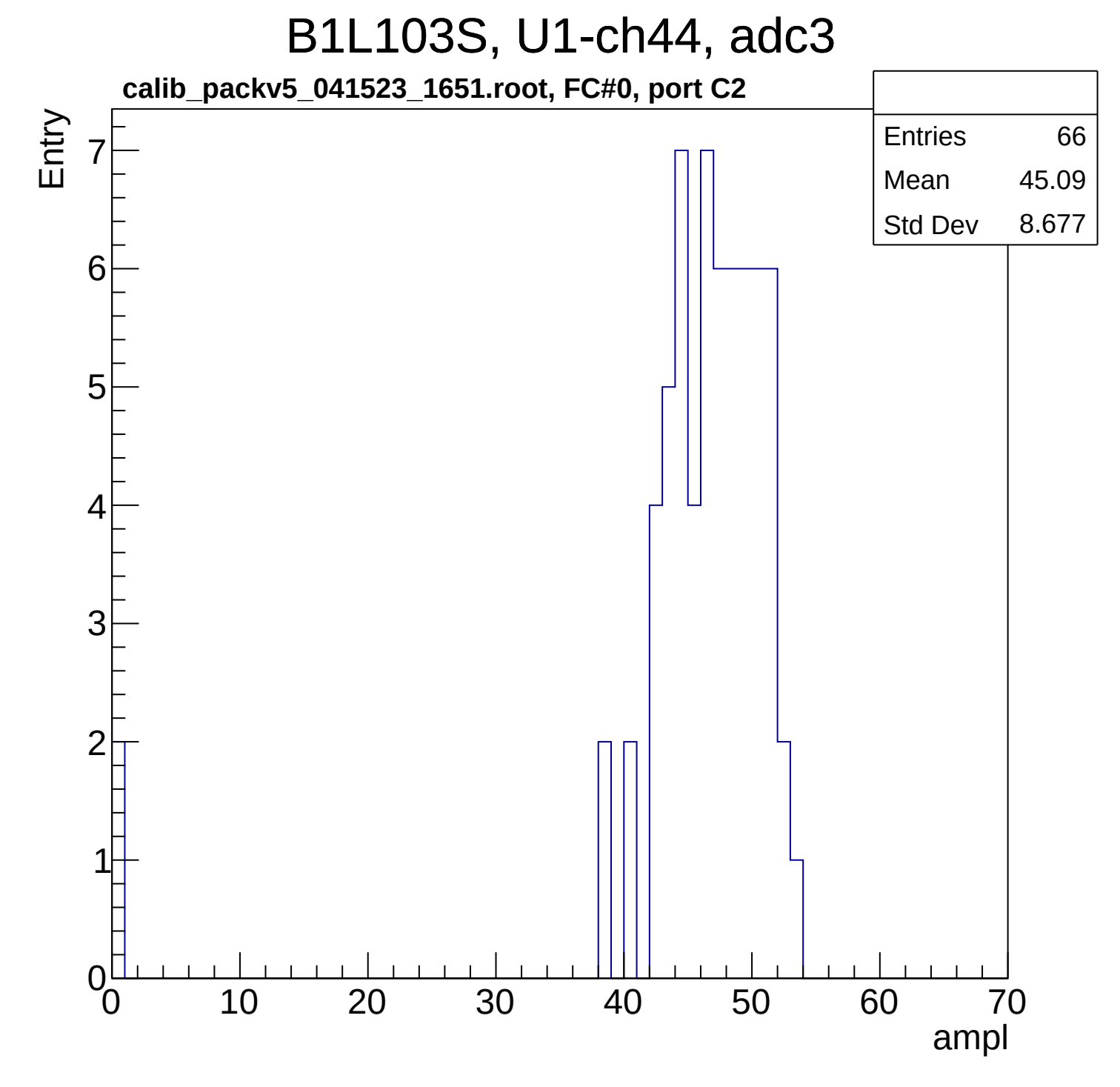
20
30
40
50
60
70


B1L103S, U1-ch44, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 34.57
Std Dev 14.1
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch44, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 45.09
Std Dev 8.677
Entry
ampl
0
1
2
3
4
5
6
7
0
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20
30
40
50
60
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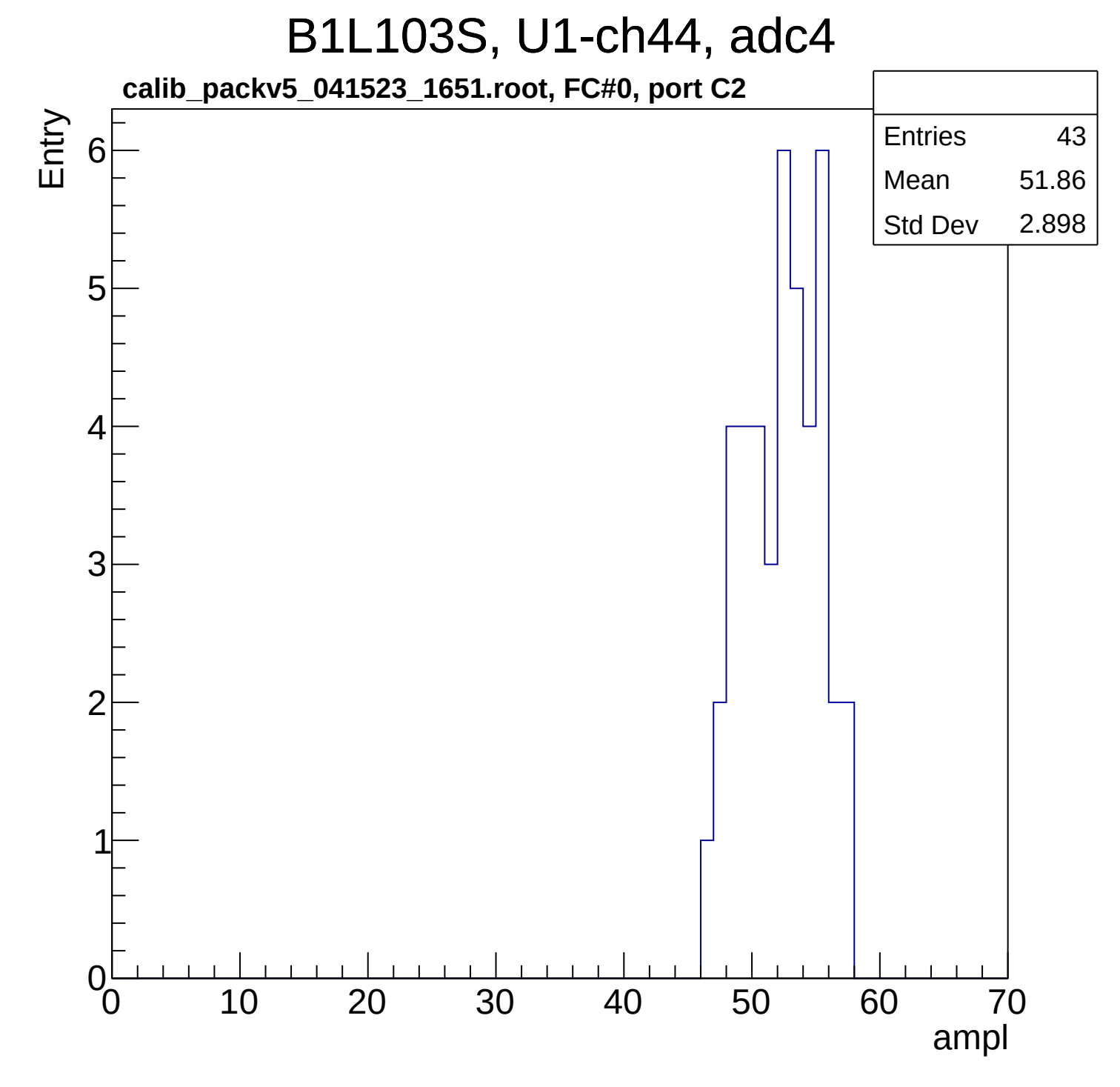
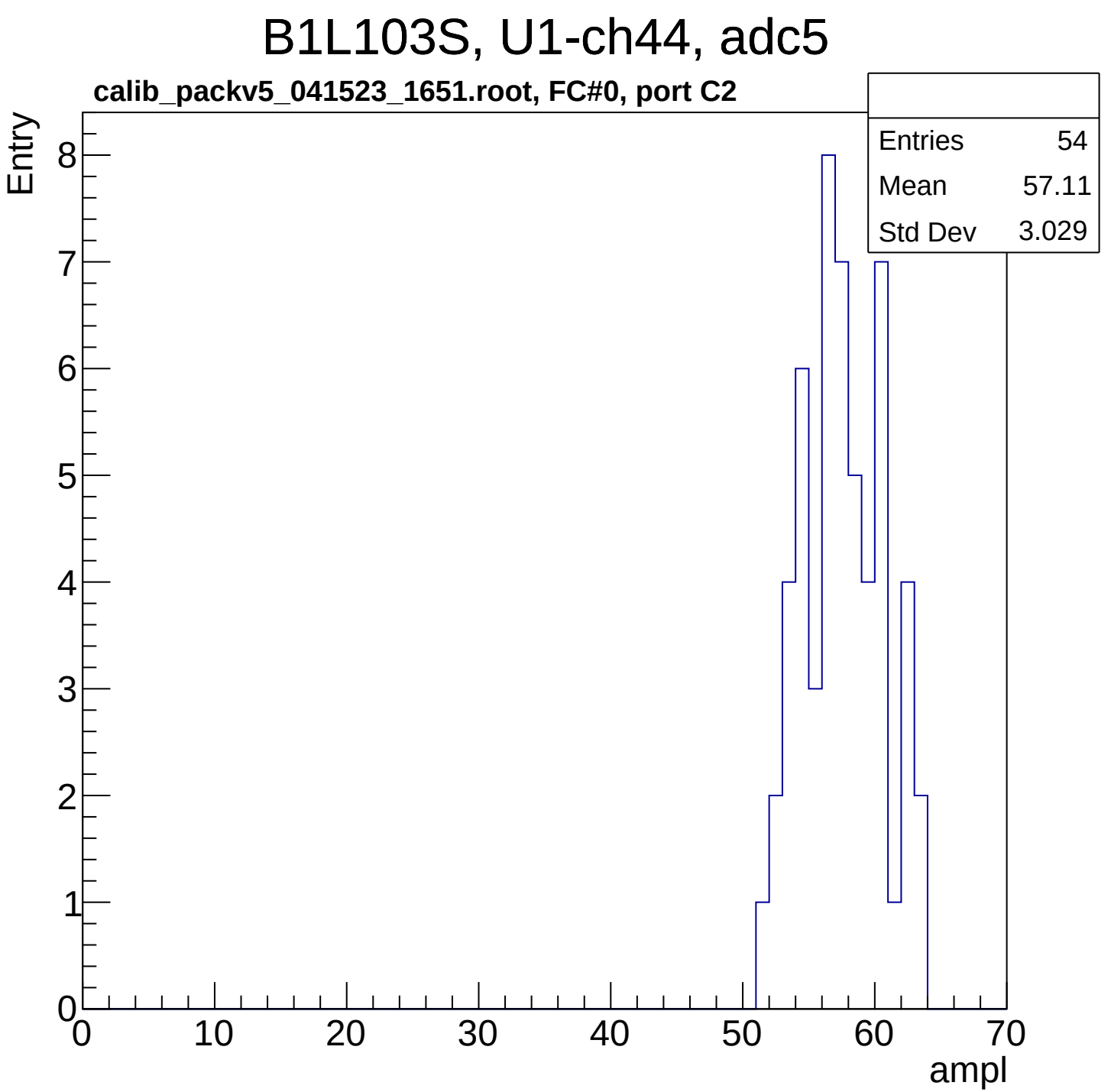

B1L103S, U1-ch44, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 43
Mean 51.86
Std Dev 2.898
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U1-ch44, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 57.11
Std Dev 3.029
Entry
ampl
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2
3
4
5
6
7
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0
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60
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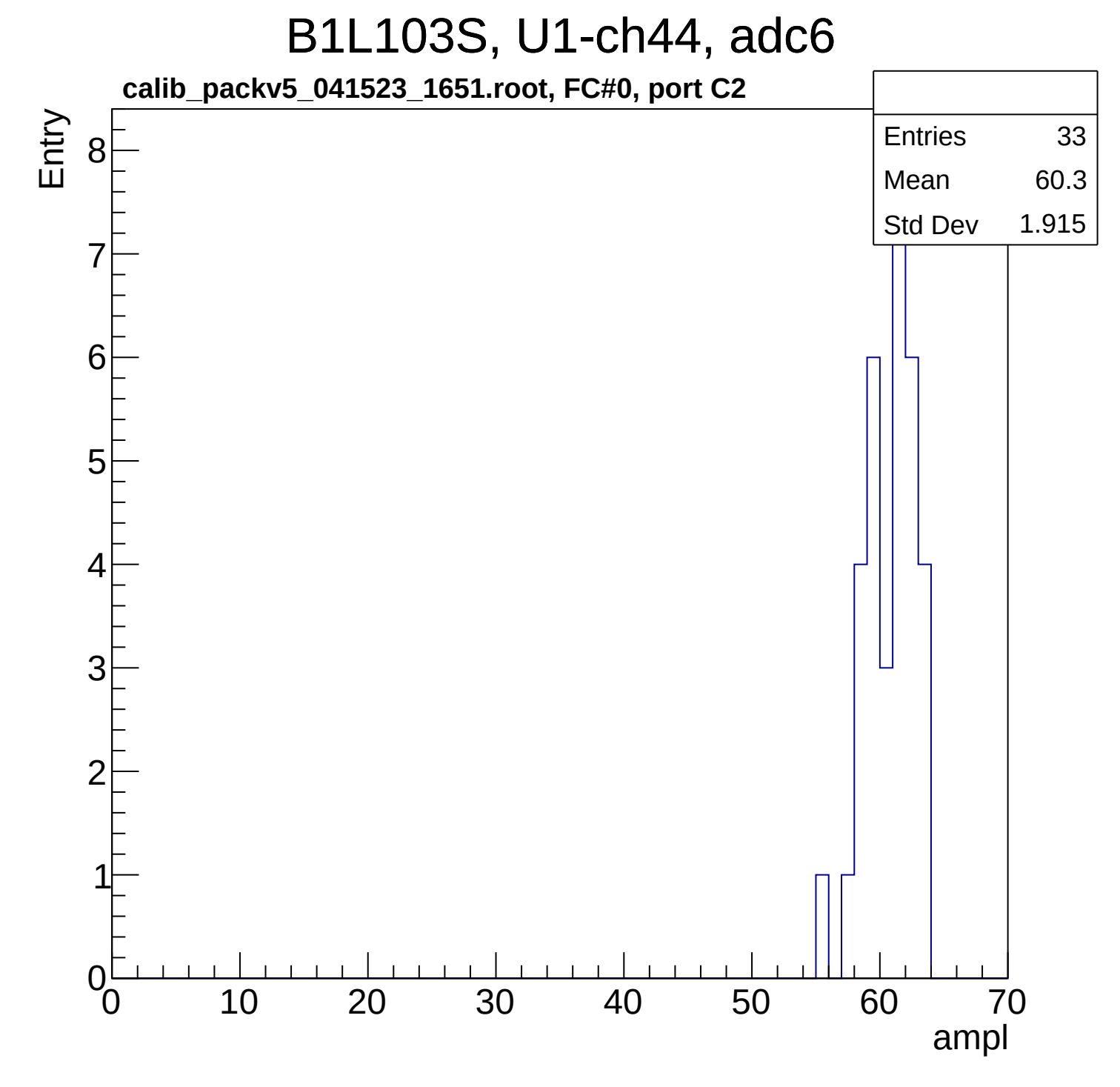
B1L103S, U1-ch44, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 33
Mean 60.3
Std Dev 1.915
Entry
ampl
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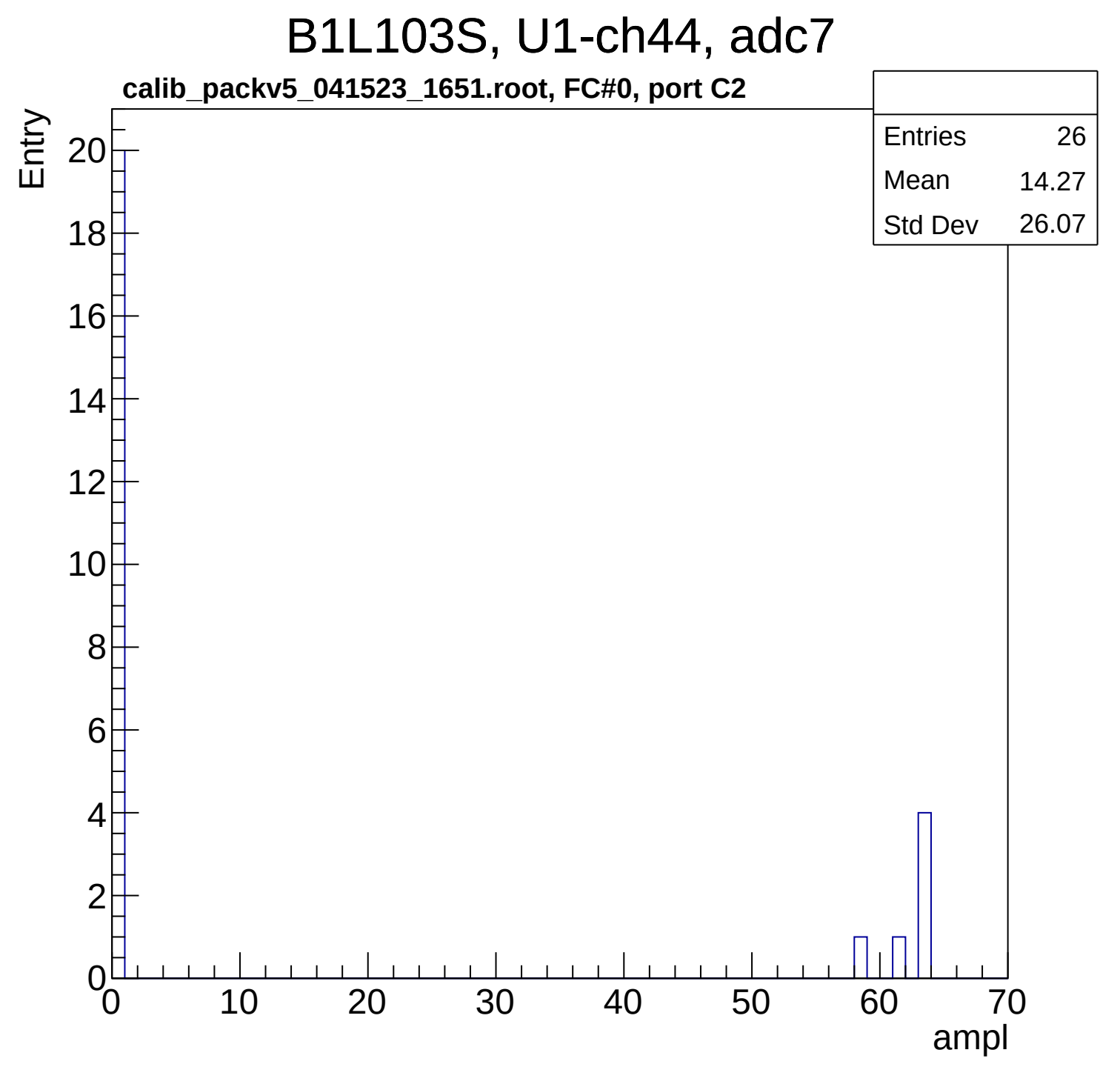
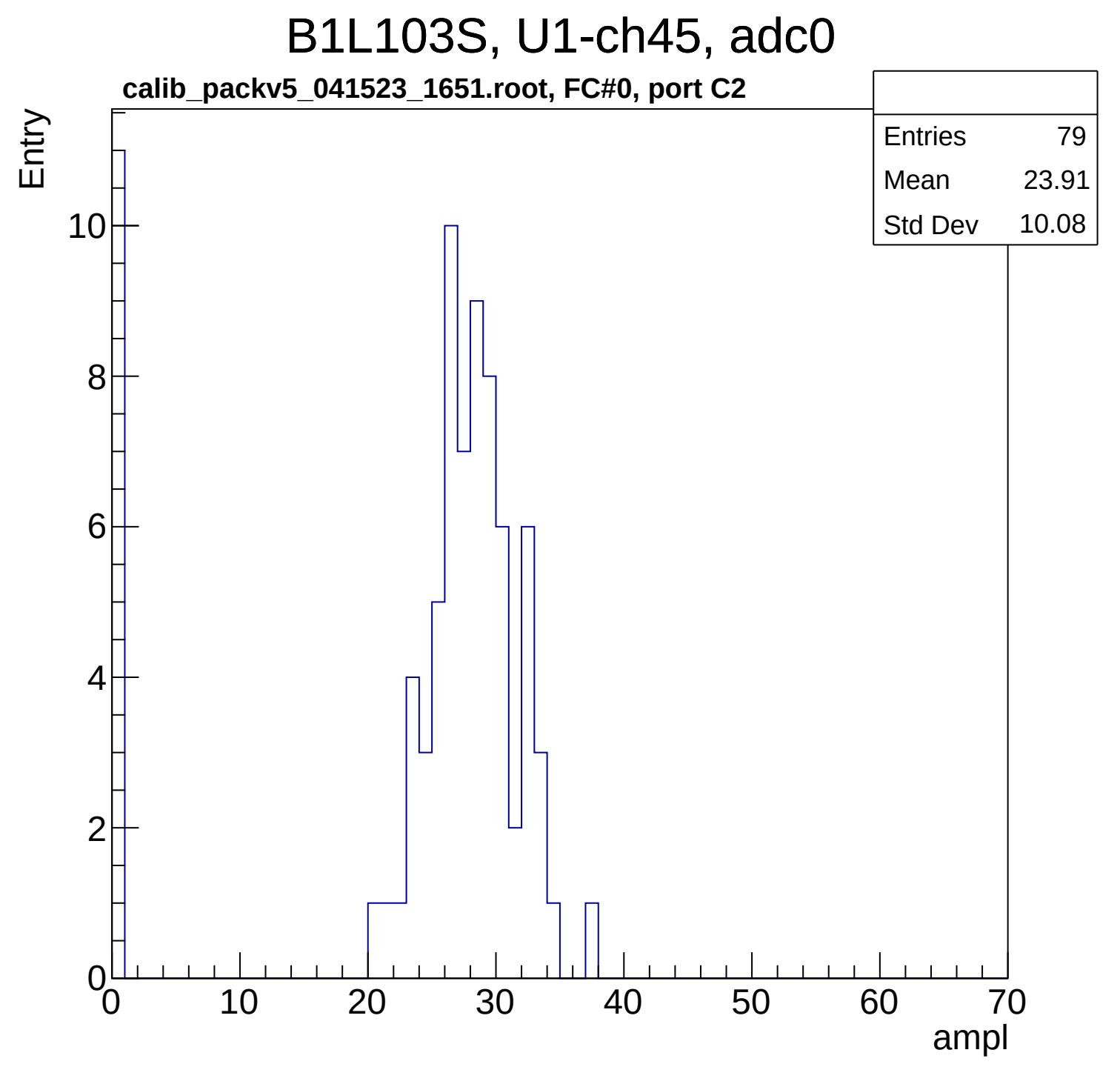
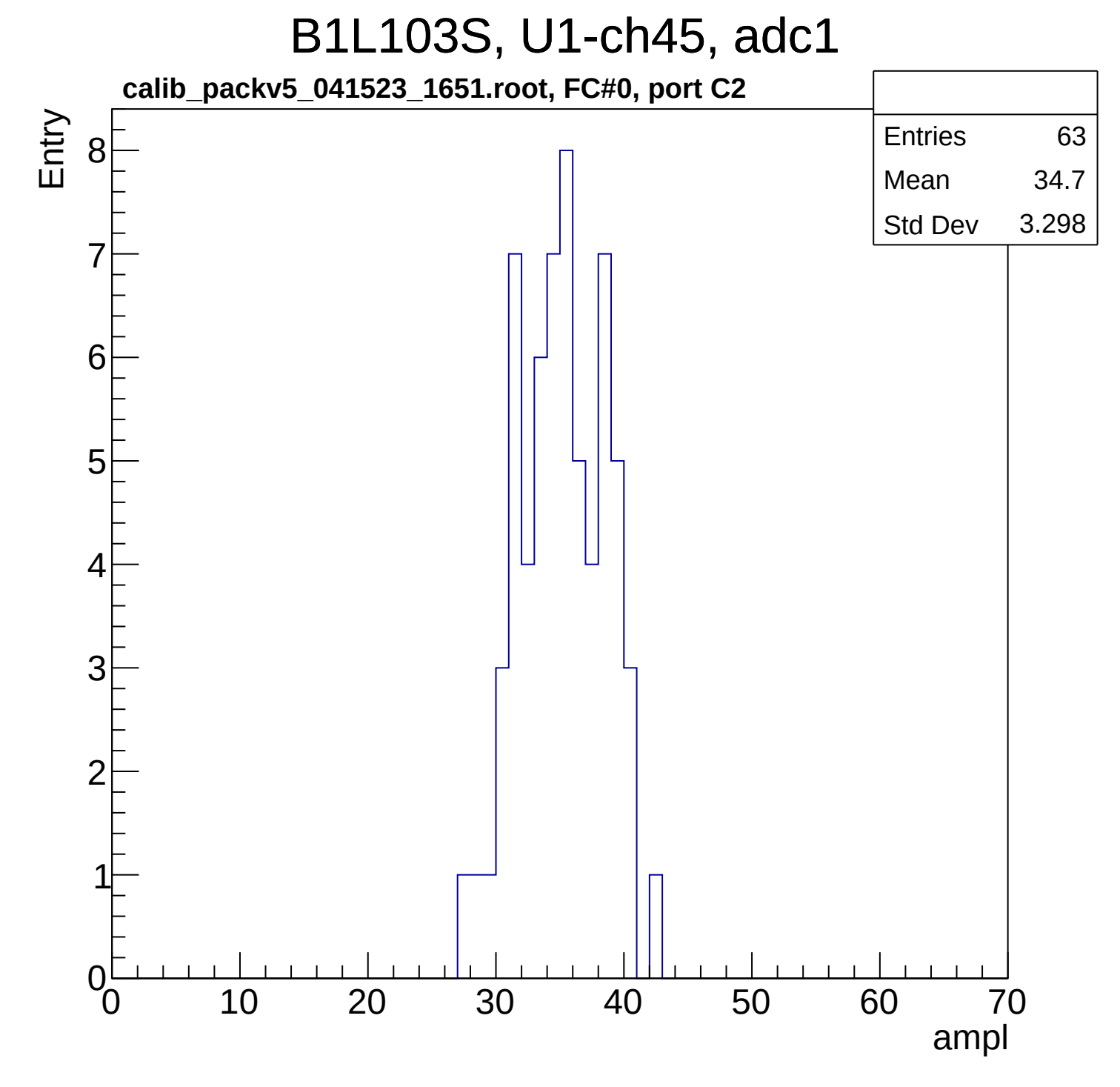
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U1-ch44, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 26
Mean 14.27
Std Dev 26.07
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70


B1L103S, U1-ch45, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 23.91
Std Dev 10.08
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch45, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 34.7
Std Dev 3.298
Entry
ampl
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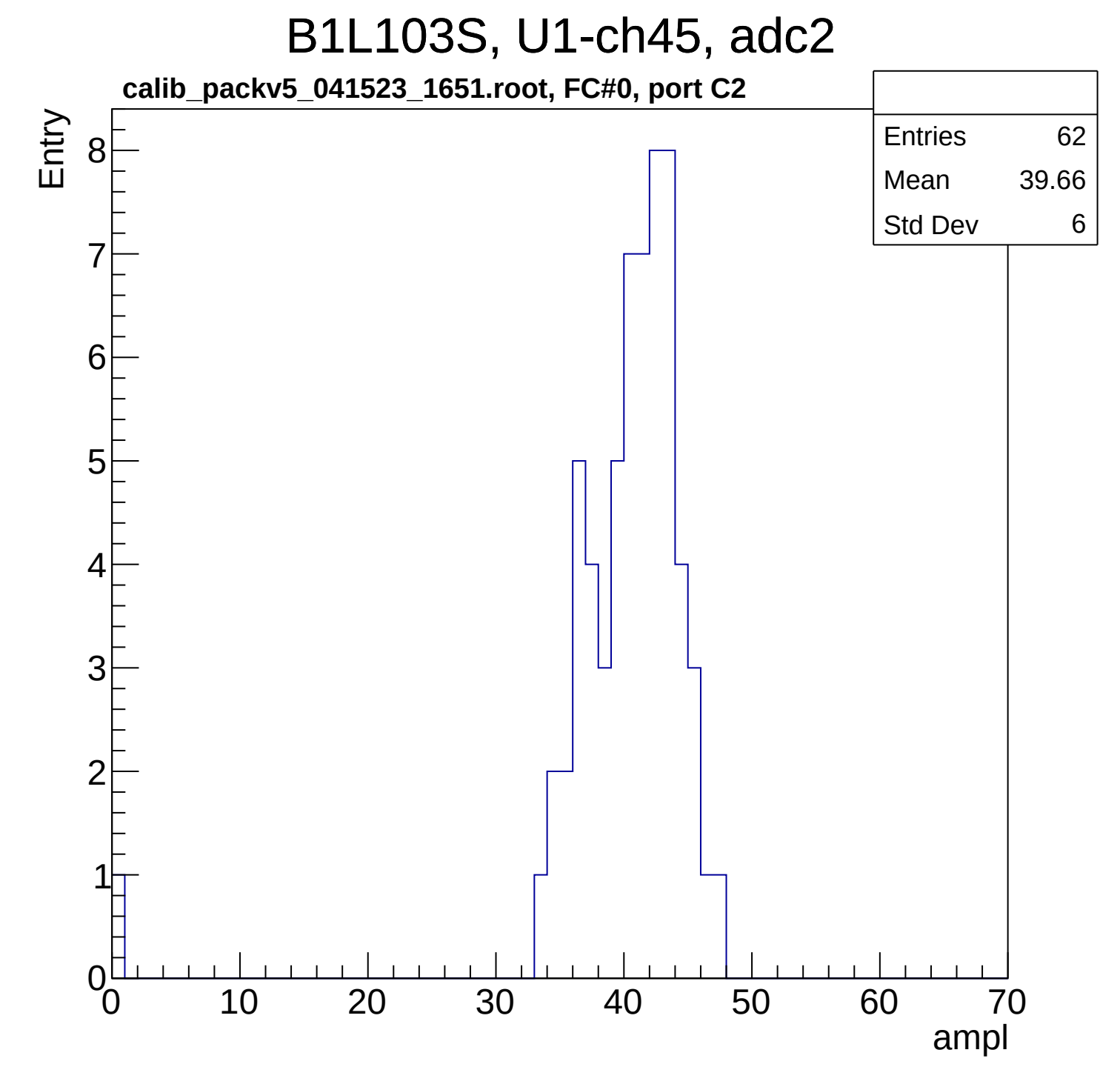
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U1-ch45, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 39.66
Std Dev 6
Entry
ampl
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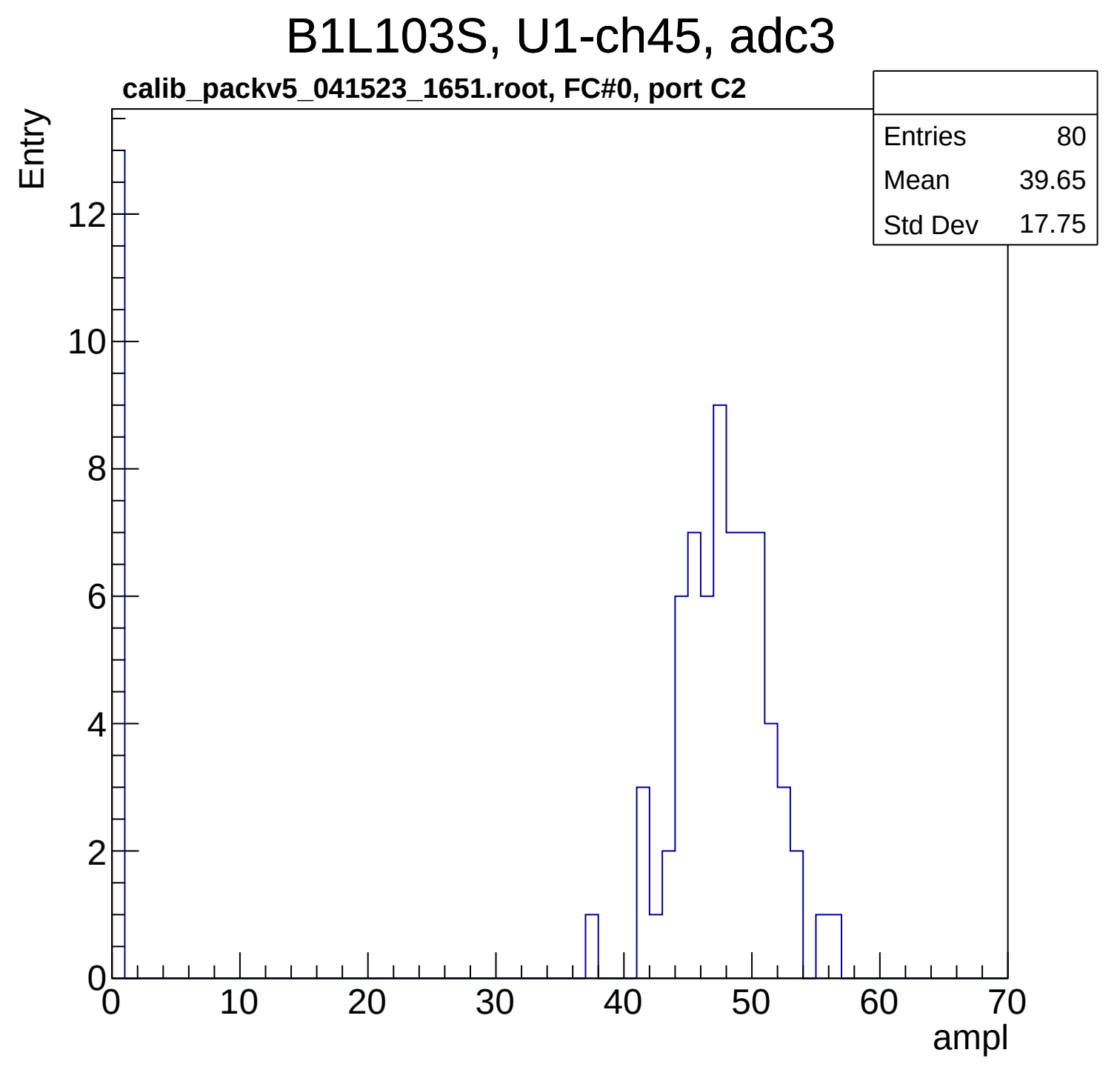
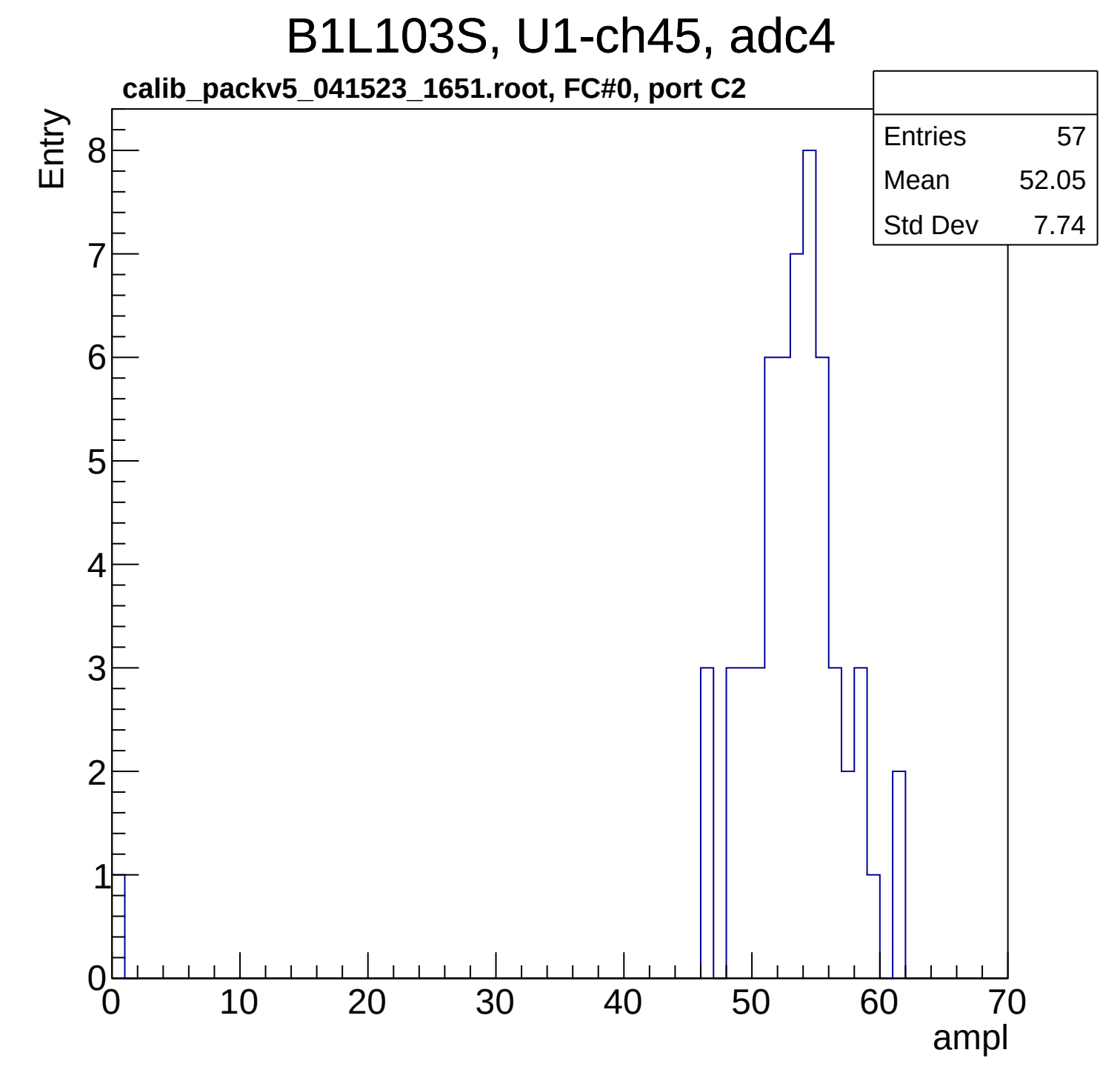
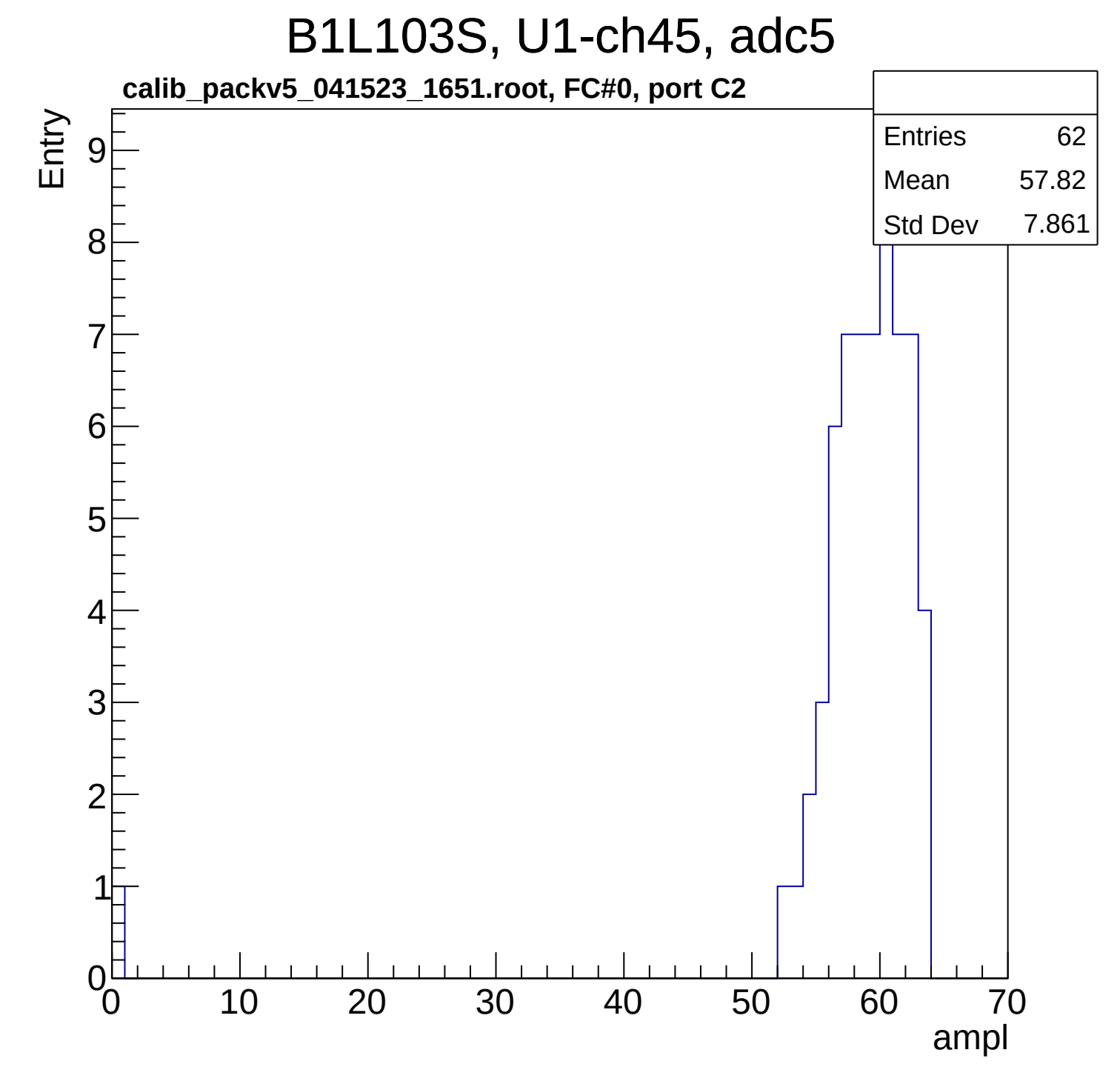
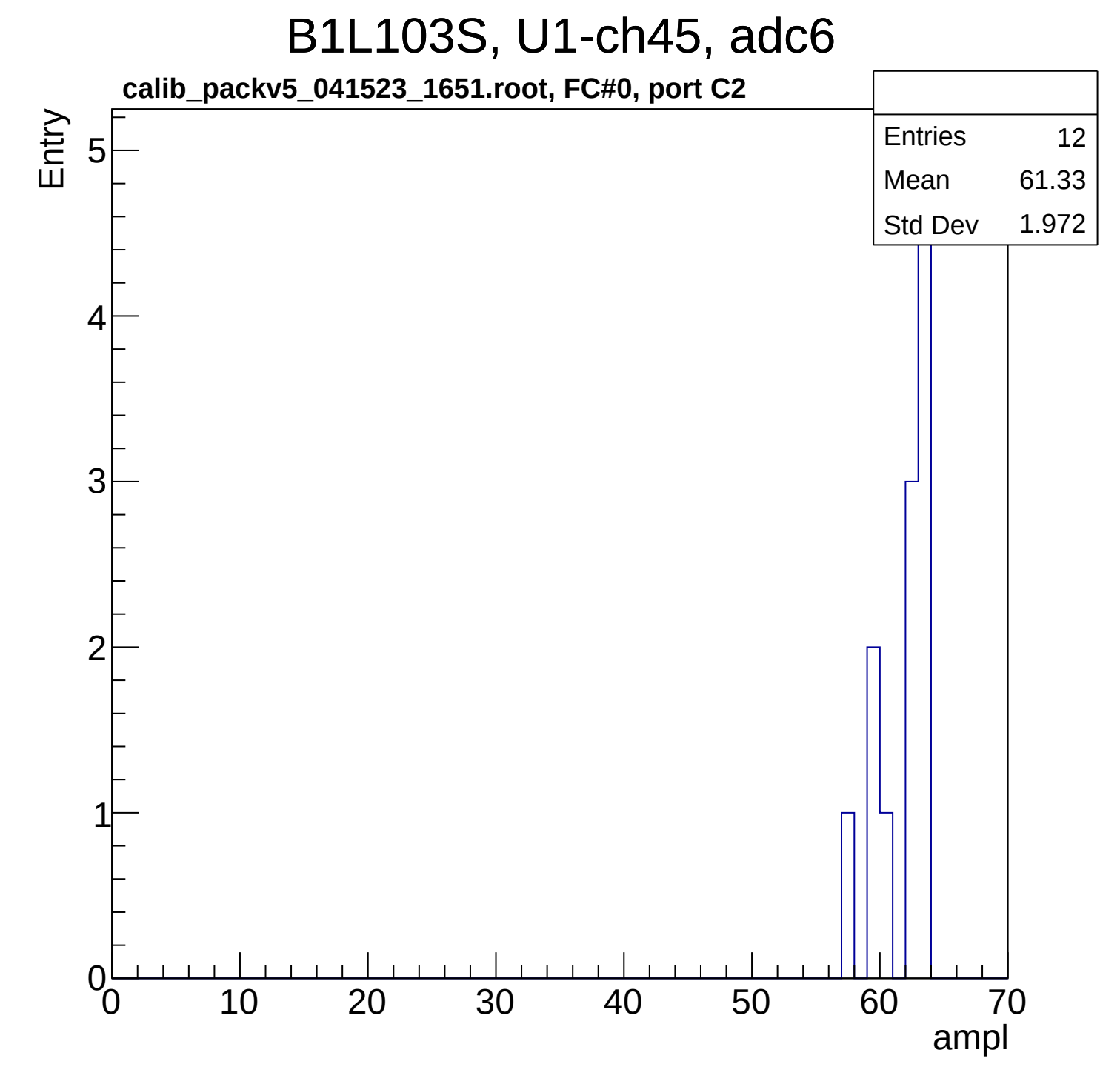
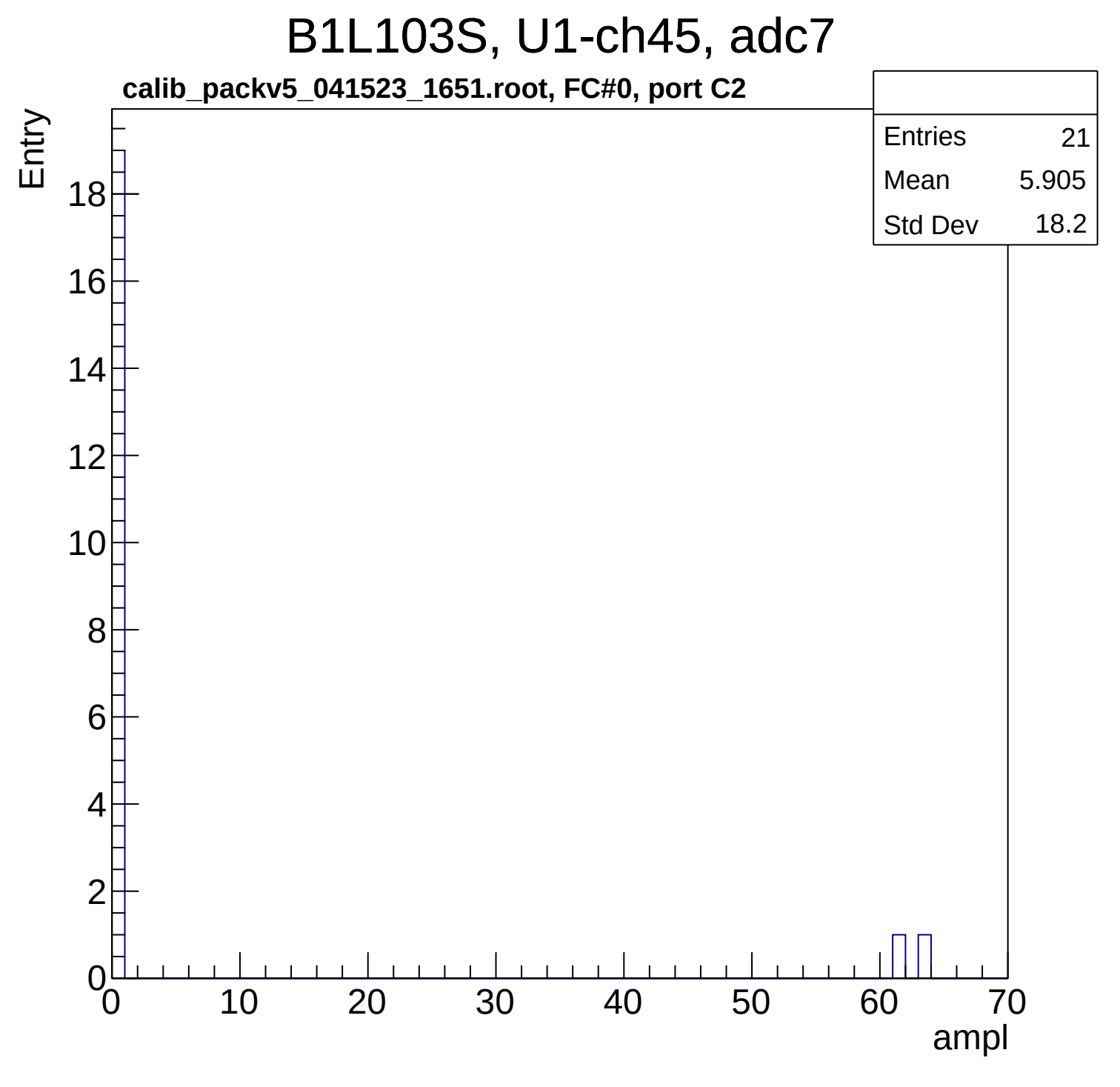
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

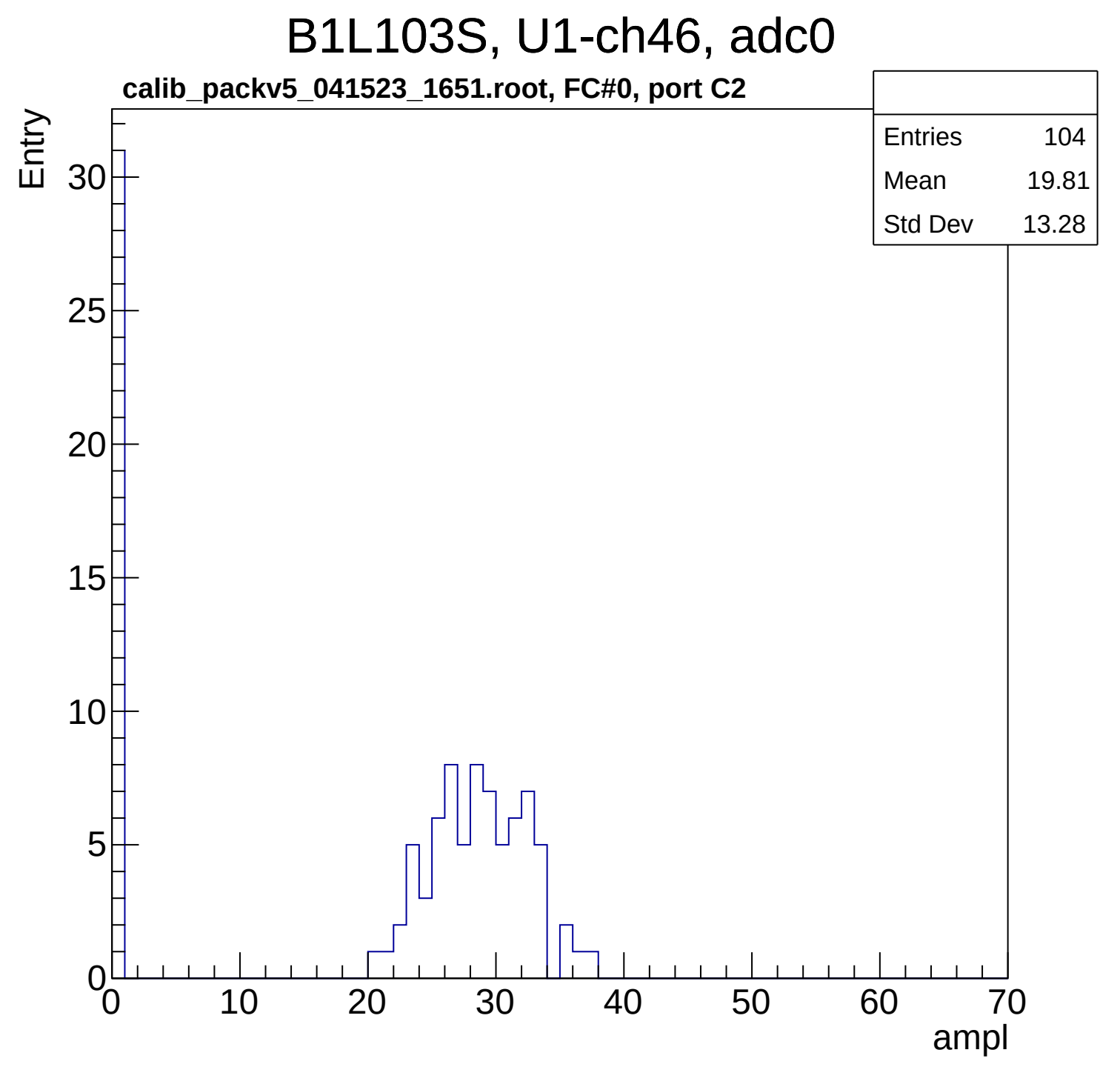

B1L103S, U1-ch45, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 39.65
Std Dev 17.75
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70

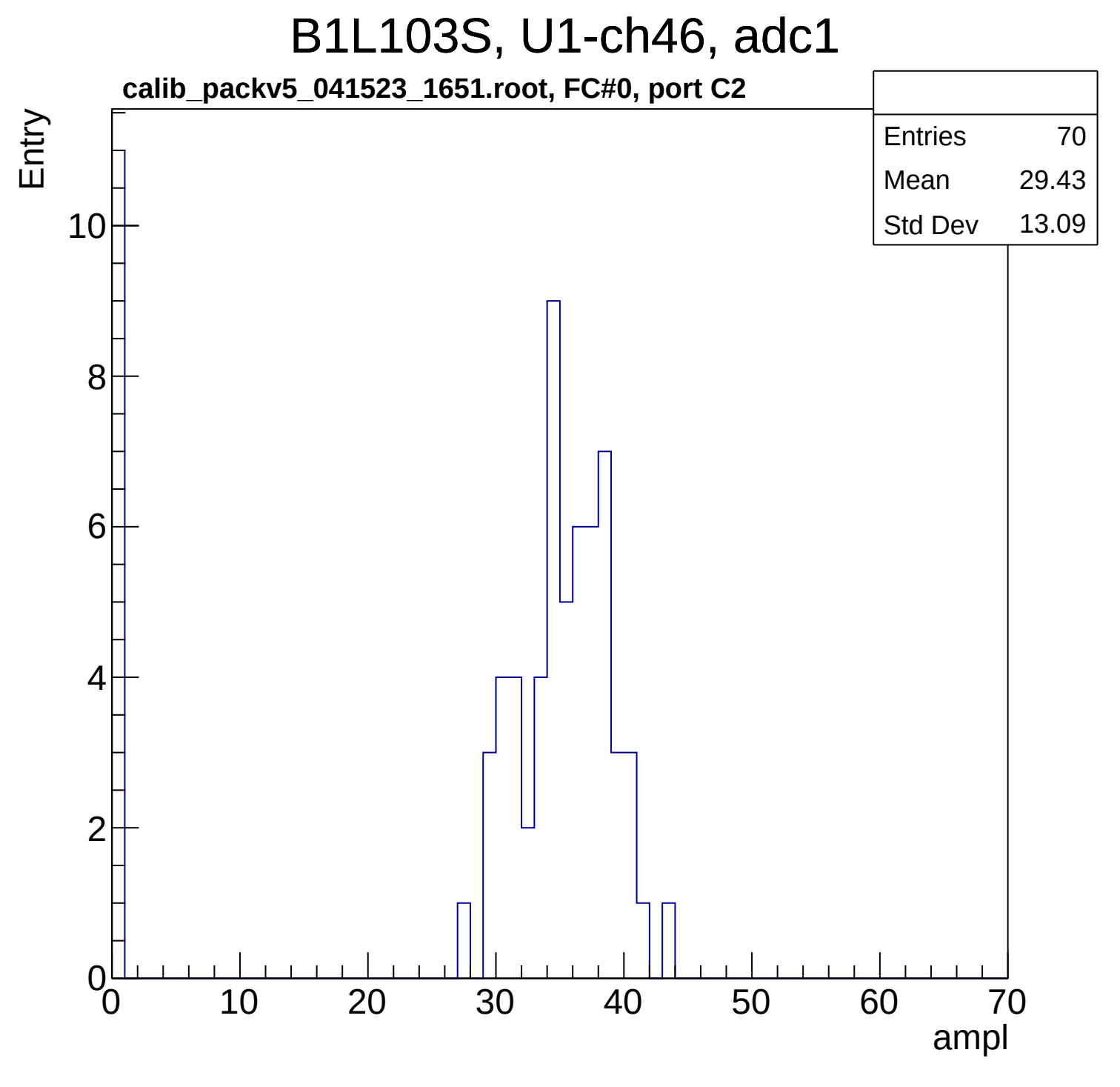

B1L103S, U1-ch45, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 52.05
Std Dev 7.74
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

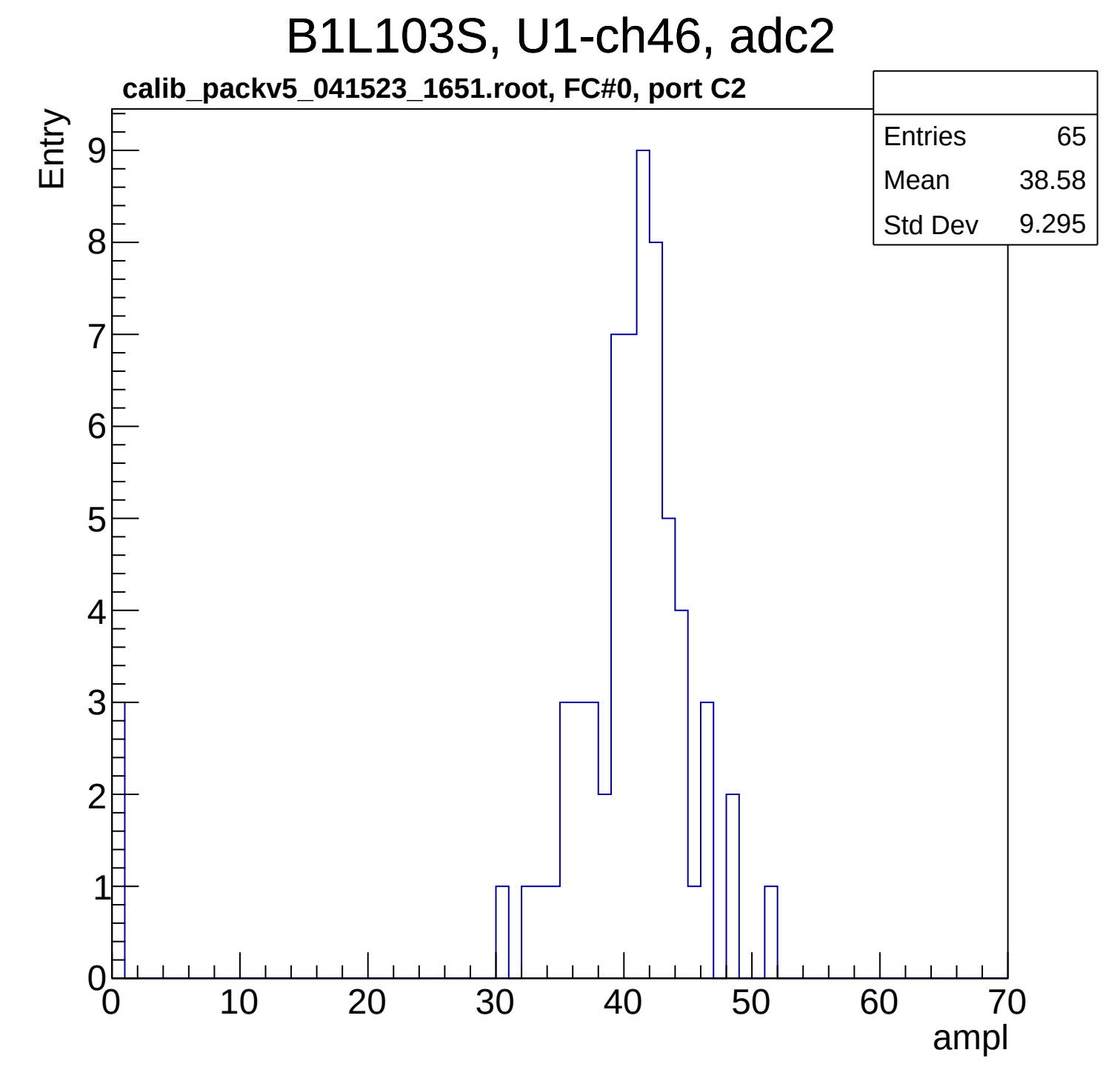

B1L103S, U1-ch45, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 57.82
Std Dev 7.861
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U1-ch45, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 61.33
Std Dev 1.972
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U1-ch45, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 5.905
Std Dev 18.2
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch46, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 104
Mean 19.81
Std Dev 13.28
Entry
0
5
10
15
20
25
30
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch46, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 29.43
Std Dev 13.09
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch46, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 38.58
Std Dev 9.295
Entry
ampl
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2
3
4
5
6
7
8
9
0
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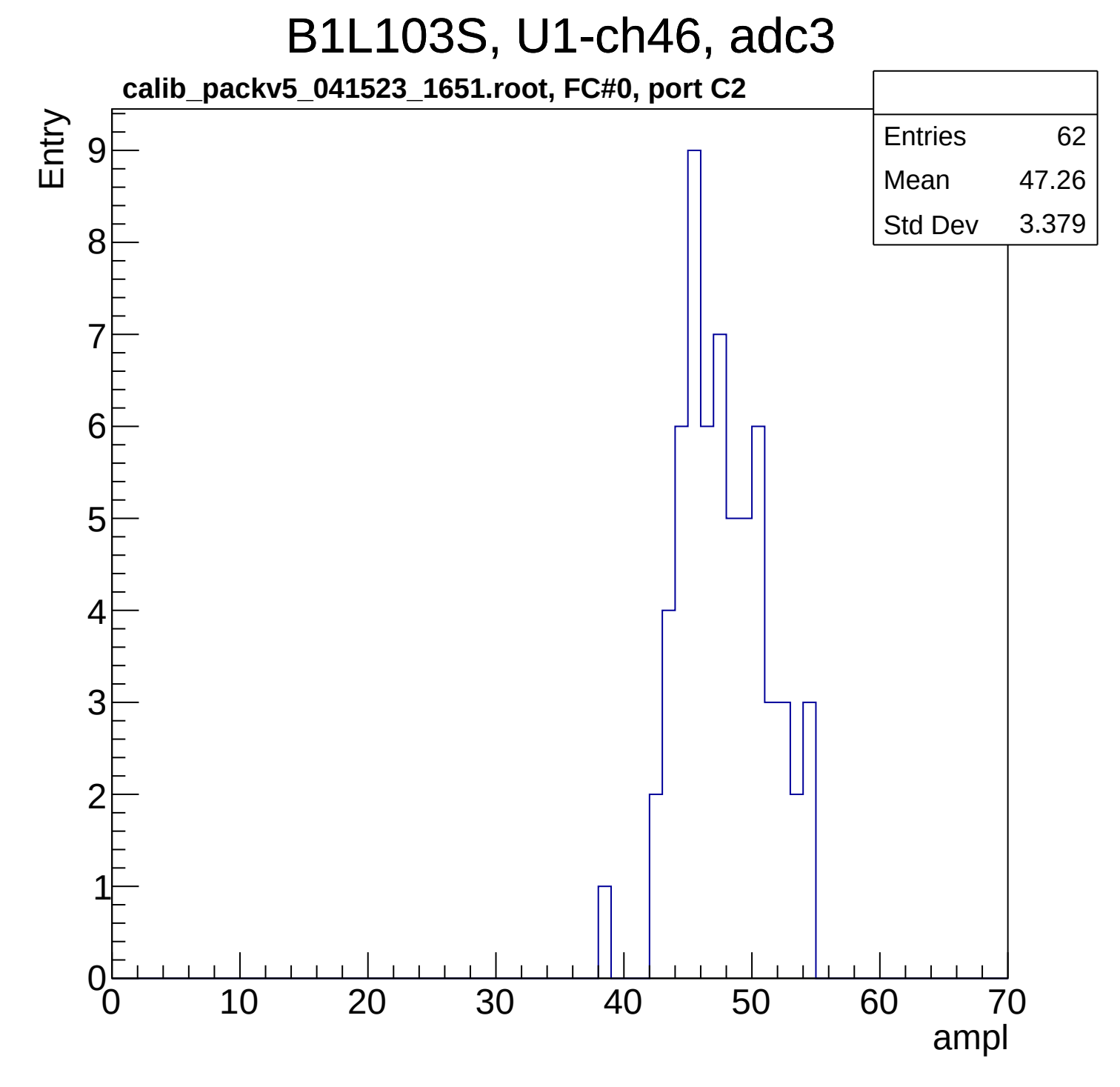
20
30
40
50
60
70


B1L103S, U1-ch46, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 47.26
Std Dev 3.379
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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40
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60
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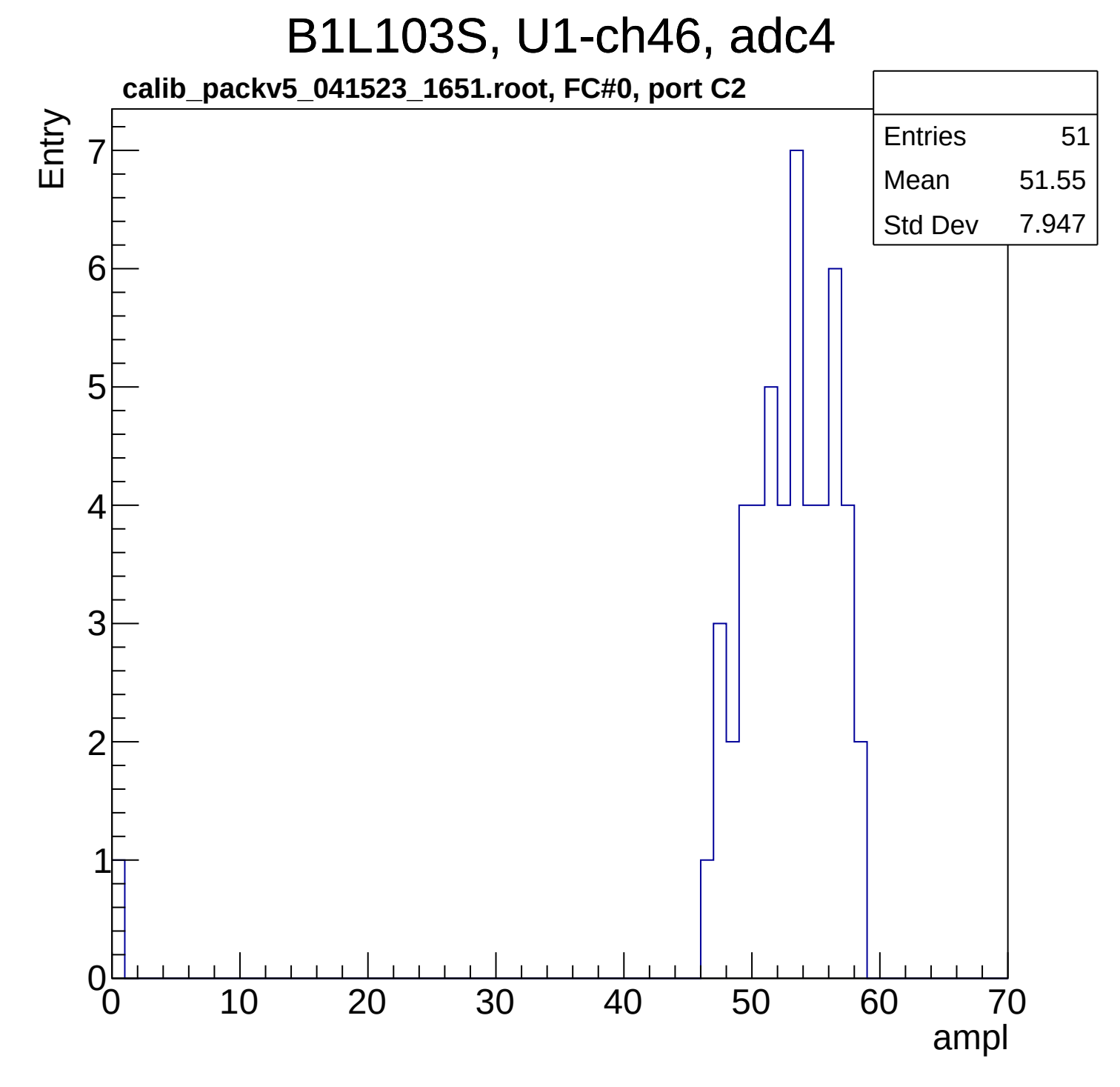
B1L103S, U1-ch46, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 51.55
Std Dev 7.947
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
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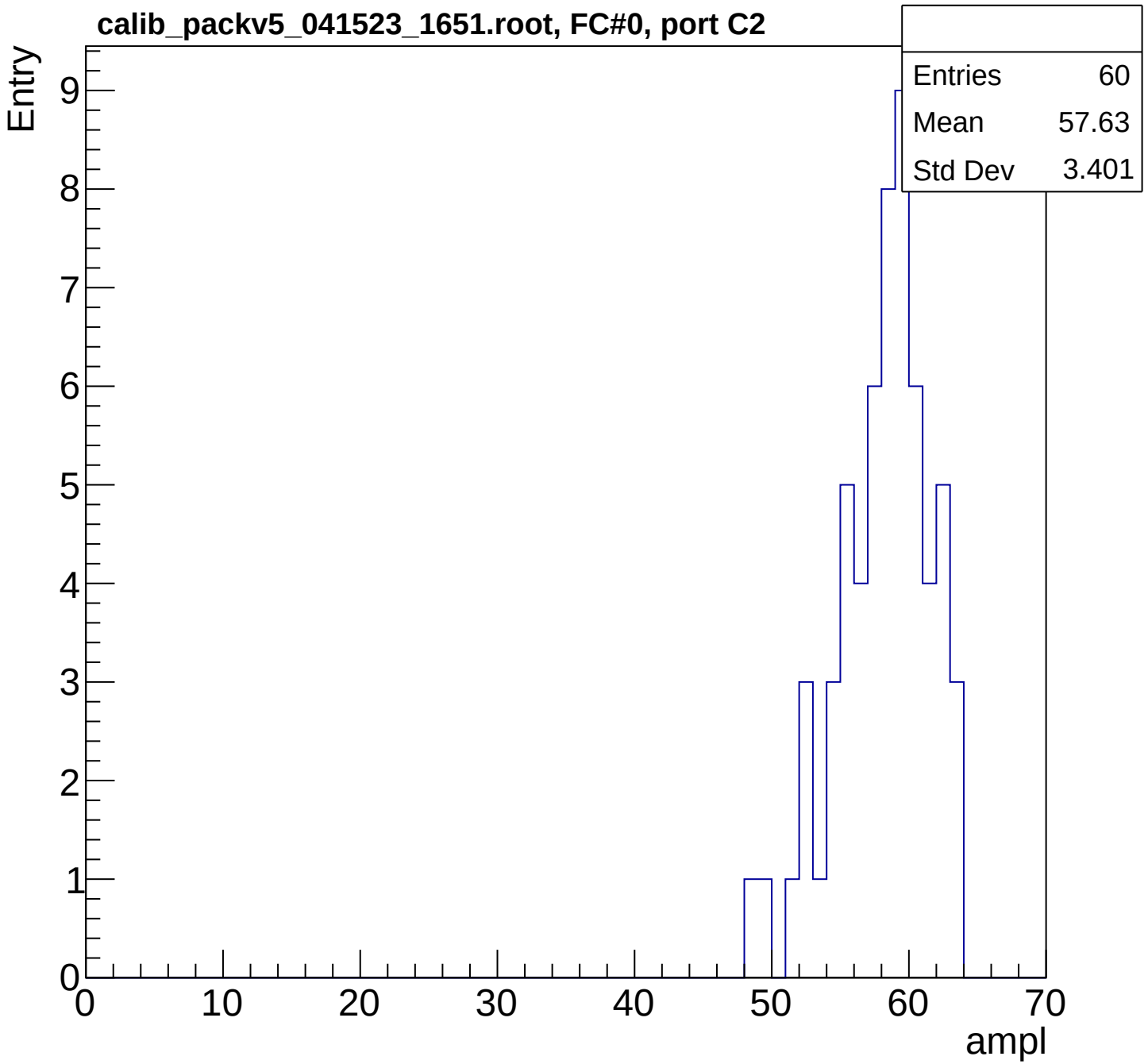
40
50
60
70


B1L103S, U1-ch46, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 57.63
Std Dev 3.401
Entry
ampl
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2
3
4
5
6
7
8
9
0
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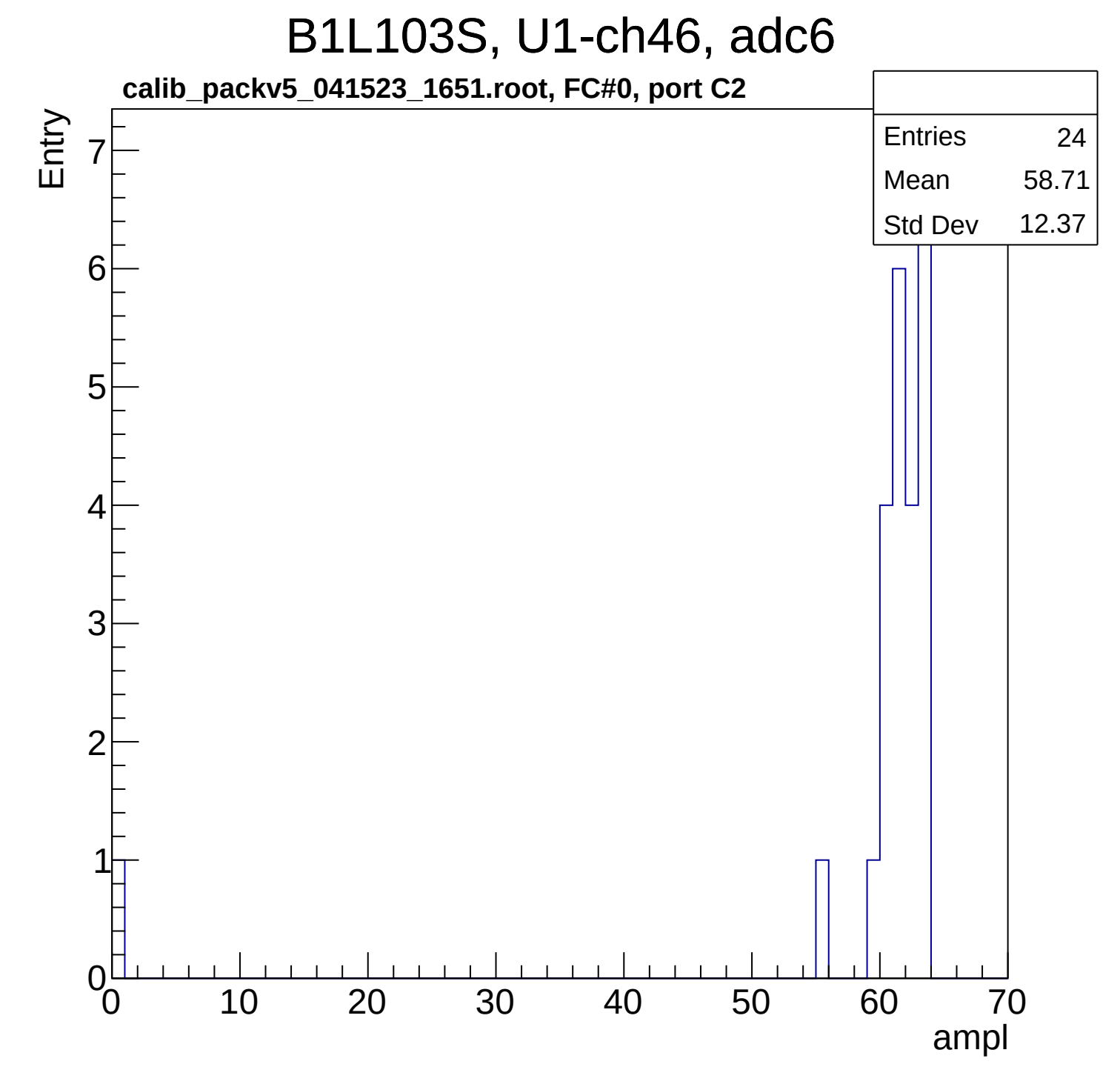
40
50
60
70


B1L103S, U1-ch46, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 24
Mean 58.71
Std Dev 12.37
Entry
ampl
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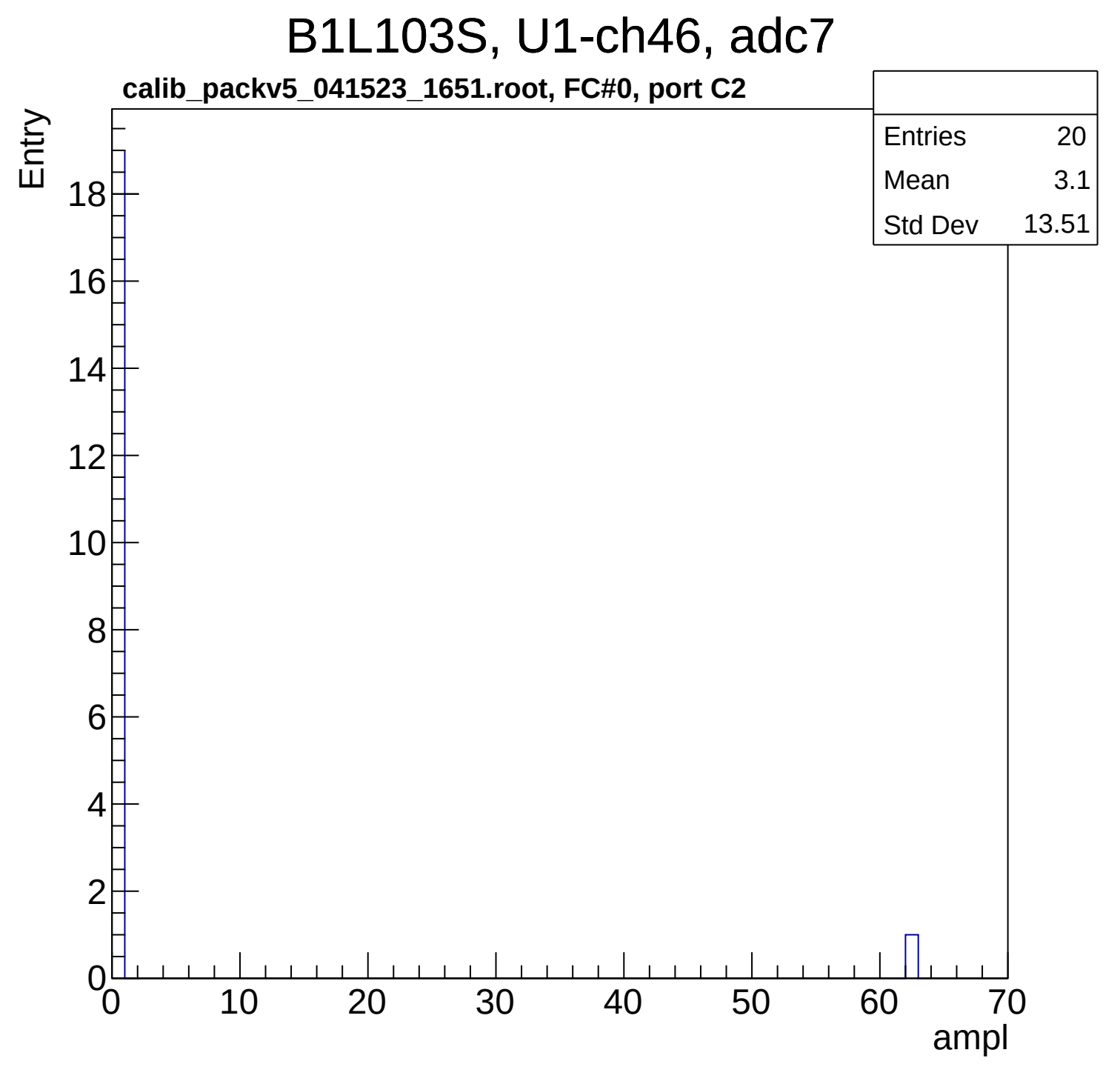
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U1-ch46, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.1
Std Dev 13.51
Entry
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6
8
10
12
14
16
18
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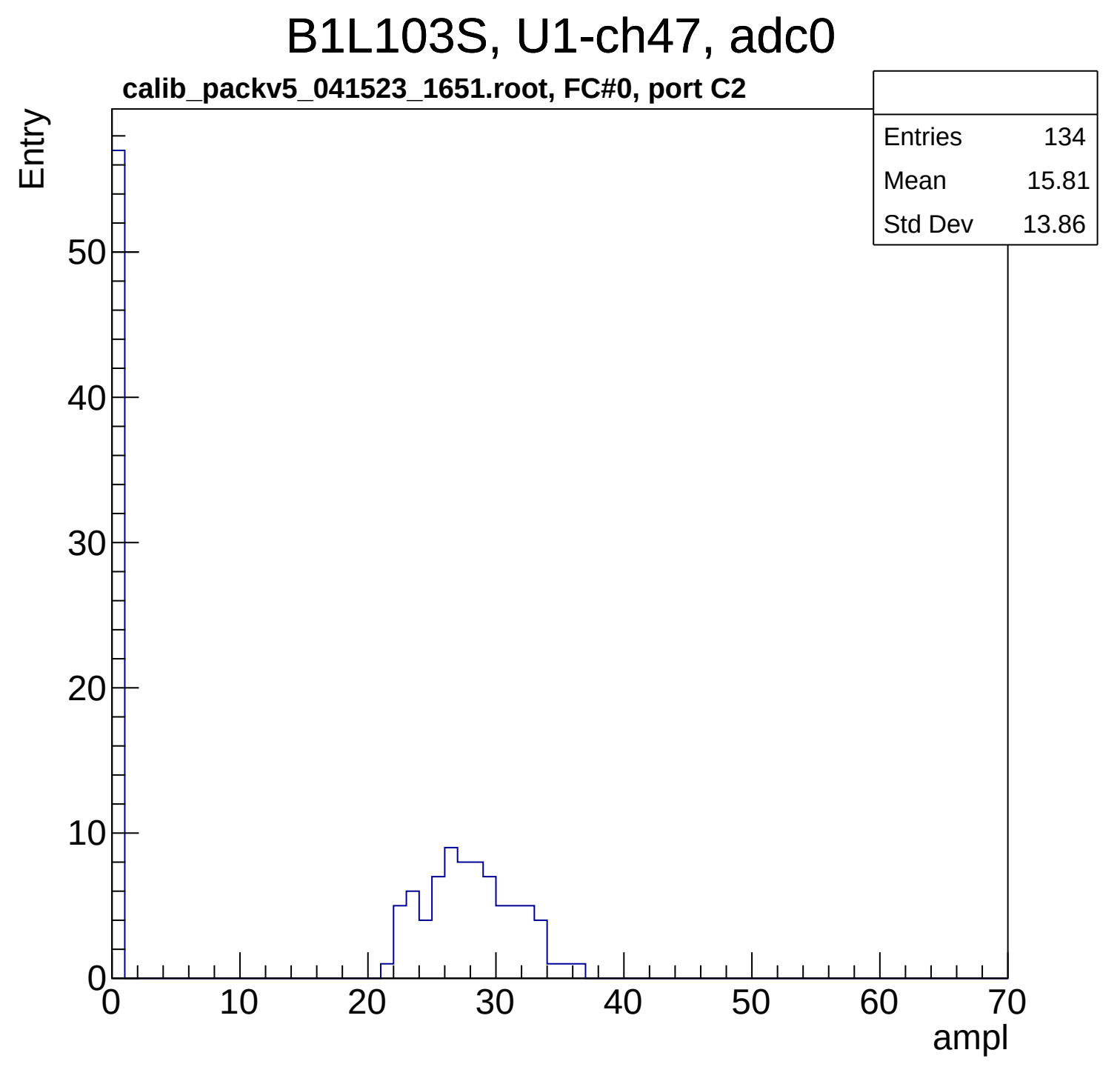
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch47, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 134
Mean 15.81
Std Dev 13.86
Entry
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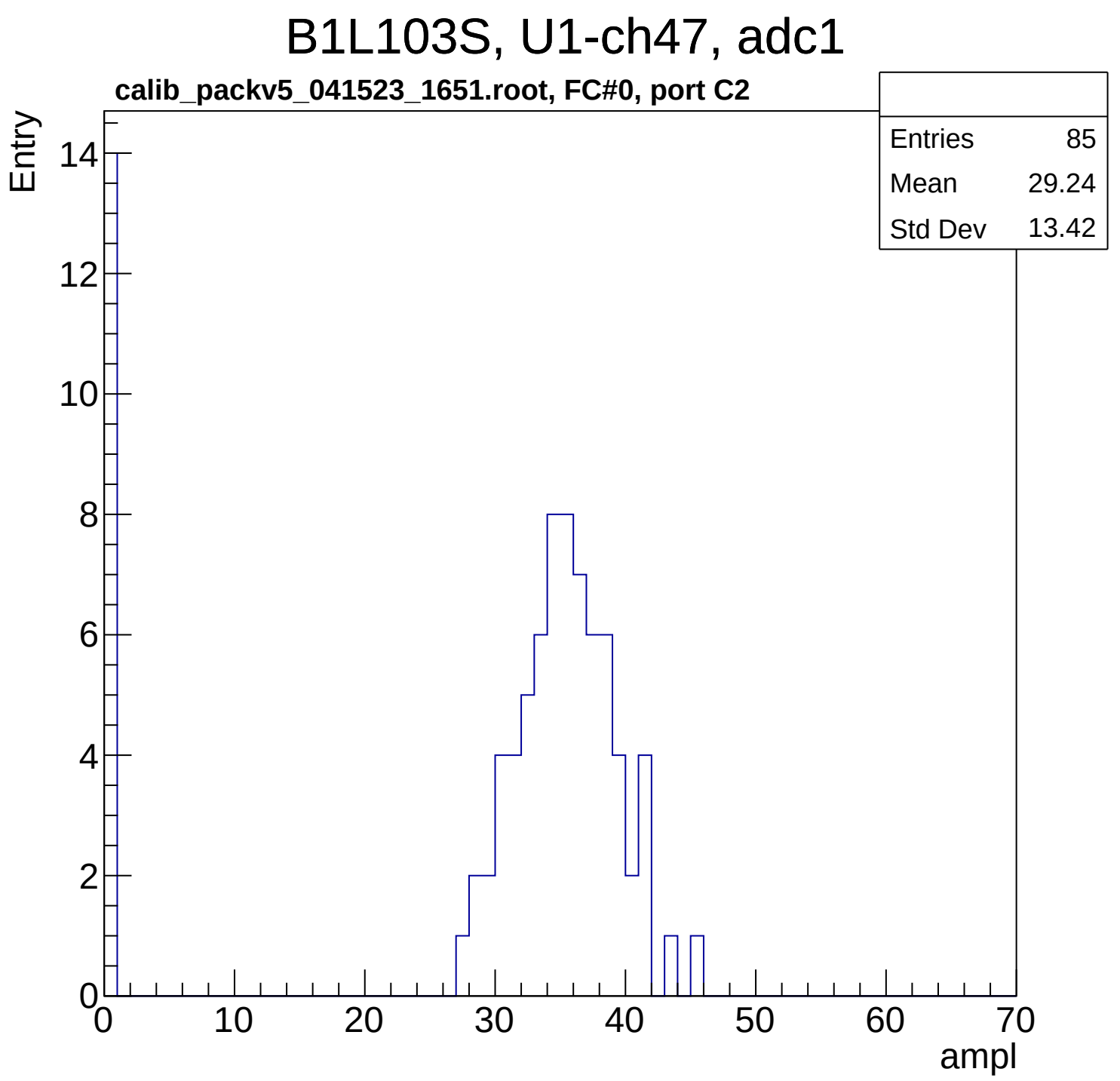
10
20
30
40
50
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch47, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 29.24
Std Dev 13.42
Entry
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4
6
8
10
12
14
0
10
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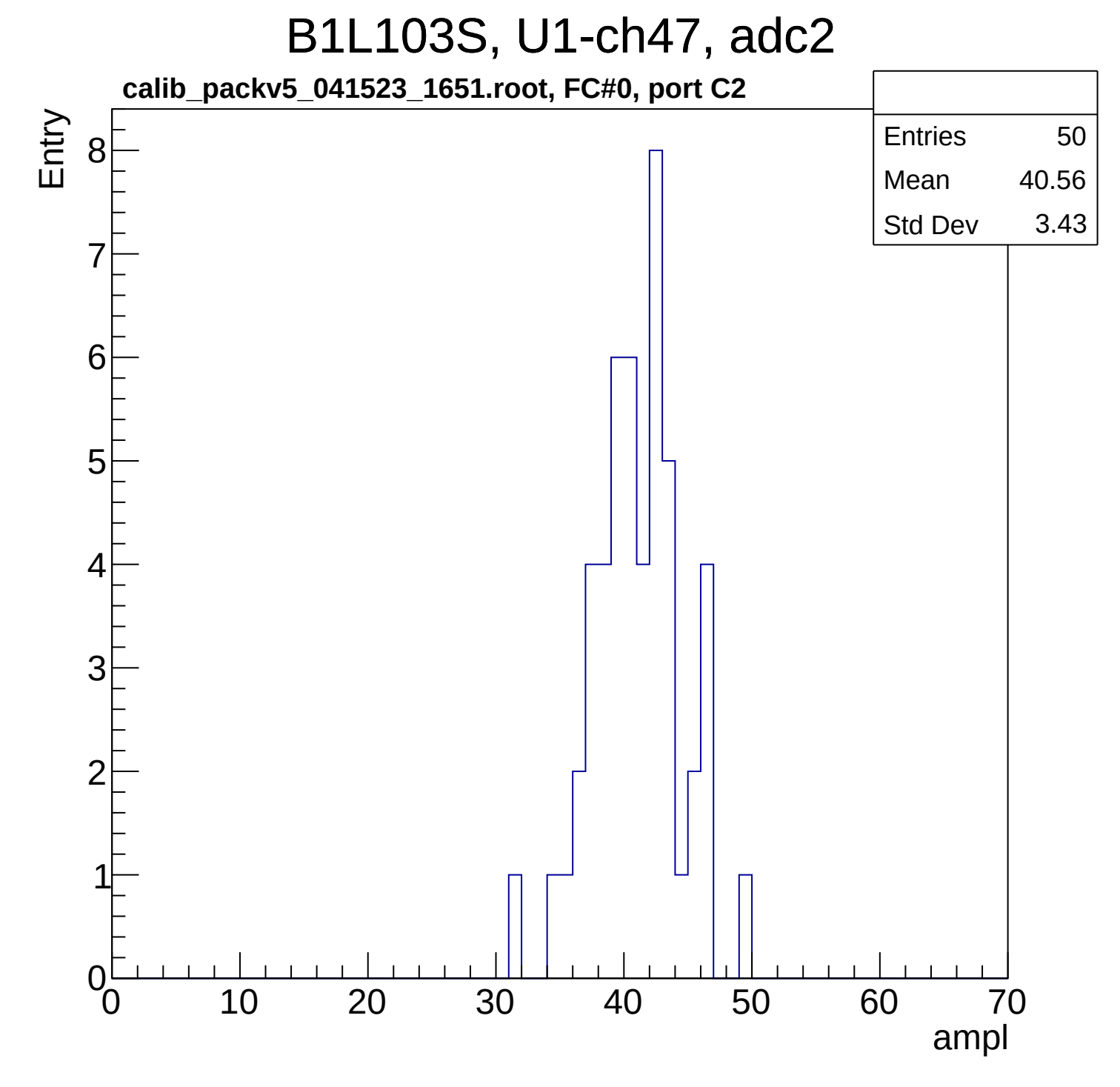
50
60
70
ampl


B1L103S, U1-ch47, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 40.56
Std Dev 3.43
Entry
ampl
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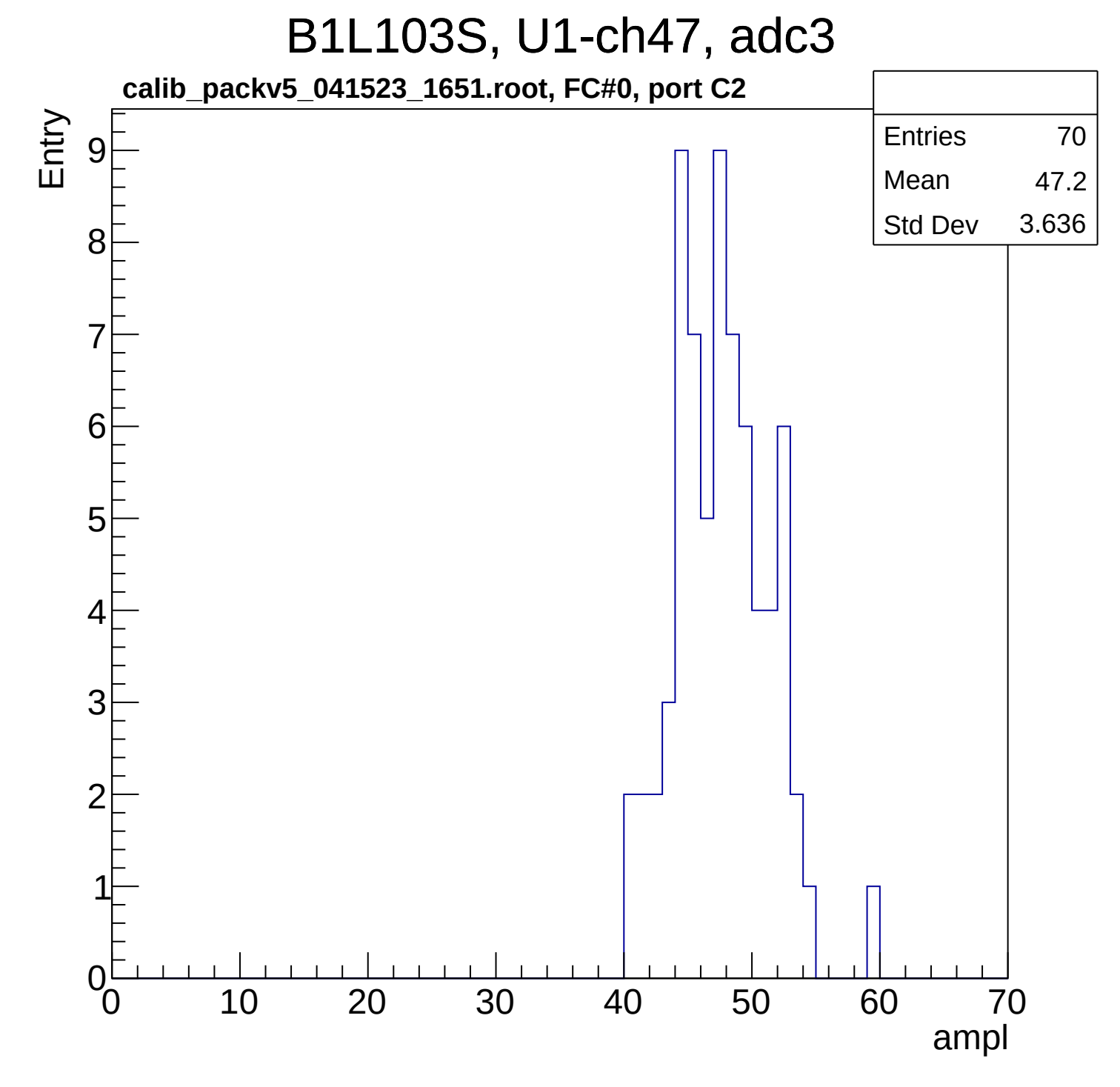
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U1-ch47, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 47.2
Std Dev 3.636
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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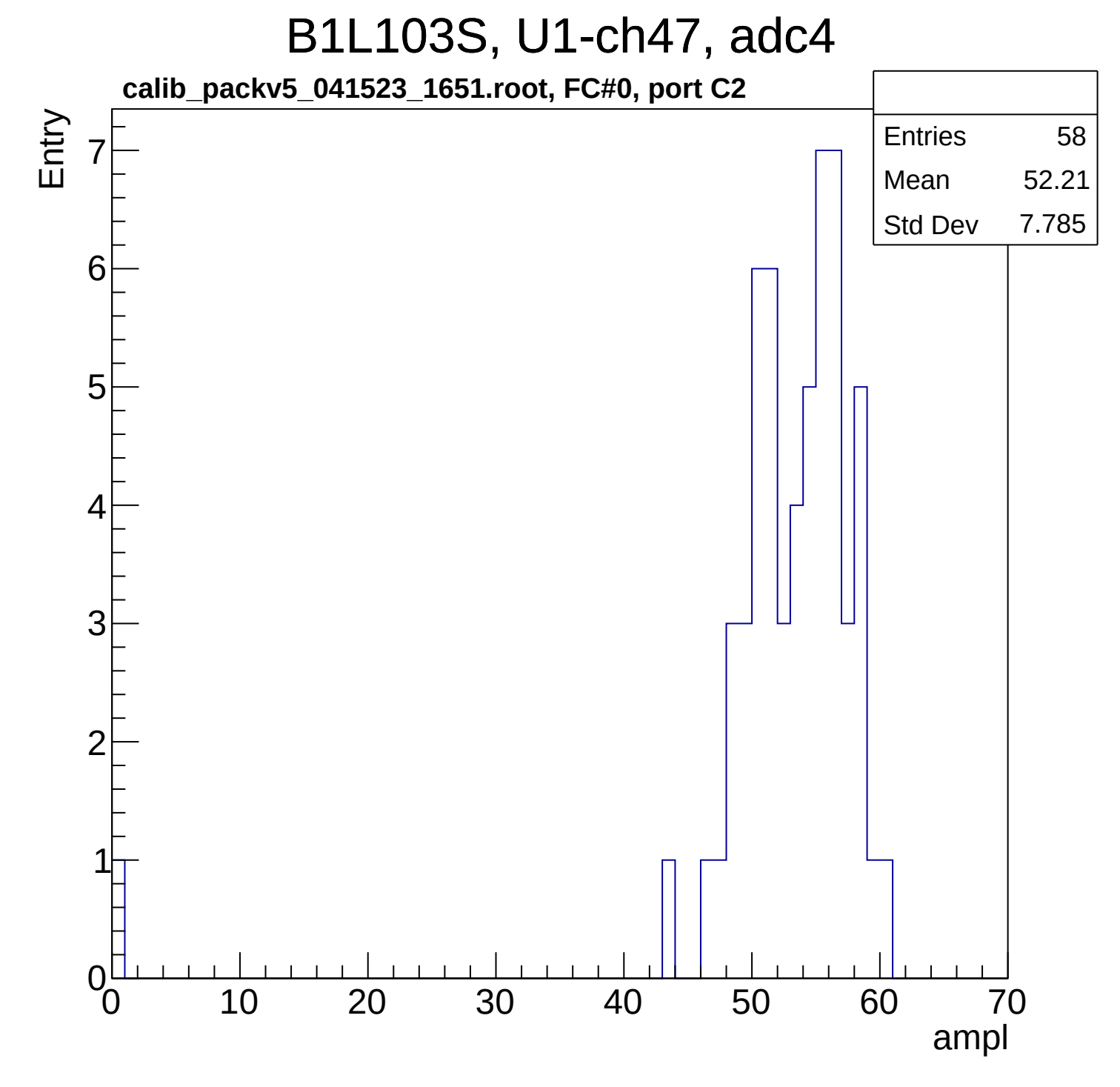
40
50
60
70


B1L103S, U1-ch47, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 52.21
Std Dev 7.785
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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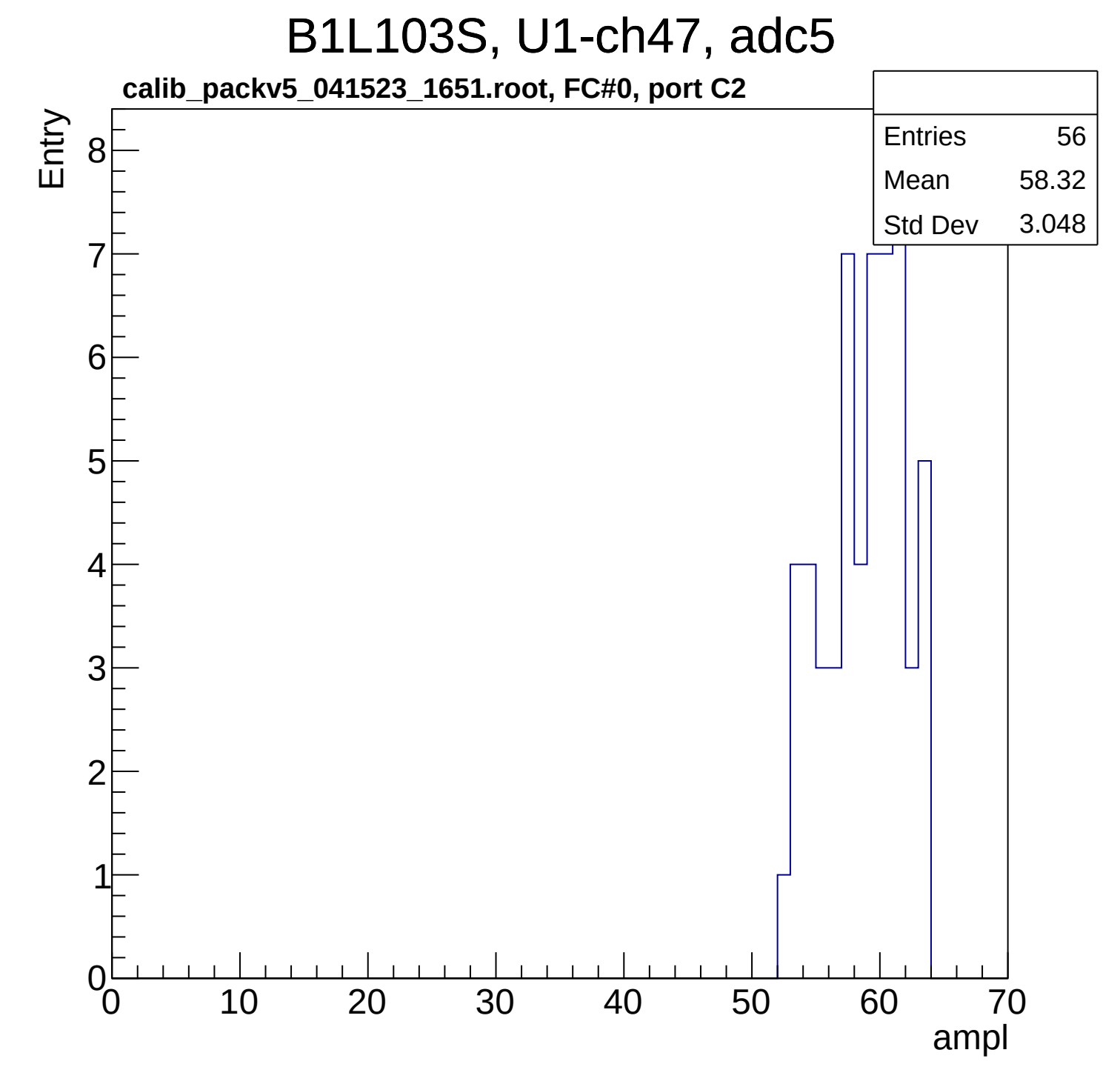
B1L103S, U1-ch47, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 58.32
Std Dev 3.048
Entry
ampl
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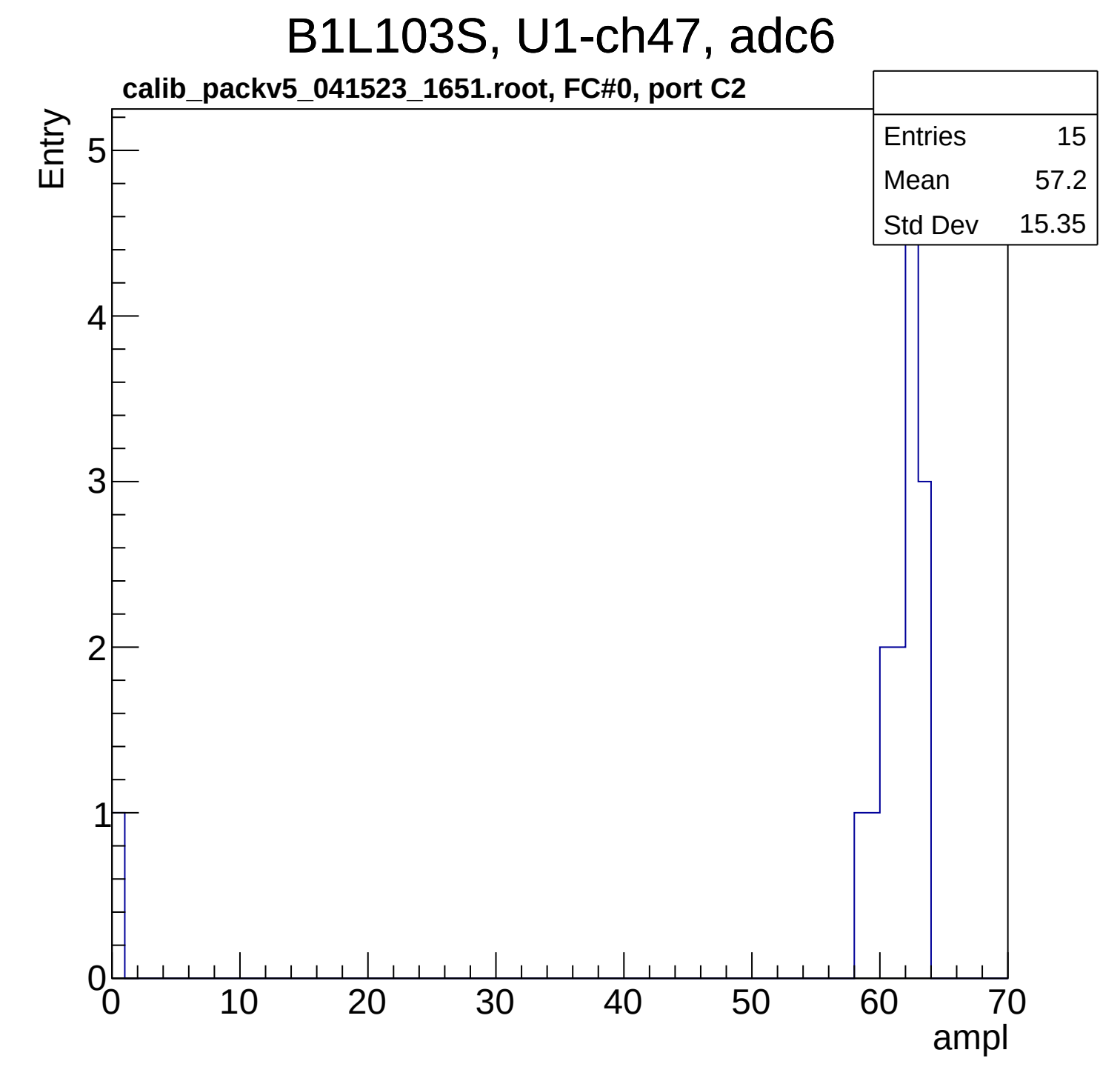
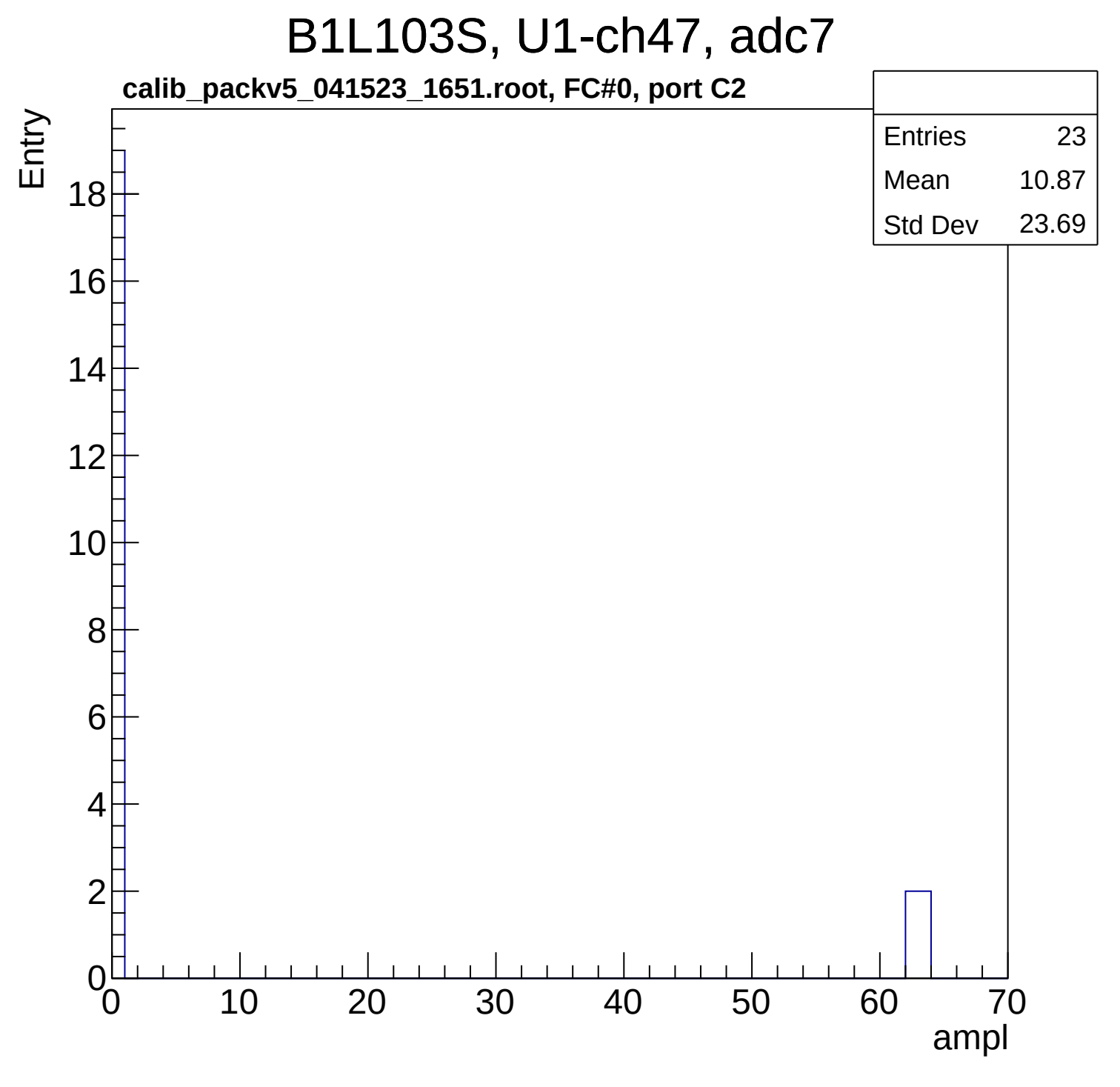
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U1-ch47, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 15
Mean 57.2
Std Dev 15.35
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U1-ch47, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 23
Mean 10.87
Std Dev 23.69
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
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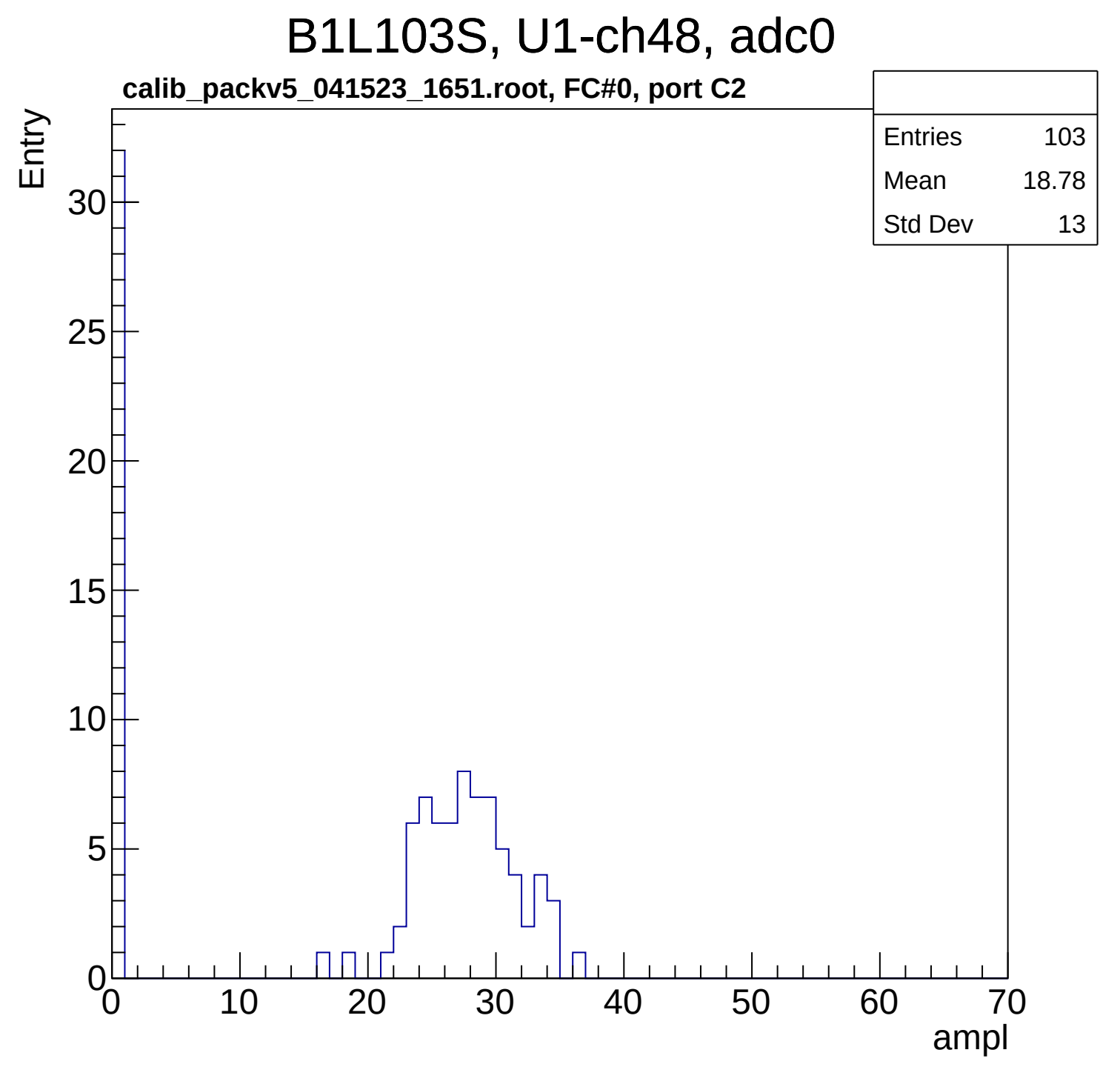
60
70
ampl


B1L103S, U1-ch48, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 103
Mean 18.78
Std Dev 13
Entry
0
5
10
15
20
25
30
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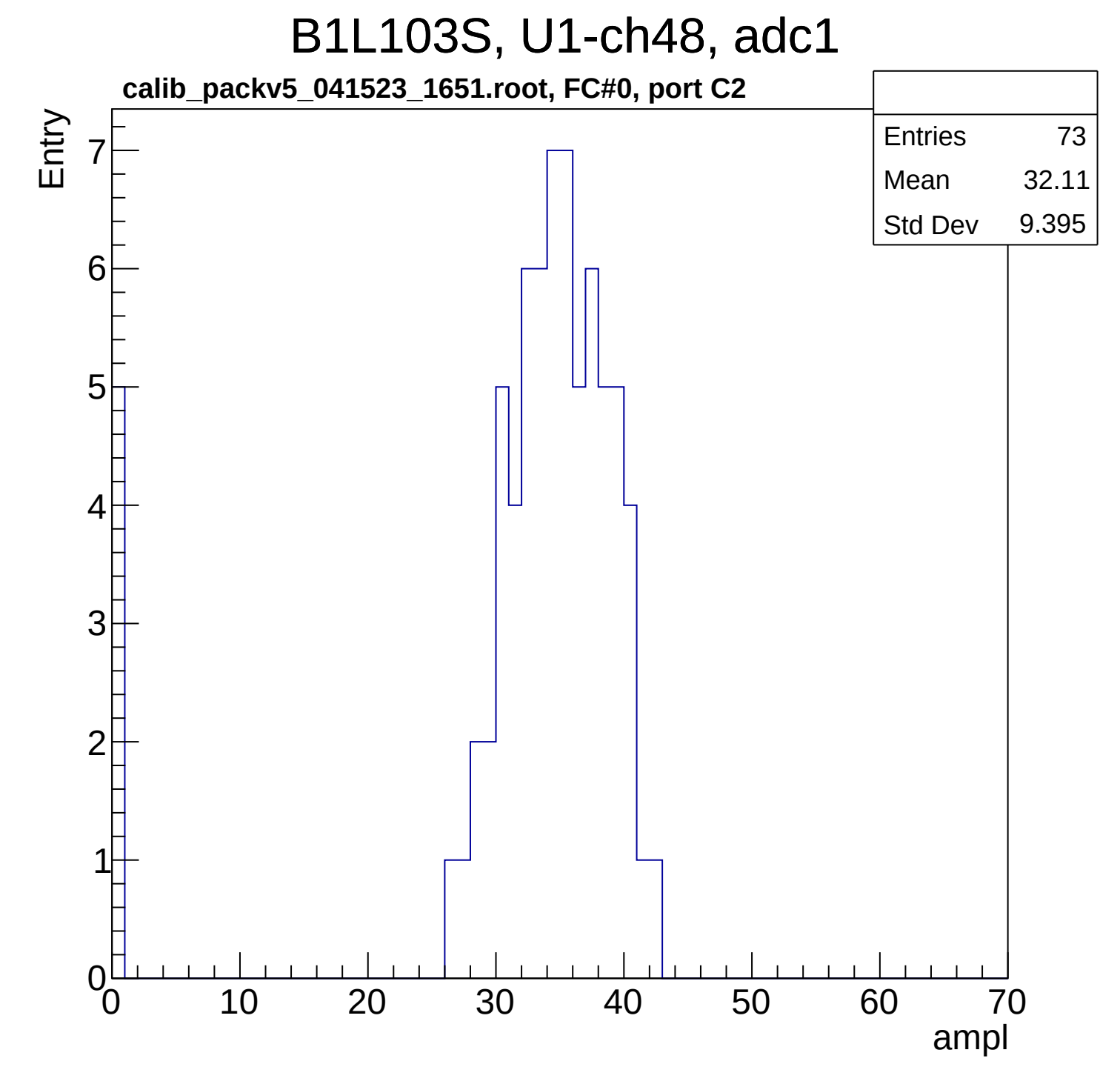
ampl


B1L103S, U1-ch48, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 32.11
Std Dev 9.395
Entry
ampl
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1
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4
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6
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0
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40
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60
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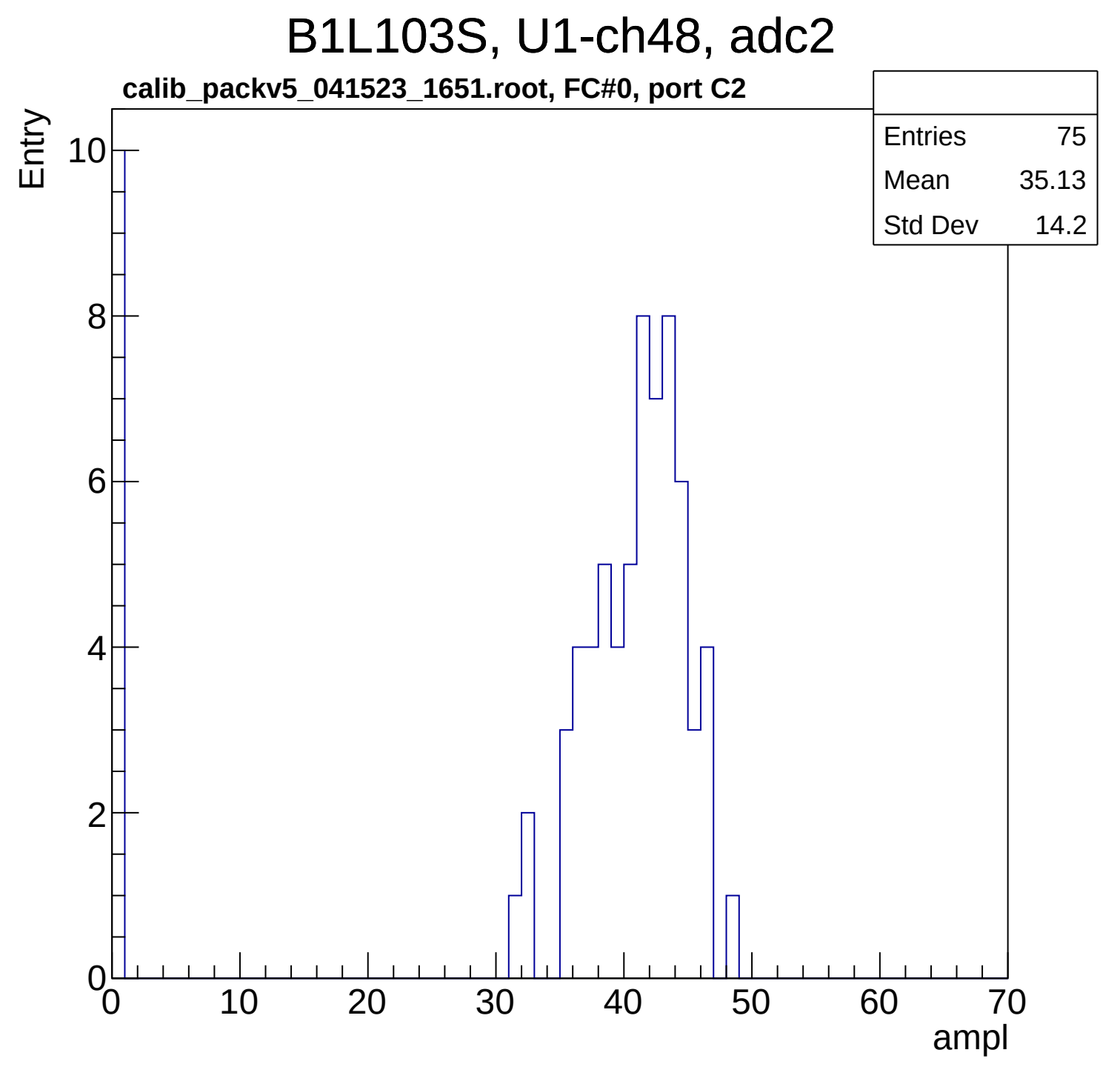
B1L103S, U1-ch48, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 35.13
Std Dev 14.2
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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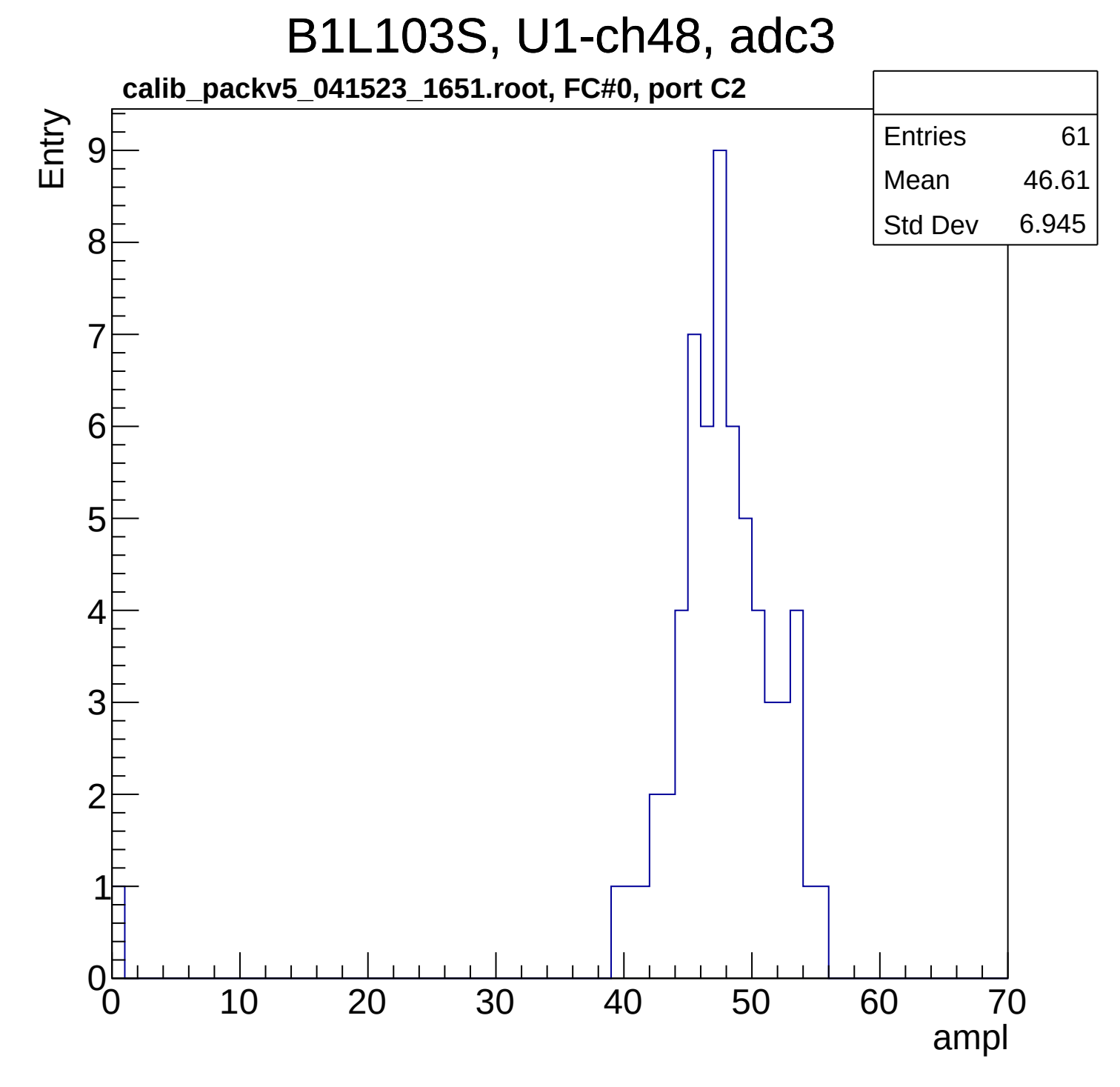
B1L103S, U1-ch48, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 46.61
Std Dev 6.945
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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60
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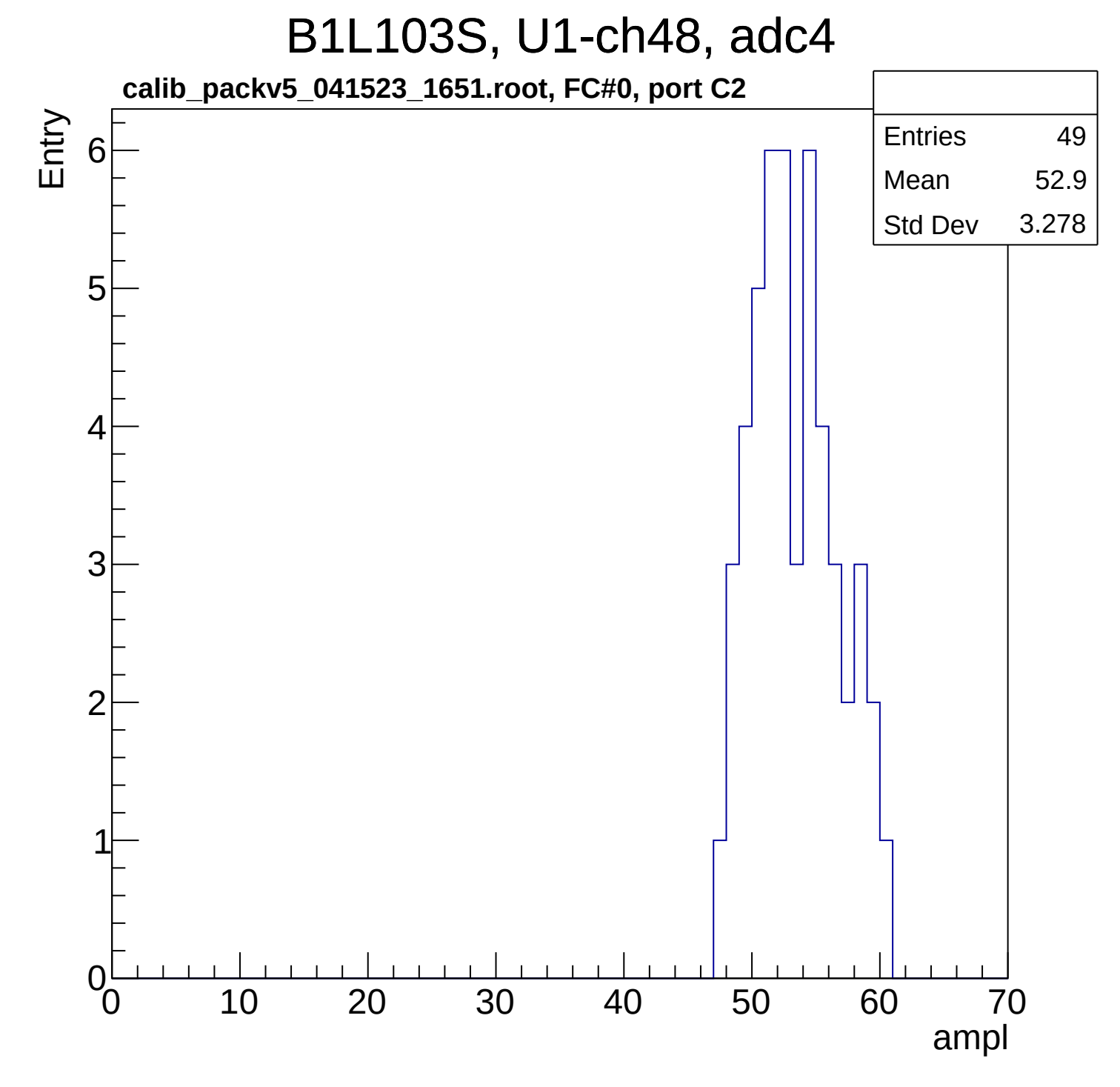
B1L103S, U1-ch48, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 52.9
Std Dev 3.278
Entry
ampl
0
1
2
3
4
5
6
0
10
20
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40
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60
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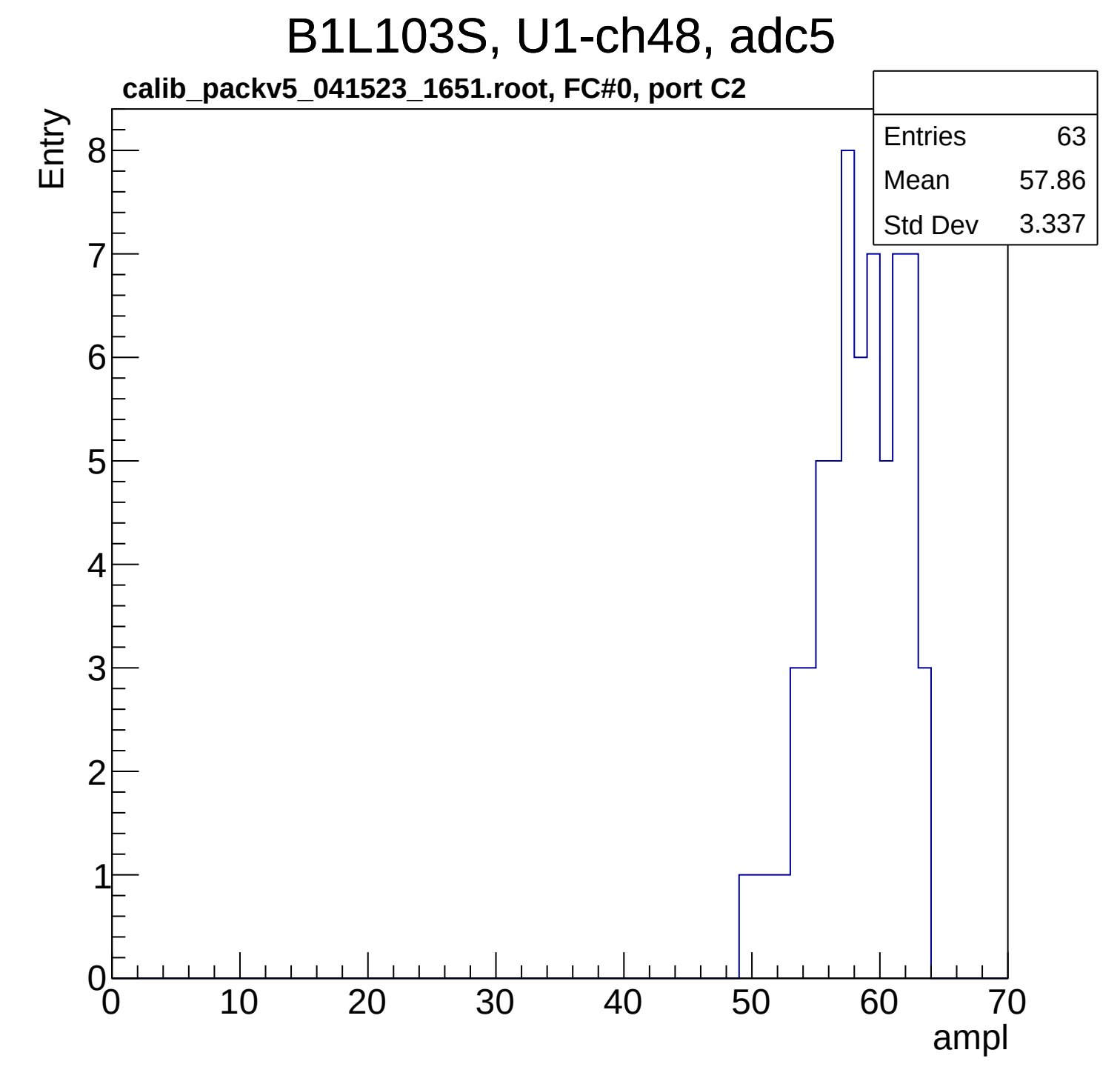
B1L103S, U1-ch48, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 57.86
Std Dev 3.337
Entry
ampl
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3
4
5
6
7
8
0
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60
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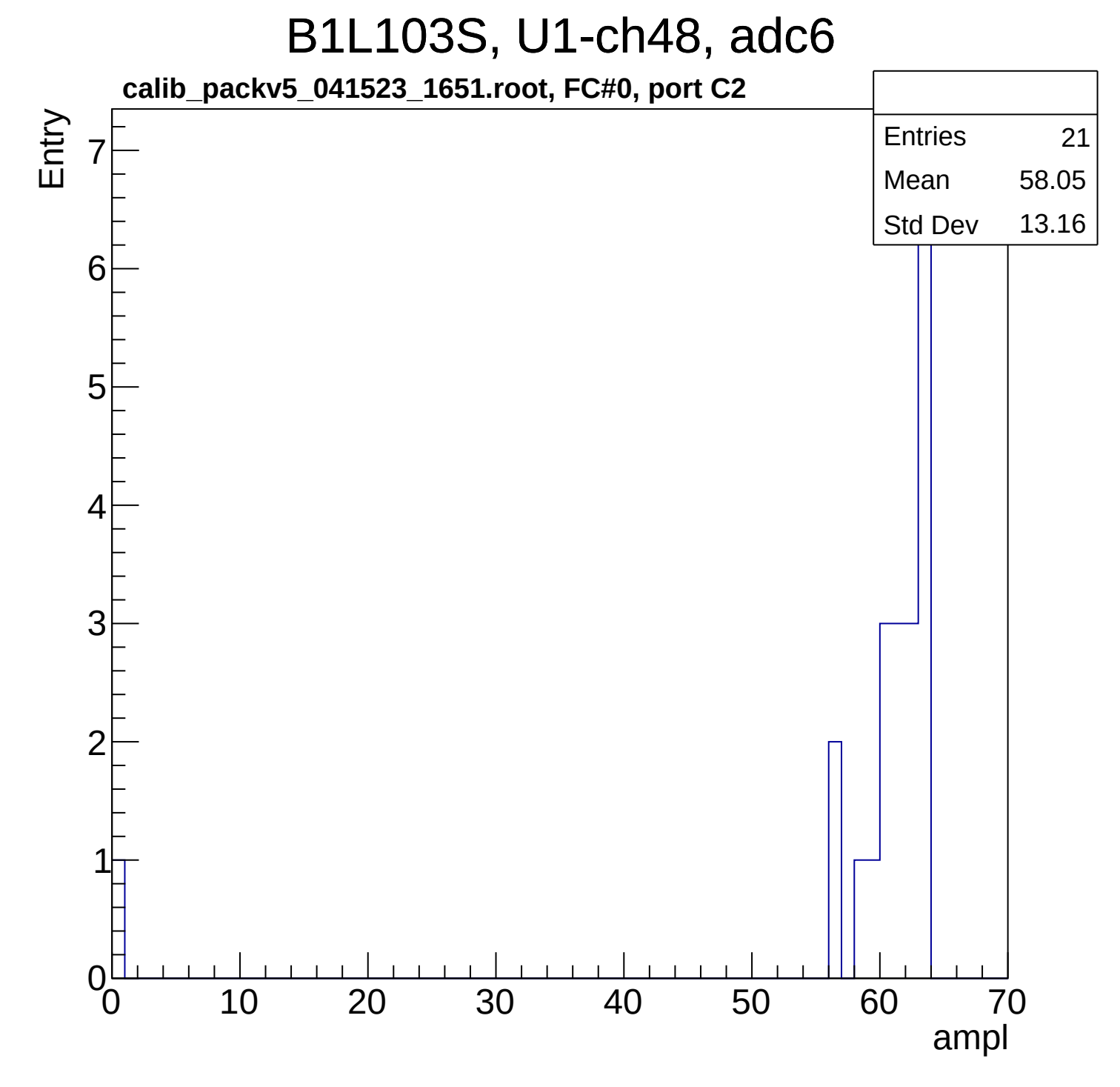
B1L103S, U1-ch48, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 58.05
Std Dev 13.16
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
30
40
50
60
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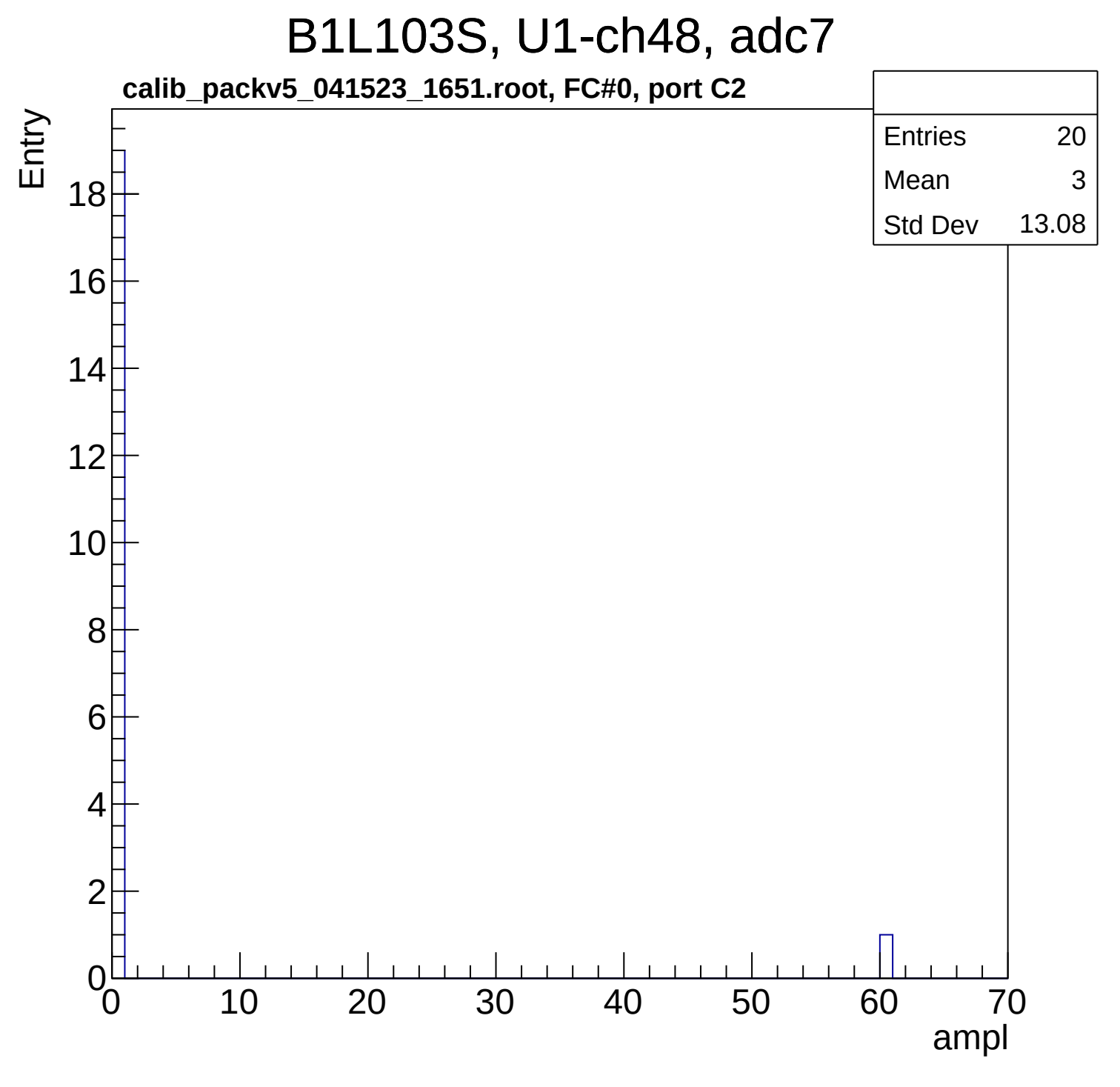
B1L103S, U1-ch48, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3
Std Dev 13.08
Entry
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6
8
10
12
14
16
18
0
10
20
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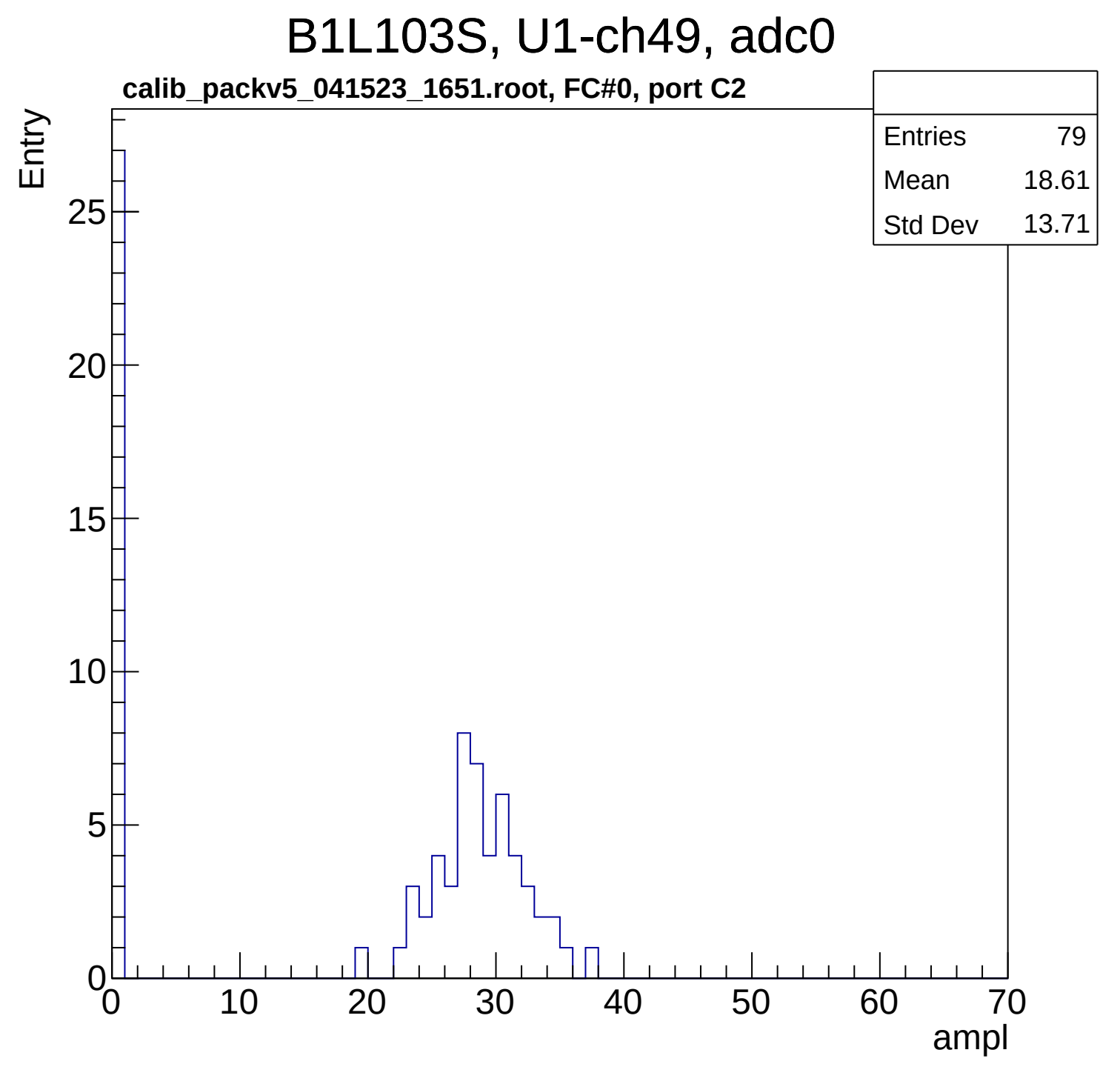
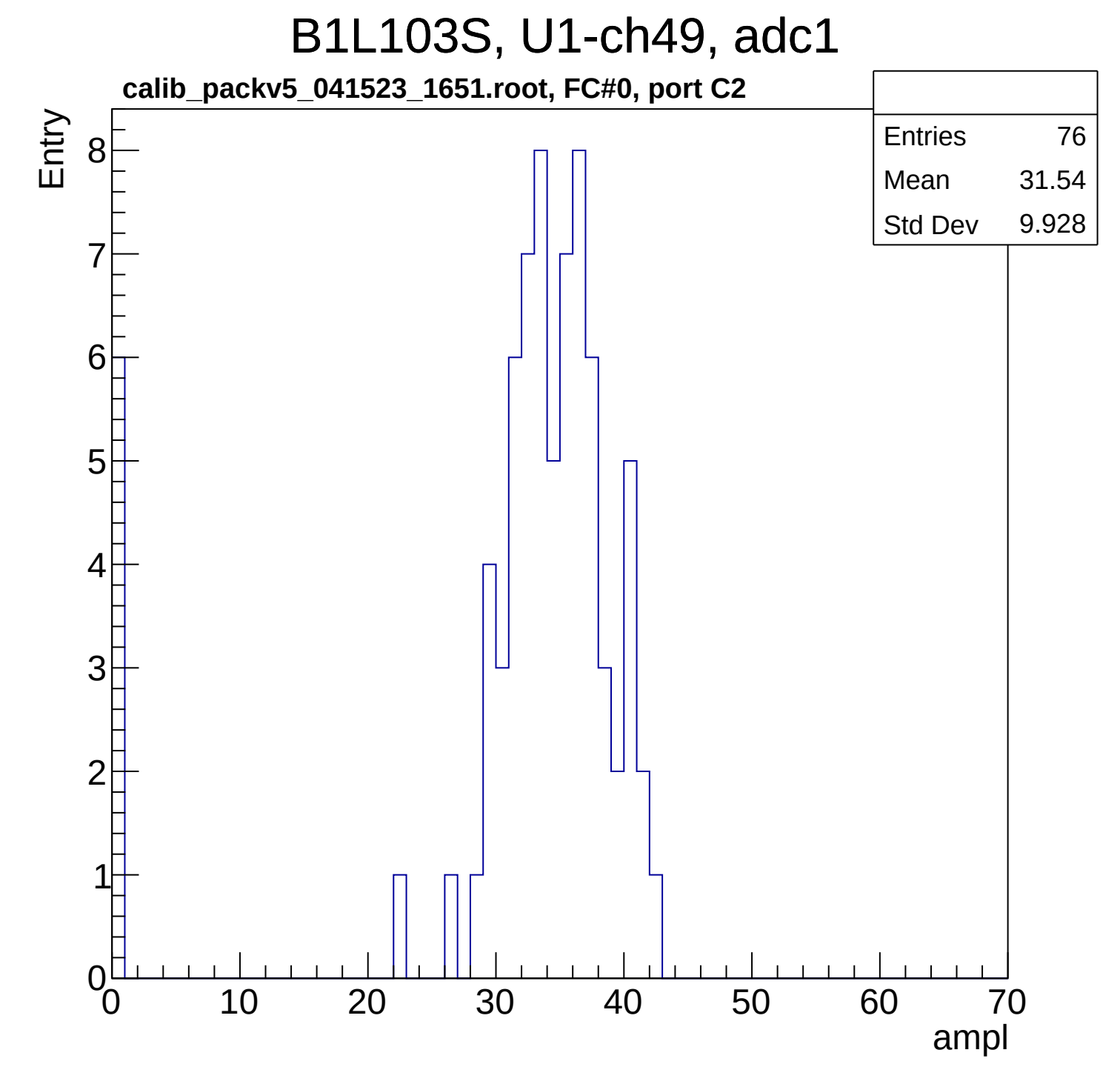
50
60
70
ampl


B1L103S, U1-ch49, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 18.61
Std Dev 13.71
Entry
0
5
10
15
20
25
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch49, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 31.54
Std Dev 9.928
Entry
ampl
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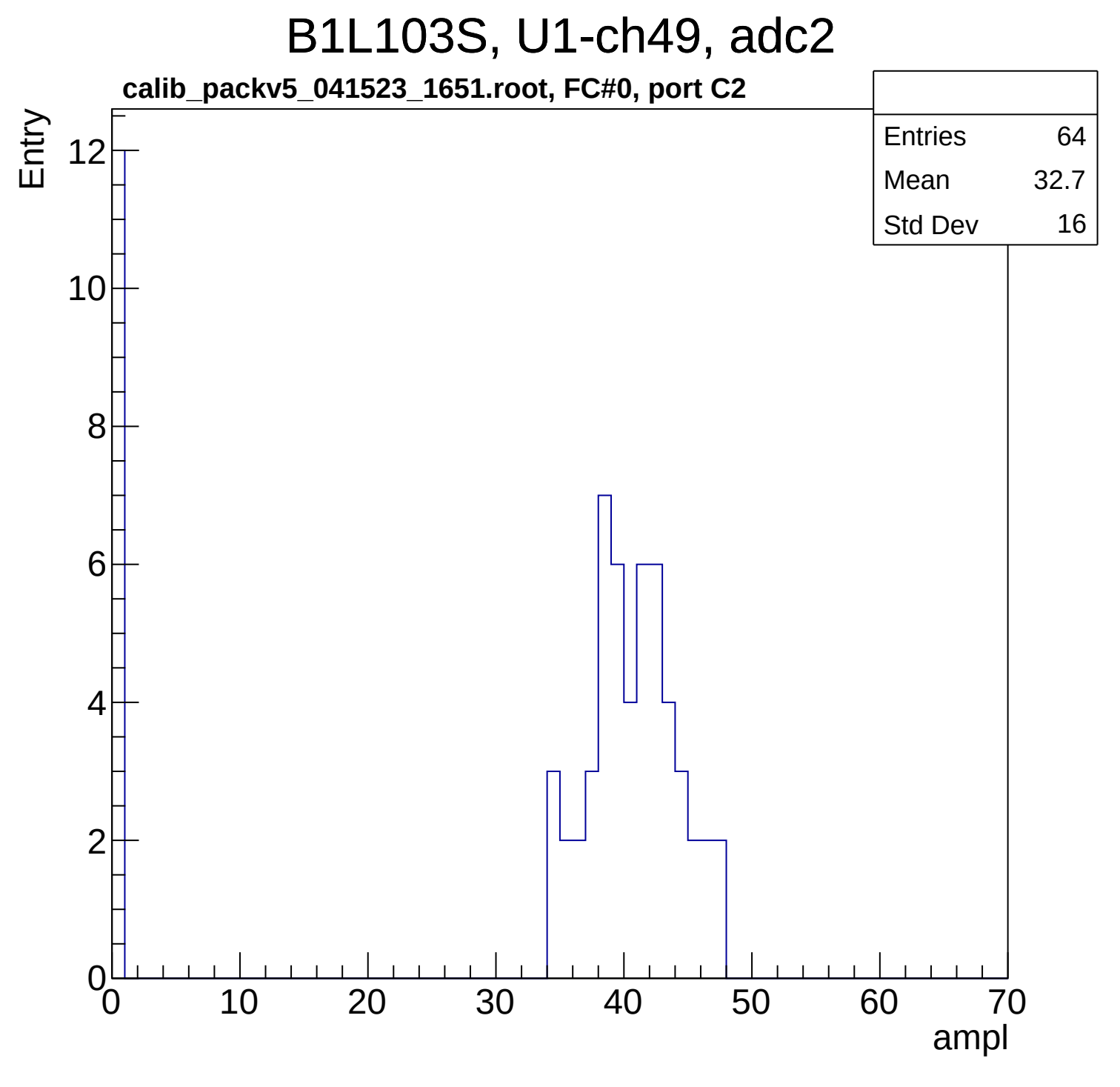
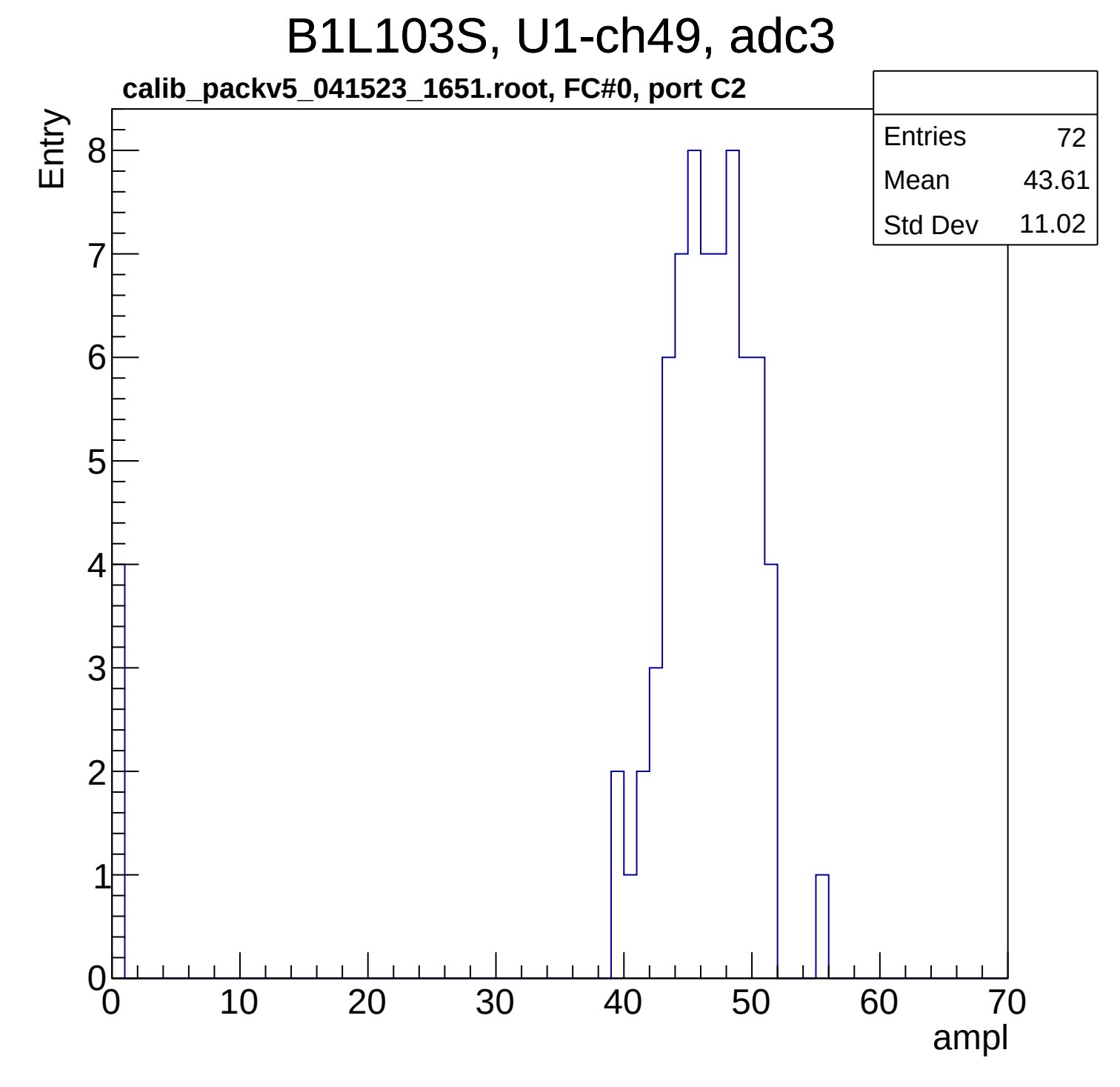
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U1-ch49, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 32.7
Std Dev 16
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch49, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 43.61
Std Dev 11.02
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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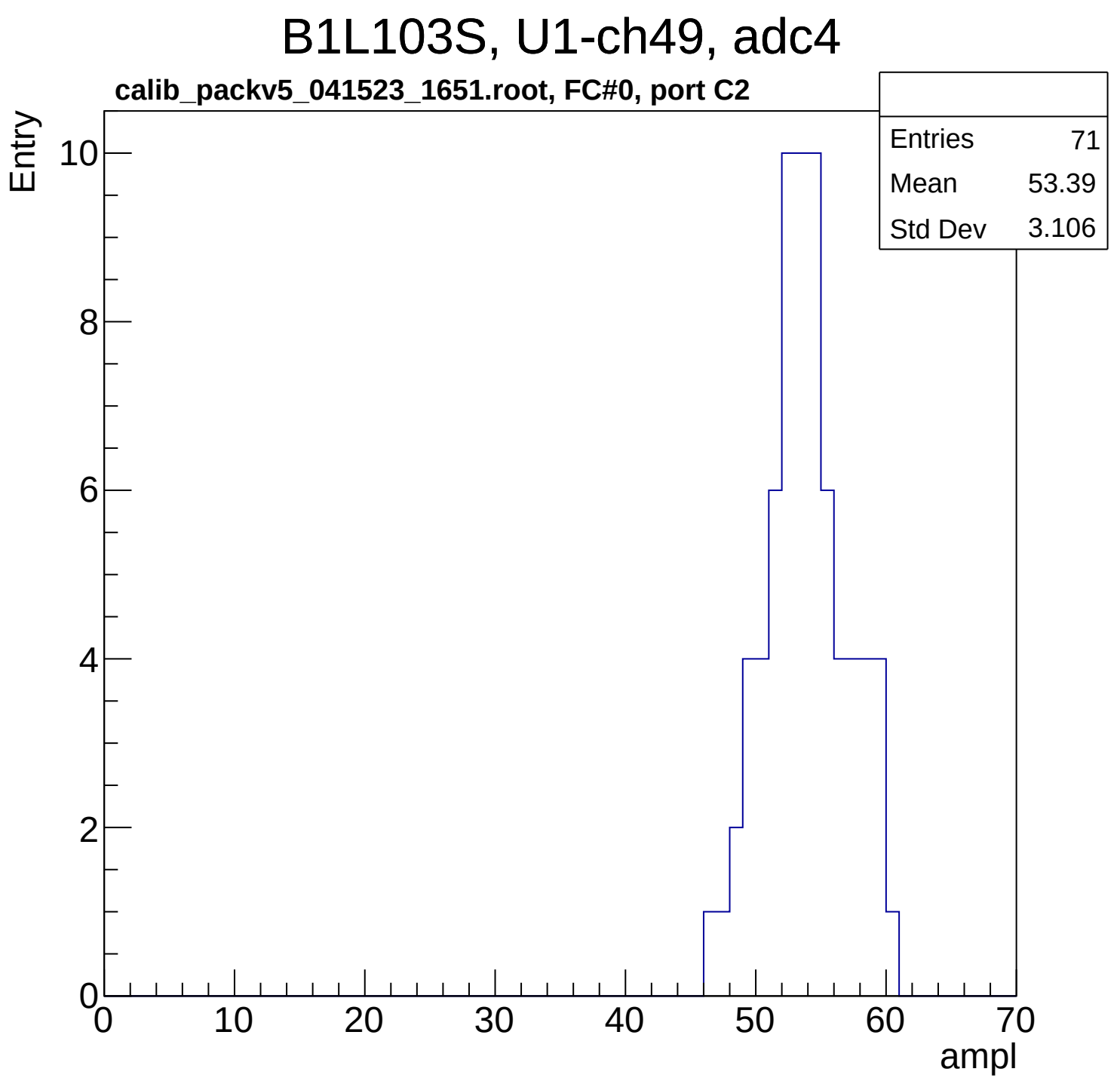
B1L103S, U1-ch49, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 53.39
Std Dev 3.106
Entry
ampl
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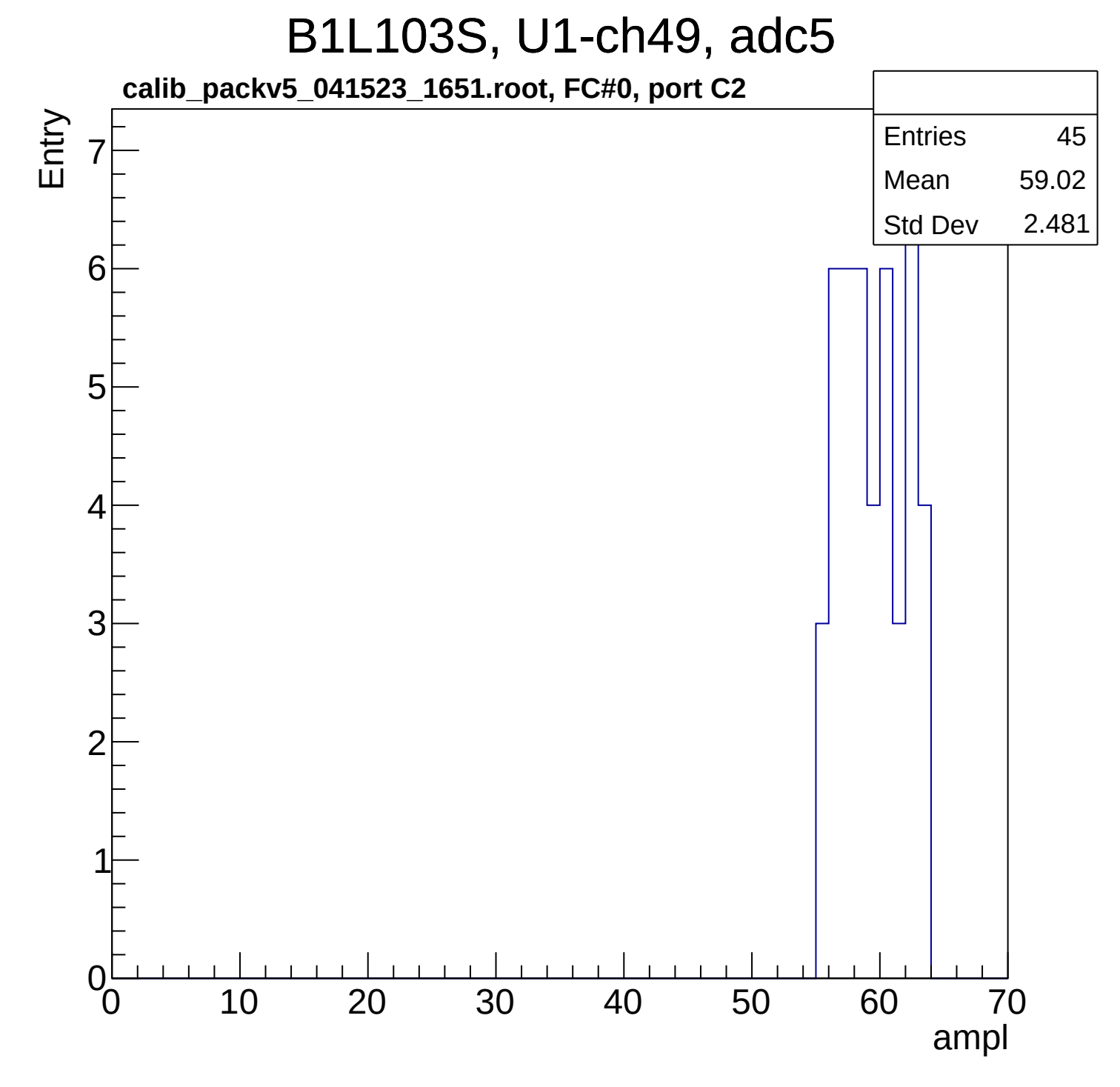
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U1-ch49, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 59.02
Std Dev 2.481
Entry
ampl
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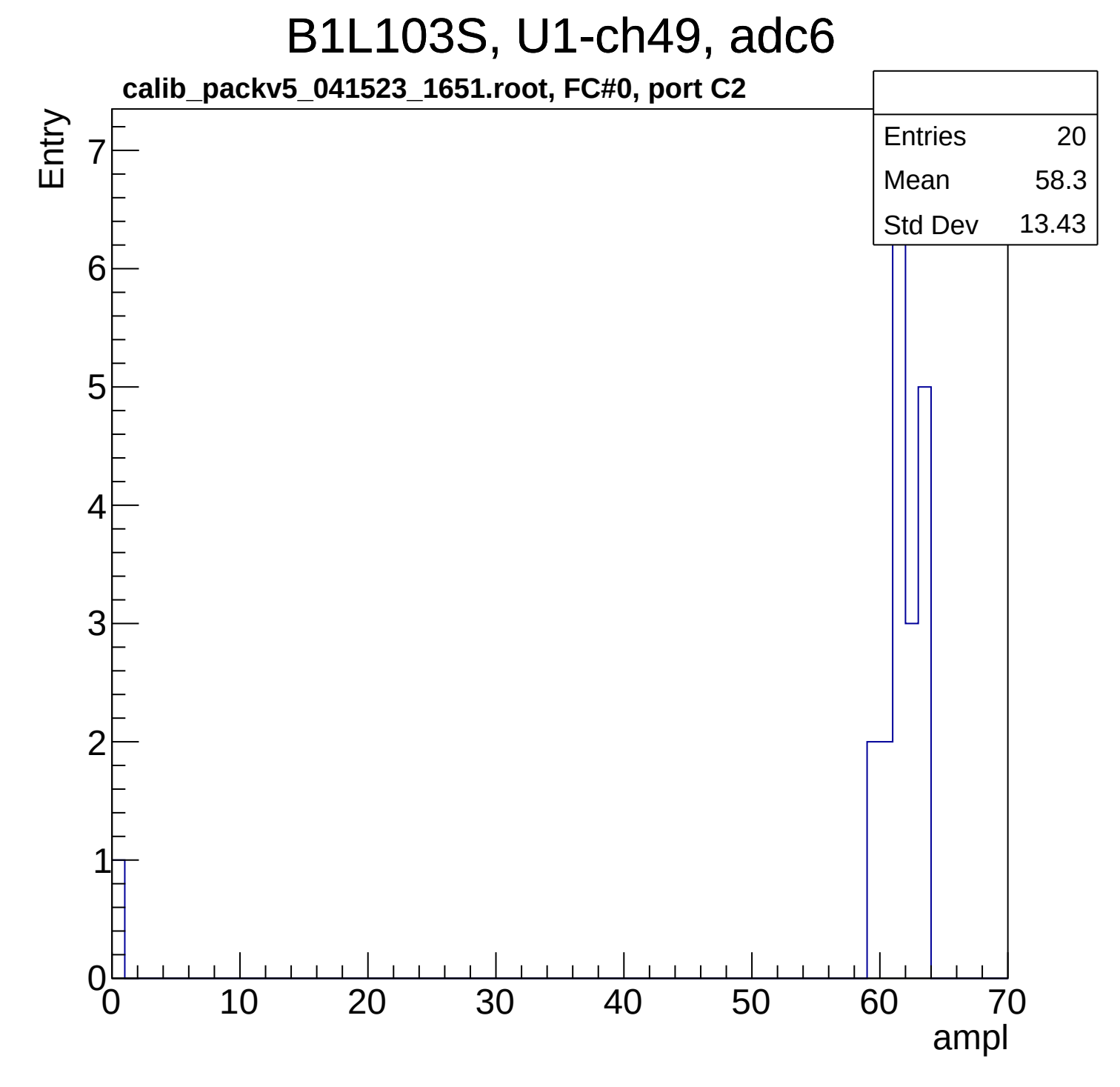
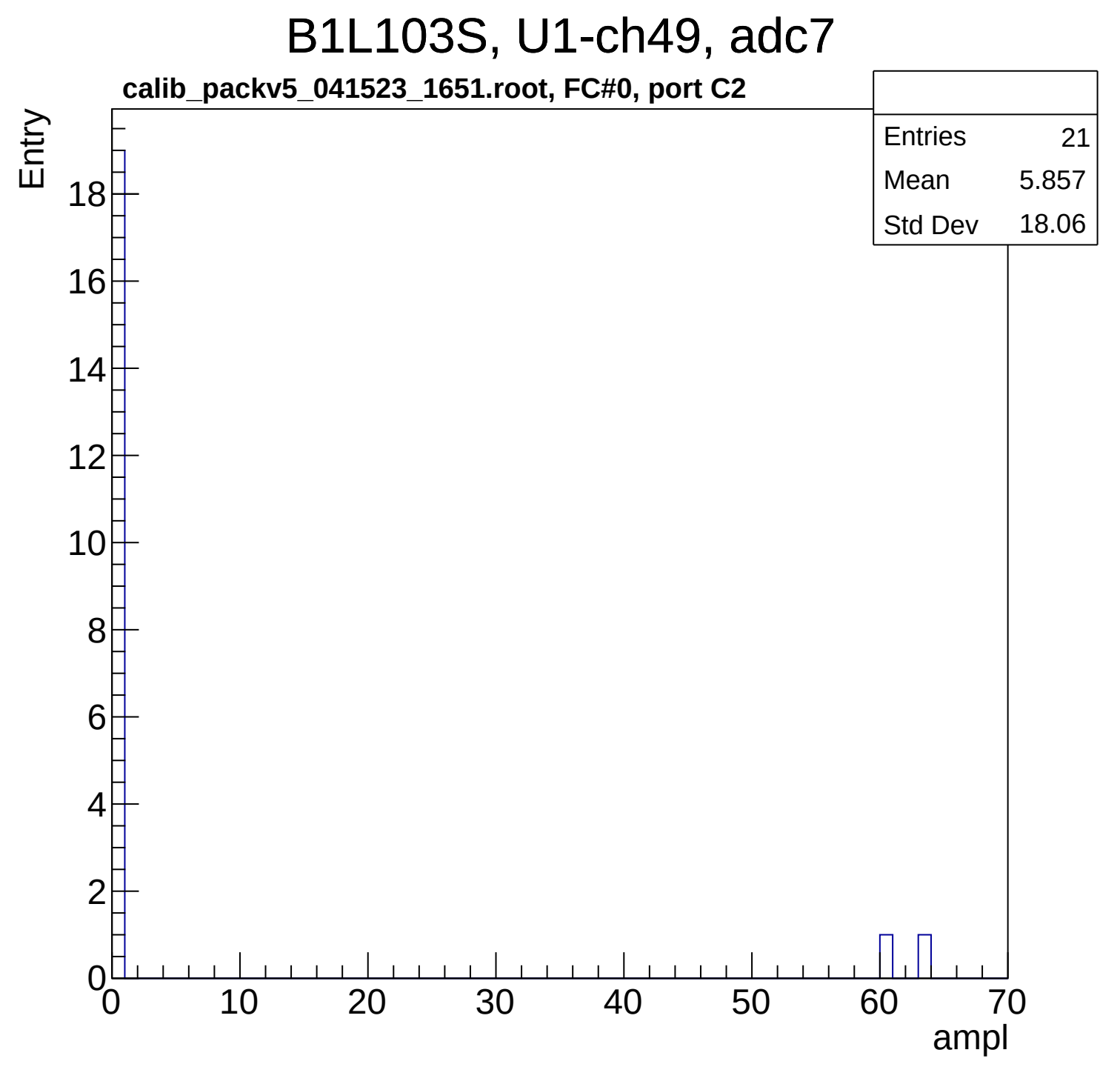
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U1-ch49, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 58.3
Std Dev 13.43
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U1-ch49, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 5.857
Std Dev 18.06
Entry
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6
8
10
12
14
16
18
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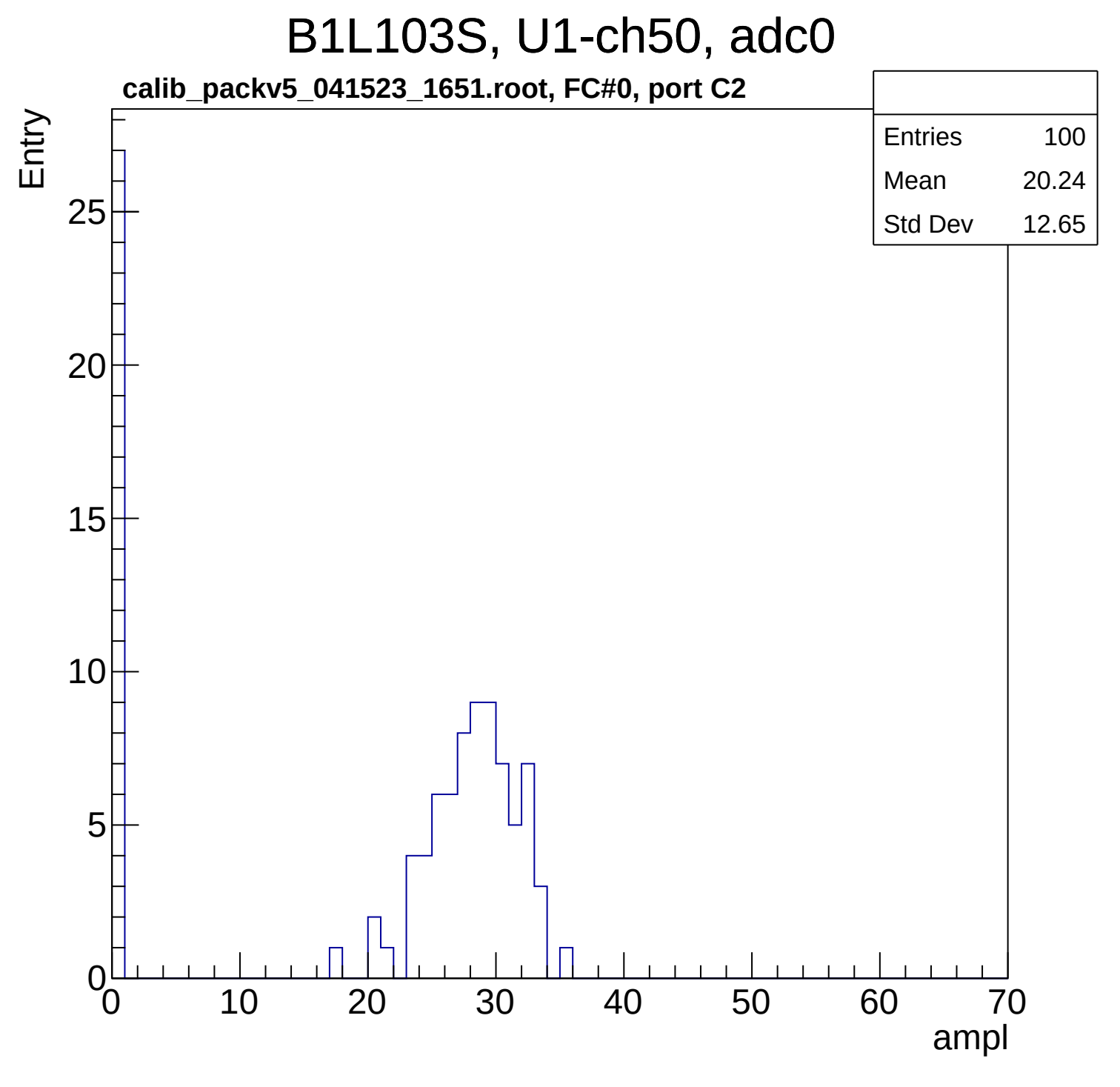
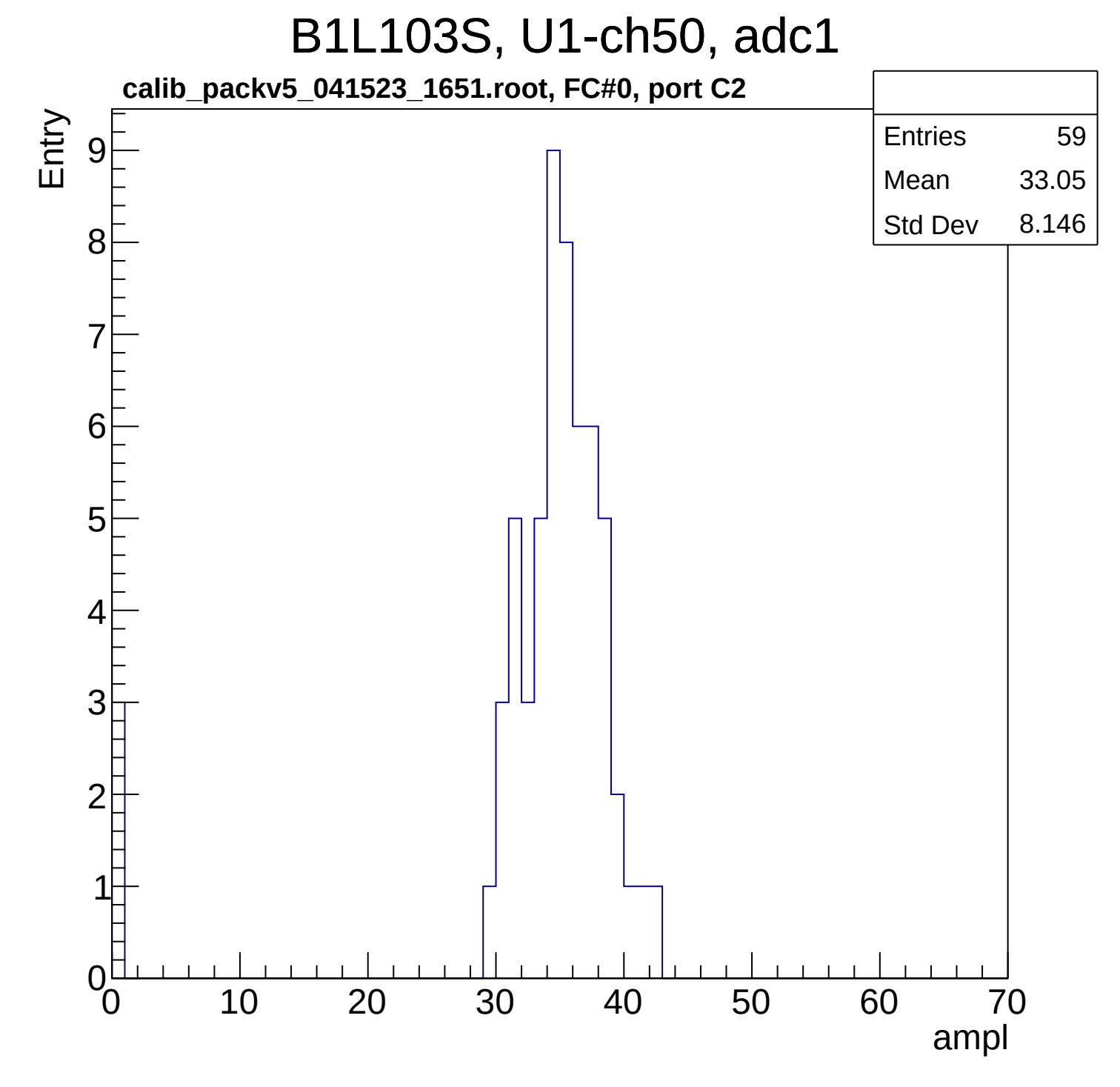
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch50, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 100
Mean 20.24
Std Dev 12.65
Entry
0
5
10
15
20
25
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch50, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 33.05
Std Dev 8.146
Entry
ampl
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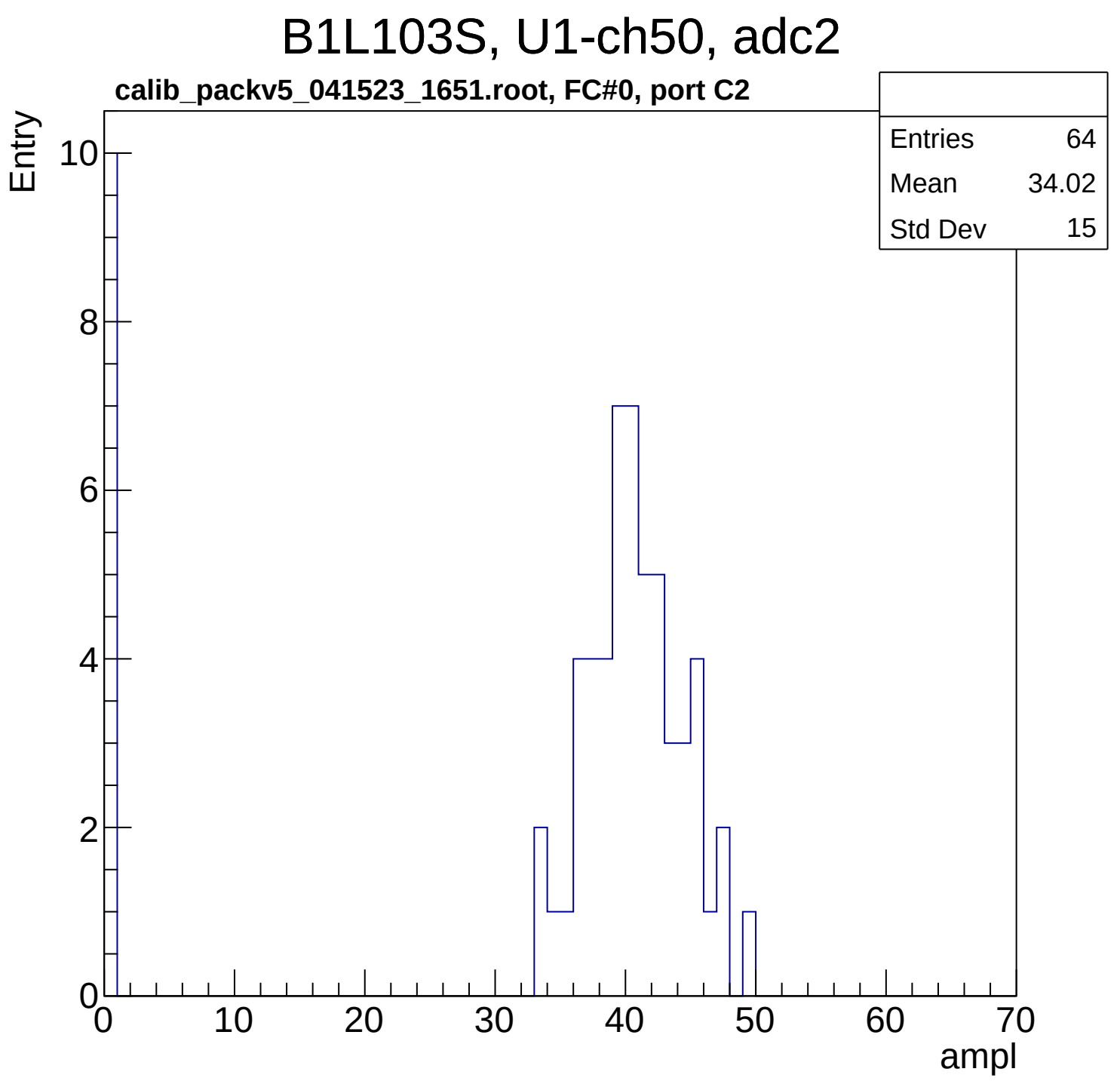
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U1-ch50, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 34.02
Std Dev 15
Entry
ampl
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0
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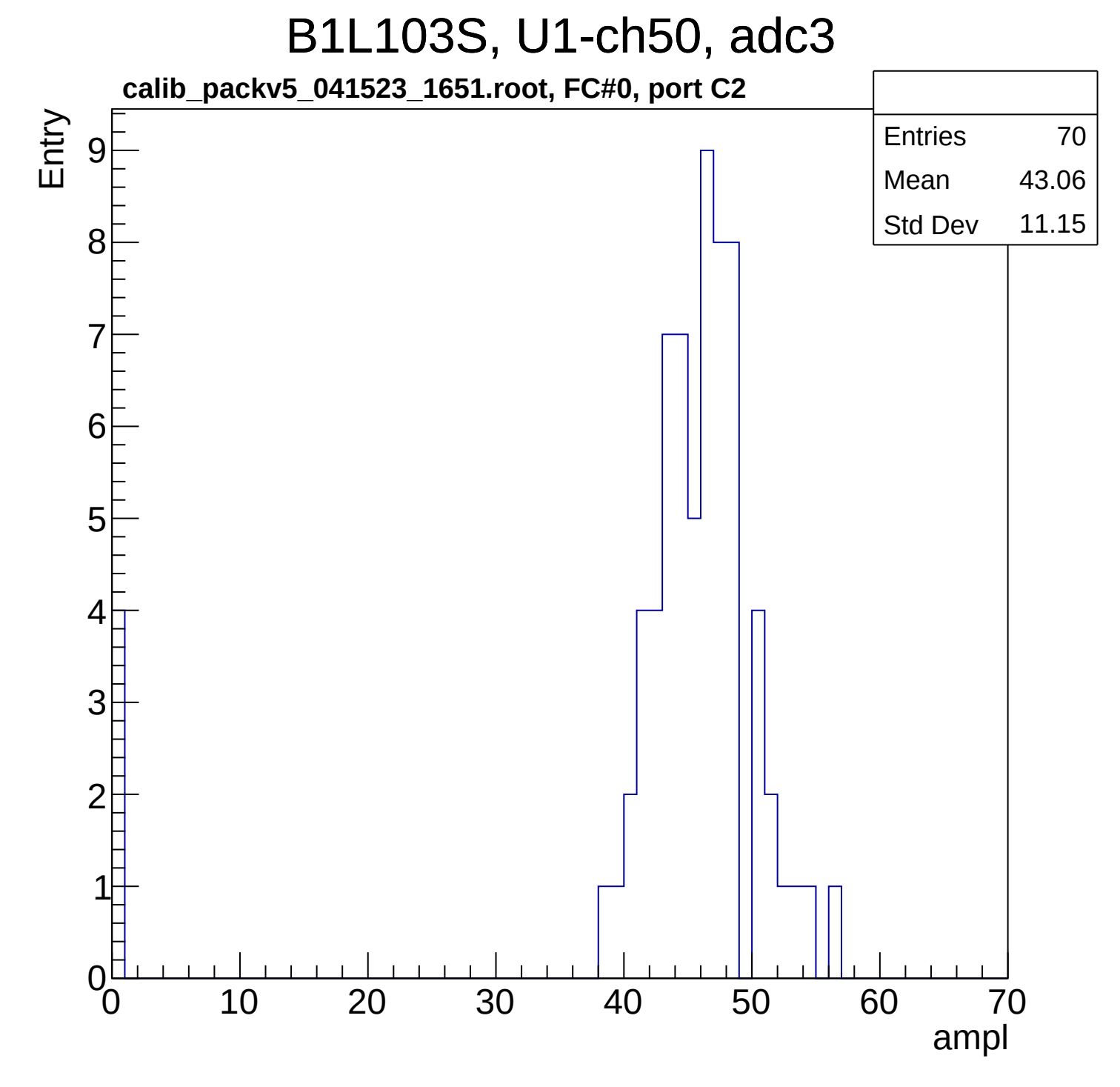
B1L103S, U1-ch50, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 43.06
Std Dev 11.15
Entry
ampl
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2
3
4
5
6
7
8
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0
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20
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60
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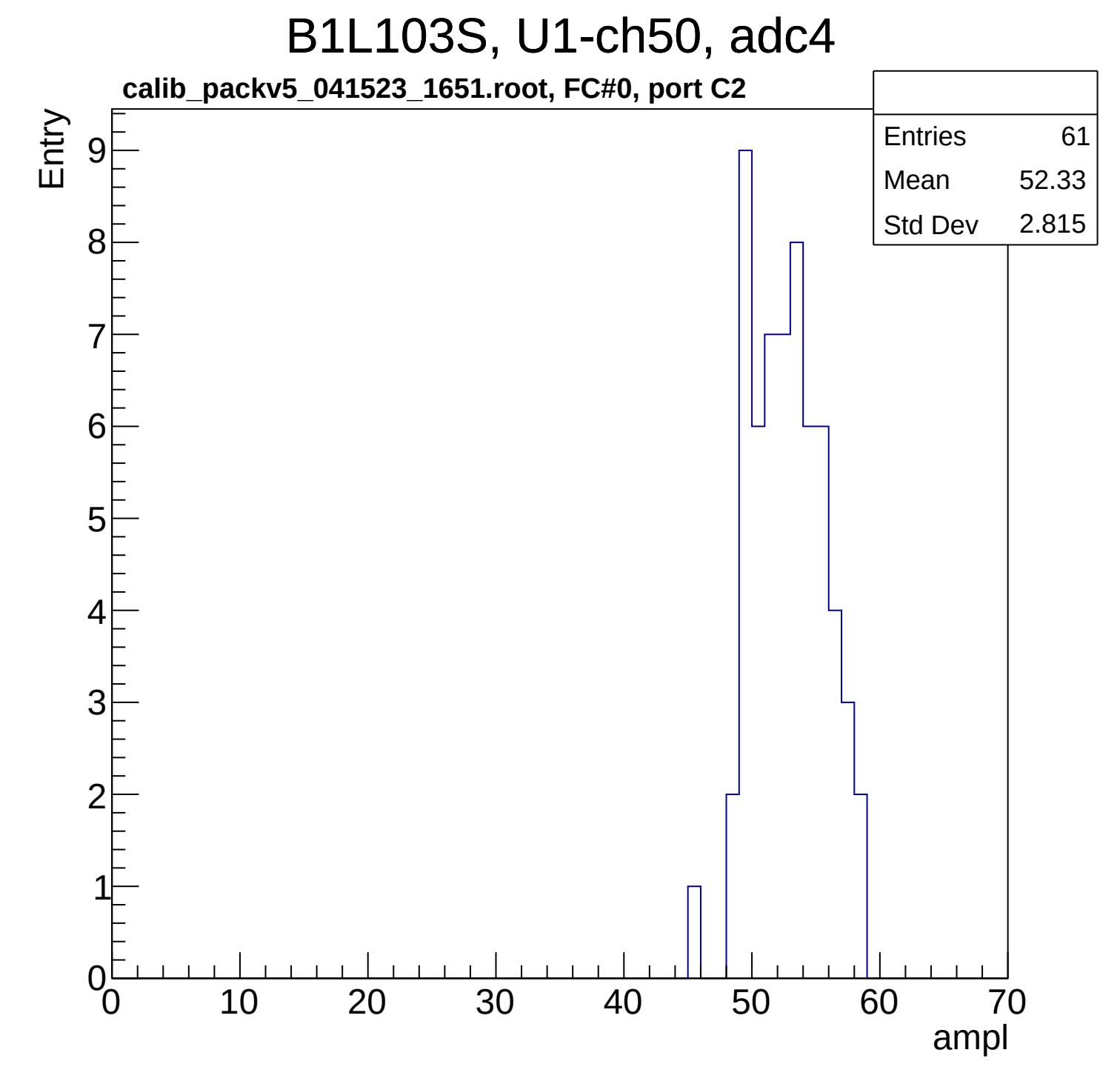
B1L103S, U1-ch50, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 52.33
Std Dev 2.815
Entry
ampl
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7
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0
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60
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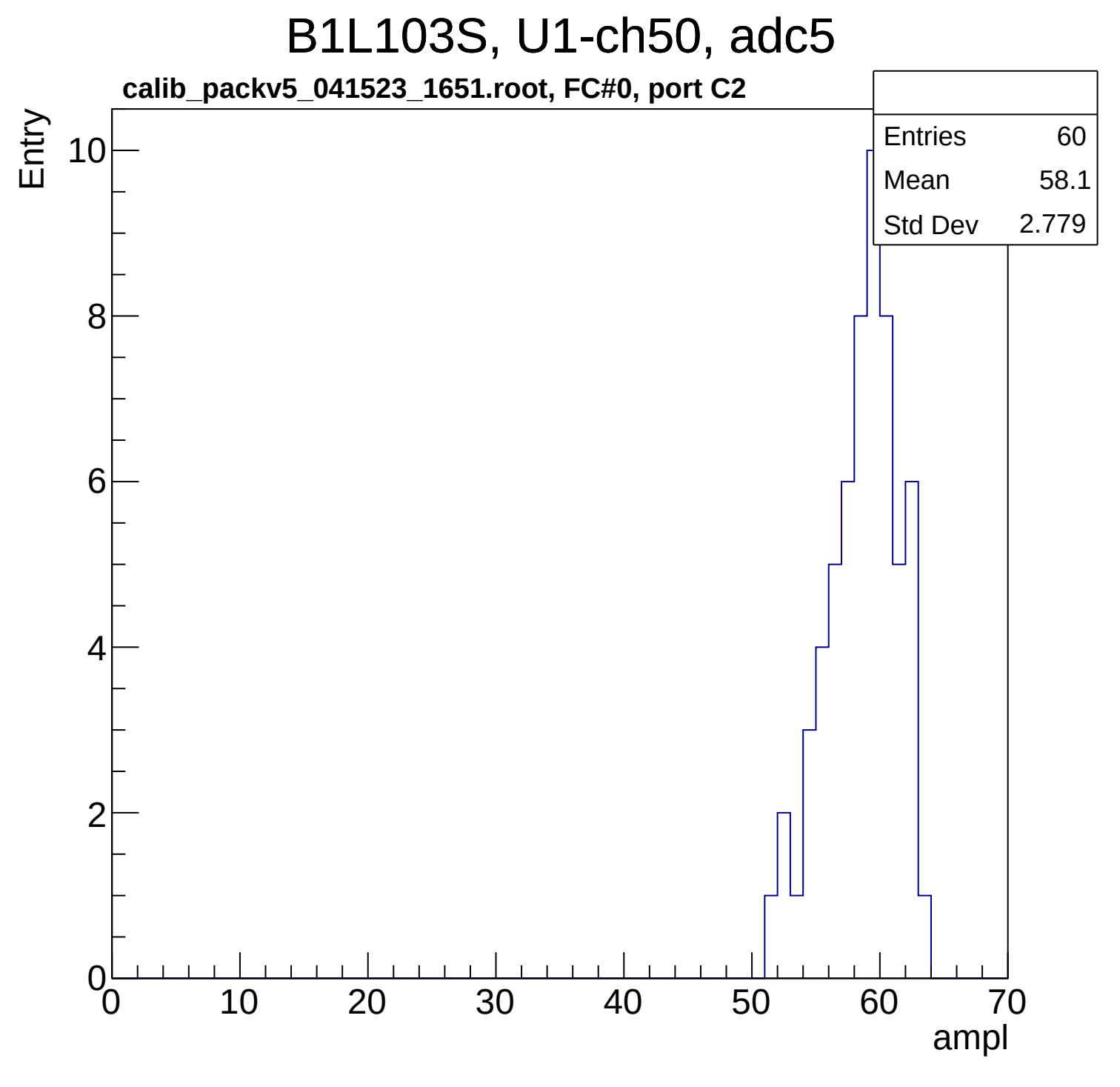
B1L103S, U1-ch50, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 58.1
Std Dev 2.779
Entry
ampl
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4
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0
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20
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60
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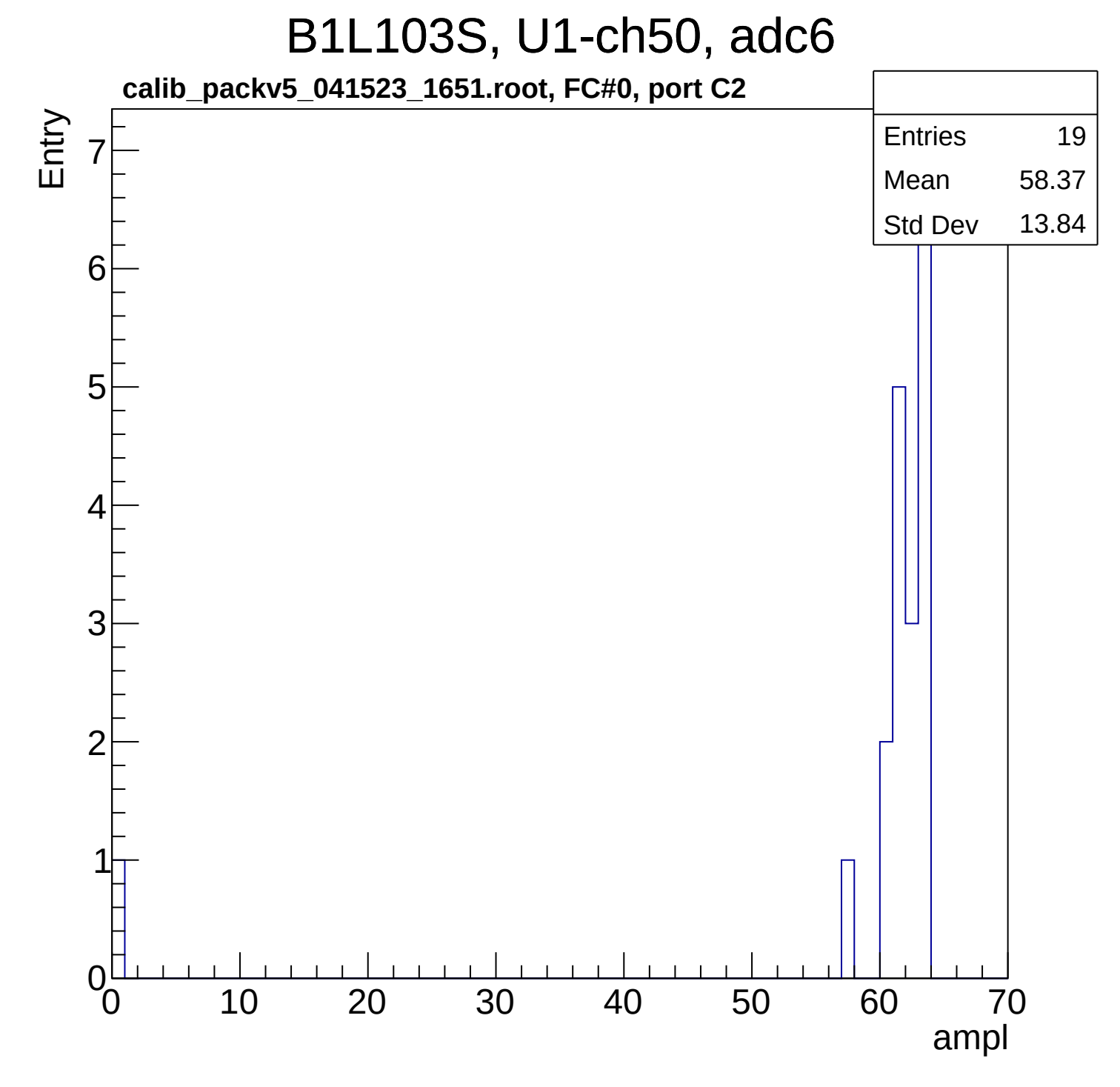
B1L103S, U1-ch50, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 58.37
Std Dev 13.84
Entry
ampl
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1
2
3
4
5
6
7
0
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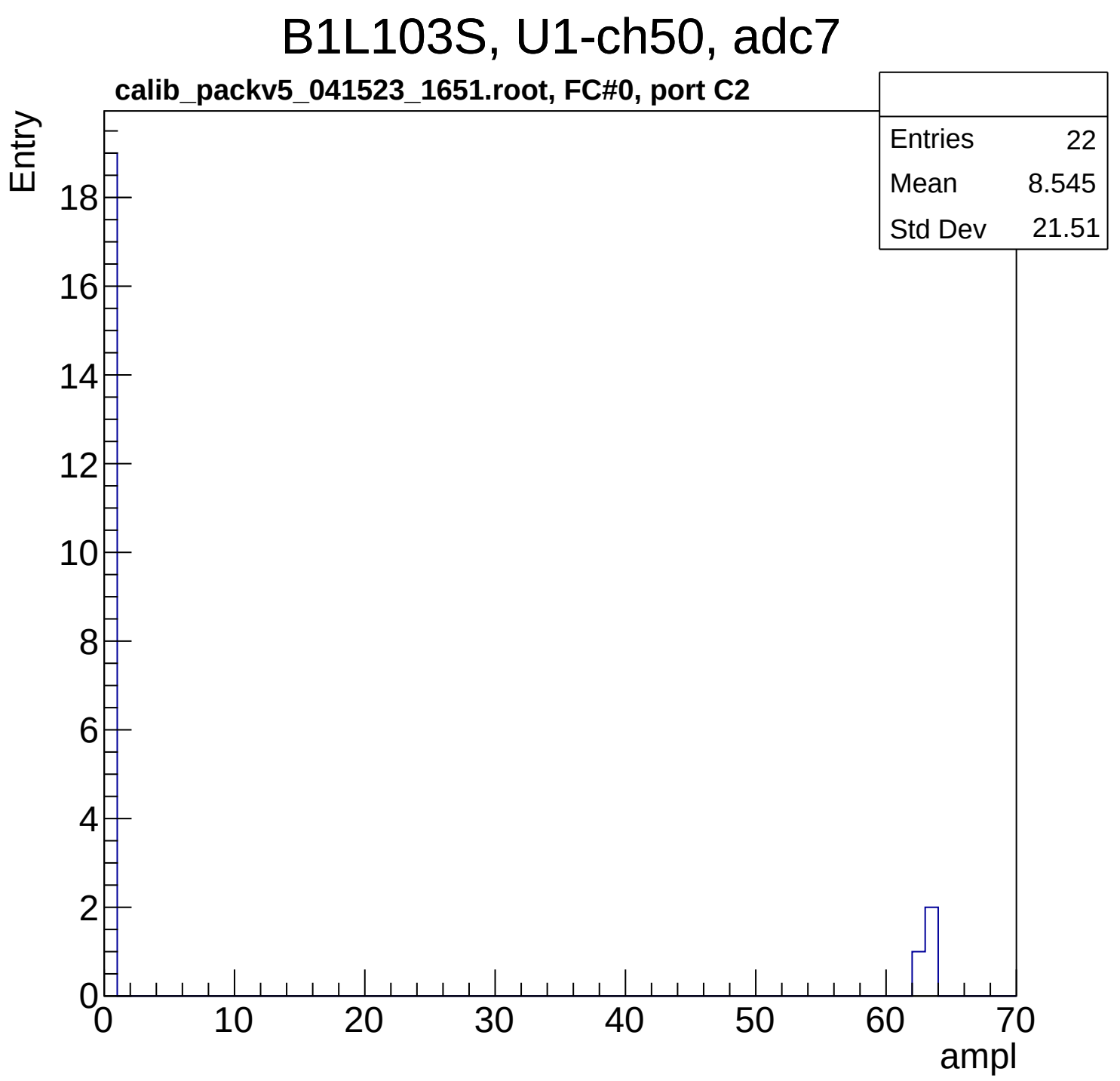
60
70


B1L103S, U1-ch50, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 8.545
Std Dev 21.51
Entry
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6
8
10
12
14
16
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10
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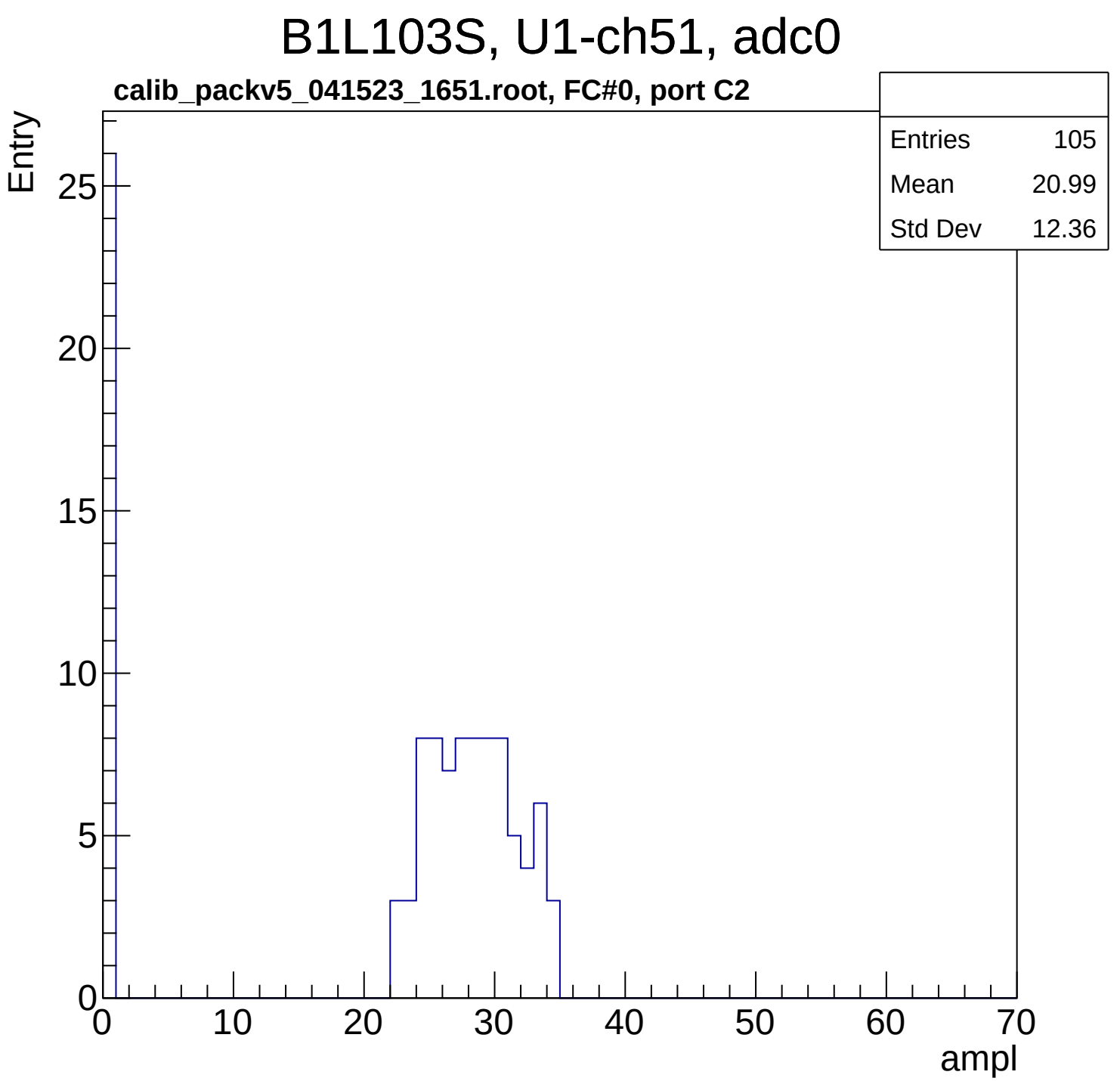
70
ampl


B1L103S, U1-ch51, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 105
Mean 20.99
Std Dev 12.36
Entry
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5
10
15
20
25
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10
20
30
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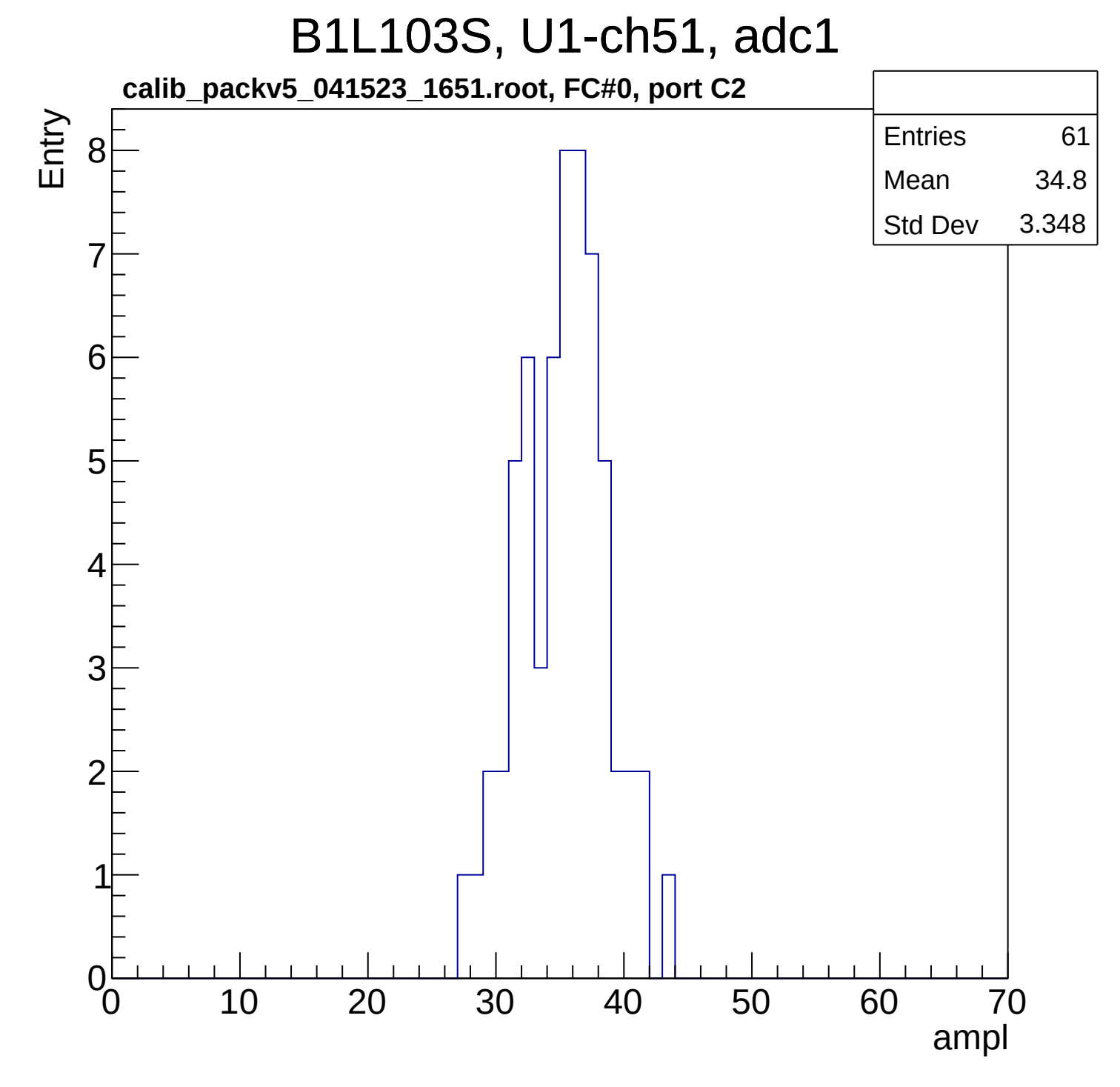
50
60
70
ampl


B1L103S, U1-ch51, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 34.8
Std Dev 3.348
Entry
ampl
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4
5
6
7
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0
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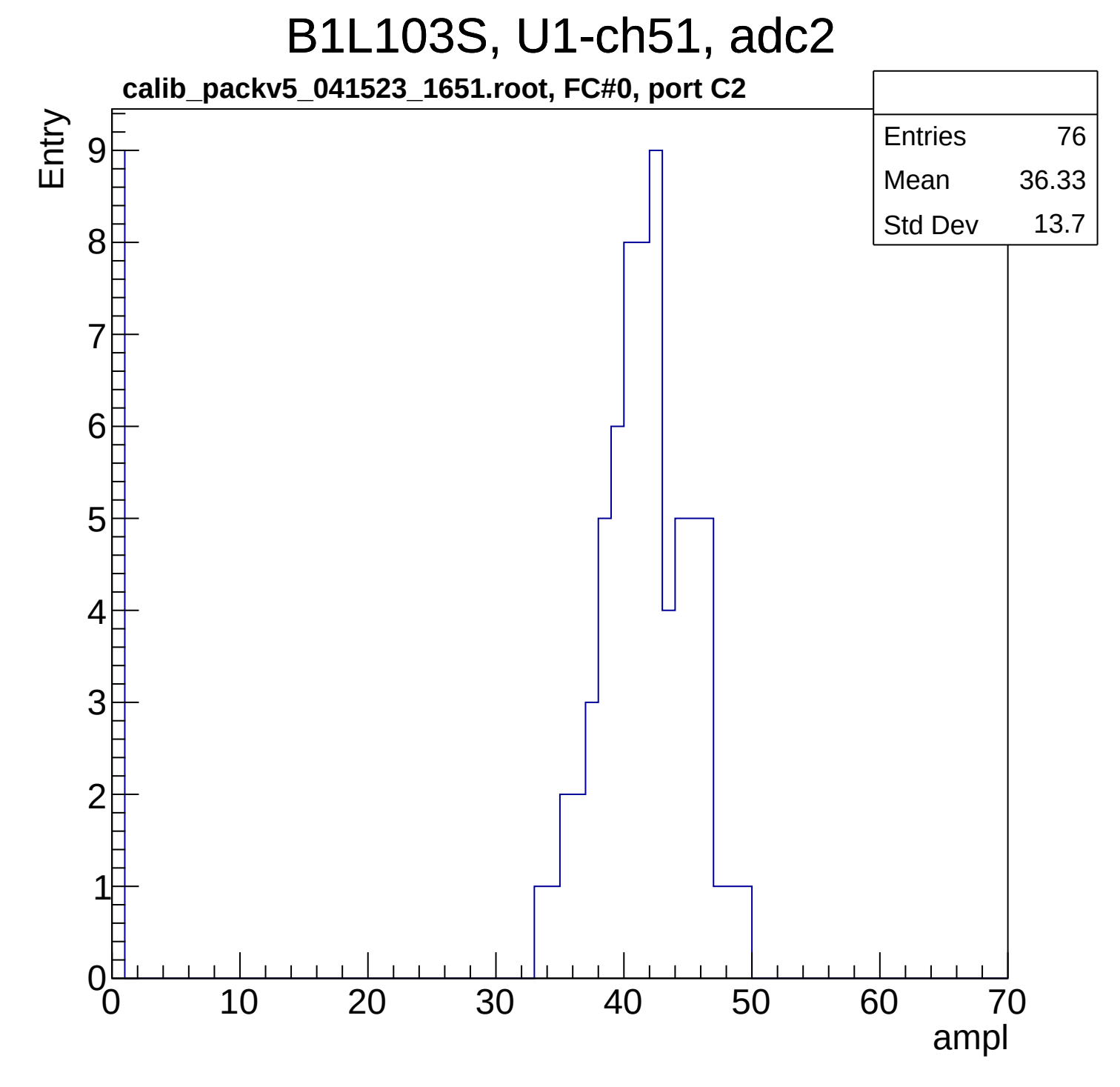
B1L103S, U1-ch51, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 36.33
Std Dev 13.7
Entry
ampl
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2
3
4
5
6
7
8
9
0
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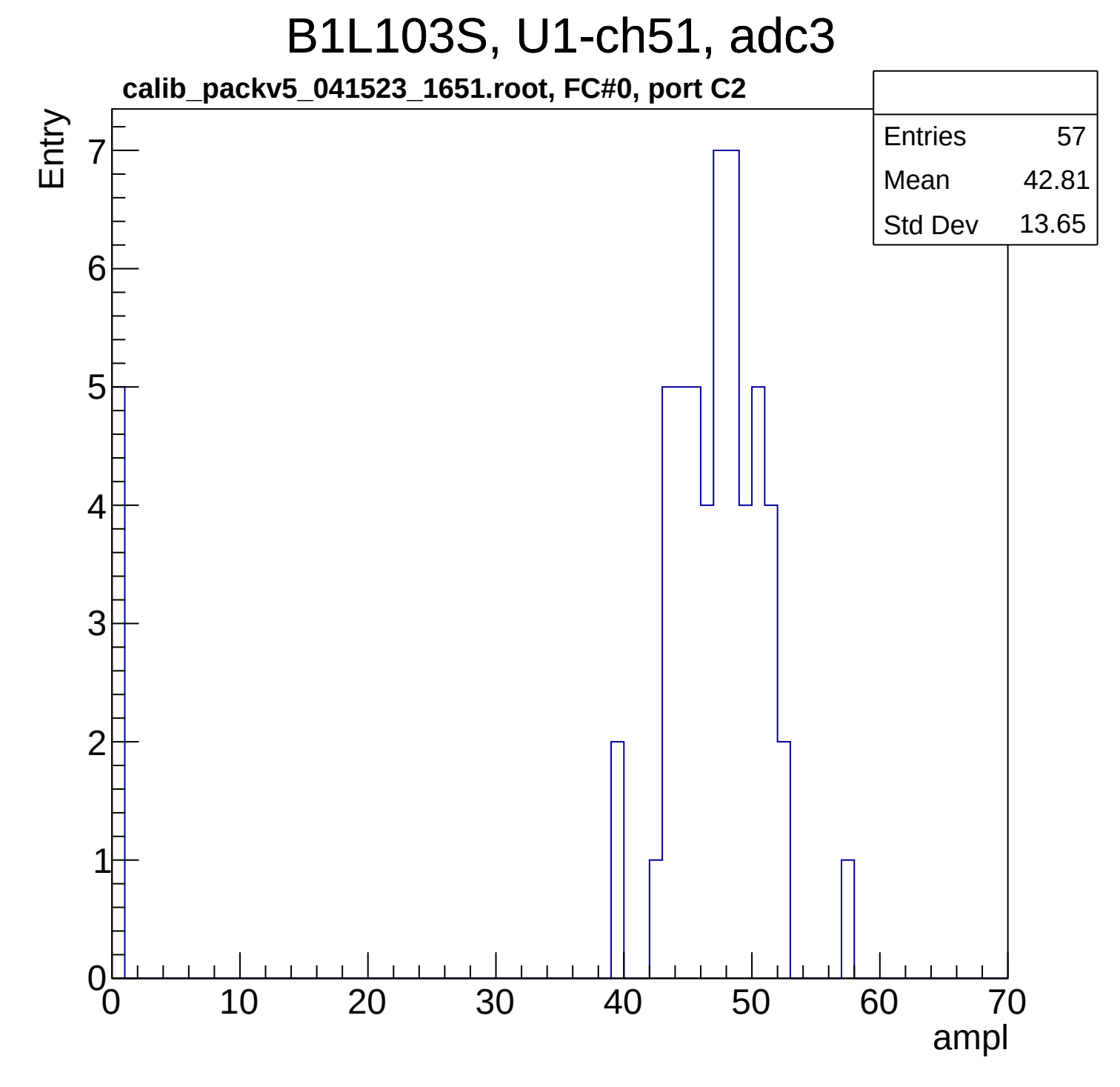
B1L103S, U1-ch51, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 42.81
Std Dev 13.65
Entry
ampl
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3
4
5
6
7
0
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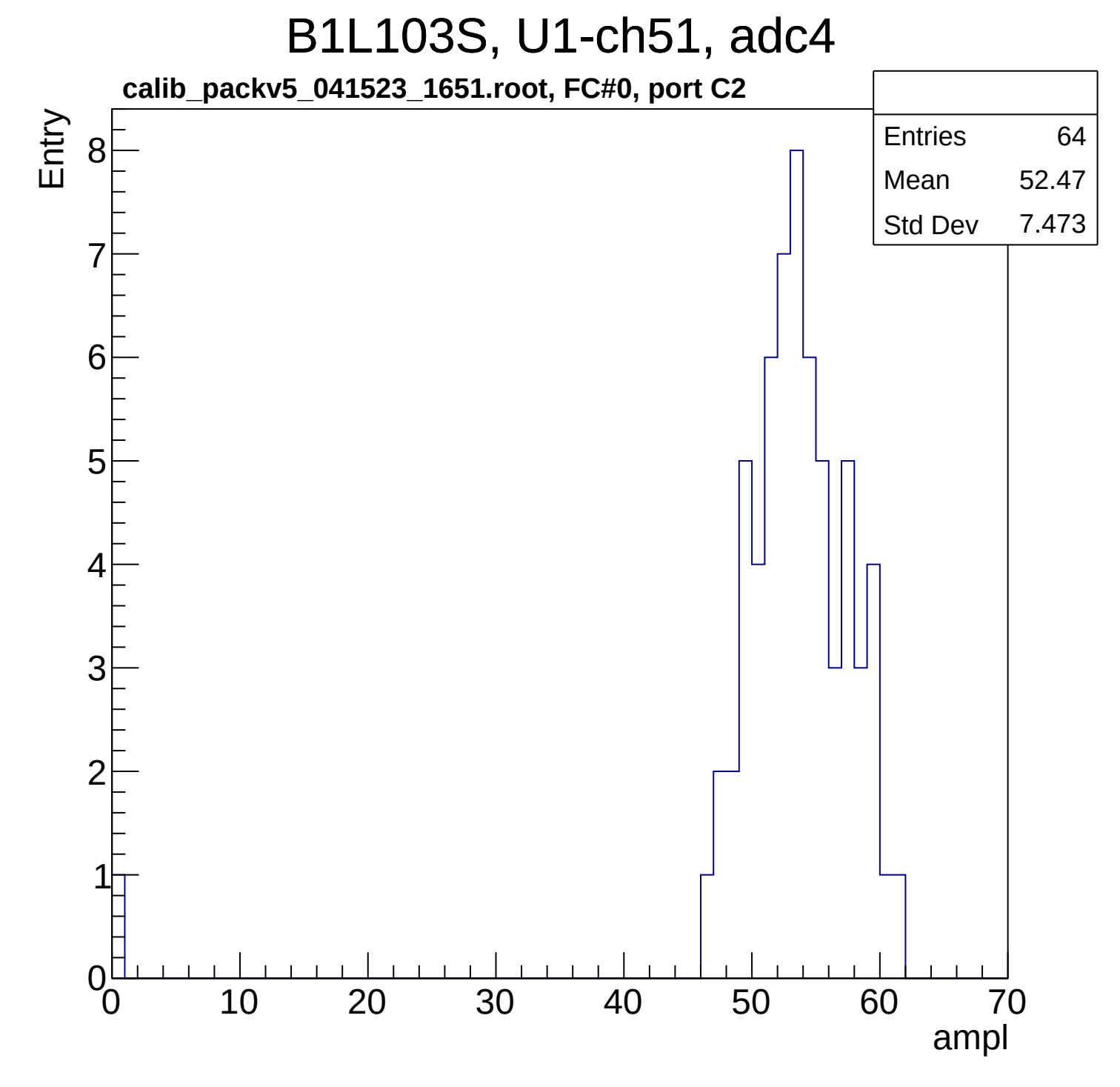
50
60
70


B1L103S, U1-ch51, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 52.47
Std Dev 7.473
Entry
ampl
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1
2
3
4
5
6
7
8
0
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40
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60
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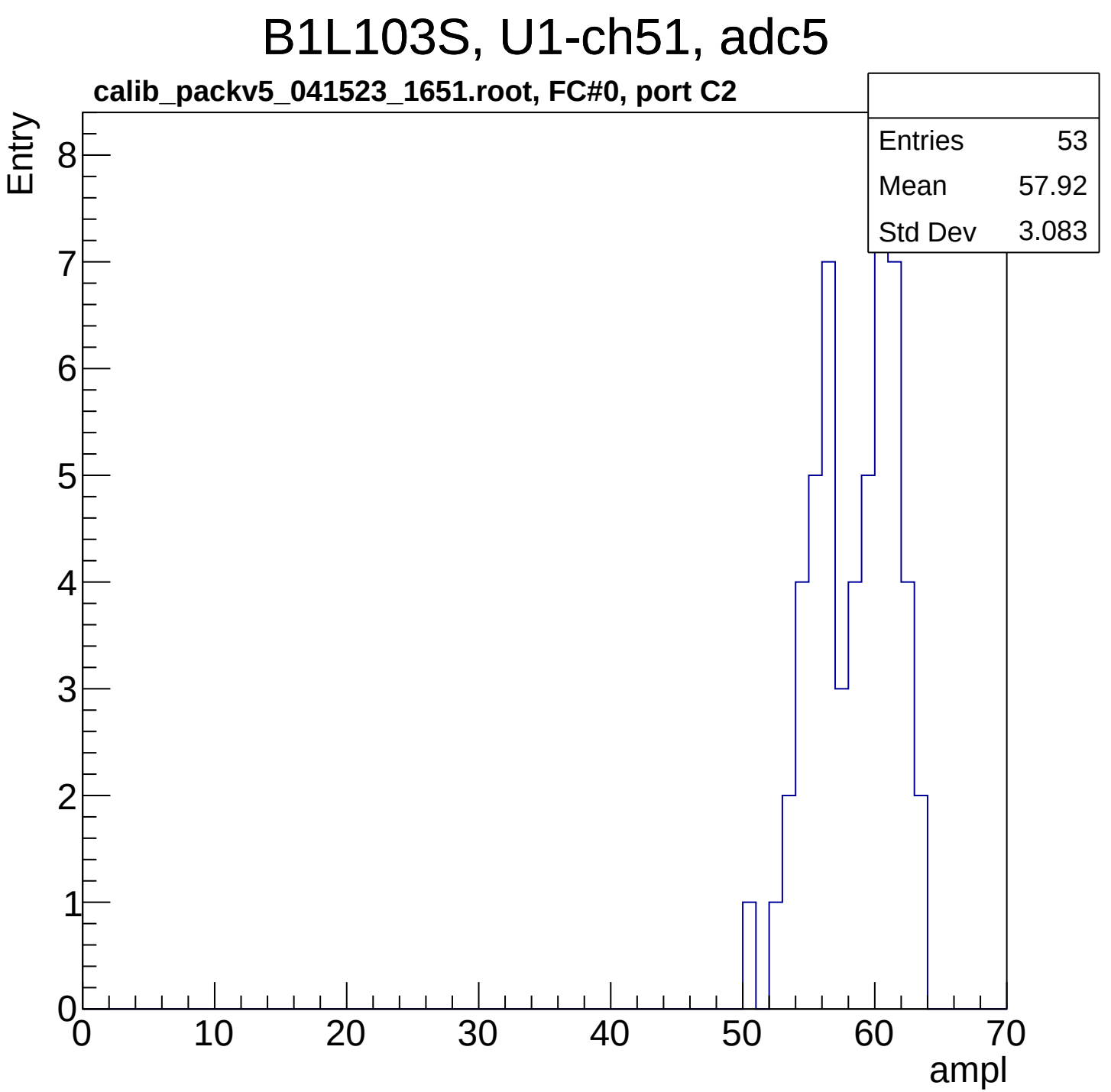
B1L103S, U1-ch51, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 57.92
Std Dev 3.083
Entry
ampl
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1
2
3
4
5
6
7
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0
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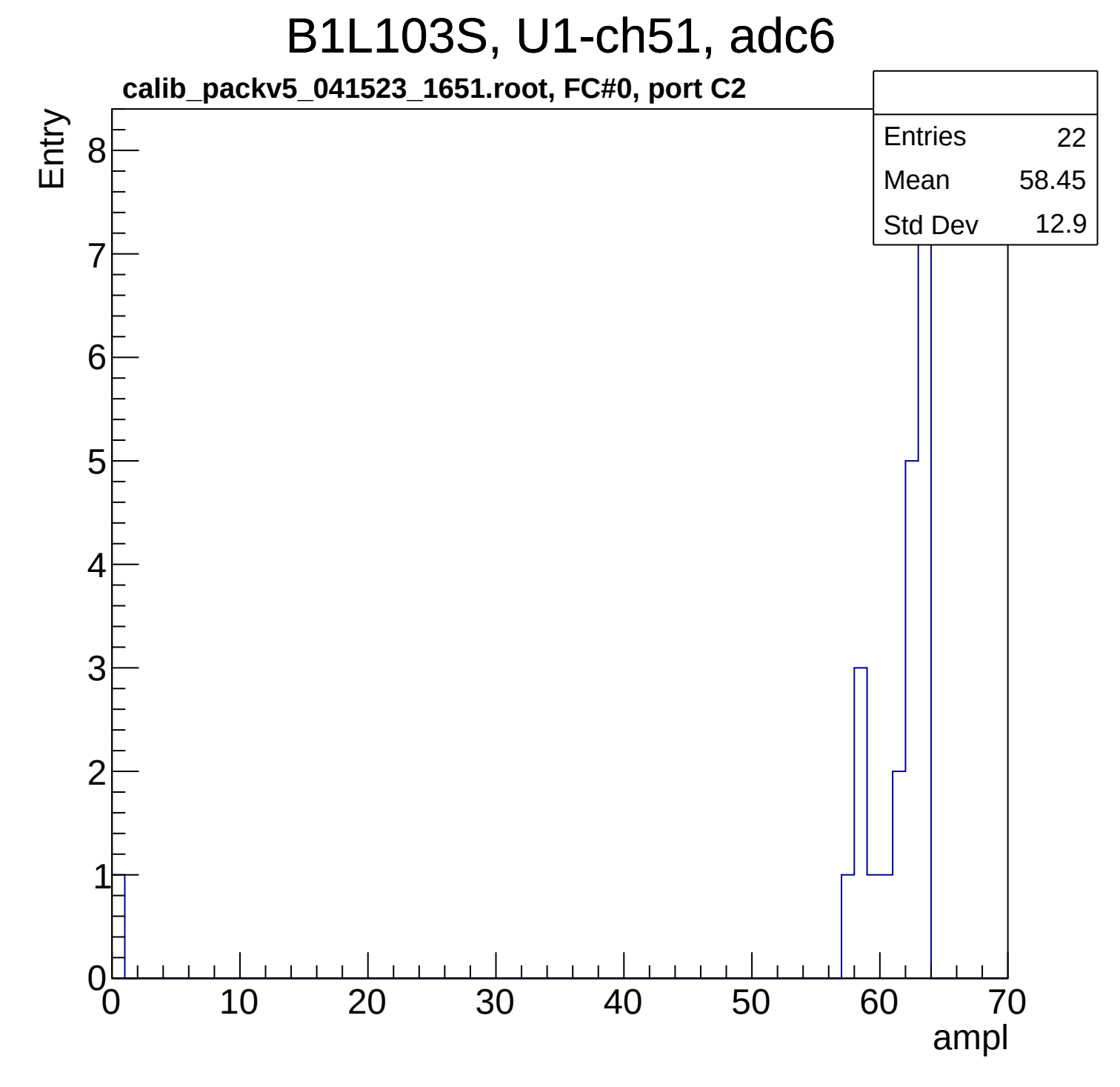
B1L103S, U1-ch51, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 58.45
Std Dev 12.9
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
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60
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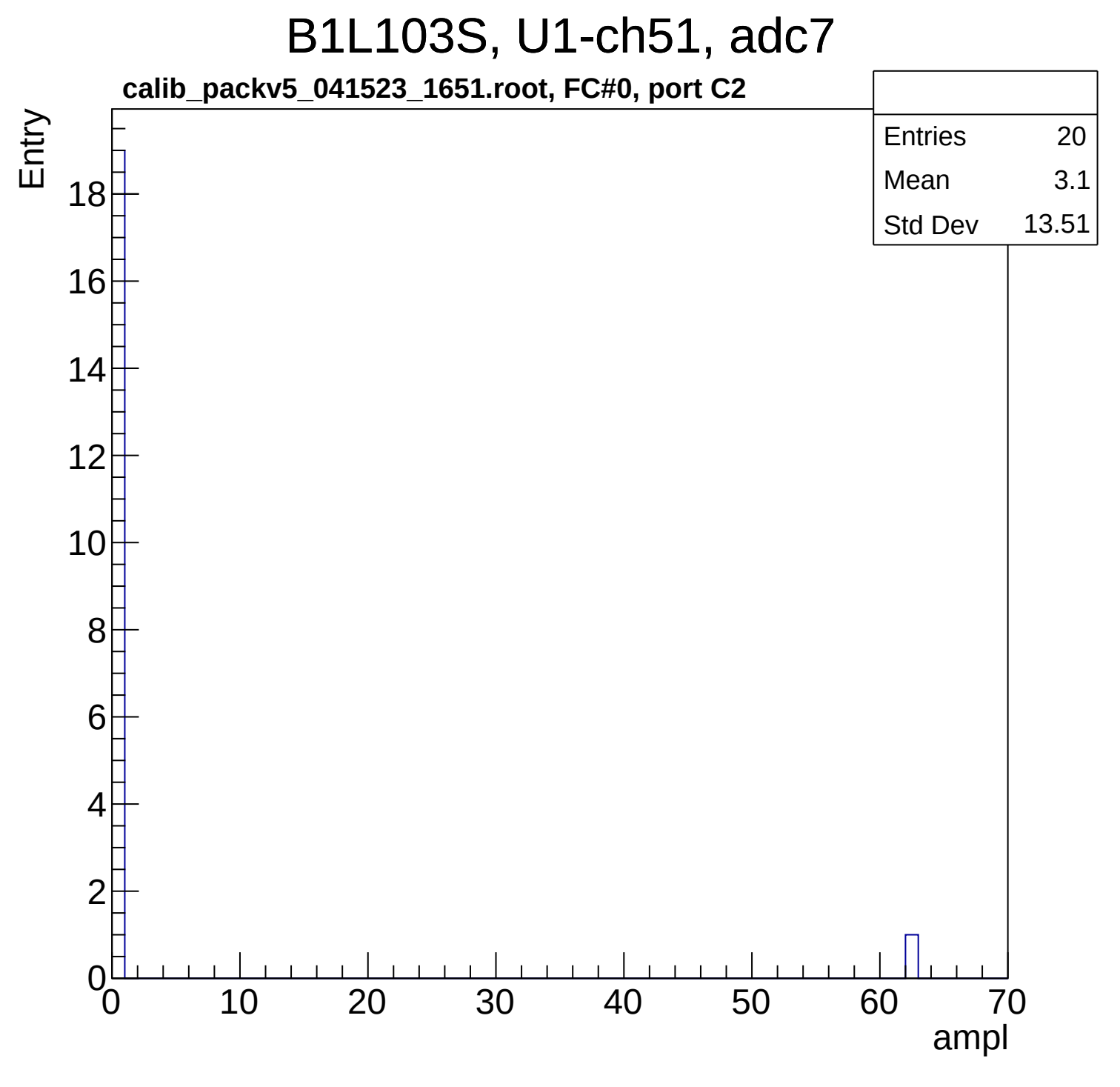
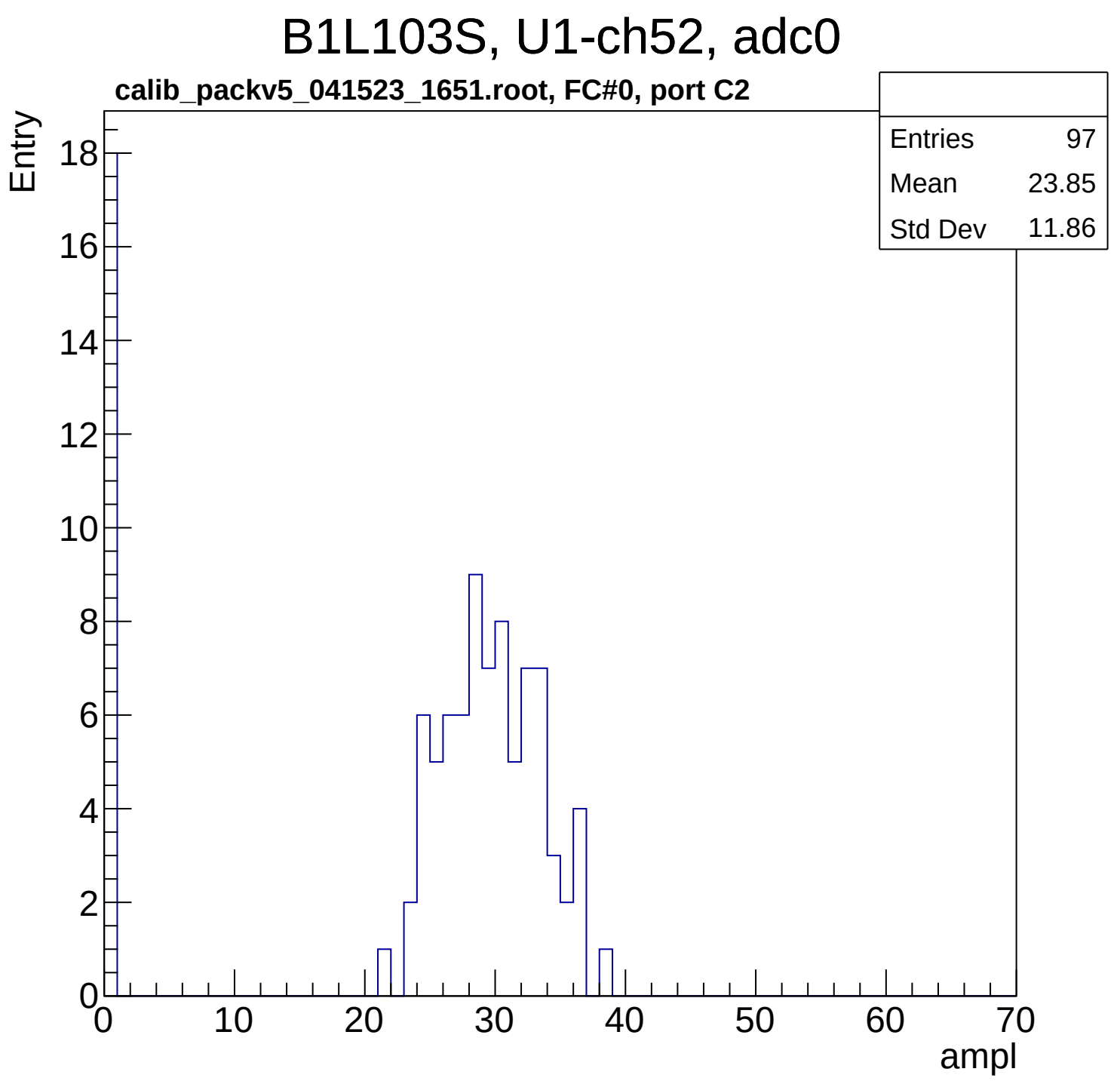

B1L103S, U1-ch51, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.1
Std Dev 13.51
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch52, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 97
Mean 23.85
Std Dev 11.86
Entry
ampl
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6
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12
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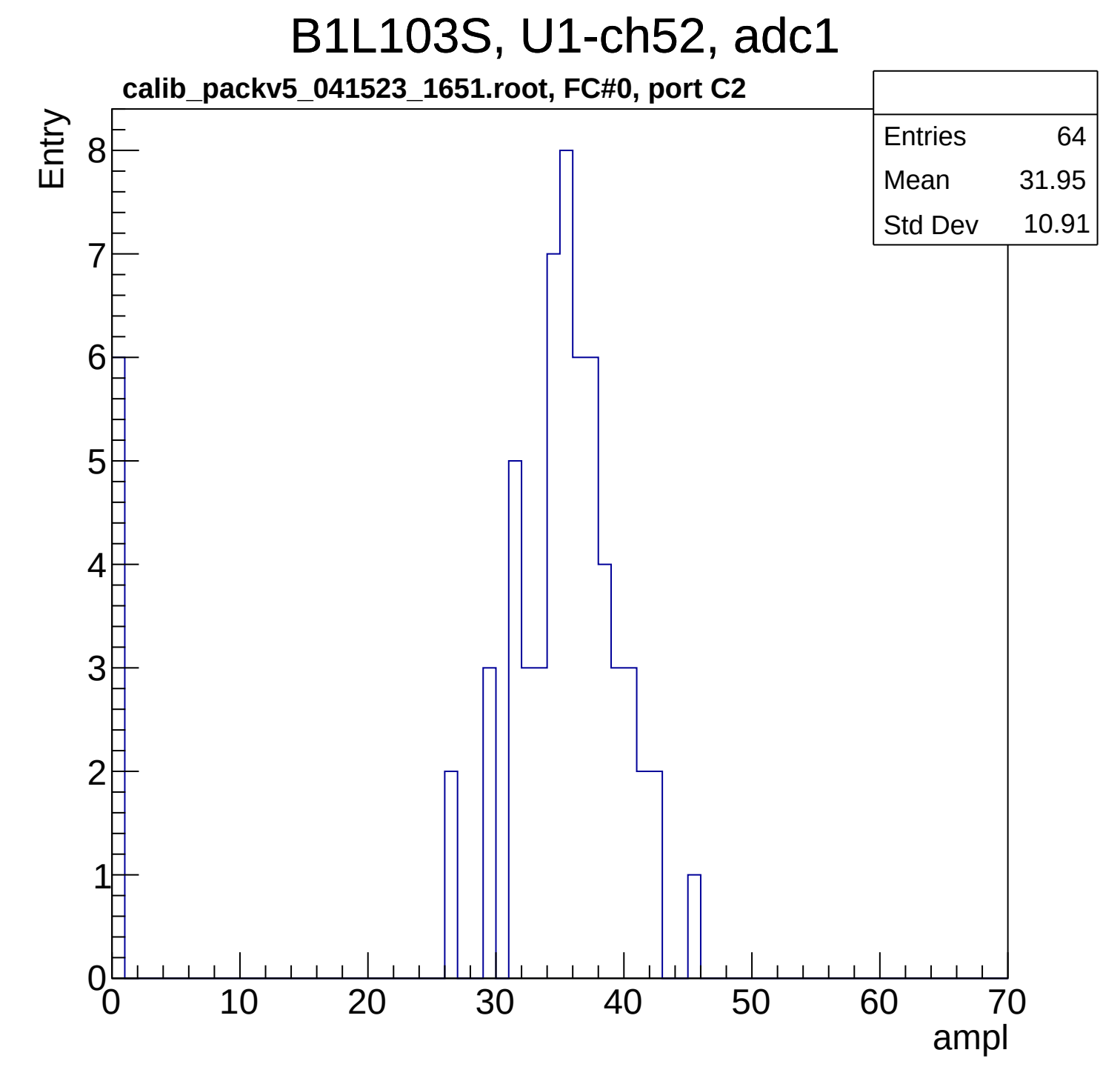
B1L103S, U1-ch52, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 31.95
Std Dev 10.91
Entry
ampl
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1
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3
4
5
6
7
8
0
10
20
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40
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60
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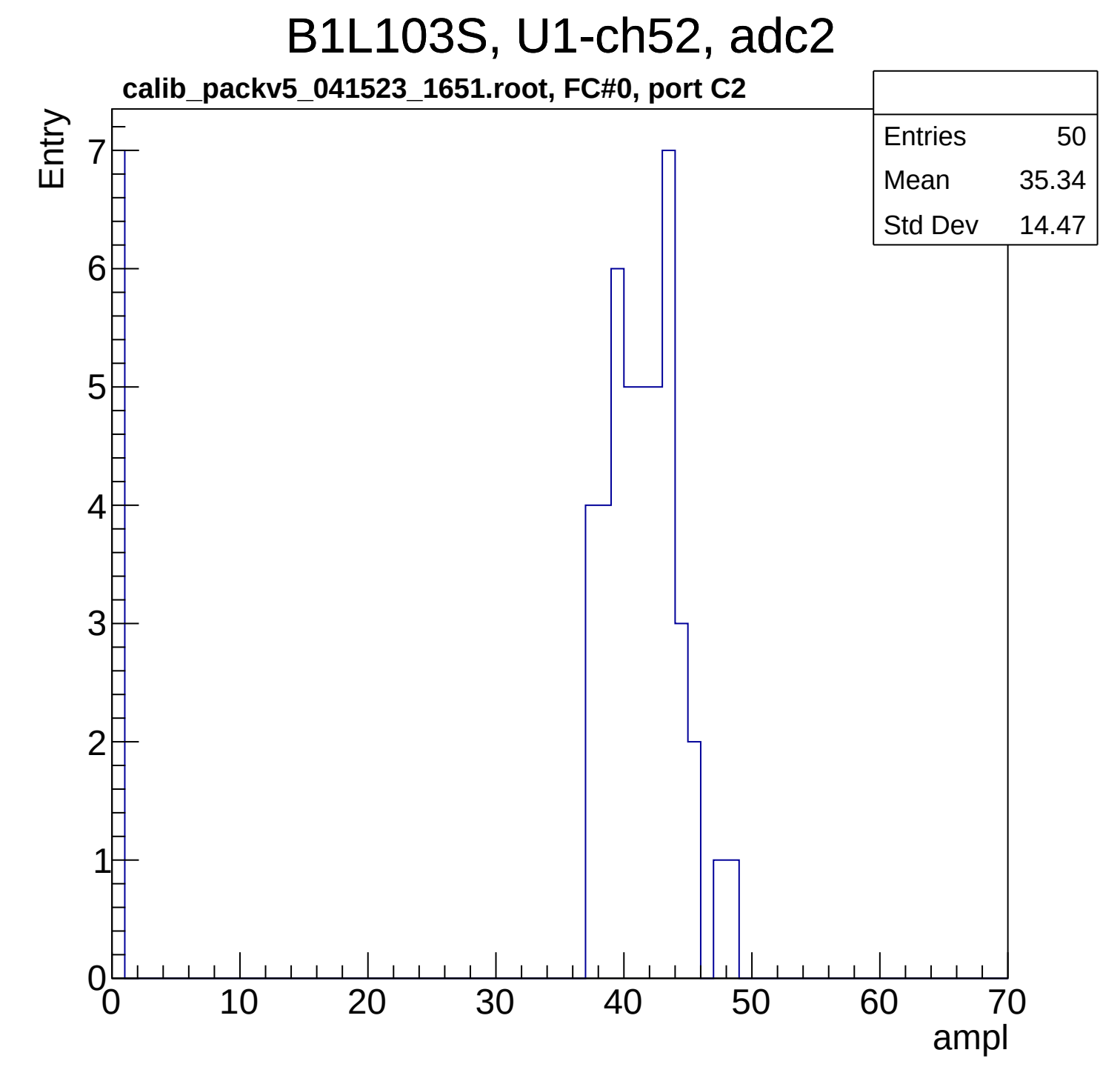
B1L103S, U1-ch52, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 35.34
Std Dev 14.47
Entry
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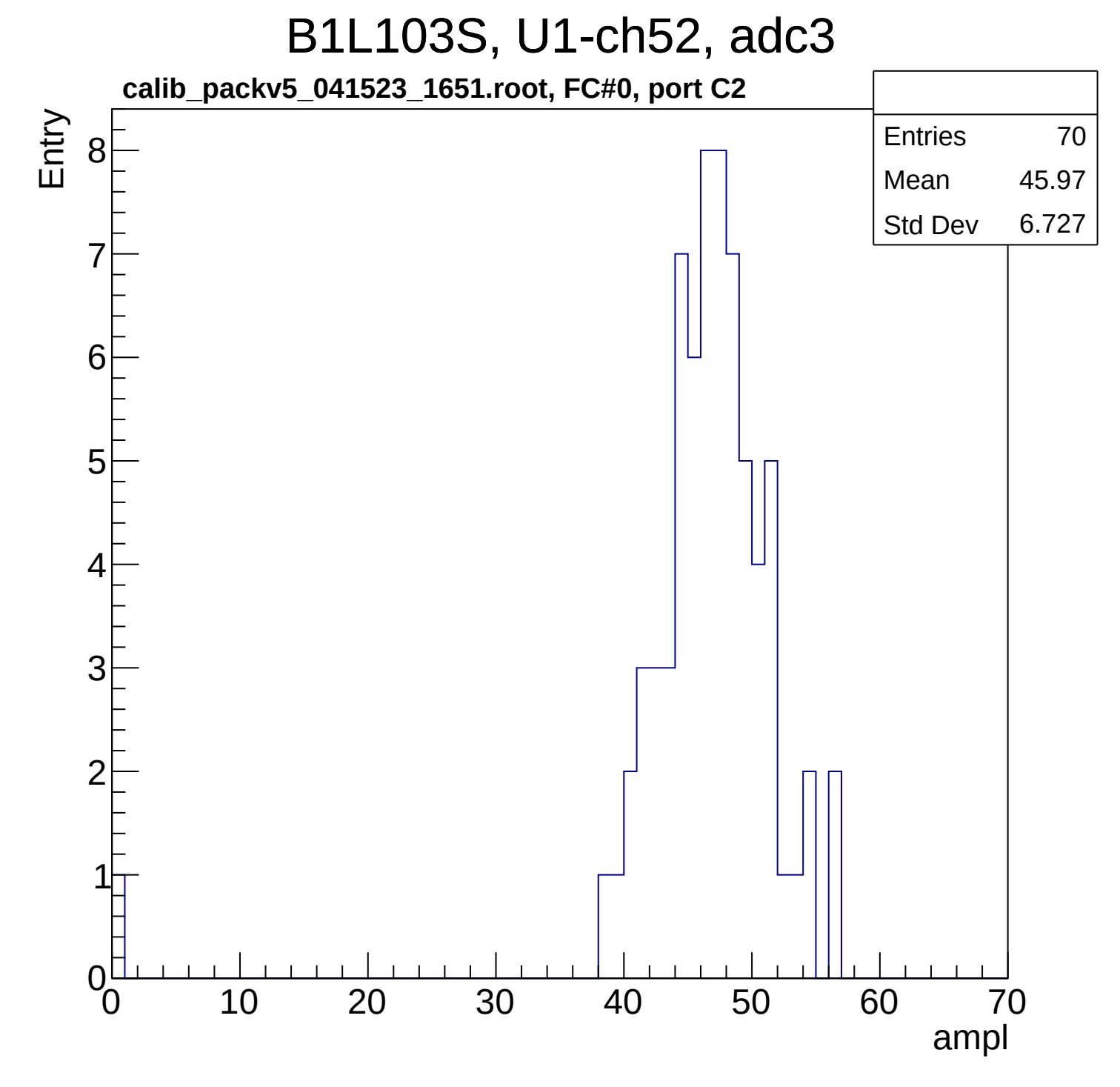
2
3
4
5
6
7
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch52, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 45.97
Std Dev 6.727
Entry
ampl
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3
4
5
6
7
8
0
10
20
30
40
50
60
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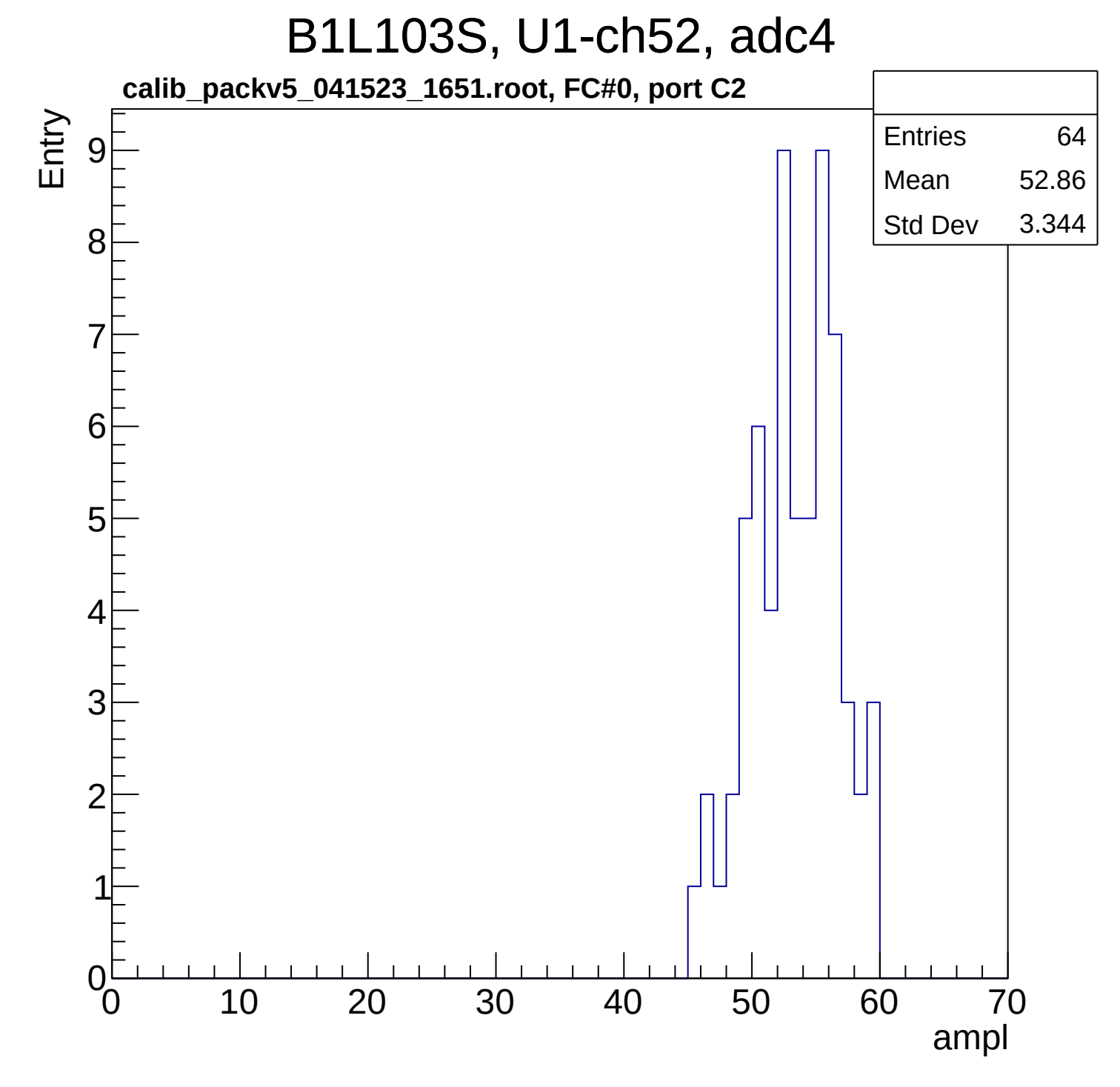
B1L103S, U1-ch52, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 52.86
Std Dev 3.344
Entry
ampl
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10
20
30
40
50
60
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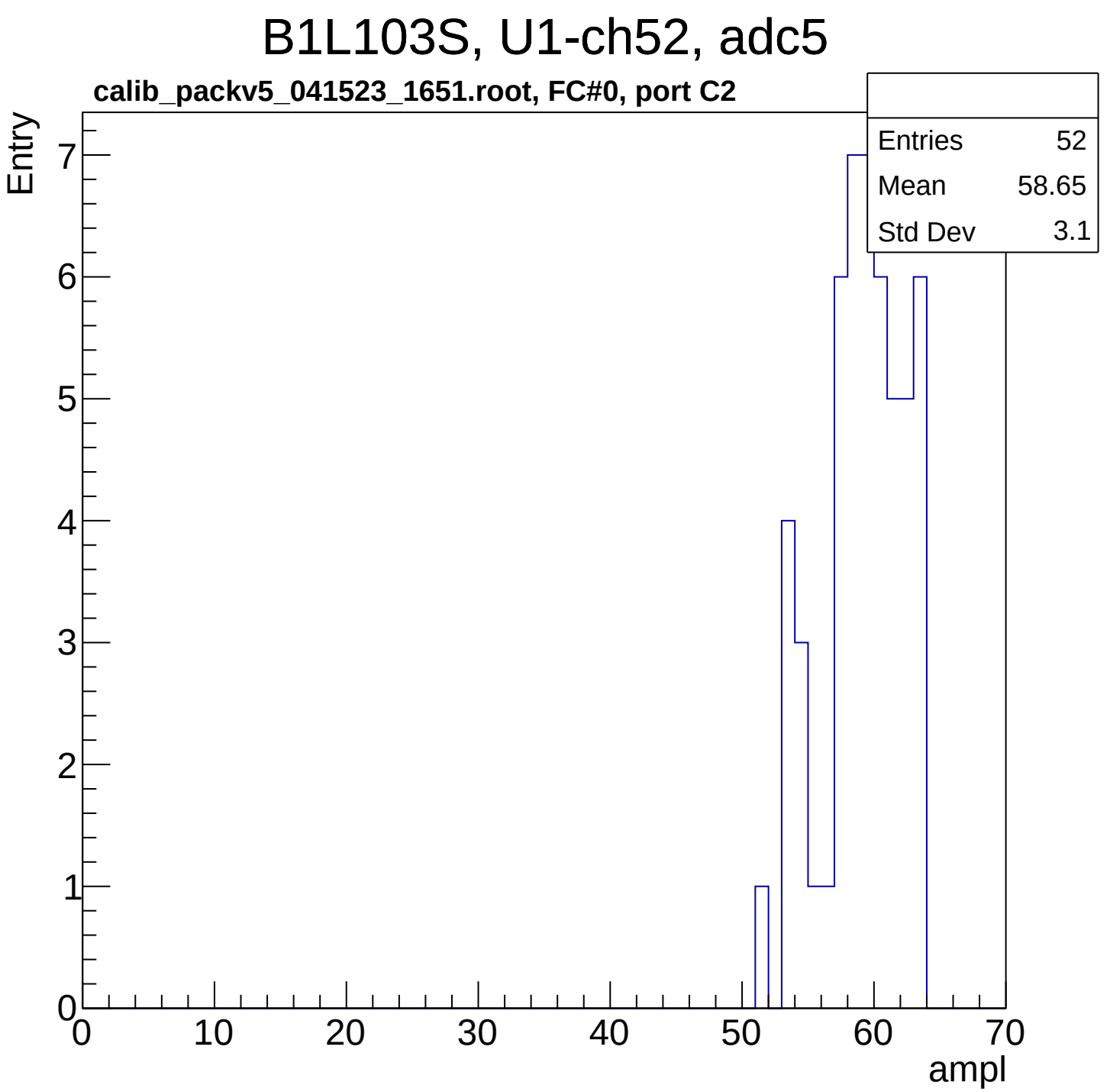
1
2
3
4
5
6
7
8
9


B1L103S, U1-ch52, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 58.65
Std Dev 3.1
Entry
ampl
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4
5
6
7
0
10
20
30
40
50
60
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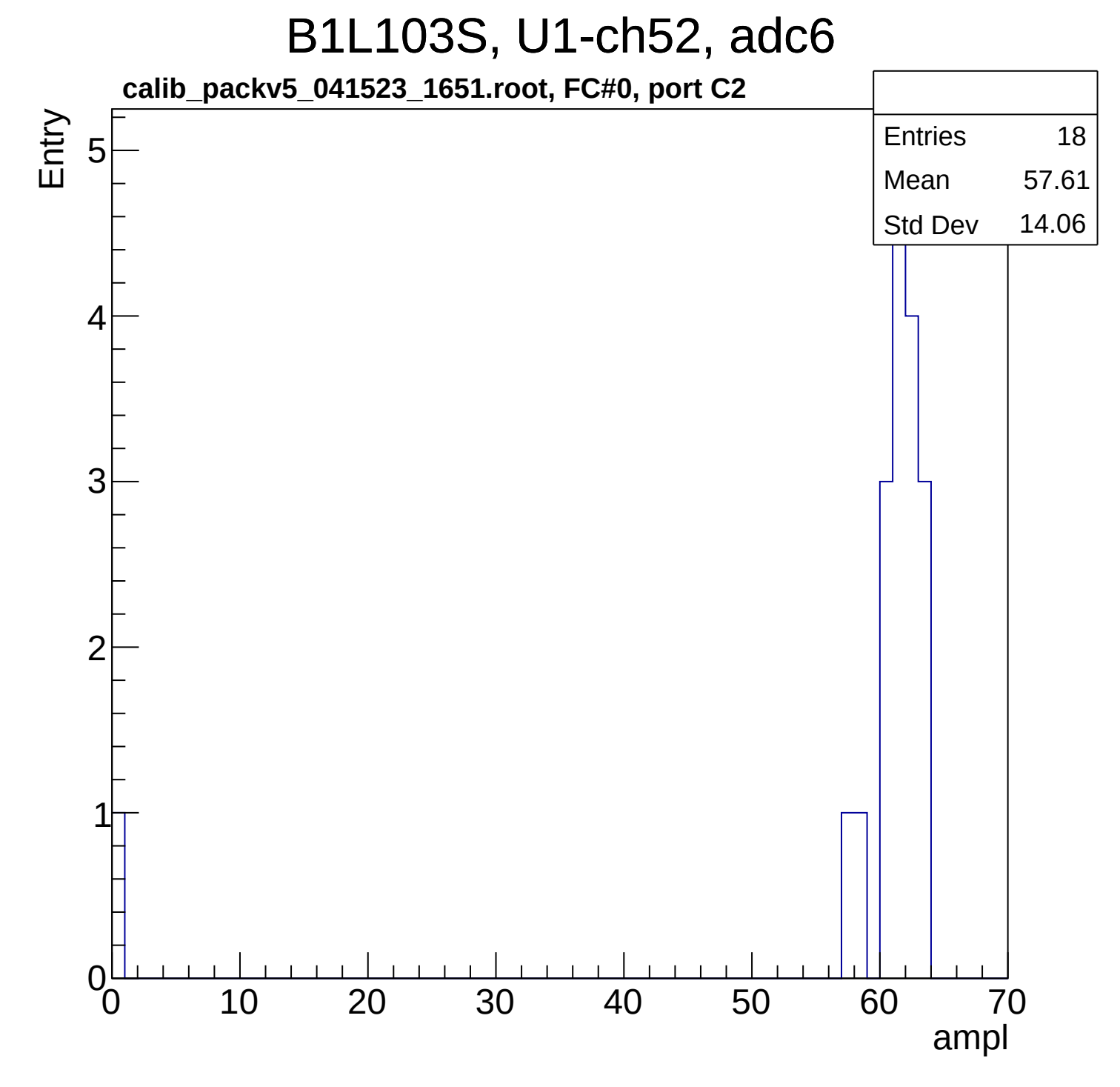
B1L103S, U1-ch52, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 57.61
Std Dev 14.06
Entry
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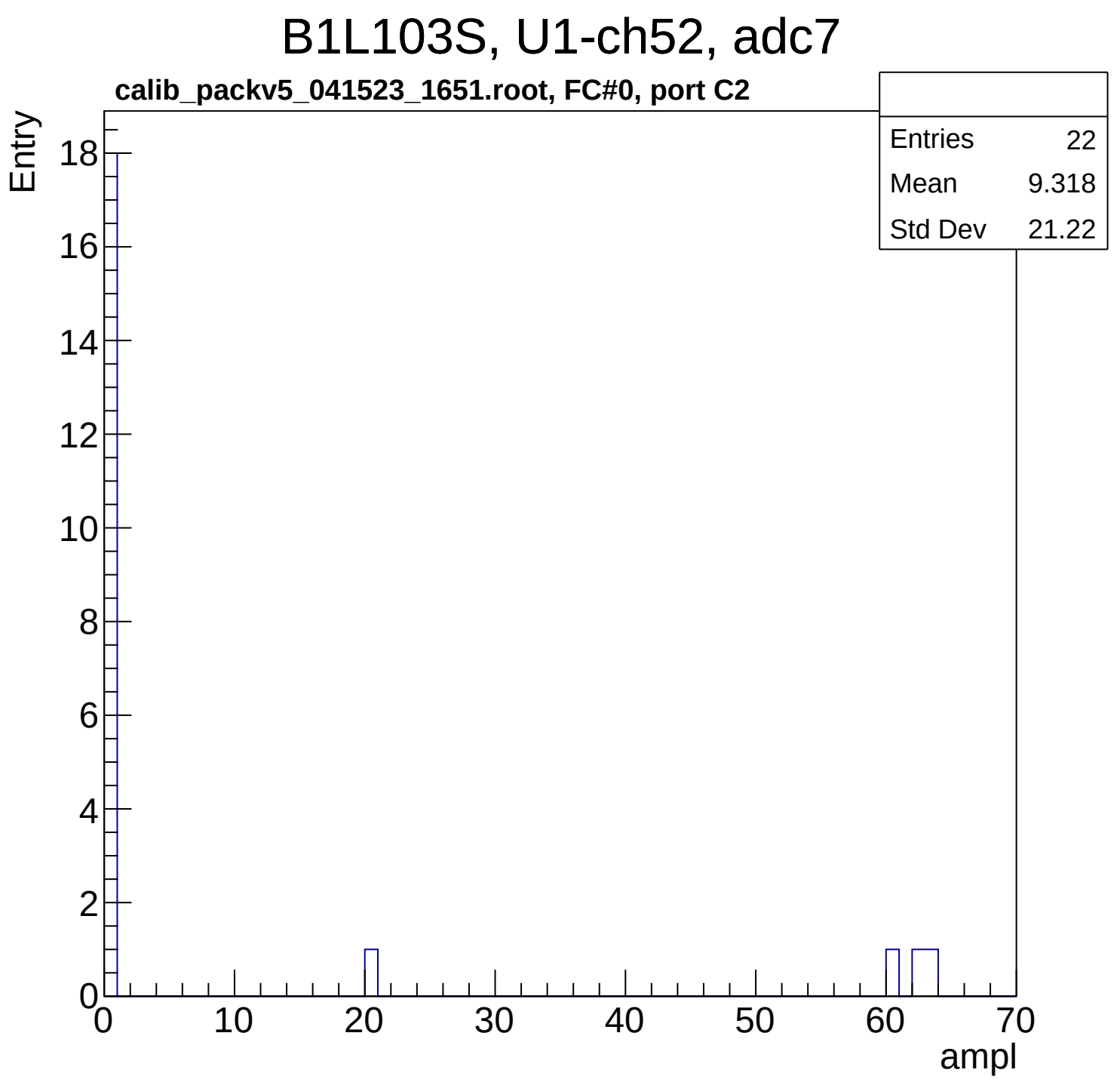
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch52, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 9.318
Std Dev 21.22
Entry
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4
6
8
10
12
14
16
18
0
10
20
30
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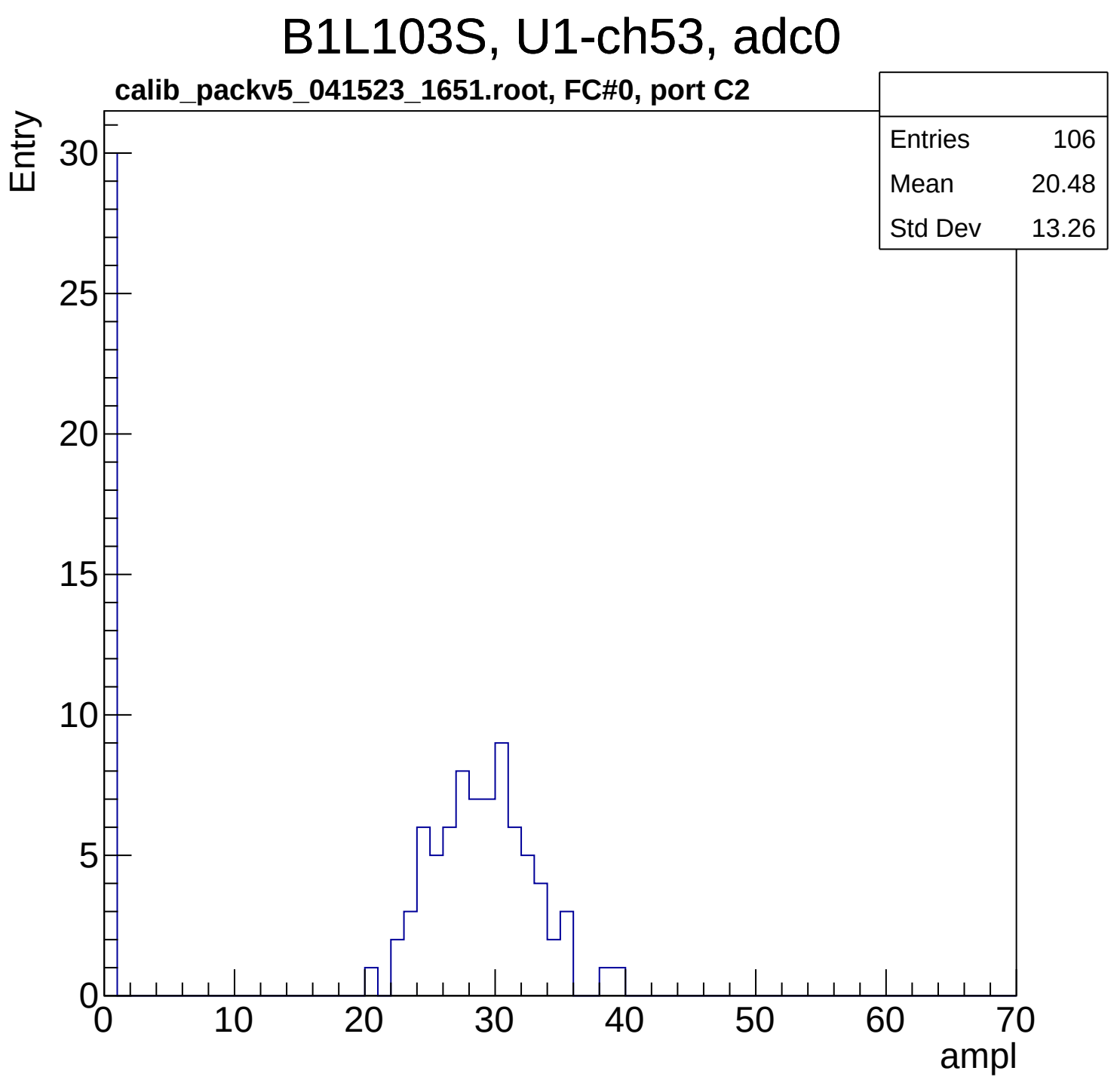
50
60
70
ampl


B1L103S, U1-ch53, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 106
Mean 20.48
Std Dev 13.26
Entry
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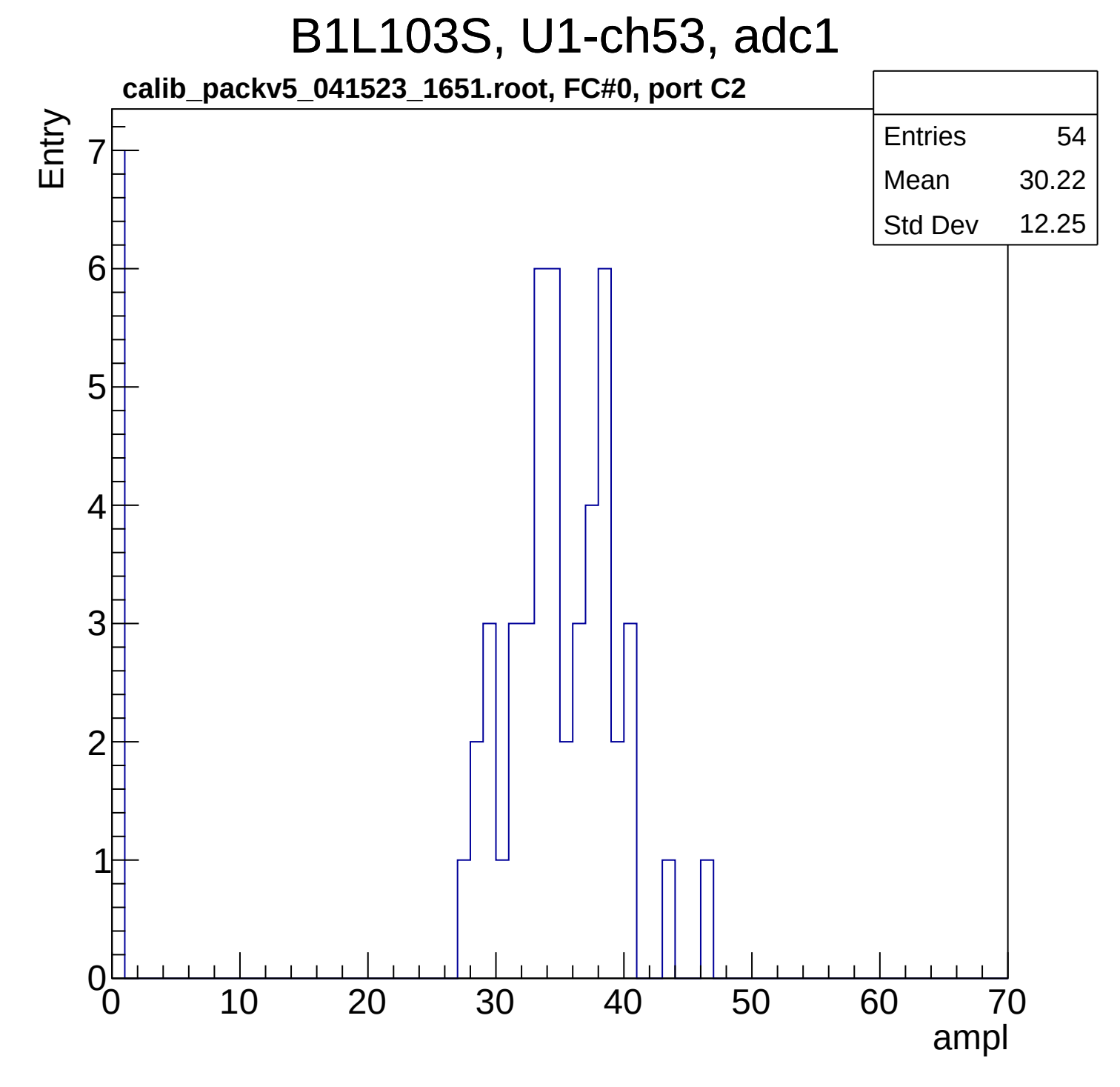
5
10
15
20
25
30
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch53, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 30.22
Std Dev 12.25
Entry
ampl
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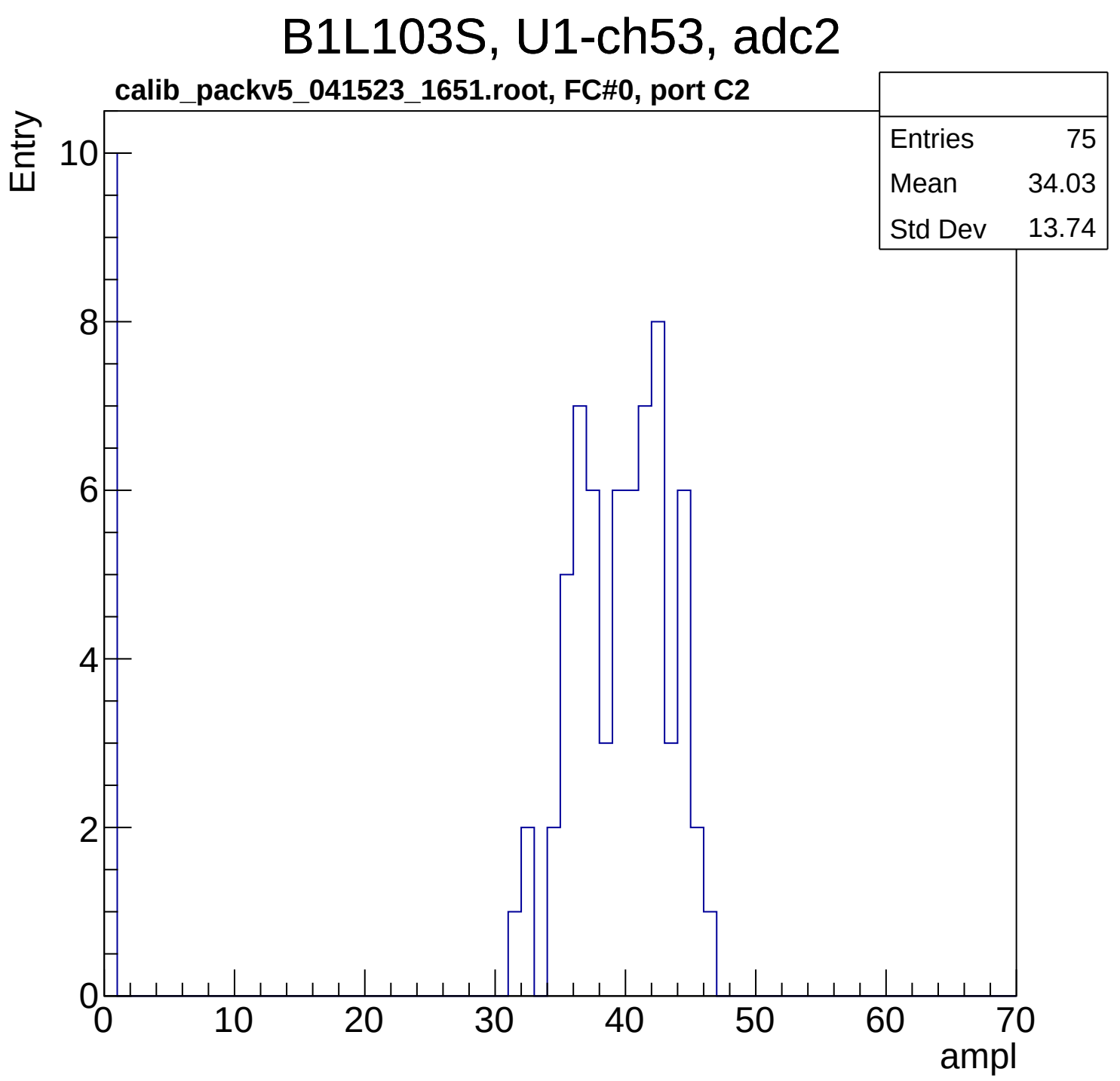
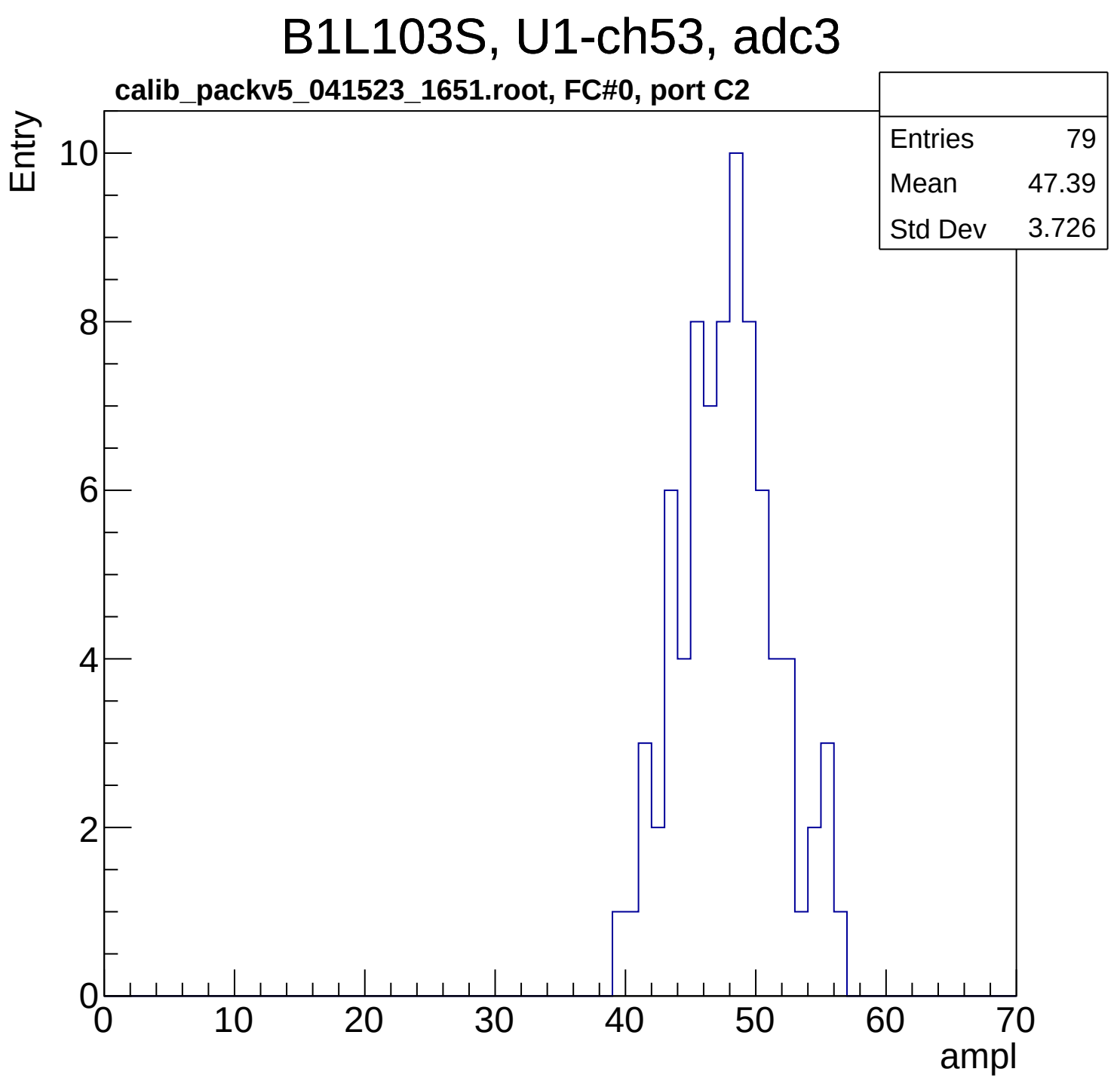
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U1-ch53, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 34.03
Std Dev 13.74
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U1-ch53, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 47.39
Std Dev 3.726
Entry
ampl
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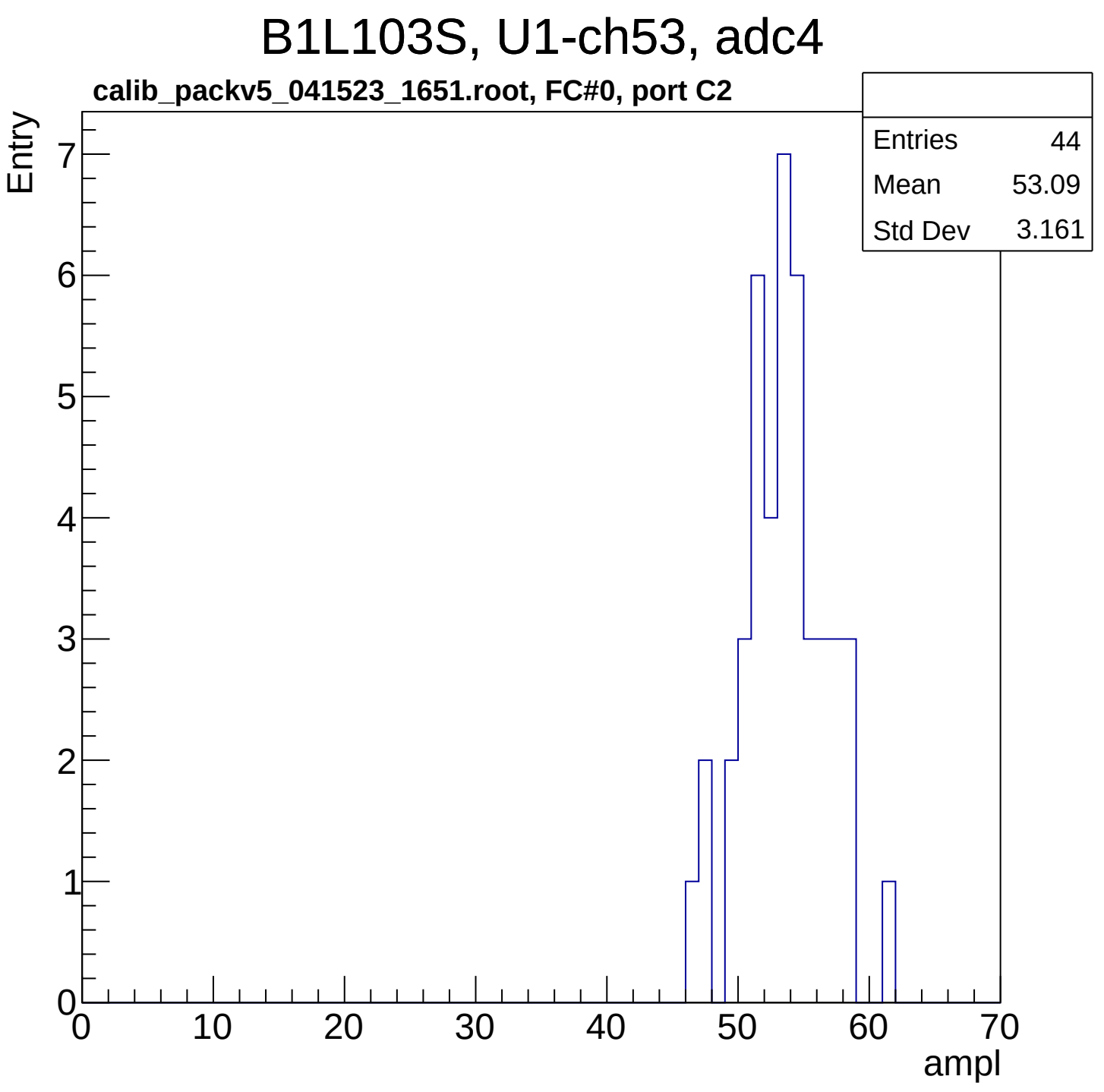
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U1-ch53, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 53.09
Std Dev 3.161
Entry
ampl
0
1
2
3
4
5
6
7
0
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20
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40
50
60
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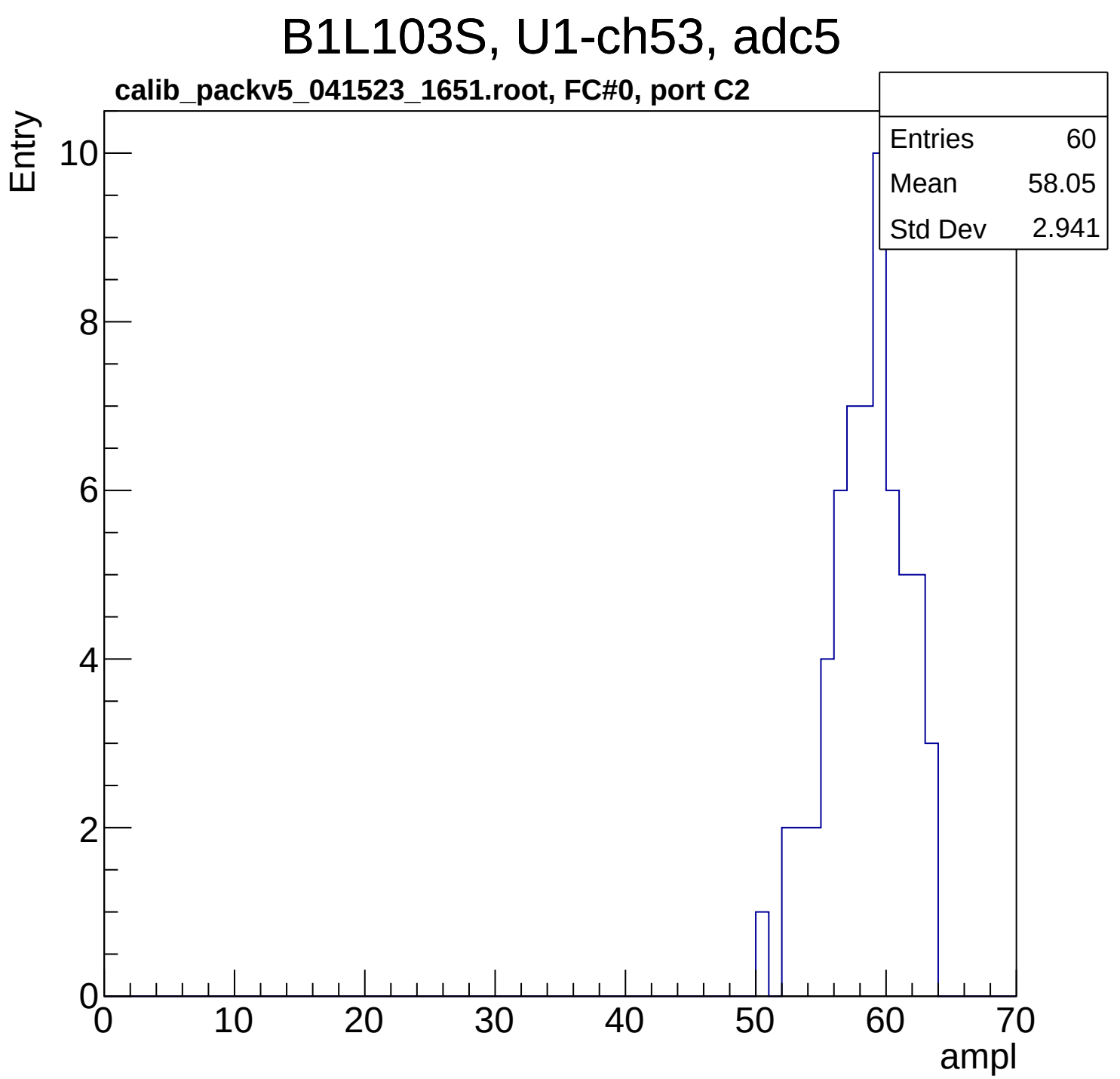
B1L103S, U1-ch53, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 58.05
Std Dev 2.941
Entry
ampl
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2
4
6
8
10
0
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20
30
40
50
60
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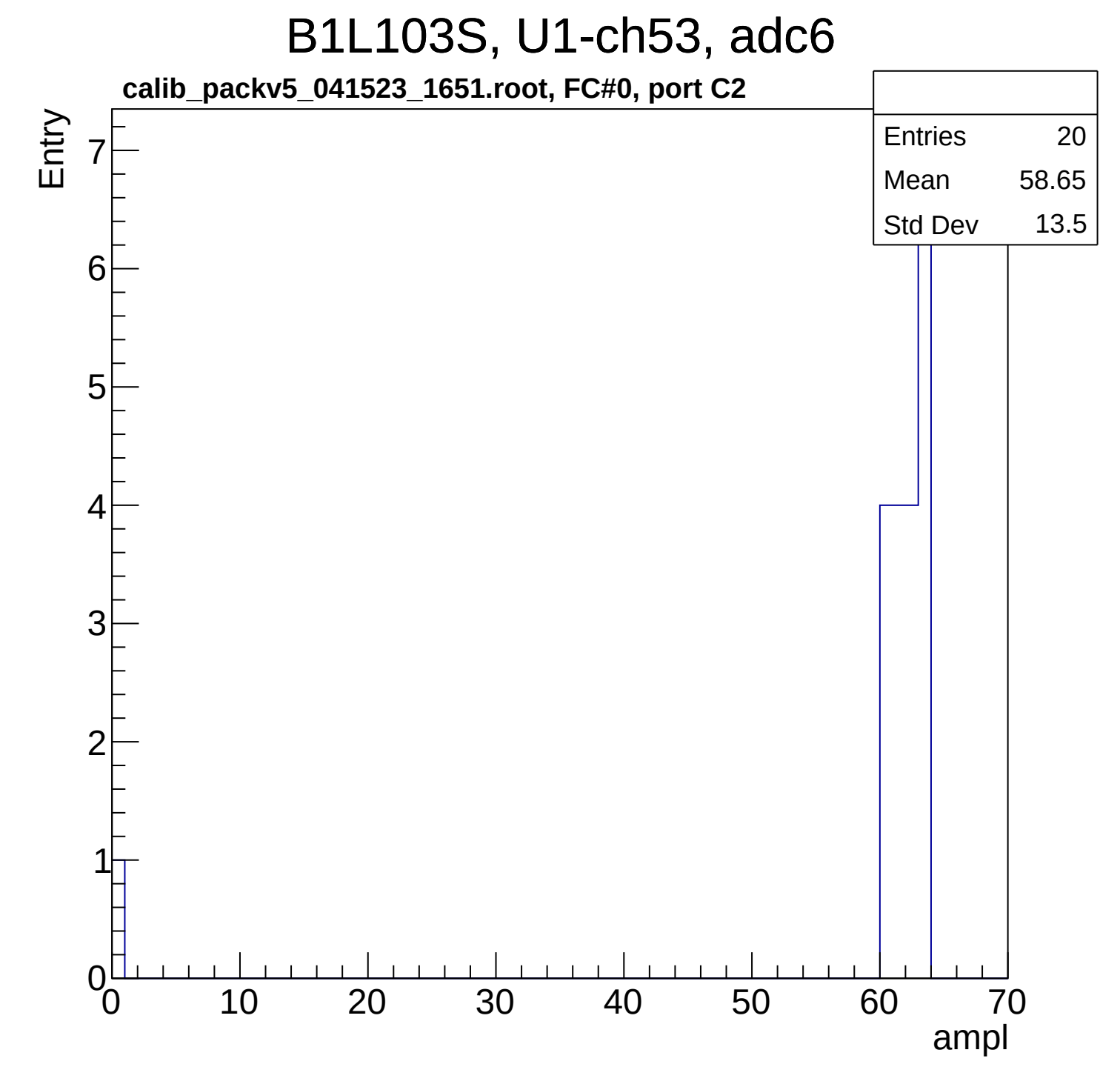
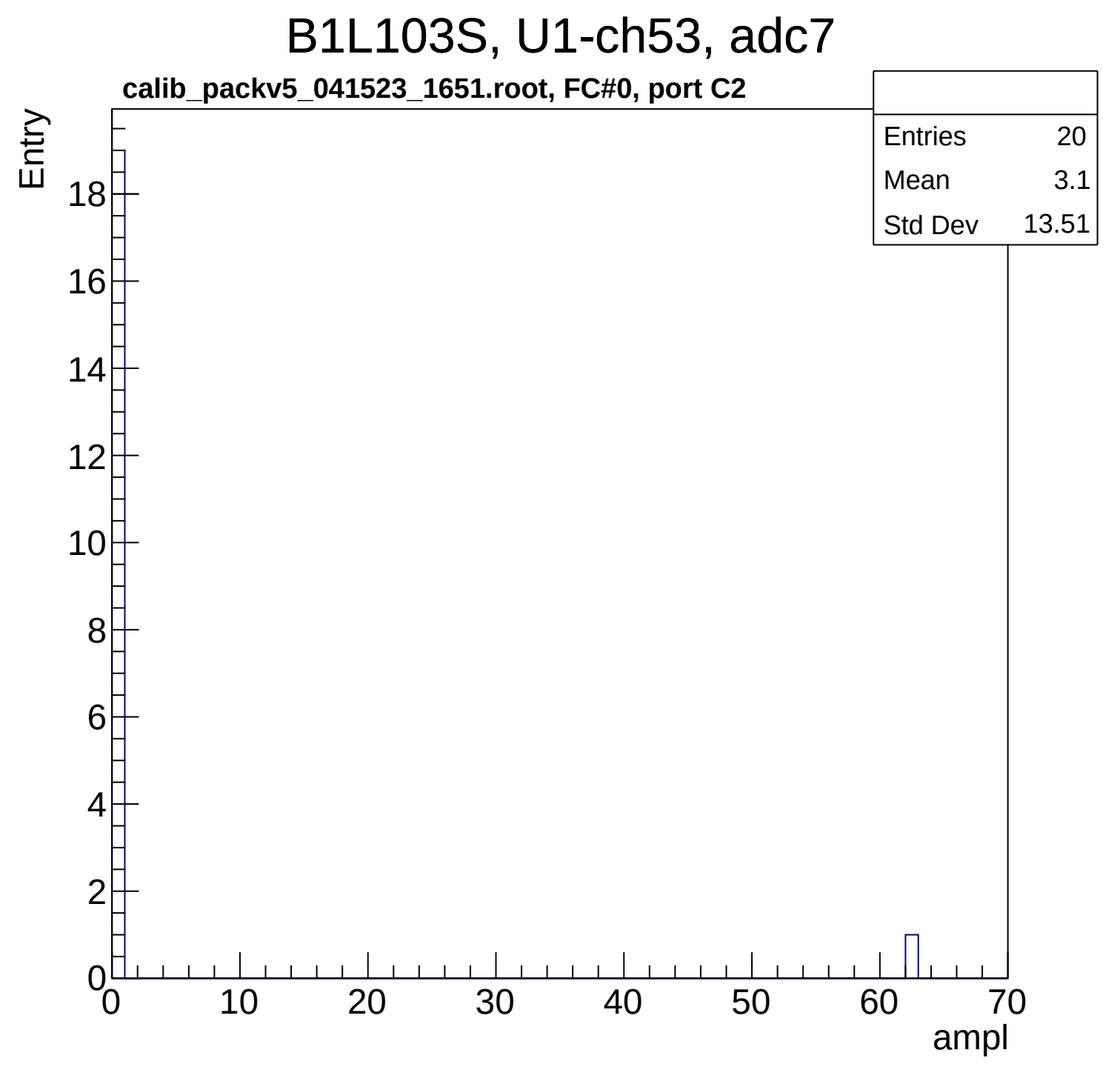

B1L103S, U1-ch53, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 58.65
Std Dev 13.5
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U1-ch53, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.1
Std Dev 13.51
Entry
0
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6
8
10
12
14
16
18
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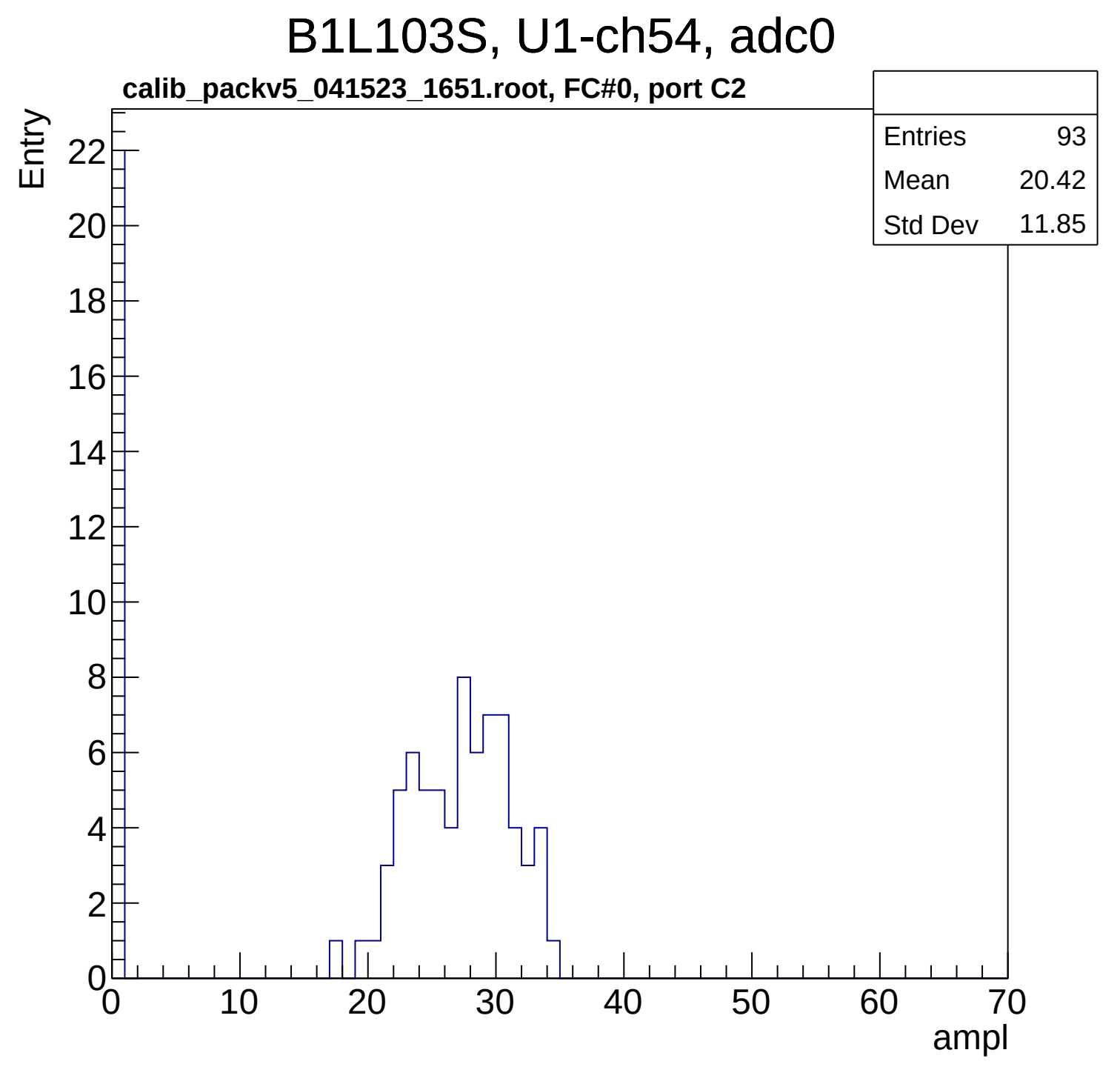
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch54, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 93
Mean 20.42
Std Dev 11.85
Entry
ampl
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4
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8
10
12
14
16
18
20
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0
10
20
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60
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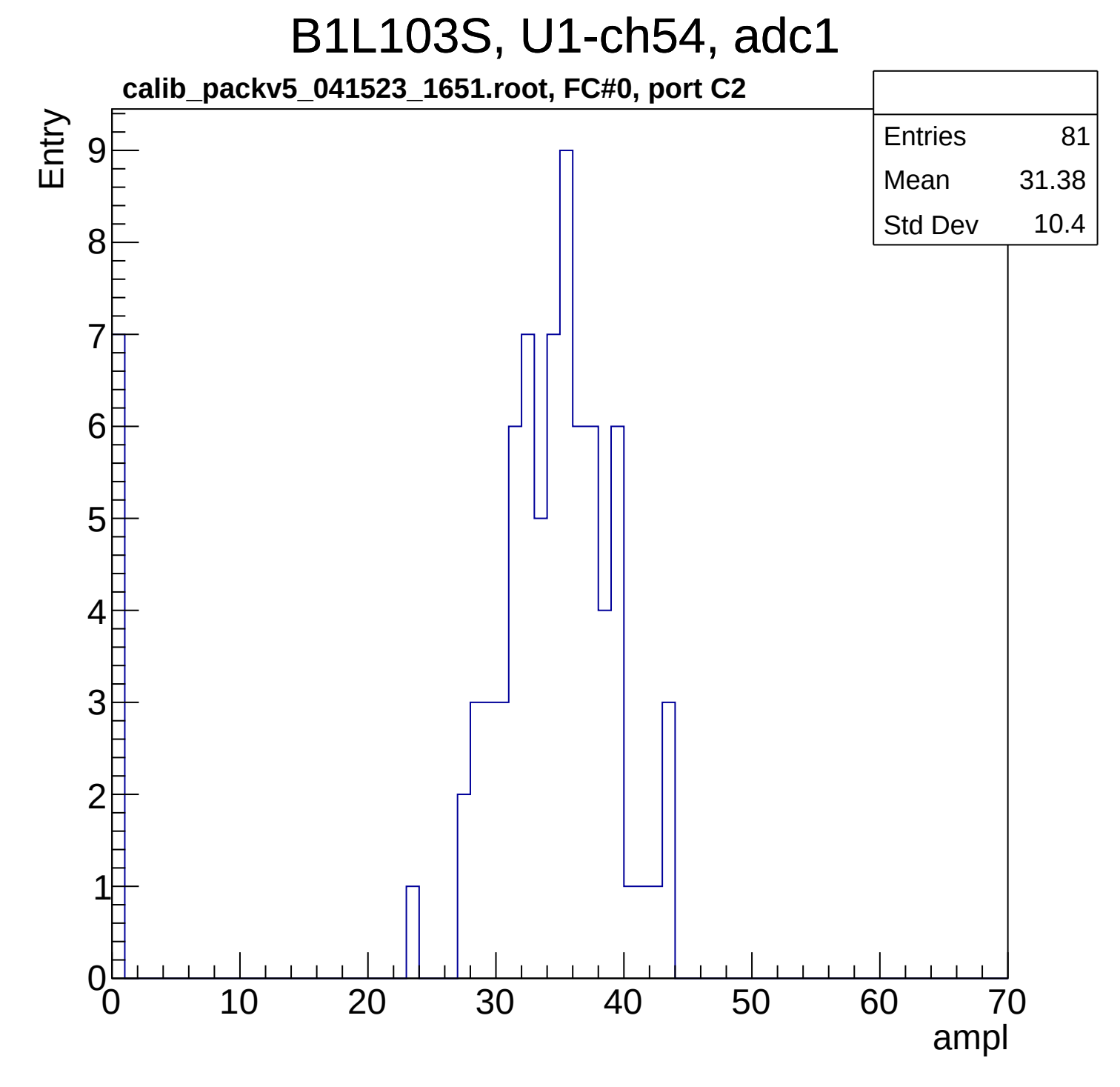
B1L103S, U1-ch54, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 31.38
Std Dev 10.4
Entry
ampl
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2
3
4
5
6
7
8
9
0
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60
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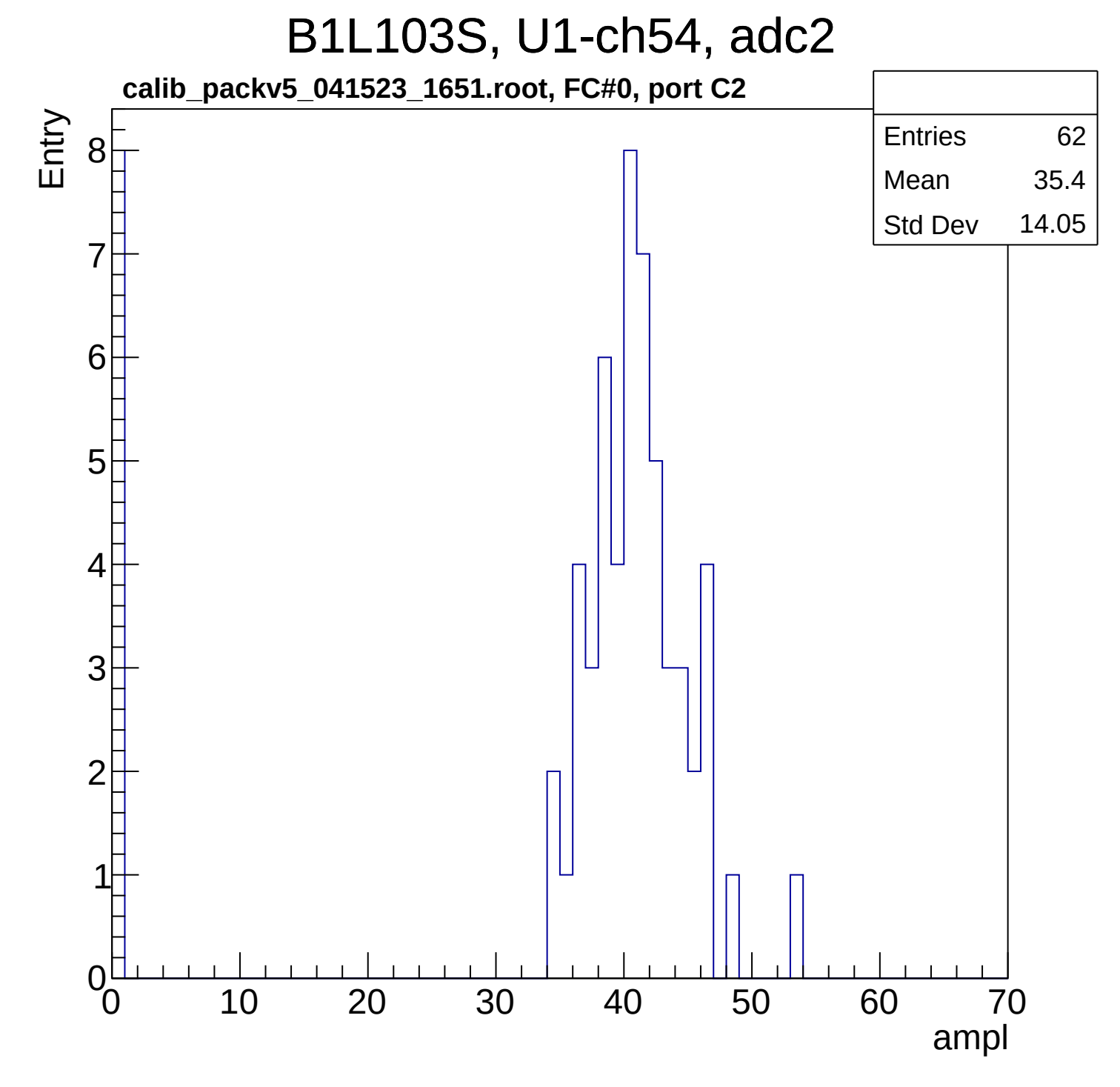
B1L103S, U1-ch54, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 35.4
Std Dev 14.05
Entry
ampl
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1
2
3
4
5
6
7
8
0
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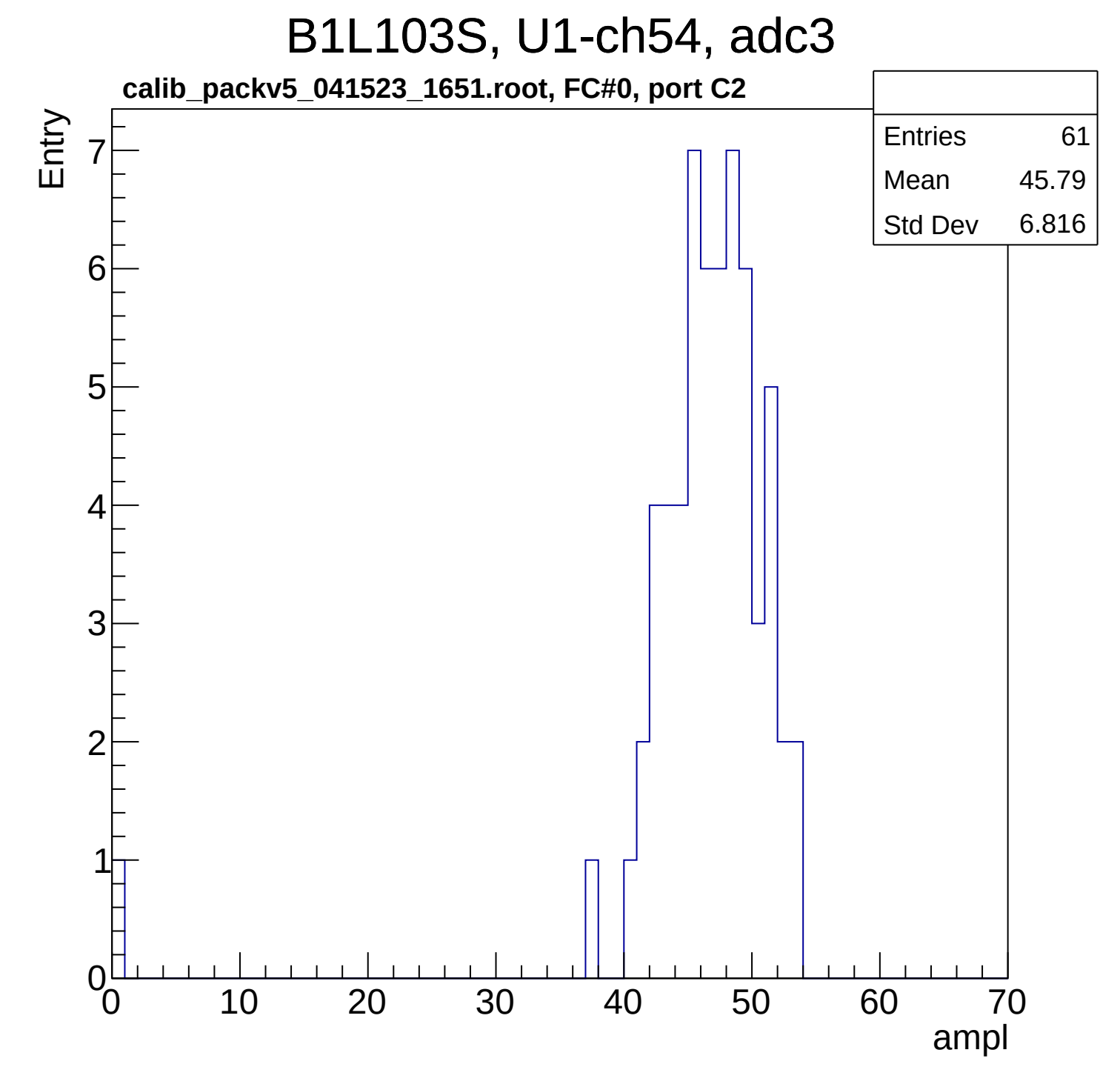
60
70


B1L103S, U1-ch54, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 45.79
Std Dev 6.816
Entry
ampl
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6
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0
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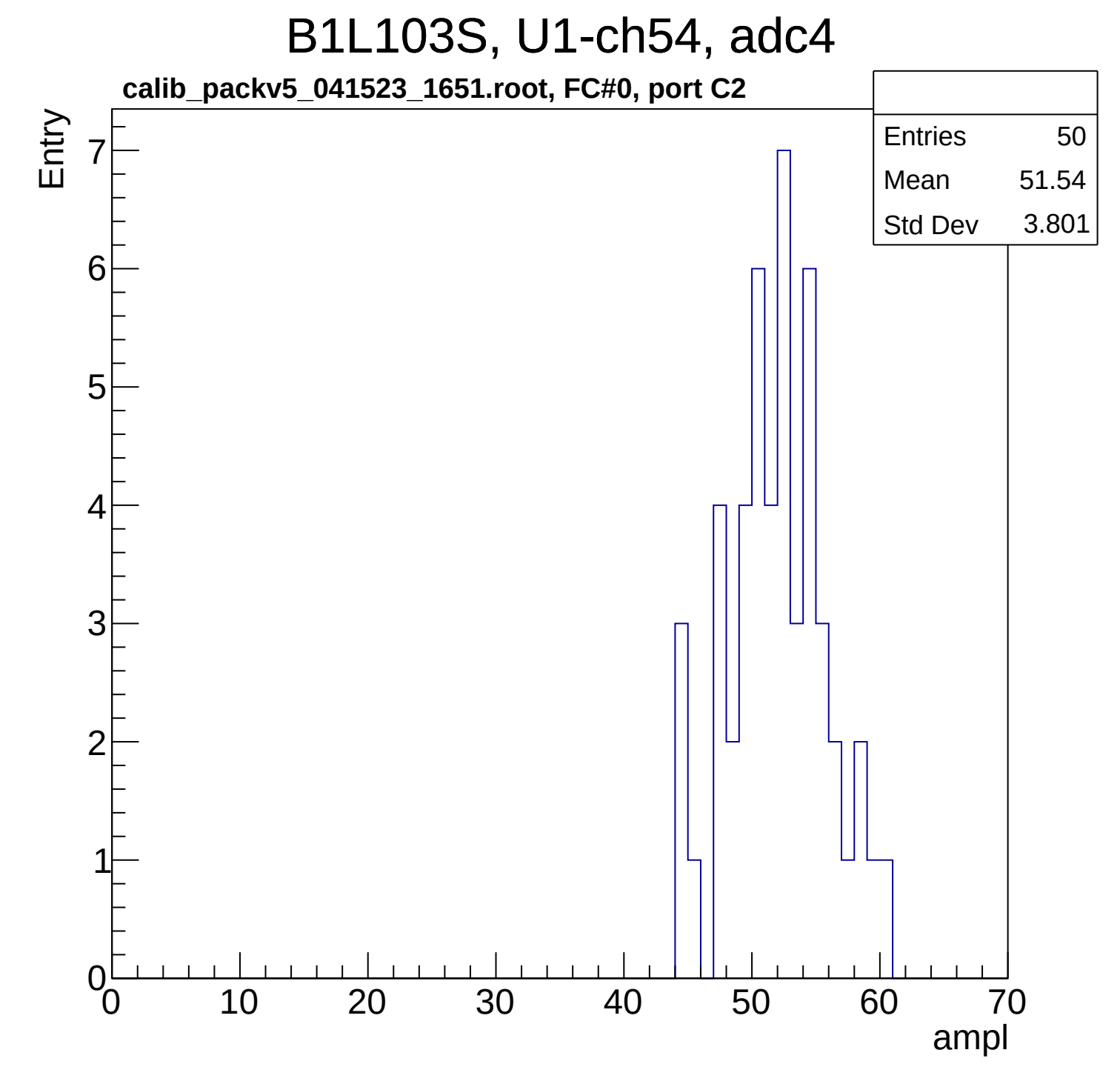
B1L103S, U1-ch54, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 51.54
Std Dev 3.801
Entry
ampl
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0
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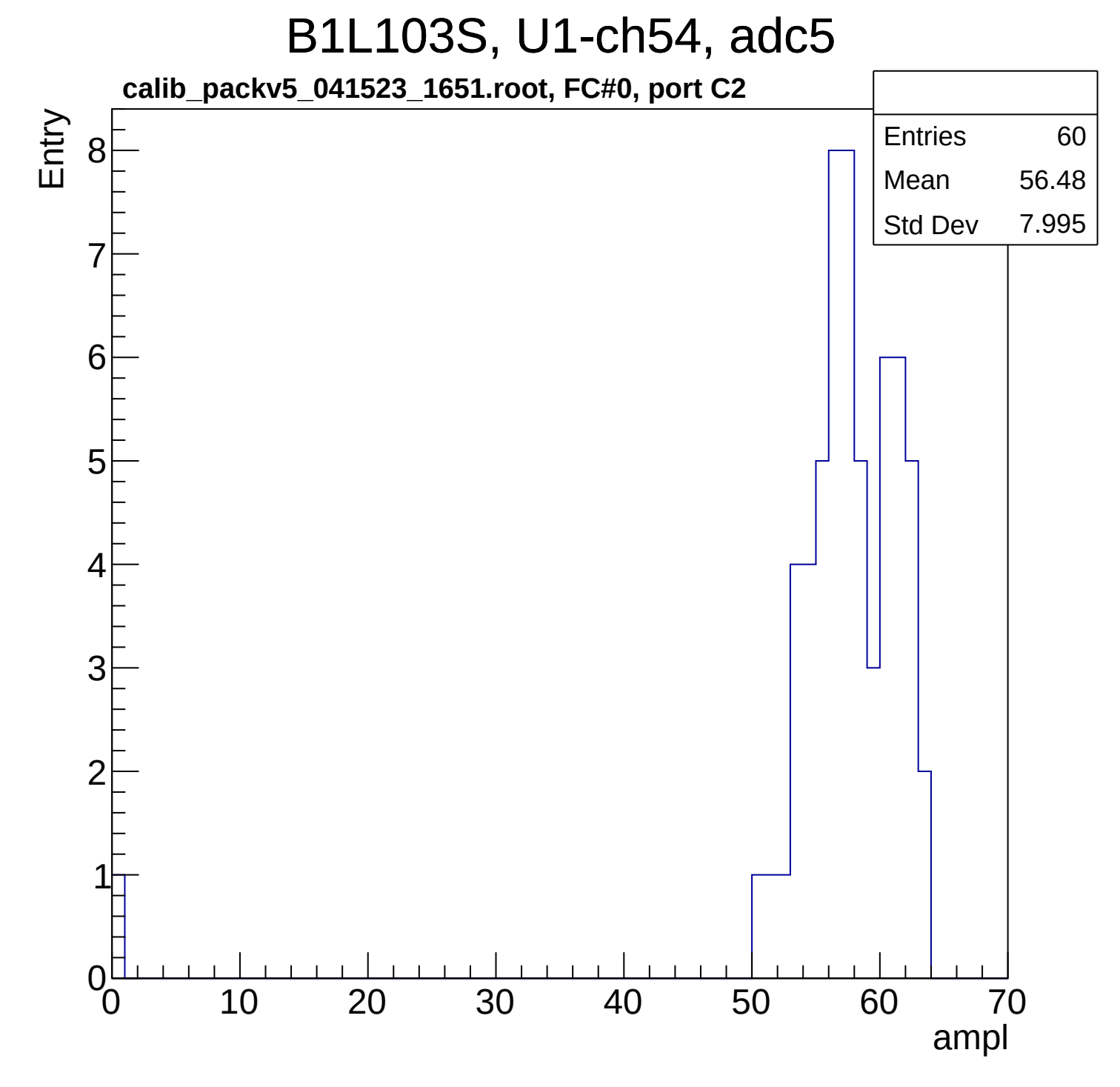
B1L103S, U1-ch54, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 56.48
Std Dev 7.995
Entry
ampl
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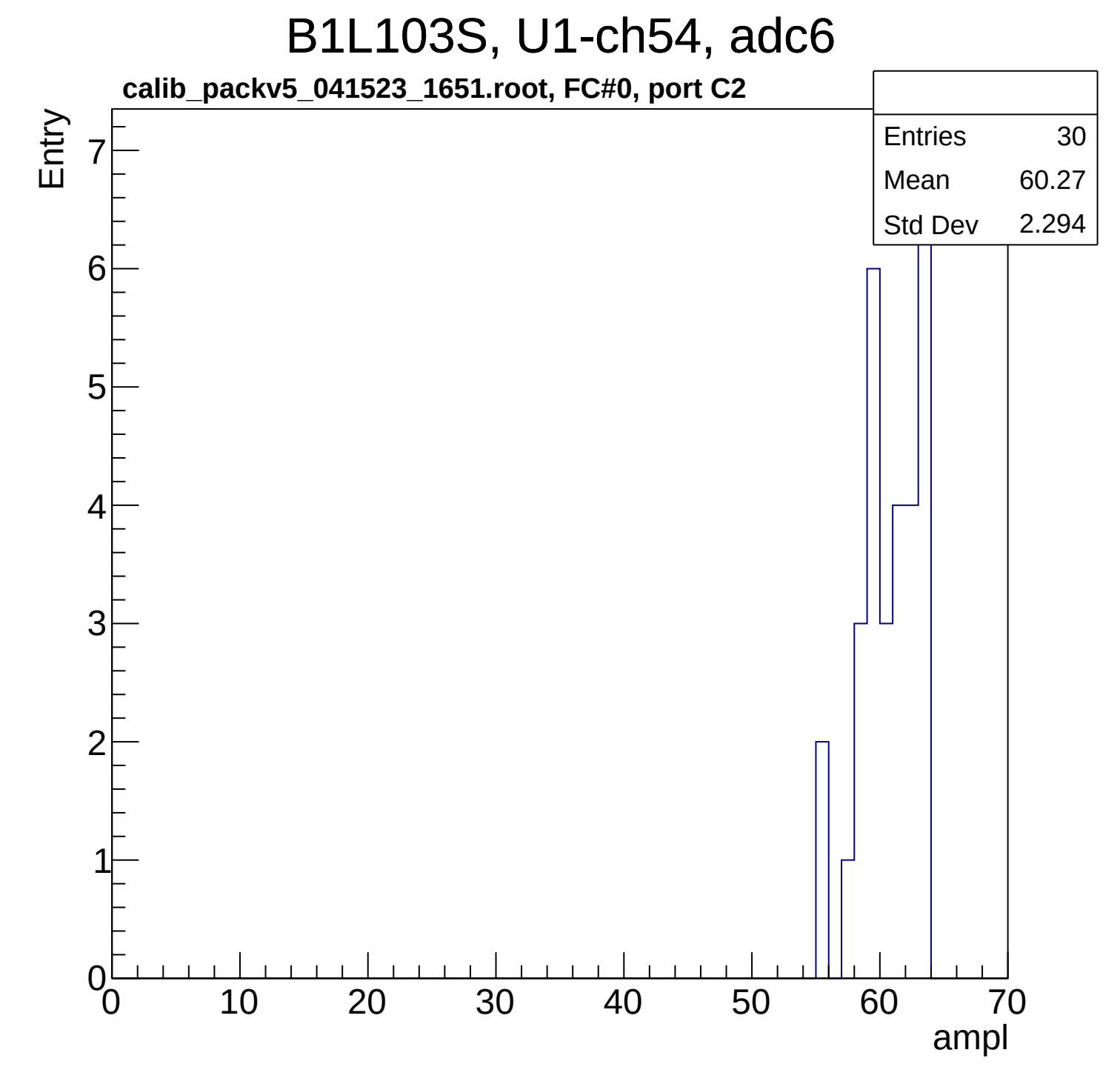
B1L103S, U1-ch54, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 30
Mean 60.27
Std Dev 2.294
Entry
ampl
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1
2
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4
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6
7
0
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20
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60
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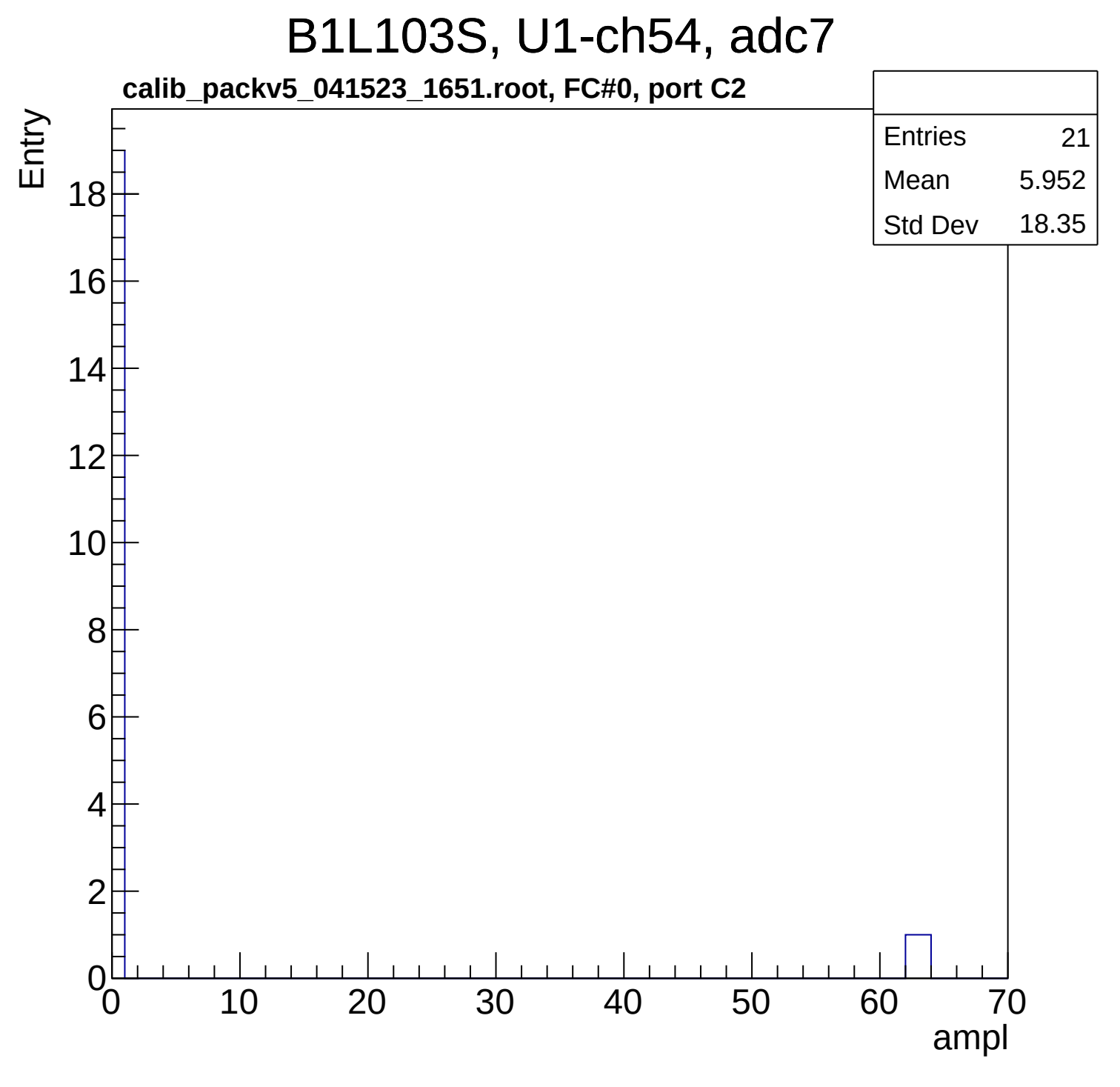
B1L103S, U1-ch54, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 5.952
Std Dev 18.35
Entry
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6
8
10
12
14
16
18
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10
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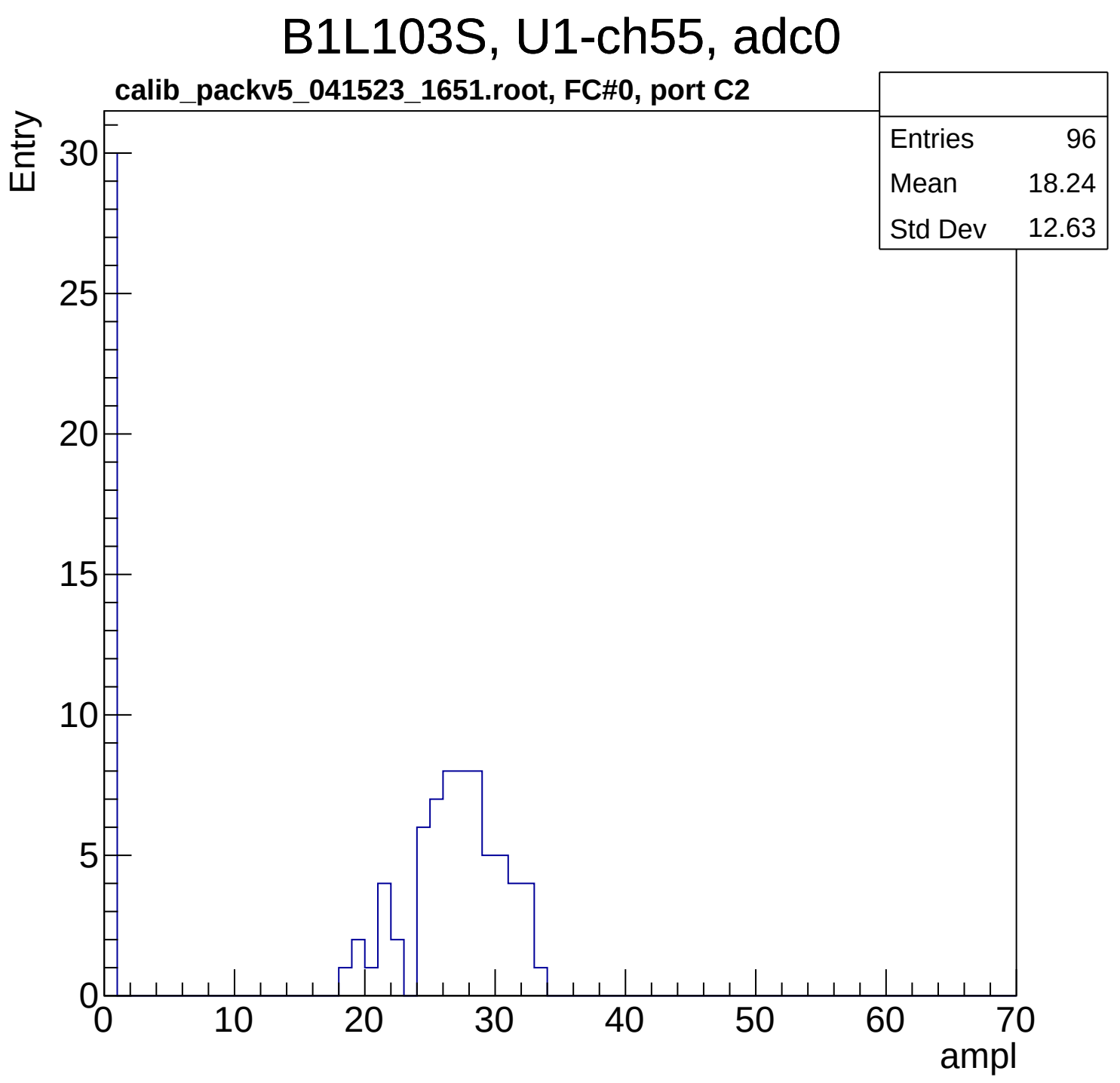
70
ampl


B1L103S, U1-ch55, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 96
Mean 18.24
Std Dev 12.63
Entry
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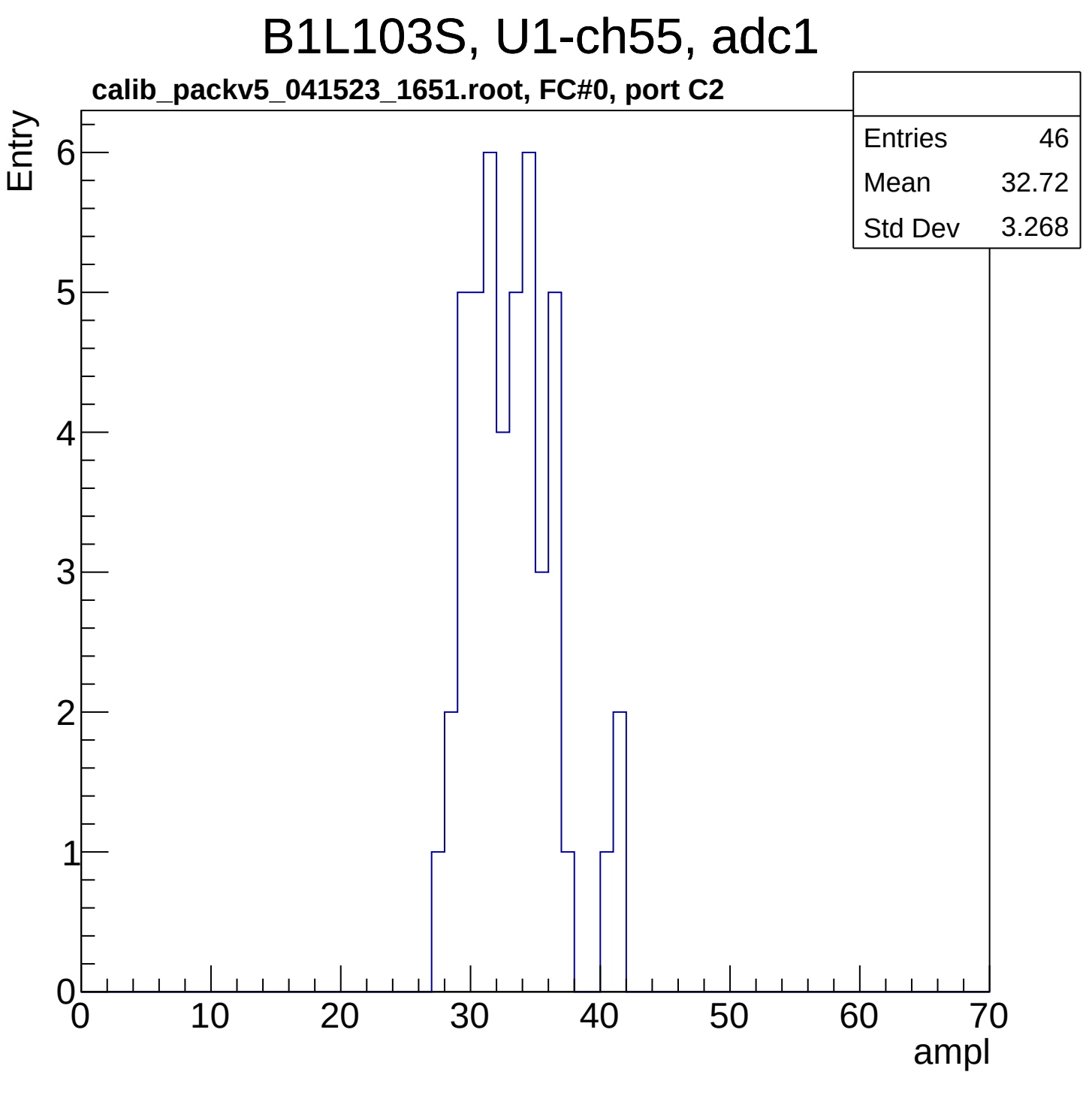
60
70
ampl


B1L103S, U1-ch55, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 32.72
Std Dev 3.268
Entry
ampl
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3
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60
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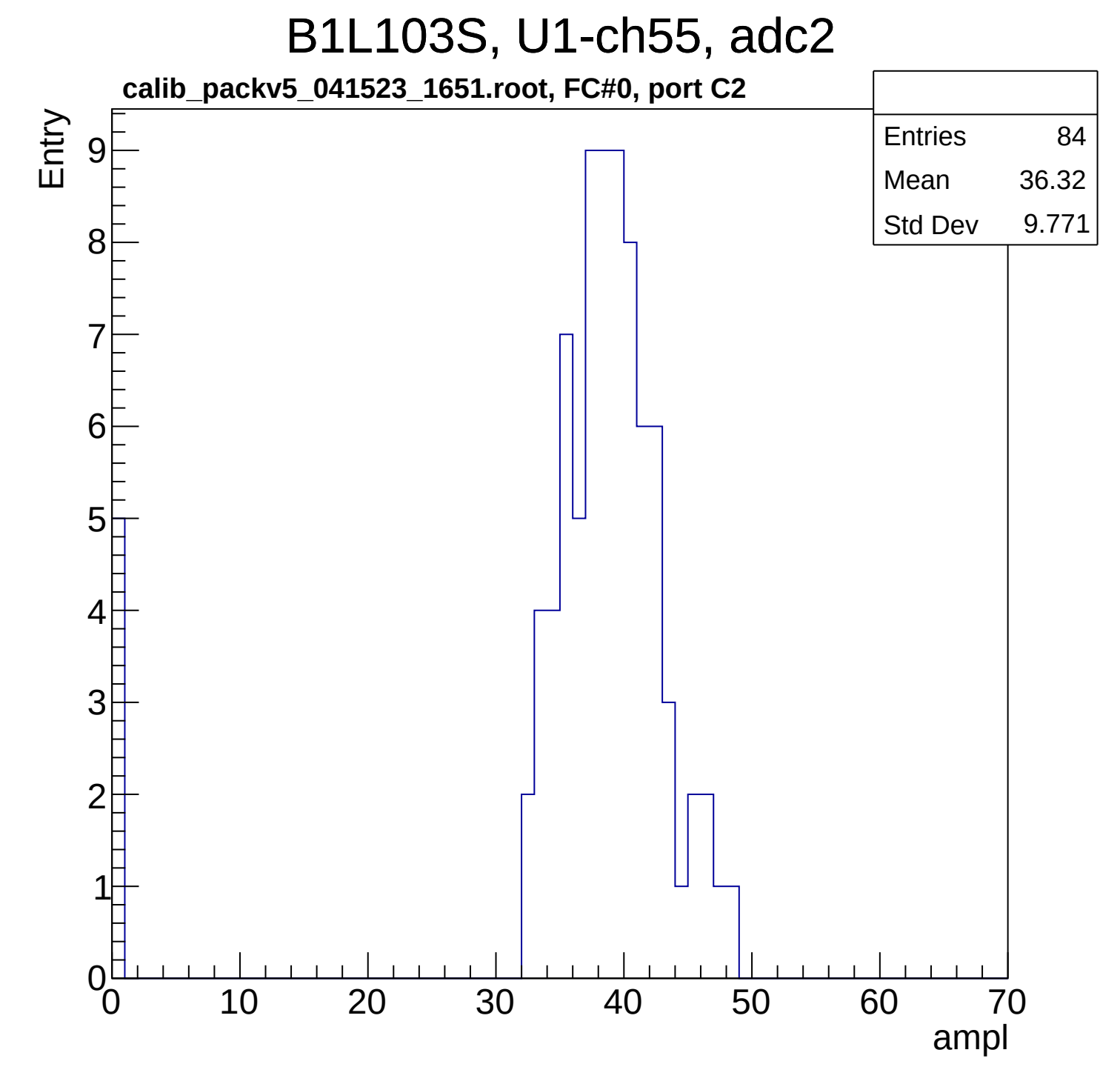
B1L103S, U1-ch55, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 36.32
Std Dev 9.771
Entry
ampl
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2
3
4
5
6
7
8
9
0
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60
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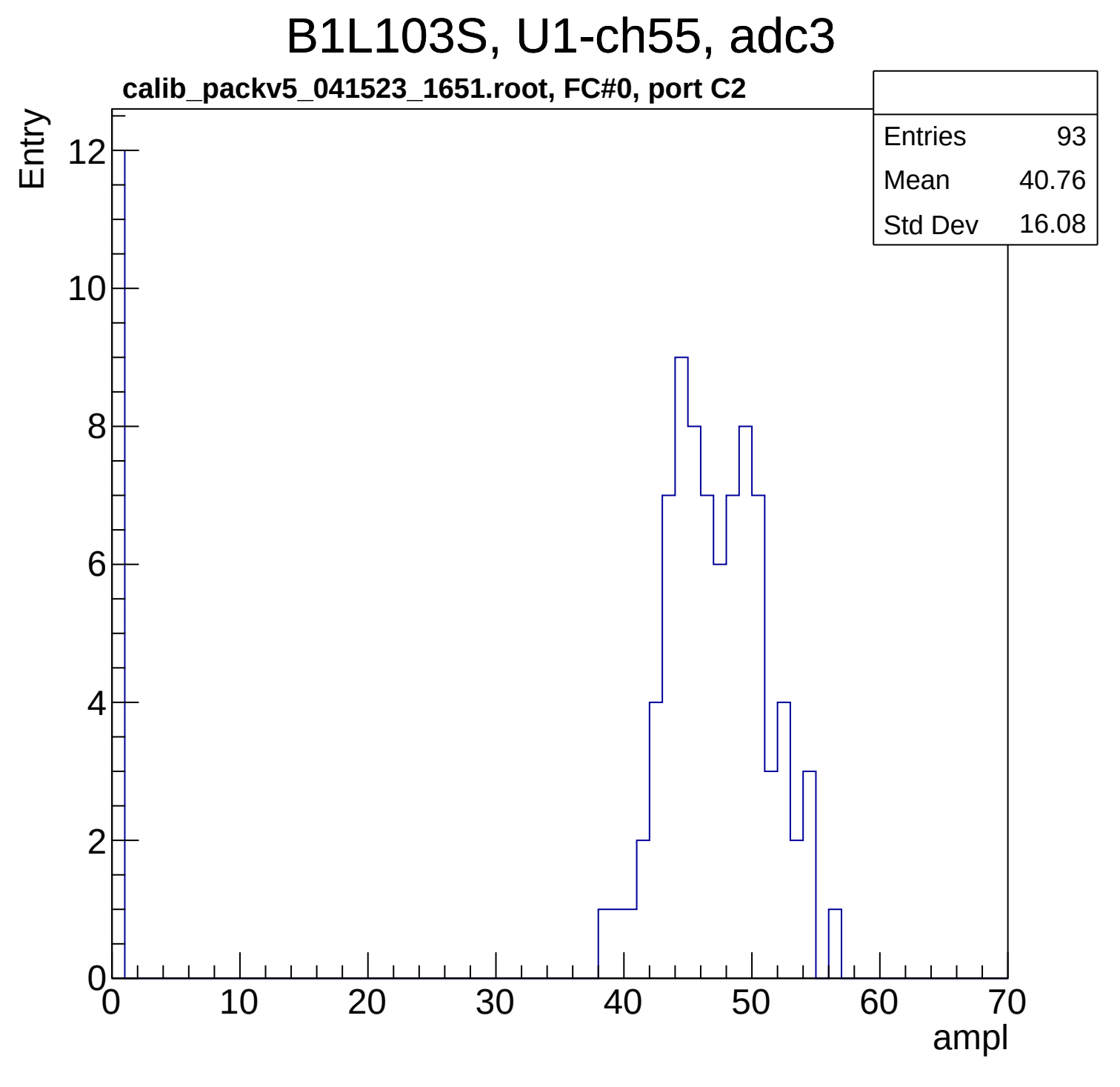
B1L103S, U1-ch55, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 93
Mean 40.76
Std Dev 16.08
Entry
ampl
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6
8
10
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0
10
20
30
40
50
60
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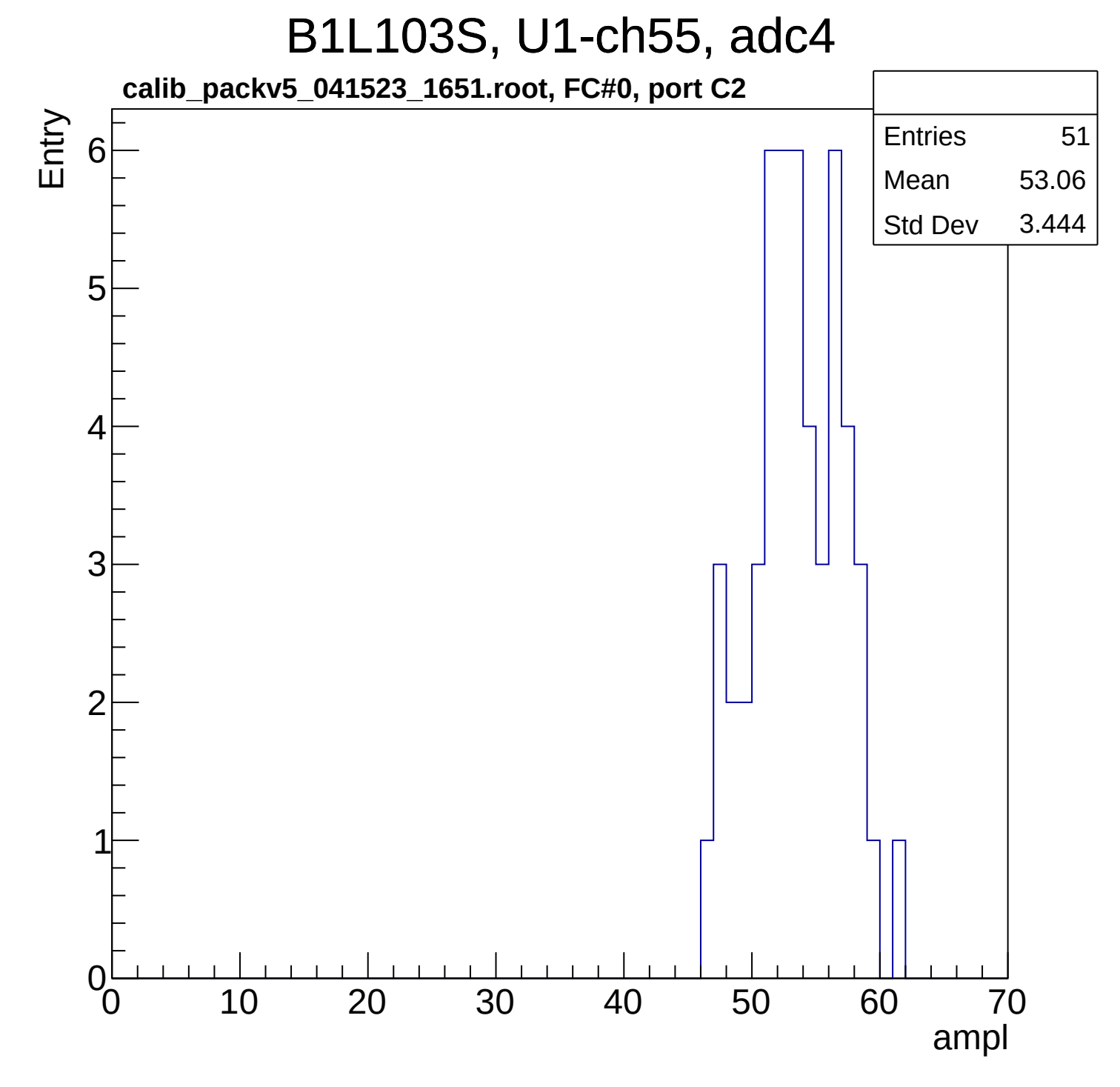
B1L103S, U1-ch55, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 53.06
Std Dev 3.444
Entry
ampl
0
1
2
3
4
5
6
0
10
20
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40
50
60
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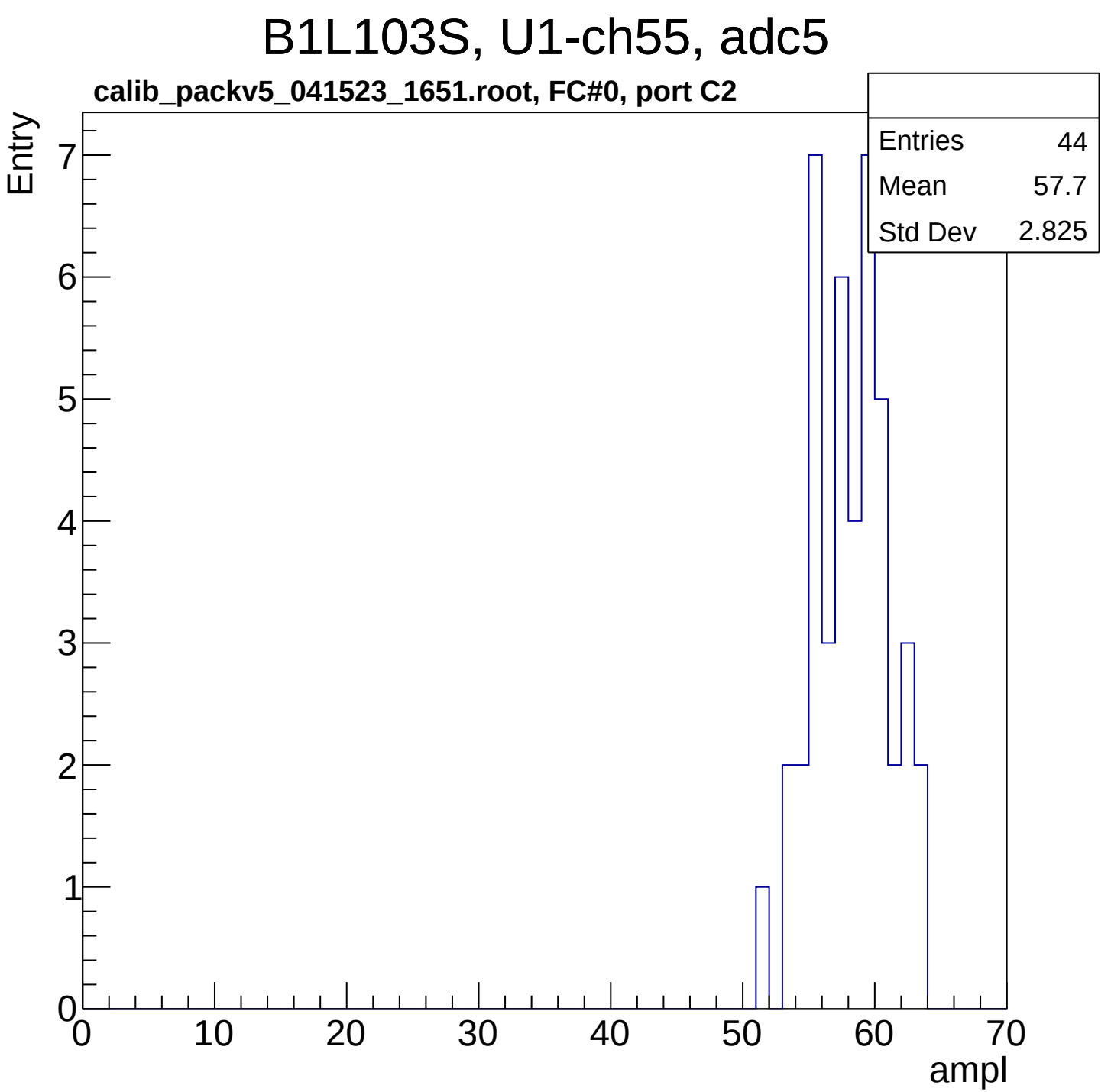
B1L103S, U1-ch55, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 57.7
Std Dev 2.825
Entry
ampl
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1
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3
4
5
6
7
0
10
20
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40
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60
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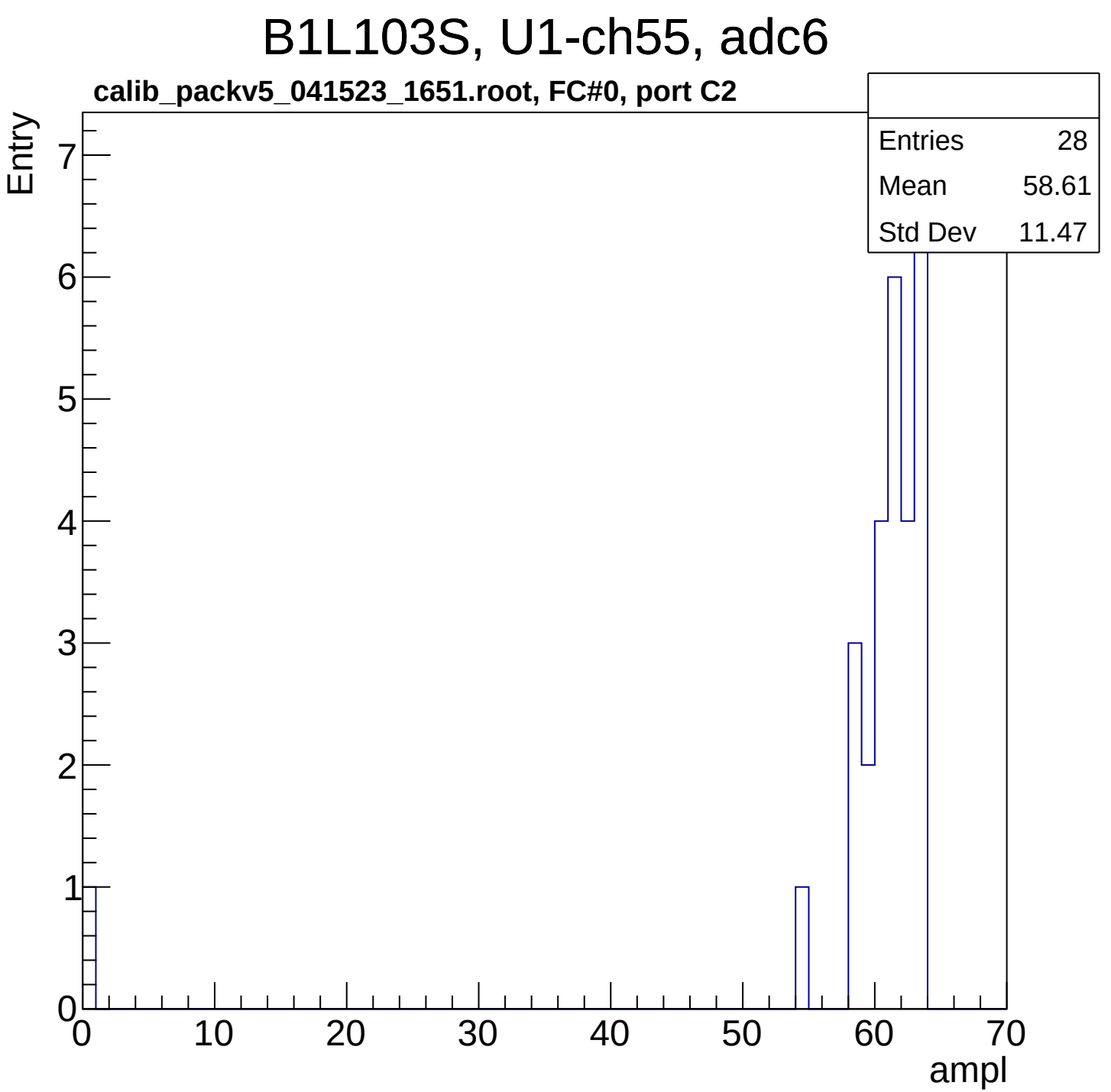
B1L103S, U1-ch55, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 28
Mean 58.61
Std Dev 11.47
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
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40
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60
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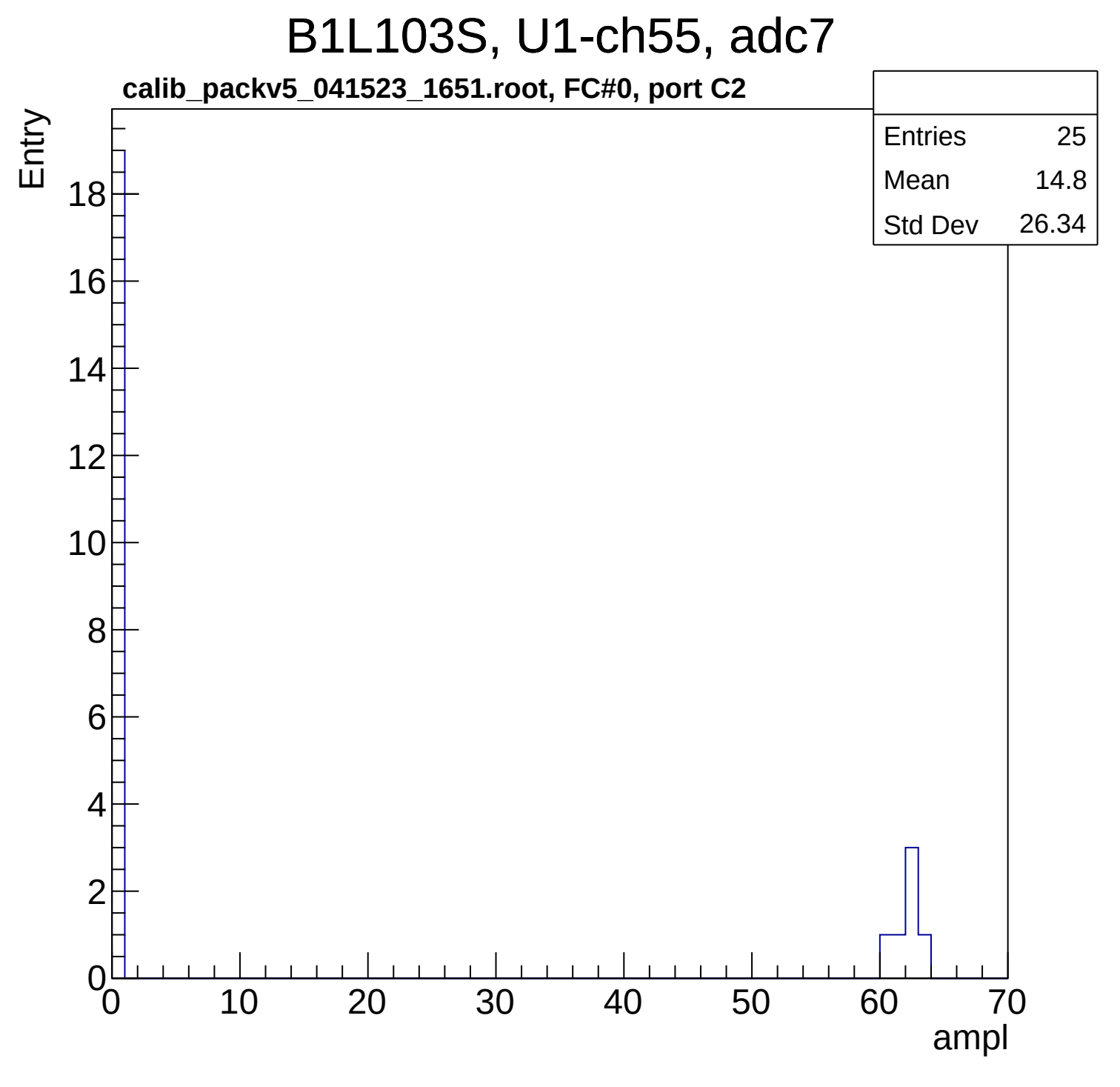
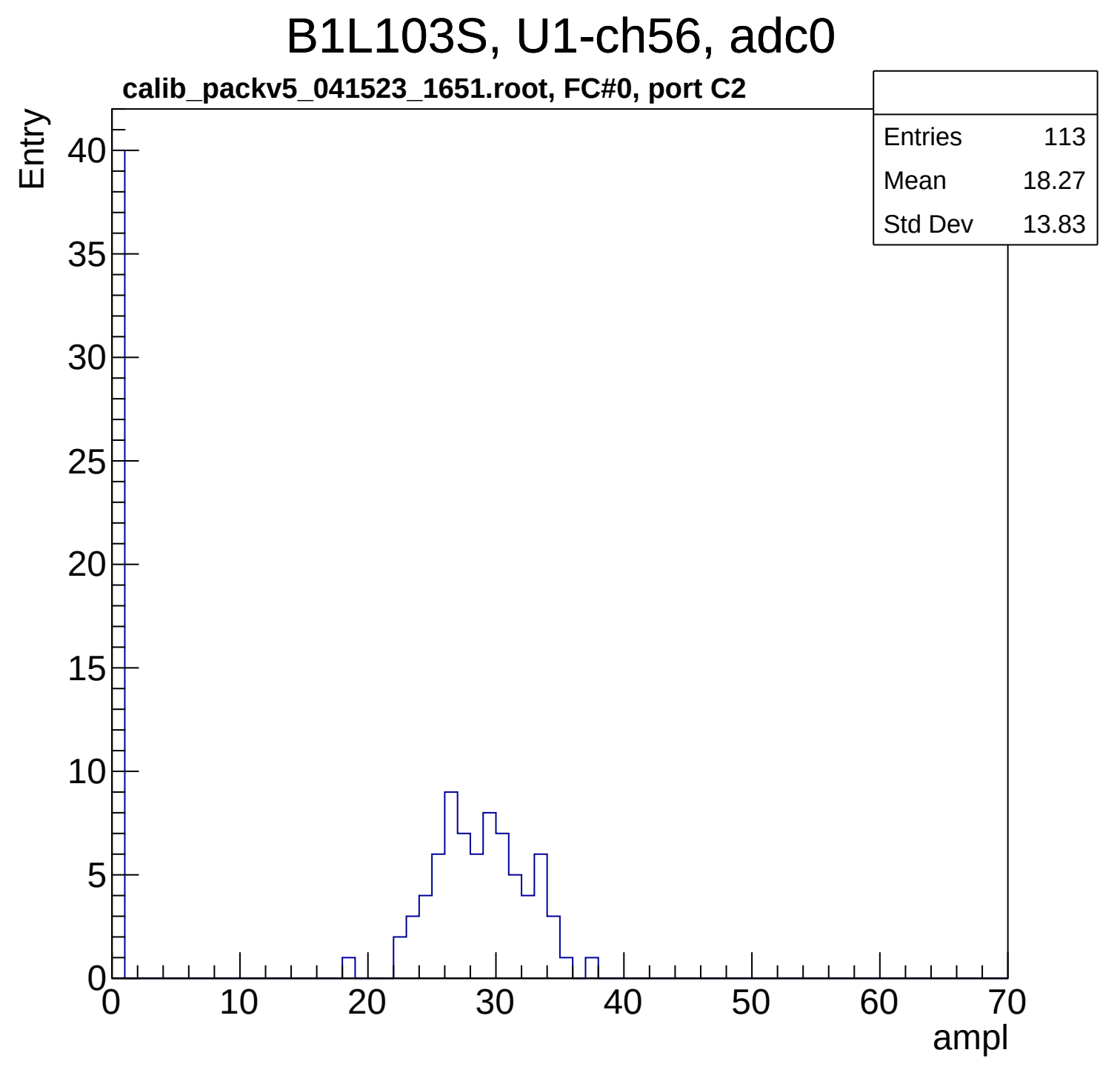

B1L103S, U1-ch55, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 25
Mean 14.8
Std Dev 26.34
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch56, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 113
Mean 18.27
Std Dev 13.83
Entry
ampl
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5
10
15
20
25
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35
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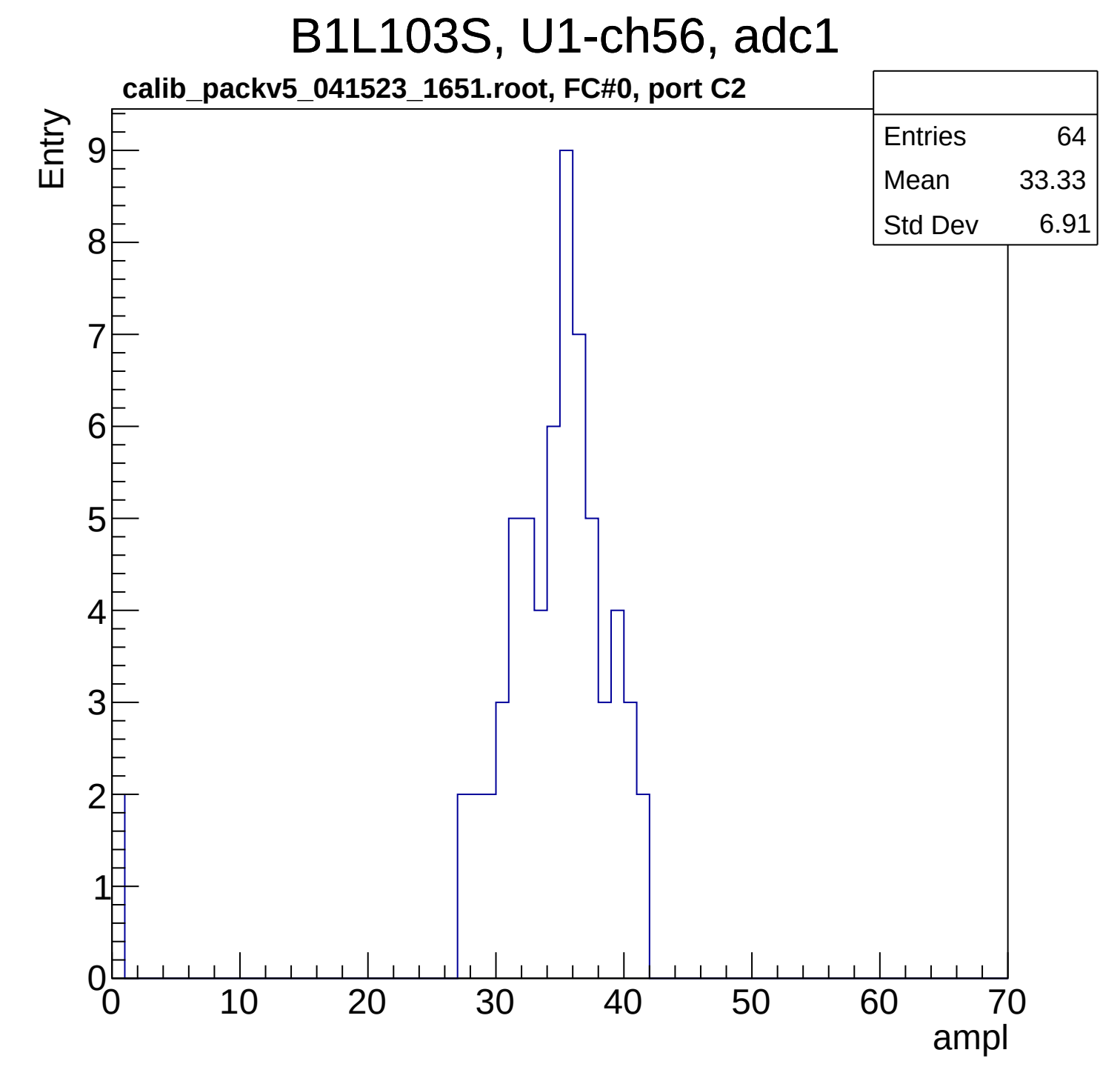
B1L103S, U1-ch56, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 33.33
Std Dev 6.91
Entry
ampl
0
1
2
3
4
5
6
7
8
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0
10
20
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40
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60
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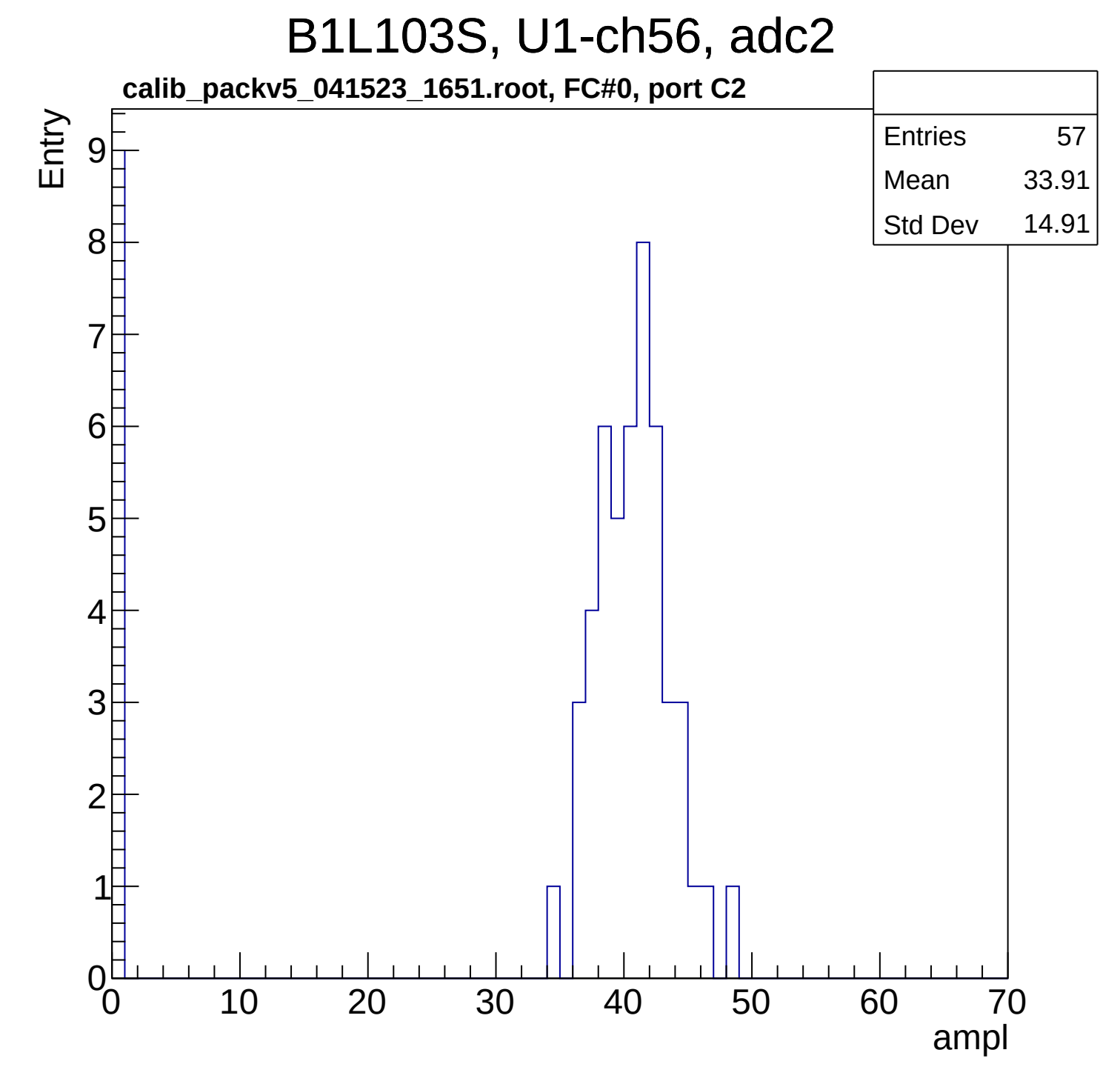
B1L103S, U1-ch56, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 33.91
Std Dev 14.91
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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60
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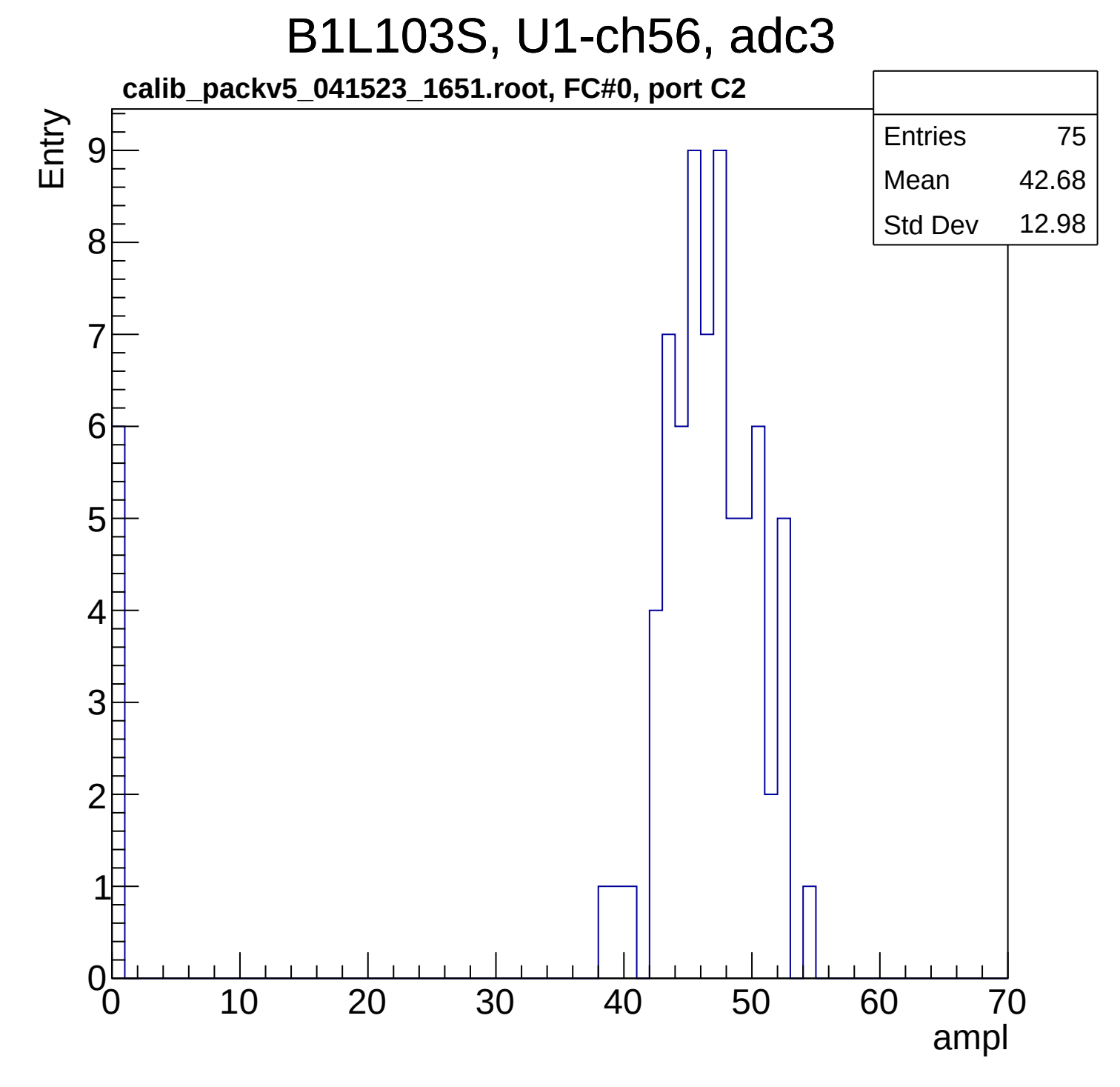
B1L103S, U1-ch56, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 42.68
Std Dev 12.98
Entry
ampl
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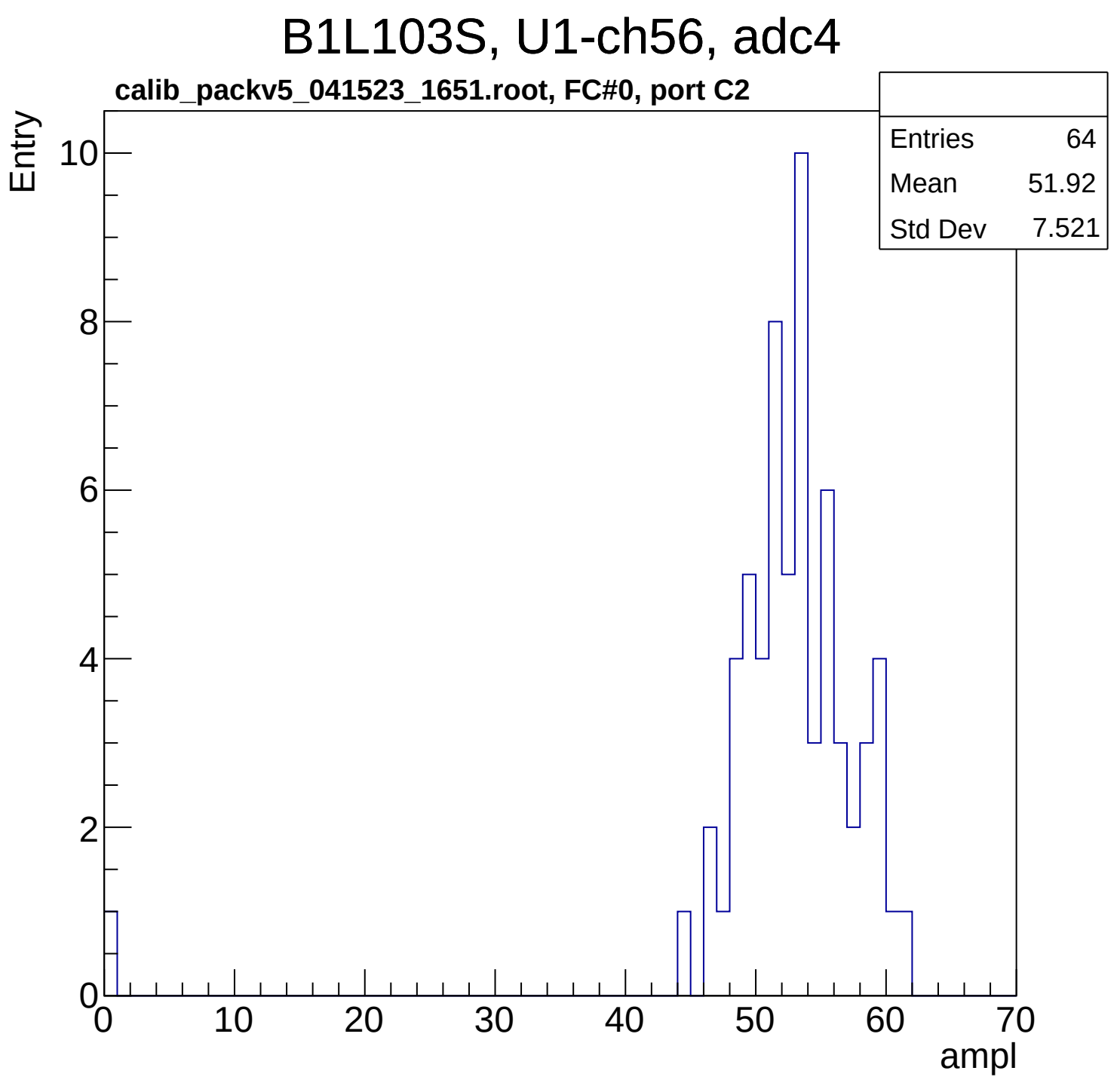
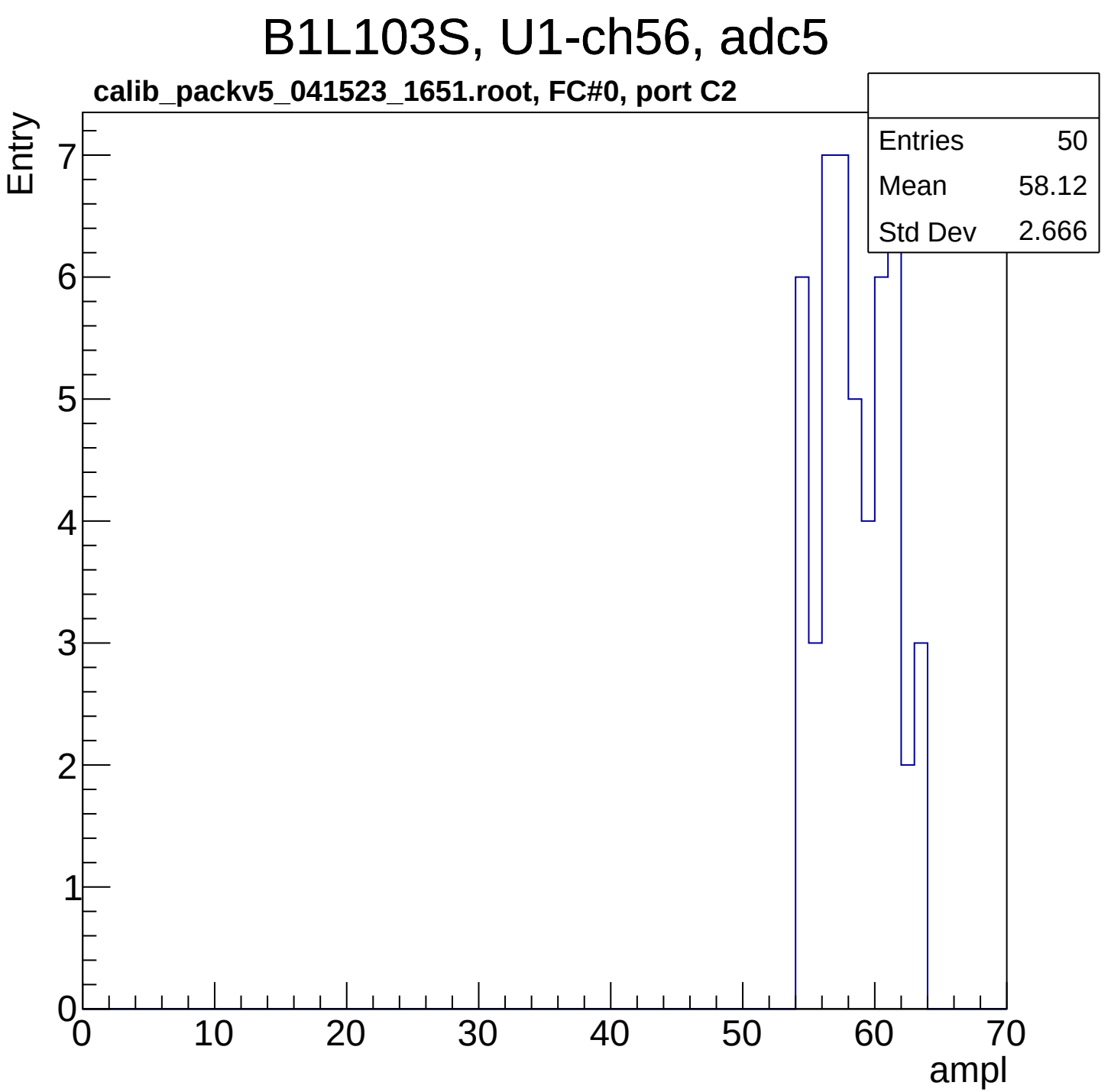
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U1-ch56, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 51.92
Std Dev 7.521
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U1-ch56, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 58.12
Std Dev 2.666
Entry
ampl
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1
2
3
4
5
6
7
0
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20
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40
50
60
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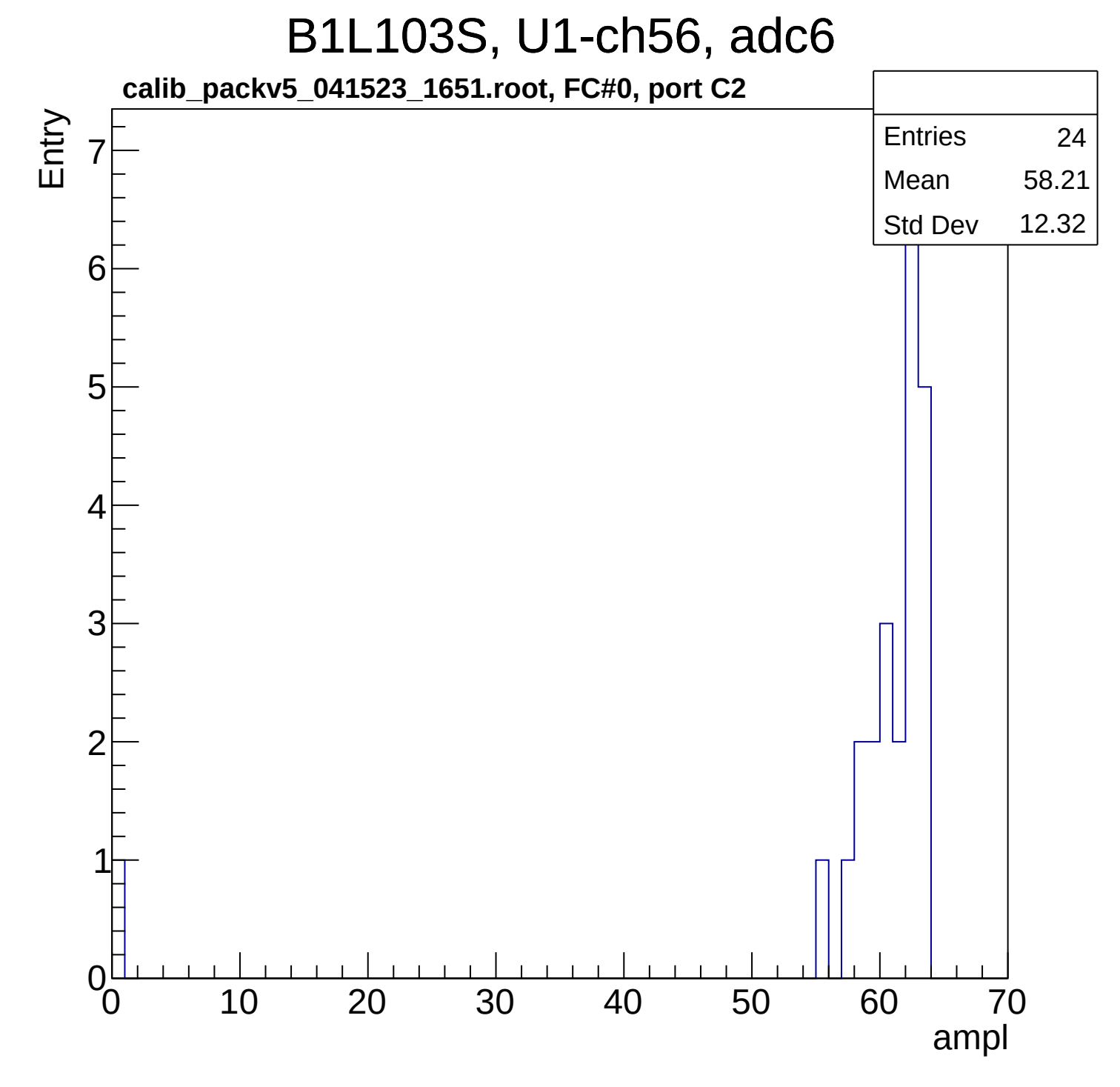
B1L103S, U1-ch56, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 24
Mean 58.21
Std Dev 12.32
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
30
40
50
60
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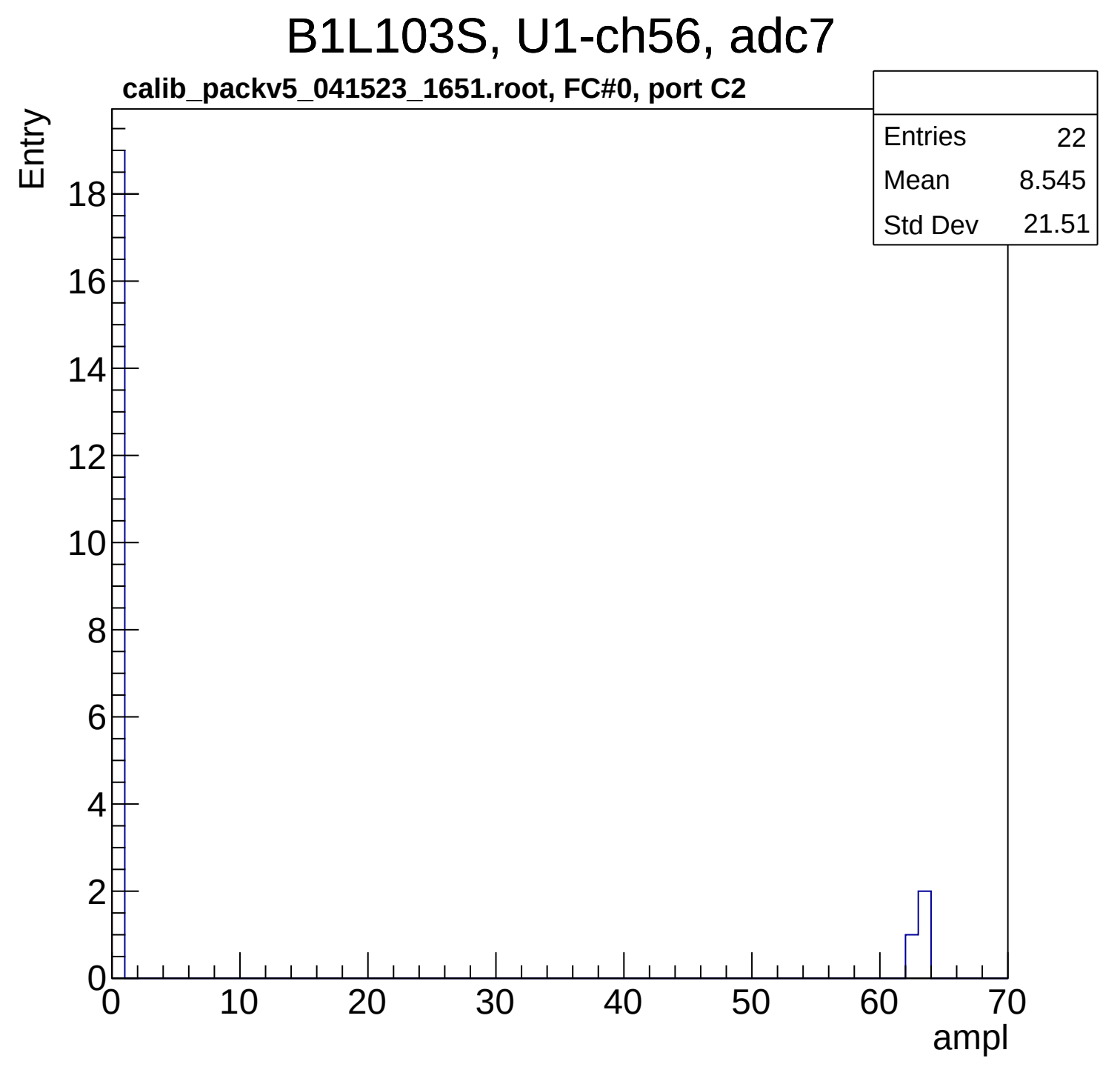
B1L103S, U1-ch56, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 8.545
Std Dev 21.51
Entry
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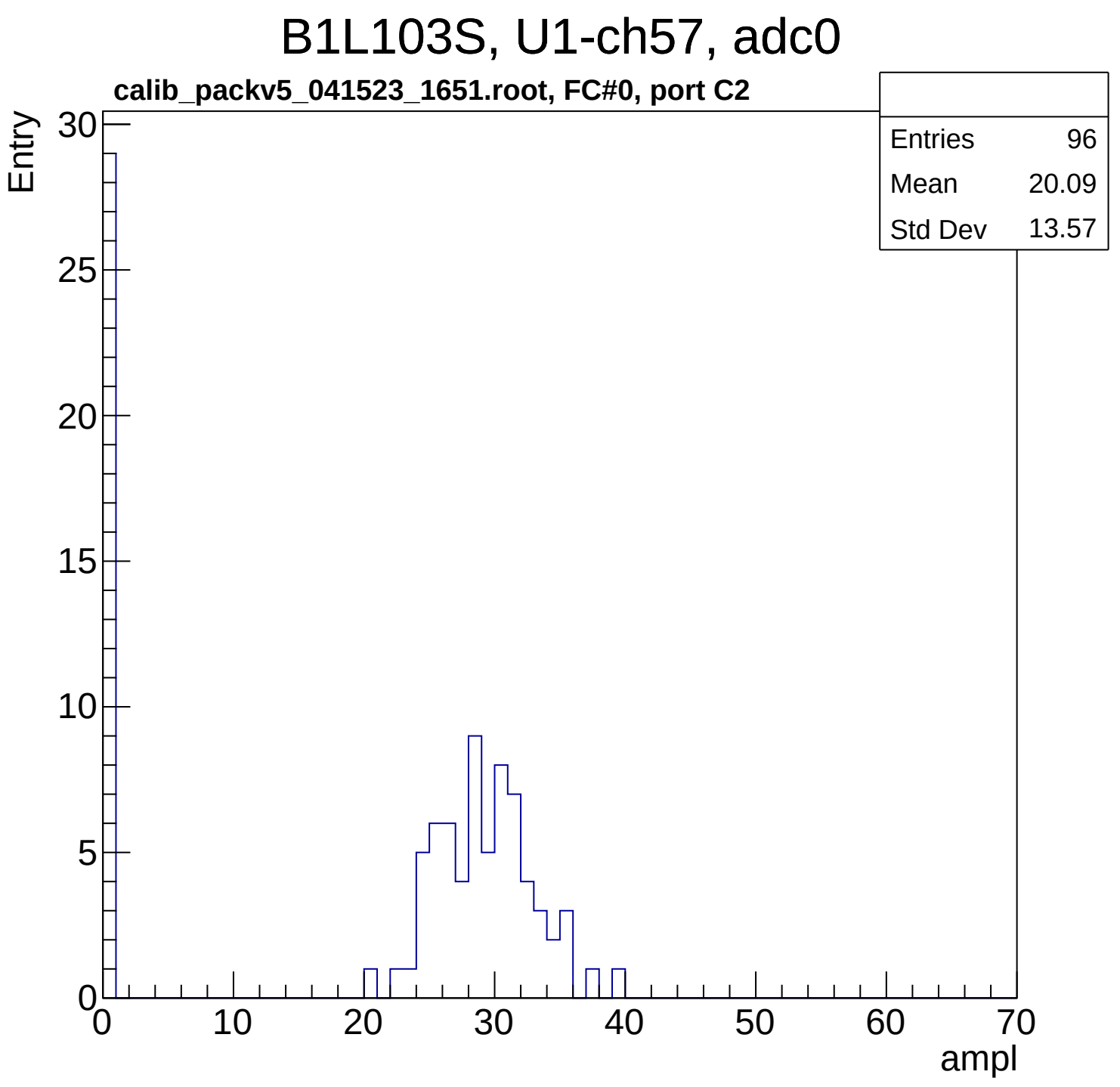
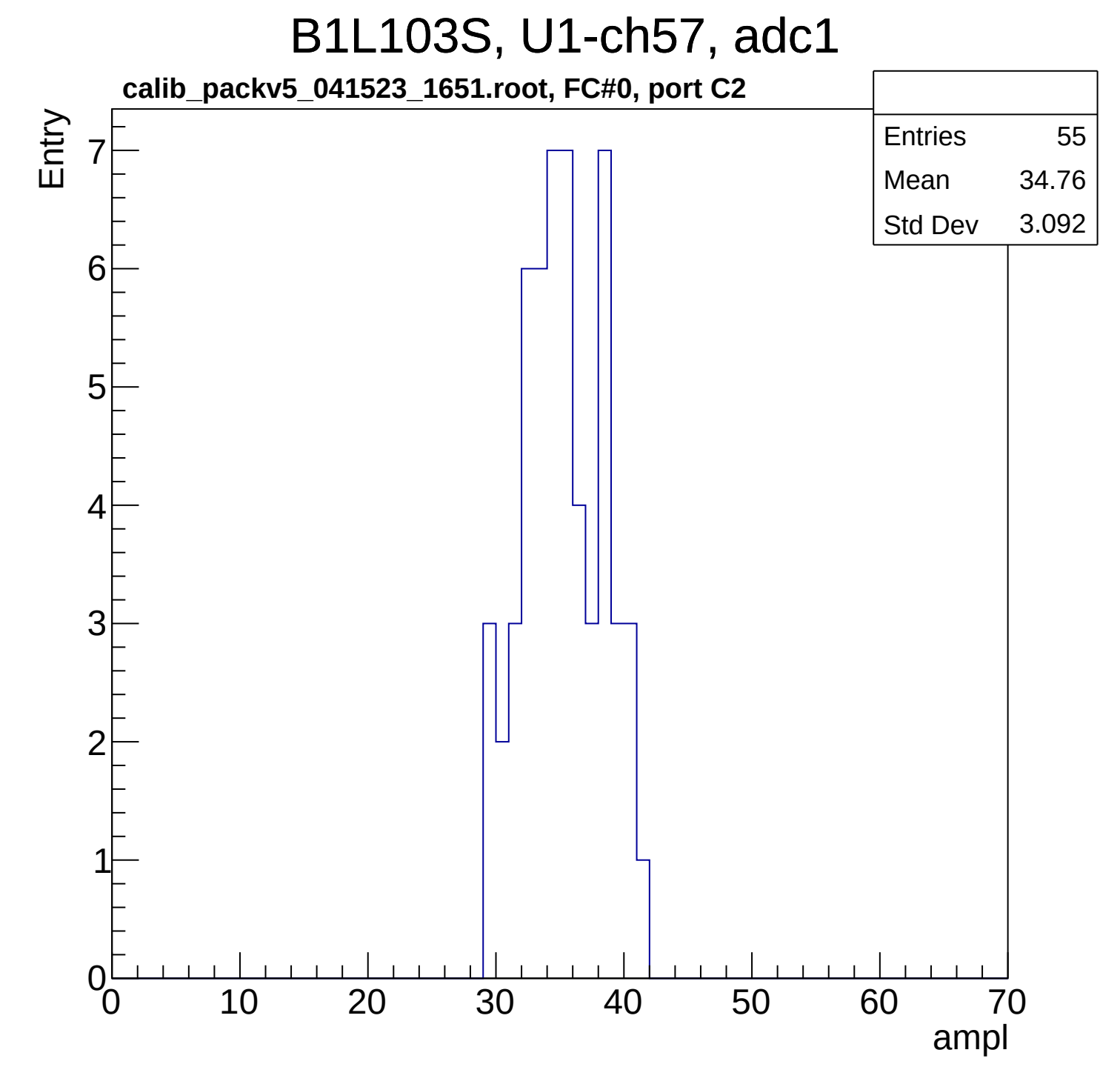
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch57, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 96
Mean 20.09
Std Dev 13.57
Entry
0
5
10
15
20
25
30
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch57, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 34.76
Std Dev 3.092
Entry
ampl
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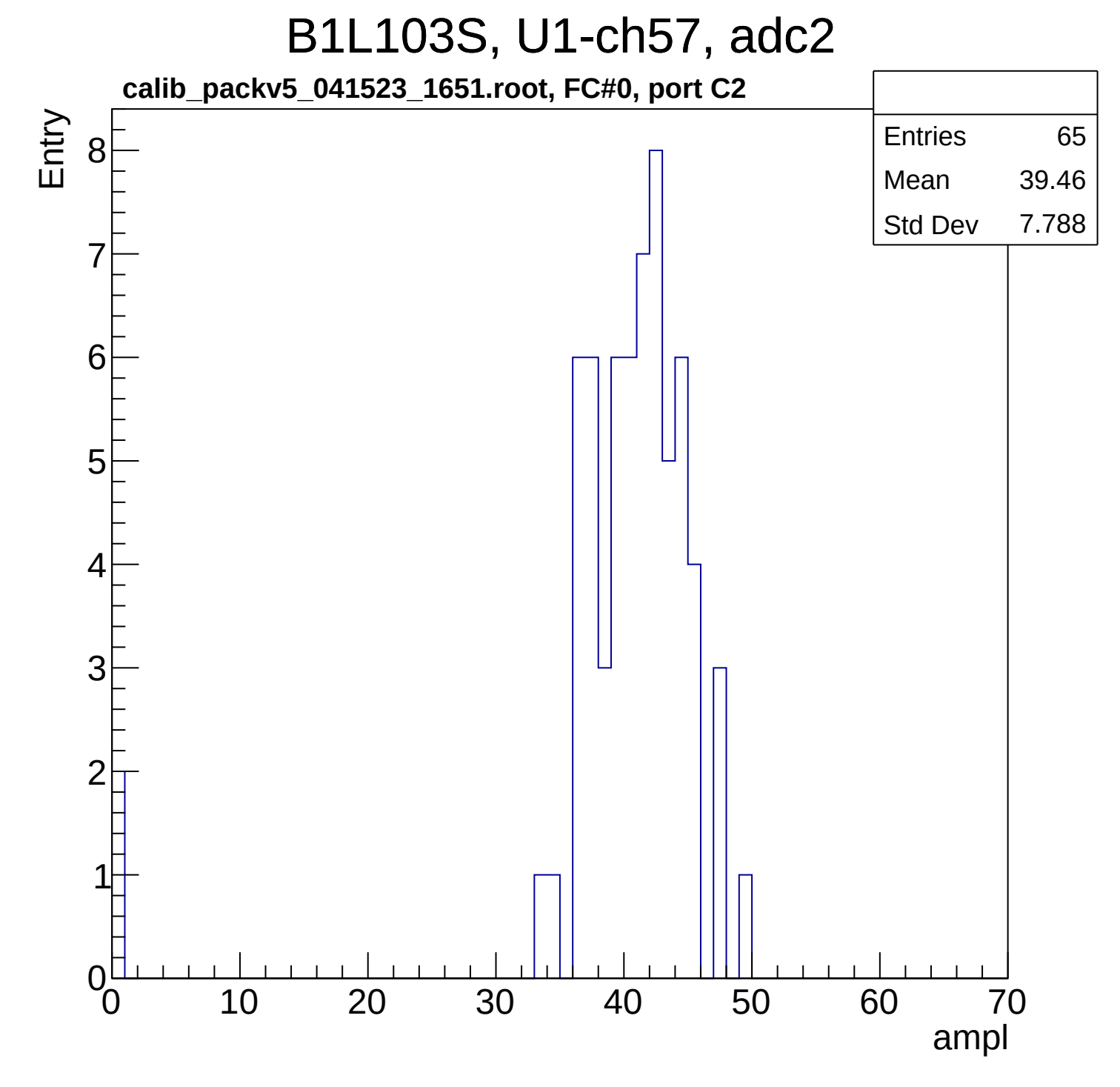
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U1-ch57, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 39.46
Std Dev 7.788
Entry
ampl
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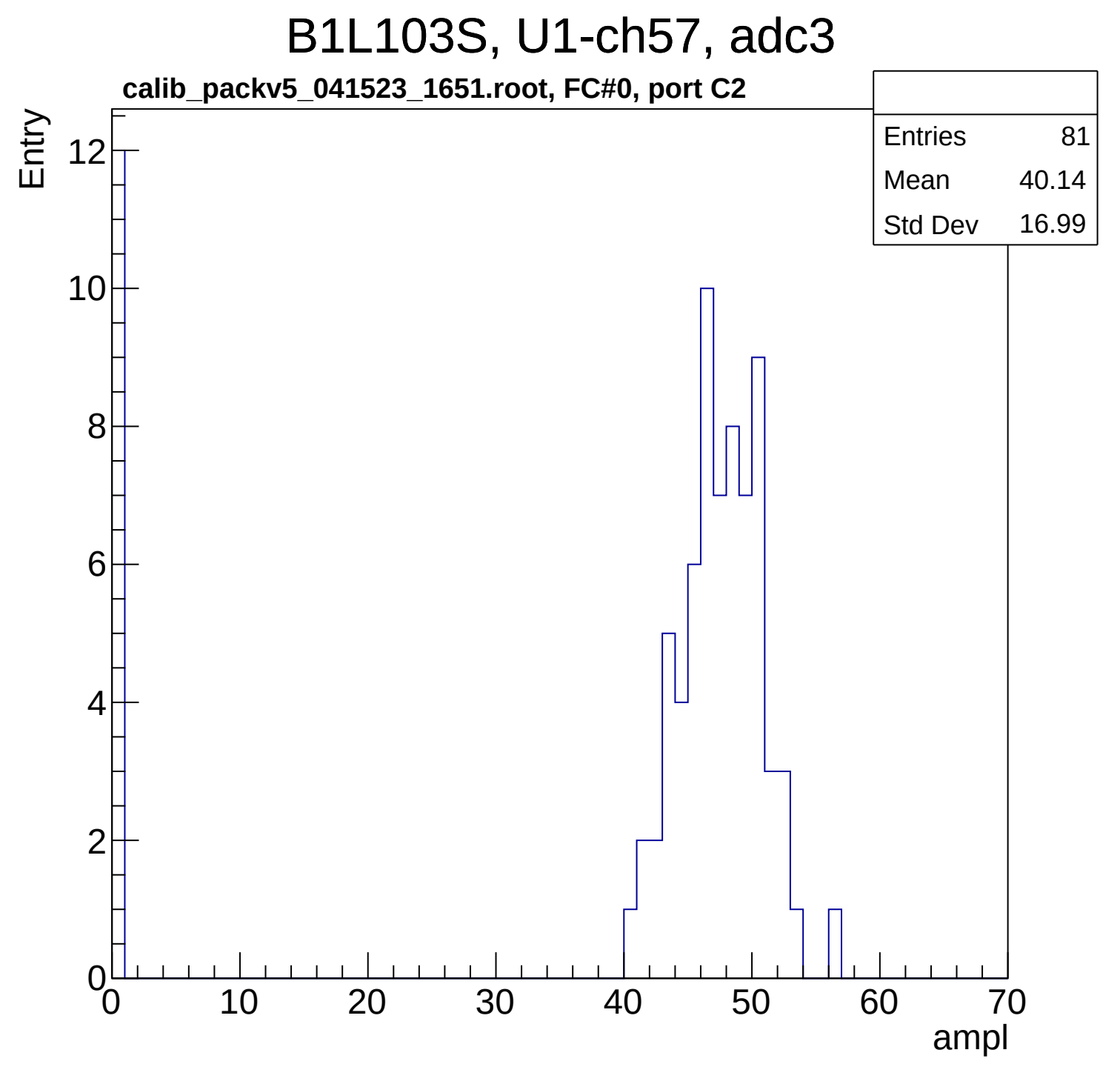
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U1-ch57, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 40.14
Std Dev 16.99
Entry
ampl
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4
6
8
10
12
0
10
20
30
40
50
60
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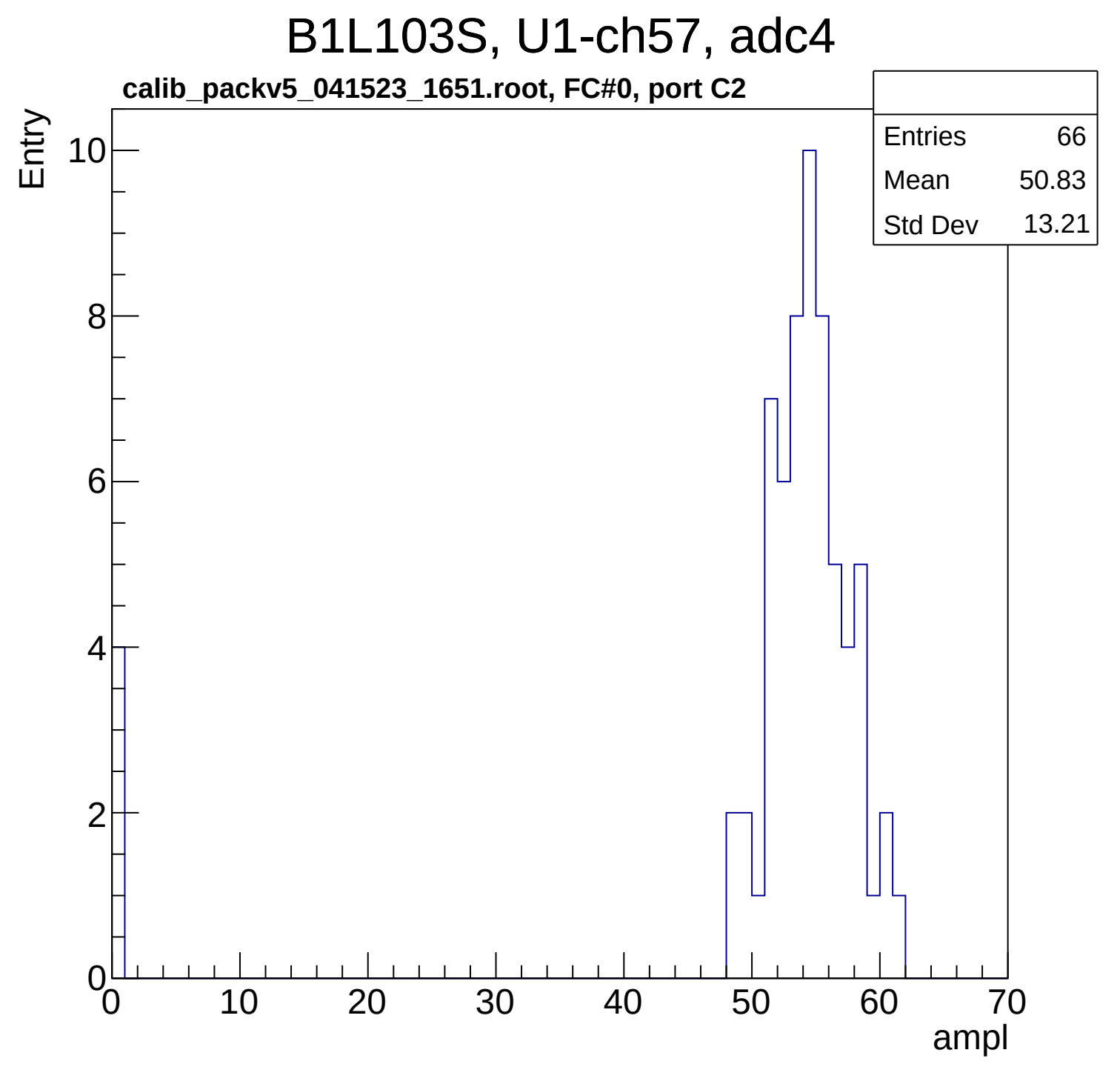
B1L103S, U1-ch57, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 50.83
Std Dev 13.21
Entry
ampl
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2
4
6
8
10
0
10
20
30
40
50
60
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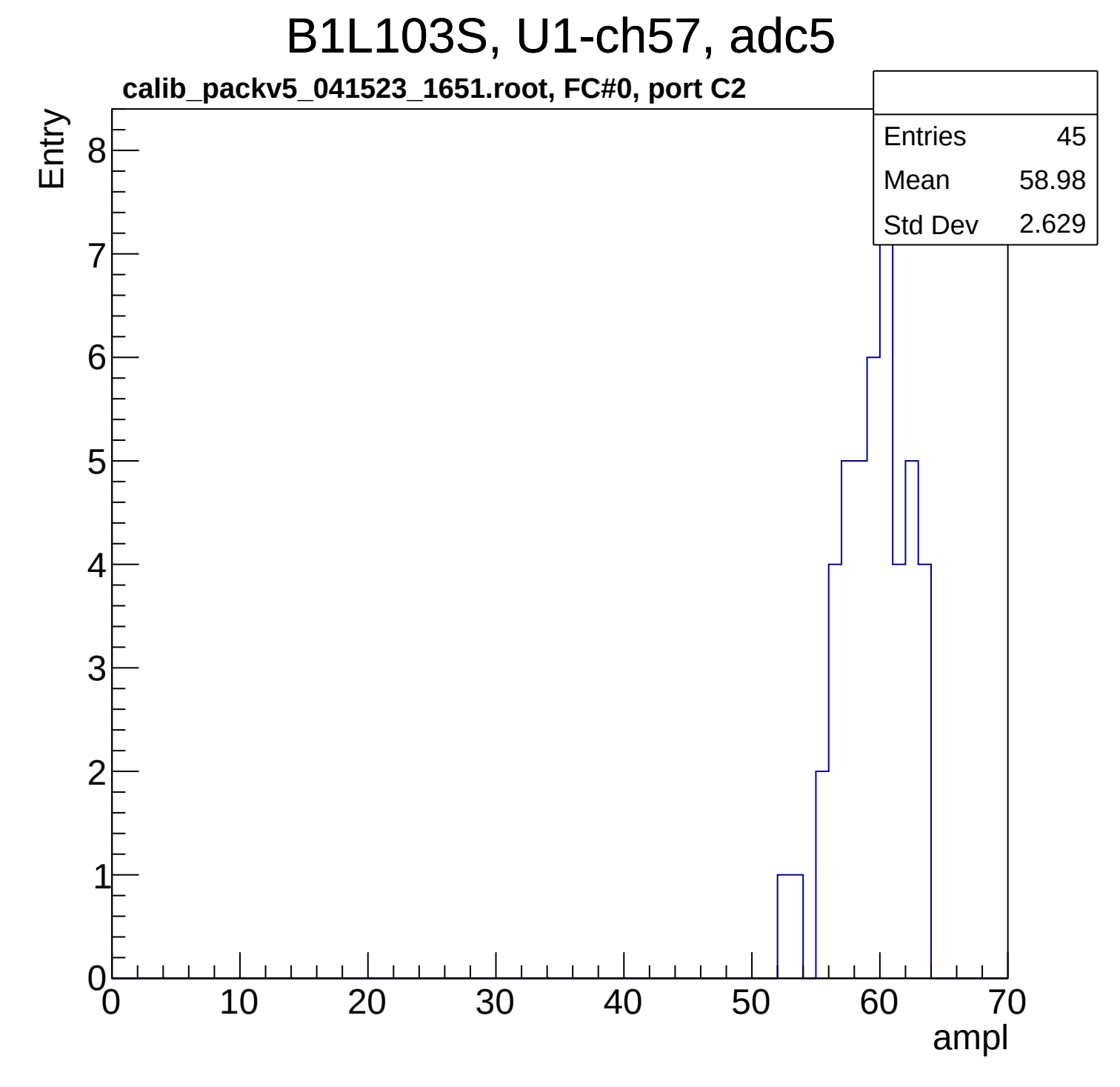
B1L103S, U1-ch57, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 58.98
Std Dev 2.629
Entry
ampl
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2
3
4
5
6
7
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0
10
20
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40
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60
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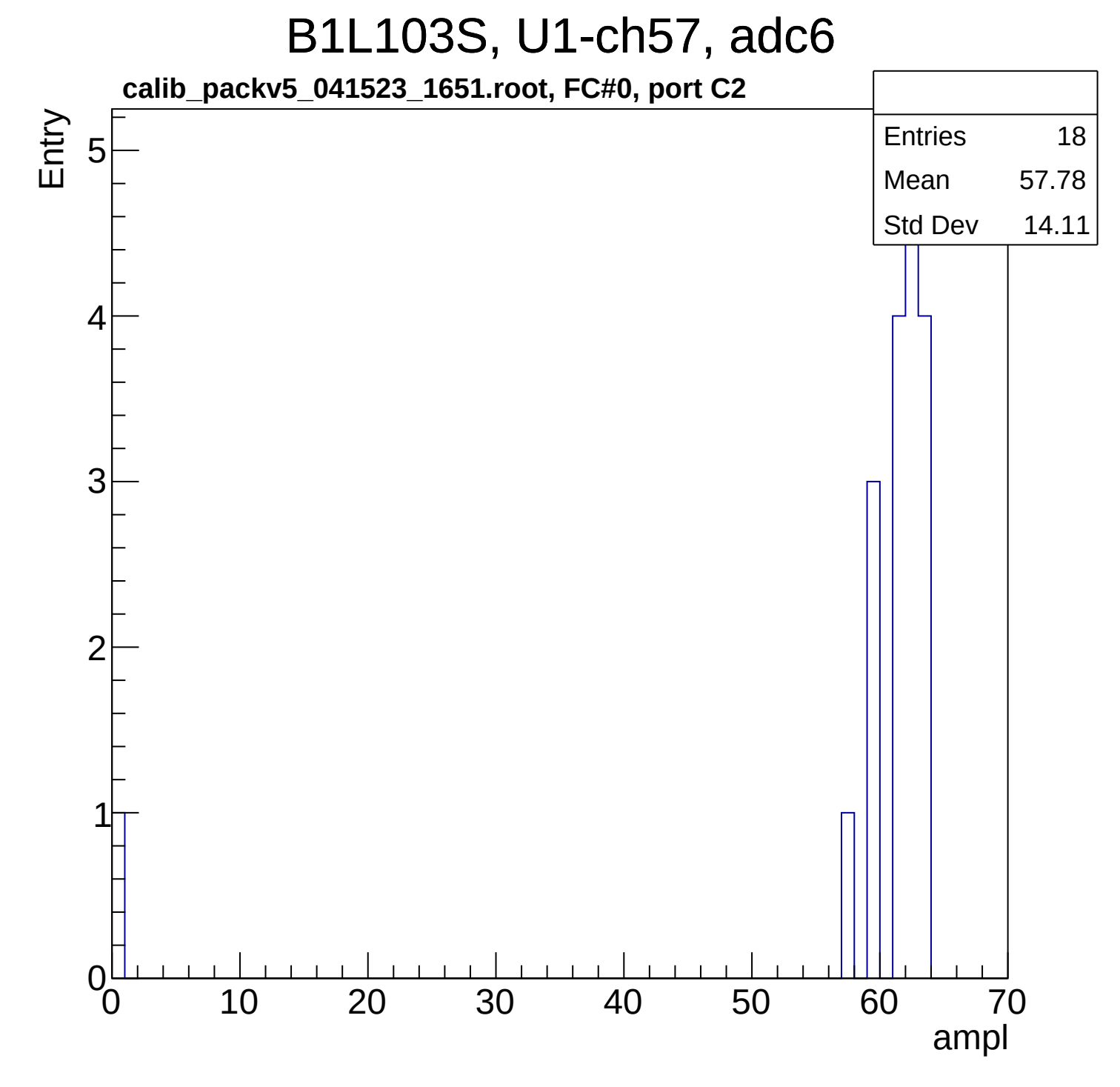
B1L103S, U1-ch57, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 57.78
Std Dev 14.11
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
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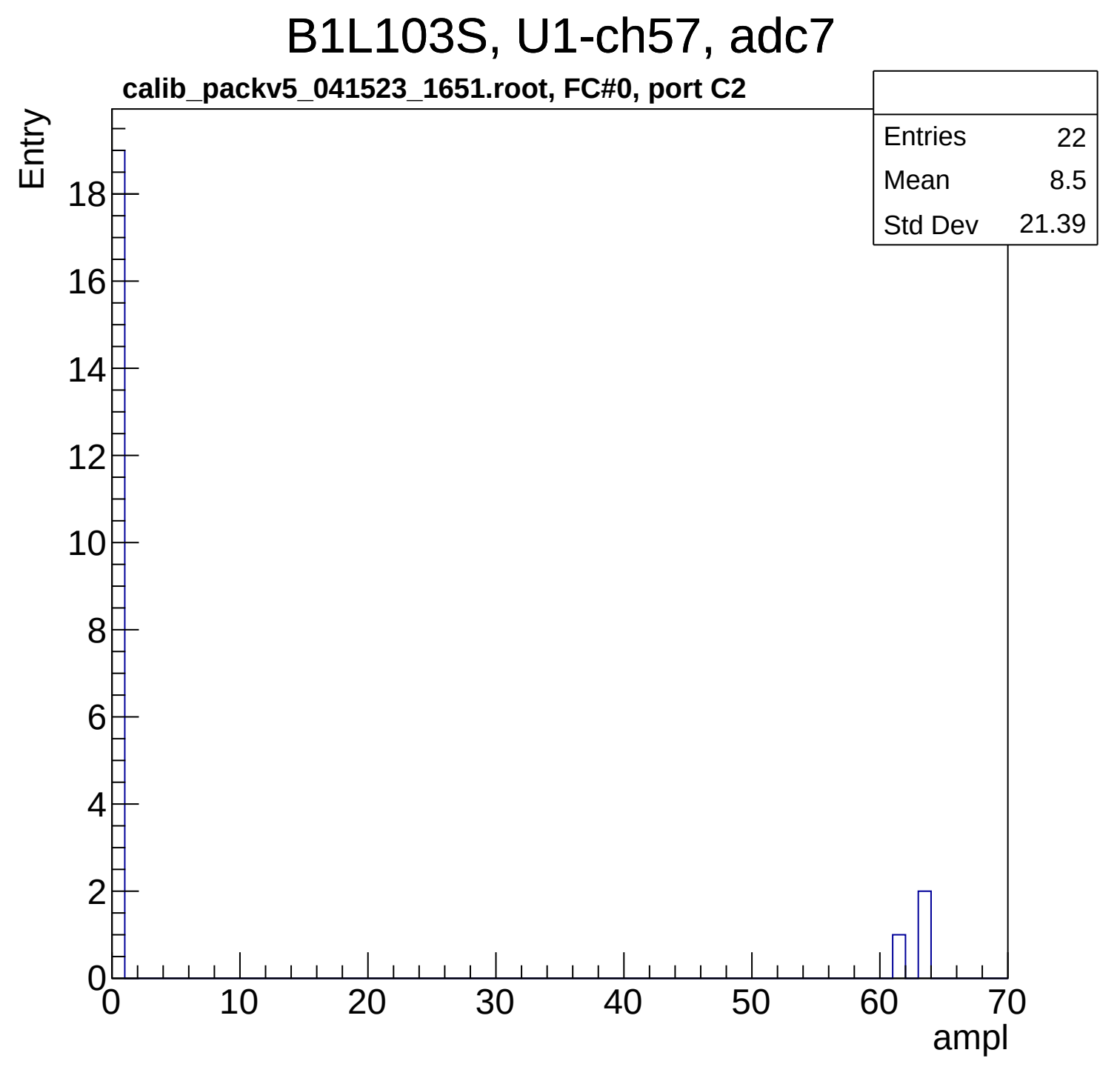
B1L103S, U1-ch57, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 8.5
Std Dev 21.39
Entry
0
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4
6
8
10
12
14
16
18
0
10
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30
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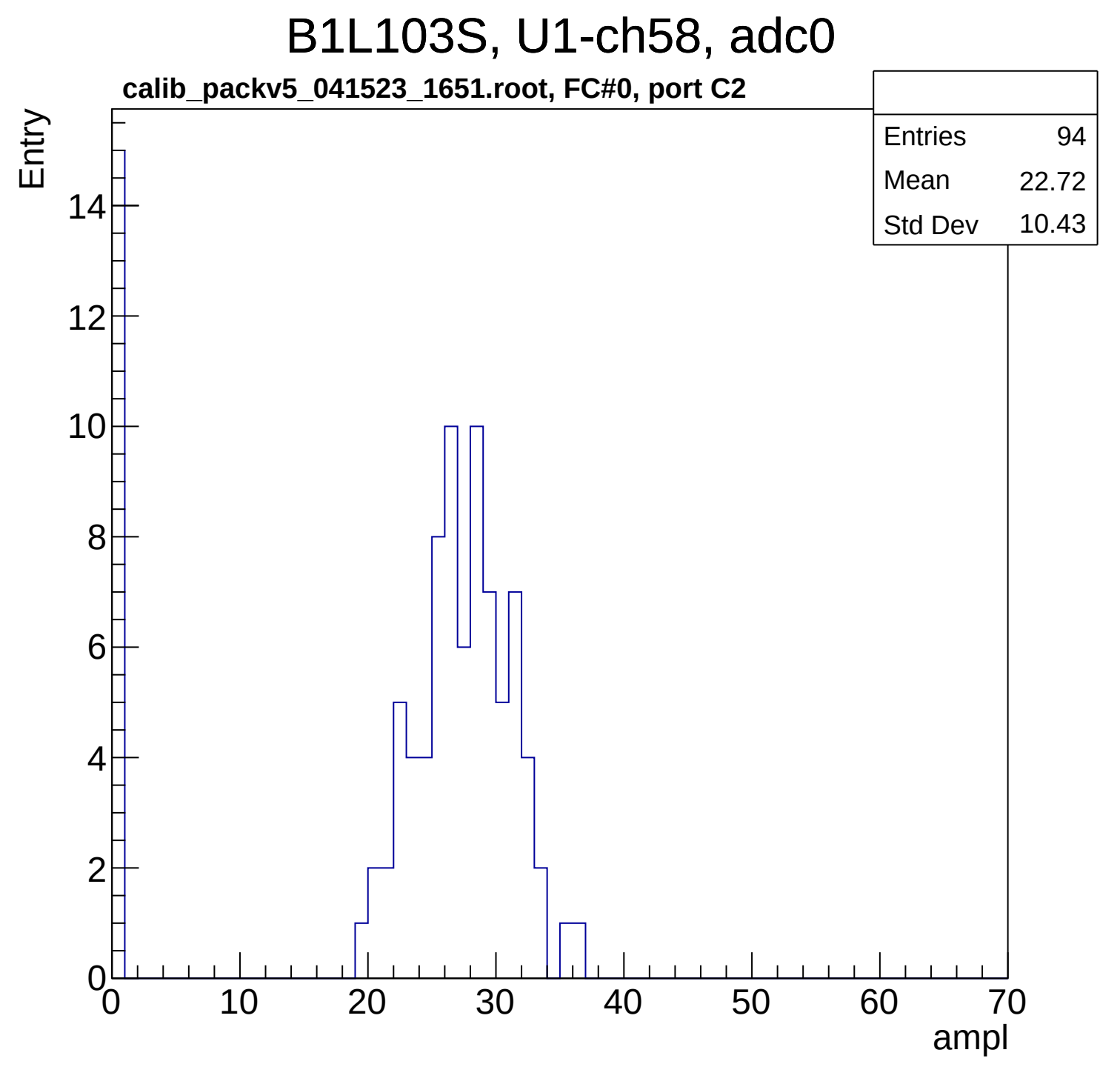
50
60
70
ampl


B1L103S, U1-ch58, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 94
Mean 22.72
Std Dev 10.43
Entry
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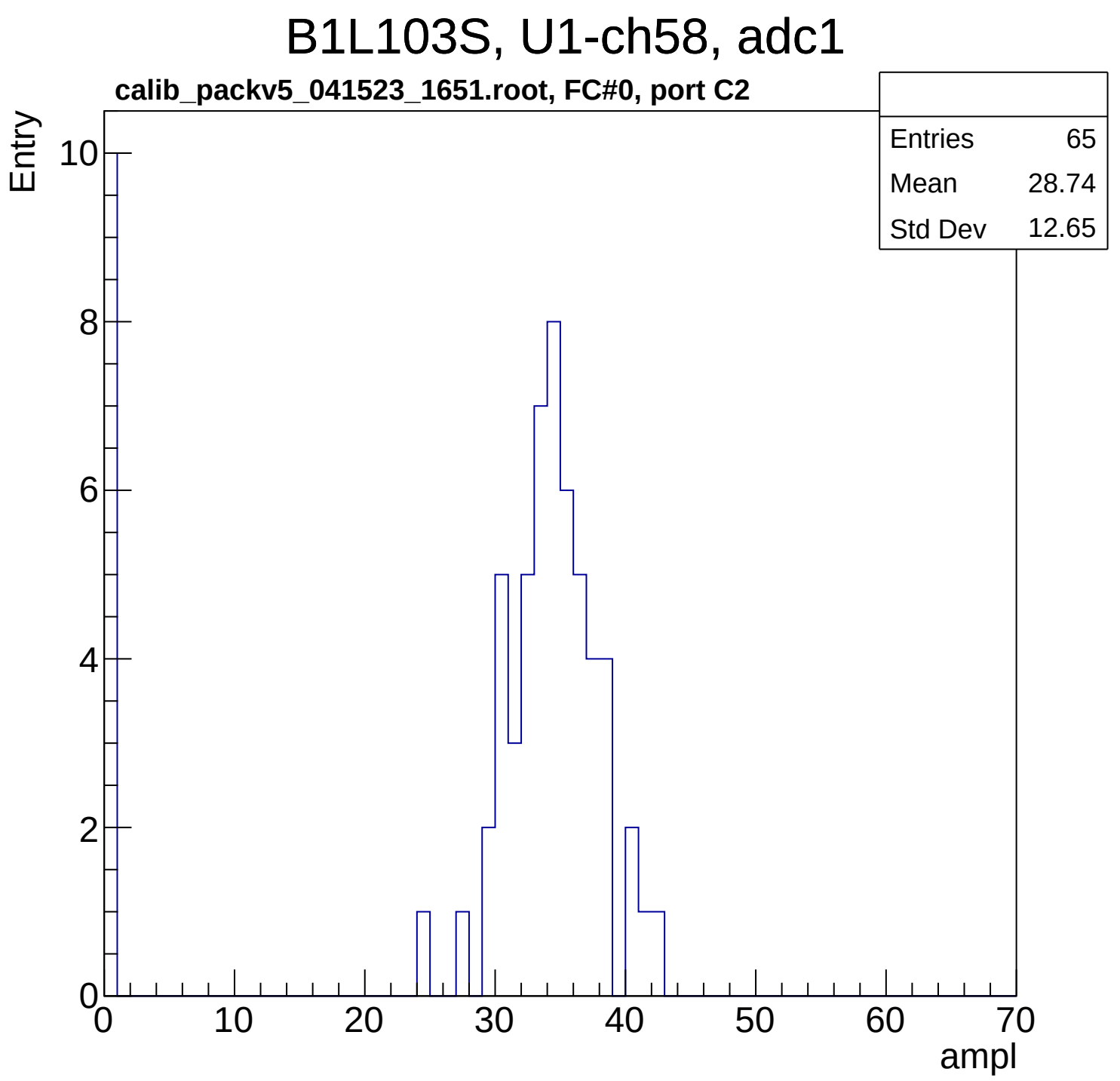
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch58, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 28.74
Std Dev 12.65
Entry
ampl
0
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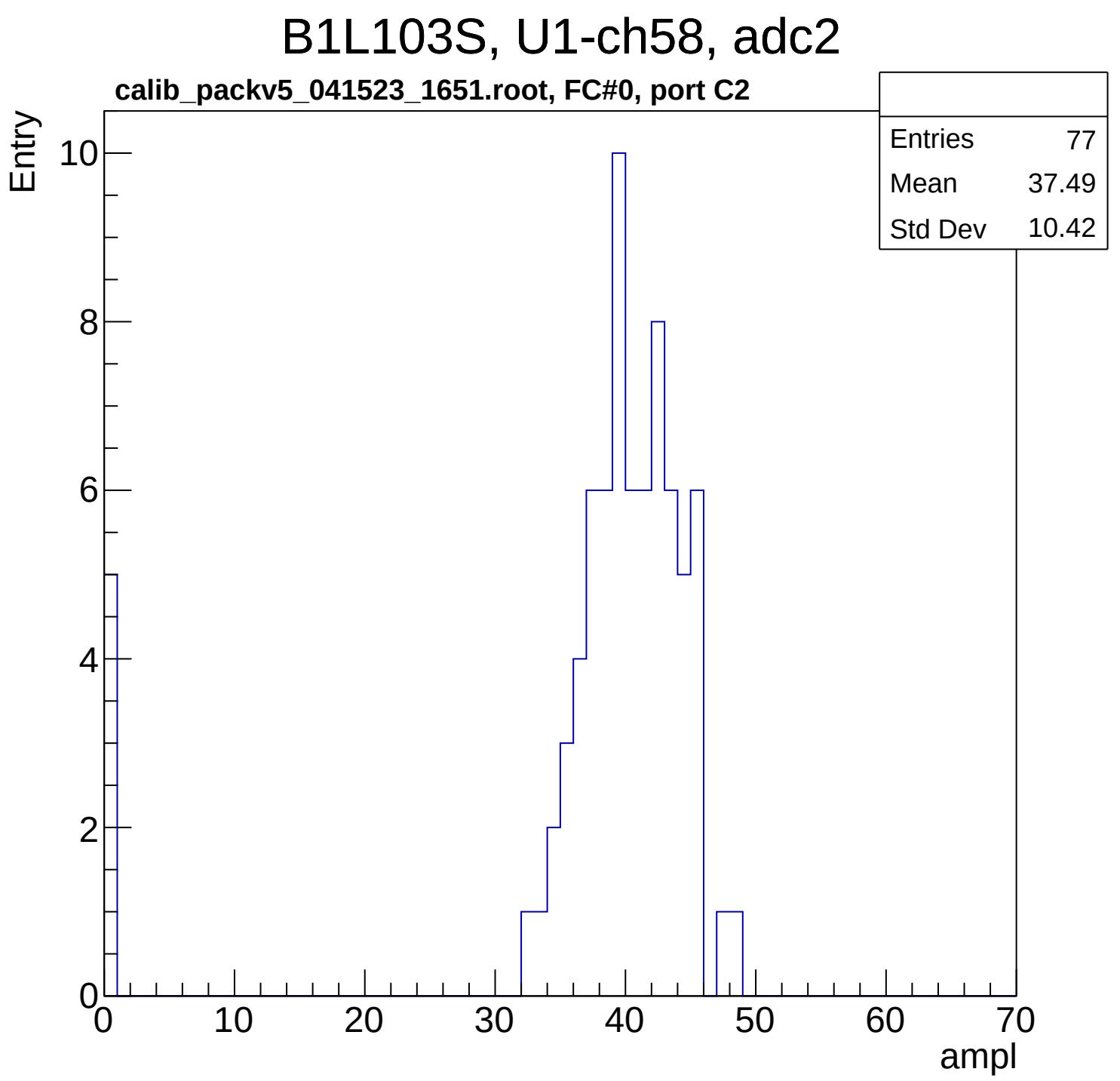
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U1-ch58, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 37.49
Std Dev 10.42
Entry
ampl
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4
6
8
10
0
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20
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40
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60
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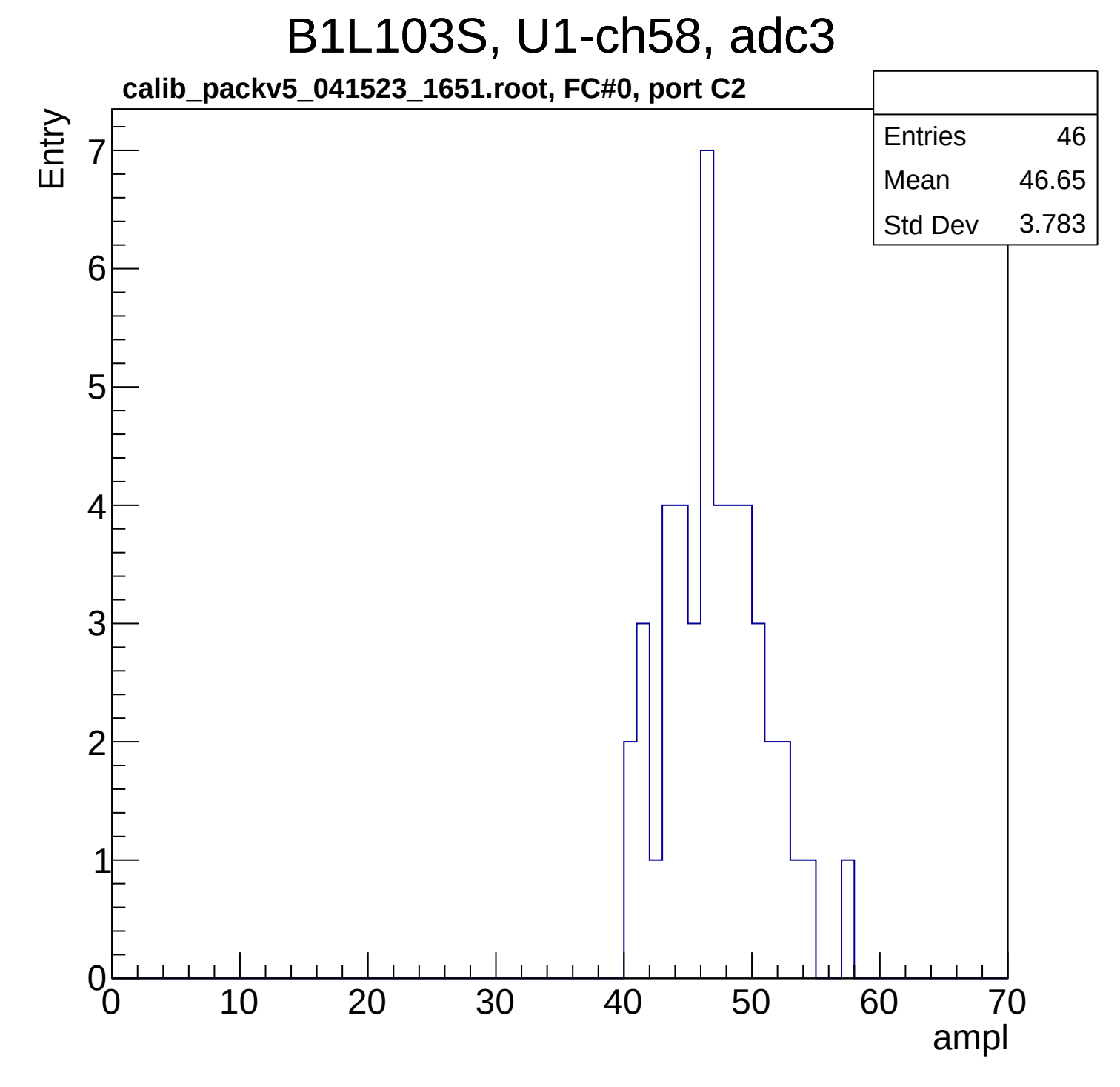
B1L103S, U1-ch58, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 46.65
Std Dev 3.783
Entry
ampl
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2
3
4
5
6
7
0
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20
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60
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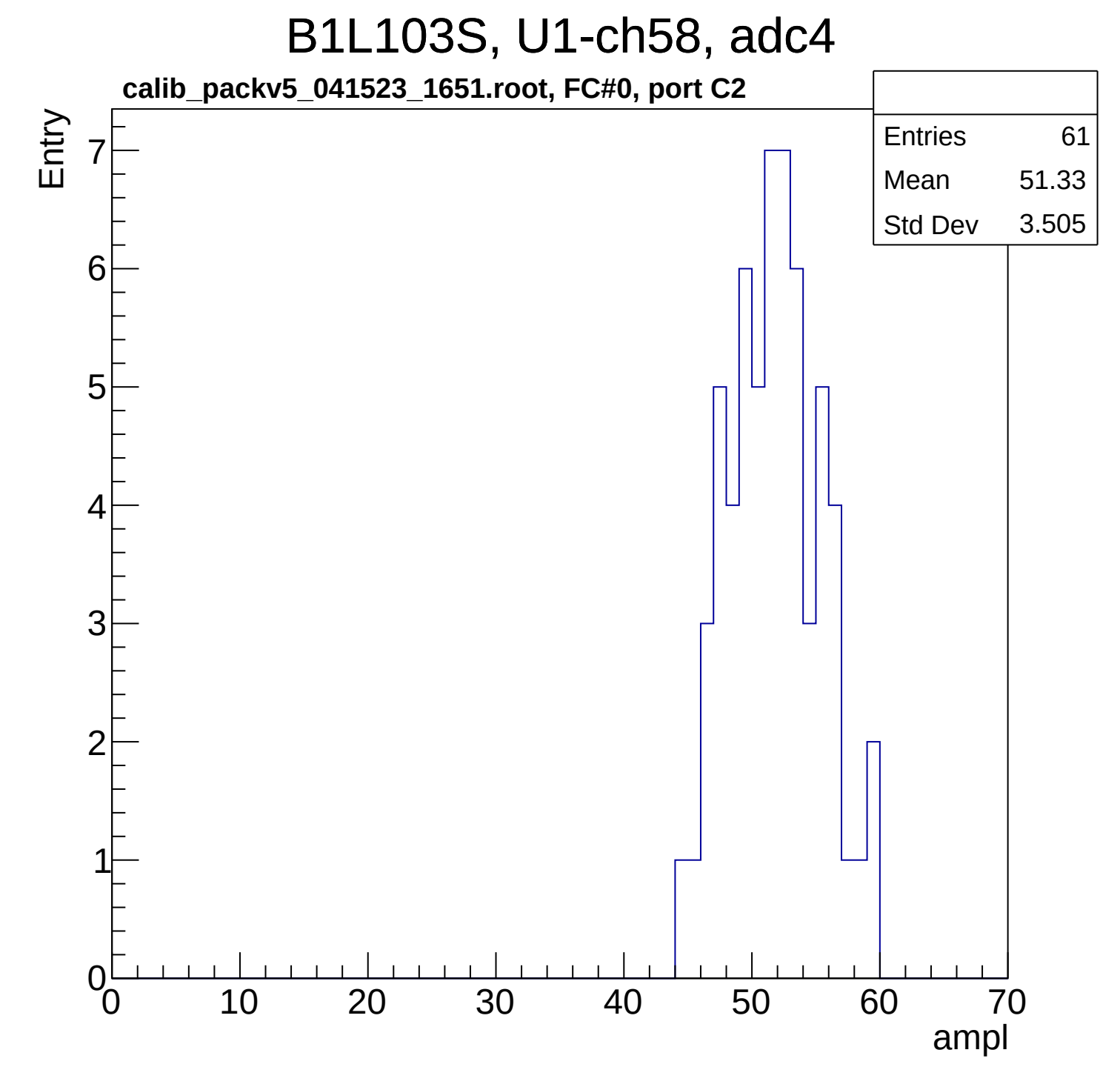
B1L103S, U1-ch58, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 51.33
Std Dev 3.505
Entry
ampl
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4
5
6
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0
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60
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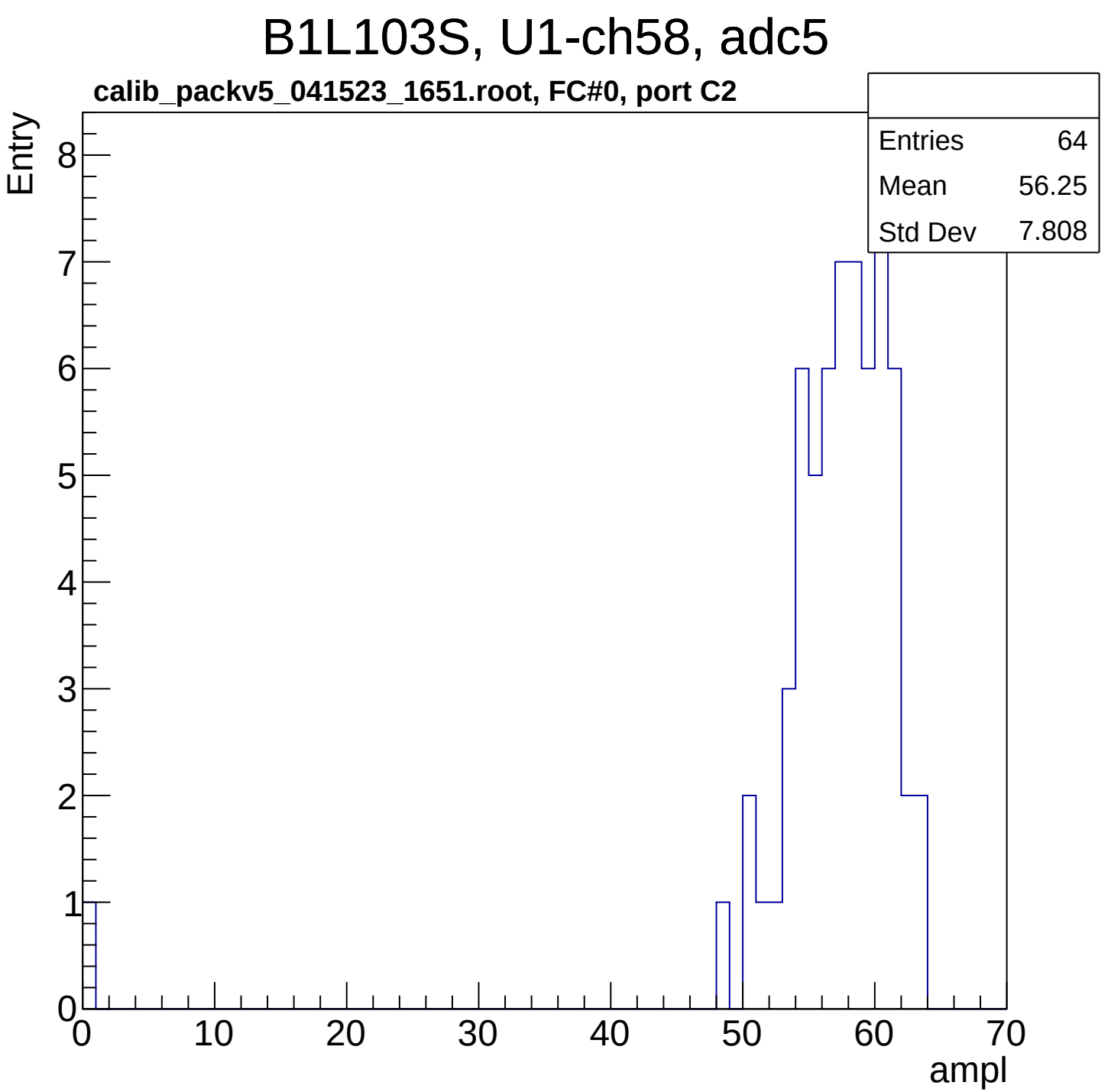
B1L103S, U1-ch58, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 56.25
Std Dev 7.808
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
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40
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60
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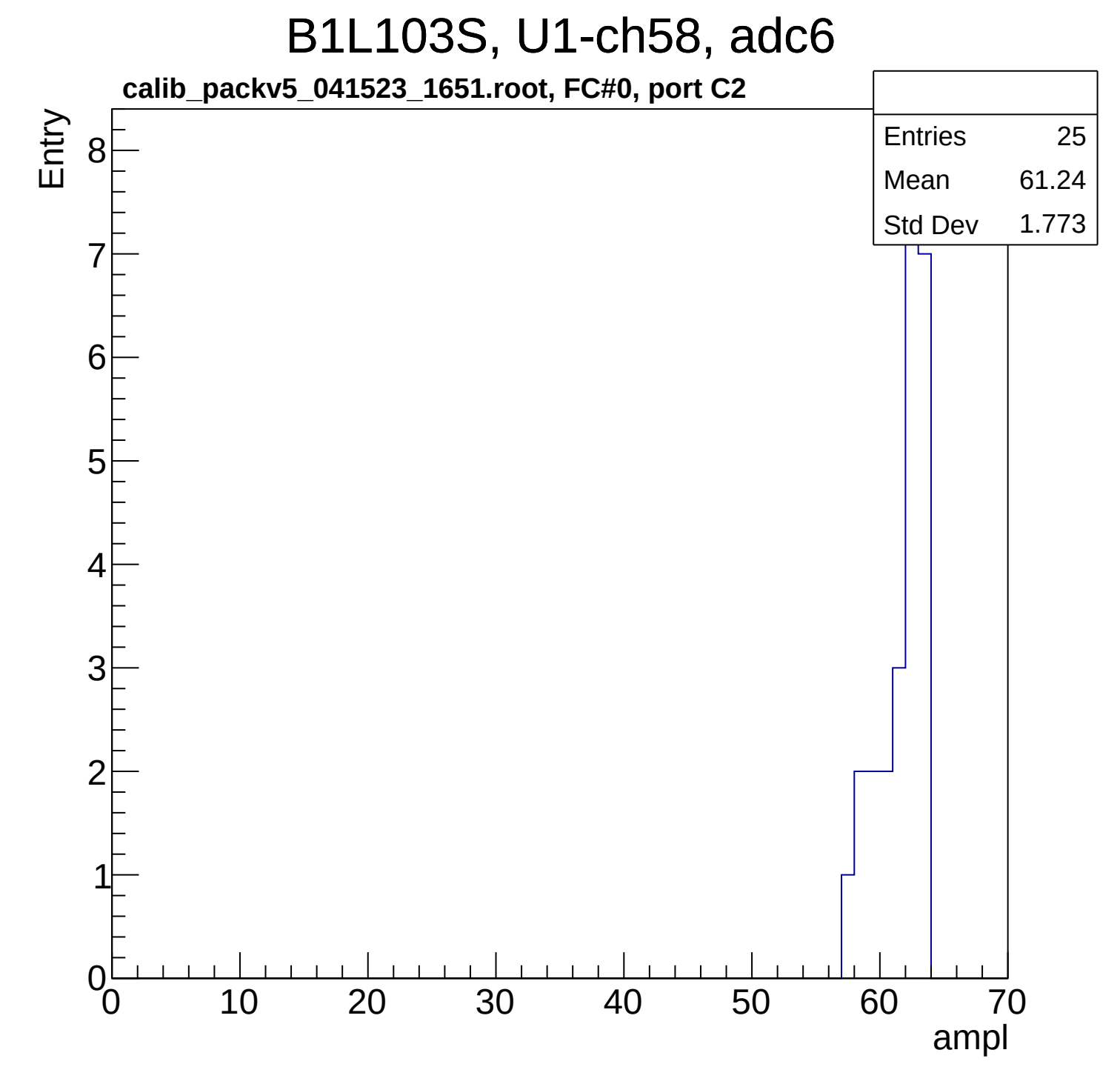
B1L103S, U1-ch58, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 25
Mean 61.24
Std Dev 1.773
Entry
ampl
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2
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4
5
6
7
8
0
10
20
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40
50
60
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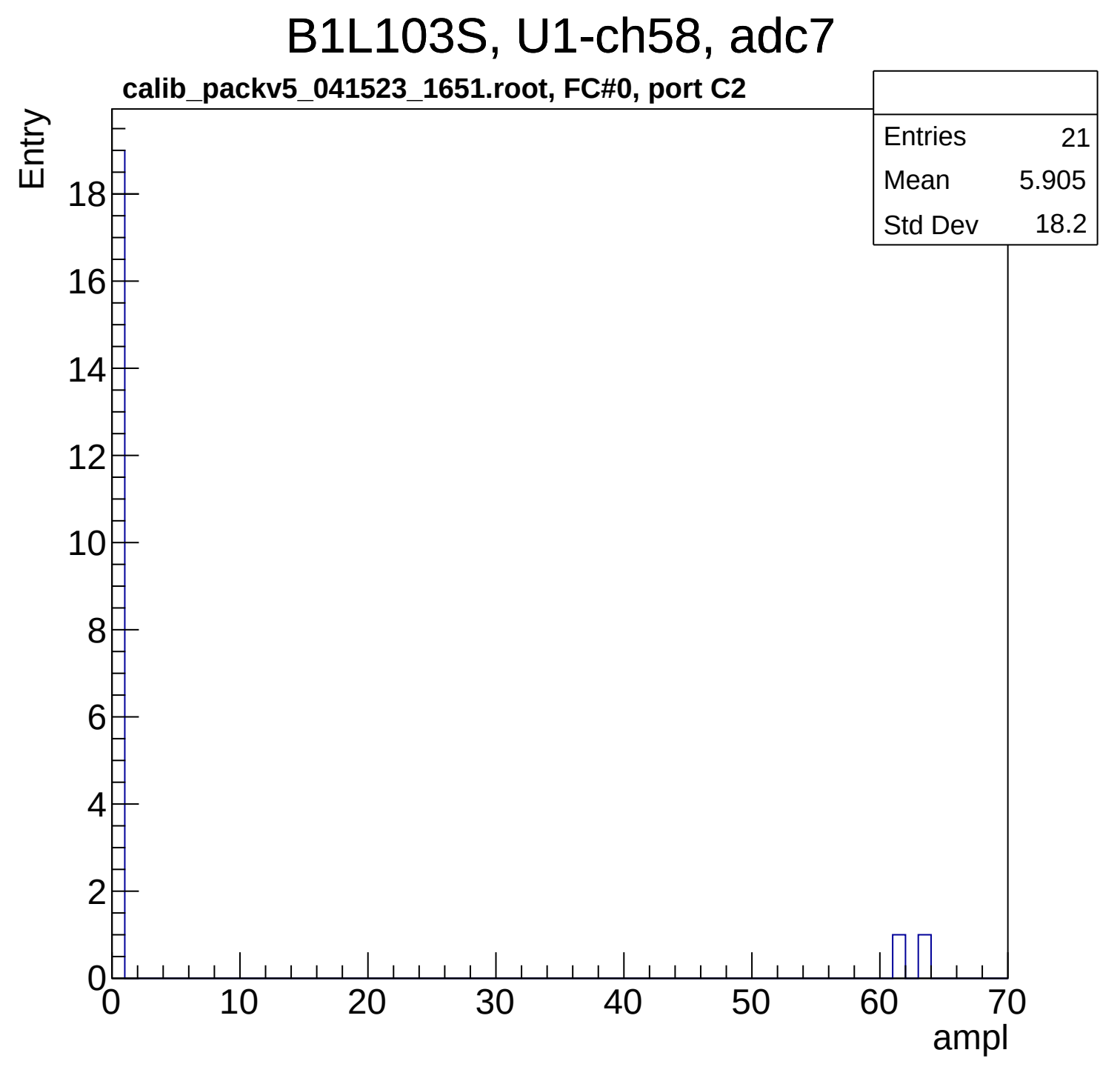
B1L103S, U1-ch58, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 5.905
Std Dev 18.2
Entry
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6
8
10
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14
16
18
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10
20
30
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50
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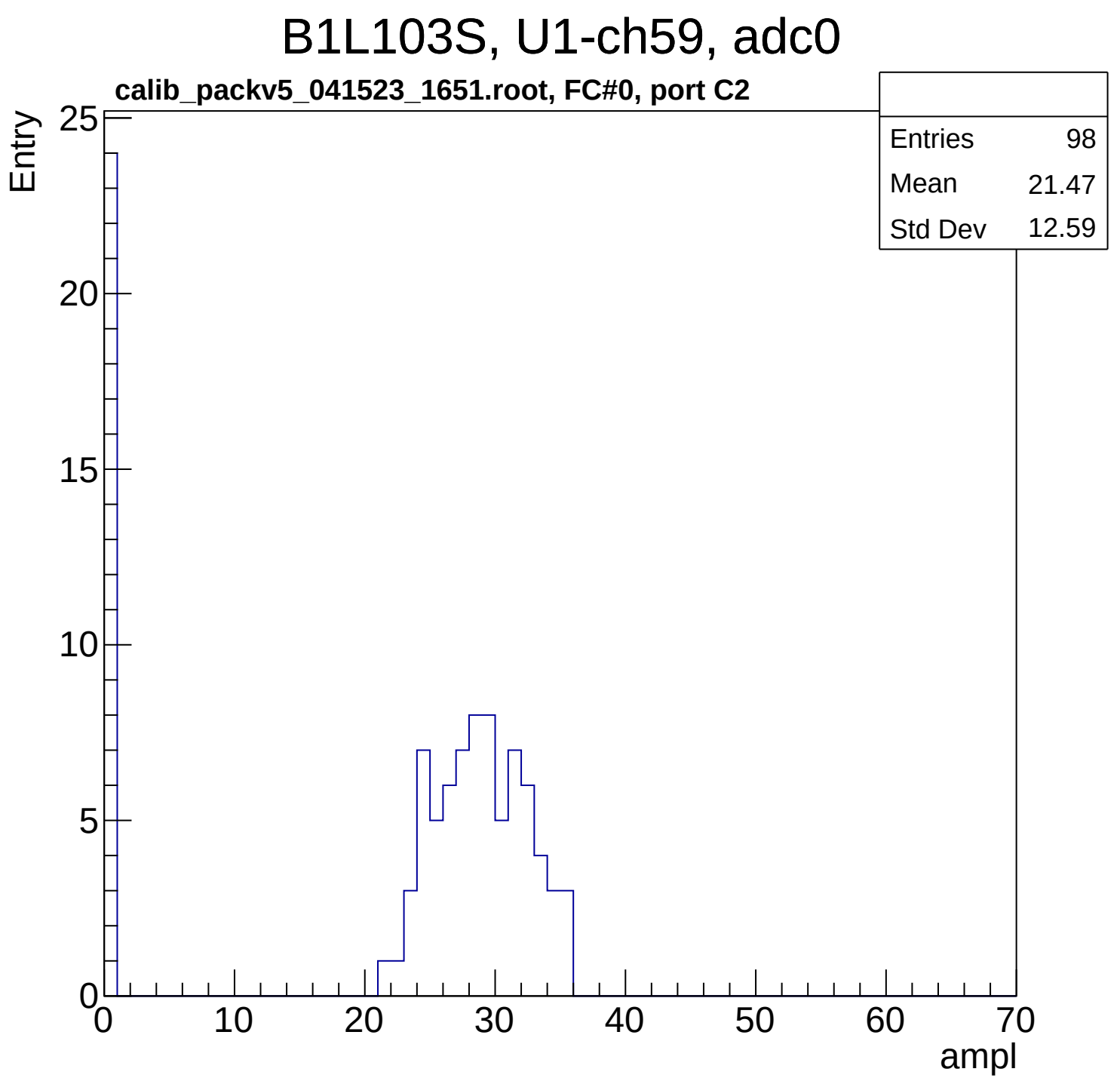
70
ampl


B1L103S, U1-ch59, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 98
Mean 21.47
Std Dev 12.59
Entry
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15
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25
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10
20
30
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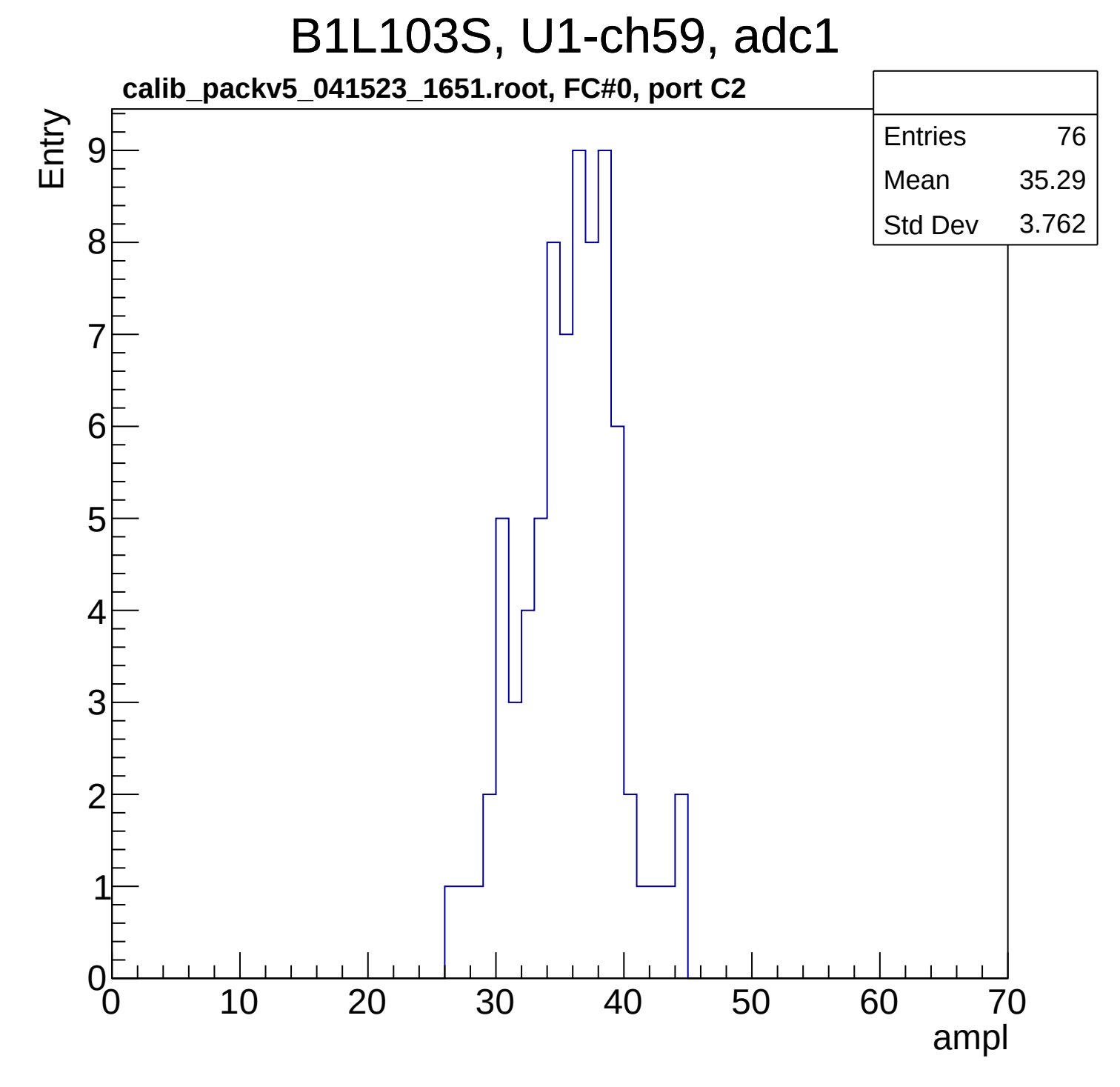
50
60
70
ampl


B1L103S, U1-ch59, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 35.29
Std Dev 3.762
Entry
ampl
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3
4
5
6
7
8
9
0
10
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60
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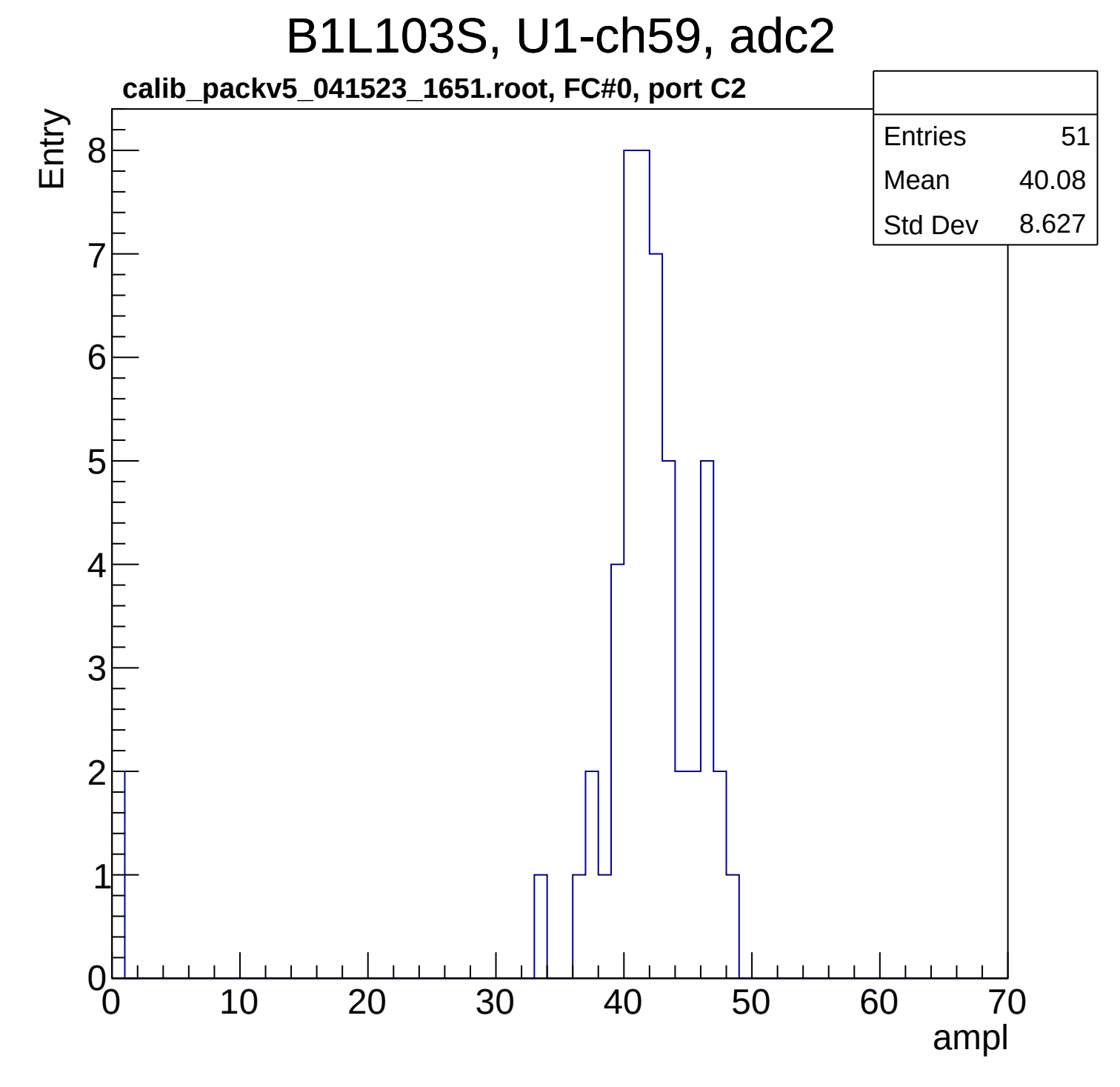
B1L103S, U1-ch59, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 40.08
Std Dev 8.627
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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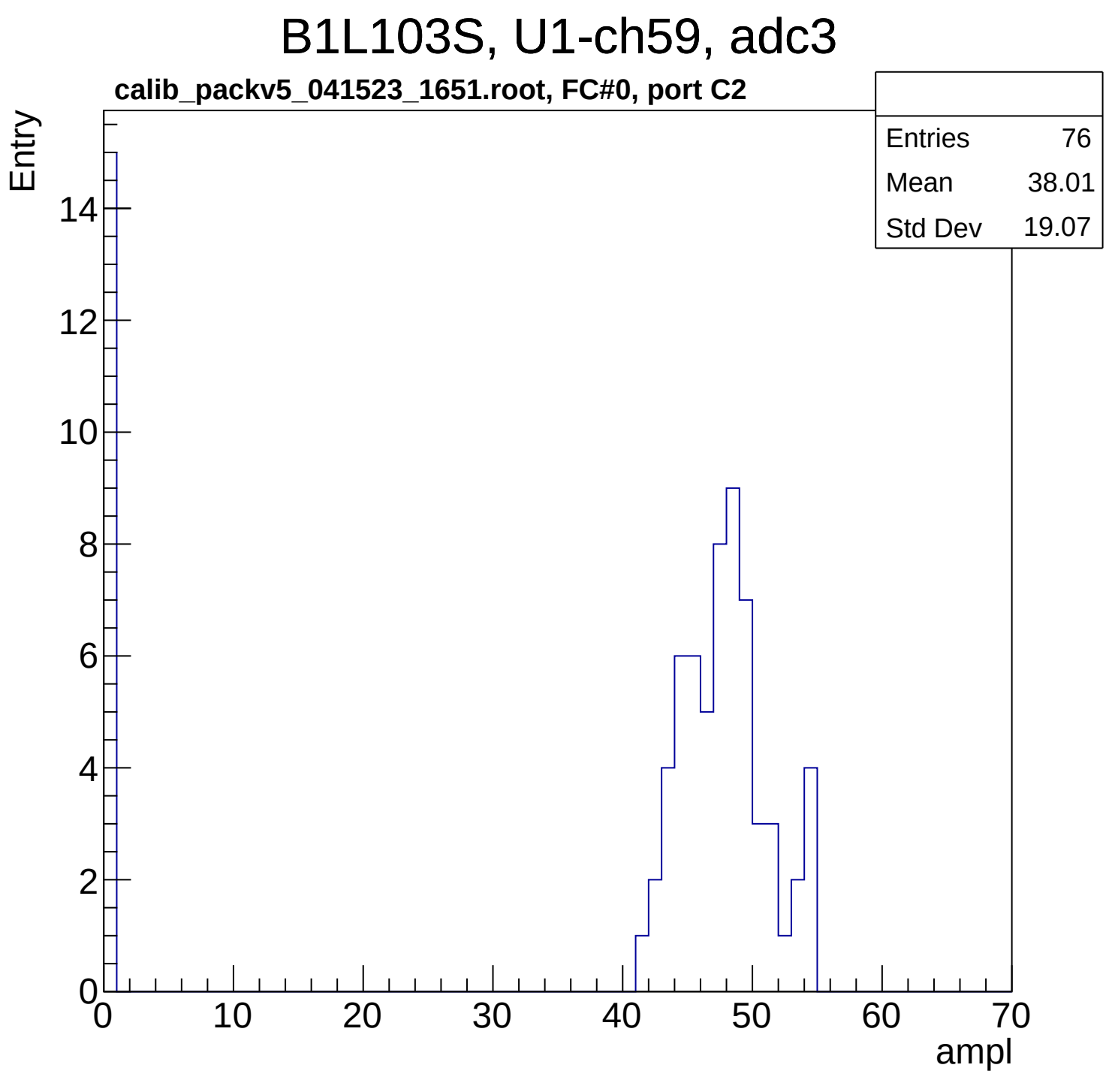
50
60
70


B1L103S, U1-ch59, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 38.01
Std Dev 19.07
Entry
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2
4
6
8
10
12
14
0
10
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30
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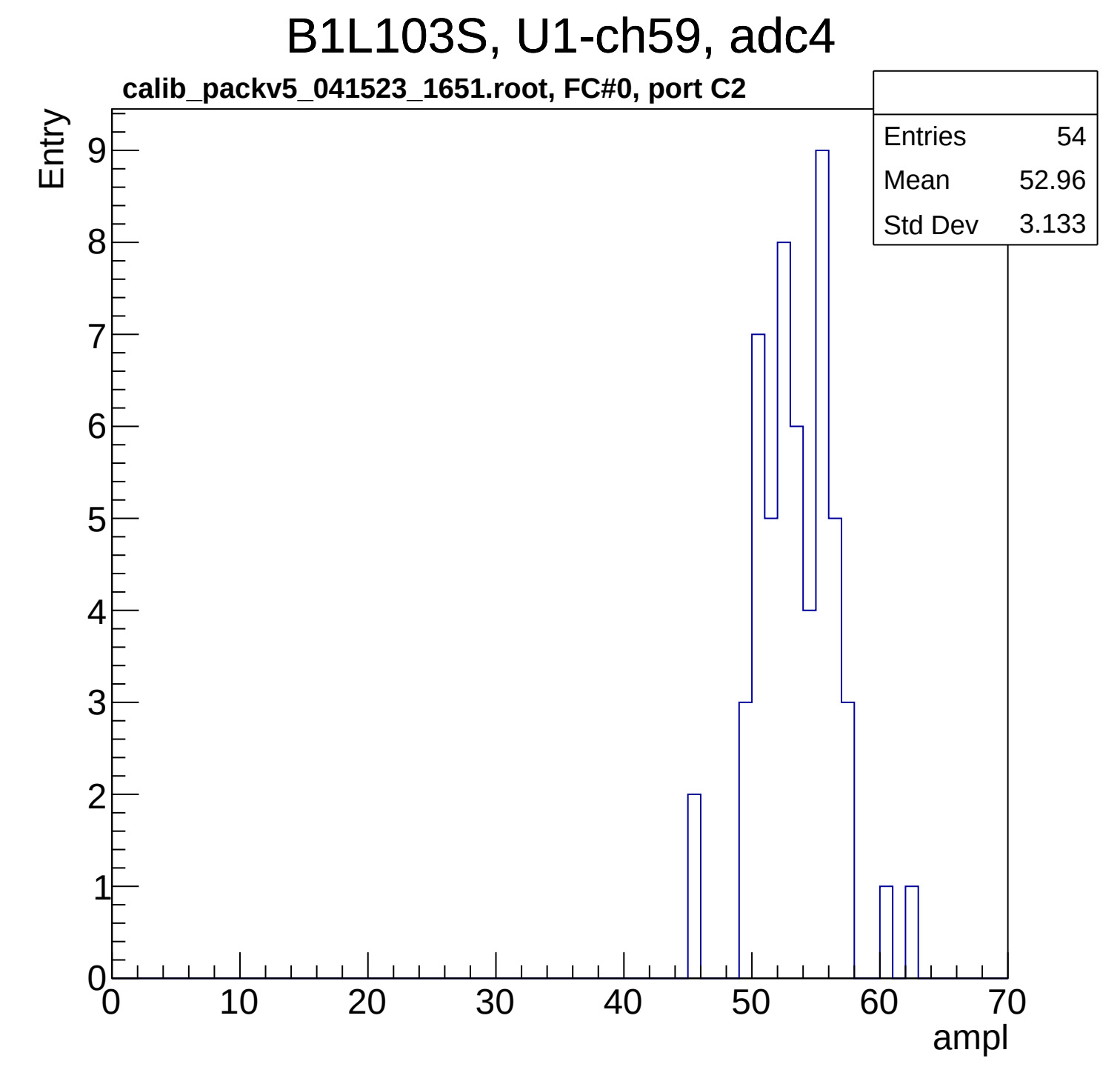
50
60
70
ampl


B1L103S, U1-ch59, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 52.96
Std Dev 3.133
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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40
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60
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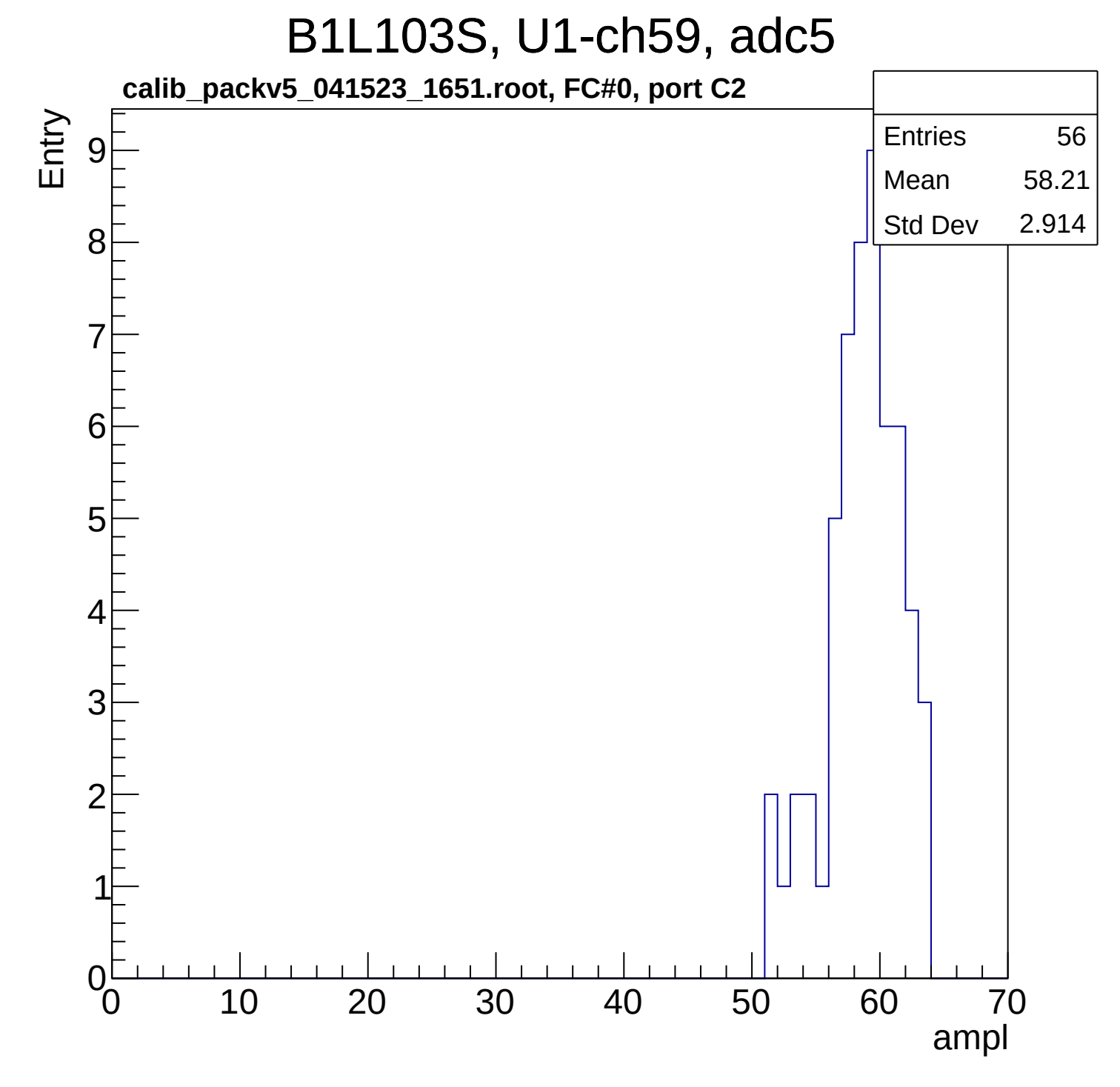
B1L103S, U1-ch59, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 58.21
Std Dev 2.914
Entry
ampl
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3
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5
6
7
8
9
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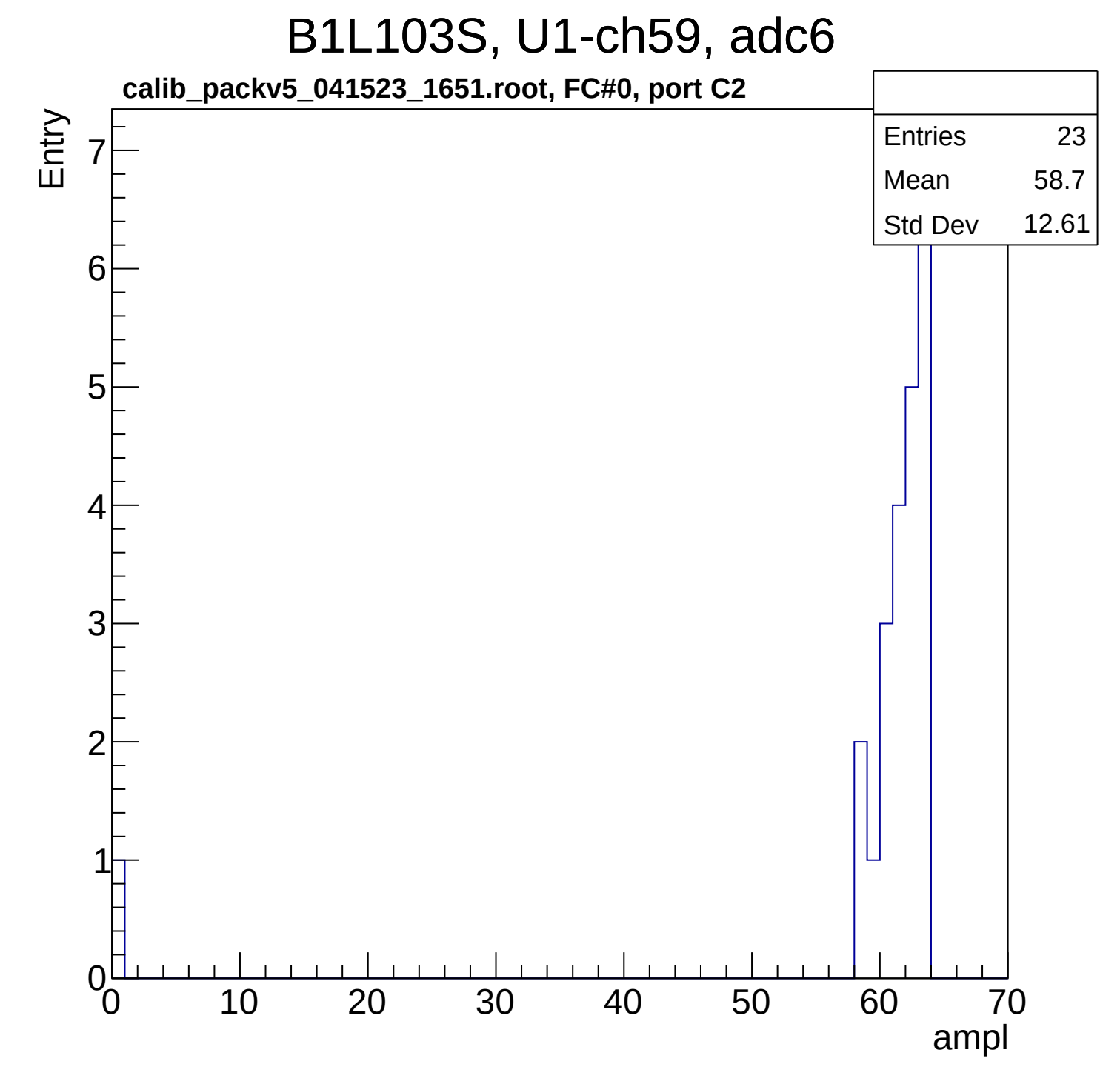
B1L103S, U1-ch59, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 23
Mean 58.7
Std Dev 12.61
Entry
ampl
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2
3
4
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6
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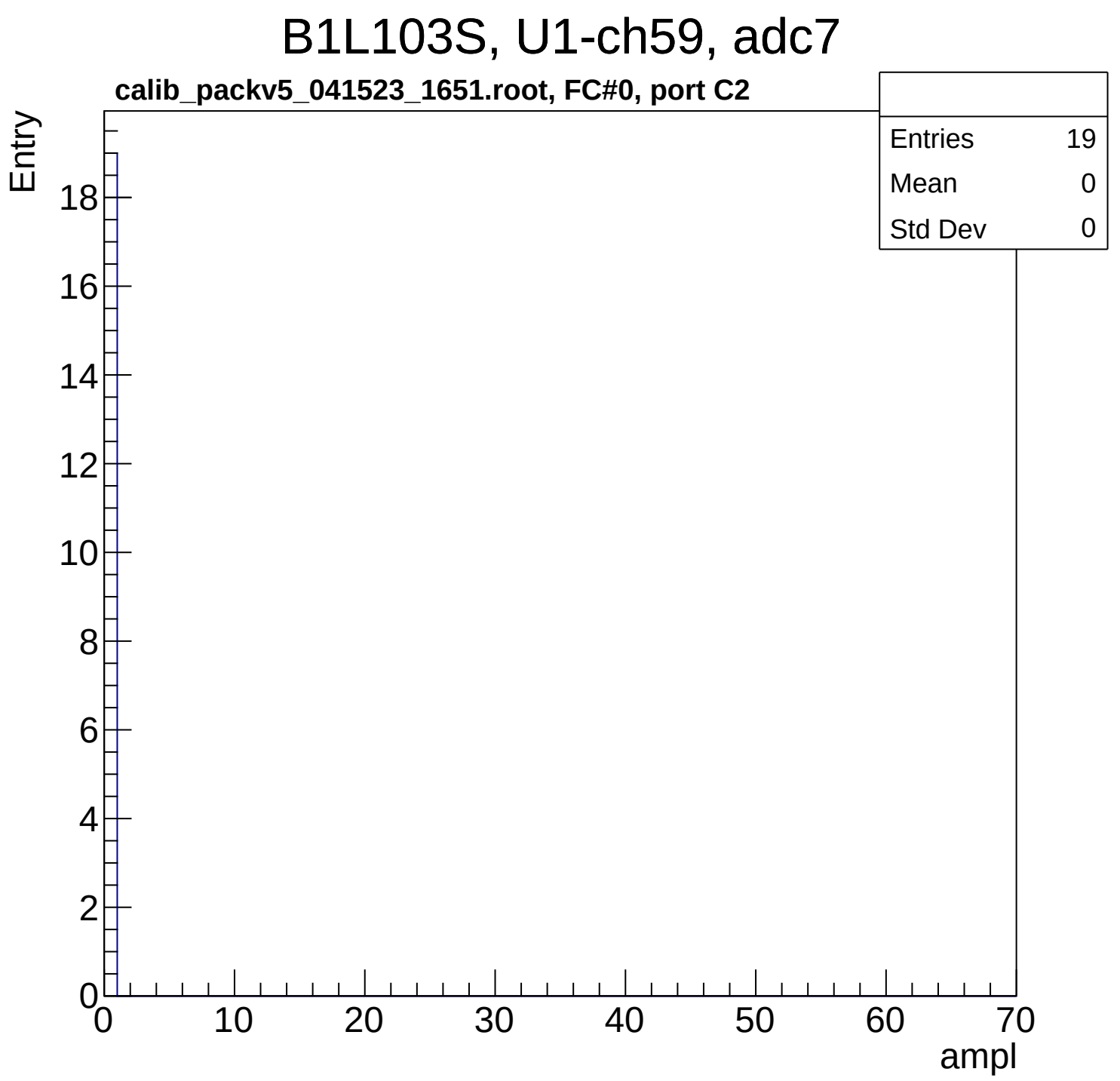
B1L103S, U1-ch59, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
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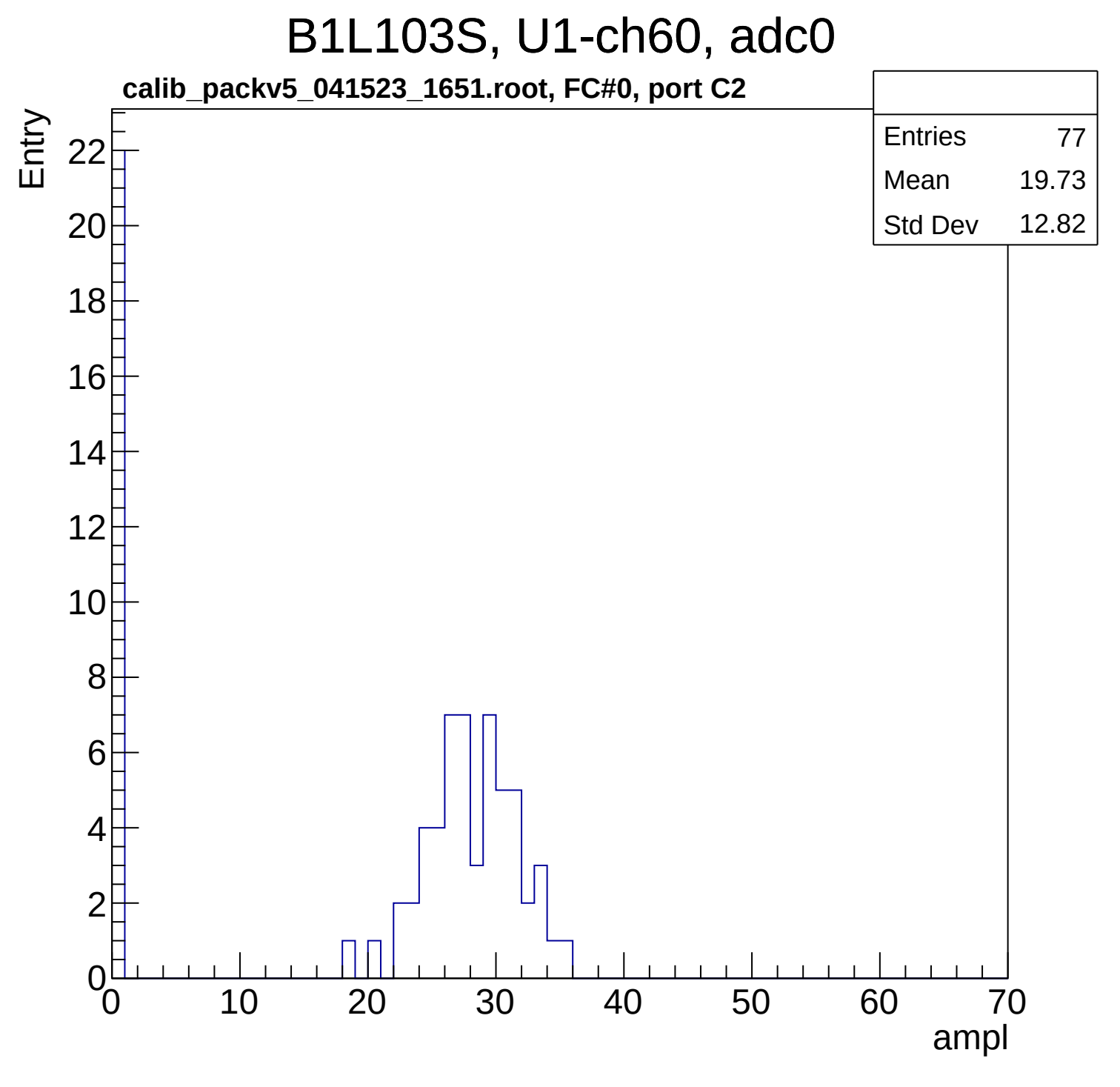
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch60, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 19.73
Std Dev 12.82
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
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0
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40
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60
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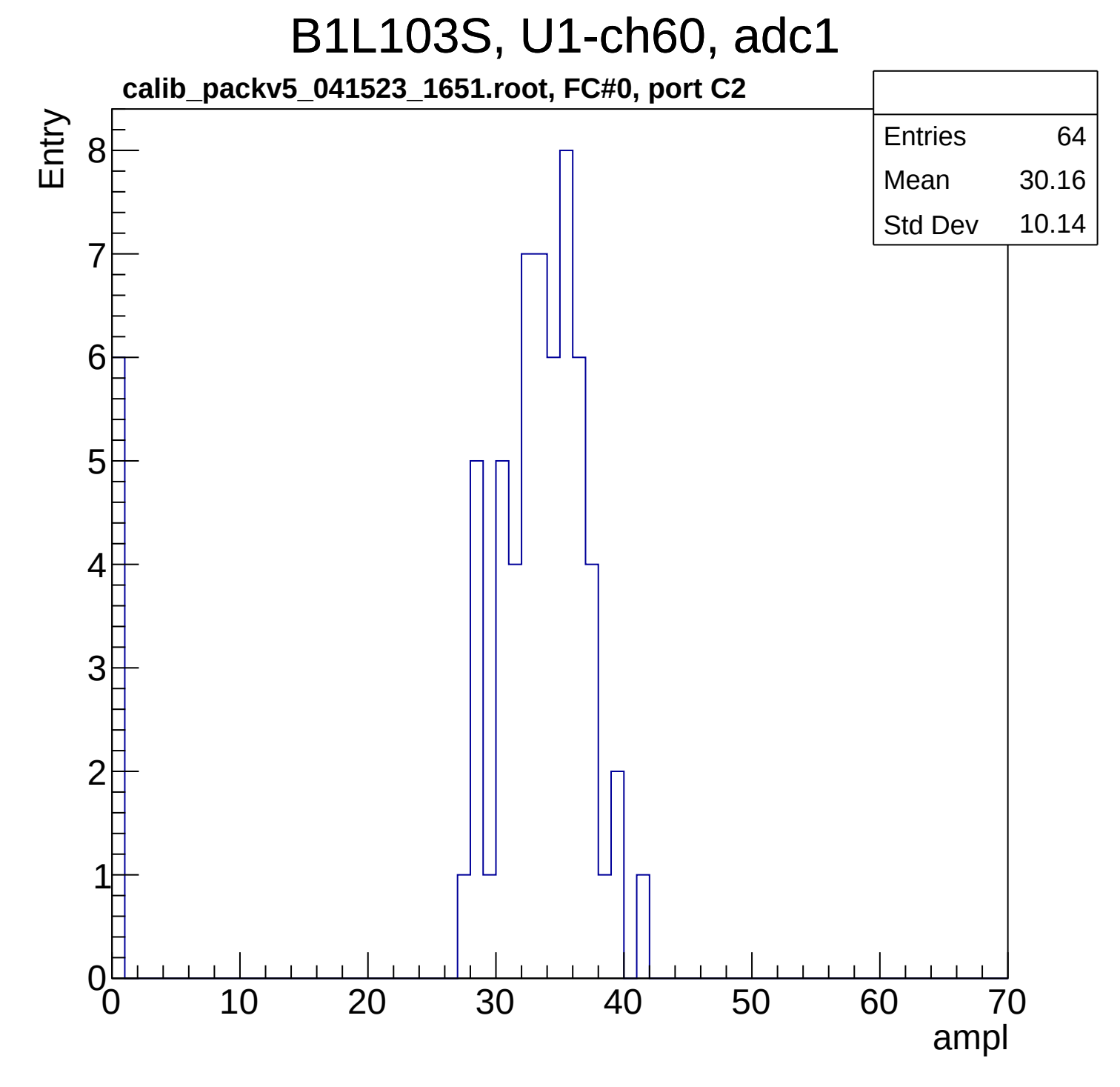
B1L103S, U1-ch60, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 30.16
Std Dev 10.14
Entry
ampl
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2
3
4
5
6
7
8
0
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40
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60
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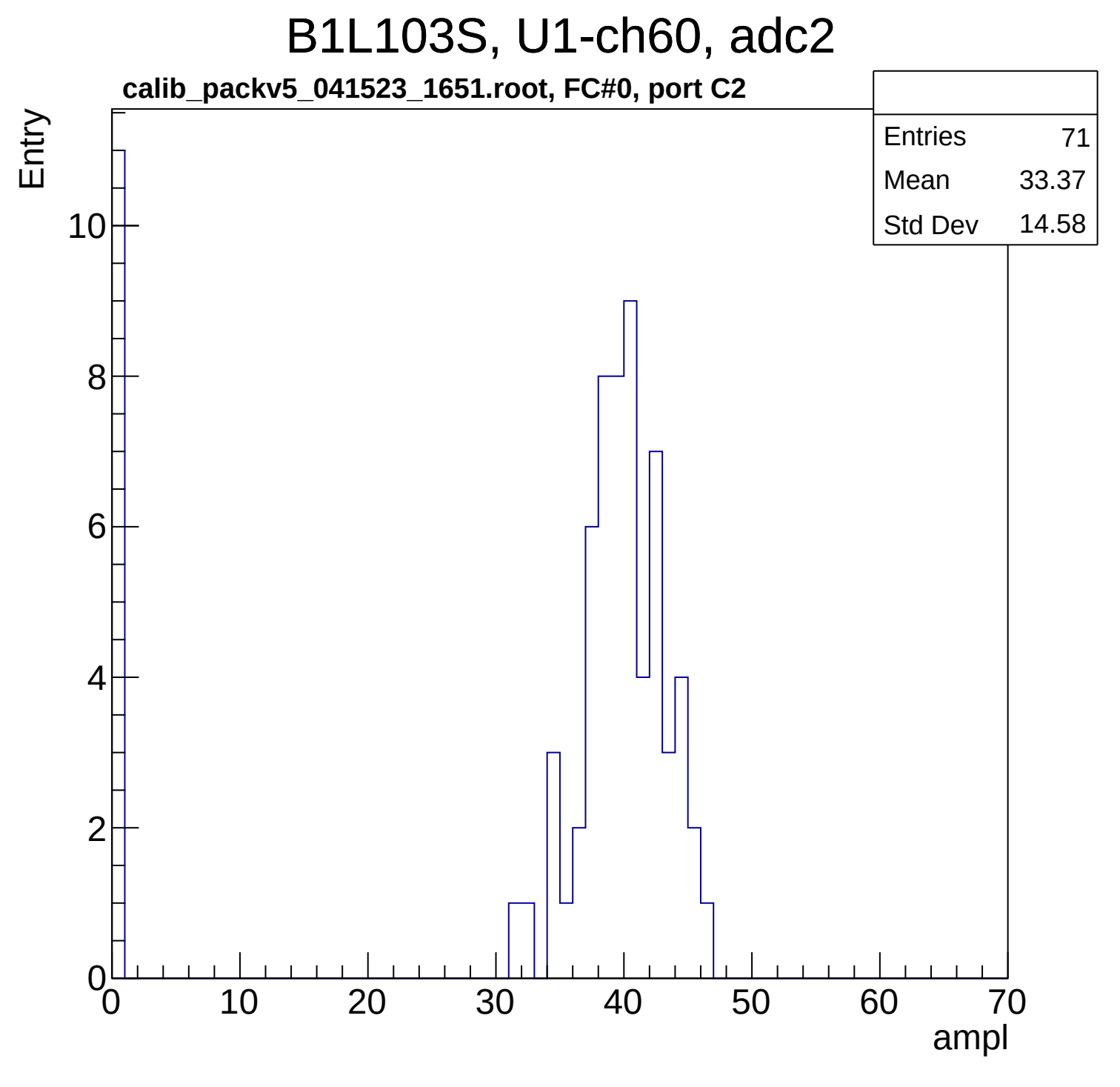
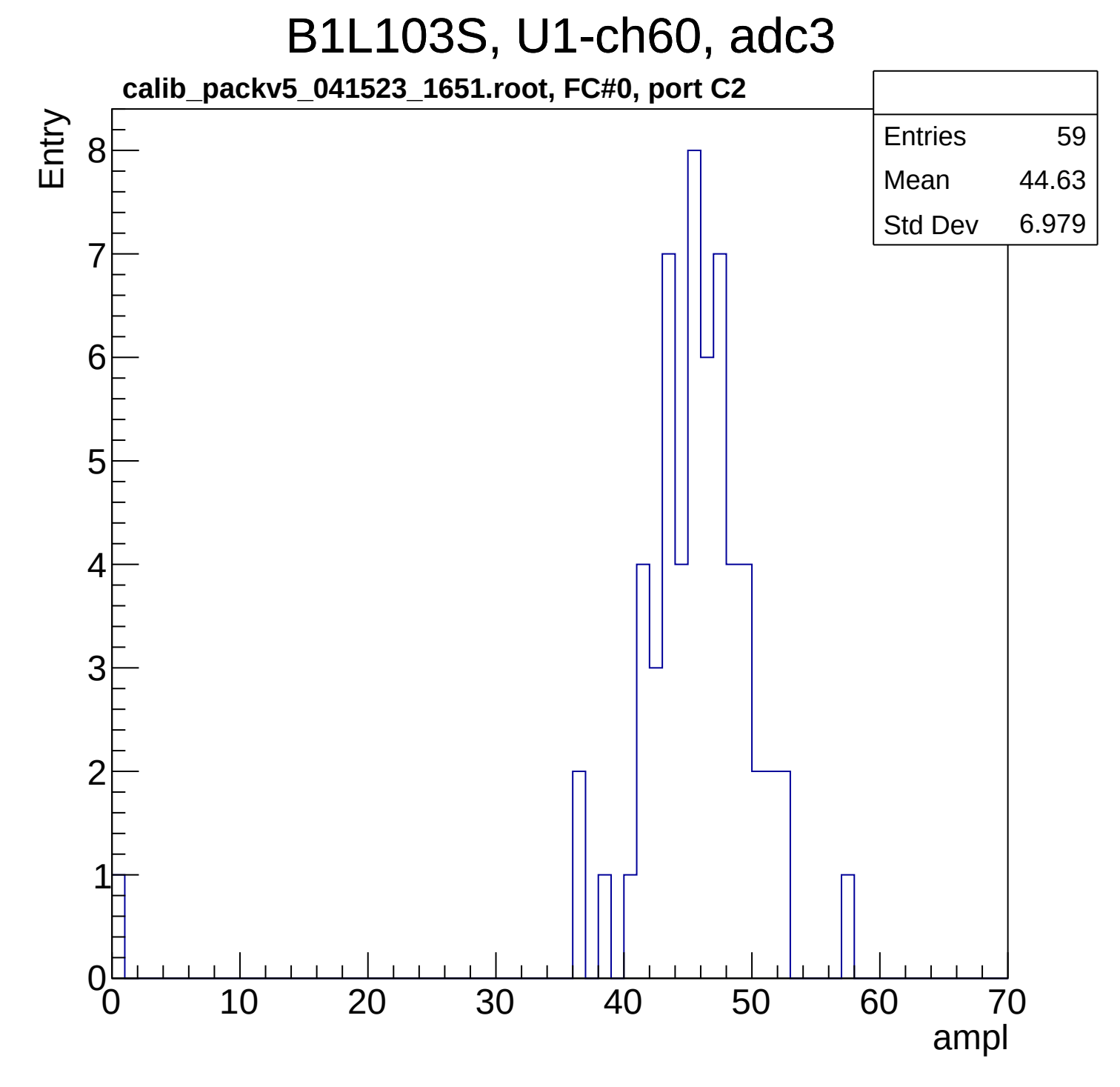

B1L103S, U1-ch60, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 33.37
Std Dev 14.58
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch60, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 44.63
Std Dev 6.979
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
30
40
50
60
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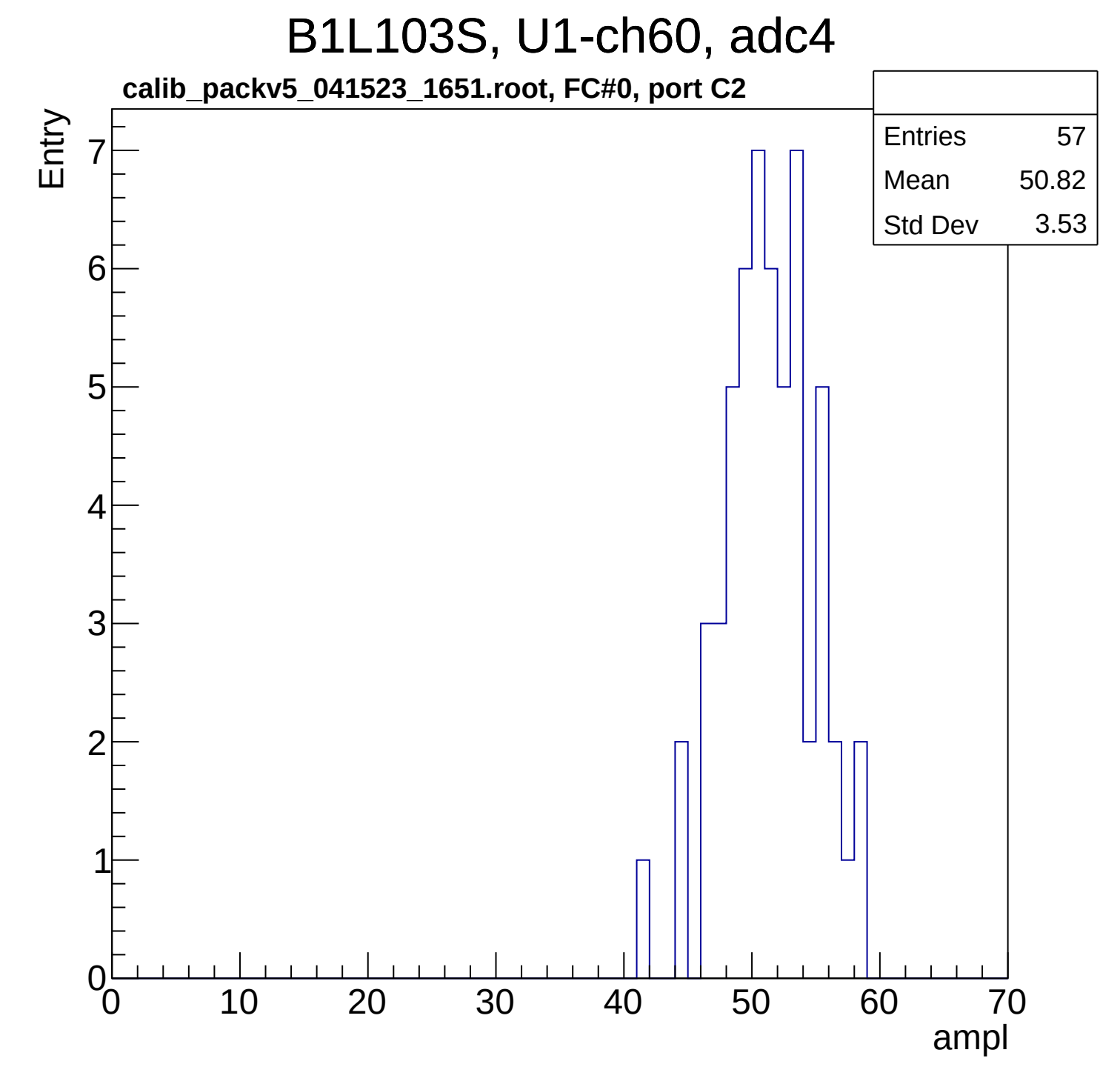
B1L103S, U1-ch60, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 50.82
Std Dev 3.53
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
30
40
50
60
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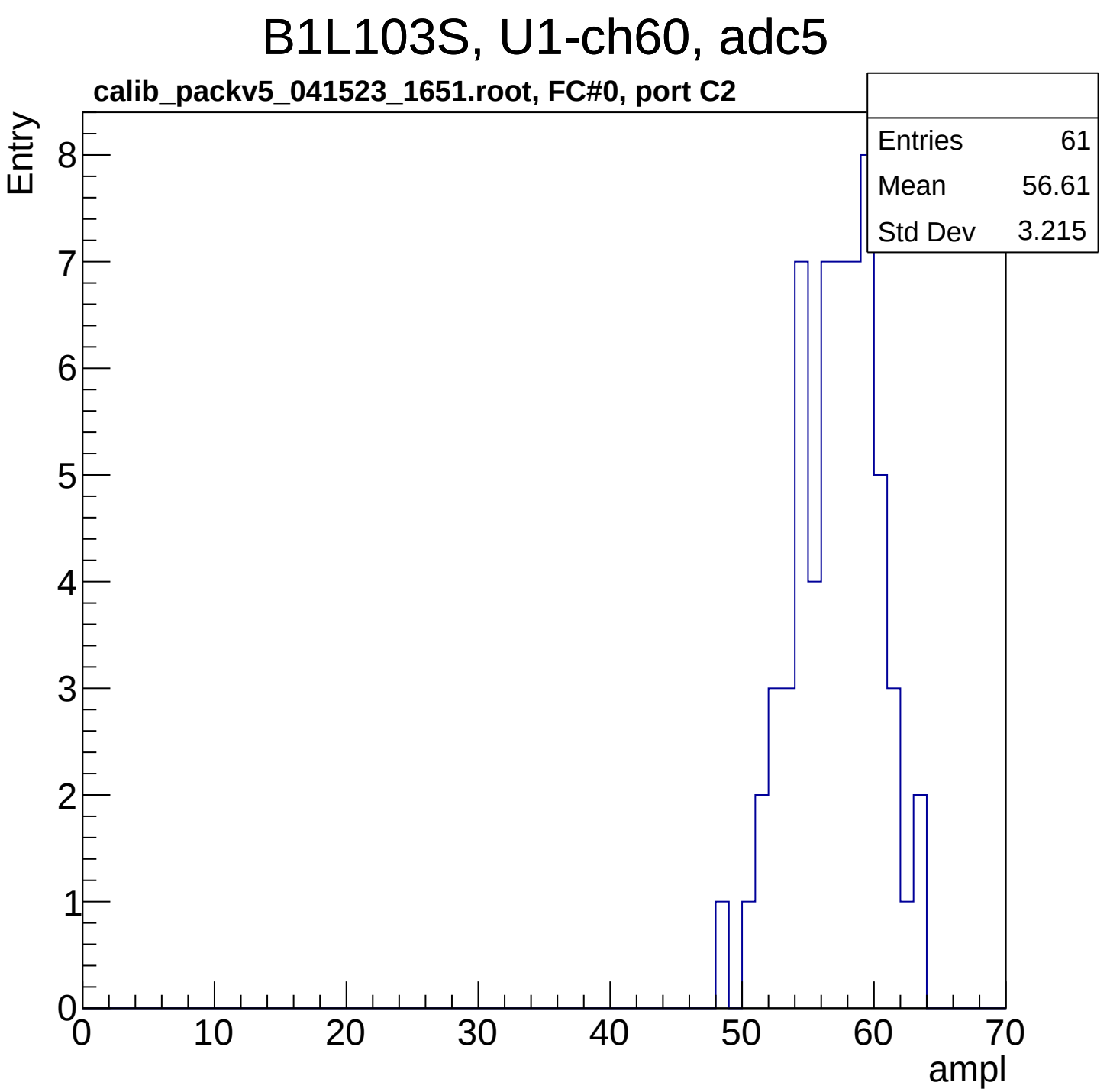
B1L103S, U1-ch60, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 56.61
Std Dev 3.215
Entry
ampl
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2
3
4
5
6
7
8
0
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20
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40
50
60
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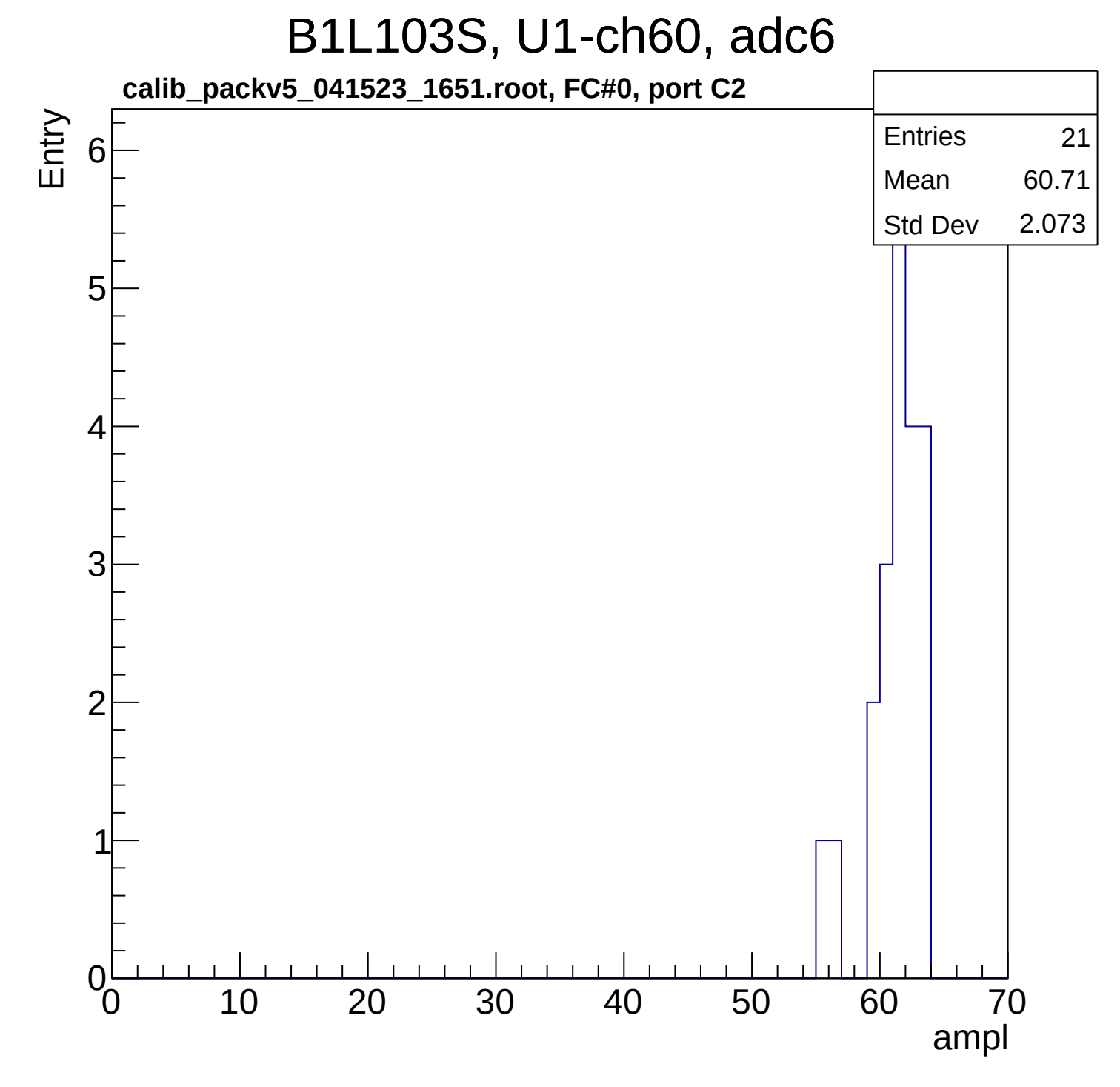
B1L103S, U1-ch60, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 60.71
Std Dev 2.073
Entry
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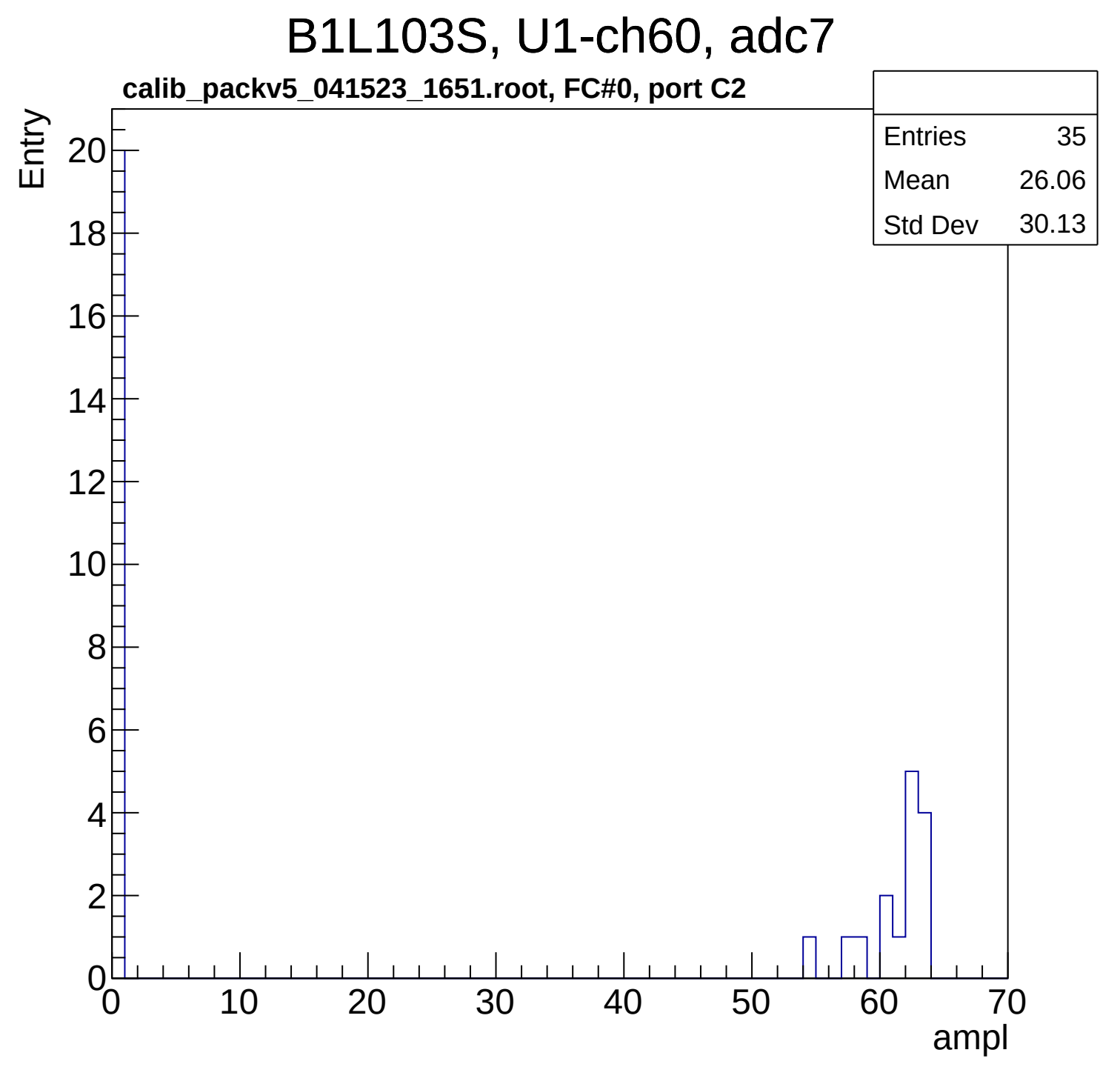
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch60, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 35
Mean 26.06
Std Dev 30.13
Entry
ampl
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2
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6
8
10
12
14
16
18
20
0
10
20
30
40
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60
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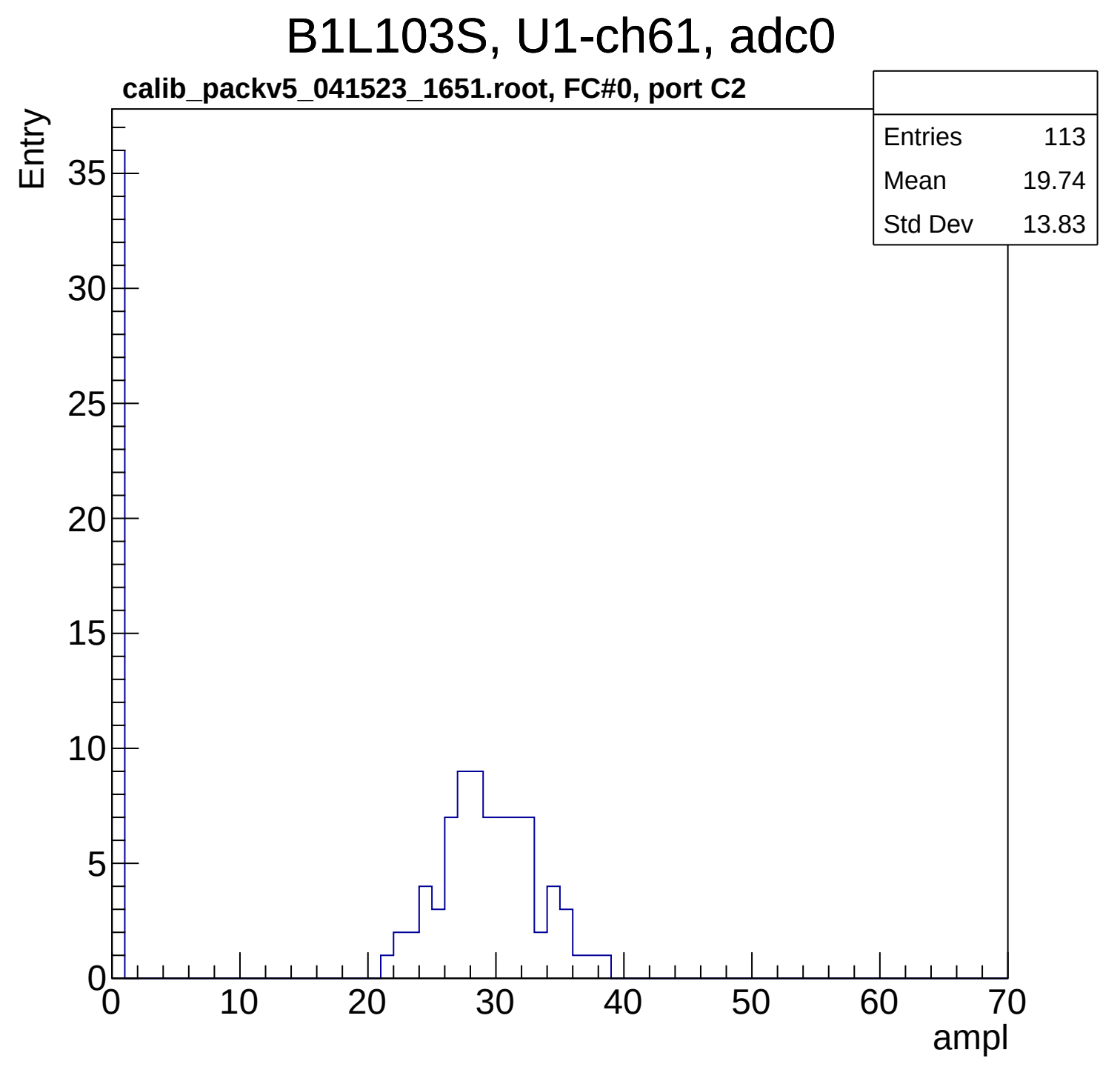
B1L103S, U1-ch61, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 113
Mean 19.74
Std Dev 13.83
Entry
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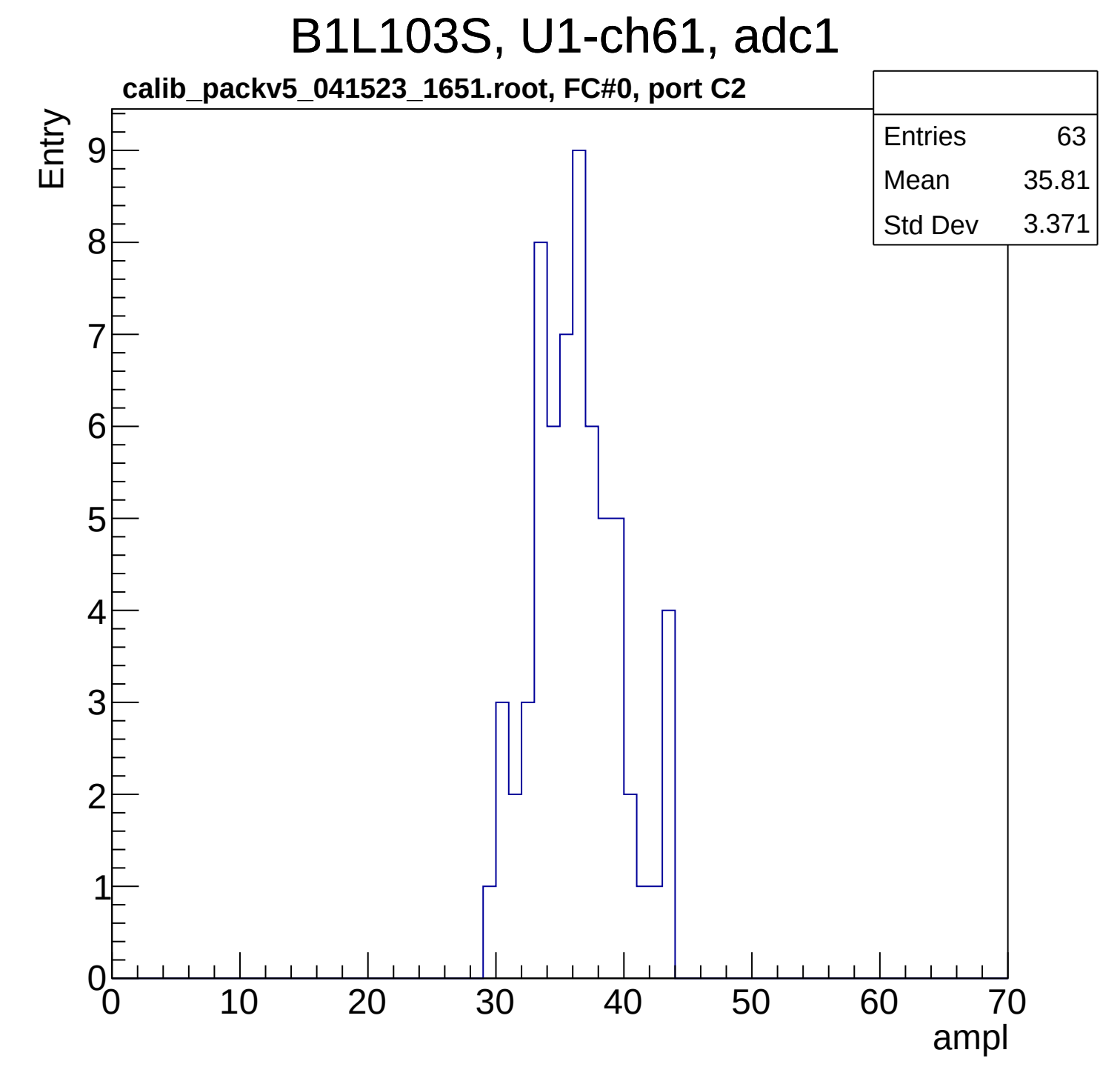
5
10
15
20
25
30
35
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch61, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 35.81
Std Dev 3.371
Entry
ampl
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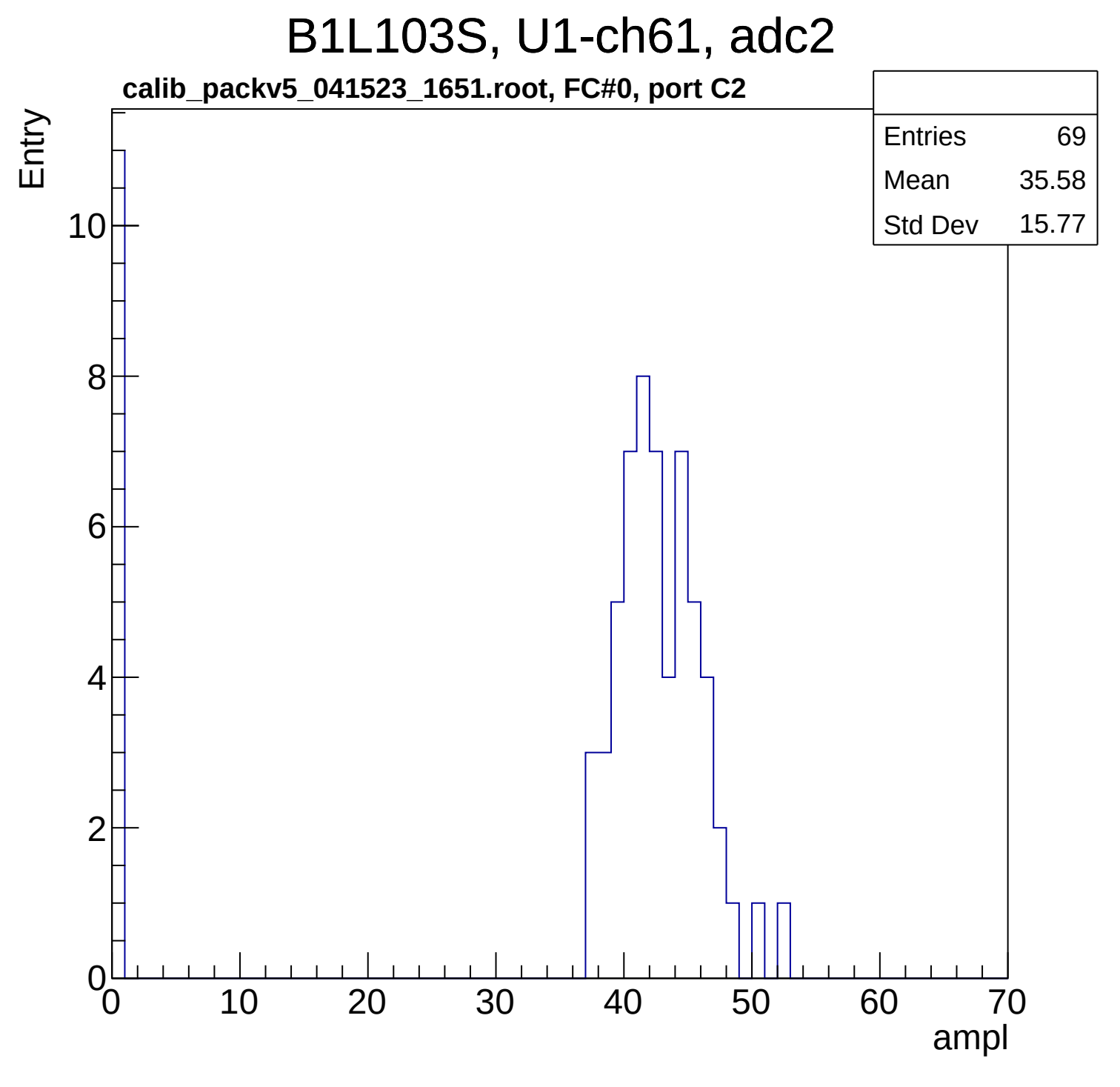
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9


B1L103S, U1-ch61, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 35.58
Std Dev 15.77
Entry
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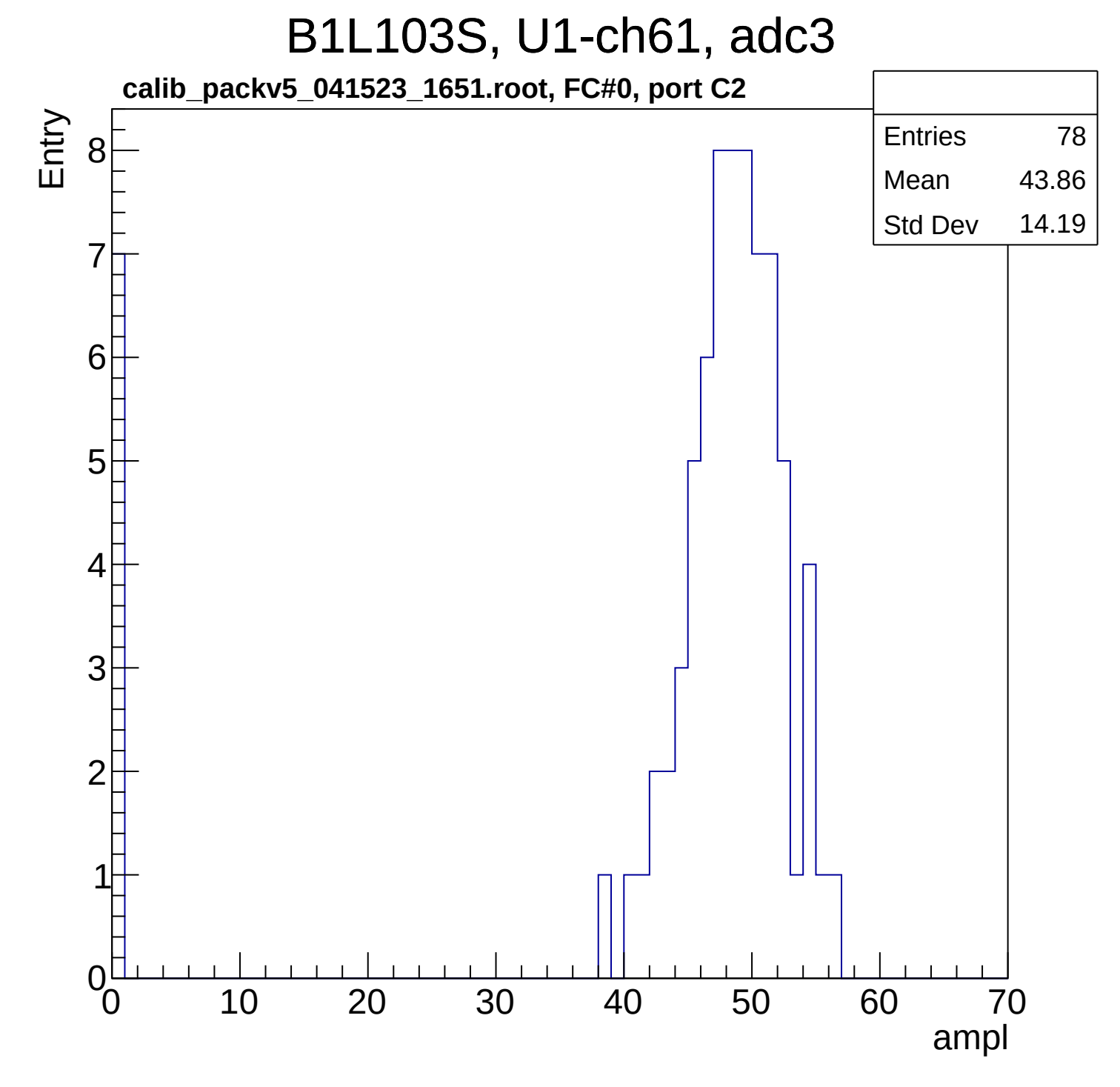
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch61, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 43.86
Std Dev 14.19
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
30
40
50
60
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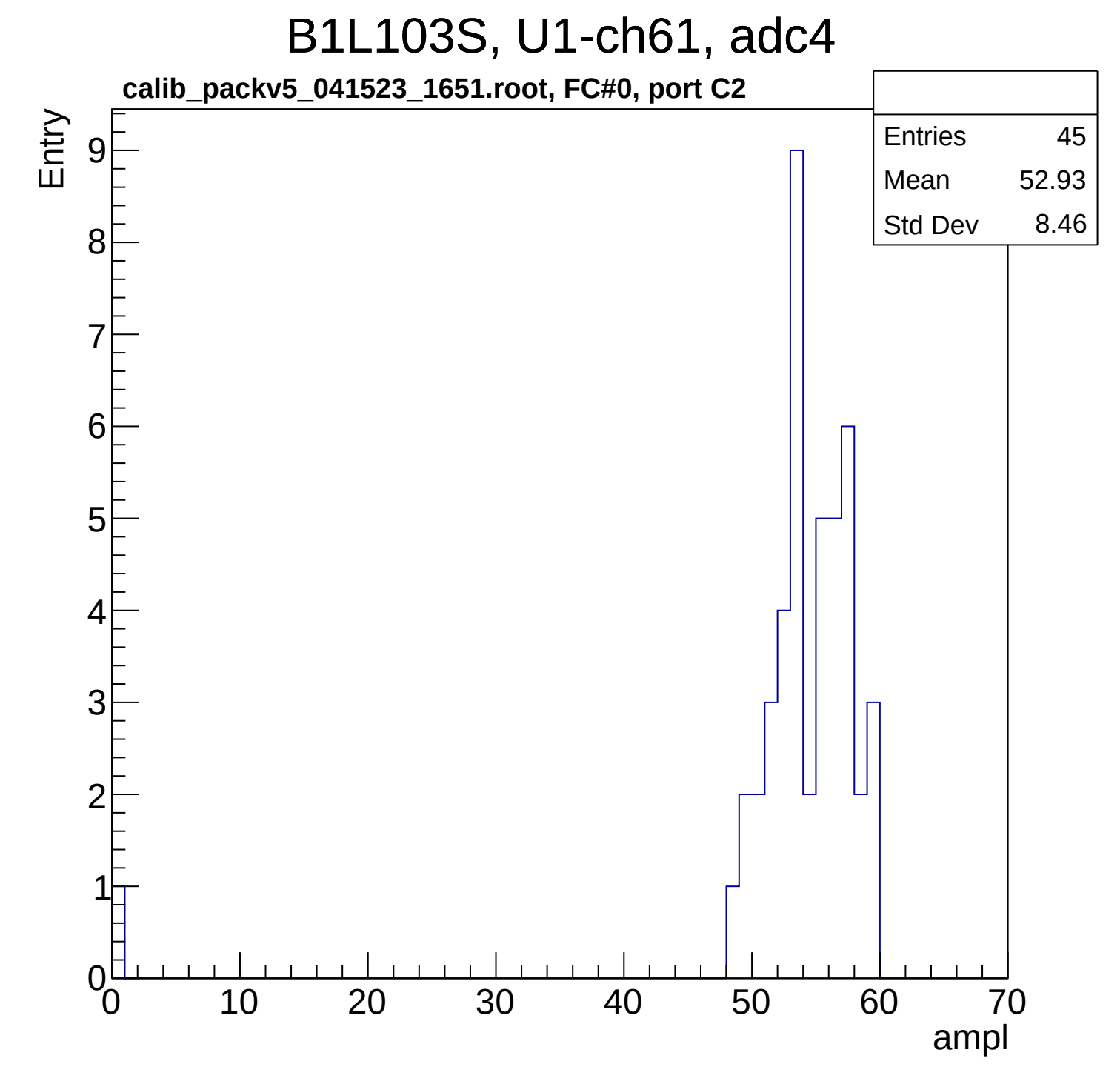
B1L103S, U1-ch61, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 52.93
Std Dev 8.46
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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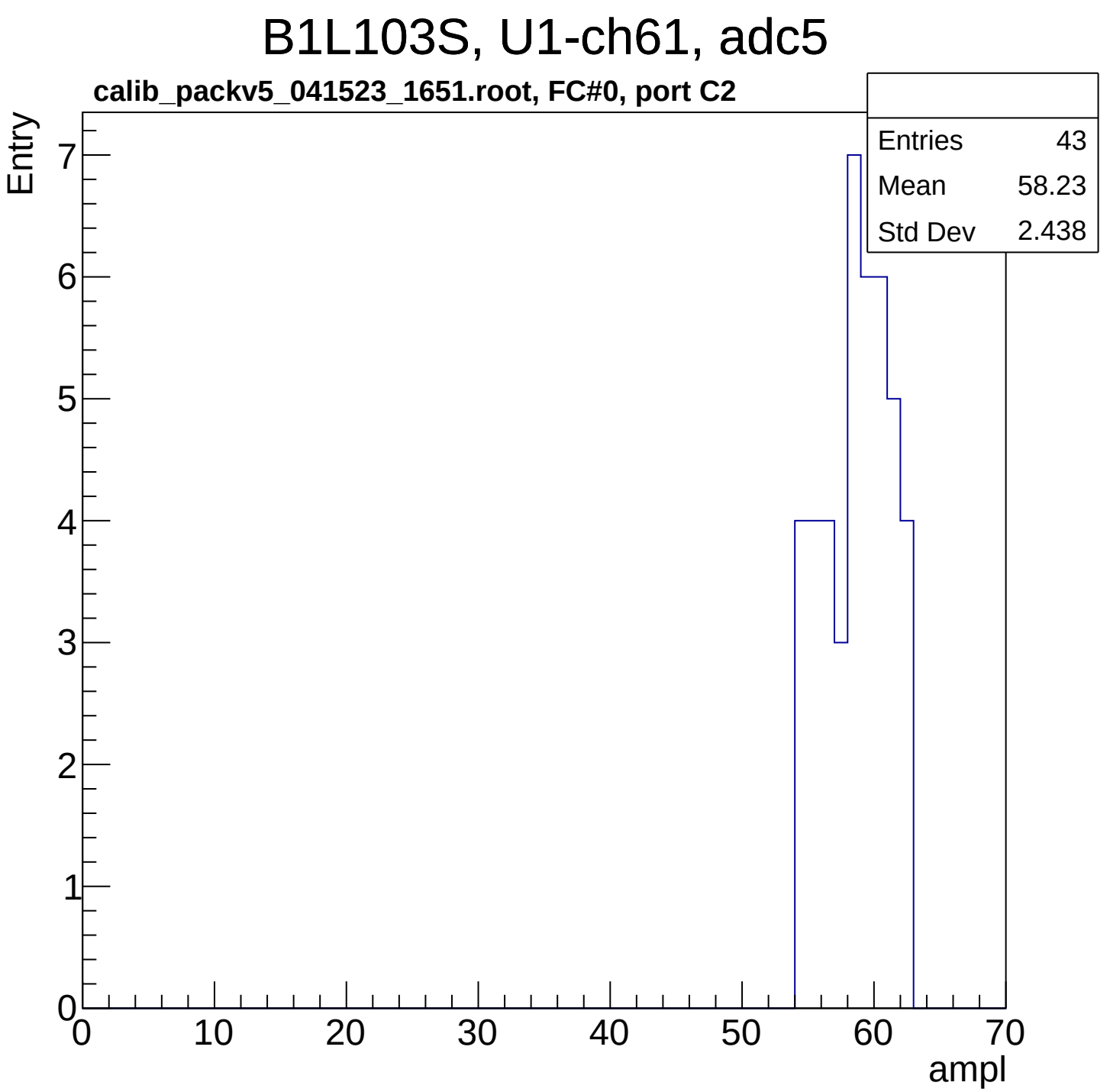
B1L103S, U1-ch61, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 43
Mean 58.23
Std Dev 2.438
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
30
40
50
60
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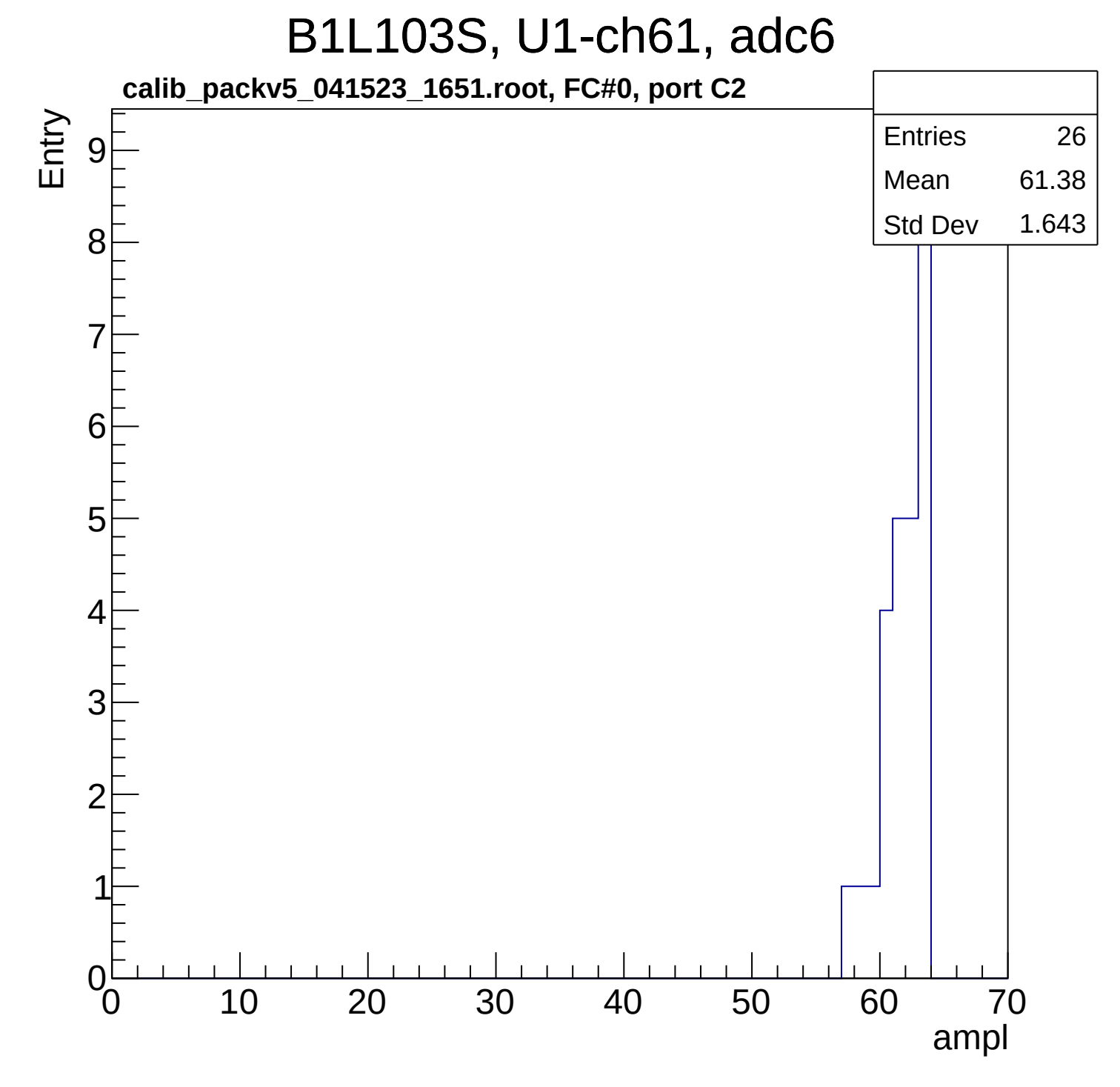
B1L103S, U1-ch61, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 26
Mean 61.38
Std Dev 1.643
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
50
60
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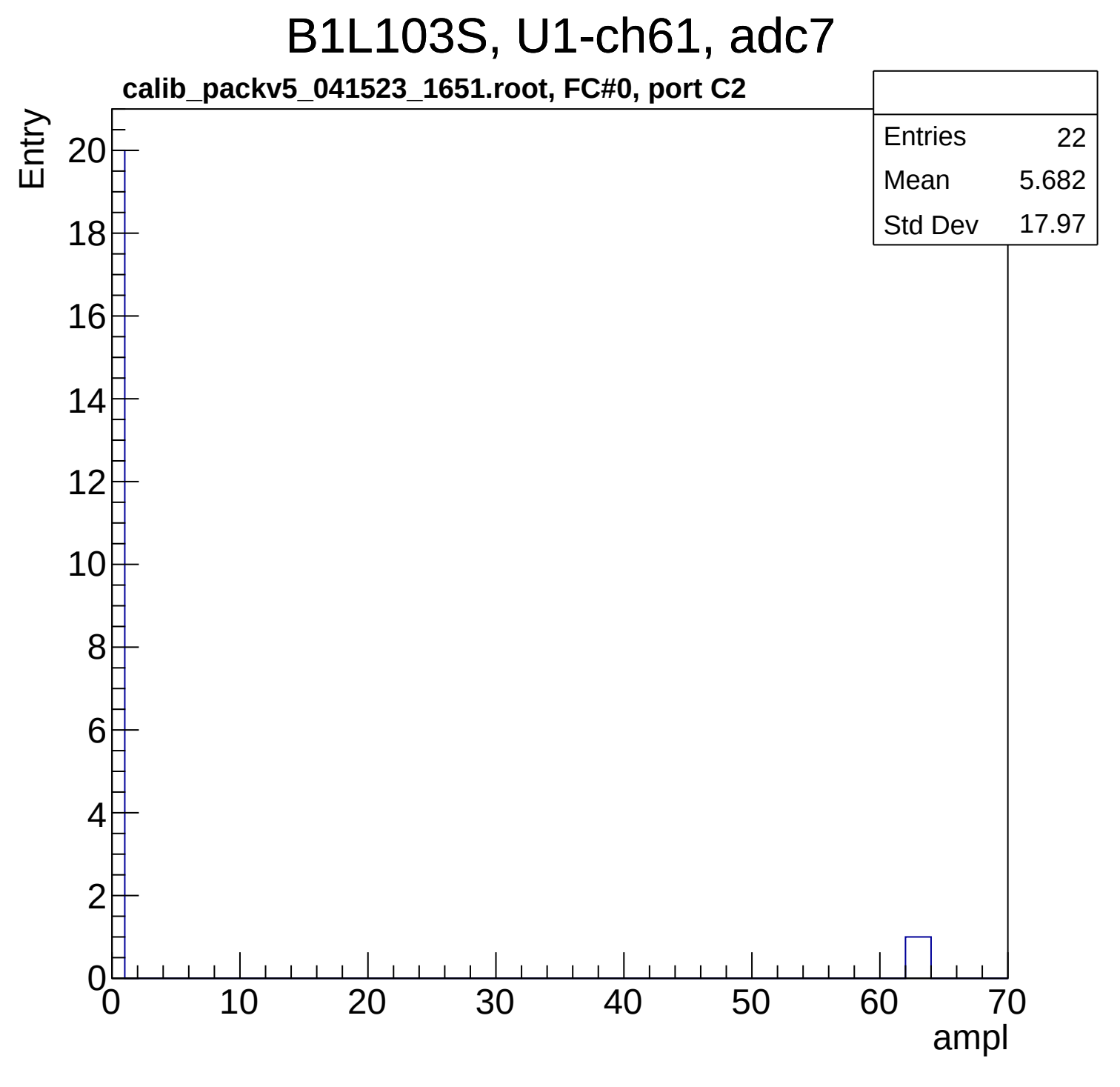
B1L103S, U1-ch61, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 5.682
Std Dev 17.97
Entry
0
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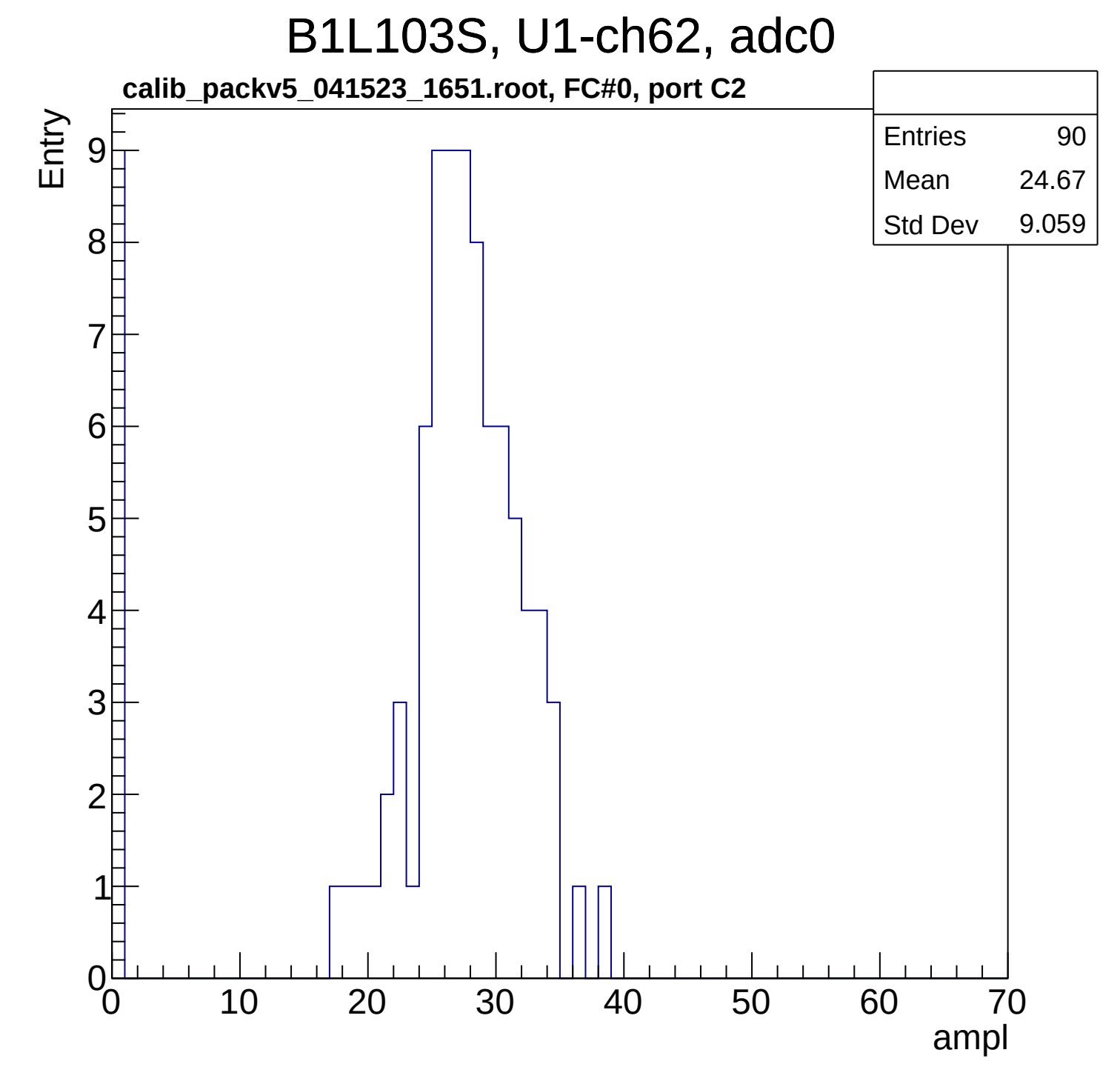
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch62, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 90
Mean 24.67
Std Dev 9.059
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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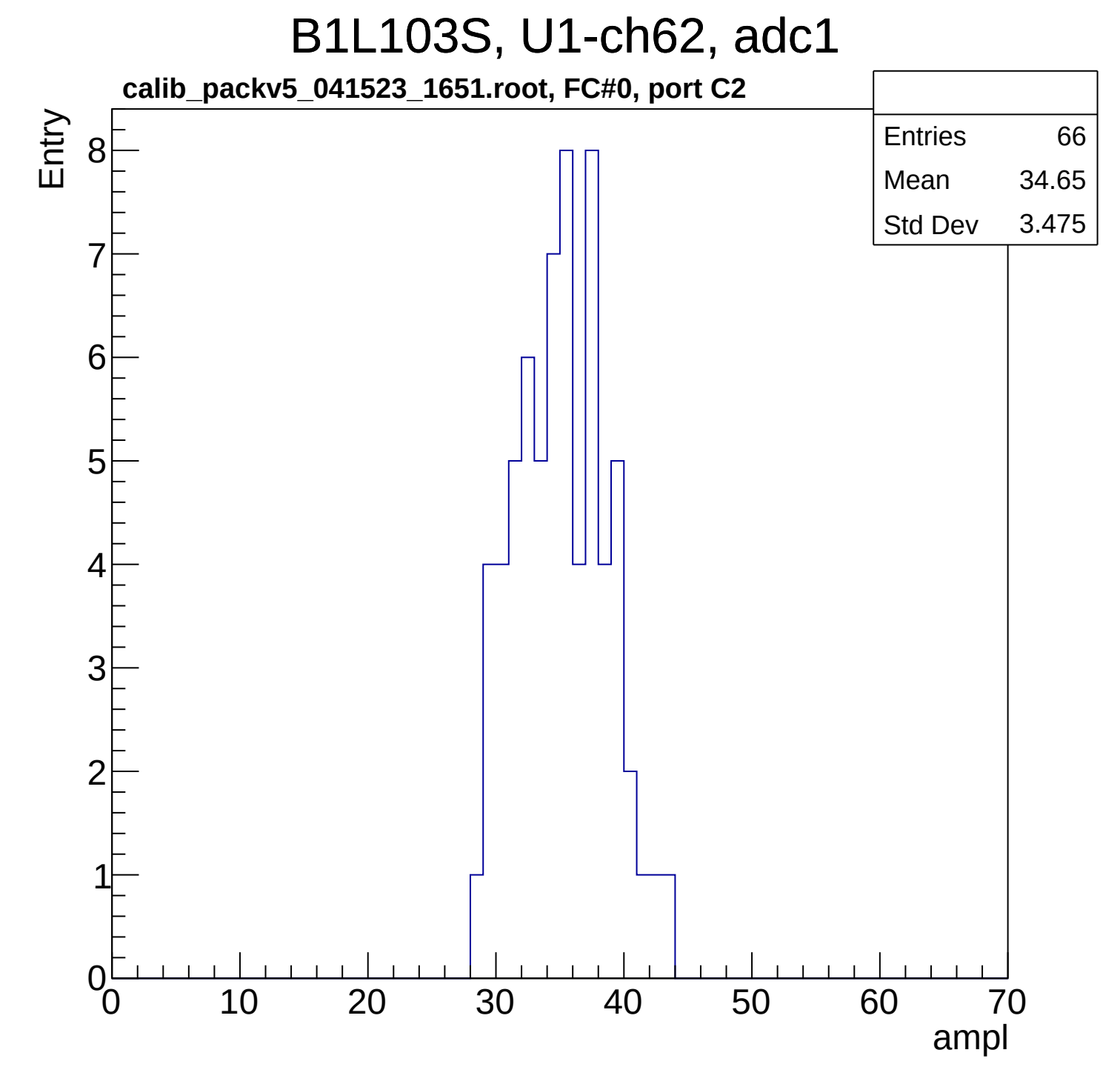
40
50
60
70


B1L103S, U1-ch62, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 34.65
Std Dev 3.475
Entry
ampl
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4
5
6
7
8
0
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20
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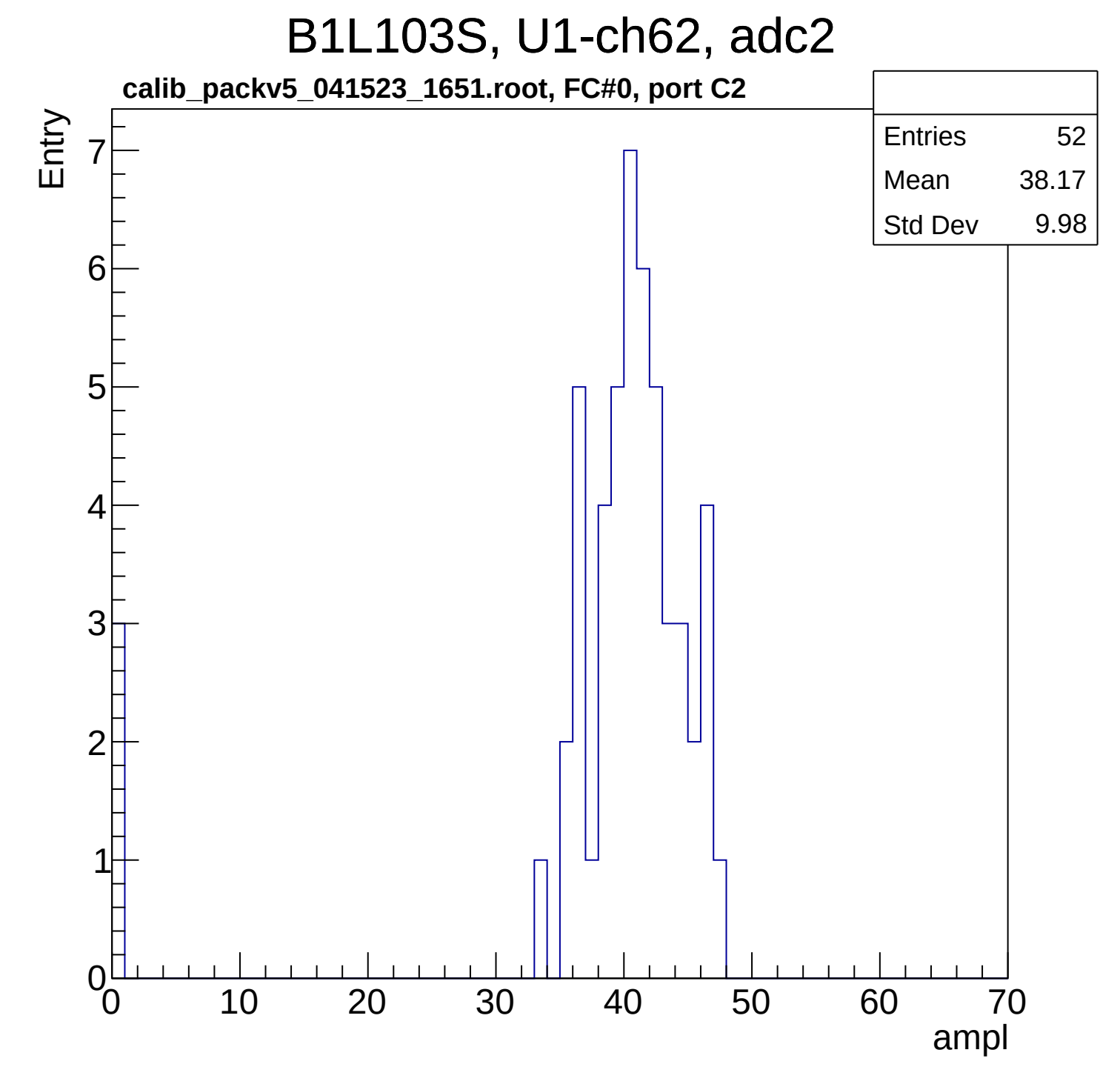
40
50
60
70


B1L103S, U1-ch62, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 38.17
Std Dev 9.98
Entry
ampl
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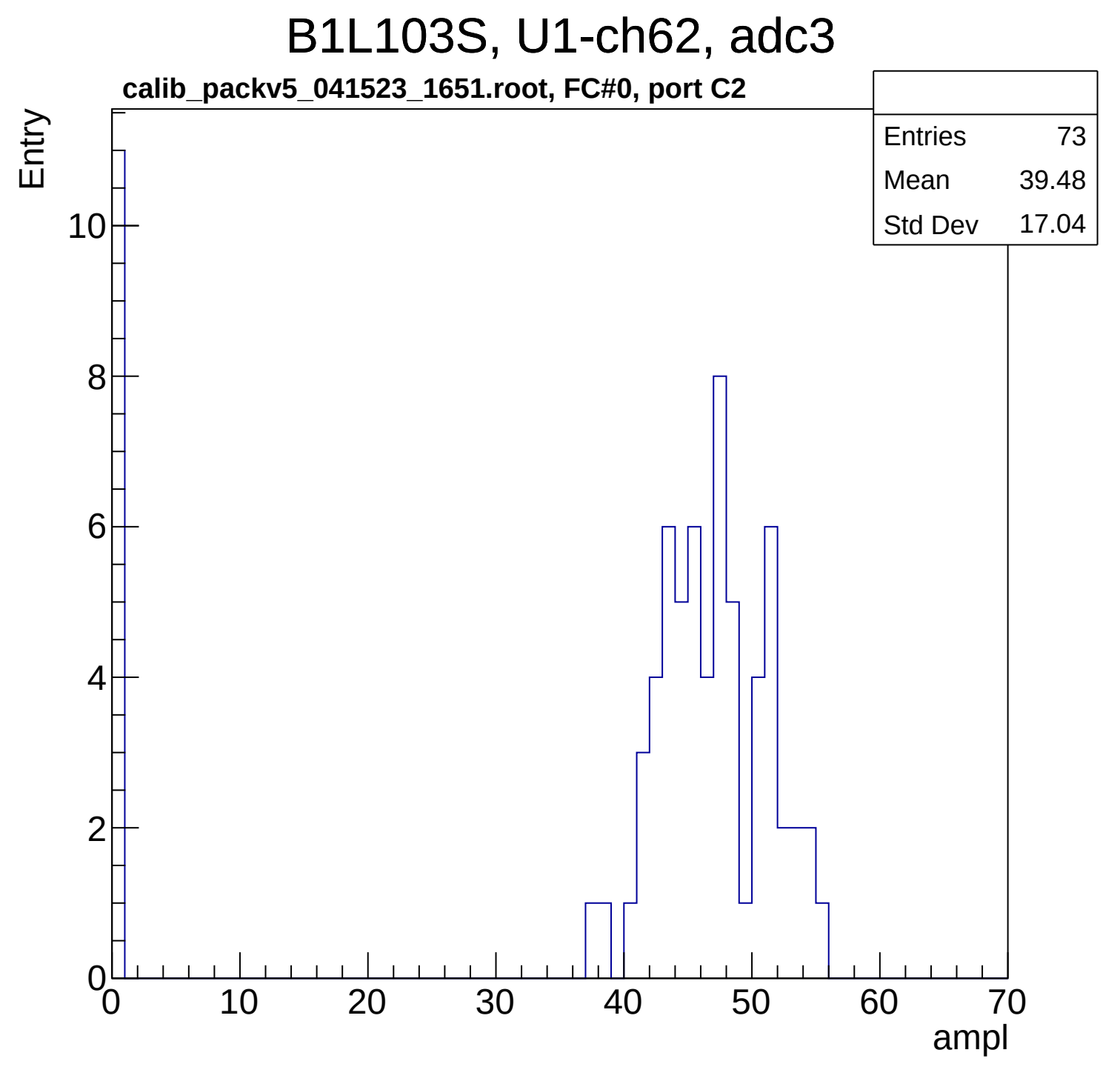
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U1-ch62, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 39.48
Std Dev 17.04
Entry
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4
6
8
10
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10
20
30
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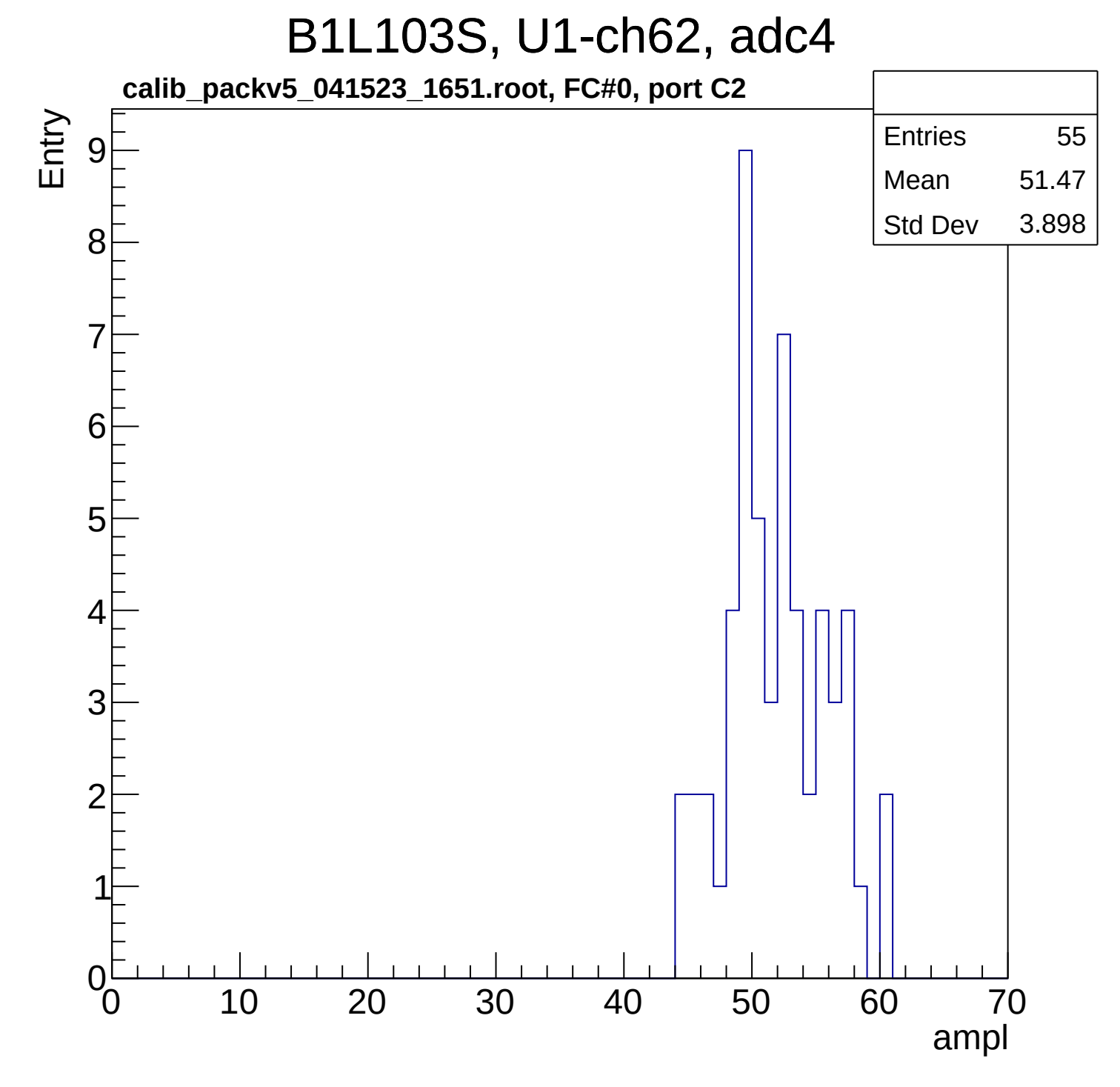
50
60
70
ampl


B1L103S, U1-ch62, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 51.47
Std Dev 3.898
Entry
ampl
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5
6
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8
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0
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60
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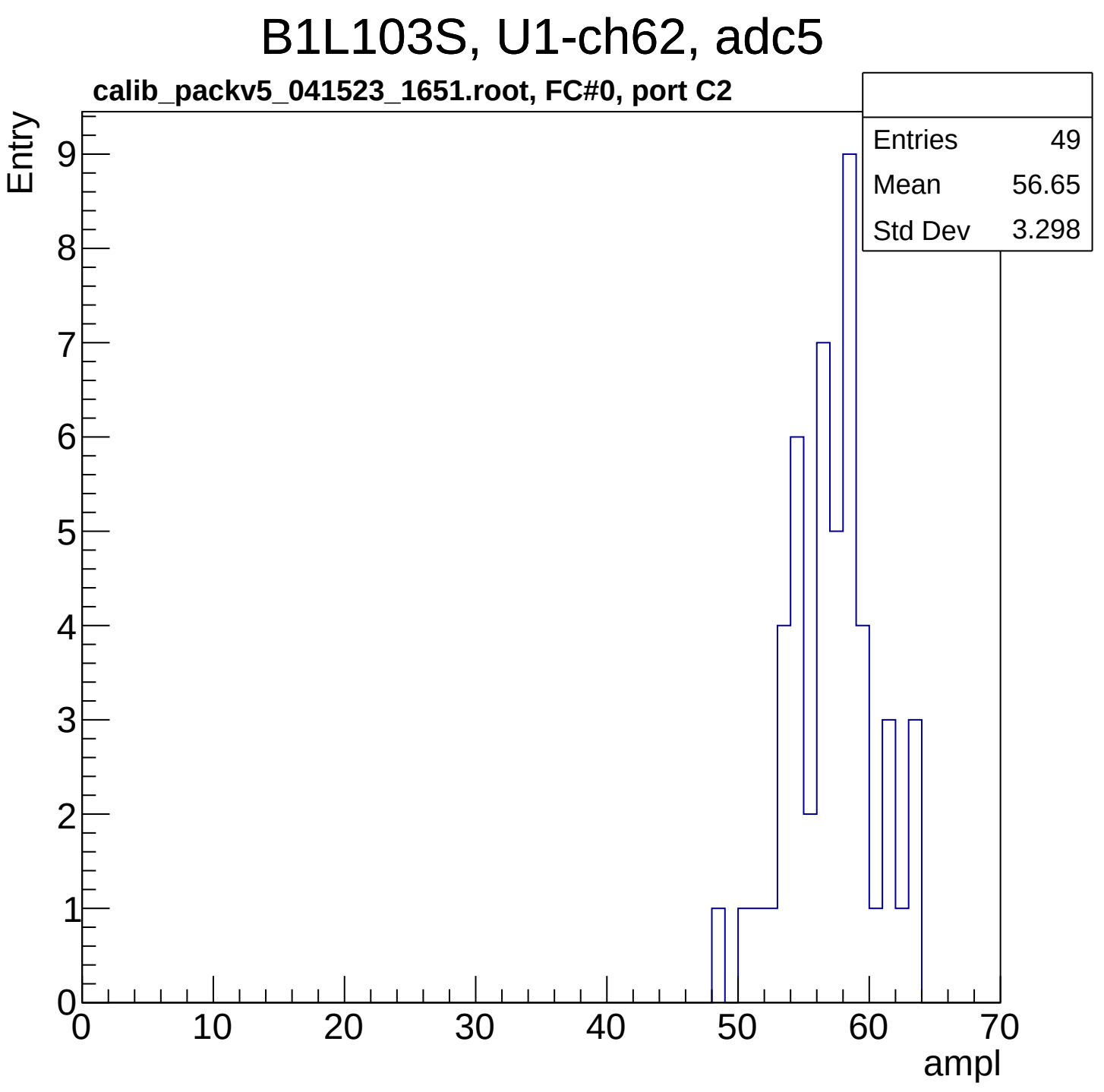
B1L103S, U1-ch62, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 56.65
Std Dev 3.298
Entry
ampl
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4
5
6
7
8
9
0
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60
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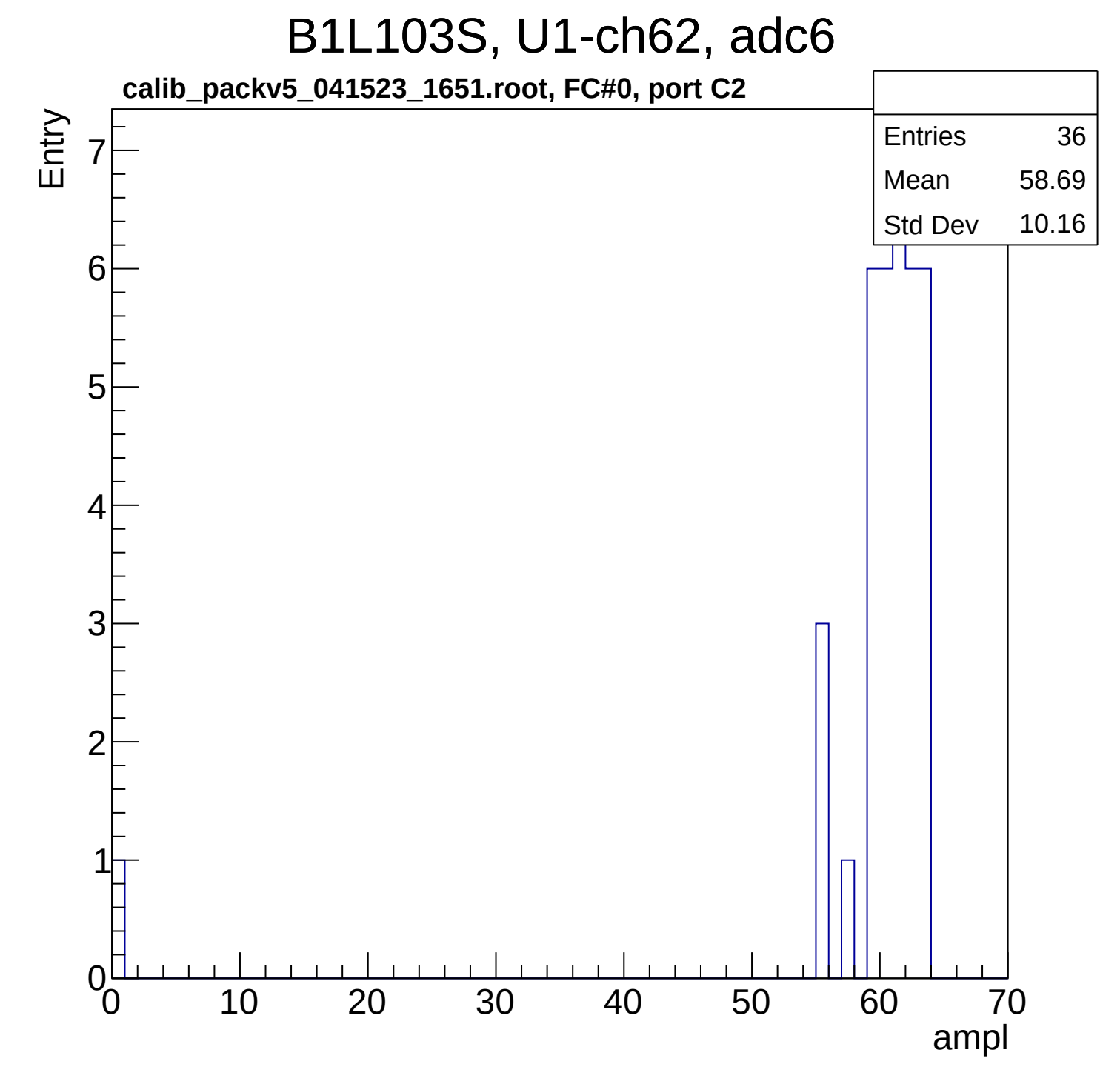
B1L103S, U1-ch62, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 36
Mean 58.69
Std Dev 10.16
Entry
ampl
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2
3
4
5
6
7
0
10
20
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40
50
60
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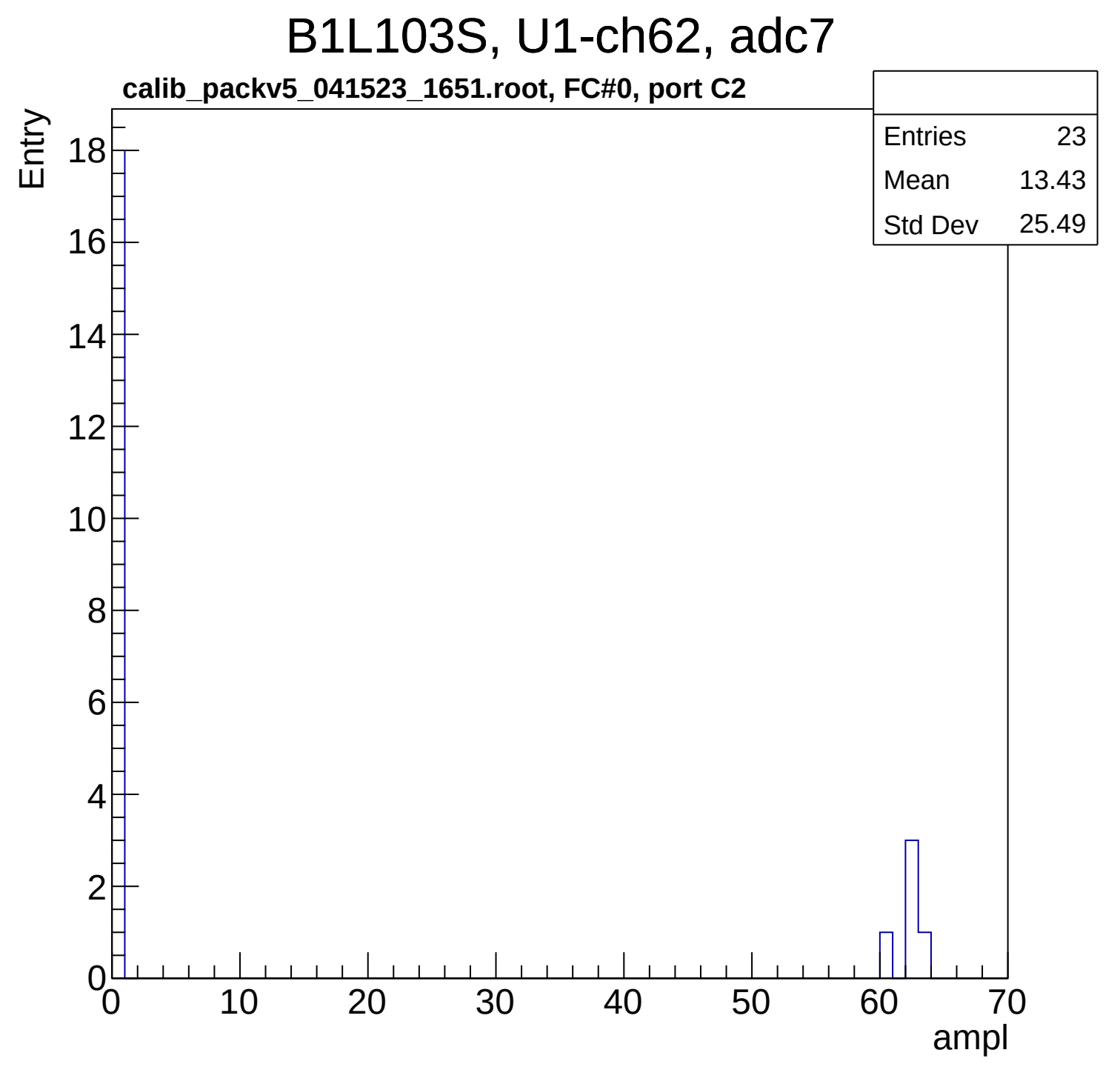
B1L103S, U1-ch62, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 23
Mean 13.43
Std Dev 25.49
Entry
ampl
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6
8
10
12
14
16
18
0
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20
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40
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60
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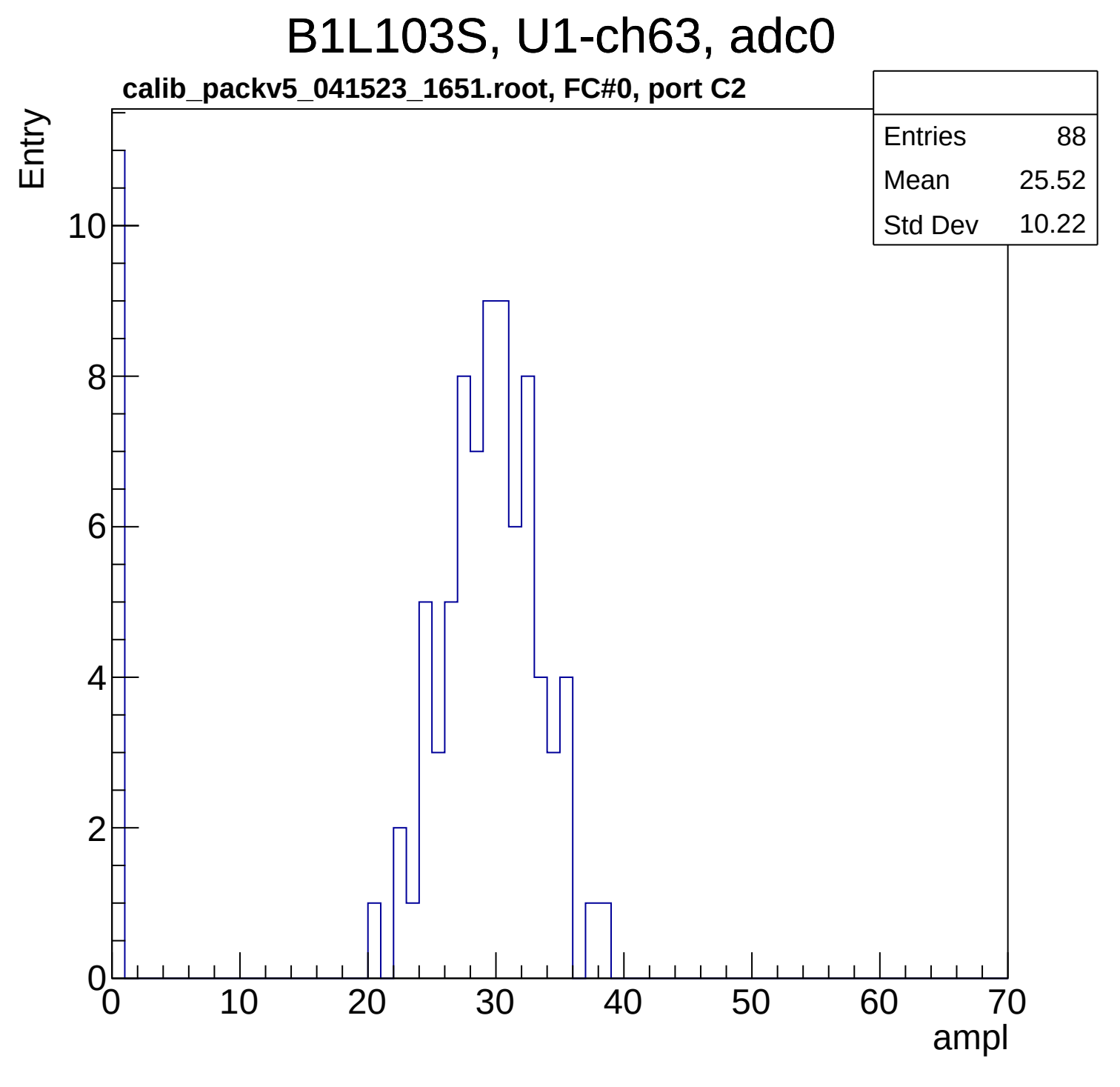
B1L103S, U1-ch63, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 88
Mean 25.52
Std Dev 10.22
Entry
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6
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10
0
10
20
30
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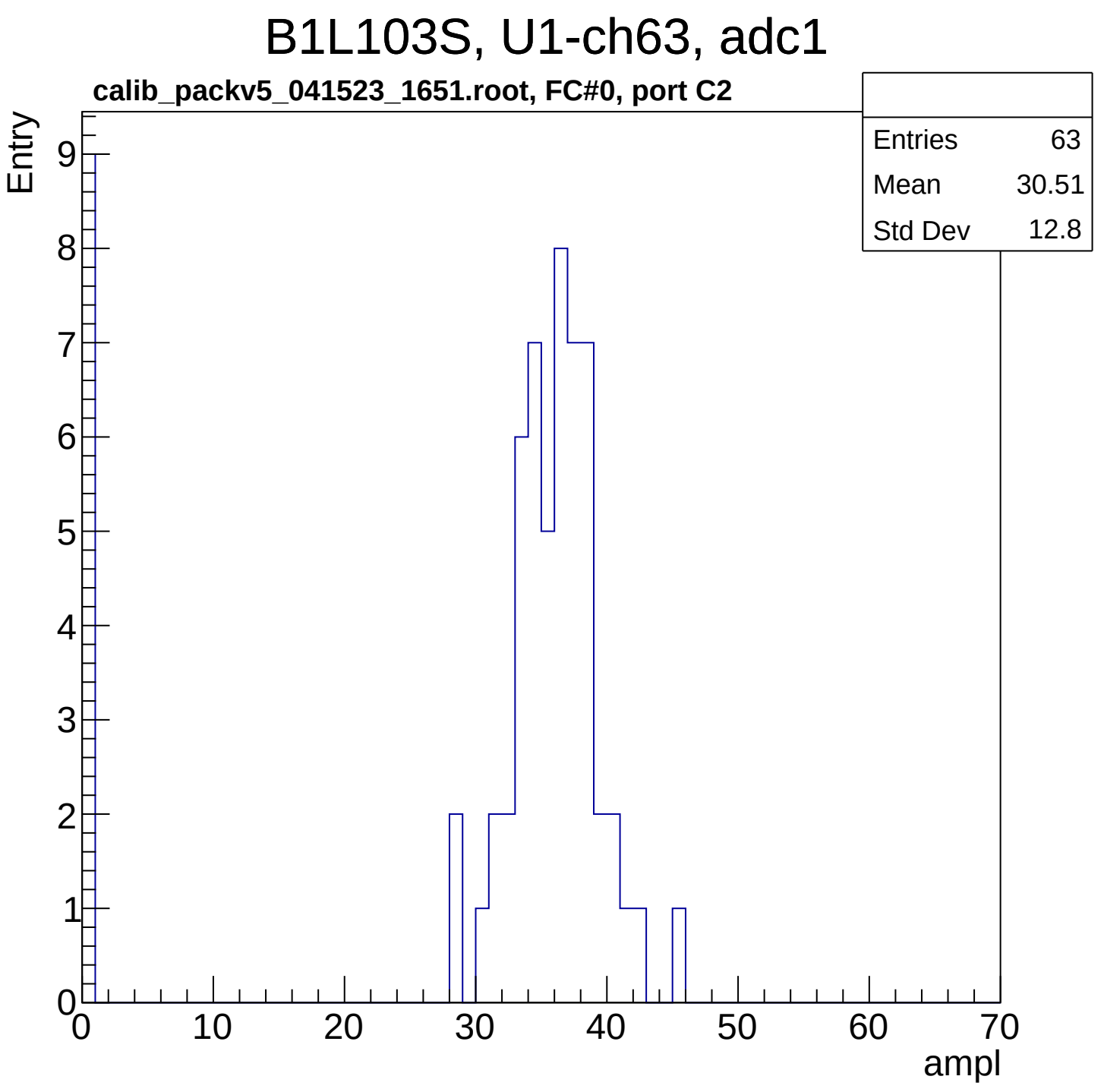
50
60
70
ampl


B1L103S, U1-ch63, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 30.51
Std Dev 12.8
Entry
ampl
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2
3
4
5
6
7
8
9
0
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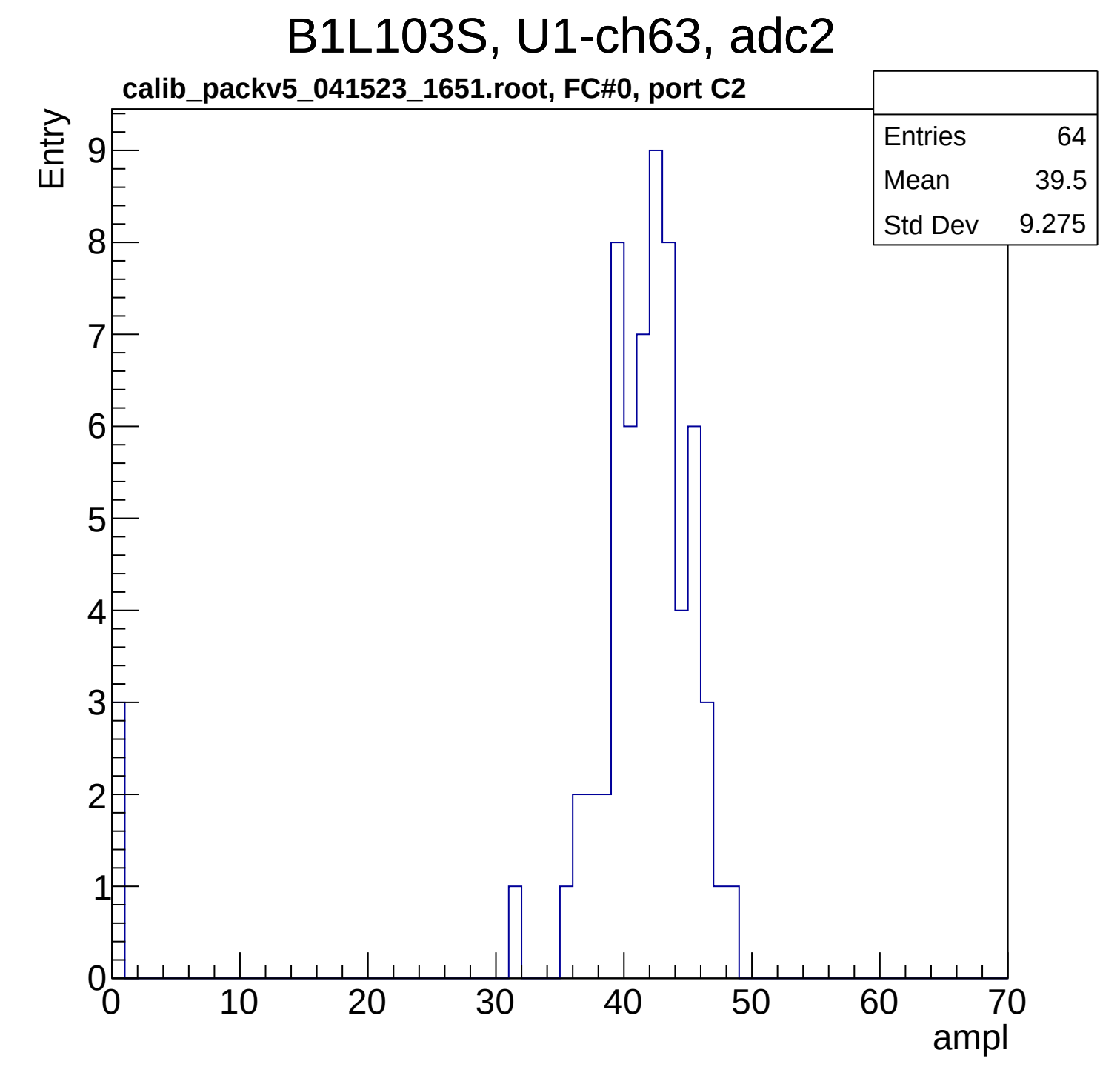
20
30
40
50
60
70


B1L103S, U1-ch63, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 39.5
Std Dev 9.275
Entry
ampl
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3
4
5
6
7
8
9
0
10
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40
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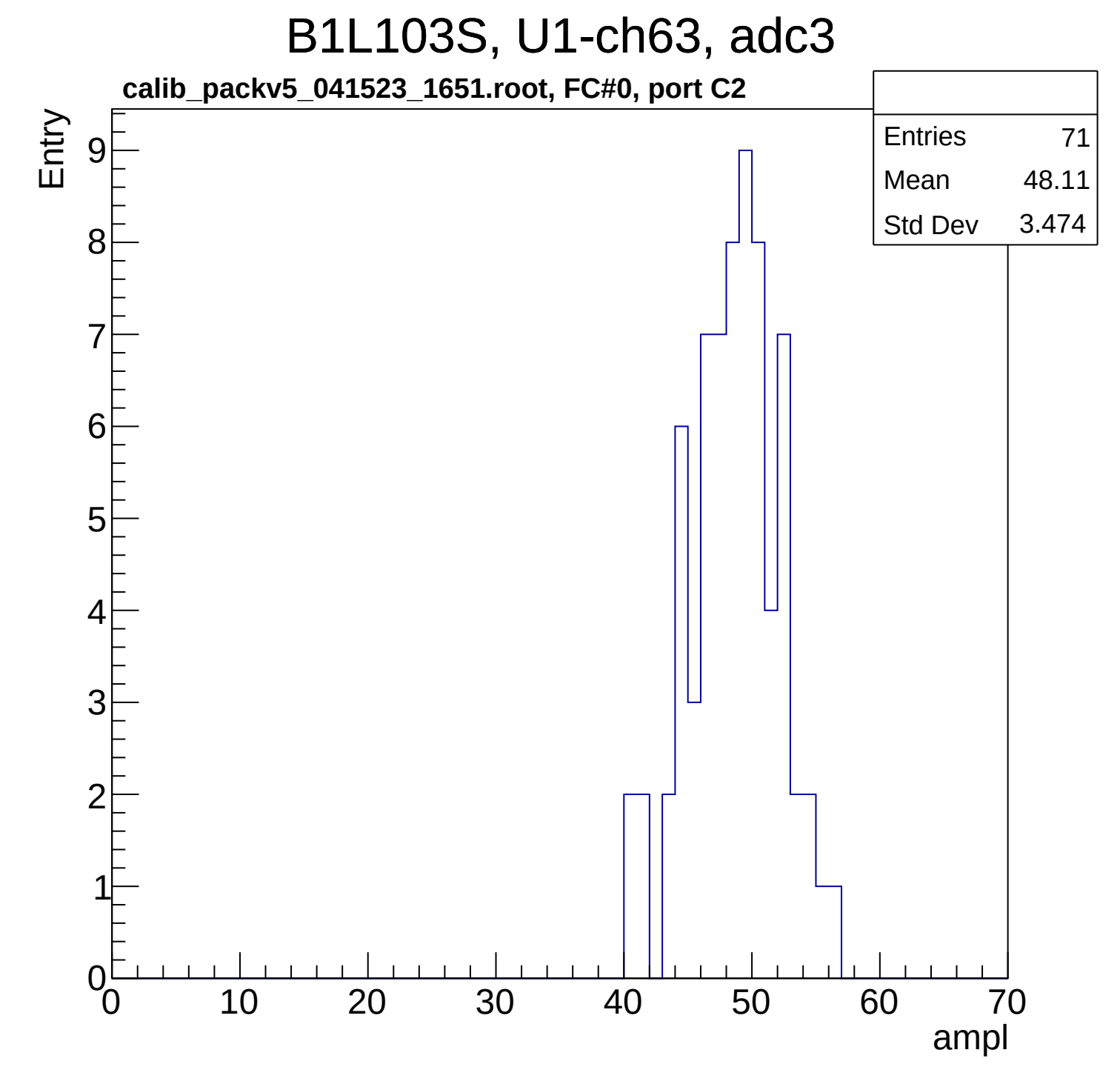
B1L103S, U1-ch63, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 48.11
Std Dev 3.474
Entry
ampl
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3
4
5
6
7
8
9
0
10
20
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40
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60
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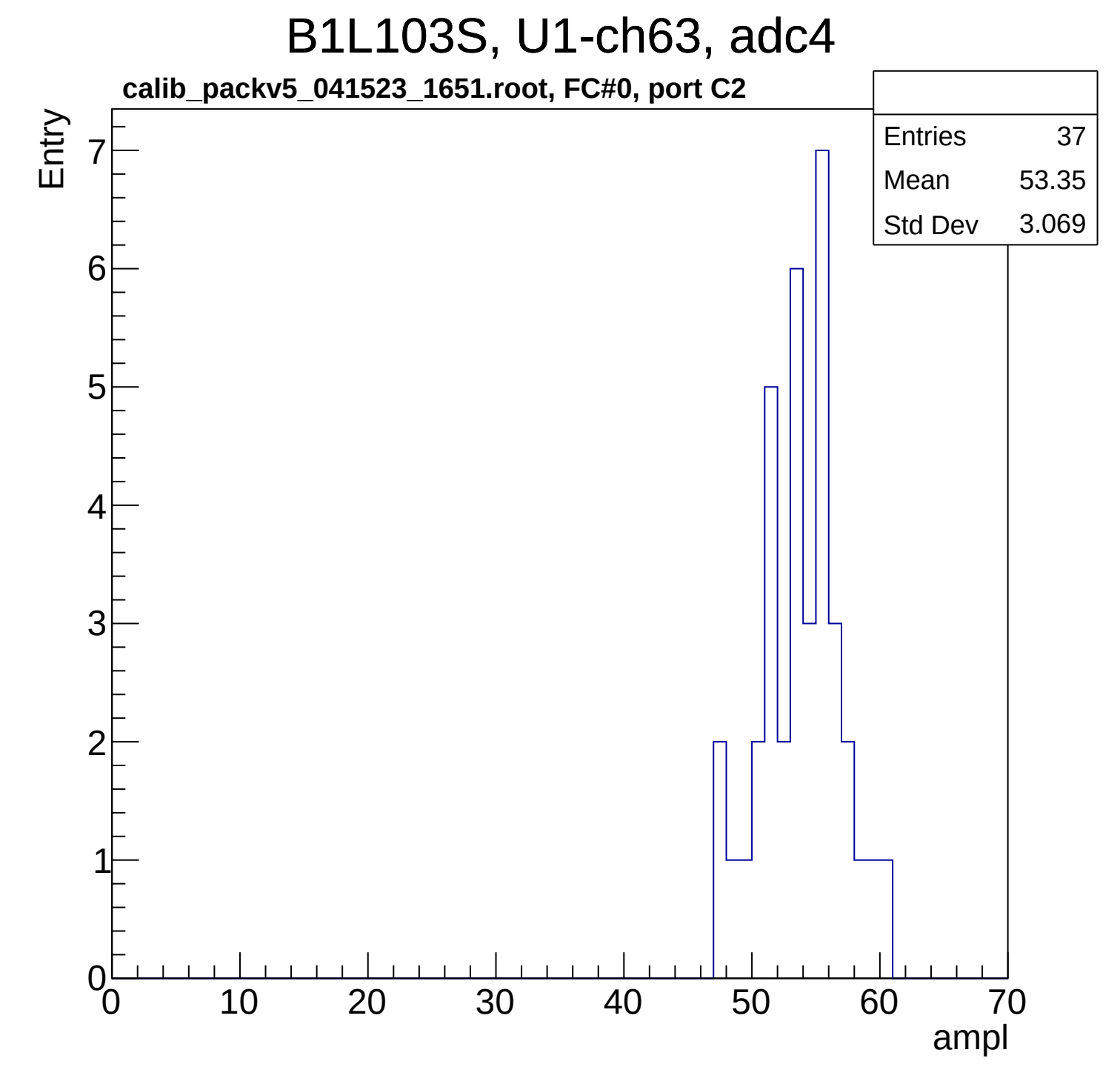
B1L103S, U1-ch63, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 37
Mean 53.35
Std Dev 3.069
Entry
ampl
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1
2
3
4
5
6
7
0
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20
30
40
50
60
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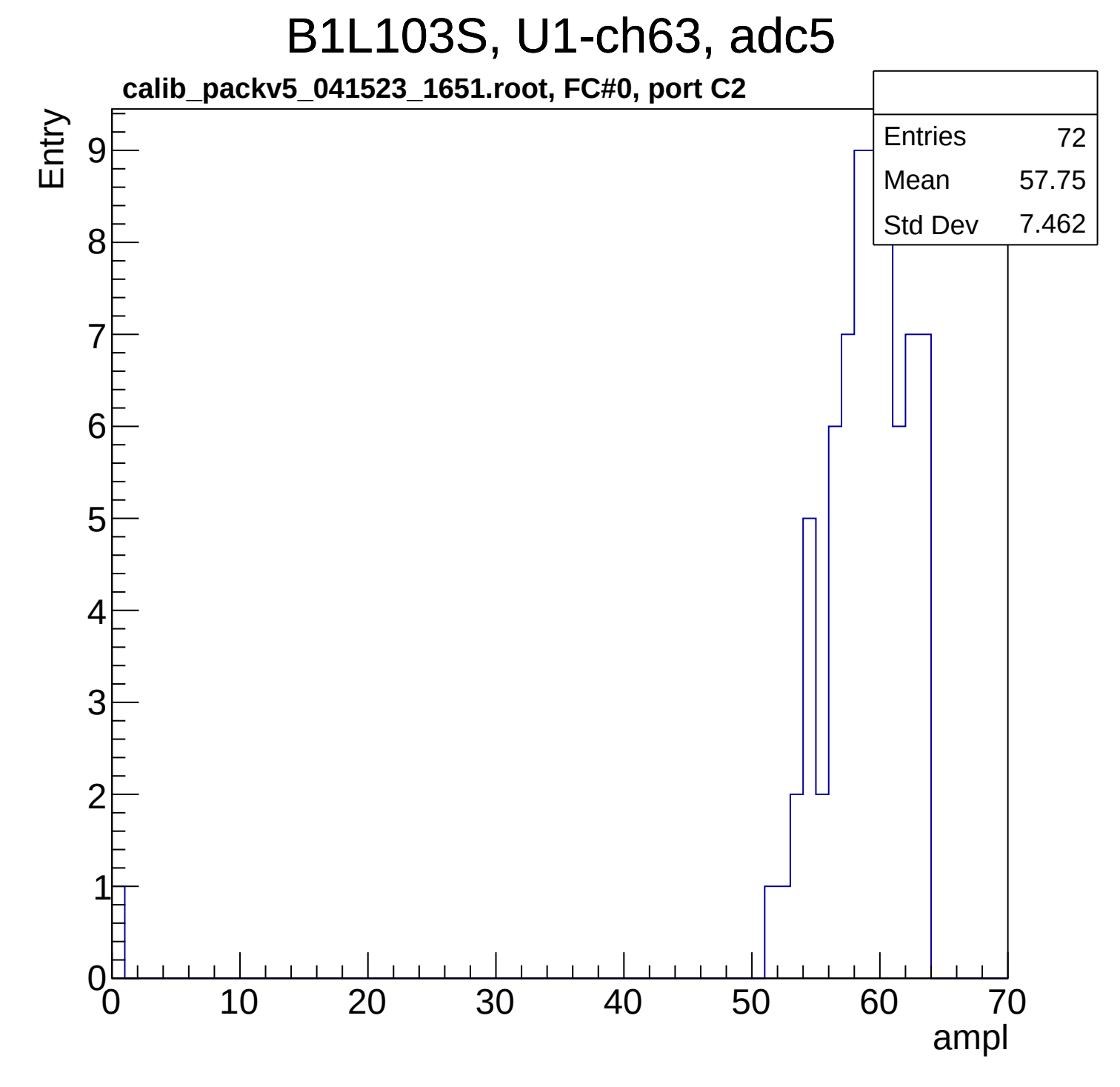
B1L103S, U1-ch63, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 57.75
Std Dev 7.462
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
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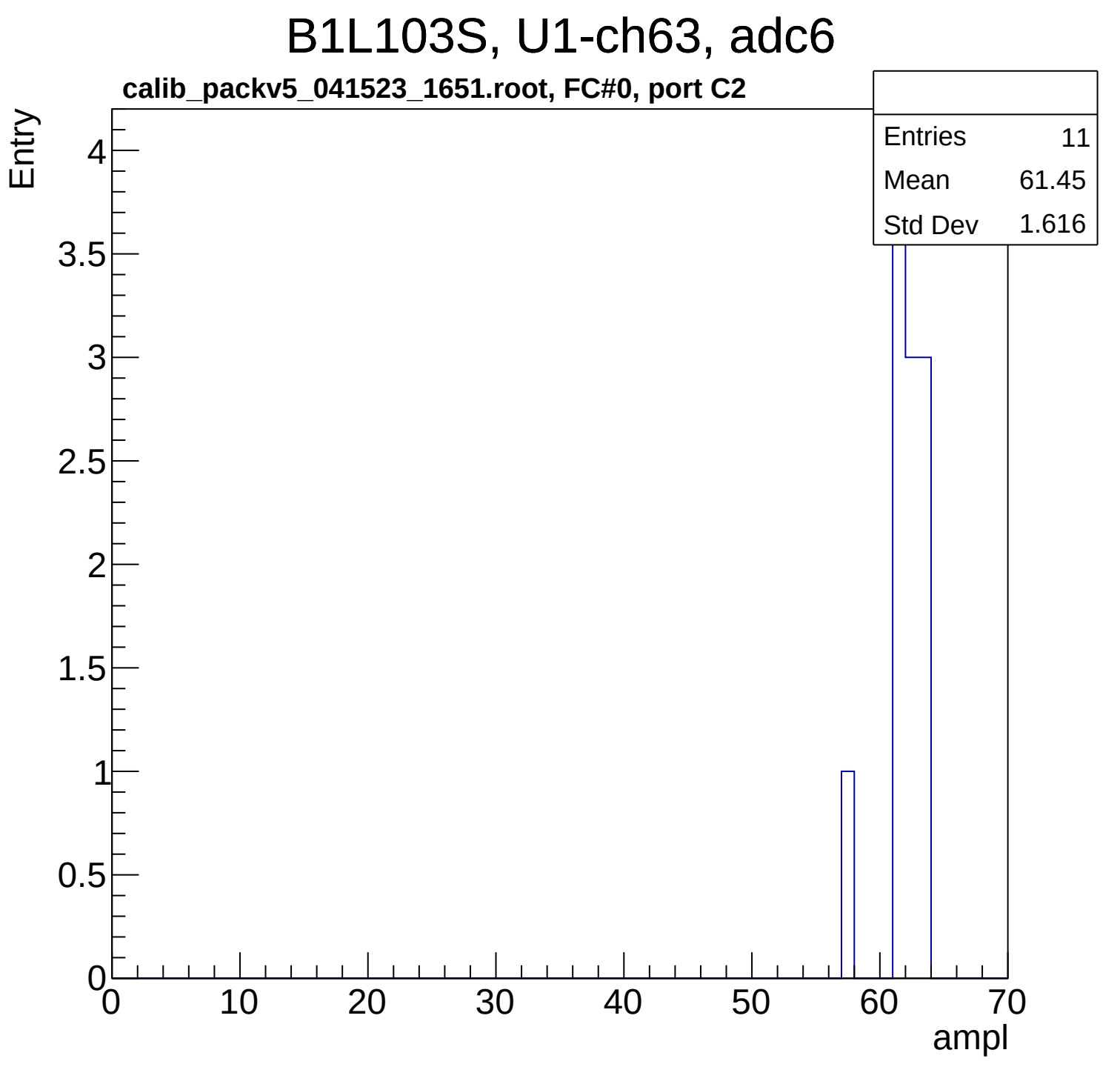
B1L103S, U1-ch63, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 61.45
Std Dev 1.616
Entry
ampl
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1.5
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3
3.5
4
0
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20
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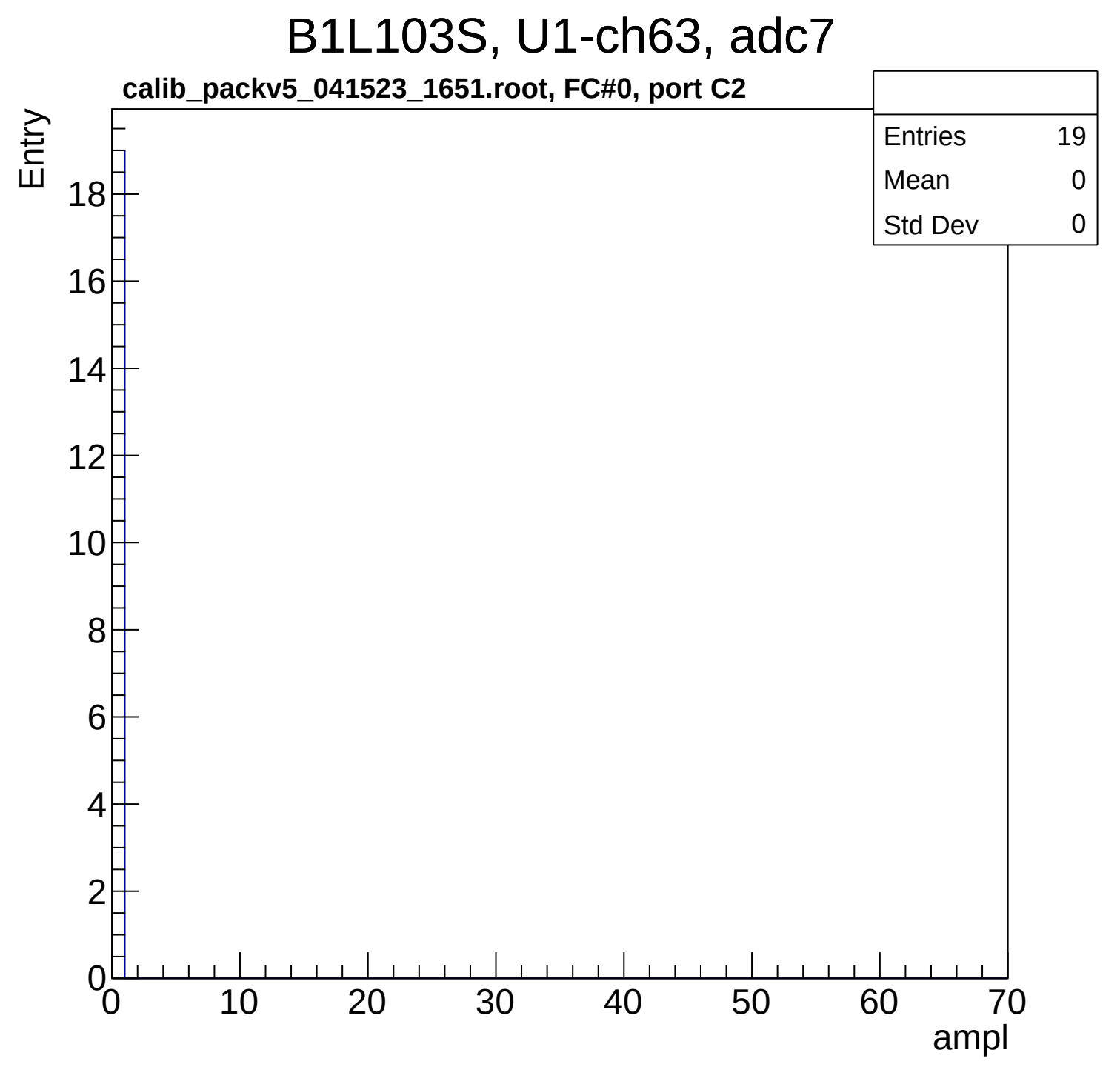
40
50
60
70


B1L103S, U1-ch63, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
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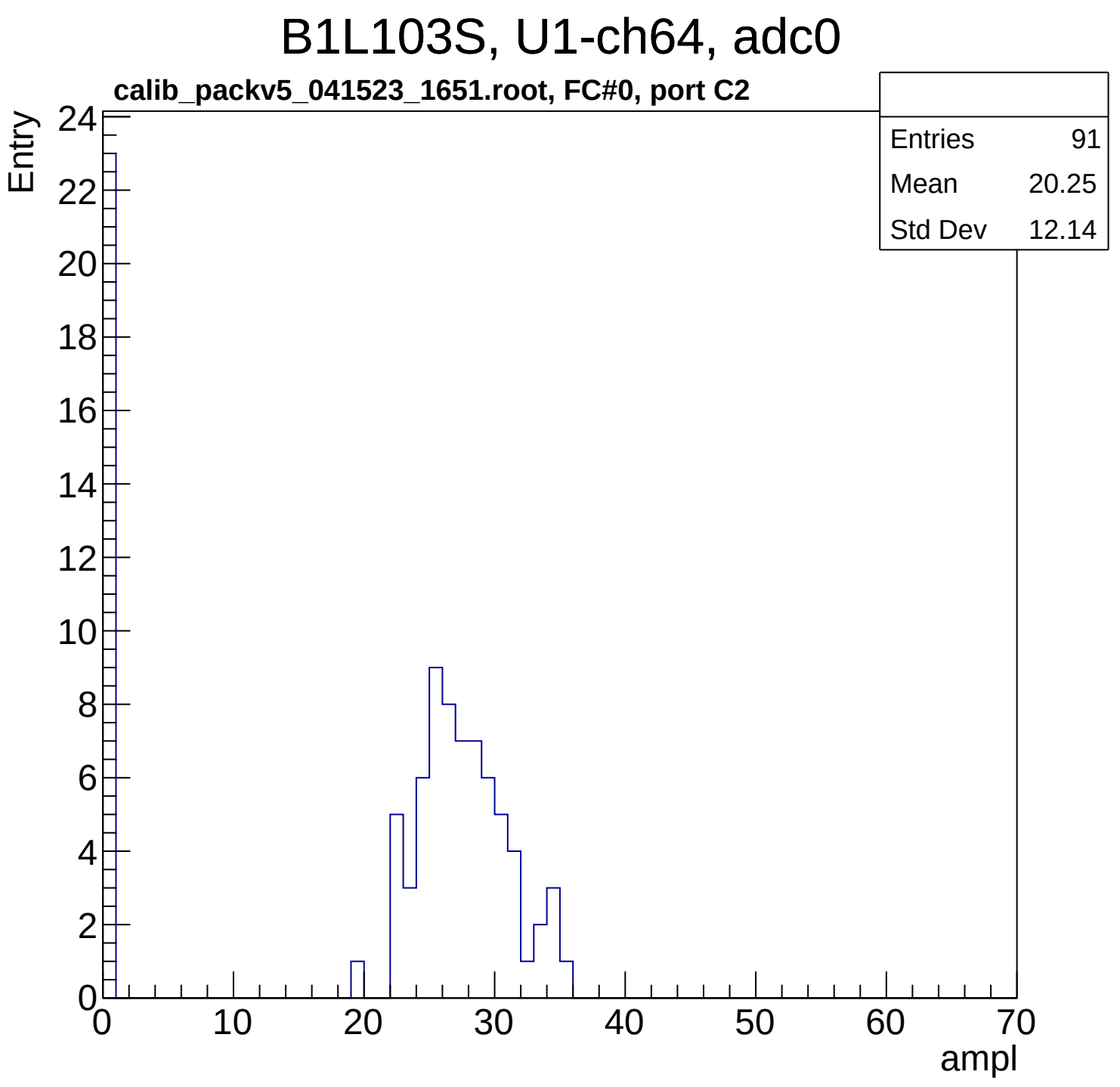
40
50
60
70
ampl


B1L103S, U1-ch64, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 91
Mean 20.25
Std Dev 12.14
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
22
24
0
10
20
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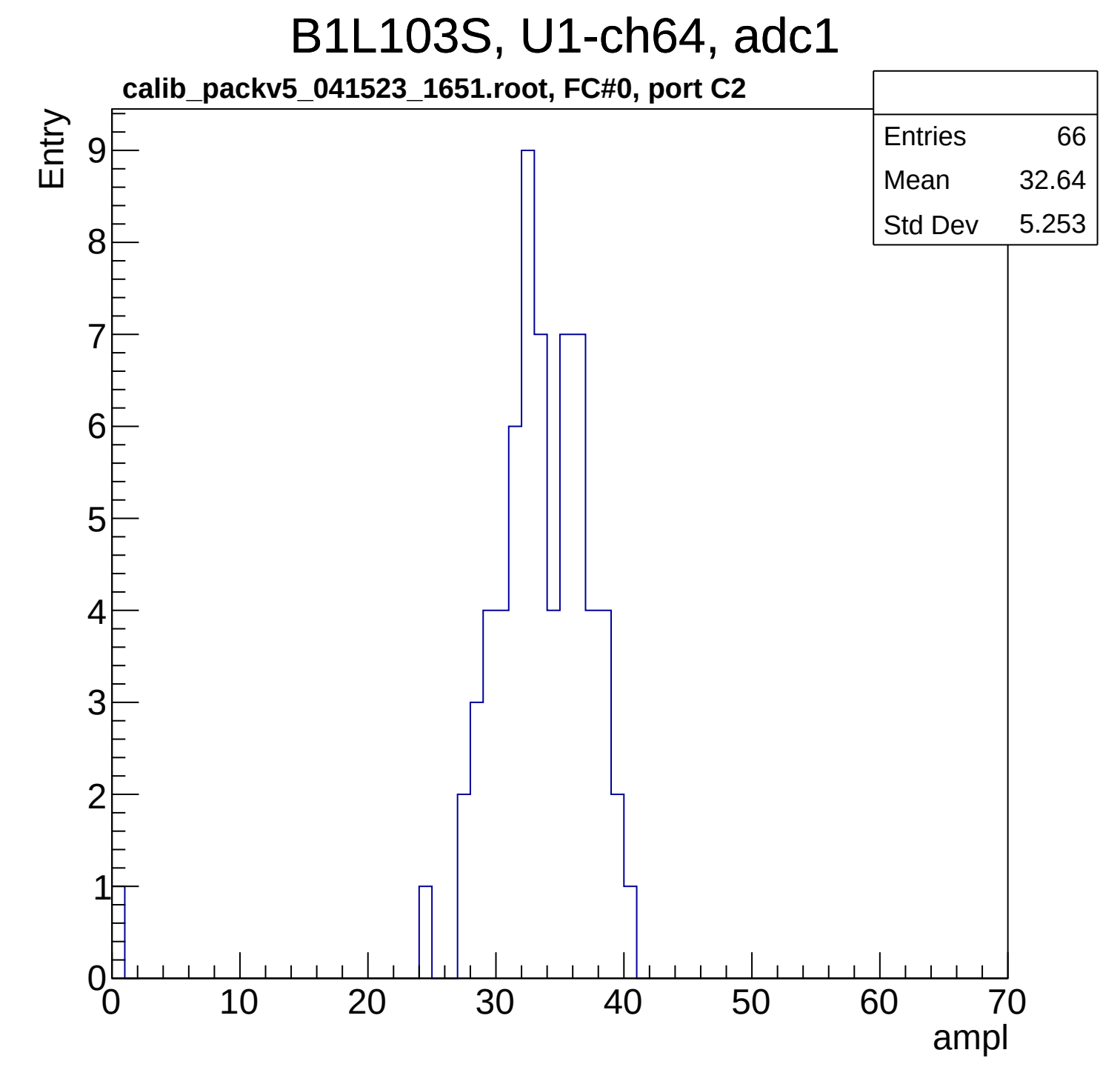
40
50
60
70


B1L103S, U1-ch64, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 32.64
Std Dev 5.253
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
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20
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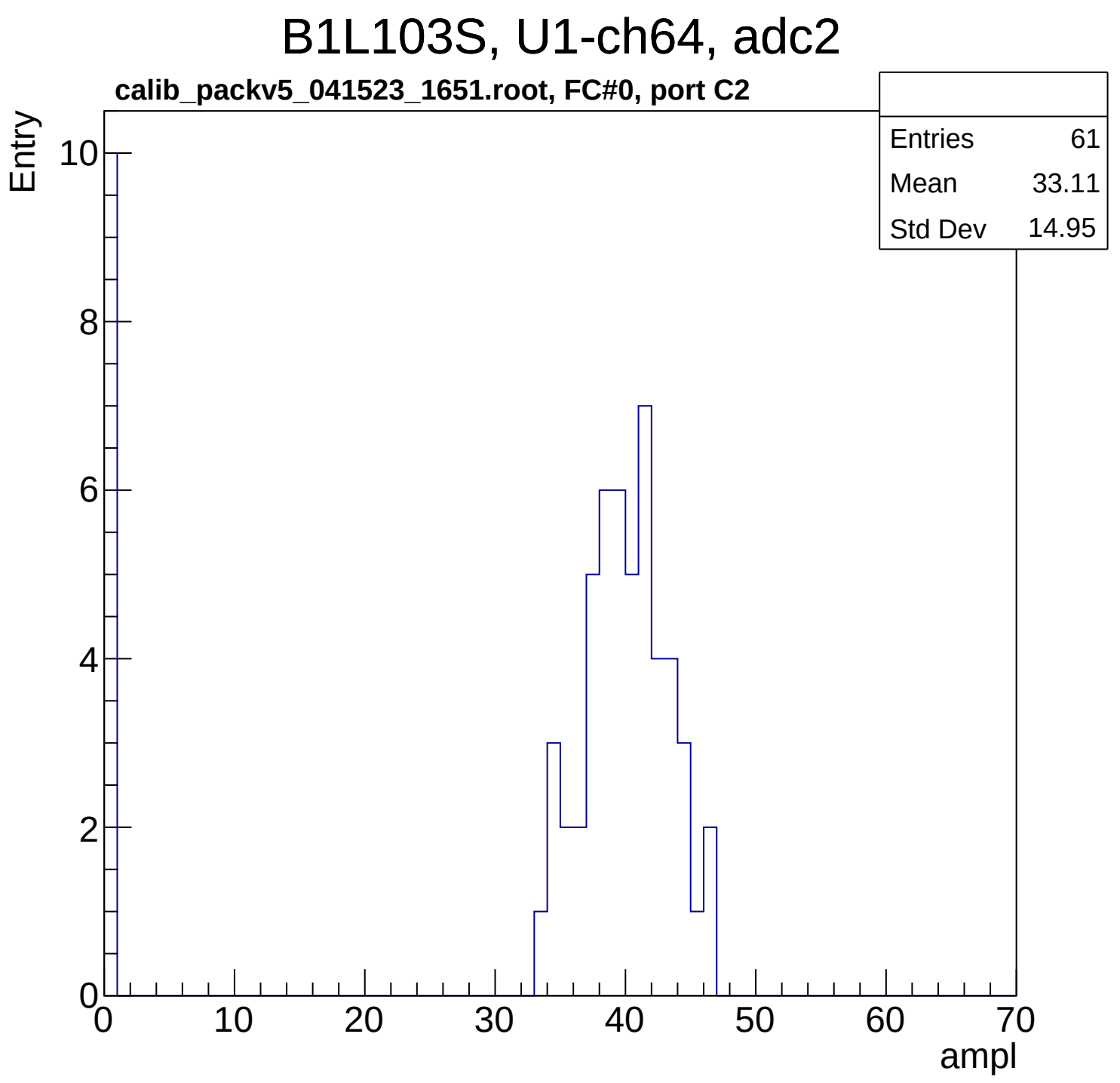
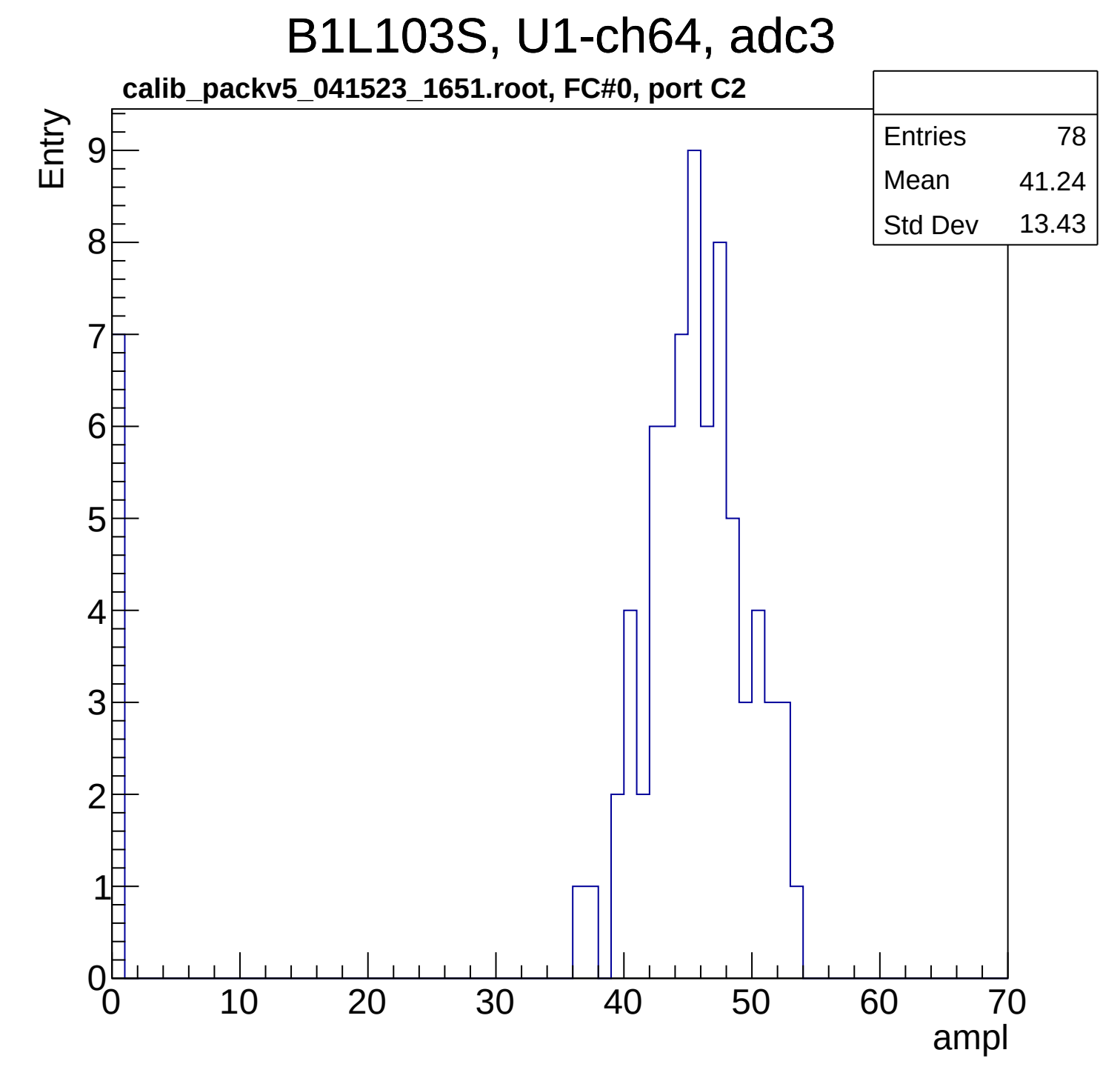
40
50
60
70


B1L103S, U1-ch64, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 33.11
Std Dev 14.95
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch64, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 41.24
Std Dev 13.43
Entry
ampl
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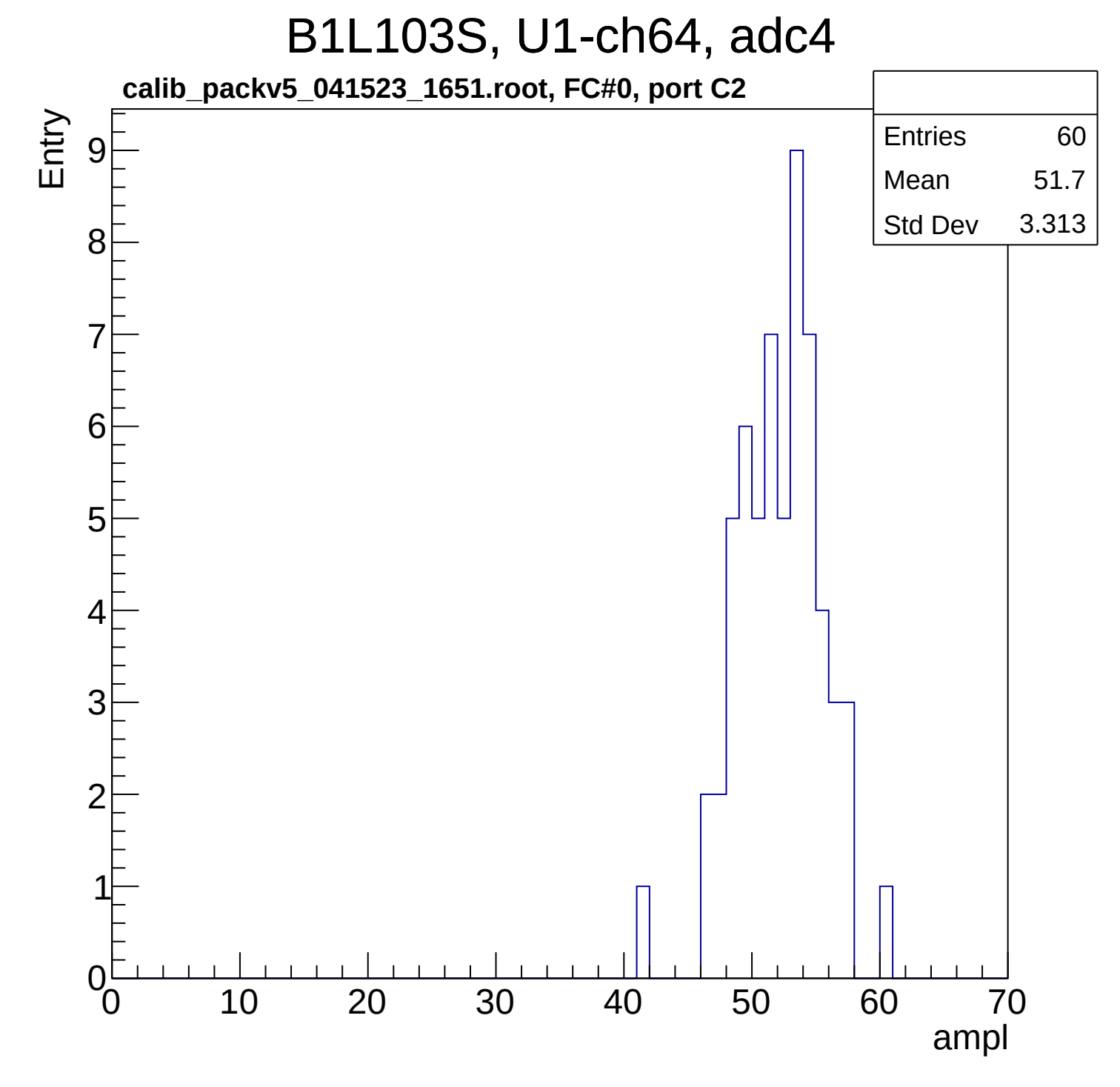
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9


B1L103S, U1-ch64, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 51.7
Std Dev 3.313
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
30
40
50
60
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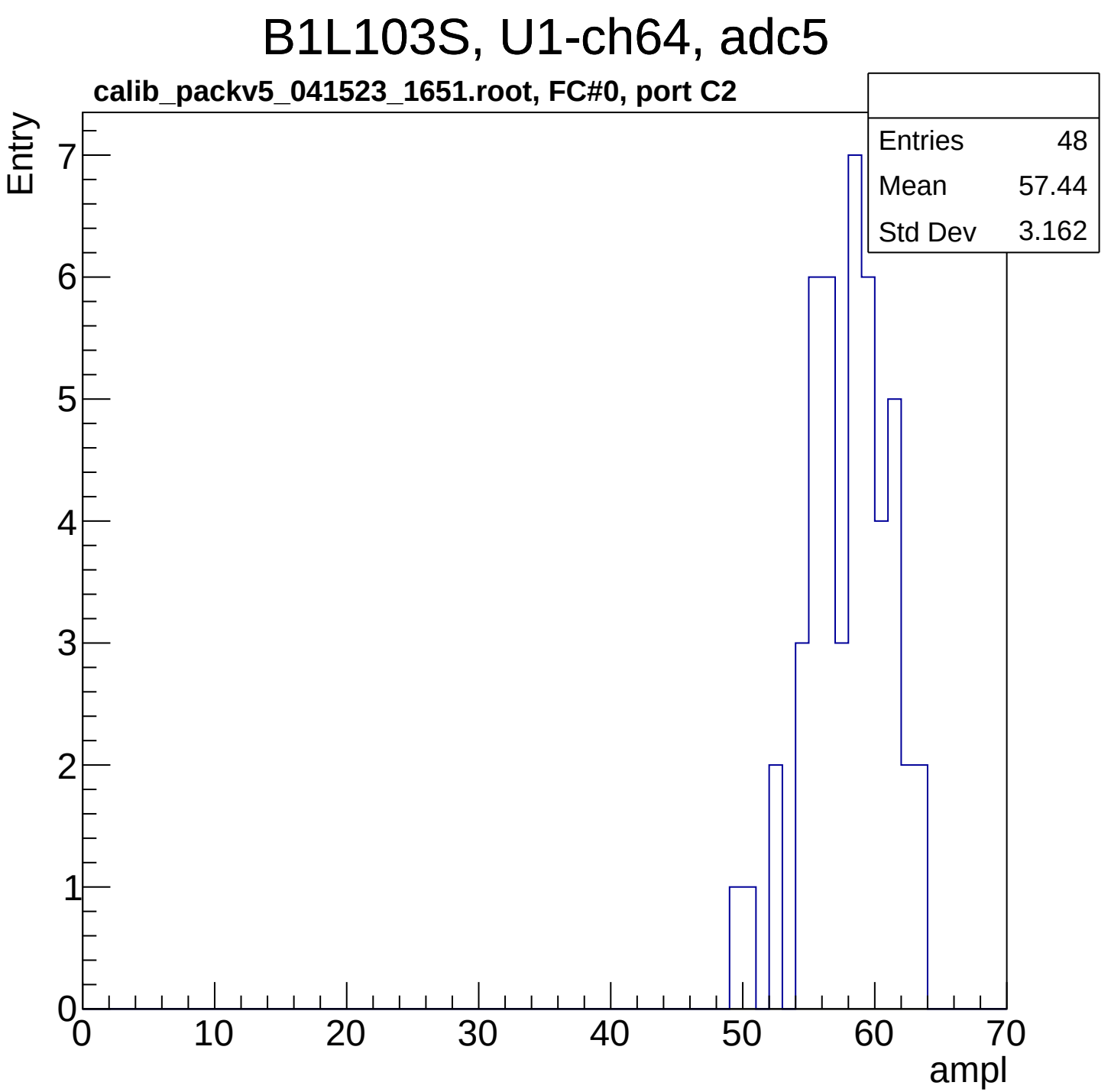
B1L103S, U1-ch64, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 57.44
Std Dev 3.162
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
30
40
50
60
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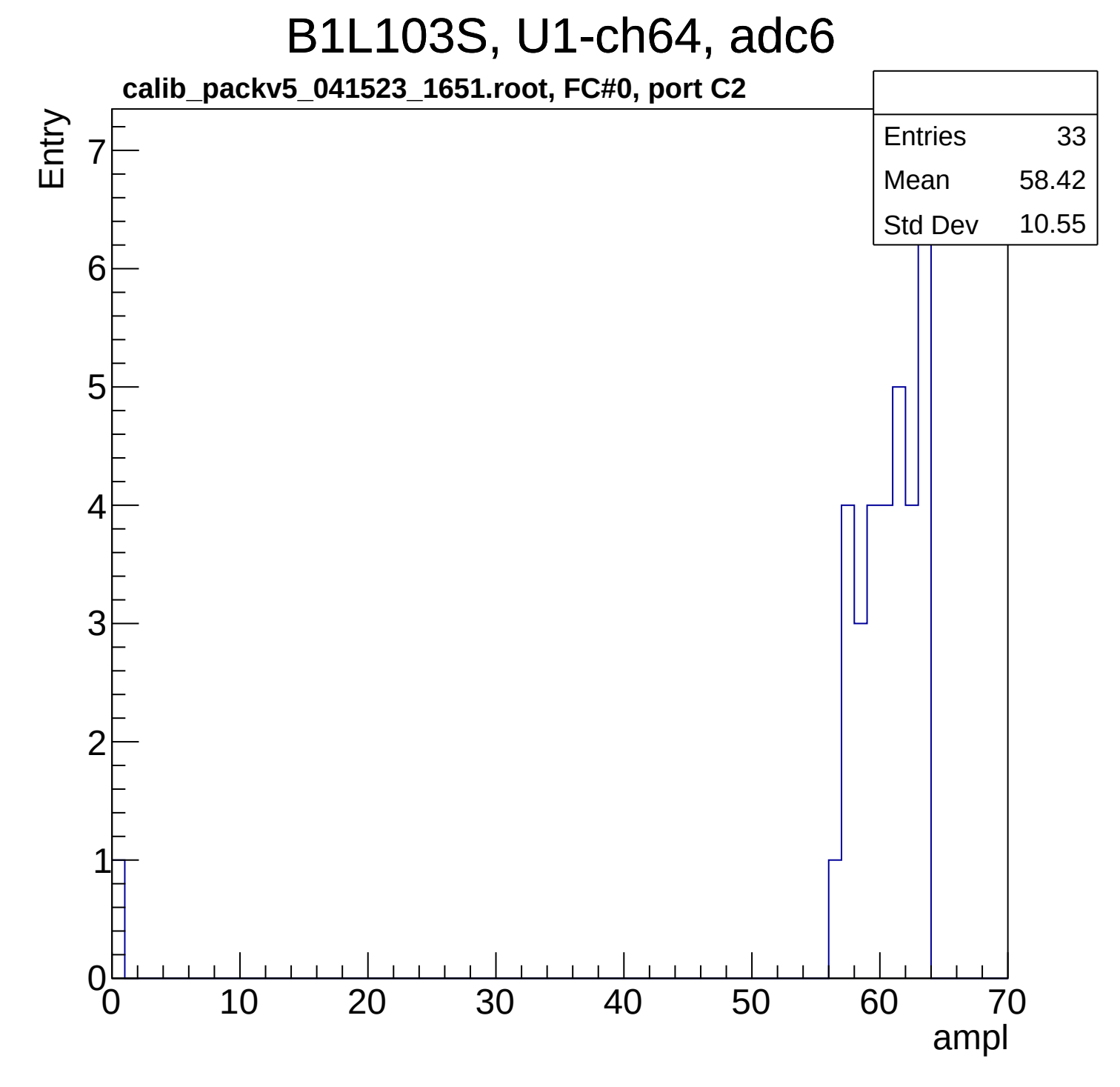
B1L103S, U1-ch64, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 33
Mean 58.42
Std Dev 10.55
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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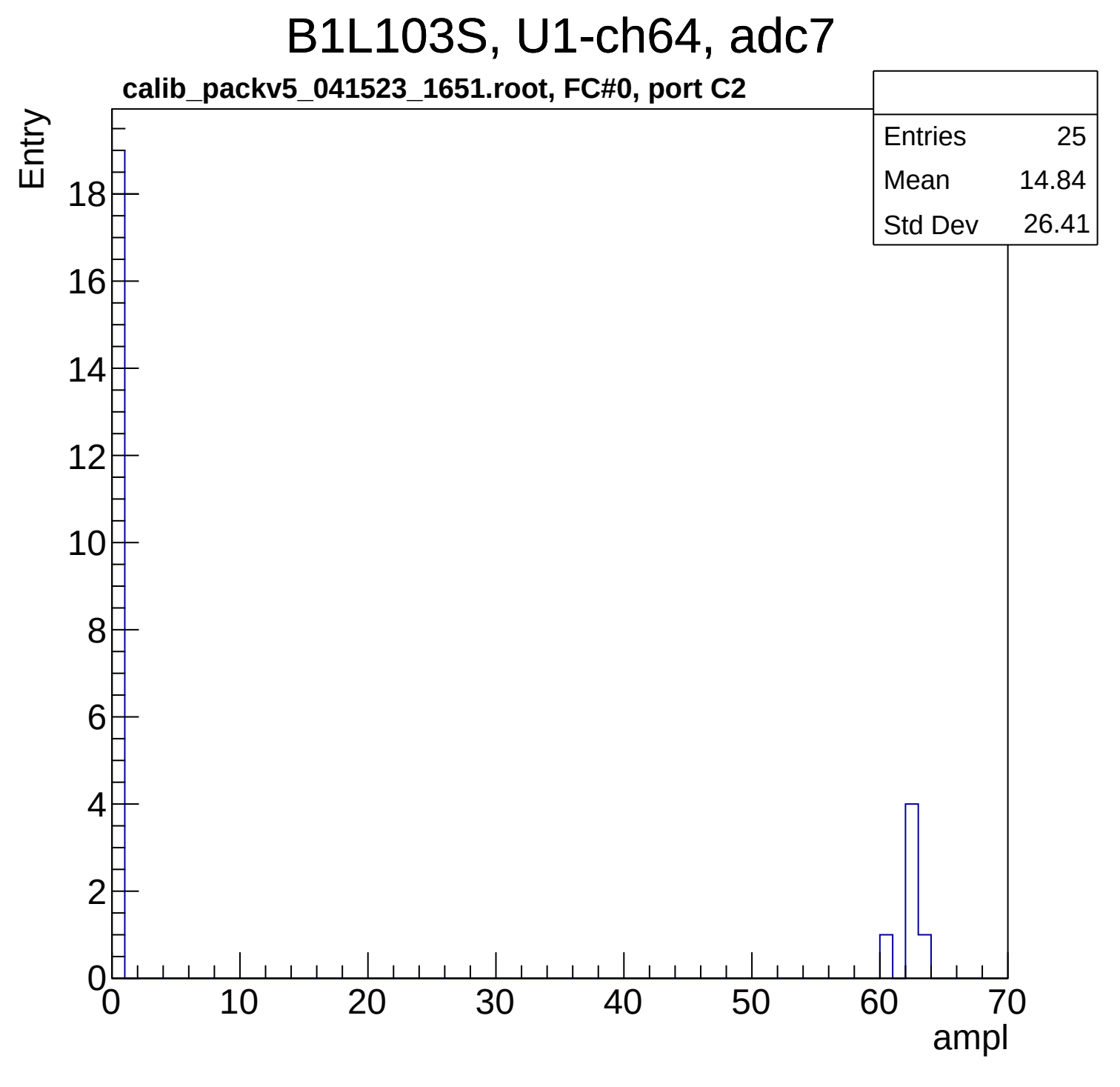
B1L103S, U1-ch64, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 25
Mean 14.84
Std Dev 26.41
Entry
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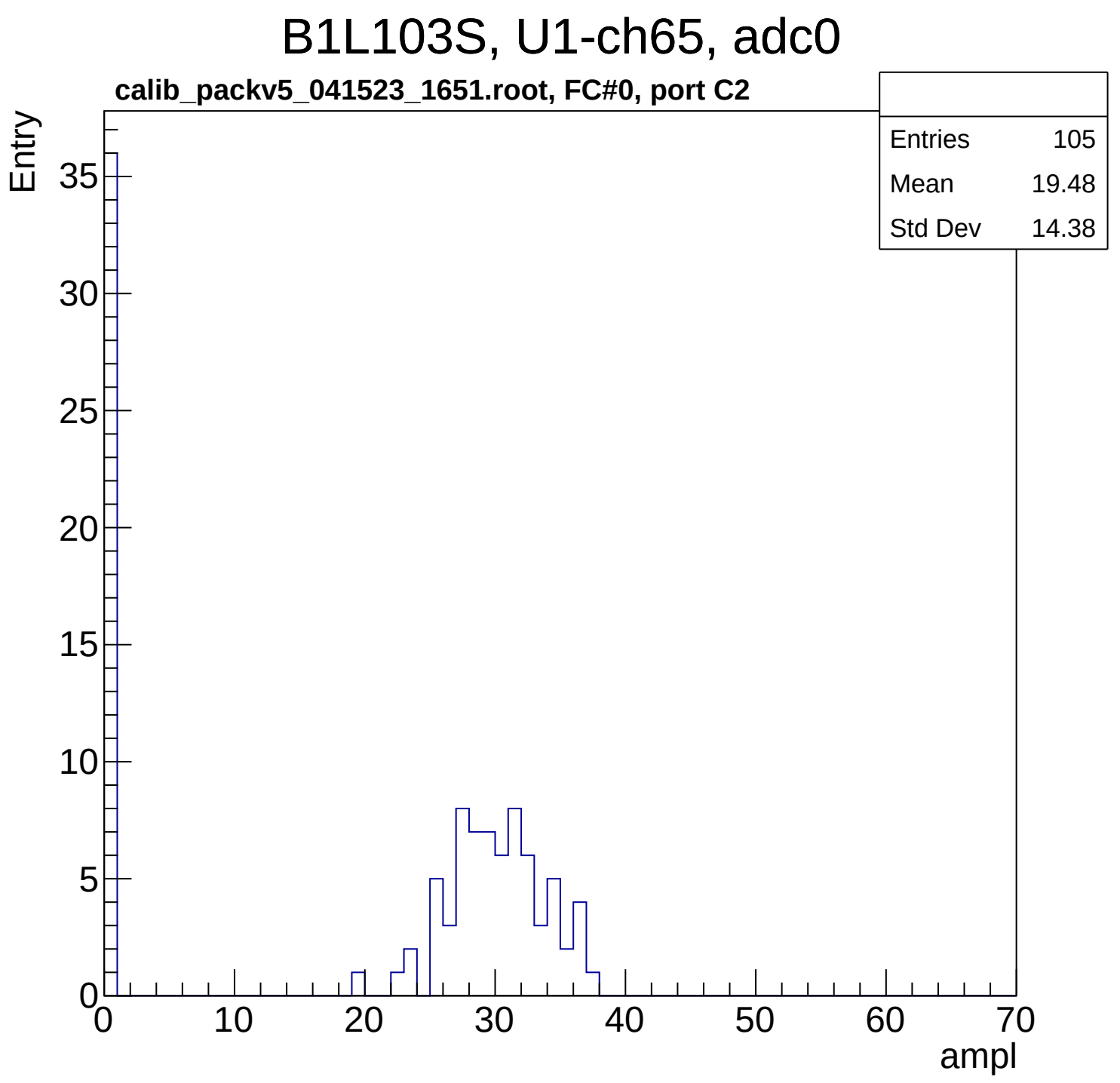
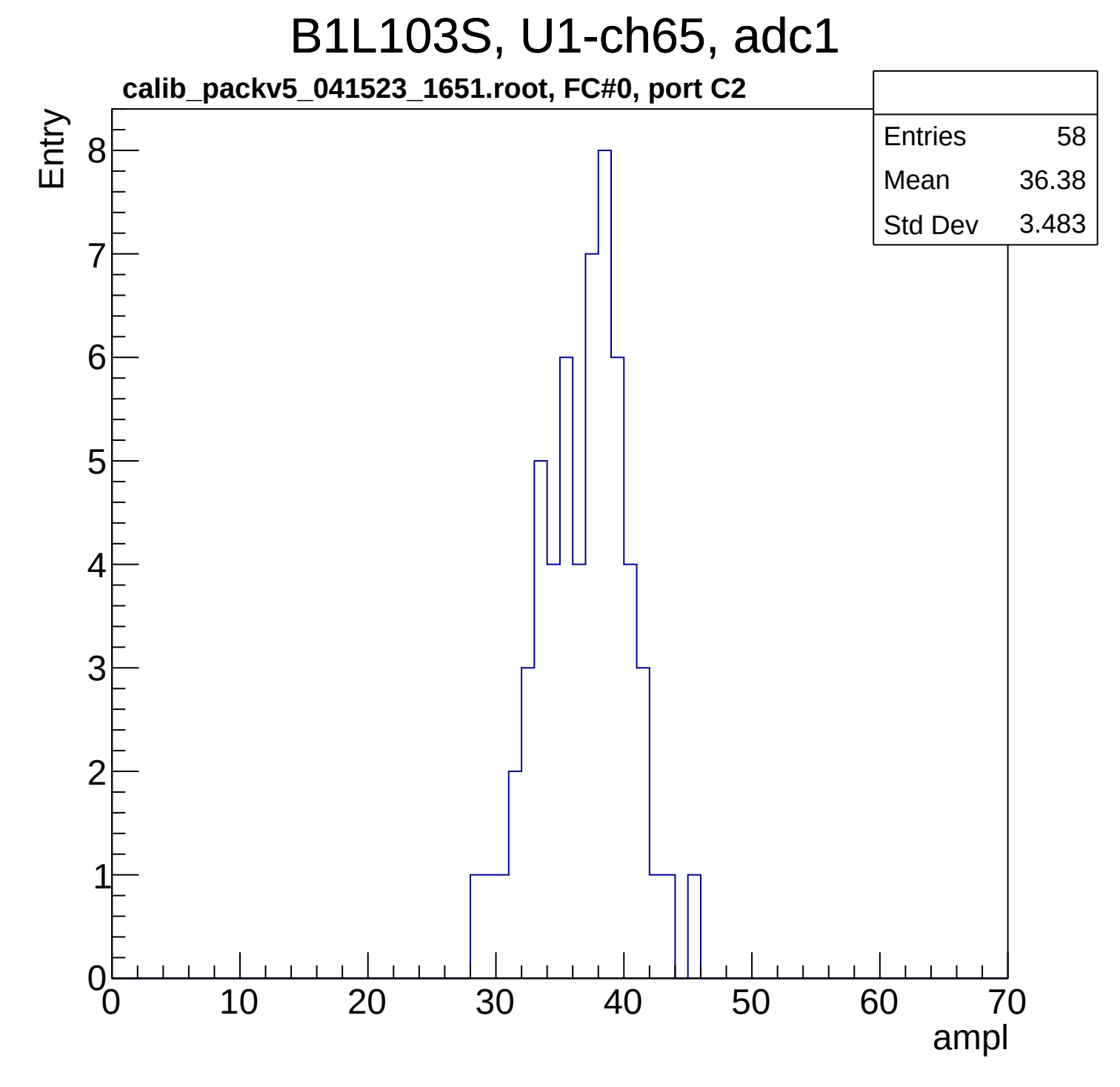
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch65, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 105
Mean 19.48
Std Dev 14.38
Entry
0
5
10
15
20
25
30
35
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch65, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 36.38
Std Dev 3.483
Entry
ampl
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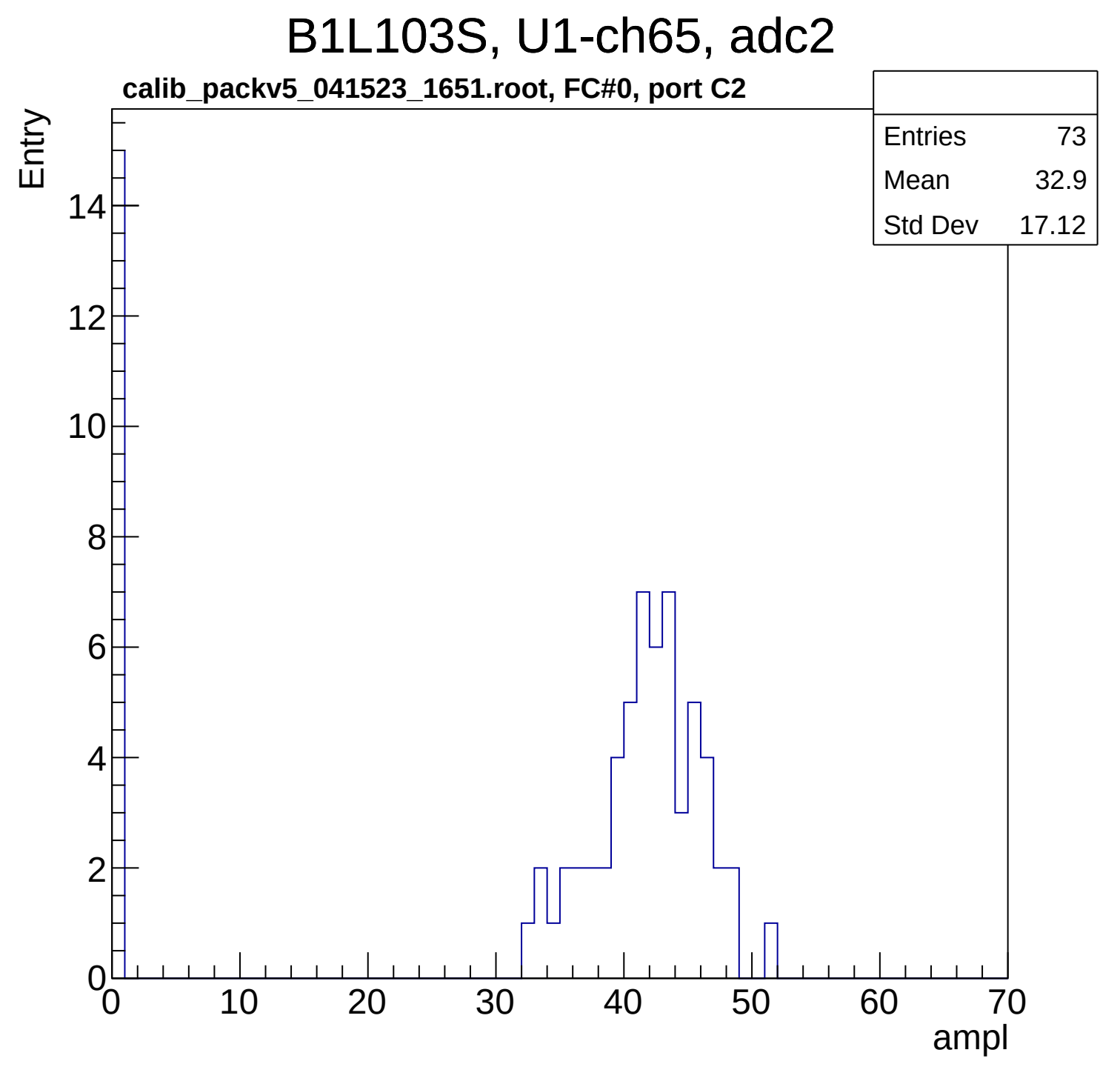
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U1-ch65, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 32.9
Std Dev 17.12
Entry
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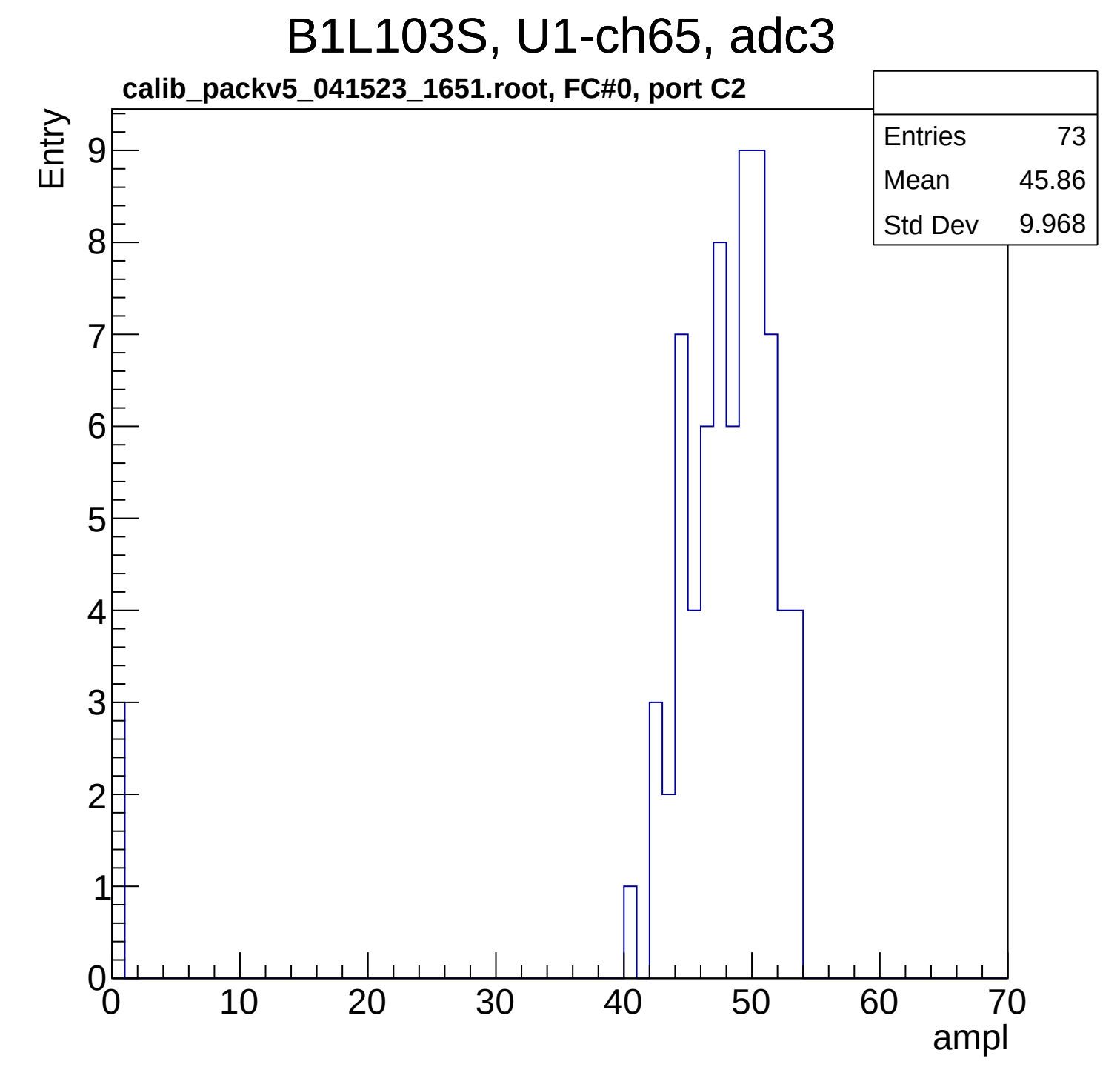
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch65, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 45.86
Std Dev 9.968
Entry
ampl
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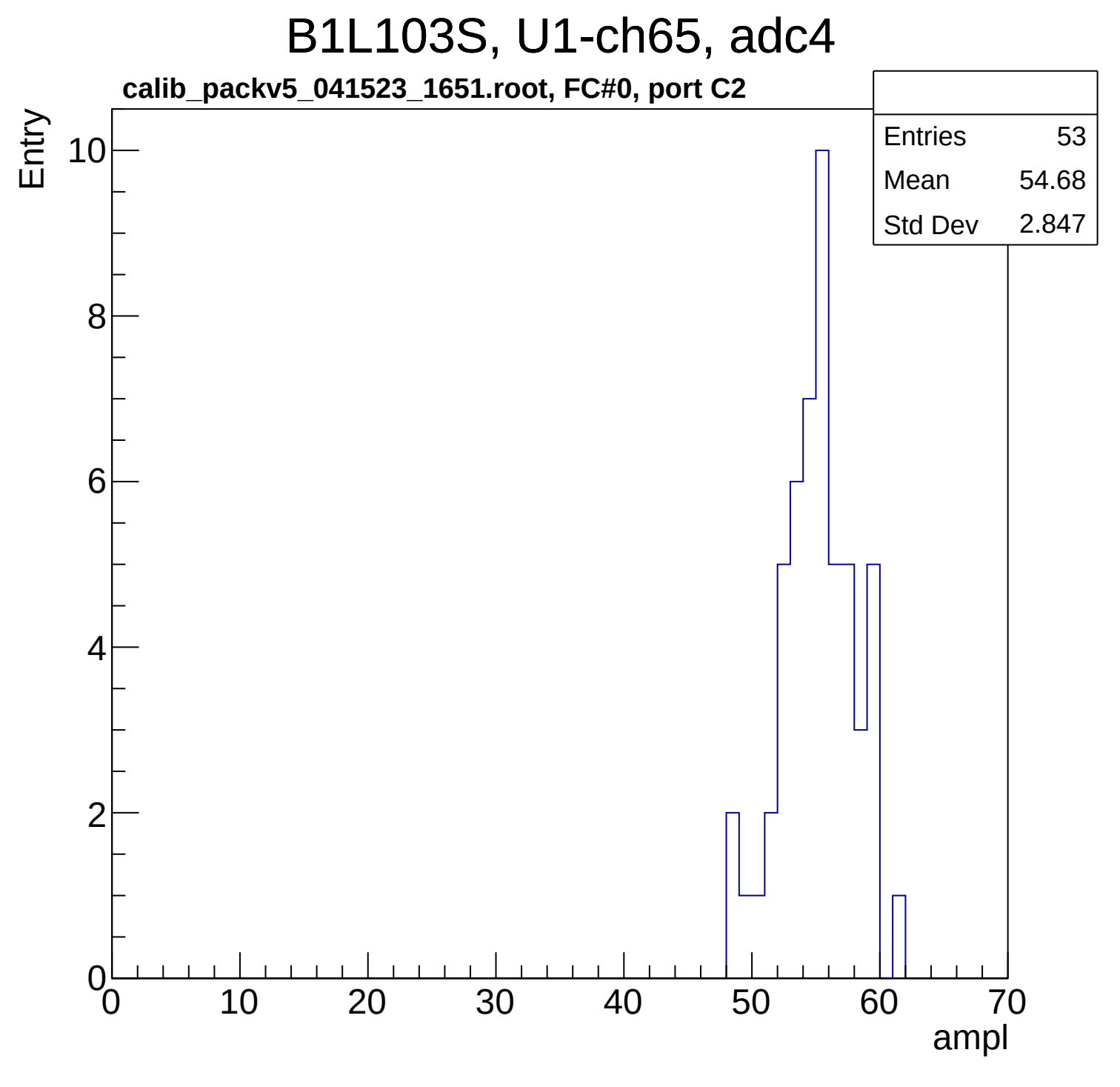
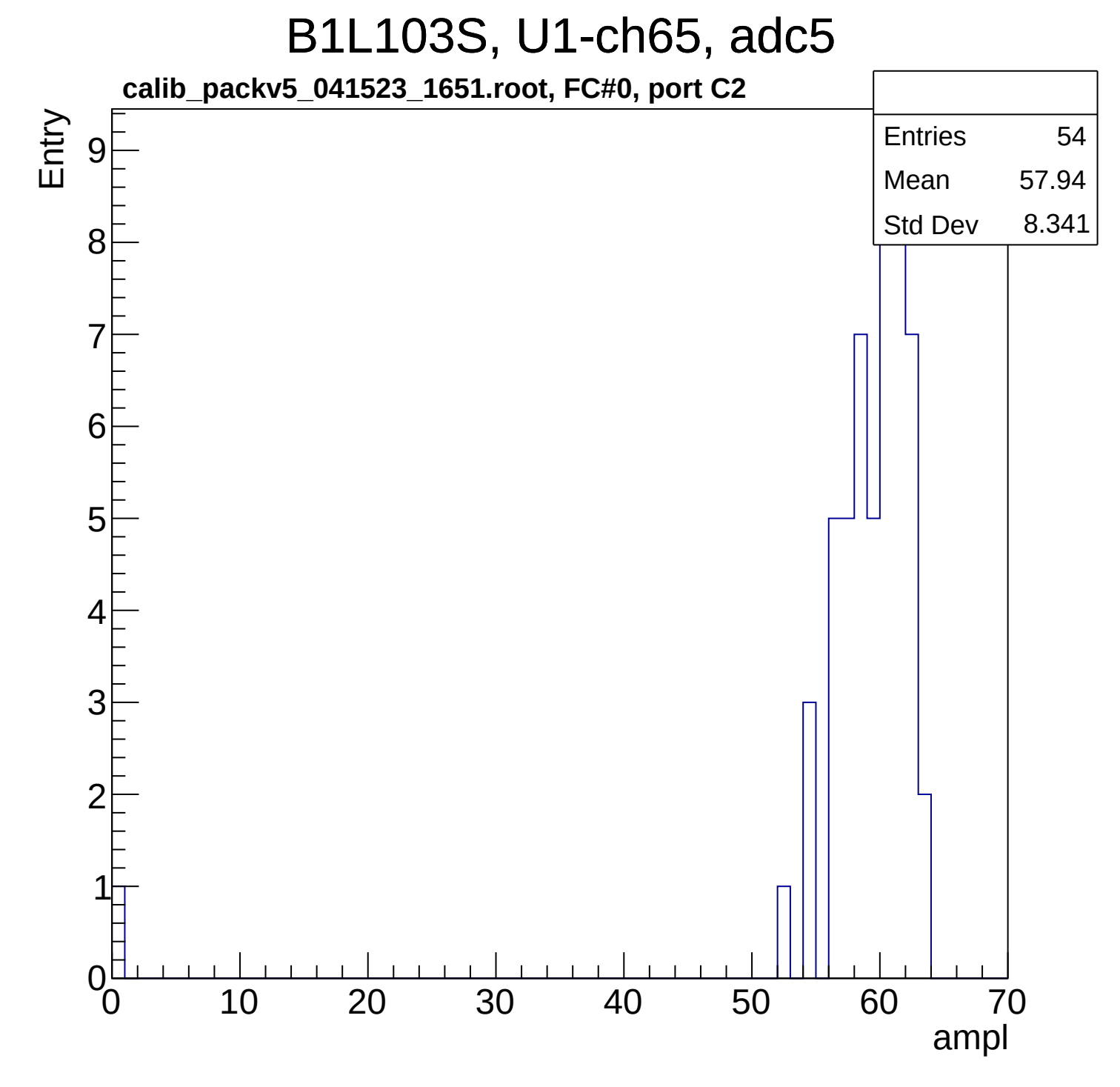
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U1-ch65, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 54.68
Std Dev 2.847
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U1-ch65, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 57.94
Std Dev 8.341
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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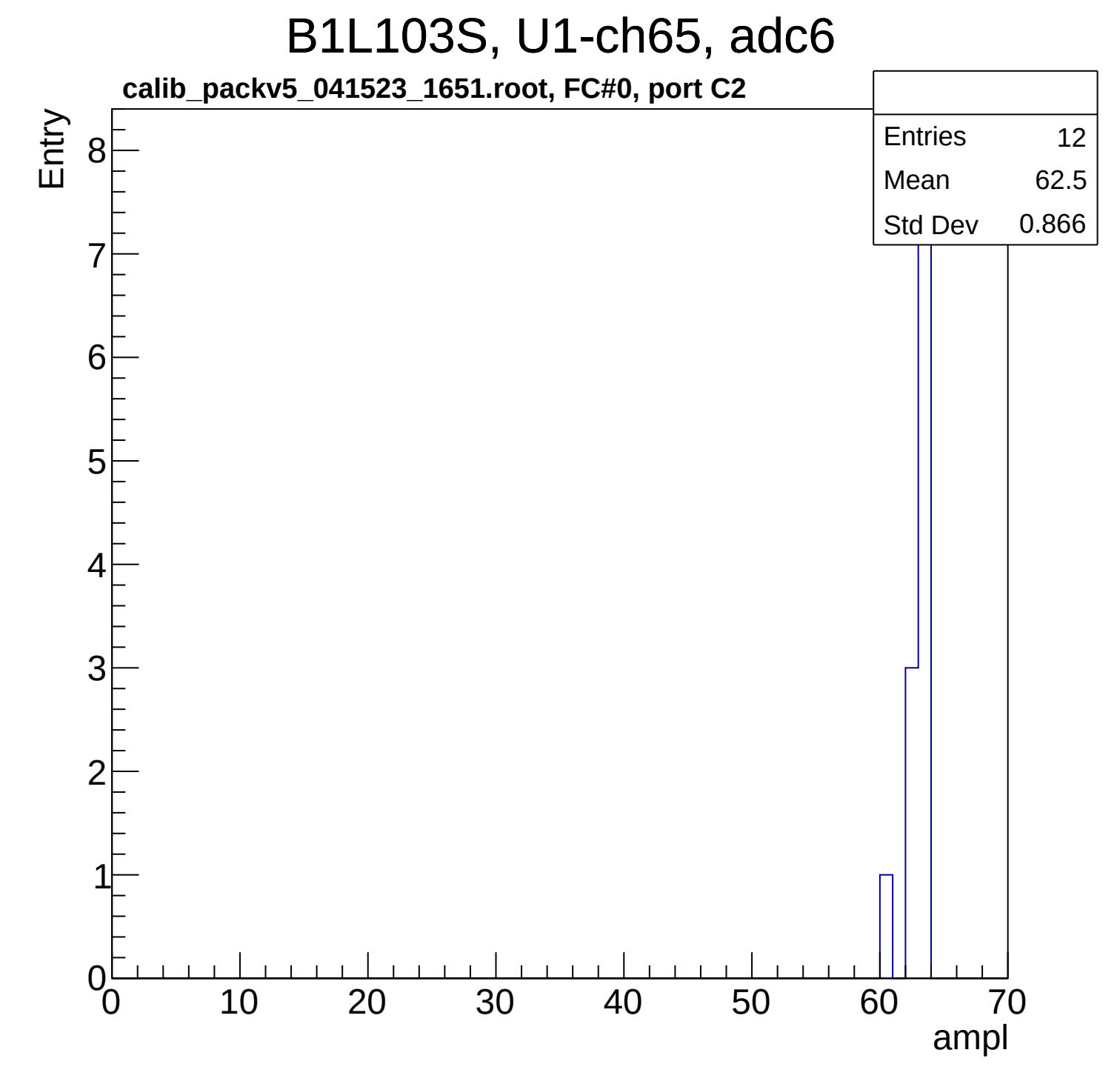
B1L103S, U1-ch65, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 62.5
Std Dev 0.866
Entry
ampl
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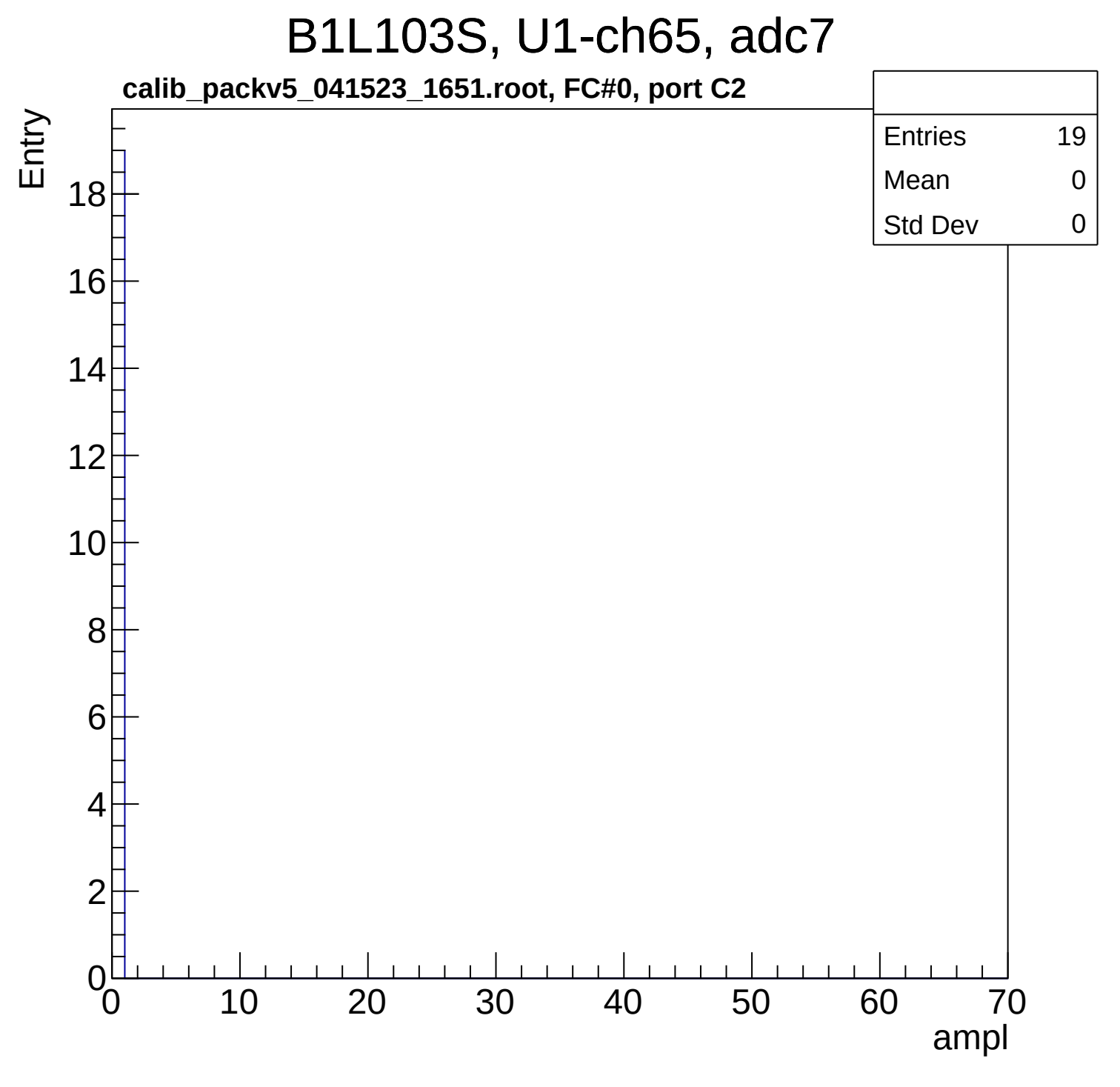
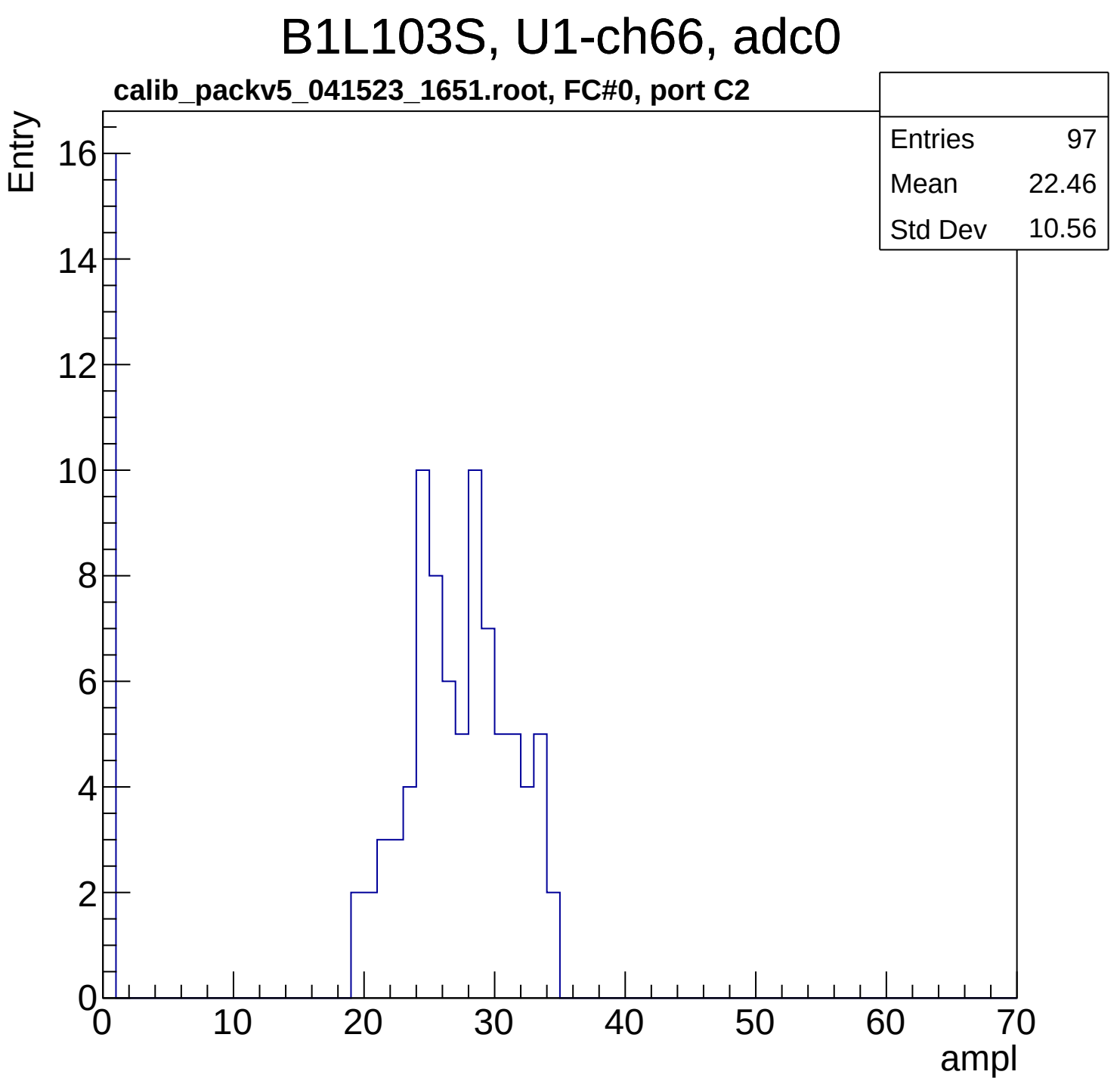
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U1-ch65, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch66, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 97
Mean 22.46
Std Dev 10.56
Entry
ampl
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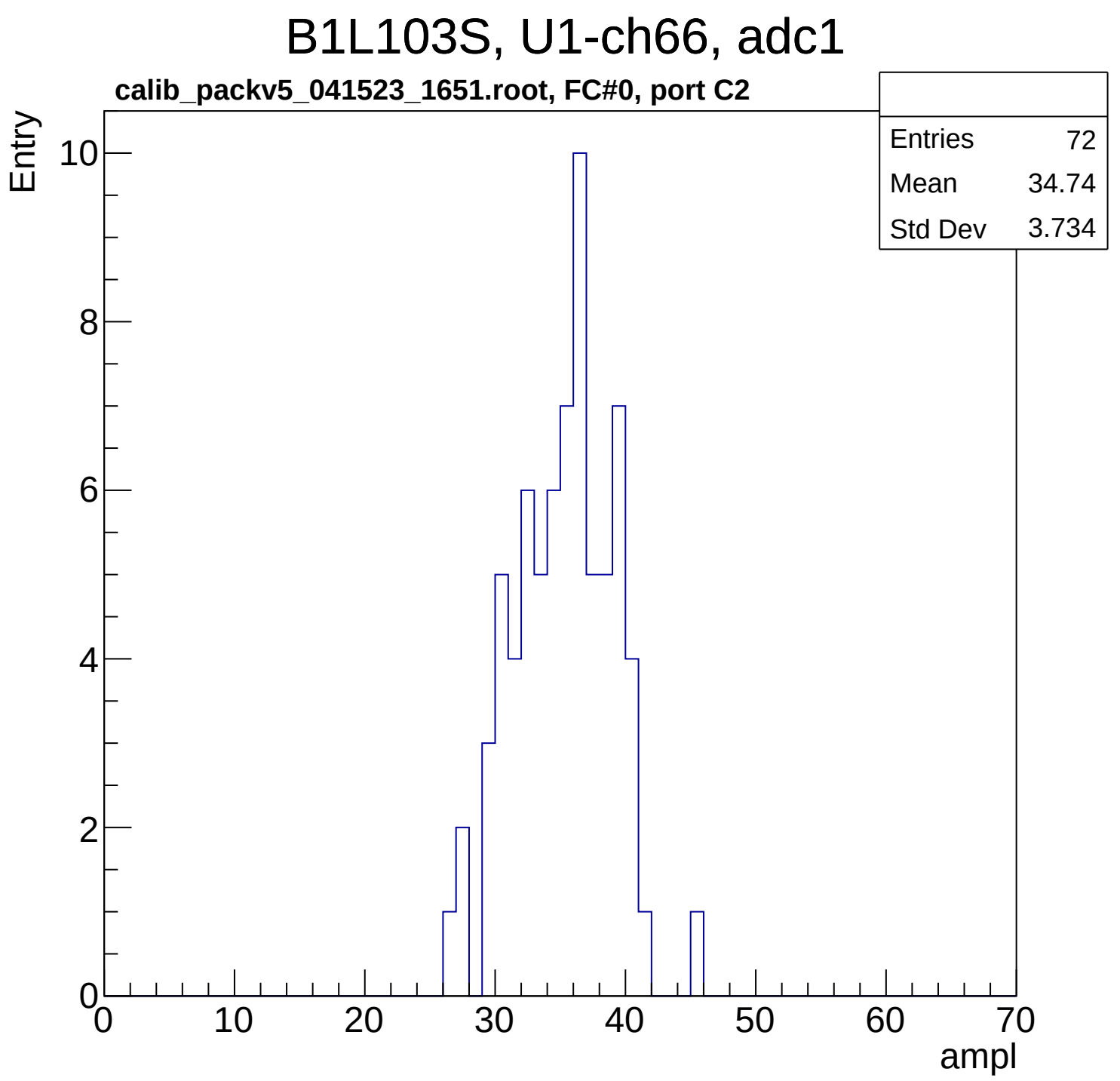
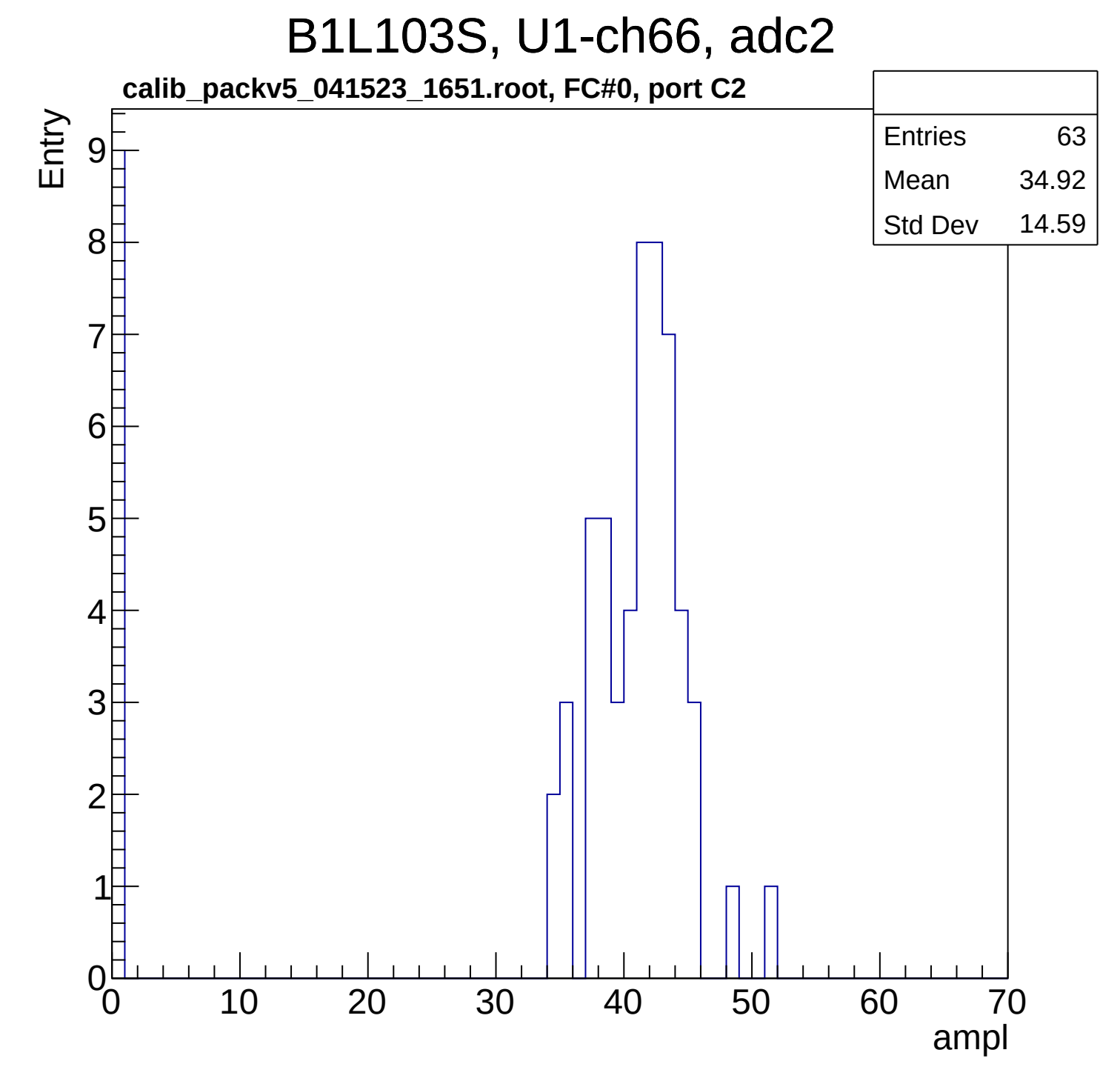
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70


B1L103S, U1-ch66, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 34.74
Std Dev 3.734
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U1-ch66, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 34.92
Std Dev 14.59
Entry
ampl
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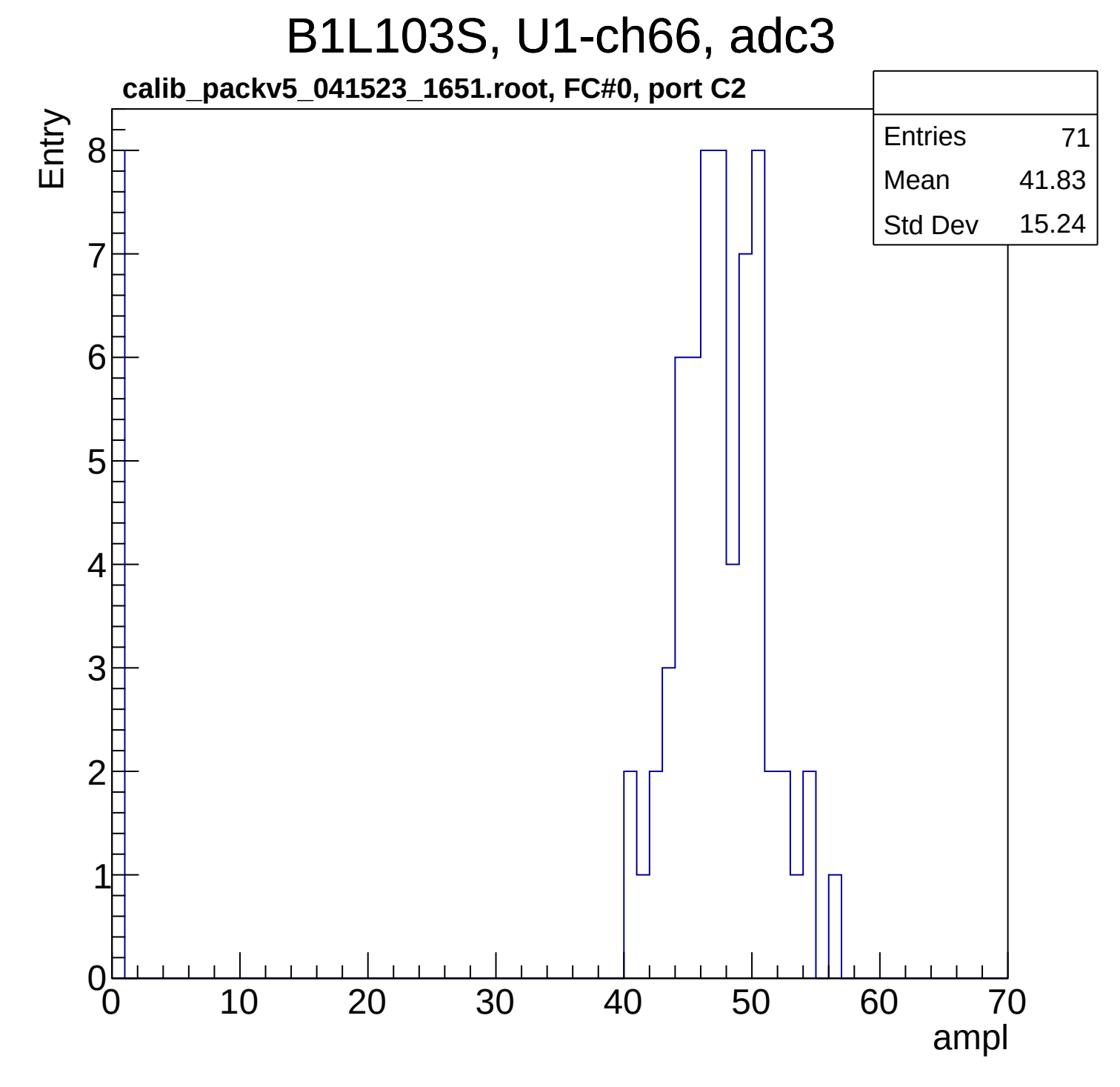
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U1-ch66, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 41.83
Std Dev 15.24
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
30
40
50
60
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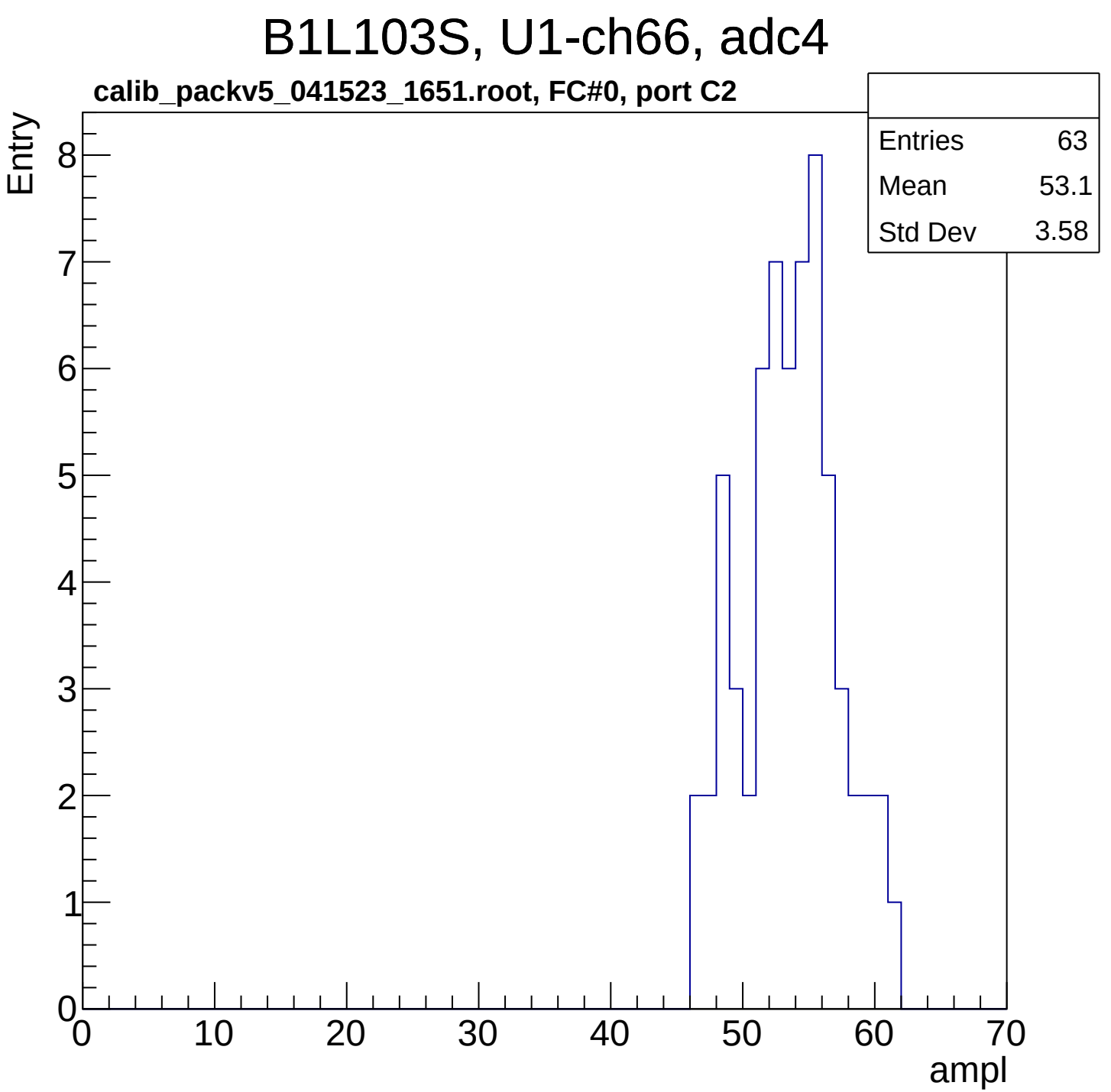
B1L103S, U1-ch66, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 53.1
Std Dev 3.58
Entry
ampl
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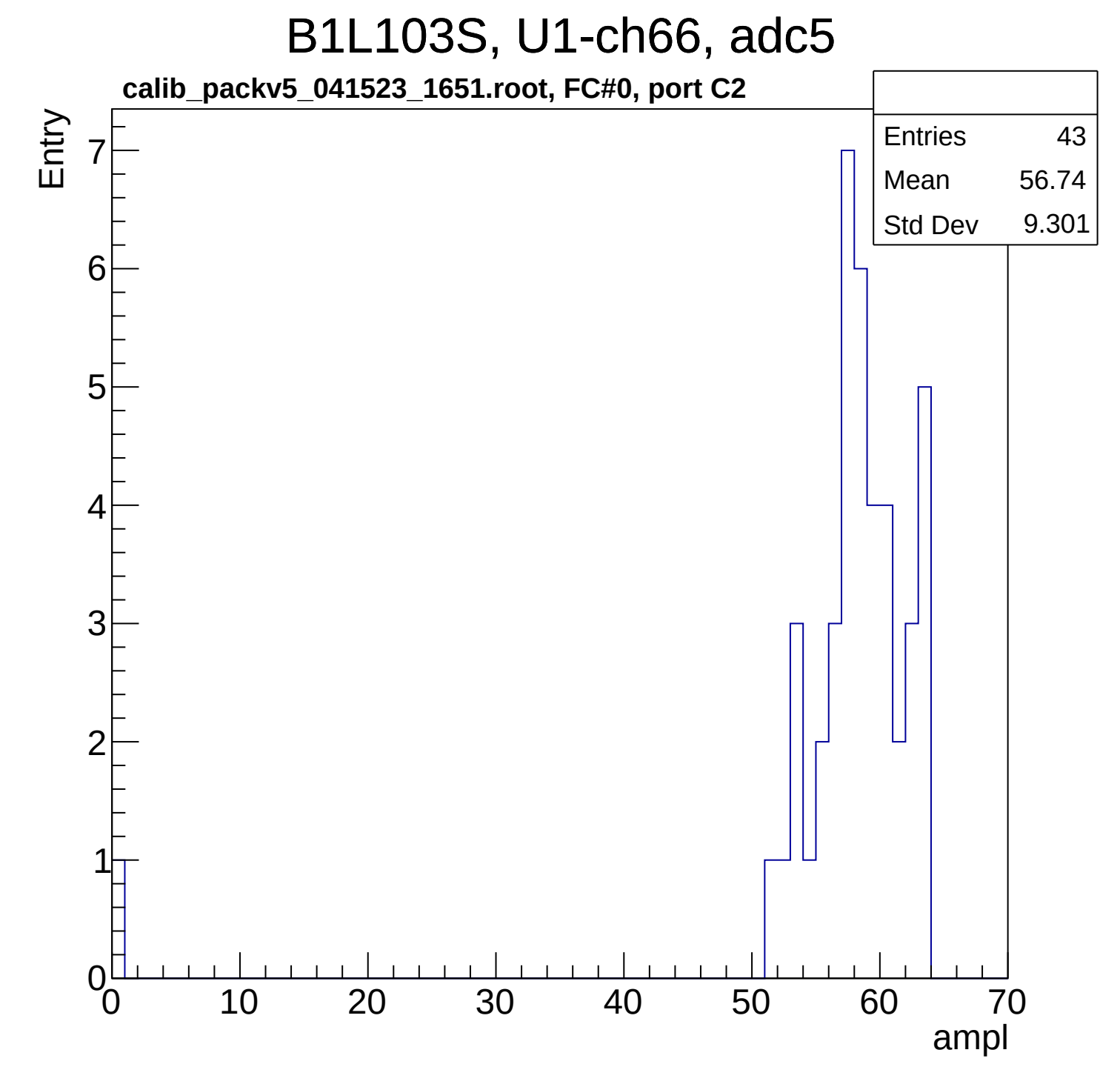
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U1-ch66, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 43
Mean 56.74
Std Dev 9.301
Entry
ampl
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2
3
4
5
6
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0
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20
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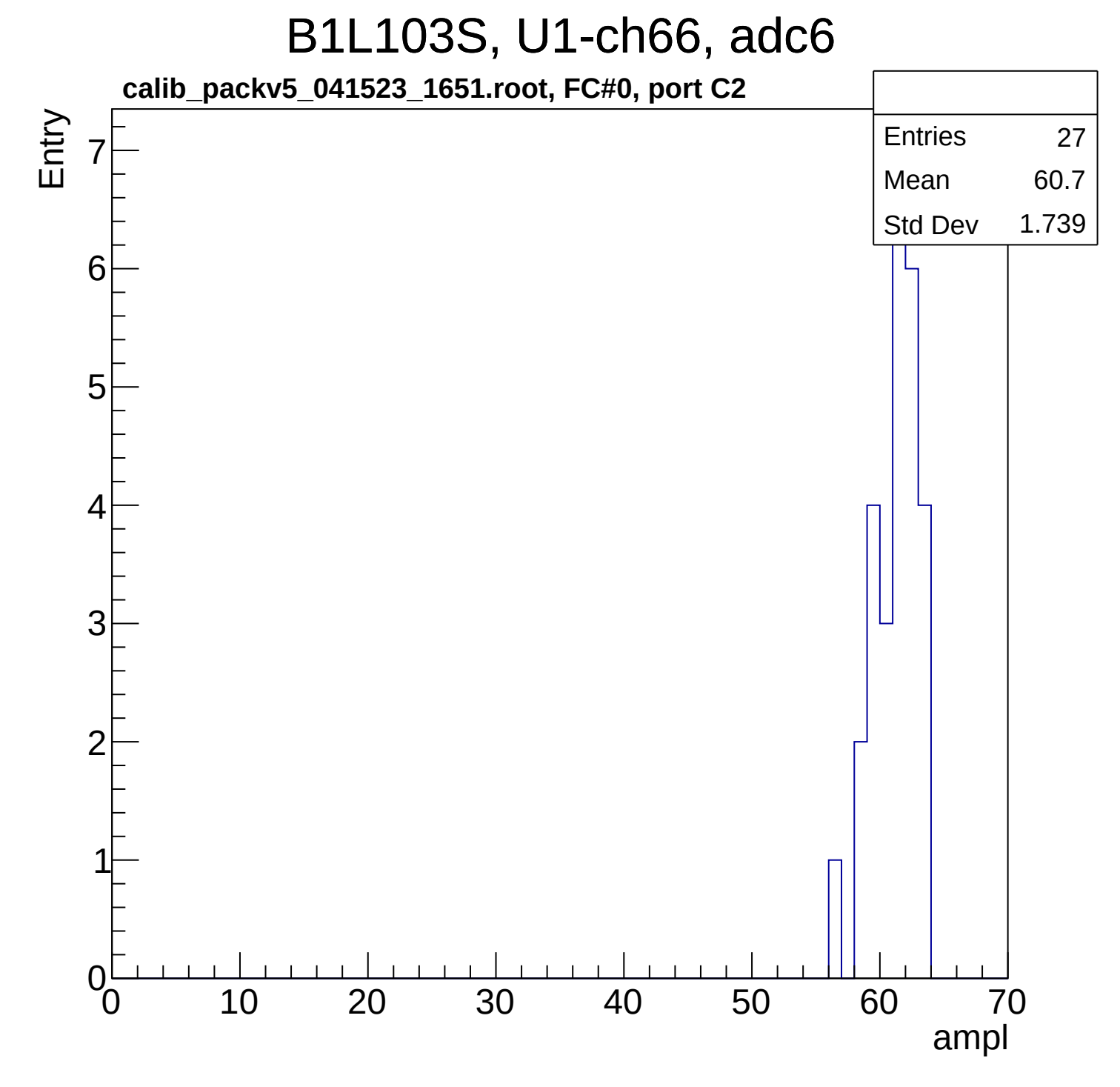
40
50
60
70


B1L103S, U1-ch66, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 27
Mean 60.7
Std Dev 1.739
Entry
ampl
0
1
2
3
4
5
6
7
0
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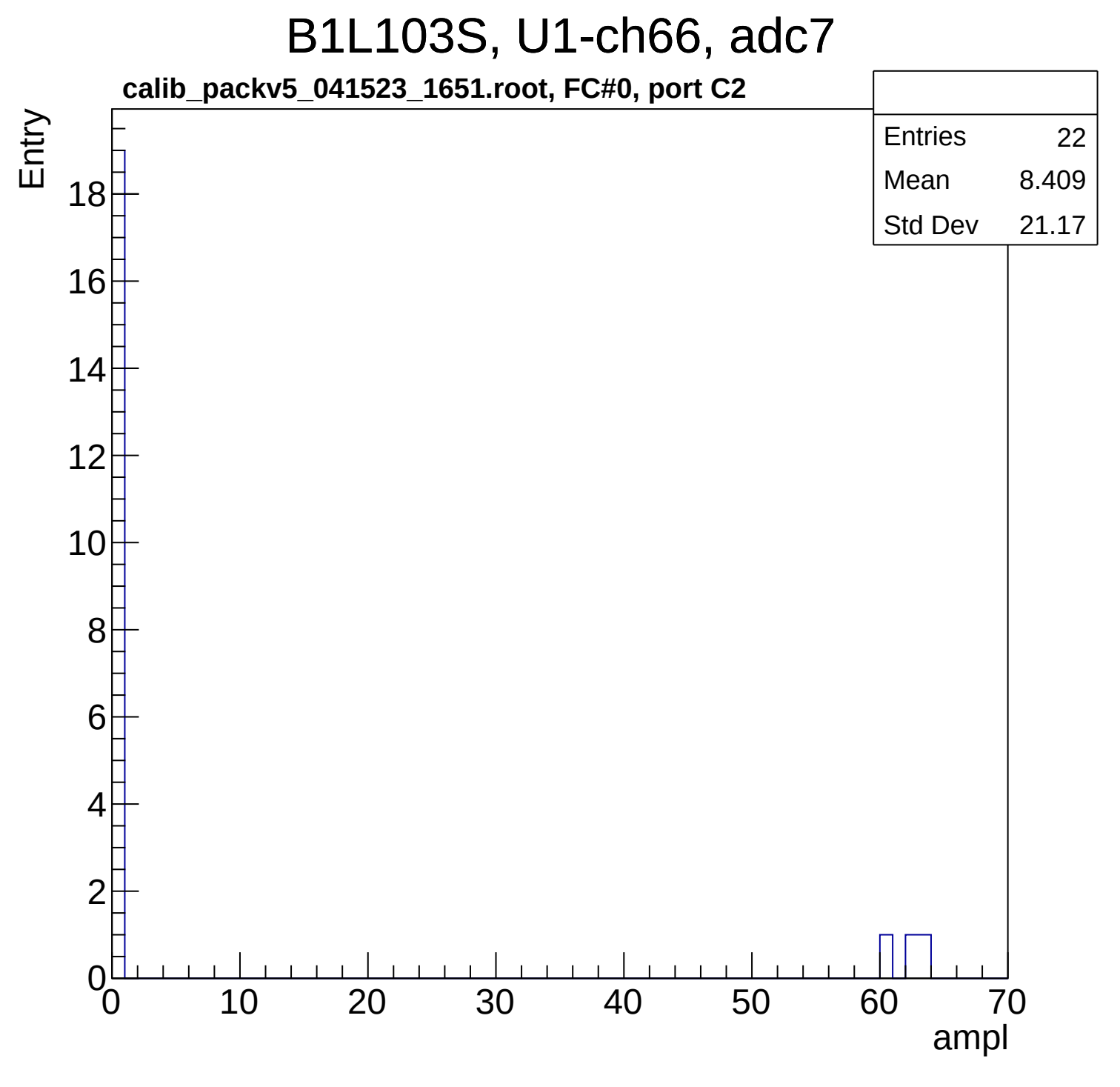
20
30
40
50
60
70


B1L103S, U1-ch66, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 8.409
Std Dev 21.17
Entry
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6
8
10
12
14
16
18
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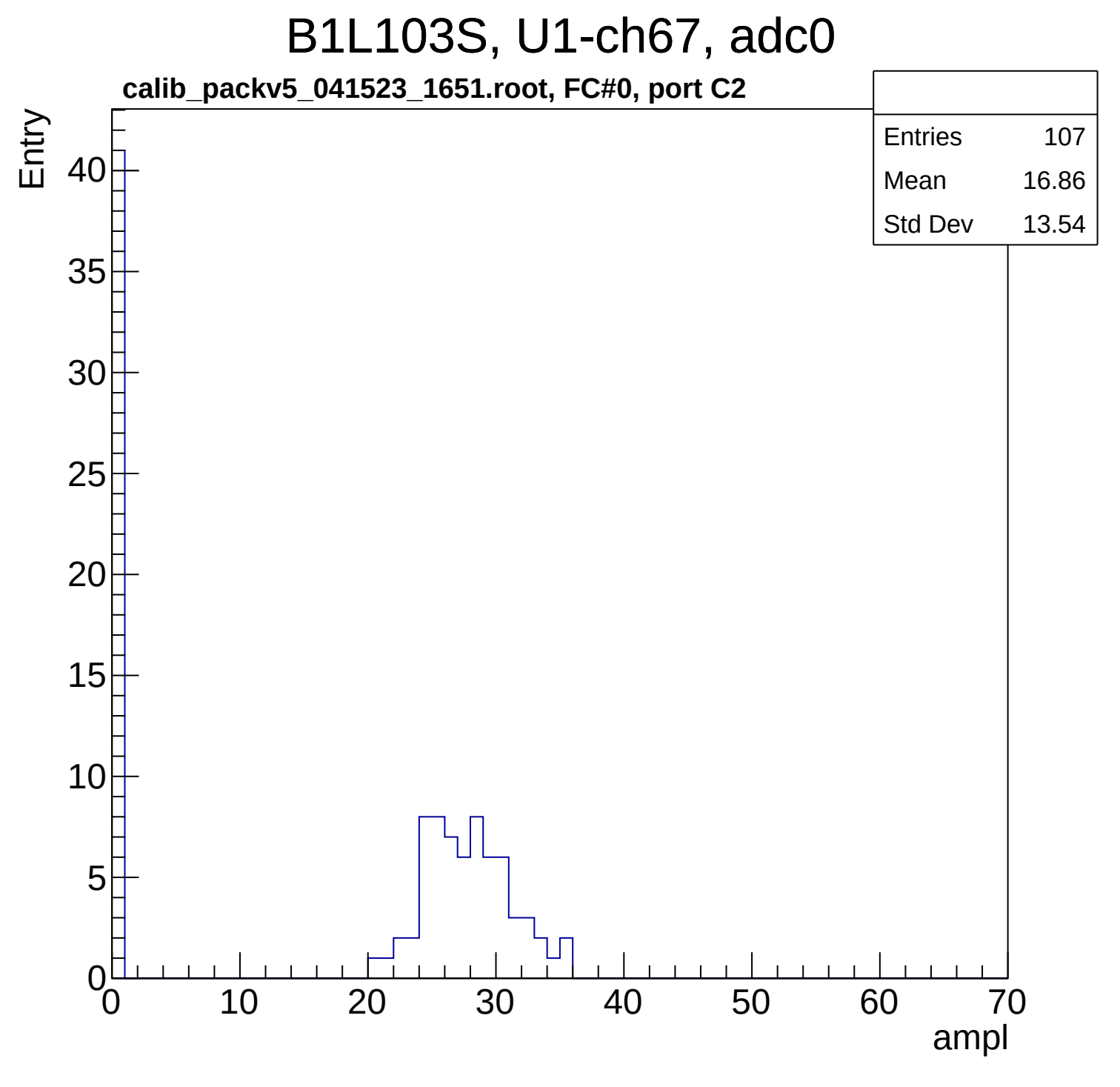
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch67, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 107
Mean 16.86
Std Dev 13.54
Entry
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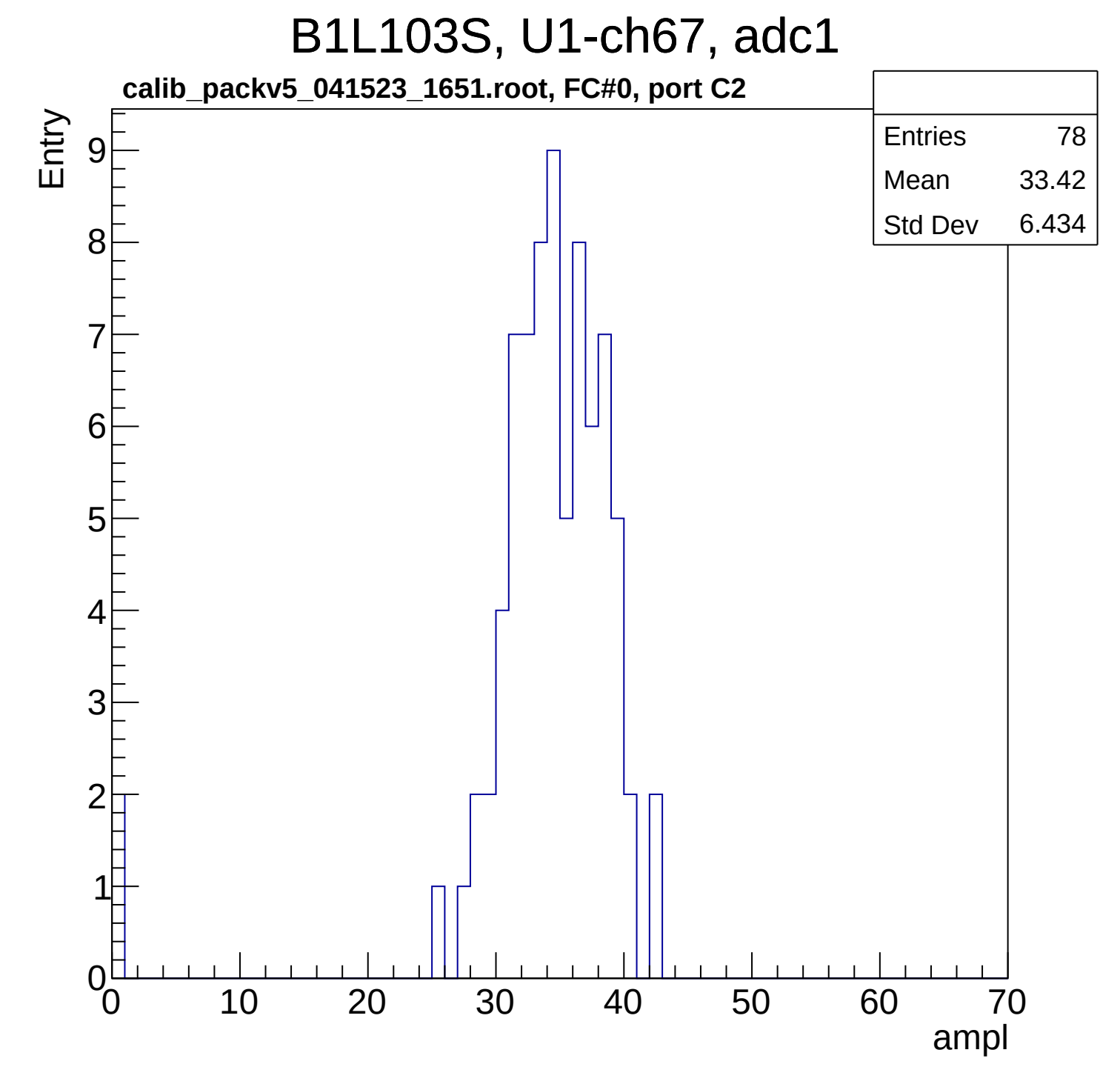
10
15
20
25
30
35
40
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch67, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 33.42
Std Dev 6.434
Entry
ampl
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3
4
5
6
7
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0
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20
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60
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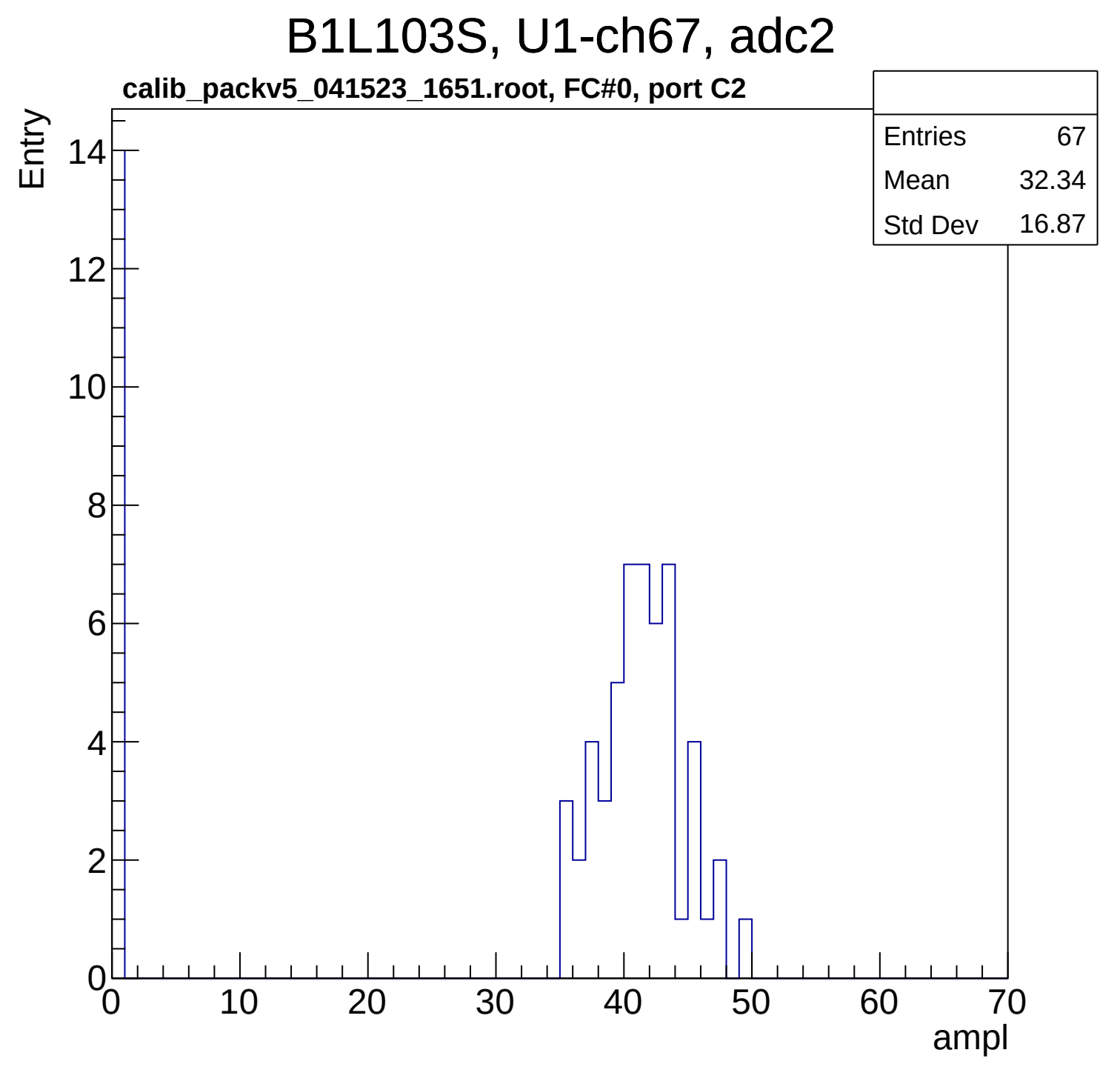
B1L103S, U1-ch67, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 32.34
Std Dev 16.87
Entry
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4
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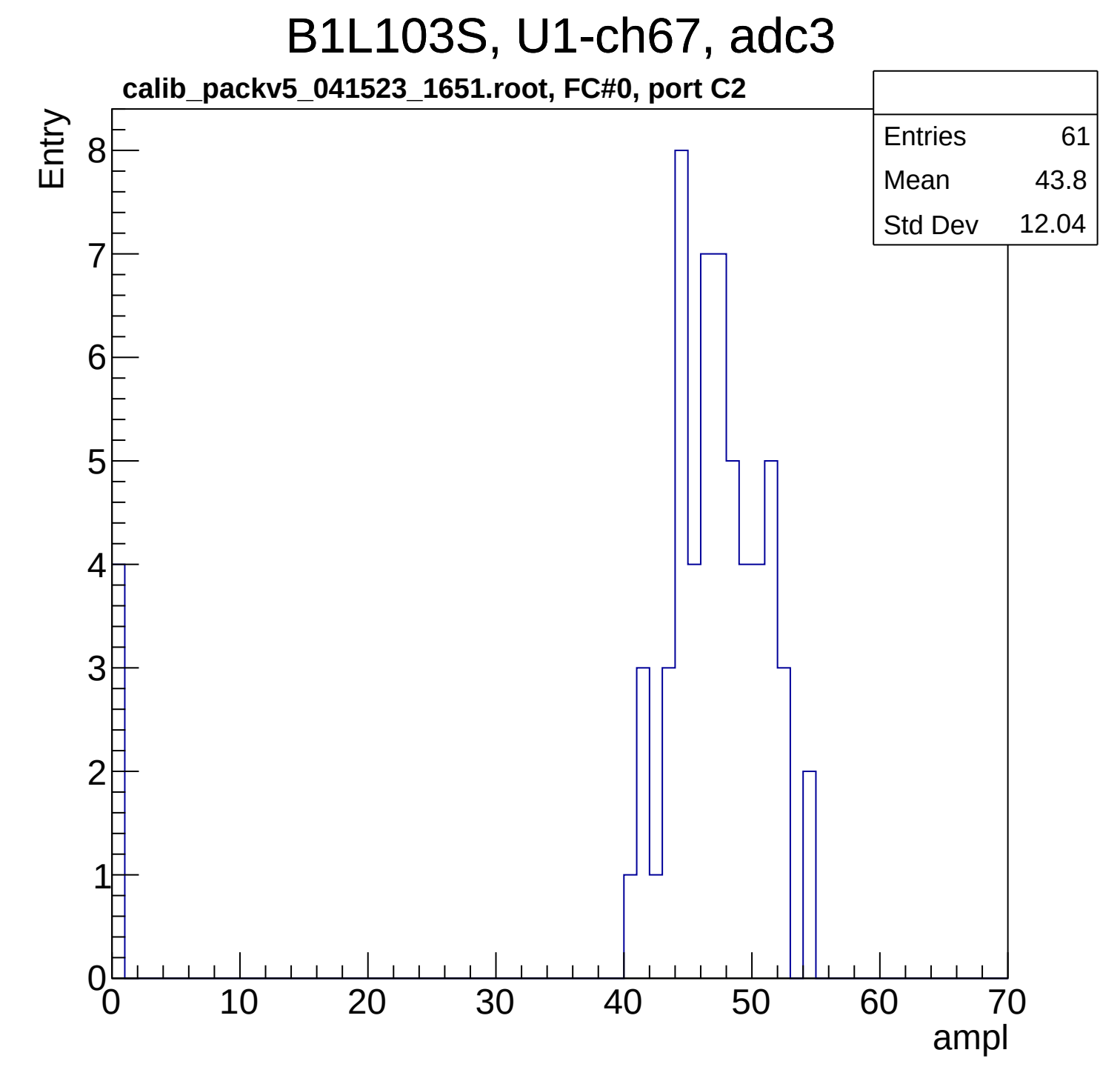
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch67, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 43.8
Std Dev 12.04
Entry
ampl
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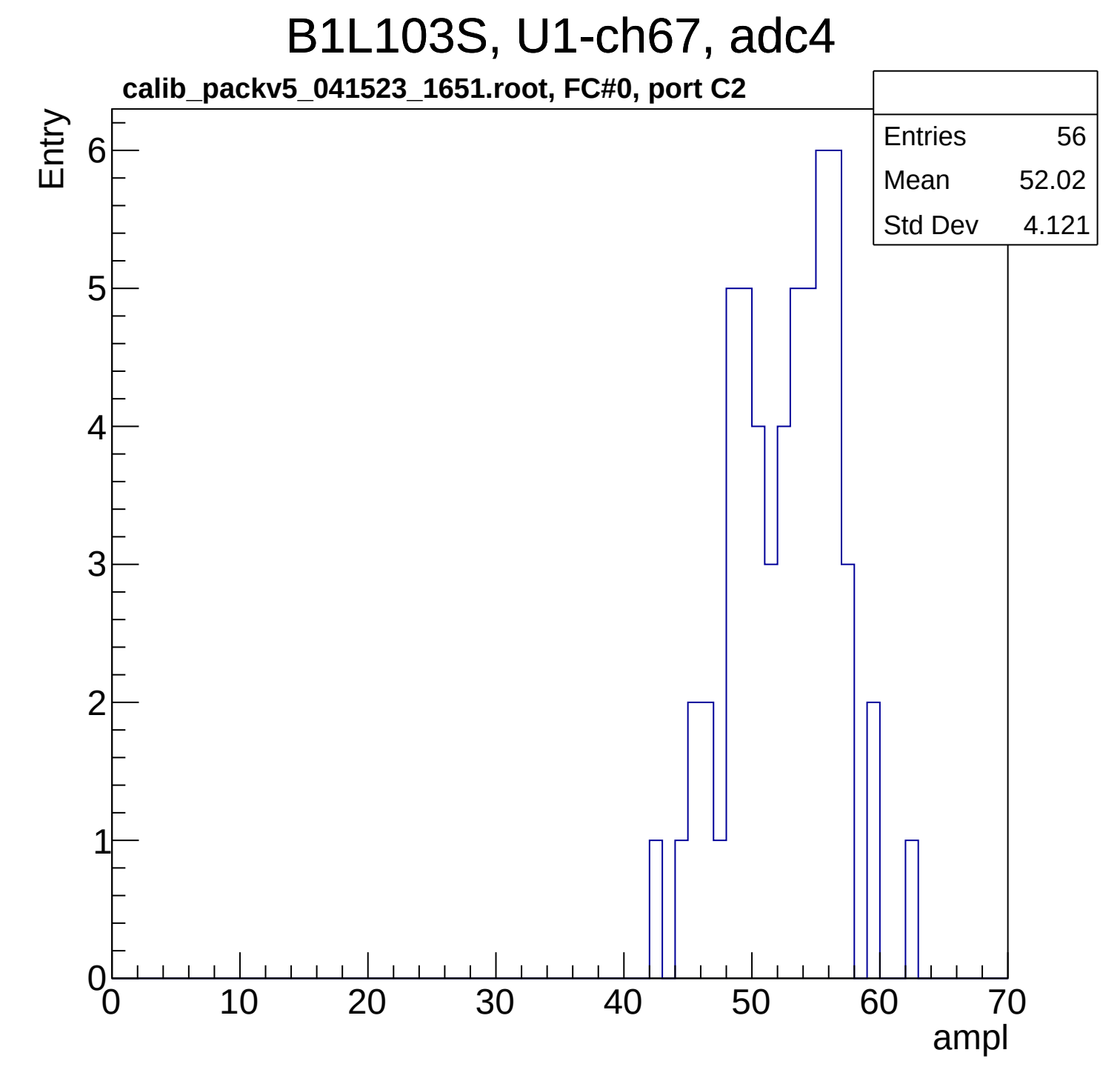
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U1-ch67, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 52.02
Std Dev 4.121
Entry
ampl
0
1
2
3
4
5
6
0
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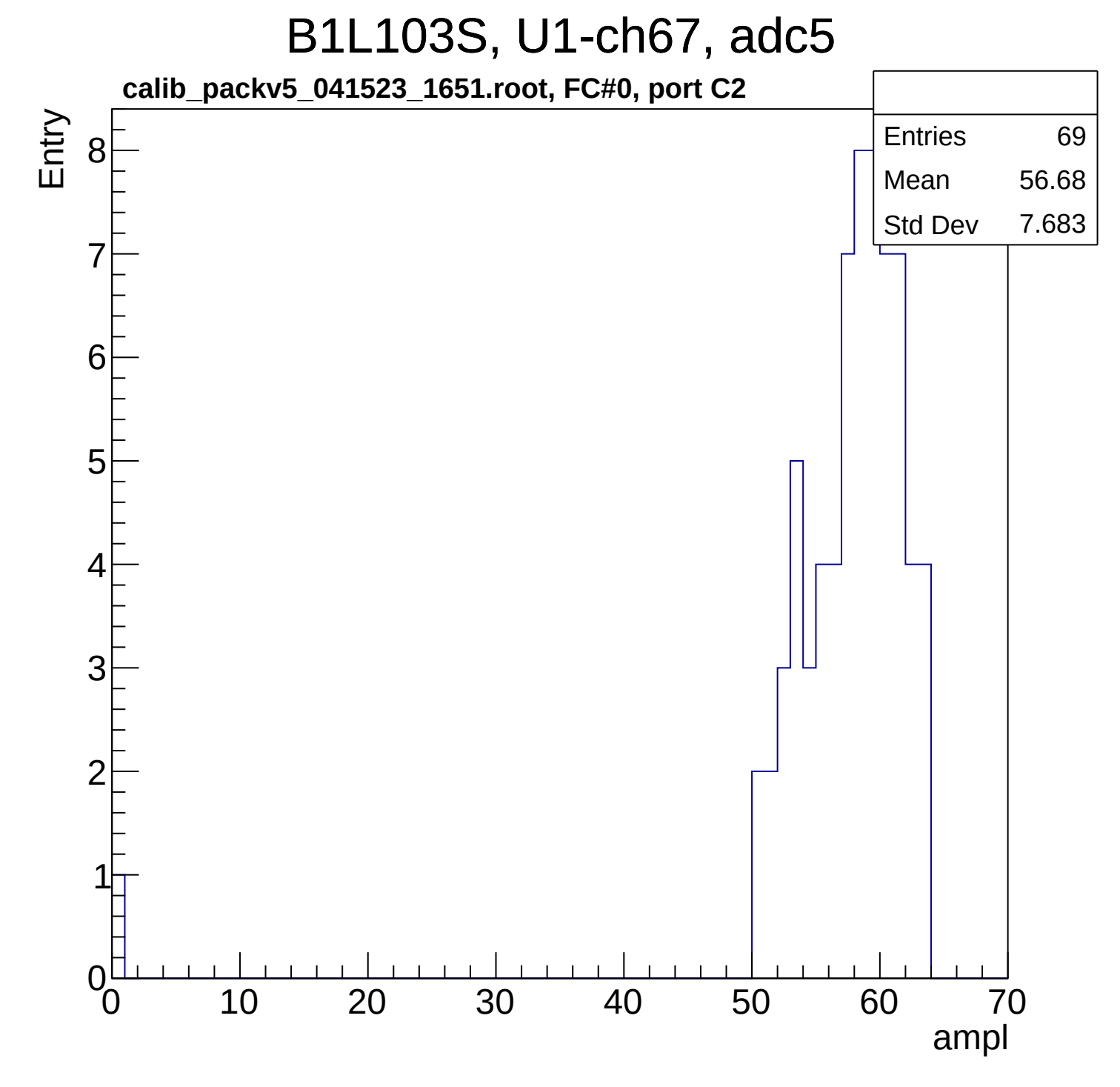
20
30
40
50
60
70


B1L103S, U1-ch67, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 56.68
Std Dev 7.683
Entry
ampl
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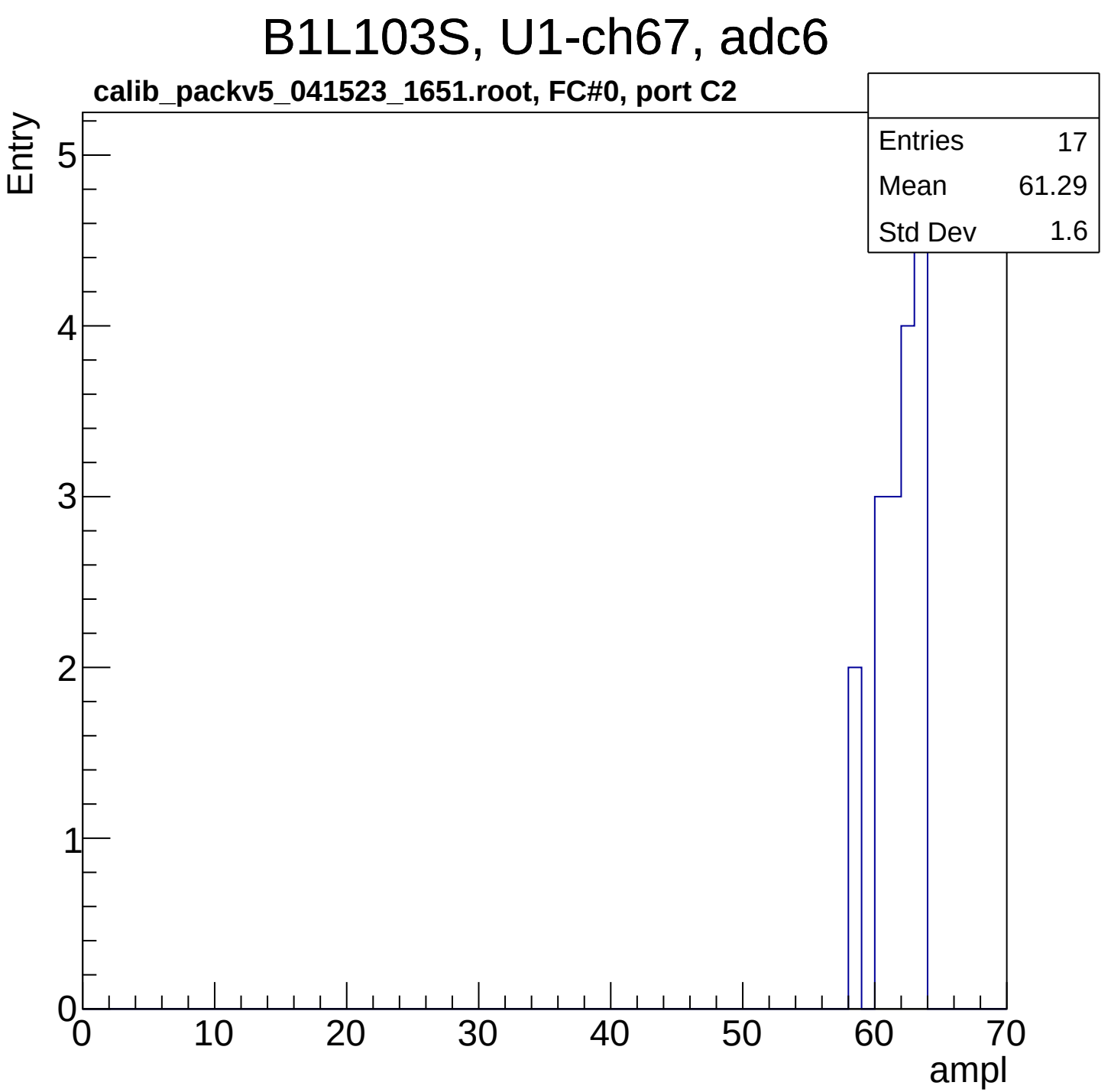
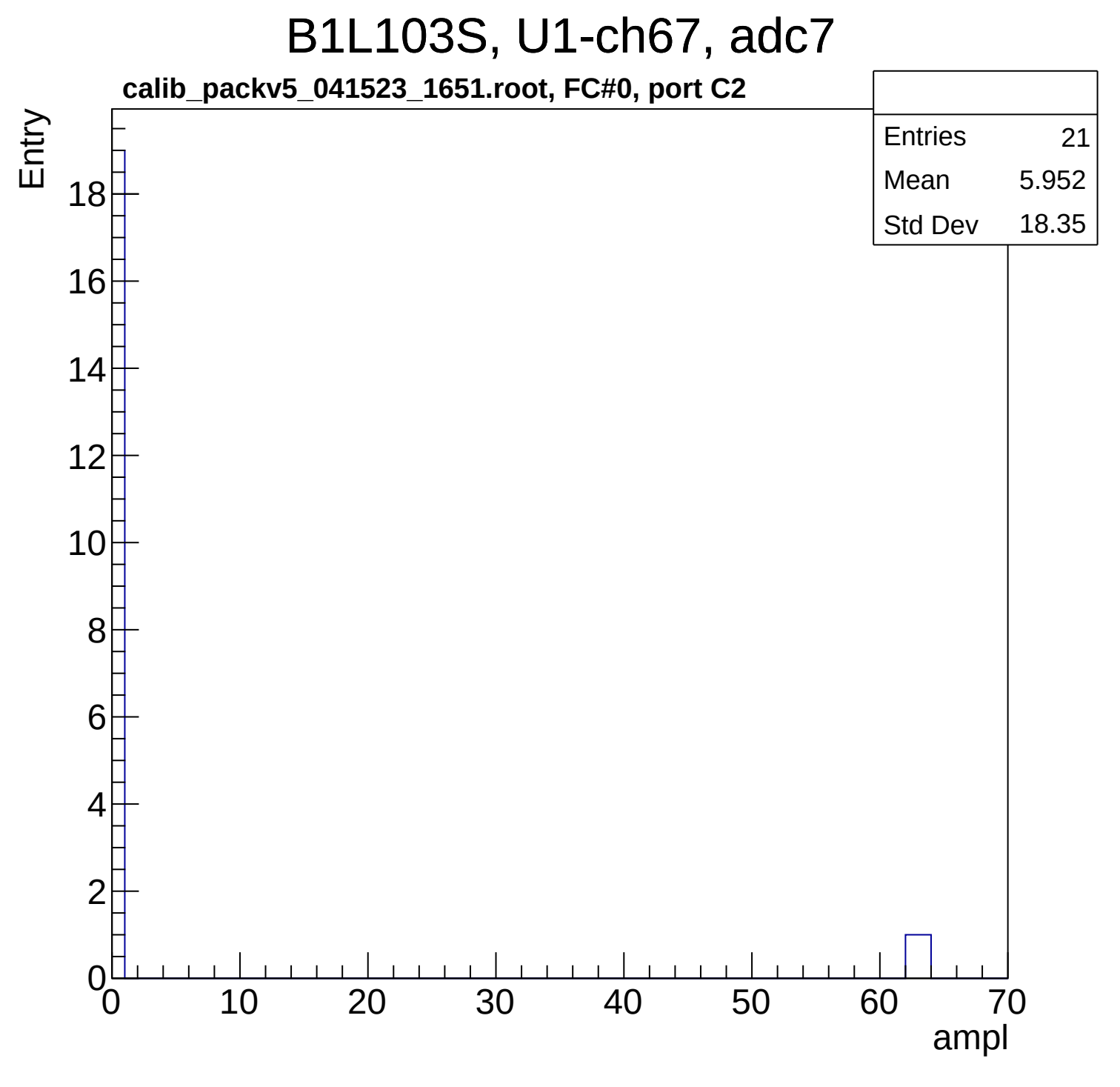
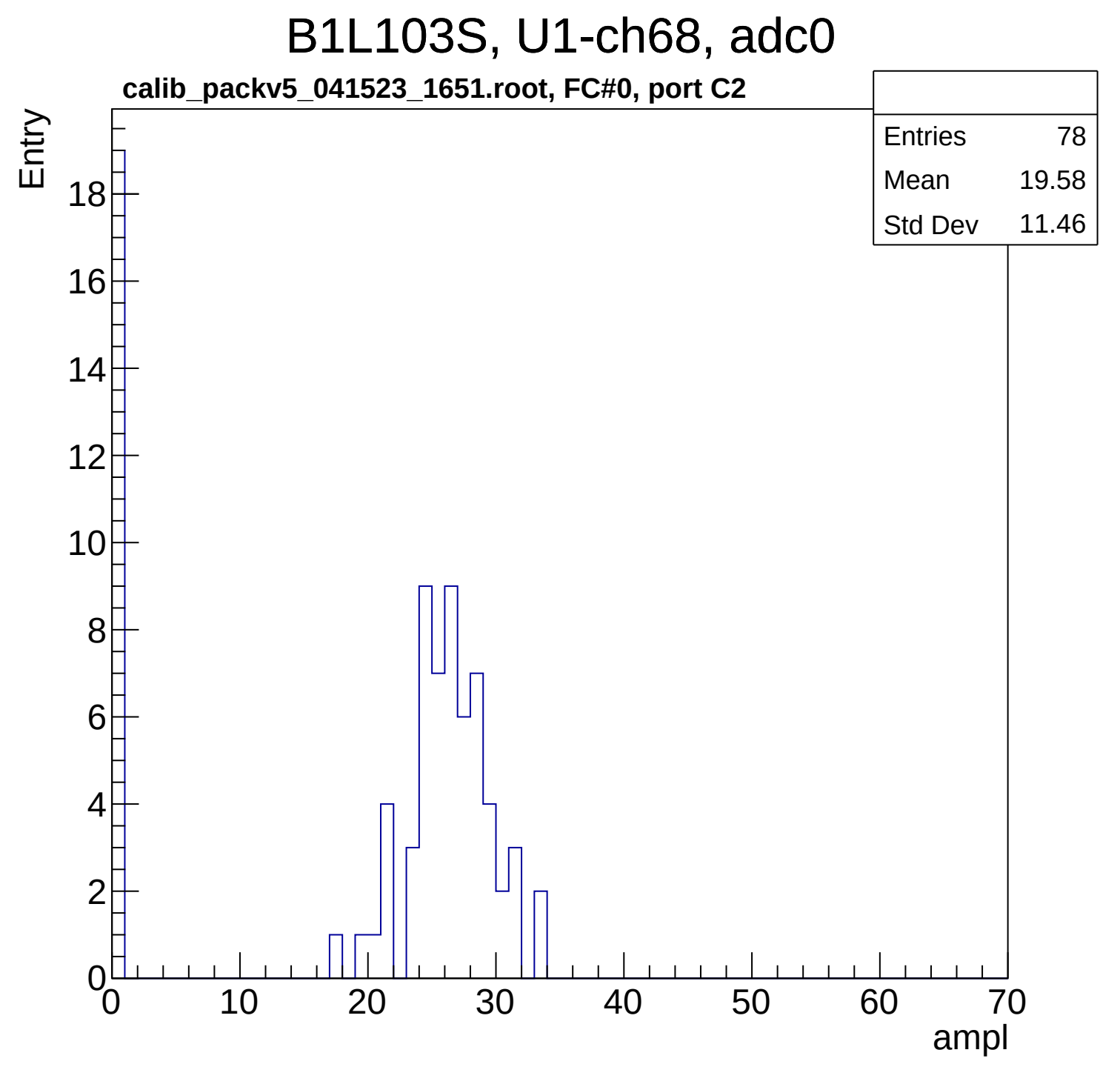
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U1-ch67, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 17
Mean 61.29
Std Dev 1.6
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch67, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 5.952
Std Dev 18.35
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch68, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 19.58
Std Dev 11.46
Entry
ampl
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4
6
8
10
12
14
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0
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40
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60
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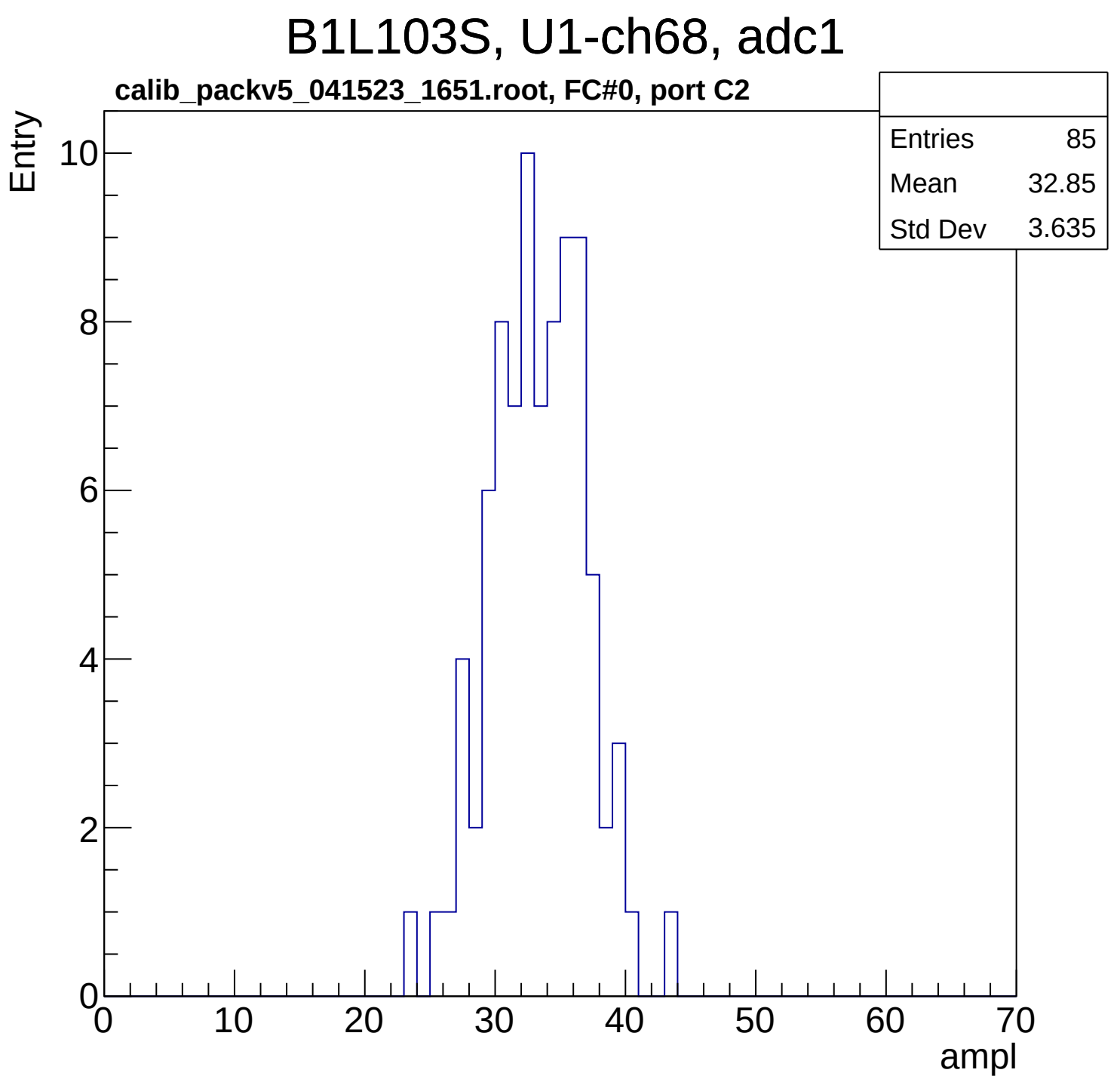
B1L103S, U1-ch68, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 32.85
Std Dev 3.635
Entry
ampl
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4
6
8
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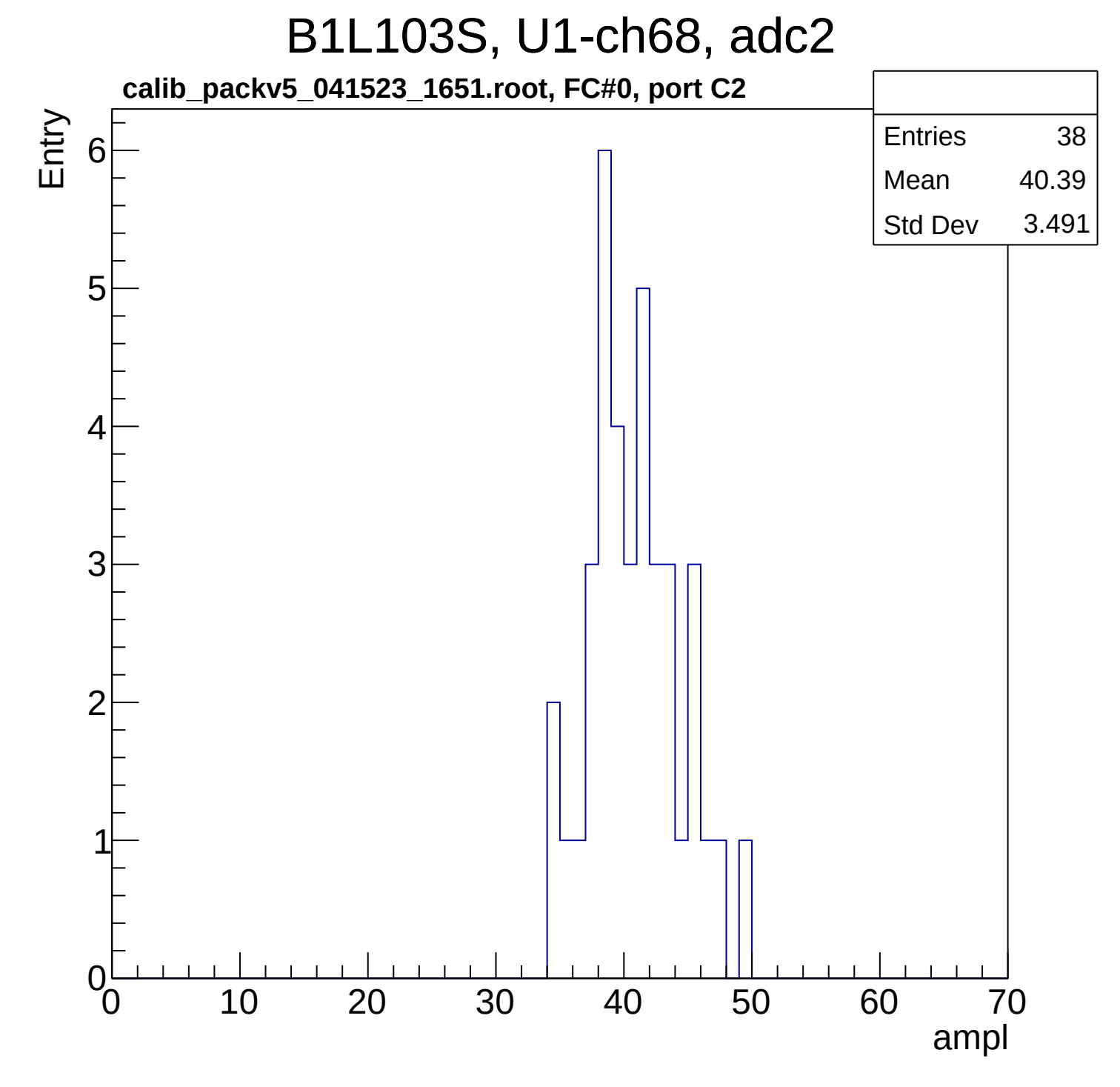
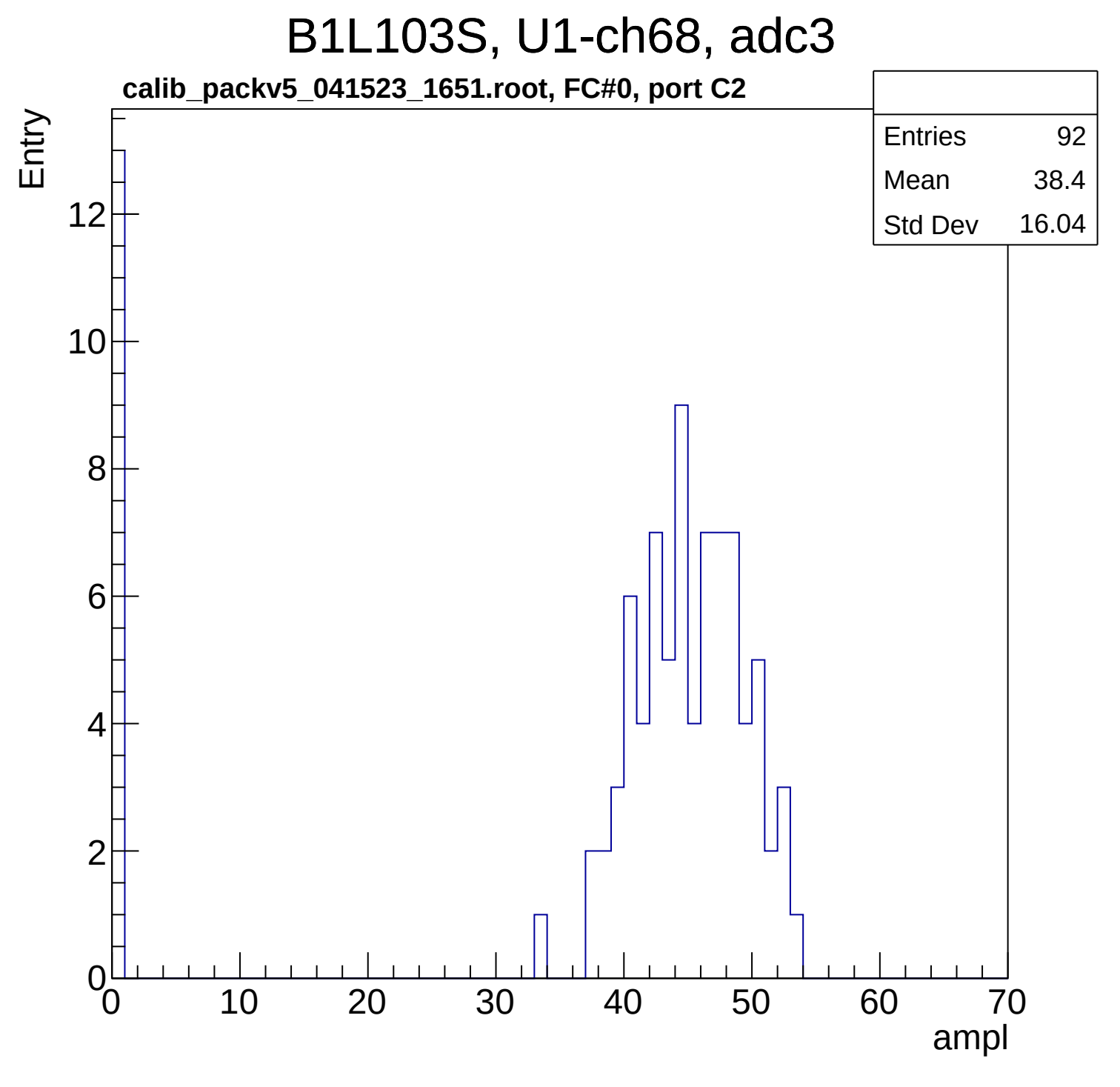
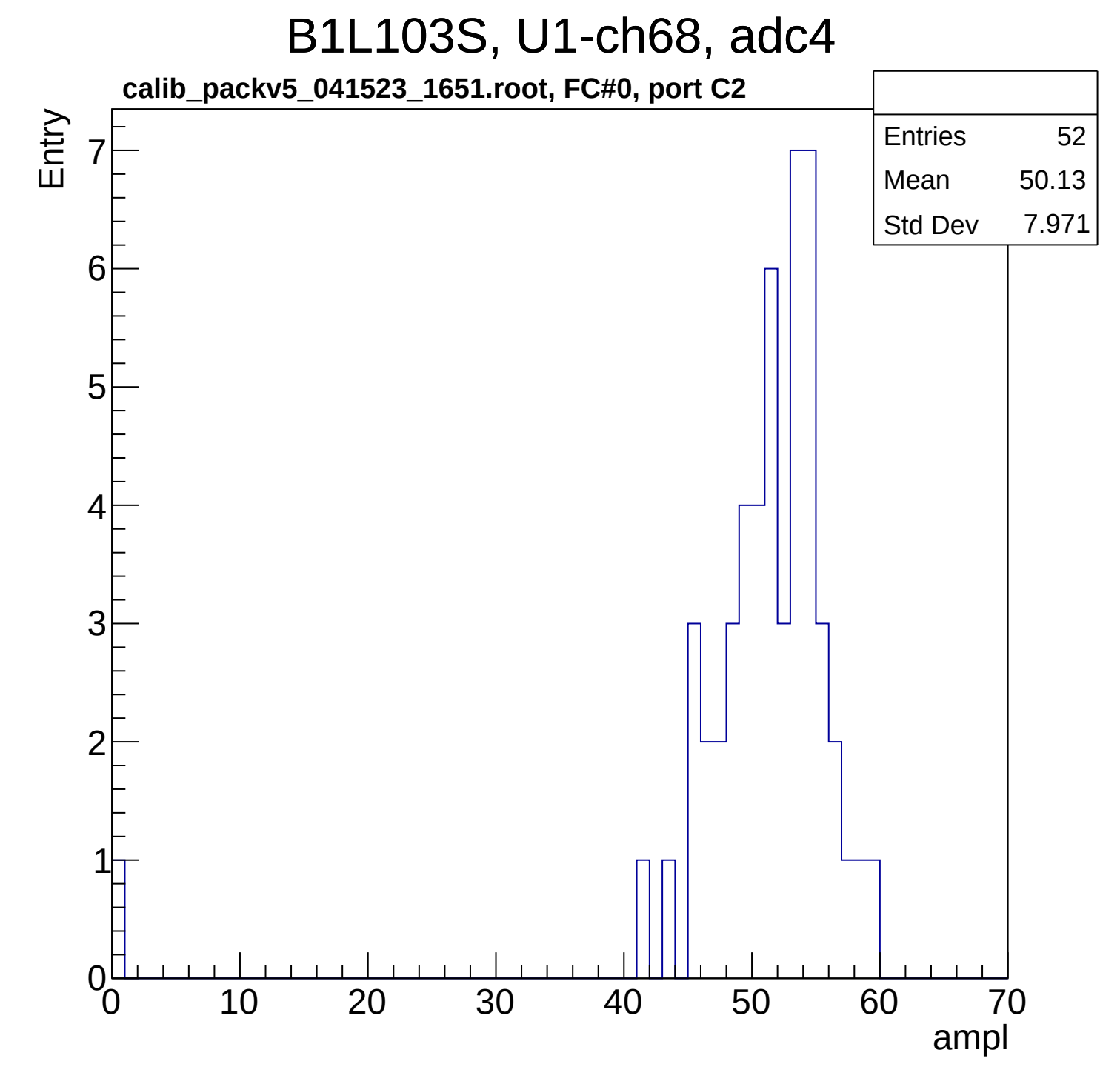
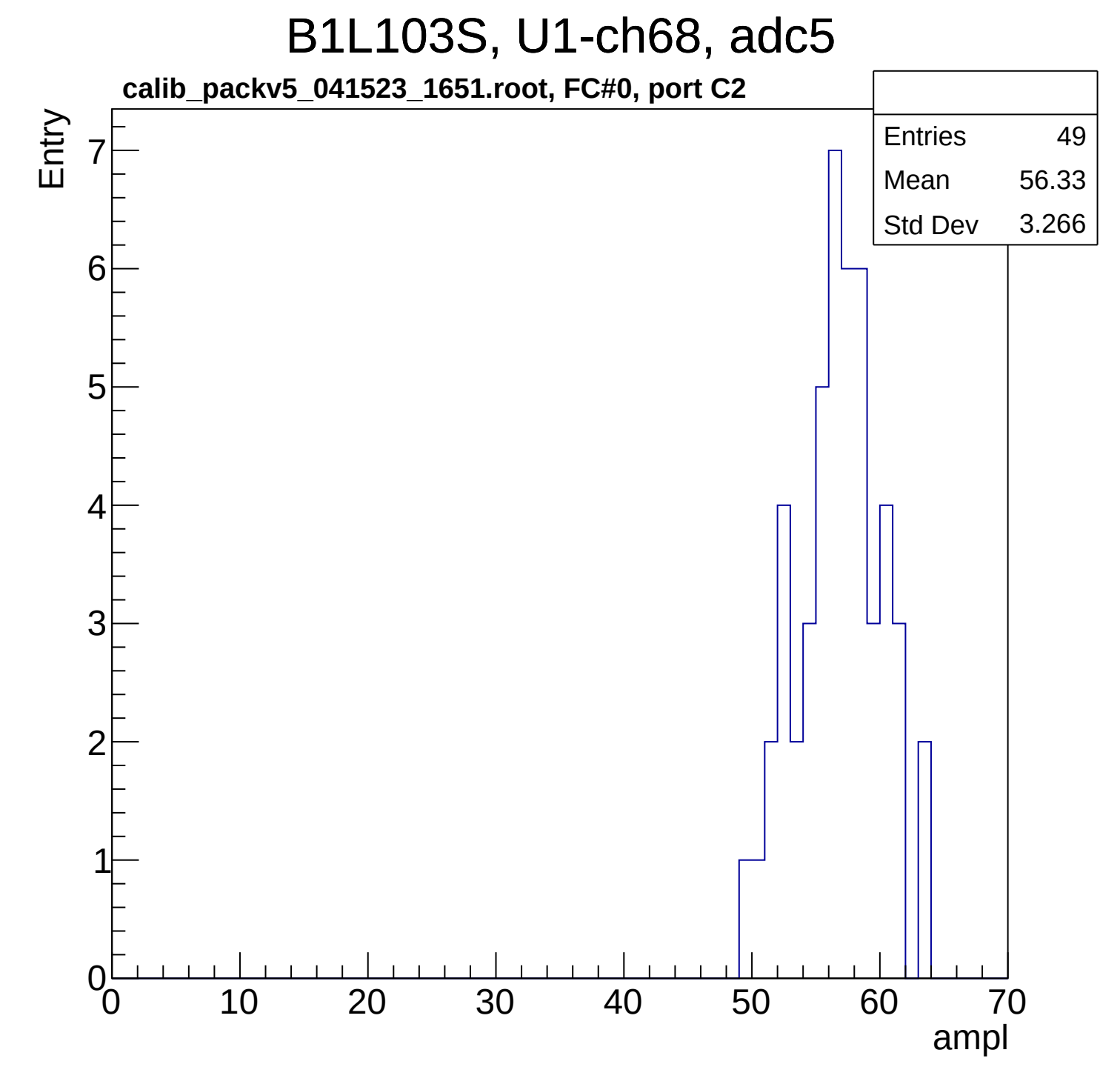
0
10
20
30
40
50
60
70


B1L103S, U1-ch68, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 38
Mean 40.39
Std Dev 3.491
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch68, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 92
Mean 38.4
Std Dev 16.04
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch68, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 50.13
Std Dev 7.971
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U1-ch68, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 56.33
Std Dev 3.266
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
30
40
50
60
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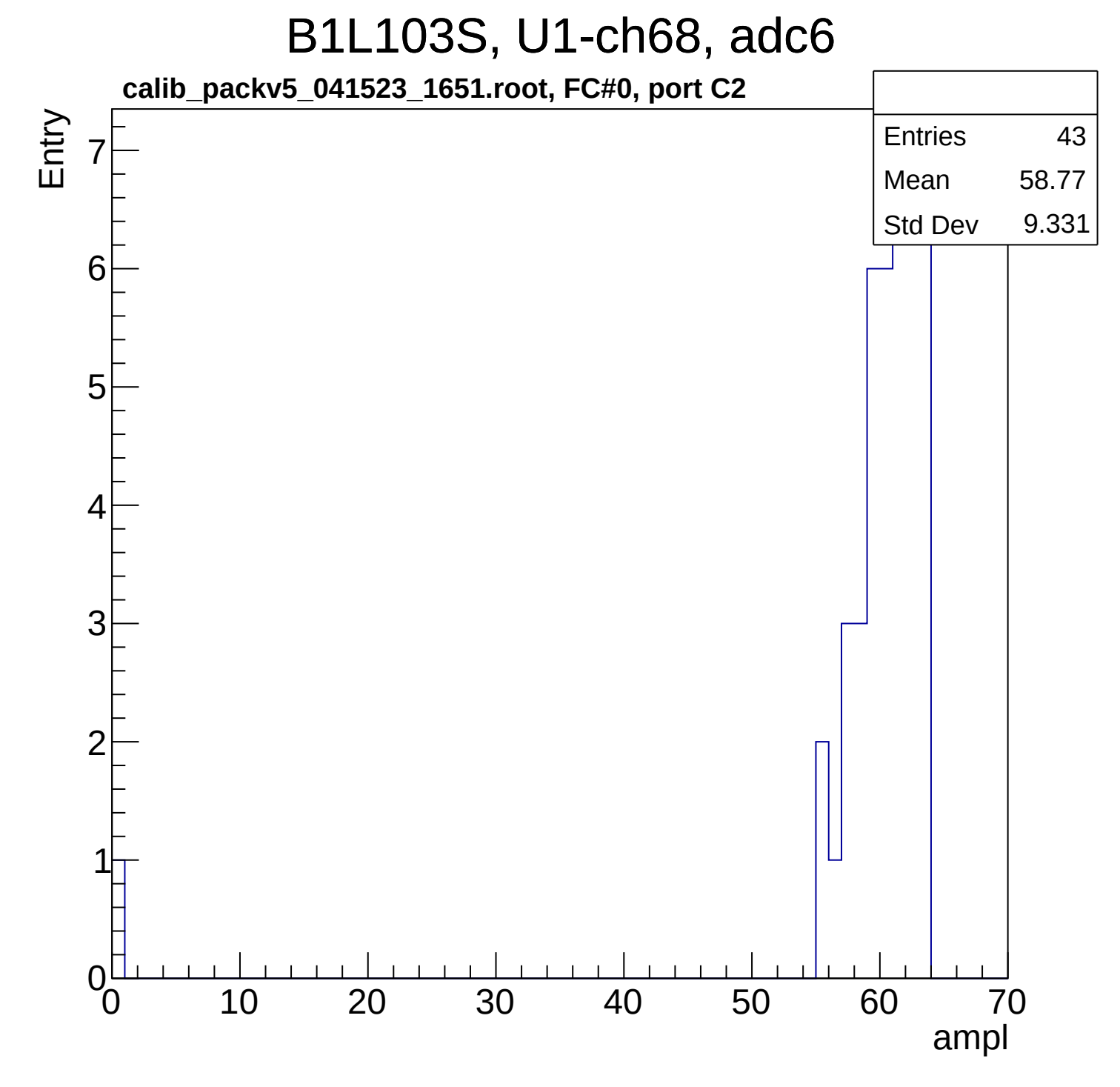
B1L103S, U1-ch68, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 43
Mean 58.77
Std Dev 9.331
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
30
40
50
60
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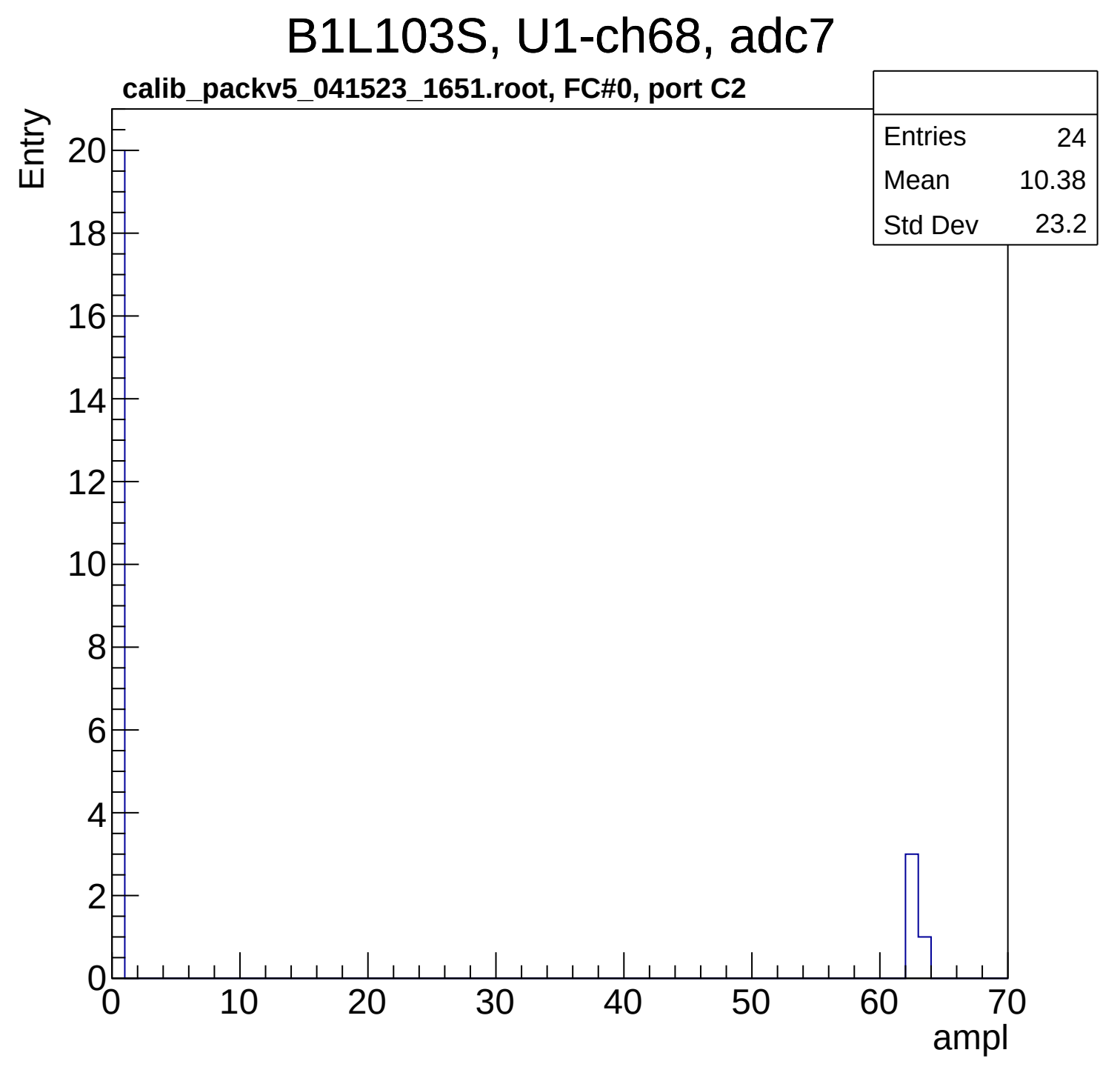
B1L103S, U1-ch68, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 24
Mean 10.38
Std Dev 23.2
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
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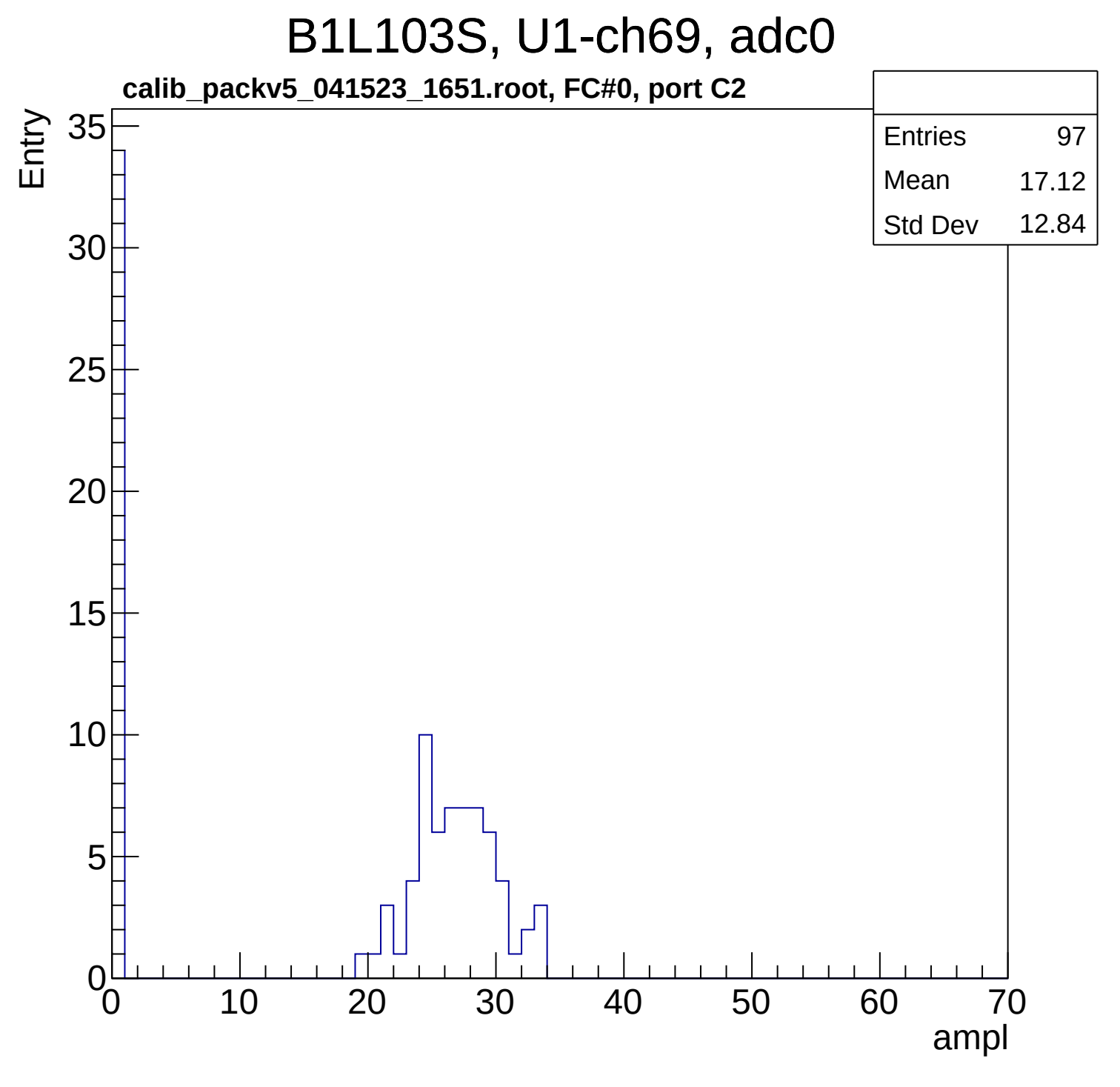
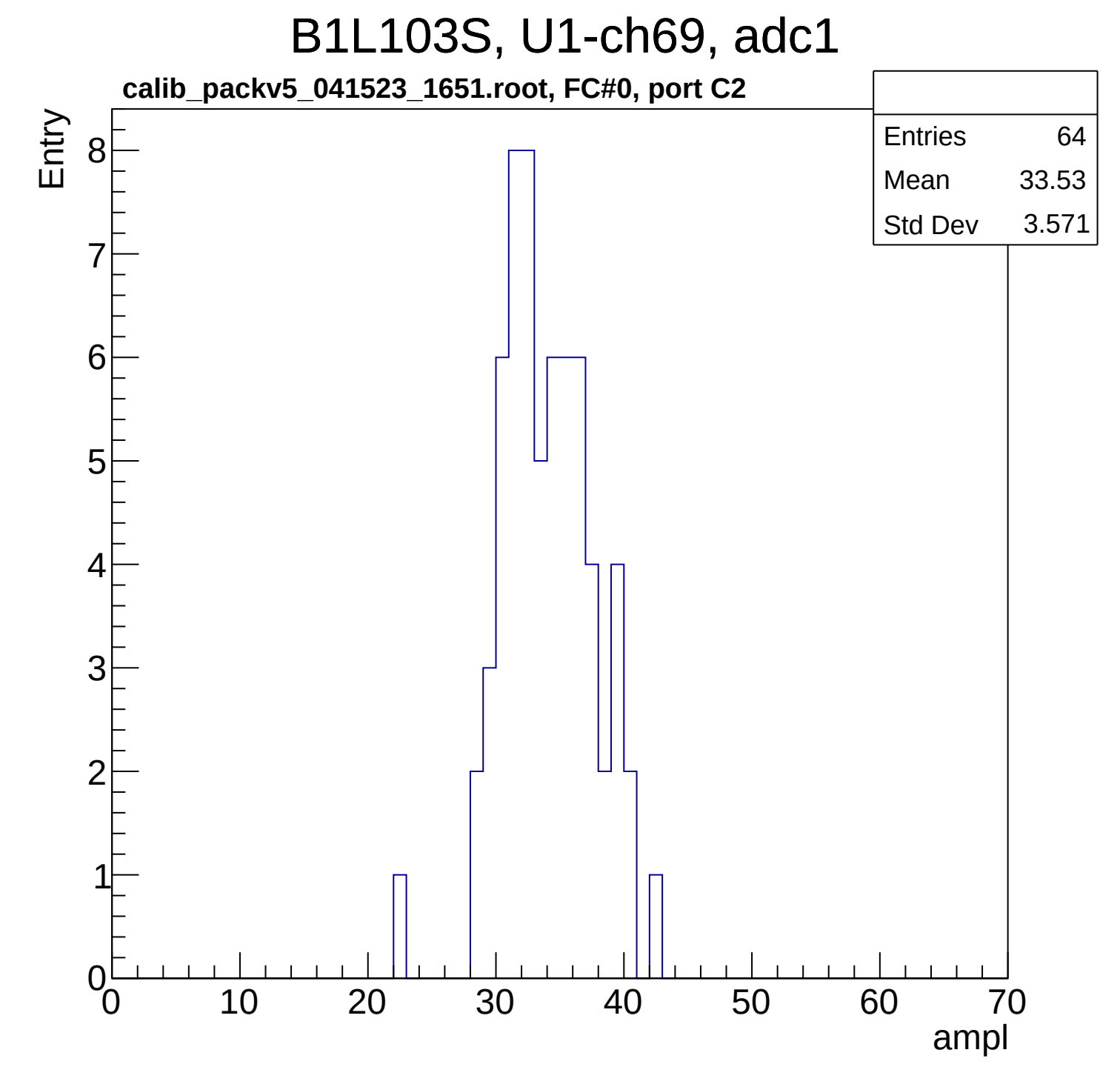
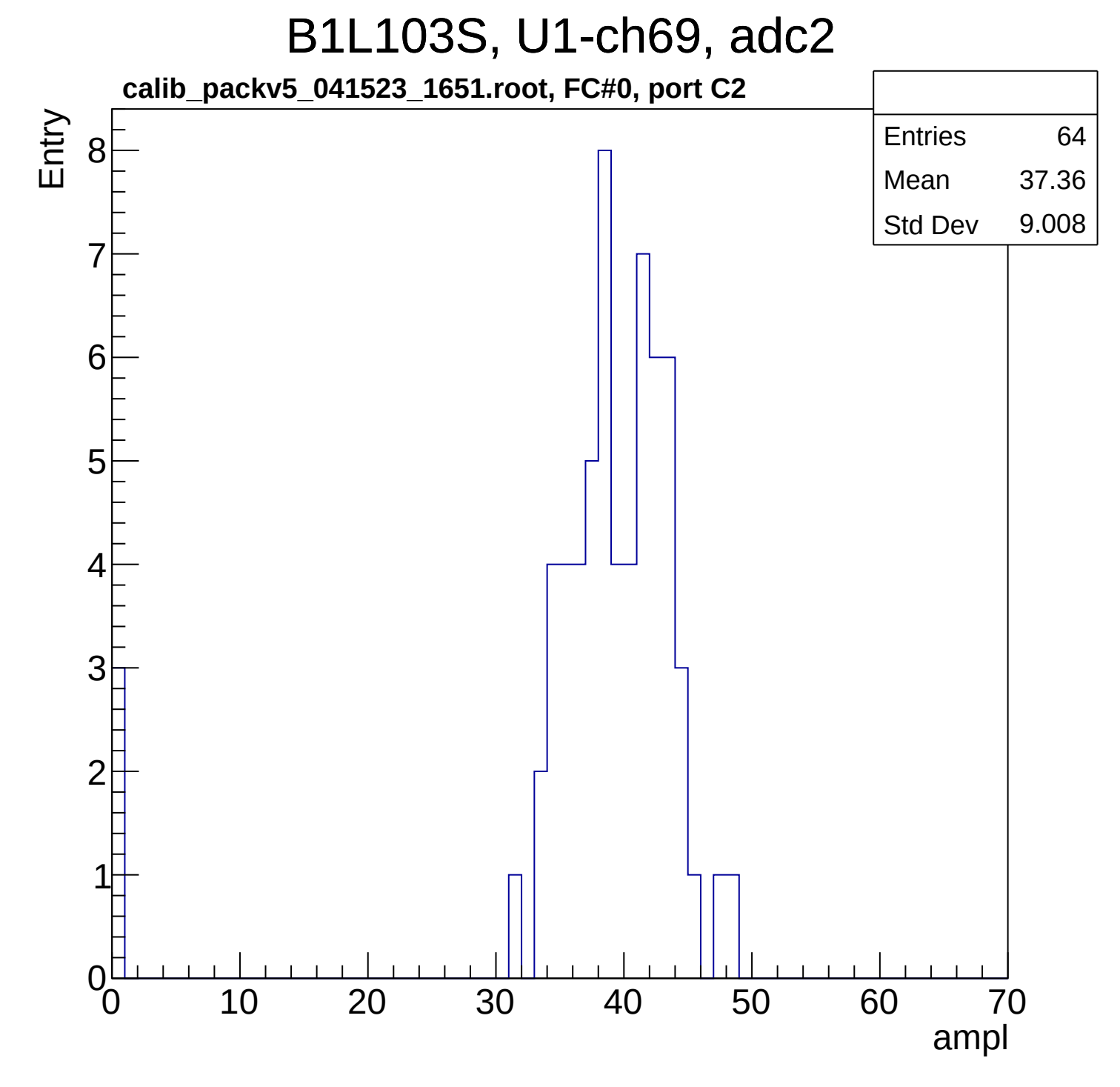

B1L103S, U1-ch69, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 97
Mean 17.12
Std Dev 12.84
Entry
ampl
0
5
10
15
20
25
30
35
0
10
20
30
40
50
60
70


B1L103S, U1-ch69, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 33.53
Std Dev 3.571
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U1-ch69, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 37.36
Std Dev 9.008
Entry
ampl
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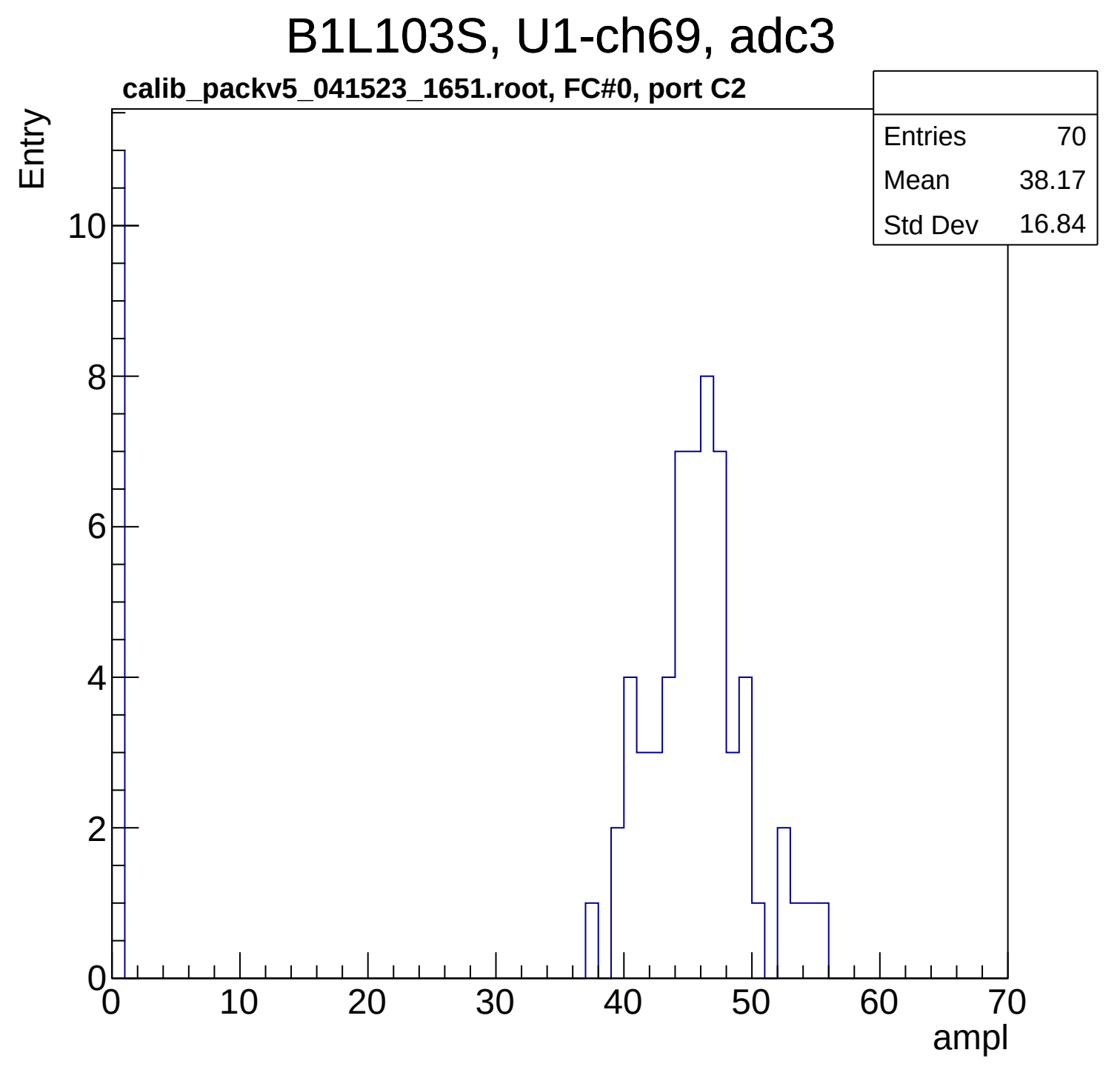
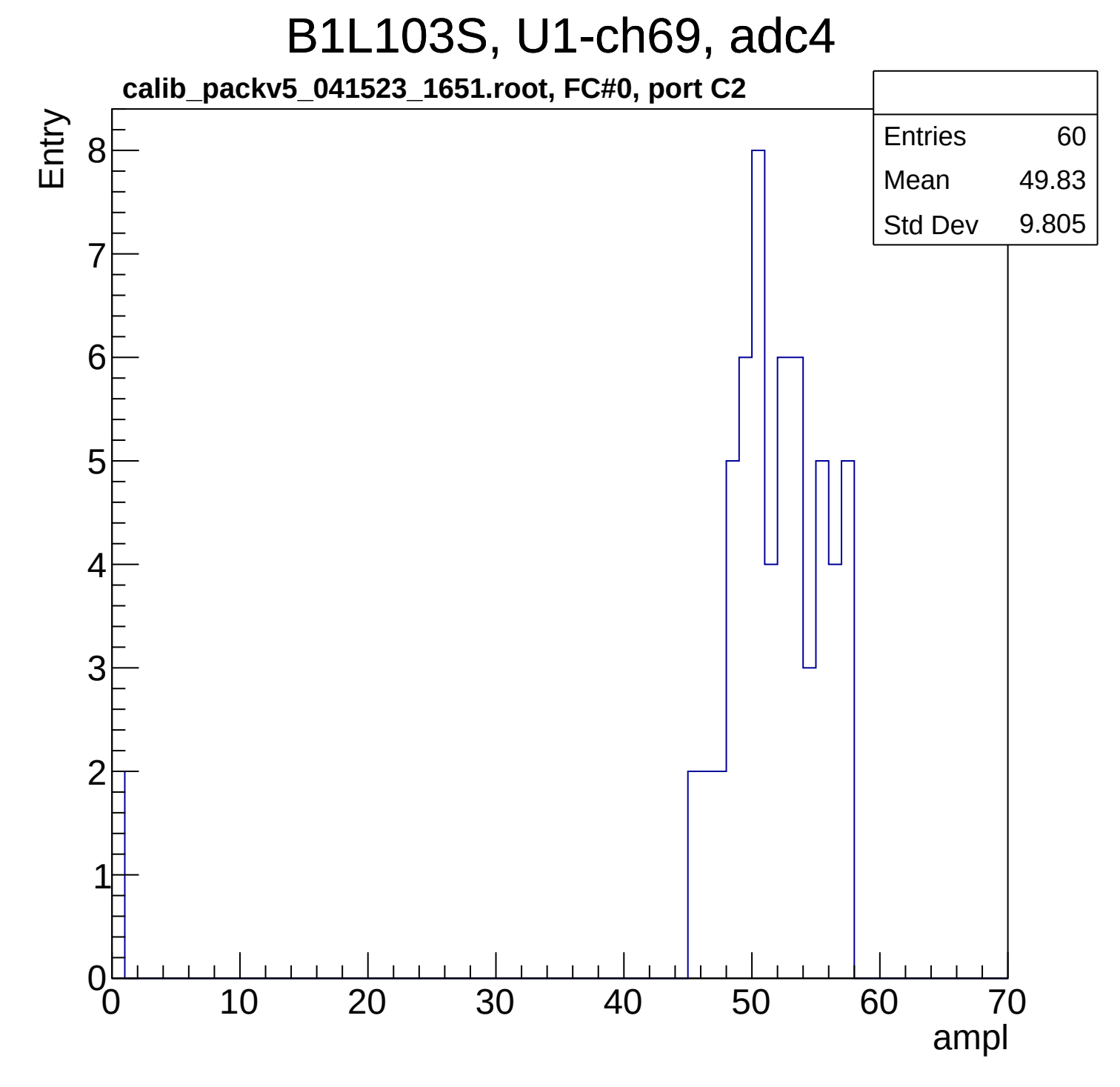
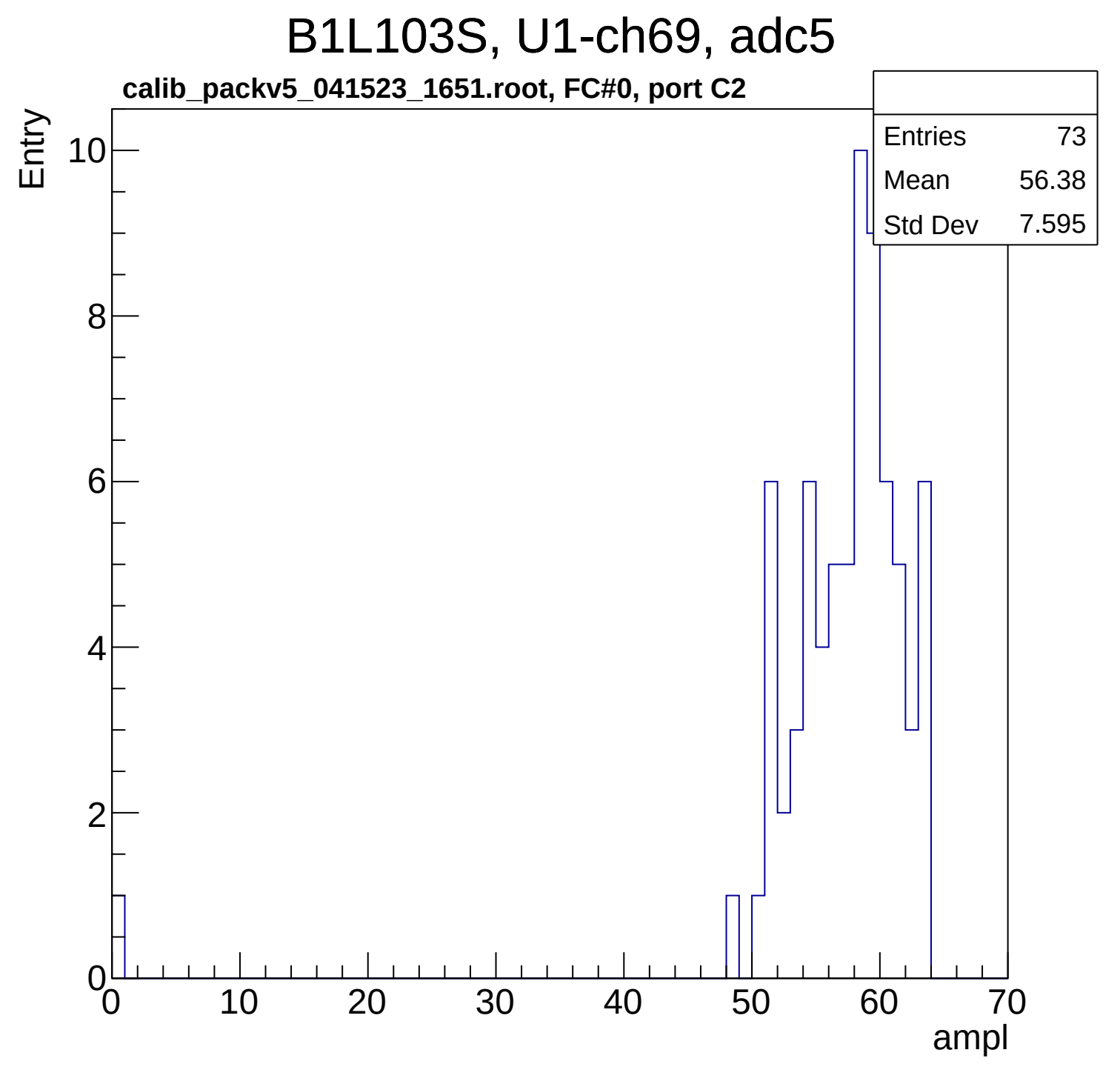
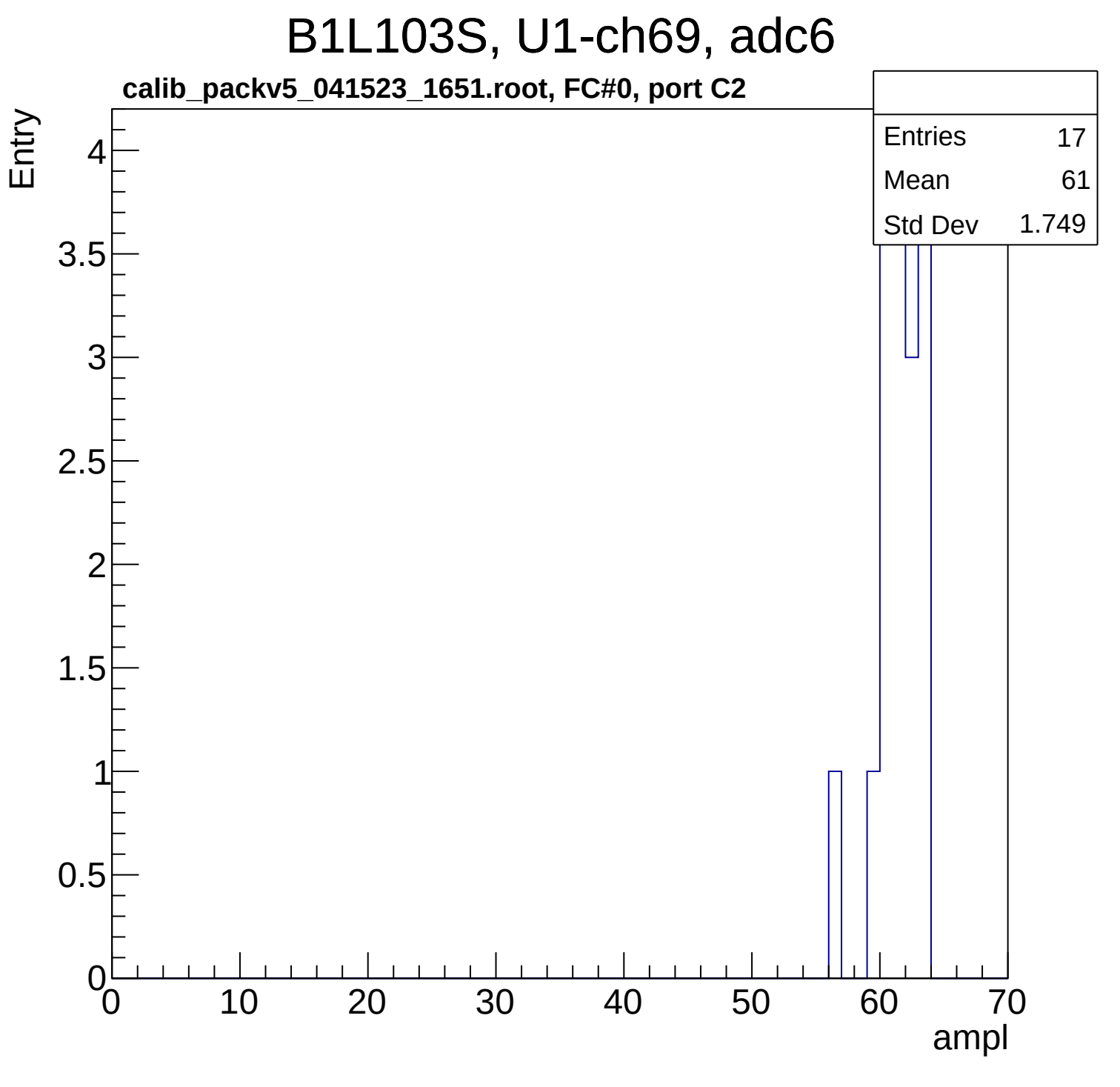
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U1-ch69, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 38.17
Std Dev 16.84
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch69, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 49.83
Std Dev 9.805
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U1-ch69, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 56.38
Std Dev 7.595
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U1-ch69, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 17
Mean 61
Std Dev 1.749
Entry
ampl
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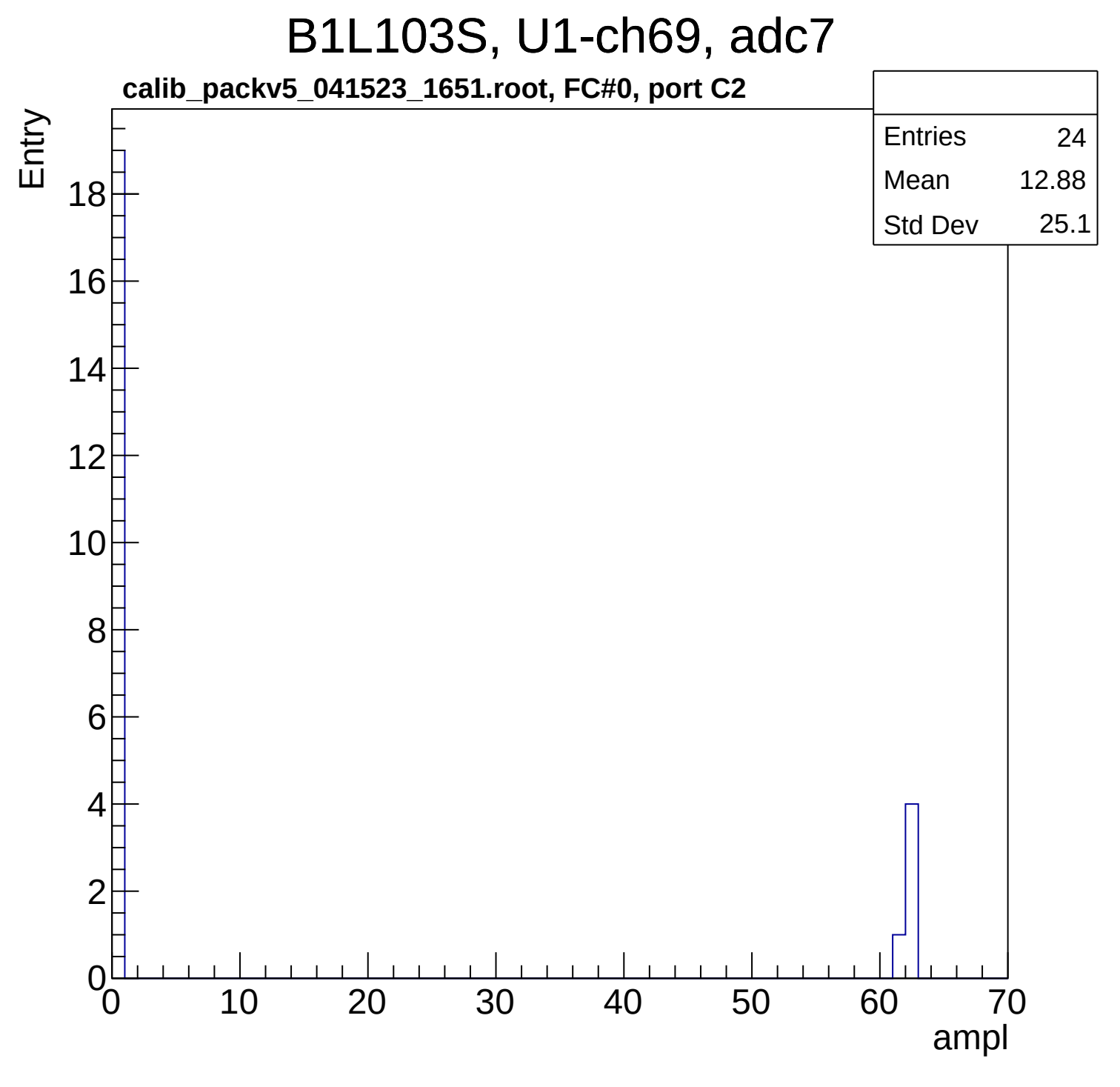
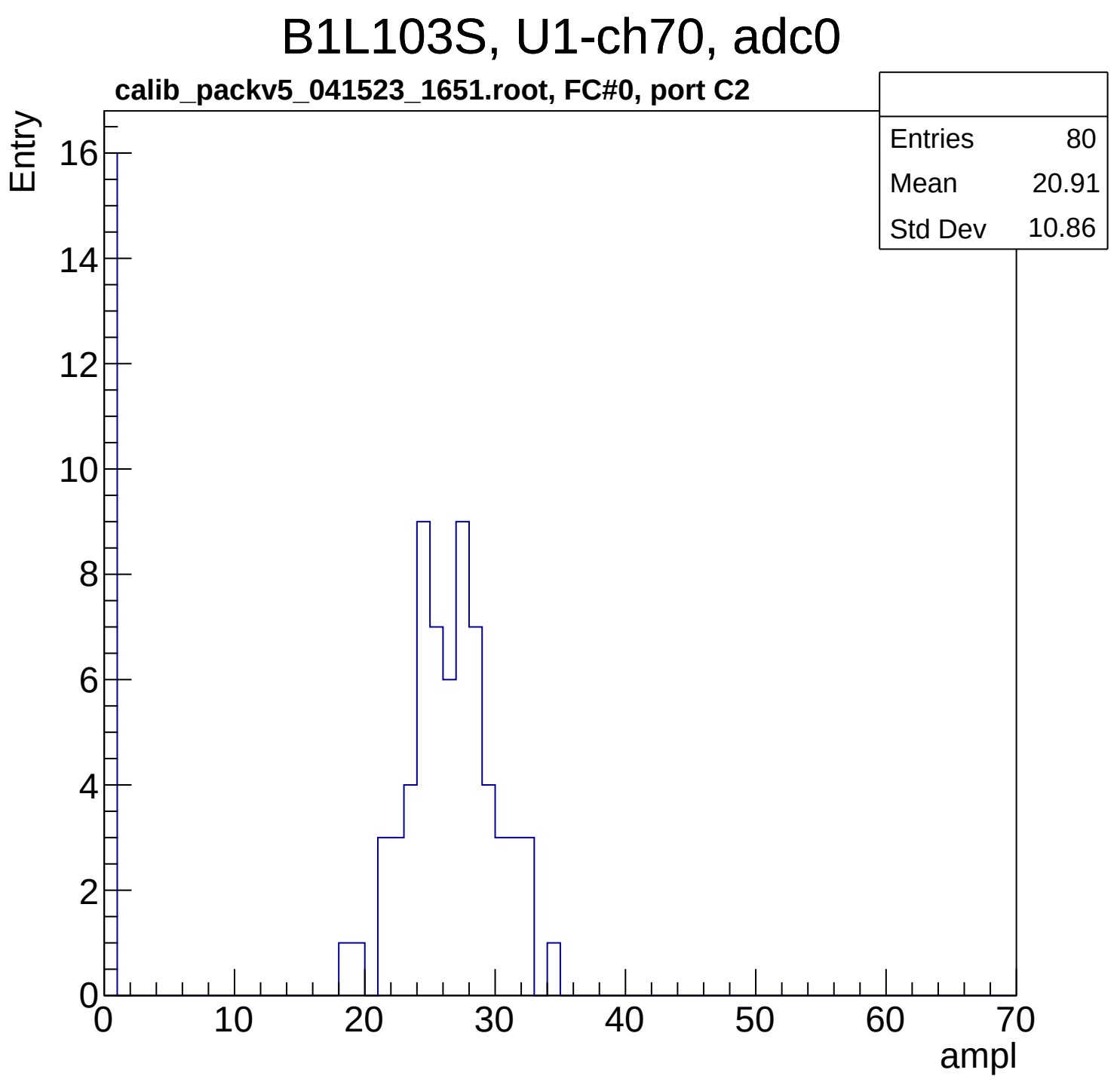
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U1-ch69, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 24
Mean 12.88
Std Dev 25.1
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch70, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 20.91
Std Dev 10.86
Entry
ampl
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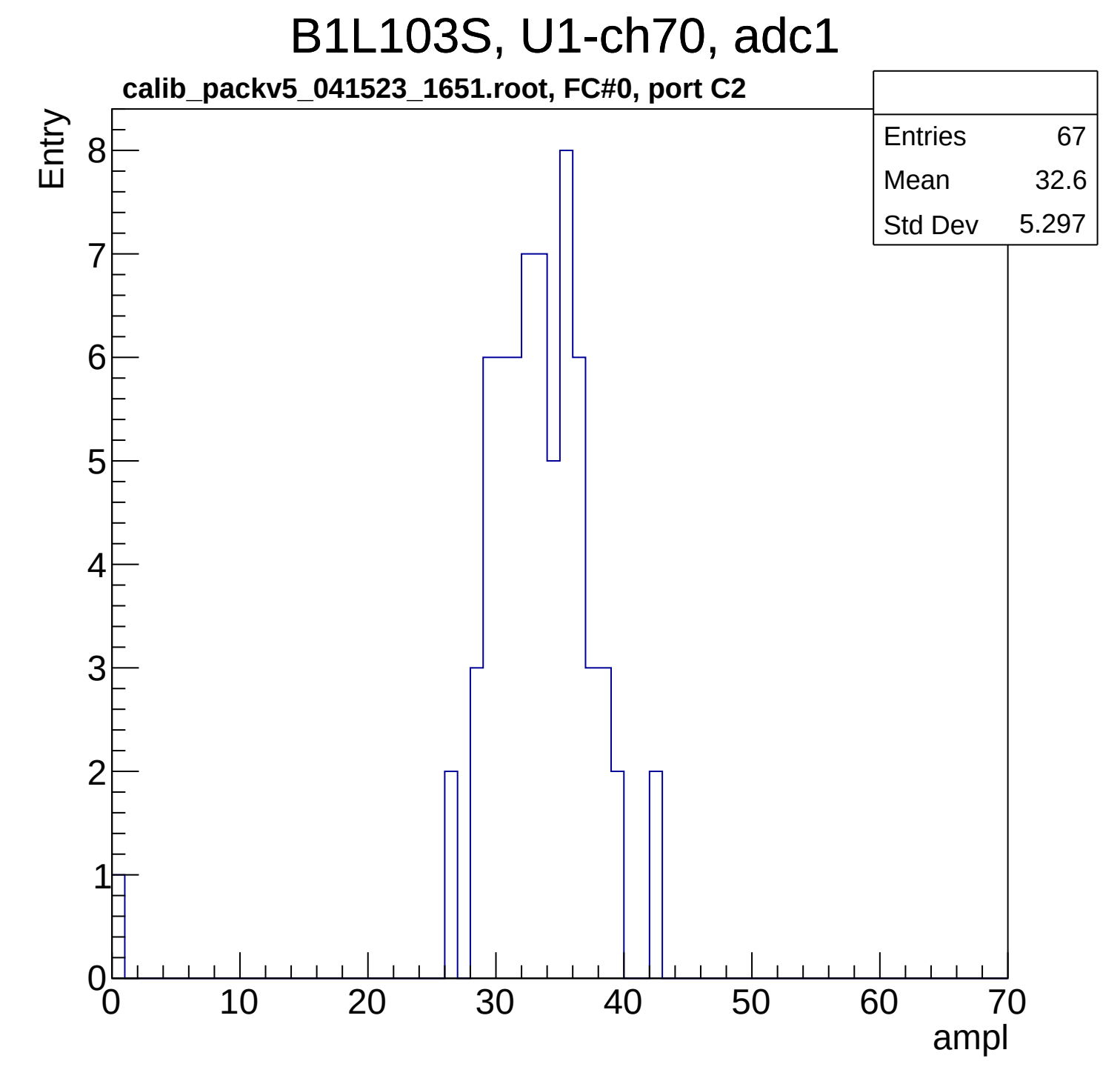
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70


B1L103S, U1-ch70, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 32.6
Std Dev 5.297
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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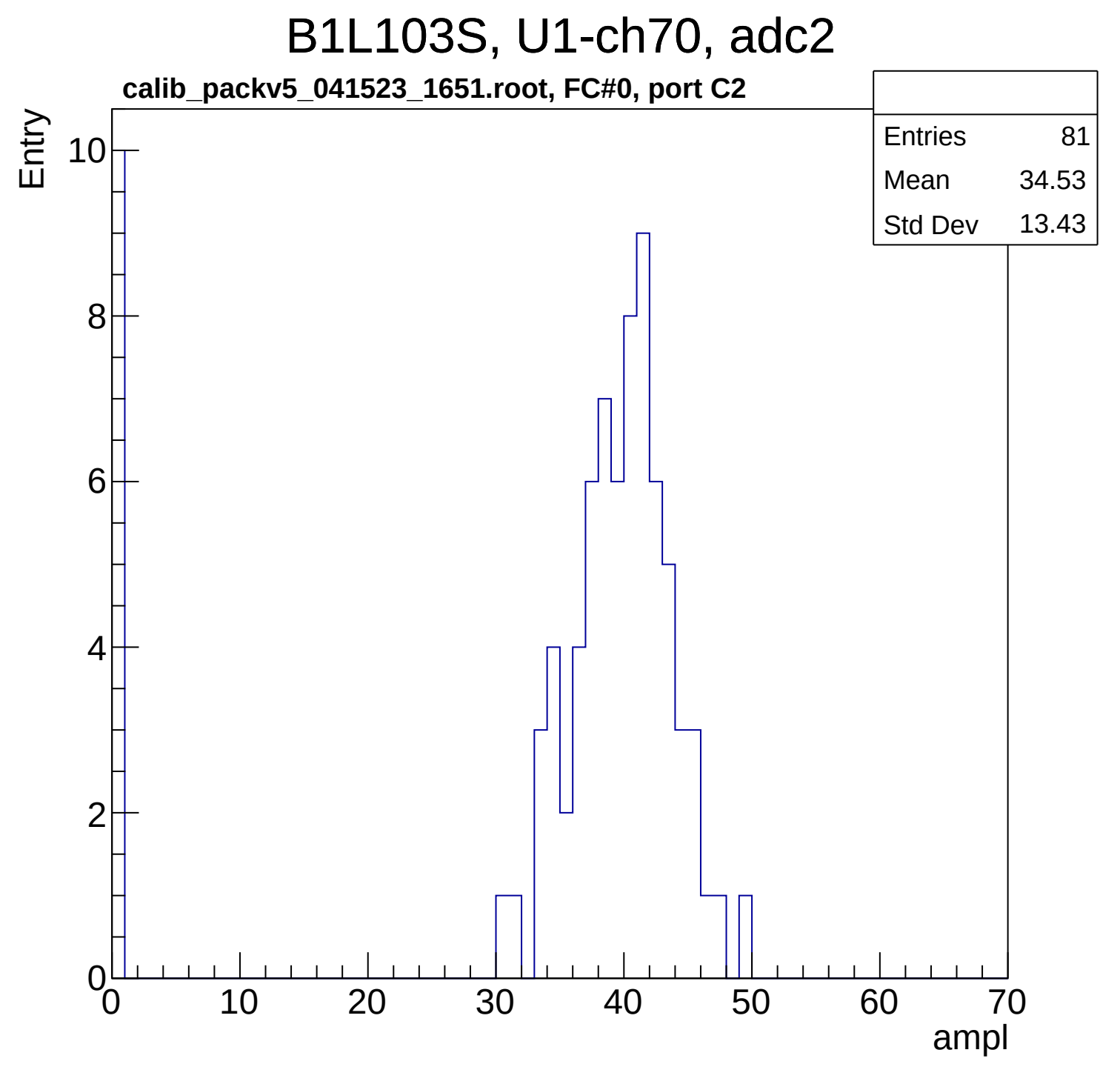
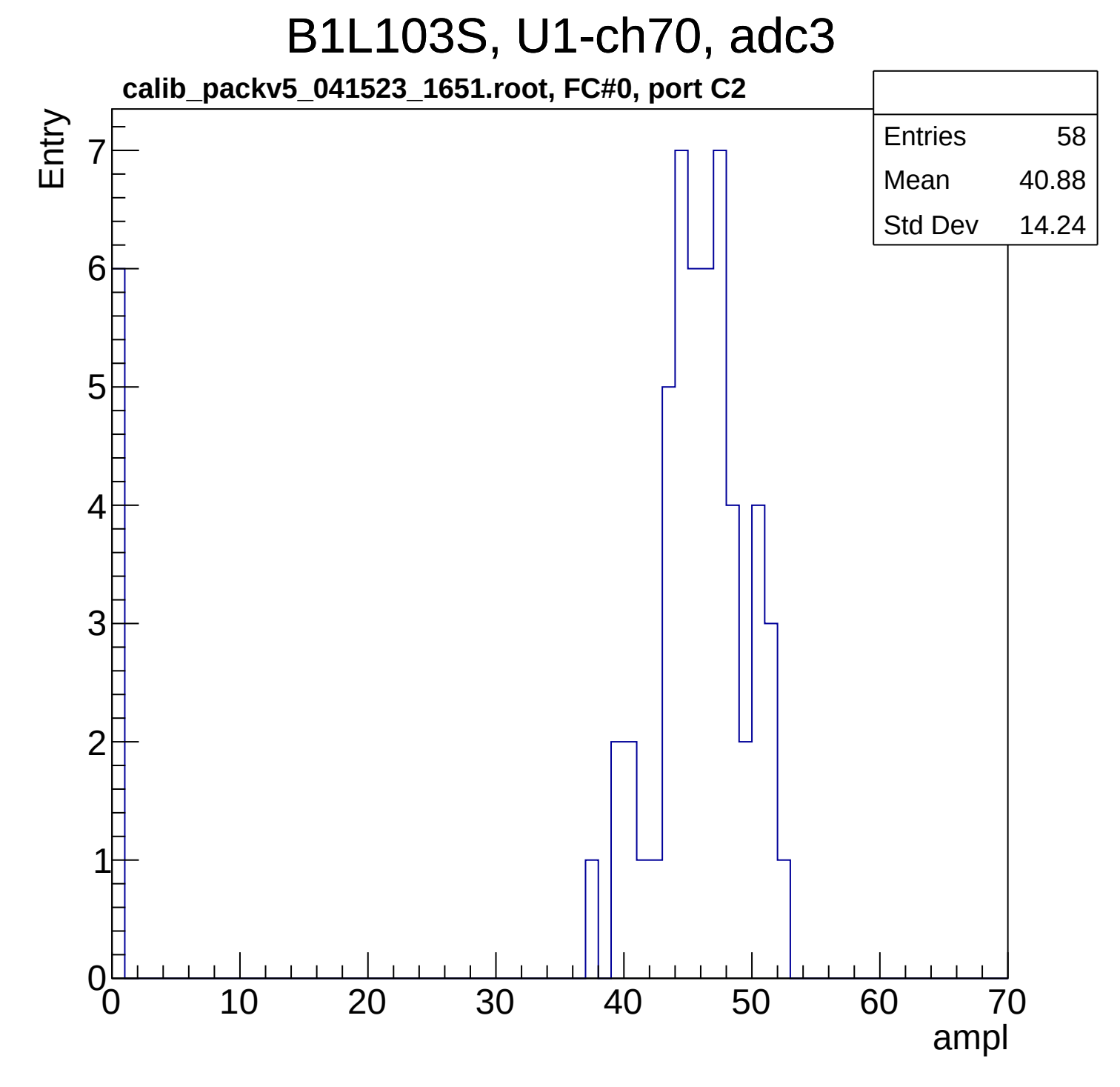

B1L103S, U1-ch70, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 34.53
Std Dev 13.43
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U1-ch70, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 40.88
Std Dev 14.24
Entry
ampl
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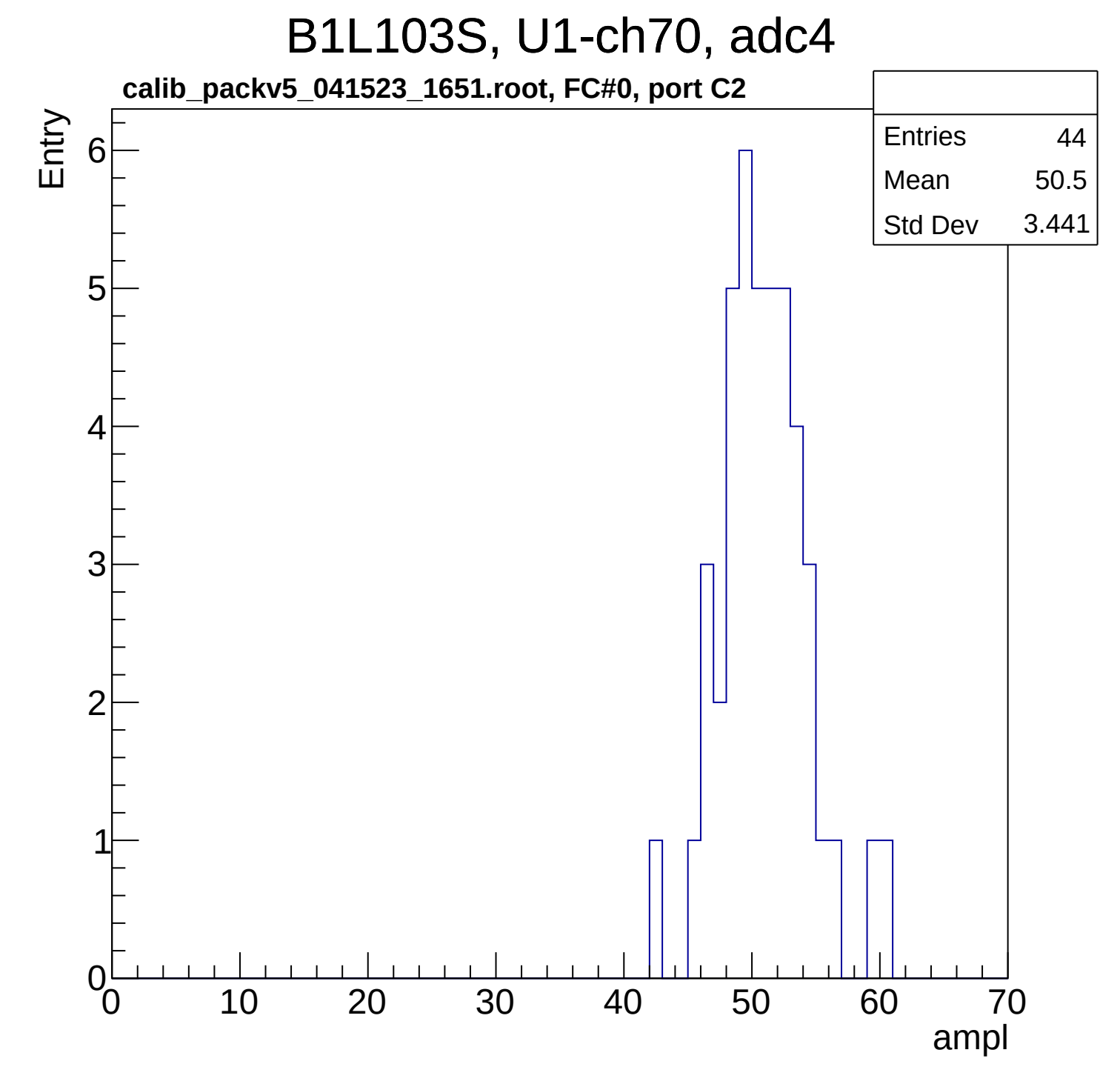
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U1-ch70, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 50.5
Std Dev 3.441
Entry
ampl
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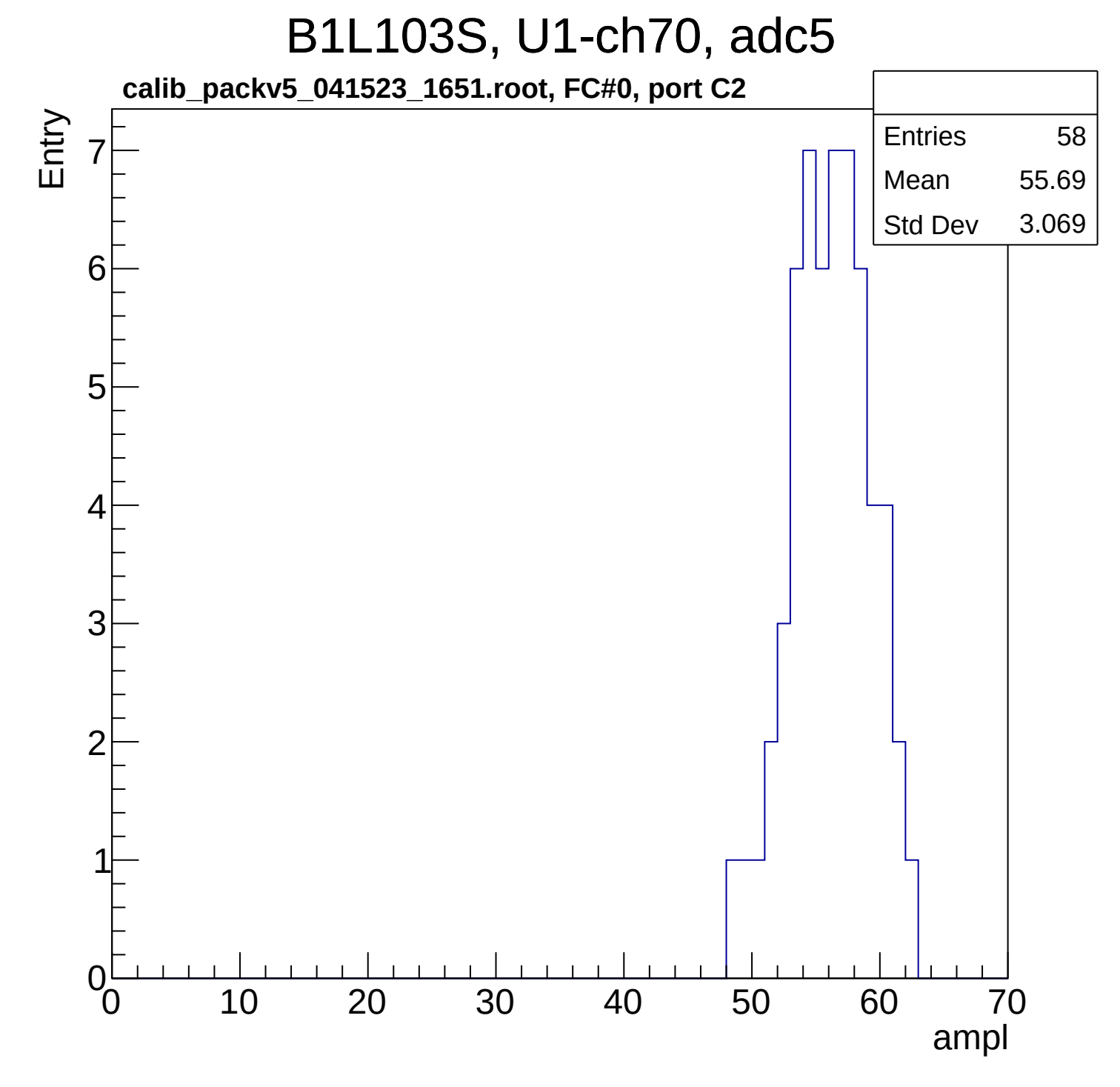
60
70


B1L103S, U1-ch70, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 55.69
Std Dev 3.069
Entry
ampl
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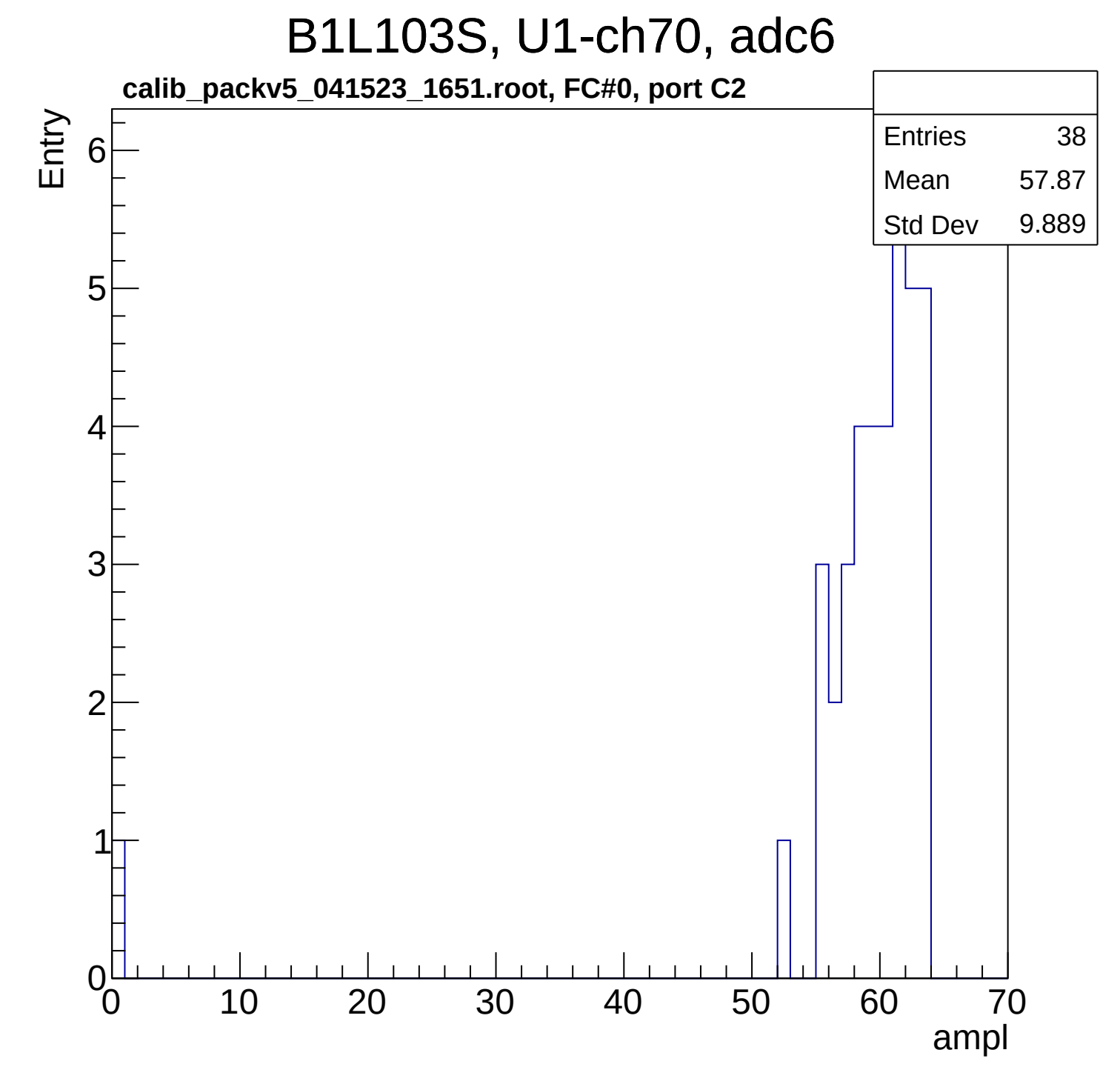
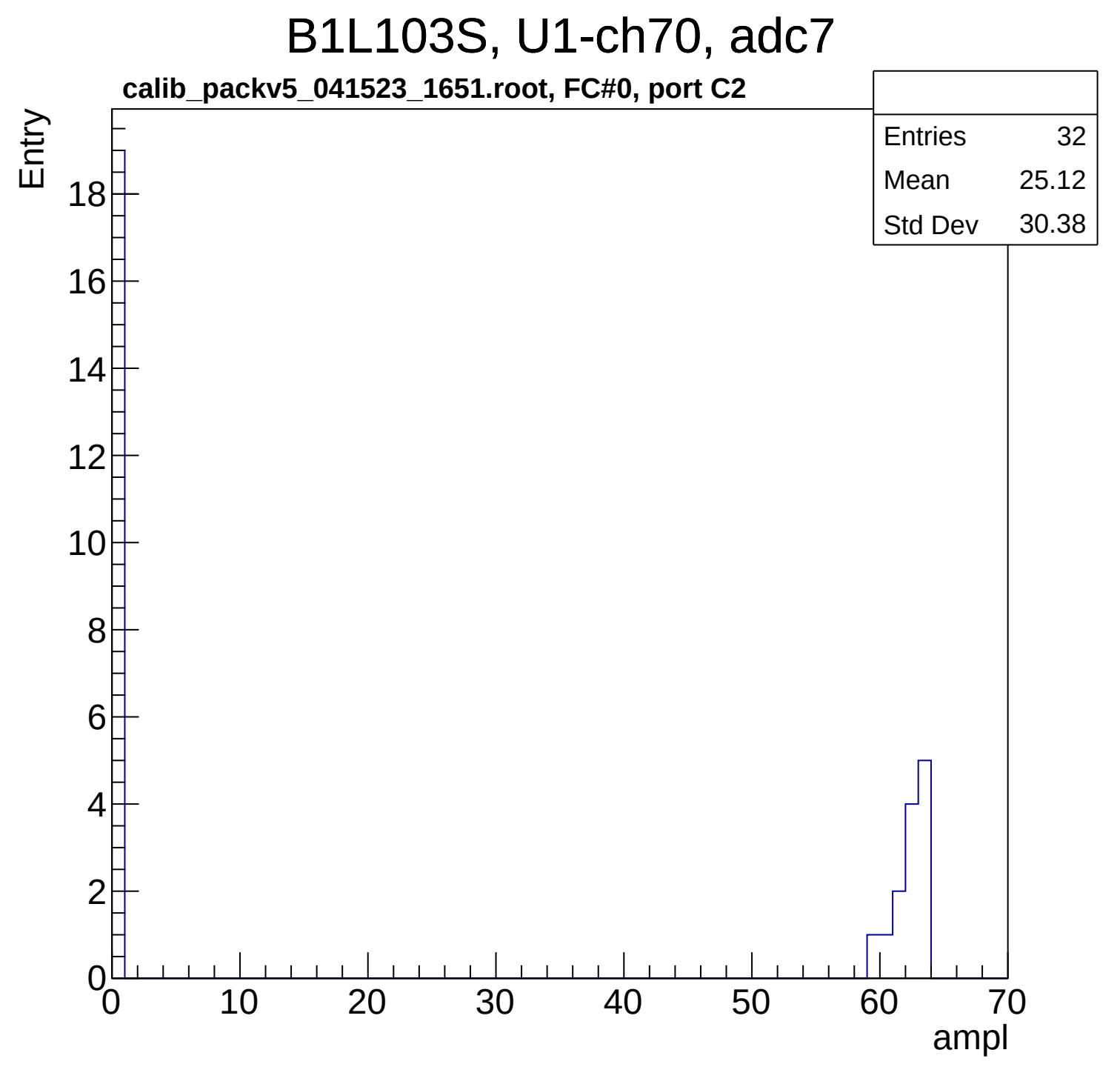
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U1-ch70, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 38
Mean 57.87
Std Dev 9.889
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U1-ch70, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 32
Mean 25.12
Std Dev 30.38
Entry
0
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6
8
10
12
14
16
18
0
10
20
30
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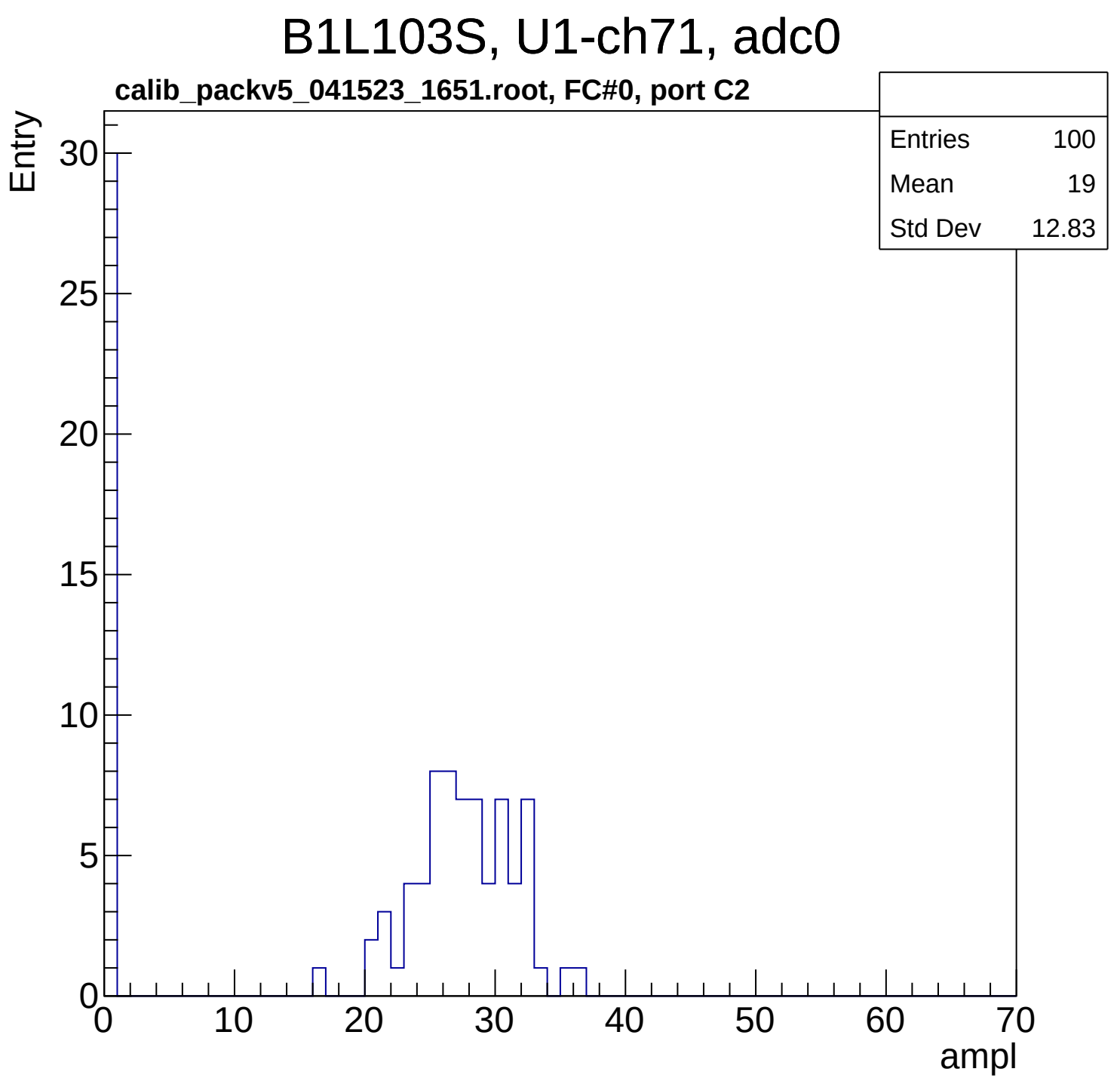
50
60
70
ampl


B1L103S, U1-ch71, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 100
Mean 19
Std Dev 12.83
Entry
ampl
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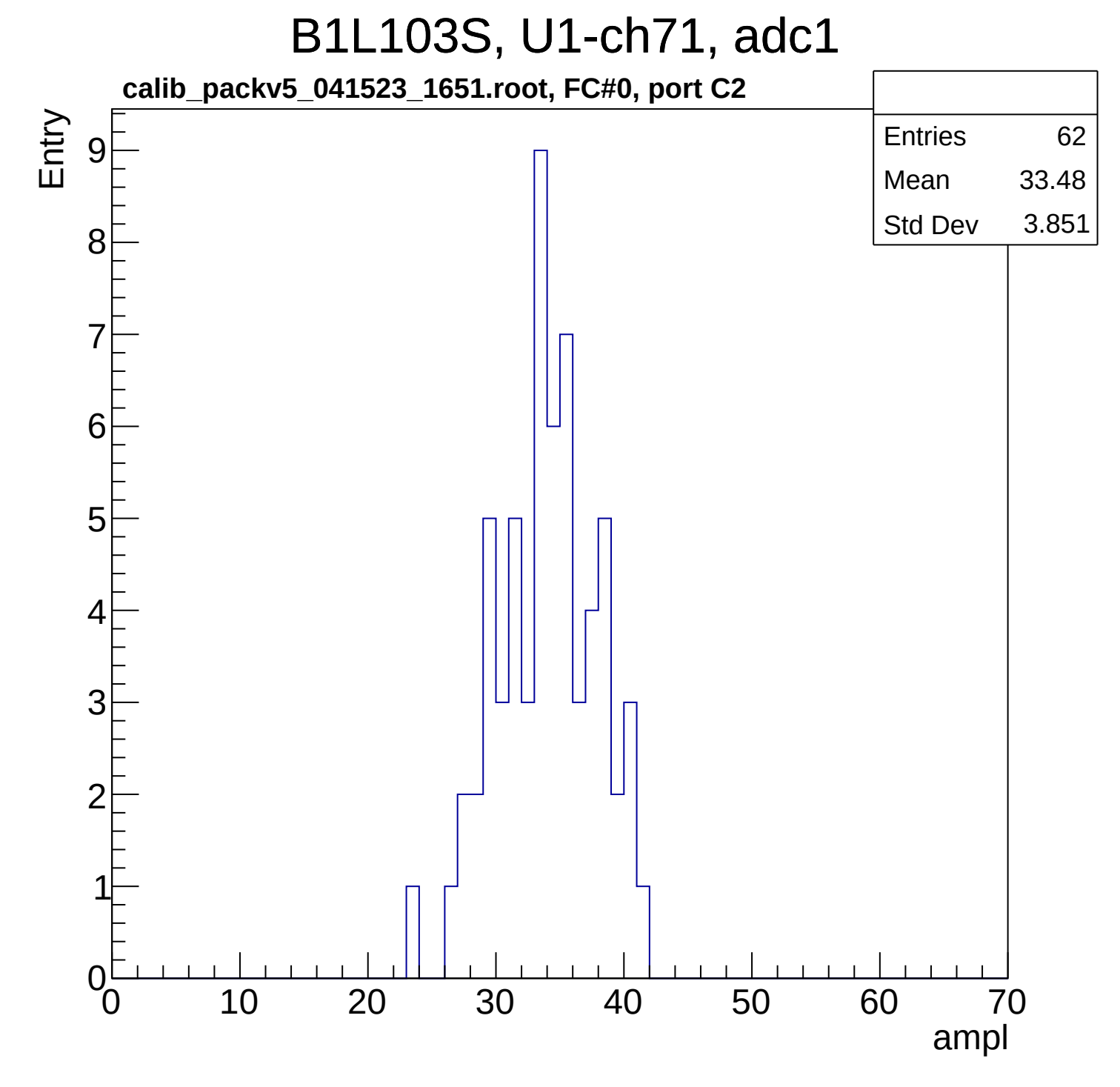
5
10
15
20
25
30
0
10
20
30
40
50
60
70


B1L103S, U1-ch71, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 33.48
Std Dev 3.851
Entry
ampl
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2
3
4
5
6
7
8
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0
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60
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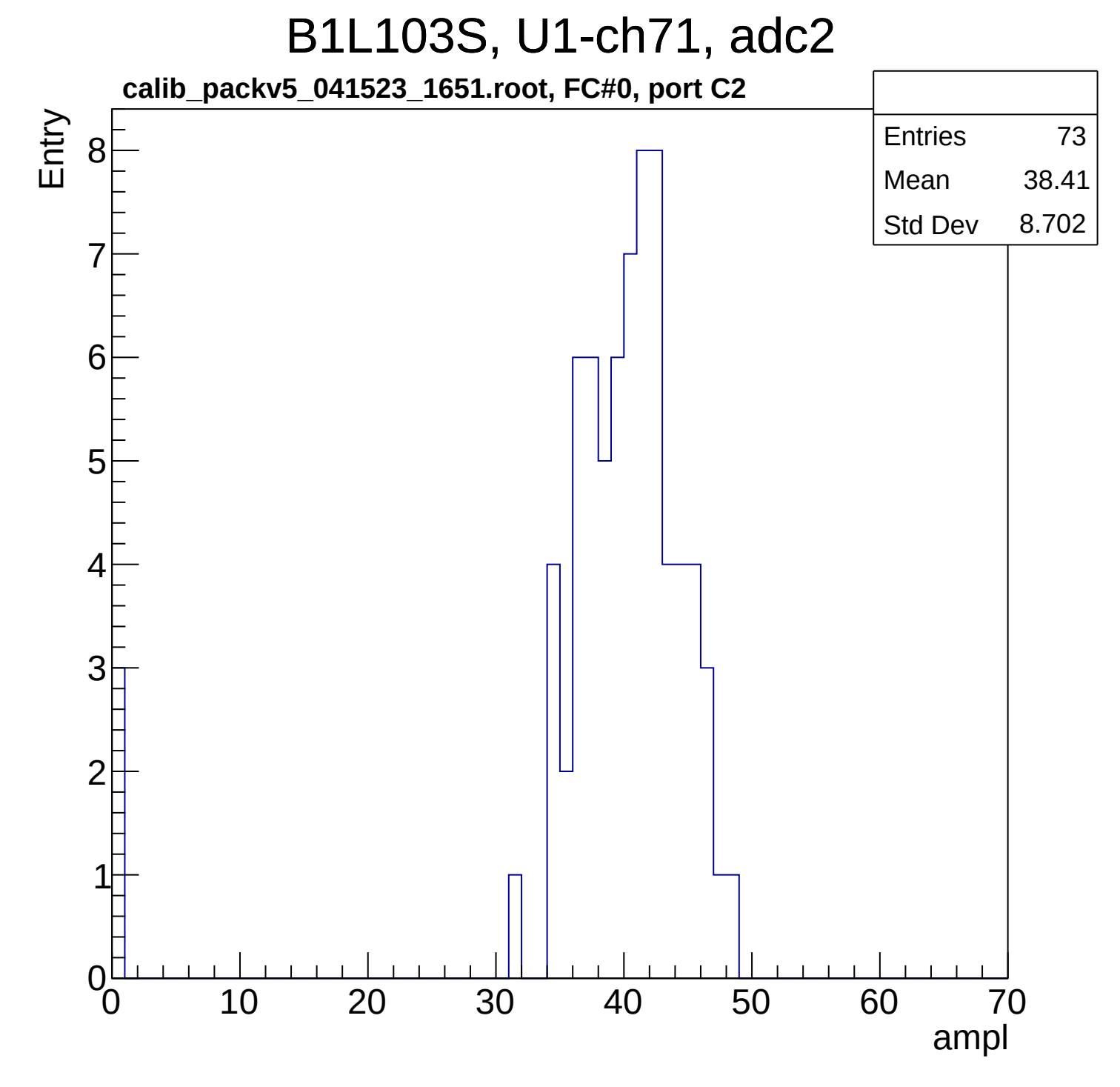
B1L103S, U1-ch71, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 38.41
Std Dev 8.702
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
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60
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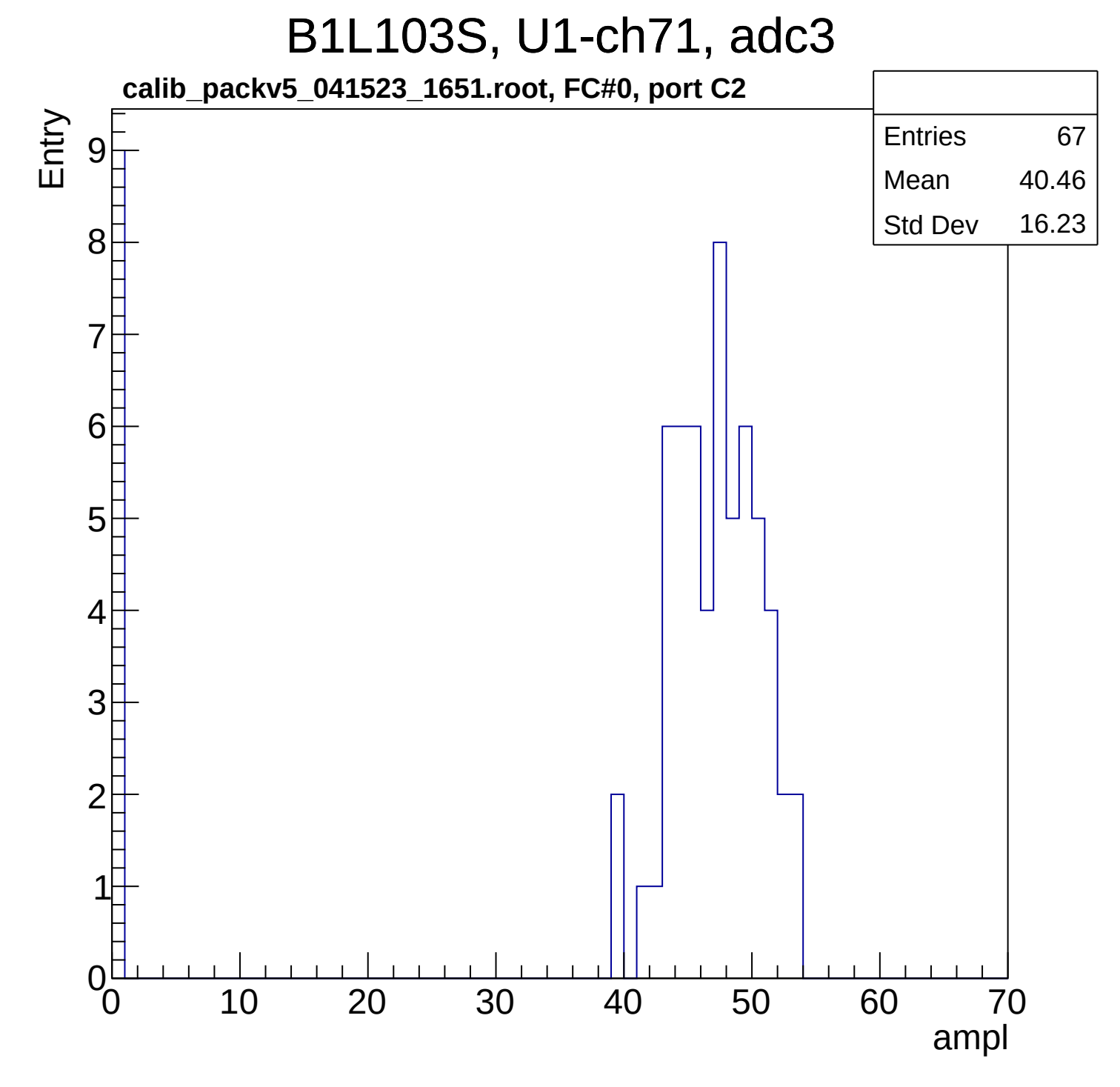
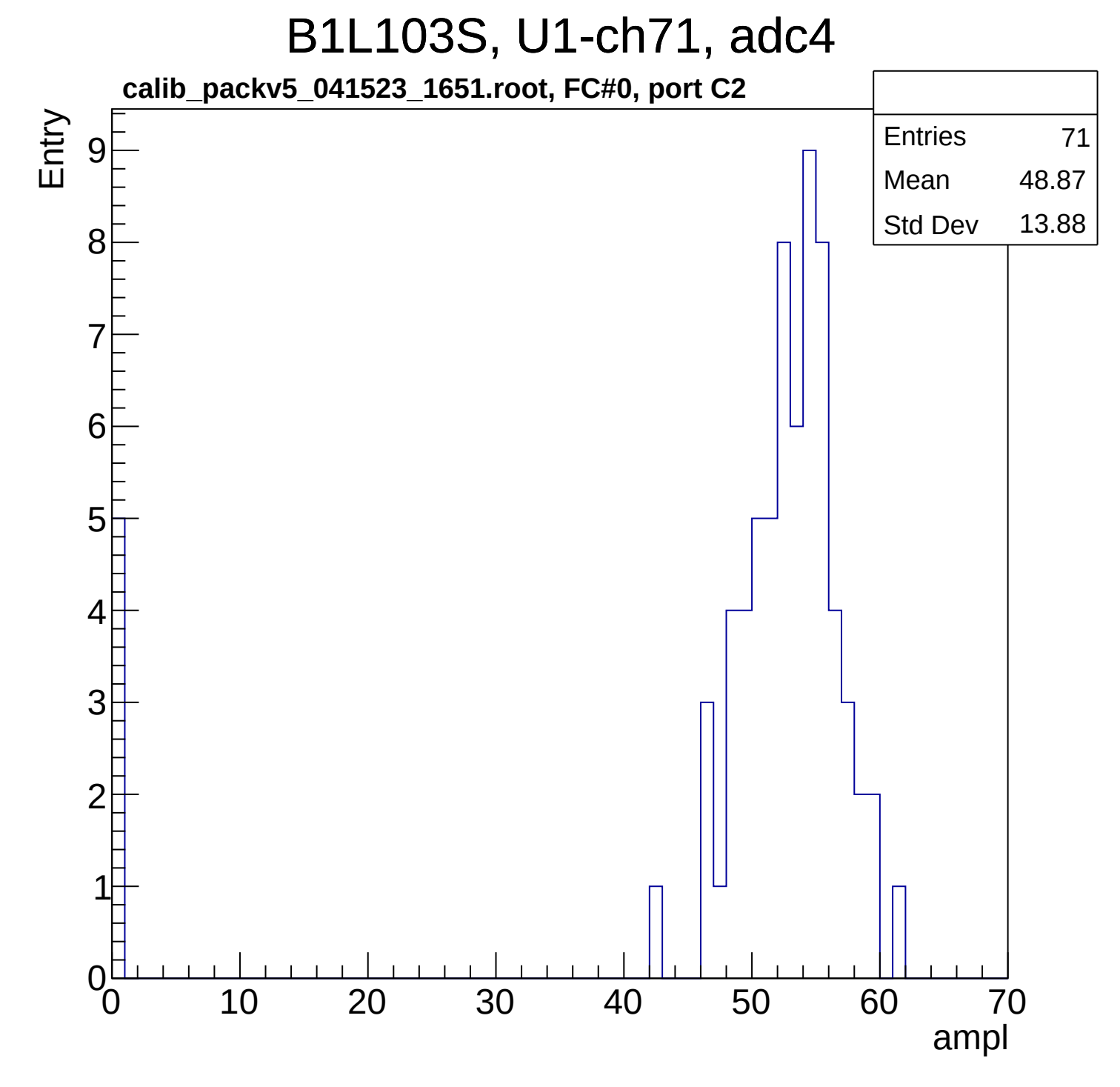

B1L103S, U1-ch71, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 40.46
Std Dev 16.23
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U1-ch71, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 48.87
Std Dev 13.88
Entry
ampl
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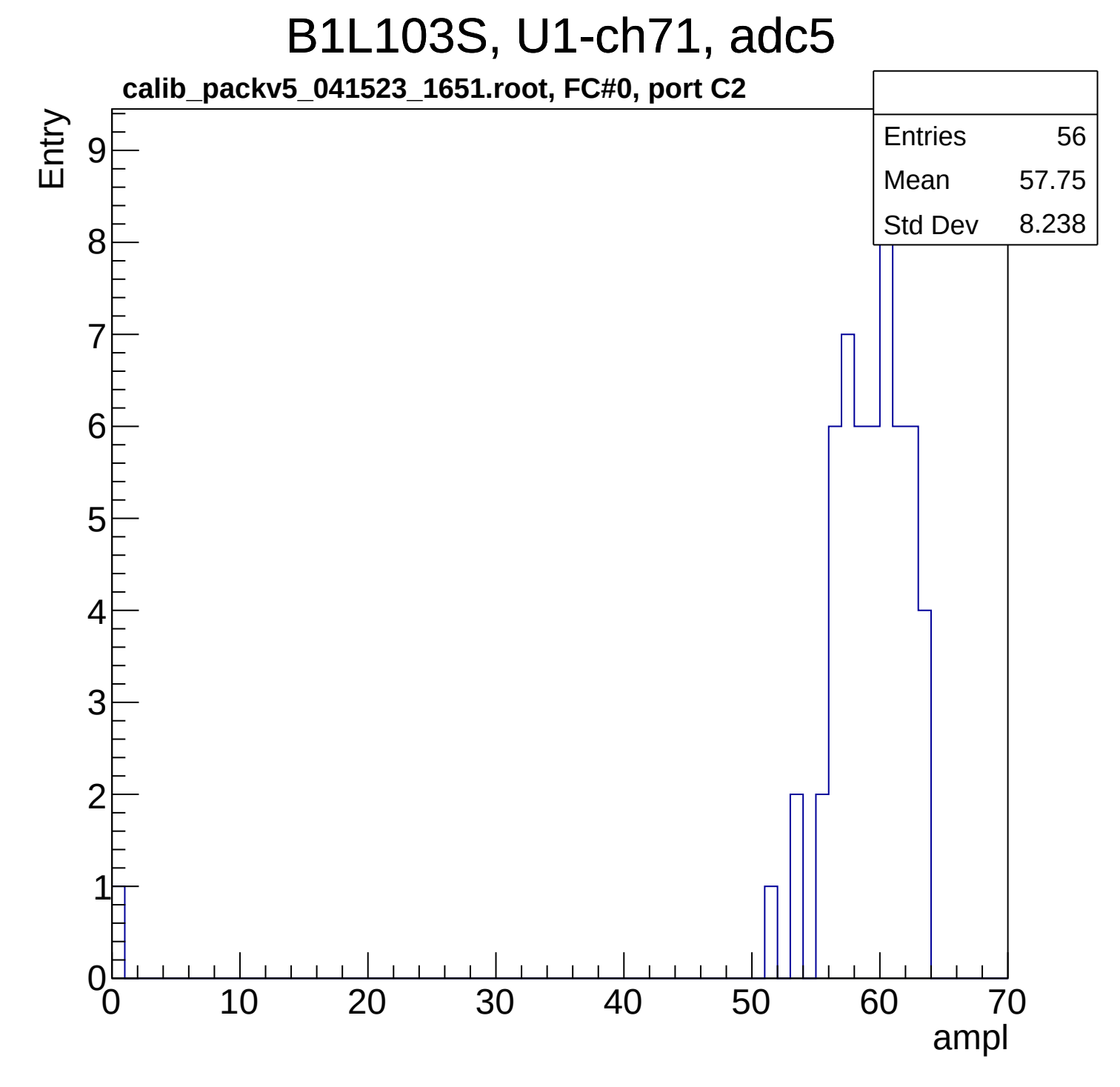
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U1-ch71, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 57.75
Std Dev 8.238
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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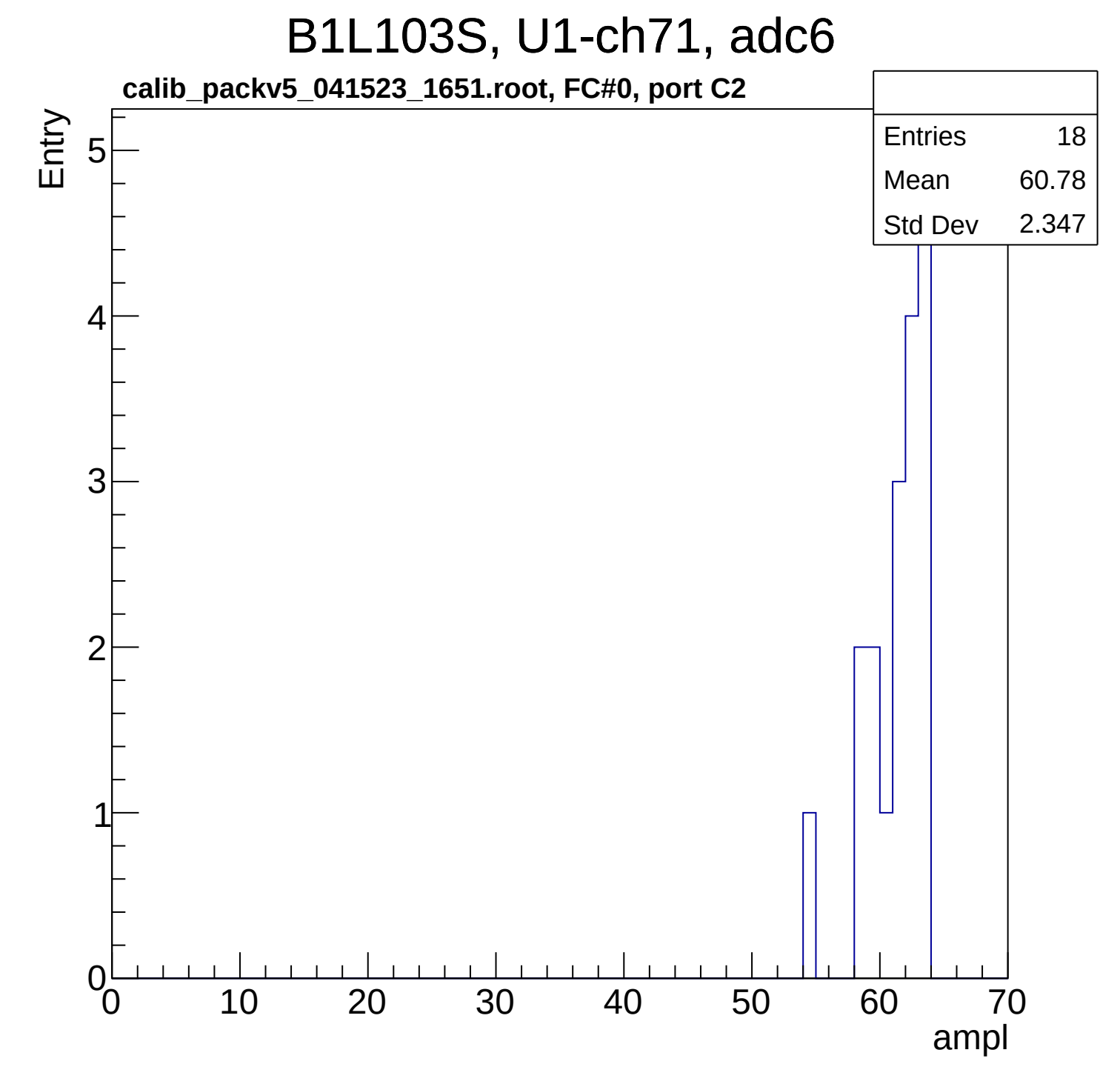
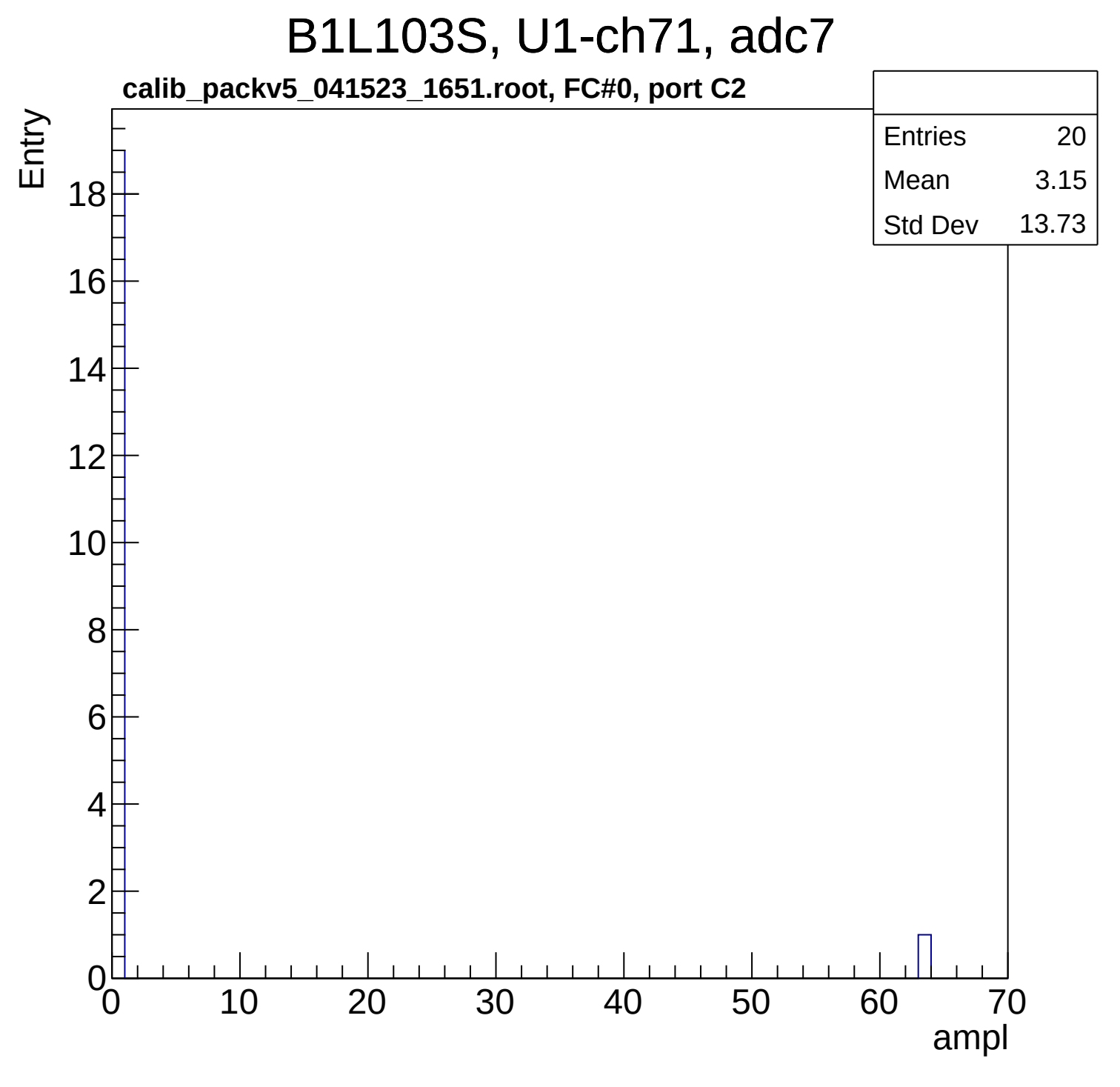
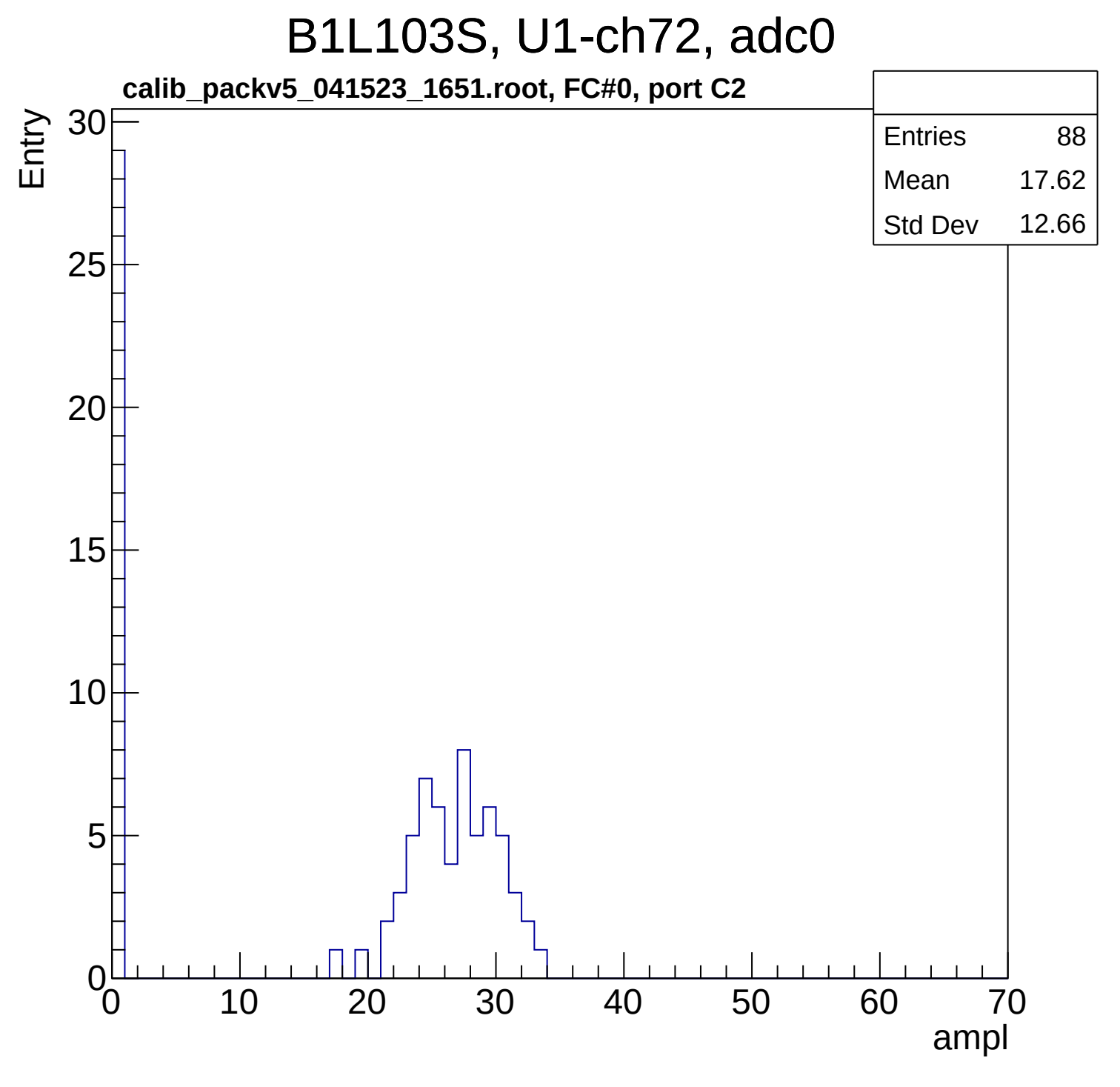
60
70


B1L103S, U1-ch71, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 60.78
Std Dev 2.347
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U1-ch71, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch72, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 88
Mean 17.62
Std Dev 12.66
Entry
ampl
0
5
10
15
20
25
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0
10
20
30
40
50
60
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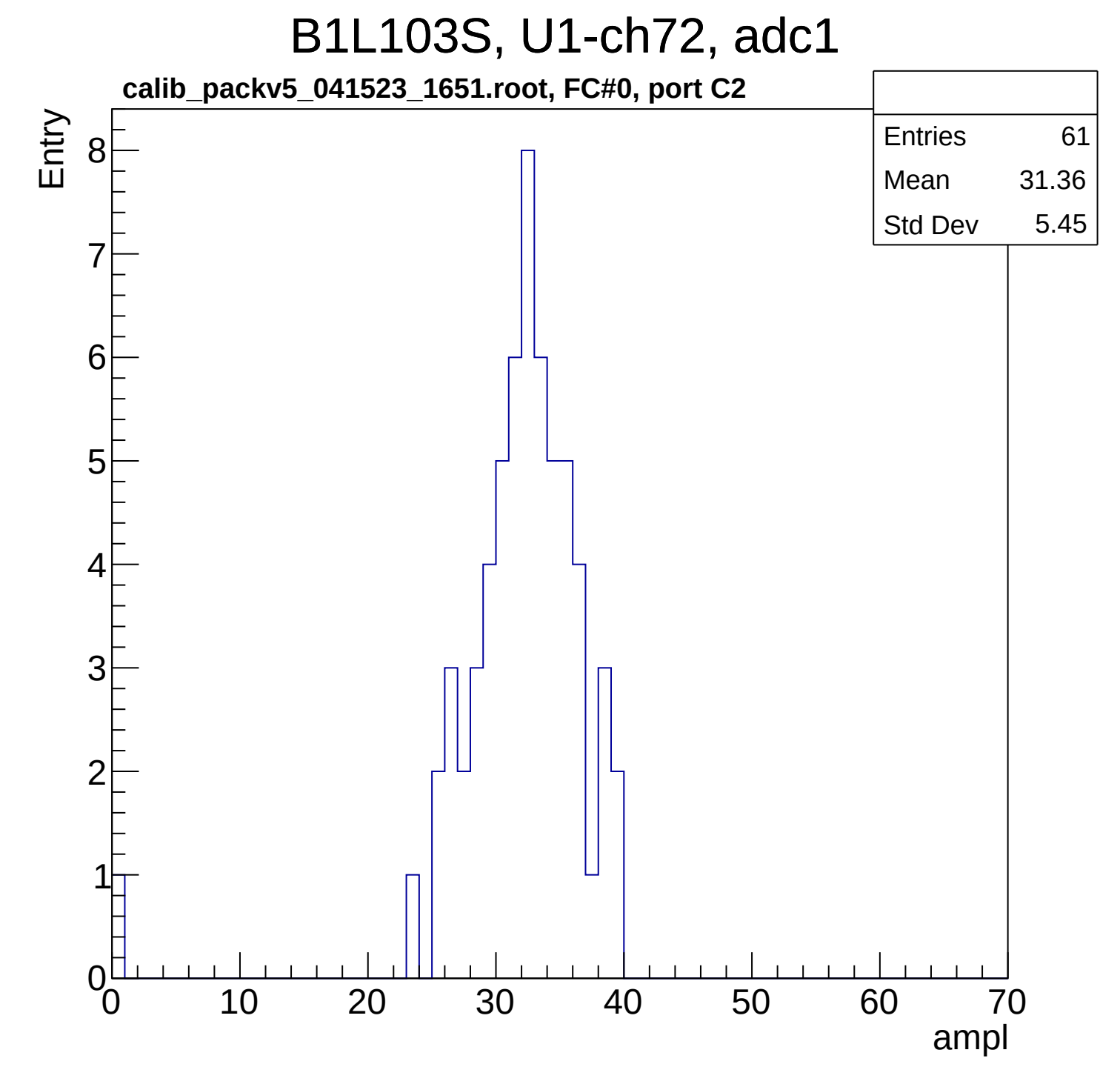
B1L103S, U1-ch72, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 31.36
Std Dev 5.45
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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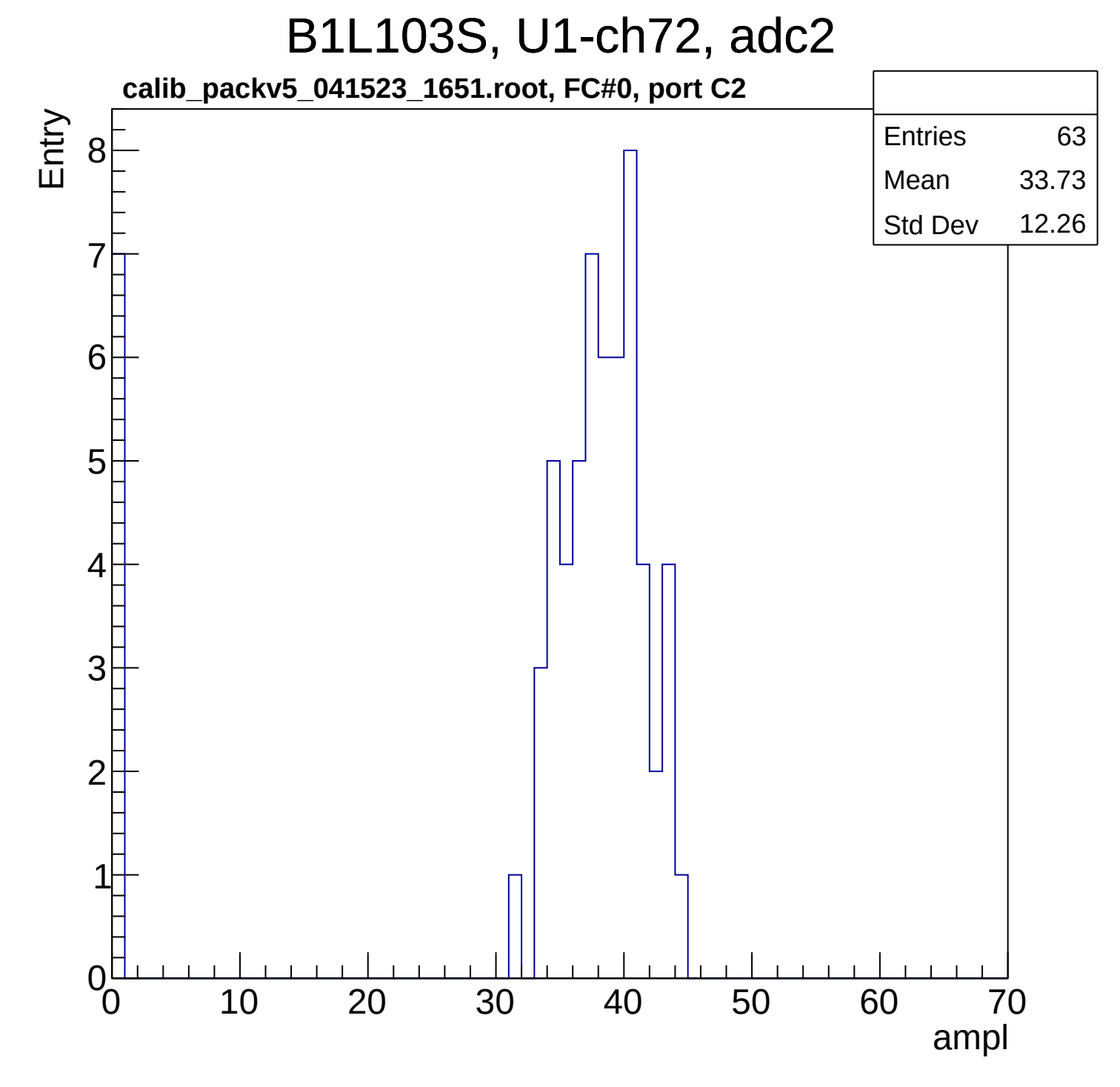
B1L103S, U1-ch72, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 33.73
Std Dev 12.26
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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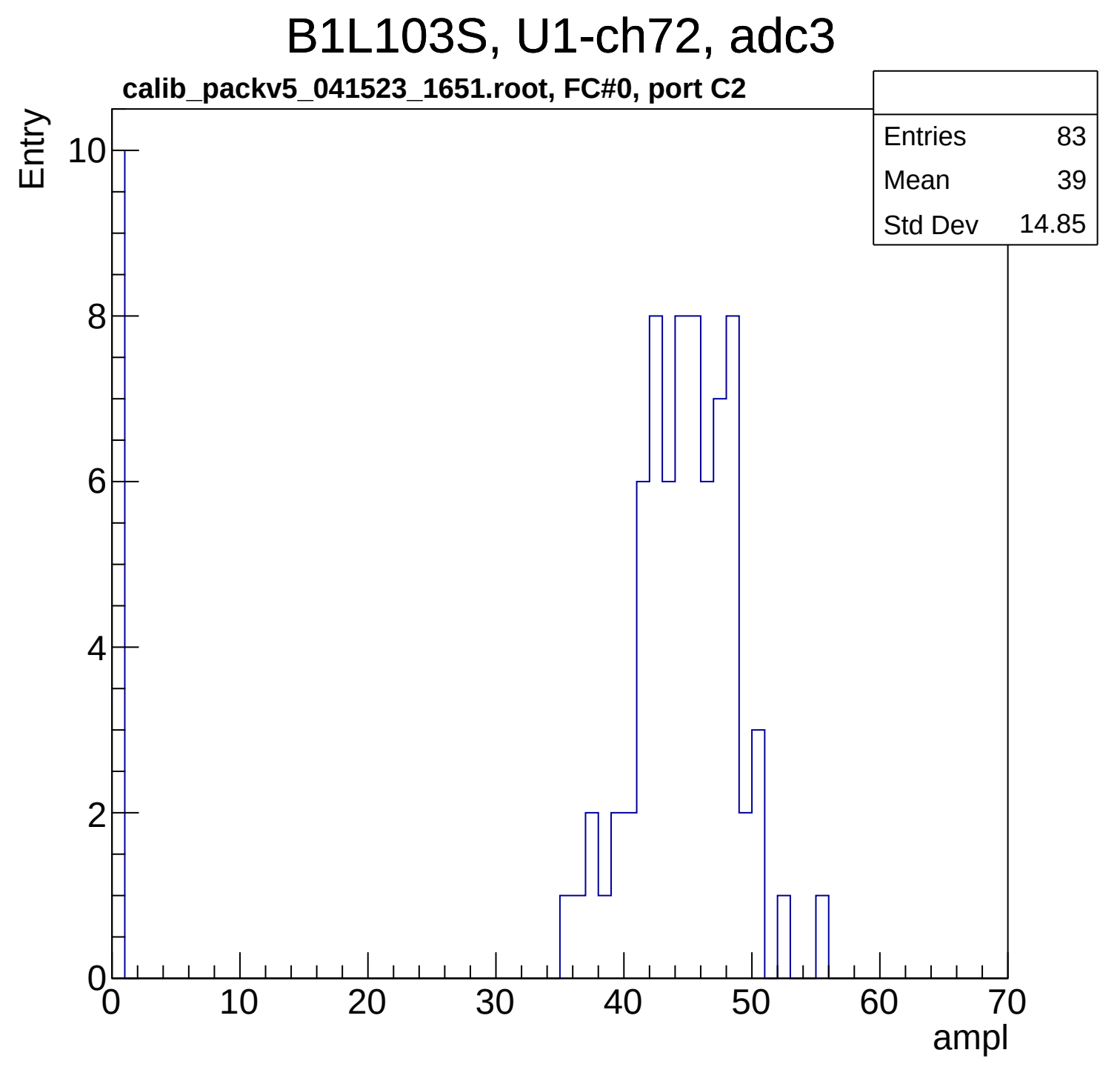
B1L103S, U1-ch72, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 39
Std Dev 14.85
Entry
ampl
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2
4
6
8
10
0
10
20
30
40
50
60
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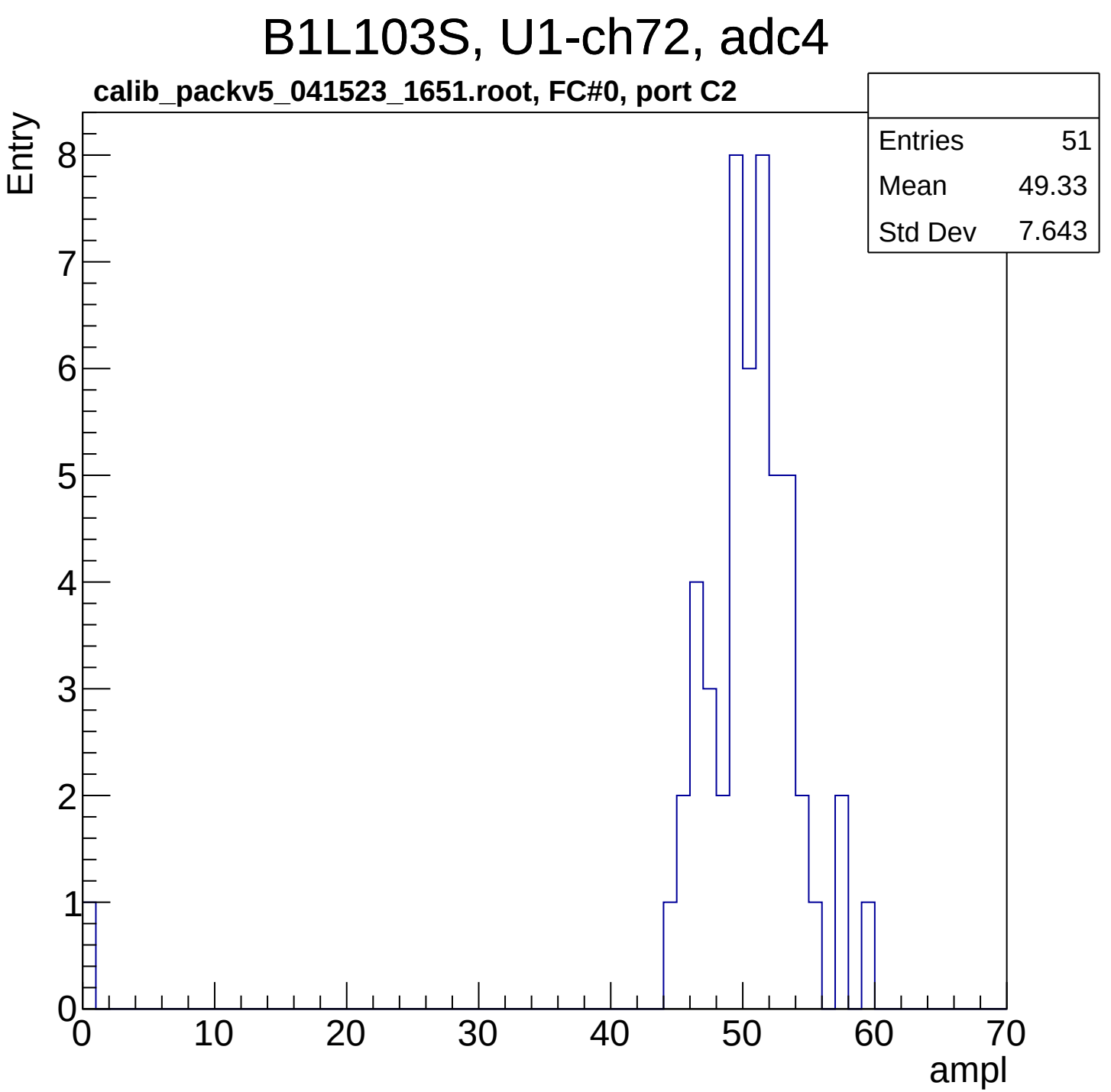
B1L103S, U1-ch72, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 49.33
Std Dev 7.643
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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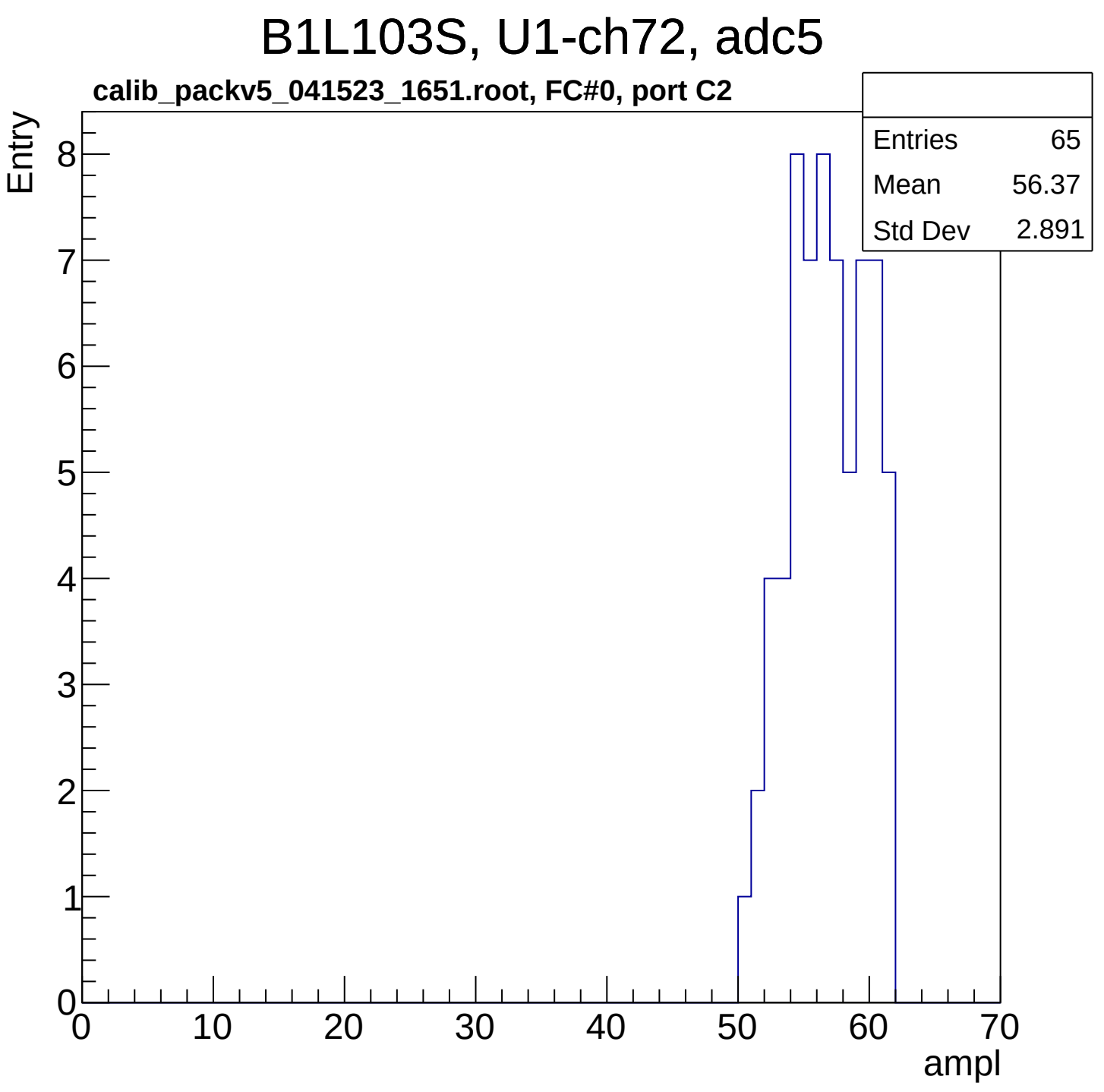
B1L103S, U1-ch72, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 56.37
Std Dev 2.891
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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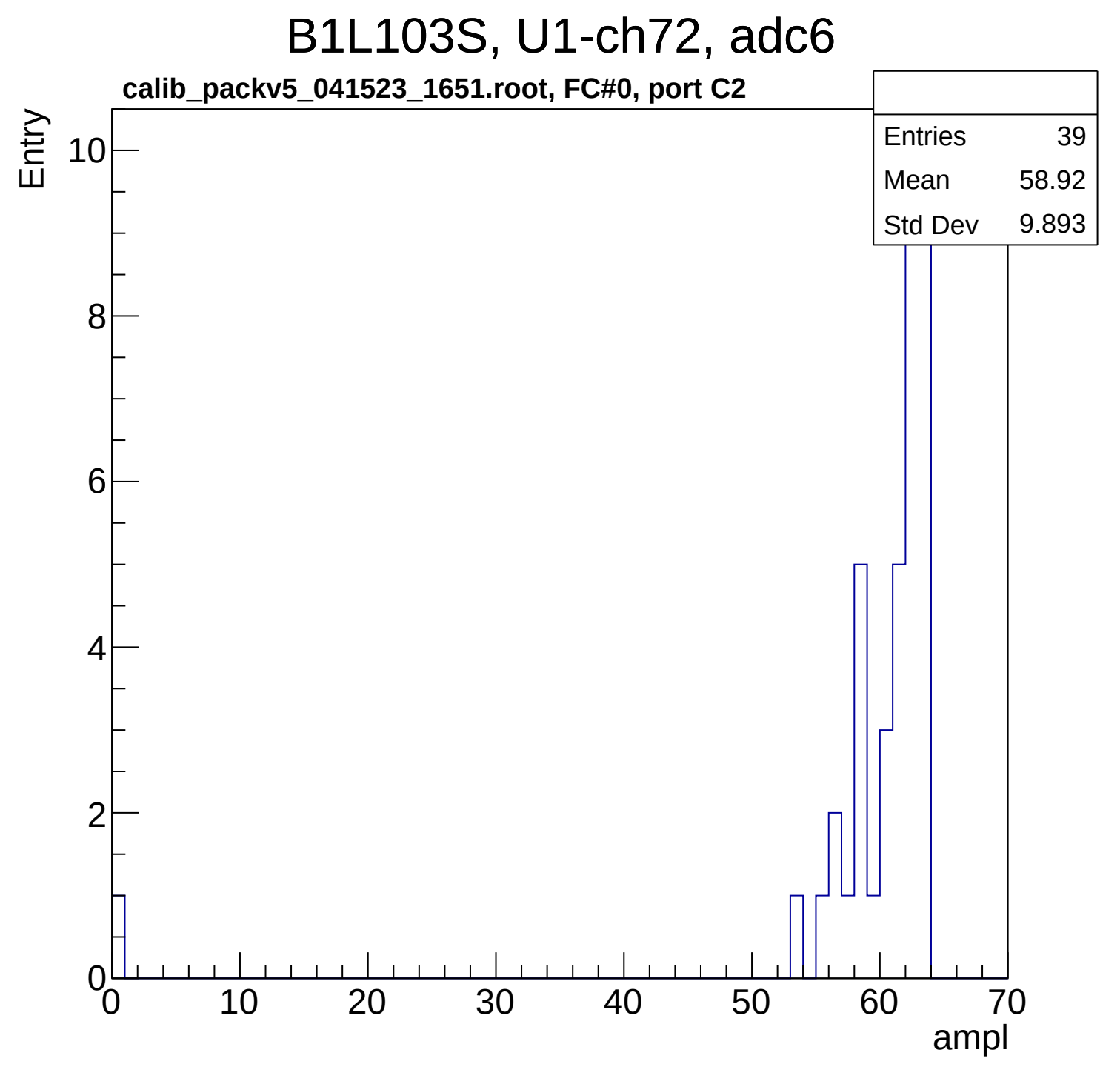
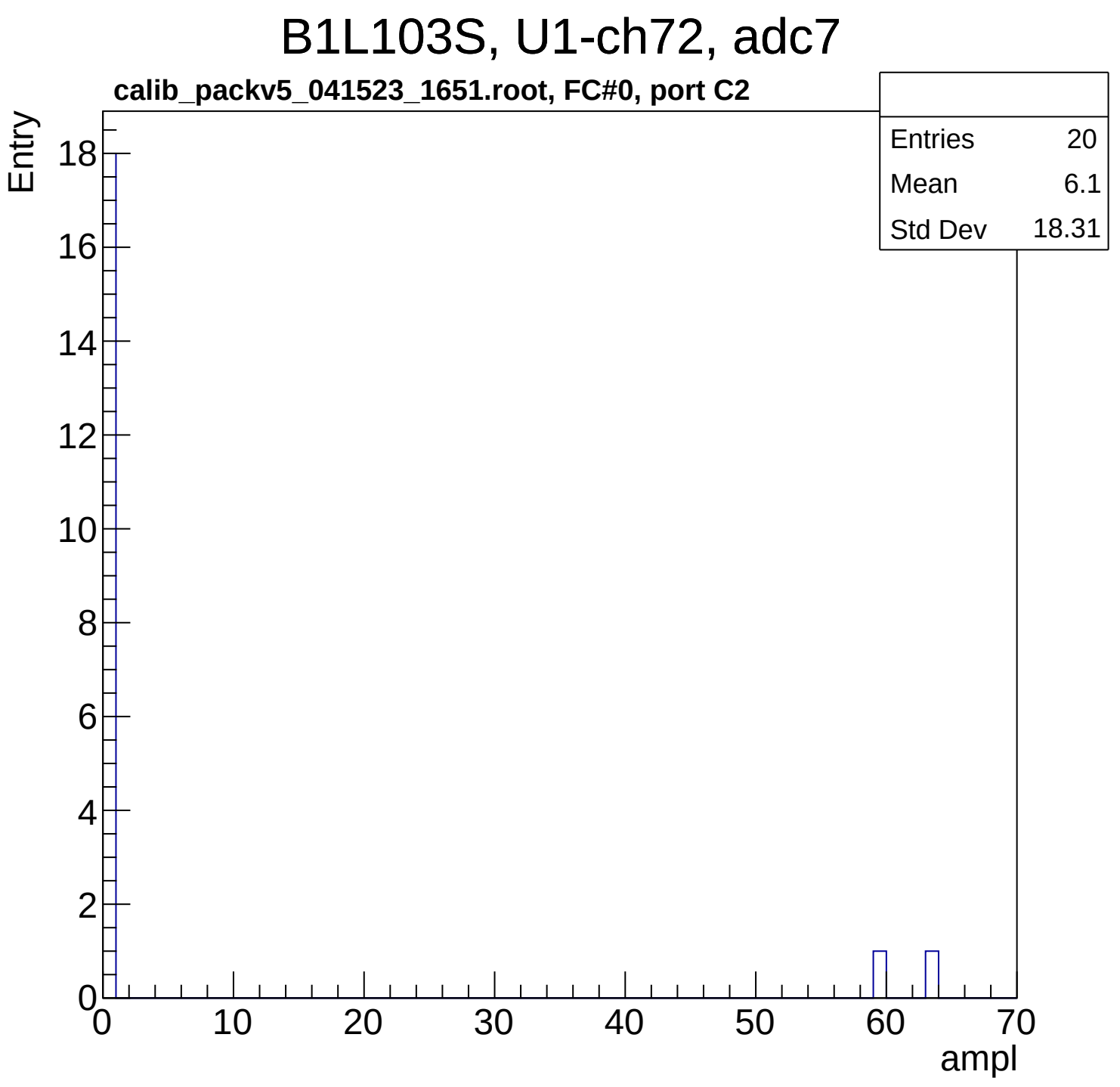

B1L103S, U1-ch72, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 39
Mean 58.92
Std Dev 9.893
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch72, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 6.1
Std Dev 18.31
Entry
0
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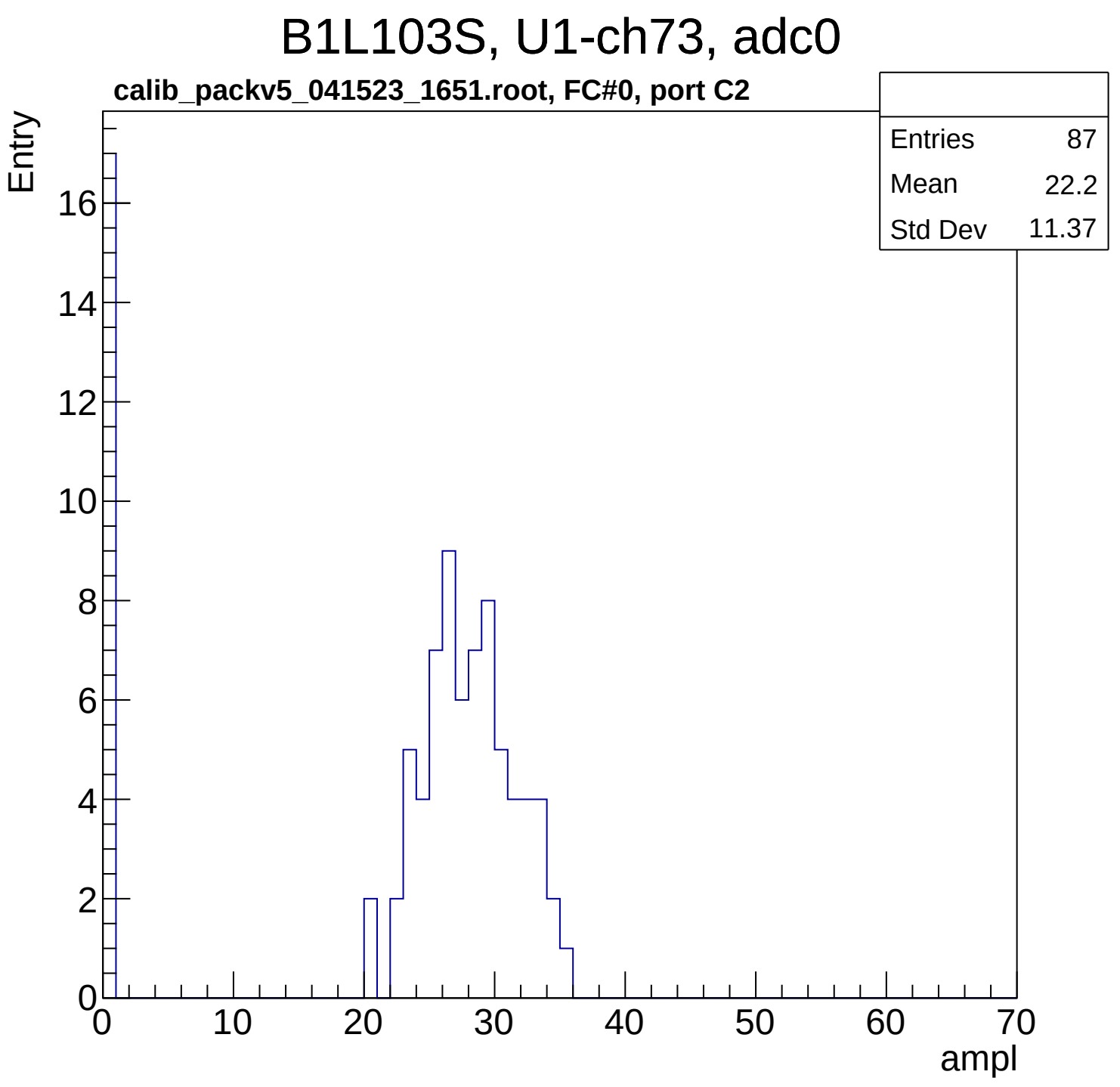
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch73, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 87
Mean 22.2
Std Dev 11.37
Entry
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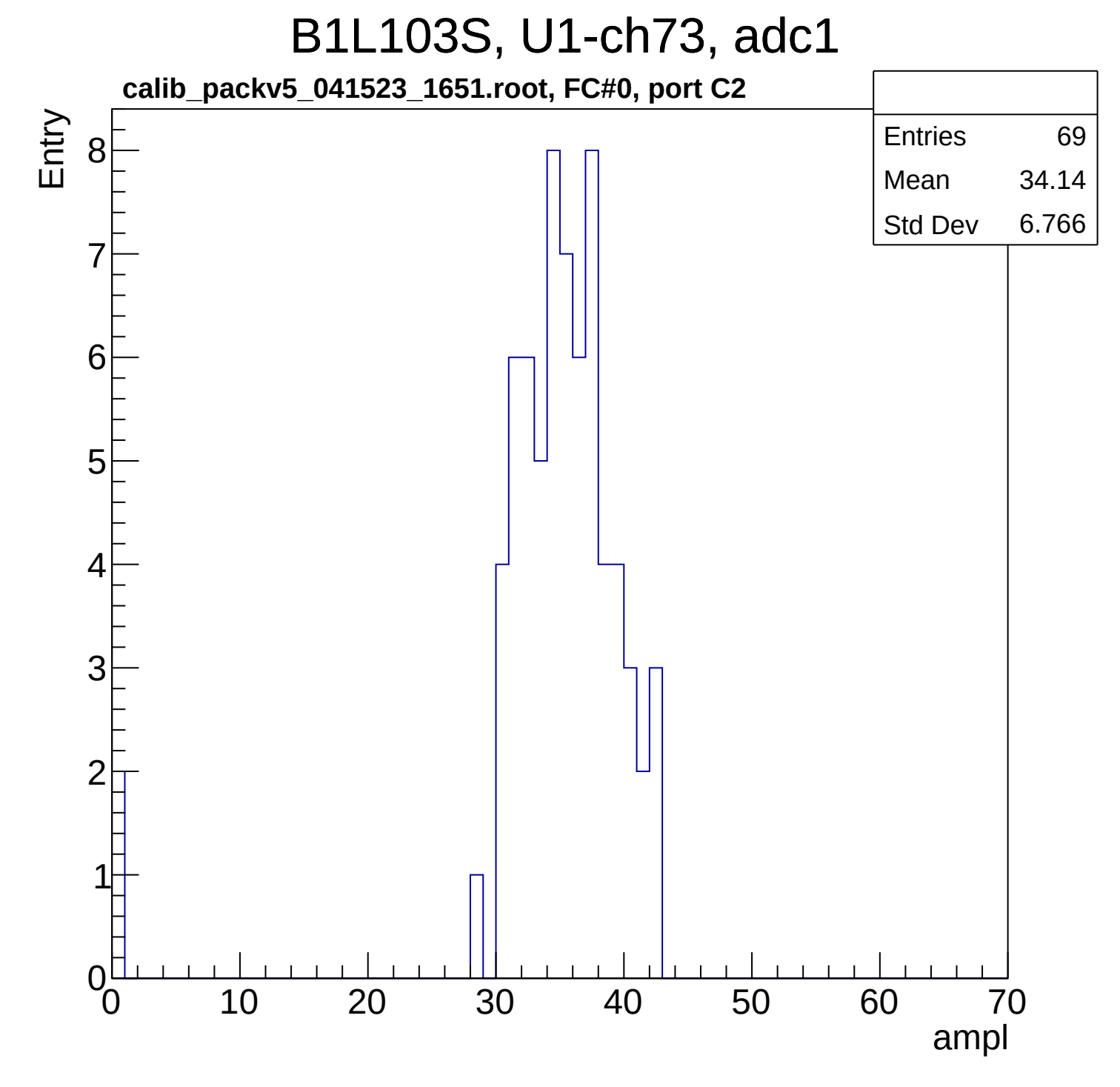
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch73, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 34.14
Std Dev 6.766
Entry
ampl
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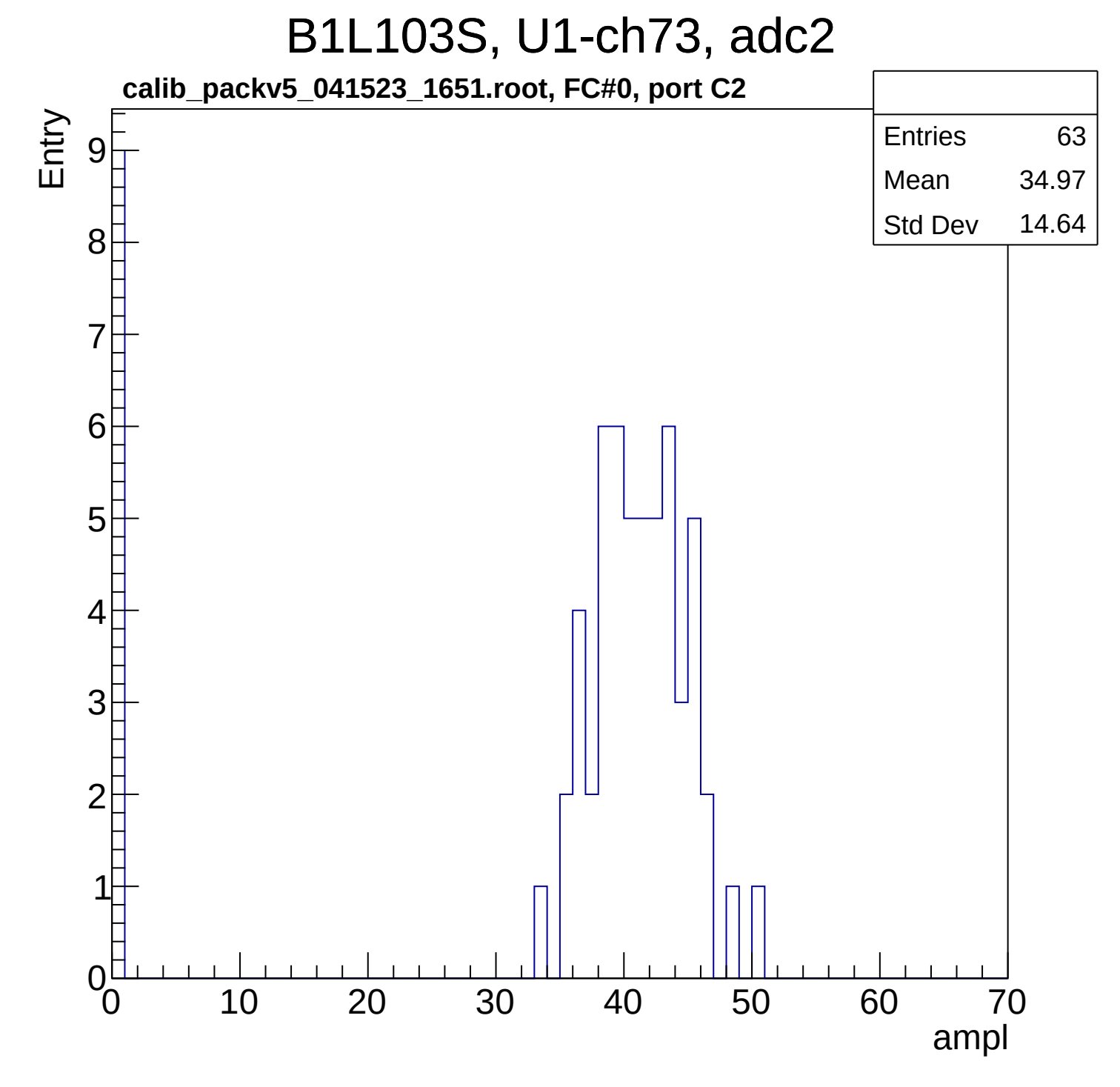
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U1-ch73, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 34.97
Std Dev 14.64
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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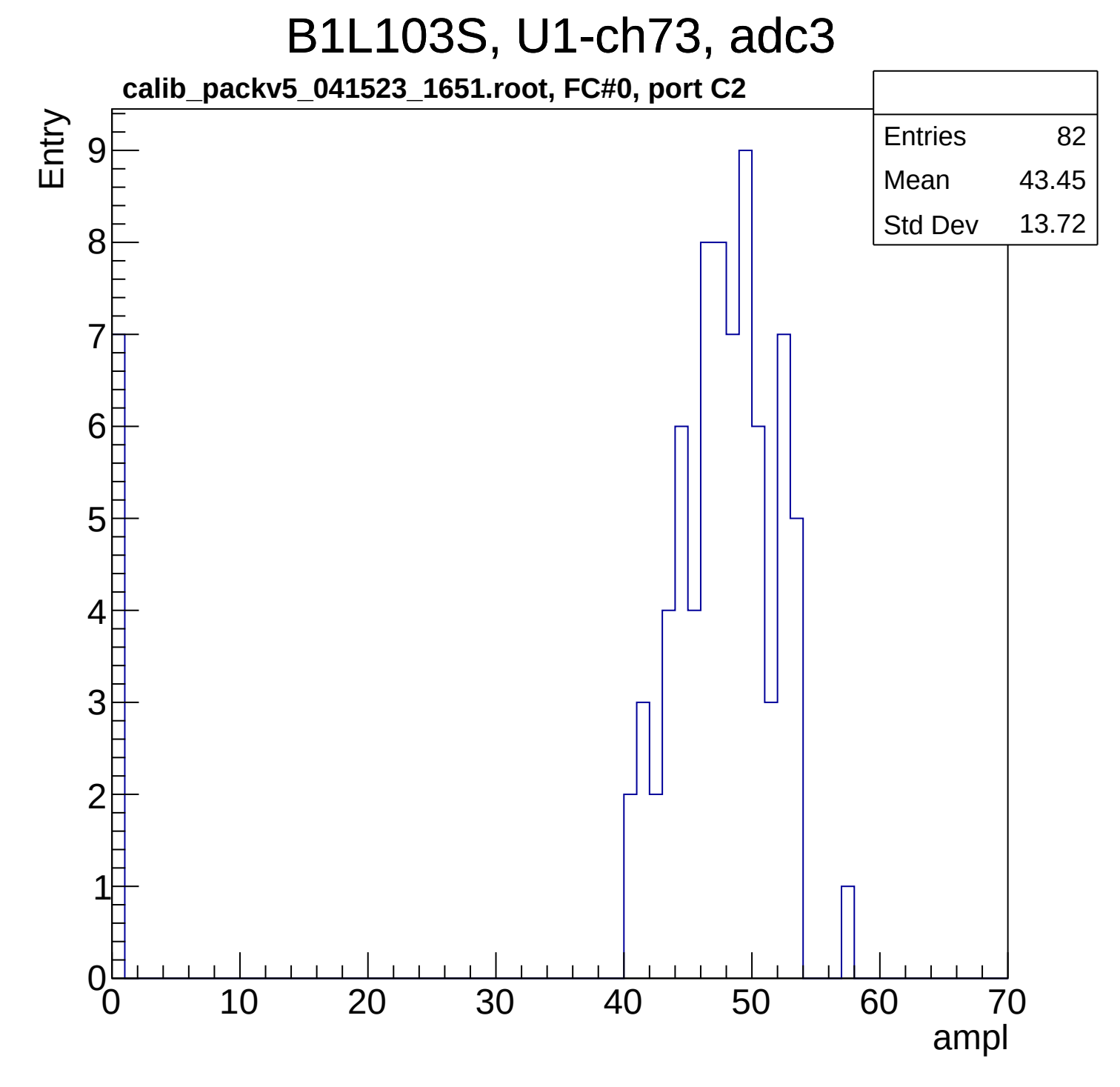
B1L103S, U1-ch73, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 43.45
Std Dev 13.72
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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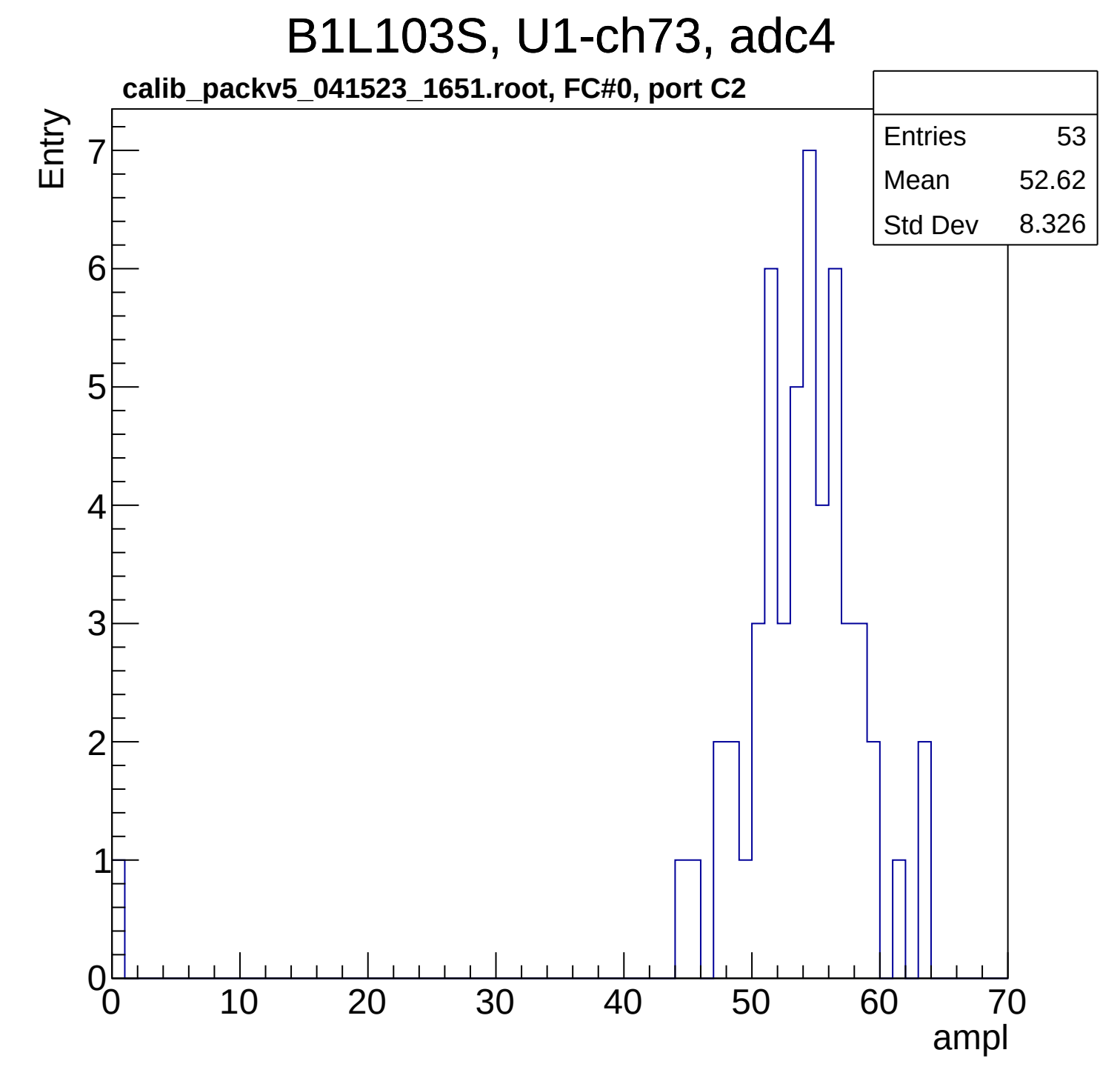
B1L103S, U1-ch73, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 52.62
Std Dev 8.326
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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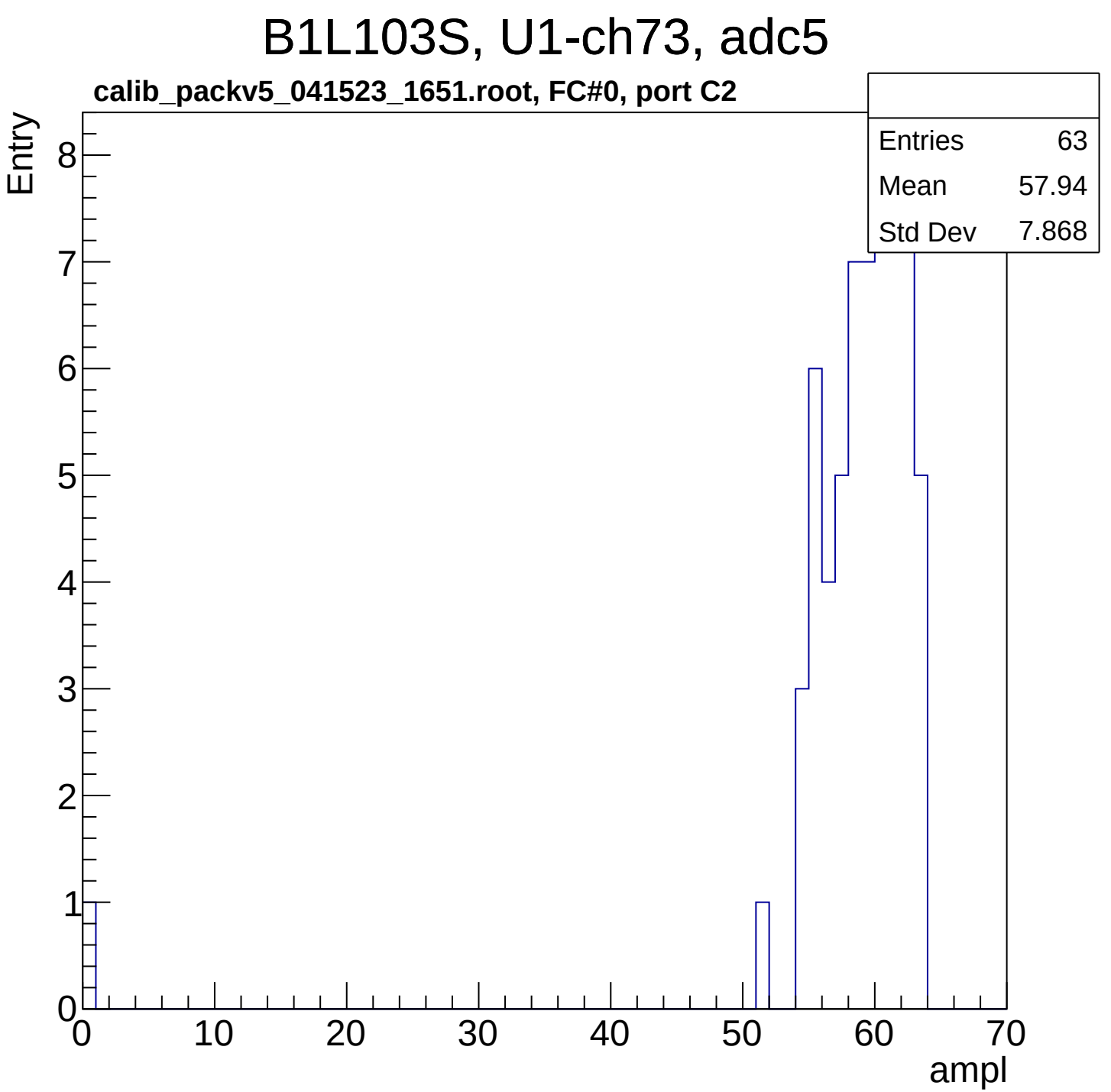
B1L103S, U1-ch73, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 57.94
Std Dev 7.868
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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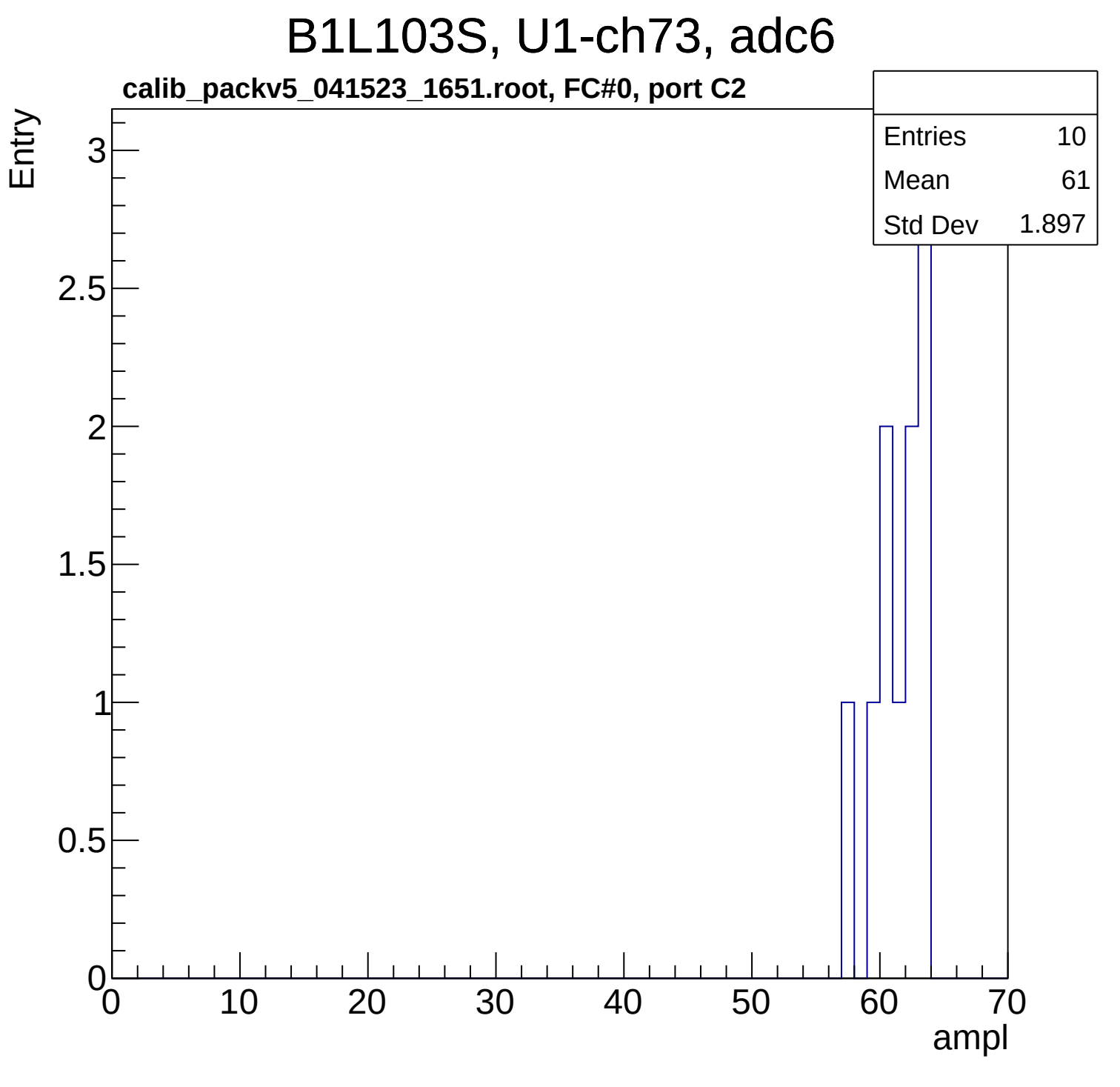
B1L103S, U1-ch73, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 61
Std Dev 1.897
Entry
ampl
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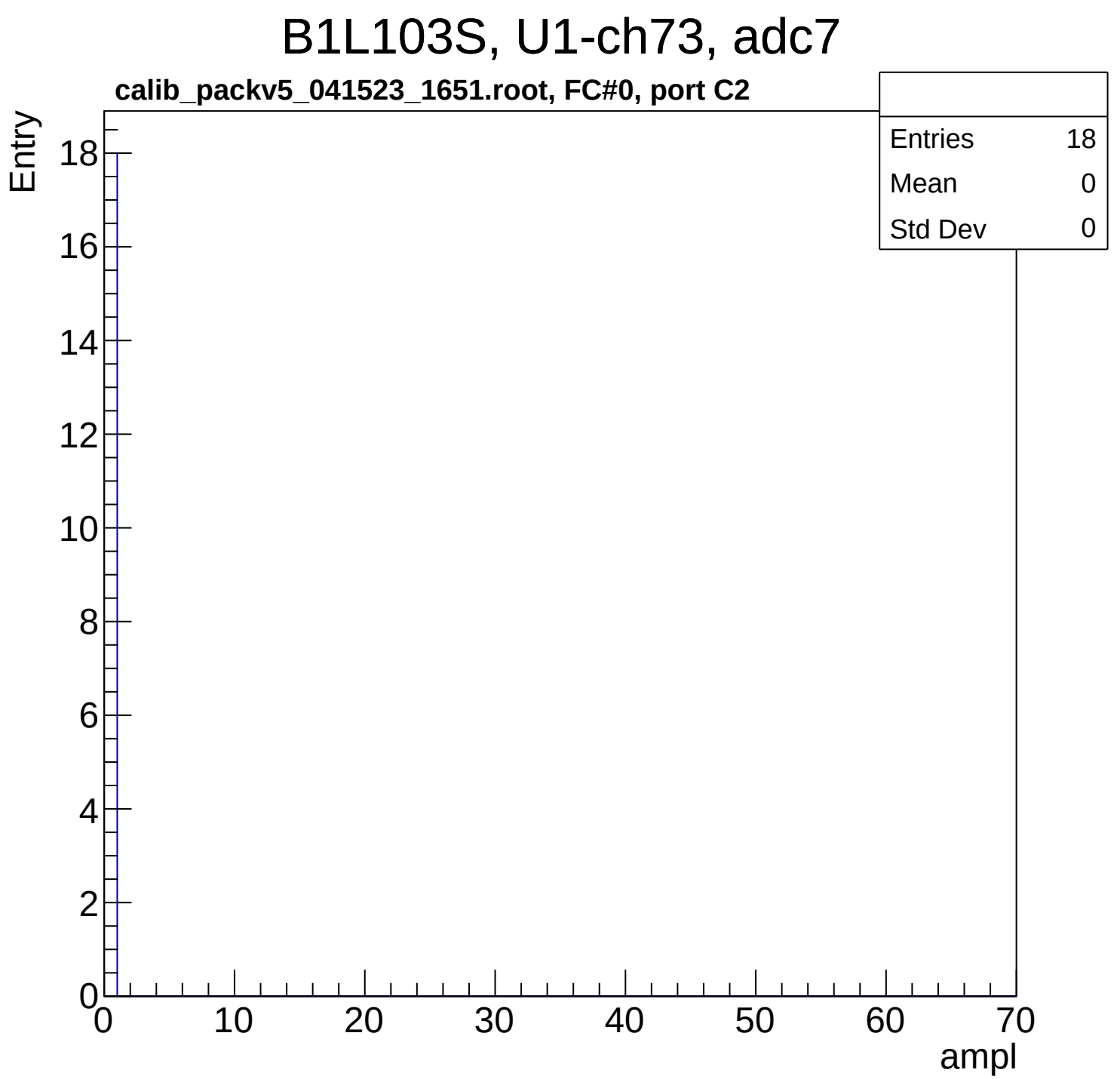
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U1-ch73, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
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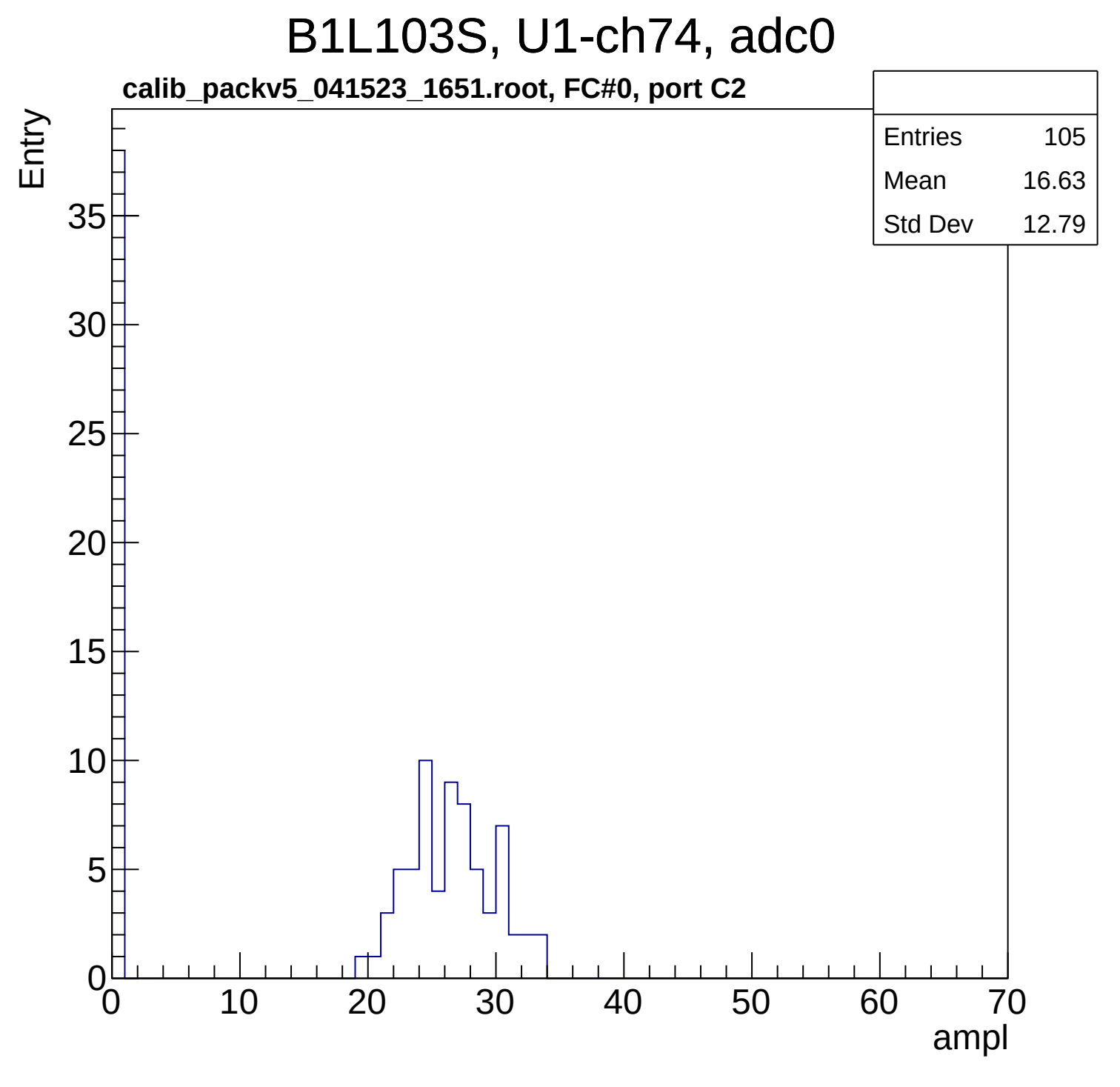
50
60
70
ampl


B1L103S, U1-ch74, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 105
Mean 16.63
Std Dev 12.79
Entry
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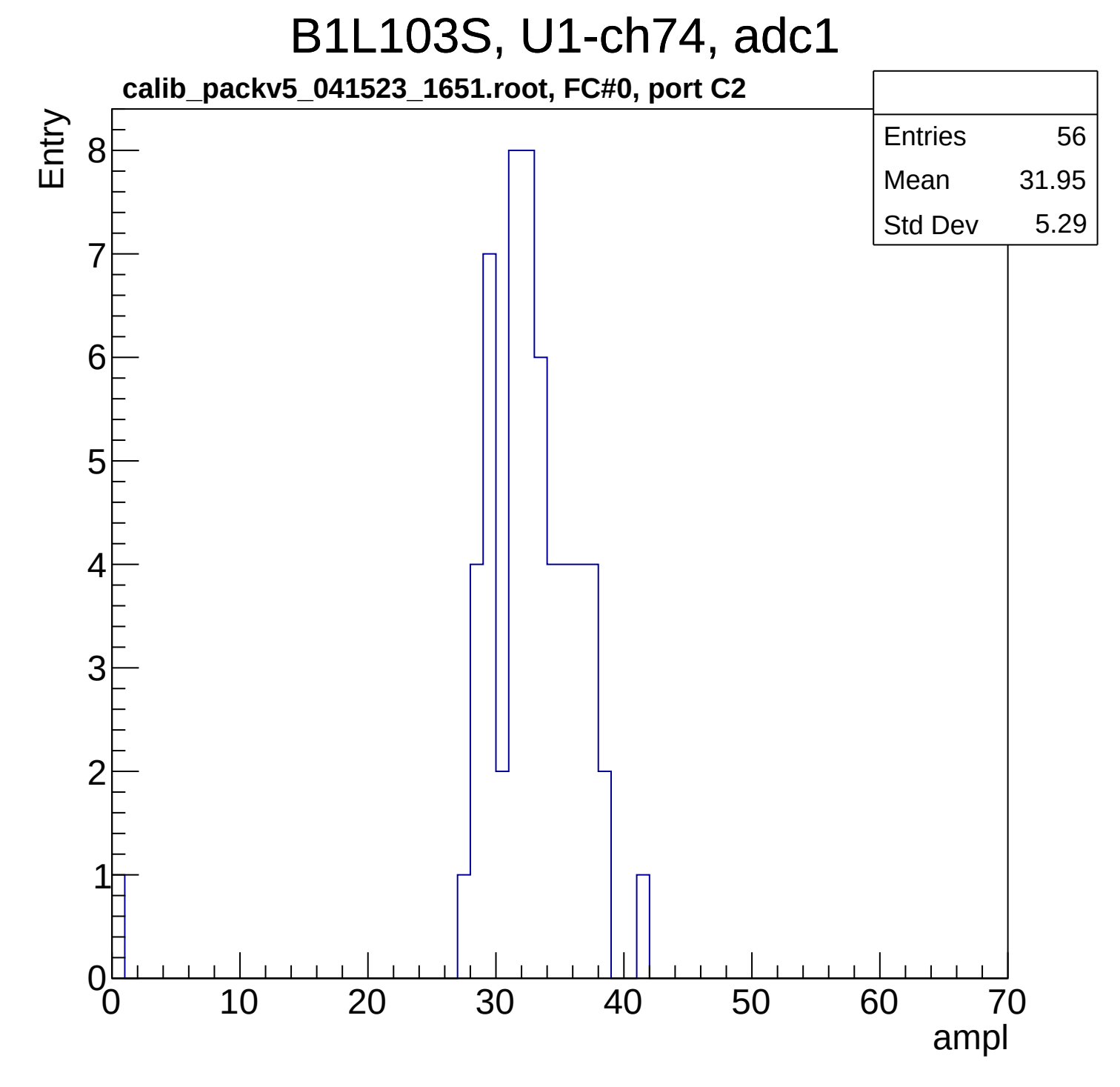
5
10
15
20
25
30
35
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch74, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 31.95
Std Dev 5.29
Entry
ampl
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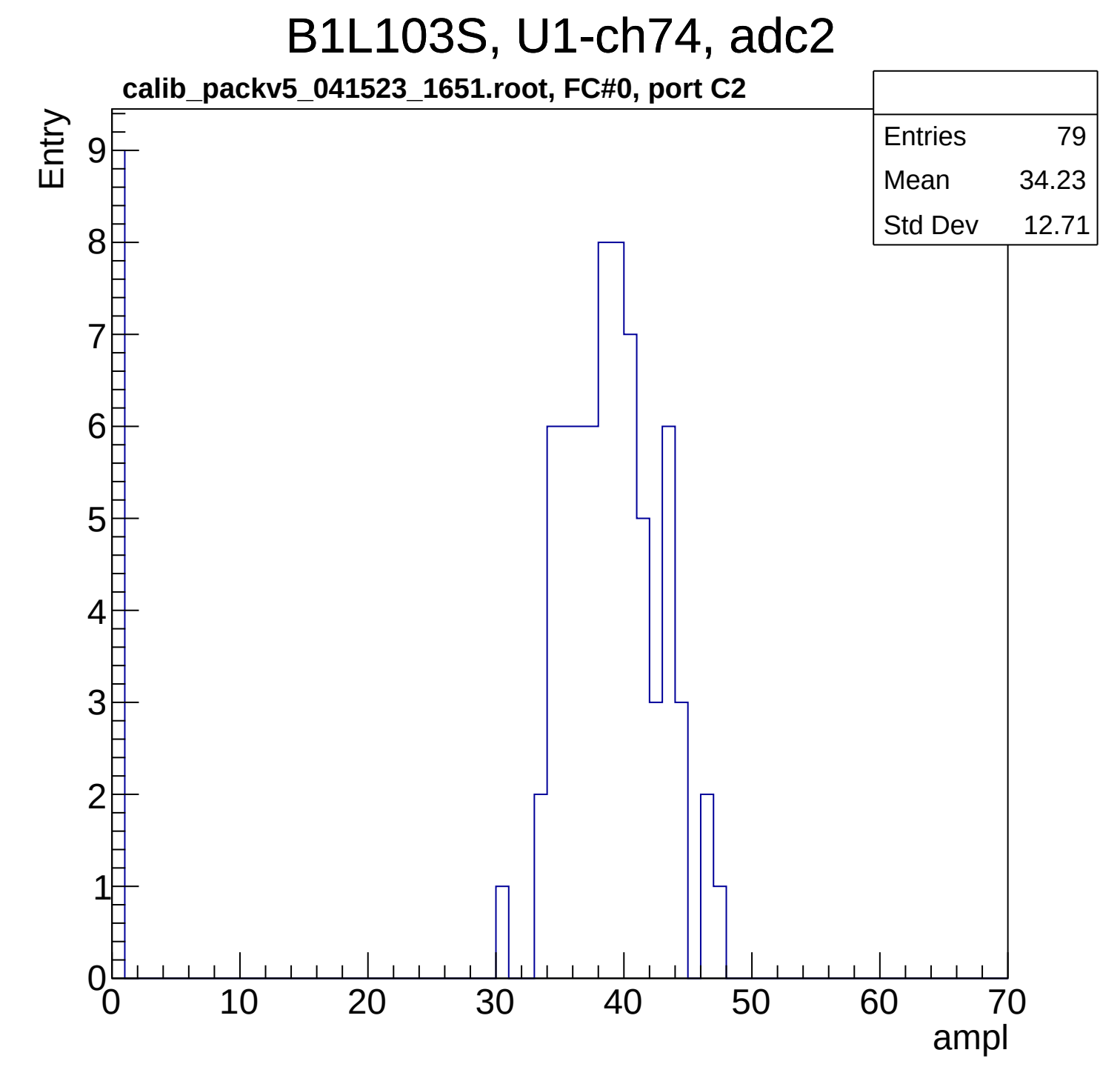
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U1-ch74, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 34.23
Std Dev 12.71
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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40
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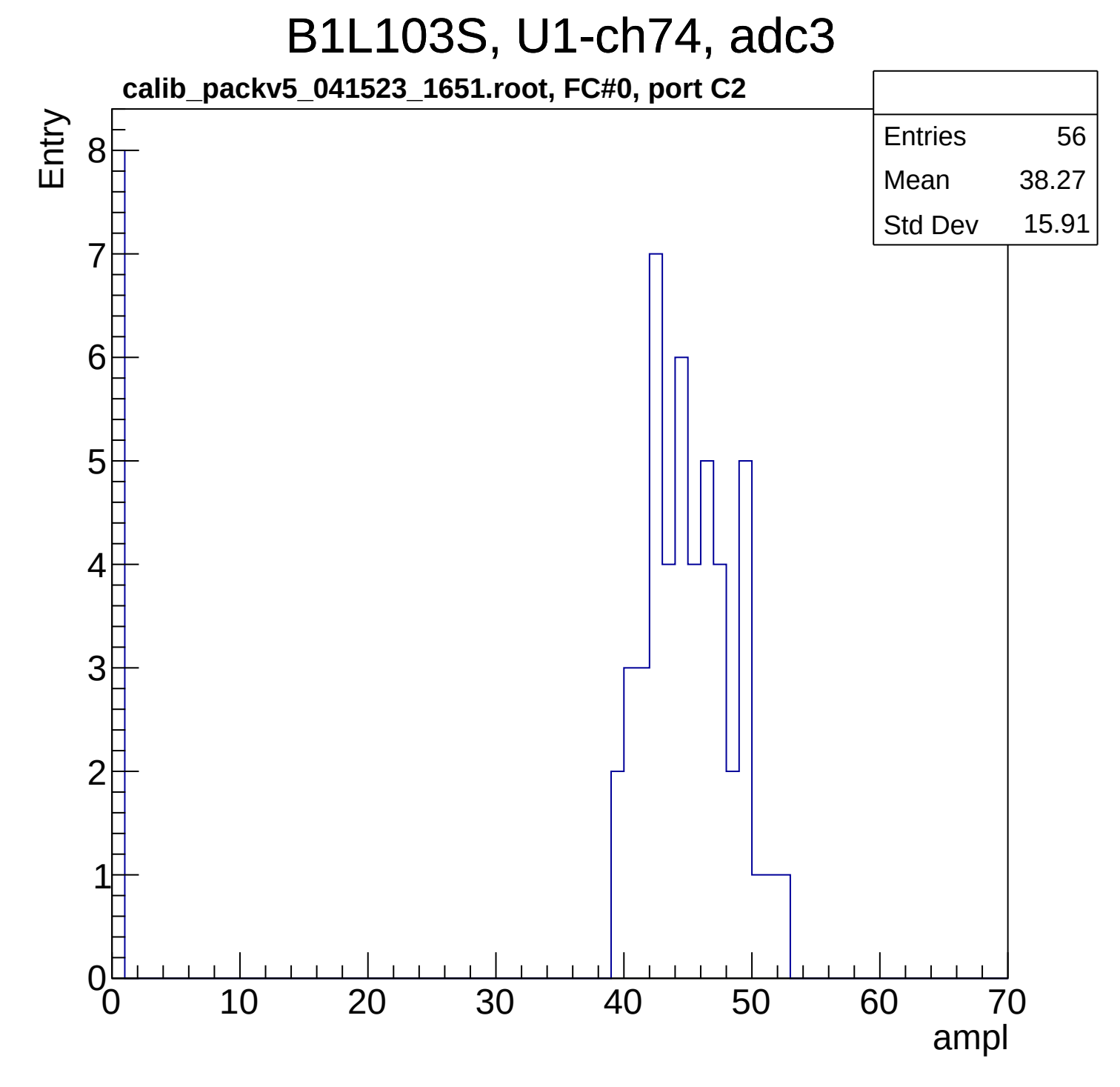
60
70


B1L103S, U1-ch74, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 38.27
Std Dev 15.91
Entry
ampl
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2
3
4
5
6
7
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0
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20
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40
50
60
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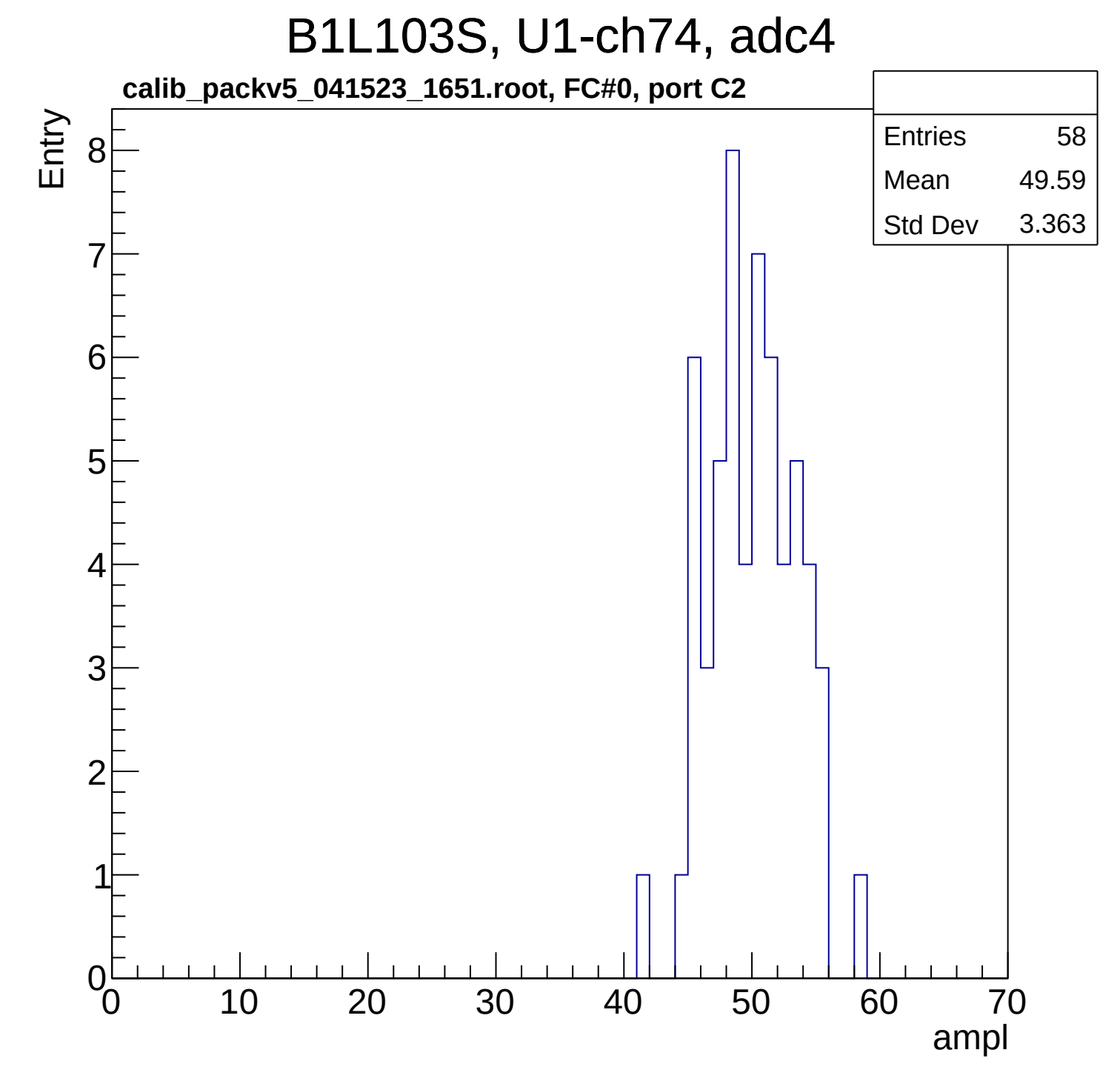
B1L103S, U1-ch74, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 49.59
Std Dev 3.363
Entry
ampl
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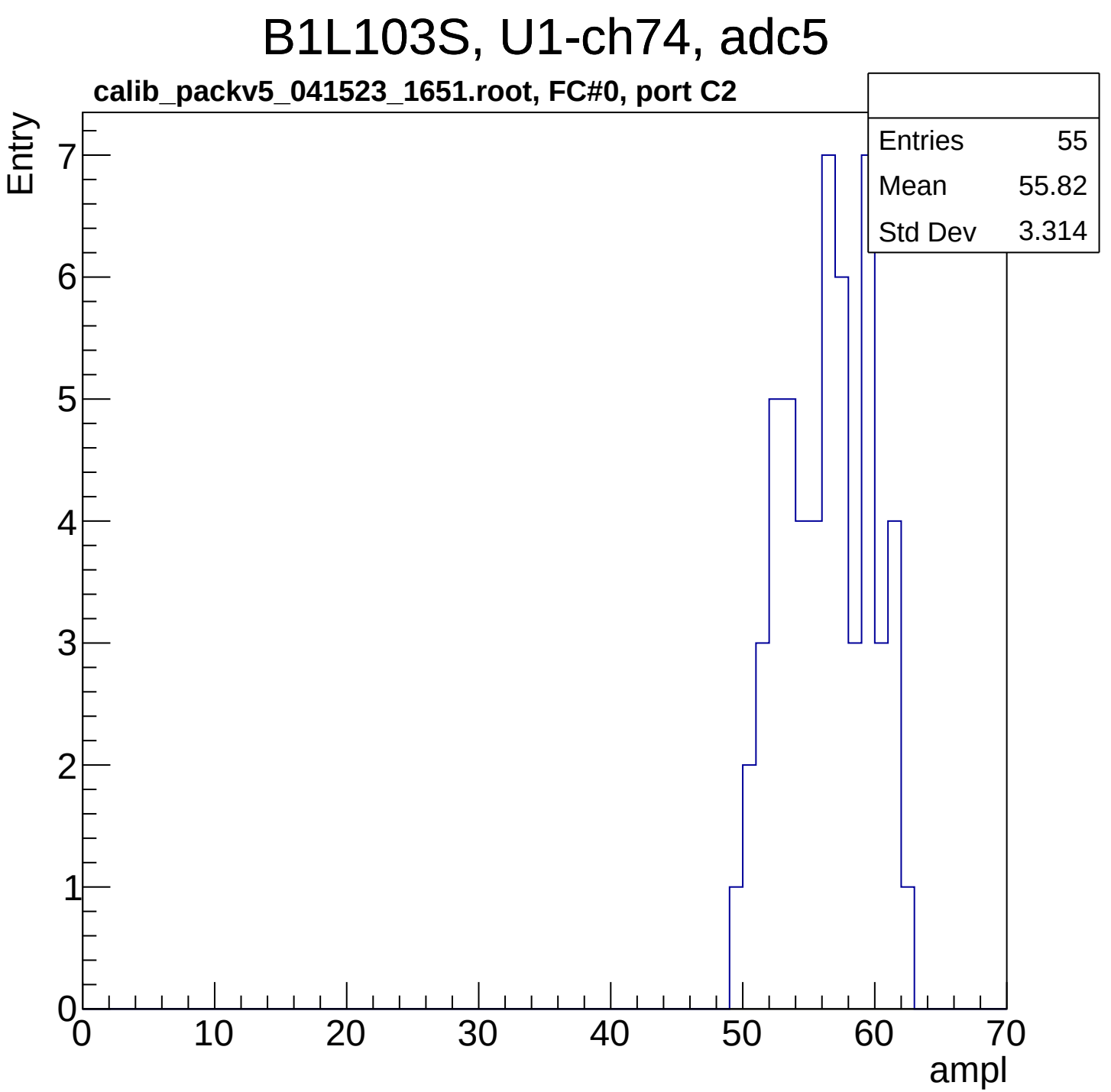
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U1-ch74, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 55.82
Std Dev 3.314
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
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40
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60
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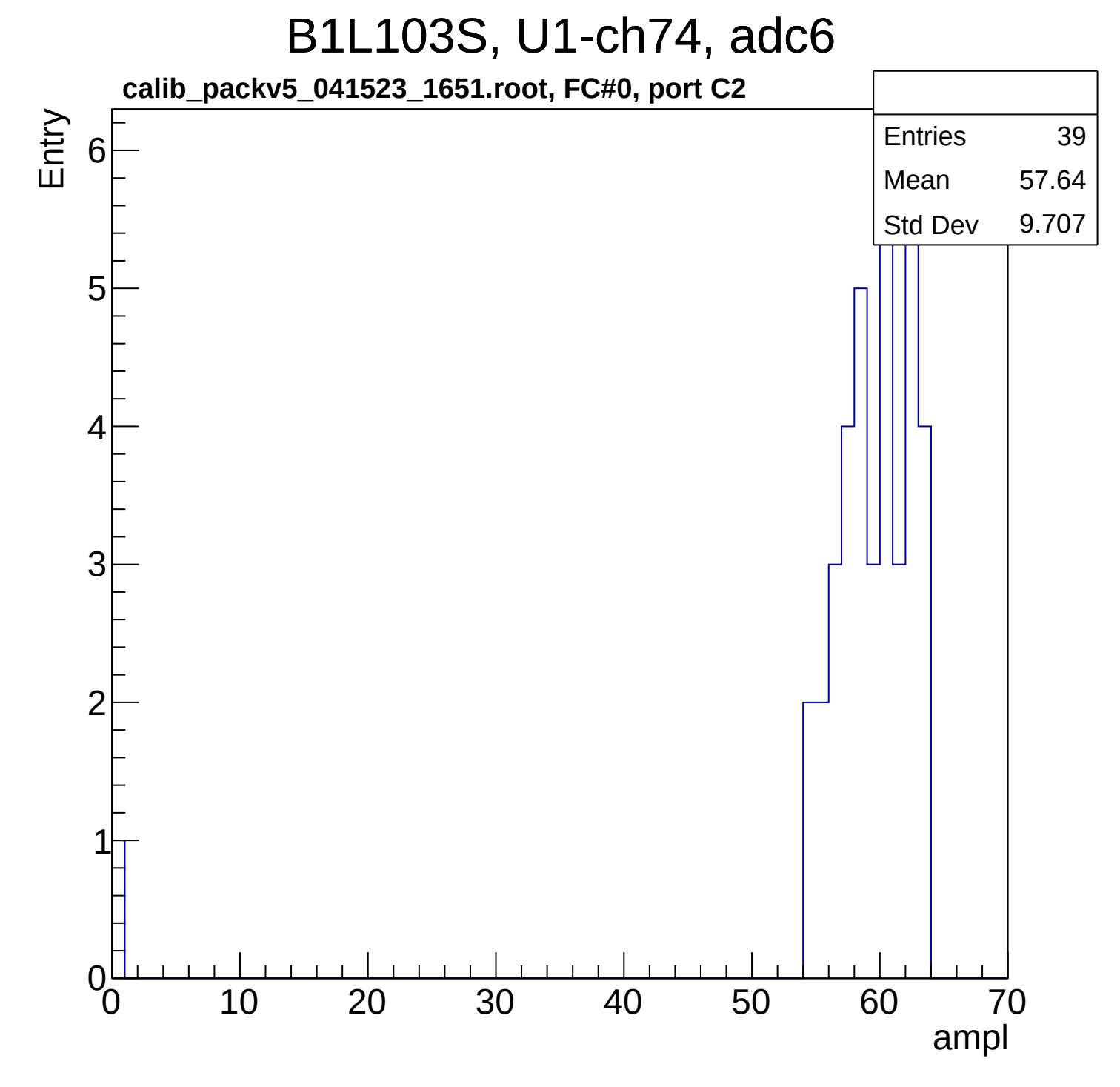
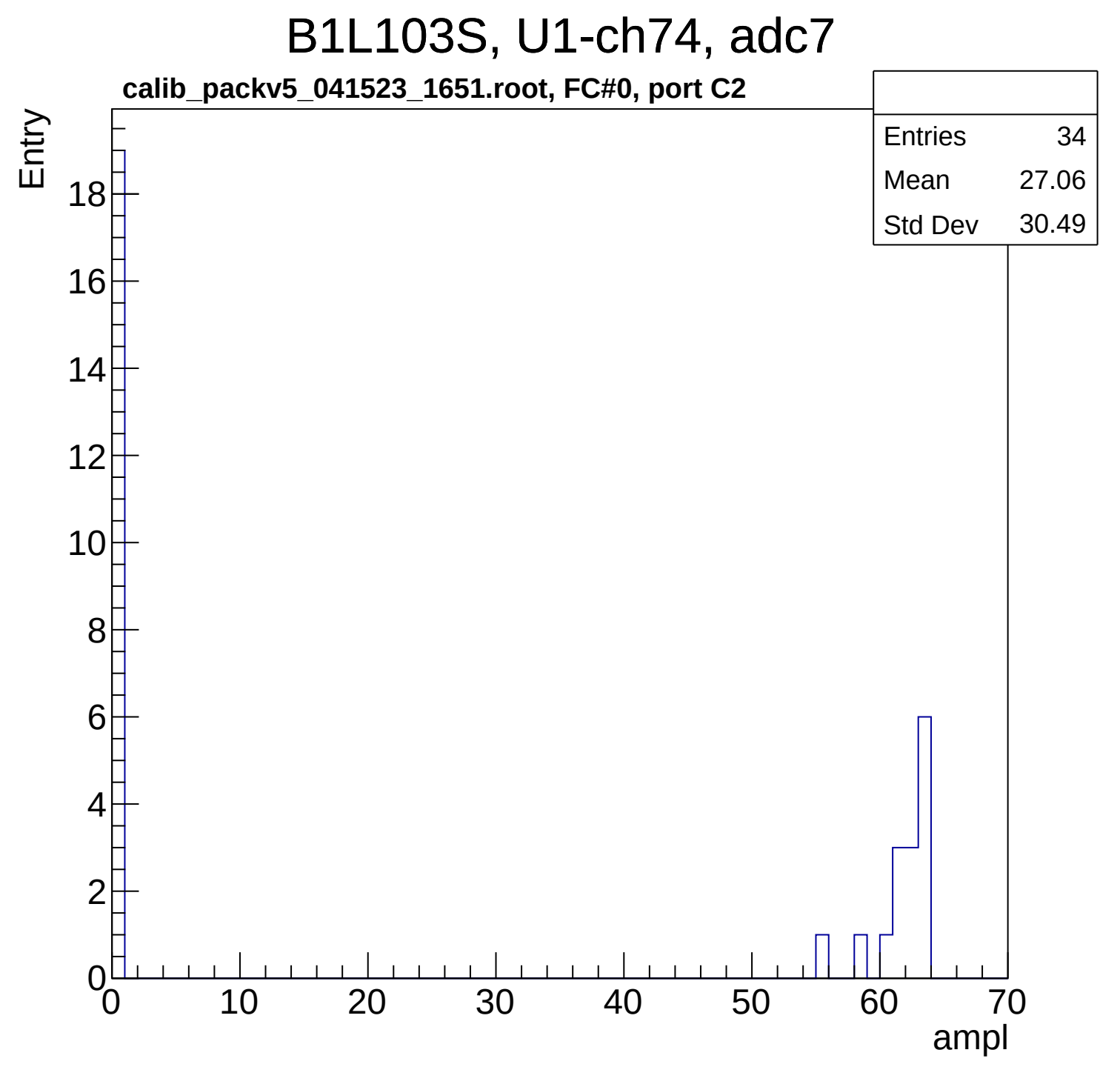

B1L103S, U1-ch74, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 39
Mean 57.64
Std Dev 9.707
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U1-ch74, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 34
Mean 27.06
Std Dev 30.49
Entry
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8
10
12
14
16
18
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10
20
30
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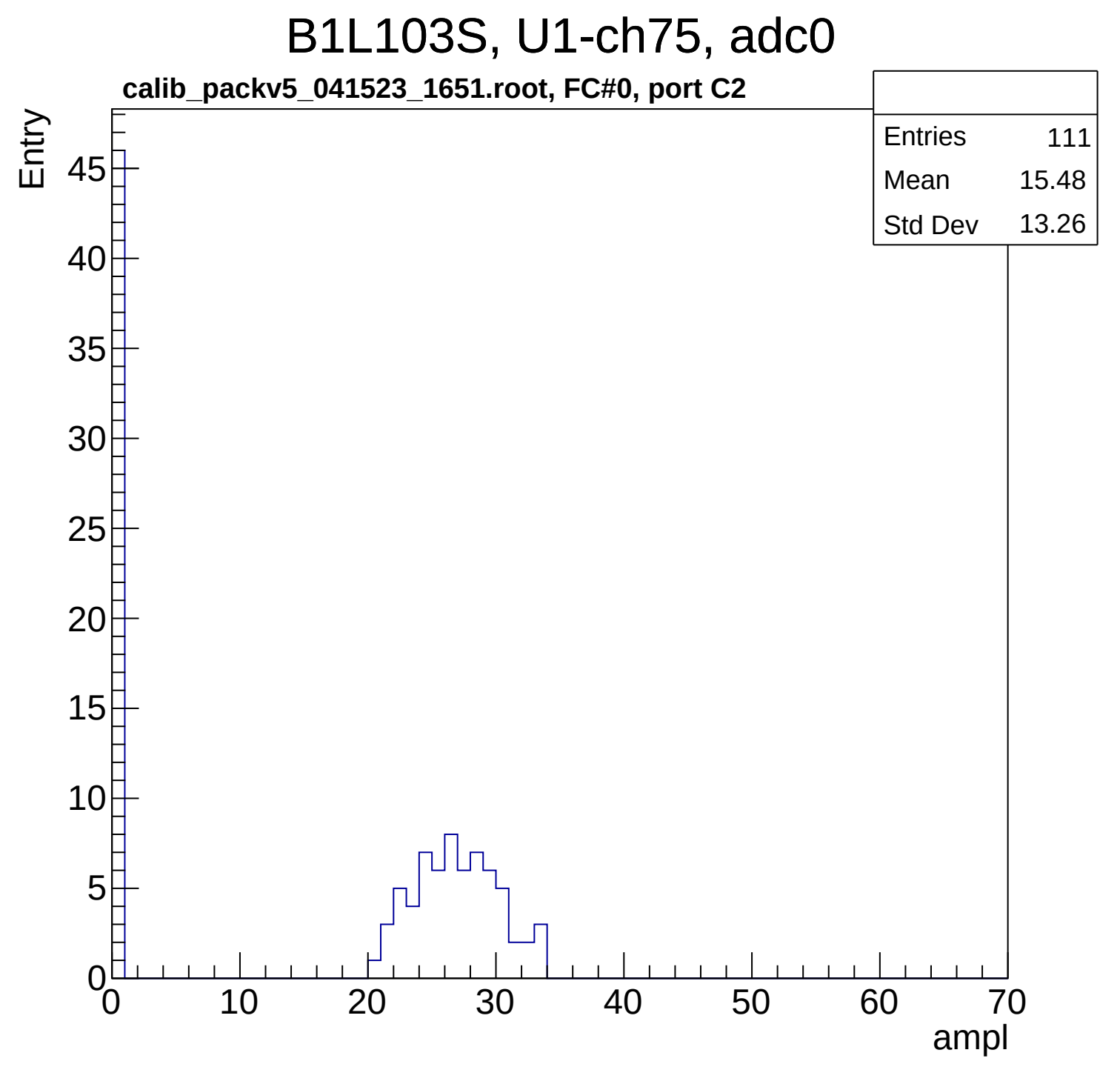
50
60
70
ampl


B1L103S, U1-ch75, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 111
Mean 15.48
Std Dev 13.26
Entry
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15
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25
30
35
40
45
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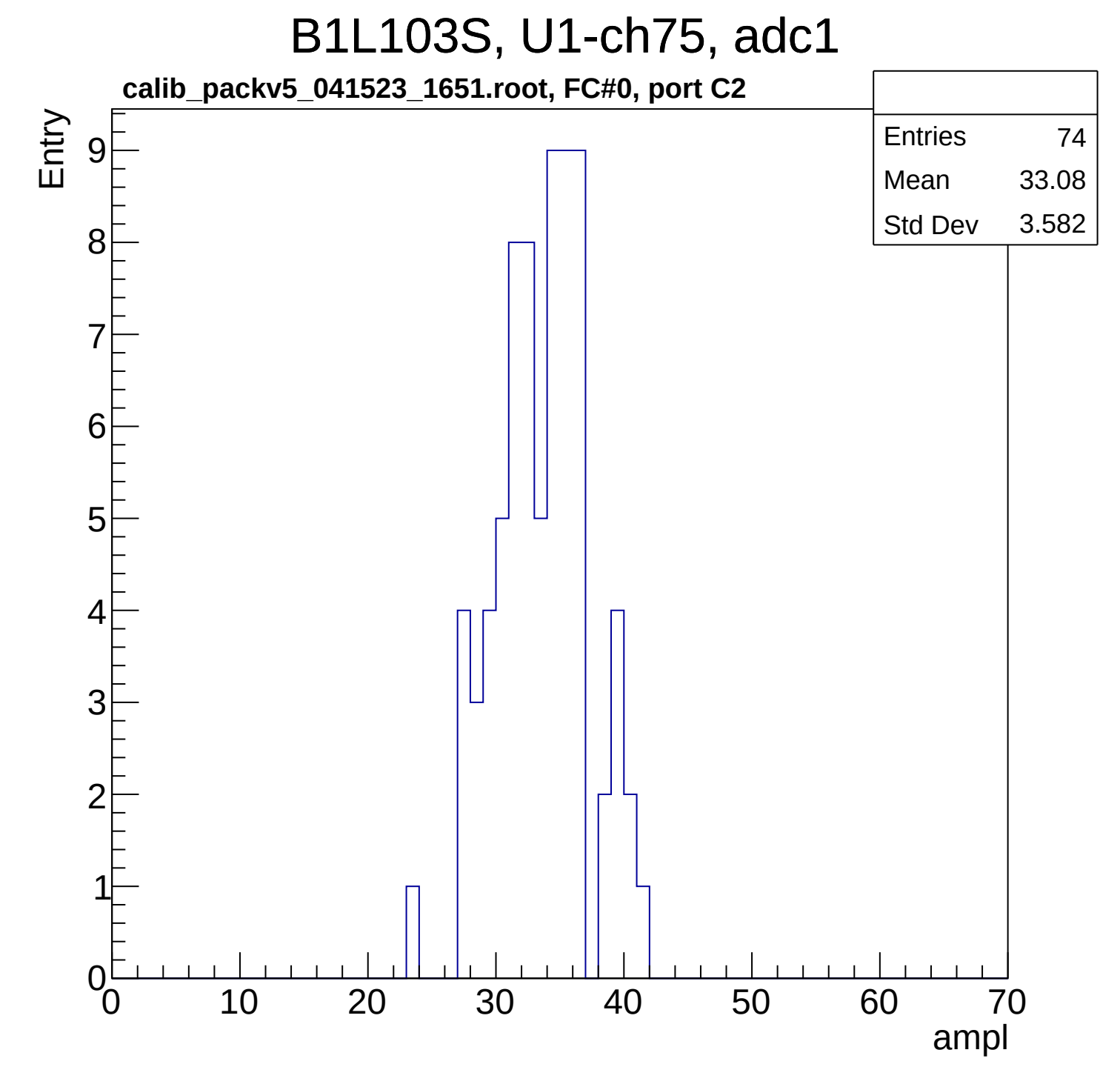
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch75, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 33.08
Std Dev 3.582
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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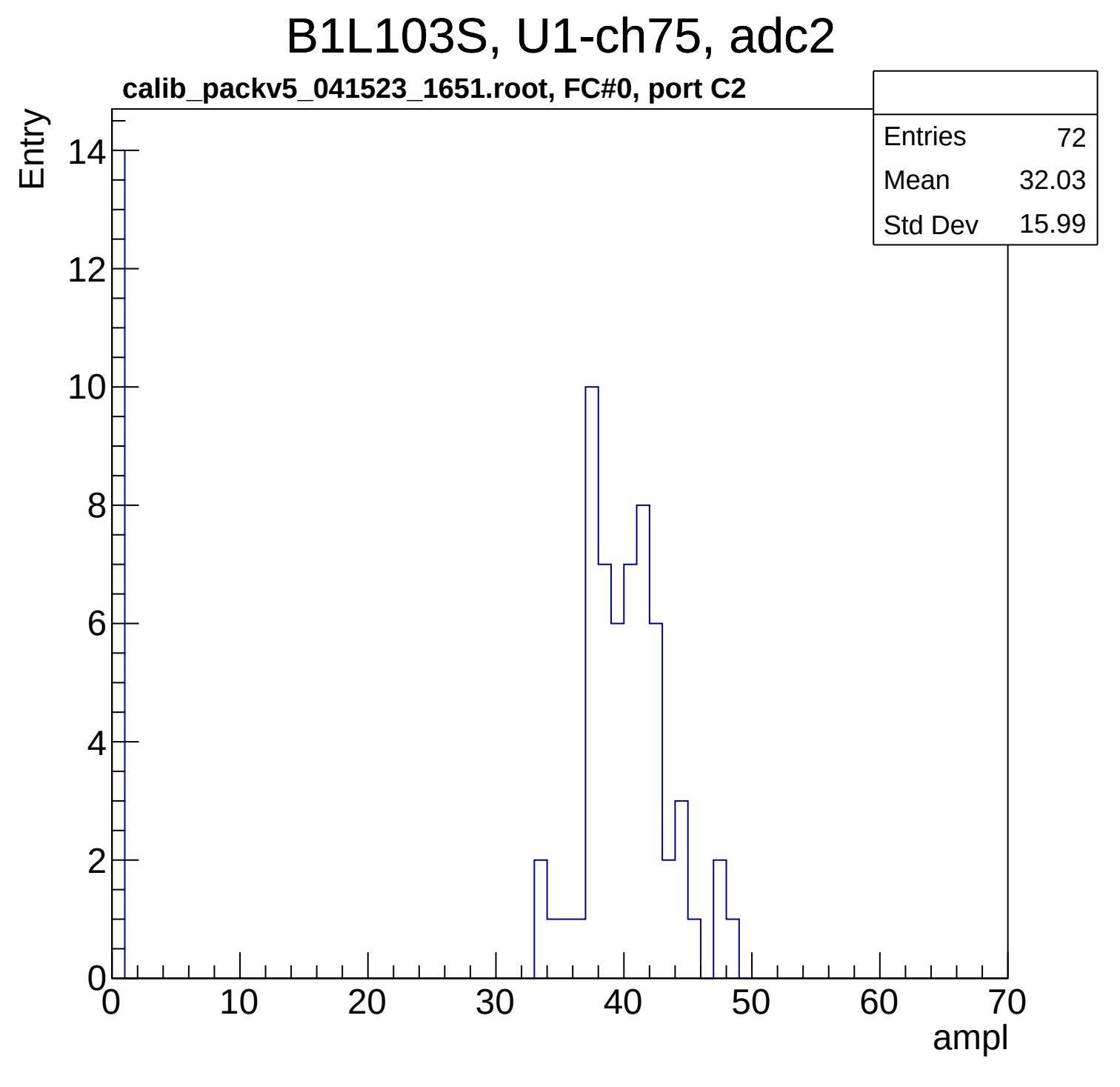
40
50
60
70


B1L103S, U1-ch75, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 32.03
Std Dev 15.99
Entry
ampl
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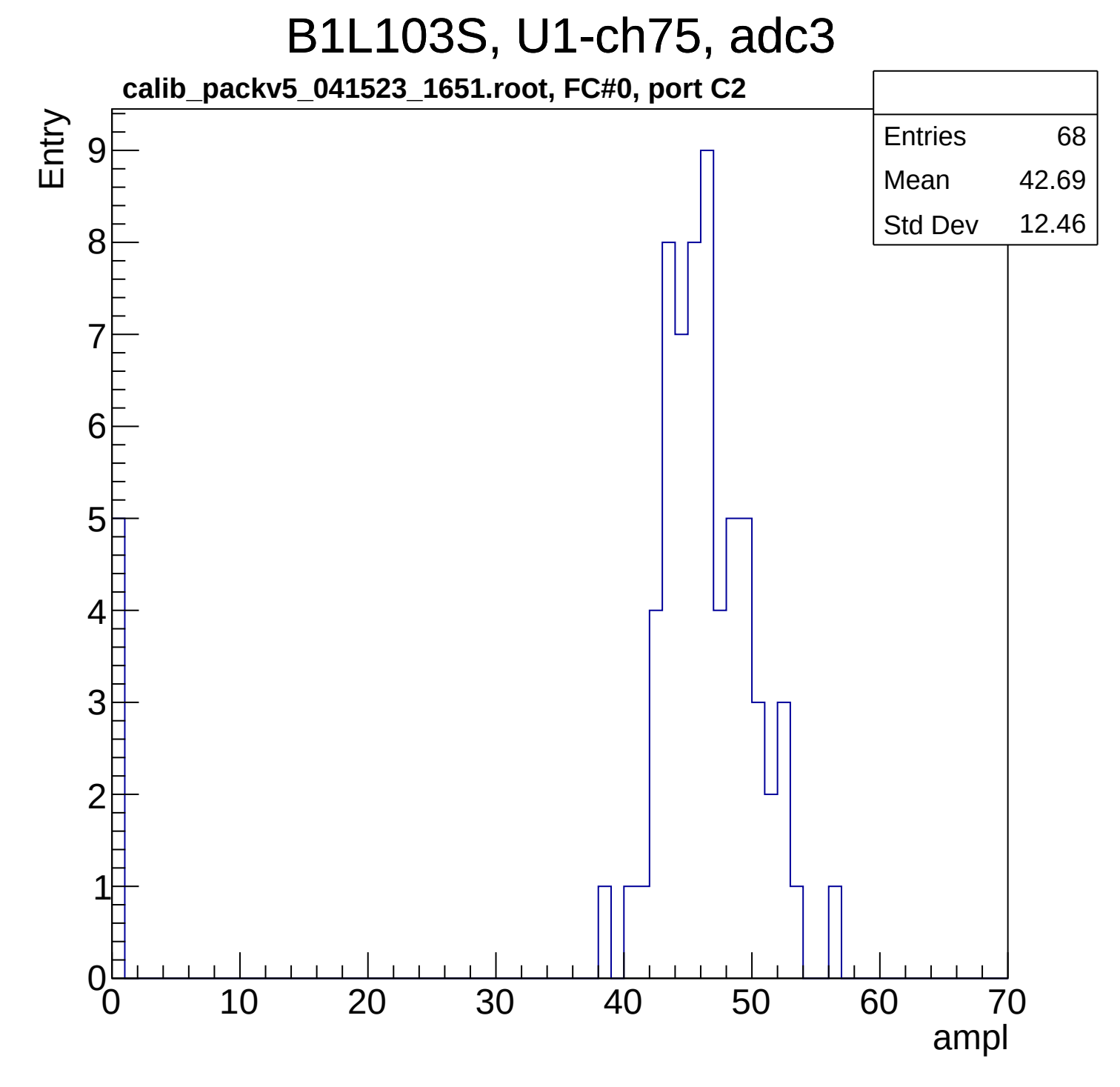
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L103S, U1-ch75, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 42.69
Std Dev 12.46
Entry
ampl
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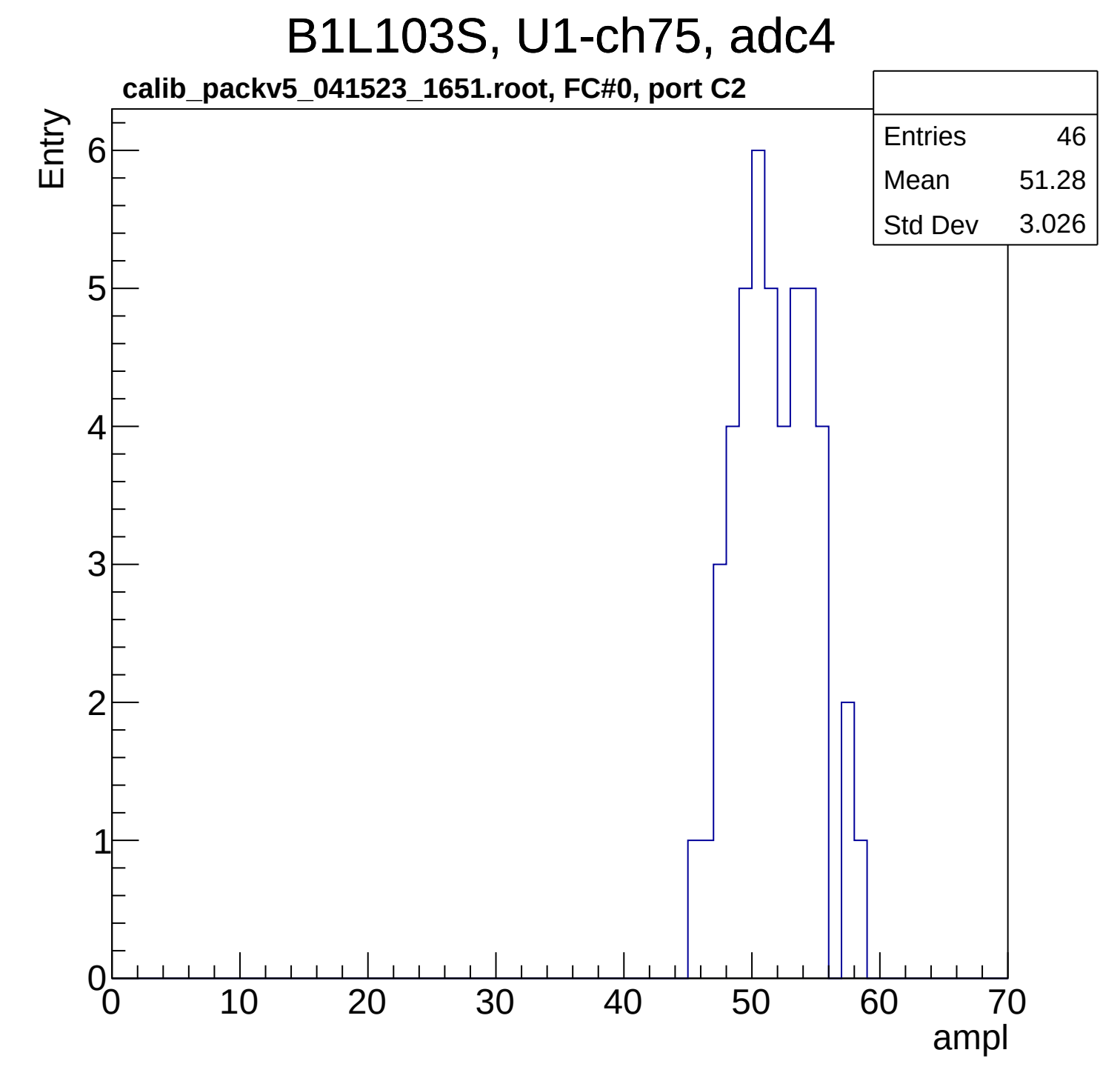
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U1-ch75, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 51.28
Std Dev 3.026
Entry
ampl
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2
3
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5
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0
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60
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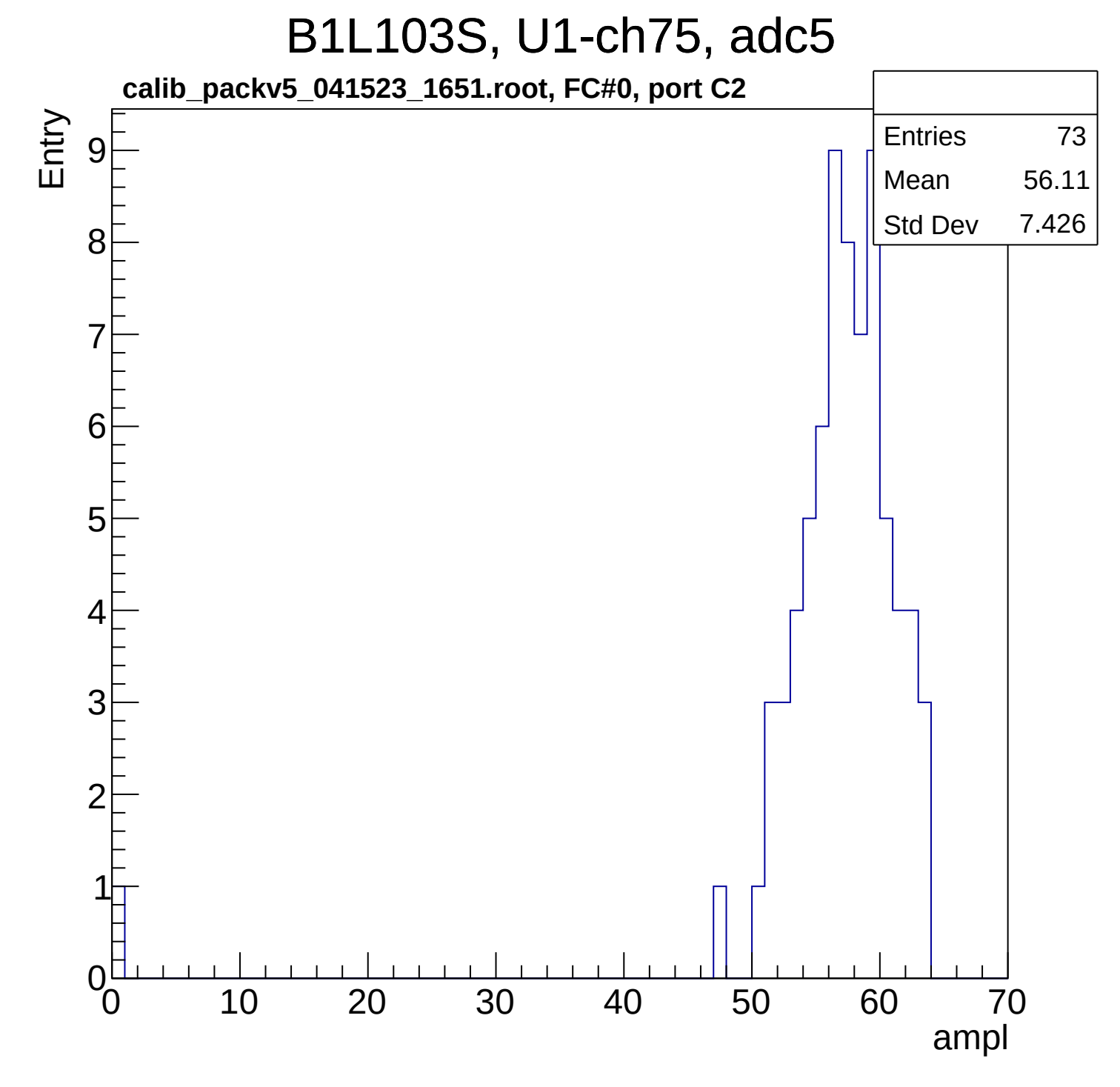
B1L103S, U1-ch75, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 56.11
Std Dev 7.426
Entry
ampl
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3
4
5
6
7
8
9
0
10
20
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60
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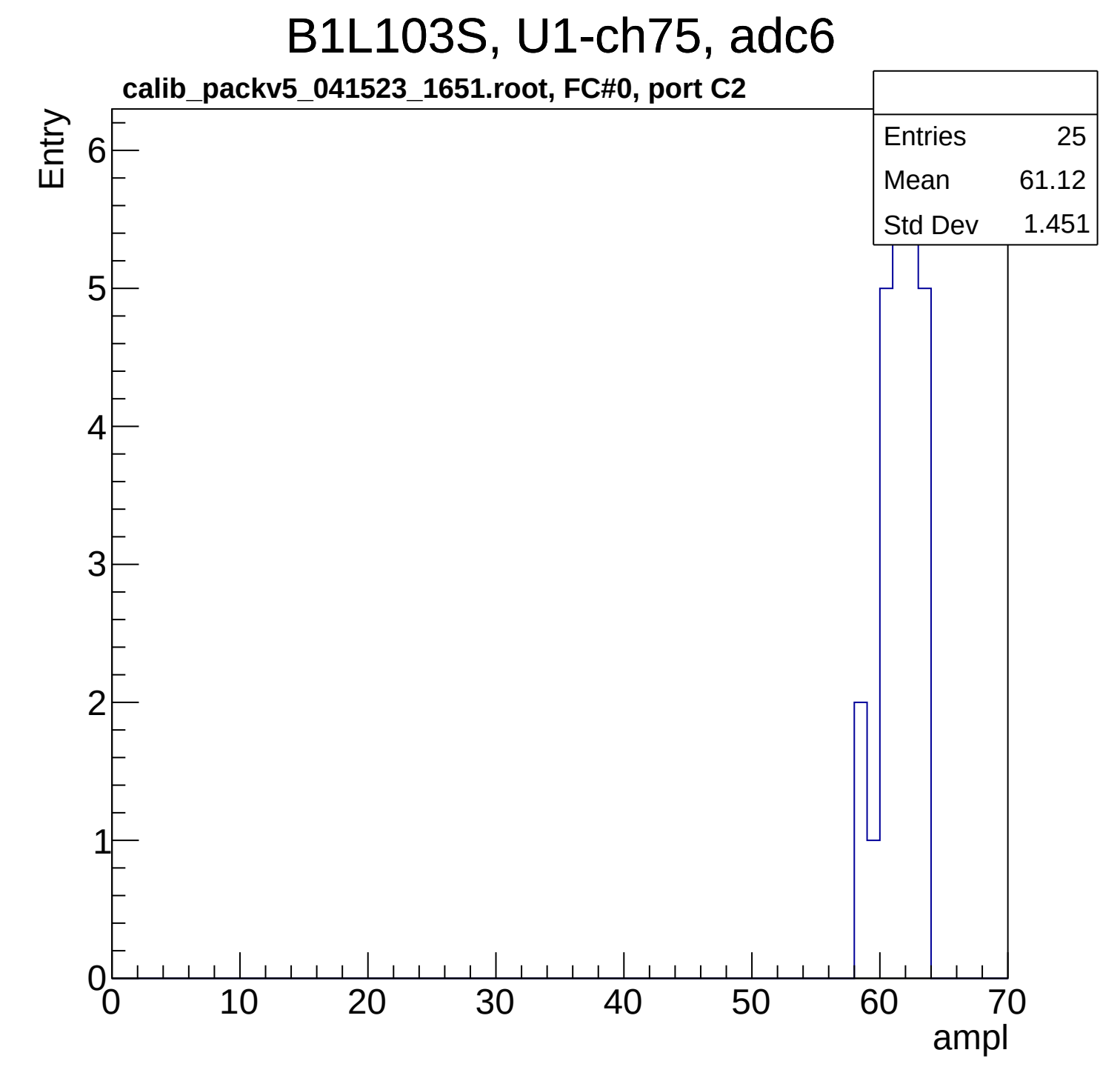
B1L103S, U1-ch75, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 25
Mean 61.12
Std Dev 1.451
Entry
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2
3
4
5
6
0
10
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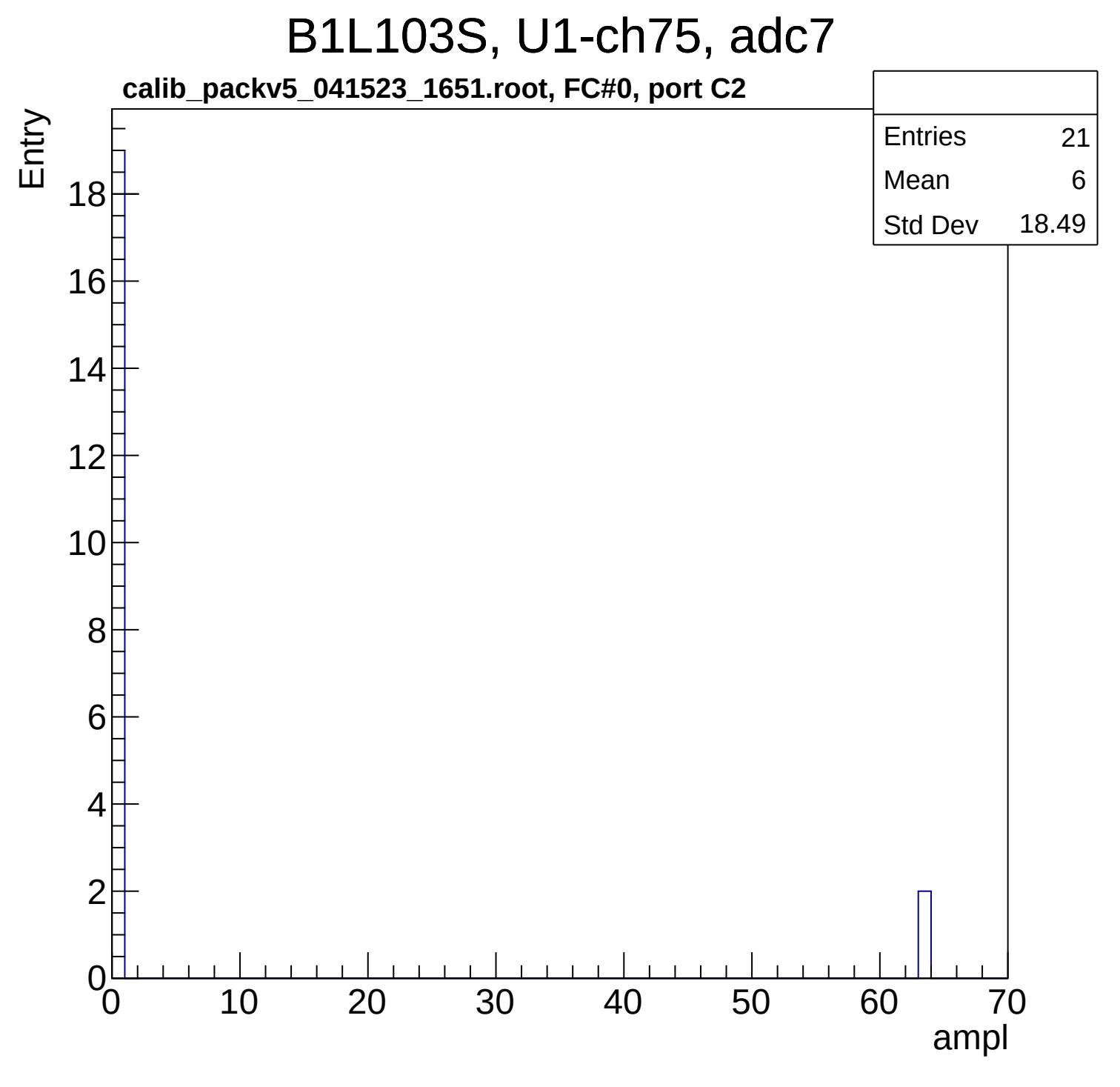
30
40
50
60
70
ampl


B1L103S, U1-ch75, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 6
Std Dev 18.49
Entry
0
2
4
6
8
10
12
14
16
18
0
10
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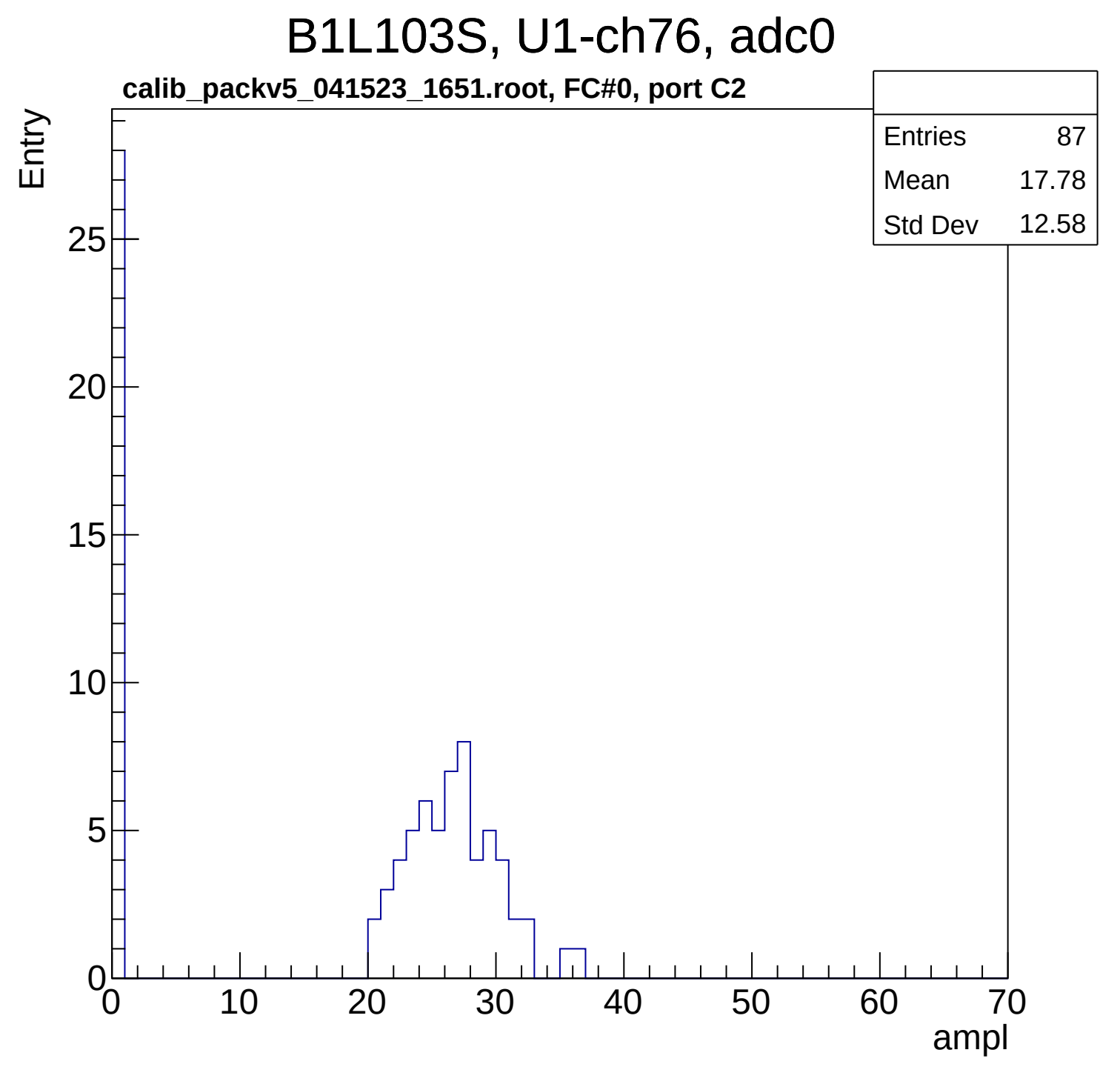
50
60
70
ampl


B1L103S, U1-ch76, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 87
Mean 17.78
Std Dev 12.58
Entry
0
5
10
15
20
25
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10
20
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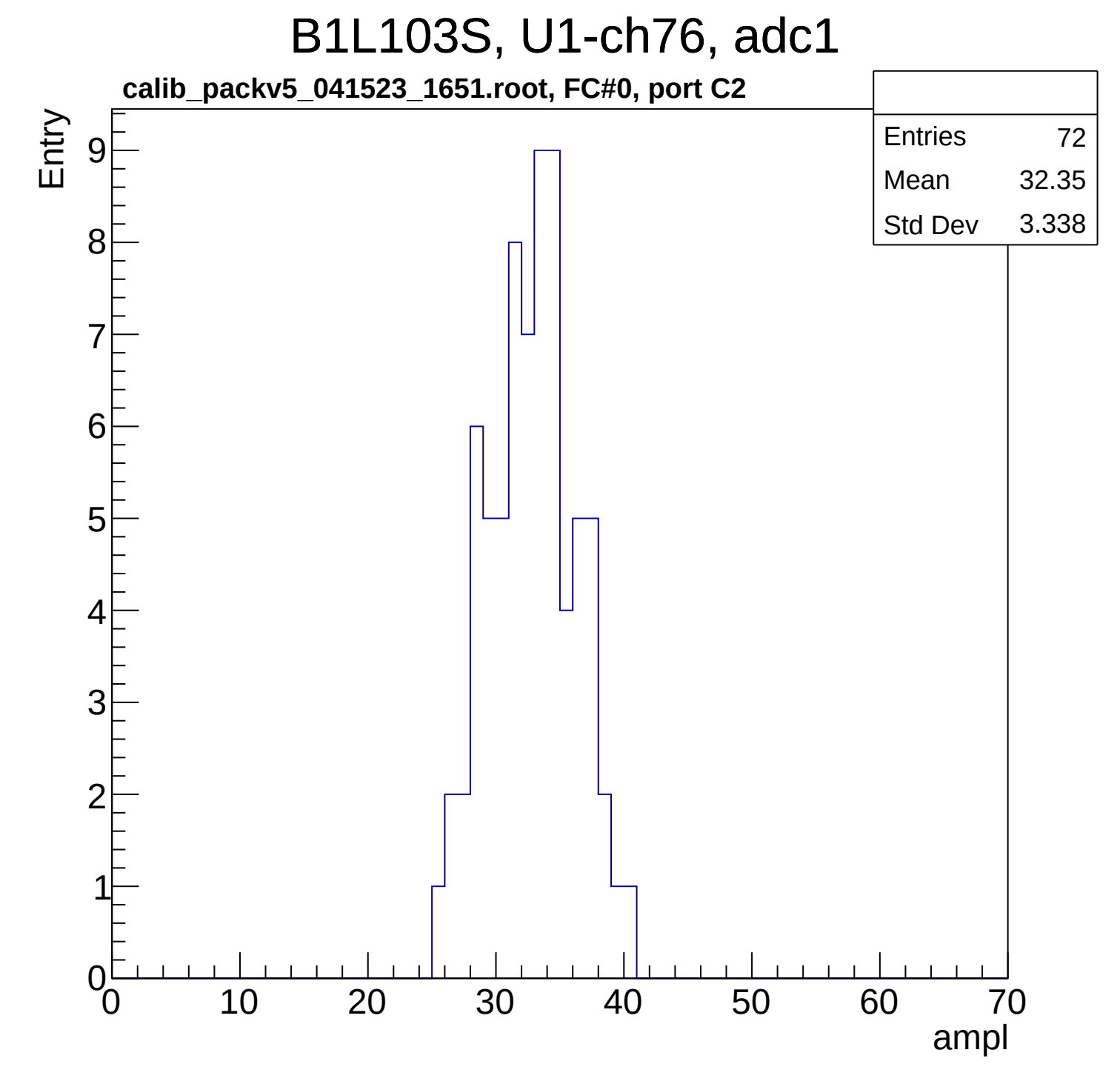
50
60
70
ampl


B1L103S, U1-ch76, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 32.35
Std Dev 3.338
Entry
ampl
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3
4
5
6
7
8
9
0
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40
50
60
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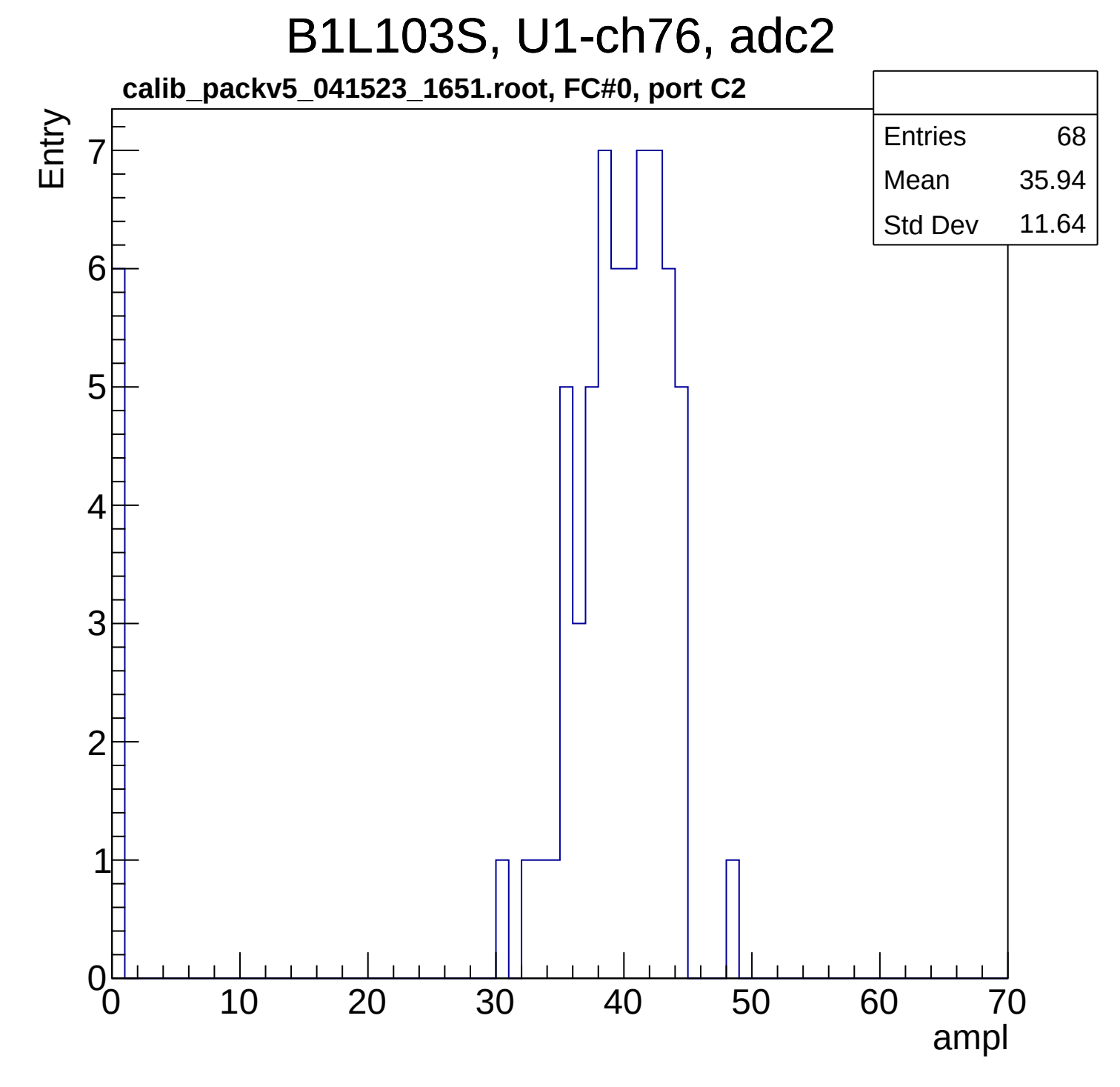
B1L103S, U1-ch76, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 35.94
Std Dev 11.64
Entry
ampl
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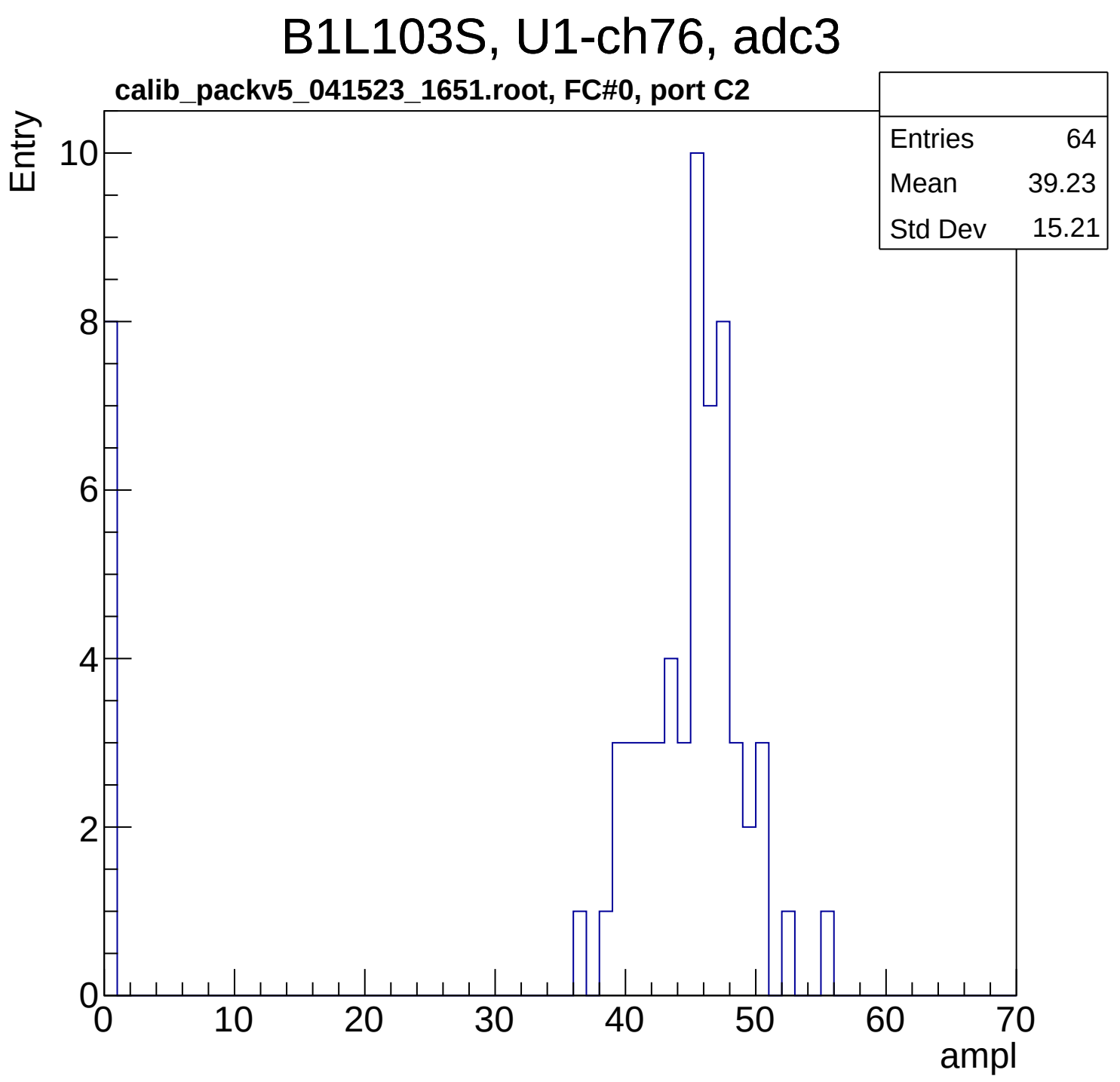
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U1-ch76, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 39.23
Std Dev 15.21
Entry
ampl
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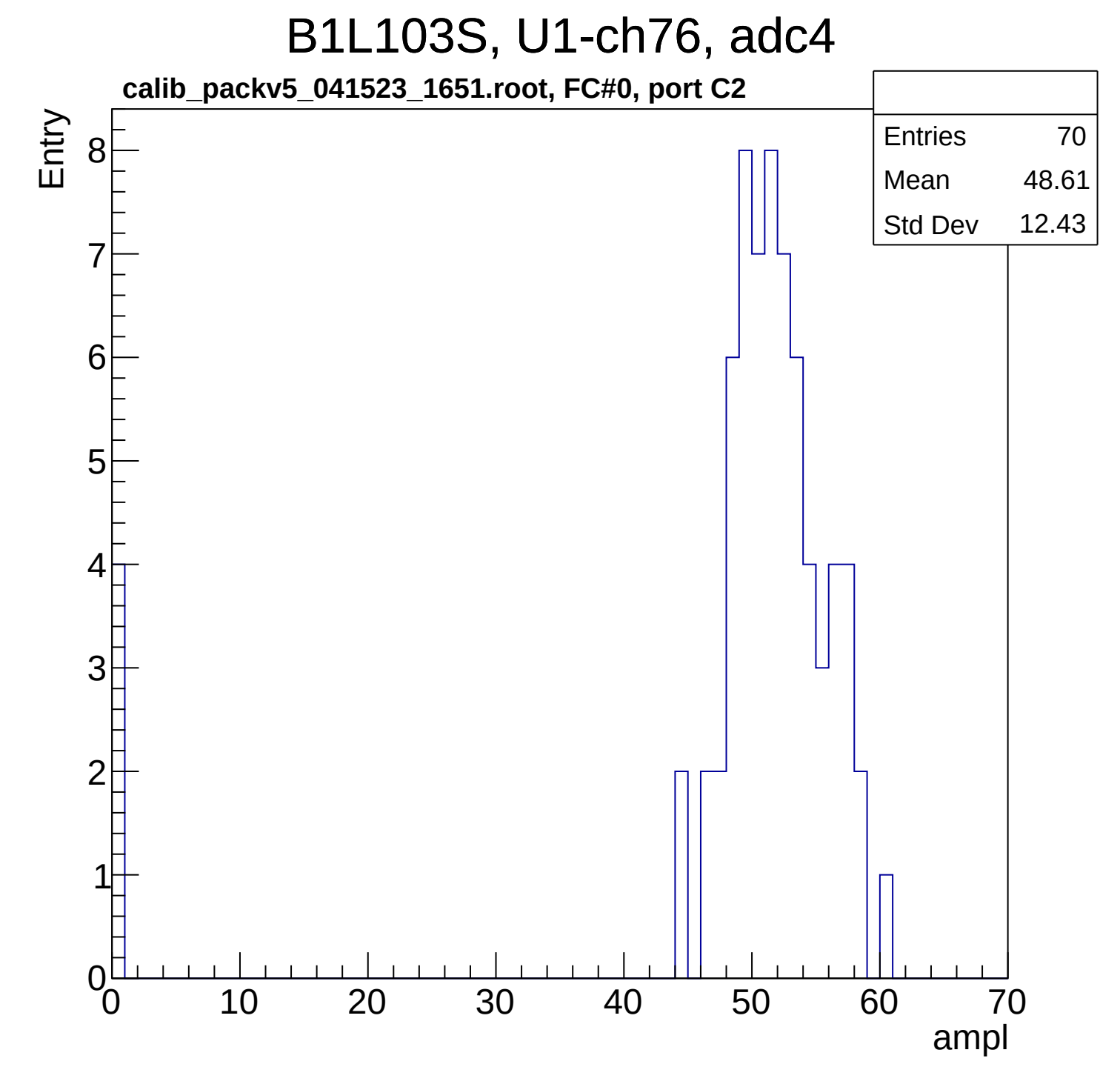
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U1-ch76, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 48.61
Std Dev 12.43
Entry
ampl
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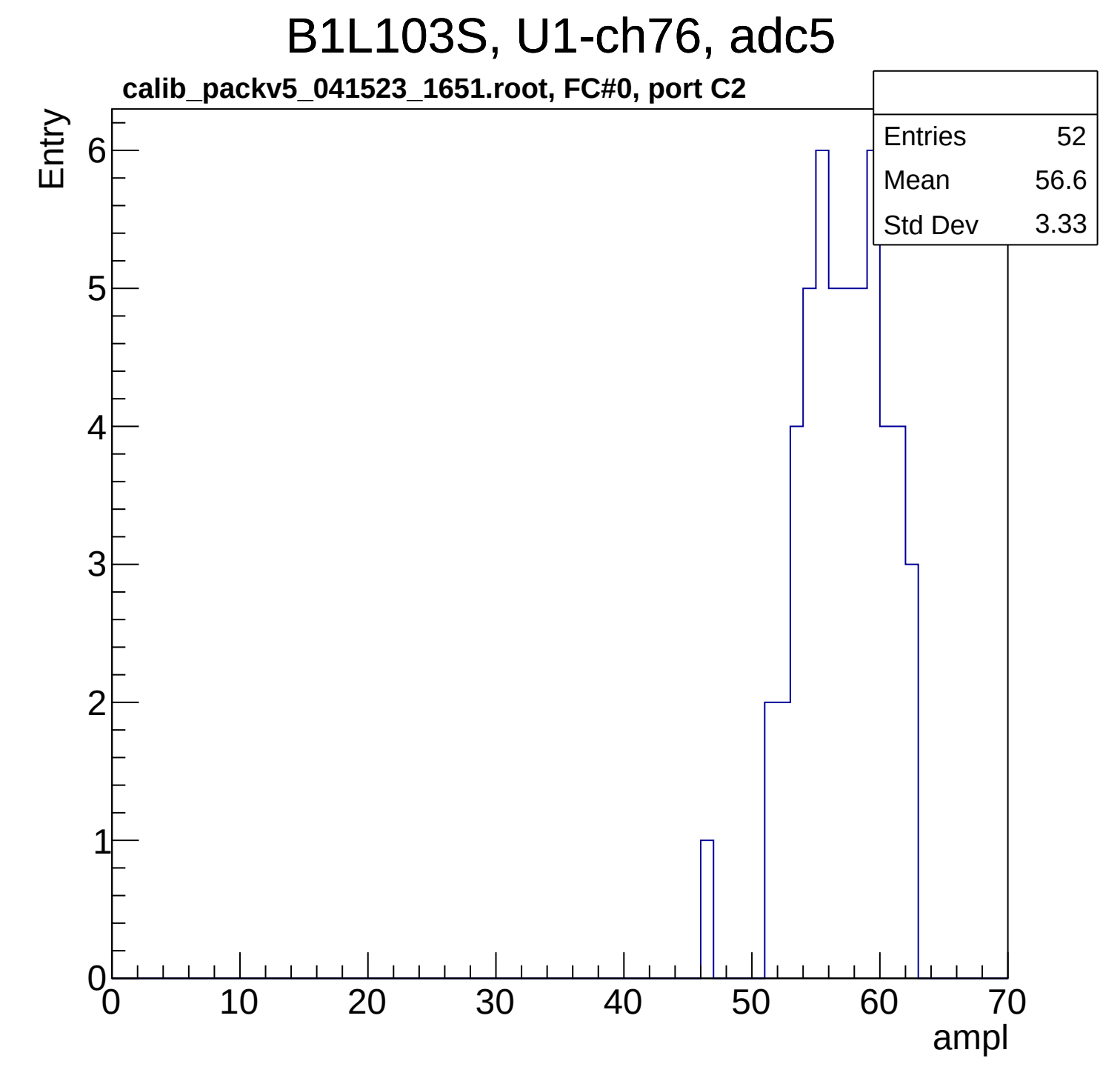
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U1-ch76, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 56.6
Std Dev 3.33
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
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60
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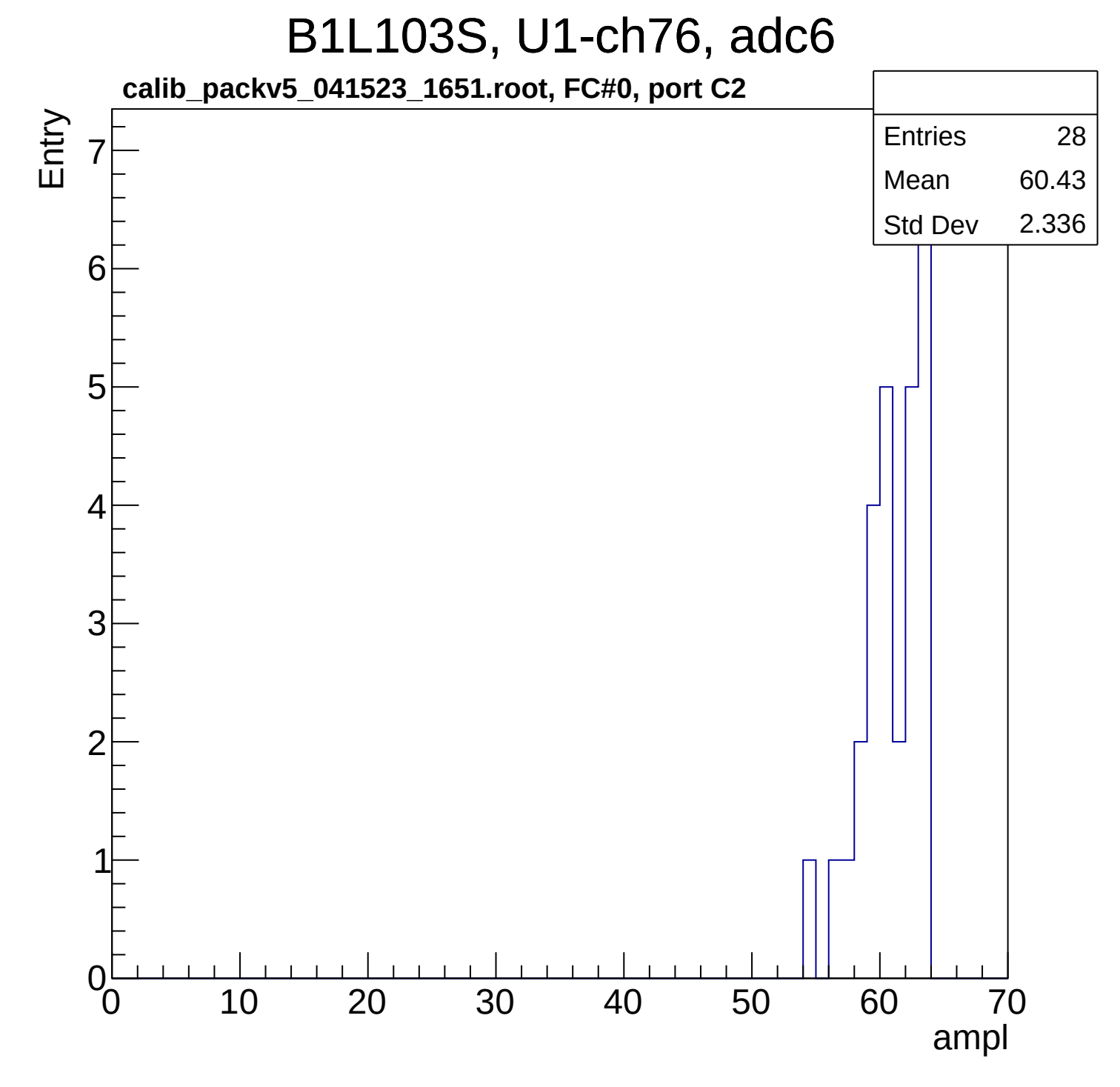
B1L103S, U1-ch76, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 28
Mean 60.43
Std Dev 2.336
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
30
40
50
60
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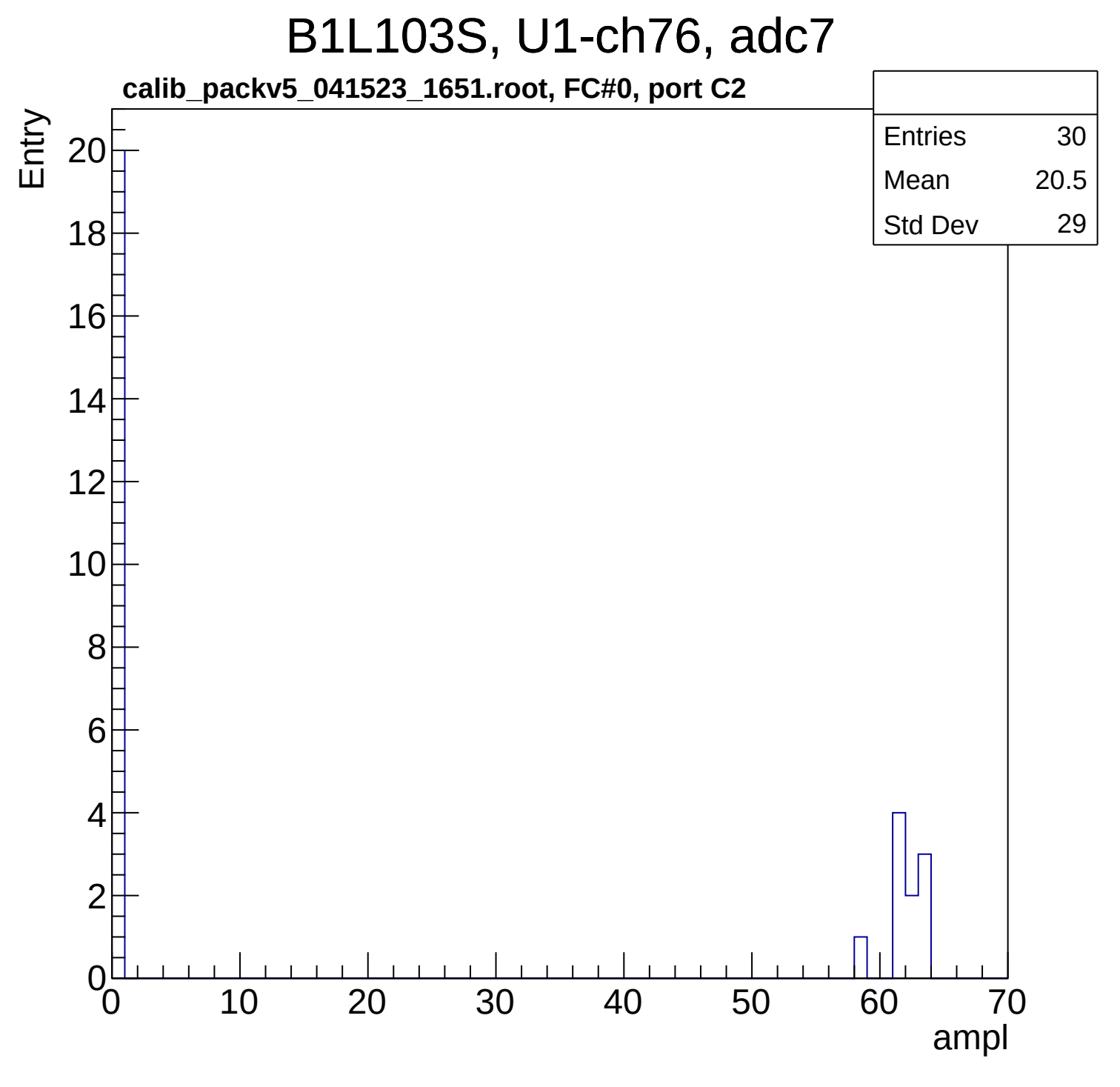
B1L103S, U1-ch76, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 30
Mean 20.5
Std Dev 29
Entry
ampl
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4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
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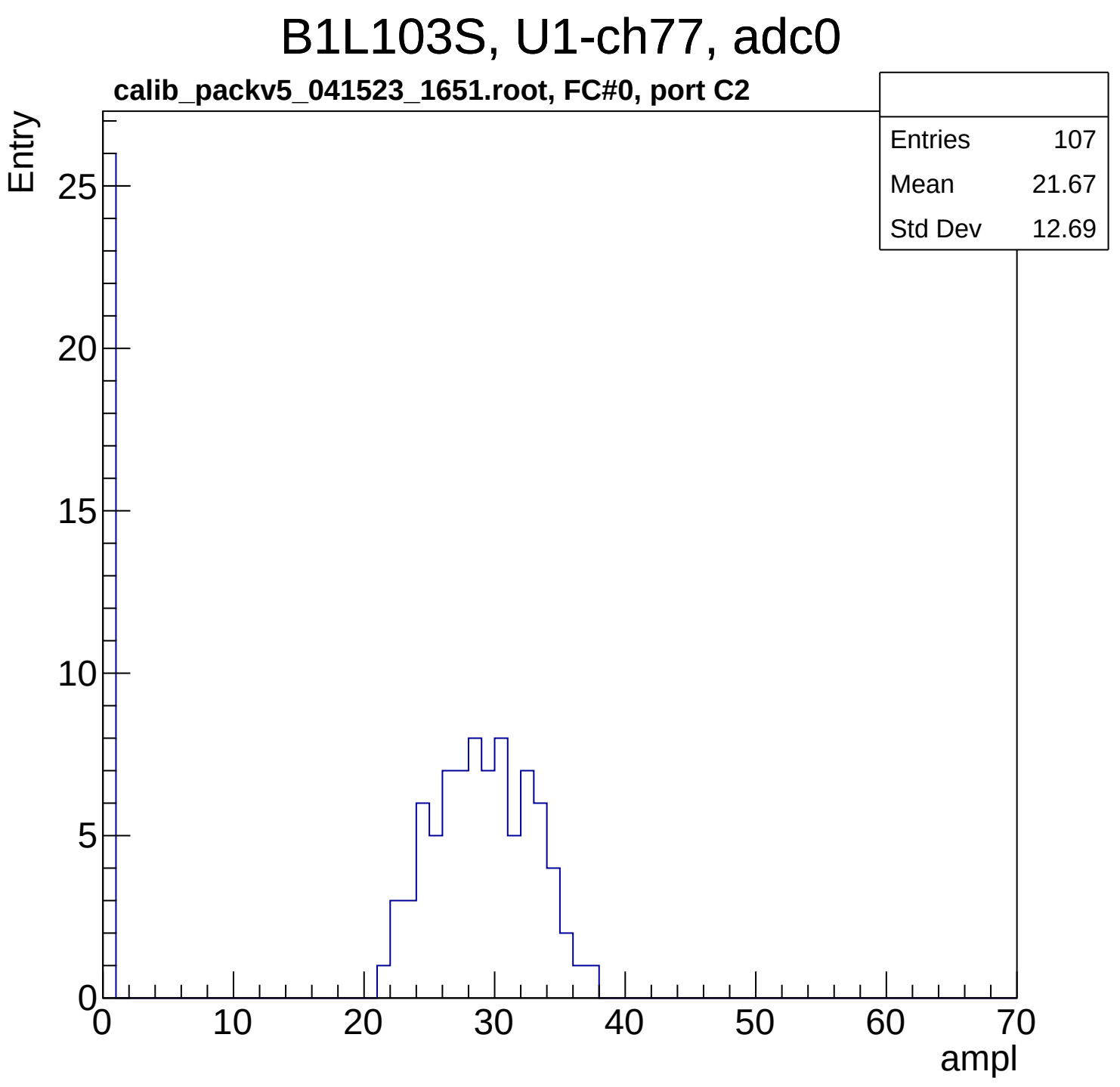
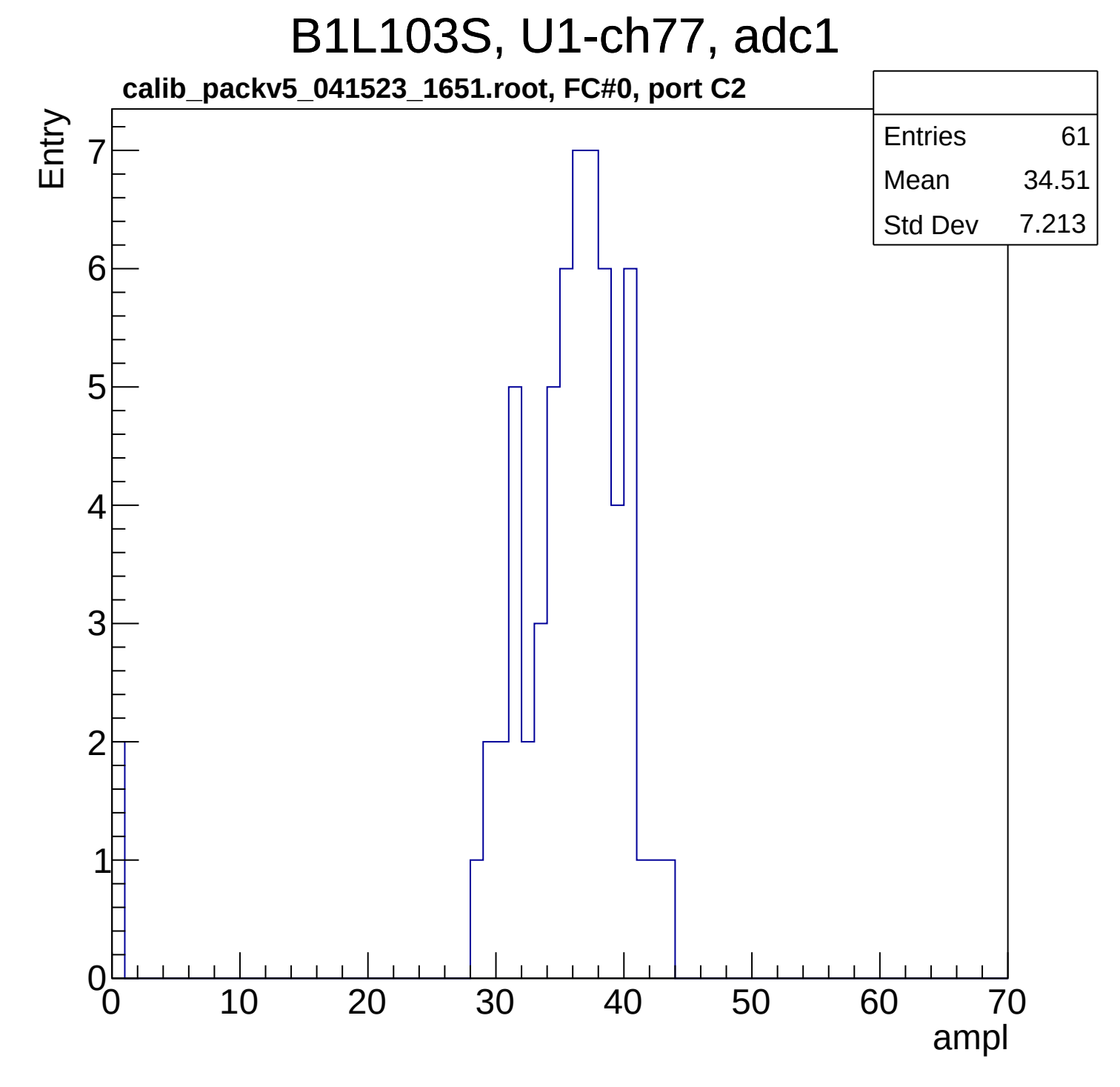
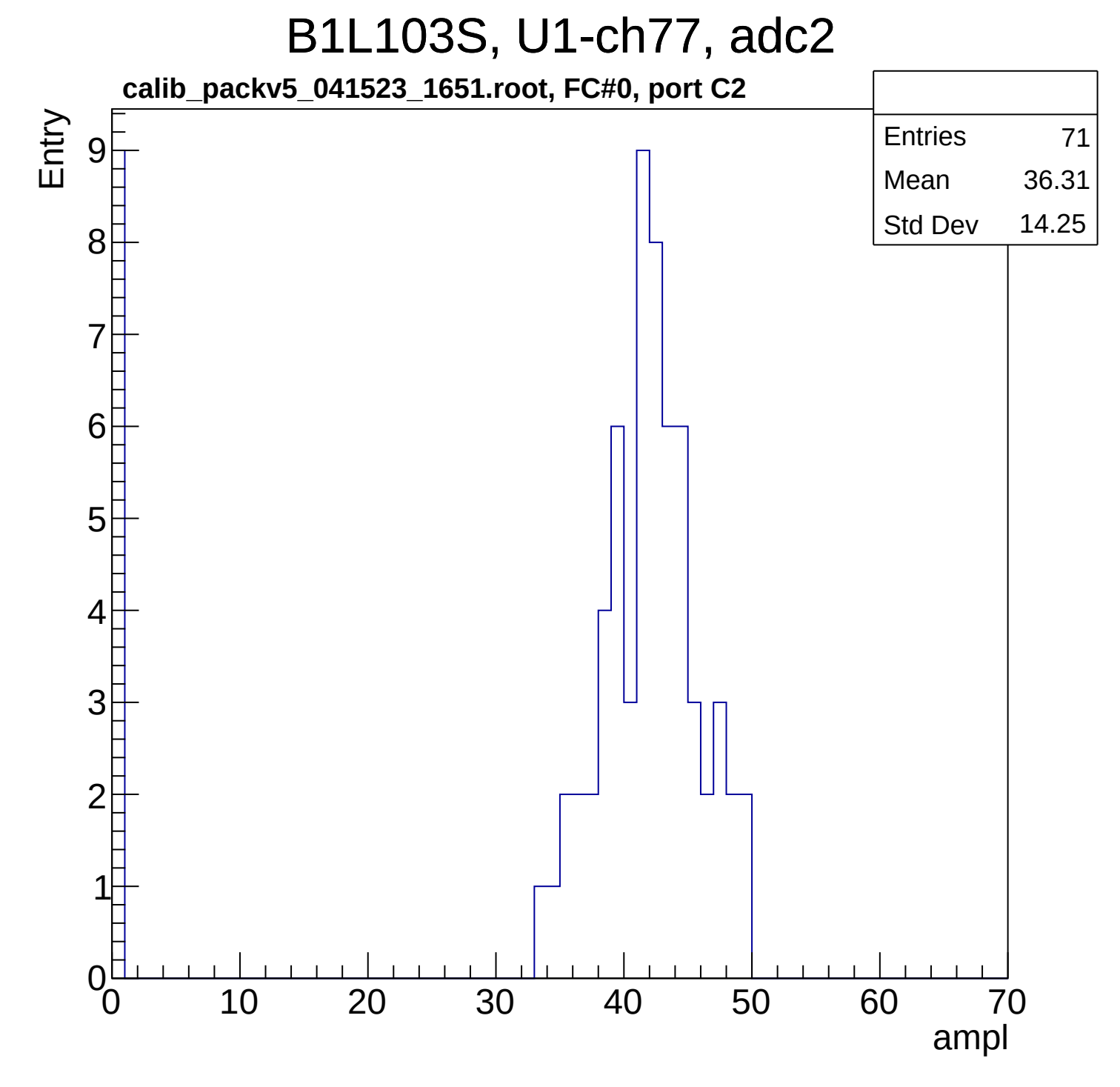

B1L103S, U1-ch77, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 107
Mean 21.67
Std Dev 12.69
Entry
0
5
10
15
20
25
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch77, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 34.51
Std Dev 7.213
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U1-ch77, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 36.31
Std Dev 14.25
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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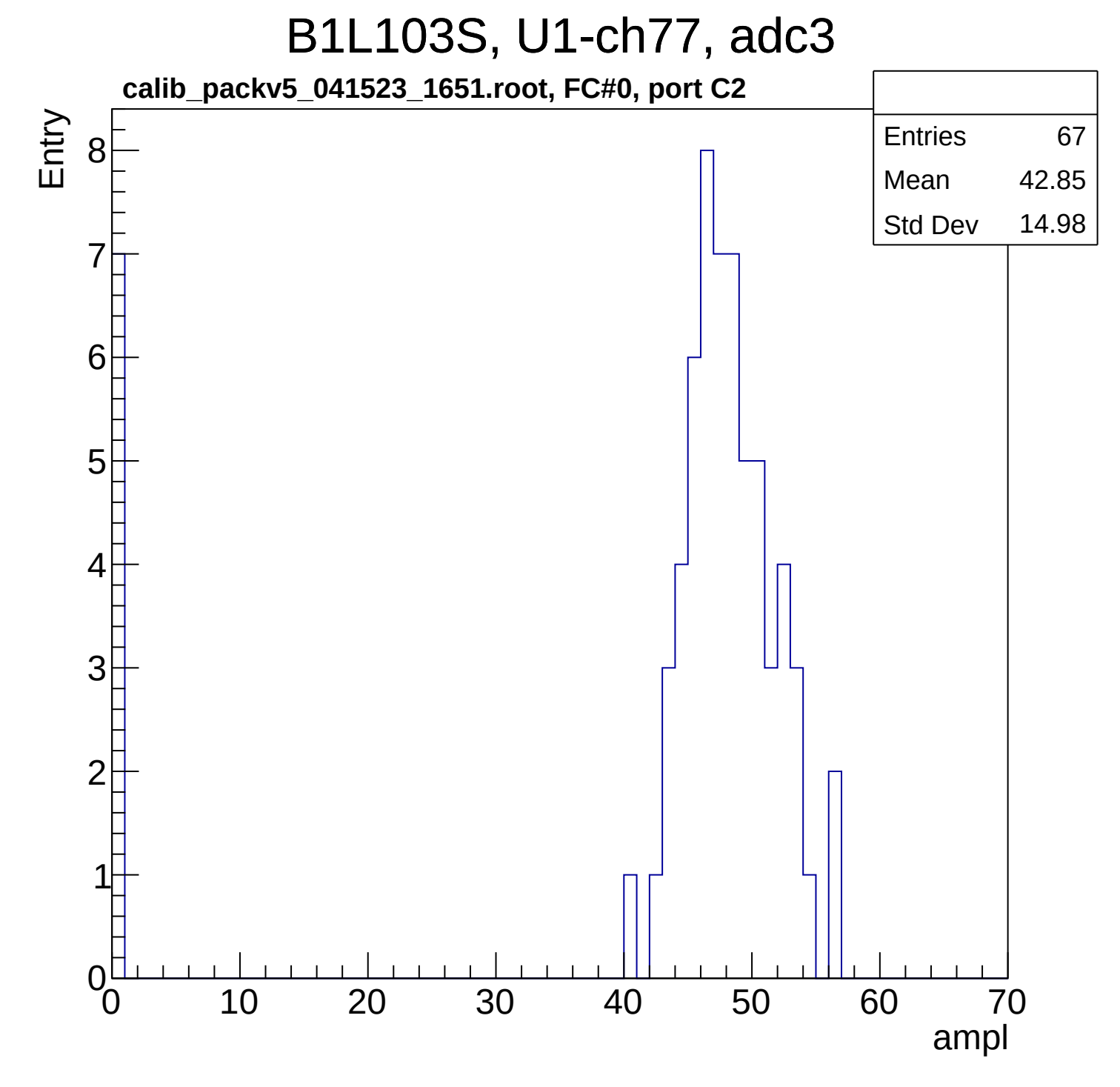
B1L103S, U1-ch77, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 42.85
Std Dev 14.98
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
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40
50
60
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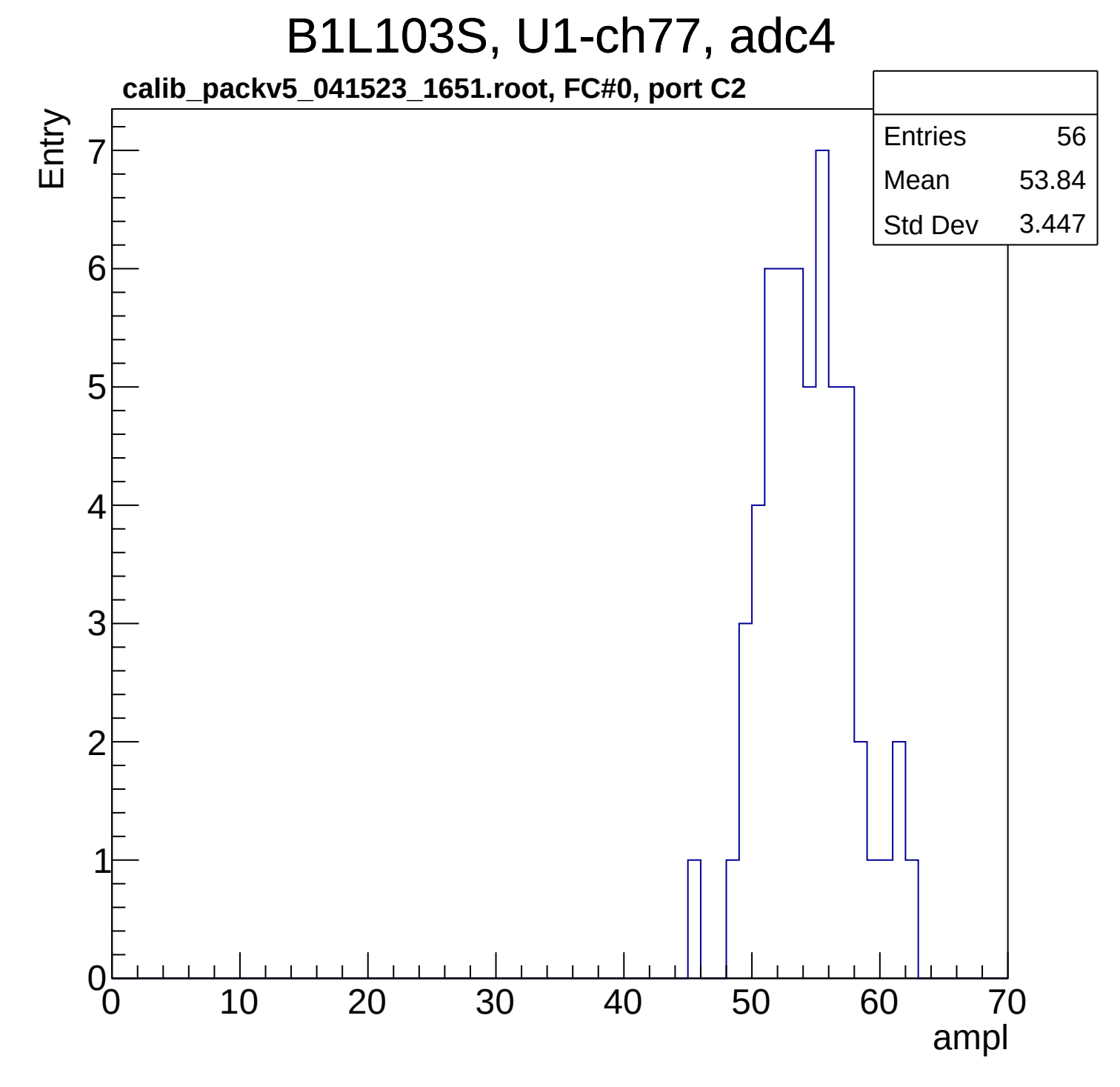
B1L103S, U1-ch77, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 53.84
Std Dev 3.447
Entry
ampl
0
1
2
3
4
5
6
7
0
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20
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40
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60
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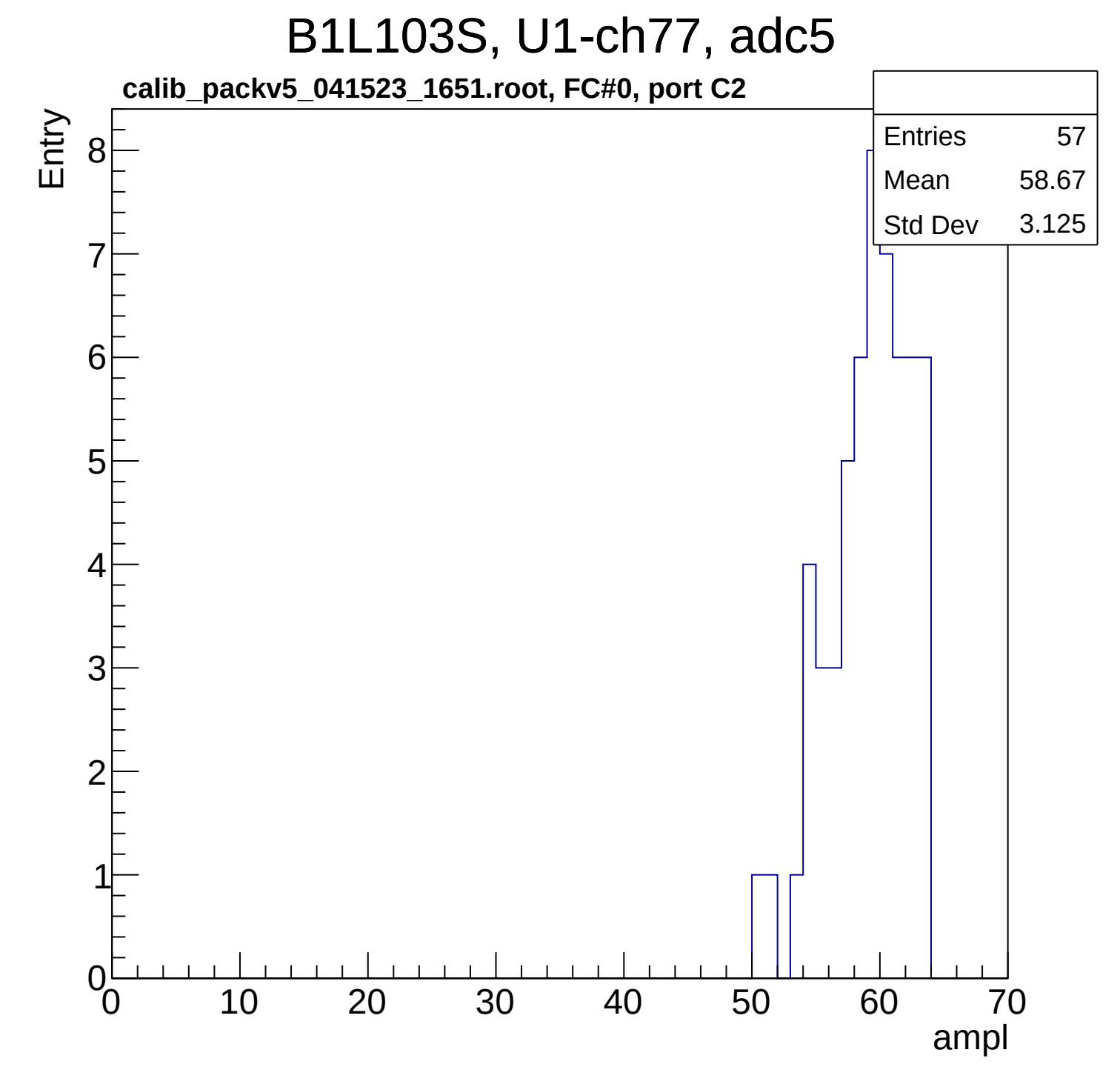
B1L103S, U1-ch77, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 58.67
Std Dev 3.125
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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40
50
60
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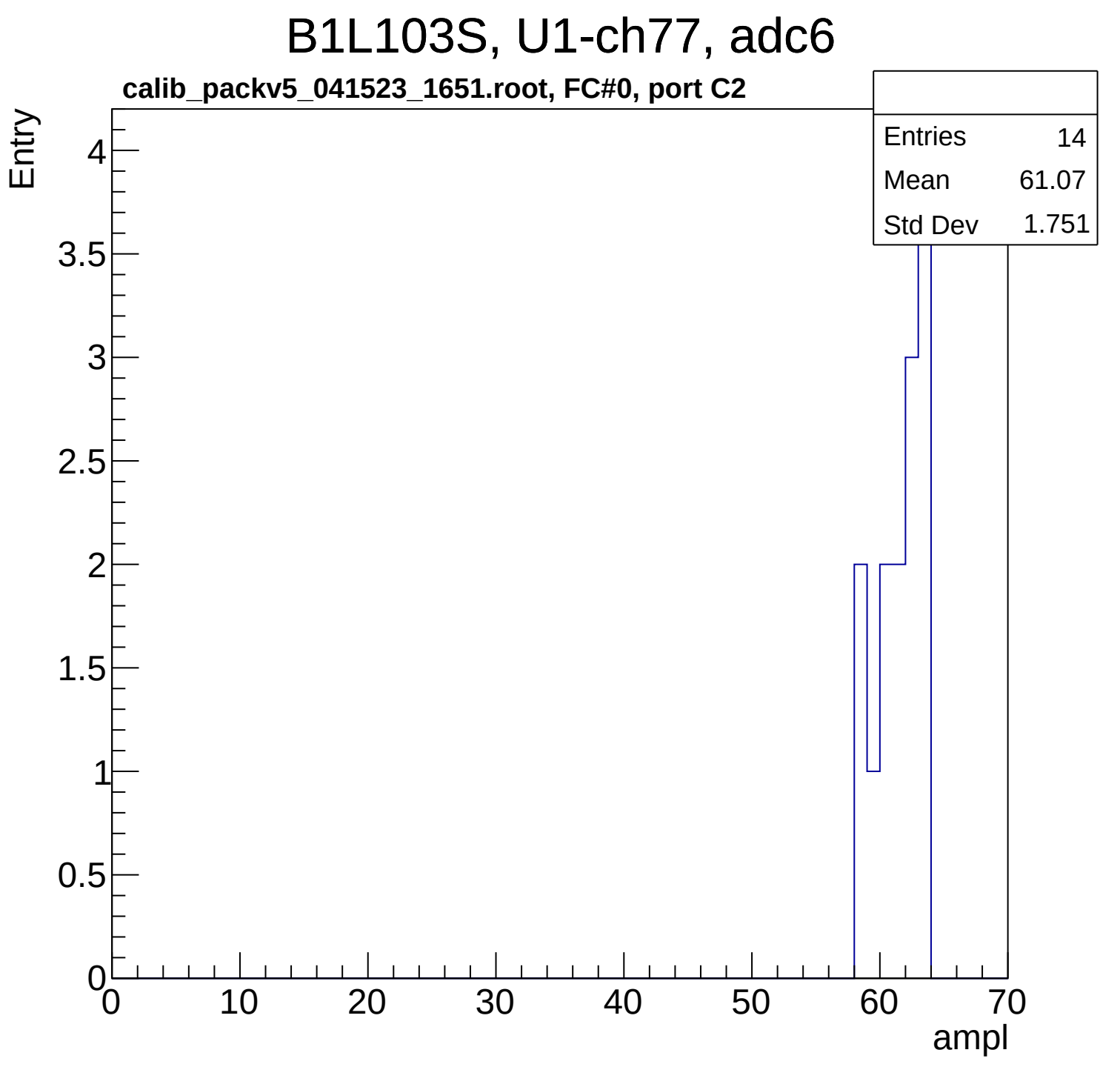
B1L103S, U1-ch77, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 14
Mean 61.07
Std Dev 1.751
Entry
ampl
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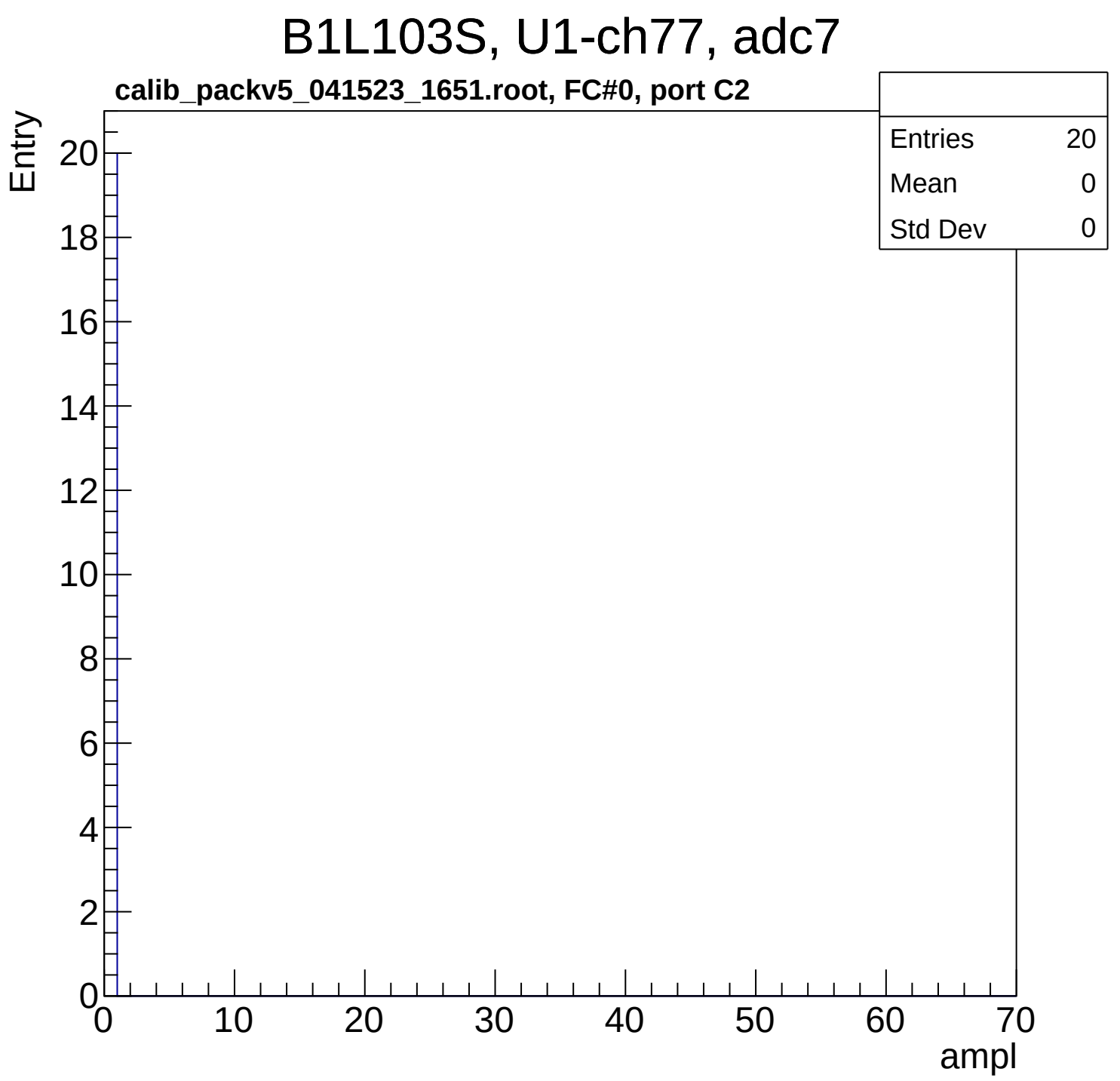
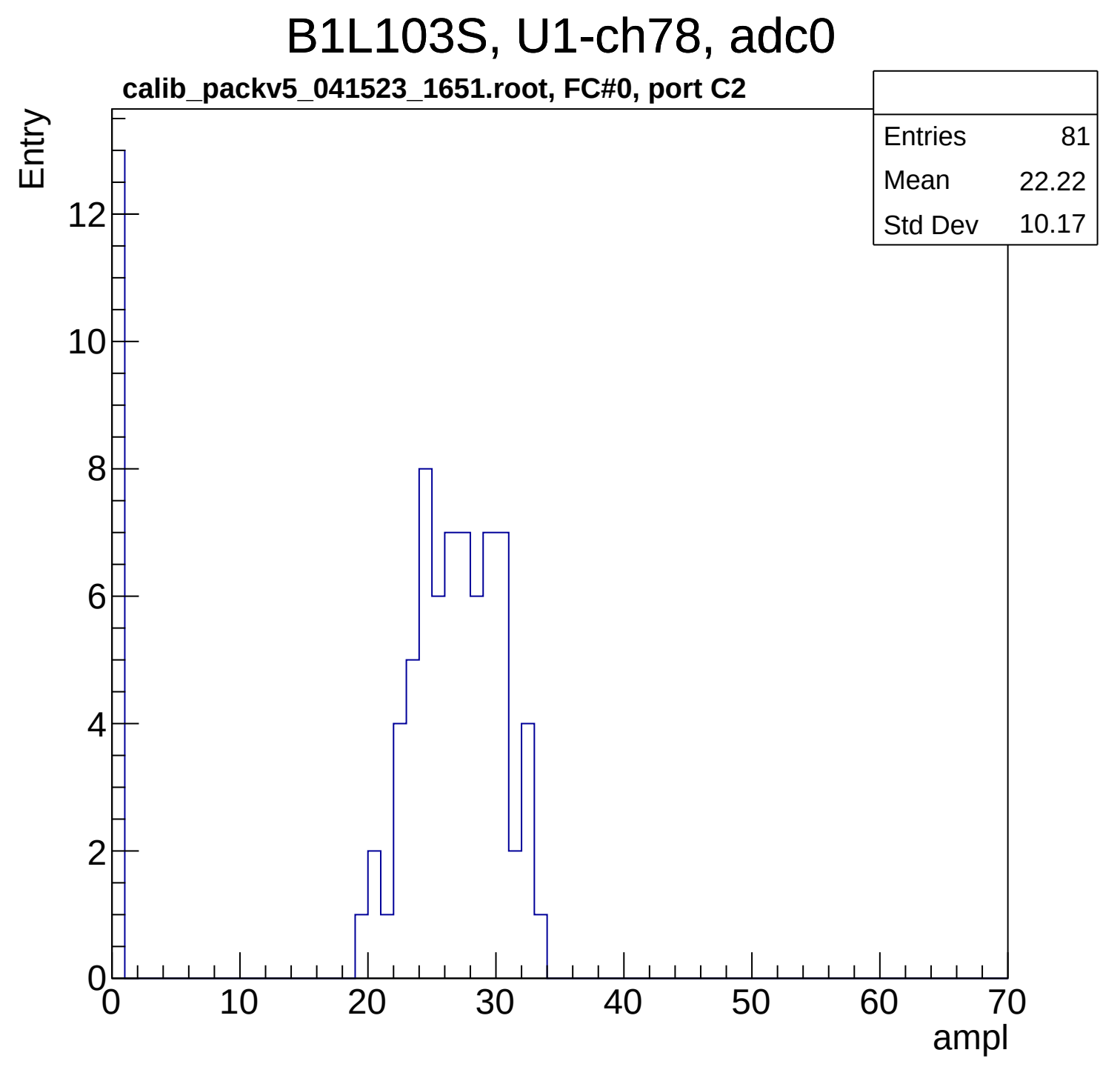
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U1-ch77, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch78, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 22.22
Std Dev 10.17
Entry
ampl
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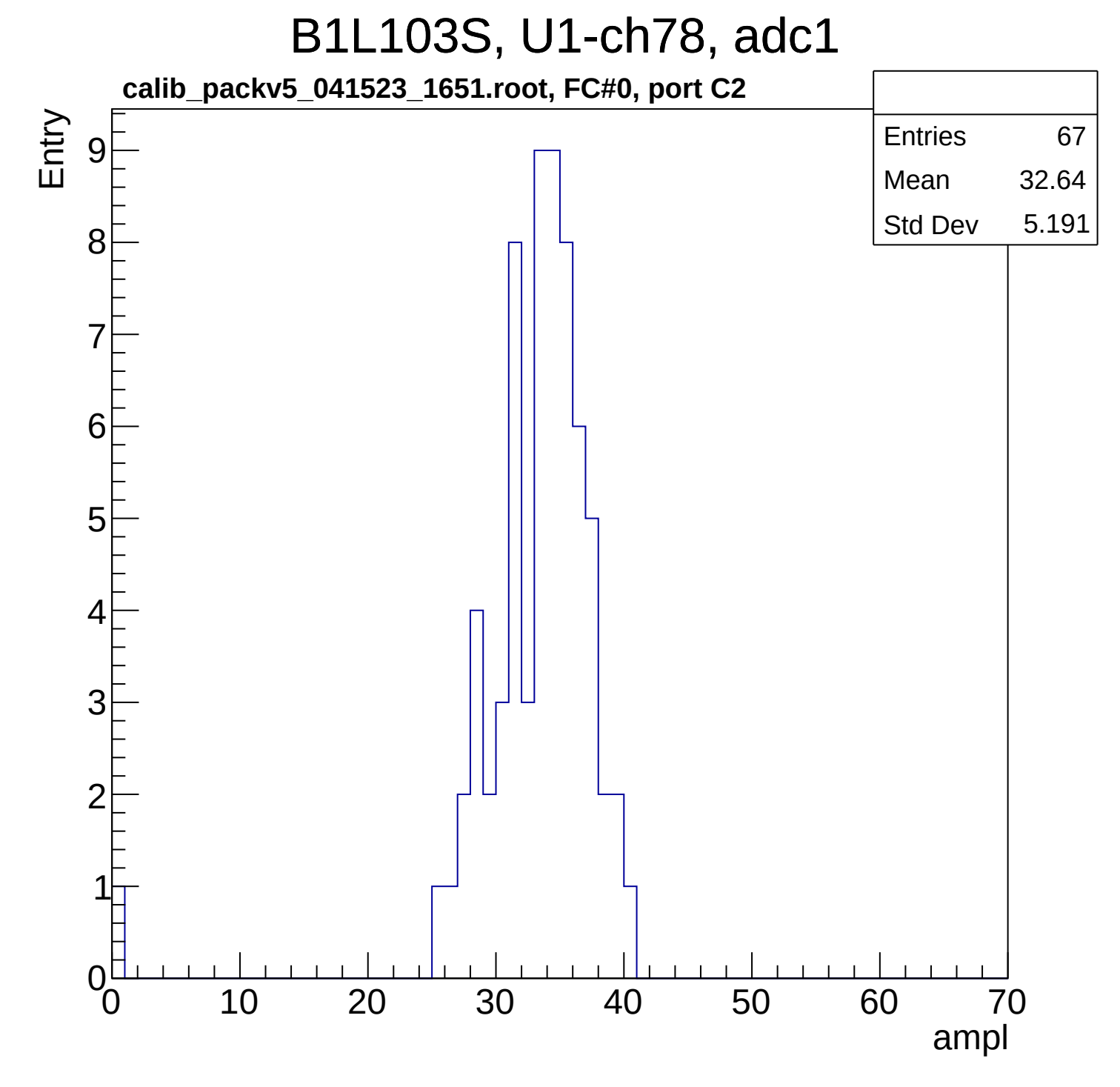
2
4
6
8
10
12
0
10
20
30
40
50
60
70


B1L103S, U1-ch78, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 32.64
Std Dev 5.191
Entry
ampl
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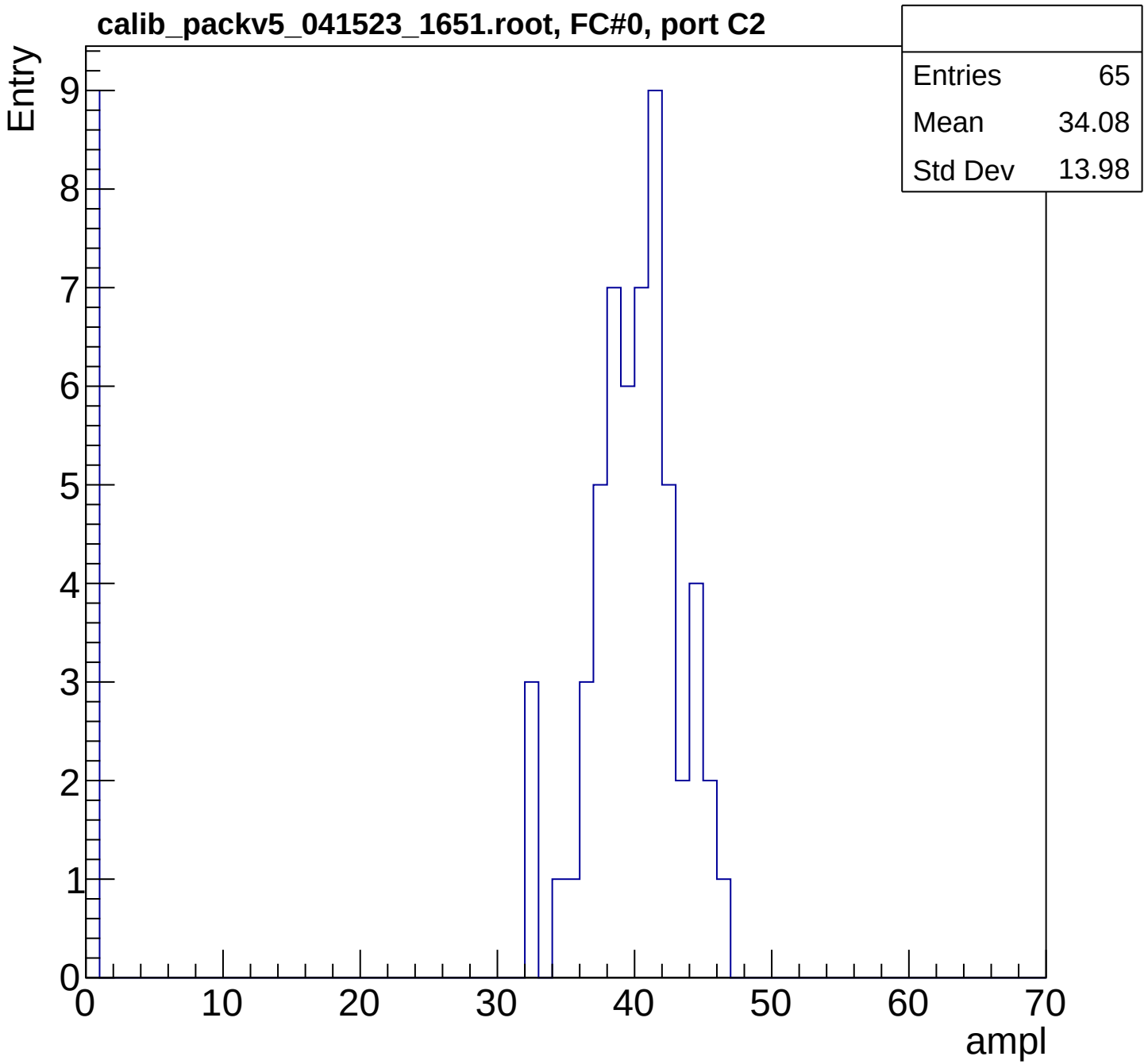
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U1-ch78, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 34.08
Std Dev 13.98
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
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20
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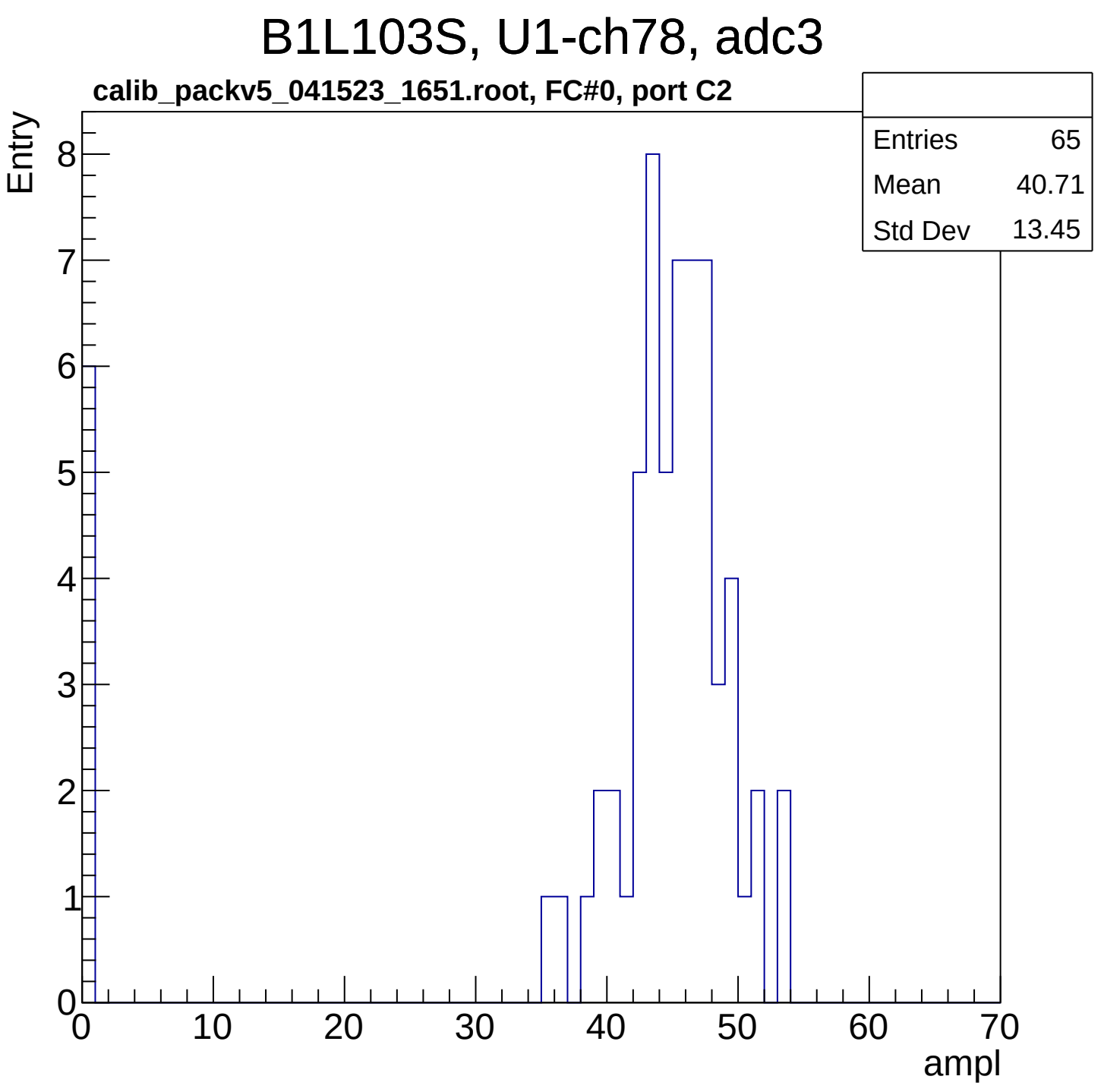
40
50
60
70


B1L103S, U1-ch78, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 40.71
Std Dev 13.45
Entry
ampl
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1
2
3
4
5
6
7
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0
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60
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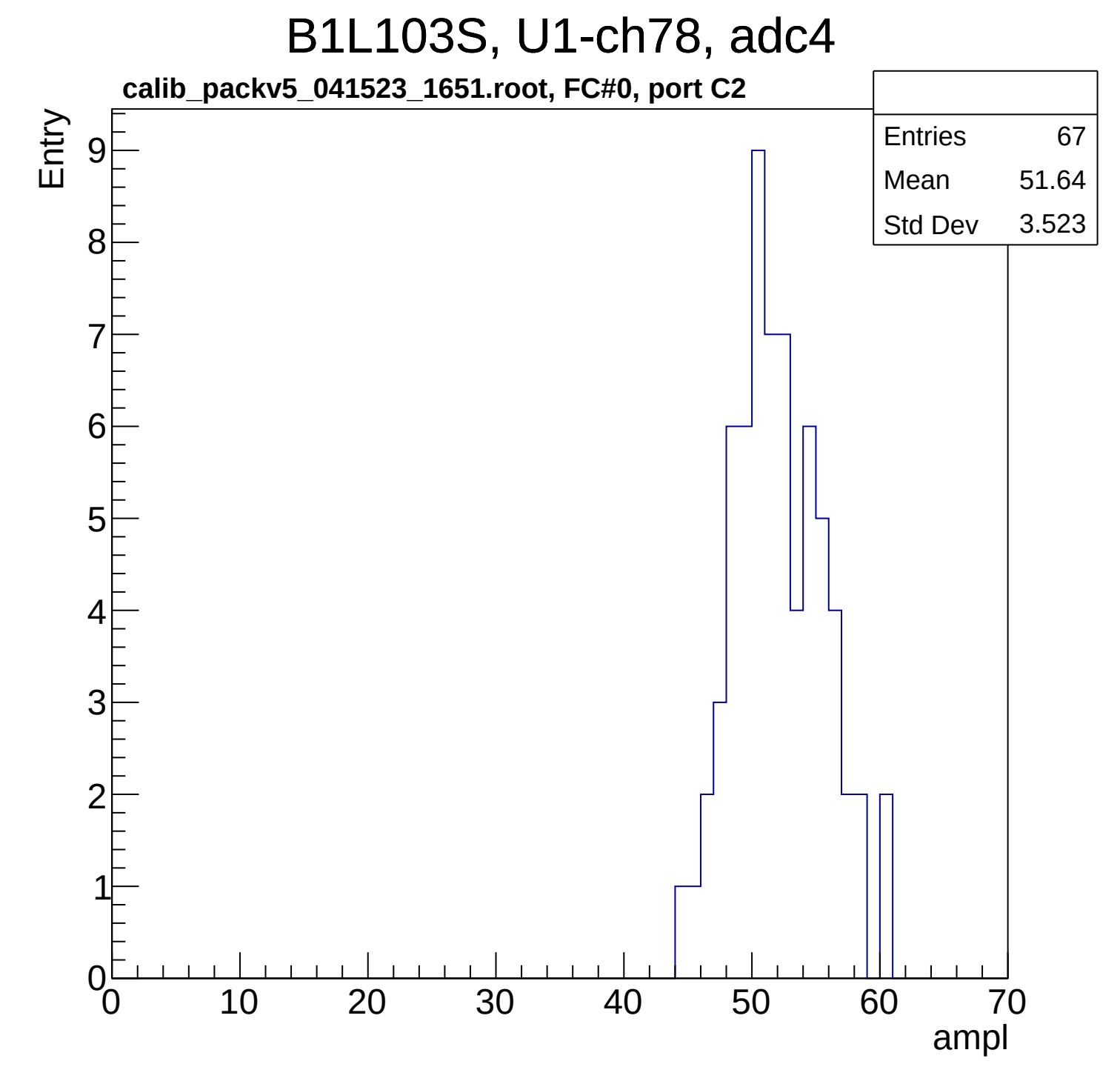
B1L103S, U1-ch78, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 51.64
Std Dev 3.523
Entry
ampl
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3
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5
6
7
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0
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60
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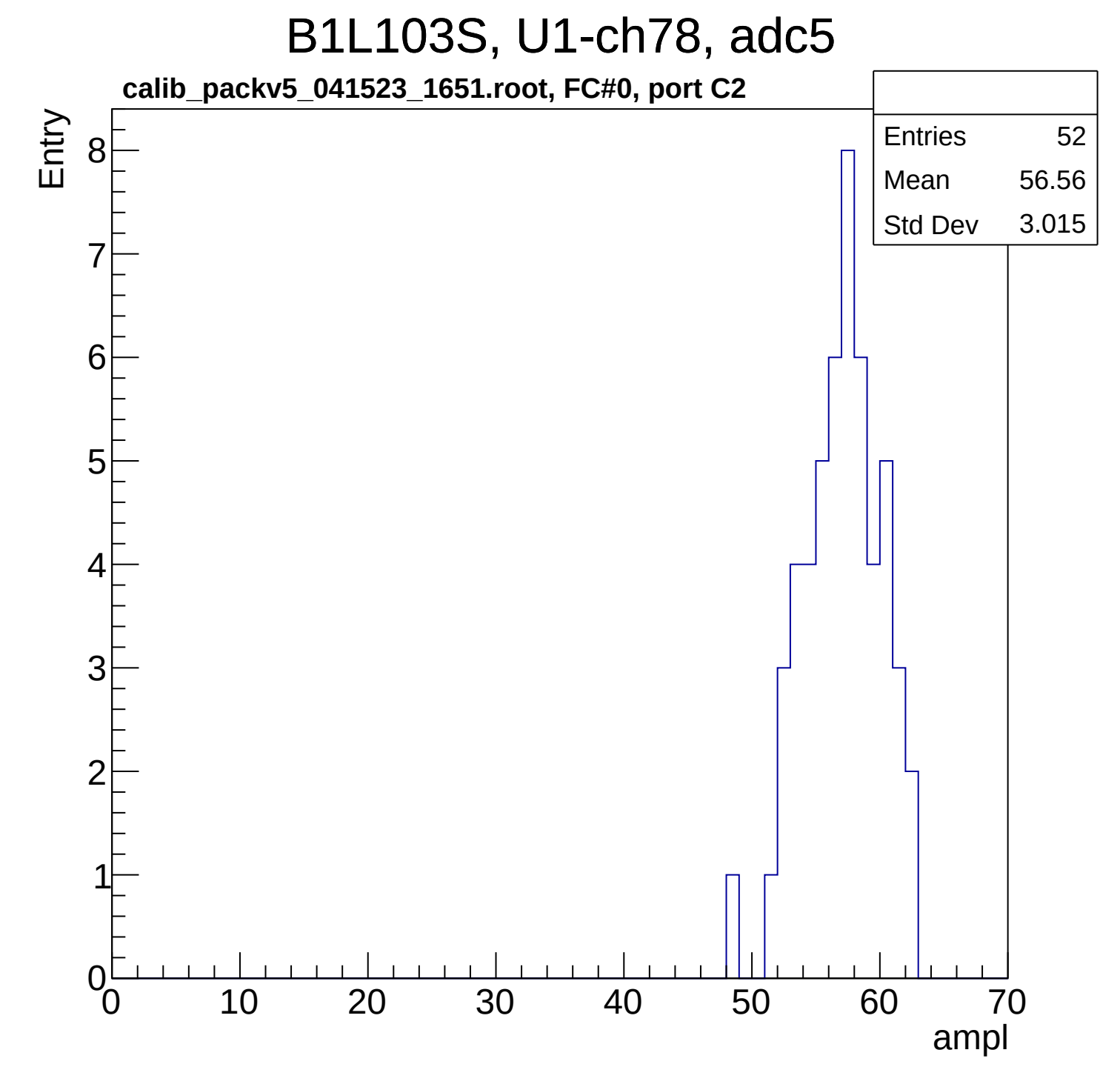
B1L103S, U1-ch78, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 56.56
Std Dev 3.015
Entry
ampl
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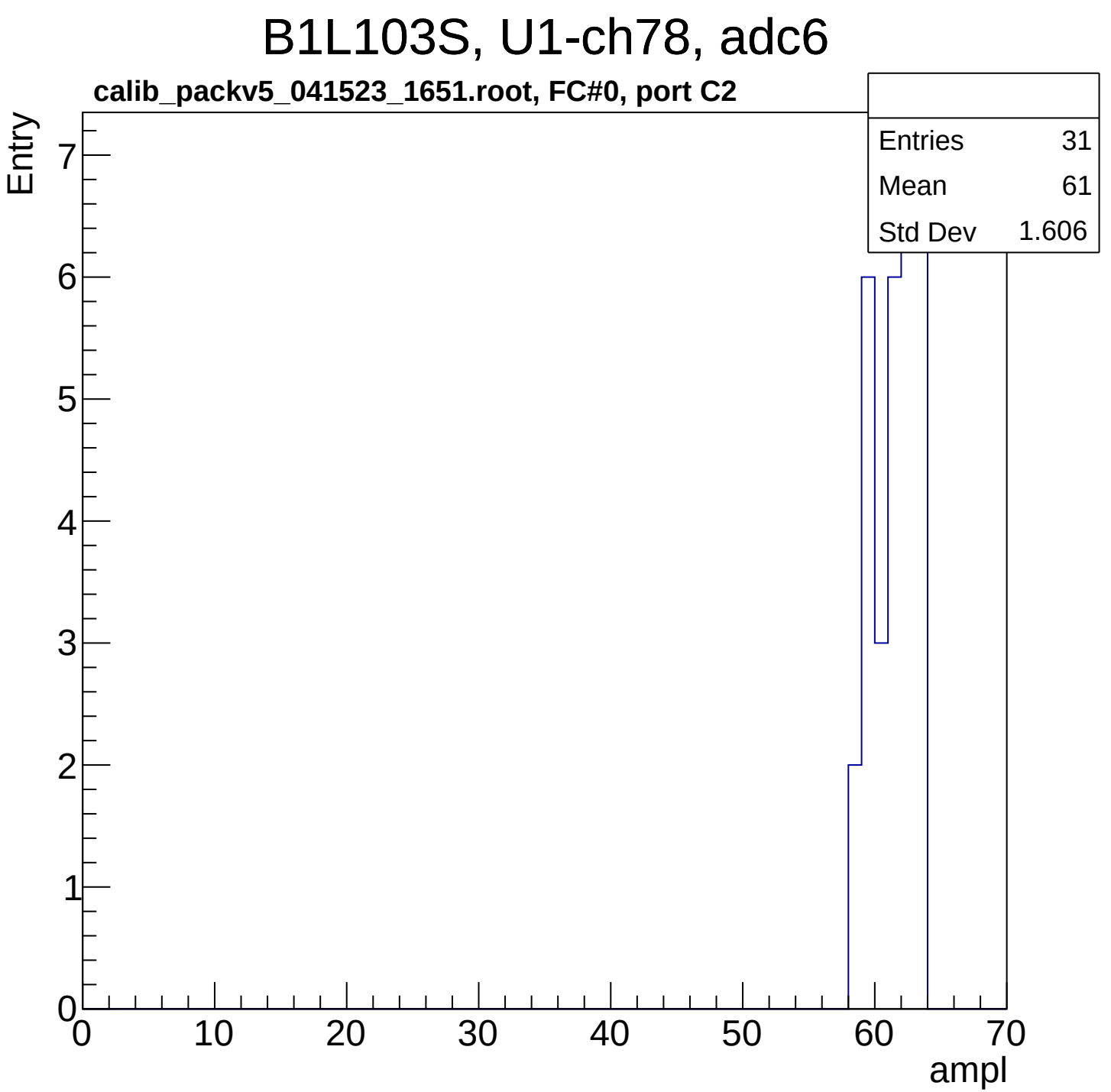
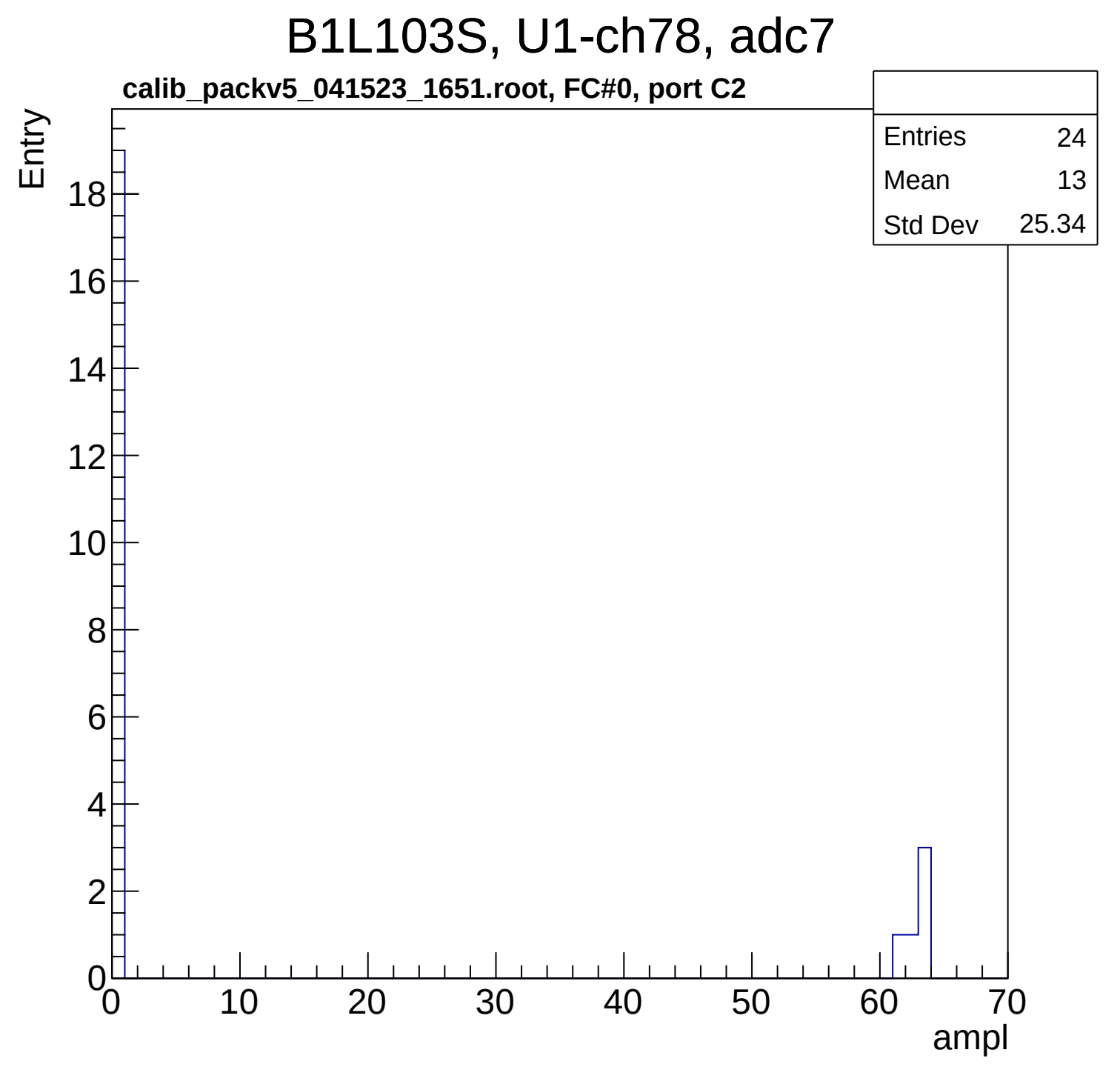
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U1-ch78, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 31
Mean 61
Std Dev 1.606
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U1-ch78, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 24
Mean 13
Std Dev 25.34
Entry
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10
12
14
16
18
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10
20
30
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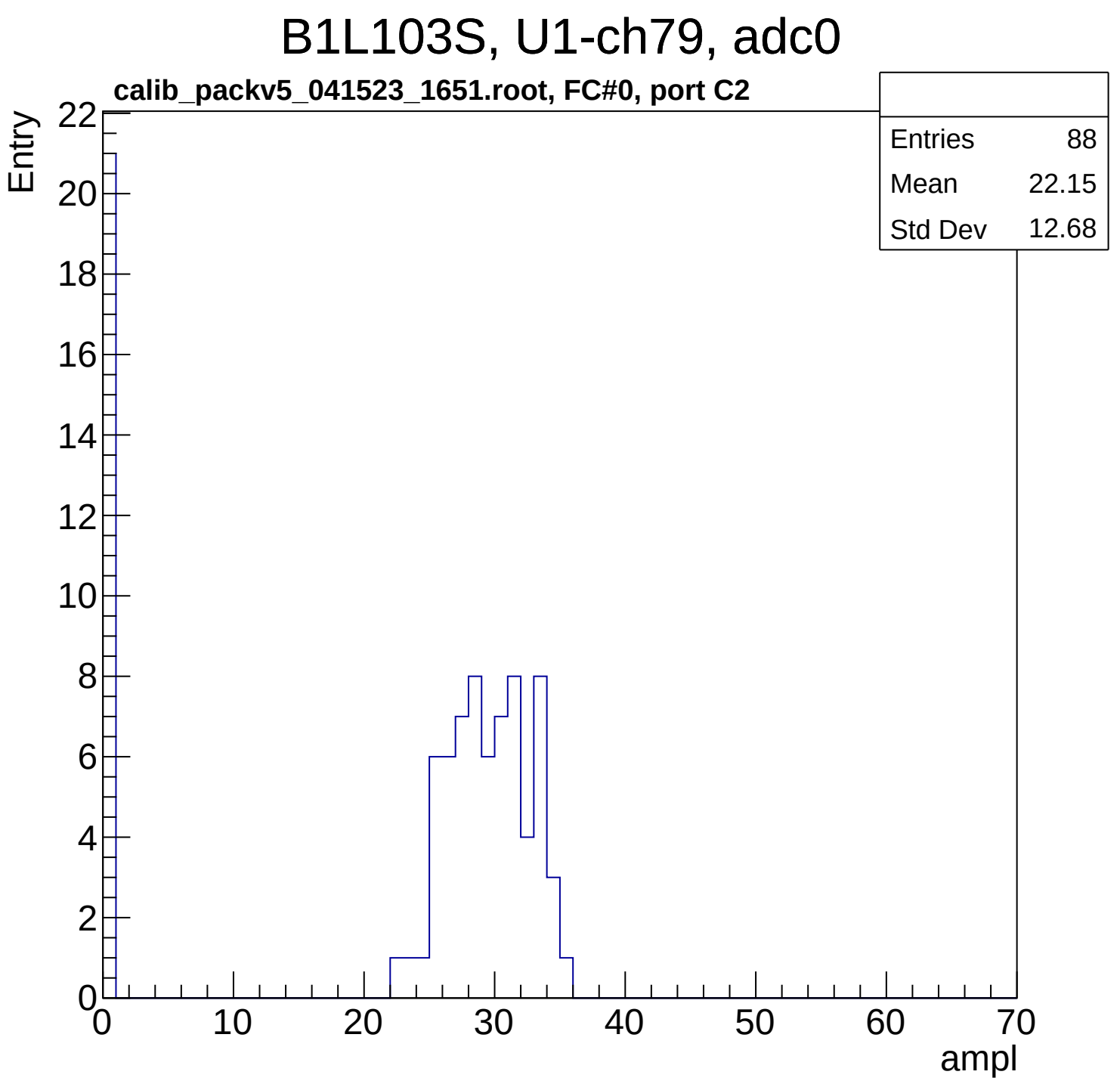
50
60
70
ampl


B1L103S, U1-ch79, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 88
Mean 22.15
Std Dev 12.68
Entry
ampl
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10
12
14
16
18
20
22
0
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40
50
60
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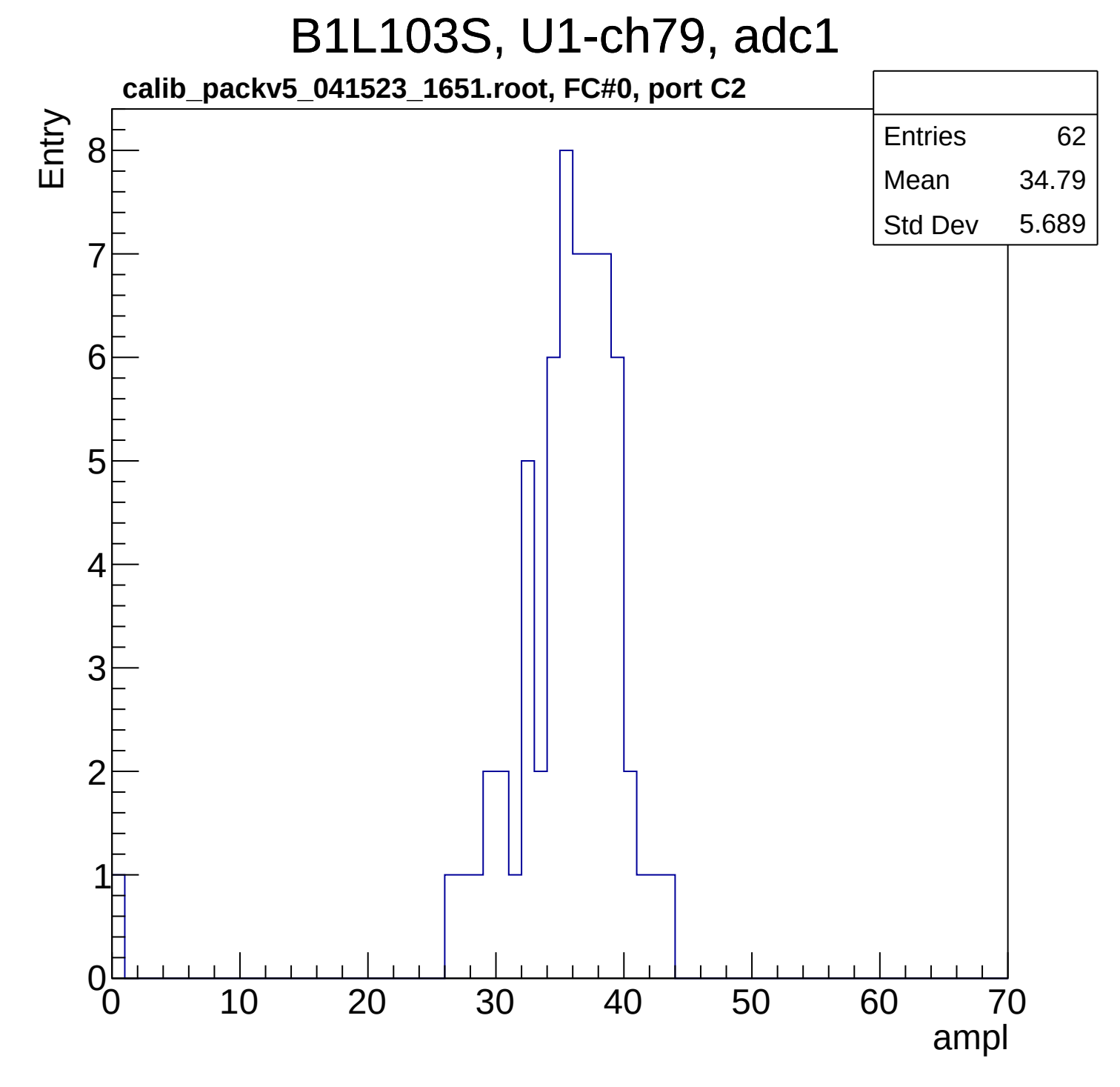
B1L103S, U1-ch79, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 34.79
Std Dev 5.689
Entry
ampl
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4
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6
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60
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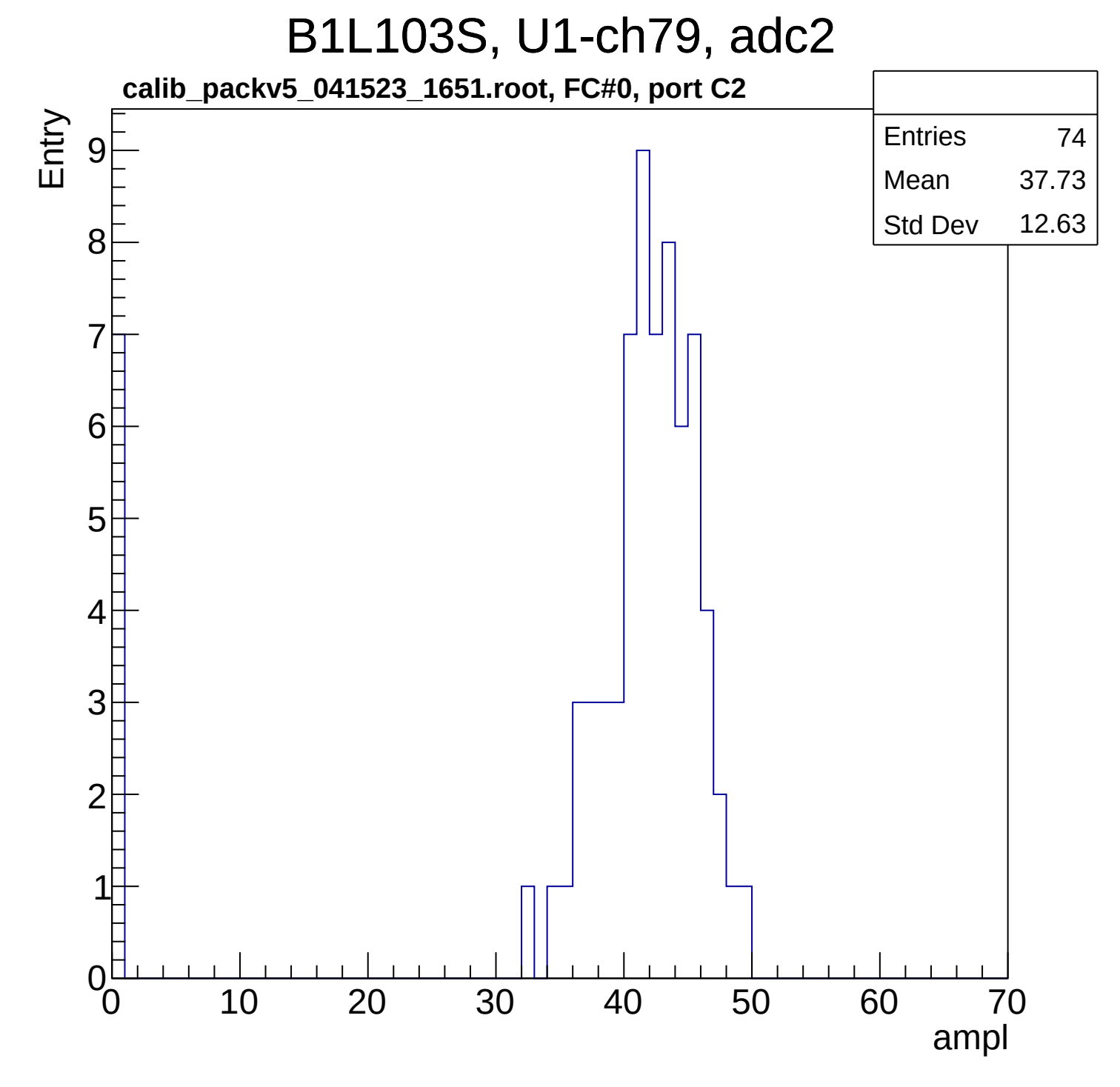
B1L103S, U1-ch79, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 37.73
Std Dev 12.63
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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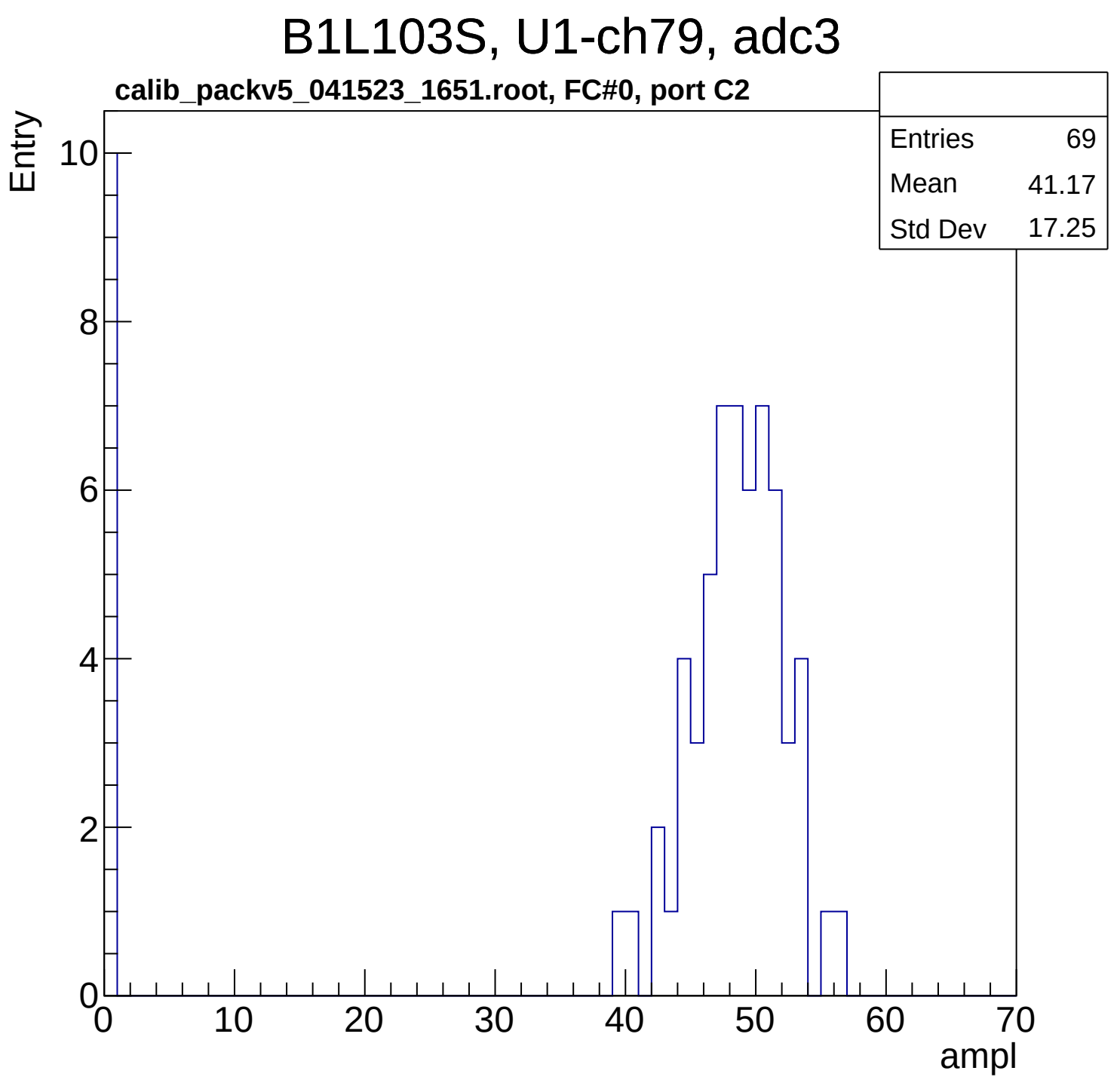
40
50
60
70


B1L103S, U1-ch79, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 41.17
Std Dev 17.25
Entry
ampl
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4
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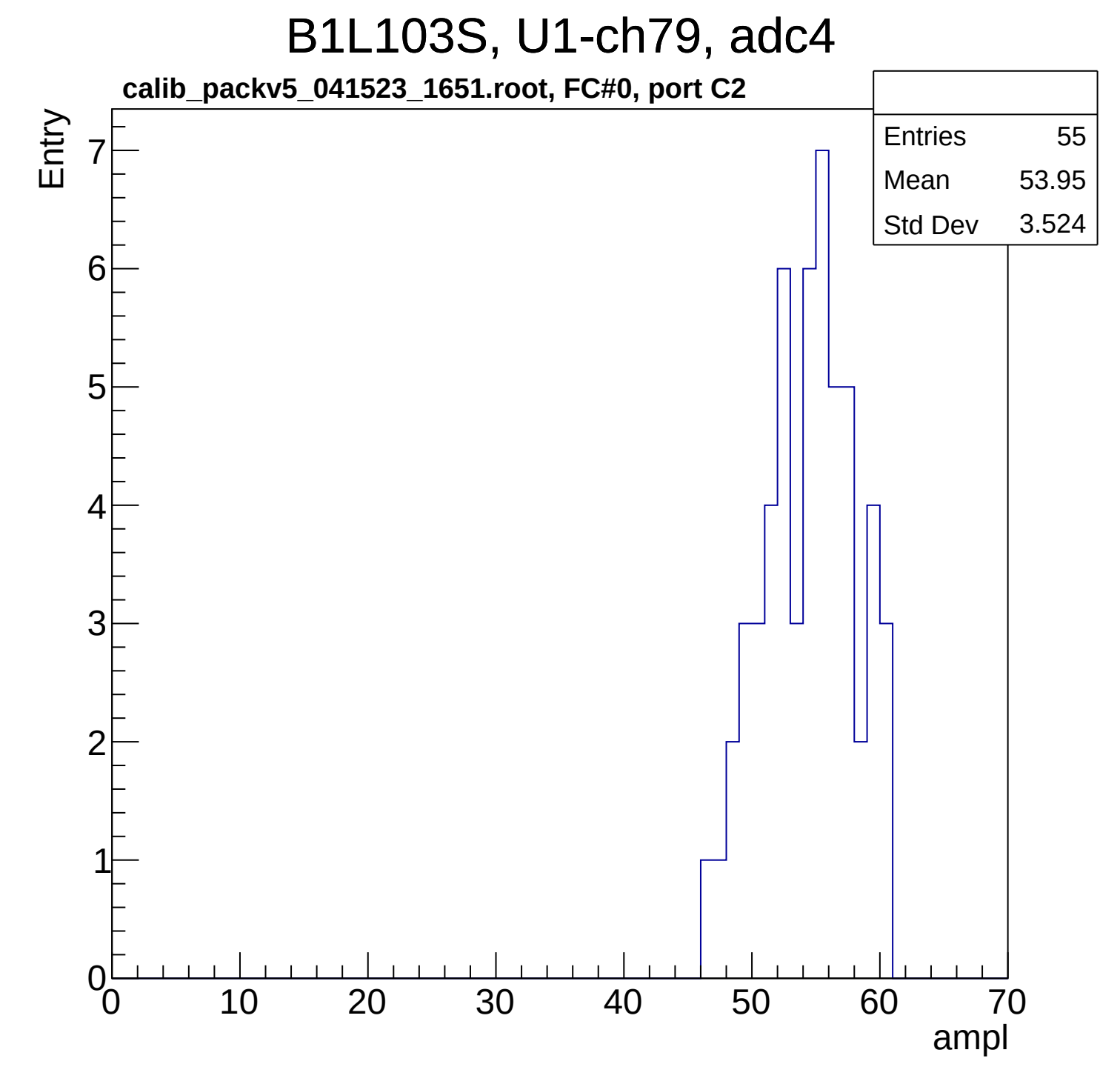
8
10
0
10
20
30
40
50
60
70


B1L103S, U1-ch79, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 53.95
Std Dev 3.524
Entry
ampl
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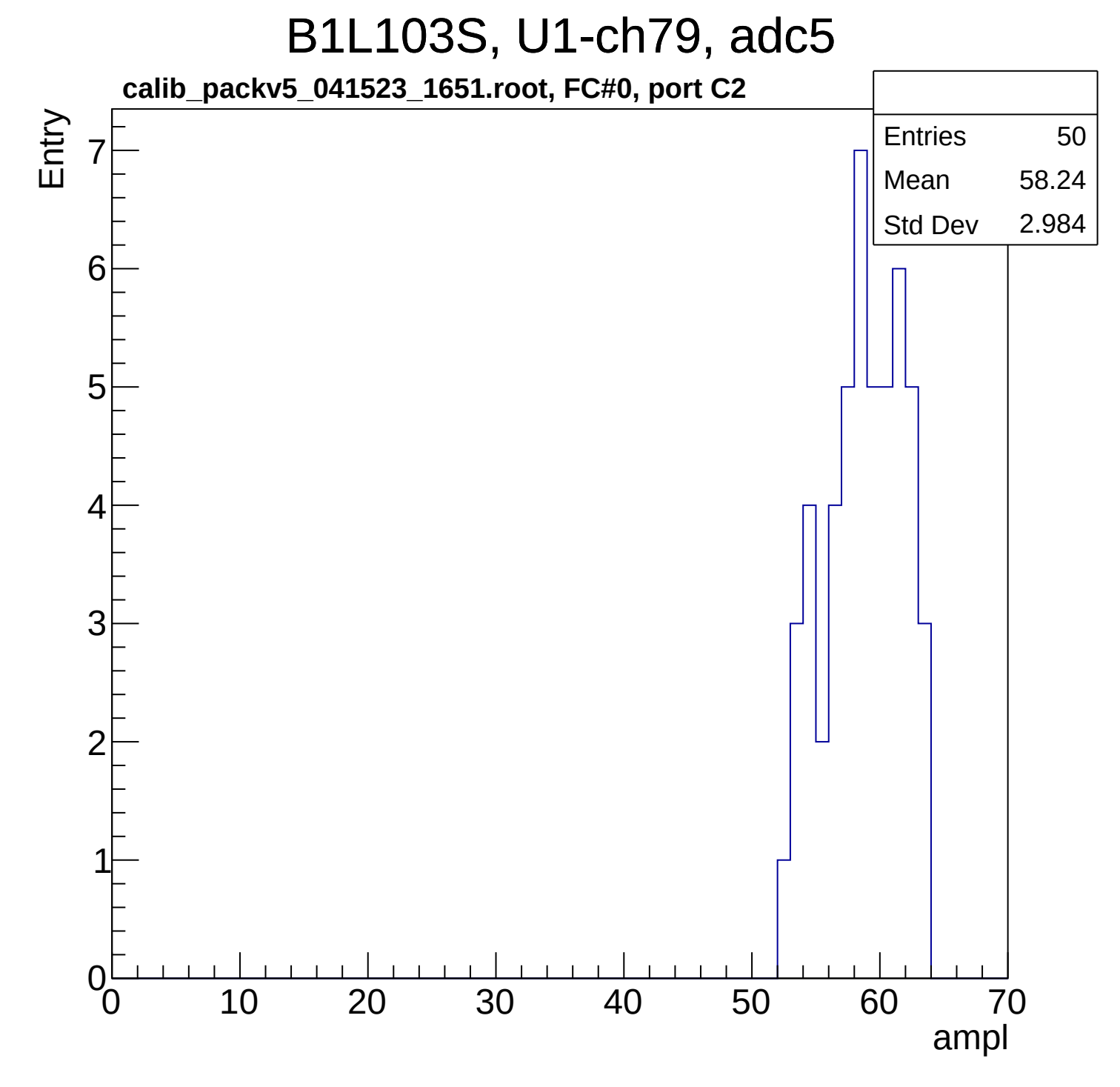
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U1-ch79, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 58.24
Std Dev 2.984
Entry
ampl
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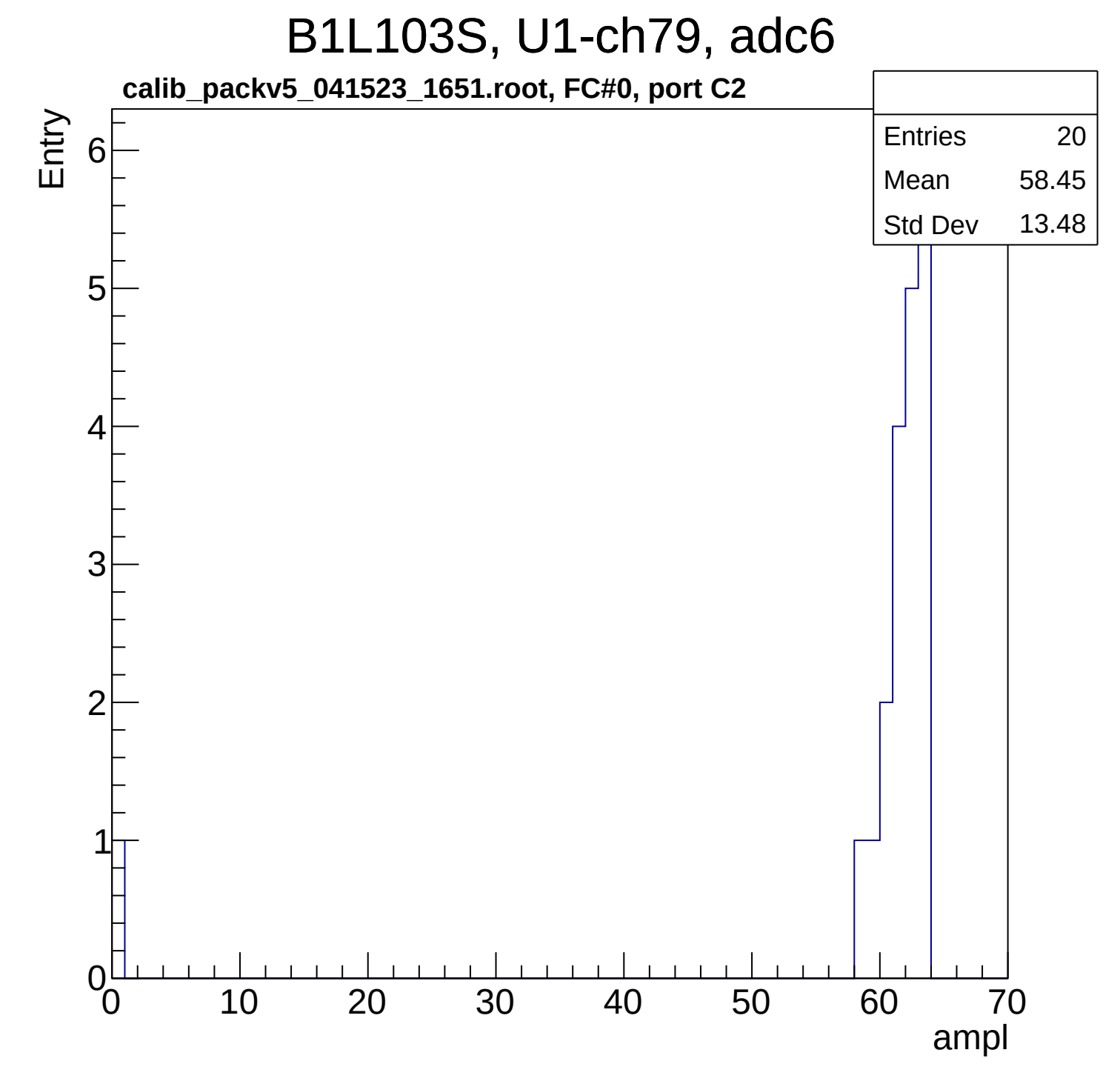
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U1-ch79, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 58.45
Std Dev 13.48
Entry
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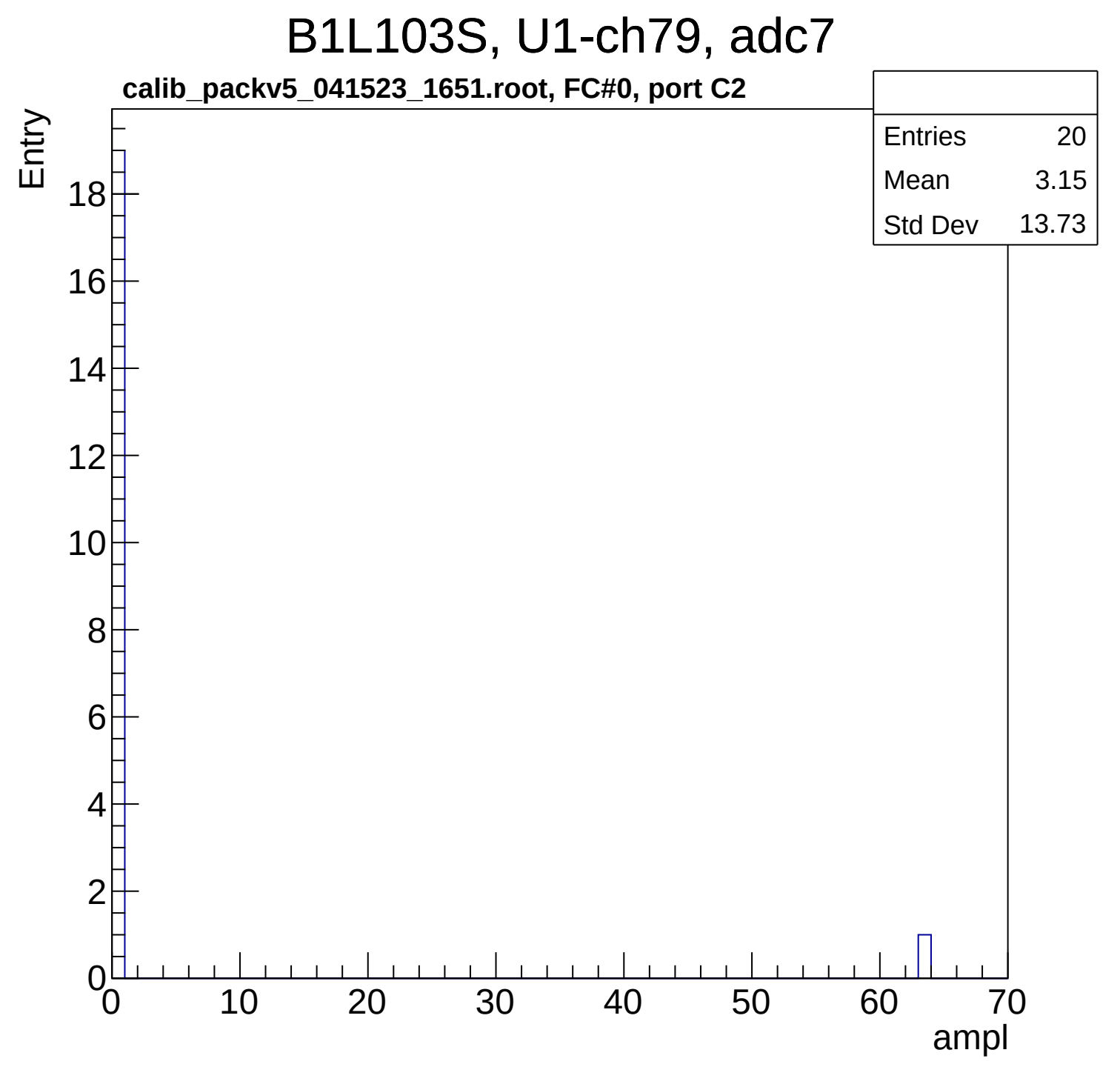
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch79, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
0
2
4
6
8
10
12
14
16
18
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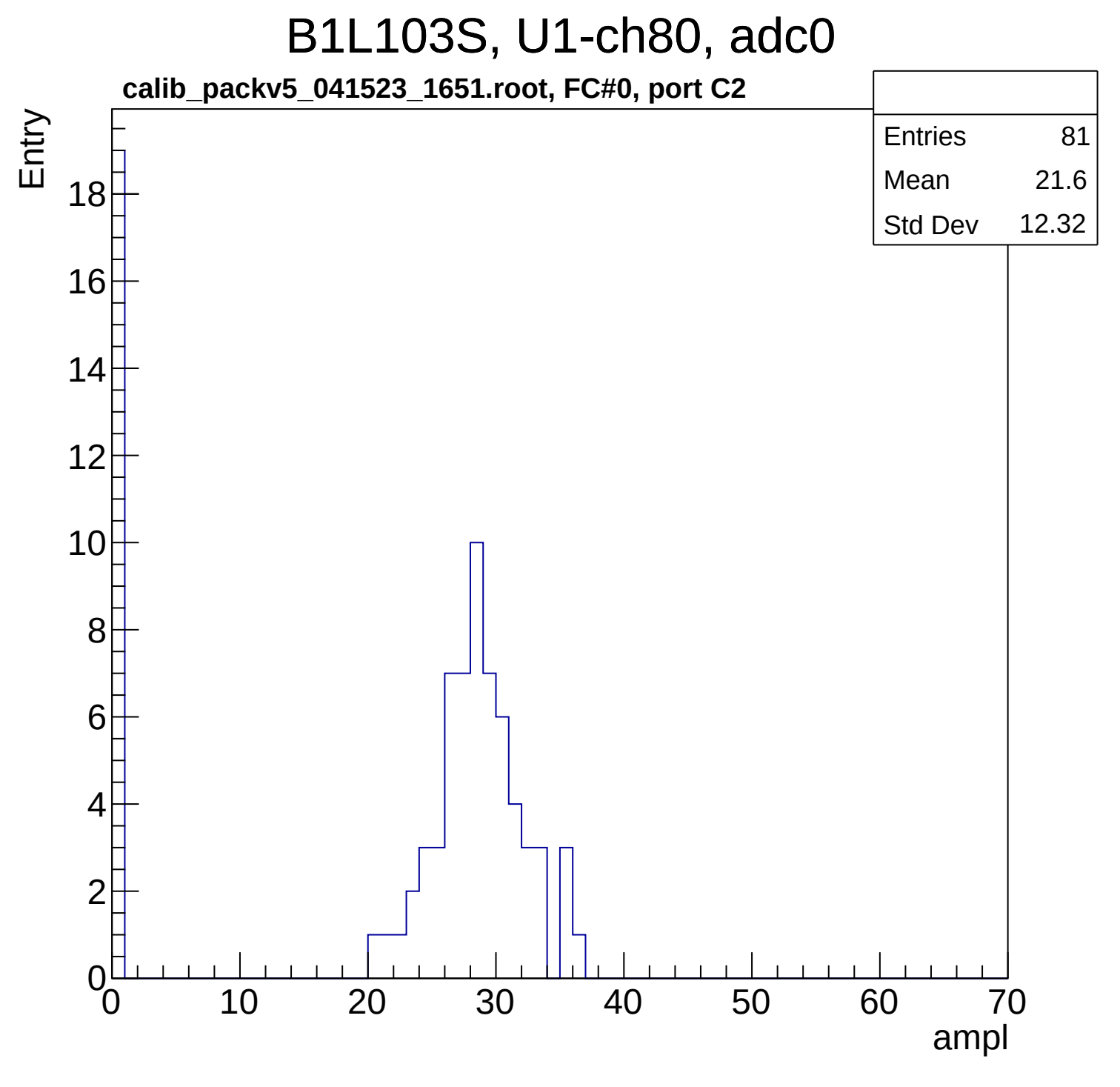
60
70
ampl


B1L103S, U1-ch80, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 21.6
Std Dev 12.32
Entry
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6
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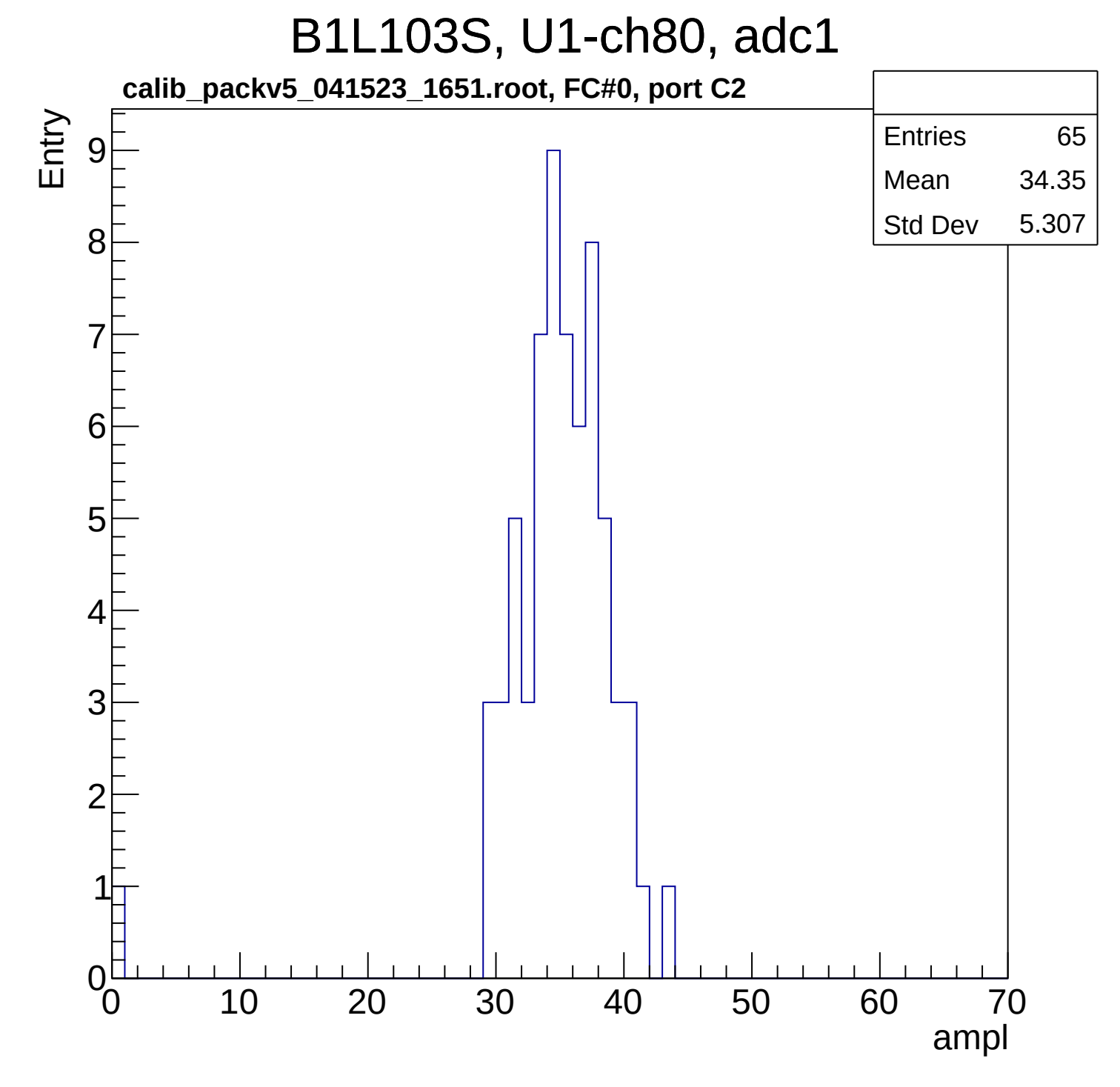
ampl


B1L103S, U1-ch80, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 34.35
Std Dev 5.307
Entry
ampl
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2
3
4
5
6
7
8
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0
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40
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60
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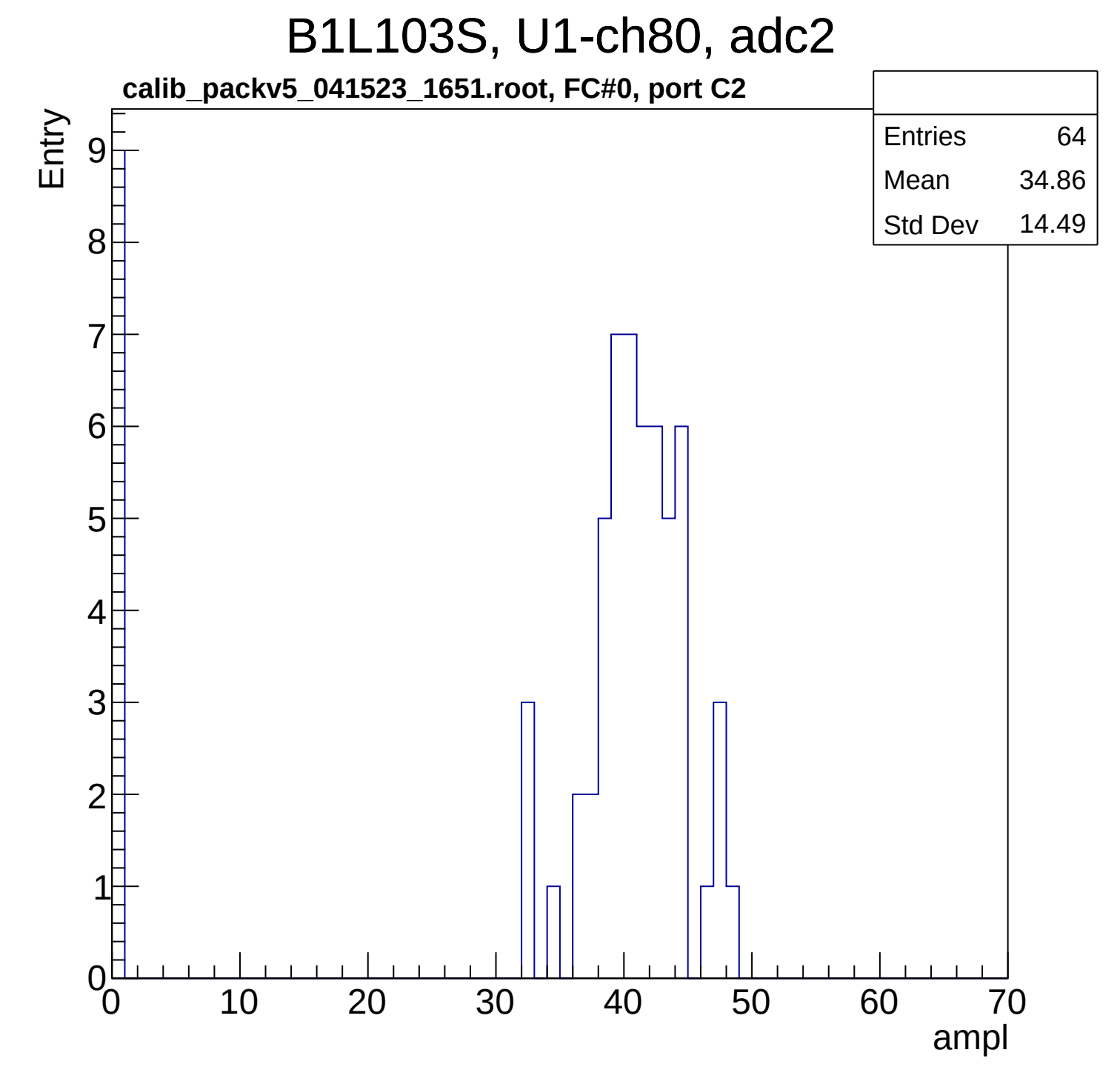
B1L103S, U1-ch80, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 34.86
Std Dev 14.49
Entry
ampl
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3
4
5
6
7
8
9
0
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60
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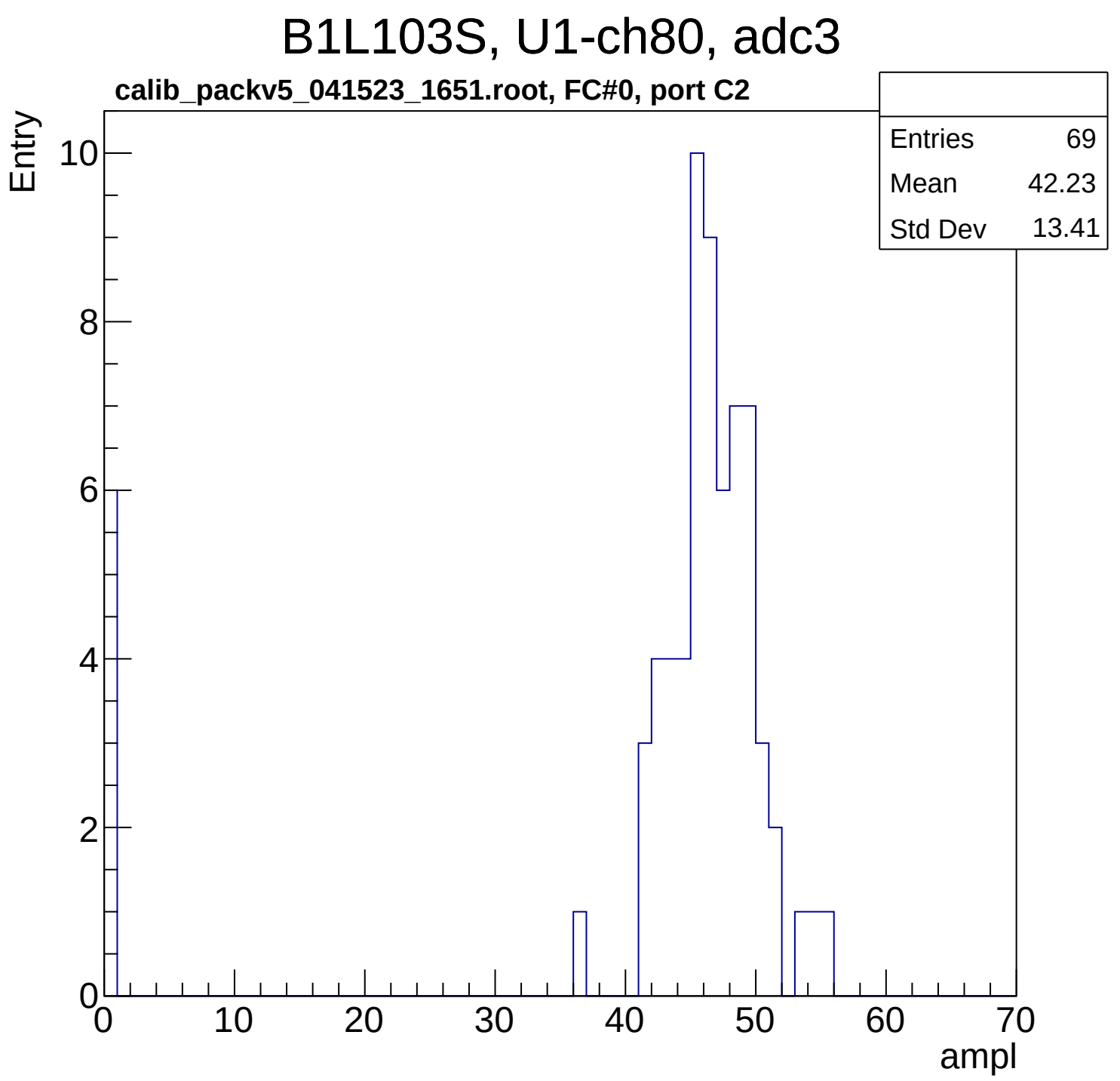
B1L103S, U1-ch80, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 42.23
Std Dev 13.41
Entry
ampl
0
2
4
6
8
10
0
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20
30
40
50
60
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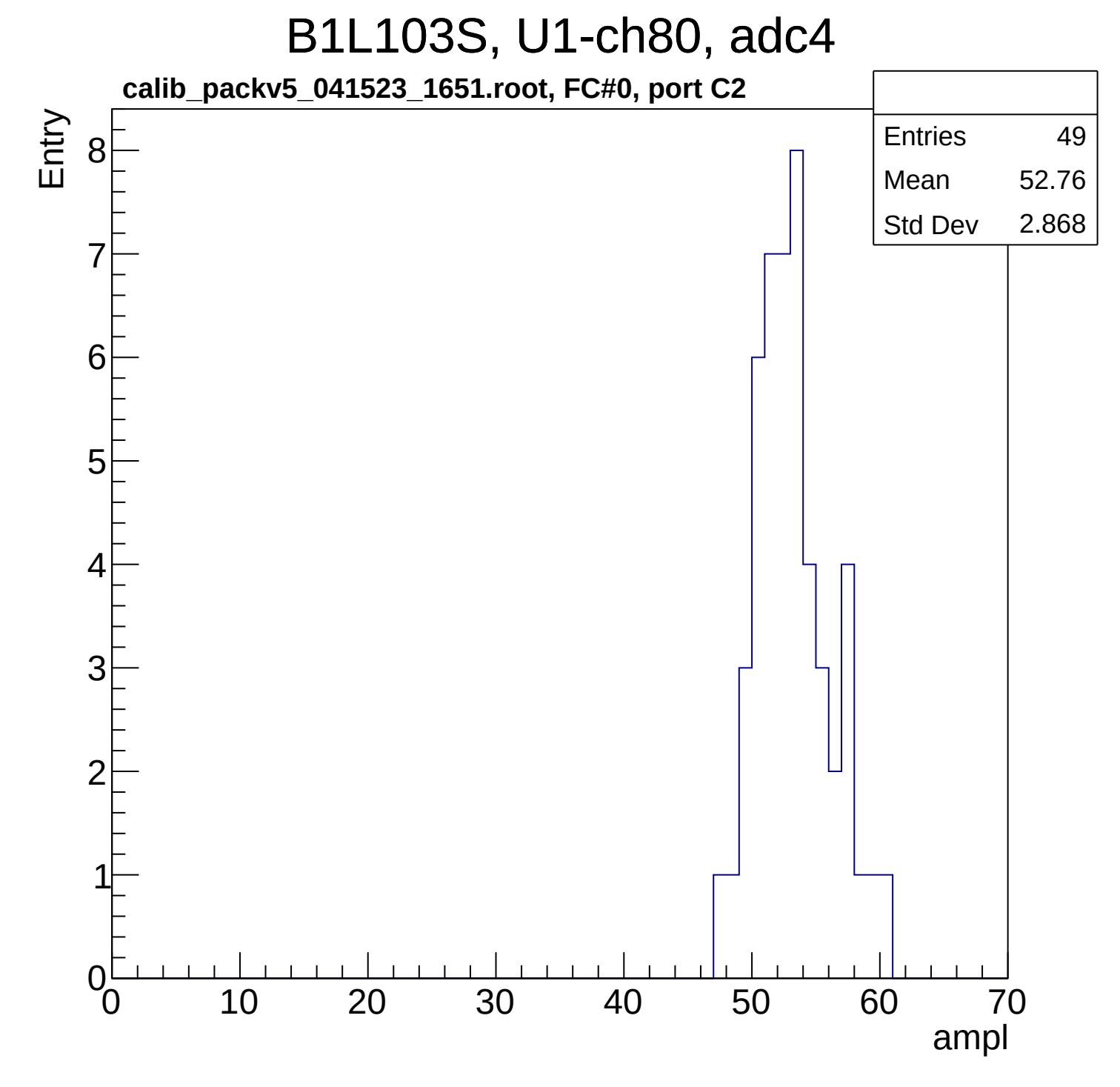
B1L103S, U1-ch80, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 52.76
Std Dev 2.868
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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40
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60
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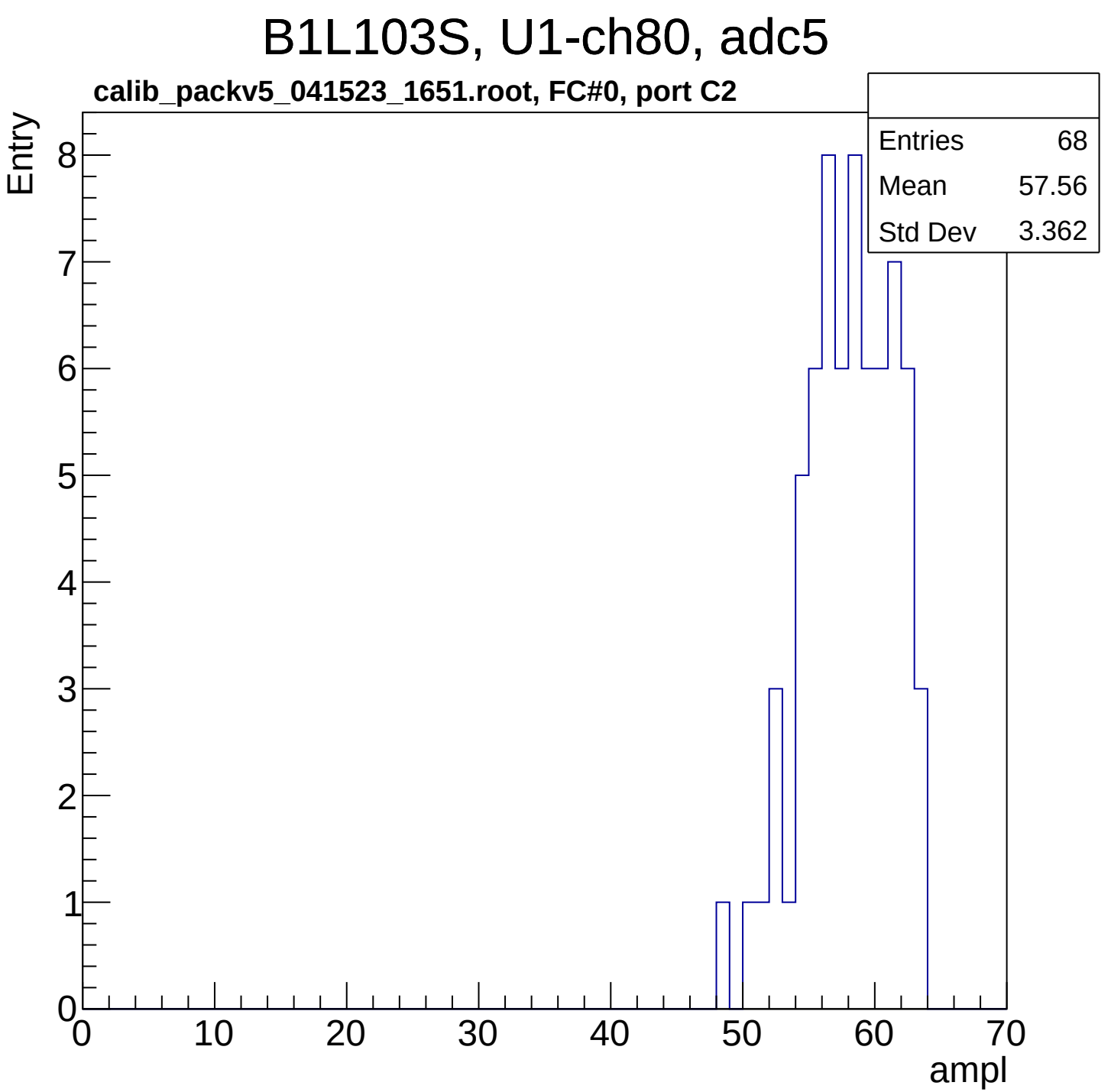
B1L103S, U1-ch80, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 57.56
Std Dev 3.362
Entry
ampl
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2
3
4
5
6
7
8
0
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40
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60
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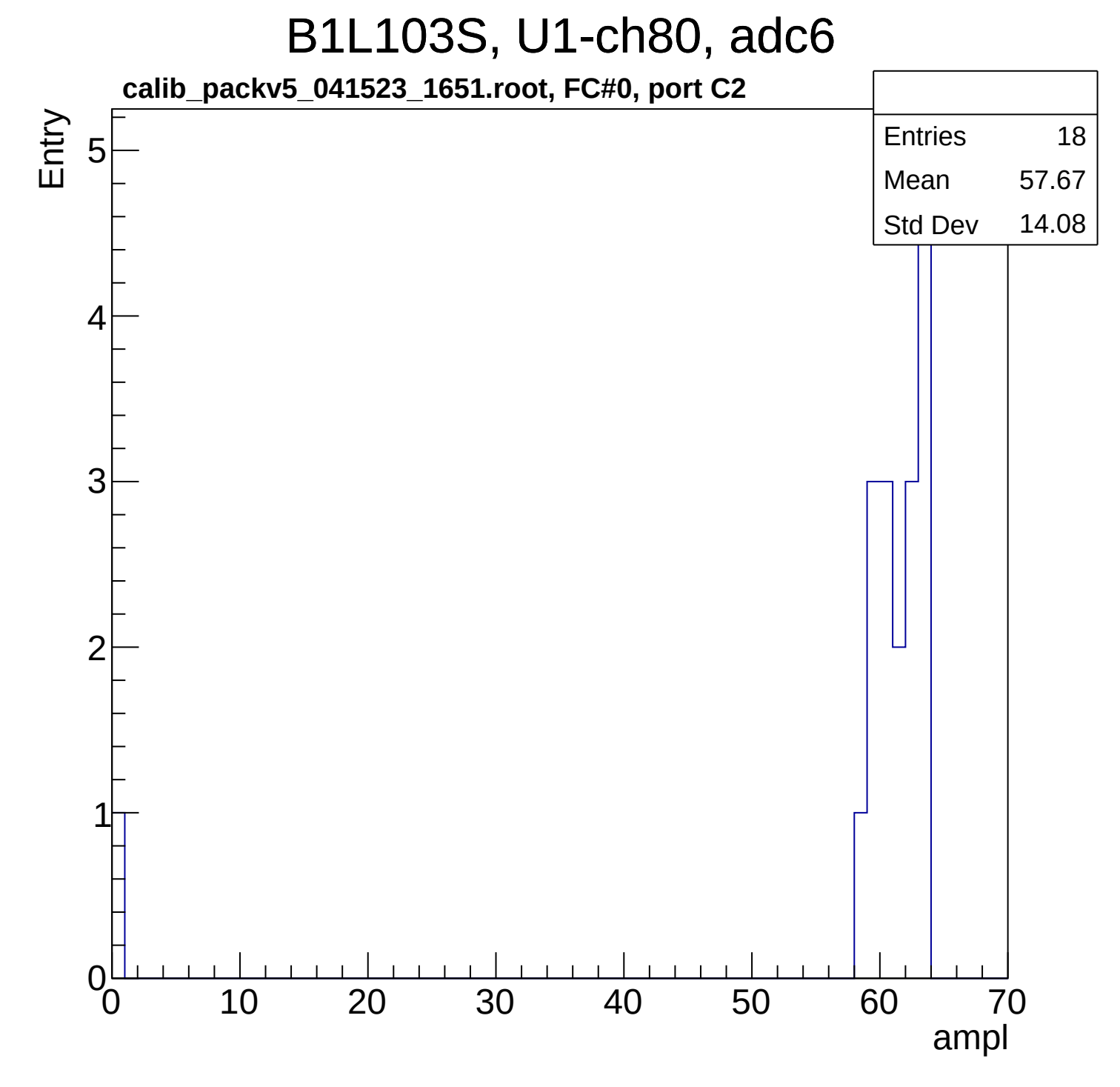
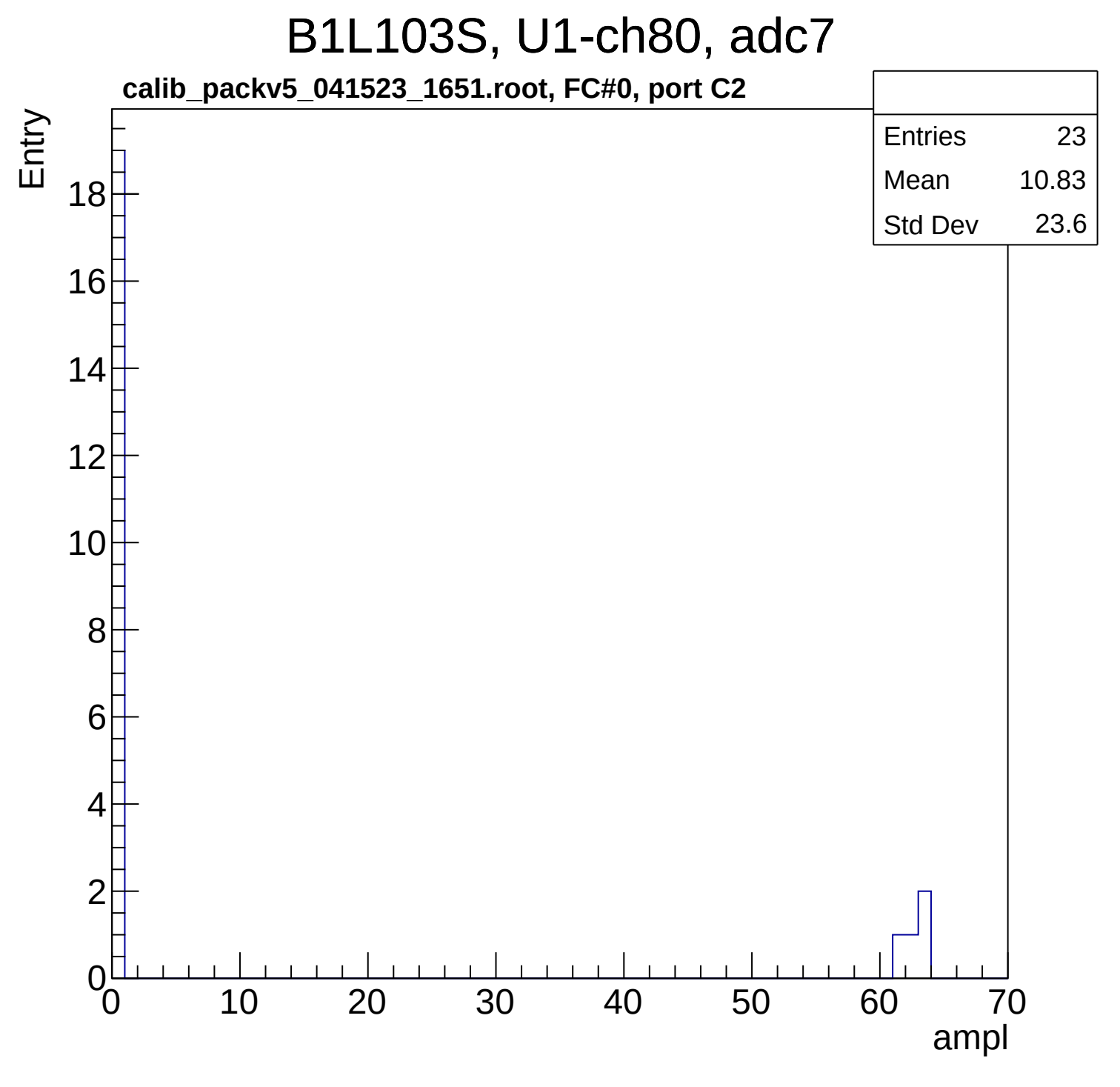

B1L103S, U1-ch80, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 57.67
Std Dev 14.08
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U1-ch80, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 23
Mean 10.83
Std Dev 23.6
Entry
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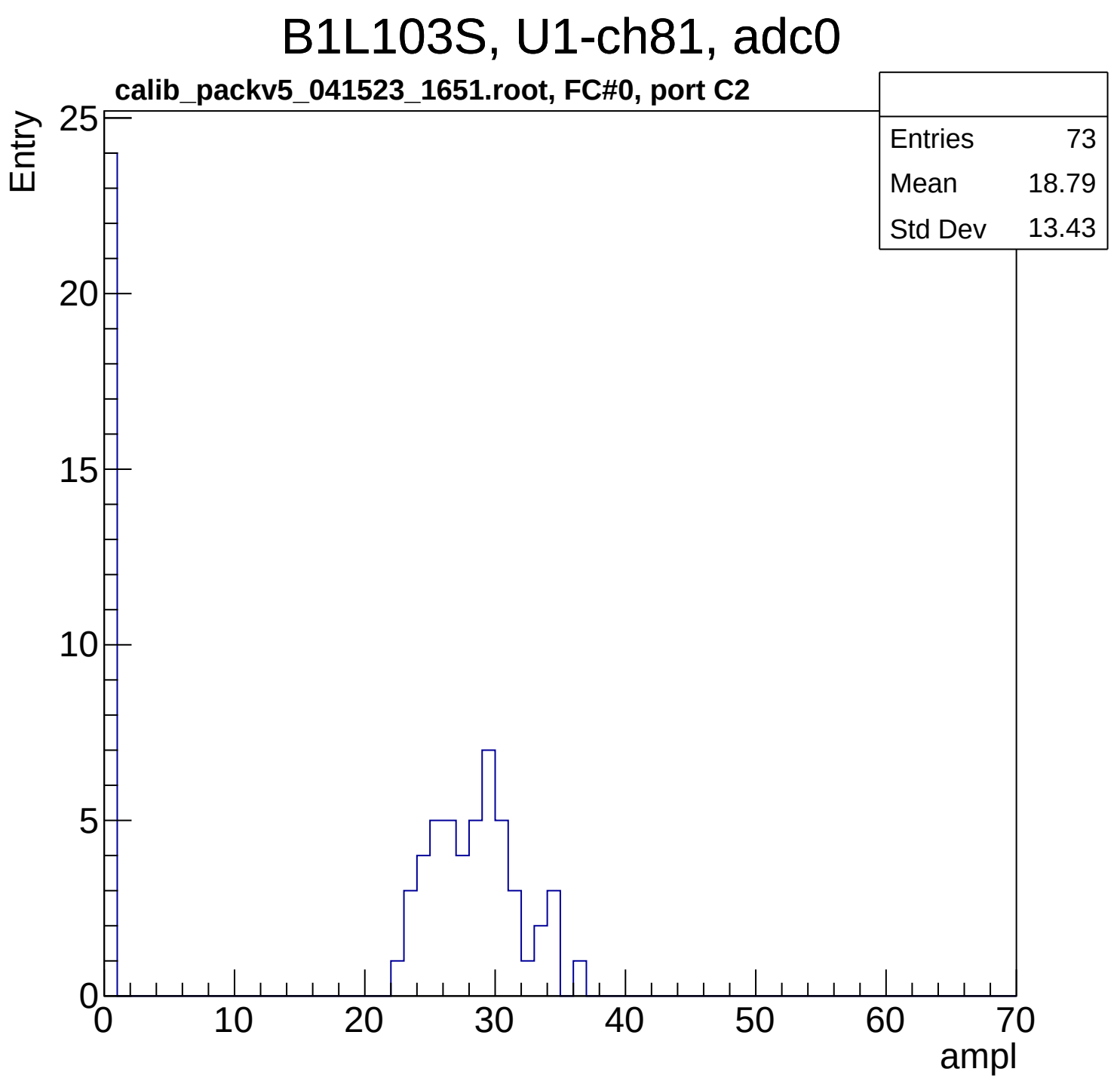
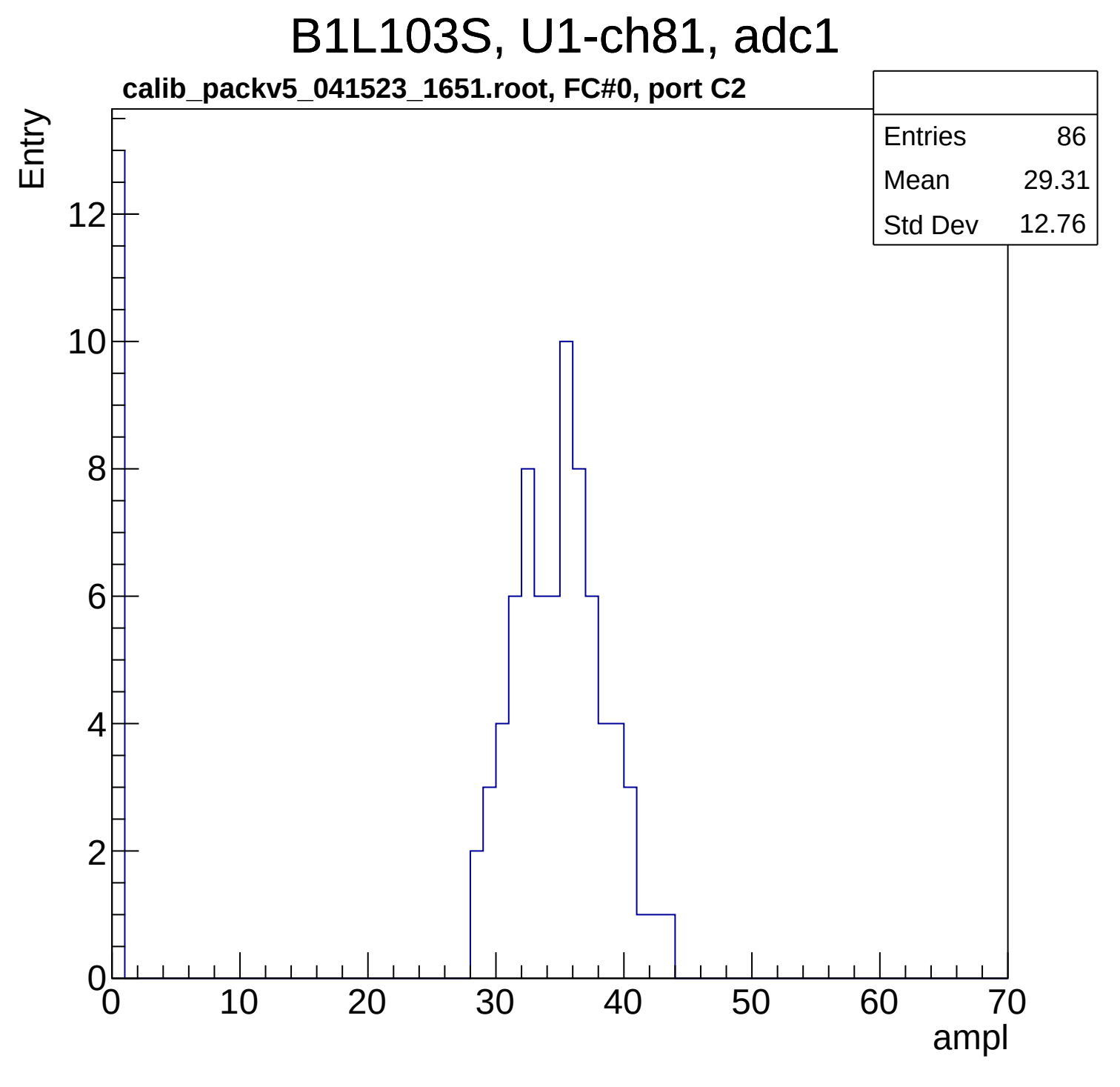
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch81, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 18.79
Std Dev 13.43
Entry
0
5
10
15
20
25
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch81, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 29.31
Std Dev 12.76
Entry
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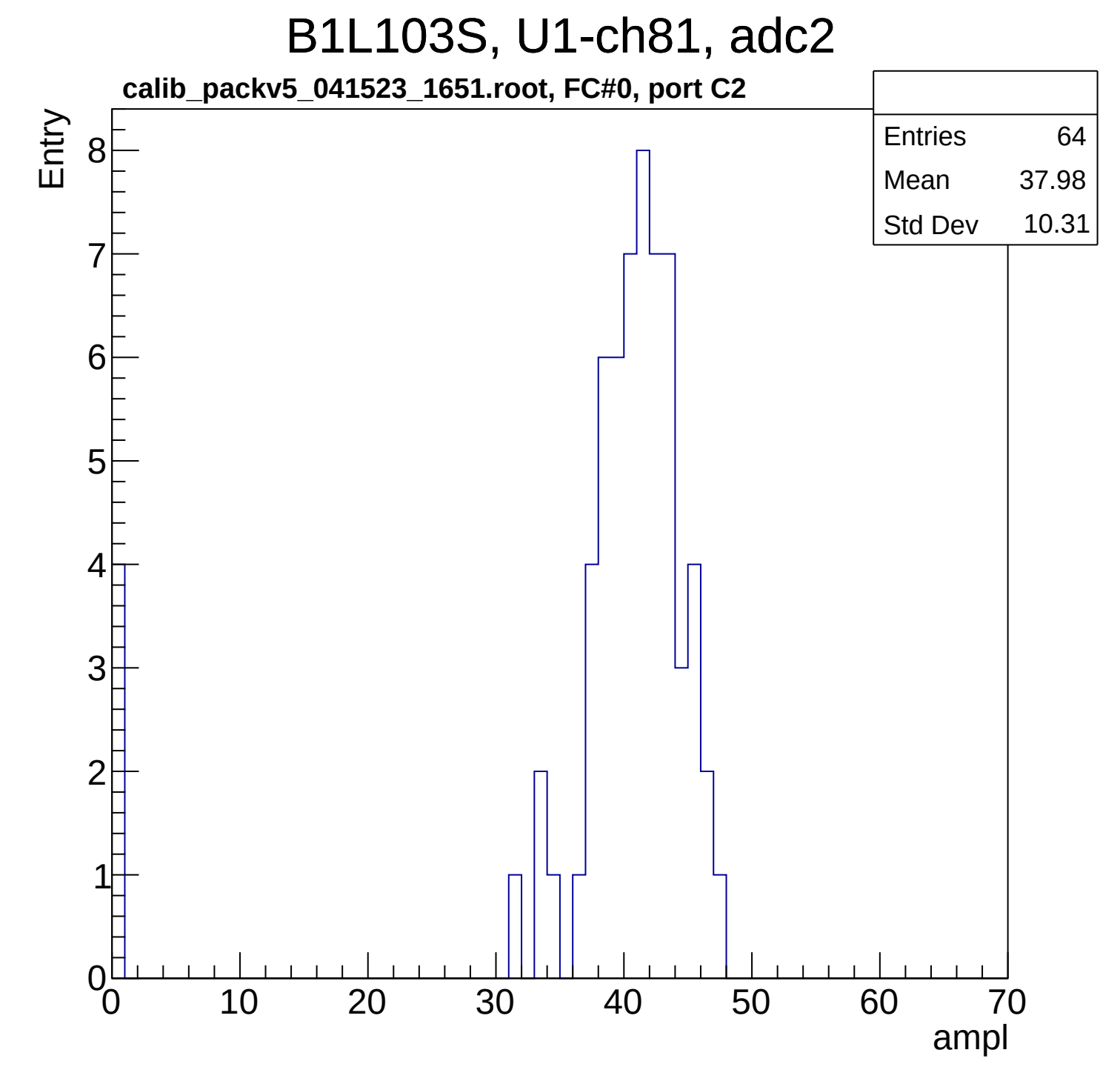
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch81, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 37.98
Std Dev 10.31
Entry
ampl
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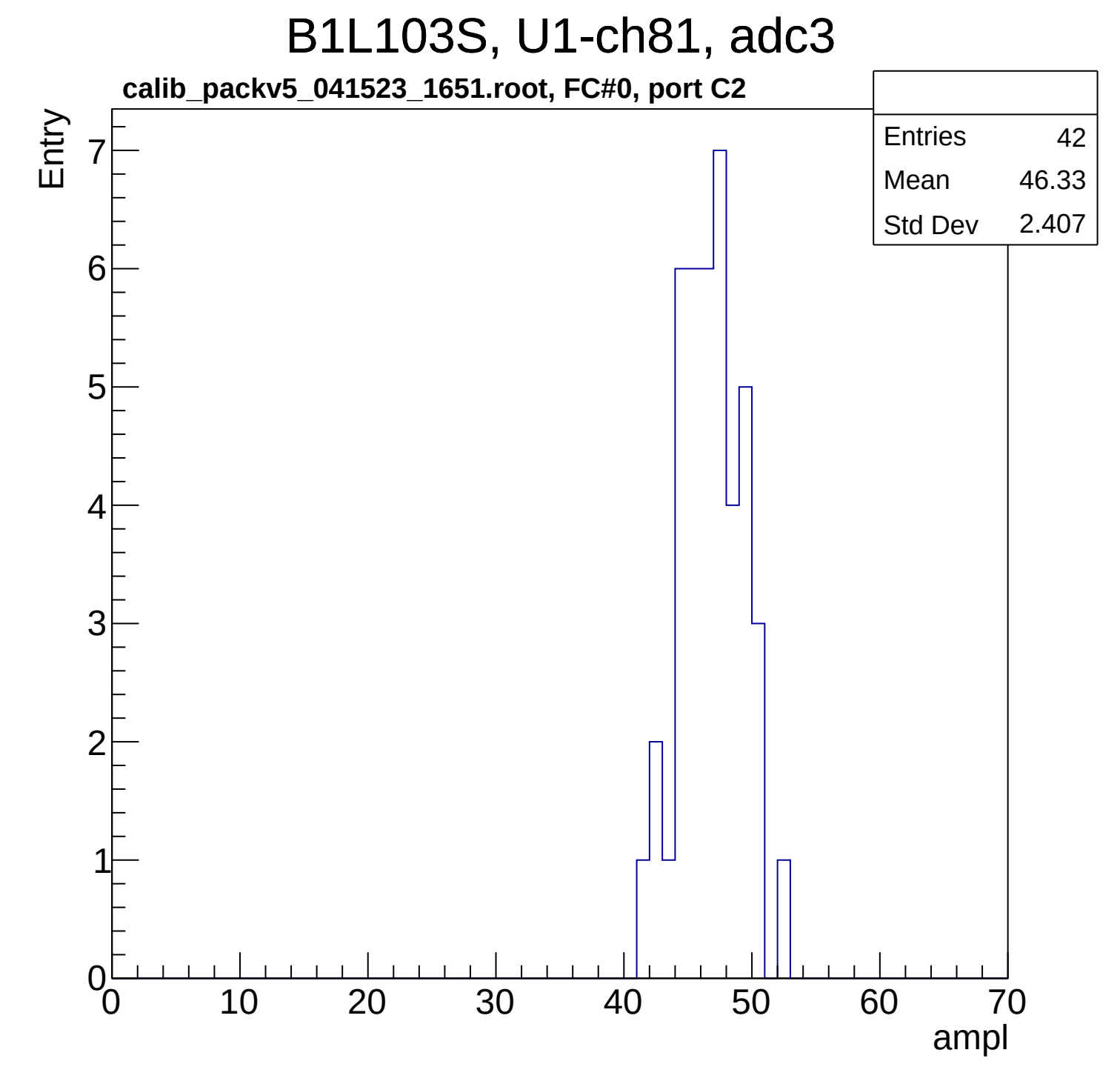
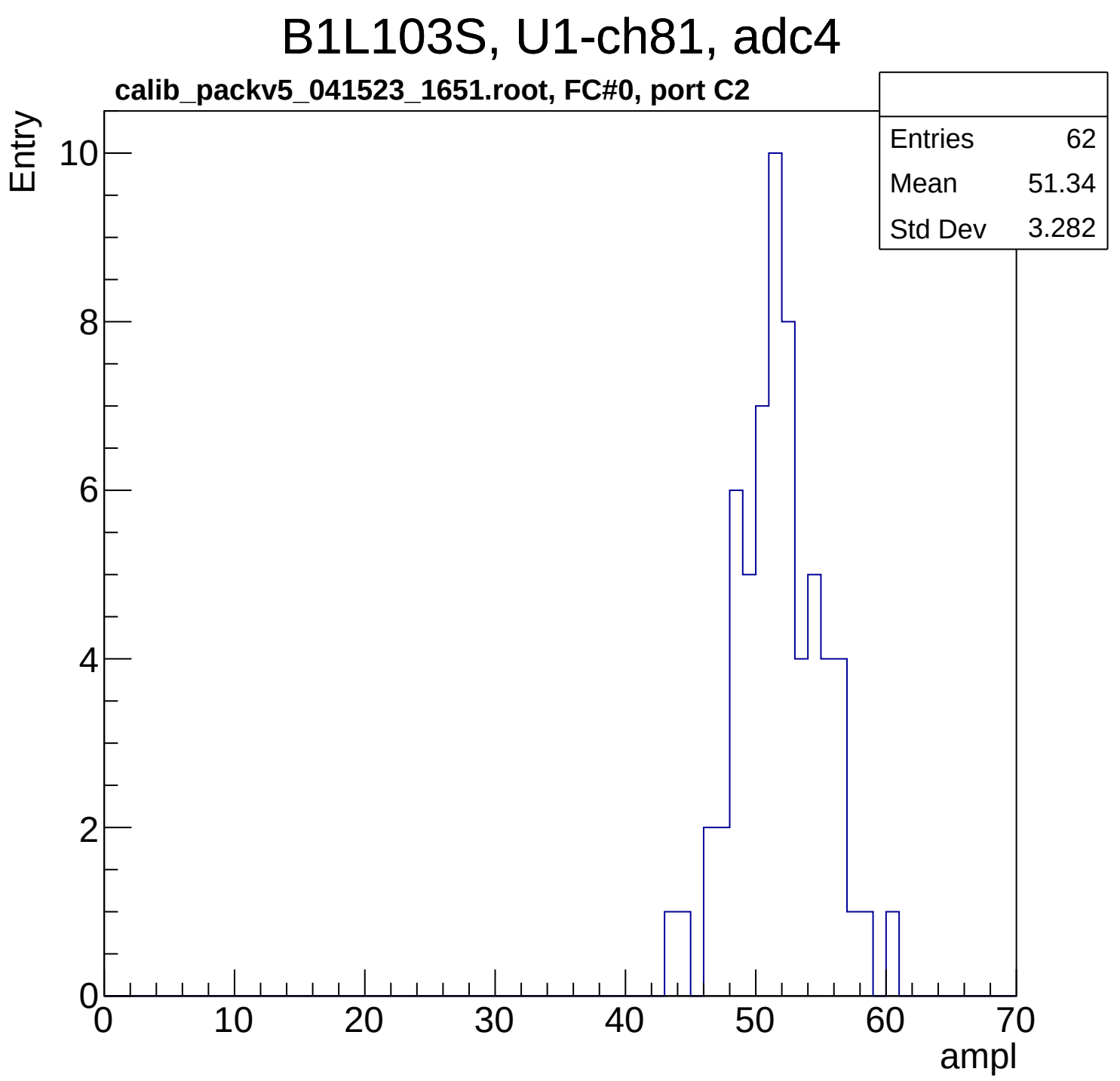
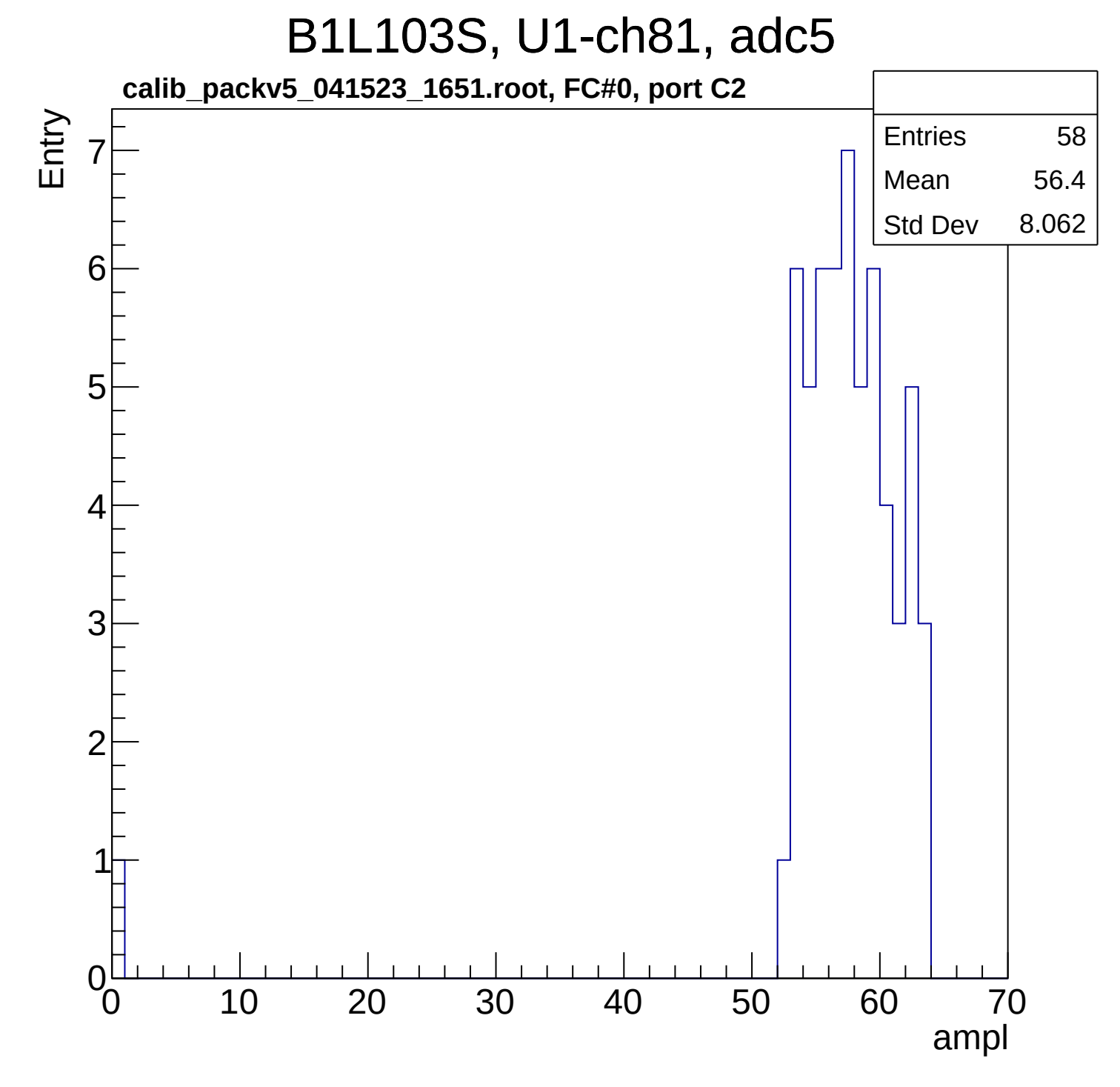
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U1-ch81, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 42
Mean 46.33
Std Dev 2.407
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U1-ch81, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 51.34
Std Dev 3.282
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U1-ch81, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 56.4
Std Dev 8.062
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
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40
50
60
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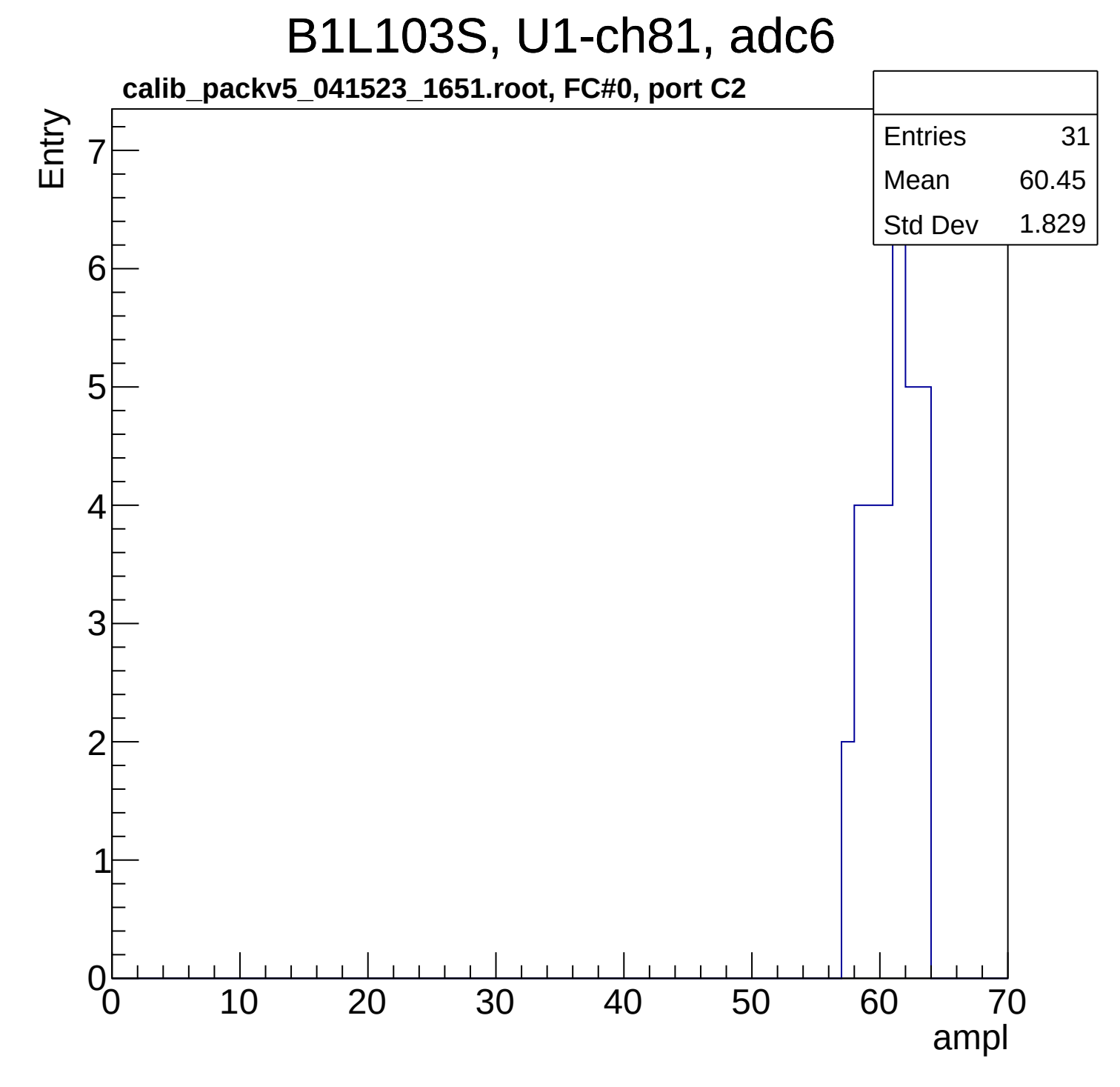
B1L103S, U1-ch81, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 31
Mean 60.45
Std Dev 1.829
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
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40
50
60
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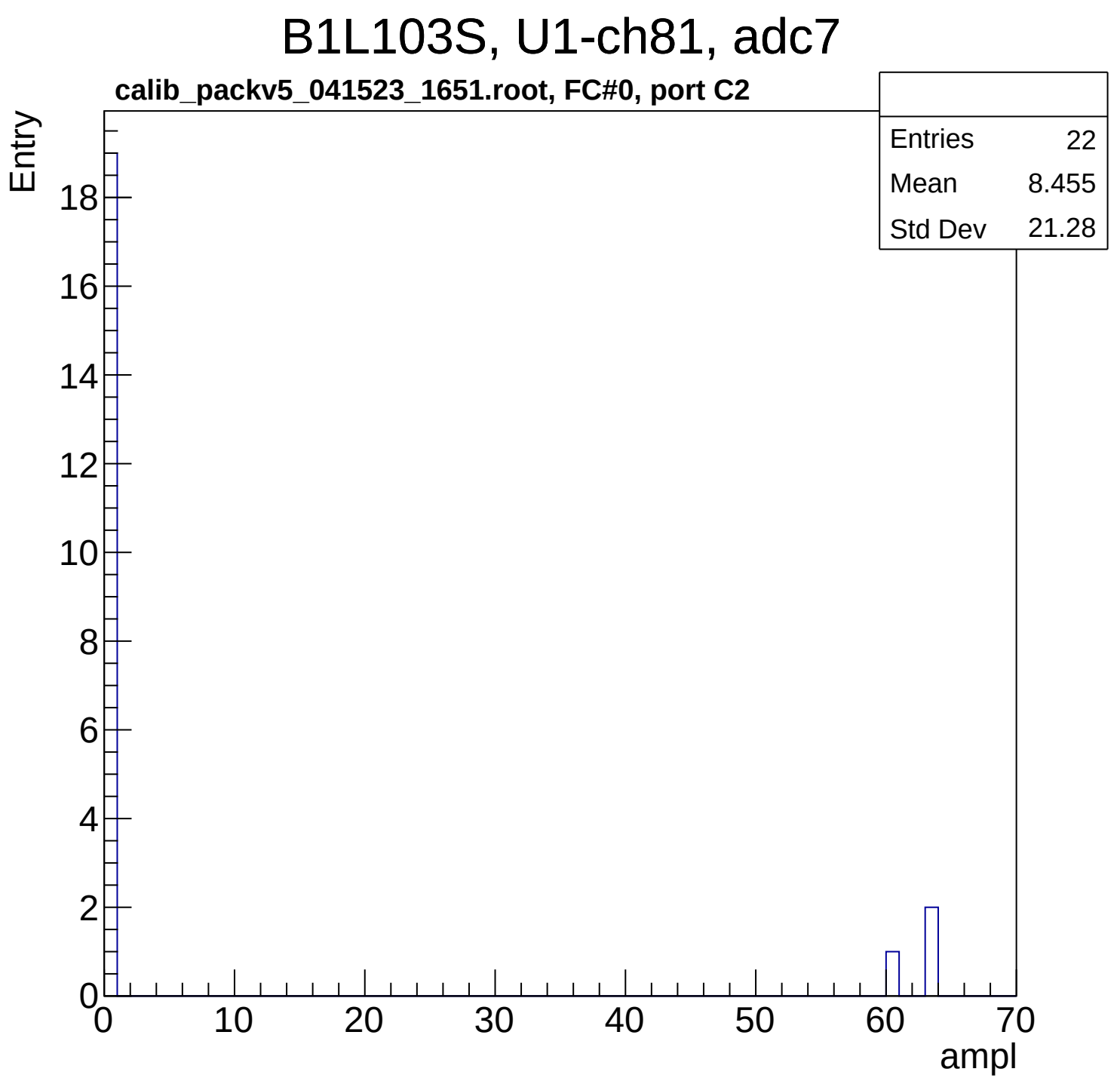
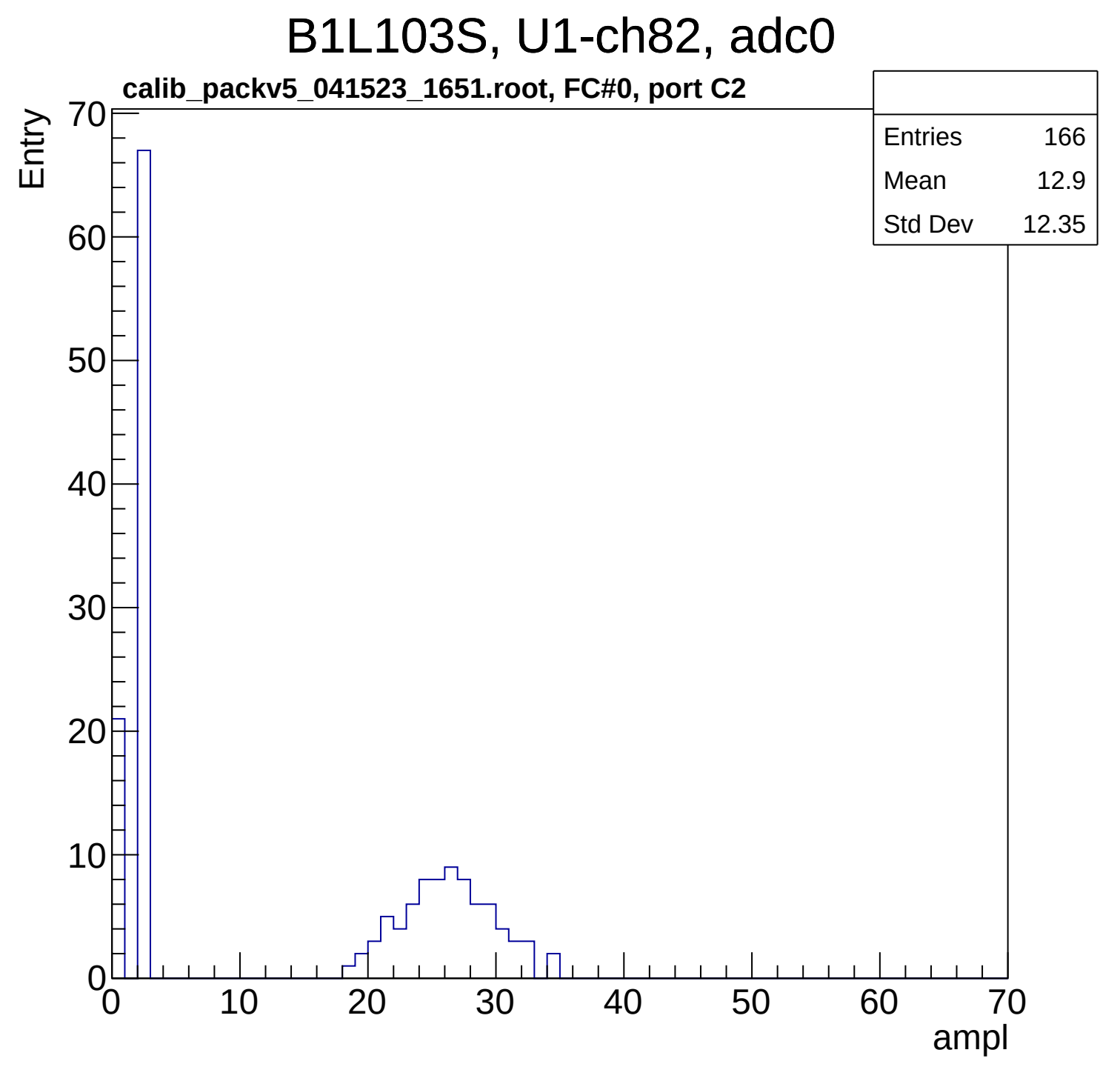

B1L103S, U1-ch81, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 8.455
Std Dev 21.28
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch82, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 166
Mean 12.9
Std Dev 12.35
Entry
ampl
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20
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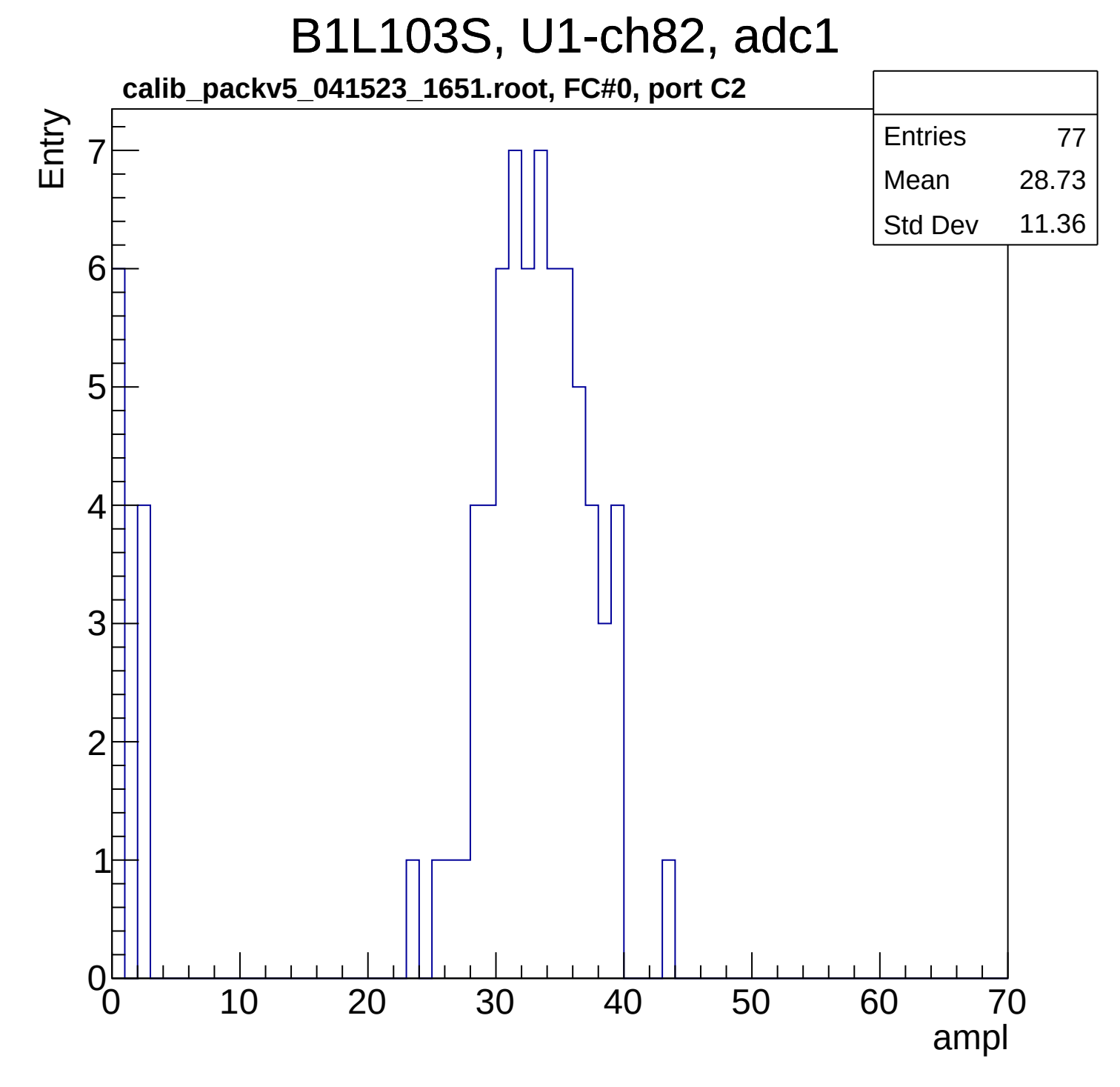
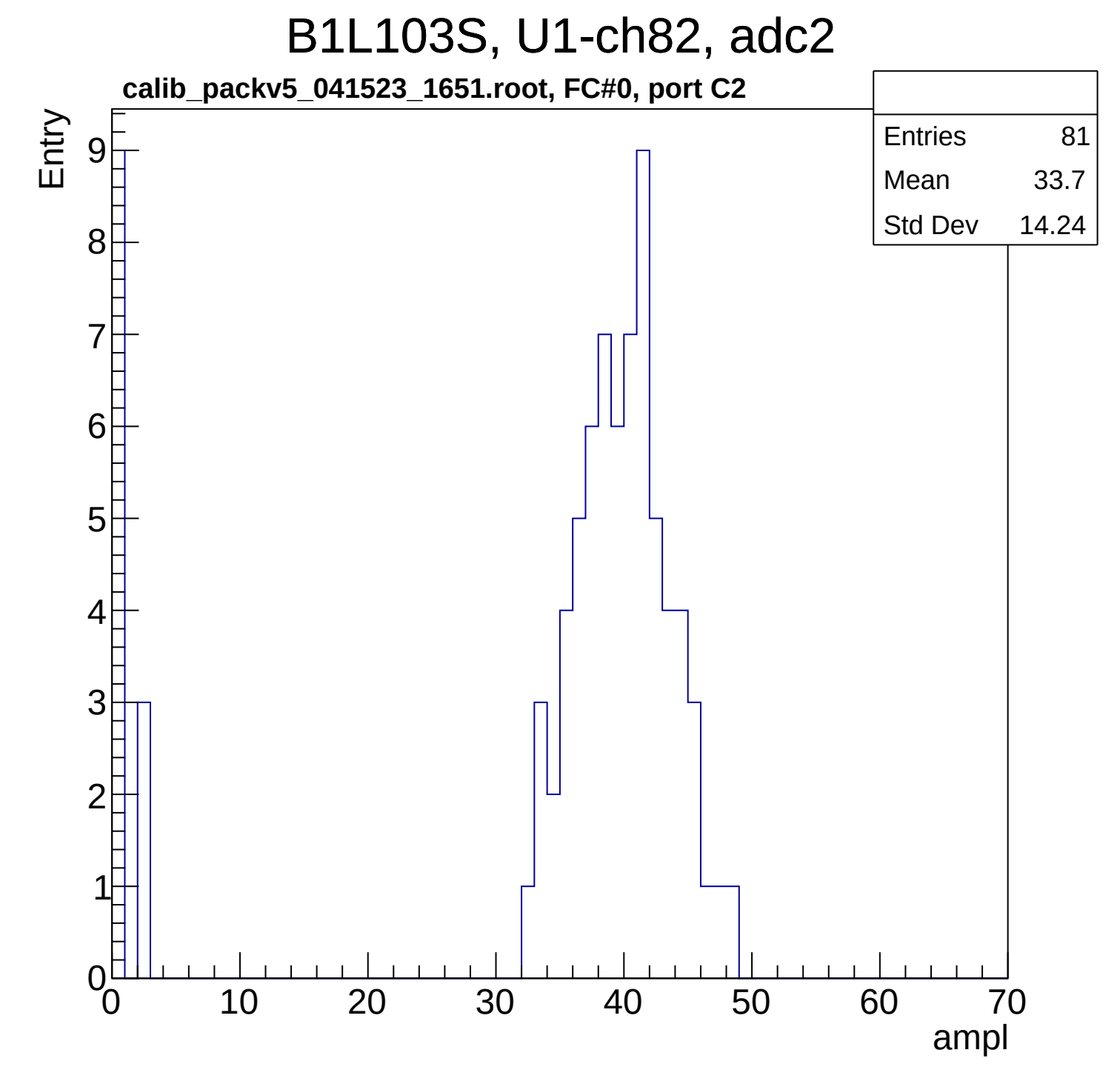
40
50
60
70


B1L103S, U1-ch82, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 28.73
Std Dev 11.36
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U1-ch82, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 33.7
Std Dev 14.24
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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40
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60
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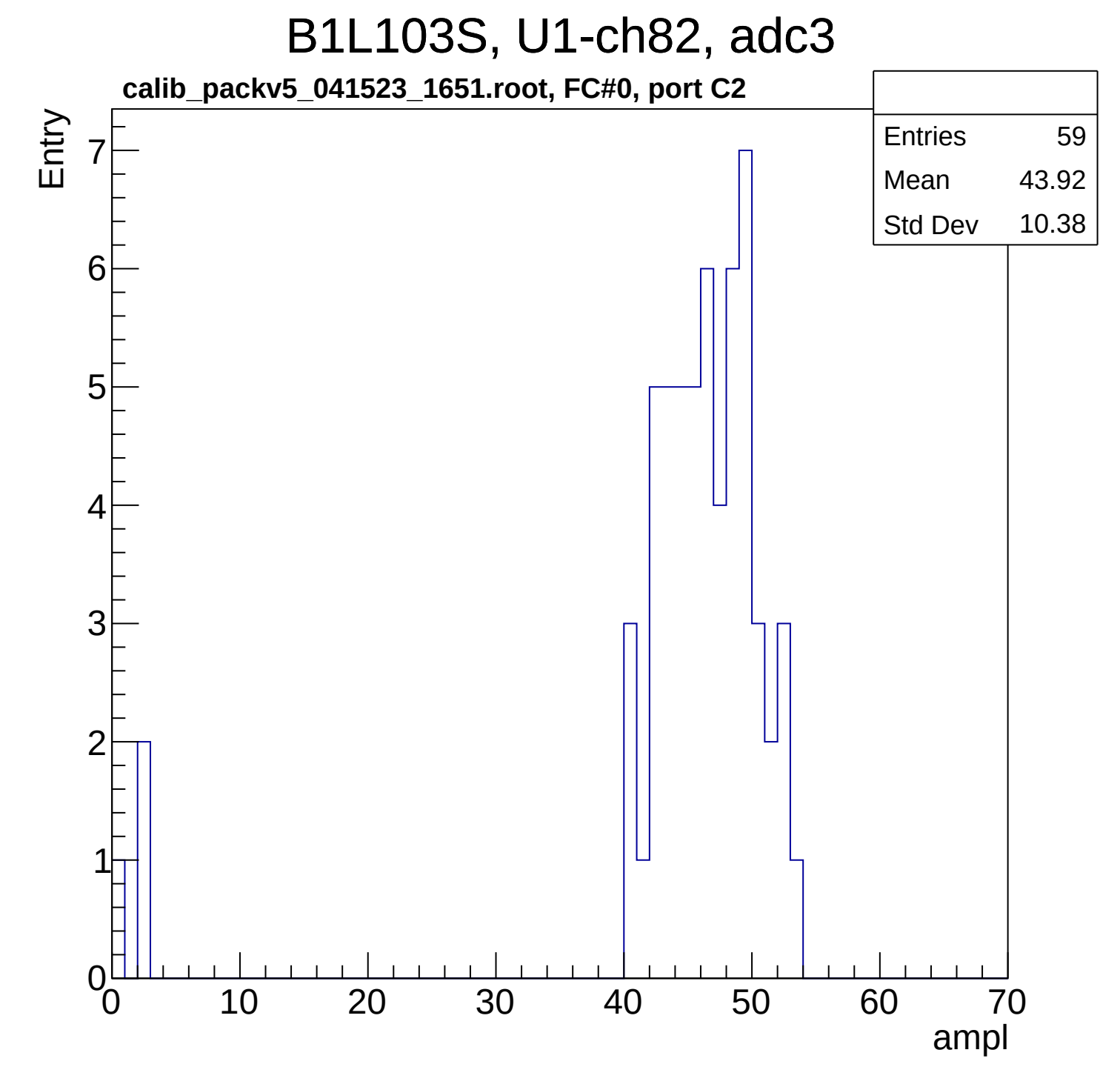
B1L103S, U1-ch82, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 43.92
Std Dev 10.38
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
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40
50
60
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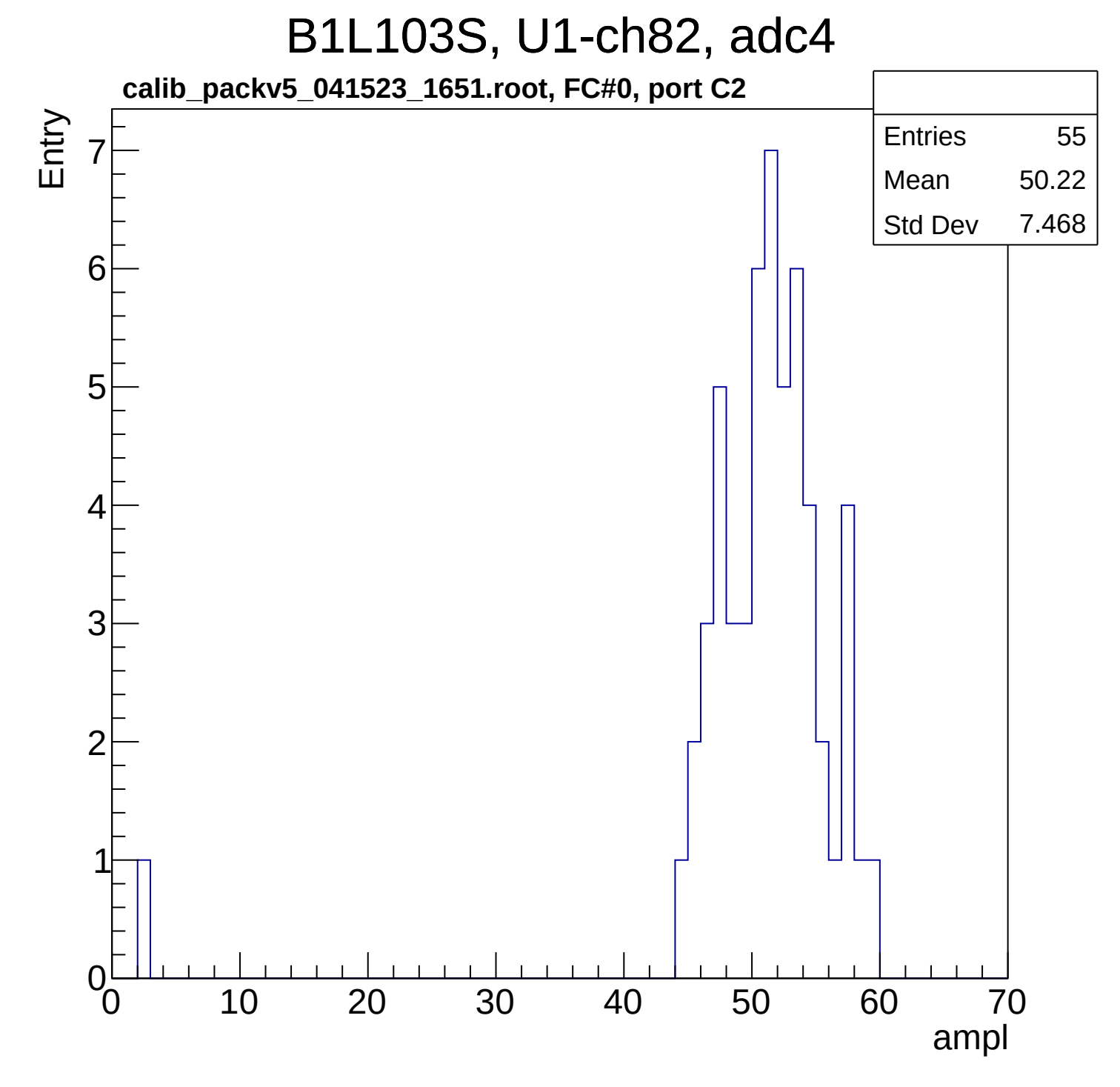
B1L103S, U1-ch82, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 50.22
Std Dev 7.468
Entry
ampl
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1
2
3
4
5
6
7
0
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20
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60
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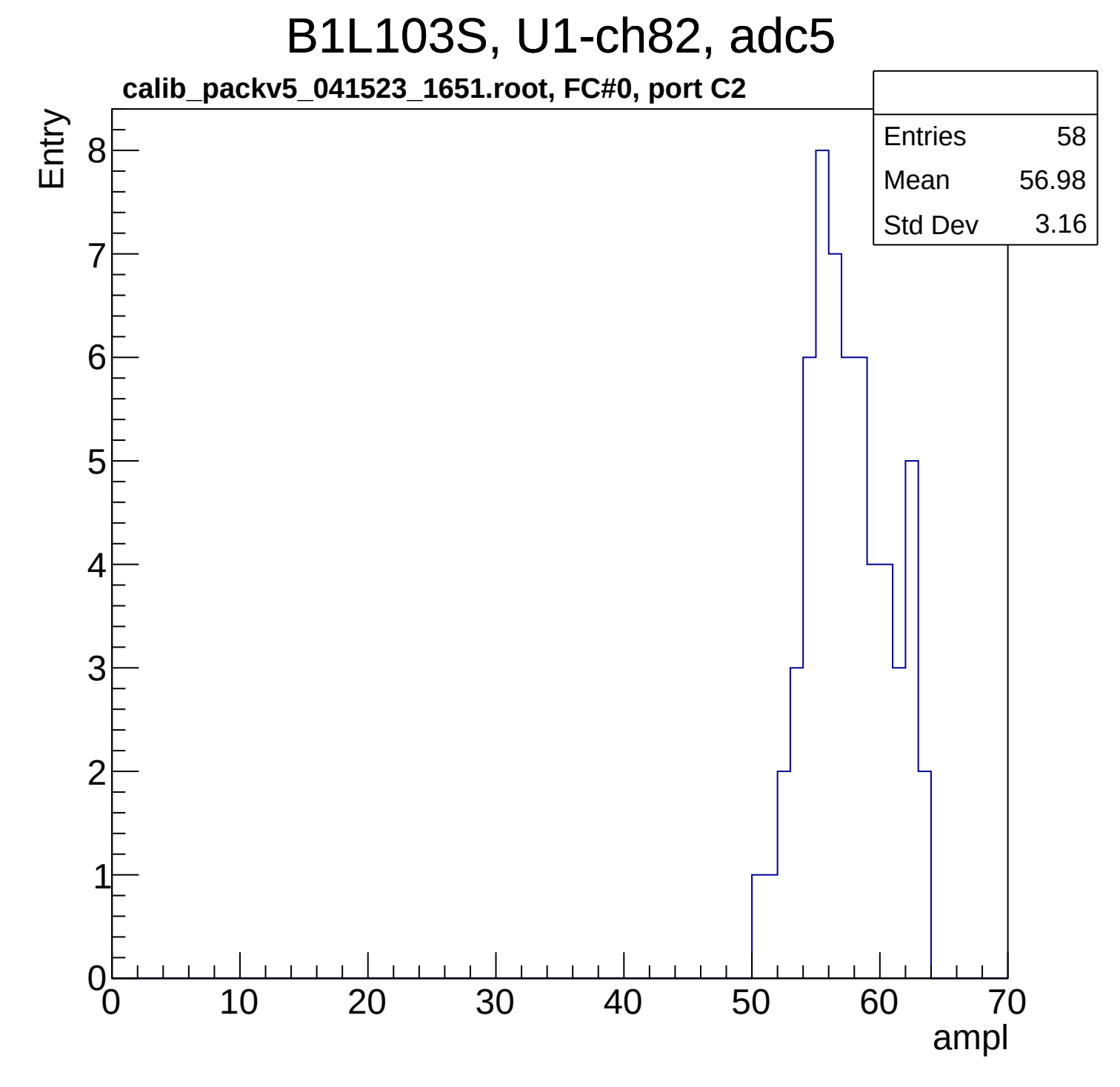
B1L103S, U1-ch82, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 56.98
Std Dev 3.16
Entry
ampl
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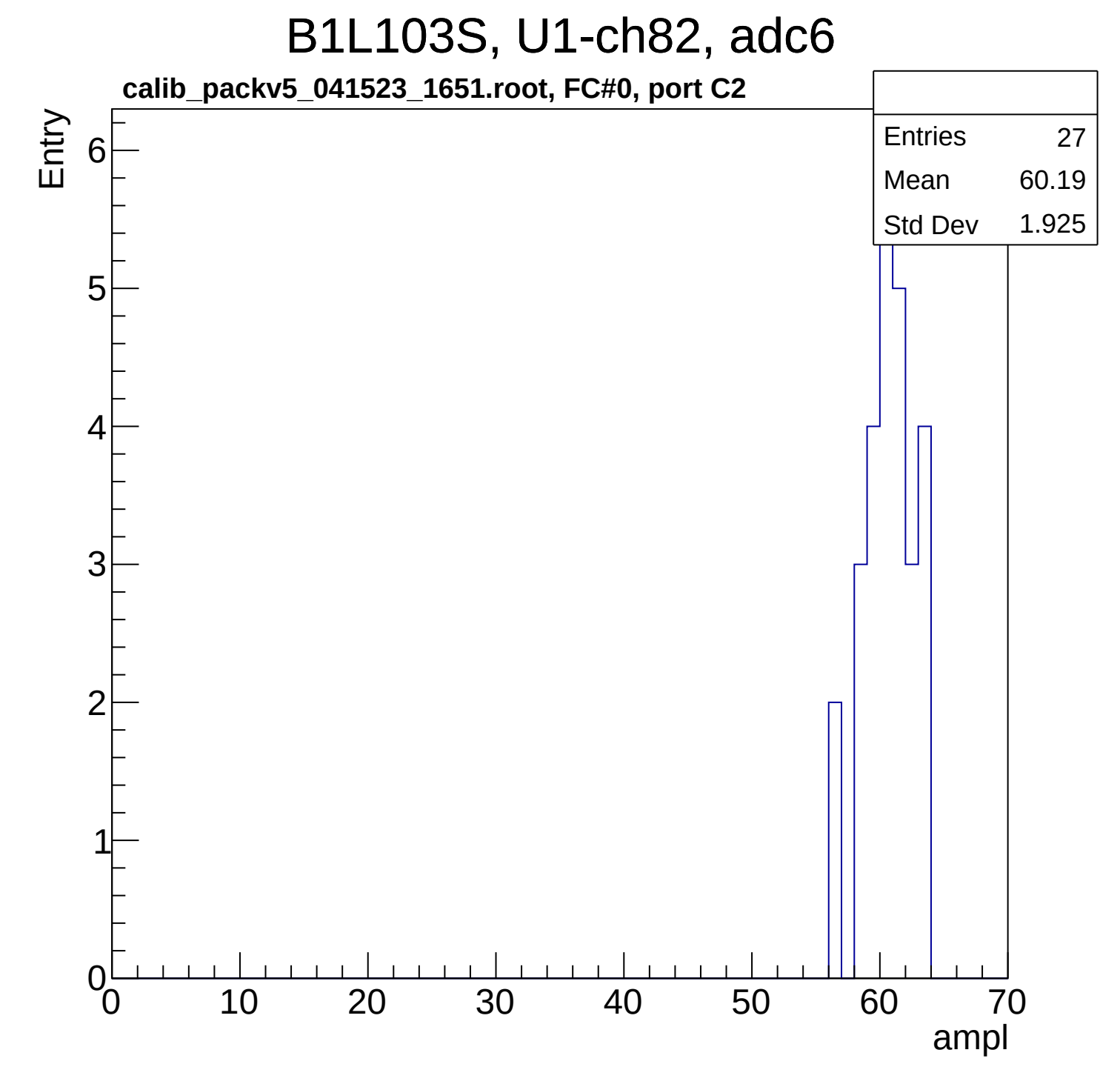
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U1-ch82, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 27
Mean 60.19
Std Dev 1.925
Entry
ampl
0
1
2
3
4
5
6
0
10
20
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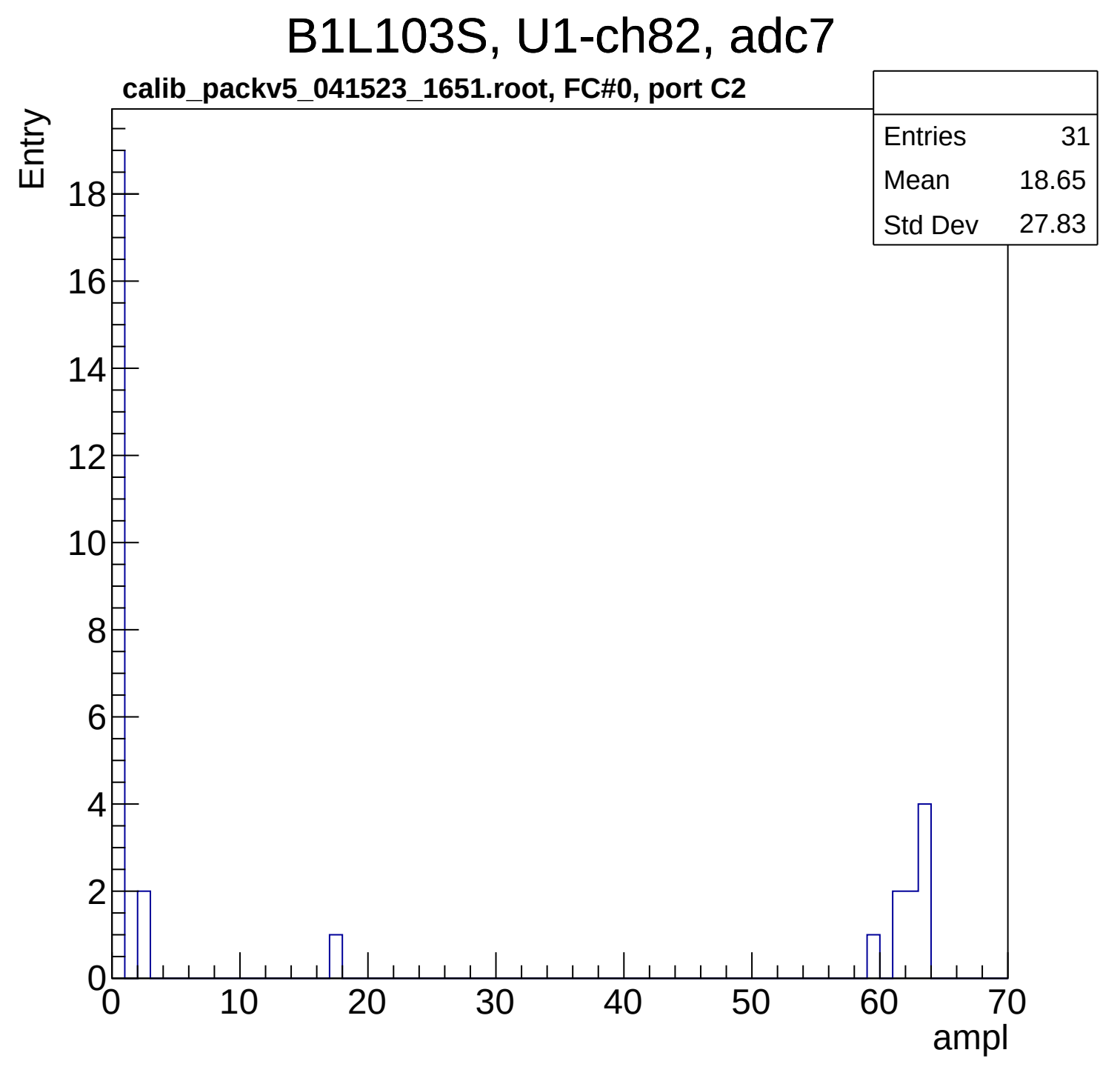
40
50
60
70


B1L103S, U1-ch82, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 31
Mean 18.65
Std Dev 27.83
Entry
0
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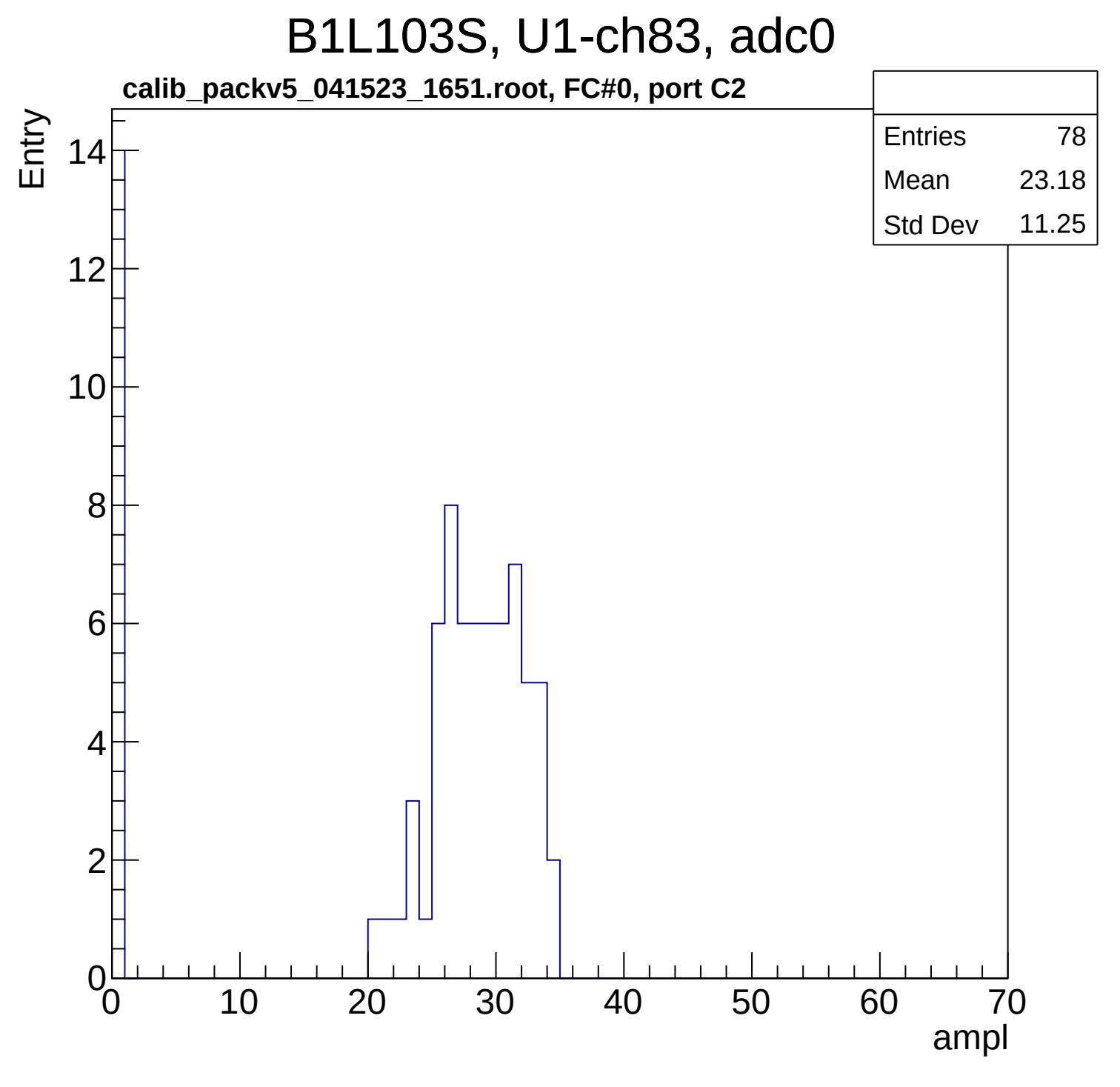
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch83, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 23.18
Std Dev 11.25
Entry
ampl
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2
4
6
8
10
12
14
0
10
20
30
40
50
60
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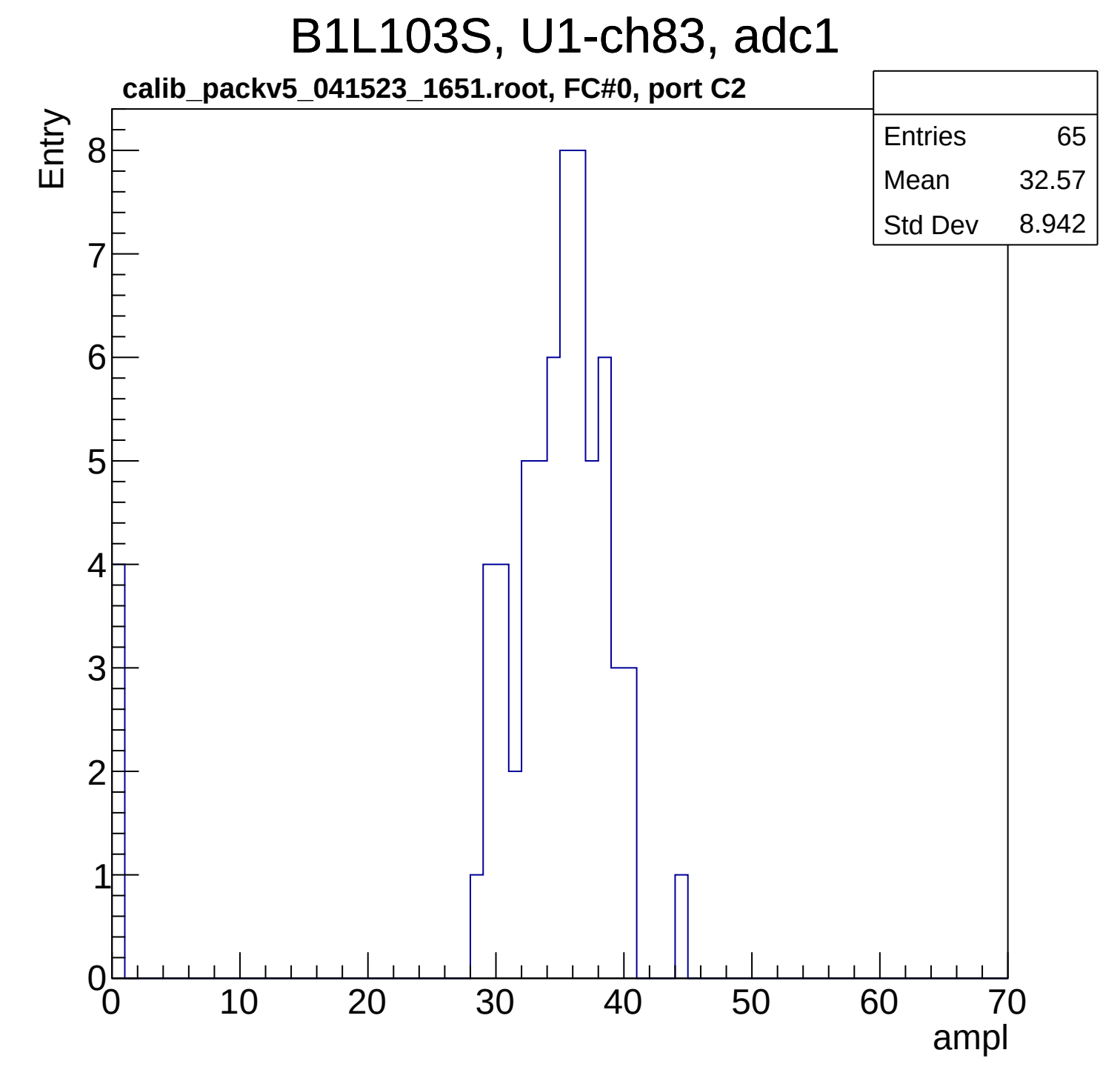
B1L103S, U1-ch83, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 32.57
Std Dev 8.942
Entry
ampl
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2
3
4
5
6
7
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0
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20
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60
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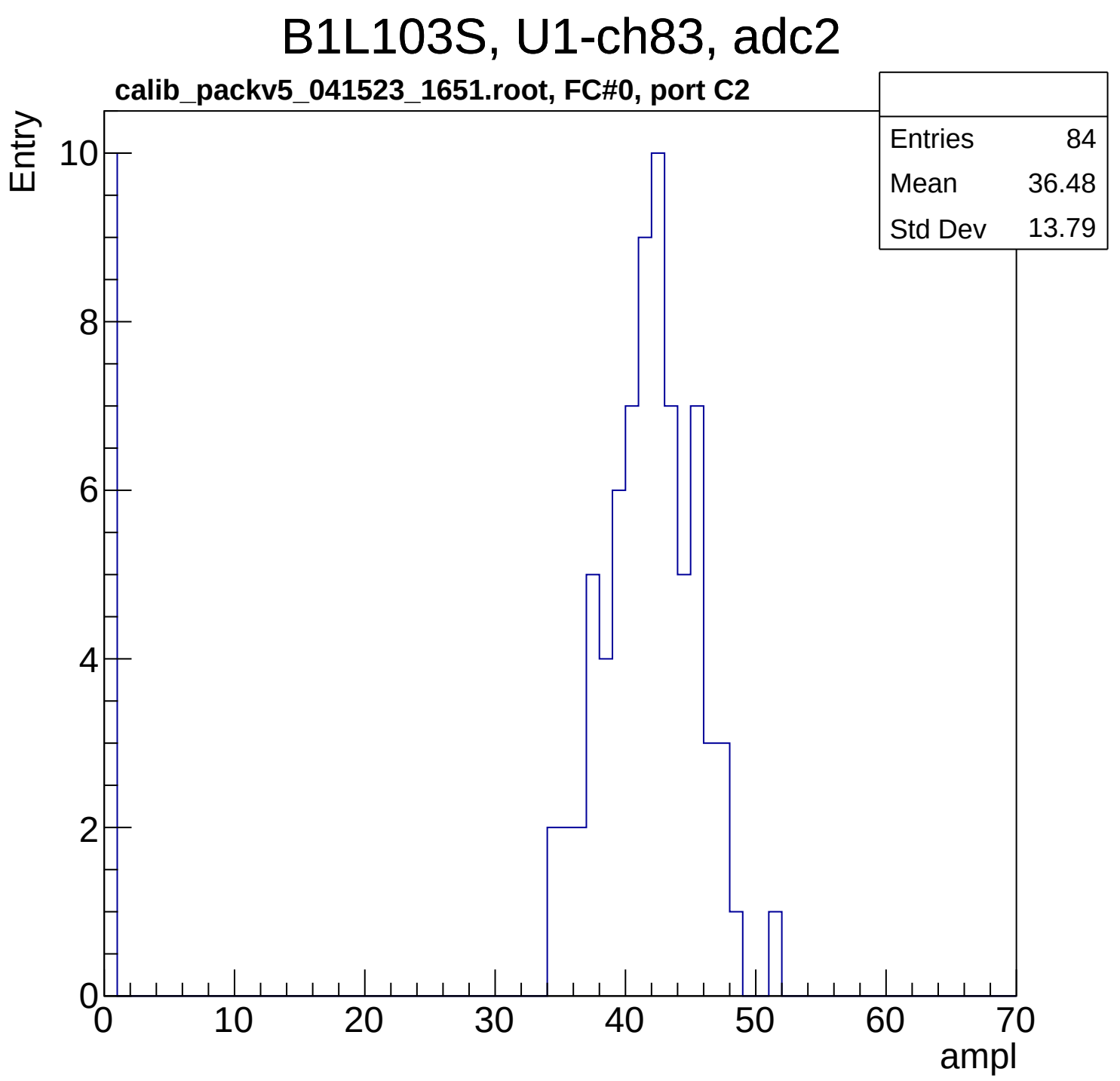
B1L103S, U1-ch83, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 36.48
Std Dev 13.79
Entry
ampl
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2
4
6
8
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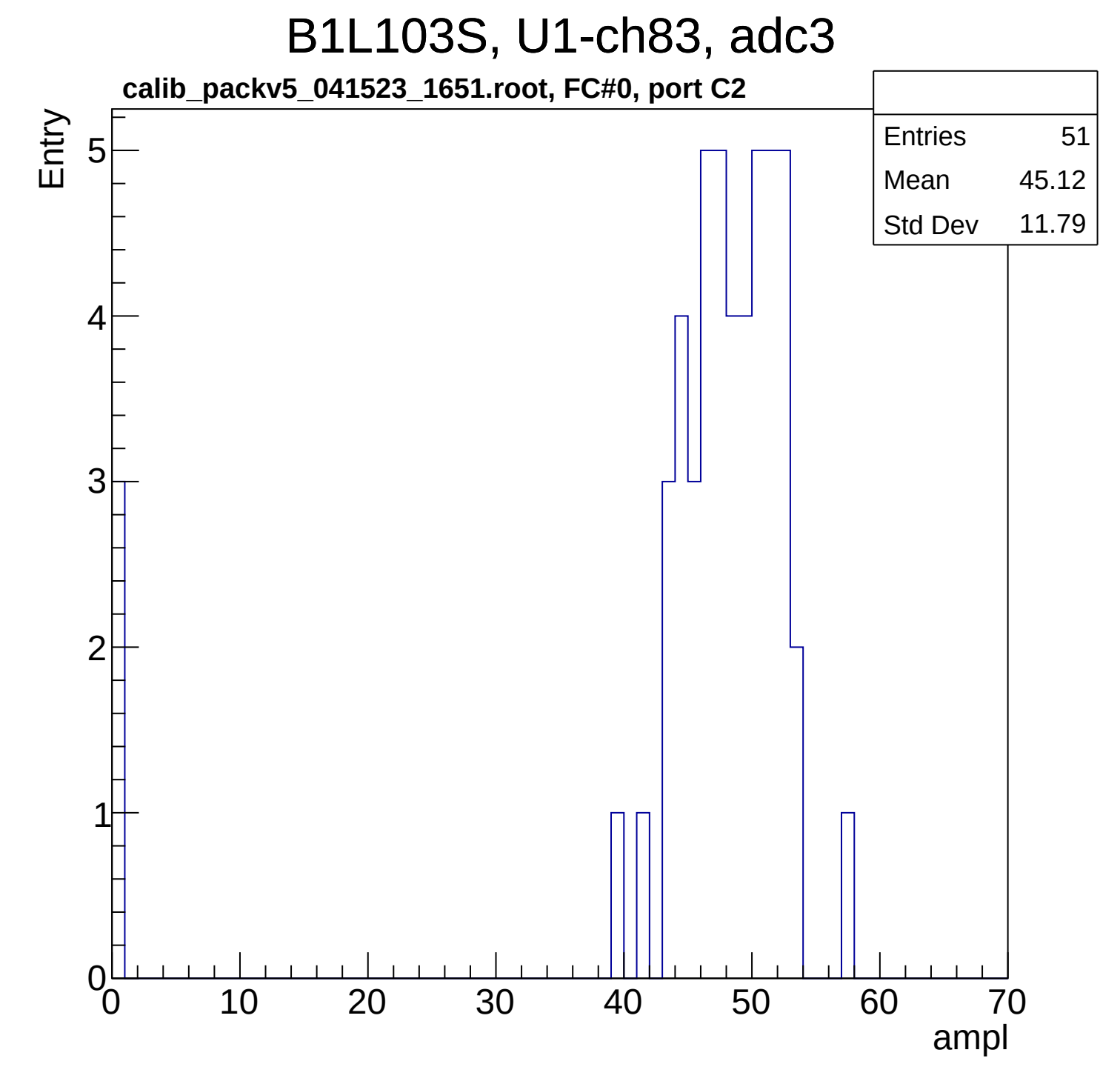
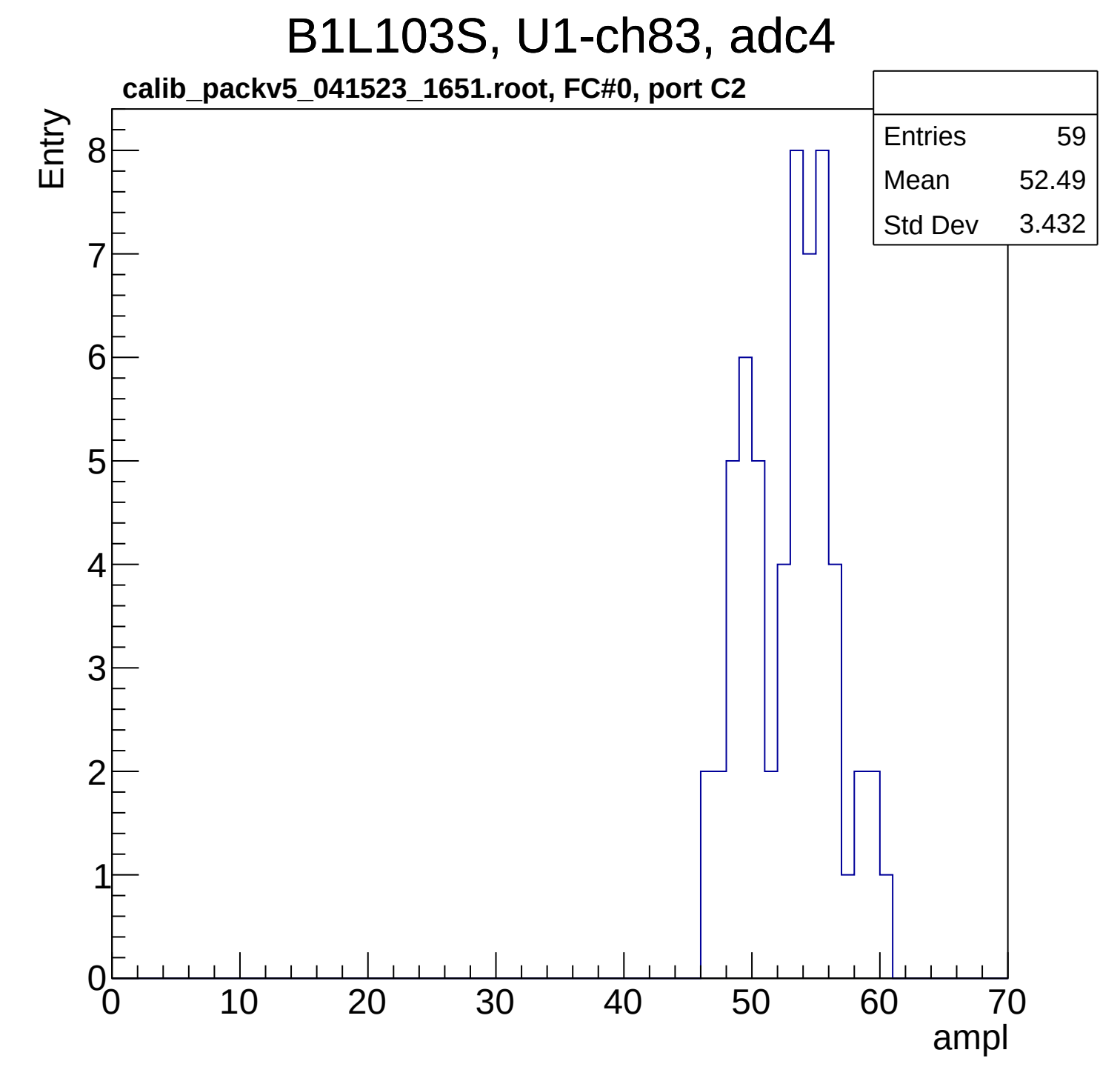
0
10
20
30
40
50
60
70


B1L103S, U1-ch83, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 45.12
Std Dev 11.79
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U1-ch83, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 52.49
Std Dev 3.432
Entry
ampl
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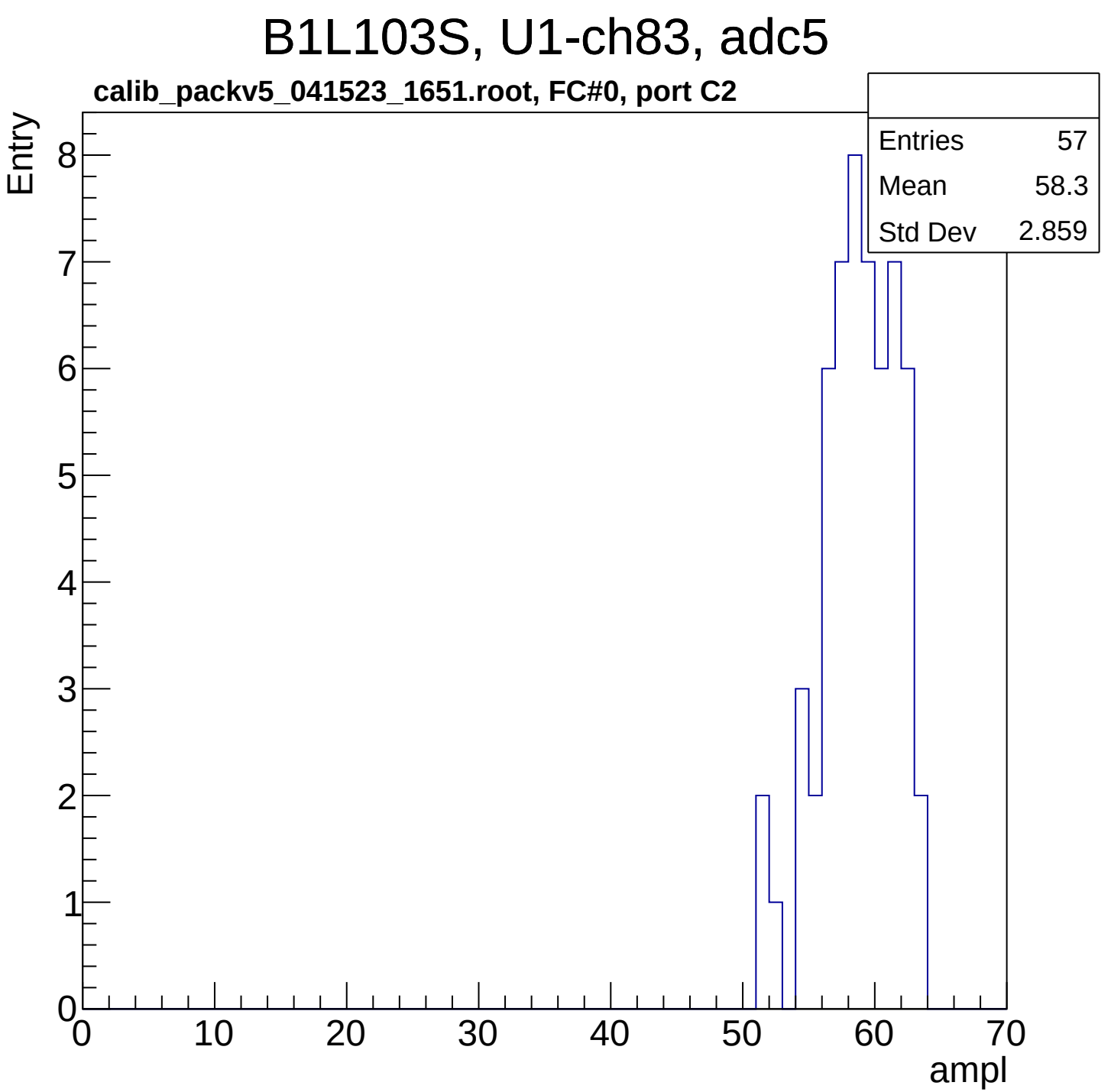
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U1-ch83, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 58.3
Std Dev 2.859
Entry
ampl
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2
3
4
5
6
7
8
0
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20
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40
50
60
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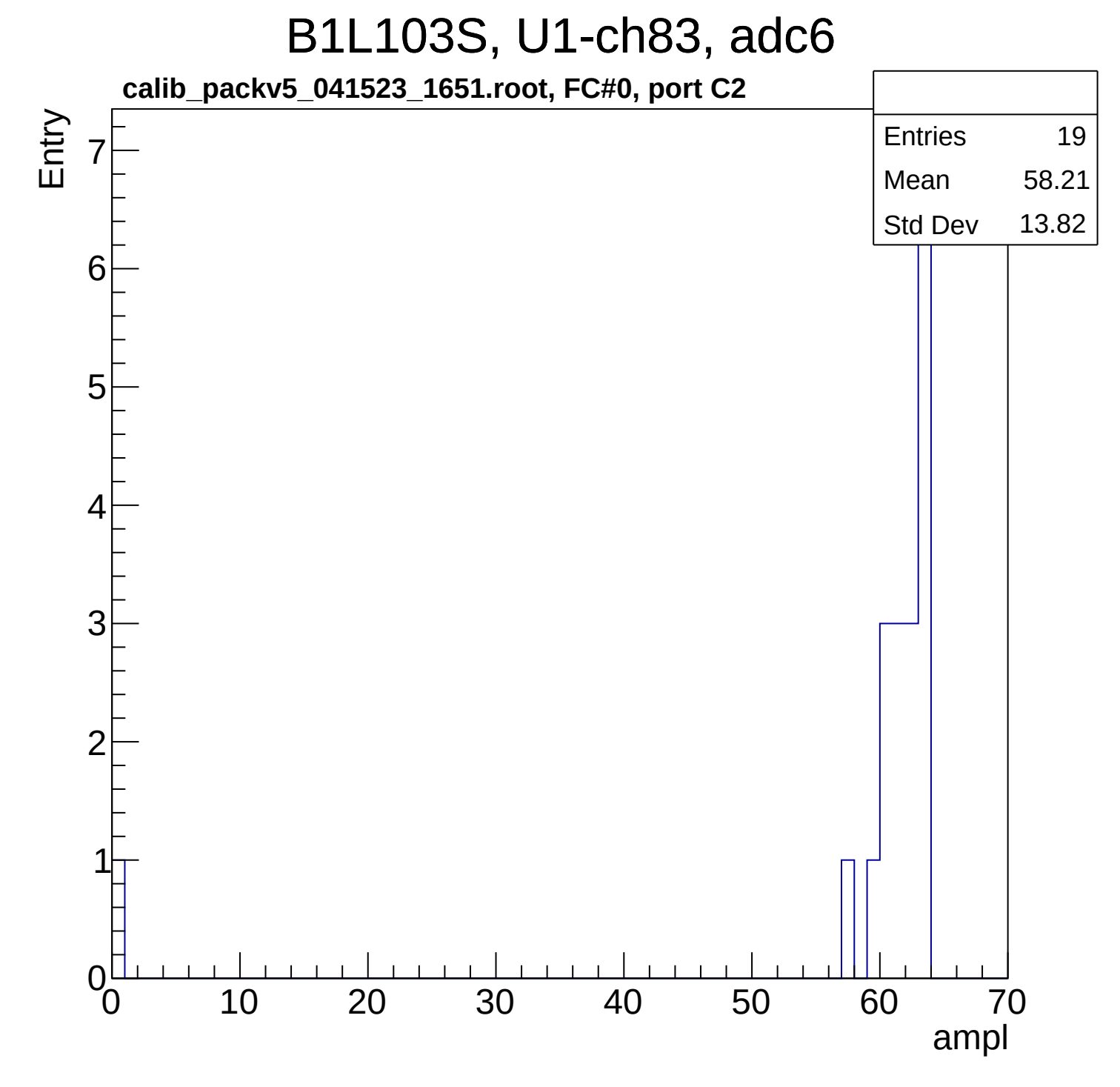
B1L103S, U1-ch83, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 58.21
Std Dev 13.82
Entry
ampl
0
1
2
3
4
5
6
7
0
10
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40
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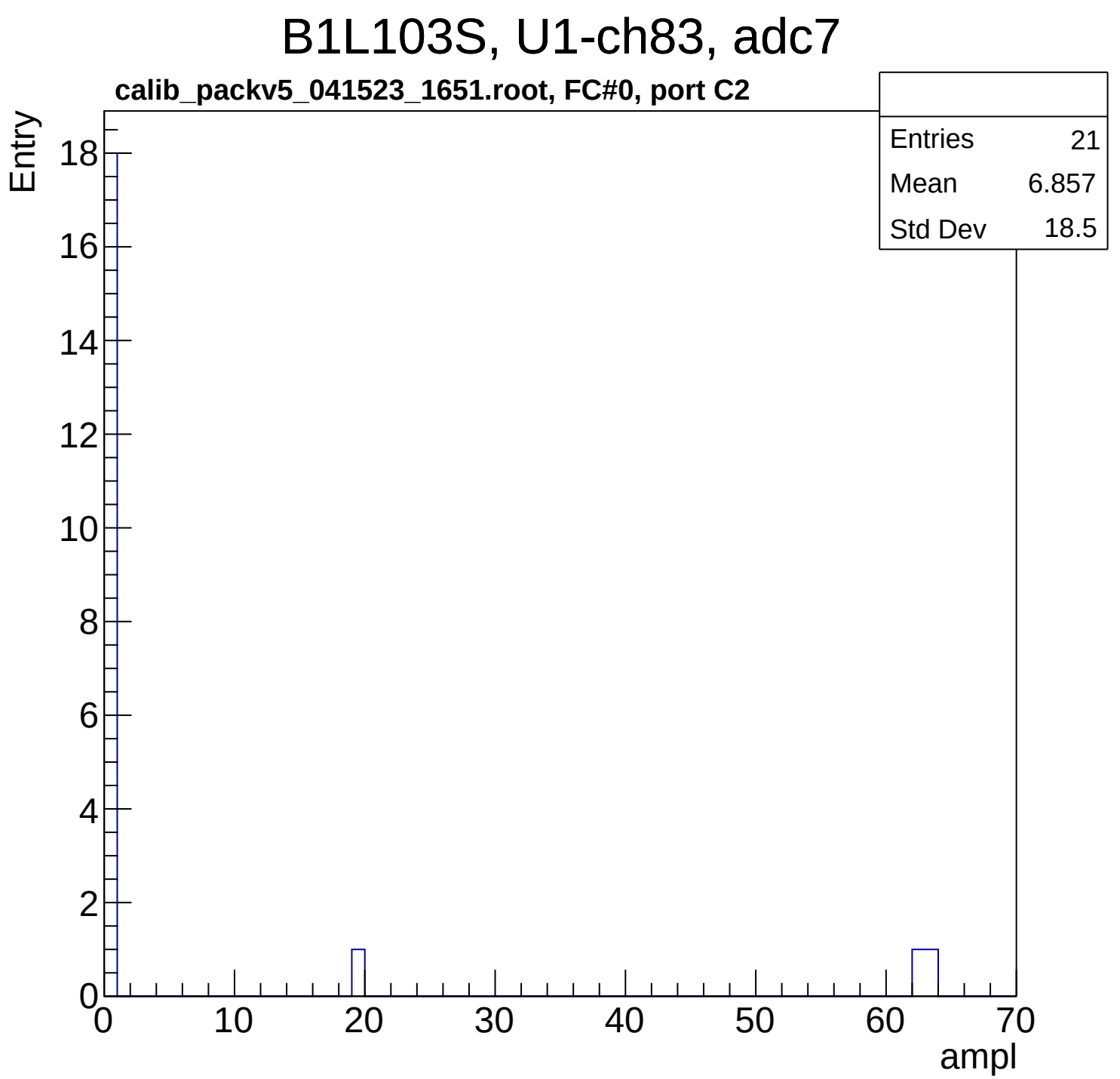
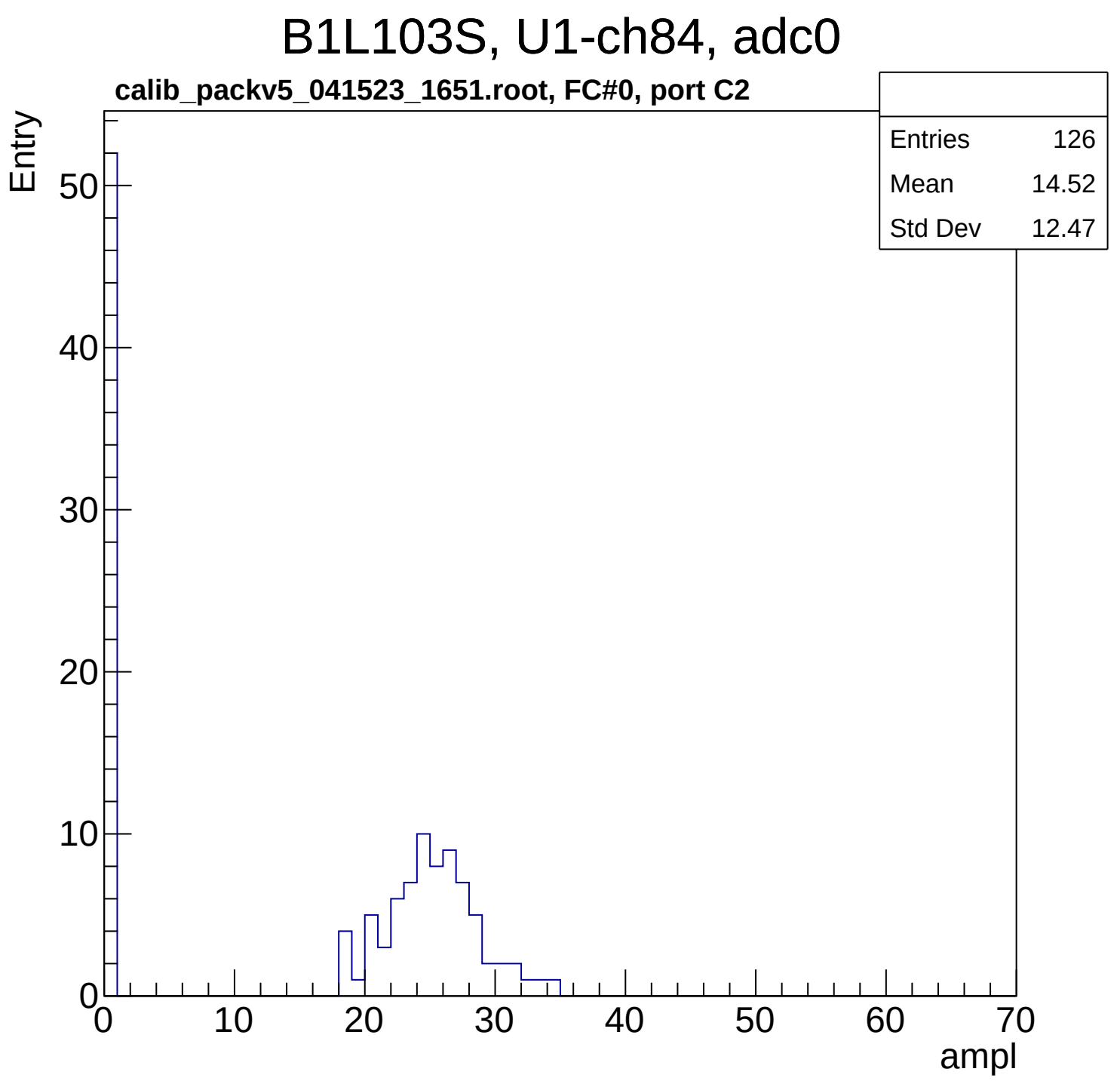
60
70


B1L103S, U1-ch83, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 6.857
Std Dev 18.5
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch84, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 126
Mean 14.52
Std Dev 12.47
Entry
0
10
20
30
40
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0
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20
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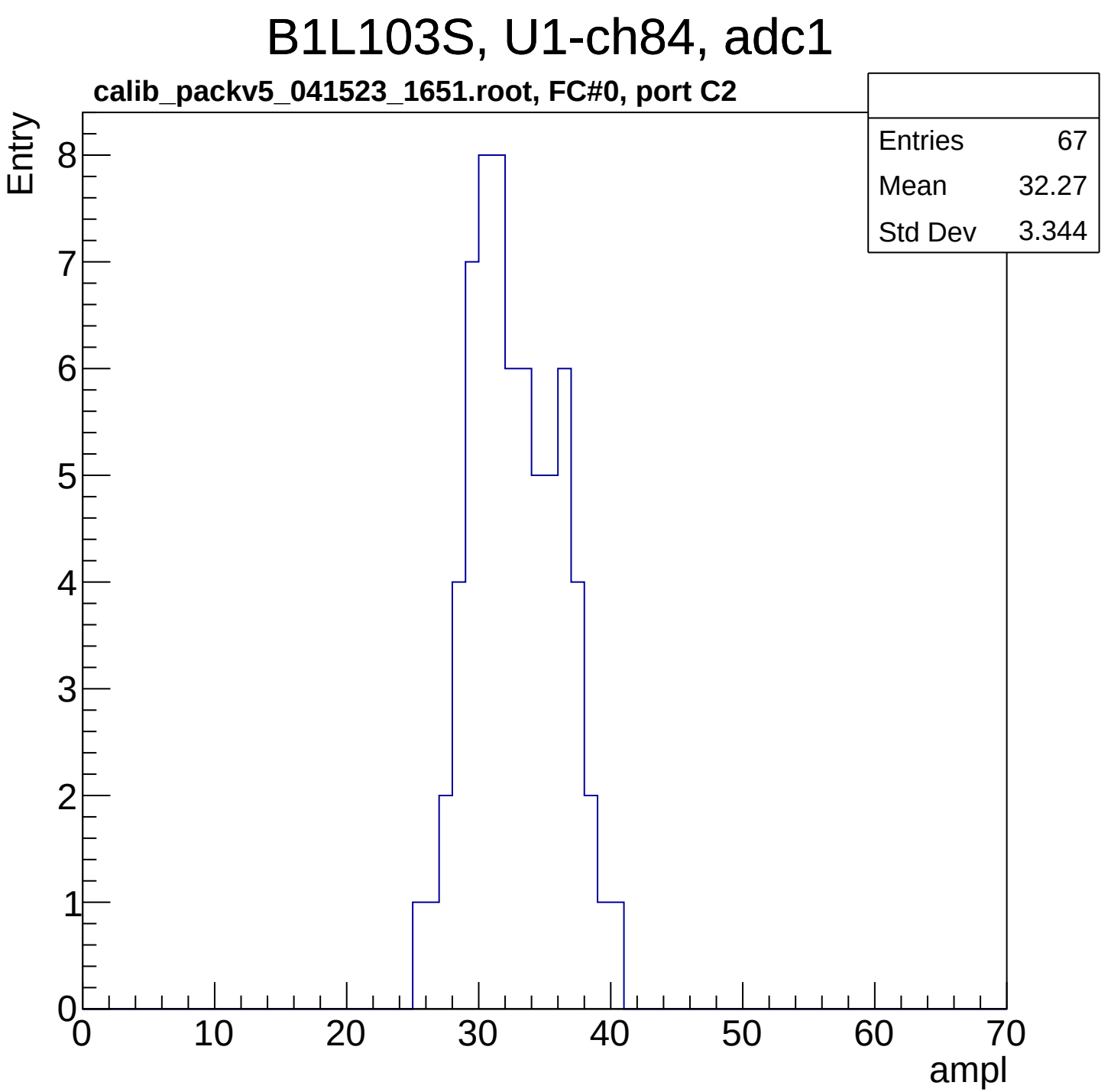
50
60
70
ampl


B1L103S, U1-ch84, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 32.27
Std Dev 3.344
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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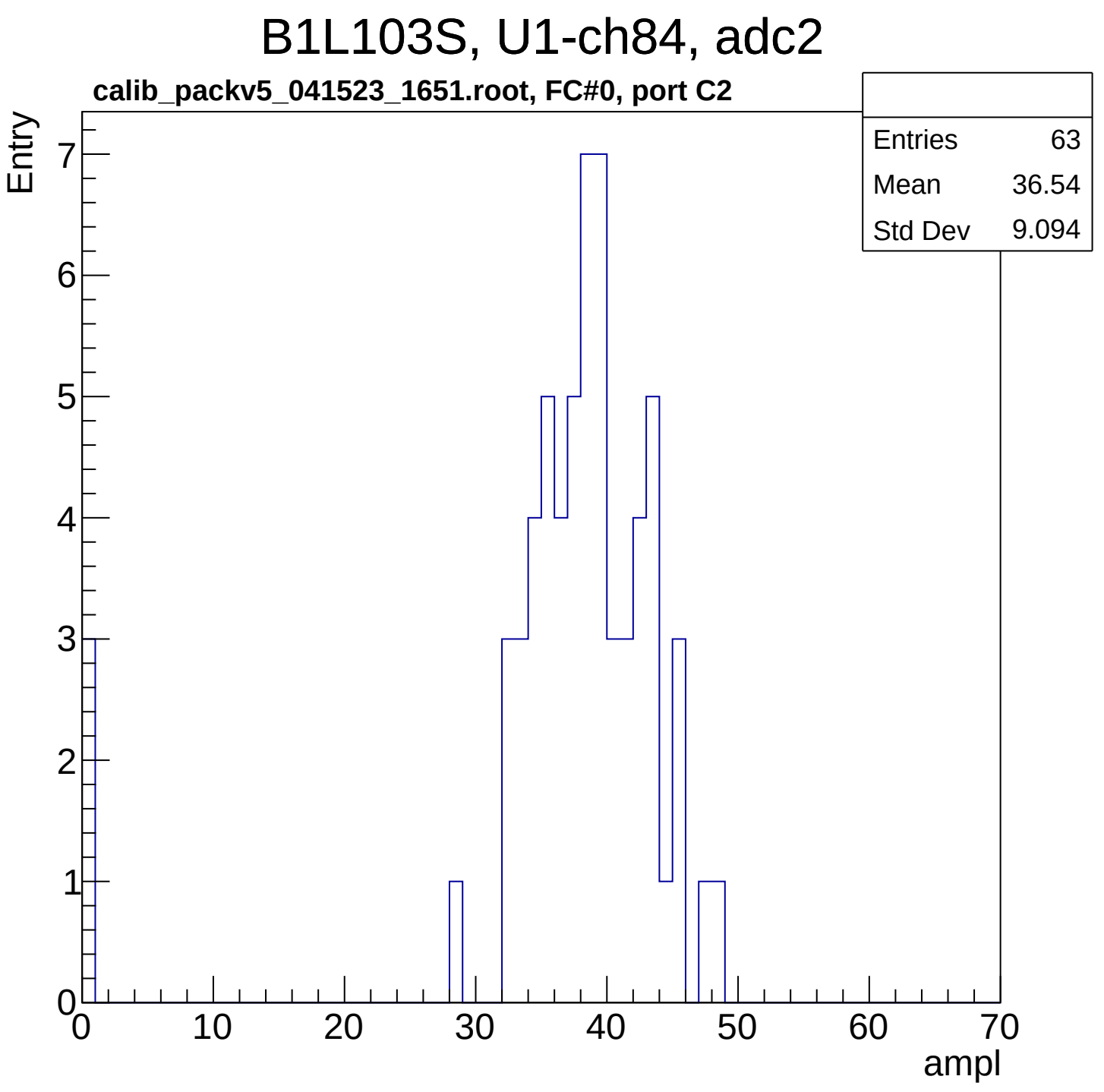
40
50
60
70


B1L103S, U1-ch84, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 36.54
Std Dev 9.094
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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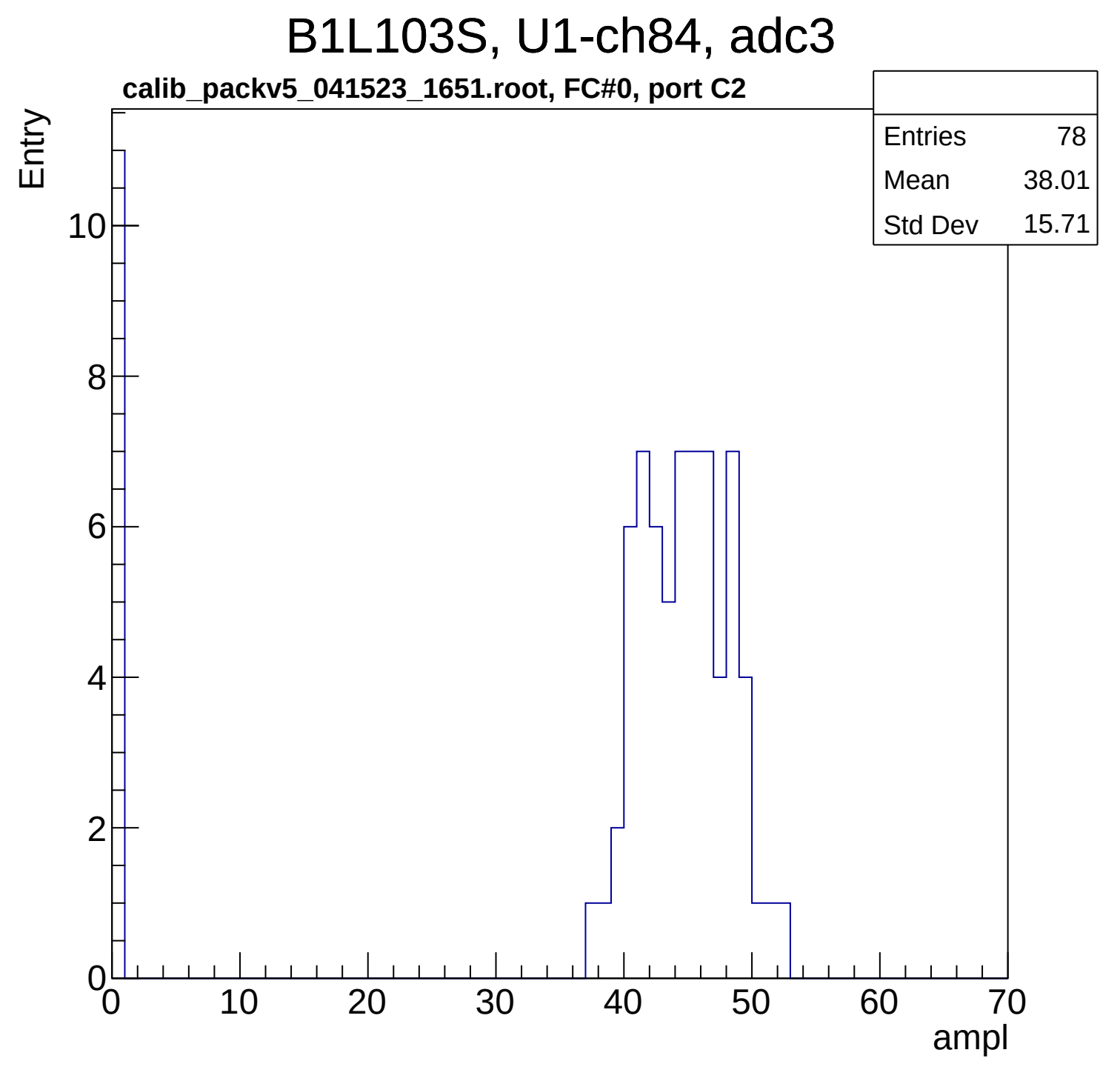
B1L103S, U1-ch84, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 38.01
Std Dev 15.71
Entry
ampl
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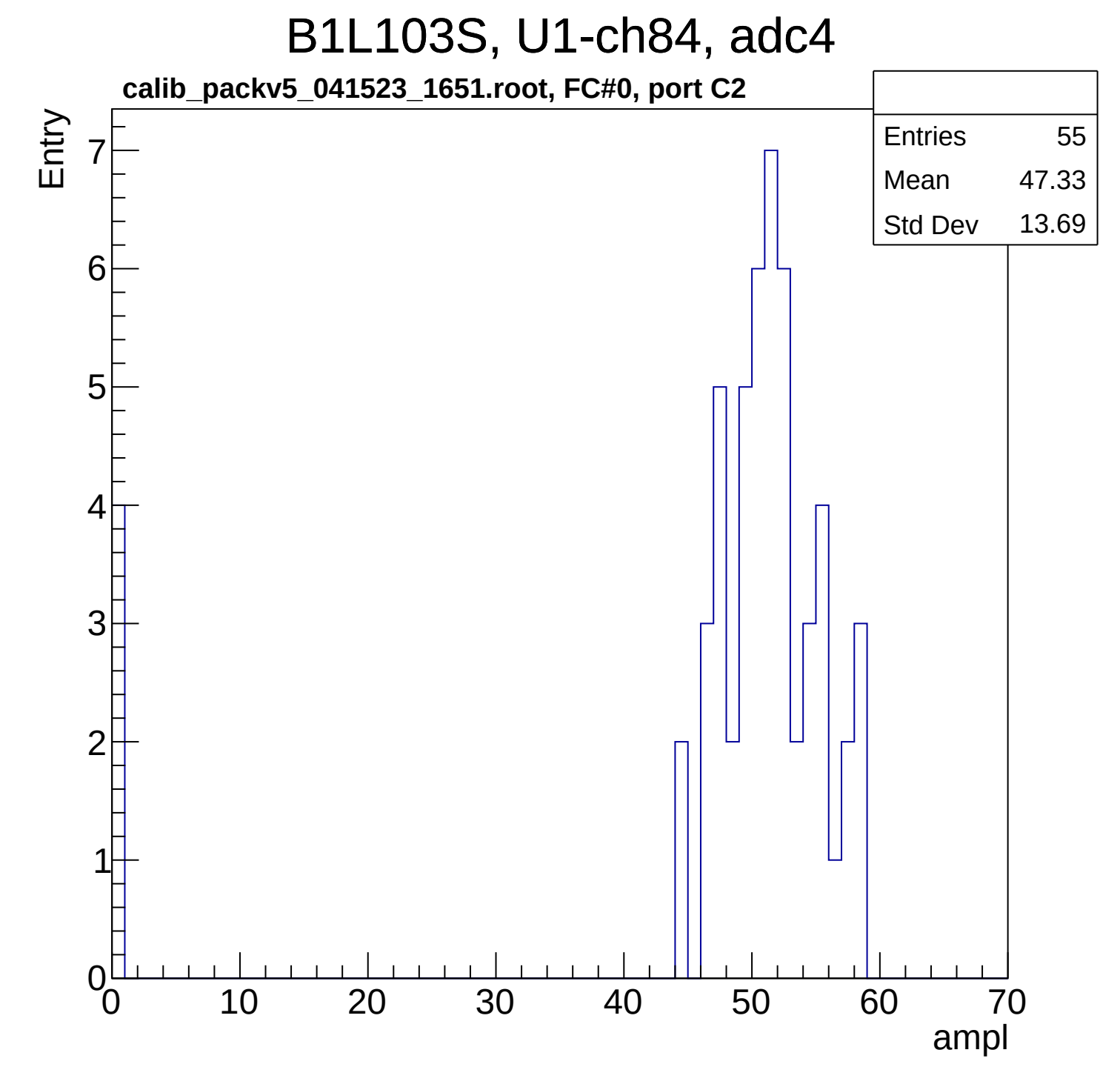
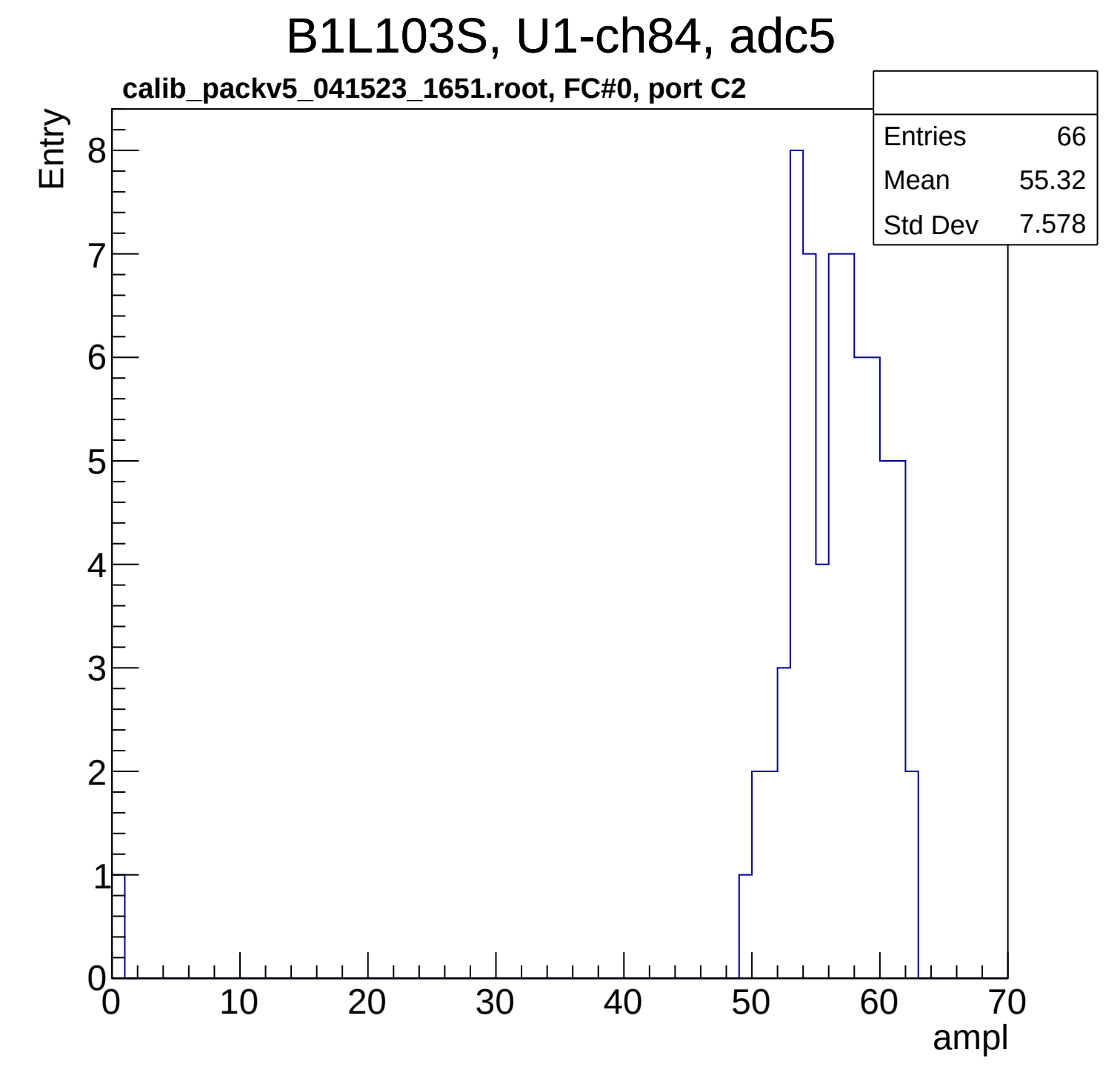
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U1-ch84, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 47.33
Std Dev 13.69
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U1-ch84, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 55.32
Std Dev 7.578
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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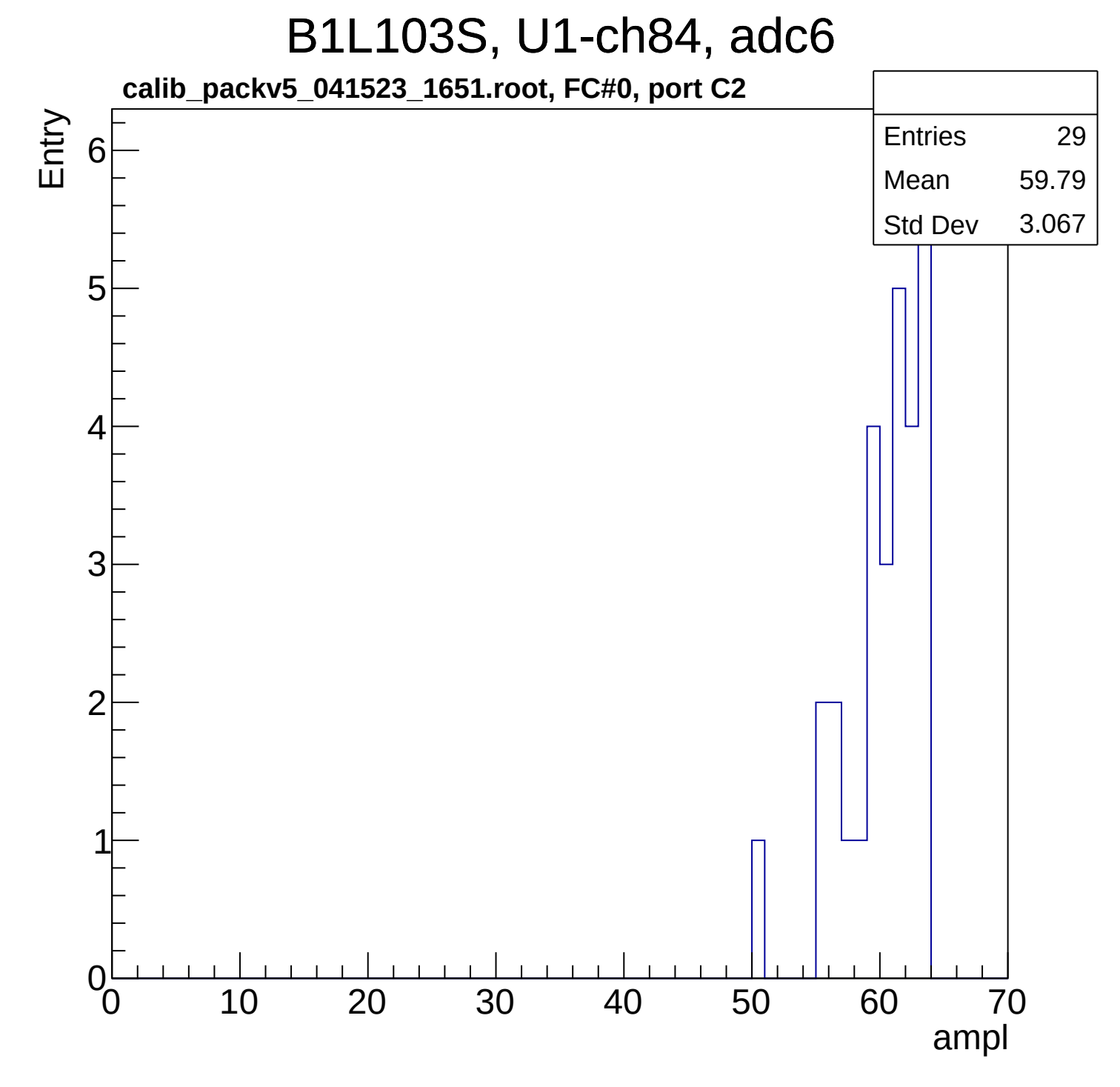
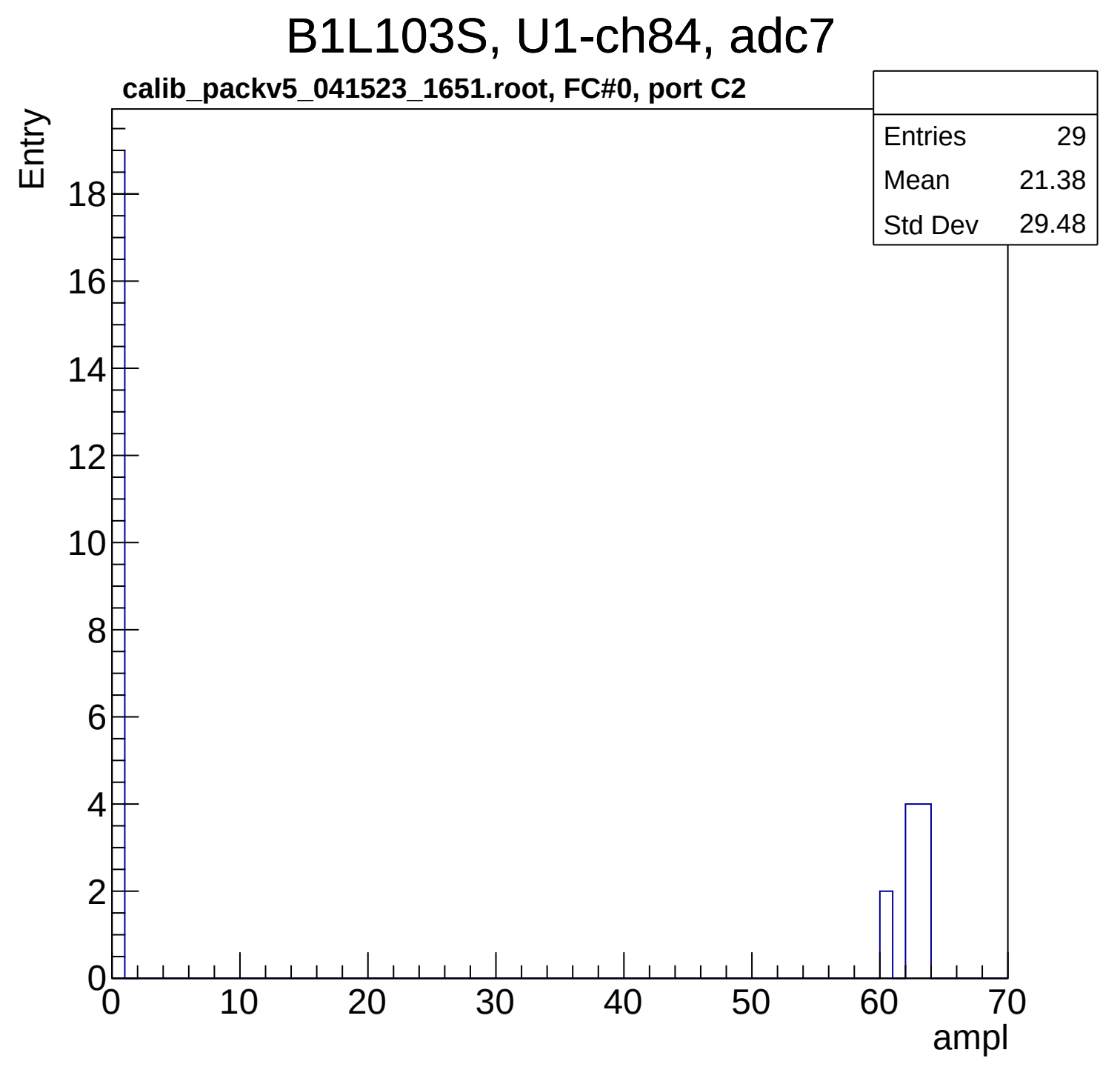
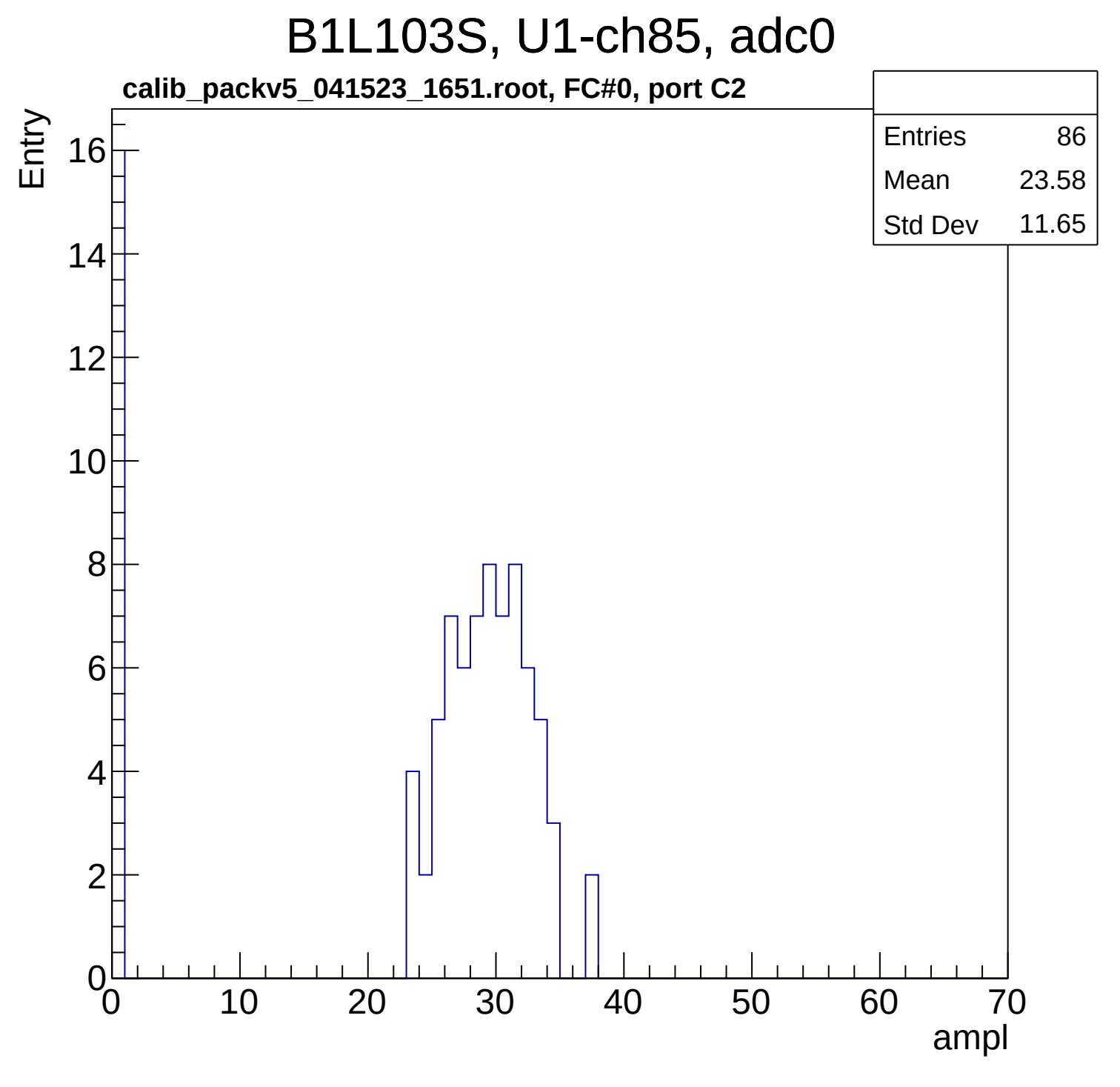

B1L103S, U1-ch84, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 29
Mean 59.79
Std Dev 3.067
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U1-ch84, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 29
Mean 21.38
Std Dev 29.48
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch85, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 23.58
Std Dev 11.65
Entry
ampl
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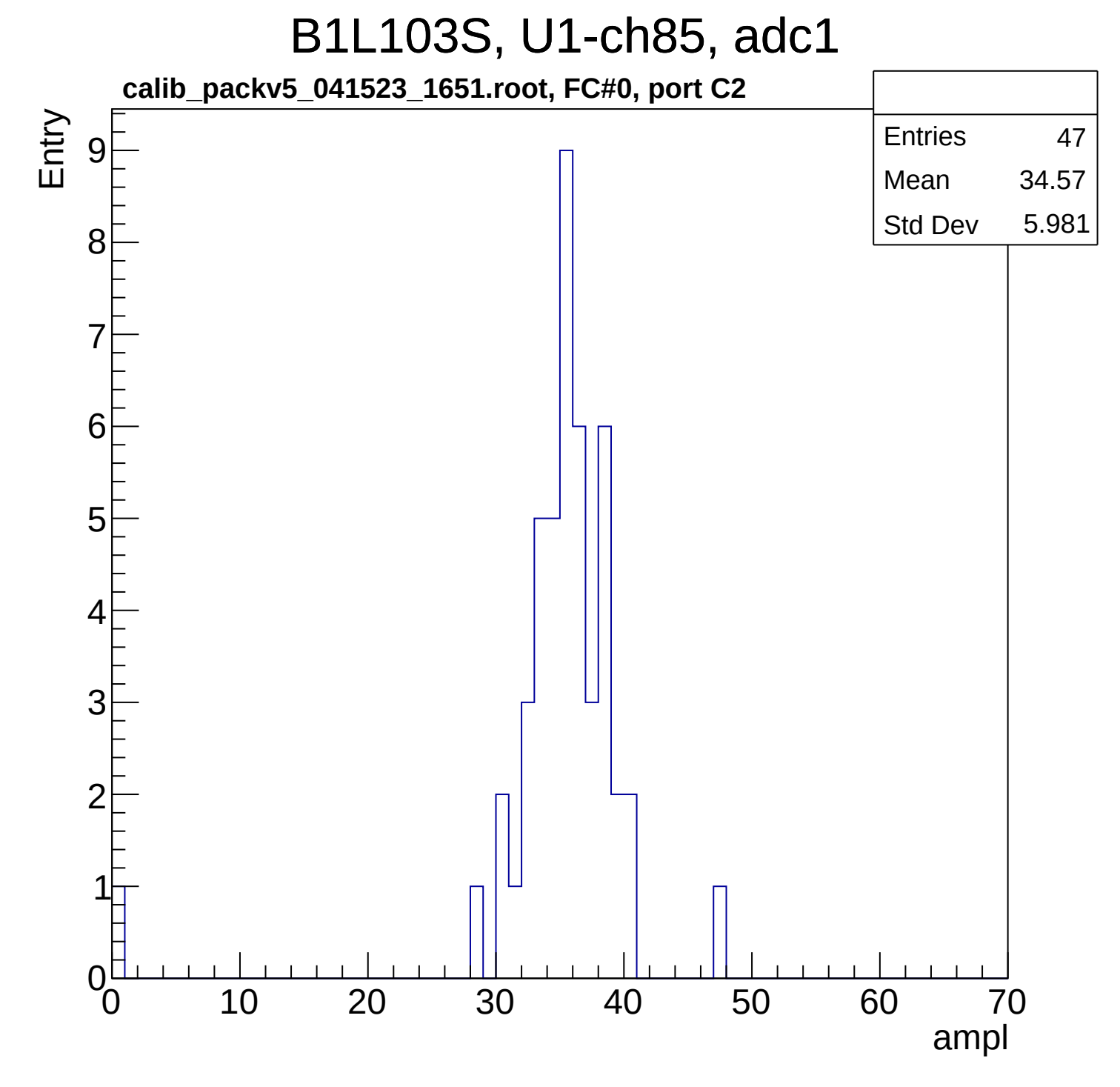
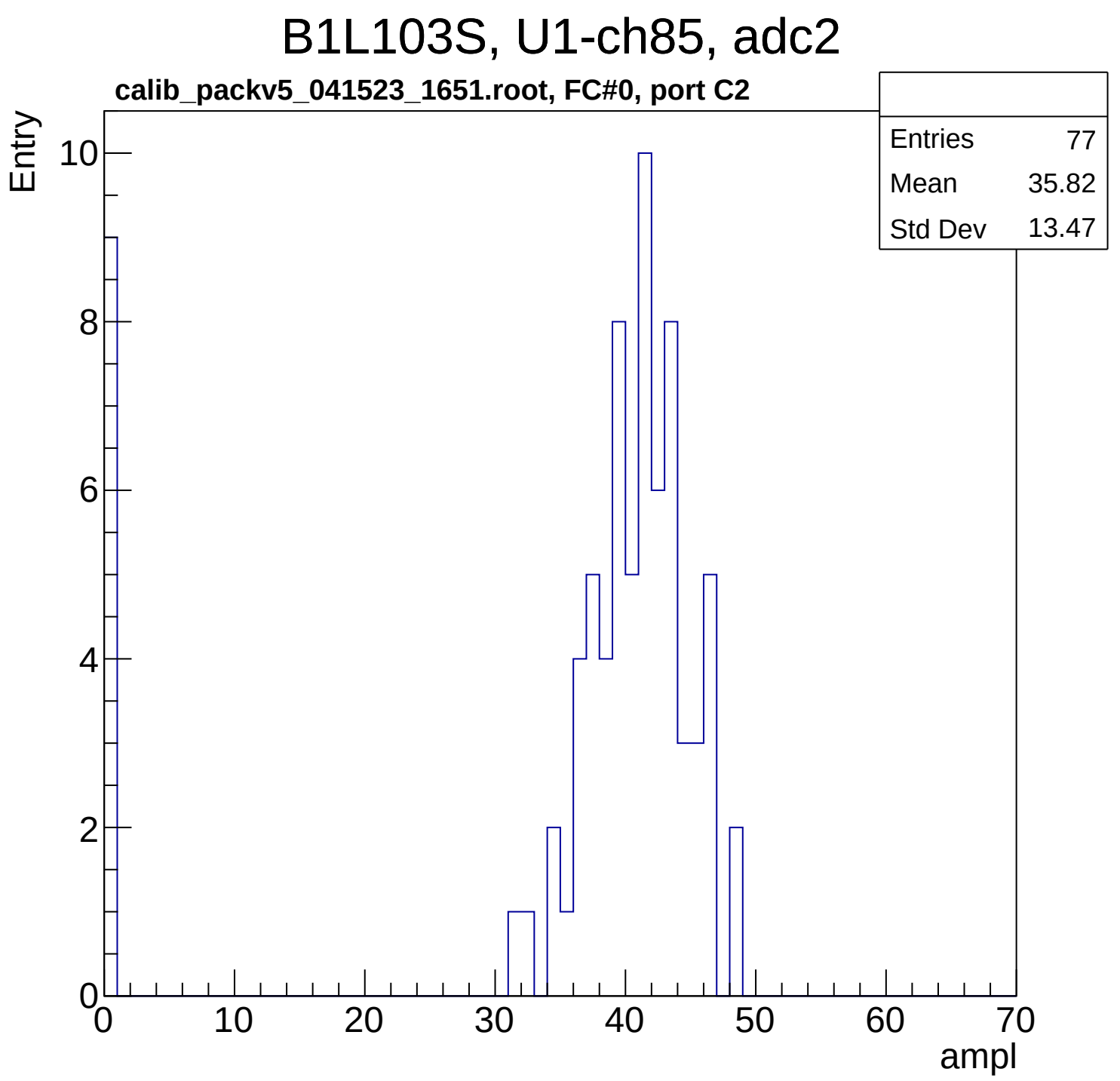
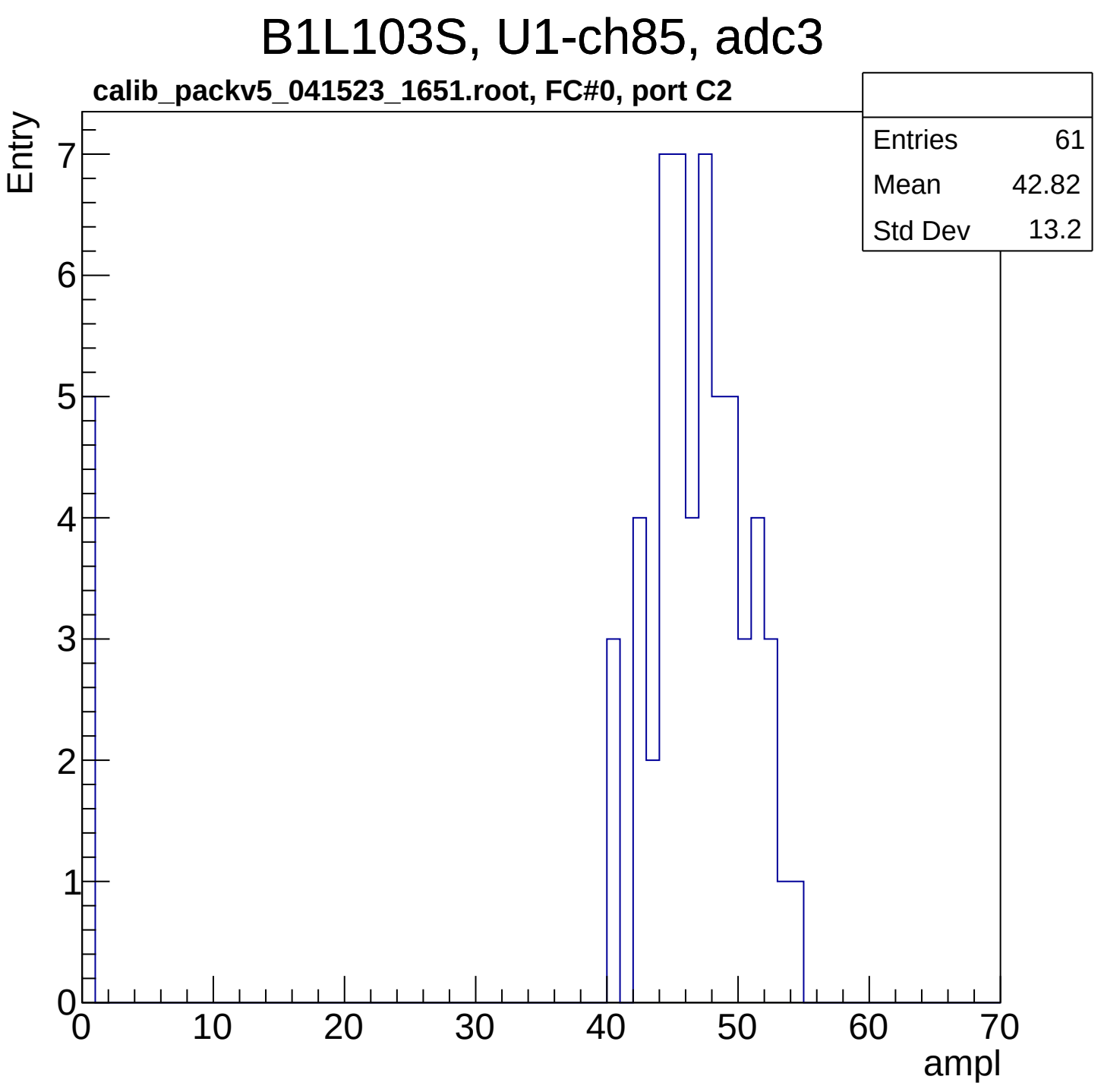
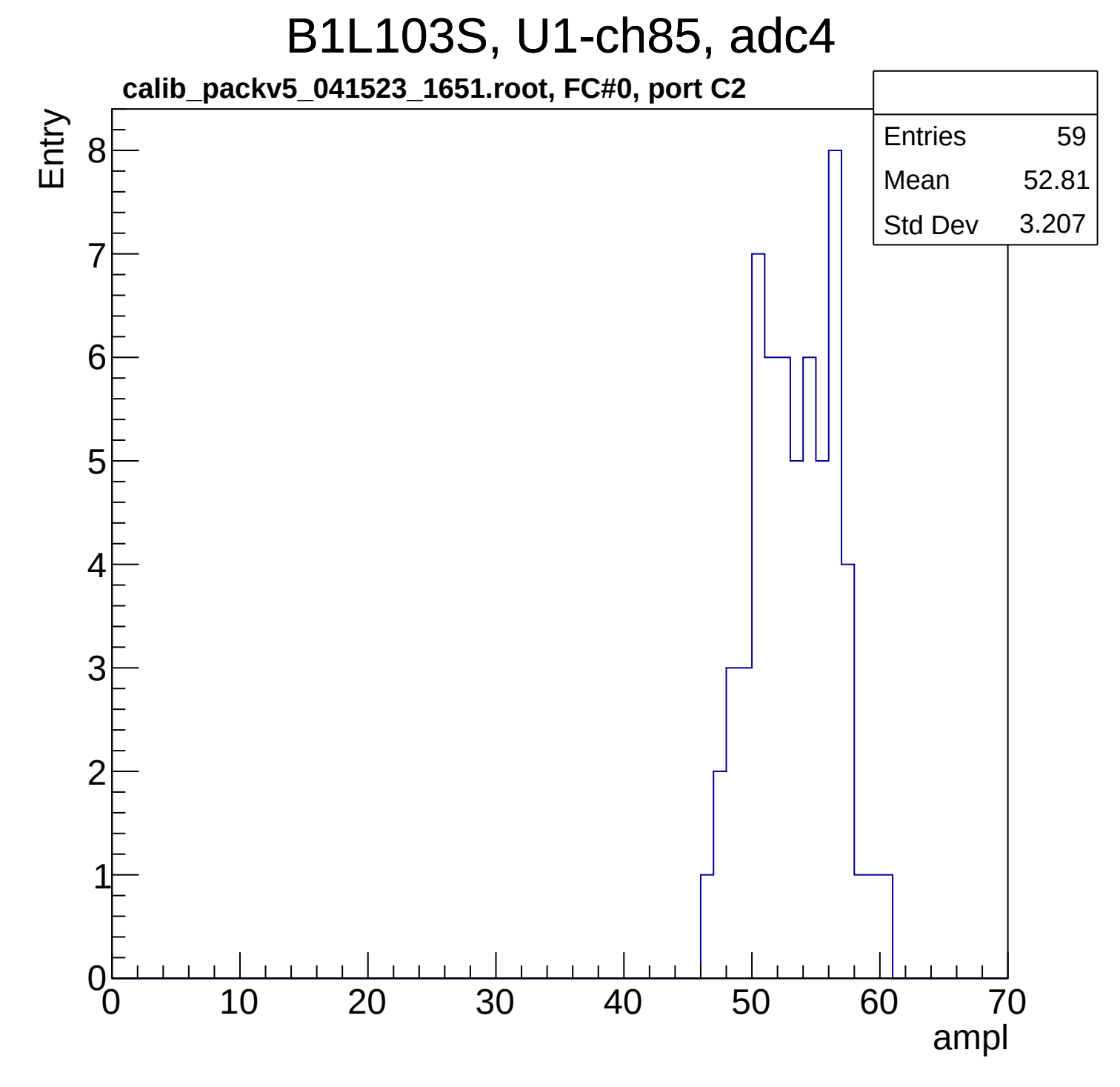
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70


B1L103S, U1-ch85, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 34.57
Std Dev 5.981
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U1-ch85, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 35.82
Std Dev 13.47
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U1-ch85, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 42.82
Std Dev 13.2
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U1-ch85, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 52.81
Std Dev 3.207
Entry
ampl
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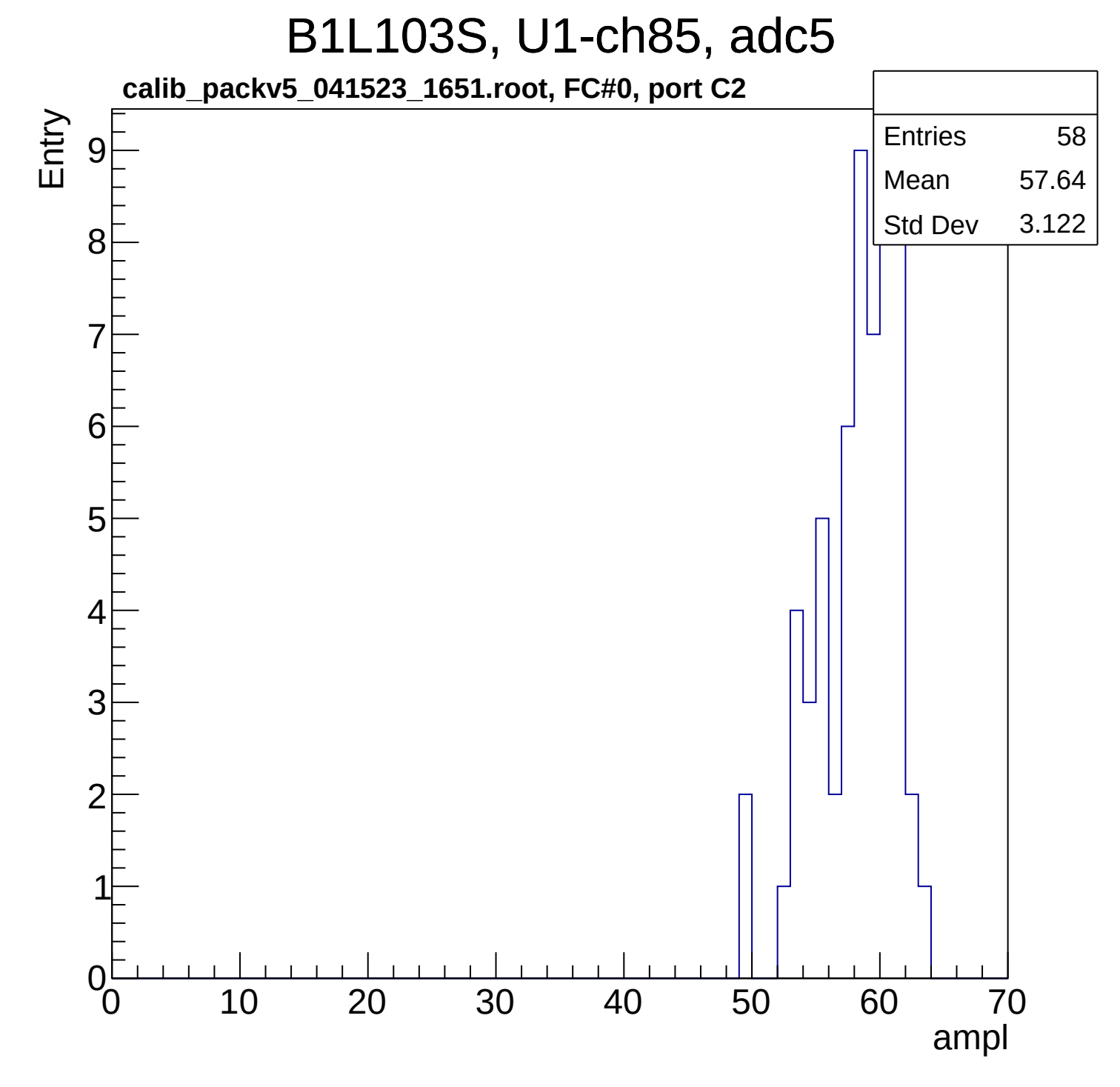
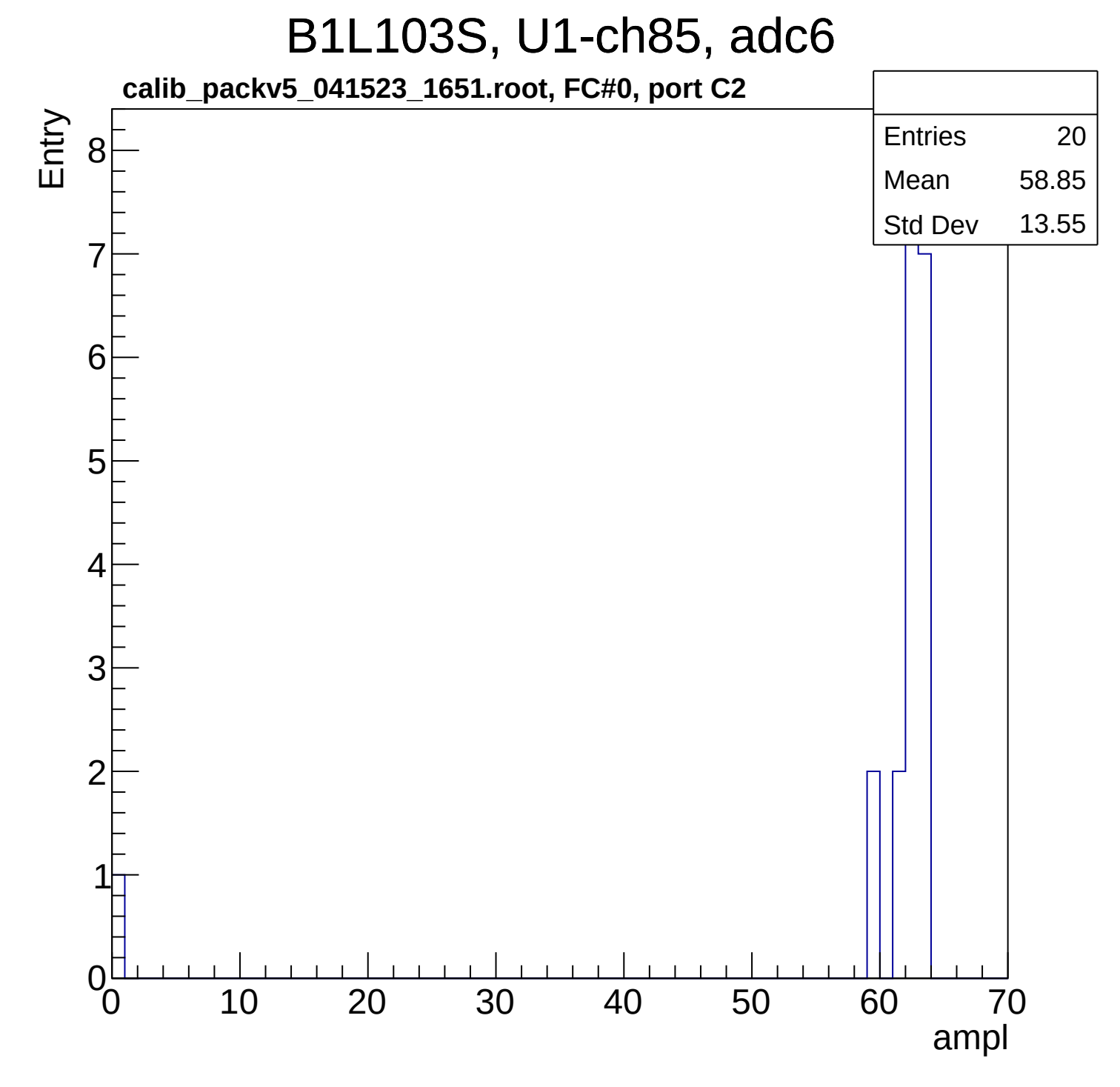
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U1-ch85, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 57.64
Std Dev 3.122
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U1-ch85, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 58.85
Std Dev 13.55
Entry
ampl
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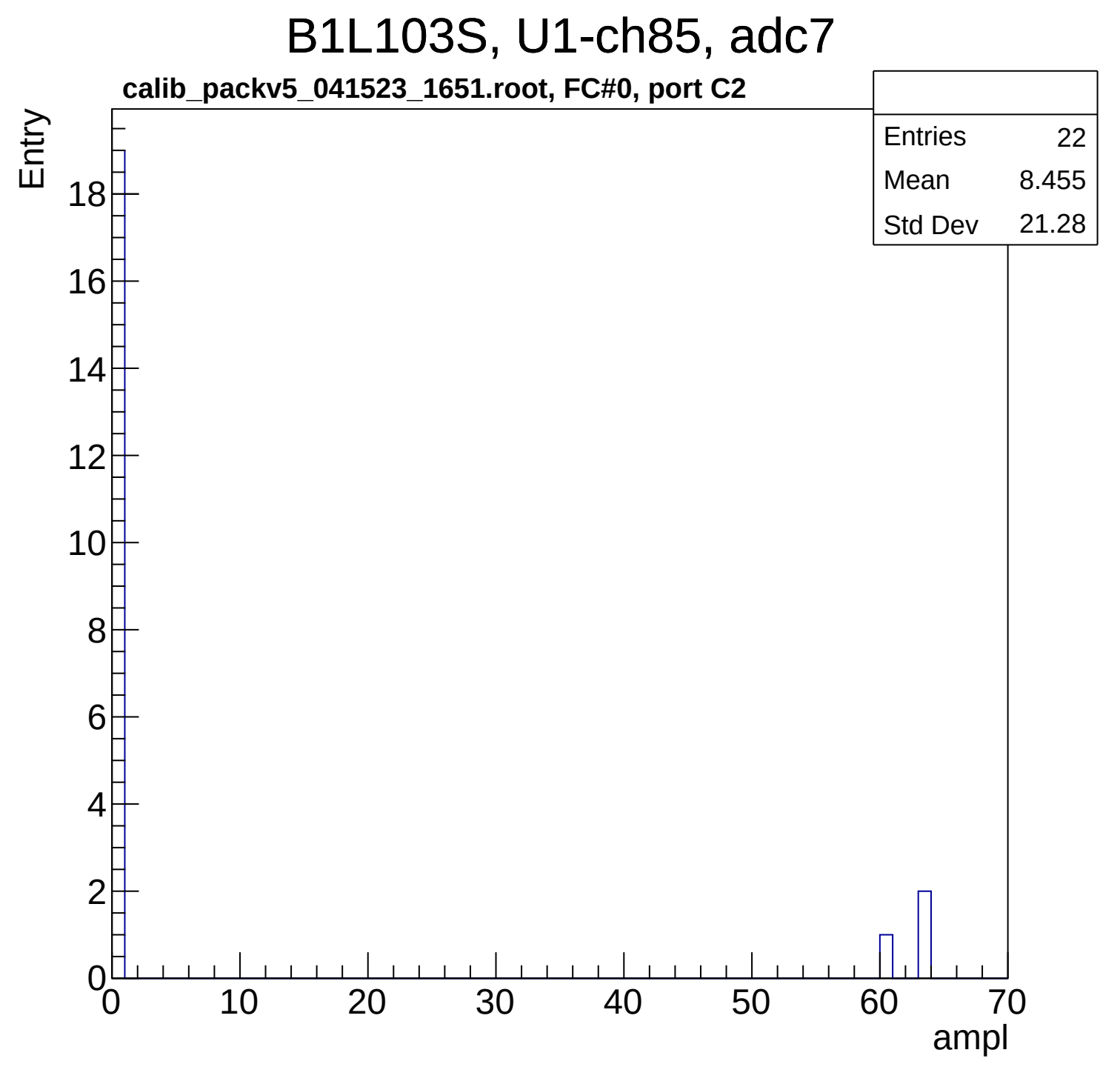
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U1-ch85, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 8.455
Std Dev 21.28
Entry
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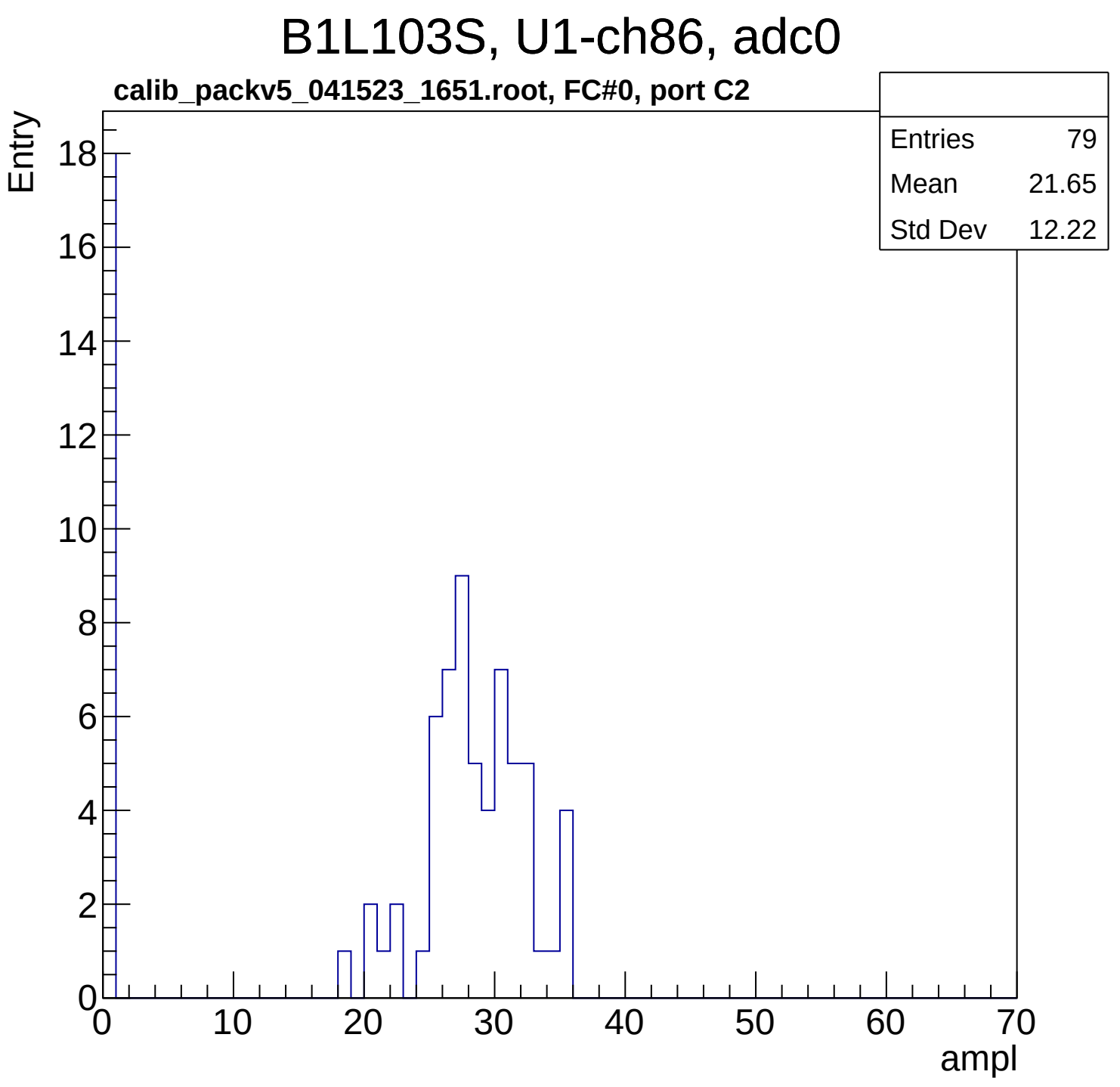
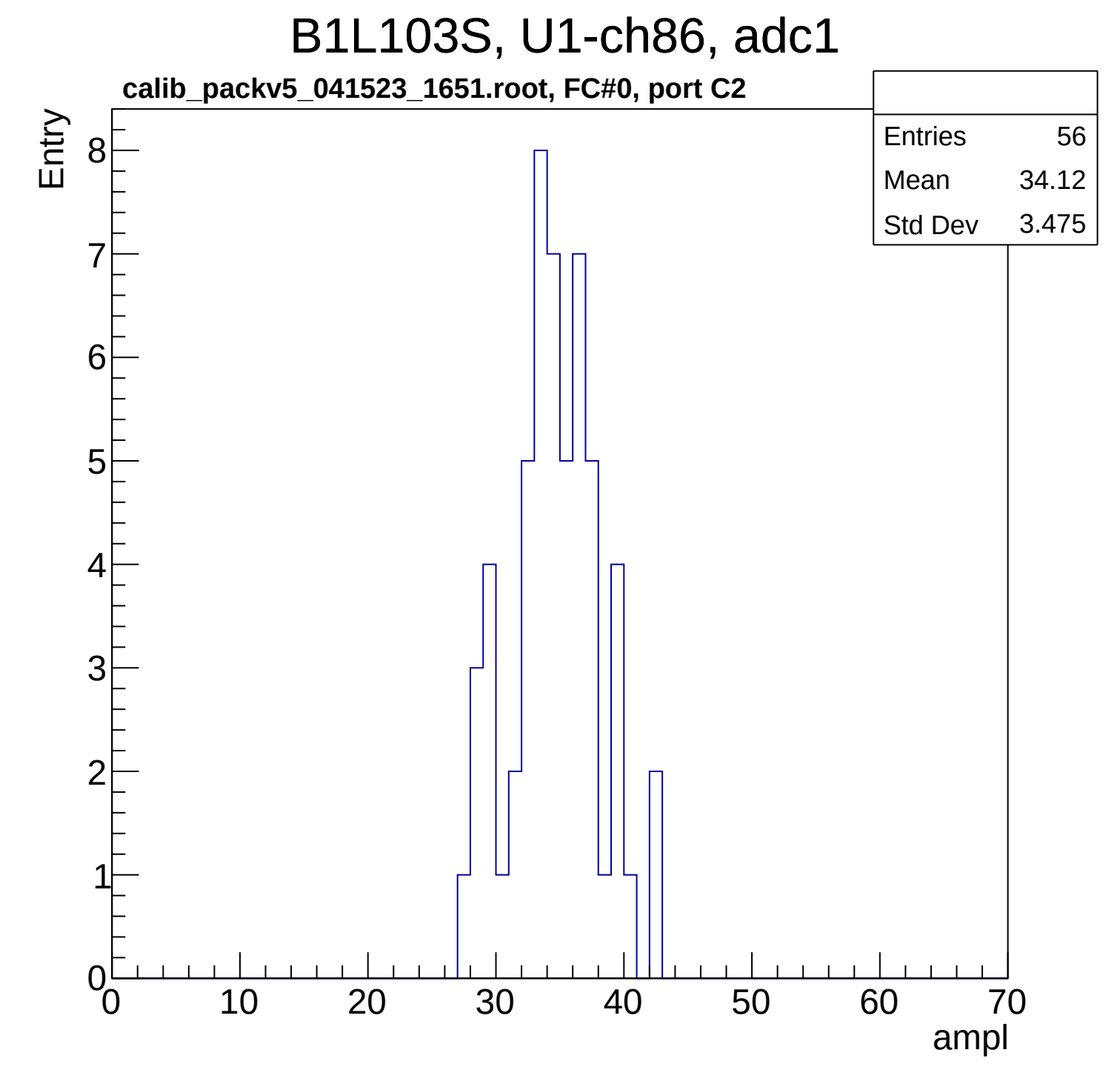
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch86, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 21.65
Std Dev 12.22
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch86, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 34.12
Std Dev 3.475
Entry
ampl
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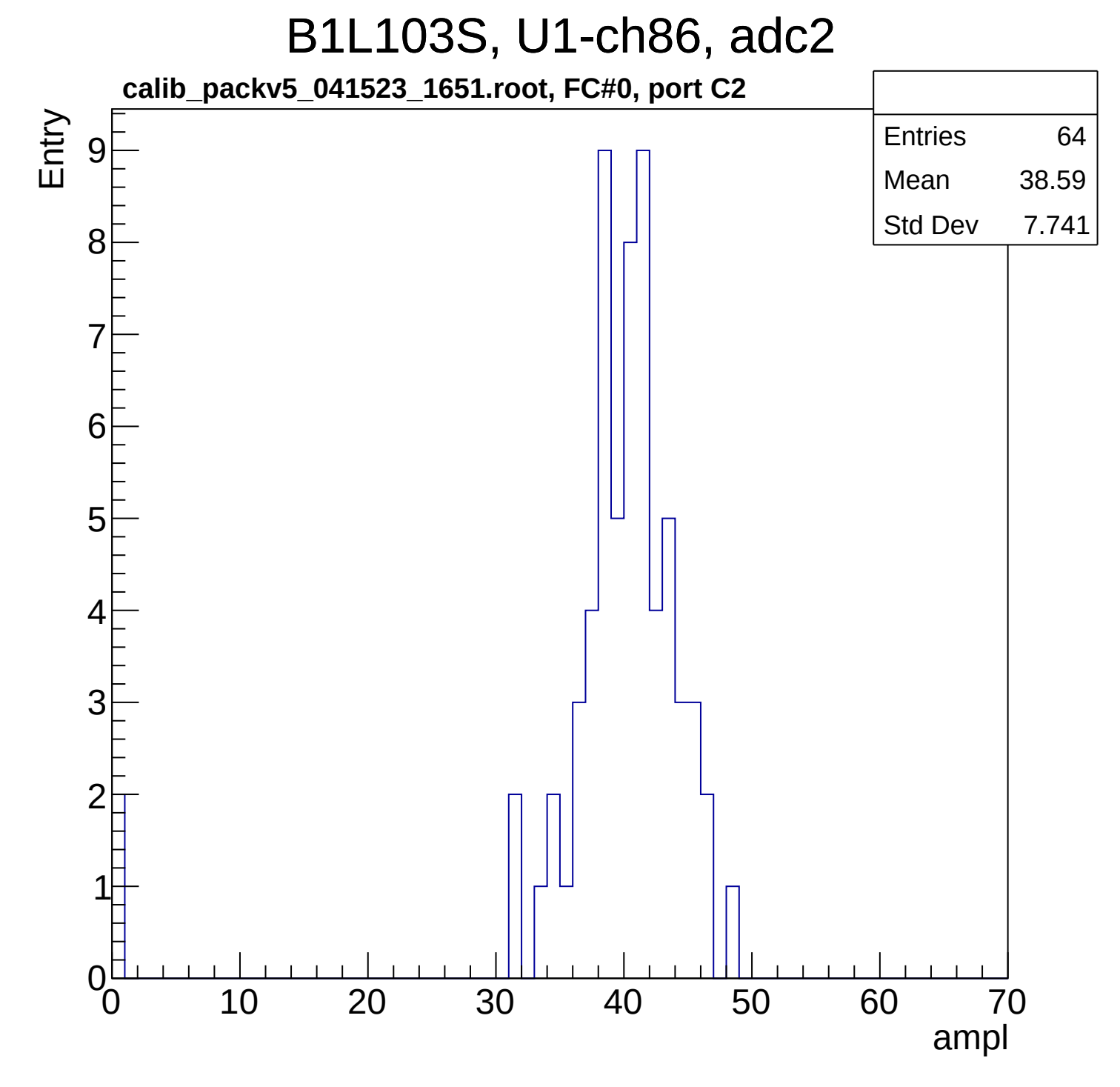
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U1-ch86, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 38.59
Std Dev 7.741
Entry
ampl
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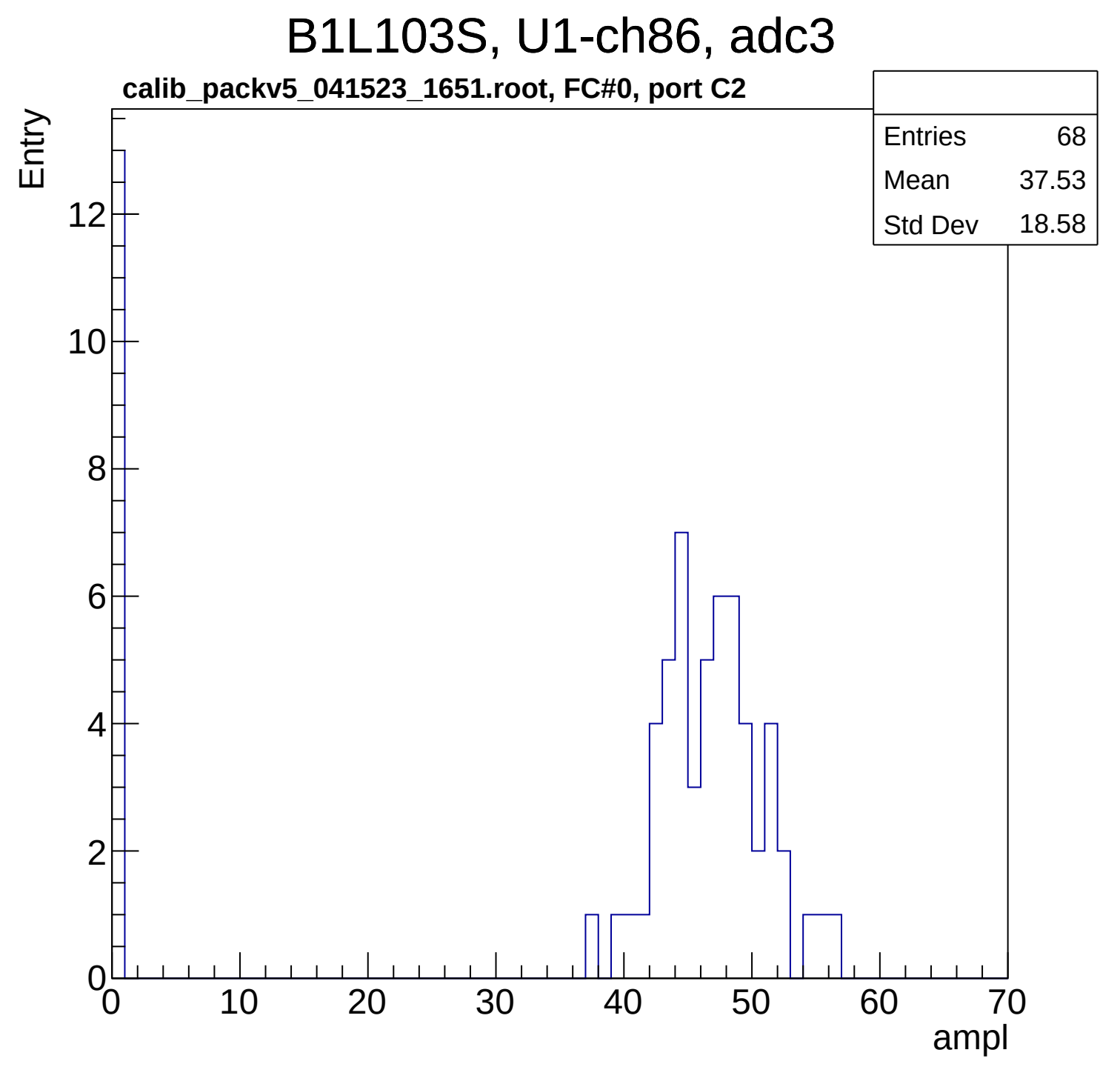
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U1-ch86, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 37.53
Std Dev 18.58
Entry
ampl
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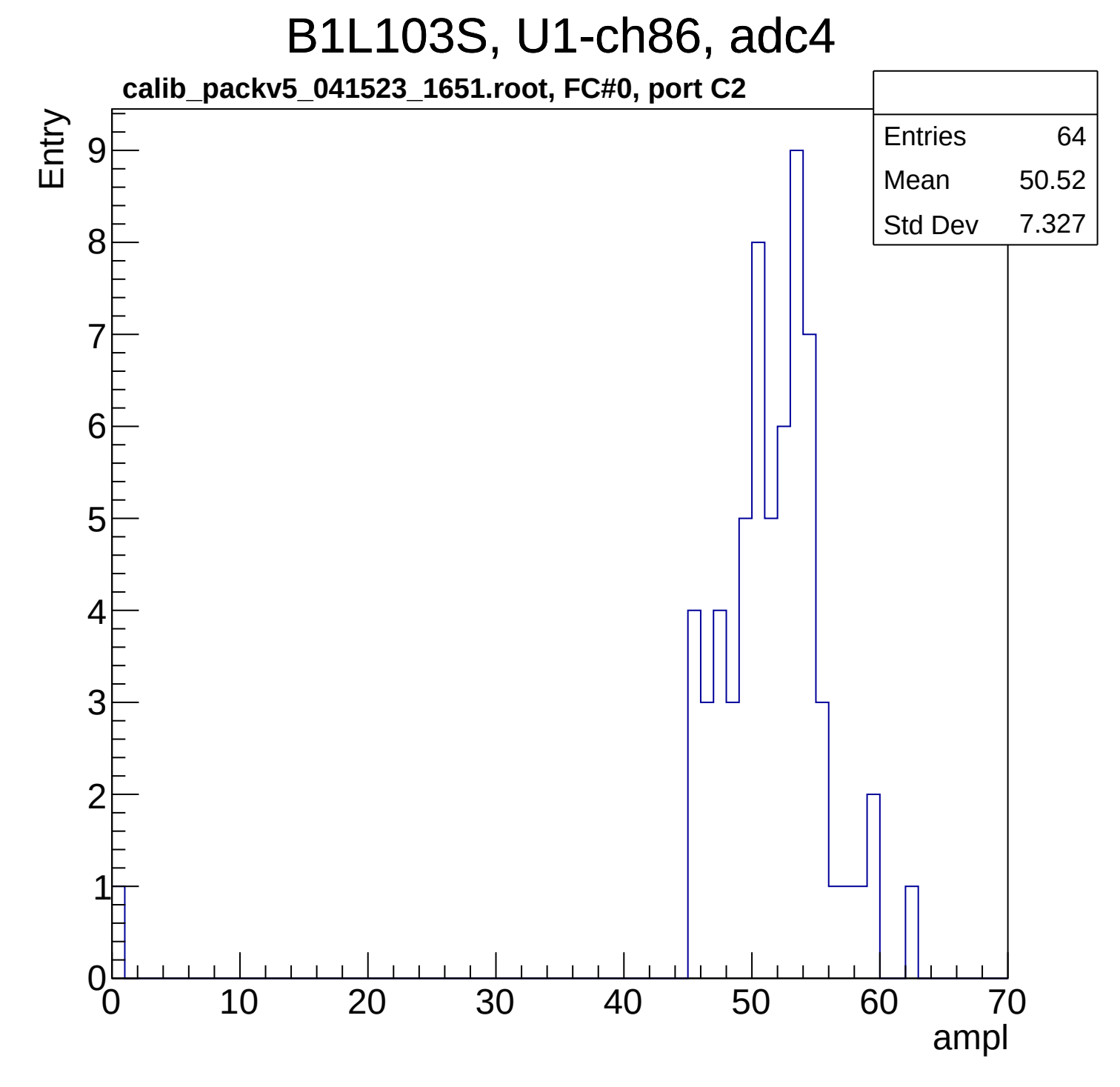
2
4
6
8
10
12
0
10
20
30
40
50
60
70


B1L103S, U1-ch86, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 50.52
Std Dev 7.327
Entry
ampl
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10
20
30
40
50
60
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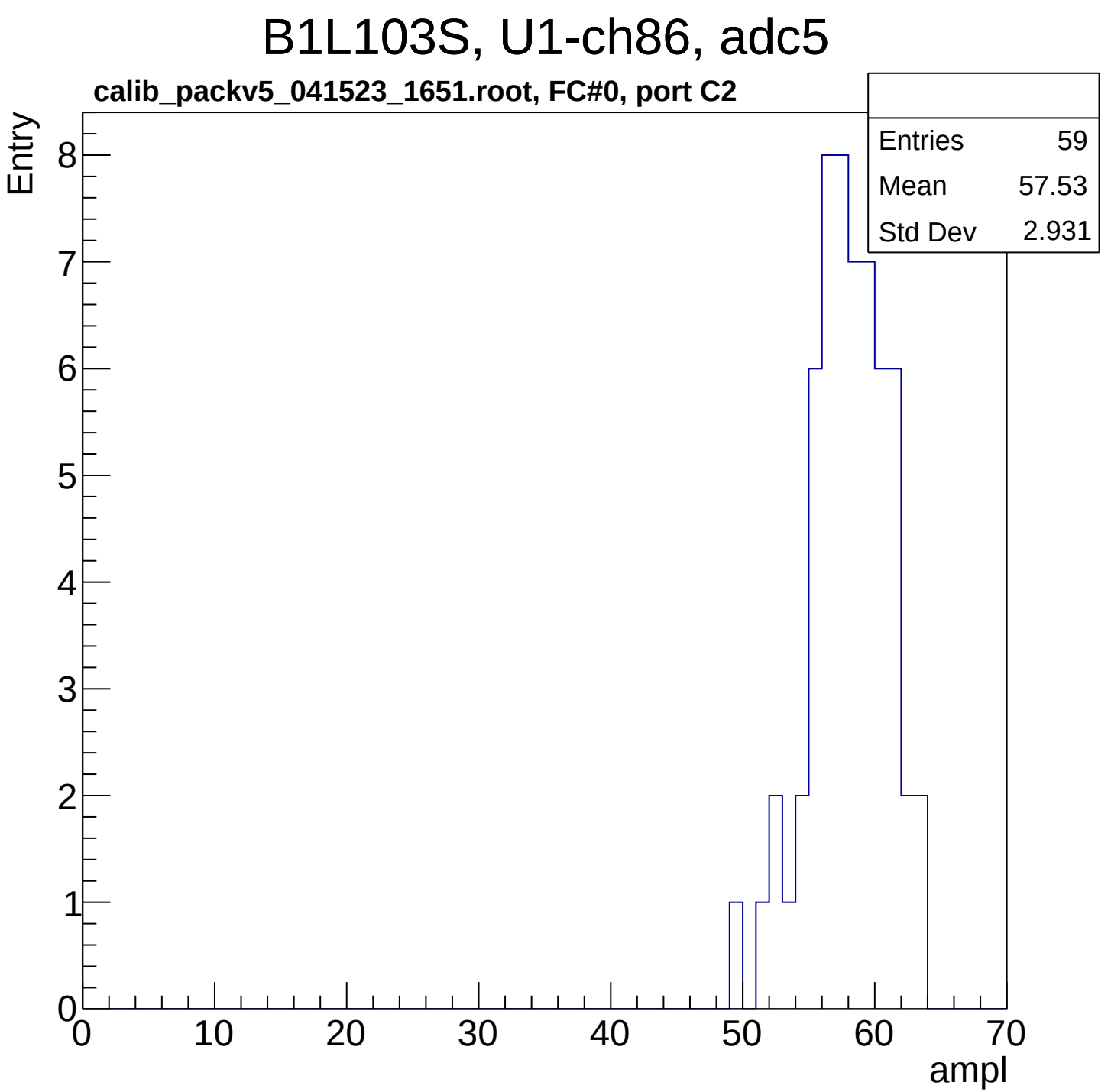
1
2
3
4
5
6
7
8
9


B1L103S, U1-ch86, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 57.53
Std Dev 2.931
Entry
ampl
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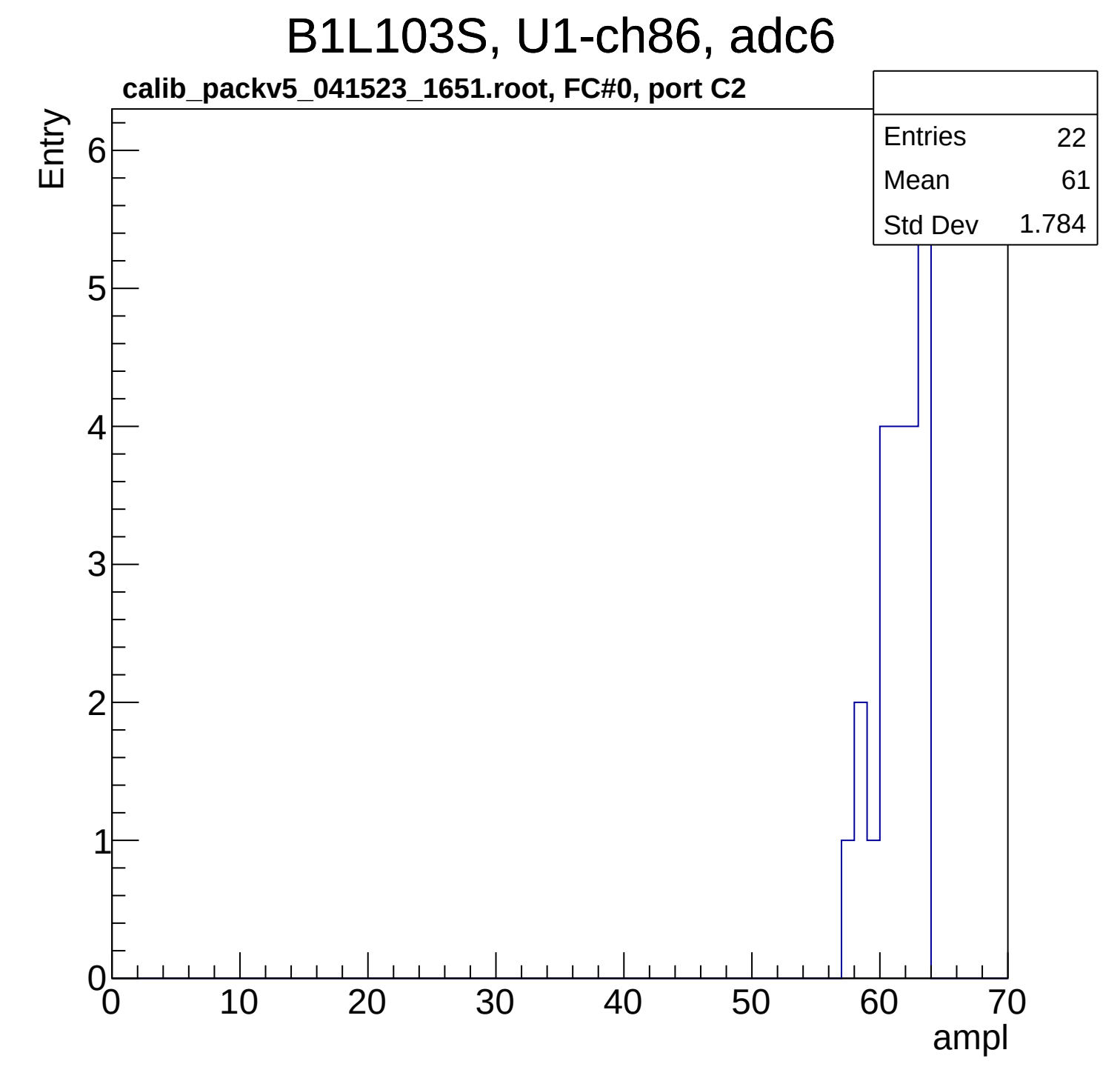
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U1-ch86, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 61
Std Dev 1.784
Entry
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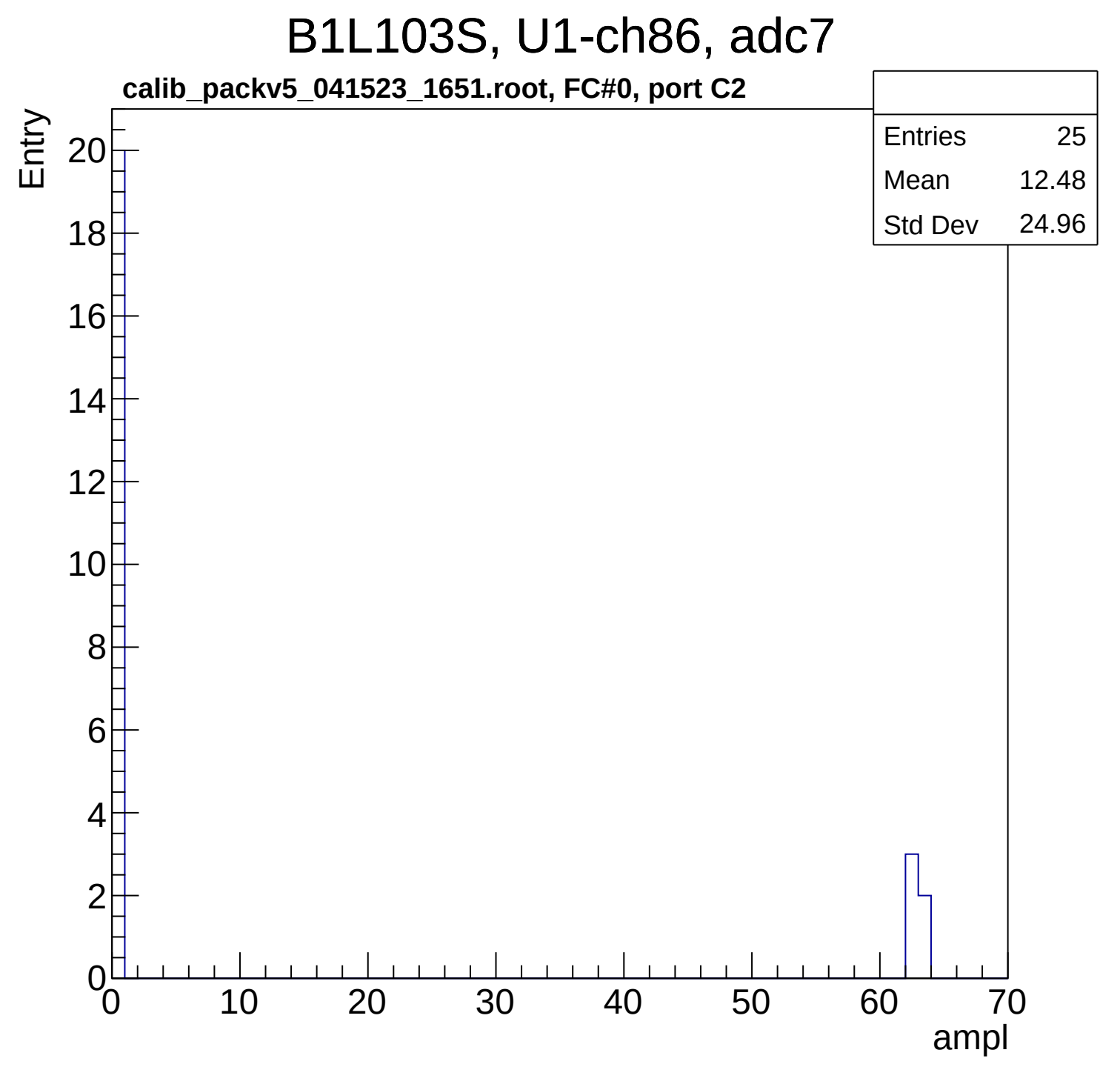
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch86, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 25
Mean 12.48
Std Dev 24.96
Entry
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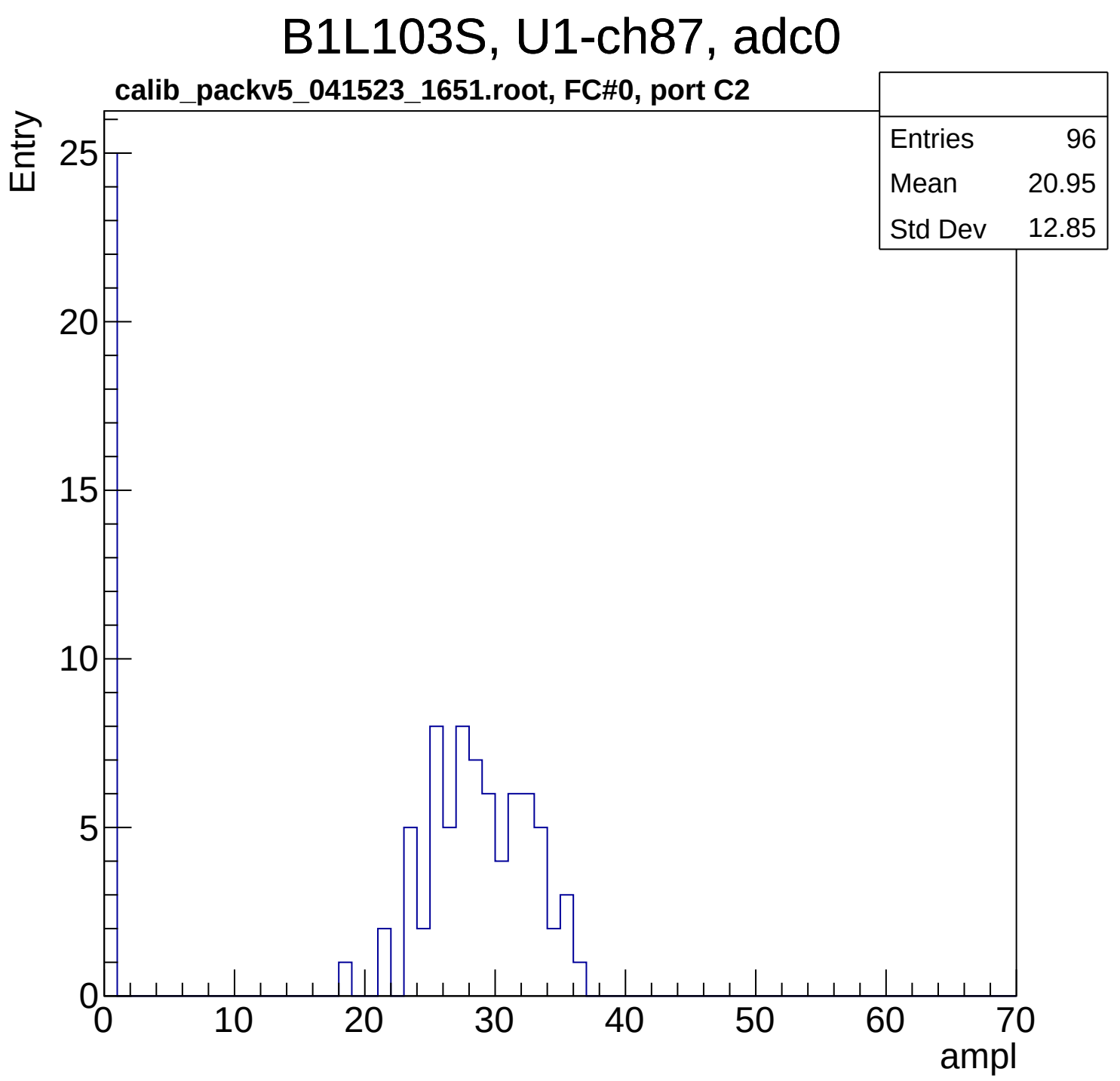
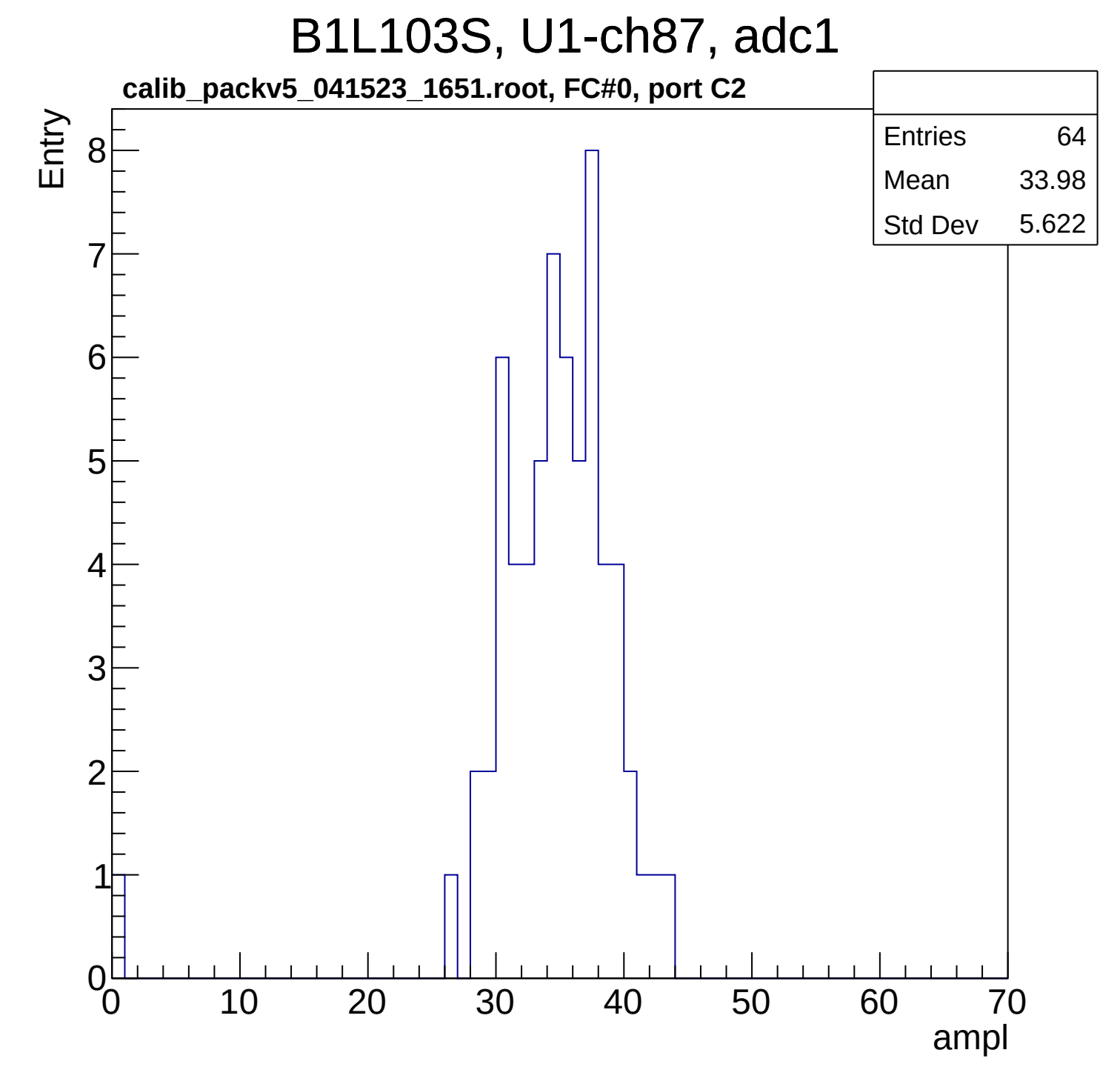
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch87, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 96
Mean 20.95
Std Dev 12.85
Entry
0
5
10
15
20
25
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch87, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 33.98
Std Dev 5.622
Entry
ampl
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1
2
3
4
5
6
7
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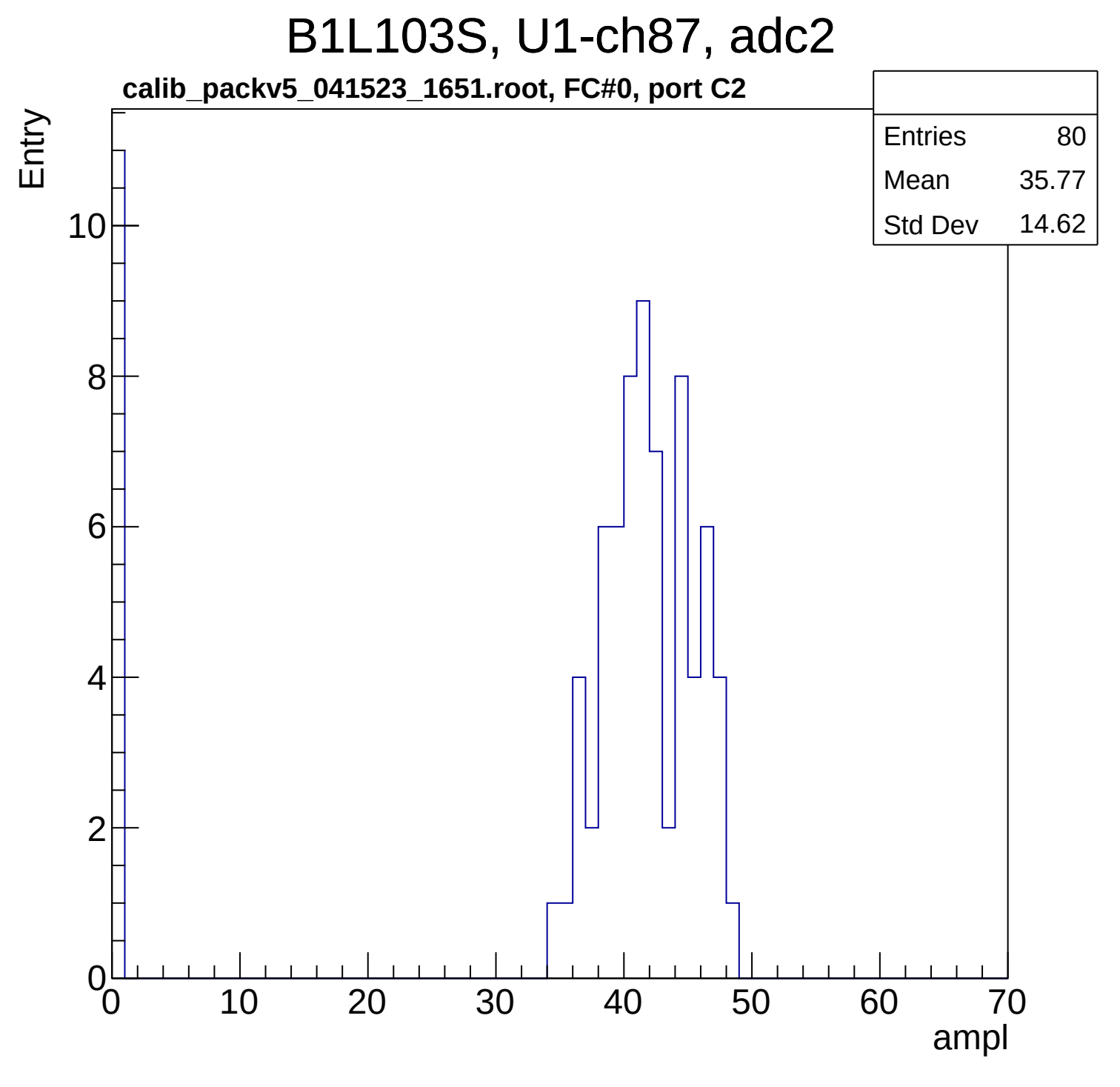
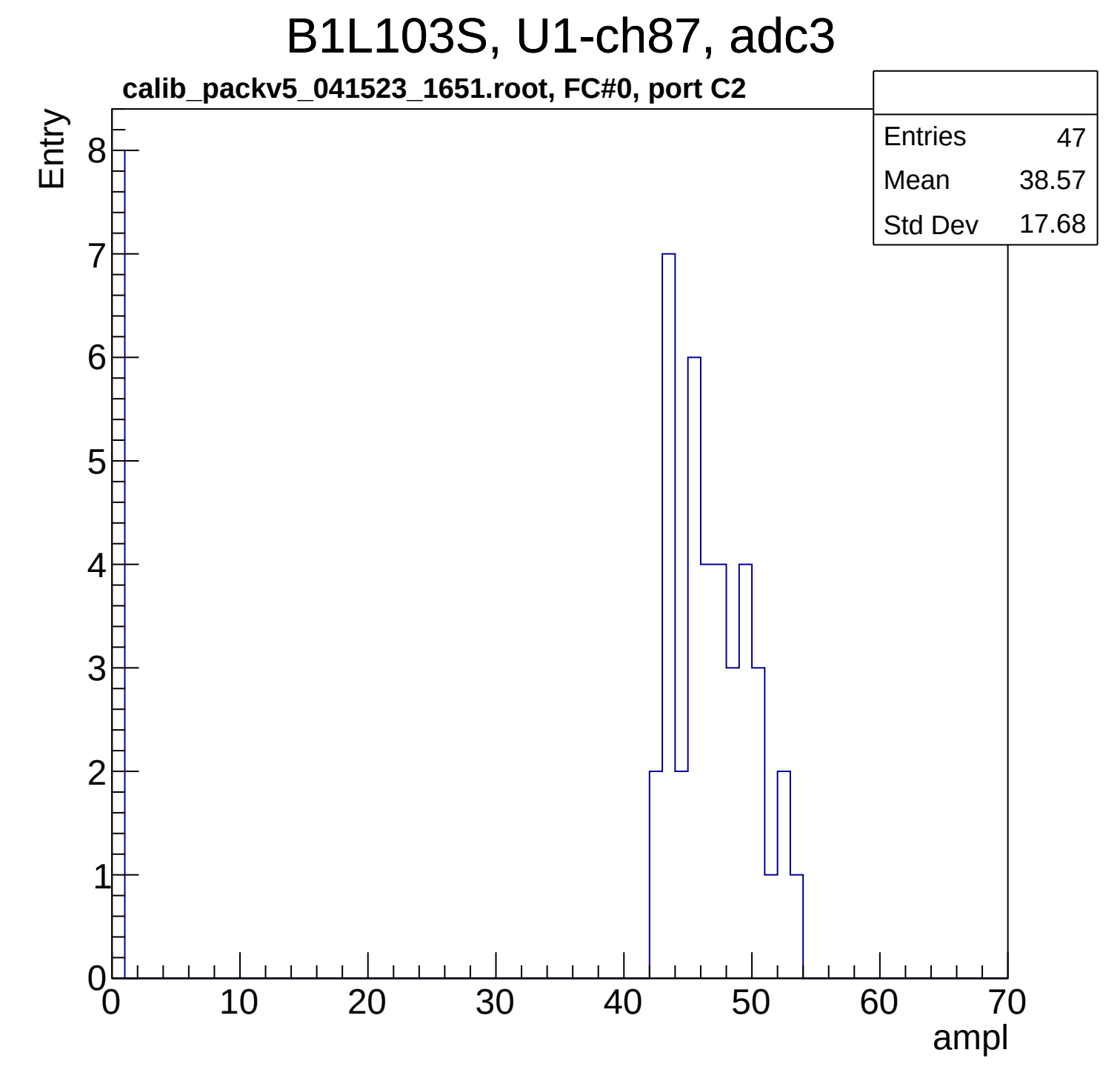
0
10
20
30
40
50
60
70


B1L103S, U1-ch87, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 35.77
Std Dev 14.62
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch87, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 38.57
Std Dev 17.68
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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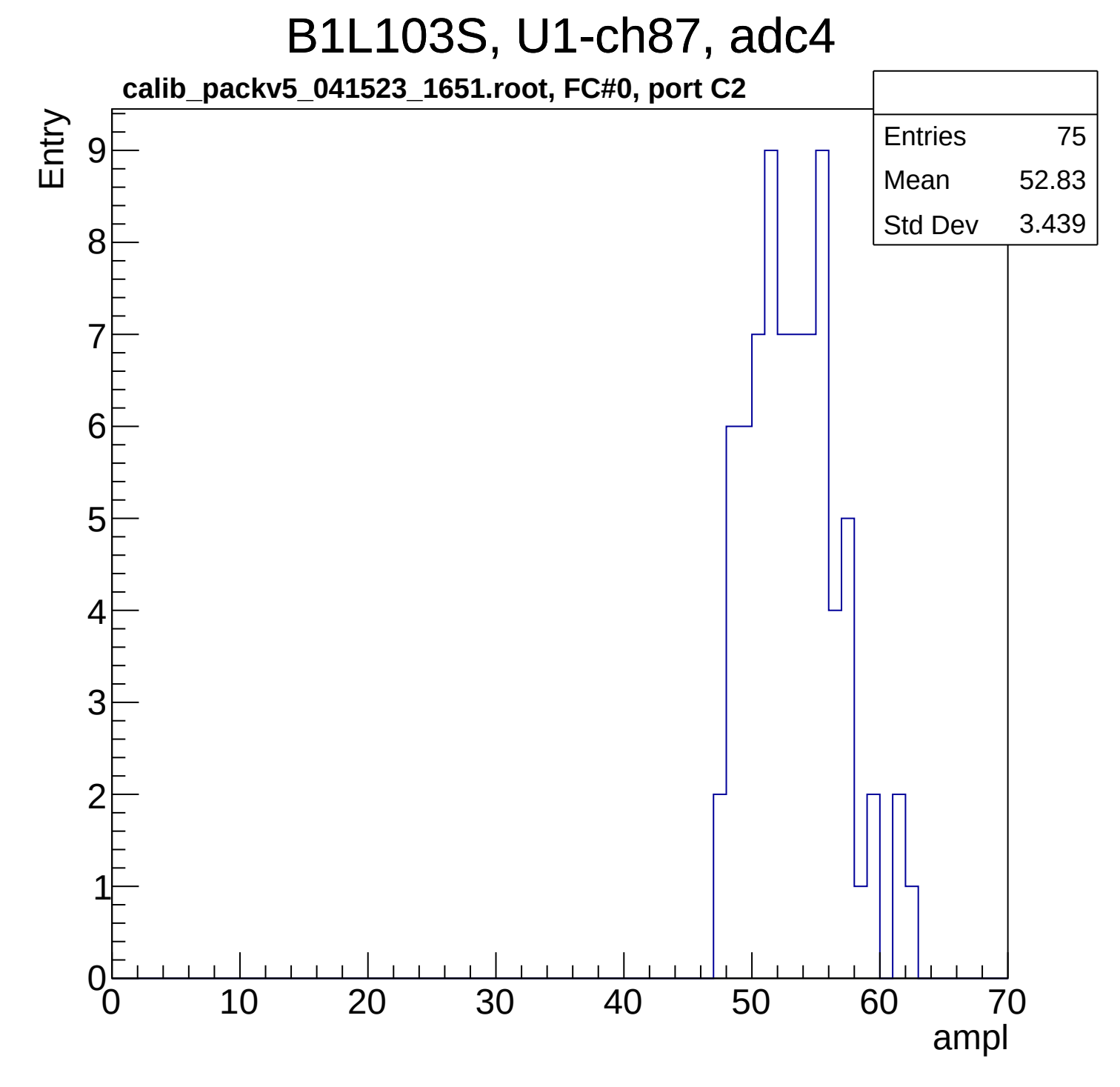
B1L103S, U1-ch87, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 52.83
Std Dev 3.439
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
50
60
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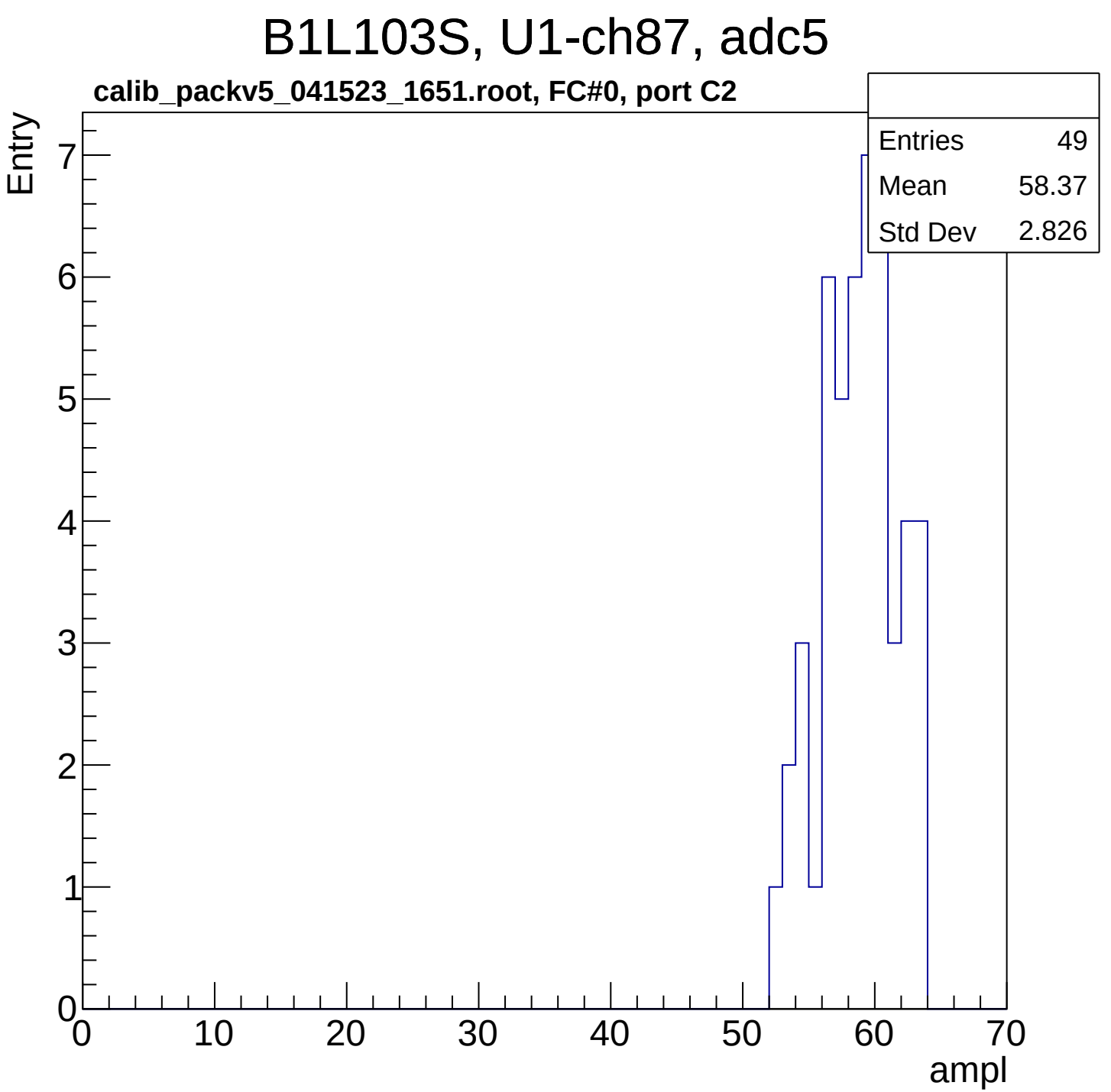
B1L103S, U1-ch87, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 58.37
Std Dev 2.826
Entry
ampl
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1
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3
4
5
6
7
0
10
20
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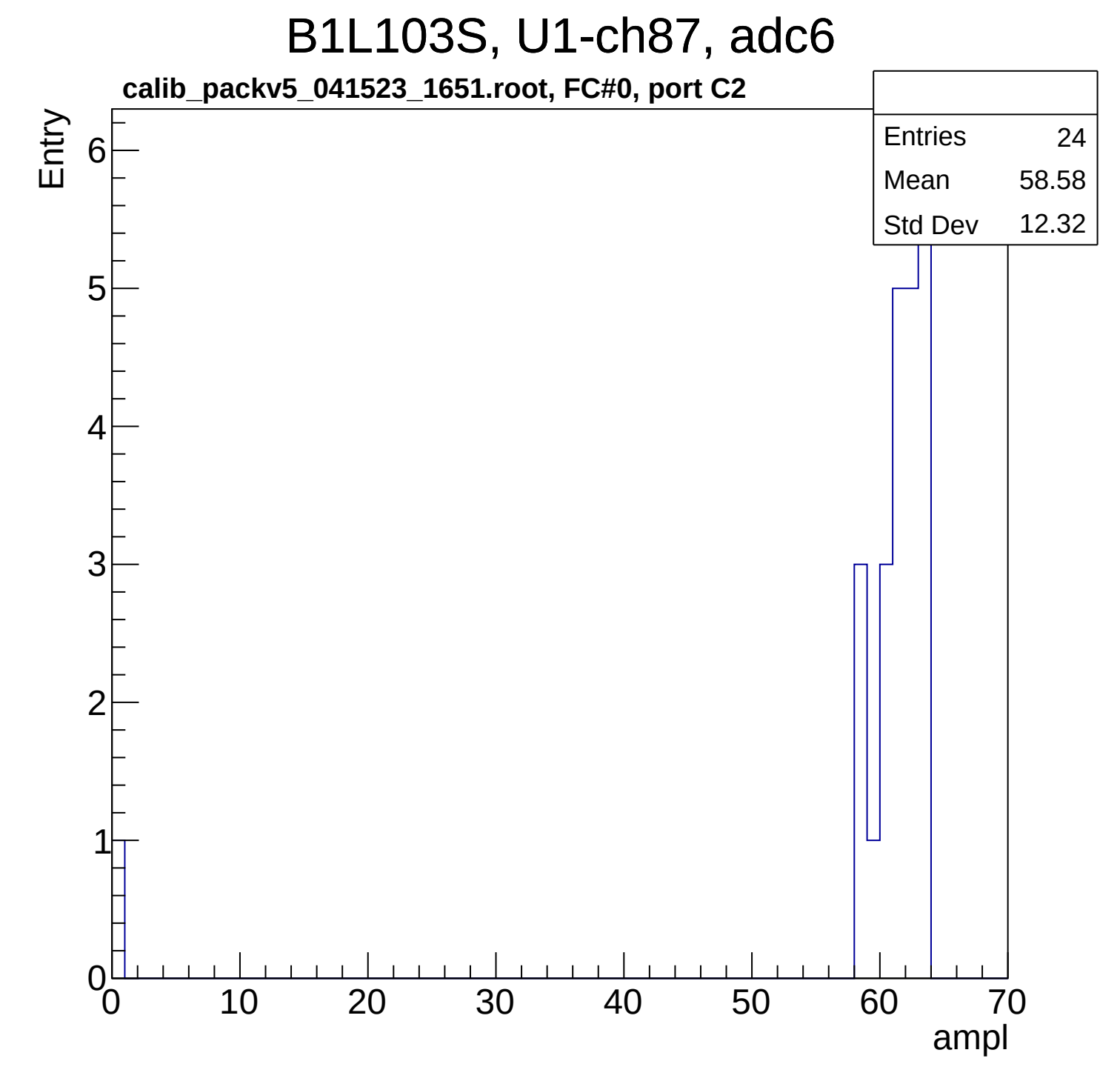
40
50
60
70


B1L103S, U1-ch87, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 24
Mean 58.58
Std Dev 12.32
Entry
ampl
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2
3
4
5
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0
10
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40
50
60
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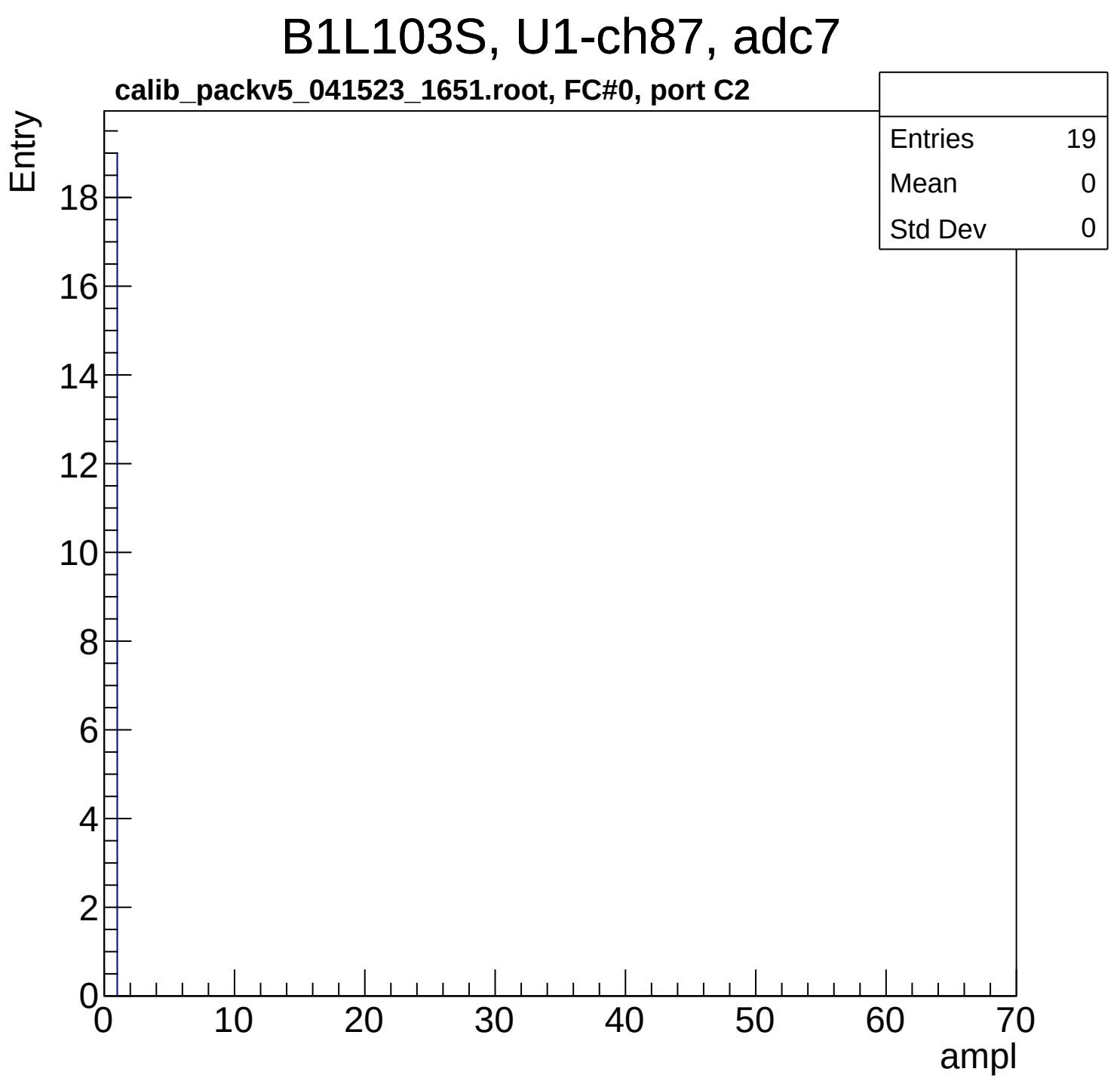
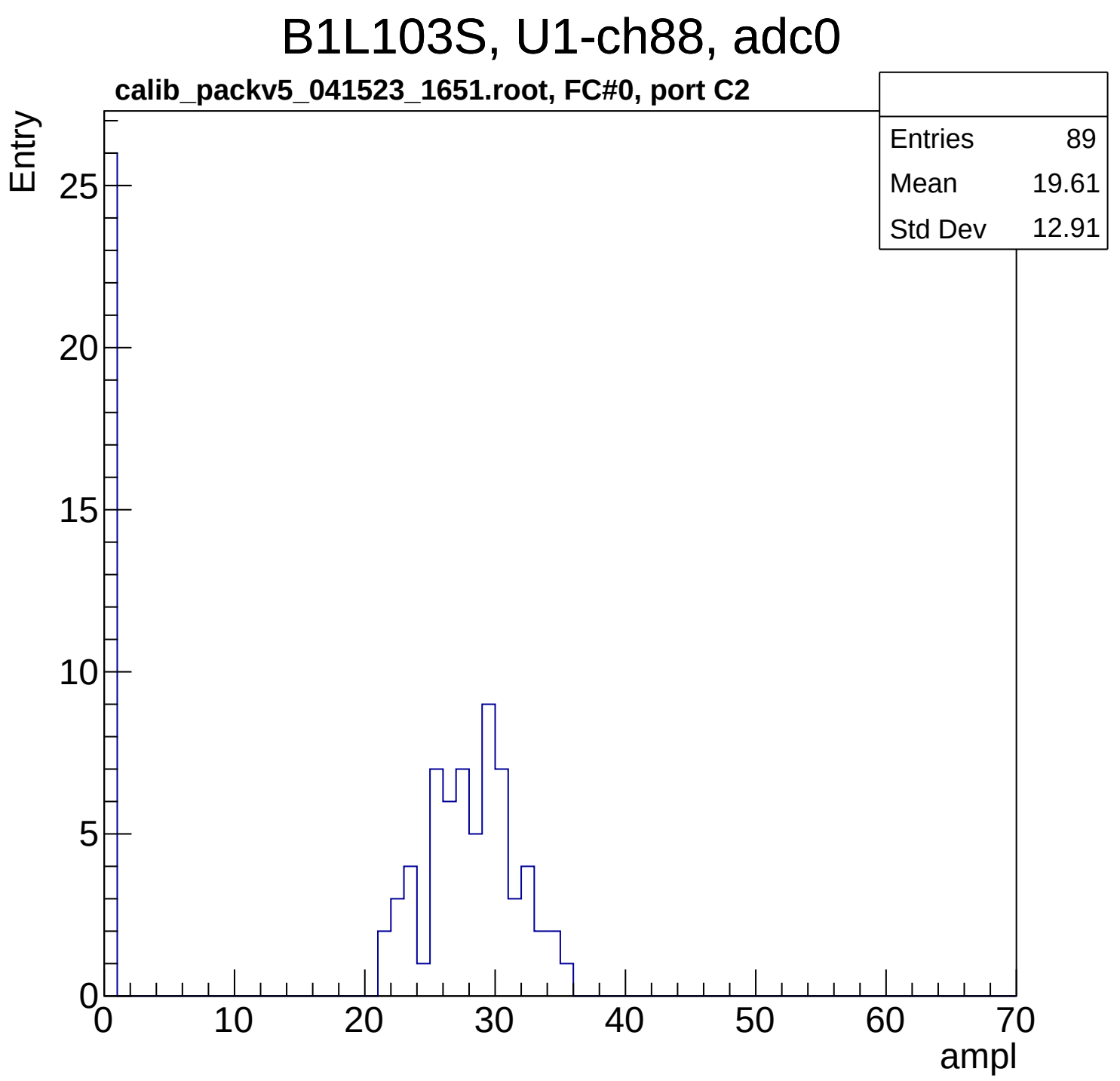

B1L103S, U1-ch87, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch88, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 89
Mean 19.61
Std Dev 12.91
Entry
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10
15
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25
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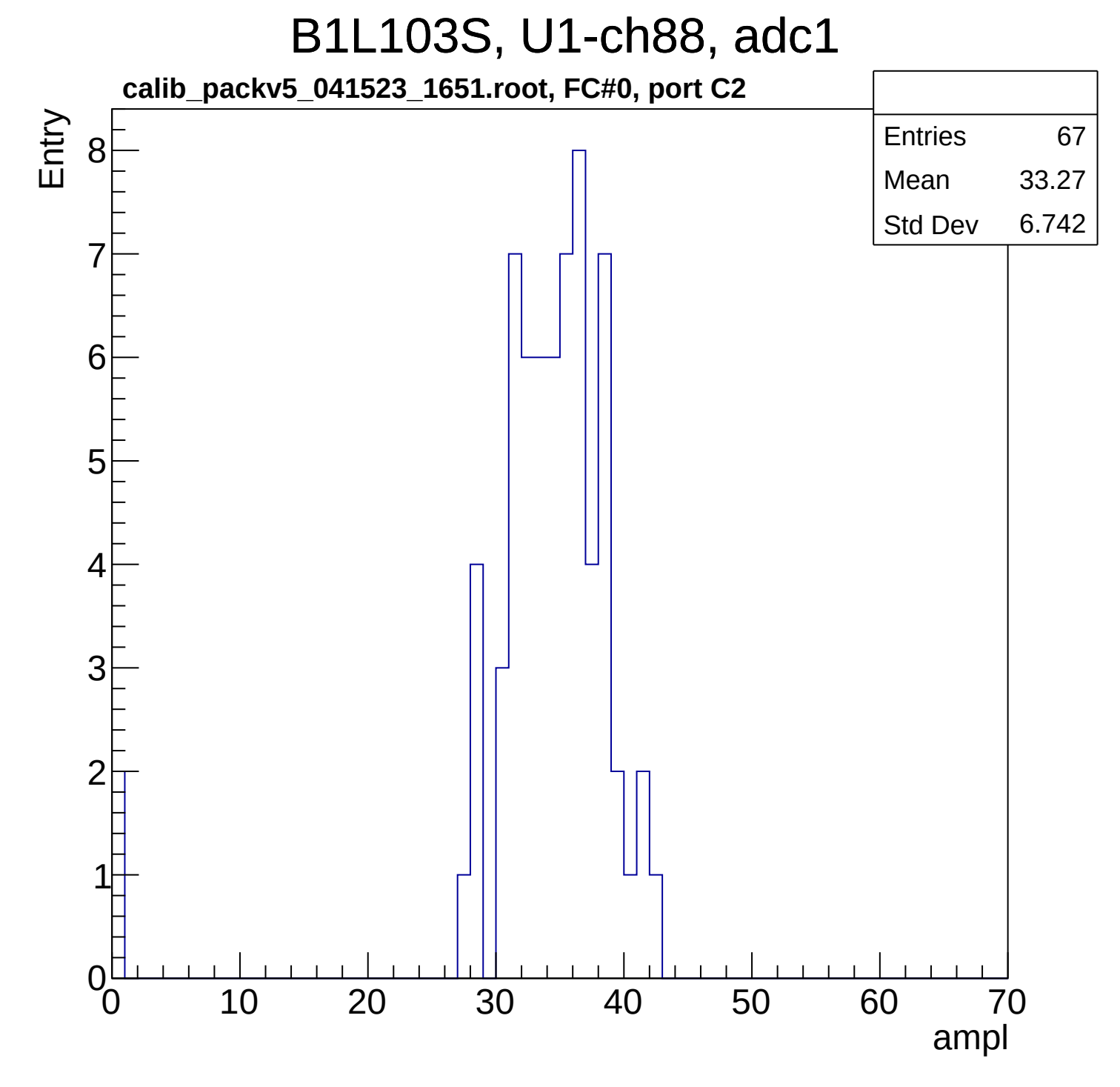
70
ampl


B1L103S, U1-ch88, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 33.27
Std Dev 6.742
Entry
ampl
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0
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60
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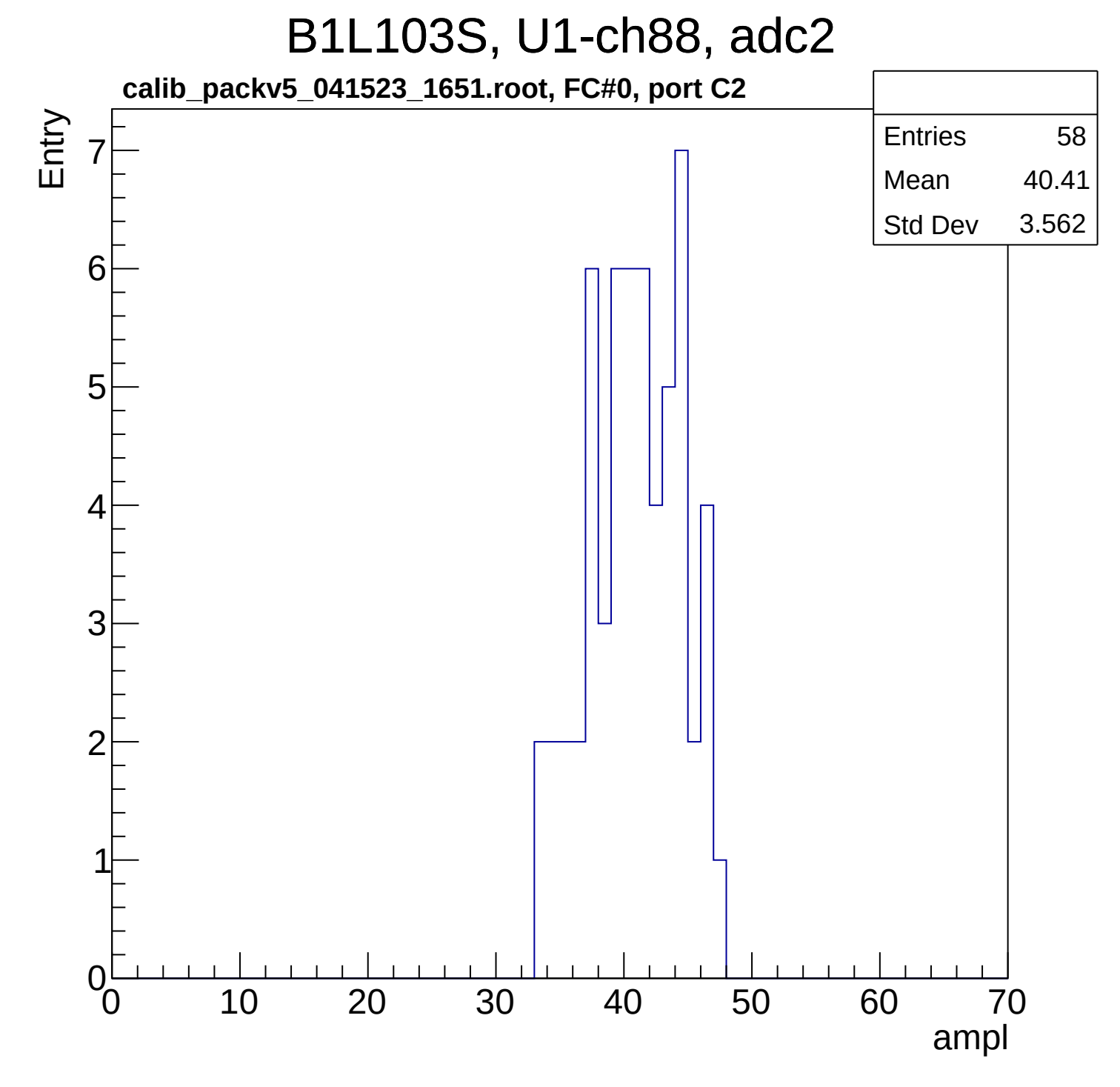
B1L103S, U1-ch88, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 40.41
Std Dev 3.562
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
30
40
50
60
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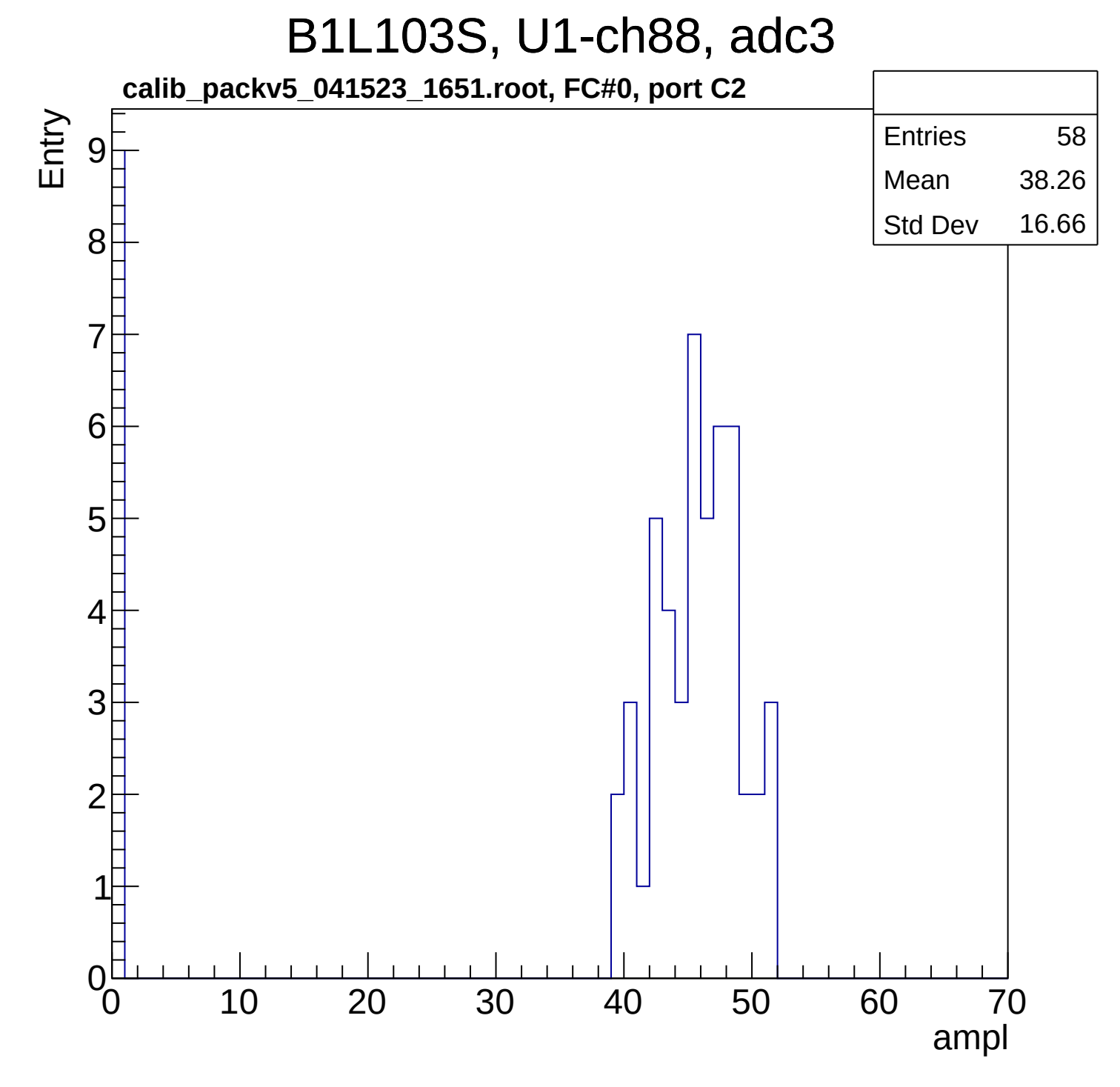
B1L103S, U1-ch88, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 38.26
Std Dev 16.66
Entry
ampl
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6
7
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0
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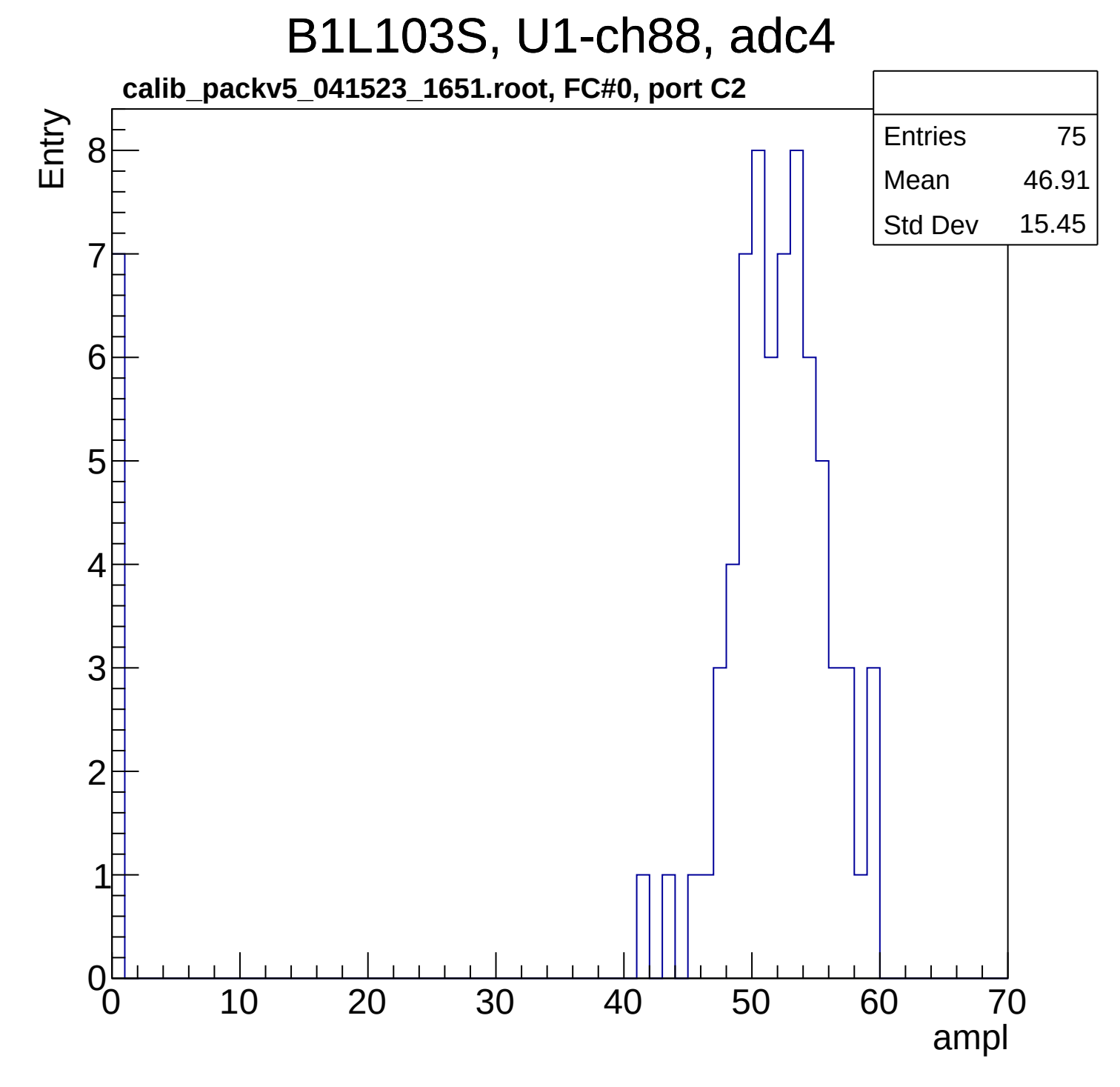
B1L103S, U1-ch88, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 46.91
Std Dev 15.45
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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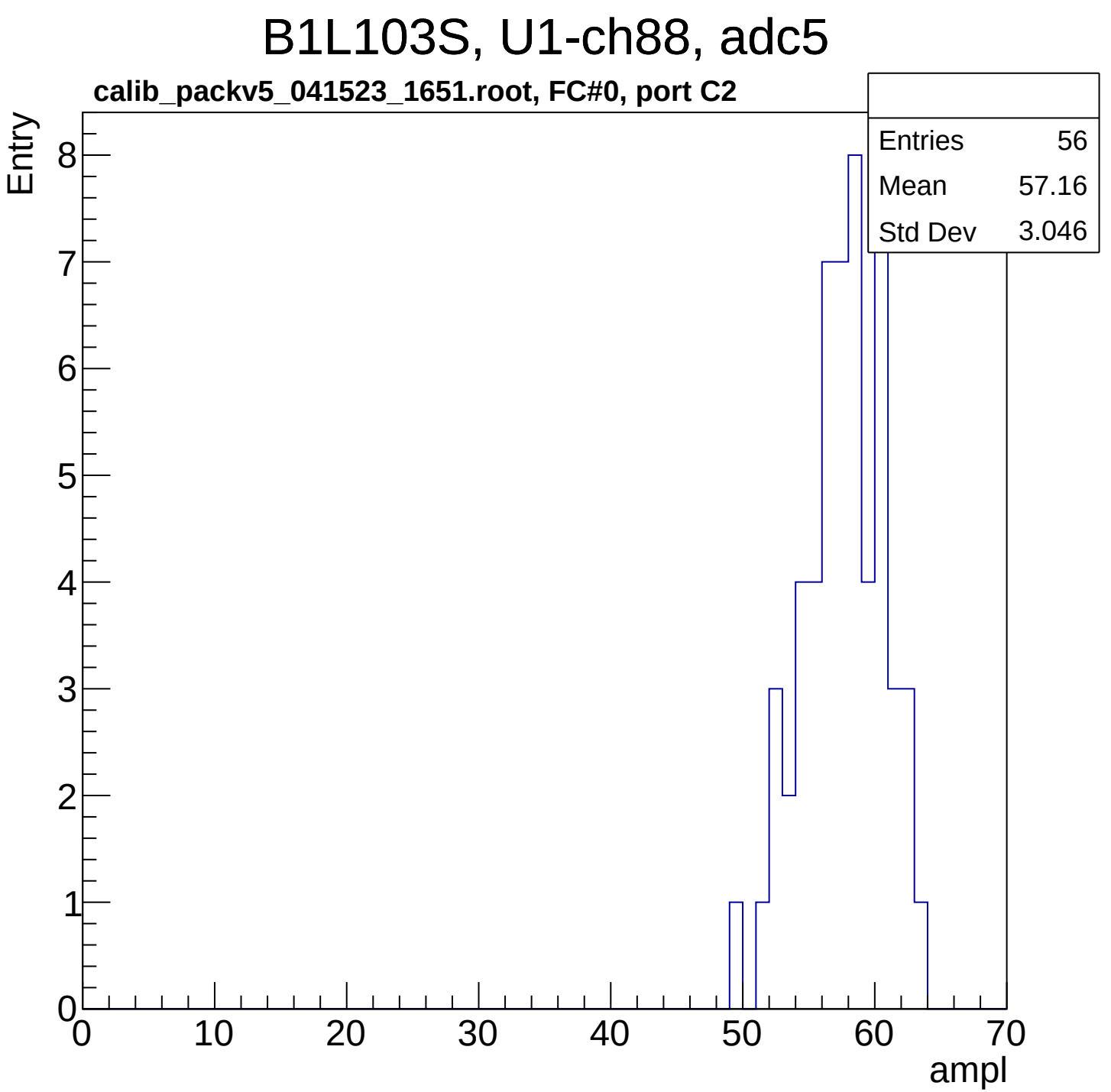
B1L103S, U1-ch88, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 57.16
Std Dev 3.046
Entry
ampl
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2
3
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5
6
7
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0
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60
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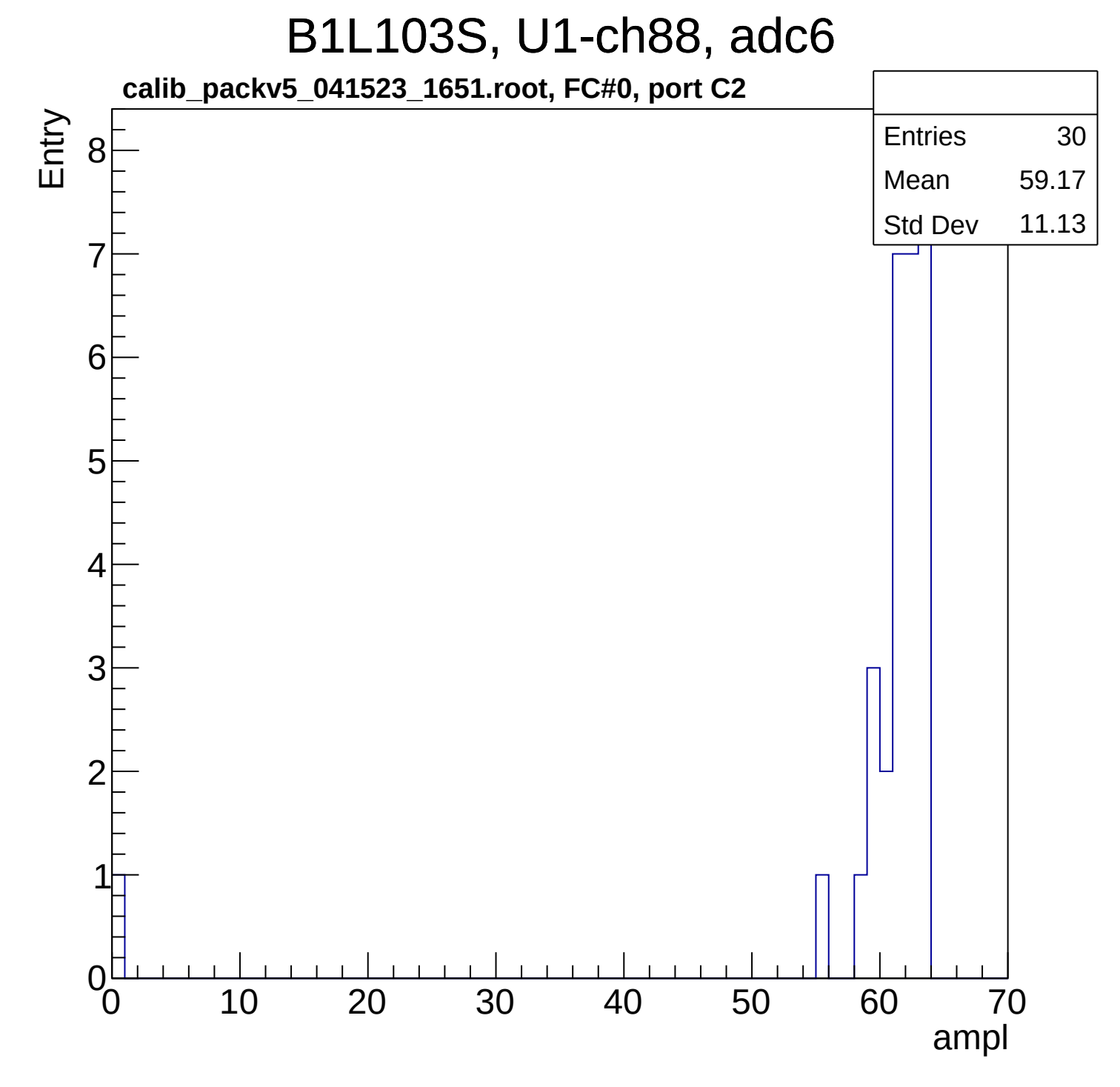
B1L103S, U1-ch88, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 30
Mean 59.17
Std Dev 11.13
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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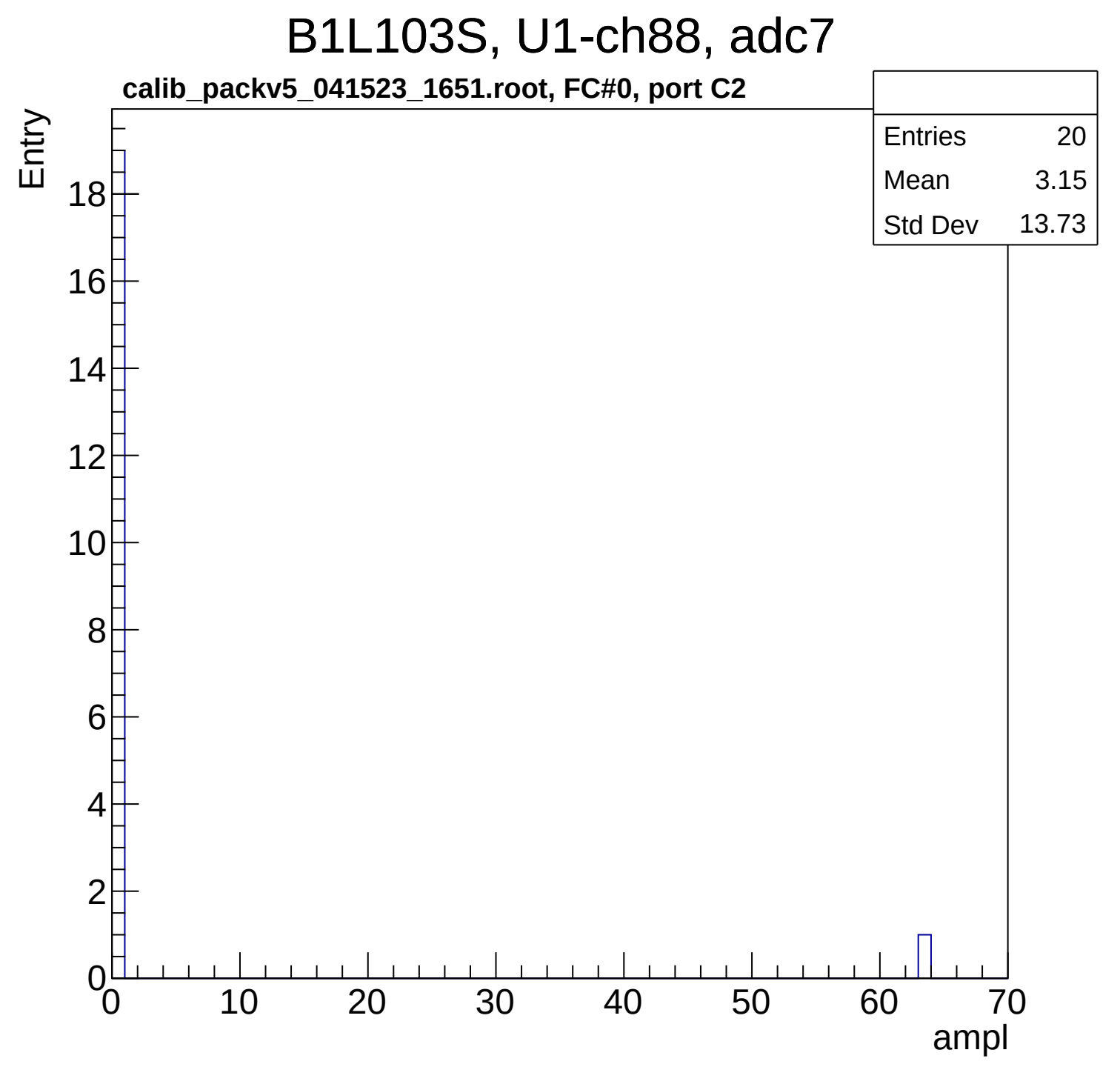
B1L103S, U1-ch88, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
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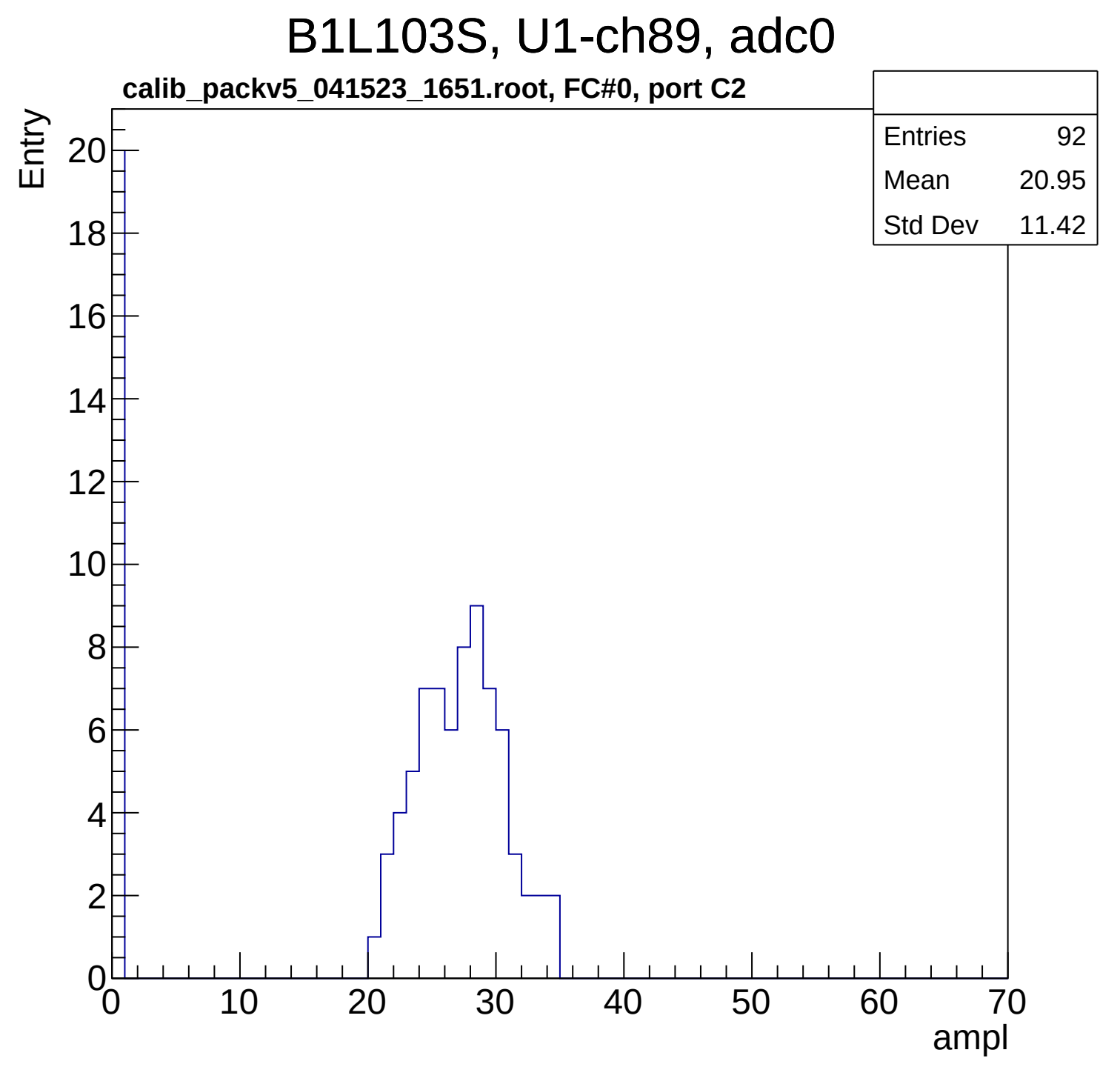
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch89, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 92
Mean 20.95
Std Dev 11.42
Entry
ampl
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6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
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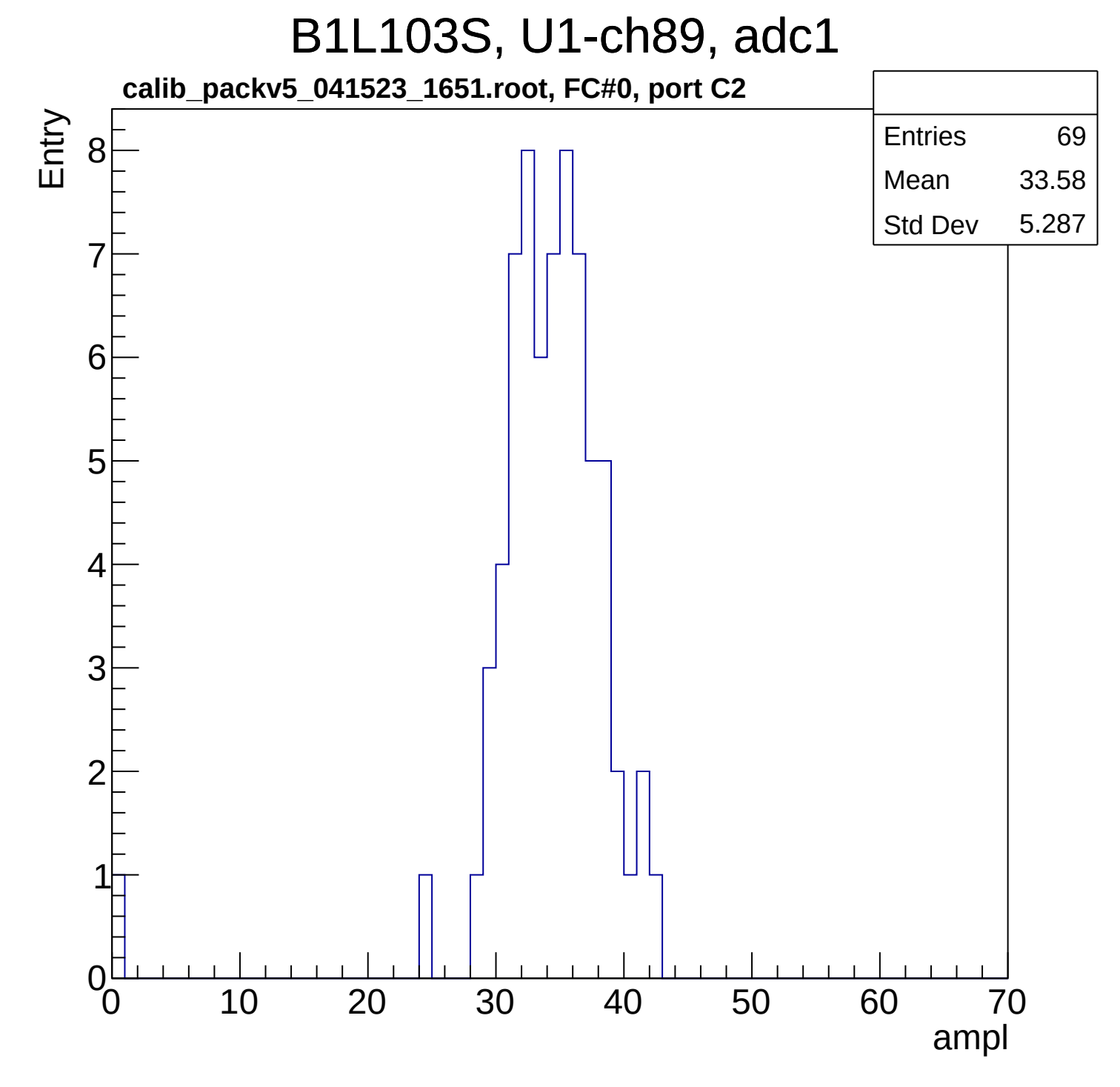
B1L103S, U1-ch89, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 33.58
Std Dev 5.287
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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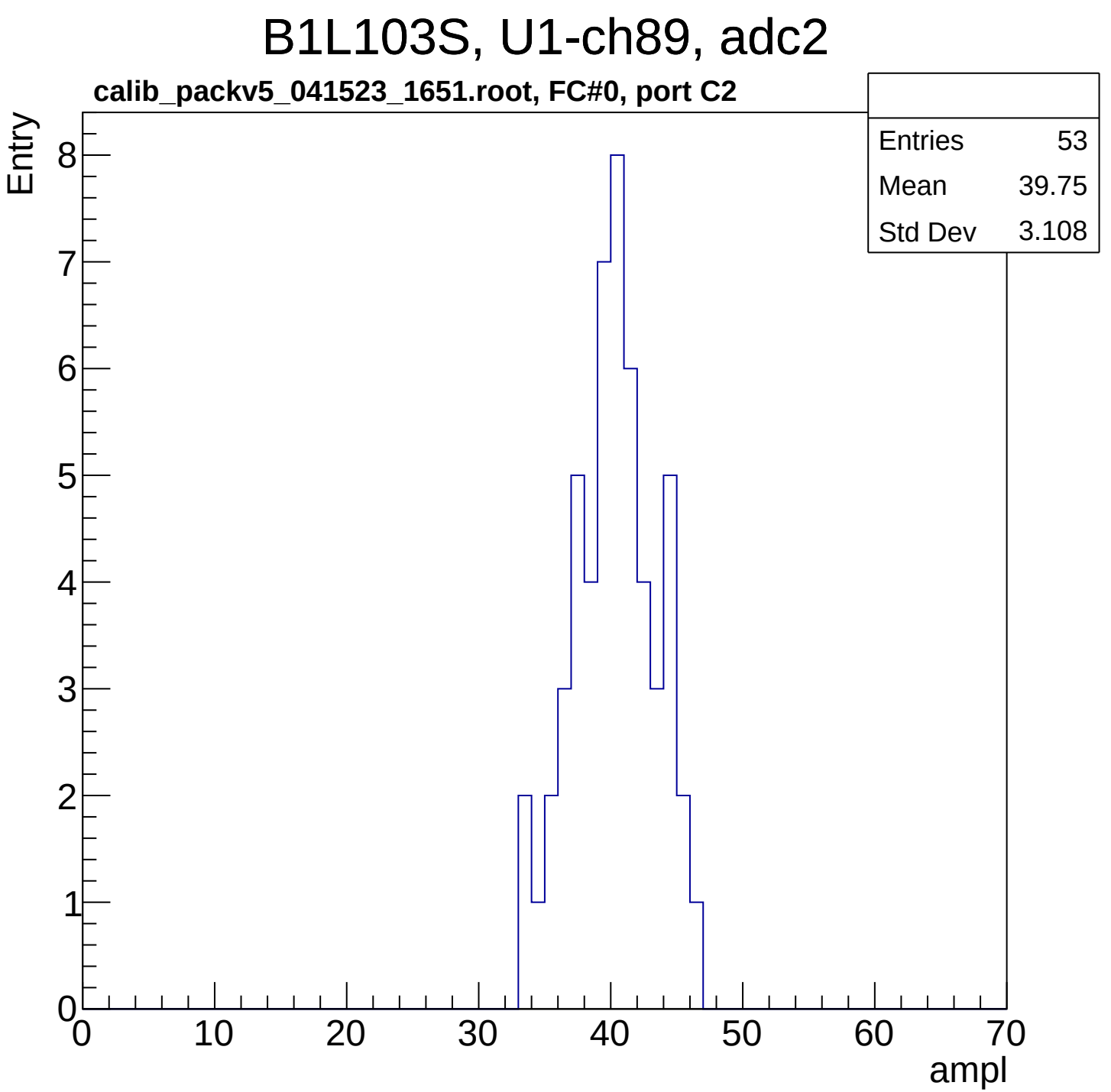
B1L103S, U1-ch89, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 39.75
Std Dev 3.108
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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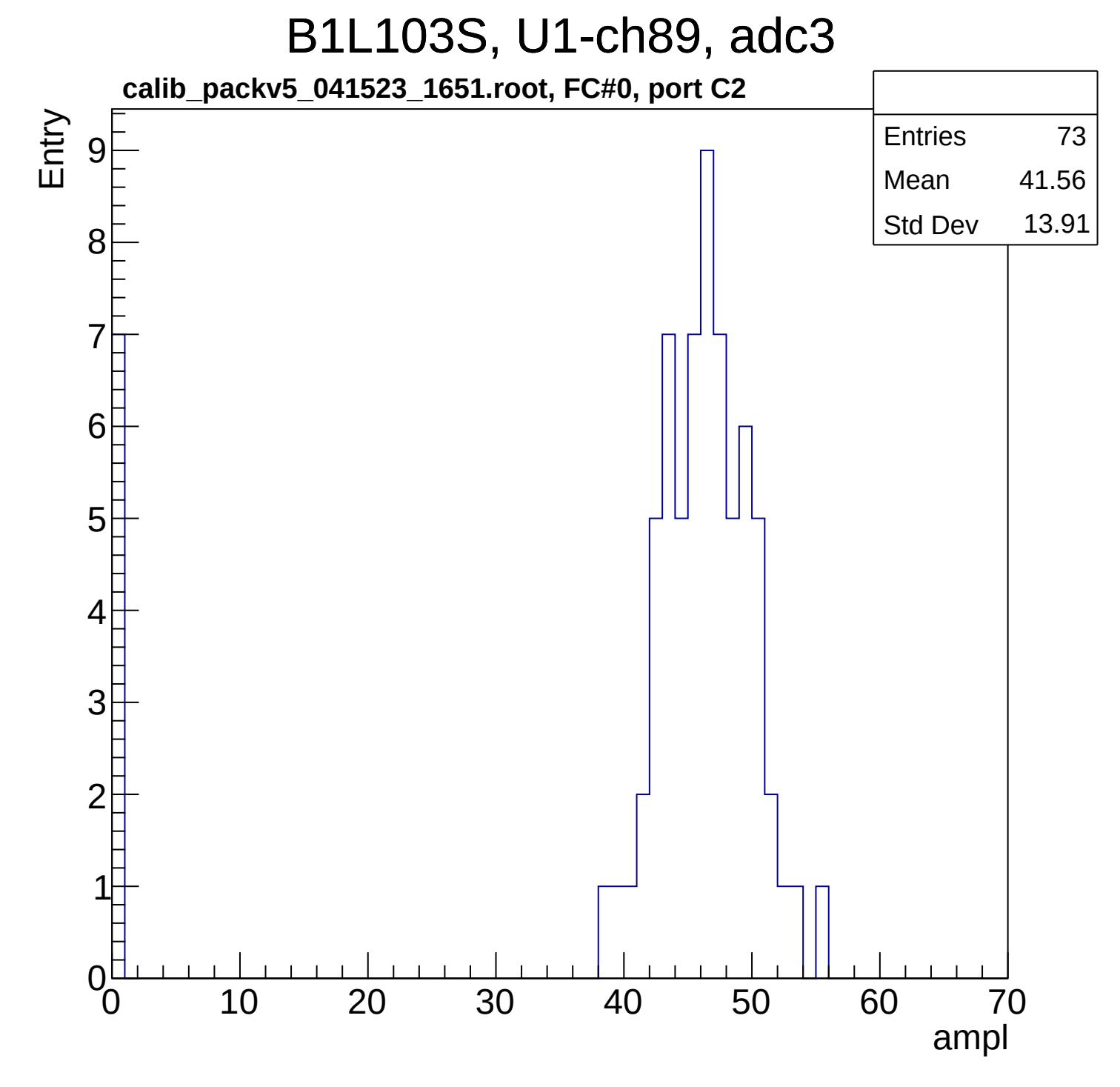
B1L103S, U1-ch89, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 41.56
Std Dev 13.91
Entry
ampl
0
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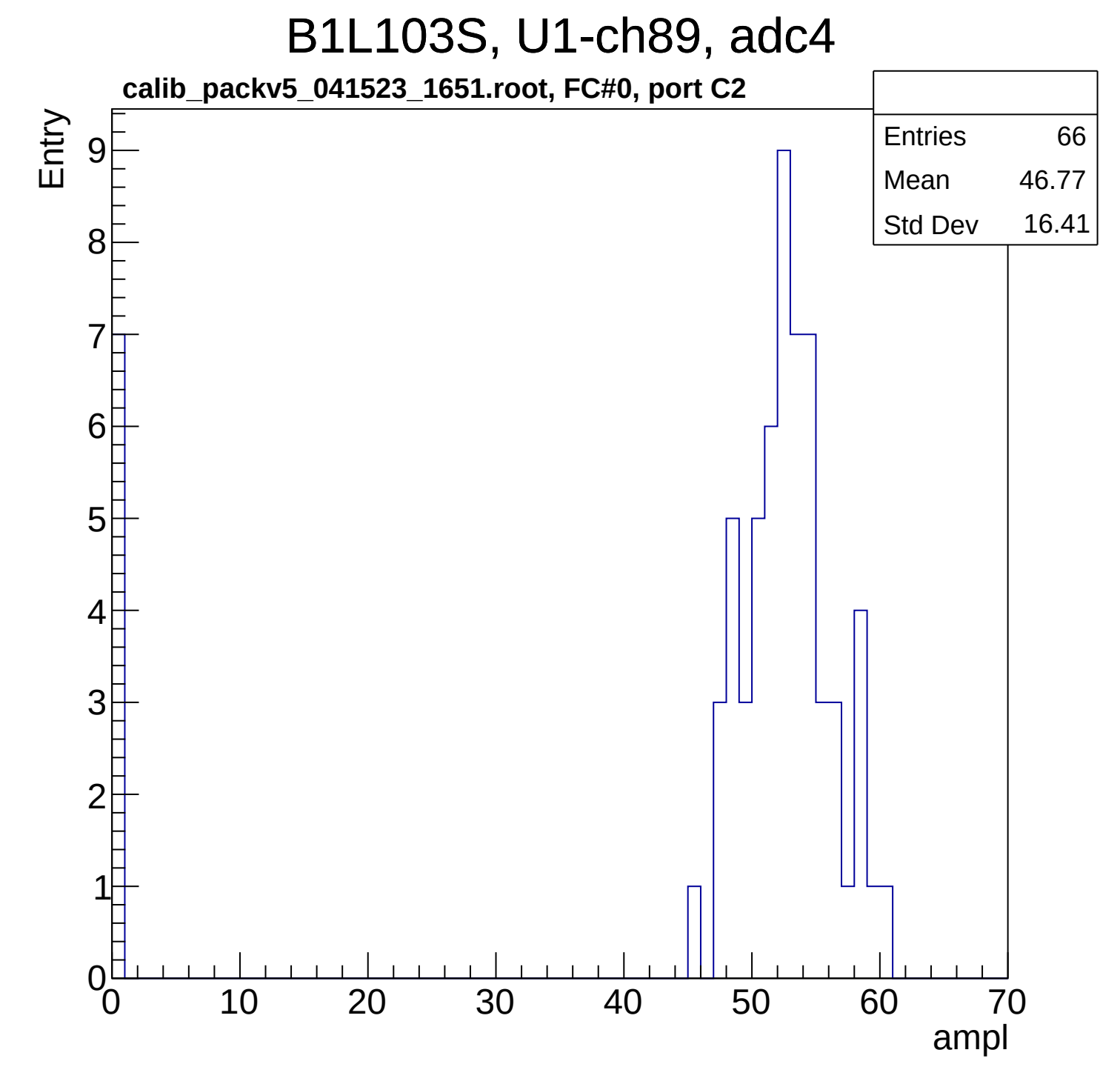
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U1-ch89, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 46.77
Std Dev 16.41
Entry
ampl
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2
3
4
5
6
7
8
9
0
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60
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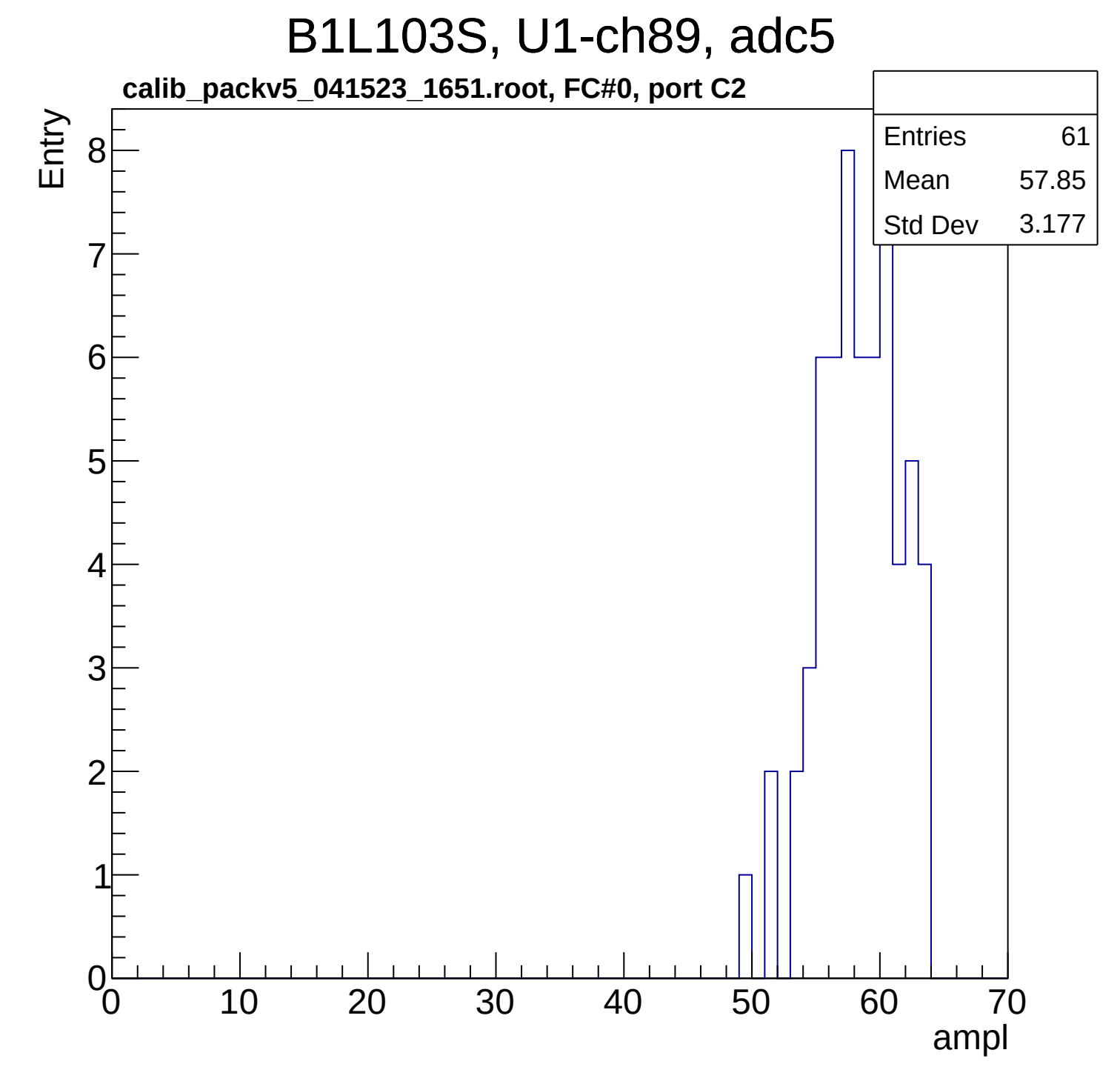
B1L103S, U1-ch89, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 57.85
Std Dev 3.177
Entry
ampl
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2
3
4
5
6
7
8
0
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20
30
40
50
60
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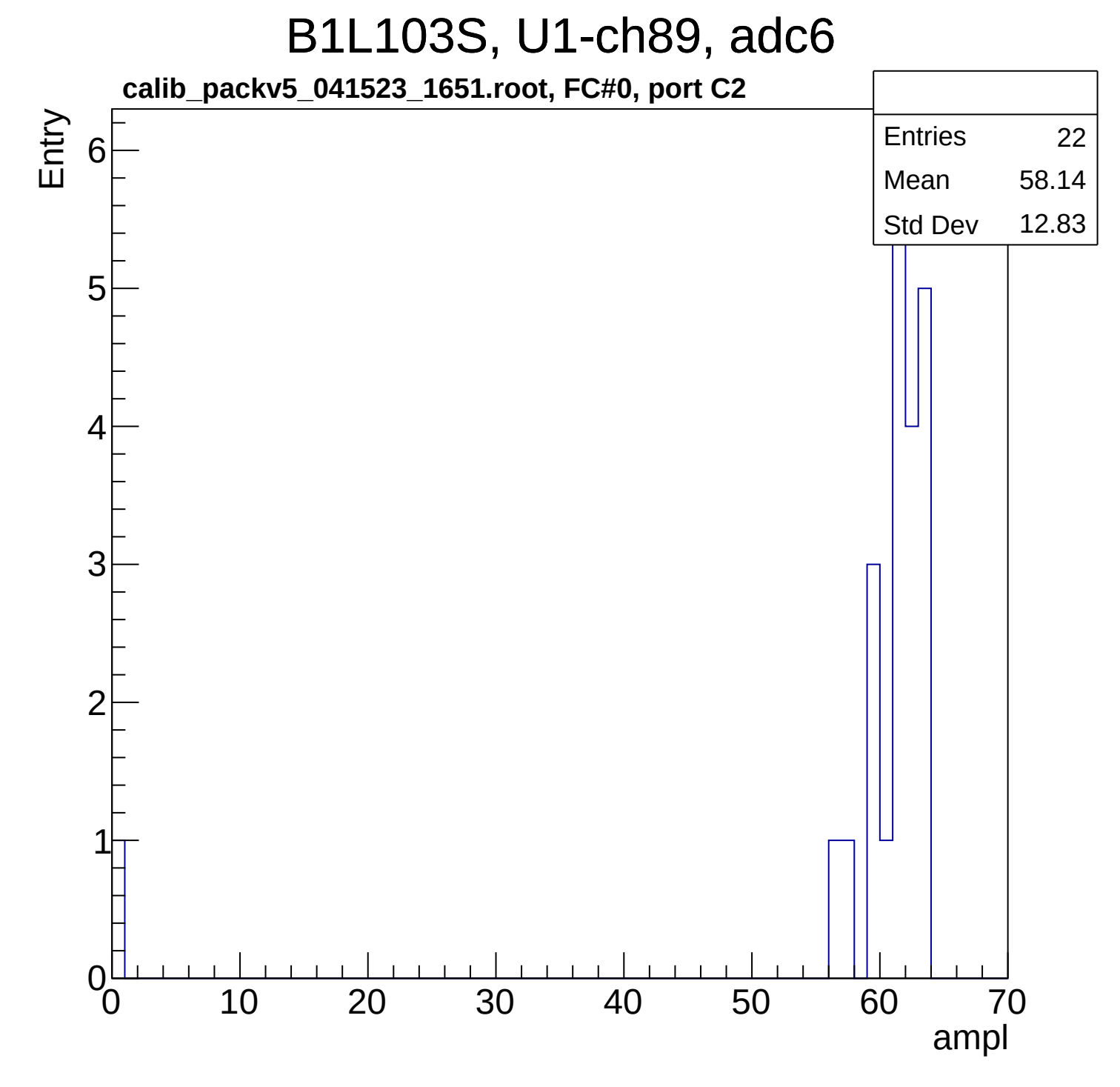
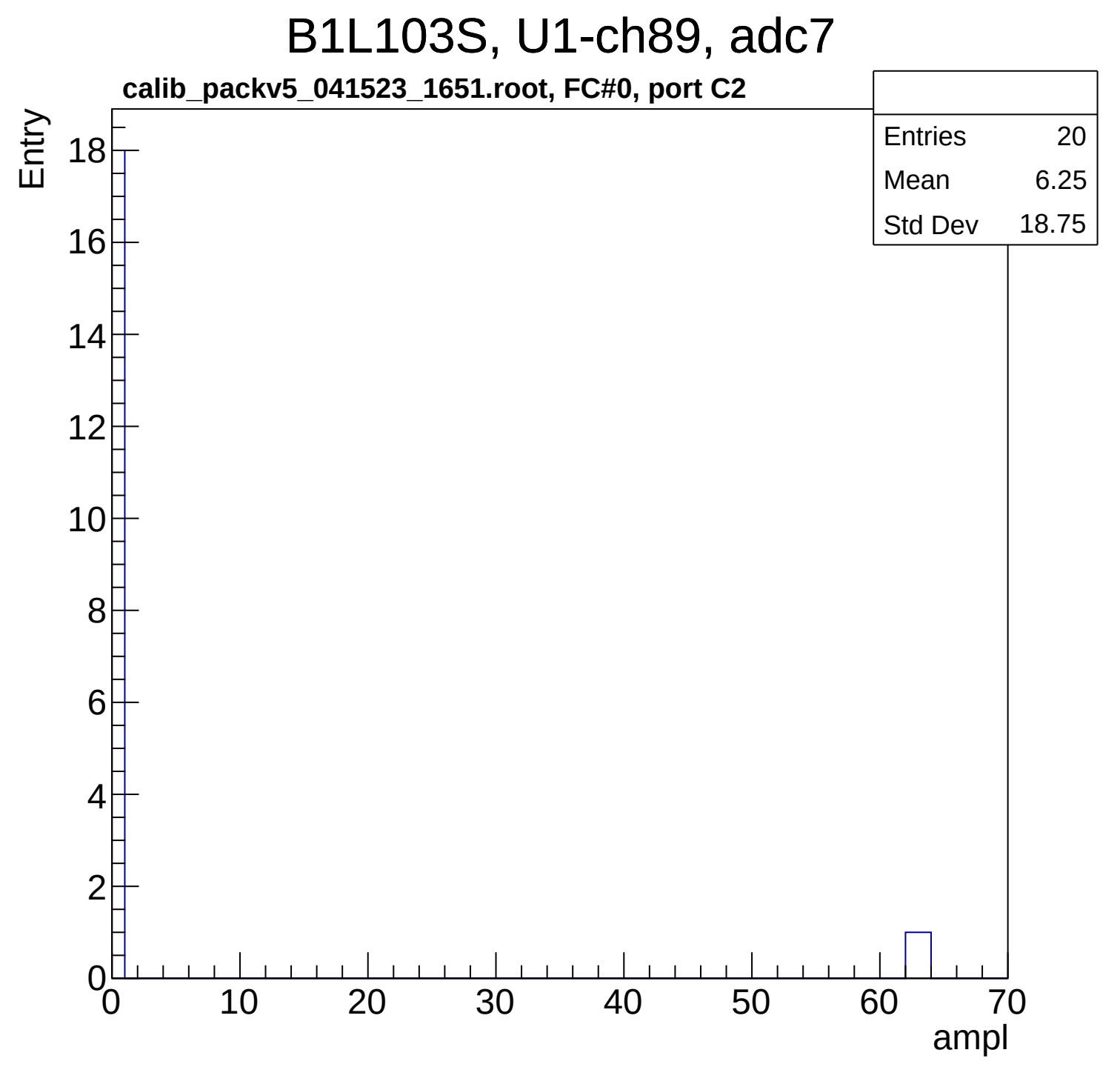

B1L103S, U1-ch89, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 58.14
Std Dev 12.83
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U1-ch89, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 6.25
Std Dev 18.75
Entry
ampl
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4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
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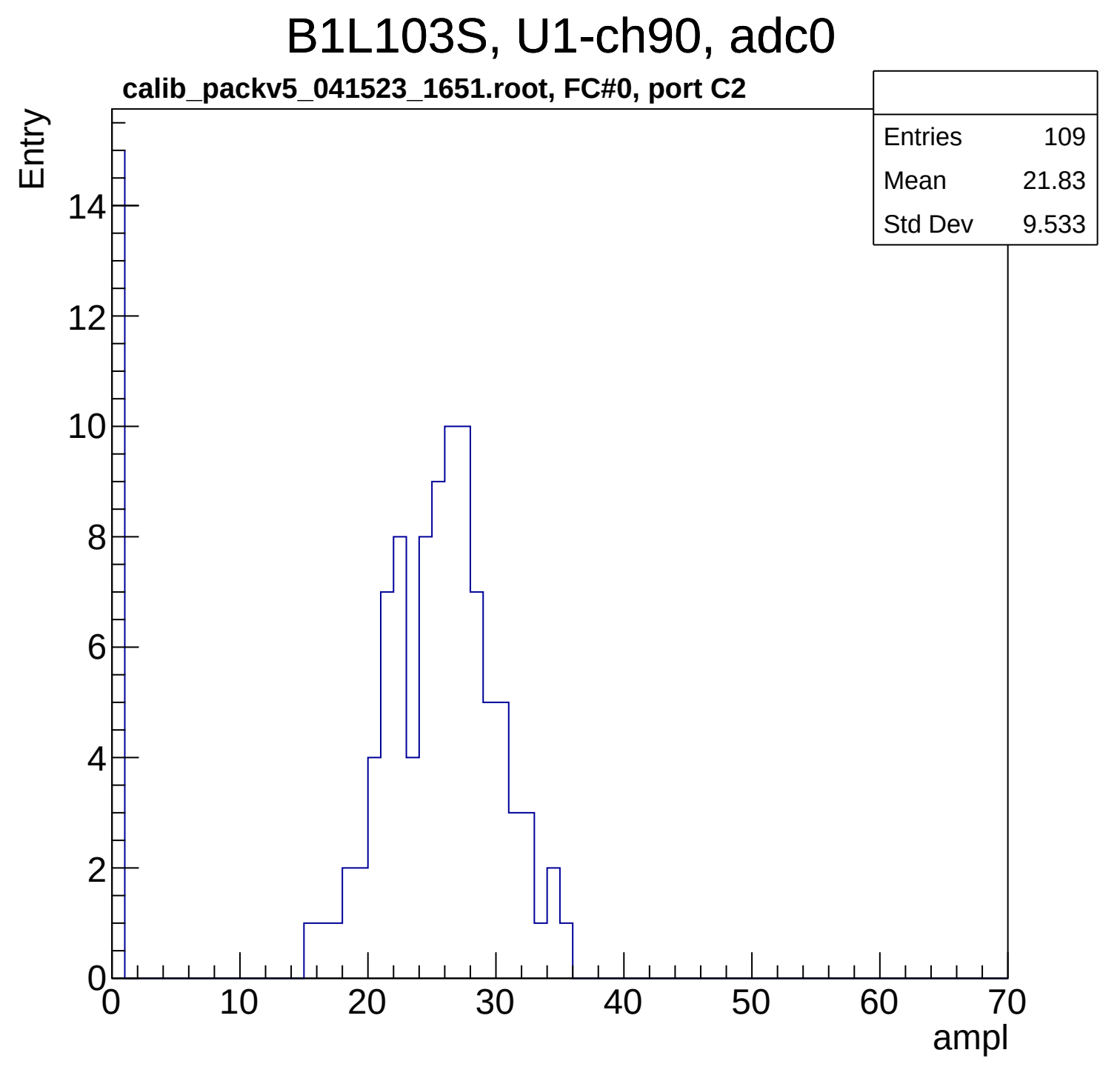
B1L103S, U1-ch90, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 109
Mean 21.83
Std Dev 9.533
Entry
ampl
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2
4
6
8
10
12
14
0
10
20
30
40
50
60
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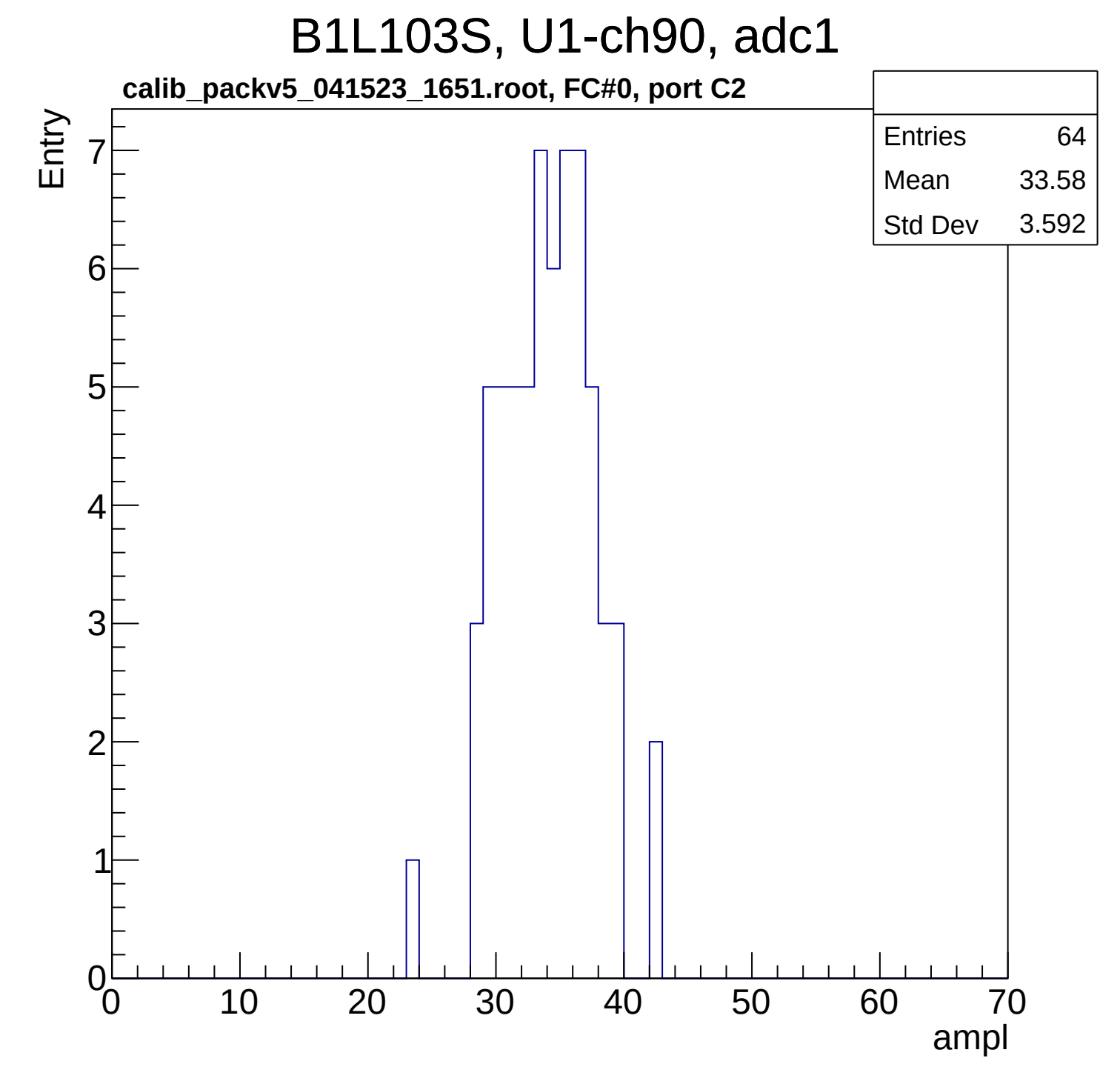
B1L103S, U1-ch90, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 33.58
Std Dev 3.592
Entry
ampl
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3
4
5
6
7
0
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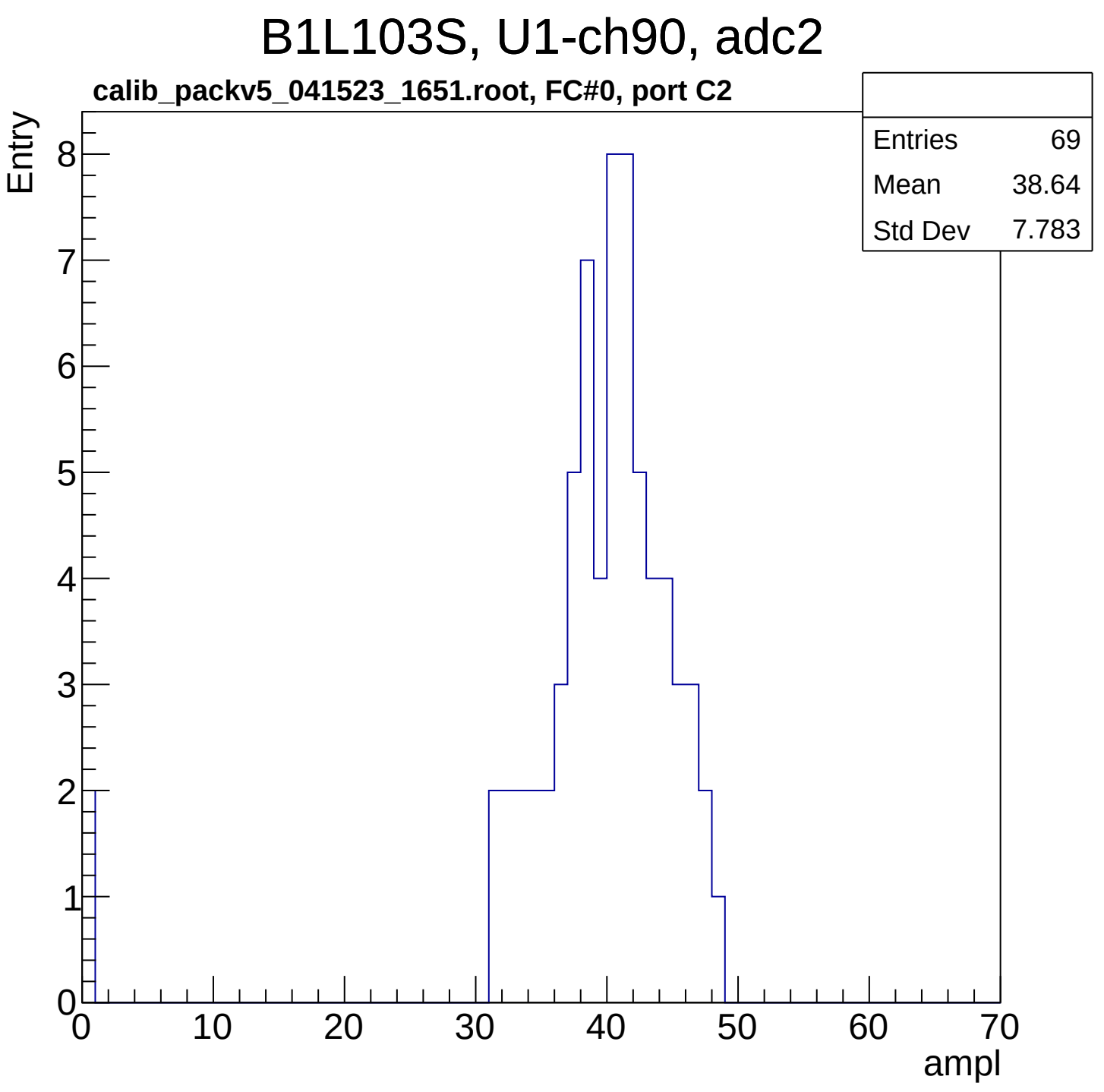
20
30
40
50
60
70


B1L103S, U1-ch90, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 38.64
Std Dev 7.783
Entry
ampl
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2
3
4
5
6
7
8
0
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40
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60
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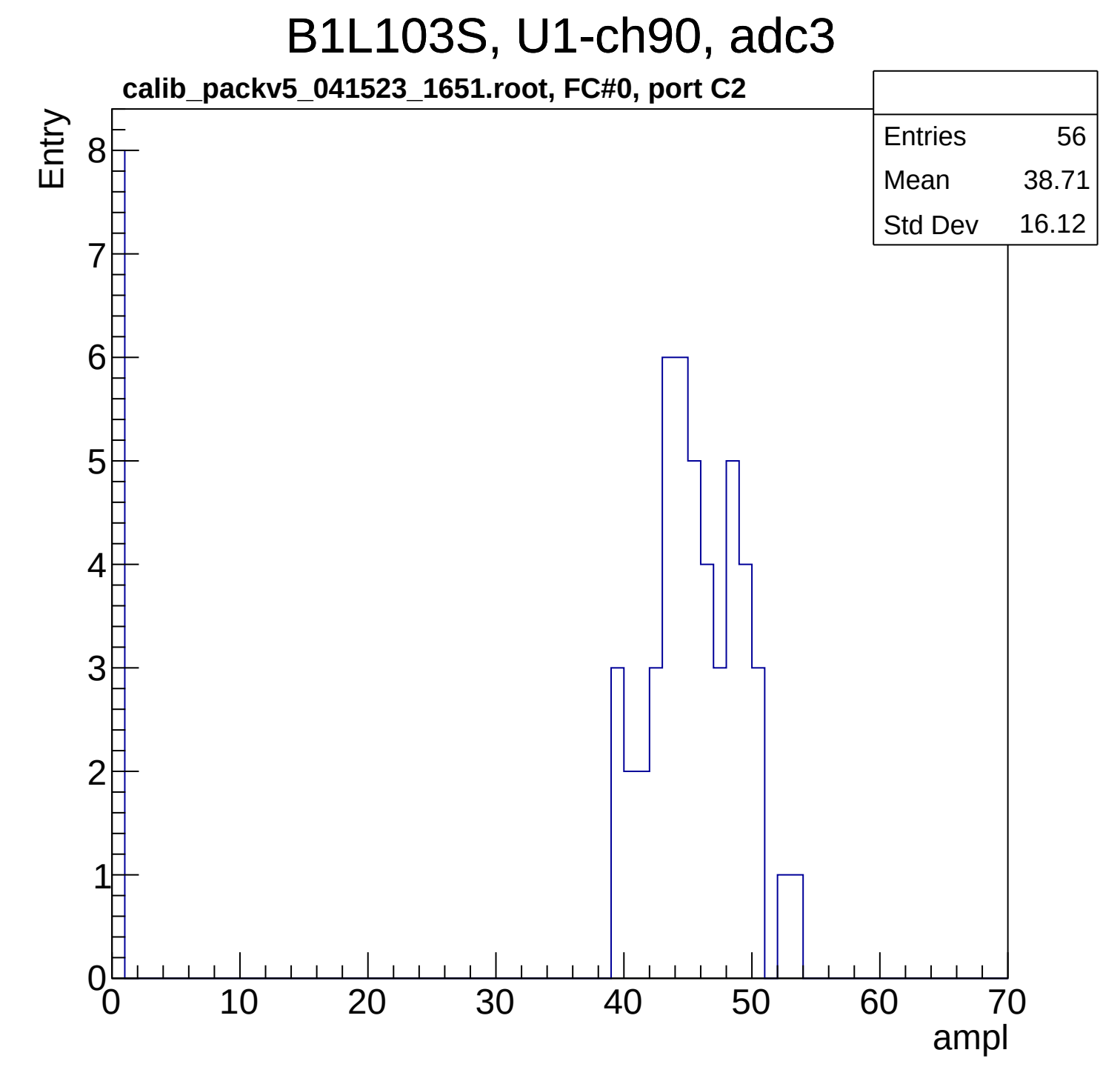
B1L103S, U1-ch90, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 38.71
Std Dev 16.12
Entry
ampl
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1
2
3
4
5
6
7
8
0
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40
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60
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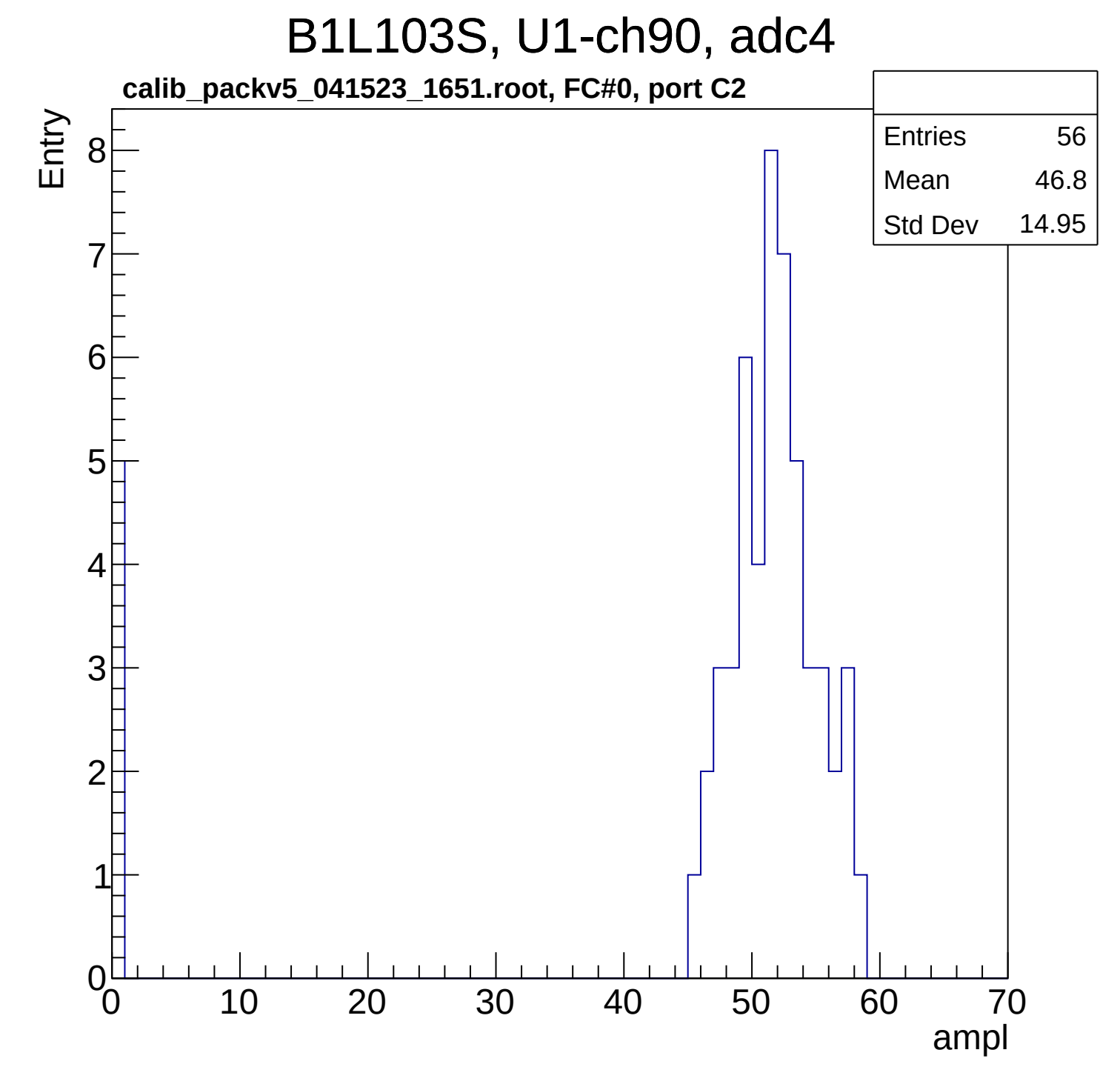
B1L103S, U1-ch90, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 46.8
Std Dev 14.95
Entry
ampl
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3
4
5
6
7
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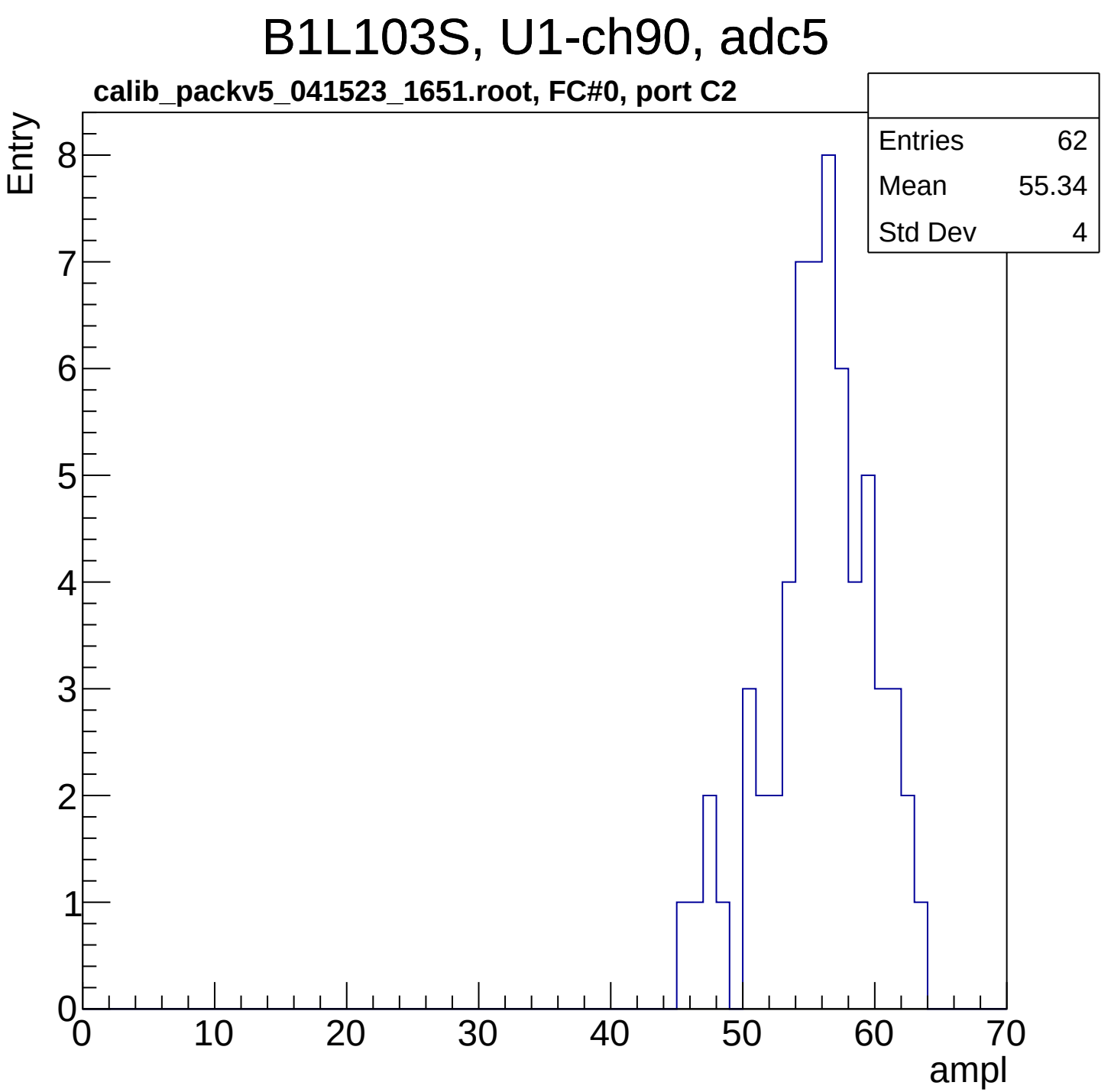
0
10
20
30
40
50
60
70


B1L103S, U1-ch90, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 55.34
Std Dev 4
Entry
ampl
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2
3
4
5
6
7
8
0
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20
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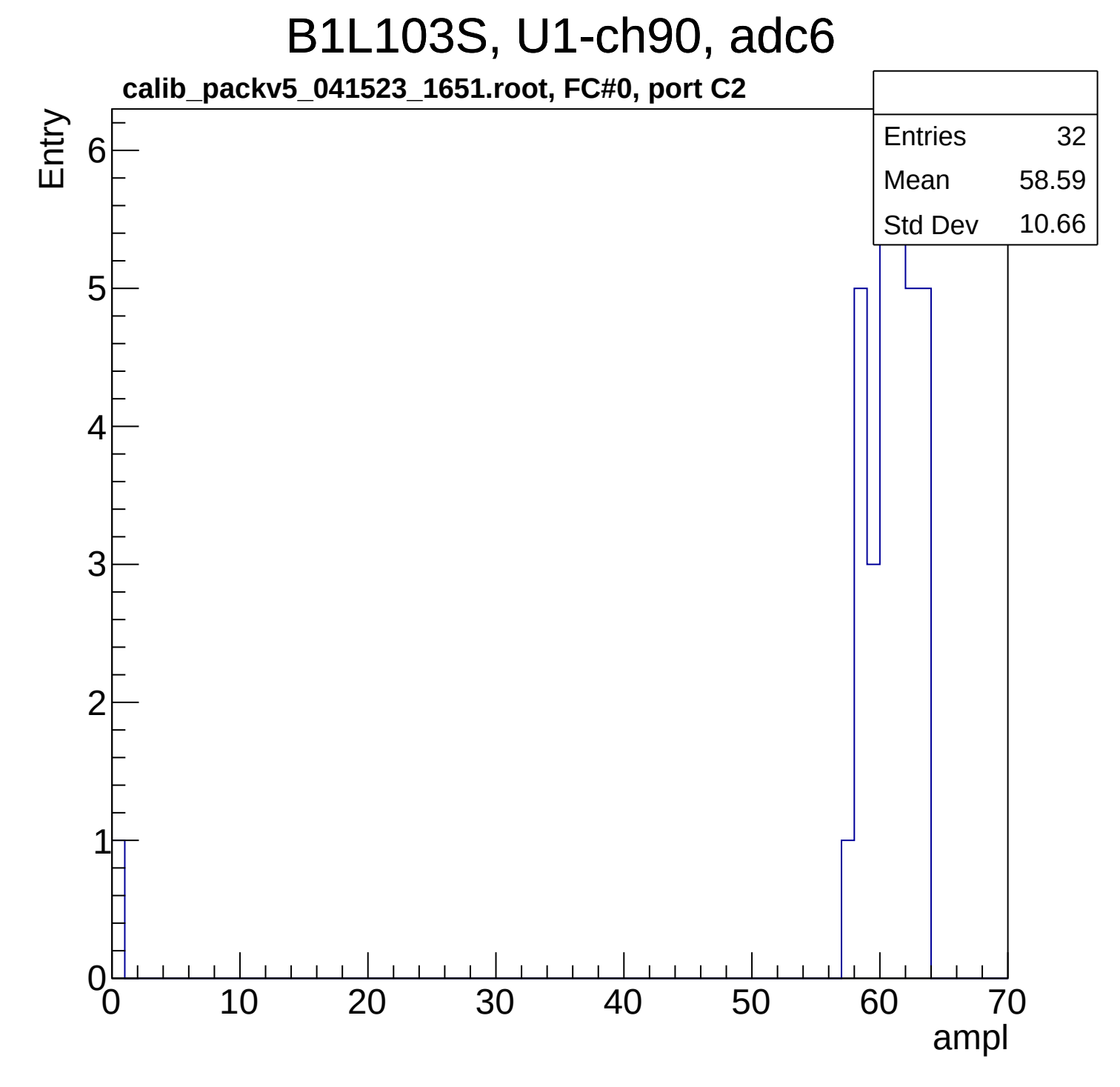
B1L103S, U1-ch90, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 32
Mean 58.59
Std Dev 10.66
Entry
ampl
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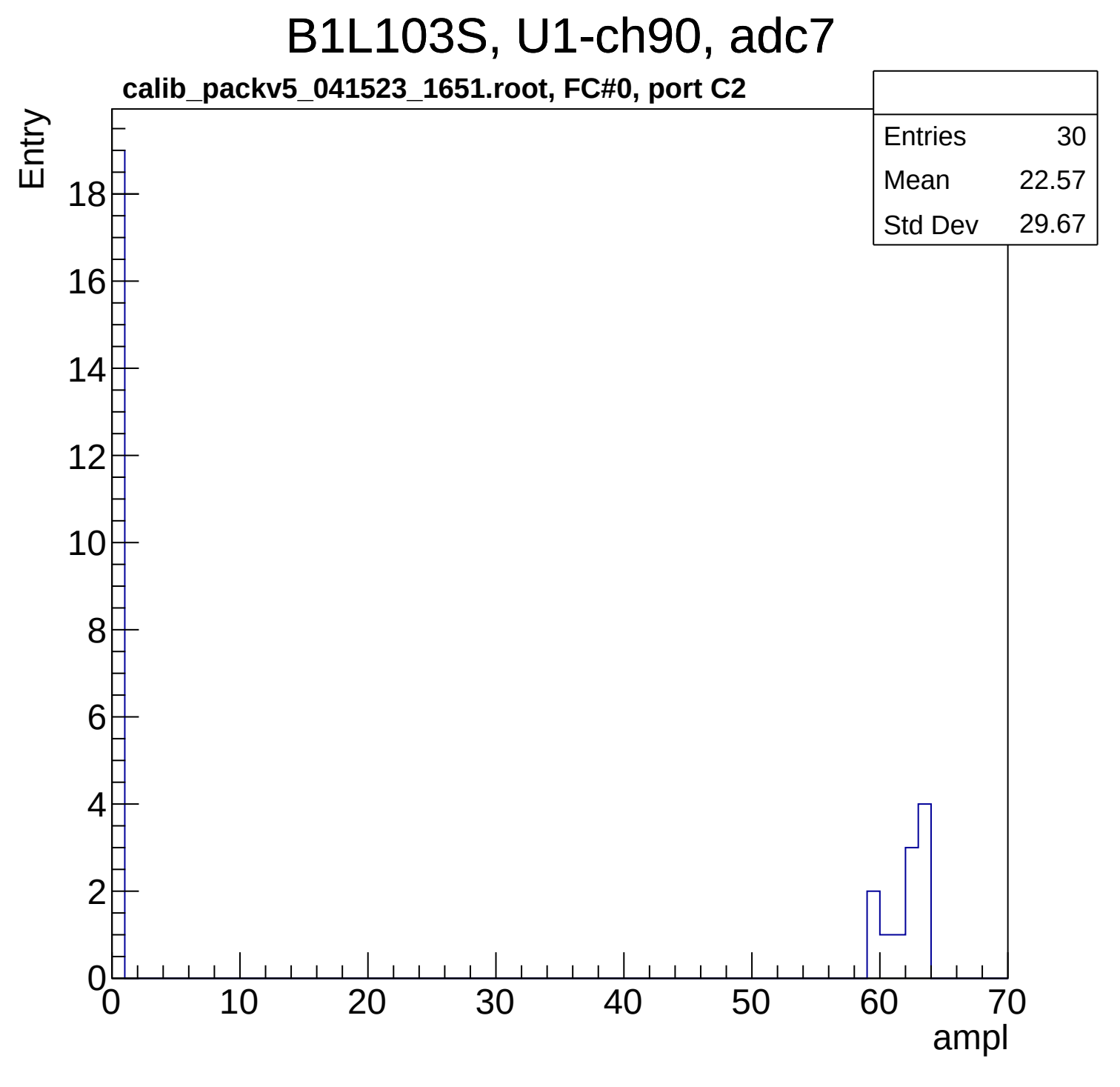
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U1-ch90, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 30
Mean 22.57
Std Dev 29.67
Entry
ampl
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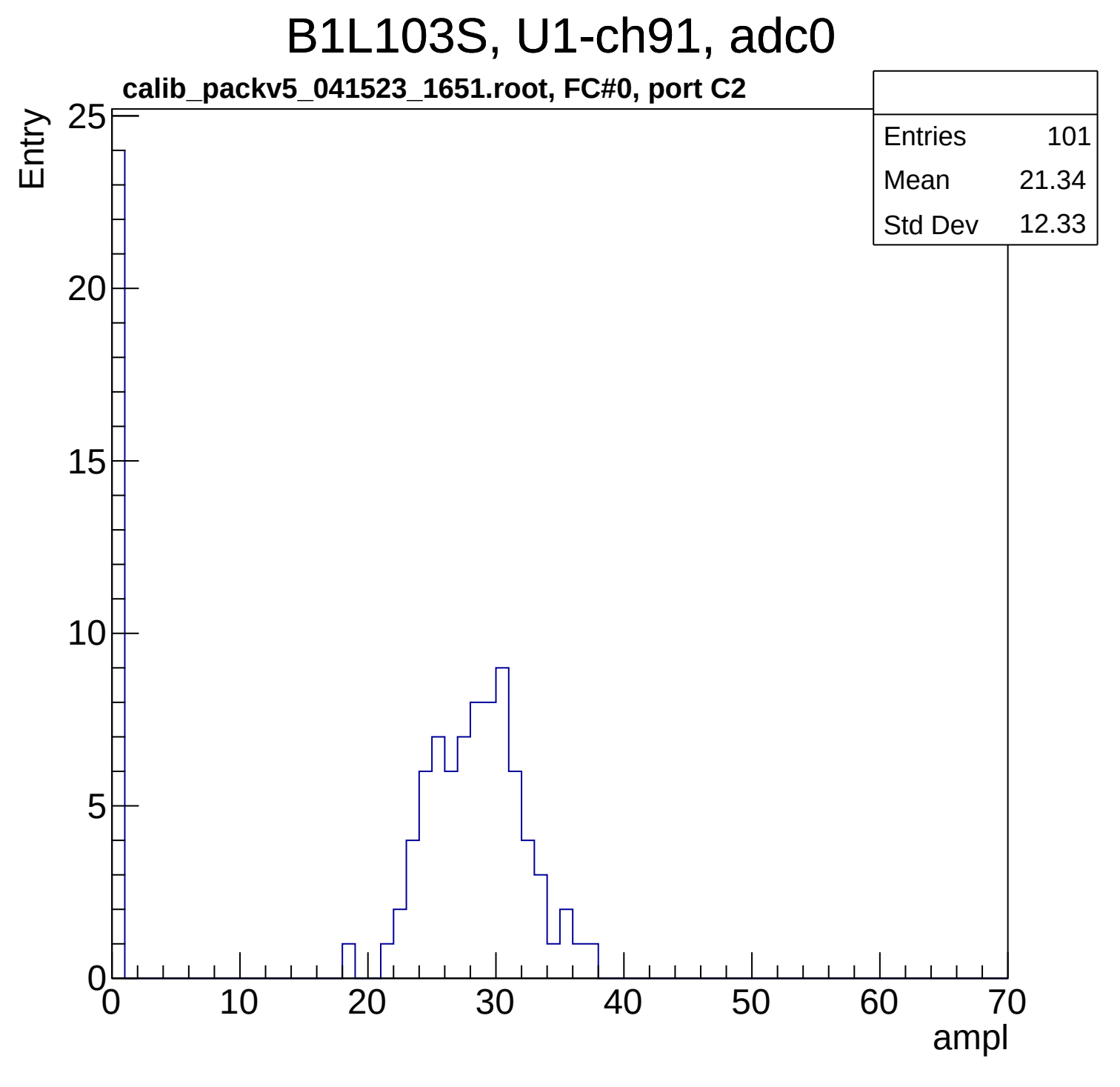
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70


B1L103S, U1-ch91, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 101
Mean 21.34
Std Dev 12.33
Entry
ampl
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10
15
20
25
0
10
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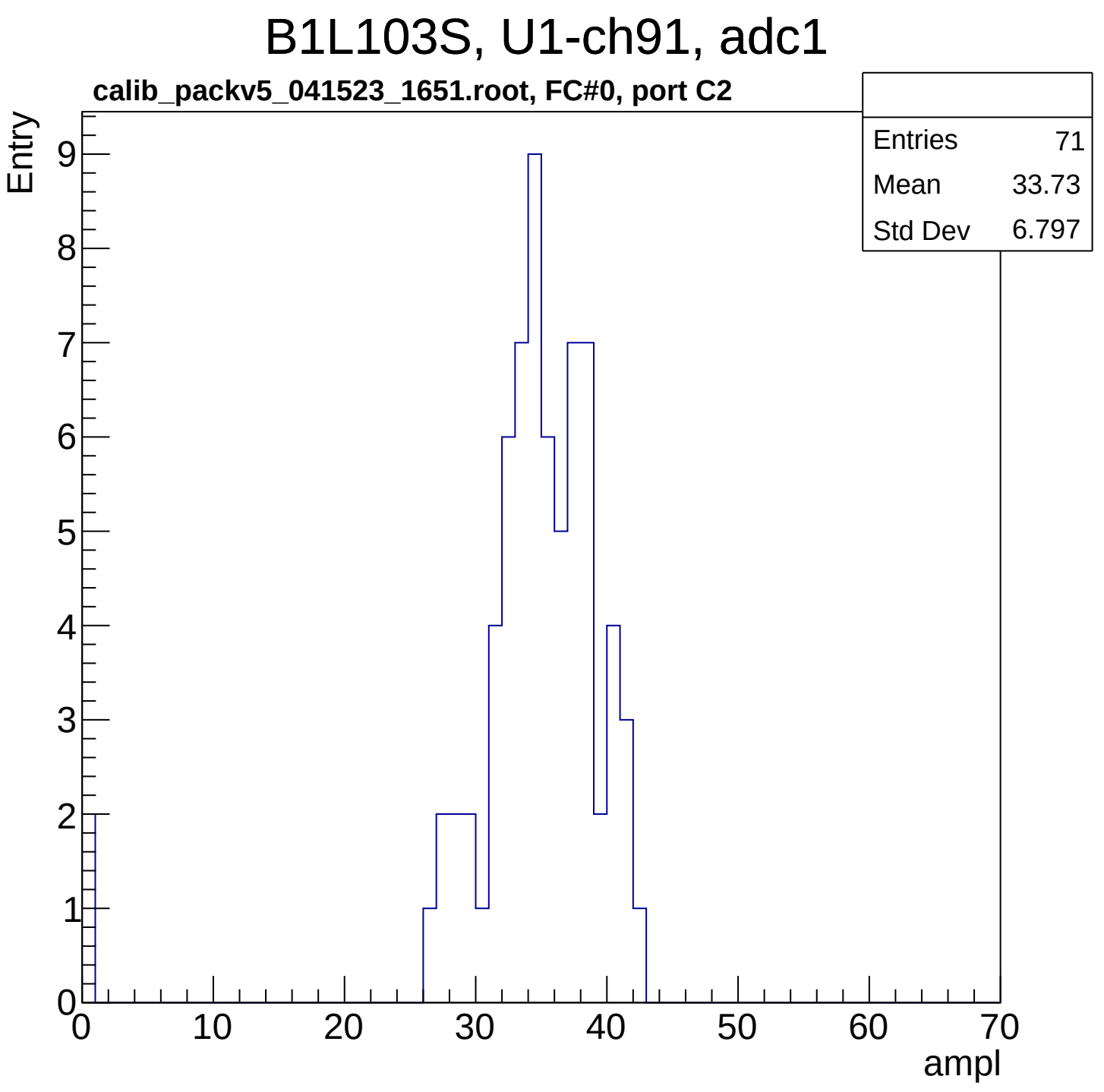
40
50
60
70


B1L103S, U1-ch91, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 33.73
Std Dev 6.797
Entry
ampl
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3
4
5
6
7
8
9
0
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20
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40
50
60
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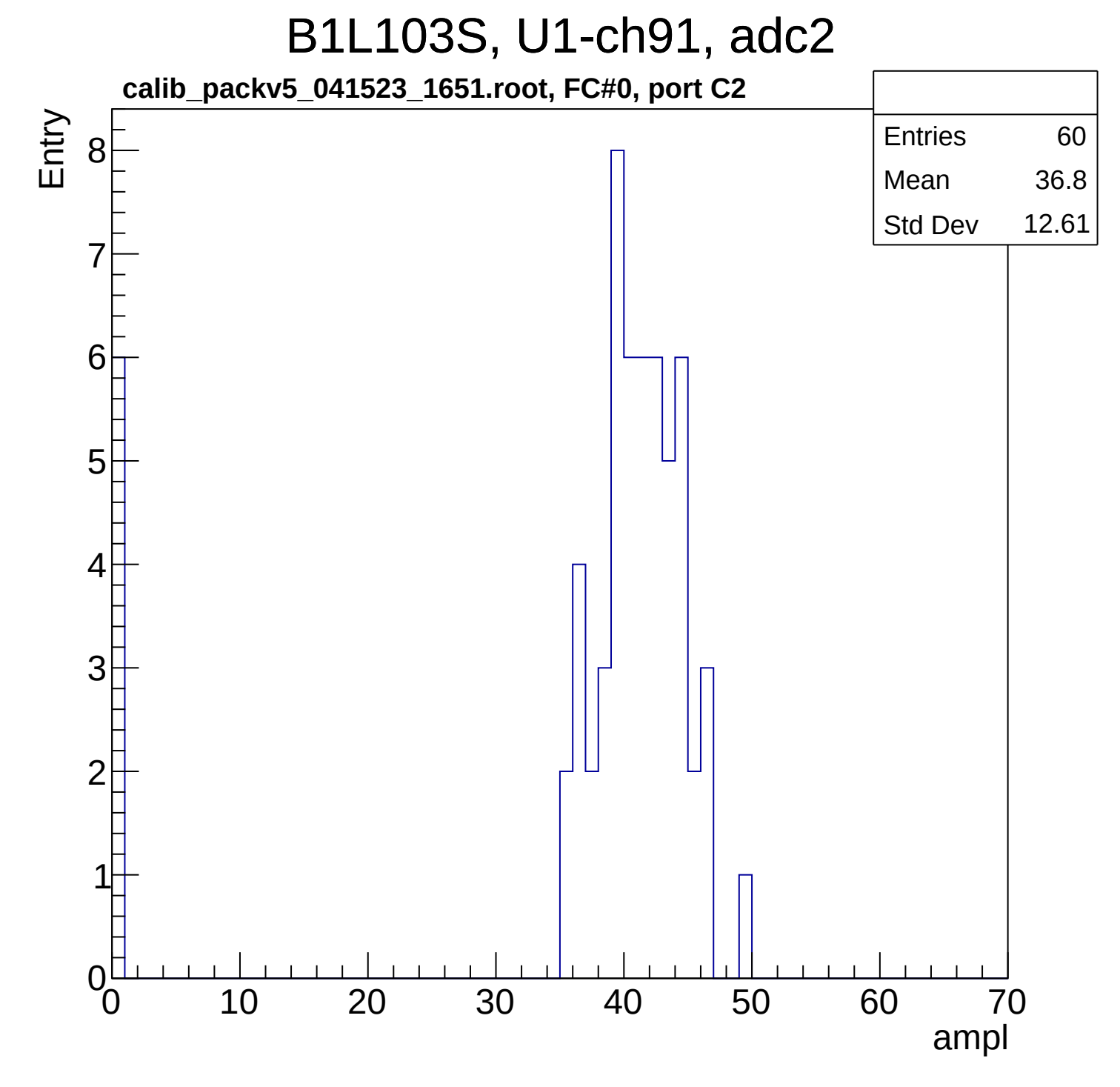
B1L103S, U1-ch91, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 36.8
Std Dev 12.61
Entry
ampl
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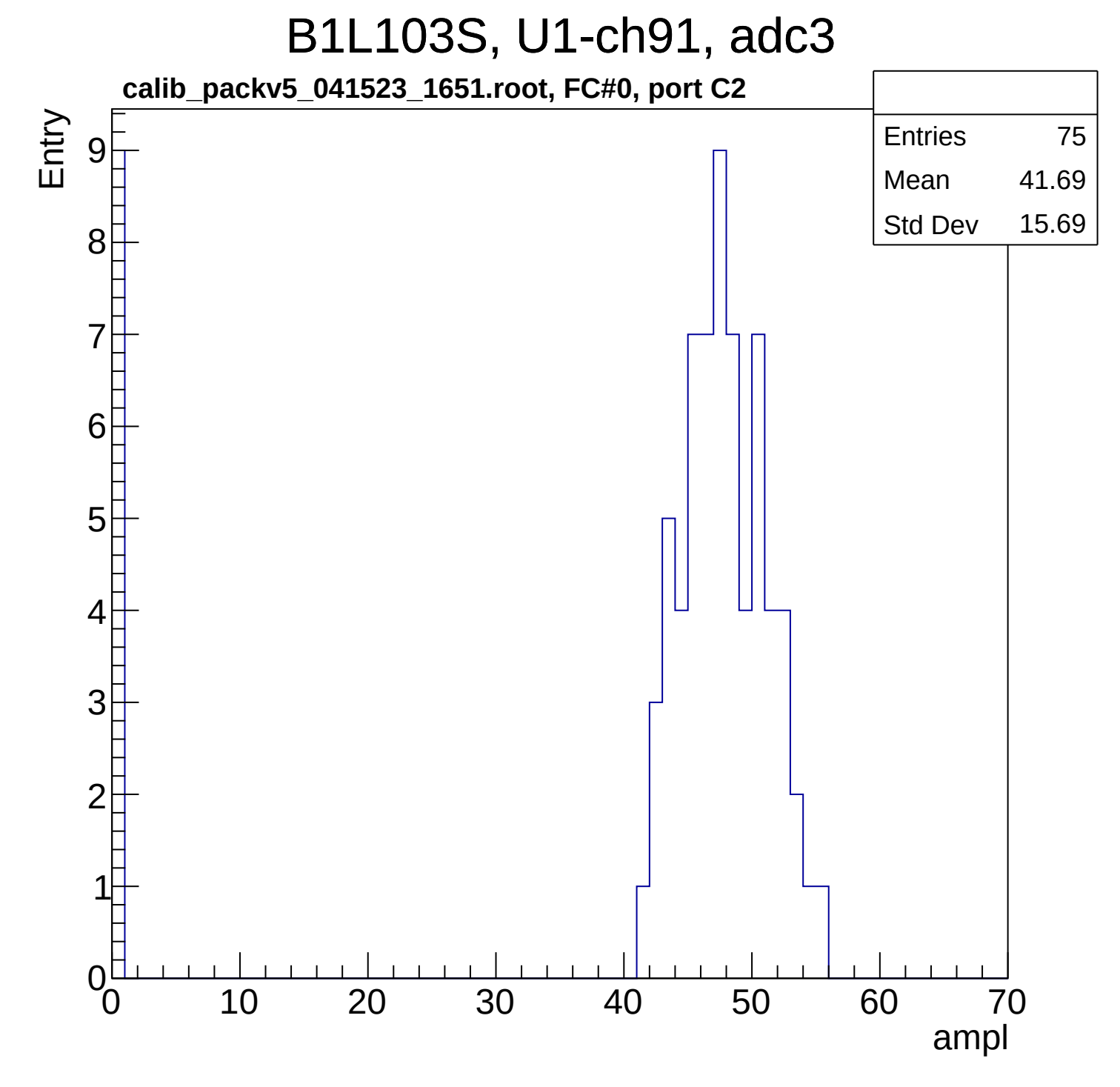
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U1-ch91, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 41.69
Std Dev 15.69
Entry
ampl
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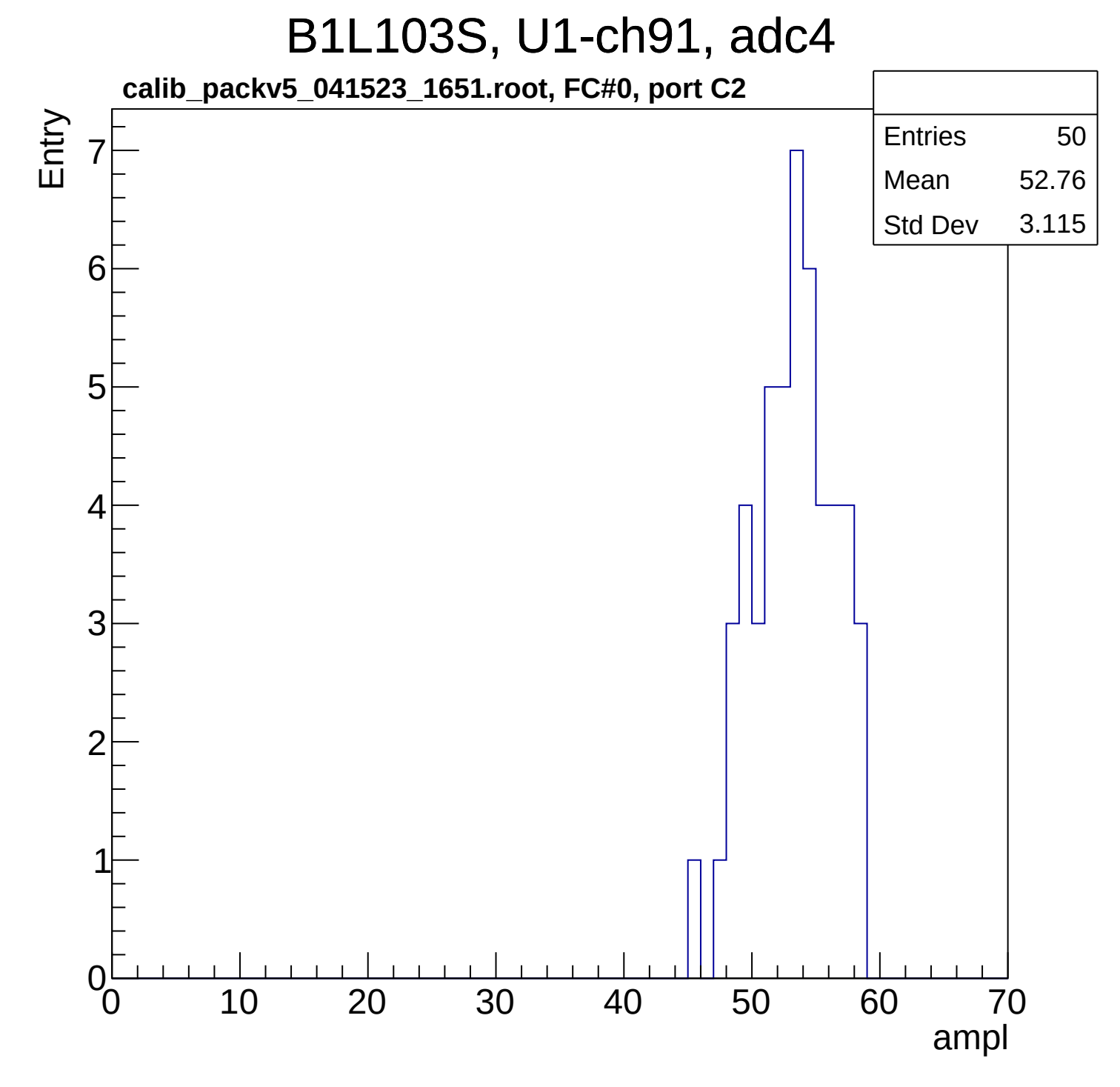
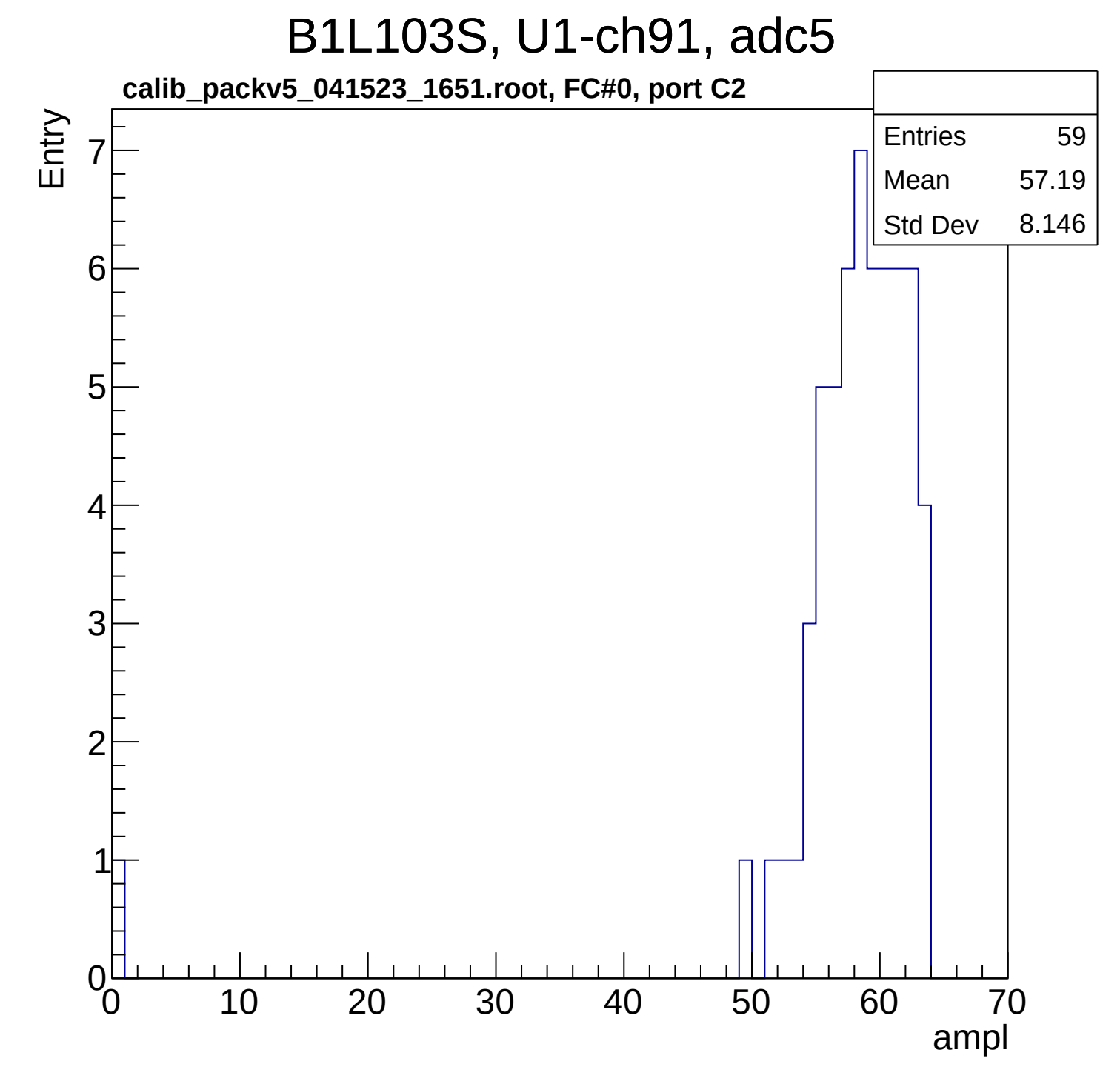
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U1-ch91, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 52.76
Std Dev 3.115
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U1-ch91, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 57.19
Std Dev 8.146
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
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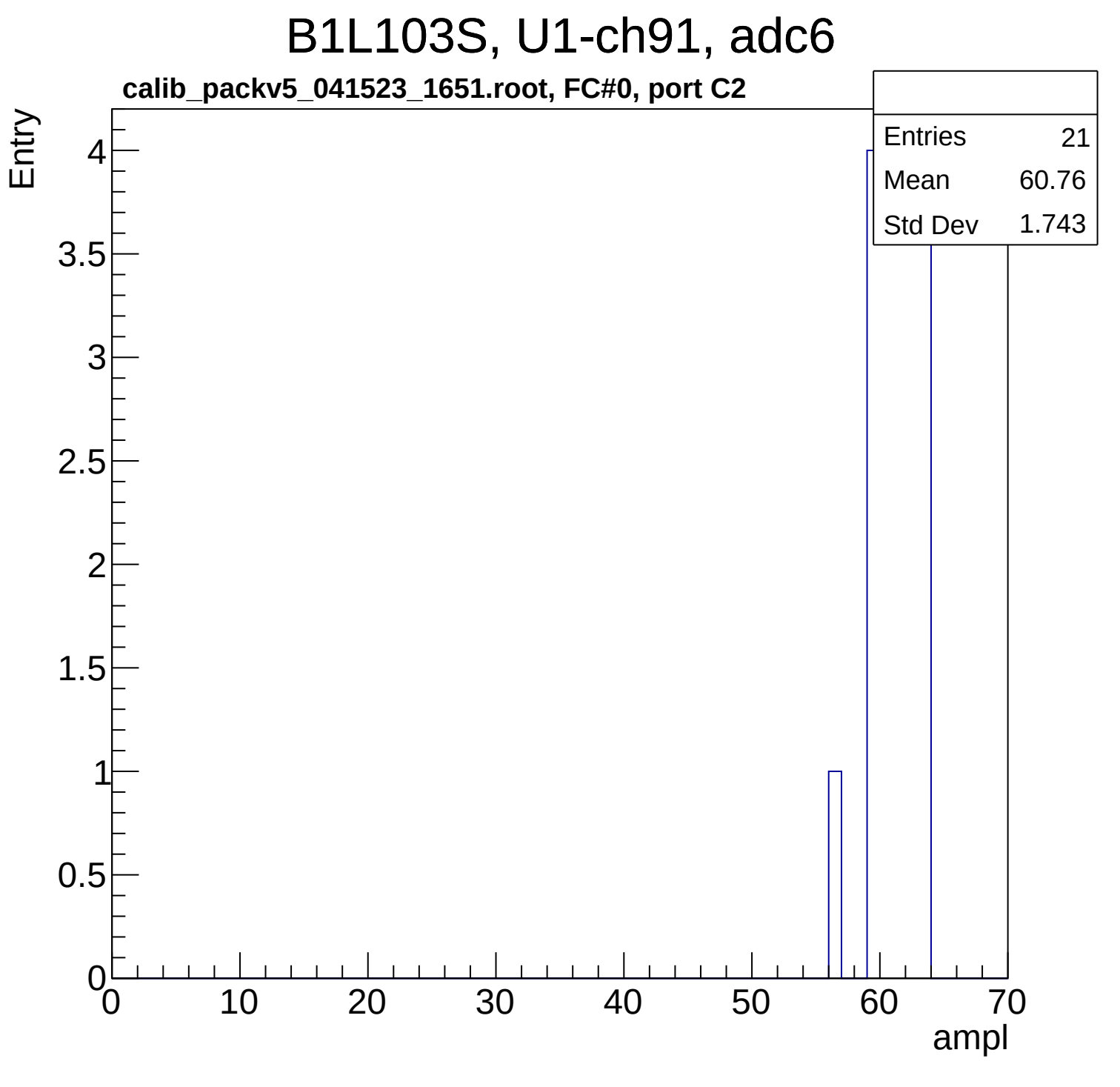
40
50
60
70


B1L103S, U1-ch91, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 60.76
Std Dev 1.743
Entry
ampl
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1.5
2
2.5
3
3.5
4
0
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60
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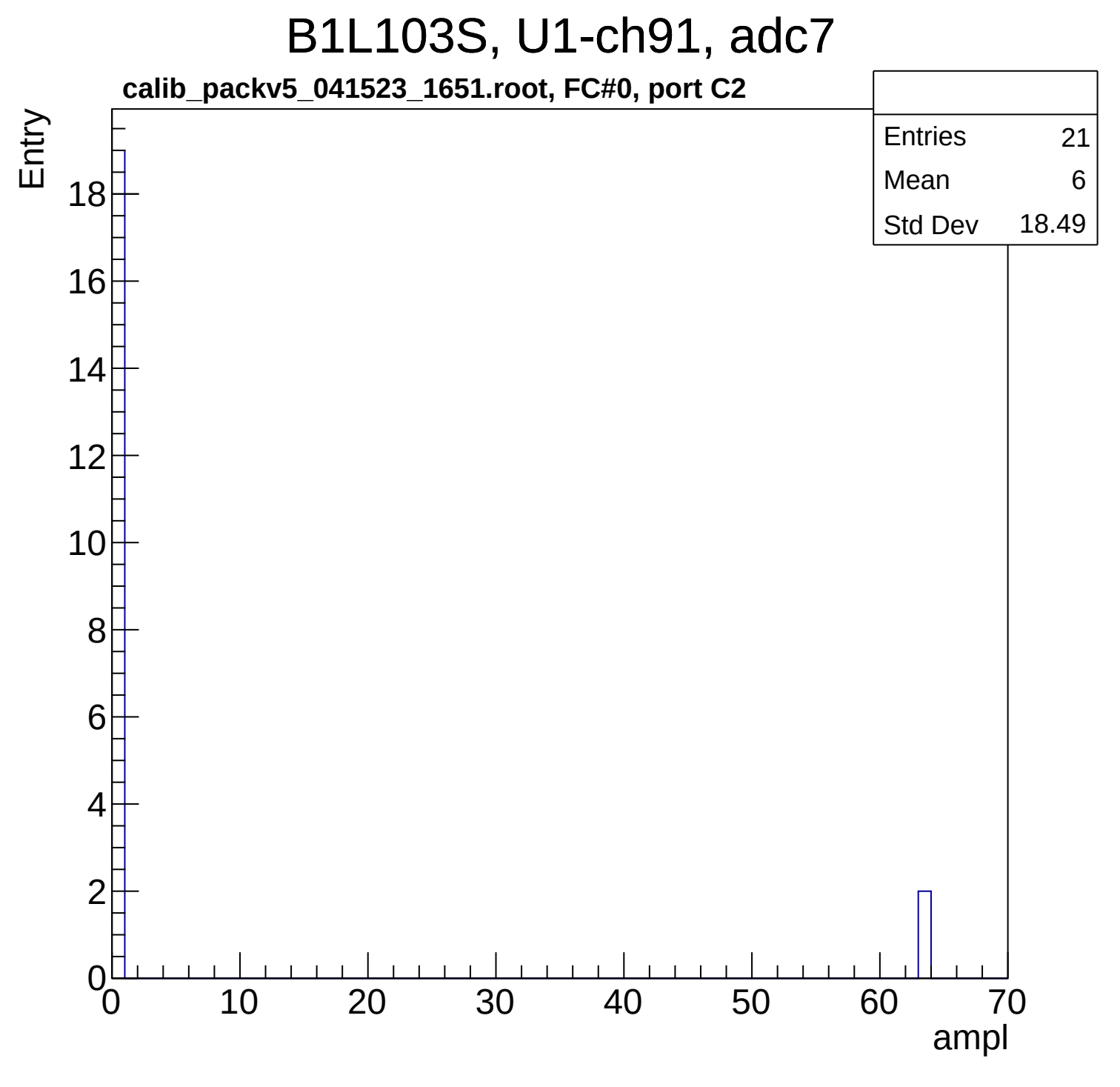
B1L103S, U1-ch91, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 6
Std Dev 18.49
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
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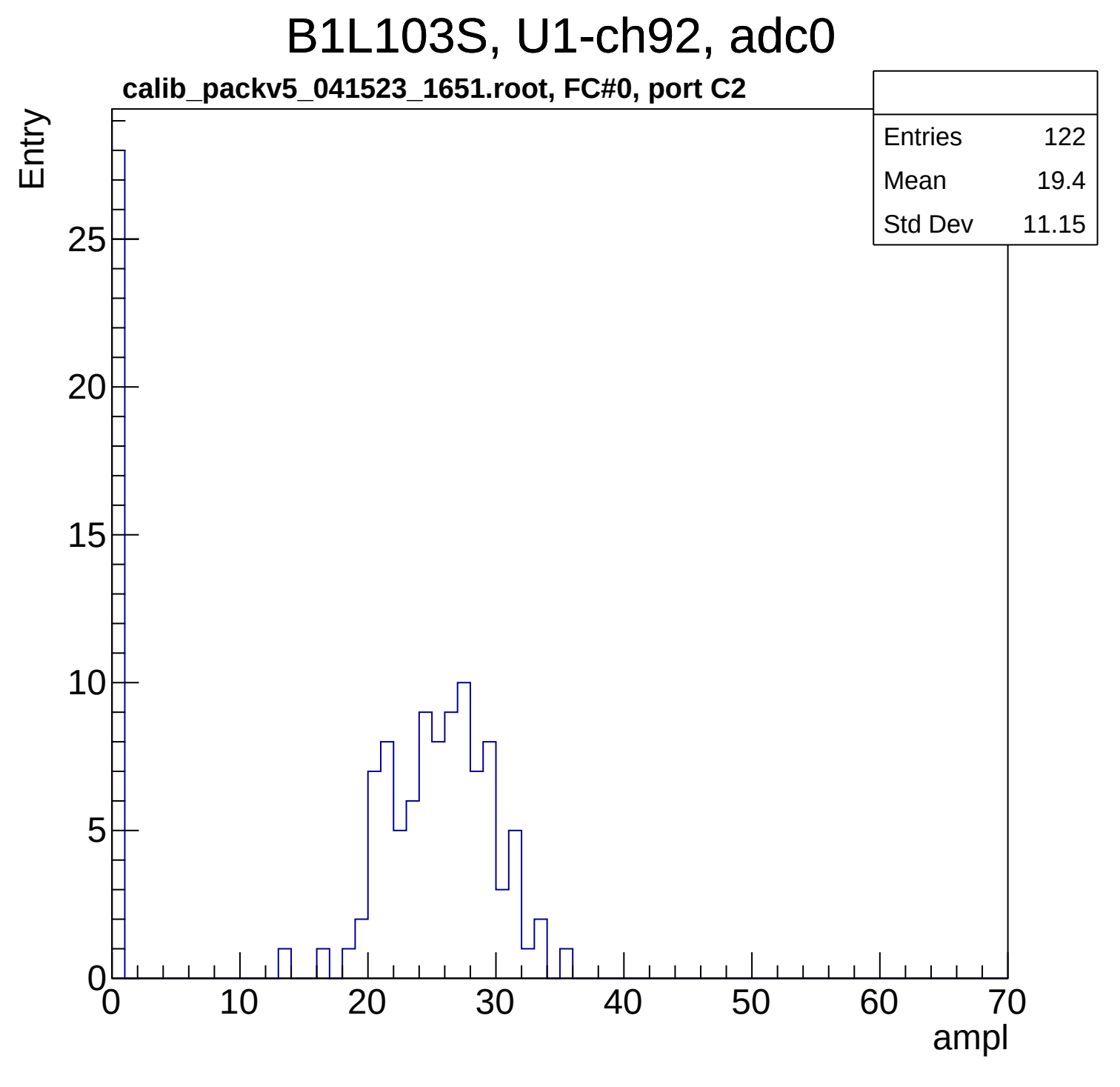
50
60
70
ampl


B1L103S, U1-ch92, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 122
Mean 19.4
Std Dev 11.15
Entry
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5
10
15
20
25
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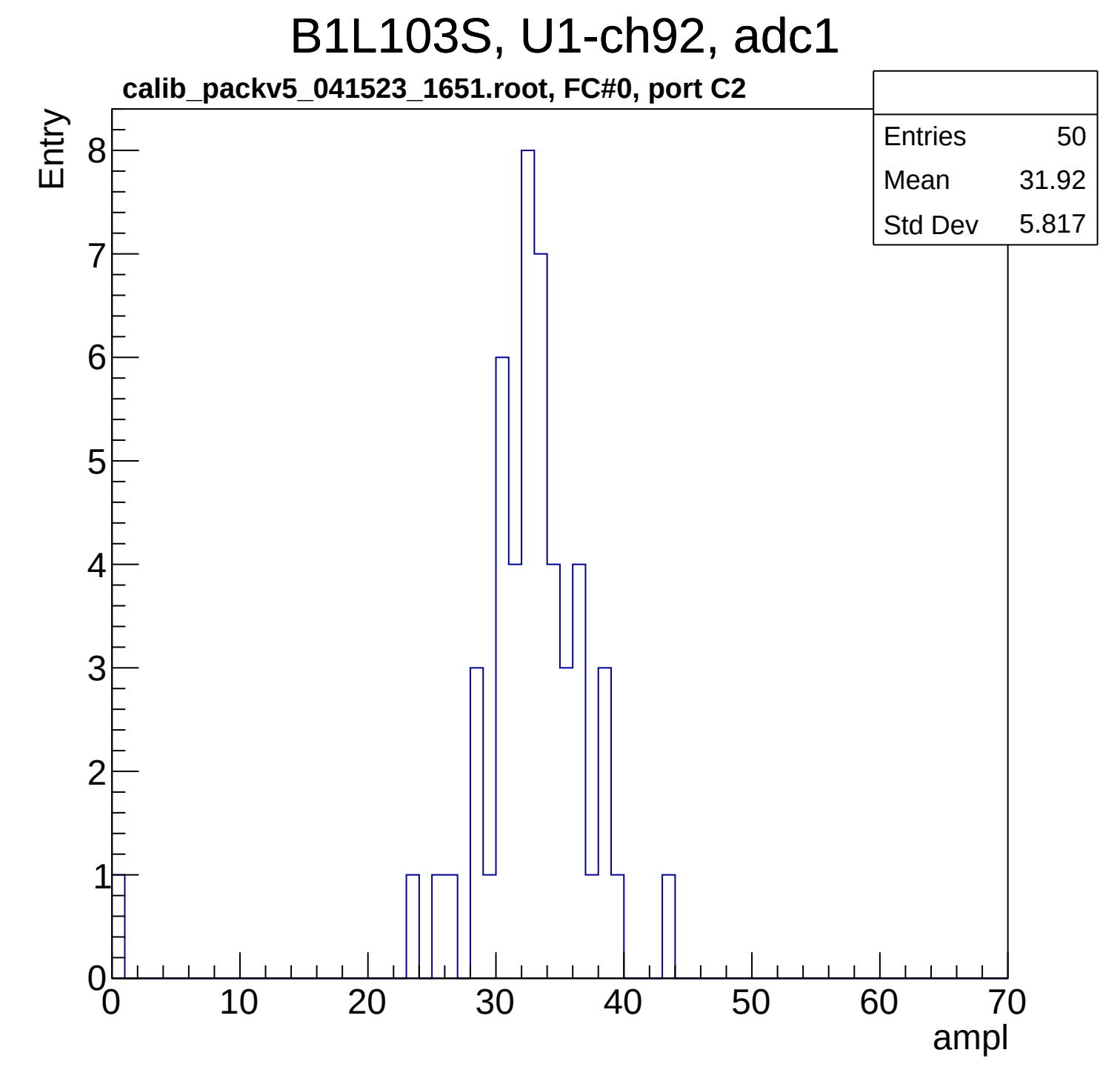
70
ampl


B1L103S, U1-ch92, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 31.92
Std Dev 5.817
Entry
ampl
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2
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60
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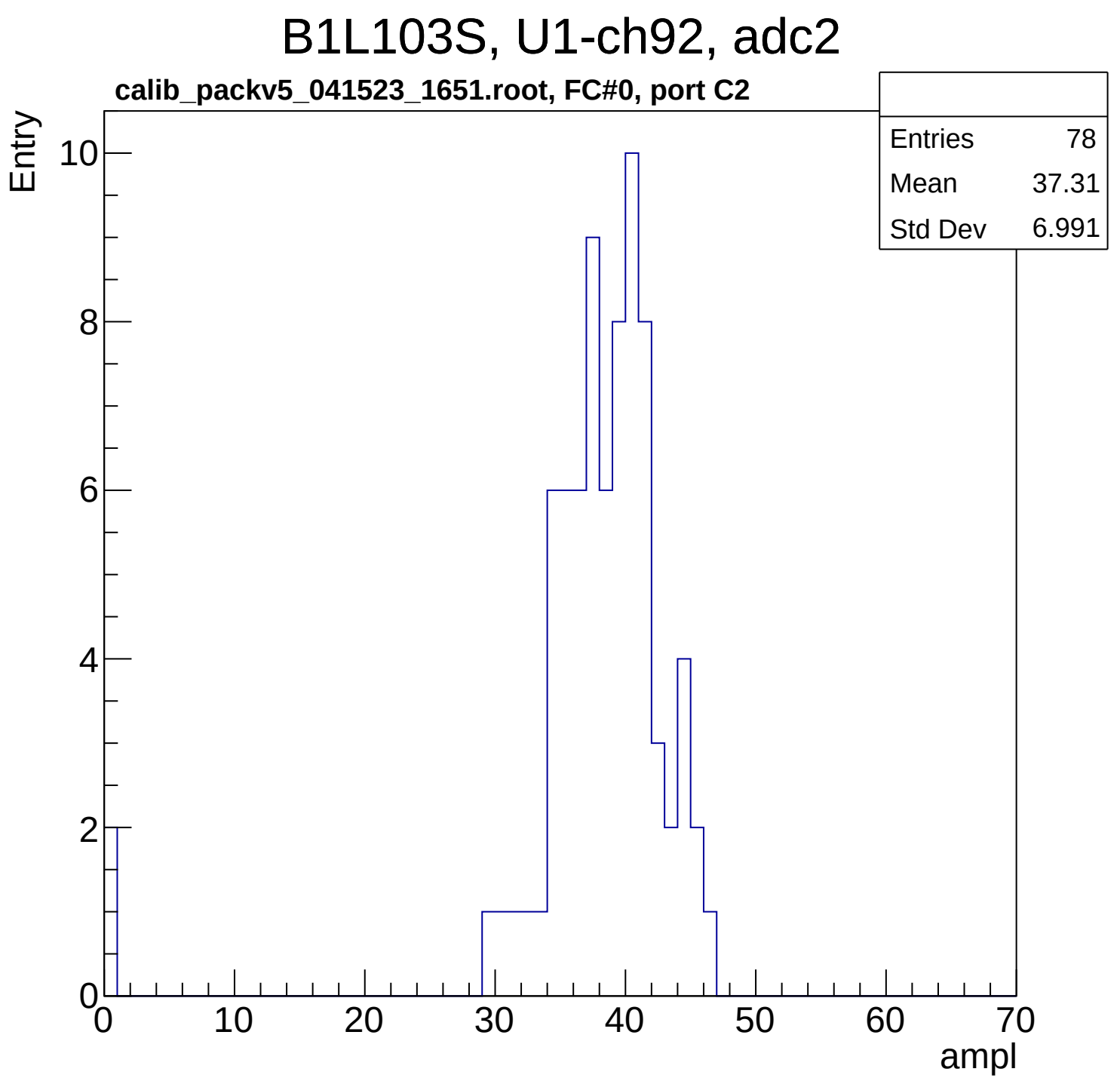
B1L103S, U1-ch92, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 37.31
Std Dev 6.991
Entry
ampl
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2
4
6
8
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0
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20
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40
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60
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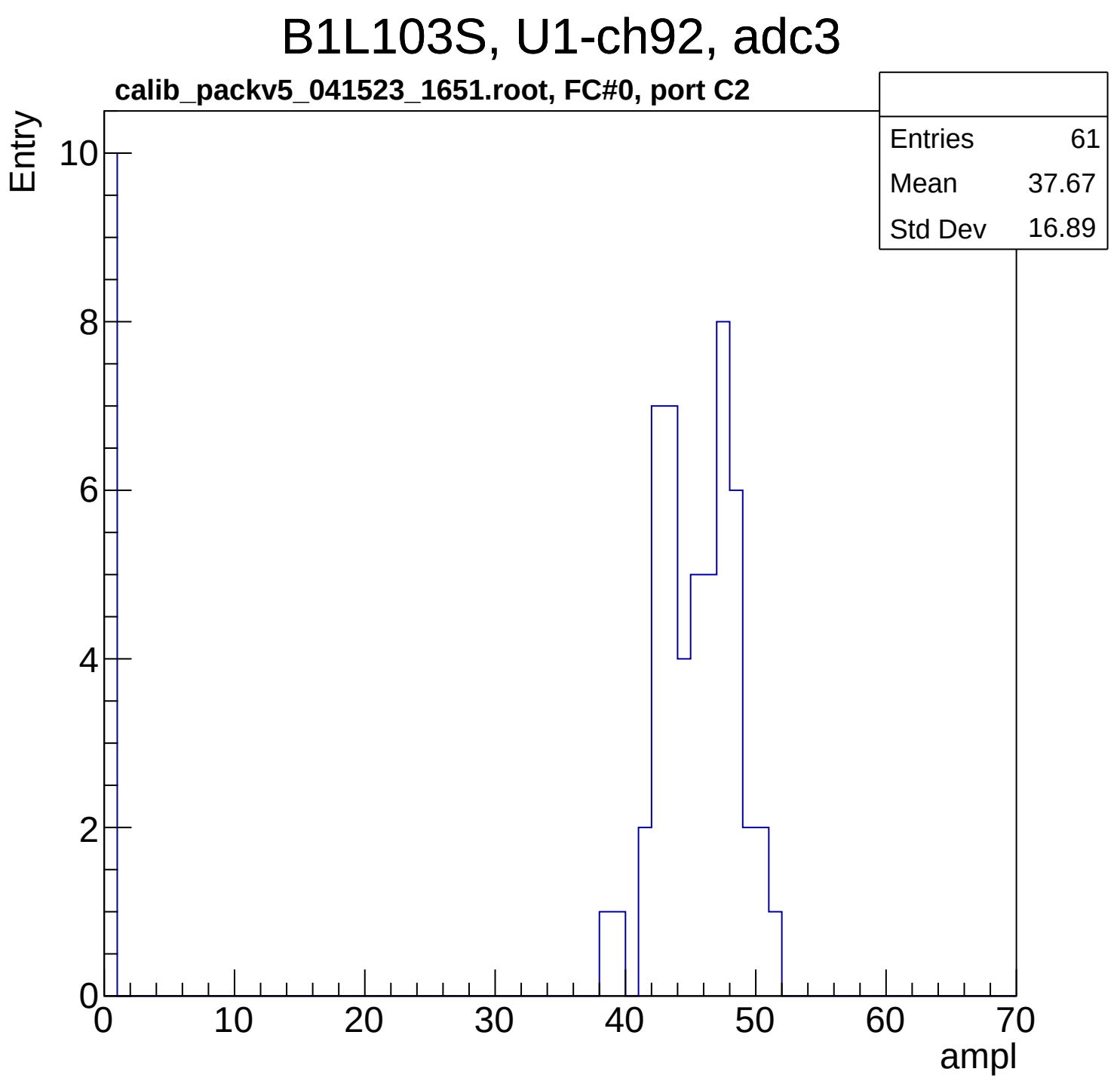
B1L103S, U1-ch92, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 37.67
Std Dev 16.89
Entry
ampl
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2
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8
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0
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40
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60
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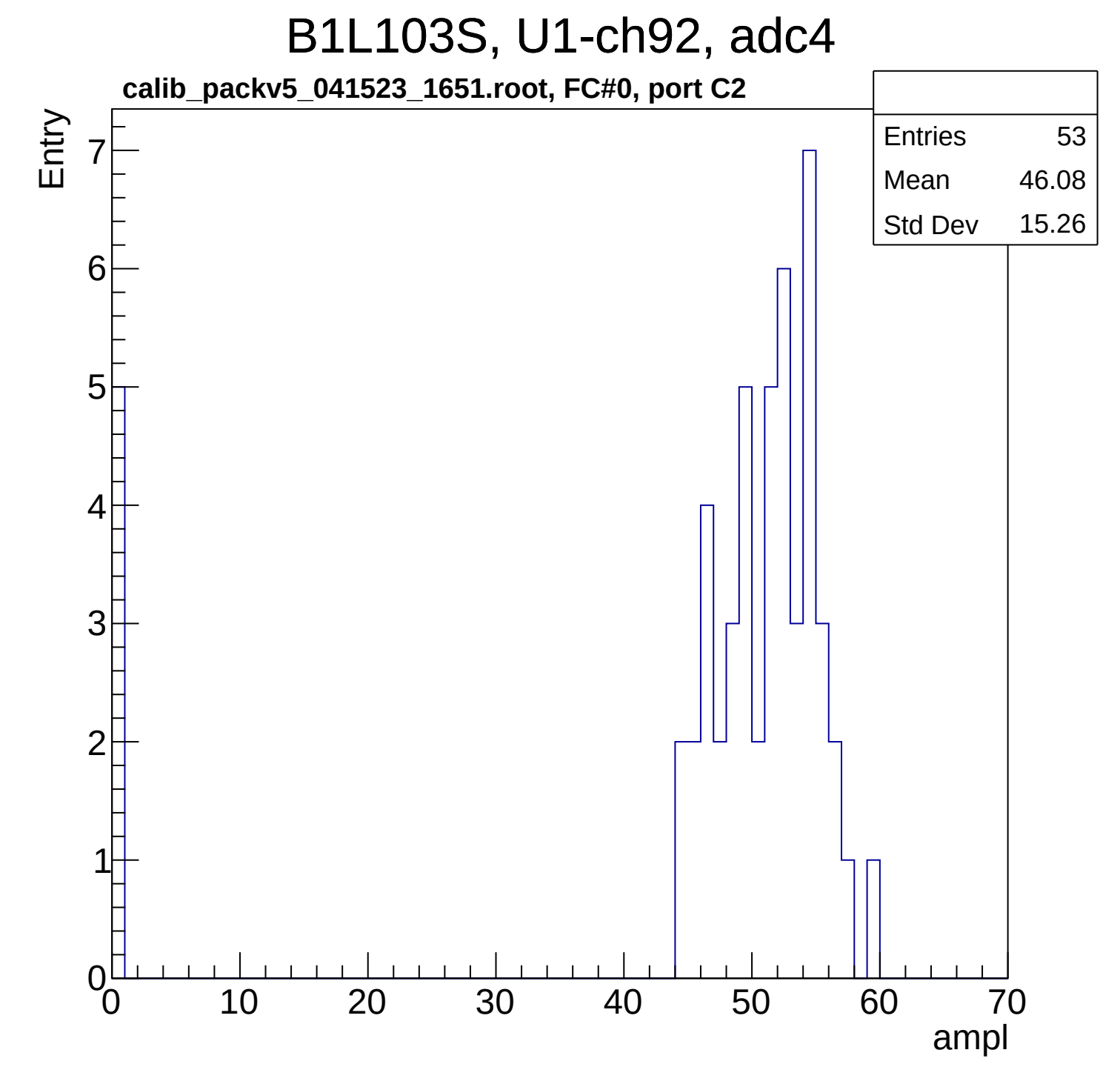
B1L103S, U1-ch92, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 46.08
Std Dev 15.26
Entry
ampl
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3
4
5
6
7
0
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20
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40
50
60
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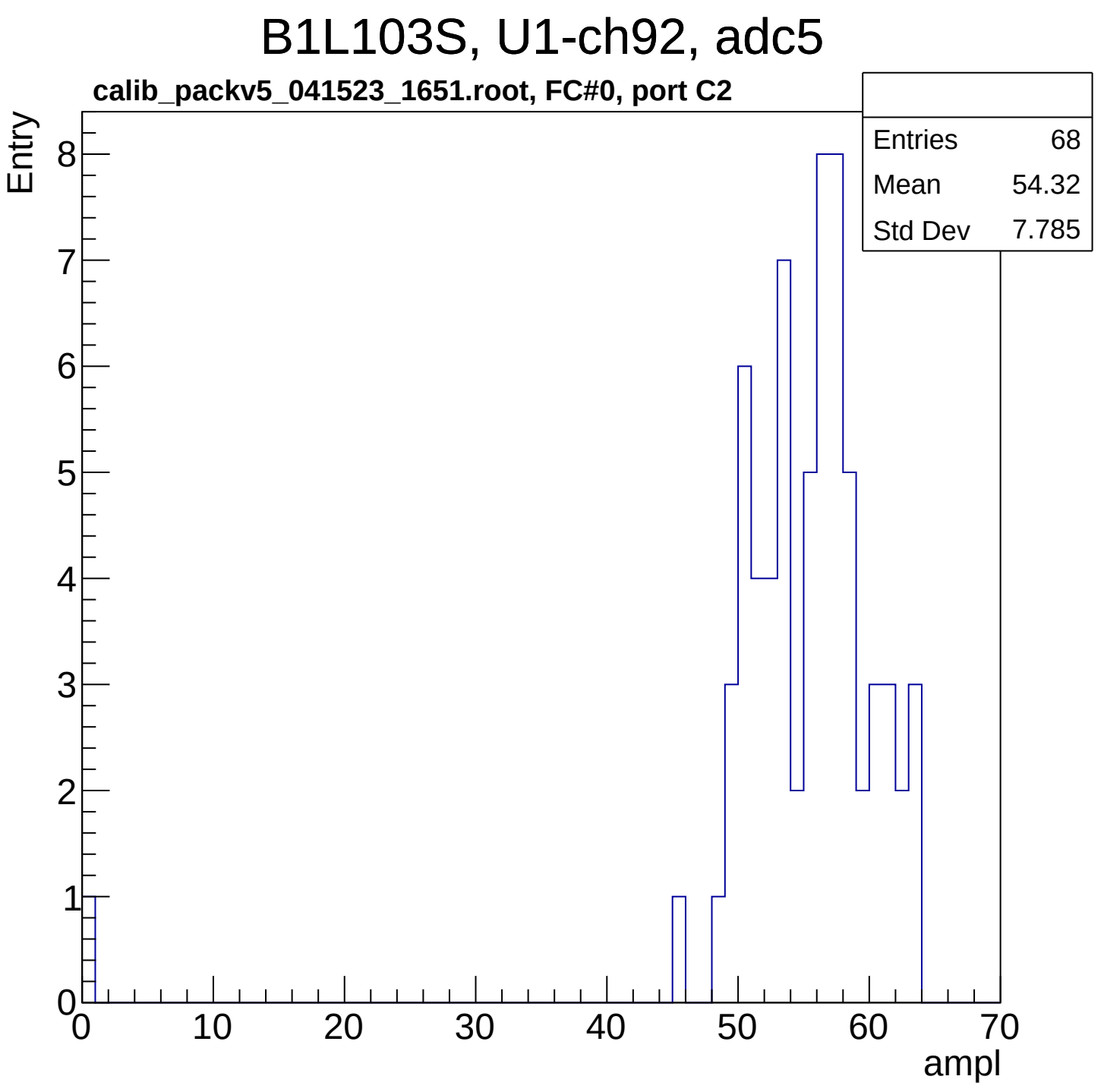
B1L103S, U1-ch92, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 54.32
Std Dev 7.785
Entry
ampl
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5
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0
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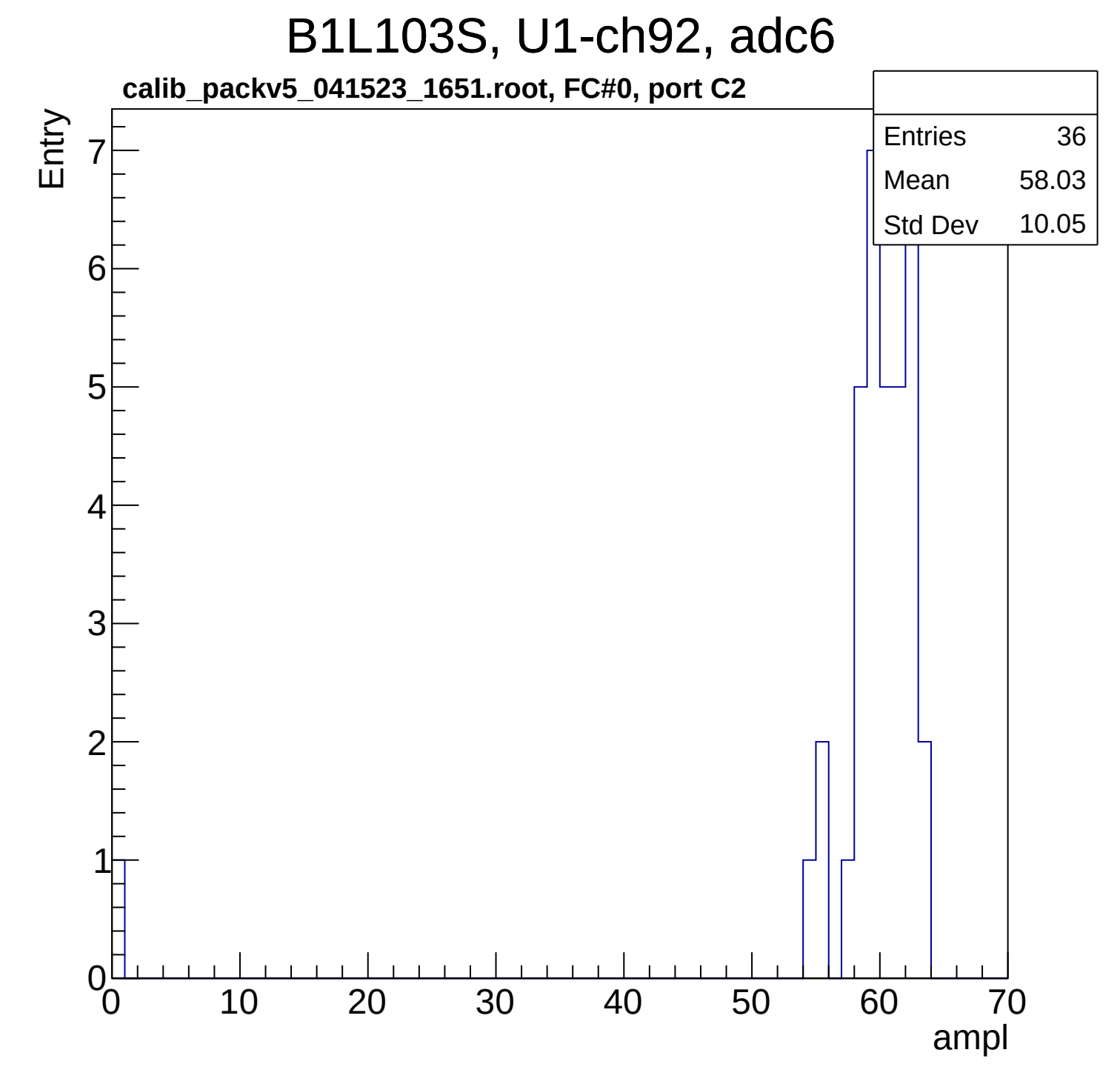
B1L103S, U1-ch92, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 36
Mean 58.03
Std Dev 10.05
Entry
ampl
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2
3
4
5
6
7
0
10
20
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40
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60
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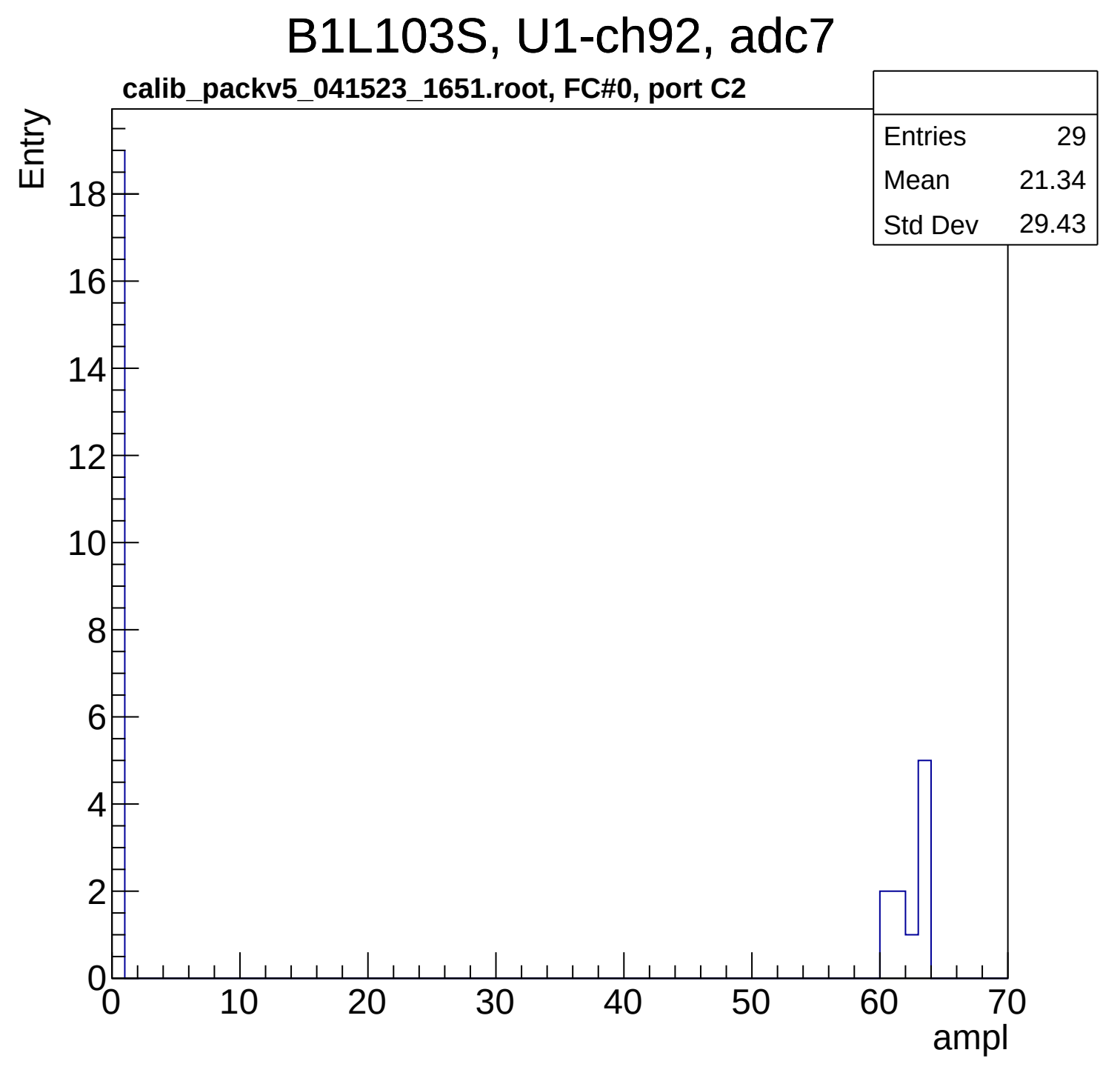
B1L103S, U1-ch92, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 29
Mean 21.34
Std Dev 29.43
Entry
ampl
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6
8
10
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16
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0
10
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40
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60
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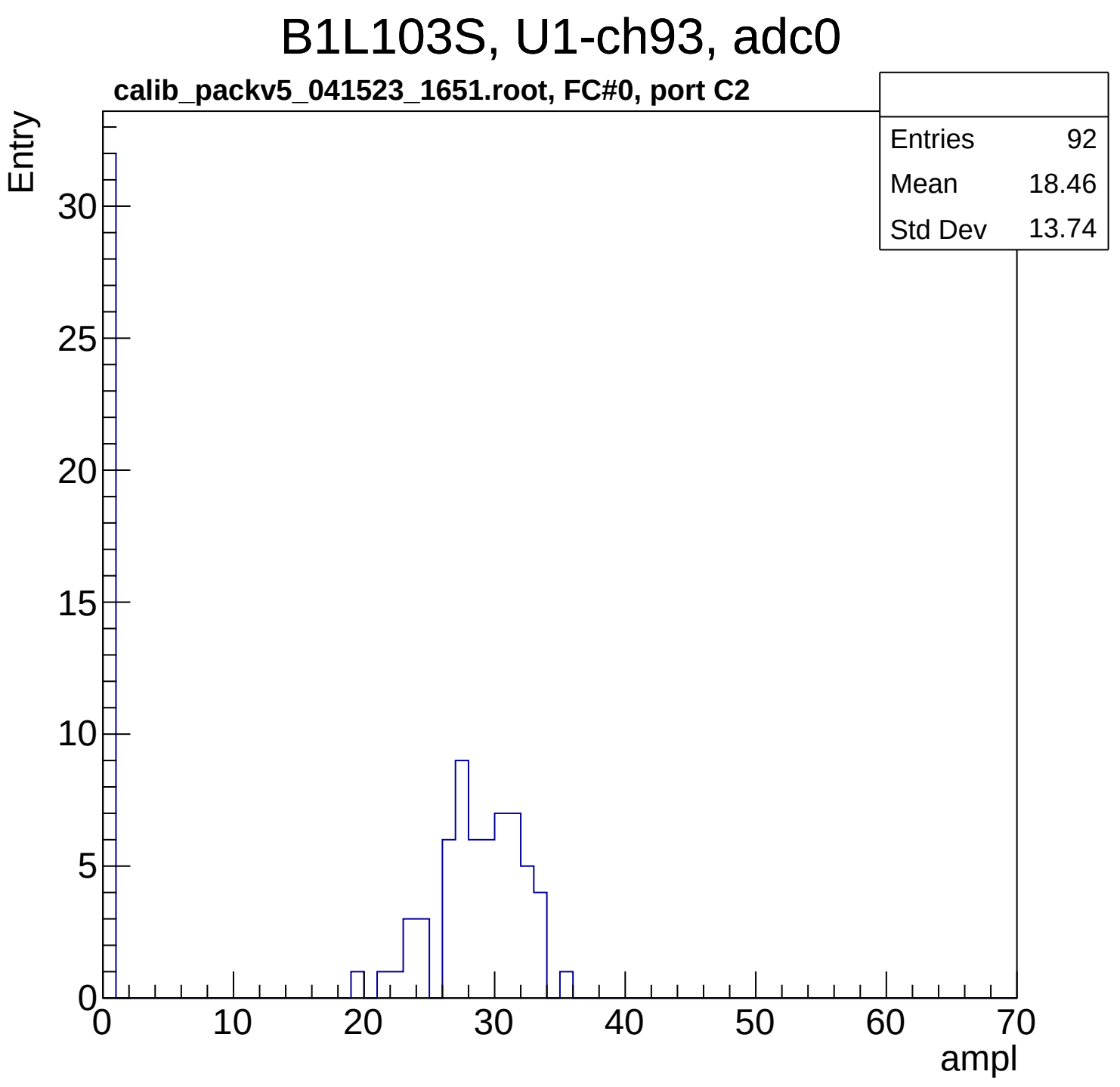
B1L103S, U1-ch93, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 92
Mean 18.46
Std Dev 13.74
Entry
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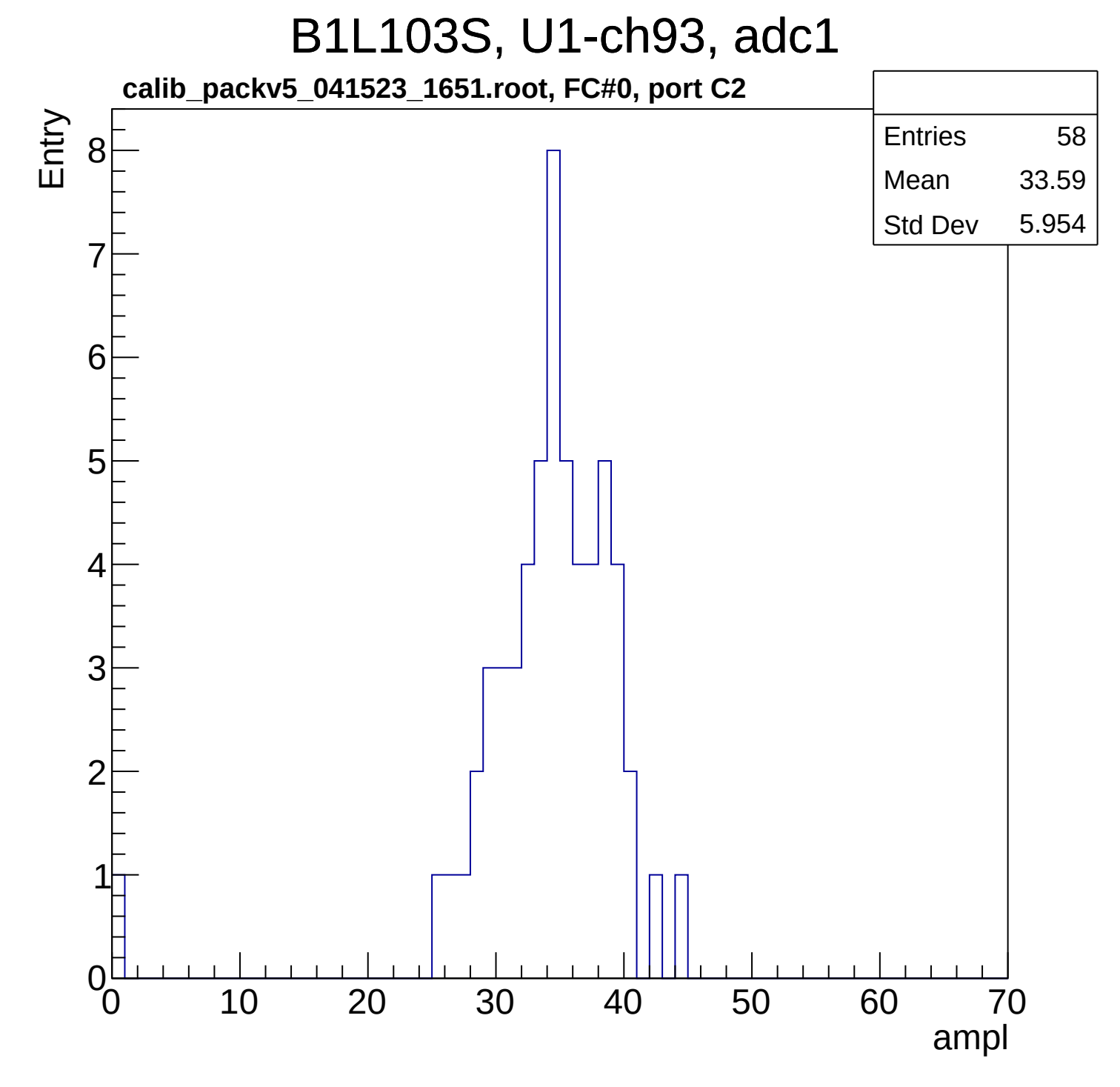
5
10
15
20
25
30
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch93, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 33.59
Std Dev 5.954
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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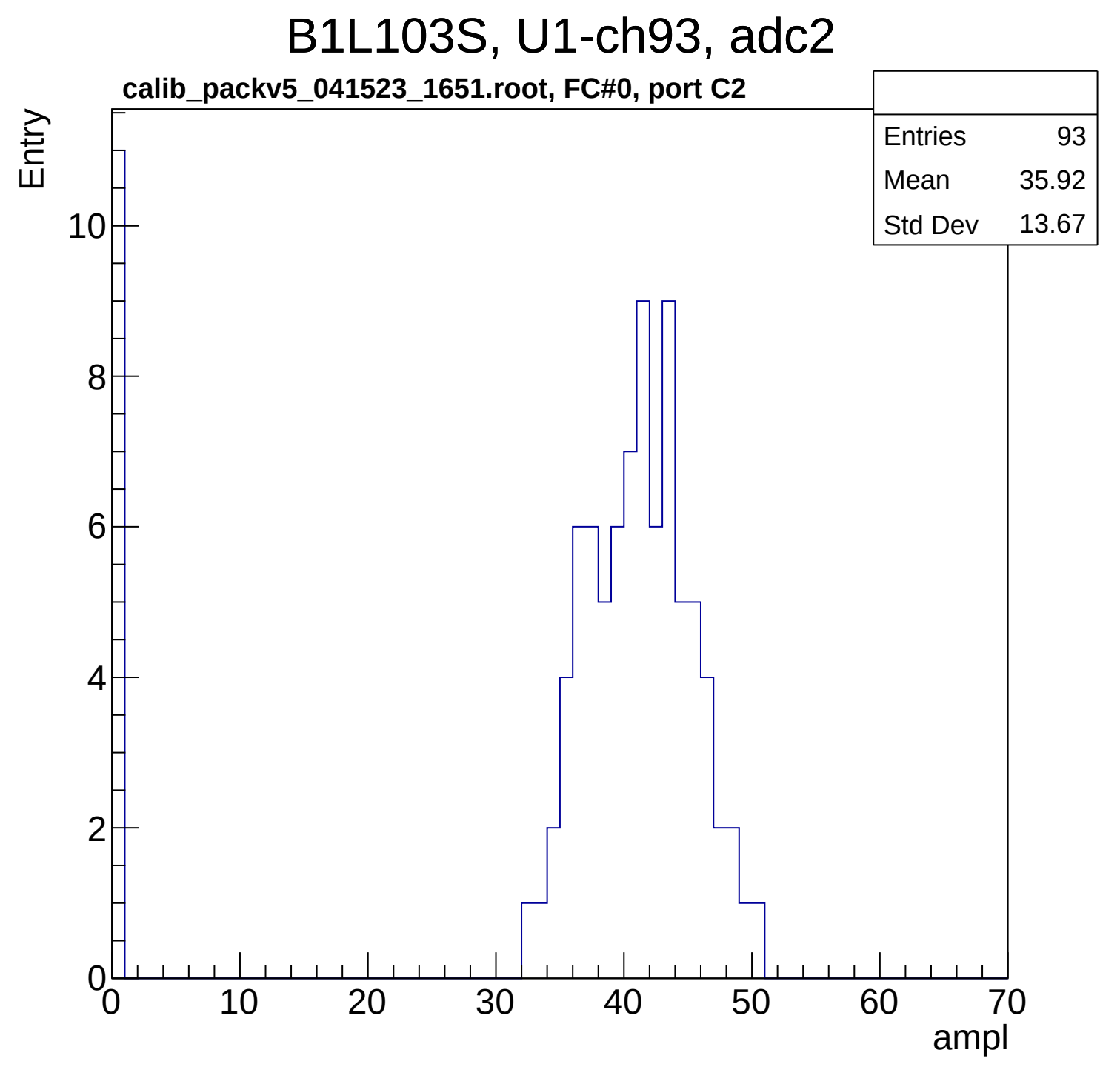
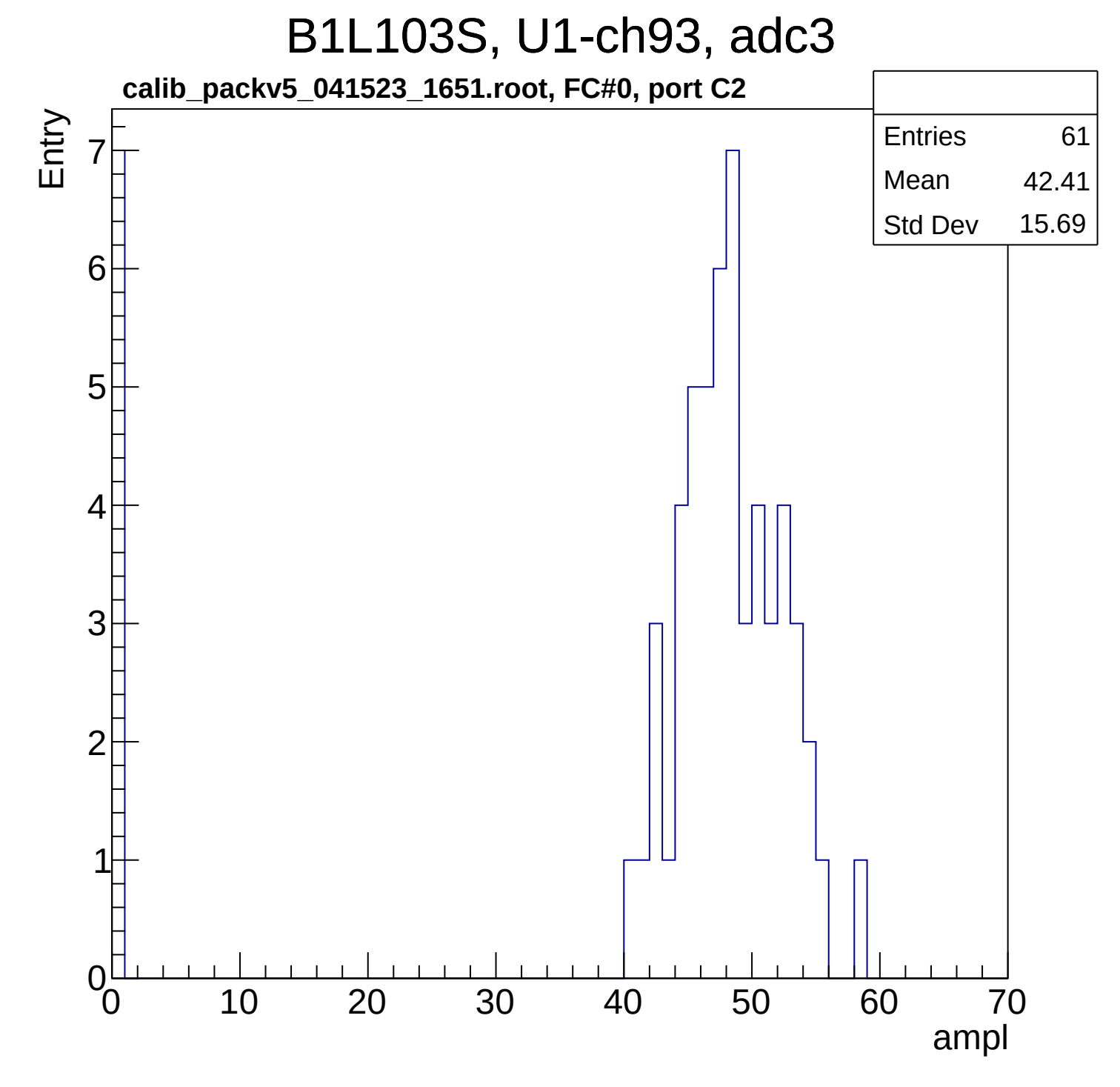

B1L103S, U1-ch93, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 93
Mean 35.92
Std Dev 13.67
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch93, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 42.41
Std Dev 15.69
Entry
ampl
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2
3
4
5
6
7
0
10
20
30
40
50
60
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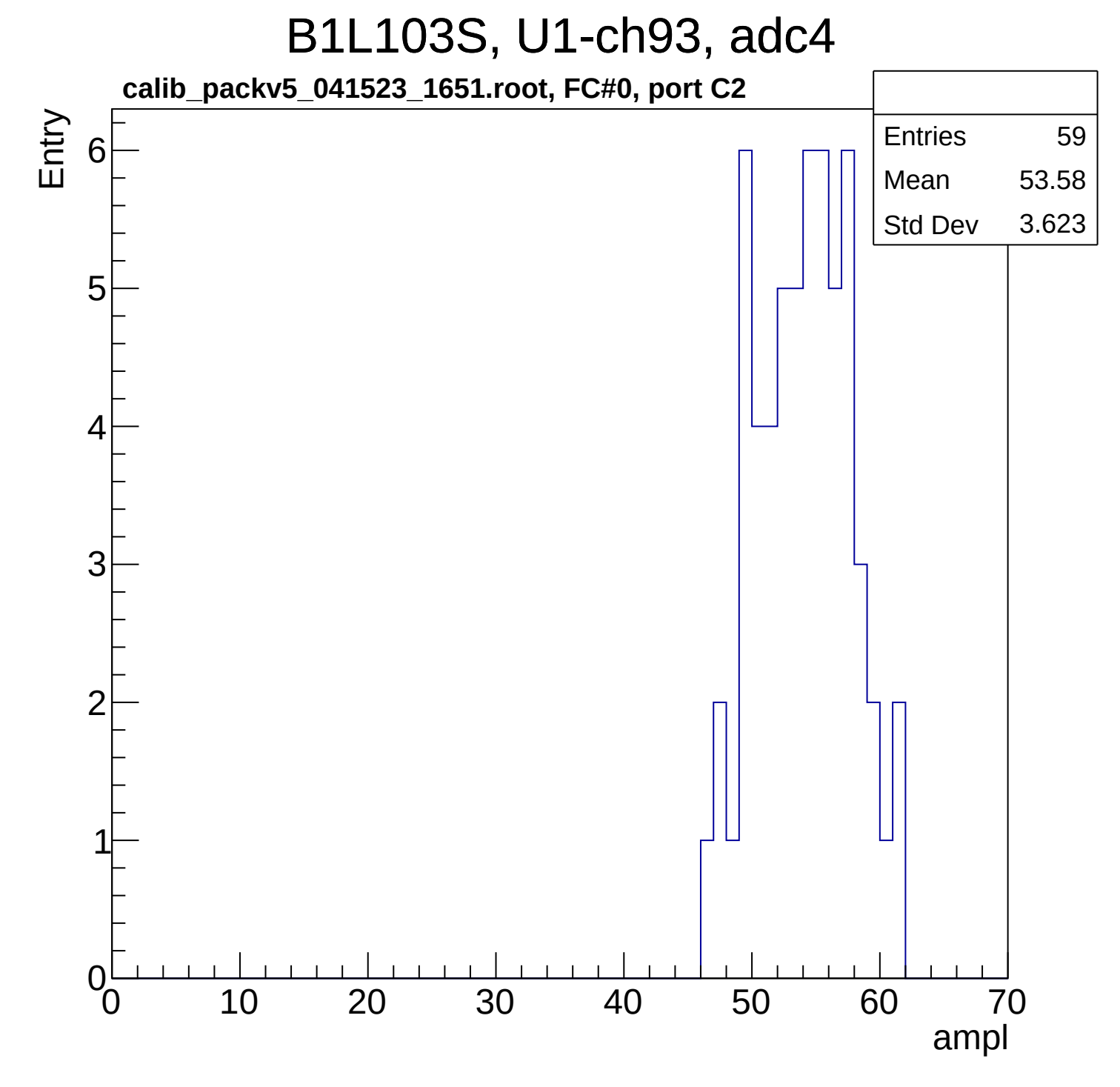
B1L103S, U1-ch93, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 53.58
Std Dev 3.623
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
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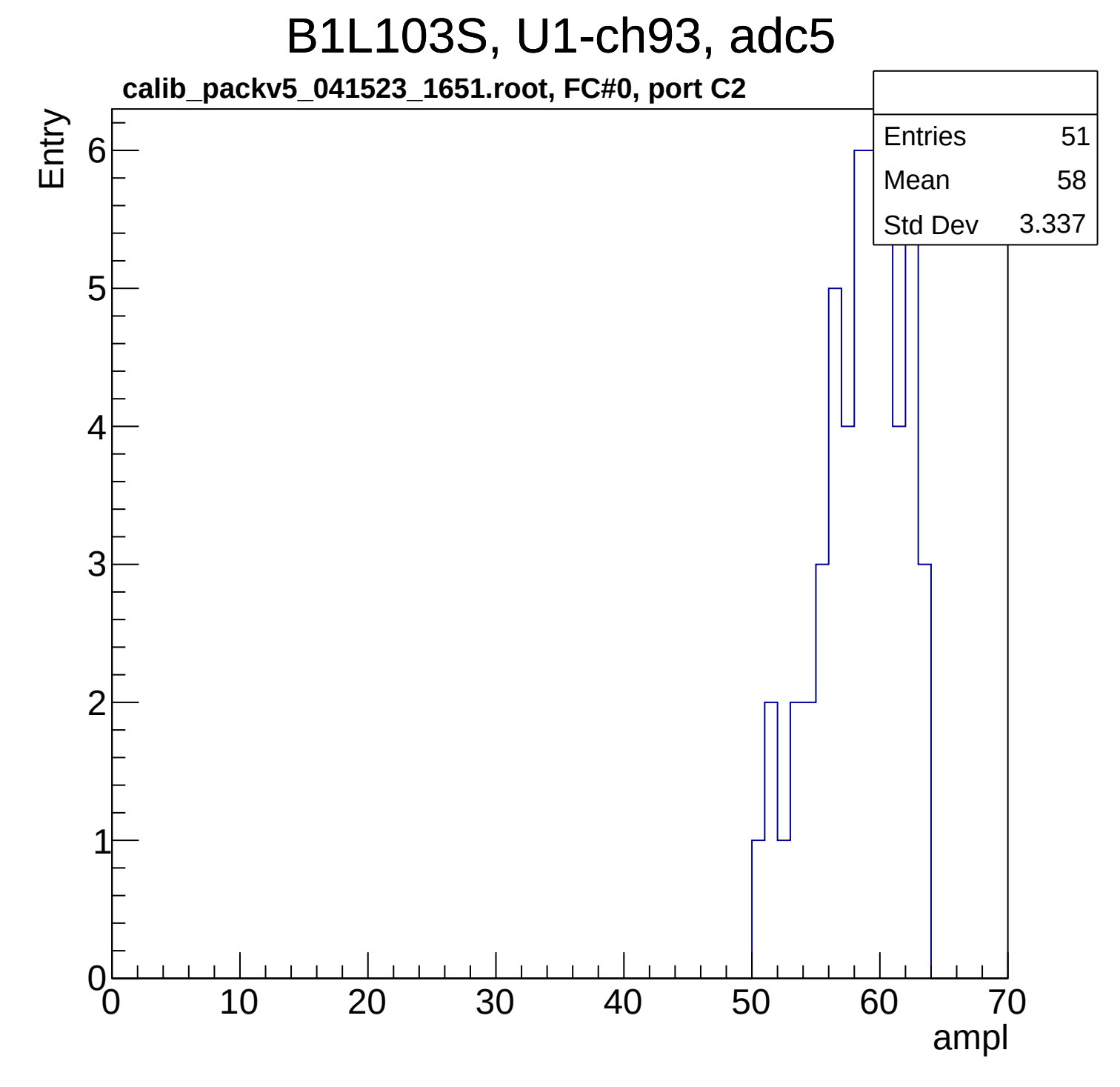
B1L103S, U1-ch93, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 58
Std Dev 3.337
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
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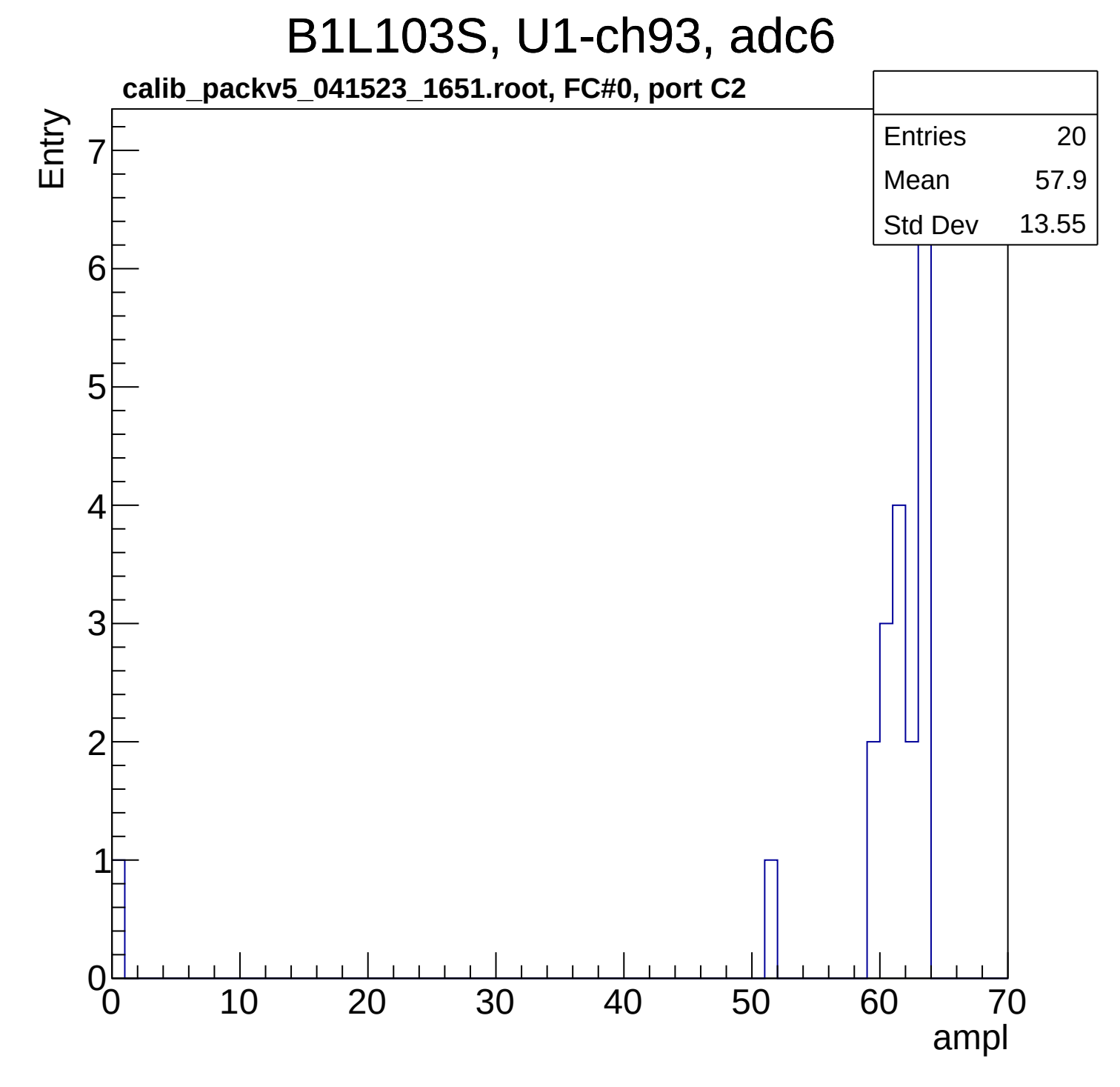
B1L103S, U1-ch93, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 57.9
Std Dev 13.55
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
30
40
50
60
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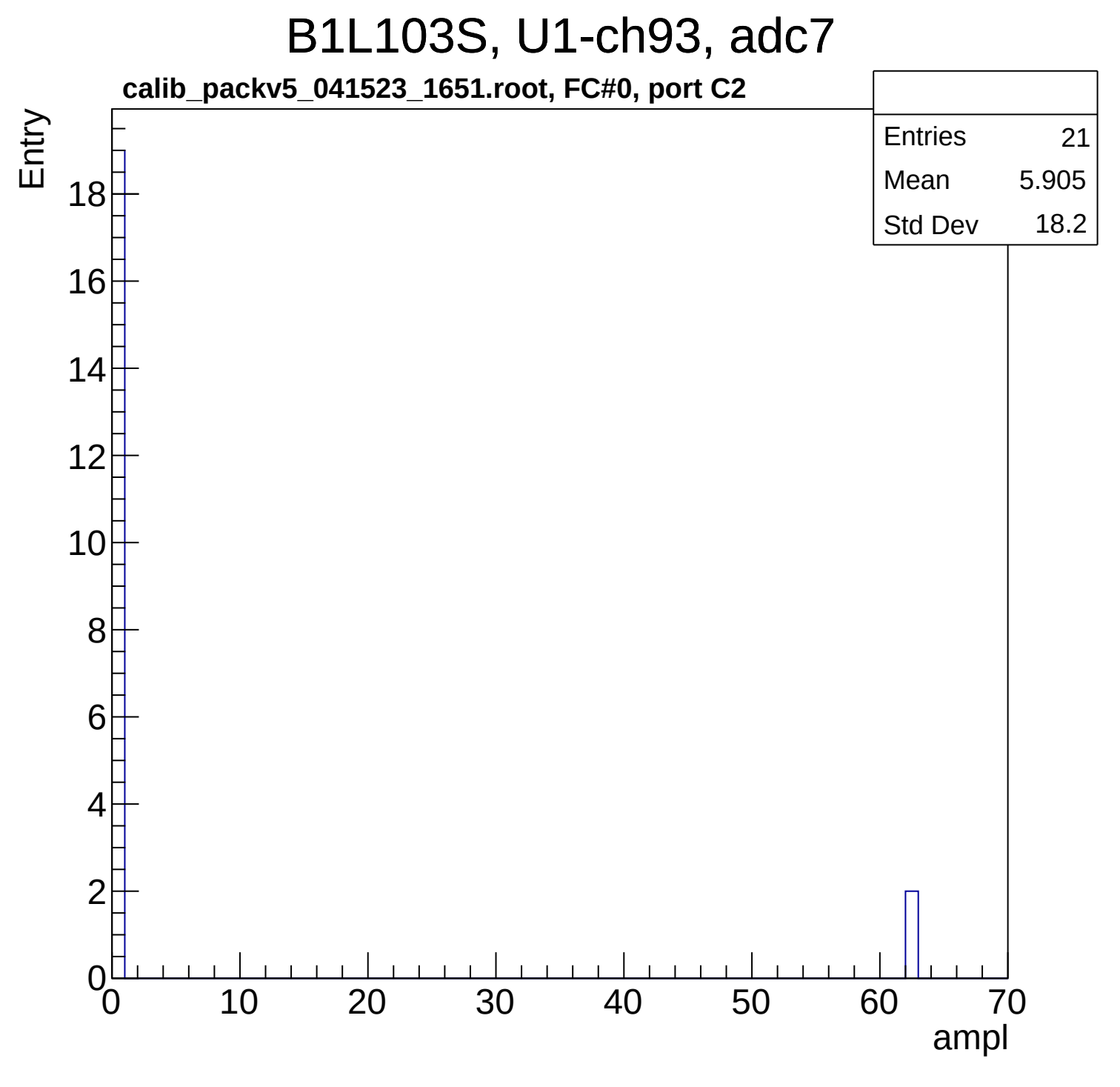
B1L103S, U1-ch93, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 5.905
Std Dev 18.2
Entry
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6
8
10
12
14
16
18
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10
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30
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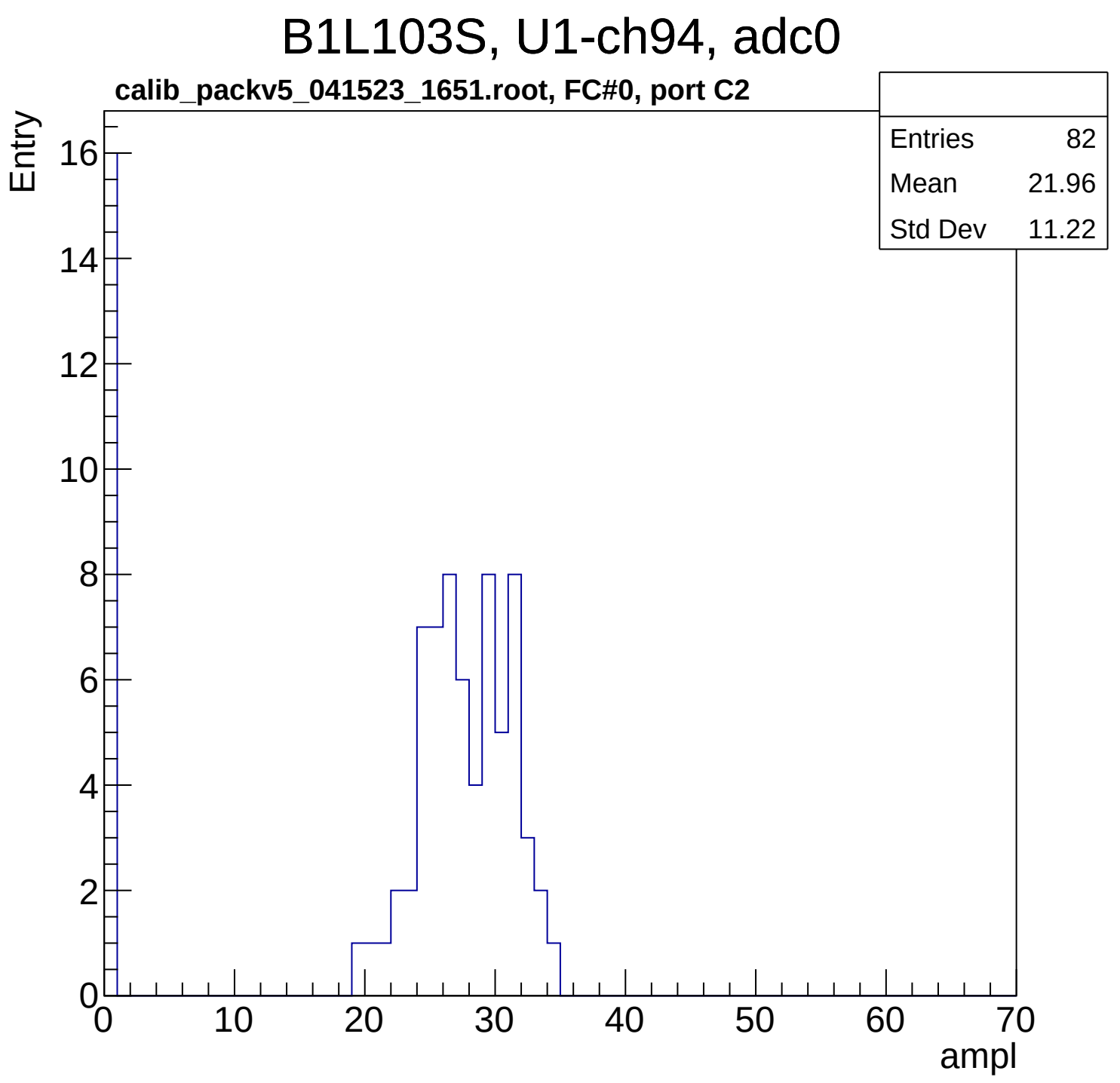
50
60
70
ampl


B1L103S, U1-ch94, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 21.96
Std Dev 11.22
Entry
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4
6
8
10
12
14
16
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10
20
30
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50
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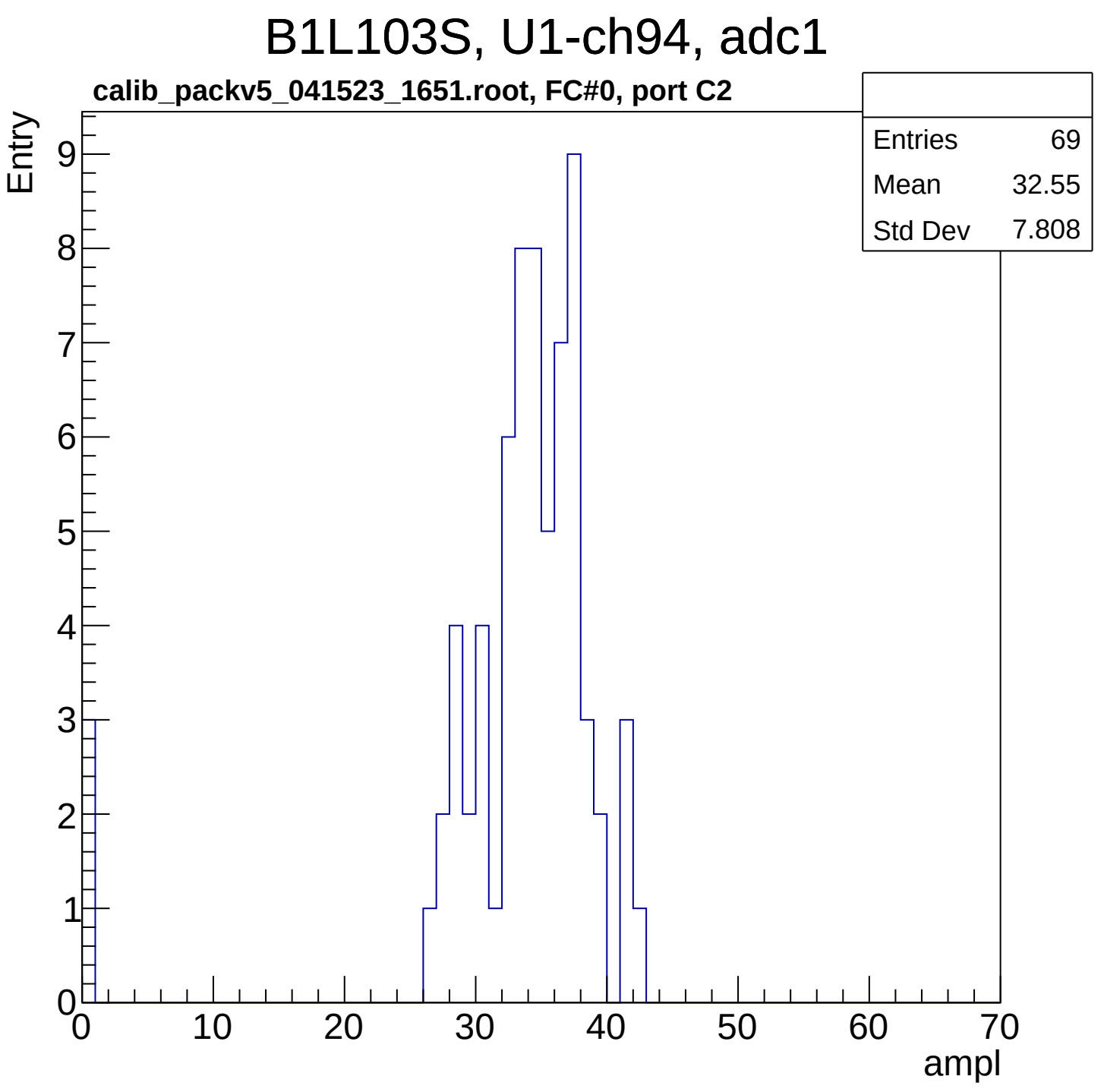
70
ampl


B1L103S, U1-ch94, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 32.55
Std Dev 7.808
Entry
ampl
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2
3
4
5
6
7
8
9
0
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60
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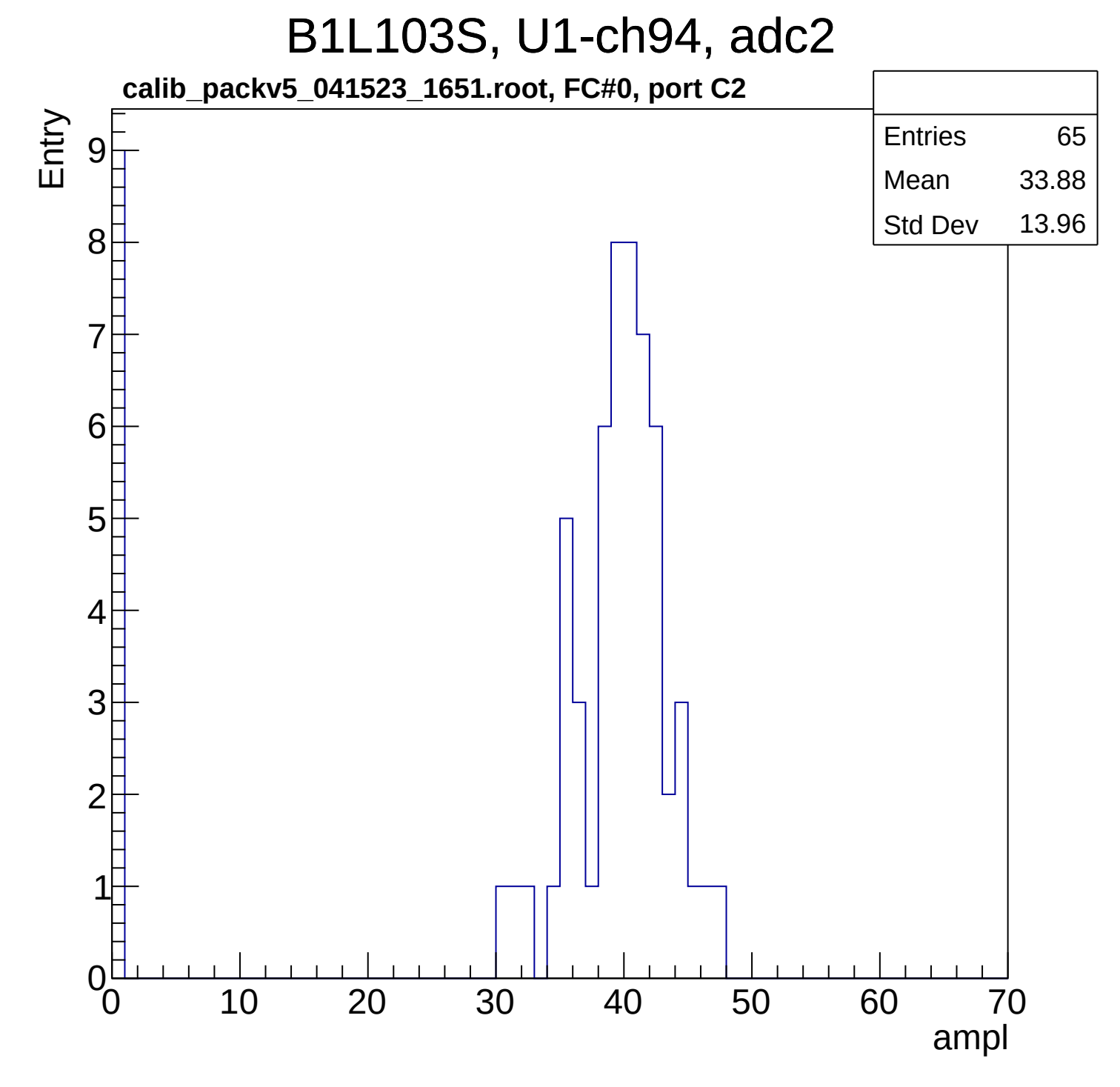
B1L103S, U1-ch94, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 33.88
Std Dev 13.96
Entry
ampl
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3
4
5
6
7
8
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0
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20
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40
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60
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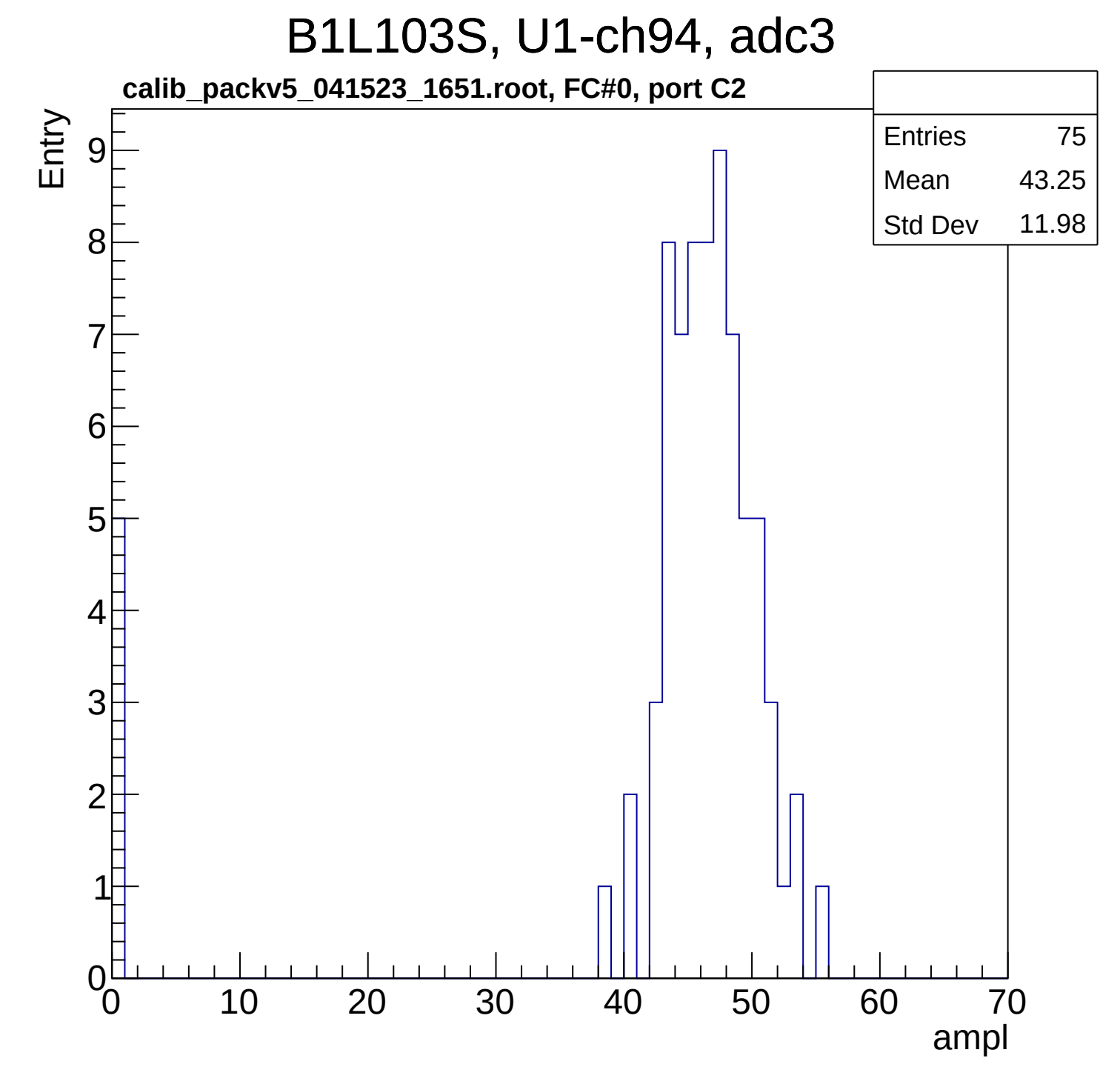
B1L103S, U1-ch94, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 43.25
Std Dev 11.98
Entry
ampl
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6
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8
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0
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60
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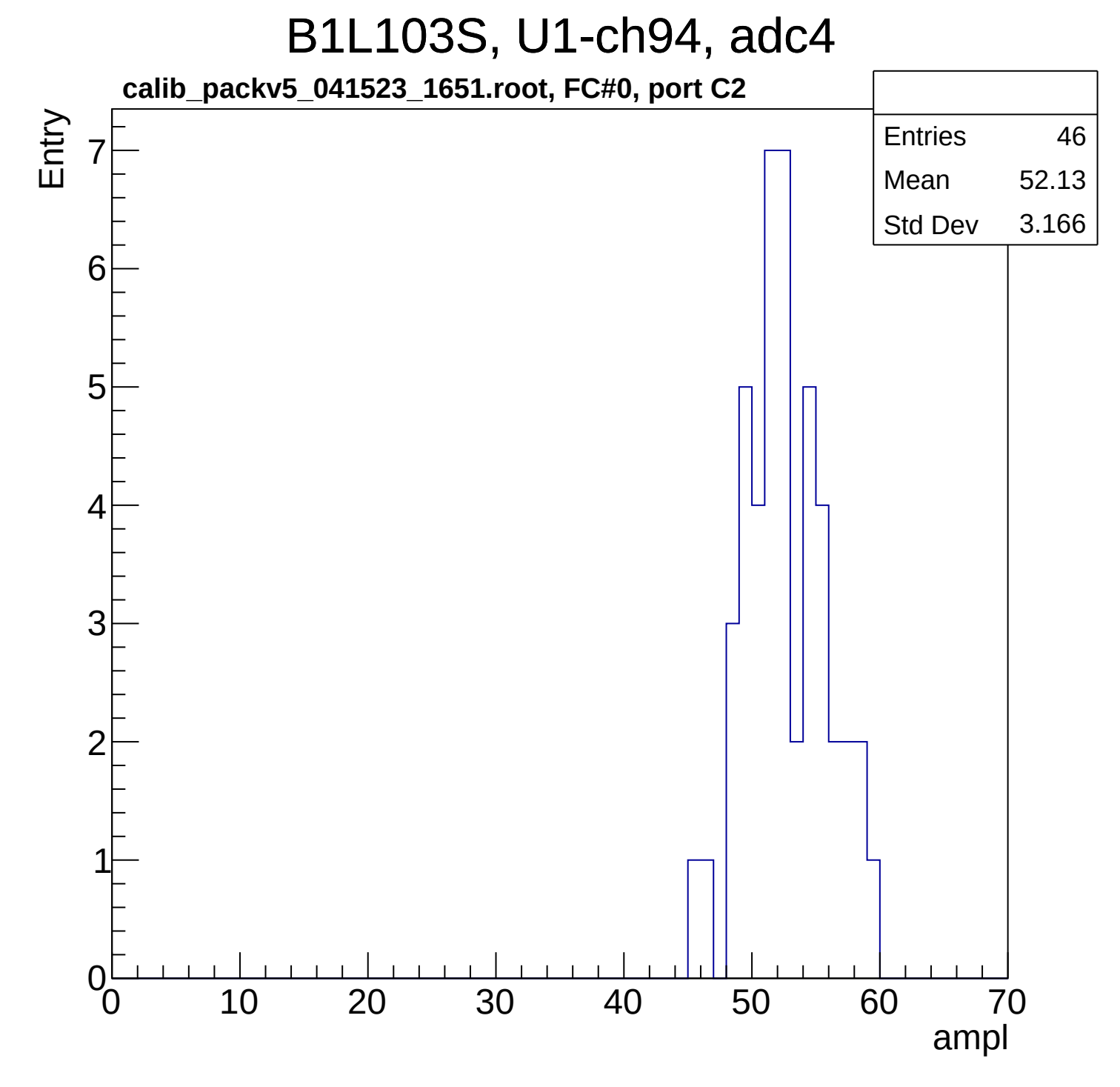
B1L103S, U1-ch94, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 52.13
Std Dev 3.166
Entry
ampl
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4
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0
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20
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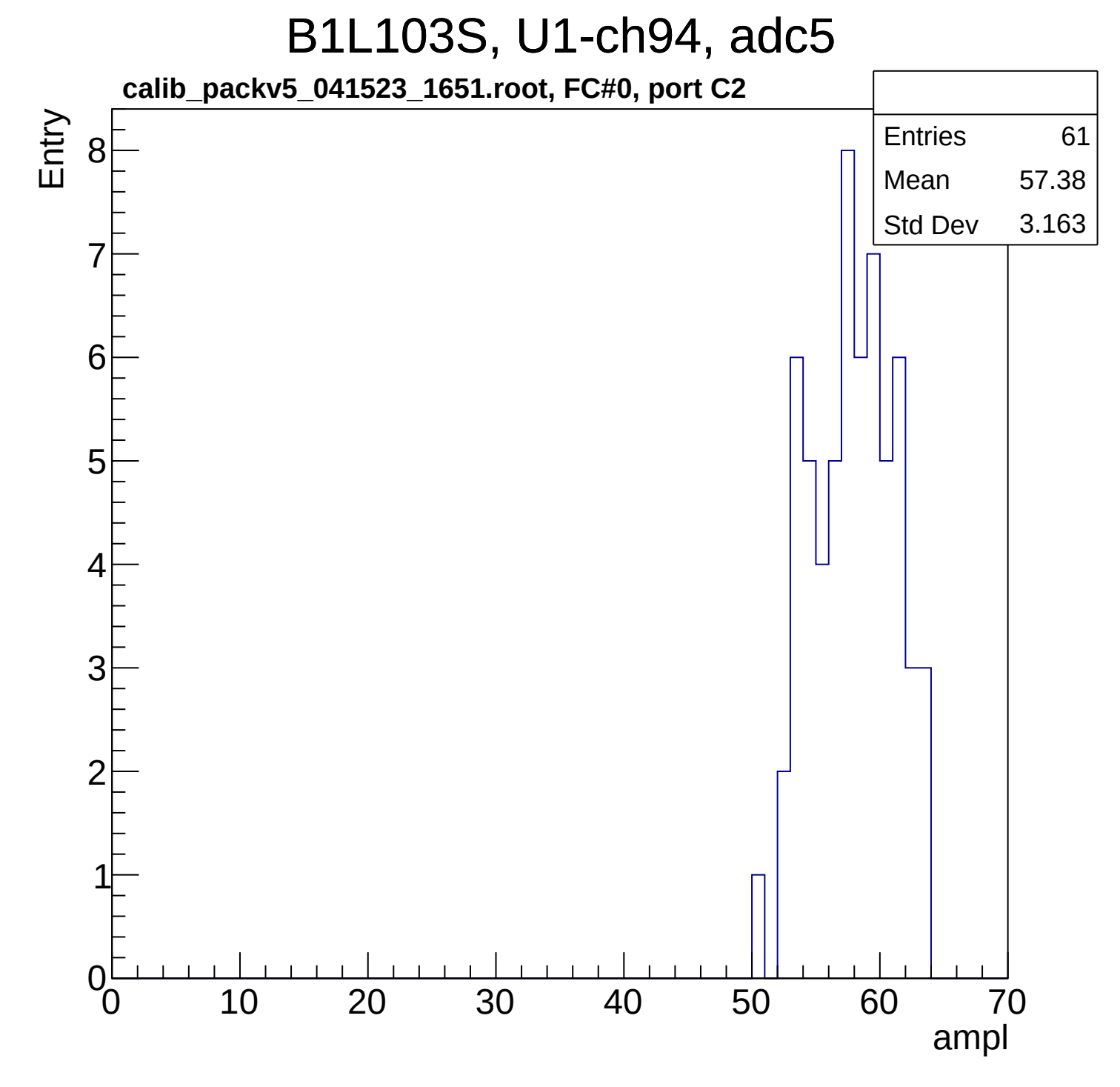
B1L103S, U1-ch94, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 57.38
Std Dev 3.163
Entry
ampl
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5
6
7
8
0
10
20
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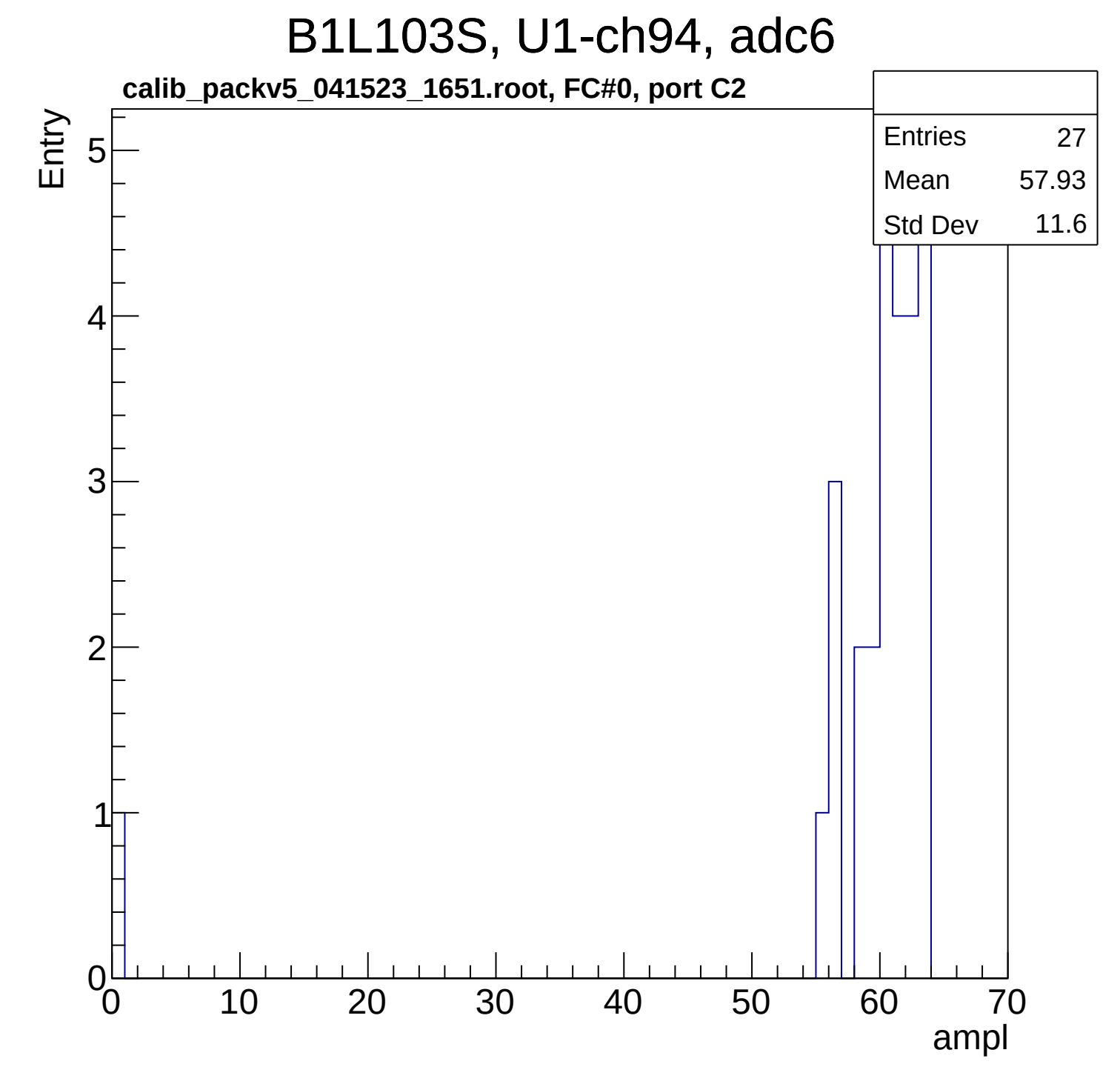
B1L103S, U1-ch94, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 27
Mean 57.93
Std Dev 11.6
Entry
ampl
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2
3
4
5
0
10
20
30
40
50
60
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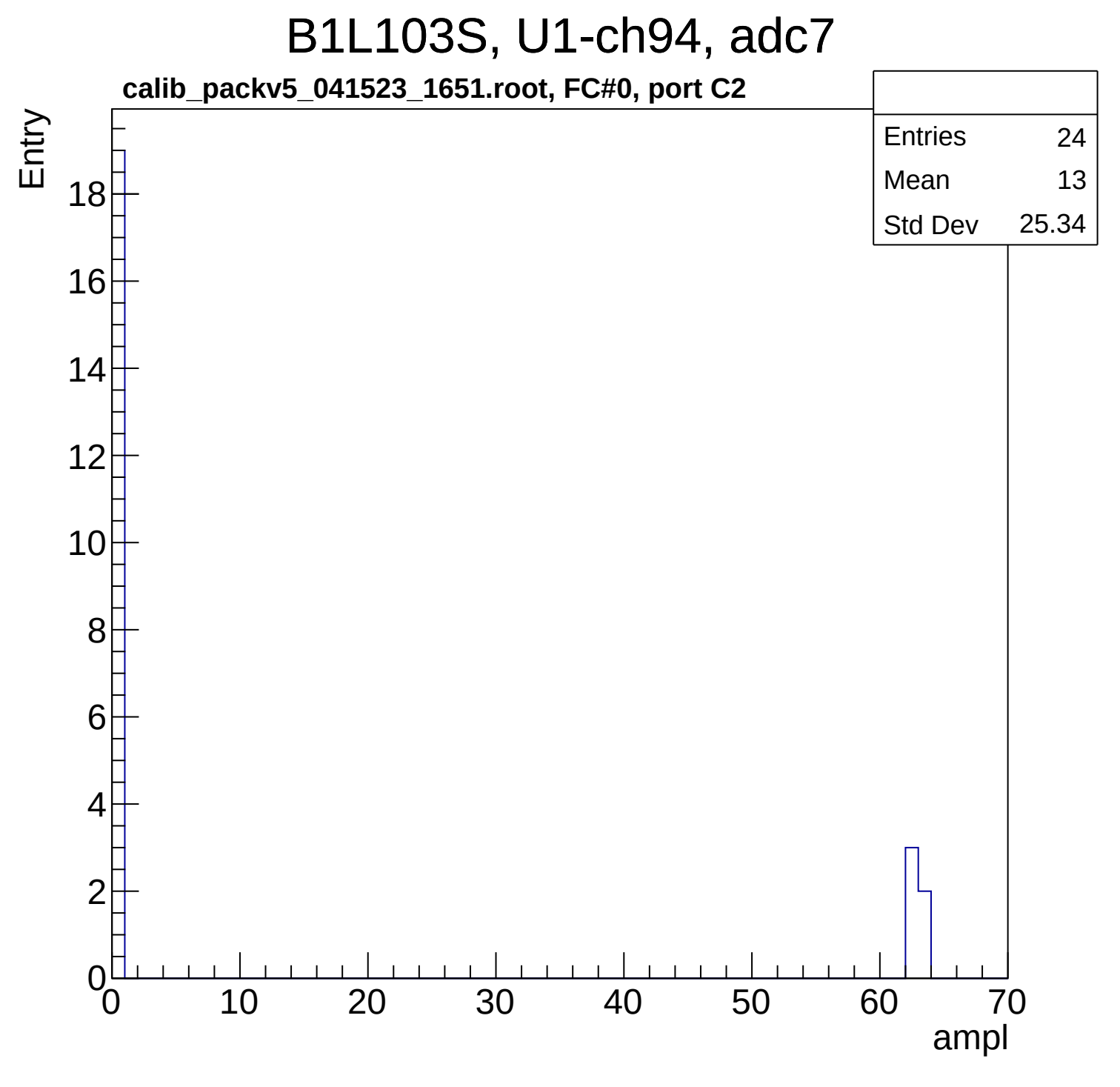
B1L103S, U1-ch94, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 24
Mean 13
Std Dev 25.34
Entry
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6
8
10
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14
16
18
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10
20
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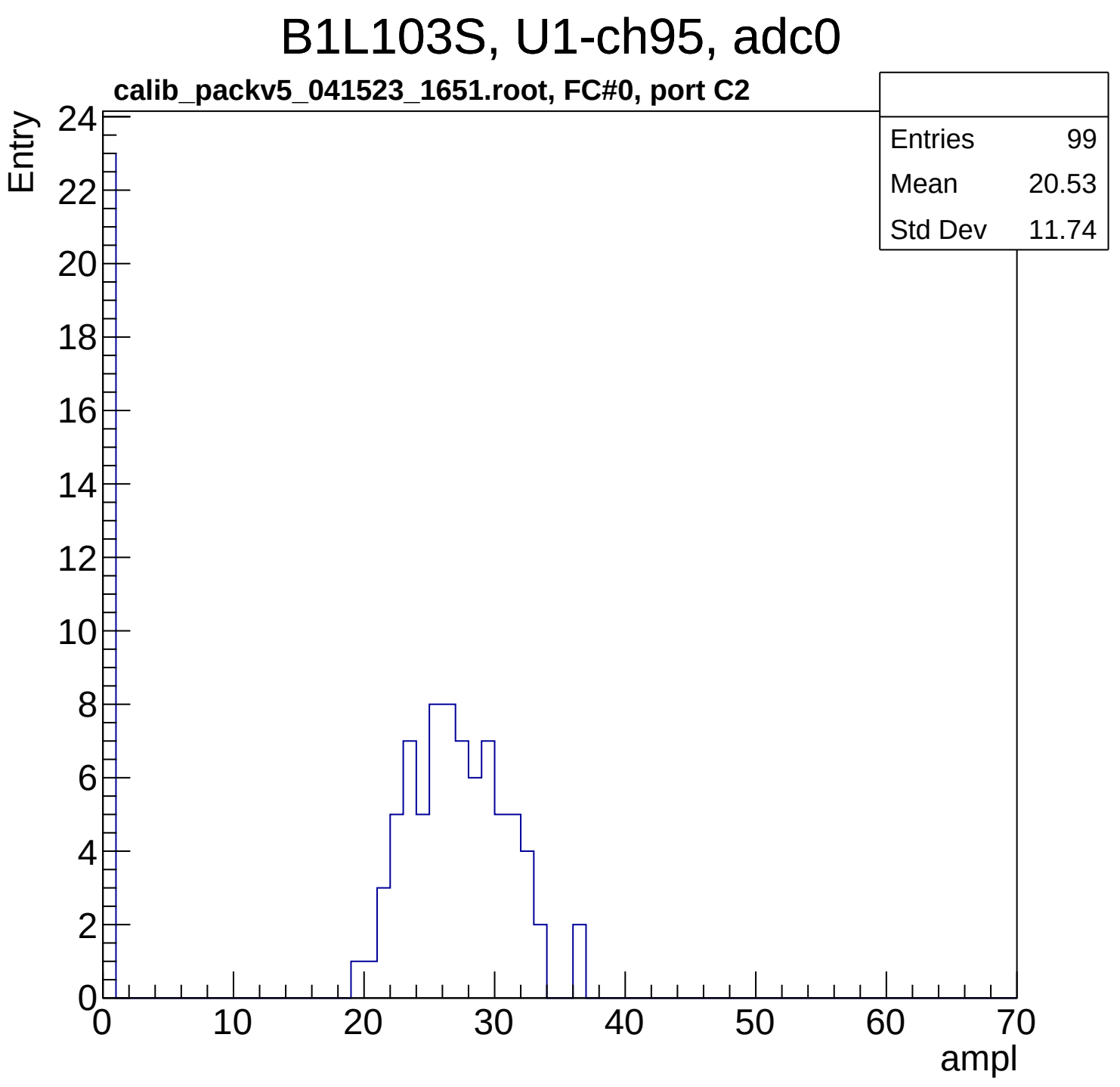
50
60
70
ampl


B1L103S, U1-ch95, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 99
Mean 20.53
Std Dev 11.74
Entry
ampl
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10
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14
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20
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60
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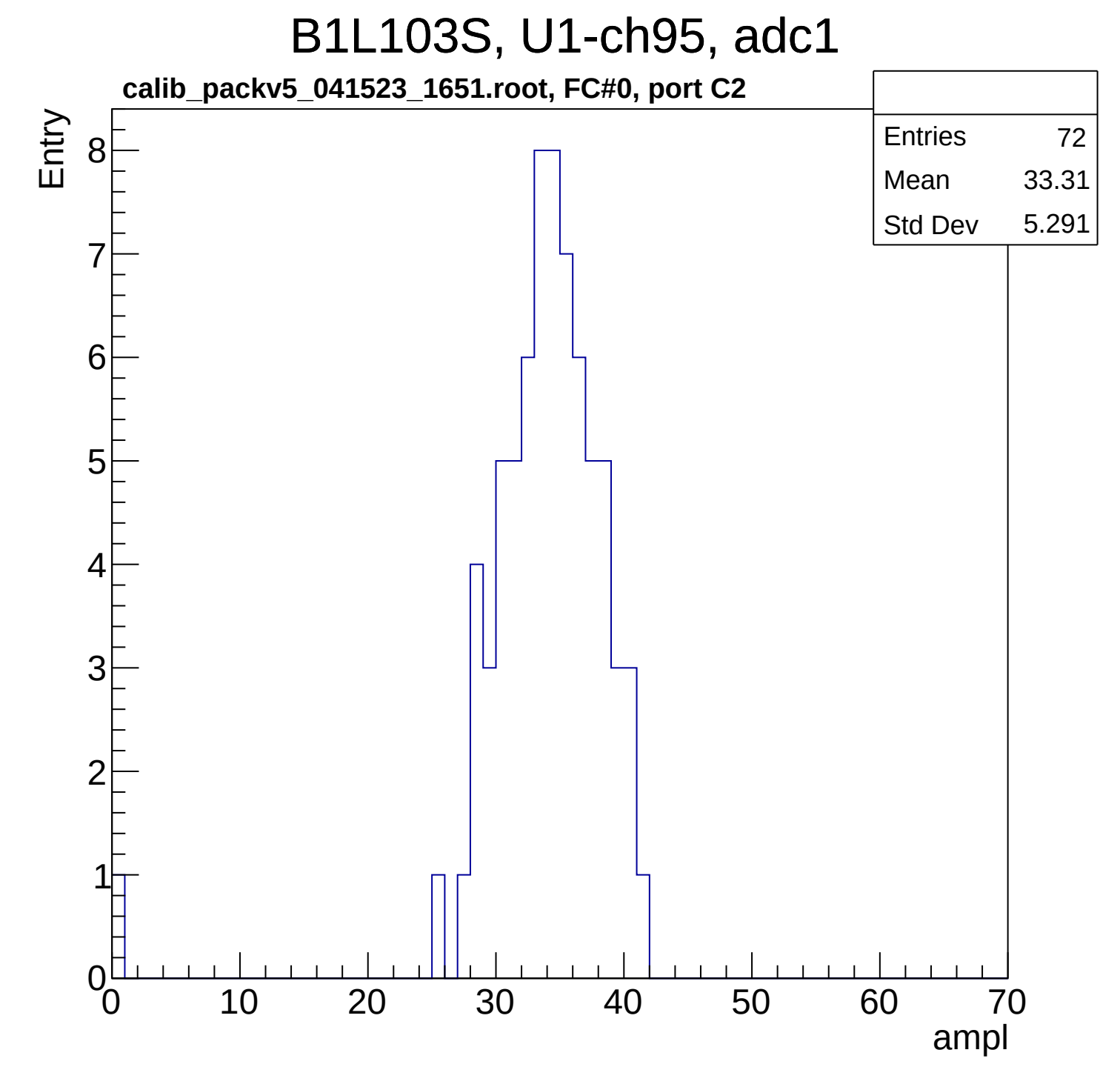
B1L103S, U1-ch95, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 33.31
Std Dev 5.291
Entry
ampl
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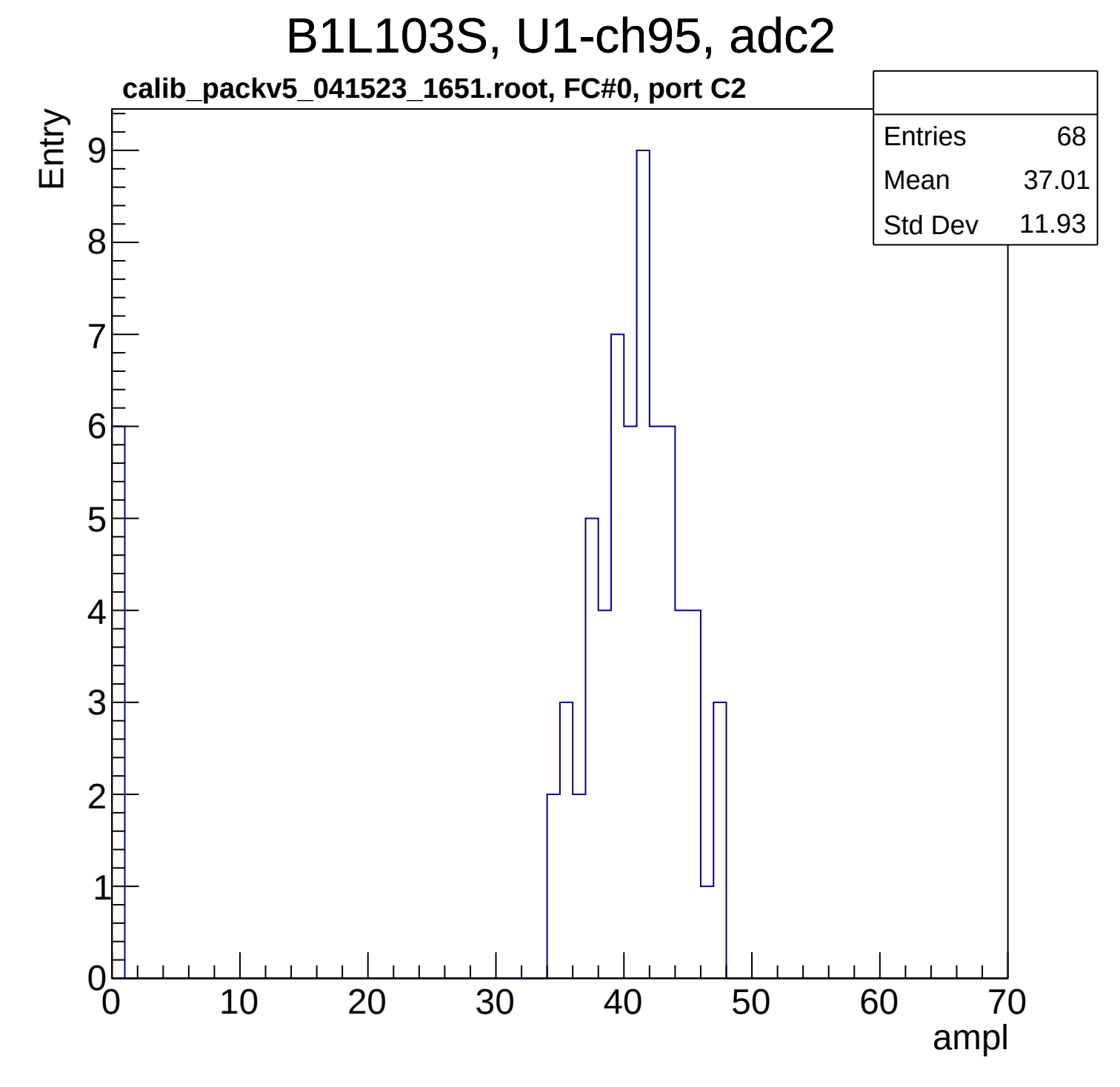
B1L103S, U1-ch95, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 37.01
Std Dev 11.93
Entry
ampl
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4
5
6
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0
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60
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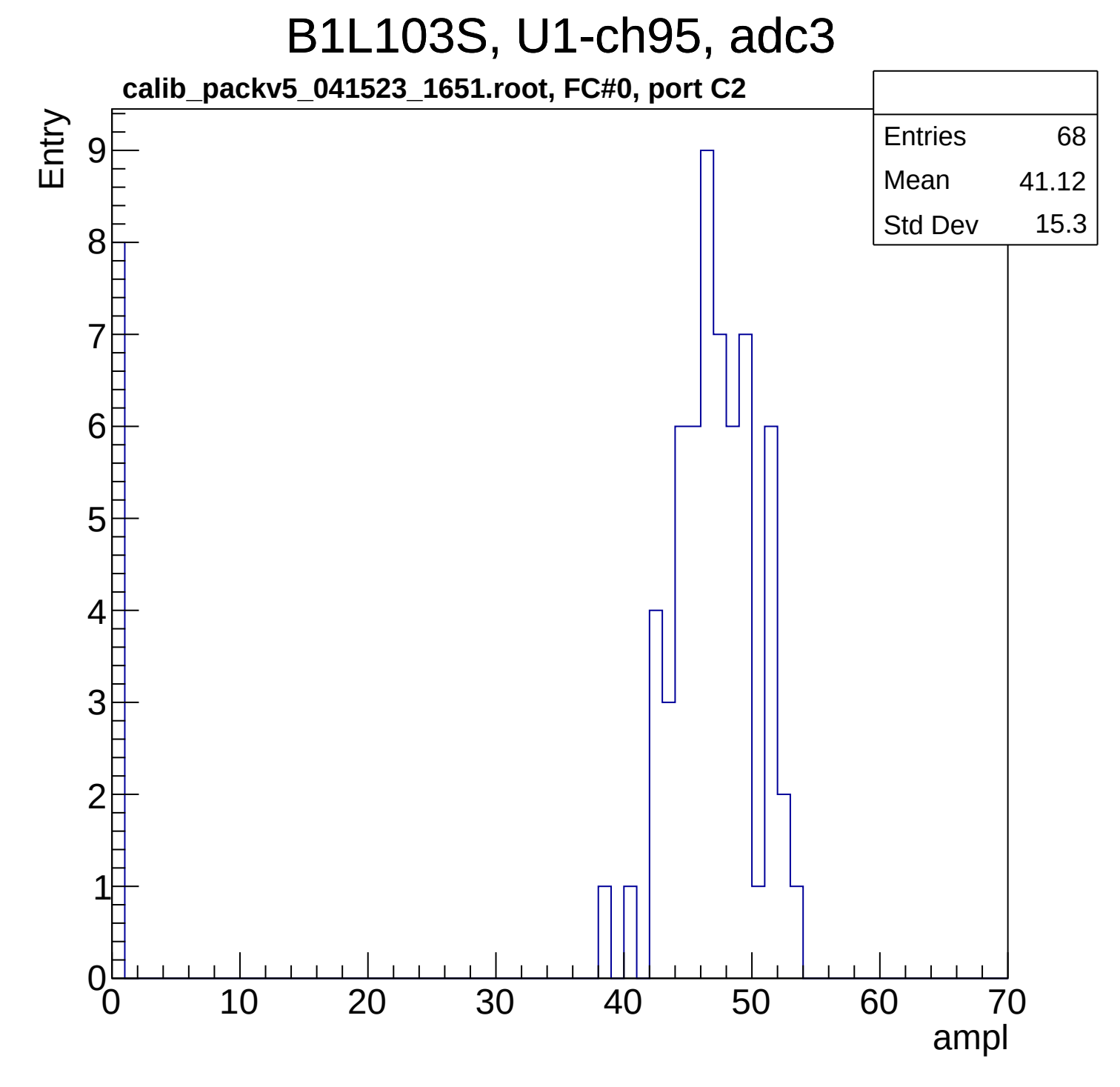
B1L103S, U1-ch95, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 41.12
Std Dev 15.3
Entry
ampl
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5
6
7
8
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0
10
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60
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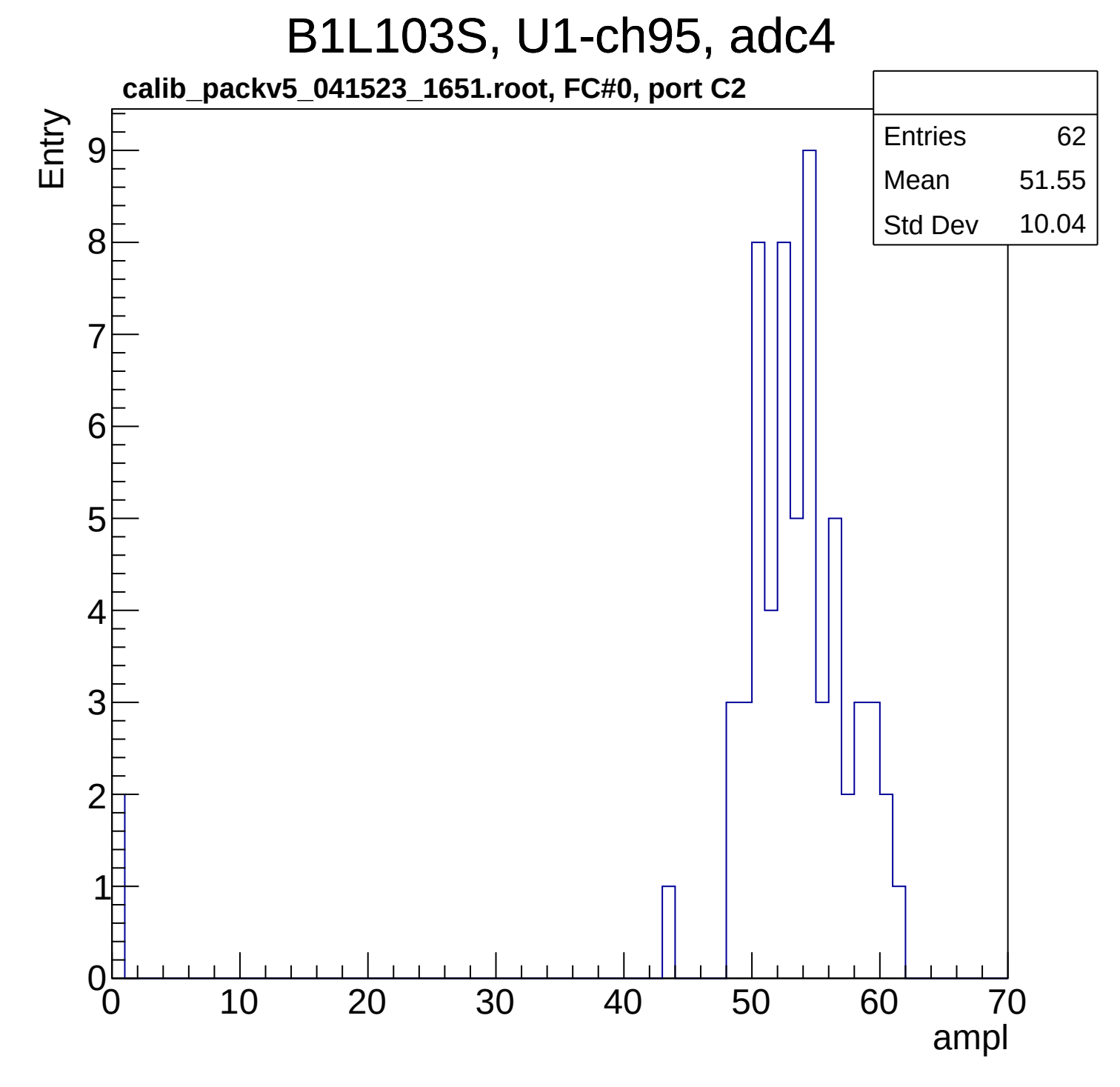
B1L103S, U1-ch95, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 51.55
Std Dev 10.04
Entry
ampl
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0
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60
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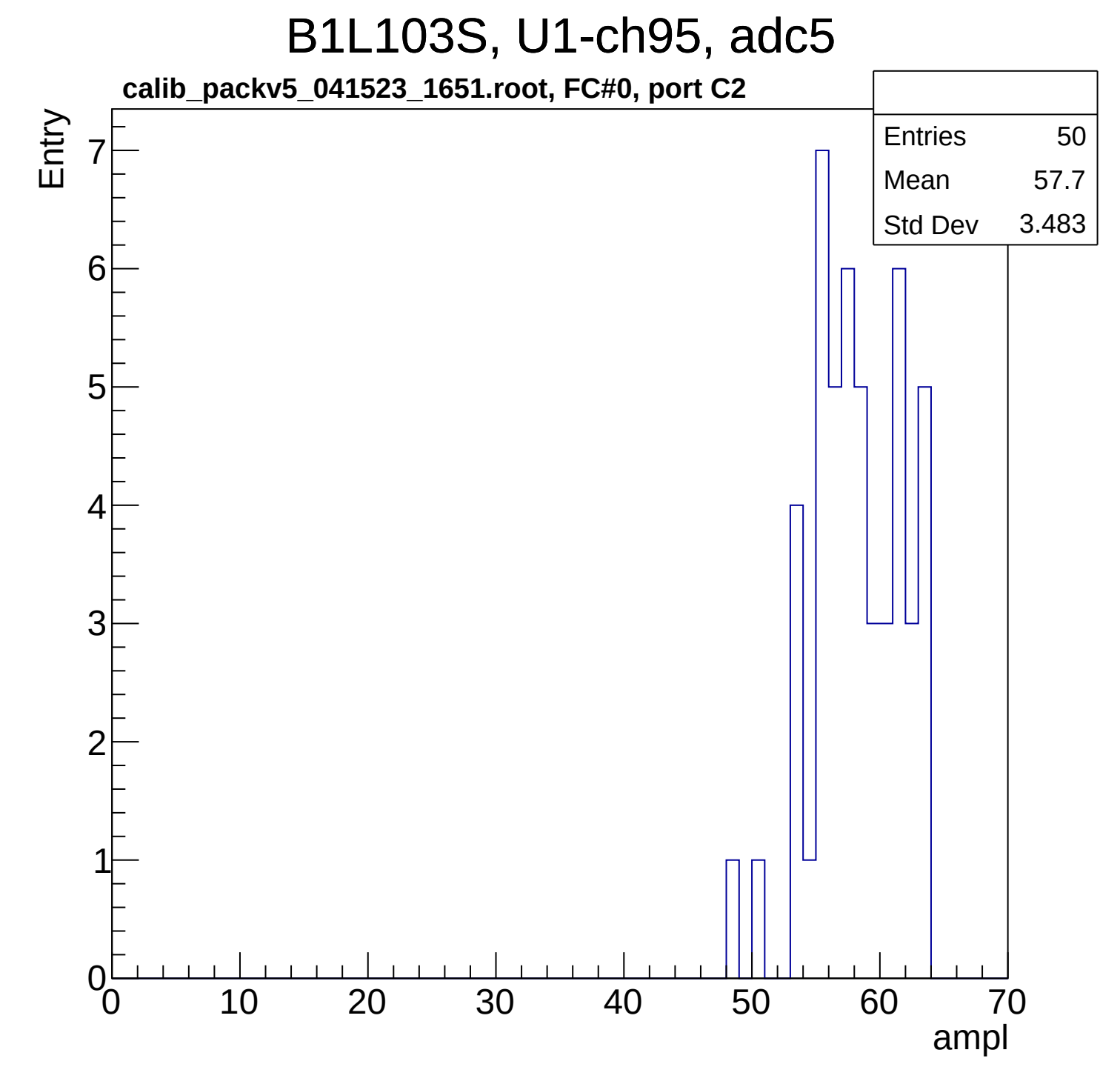
B1L103S, U1-ch95, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 57.7
Std Dev 3.483
Entry
ampl
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60
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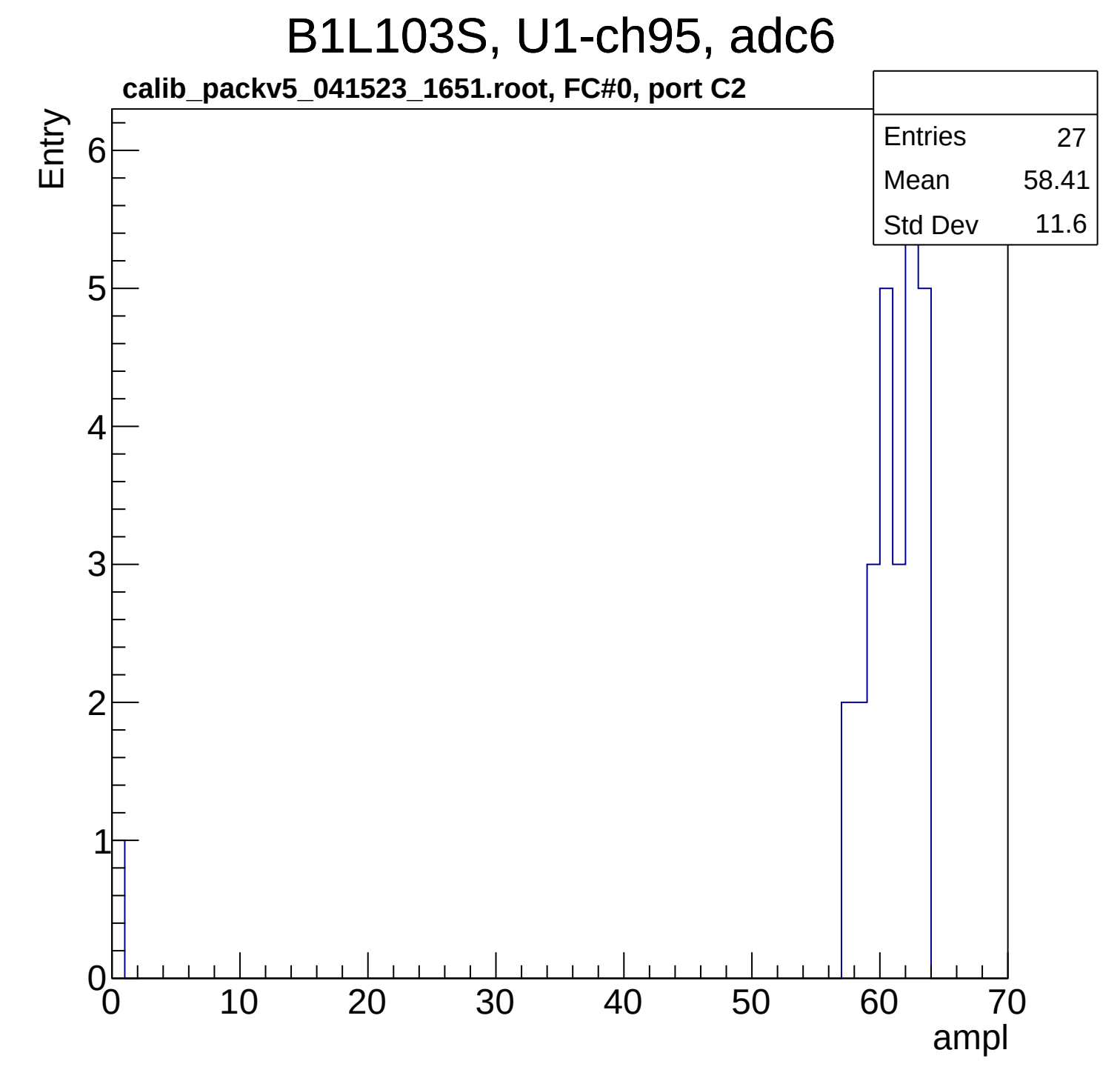
B1L103S, U1-ch95, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 27
Mean 58.41
Std Dev 11.6
Entry
ampl
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0
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40
50
60
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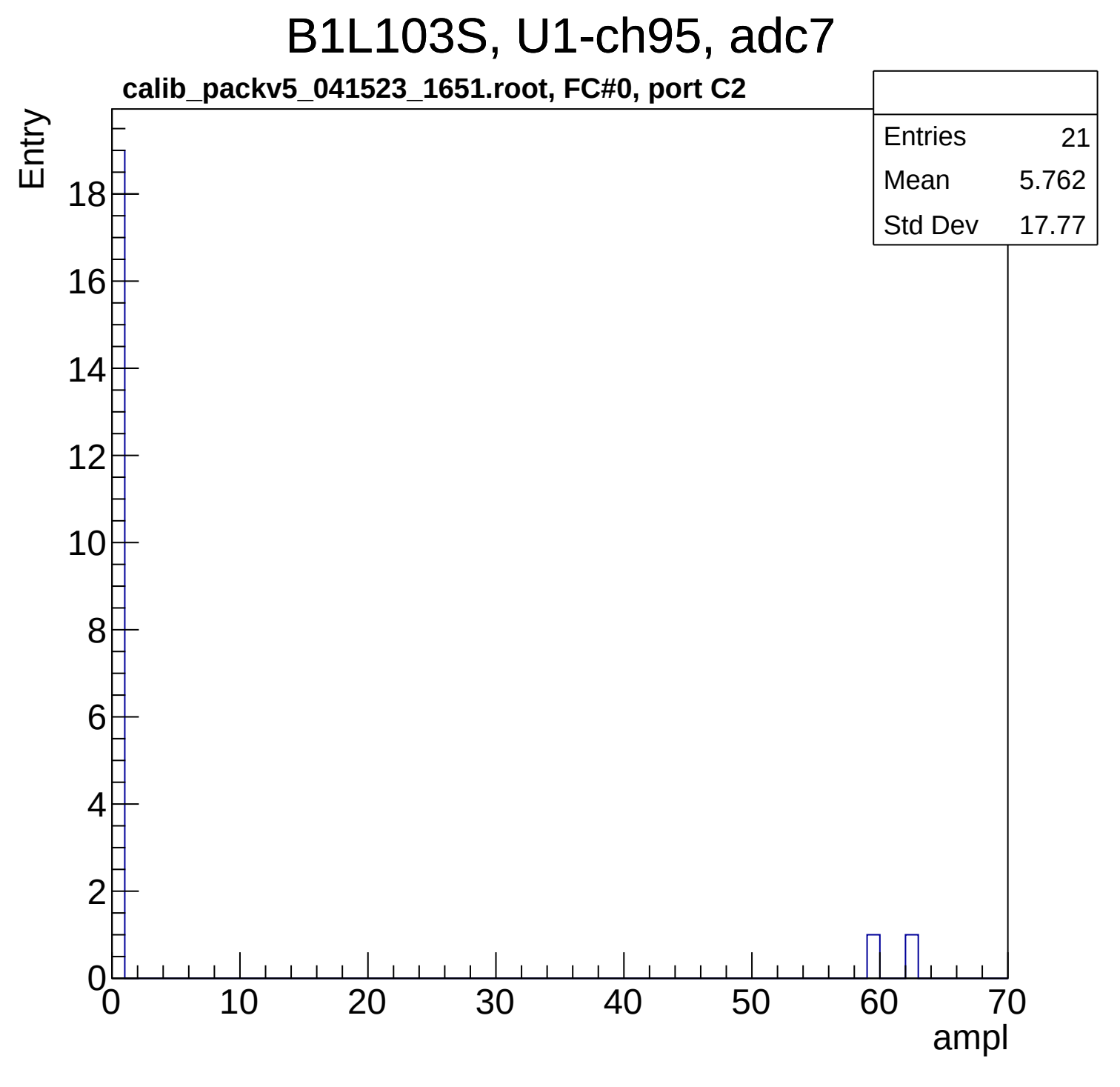
B1L103S, U1-ch95, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 5.762
Std Dev 17.77
Entry
0
2
4
6
8
10
12
14
16
18
0
10
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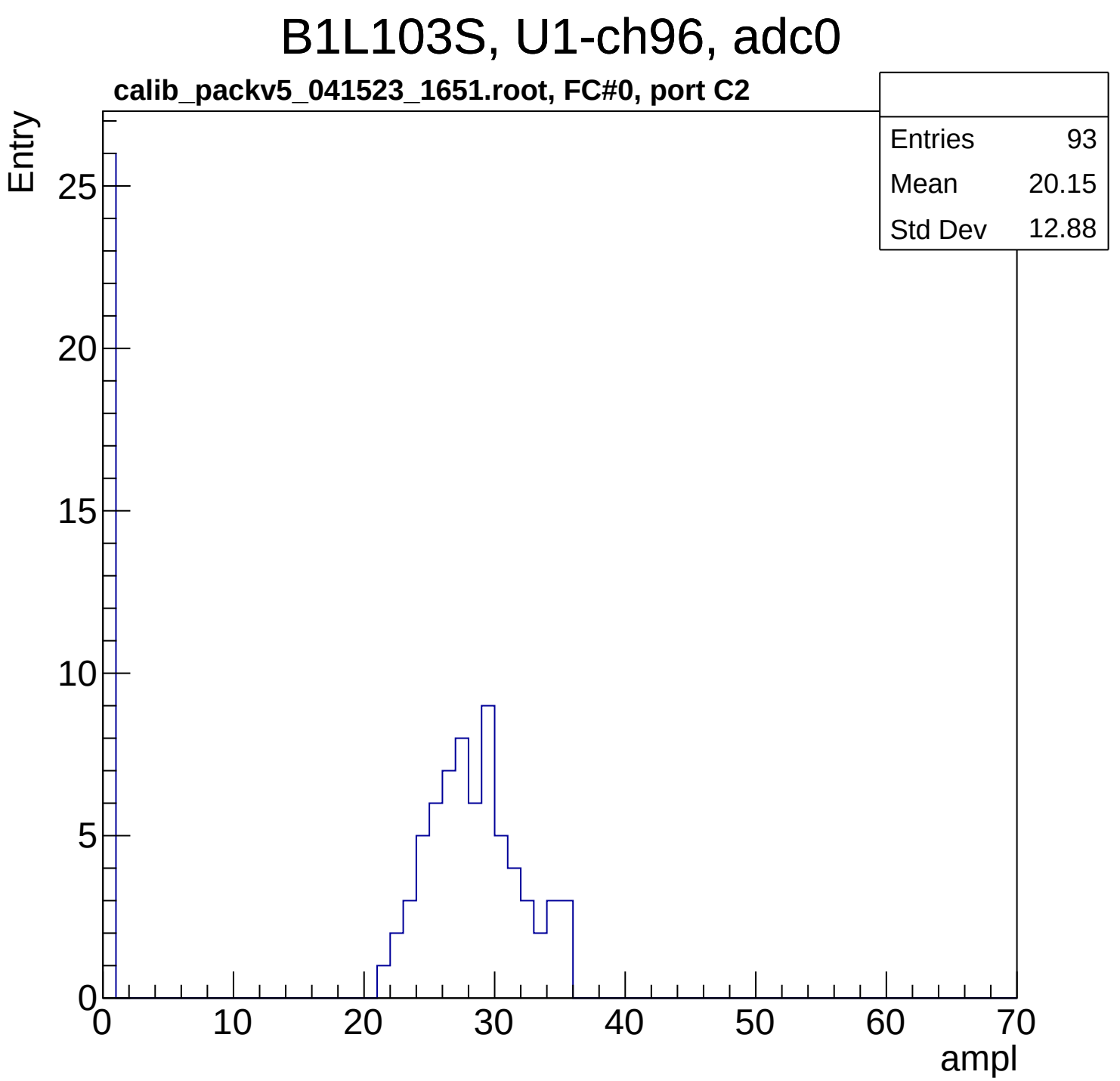
50
60
70
ampl


B1L103S, U1-ch96, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 93
Mean 20.15
Std Dev 12.88
Entry
0
5
10
15
20
25
0
10
20
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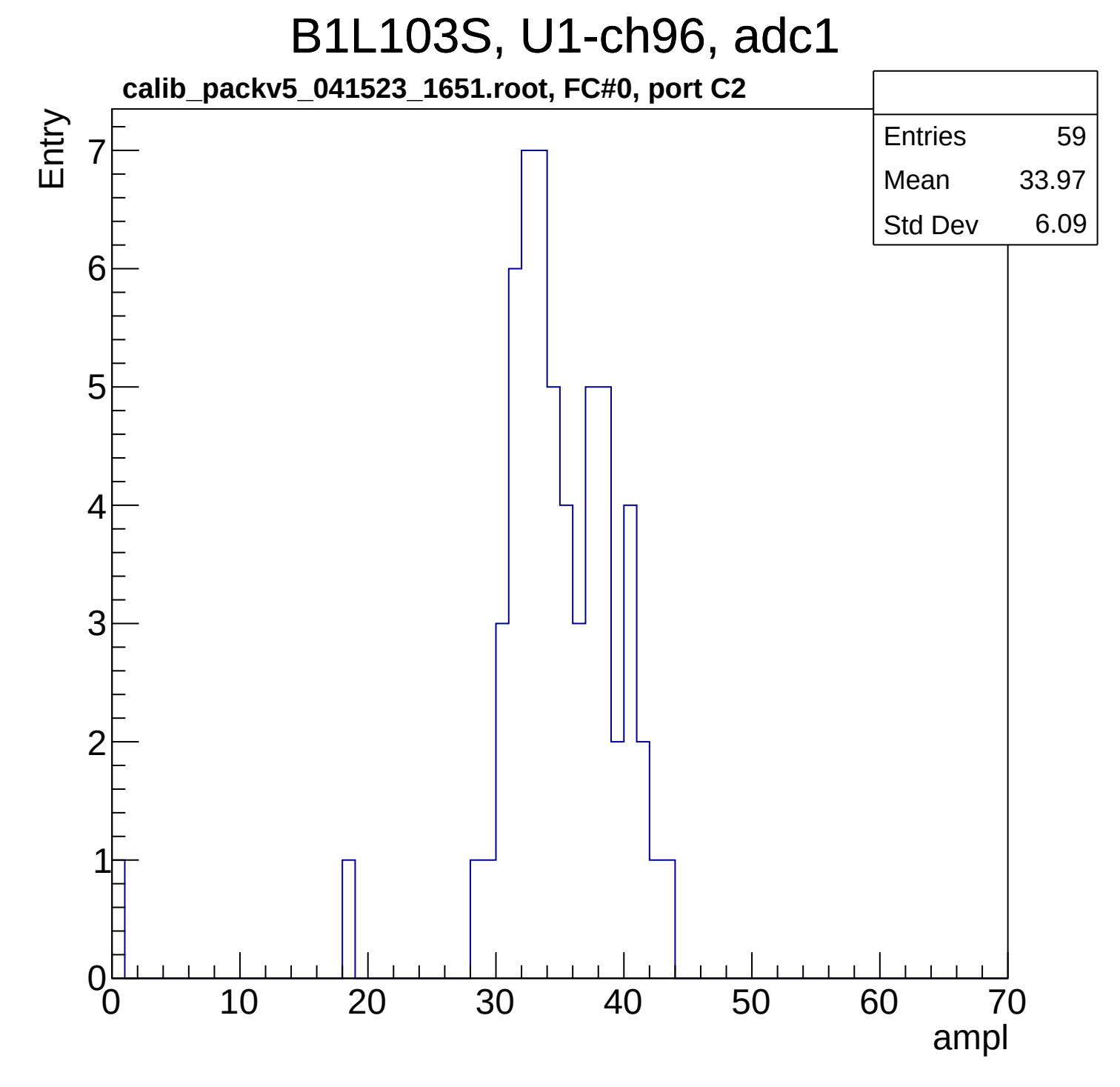
50
60
70
ampl


B1L103S, U1-ch96, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 33.97
Std Dev 6.09
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
30
40
50
60
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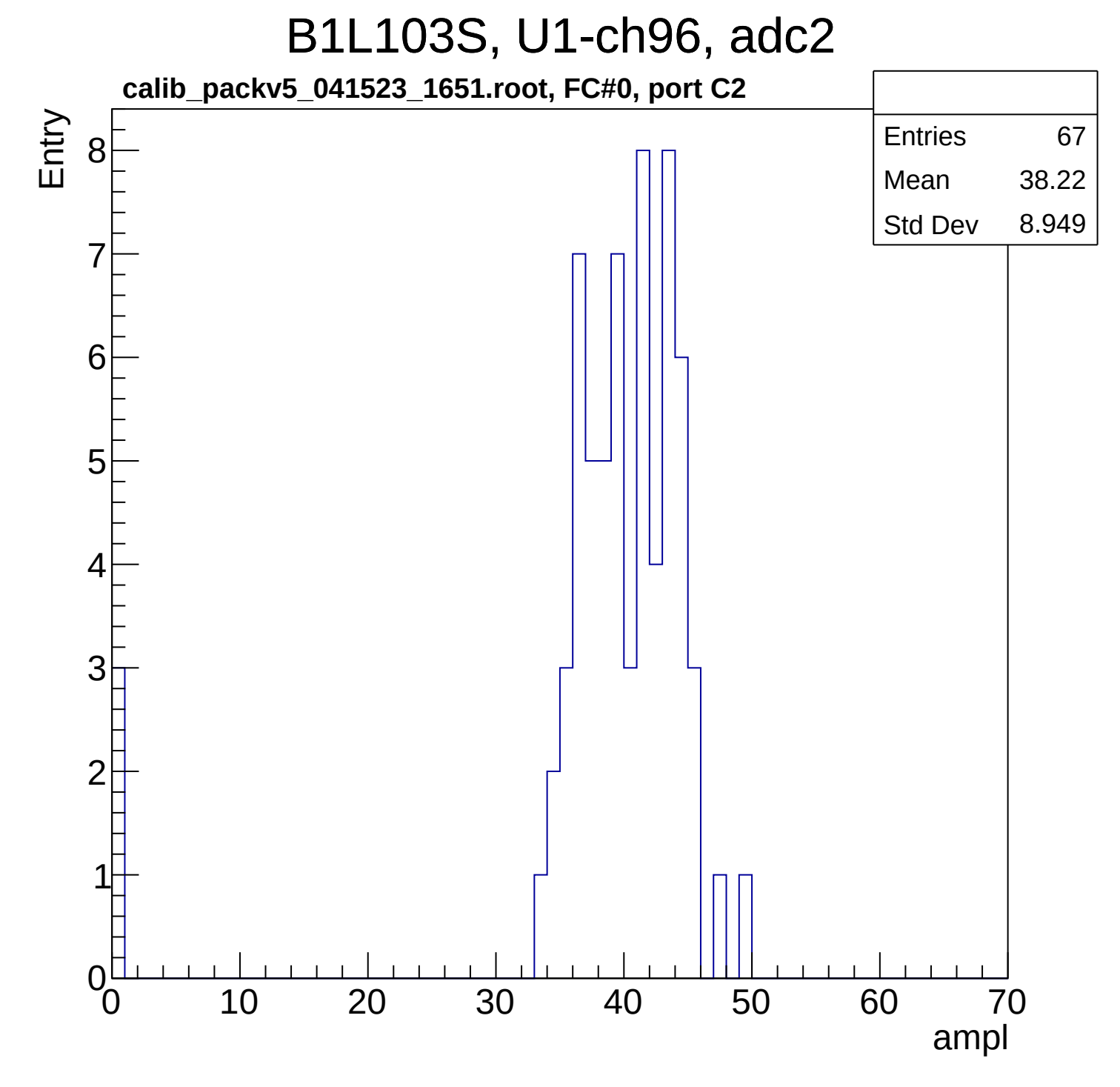
B1L103S, U1-ch96, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 38.22
Std Dev 8.949
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
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60
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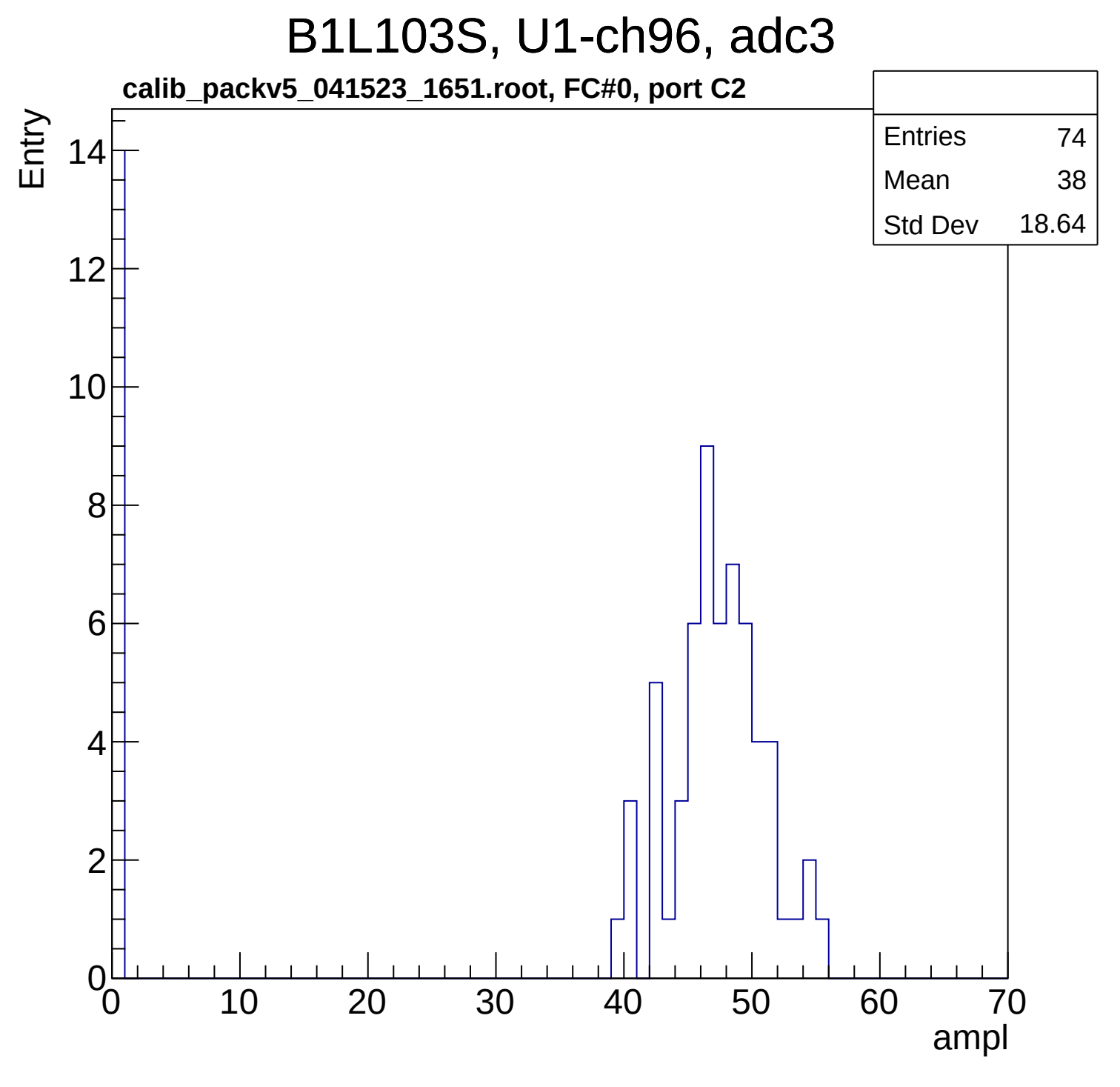
B1L103S, U1-ch96, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 38
Std Dev 18.64
Entry
ampl
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2
4
6
8
10
12
14
0
10
20
30
40
50
60
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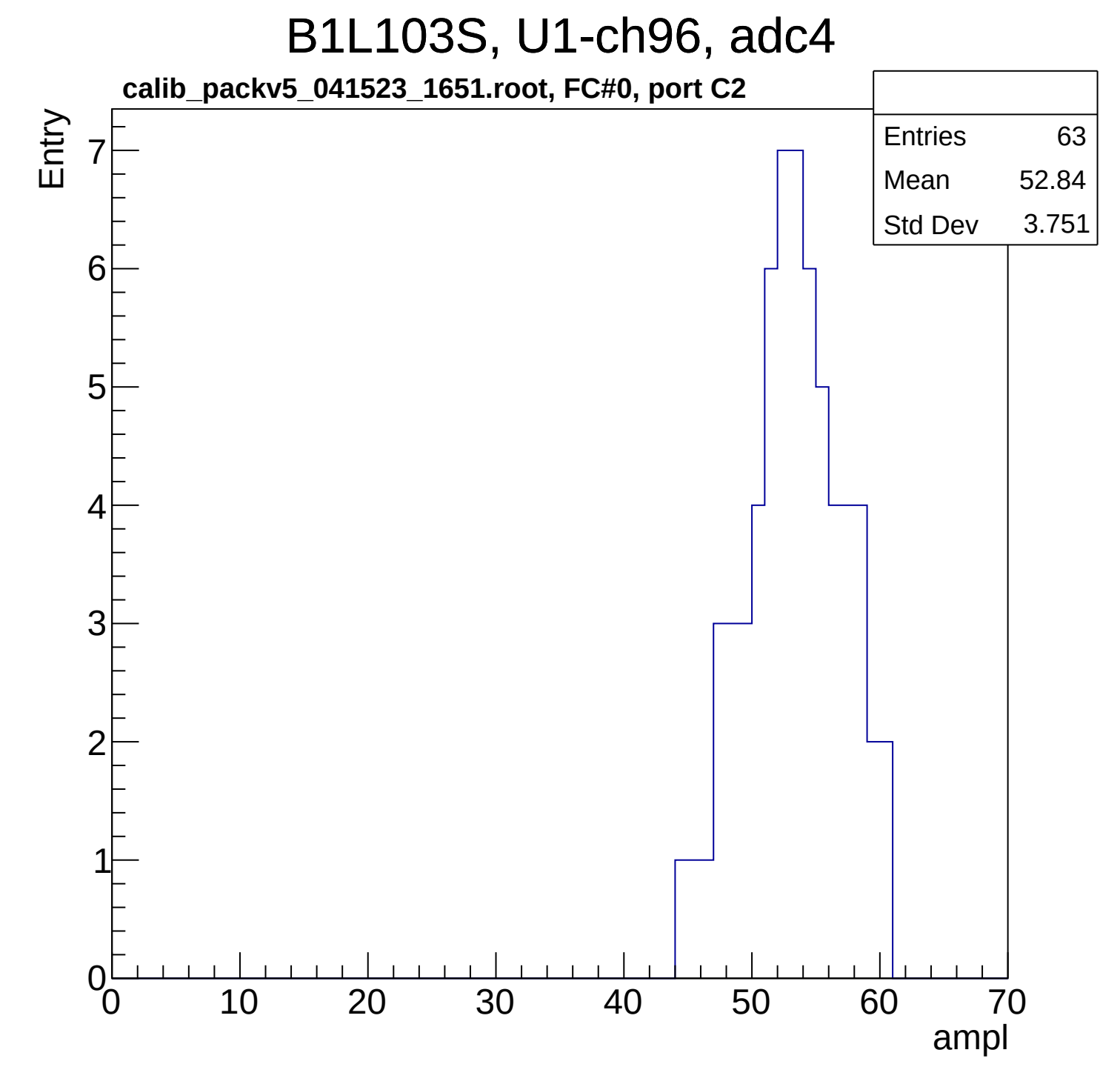
B1L103S, U1-ch96, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 52.84
Std Dev 3.751
Entry
ampl
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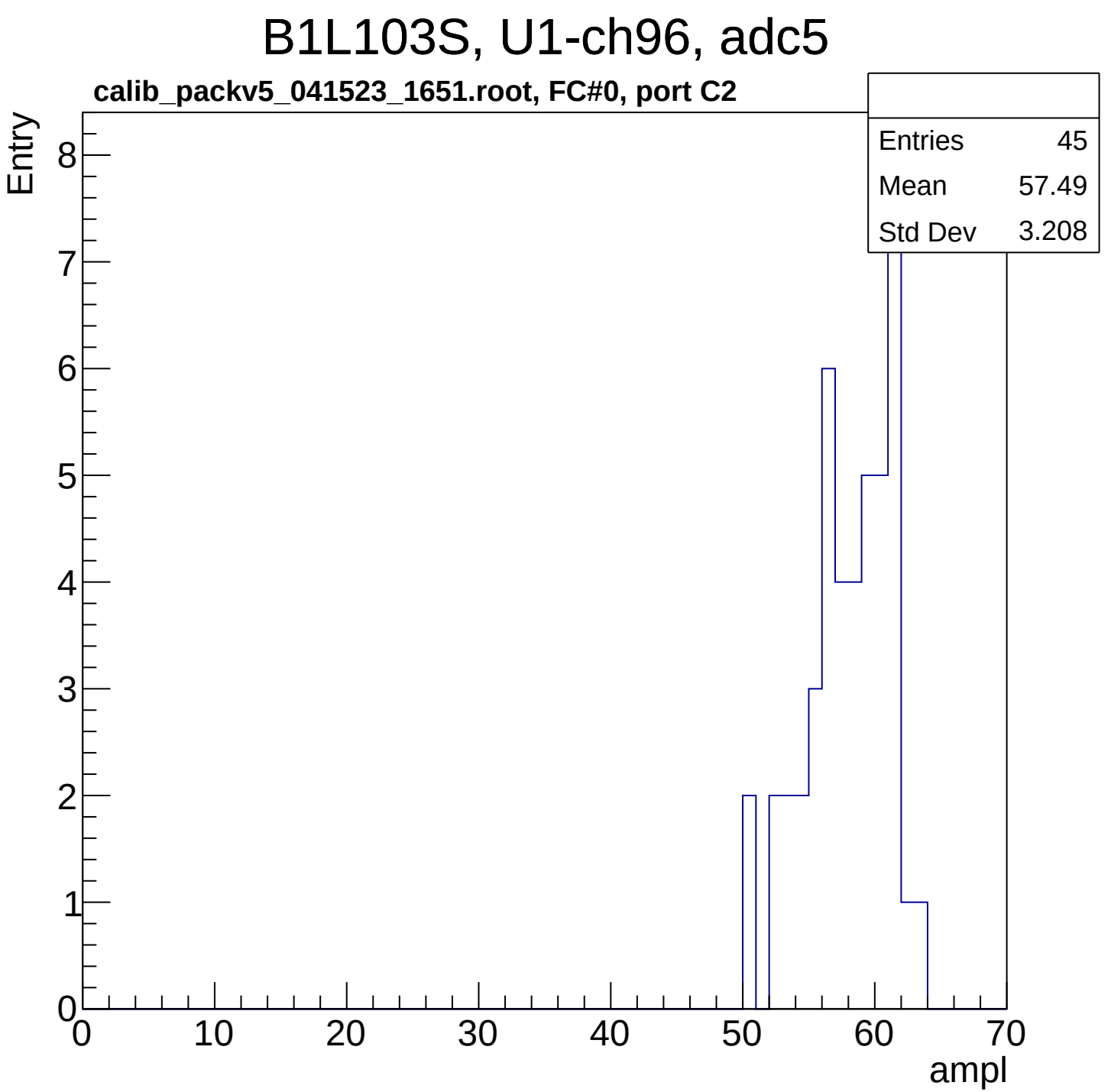
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U1-ch96, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 57.49
Std Dev 3.208
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
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60
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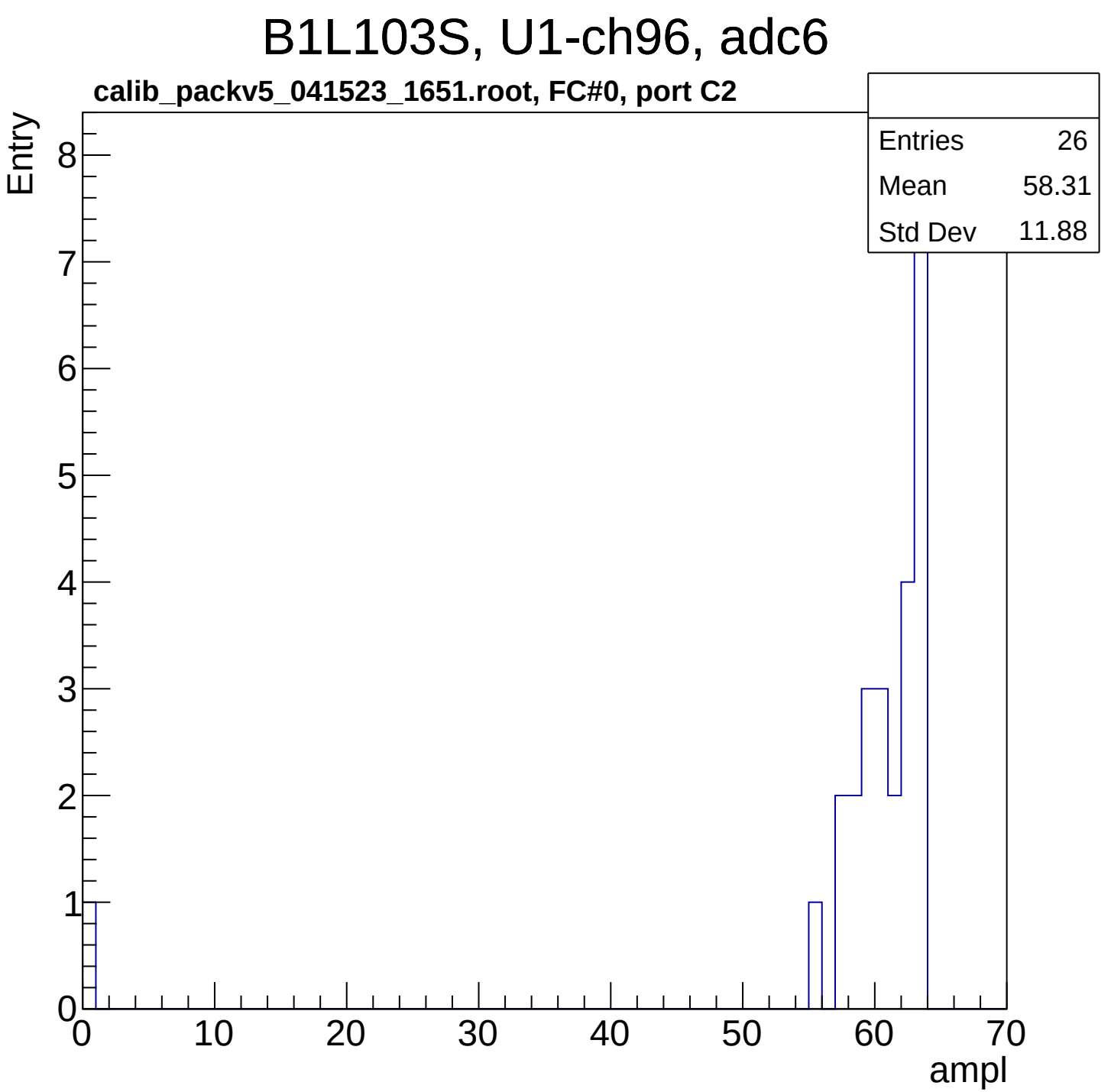
B1L103S, U1-ch96, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 26
Mean 58.31
Std Dev 11.88
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
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60
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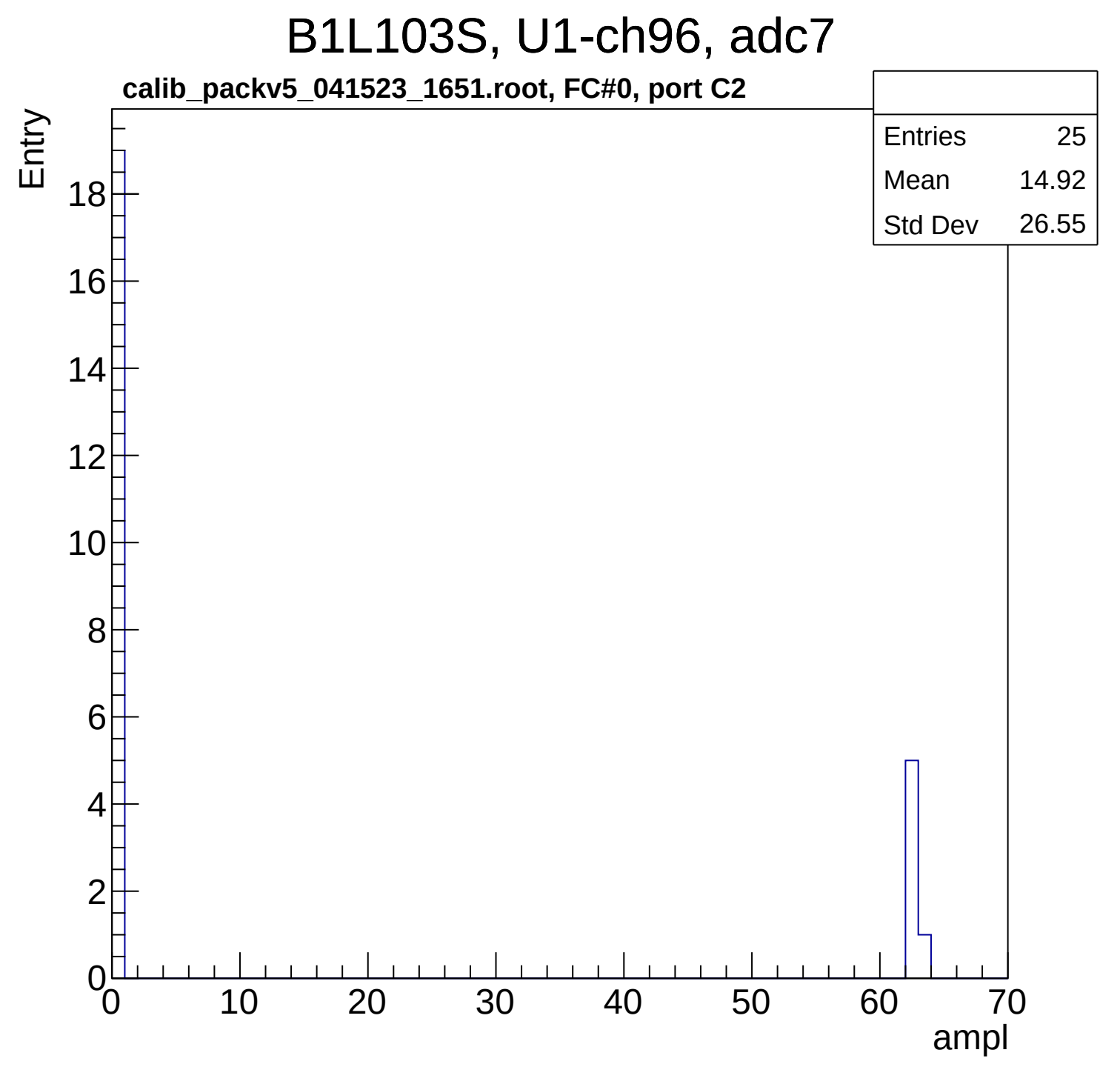
B1L103S, U1-ch96, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 25
Mean 14.92
Std Dev 26.55
Entry
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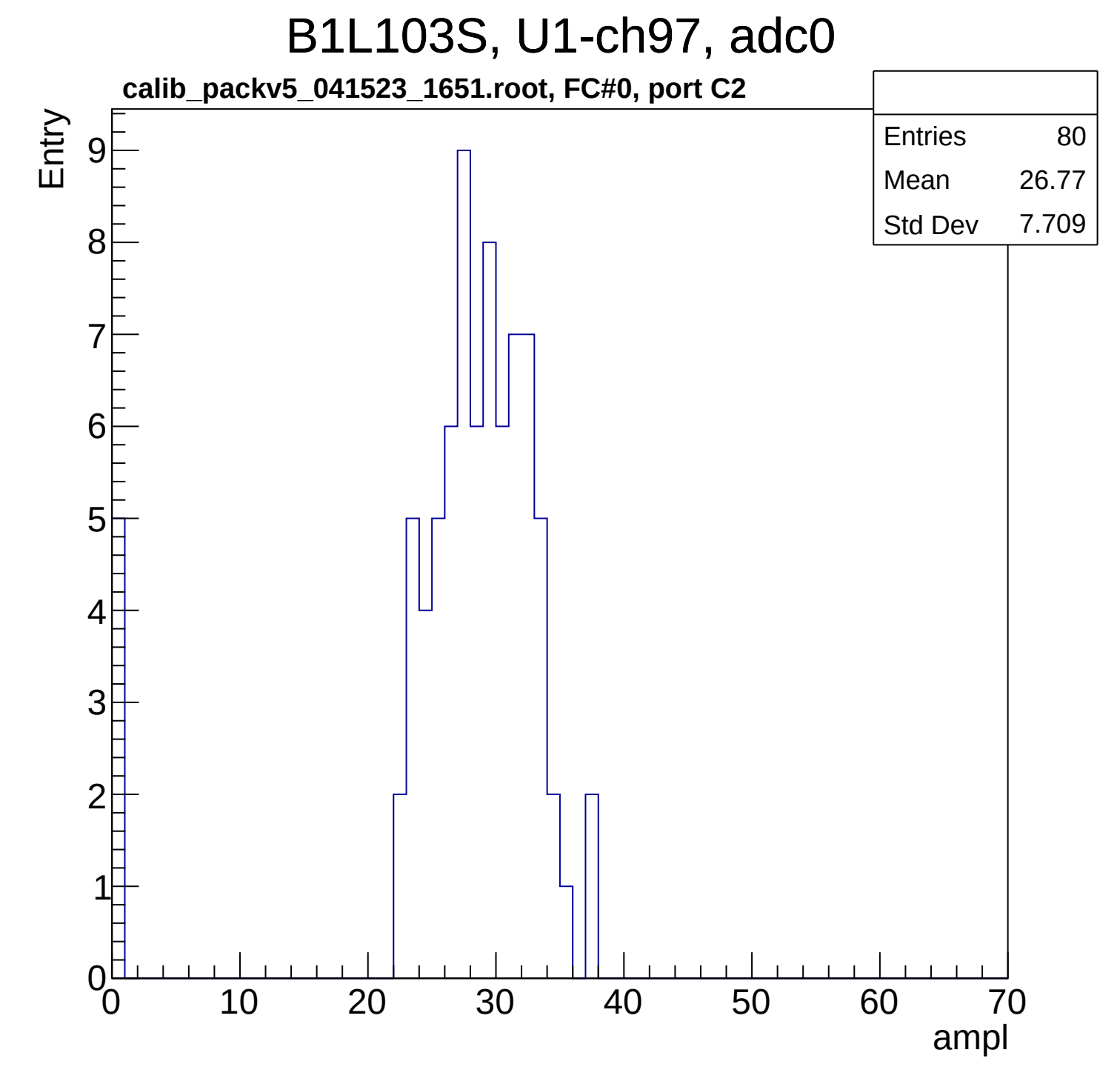
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch97, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 26.77
Std Dev 7.709
Entry
ampl
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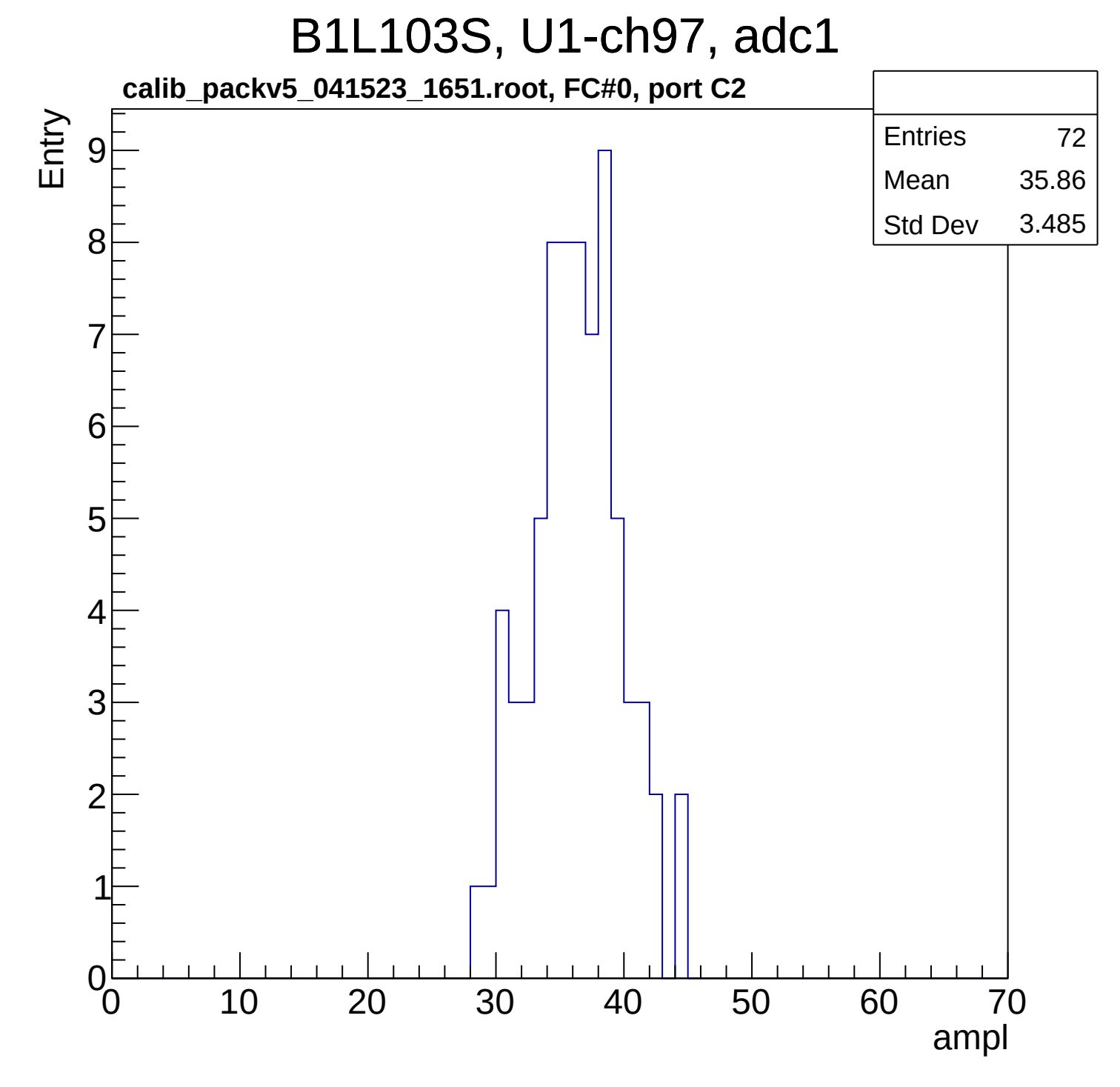
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U1-ch97, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 35.86
Std Dev 3.485
Entry
ampl
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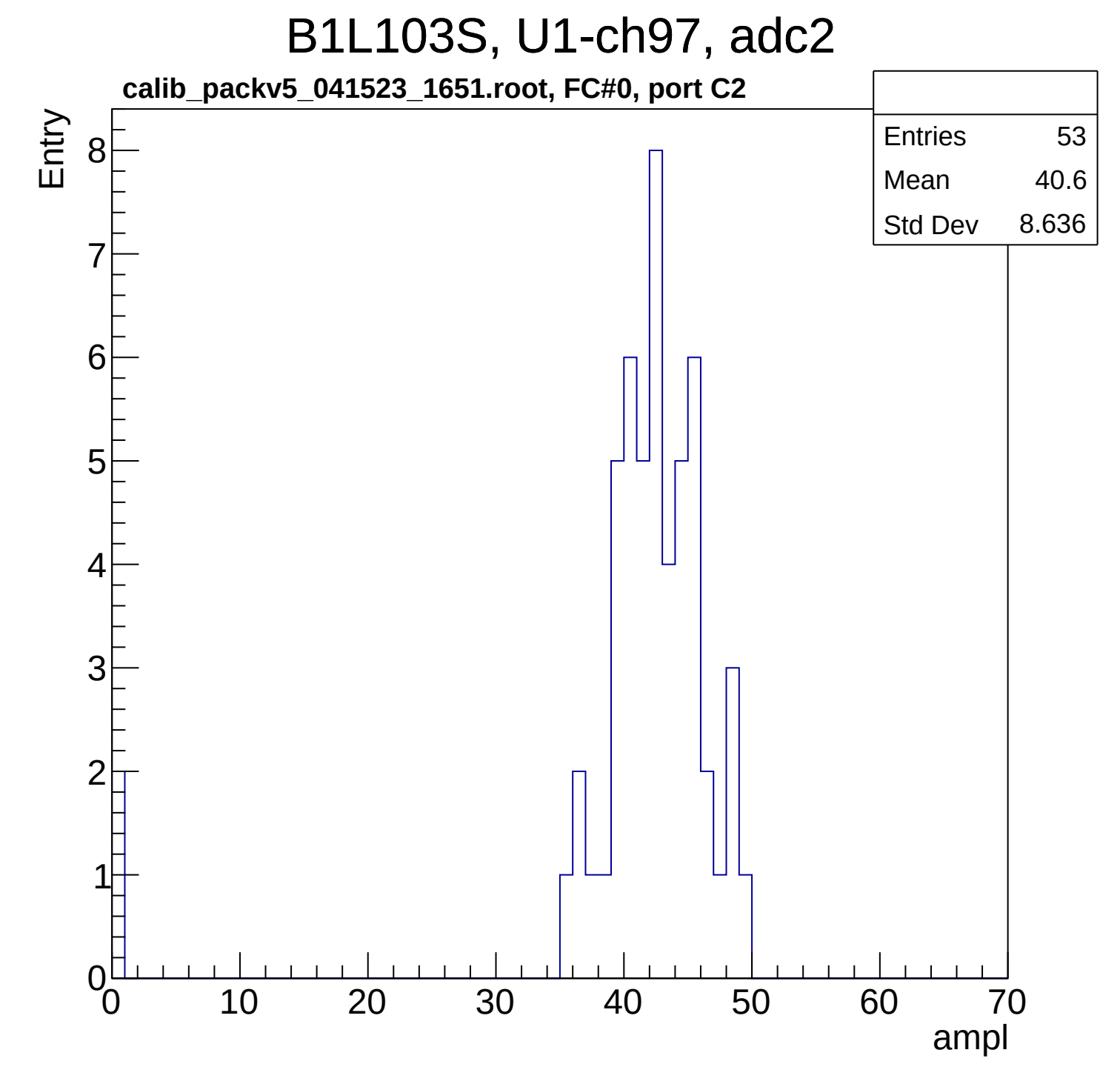
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U1-ch97, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 40.6
Std Dev 8.636
Entry
ampl
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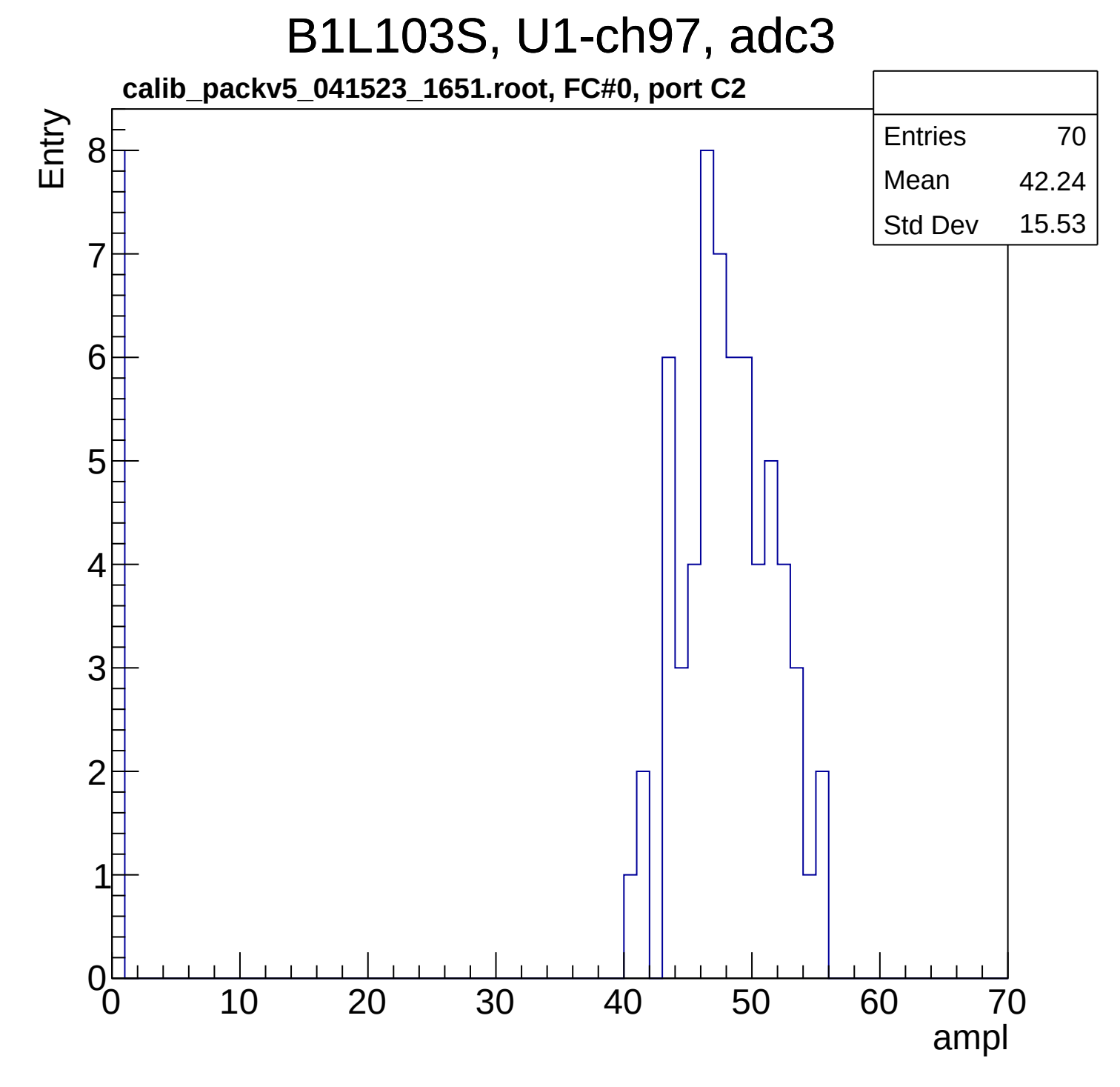
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U1-ch97, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 42.24
Std Dev 15.53
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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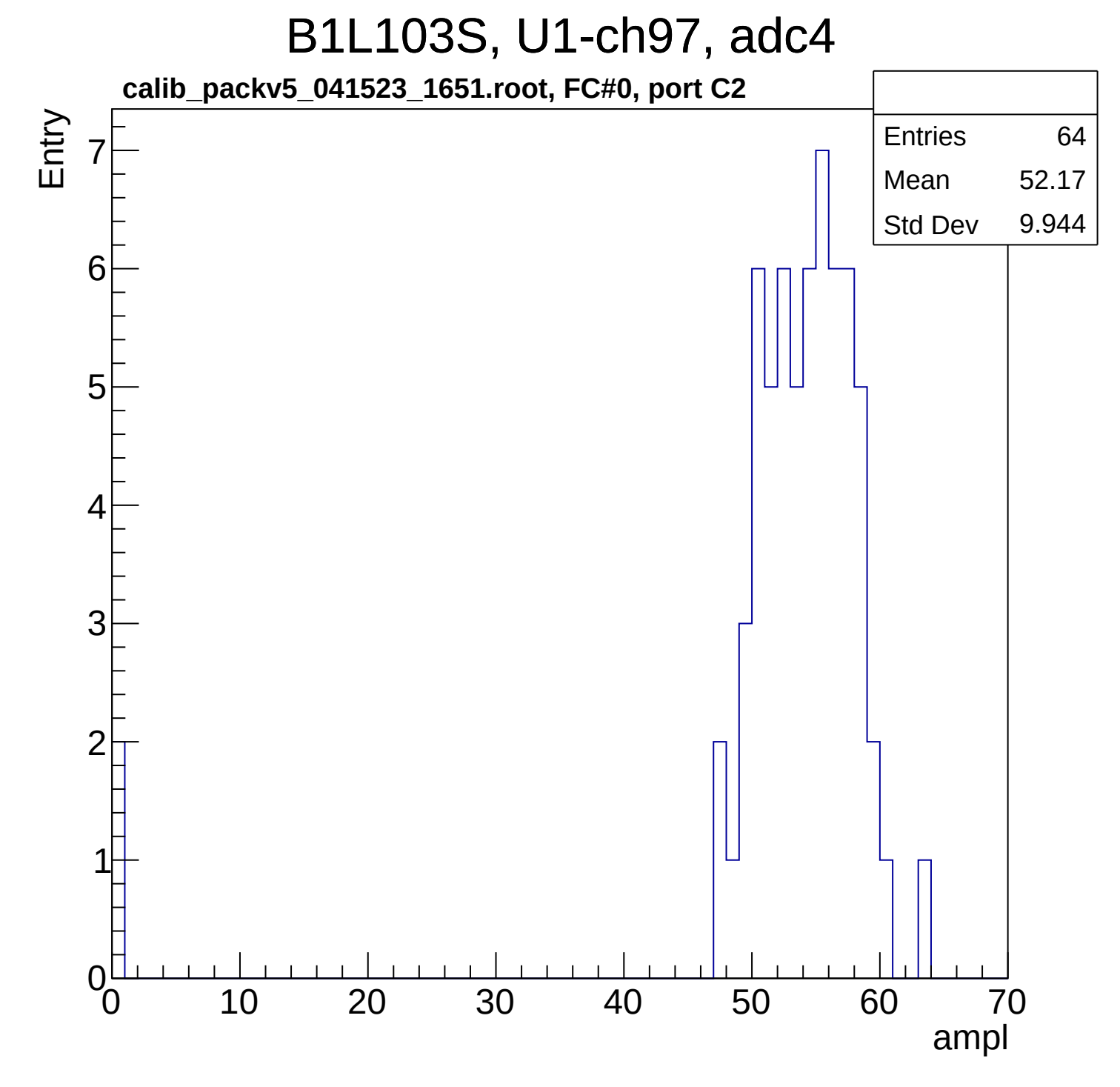
B1L103S, U1-ch97, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 52.17
Std Dev 9.944
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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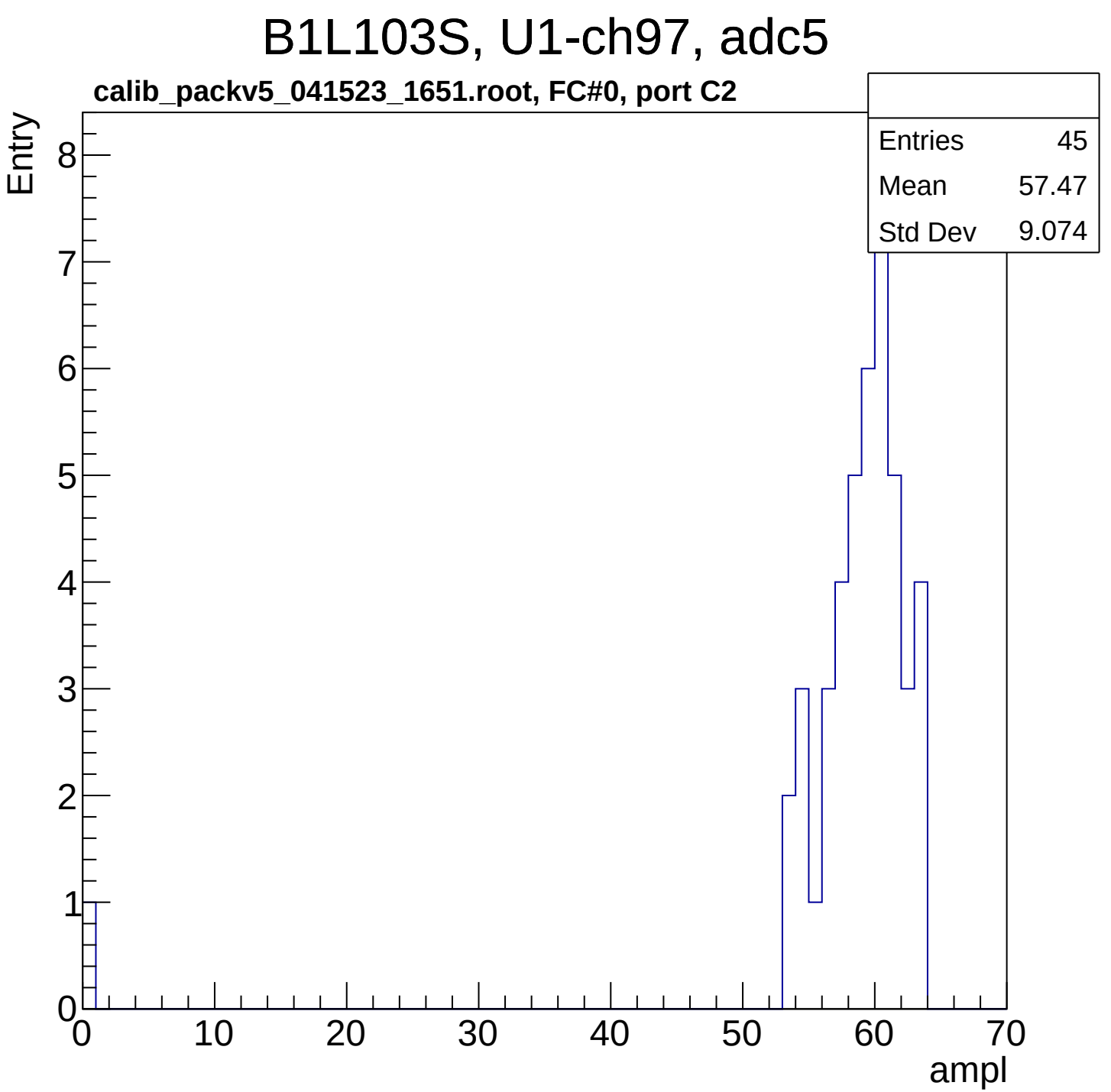
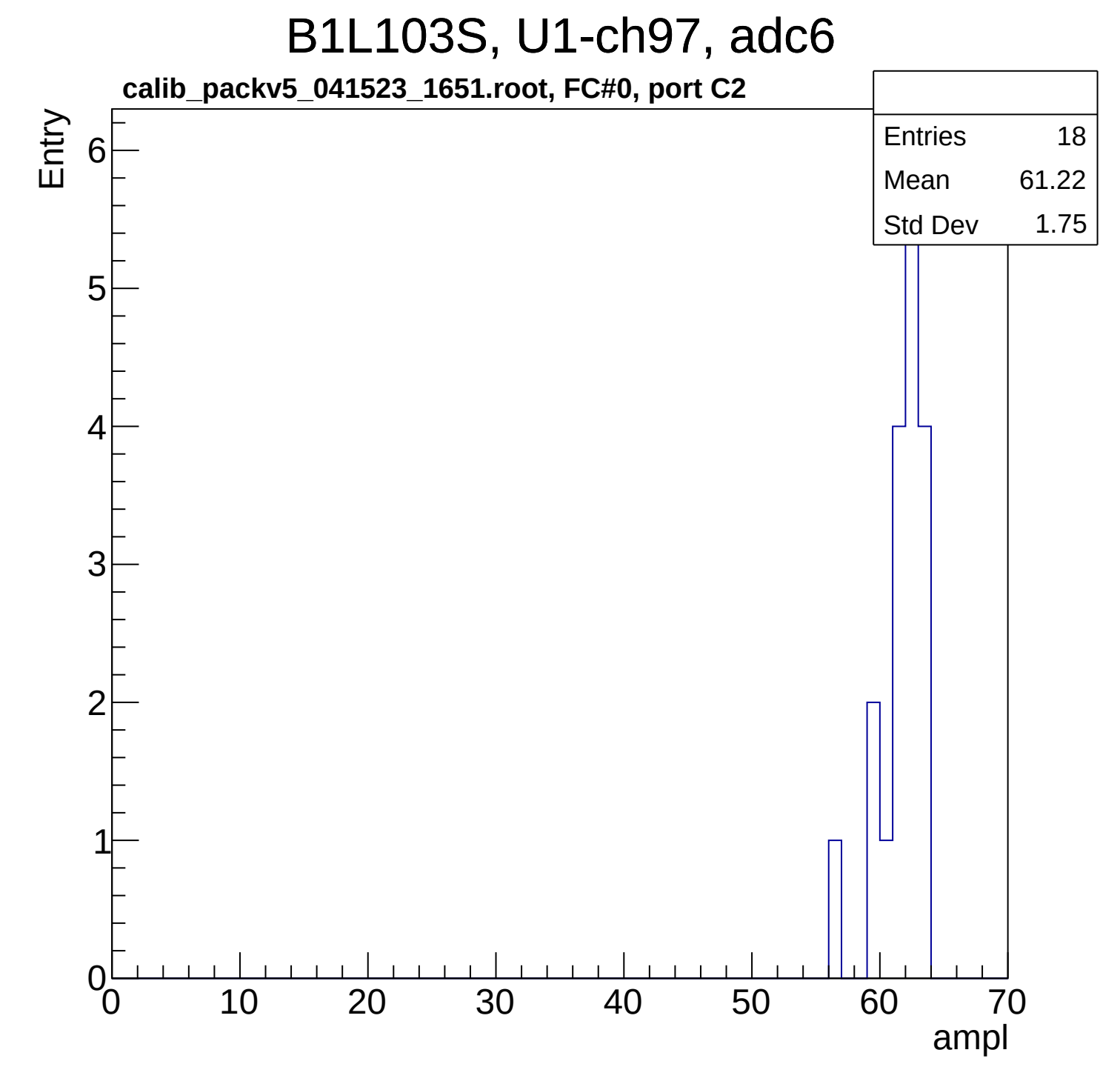
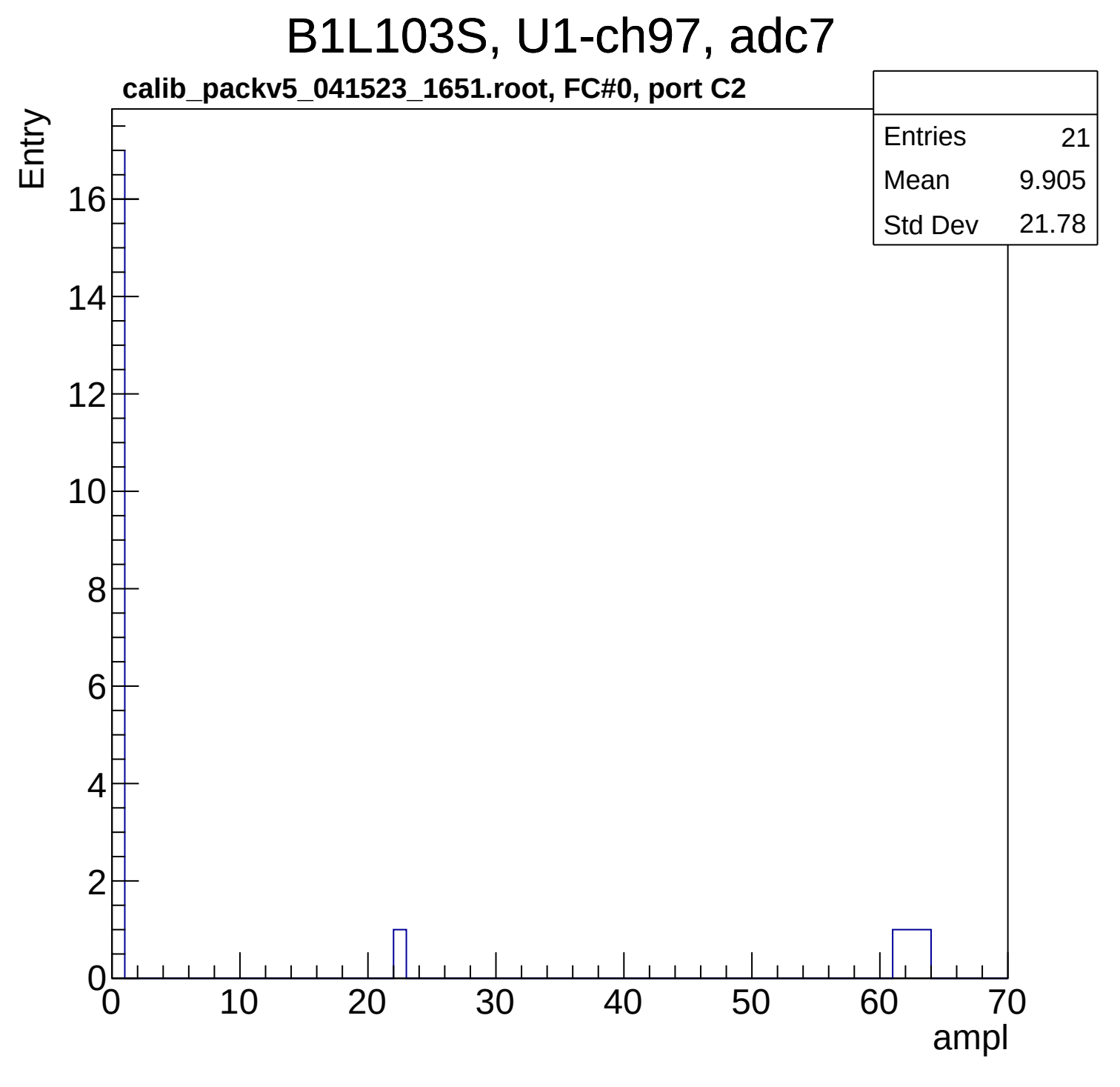

B1L103S, U1-ch97, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 57.47
Std Dev 9.074
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U1-ch97, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 61.22
Std Dev 1.75
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U1-ch97, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 9.905
Std Dev 21.78
Entry
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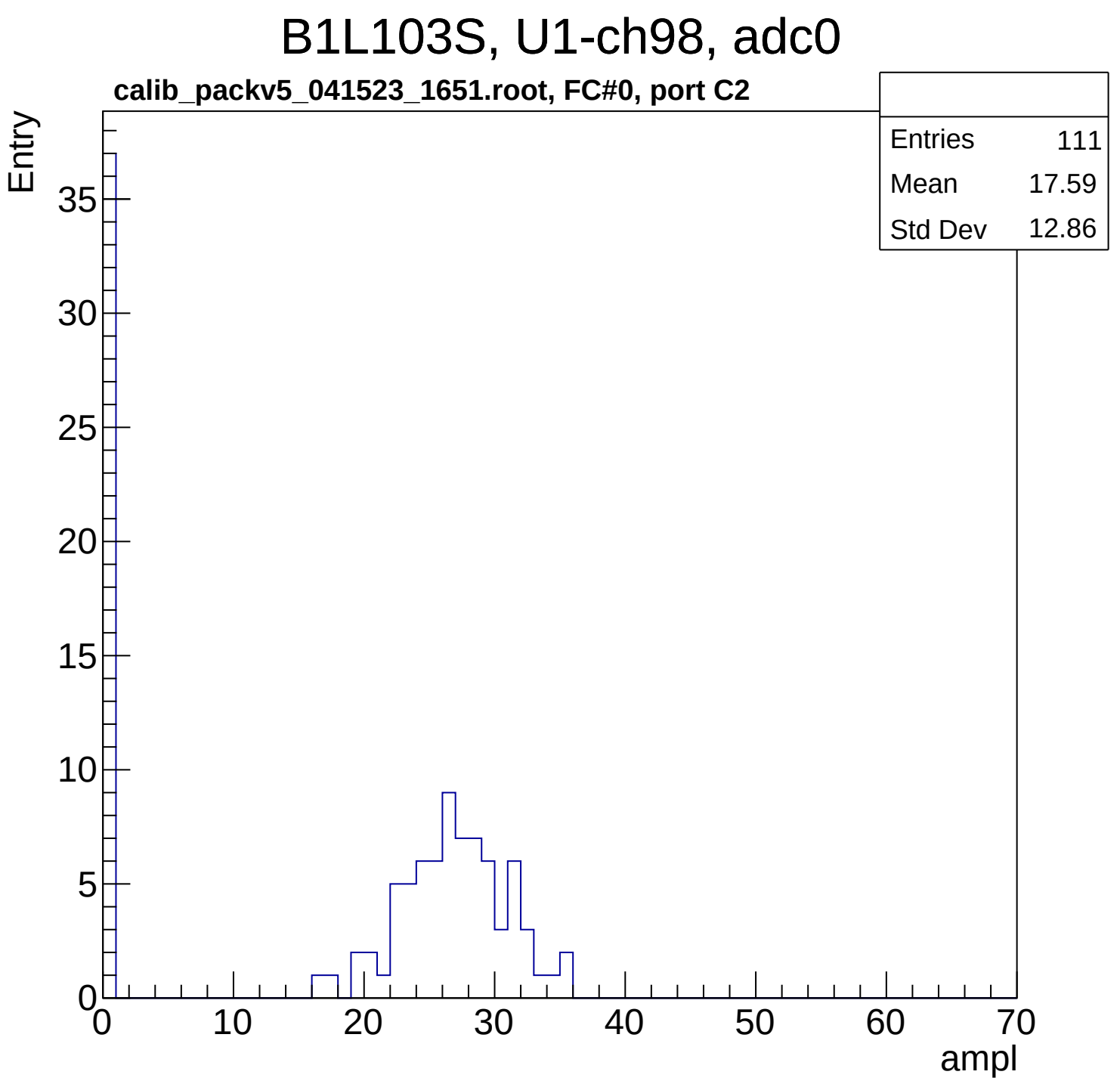
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch98, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 111
Mean 17.59
Std Dev 12.86
Entry
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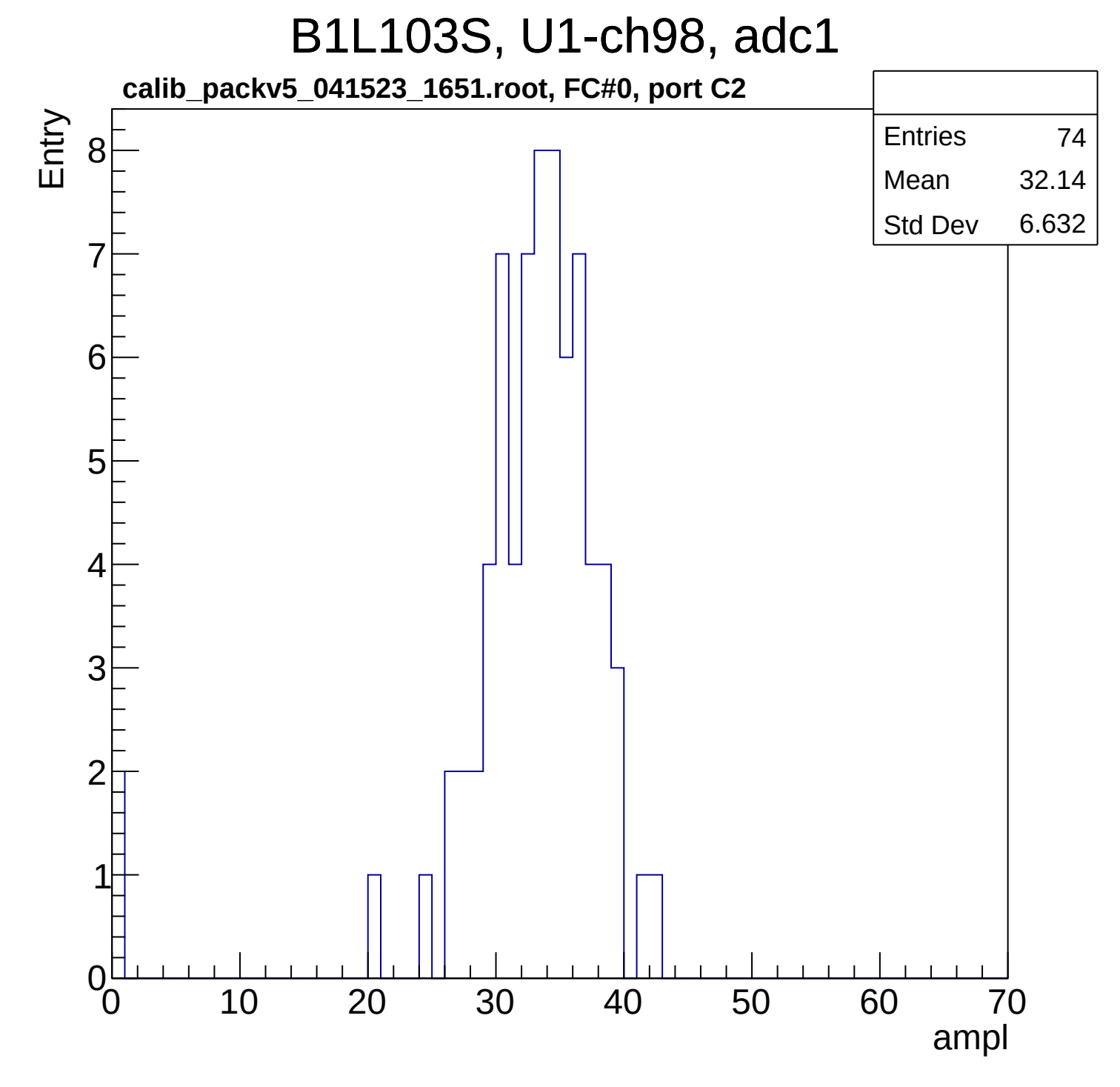
5
10
15
20
25
30
35
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch98, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 32.14
Std Dev 6.632
Entry
ampl
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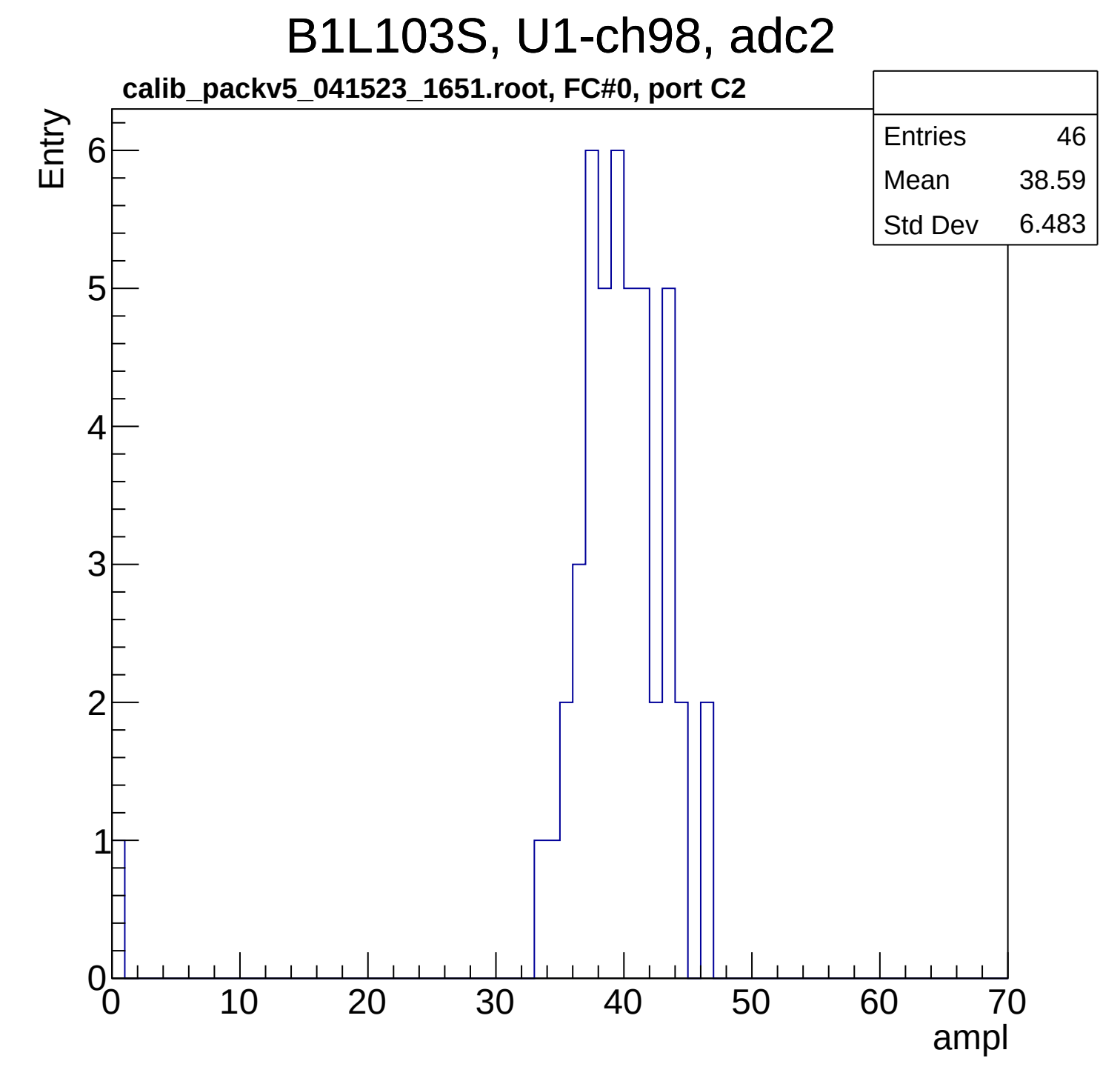
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U1-ch98, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 38.59
Std Dev 6.483
Entry
ampl
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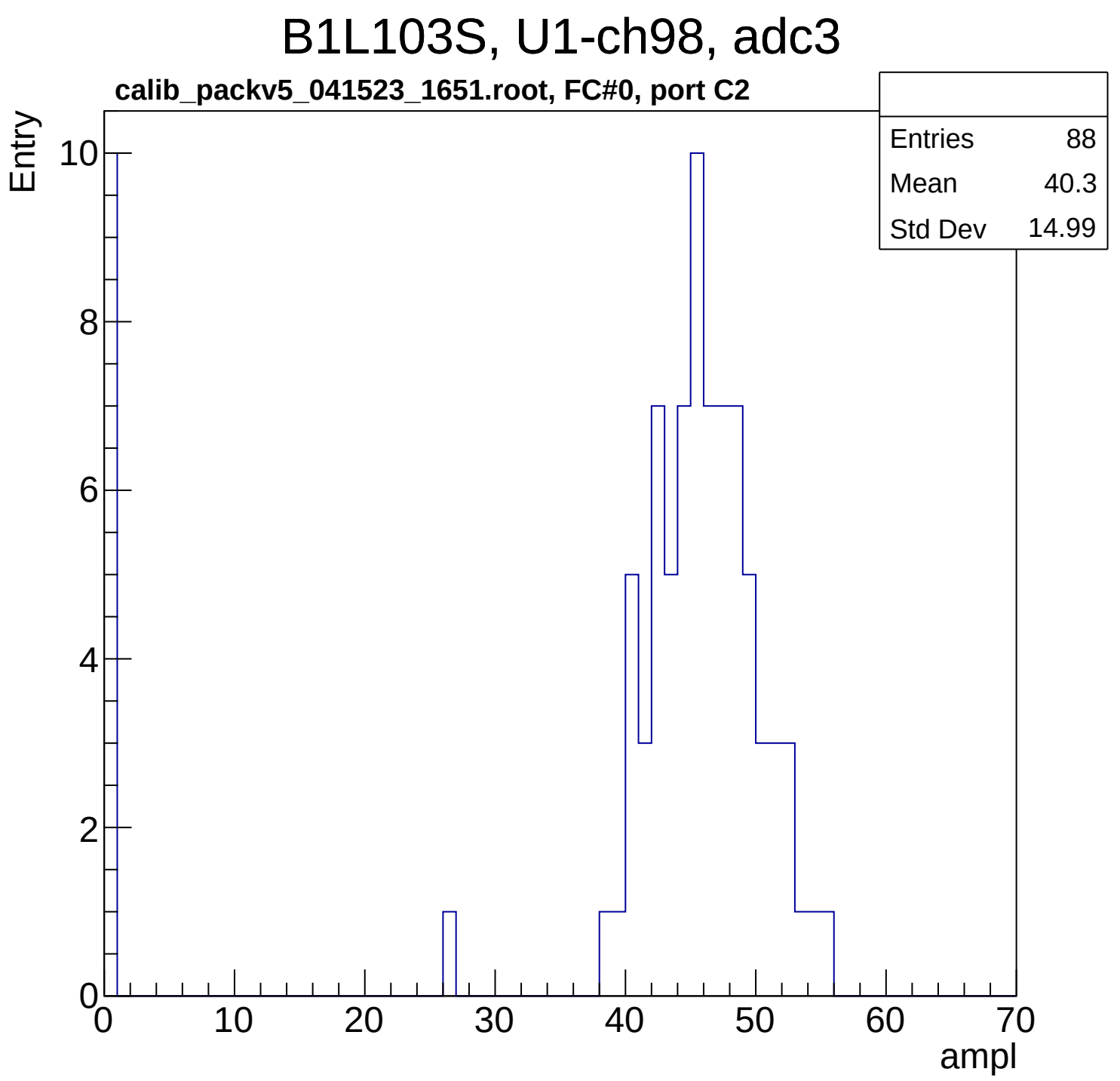
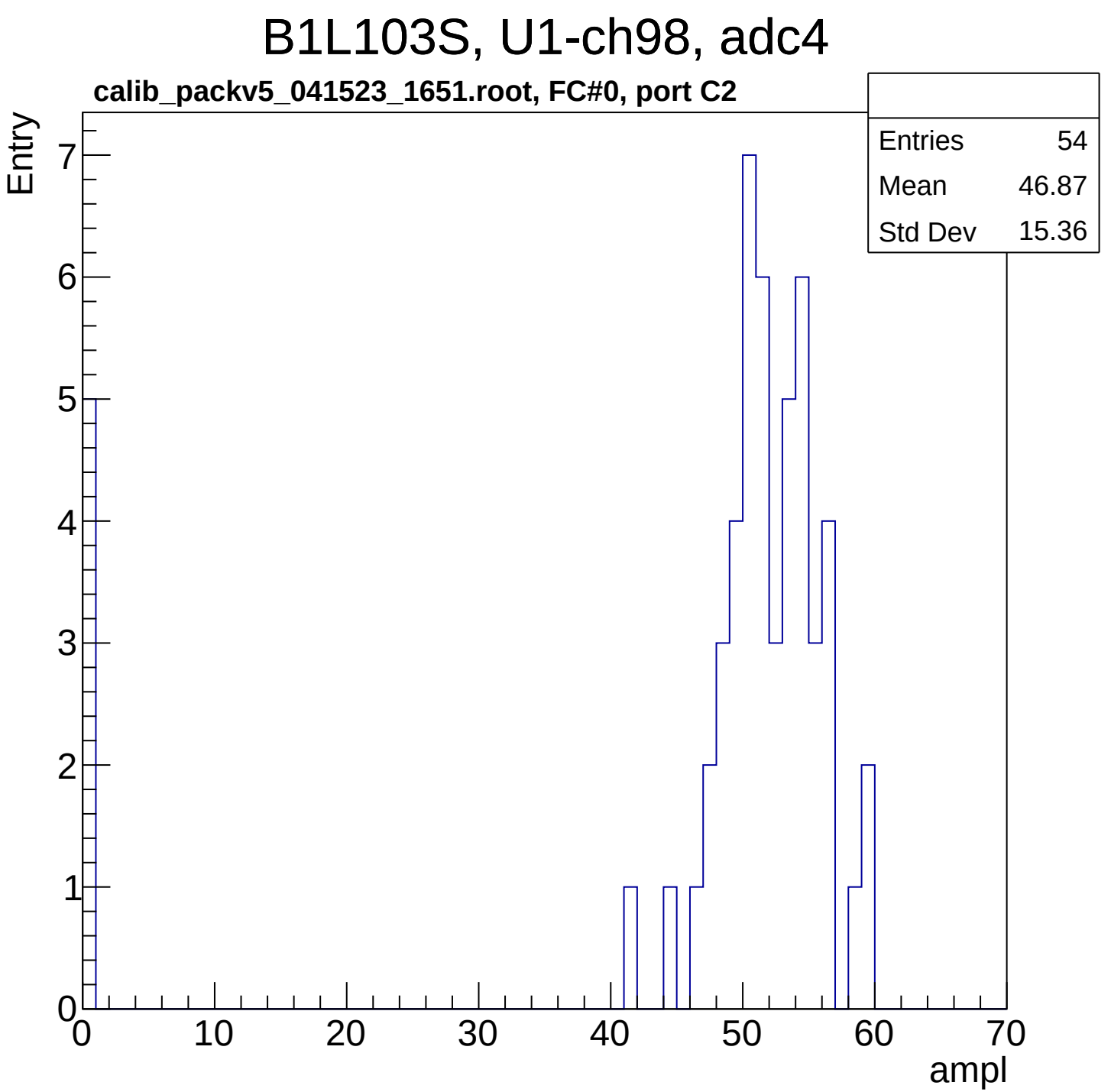
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U1-ch98, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 88
Mean 40.3
Std Dev 14.99
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch98, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 46.87
Std Dev 15.36
Entry
ampl
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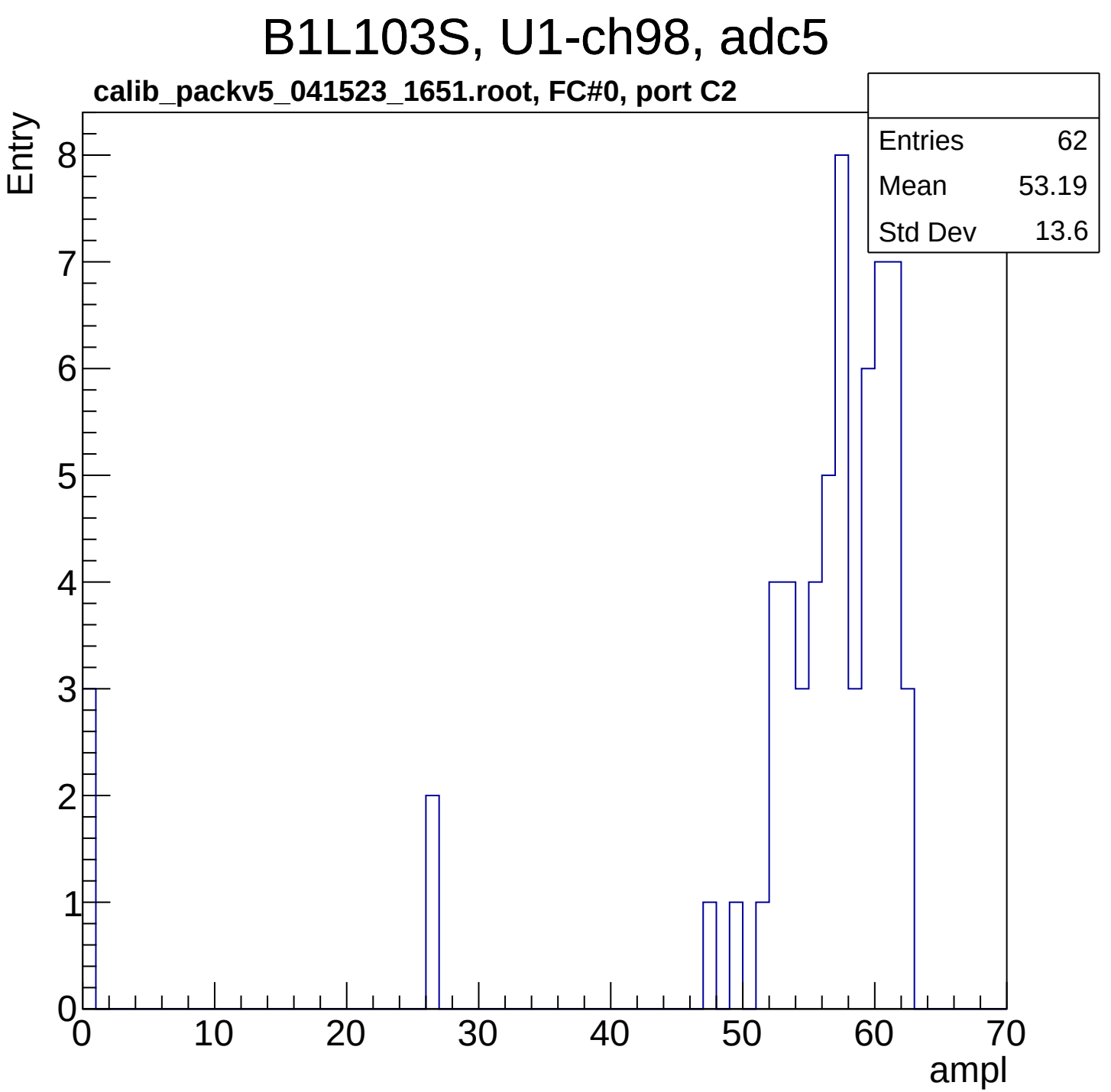
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U1-ch98, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 53.19
Std Dev 13.6
Entry
ampl
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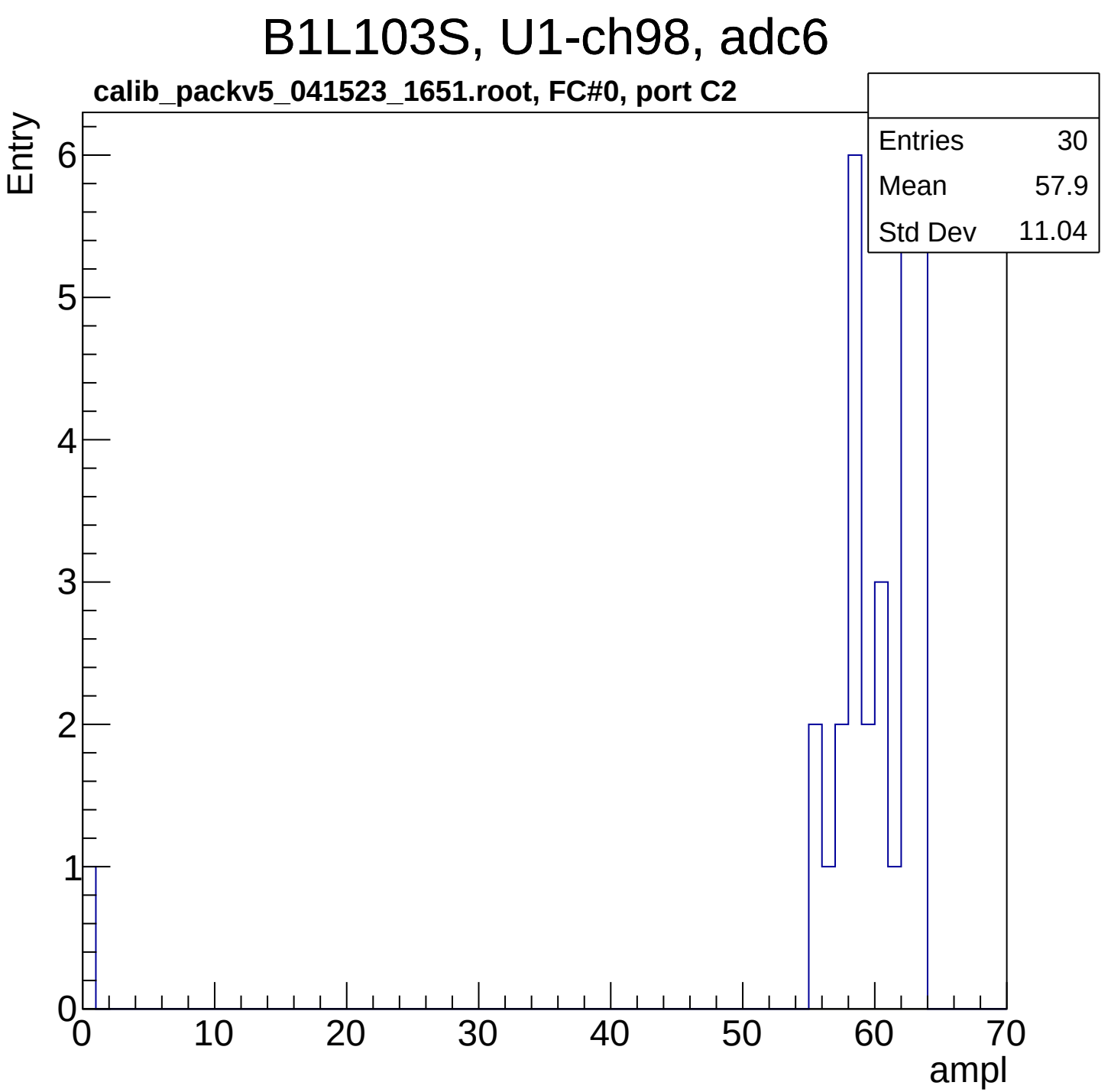
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U1-ch98, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 30
Mean 57.9
Std Dev 11.04
Entry
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2
3
4
5
6
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10
20
30
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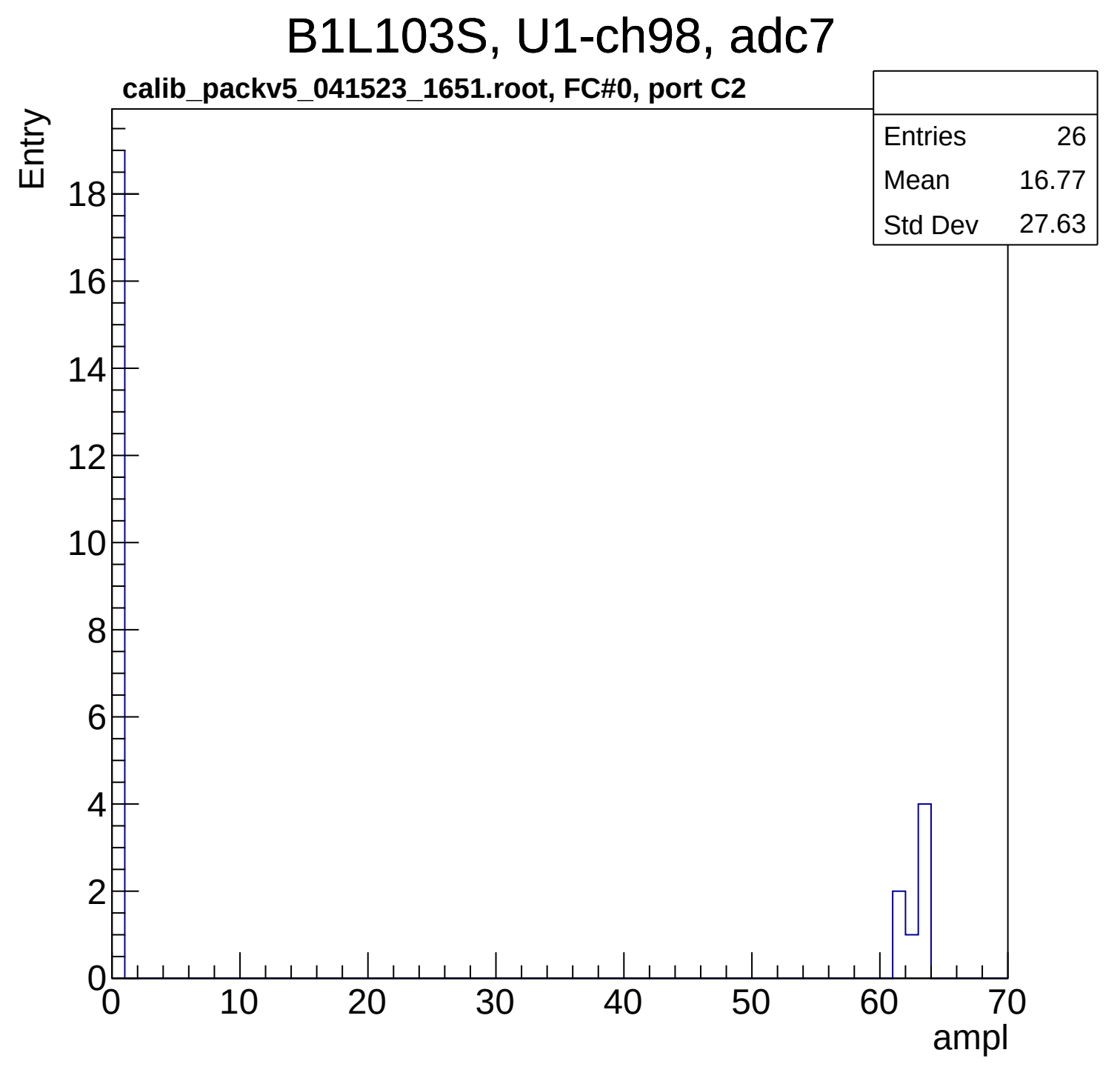
50
60
70
ampl


B1L103S, U1-ch98, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 26
Mean 16.77
Std Dev 27.63
Entry
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2
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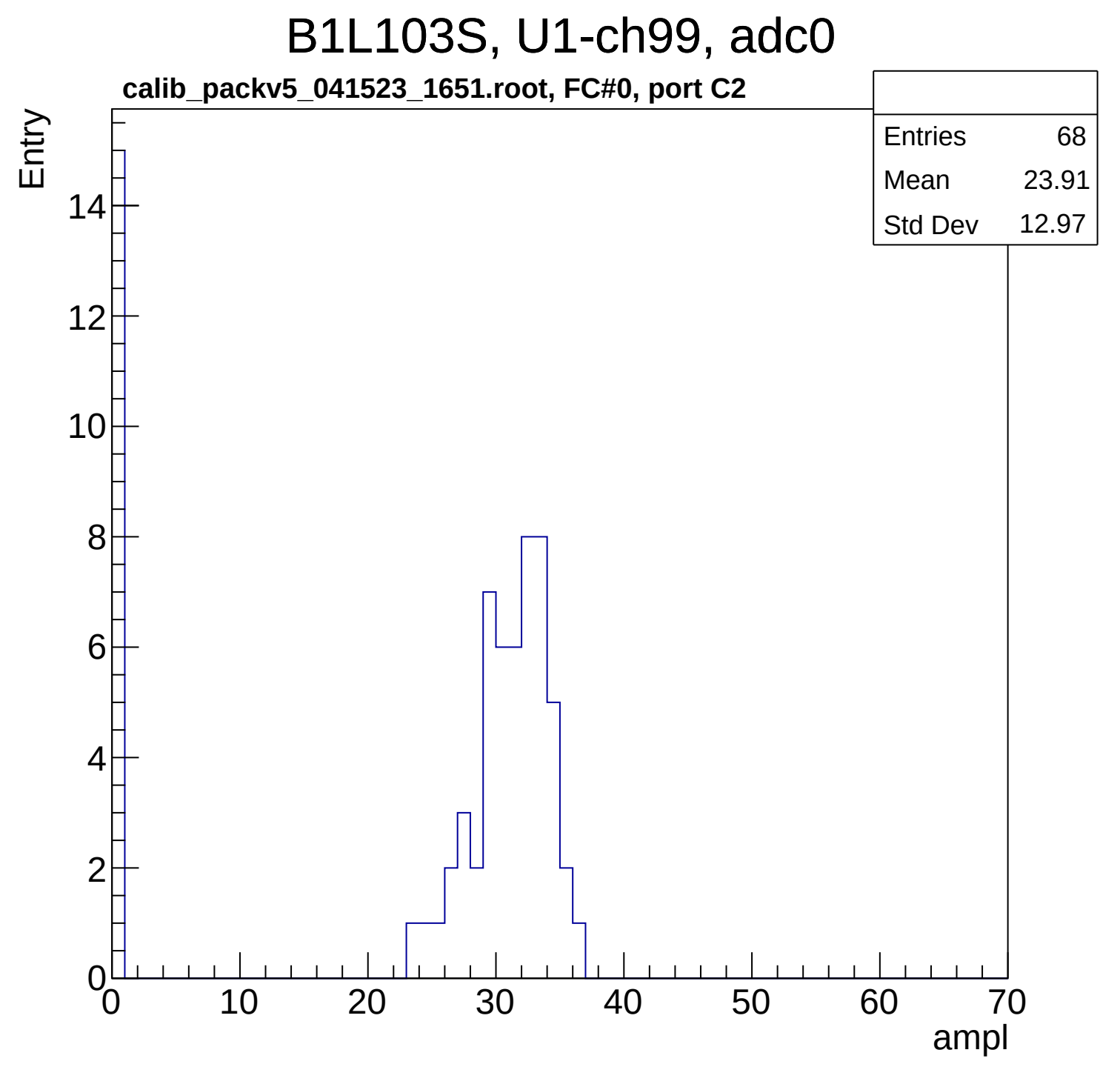
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch99, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 23.91
Std Dev 12.97
Entry
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2
4
6
8
10
12
14
0
10
20
30
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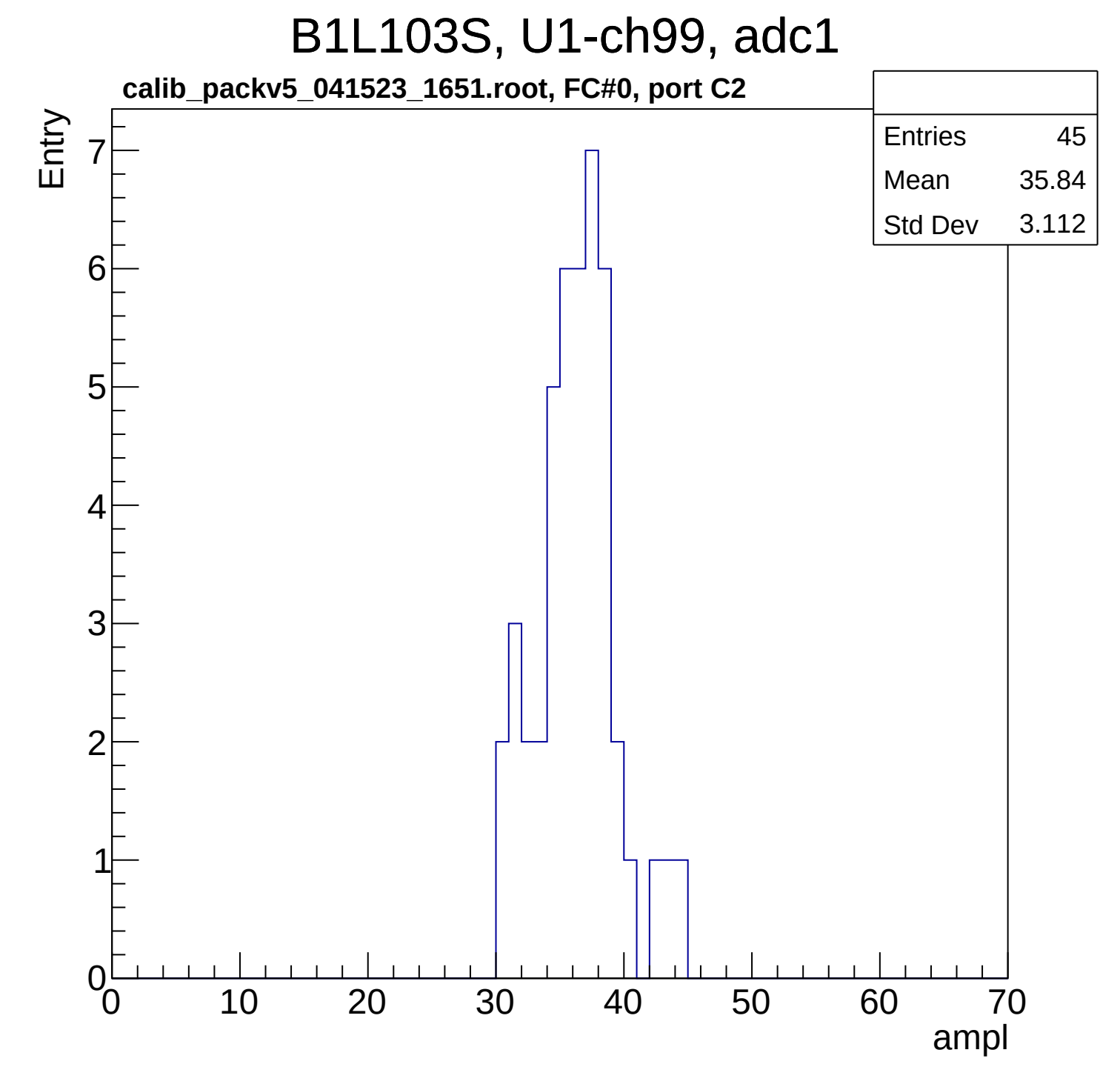
50
60
70
ampl


B1L103S, U1-ch99, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 35.84
Std Dev 3.112
Entry
ampl
0
1
2
3
4
5
6
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0
10
20
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60
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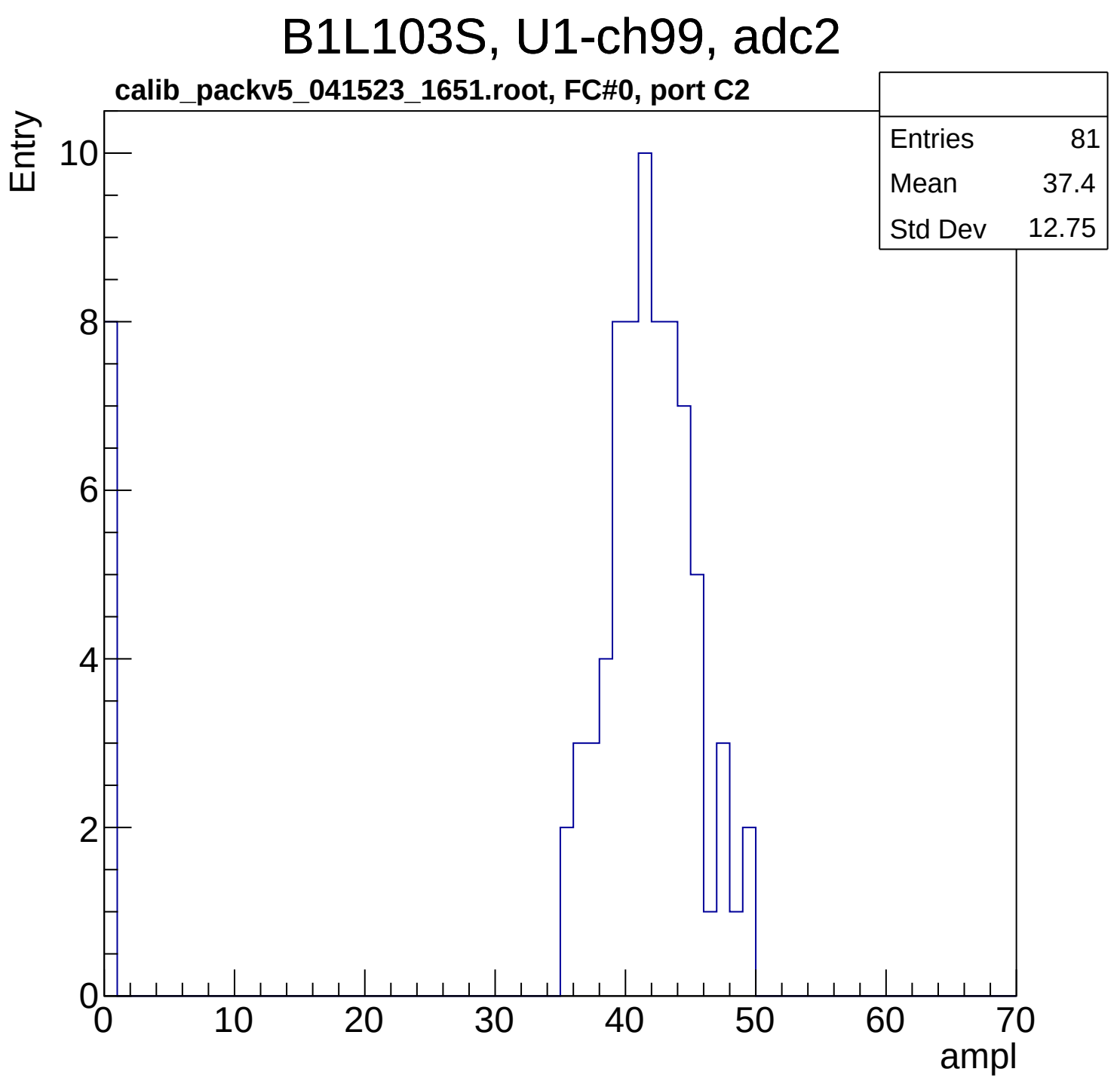
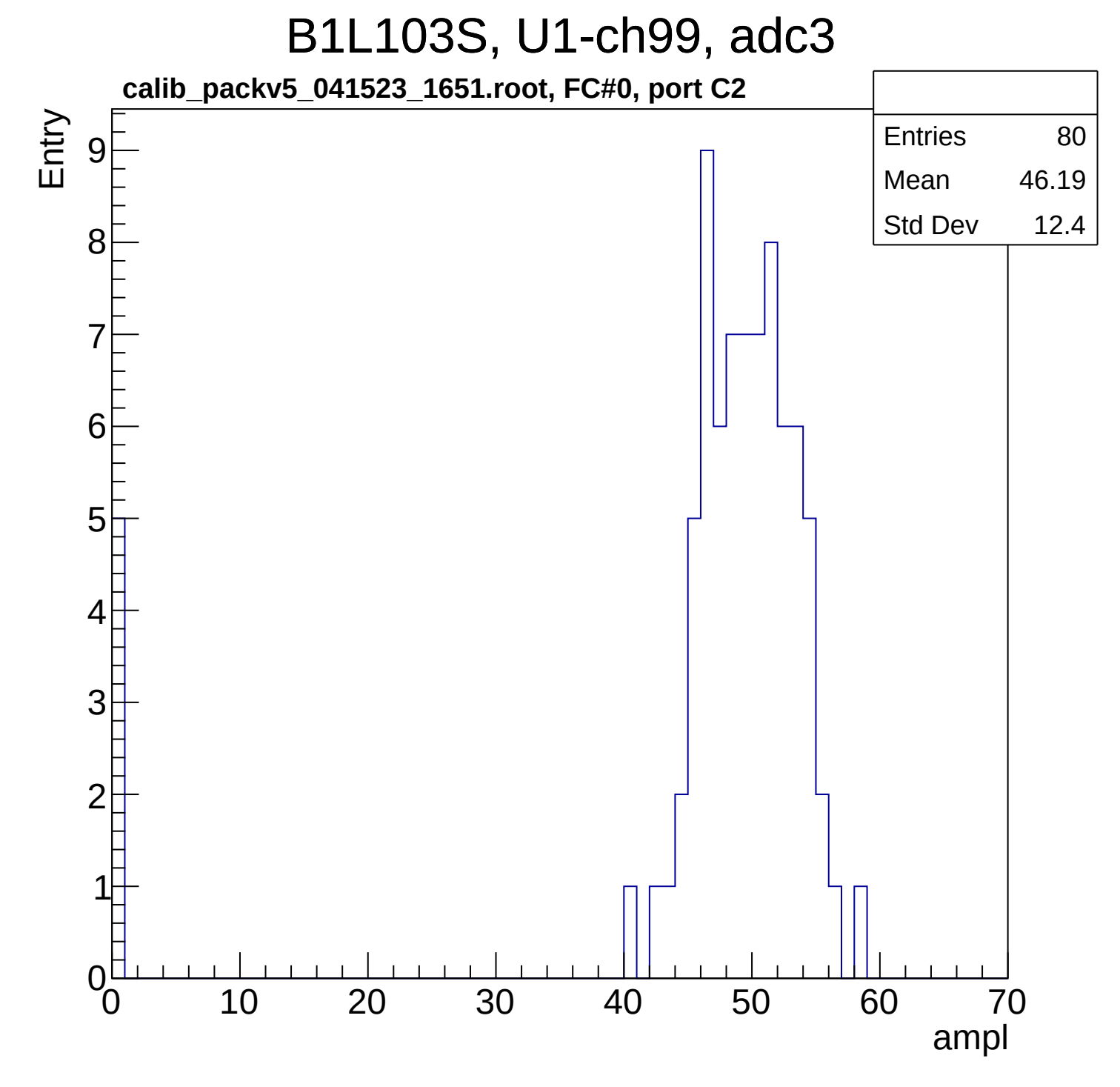

B1L103S, U1-ch99, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 37.4
Std Dev 12.75
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch99, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 46.19
Std Dev 12.4
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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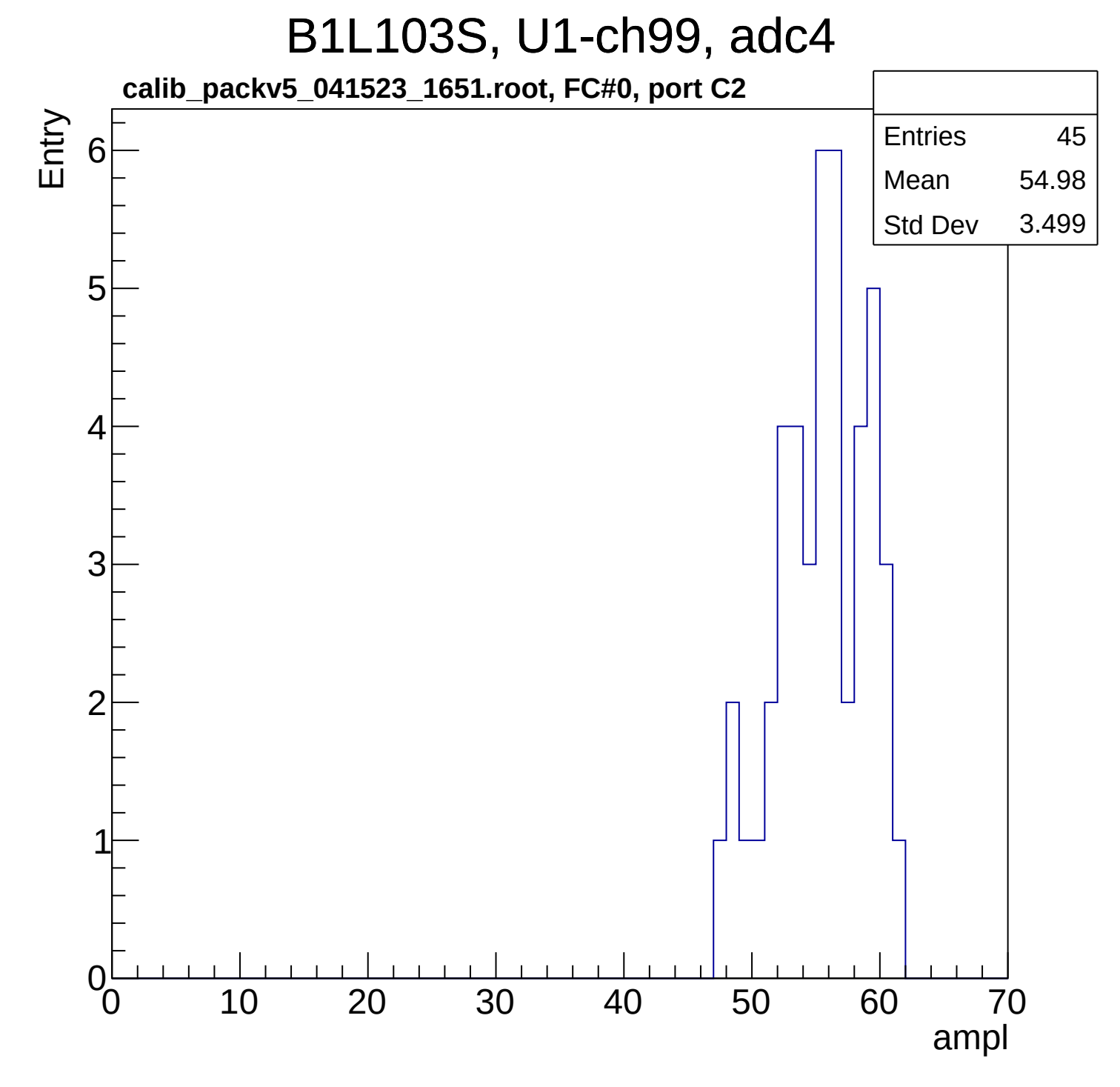
60
70


B1L103S, U1-ch99, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 54.98
Std Dev 3.499
Entry
ampl
0
1
2
3
4
5
6
0
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20
30
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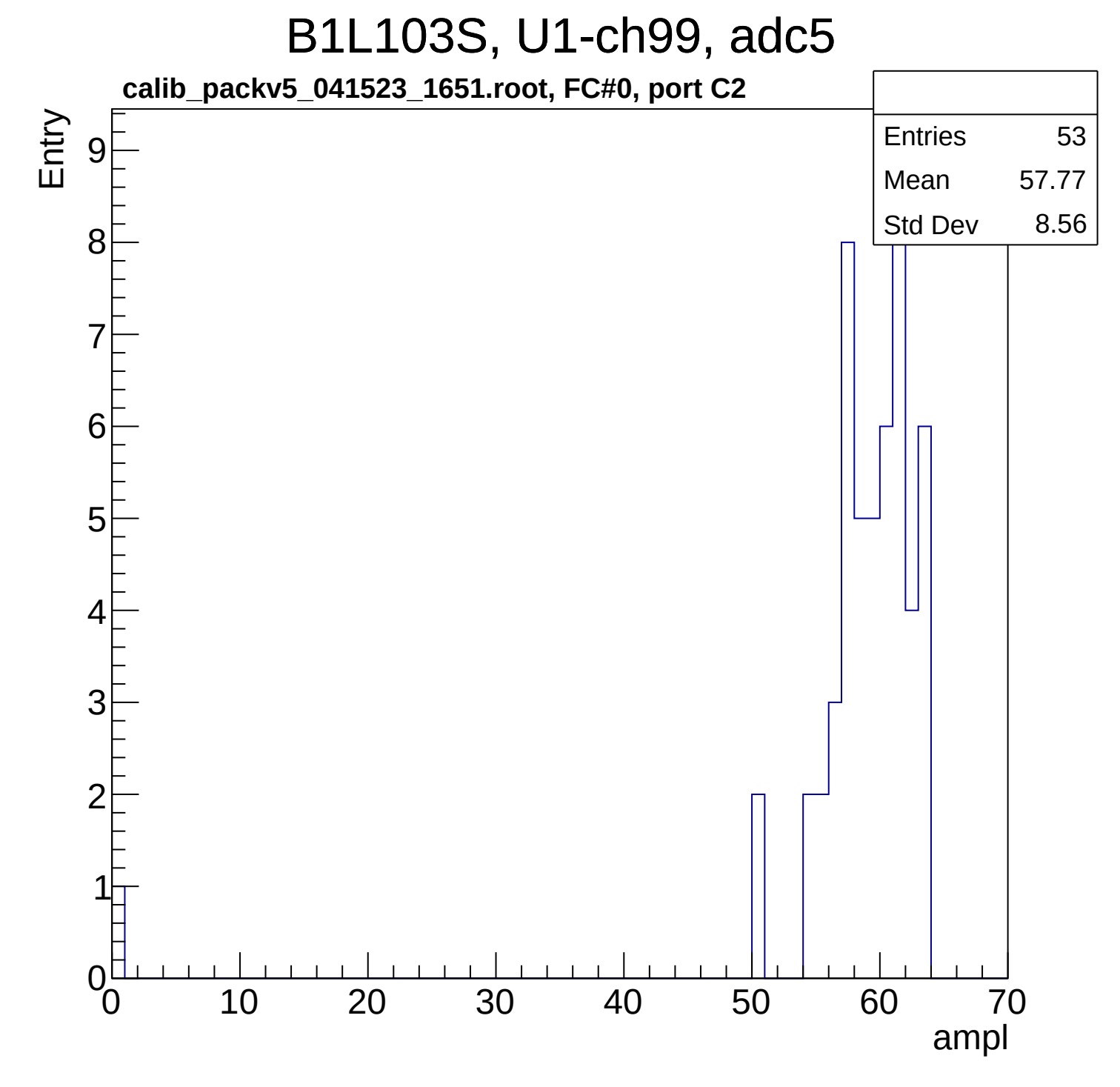
B1L103S, U1-ch99, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 57.77
Std Dev 8.56
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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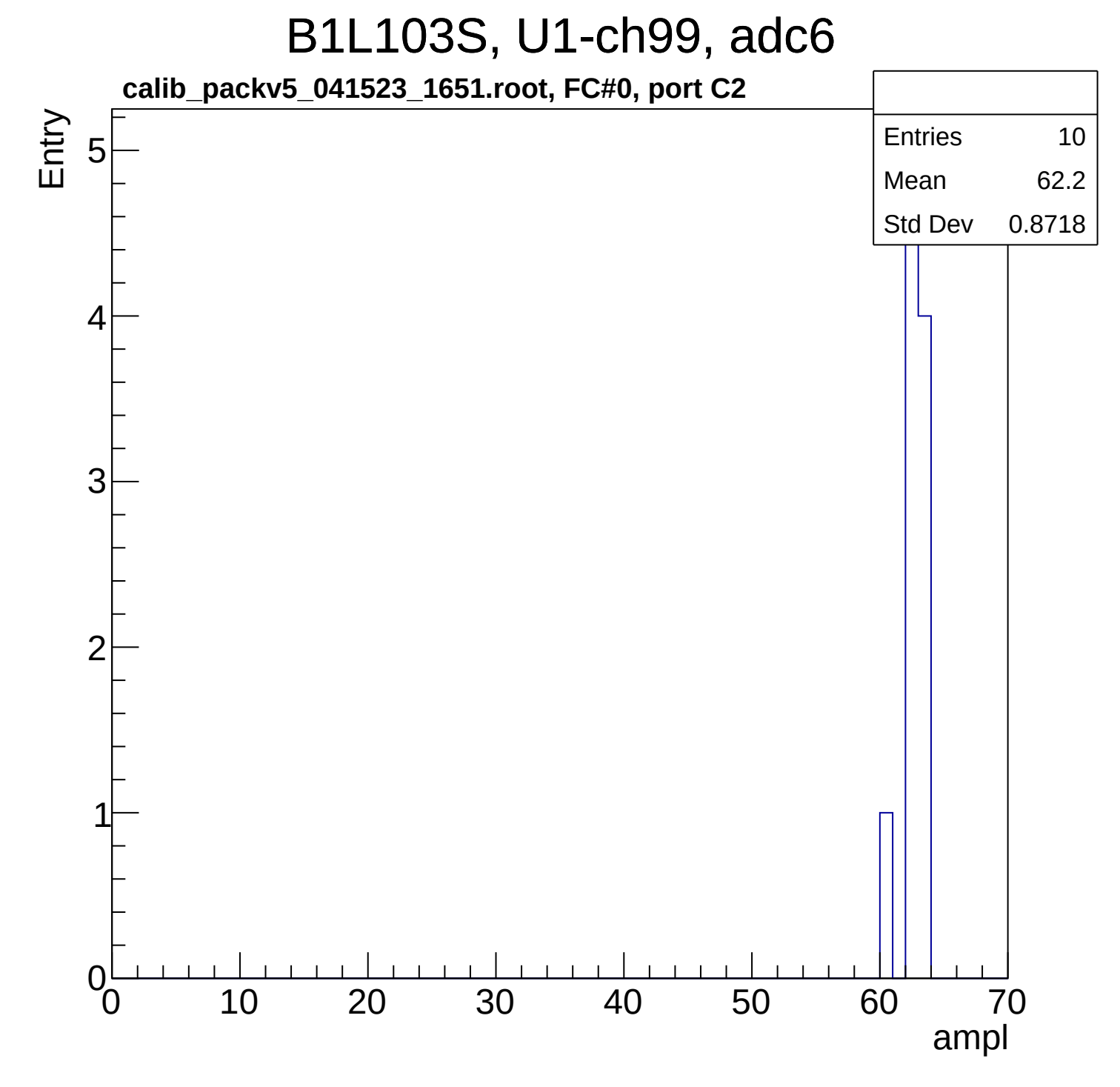
B1L103S, U1-ch99, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 62.2
Std Dev 0.8718
Entry
ampl
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1
2
3
4
5
0
10
20
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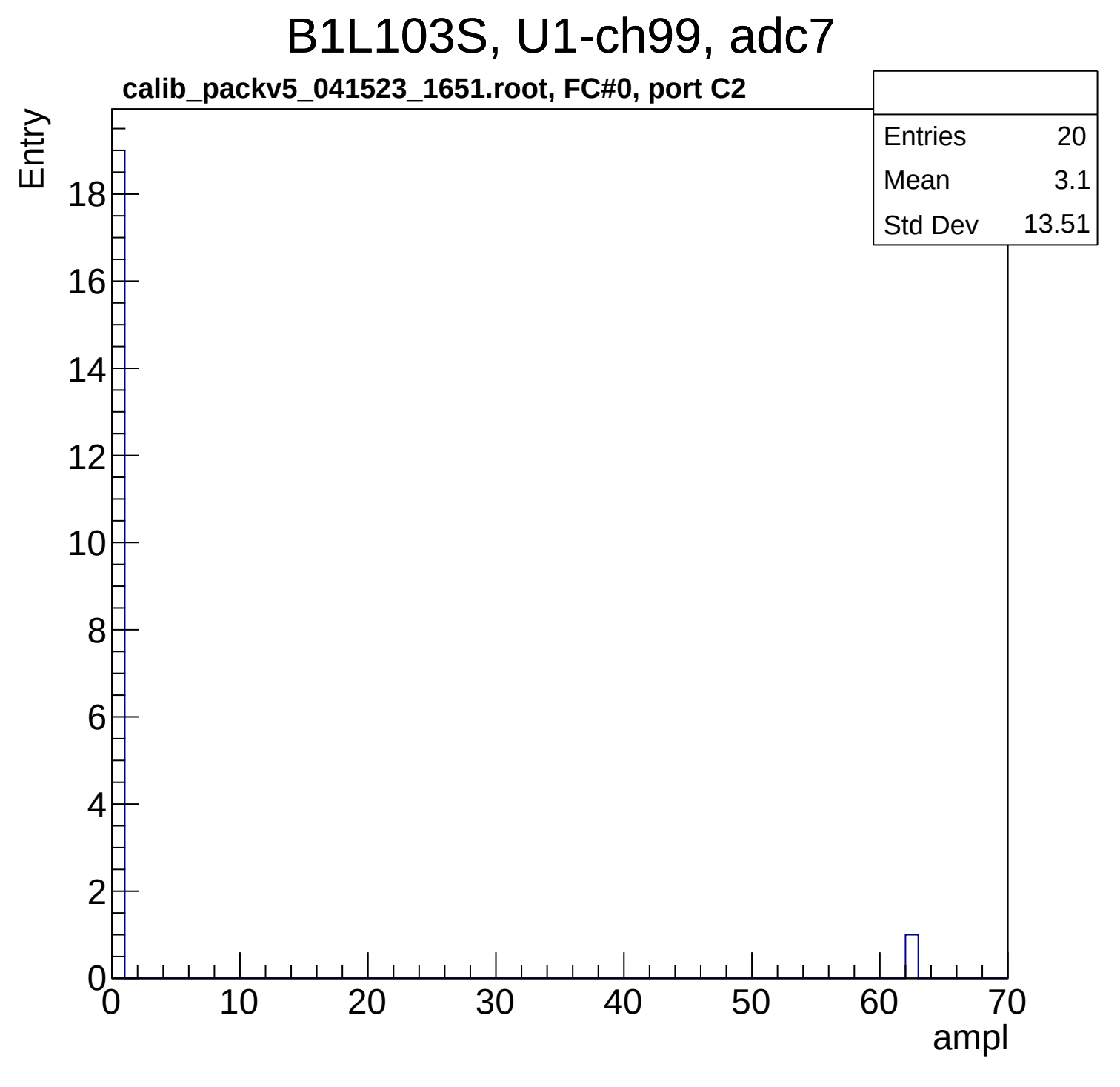
40
50
60
70


B1L103S, U1-ch99, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.1
Std Dev 13.51
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
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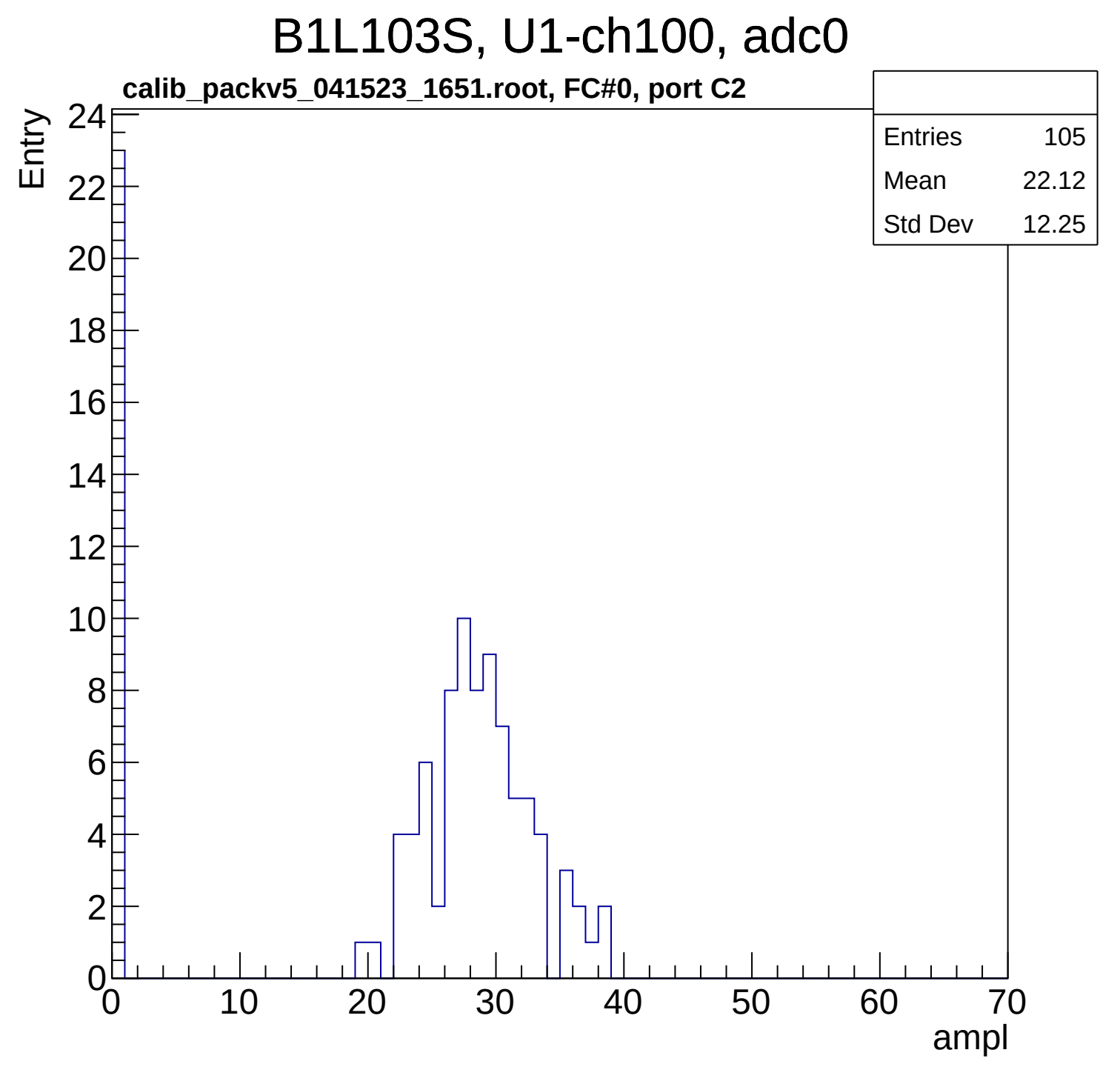
50
60
70
ampl


B1L103S, U1-ch100, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 105
Mean 22.12
Std Dev 12.25
Entry
ampl
0
2
4
6
8
10
12
14
16
18
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0
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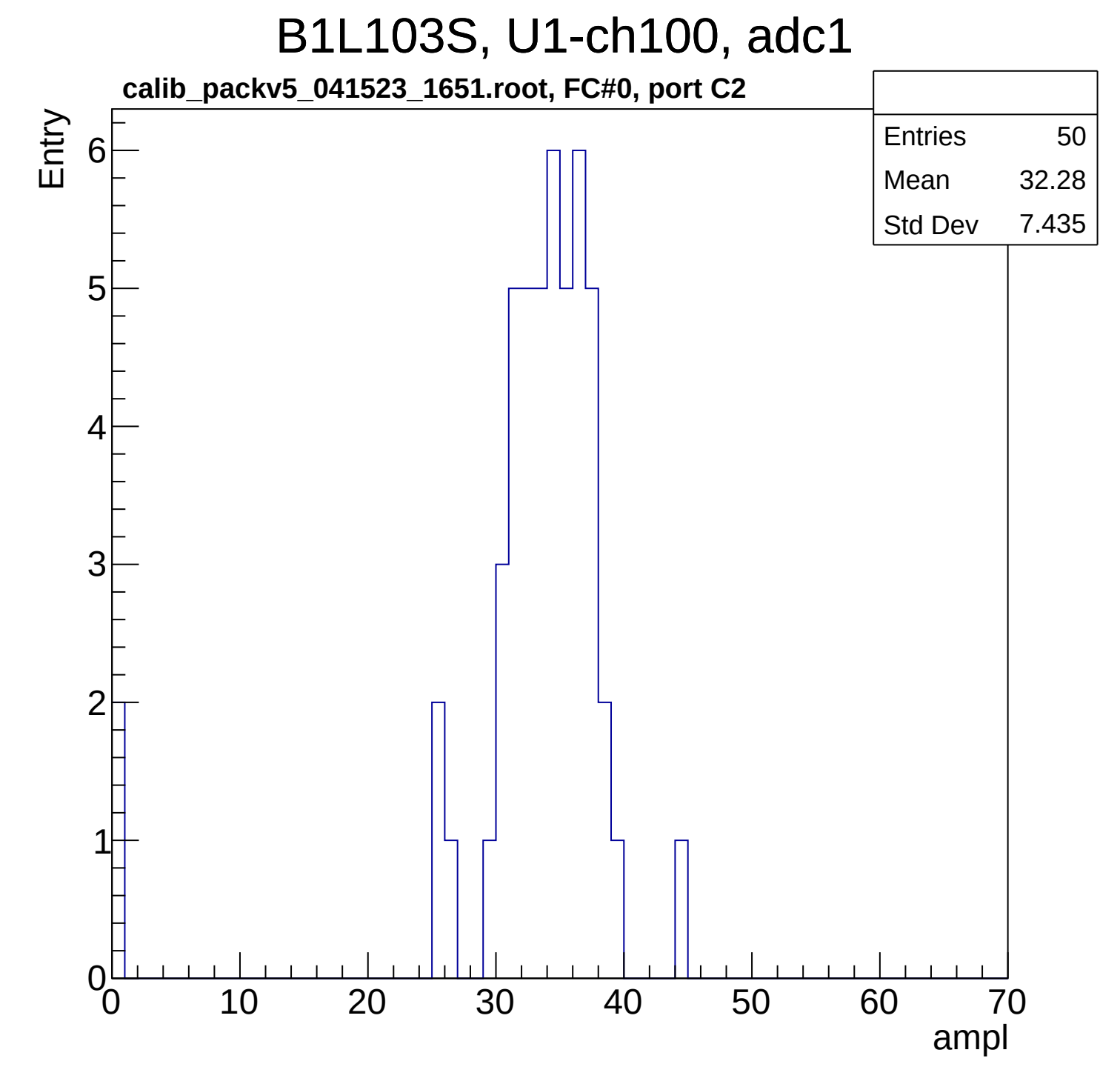
B1L103S, U1-ch100, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 32.28
Std Dev 7.435
Entry
ampl
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1
2
3
4
5
6
0
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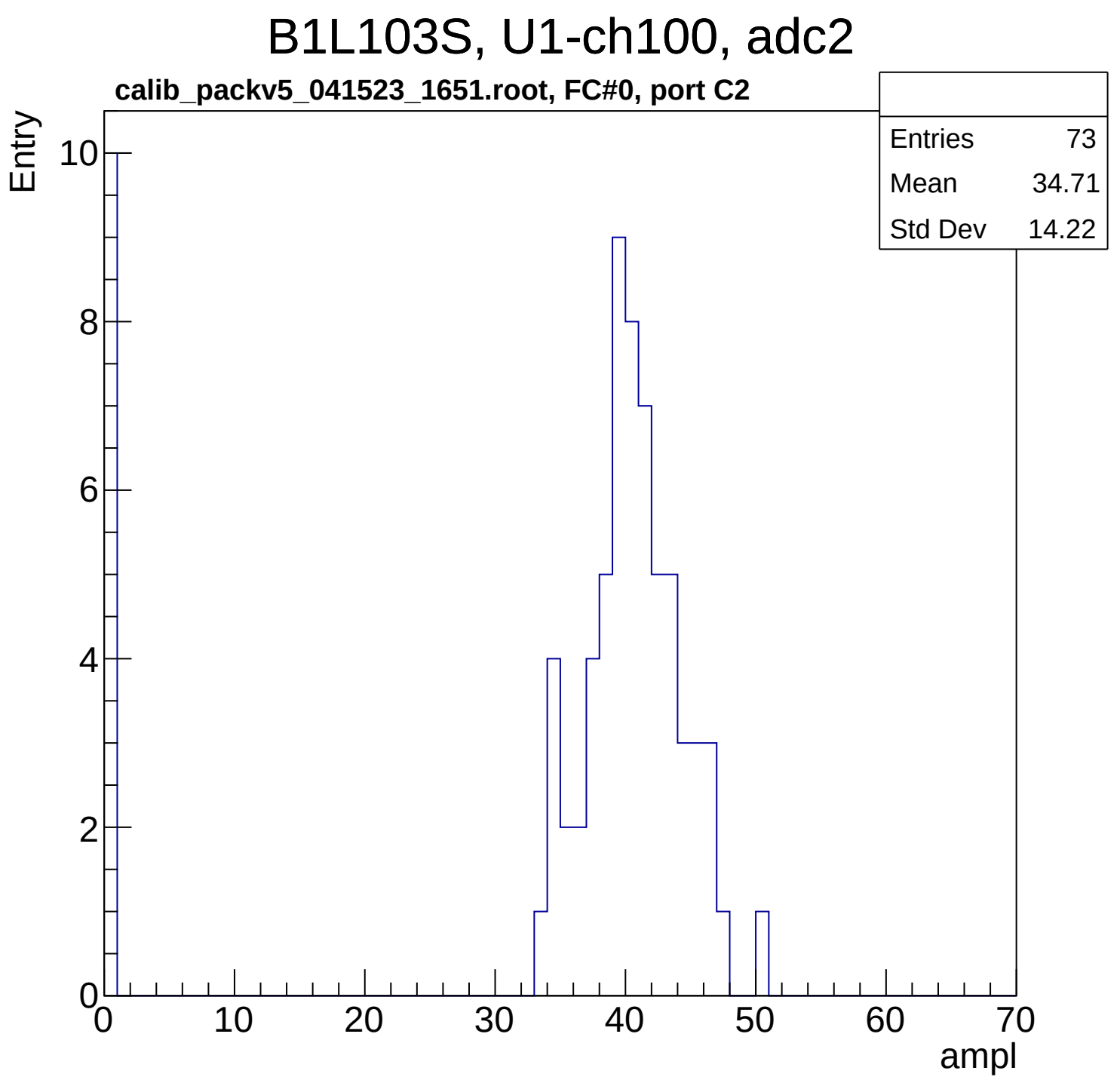
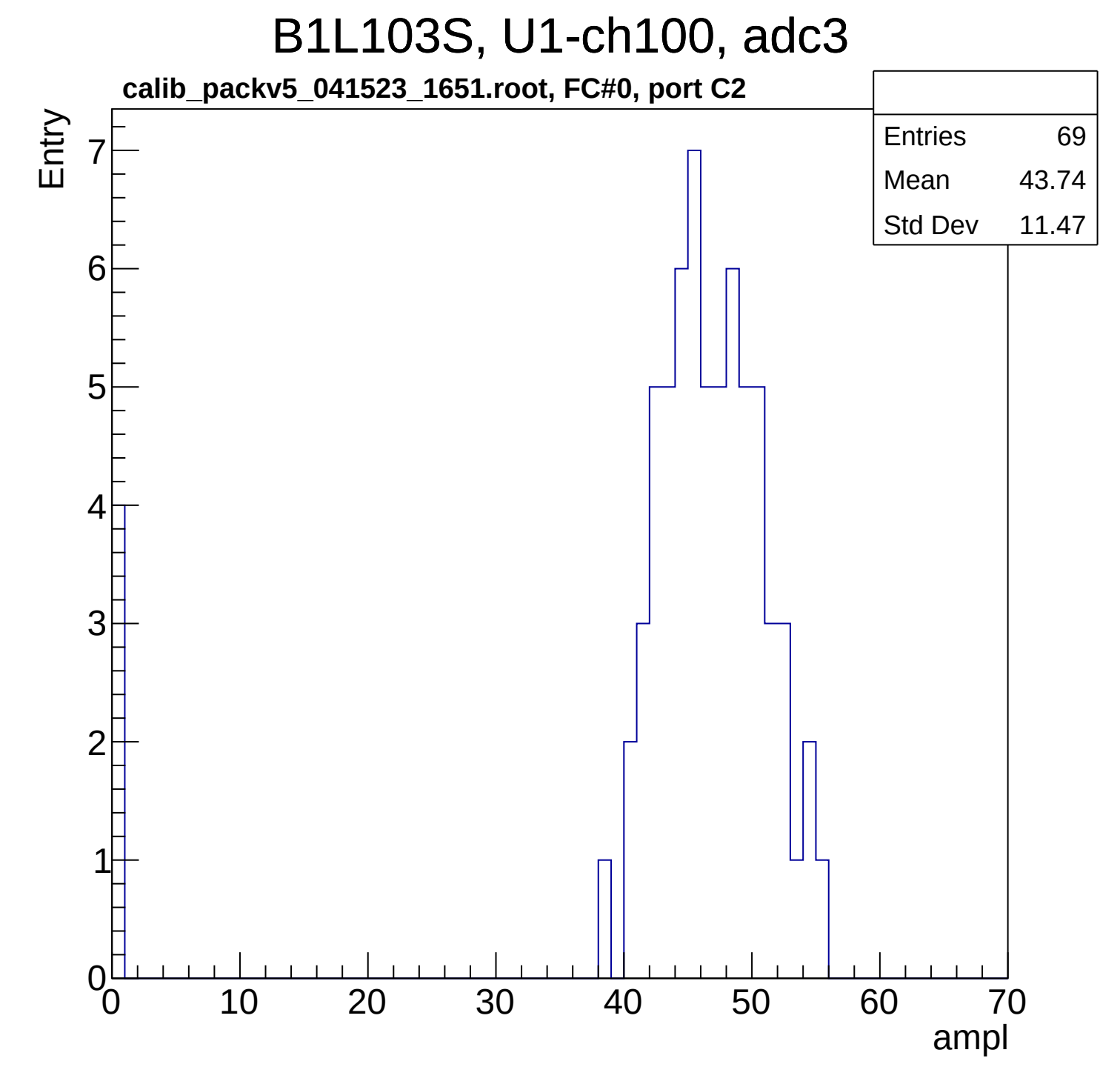
20
30
40
50
60
70


B1L103S, U1-ch100, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 34.71
Std Dev 14.22
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch100, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 43.74
Std Dev 11.47
Entry
ampl
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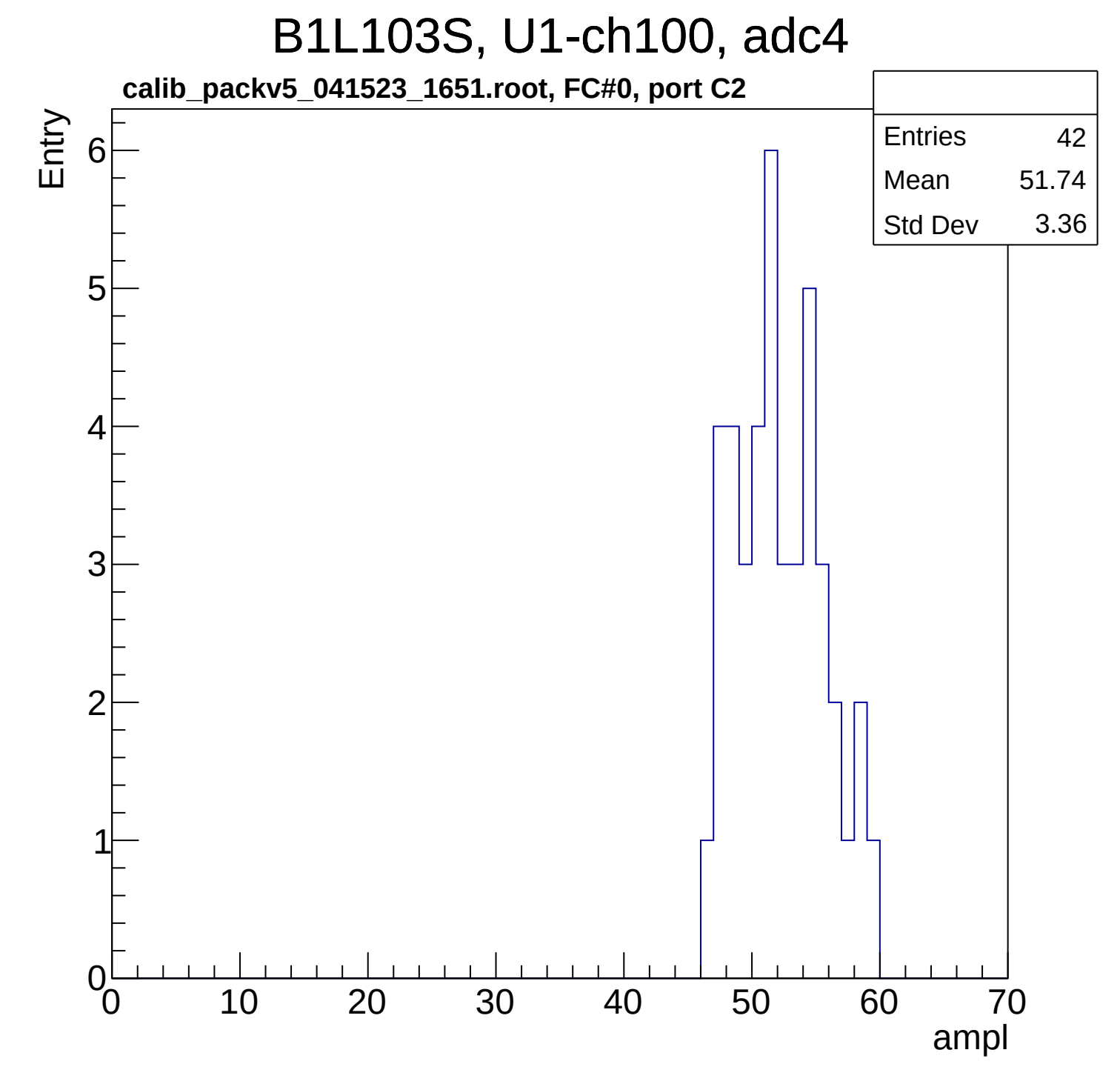
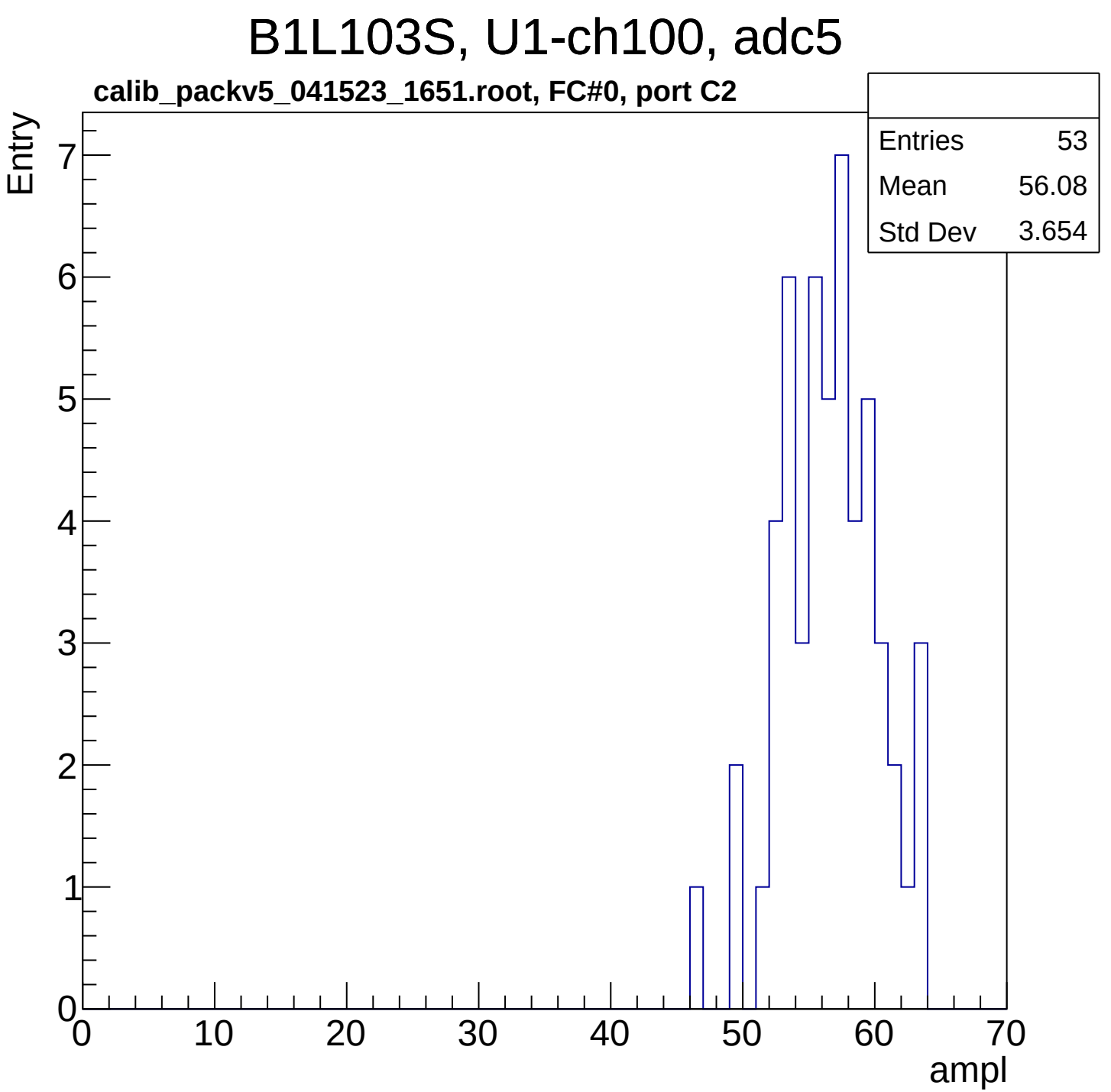
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U1-ch100, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 42
Mean 51.74
Std Dev 3.36
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U1-ch100, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 56.08
Std Dev 3.654
Entry
ampl
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1
2
3
4
5
6
7
0
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20
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40
50
60
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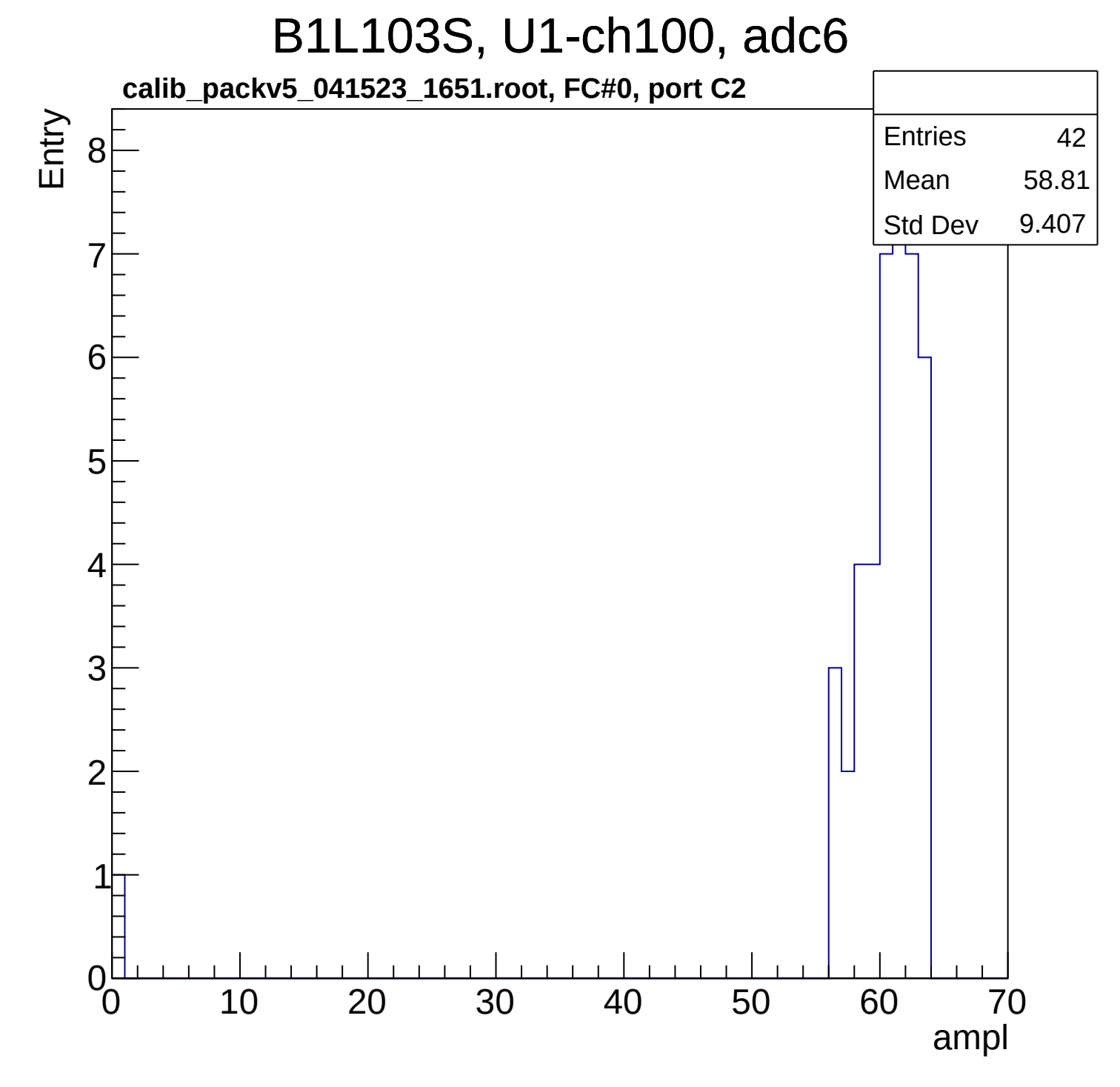
B1L103S, U1-ch100, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 42
Mean 58.81
Std Dev 9.407
Entry
ampl
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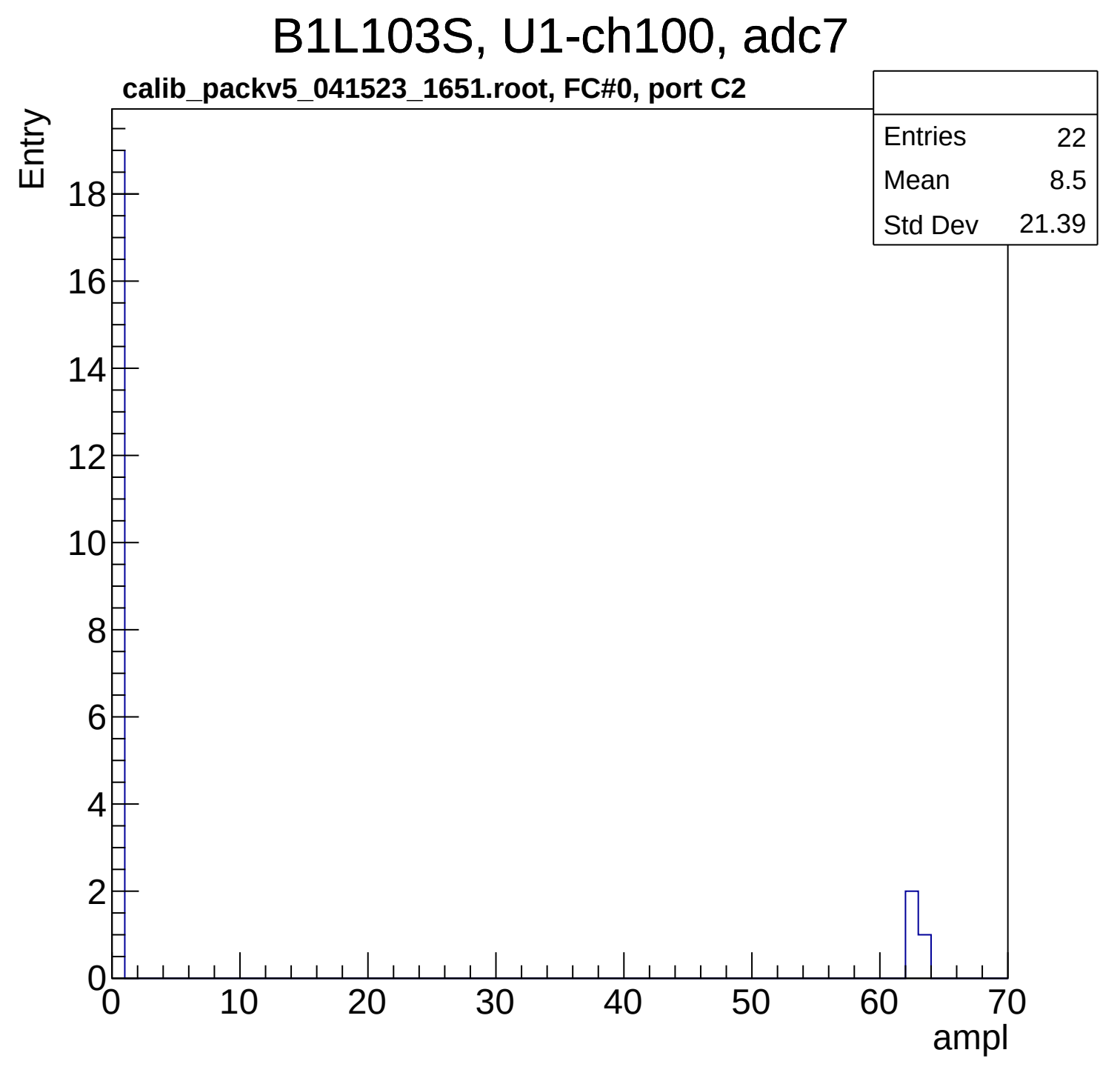
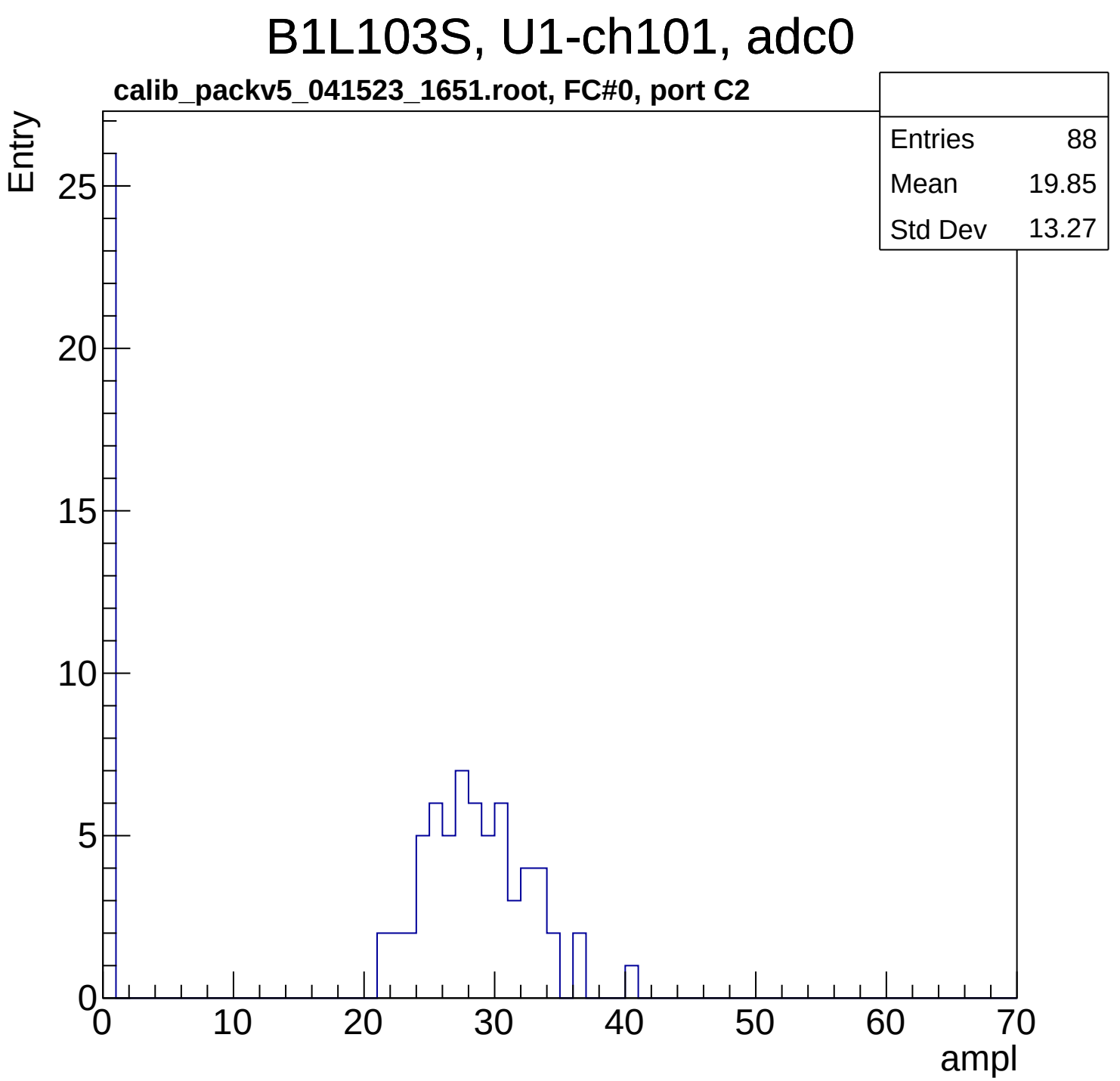
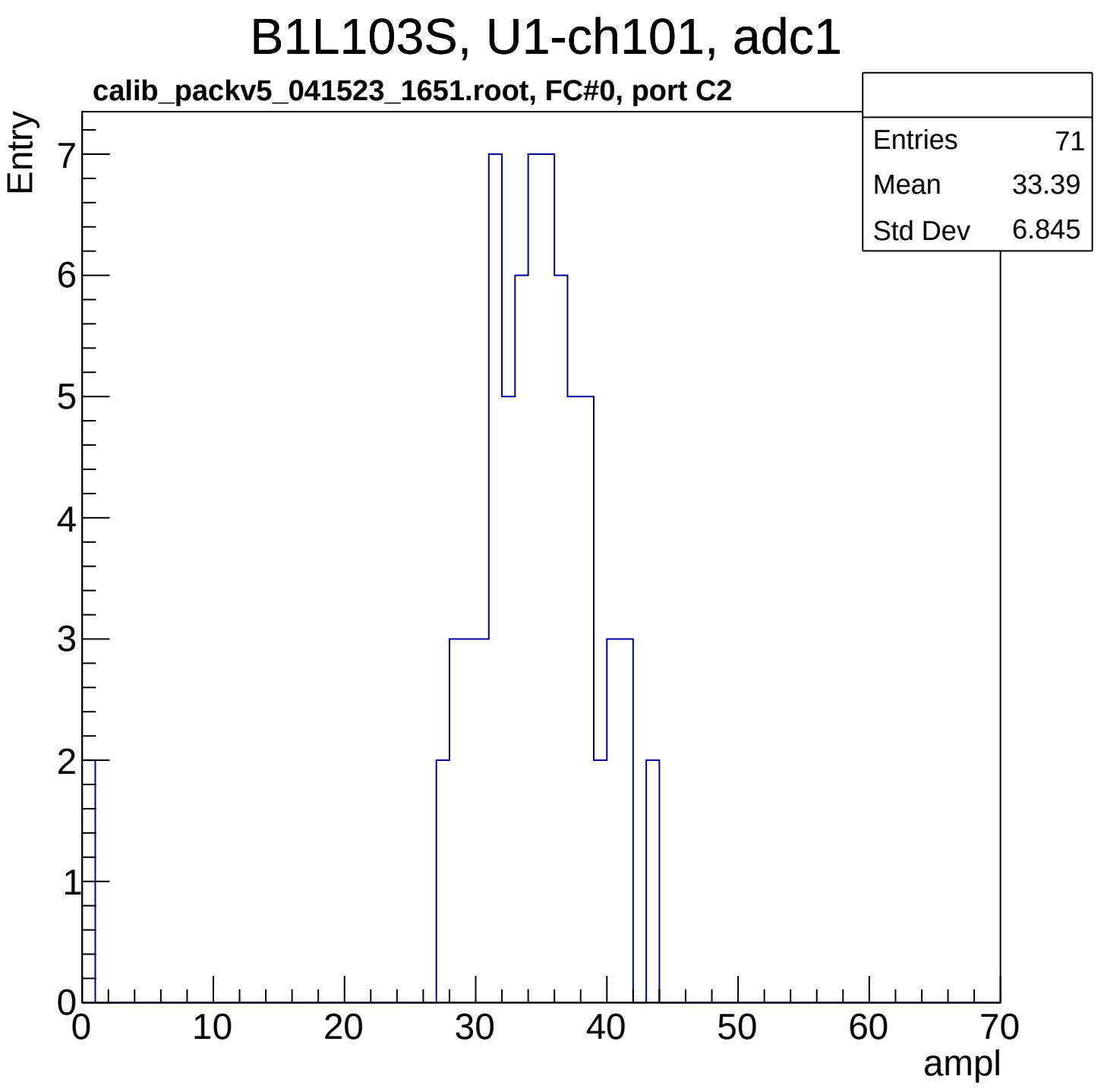
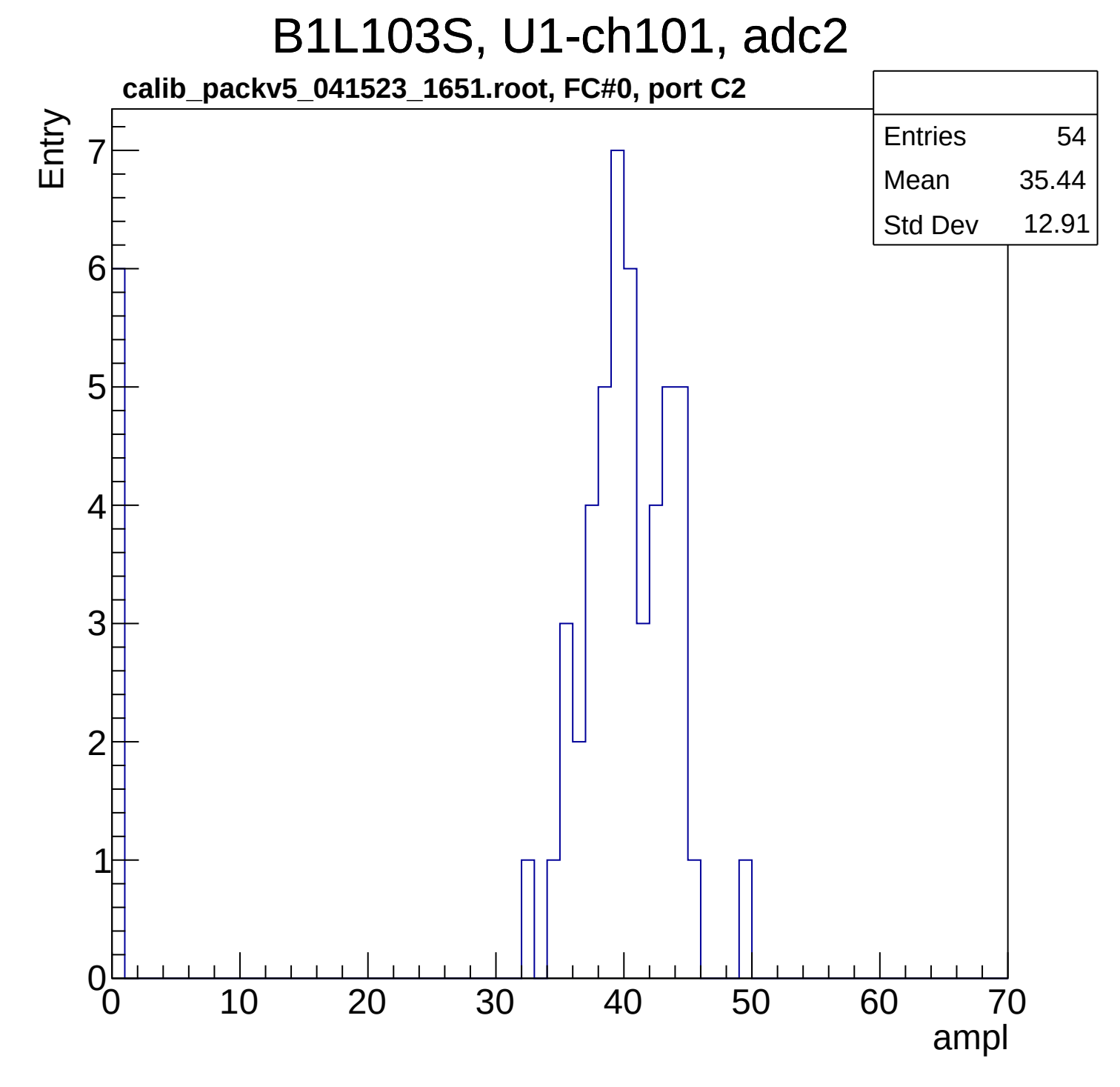
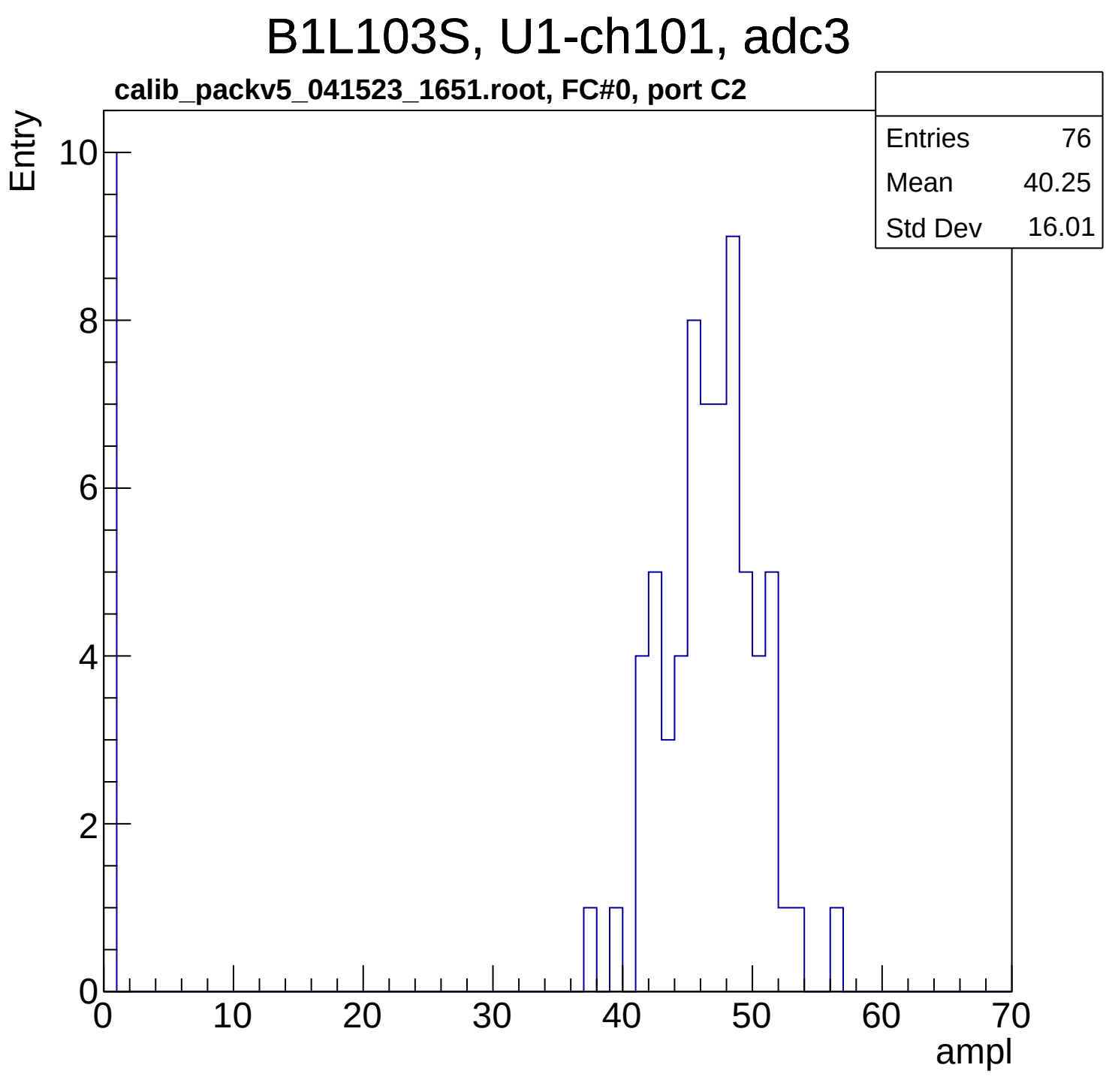
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

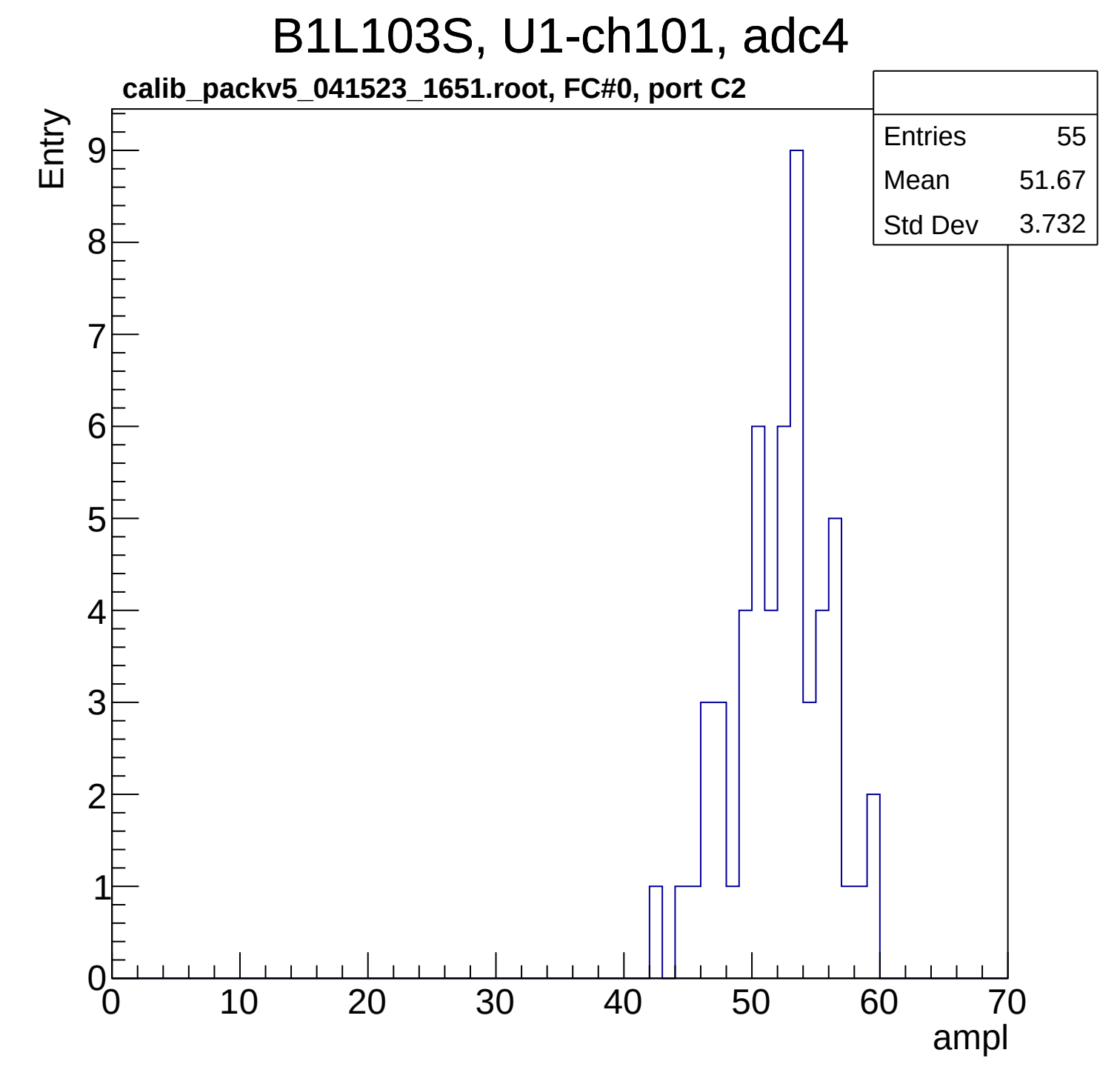

B1L103S, U1-ch100, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 8.5
Std Dev 21.39
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch101, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 88
Mean 19.85
Std Dev 13.27
Entry
0
5
10
15
20
25
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch101, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 33.39
Std Dev 6.845
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U1-ch101, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 35.44
Std Dev 12.91
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U1-ch101, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 40.25
Std Dev 16.01
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U1-ch101, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 51.67
Std Dev 3.732
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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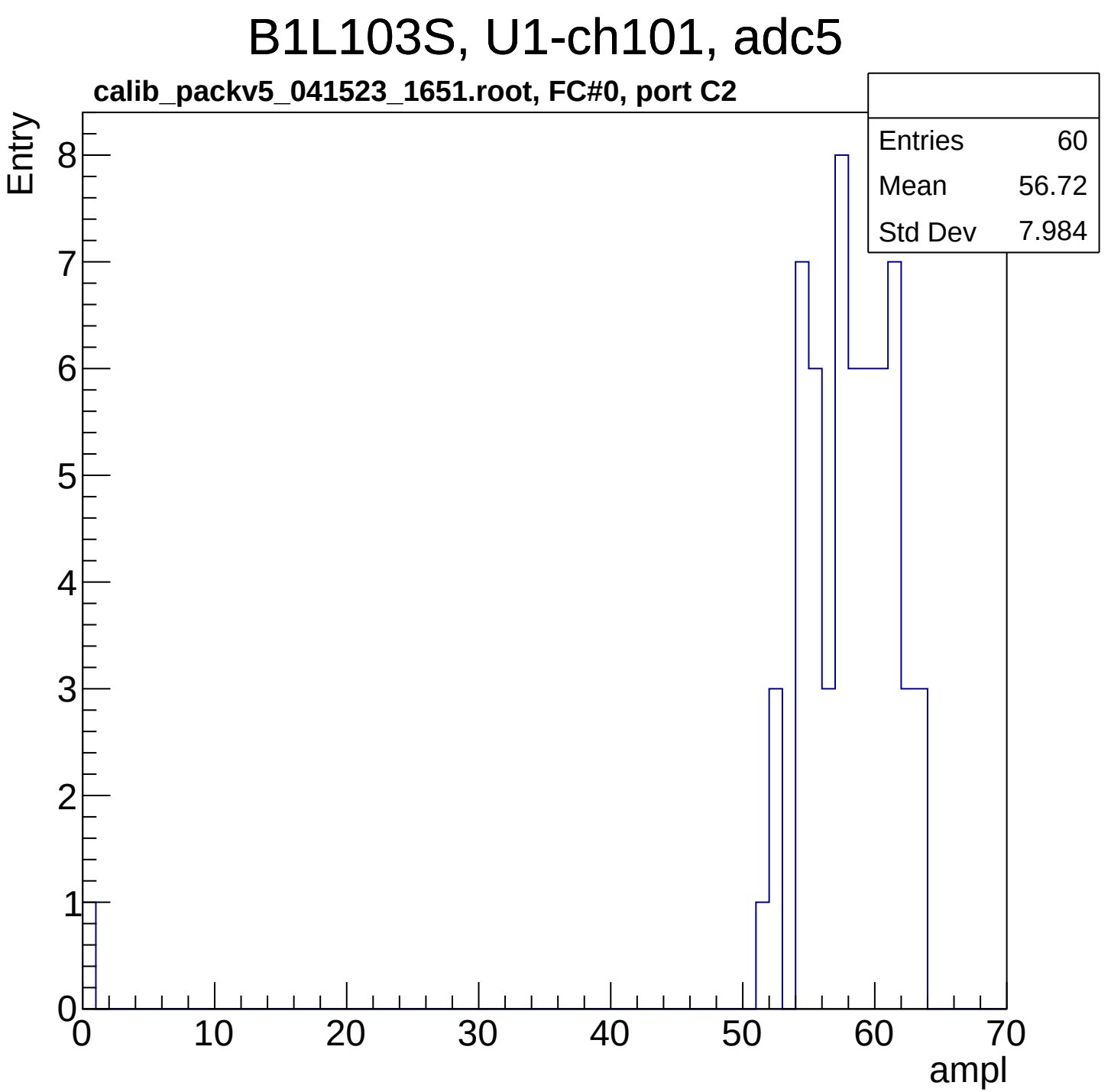
B1L103S, U1-ch101, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 56.72
Std Dev 7.984
Entry
ampl
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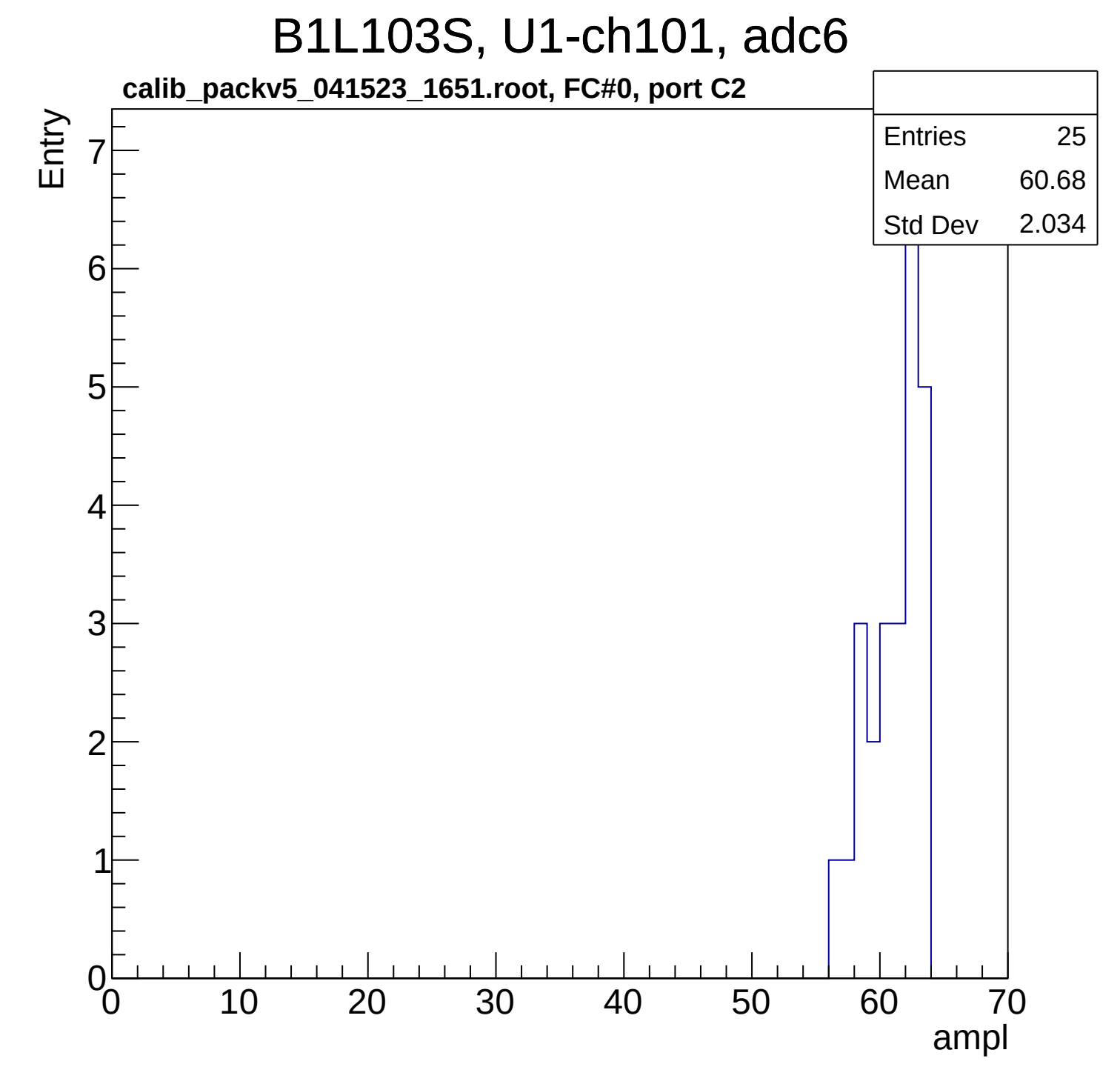
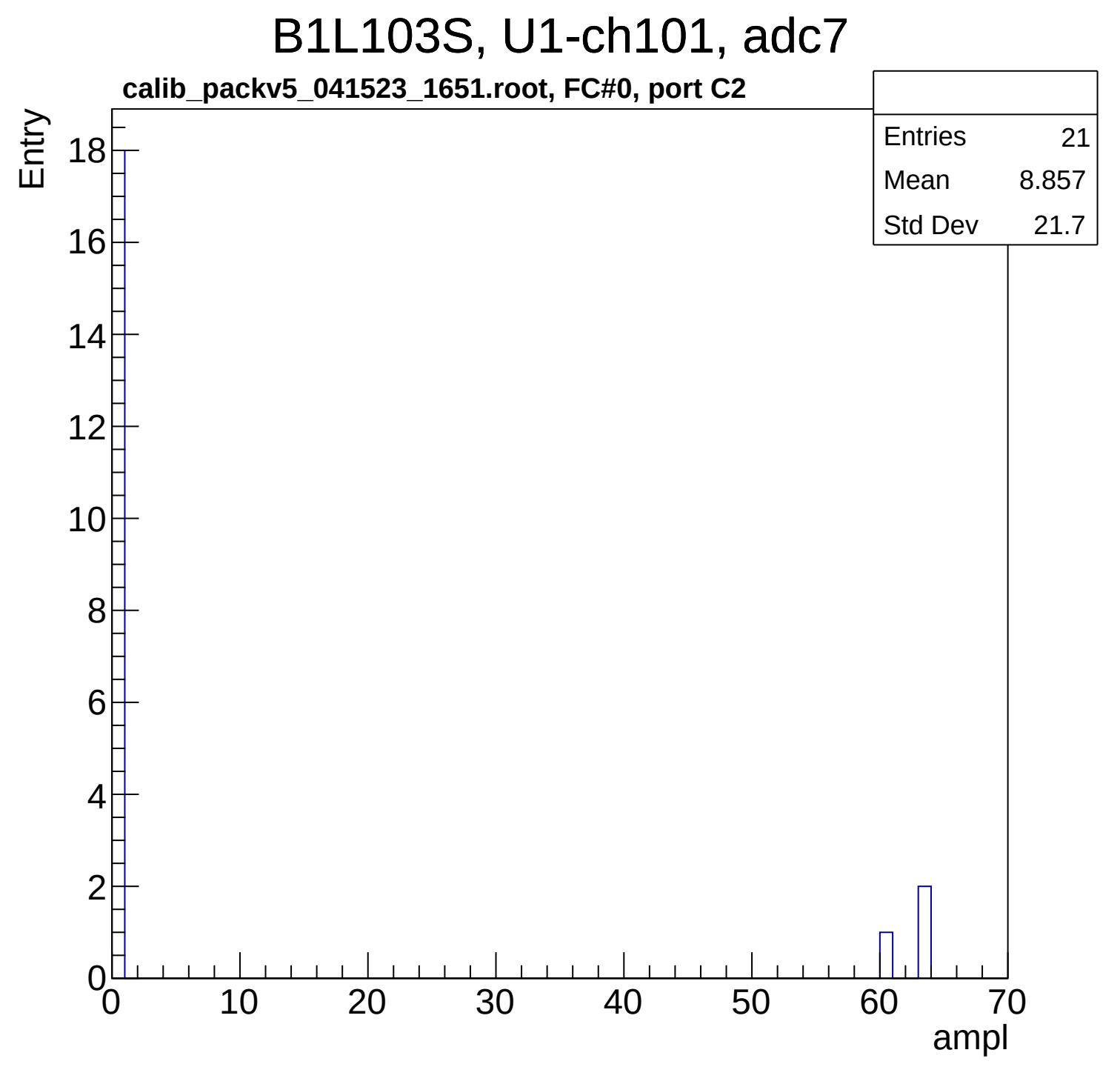
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U1-ch101, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 25
Mean 60.68
Std Dev 2.034
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U1-ch101, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 8.857
Std Dev 21.7
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
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60
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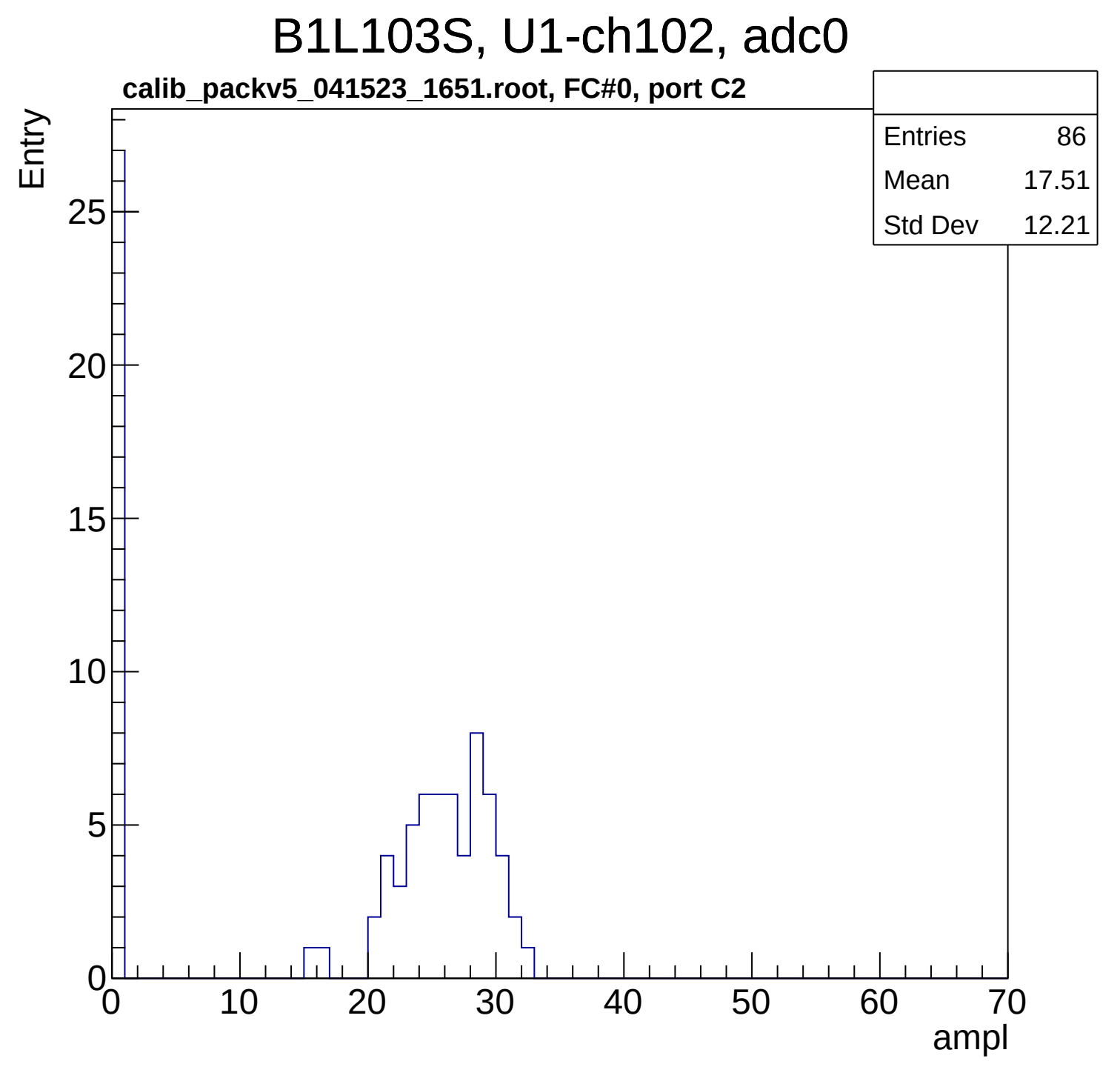
B1L103S, U1-ch102, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 17.51
Std Dev 12.21
Entry
ampl
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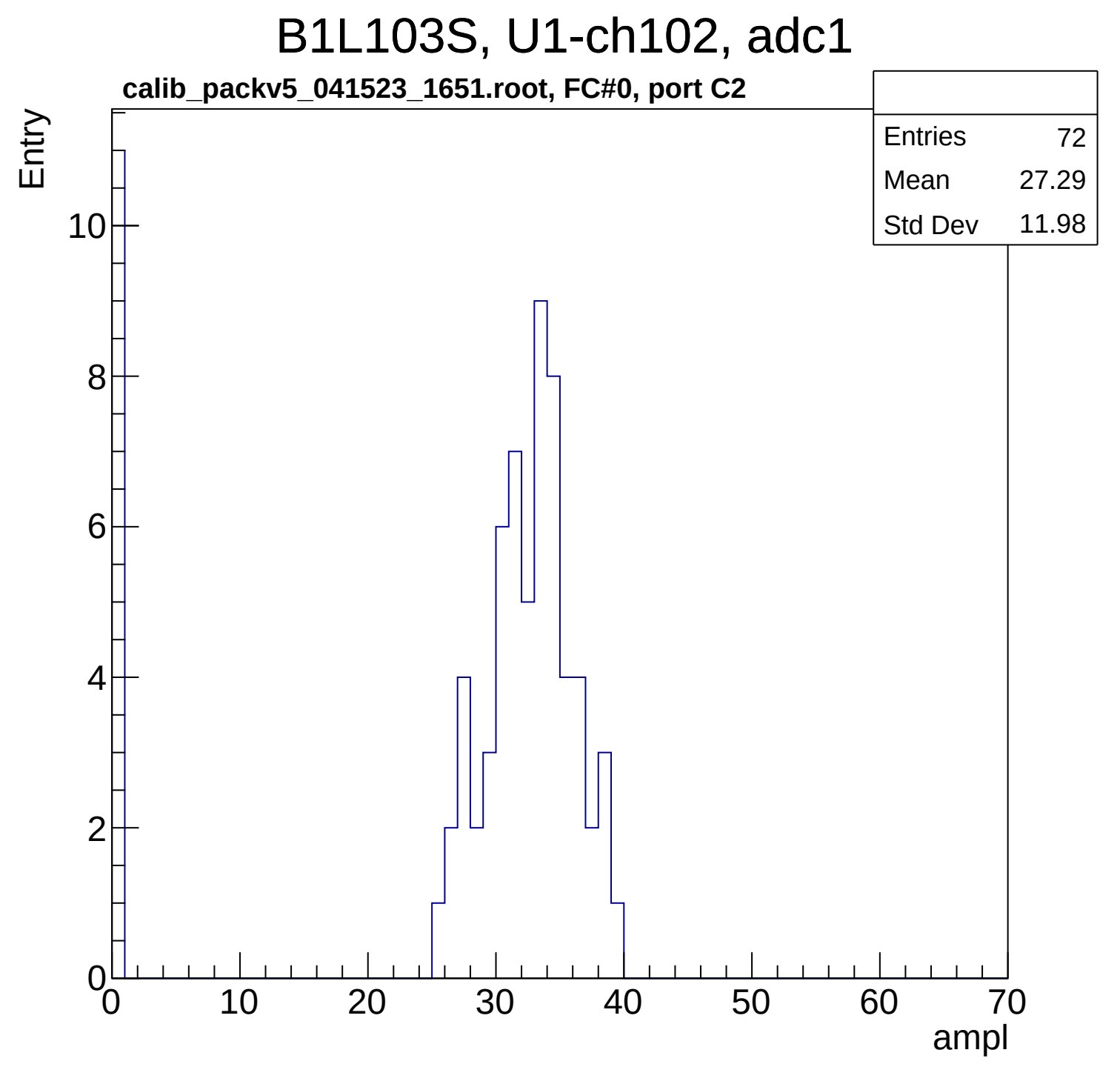
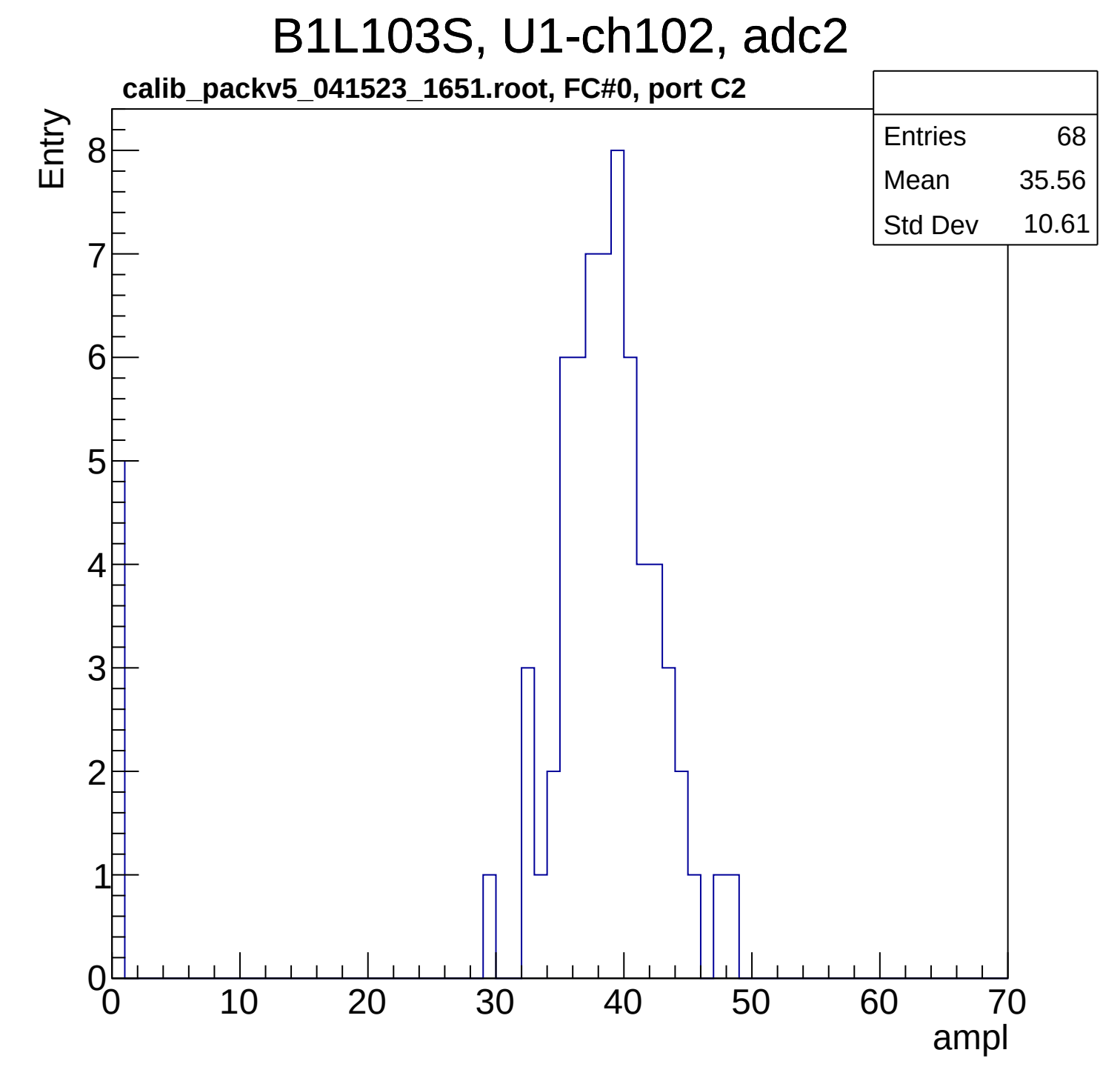
5
10
15
20
25
0
10
20
30
40
50
60
70


B1L103S, U1-ch102, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 27.29
Std Dev 11.98
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch102, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 35.56
Std Dev 10.61
Entry
ampl
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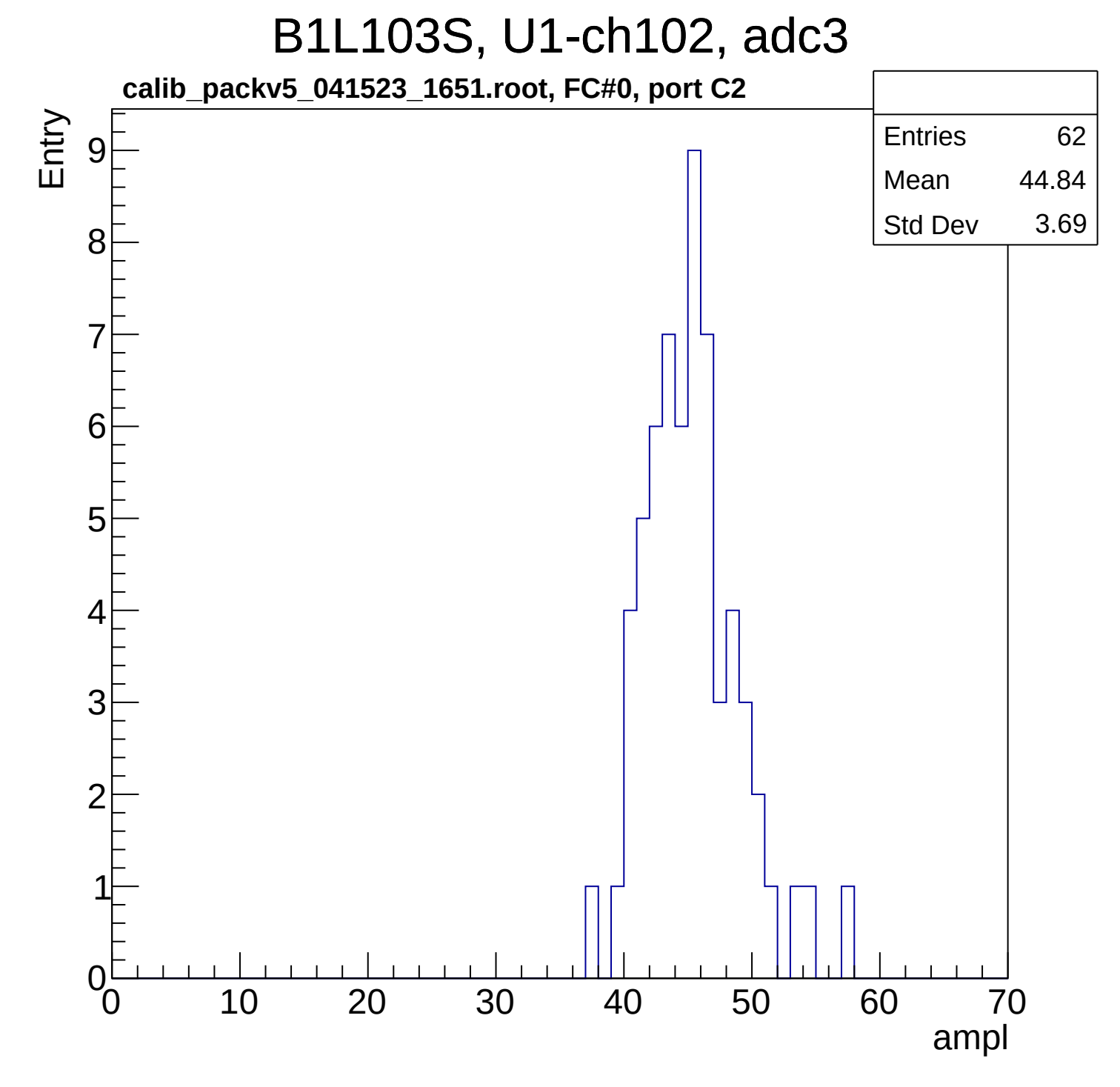
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U1-ch102, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 44.84
Std Dev 3.69
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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40
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60
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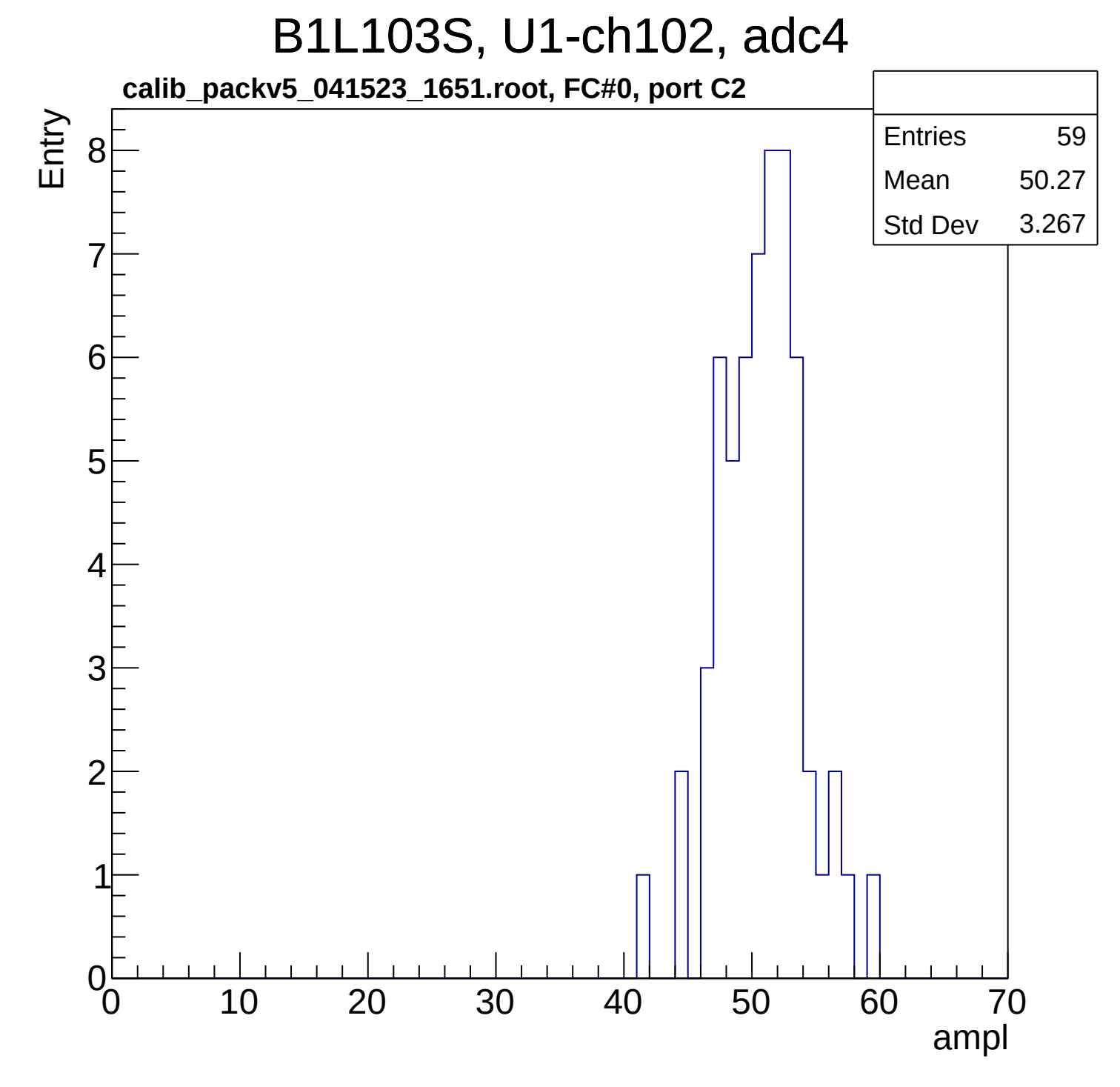
B1L103S, U1-ch102, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 50.27
Std Dev 3.267
Entry
ampl
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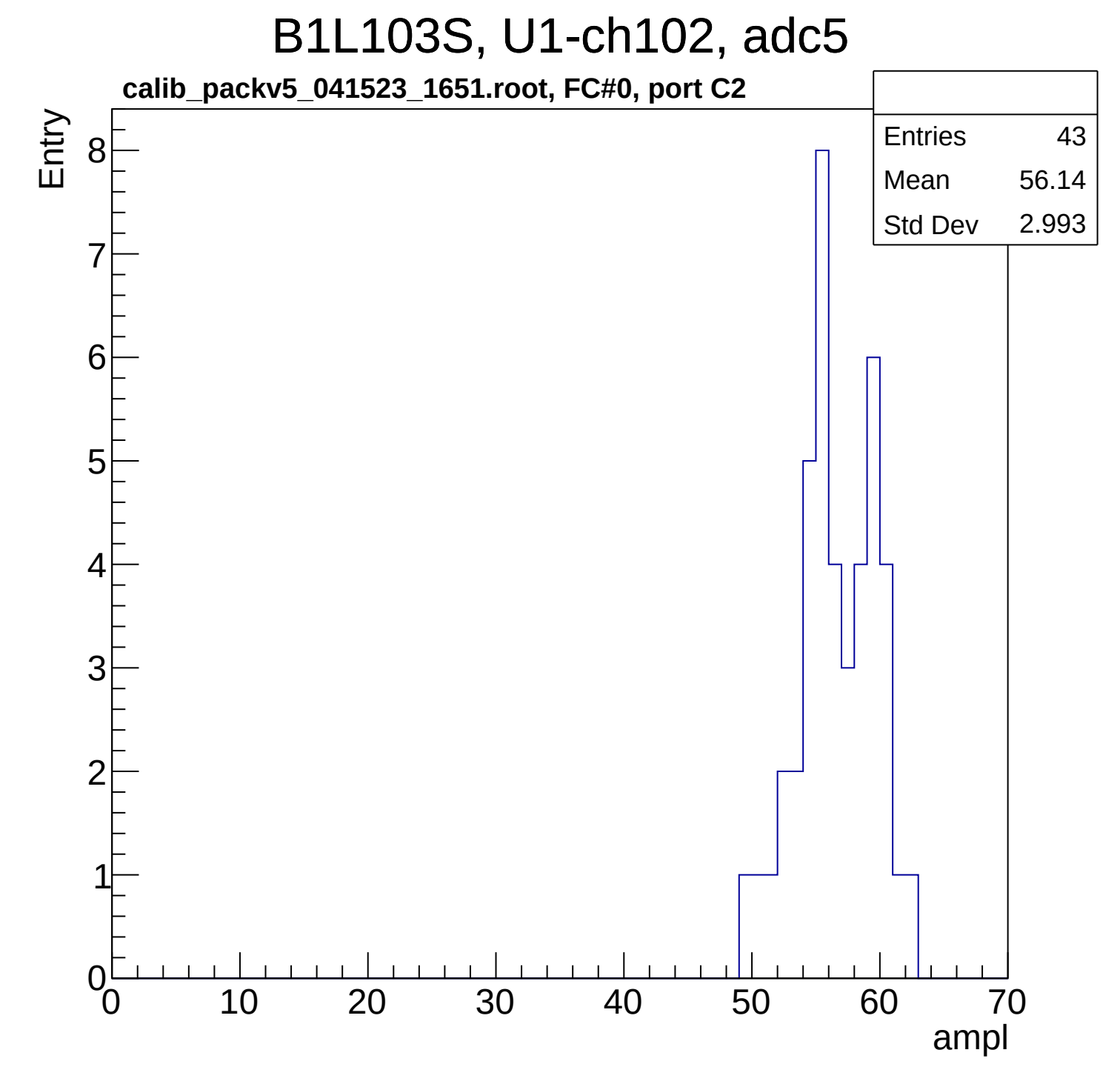
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U1-ch102, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 43
Mean 56.14
Std Dev 2.993
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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40
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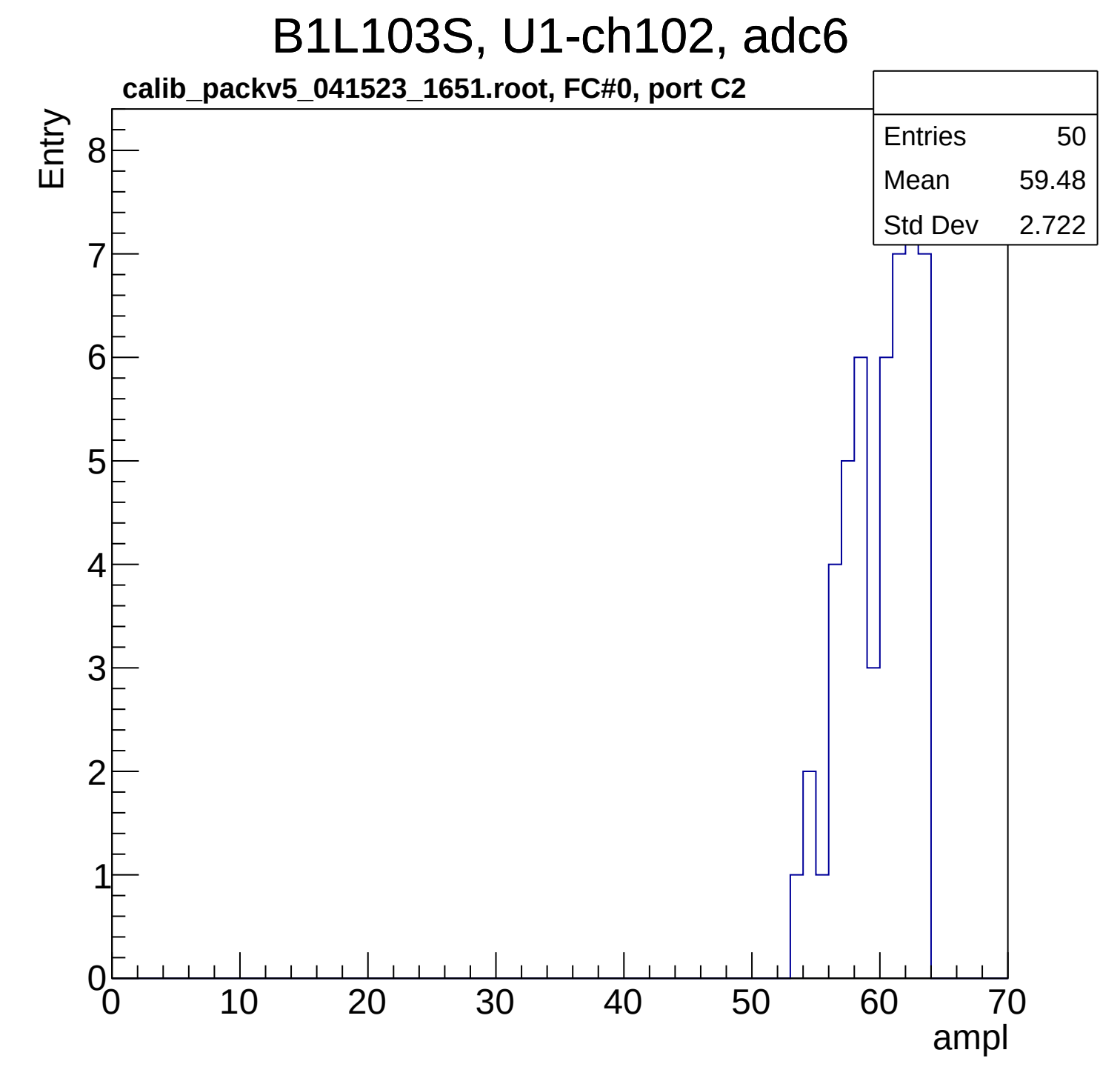
60
70


B1L103S, U1-ch102, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 59.48
Std Dev 2.722
Entry
ampl
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2
3
4
5
6
7
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0
10
20
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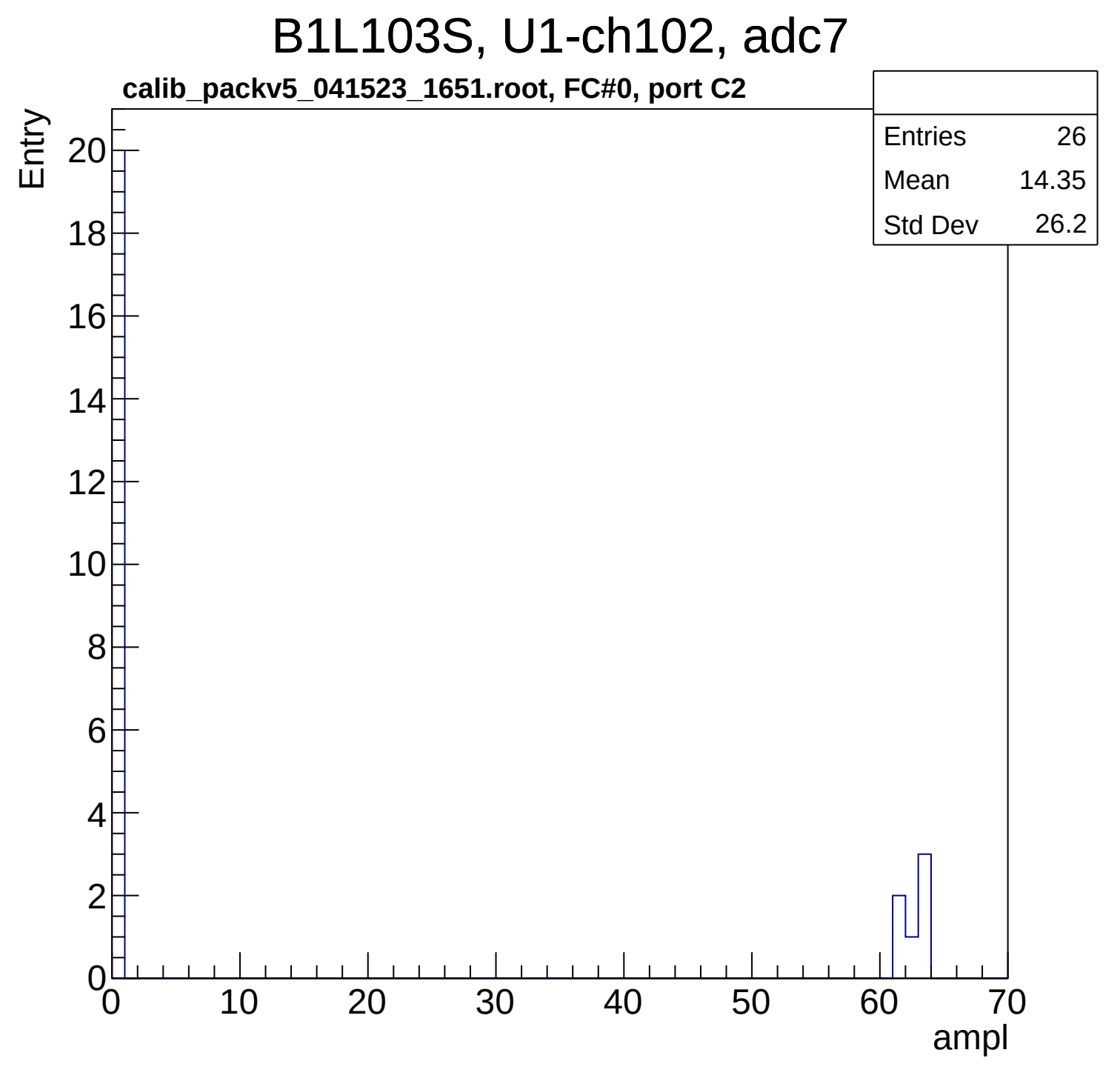
40
50
60
70


B1L103S, U1-ch102, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 26
Mean 14.35
Std Dev 26.2
Entry
ampl
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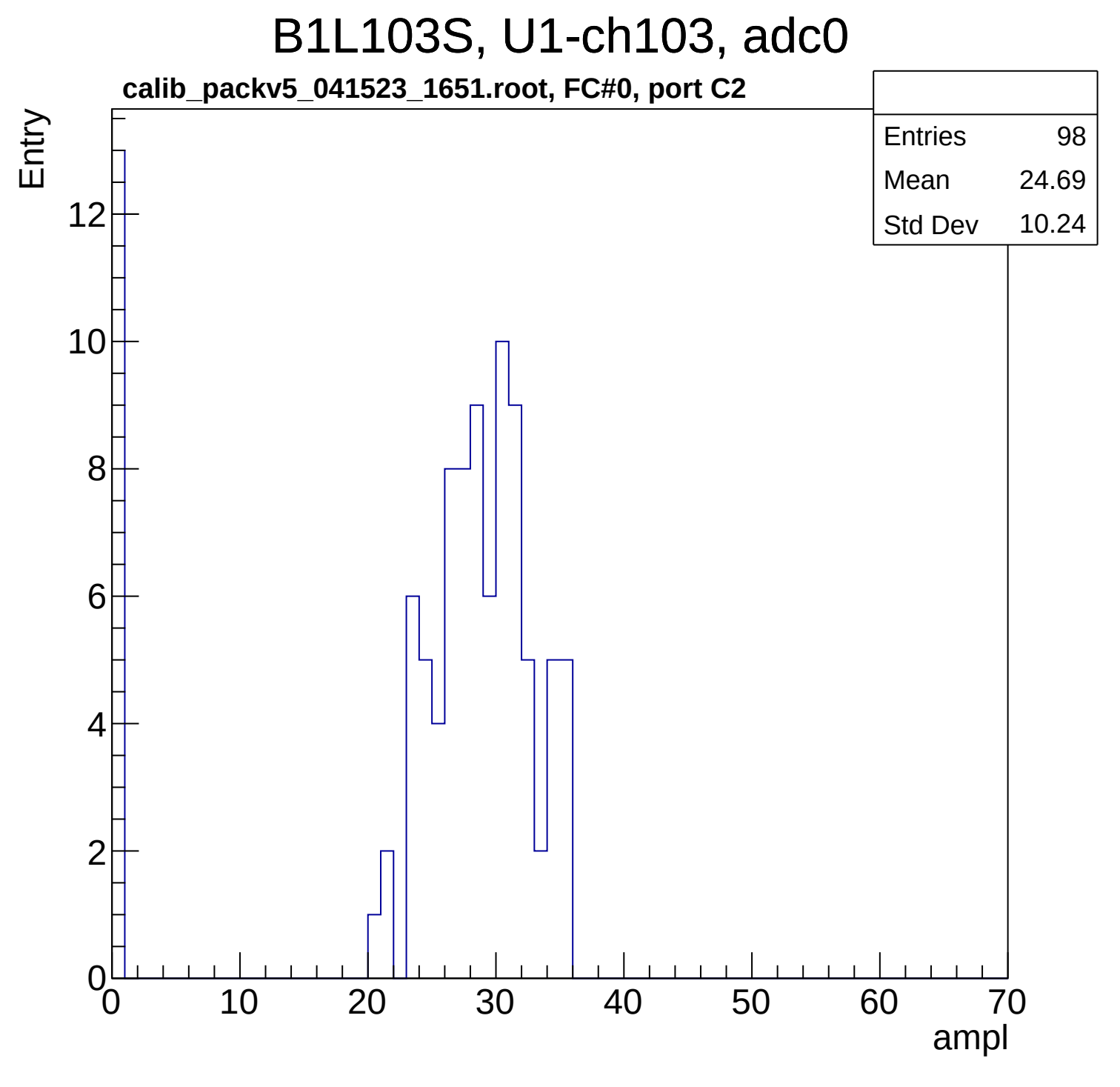
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70


B1L103S, U1-ch103, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 98
Mean 24.69
Std Dev 10.24
Entry
ampl
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8
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0
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20
30
40
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60
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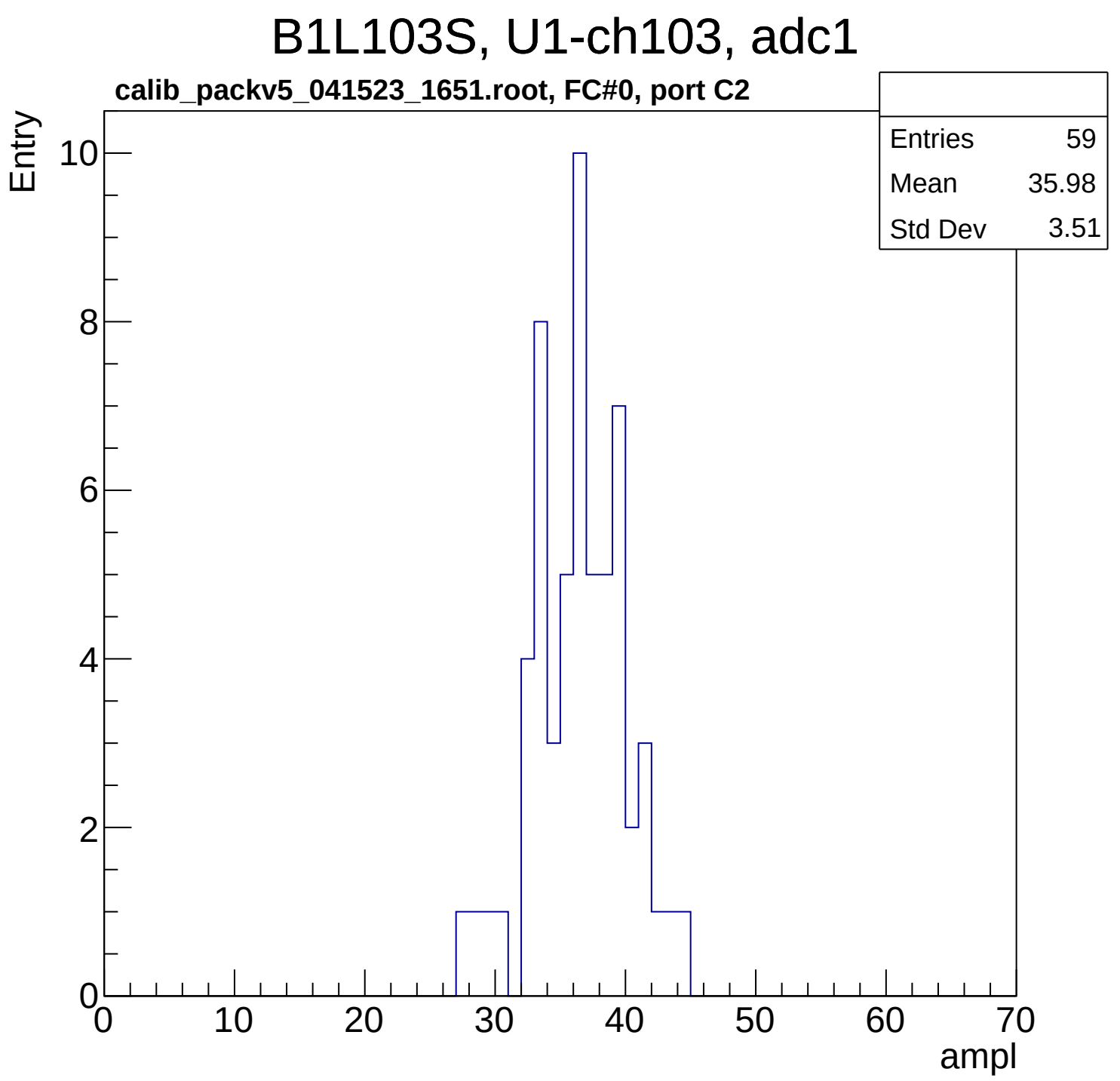
B1L103S, U1-ch103, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 35.98
Std Dev 3.51
Entry
ampl
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2
4
6
8
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0
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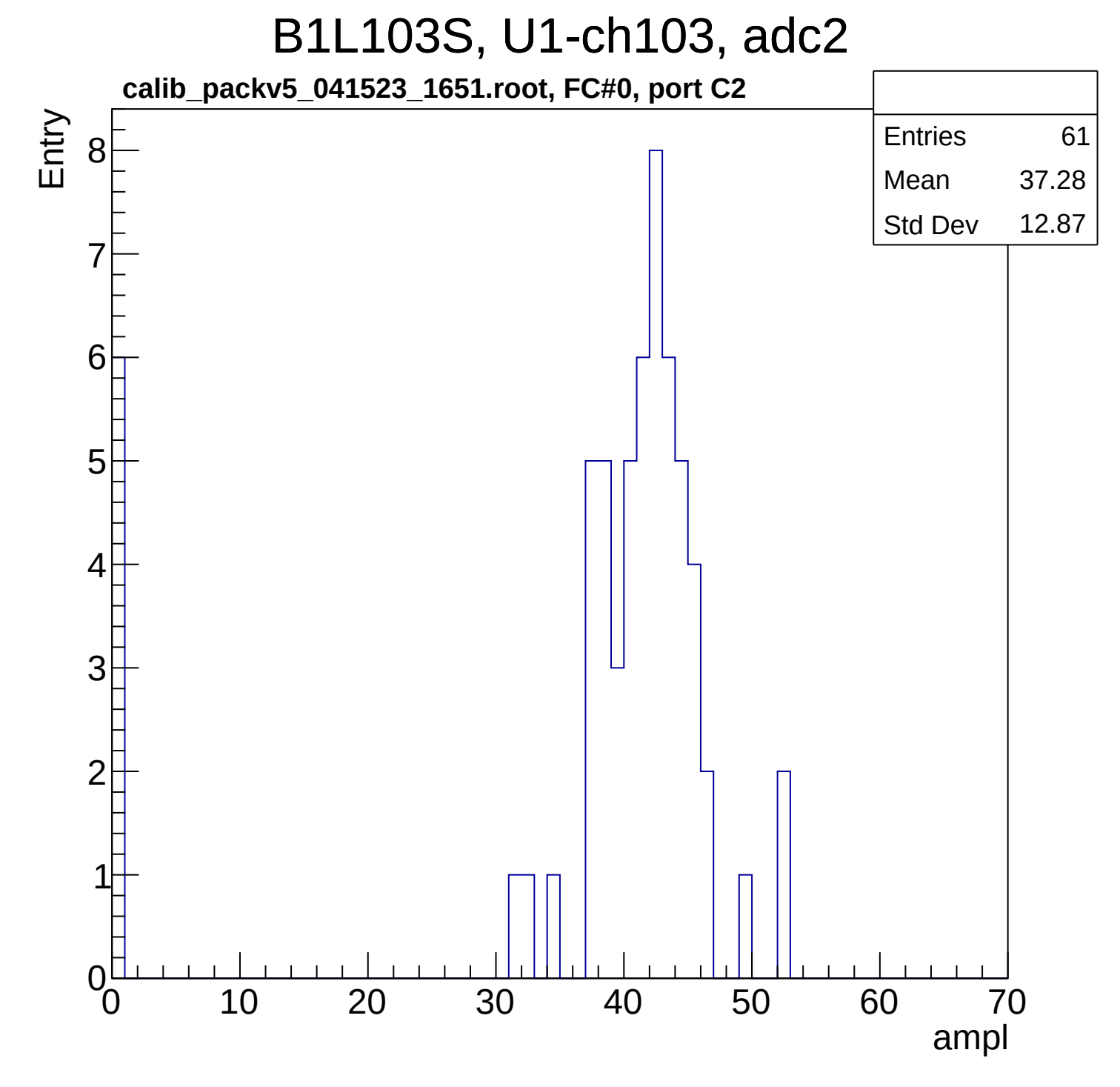
B1L103S, U1-ch103, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 37.28
Std Dev 12.87
Entry
ampl
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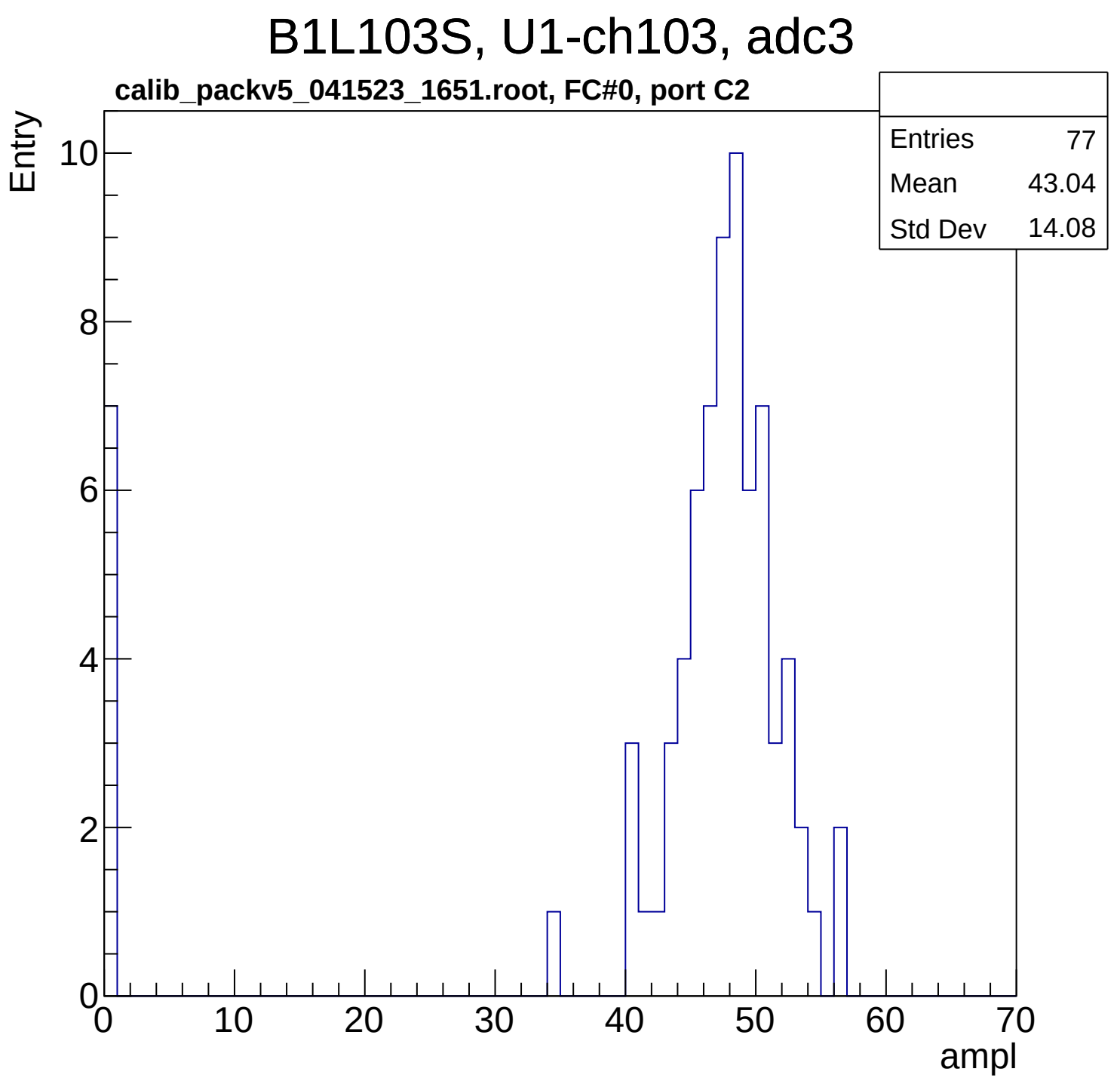
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U1-ch103, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 43.04
Std Dev 14.08
Entry
ampl
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4
6
8
10
0
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20
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50
60
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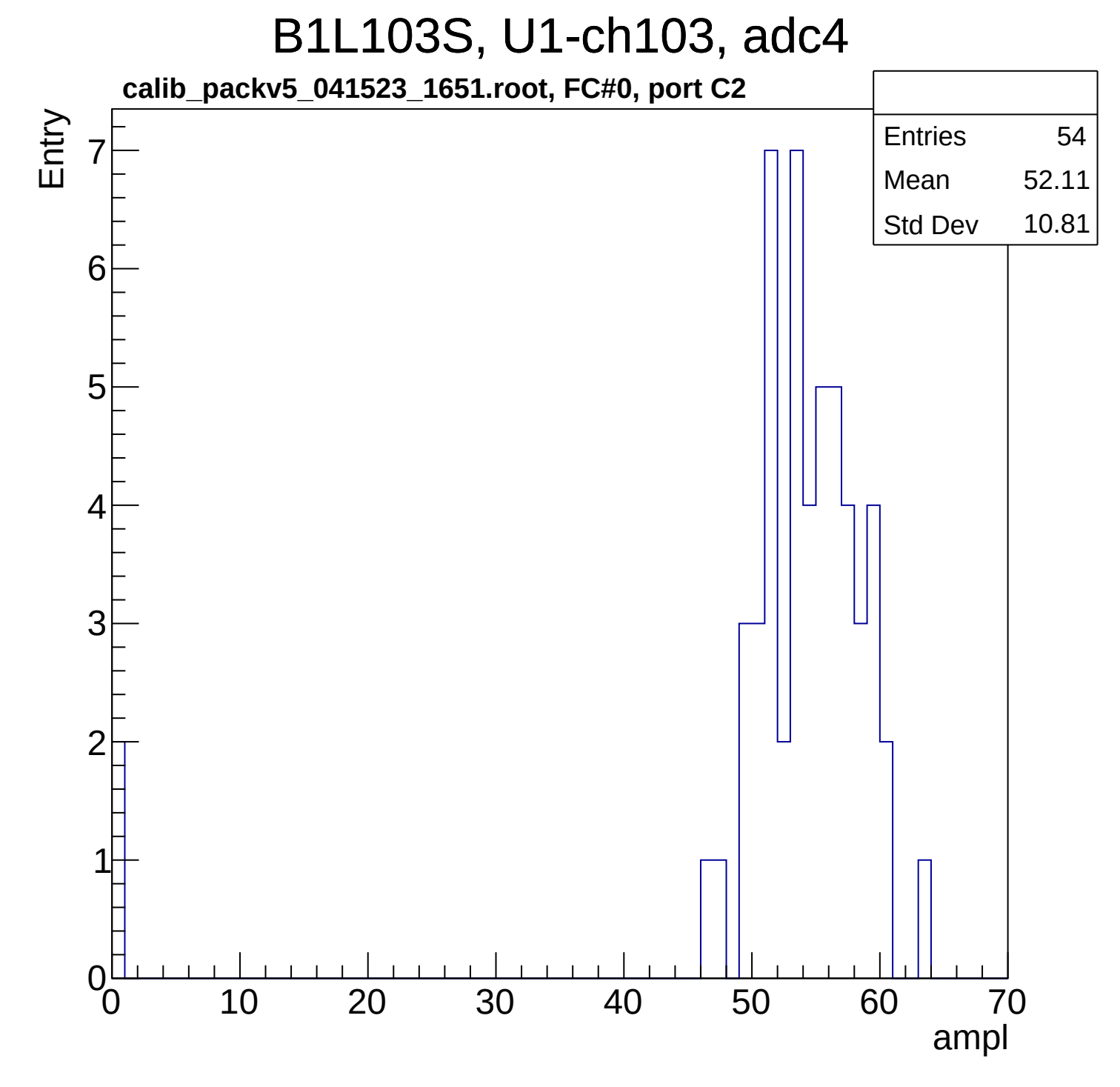
B1L103S, U1-ch103, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 52.11
Std Dev 10.81
Entry
ampl
0
1
2
3
4
5
6
7
0
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60
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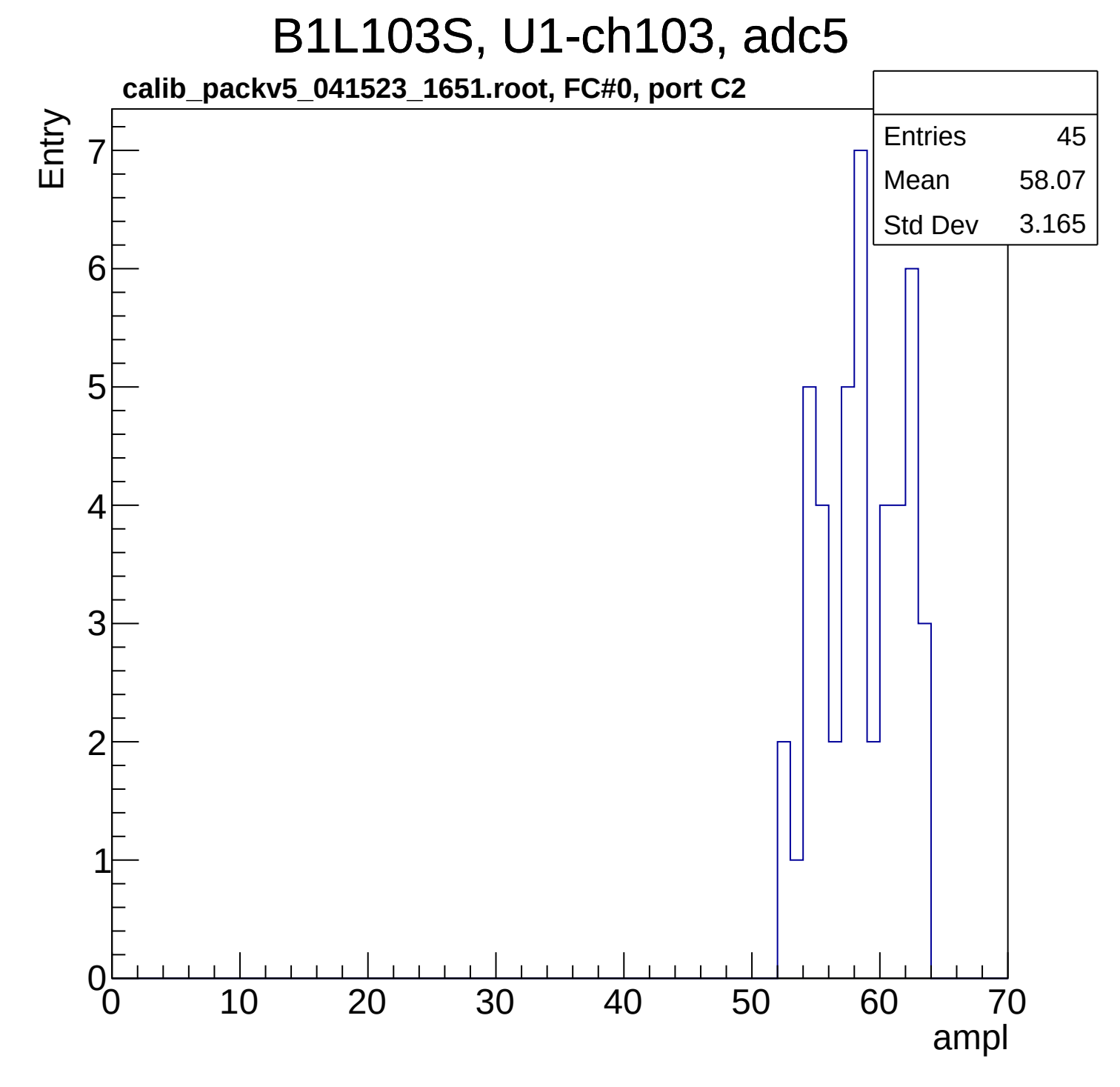
B1L103S, U1-ch103, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 58.07
Std Dev 3.165
Entry
ampl
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4
5
6
7
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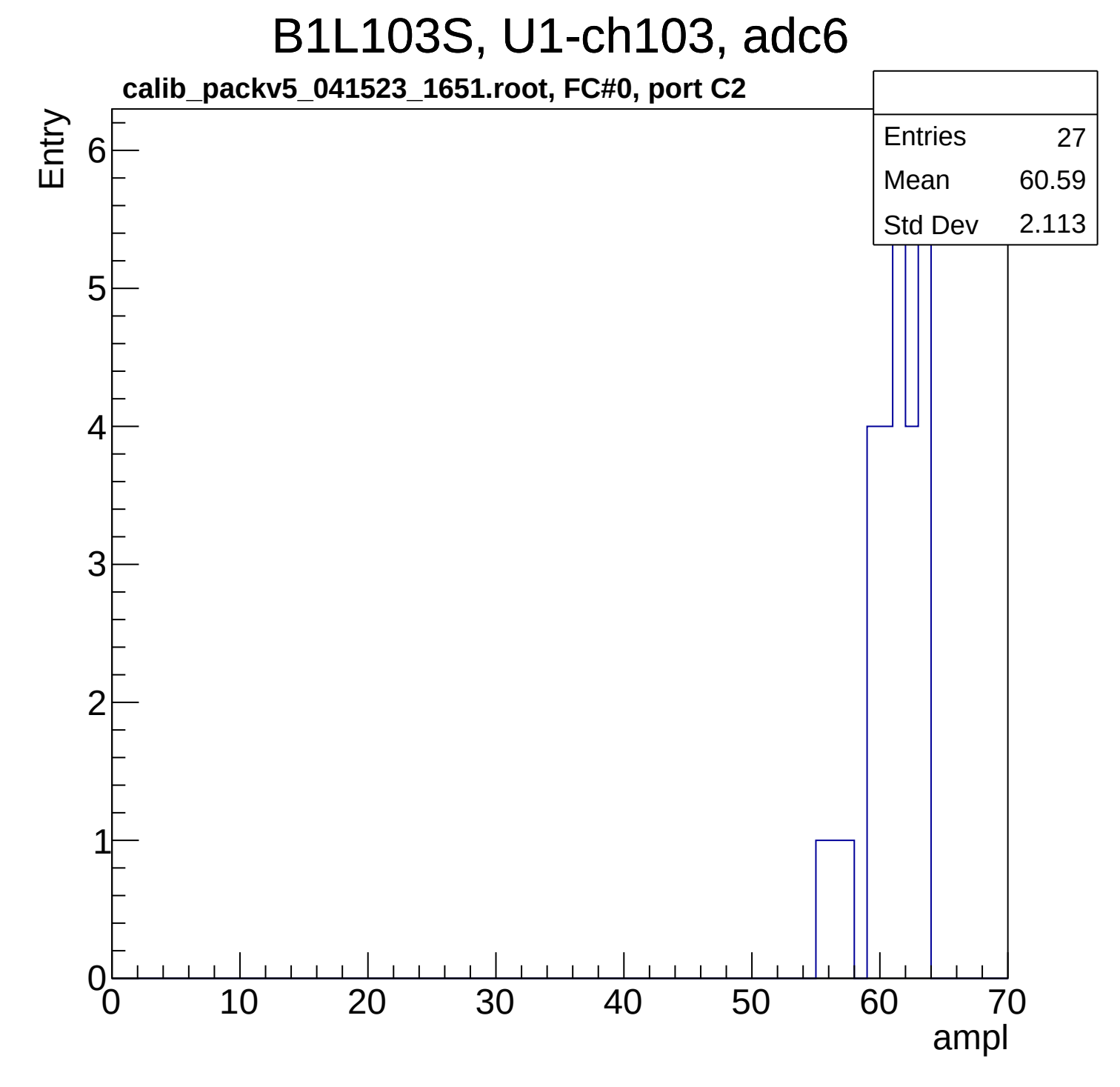
B1L103S, U1-ch103, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 27
Mean 60.59
Std Dev 2.113
Entry
ampl
0
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3
4
5
6
0
10
20
30
40
50
60
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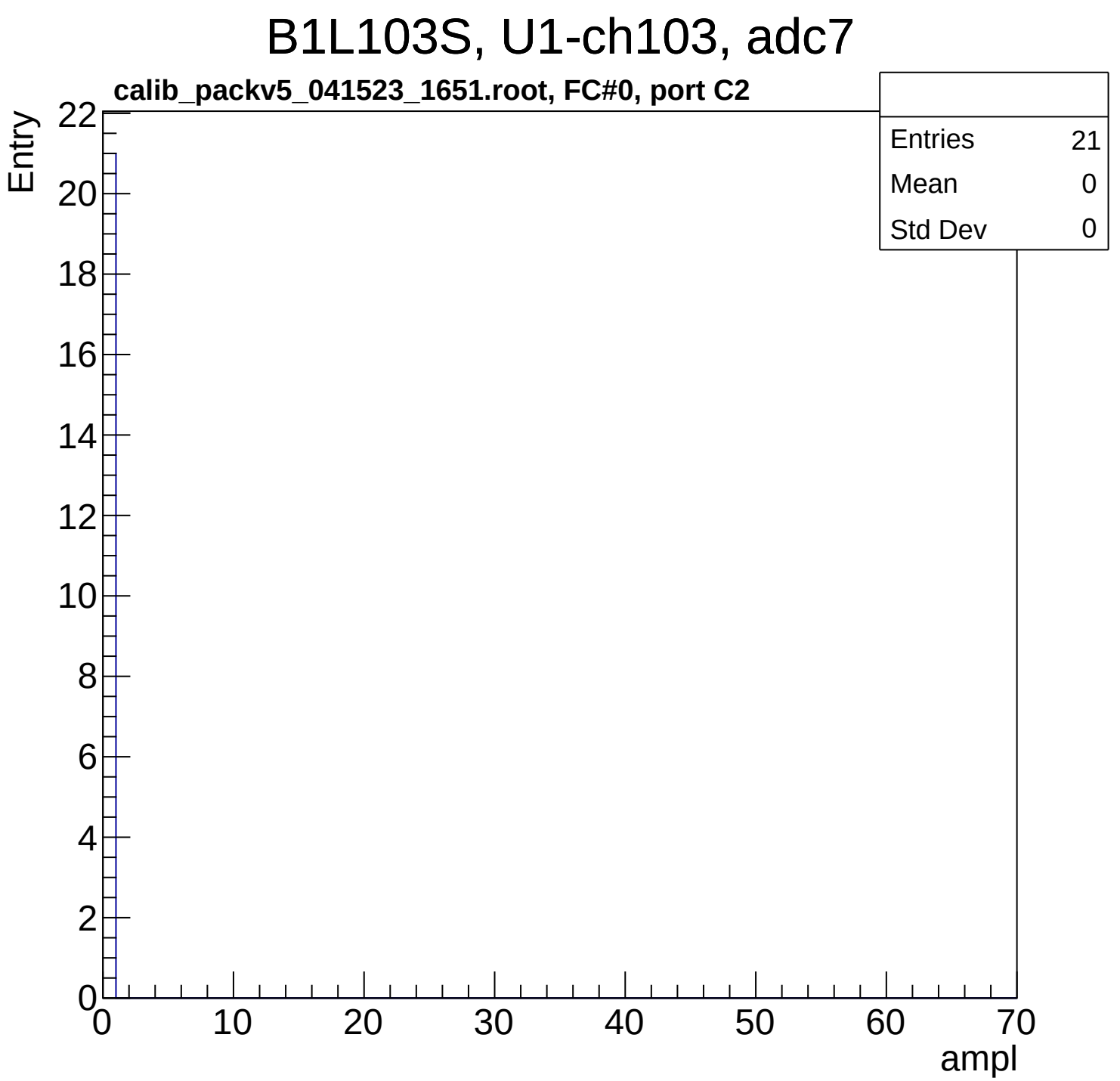
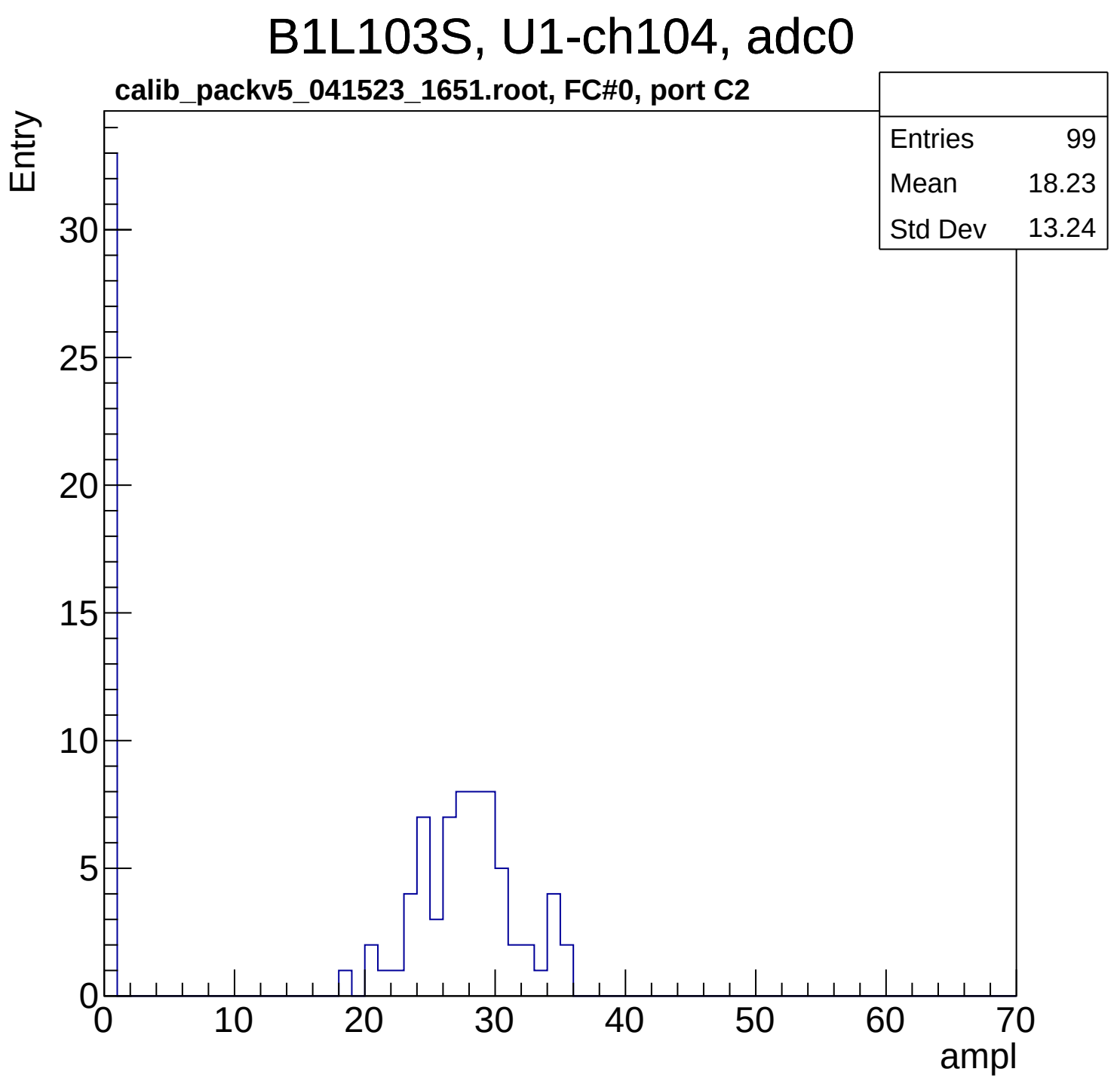

B1L103S, U1-ch103, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 0
Std Dev 0
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
22
0
10
20
30
40
50
60
70


B1L103S, U1-ch104, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 99
Mean 18.23
Std Dev 13.24
Entry
0
5
10
15
20
25
30
0
10
20
30
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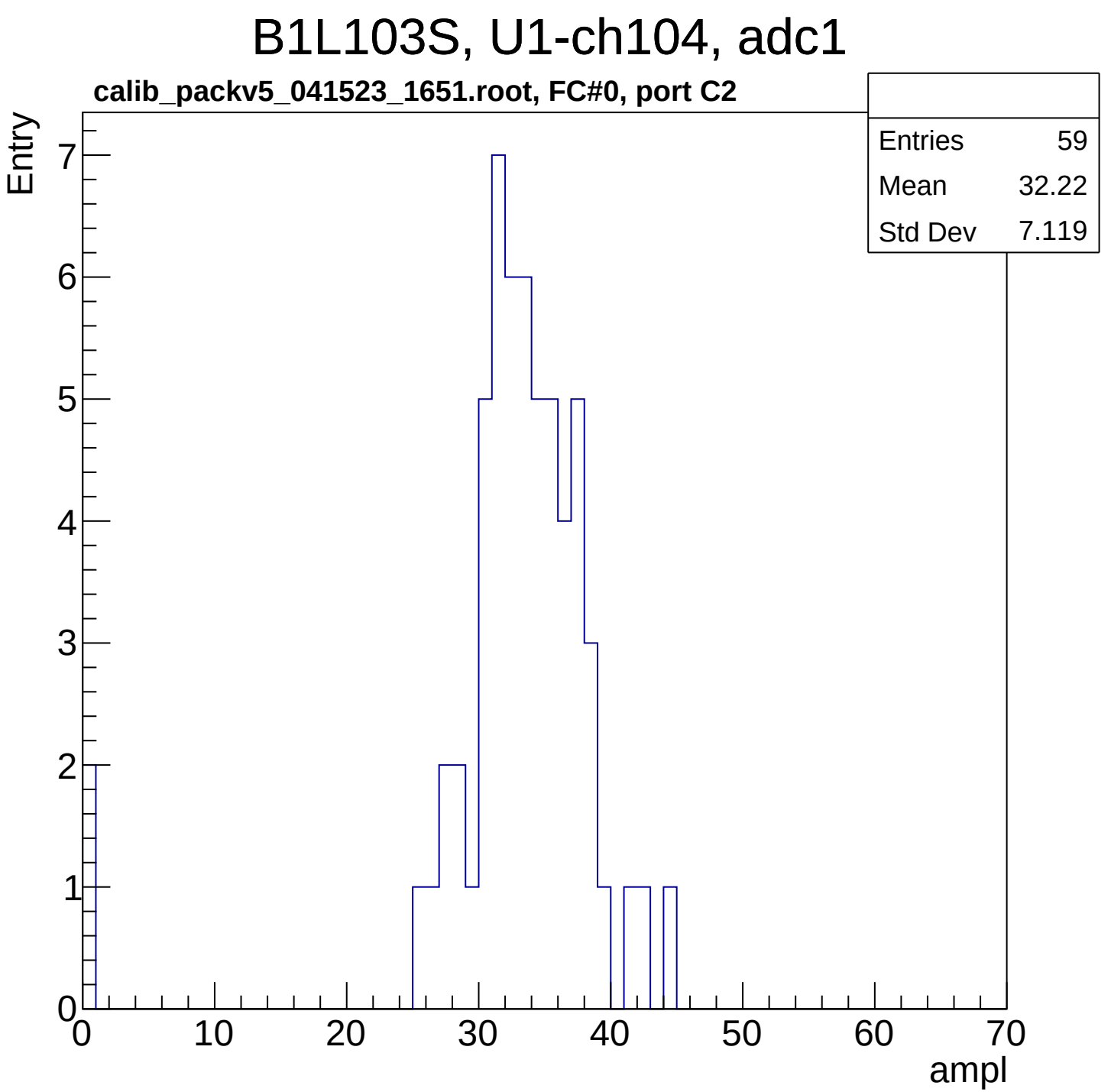
70
ampl


B1L103S, U1-ch104, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 32.22
Std Dev 7.119
Entry
ampl
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1
2
3
4
5
6
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0
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60
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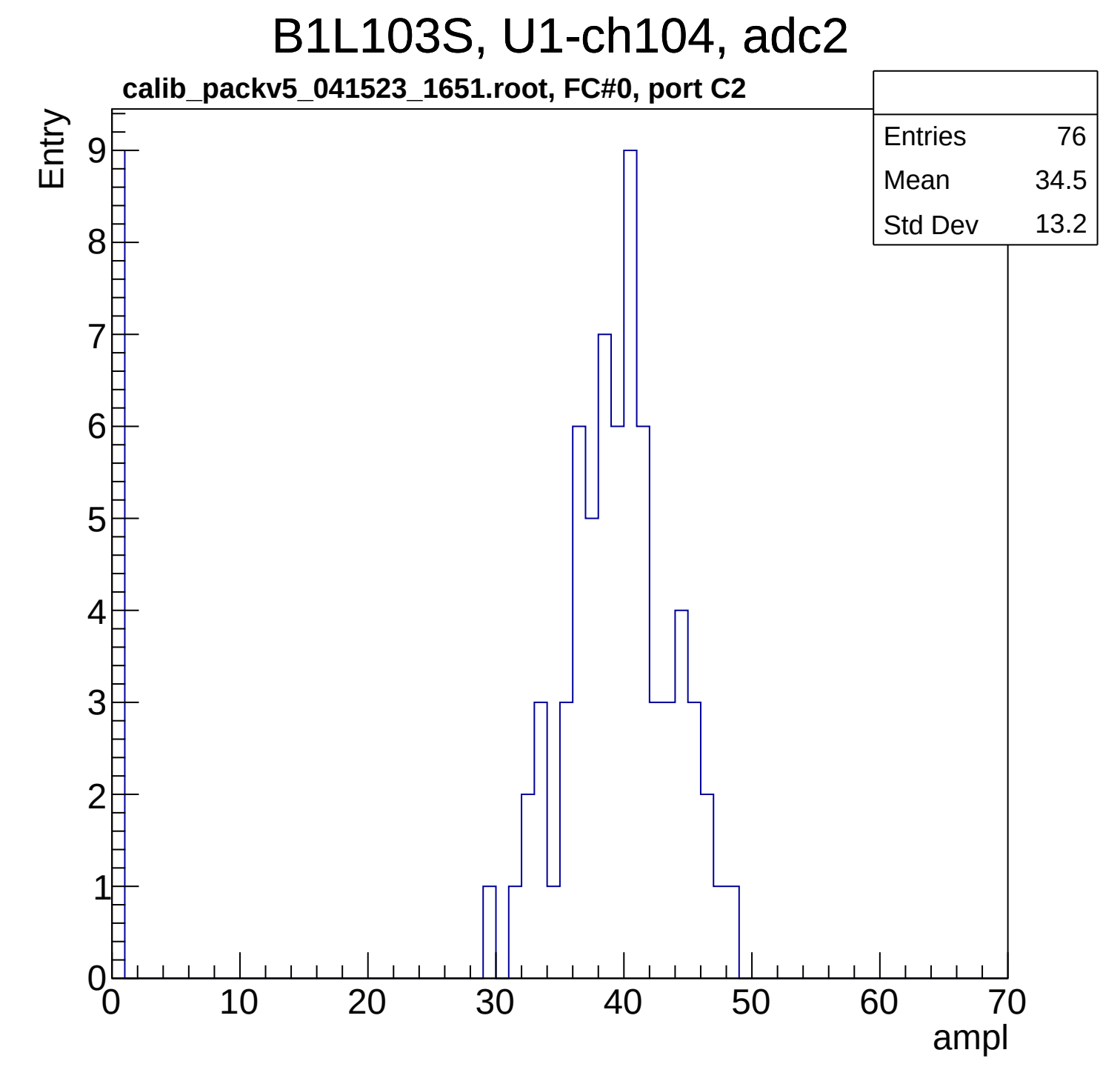
B1L103S, U1-ch104, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 34.5
Std Dev 13.2
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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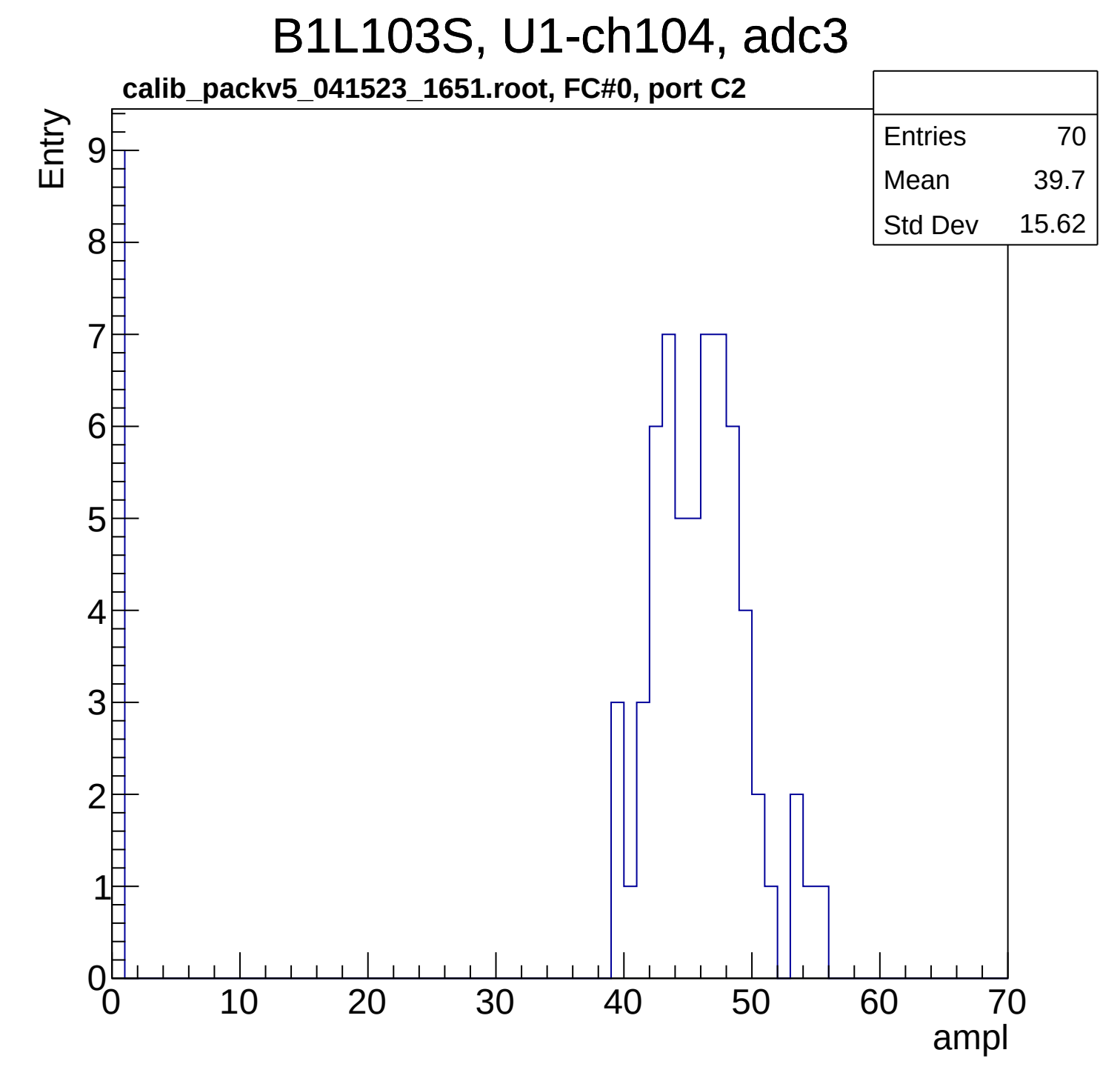
B1L103S, U1-ch104, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 39.7
Std Dev 15.62
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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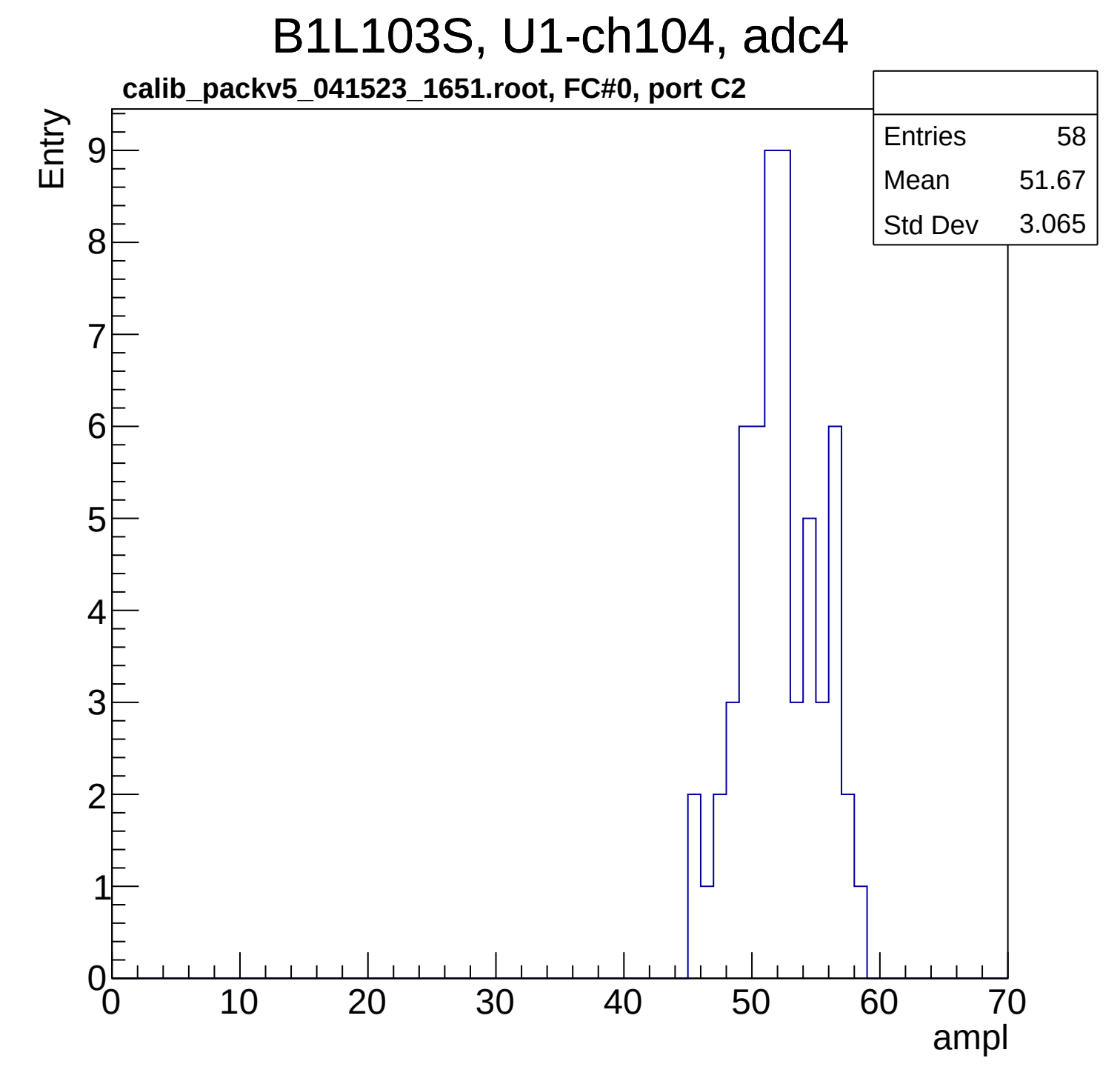
B1L103S, U1-ch104, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 51.67
Std Dev 3.065
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
50
60
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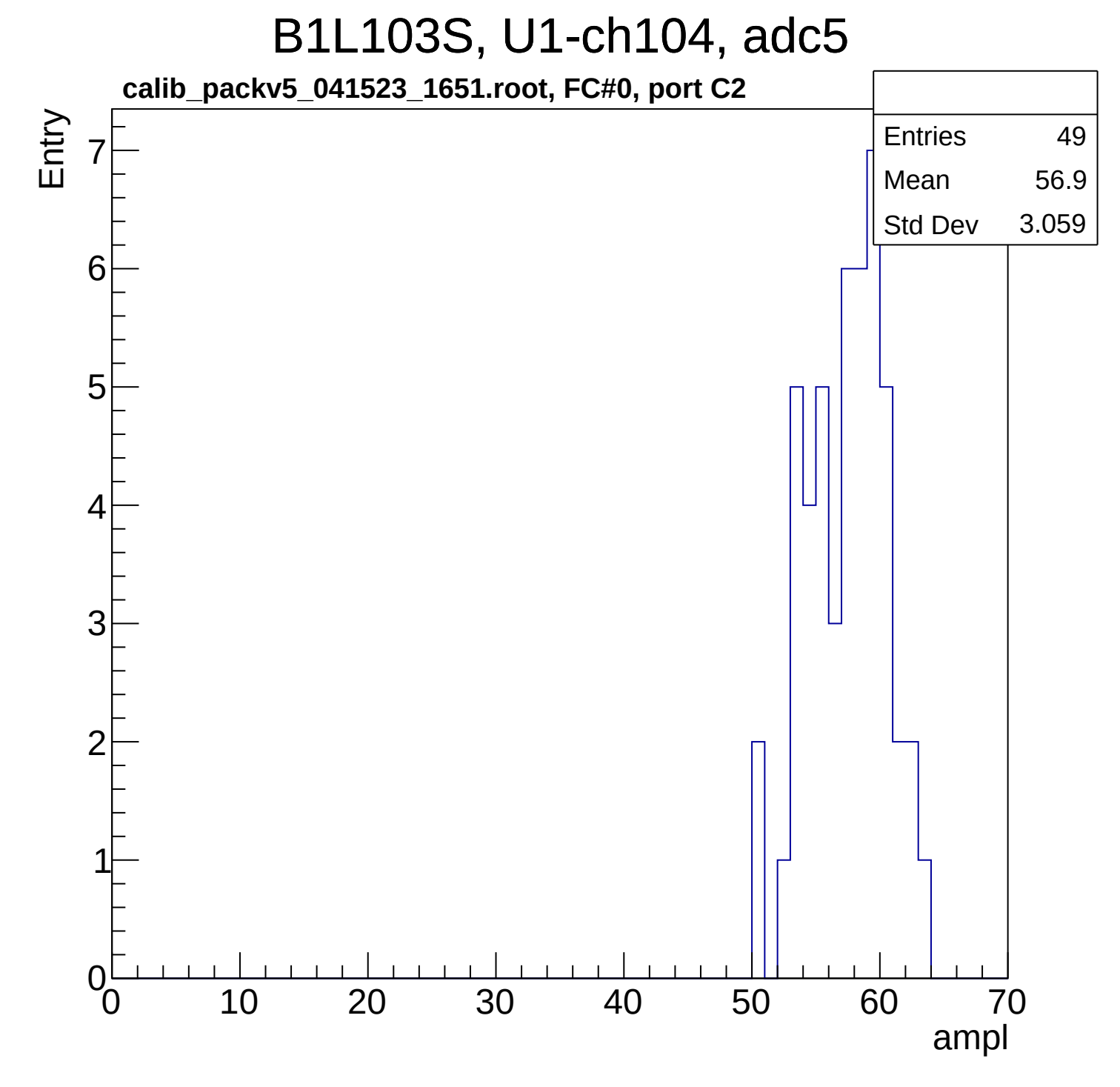
B1L103S, U1-ch104, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 56.9
Std Dev 3.059
Entry
ampl
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2
3
4
5
6
7
0
10
20
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40
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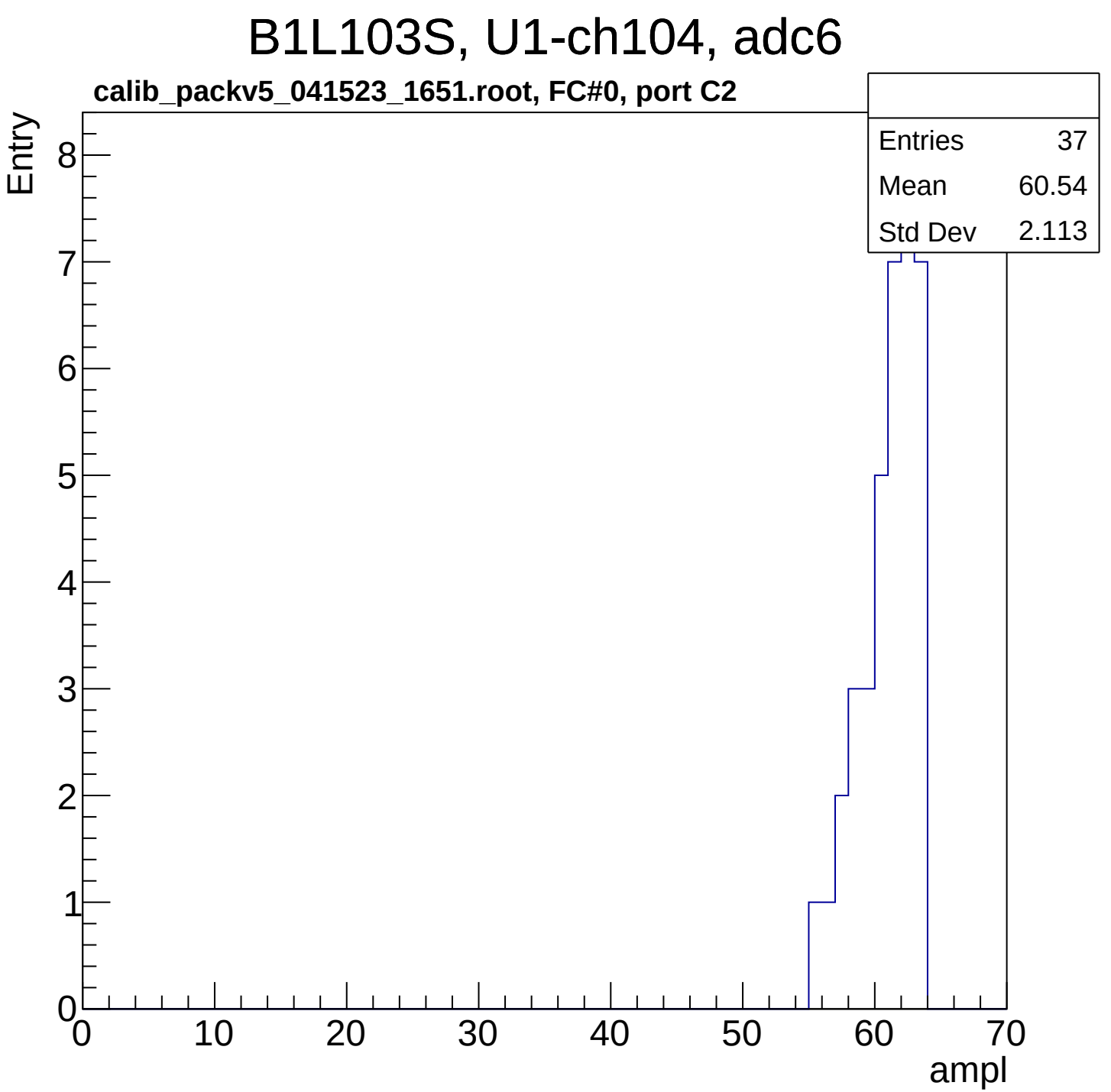
60
70


B1L103S, U1-ch104, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 37
Mean 60.54
Std Dev 2.113
Entry
ampl
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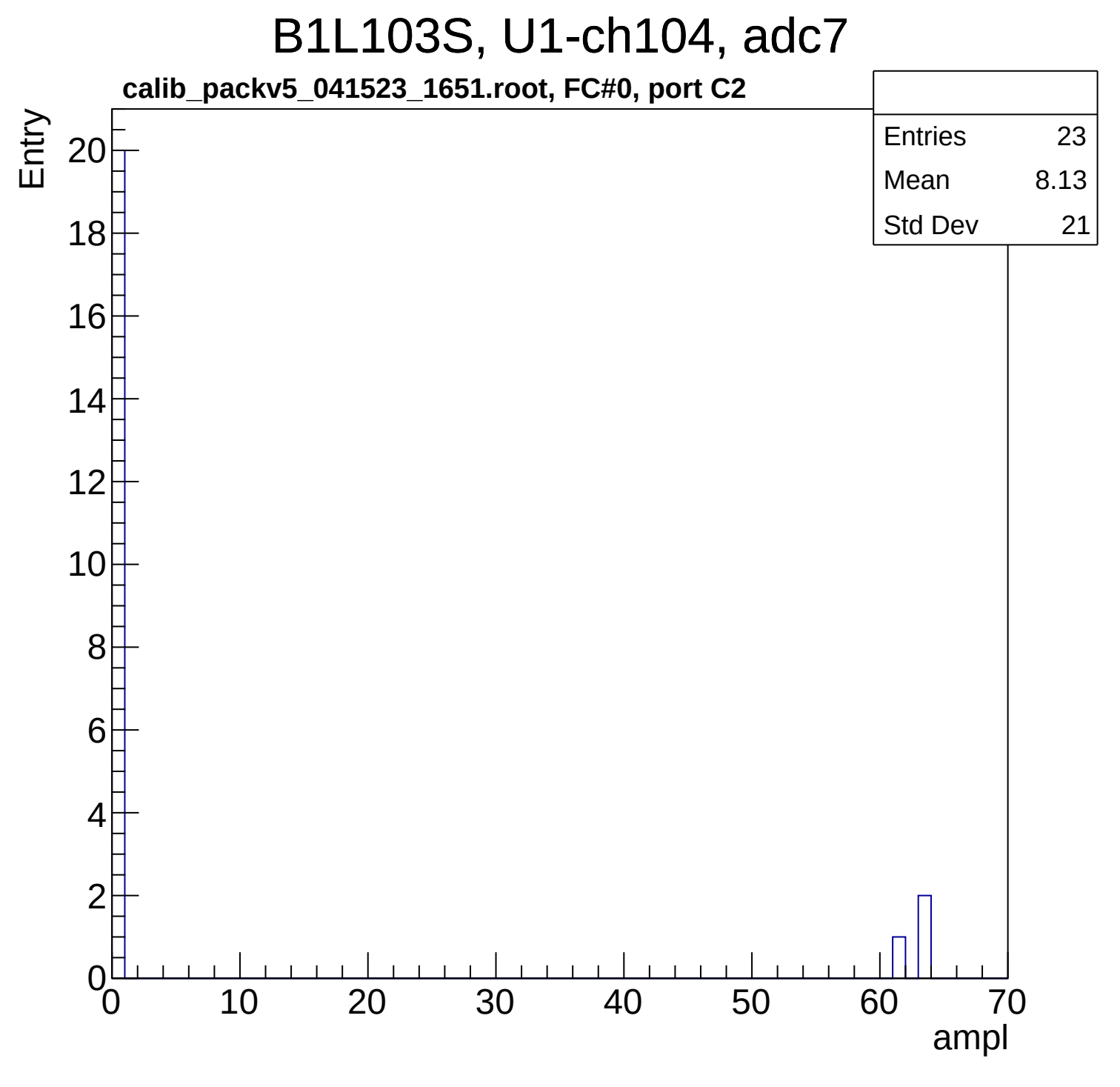
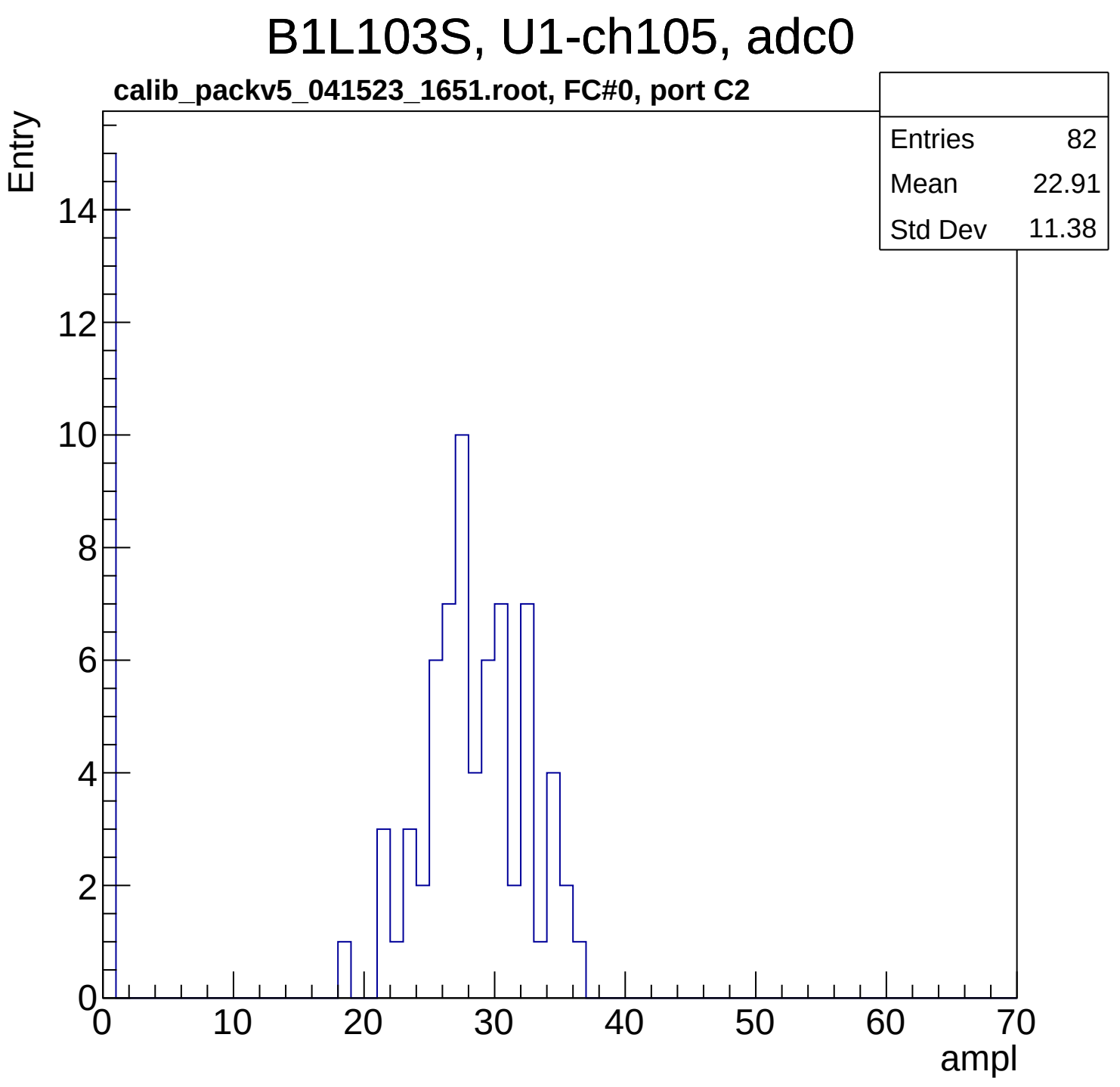
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U1-ch104, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 23
Mean 8.13
Std Dev 21
Entry
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch105, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 22.91
Std Dev 11.38
Entry
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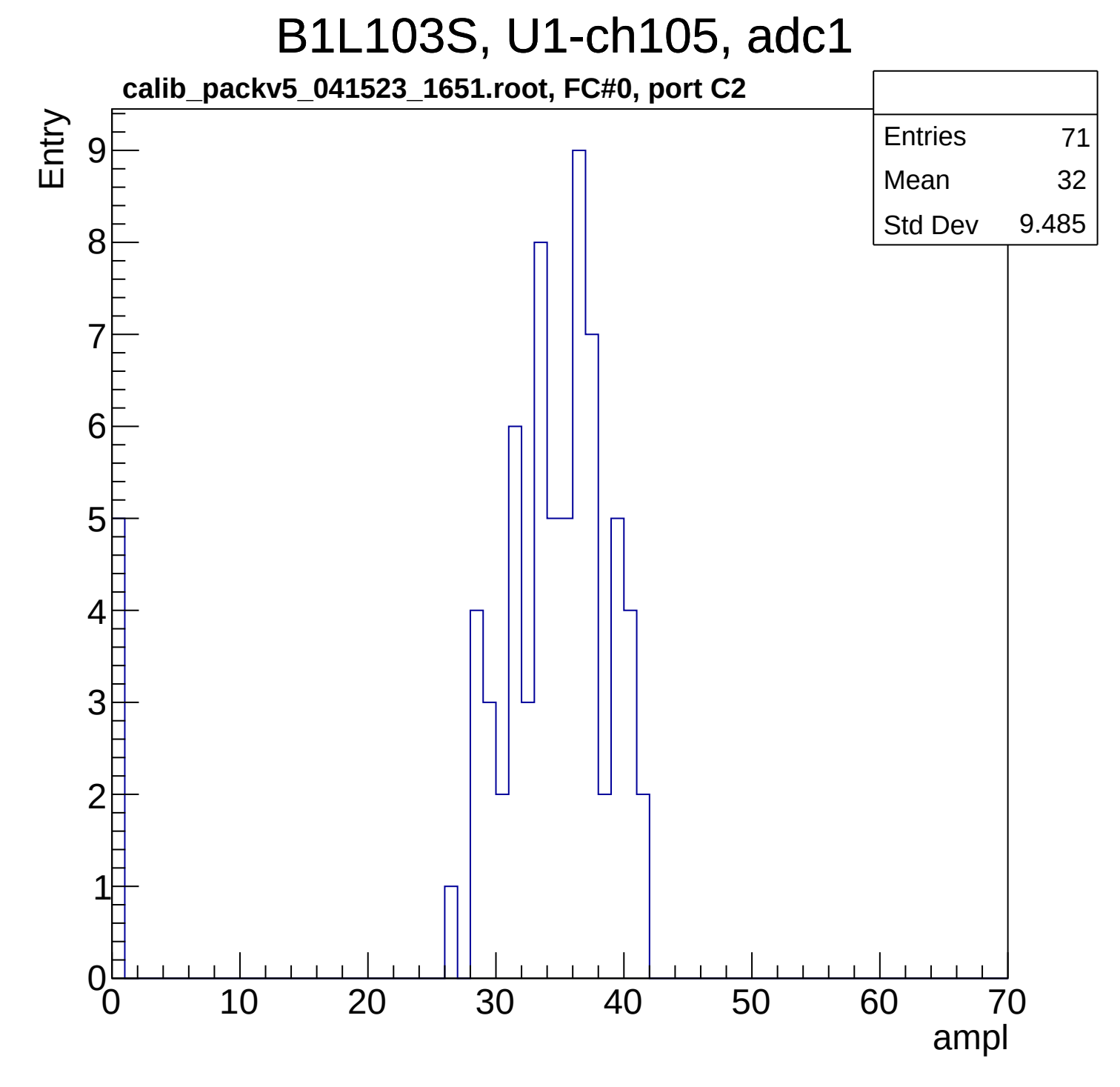
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch105, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 32
Std Dev 9.485
Entry
ampl
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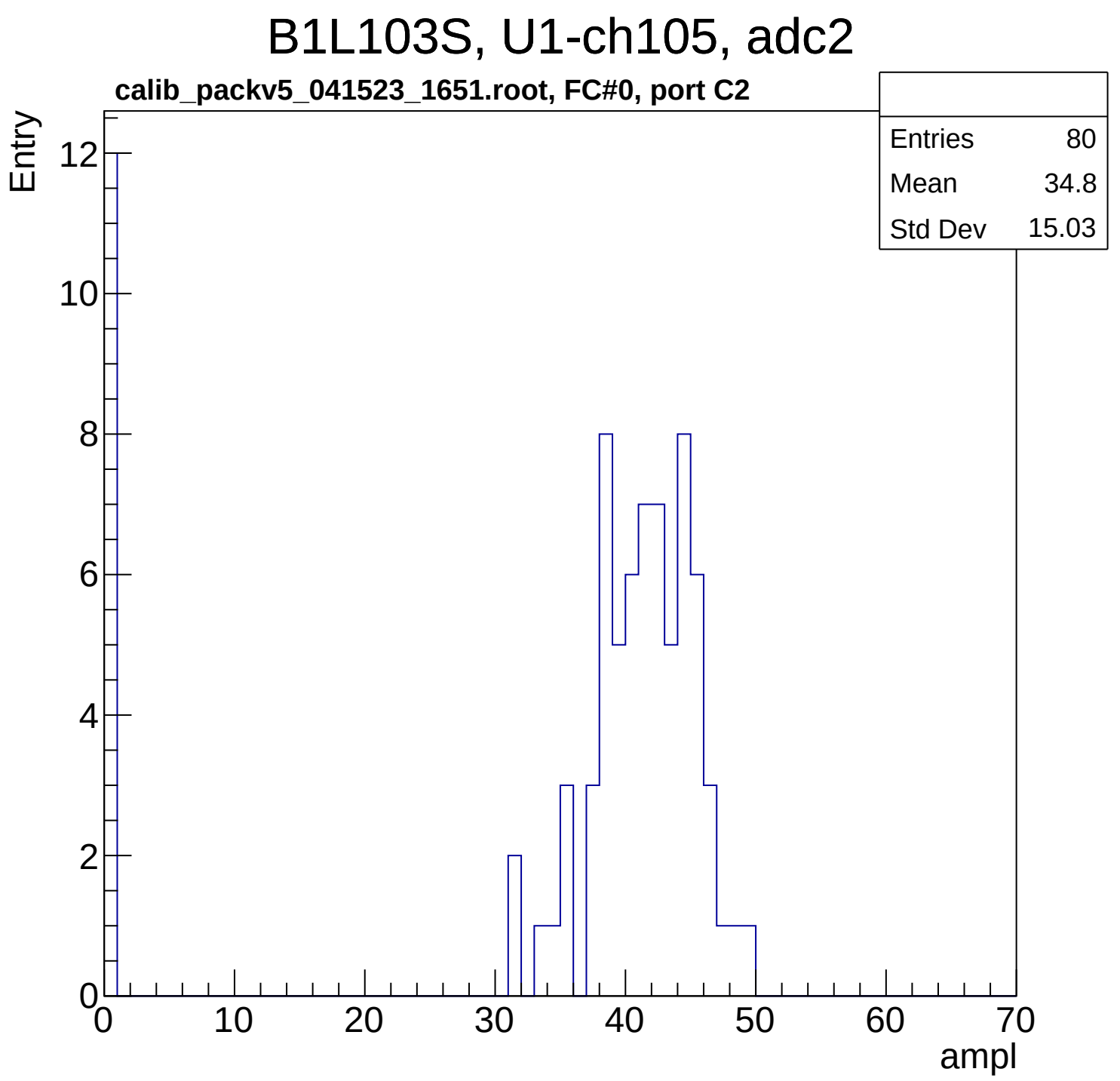
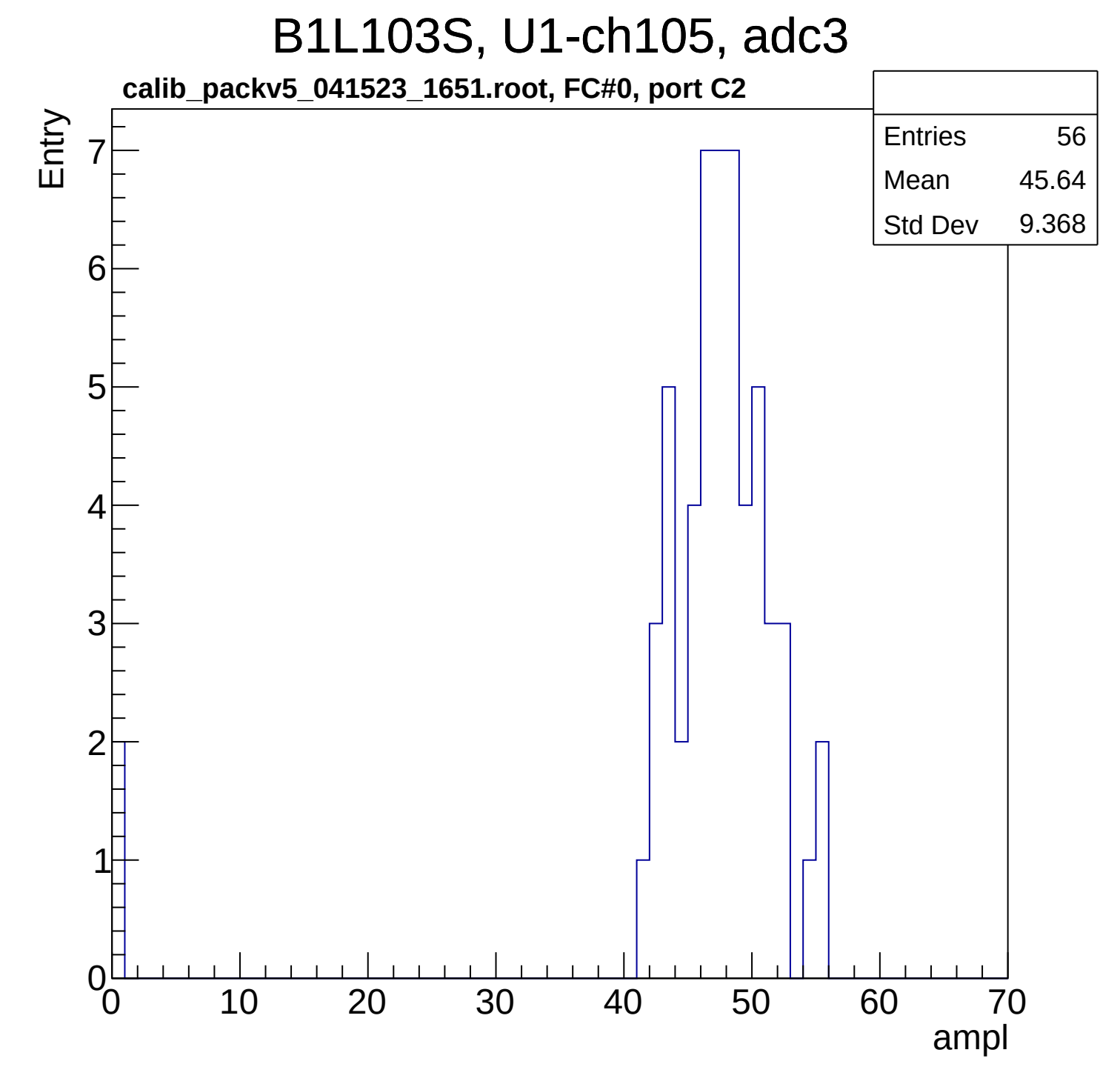
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U1-ch105, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 34.8
Std Dev 15.03
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70


B1L103S, U1-ch105, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 45.64
Std Dev 9.368
Entry
ampl
0
1
2
3
4
5
6
7
0
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20
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40
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60
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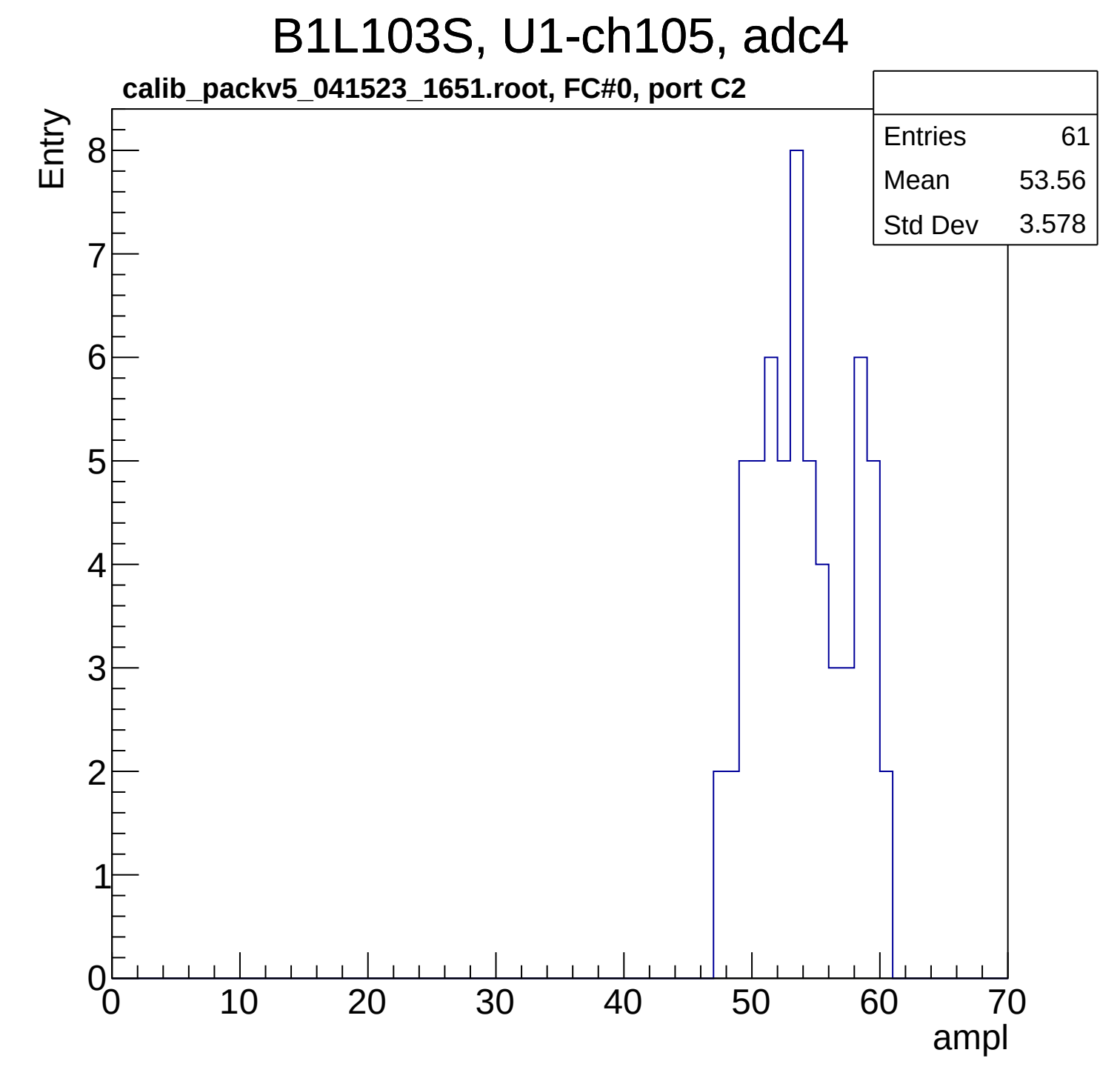
B1L103S, U1-ch105, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 53.56
Std Dev 3.578
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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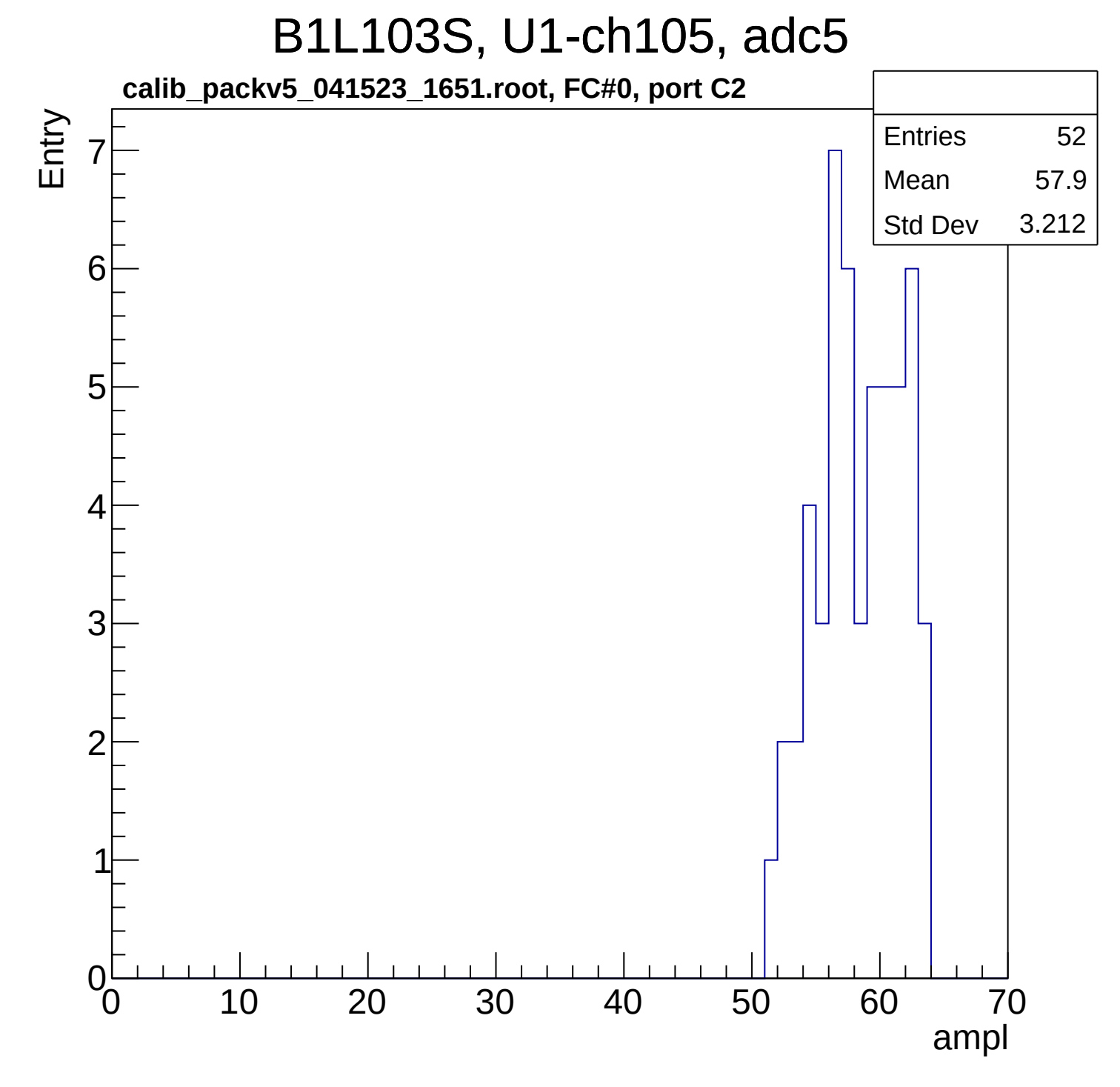
B1L103S, U1-ch105, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 57.9
Std Dev 3.212
Entry
ampl
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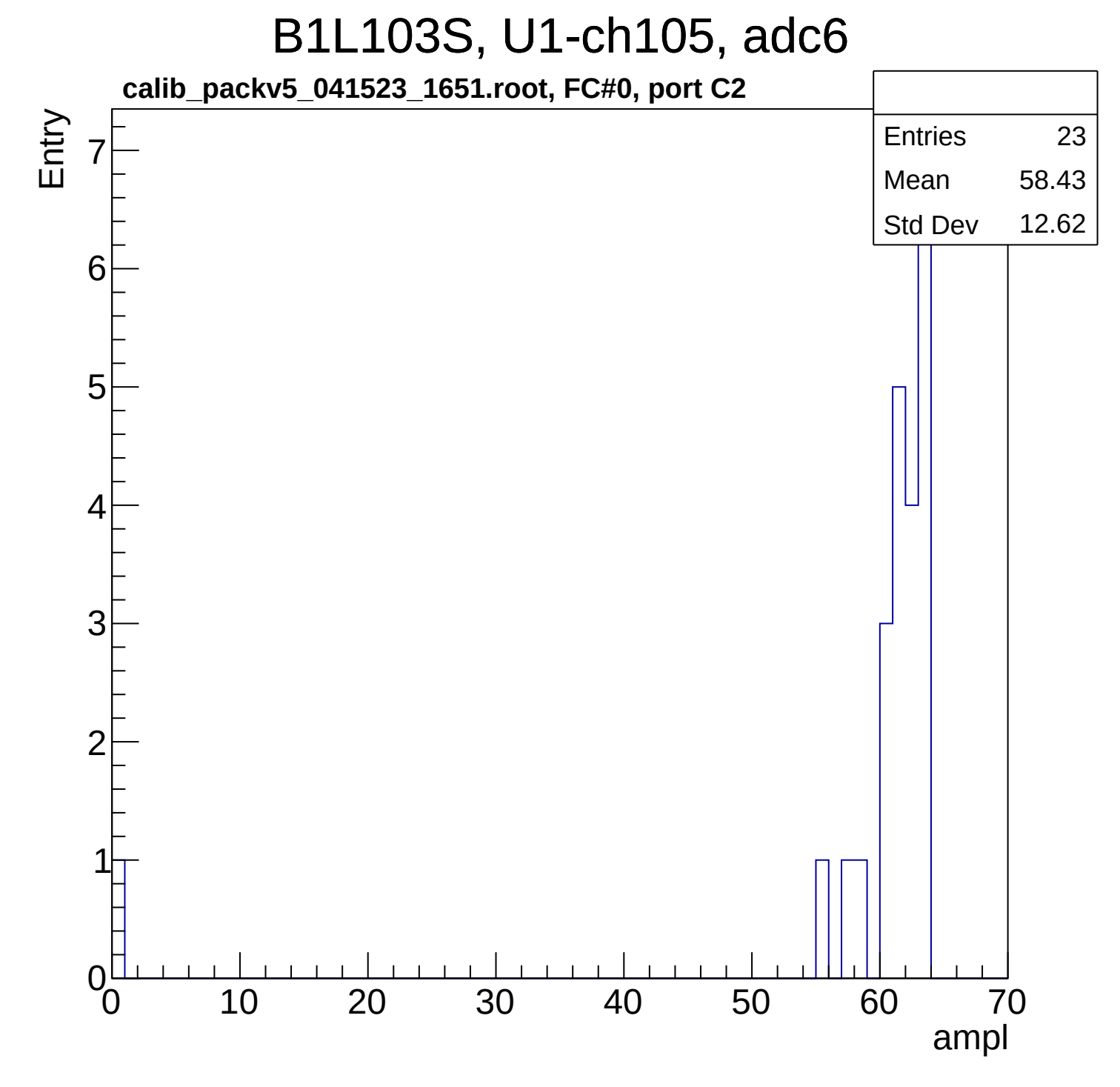
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U1-ch105, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 23
Mean 58.43
Std Dev 12.62
Entry
ampl
0
1
2
3
4
5
6
7
0
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20
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40
50
60
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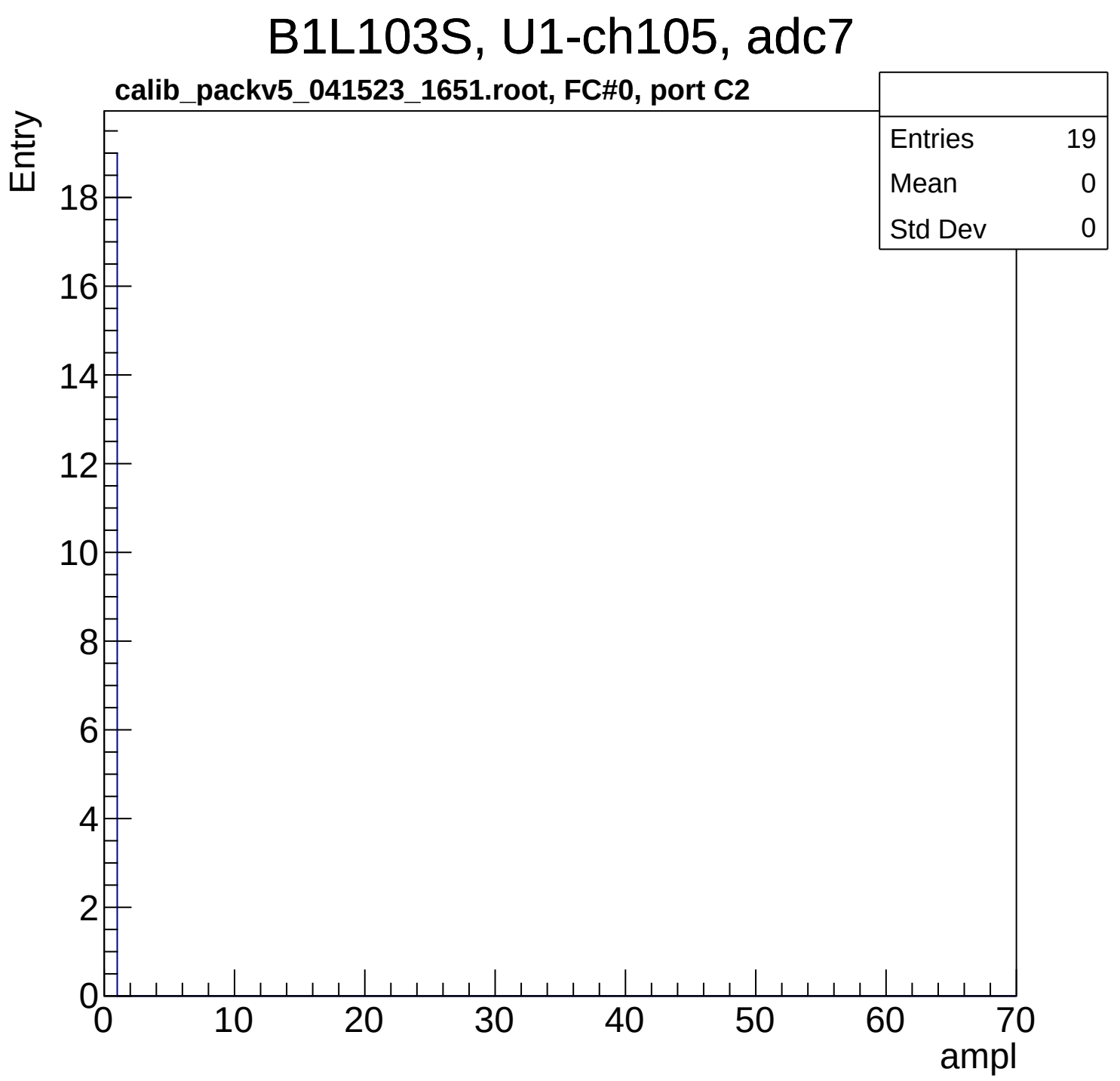
B1L103S, U1-ch105, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
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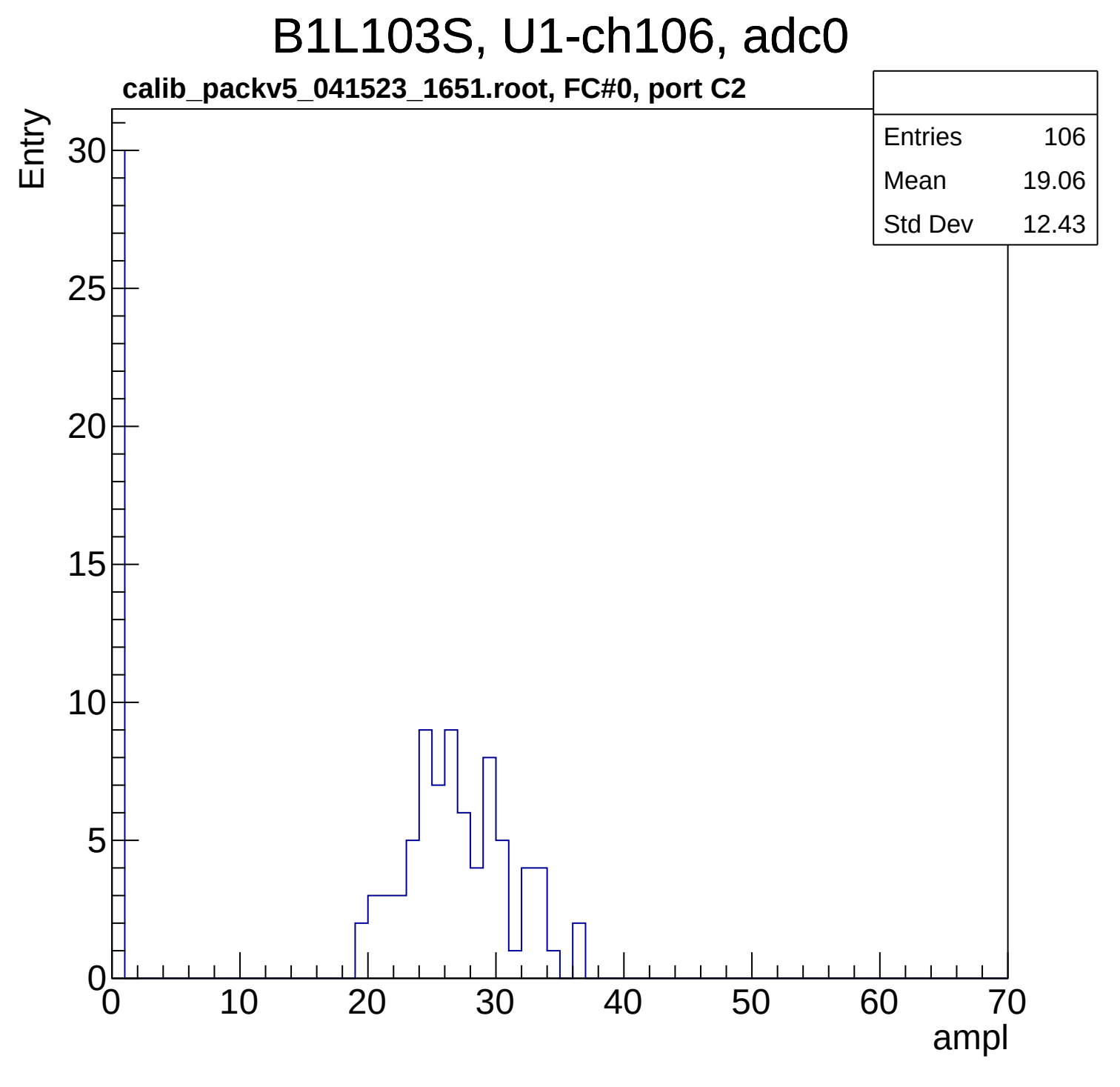
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch106, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 106
Mean 19.06
Std Dev 12.43
Entry
ampl
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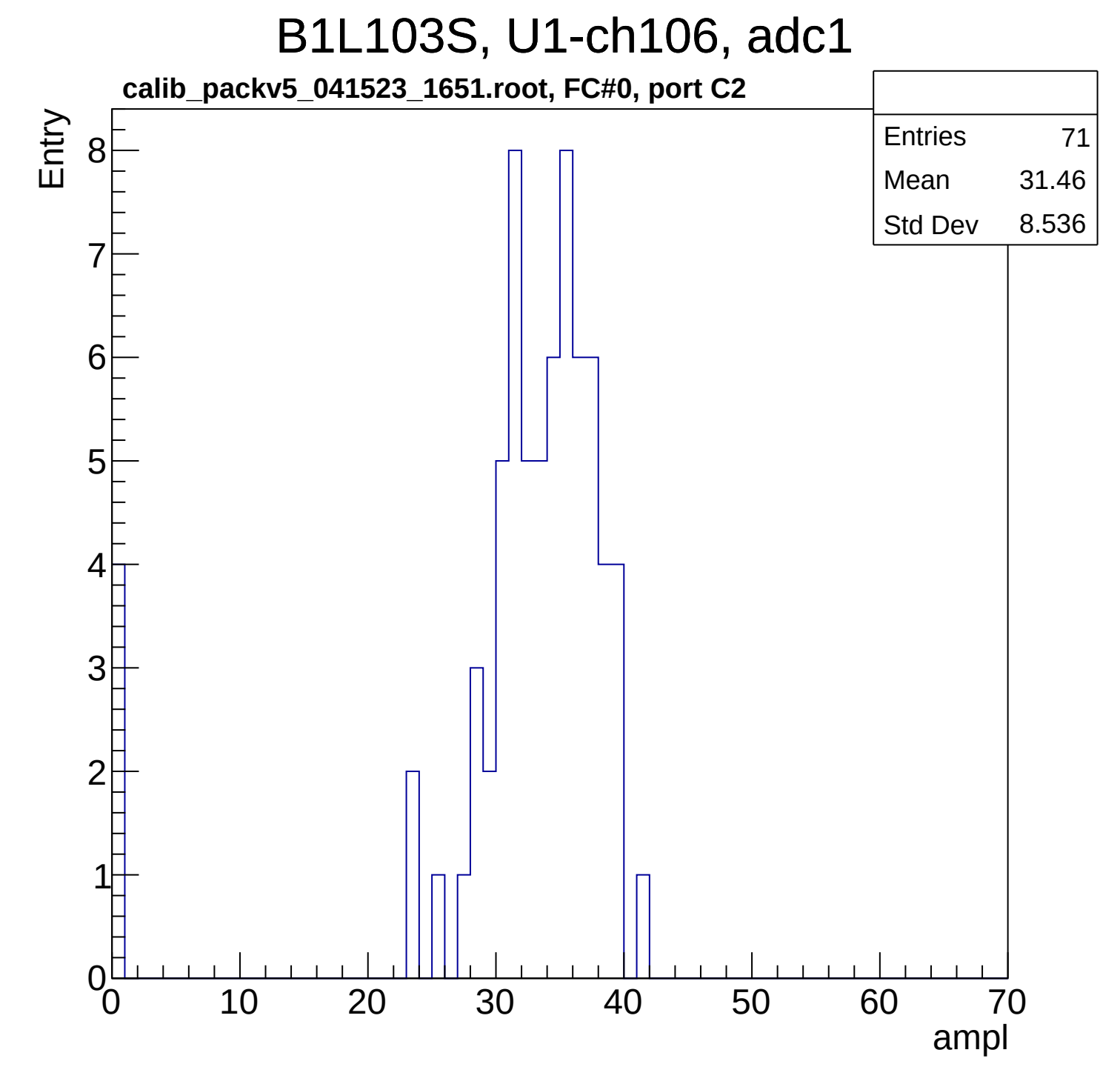
5
10
15
20
25
30
0
10
20
30
40
50
60
70


B1L103S, U1-ch106, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 31.46
Std Dev 8.536
Entry
ampl
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7
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0
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20
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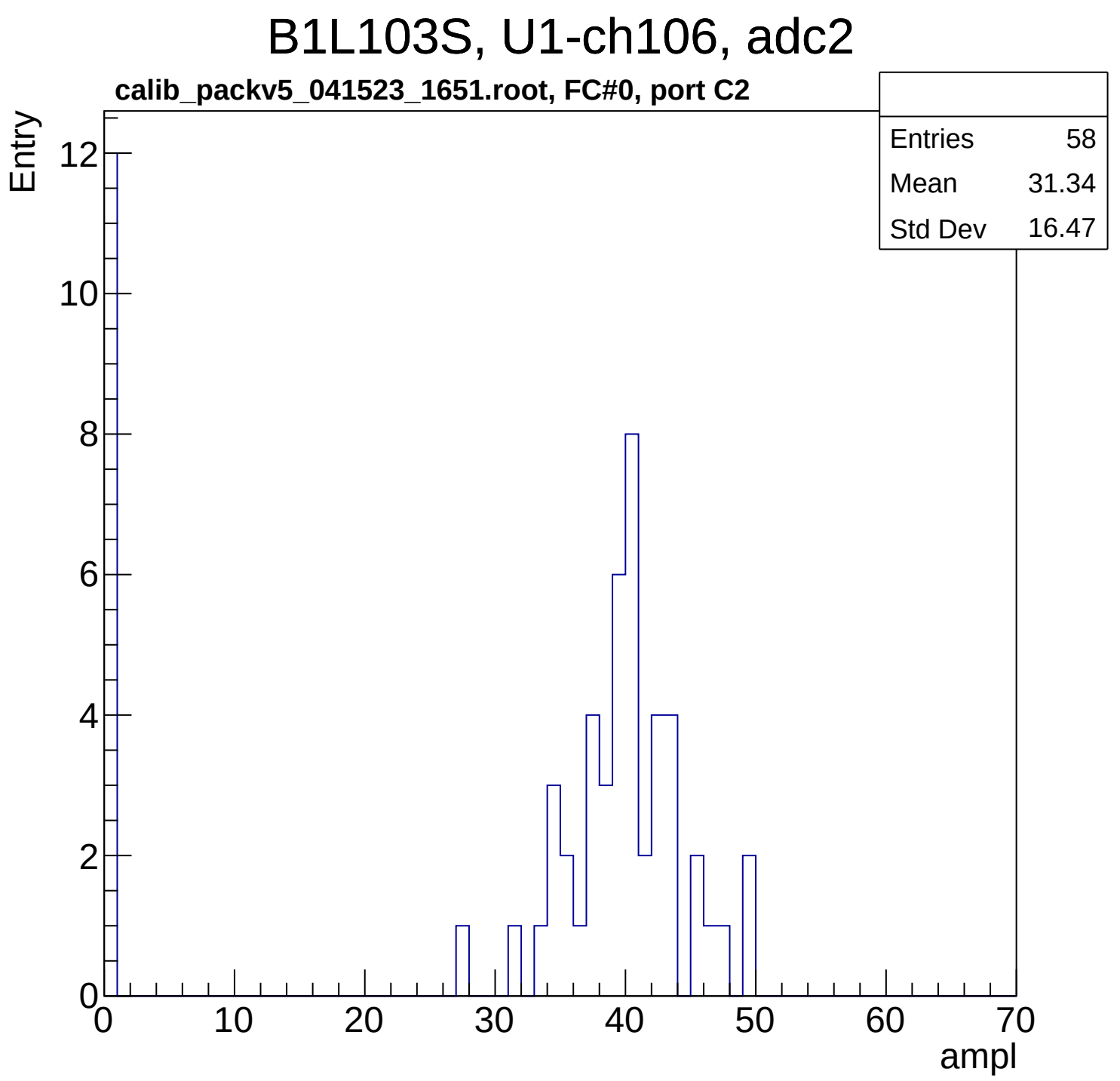
40
50
60
70


B1L103S, U1-ch106, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 31.34
Std Dev 16.47
Entry
0
2
4
6
8
10
12
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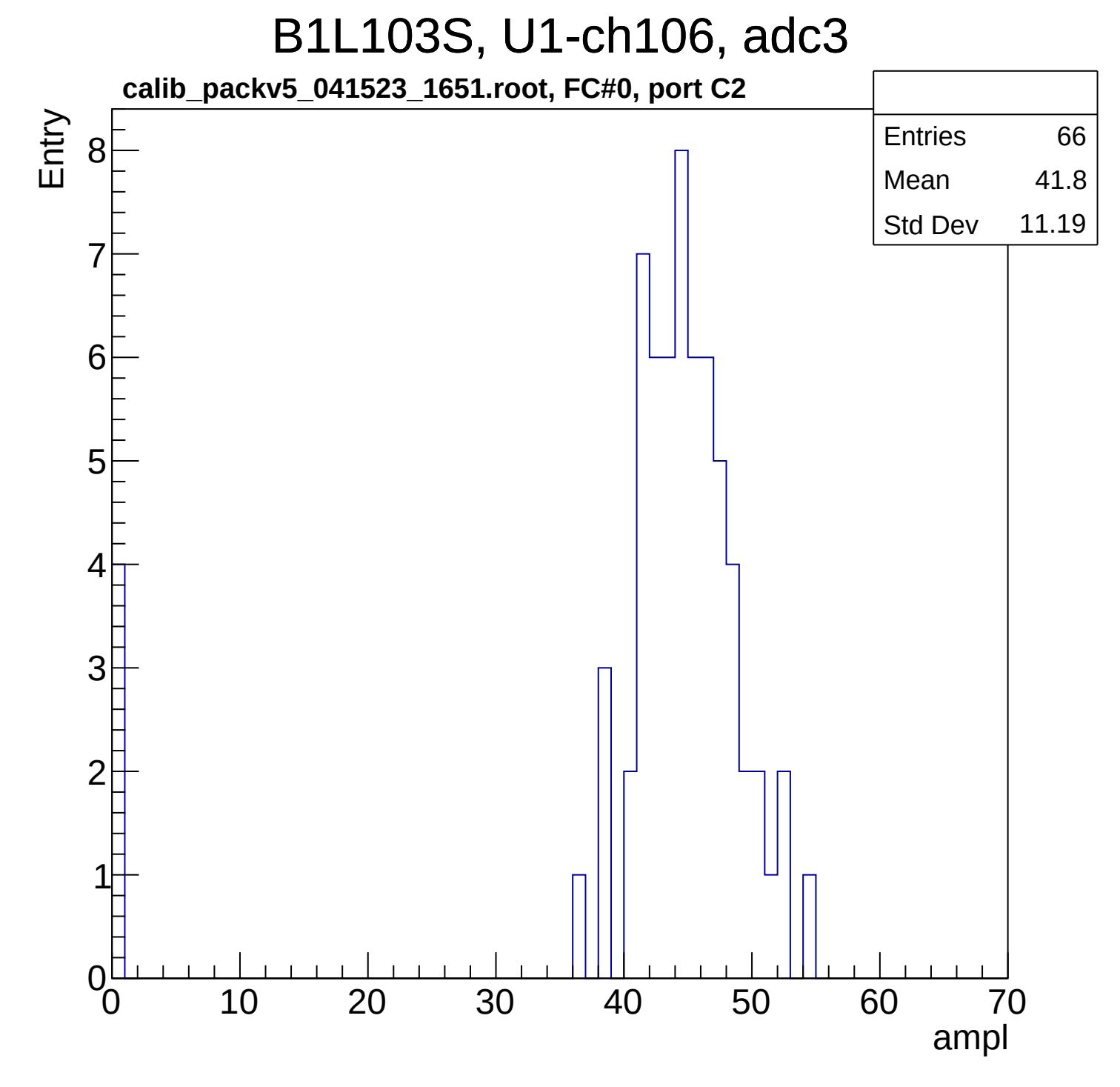
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch106, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 41.8
Std Dev 11.19
Entry
ampl
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5
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0
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60
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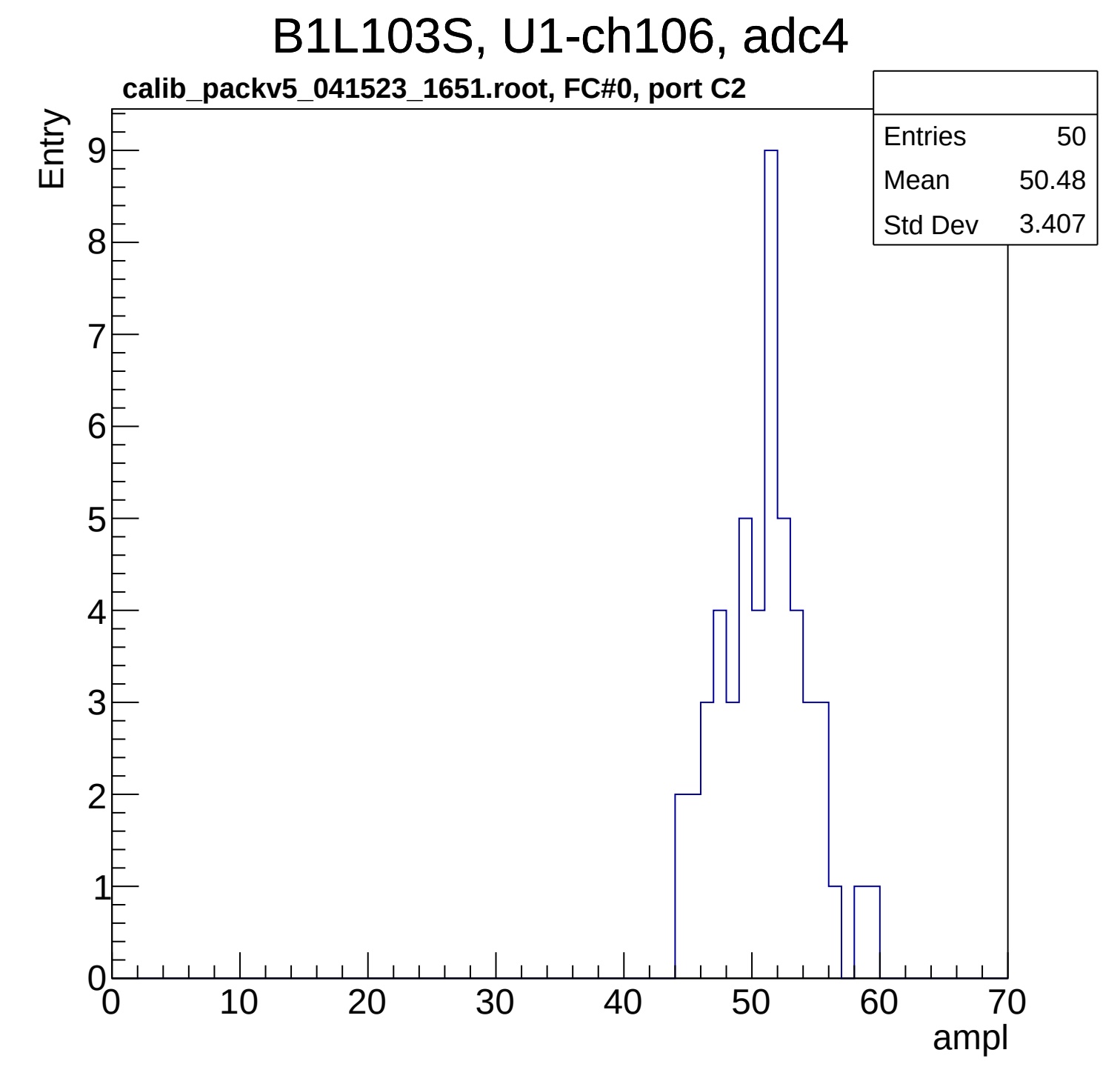
B1L103S, U1-ch106, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 50.48
Std Dev 3.407
Entry
ampl
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10
20
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40
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2
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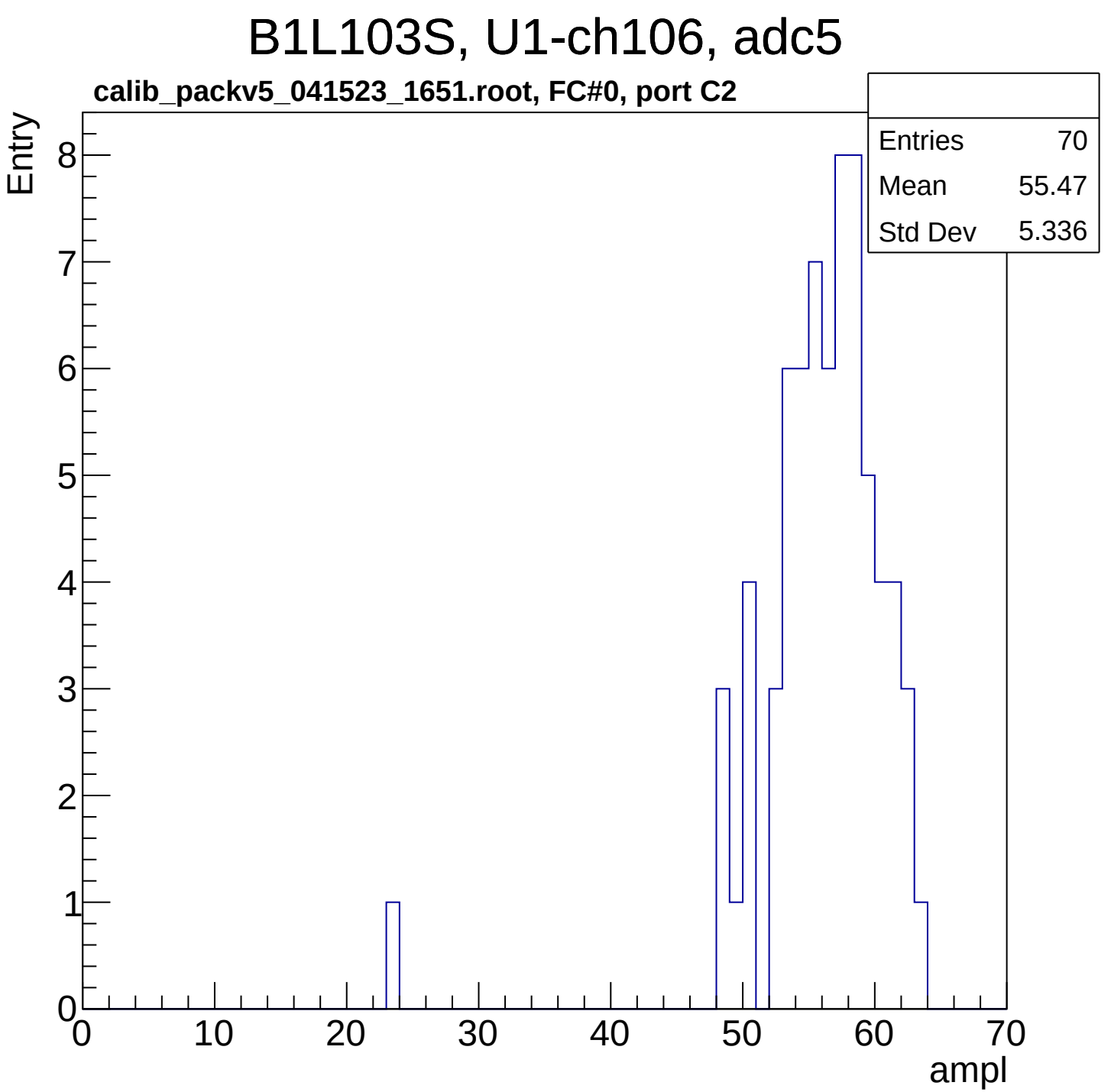
6
7
8
9


B1L103S, U1-ch106, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 55.47
Std Dev 5.336
Entry
ampl
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2
3
4
5
6
7
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0
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20
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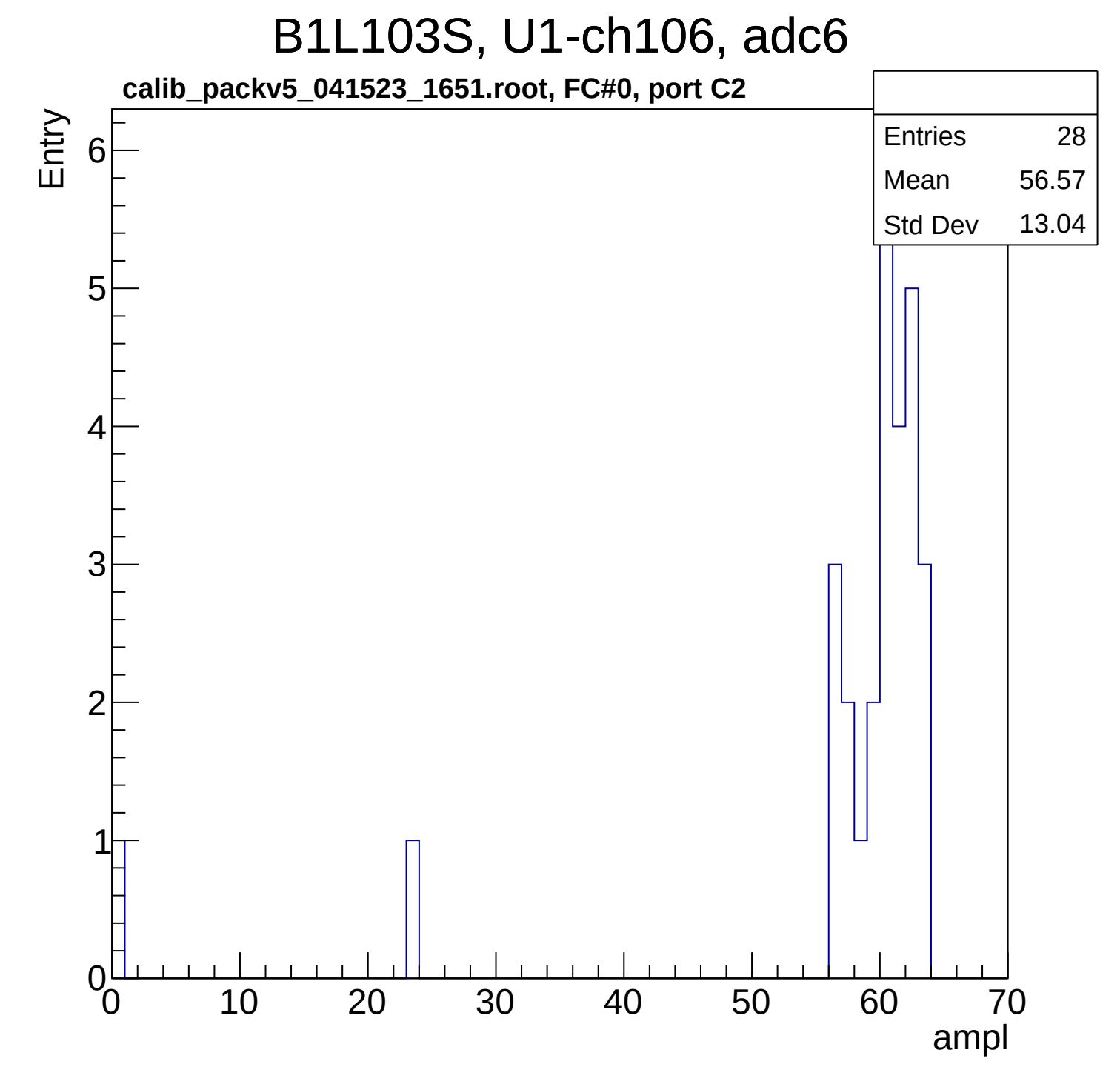
40
50
60
70


B1L103S, U1-ch106, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 28
Mean 56.57
Std Dev 13.04
Entry
ampl
0
1
2
3
4
5
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0
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20
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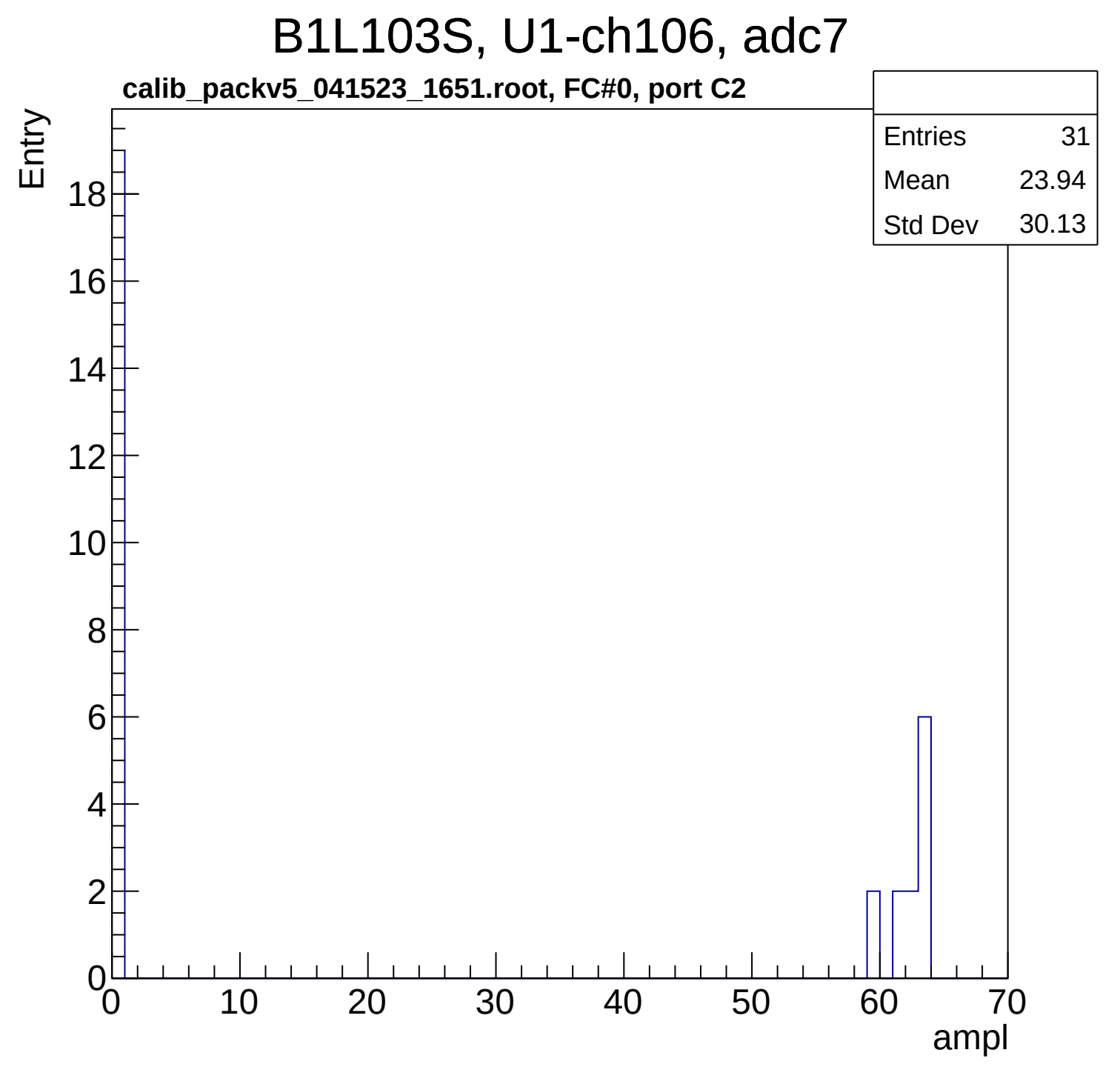
50
60
70


B1L103S, U1-ch106, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 31
Mean 23.94
Std Dev 30.13
Entry
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6
8
10
12
14
16
18
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10
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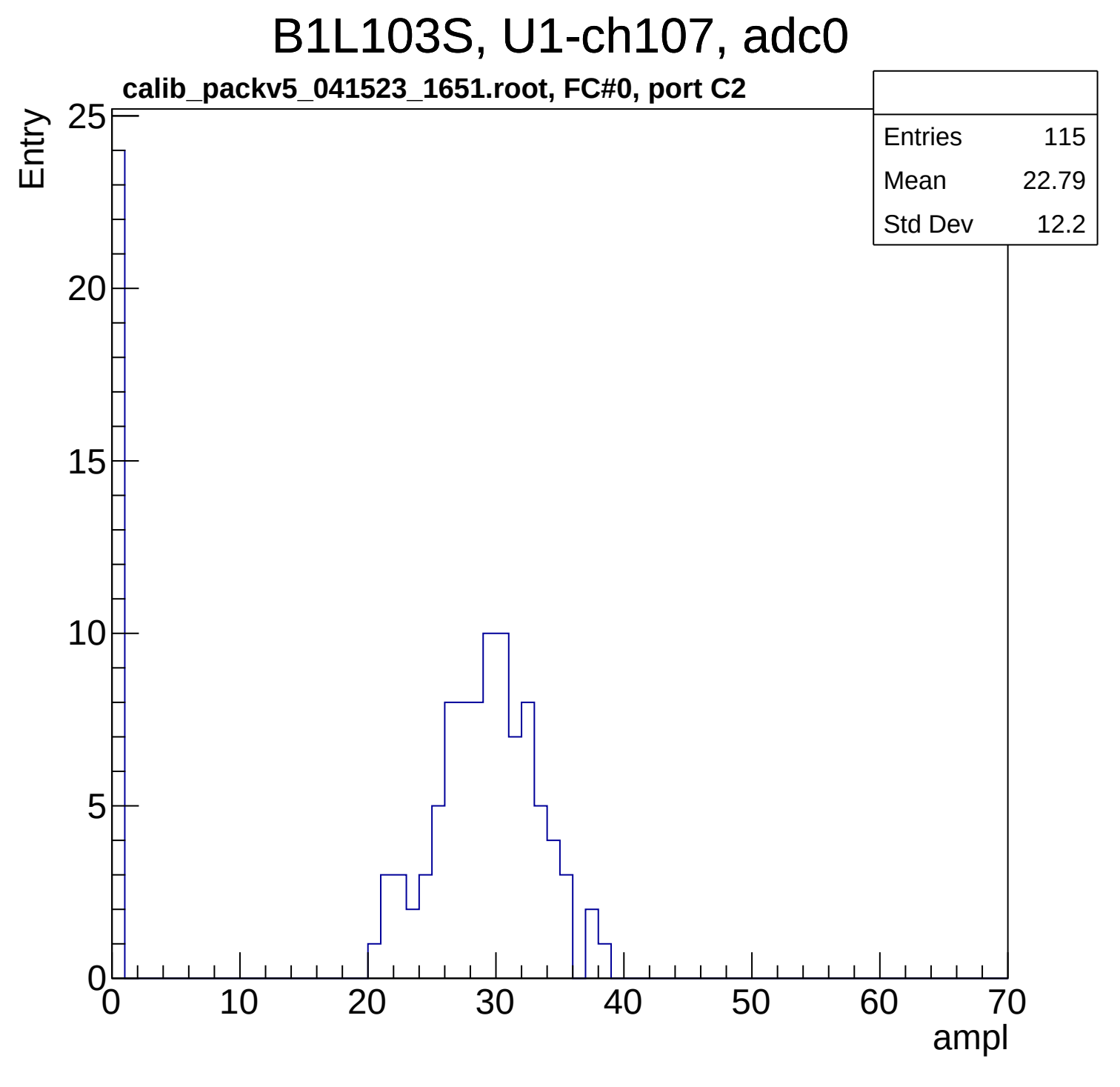
30
40
50
60
70
ampl


B1L103S, U1-ch107, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 115
Mean 22.79
Std Dev 12.2
Entry
ampl
0
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10
15
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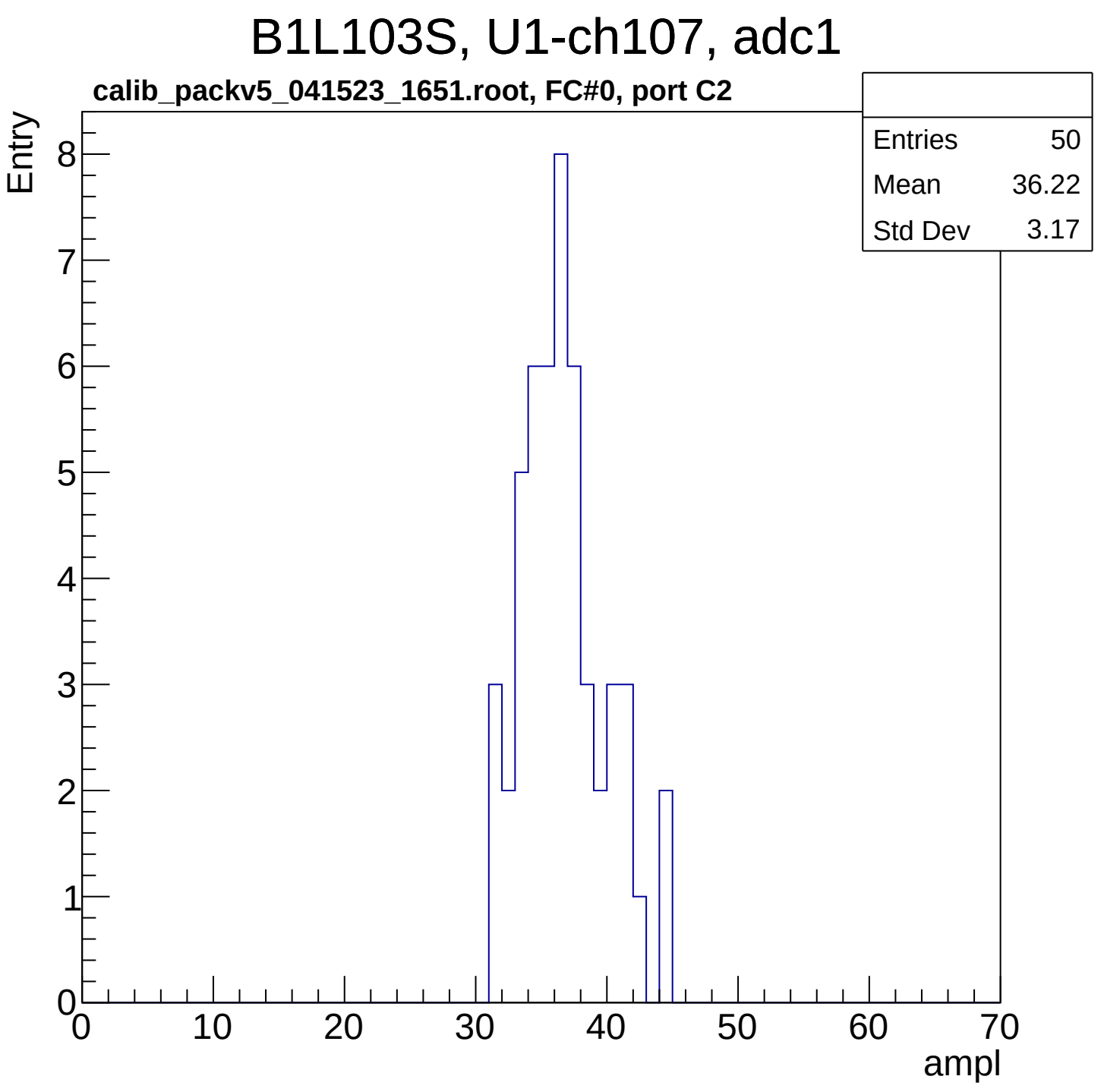
50
60
70


B1L103S, U1-ch107, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 36.22
Std Dev 3.17
Entry
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2
3
4
5
6
7
8
0
10
20
30
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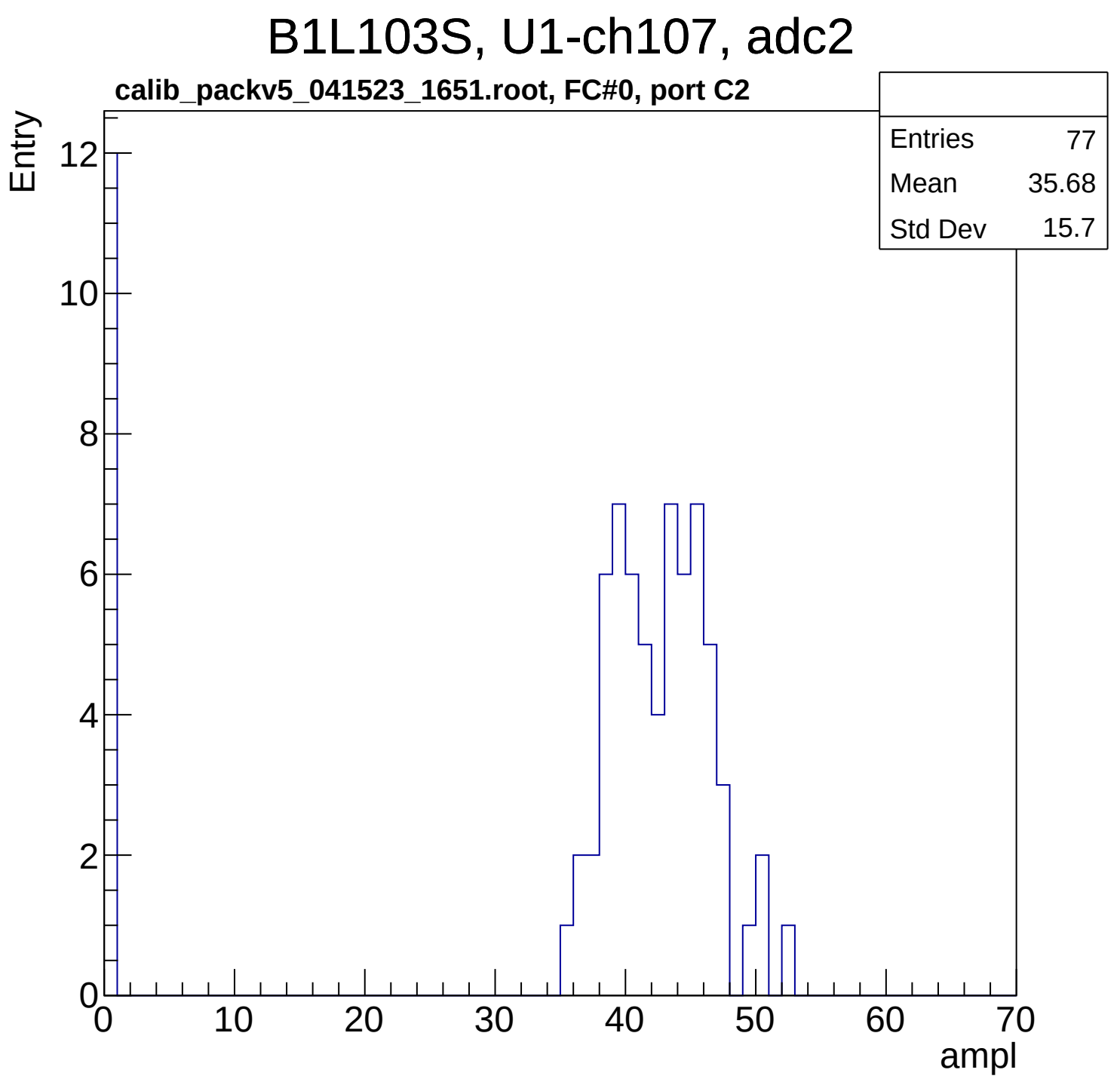
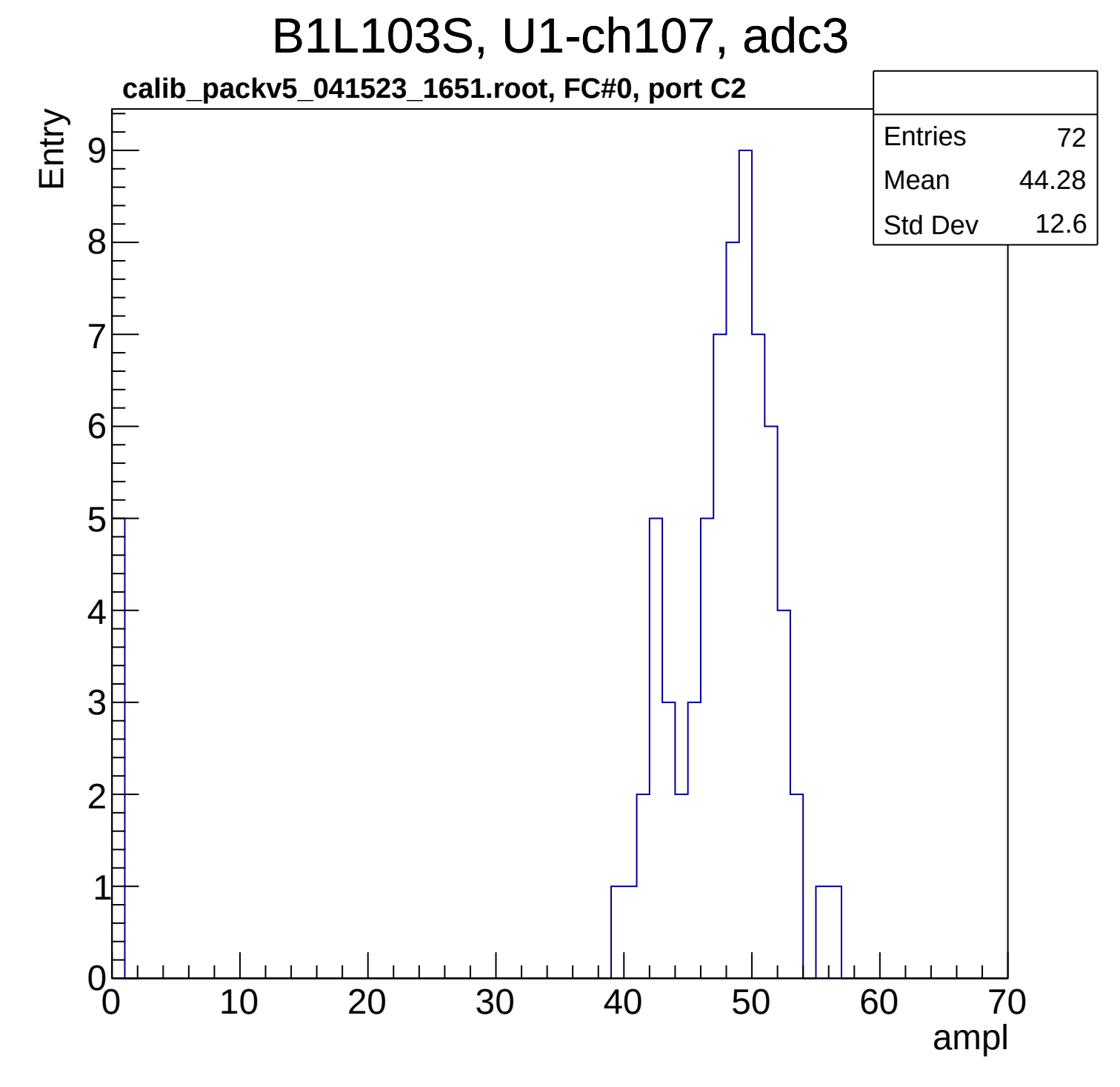
50
60
70
ampl


B1L103S, U1-ch107, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 35.68
Std Dev 15.7
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch107, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 44.28
Std Dev 12.6
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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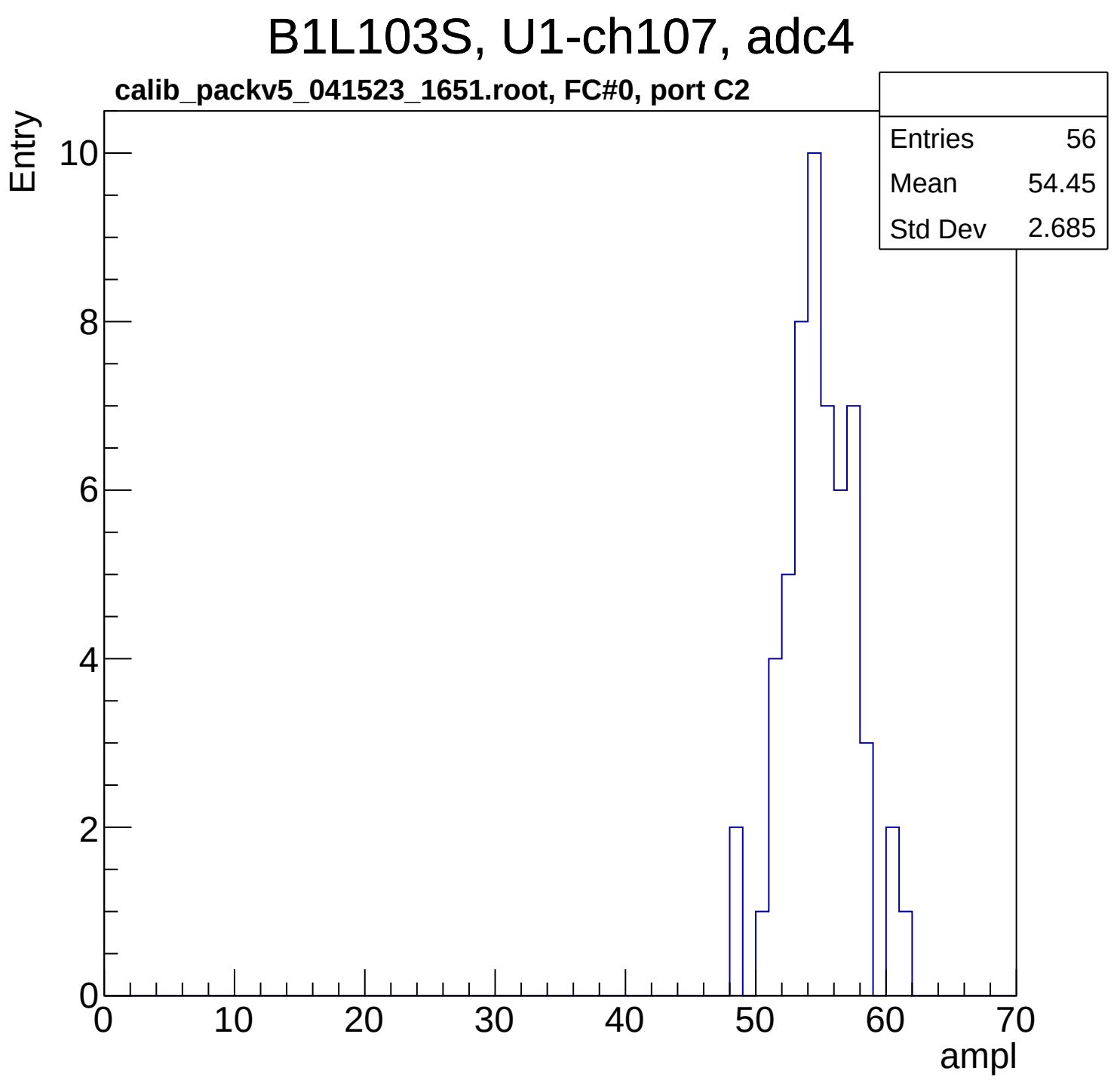
40
50
60
70


B1L103S, U1-ch107, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 54.45
Std Dev 2.685
Entry
ampl
0
2
4
6
8
10
0
10
20
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40
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60
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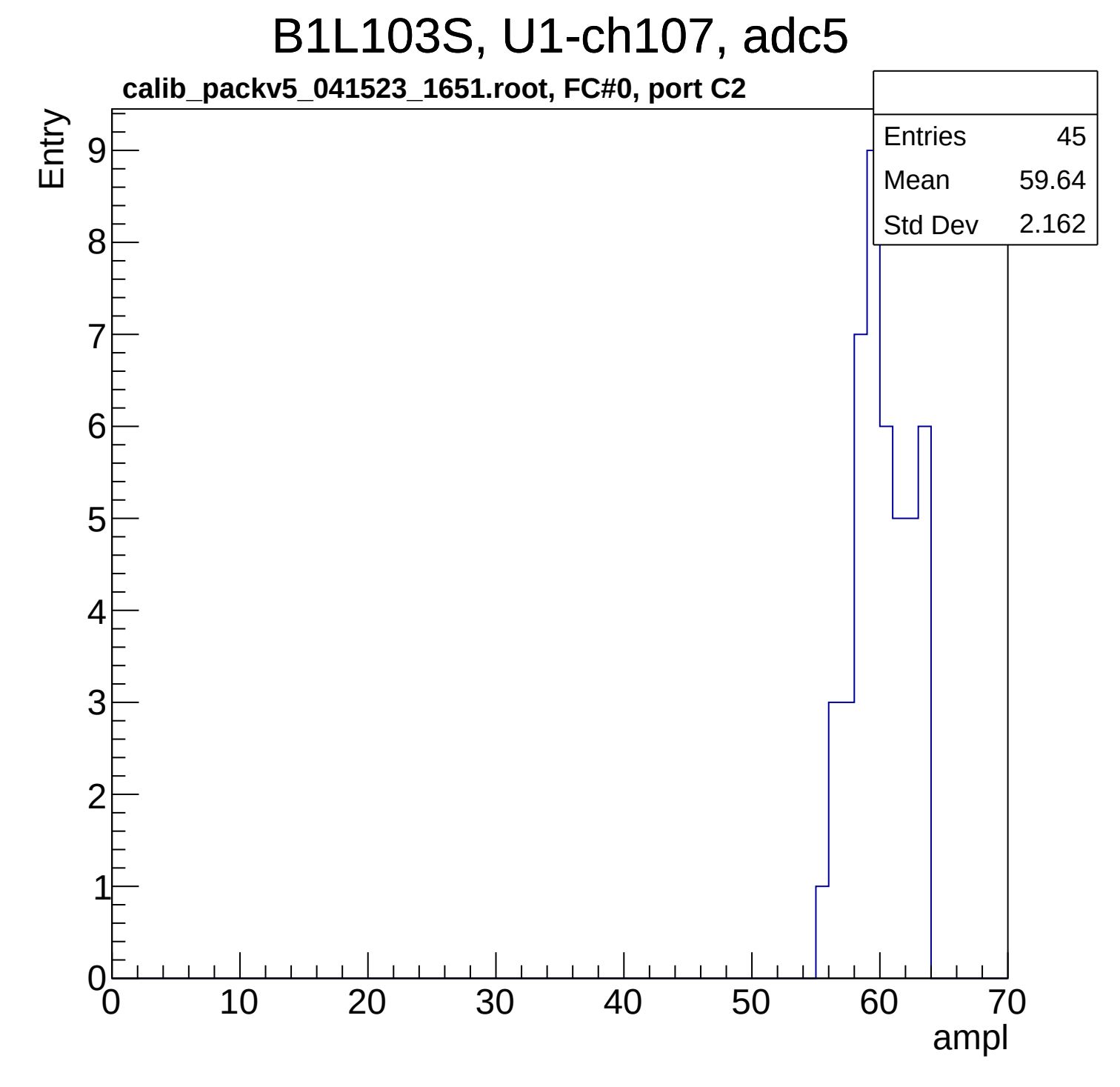
B1L103S, U1-ch107, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 59.64
Std Dev 2.162
Entry
ampl
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2
3
4
5
6
7
8
9
0
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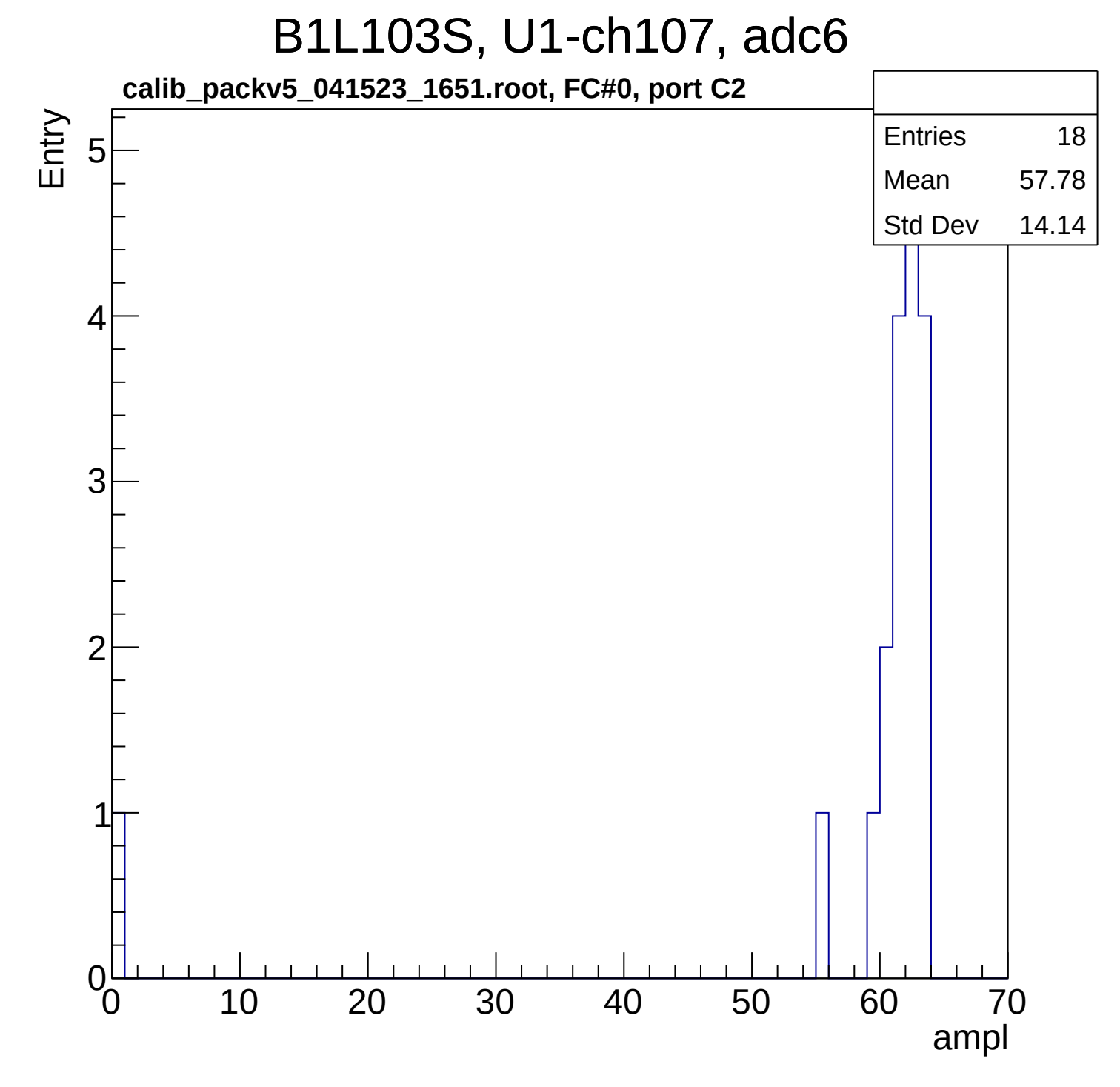
B1L103S, U1-ch107, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 57.78
Std Dev 14.14
Entry
ampl
0
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2
3
4
5
0
10
20
30
40
50
60
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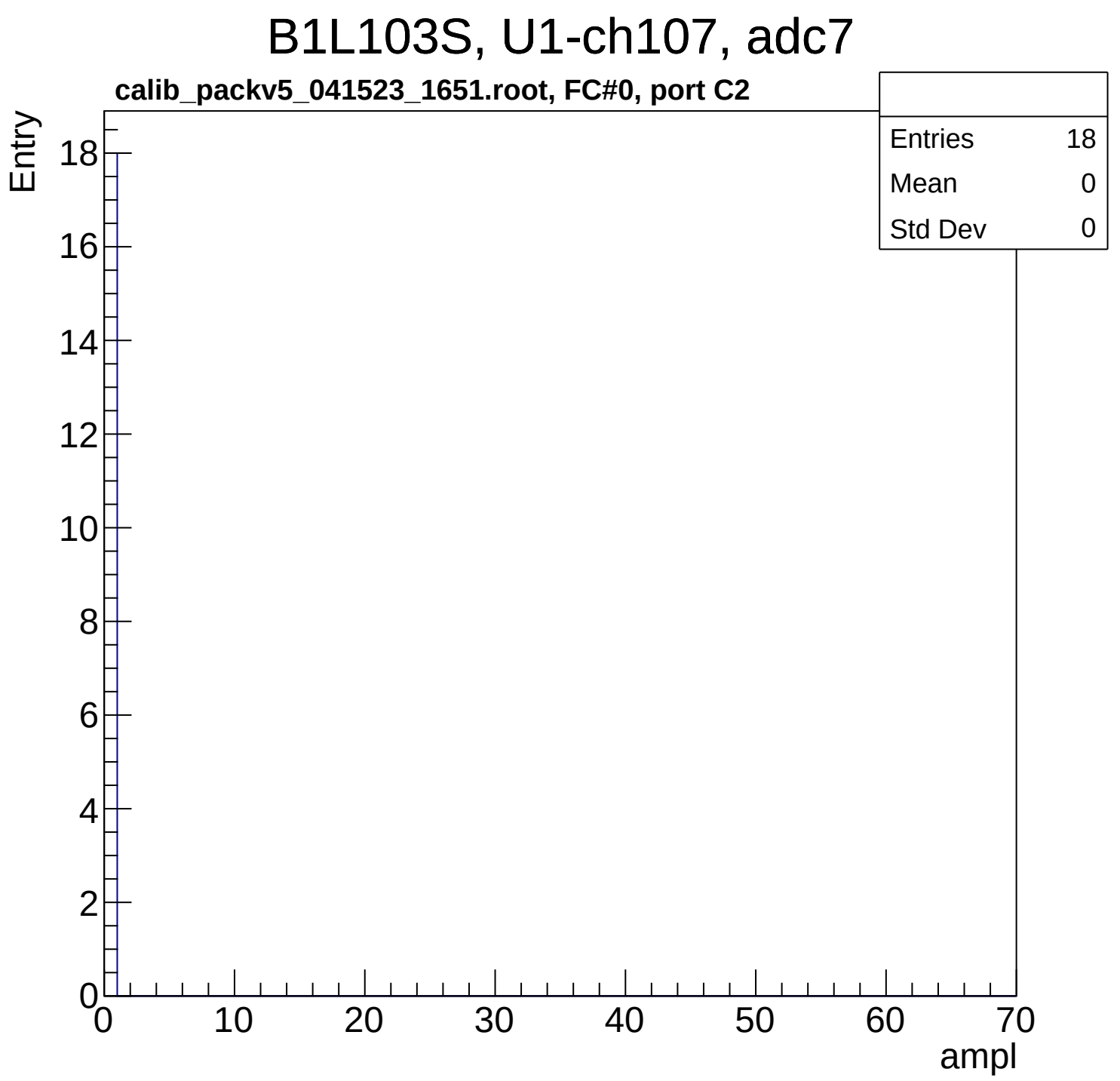
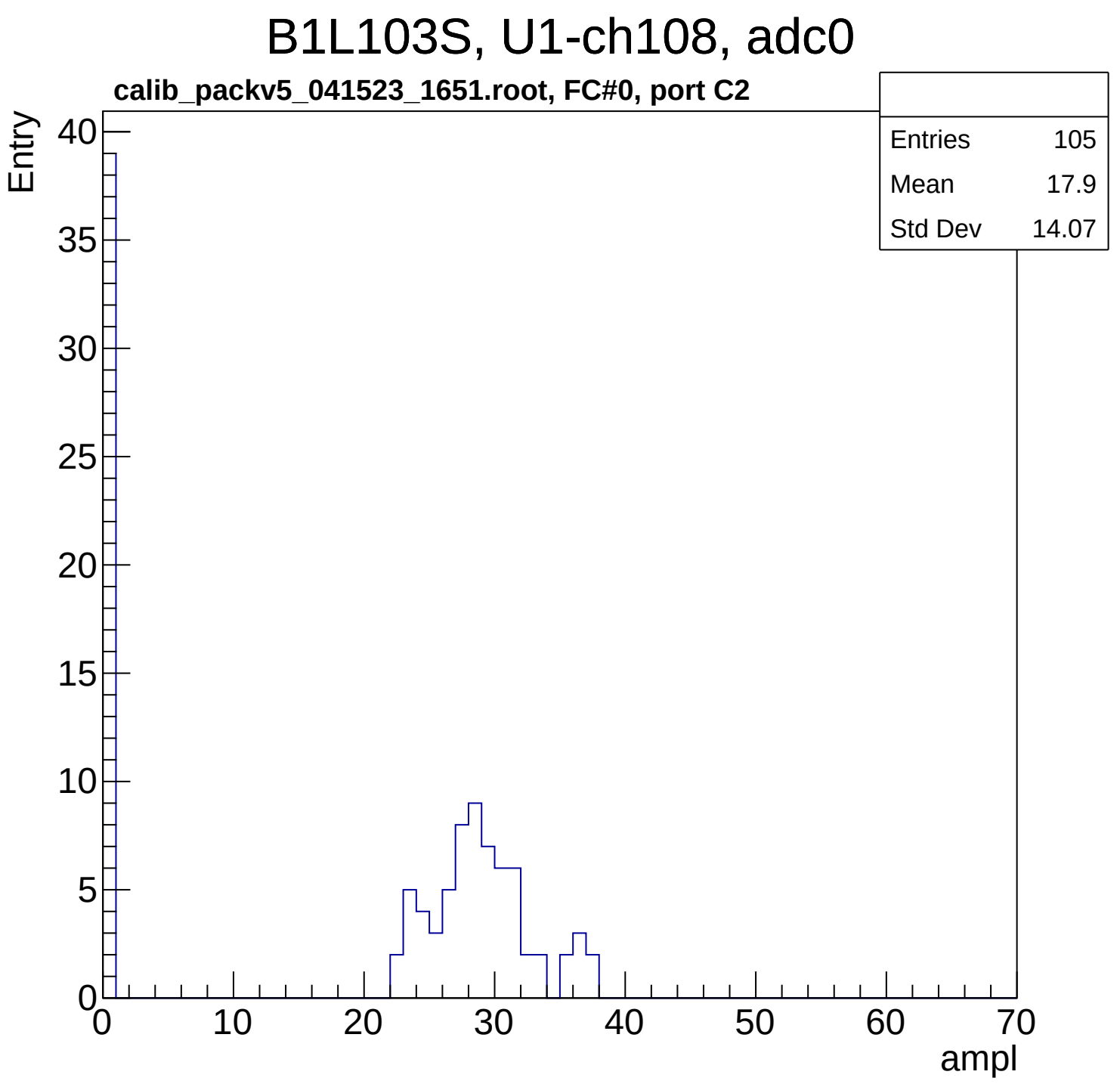

B1L103S, U1-ch107, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch108, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 105
Mean 17.9
Std Dev 14.07
Entry
ampl
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5
10
15
20
25
30
35
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0
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40
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60
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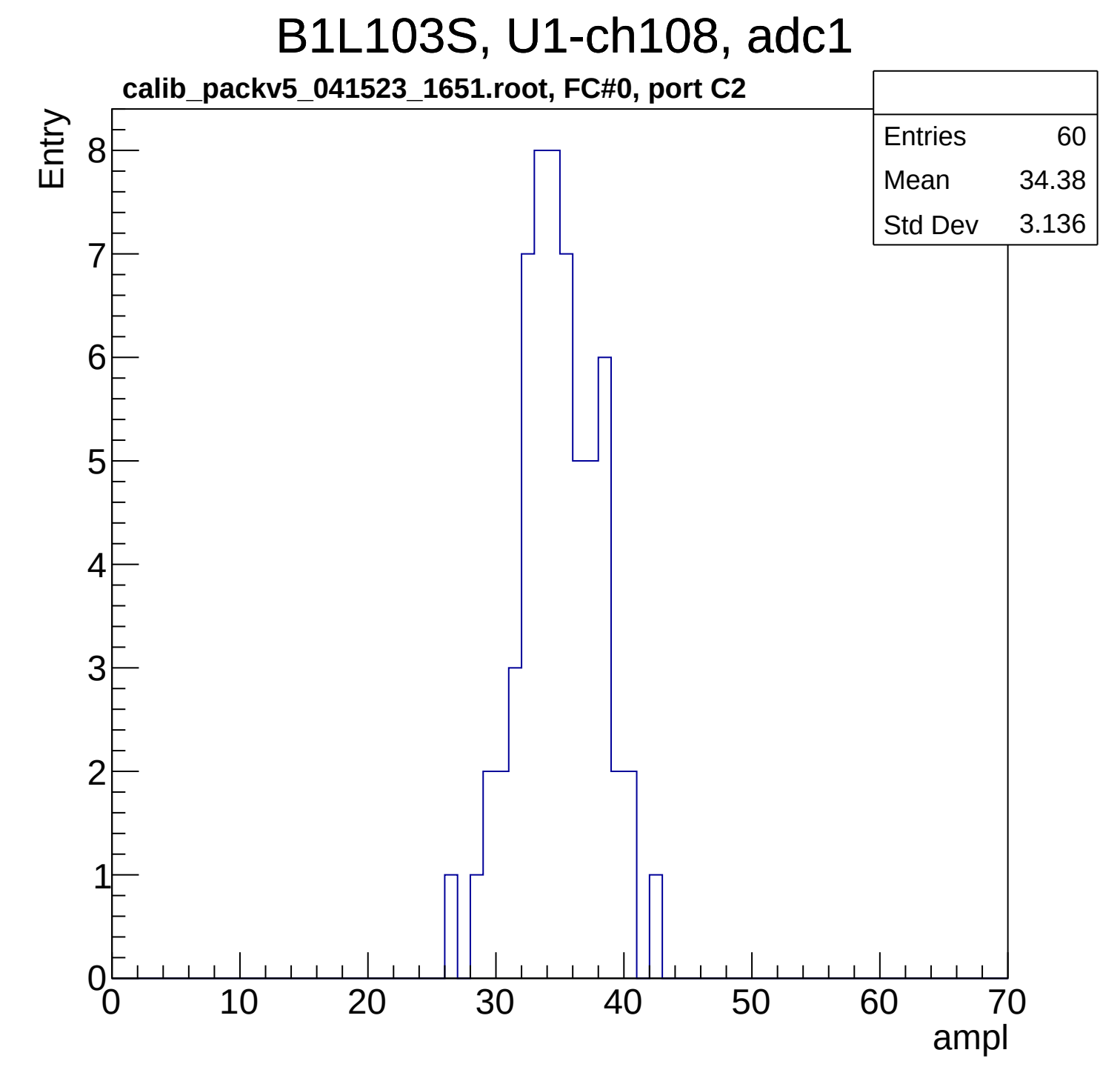
B1L103S, U1-ch108, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 34.38
Std Dev 3.136
Entry
ampl
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2
3
4
5
6
7
8
0
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20
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40
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60
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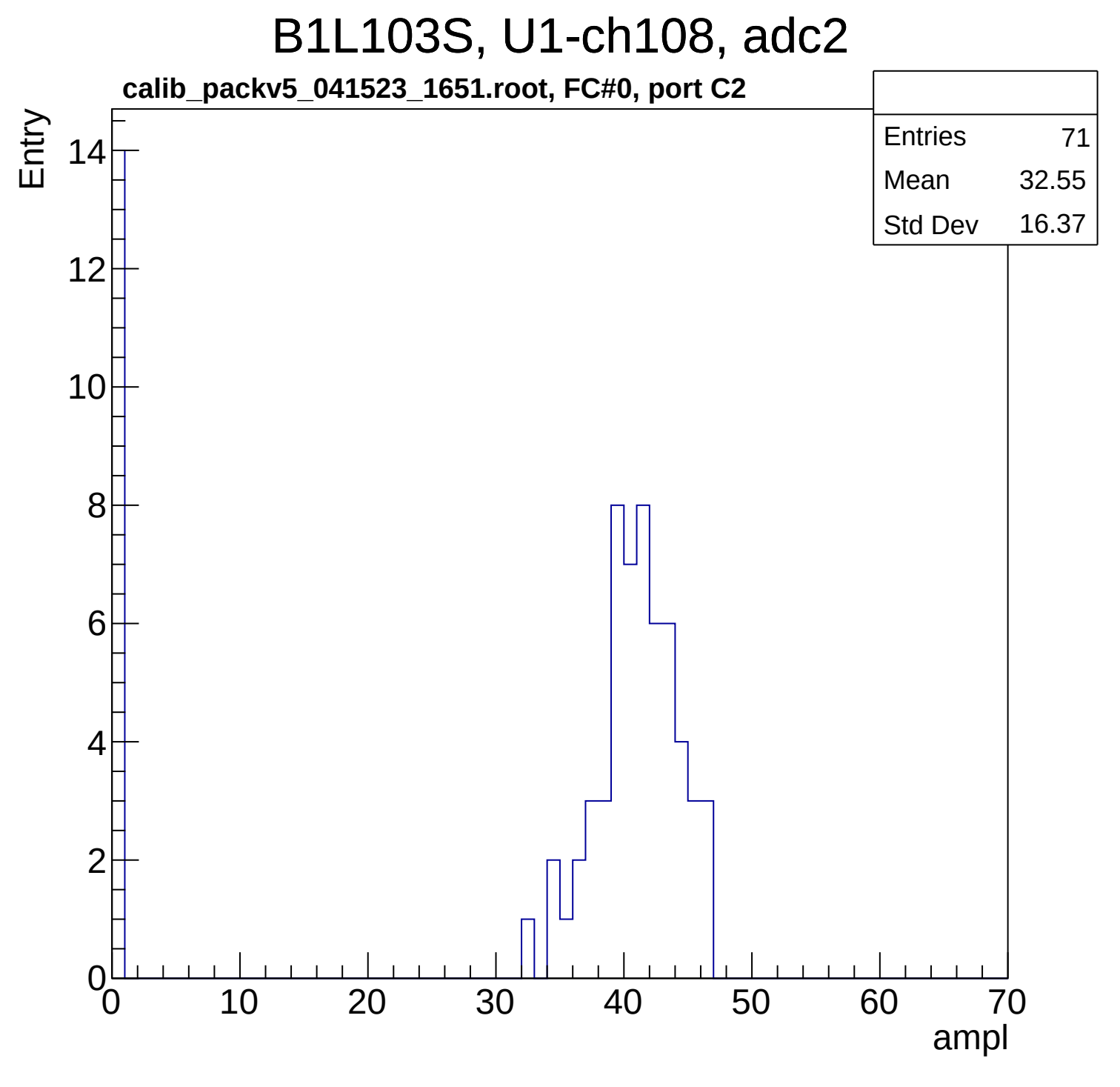
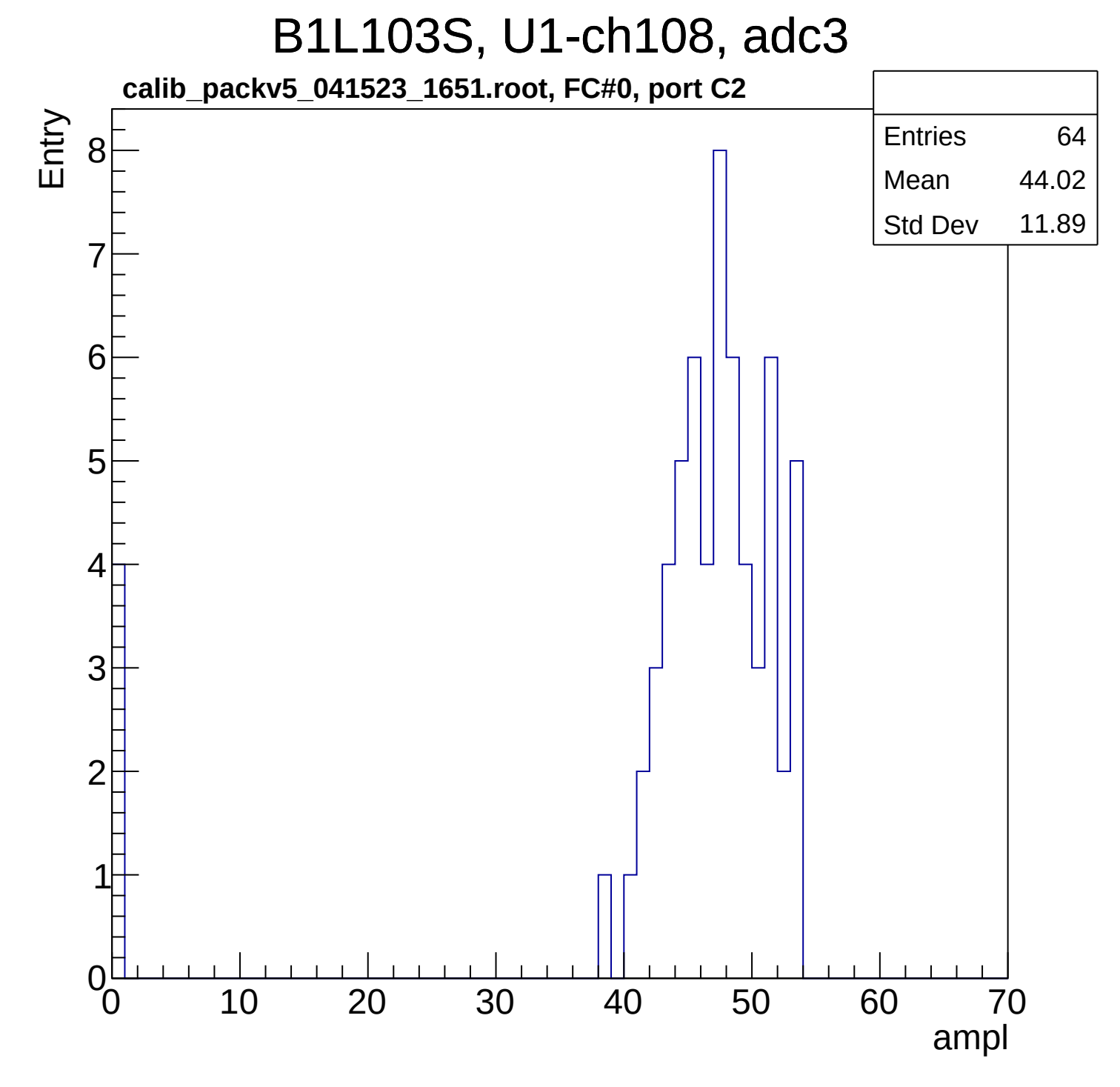

B1L103S, U1-ch108, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 32.55
Std Dev 16.37
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch108, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 44.02
Std Dev 11.89
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
30
40
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60
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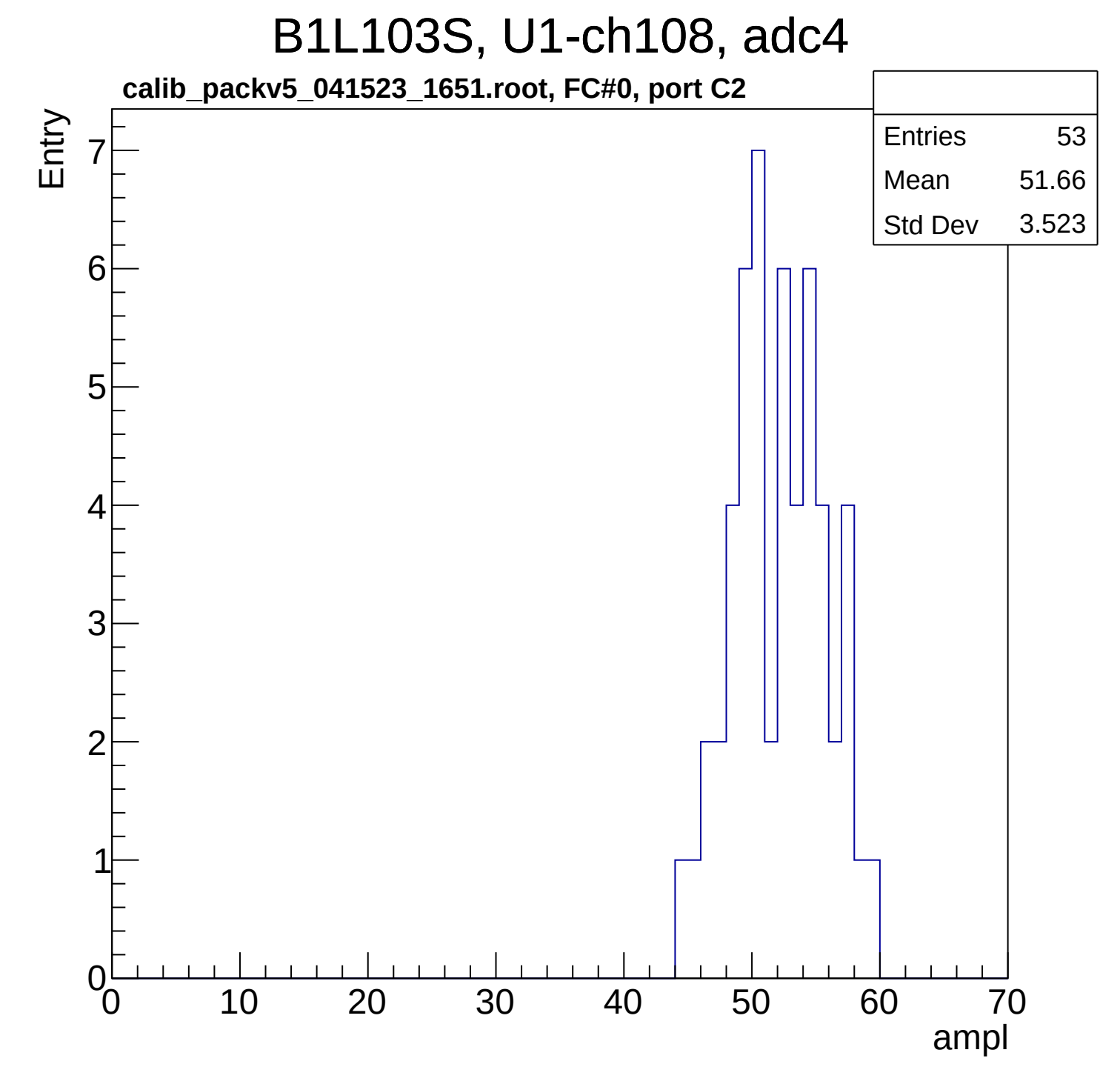
B1L103S, U1-ch108, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 51.66
Std Dev 3.523
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
30
40
50
60
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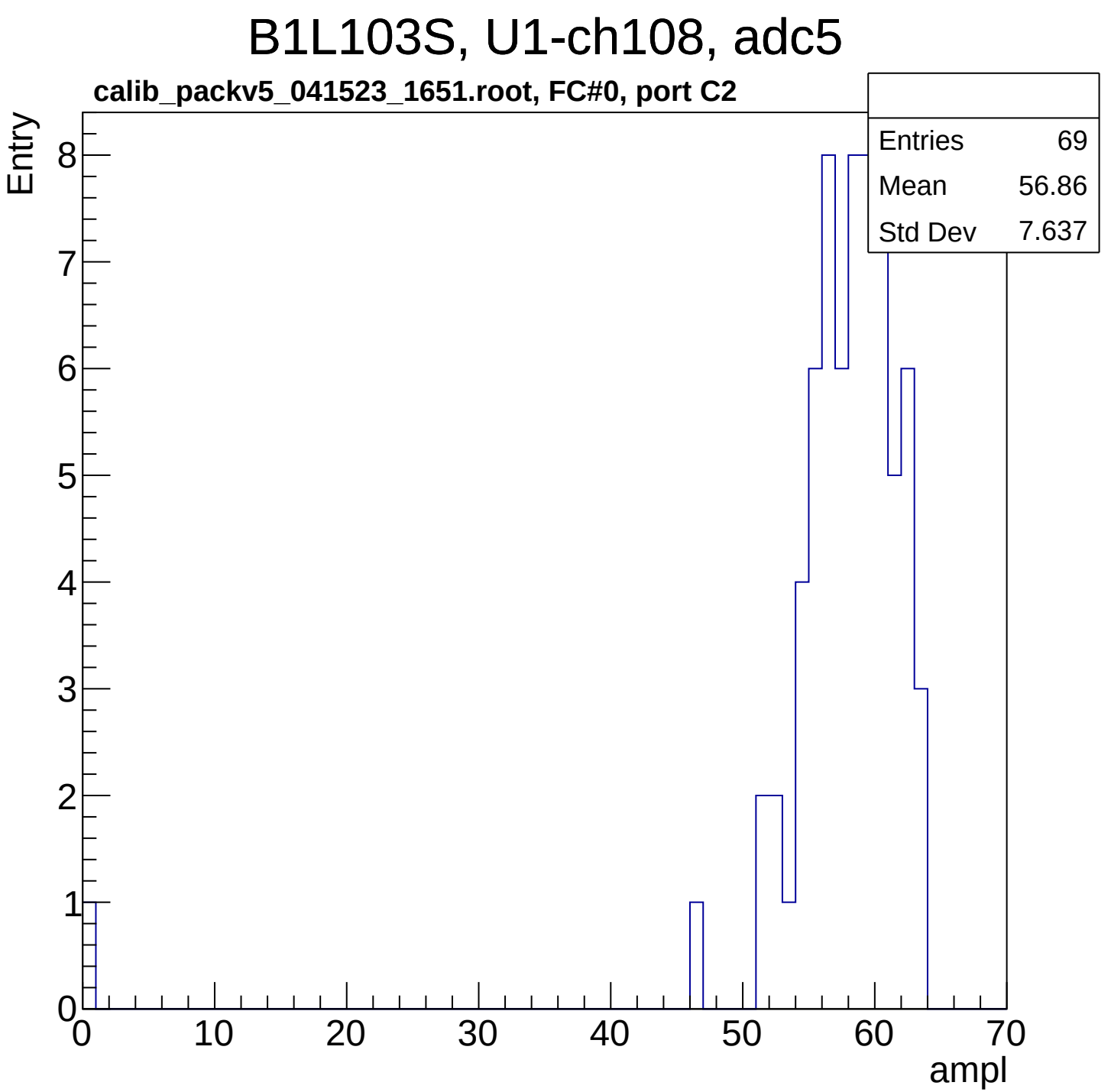
B1L103S, U1-ch108, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 56.86
Std Dev 7.637
Entry
ampl
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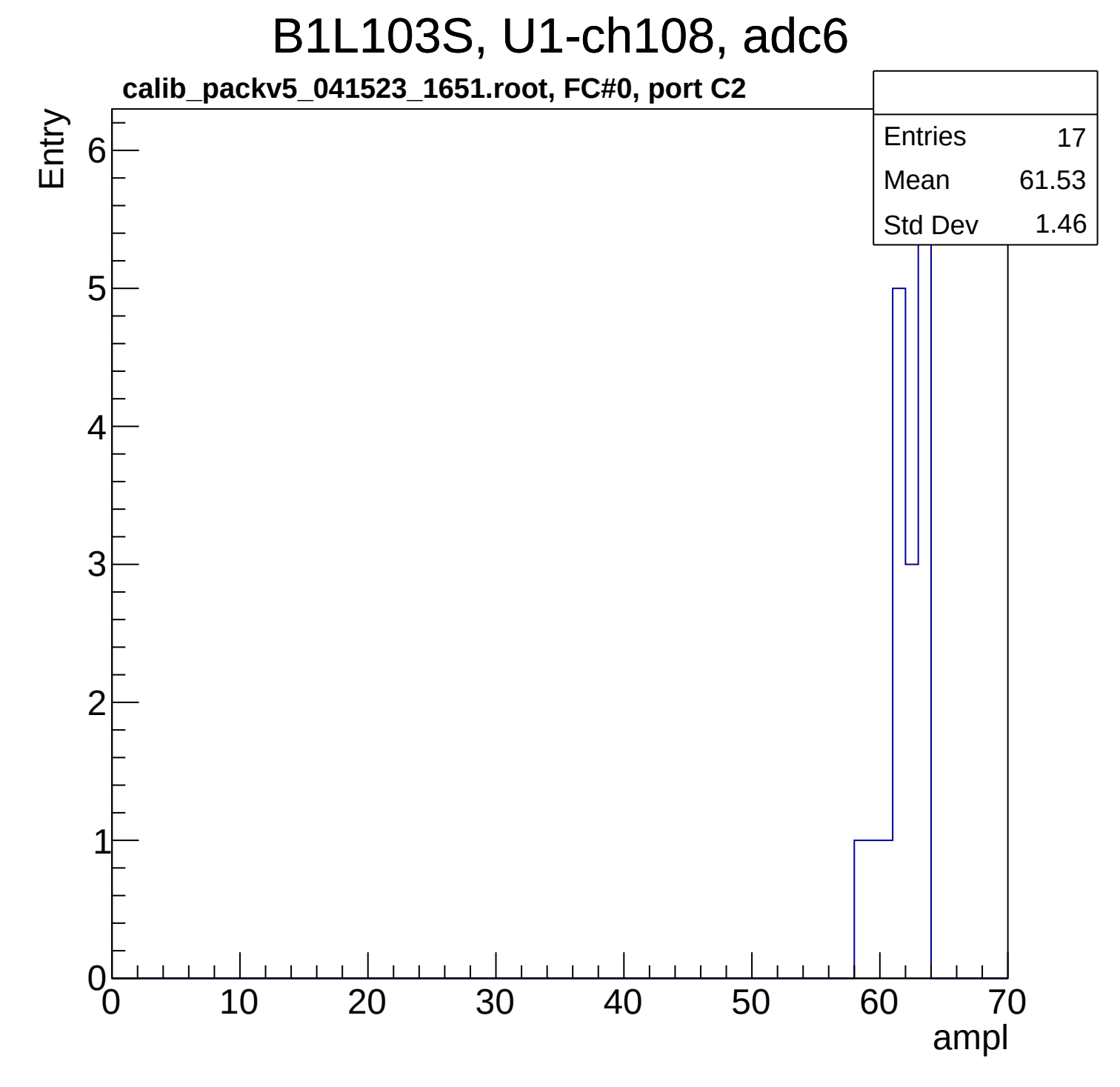
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U1-ch108, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 17
Mean 61.53
Std Dev 1.46
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
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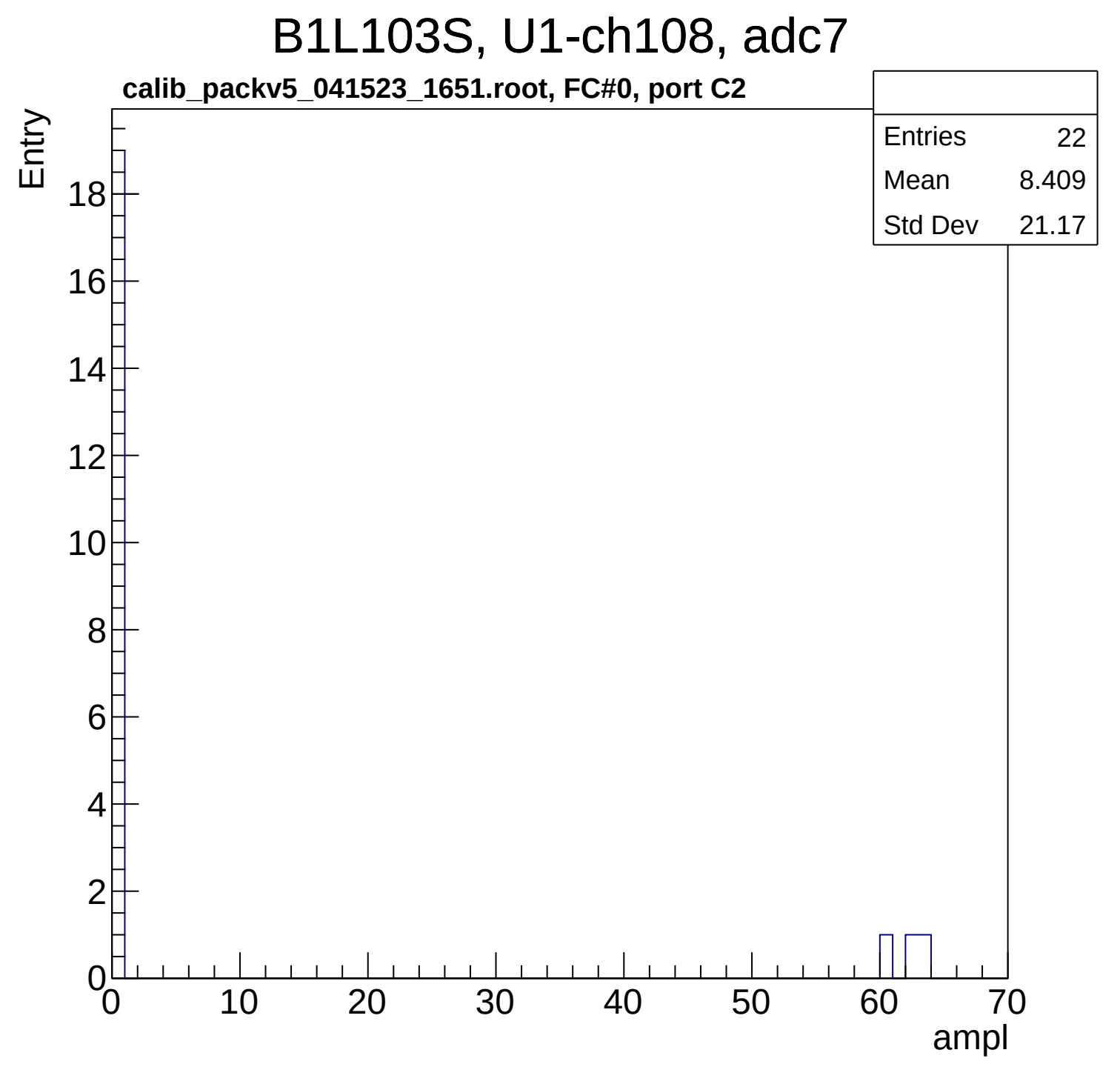
B1L103S, U1-ch108, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 8.409
Std Dev 21.17
Entry
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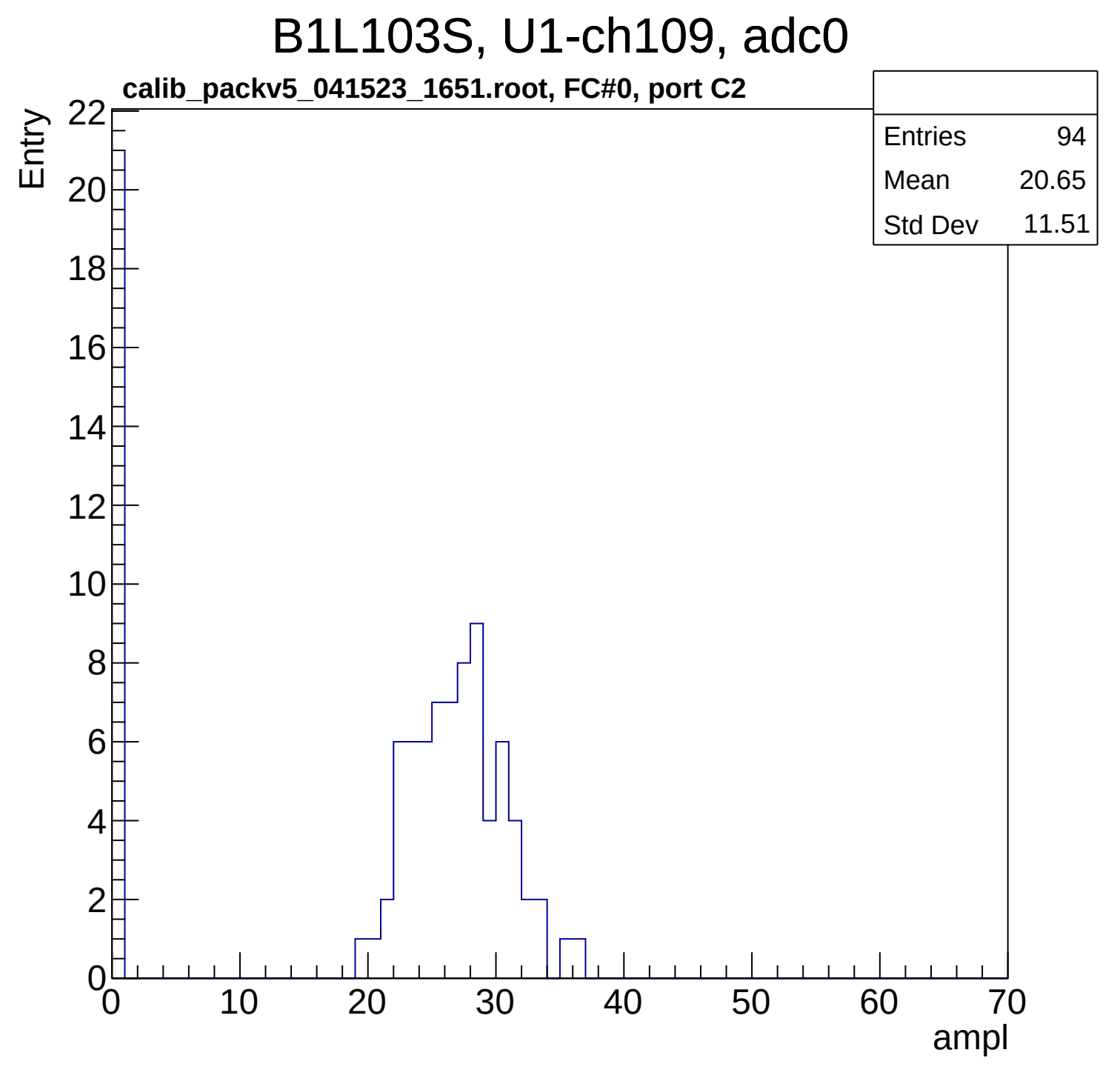
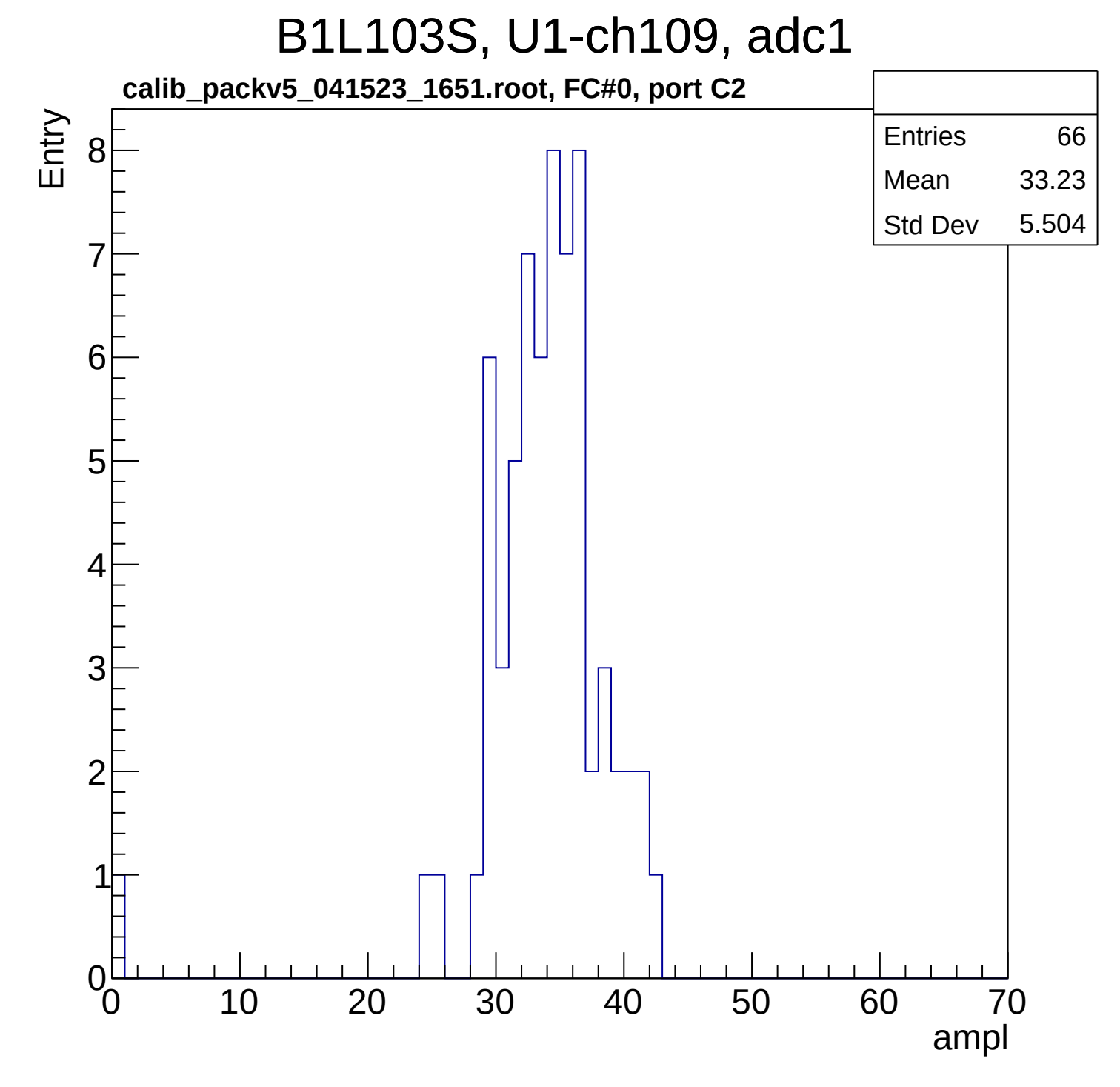
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch109, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 94
Mean 20.65
Std Dev 11.51
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
22
0
10
20
30
40
50
60
70


B1L103S, U1-ch109, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 33.23
Std Dev 5.504
Entry
ampl
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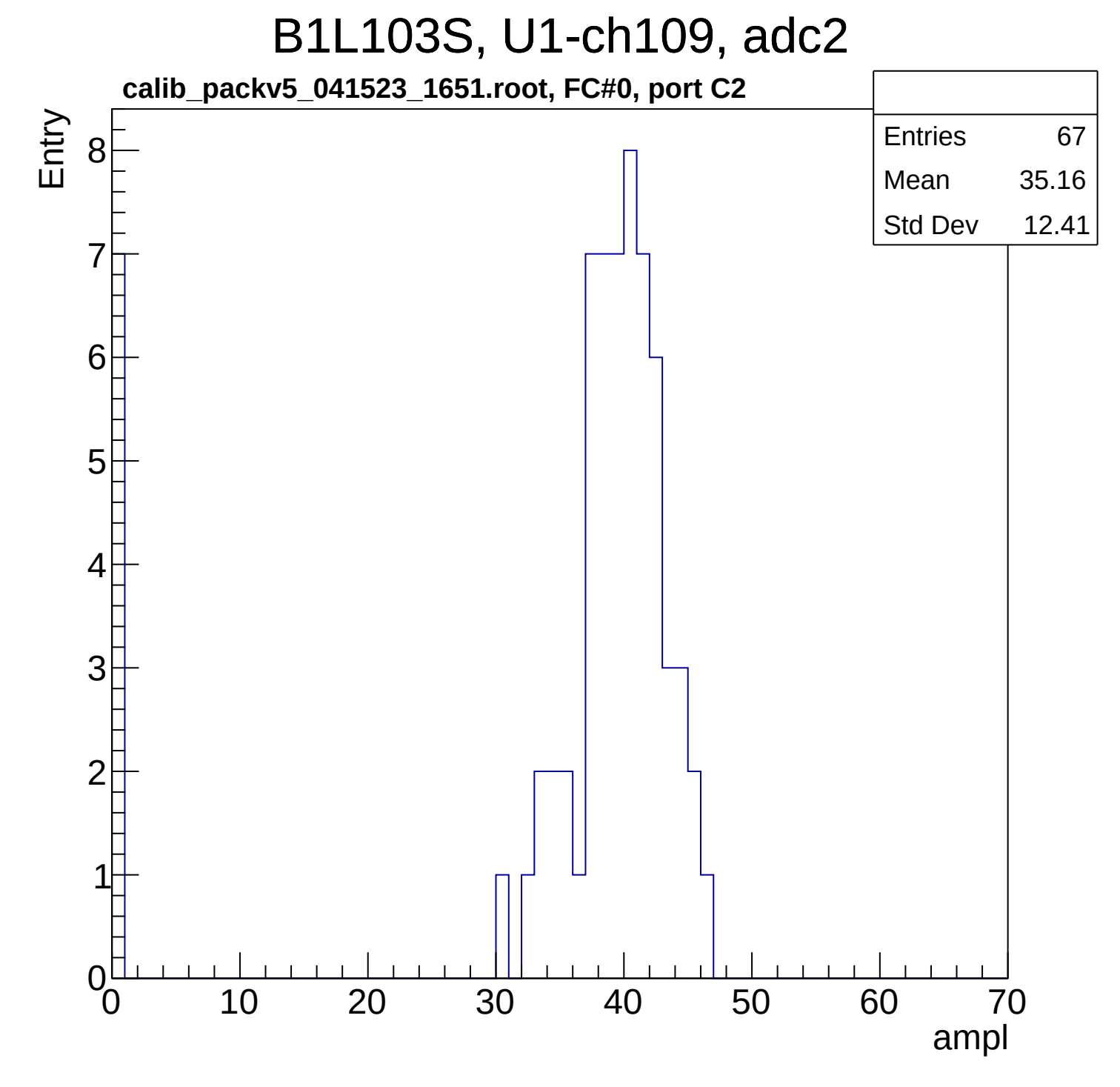
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U1-ch109, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 35.16
Std Dev 12.41
Entry
ampl
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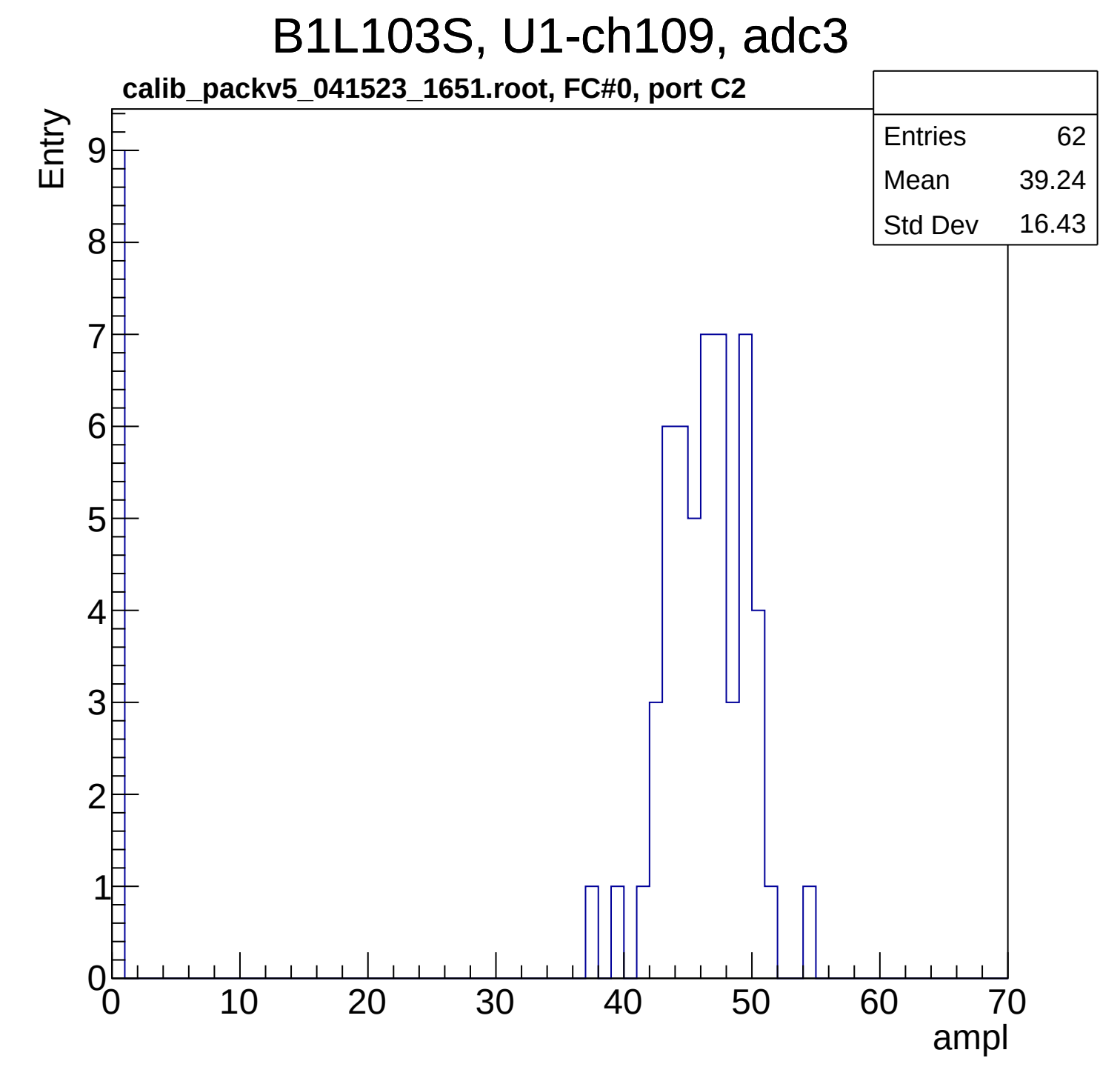
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U1-ch109, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 39.24
Std Dev 16.43
Entry
ampl
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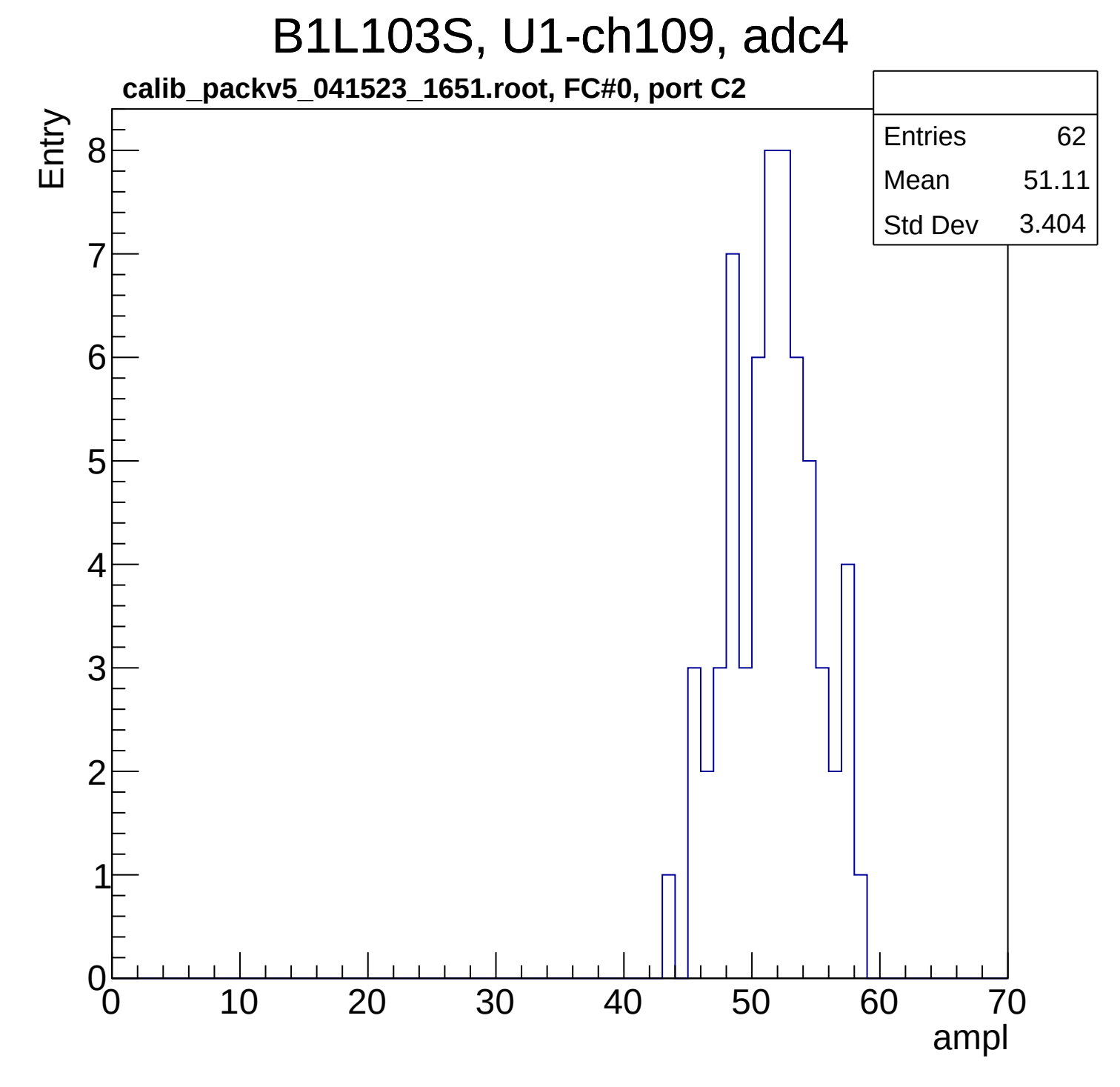
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U1-ch109, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 51.11
Std Dev 3.404
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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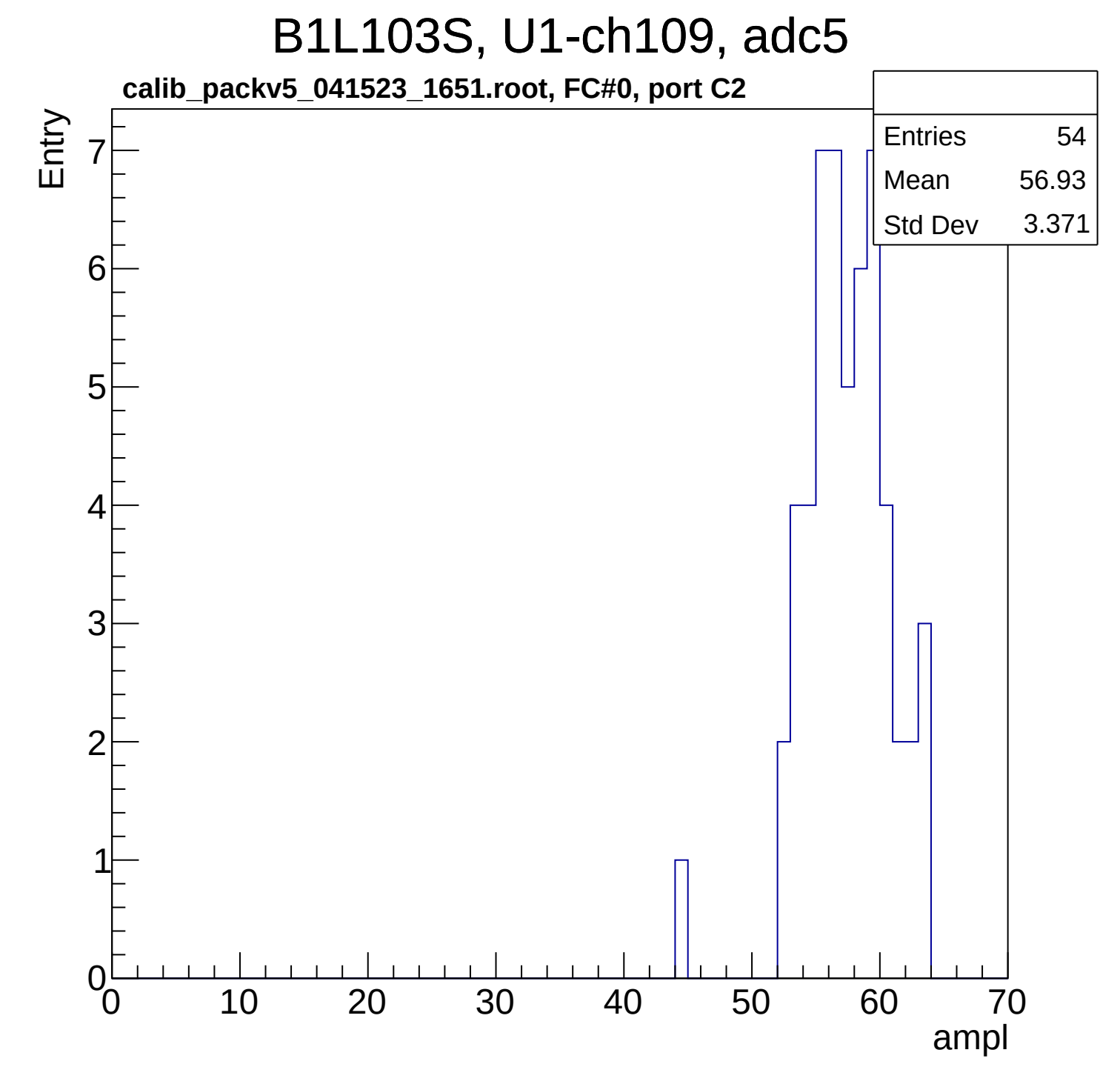
B1L103S, U1-ch109, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 56.93
Std Dev 3.371
Entry
ampl
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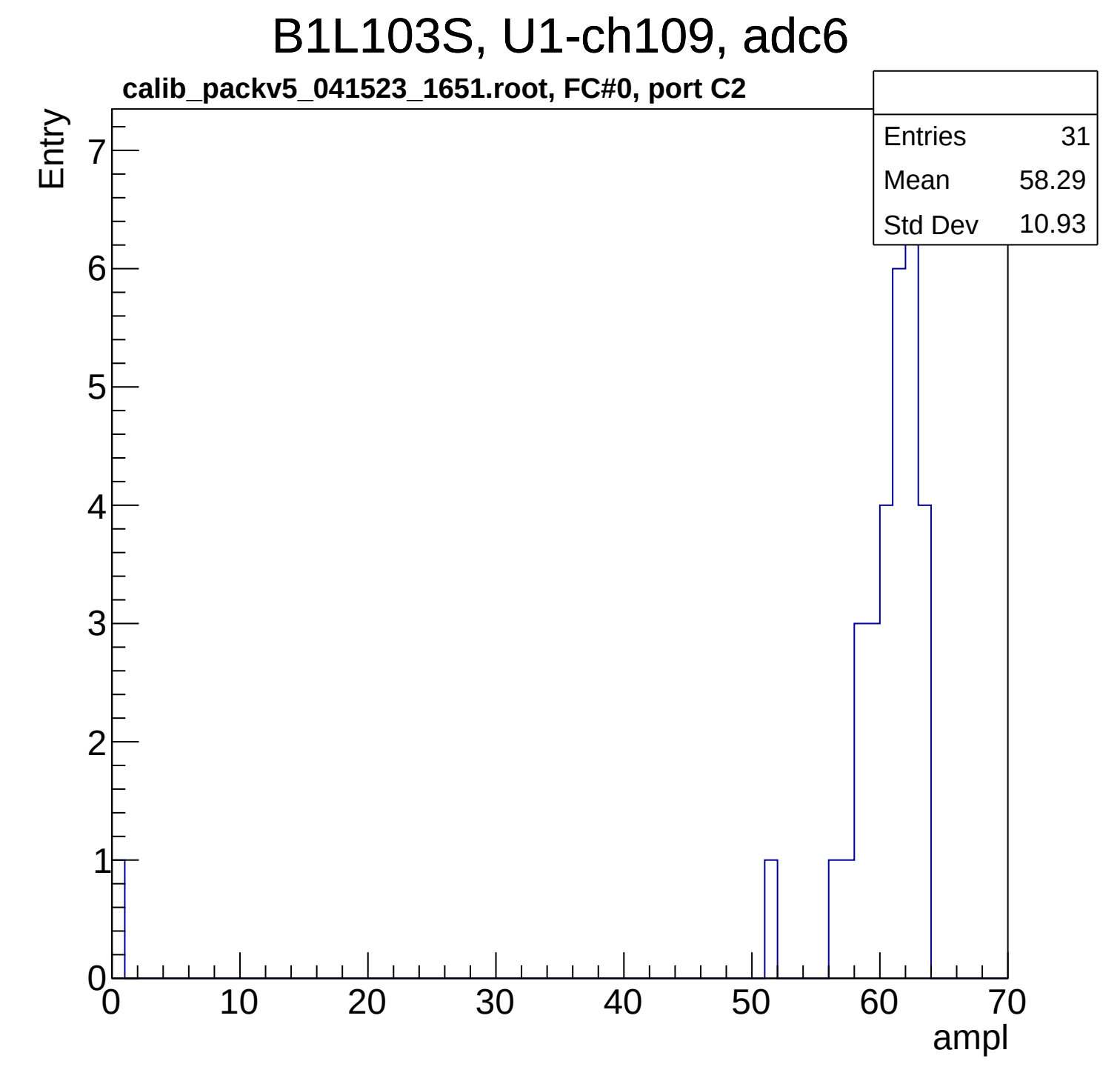
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U1-ch109, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 31
Mean 58.29
Std Dev 10.93
Entry
ampl
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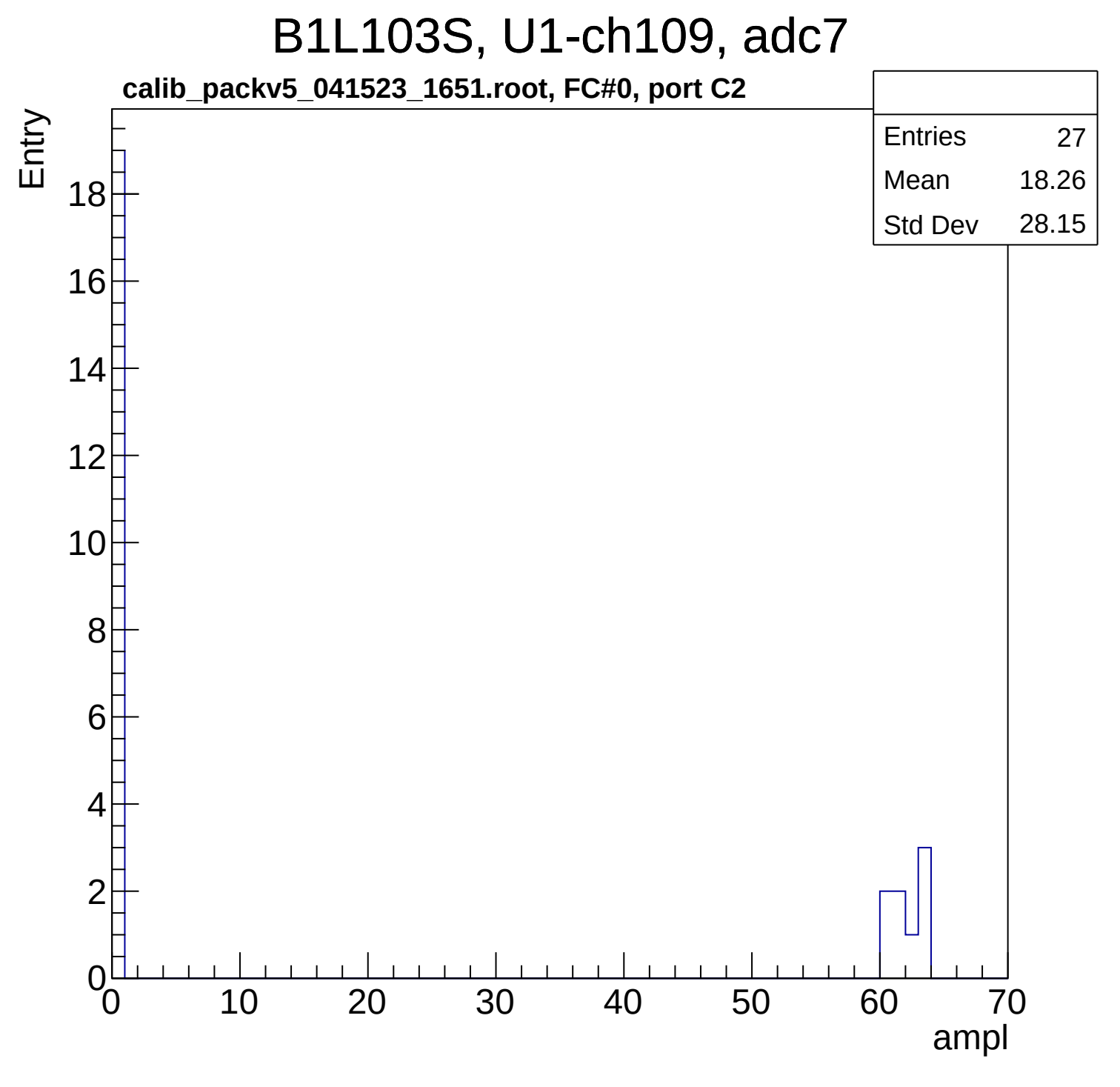
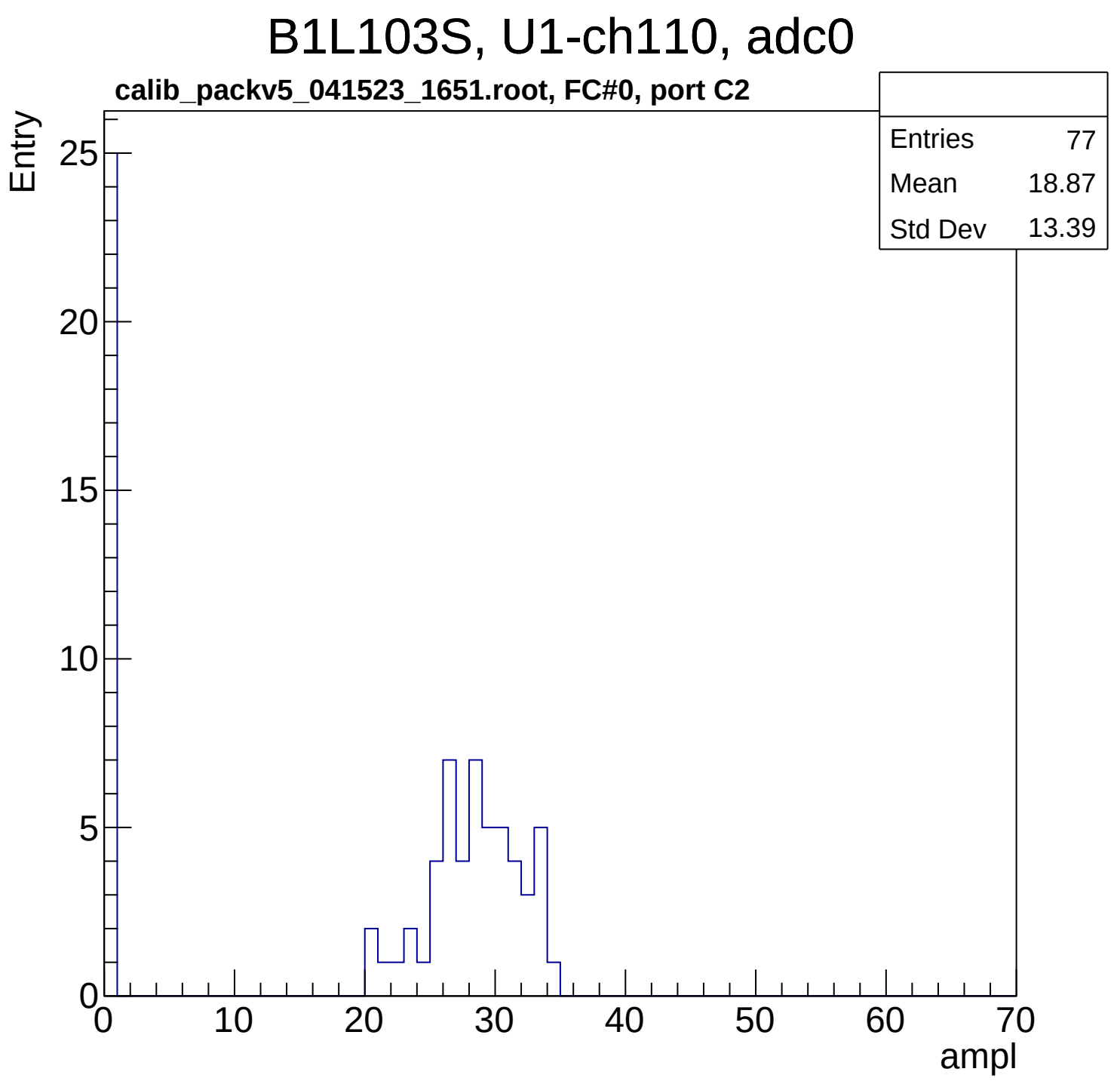
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U1-ch109, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 27
Mean 18.26
Std Dev 28.15
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch110, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 18.87
Std Dev 13.39
Entry
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5
10
15
20
25
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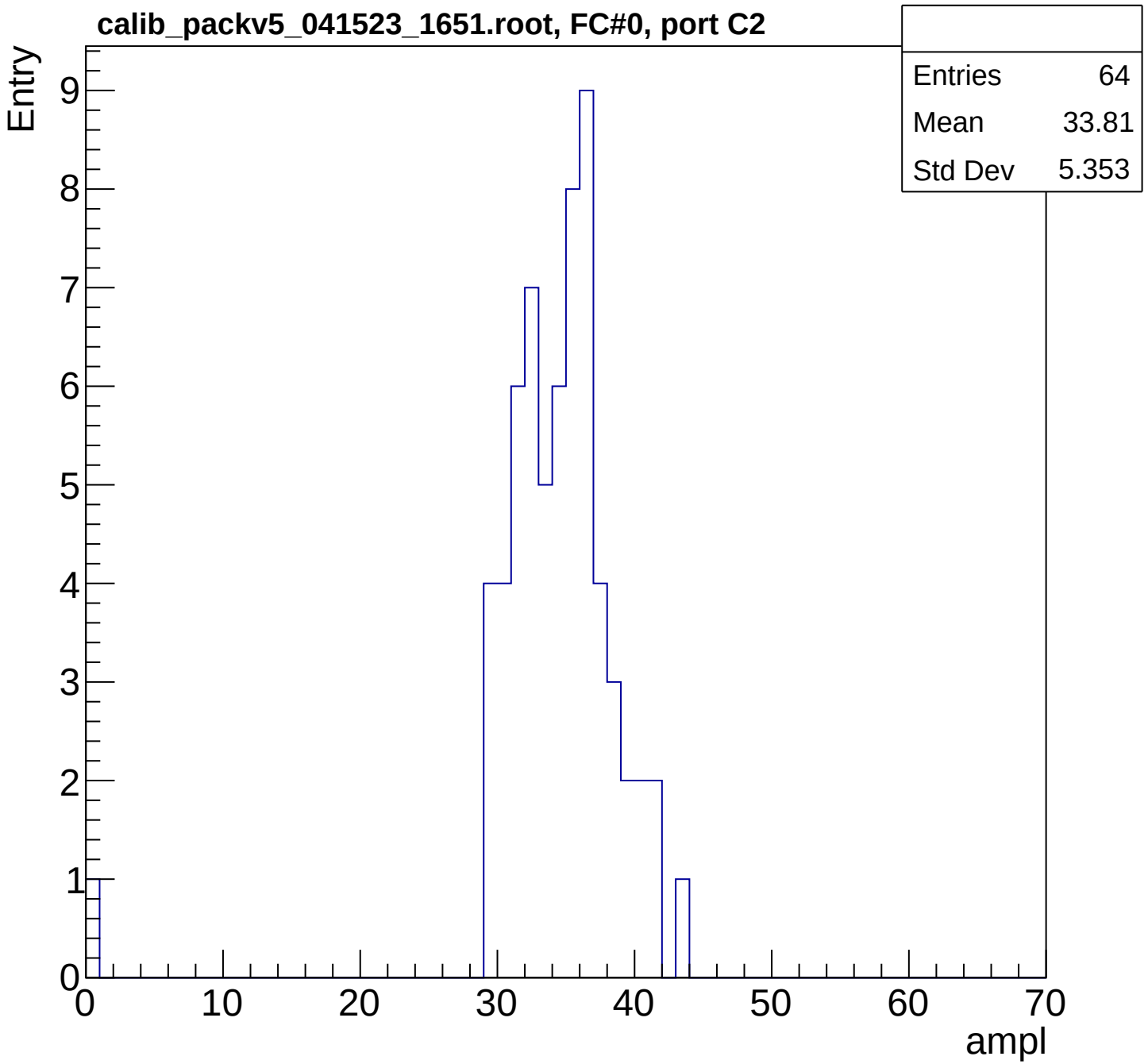
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch110, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 33.81
Std Dev 5.353
Entry
ampl
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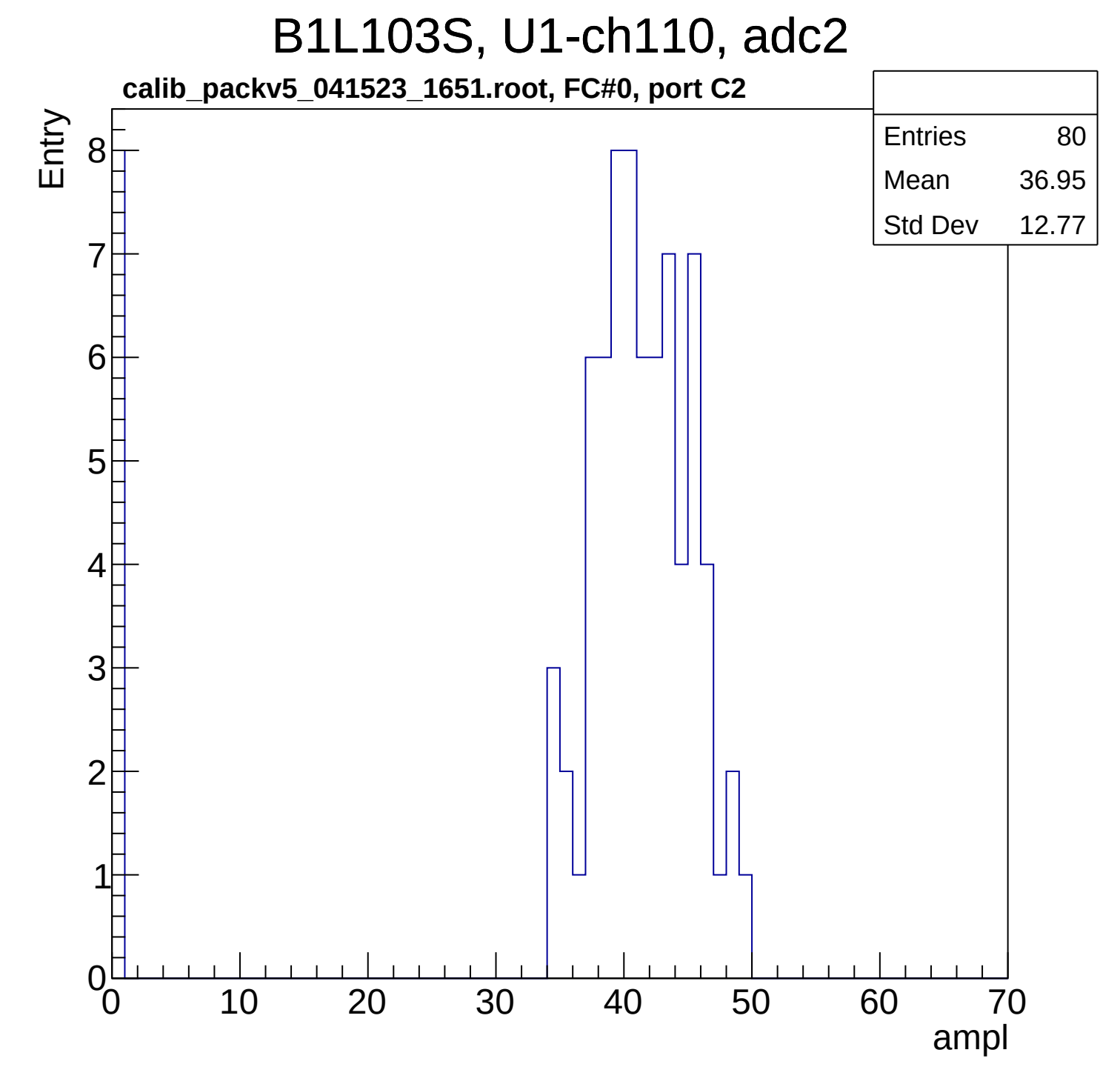
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U1-ch110, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 36.95
Std Dev 12.77
Entry
ampl
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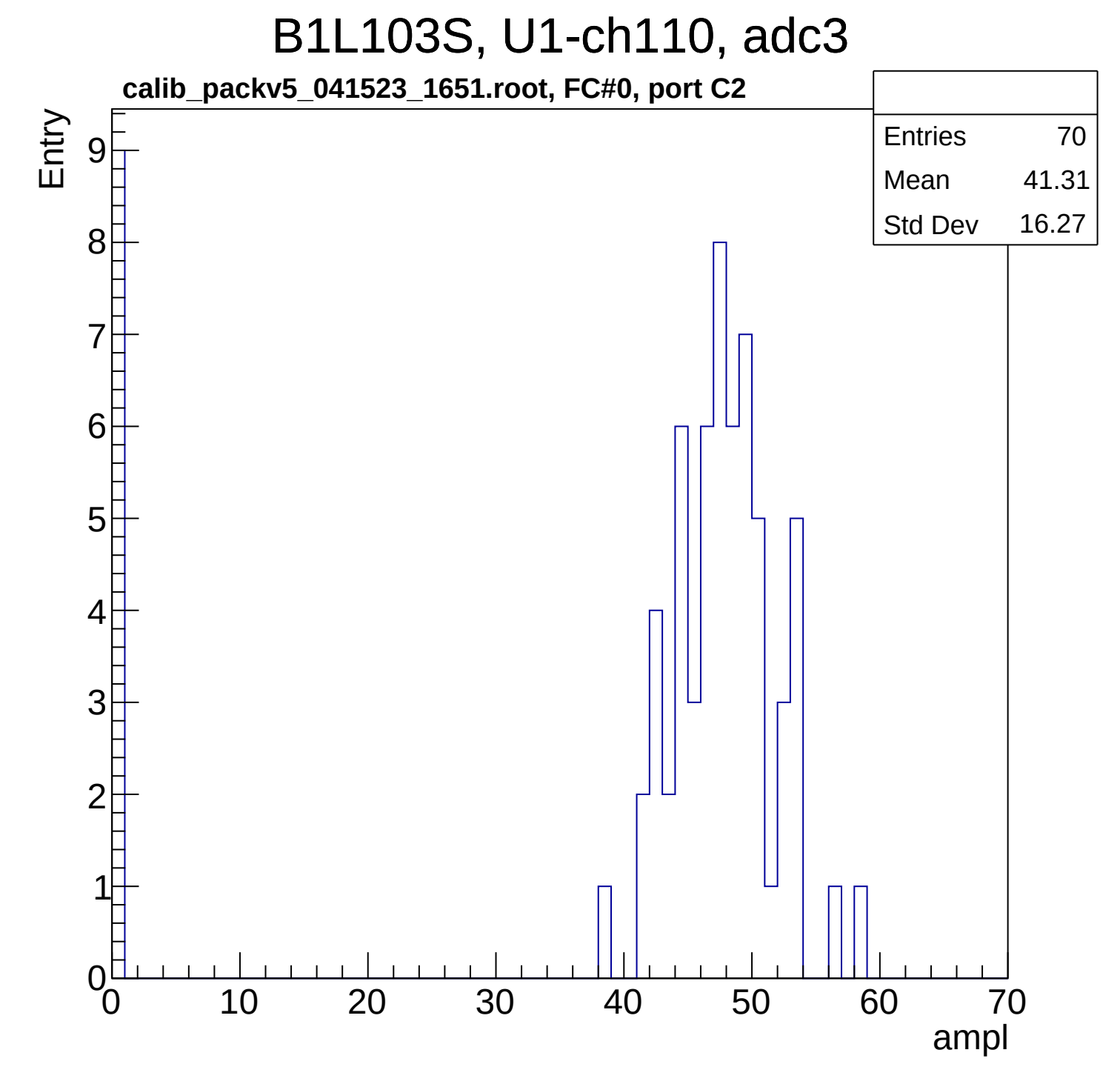
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U1-ch110, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 41.31
Std Dev 16.27
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
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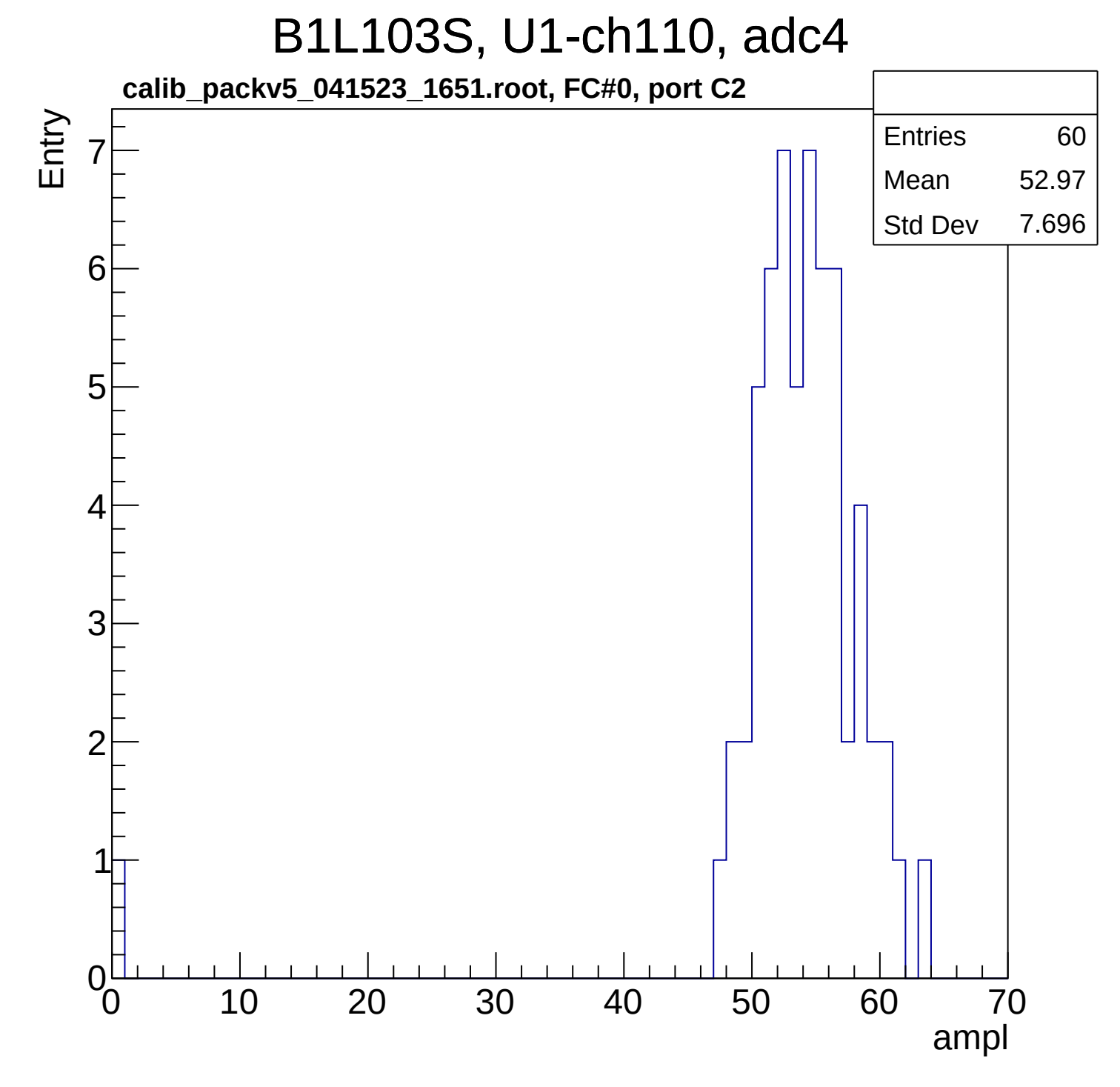
60
70


B1L103S, U1-ch110, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 52.97
Std Dev 7.696
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
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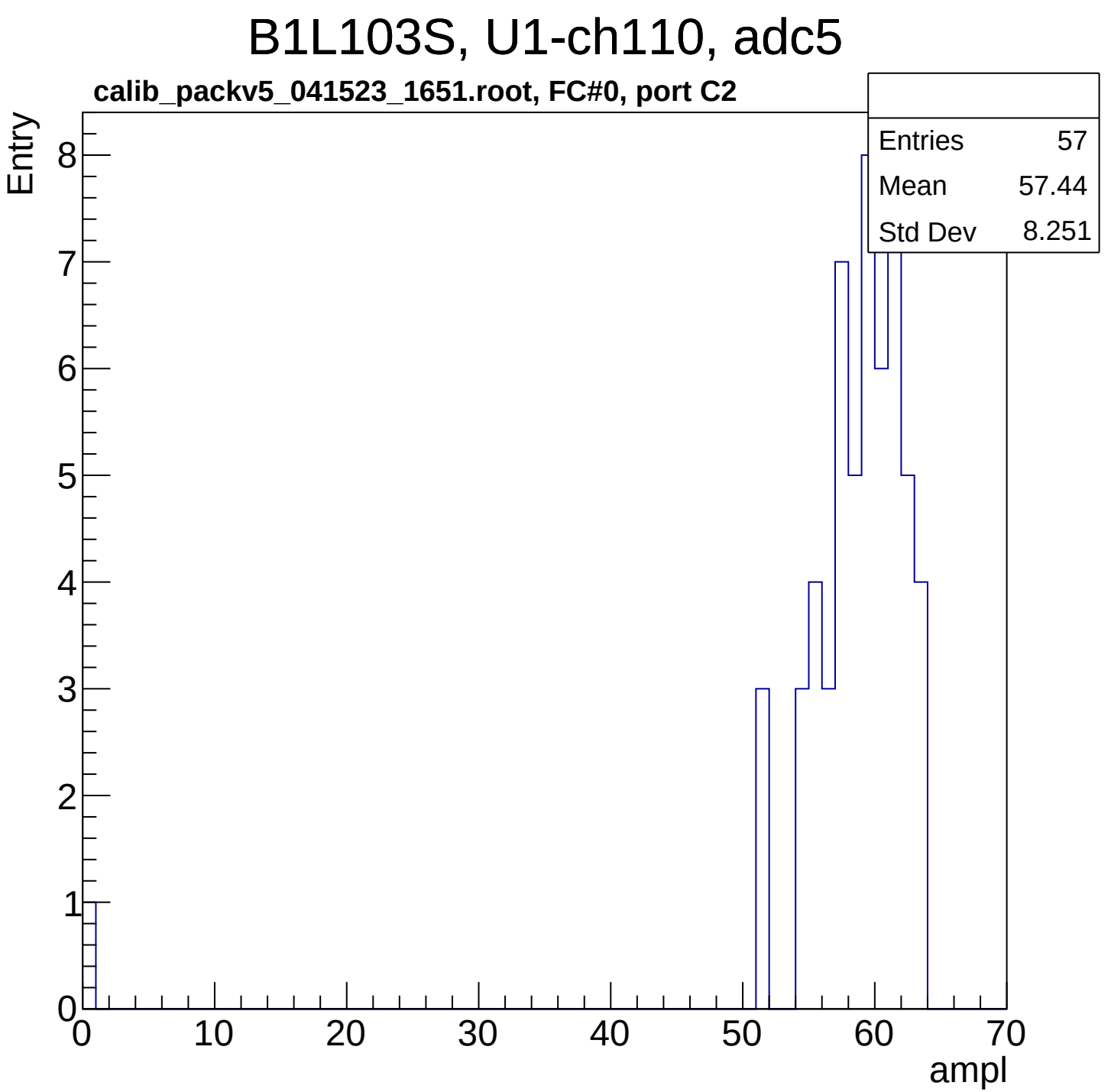
40
50
60
70


B1L103S, U1-ch110, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 57.44
Std Dev 8.251
Entry
ampl
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4
5
6
7
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0
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20
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60
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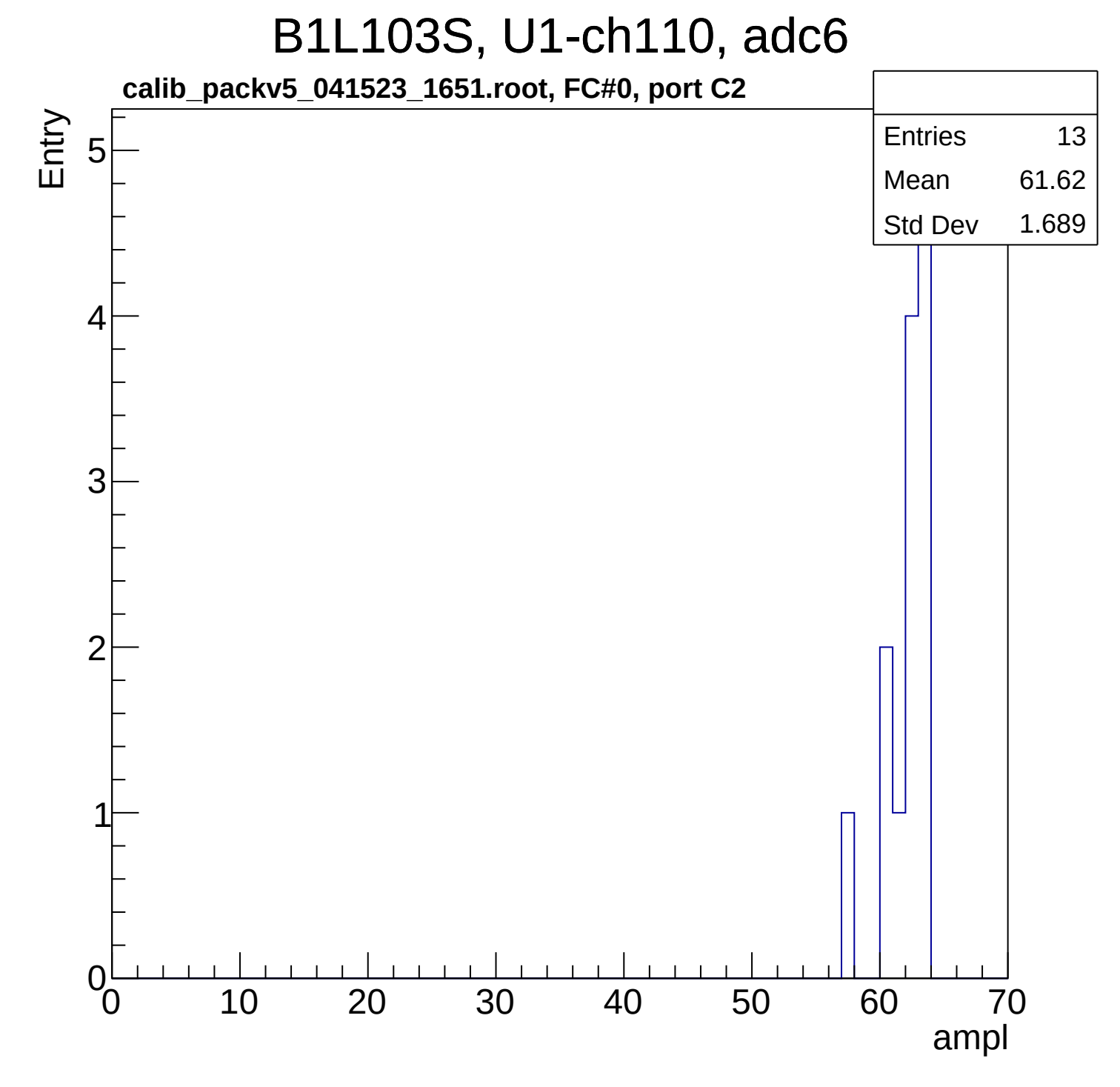
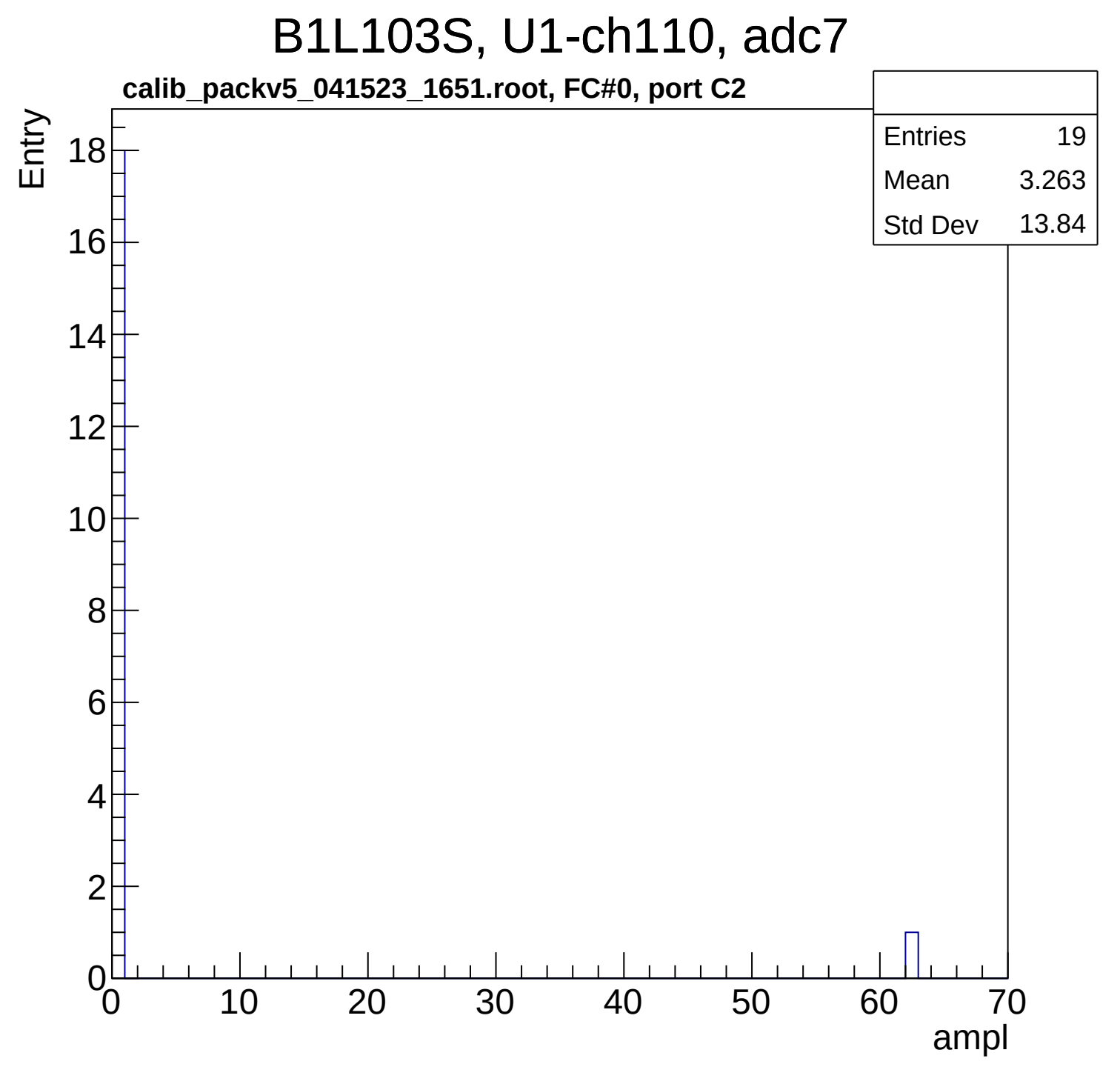

B1L103S, U1-ch110, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 13
Mean 61.62
Std Dev 1.689
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U1-ch110, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 3.263
Std Dev 13.84
Entry
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6
8
10
12
14
16
18
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10
20
30
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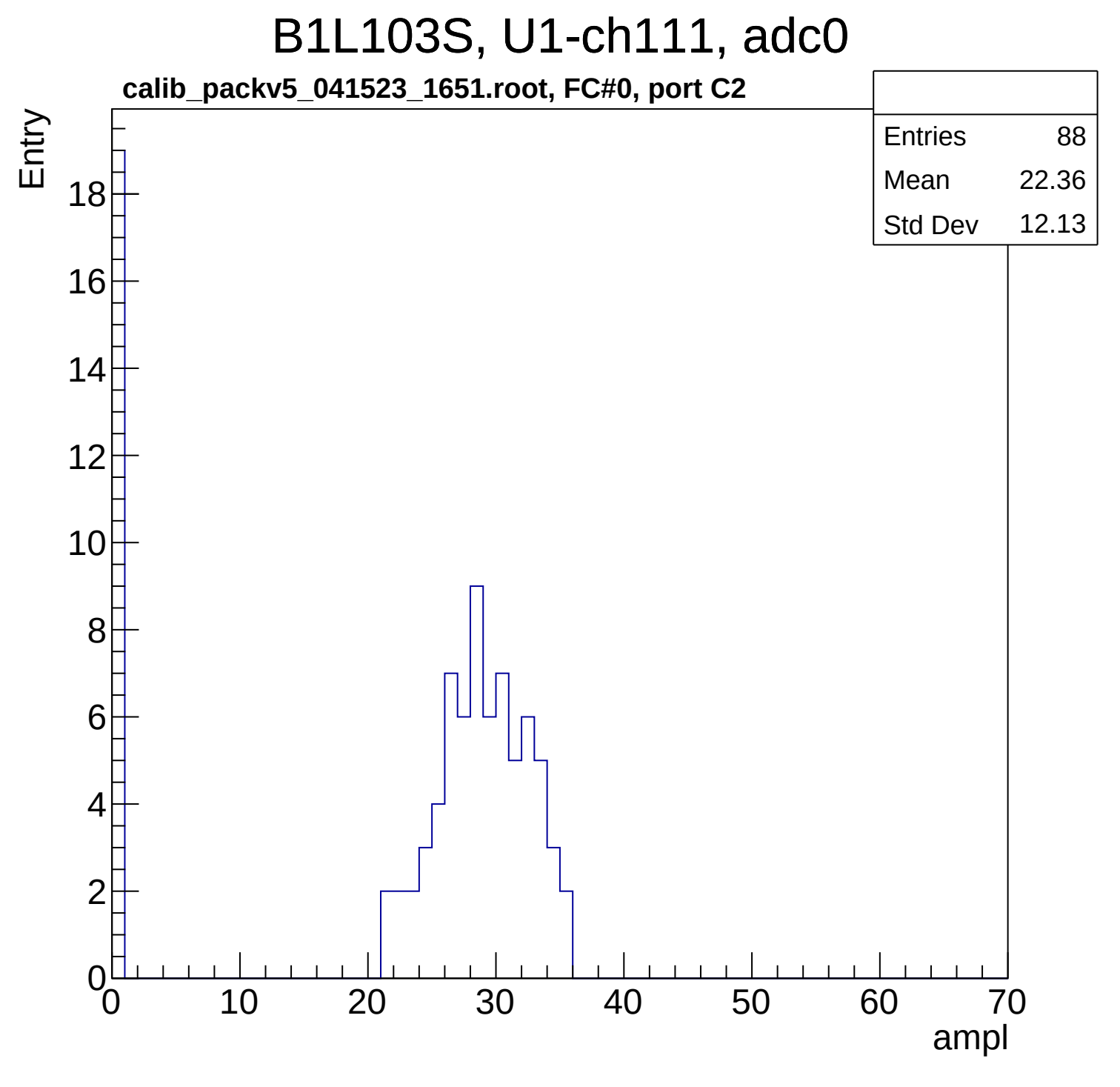
50
60
70
ampl


B1L103S, U1-ch111, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 88
Mean 22.36
Std Dev 12.13
Entry
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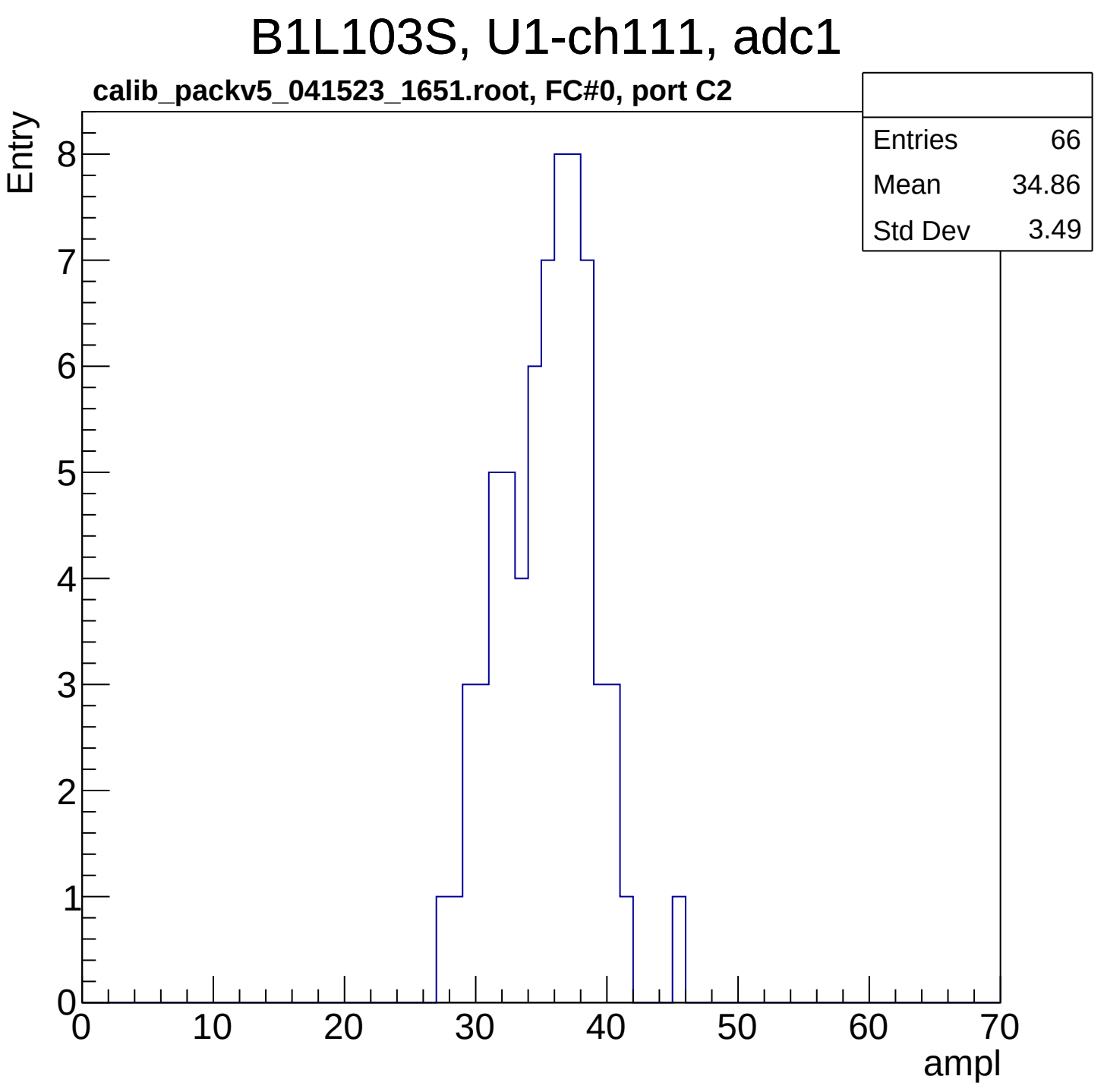
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch111, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 34.86
Std Dev 3.49
Entry
ampl
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3
4
5
6
7
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0
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40
50
60
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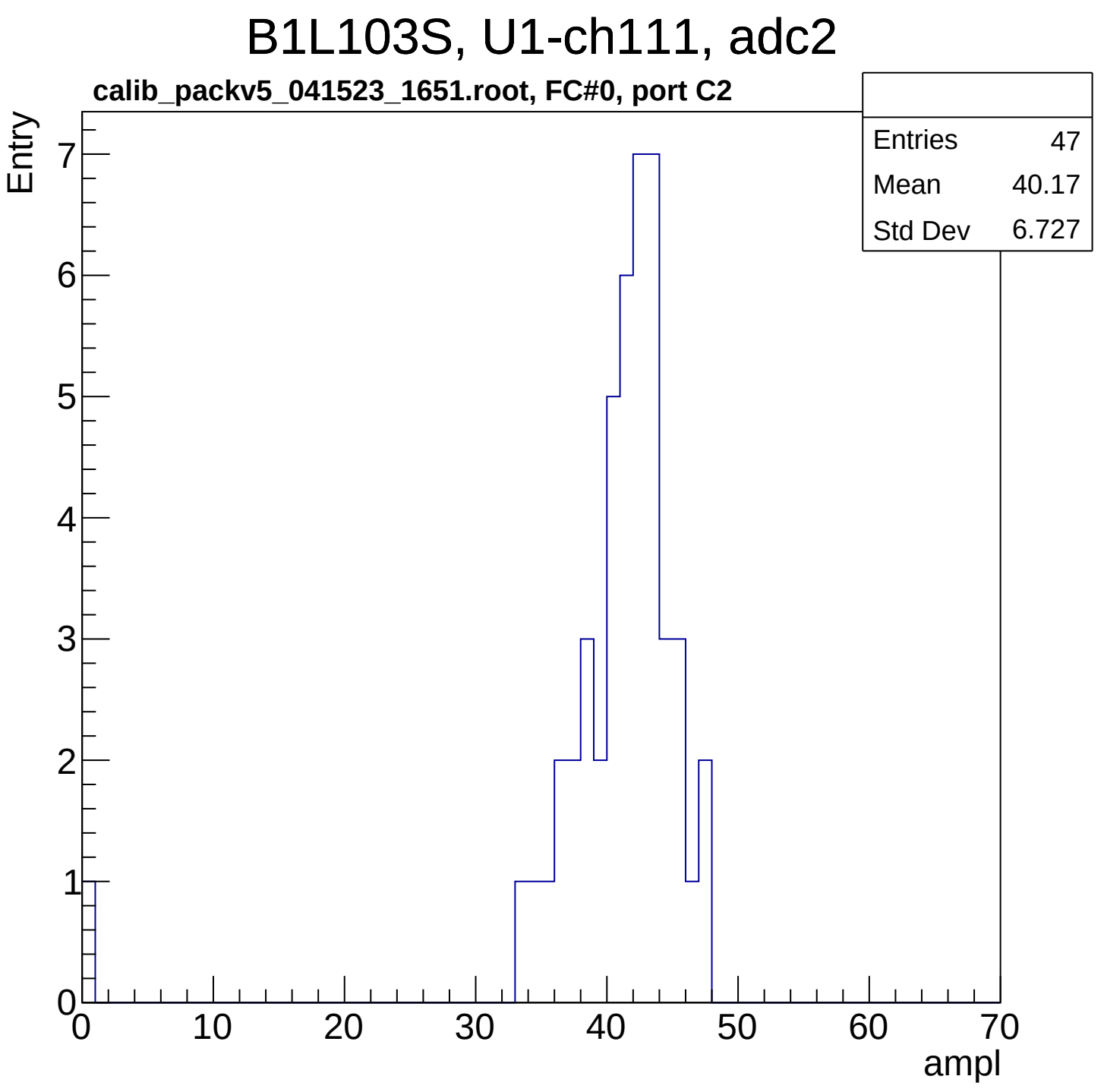
B1L103S, U1-ch111, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 40.17
Std Dev 6.727
Entry
ampl
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1
2
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4
5
6
7
0
10
20
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40
50
60
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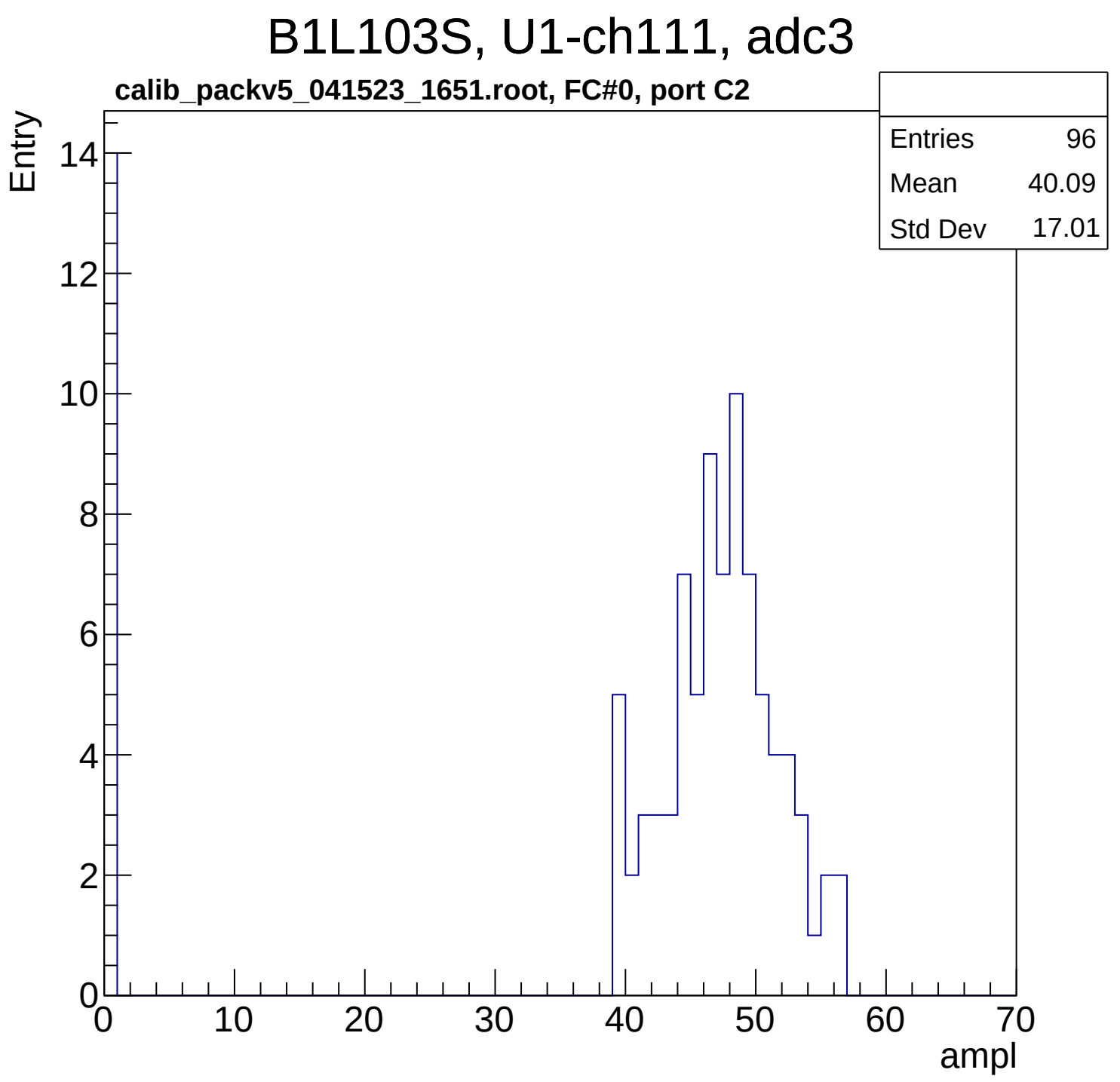
B1L103S, U1-ch111, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 96
Mean 40.09
Std Dev 17.01
Entry
ampl
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2
4
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8
10
12
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0
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20
30
40
50
60
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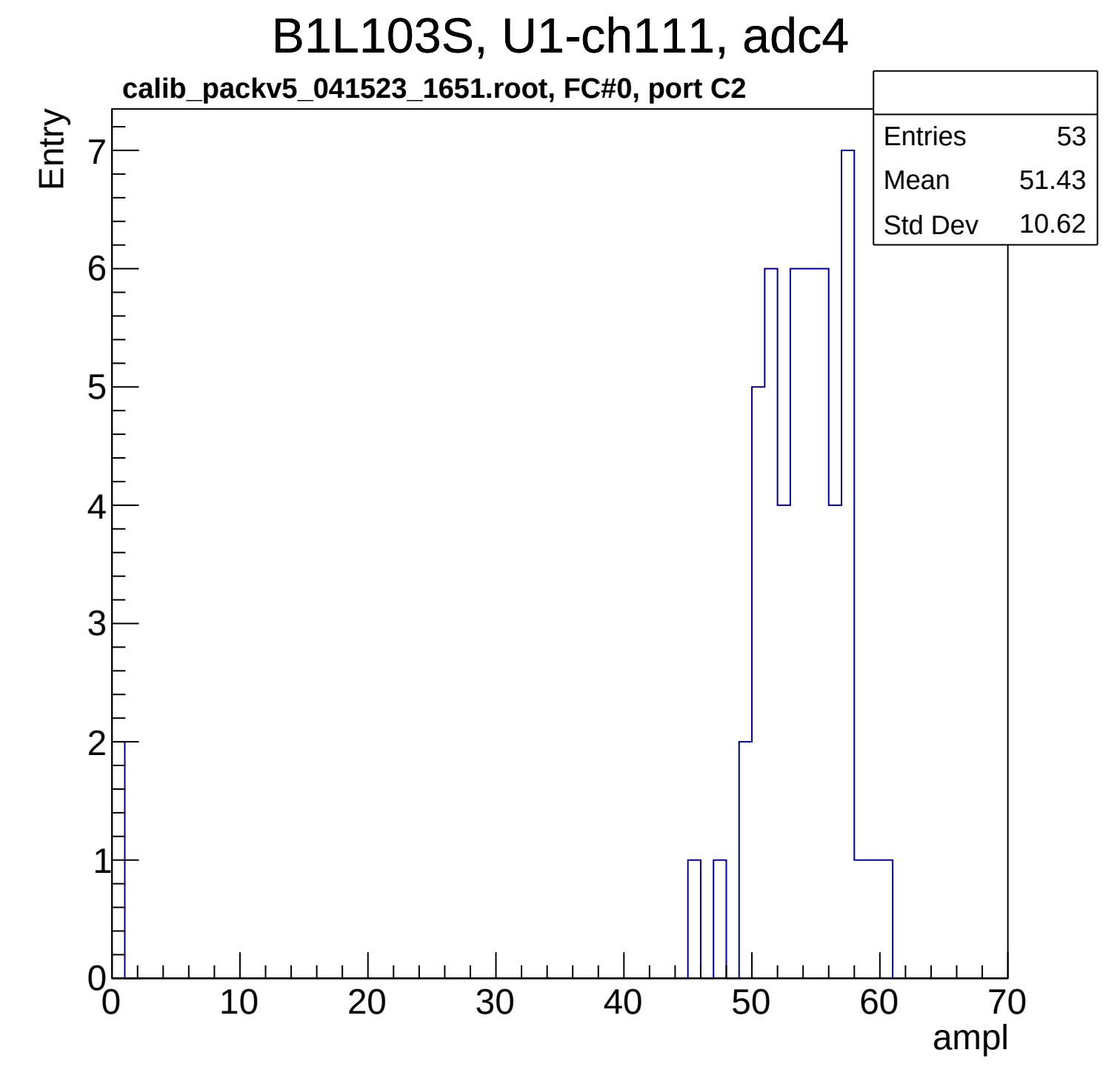
B1L103S, U1-ch111, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 51.43
Std Dev 10.62
Entry
ampl
0
1
2
3
4
5
6
7
0
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20
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40
50
60
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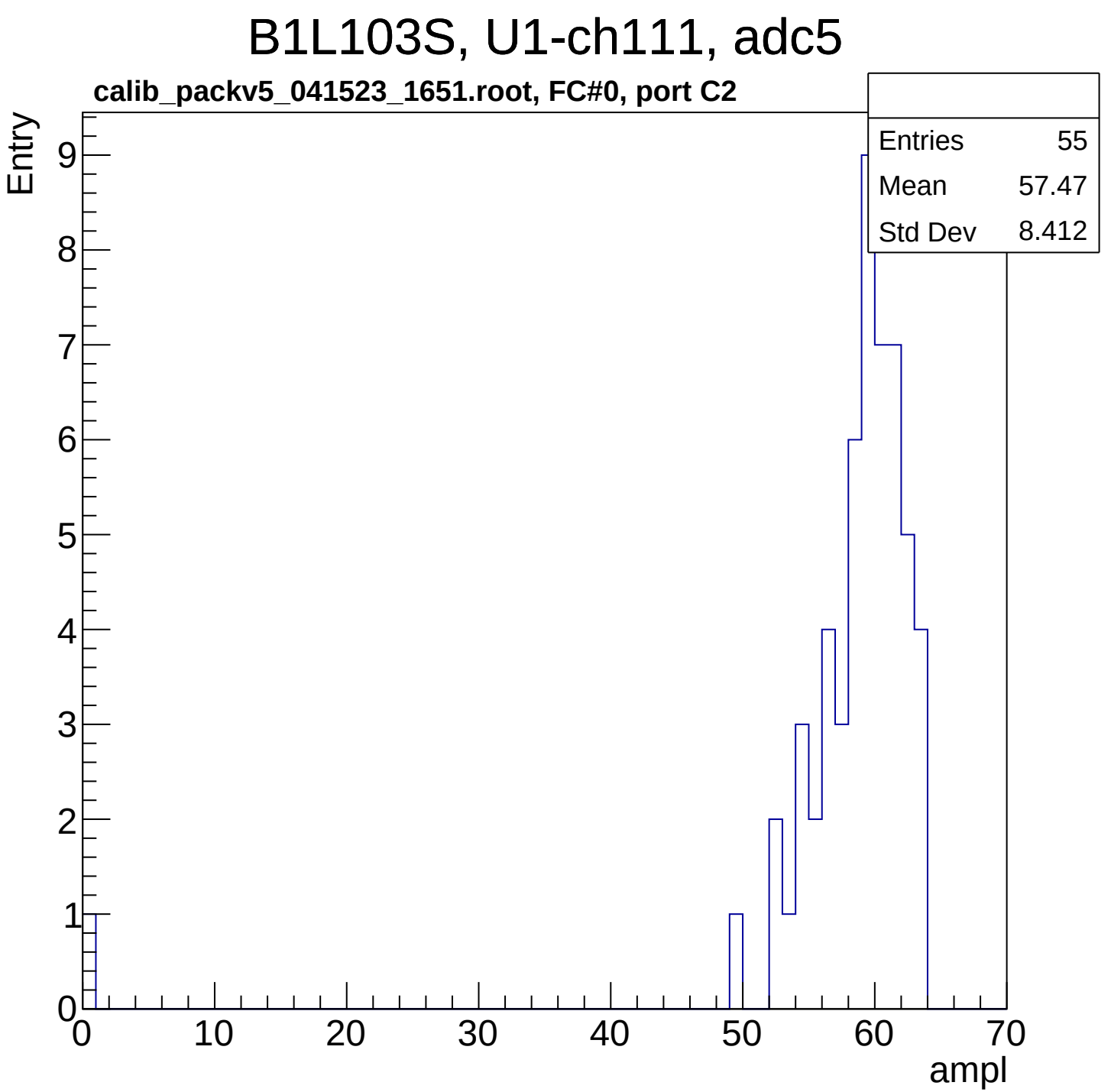
B1L103S, U1-ch111, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 57.47
Std Dev 8.412
Entry
ampl
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2
3
4
5
6
7
8
9
0
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40
50
60
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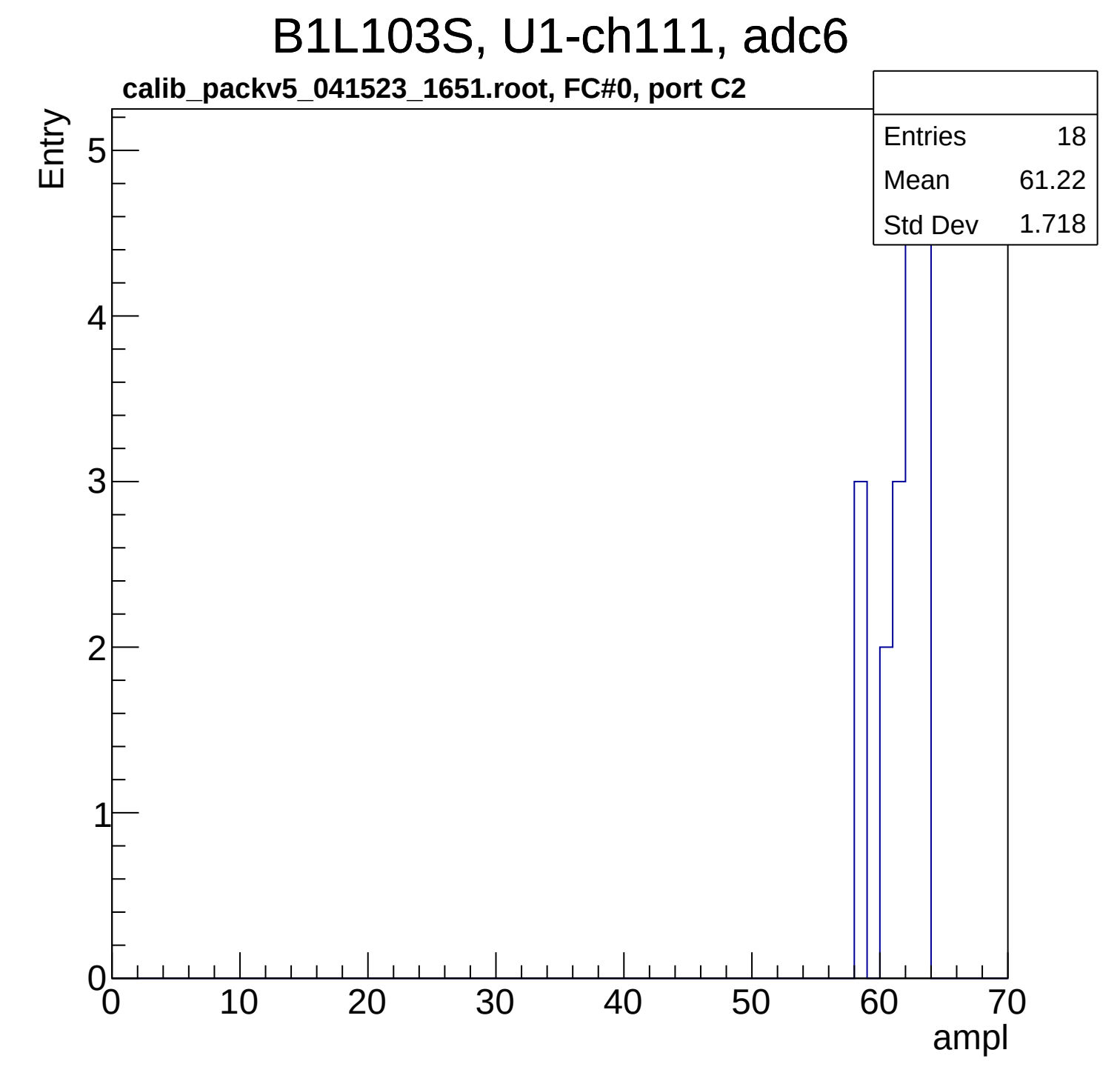
B1L103S, U1-ch111, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 61.22
Std Dev 1.718
Entry
ampl
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2
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4
5
0
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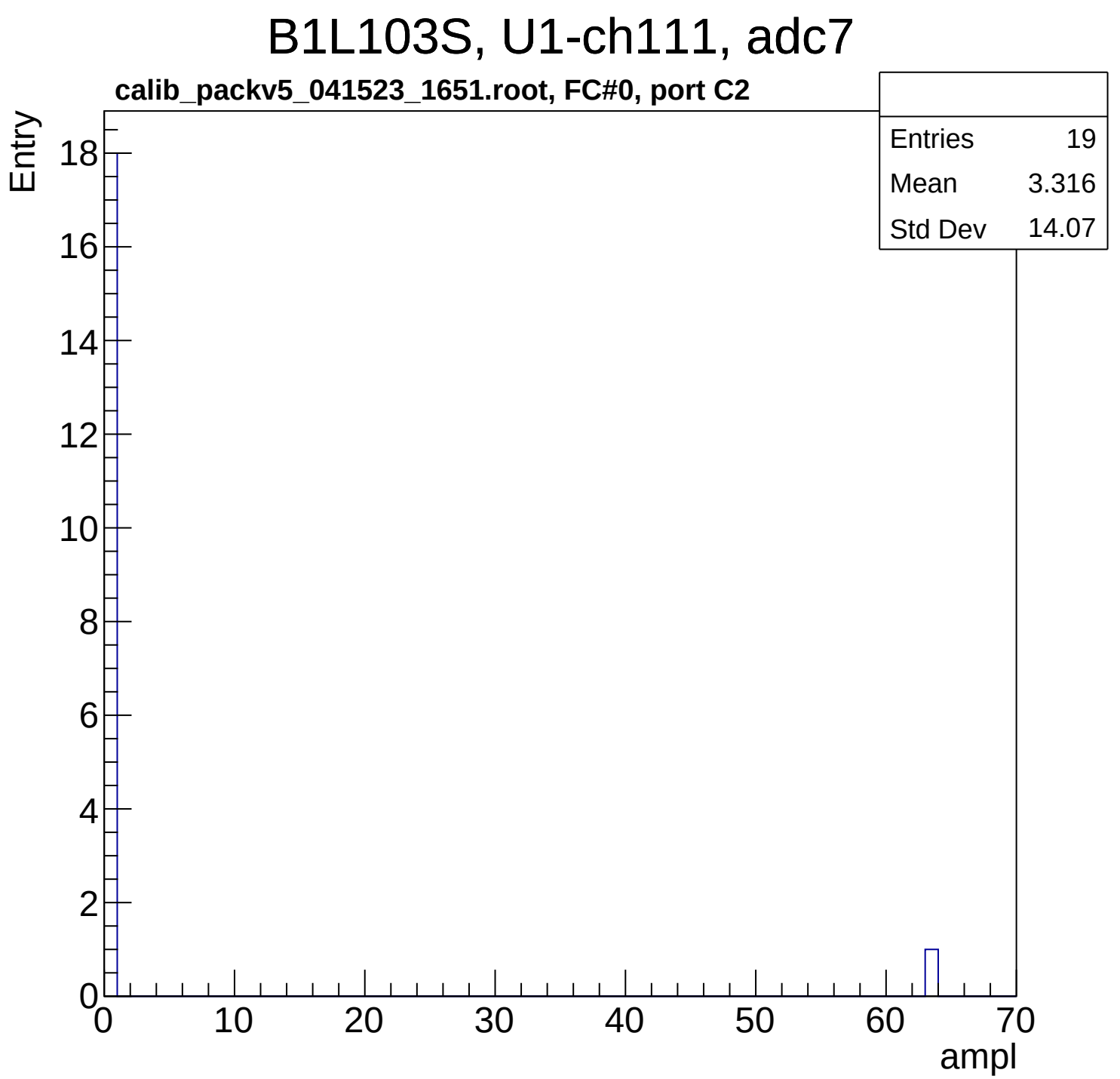
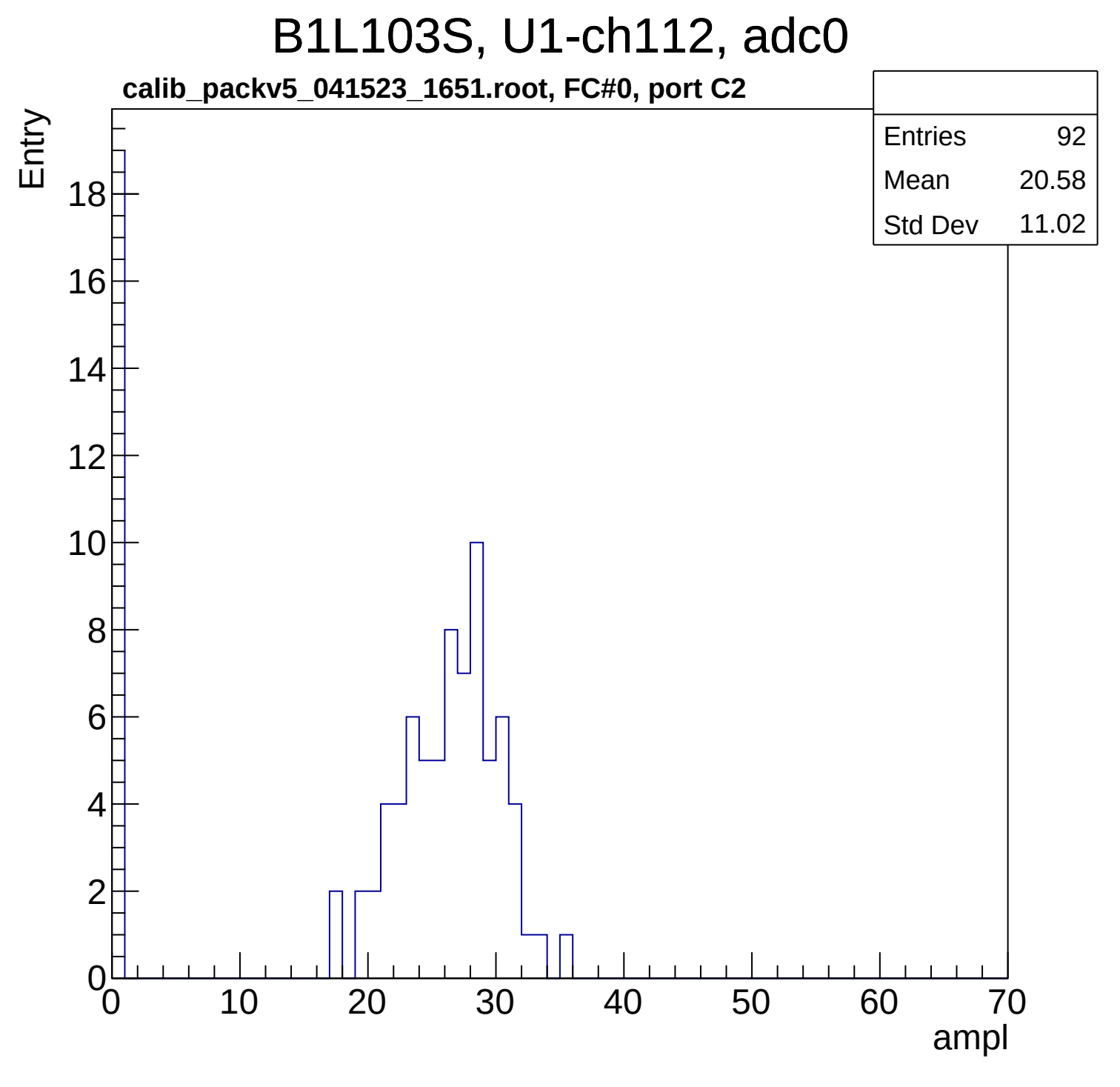
40
50
60
70


B1L103S, U1-ch111, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 3.316
Std Dev 14.07
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch112, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 92
Mean 20.58
Std Dev 11.02
Entry
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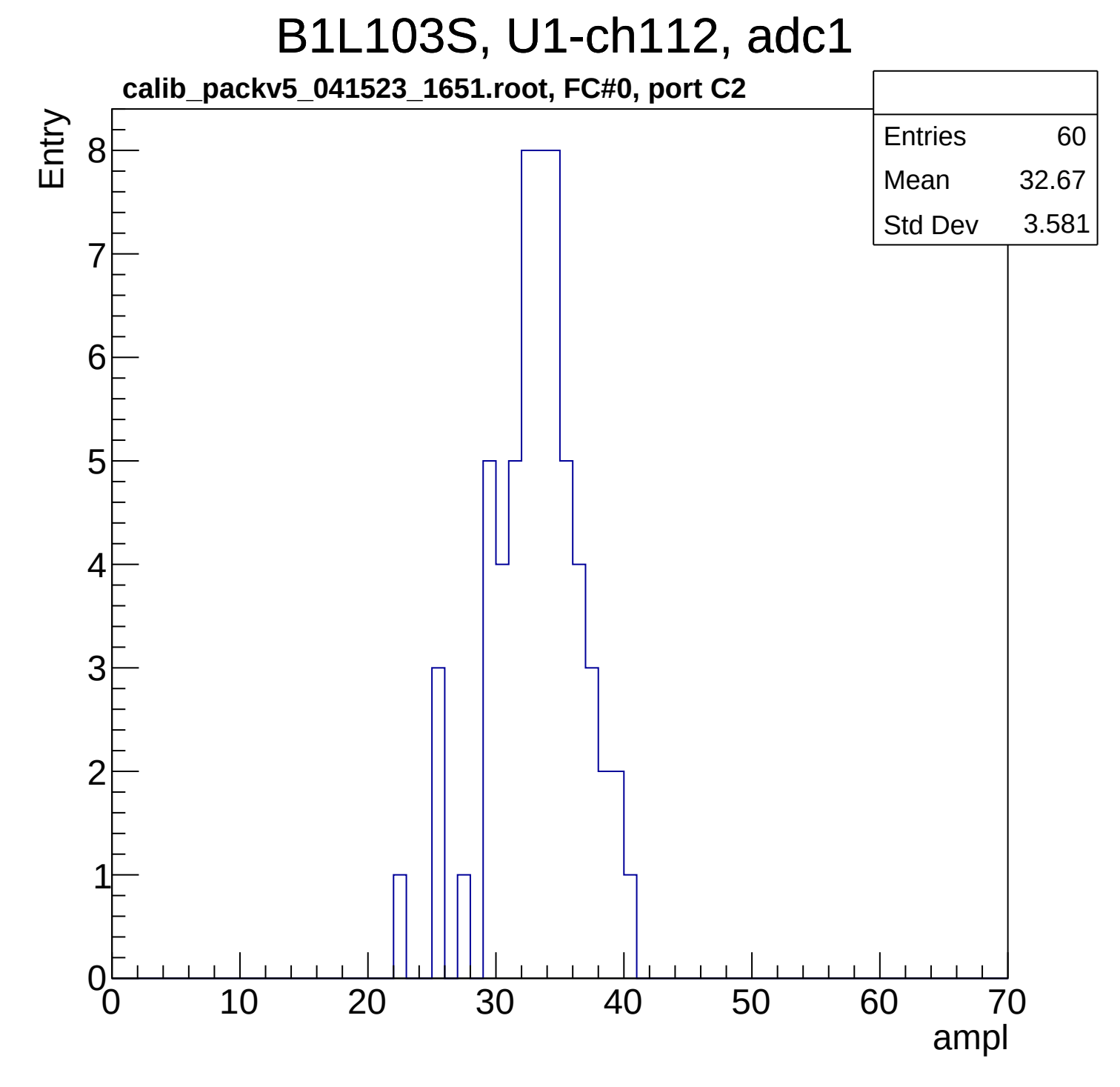
ampl


B1L103S, U1-ch112, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 32.67
Std Dev 3.581
Entry
ampl
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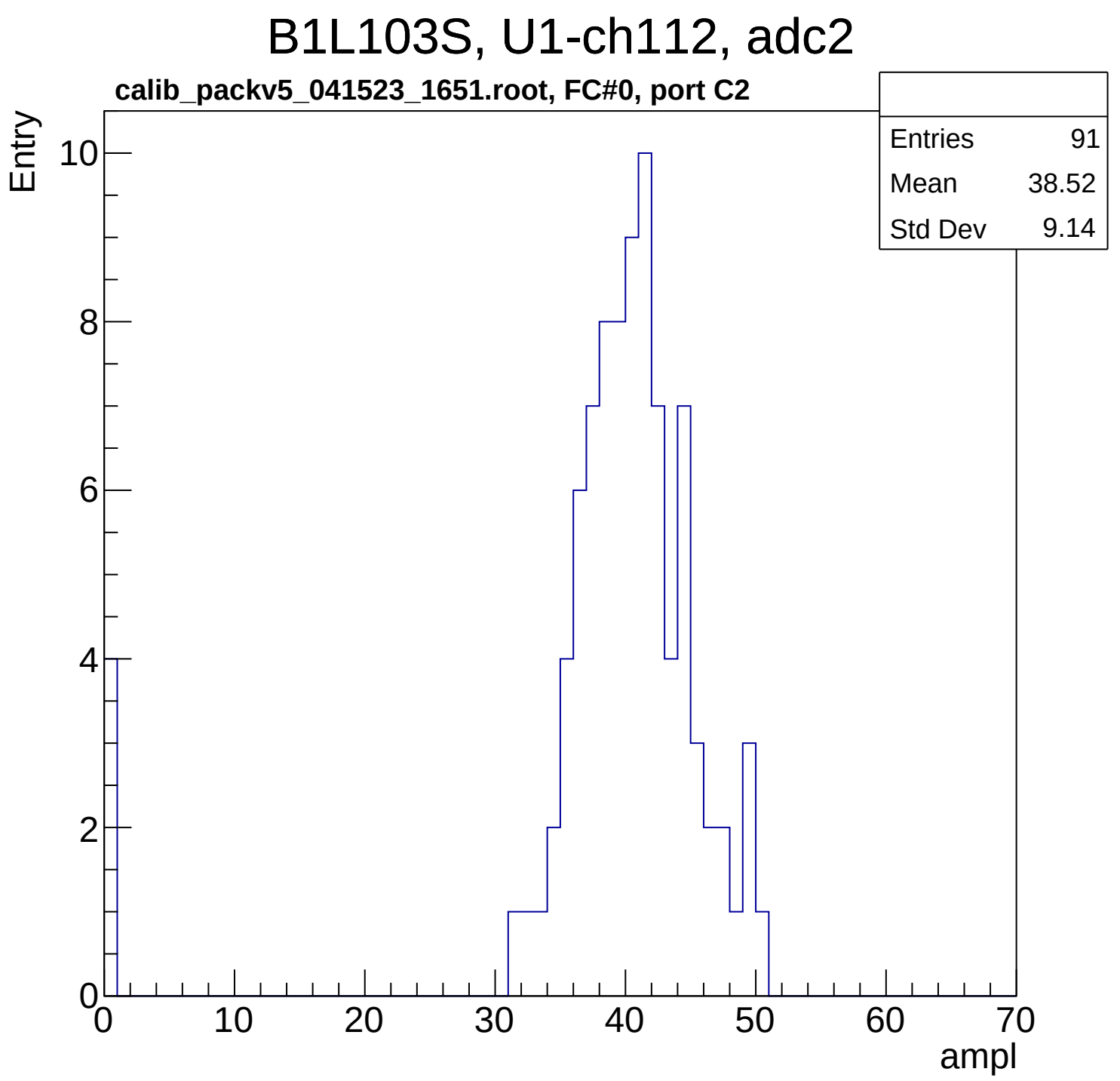
B1L103S, U1-ch112, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 91
Mean 38.52
Std Dev 9.14
Entry
ampl
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6
8
10
0
10
20
30
40
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60
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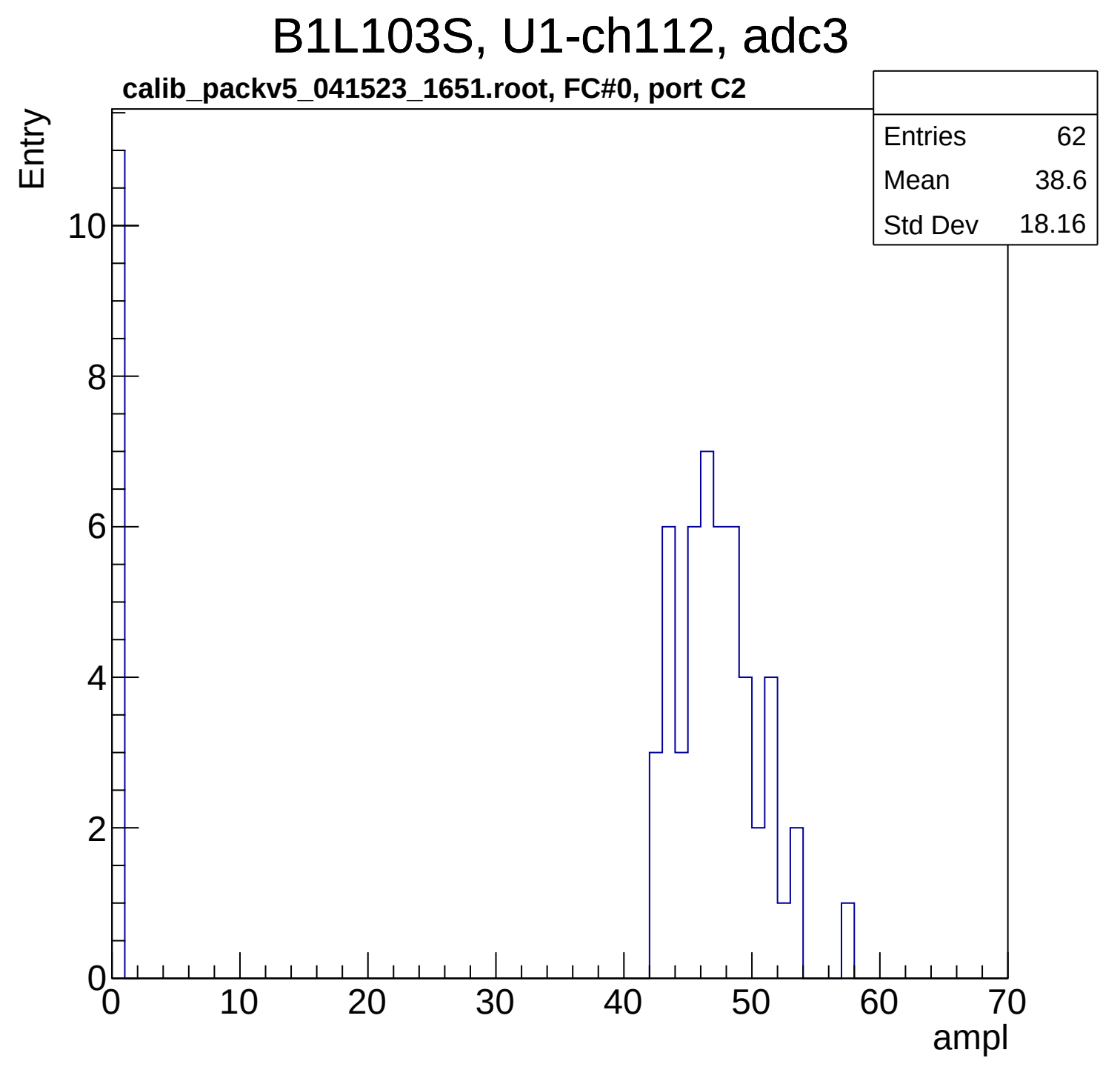
B1L103S, U1-ch112, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 38.6
Std Dev 18.16
Entry
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50
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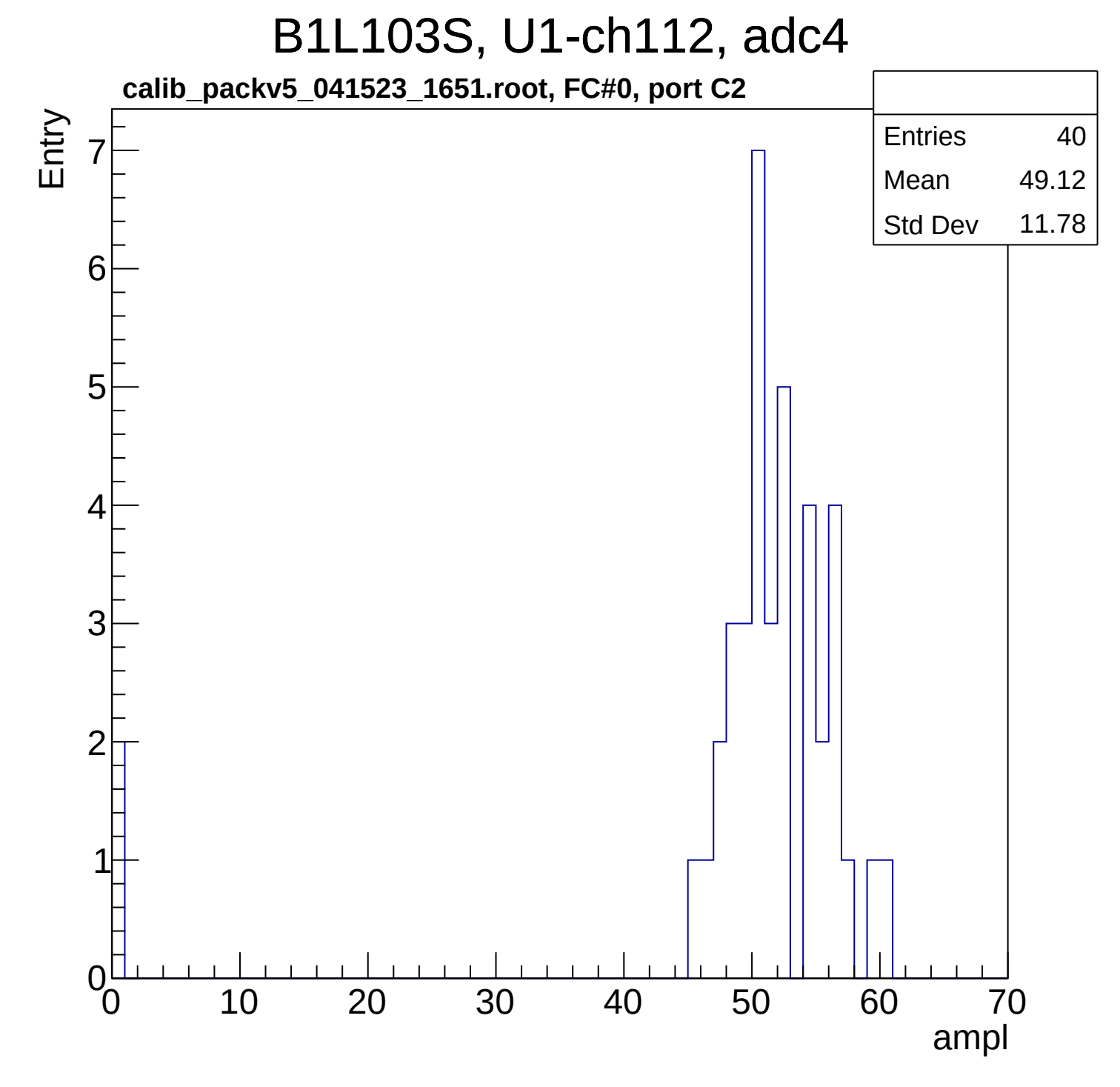
70
ampl


B1L103S, U1-ch112, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 40
Mean 49.12
Std Dev 11.78
Entry
ampl
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2
3
4
5
6
7
0
10
20
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40
50
60
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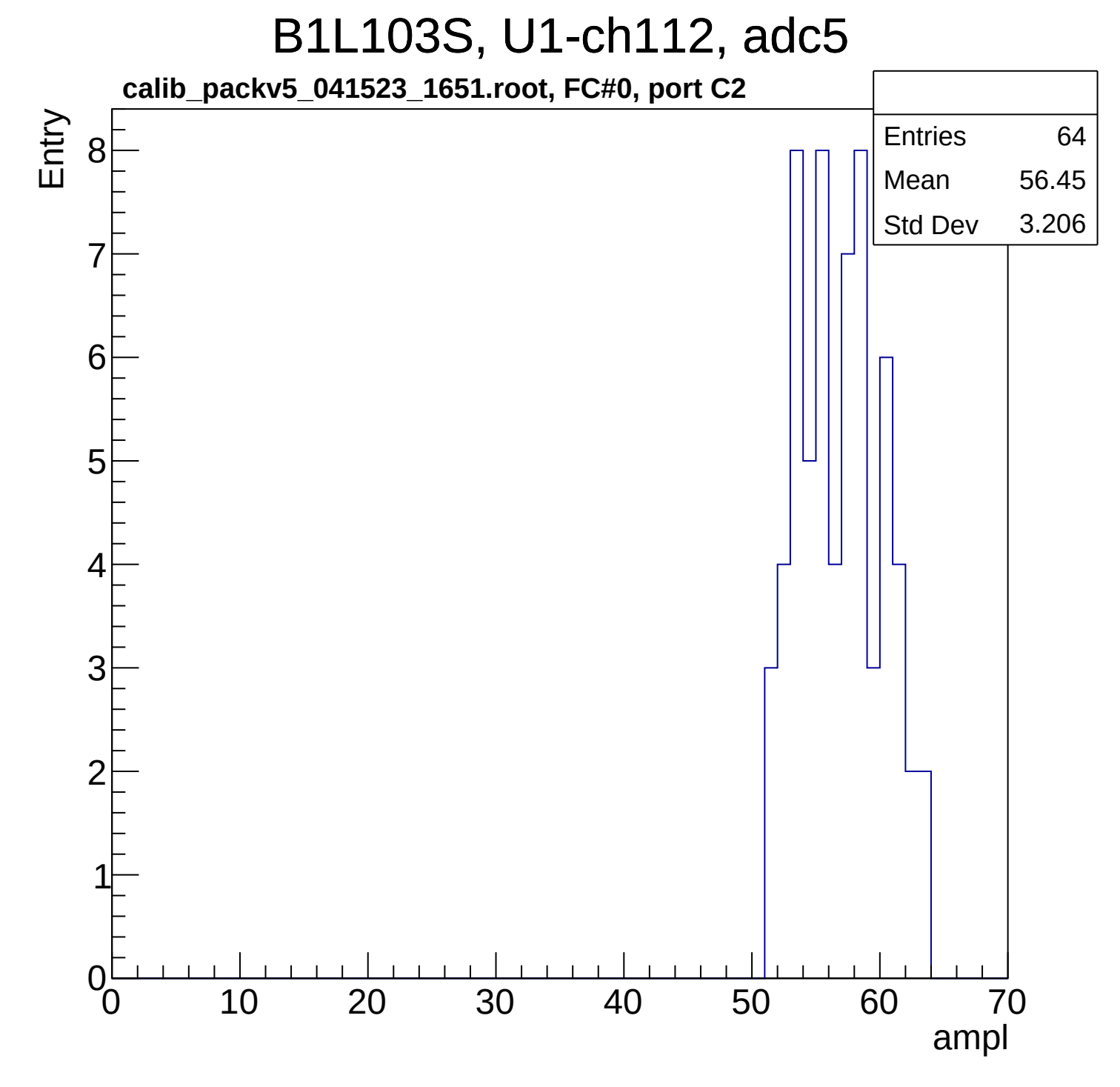
B1L103S, U1-ch112, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 56.45
Std Dev 3.206
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
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40
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60
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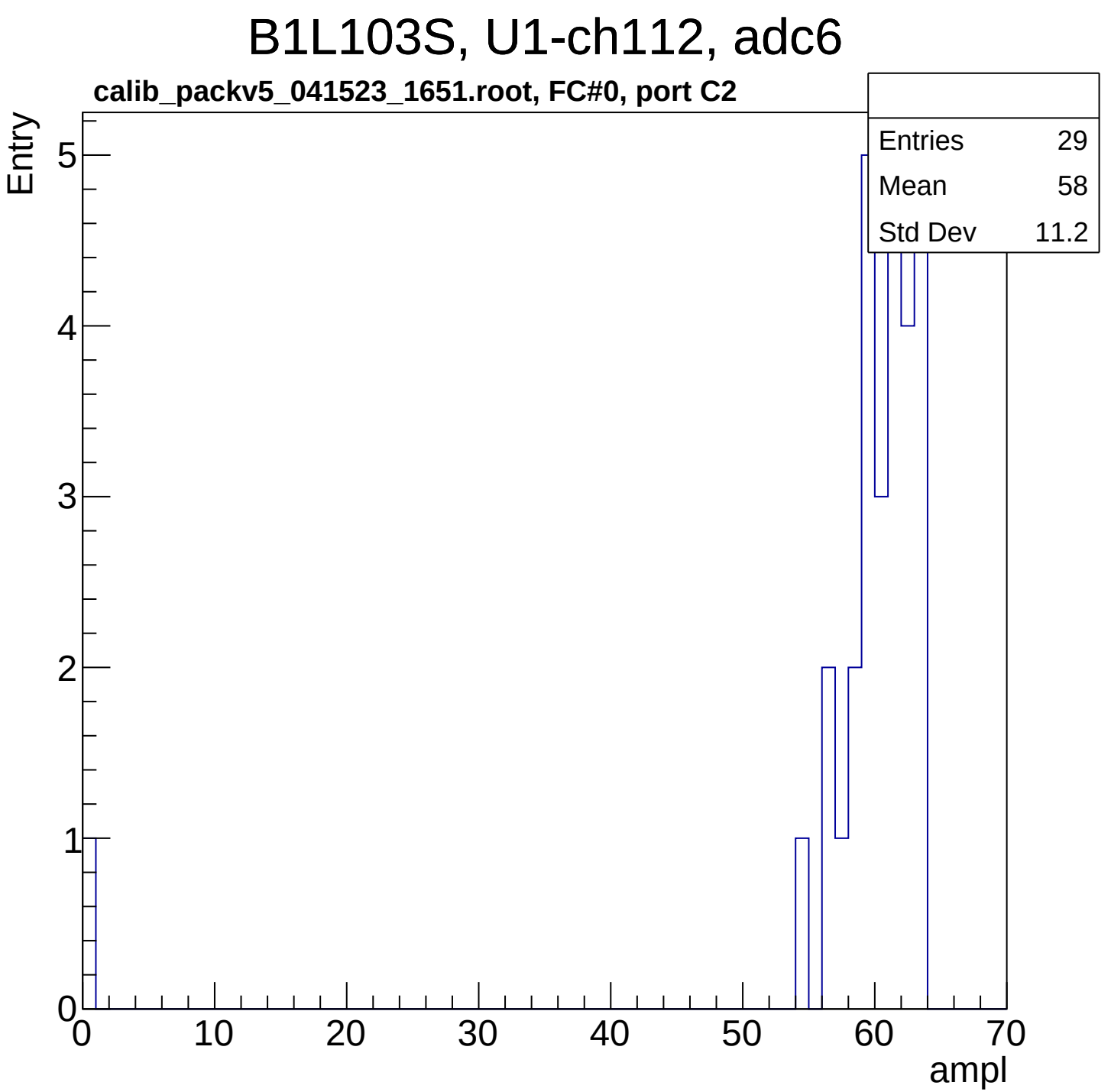
B1L103S, U1-ch112, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 29
Mean 58
Std Dev 11.2
Entry
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1
2
3
4
5
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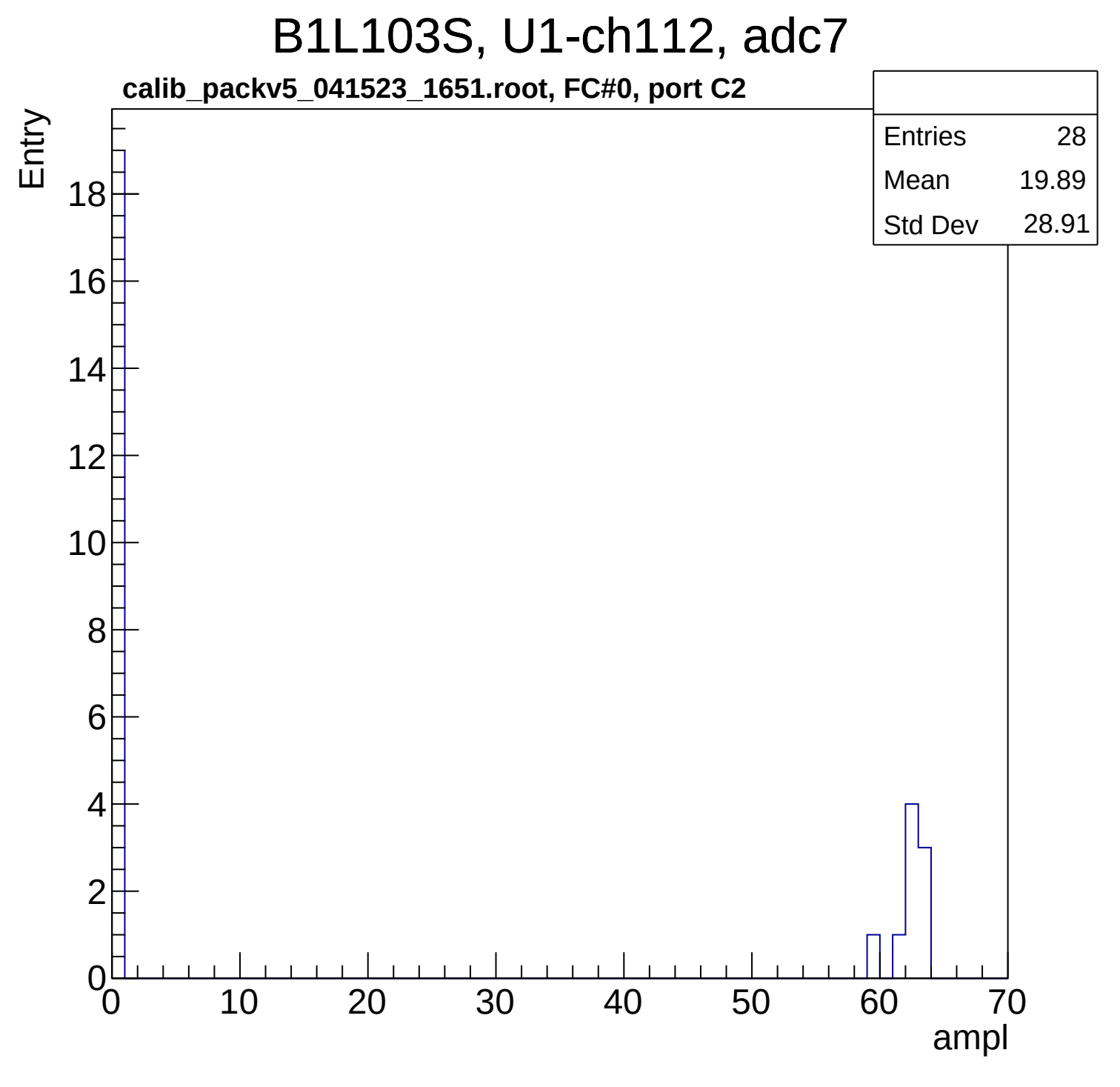
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch112, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 28
Mean 19.89
Std Dev 28.91
Entry
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6
8
10
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14
16
18
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10
20
30
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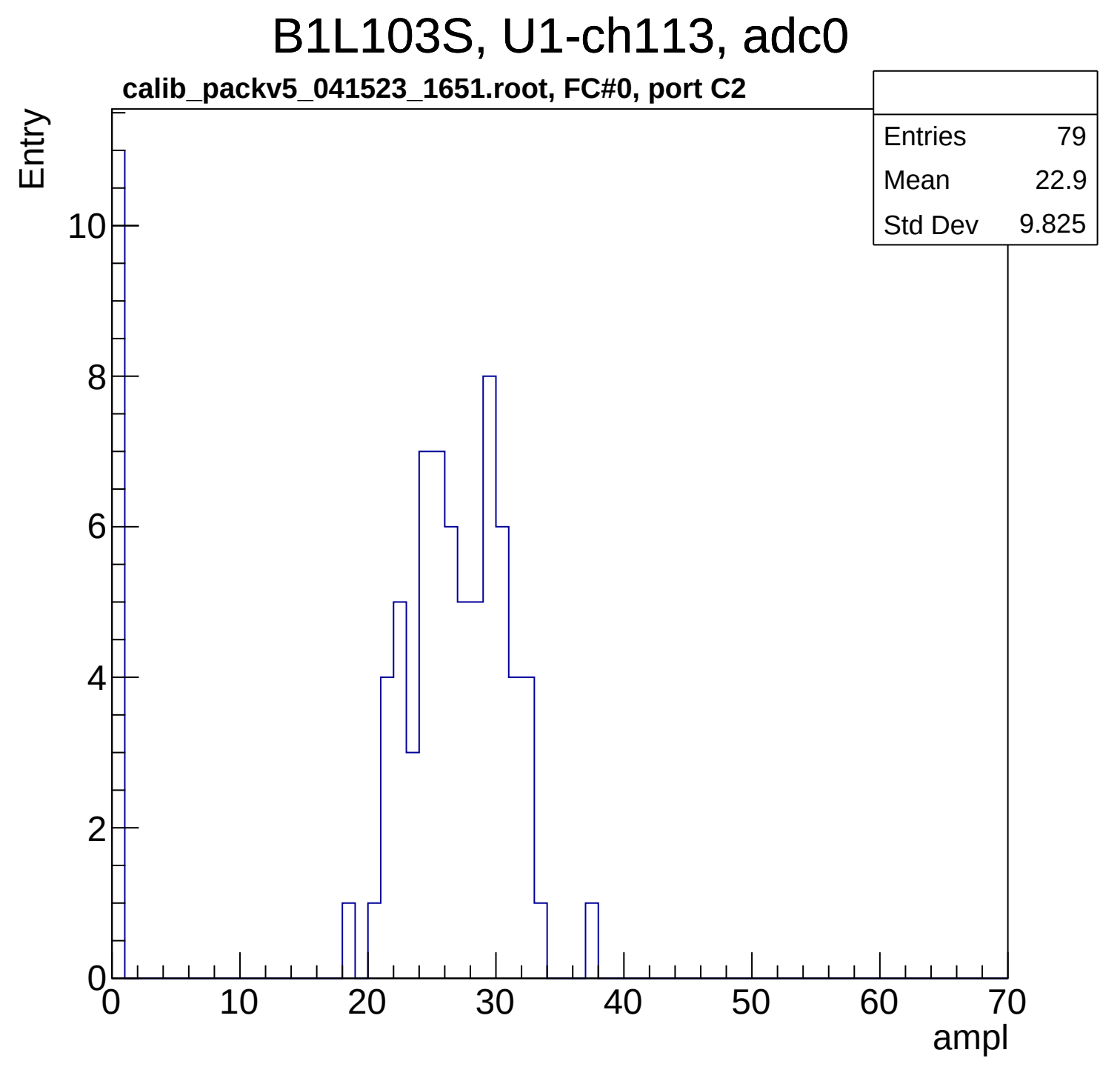
50
60
70
ampl


B1L103S, U1-ch113, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 22.9
Std Dev 9.825
Entry
ampl
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0
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40
50
60
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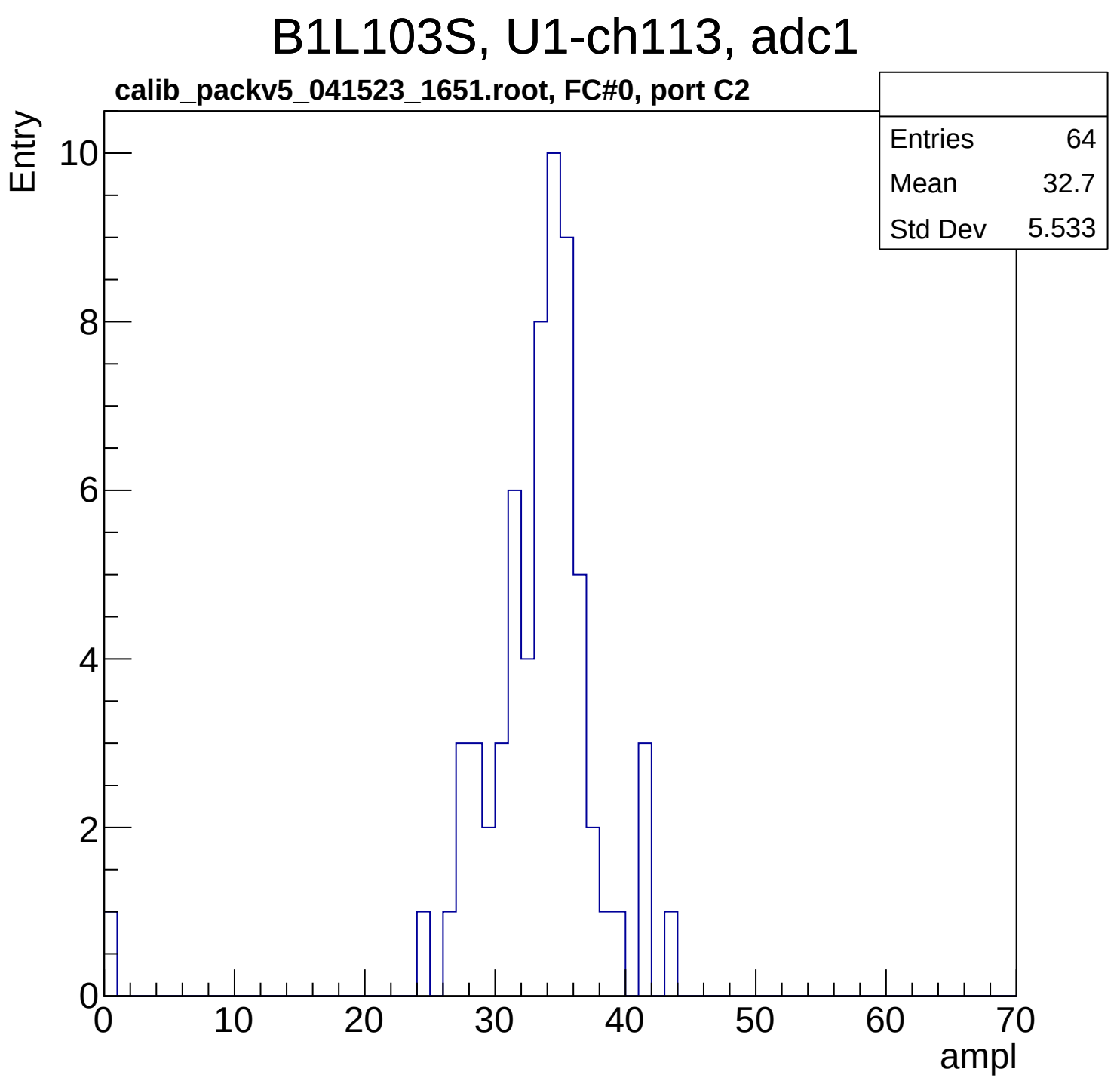
B1L103S, U1-ch113, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 32.7
Std Dev 5.533
Entry
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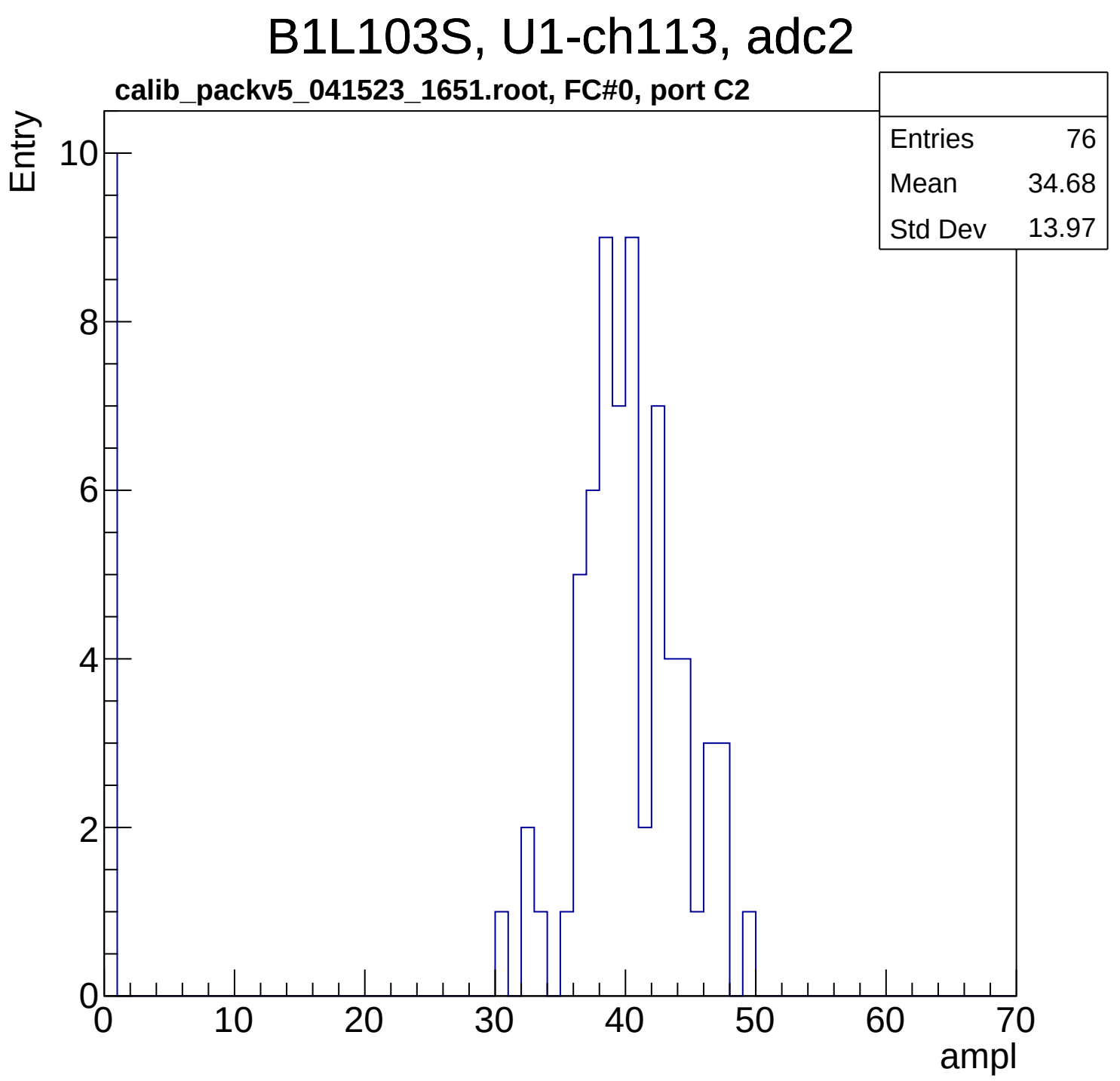
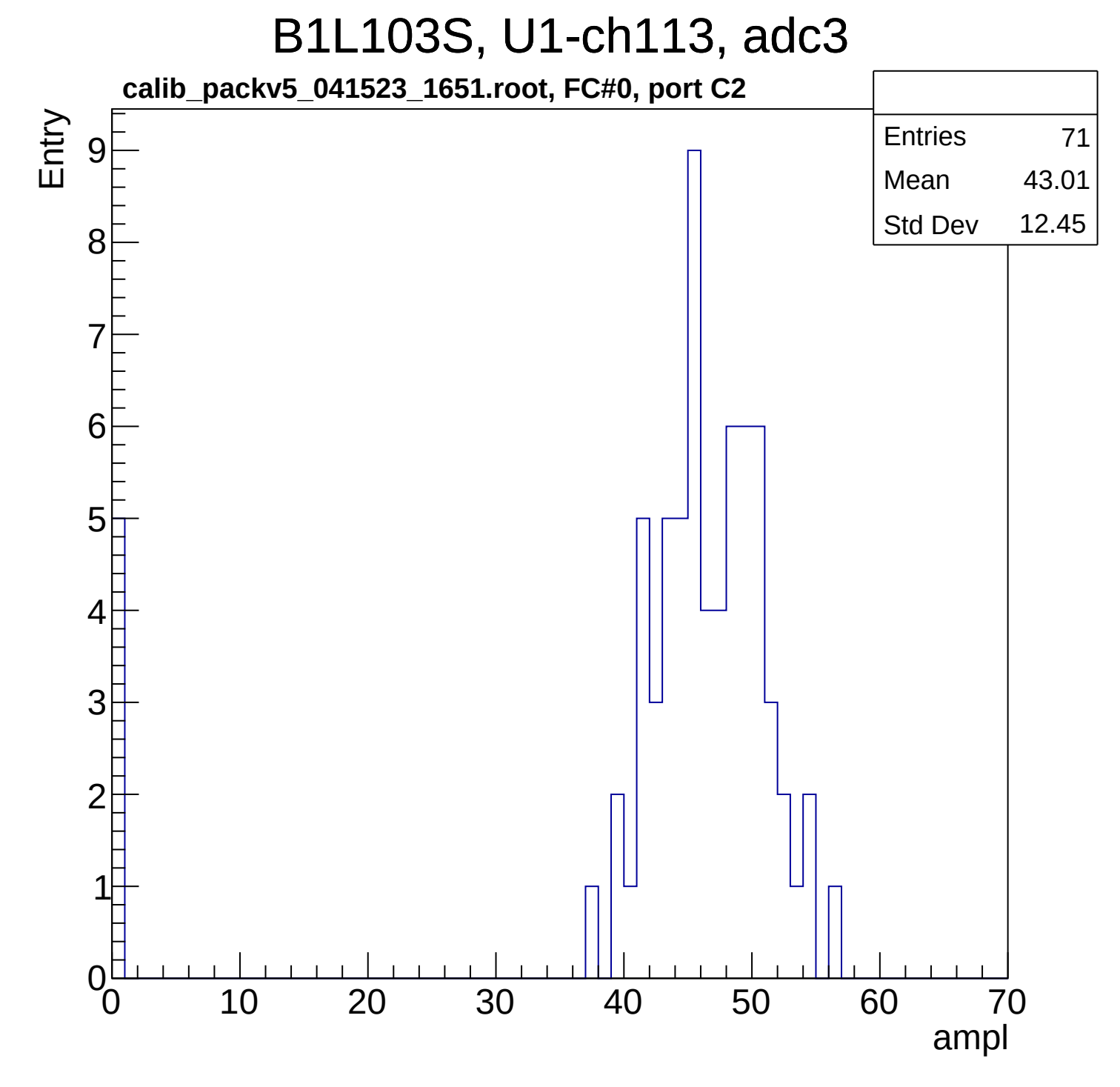
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch113, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 34.68
Std Dev 13.97
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch113, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 43.01
Std Dev 12.45
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
50
60
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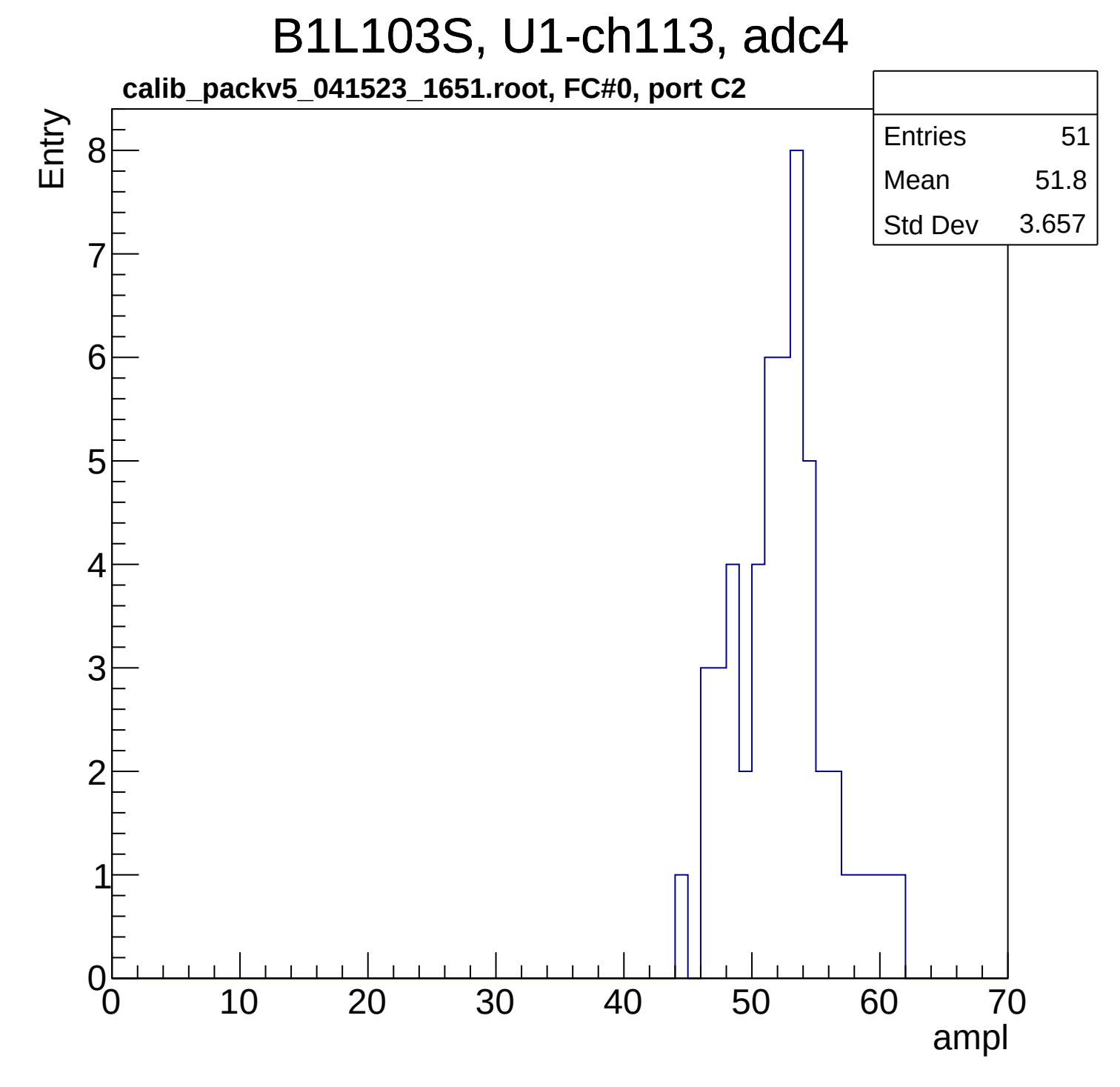
B1L103S, U1-ch113, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 51.8
Std Dev 3.657
Entry
ampl
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2
3
4
5
6
7
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0
10
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40
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60
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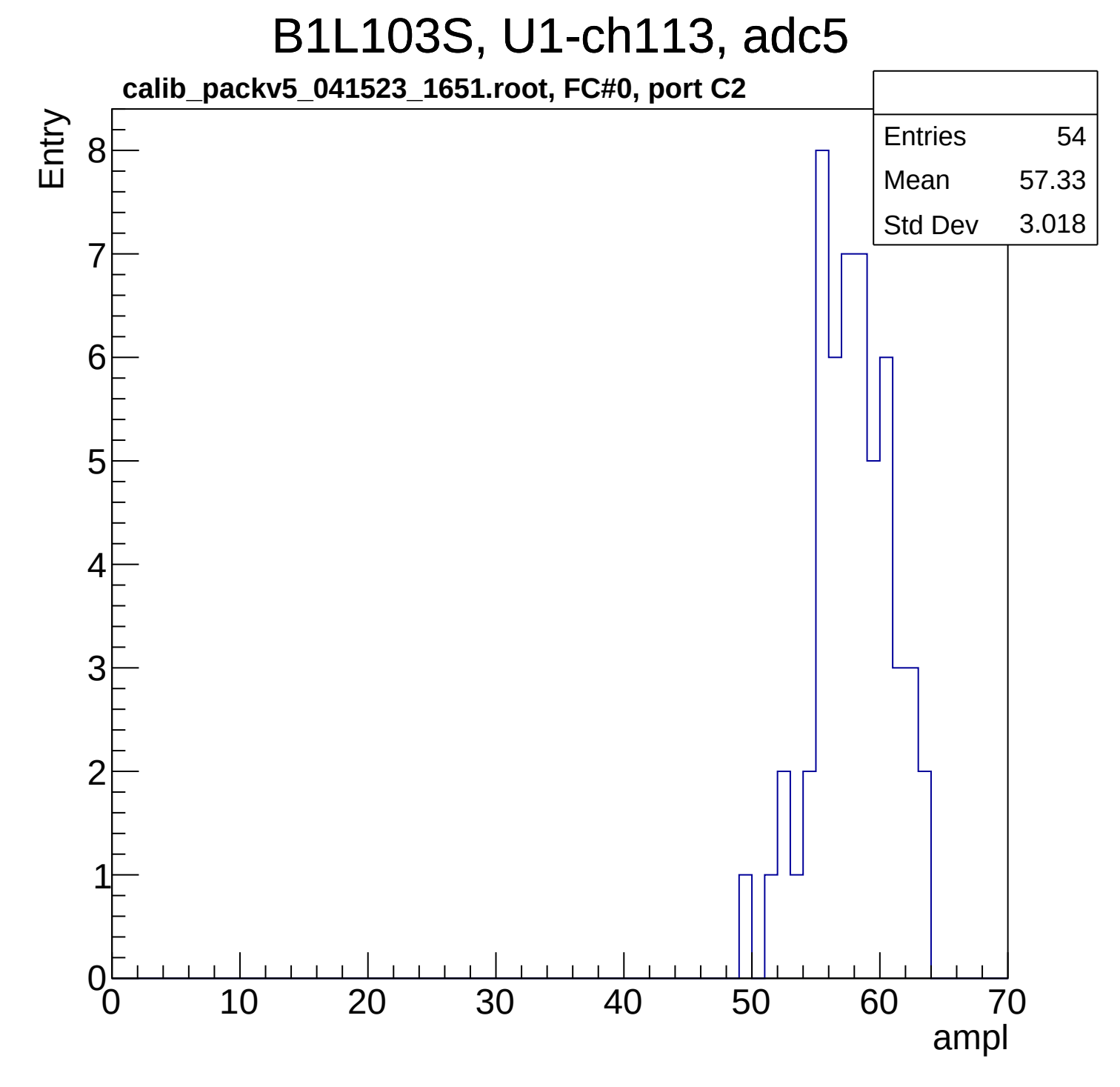
B1L103S, U1-ch113, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 57.33
Std Dev 3.018
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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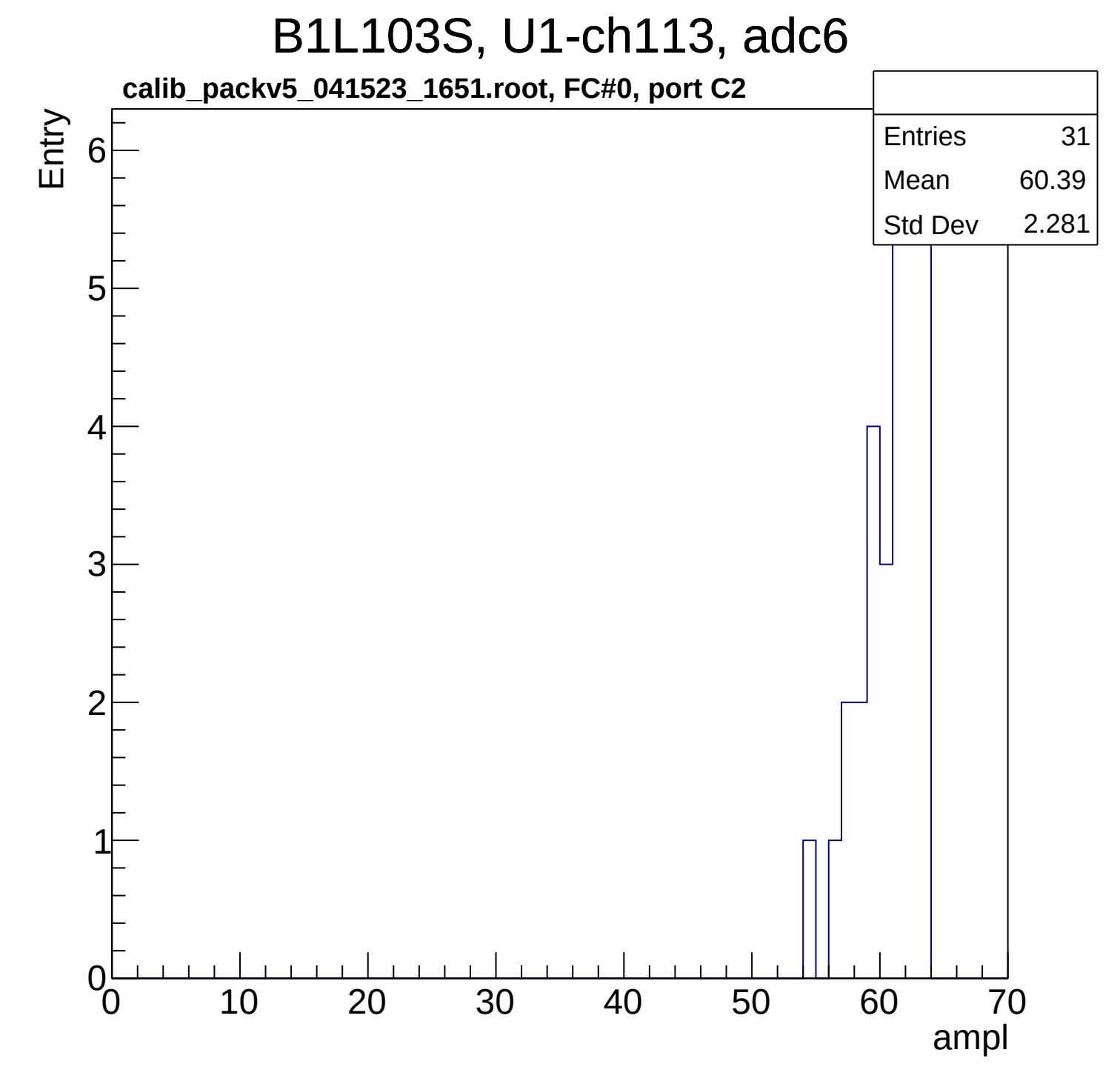
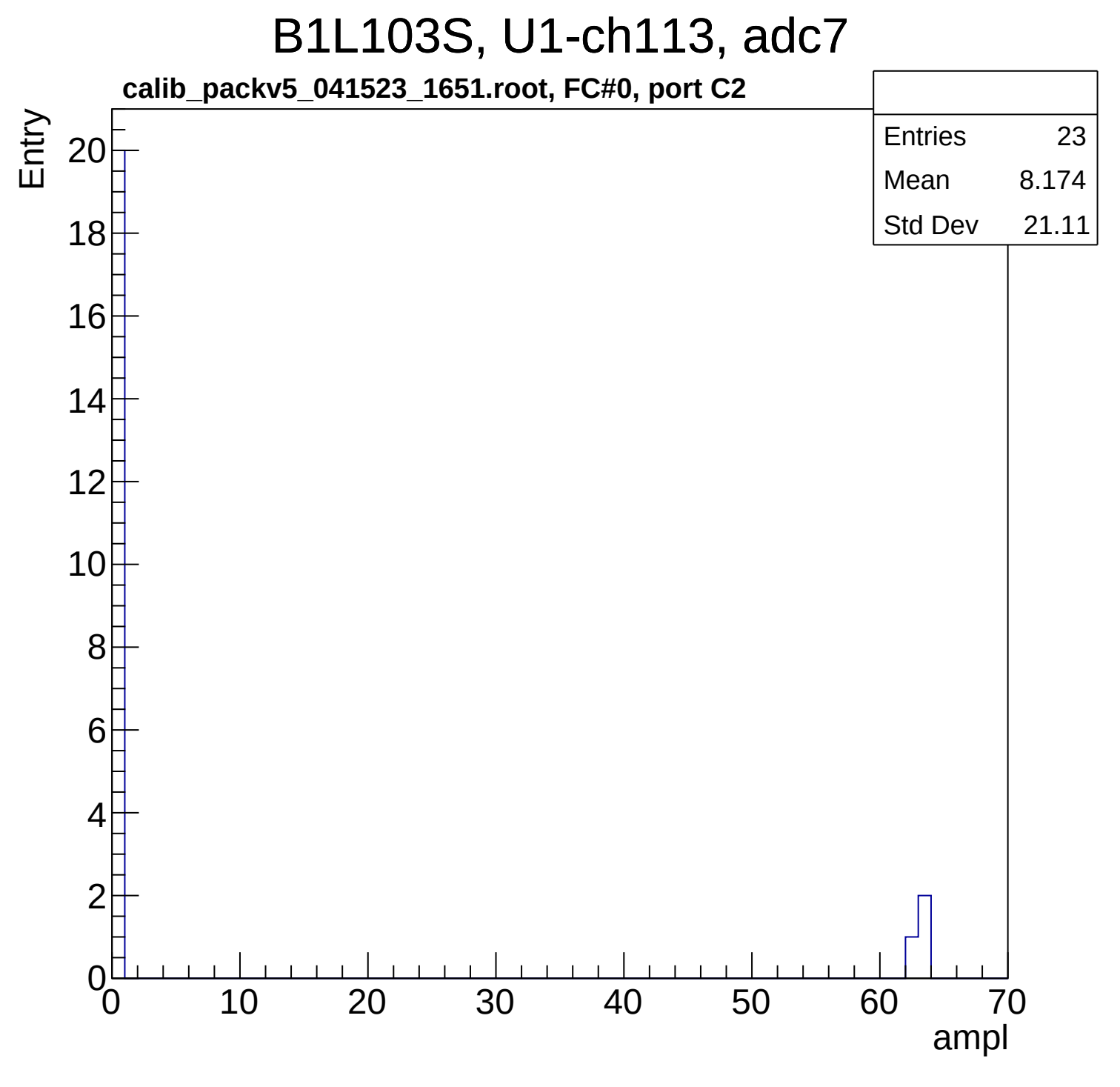

B1L103S, U1-ch113, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 31
Mean 60.39
Std Dev 2.281
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U1-ch113, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 23
Mean 8.174
Std Dev 21.11
Entry
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8
10
12
14
16
18
20
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10
20
30
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50
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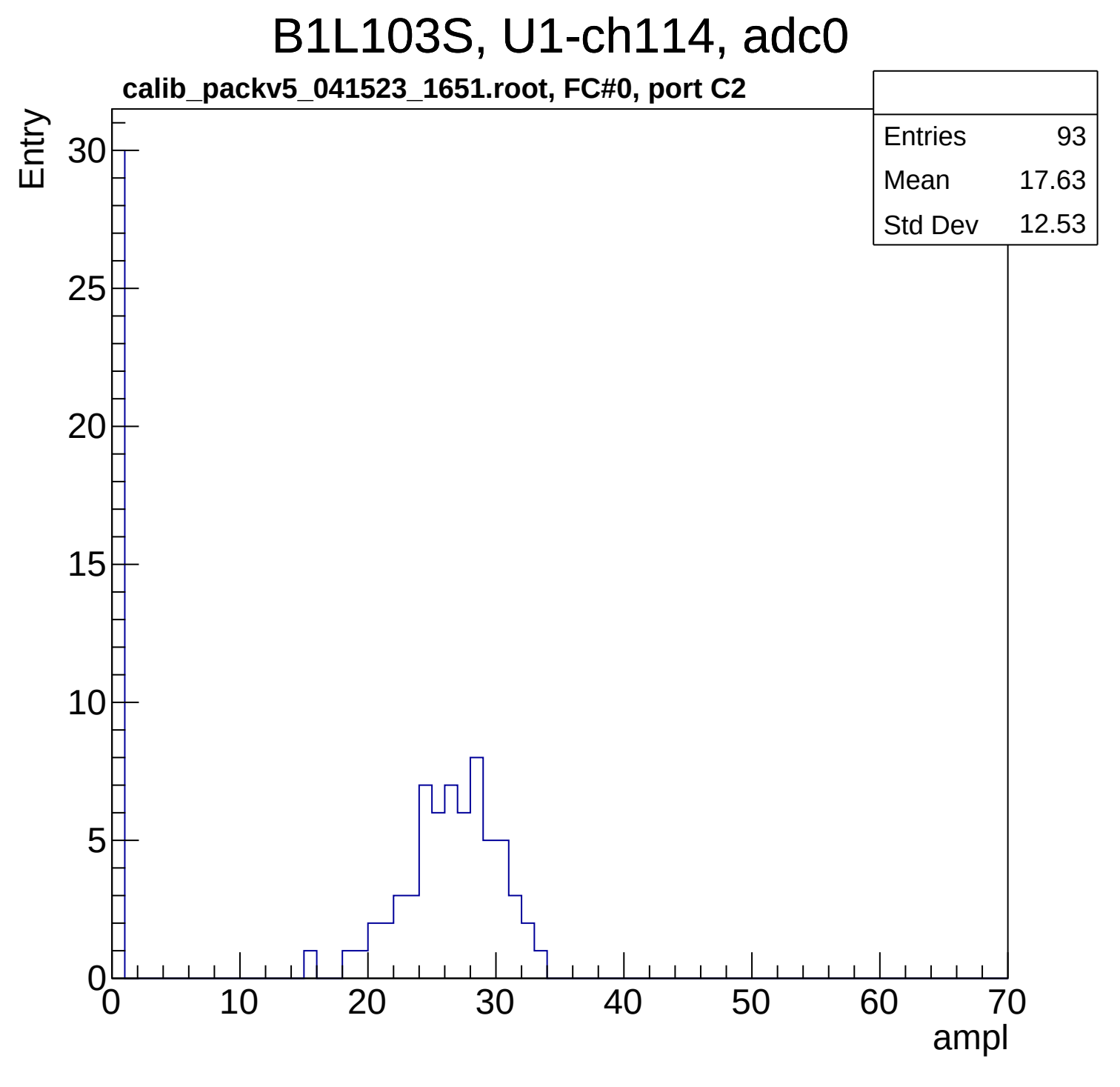
70
ampl


B1L103S, U1-ch114, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 93
Mean 17.63
Std Dev 12.53
Entry
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5
10
15
20
25
30
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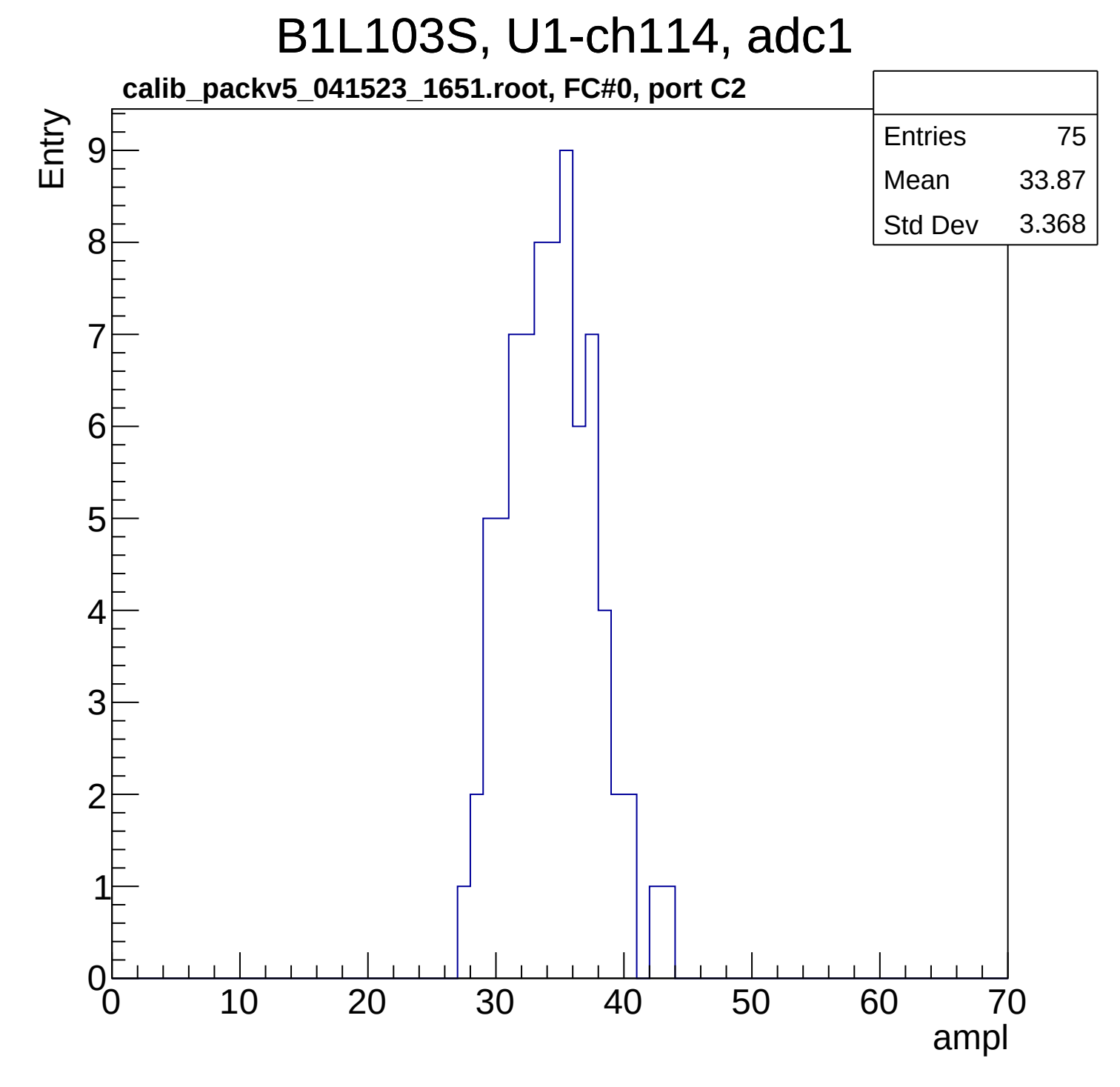
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch114, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 33.87
Std Dev 3.368
Entry
ampl
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3
4
5
6
7
8
9
0
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60
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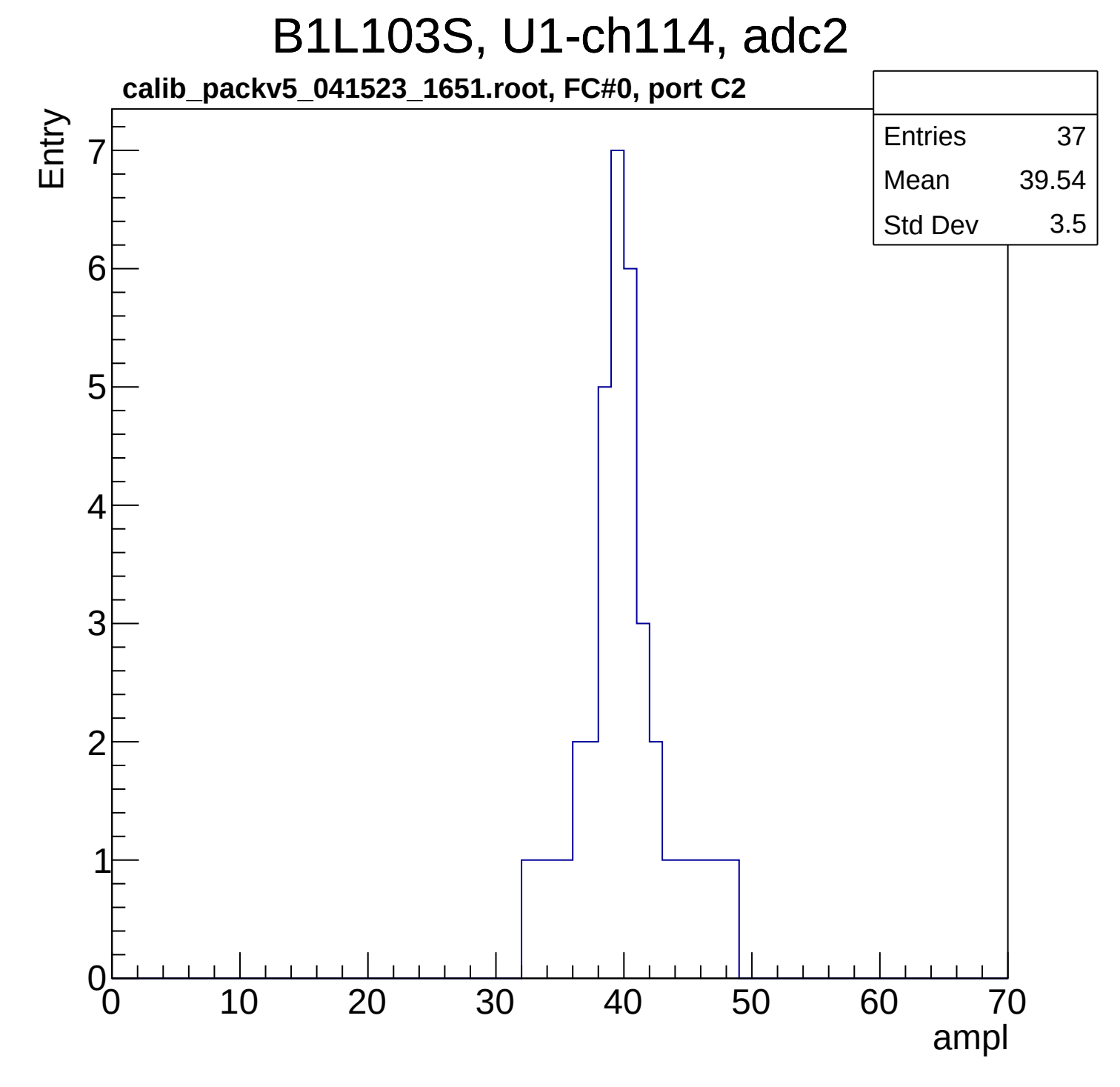
B1L103S, U1-ch114, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 37
Mean 39.54
Std Dev 3.5
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
30
40
50
60
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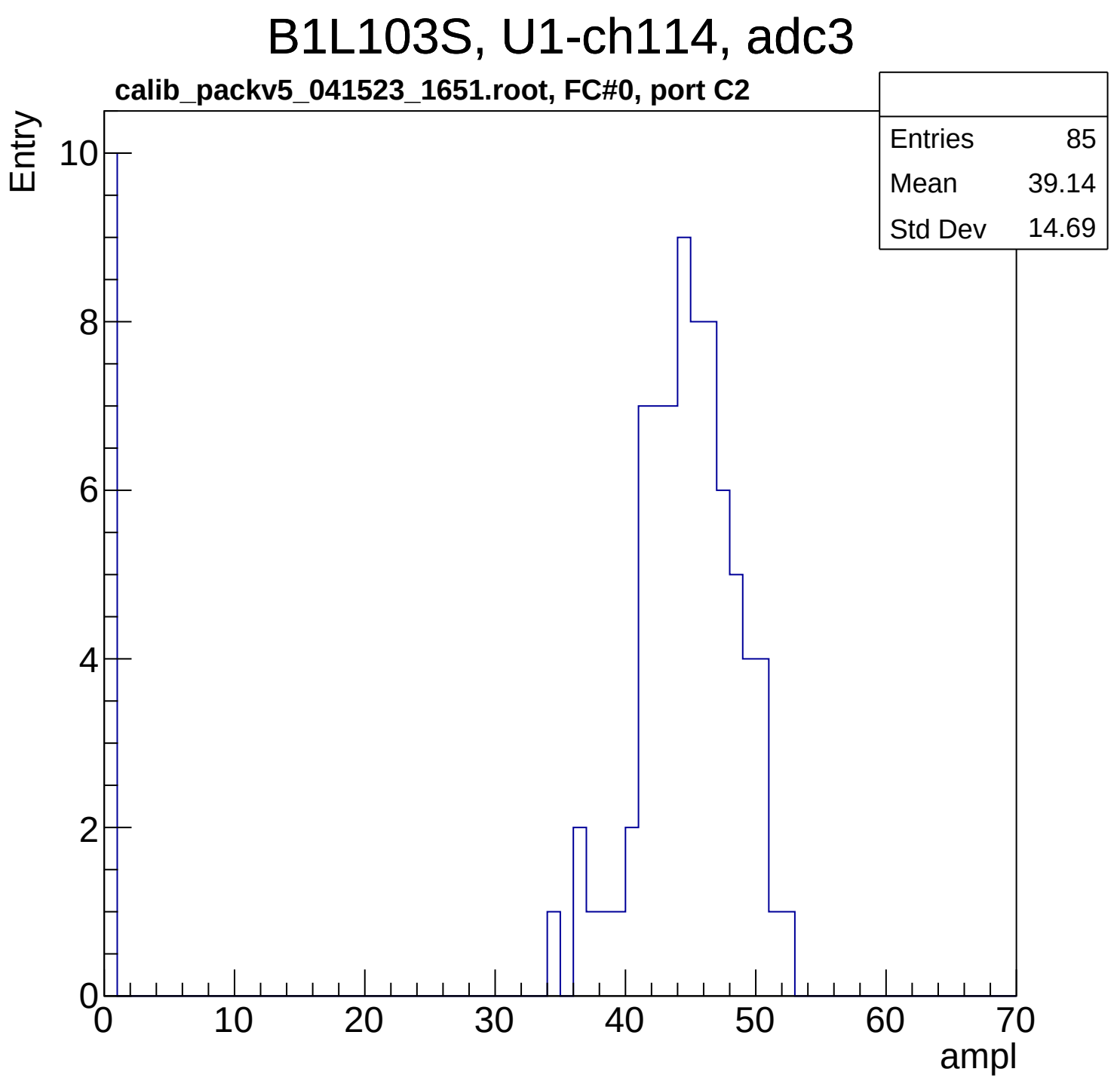
B1L103S, U1-ch114, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 39.14
Std Dev 14.69
Entry
ampl
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0
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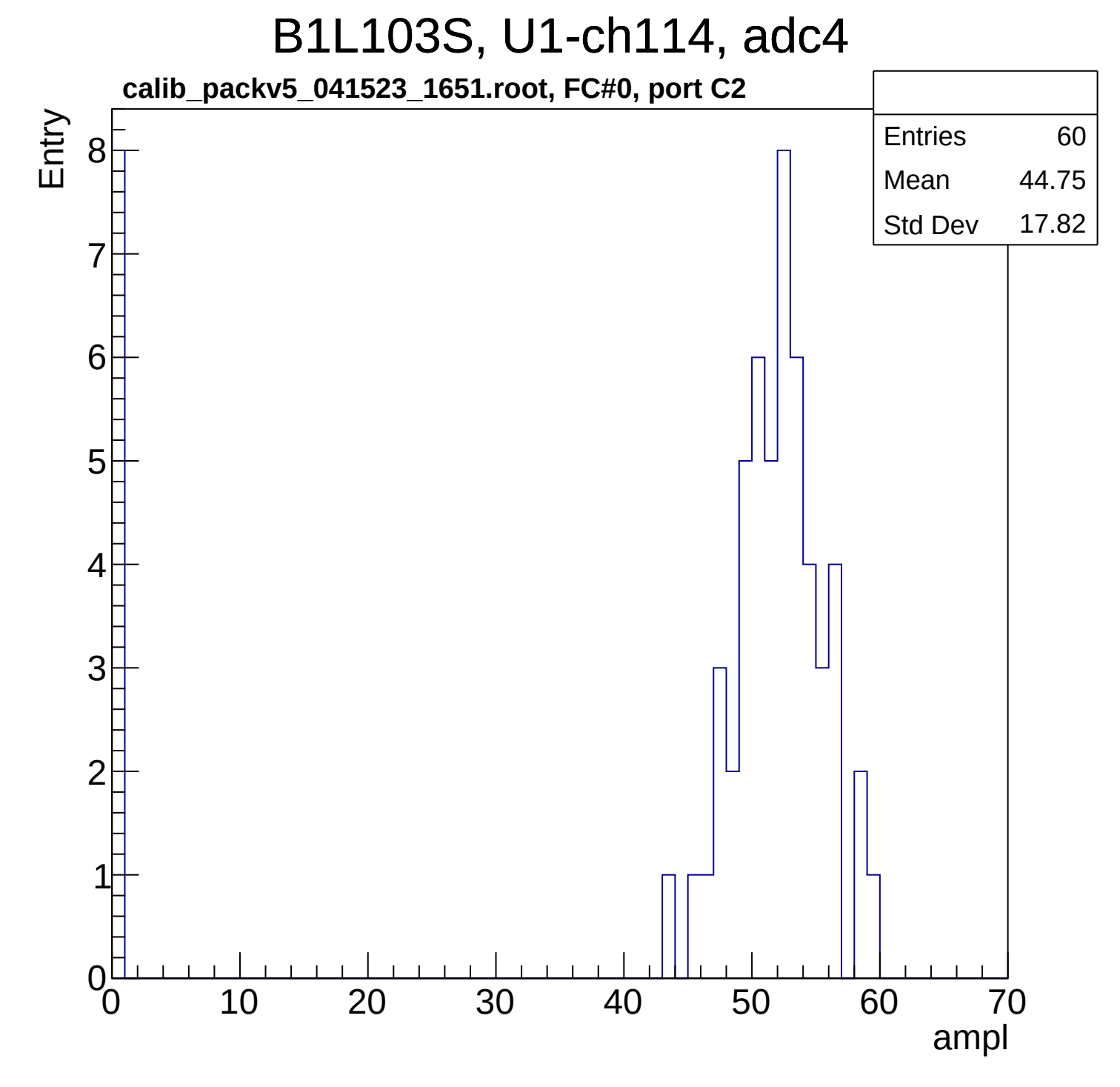
B1L103S, U1-ch114, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 44.75
Std Dev 17.82
Entry
ampl
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2
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5
6
7
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0
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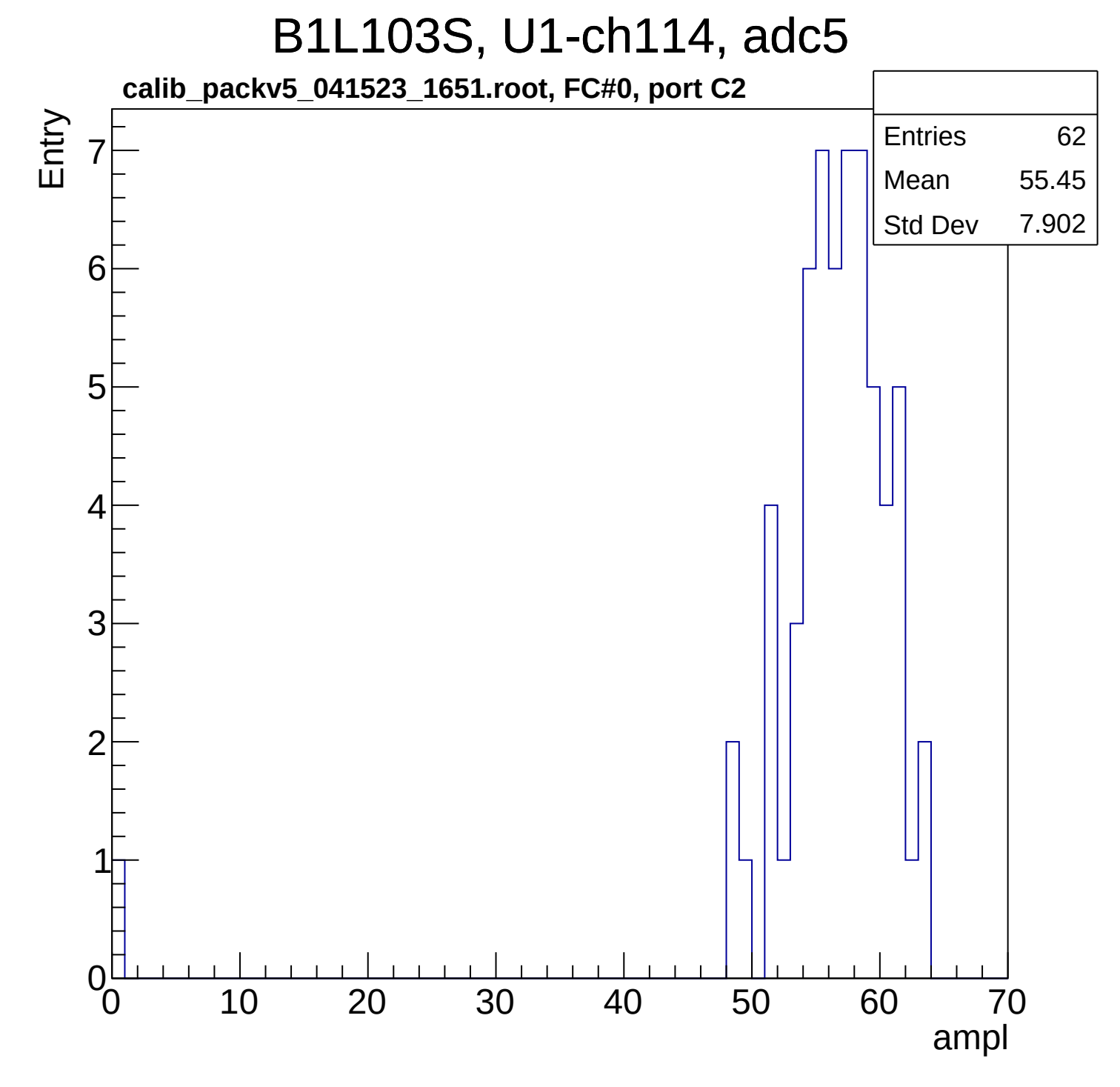
B1L103S, U1-ch114, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 55.45
Std Dev 7.902
Entry
ampl
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3
4
5
6
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0
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40
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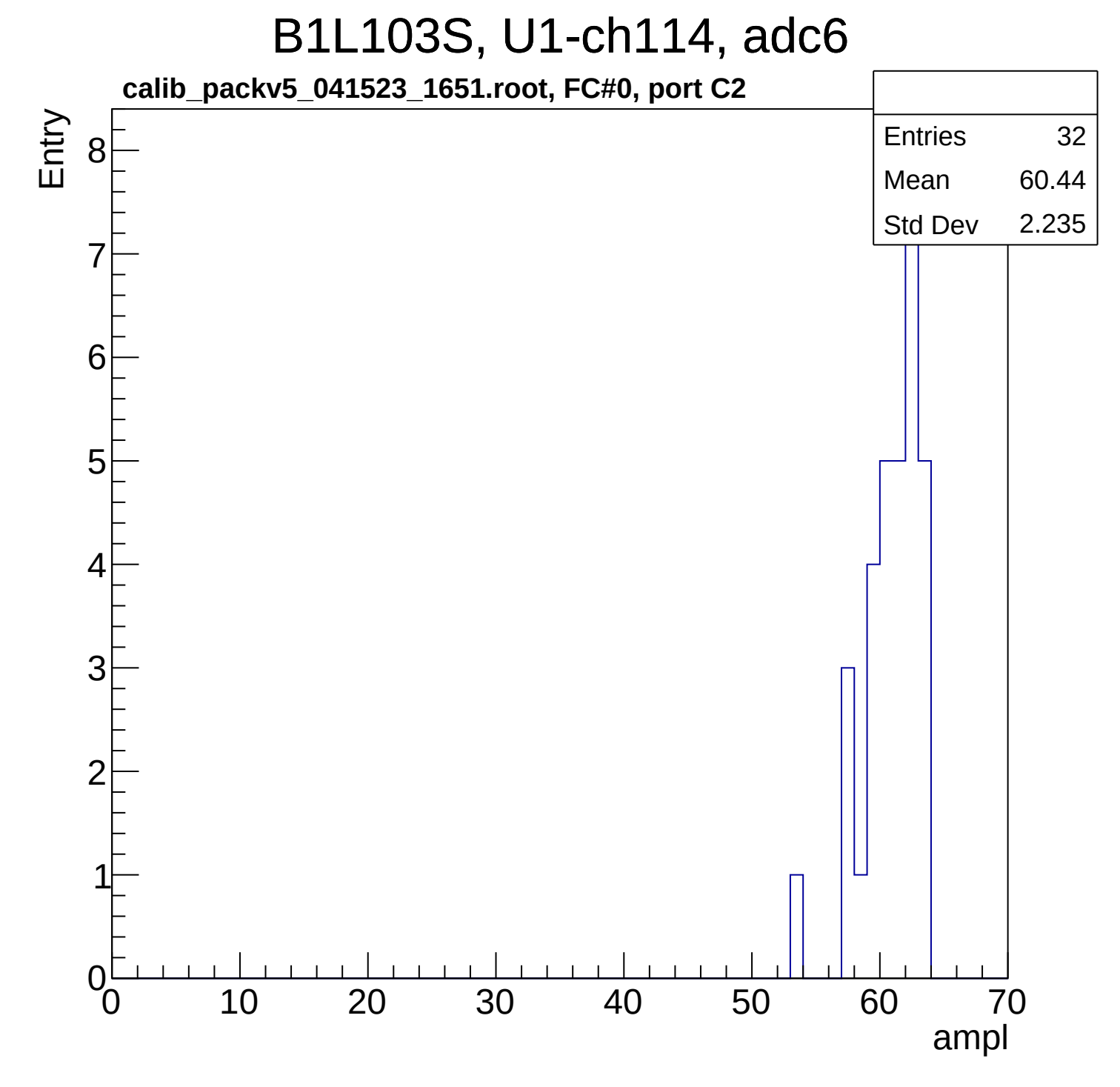
B1L103S, U1-ch114, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 32
Mean 60.44
Std Dev 2.235
Entry
ampl
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6
7
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0
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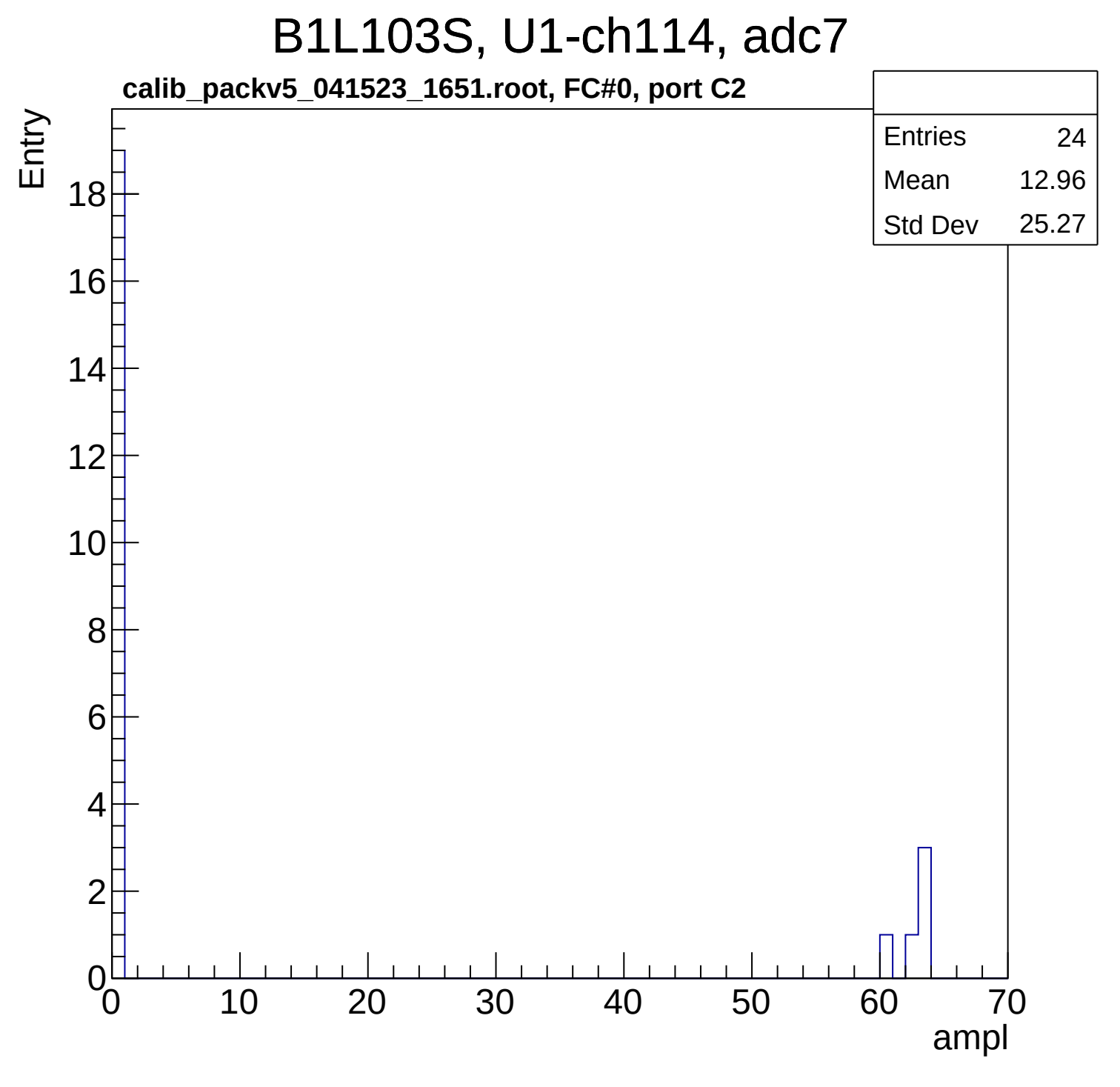
B1L103S, U1-ch114, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 24
Mean 12.96
Std Dev 25.27
Entry
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6
8
10
12
14
16
18
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10
20
30
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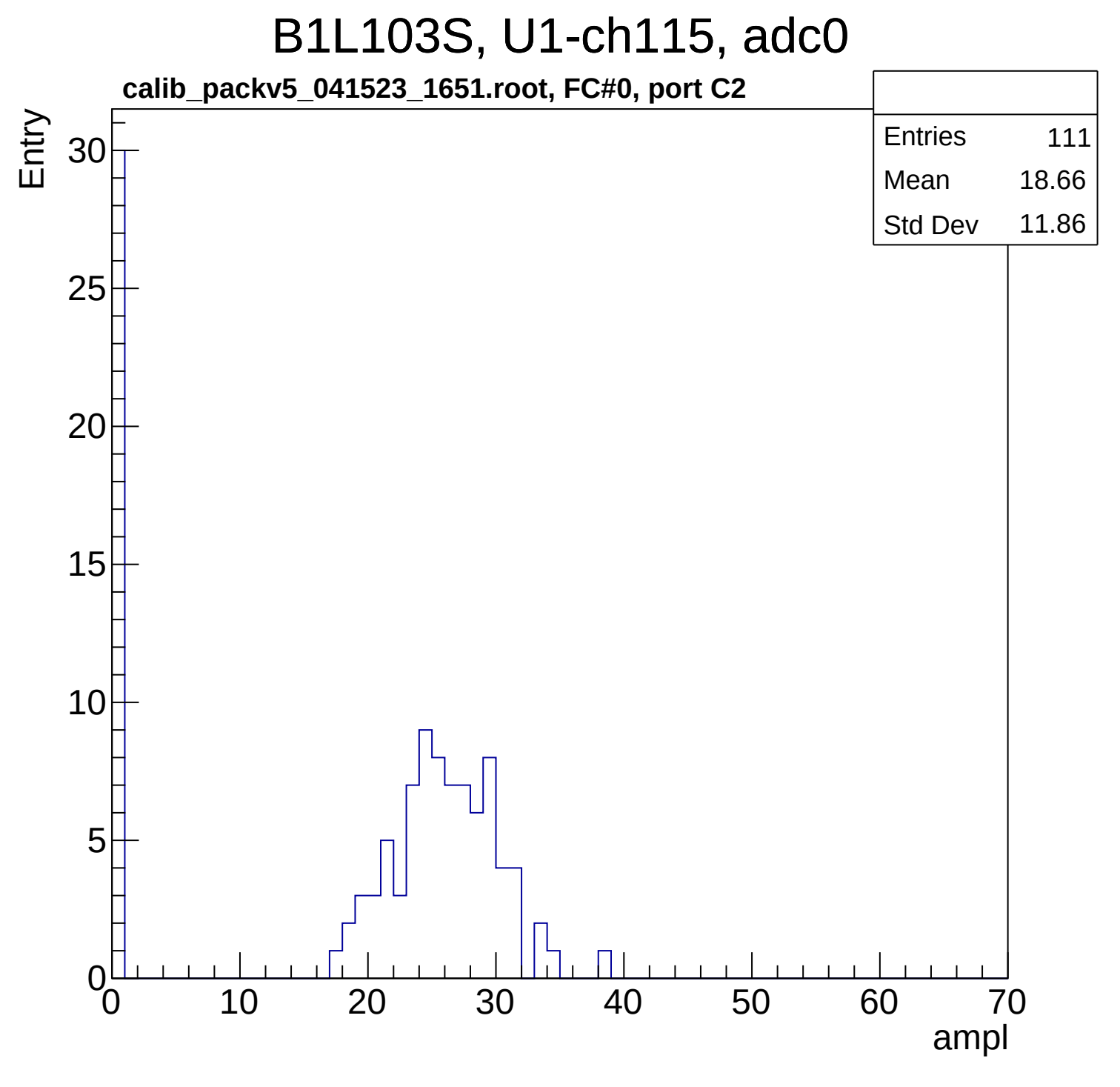
50
60
70
ampl


B1L103S, U1-ch115, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 111
Mean 18.66
Std Dev 11.86
Entry
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20
25
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10
20
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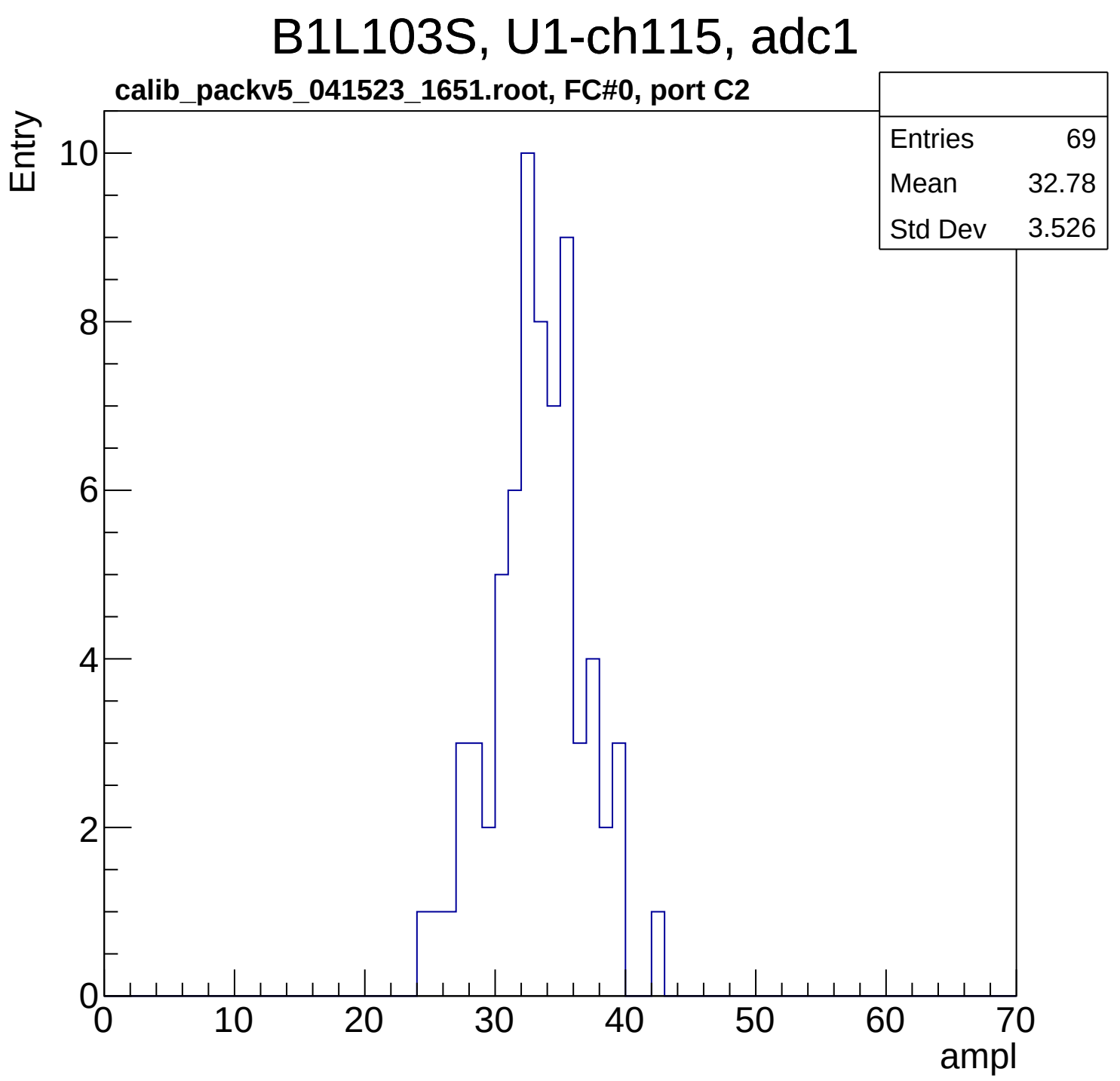
50
60
70
ampl


B1L103S, U1-ch115, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 32.78
Std Dev 3.526
Entry
ampl
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0
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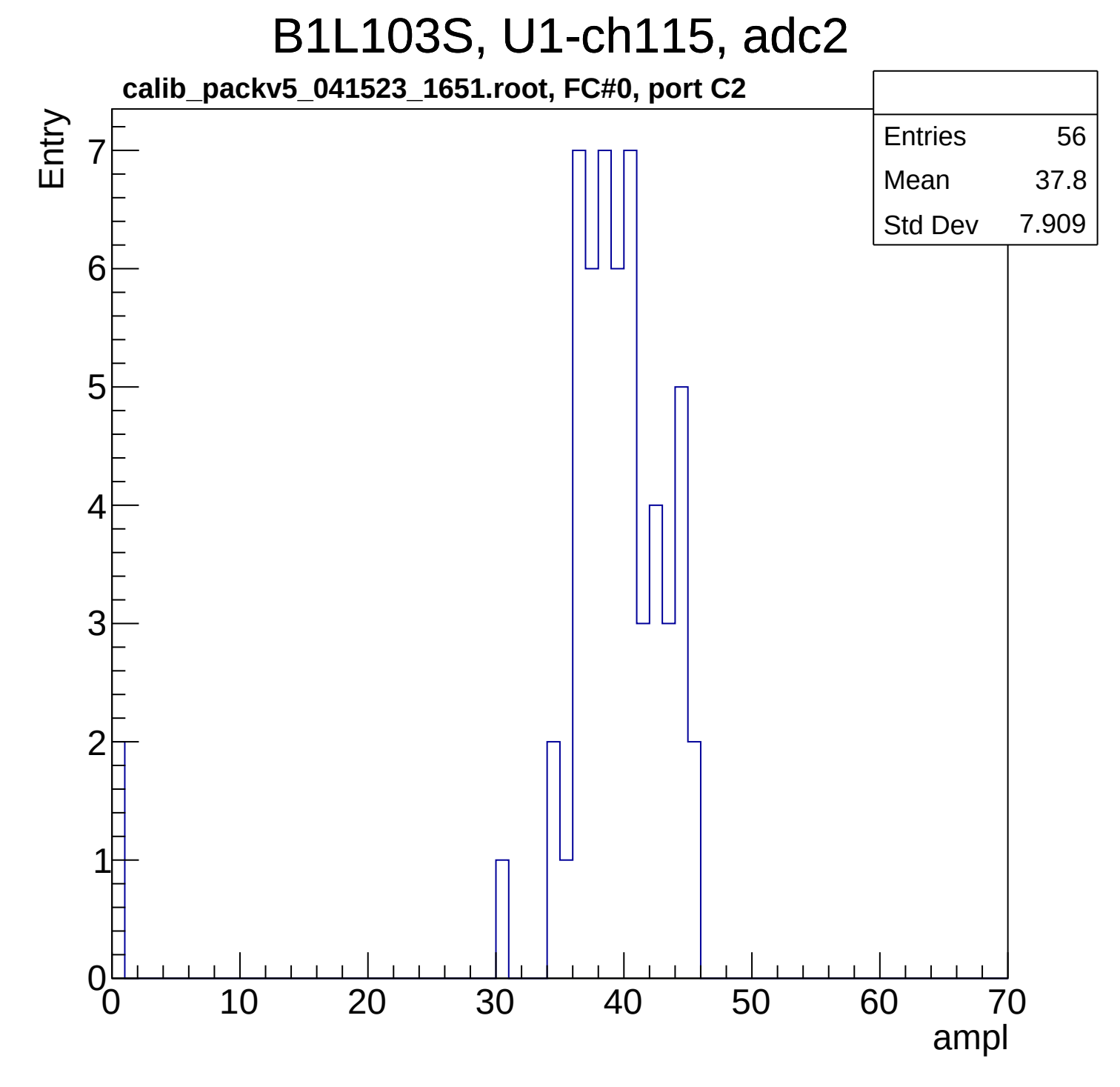
B1L103S, U1-ch115, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 37.8
Std Dev 7.909
Entry
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4
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0
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60
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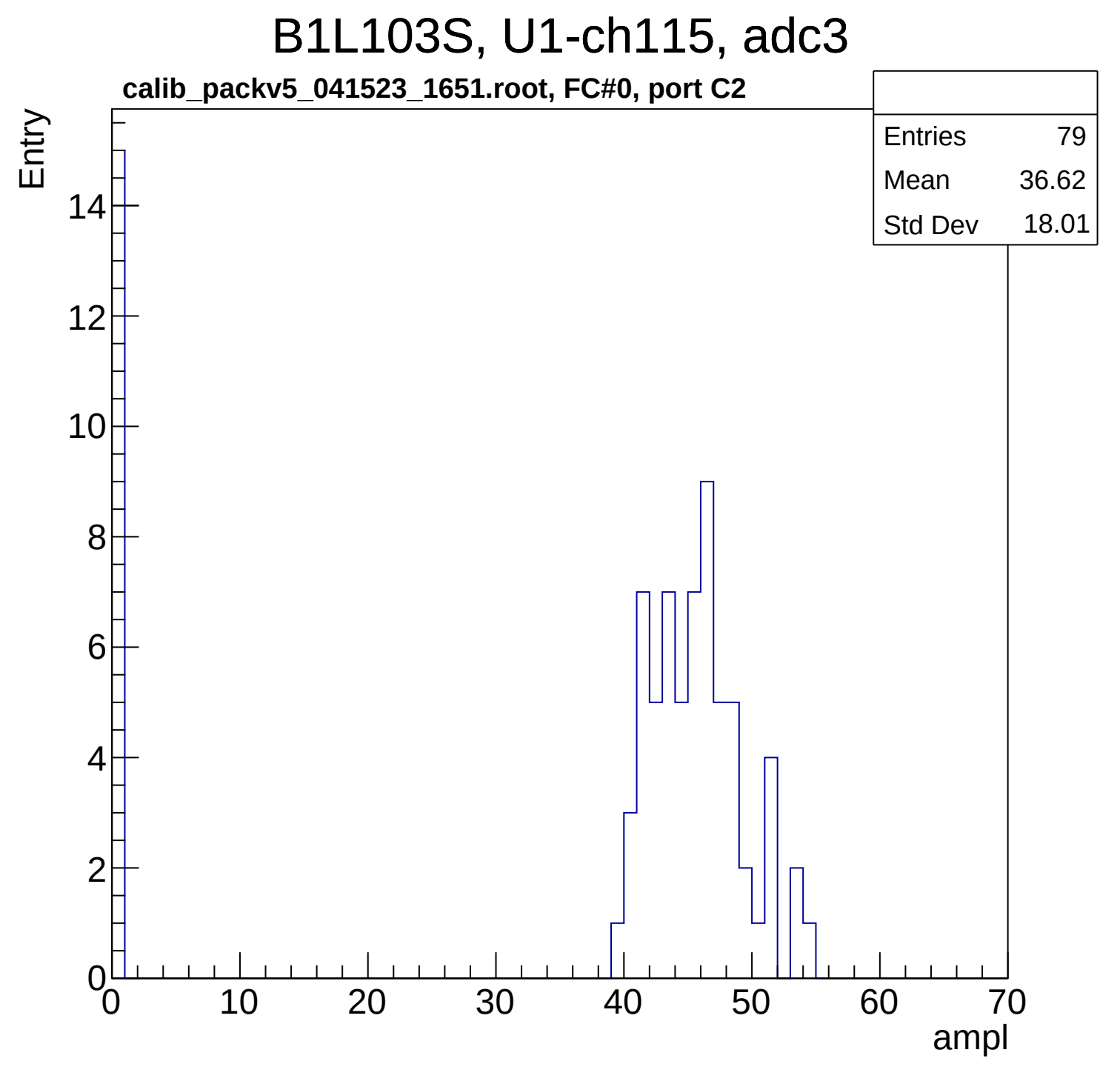
B1L103S, U1-ch115, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 36.62
Std Dev 18.01
Entry
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6
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10
12
14
0
10
20
30
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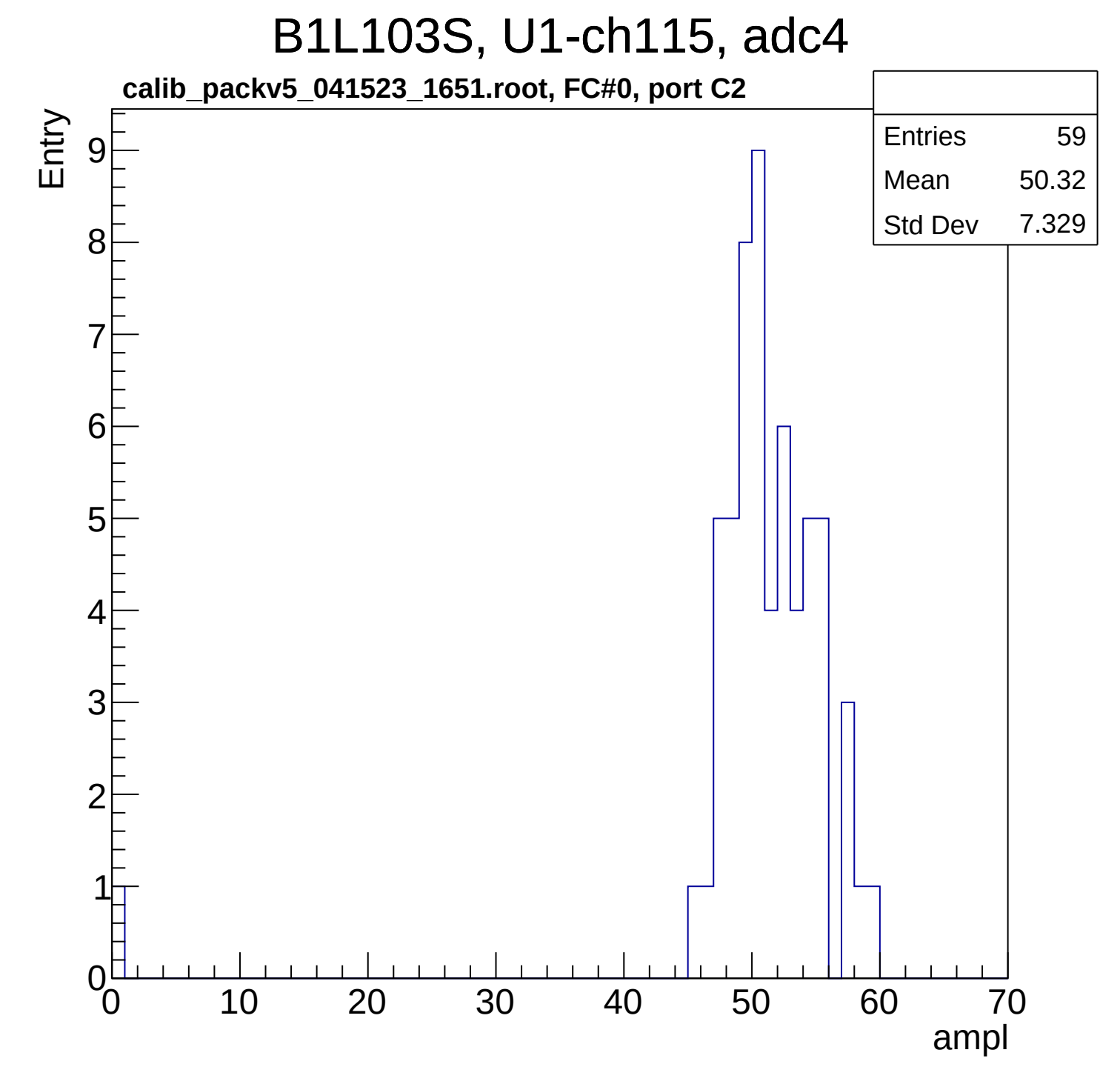
50
60
70
ampl


B1L103S, U1-ch115, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 50.32
Std Dev 7.329
Entry
ampl
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4
5
6
7
8
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0
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60
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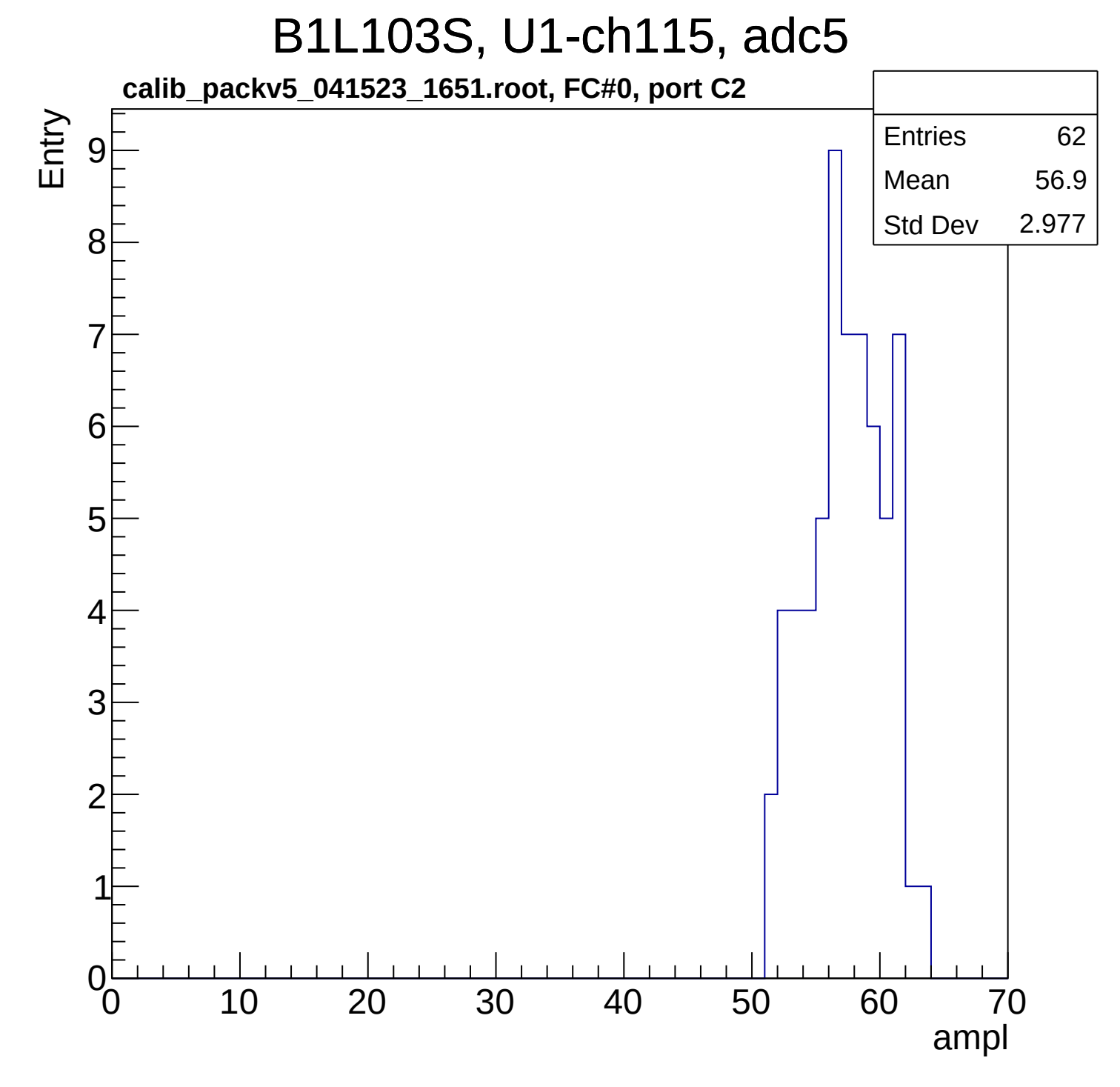
B1L103S, U1-ch115, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 56.9
Std Dev 2.977
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ampl
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3
4
5
6
7
8
9
0
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60
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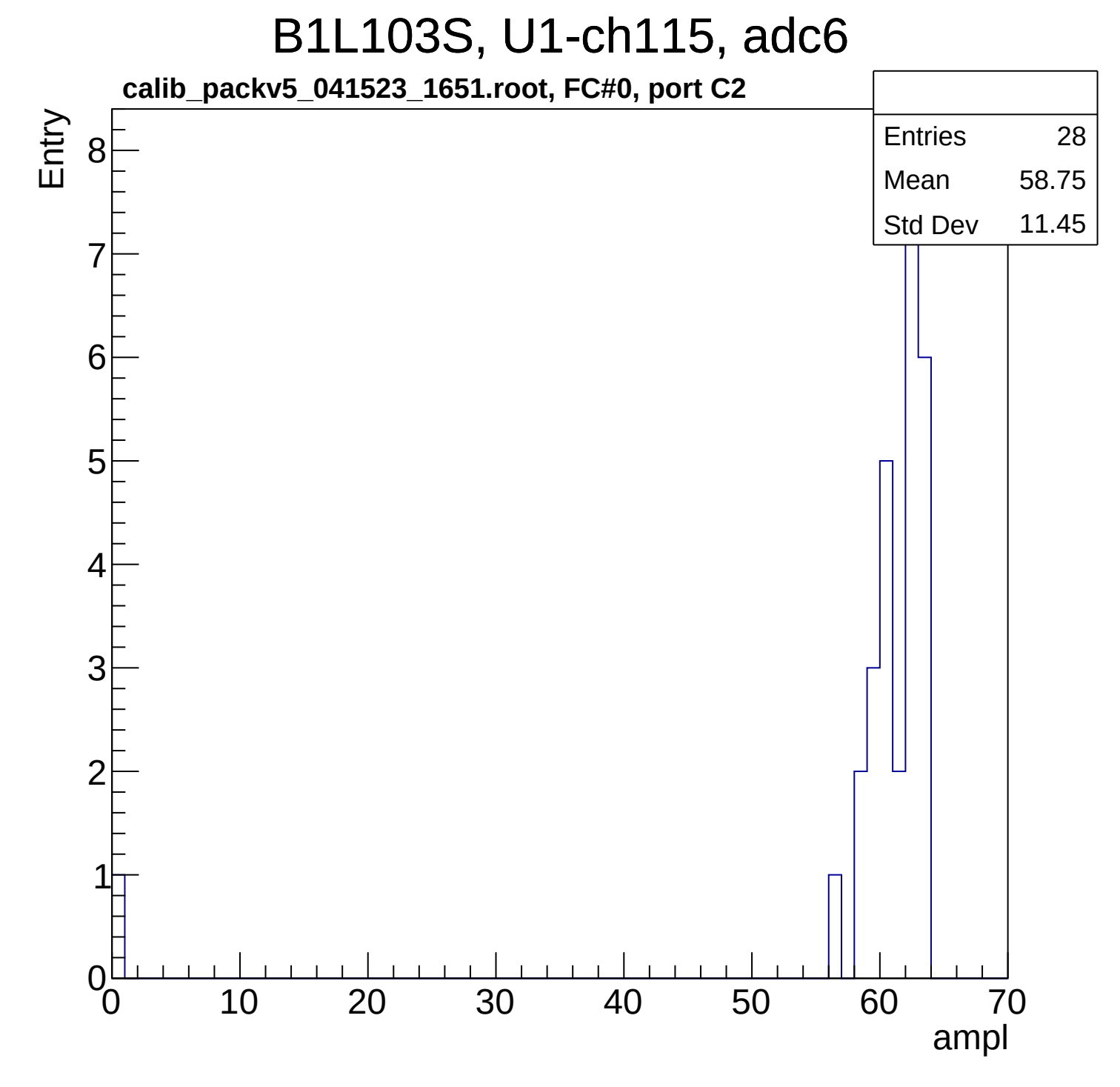
B1L103S, U1-ch115, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 28
Mean 58.75
Std Dev 11.45
Entry
ampl
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2
3
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5
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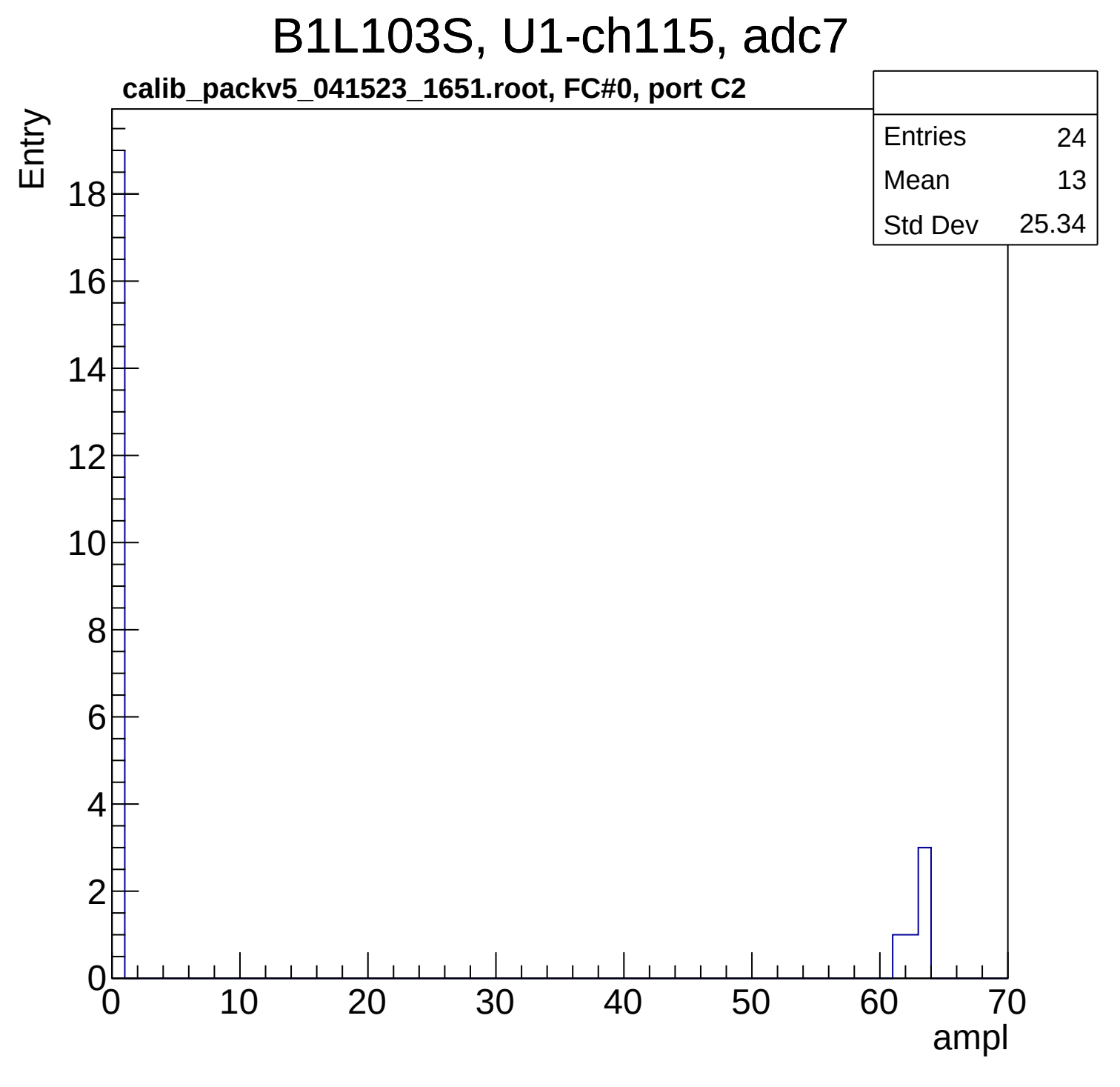
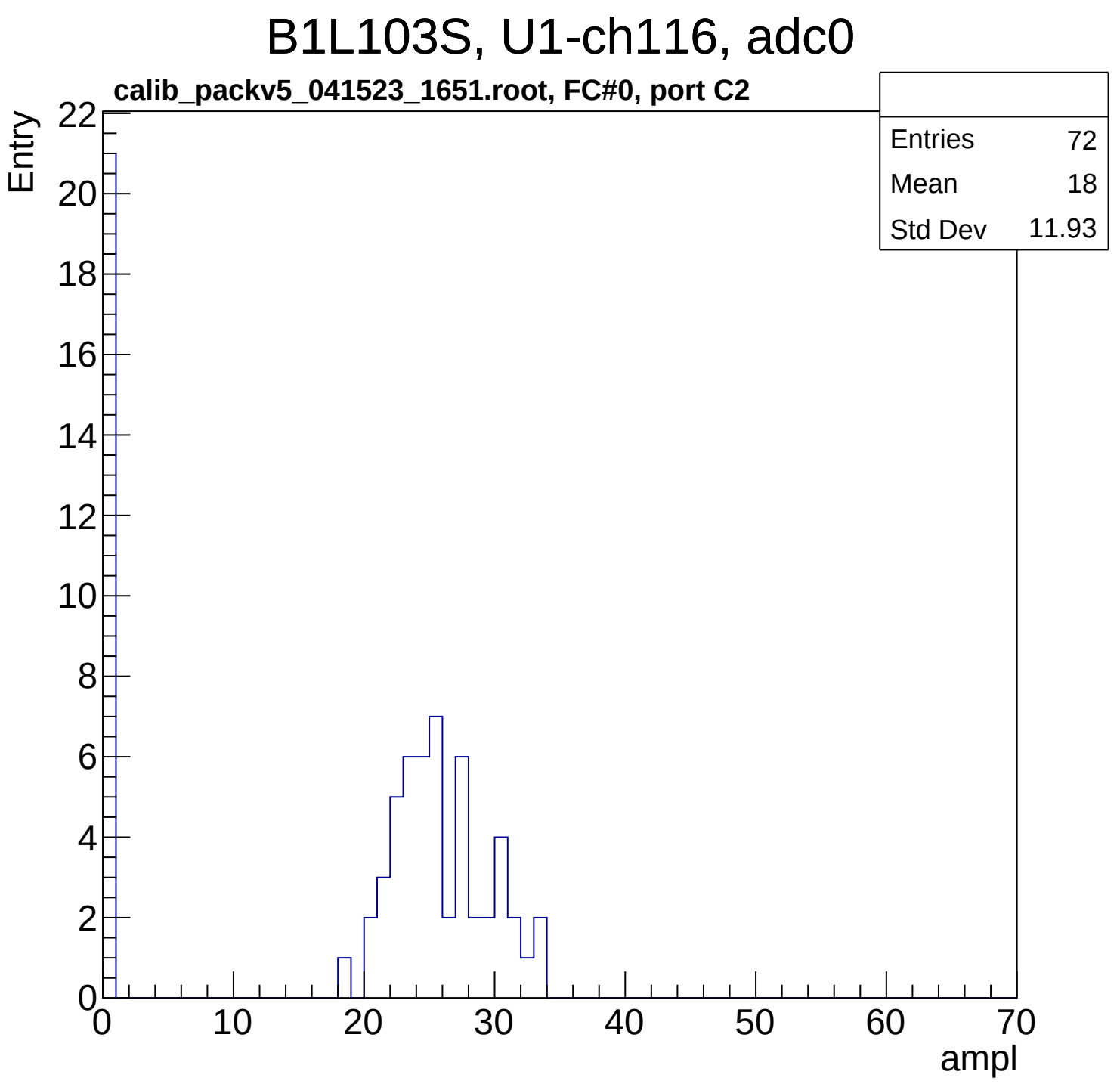

B1L103S, U1-ch115, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 24
Mean 13
Std Dev 25.34
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch116, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 18
Std Dev 11.93
Entry
ampl
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8
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12
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16
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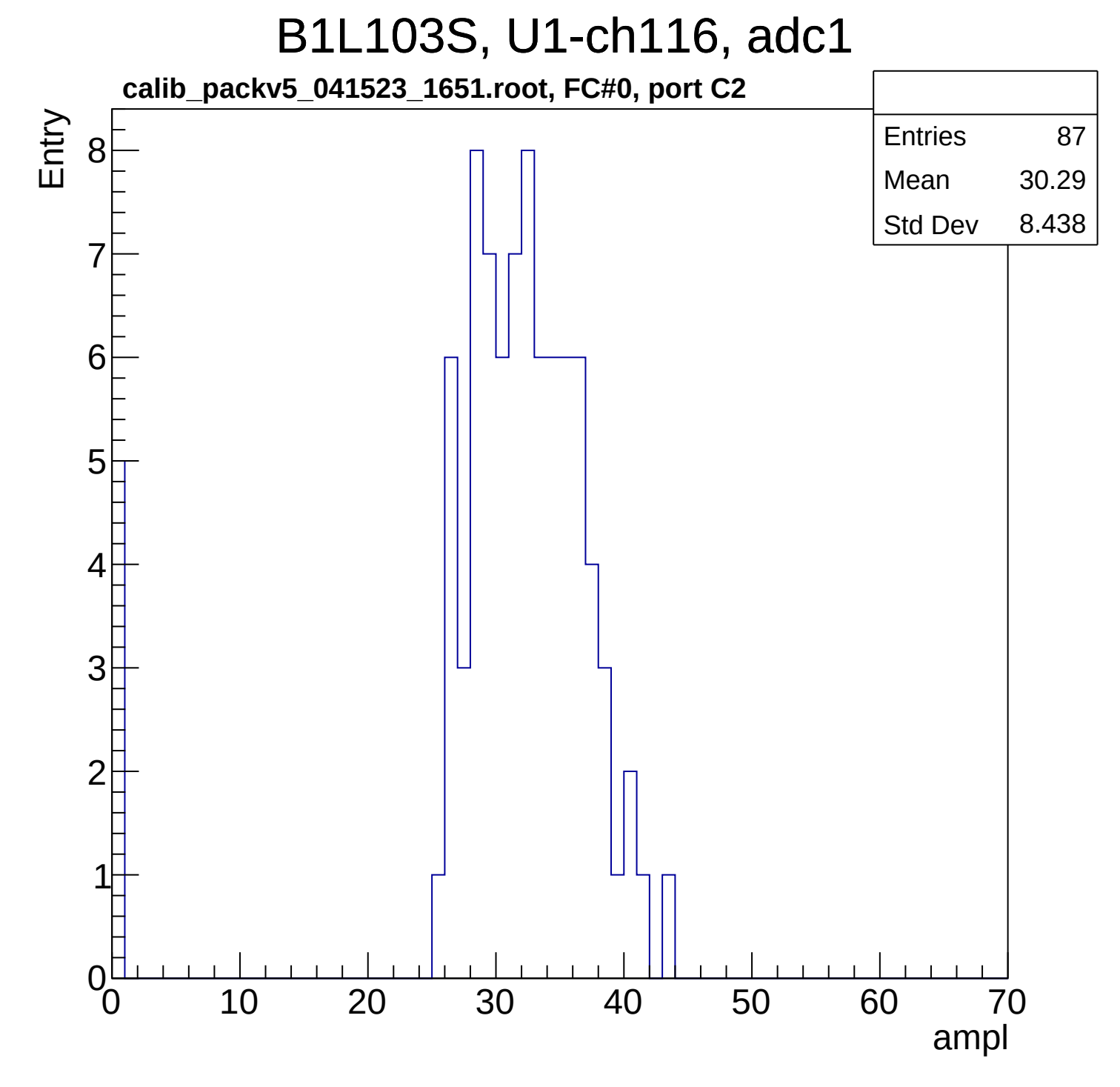
B1L103S, U1-ch116, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 87
Mean 30.29
Std Dev 8.438
Entry
ampl
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0
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60
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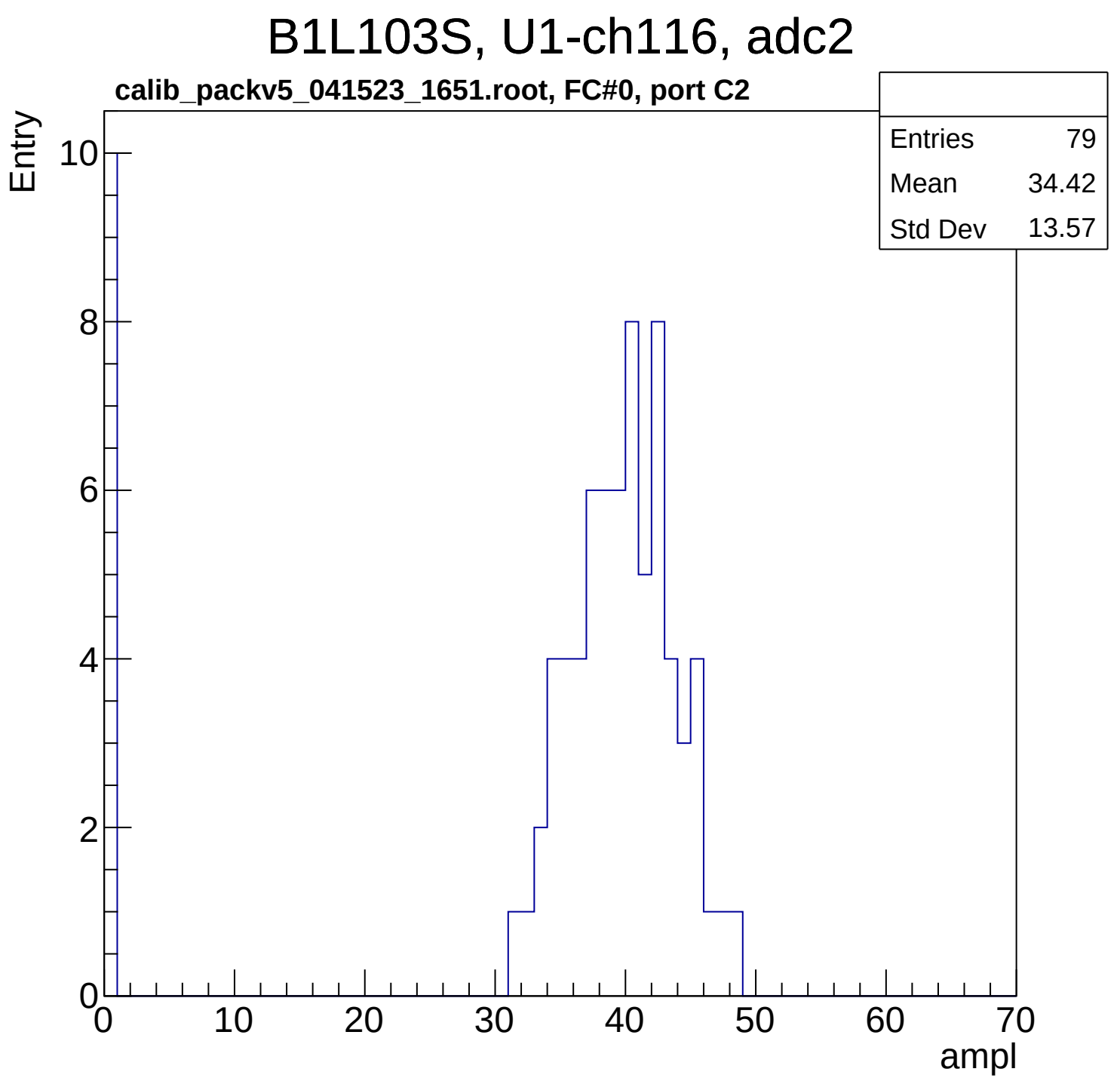
B1L103S, U1-ch116, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 34.42
Std Dev 13.57
Entry
ampl
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0
10
20
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40
50
60
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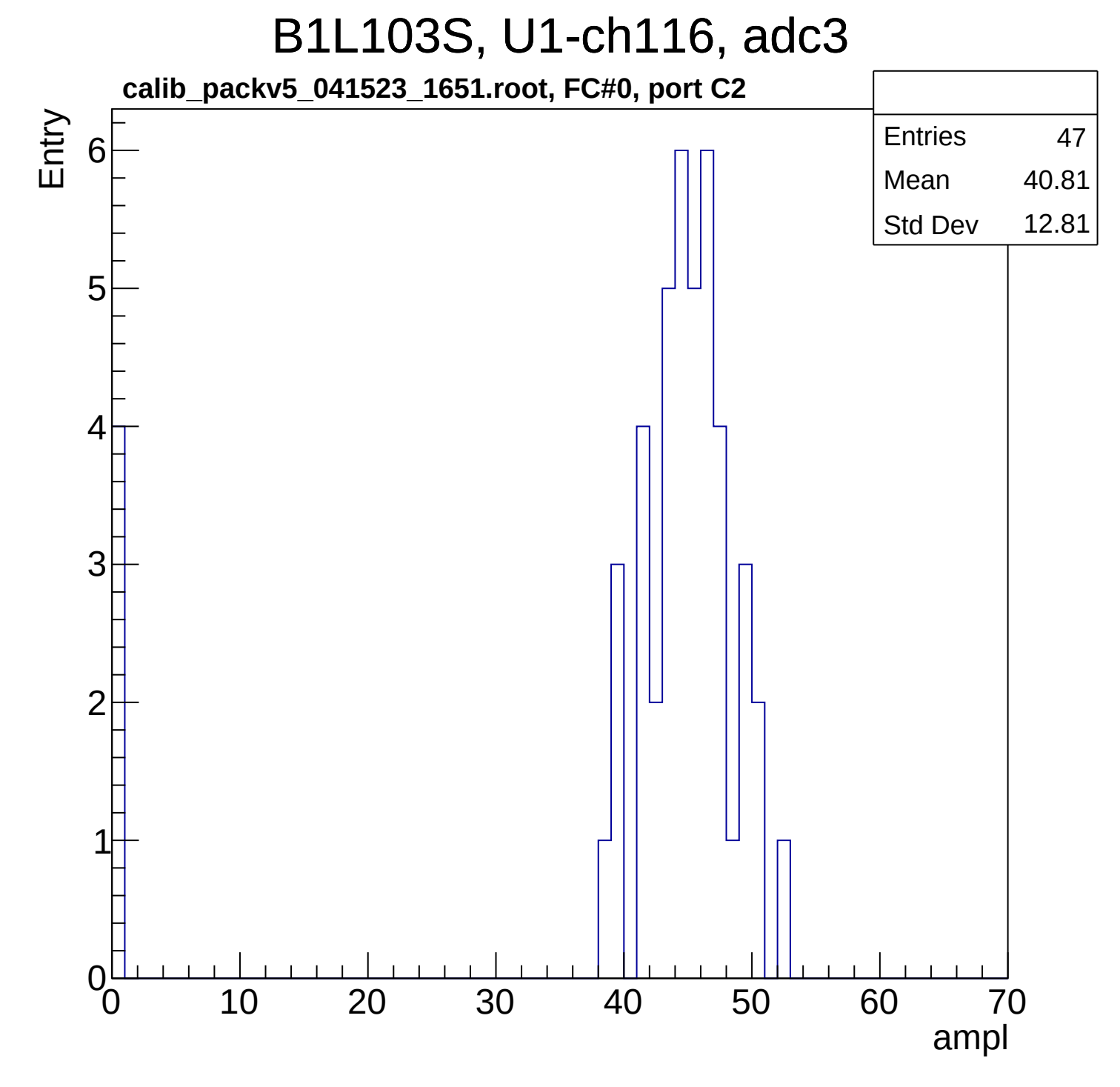
B1L103S, U1-ch116, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 40.81
Std Dev 12.81
Entry
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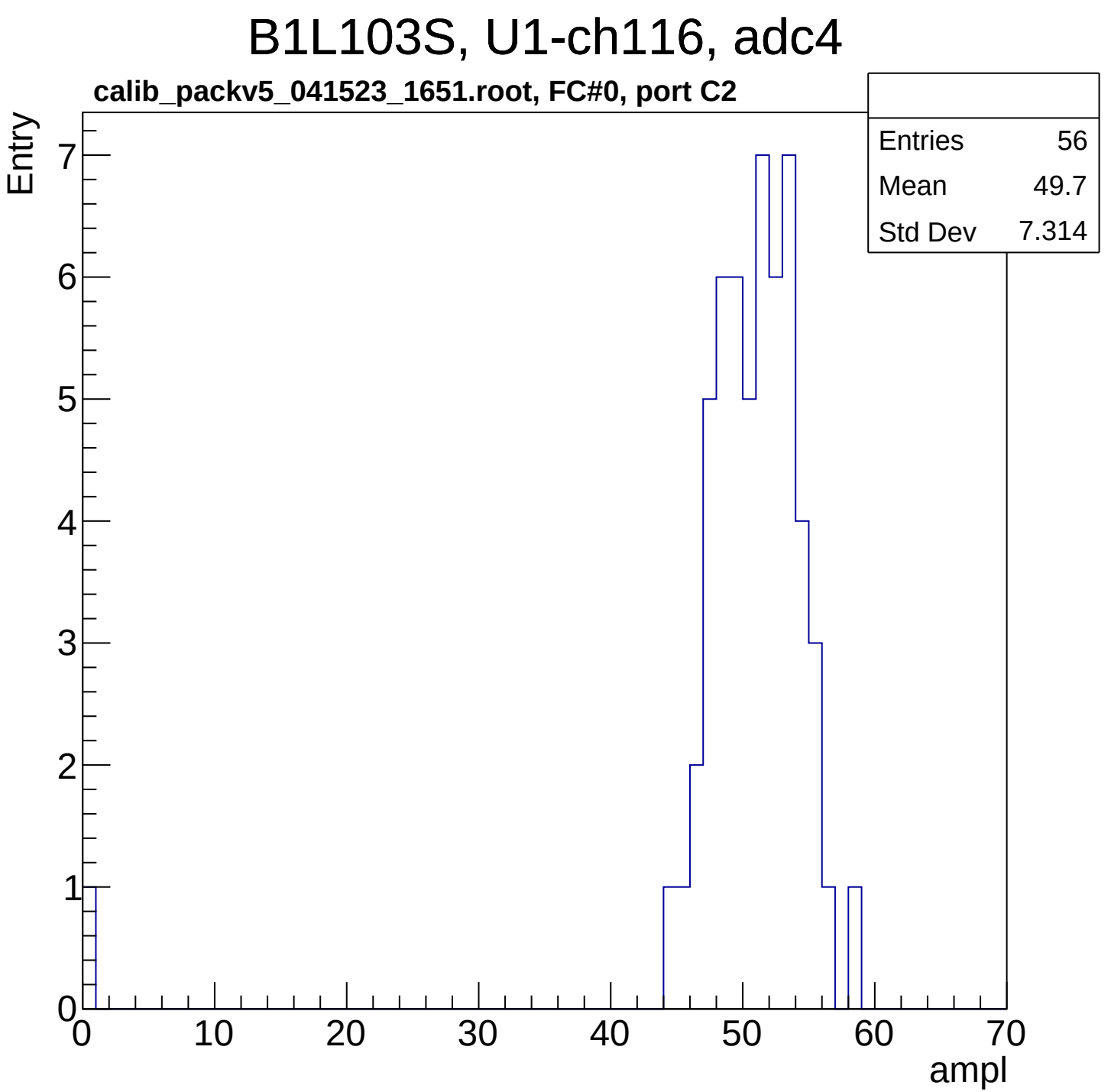
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch116, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 49.7
Std Dev 7.314
Entry
ampl
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3
4
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0
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40
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60
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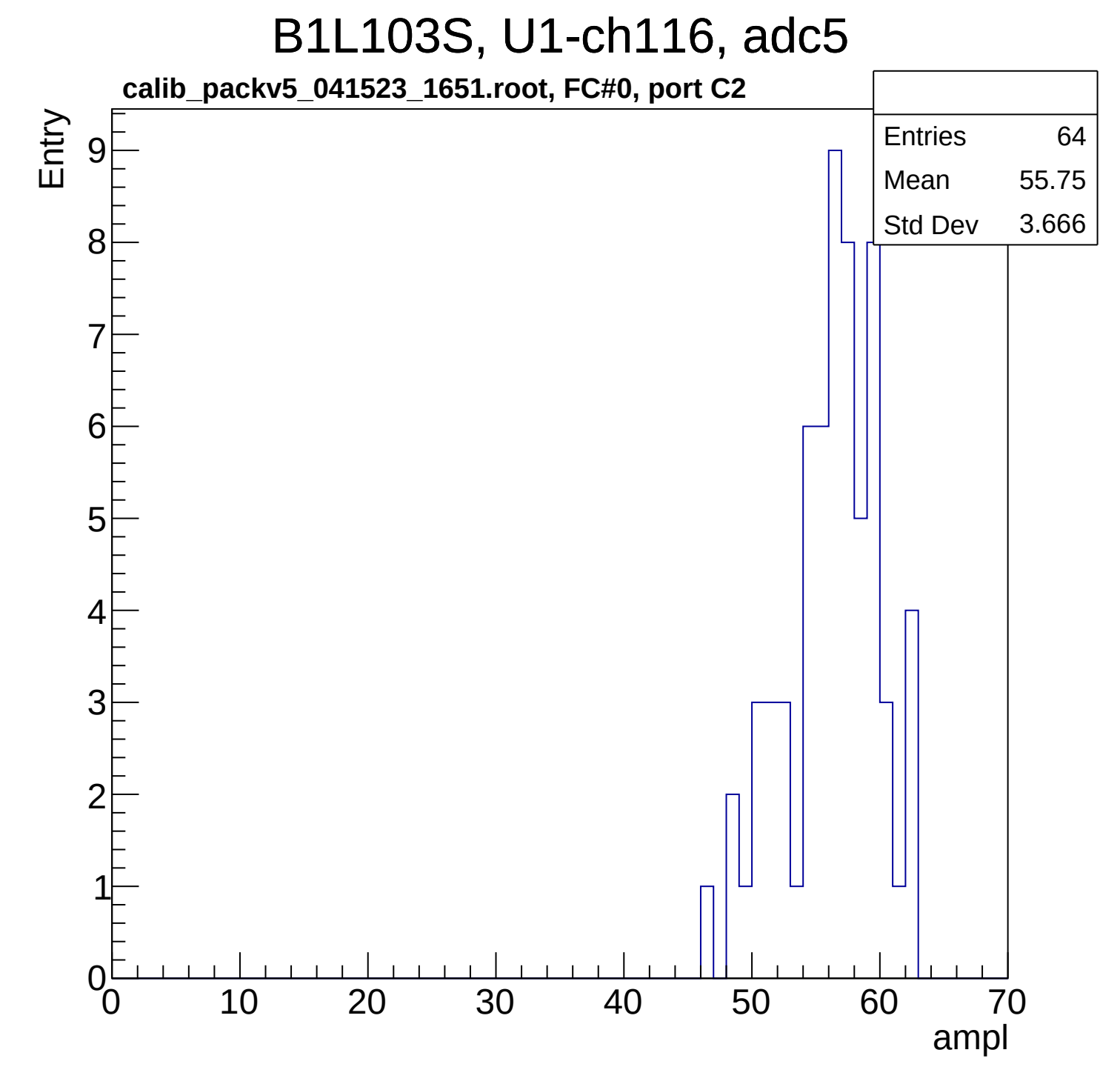
B1L103S, U1-ch116, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 55.75
Std Dev 3.666
Entry
ampl
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3
4
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6
7
8
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0
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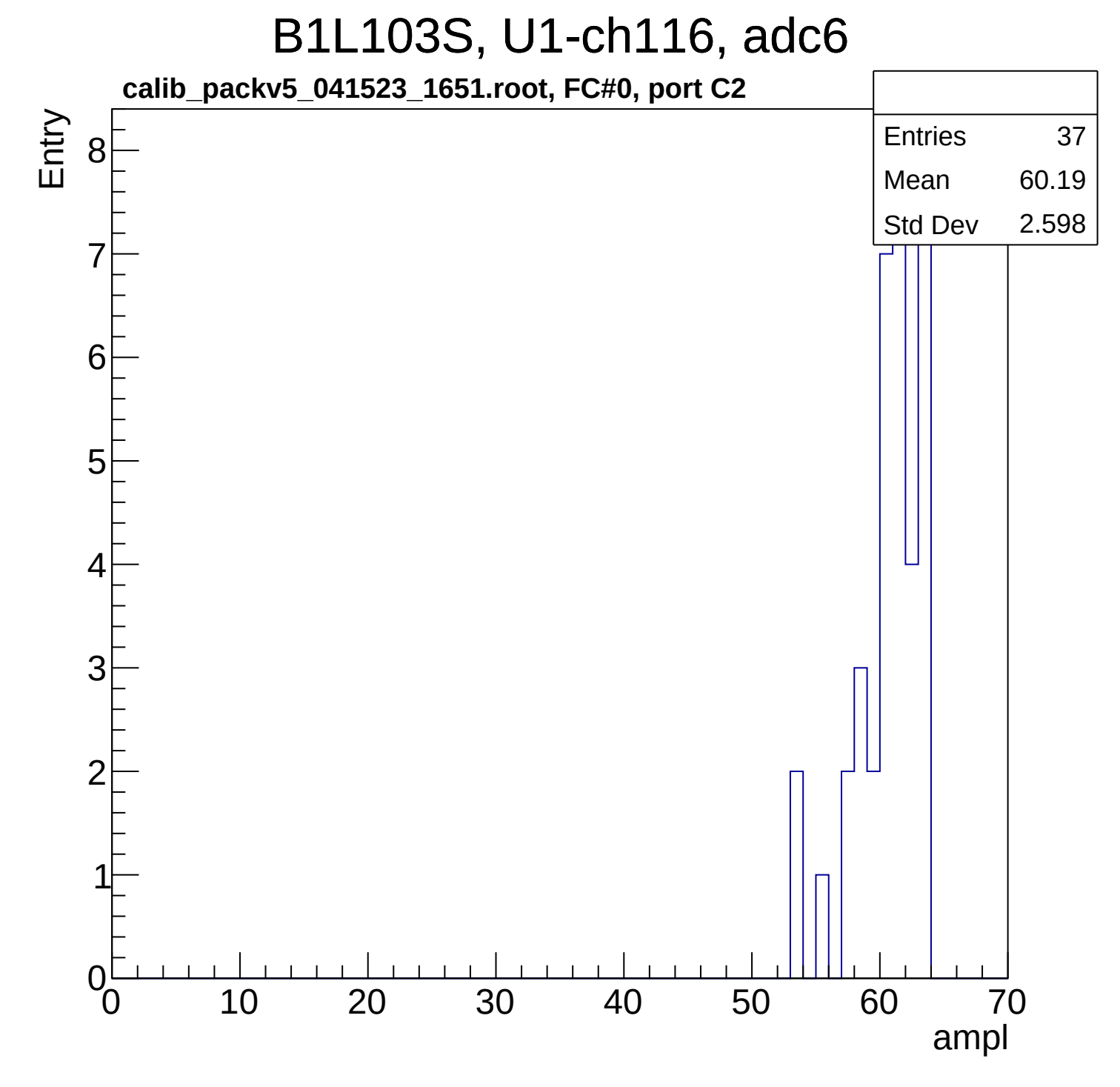
B1L103S, U1-ch116, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 37
Mean 60.19
Std Dev 2.598
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
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40
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60
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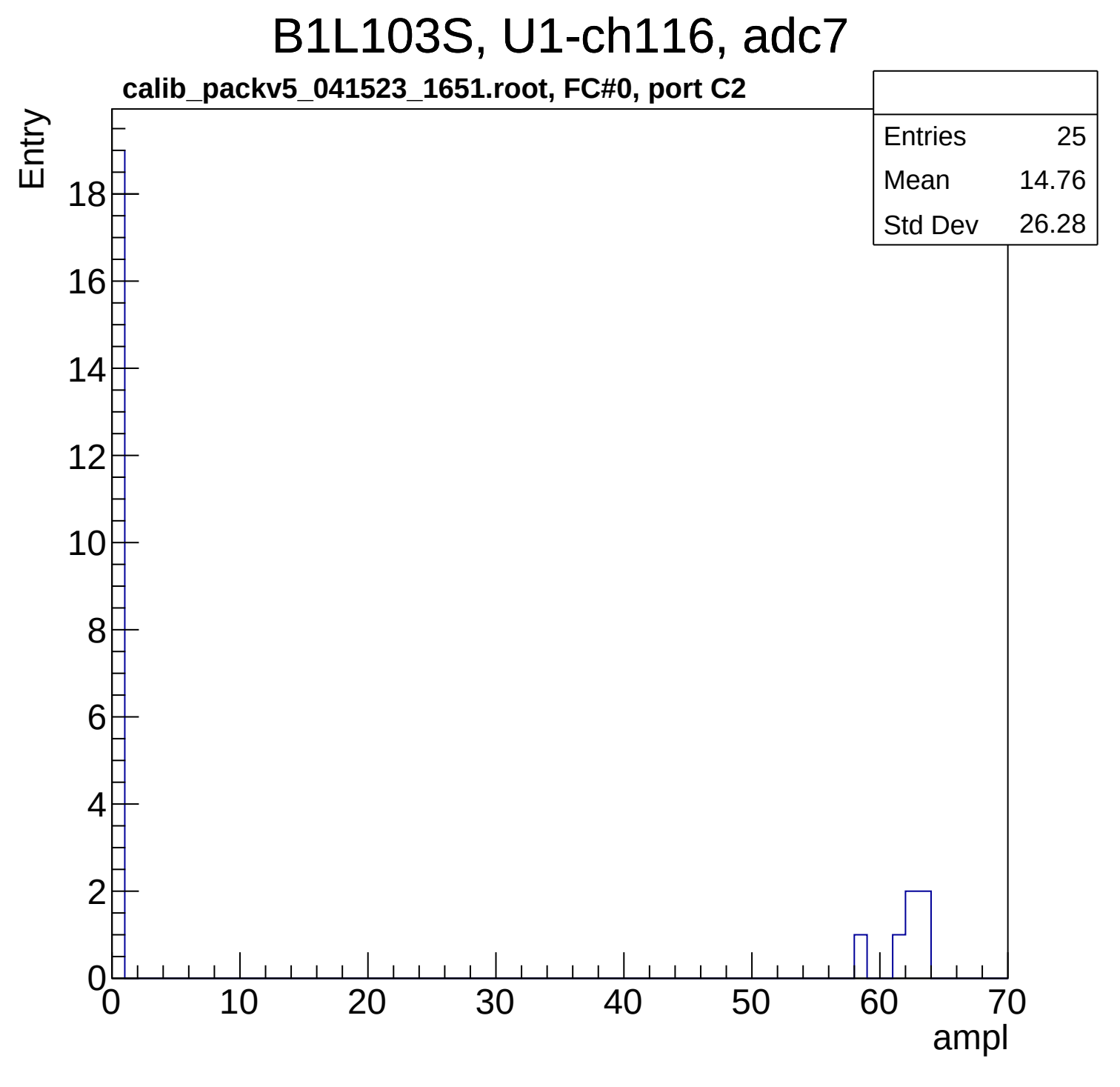
B1L103S, U1-ch116, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 25
Mean 14.76
Std Dev 26.28
Entry
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6
8
10
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14
16
18
0
10
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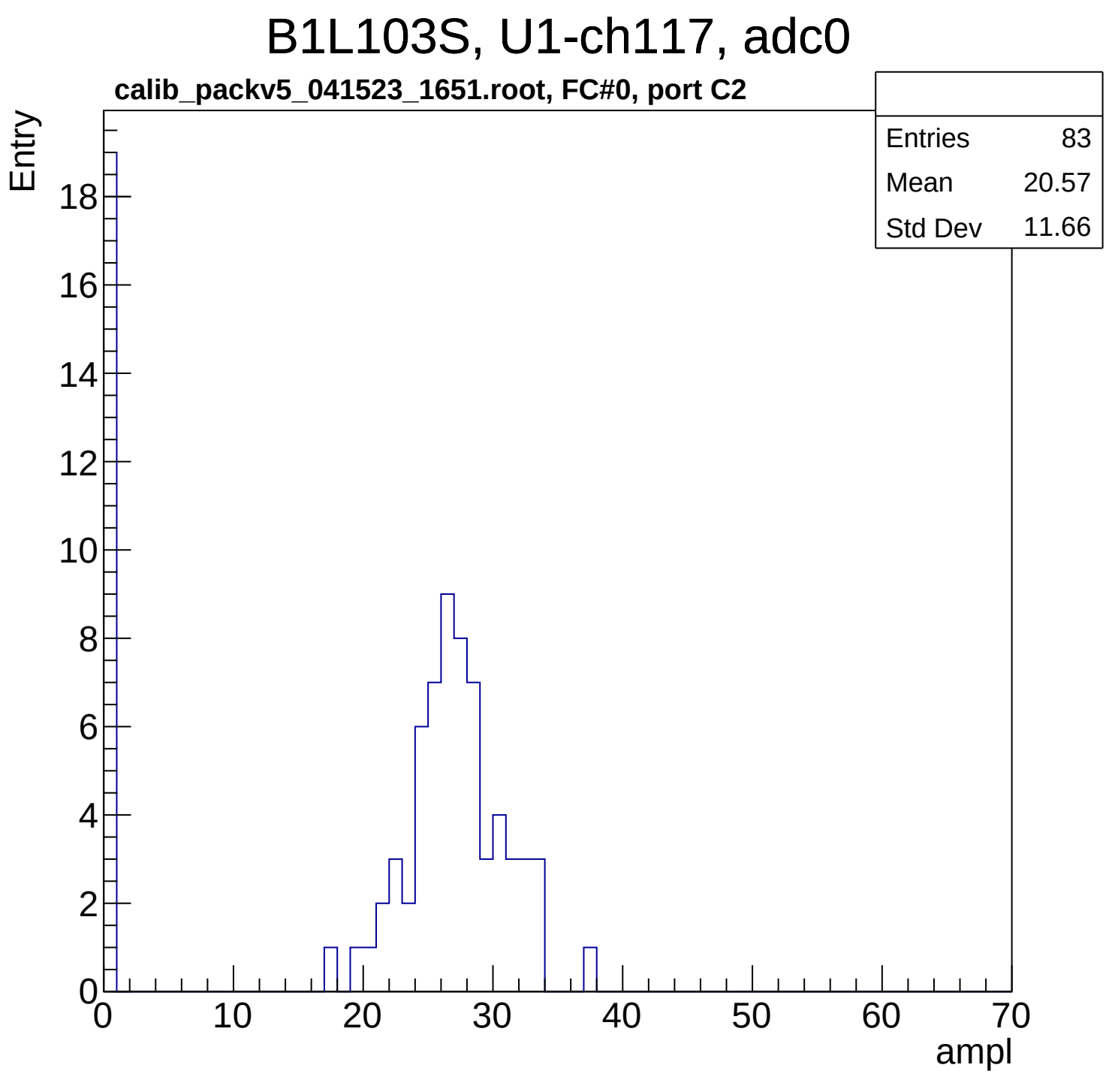
50
60
70
ampl


B1L103S, U1-ch117, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 20.57
Std Dev 11.66
Entry
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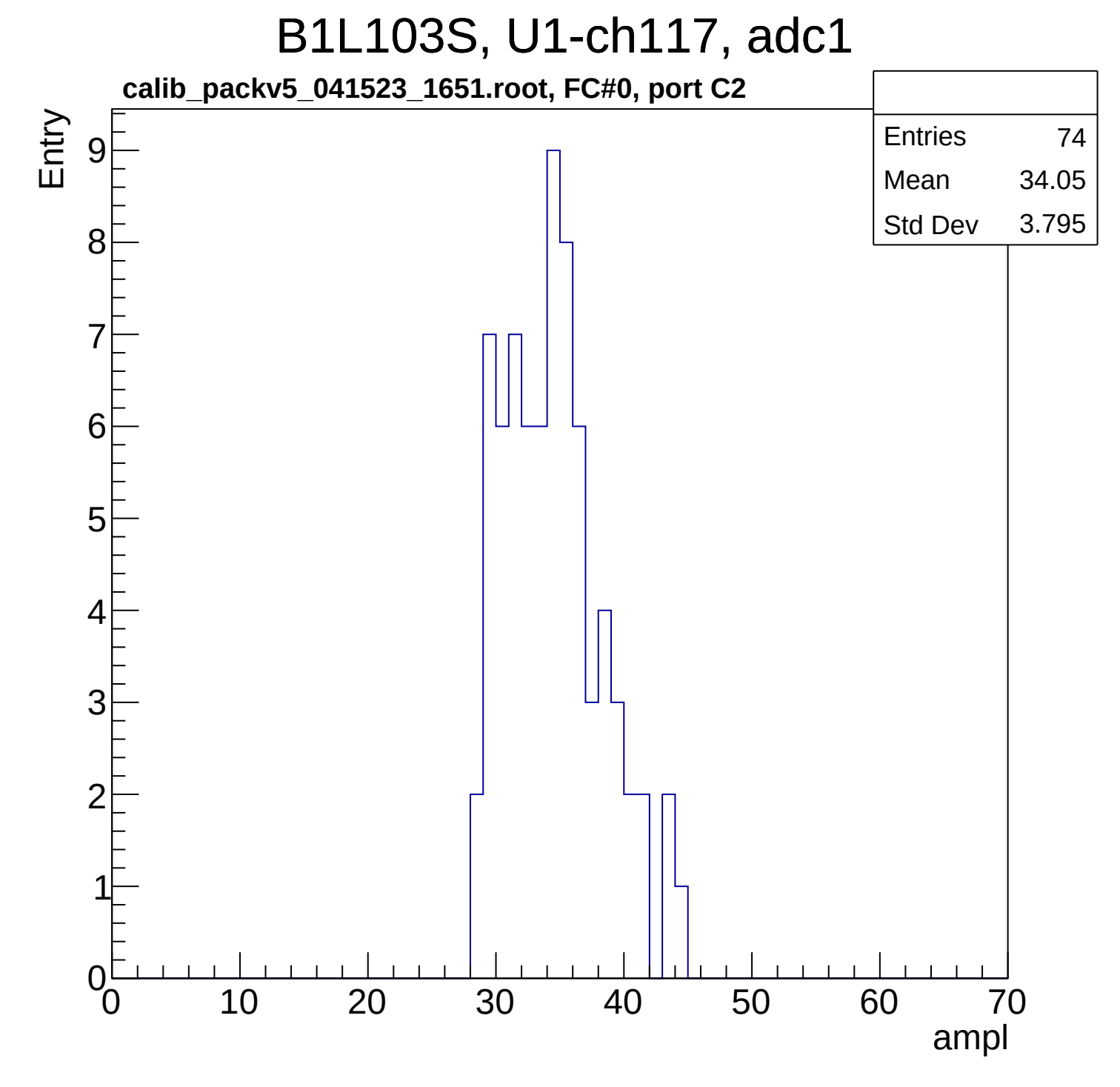
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch117, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 34.05
Std Dev 3.795
Entry
ampl
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3
4
5
6
7
8
9
0
10
20
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40
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60
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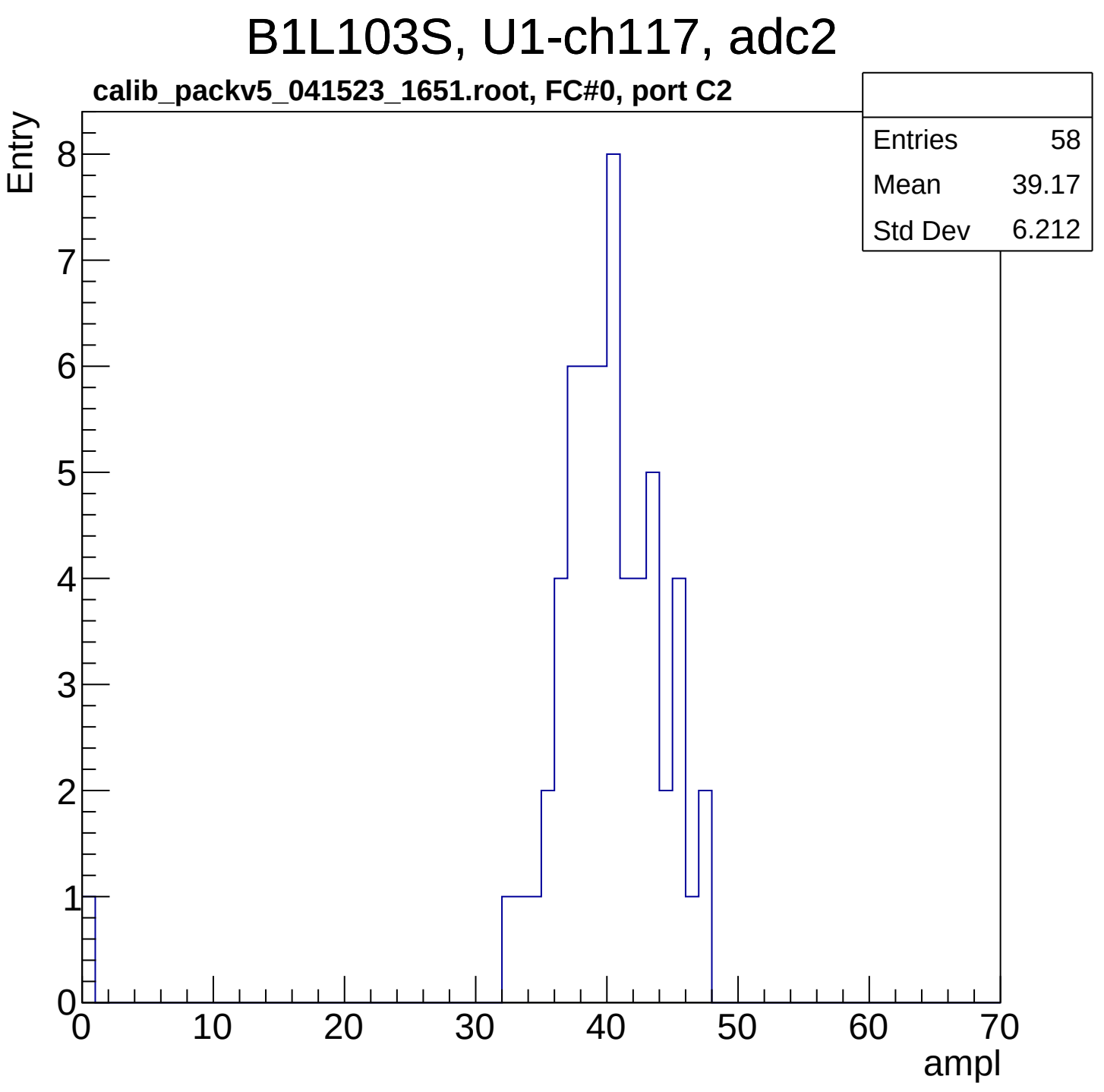
B1L103S, U1-ch117, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 39.17
Std Dev 6.212
Entry
ampl
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2
3
4
5
6
7
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0
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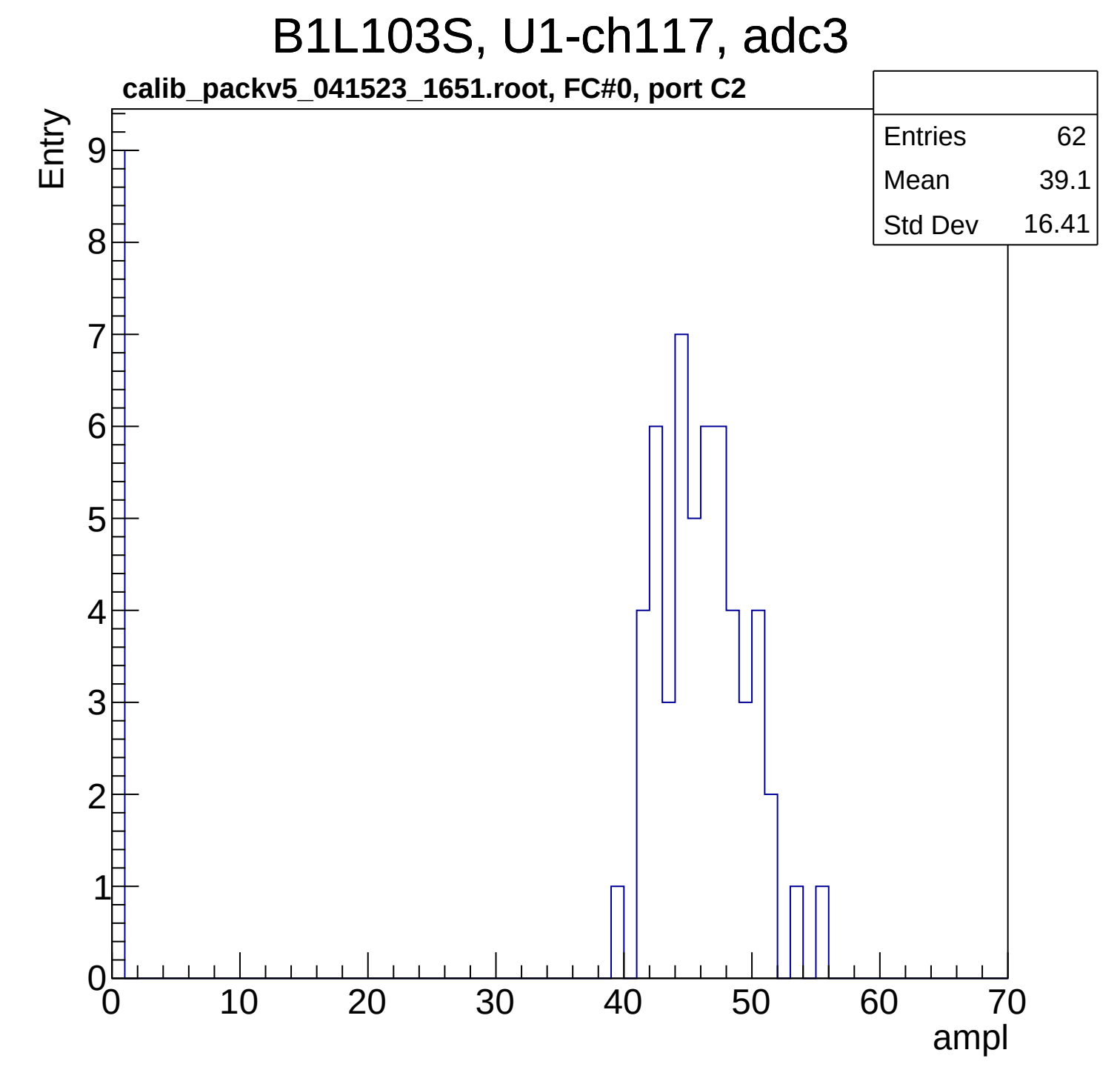
B1L103S, U1-ch117, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 39.1
Std Dev 16.41
Entry
ampl
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3
4
5
6
7
8
9
0
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60
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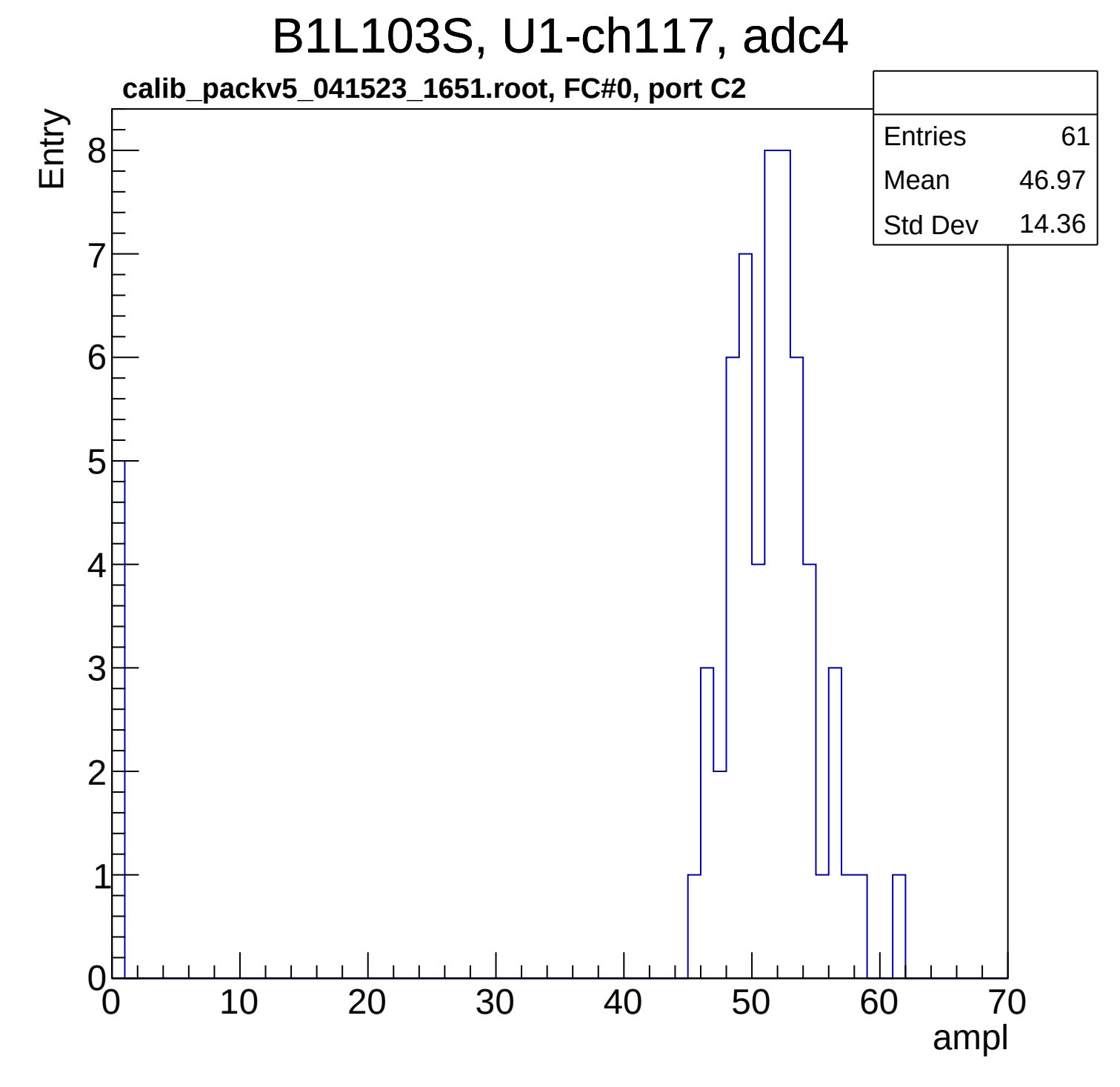
B1L103S, U1-ch117, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 46.97
Std Dev 14.36
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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40
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60
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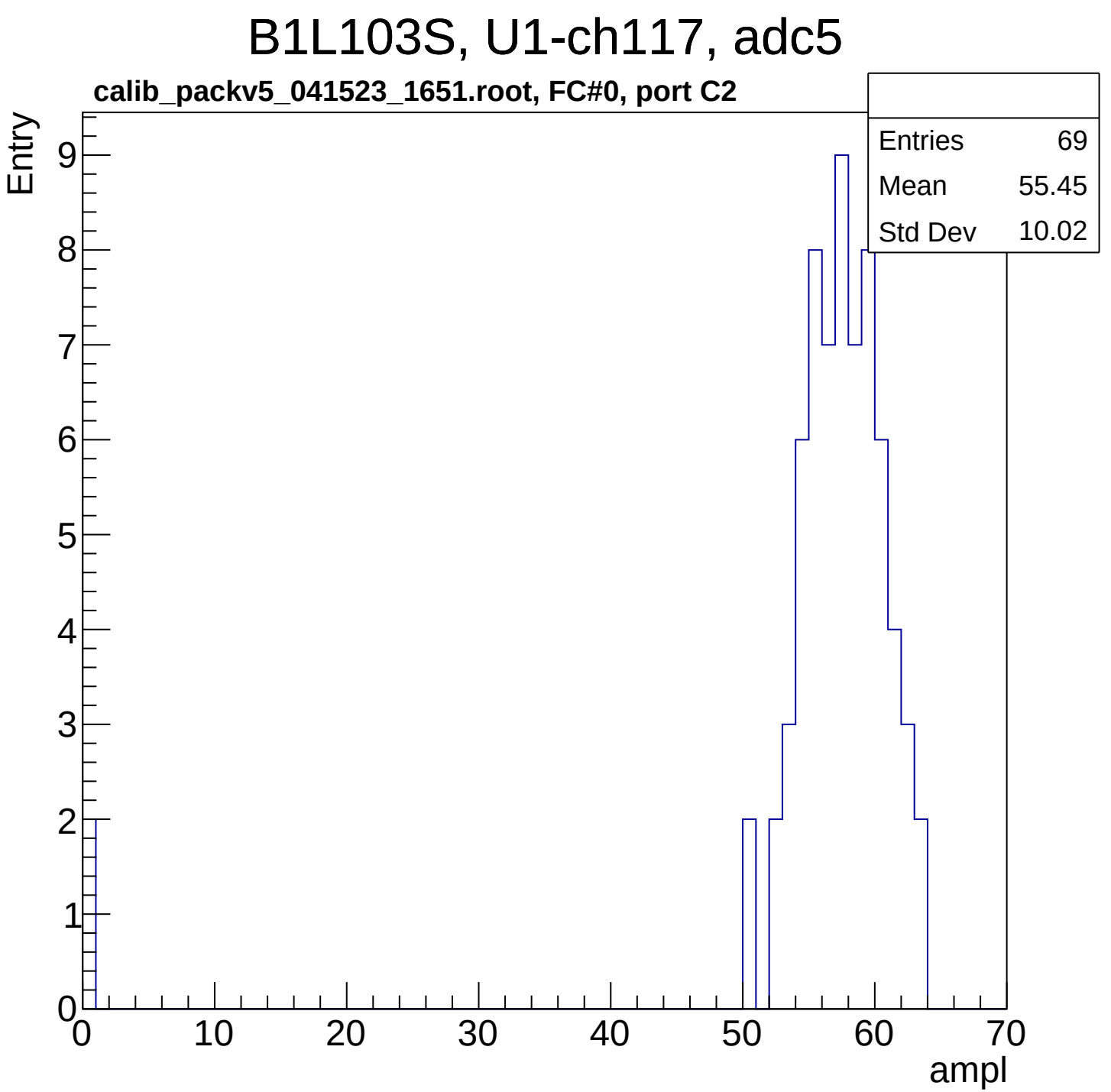
B1L103S, U1-ch117, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 55.45
Std Dev 10.02
Entry
ampl
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3
4
5
6
7
8
9
0
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60
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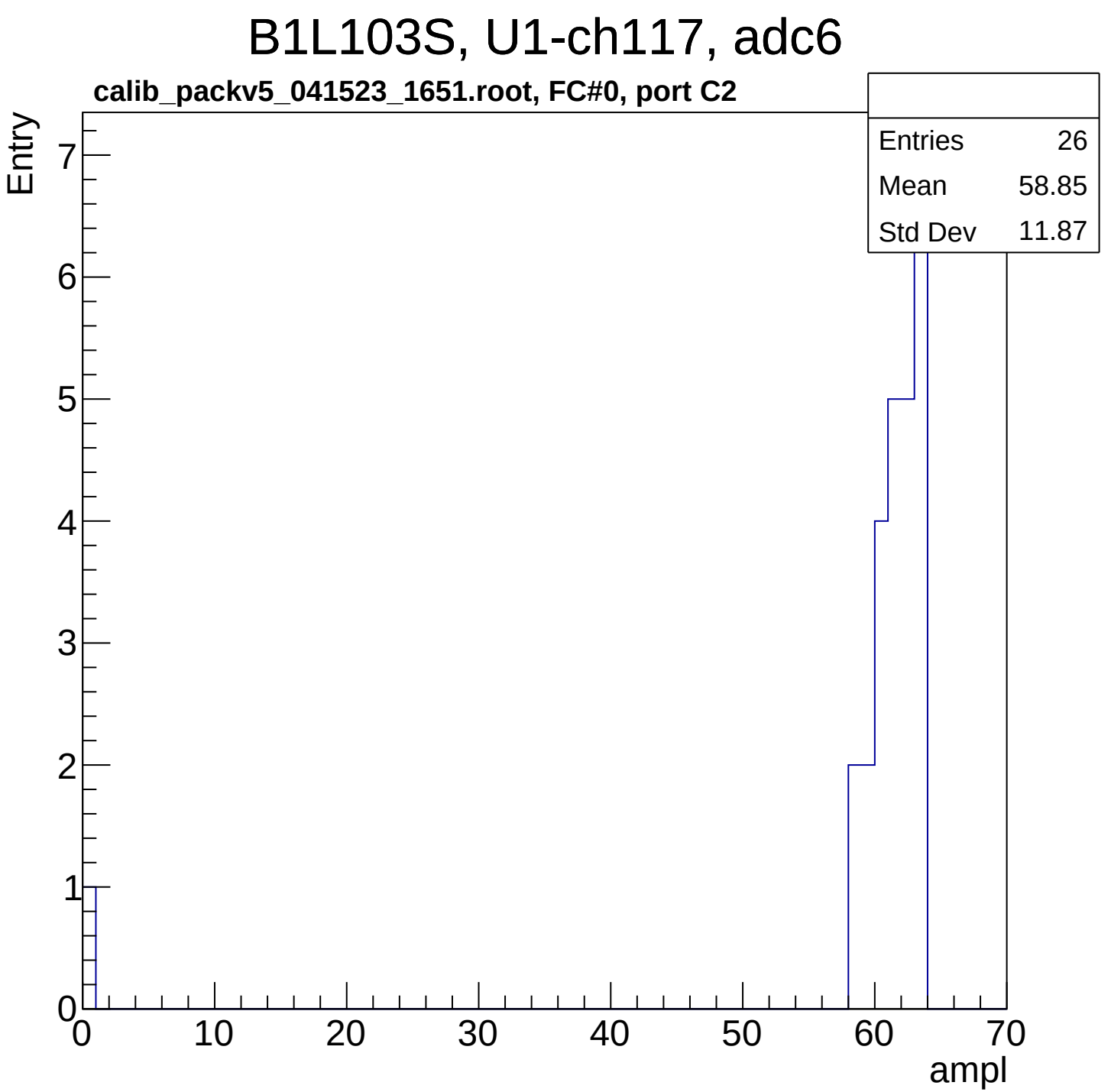
B1L103S, U1-ch117, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 26
Mean 58.85
Std Dev 11.87
Entry
ampl
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2
3
4
5
6
7
0
10
20
30
40
50
60
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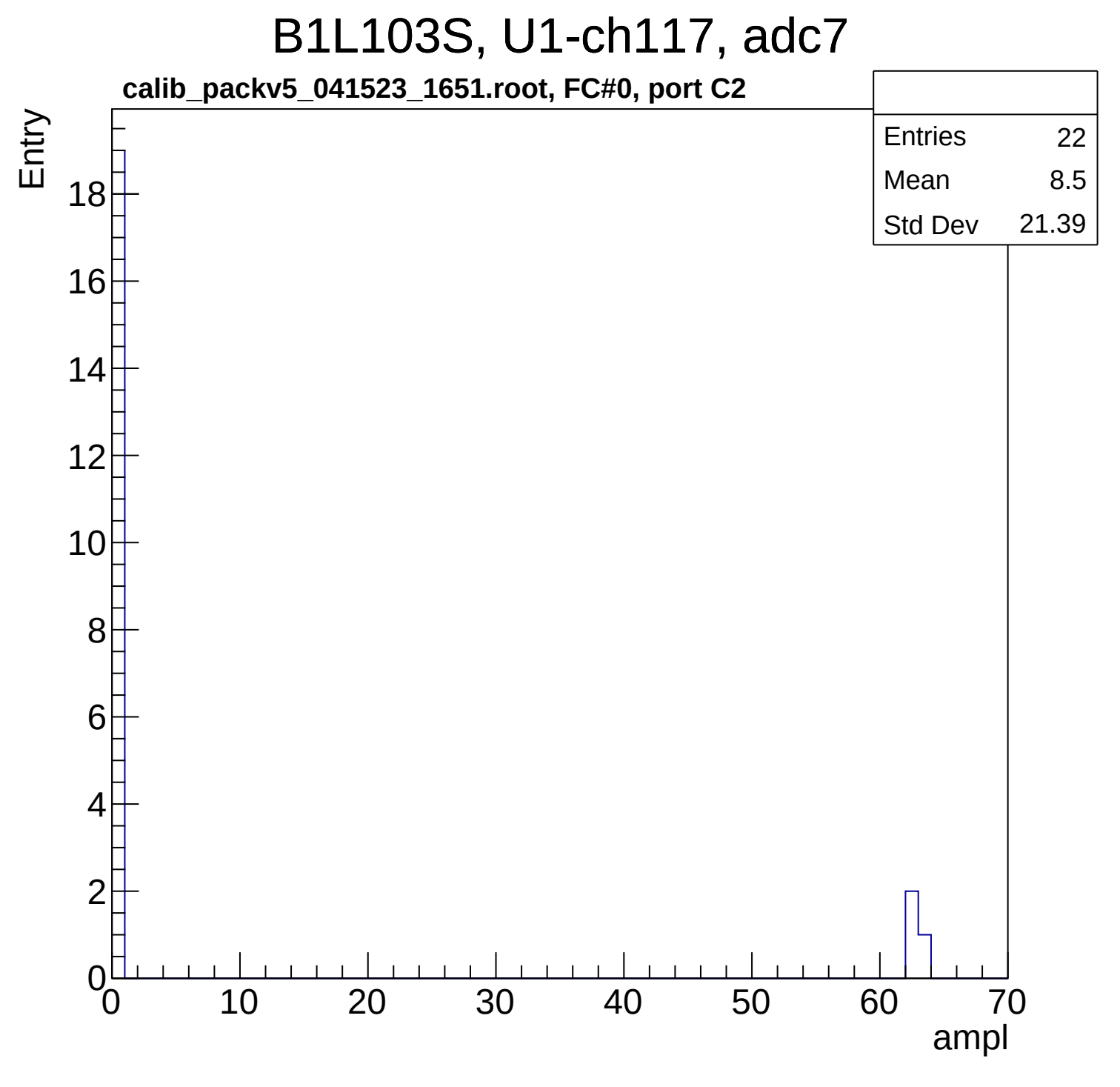
B1L103S, U1-ch117, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 8.5
Std Dev 21.39
Entry
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6
8
10
12
14
16
18
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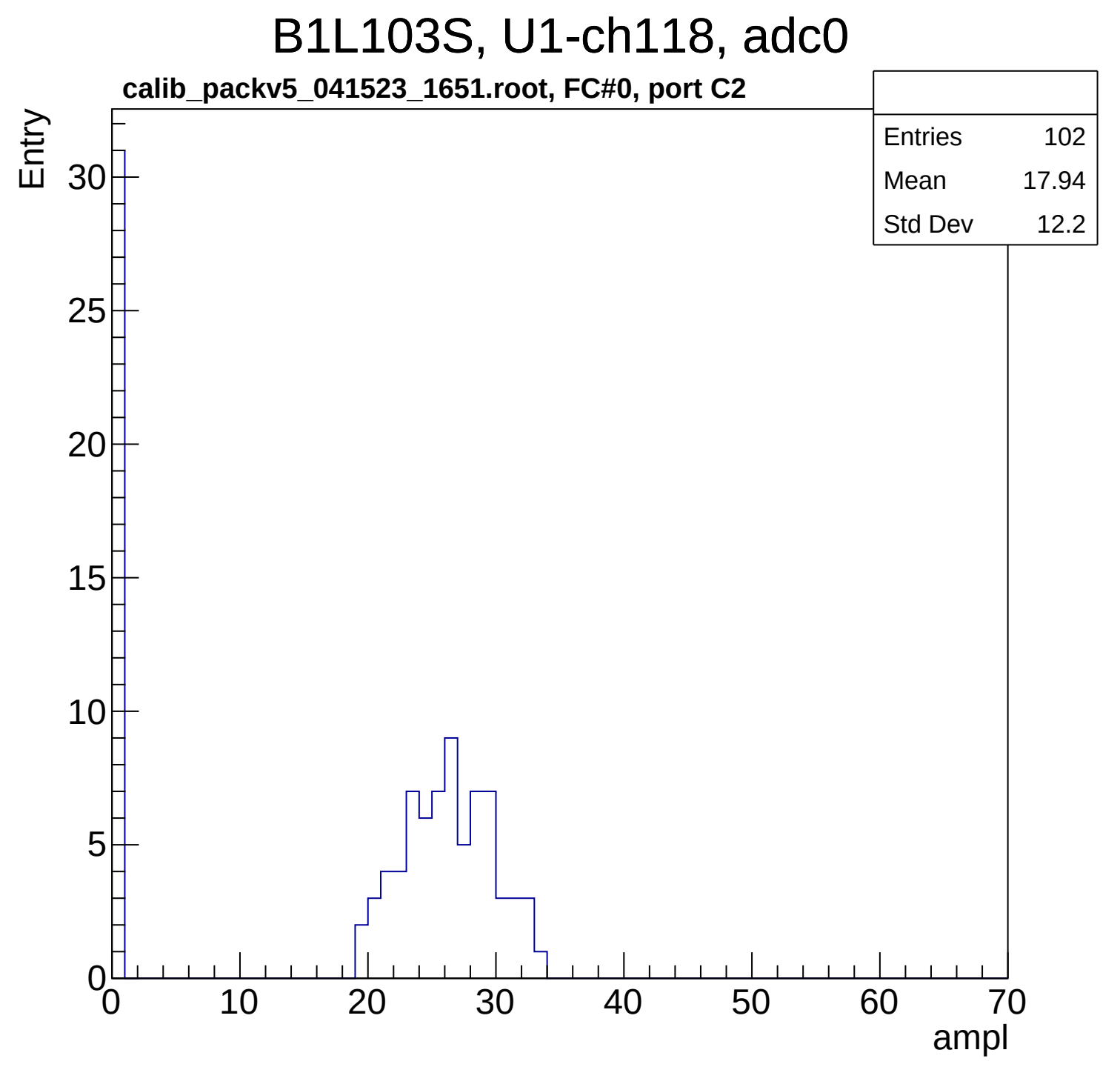
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch118, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 102
Mean 17.94
Std Dev 12.2
Entry
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10
15
20
25
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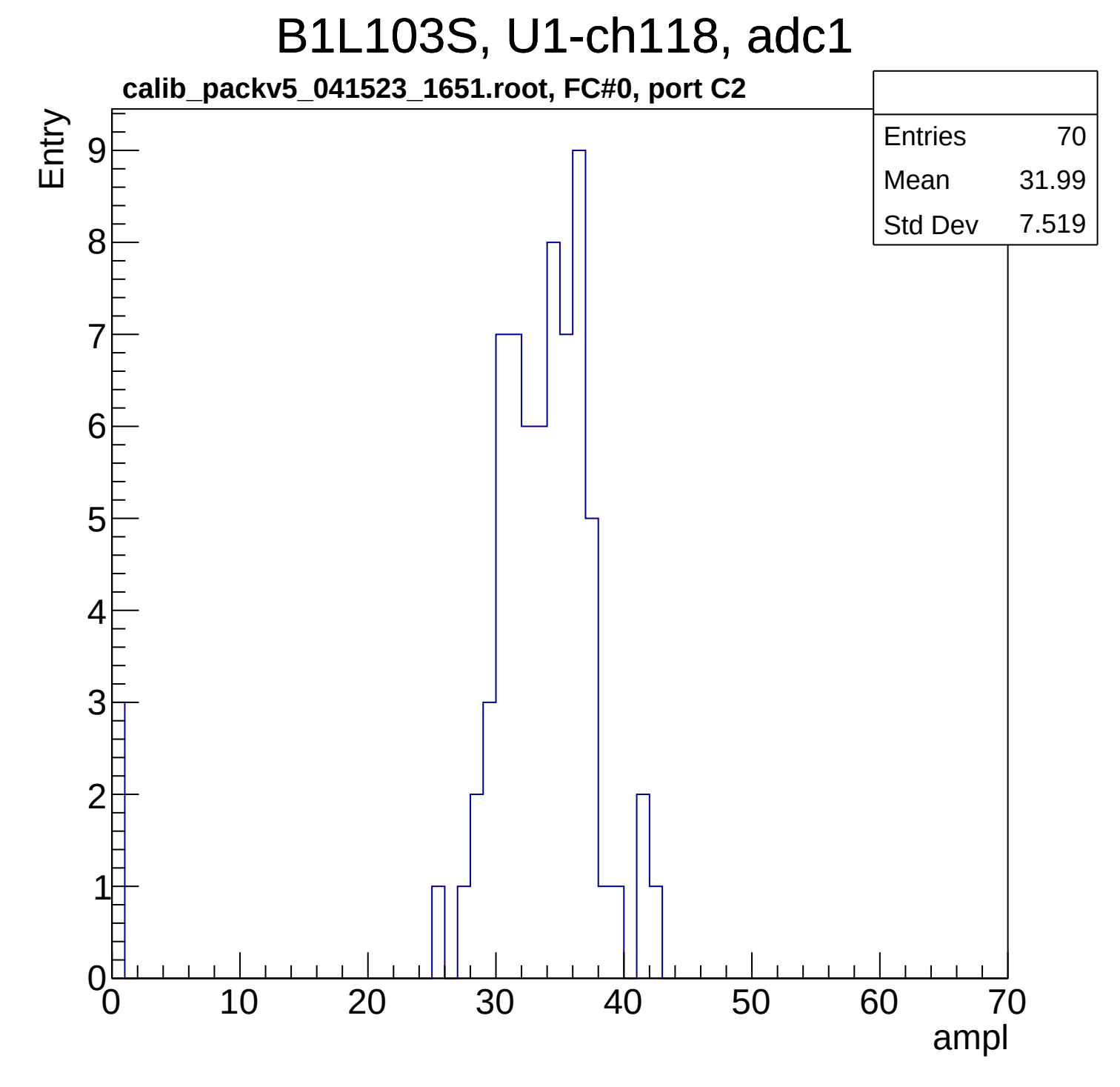
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch118, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 31.99
Std Dev 7.519
Entry
ampl
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3
4
5
6
7
8
9
0
10
20
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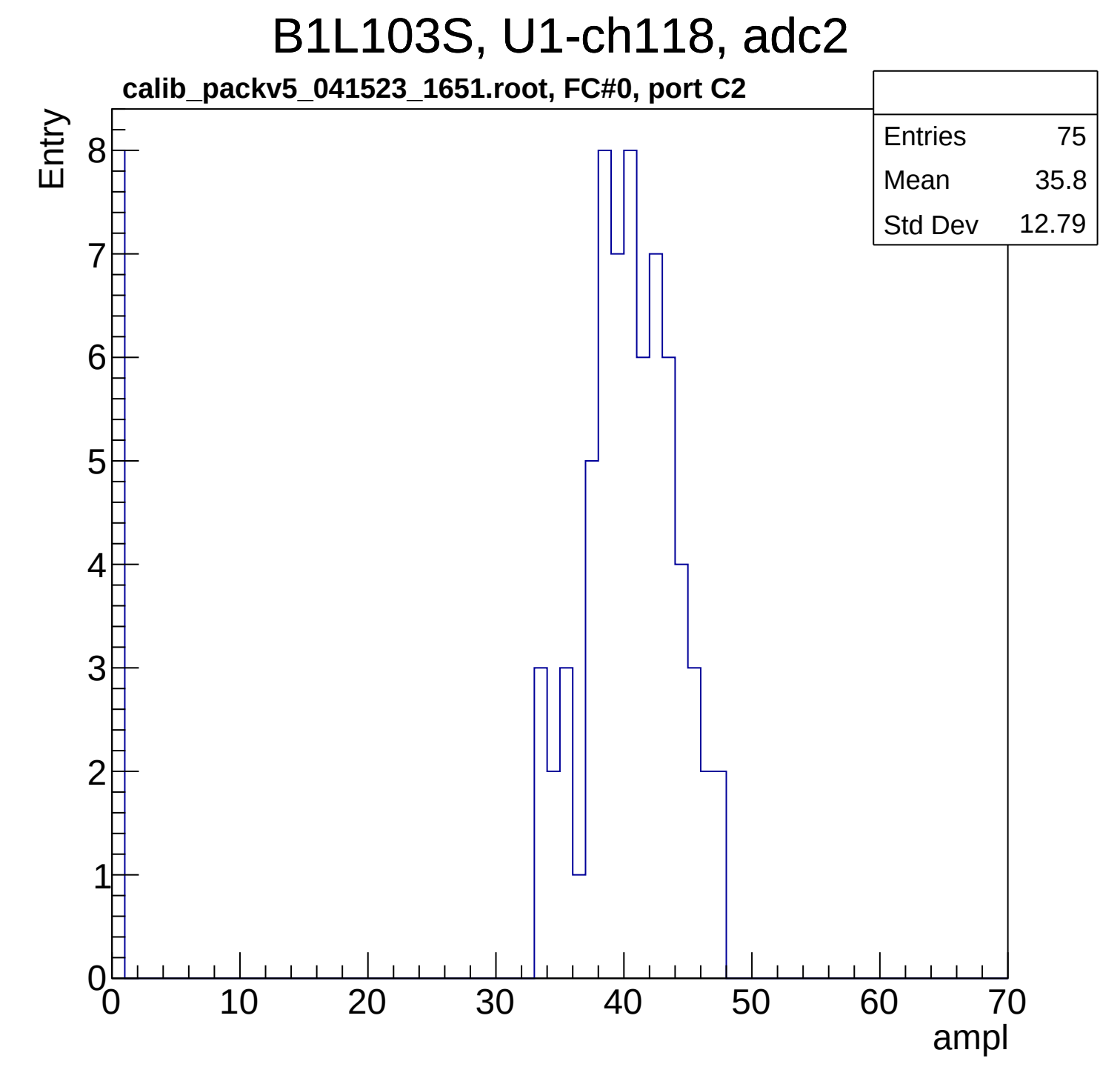
40
50
60
70


B1L103S, U1-ch118, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 35.8
Std Dev 12.79
Entry
ampl
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2
3
4
5
6
7
8
0
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20
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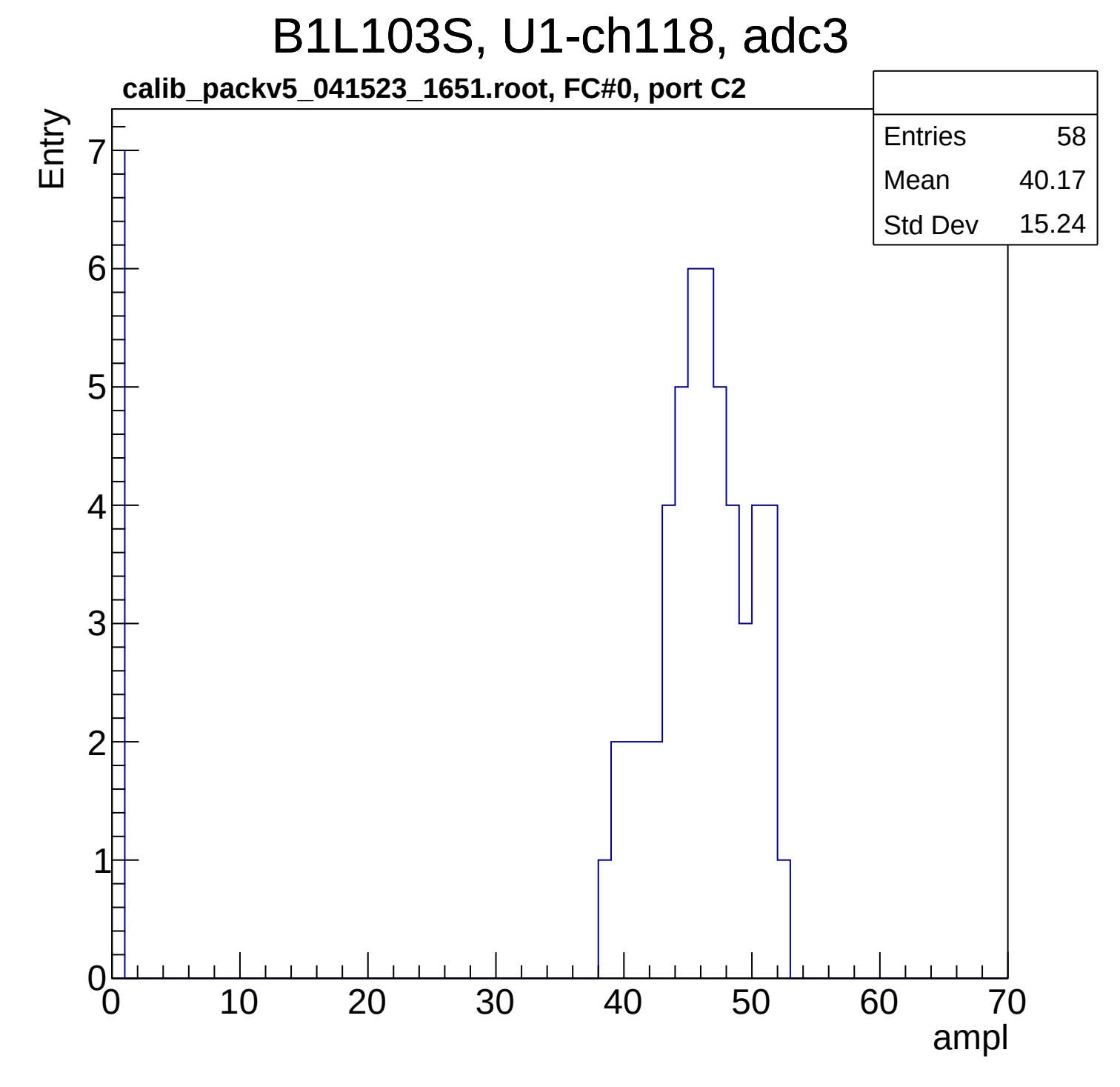
40
50
60
70


B1L103S, U1-ch118, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 40.17
Std Dev 15.24
Entry
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3
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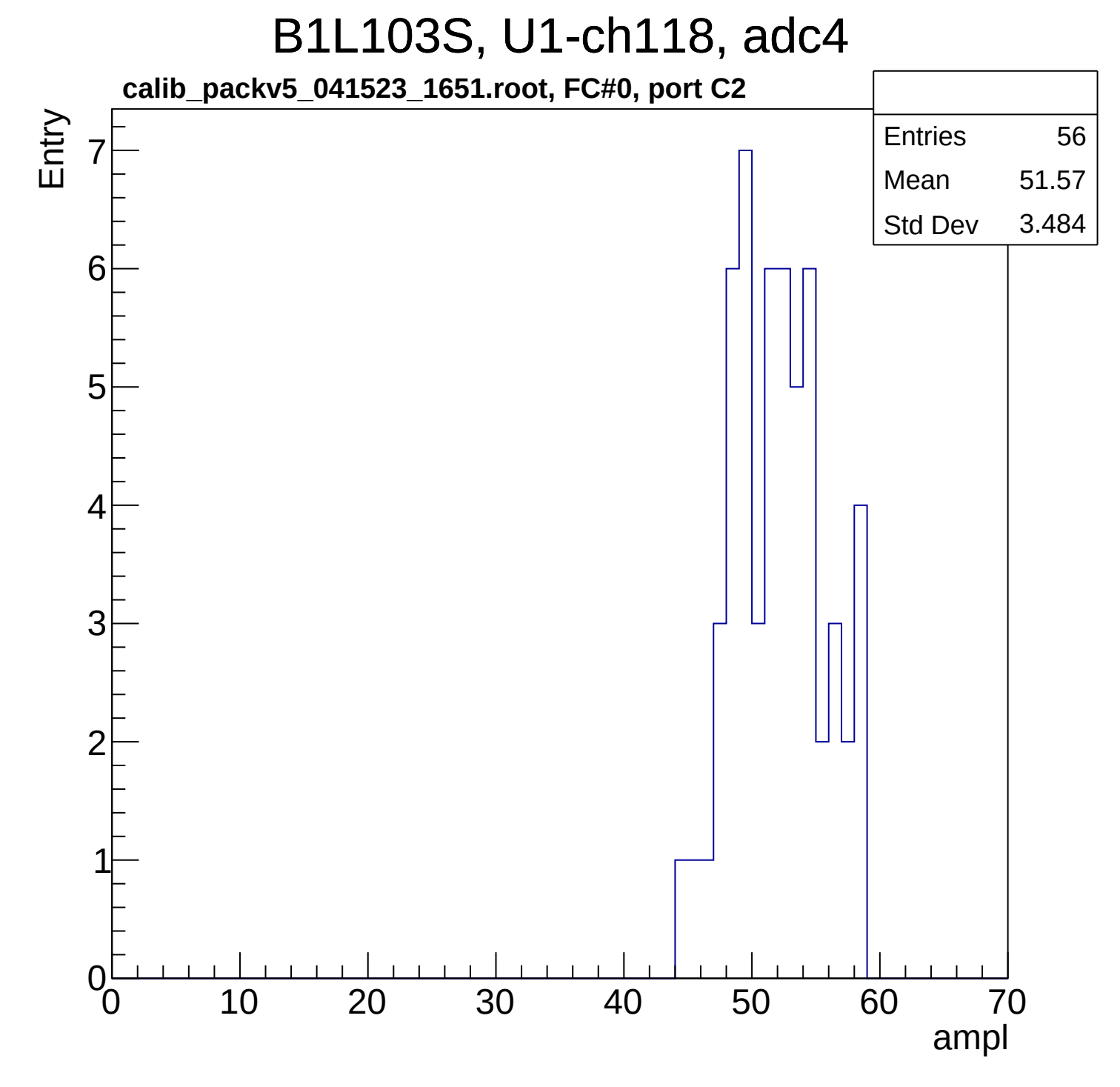
70
ampl


B1L103S, U1-ch118, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 51.57
Std Dev 3.484
Entry
ampl
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3
4
5
6
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0
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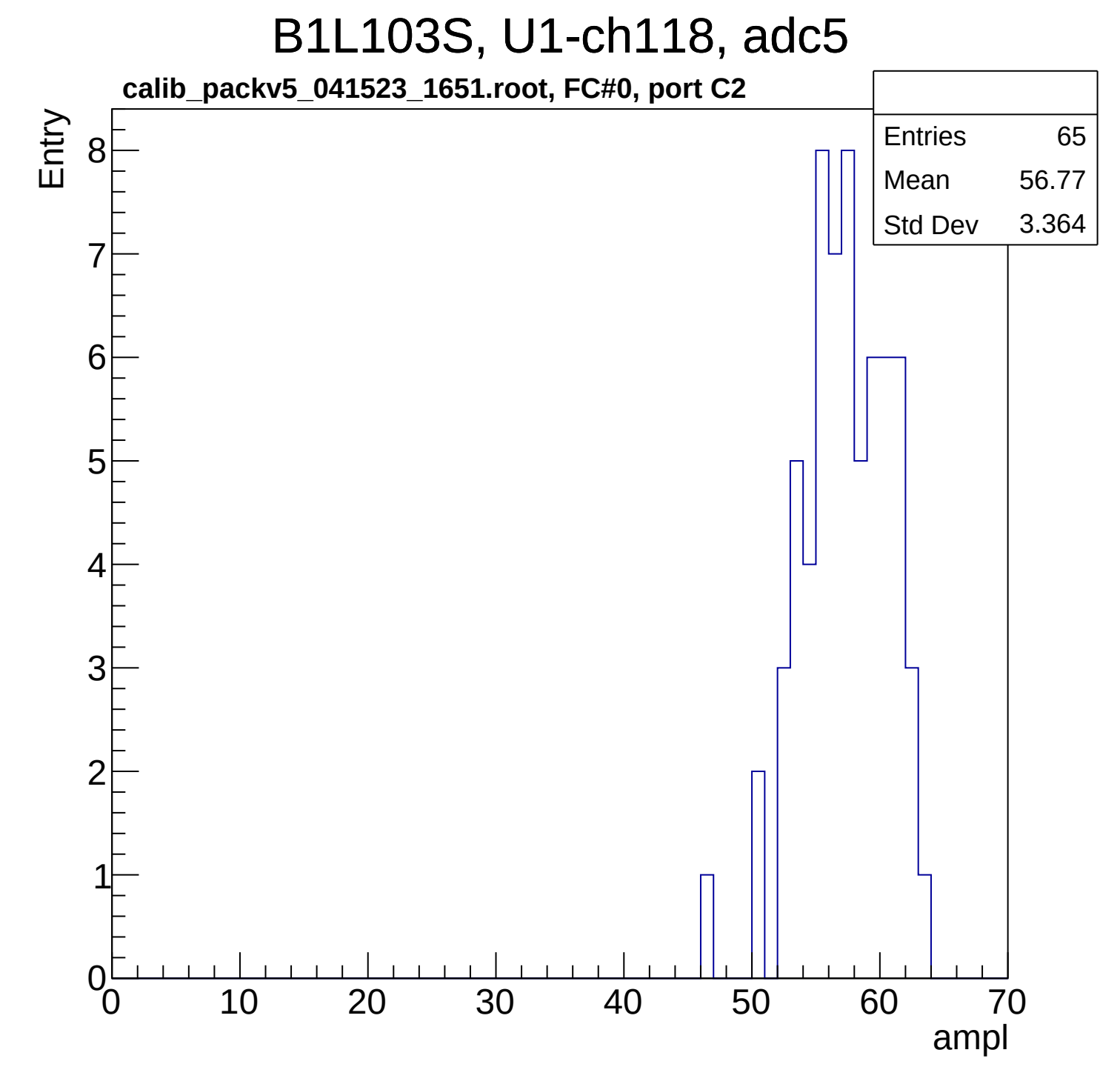
B1L103S, U1-ch118, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 56.77
Std Dev 3.364
Entry
ampl
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4
5
6
7
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0
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60
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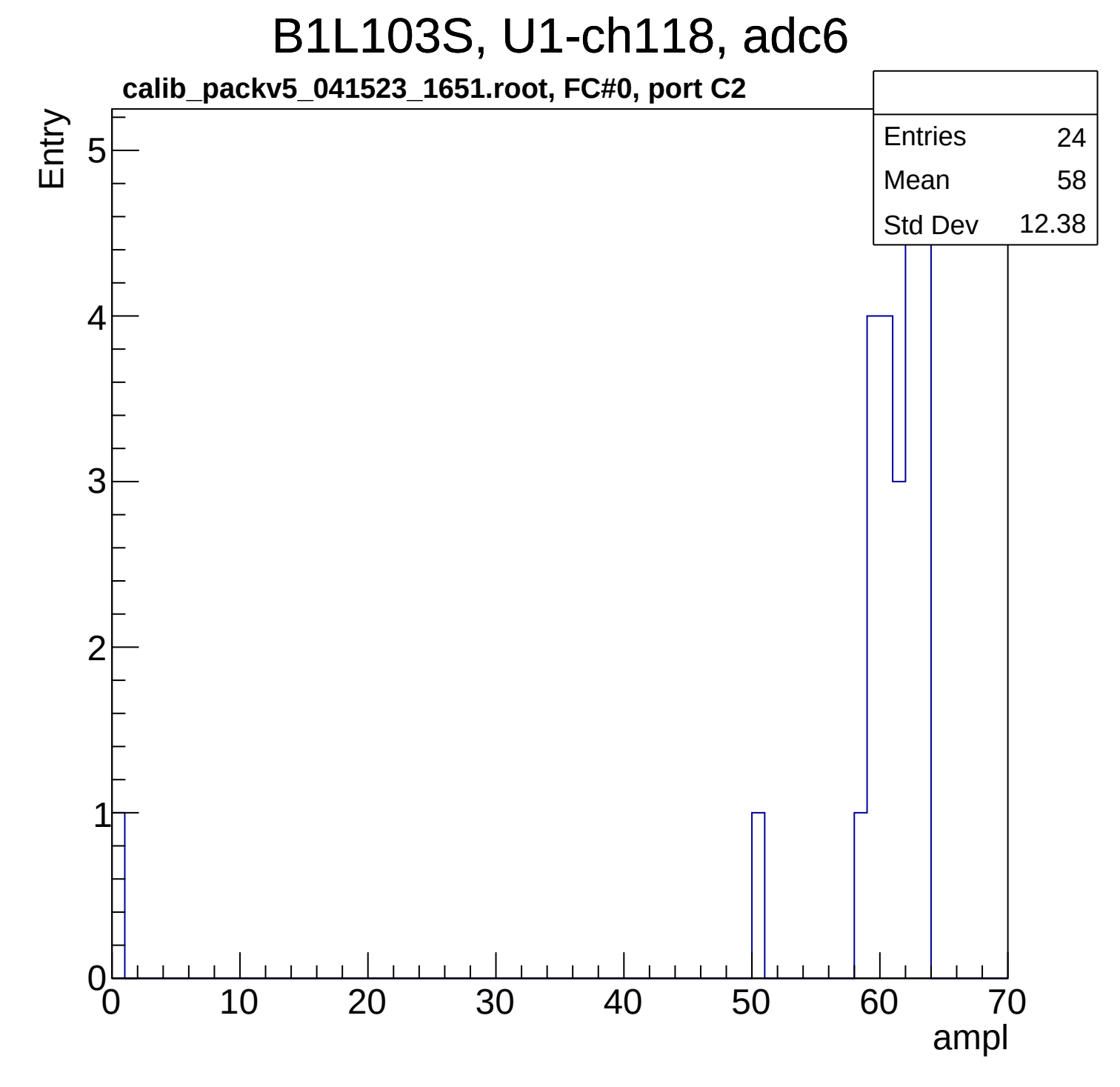
B1L103S, U1-ch118, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 24
Mean 58
Std Dev 12.38
Entry
ampl
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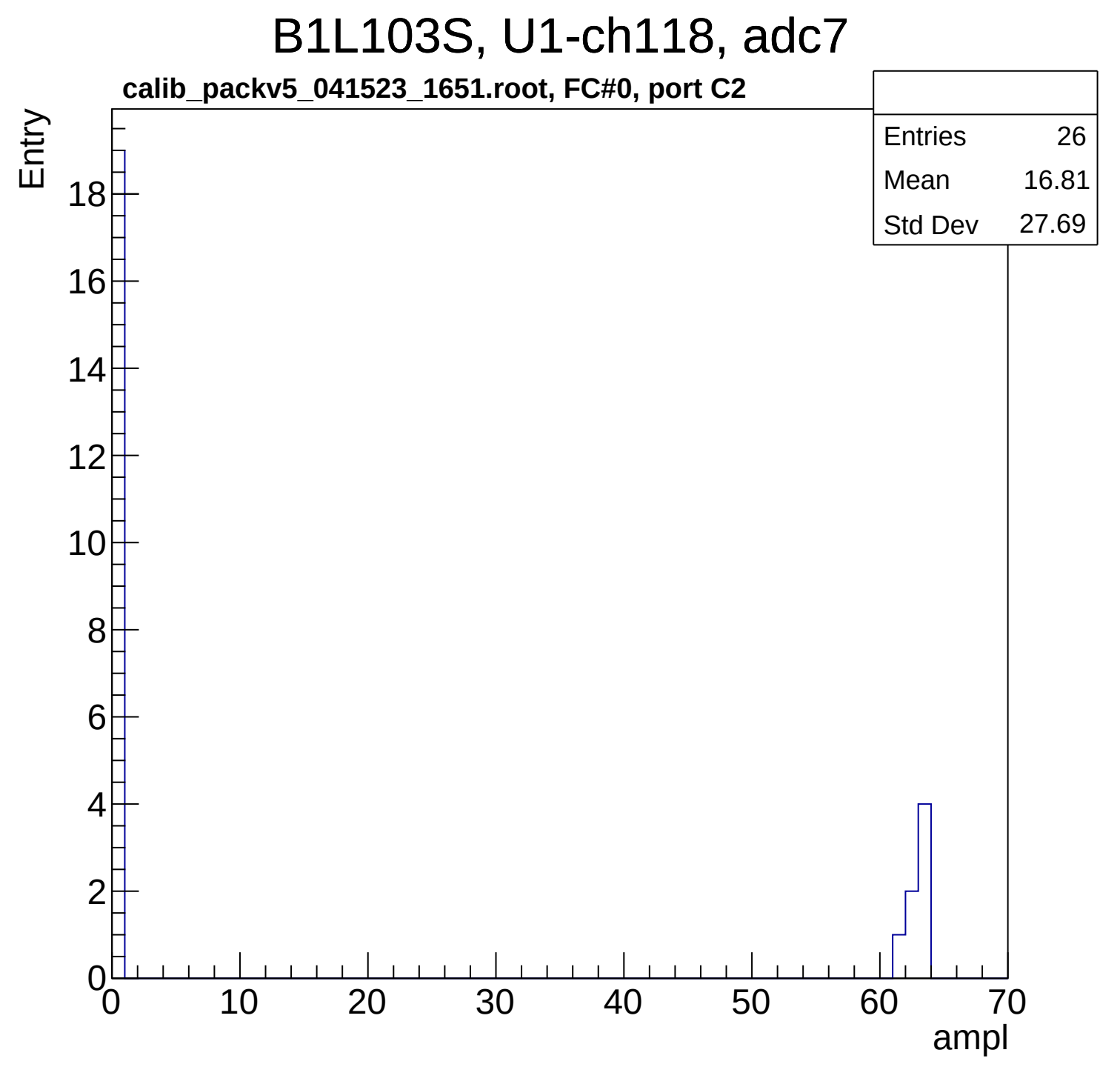
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U1-ch118, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 26
Mean 16.81
Std Dev 27.69
Entry
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10
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14
16
18
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10
20
30
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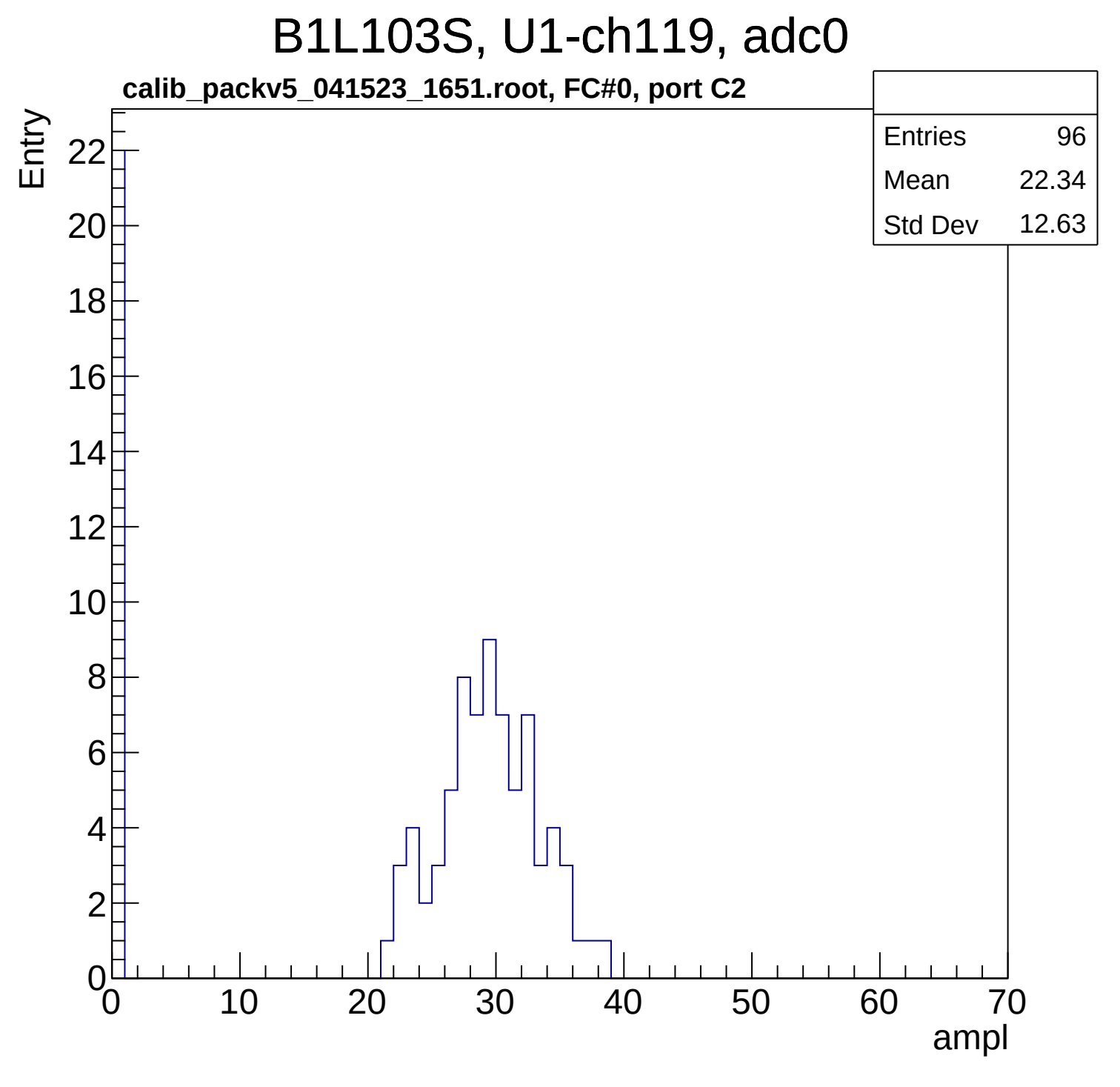
50
60
70
ampl


B1L103S, U1-ch119, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 96
Mean 22.34
Std Dev 12.63
Entry
ampl
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8
10
12
14
16
18
20
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0
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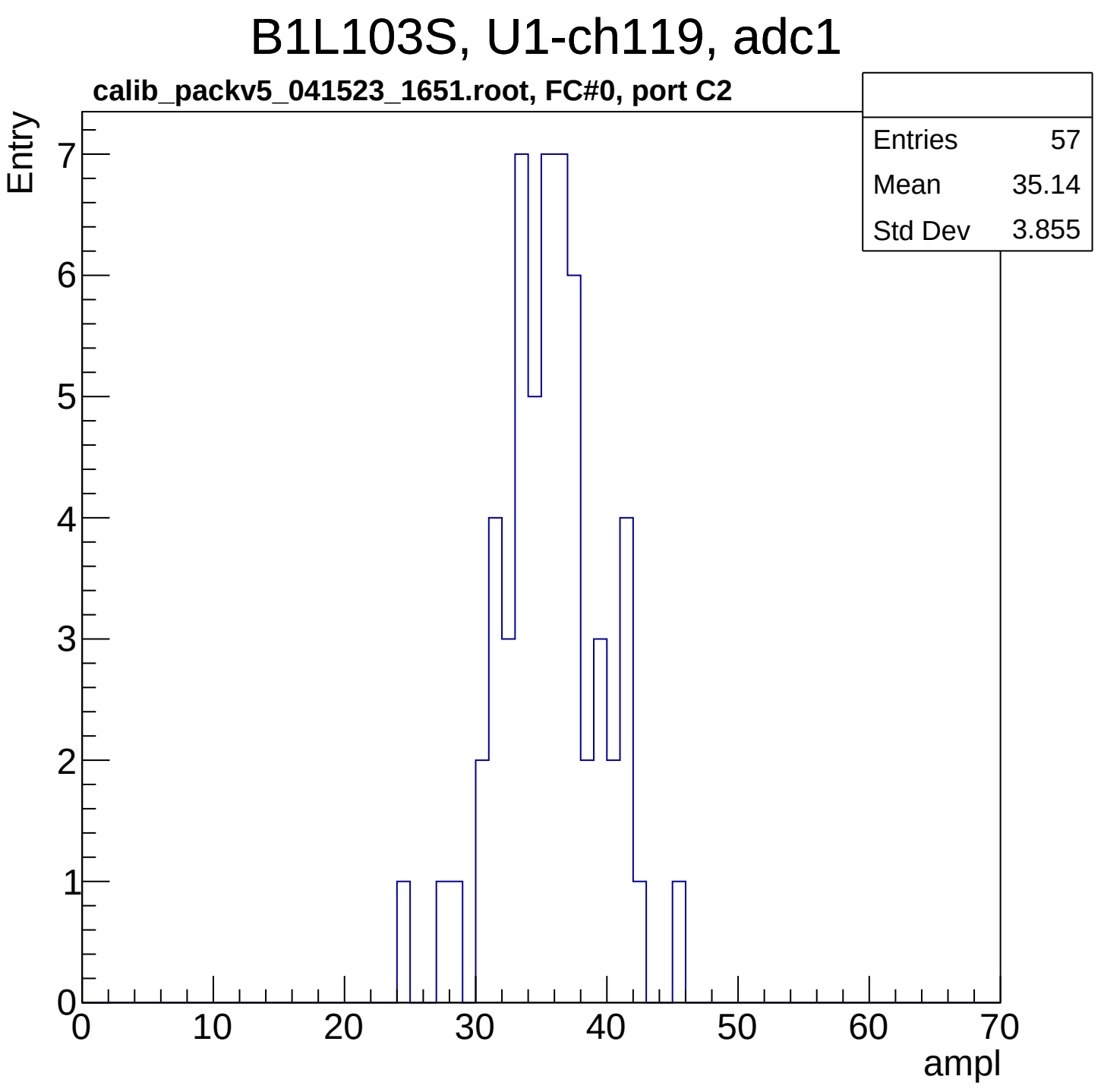
B1L103S, U1-ch119, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 35.14
Std Dev 3.855
Entry
ampl
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4
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0
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60
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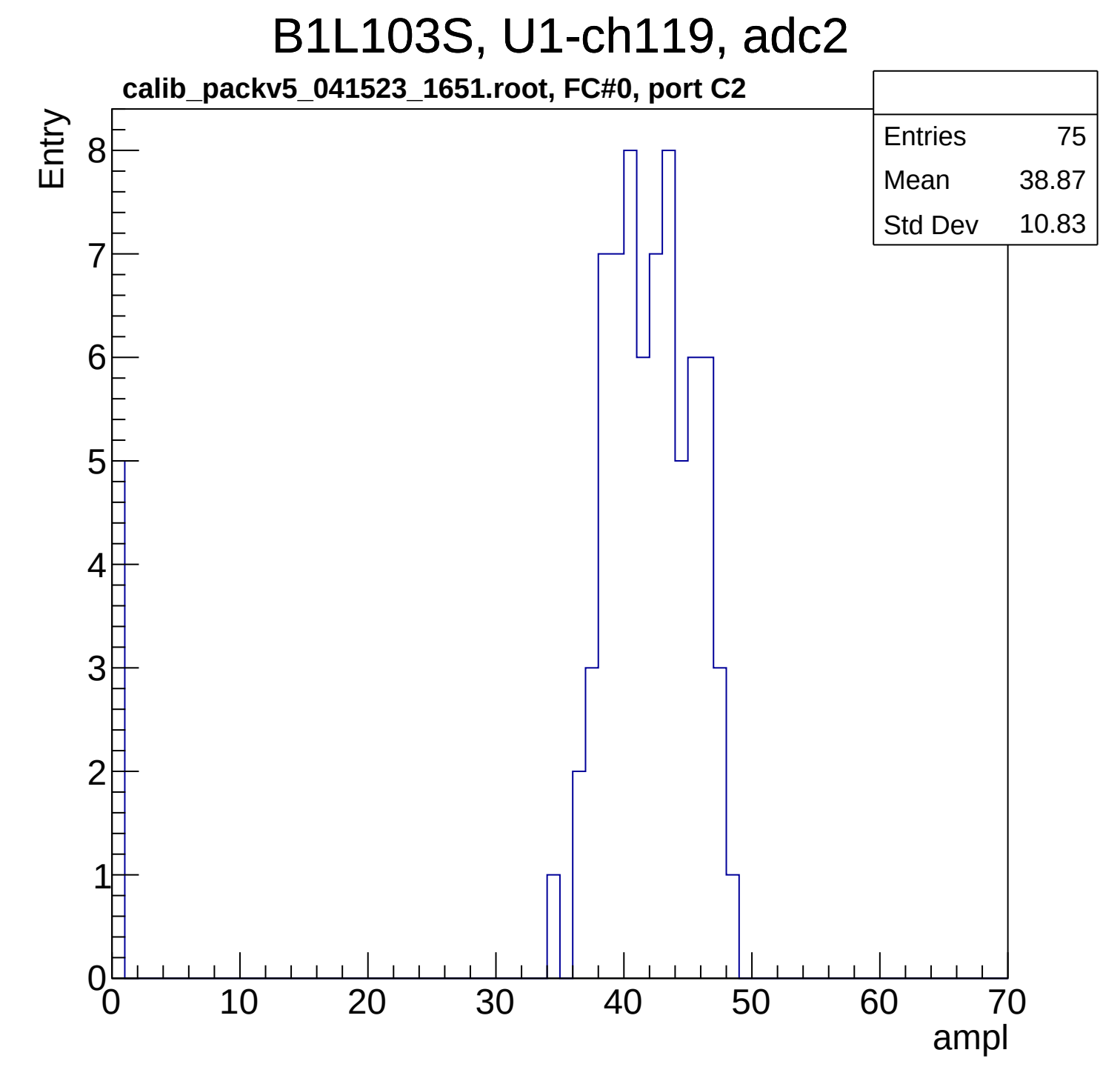
B1L103S, U1-ch119, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 38.87
Std Dev 10.83
Entry
ampl
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3
4
5
6
7
8
0
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20
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40
50
60
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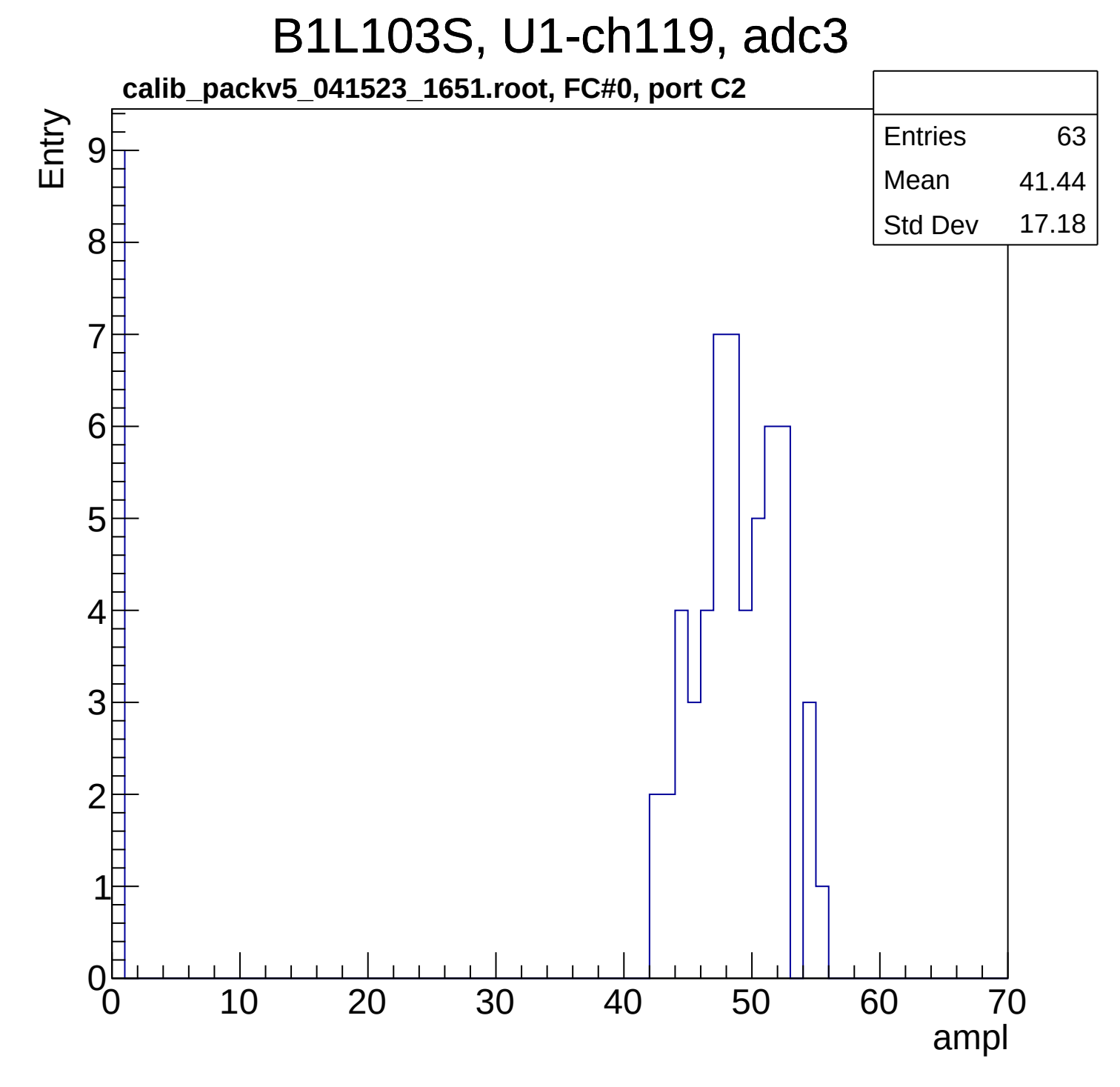
B1L103S, U1-ch119, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 41.44
Std Dev 17.18
Entry
ampl
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3
4
5
6
7
8
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0
10
20
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40
50
60
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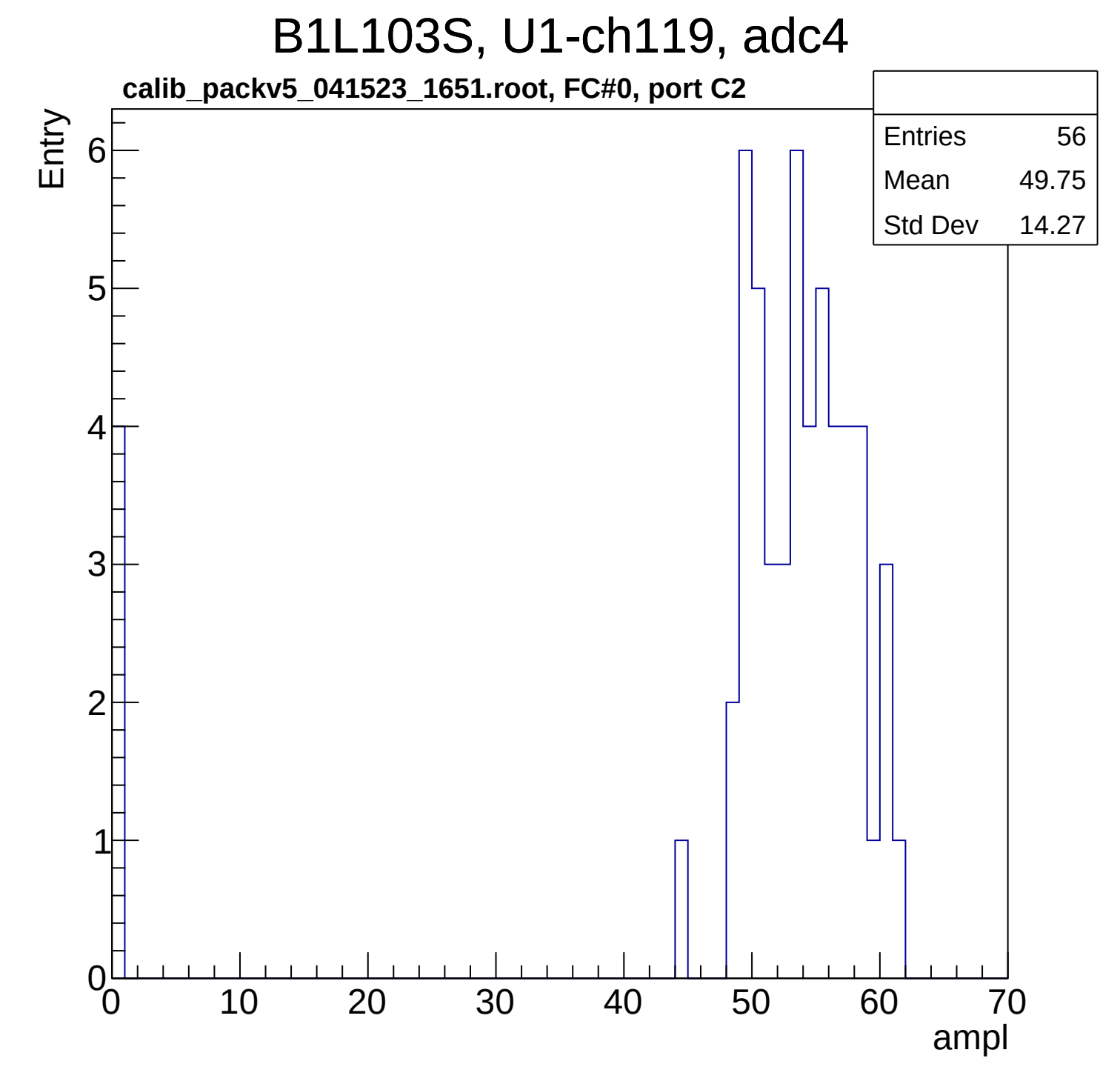
B1L103S, U1-ch119, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 49.75
Std Dev 14.27
Entry
ampl
0
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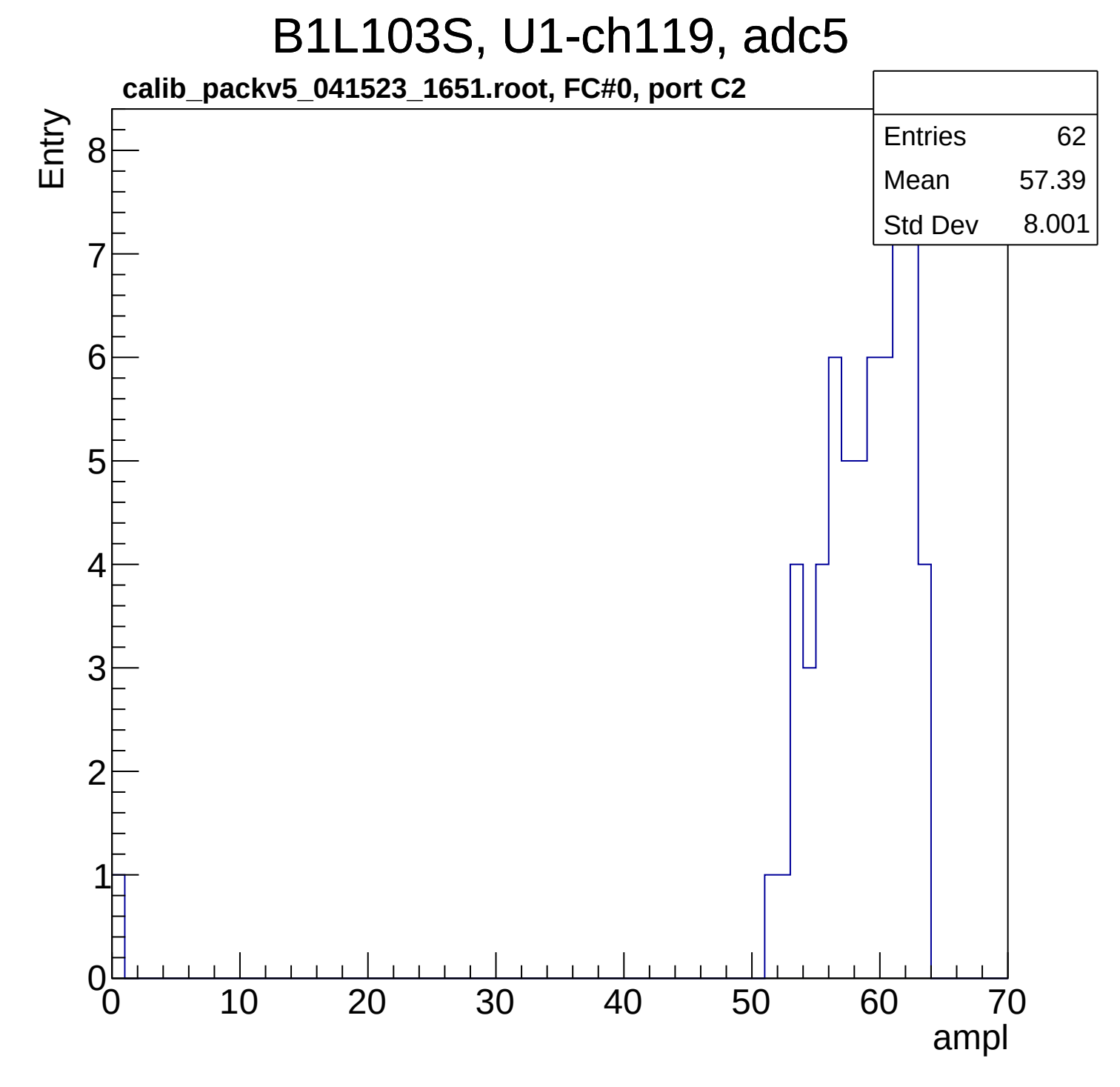
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U1-ch119, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 57.39
Std Dev 8.001
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
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40
50
60
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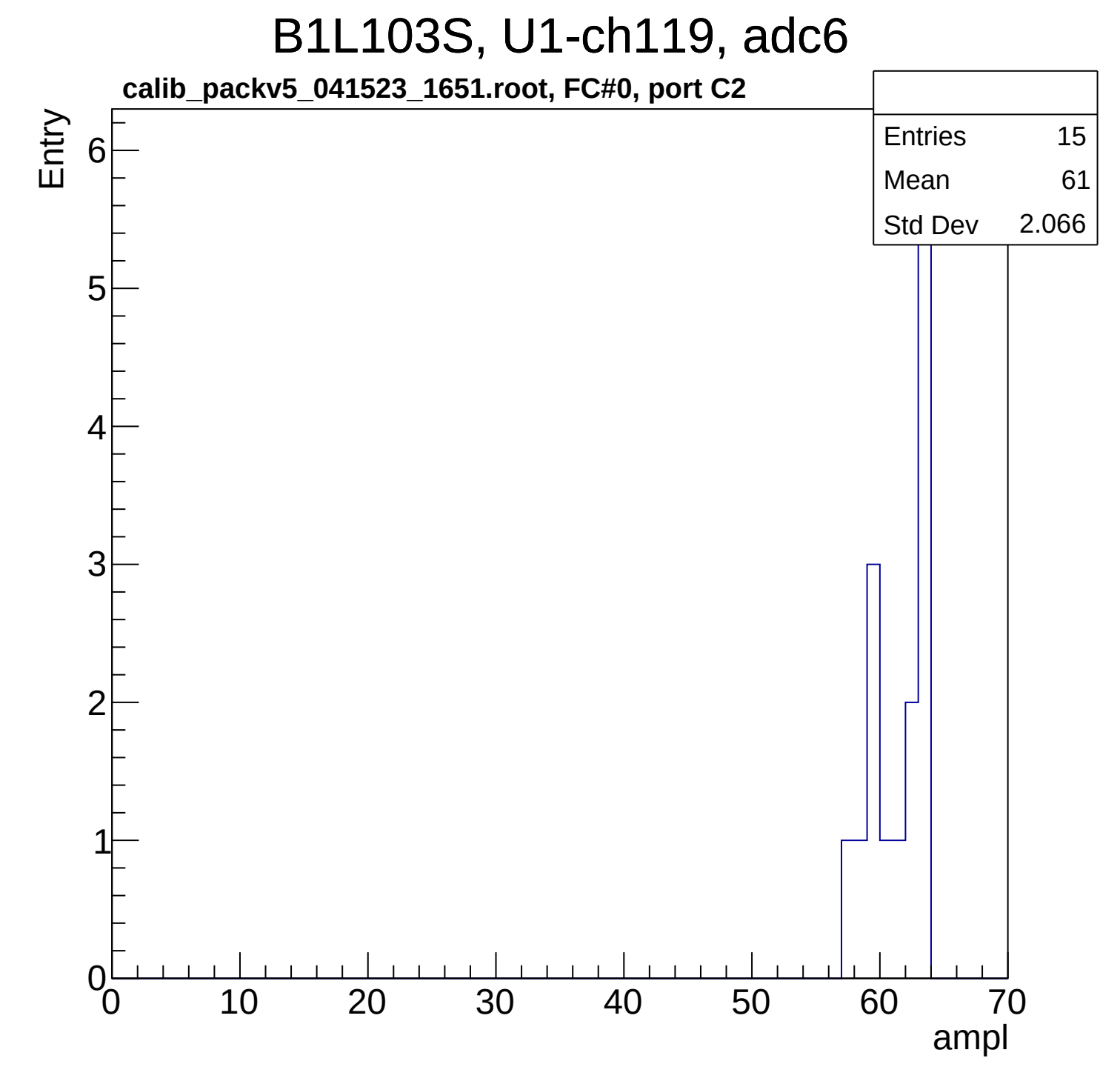
B1L103S, U1-ch119, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 15
Mean 61
Std Dev 2.066
Entry
ampl
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4
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0
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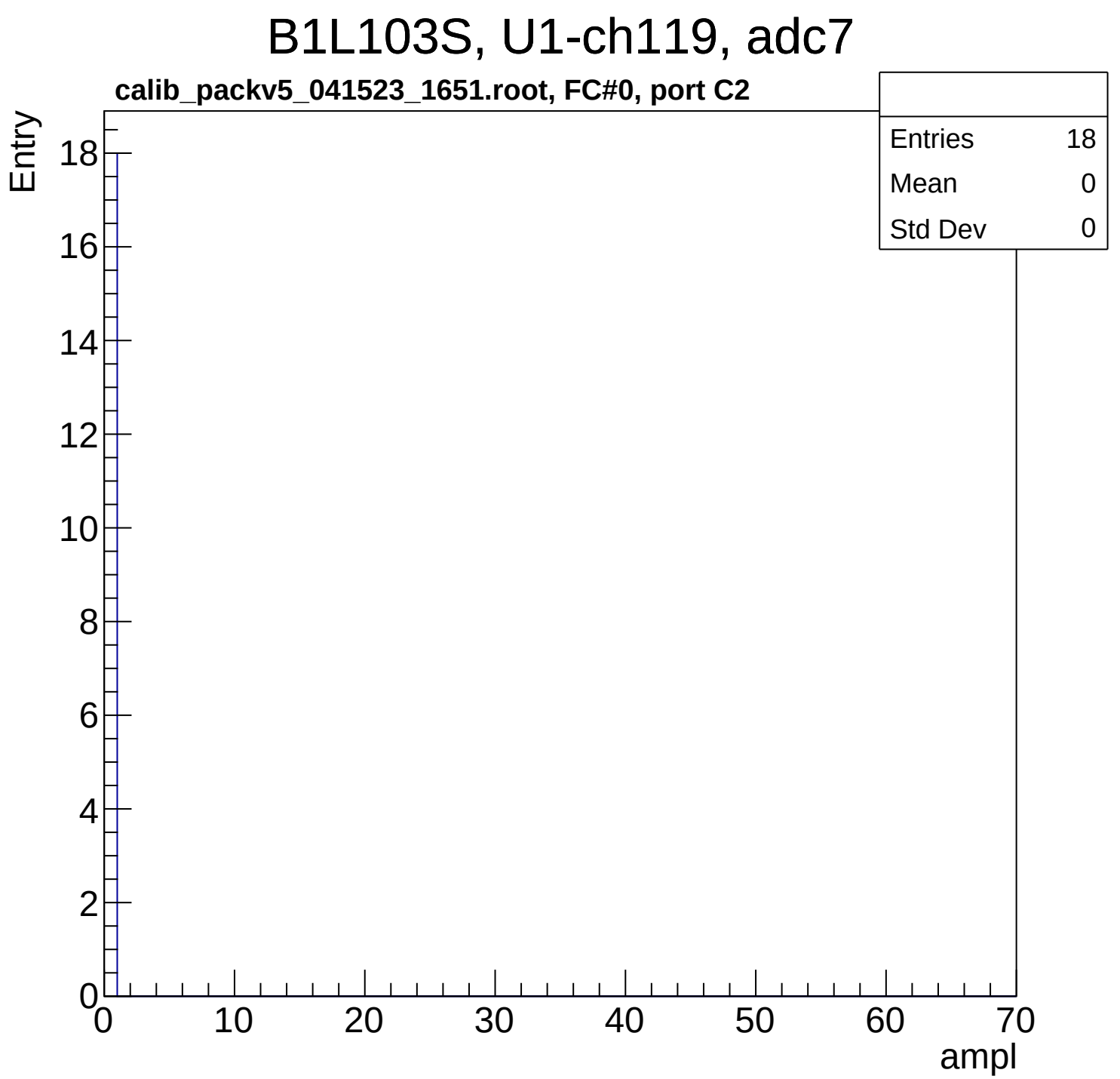
40
50
60
70


B1L103S, U1-ch119, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
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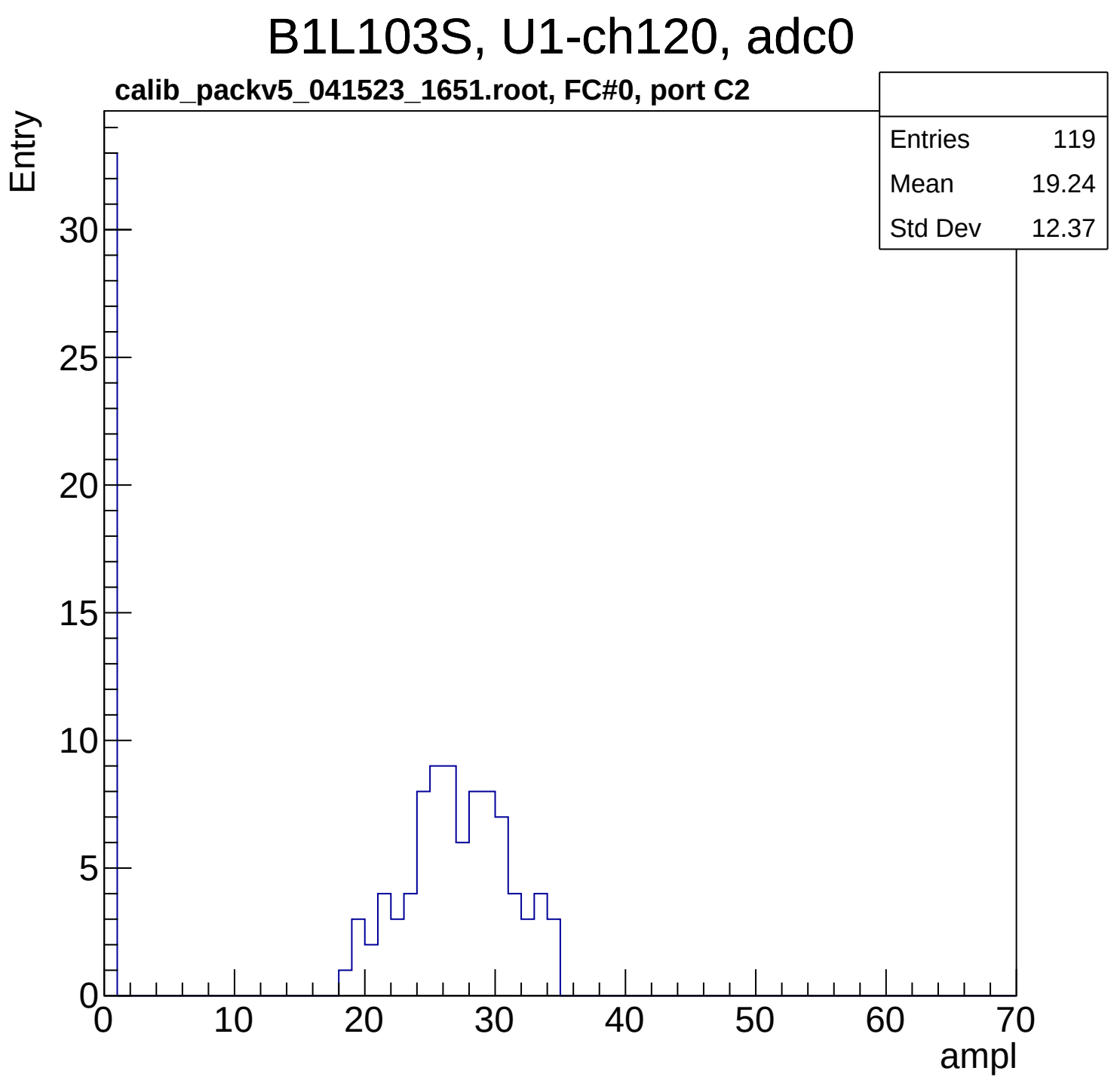
40
50
60
70
ampl


B1L103S, U1-ch120, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 119
Mean 19.24
Std Dev 12.37
Entry
0
5
10
15
20
25
30
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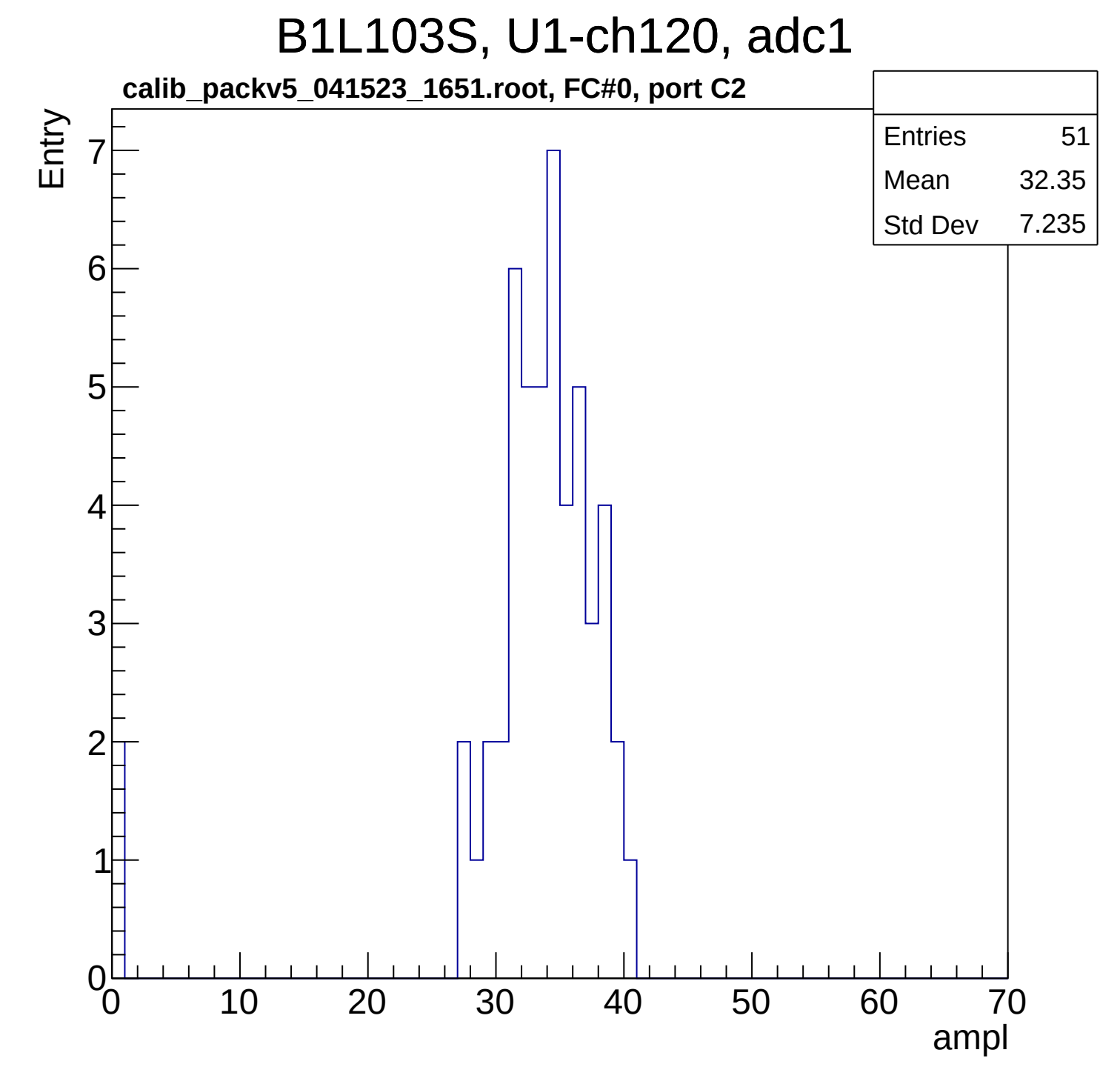
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch120, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 32.35
Std Dev 7.235
Entry
ampl
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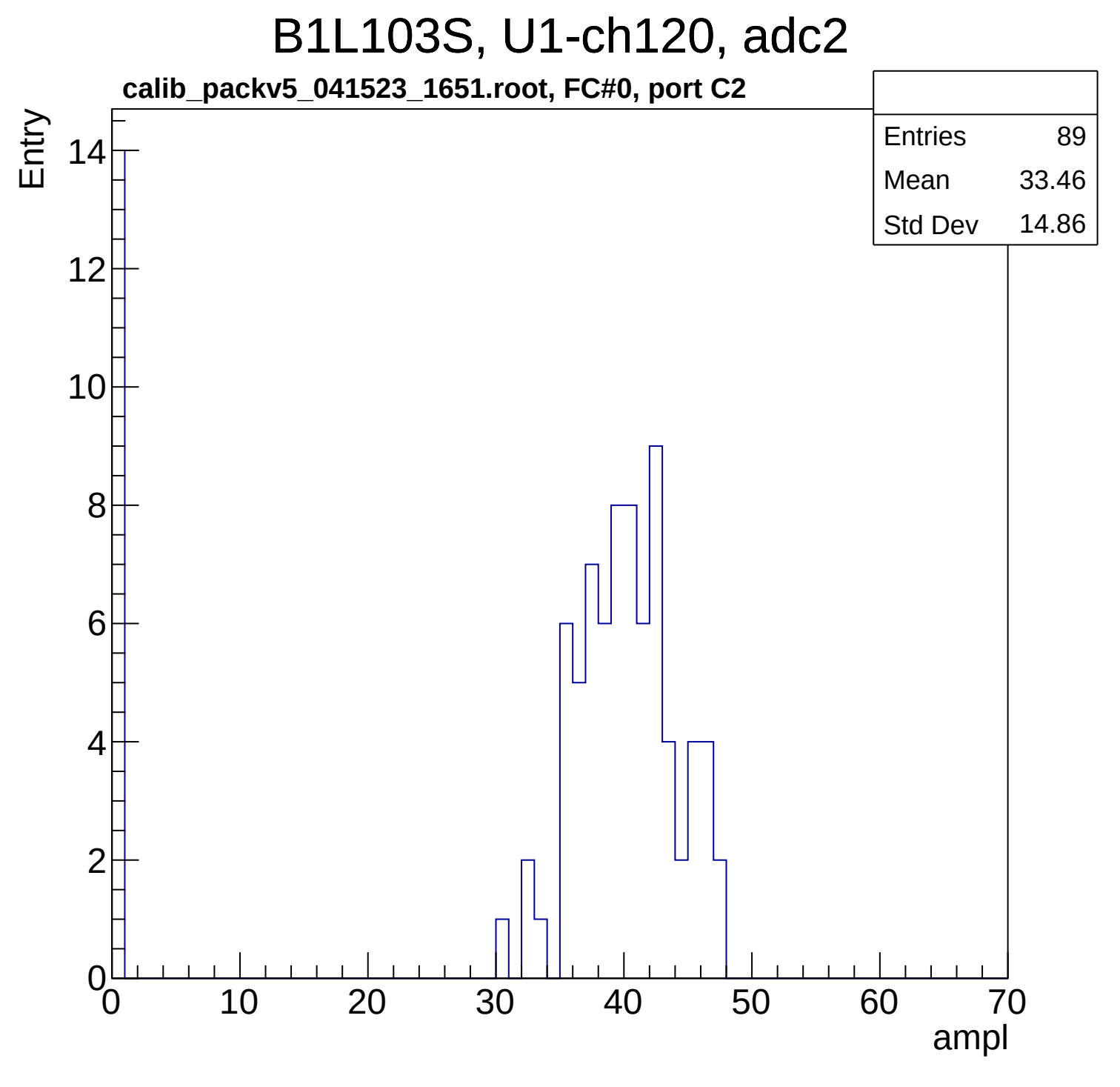
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U1-ch120, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 89
Mean 33.46
Std Dev 14.86
Entry
ampl
0
2
4
6
8
10
12
14
0
10
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40
50
60
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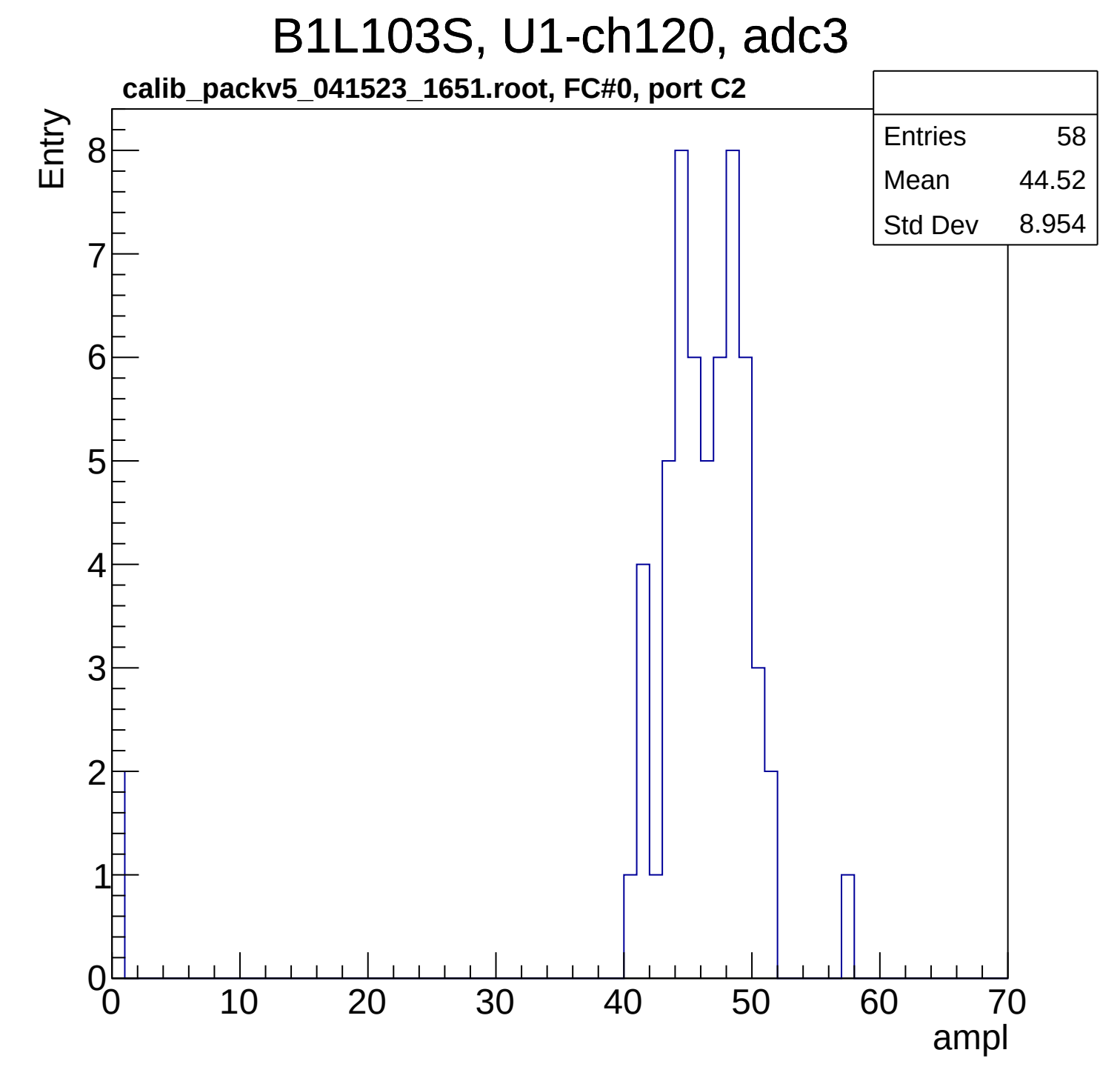
B1L103S, U1-ch120, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 44.52
Std Dev 8.954
Entry
ampl
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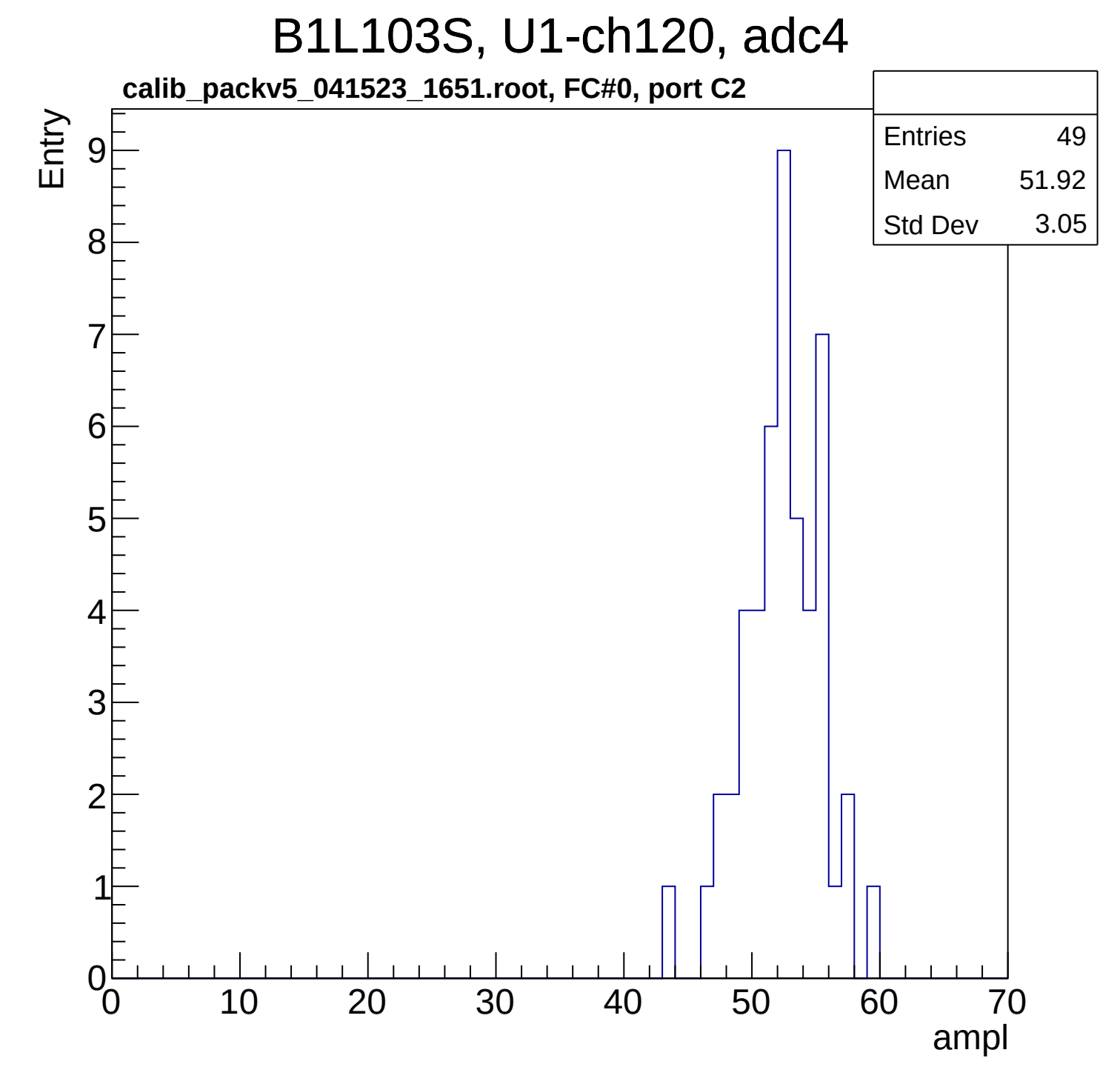
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U1-ch120, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 51.92
Std Dev 3.05
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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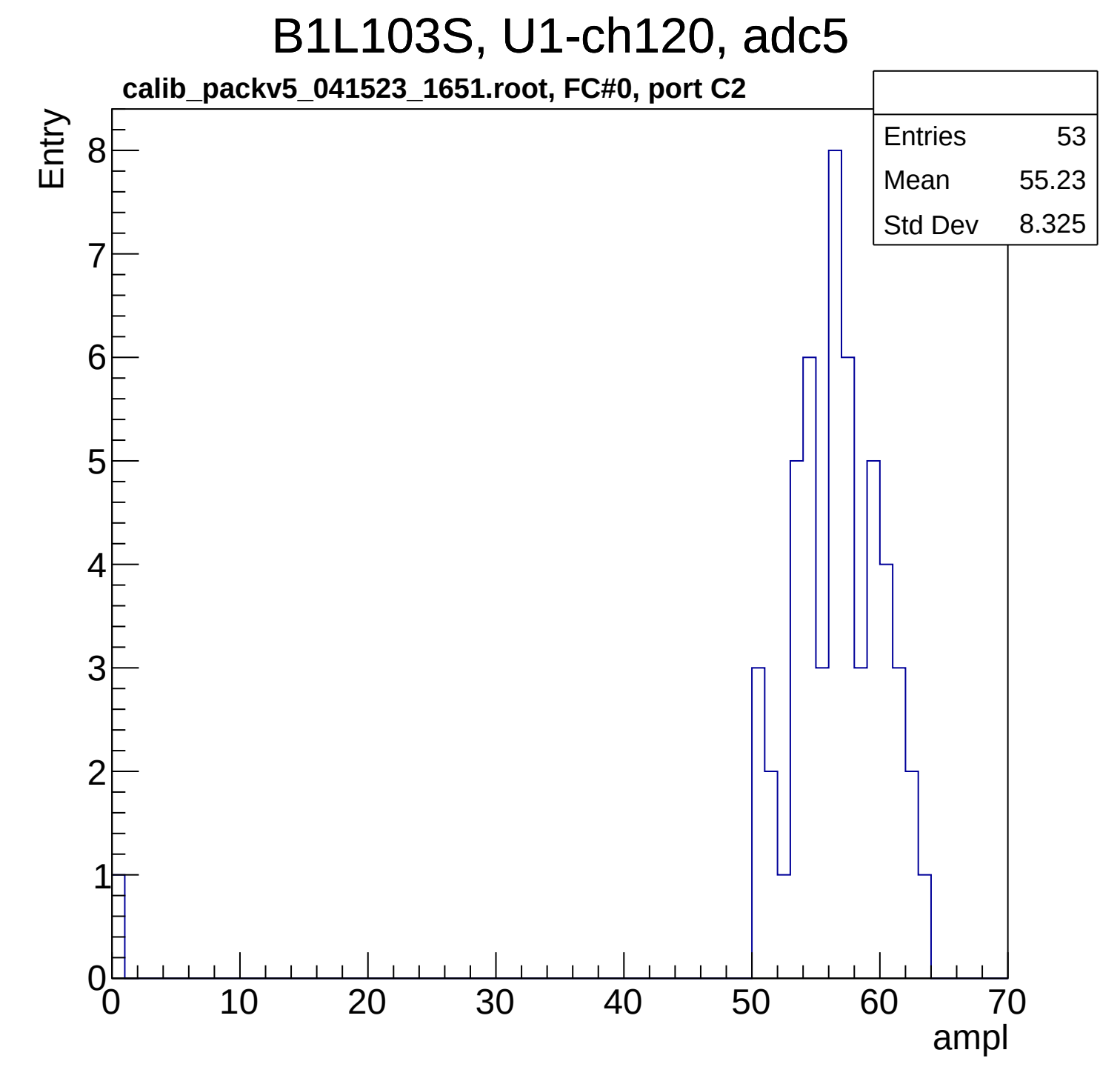
B1L103S, U1-ch120, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 55.23
Std Dev 8.325
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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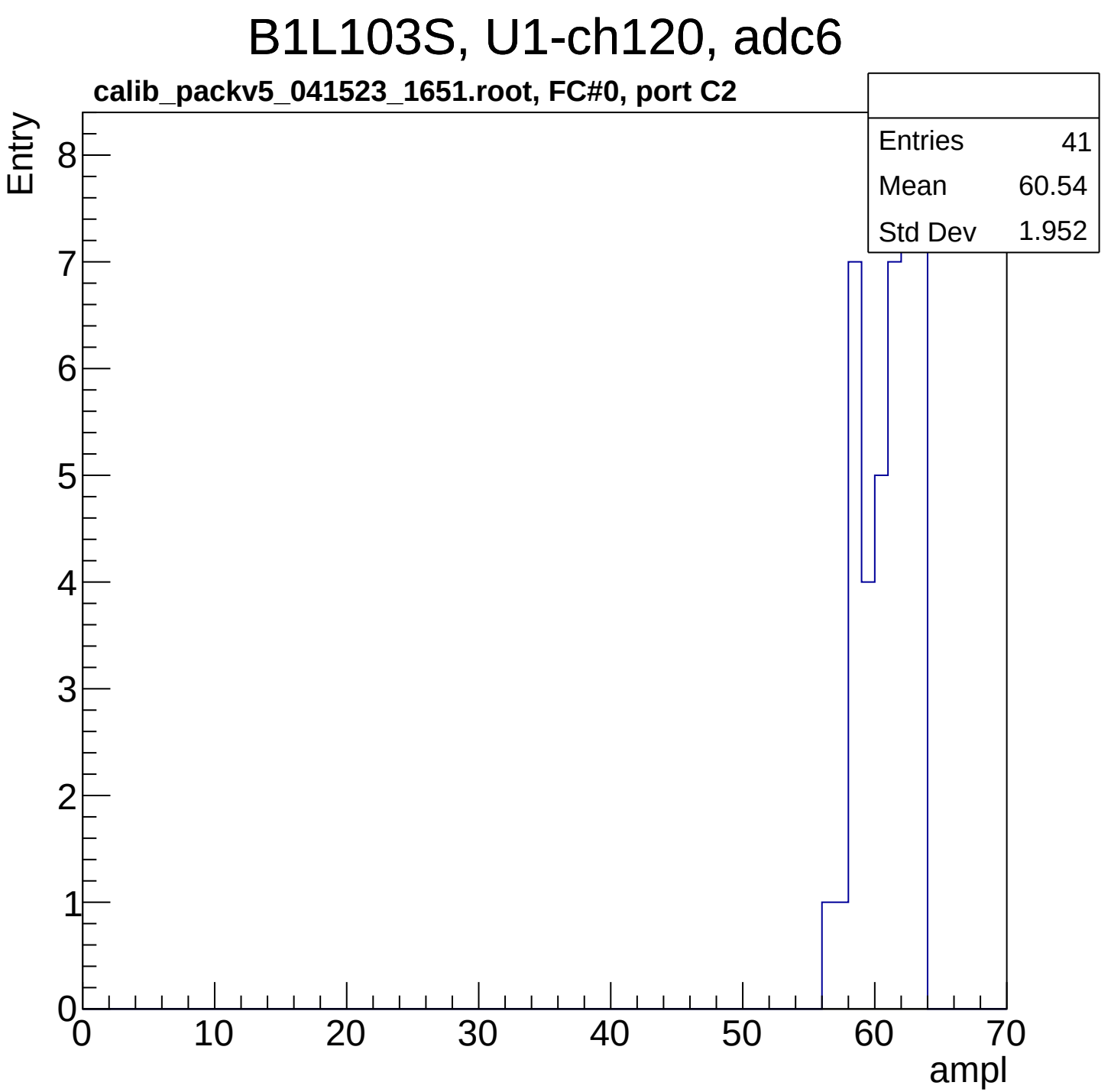
40
50
60
70


B1L103S, U1-ch120, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 41
Mean 60.54
Std Dev 1.952
Entry
ampl
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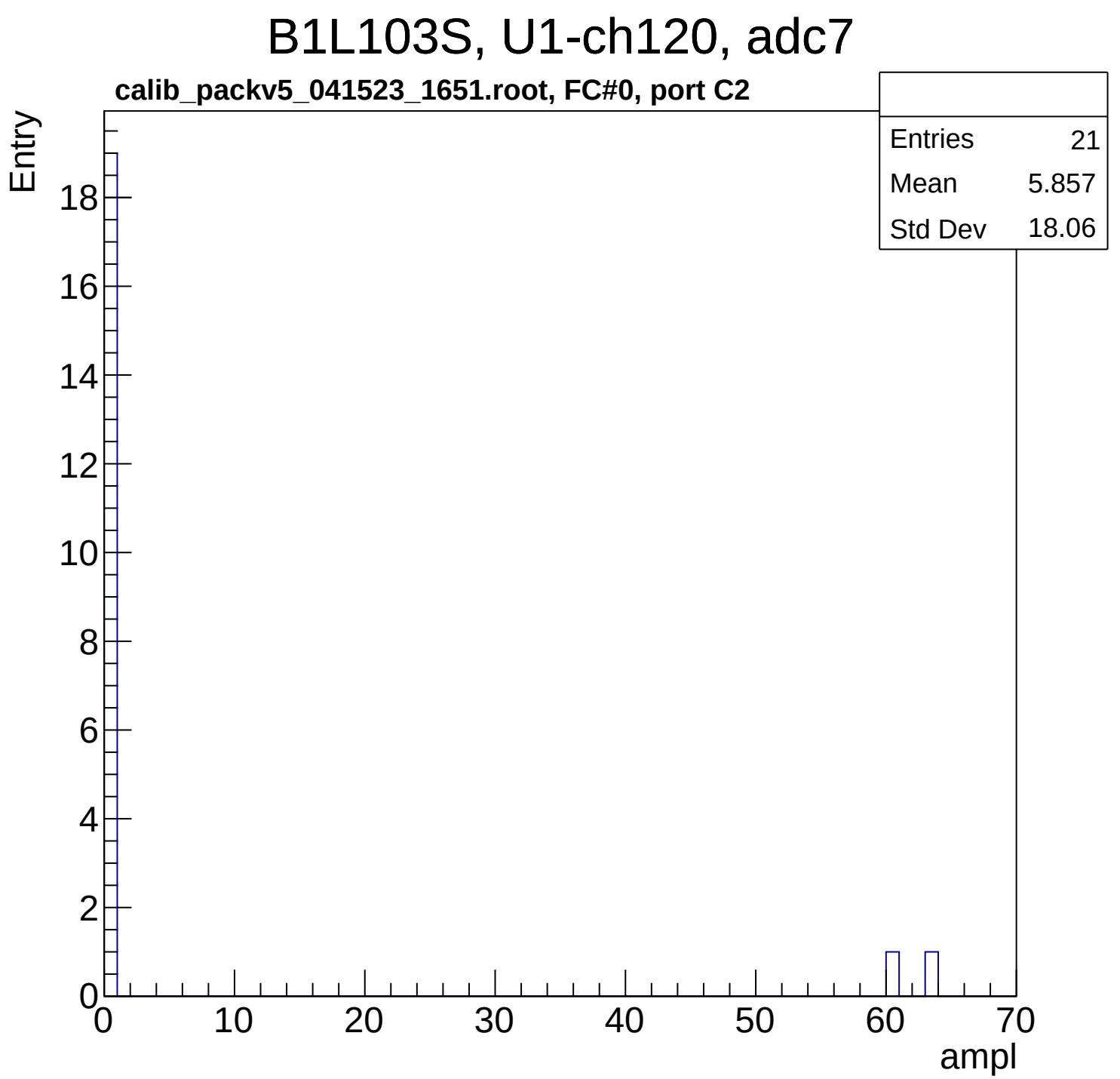
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U1-ch120, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 5.857
Std Dev 18.06
Entry
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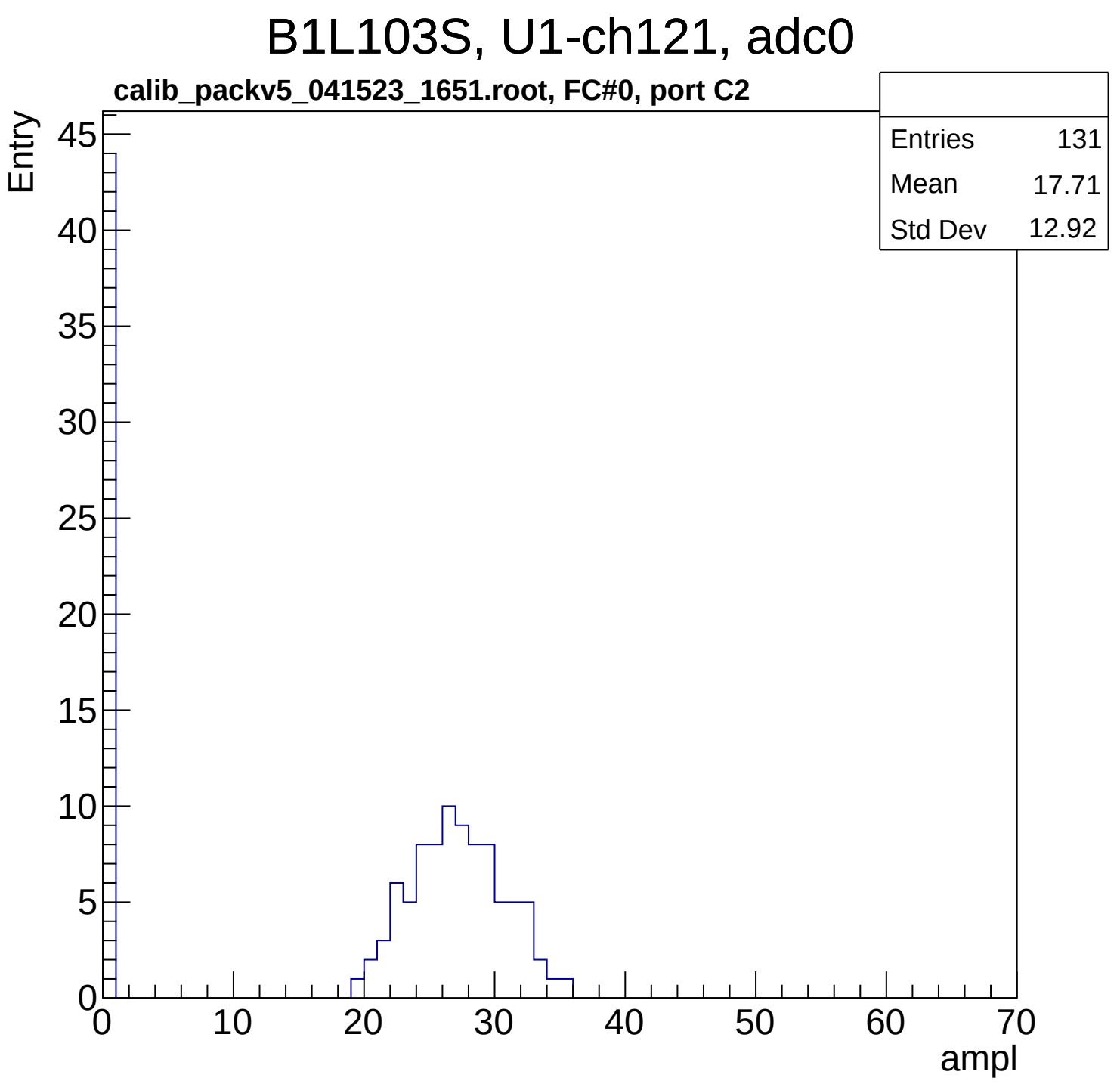
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch121, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 131
Mean 17.71
Std Dev 12.92
Entry
ampl
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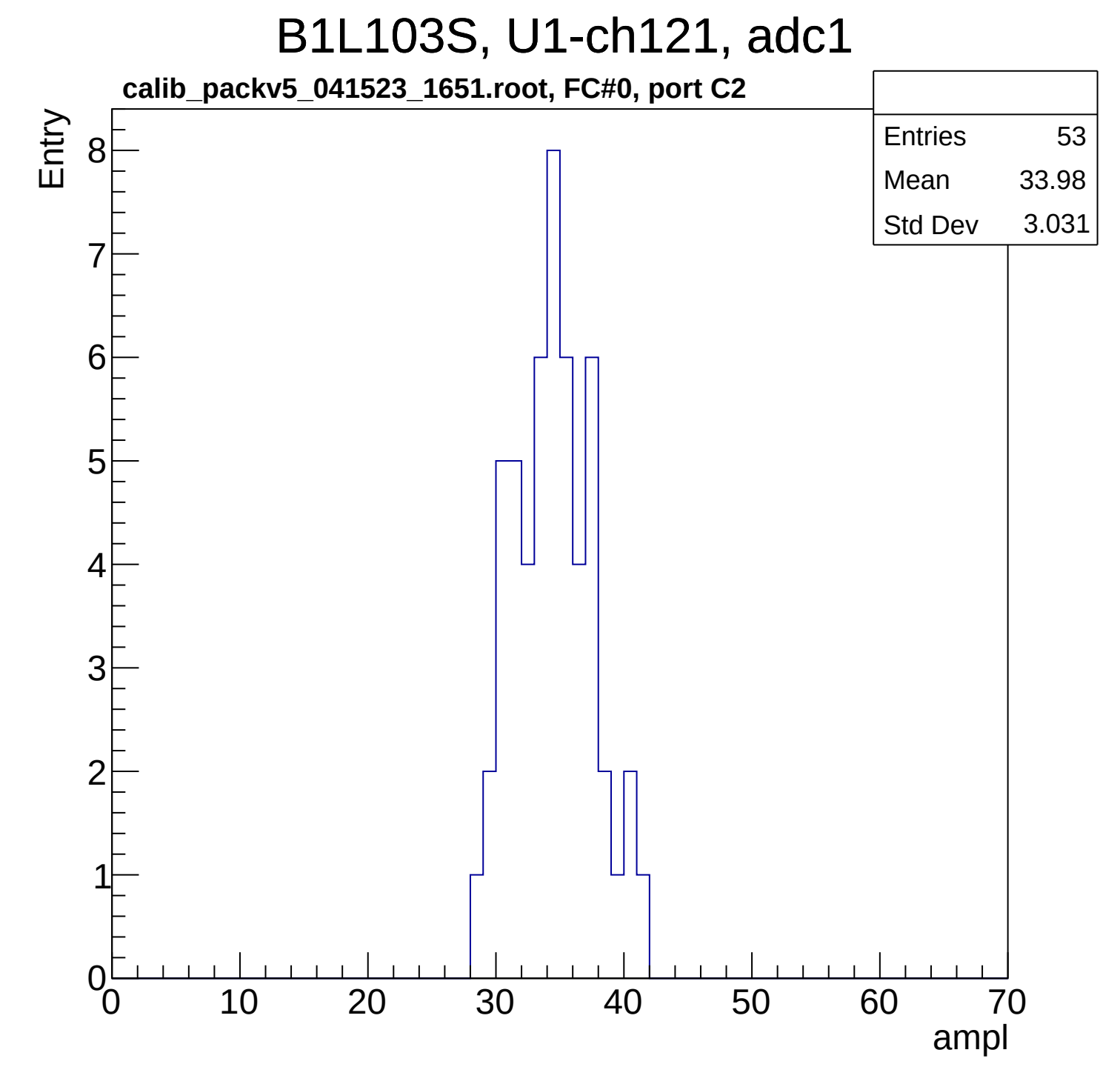
5
10
15
20
25
30
35
40
45
0
10
20
30
40
50
60
70


B1L103S, U1-ch121, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 33.98
Std Dev 3.031
Entry
ampl
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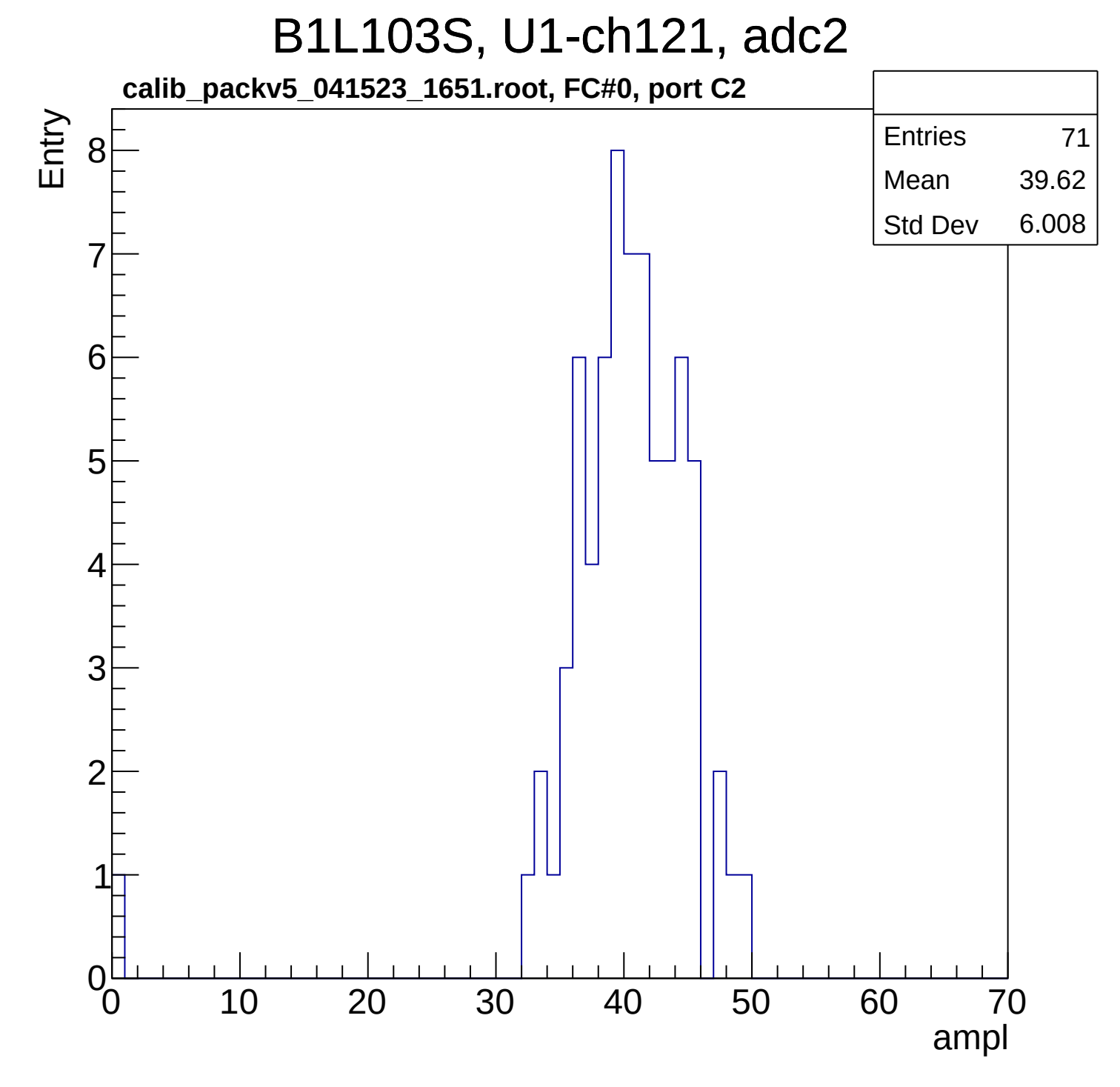
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U1-ch121, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 39.62
Std Dev 6.008
Entry
ampl
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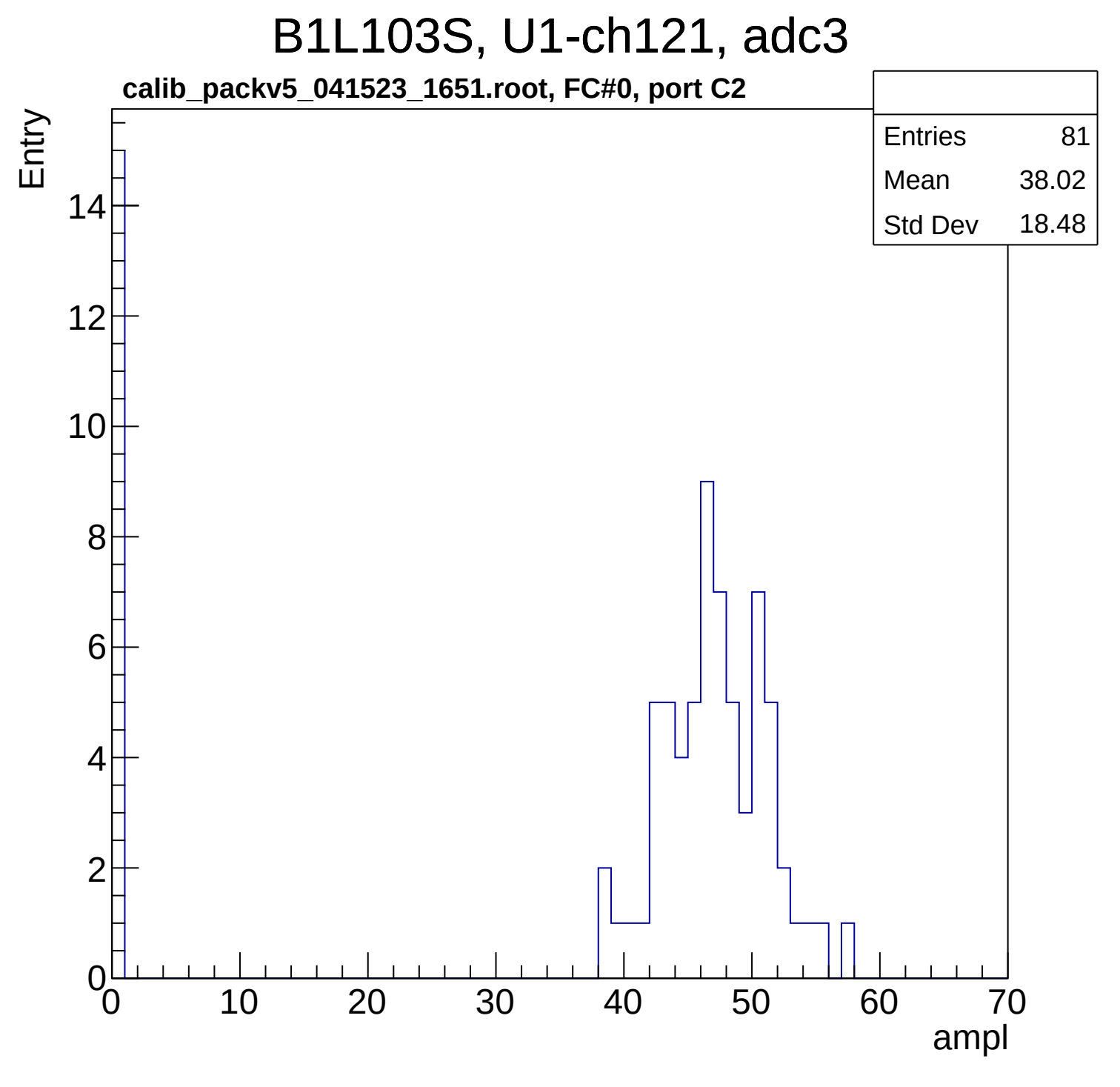
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U1-ch121, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 38.02
Std Dev 18.48
Entry
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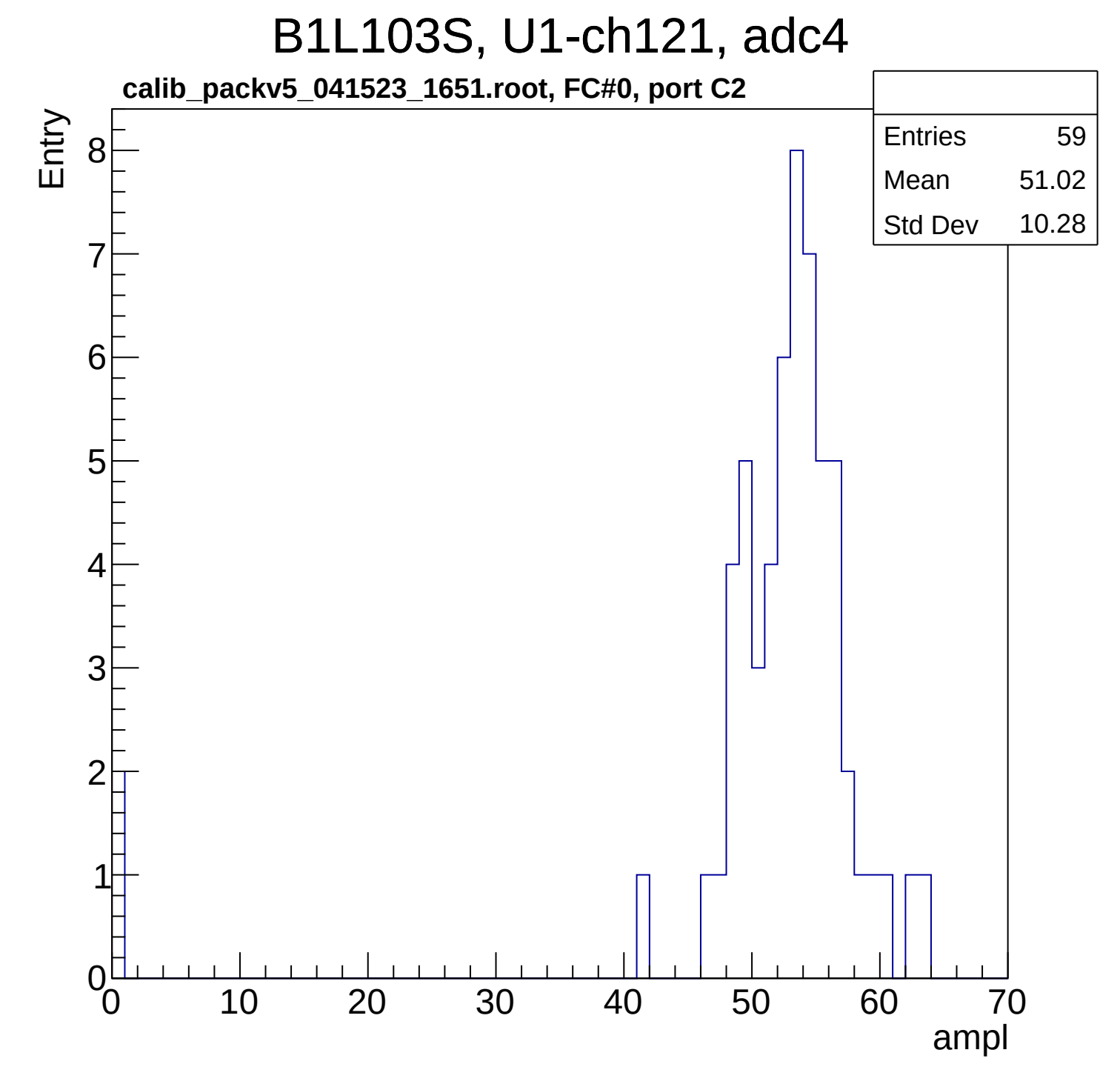
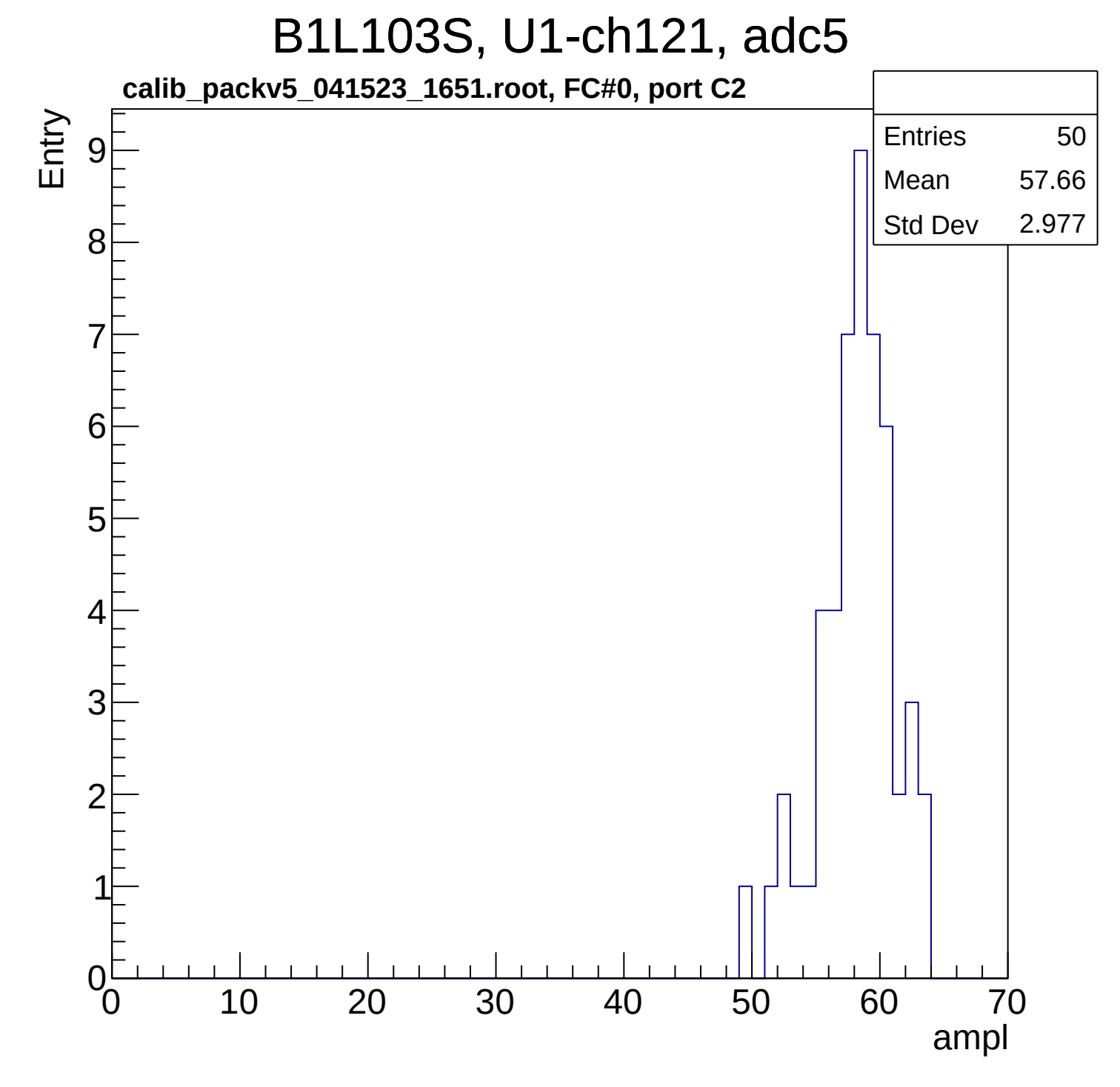
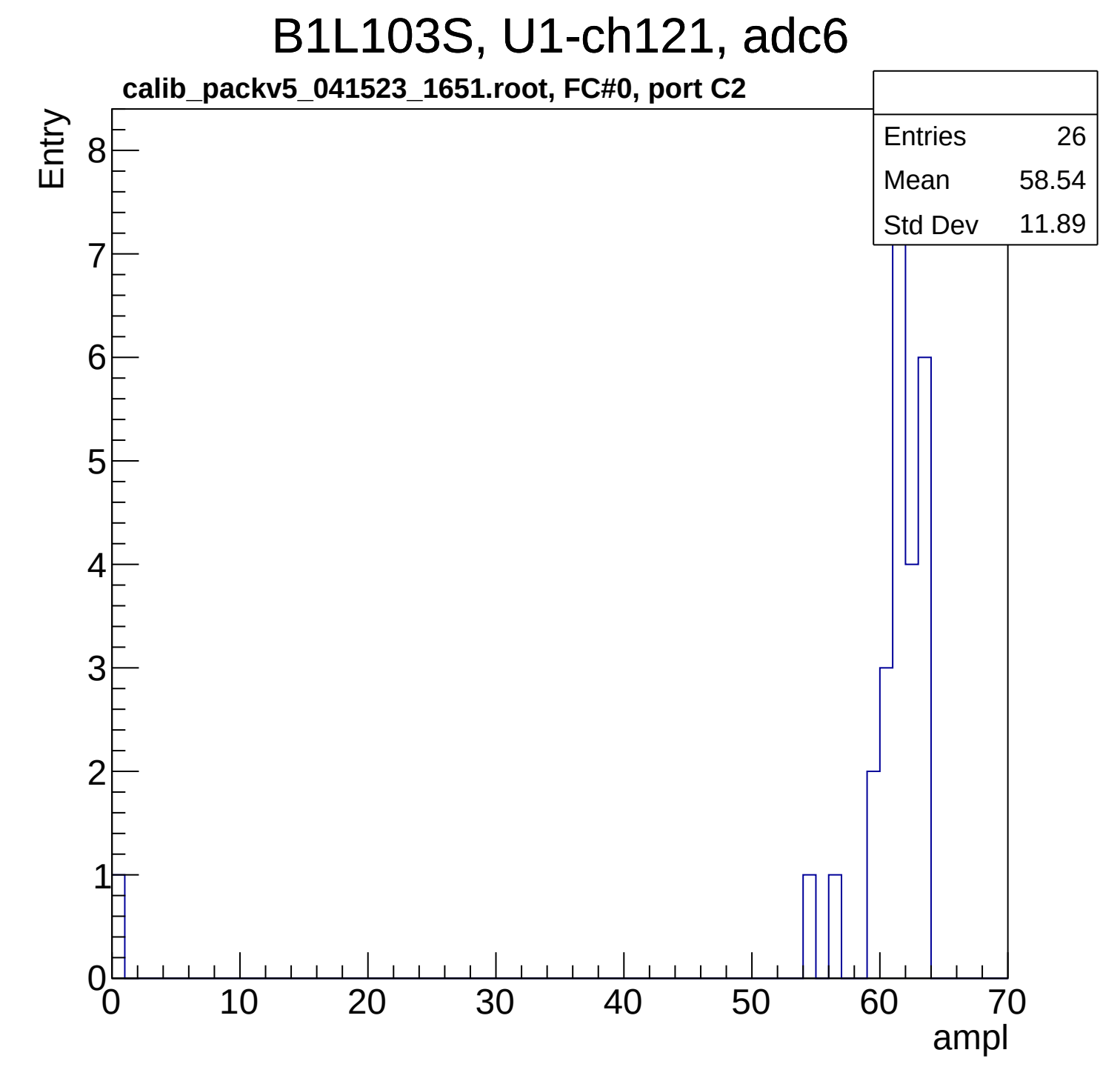
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch121, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 51.02
Std Dev 10.28
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U1-ch121, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 57.66
Std Dev 2.977
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U1-ch121, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 26
Mean 58.54
Std Dev 11.89
Entry
ampl
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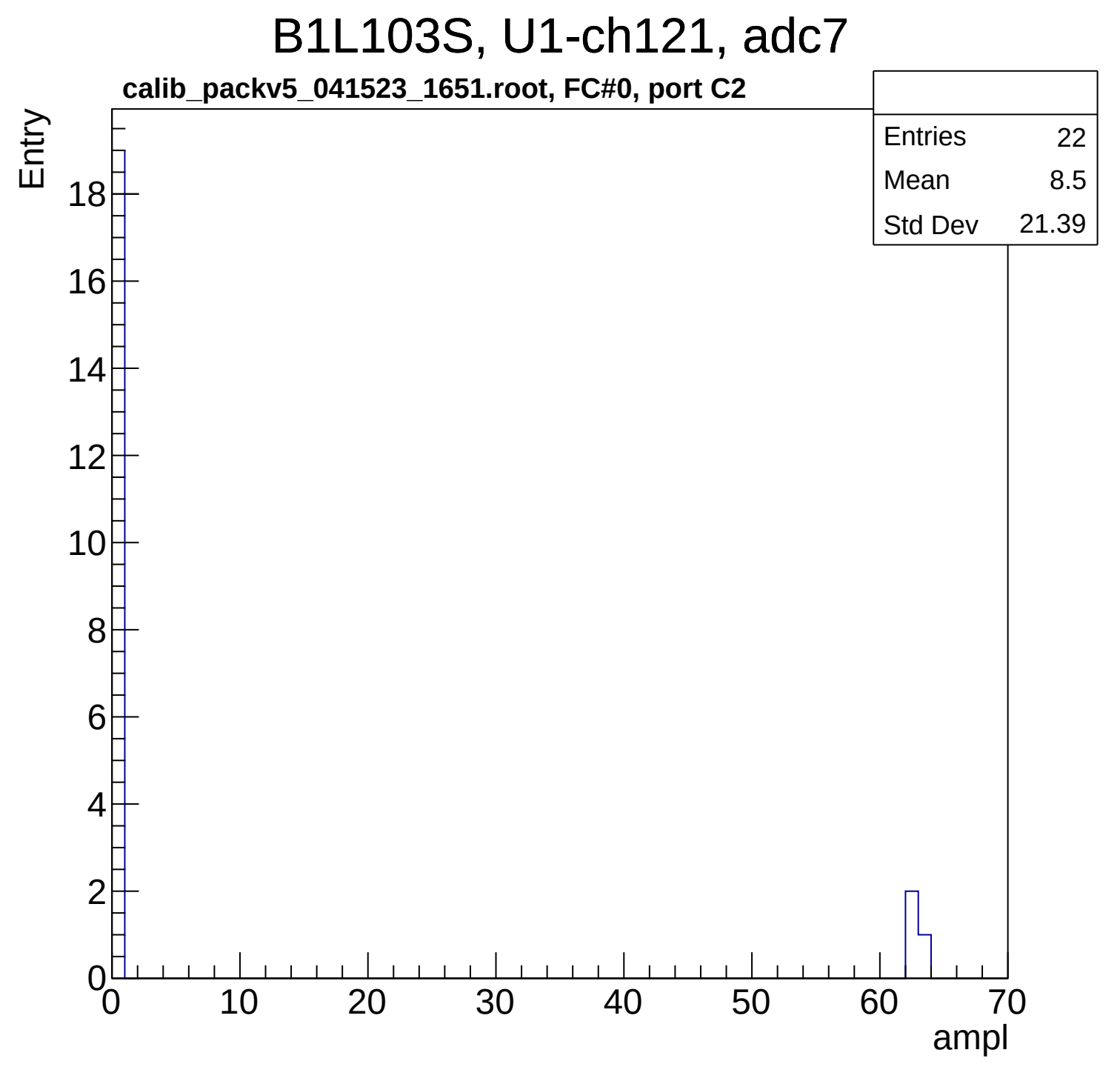
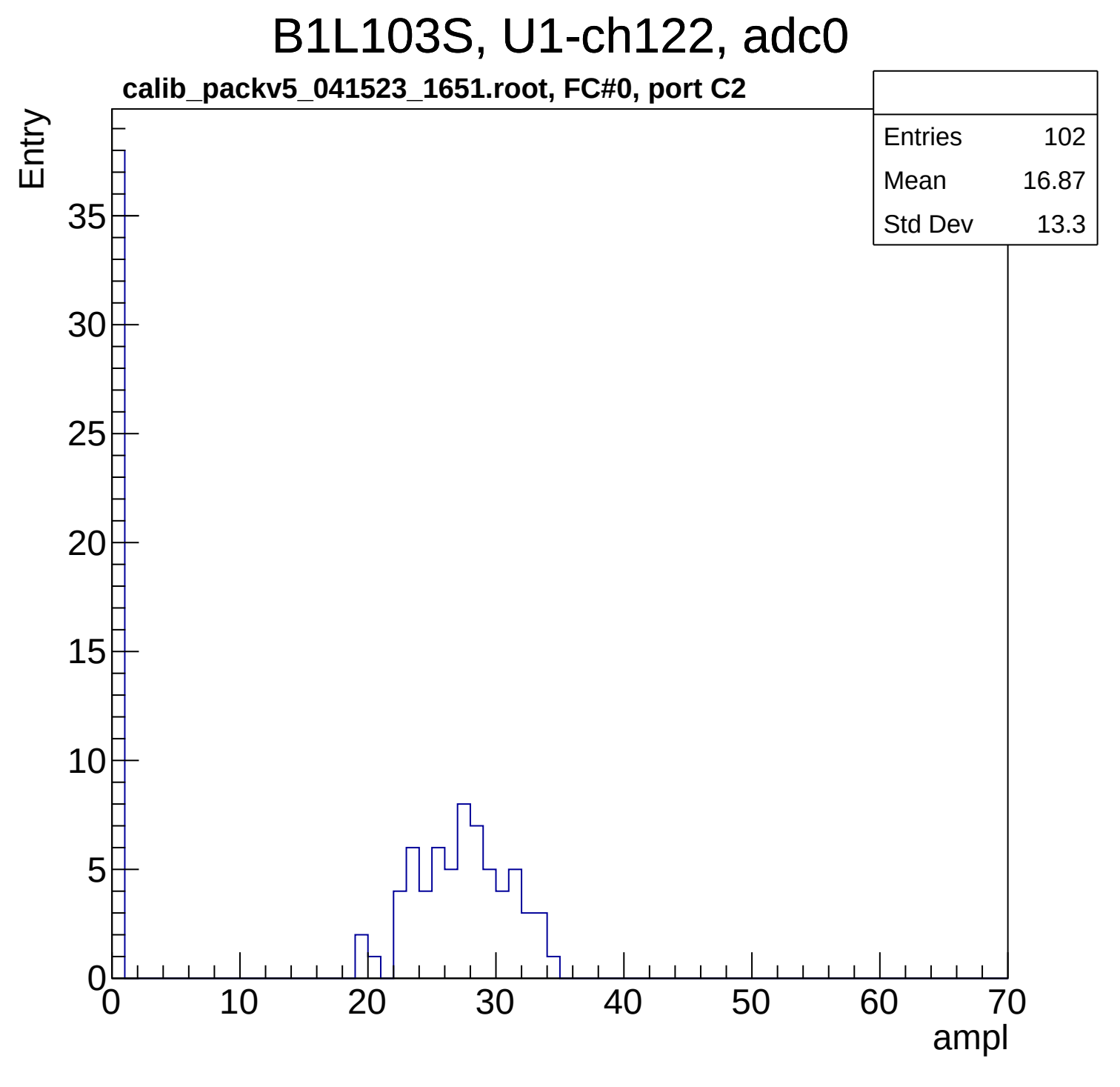
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U1-ch121, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 8.5
Std Dev 21.39
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch122, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 102
Mean 16.87
Std Dev 13.3
Entry
ampl
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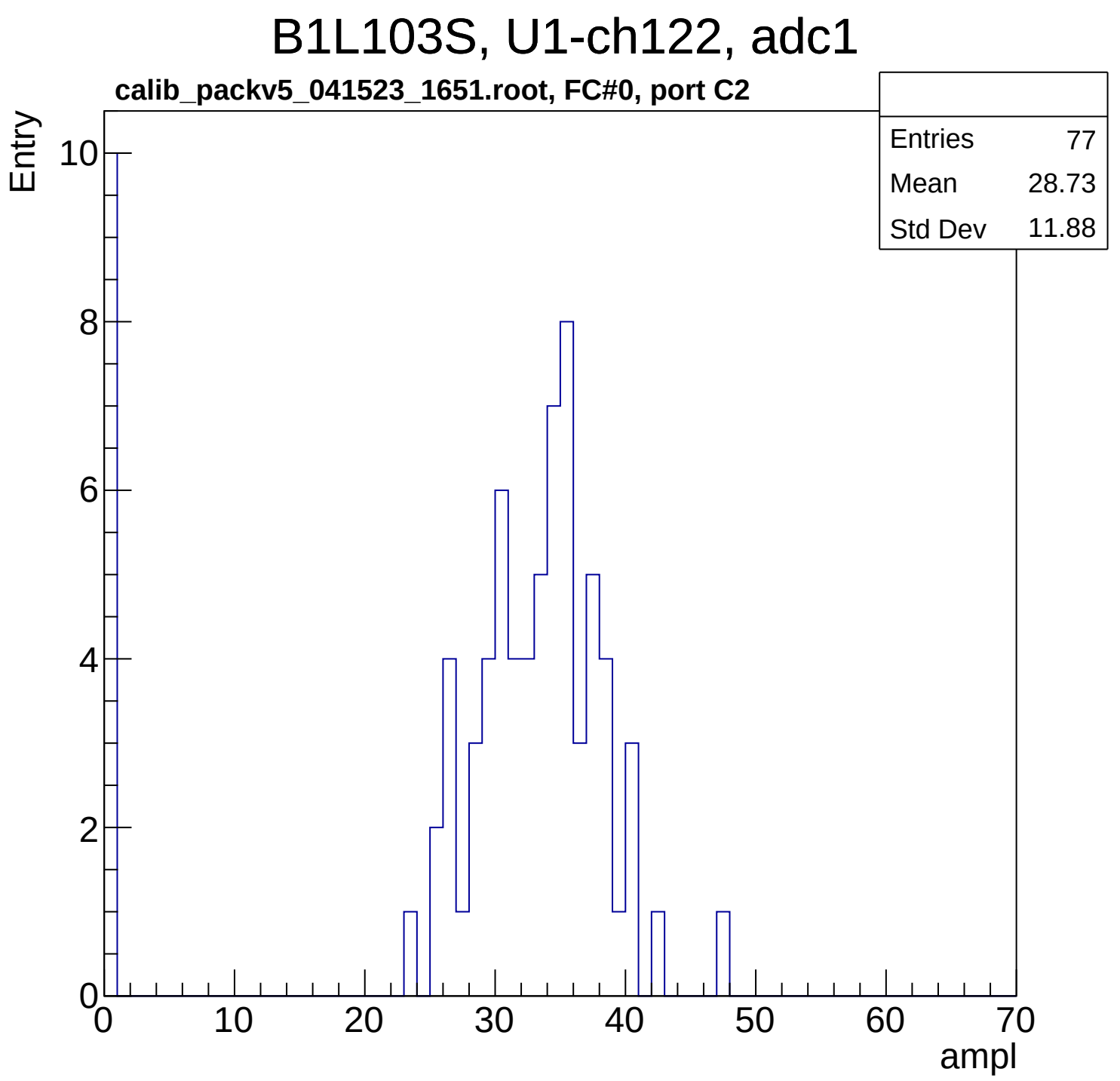
5
10
15
20
25
30
35
0
10
20
30
40
50
60
70


B1L103S, U1-ch122, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 28.73
Std Dev 11.88
Entry
ampl
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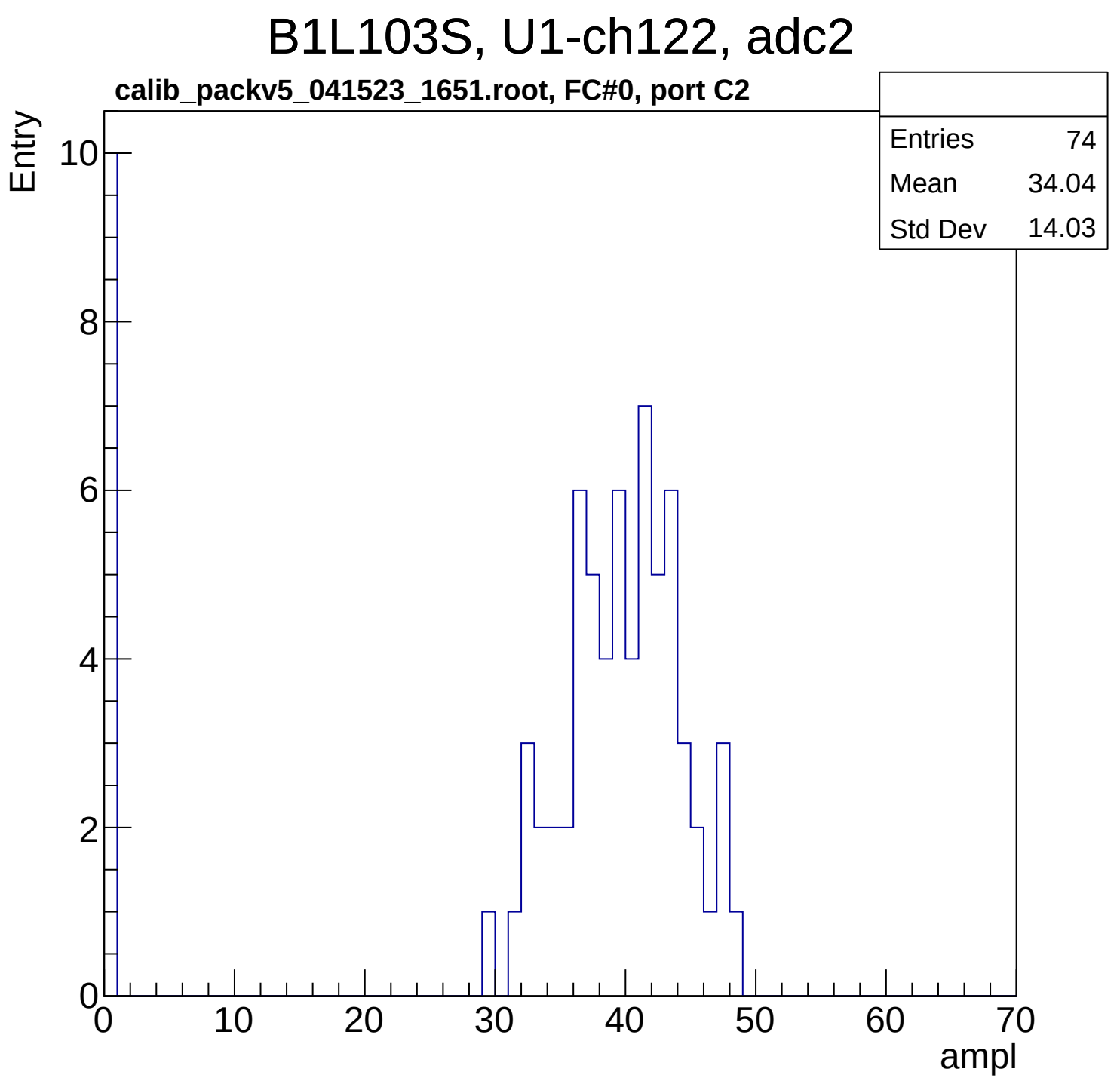
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U1-ch122, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 34.04
Std Dev 14.03
Entry
ampl
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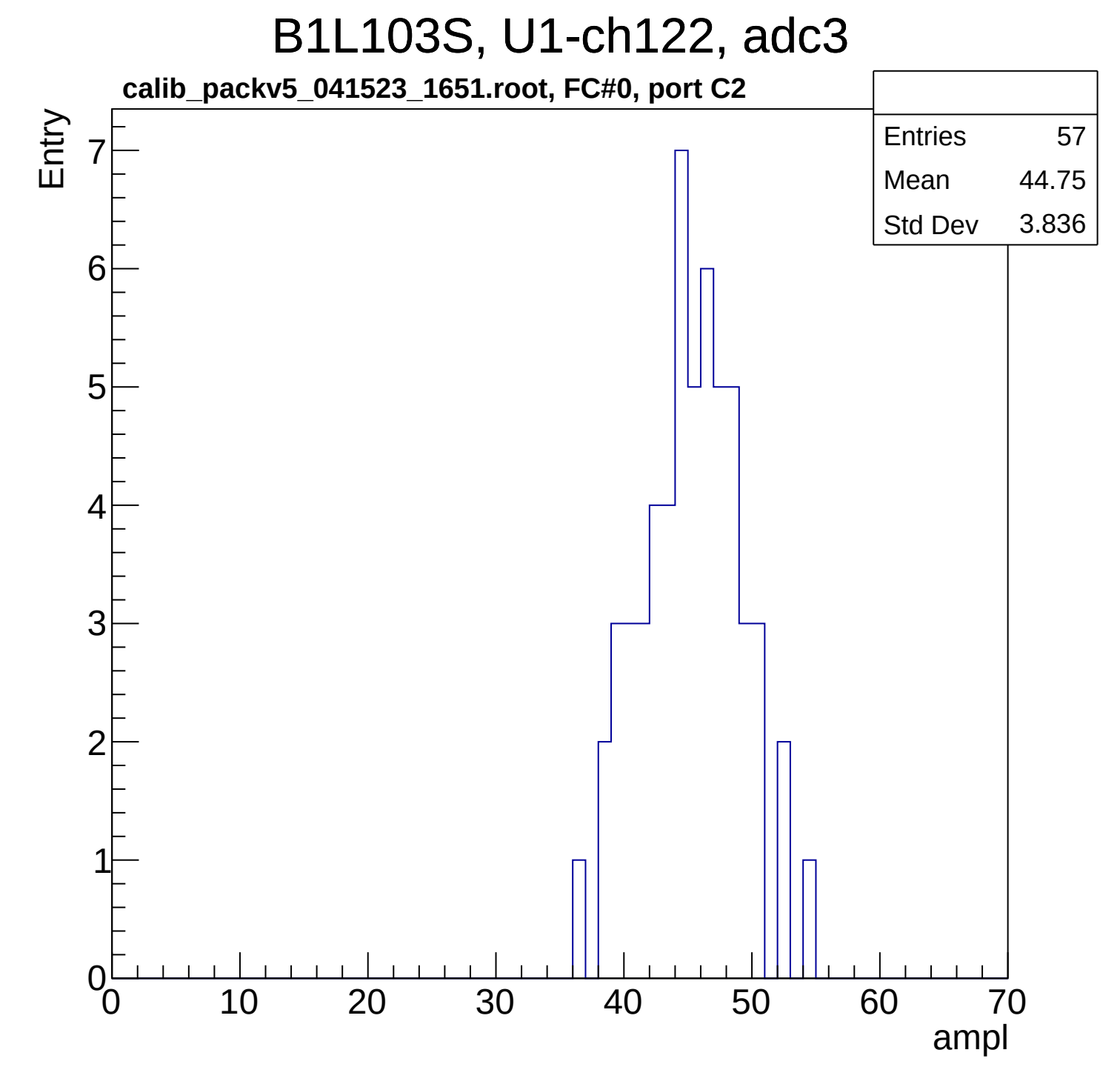
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U1-ch122, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 44.75
Std Dev 3.836
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
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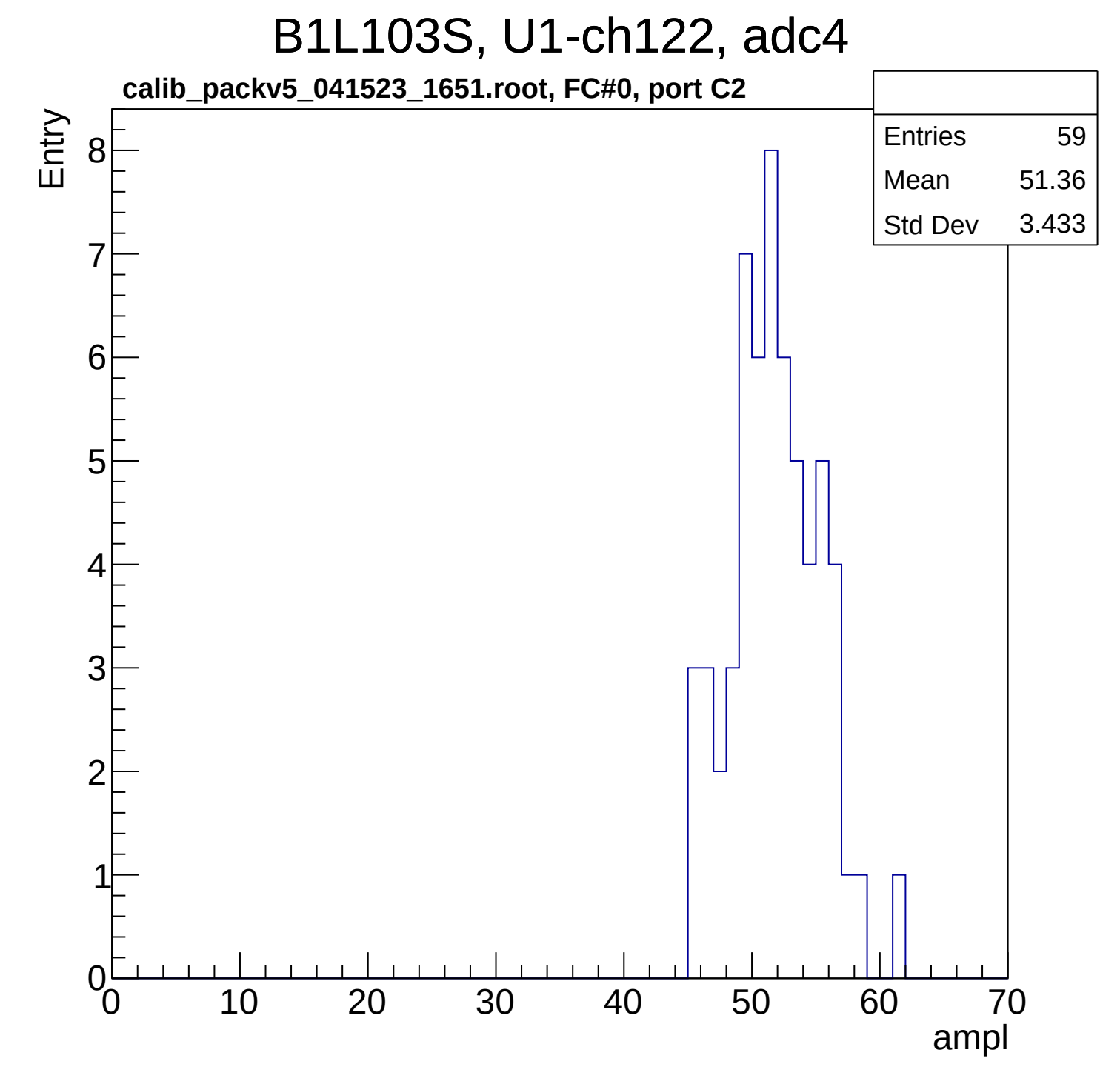
40
50
60
70


B1L103S, U1-ch122, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 51.36
Std Dev 3.433
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
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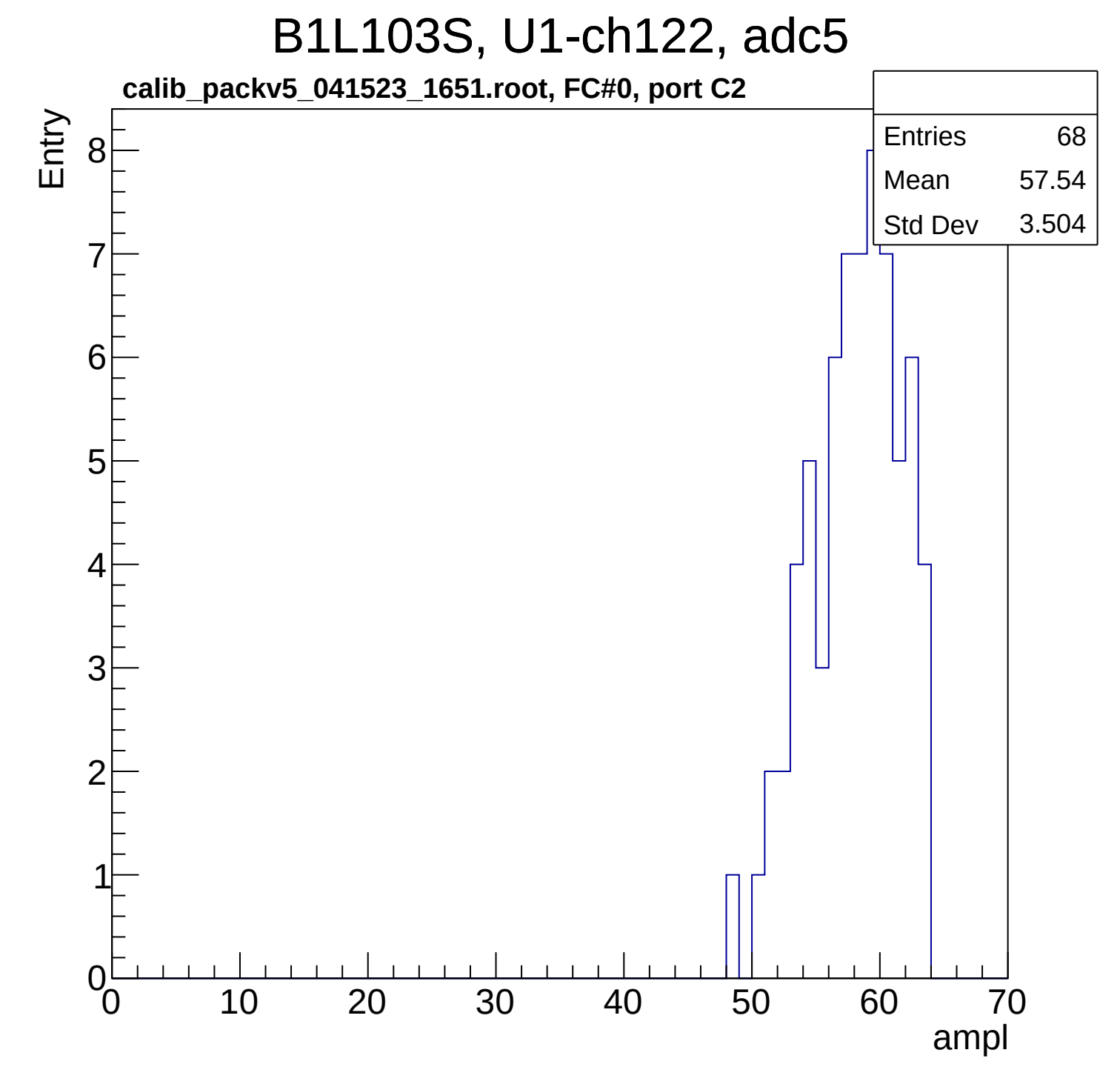
40
50
60
70


B1L103S, U1-ch122, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 57.54
Std Dev 3.504
Entry
ampl
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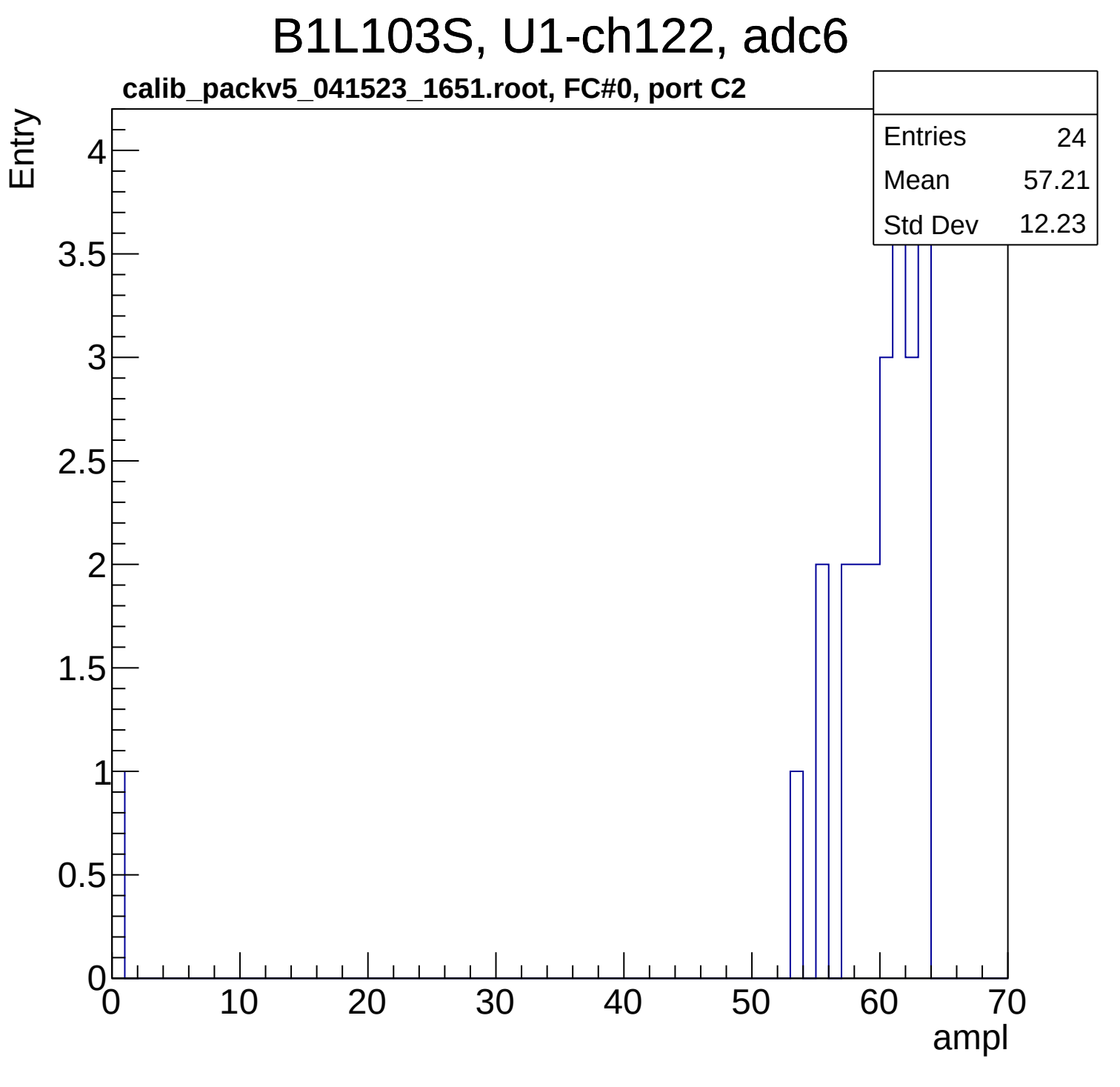
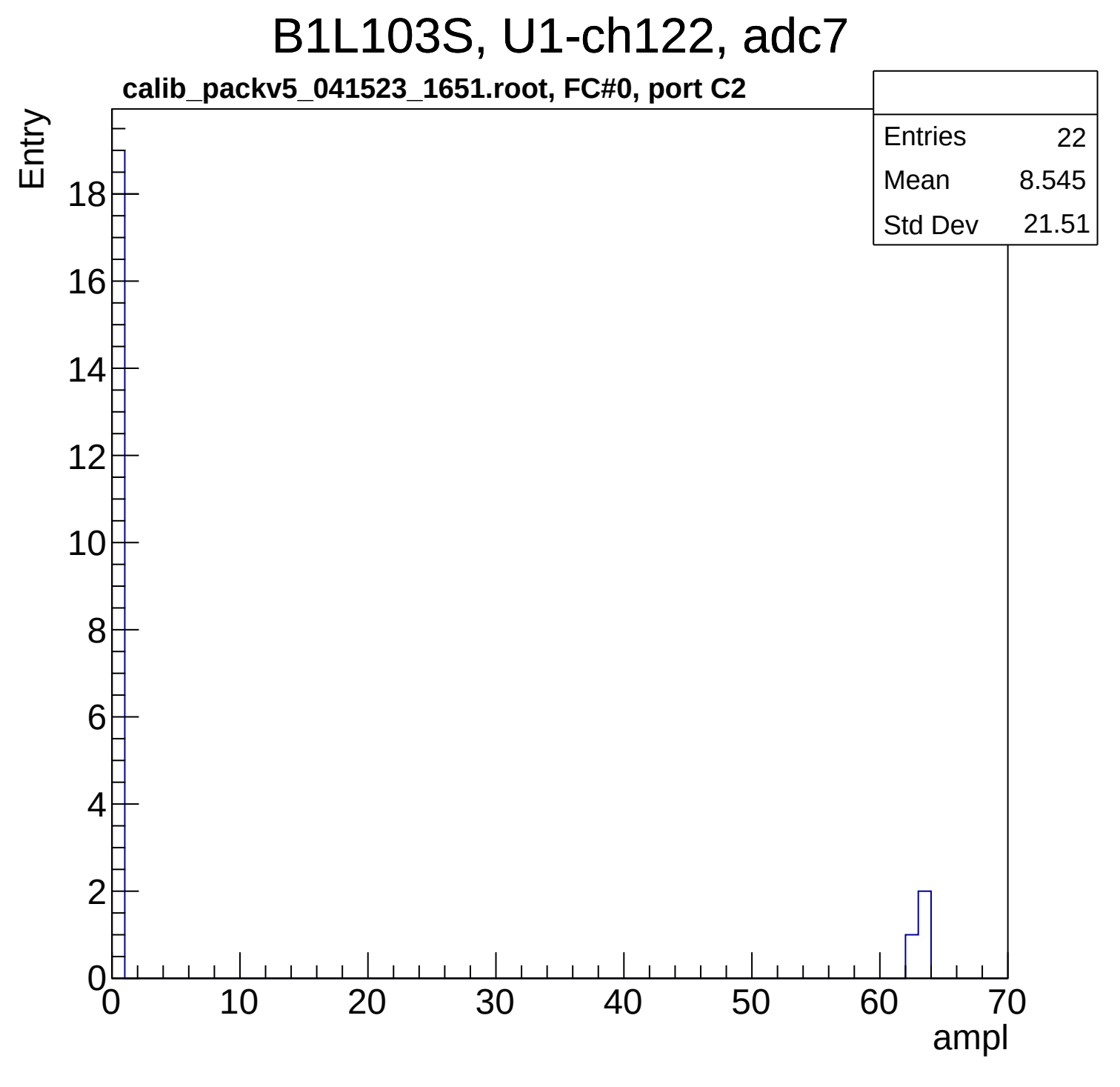
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U1-ch122, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 24
Mean 57.21
Std Dev 12.23
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U1-ch122, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 8.545
Std Dev 21.51
Entry
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6
8
10
12
14
16
18
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10
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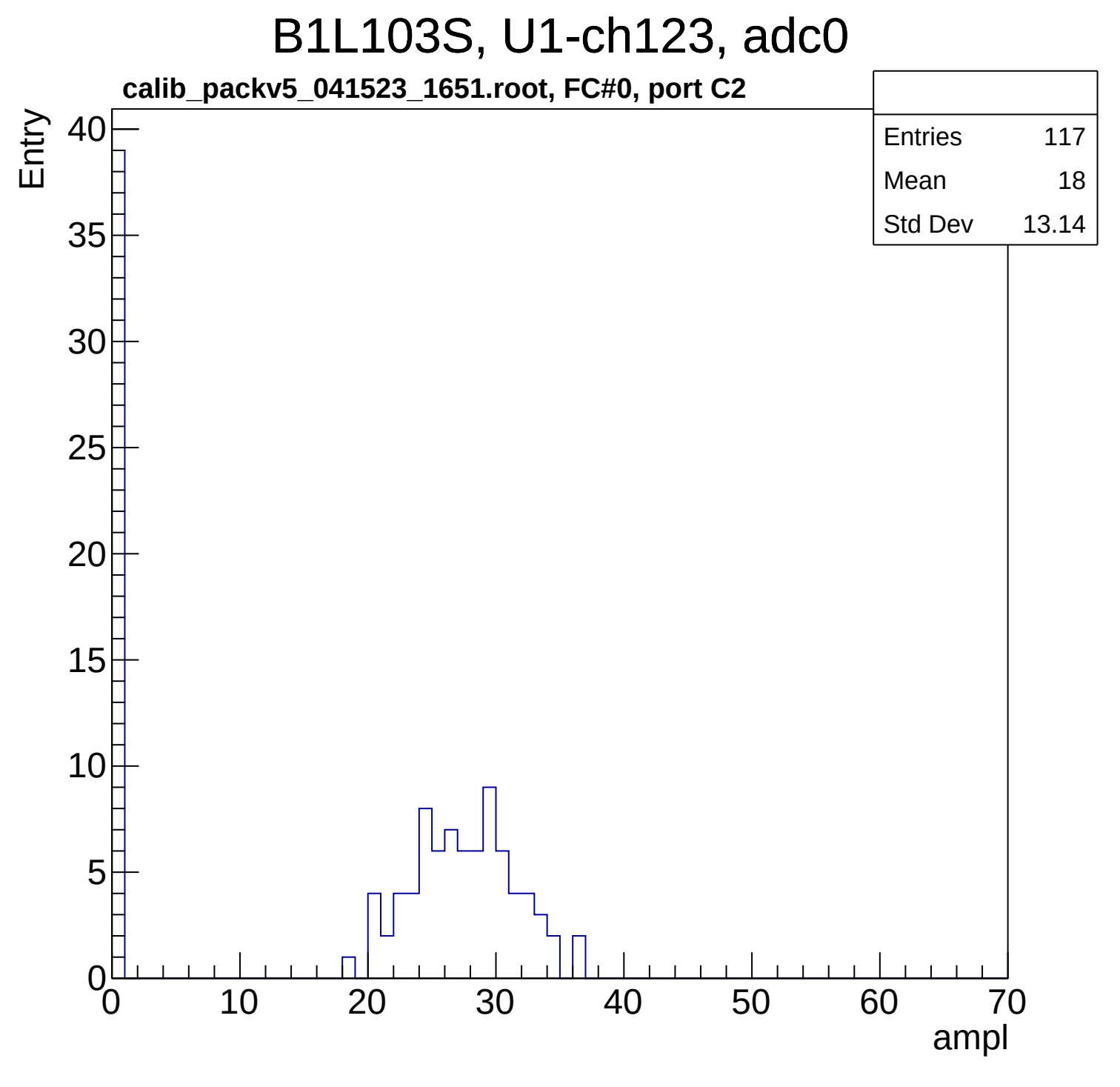
30
40
50
60
70
ampl


B1L103S, U1-ch123, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 117
Mean 18
Std Dev 13.14
Entry
ampl
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5
10
15
20
25
30
35
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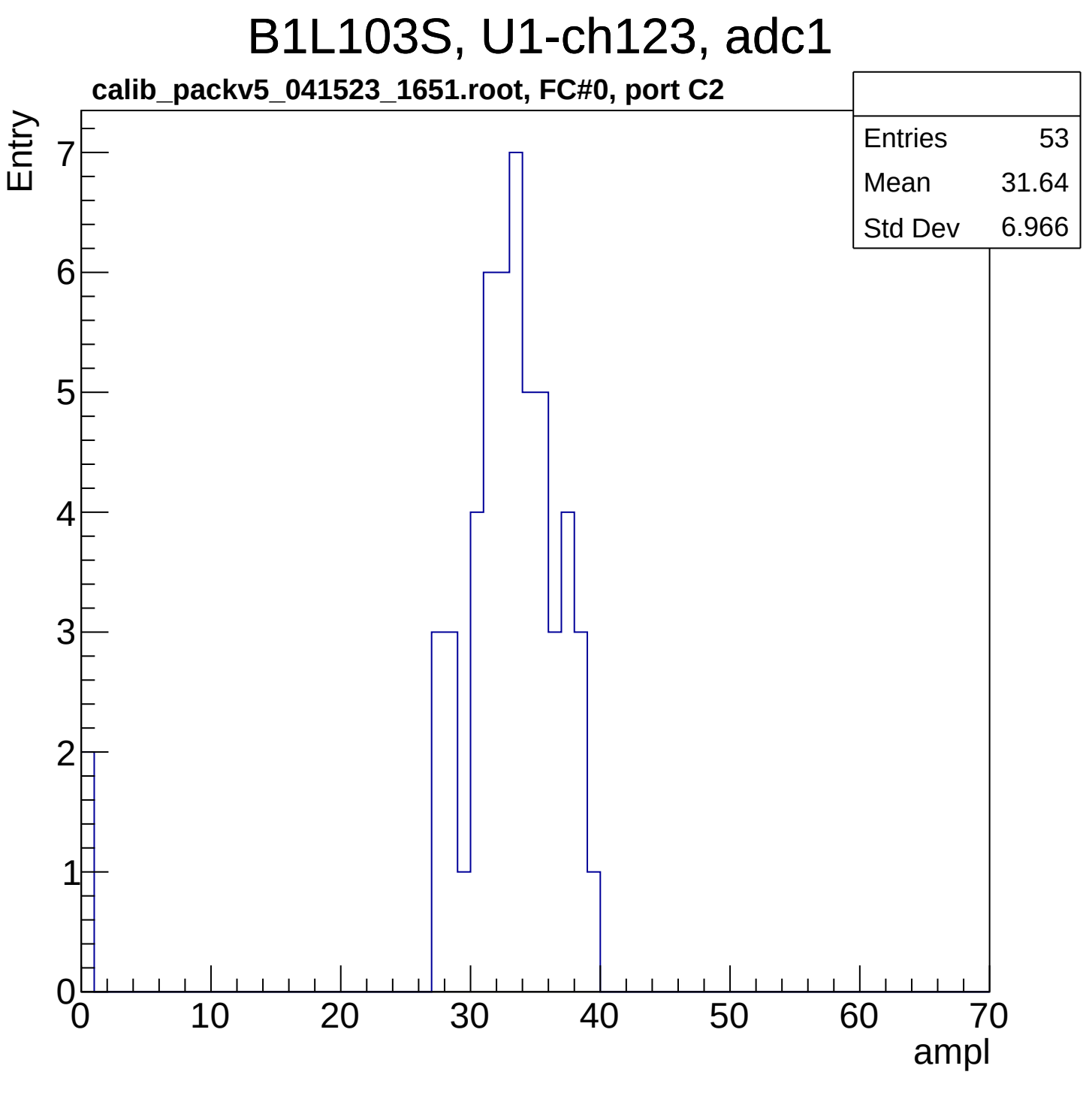
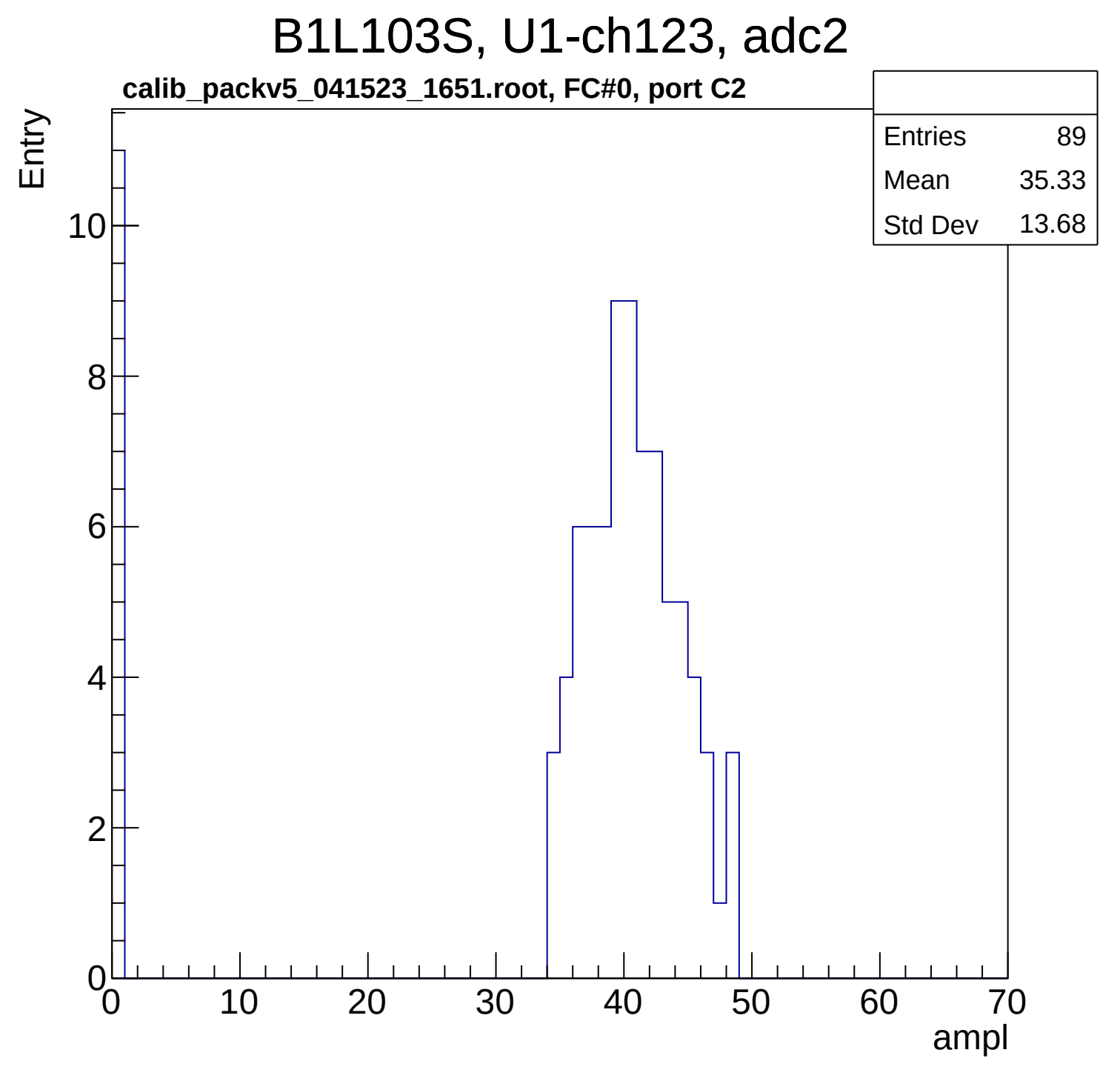
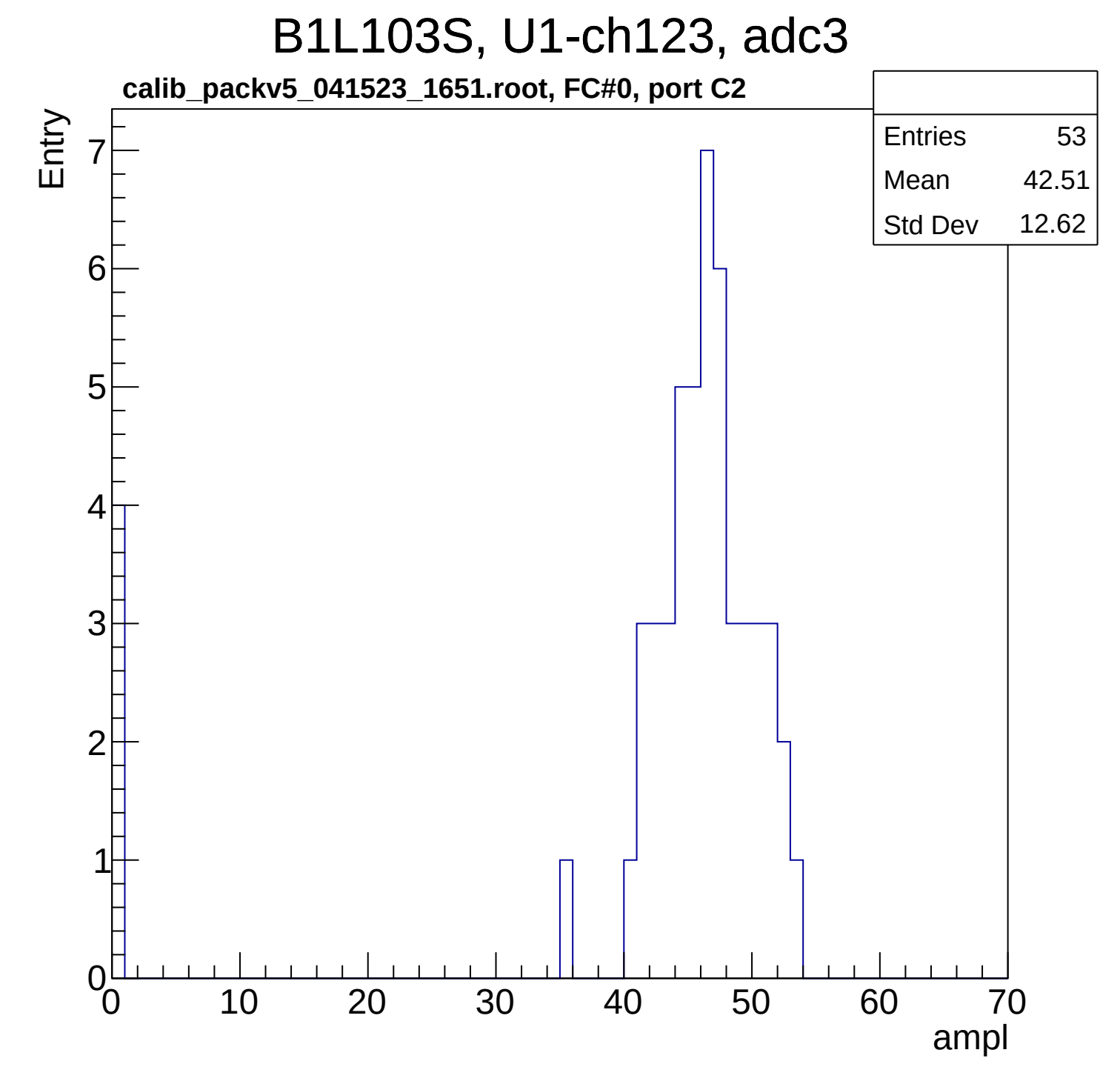
0
10
20
30
40
50
60
70


B1L103S, U1-ch123, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 31.64
Std Dev 6.966
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U1-ch123, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 89
Mean 35.33
Std Dev 13.68
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch123, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 42.51
Std Dev 12.62
Entry
ampl
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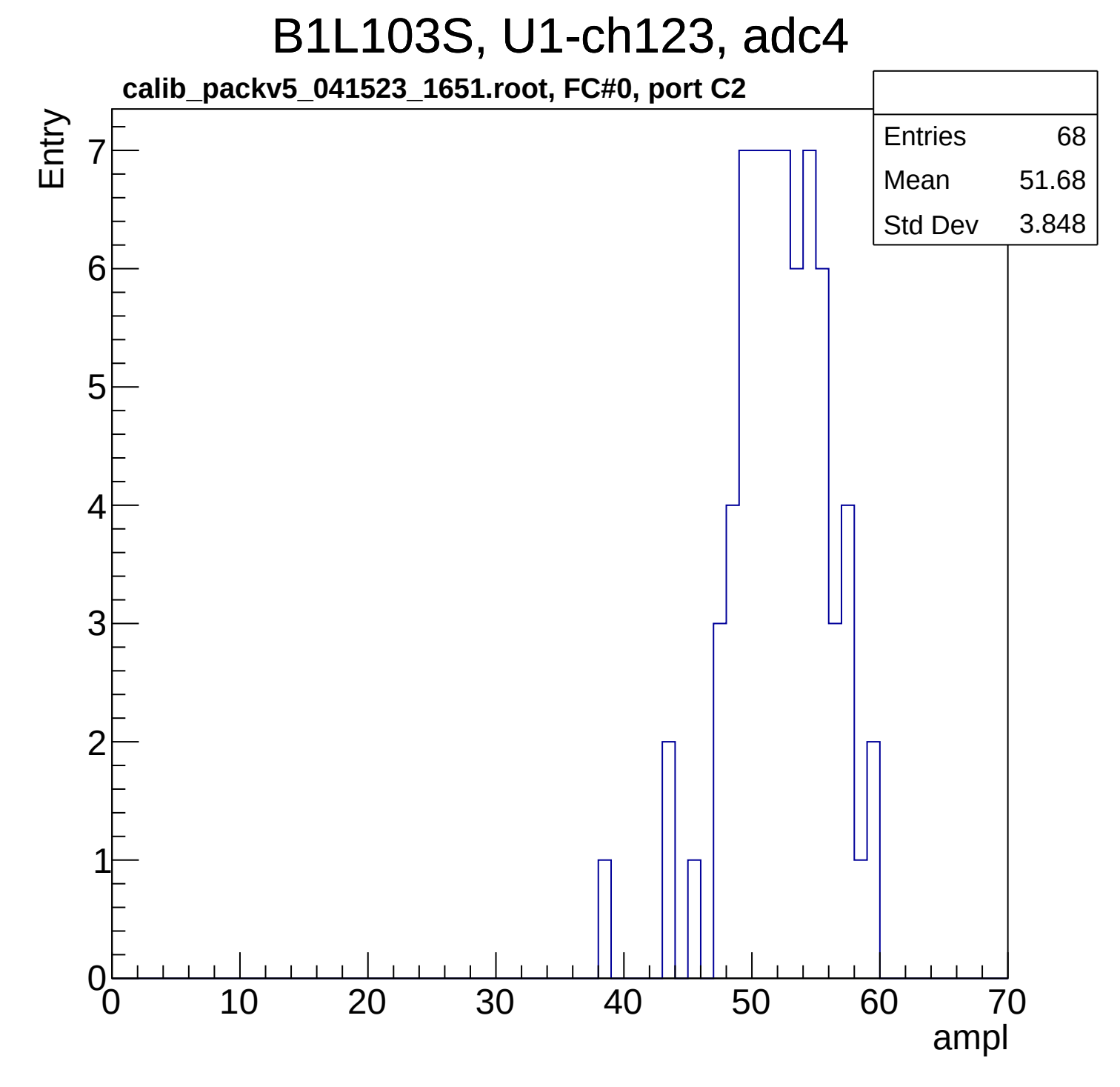
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U1-ch123, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 51.68
Std Dev 3.848
Entry
ampl
0
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2
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4
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7
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40
50
60
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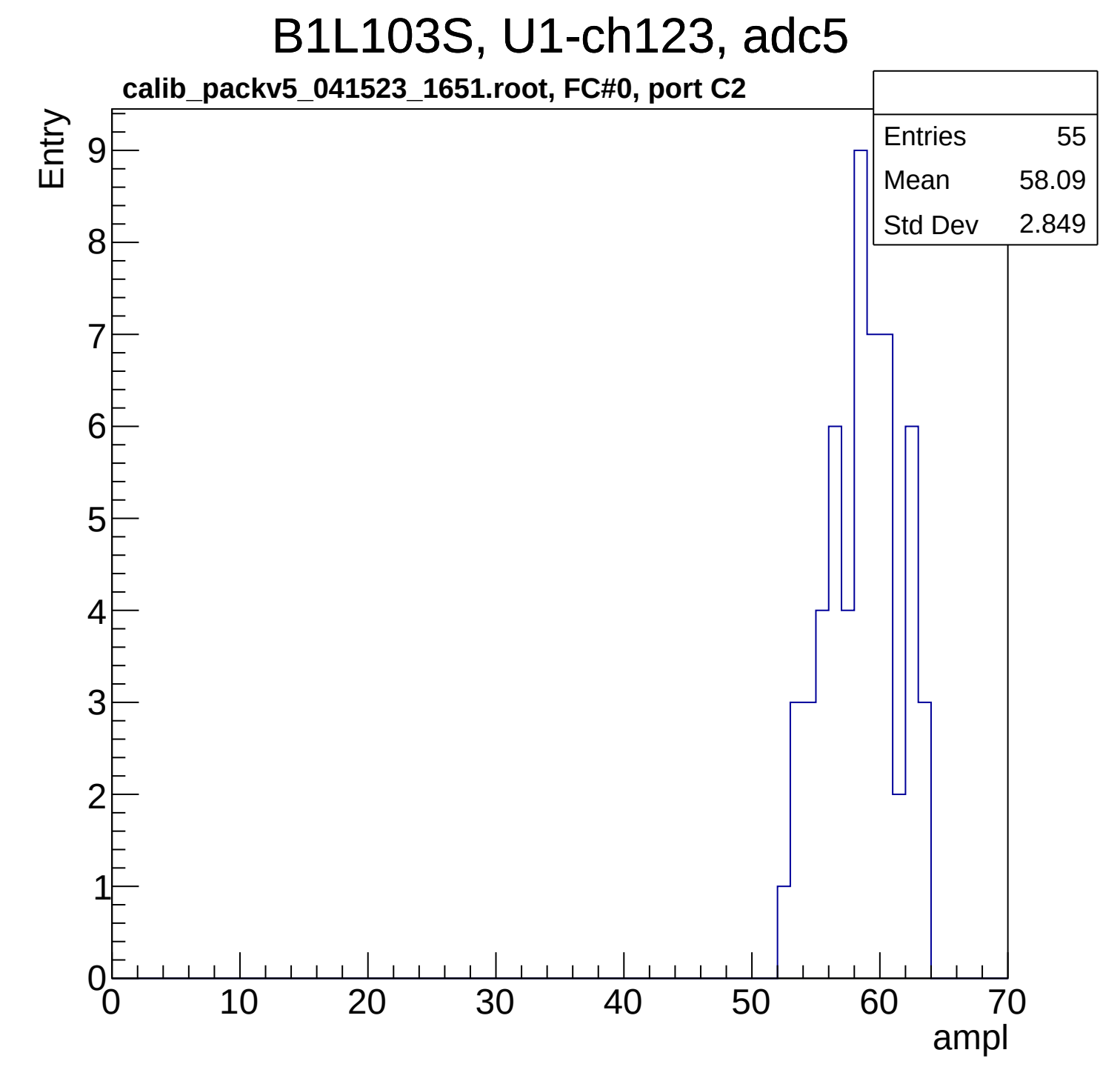
B1L103S, U1-ch123, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 58.09
Std Dev 2.849
Entry
ampl
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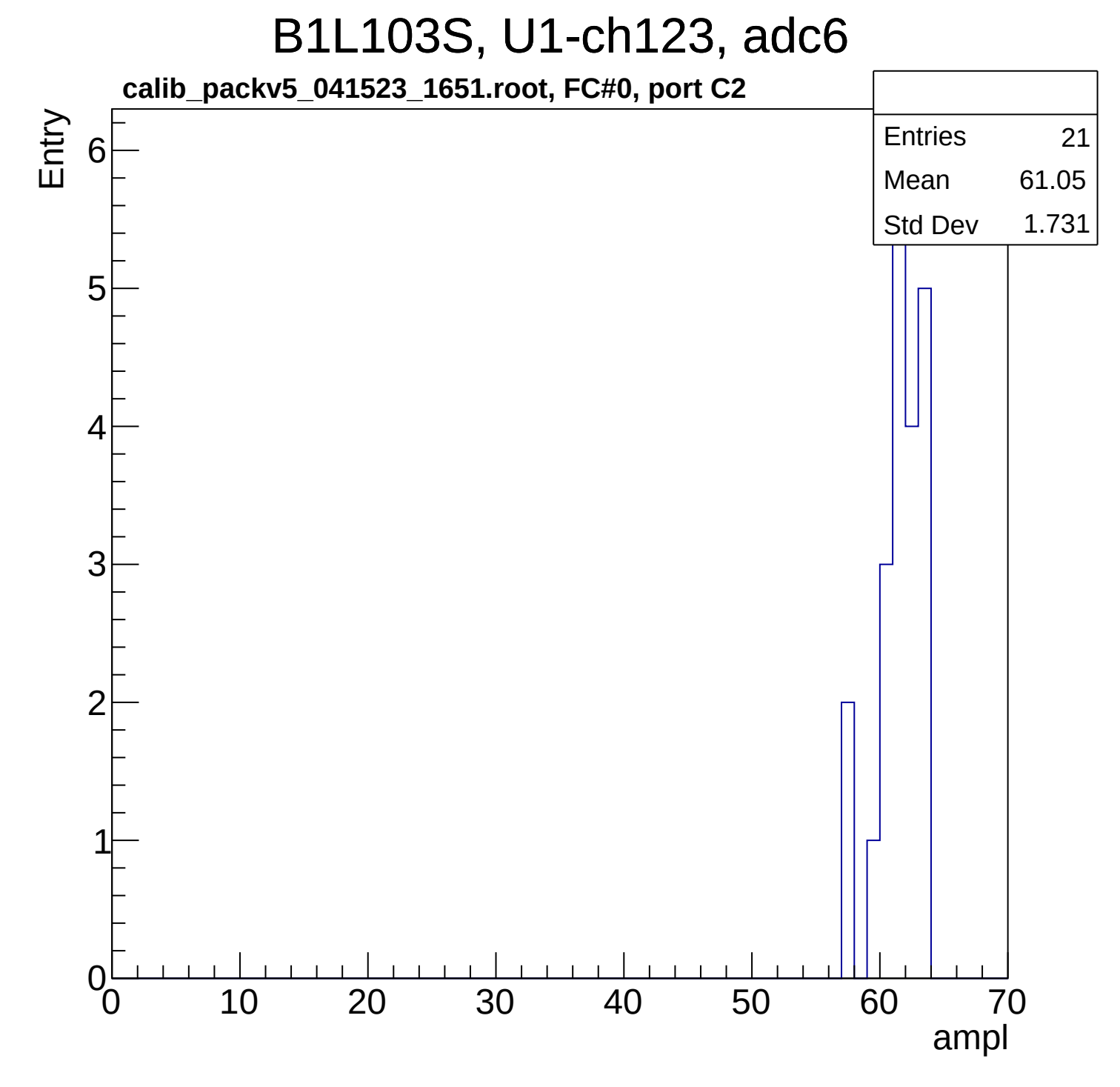
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U1-ch123, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 61.05
Std Dev 1.731
Entry
ampl
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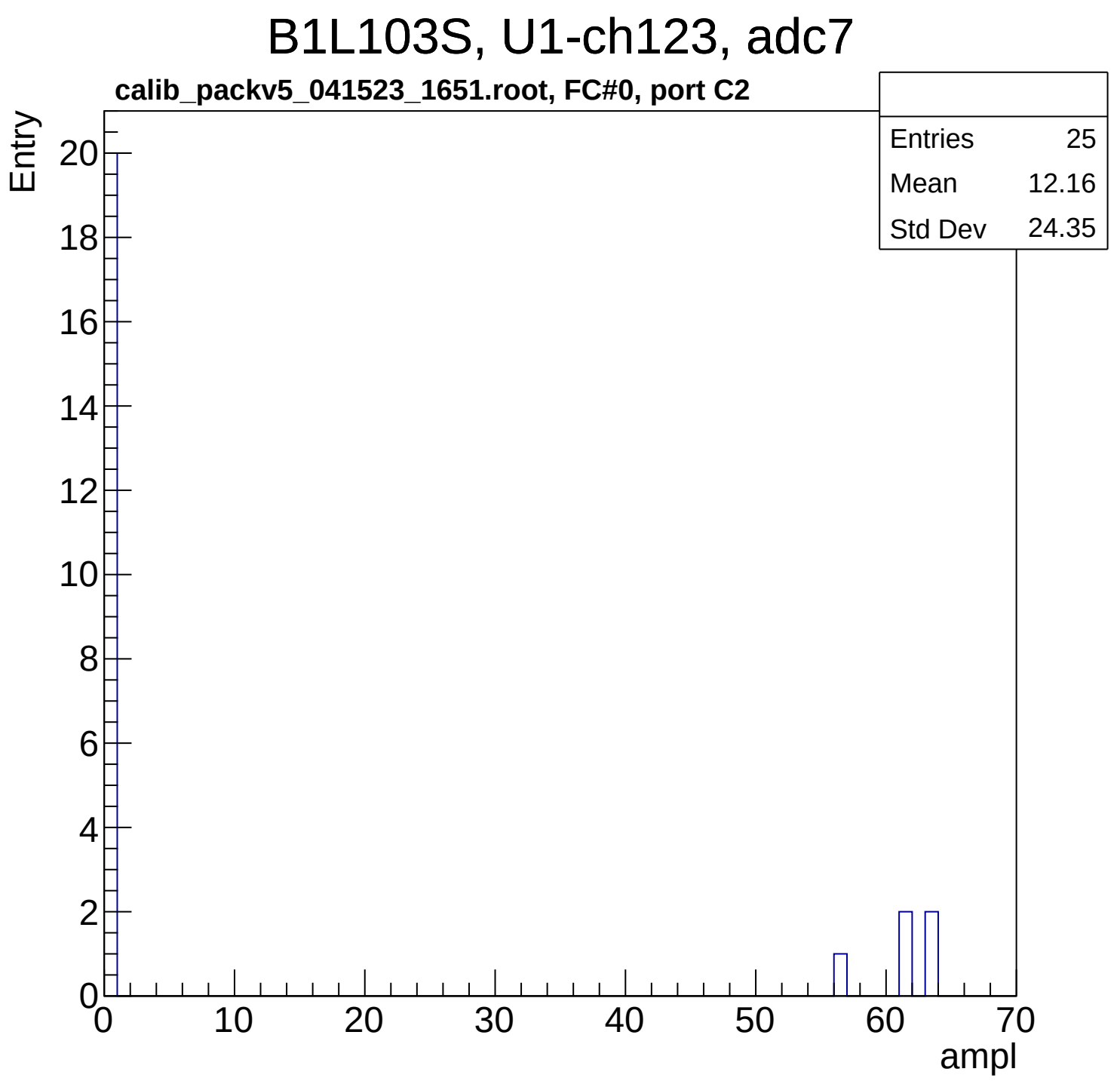
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U1-ch123, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 25
Mean 12.16
Std Dev 24.35
Entry
0
2
4
6
8
10
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16
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20
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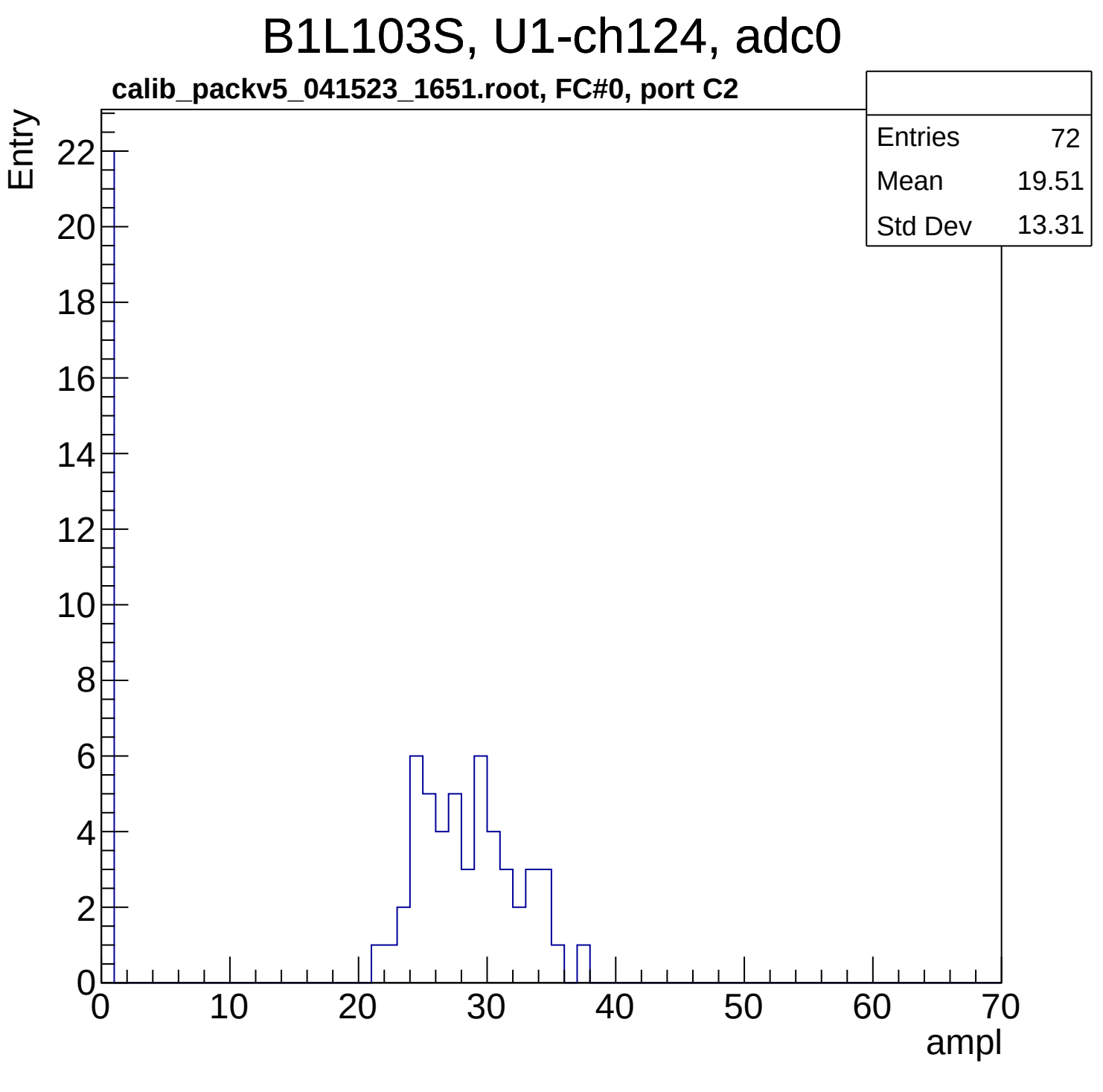
50
60
70
ampl


B1L103S, U1-ch124, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 19.51
Std Dev 13.31
Entry
0
2
4
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10
12
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16
18
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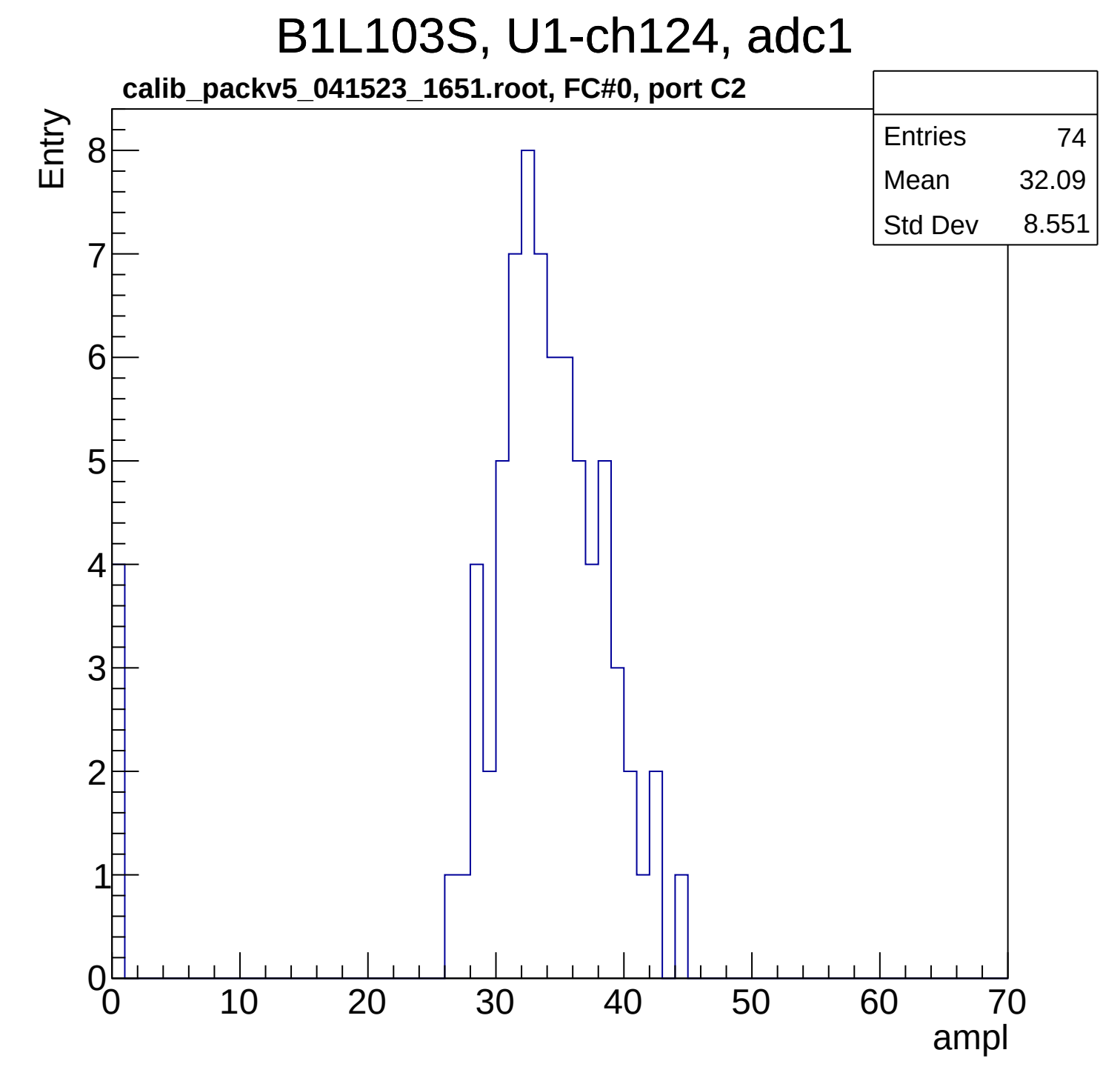
ampl


B1L103S, U1-ch124, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 32.09
Std Dev 8.551
Entry
ampl
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1
2
3
4
5
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7
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0
10
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40
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60
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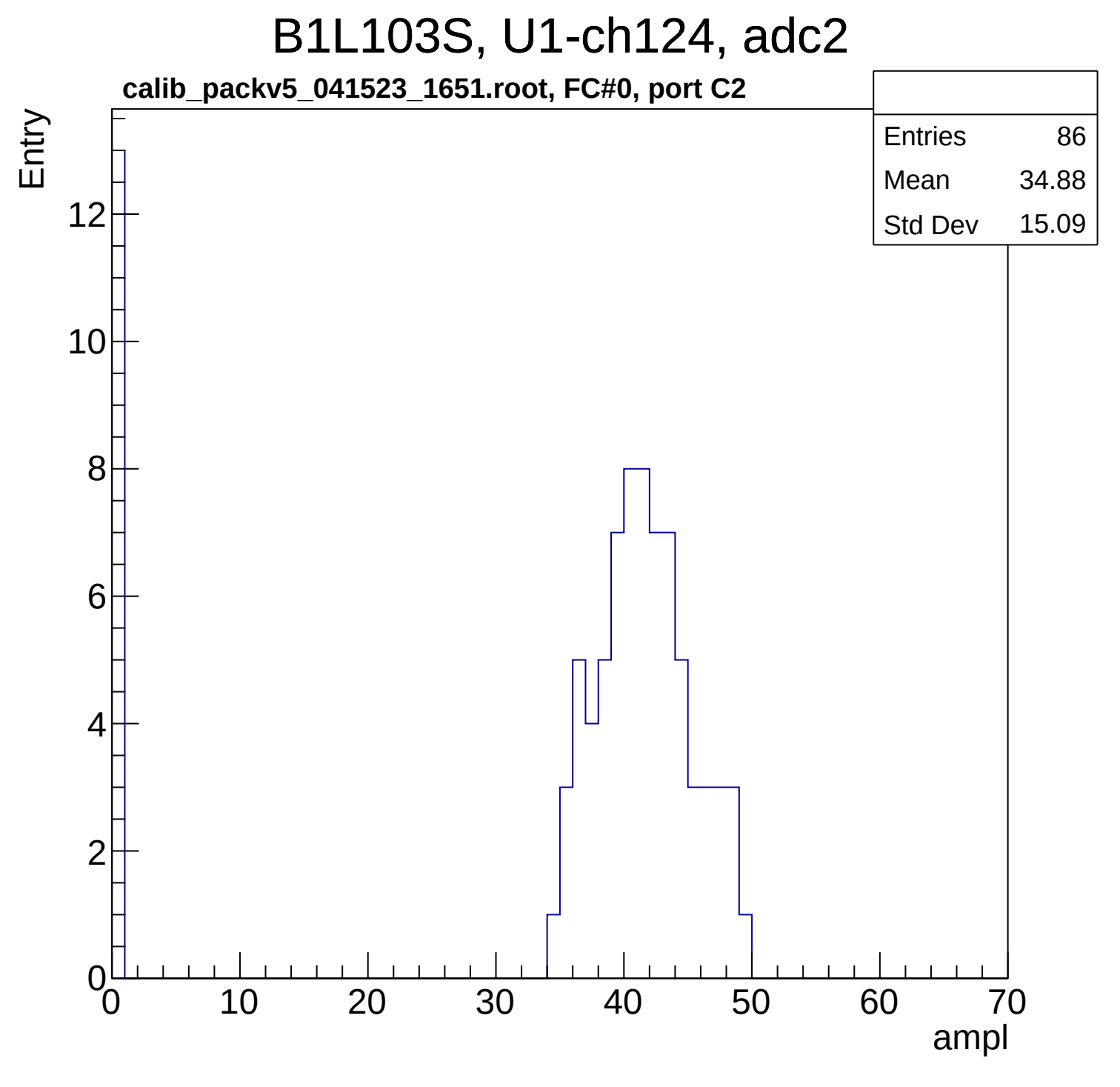
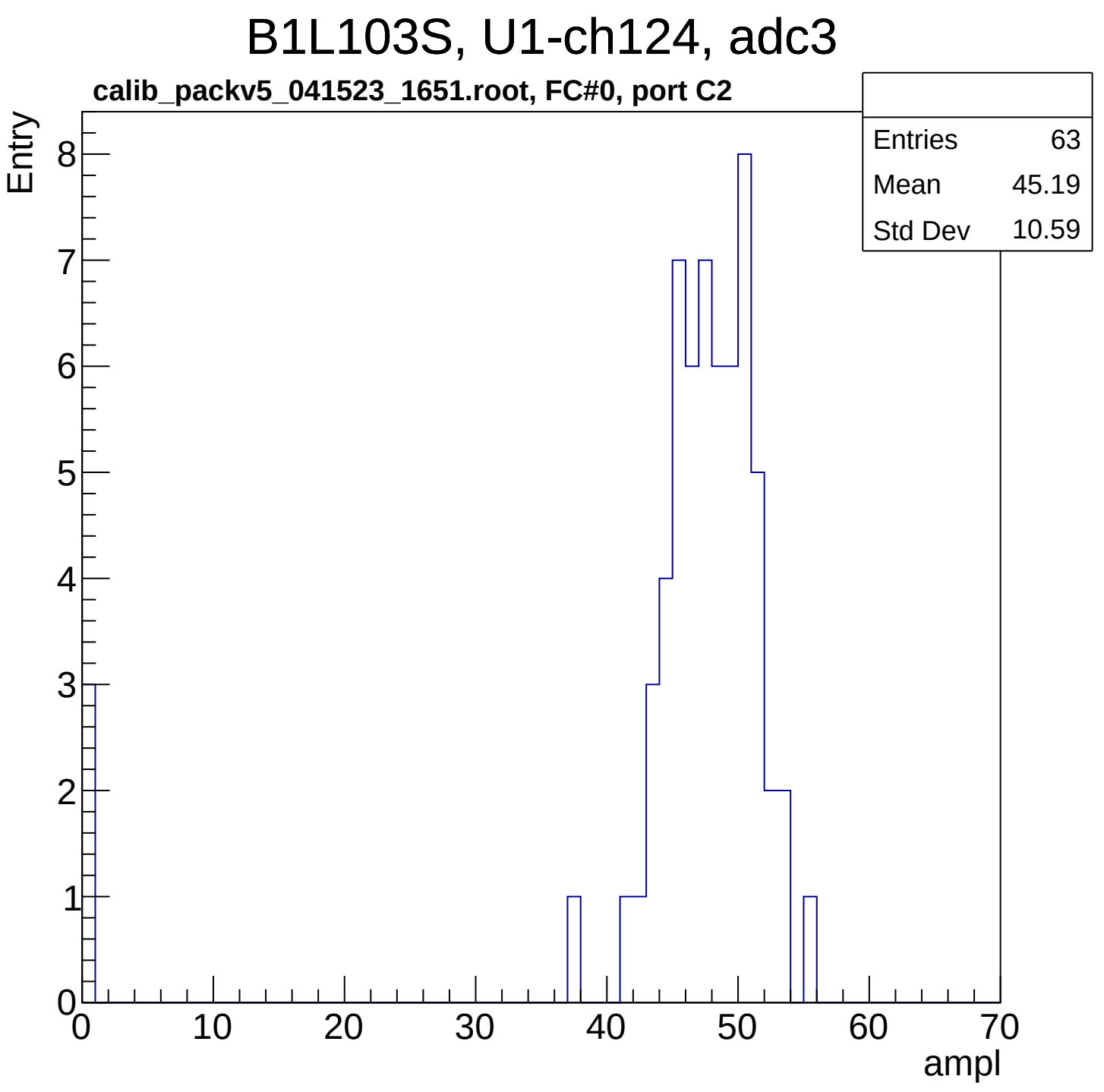

B1L103S, U1-ch124, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 34.88
Std Dev 15.09
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch124, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 45.19
Std Dev 10.59
Entry
ampl
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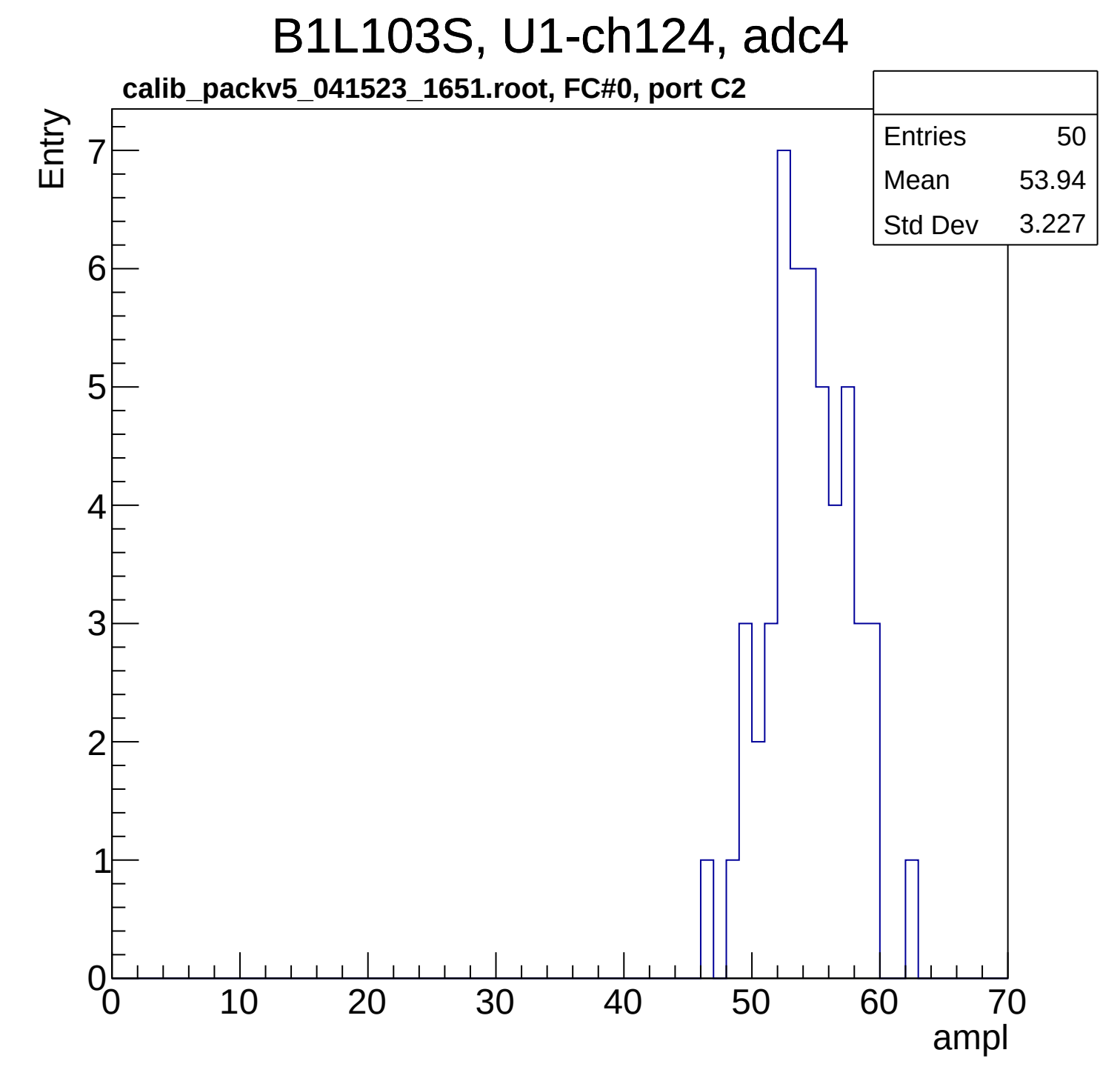
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U1-ch124, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 53.94
Std Dev 3.227
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
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40
50
60
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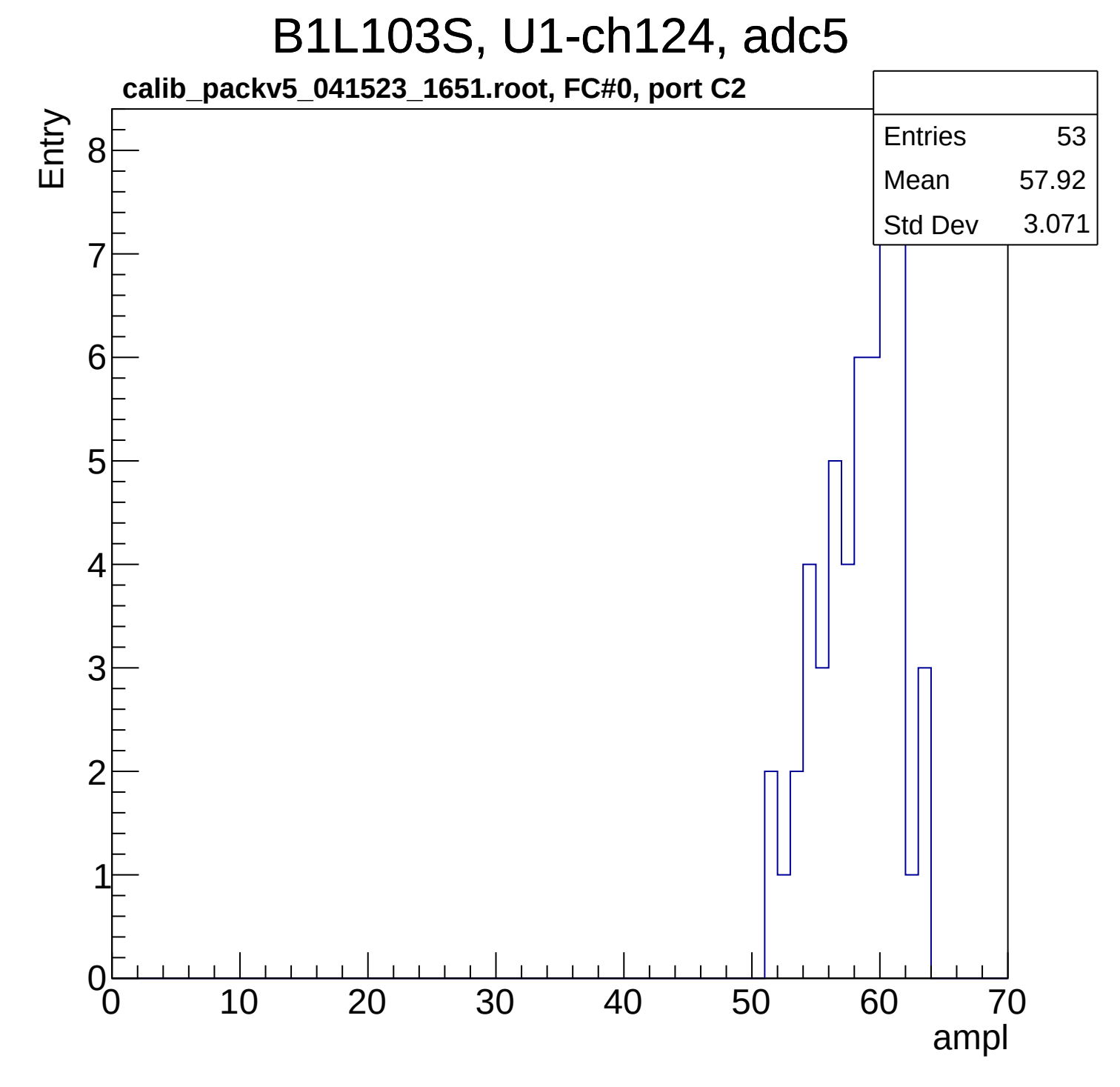
B1L103S, U1-ch124, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 57.92
Std Dev 3.071
Entry
ampl
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1
2
3
4
5
6
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0
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40
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60
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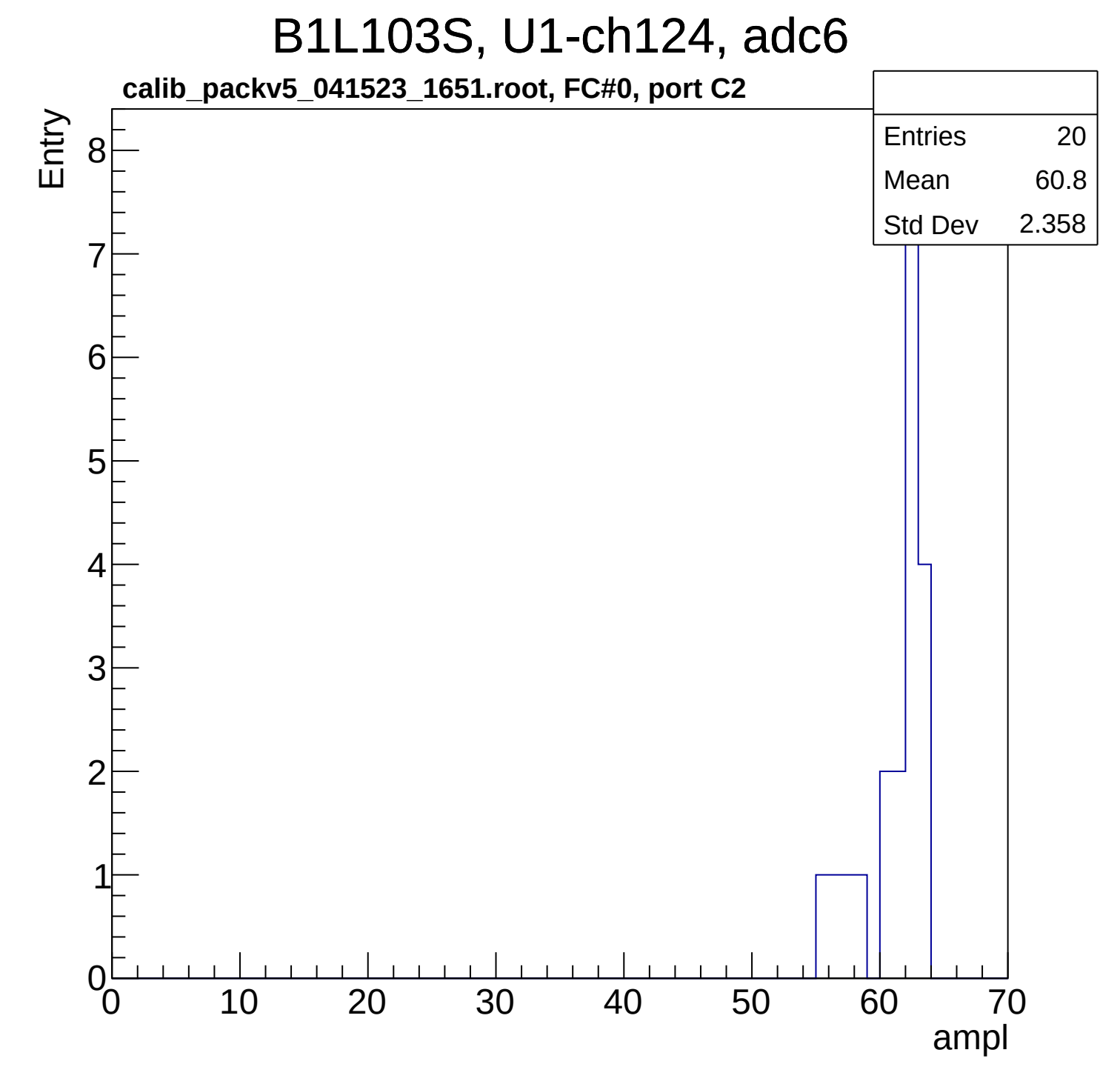
B1L103S, U1-ch124, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 60.8
Std Dev 2.358
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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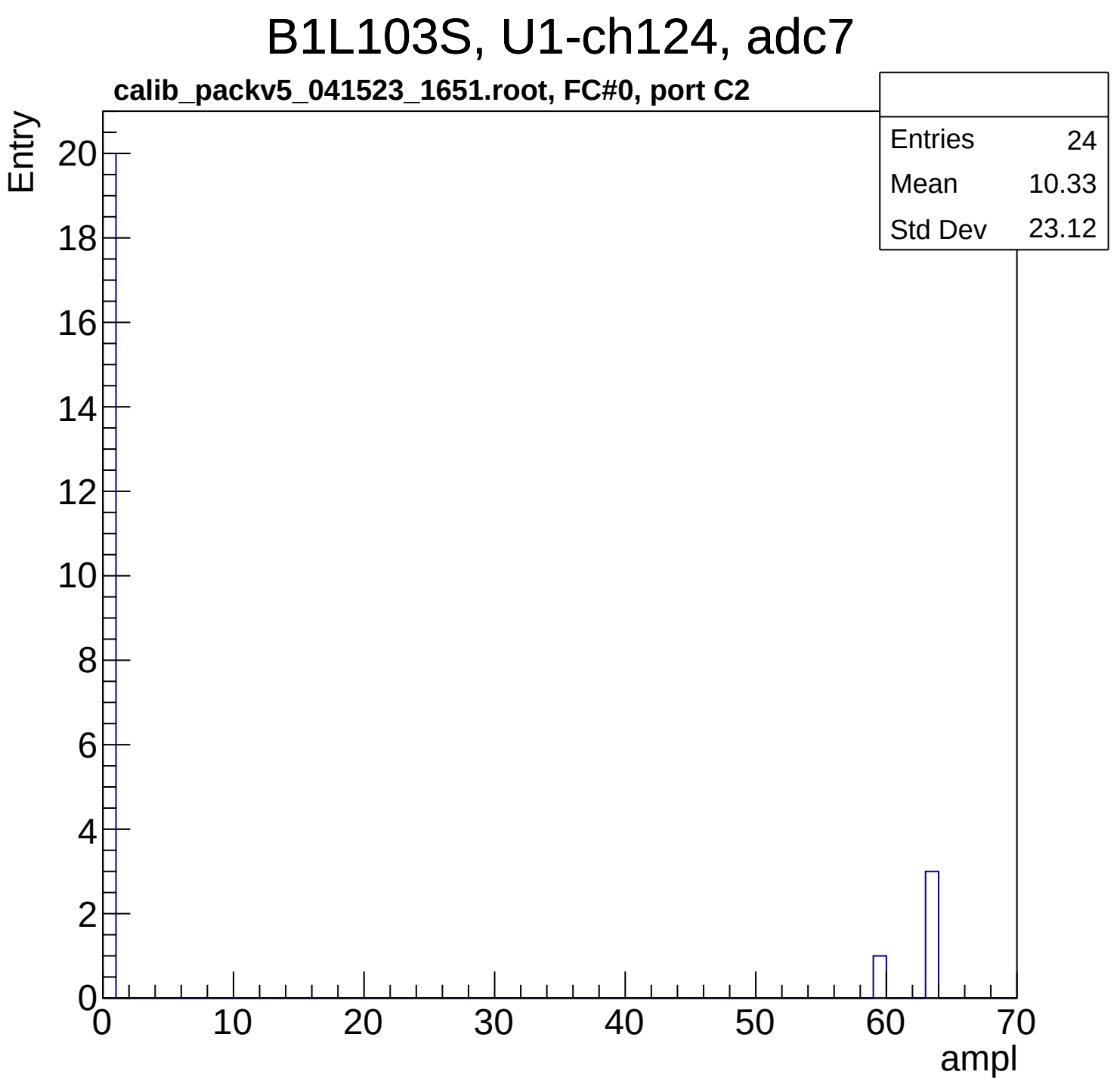
B1L103S, U1-ch124, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 24
Mean 10.33
Std Dev 23.12
Entry
0
2
4
6
8
10
12
14
16
18
20
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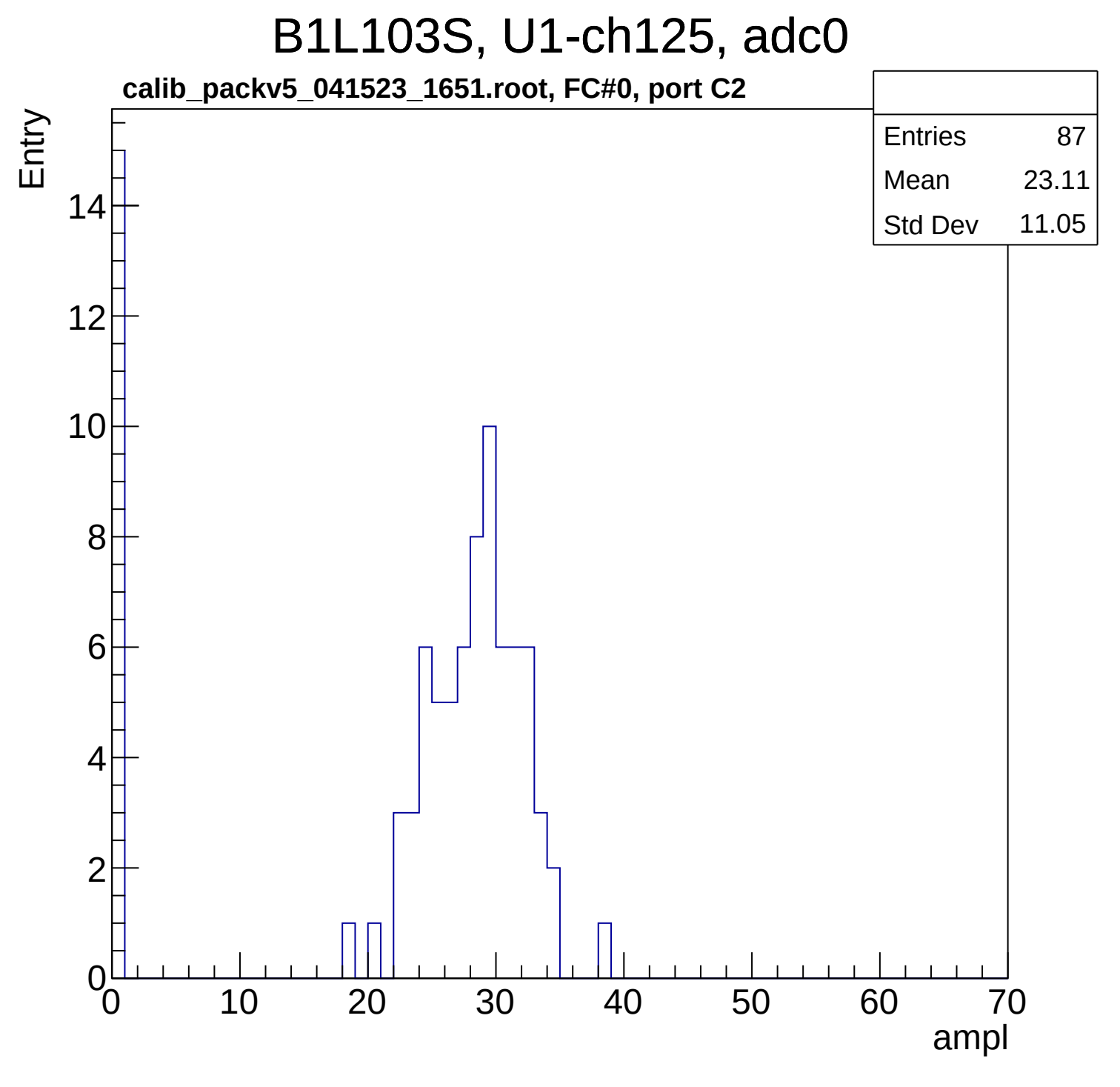
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch125, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 87
Mean 23.11
Std Dev 11.05
Entry
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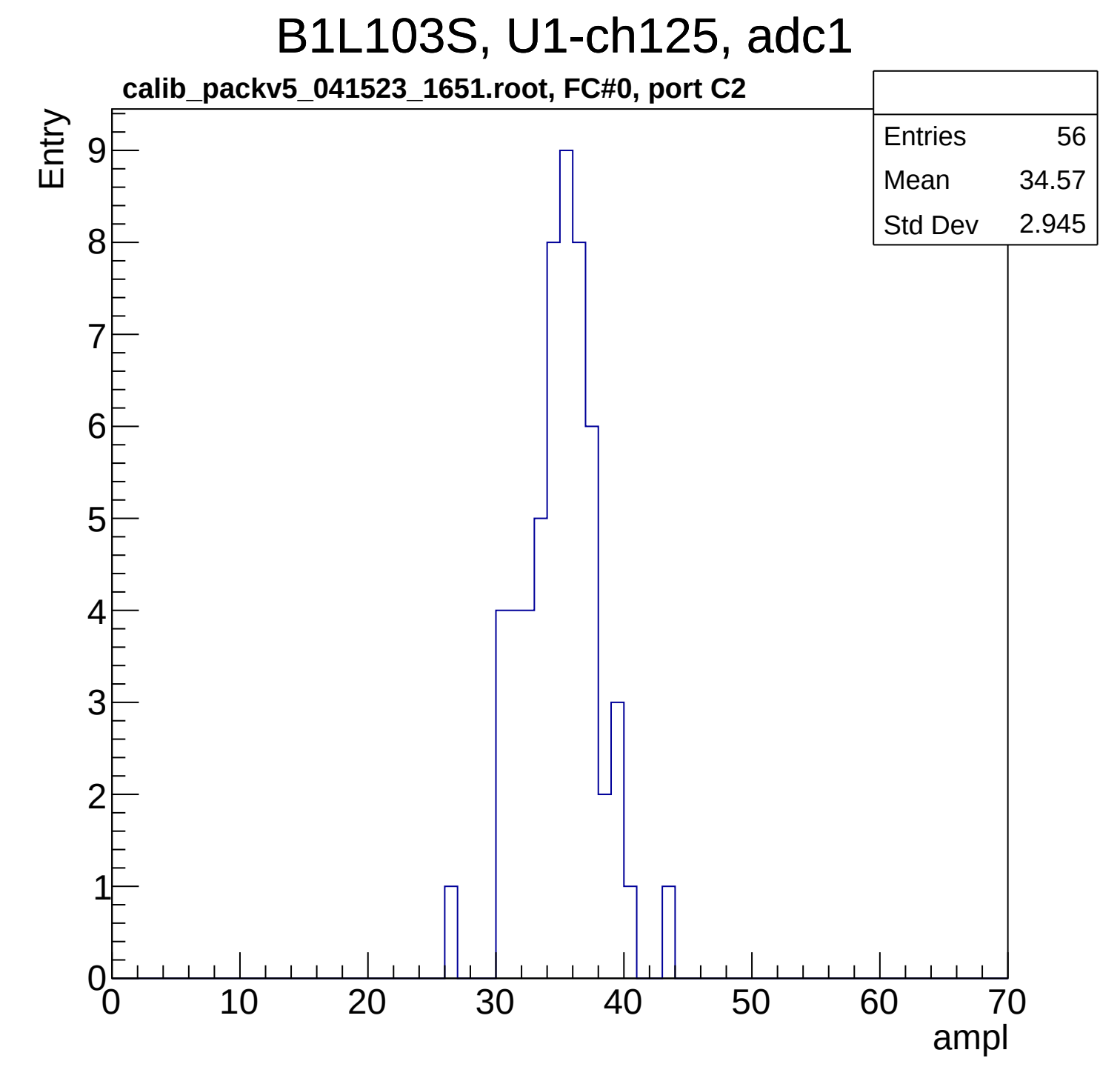
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch125, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 34.57
Std Dev 2.945
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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40
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60
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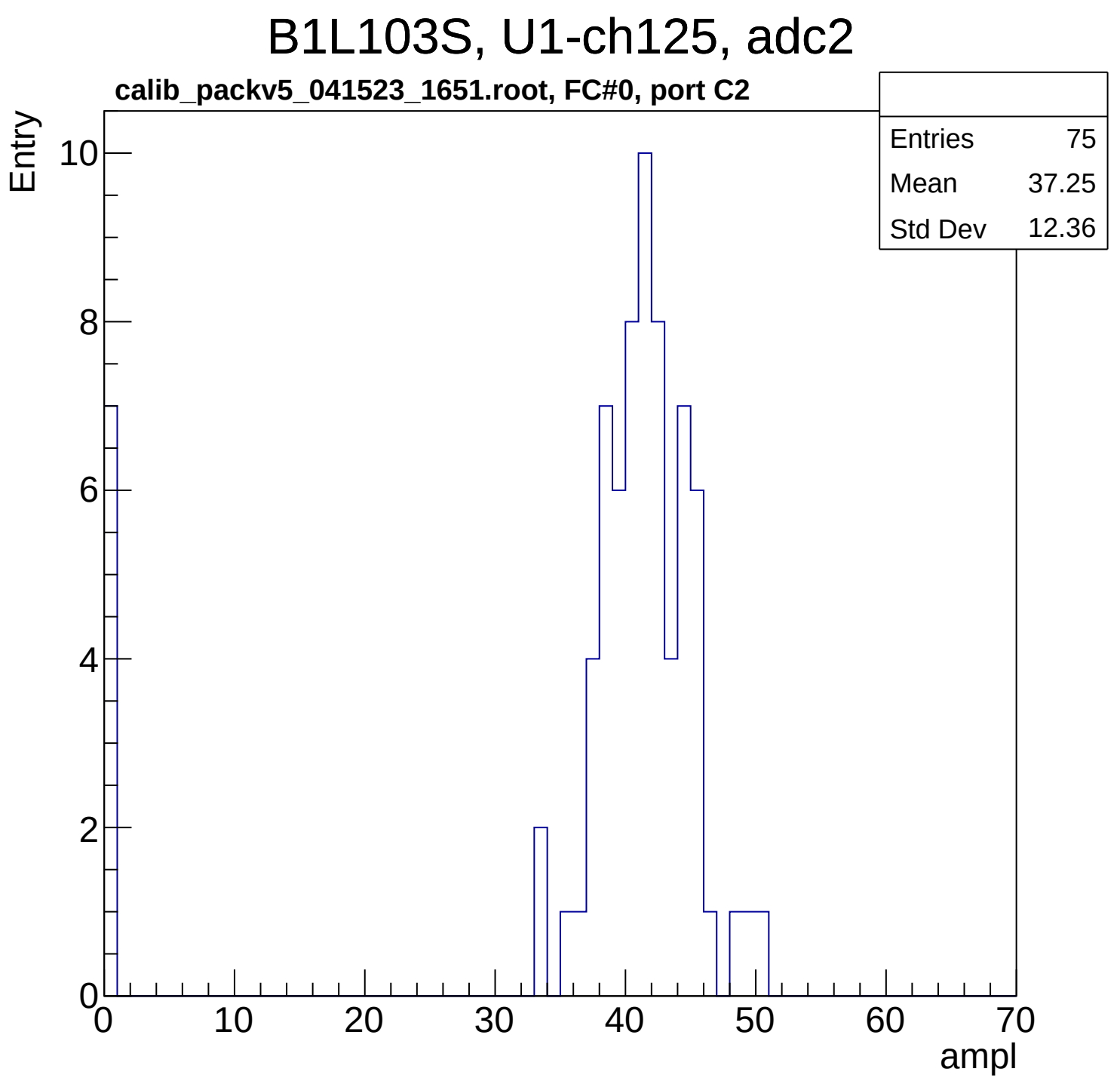
B1L103S, U1-ch125, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 37.25
Std Dev 12.36
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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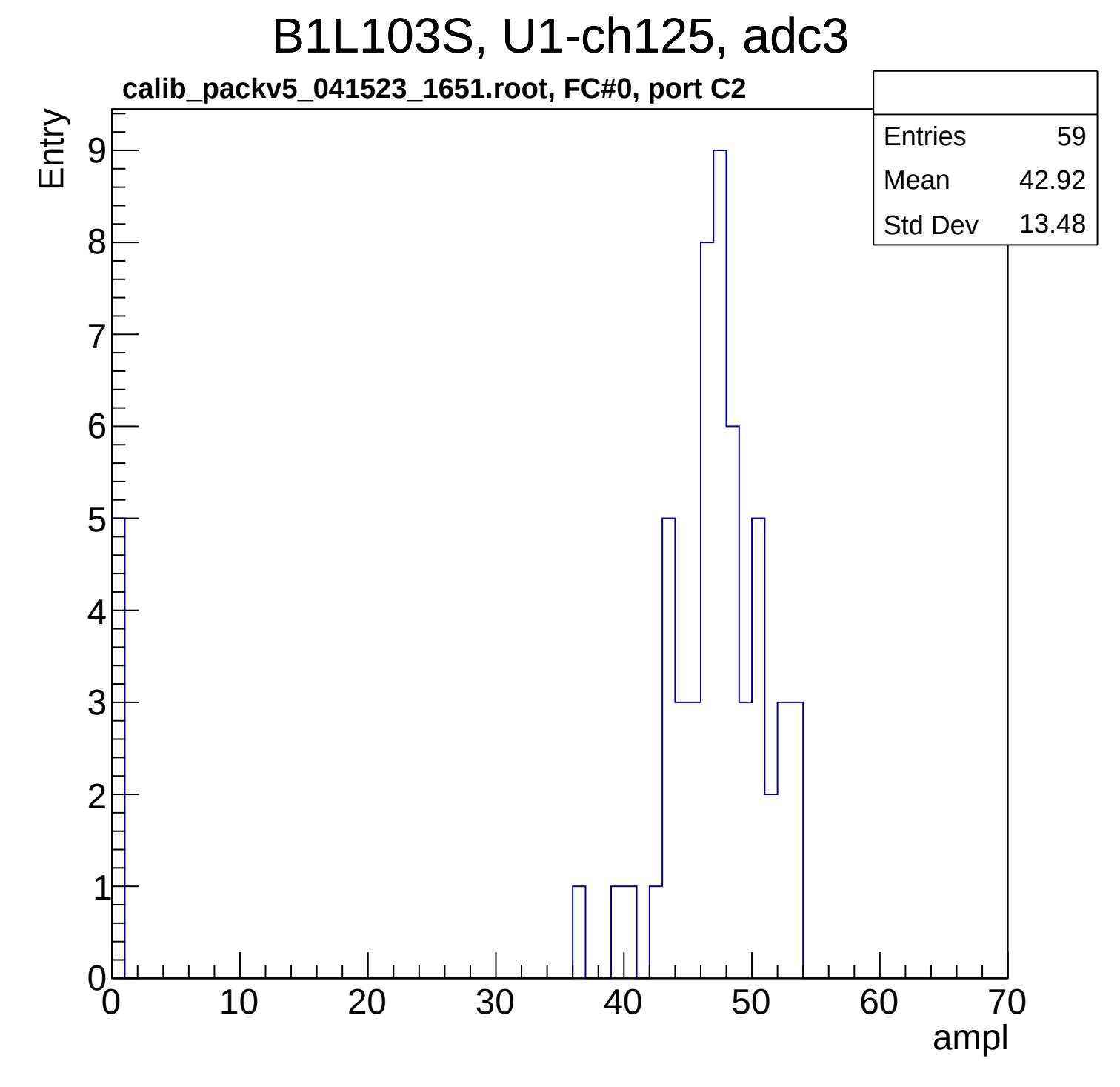
B1L103S, U1-ch125, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 42.92
Std Dev 13.48
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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40
50
60
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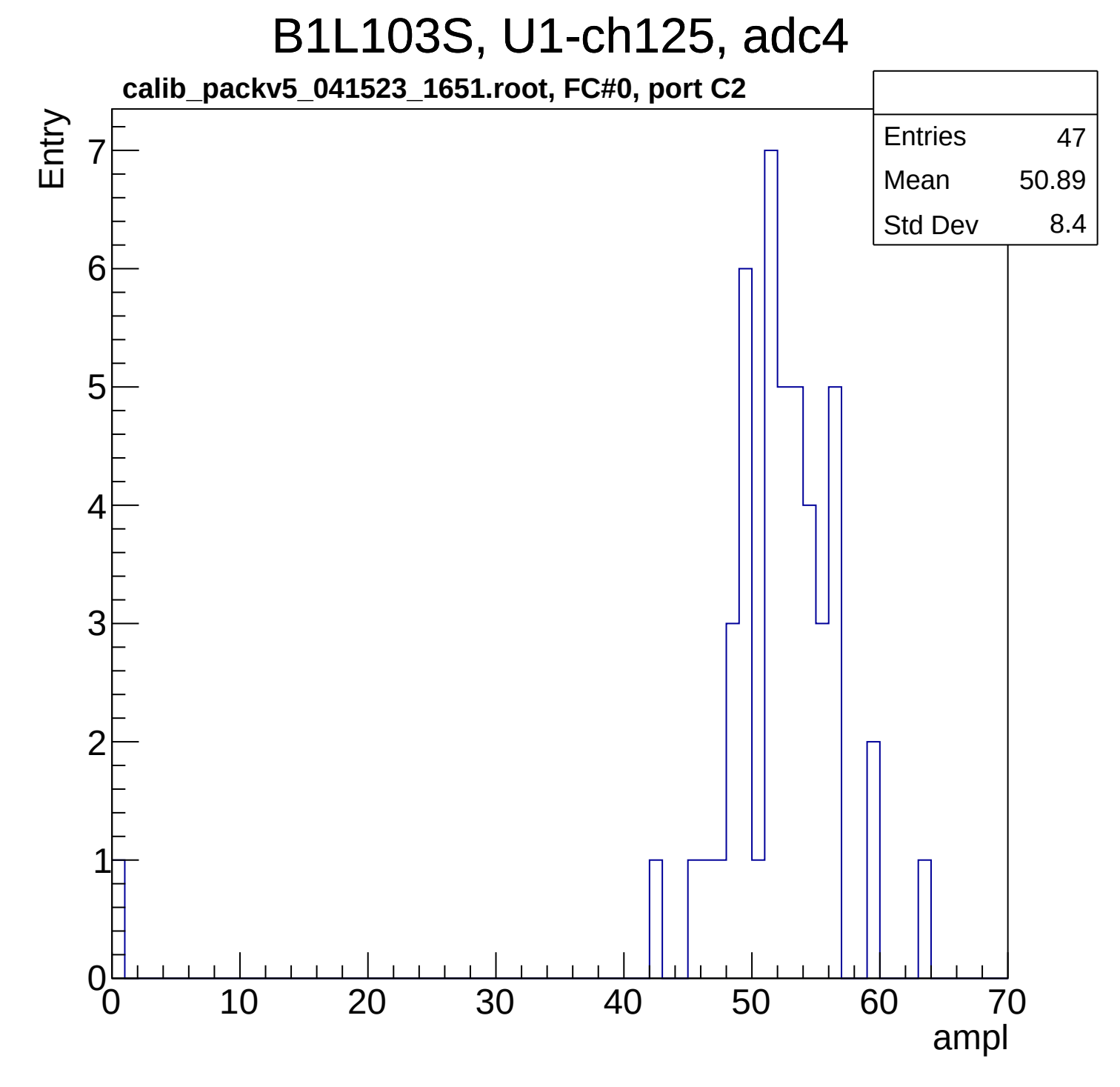
B1L103S, U1-ch125, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 50.89
Std Dev 8.4
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
30
40
50
60
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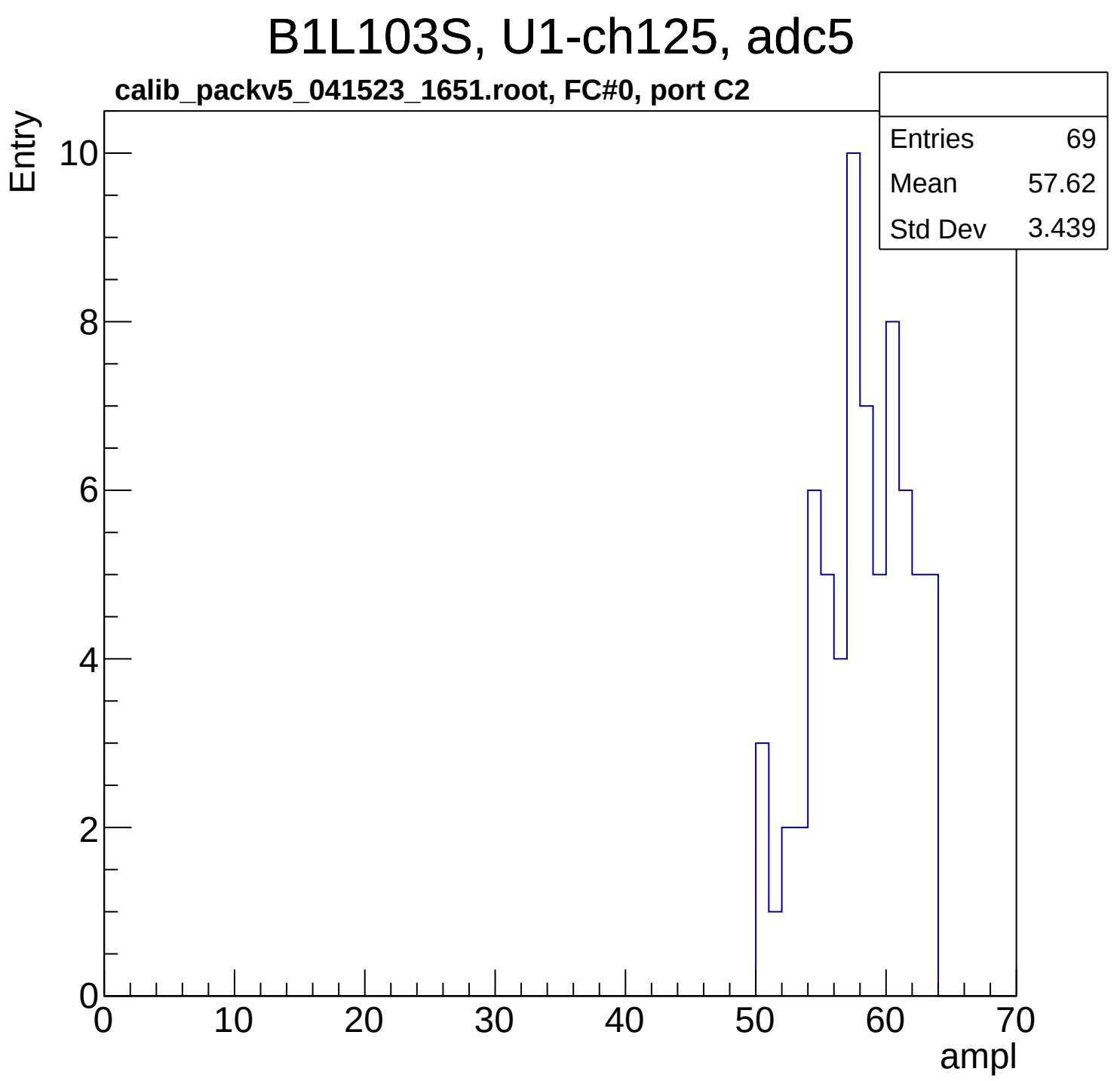
B1L103S, U1-ch125, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 57.62
Std Dev 3.439
Entry
ampl
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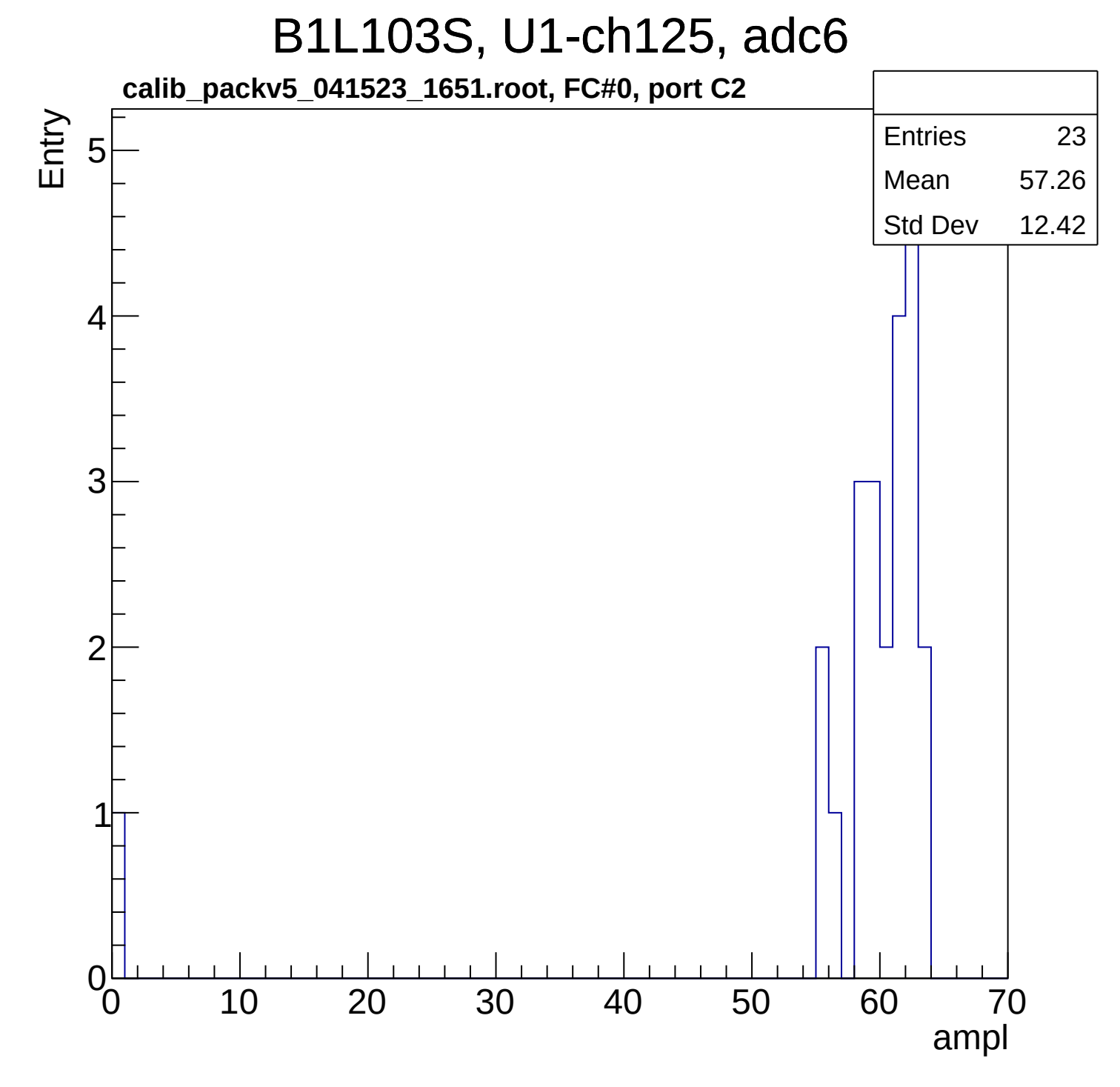
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U1-ch125, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 23
Mean 57.26
Std Dev 12.42
Entry
ampl
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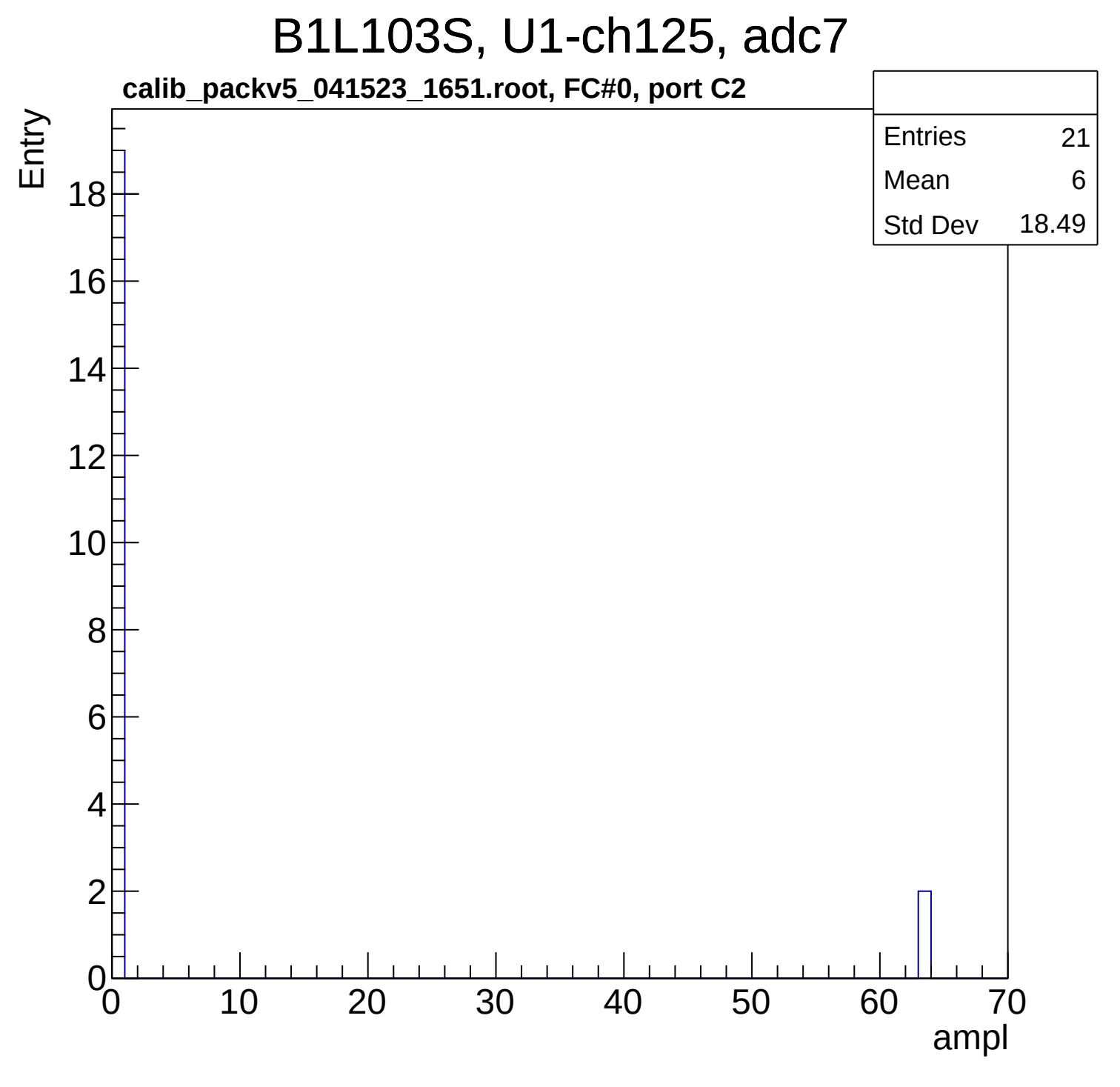
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U1-ch125, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 6
Std Dev 18.49
Entry
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6
8
10
12
14
16
18
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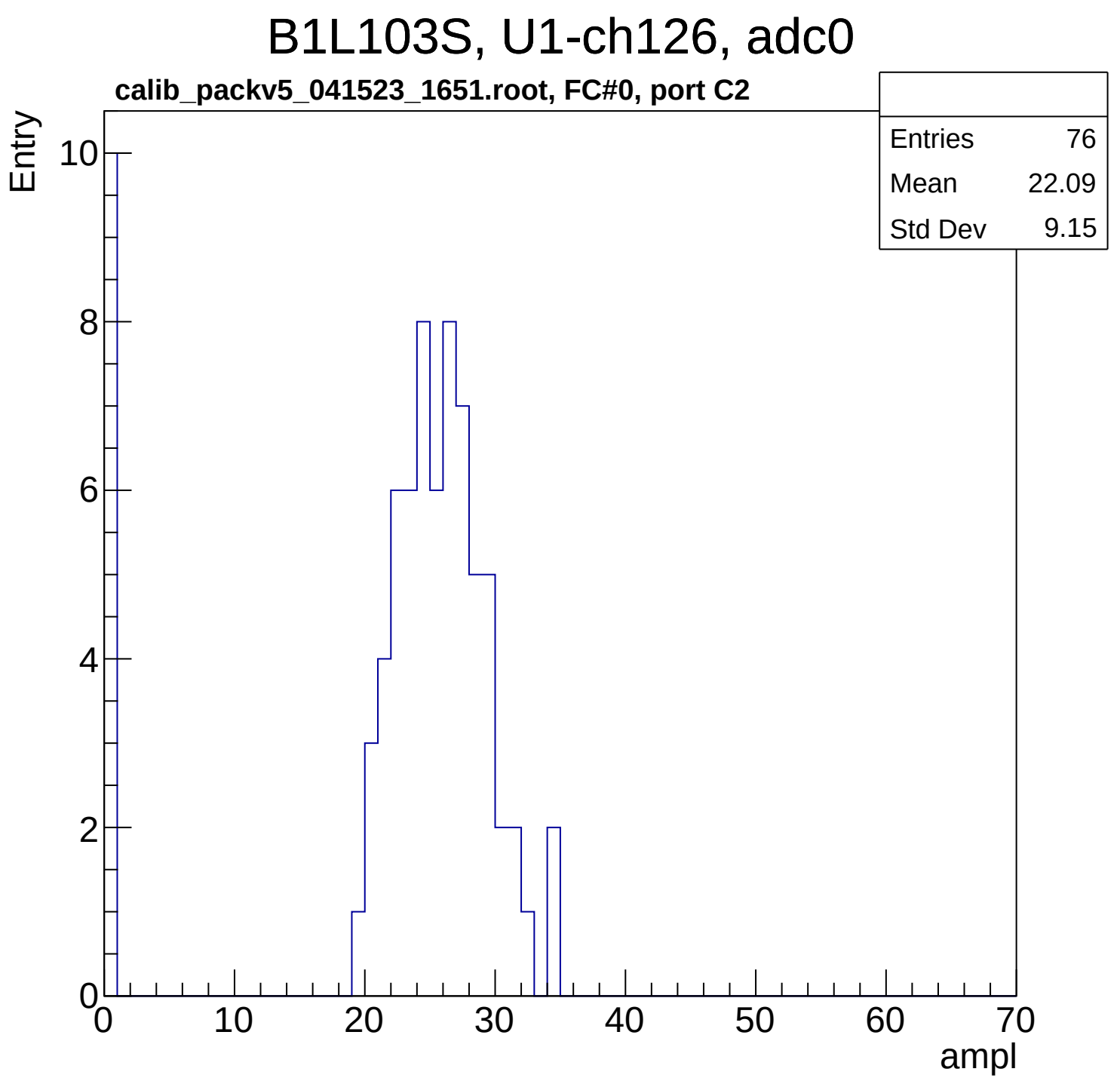
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch126, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 22.09
Std Dev 9.15
Entry
ampl
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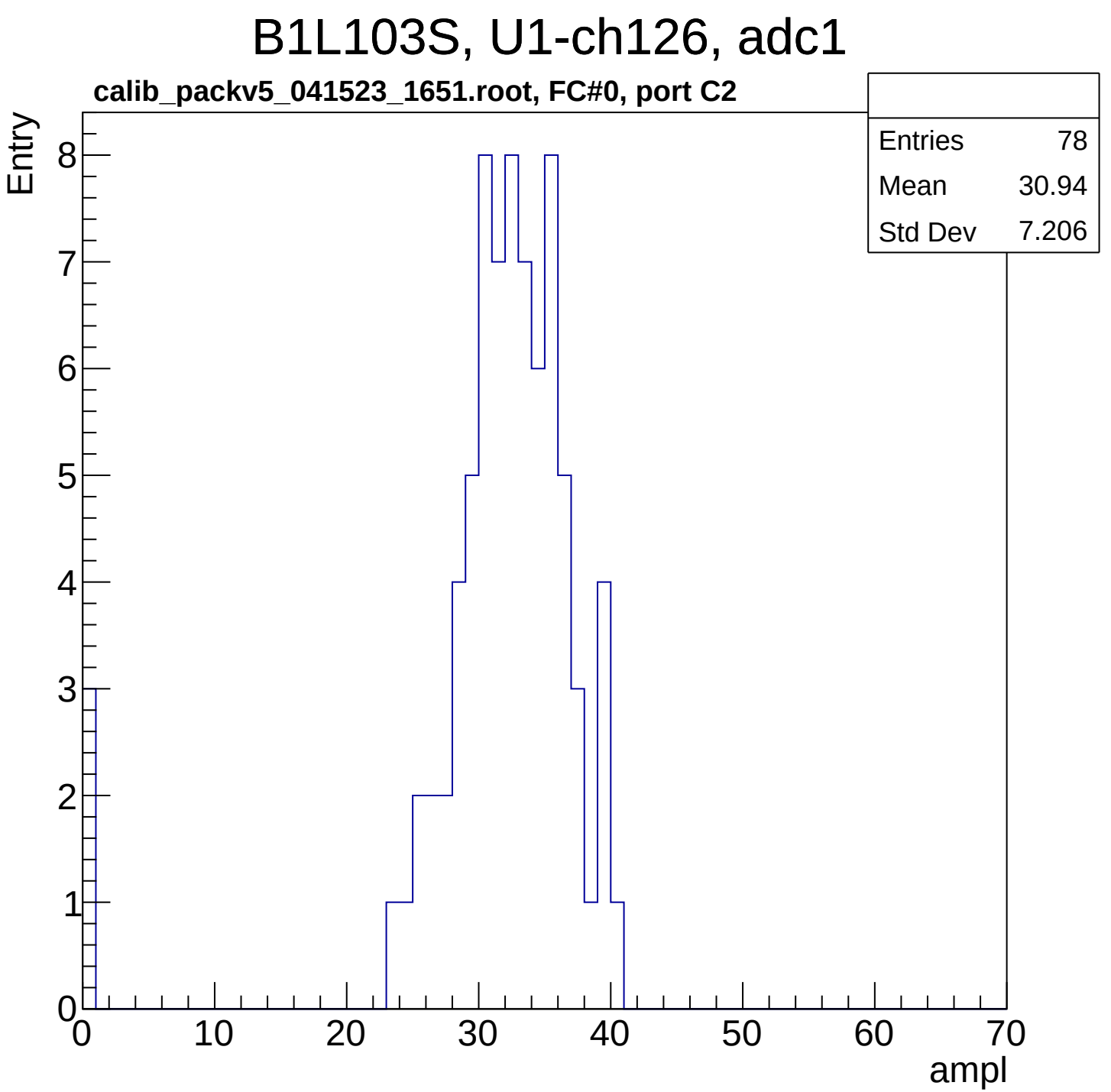
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U1-ch126, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 30.94
Std Dev 7.206
Entry
ampl
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2
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4
5
6
7
8
0
10
20
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40
50
60
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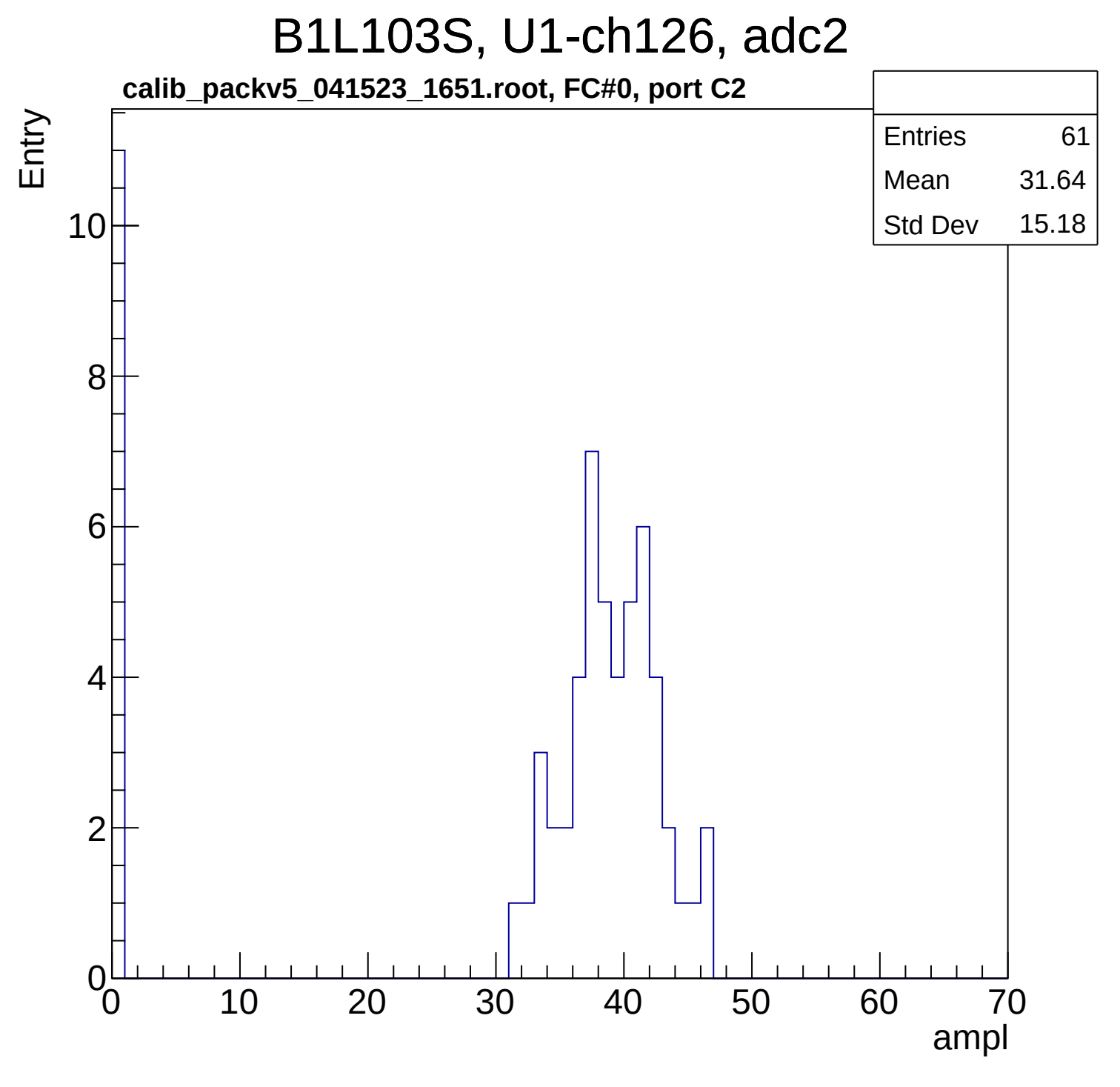
B1L103S, U1-ch126, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 31.64
Std Dev 15.18
Entry
0
2
4
6
8
10
0
10
20
30
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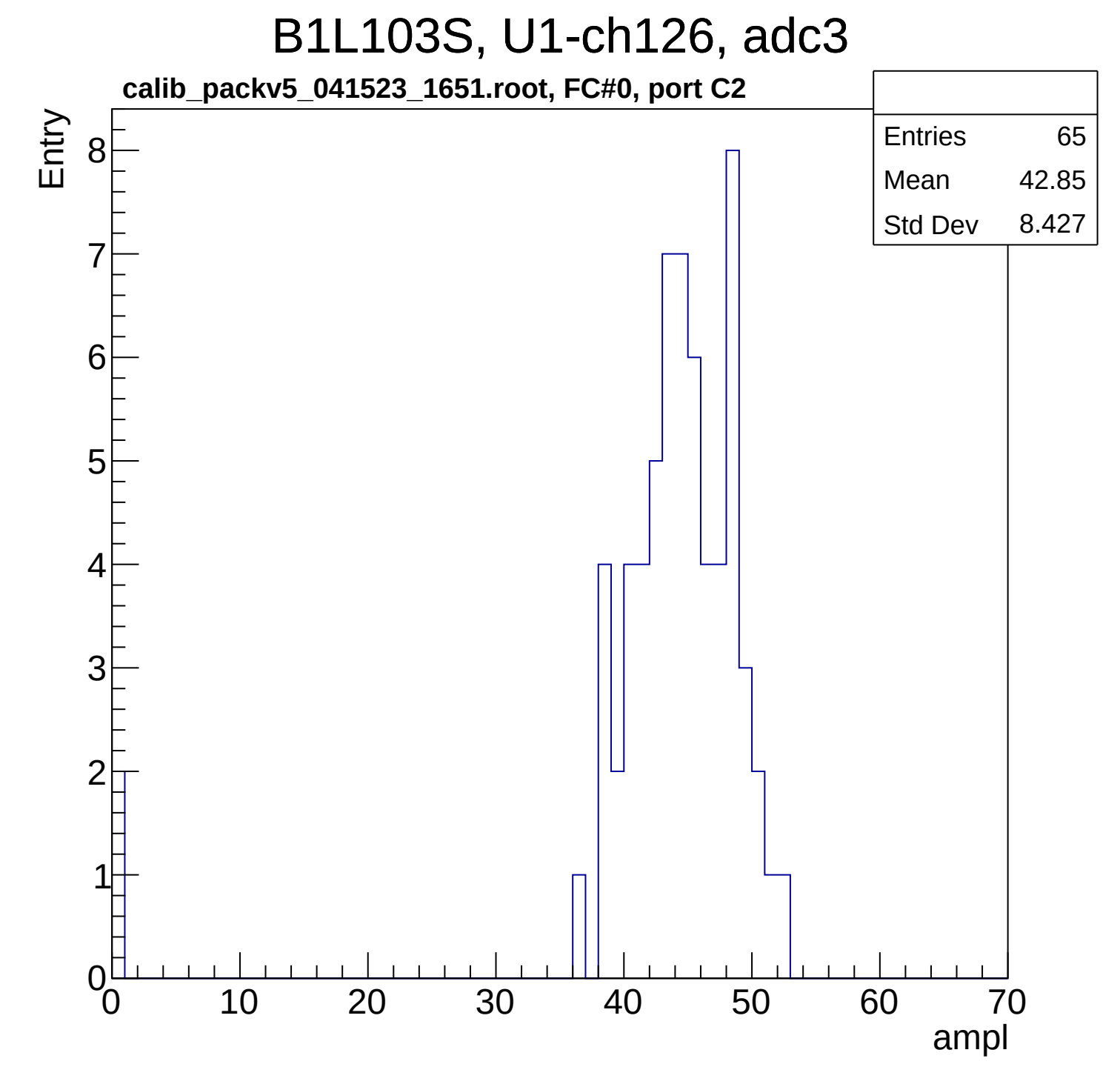
50
60
70
ampl


B1L103S, U1-ch126, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 42.85
Std Dev 8.427
Entry
ampl
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3
4
5
6
7
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0
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40
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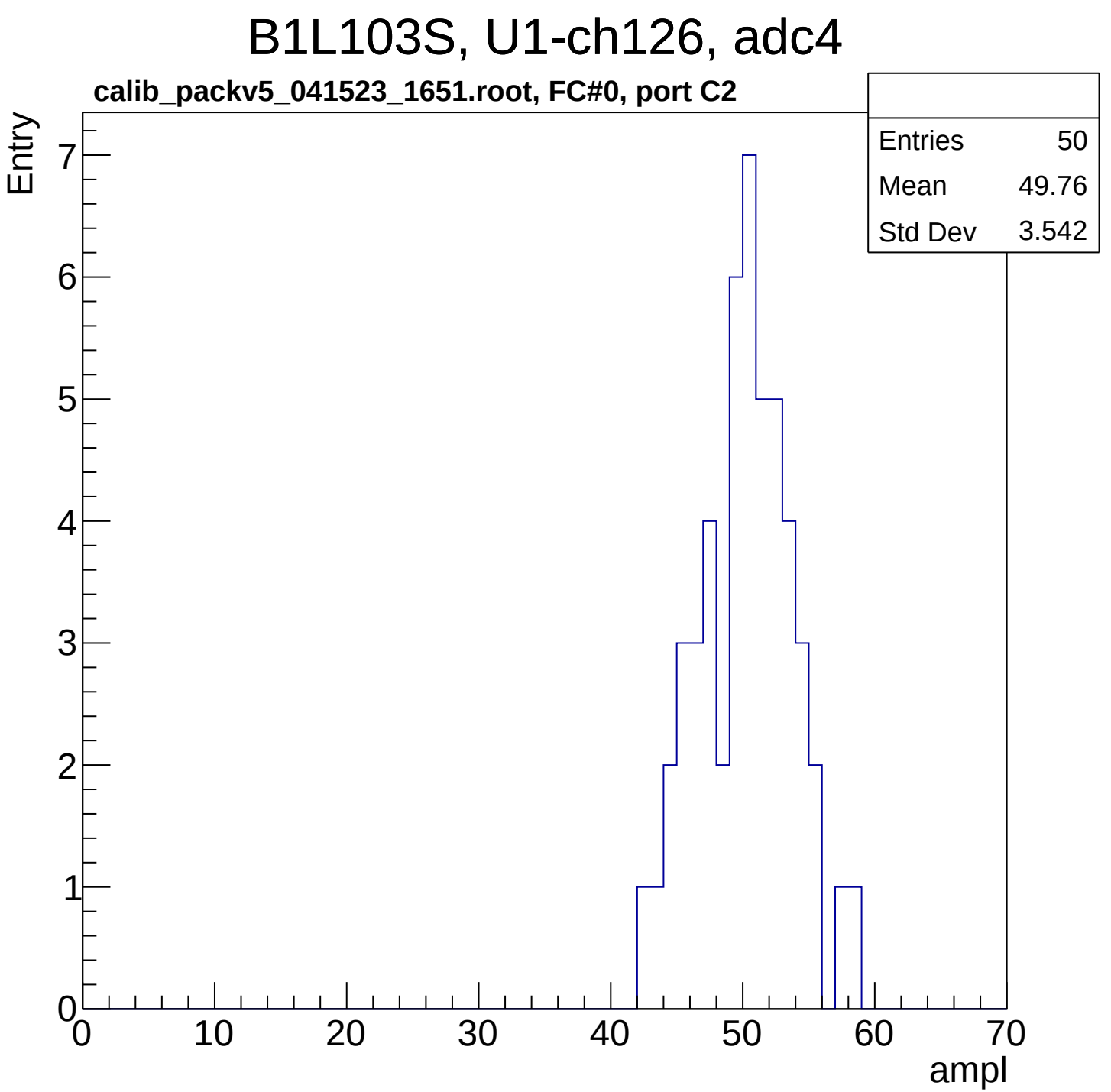
60
70


B1L103S, U1-ch126, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 49.76
Std Dev 3.542
Entry
ampl
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4
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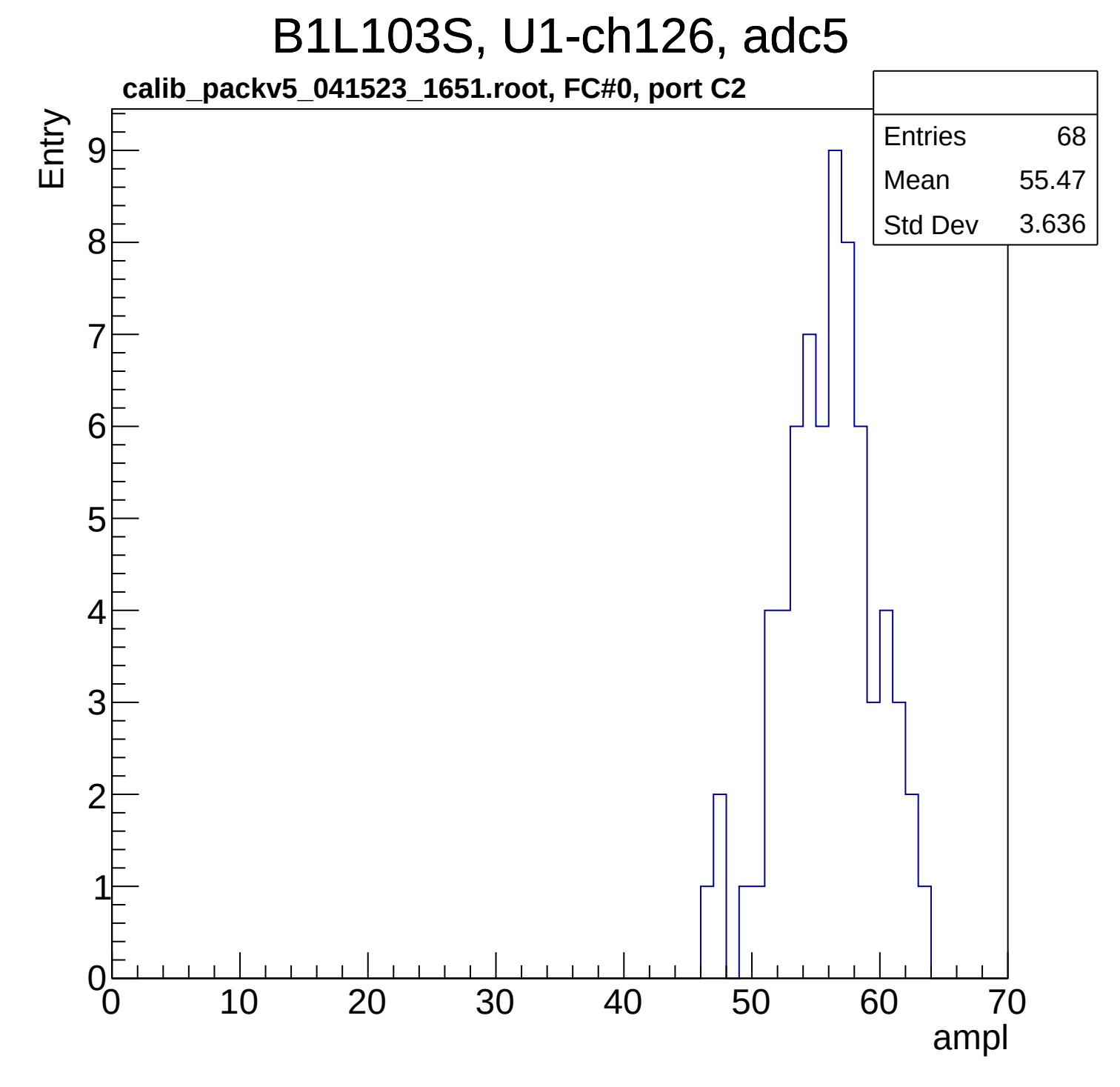
B1L103S, U1-ch126, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 55.47
Std Dev 3.636
Entry
ampl
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2
3
4
5
6
7
8
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0
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40
50
60
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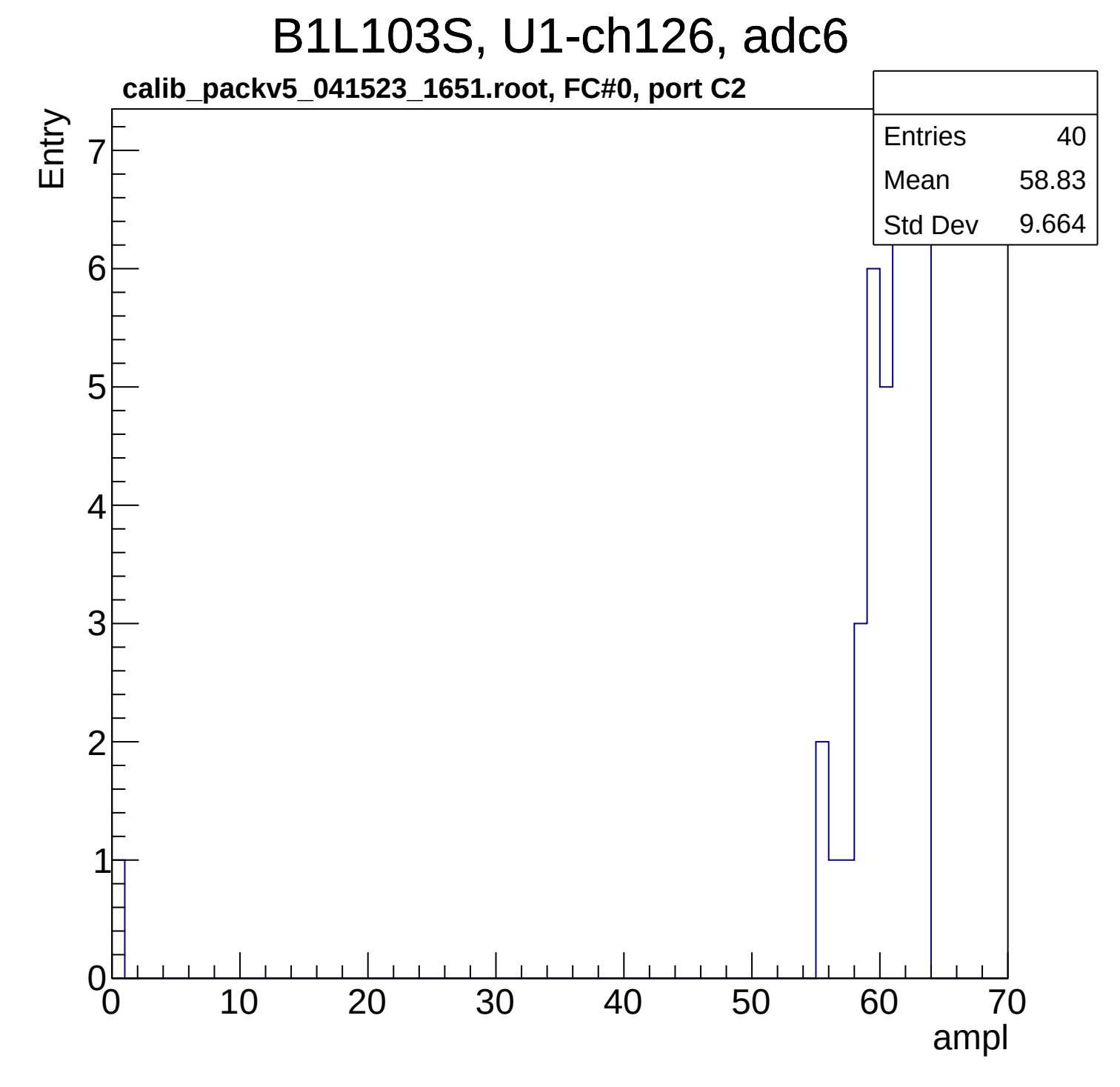
B1L103S, U1-ch126, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 40
Mean 58.83
Std Dev 9.664
Entry
ampl
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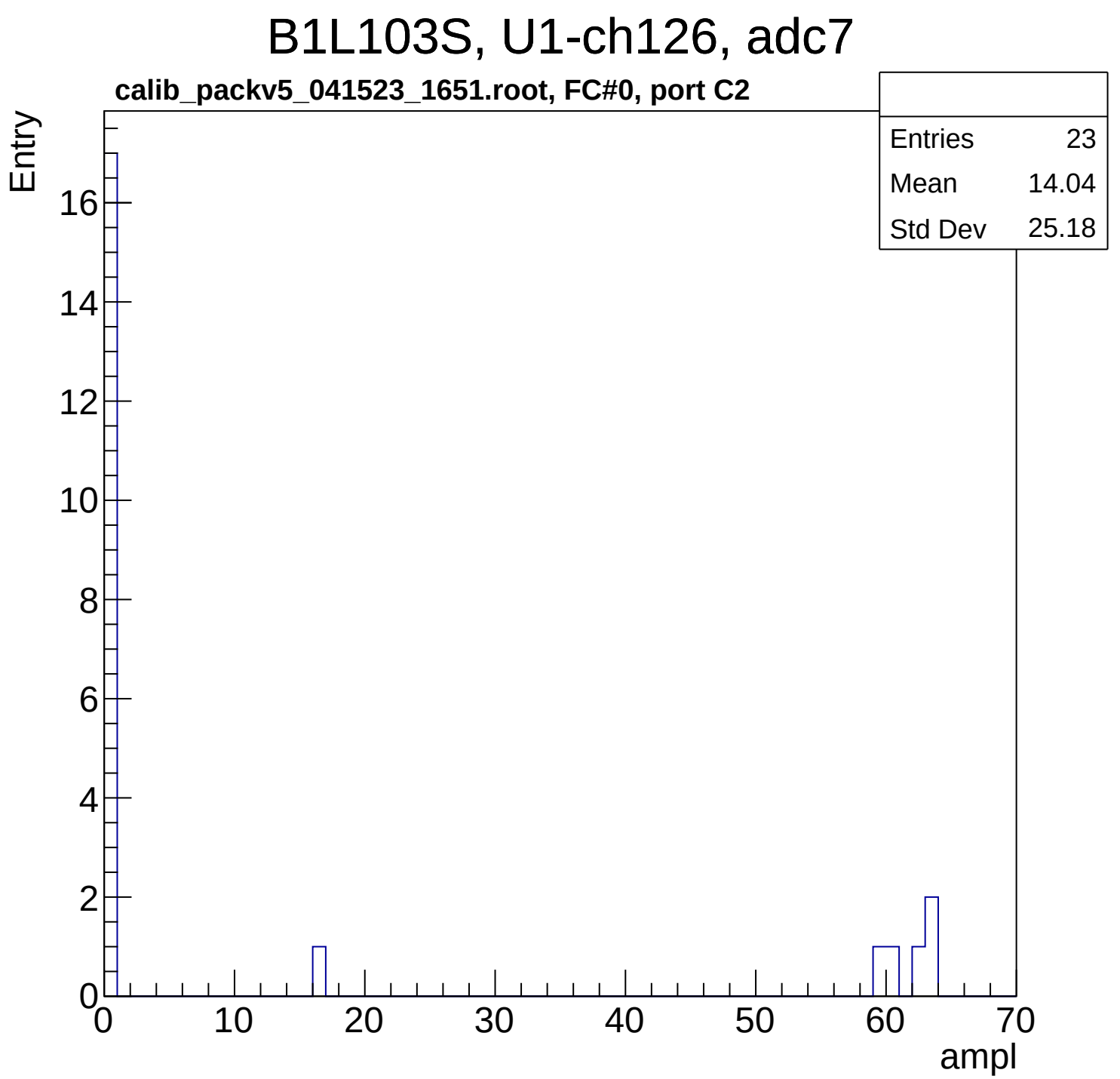
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U1-ch126, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 23
Mean 14.04
Std Dev 25.18
Entry
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8
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12
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30
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50
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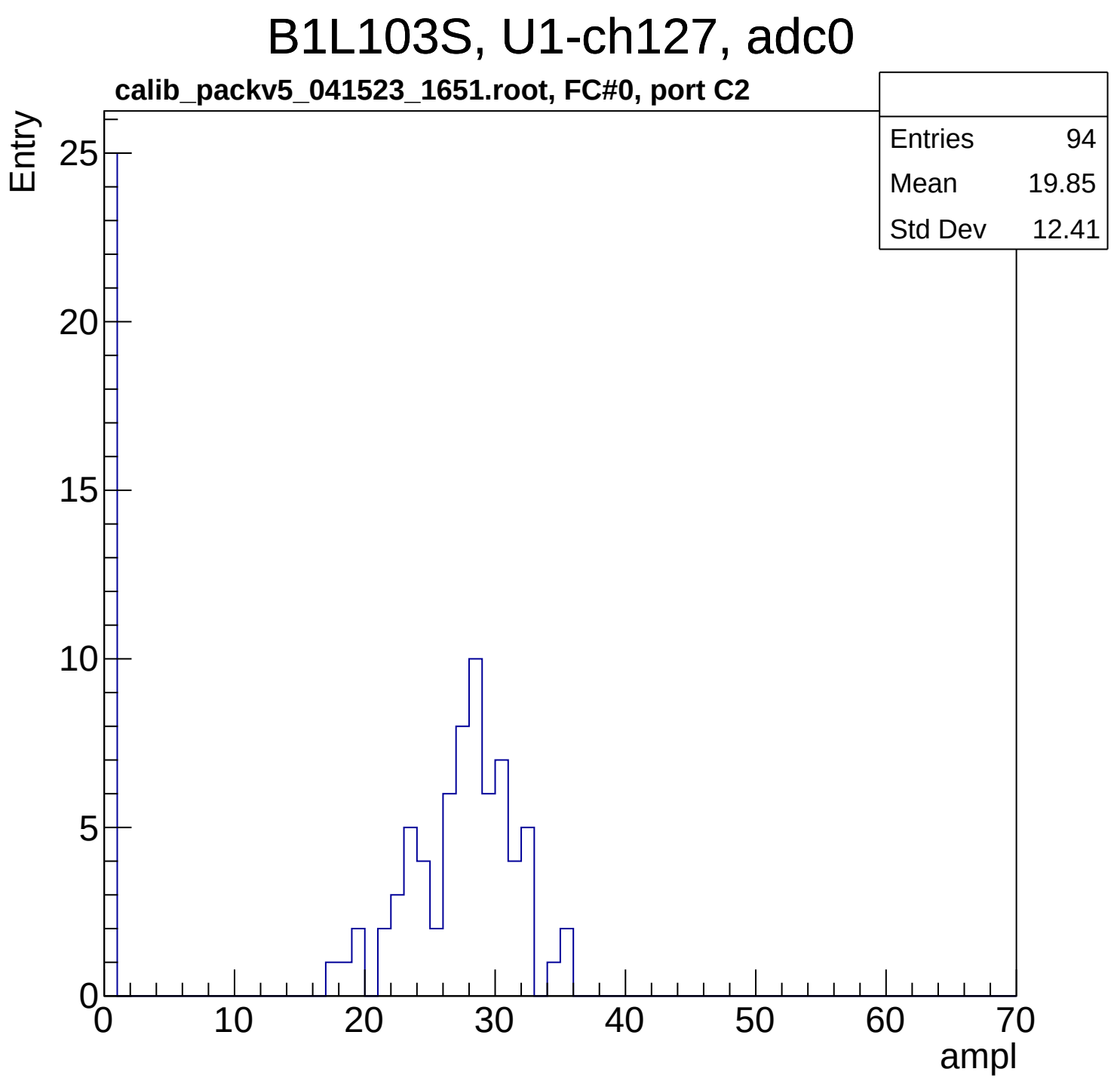
70
ampl


B1L103S, U1-ch127, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 94
Mean 19.85
Std Dev 12.41
Entry
ampl
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5
10
15
20
25
0
10
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40
50
60
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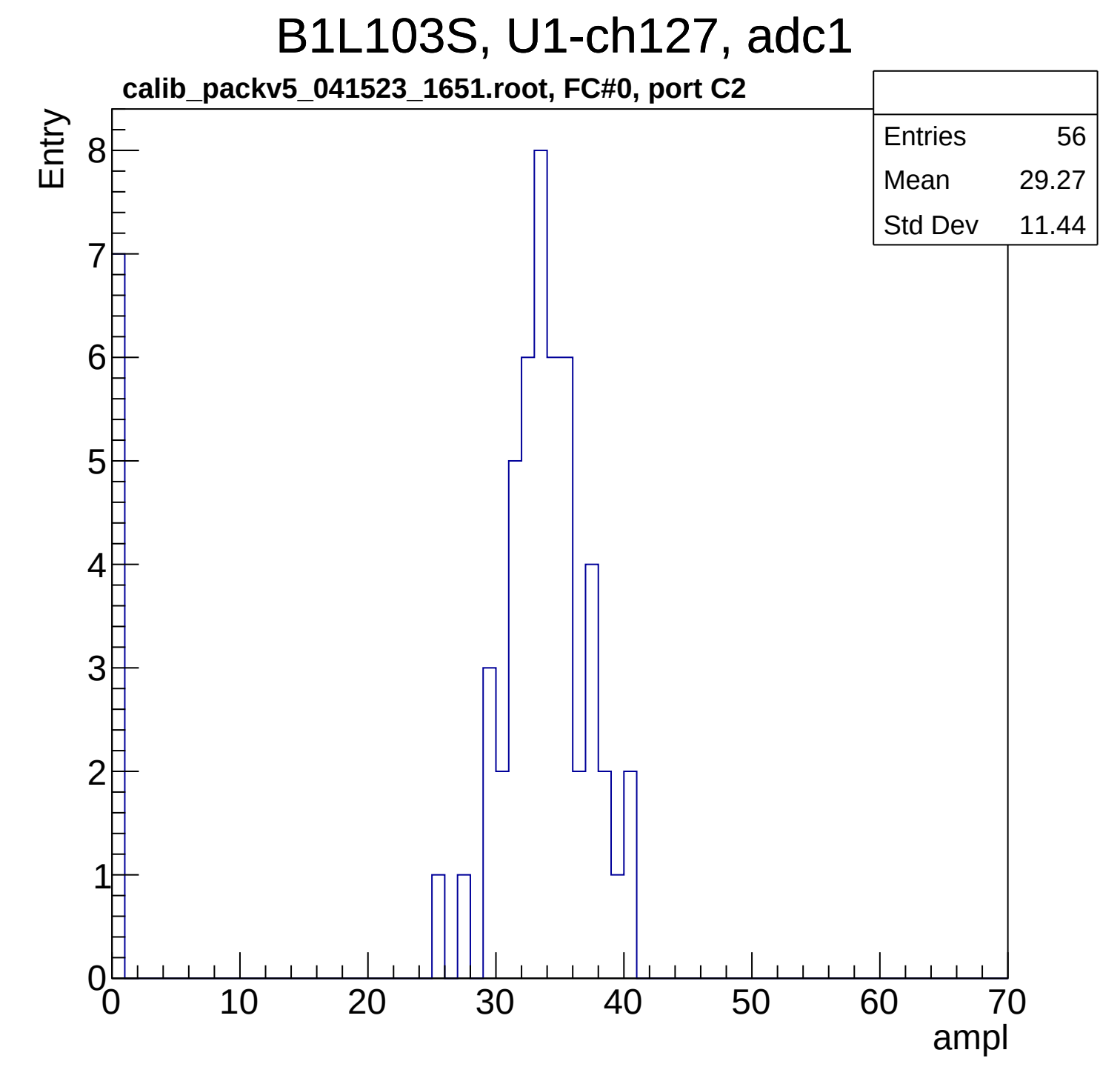
B1L103S, U1-ch127, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 29.27
Std Dev 11.44
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
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60
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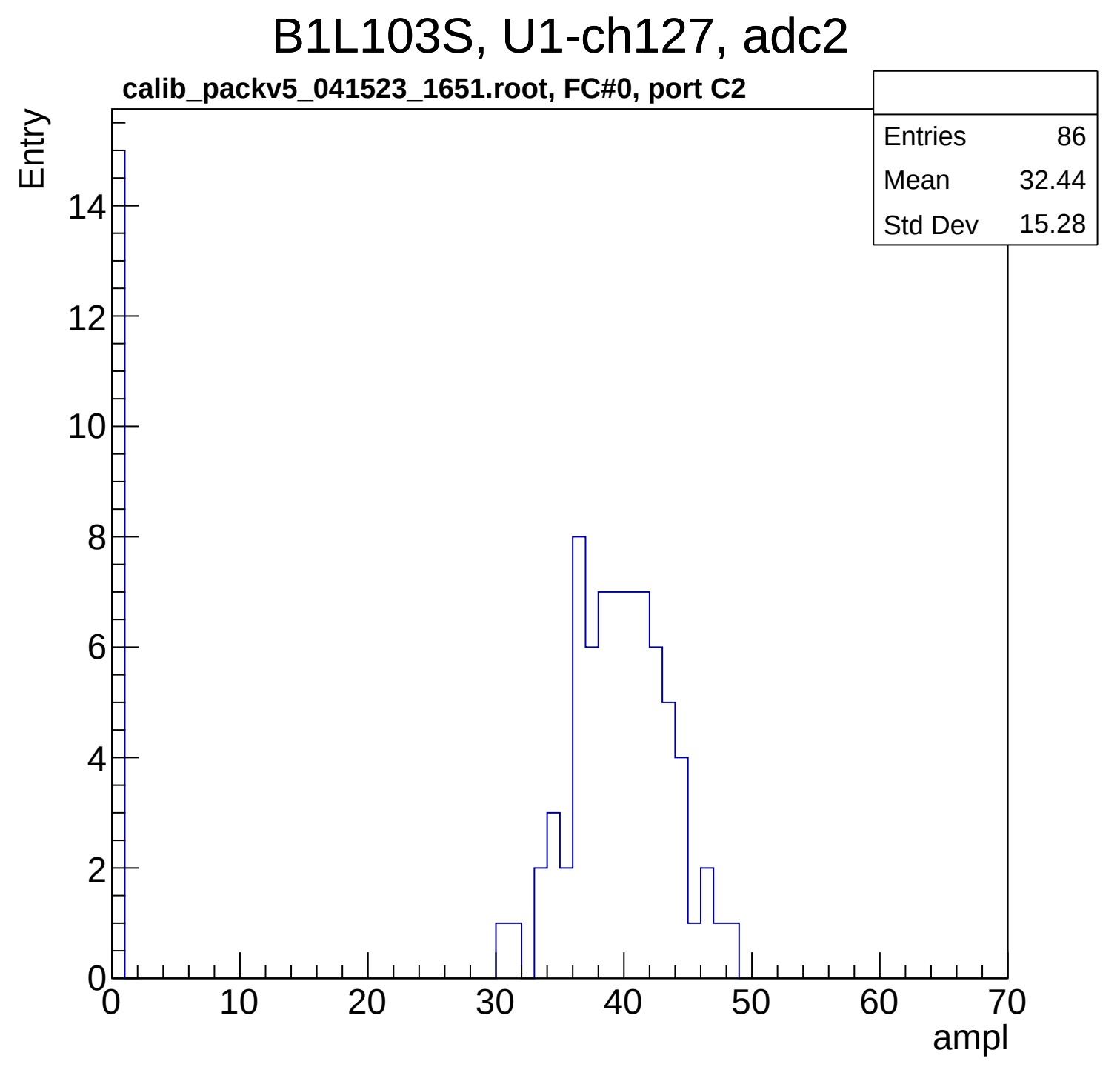
B1L103S, U1-ch127, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 32.44
Std Dev 15.28
Entry
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2
4
6
8
10
12
14
0
10
20
30
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50
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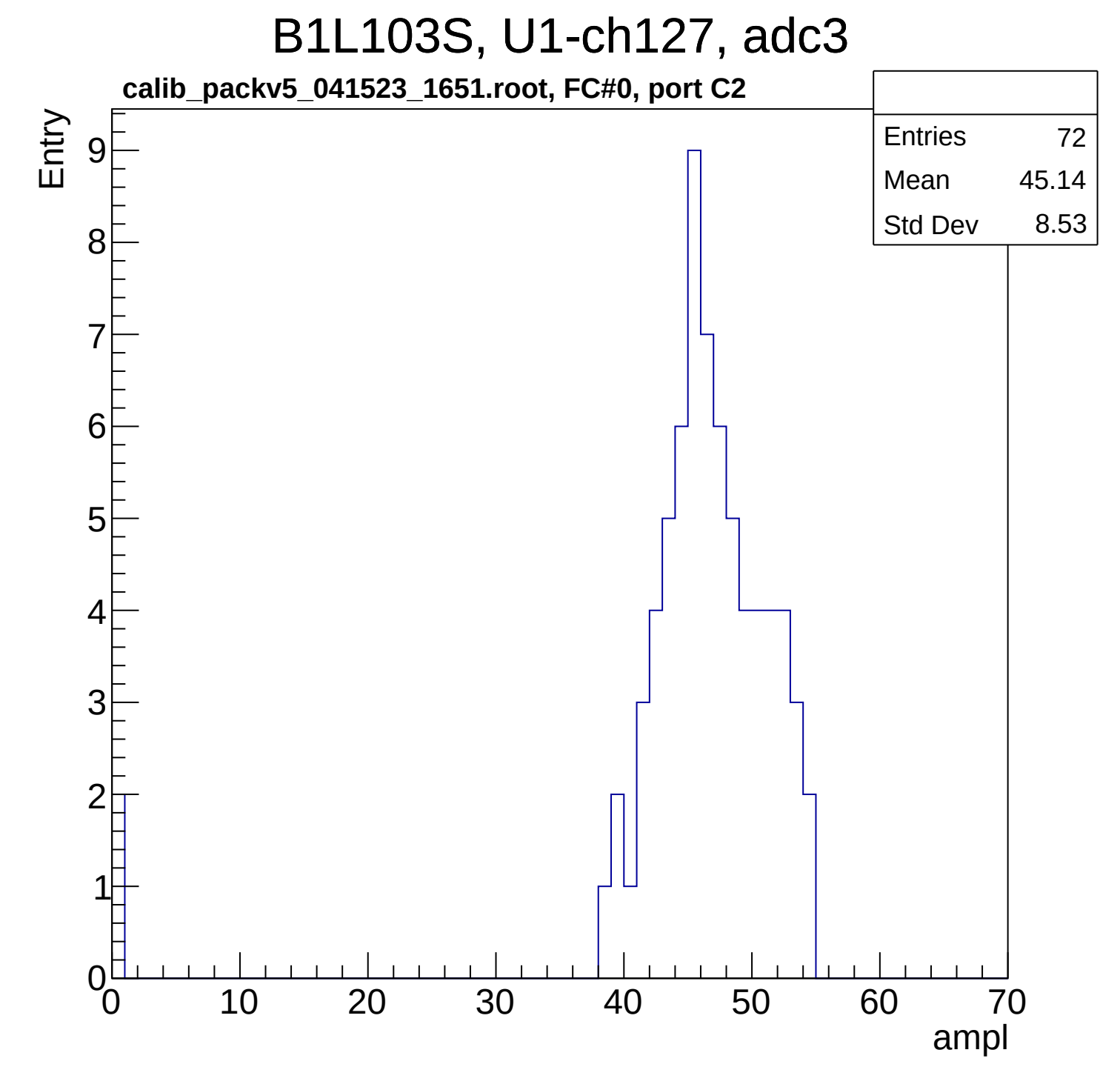
70
ampl


B1L103S, U1-ch127, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 45.14
Std Dev 8.53
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
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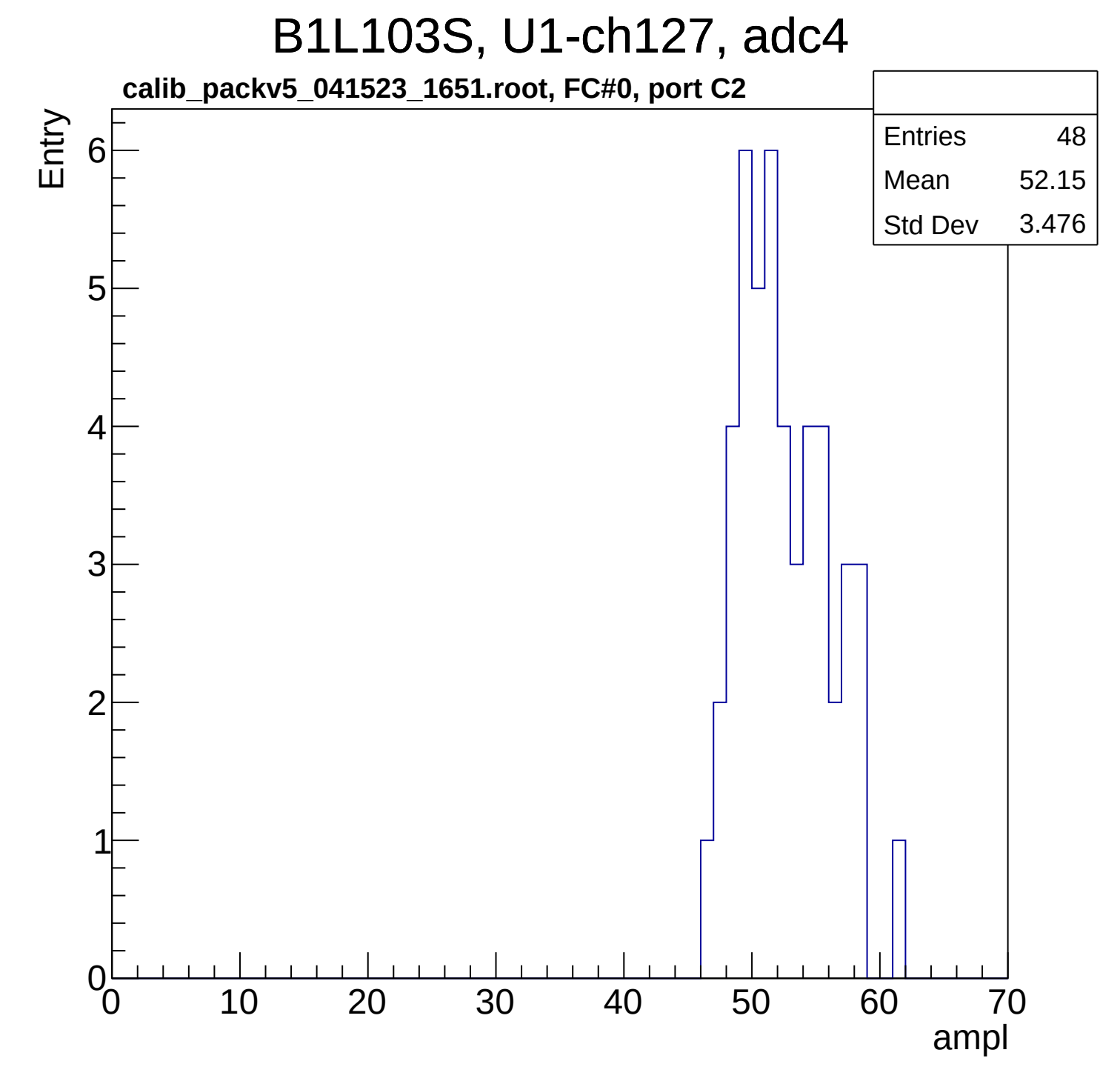
B1L103S, U1-ch127, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 52.15
Std Dev 3.476
Entry
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2
3
4
5
6
0
10
20
30
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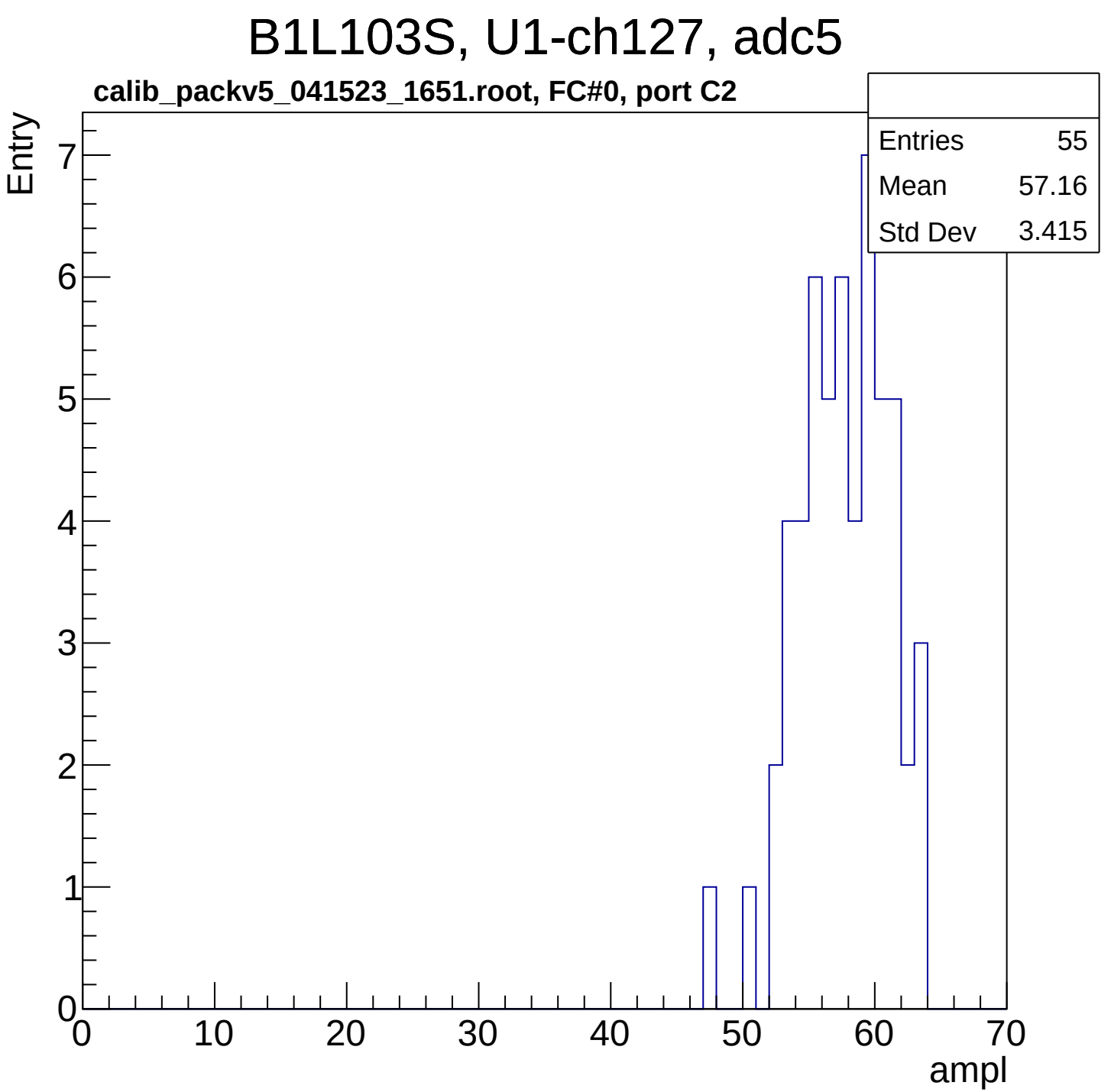
50
60
70
ampl


B1L103S, U1-ch127, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 57.16
Std Dev 3.415
Entry
ampl
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3
4
5
6
7
0
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20
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40
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60
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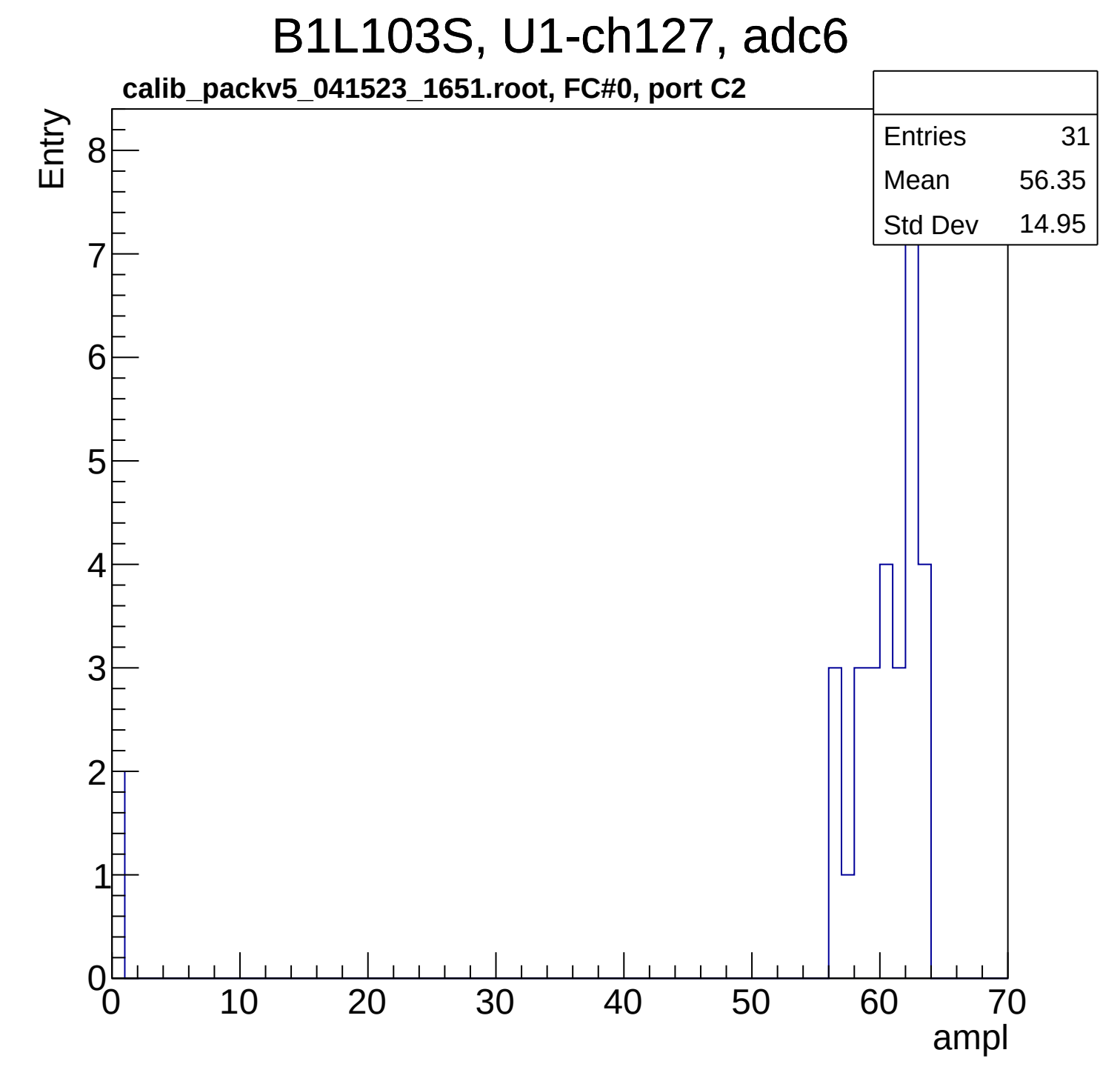
B1L103S, U1-ch127, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 31
Mean 56.35
Std Dev 14.95
Entry
ampl
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4
5
6
7
8
0
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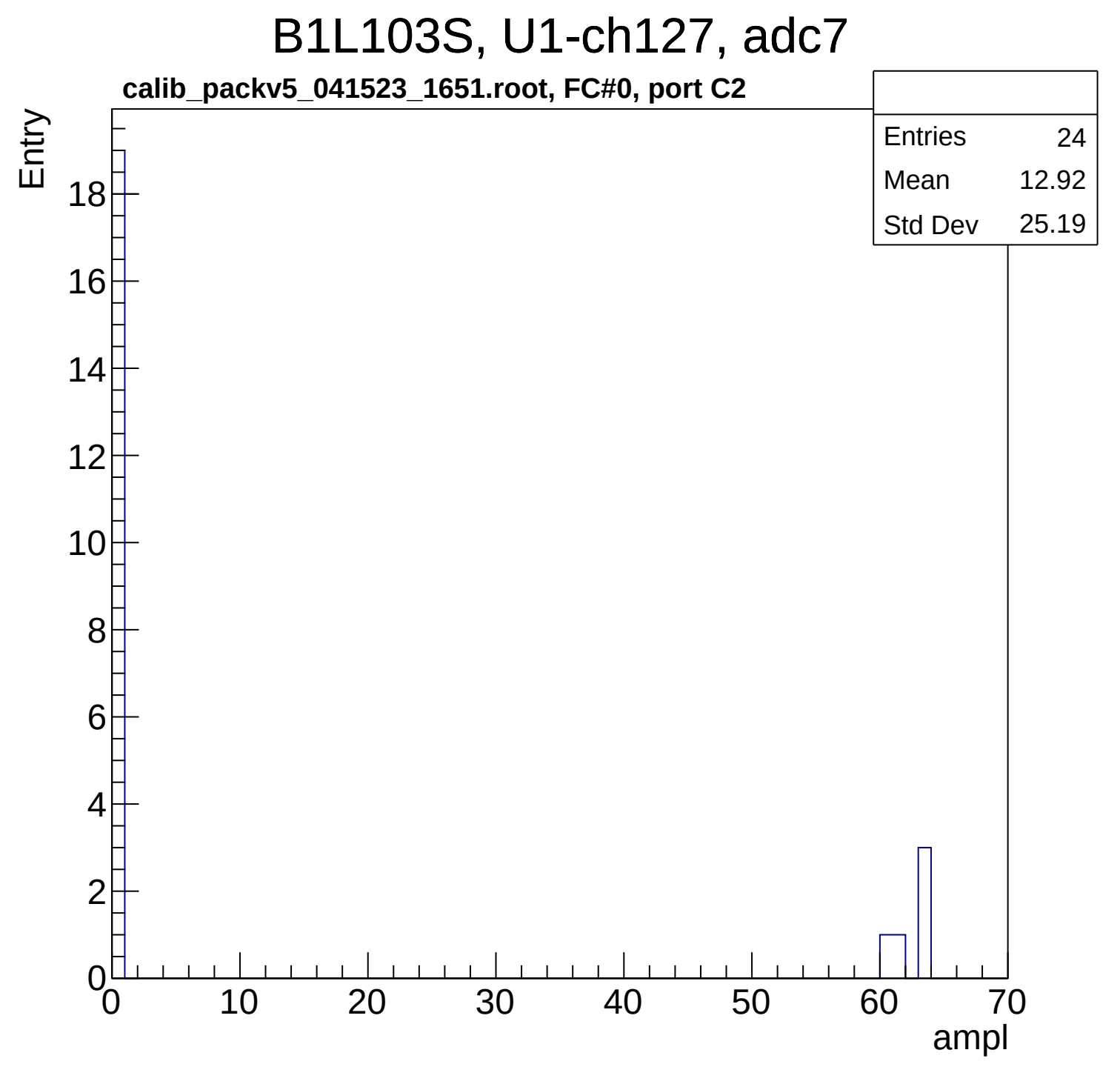
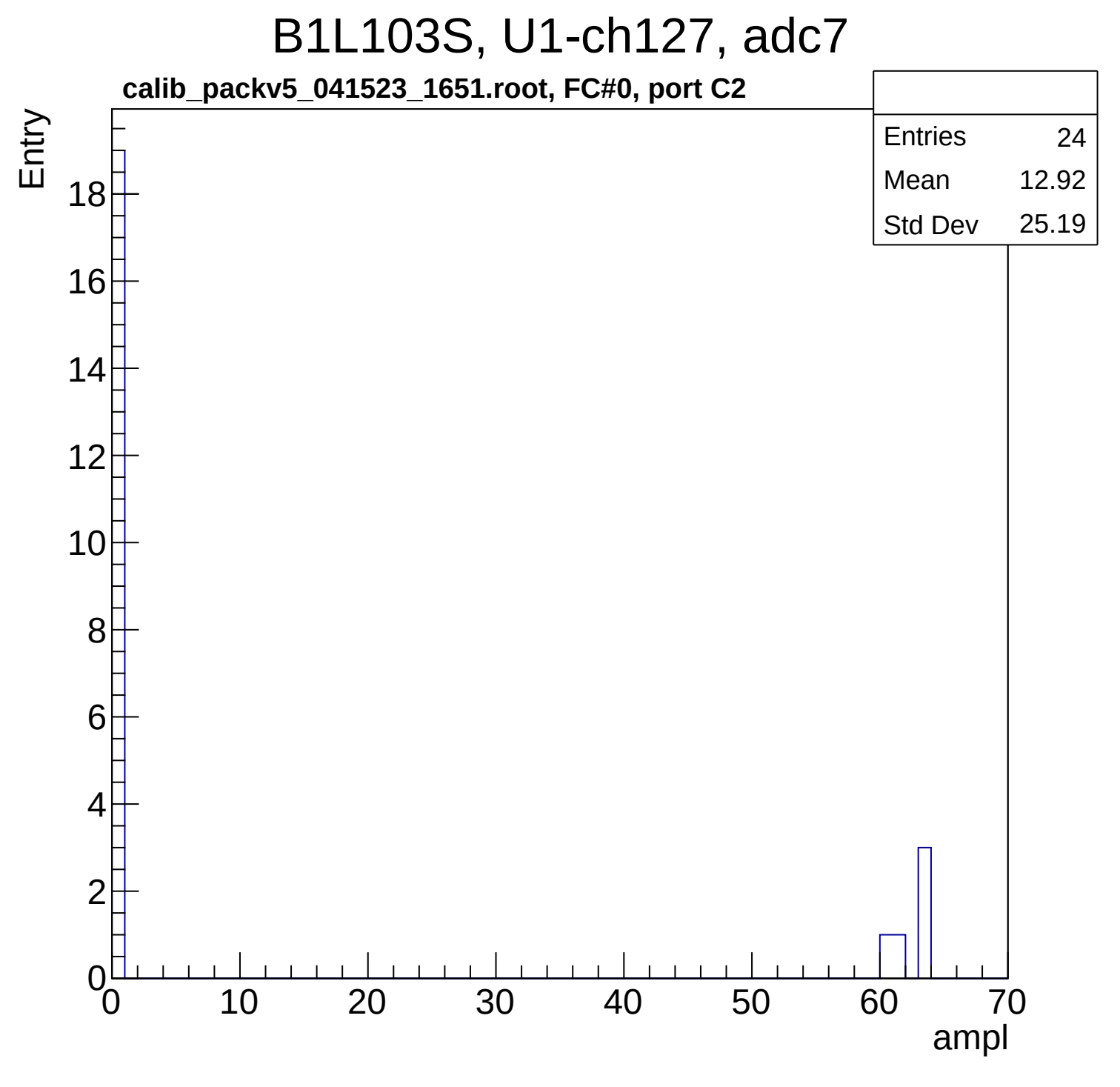

B1L103S, U1-ch127, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 24
Mean 12.92
Std Dev 25.19
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U1-ch127, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 24
Mean 12.92
Std Dev 25.19
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl