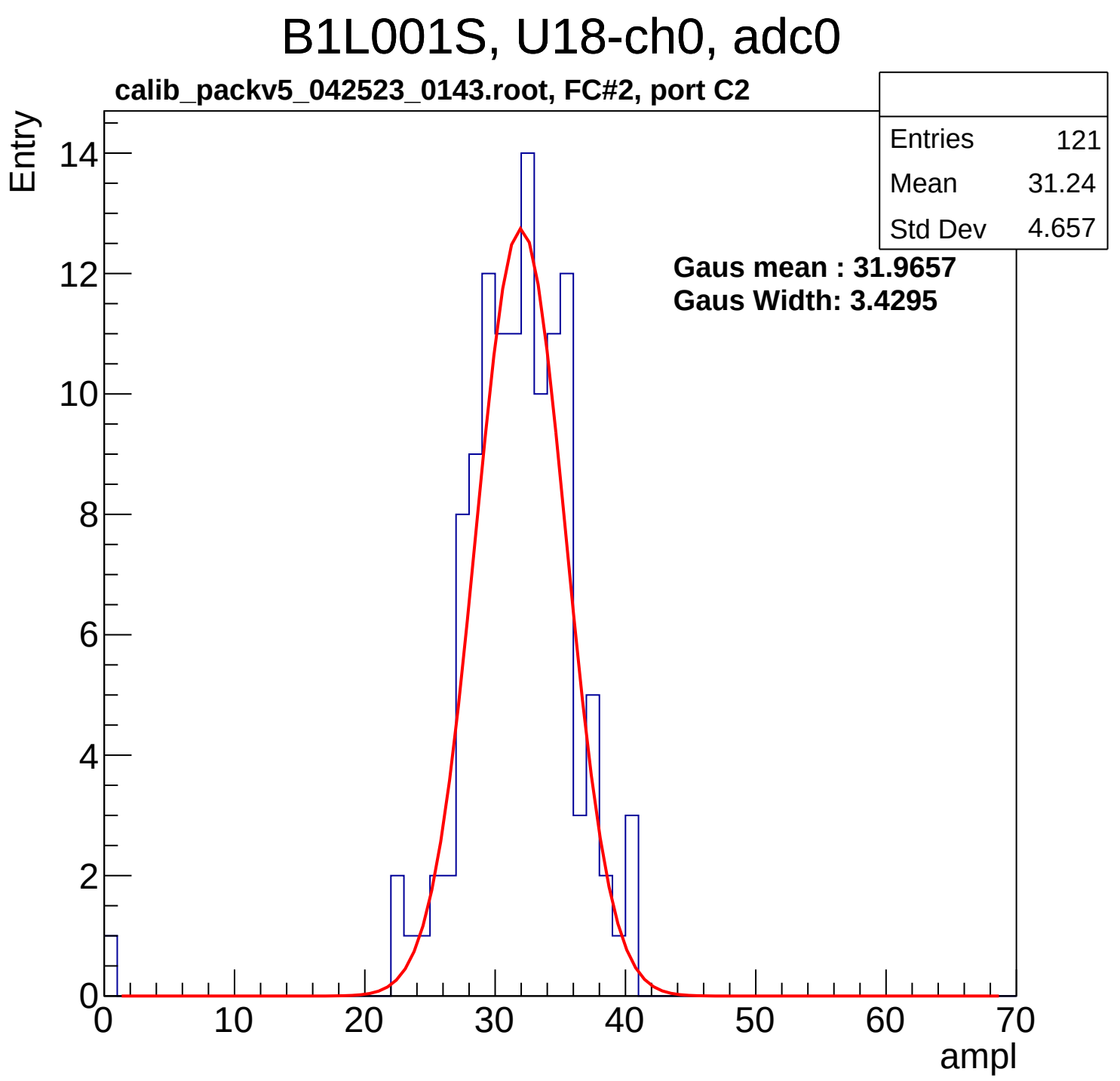
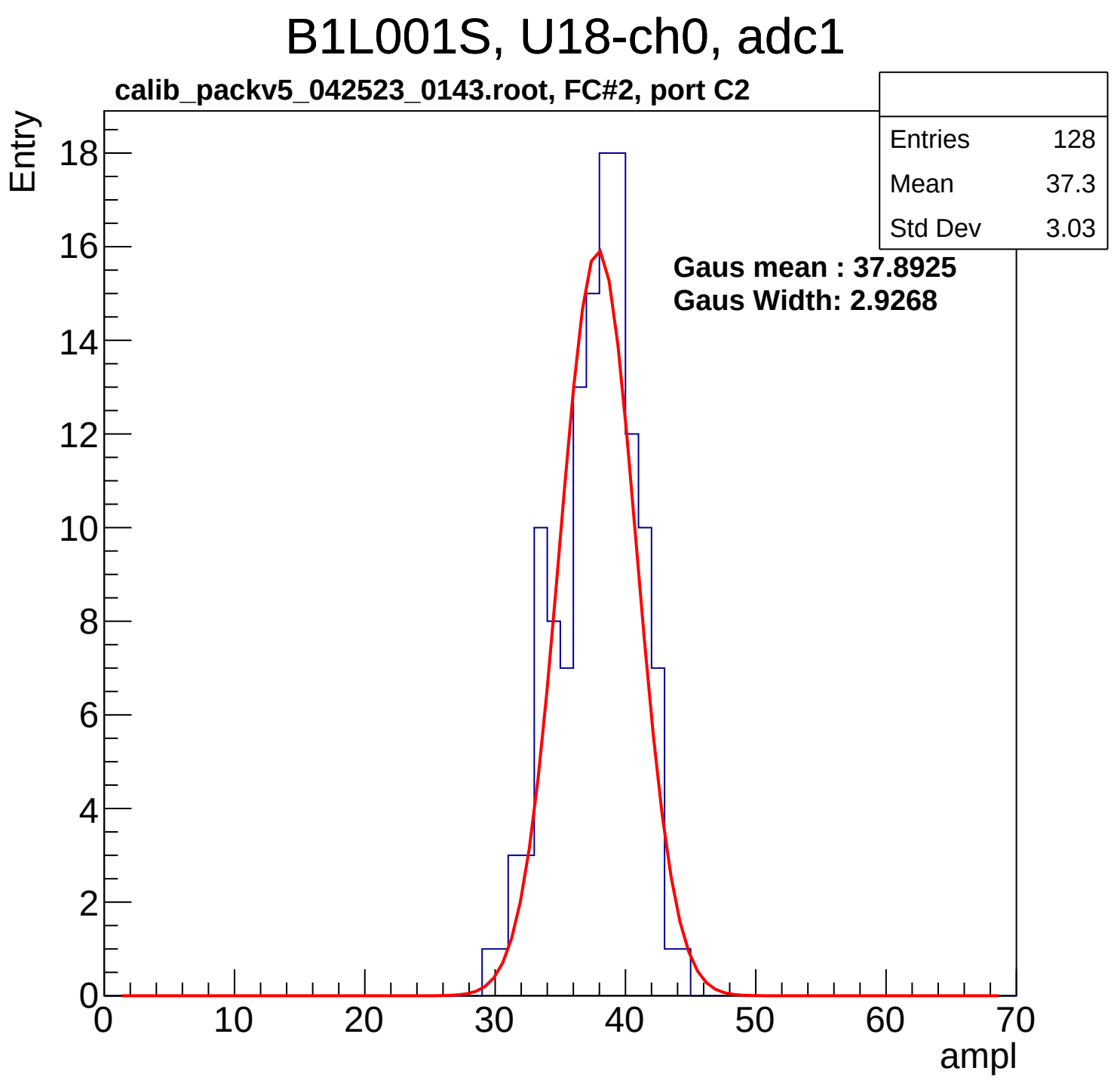
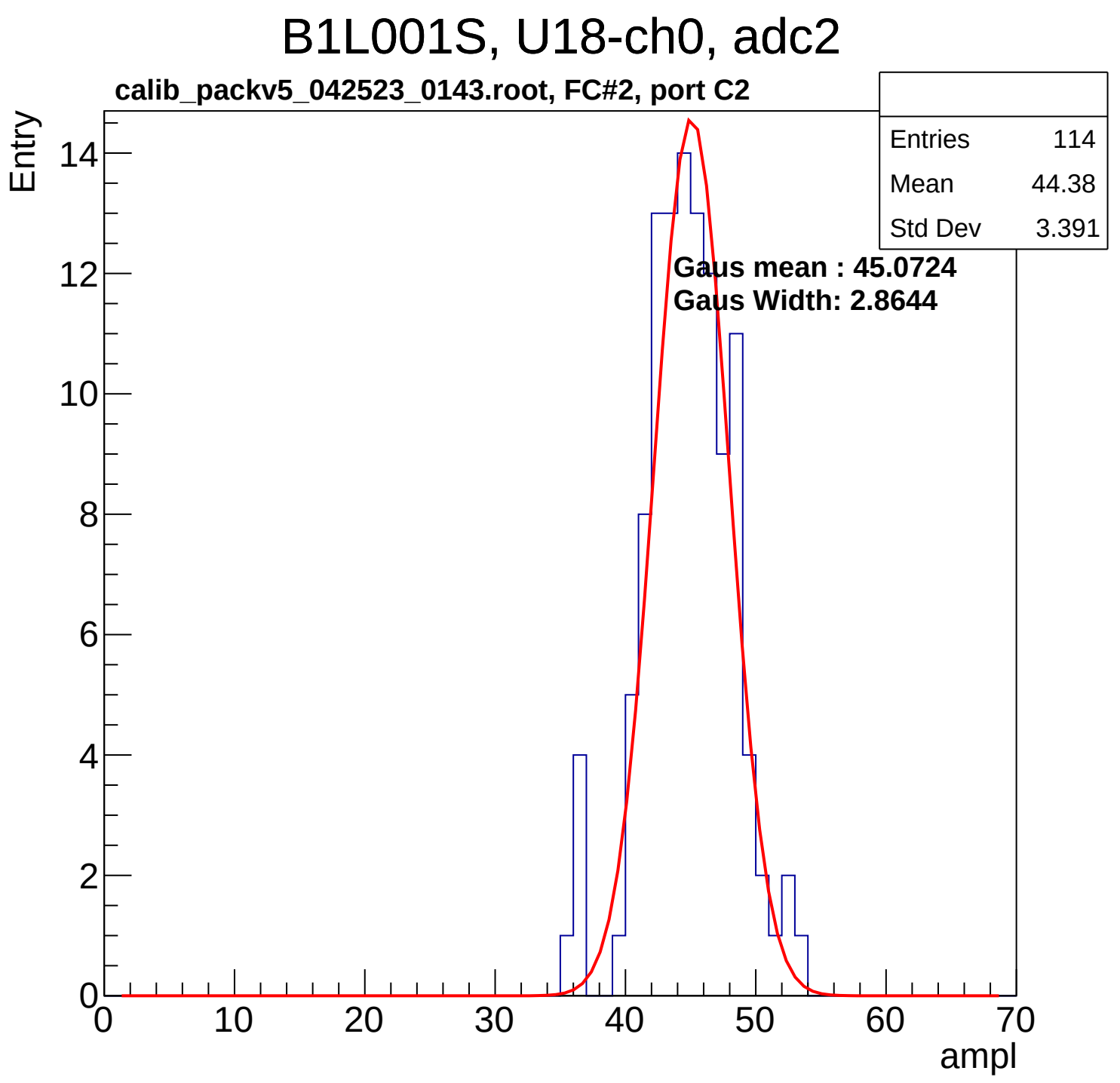
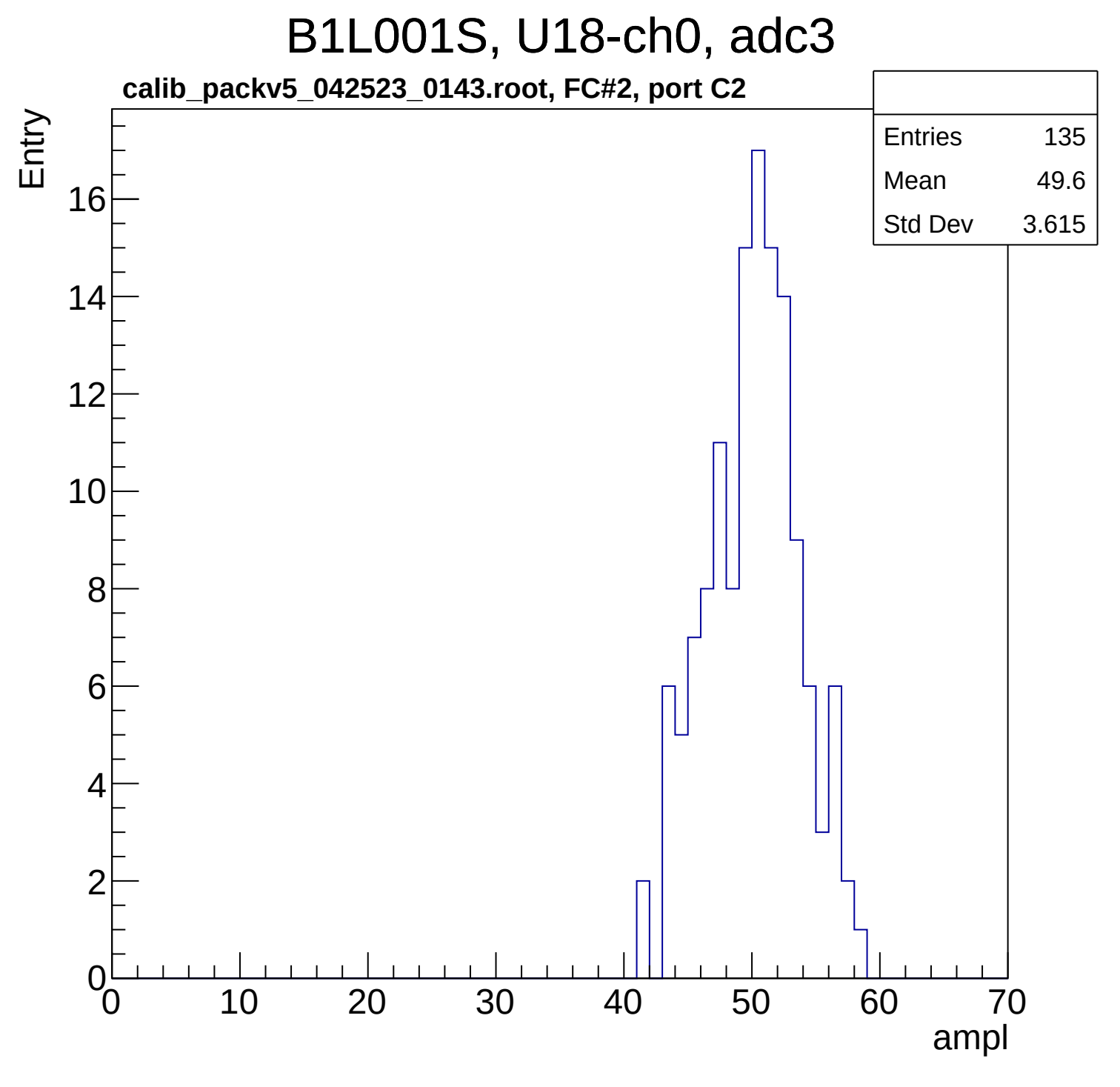
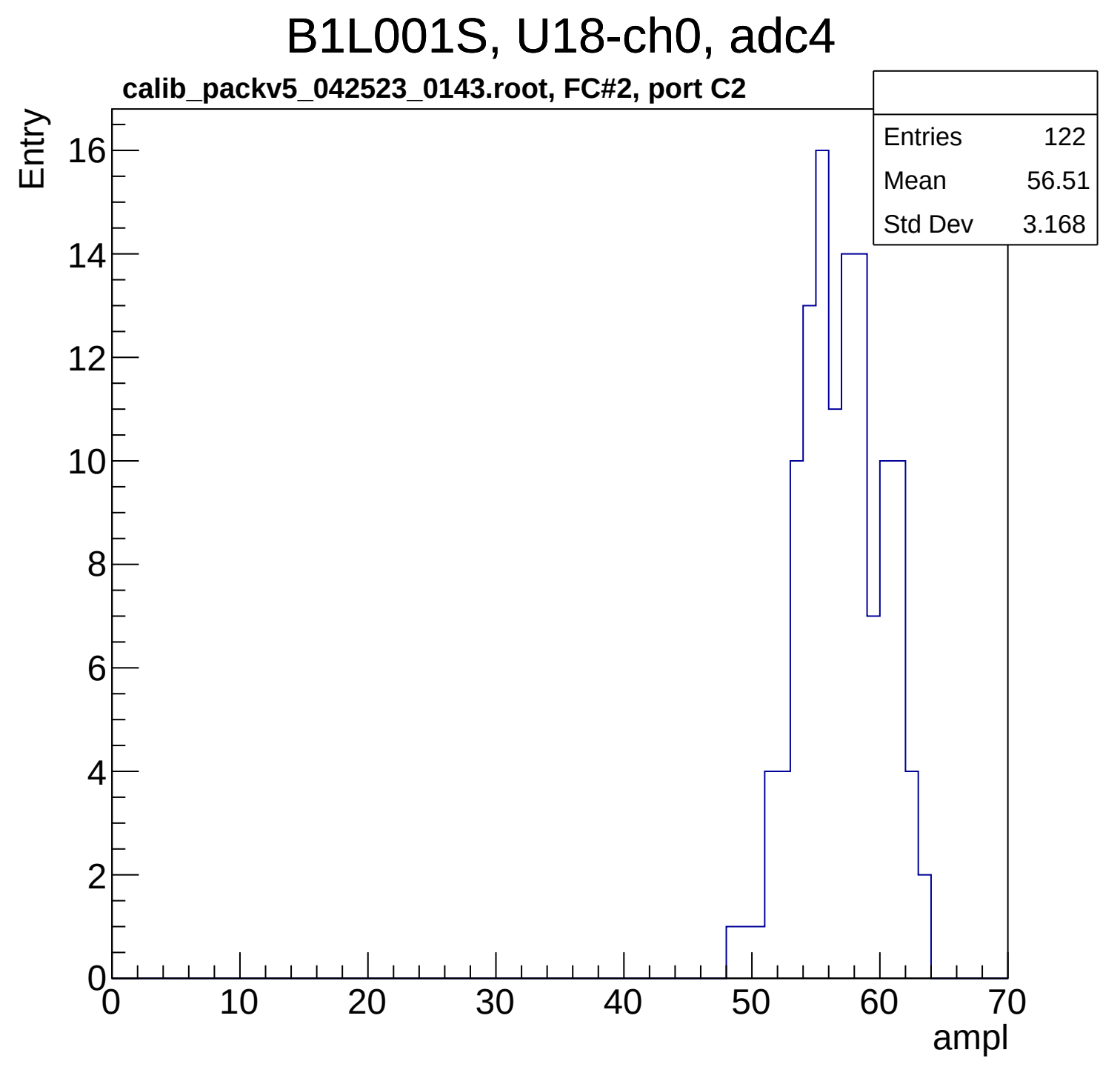
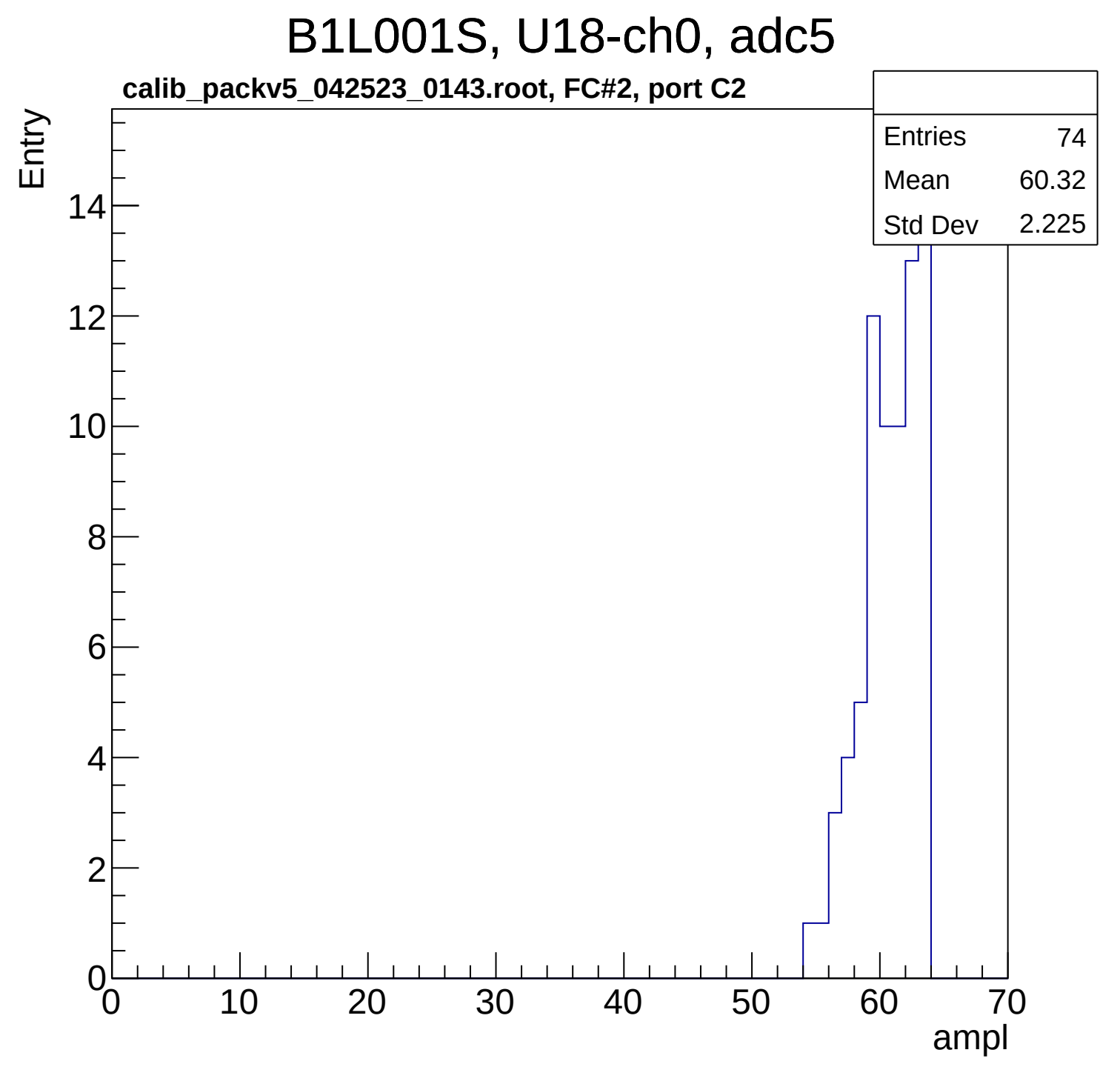

B1L001S, U18-ch0, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 121
Mean 31.24
Std Dev 4.657
Gaus mean : 31.9657
Gaus Width: 3.4295
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

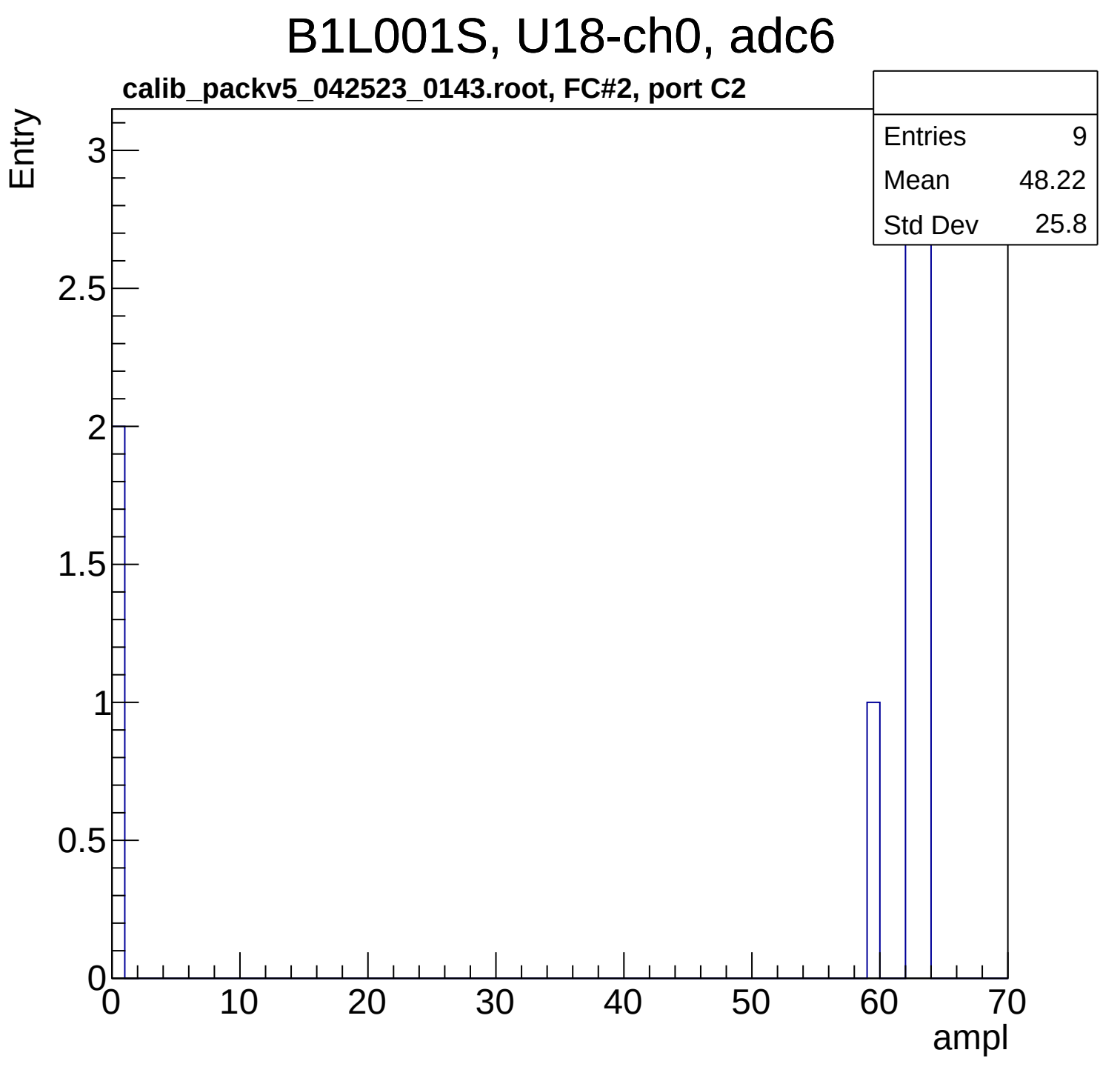

B1L001S, U18-ch0, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 128
Mean 37.3
Std Dev 3.03
Gaus mean : 37.8925
Gaus Width: 2.9268
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

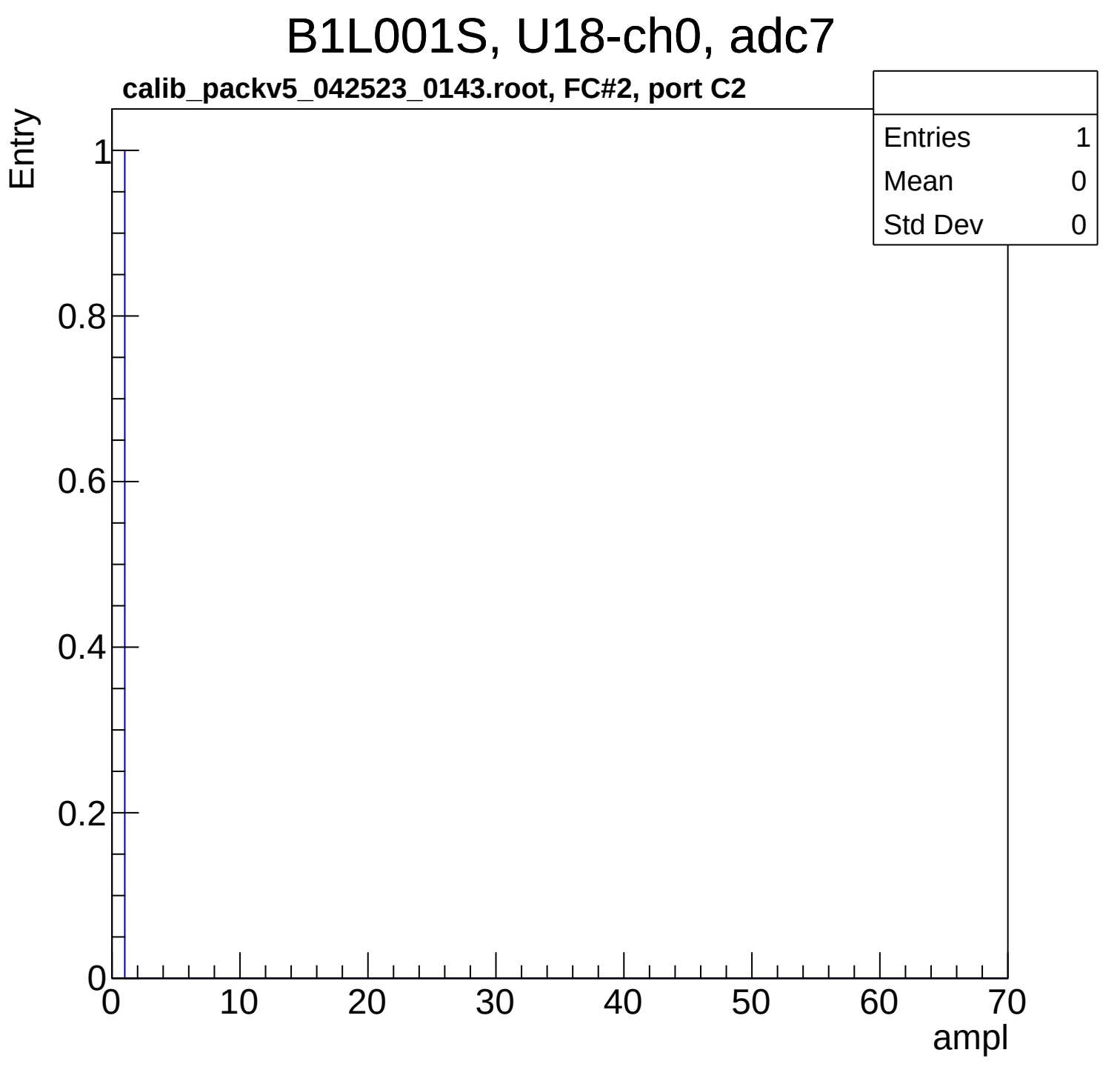

B1L001S, U18-ch0, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 114
Mean 44.38
Std Dev 3.391
Gaus mean : 45.0724
Gaus Width: 2.8644
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

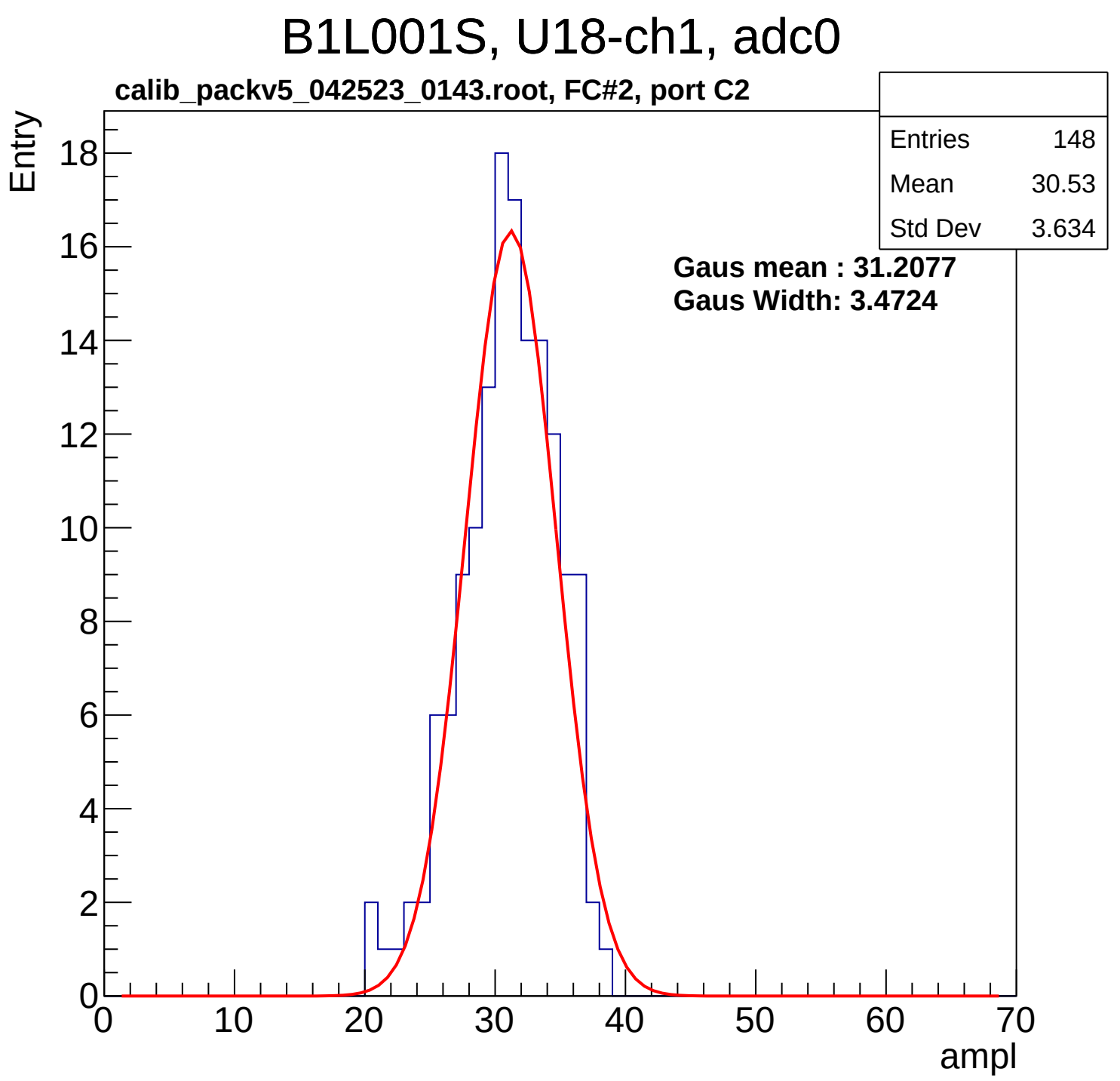

B1L001S, U18-ch0, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 135
Mean 49.6
Std Dev 3.615
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

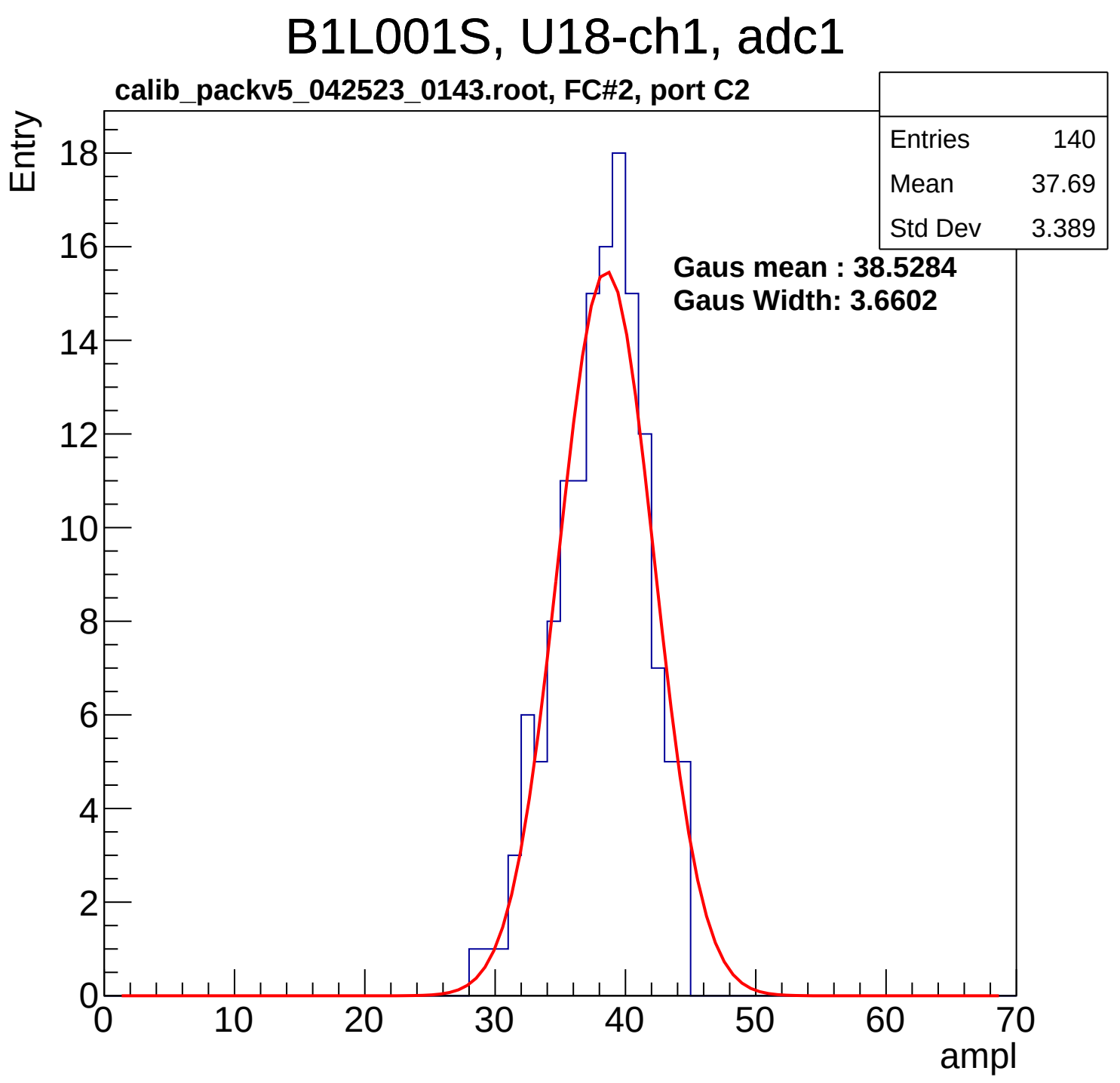

B1L001S, U18-ch0, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 122
Mean 56.51
Std Dev 3.168
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

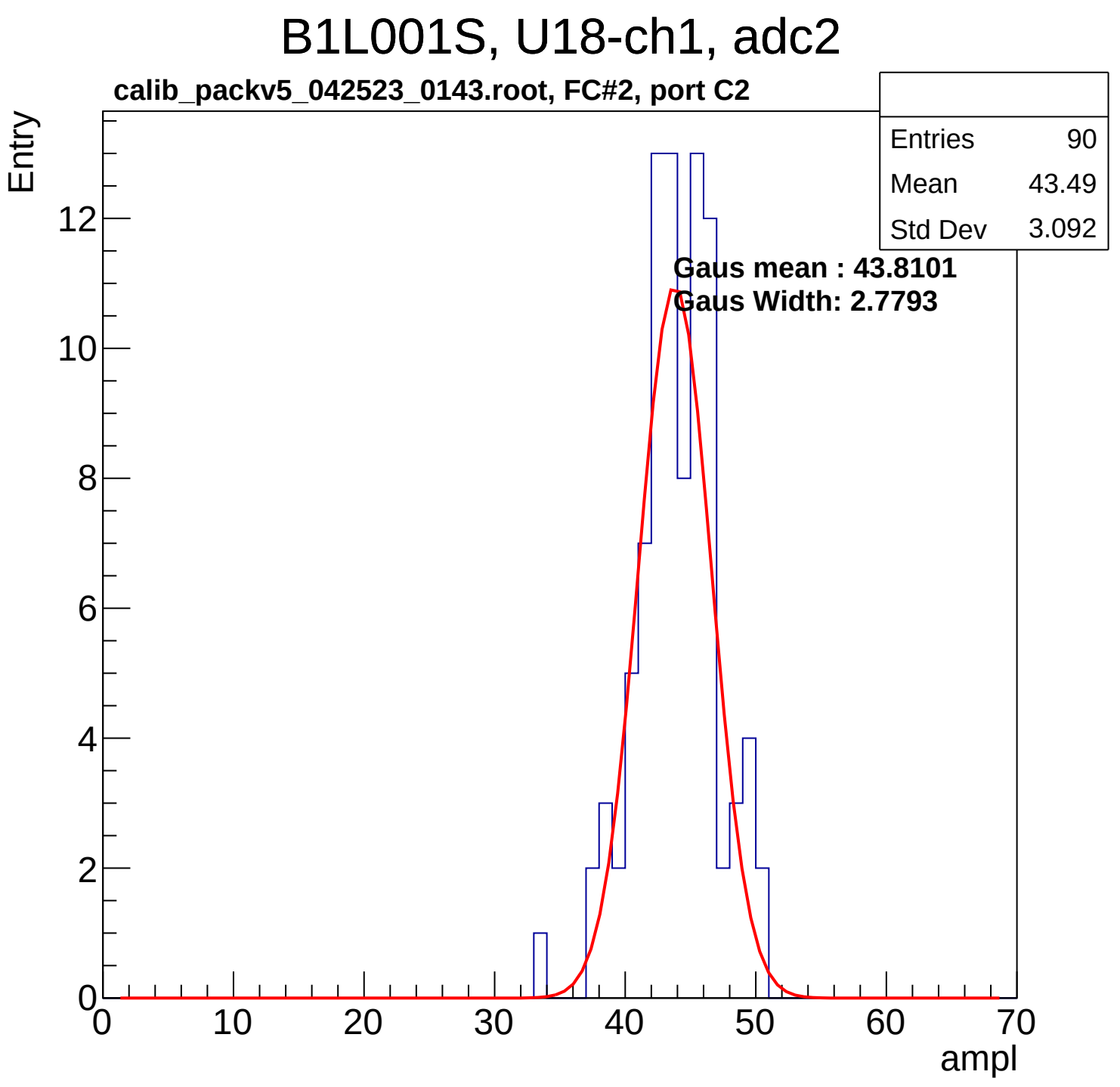

B1L001S, U18-ch0, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 74
Mean 60.32
Std Dev 2.225
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

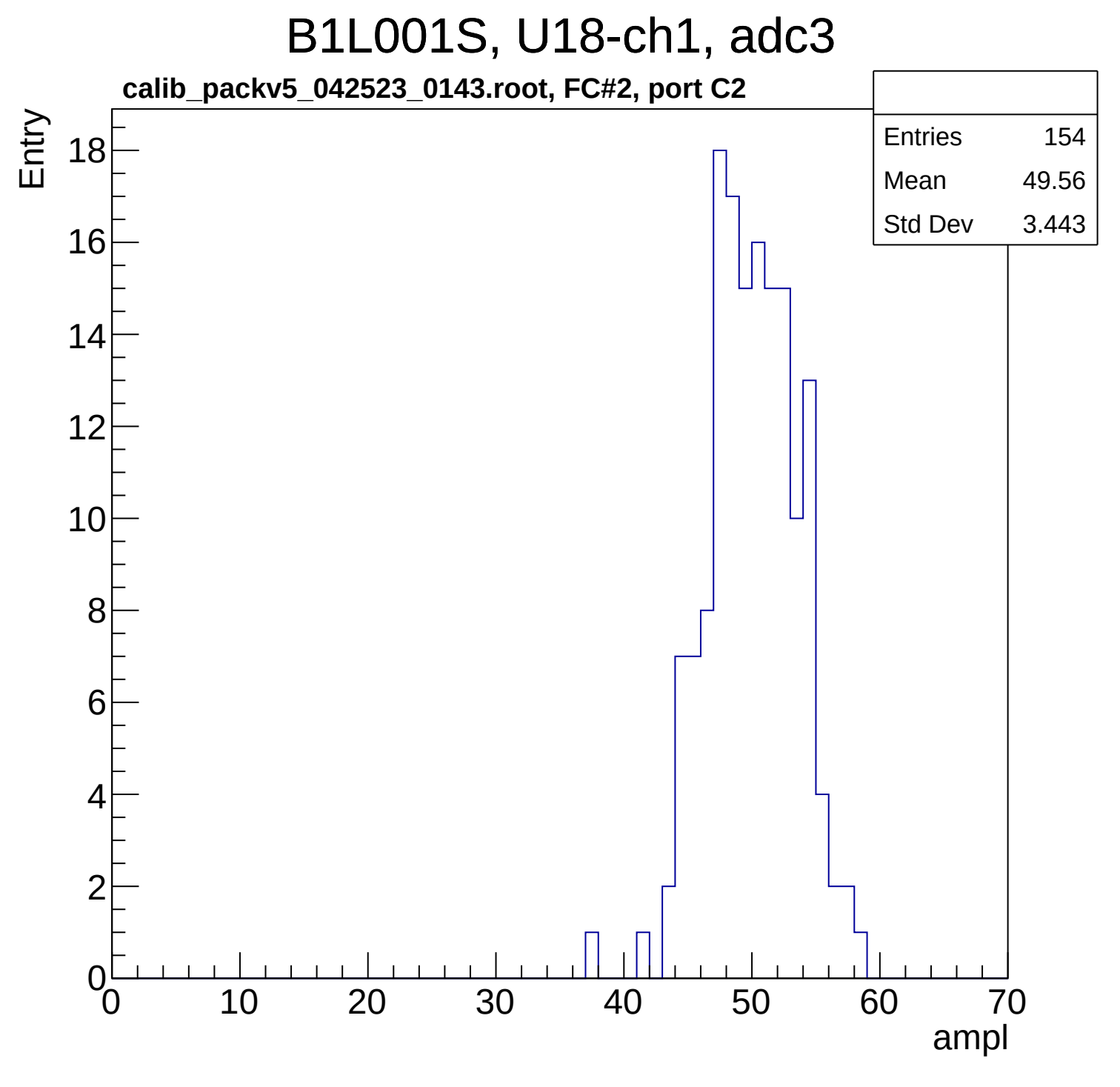

B1L001S, U18-ch0, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 9
Mean 48.22
Std Dev 25.8
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

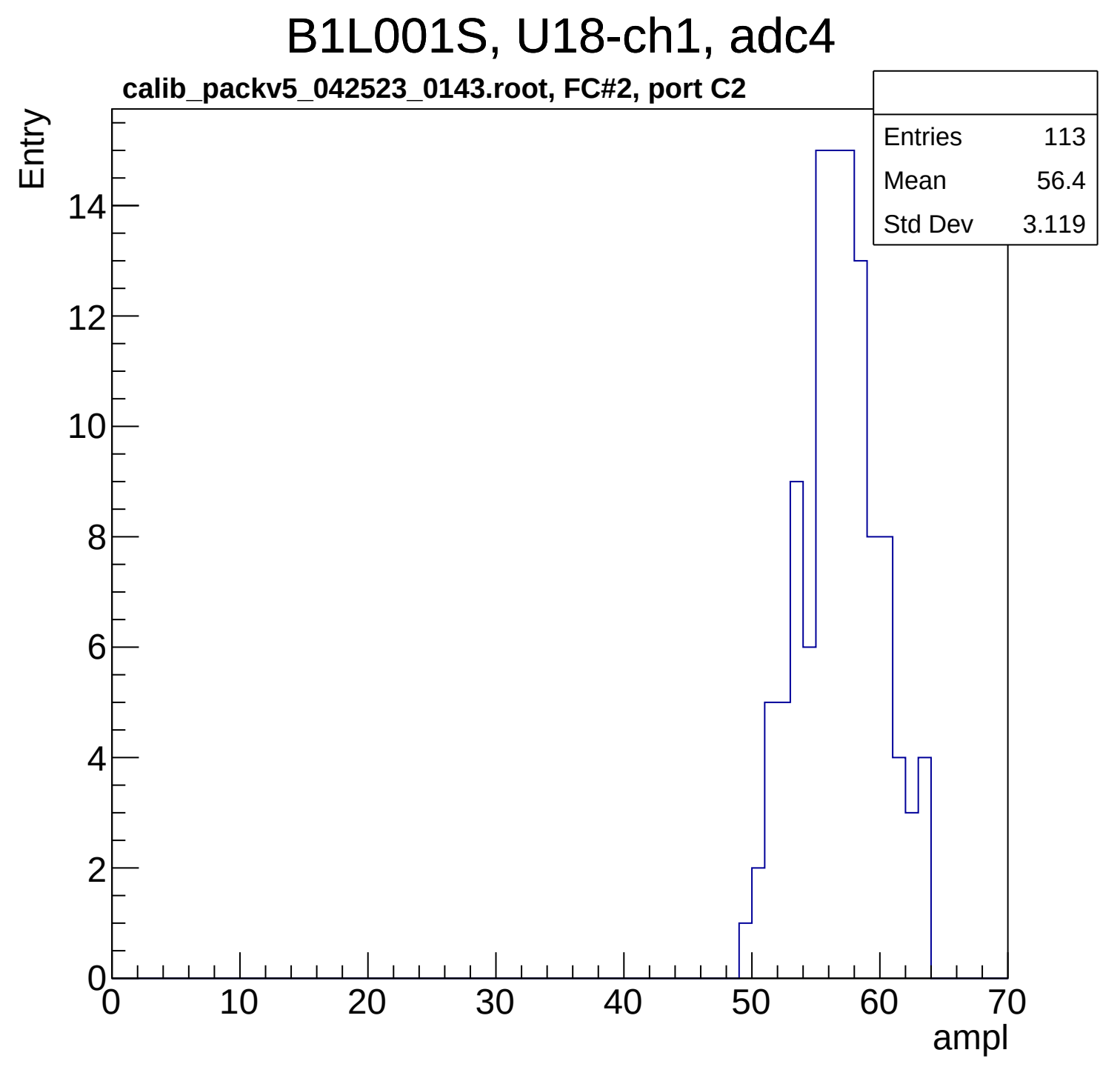

B1L001S, U18-ch0, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

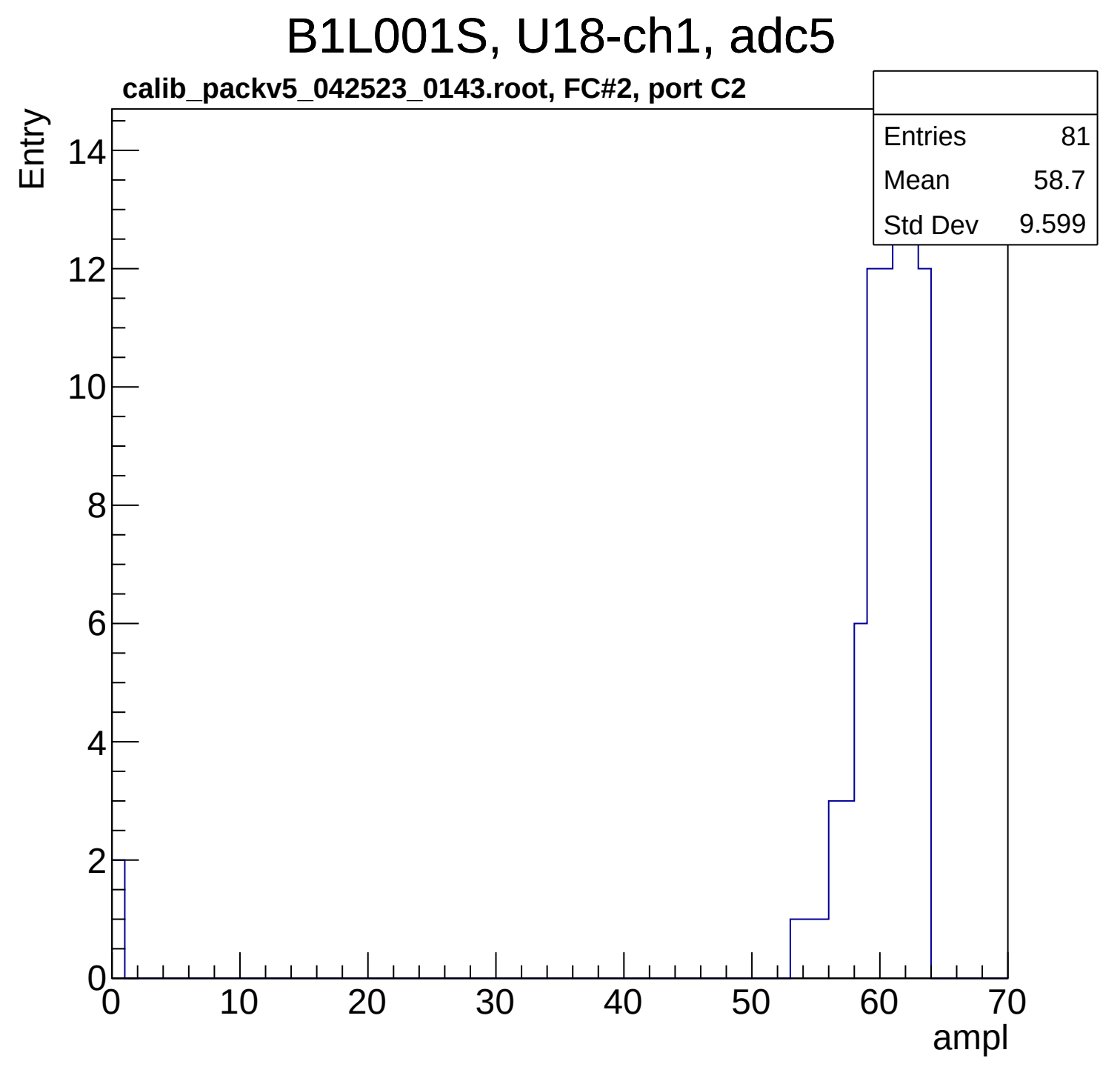

B1L001S, U18-ch1, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 148
Mean 30.53
Std Dev 3.634
Gaus mean : 31.2077
Gaus Width: 3.4724
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

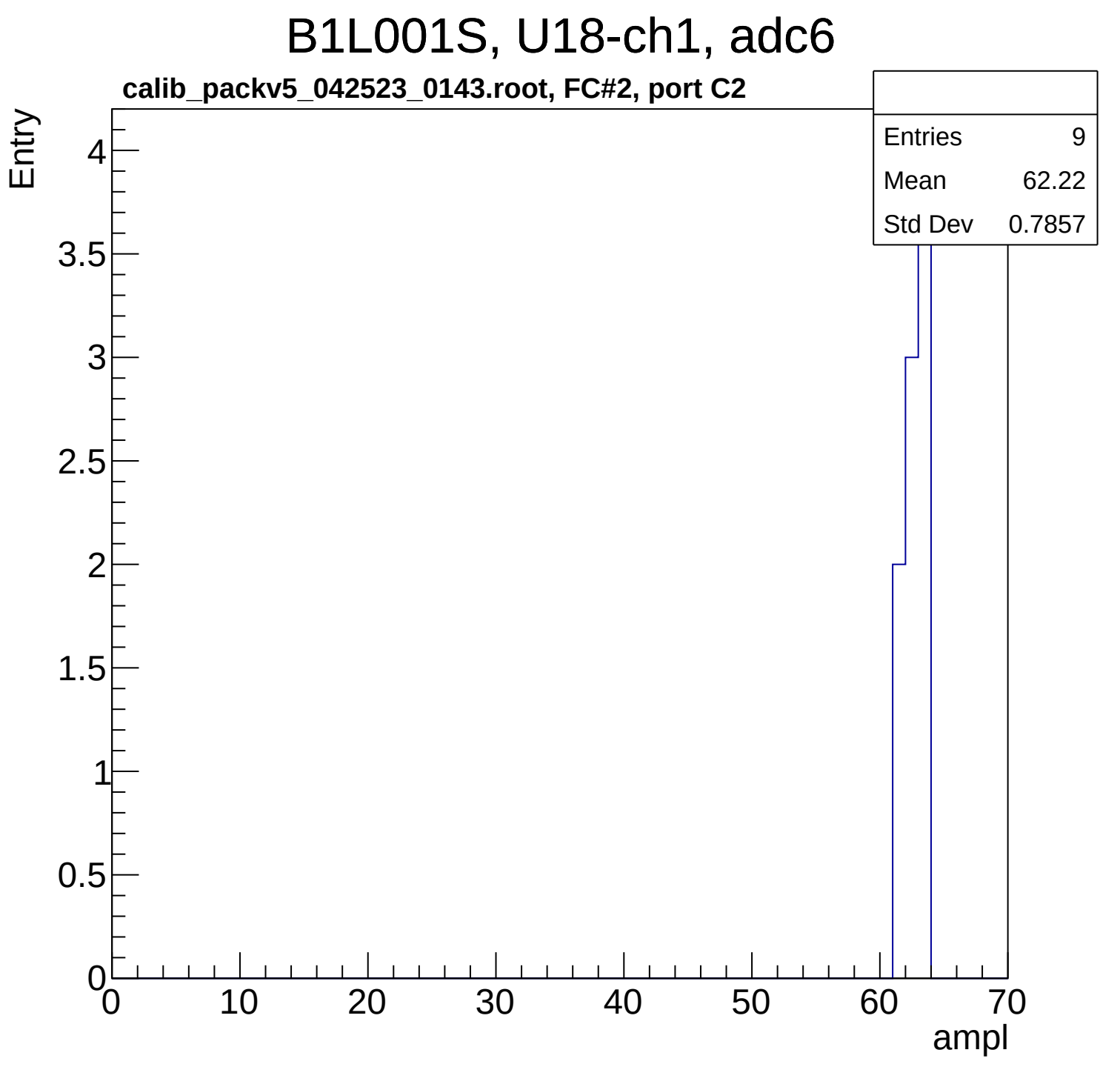

B1L001S, U18-ch1, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 140
Mean 37.69
Std Dev 3.389
Gaus mean : 38.5284
Gaus Width: 3.6602
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

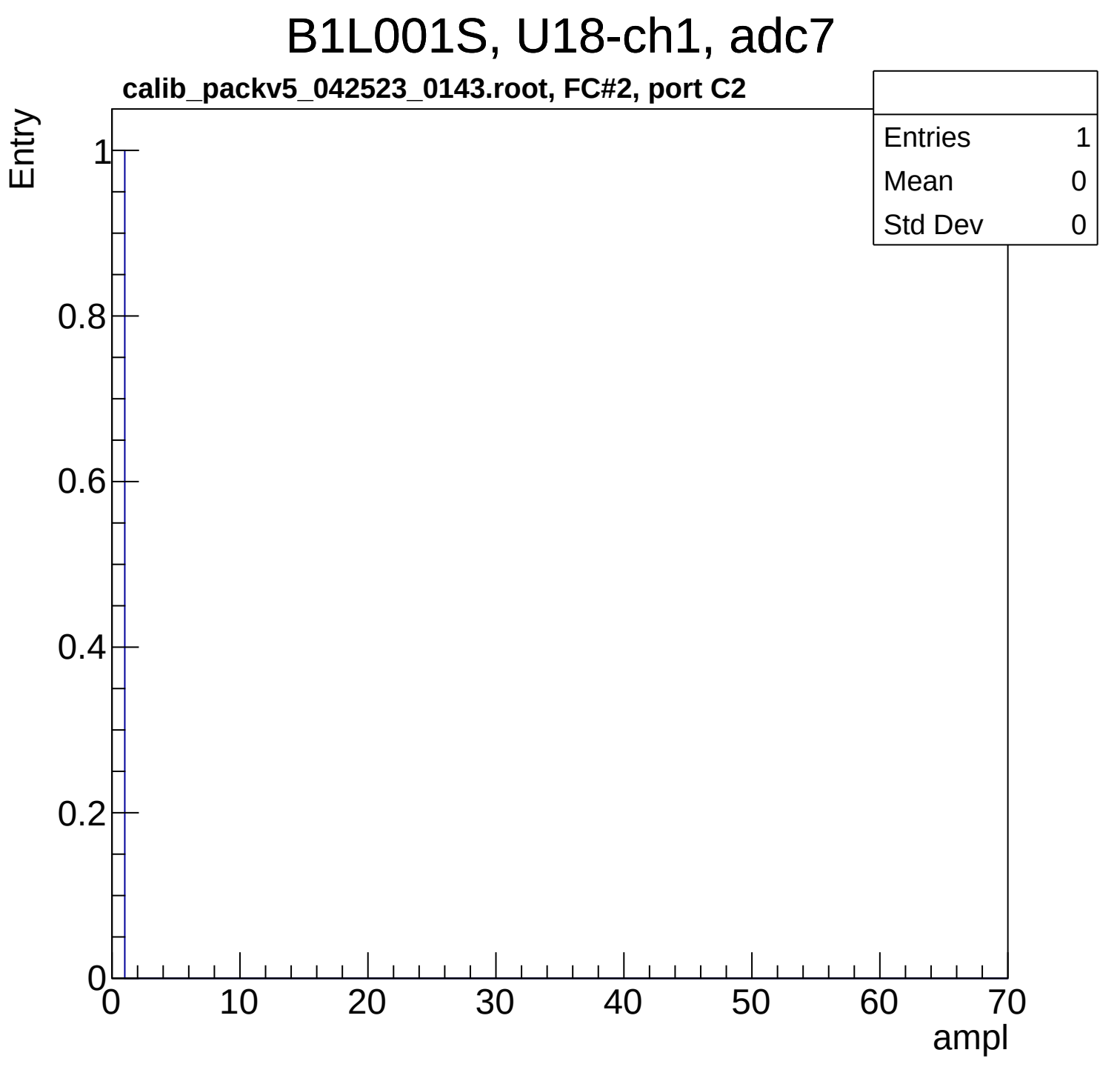

B1L001S, U18-ch1, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 90
Mean 43.49
Std Dev 3.092
Gaus mean : 43.8101
Gaus Width: 2.7793
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70

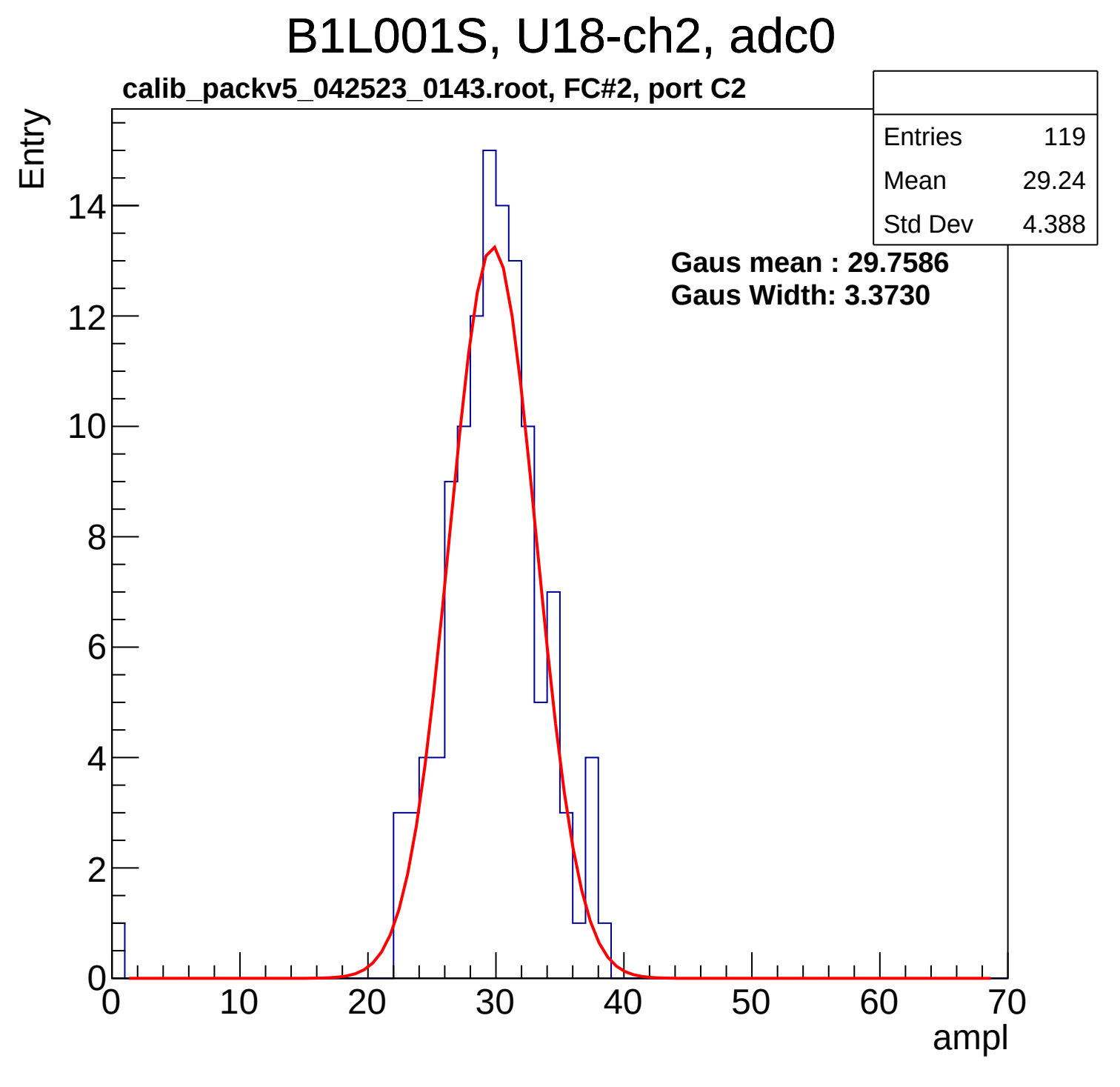

B1L001S, U18-ch1, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 154
Mean 49.56
Std Dev 3.443
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

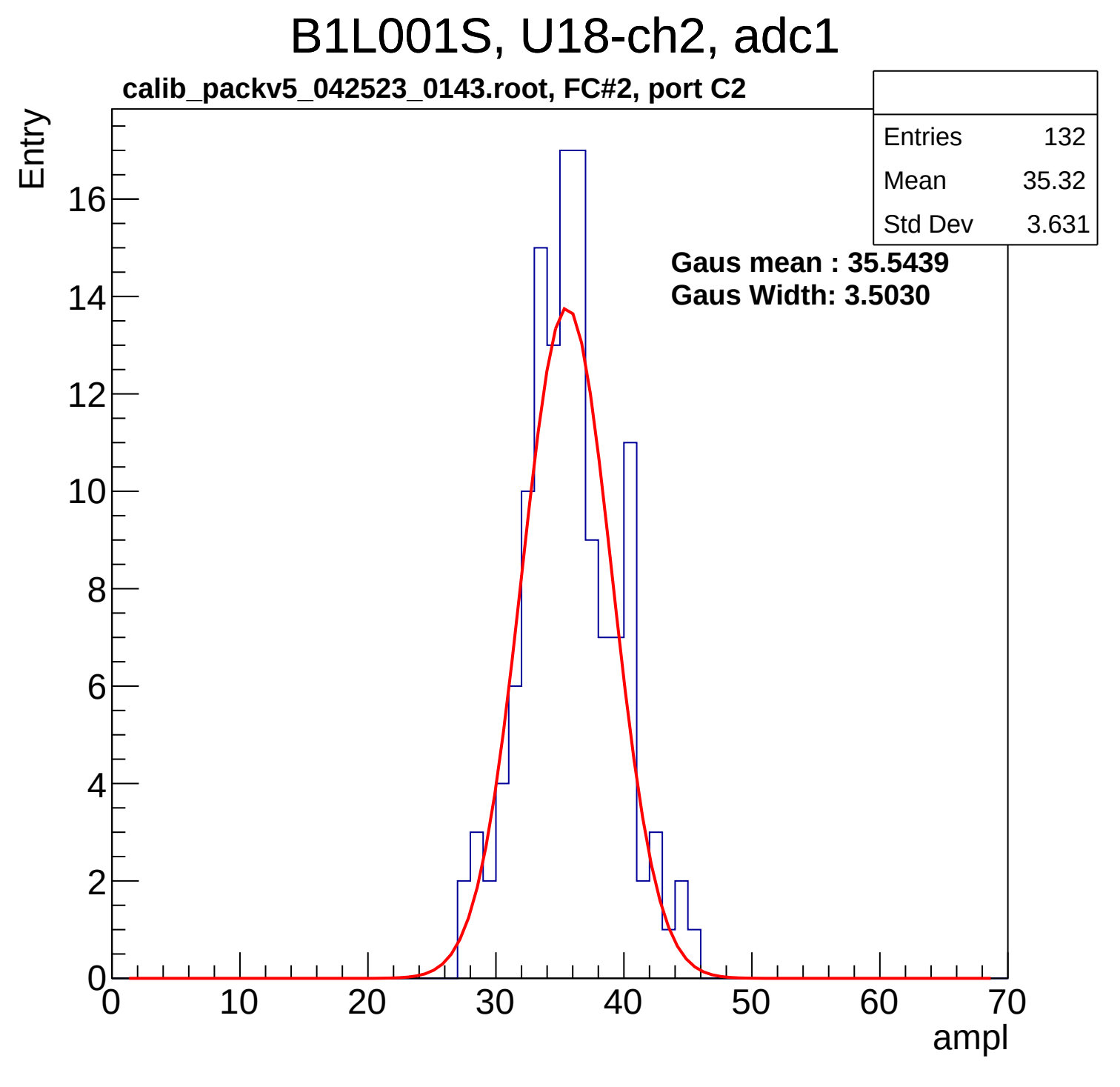

B1L001S, U18-ch1, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 113
Mean 56.4
Std Dev 3.119
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl

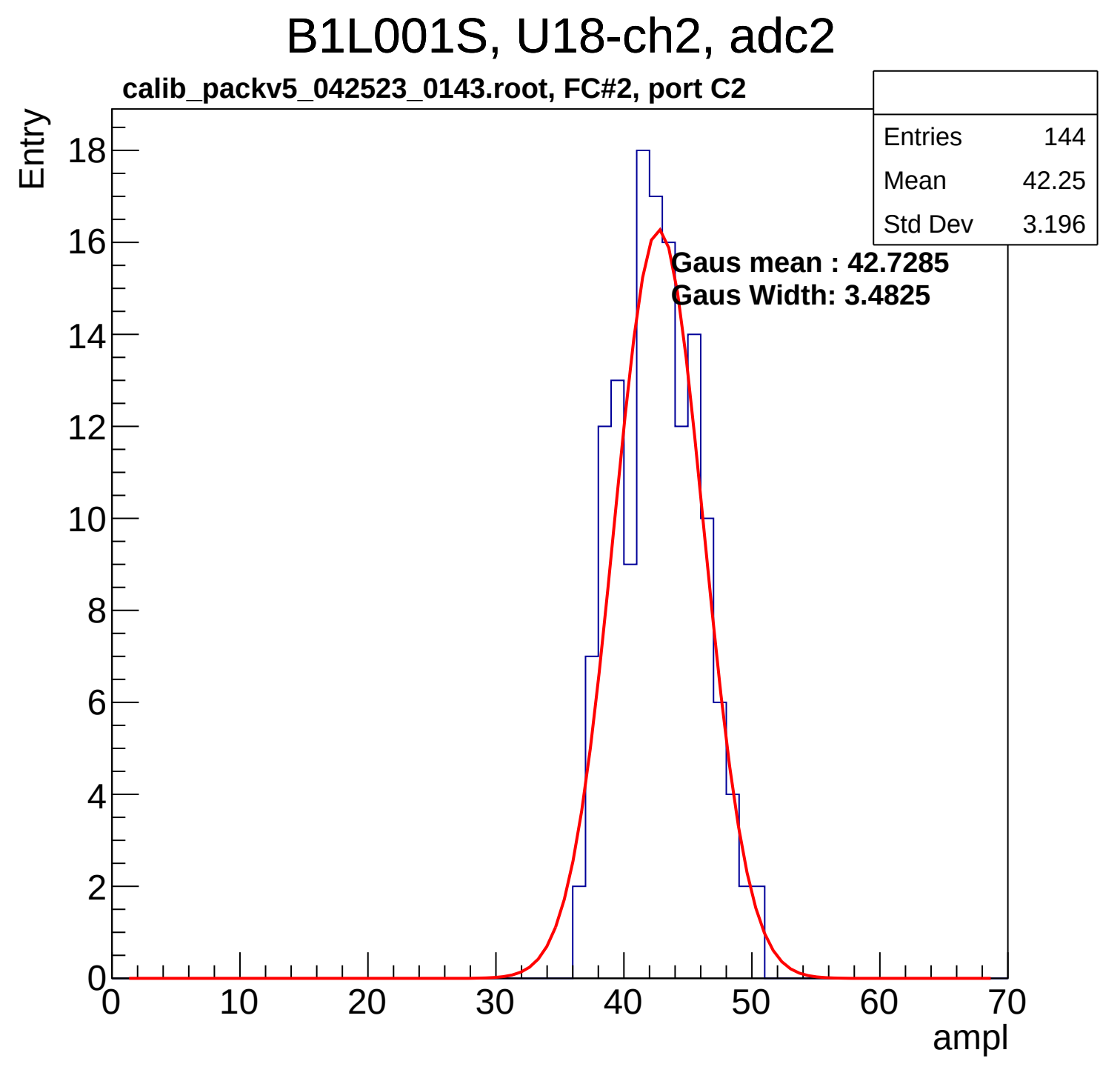

B1L001S, U18-ch1, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 81
Mean 58.7
Std Dev 9.599
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

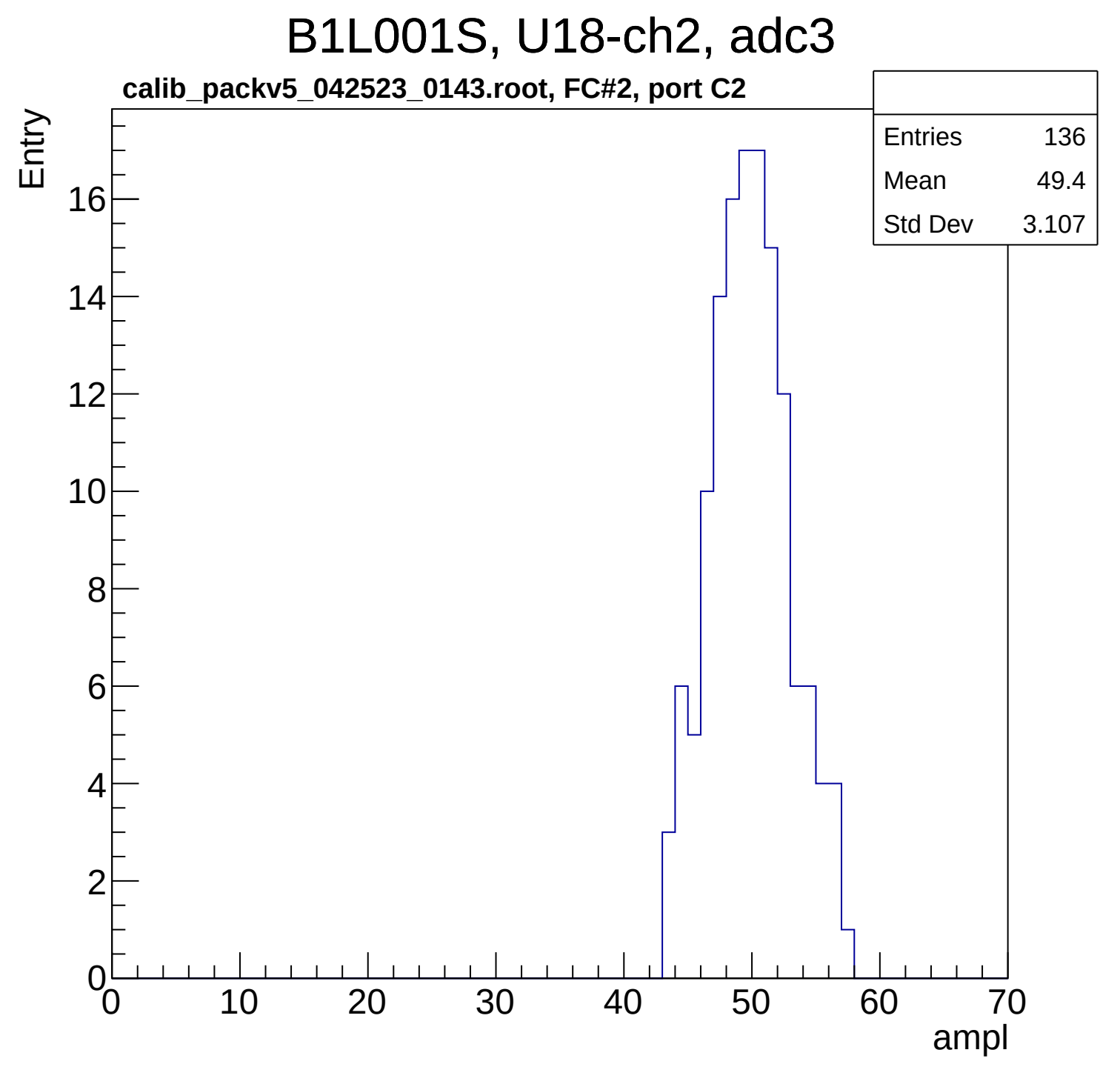

B1L001S, U18-ch1, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 9
Mean 62.22
Std Dev 0.7857
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

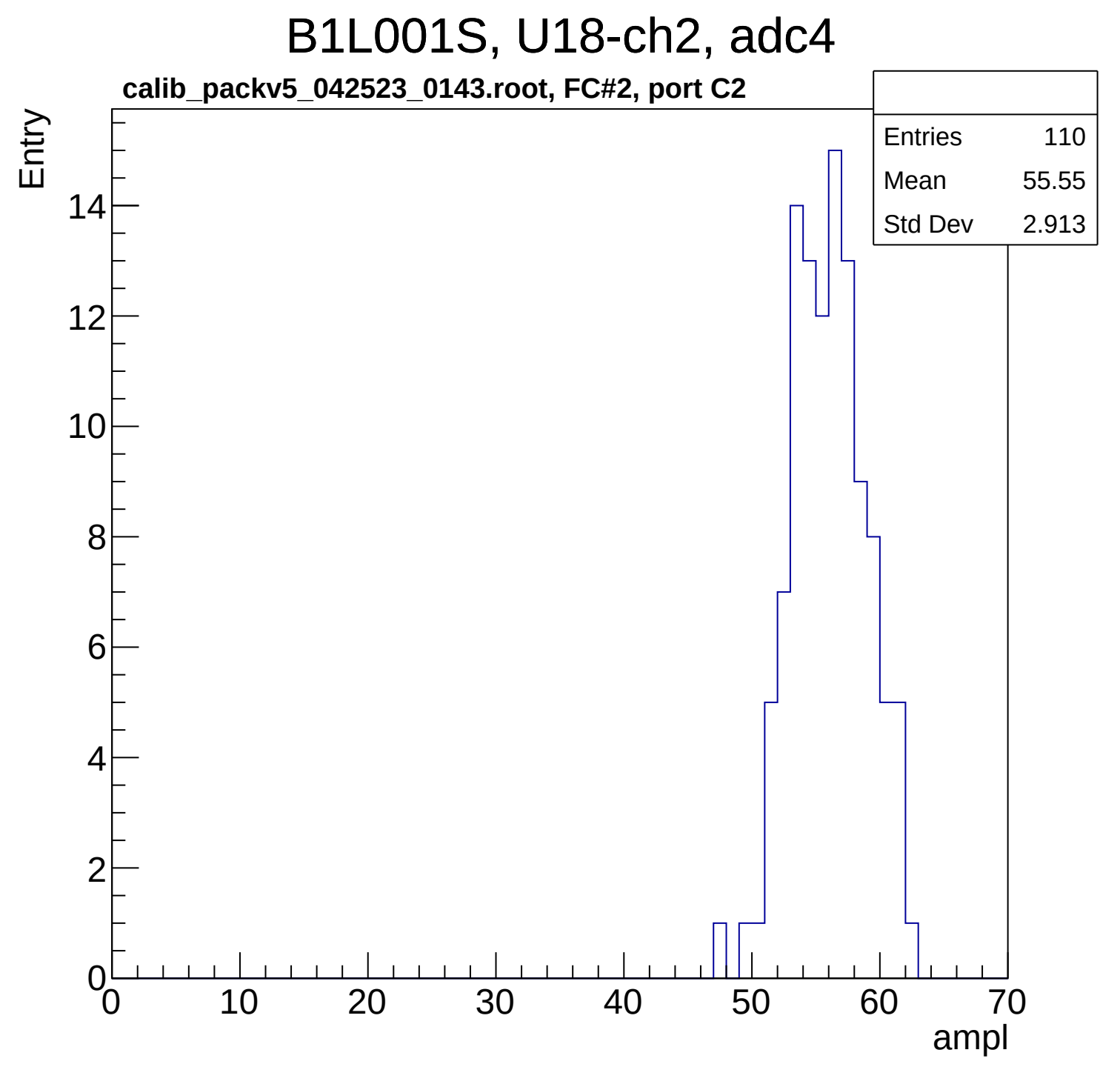

B1L001S, U18-ch1, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

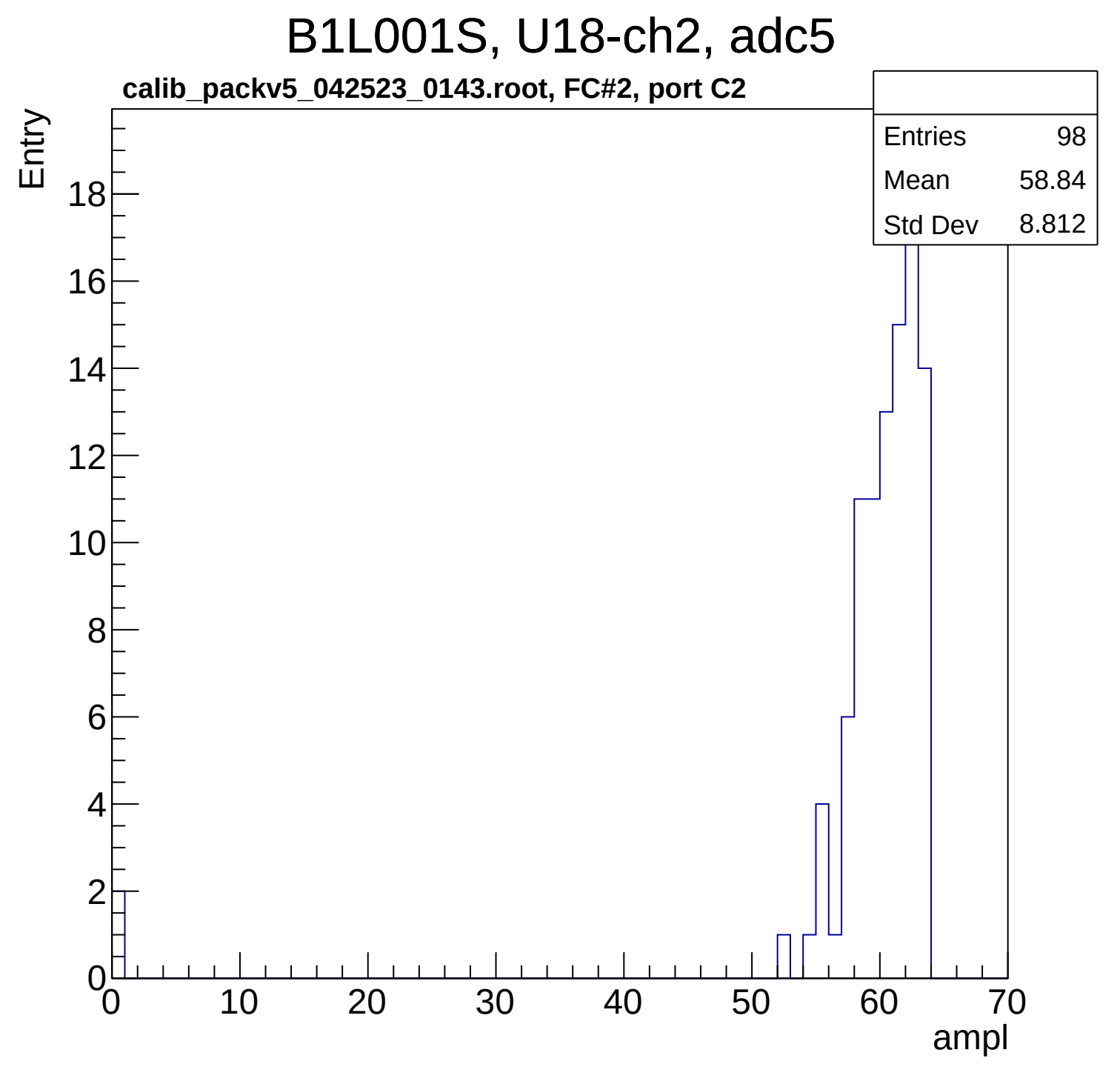

B1L001S, U18-ch2, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 119
Mean 29.24
Std Dev 4.388
Gaus mean : 29.7586
Gaus Width: 3.3730
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

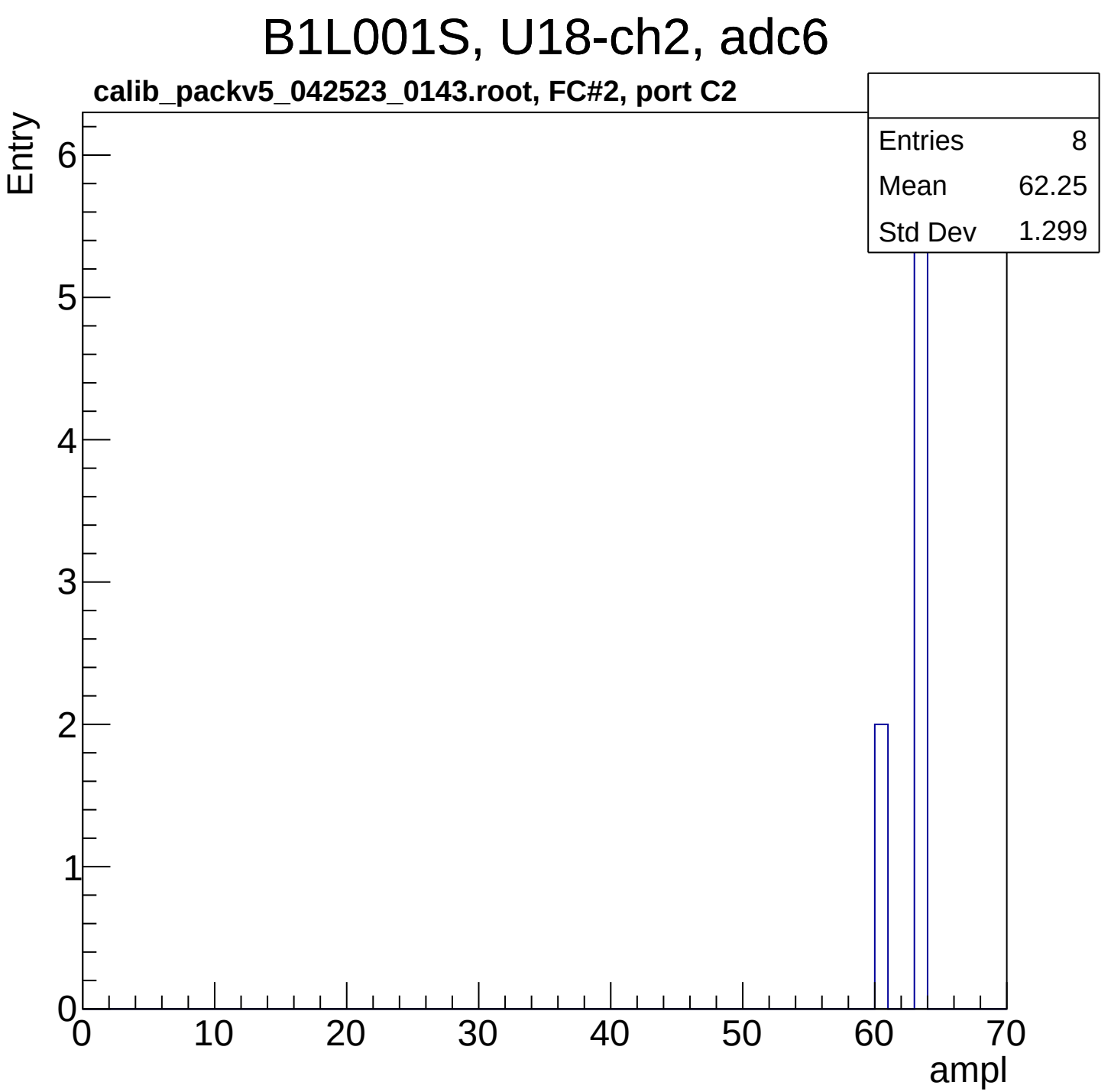

B1L001S, U18-ch2, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 132
Mean 35.32
Std Dev 3.631
Gaus mean : 35.5439
Gaus Width: 3.5030
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

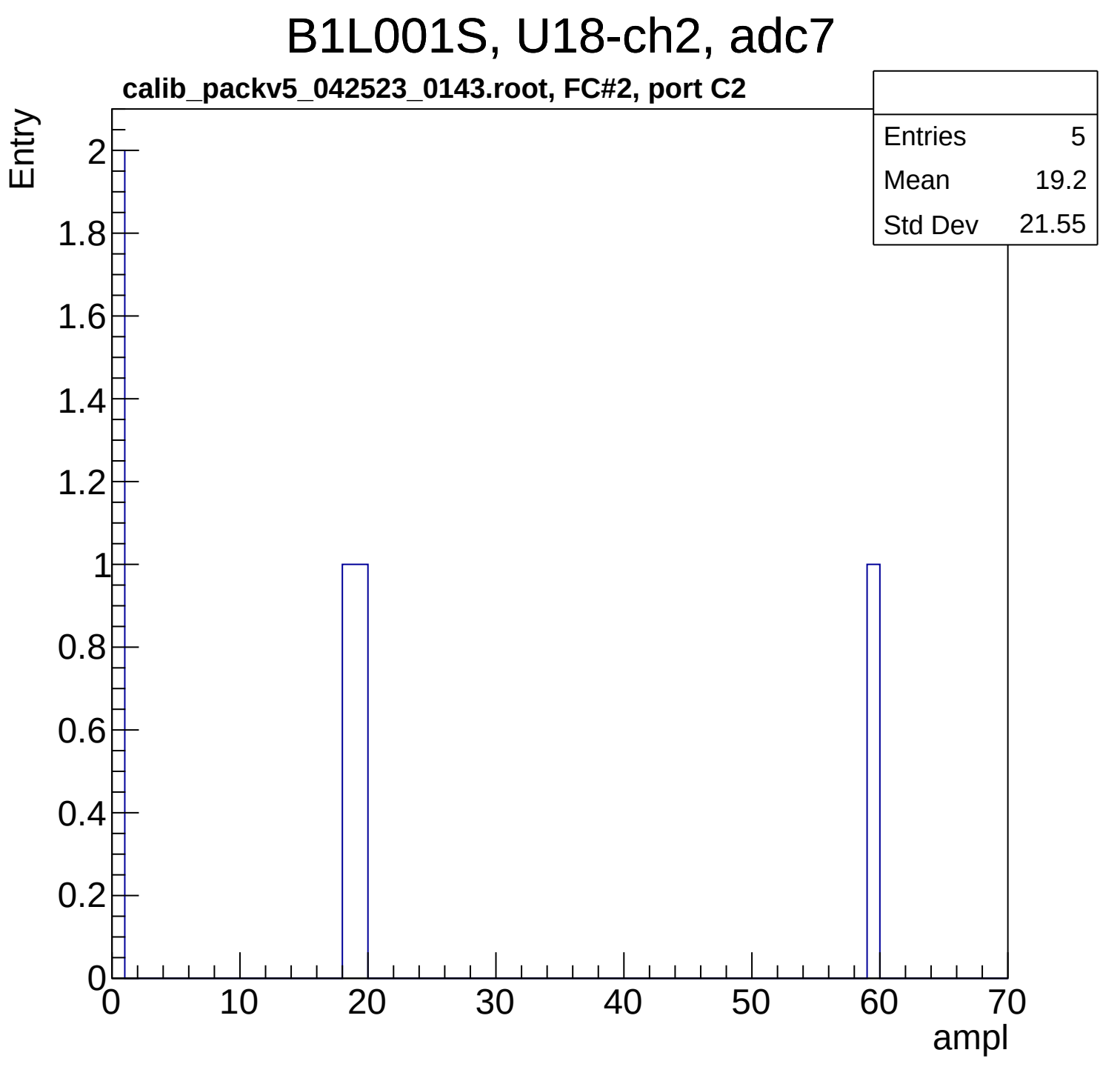

B1L001S, U18-ch2, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 144
Mean 42.25
Std Dev 3.196
Gaus mean : 42.7285
Gaus Width: 3.4825
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

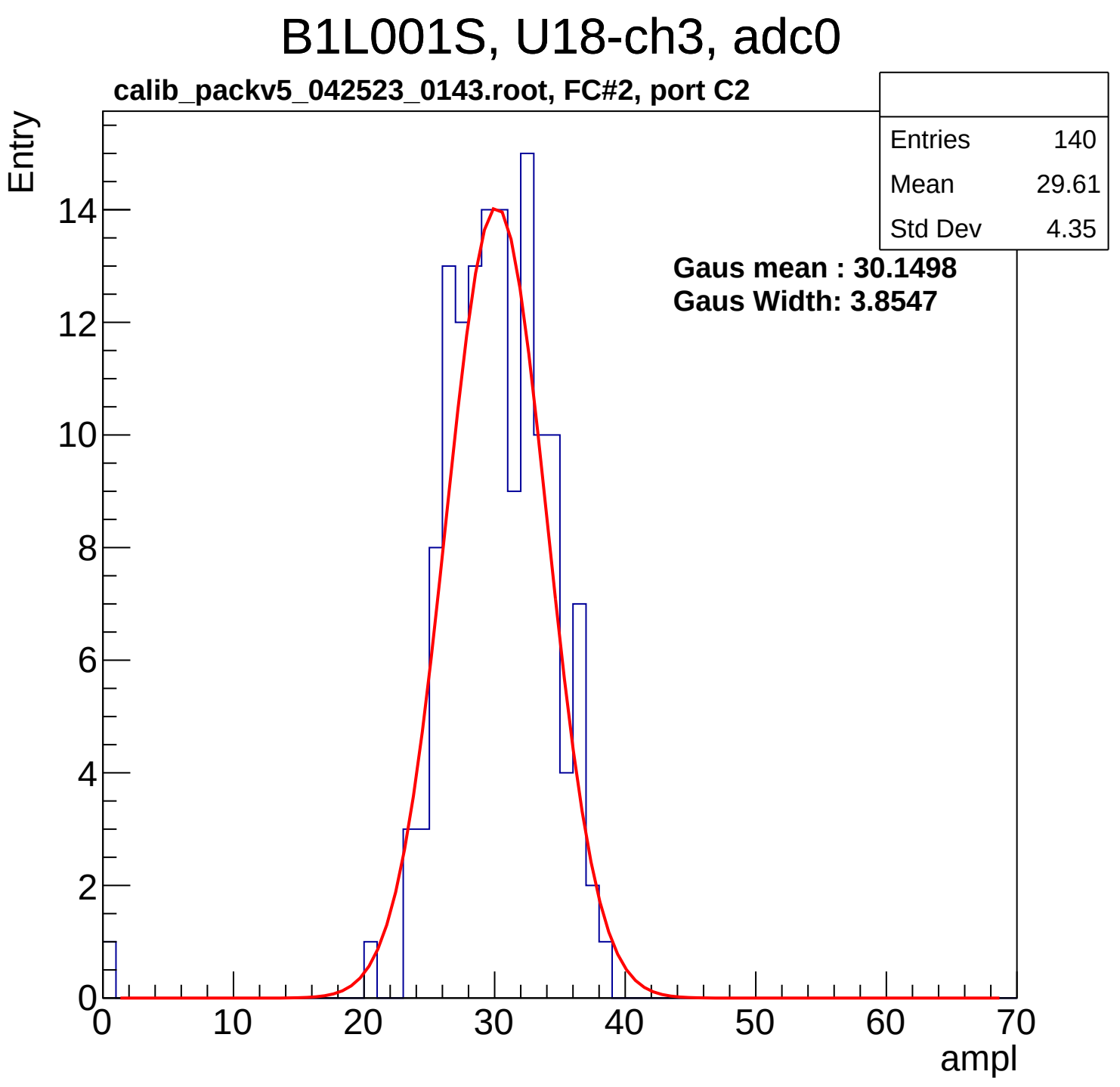

B1L001S, U18-ch2, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 136
Mean 49.4
Std Dev 3.107
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

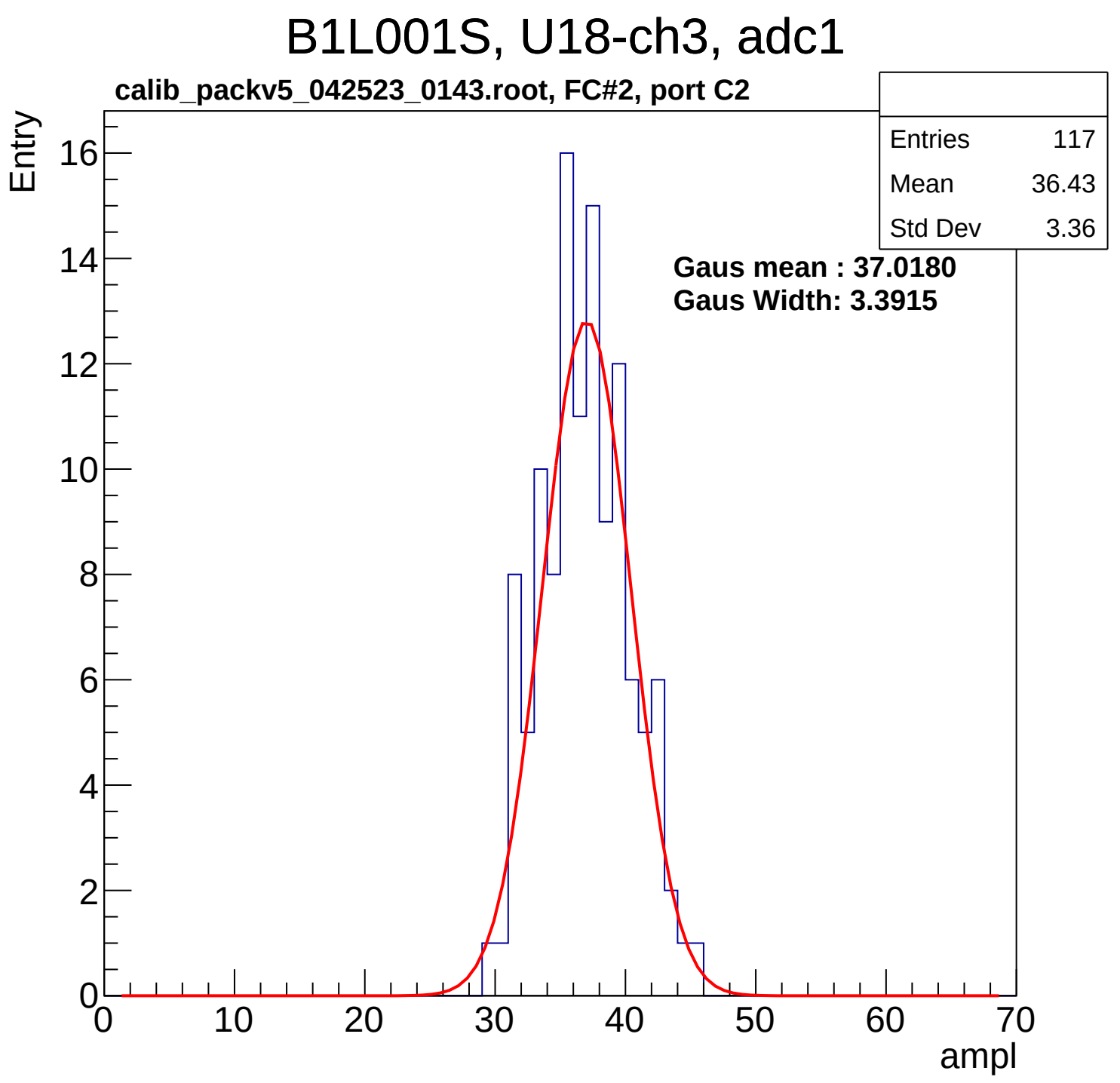

B1L001S, U18-ch2, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 110
Mean 55.55
Std Dev 2.913
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

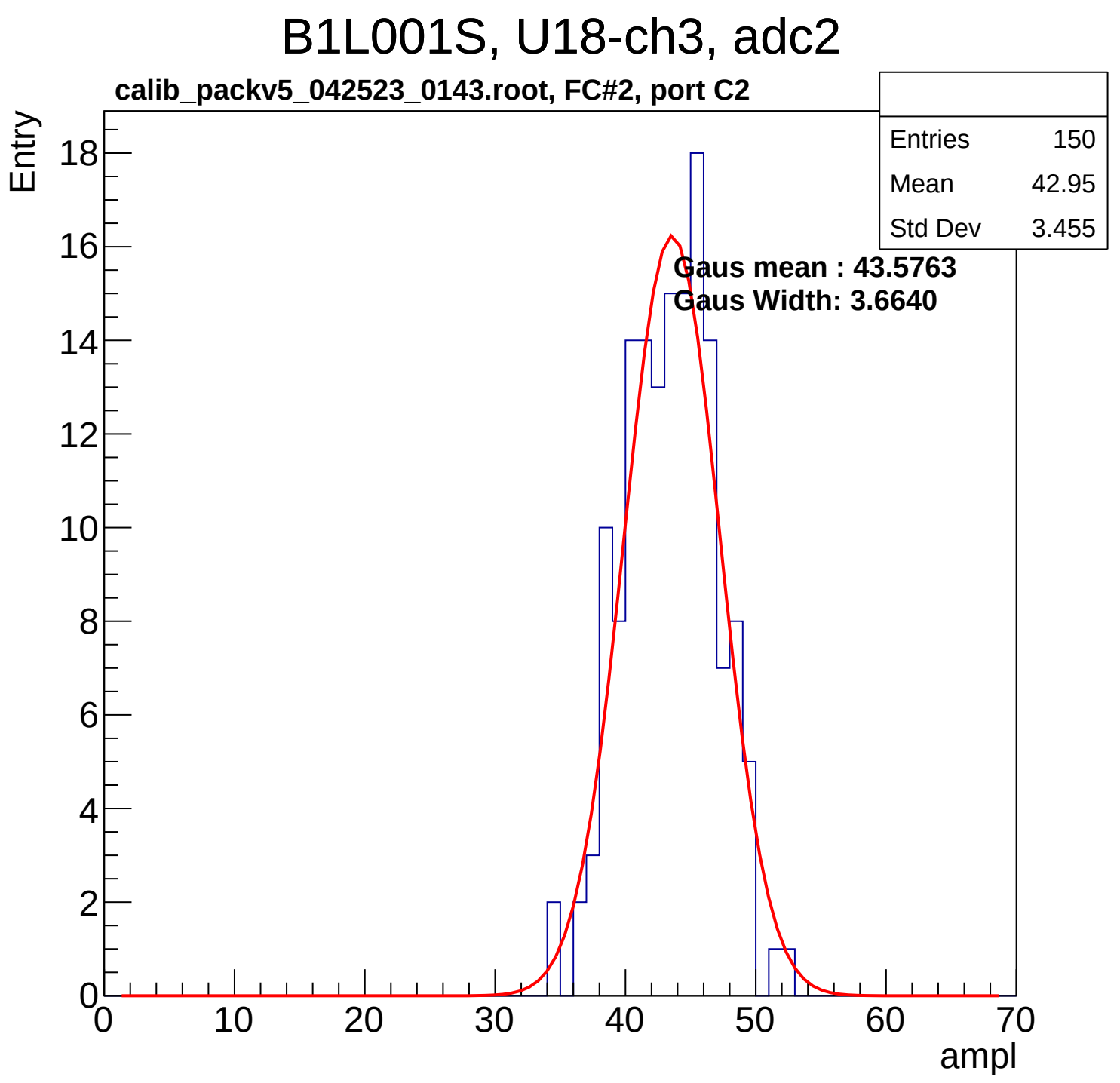

B1L001S, U18-ch2, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 98
Mean 58.84
Std Dev 8.812
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

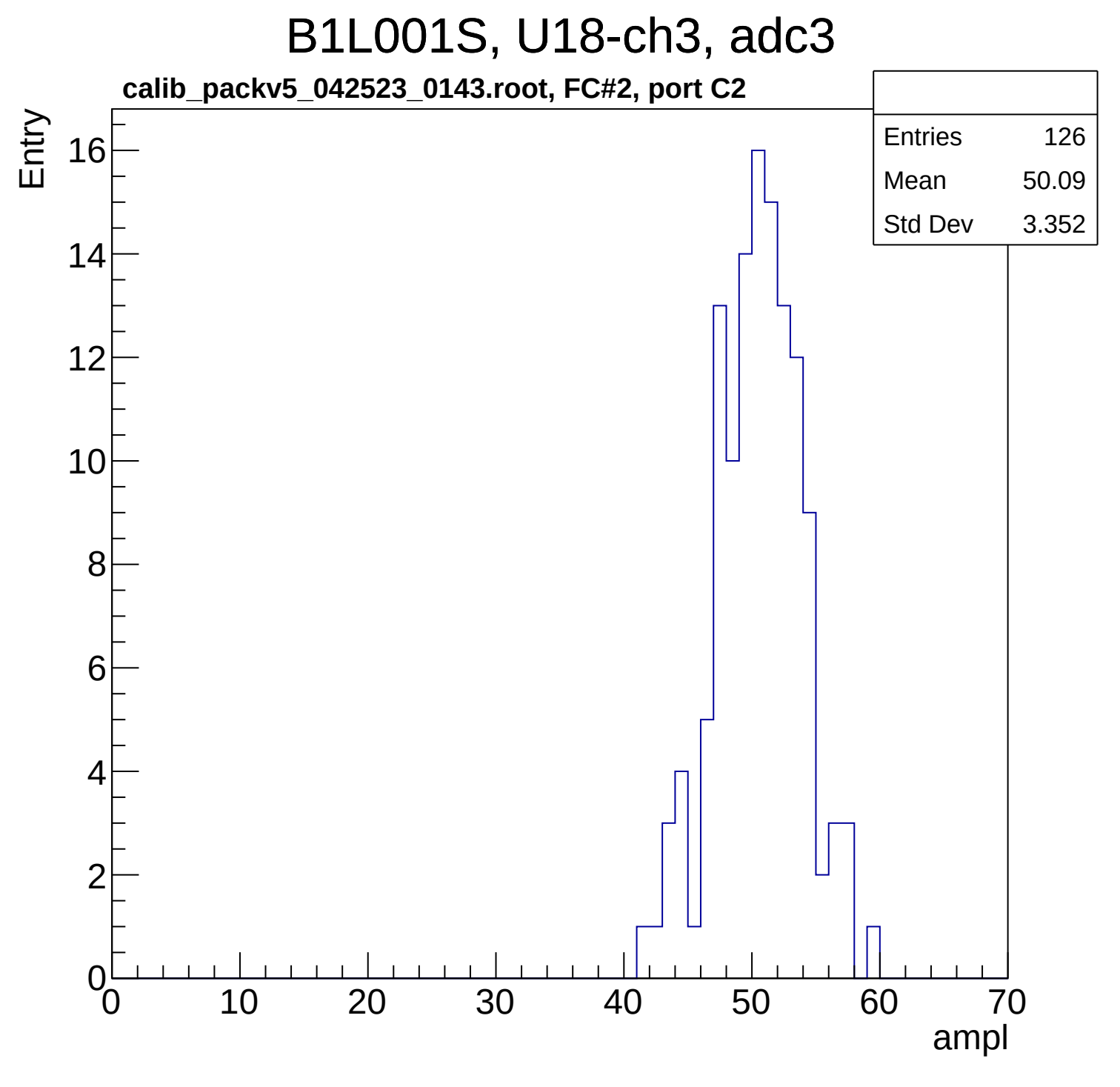

B1L001S, U18-ch2, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 8
Mean 62.25
Std Dev 1.299
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl

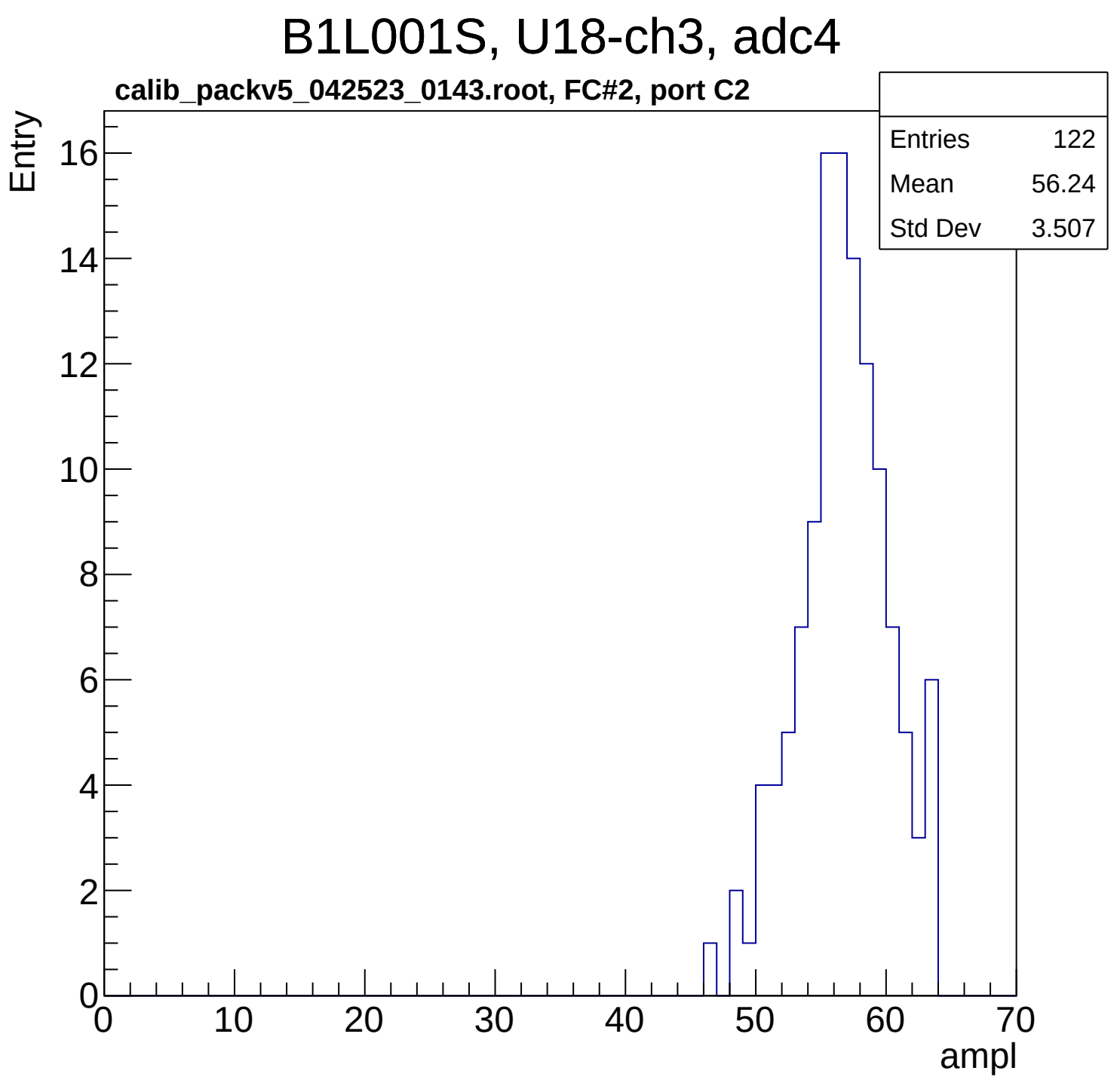

B1L001S, U18-ch2, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 5
Mean 19.2
Std Dev 21.55
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

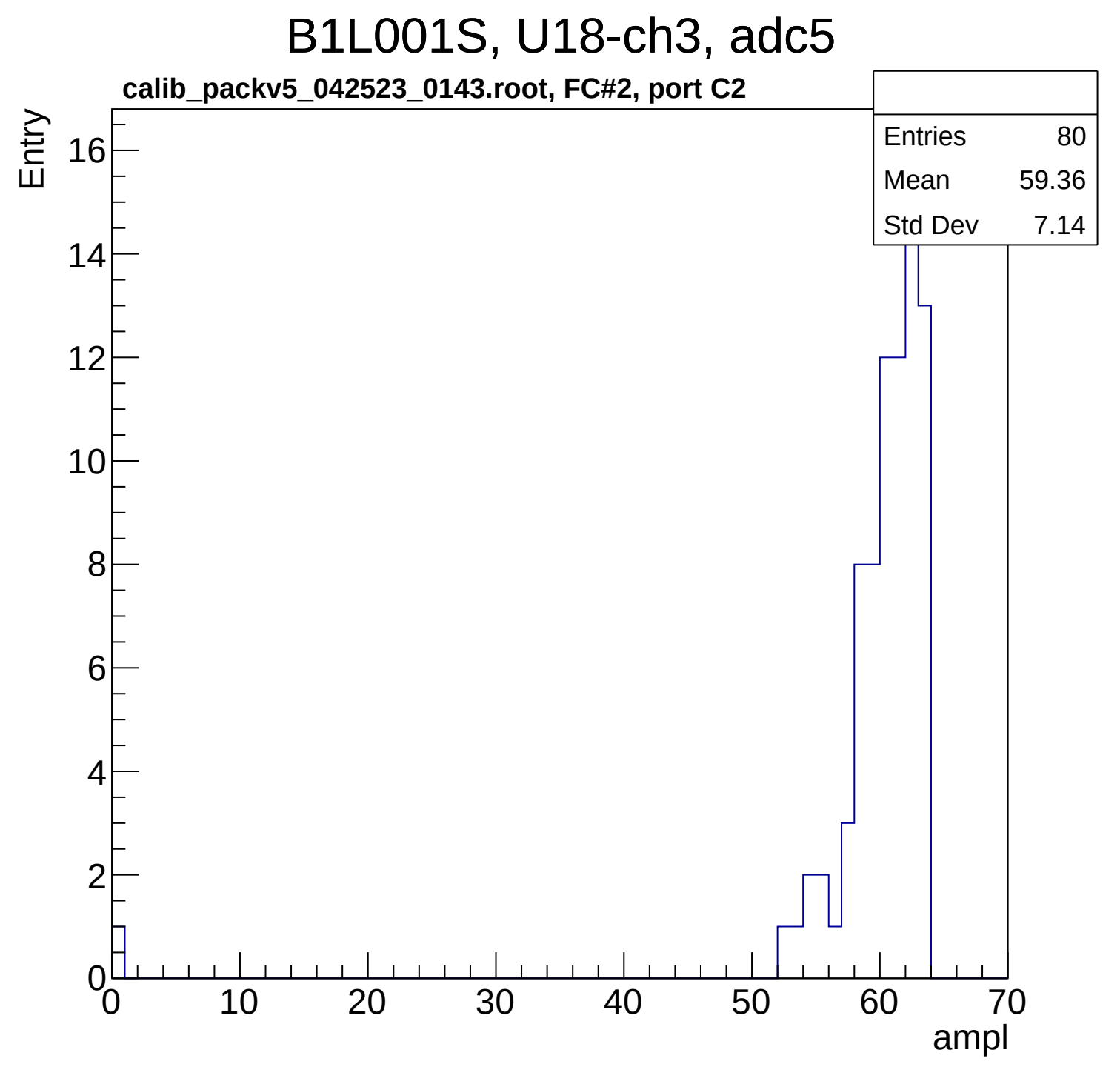

B1L001S, U18-ch3, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 140
Mean 29.61
Std Dev 4.35
Gaus mean : 30.1498
Gaus Width: 3.8547
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

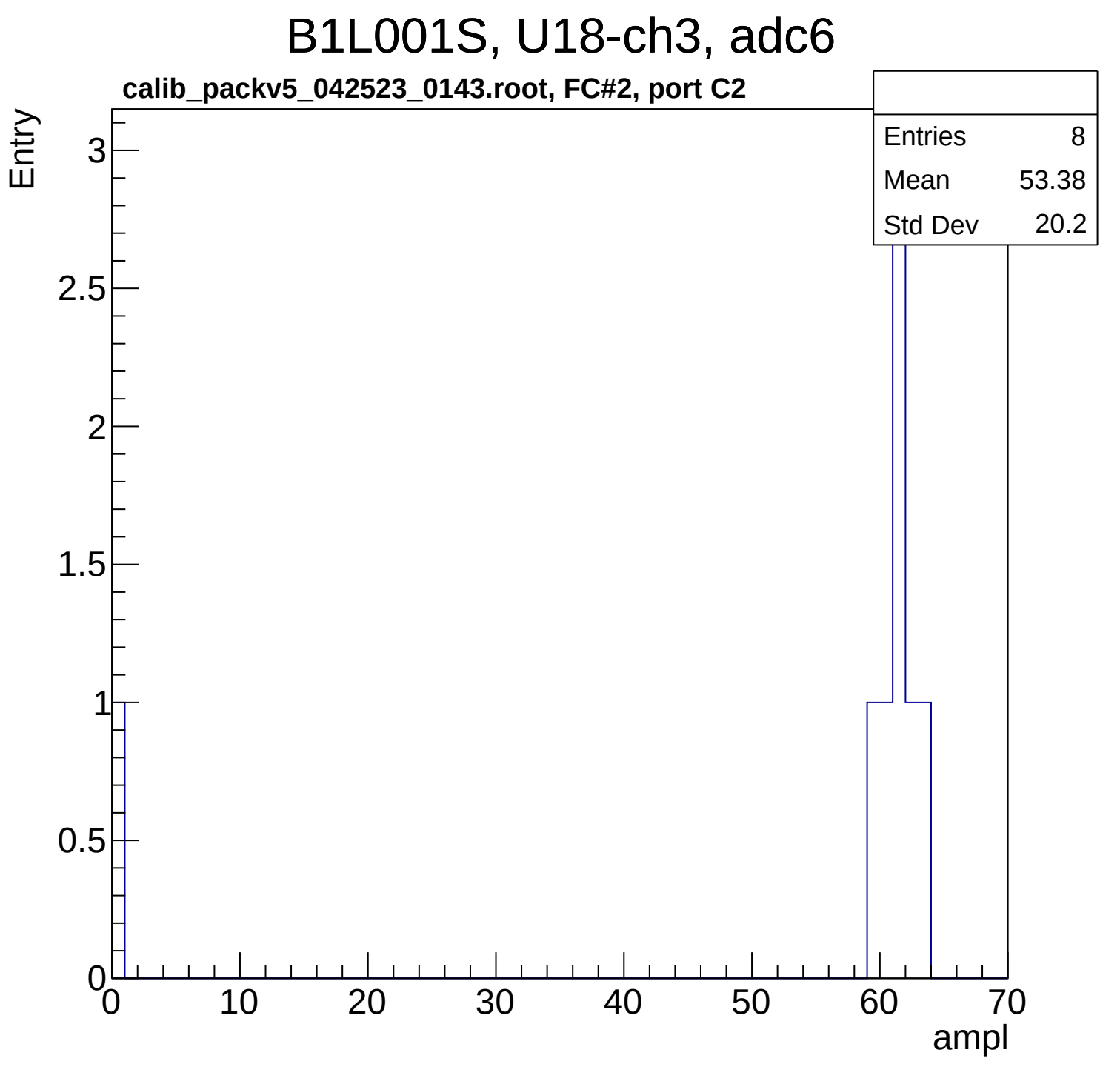

B1L001S, U18-ch3, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 117
Mean 36.43
Std Dev 3.36
Gaus mean : 37.0180
Gaus Width: 3.3915
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

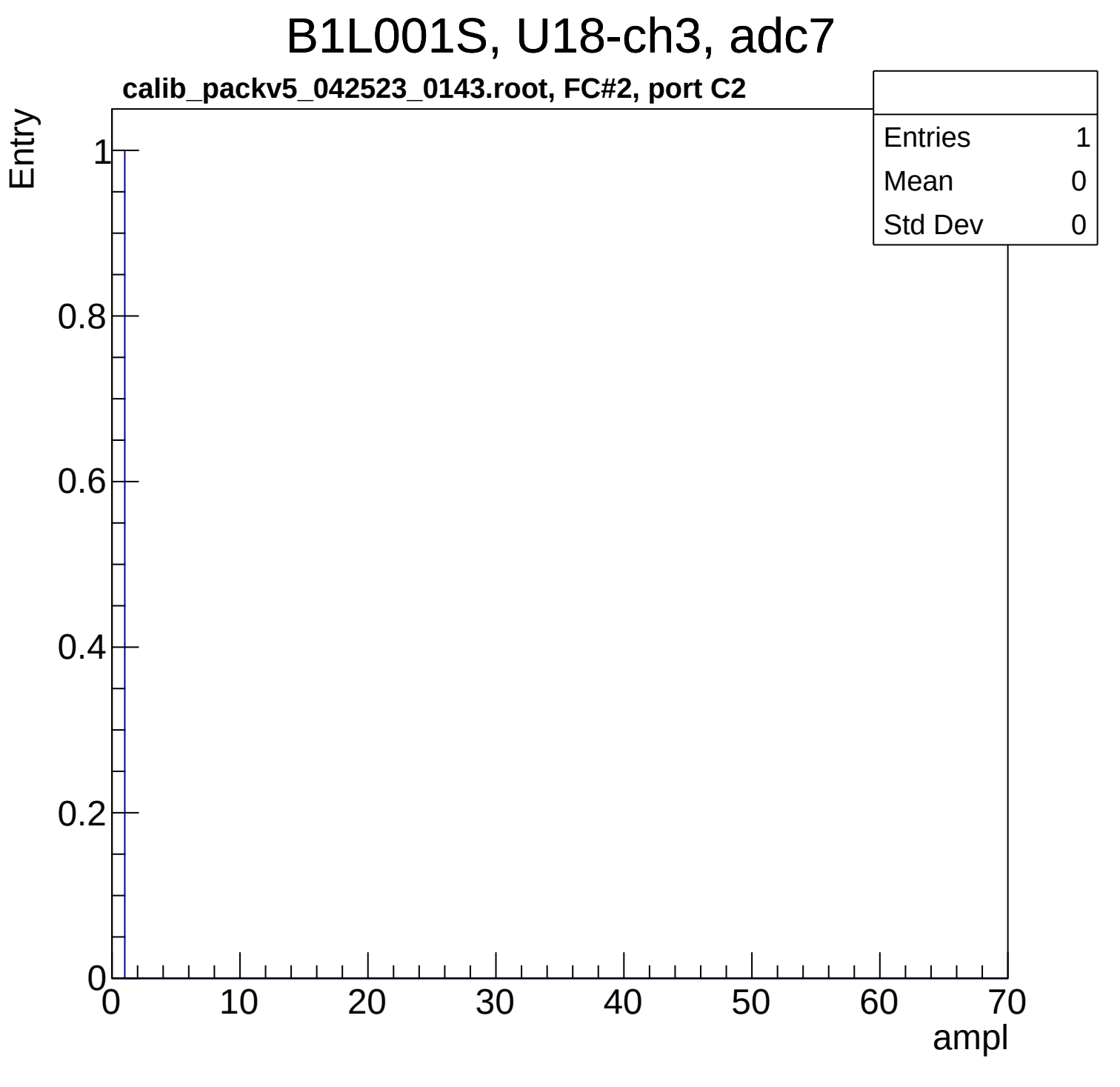

B1L001S, U18-ch3, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 150
Mean 42.95
Std Dev 3.455
Gaus mean : 43.5763
Gaus Width: 3.6640
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

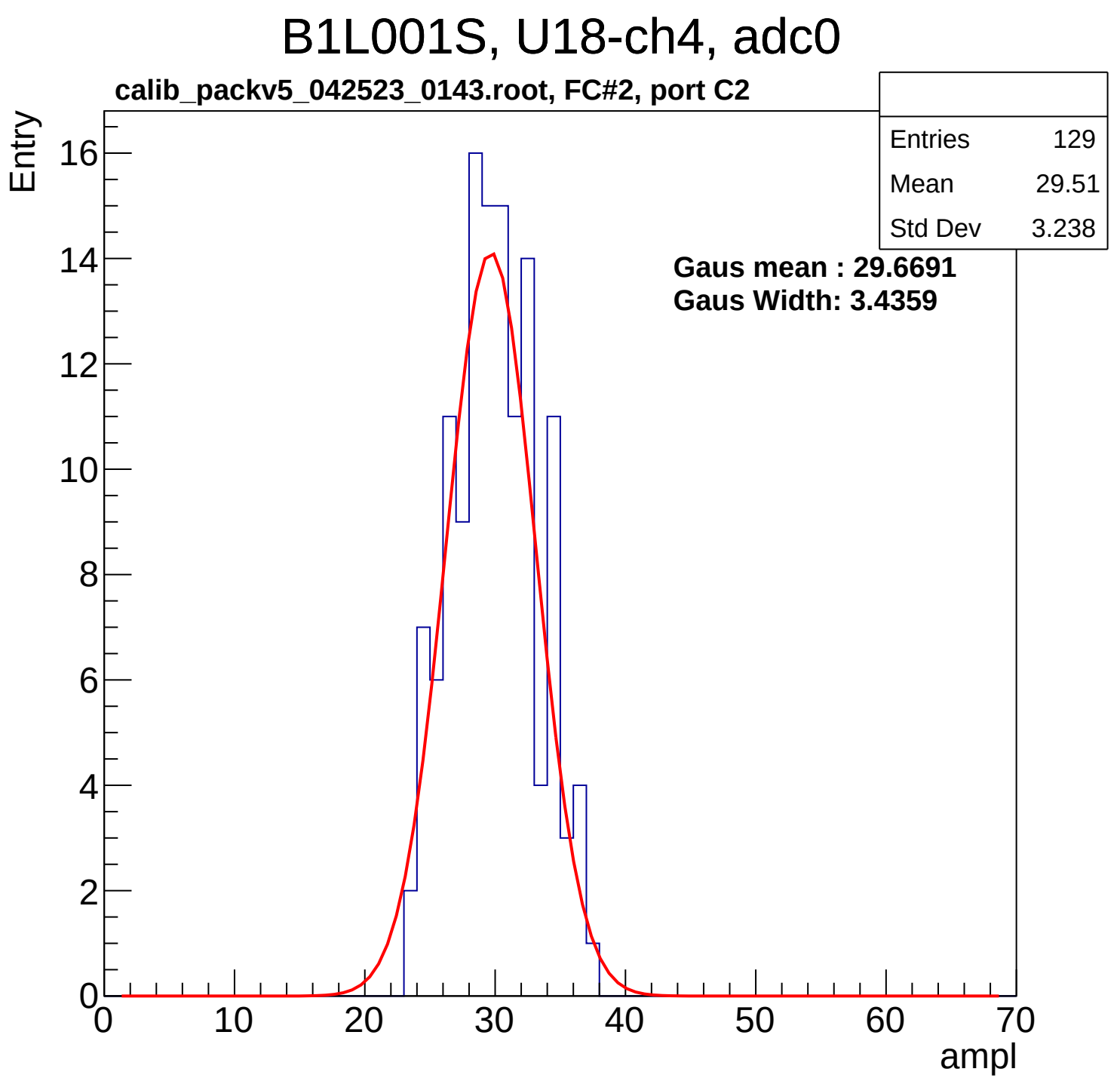

B1L001S, U18-ch3, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 126
Mean 50.09
Std Dev 3.352
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

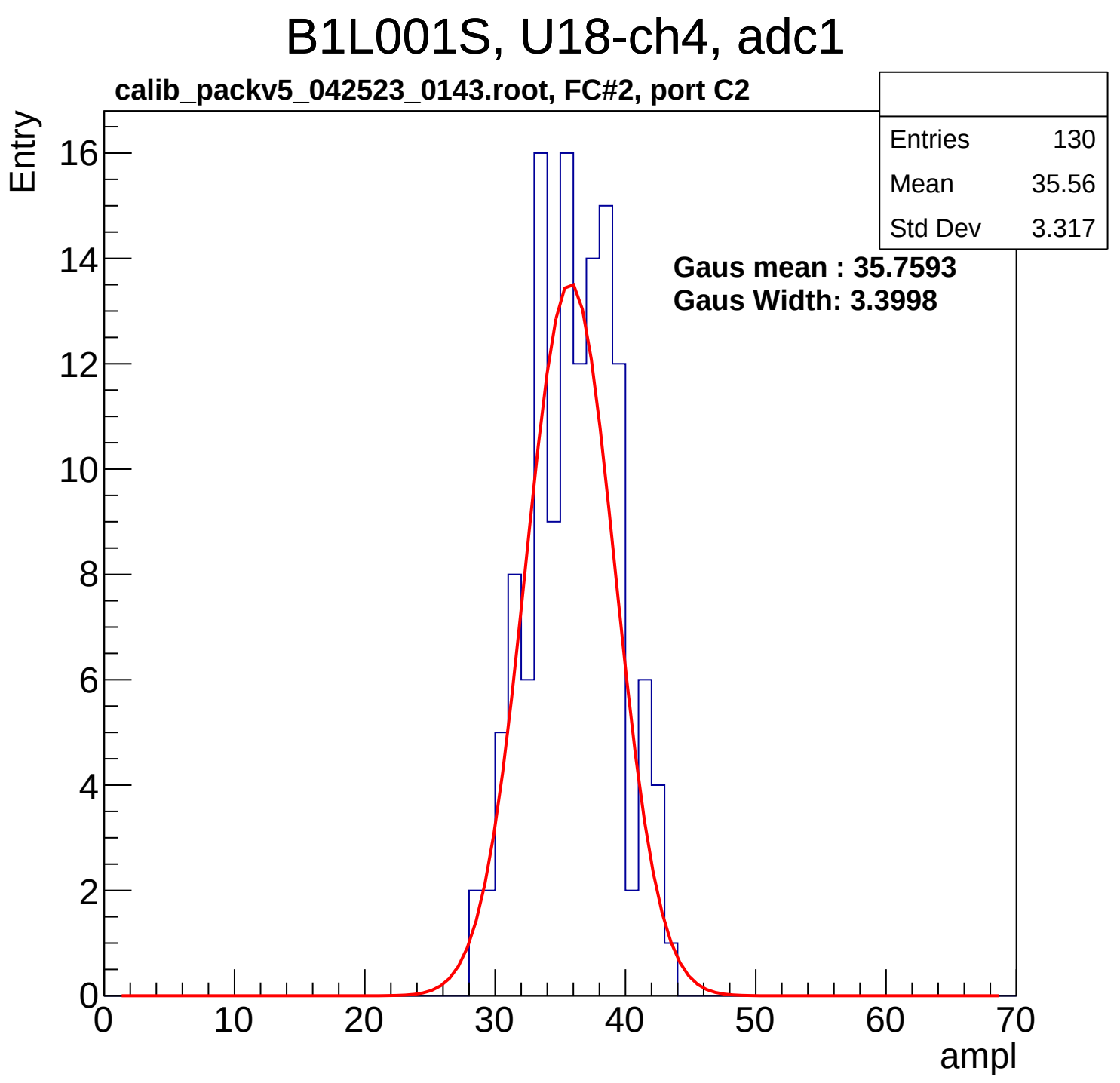

B1L001S, U18-ch3, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 122
Mean 56.24
Std Dev 3.507
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

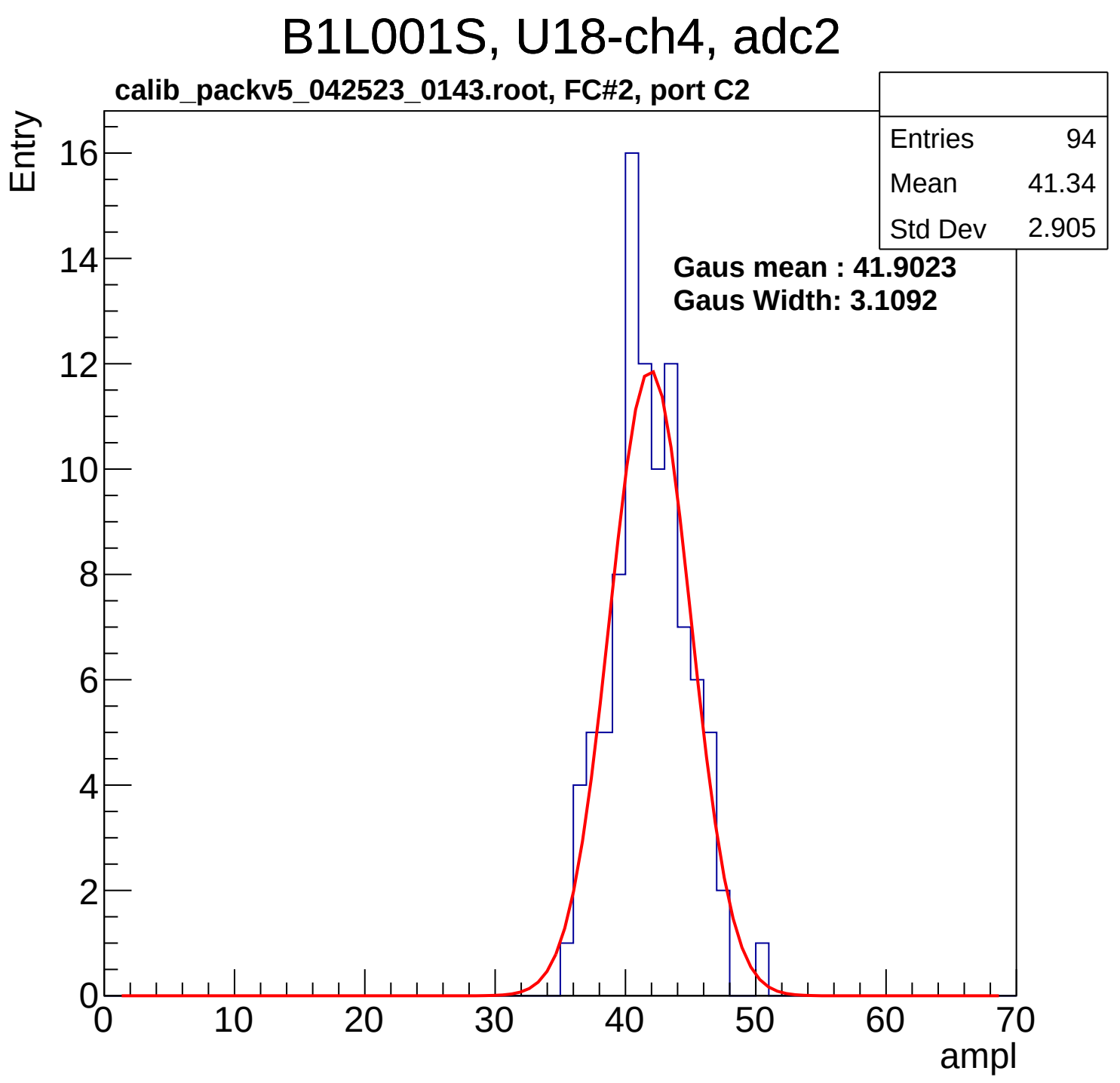

B1L001S, U18-ch3, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 80
Mean 59.36
Std Dev 7.14
Entry
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl

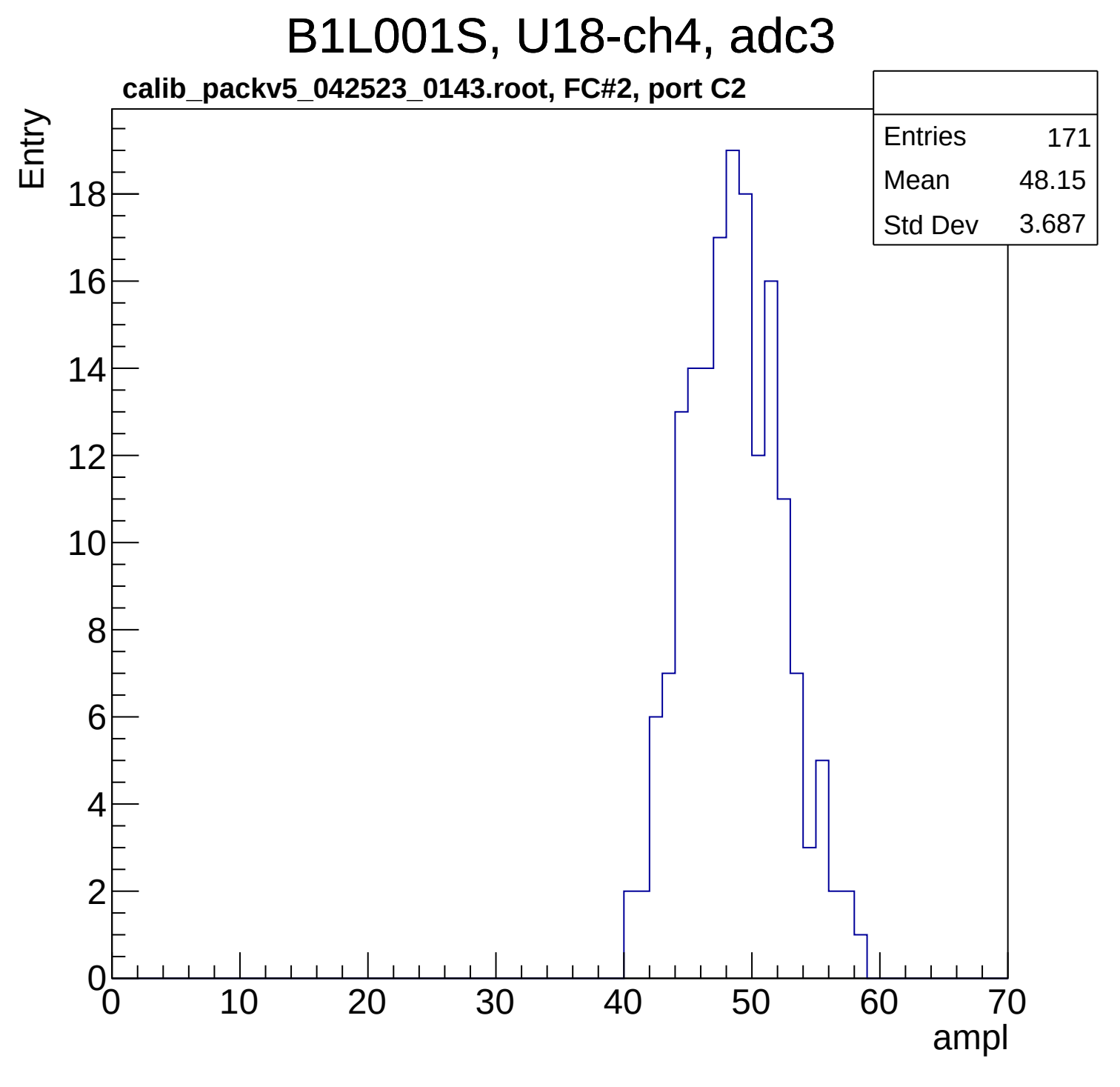

B1L001S, U18-ch3, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 8
Mean 53.38
Std Dev 20.2
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

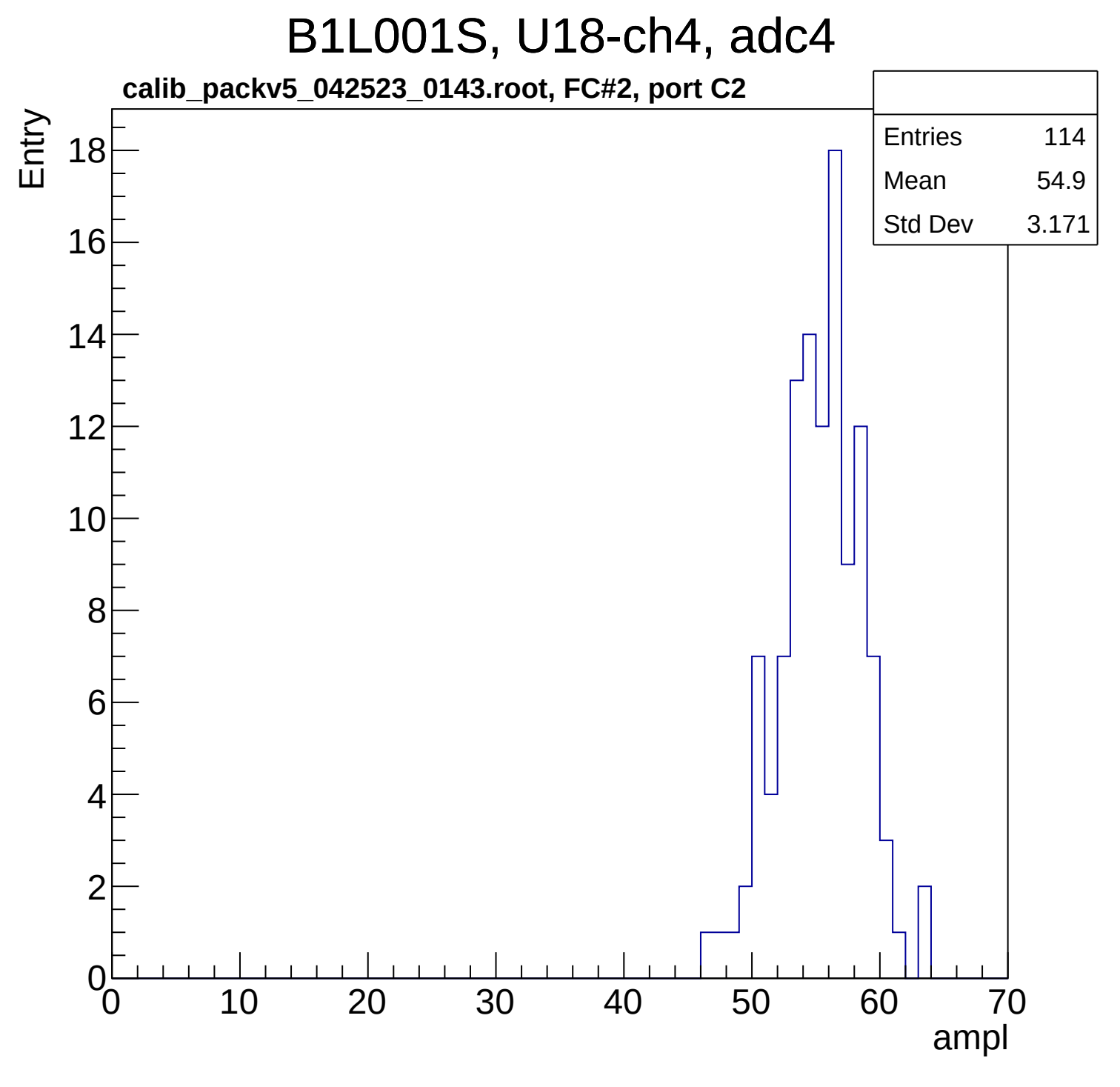

B1L001S, U18-ch3, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

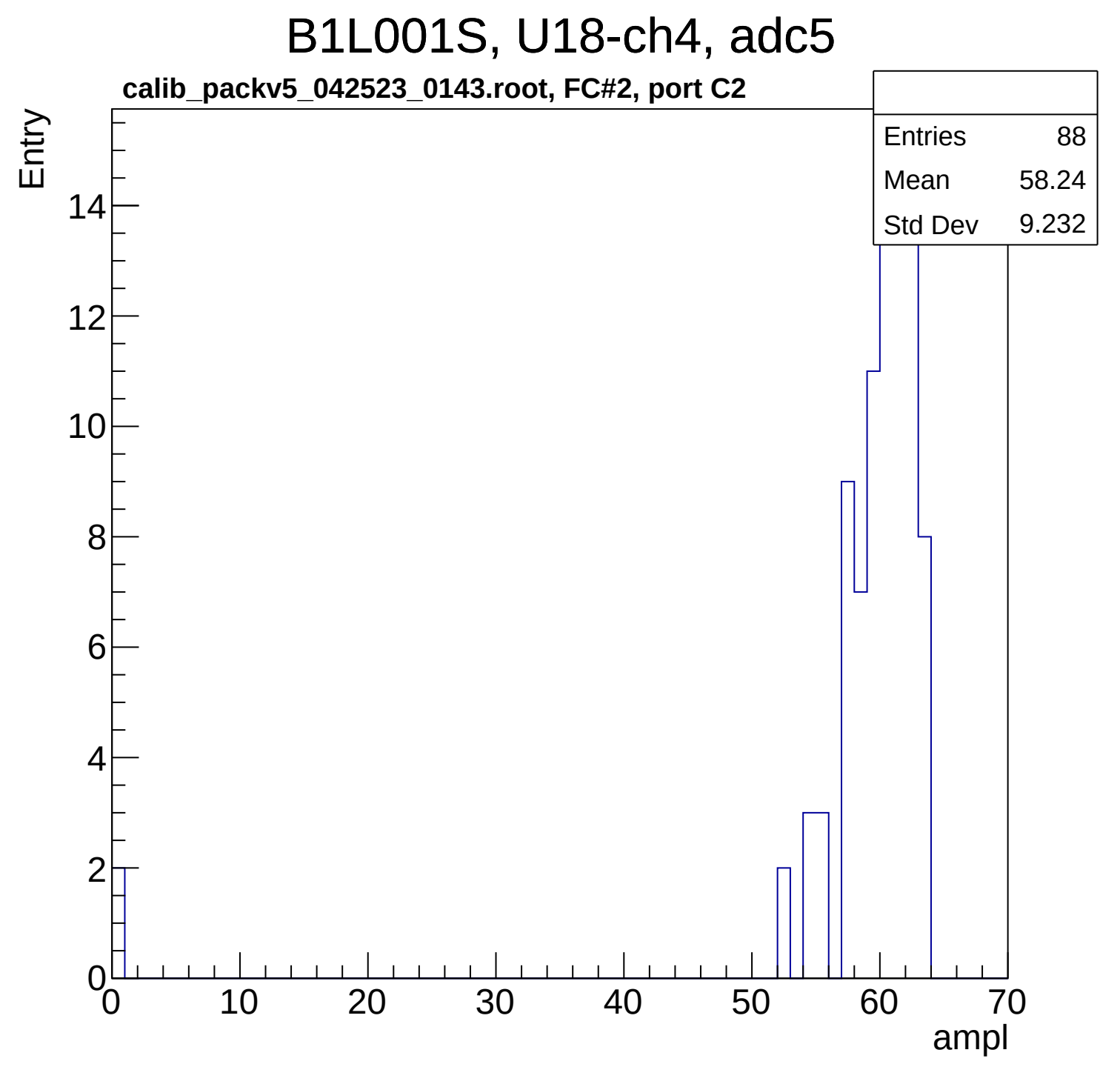

B1L001S, U18-ch4, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 129
Mean 29.51
Std Dev 3.238
Gaus mean : 29.6691
Gaus Width: 3.4359
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

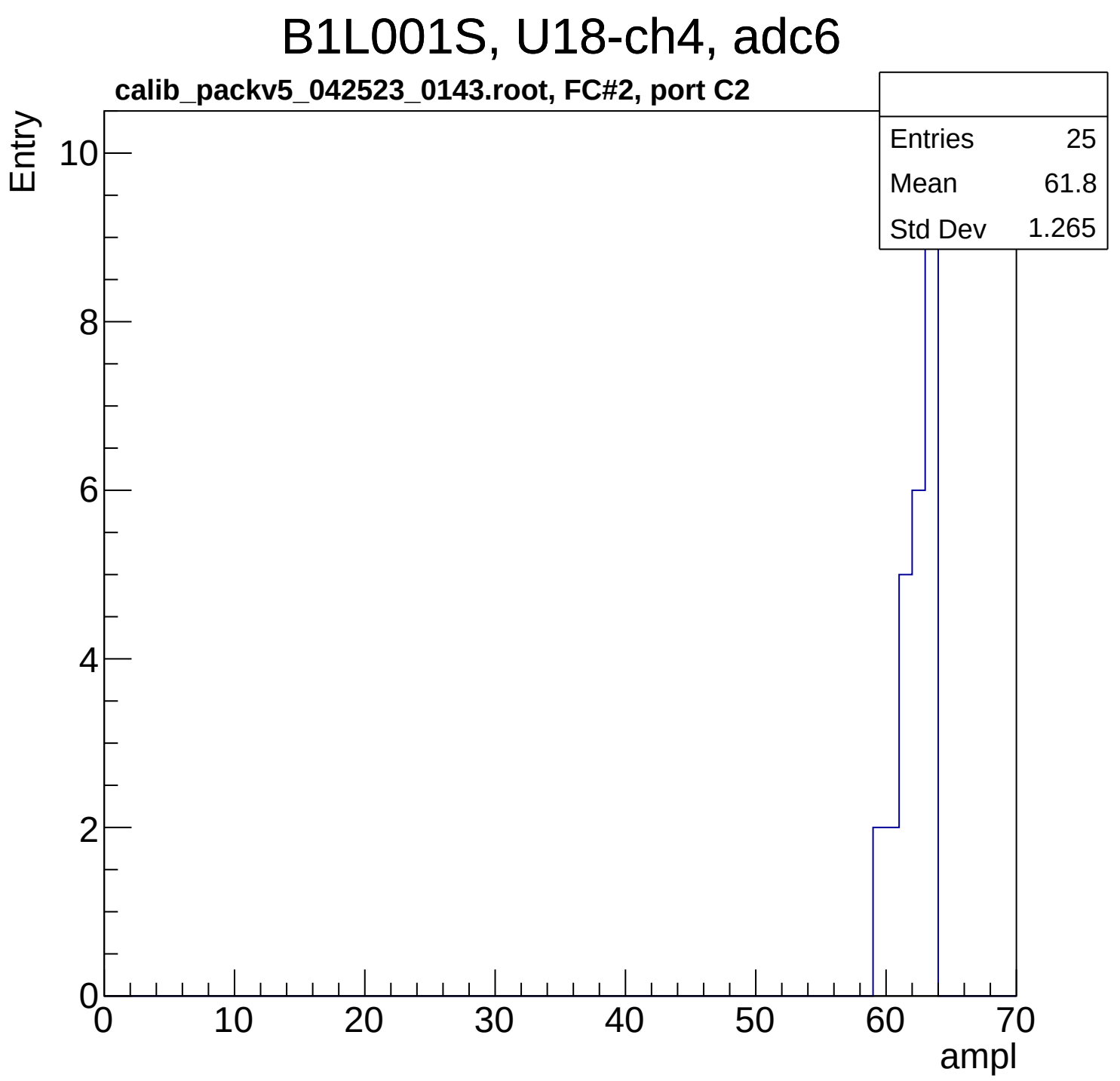

B1L001S, U18-ch4, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 130
Mean 35.56
Std Dev 3.317
Gaus mean : 35.7593
Gaus Width: 3.3998
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

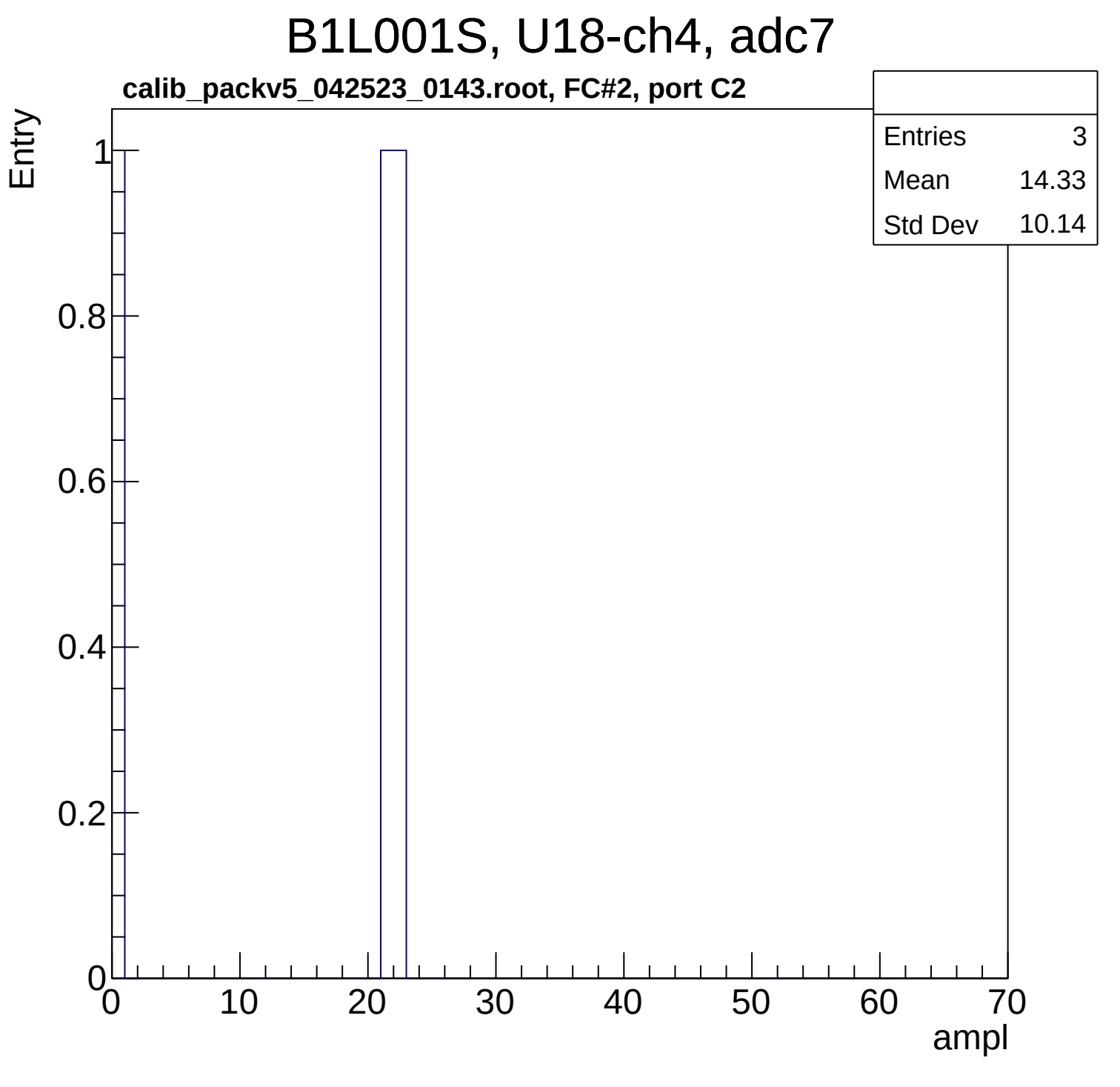

B1L001S, U18-ch4, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 94
Mean 41.34
Std Dev 2.905
Gaus mean : 41.9023
Gaus Width: 3.1092
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

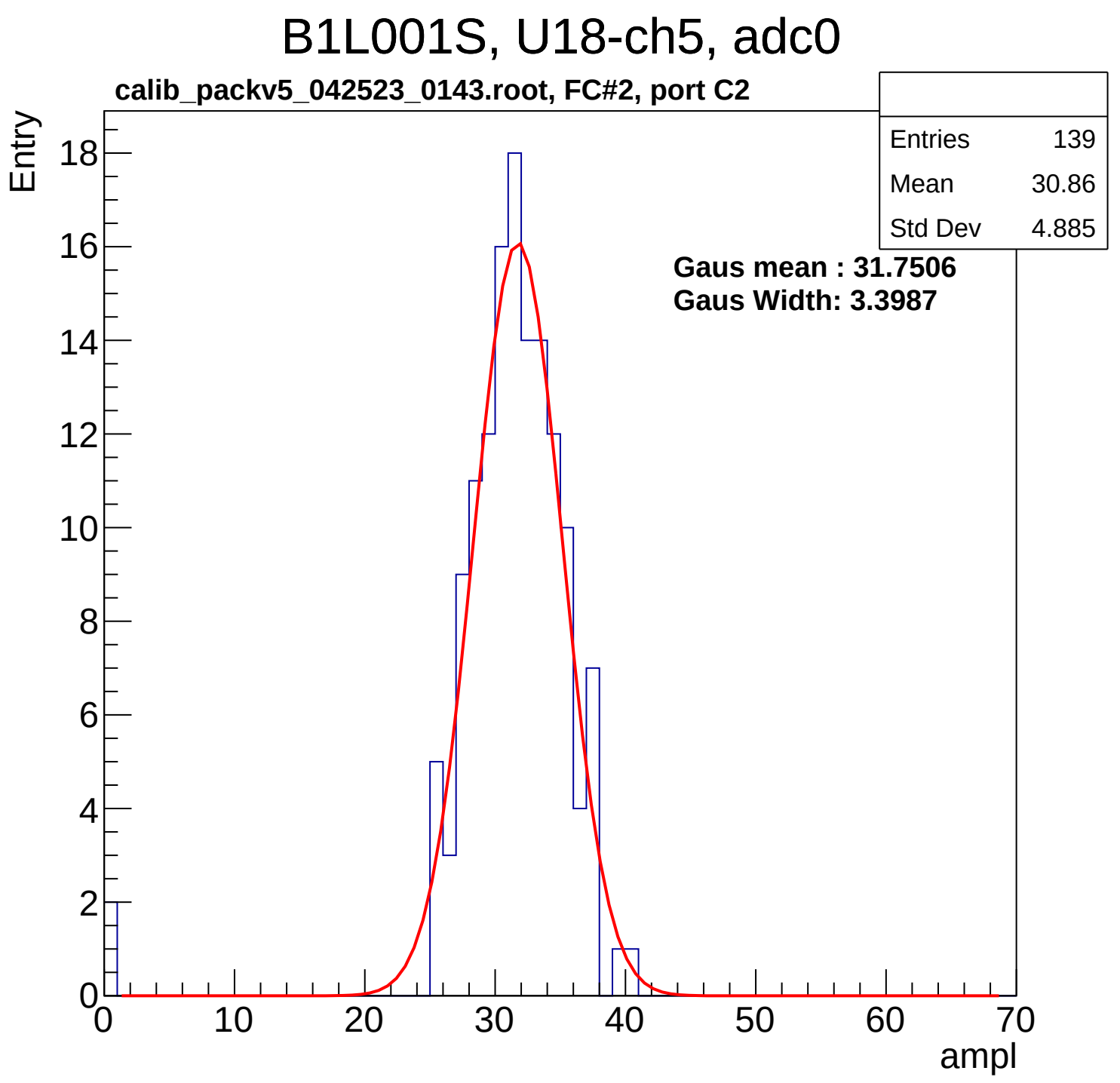

B1L001S, U18-ch4, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 171
Mean 48.15
Std Dev 3.687
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

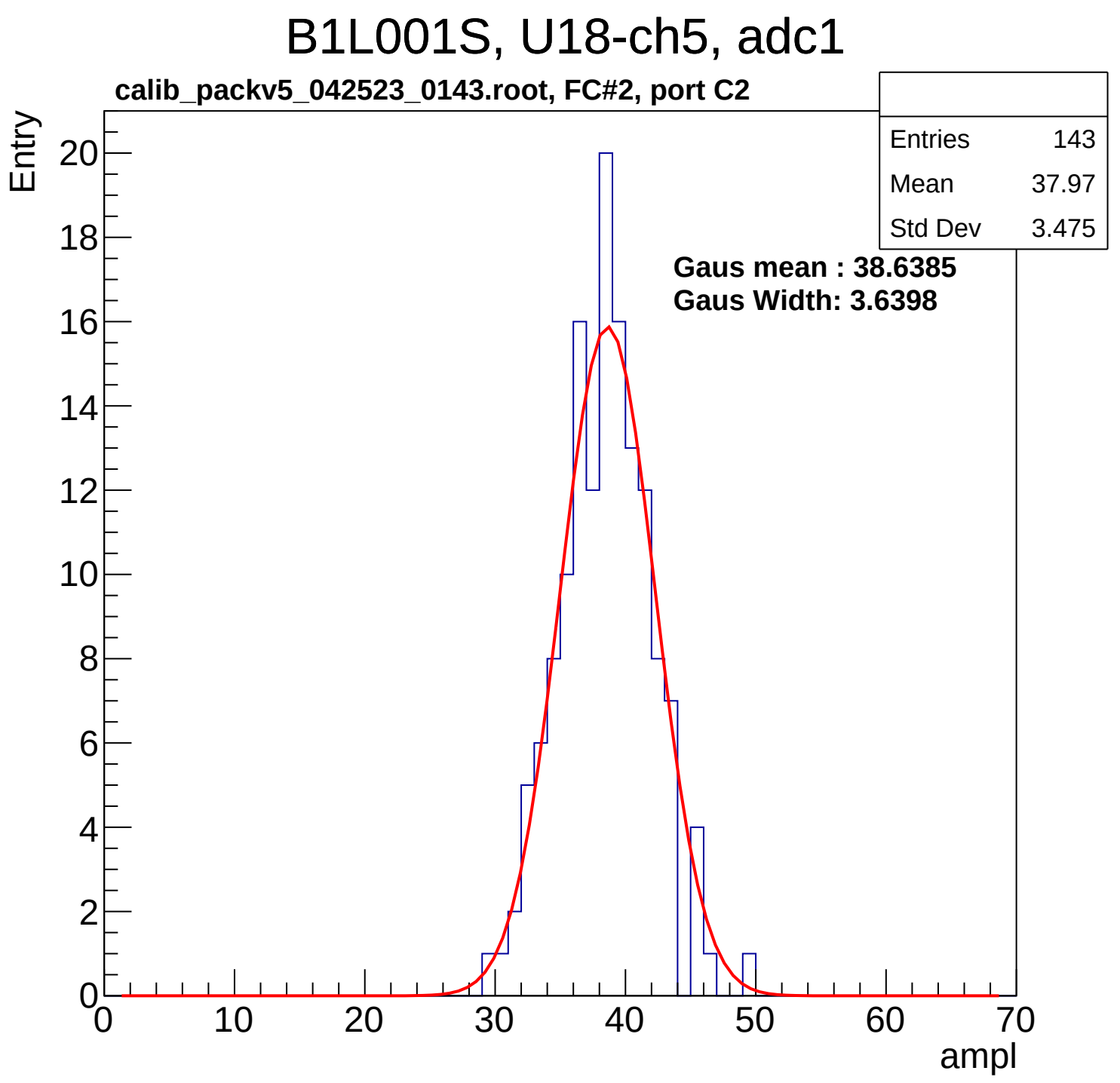

B1L001S, U18-ch4, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 114
Mean 54.9
Std Dev 3.171
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

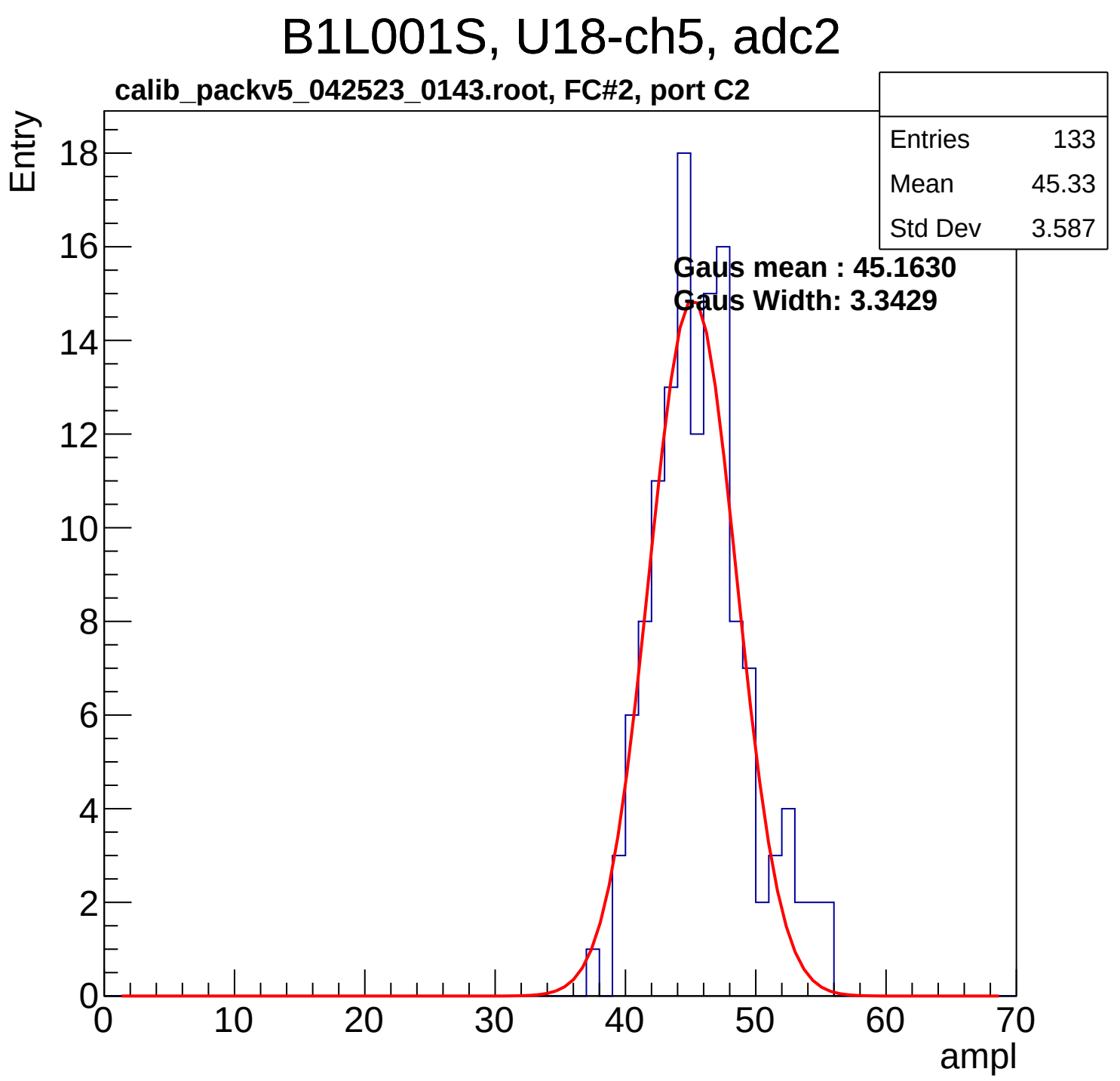

B1L001S, U18-ch4, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 88
Mean 58.24
Std Dev 9.232
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl

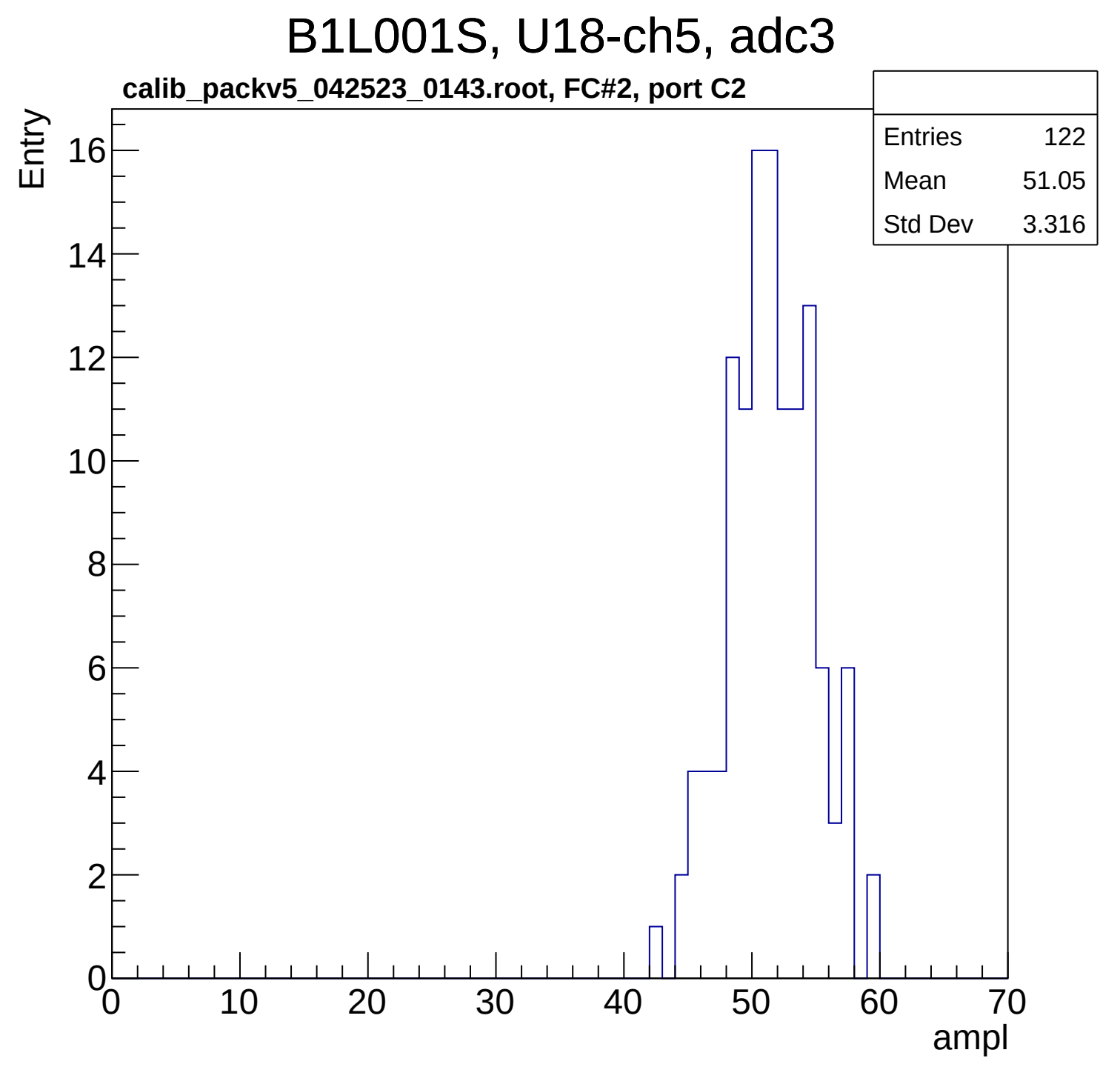

B1L001S, U18-ch4, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 25
Mean 61.8
Std Dev 1.265
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

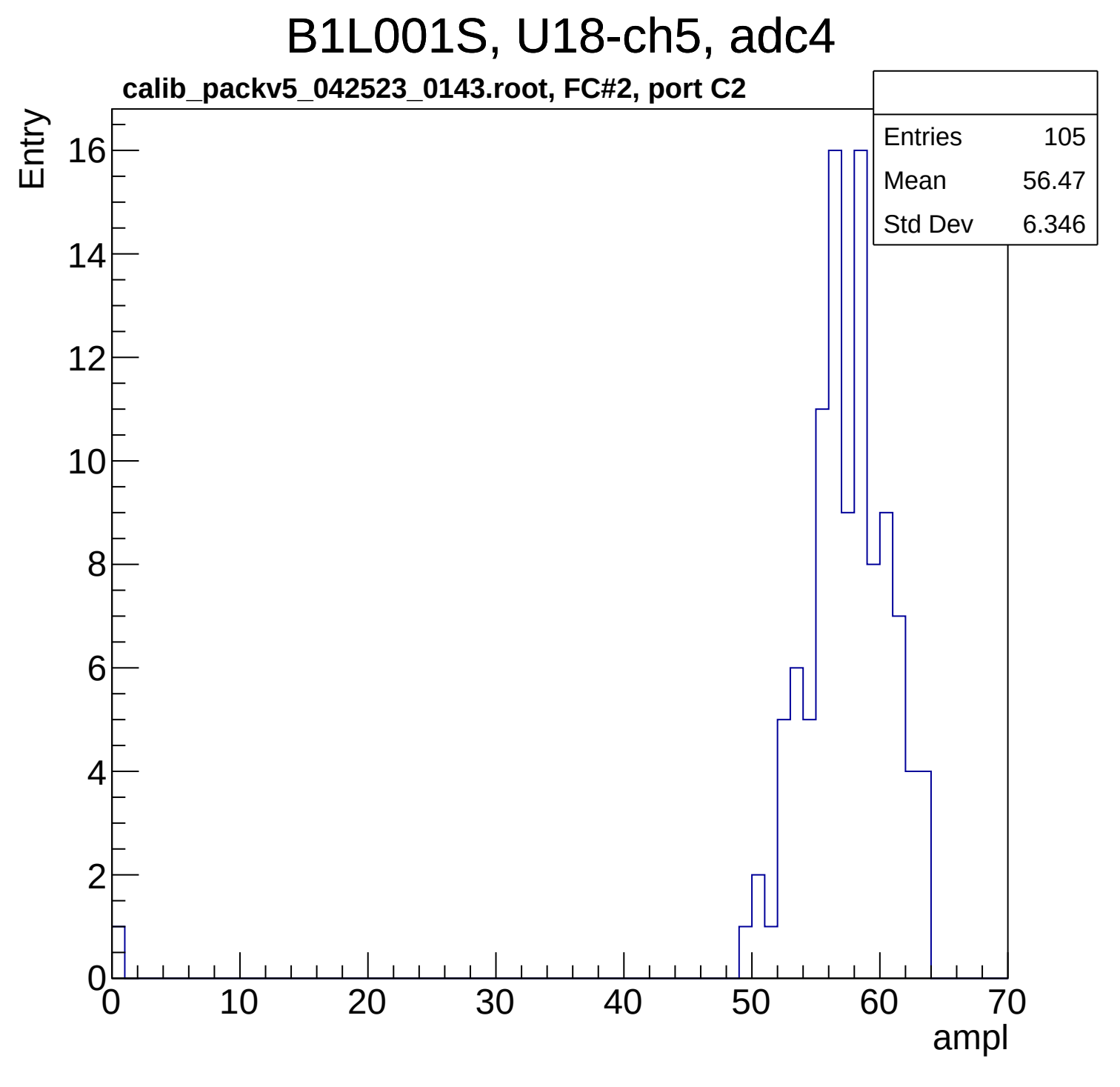

B1L001S, U18-ch4, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 3
Mean 14.33
Std Dev 10.14
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70

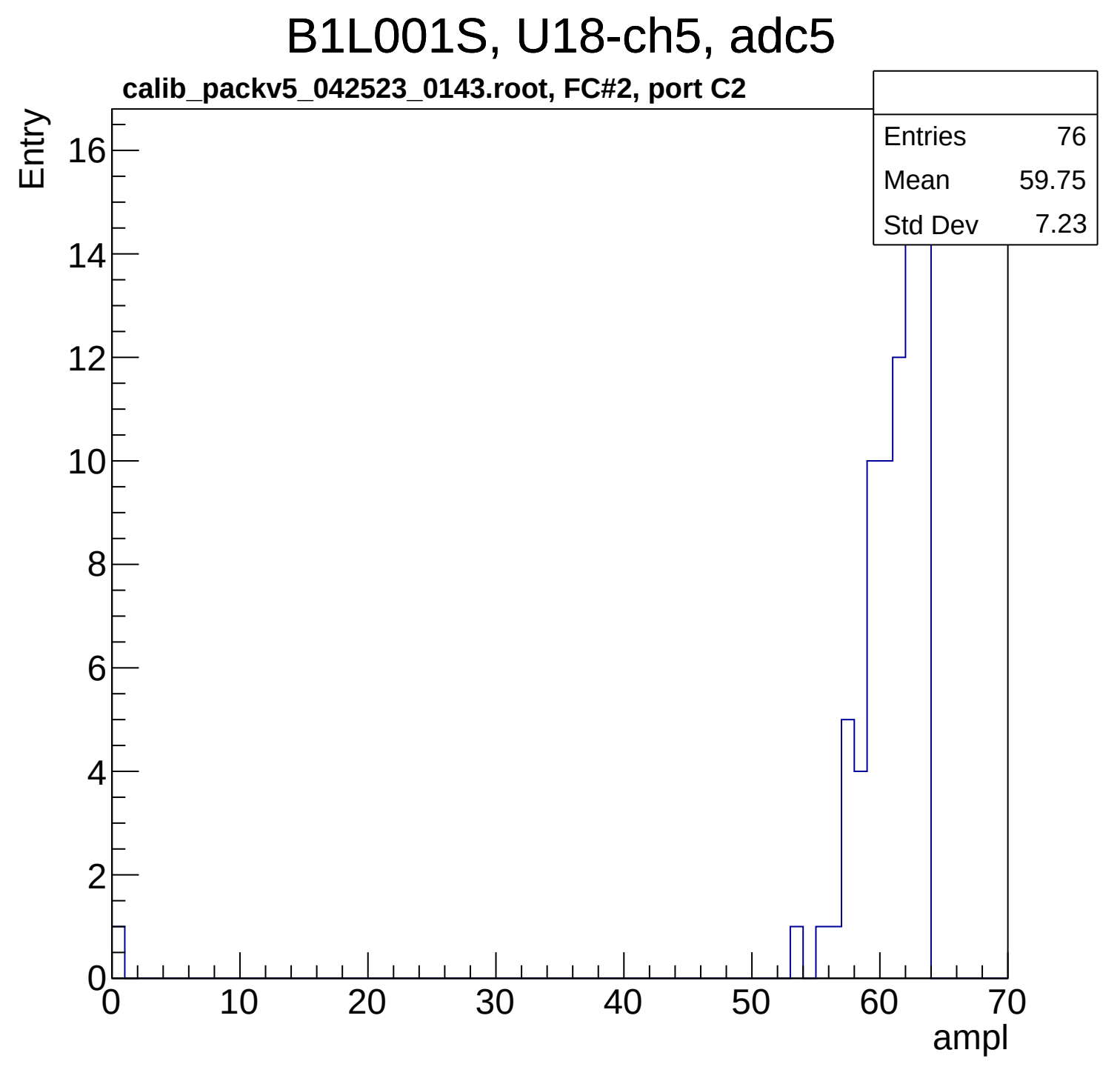

B1L001S, U18-ch5, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 139
Mean 30.86
Std Dev 4.885
Gaus mean : 31.7506
Gaus Width: 3.3987
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

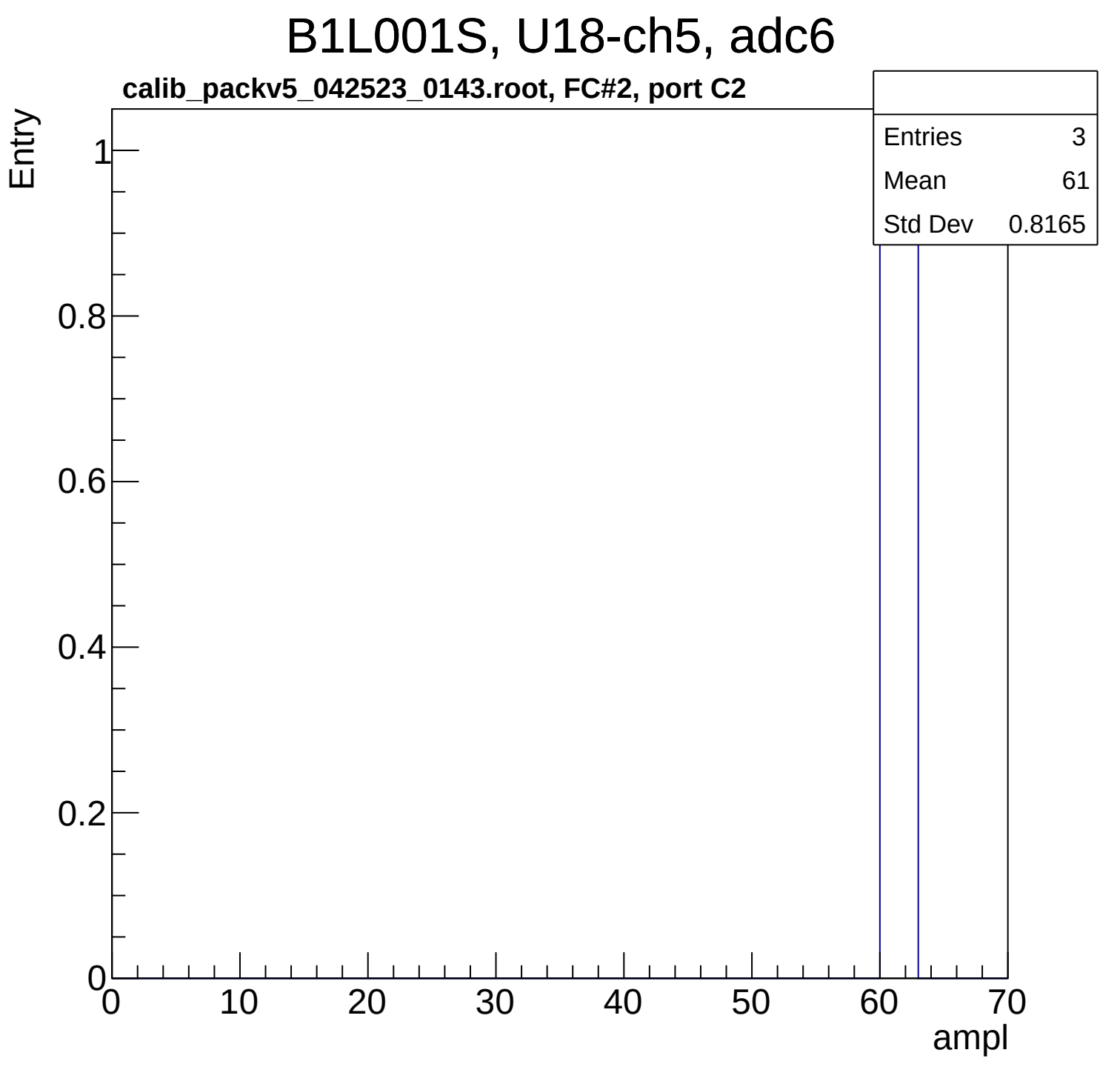

B1L001S, U18-ch5, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 143
Mean 37.97
Std Dev 3.475
Gaus mean : 38.6385
Gaus Width: 3.6398
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

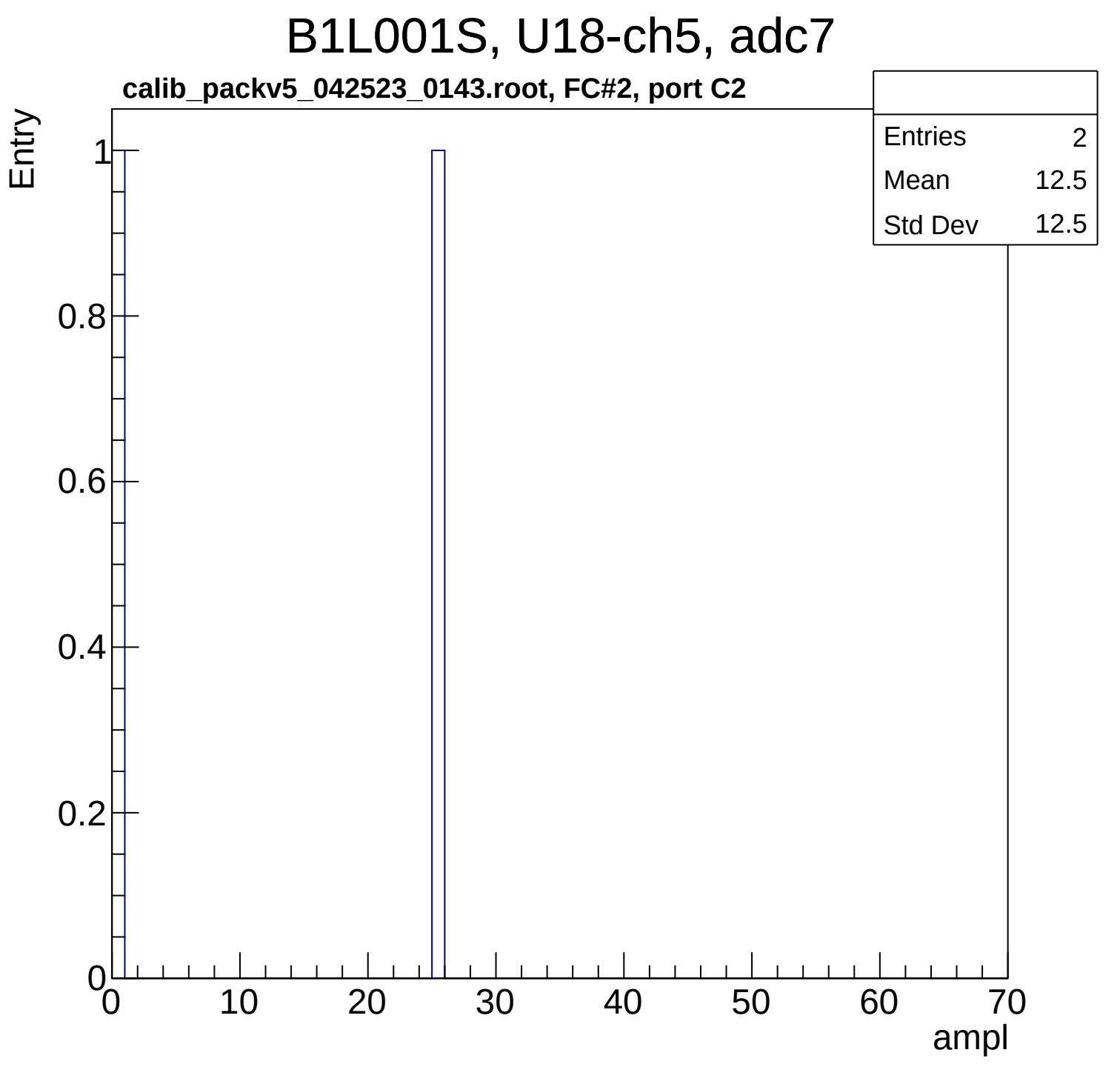

B1L001S, U18-ch5, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 133
Mean 45.33
Std Dev 3.587
Gaus mean : 45.1630
Gaus Width: 3.3429
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

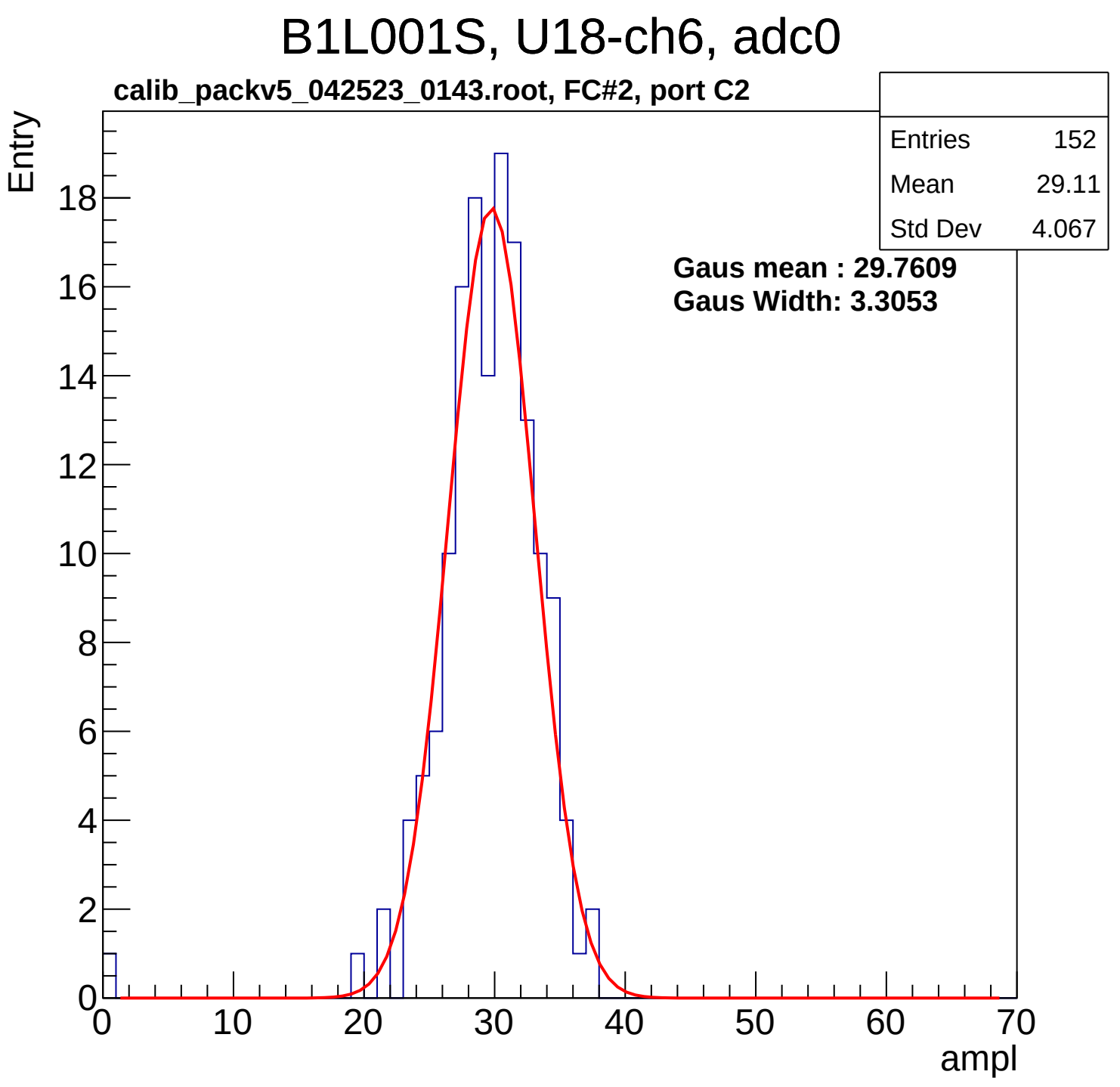

B1L001S, U18-ch5, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 122
Mean 51.05
Std Dev 3.316
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

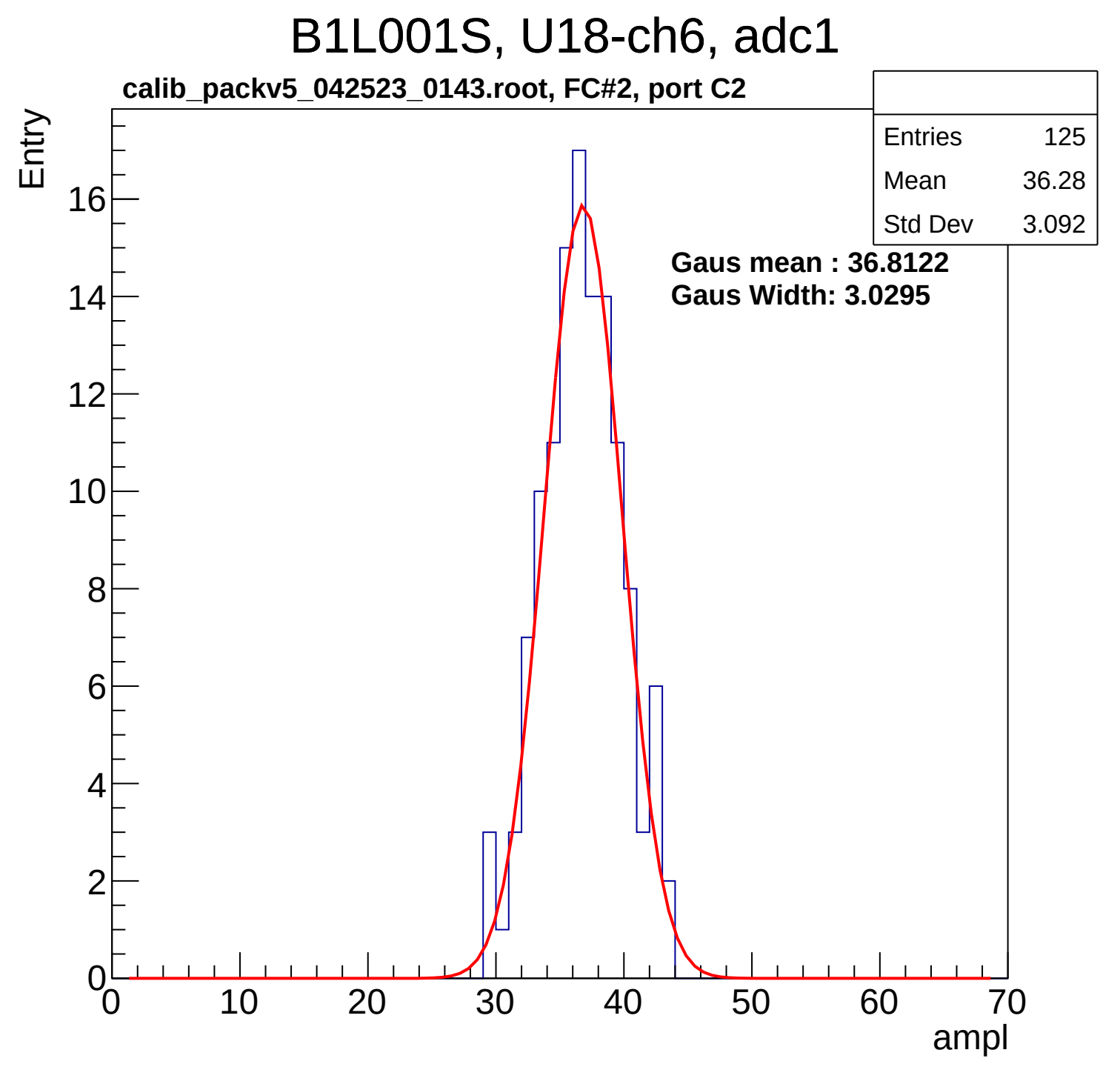

B1L001S, U18-ch5, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 105
Mean 56.47
Std Dev 6.346
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

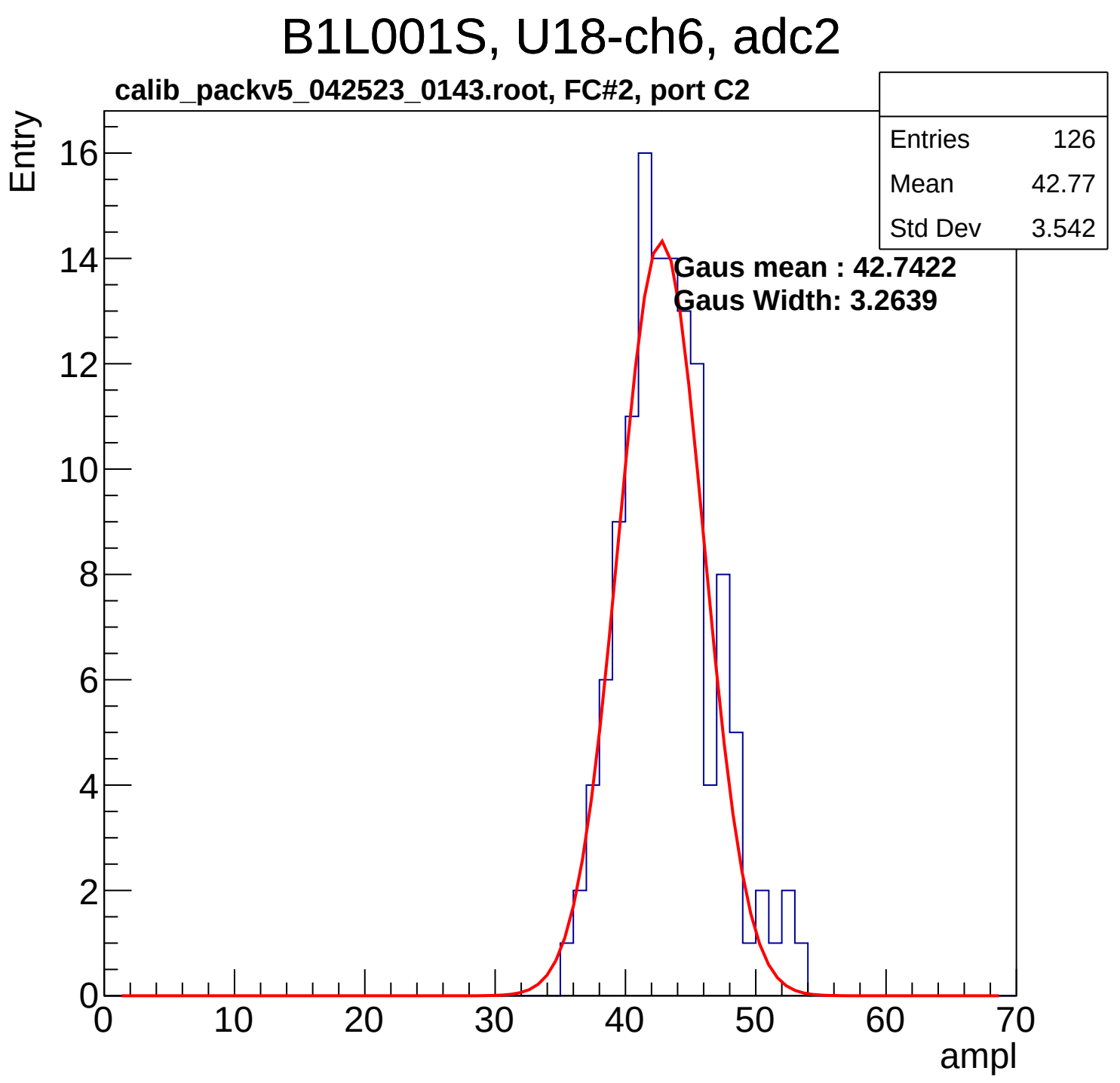

B1L001S, U18-ch5, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 76
Mean 59.75
Std Dev 7.23
Entry
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl

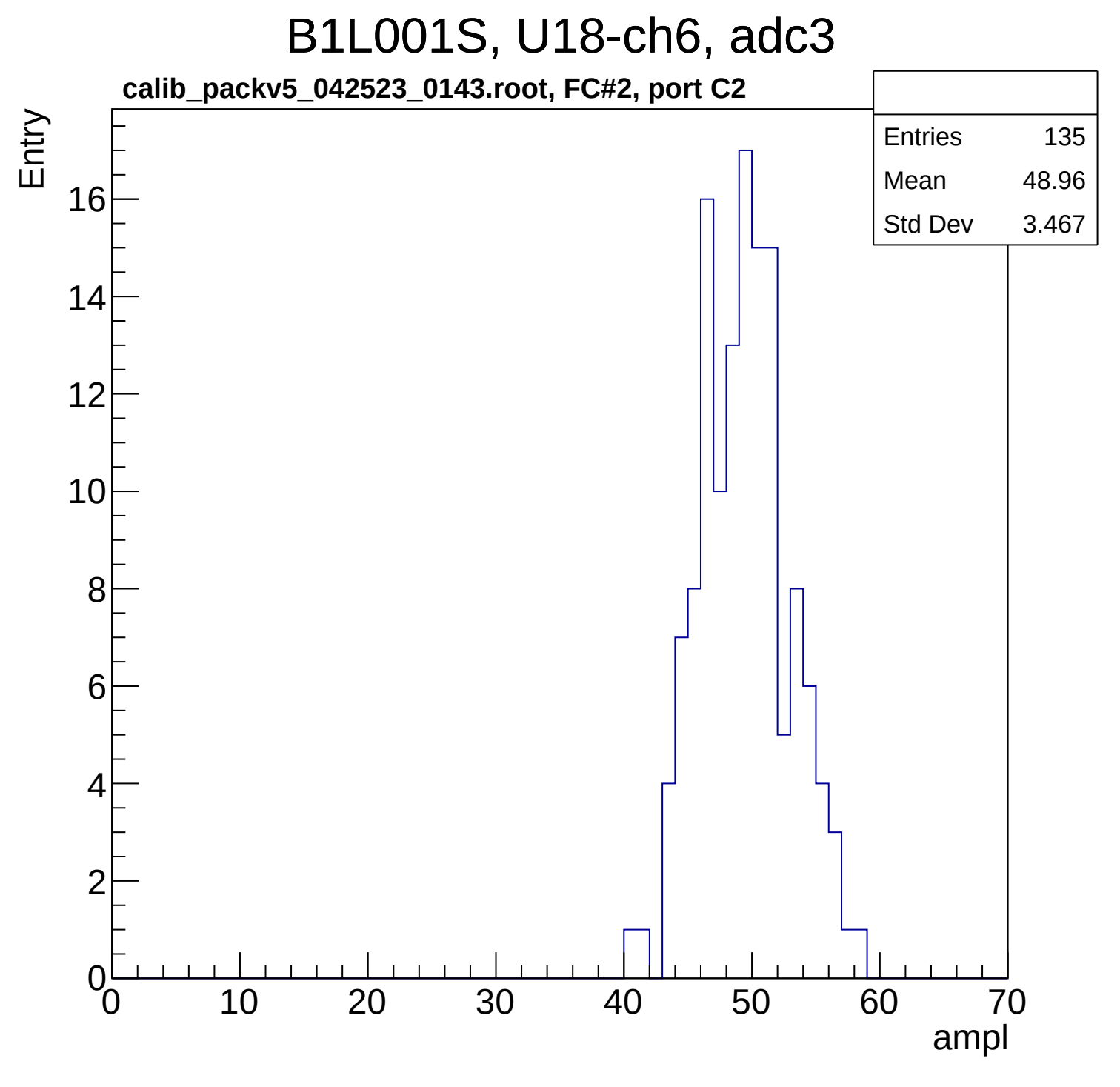

B1L001S, U18-ch5, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 3
Mean 61
Std Dev 0.8165
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

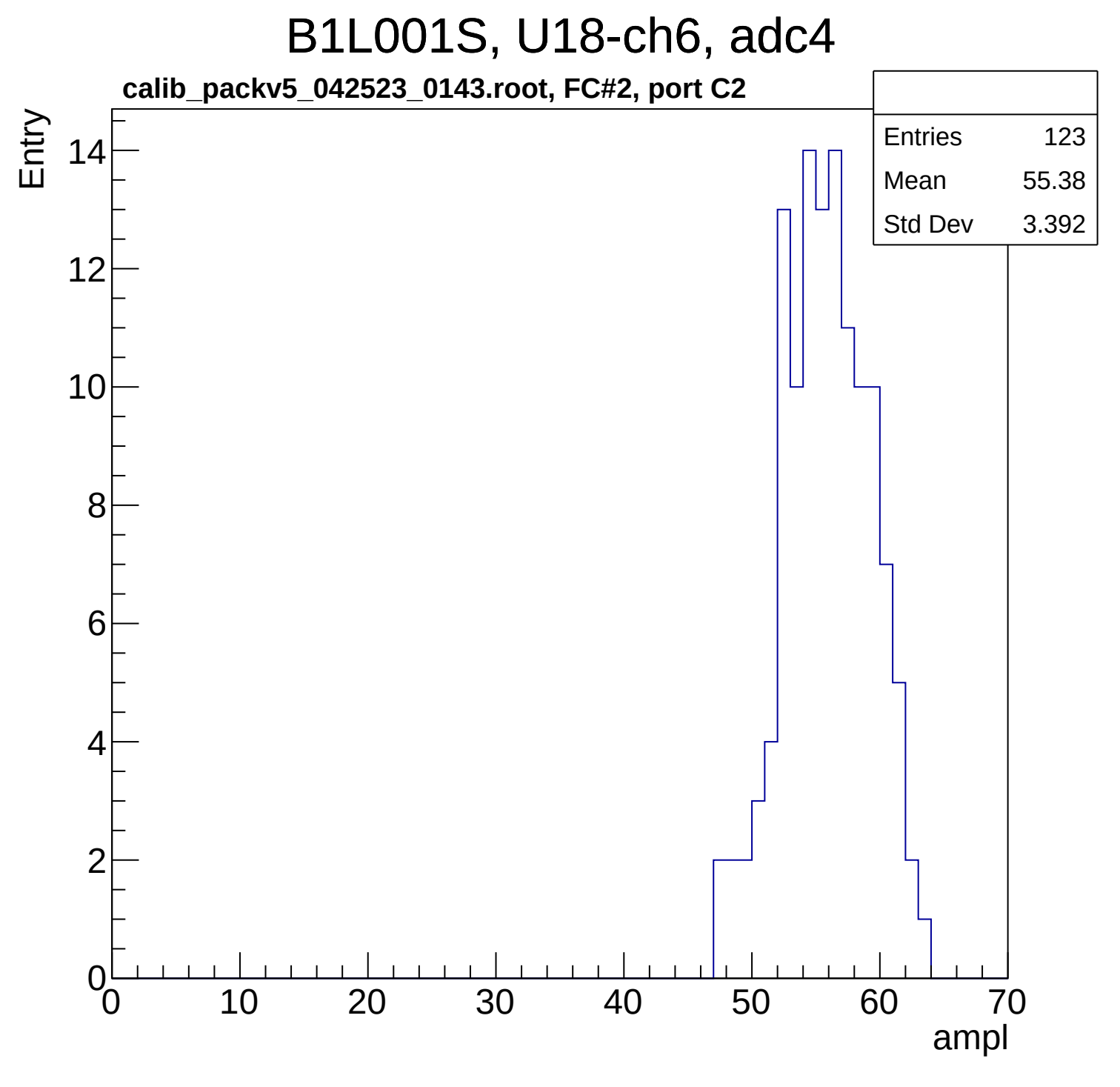

B1L001S, U18-ch5, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 12.5
Std Dev 12.5
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70

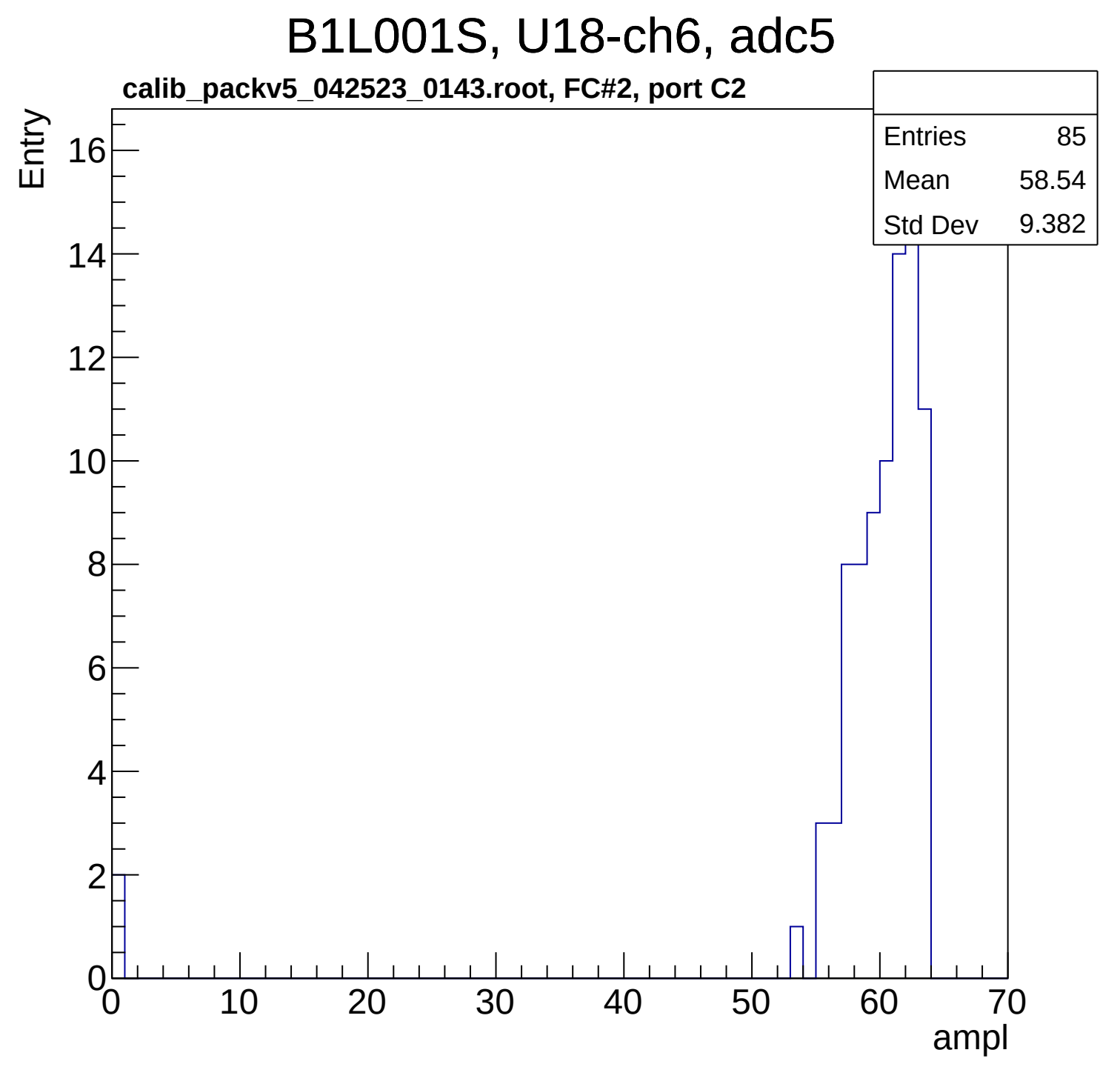

B1L001S, U18-ch6, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 152
Mean 29.11
Std Dev 4.067
Gaus mean : 29.7609
Gaus Width: 3.3053
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

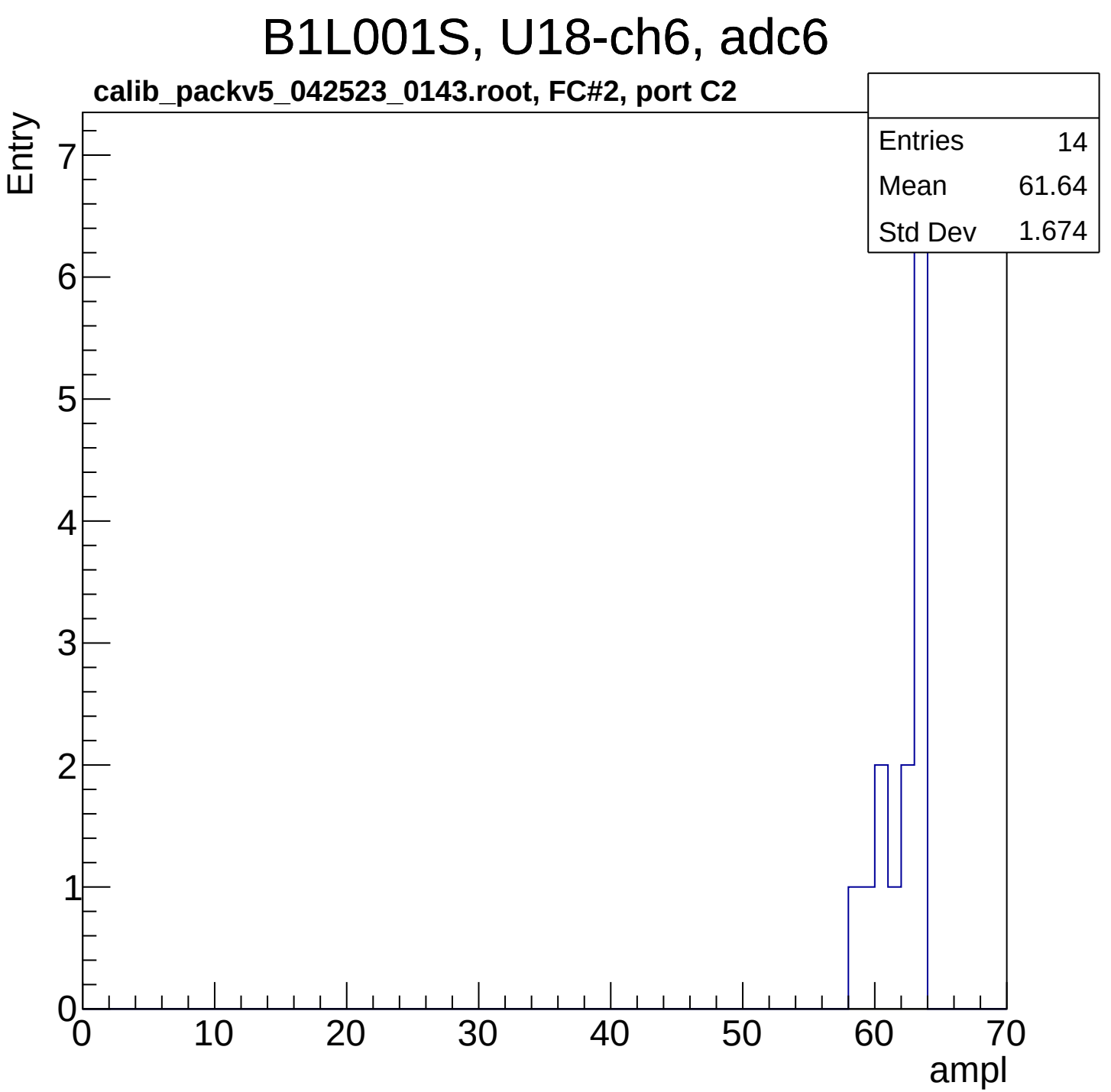

B1L001S, U18-ch6, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 125
Mean 36.28
Std Dev 3.092
Gaus mean : 36.8122
Gaus Width: 3.0295
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

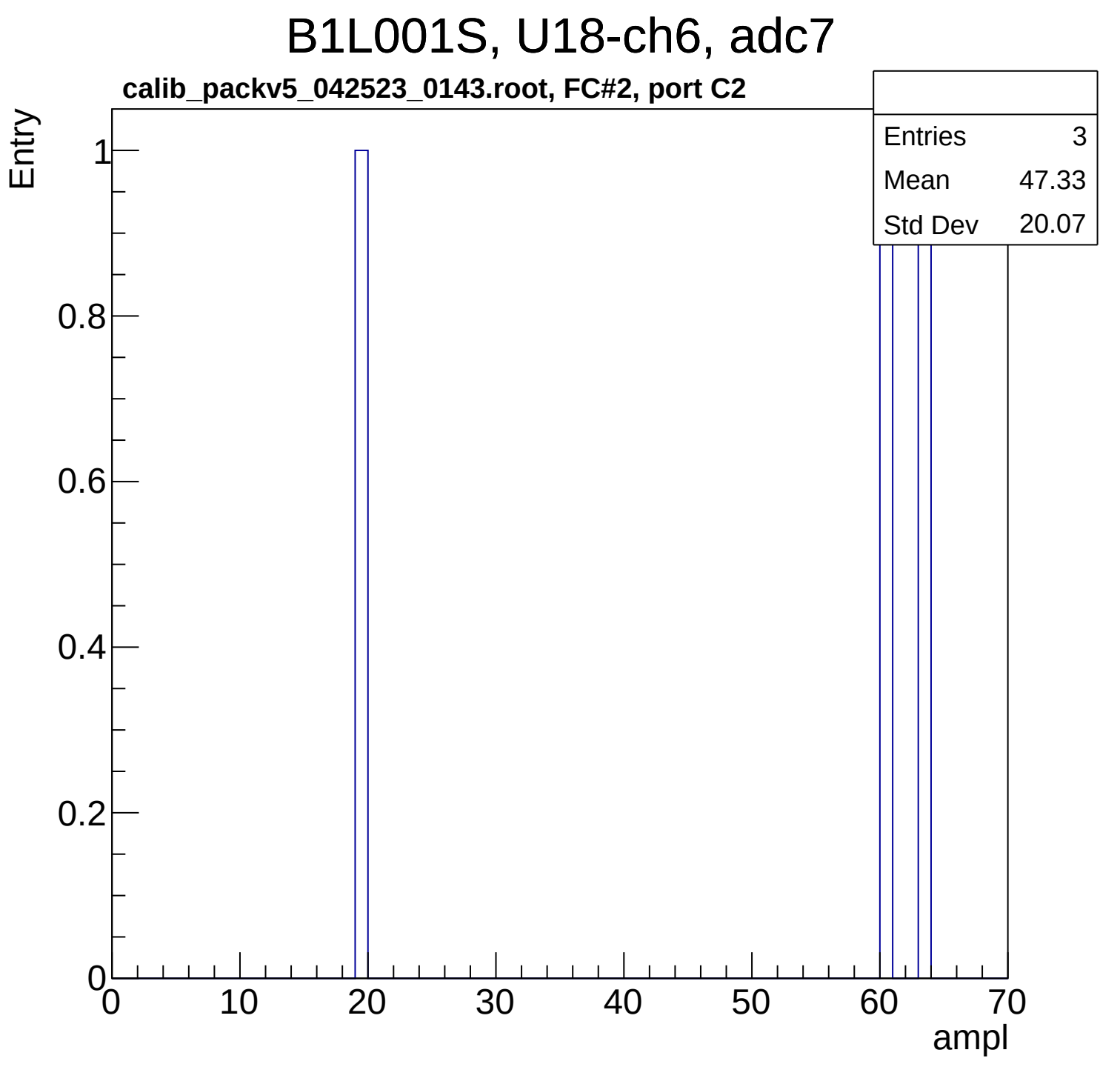

B1L001S, U18-ch6, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 126
Mean 42.77
Std Dev 3.542
Gaus mean : 42.7422
Gaus Width: 3.2639
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

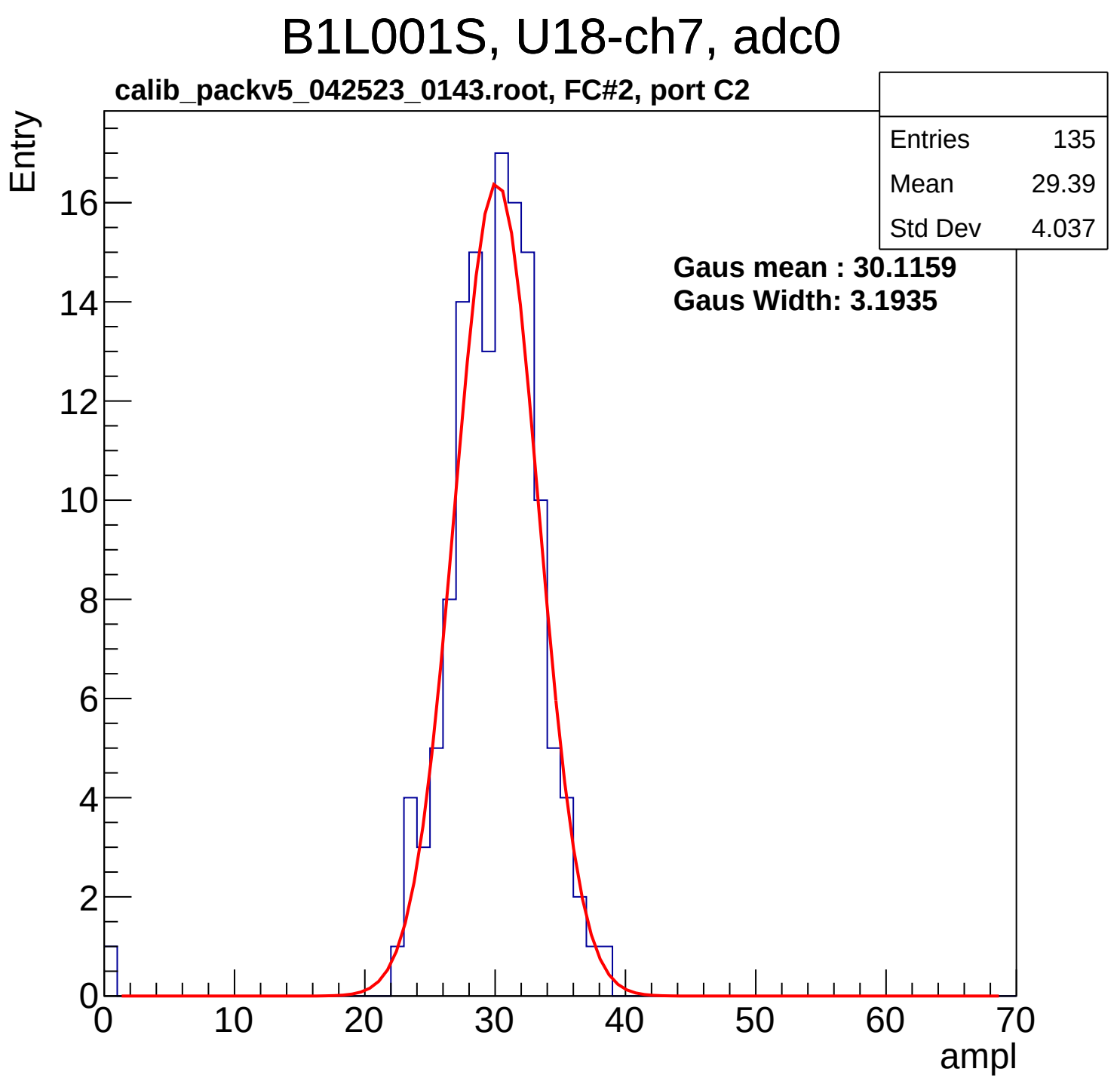

B1L001S, U18-ch6, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 135
Mean 48.96
Std Dev 3.467
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

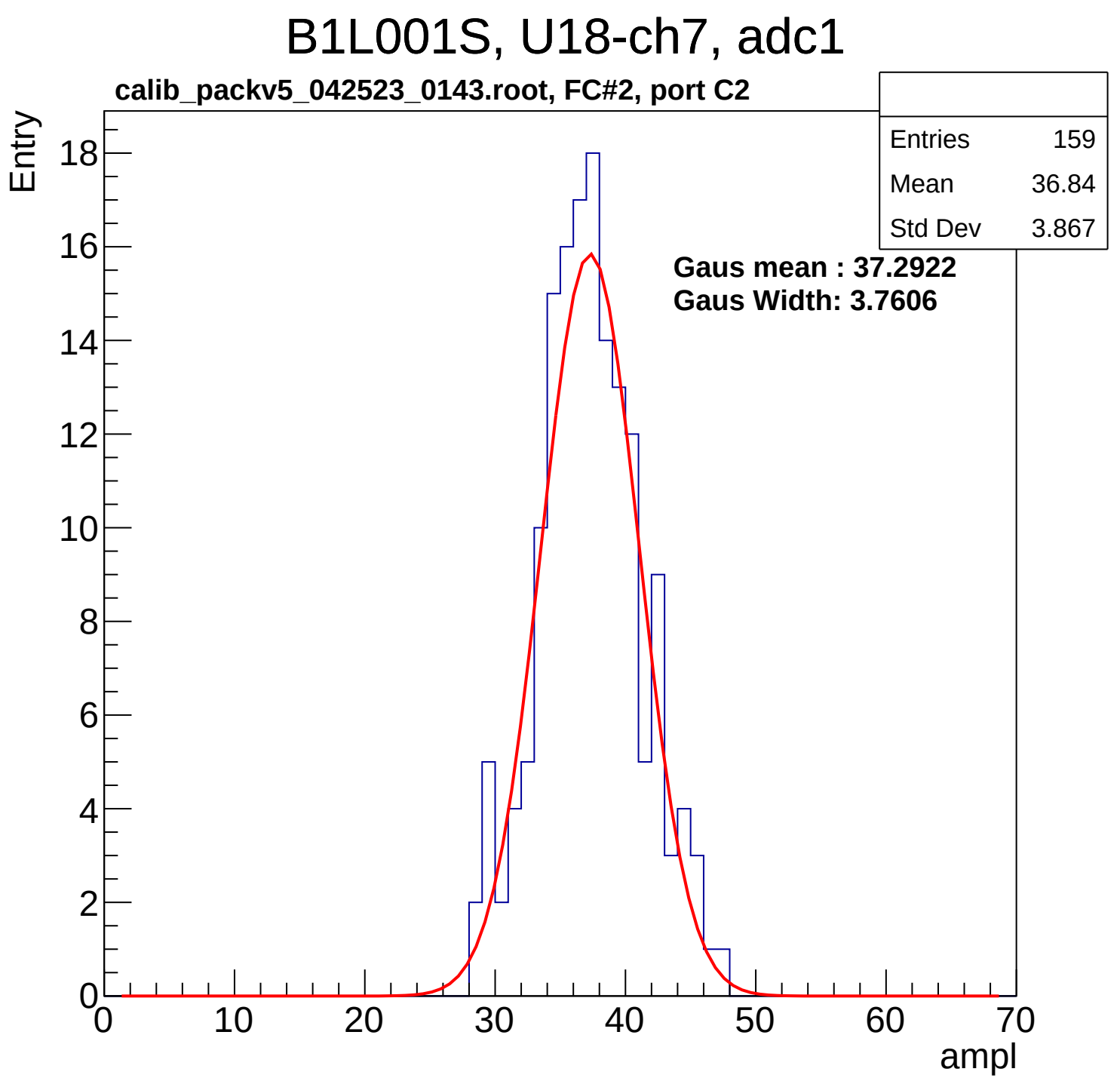

B1L001S, U18-ch6, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 123
Mean 55.38
Std Dev 3.392
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

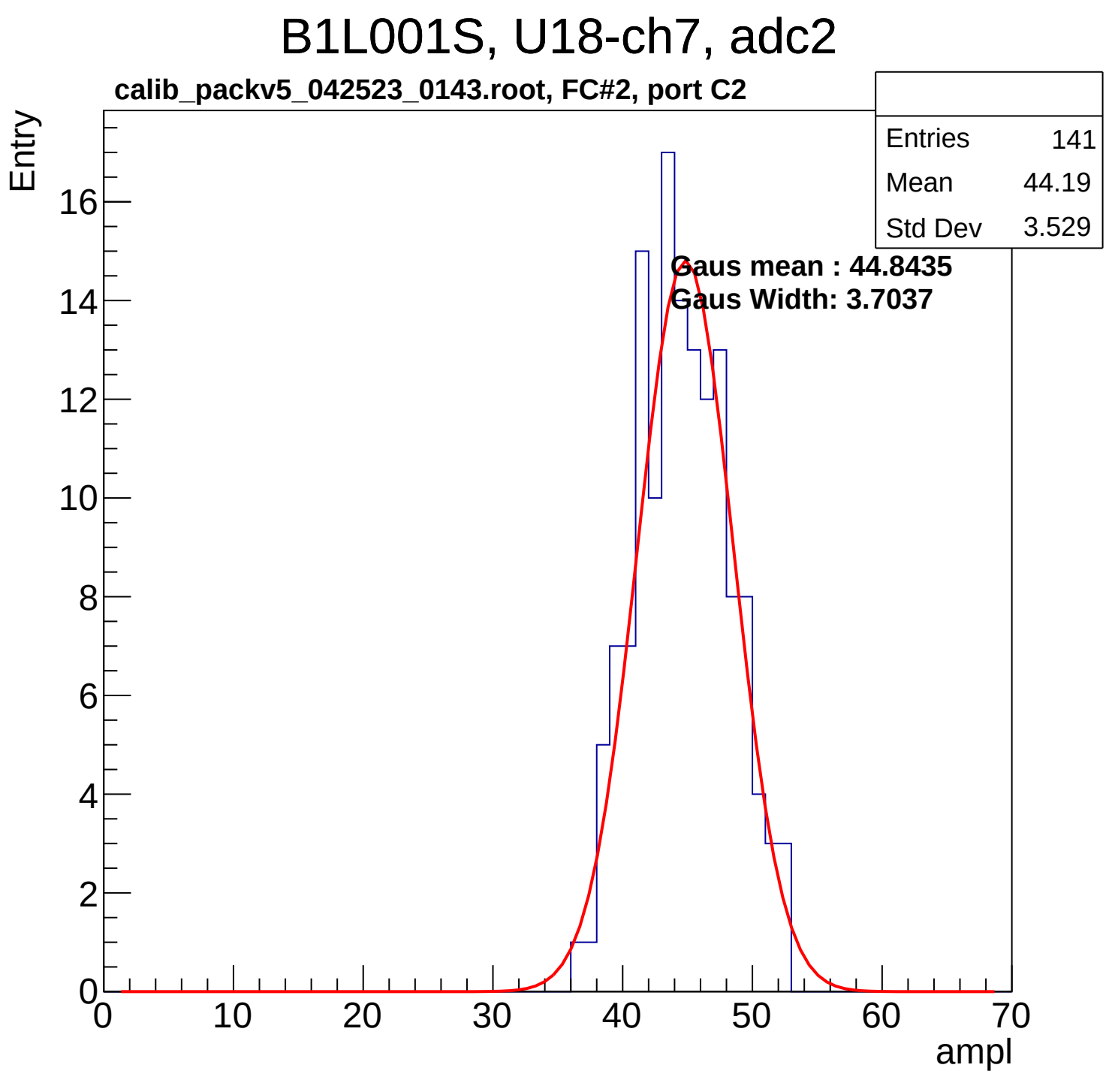

B1L001S, U18-ch6, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 85
Mean 58.54
Std Dev 9.382
Entry
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl

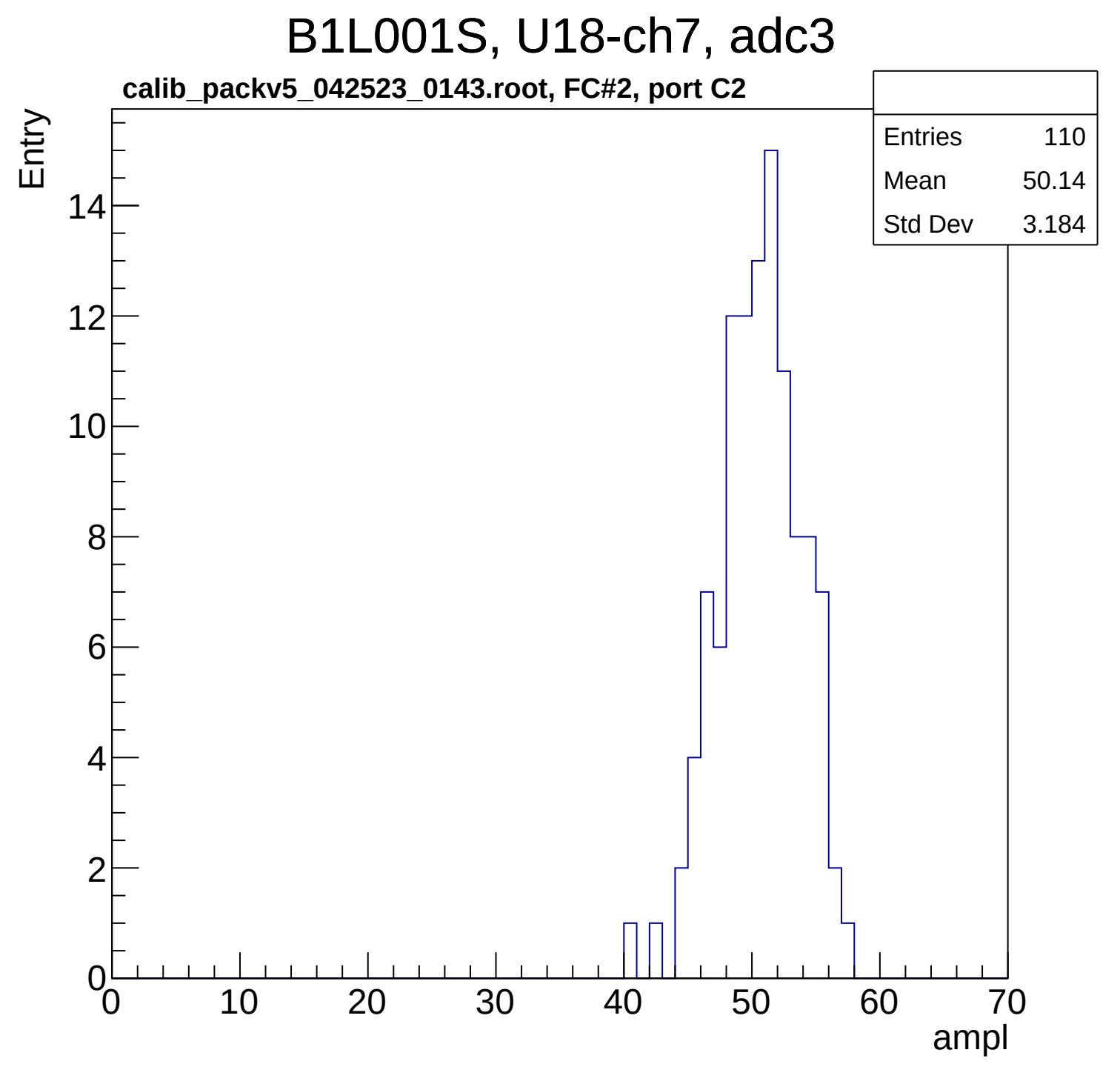

B1L001S, U18-ch6, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 14
Mean 61.64
Std Dev 1.674
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

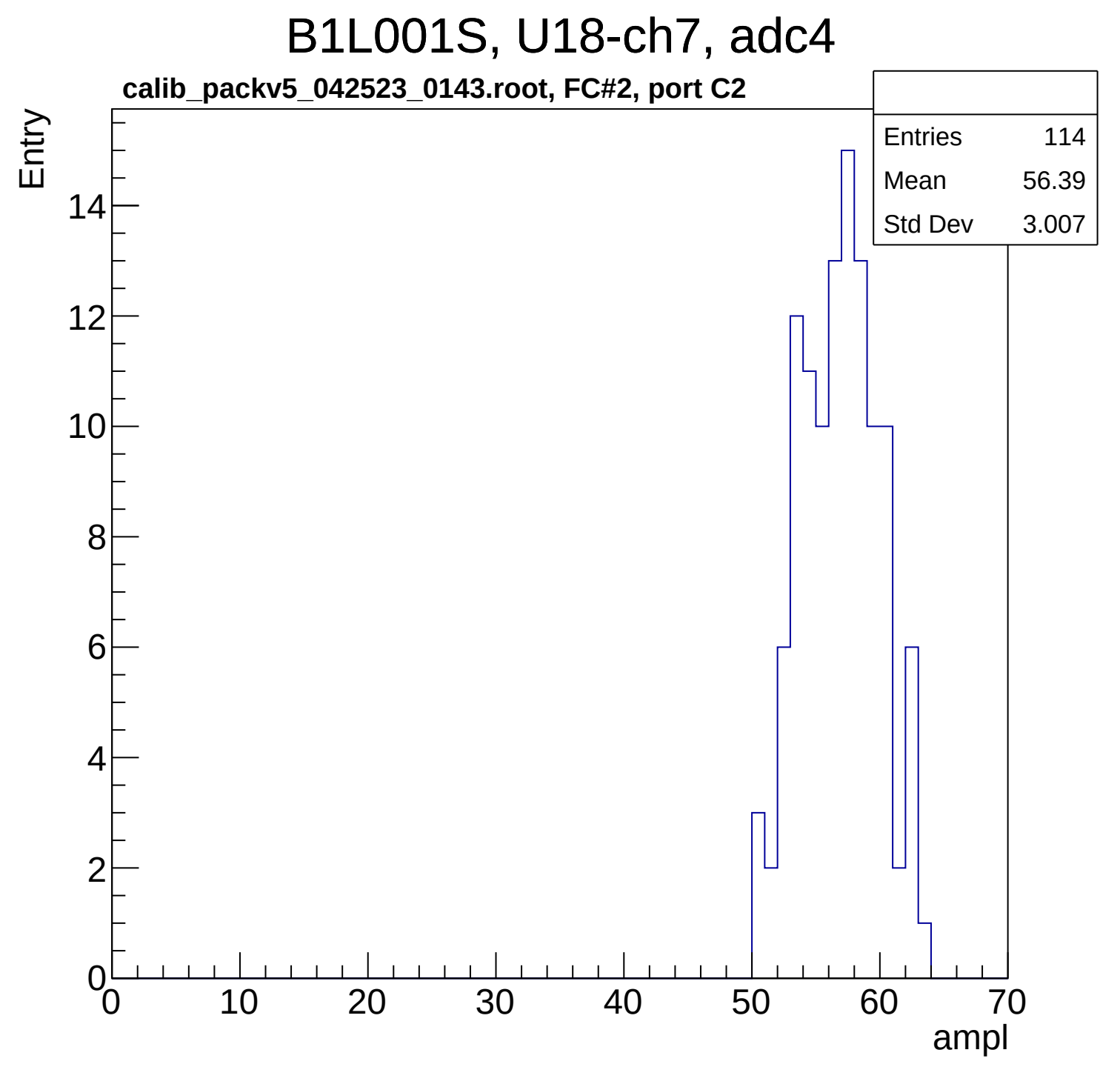

B1L001S, U18-ch6, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 3
Mean 47.33
Std Dev 20.07
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70

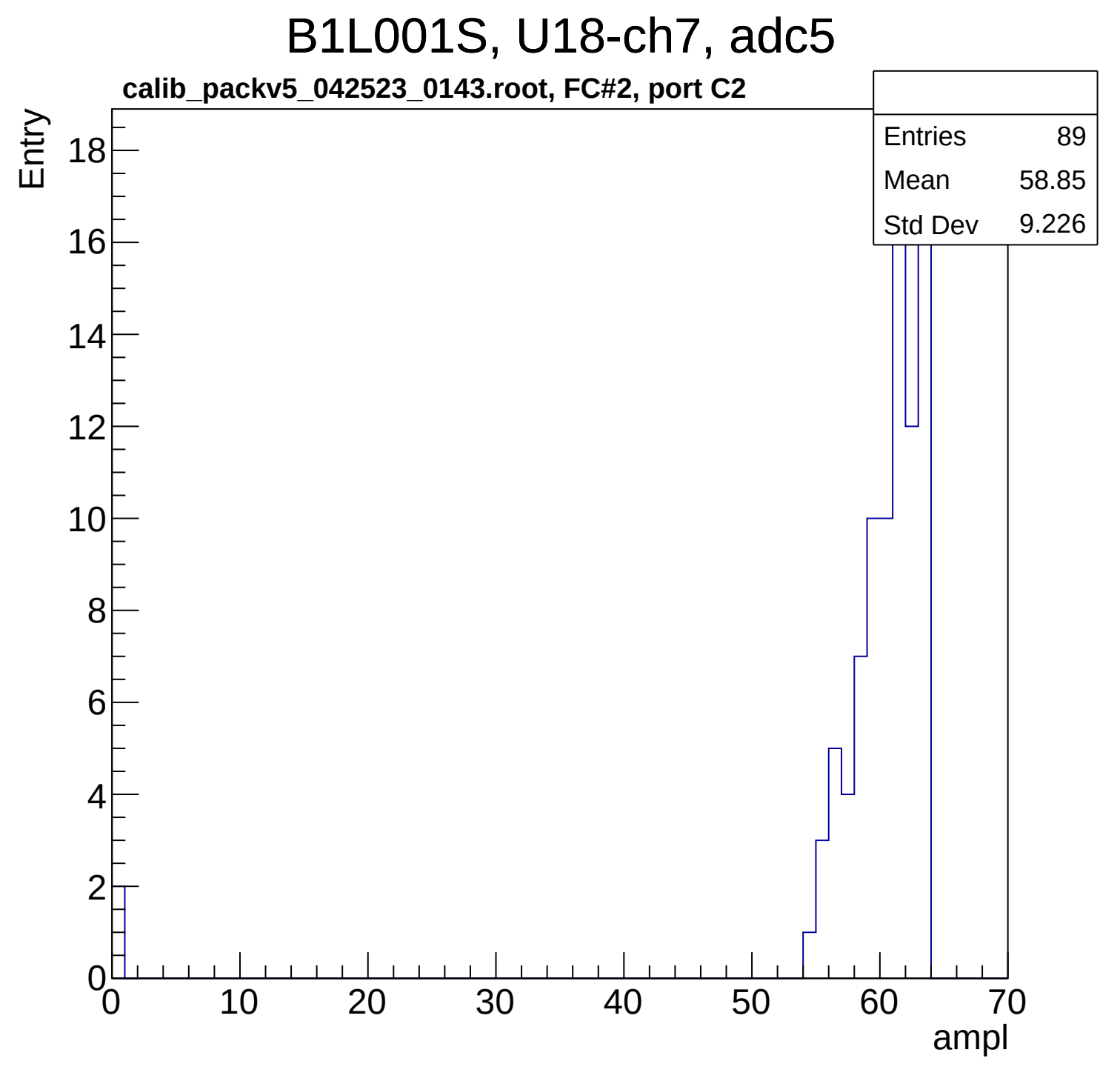

B1L001S, U18-ch7, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 135
Mean 29.39
Std Dev 4.037
Gaus mean : 30.1159
Gaus Width: 3.1935
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

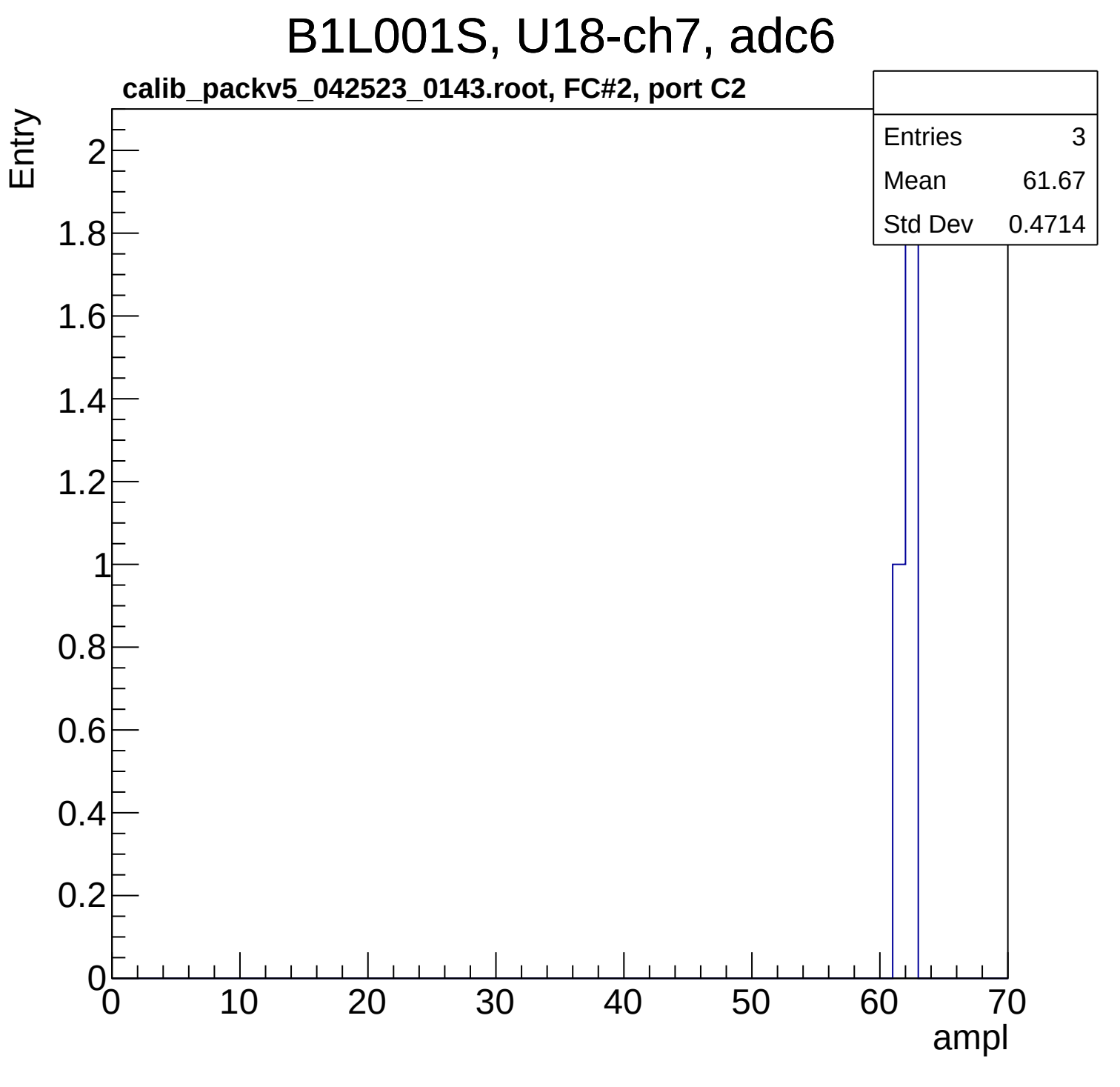

B1L001S, U18-ch7, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 159
Mean 36.84
Std Dev 3.867
Gaus mean : 37.2922
Gaus Width: 3.7606
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

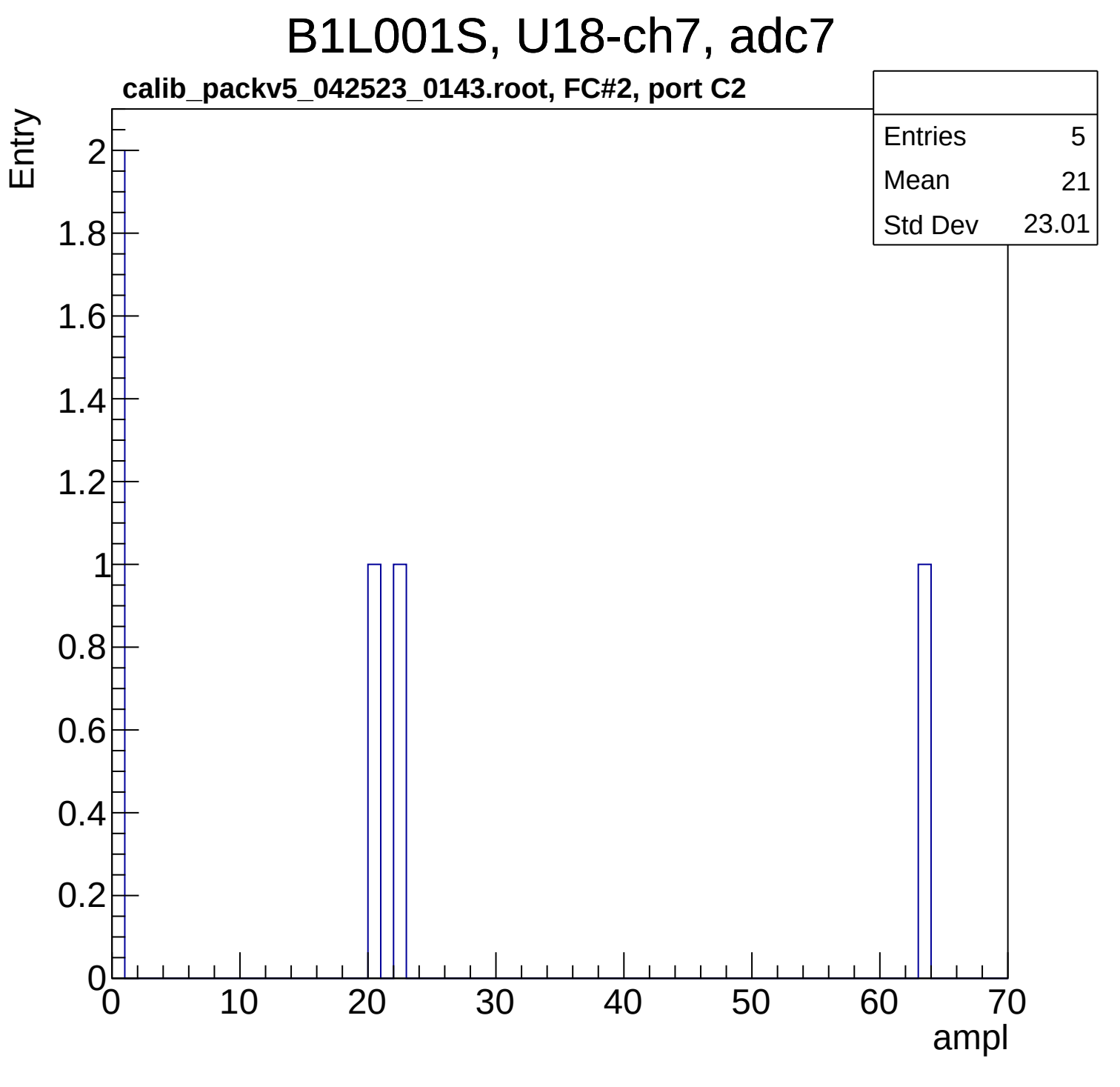

B1L001S, U18-ch7, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 141
Mean 44.19
Std Dev 3.529
Gaus mean : 44.8435
Gaus Width: 3.7037
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

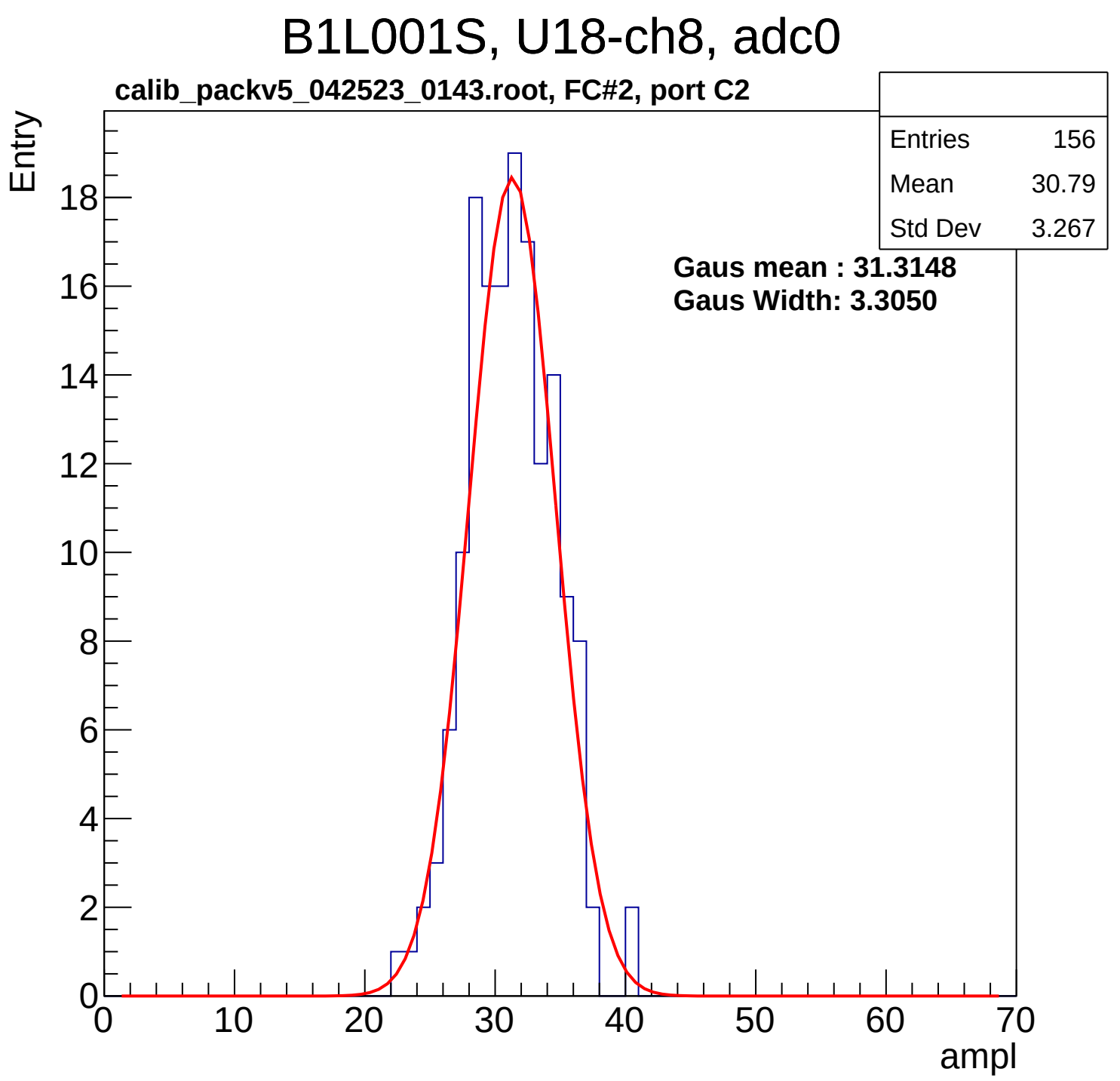

B1L001S, U18-ch7, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 110
Mean 50.14
Std Dev 3.184
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

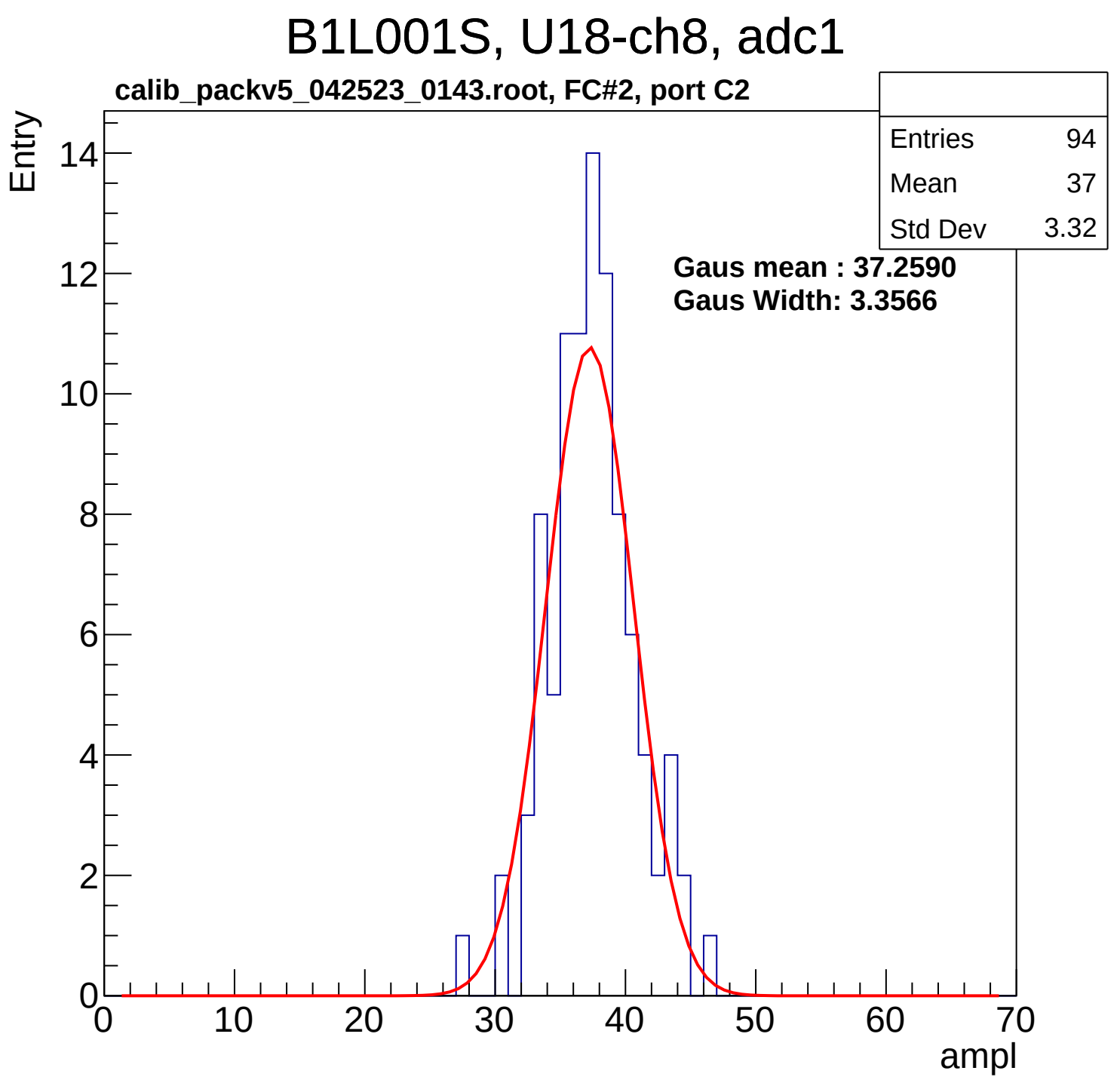

B1L001S, U18-ch7, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 114
Mean 56.39
Std Dev 3.007
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl

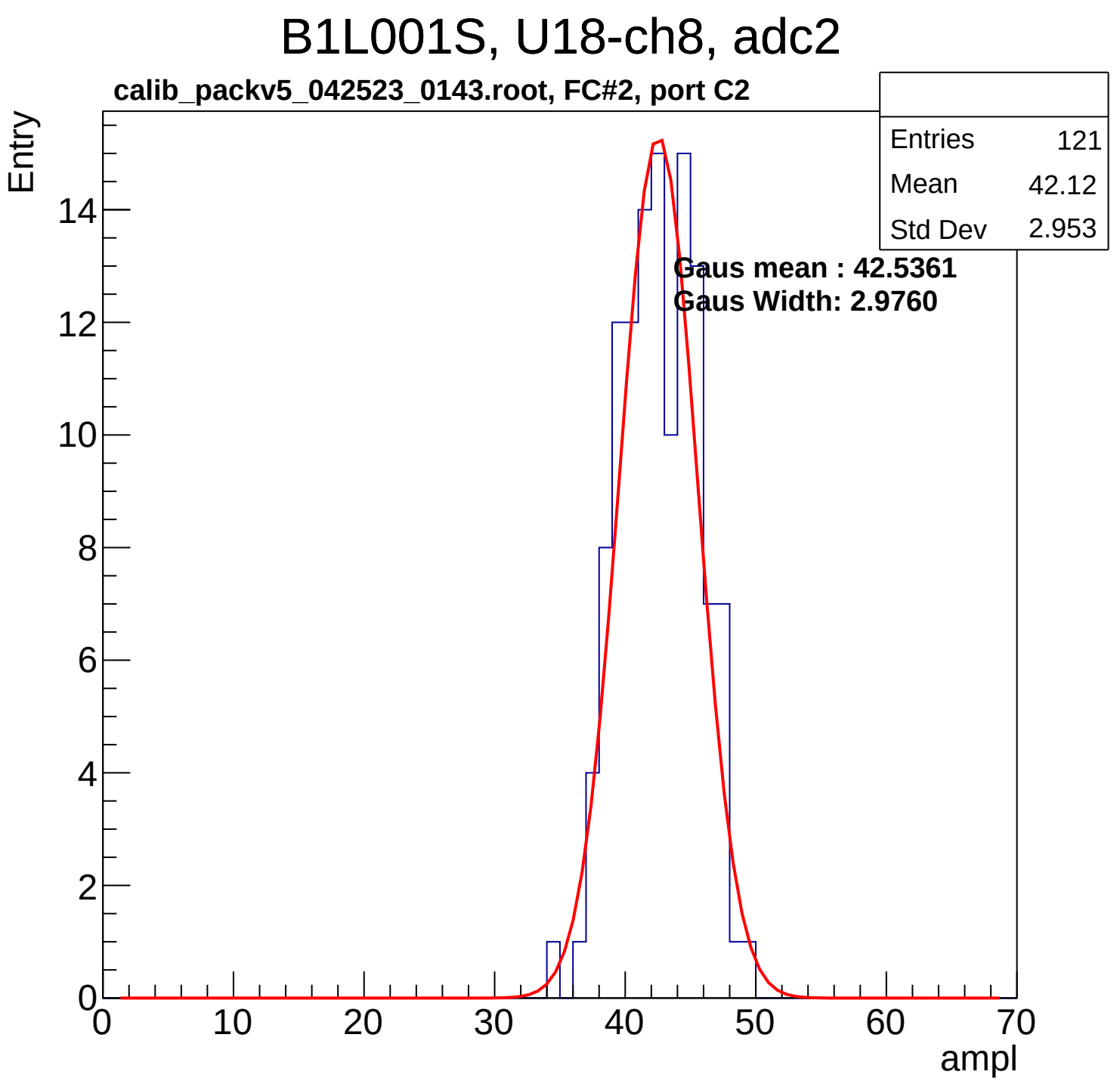

B1L001S, U18-ch7, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 89
Mean 58.85
Std Dev 9.226
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

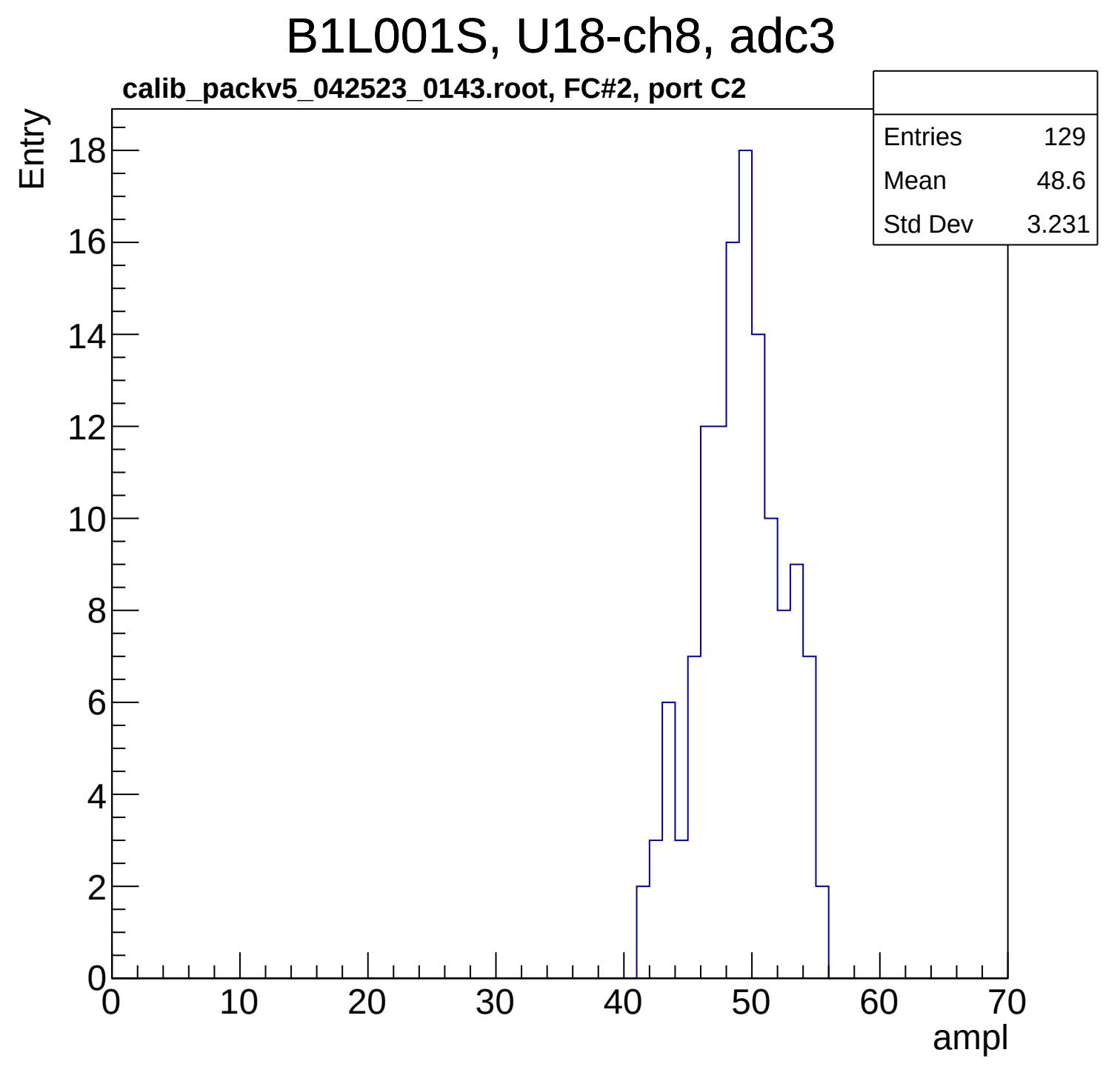

B1L001S, U18-ch7, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 3
Mean 61.67
Std Dev 0.4714
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

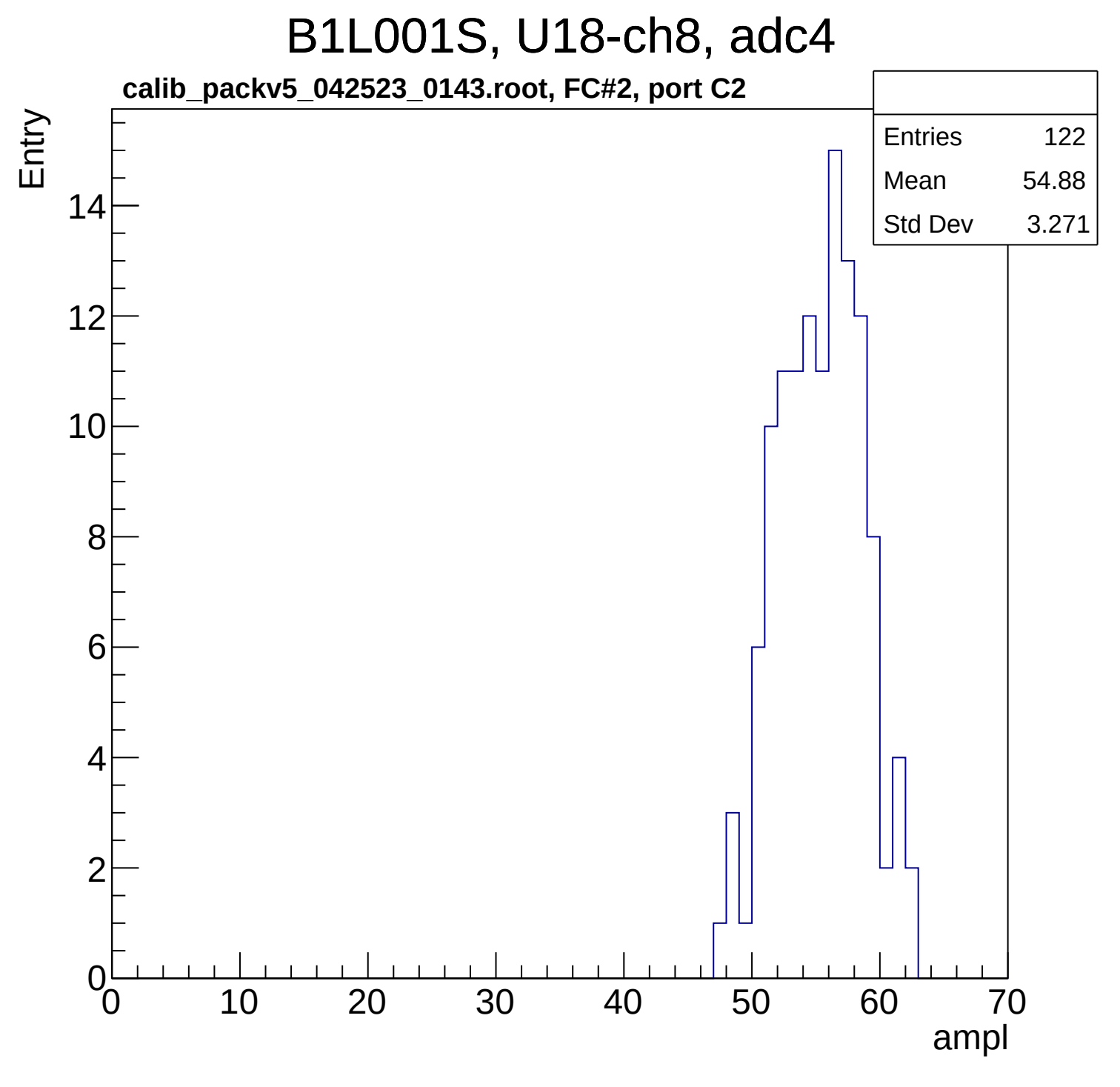

B1L001S, U18-ch7, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 5
Mean 21
Std Dev 23.01
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

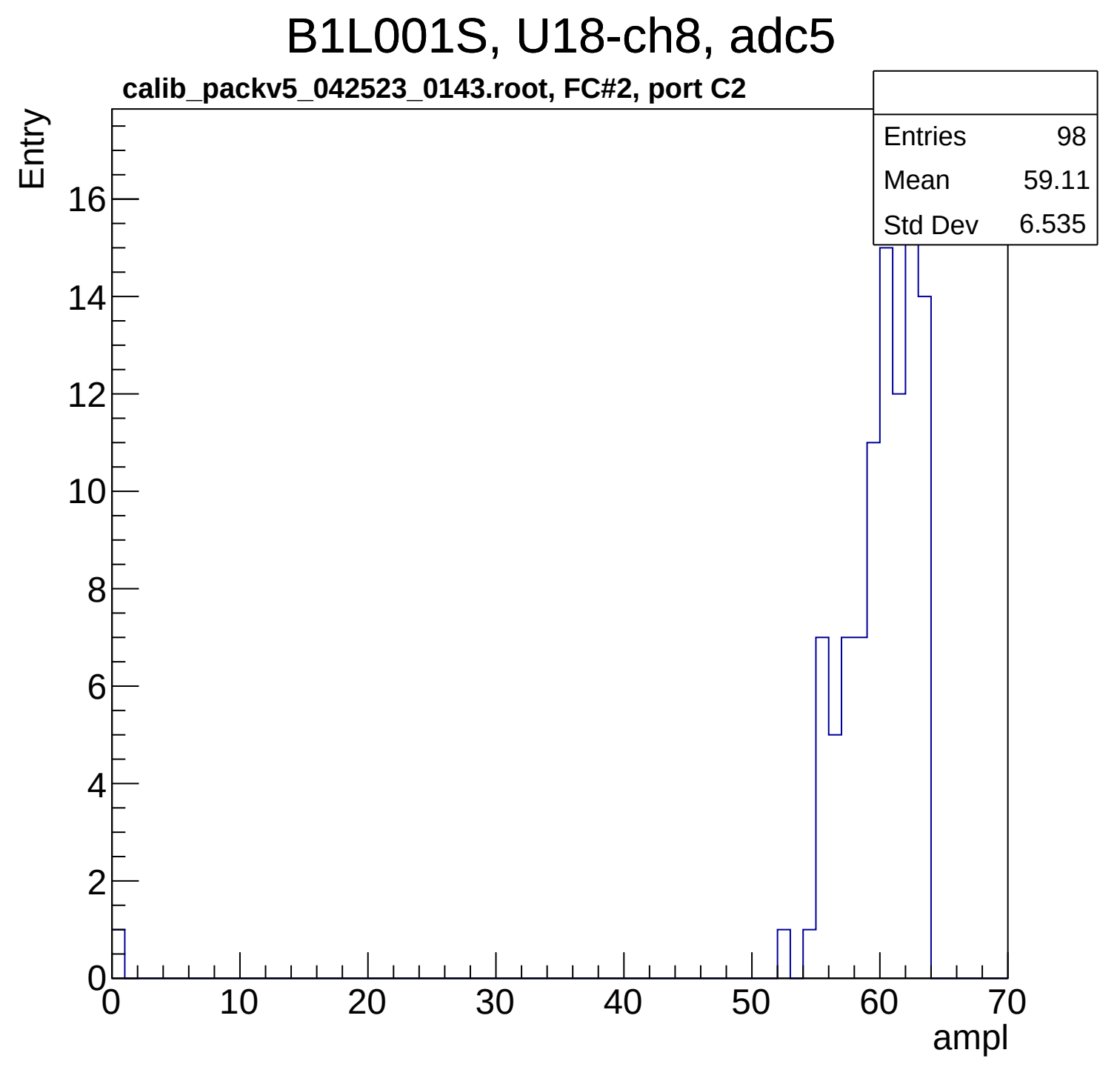

B1L001S, U18-ch8, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 156
Mean 30.79
Std Dev 3.267
Gaus mean : 31.3148
Gaus Width: 3.3050
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

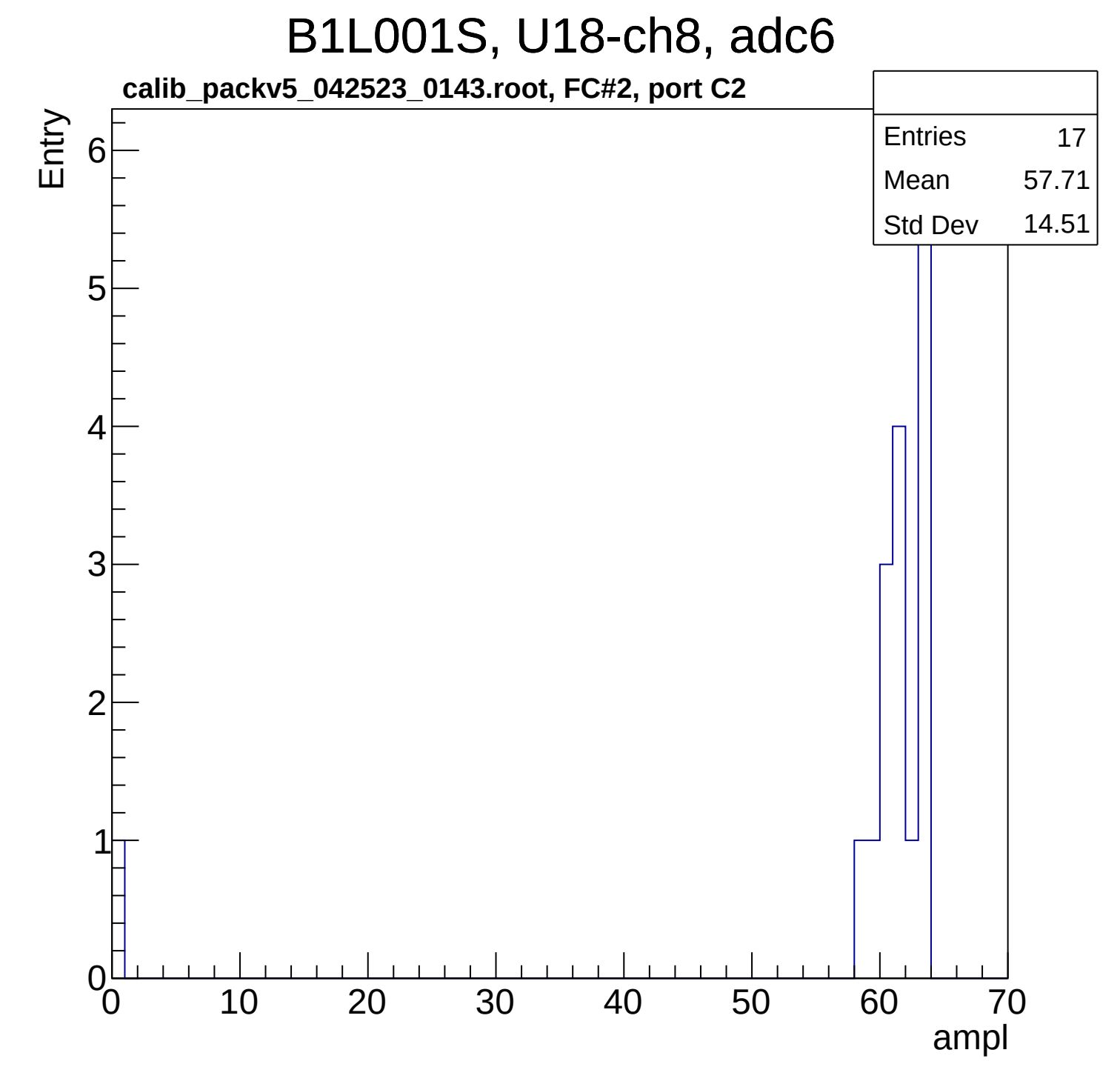

B1L001S, U18-ch8, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 94
Mean 37
Std Dev 3.32
Gaus mean : 37.2590
Gaus Width: 3.3566
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

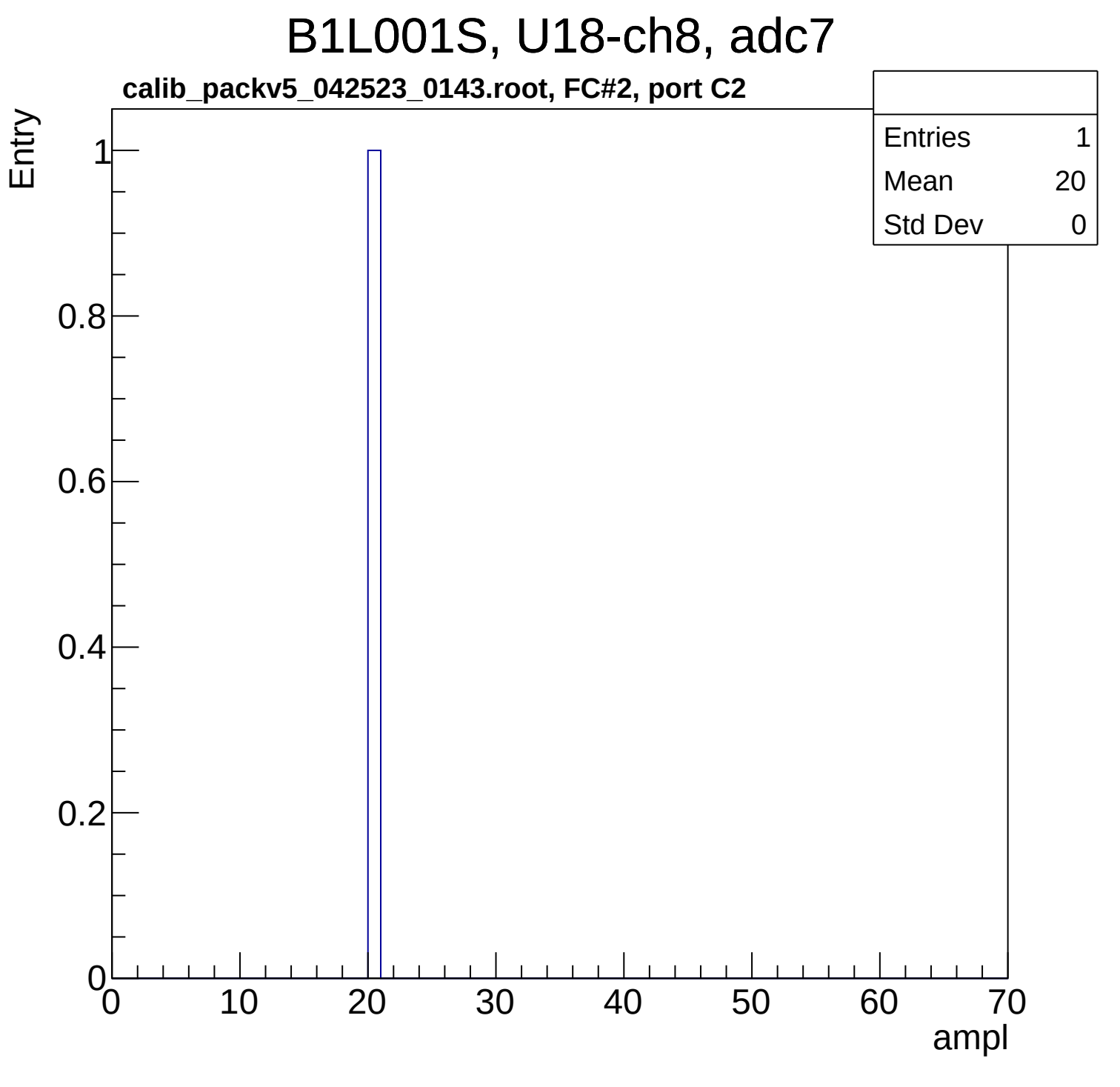

B1L001S, U18-ch8, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 121
Mean 42.12
Std Dev 2.953
Gaus mean : 42.5361
Gaus Width: 2.9760
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

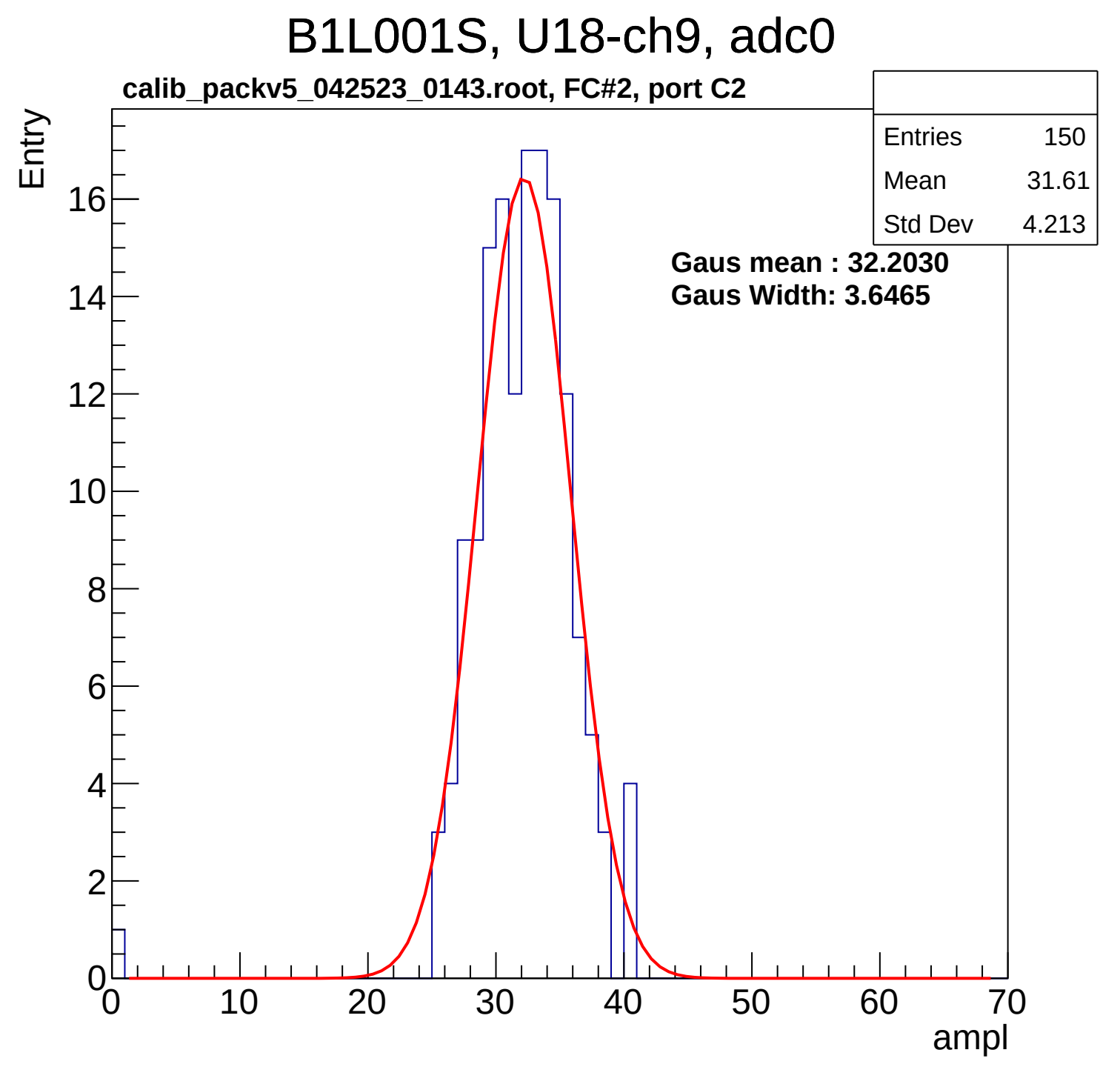

B1L001S, U18-ch8, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 129
Mean 48.6
Std Dev 3.231
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

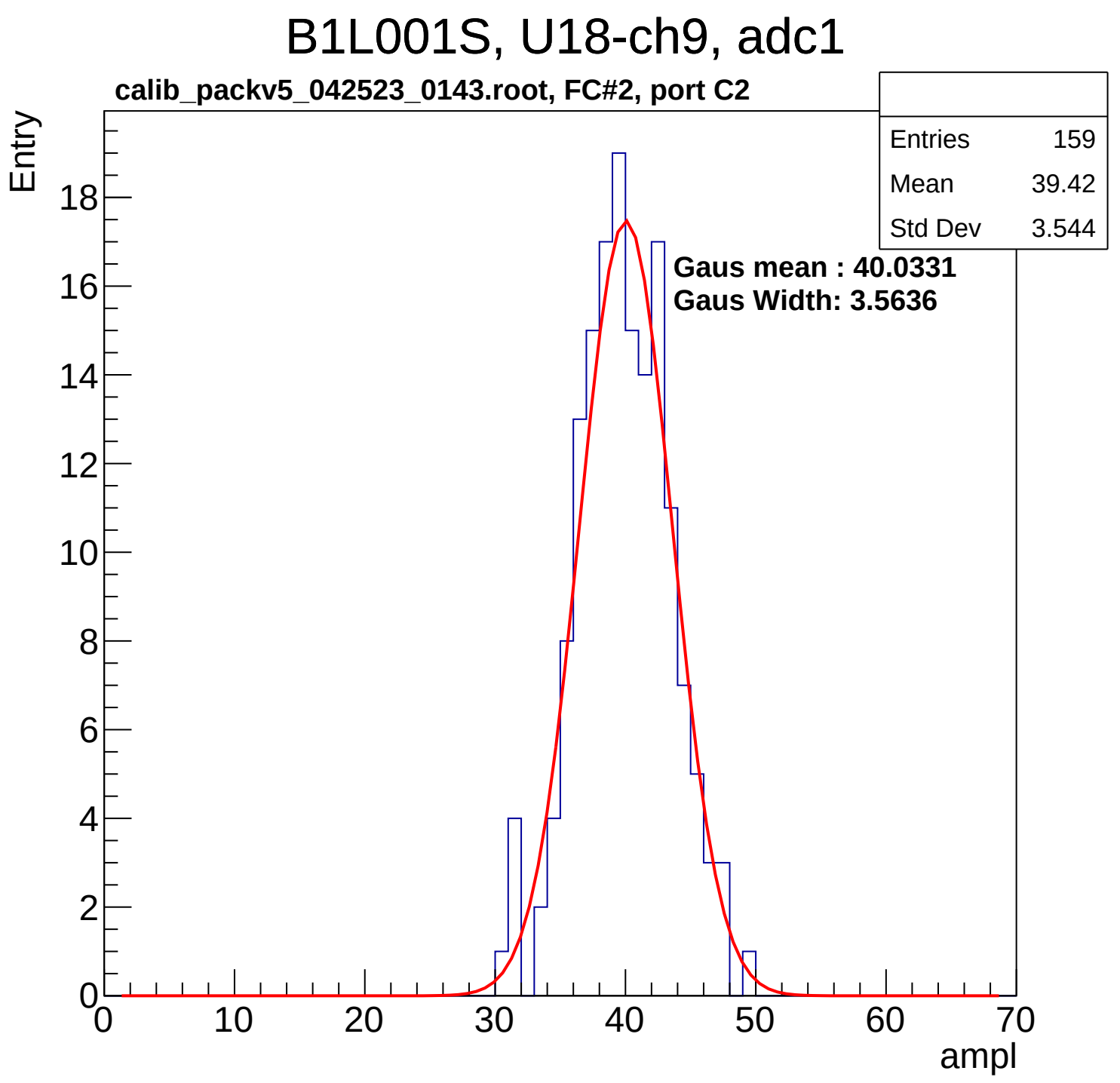

B1L001S, U18-ch8, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 122
Mean 54.88
Std Dev 3.271
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl

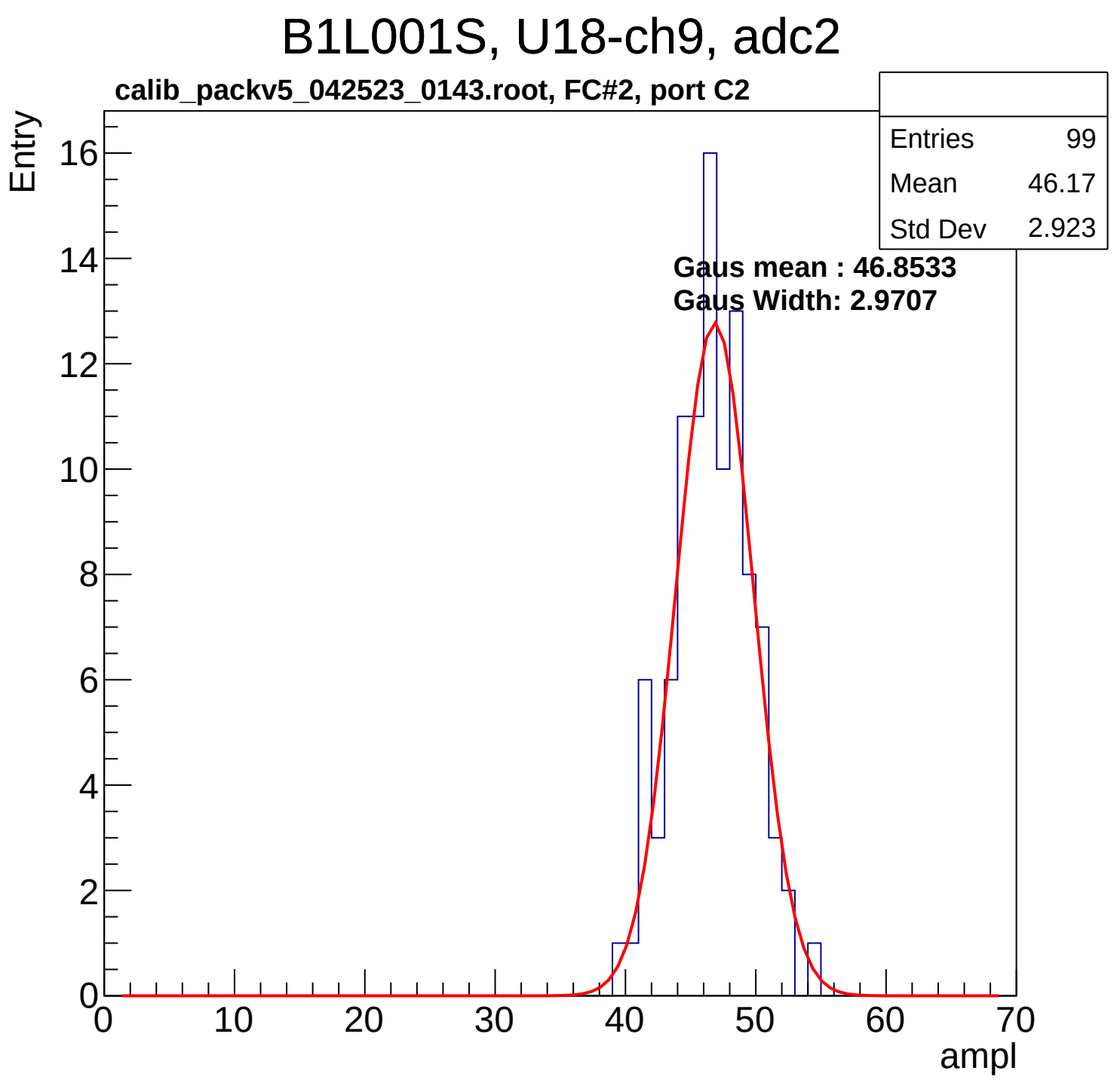

B1L001S, U18-ch8, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 98
Mean 59.11
Std Dev 6.535
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

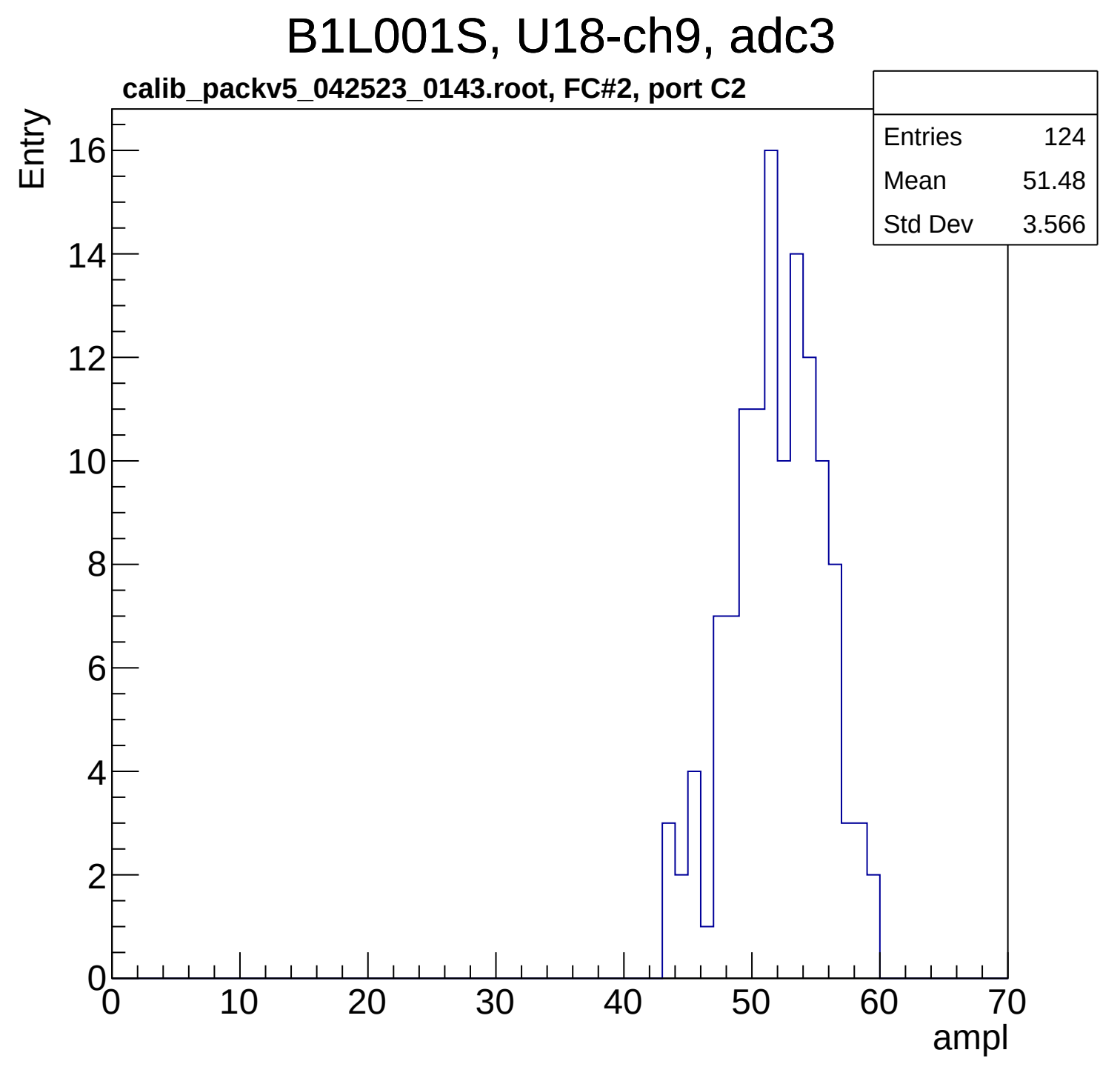

B1L001S, U18-ch8, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 17
Mean 57.71
Std Dev 14.51
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

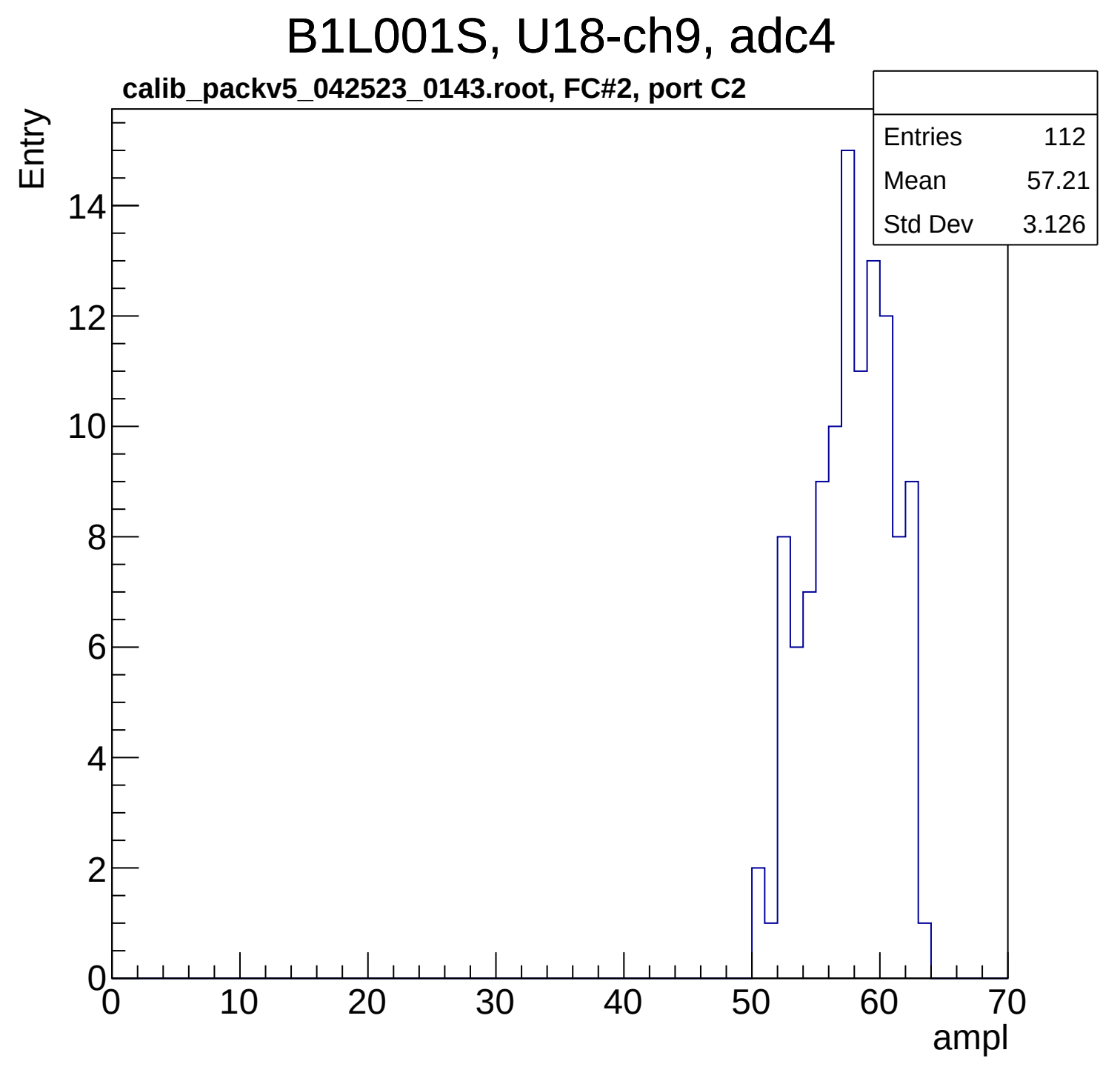

B1L001S, U18-ch8, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 20
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70

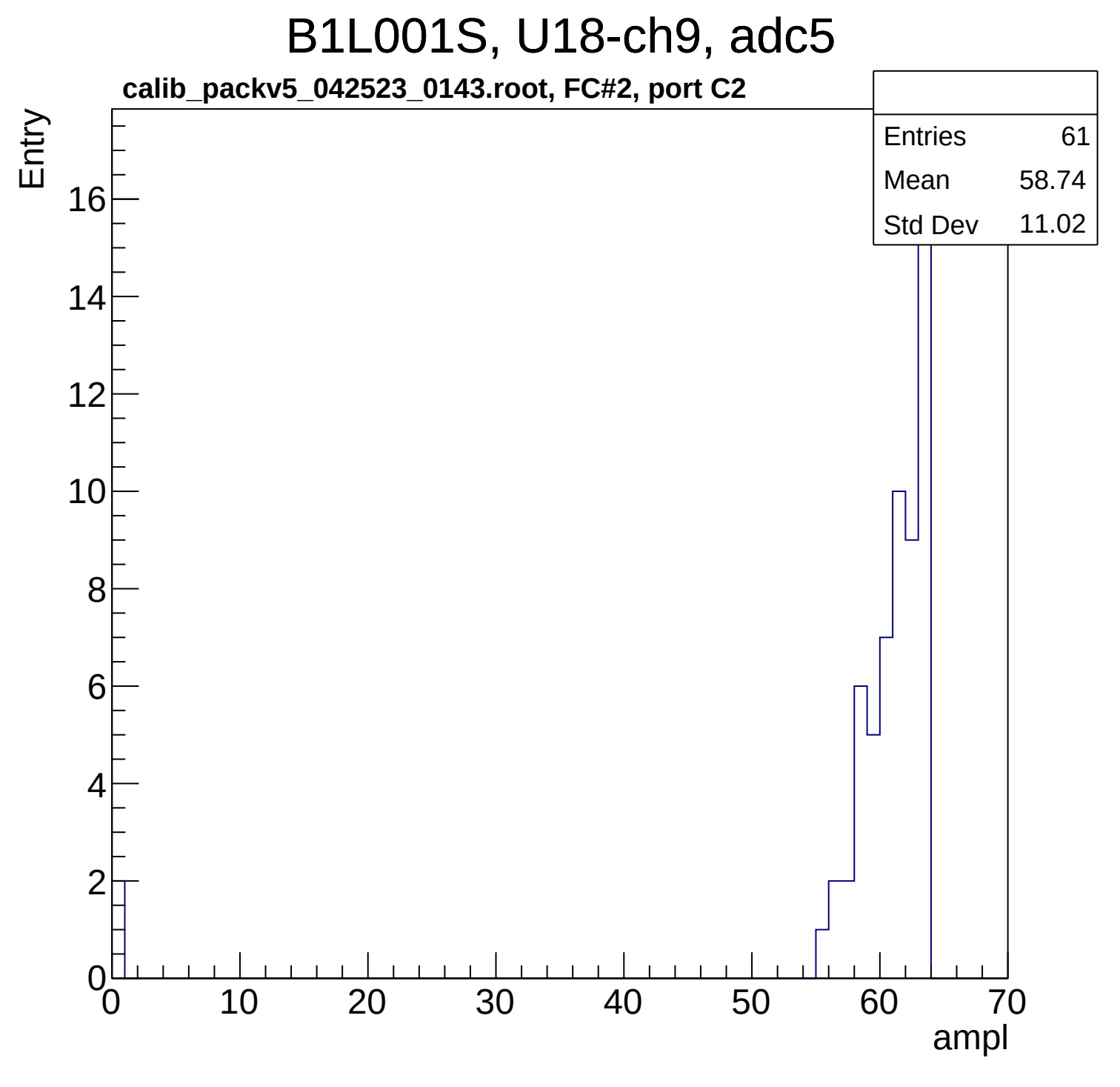

B1L001S, U18-ch9, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 150
Mean 31.61
Std Dev 4.213
Gaus mean : 32.2030
Gaus Width: 3.6465
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

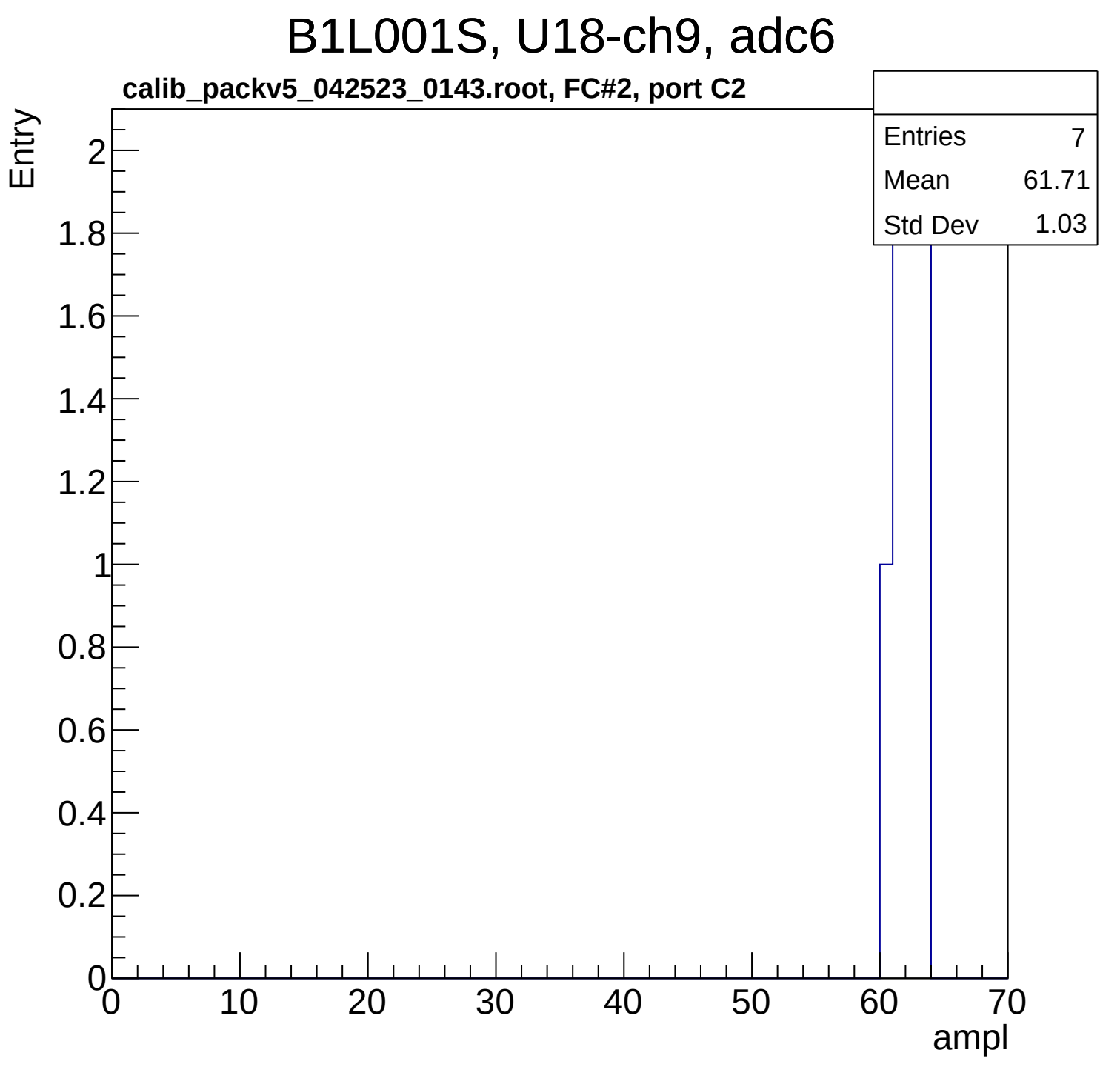

B1L001S, U18-ch9, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 159
Mean 39.42
Std Dev 3.544
Gaus mean : 40.0331
Gaus Width: 3.5636
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

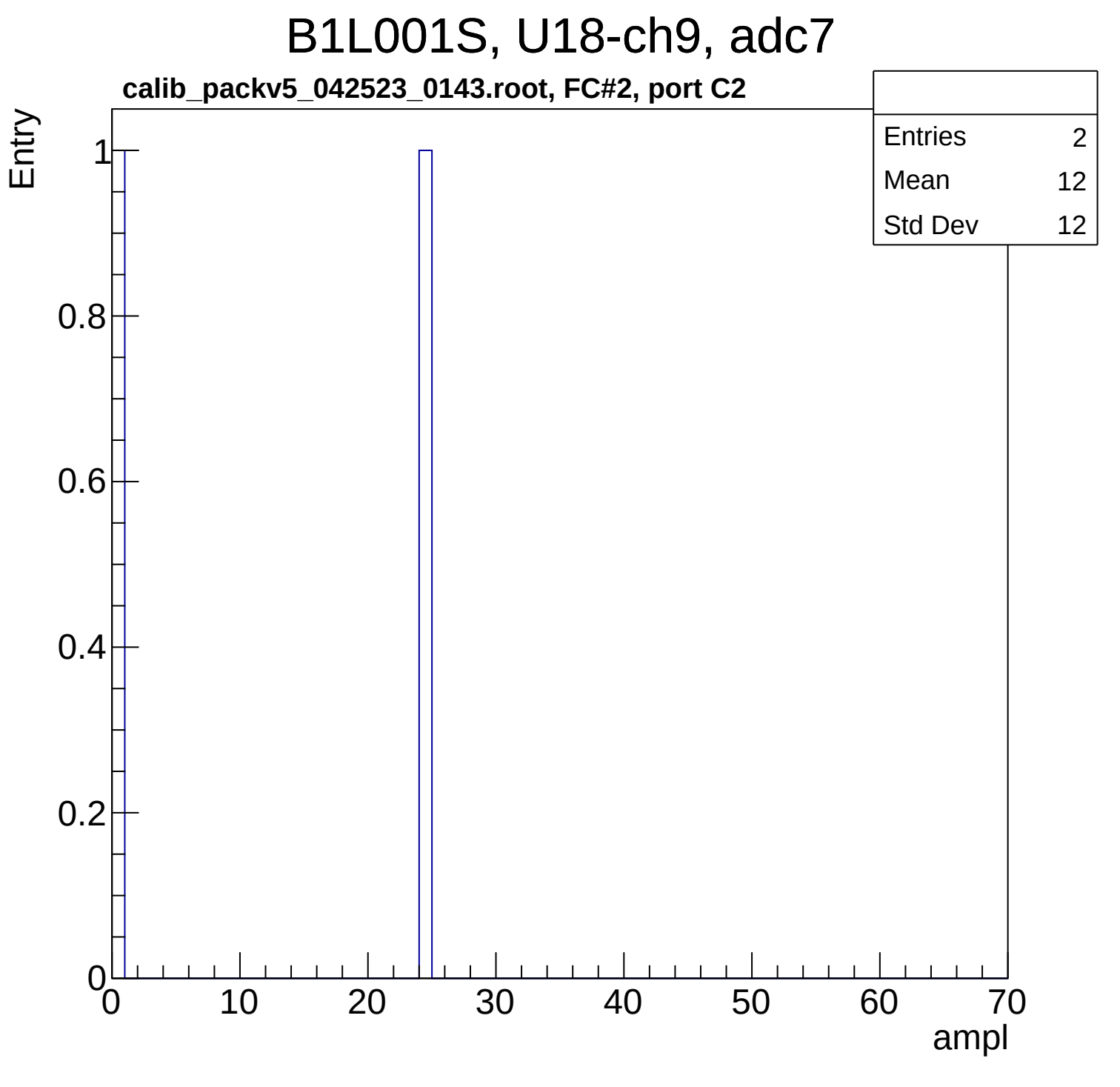

B1L001S, U18-ch9, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 99
Mean 46.17
Std Dev 2.923
Gaus mean : 46.8533
Gaus Width: 2.9707
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

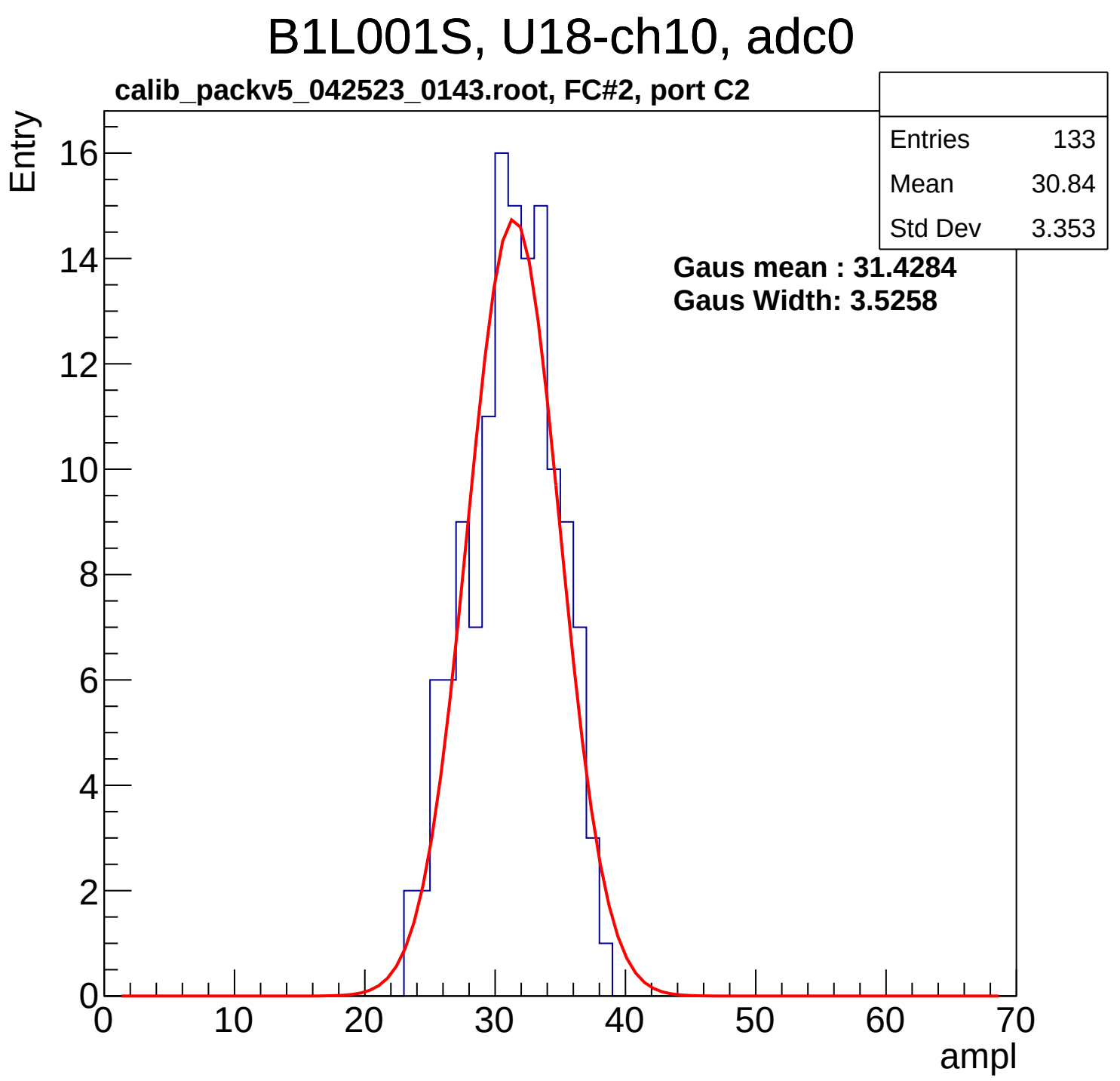

B1L001S, U18-ch9, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 124
Mean 51.48
Std Dev 3.566
Entry
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl

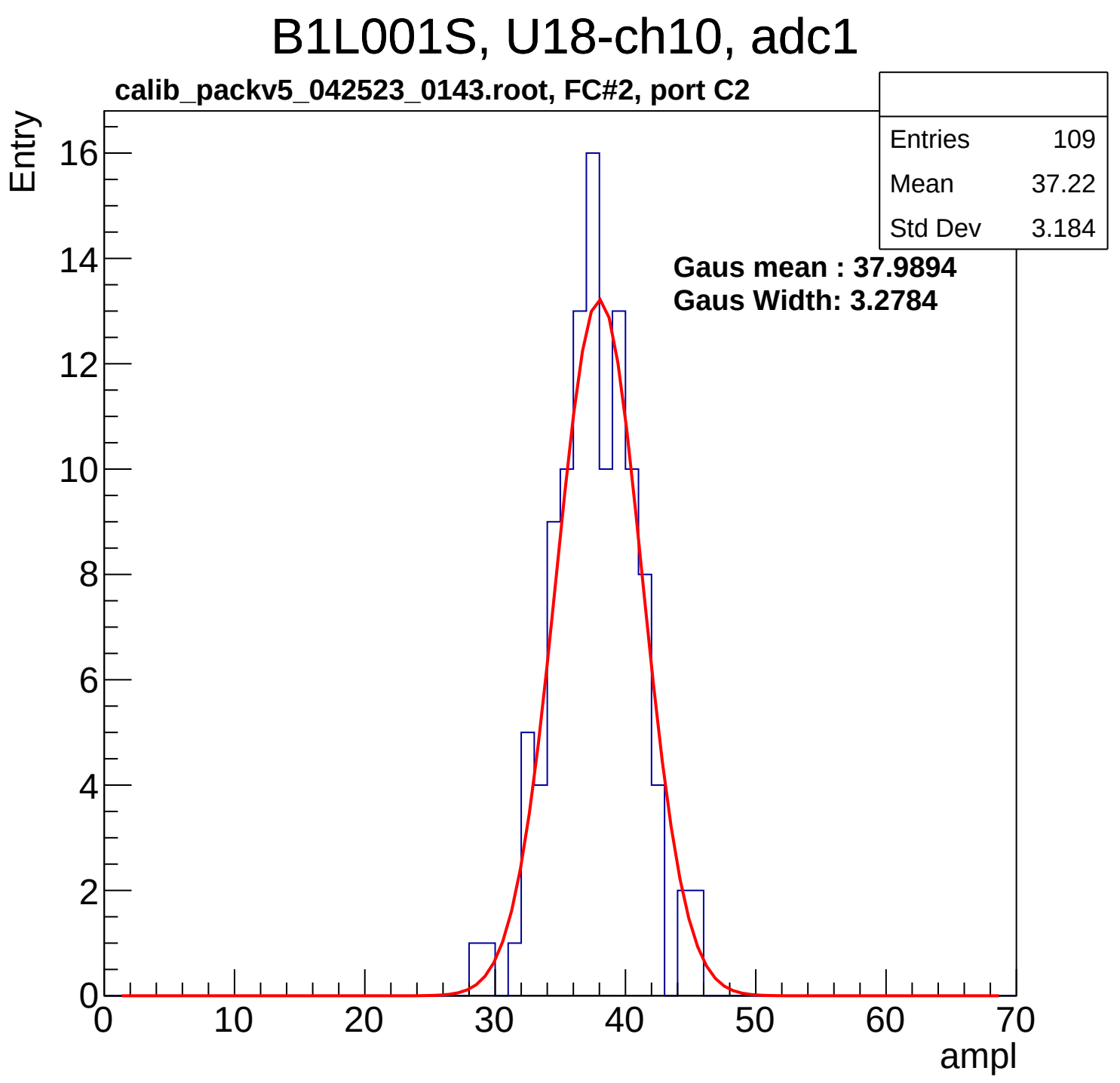

B1L001S, U18-ch9, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 112
Mean 57.21
Std Dev 3.126
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

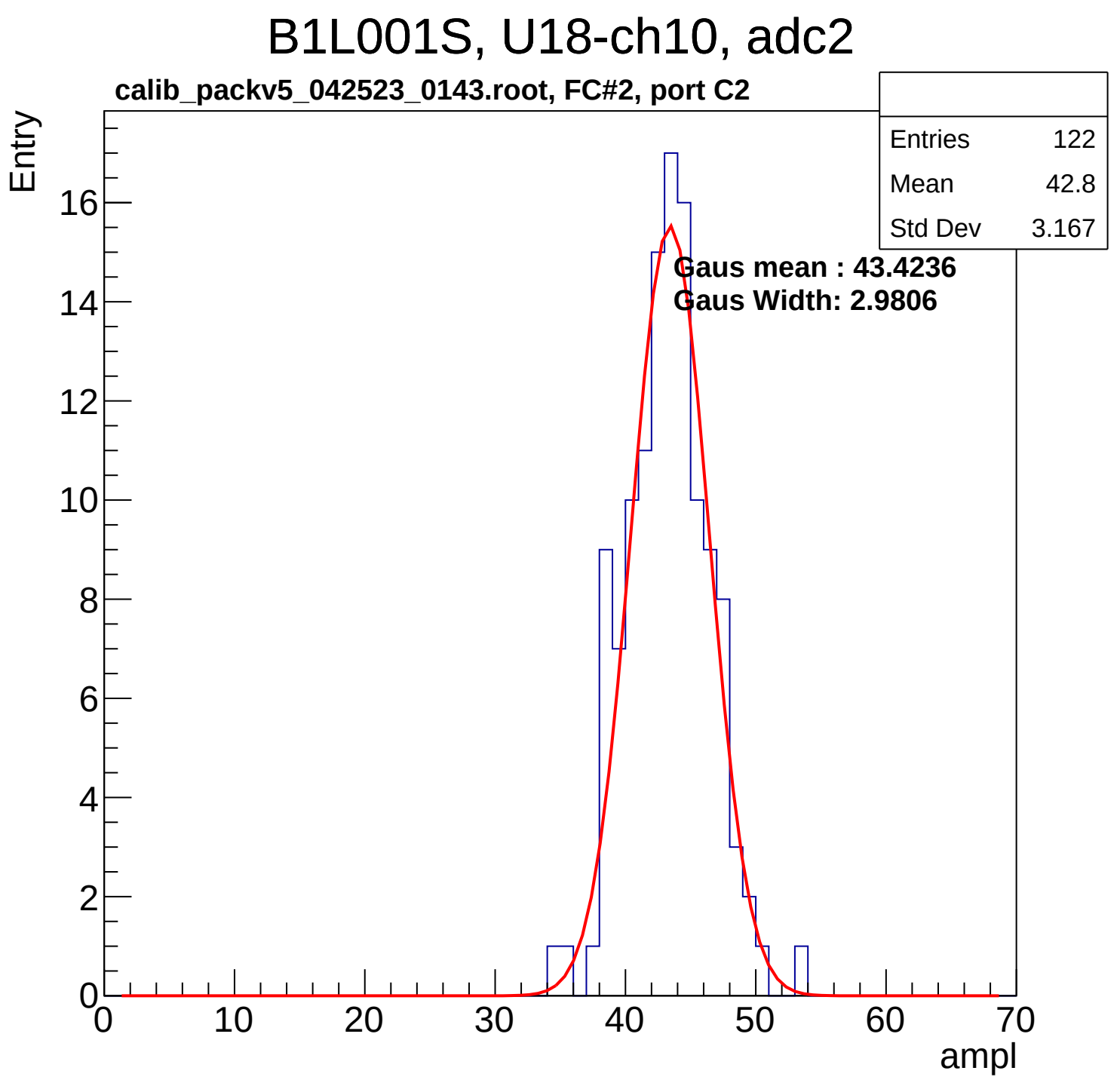

B1L001S, U18-ch9, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 61
Mean 58.74
Std Dev 11.02
Entry
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl

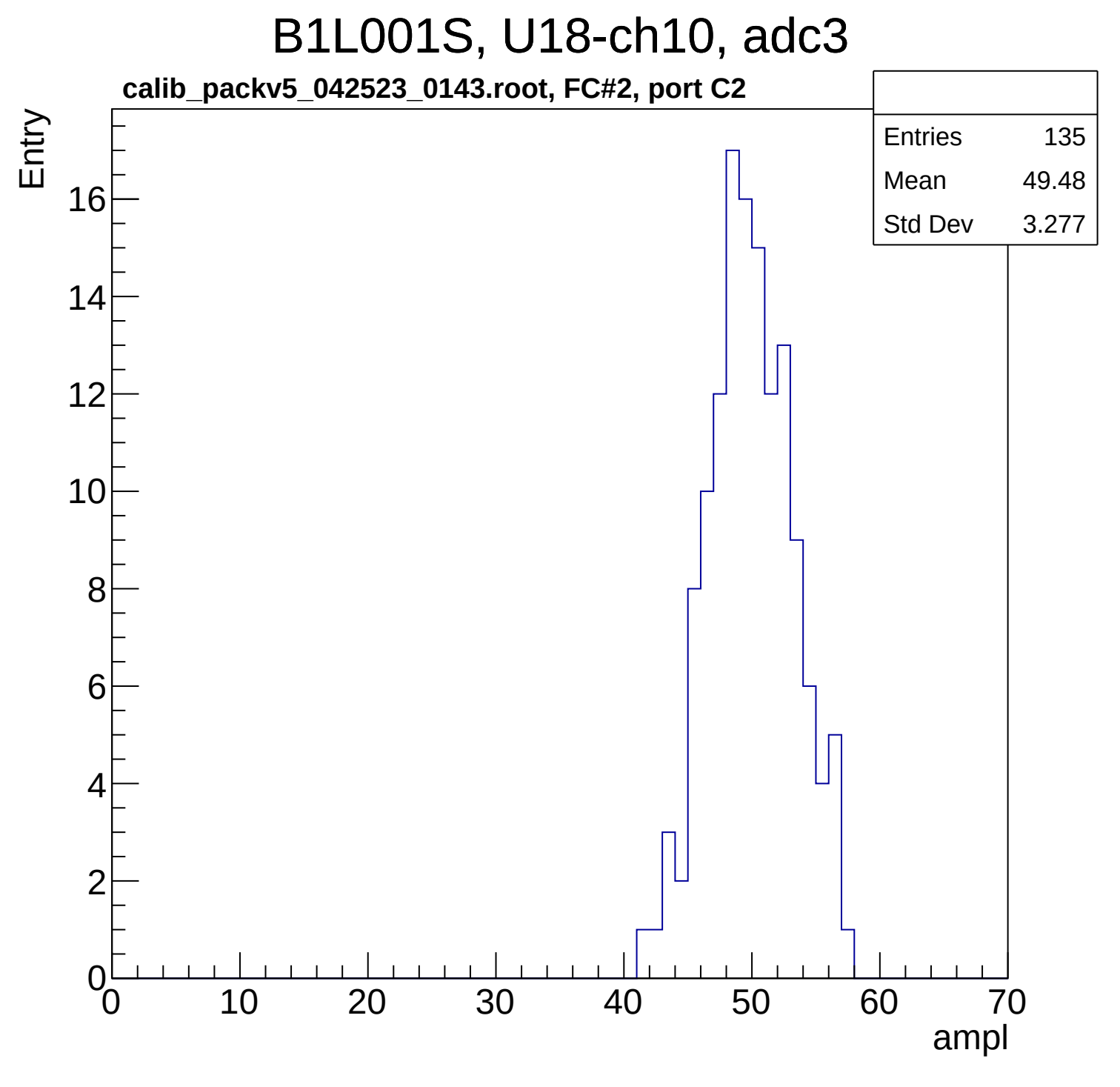

B1L001S, U18-ch9, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 7
Mean 61.71
Std Dev 1.03
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

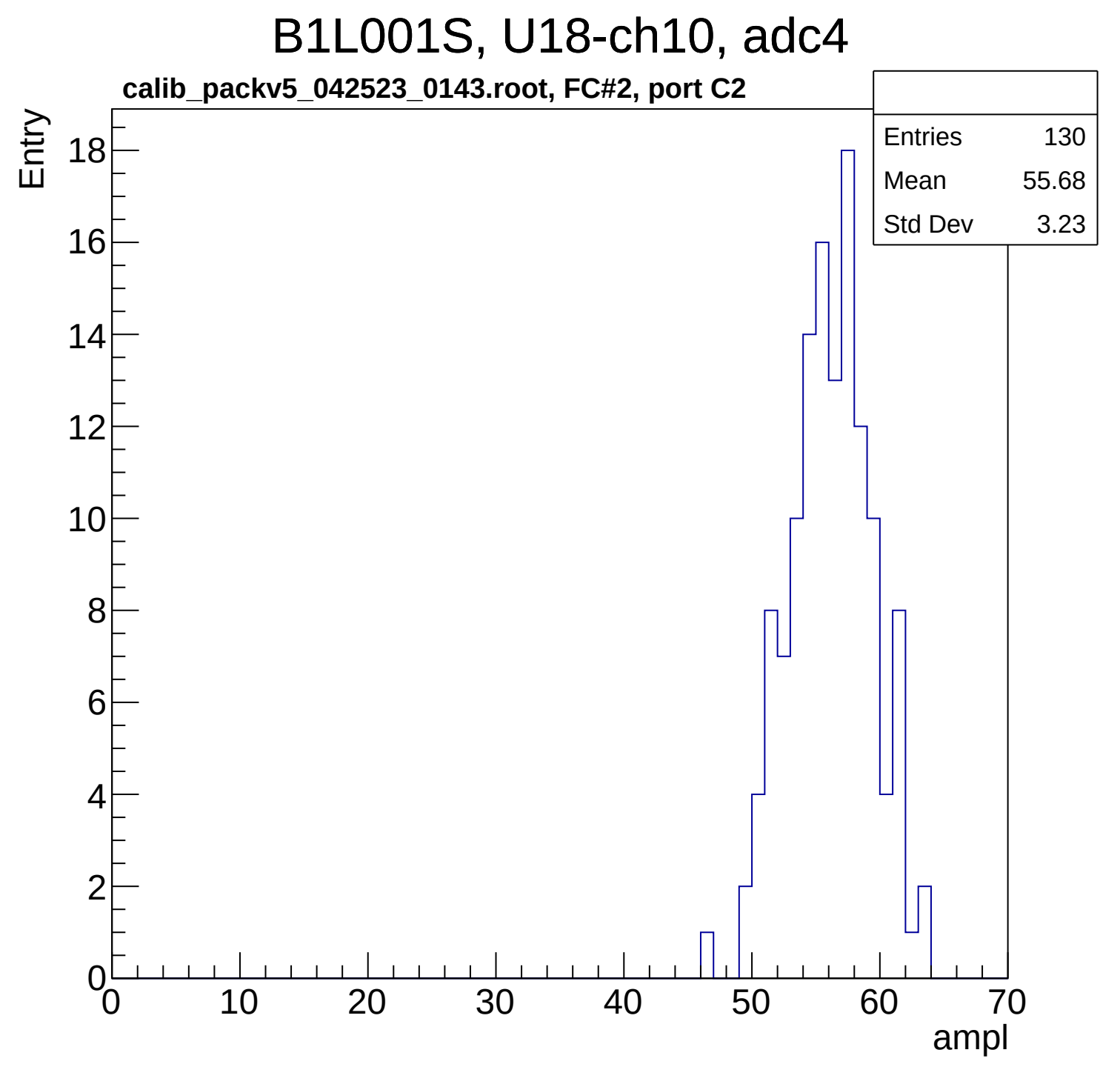

B1L001S, U18-ch9, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 12
Std Dev 12
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

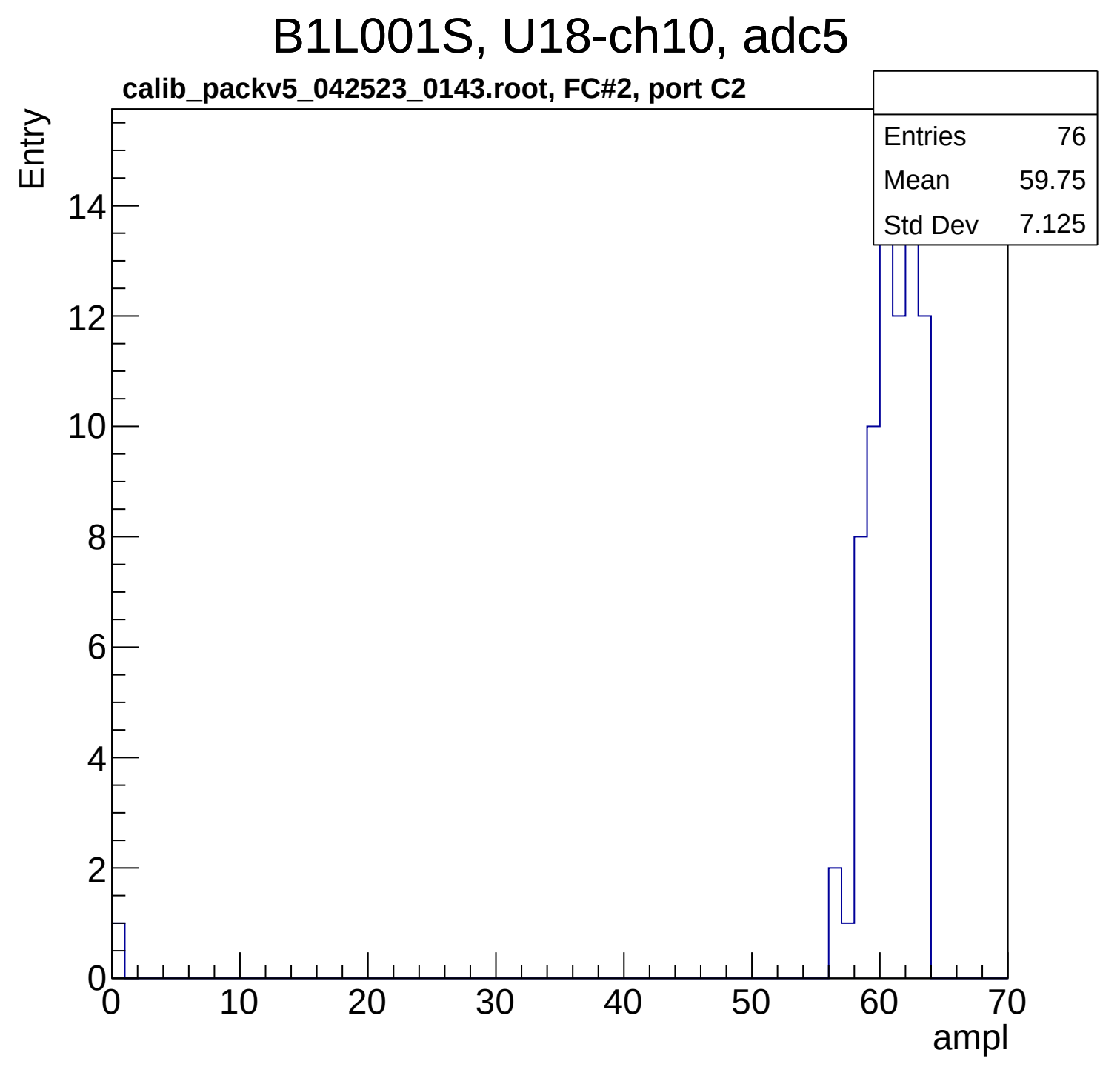

B1L001S, U18-ch10, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 133
Mean 30.84
Std Dev 3.353
Gaus mean : 31.4284
Gaus Width: 3.5258
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

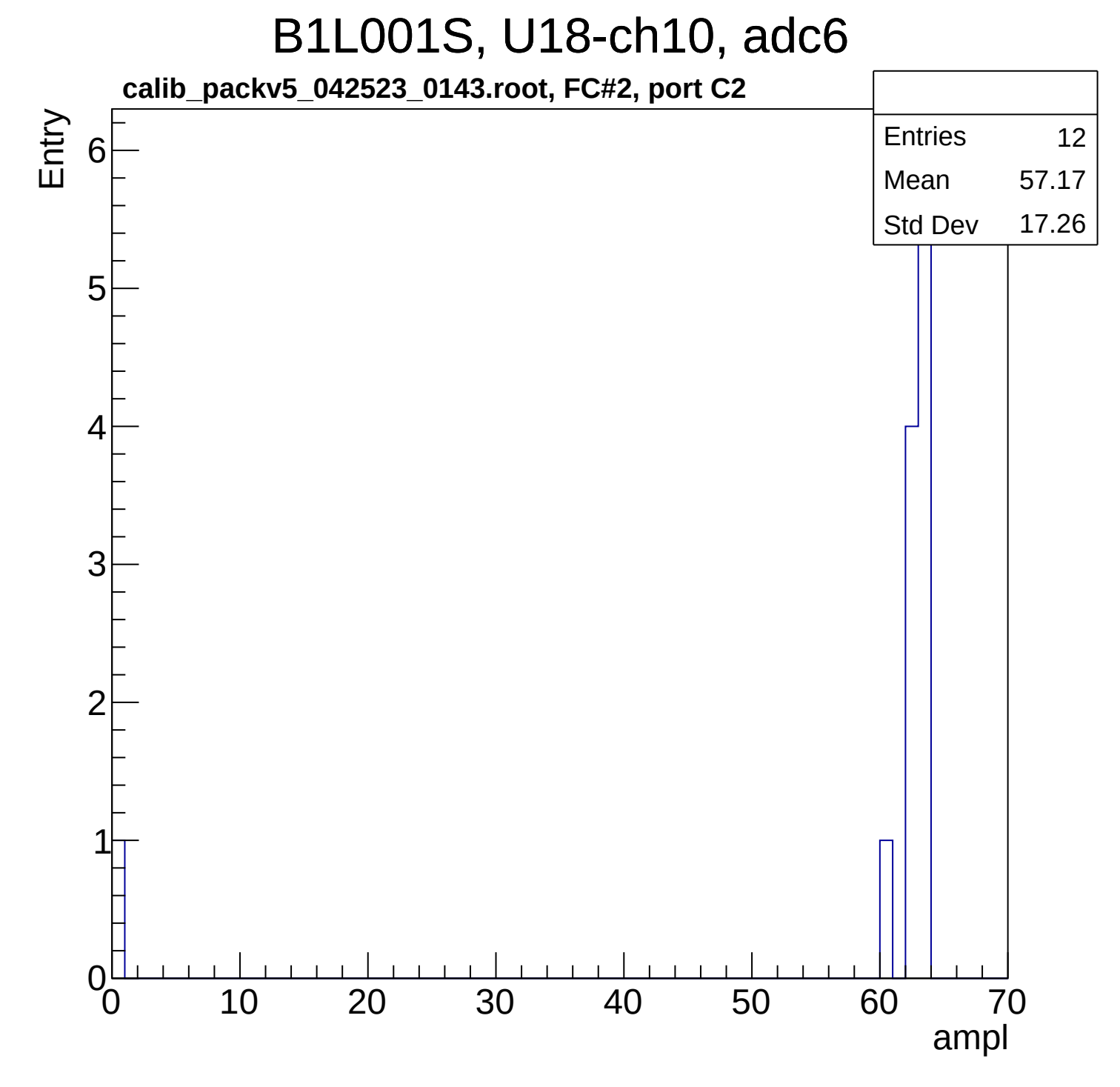

B1L001S, U18-ch10, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 109
Mean 37.22
Std Dev 3.184
Gaus mean : 37.9894
Gaus Width: 3.2784
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

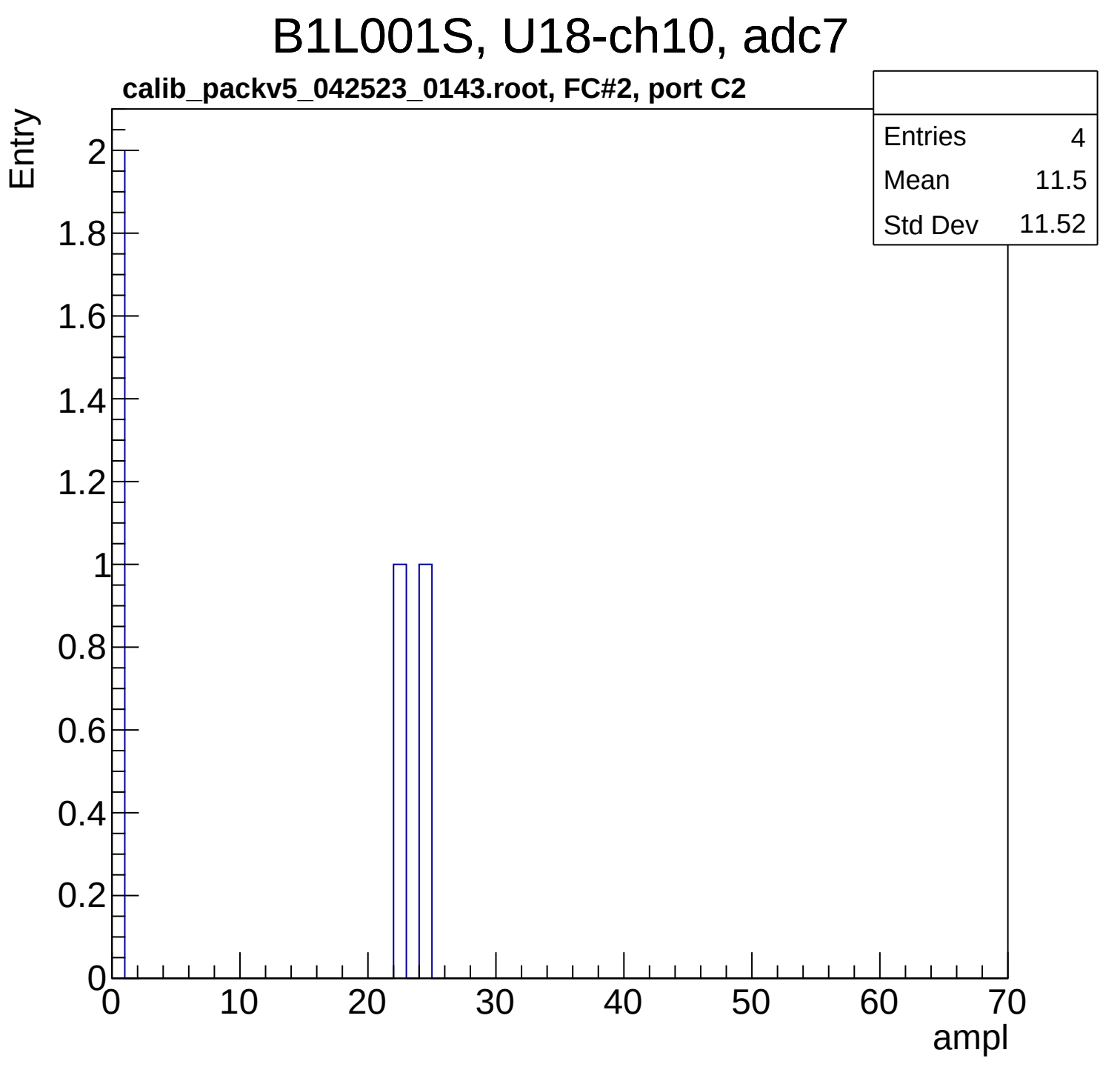

B1L001S, U18-ch10, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 122
Mean 42.8
Std Dev 3.167
Gaus mean : 43.4236
Gaus Width: 2.9806
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

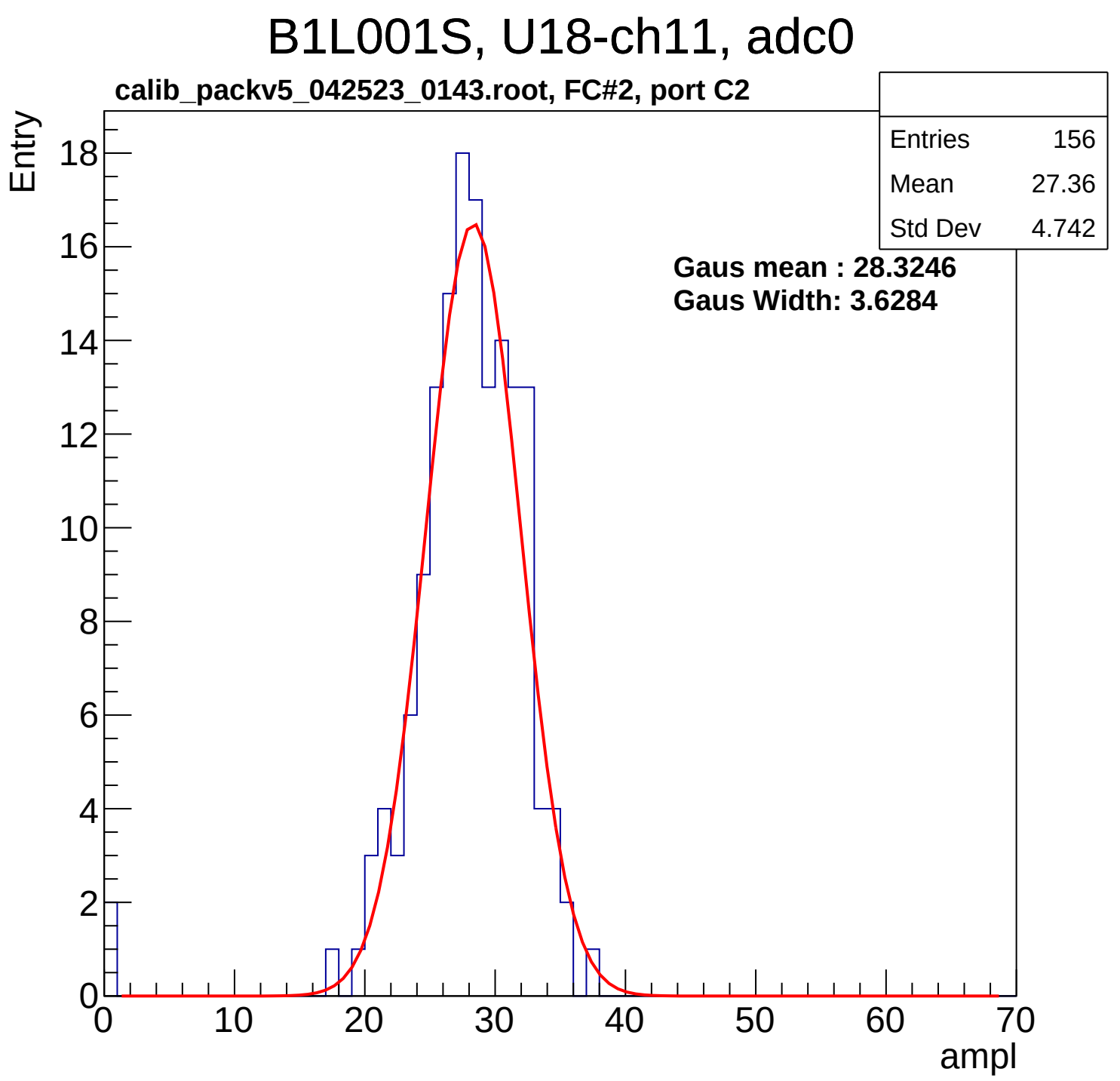

B1L001S, U18-ch10, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 135
Mean 49.48
Std Dev 3.277
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

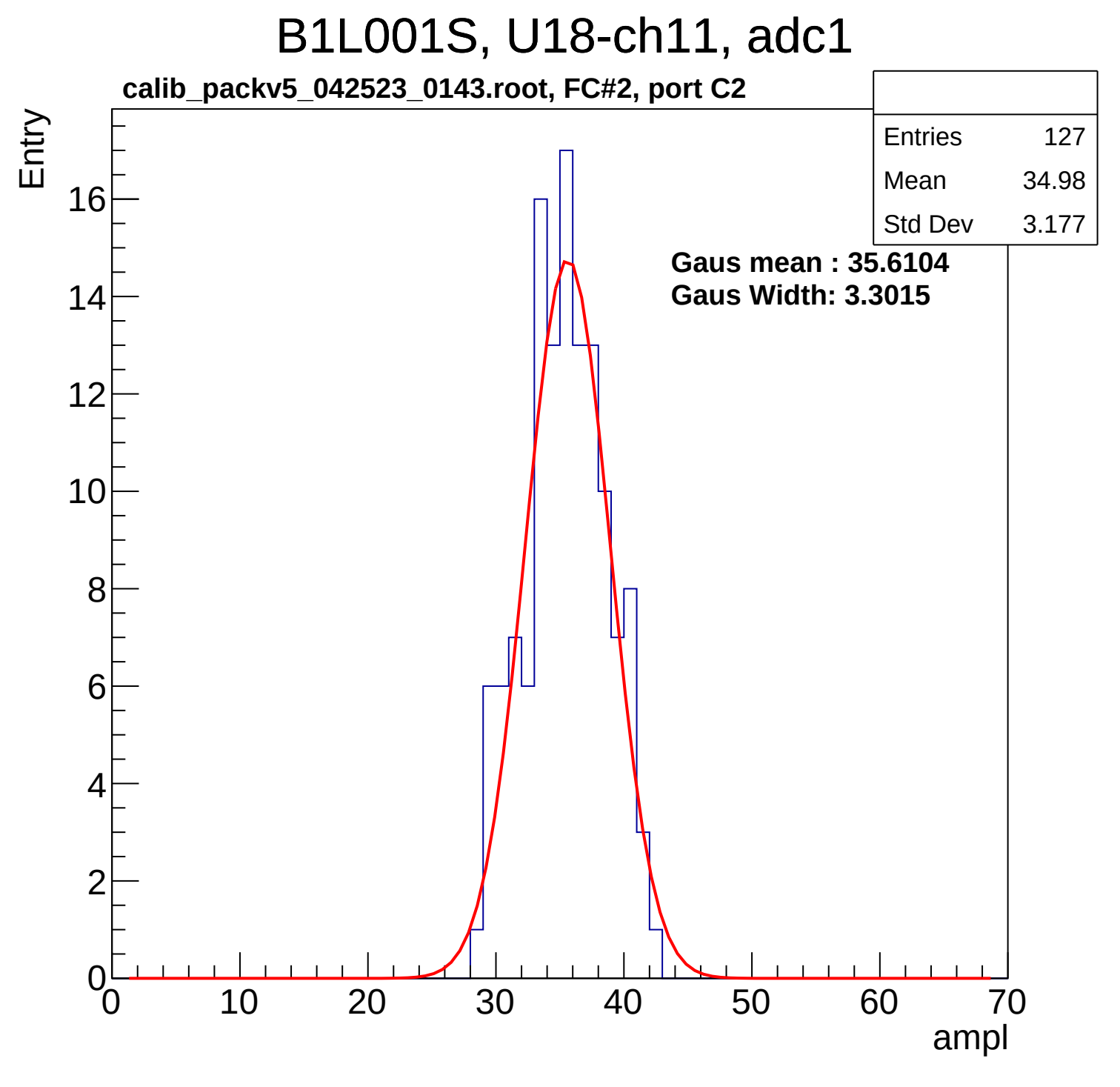

B1L001S, U18-ch10, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 130
Mean 55.68
Std Dev 3.23
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

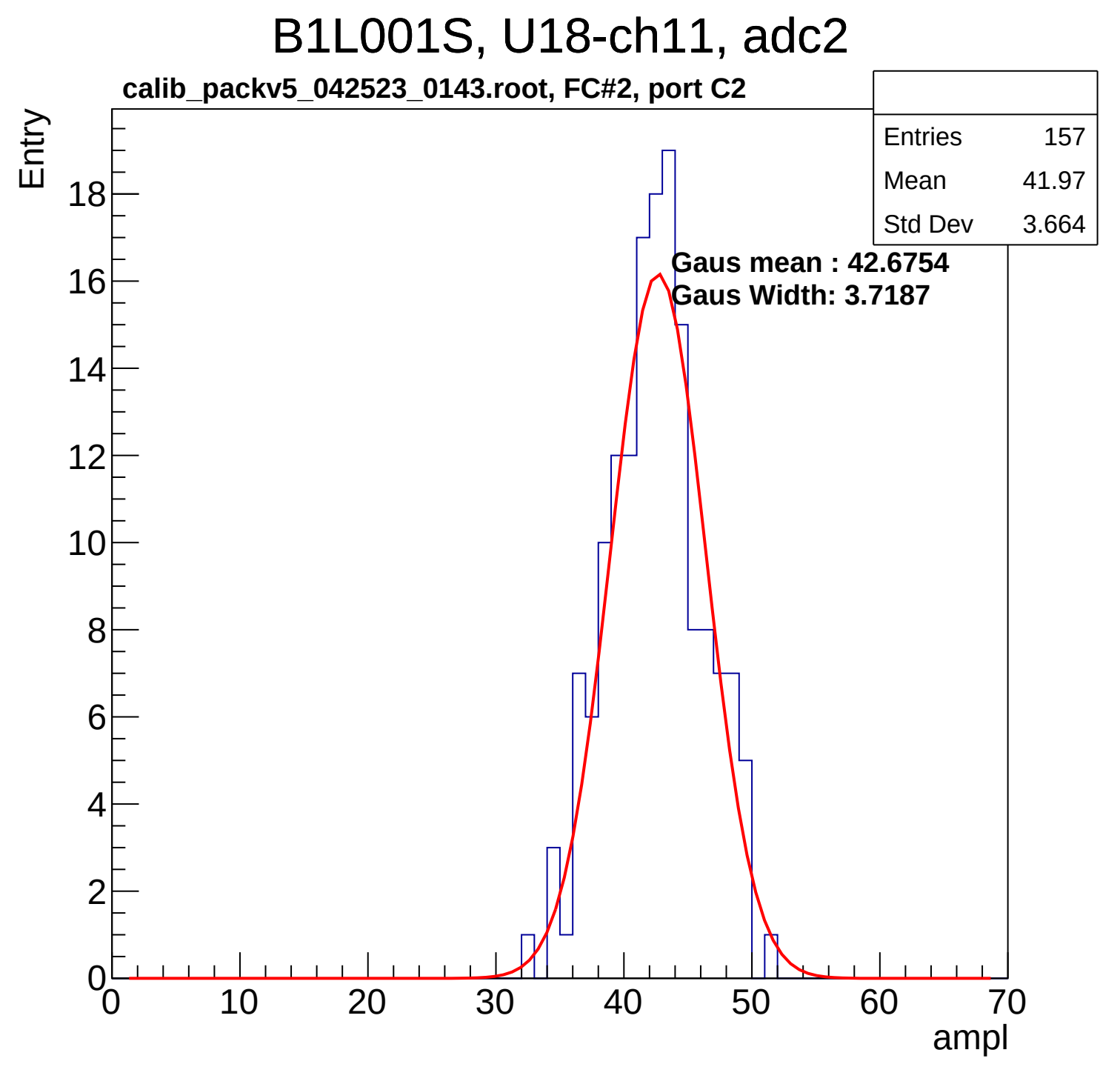

B1L001S, U18-ch10, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 76
Mean 59.75
Std Dev 7.125
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl

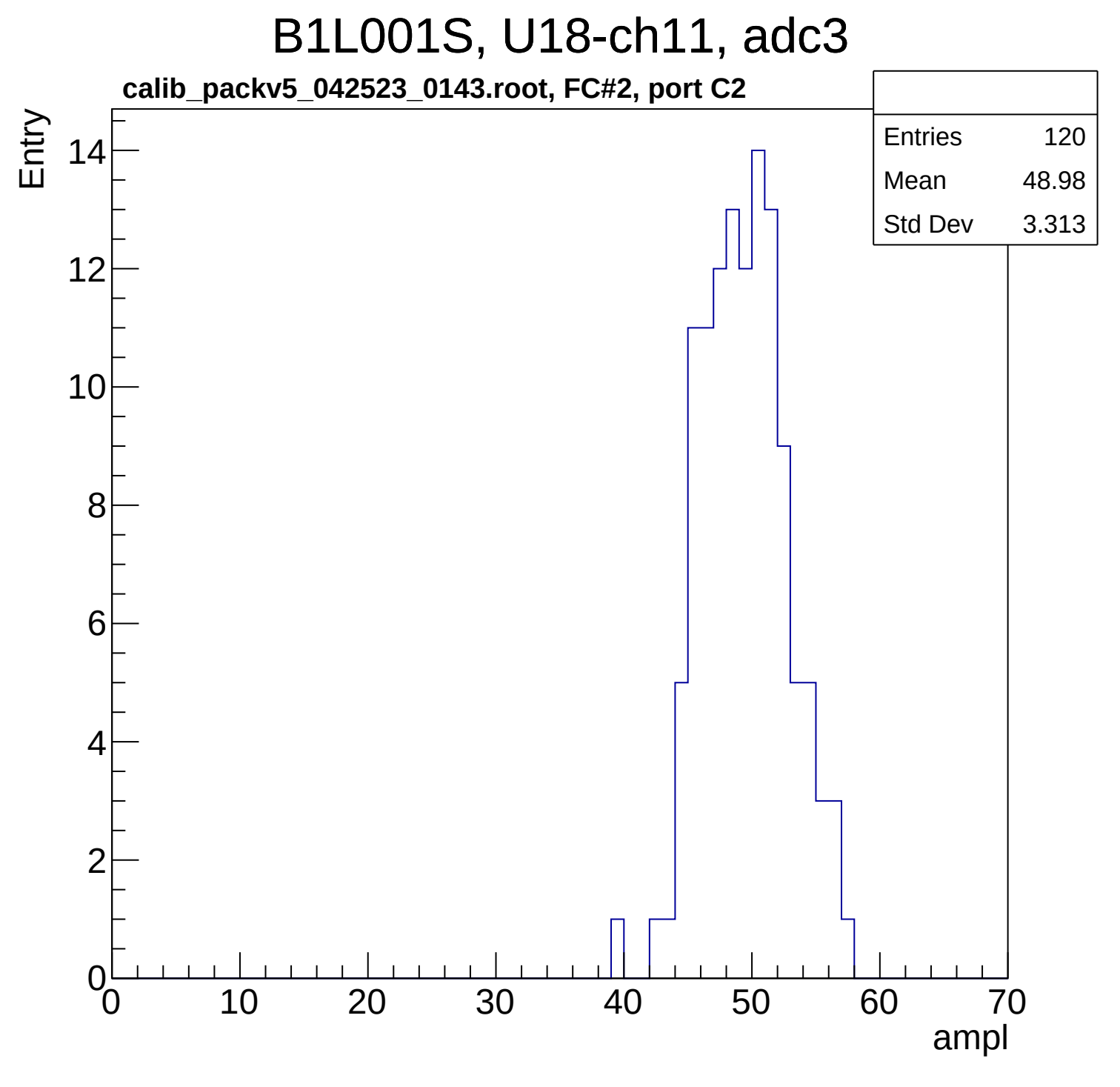

B1L001S, U18-ch10, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 12
Mean 57.17
Std Dev 17.26
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

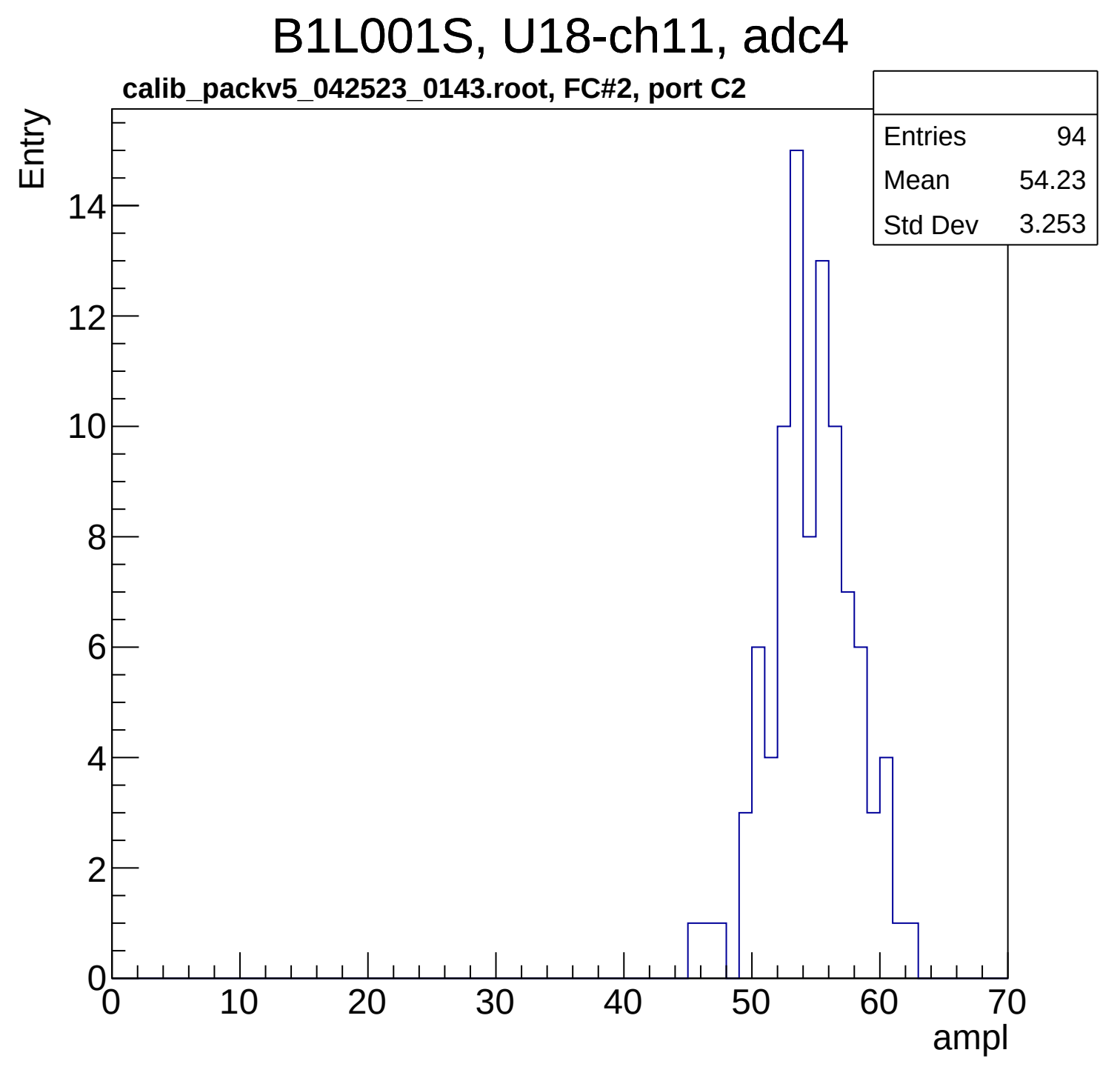

B1L001S, U18-ch10, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 4
Mean 11.5
Std Dev 11.52
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

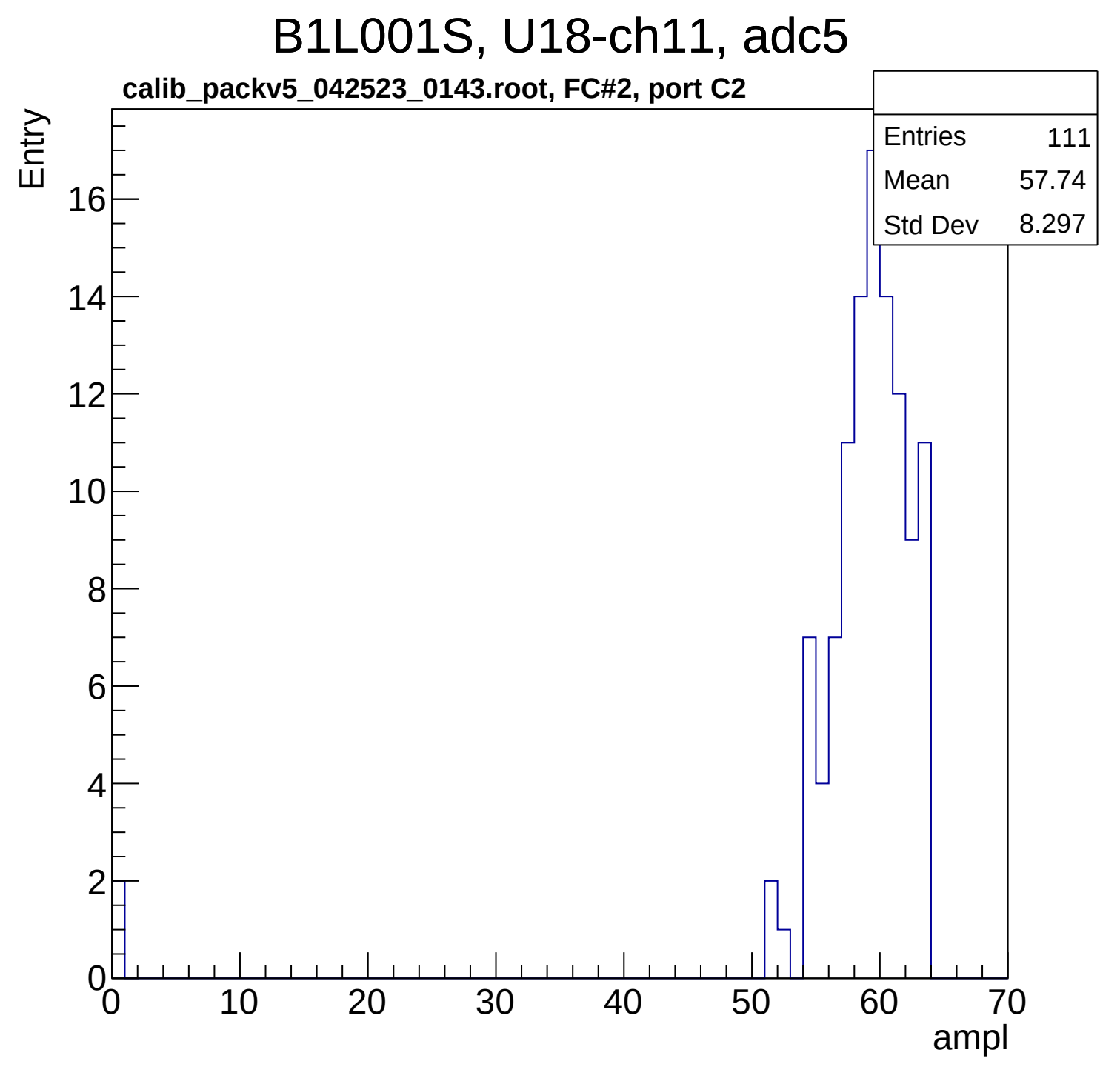

B1L001S, U18-ch11, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 156
Mean 27.36
Std Dev 4.742
Gaus mean : 28.3246
Gaus Width: 3.6284
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

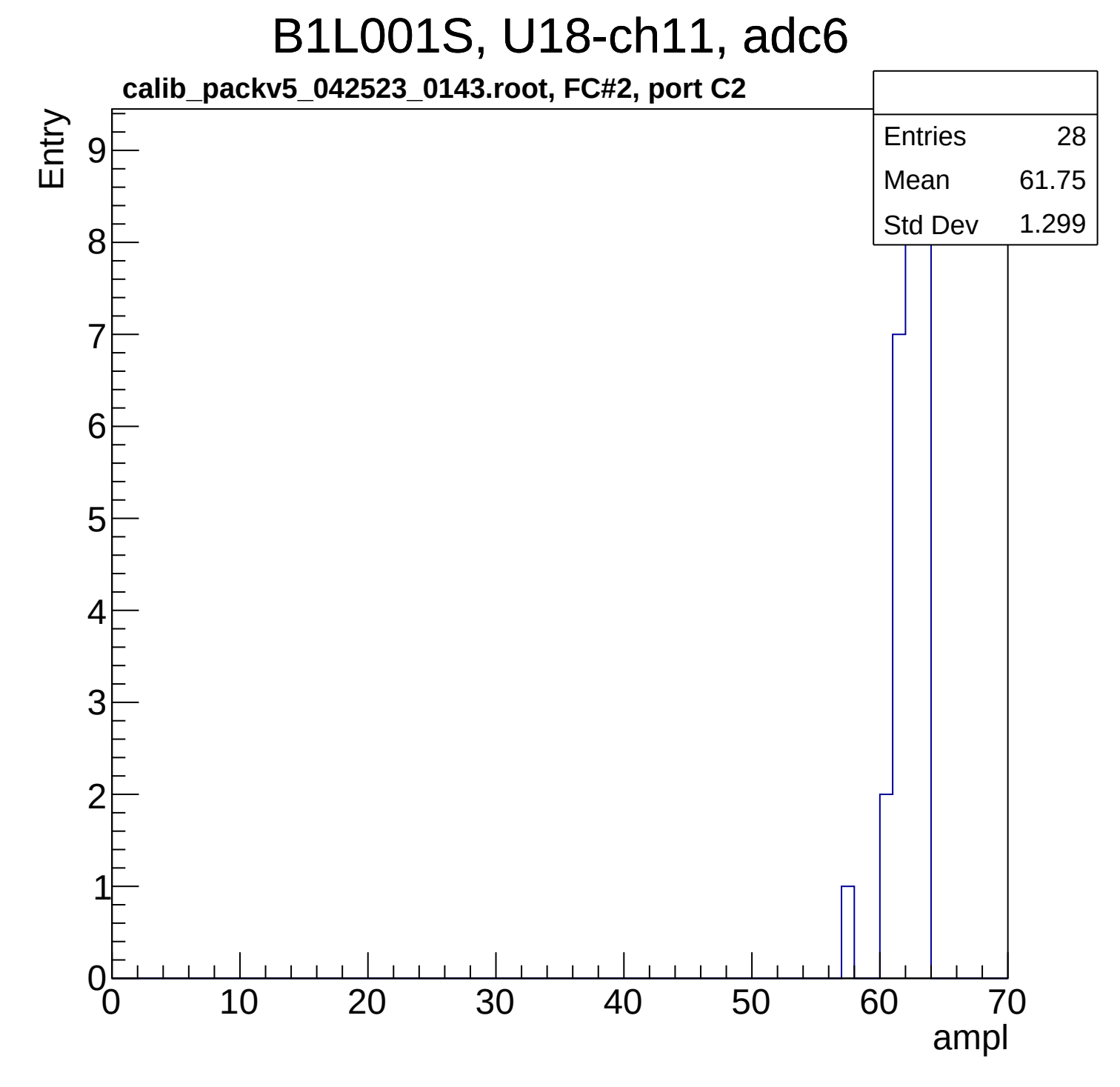

B1L001S, U18-ch11, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 127
Mean 34.98
Std Dev 3.177
Gaus mean : 35.6104
Gaus Width: 3.3015
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

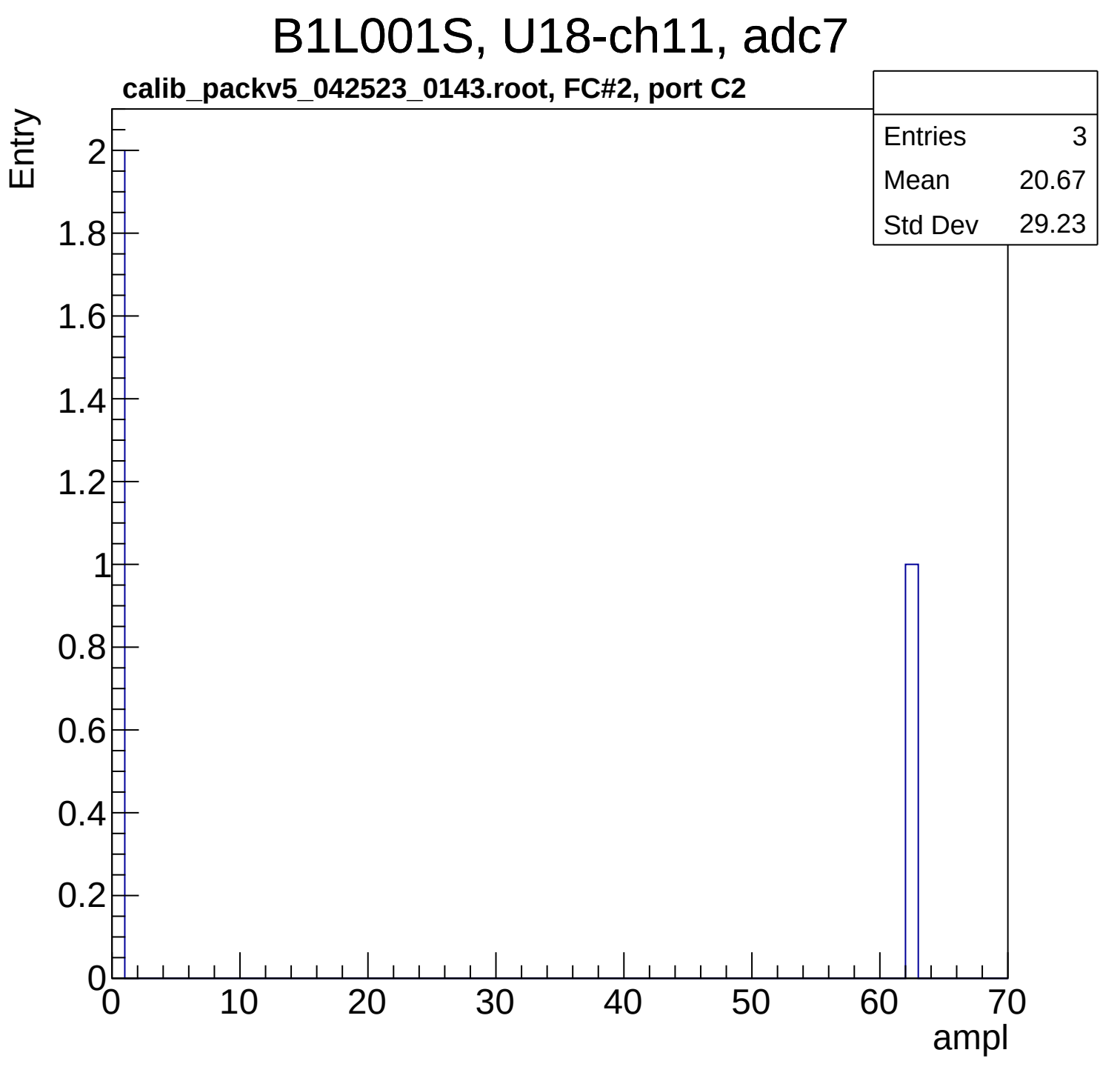

B1L001S, U18-ch11, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 157
Mean 41.97
Std Dev 3.664
Gaus mean : 42.6754
Gaus Width: 3.7187
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

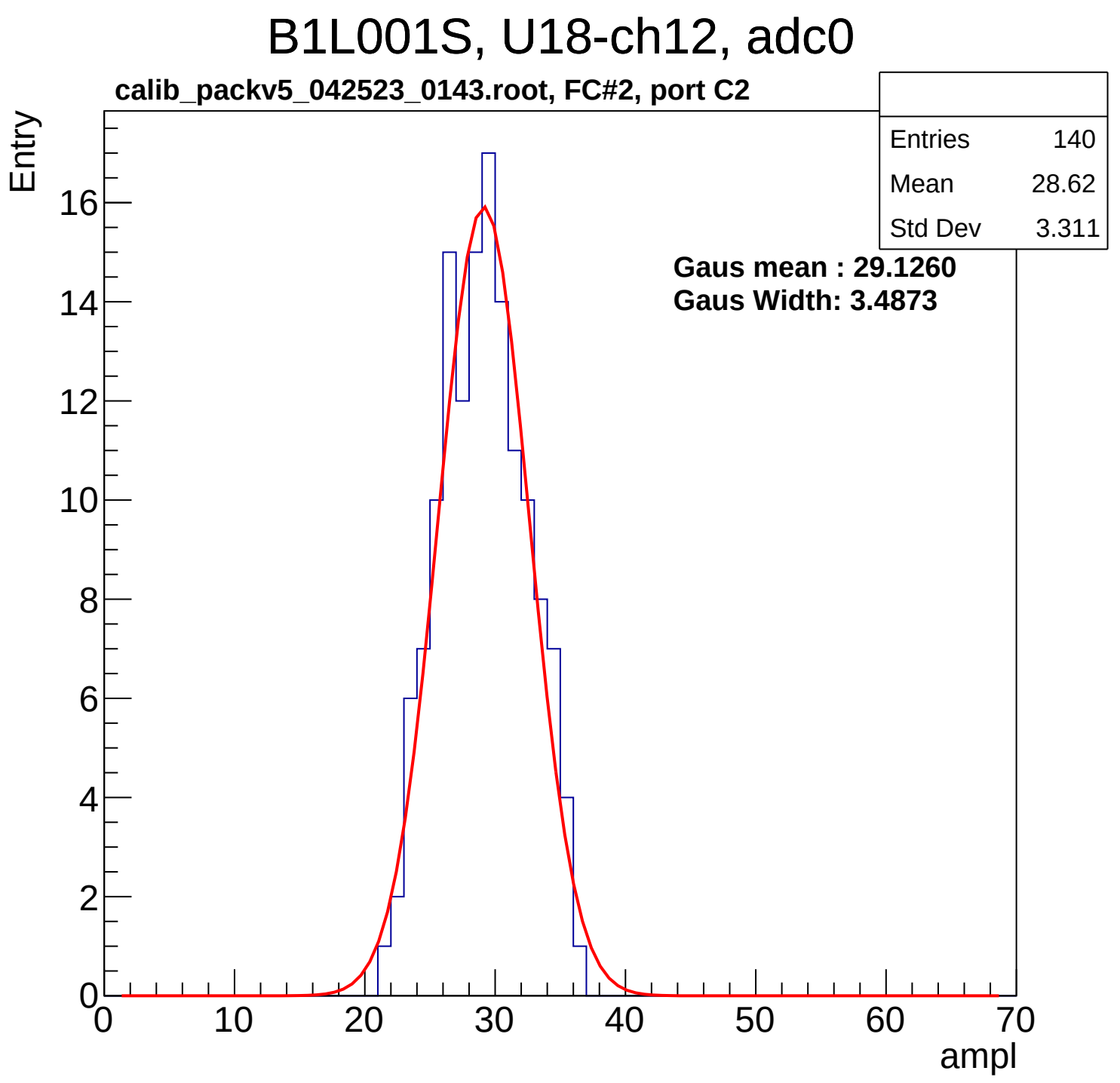

B1L001S, U18-ch11, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 120
Mean 48.98
Std Dev 3.313
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

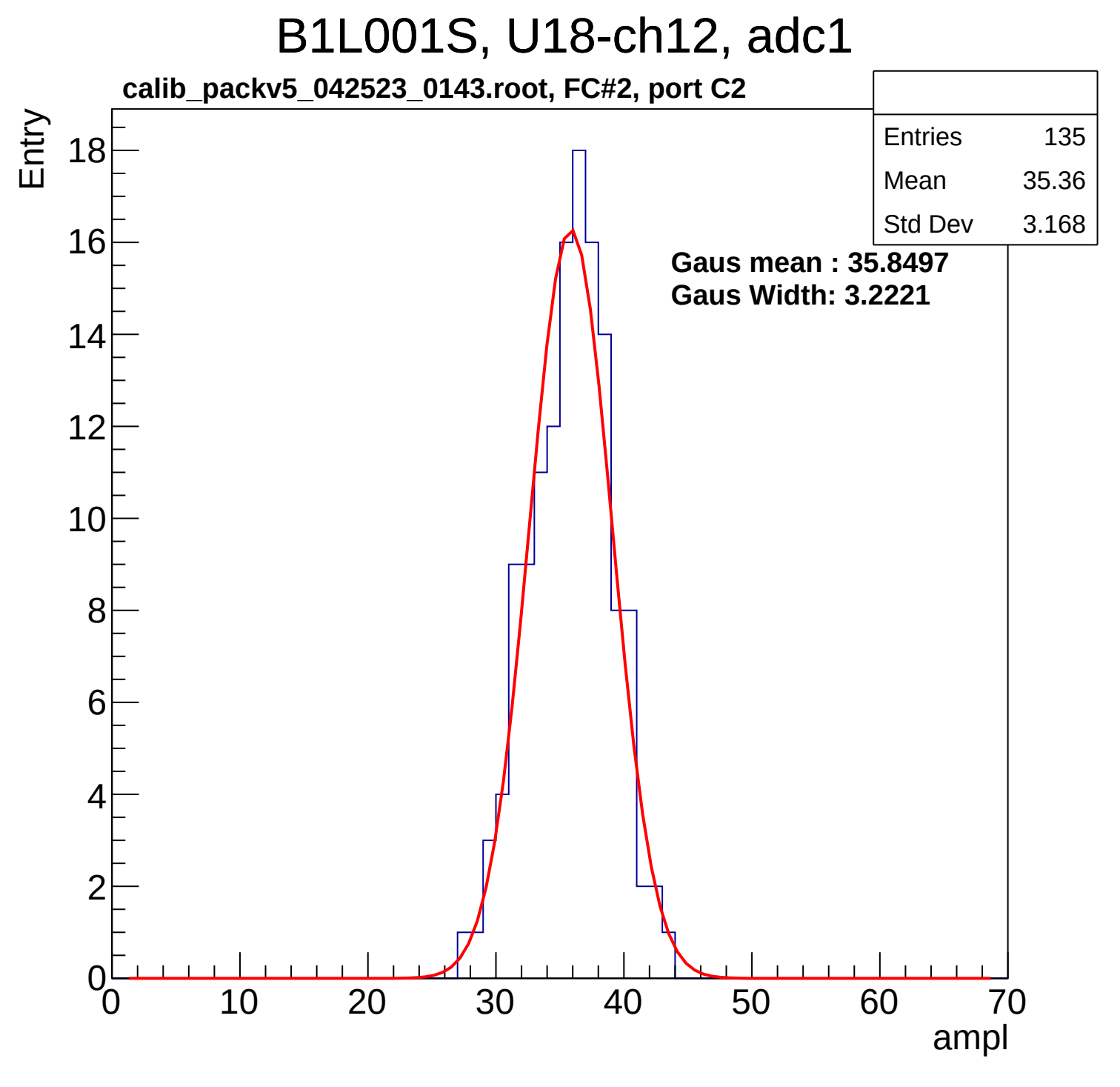

B1L001S, U18-ch11, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 94
Mean 54.23
Std Dev 3.253
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl

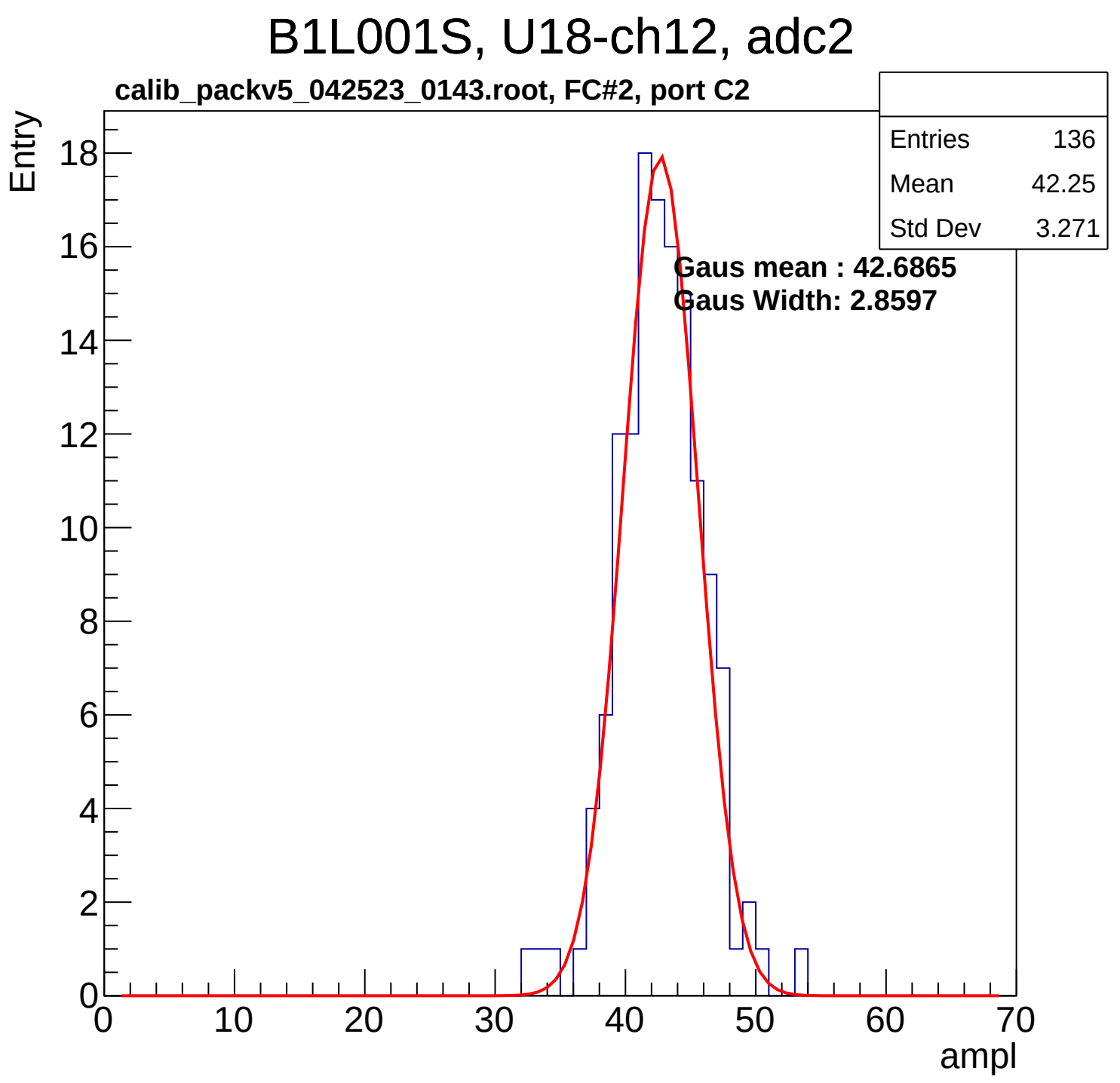

B1L001S, U18-ch11, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 111
Mean 57.74
Std Dev 8.297
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

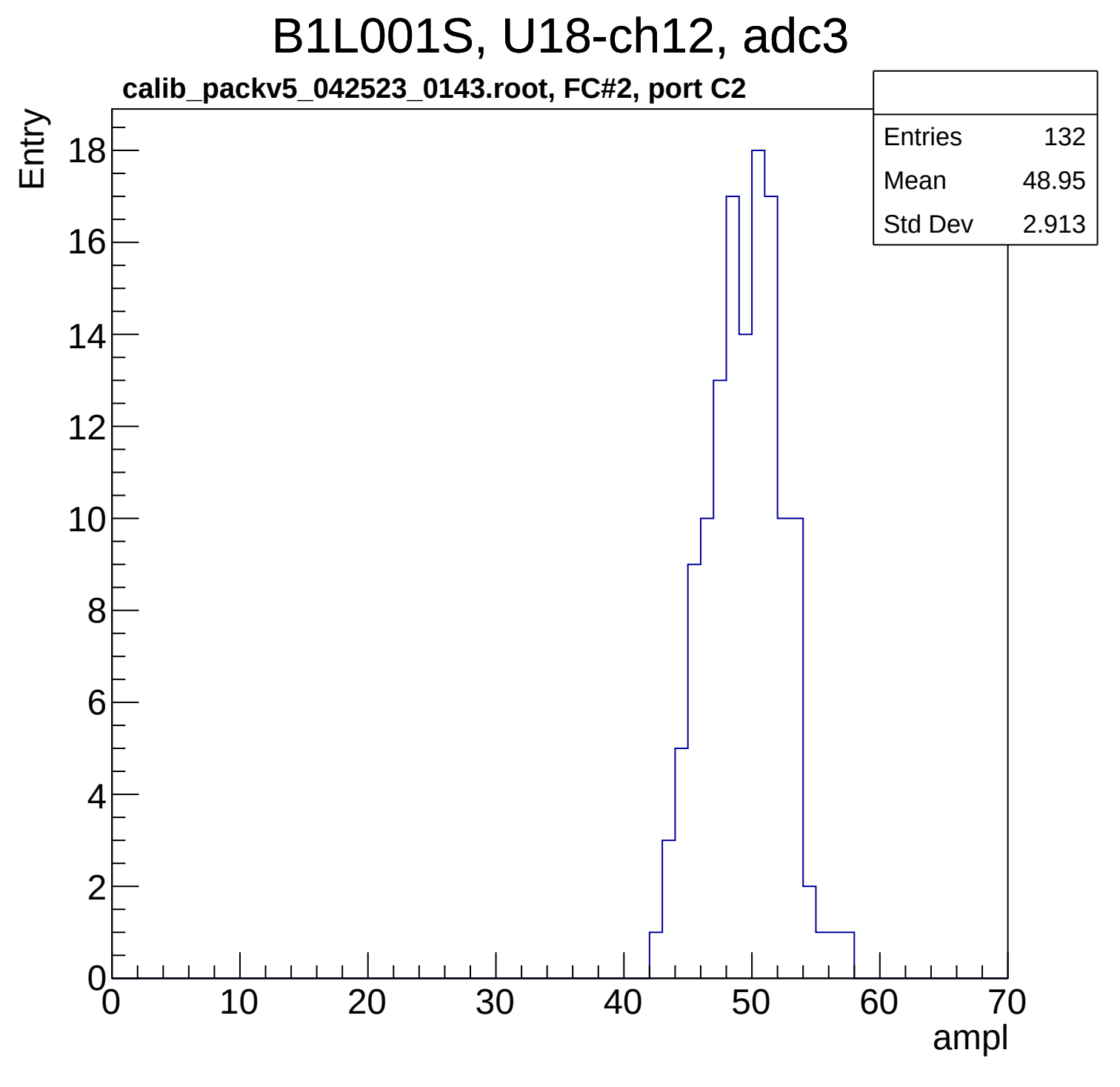

B1L001S, U18-ch11, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 28
Mean 61.75
Std Dev 1.299
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

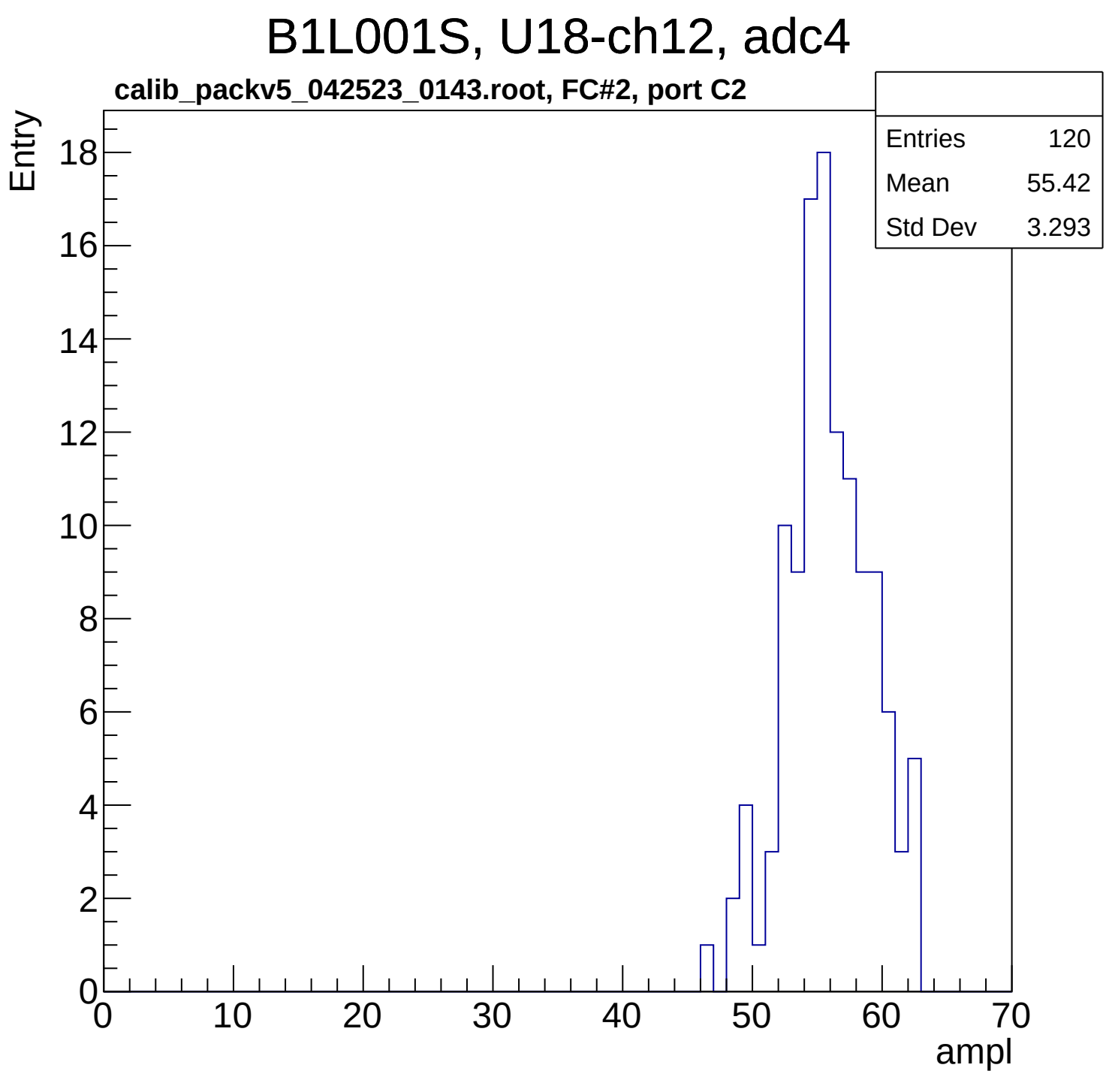

B1L001S, U18-ch11, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 3
Mean 20.67
Std Dev 29.23
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

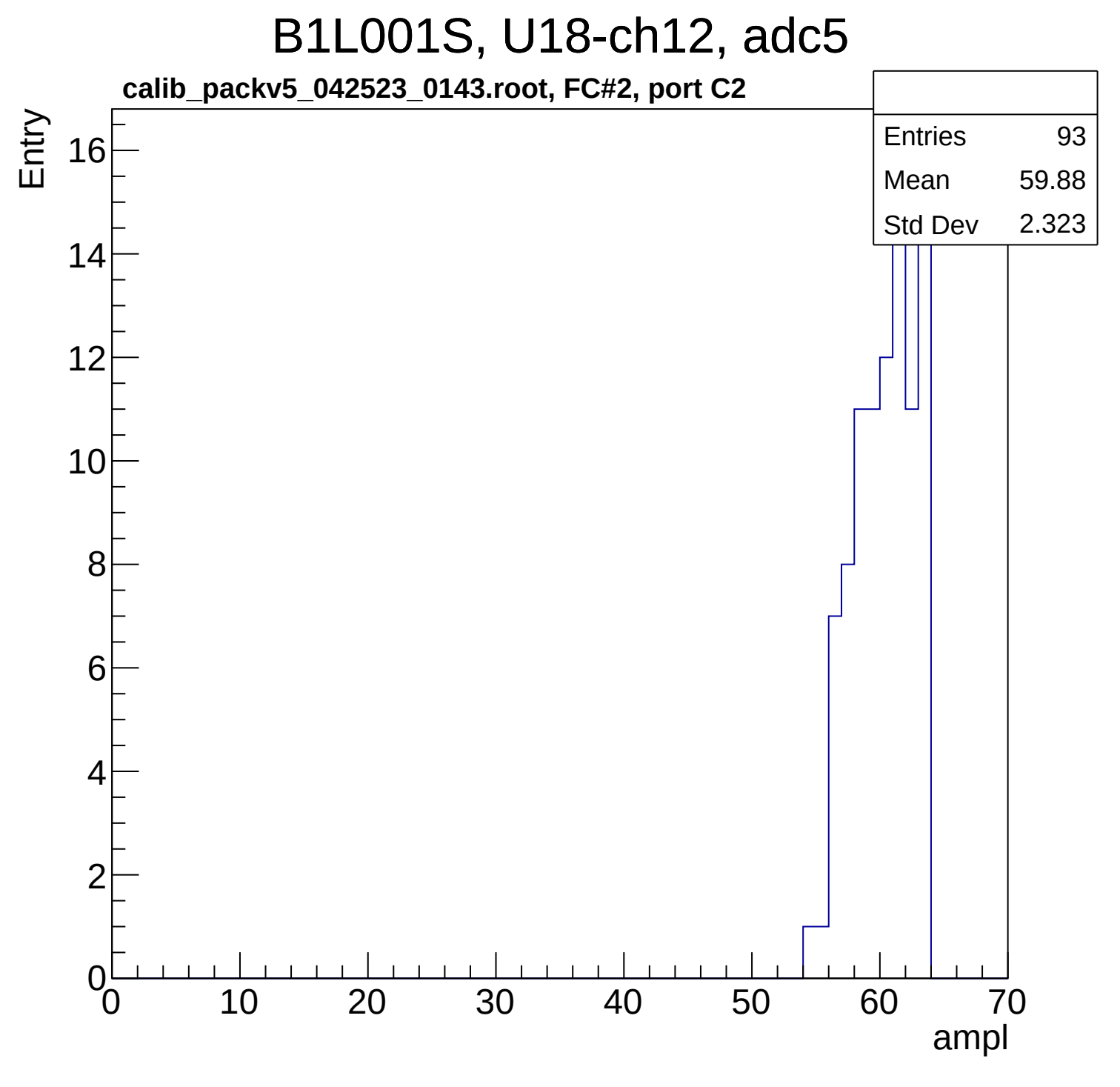

B1L001S, U18-ch12, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 140
Mean 28.62
Std Dev 3.311
Gaus mean : 29.1260
Gaus Width: 3.4873
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

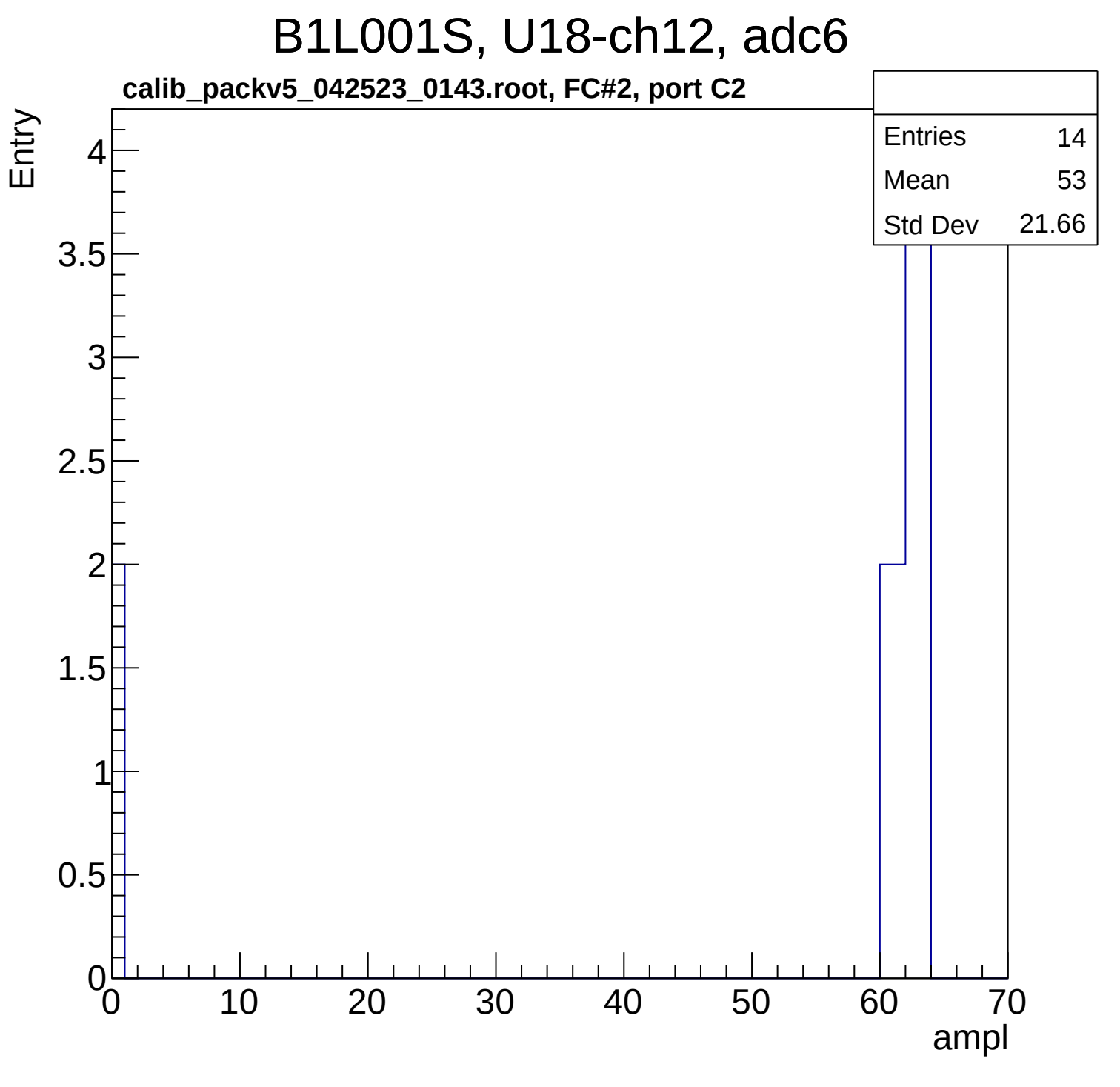

B1L001S, U18-ch12, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 135
Mean 35.36
Std Dev 3.168
Gaus mean : 35.8497
Gaus Width: 3.2221
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

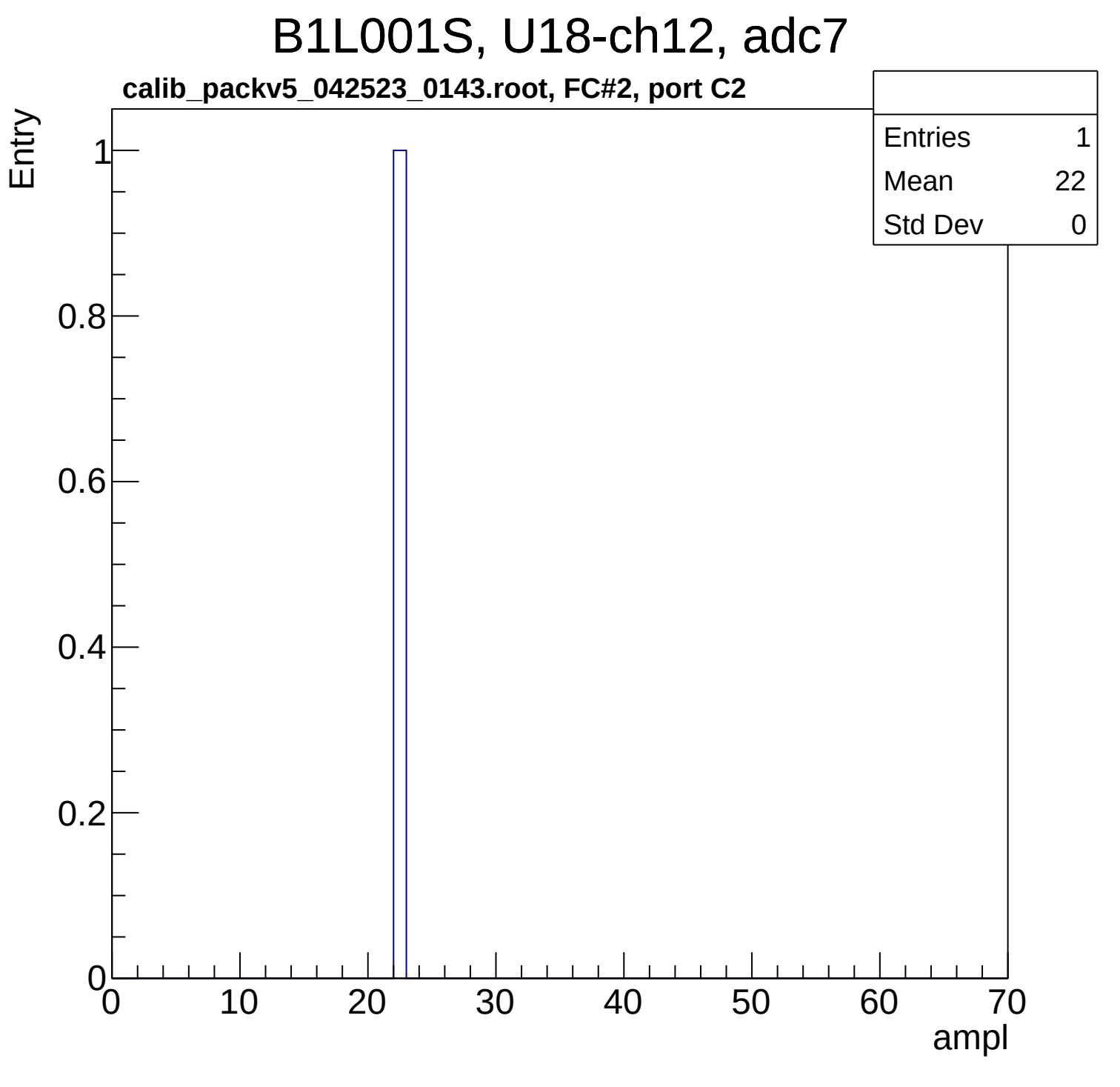

B1L001S, U18-ch12, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 136
Mean 42.25
Std Dev 3.271
Gaus mean : 42.6865
Gaus Width: 2.8597
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

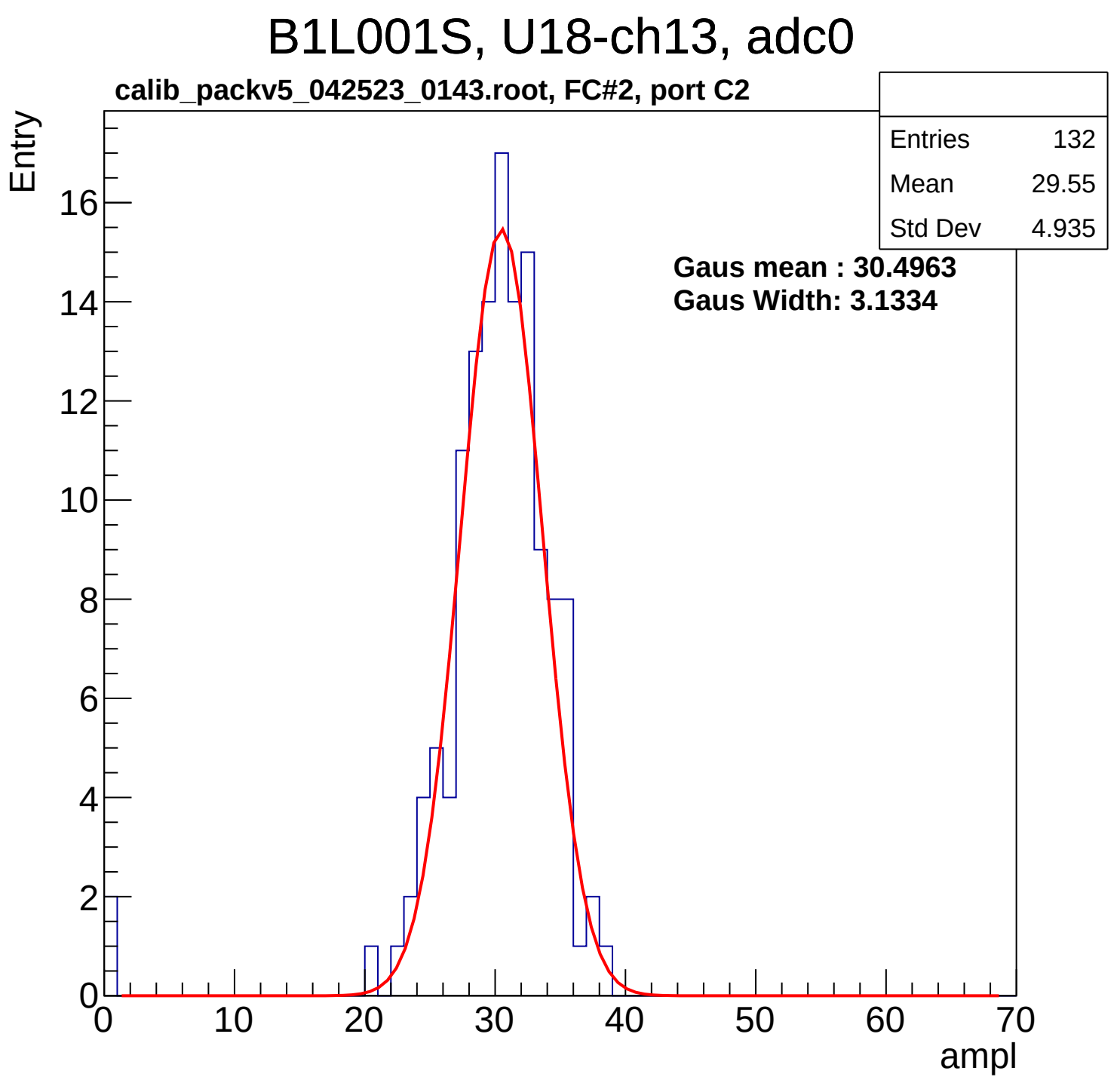

B1L001S, U18-ch12, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 132
Mean 48.95
Std Dev 2.913
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

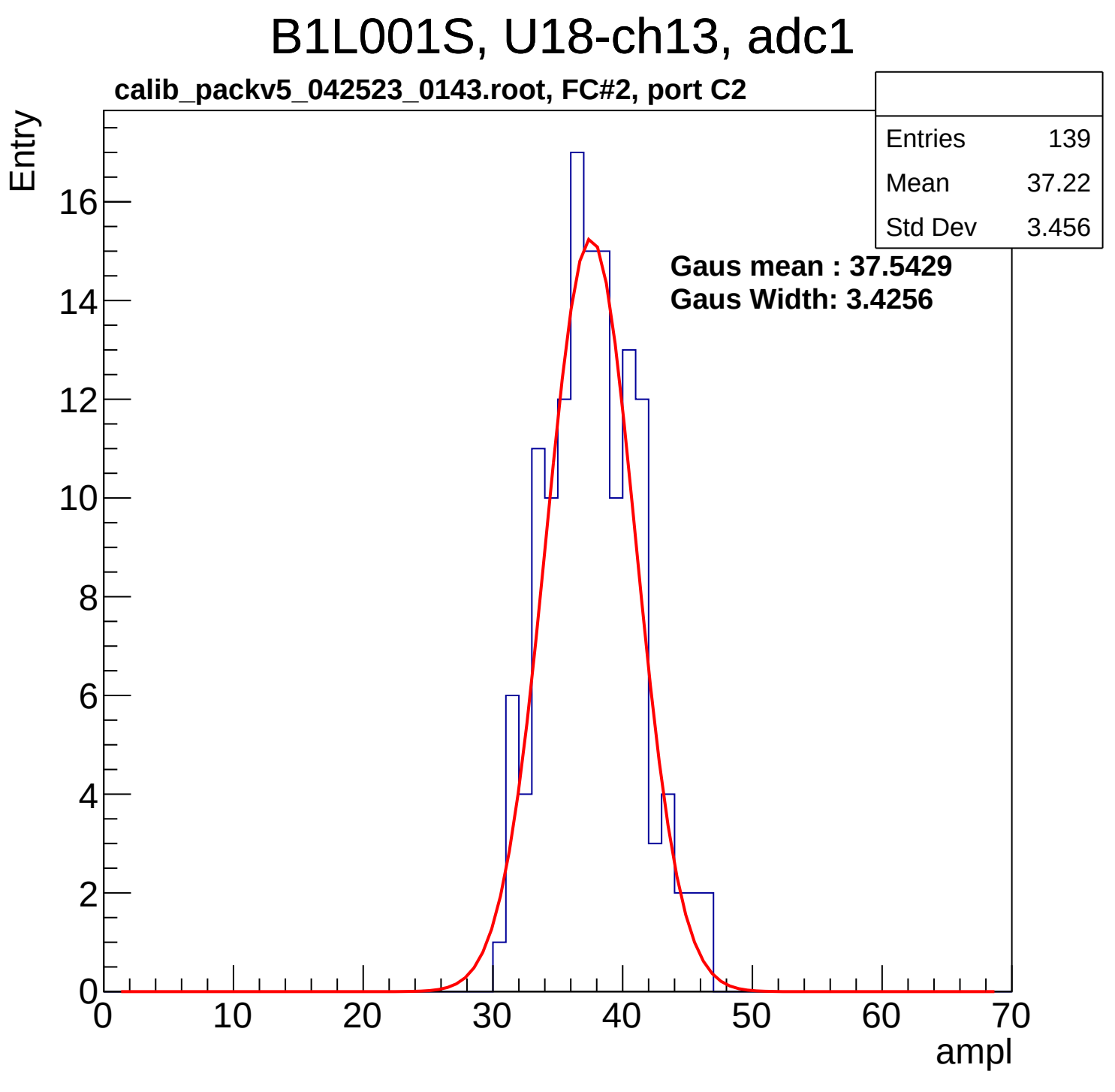

B1L001S, U18-ch12, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 120
Mean 55.42
Std Dev 3.293
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

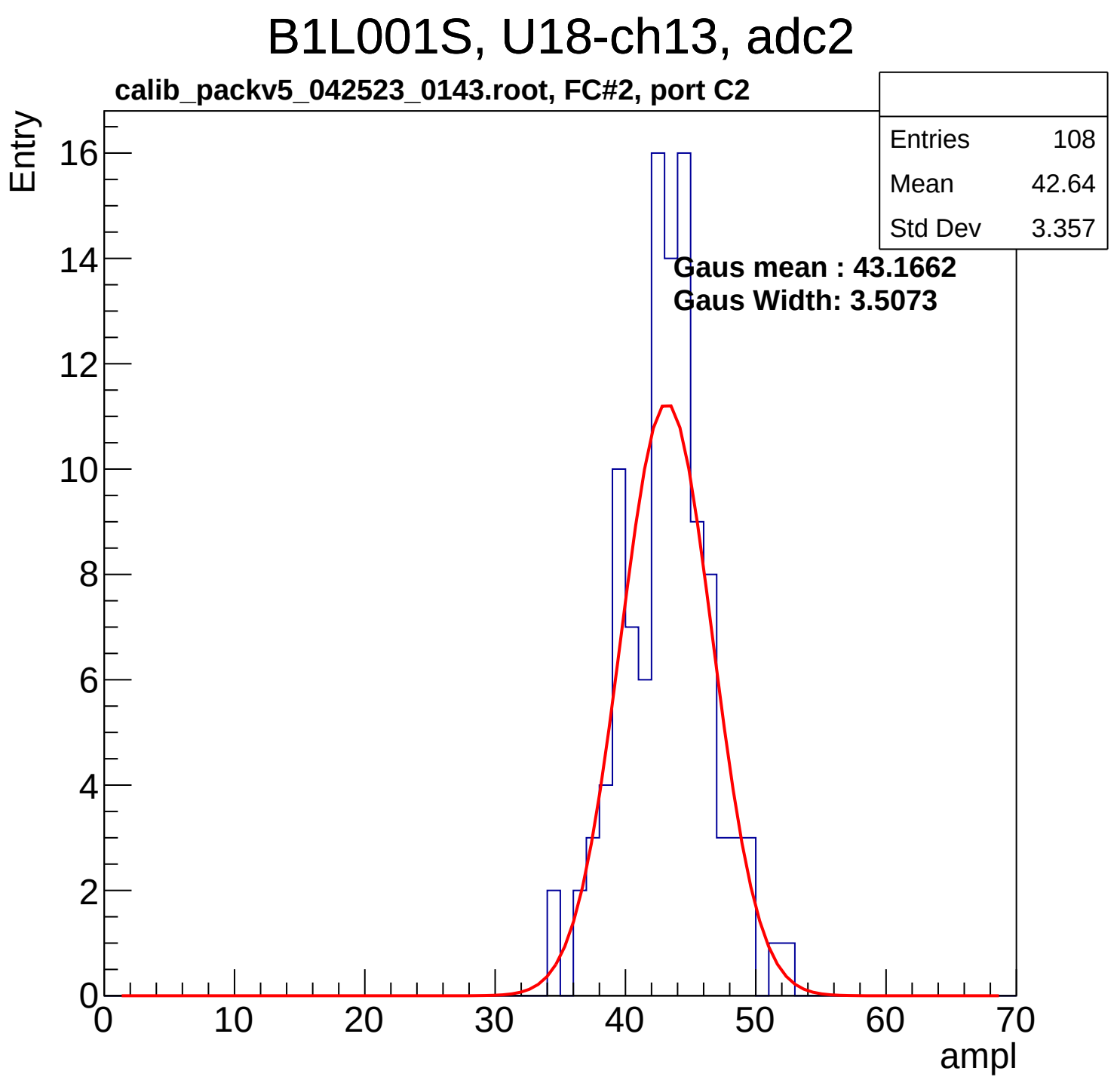

B1L001S, U18-ch12, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 93
Mean 59.88
Std Dev 2.323
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

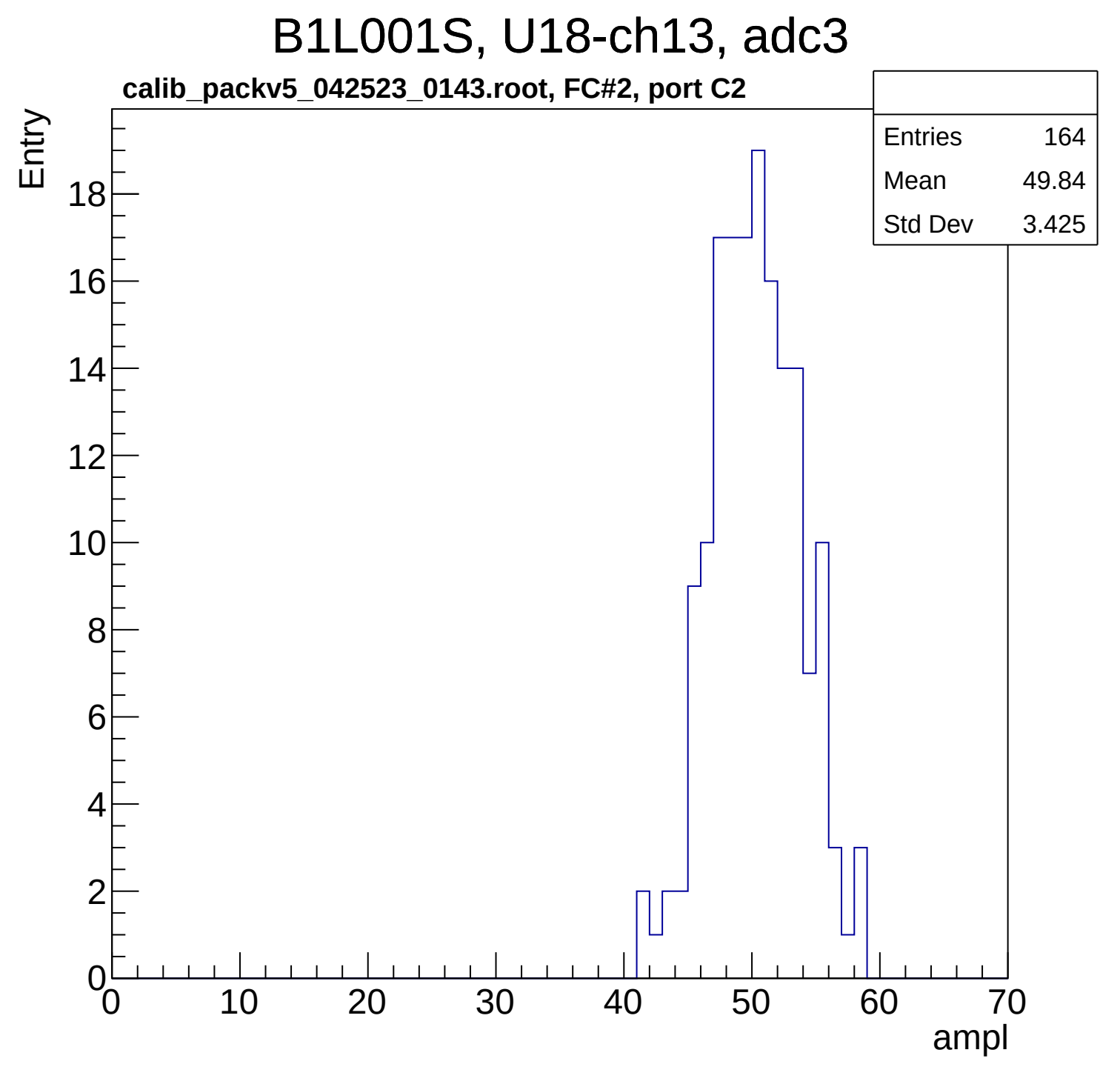

B1L001S, U18-ch12, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 14
Mean 53
Std Dev 21.66
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

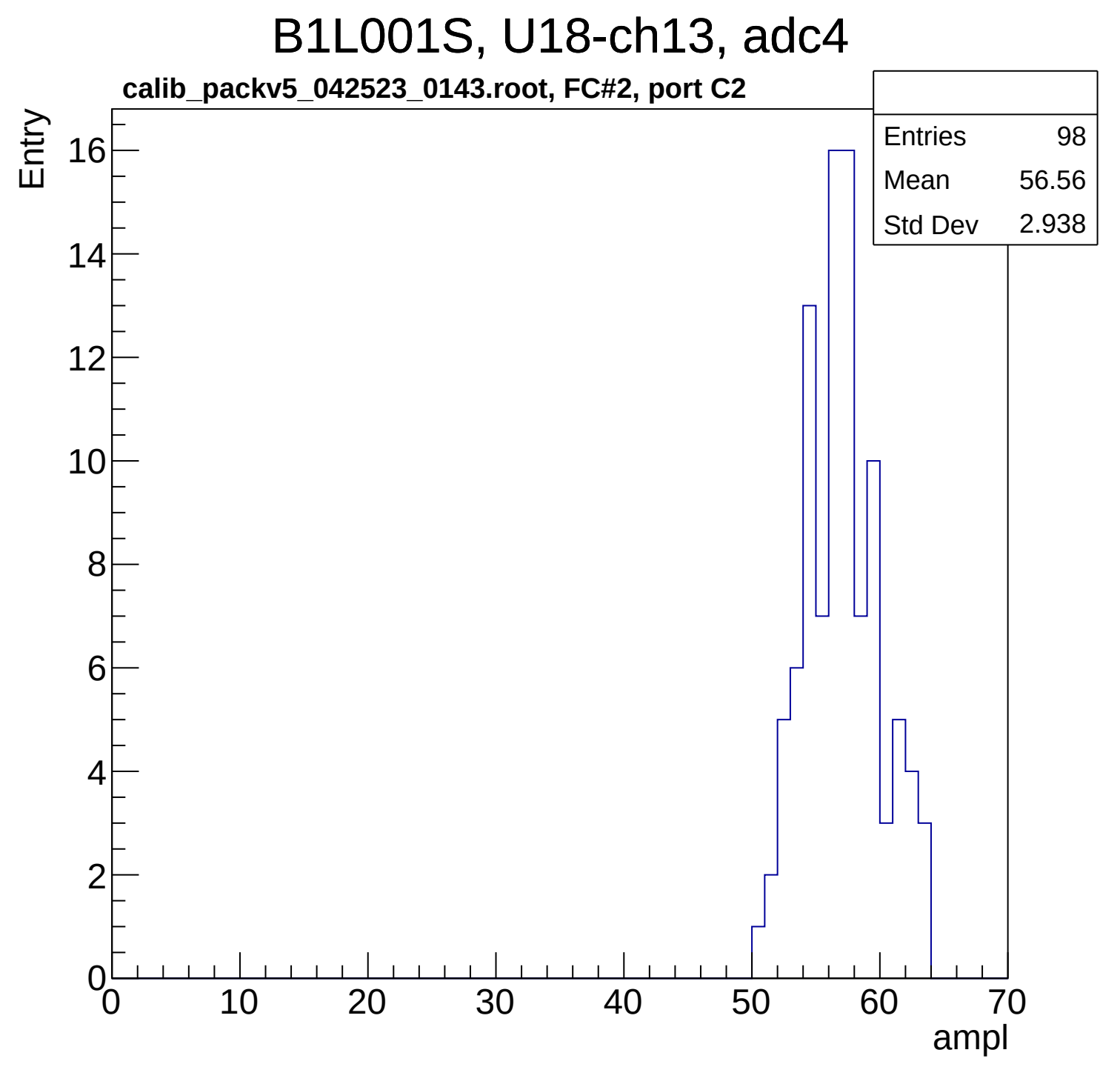

B1L001S, U18-ch12, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 22
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

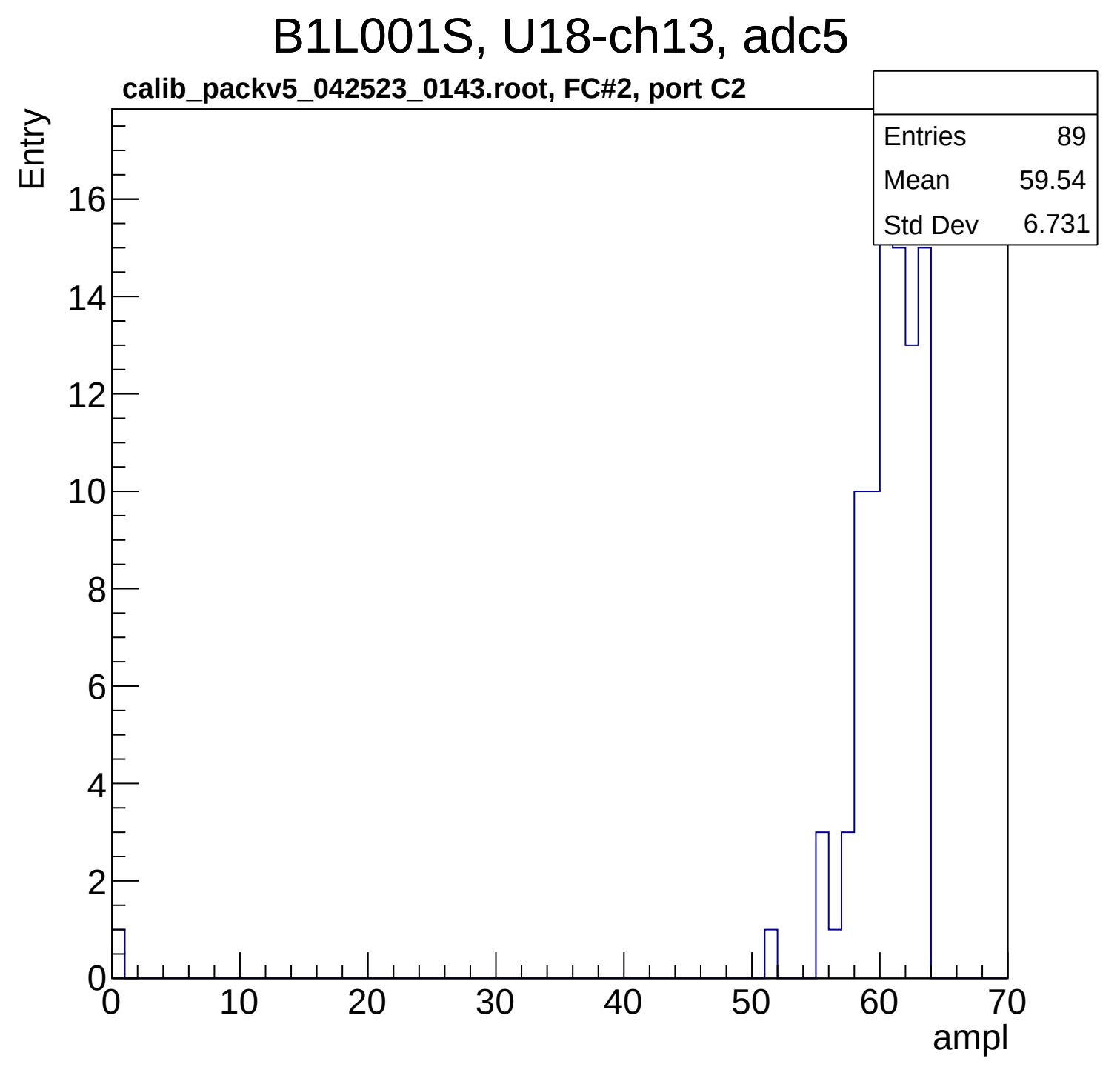

B1L001S, U18-ch13, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 132
Mean 29.55
Std Dev 4.935
Gaus mean : 30.4963
Gaus Width: 3.1334
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

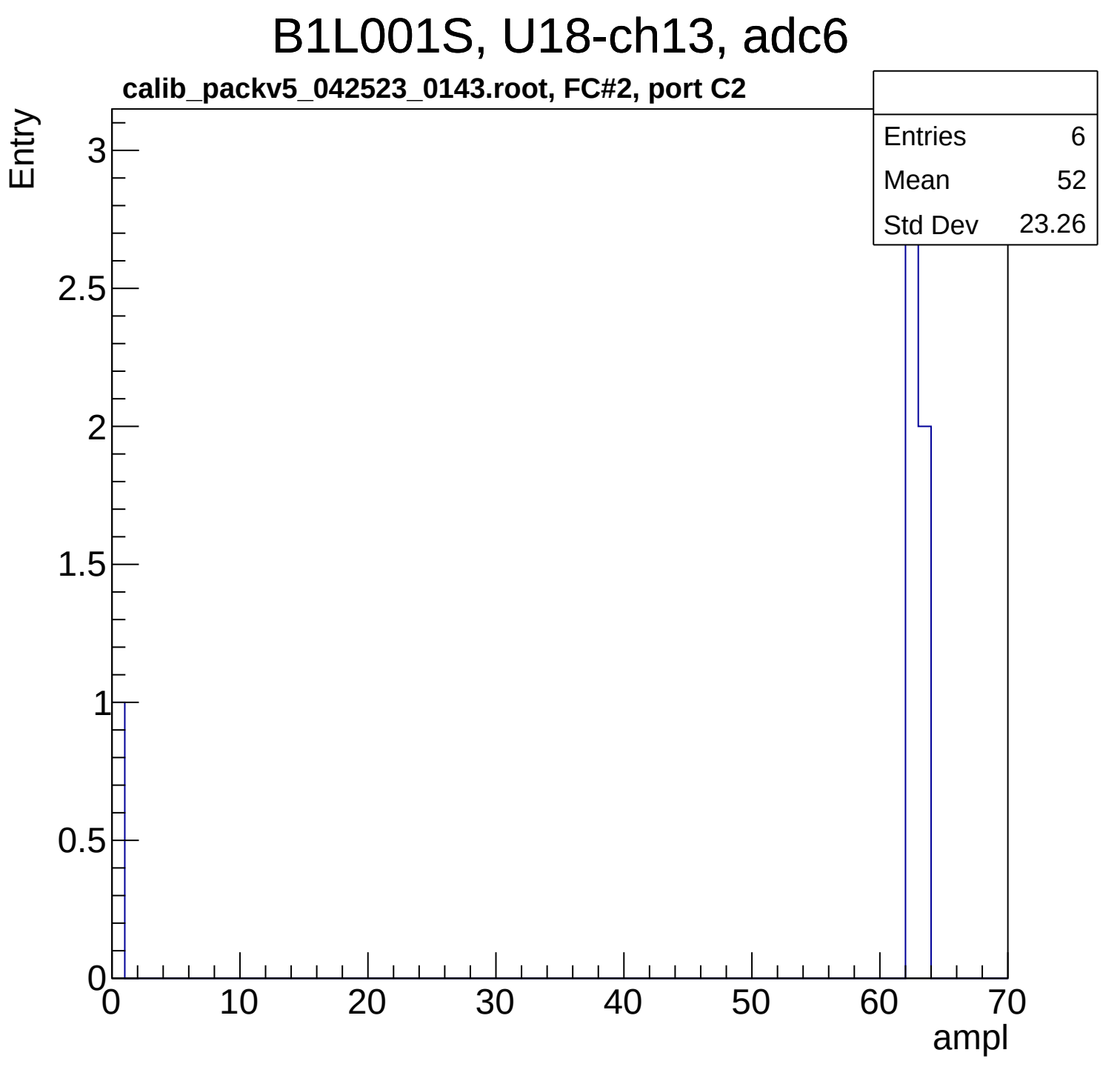

B1L001S, U18-ch13, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 139
Mean 37.22
Std Dev 3.456
Gaus mean : 37.5429
Gaus Width: 3.4256
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

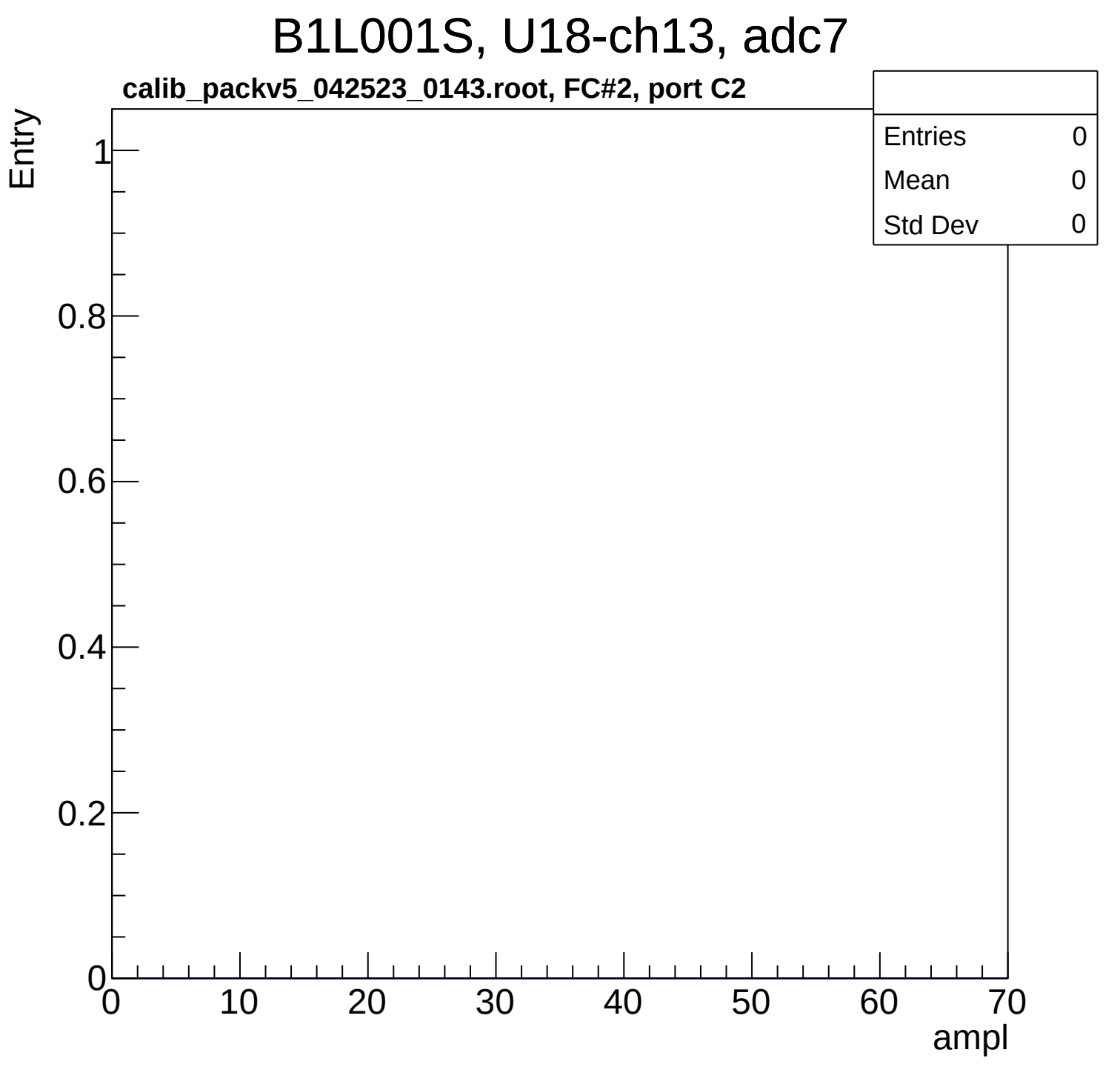

B1L001S, U18-ch13, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 108
Mean 42.64
Std Dev 3.357
Gaus mean : 43.1662
Gaus Width: 3.5073
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

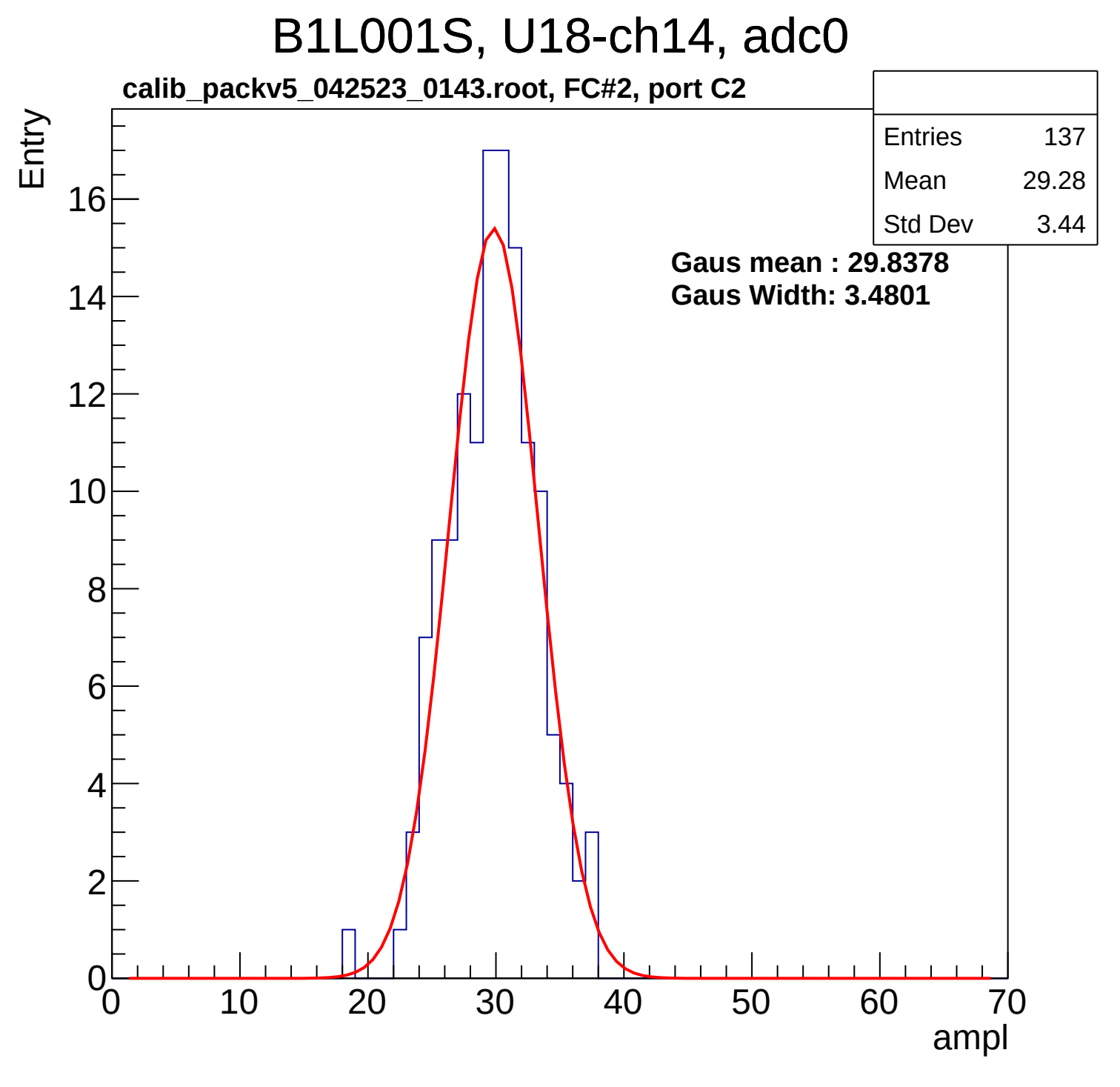

B1L001S, U18-ch13, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 164
Mean 49.84
Std Dev 3.425
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

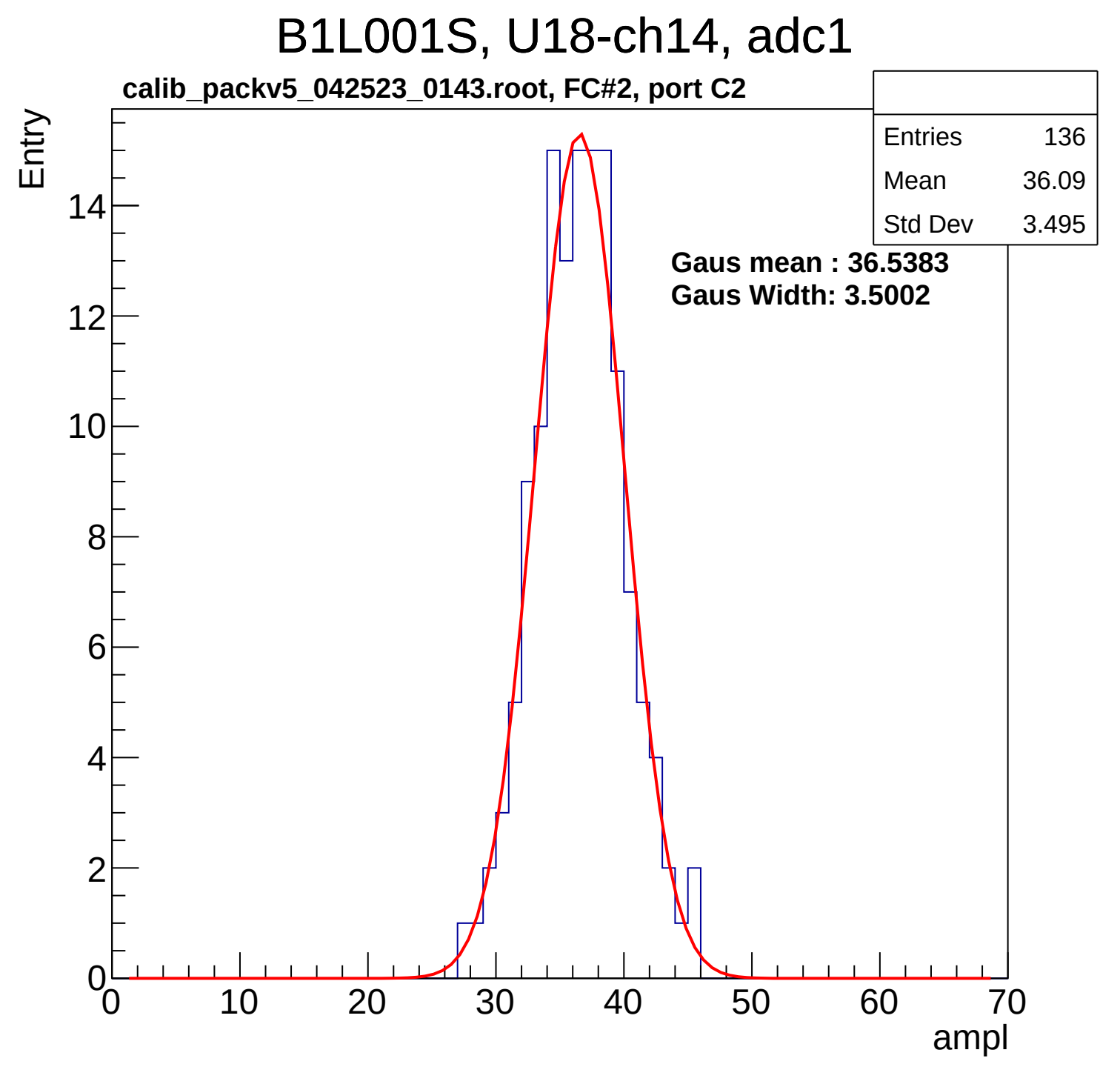

B1L001S, U18-ch13, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 98
Mean 56.56
Std Dev 2.938
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

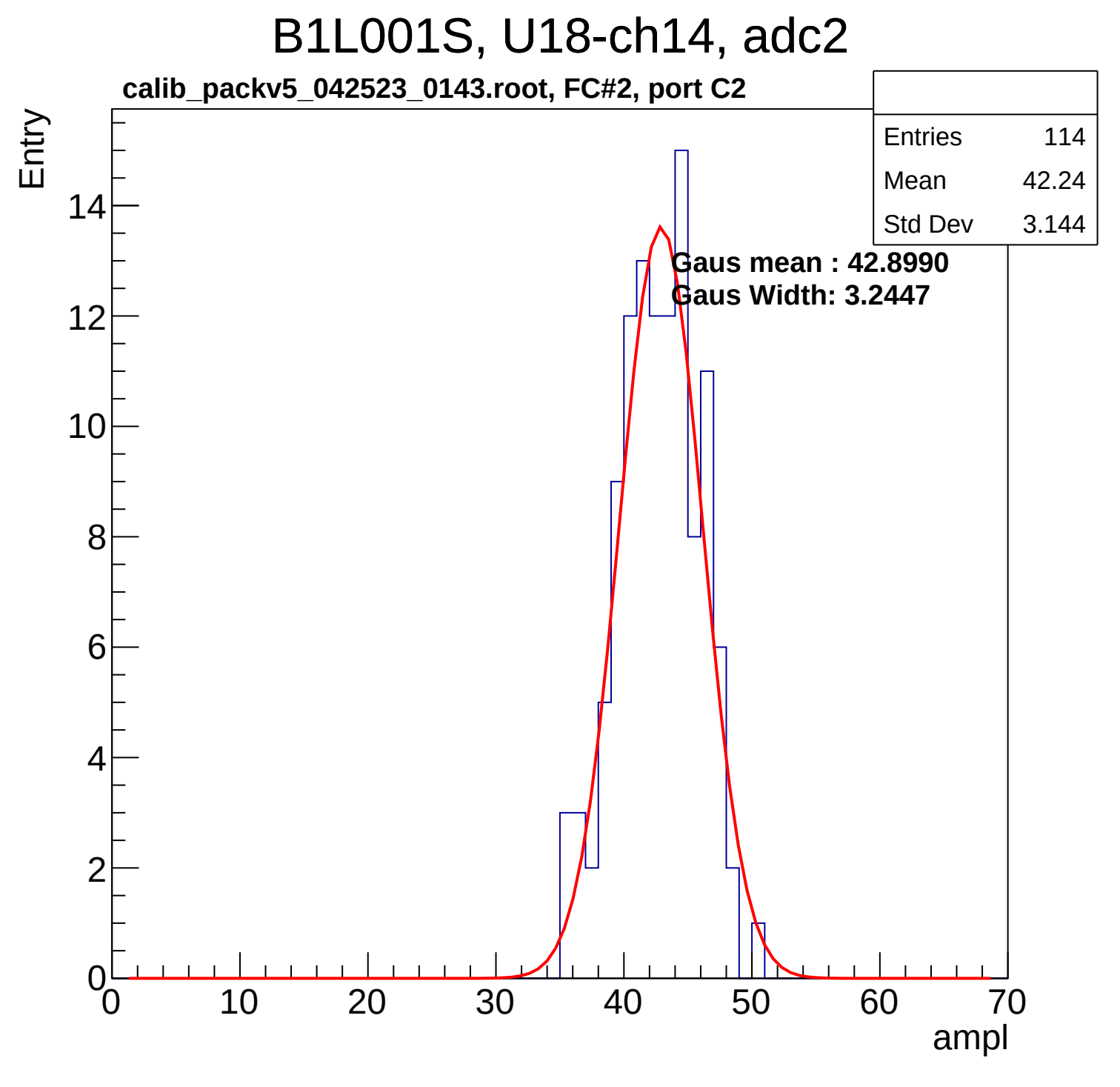

B1L001S, U18-ch13, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 89
Mean 59.54
Std Dev 6.731
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

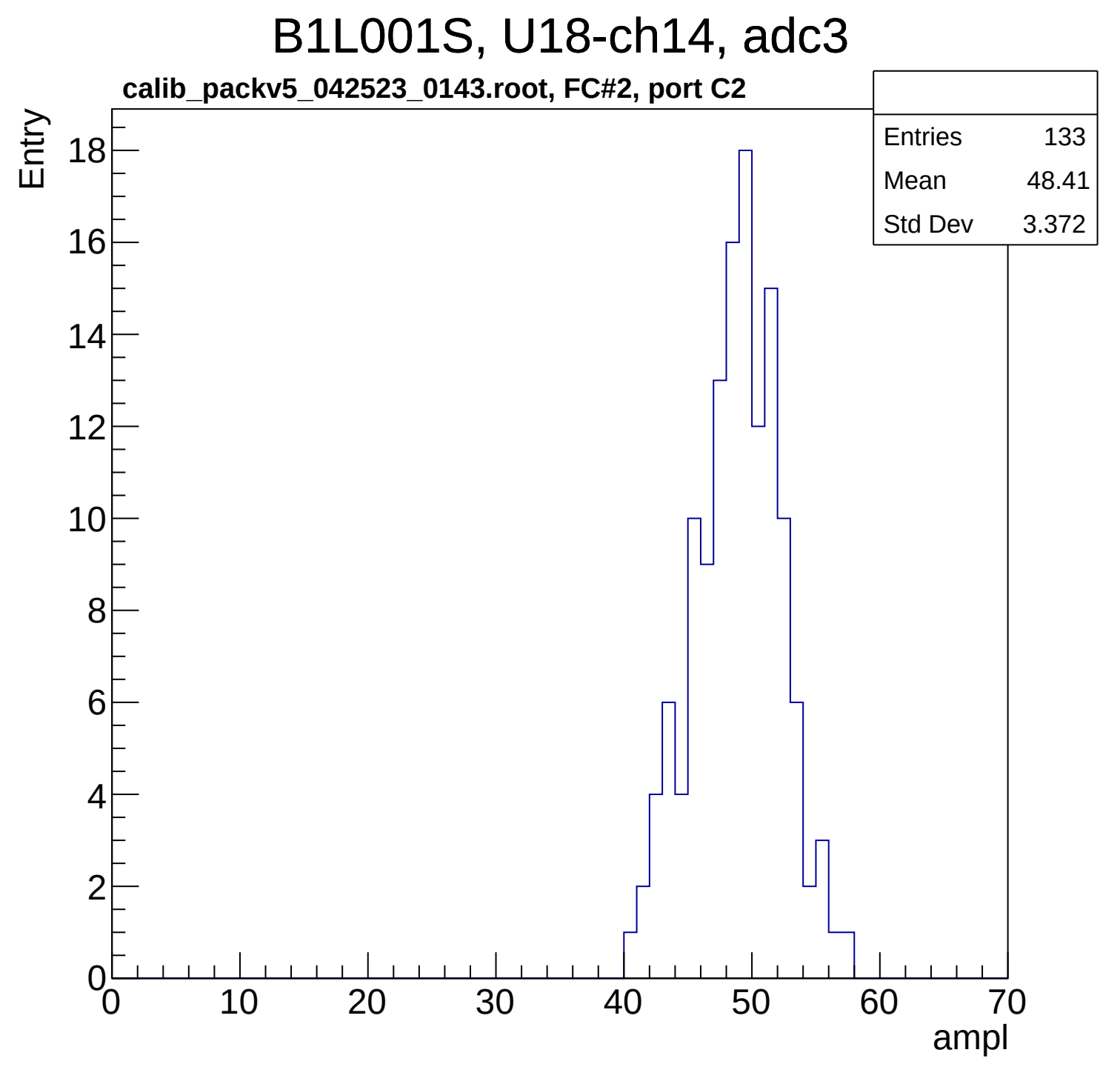

B1L001S, U18-ch13, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 6
Mean 52
Std Dev 23.26
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

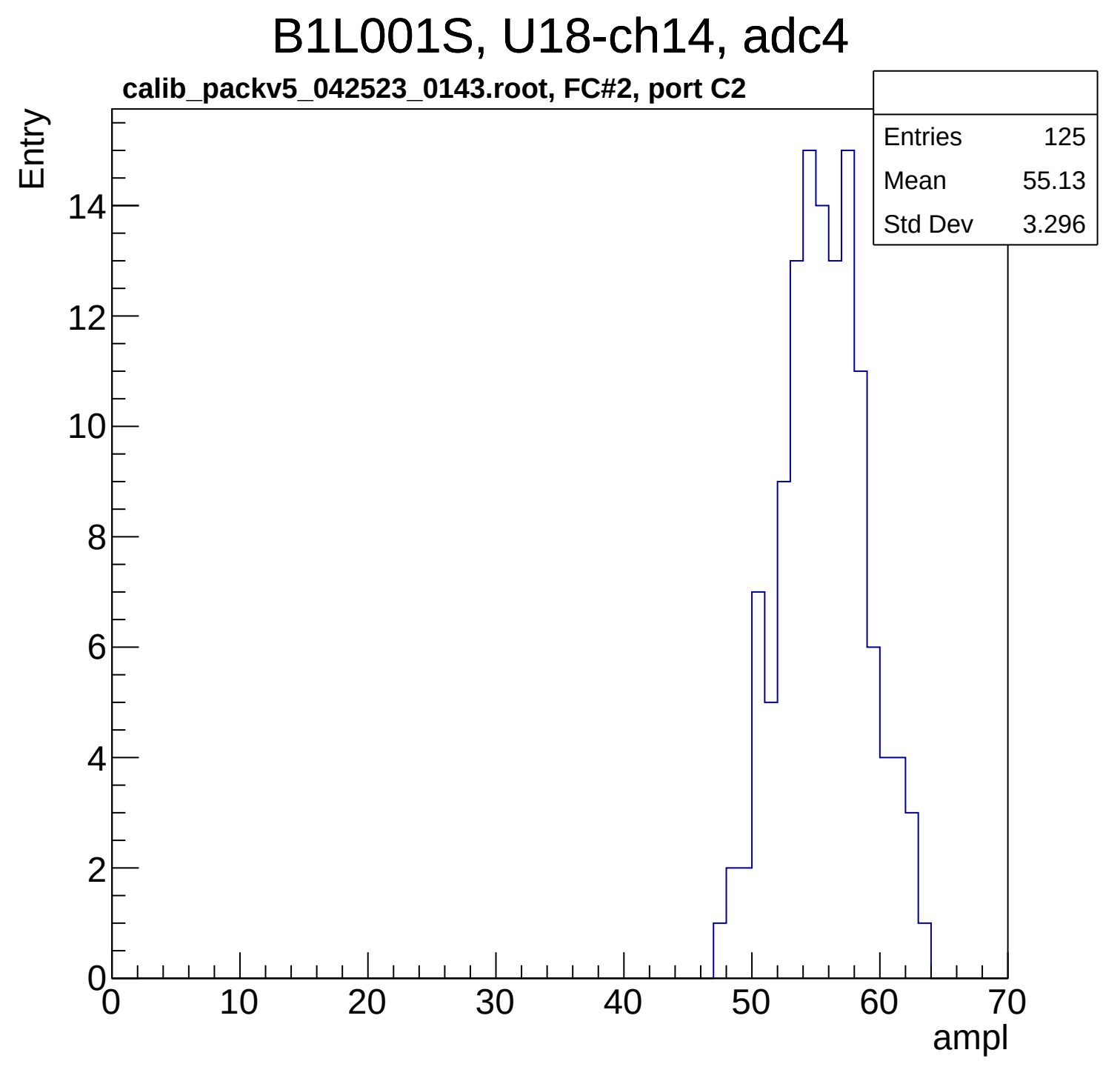

B1L001S, U18-ch13, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

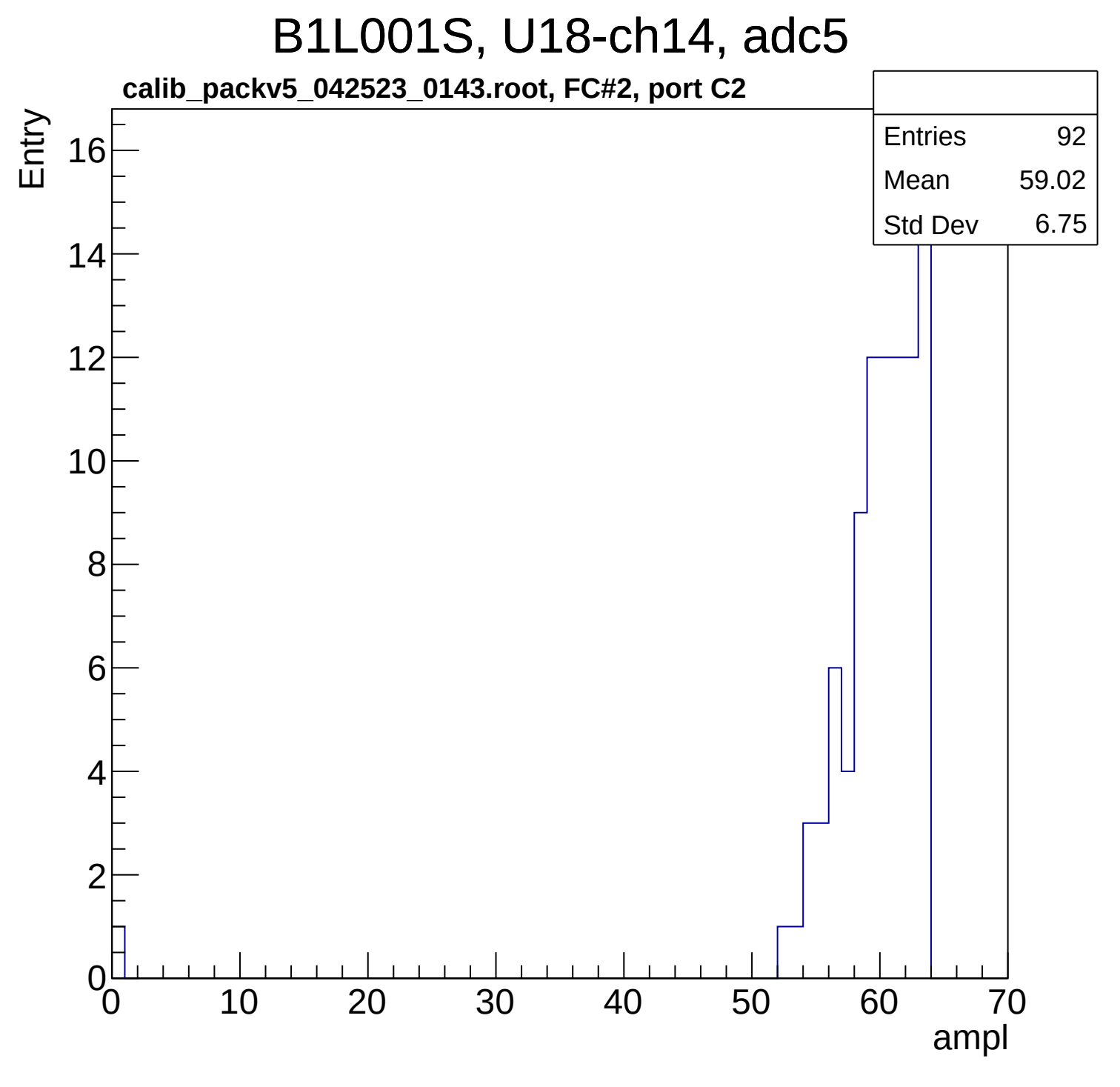

B1L001S, U18-ch14, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 137
Mean 29.28
Std Dev 3.44
Gaus mean : 29.8378
Gaus Width: 3.4801
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

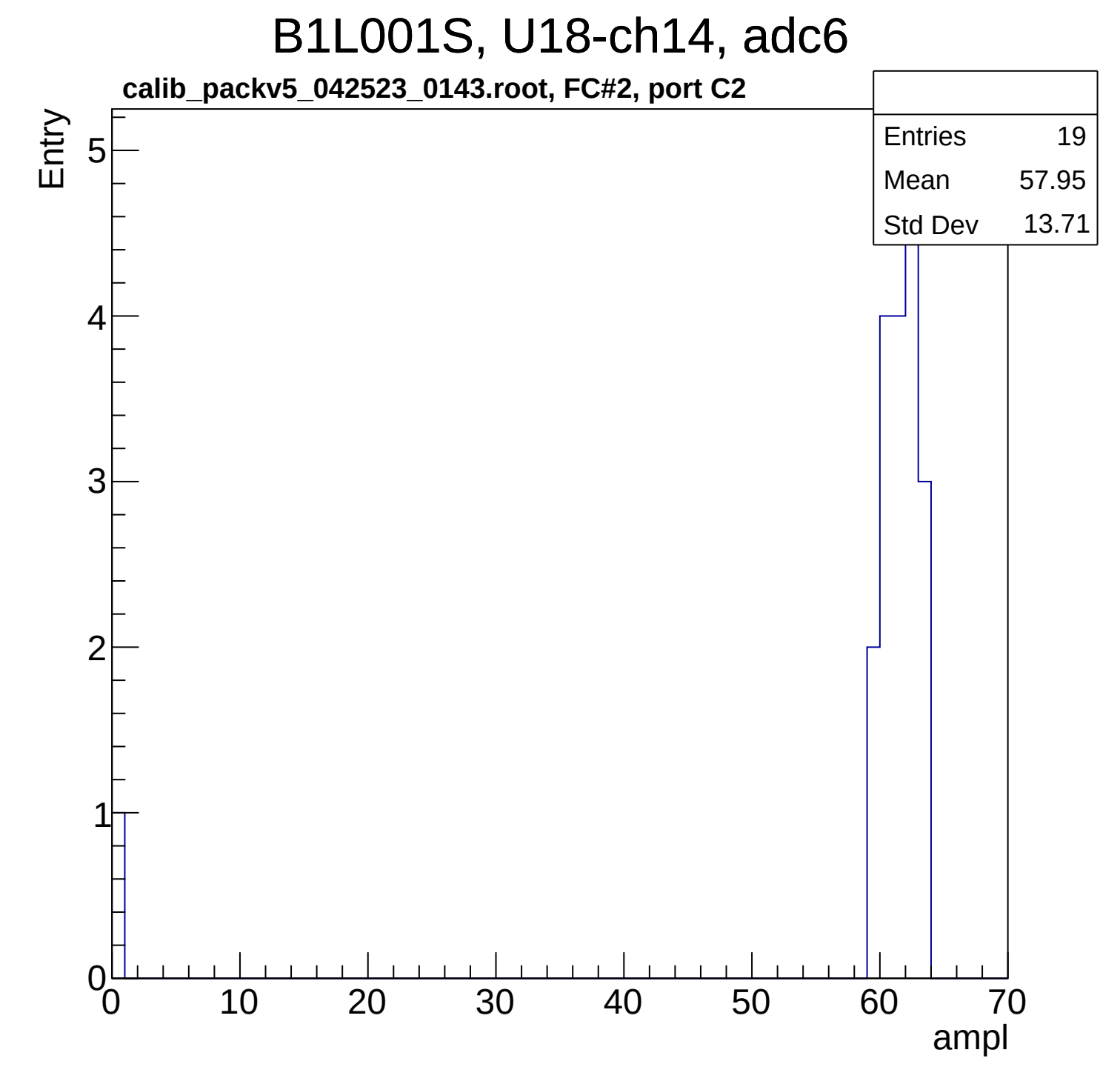

B1L001S, U18-ch14, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 136
Mean 36.09
Std Dev 3.495
Gaus mean : 36.5383
Gaus Width: 3.5002
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

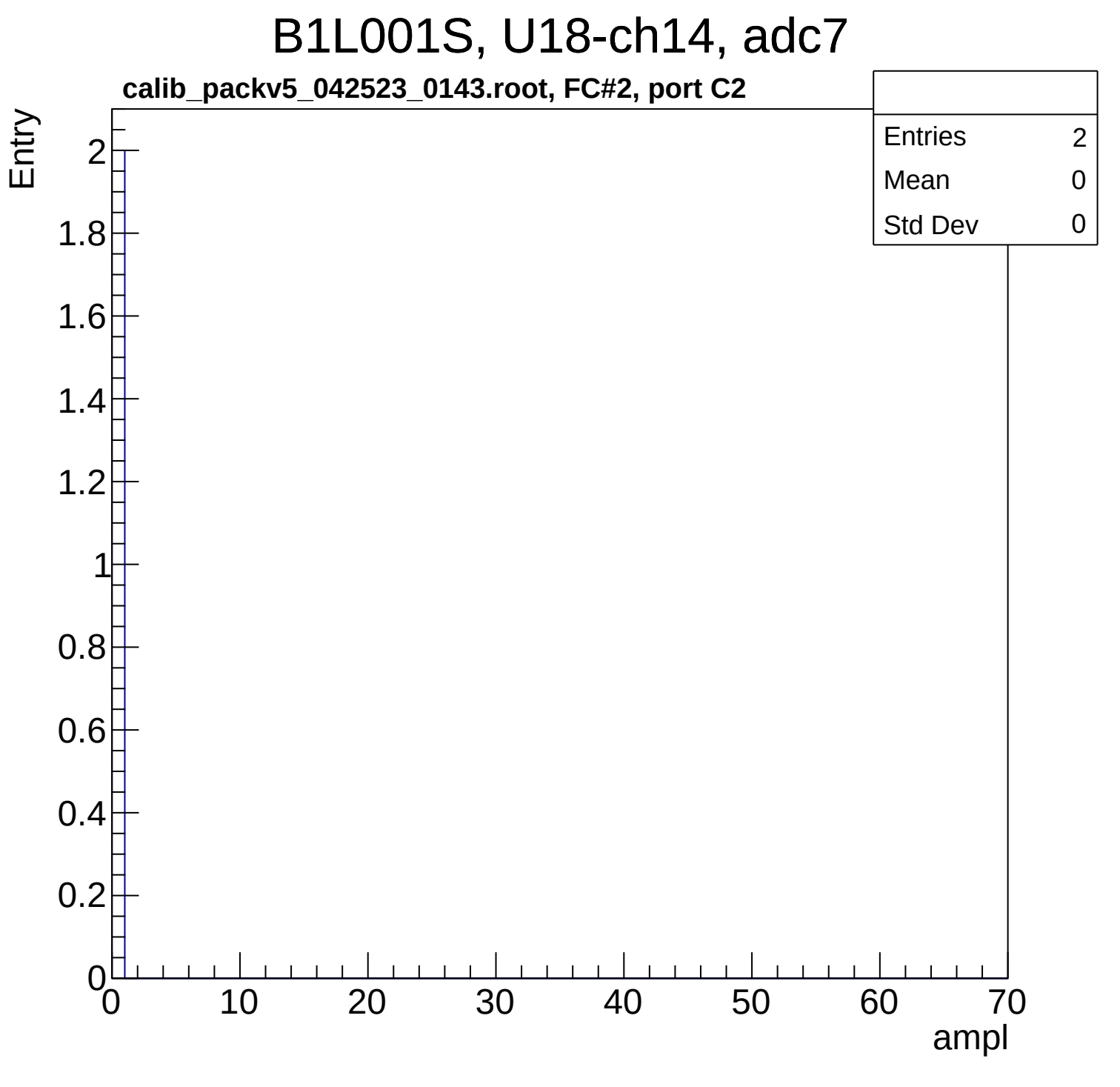

B1L001S, U18-ch14, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 114
Mean 42.24
Std Dev 3.144
Gaus mean : 42.8990
Gaus Width: 3.2447
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

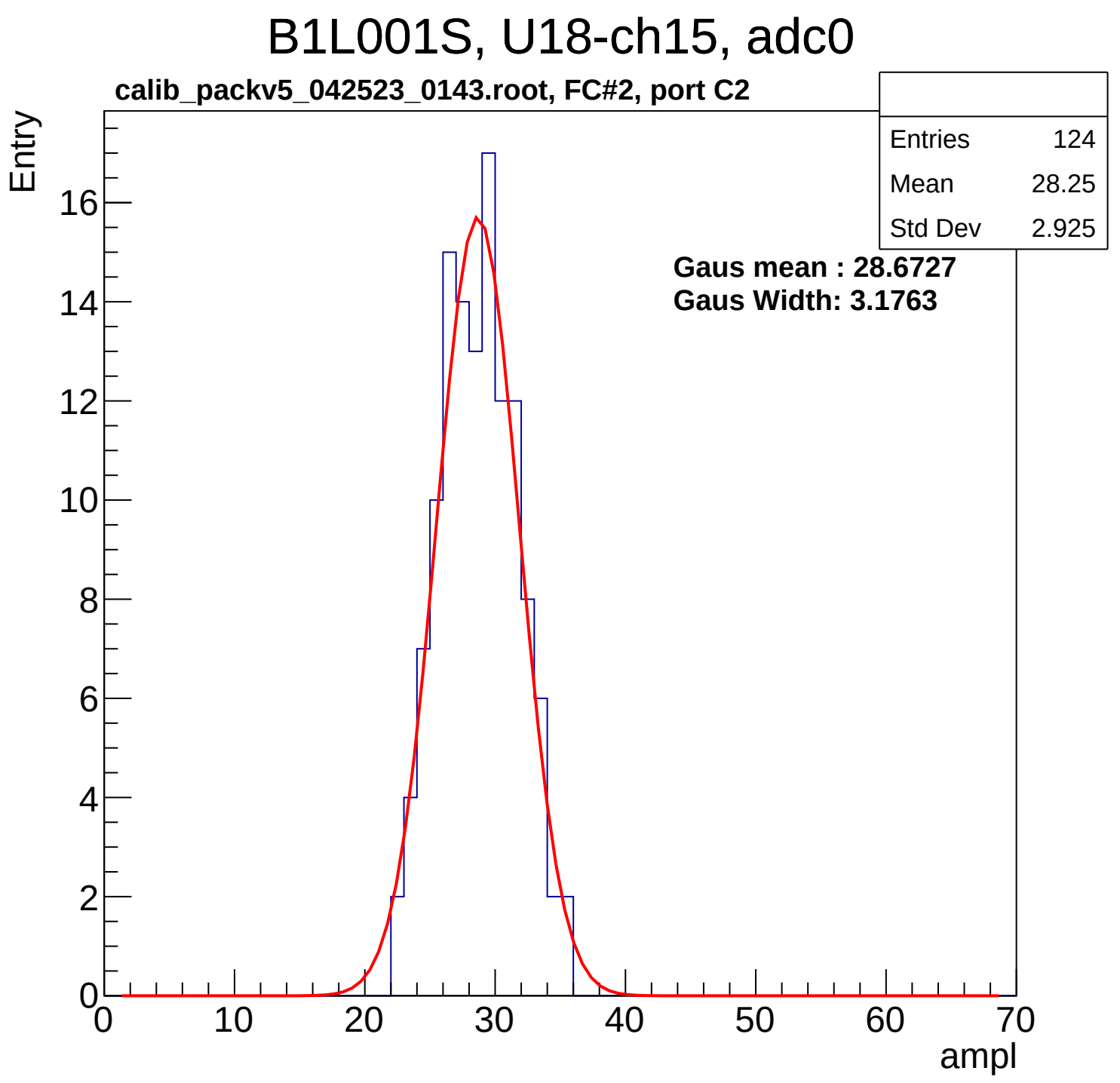

B1L001S, U18-ch14, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 133
Mean 48.41
Std Dev 3.372
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

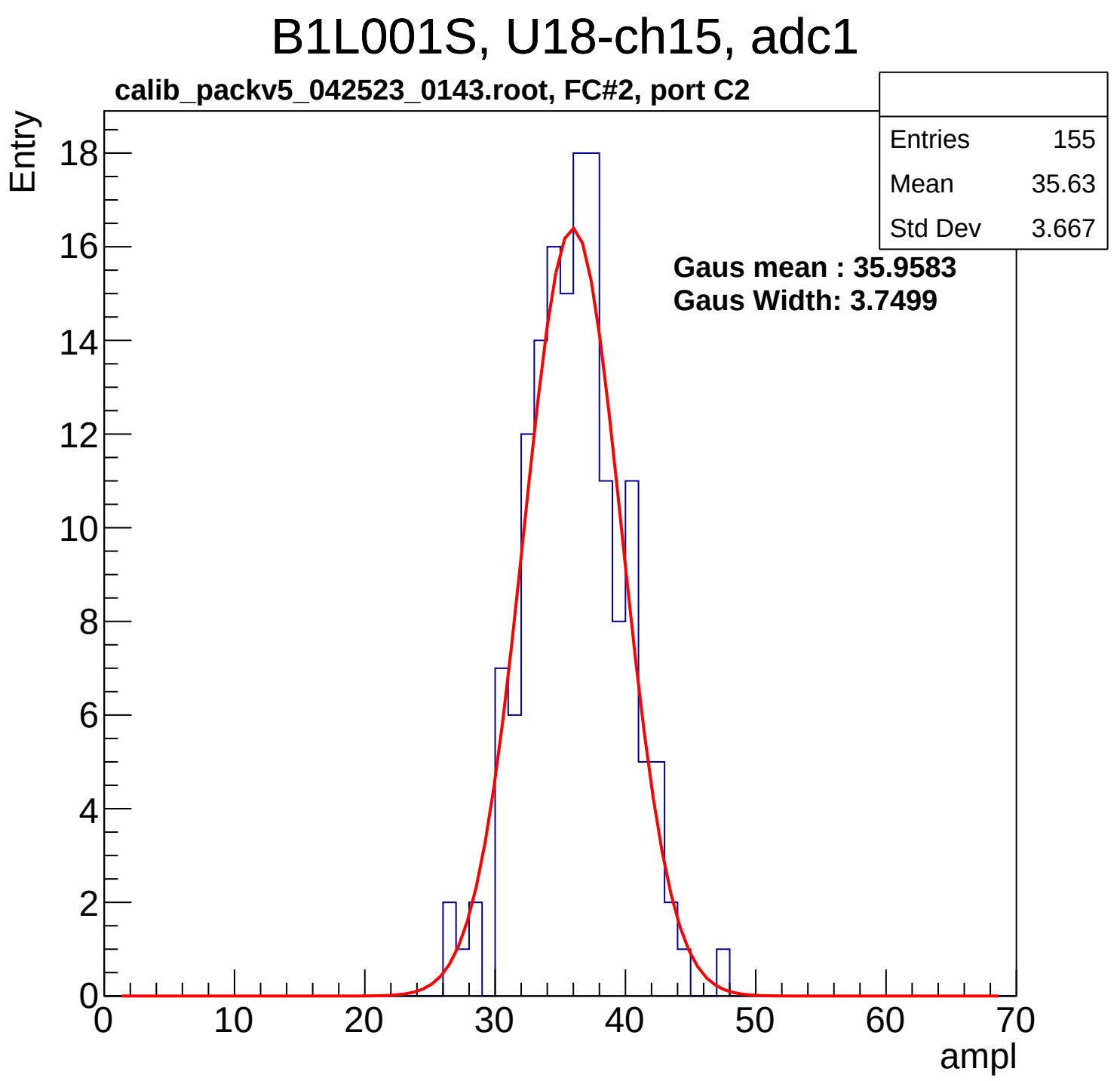

B1L001S, U18-ch14, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 125
Mean 55.13
Std Dev 3.296
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl

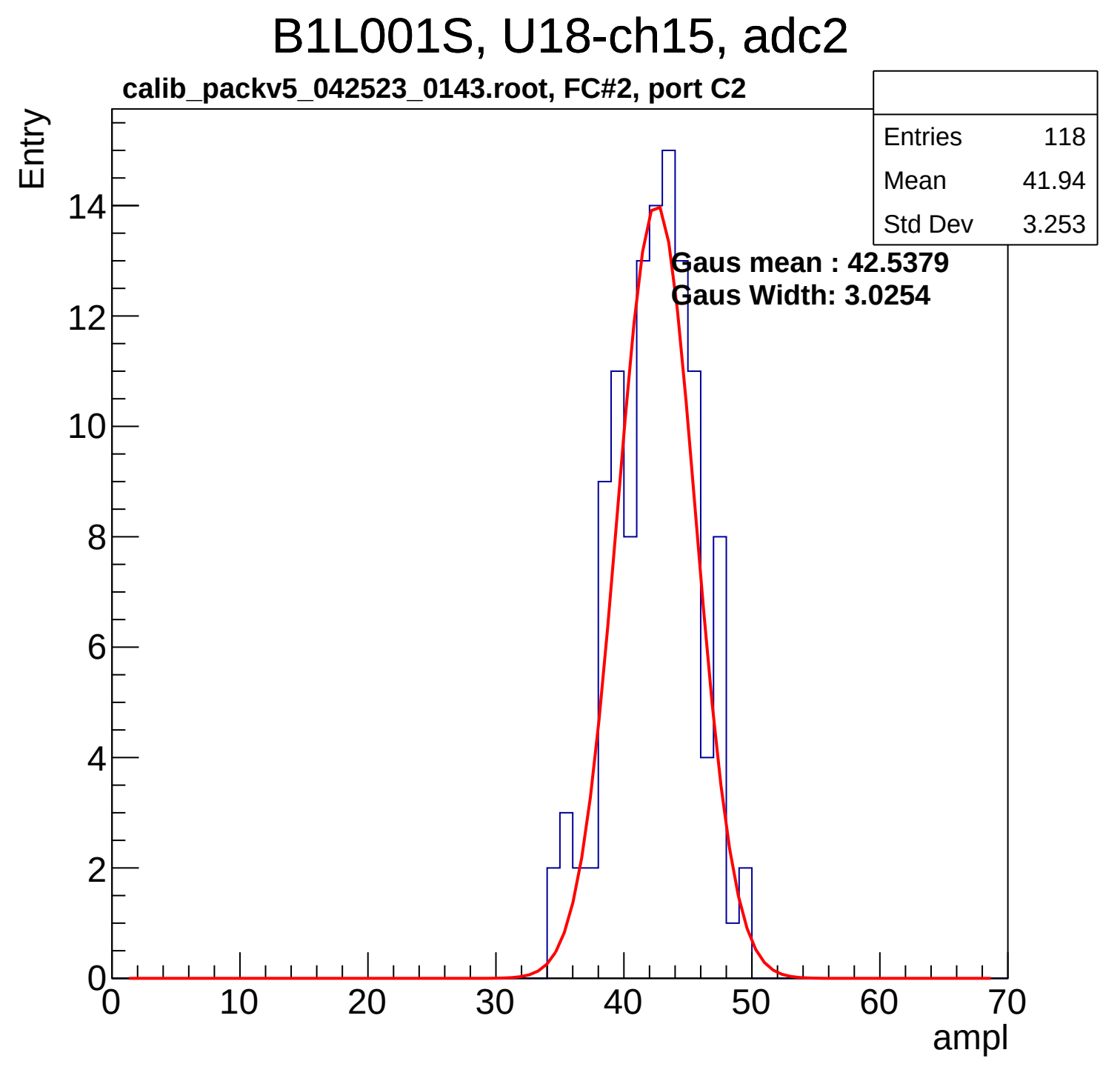

B1L001S, U18-ch14, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 92
Mean 59.02
Std Dev 6.75
Entry
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl

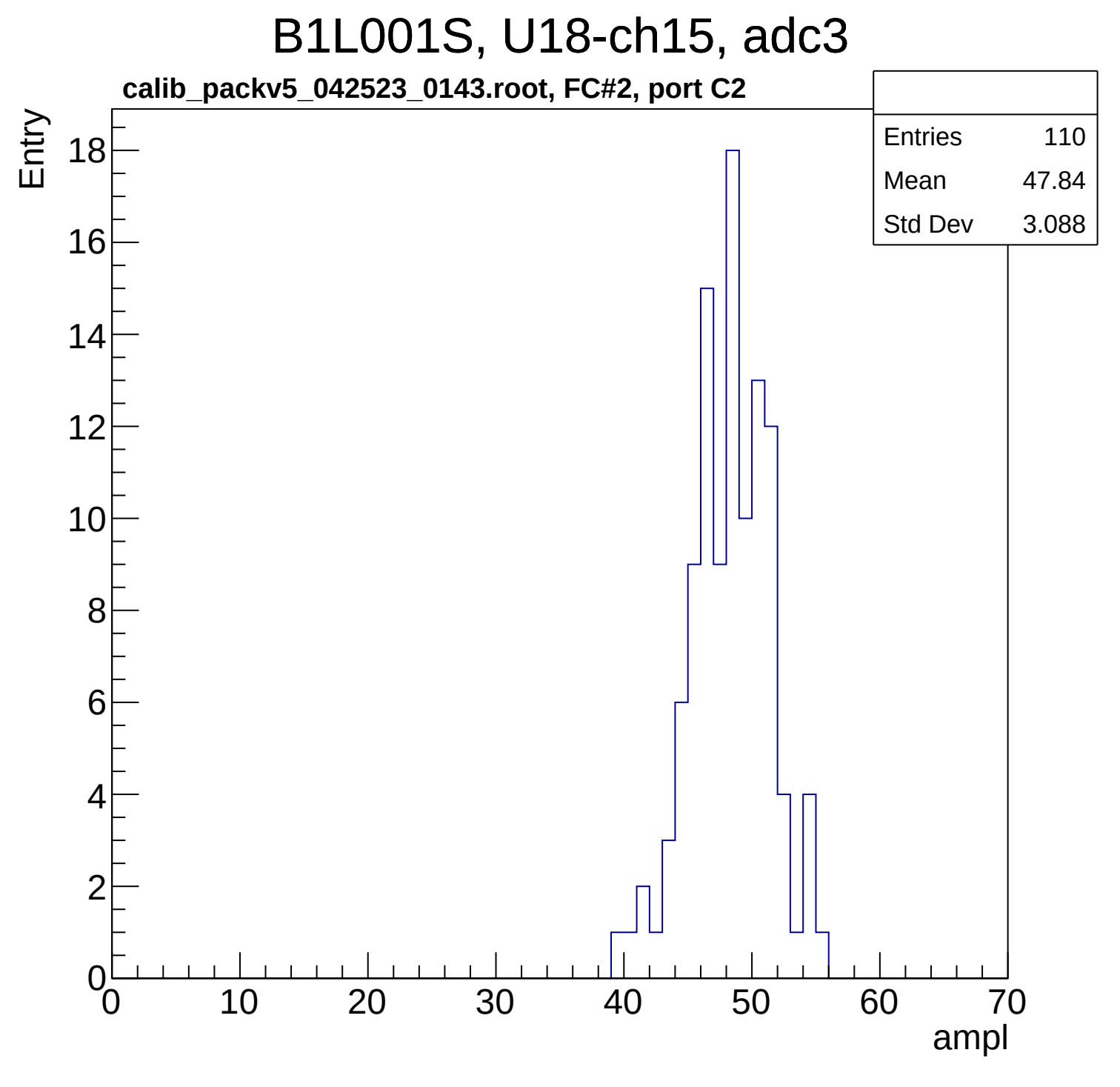

B1L001S, U18-ch14, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 19
Mean 57.95
Std Dev 13.71
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

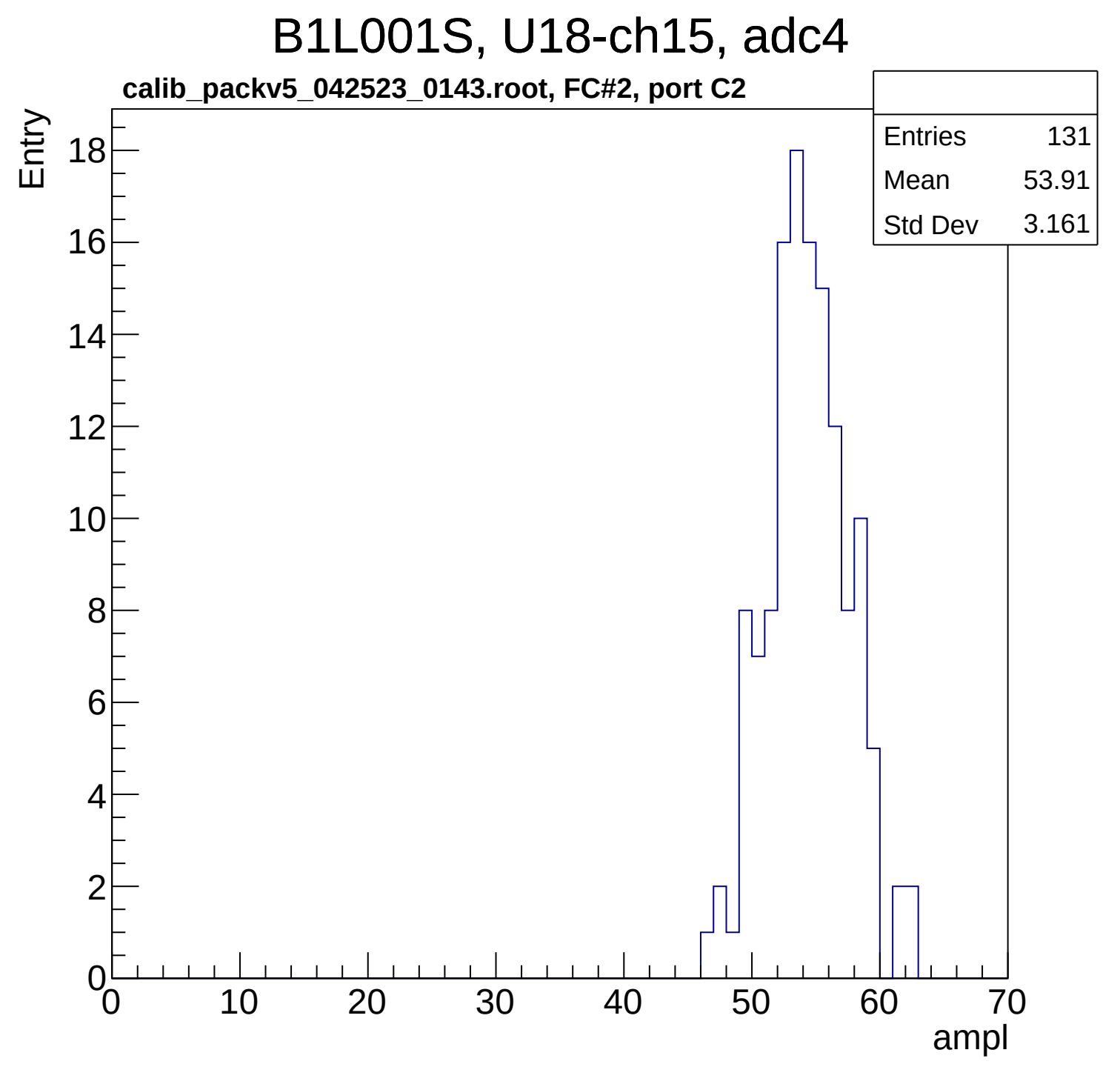

B1L001S, U18-ch14, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 0
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

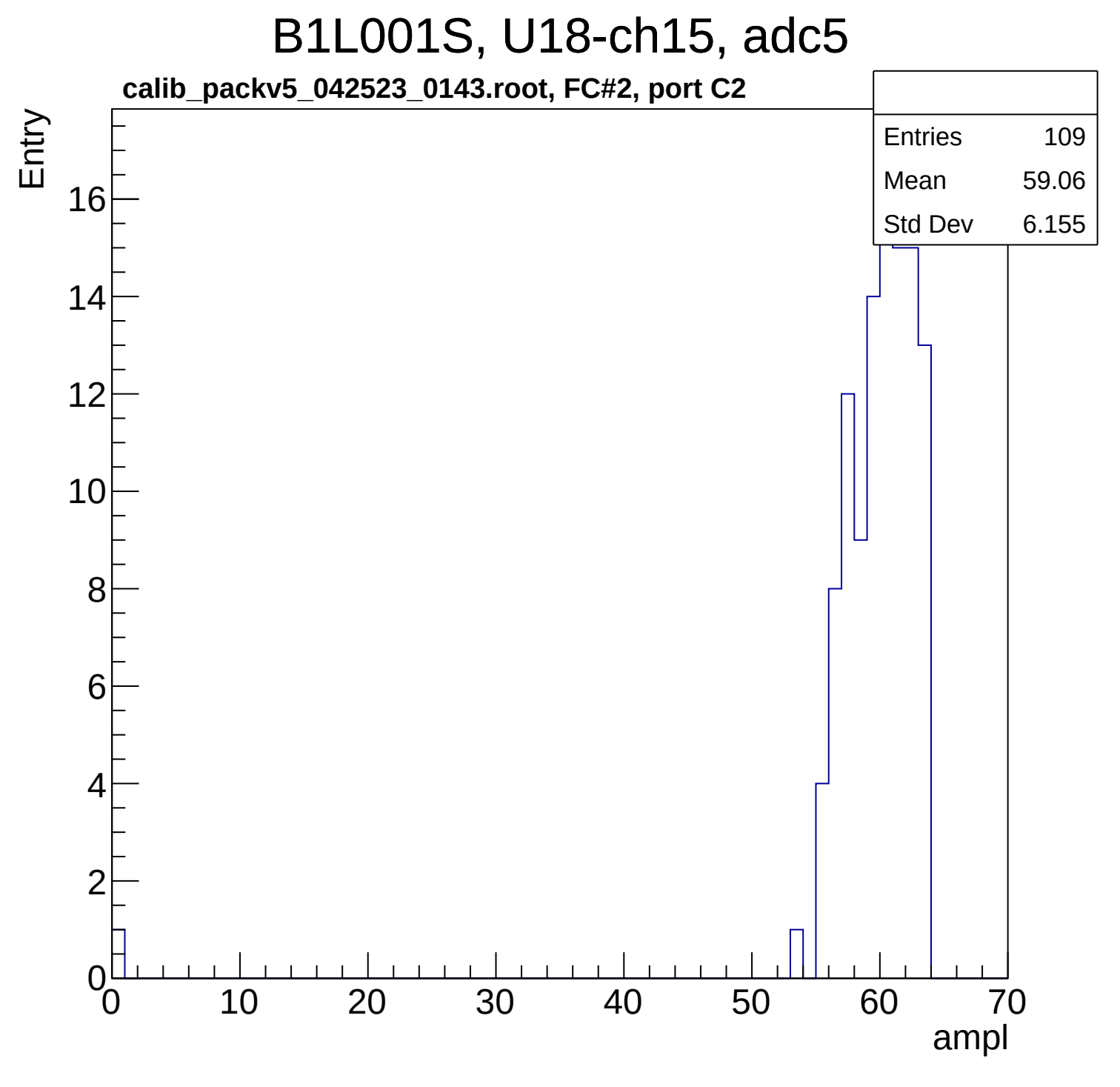

B1L001S, U18-ch15, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 124
Mean 28.25
Std Dev 2.925
Gaus mean : 28.6727
Gaus Width: 3.1763
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

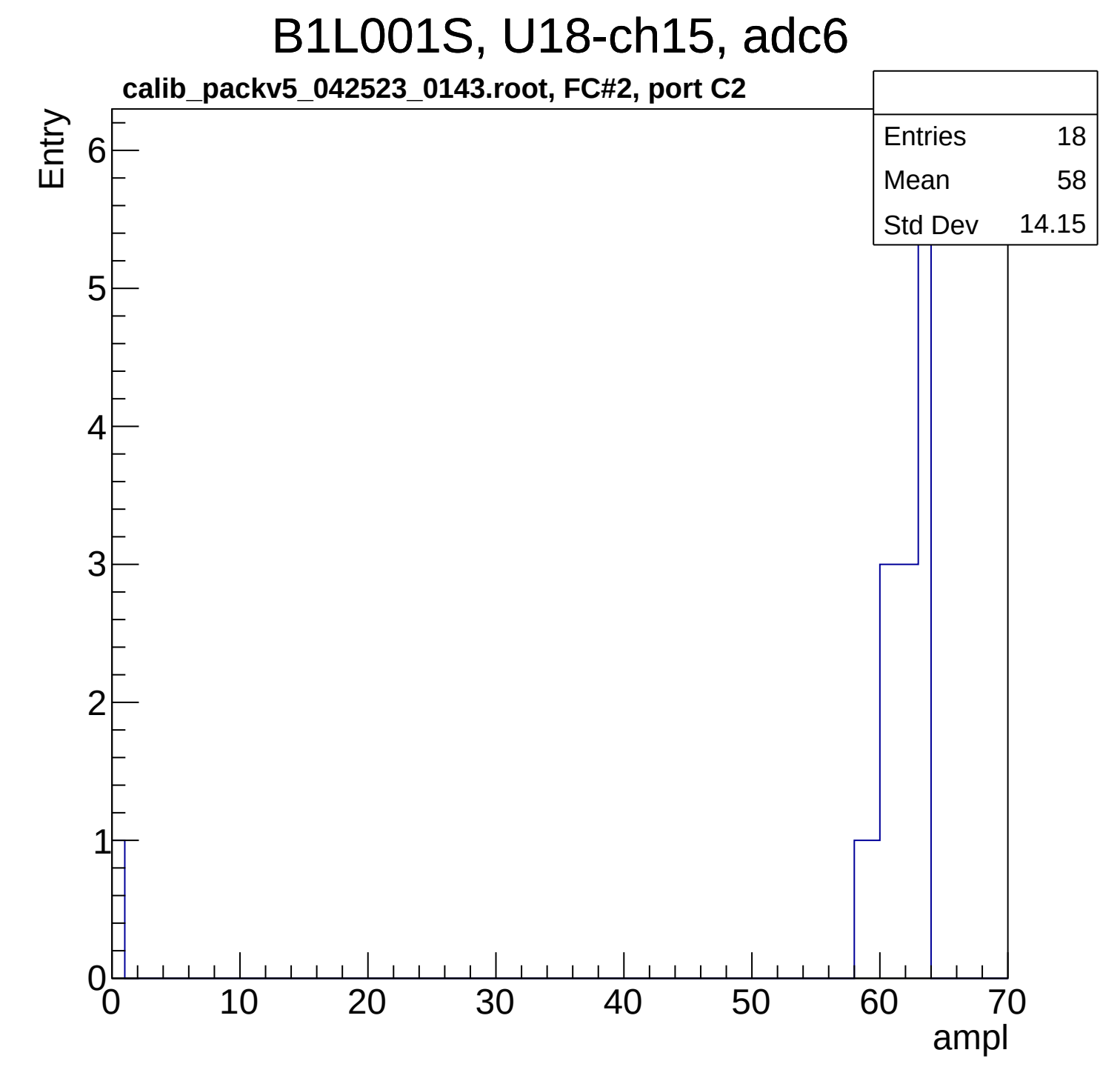

B1L001S, U18-ch15, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 155
Mean 35.63
Std Dev 3.667
Gaus mean : 35.9583
Gaus Width: 3.7499
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

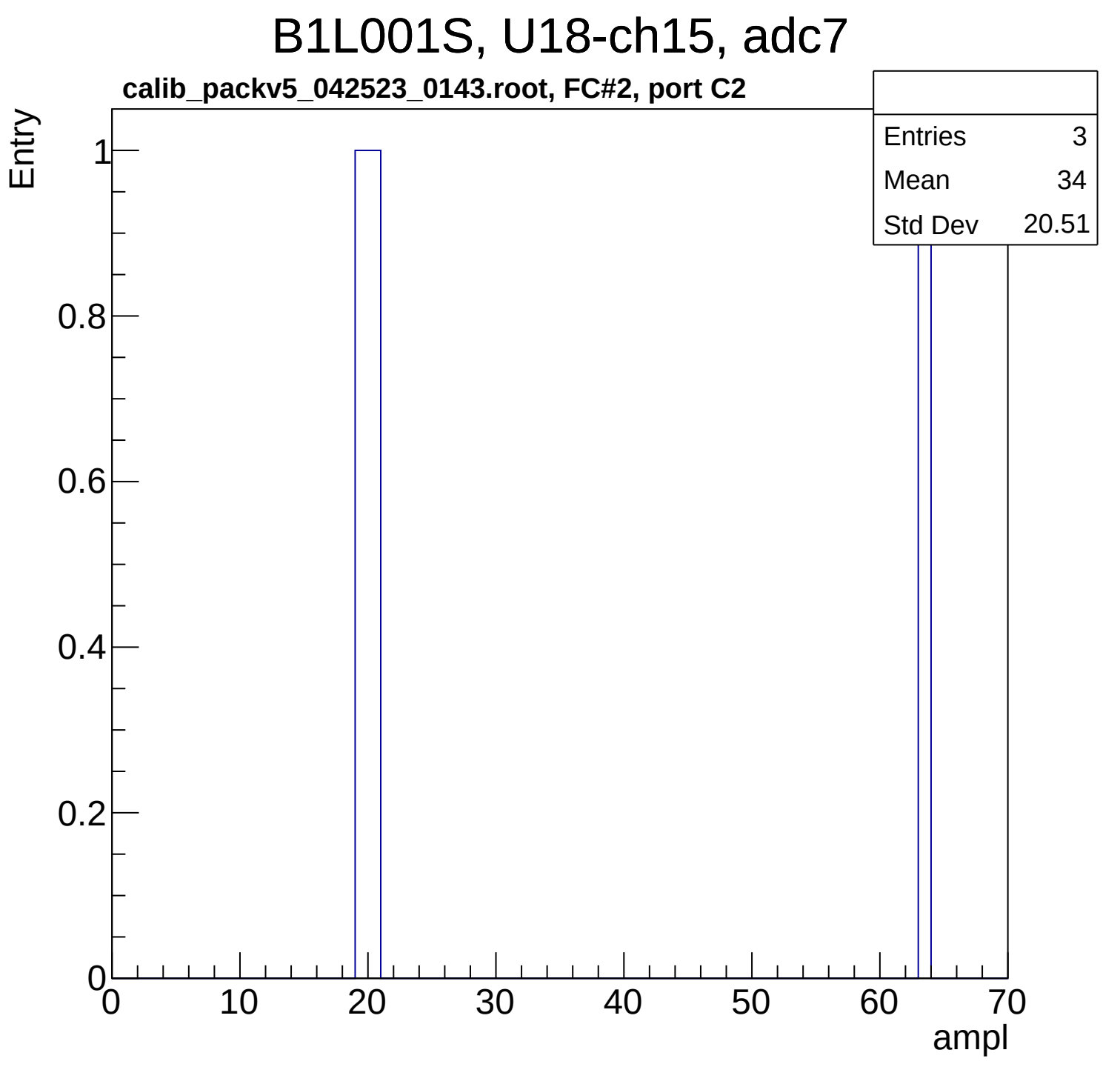

B1L001S, U18-ch15, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 118
Mean 41.94
Std Dev 3.253
Gaus mean : 42.5379
Gaus Width: 3.0254
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

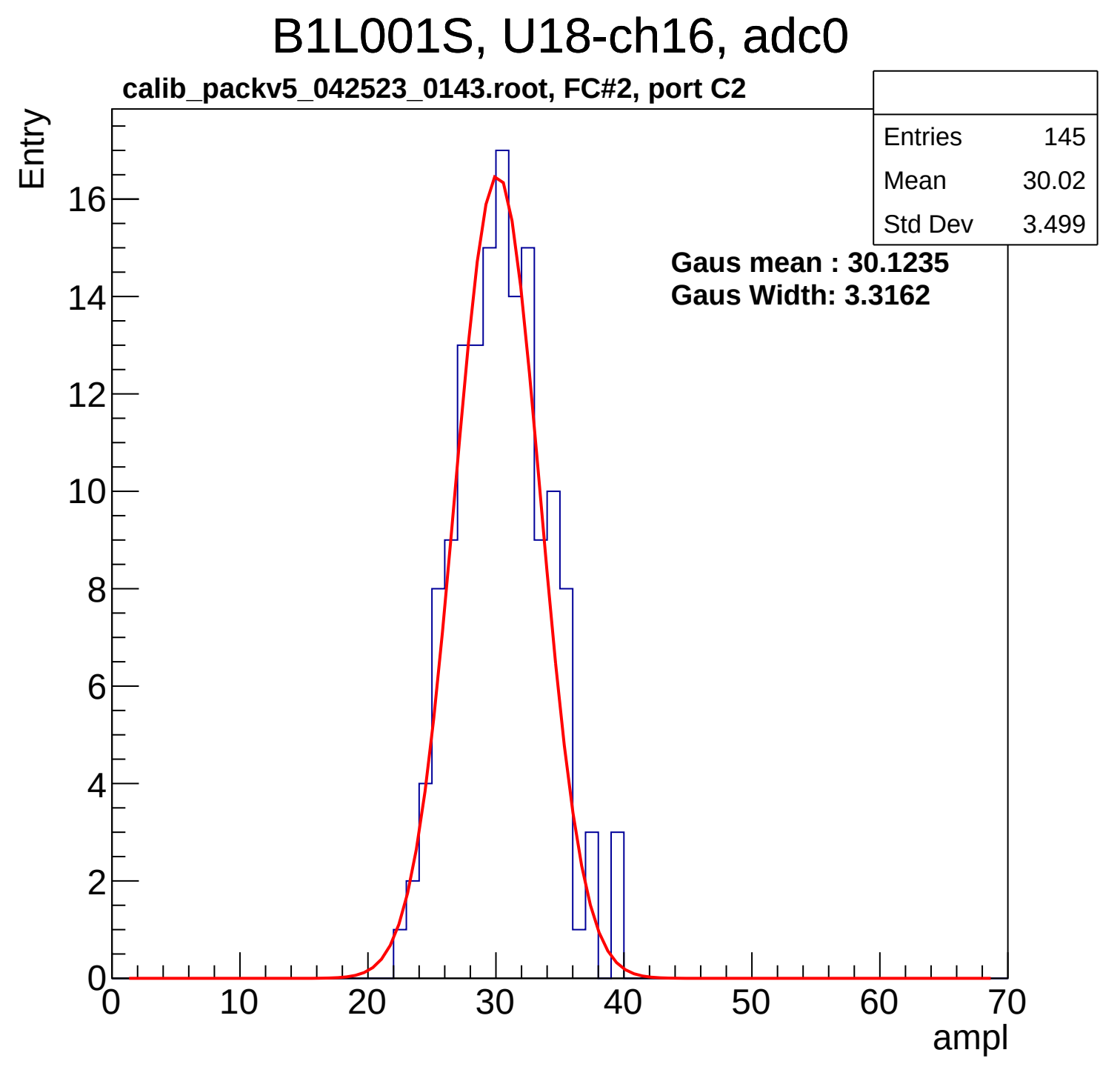

B1L001S, U18-ch15, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 110
Mean 47.84
Std Dev 3.088
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

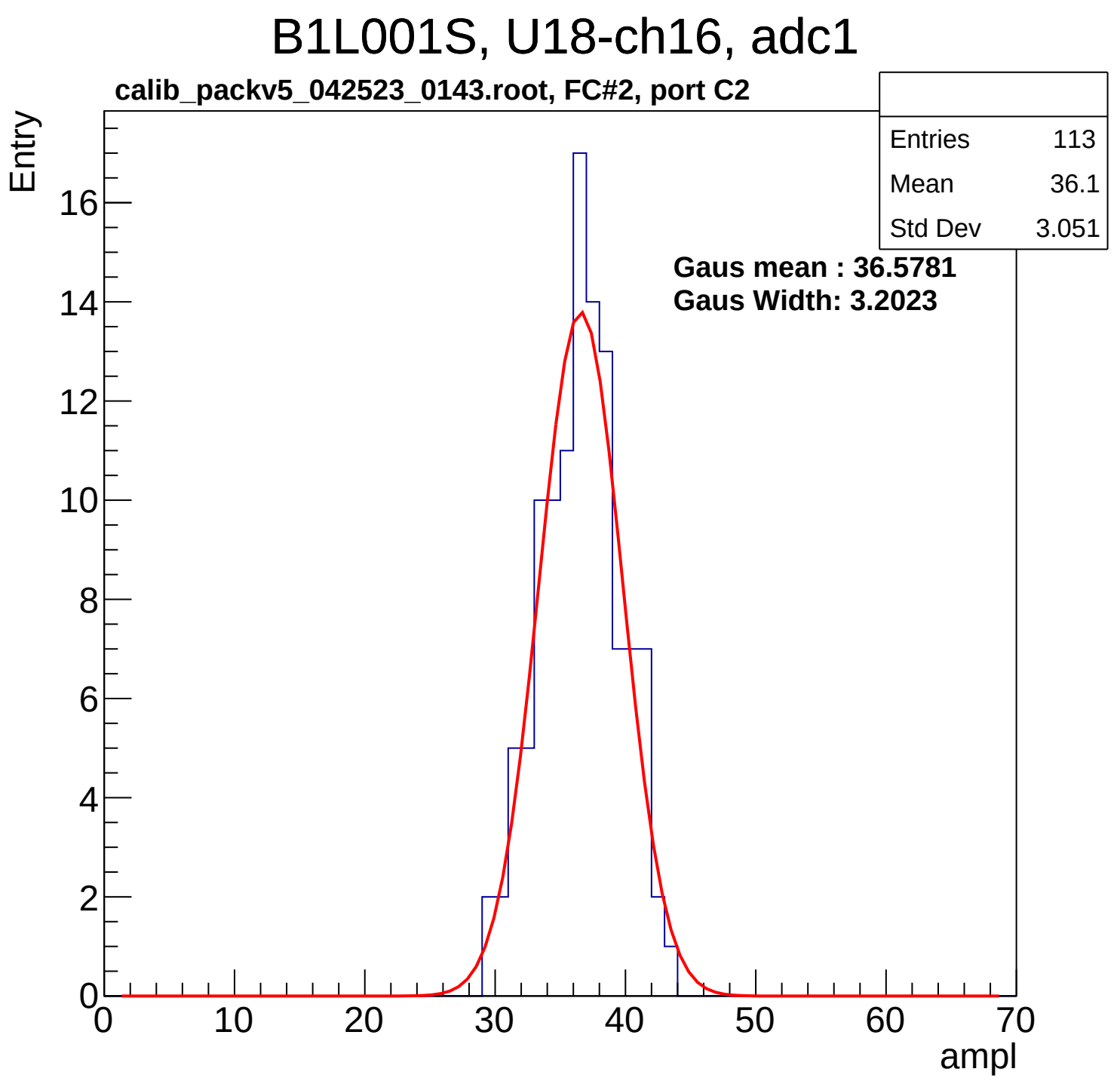

B1L001S, U18-ch15, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 131
Mean 53.91
Std Dev 3.161
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

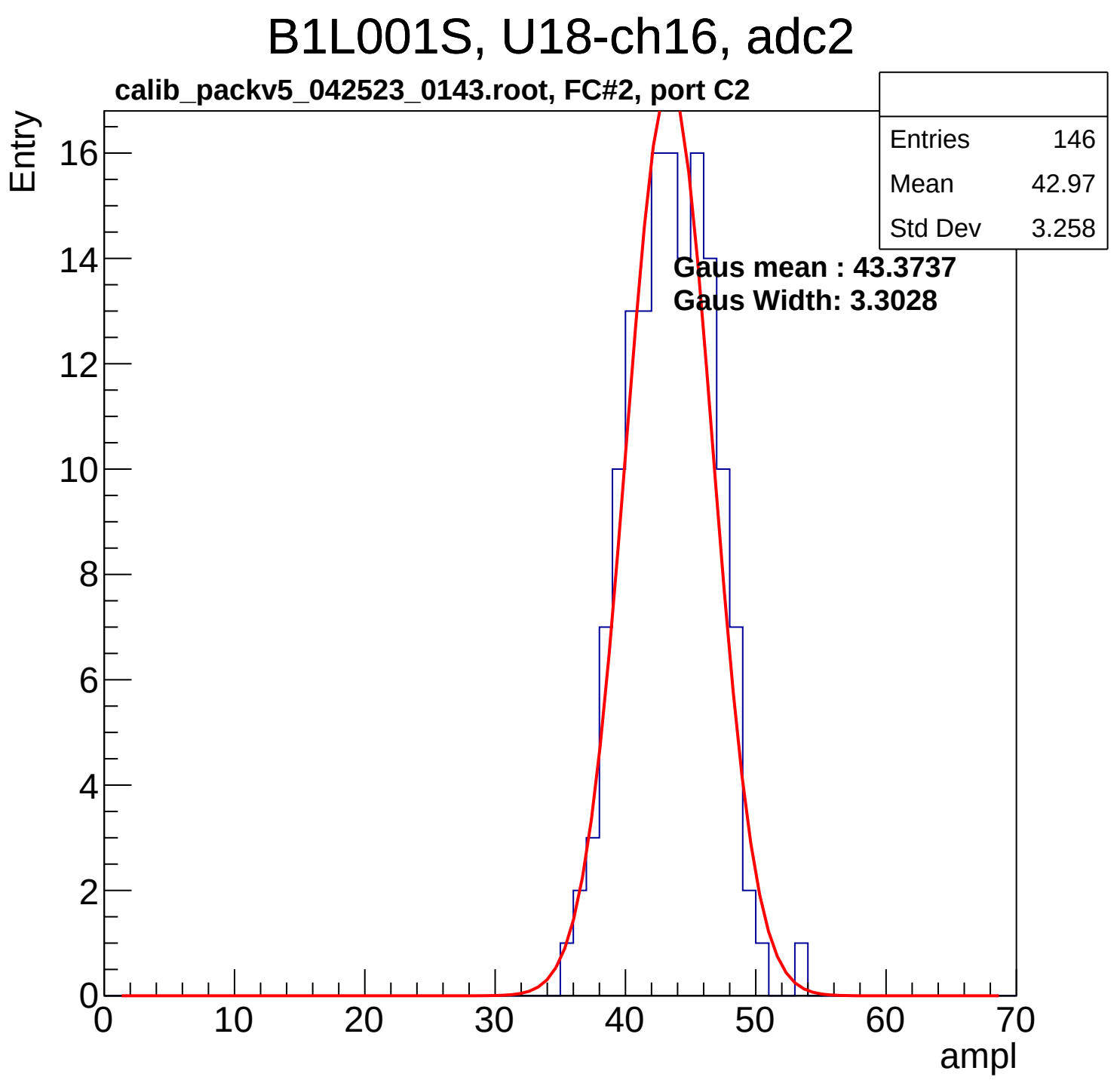

B1L001S, U18-ch15, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 109
Mean 59.06
Std Dev 6.155
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

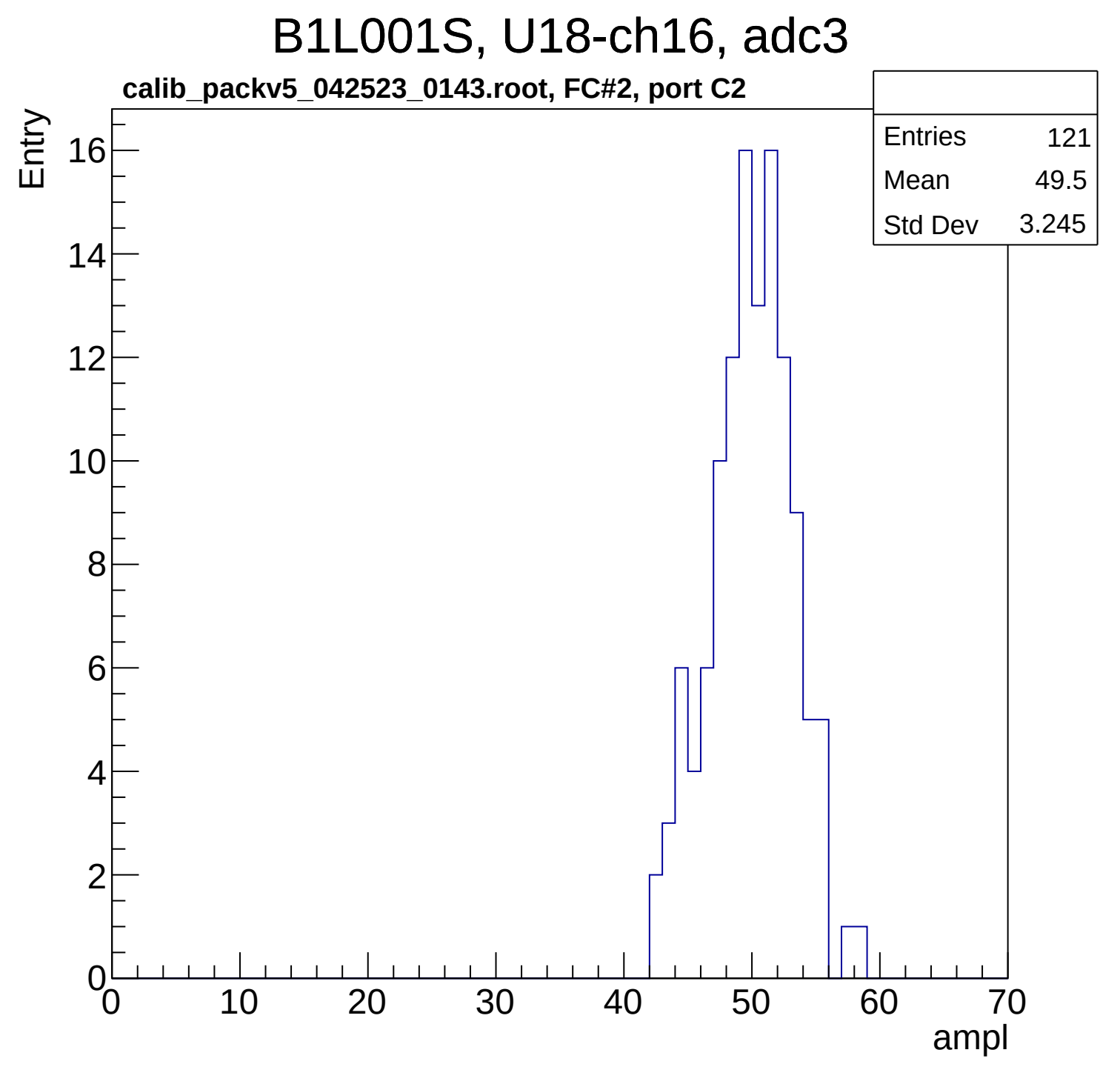

B1L001S, U18-ch15, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 18
Mean 58
Std Dev 14.15
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl

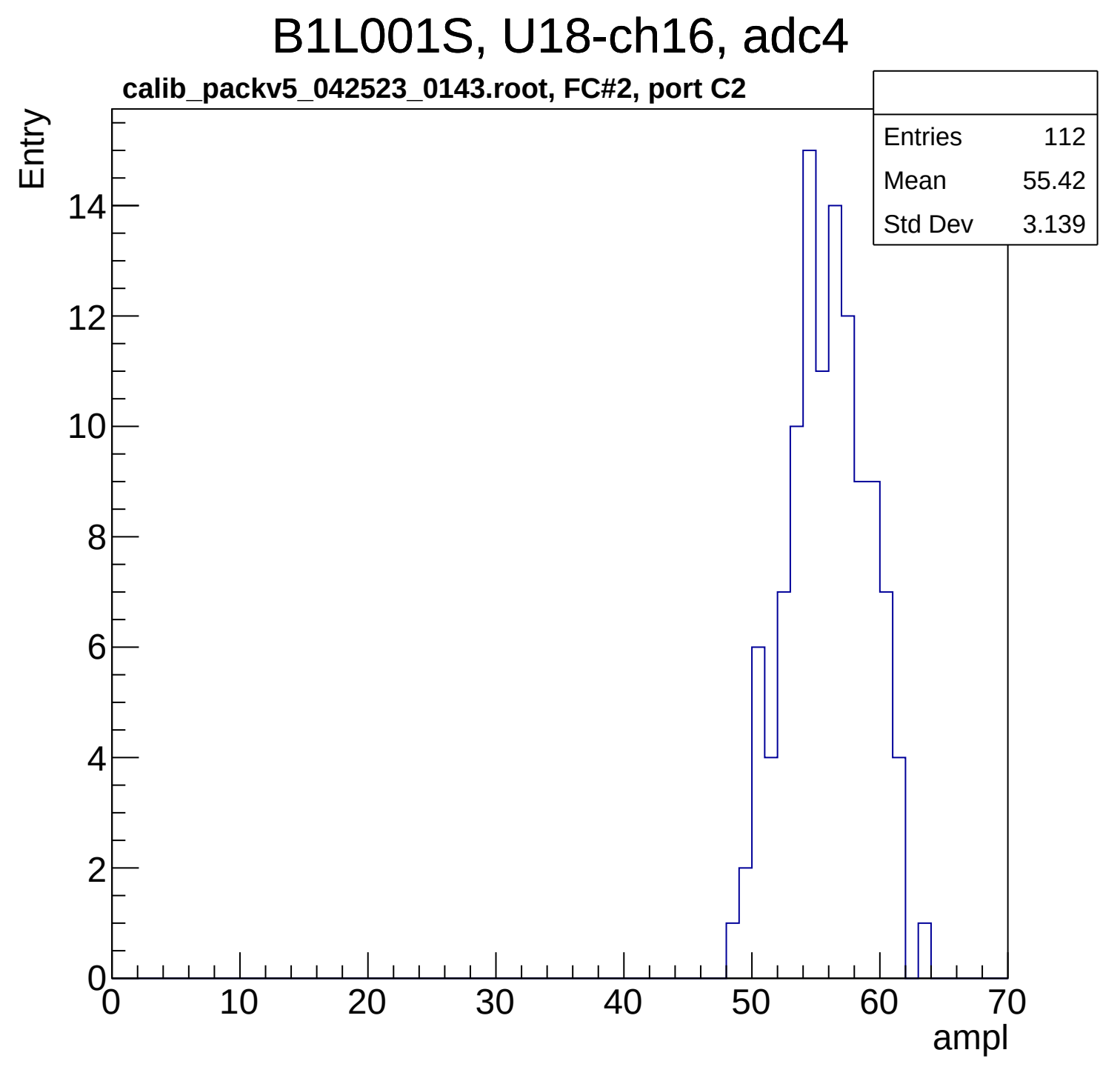

B1L001S, U18-ch15, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 3
Mean 34
Std Dev 20.51
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70

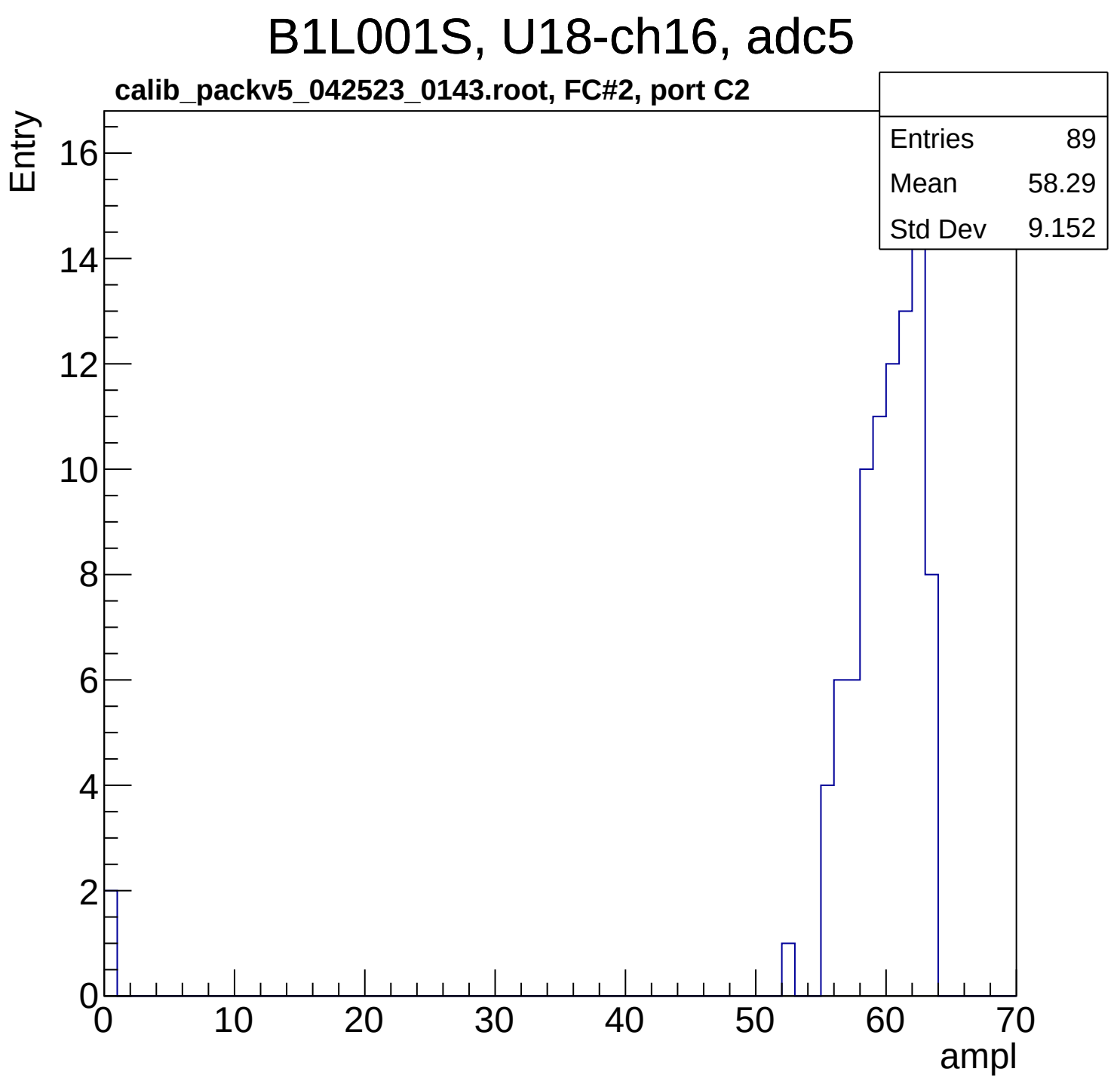

B1L001S, U18-ch16, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 145
Mean 30.02
Std Dev 3.499
Gaus mean : 30.1235
Gaus Width: 3.3162
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

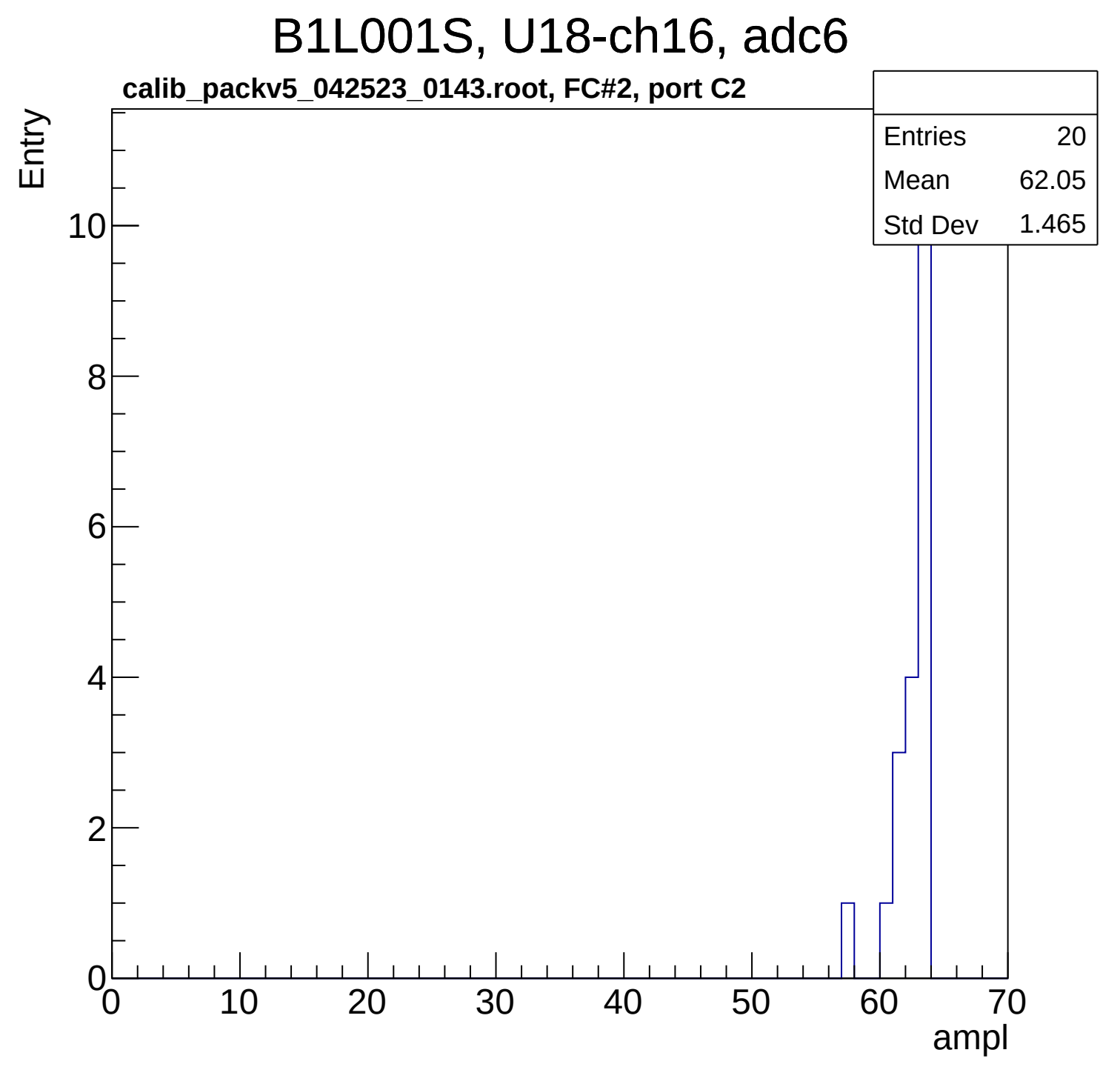

B1L001S, U18-ch16, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 113
Mean 36.1
Std Dev 3.051
Gaus mean : 36.5781
Gaus Width: 3.2023
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

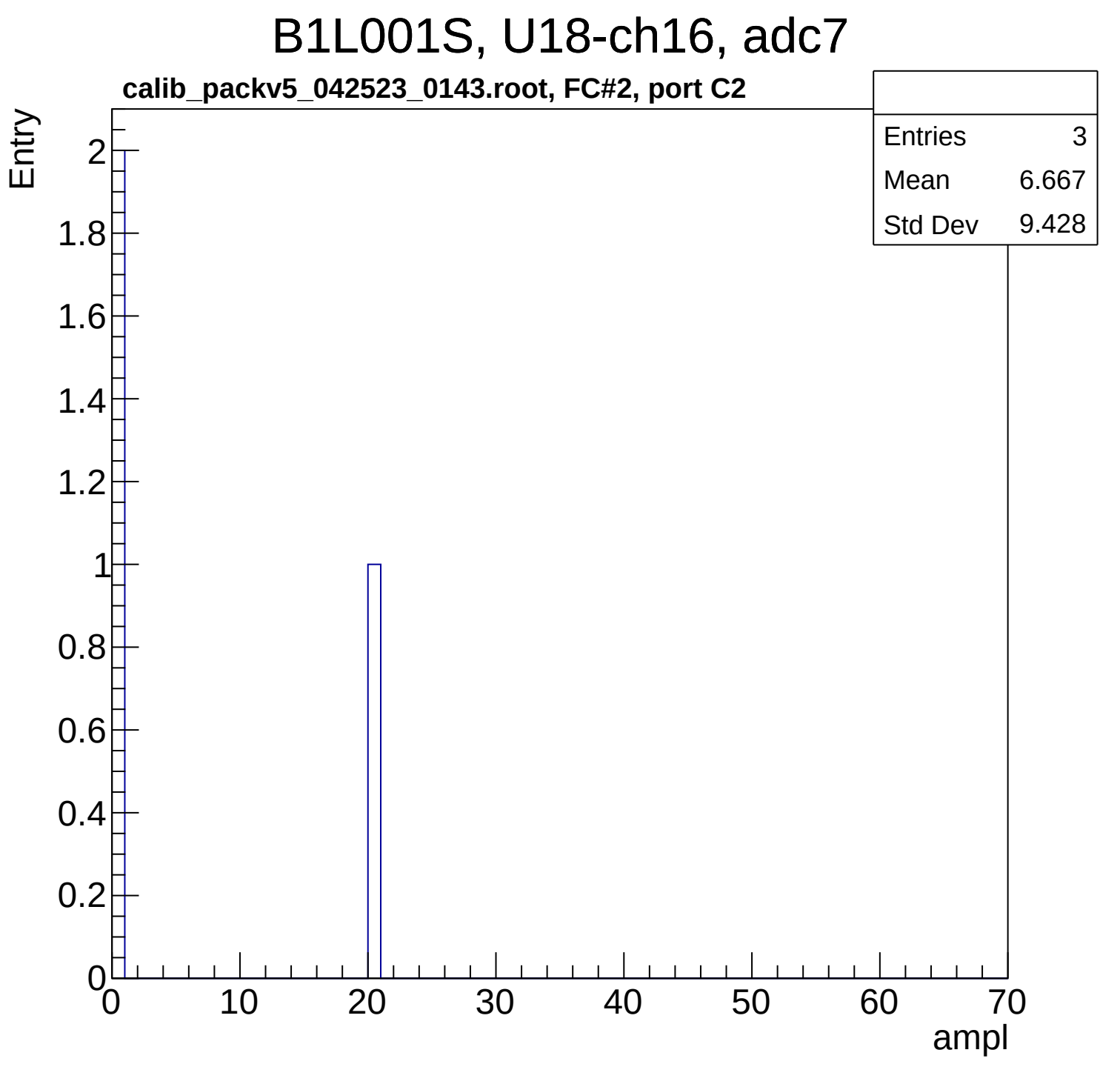

B1L001S, U18-ch16, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 146
Mean 42.97
Std Dev 3.258
Gaus mean : 43.3737
Gaus Width: 3.3028
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

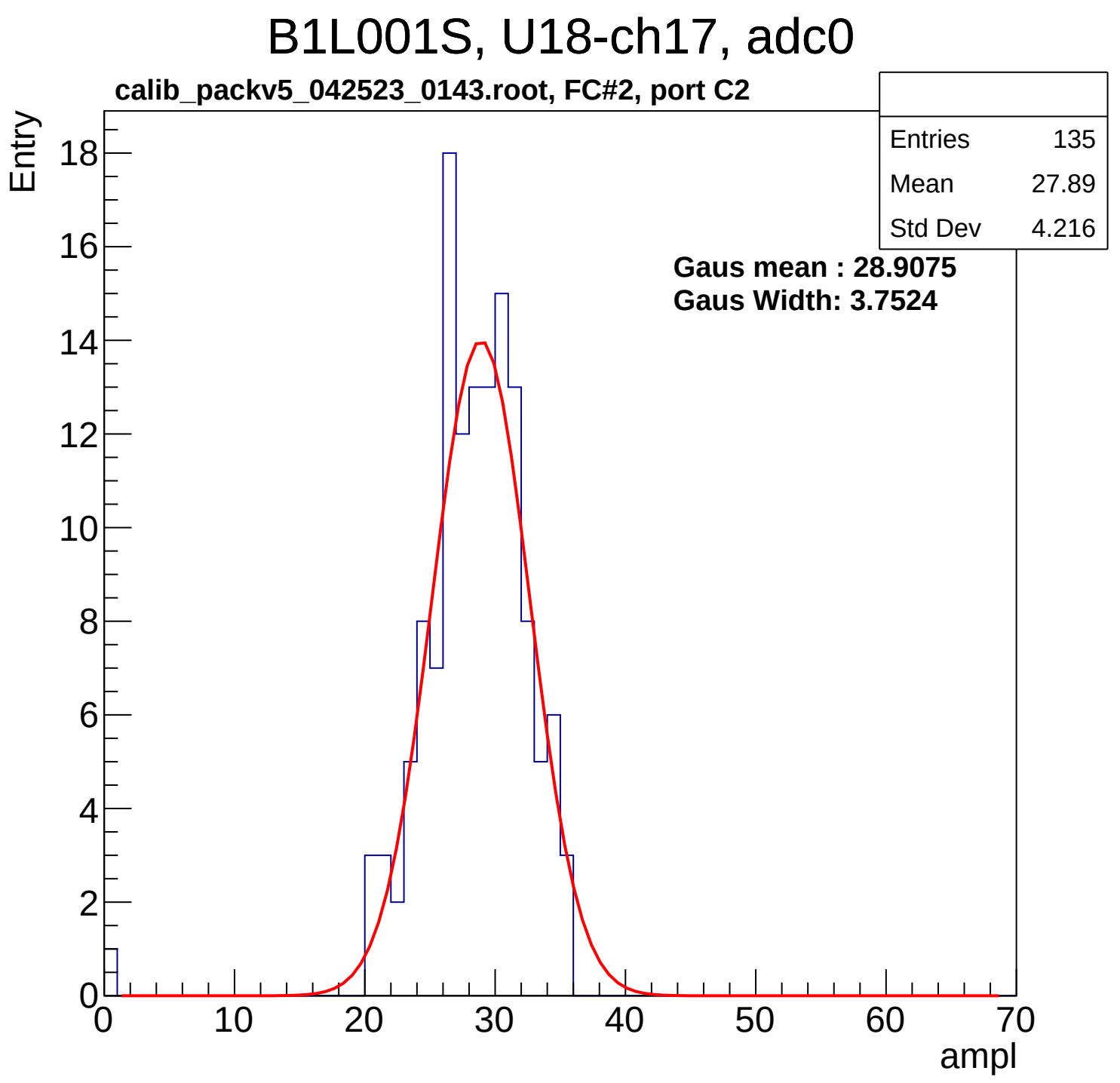

B1L001S, U18-ch16, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 121
Mean 49.5
Std Dev 3.245
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

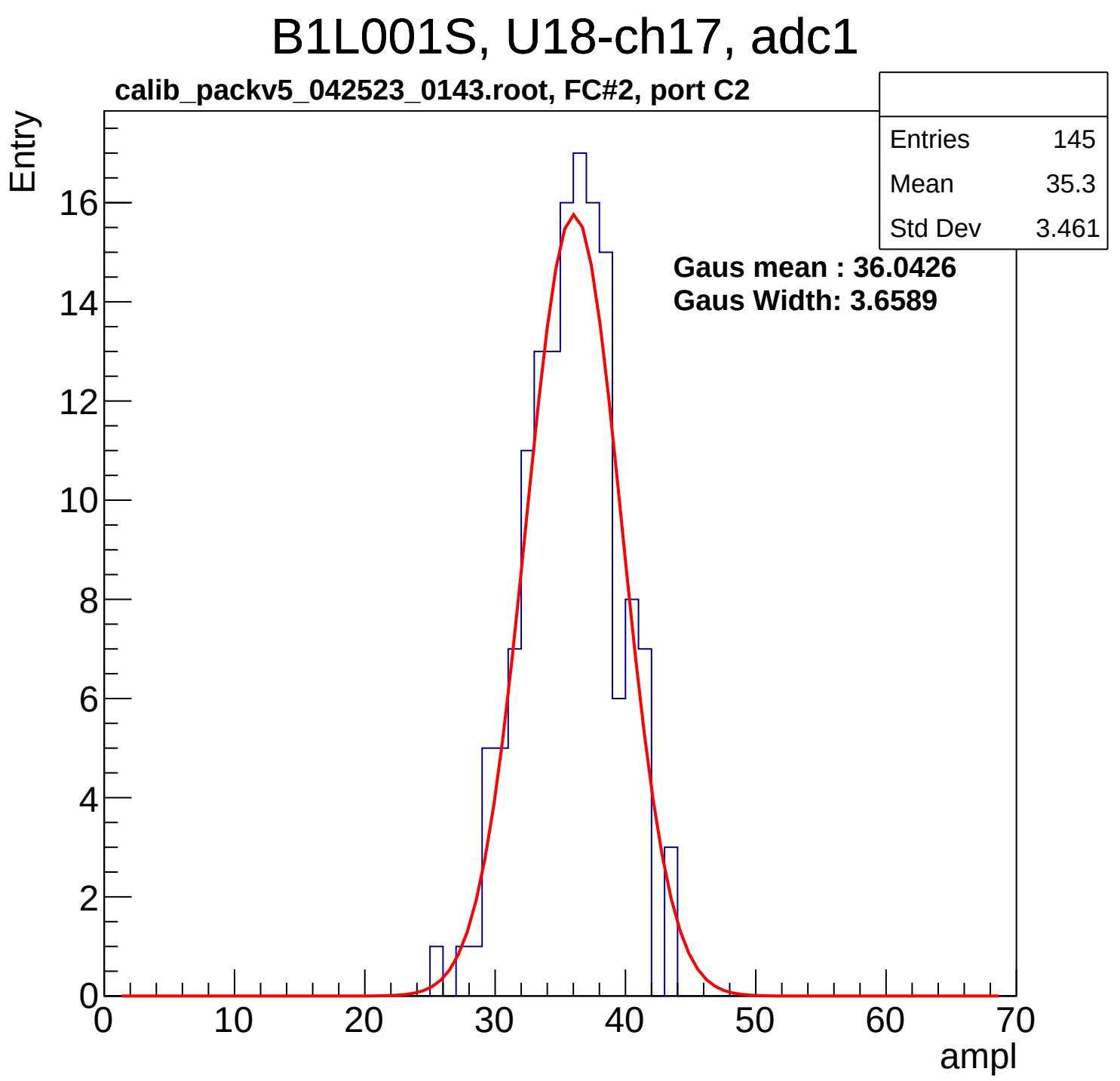

B1L001S, U18-ch16, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 112
Mean 55.42
Std Dev 3.139
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl

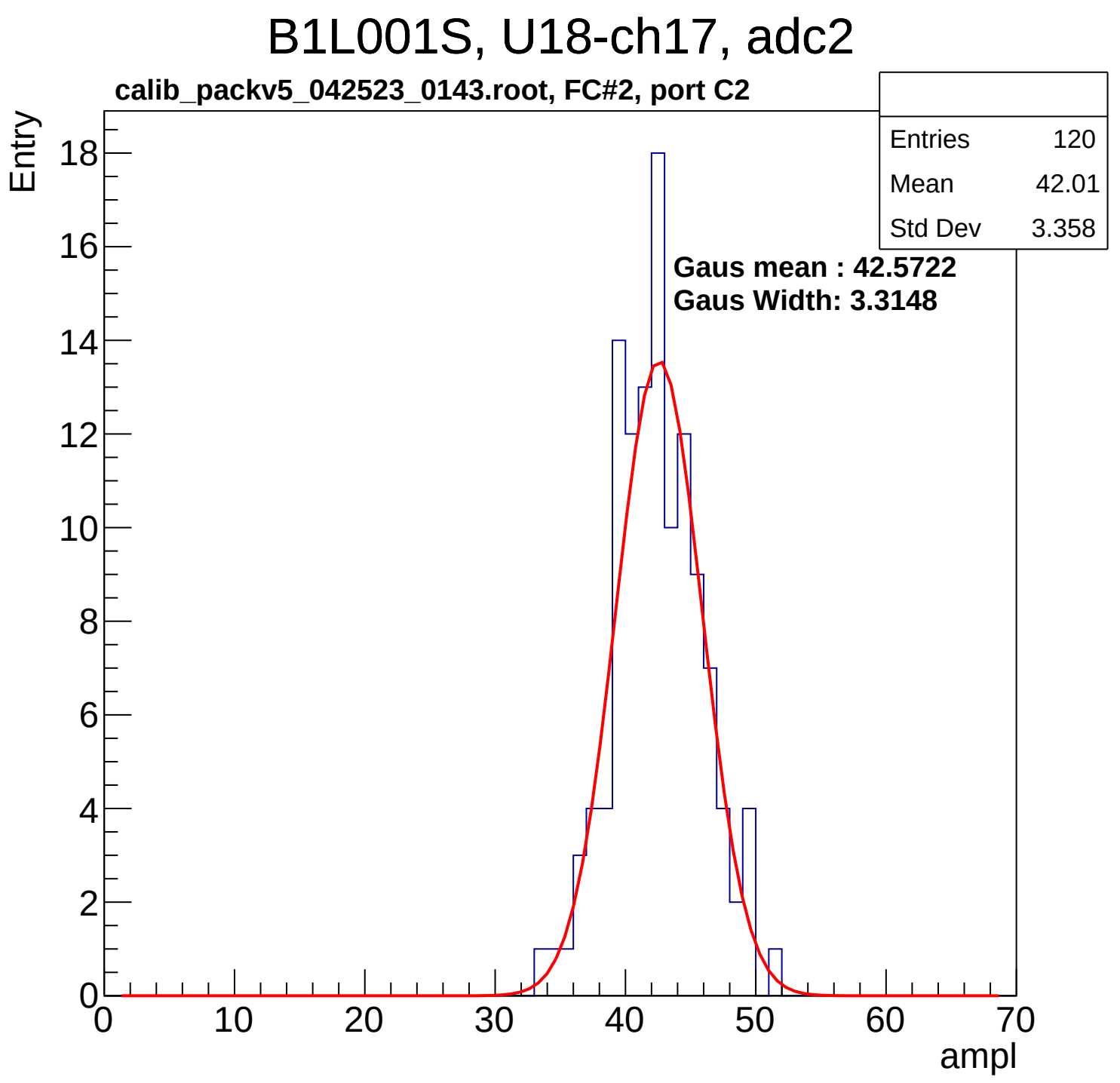

B1L001S, U18-ch16, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 89
Mean 58.29
Std Dev 9.152
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

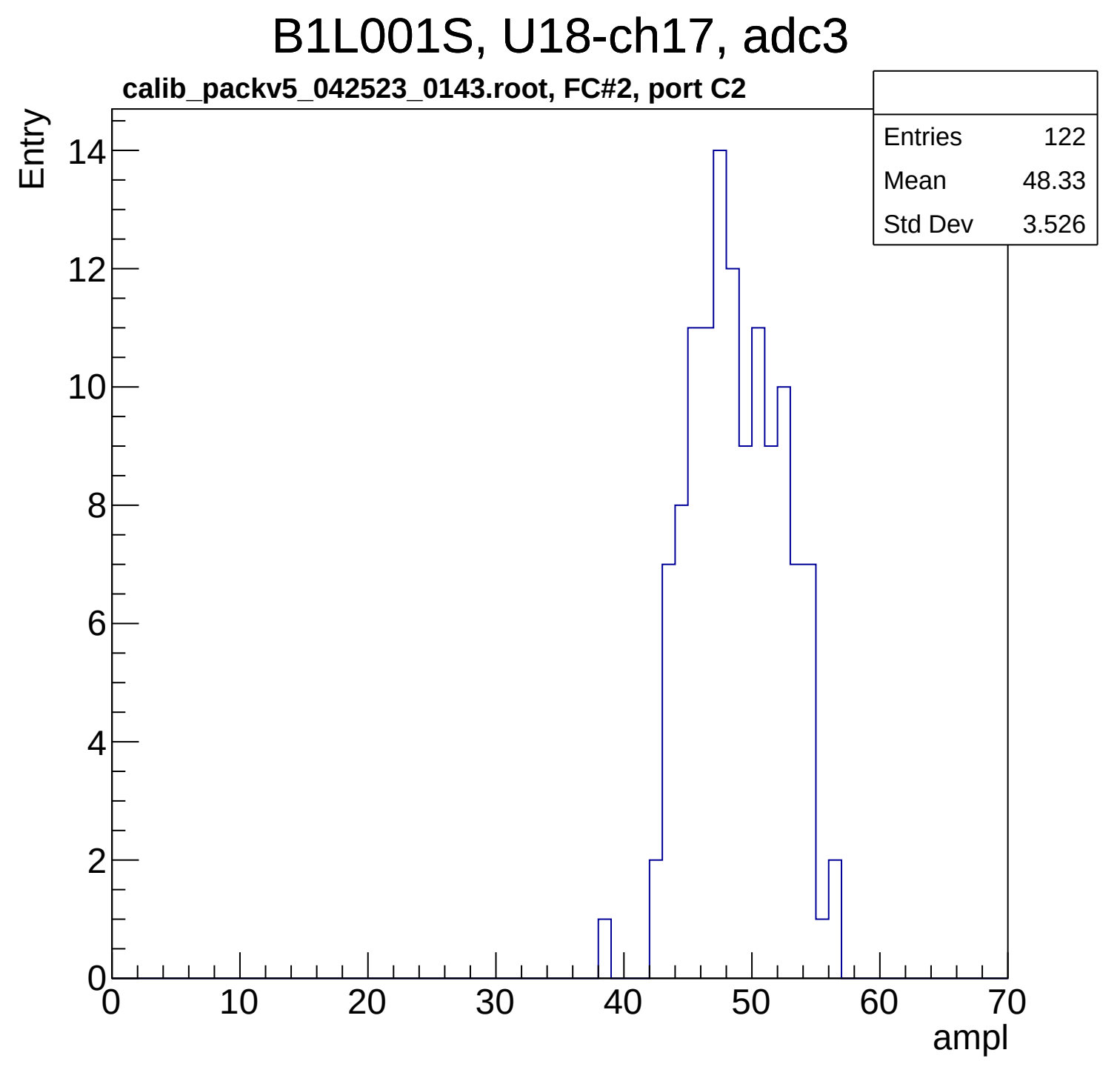

B1L001S, U18-ch16, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 20
Mean 62.05
Std Dev 1.465
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

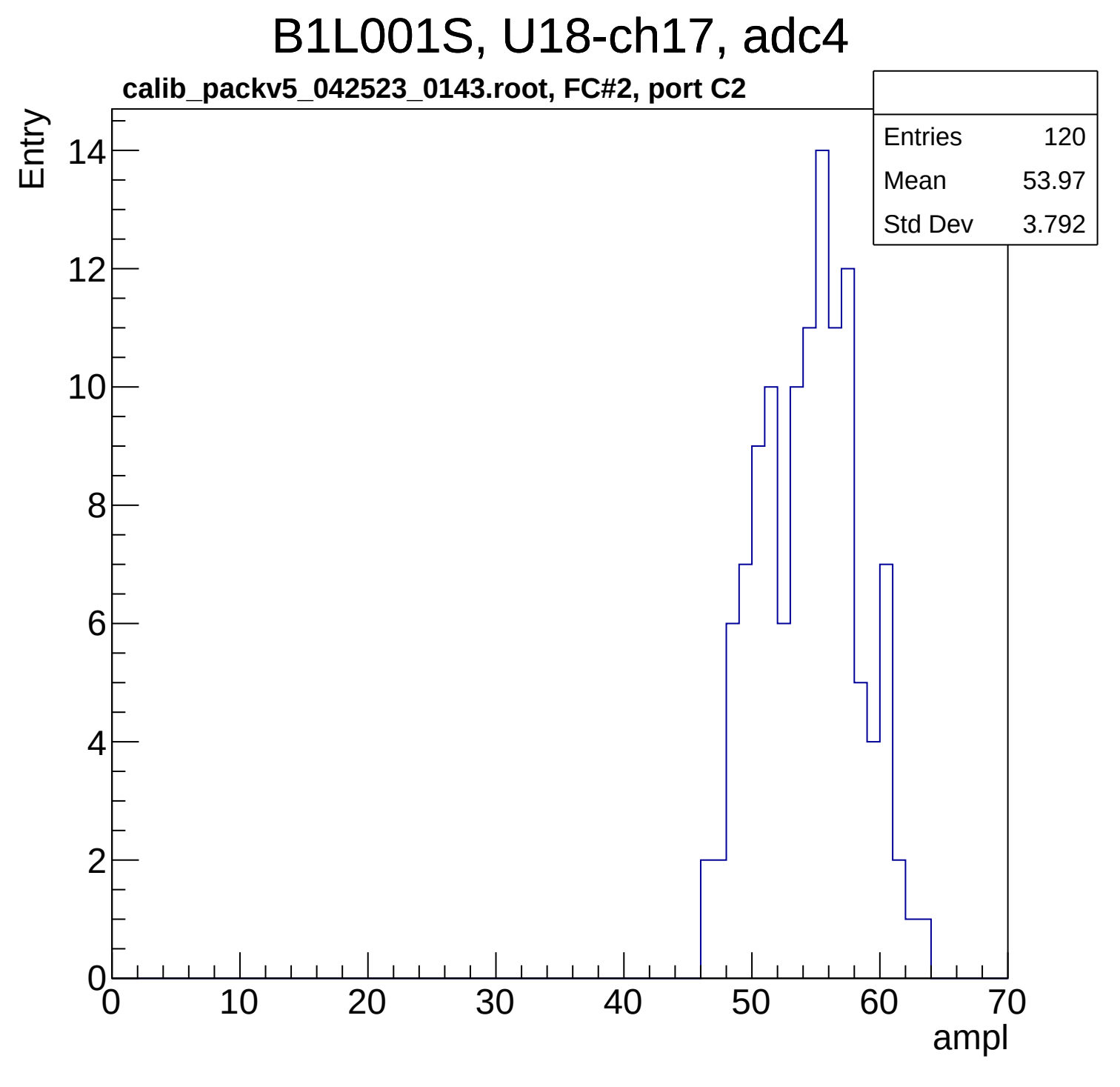

B1L001S, U18-ch16, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 3
Mean 6.667
Std Dev 9.428
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

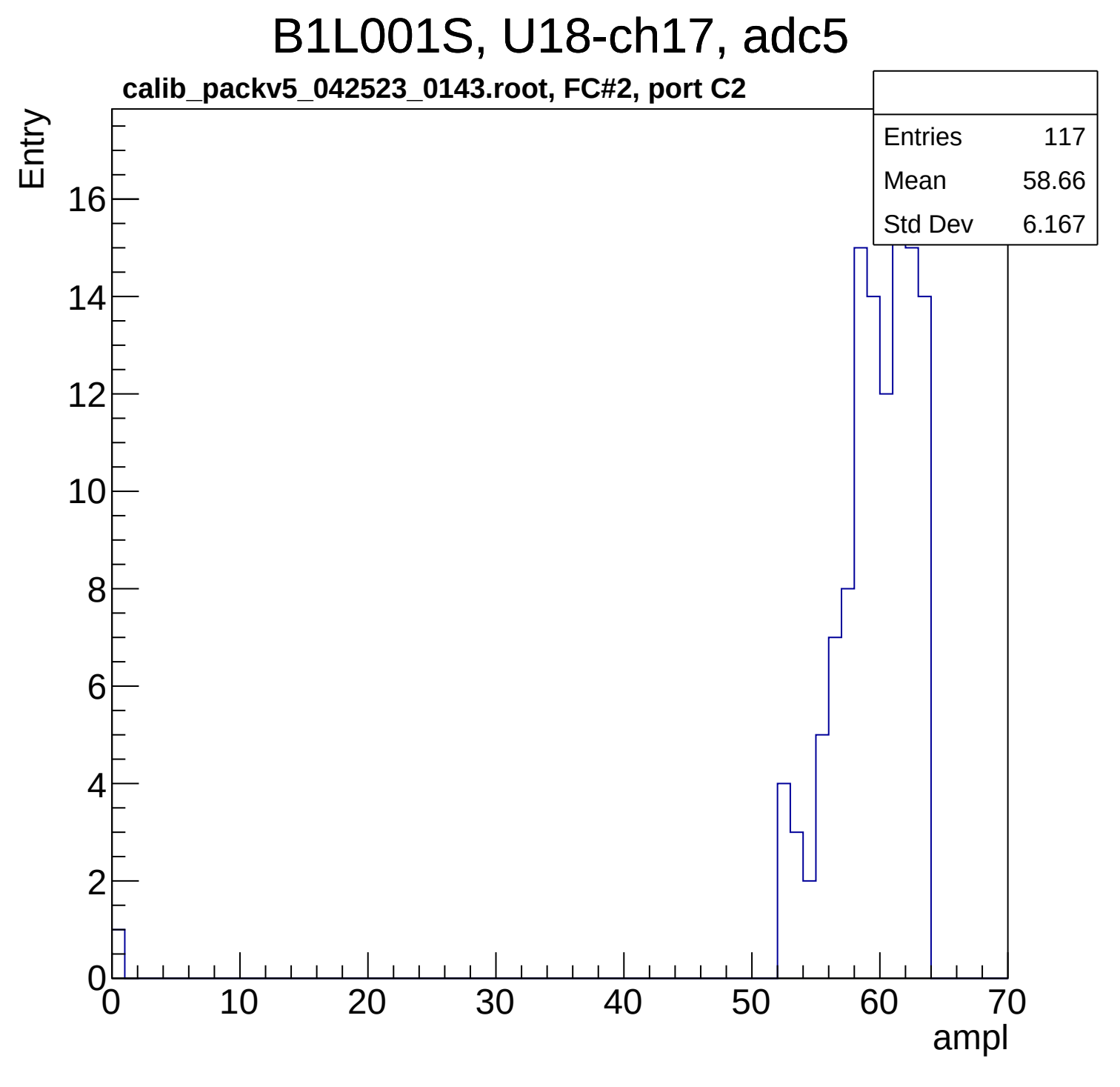

B1L001S, U18-ch17, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 135
Mean 27.89
Std Dev 4.216
Gaus mean : 28.9075
Gaus Width: 3.7524
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

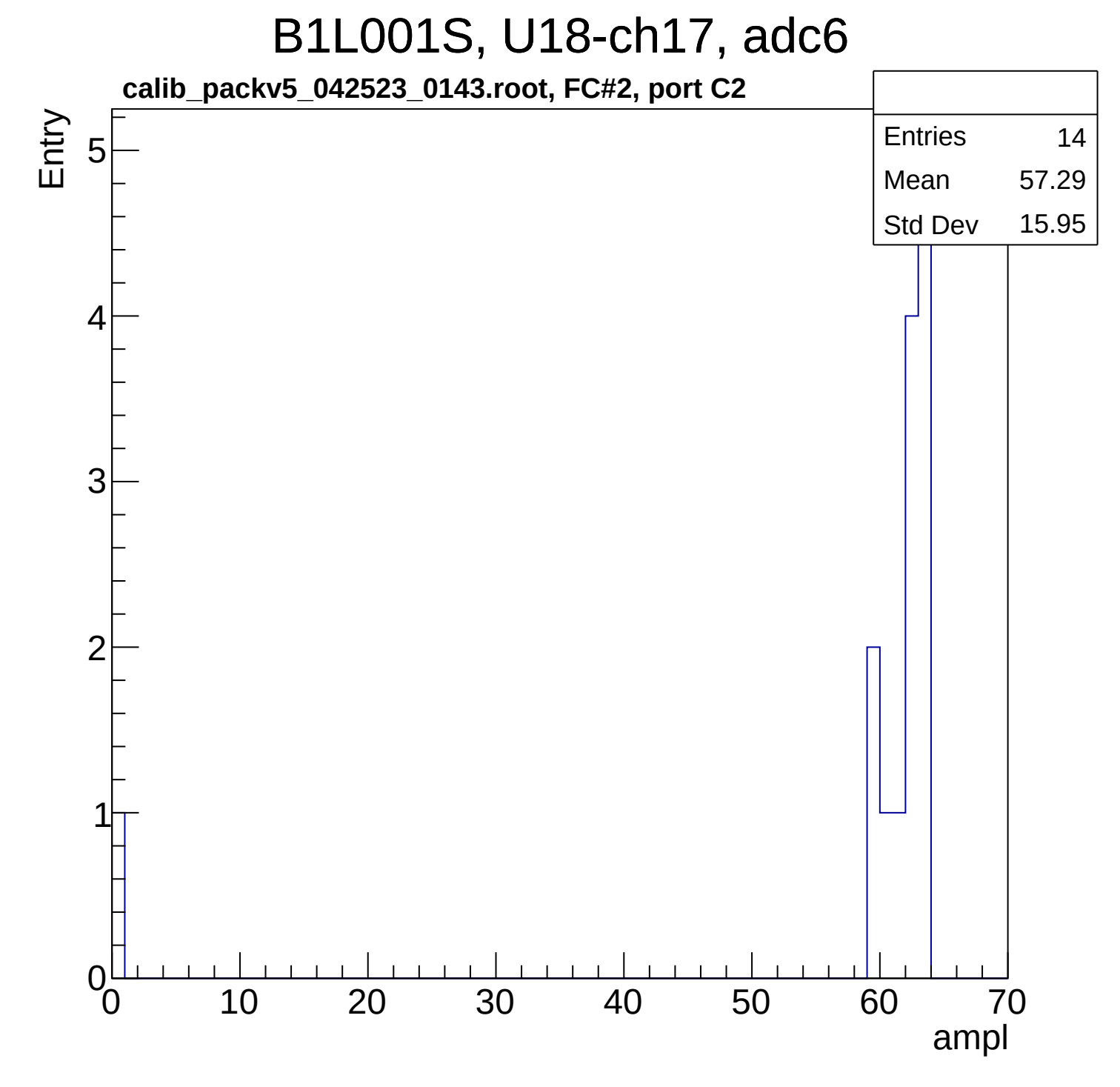

B1L001S, U18-ch17, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 145
Mean 35.3
Std Dev 3.461
Gaus mean : 36.0426
Gaus Width: 3.6589
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

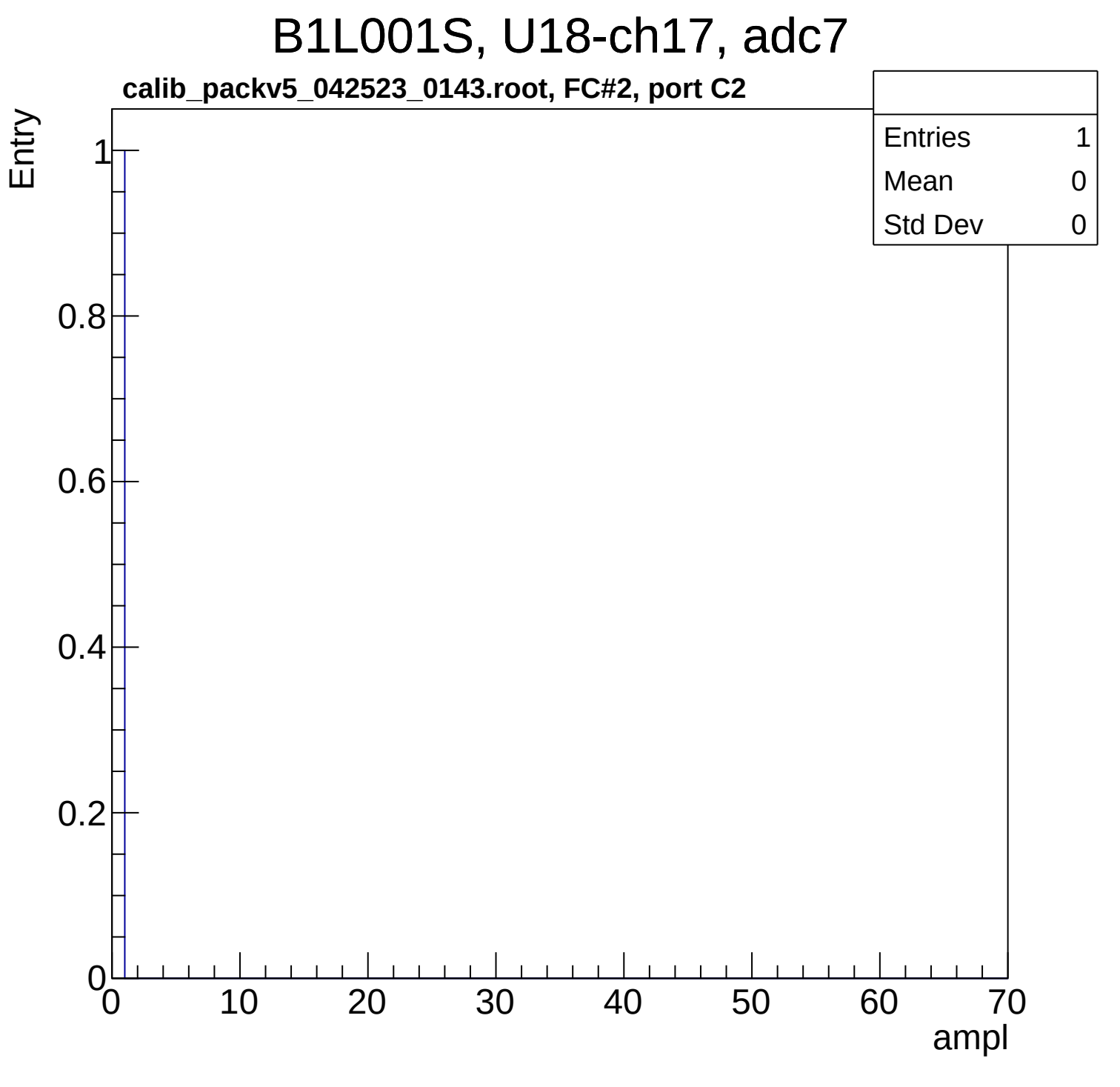

B1L001S, U18-ch17, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 120
Mean 42.01
Std Dev 3.358
Gaus mean : 42.5722
Gaus Width: 3.3148
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

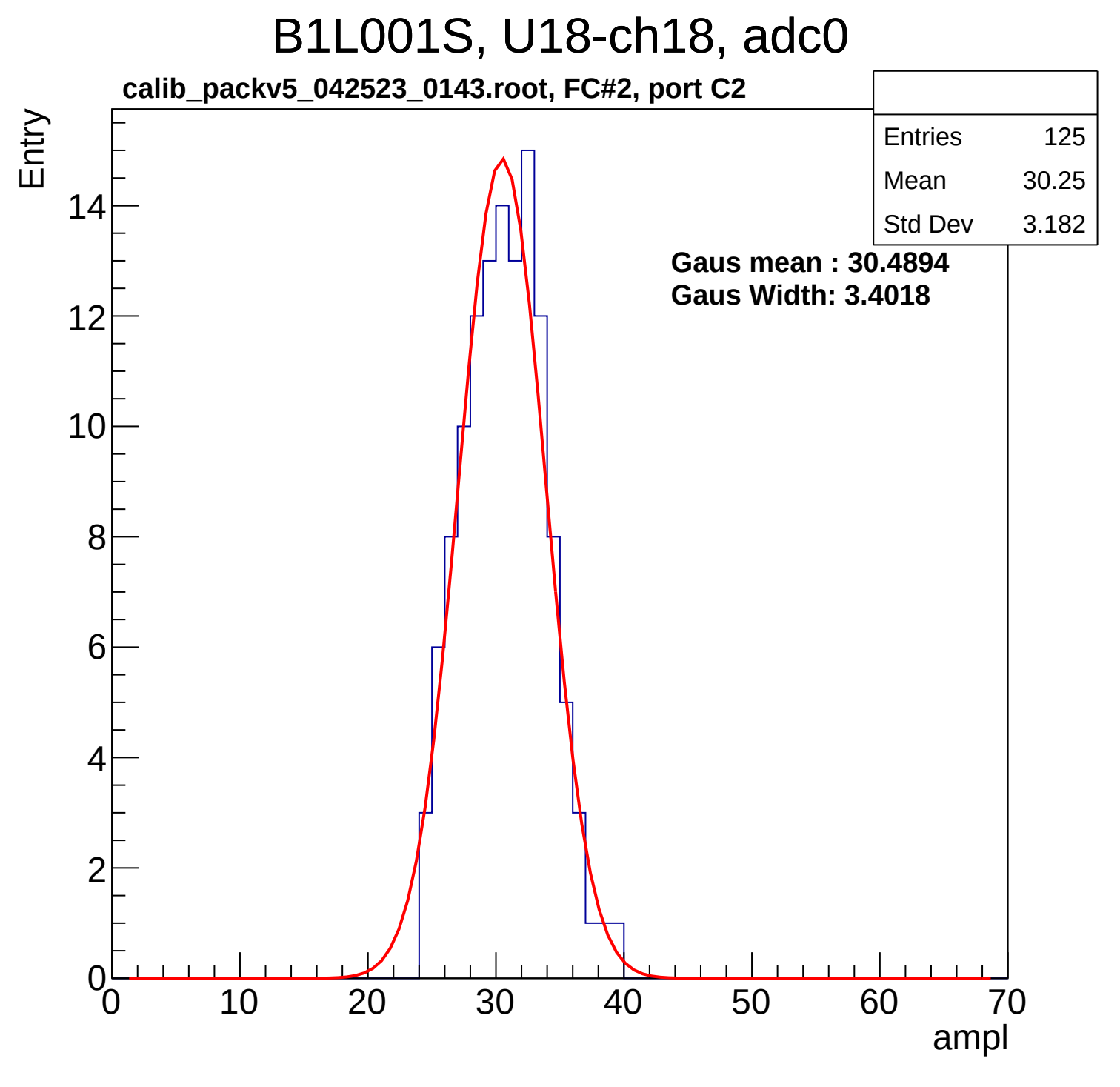

B1L001S, U18-ch17, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 122
Mean 48.33
Std Dev 3.526
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

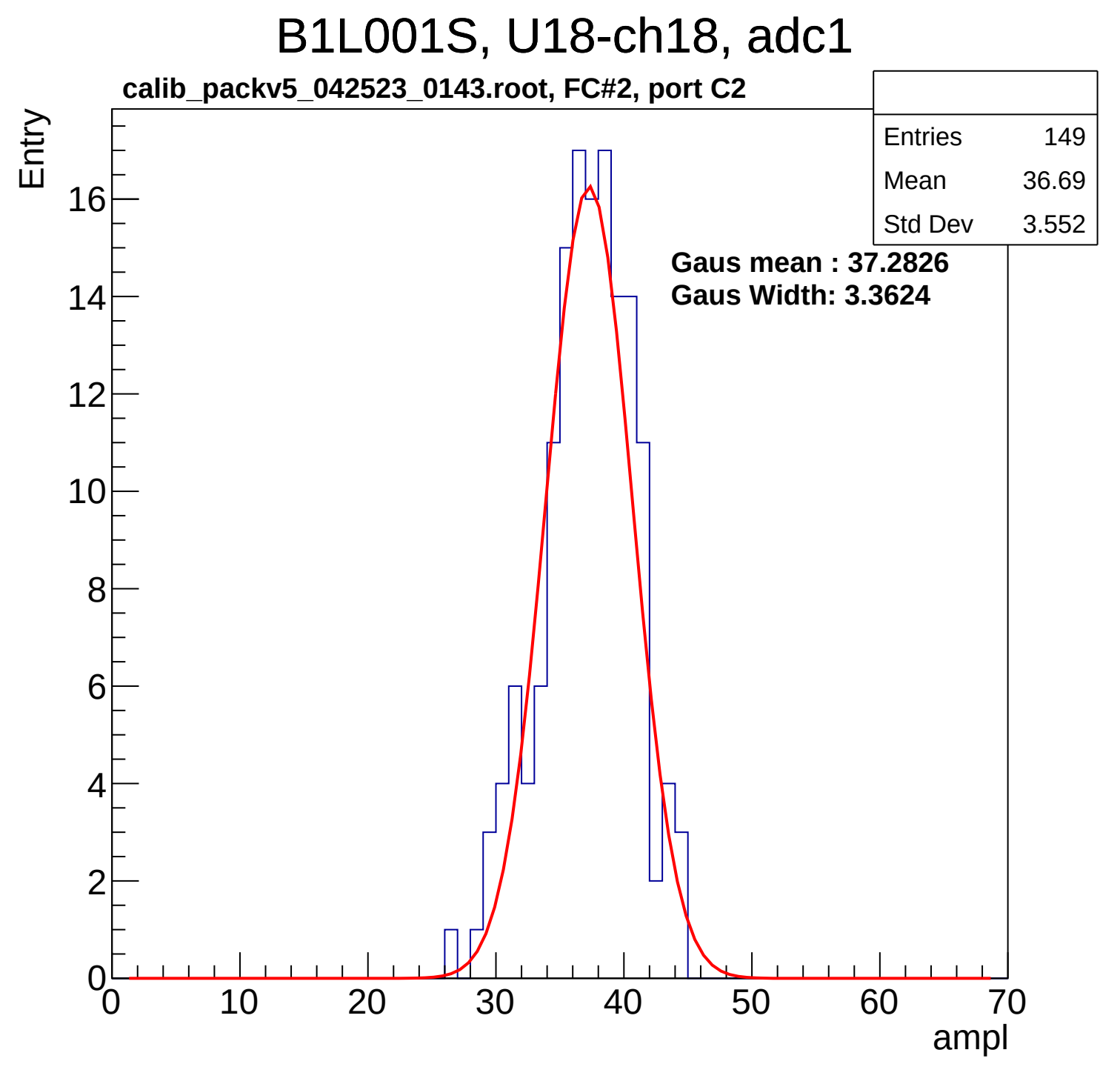

B1L001S, U18-ch17, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 120
Mean 53.97
Std Dev 3.792
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

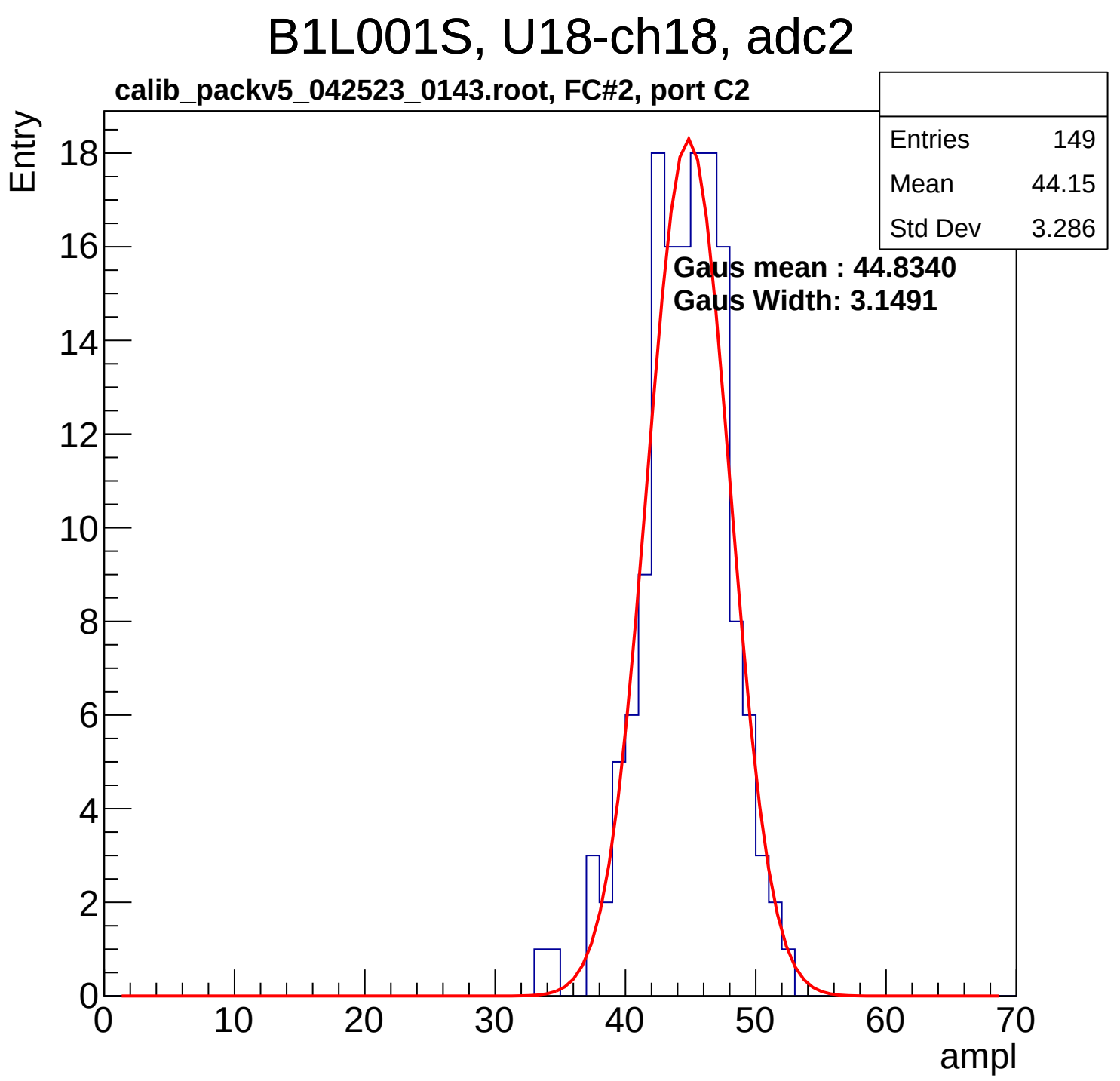

B1L001S, U18-ch17, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 117
Mean 58.66
Std Dev 6.167
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

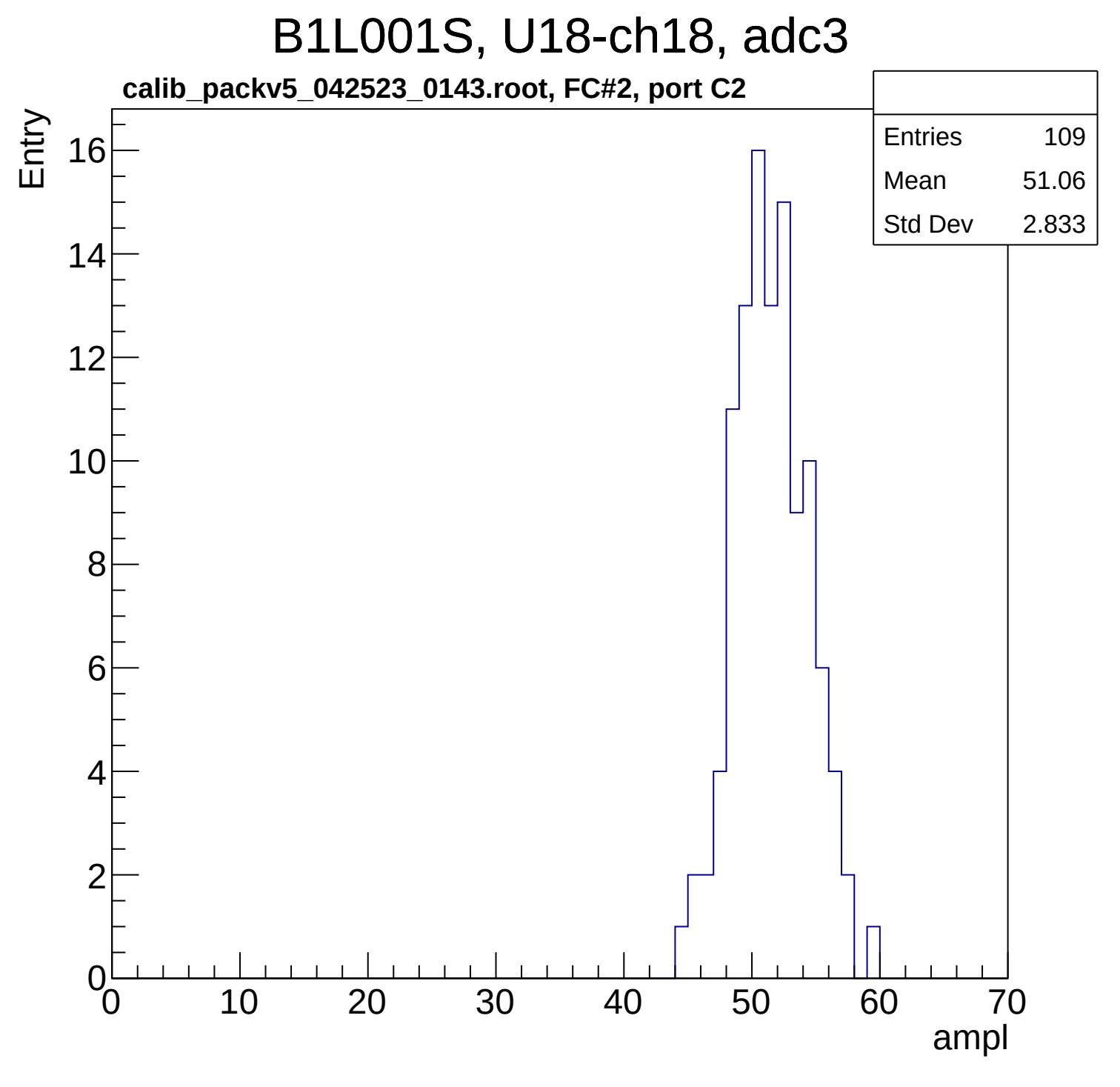

B1L001S, U18-ch17, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 14
Mean 57.29
Std Dev 15.95
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

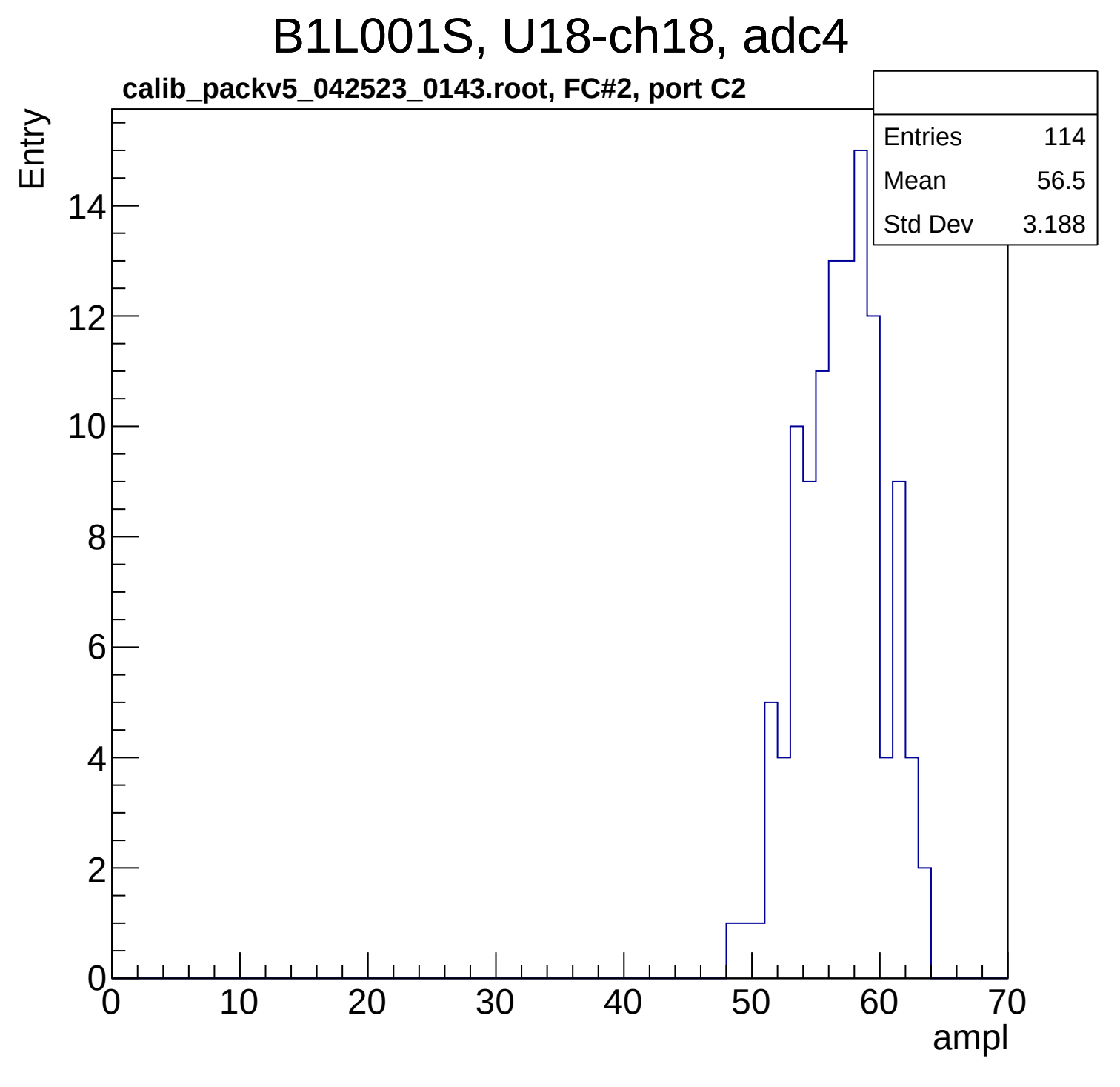

B1L001S, U18-ch17, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

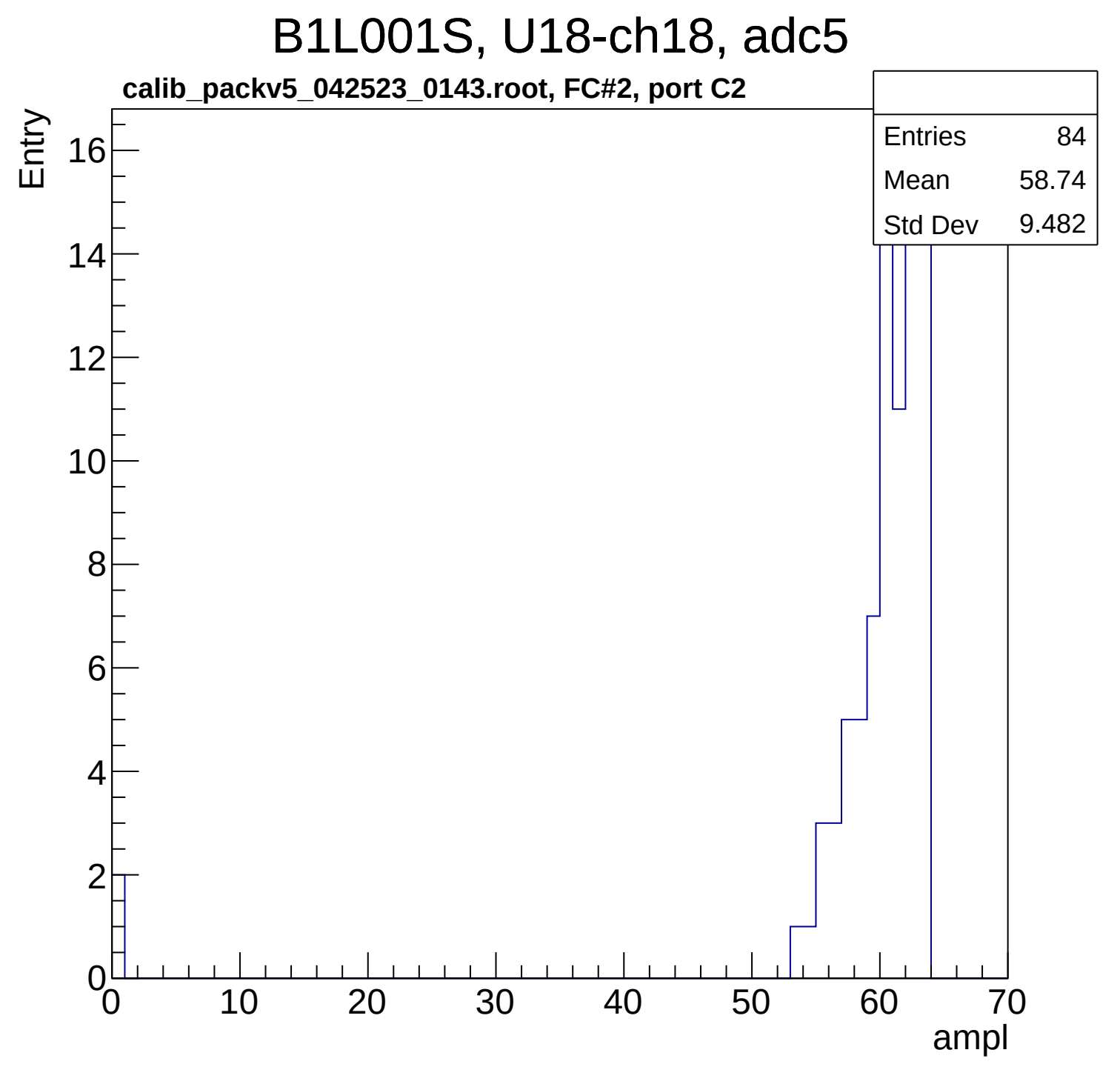

B1L001S, U18-ch18, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 125
Mean 30.25
Std Dev 3.182
Gaus mean : 30.4894
Gaus Width: 3.4018
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

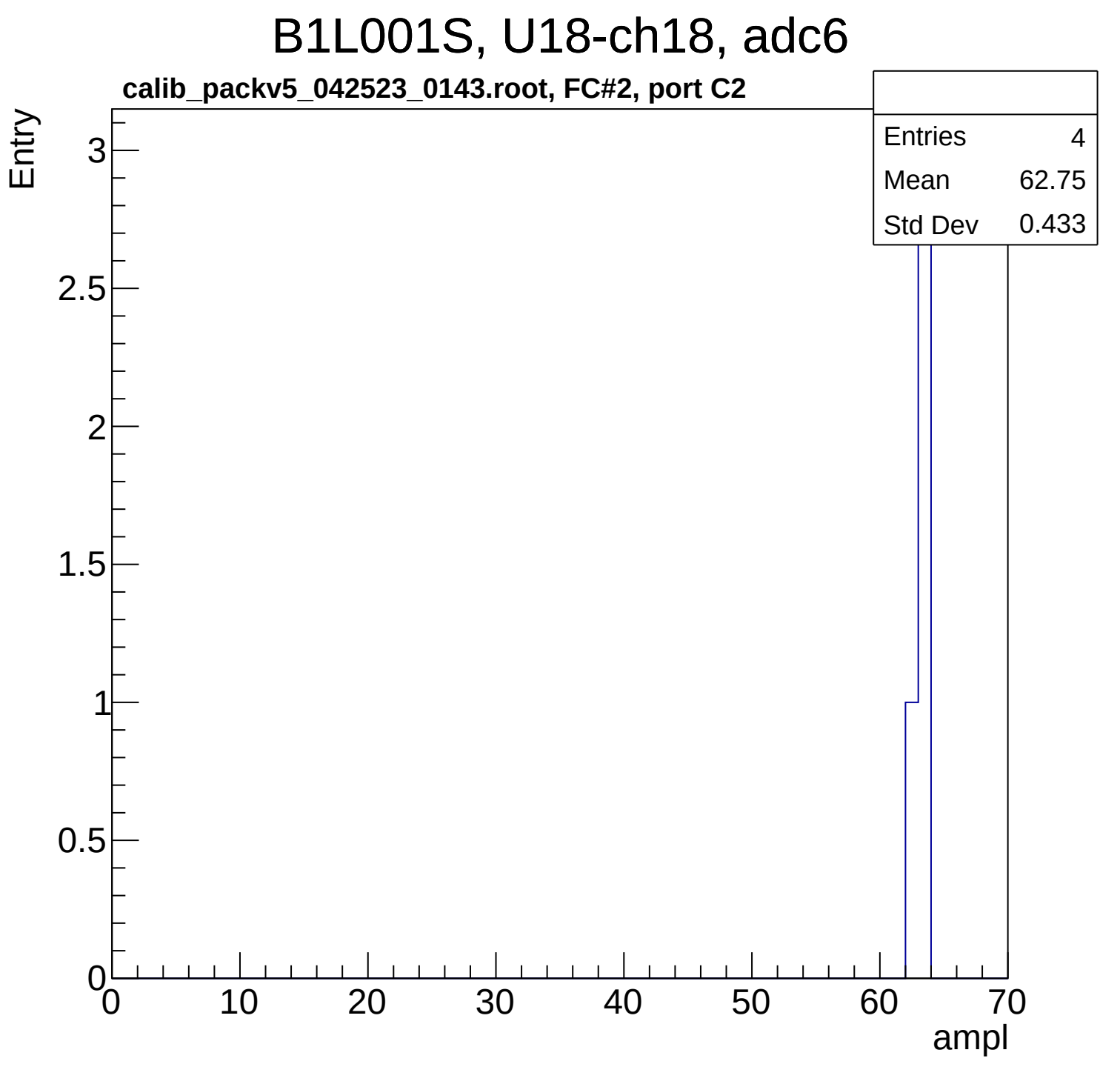

B1L001S, U18-ch18, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 149
Mean 36.69
Std Dev 3.552
Gaus mean : 37.2826
Gaus Width: 3.3624
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

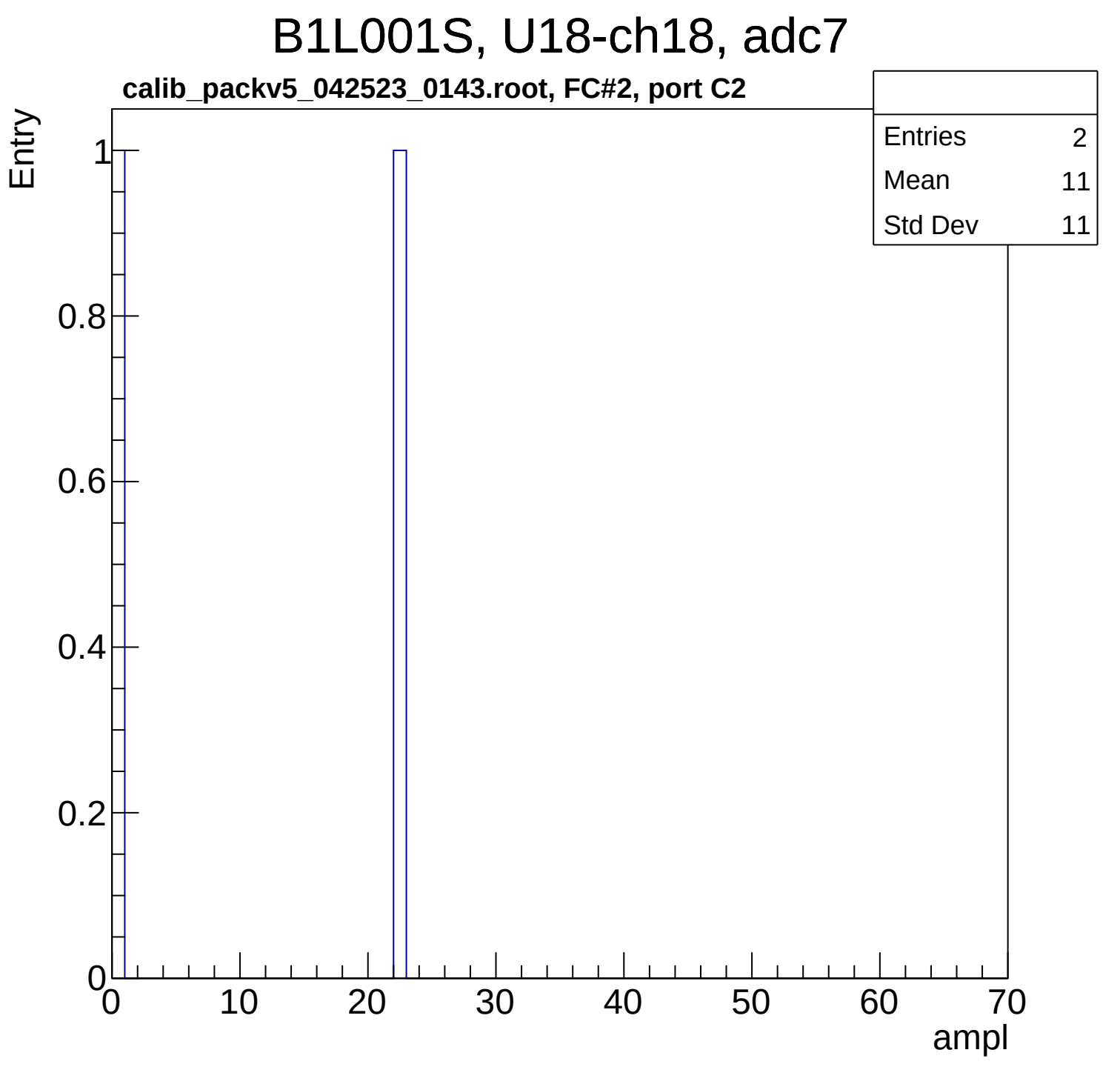

B1L001S, U18-ch18, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 149
Mean 44.15
Std Dev 3.286
Gaus mean : 44.8340
Gaus Width: 3.1491
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

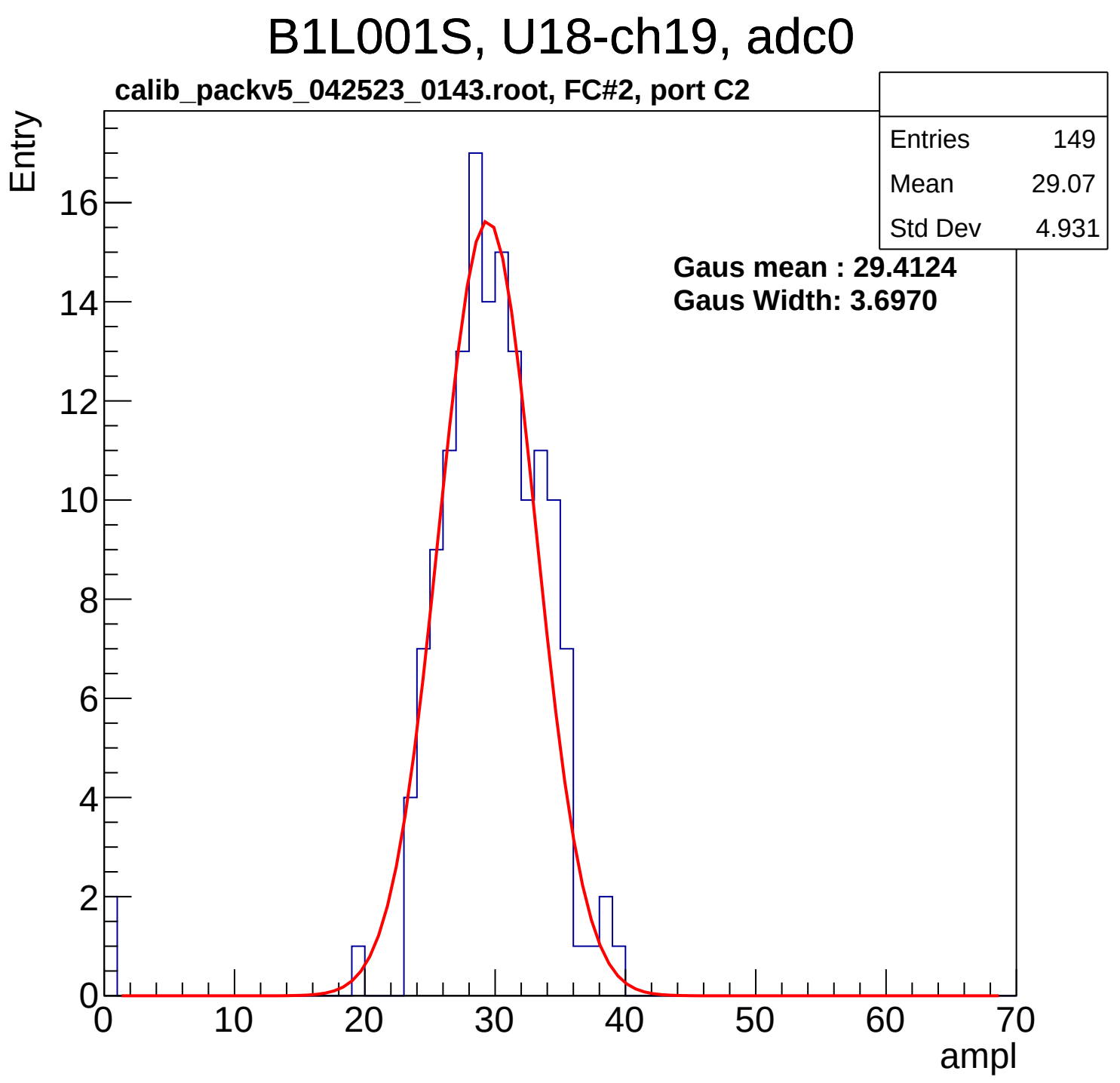

B1L001S, U18-ch18, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 109
Mean 51.06
Std Dev 2.833
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

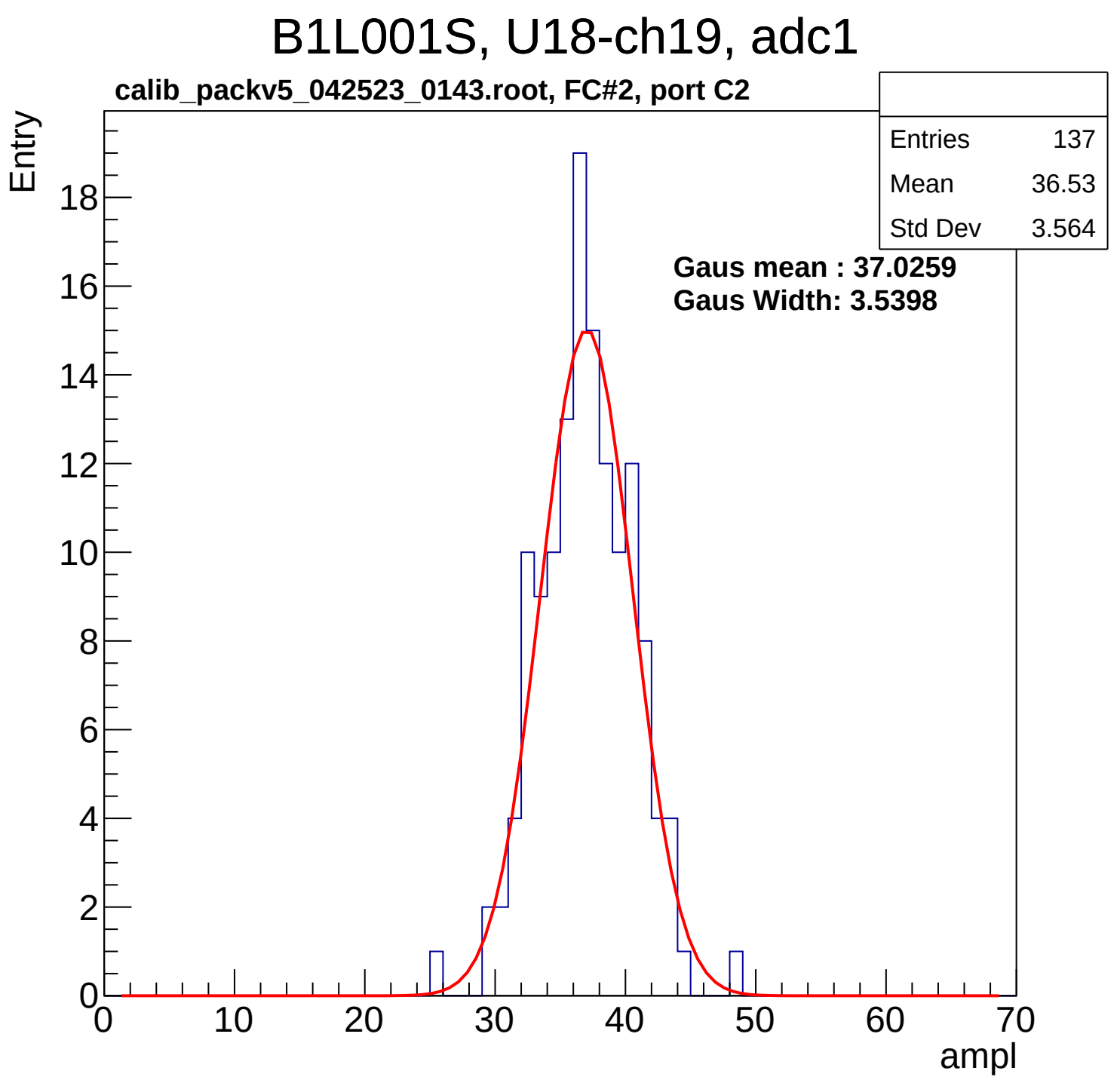

B1L001S, U18-ch18, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 114
Mean 56.5
Std Dev 3.188
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl

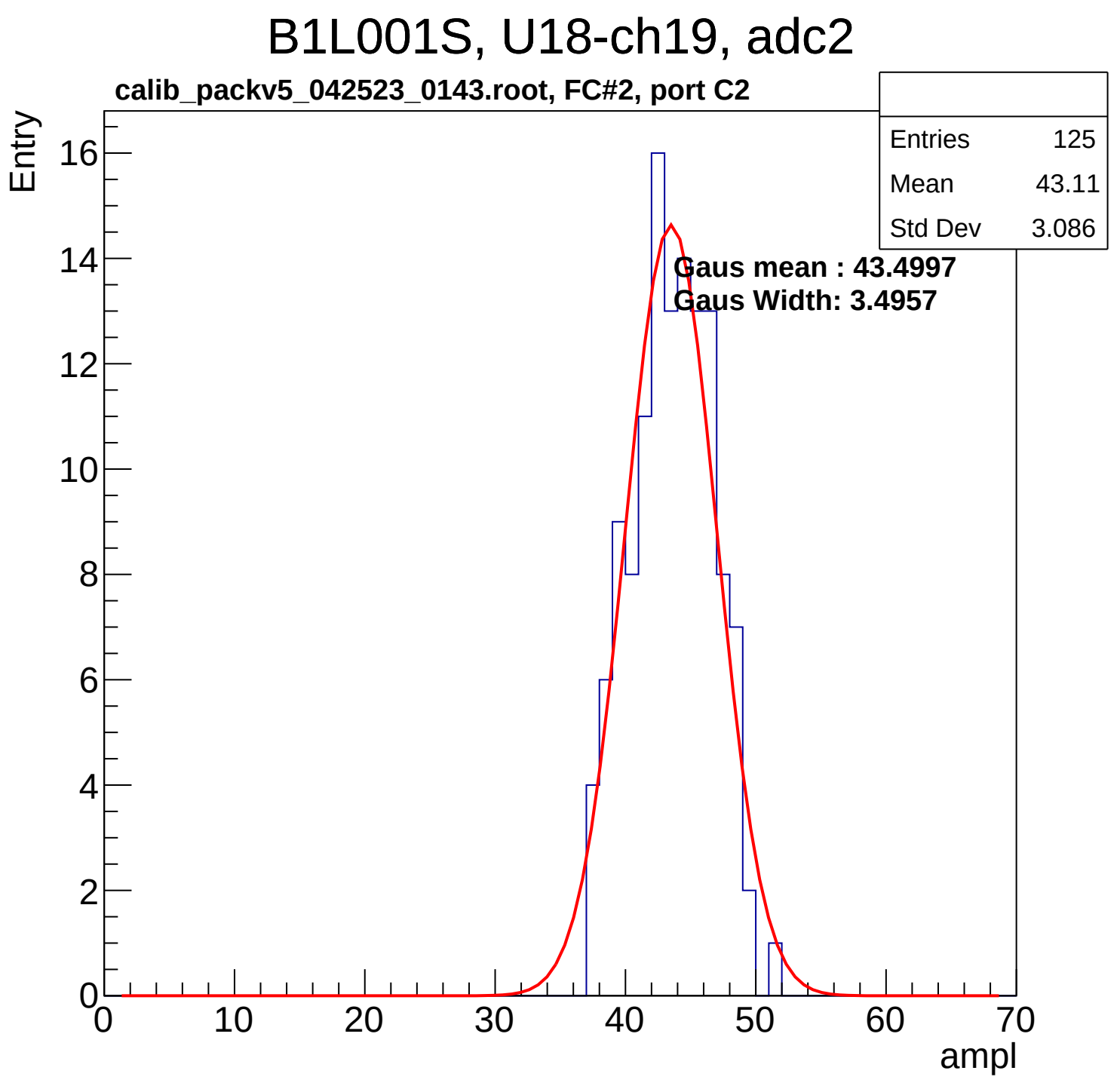

B1L001S, U18-ch18, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 84
Mean 58.74
Std Dev 9.482
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

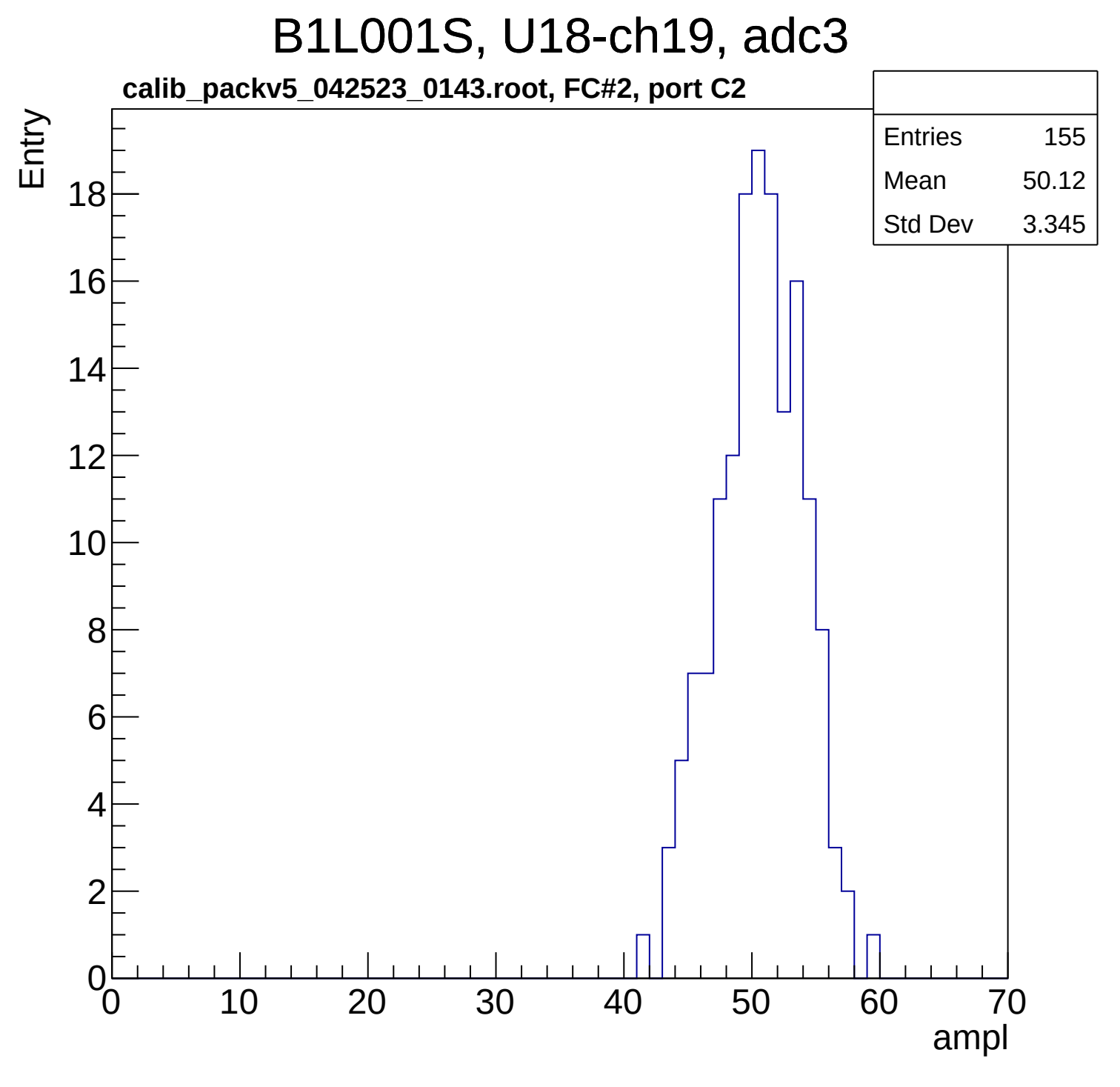

B1L001S, U18-ch18, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 4
Mean 62.75
Std Dev 0.433
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

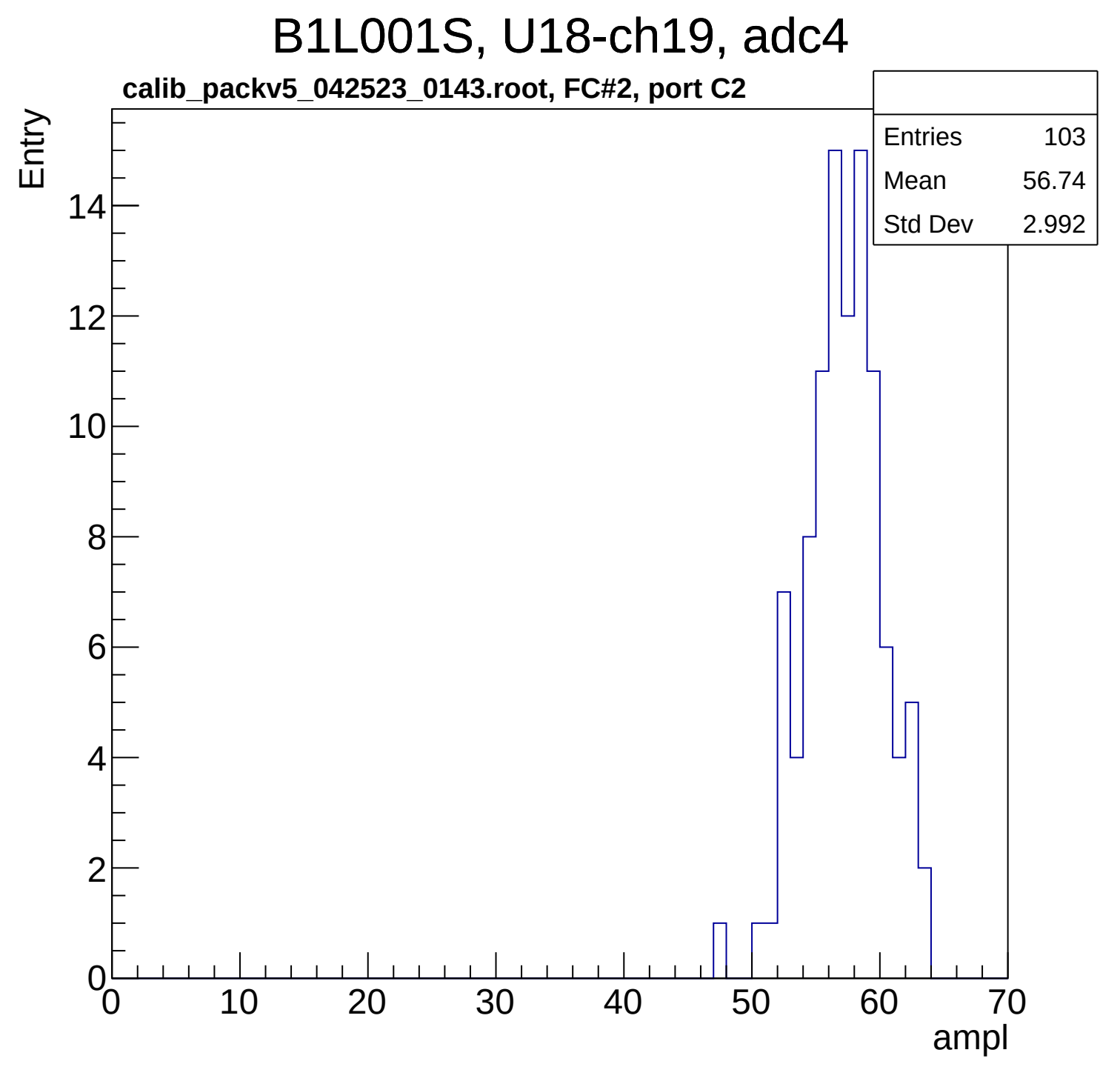

B1L001S, U18-ch18, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 11
Std Dev 11
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

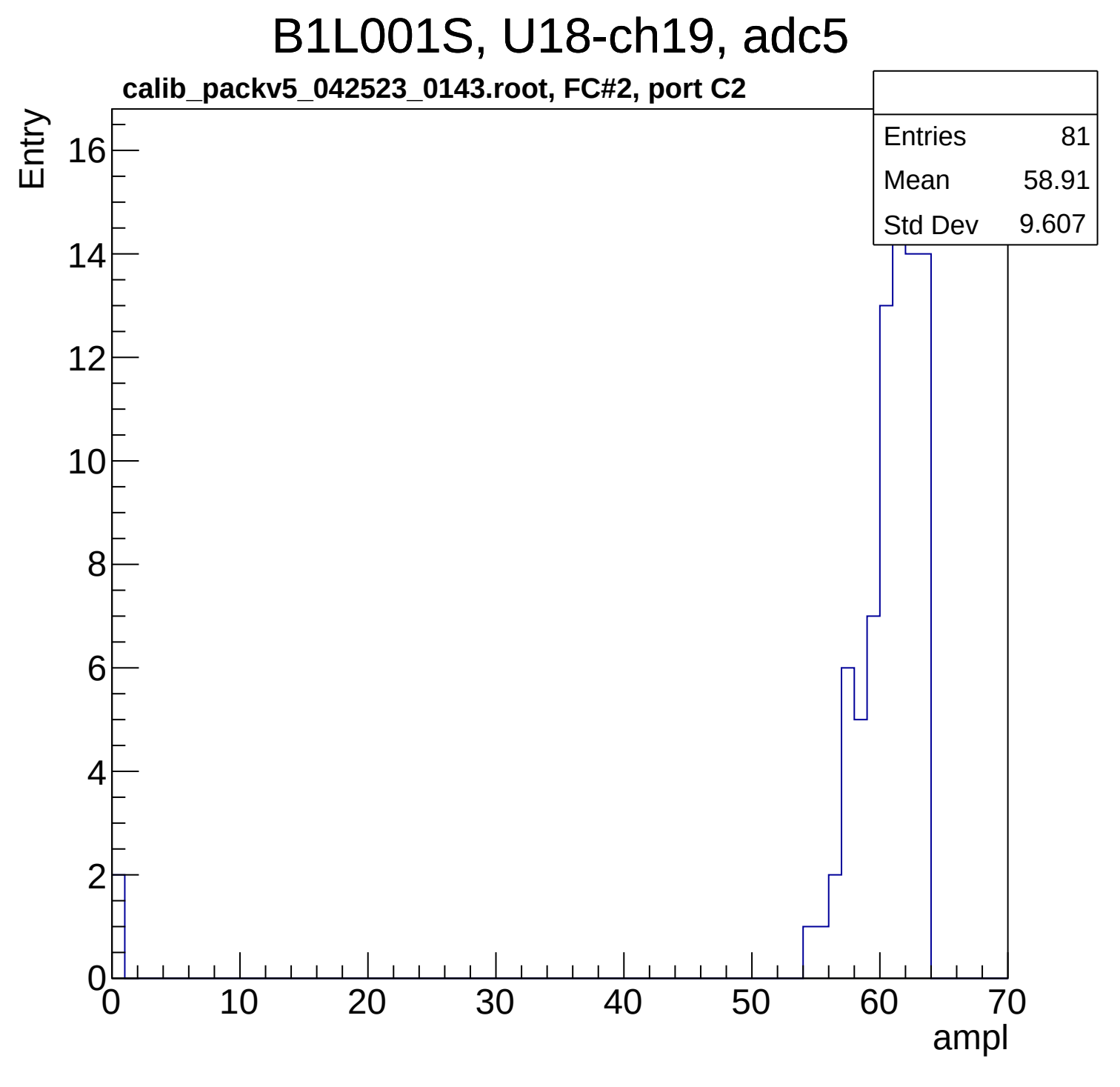

B1L001S, U18-ch19, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 149
Mean 29.07
Std Dev 4.931
Gaus mean : 29.4124
Gaus Width: 3.6970
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

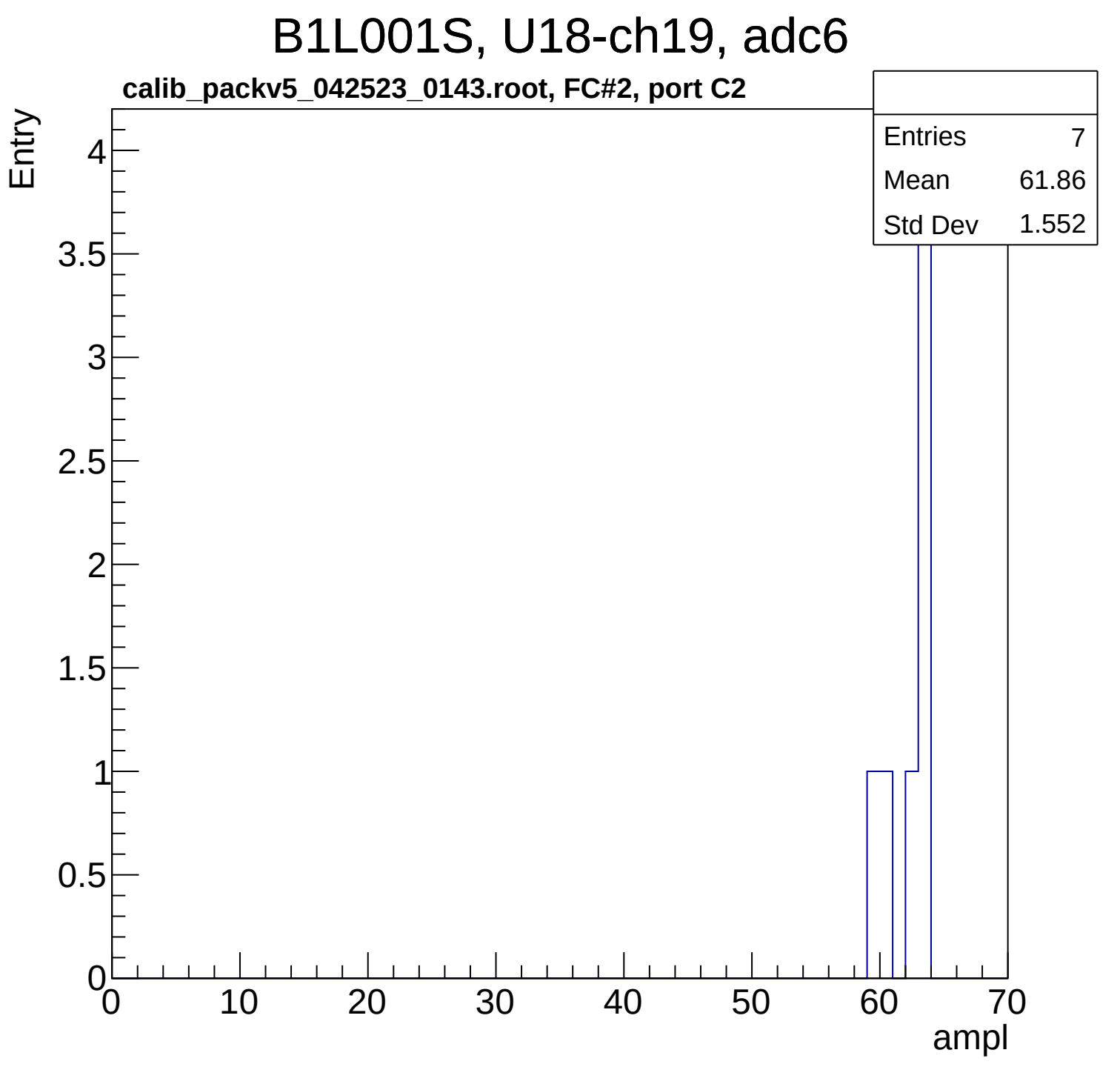

B1L001S, U18-ch19, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 137
Mean 36.53
Std Dev 3.564
Gaus mean : 37.0259
Gaus Width: 3.5398
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

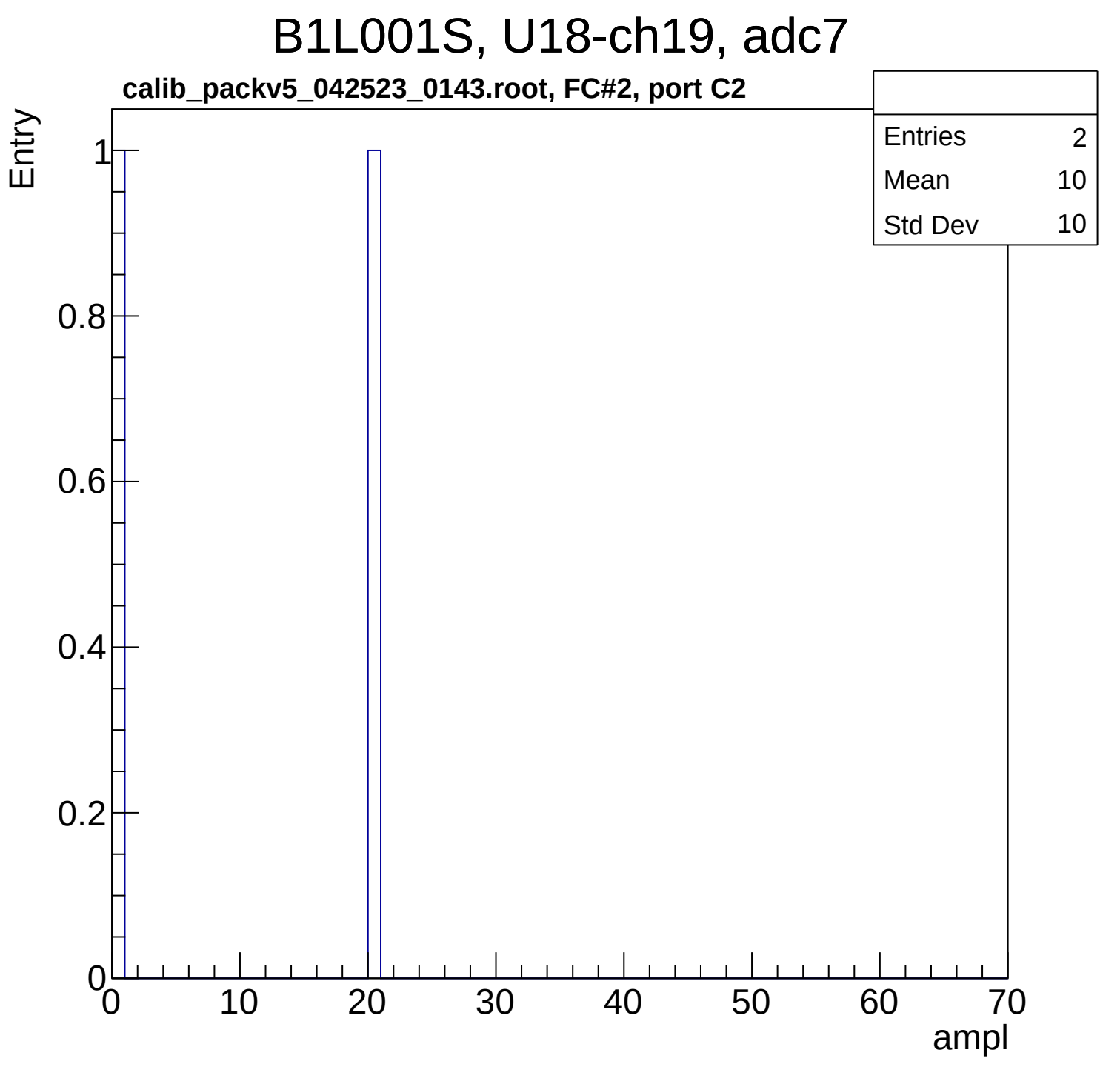

B1L001S, U18-ch19, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 125
Mean 43.11
Std Dev 3.086
Gaus mean : 43.4997
Gaus Width: 3.4957
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

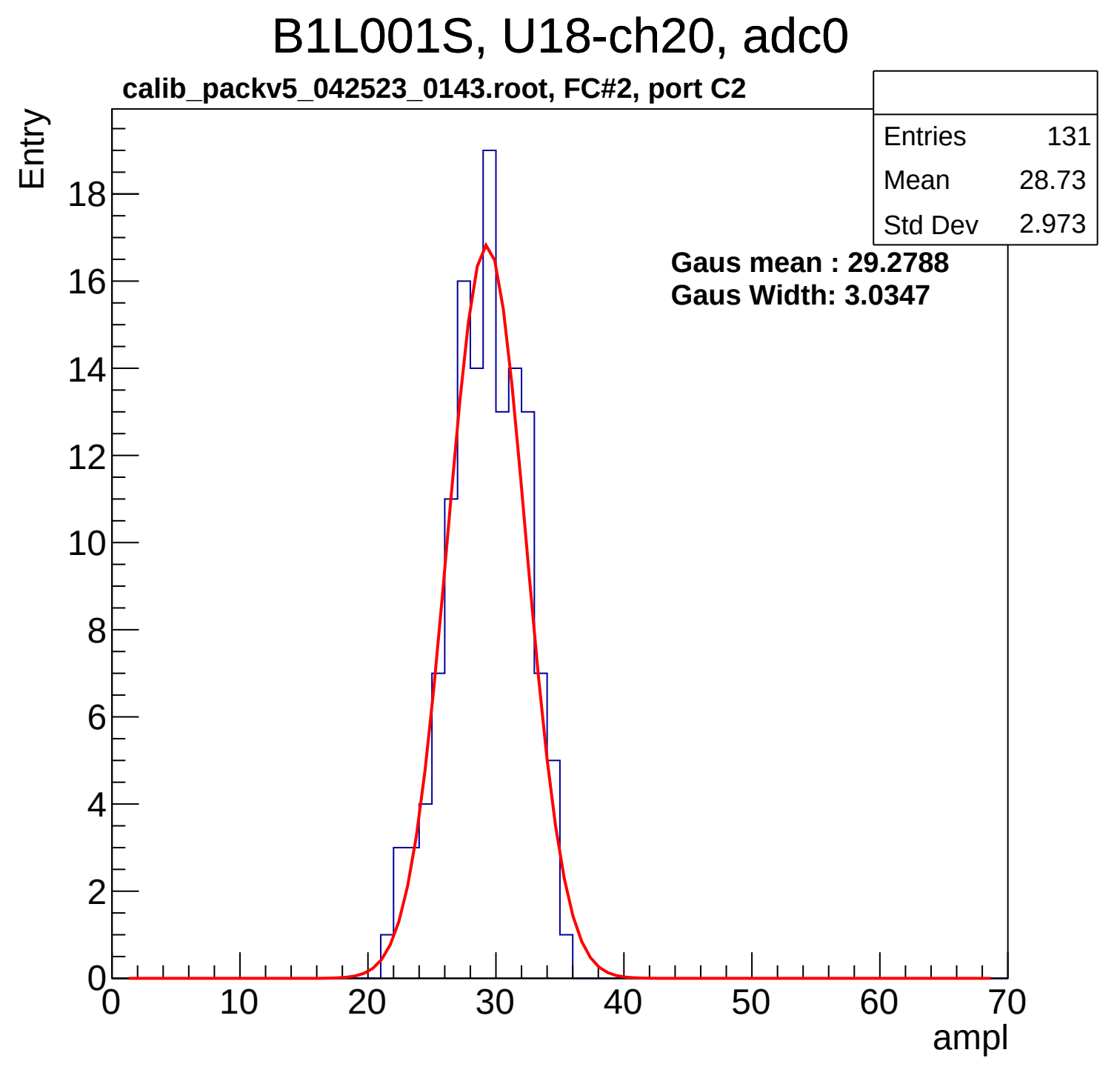

B1L001S, U18-ch19, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 155
Mean 50.12
Std Dev 3.345
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

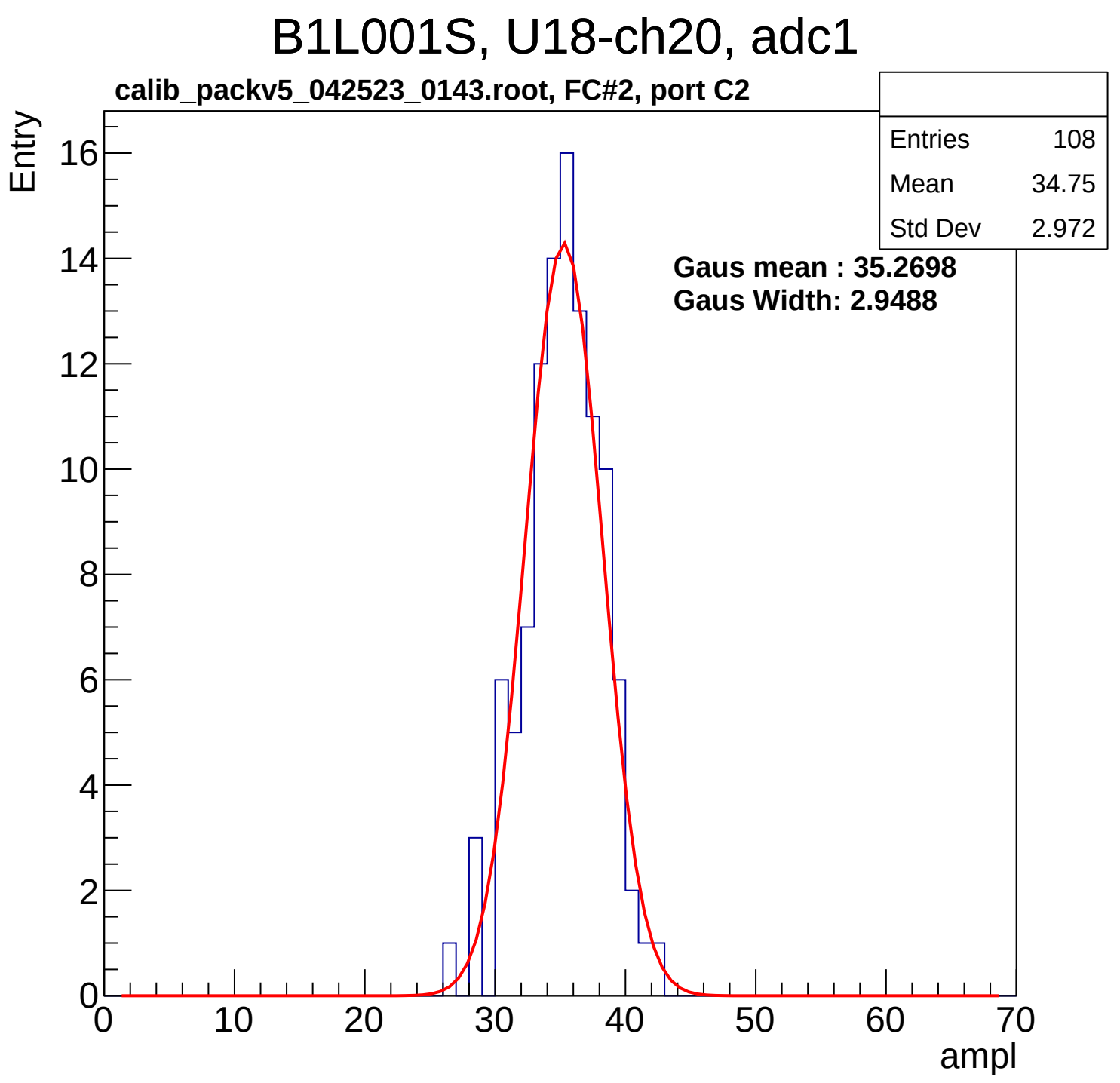

B1L001S, U18-ch19, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 103
Mean 56.74
Std Dev 2.992
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

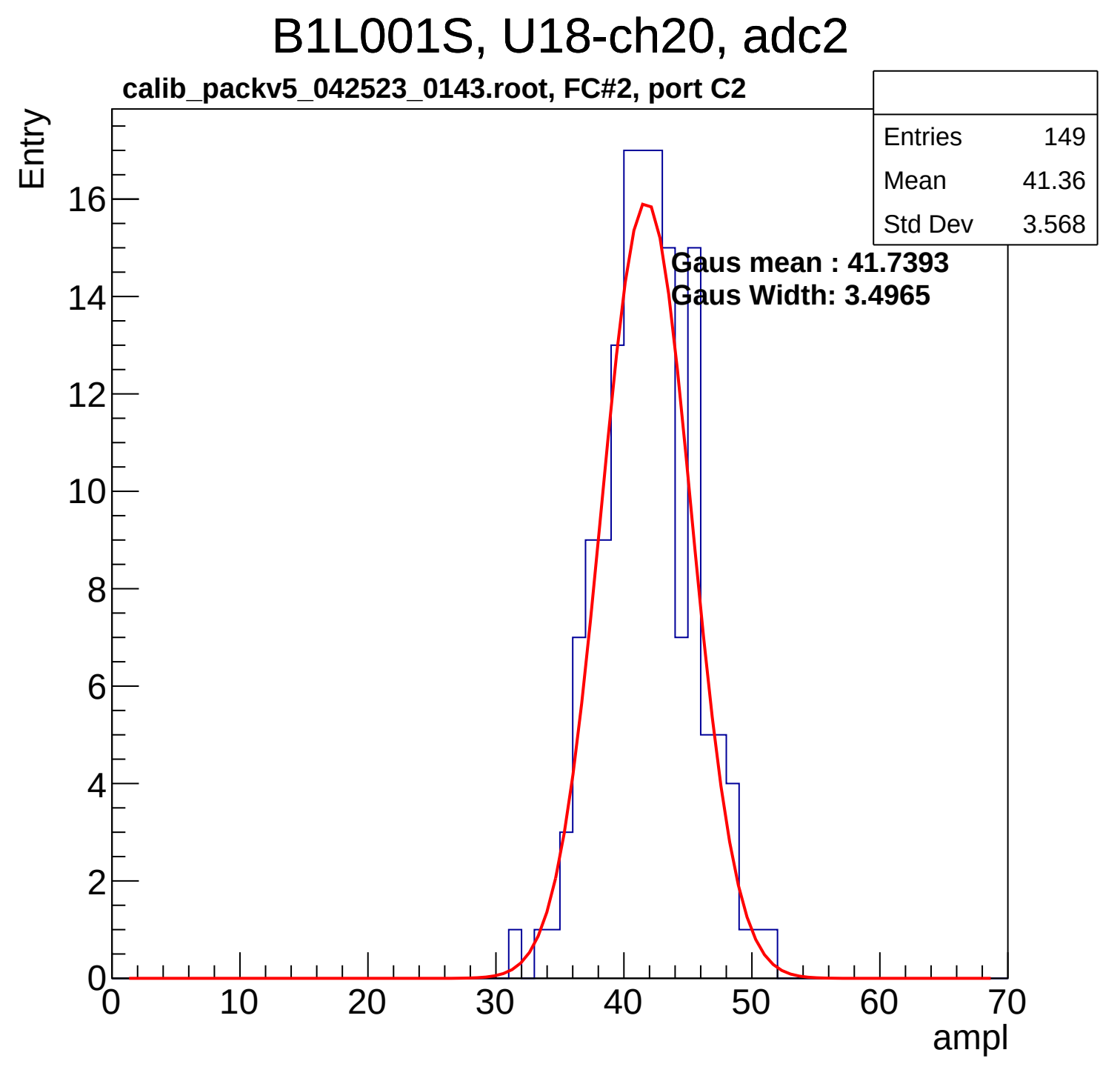

B1L001S, U18-ch19, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 81
Mean 58.91
Std Dev 9.607
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

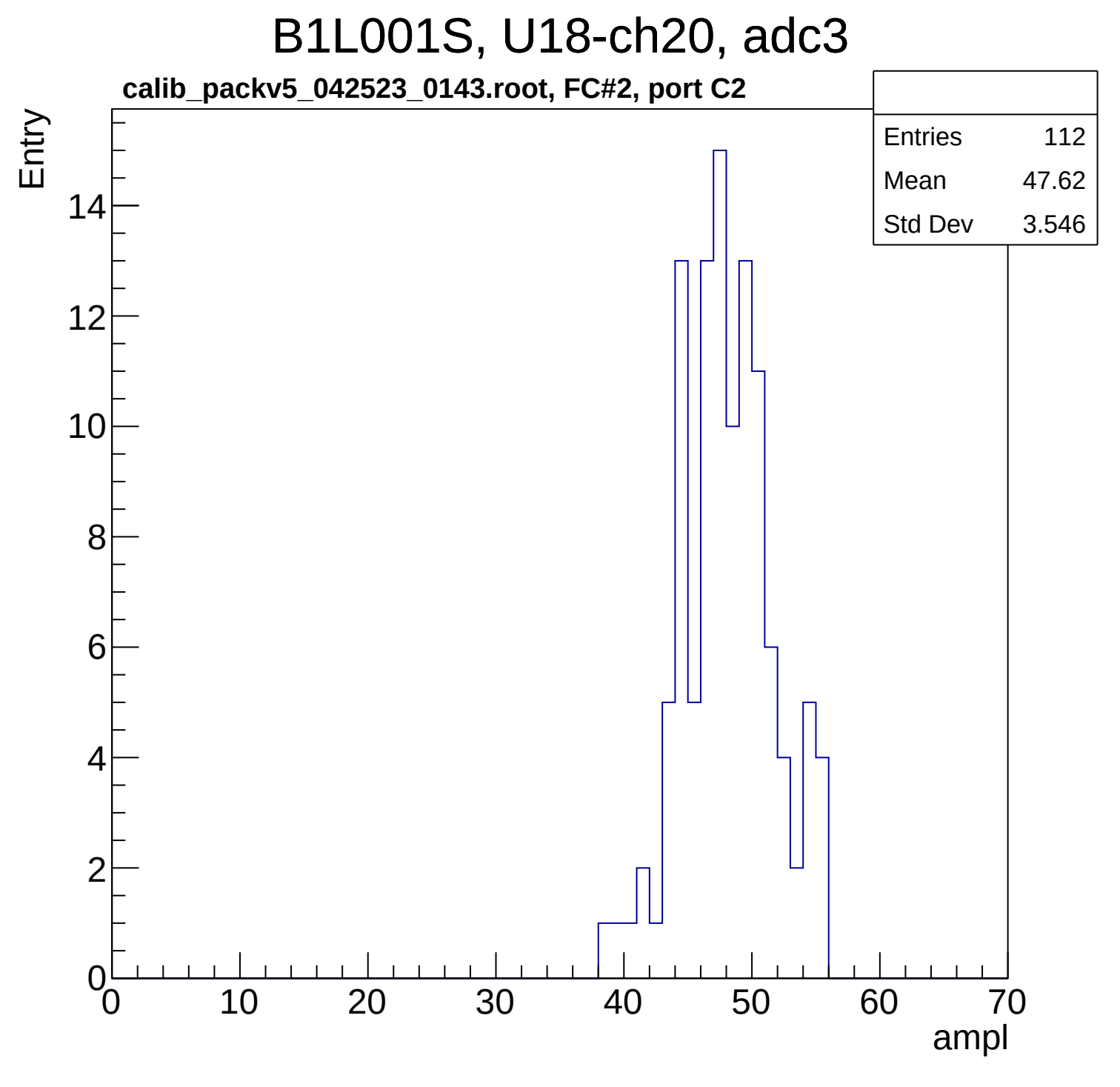

B1L001S, U18-ch19, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 7
Mean 61.86
Std Dev 1.552
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

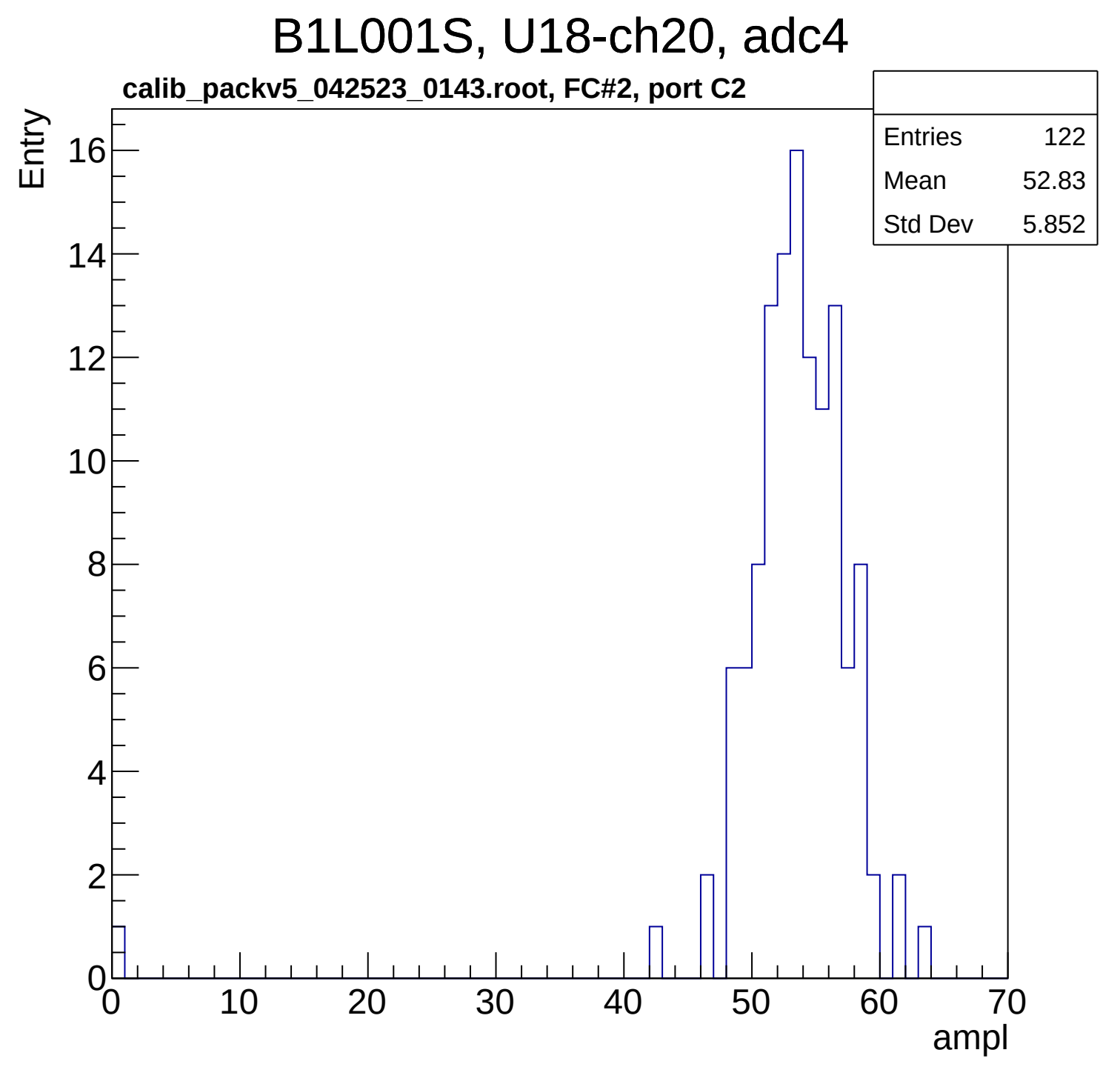

B1L001S, U18-ch19, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 10
Std Dev 10
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

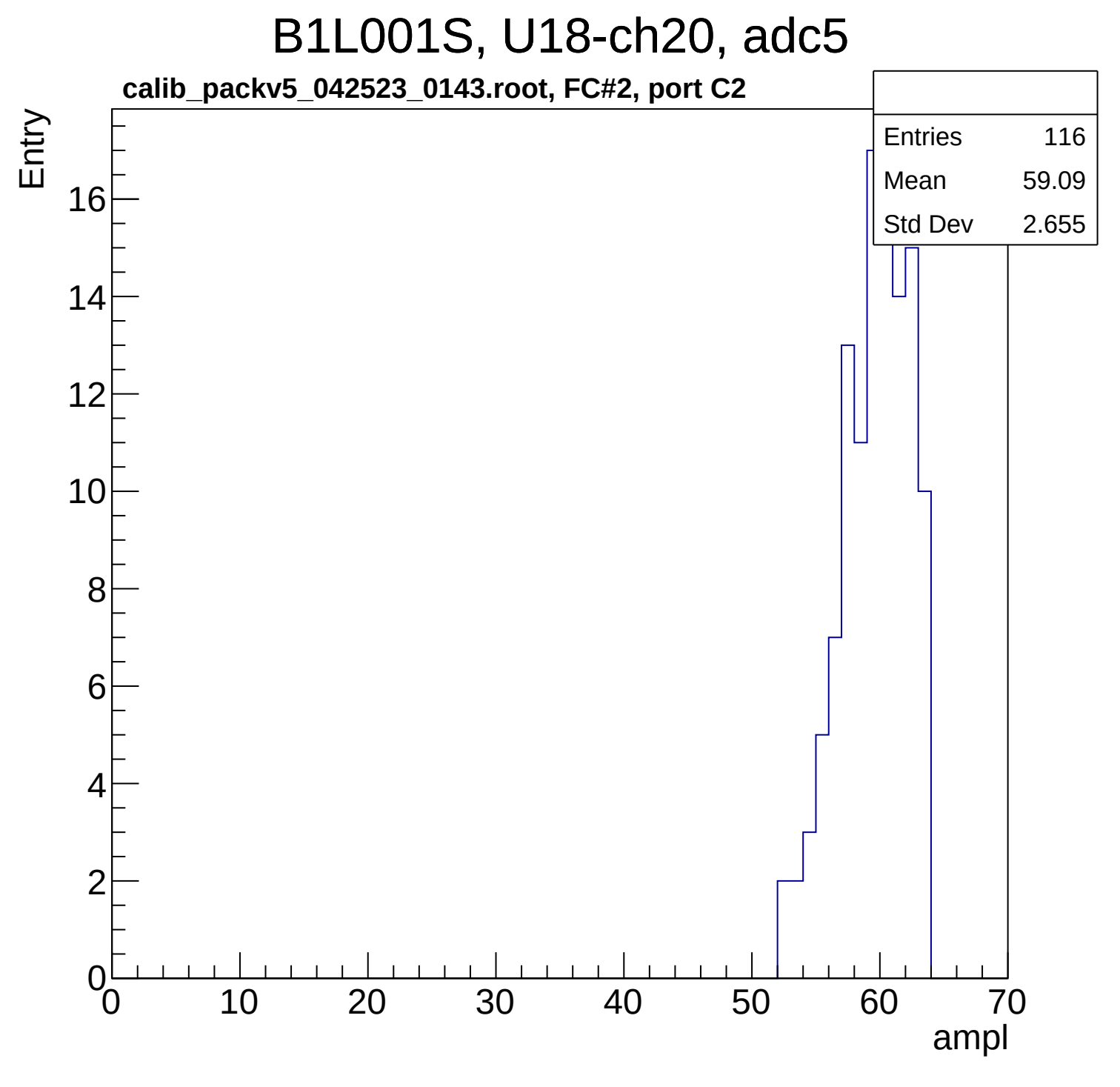

B1L001S, U18-ch20, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 131
Mean 28.73
Std Dev 2.973
Gaus mean : 29.2788
Gaus Width: 3.0347
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

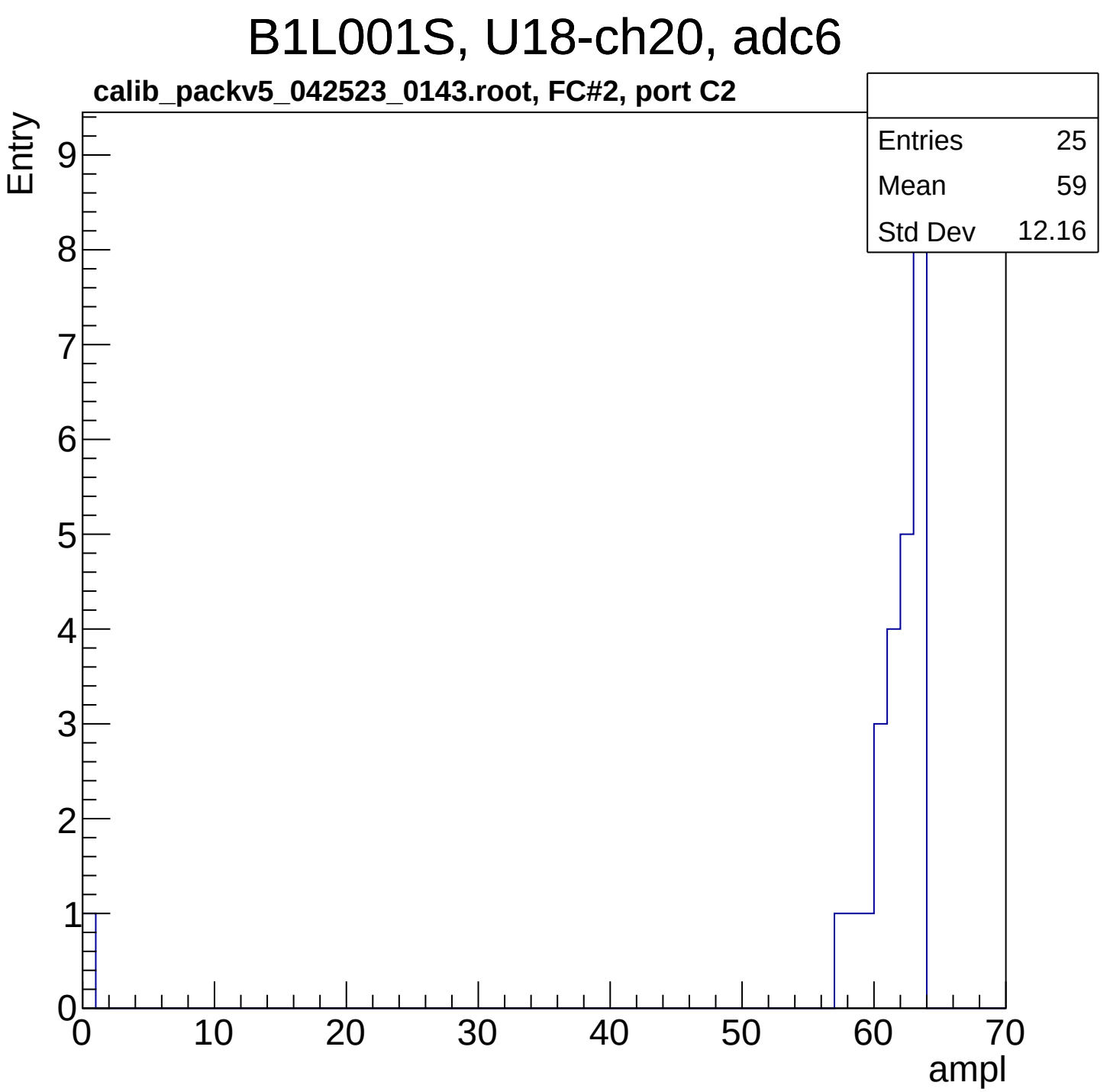

B1L001S, U18-ch20, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 108
Mean 34.75
Std Dev 2.972
Gaus mean : 35.2698
Gaus Width: 2.9488
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

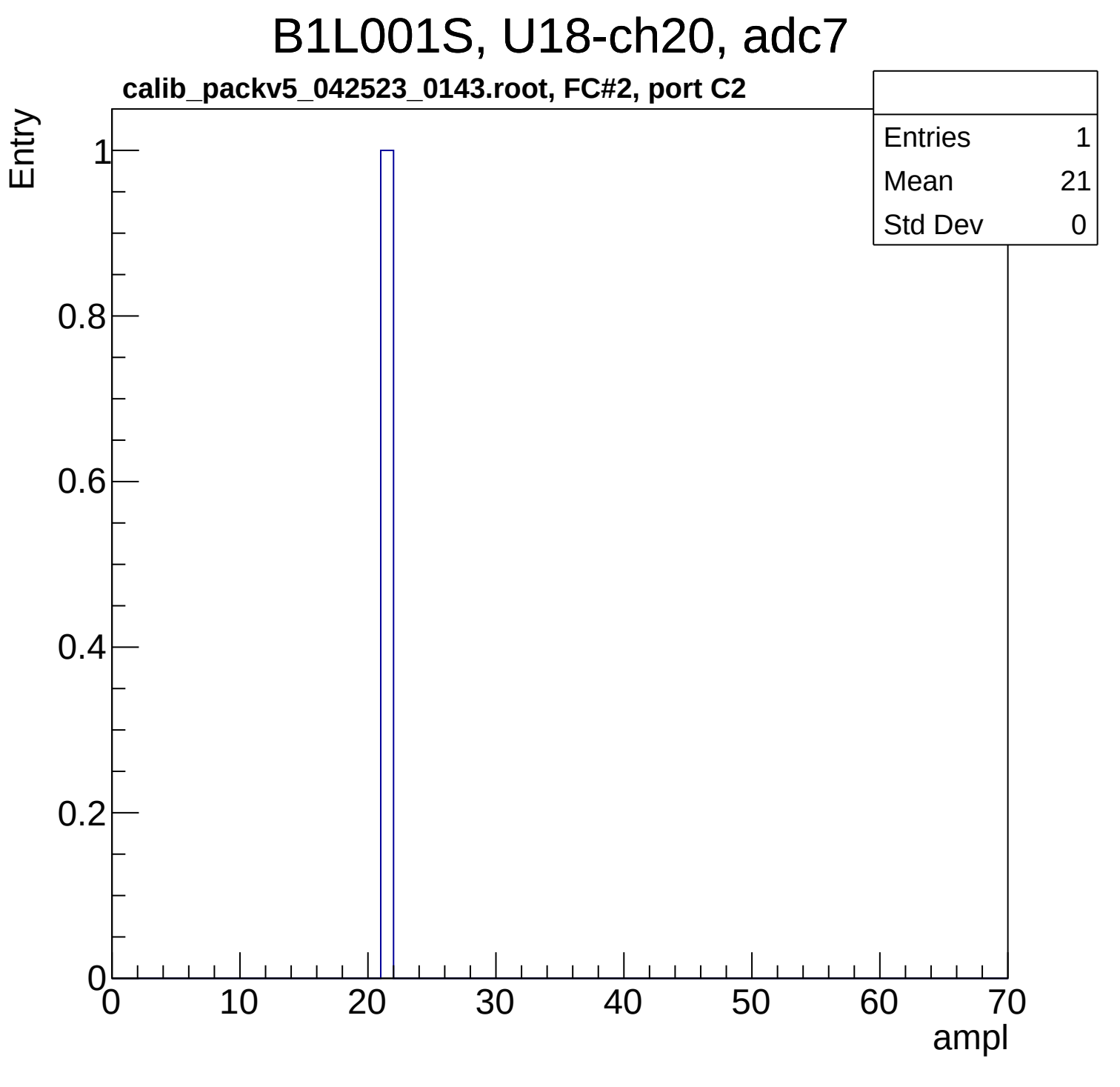

B1L001S, U18-ch20, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 149
Mean 41.36
Std Dev 3.568
Gaus mean : 41.7393
Gaus Width: 3.4965
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

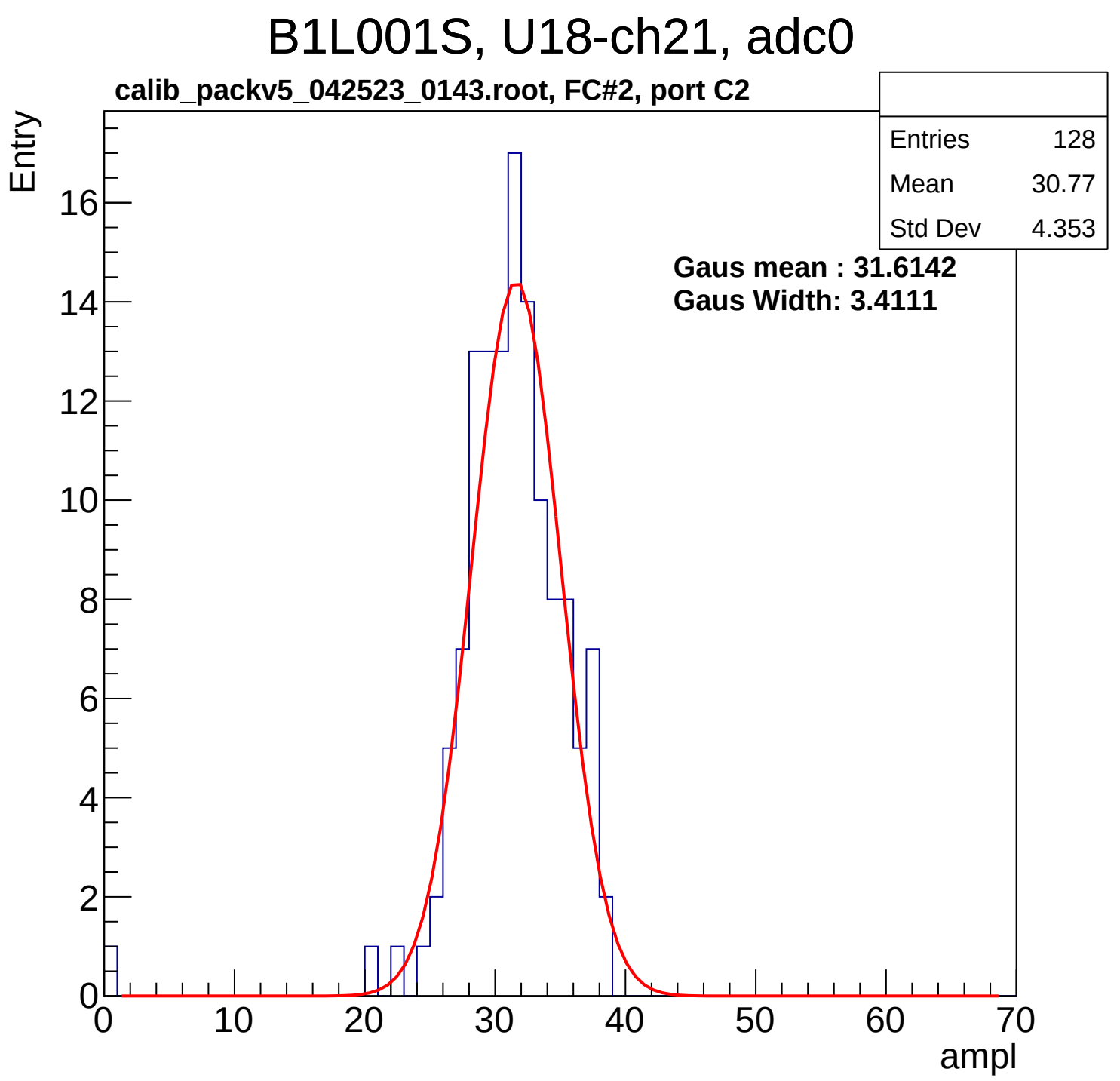

B1L001S, U18-ch20, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 112
Mean 47.62
Std Dev 3.546
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl

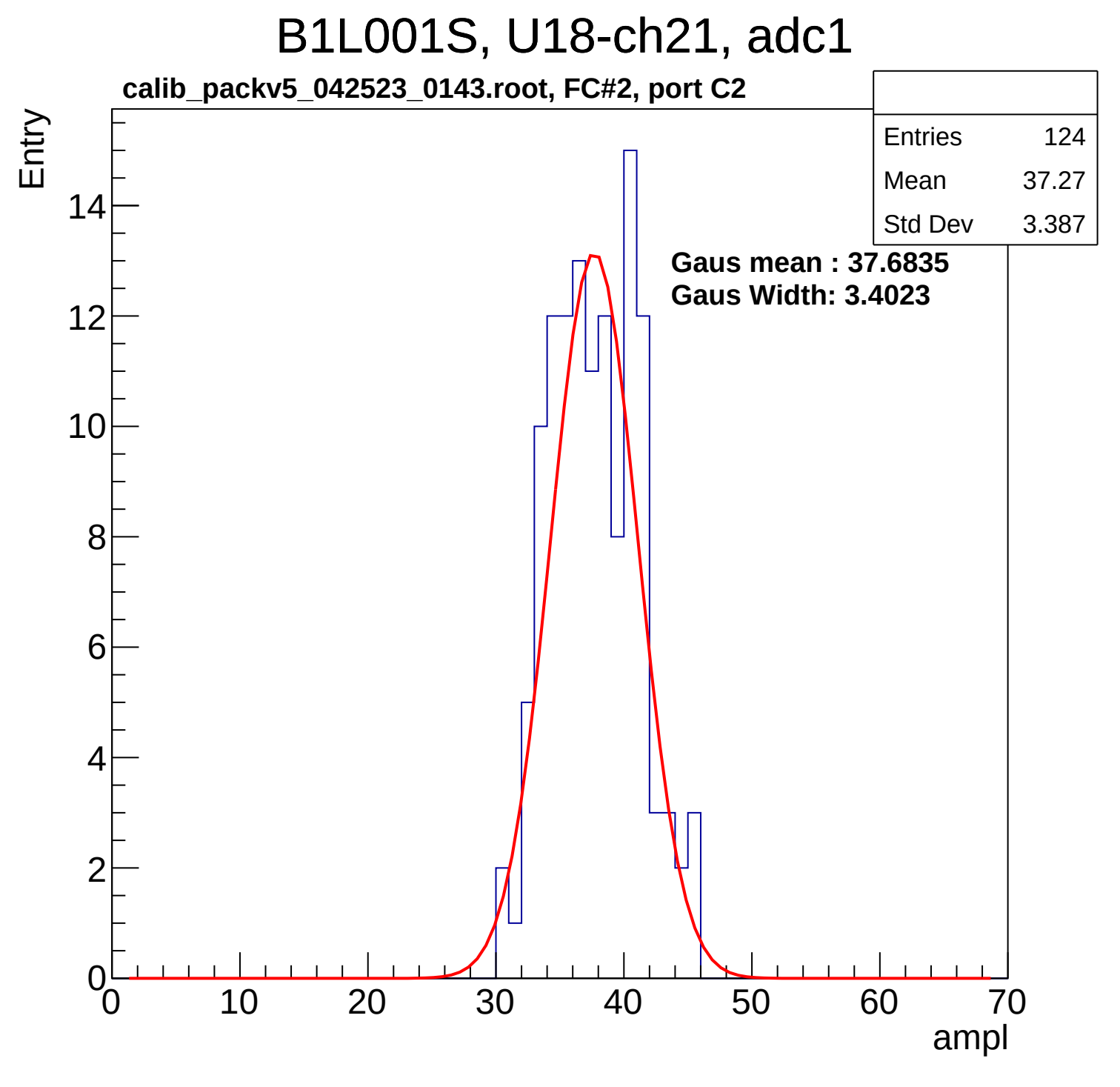

B1L001S, U18-ch20, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 122
Mean 52.83
Std Dev 5.852
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

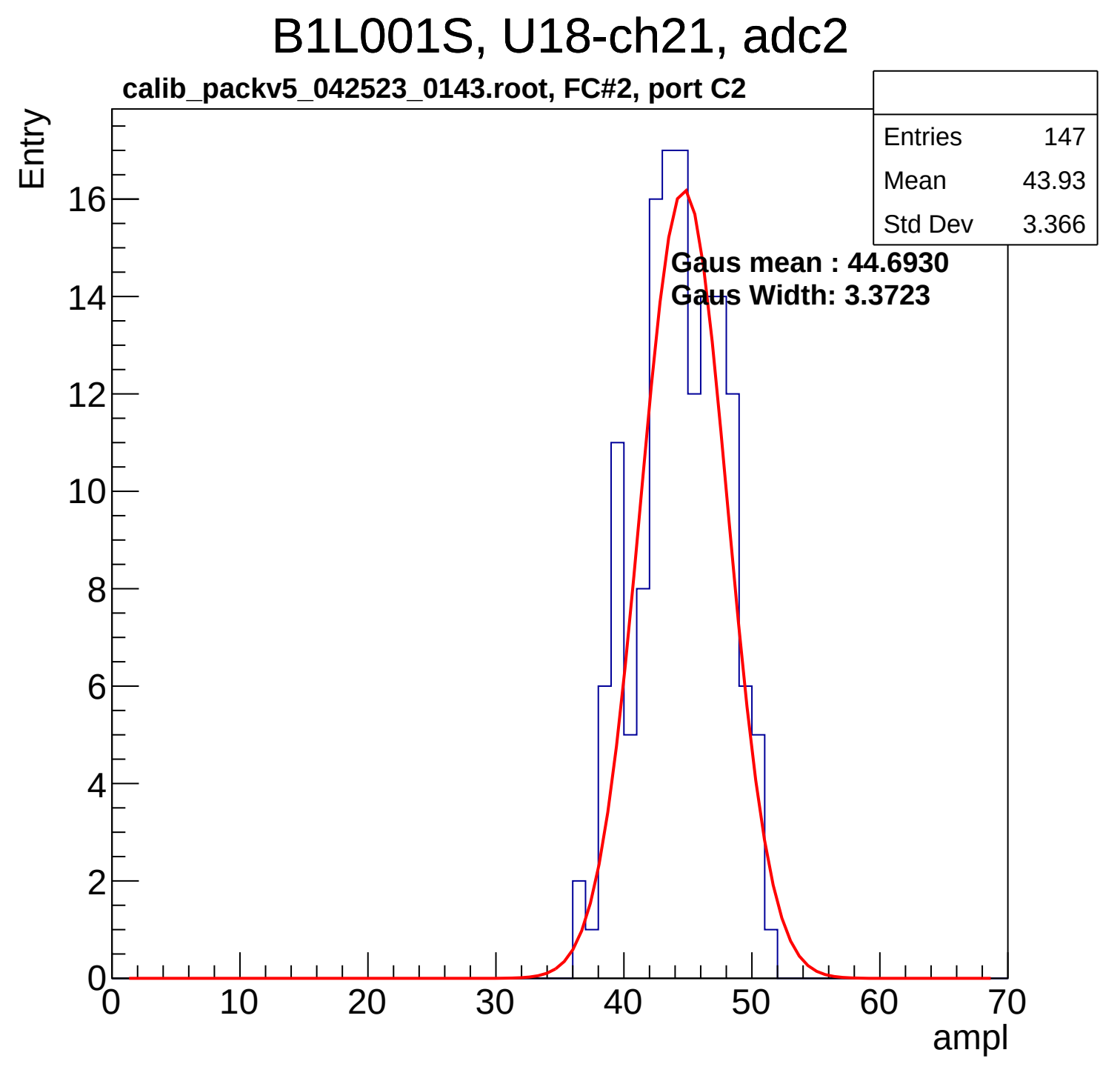

B1L001S, U18-ch20, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 116
Mean 59.09
Std Dev 2.655
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

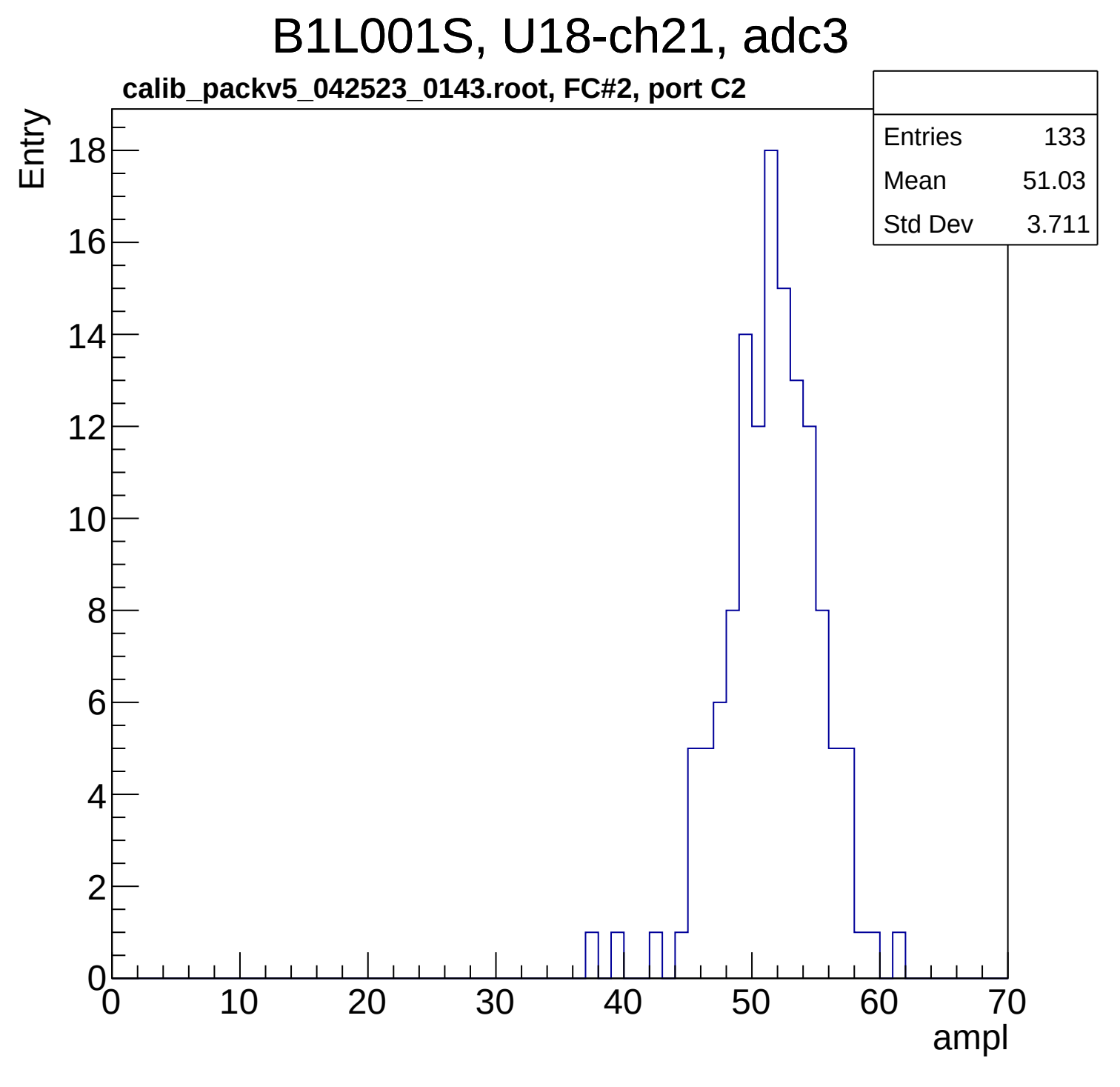

B1L001S, U18-ch20, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 25
Mean 59
Std Dev 12.16
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

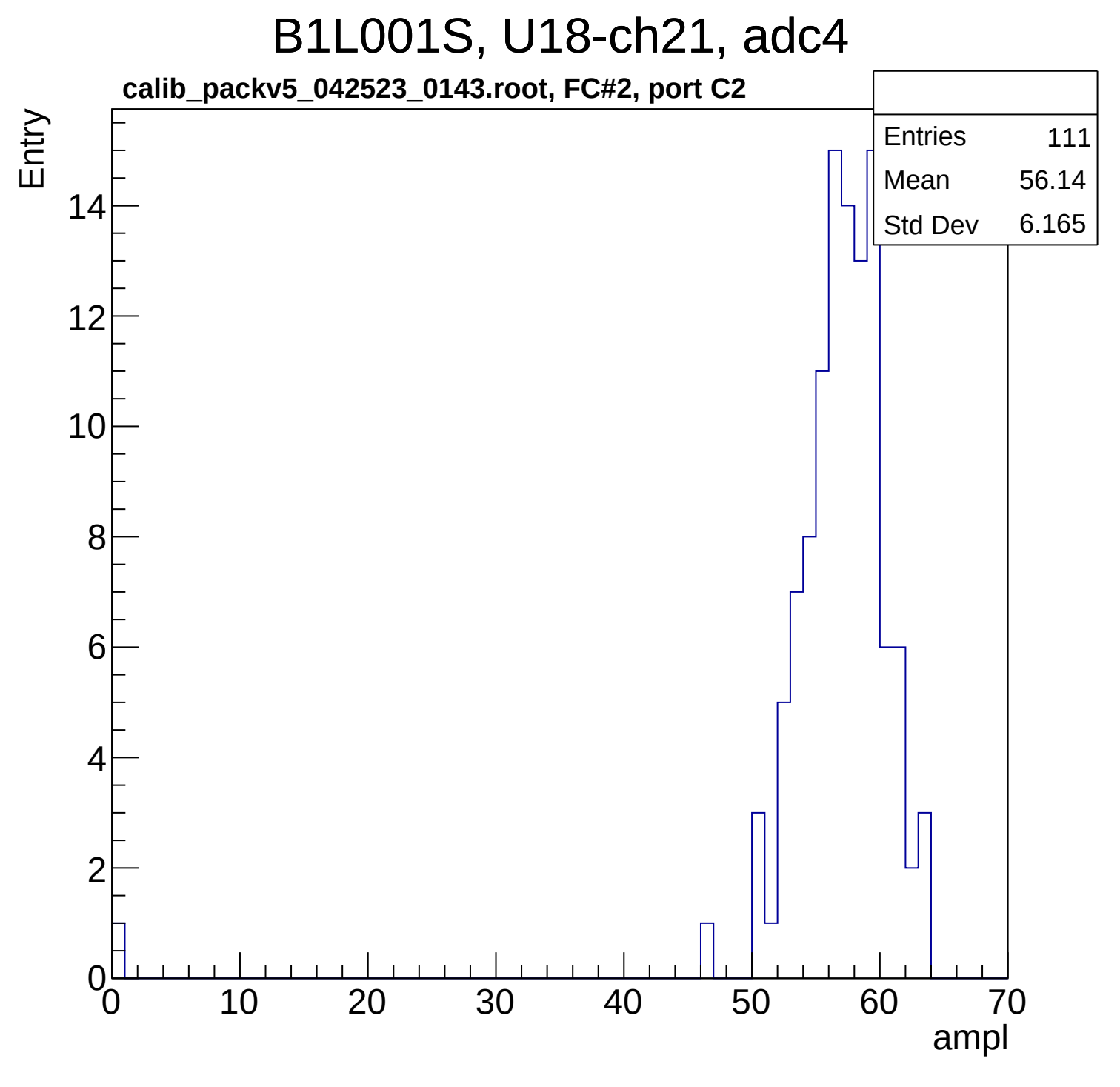

B1L001S, U18-ch20, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 21
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

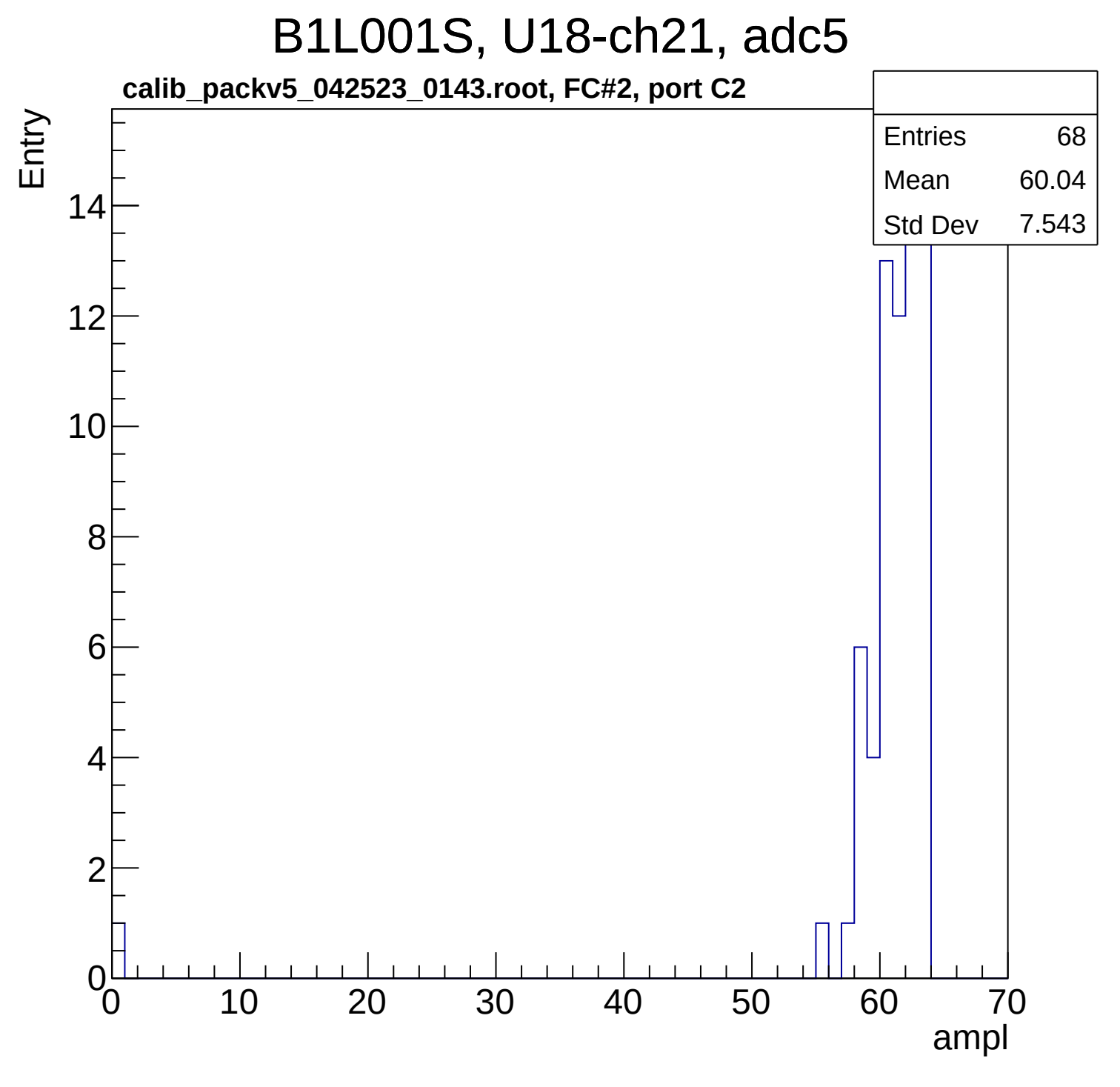

B1L001S, U18-ch21, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 128
Mean 30.77
Std Dev 4.353
Gaus mean : 31.6142
Gaus Width: 3.4111
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

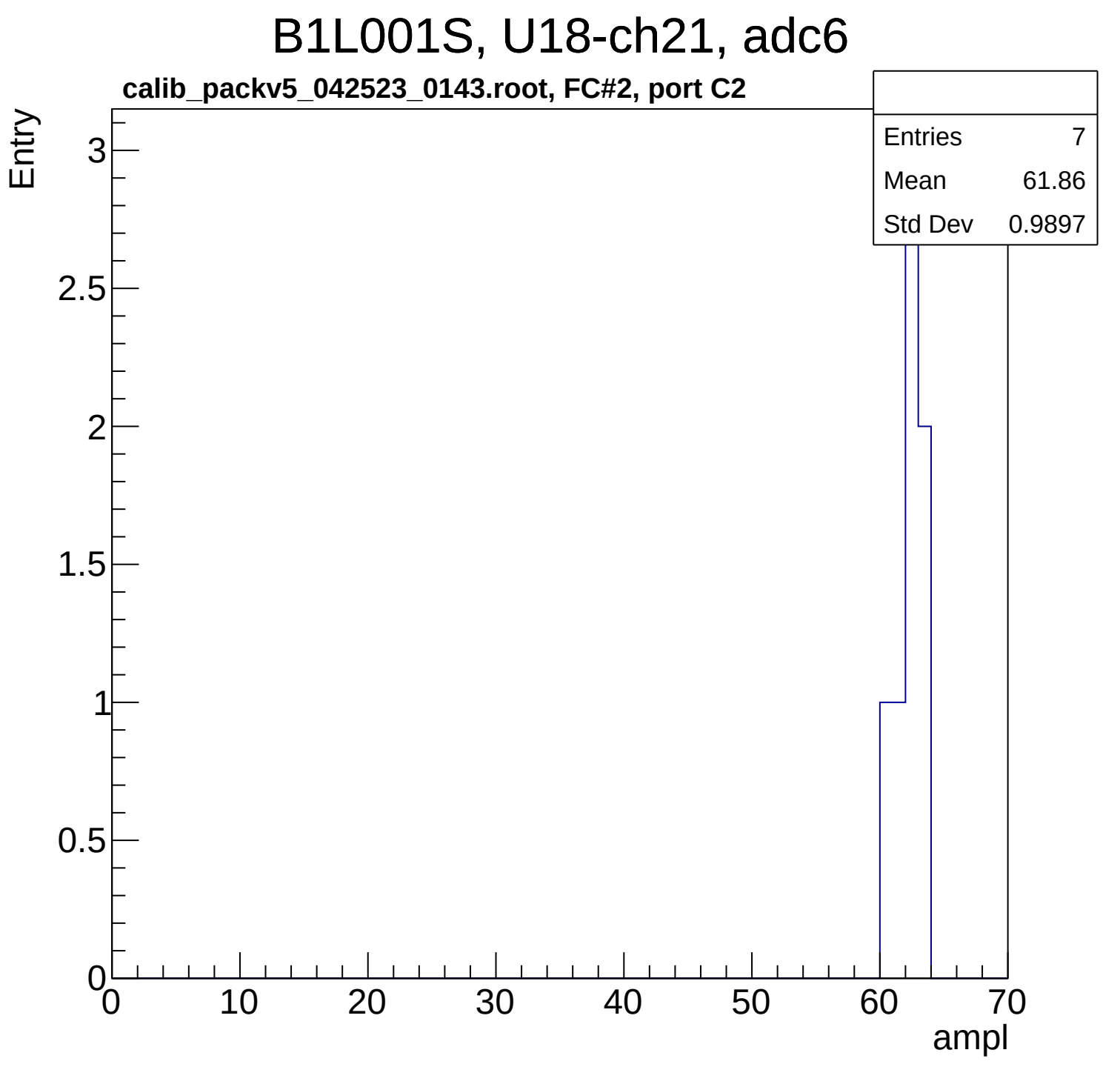

B1L001S, U18-ch21, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 124
Mean 37.27
Std Dev 3.387
Gaus mean : 37.6835
Gaus Width: 3.4023
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

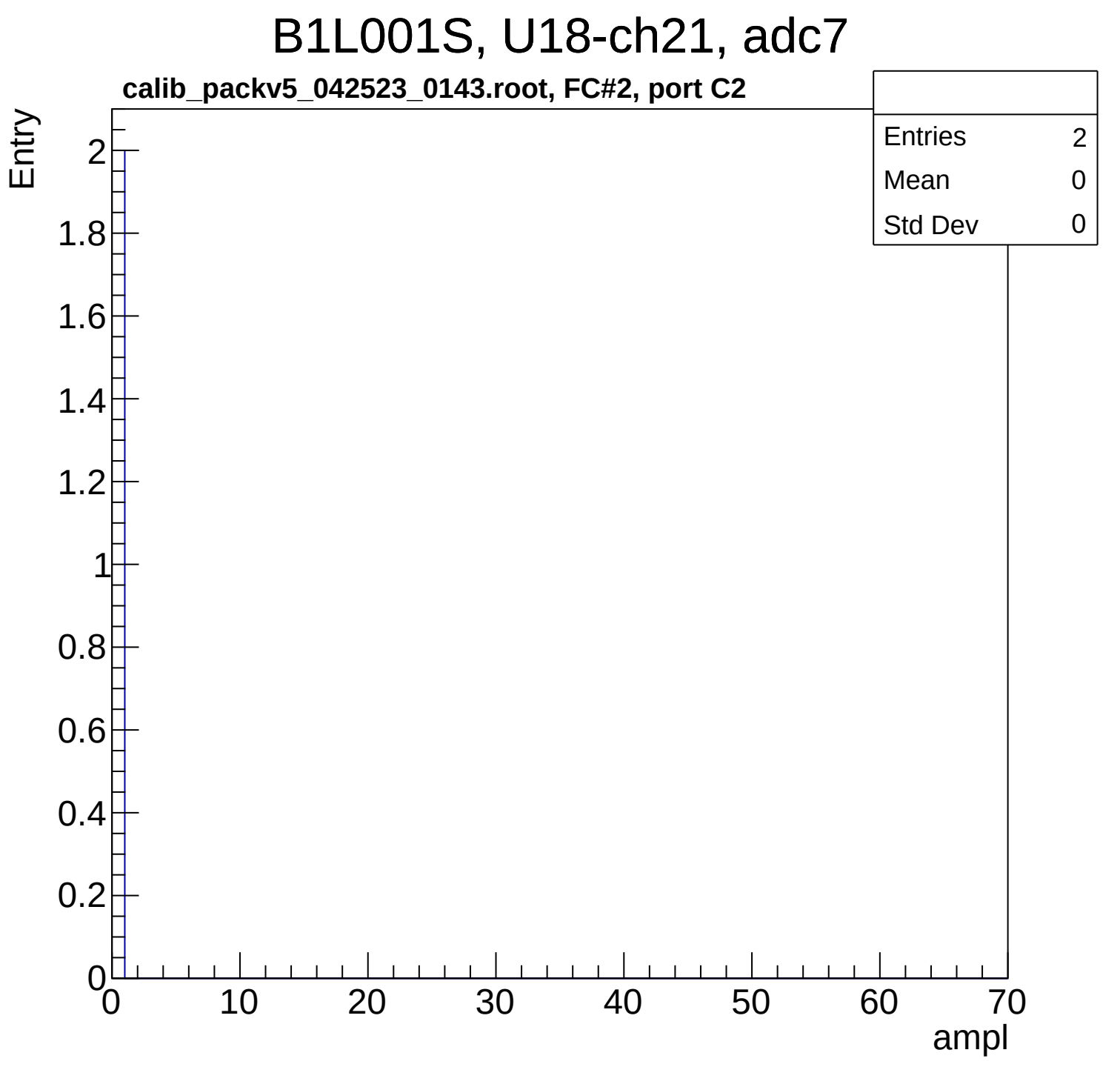

B1L001S, U18-ch21, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 147
Mean 43.93
Std Dev 3.366
Gaus mean : 44.6930
Gaus Width: 3.3723
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

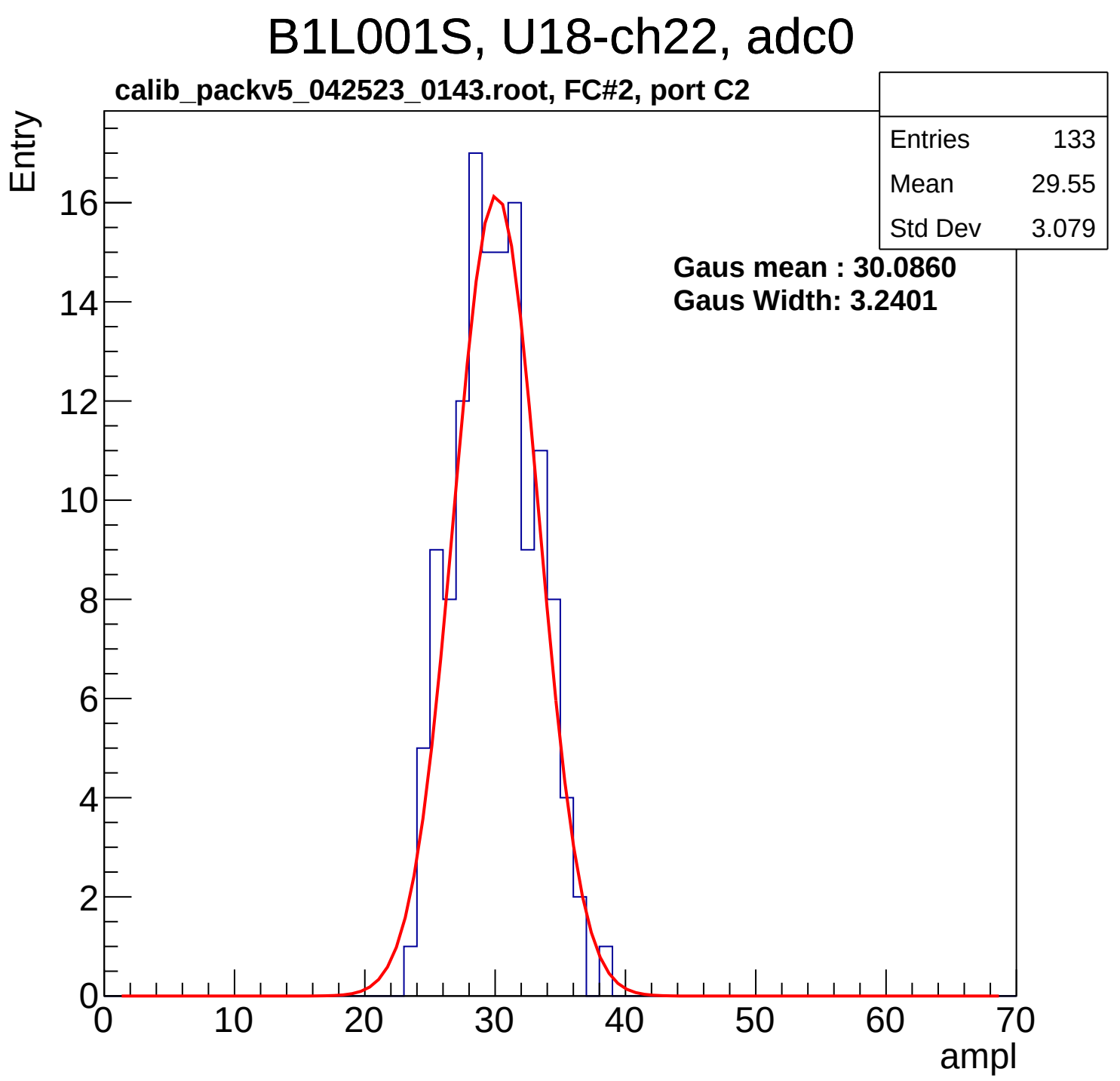

B1L001S, U18-ch21, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 133
Mean 51.03
Std Dev 3.711
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

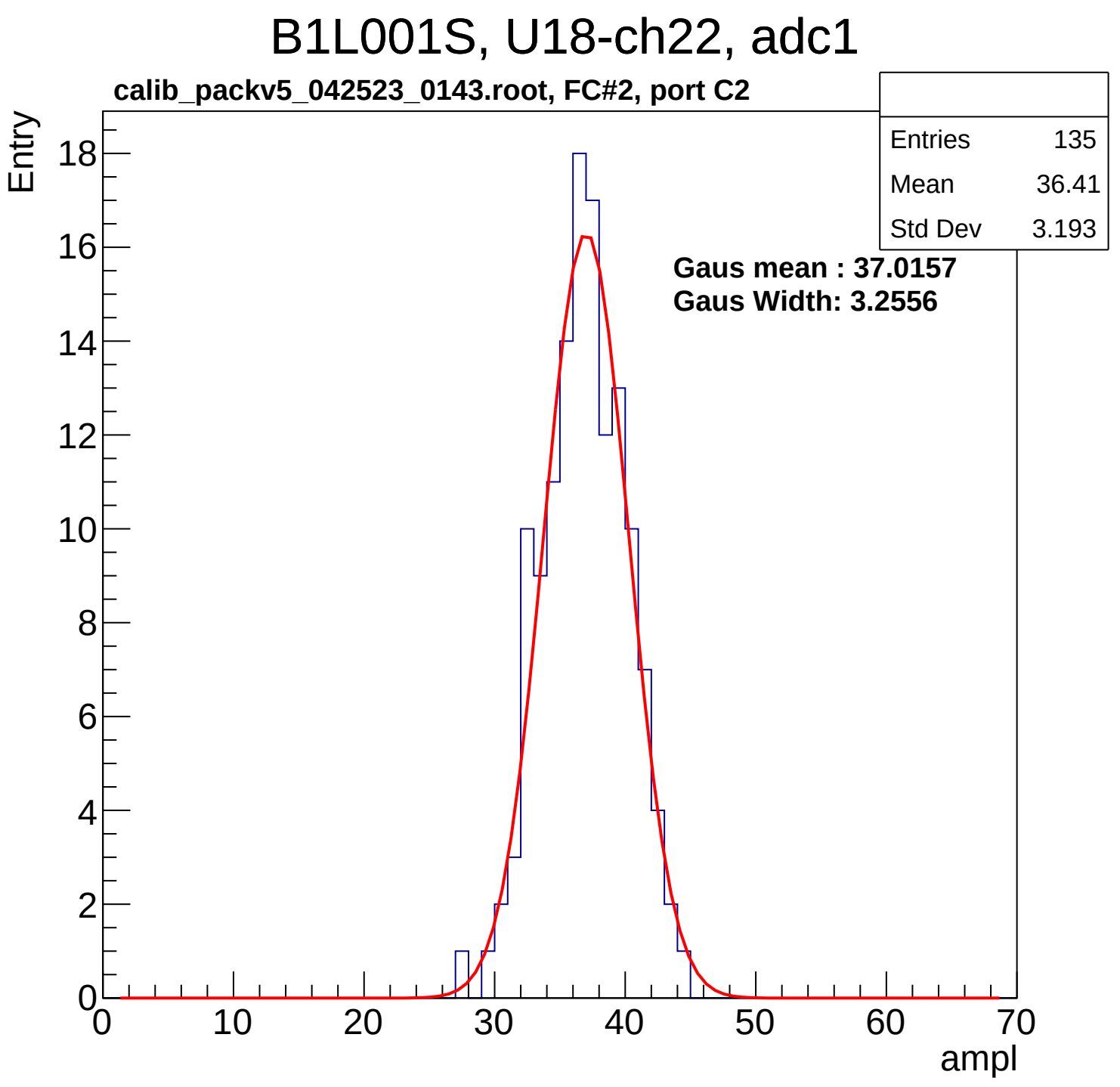

B1L001S, U18-ch21, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 111
Mean 56.14
Std Dev 6.165
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

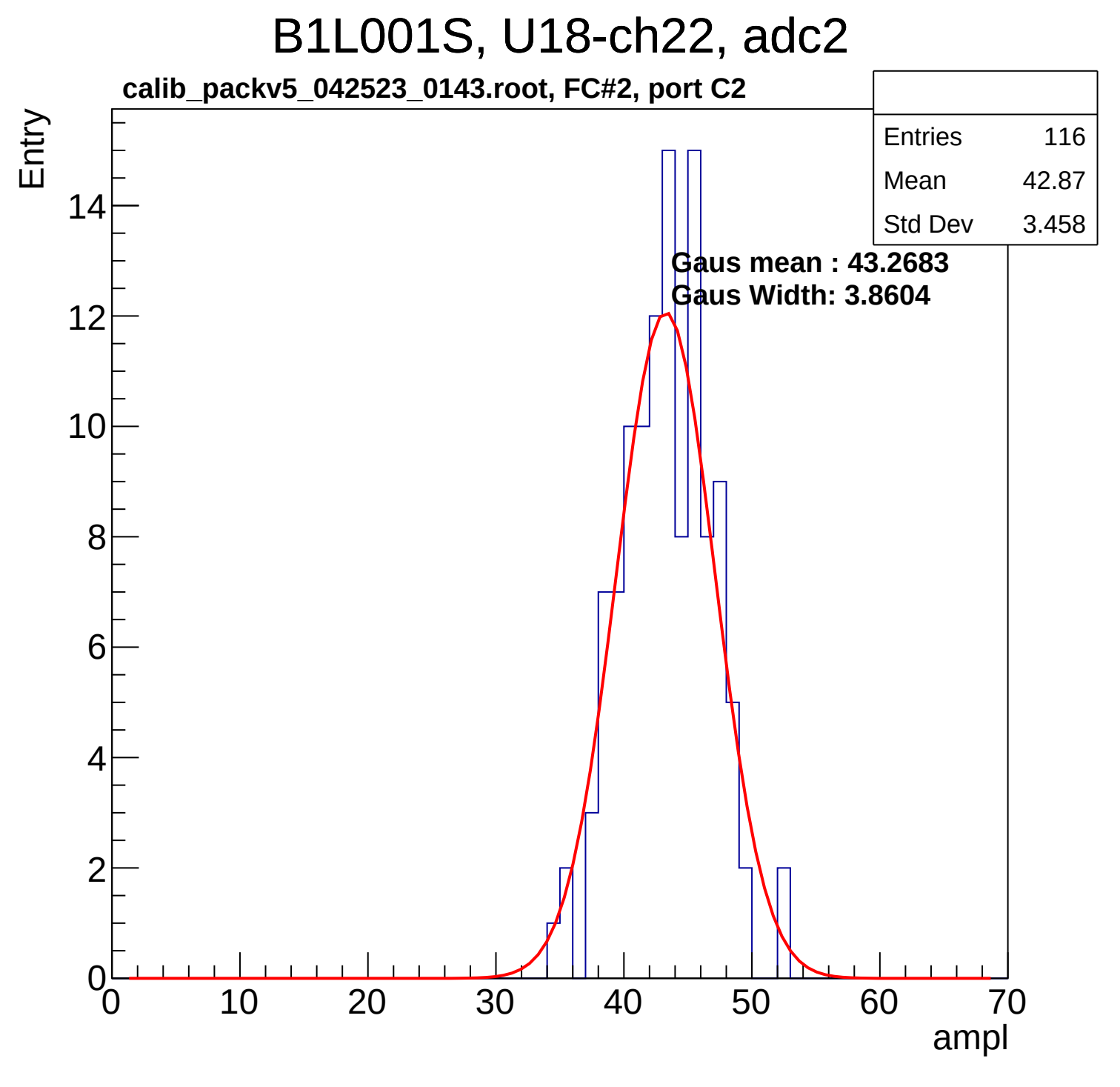

B1L001S, U18-ch21, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 68
Mean 60.04
Std Dev 7.543
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl

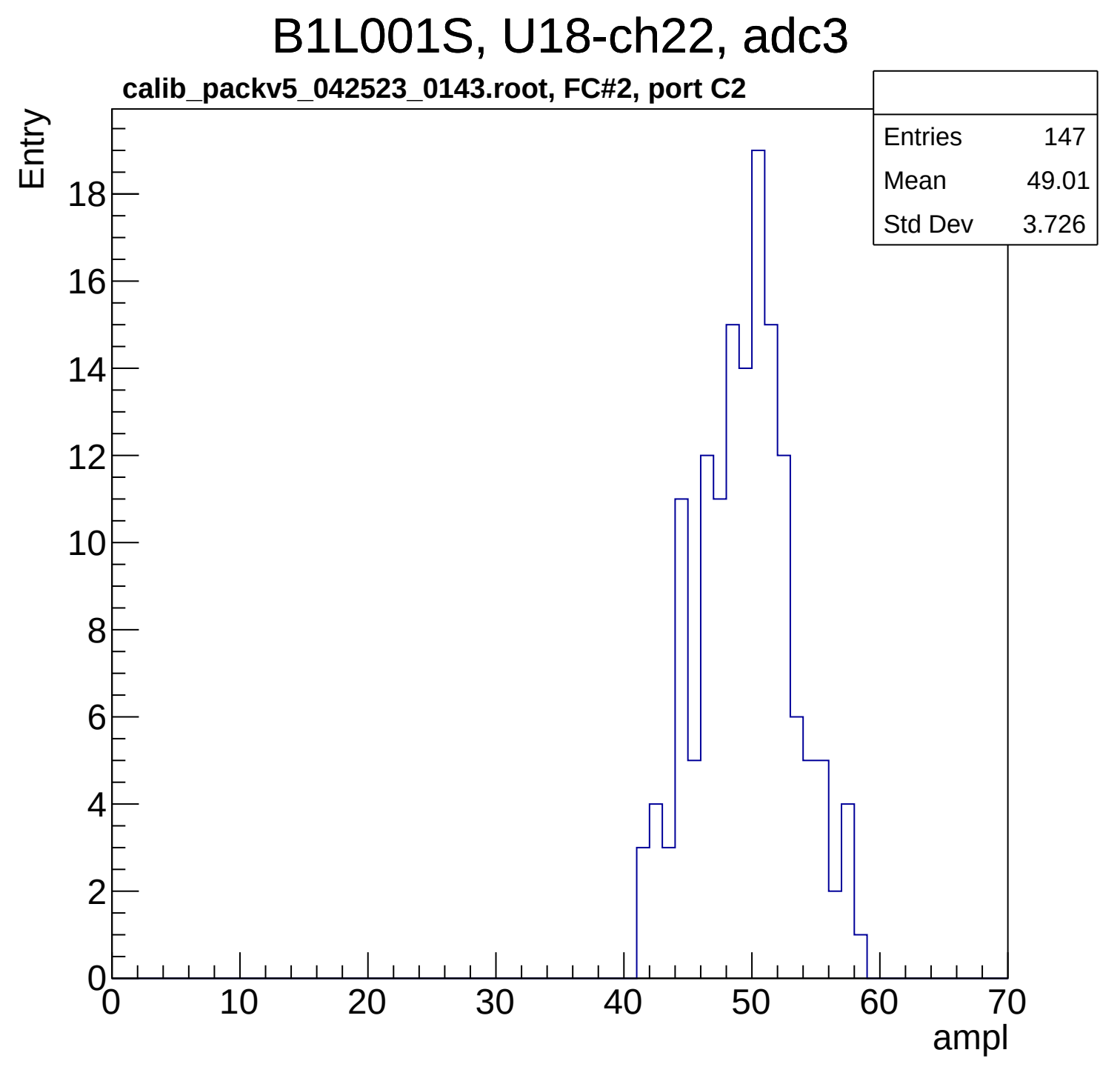

B1L001S, U18-ch21, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 7
Mean 61.86
Std Dev 0.9897
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

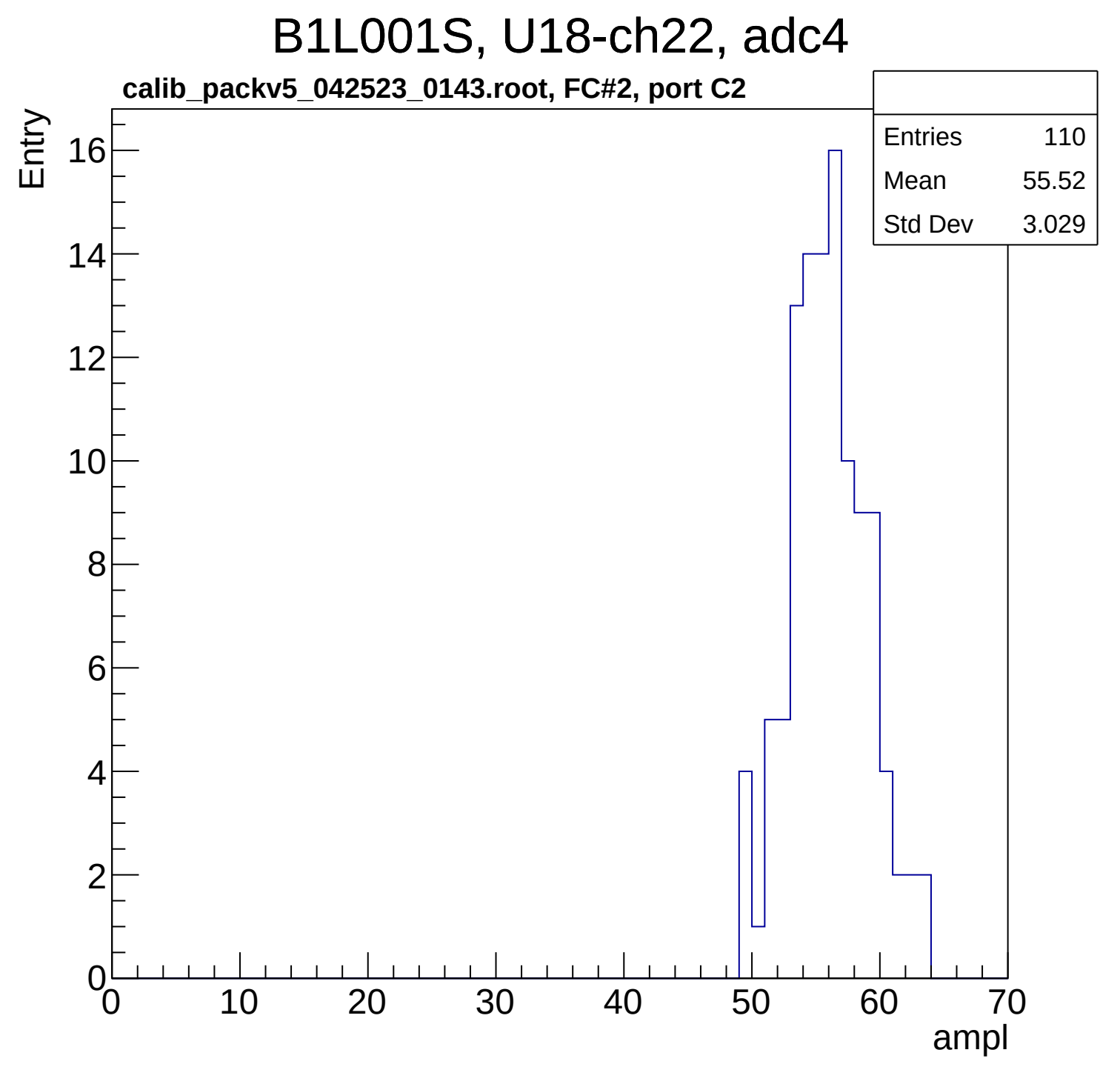

B1L001S, U18-ch21, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 0
Std Dev 0
Entry
2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

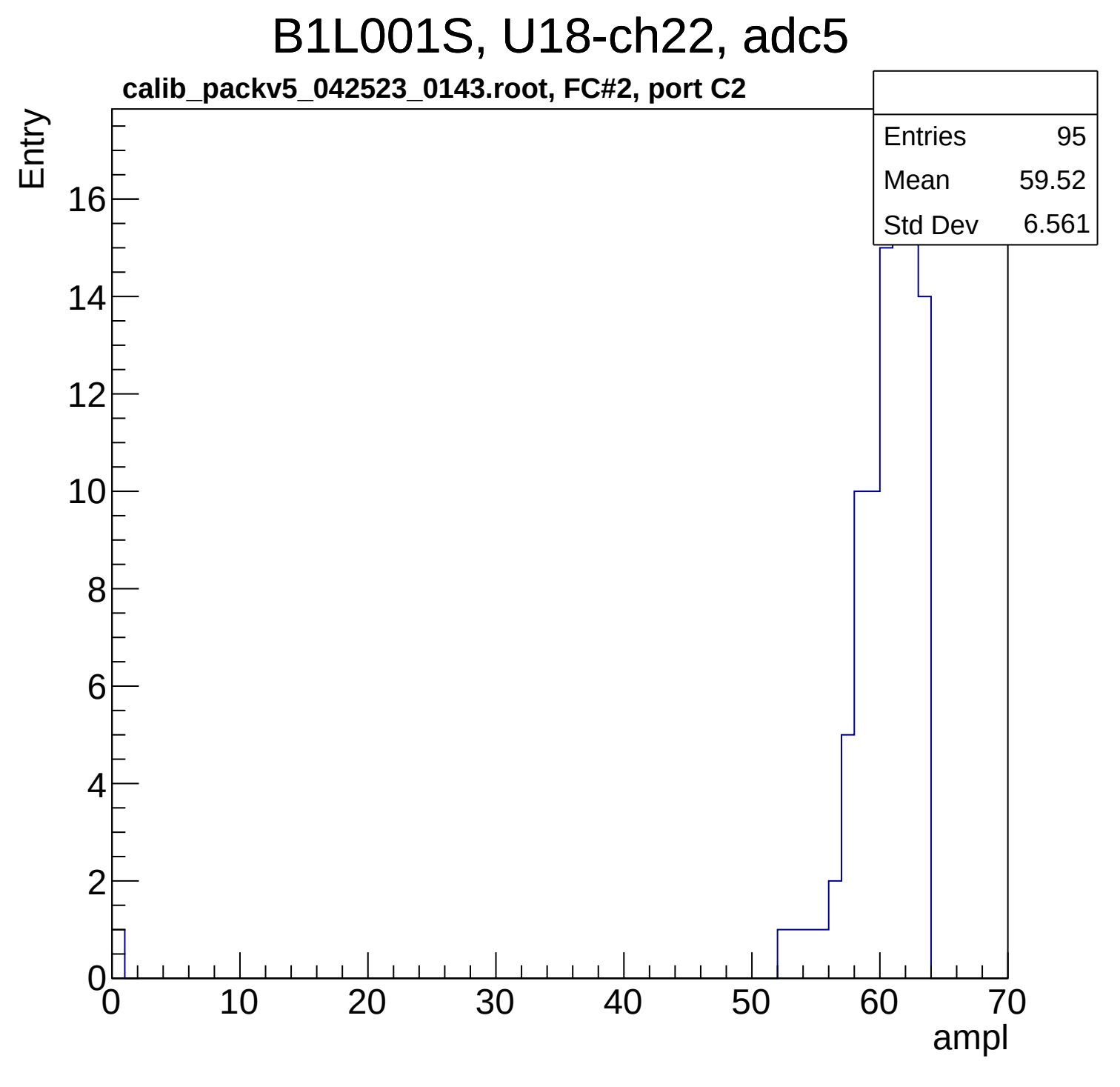

B1L001S, U18-ch22, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 133
Mean 29.55
Std Dev 3.079
Gaus mean : 30.0860
Gaus Width: 3.2401
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

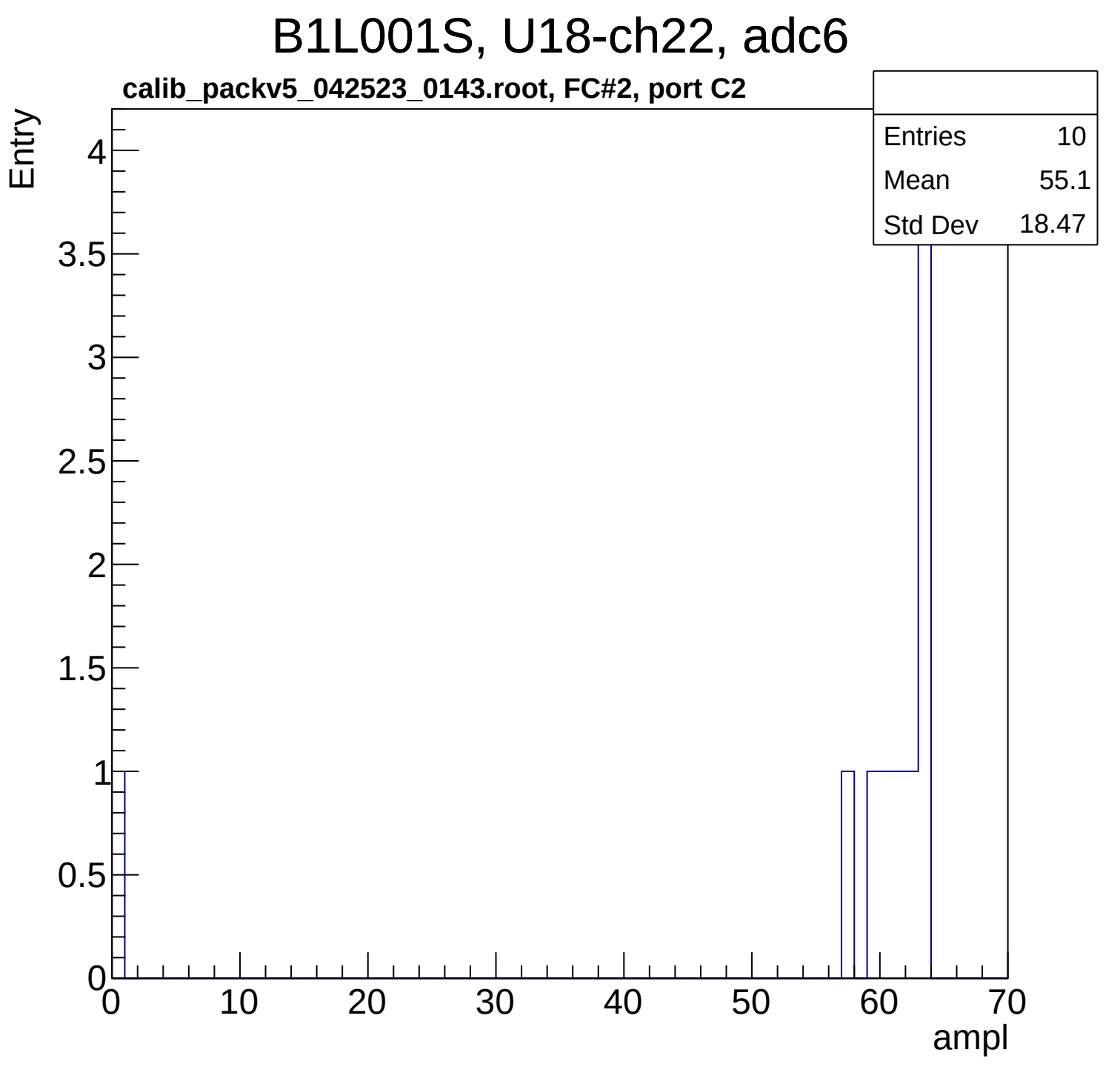

B1L001S, U18-ch22, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 135
Mean 36.41
Std Dev 3.193
Gaus mean : 37.0157
Gaus Width: 3.2556
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

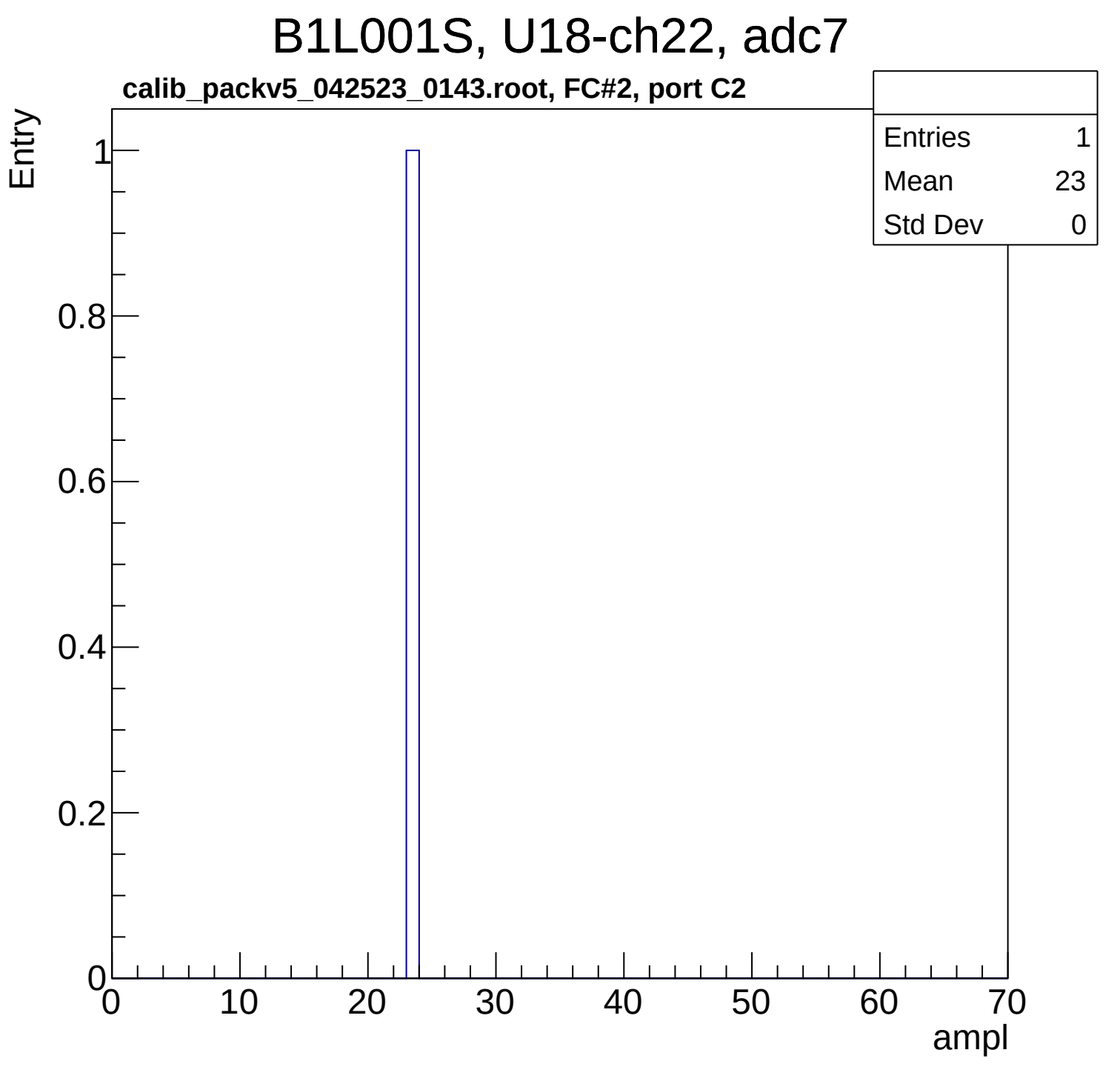

B1L001S, U18-ch22, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 116
Mean 42.87
Std Dev 3.458
Gaus mean : 43.2683
Gaus Width: 3.8604
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

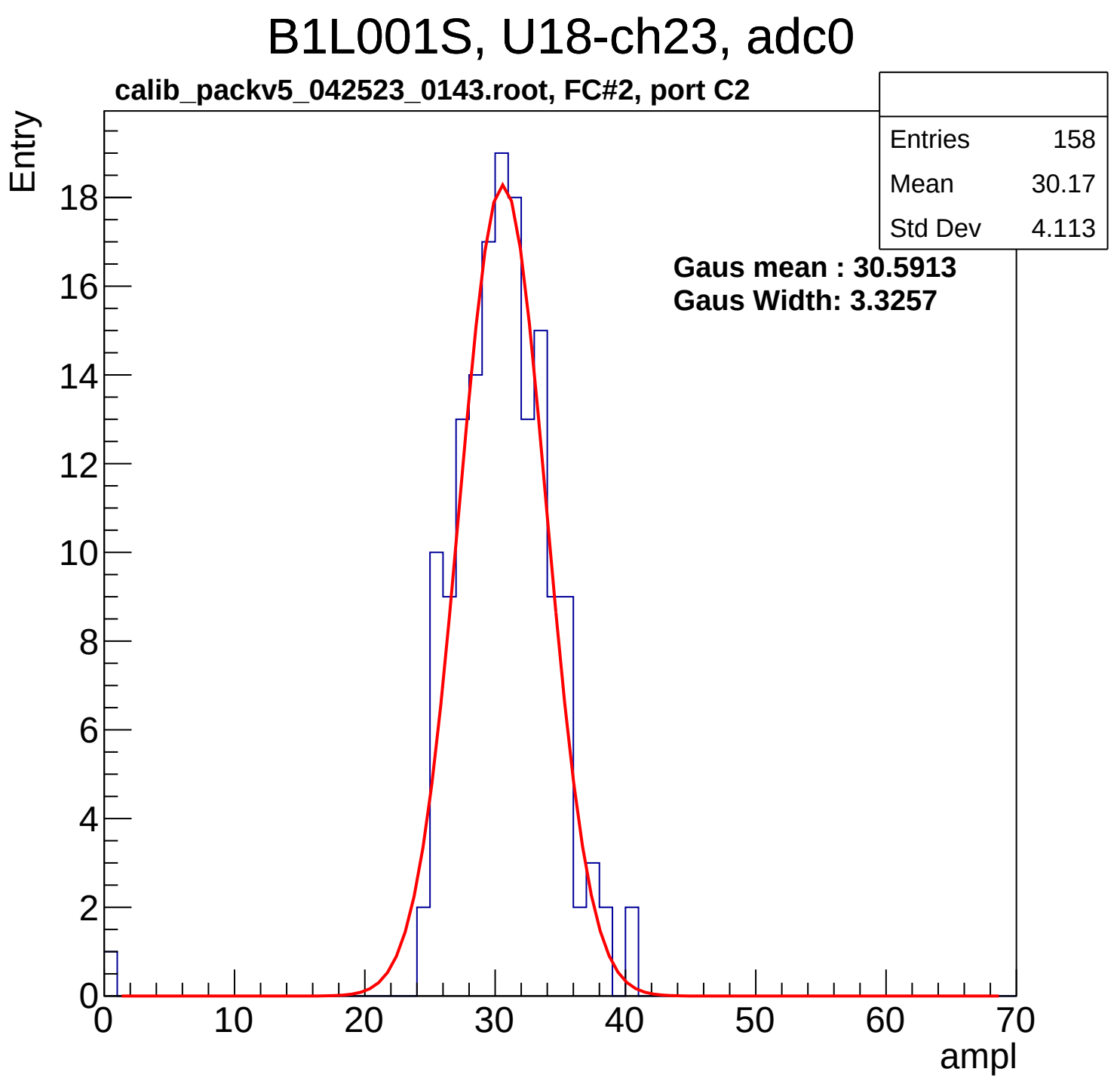

B1L001S, U18-ch22, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 147
Mean 49.01
Std Dev 3.726
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

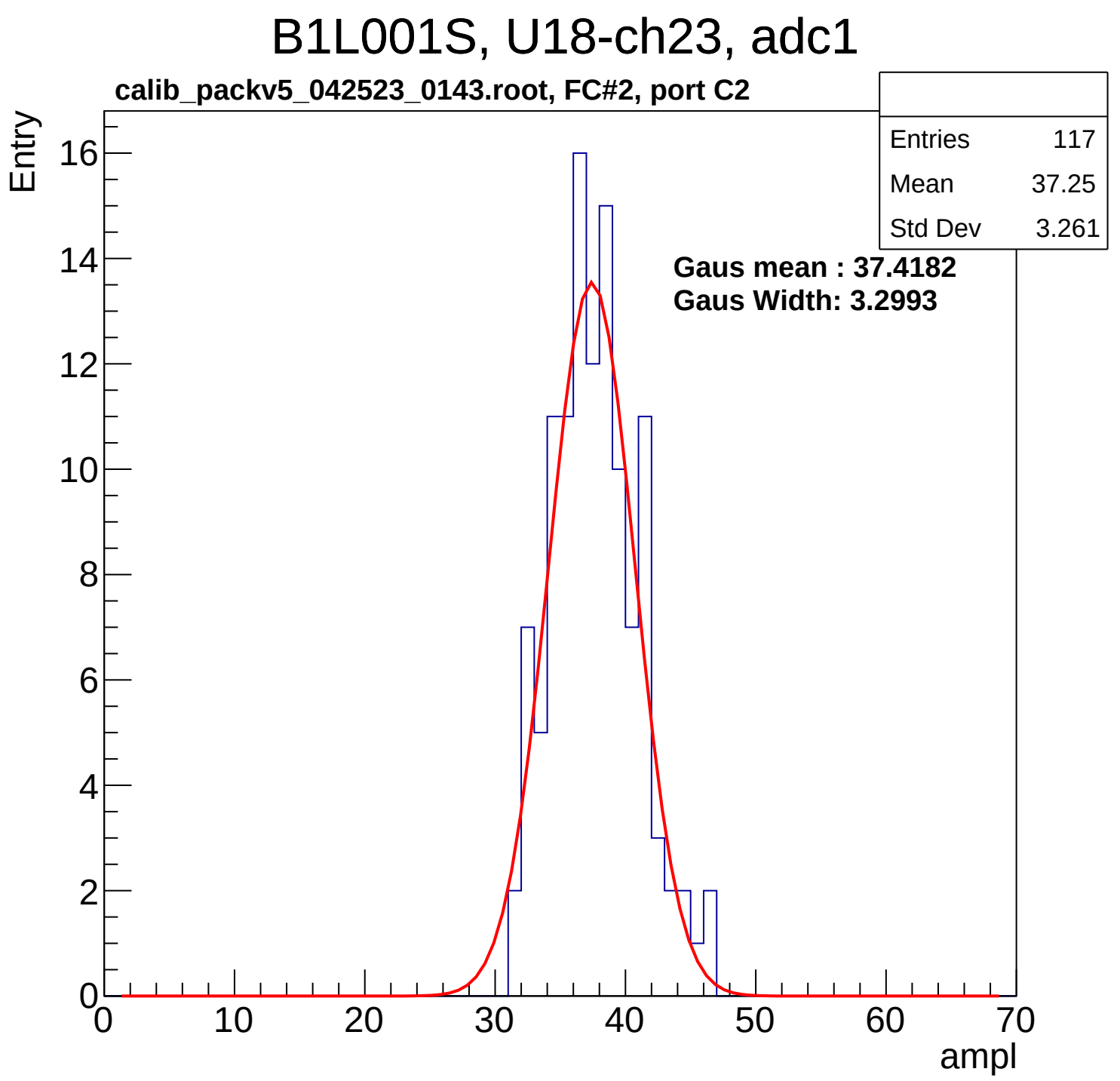

B1L001S, U18-ch22, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 110
Mean 55.52
Std Dev 3.029
Entry
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl

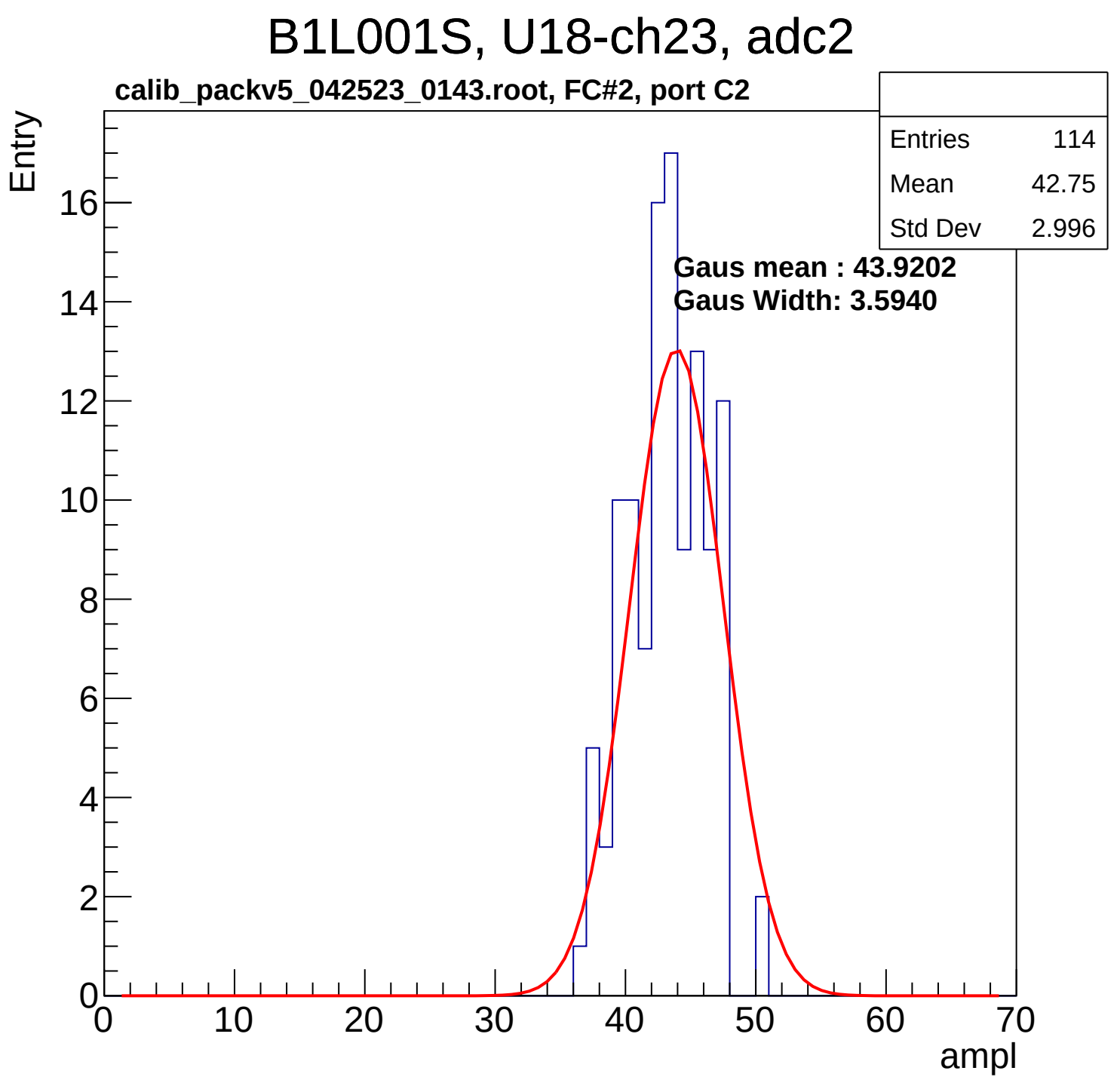

B1L001S, U18-ch22, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 95
Mean 59.52
Std Dev 6.561
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

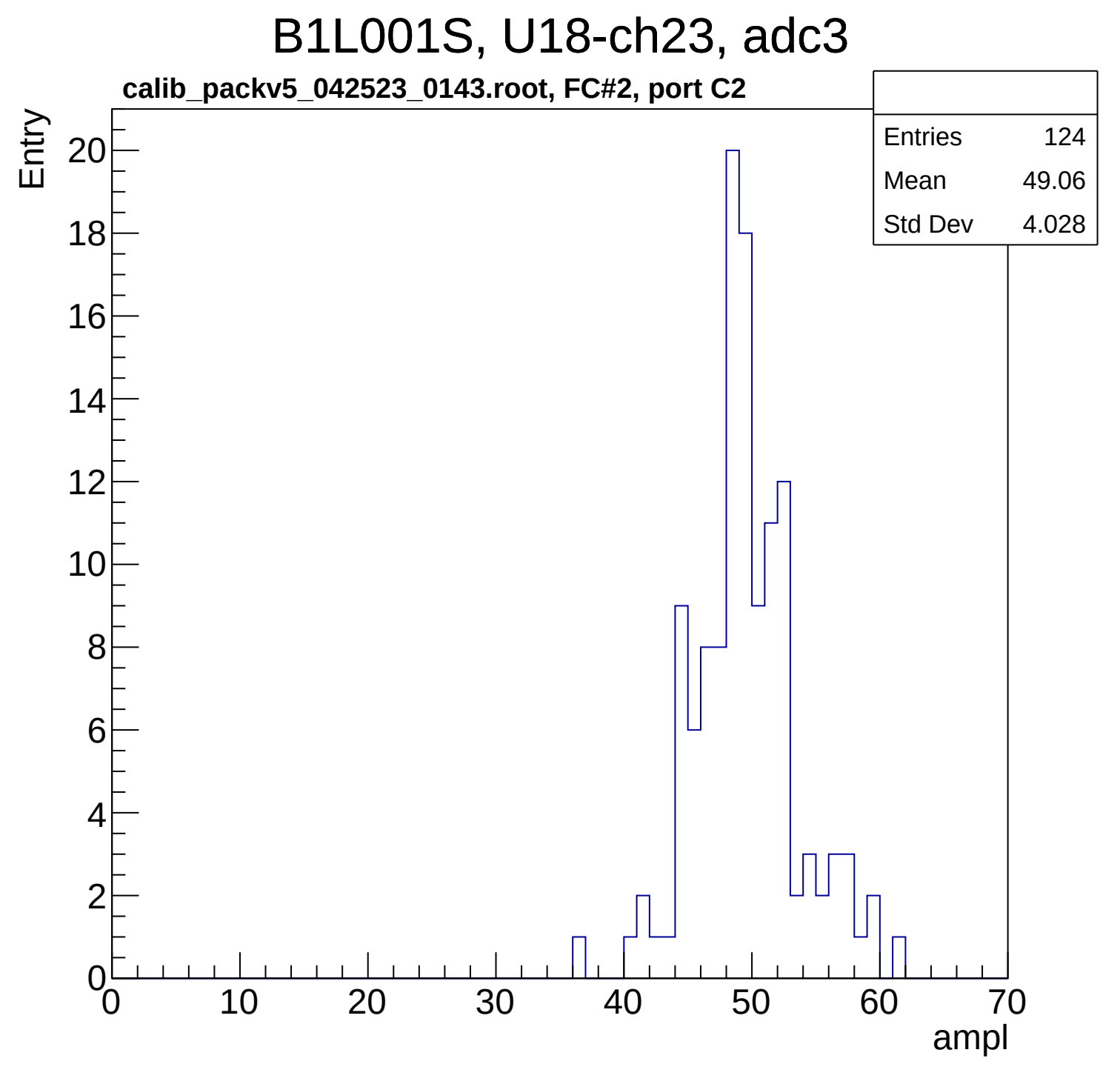

B1L001S, U18-ch22, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 10
Mean 55.1
Std Dev 18.47
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

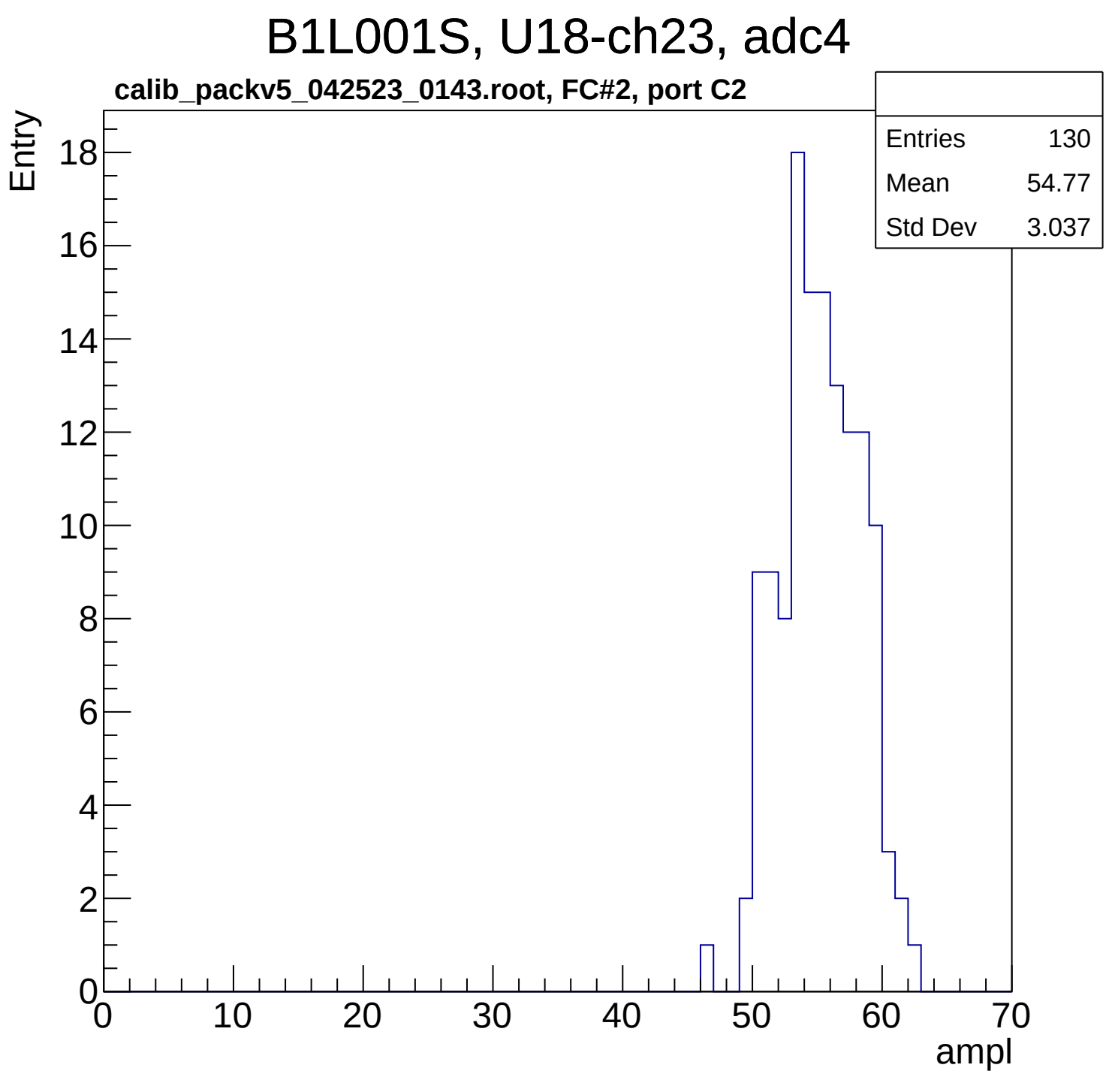

B1L001S, U18-ch22, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 23
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

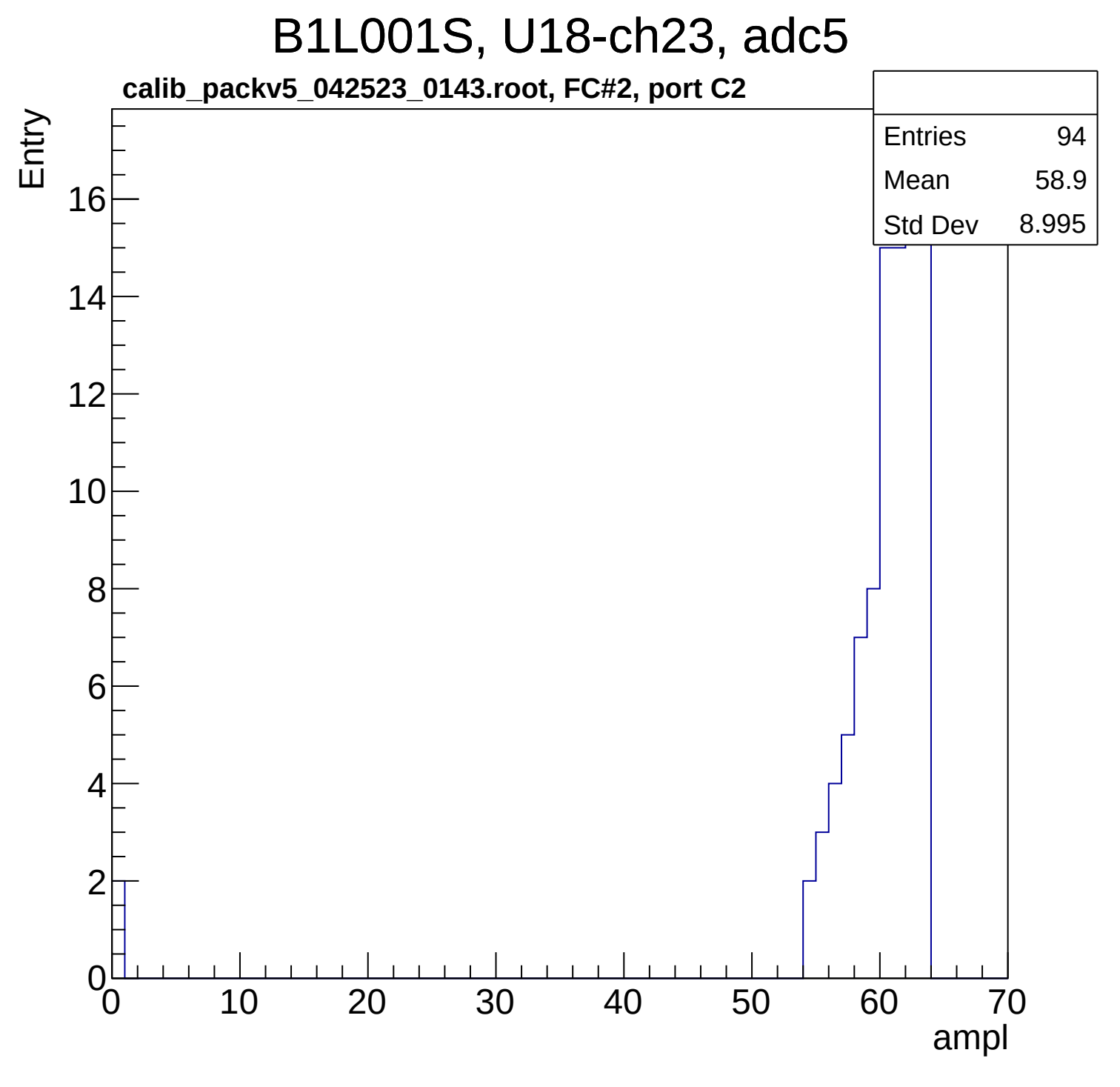

B1L001S, U18-ch23, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 158
Mean 30.17
Std Dev 4.113
Gaus mean : 30.5913
Gaus Width: 3.3257
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

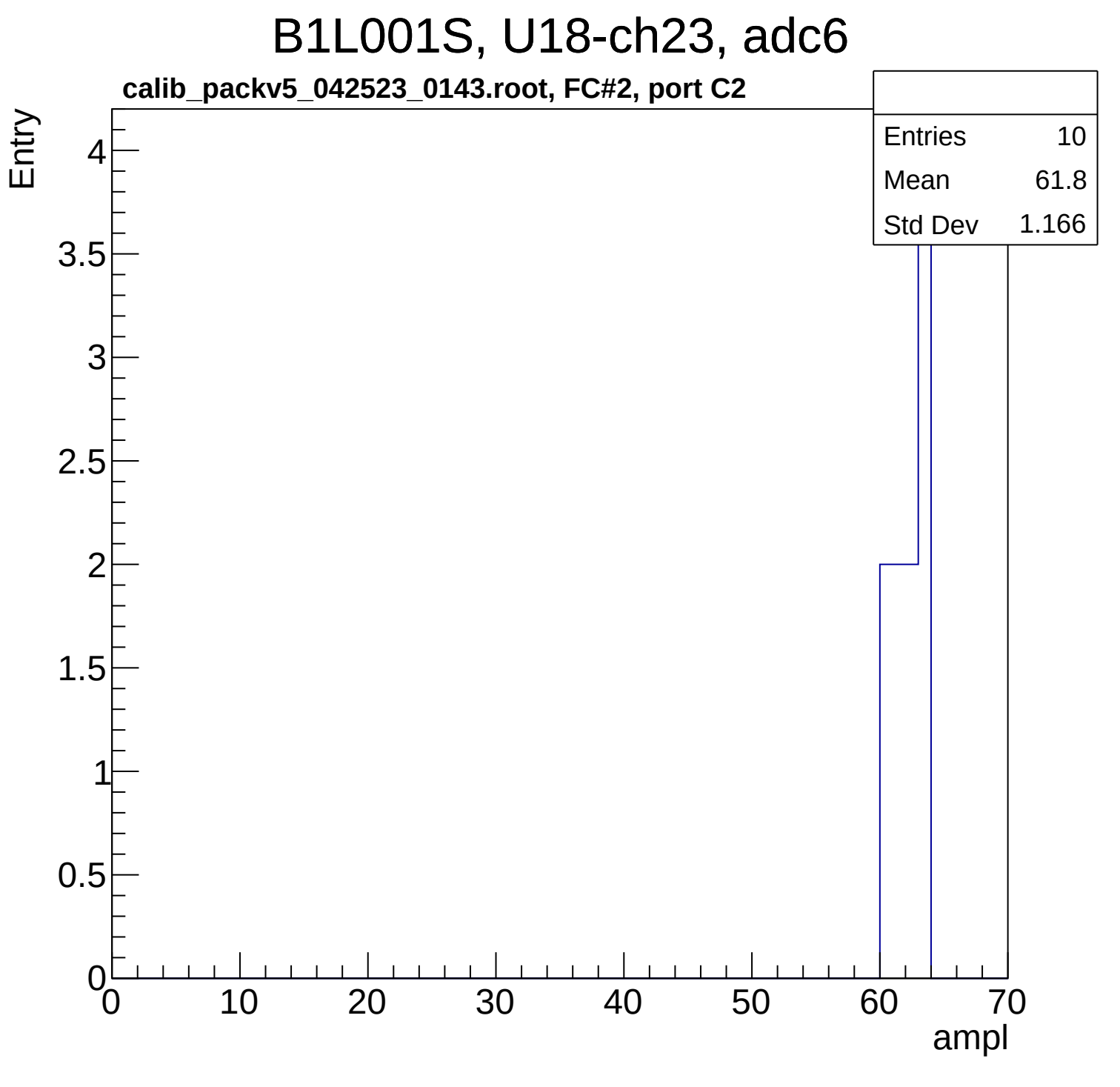

B1L001S, U18-ch23, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 117
Mean 37.25
Std Dev 3.261
Gaus mean : 37.4182
Gaus Width: 3.2993
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

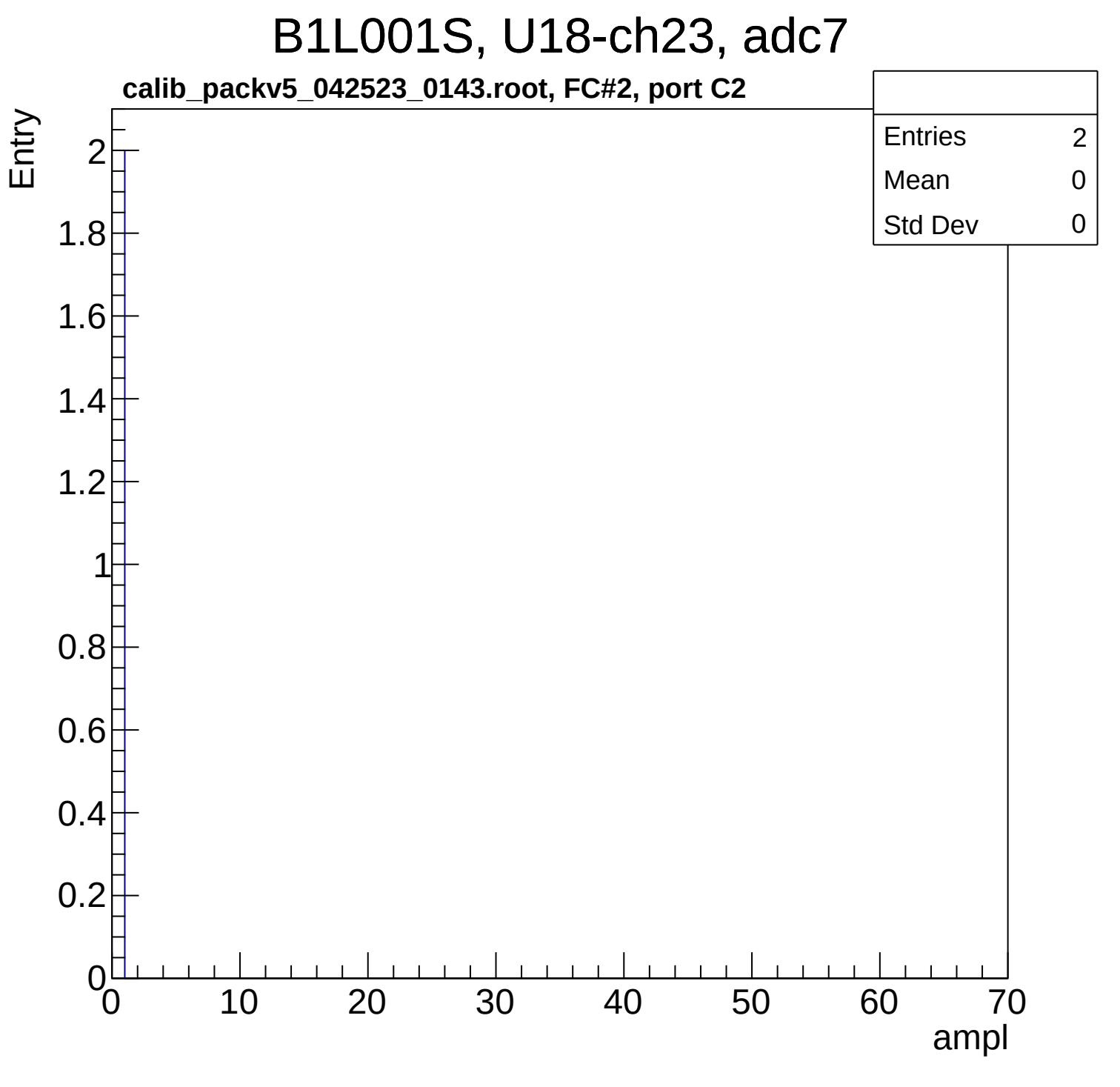

B1L001S, U18-ch23, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 114
Mean 42.75
Std Dev 2.996
Gaus mean : 43.9202
Gaus Width: 3.5940
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

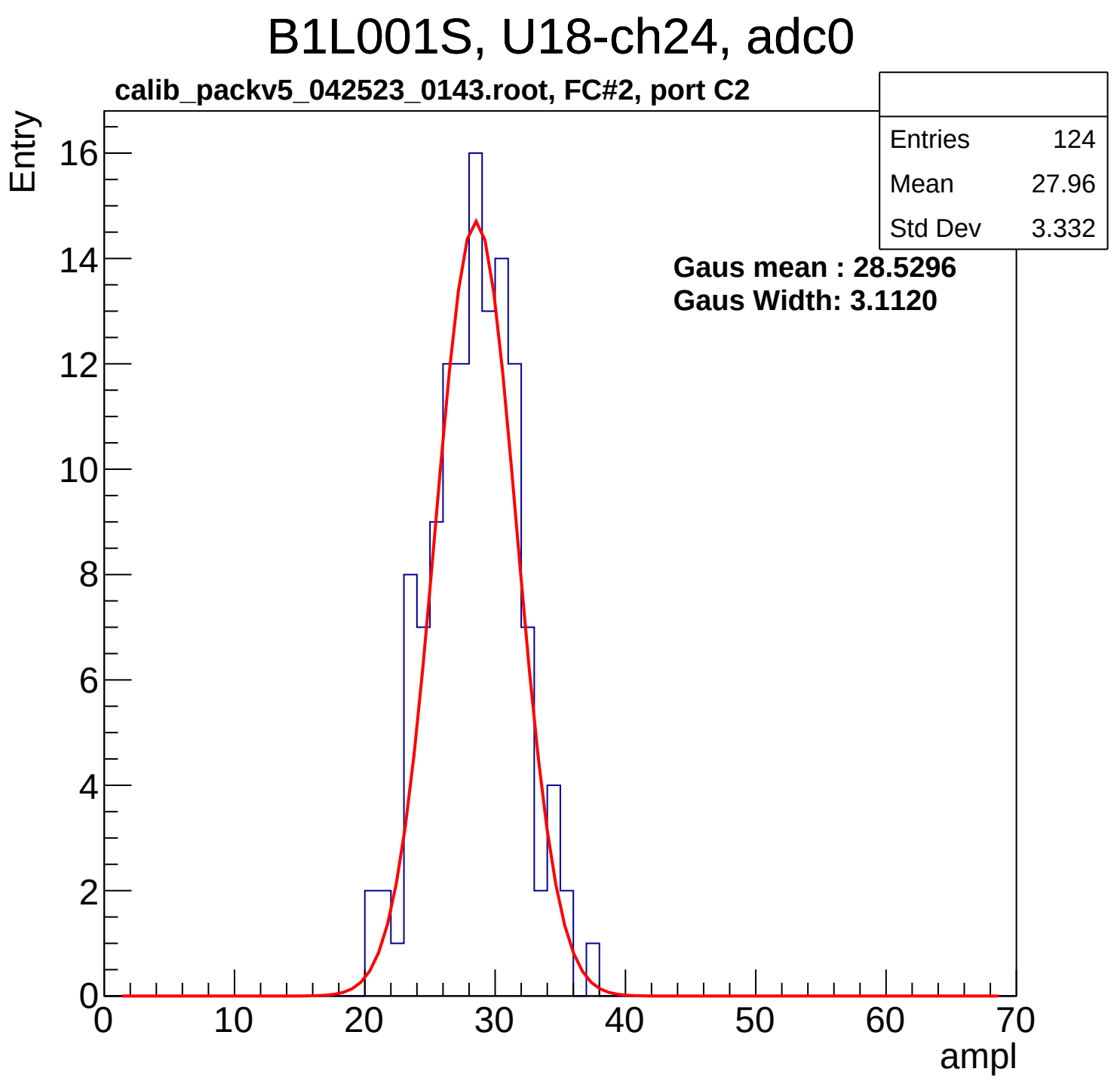

B1L001S, U18-ch23, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 124
Mean 49.06
Std Dev 4.028
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

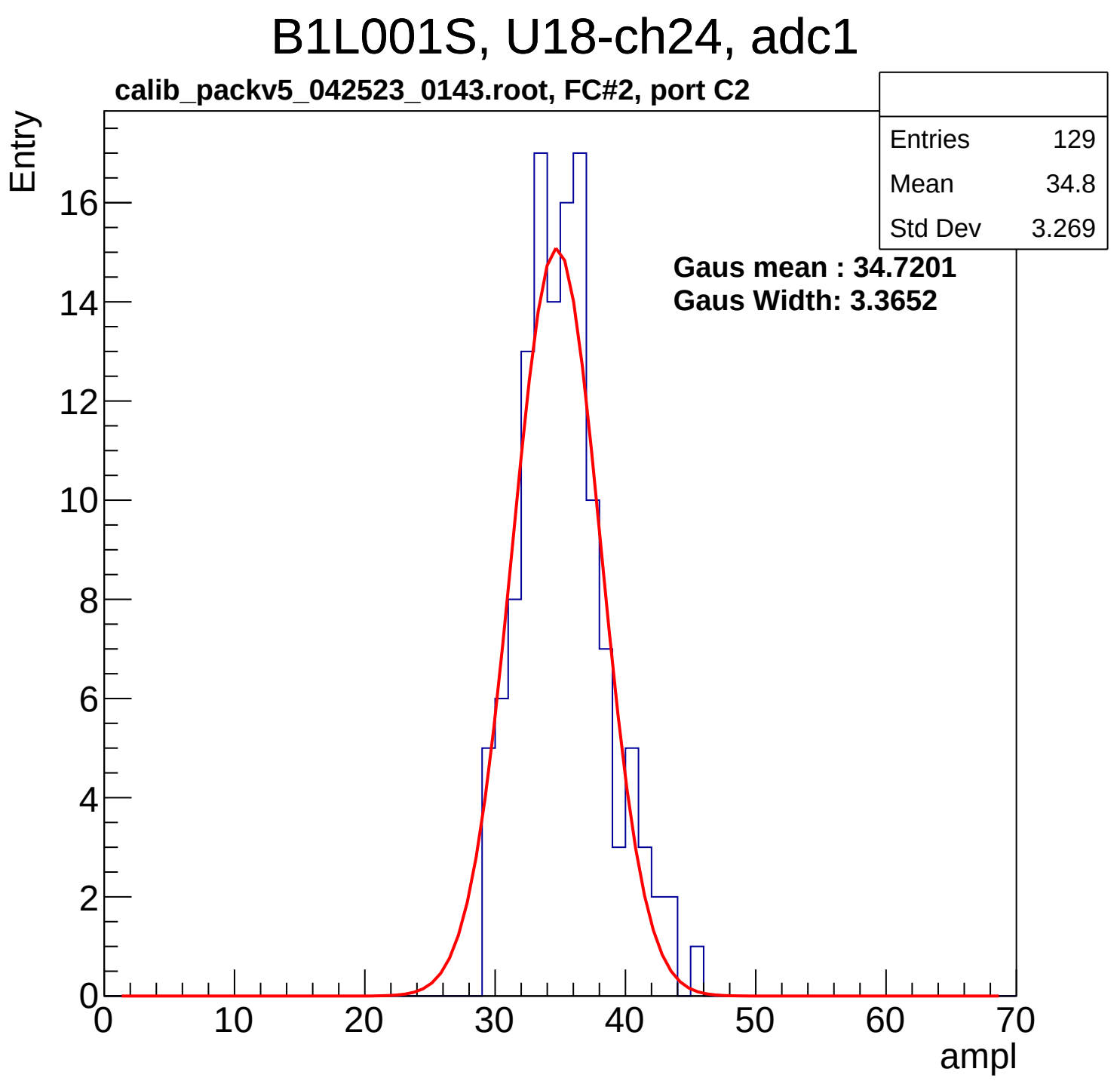

B1L001S, U18-ch23, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 130
Mean 54.77
Std Dev 3.037
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

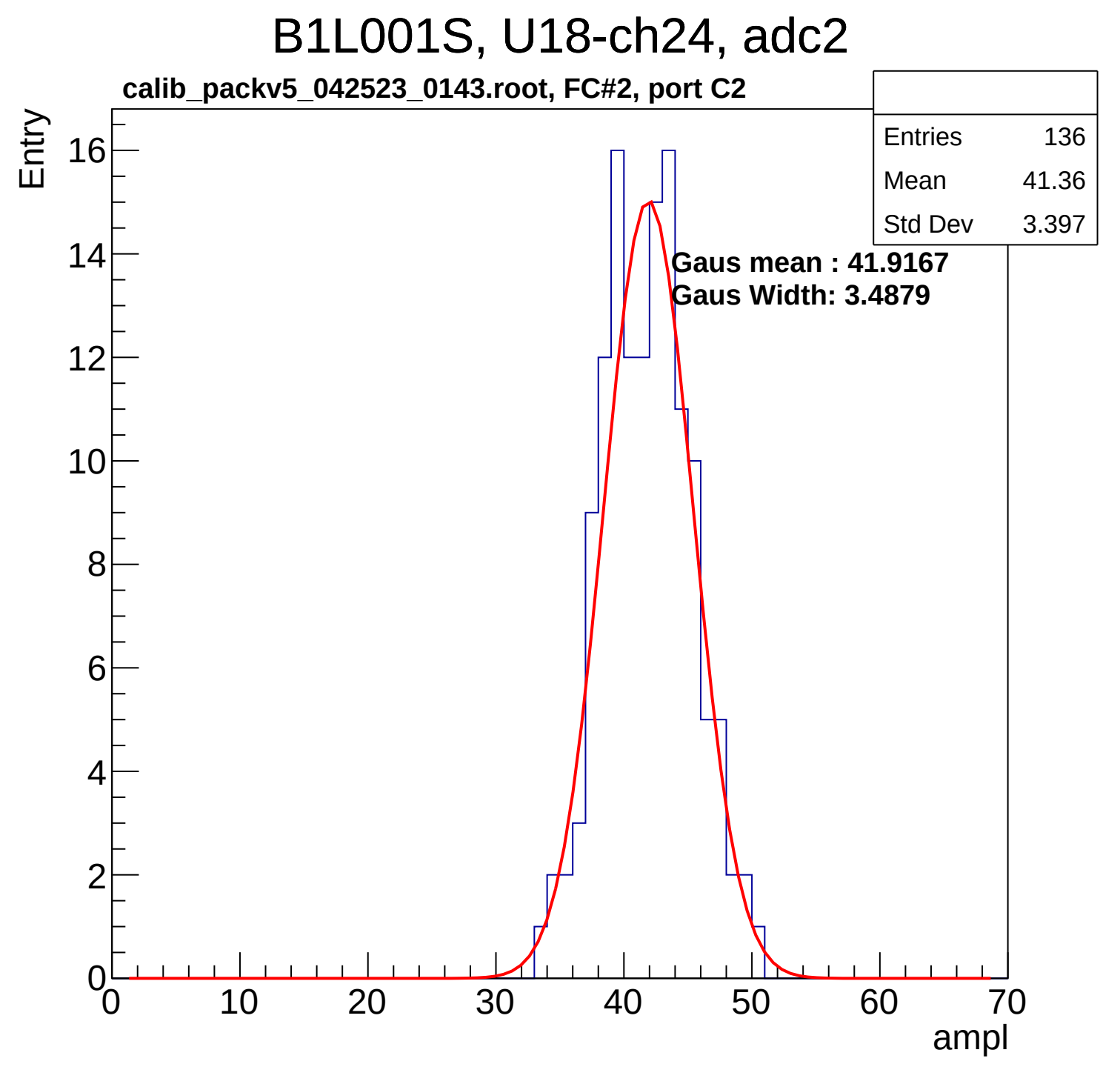

B1L001S, U18-ch23, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 94
Mean 58.9
Std Dev 8.995
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

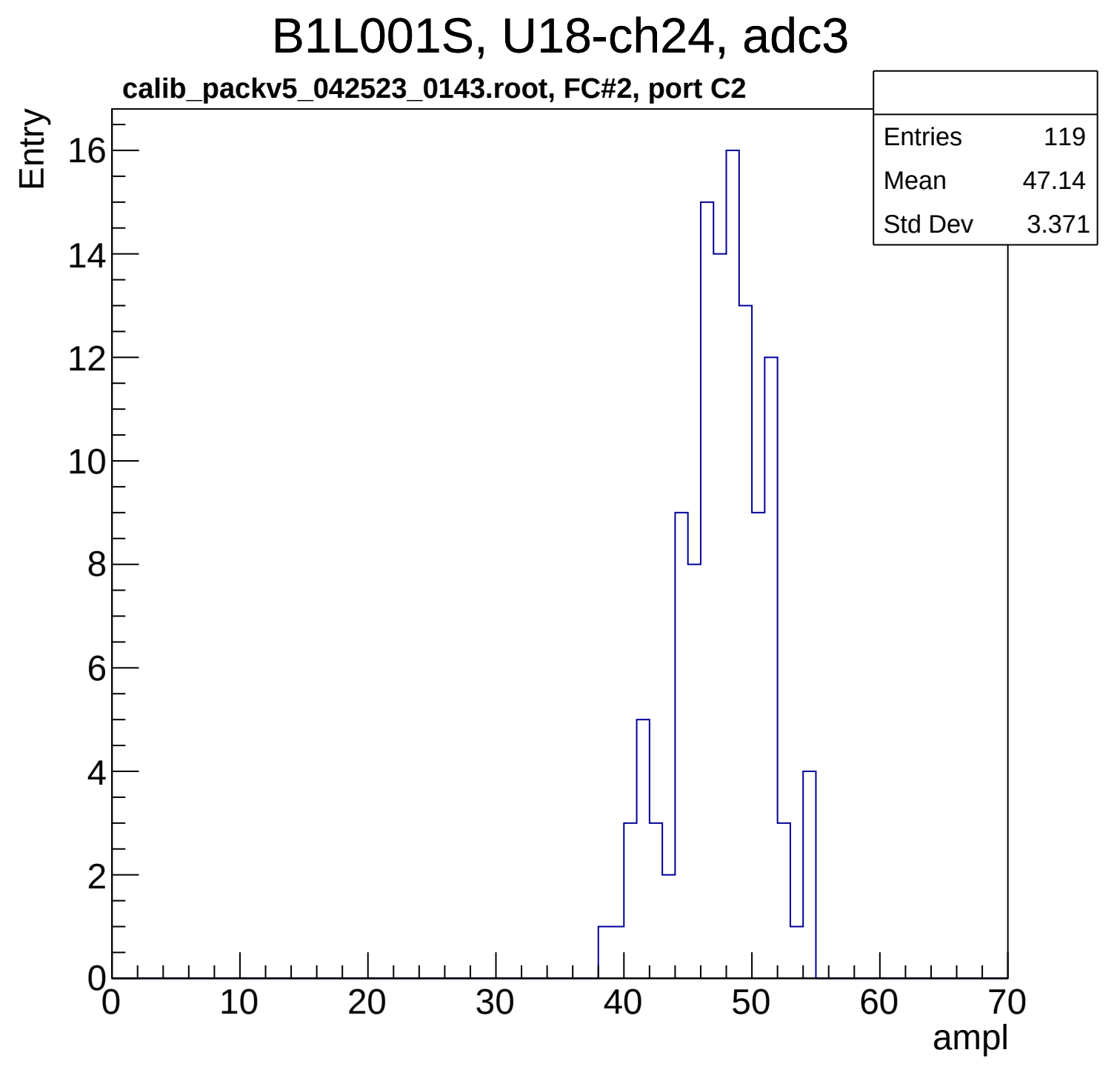

B1L001S, U18-ch23, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 10
Mean 61.8
Std Dev 1.166
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

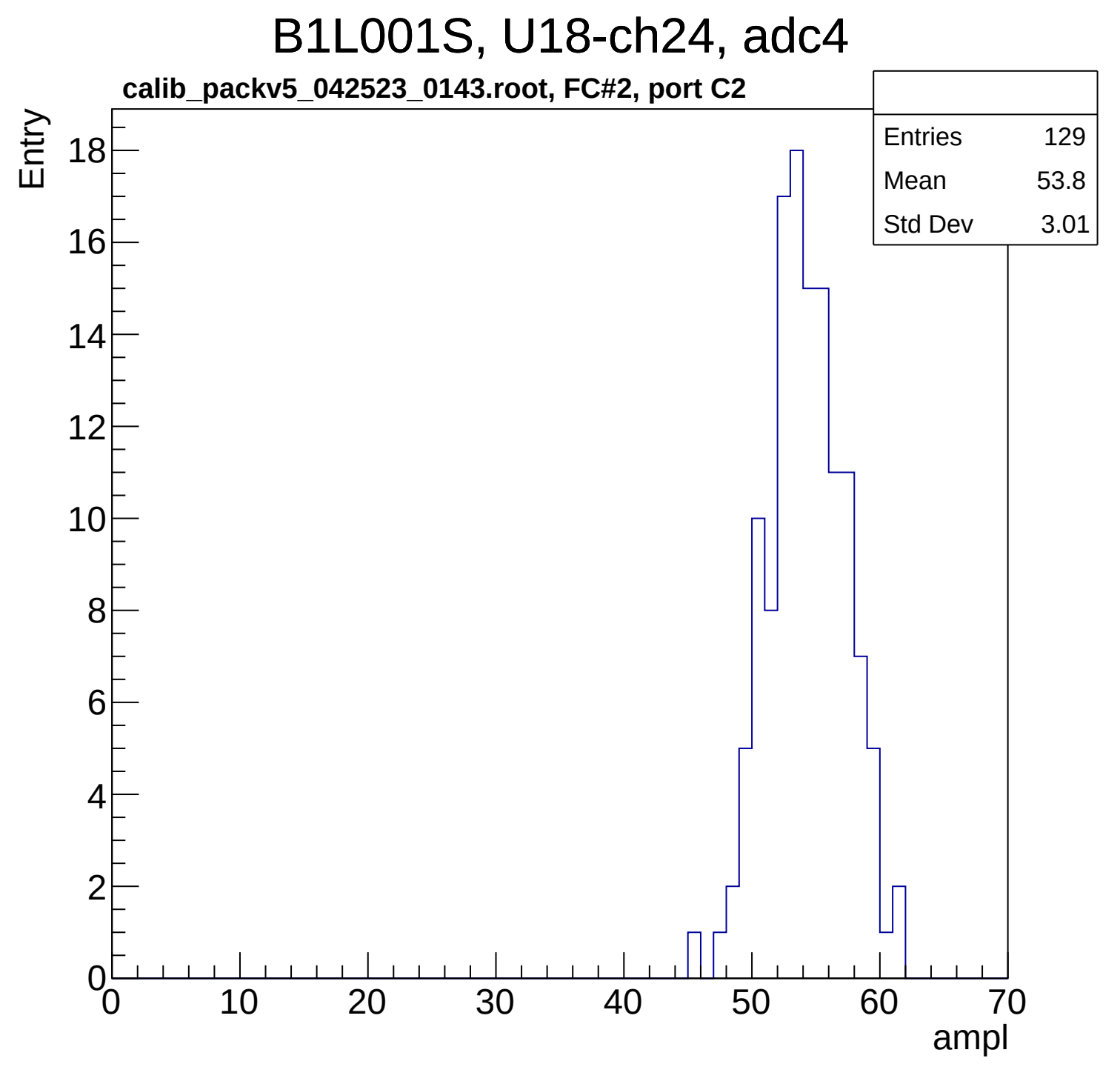

B1L001S, U18-ch23, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 0
Std Dev 0
Entry
2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

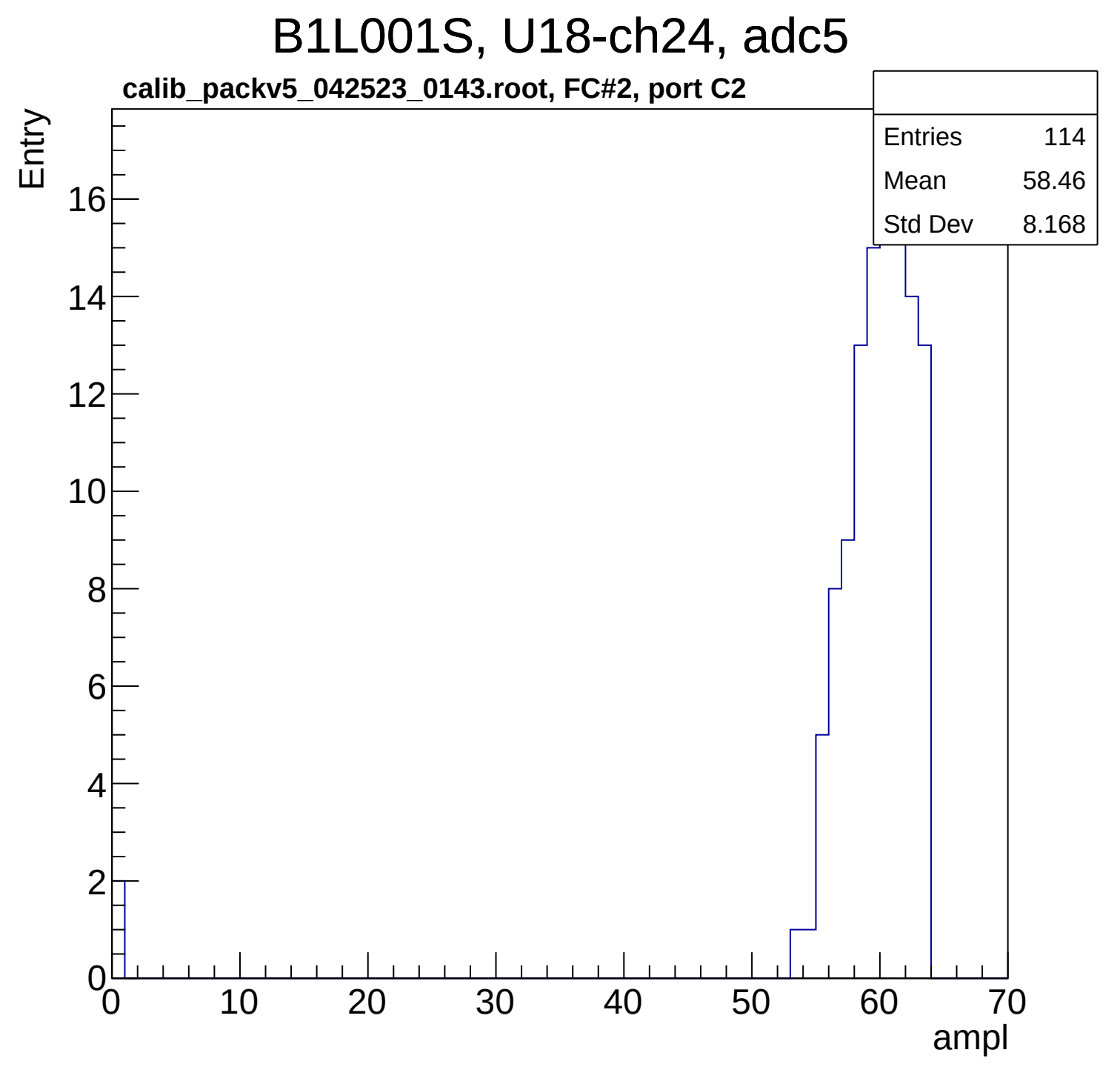

B1L001S, U18-ch24, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 124
Mean 27.96
Std Dev 3.332
Gaus mean : 28.5296
Gaus Width: 3.1120
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

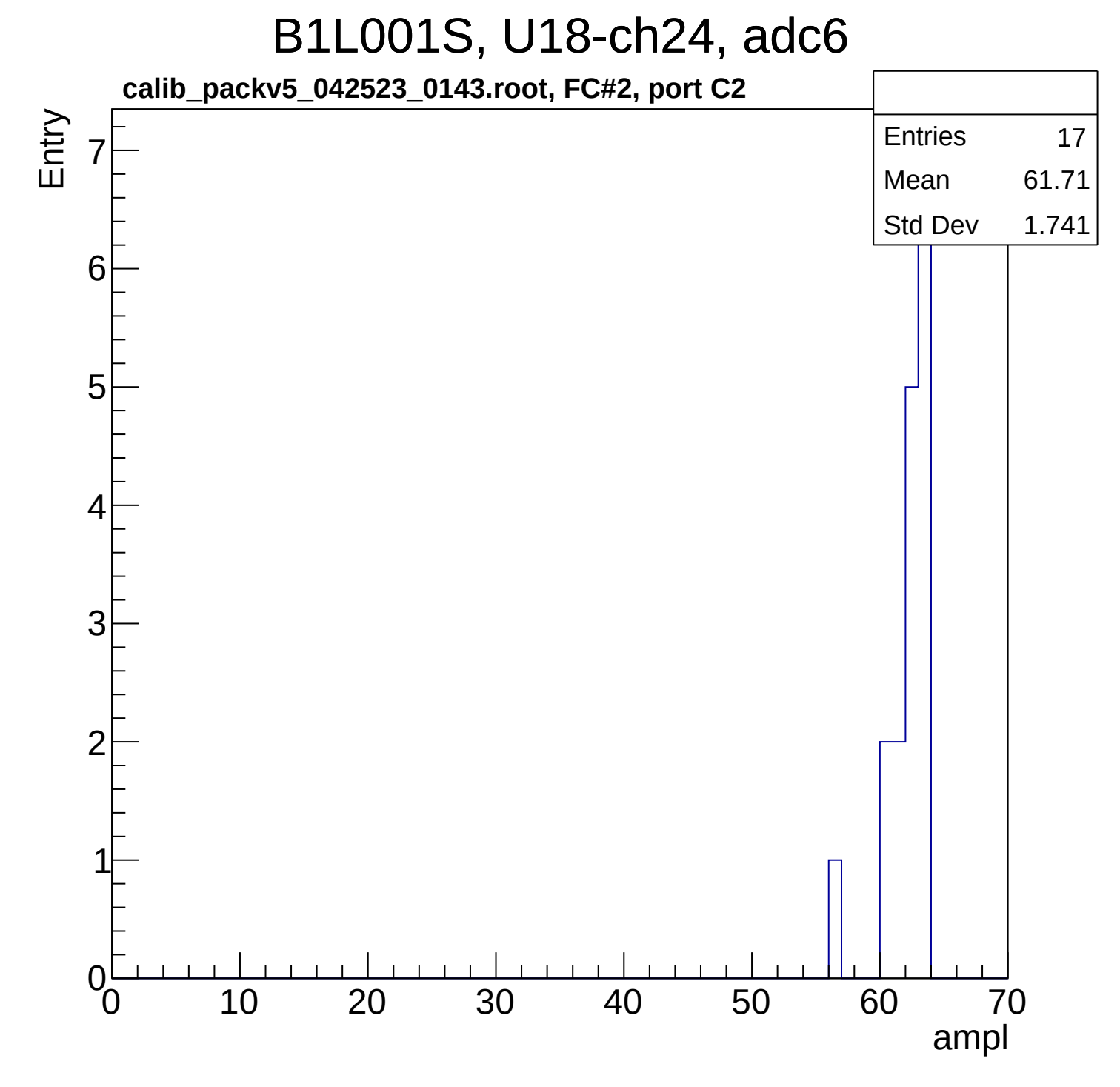

B1L001S, U18-ch24, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 129
Mean 34.8
Std Dev 3.269
Gaus mean : 34.7201
Gaus Width: 3.3652
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

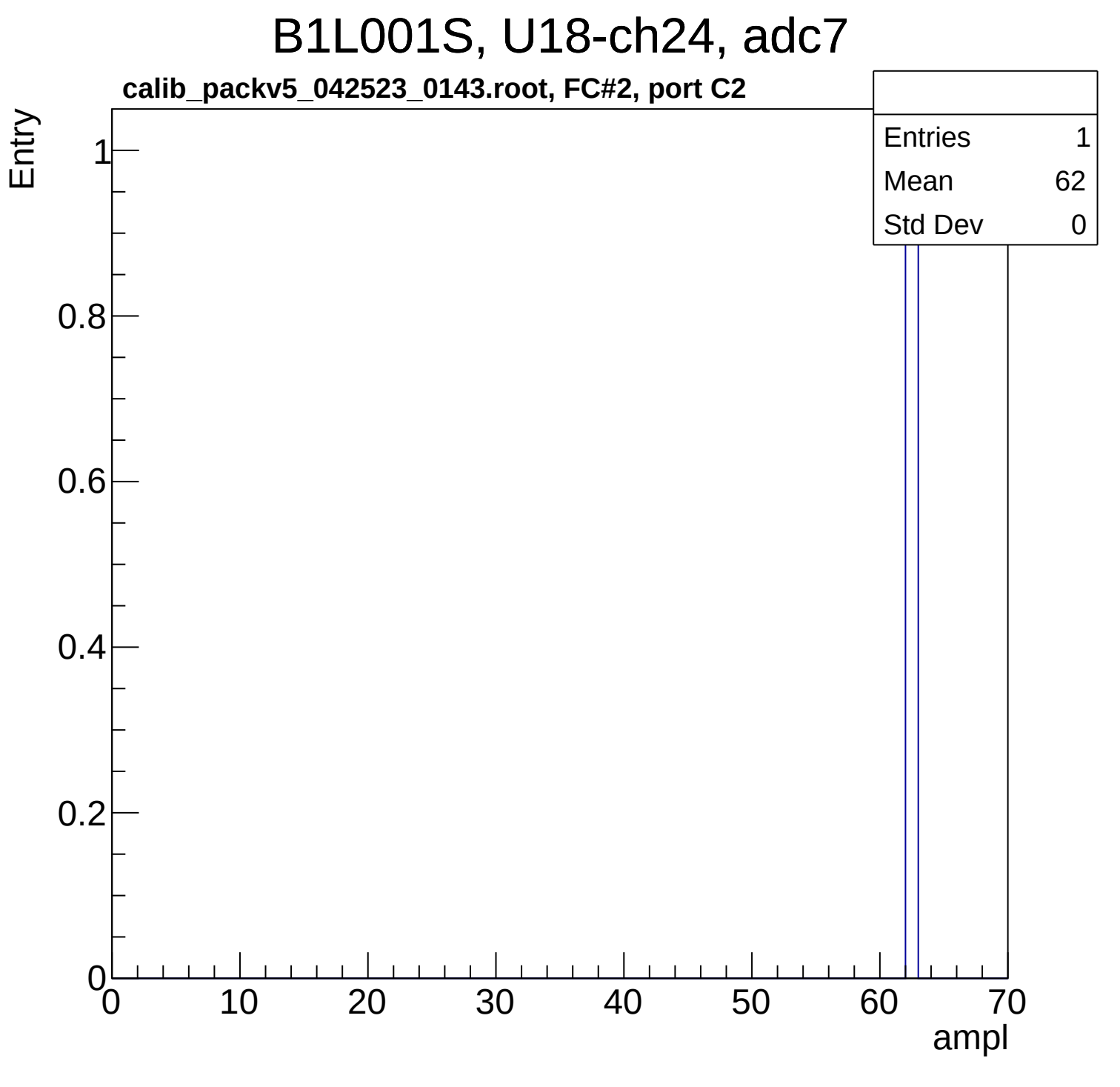

B1L001S, U18-ch24, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 136
Mean 41.36
Std Dev 3.397
Gaus mean : 41.9167
Gaus Width: 3.4879
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

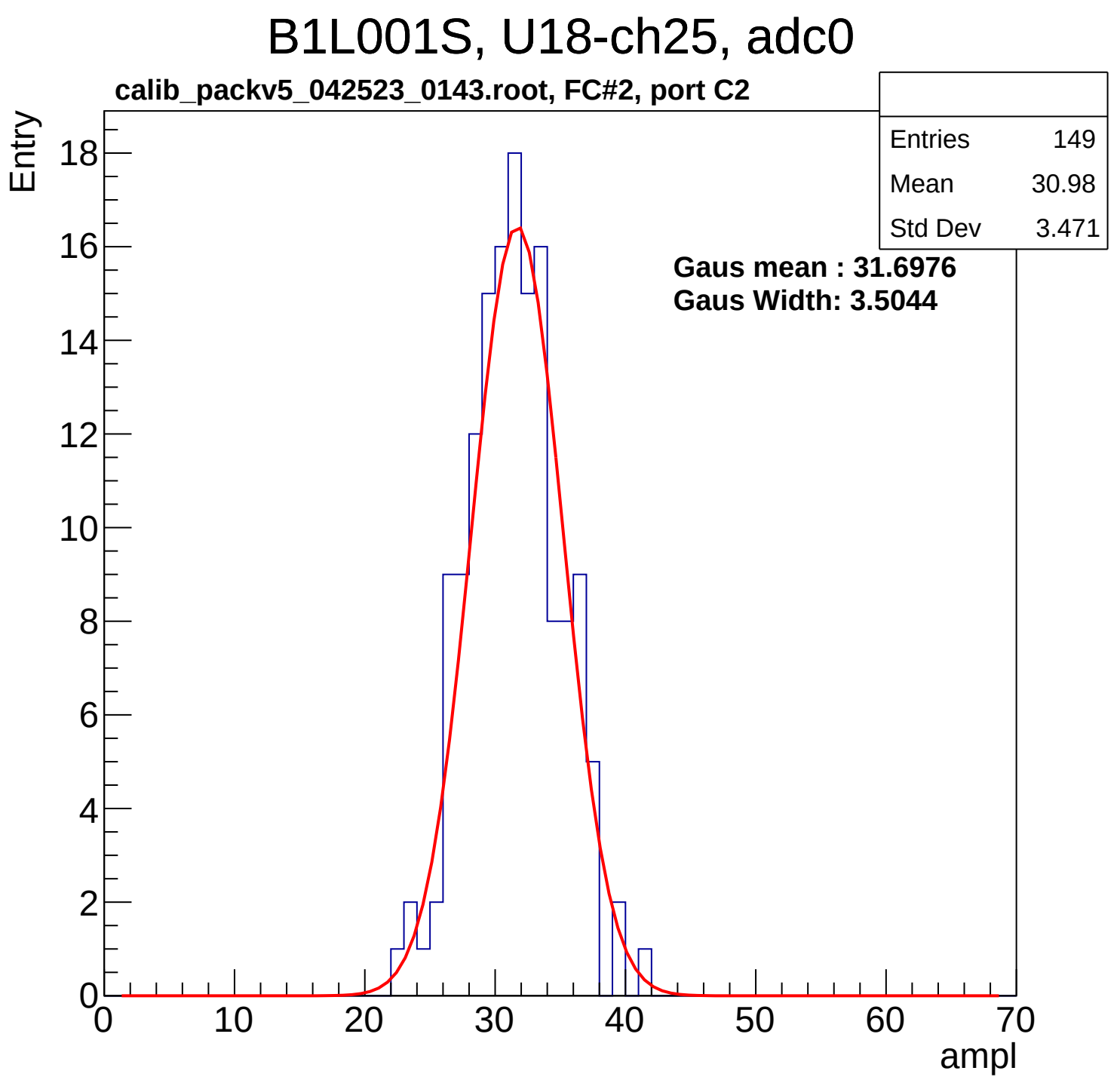

B1L001S, U18-ch24, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 119
Mean 47.14
Std Dev 3.371
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

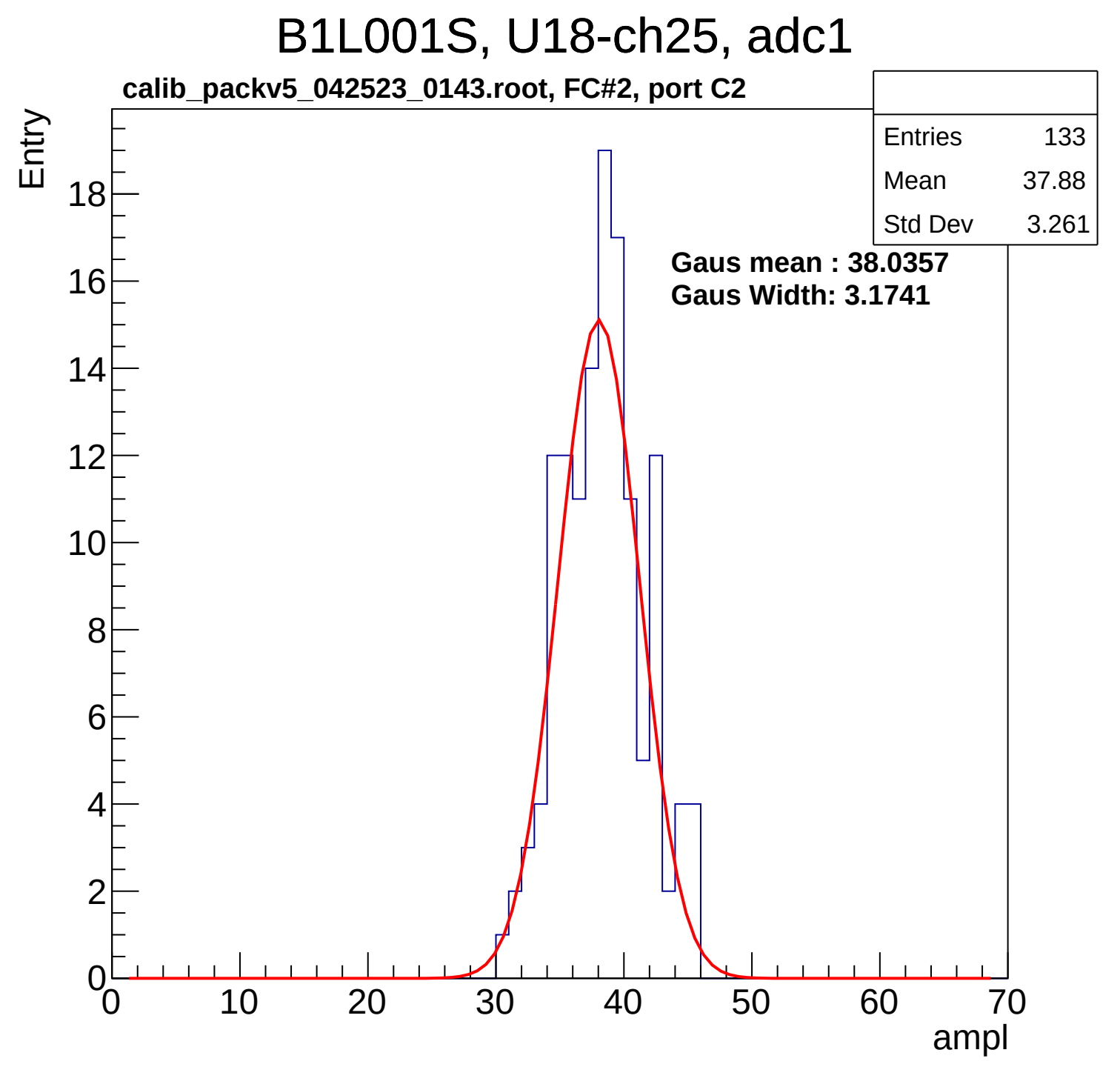

B1L001S, U18-ch24, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 129
Mean 53.8
Std Dev 3.01
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

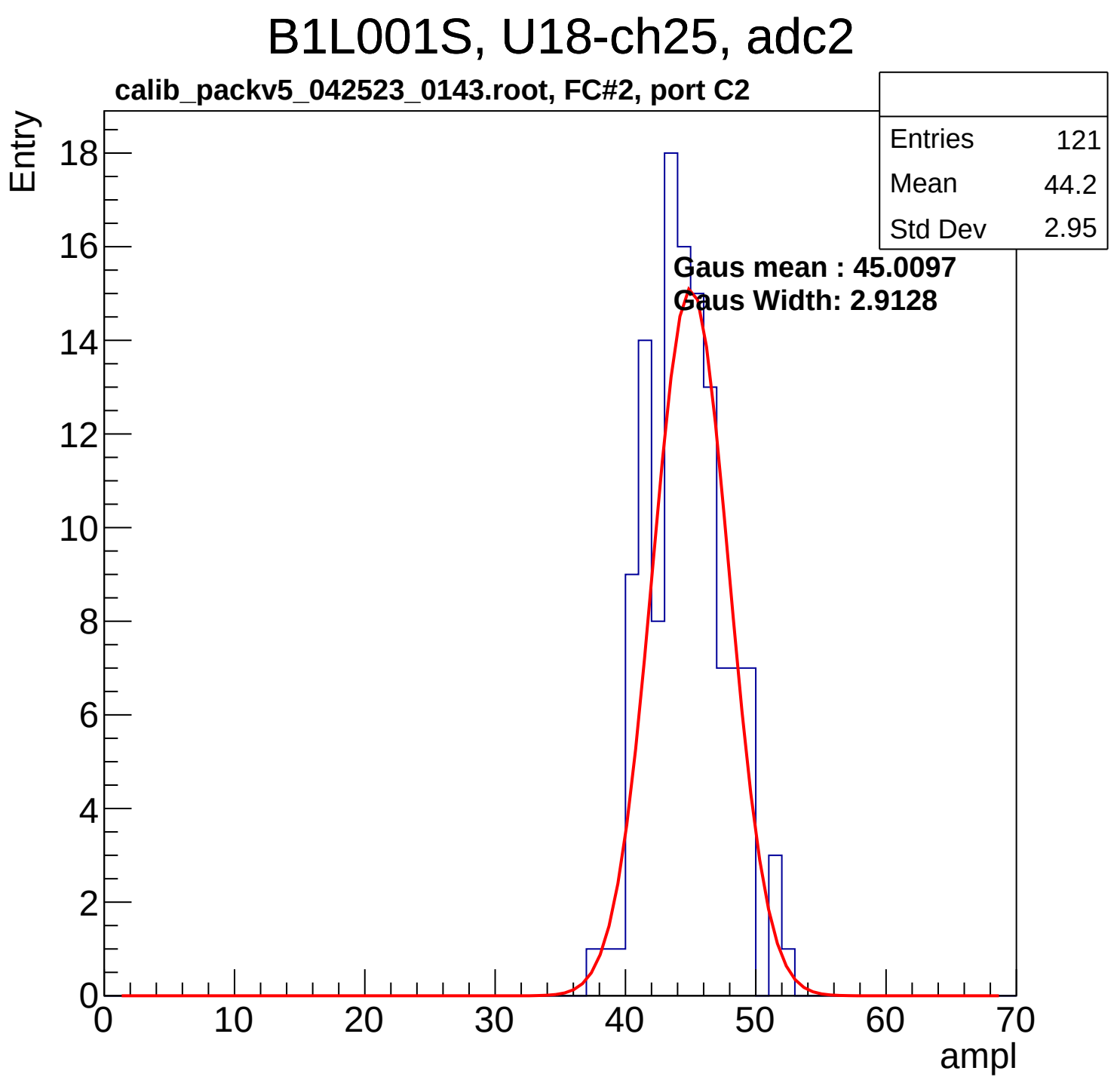

B1L001S, U18-ch24, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 114
Mean 58.46
Std Dev 8.168
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

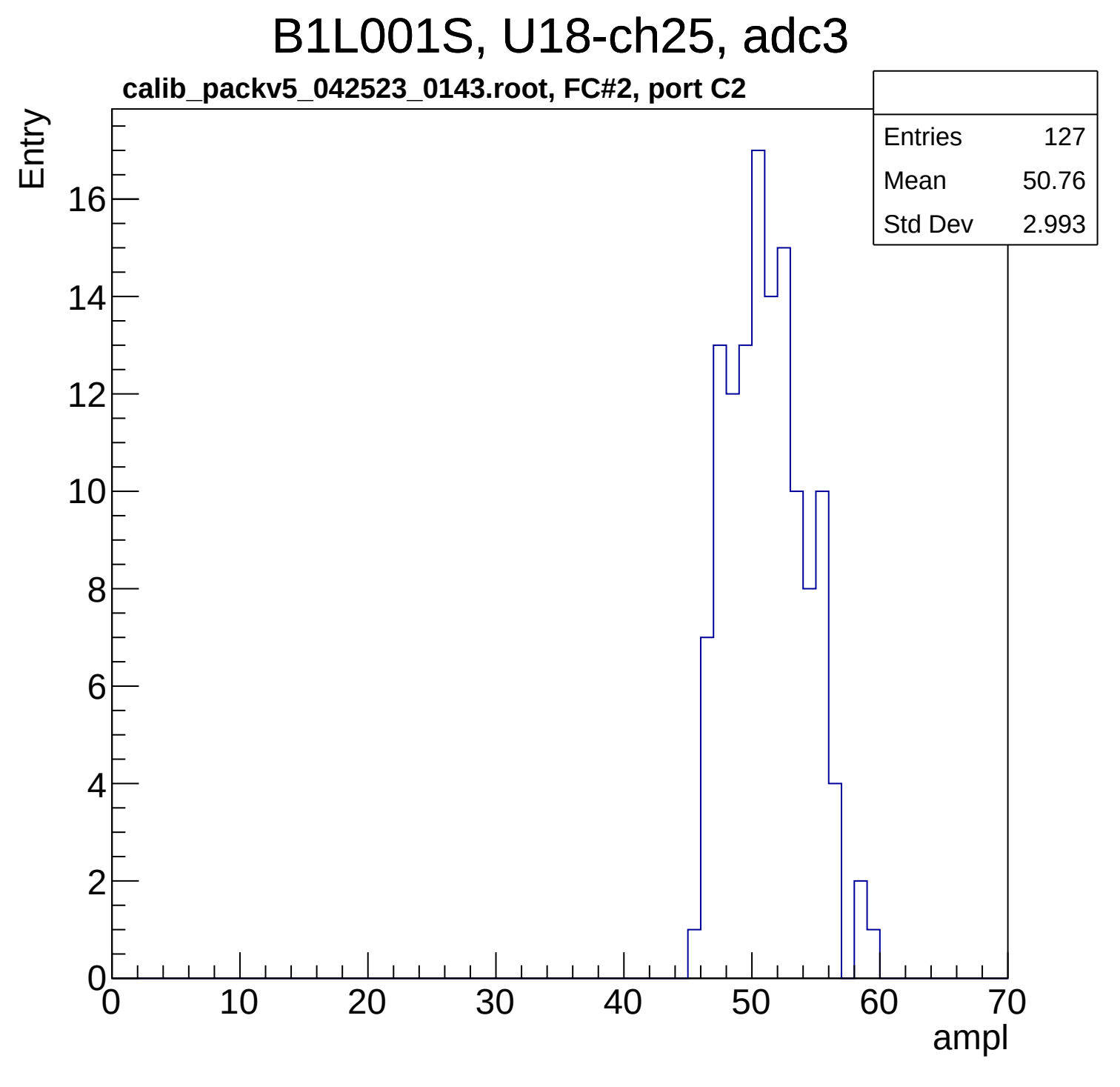

B1L001S, U18-ch24, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 17
Mean 61.71
Std Dev 1.741
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

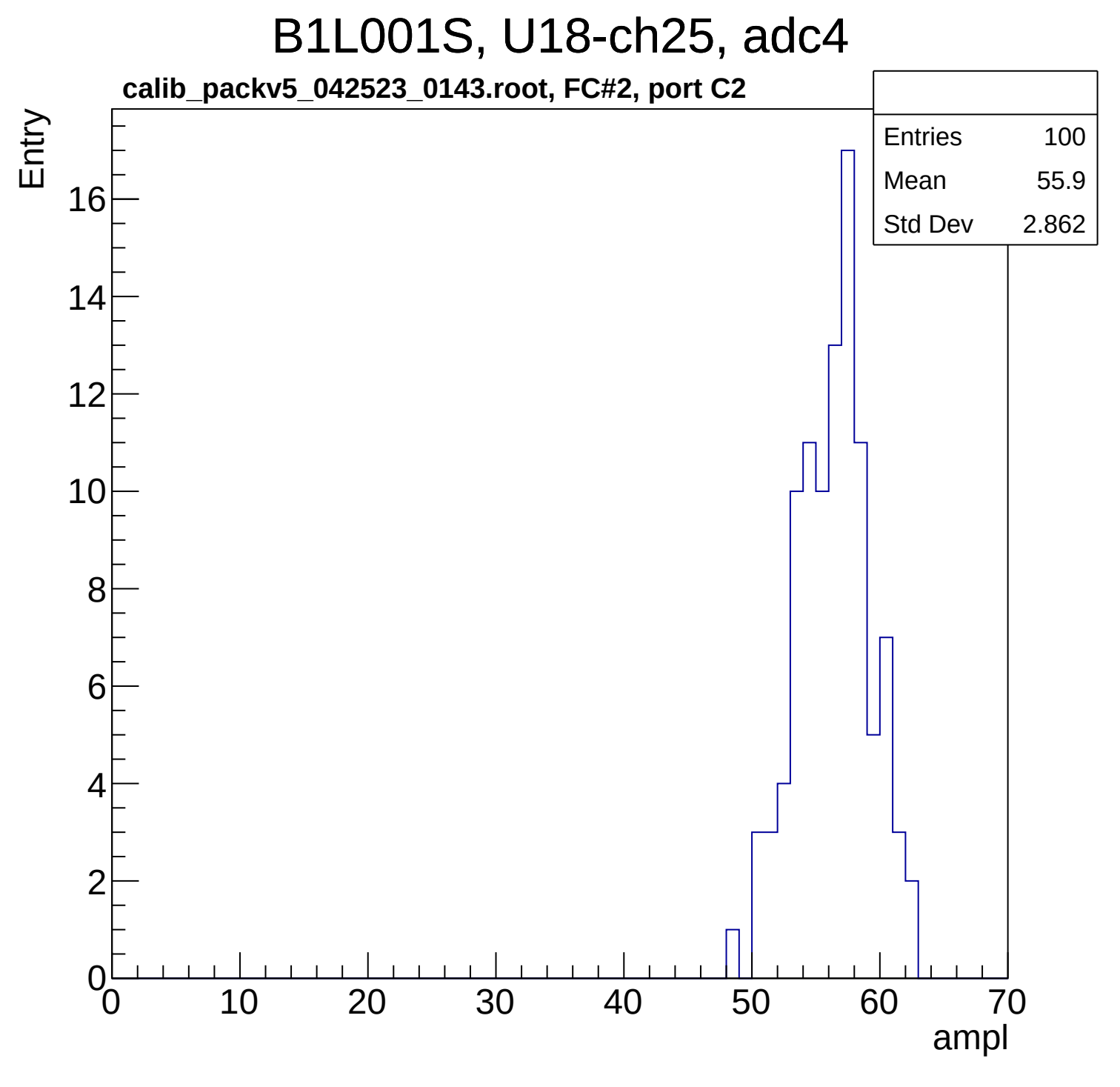

B1L001S, U18-ch24, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 62
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

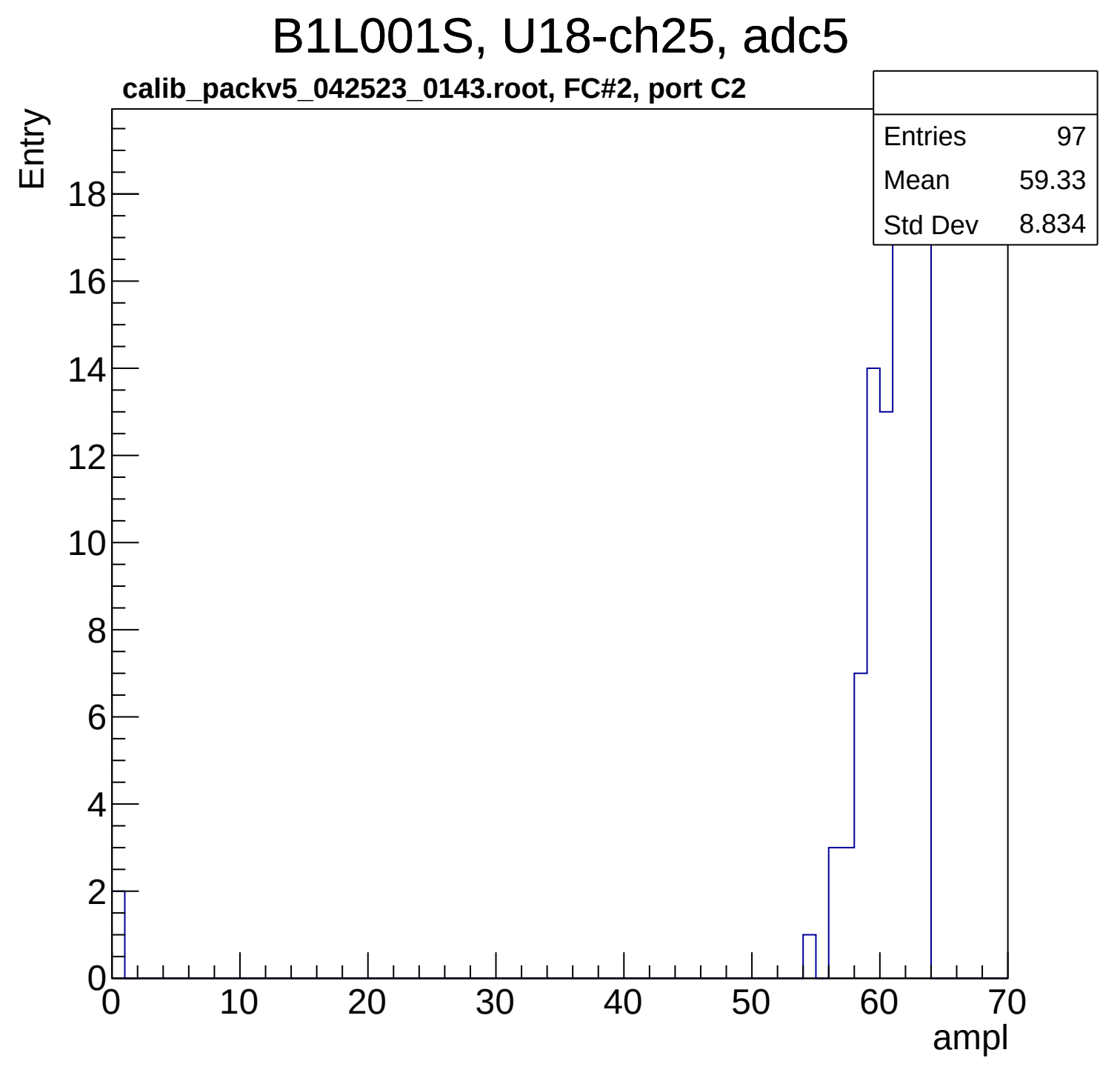

B1L001S, U18-ch25, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 149
Mean 30.98
Std Dev 3.471
Gaus mean : 31.6976
Gaus Width: 3.5044
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

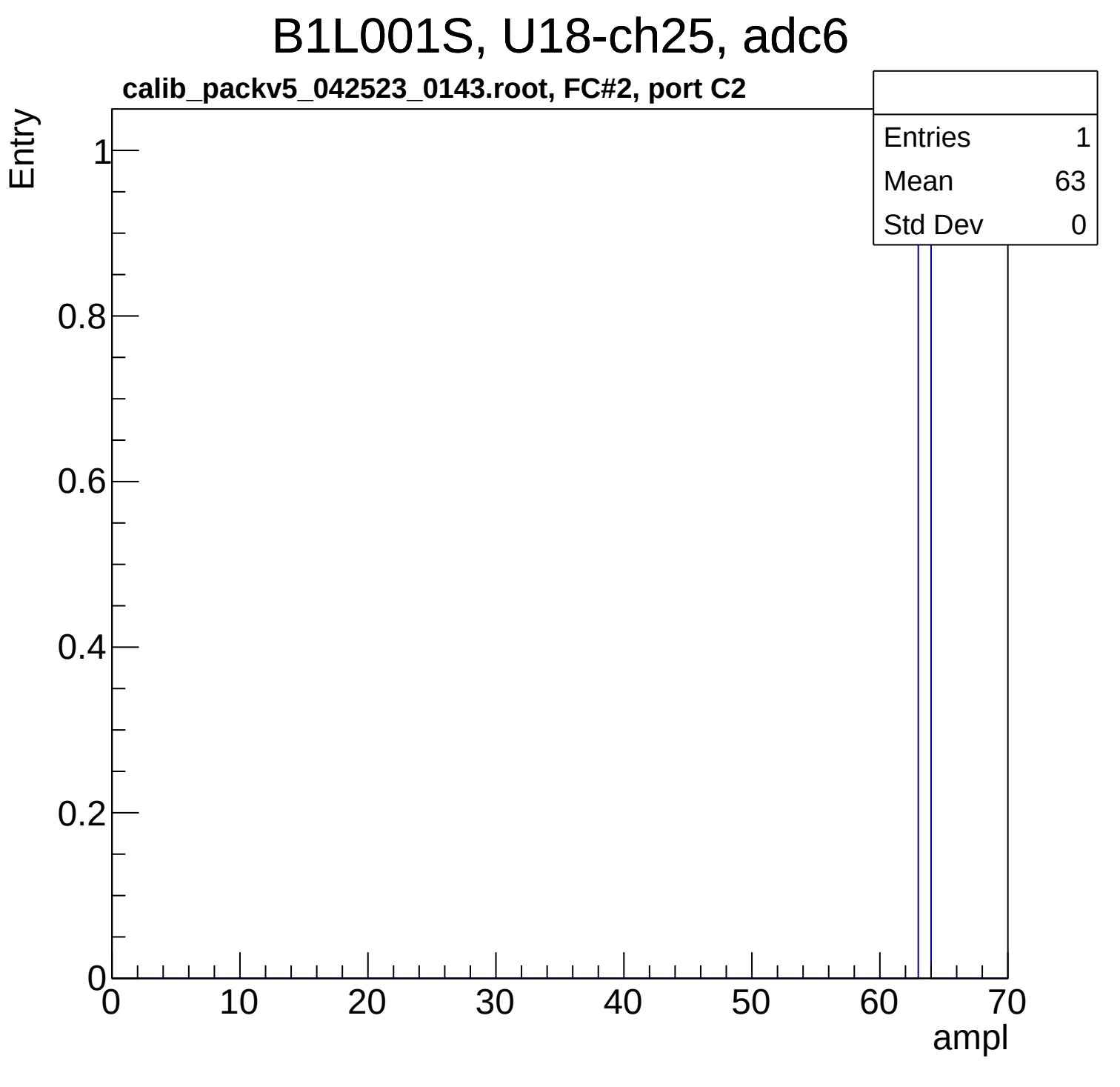

B1L001S, U18-ch25, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 133
Mean 37.88
Std Dev 3.261
Gaus mean : 38.0357
Gaus Width: 3.1741
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

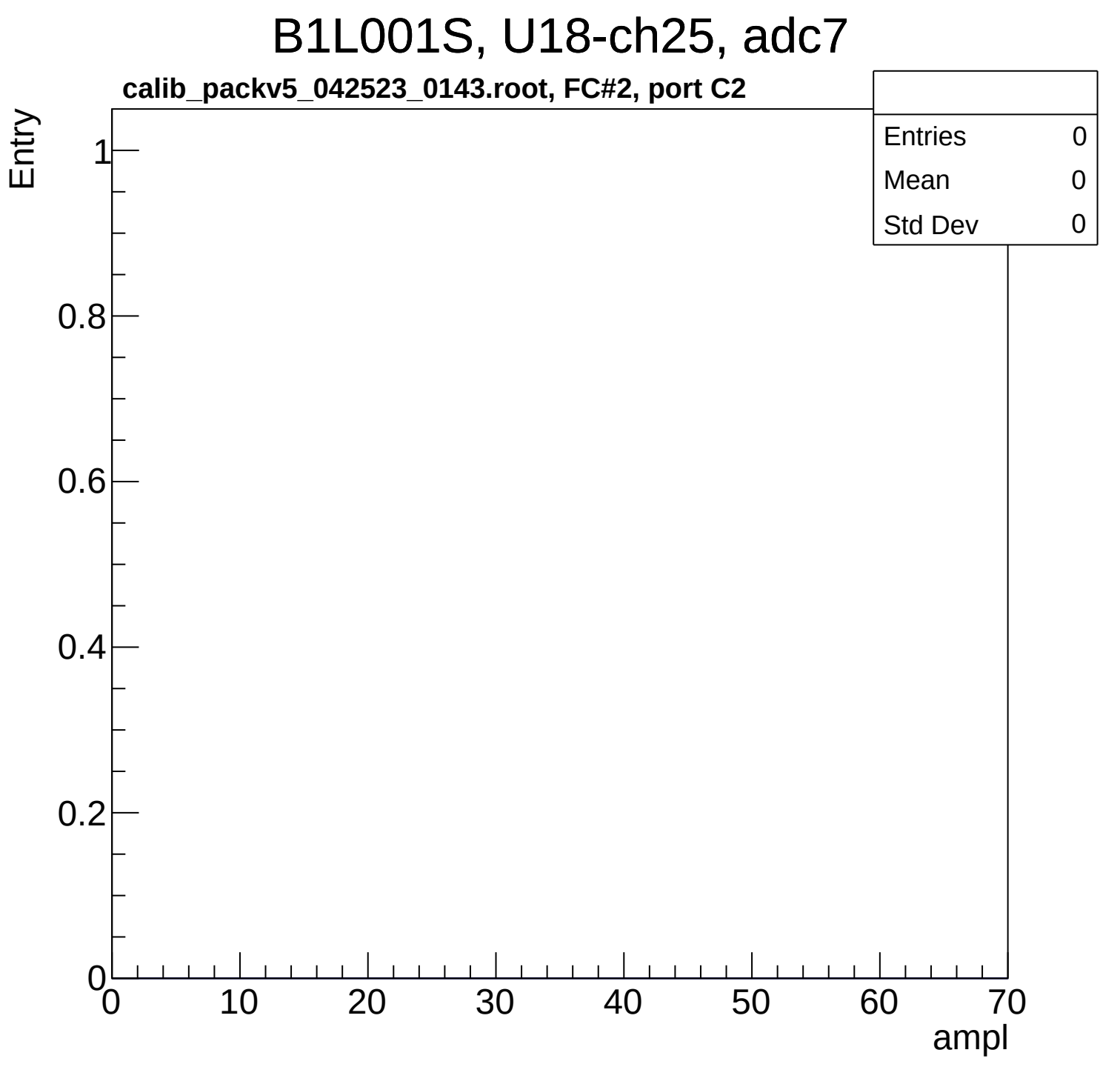

B1L001S, U18-ch25, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 121
Mean 44.2
Std Dev 2.95
Gaus mean : 45.0097
Gaus Width: 2.9128
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

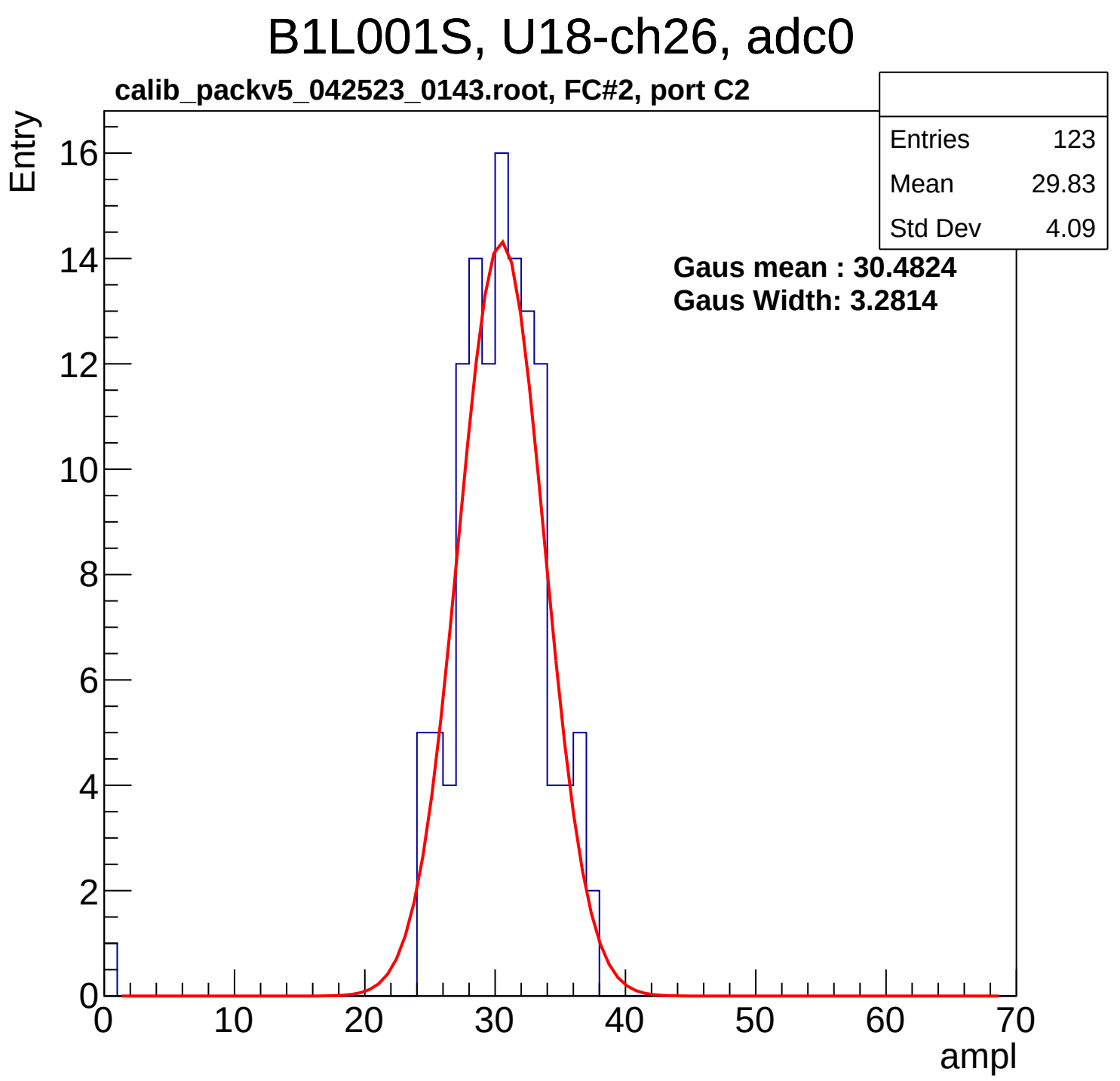

B1L001S, U18-ch25, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 127
Mean 50.76
Std Dev 2.993
Entry
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl

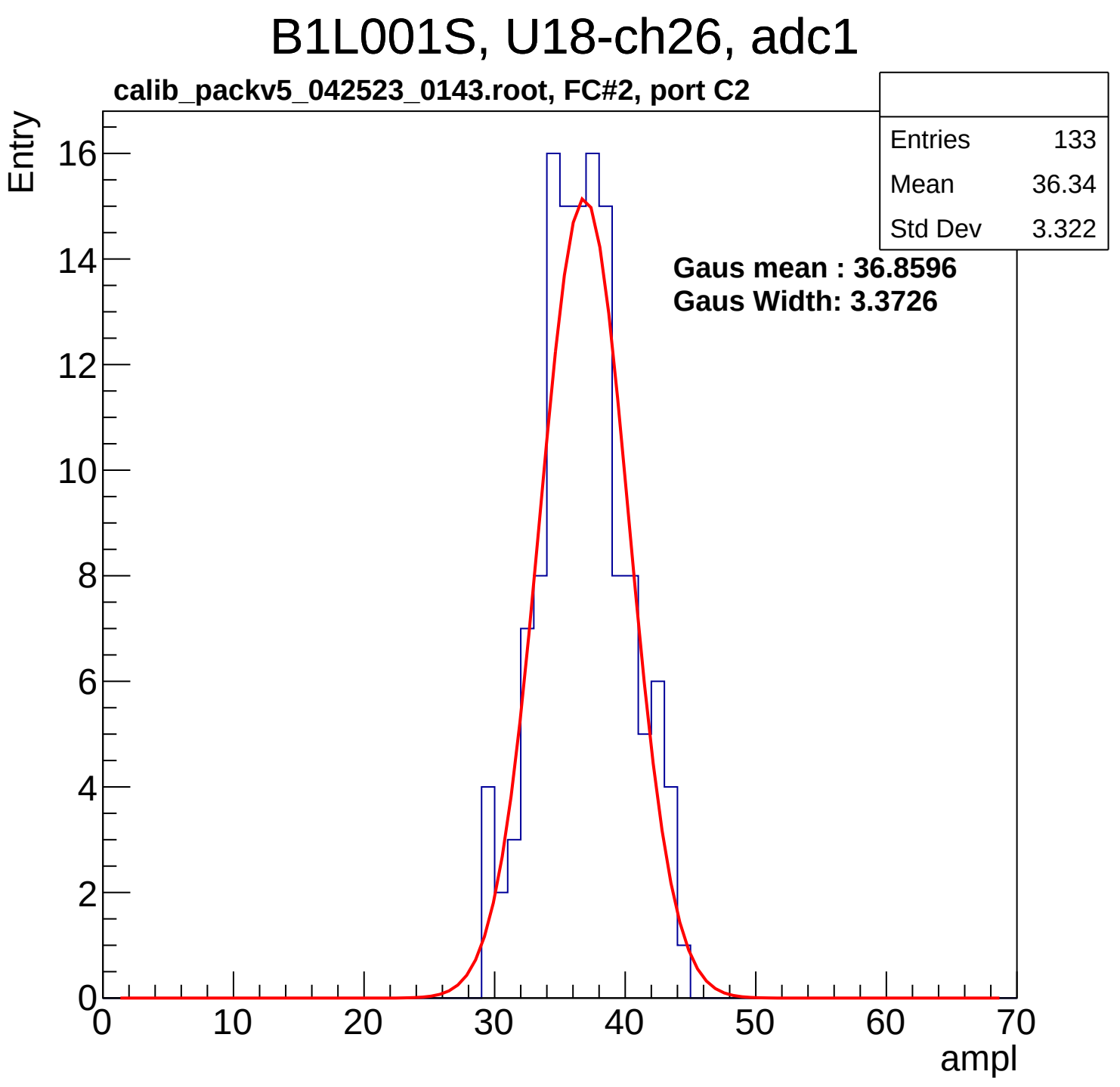

B1L001S, U18-ch25, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 100
Mean 55.9
Std Dev 2.862
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

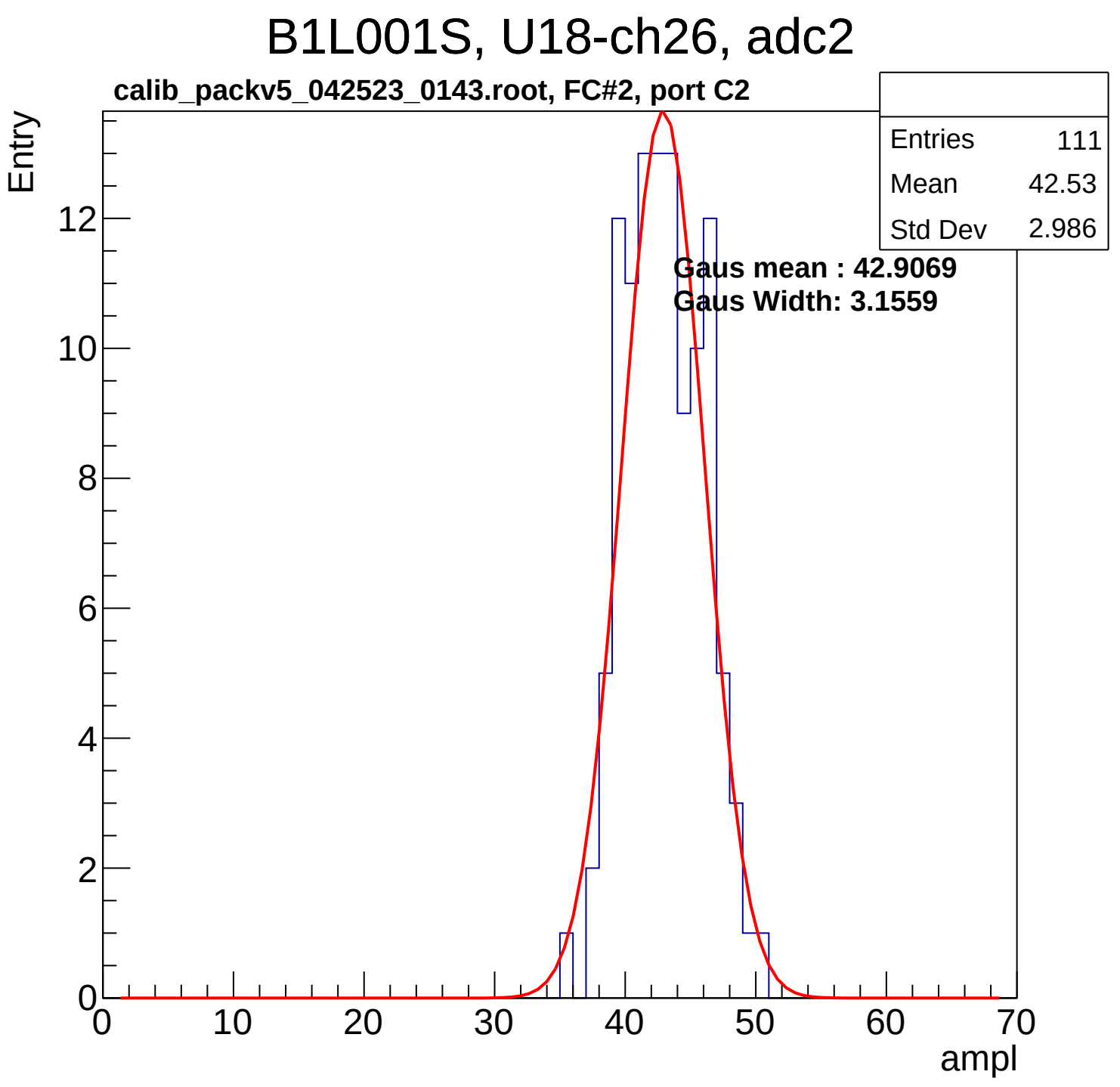

B1L001S, U18-ch25, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 97
Mean 59.33
Std Dev 8.834
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

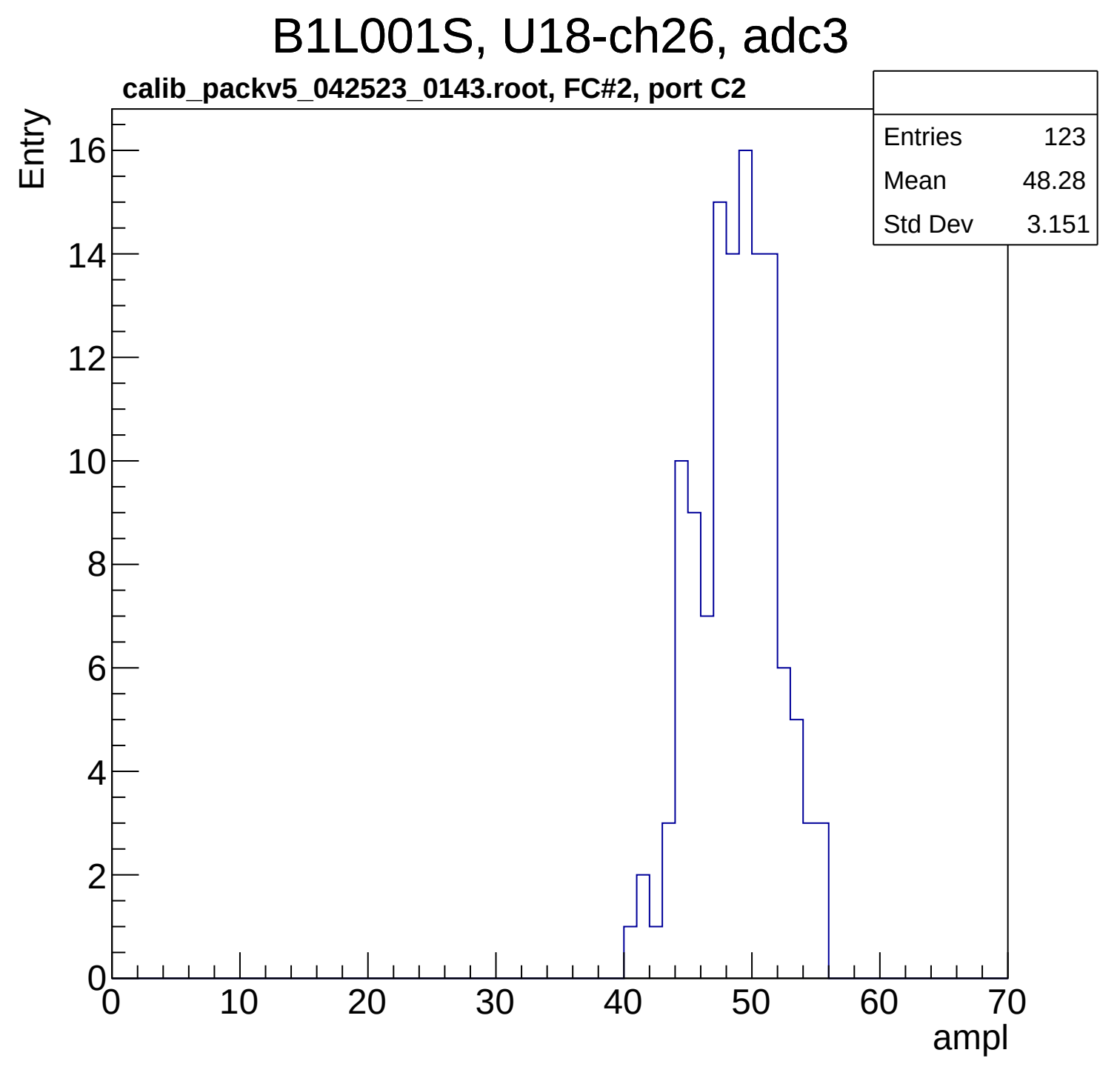

B1L001S, U18-ch25, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 63
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

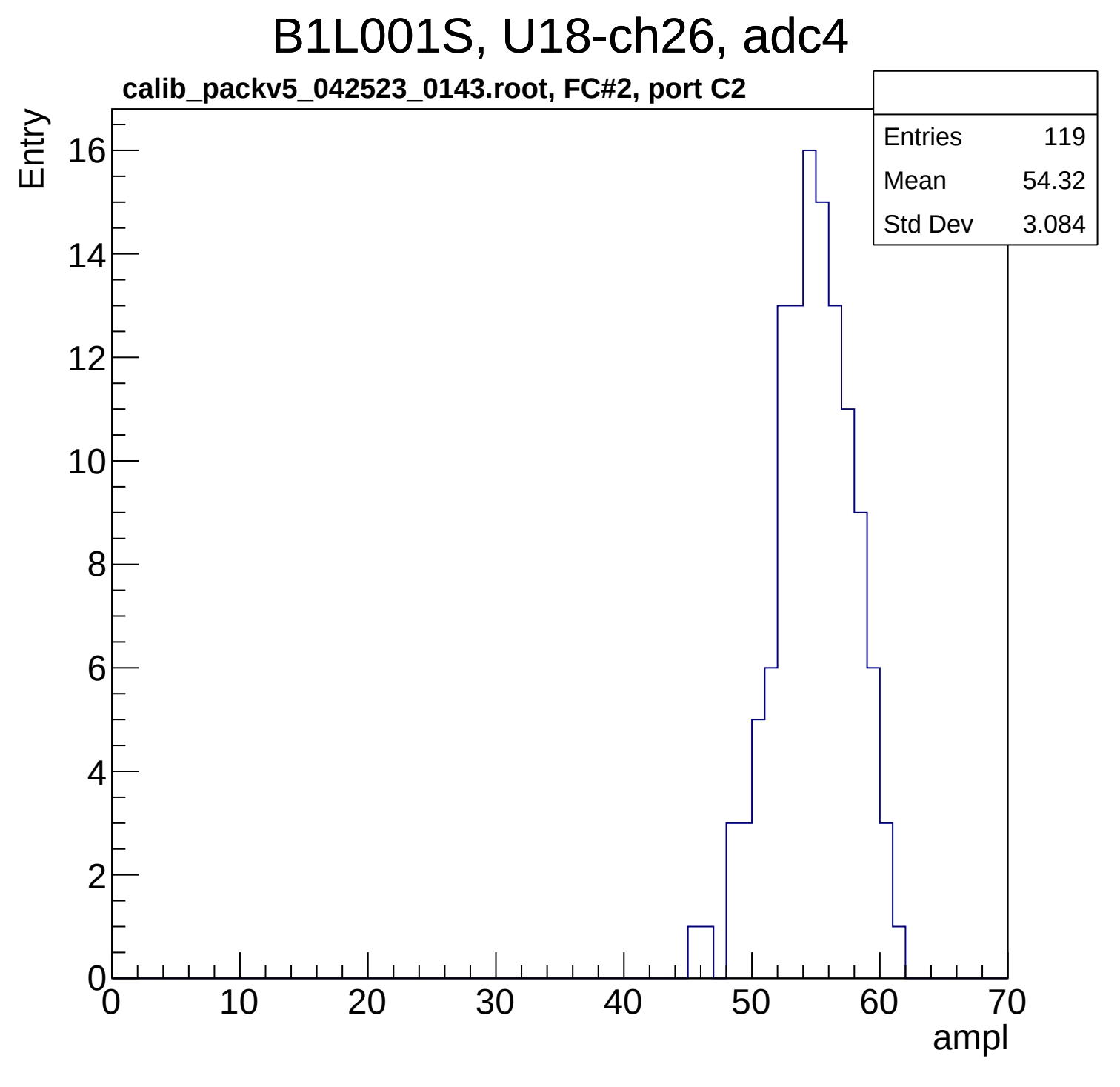

B1L001S, U18-ch25, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

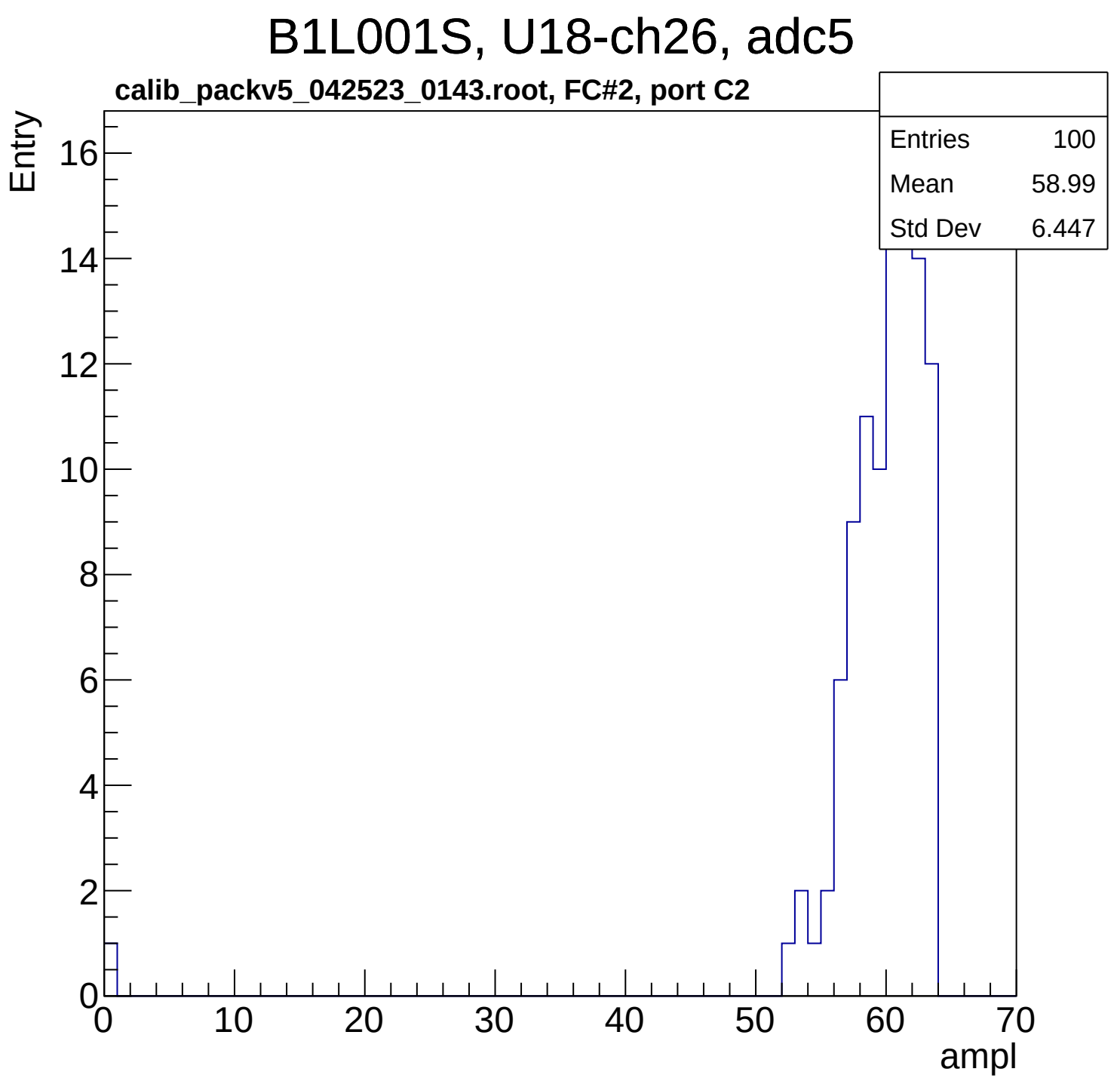

B1L001S, U18-ch26, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 123
Mean 29.83
Std Dev 4.09
Gaus mean : 30.4824
Gaus Width: 3.2814
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

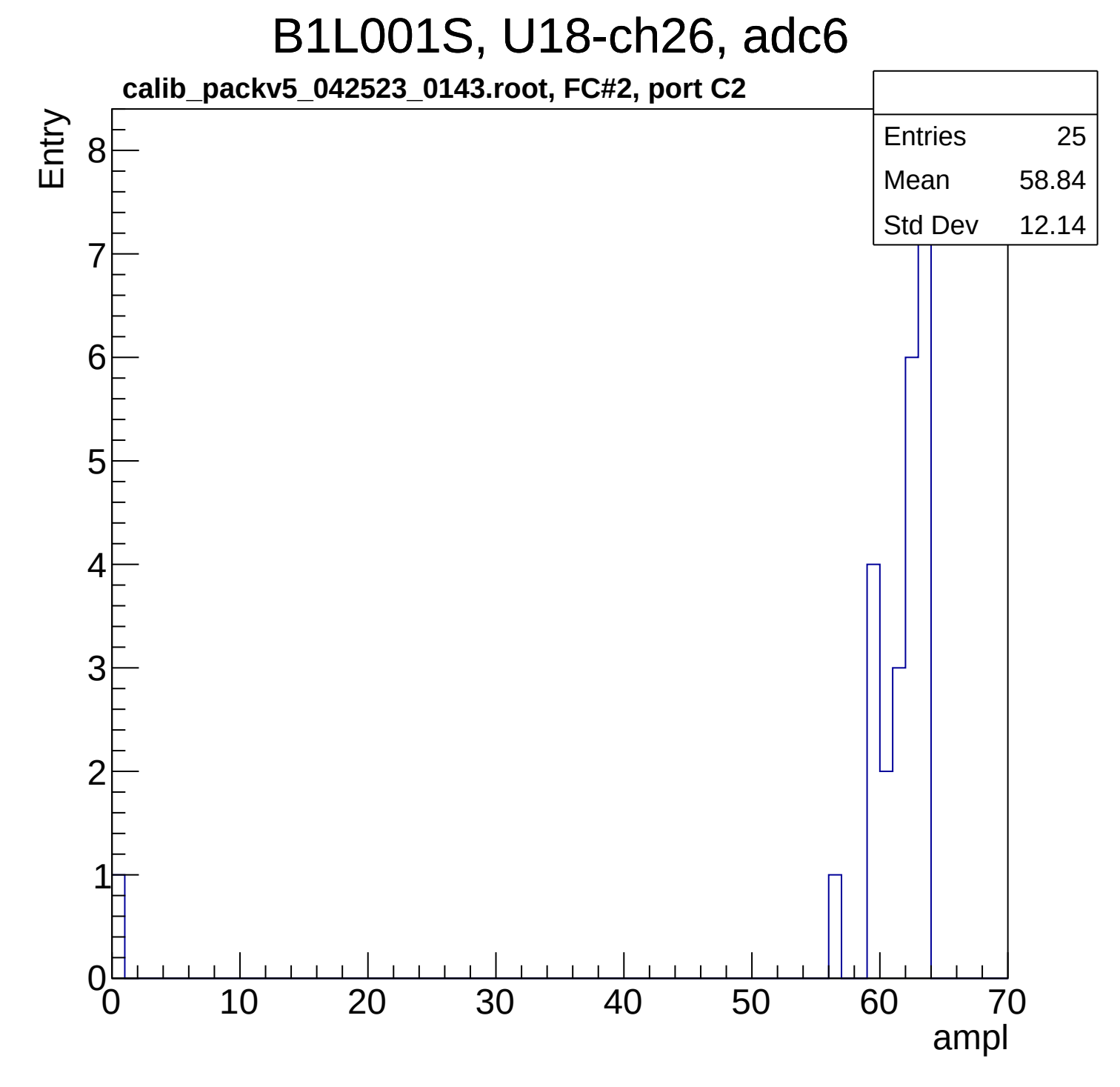

B1L001S, U18-ch26, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 133
Mean 36.34
Std Dev 3.322
Gaus mean : 36.8596
Gaus Width: 3.3726
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

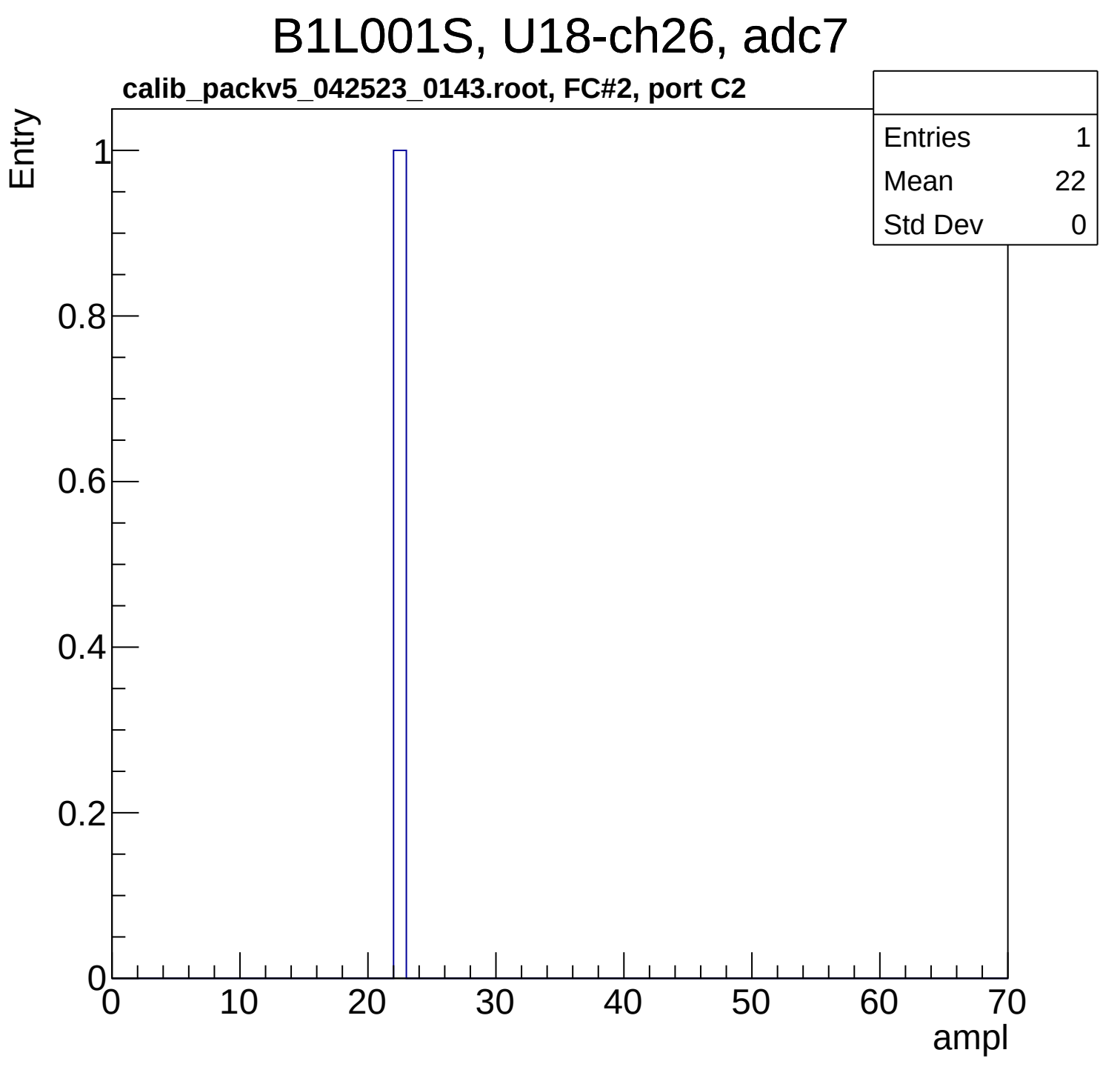

B1L001S, U18-ch26, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 111
Mean 42.53
Std Dev 2.986
Gaus mean : 42.9069
Gaus Width: 3.1559
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70

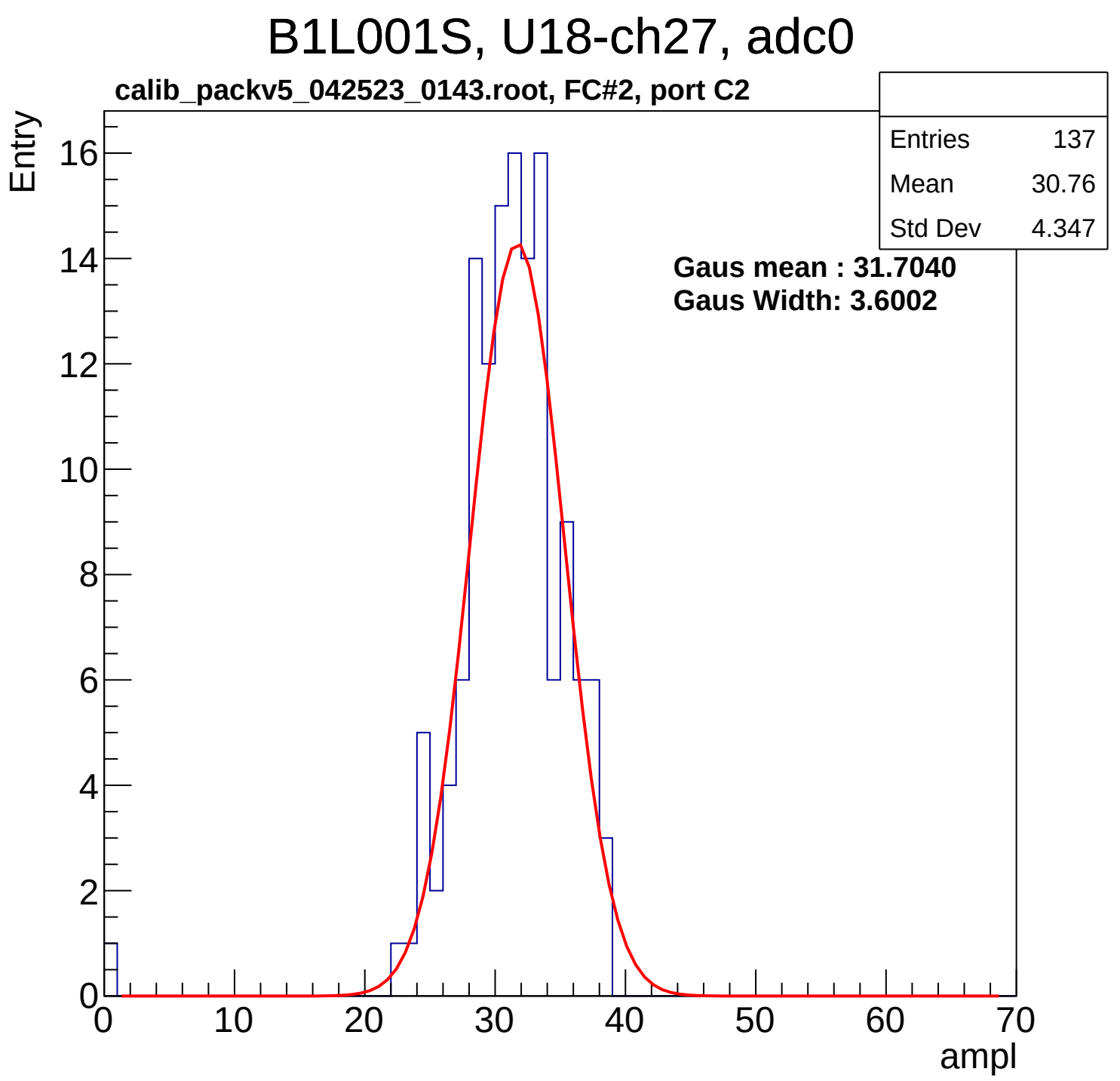

B1L001S, U18-ch26, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 123
Mean 48.28
Std Dev 3.151
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

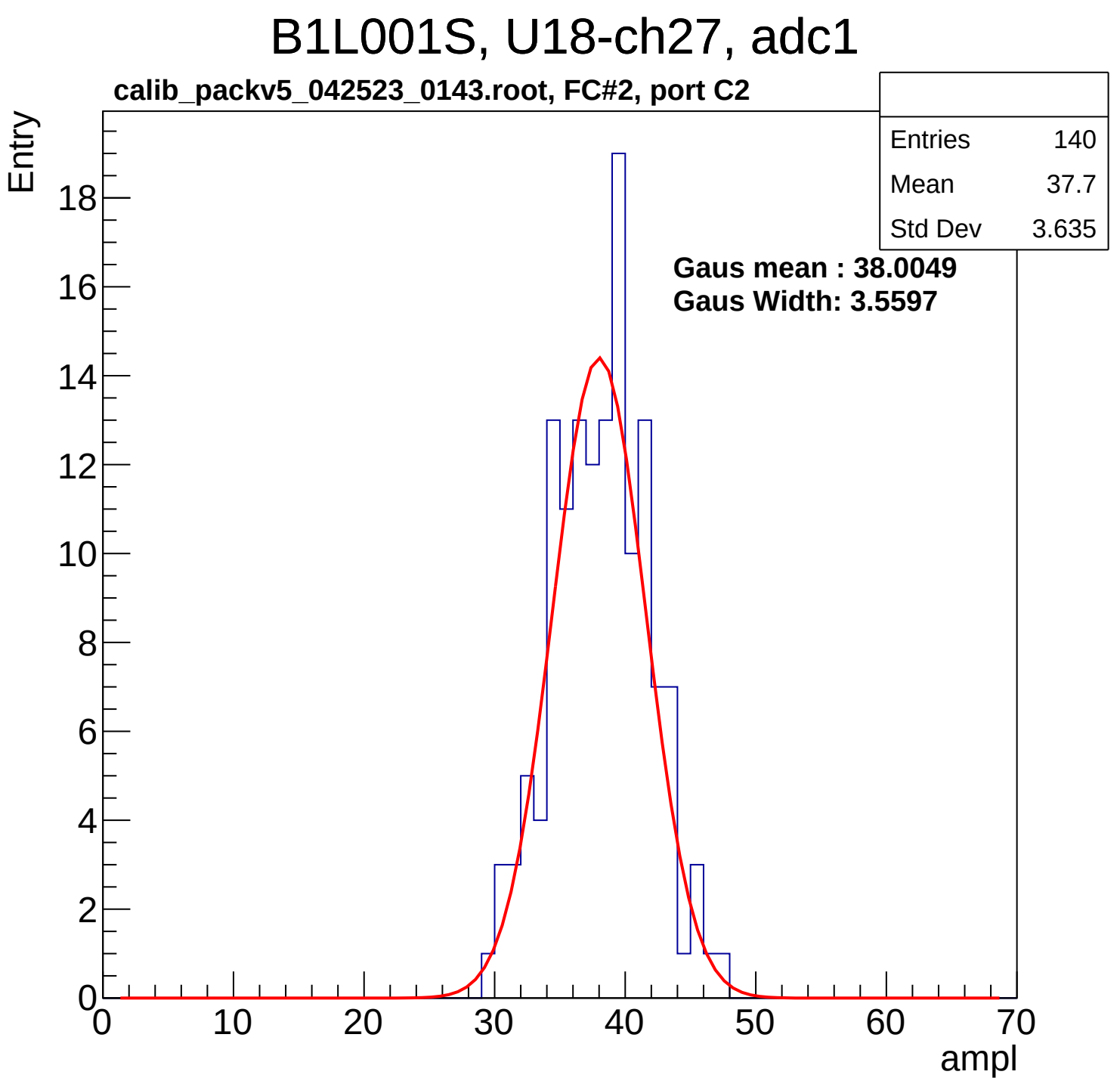

B1L001S, U18-ch26, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 119
Mean 54.32
Std Dev 3.084
Entry
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl

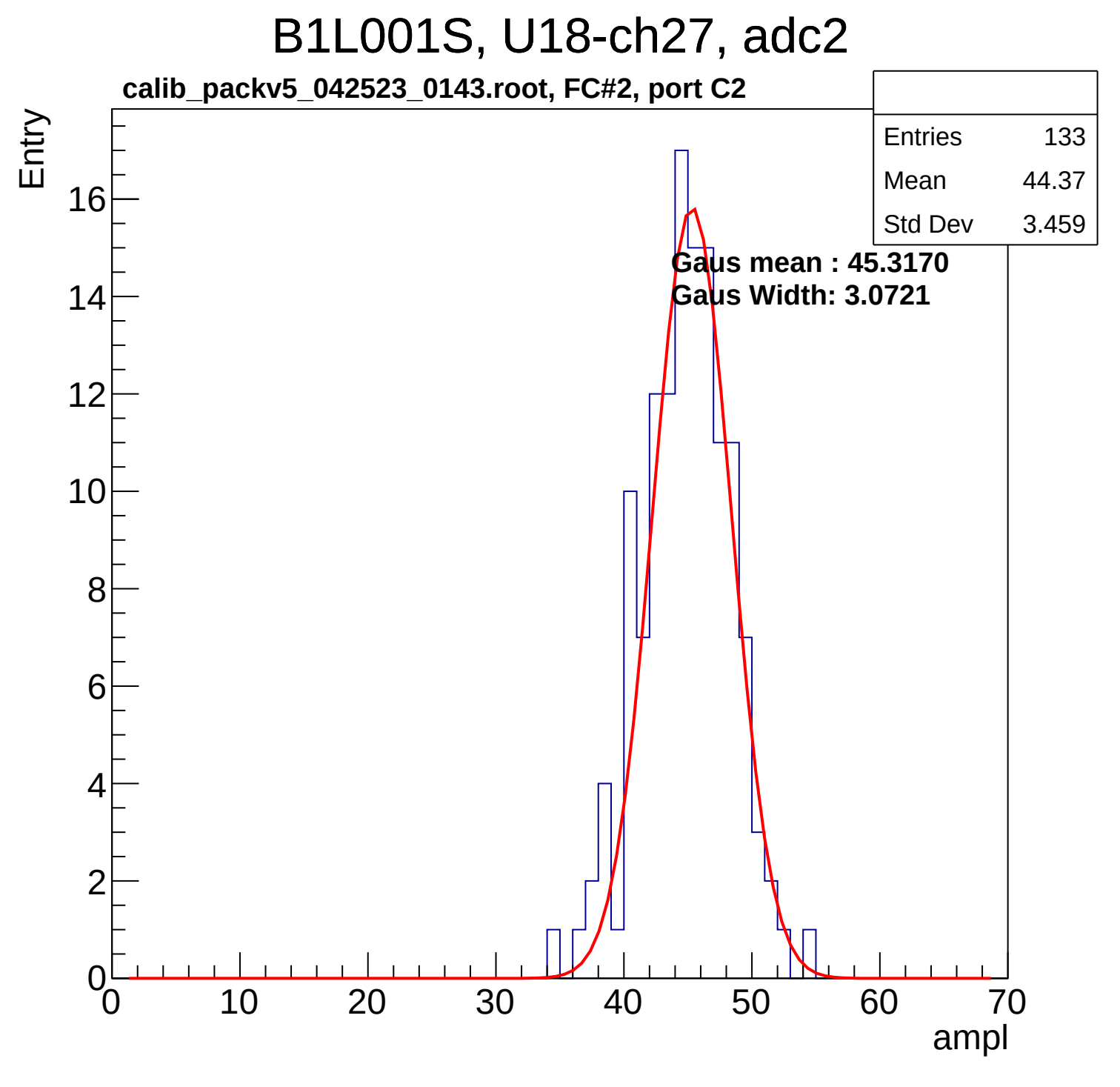

B1L001S, U18-ch26, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 100
Mean 58.99
Std Dev 6.447
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

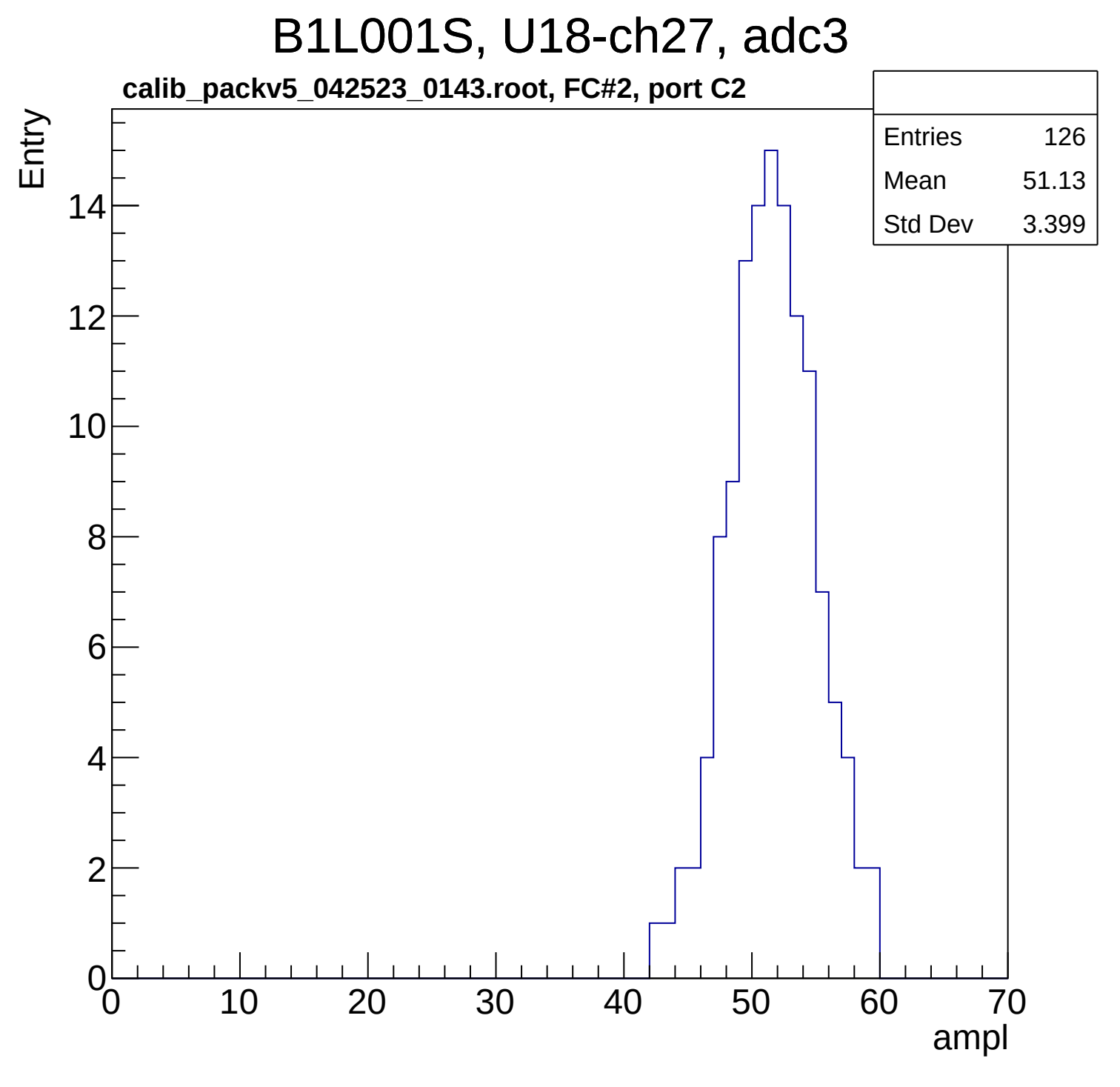

B1L001S, U18-ch26, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 25
Mean 58.84
Std Dev 12.14
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

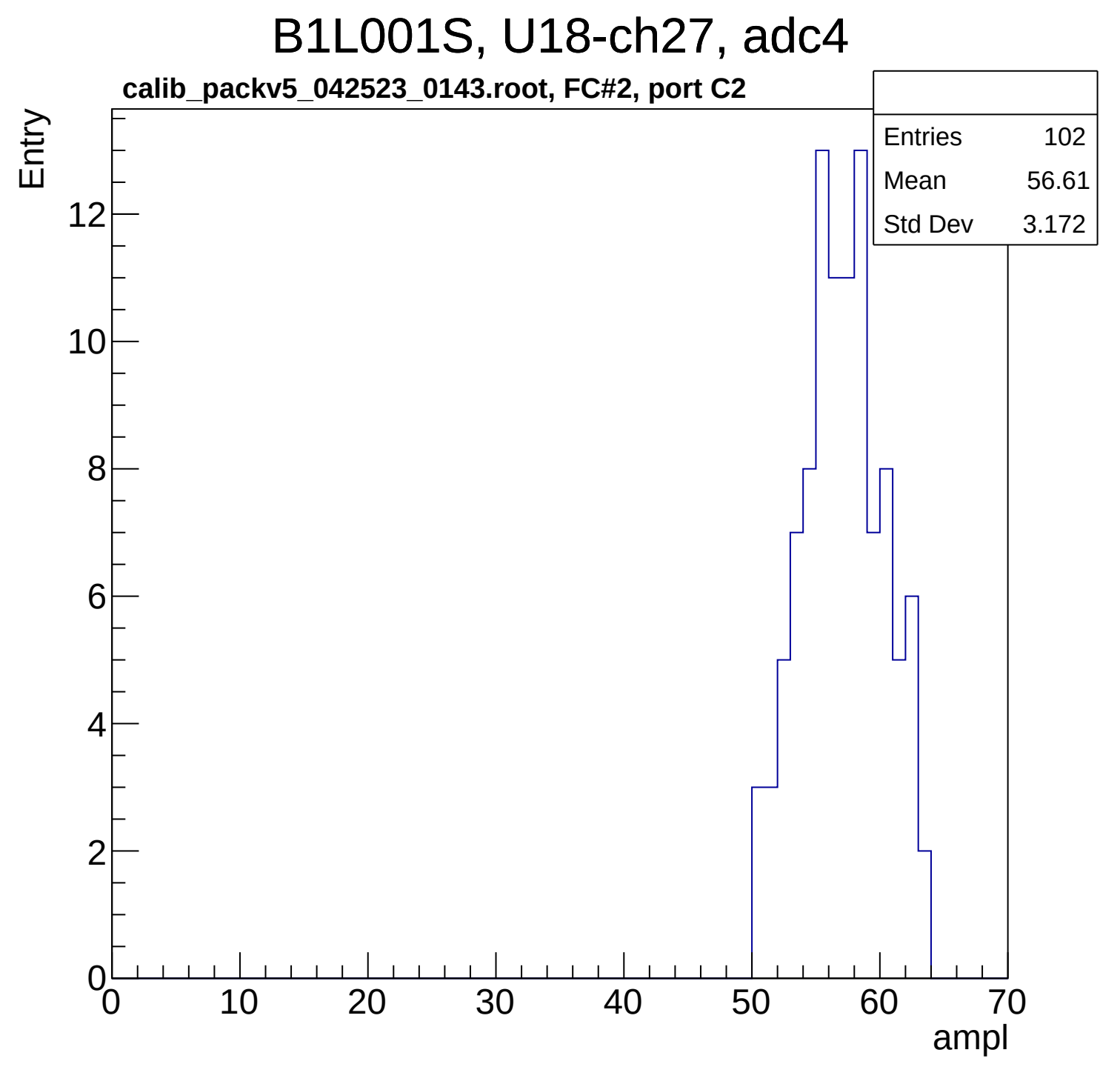

B1L001S, U18-ch26, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 22
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

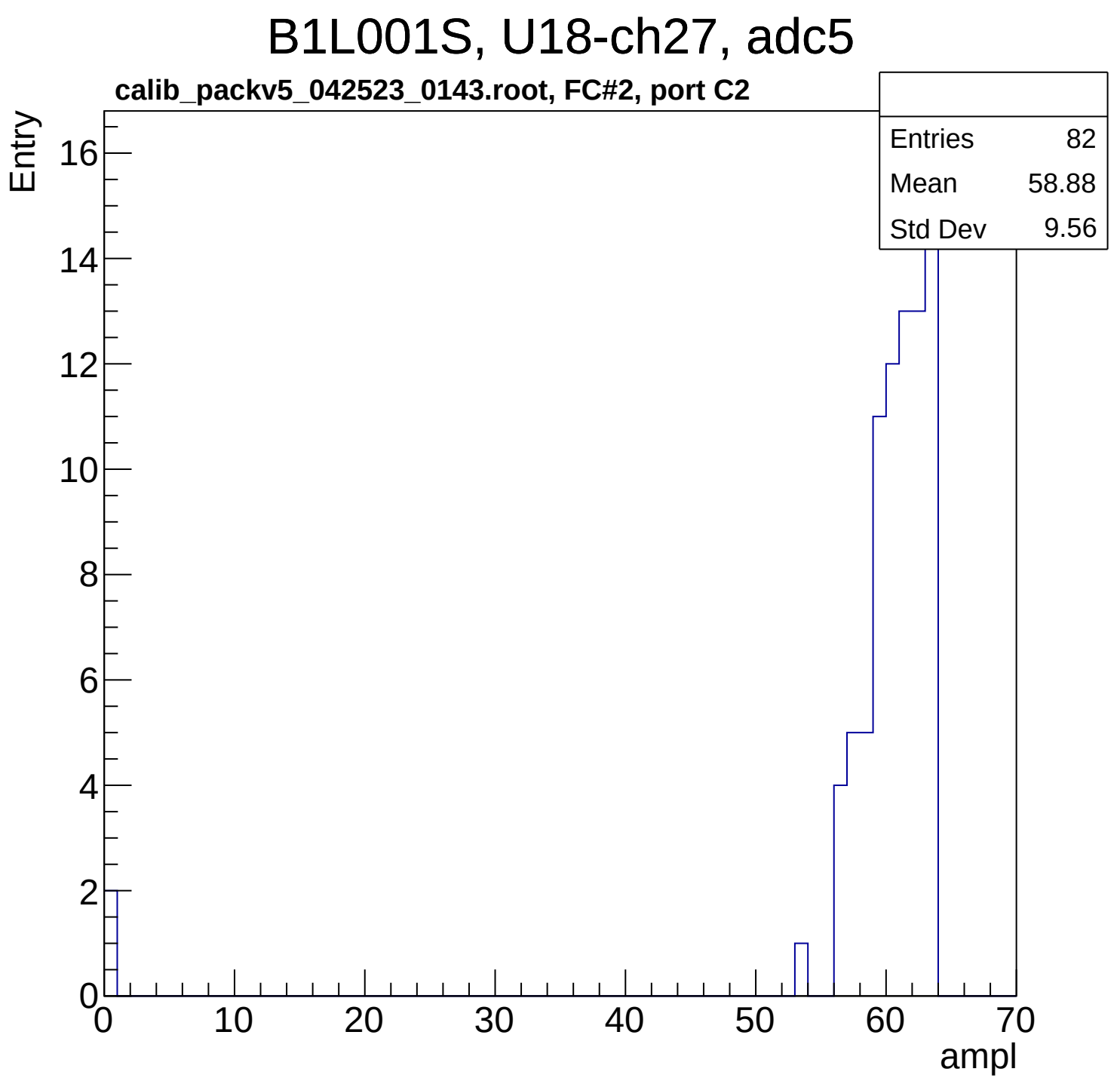

B1L001S, U18-ch27, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 137
Mean 30.76
Std Dev 4.347
Gaus mean : 31.7040
Gaus Width: 3.6002
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

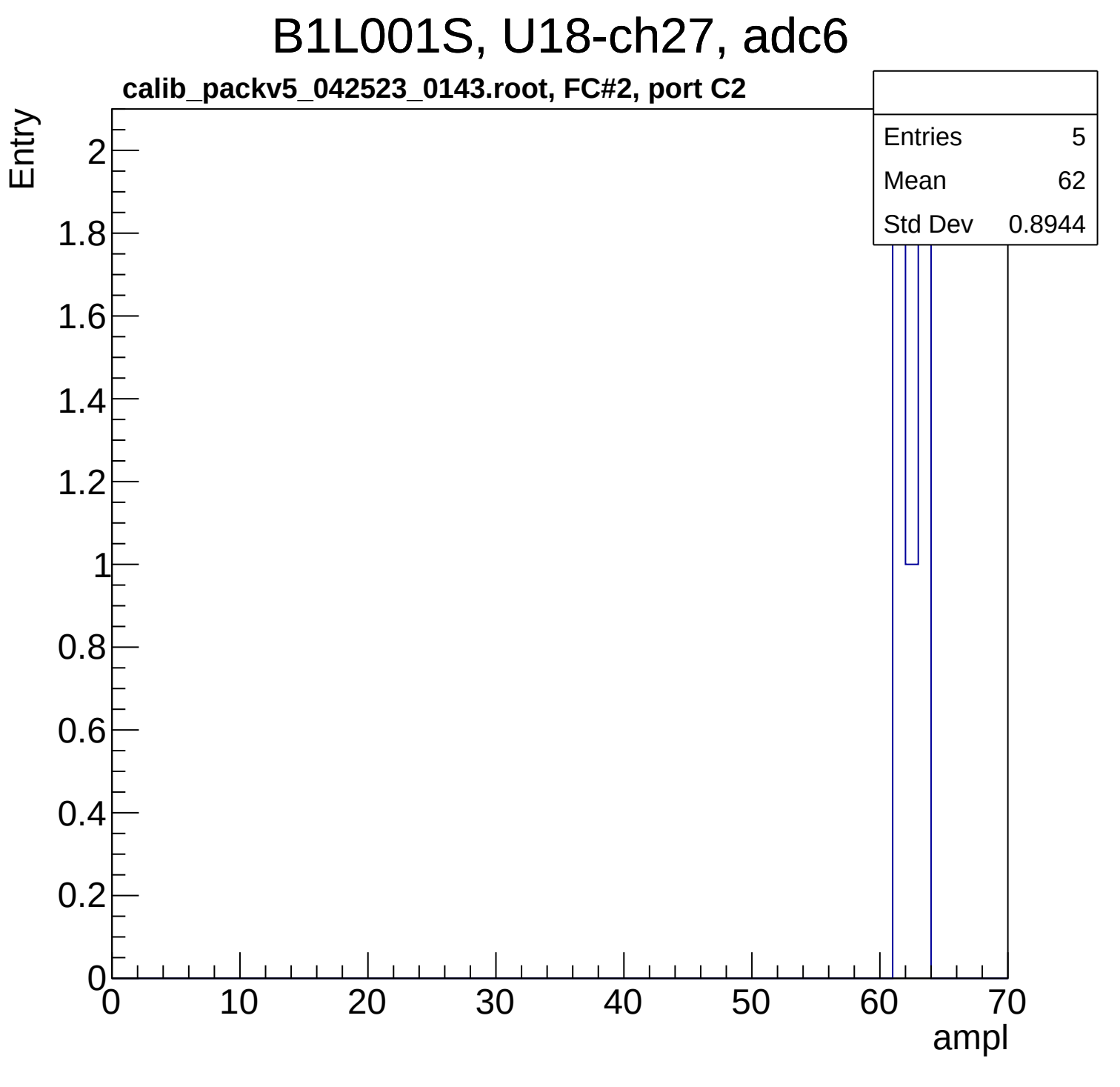

B1L001S, U18-ch27, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 140
Mean 37.7
Std Dev 3.635
Gaus mean : 38.0049
Gaus Width: 3.5597
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

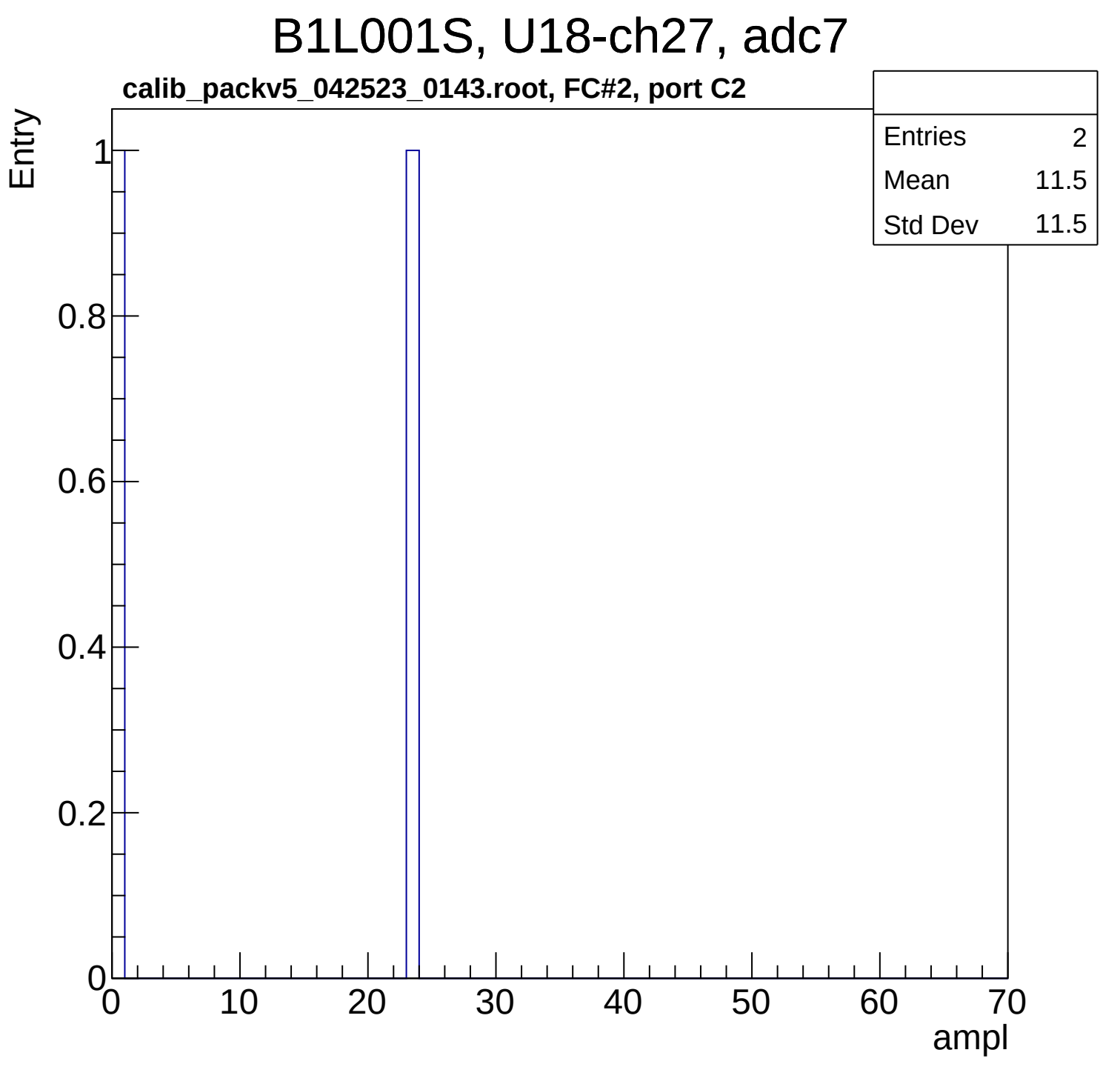

B1L001S, U18-ch27, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 133
Mean 44.37
Std Dev 3.459
Gaus mean : 45.3170
Gaus Width: 3.0721
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

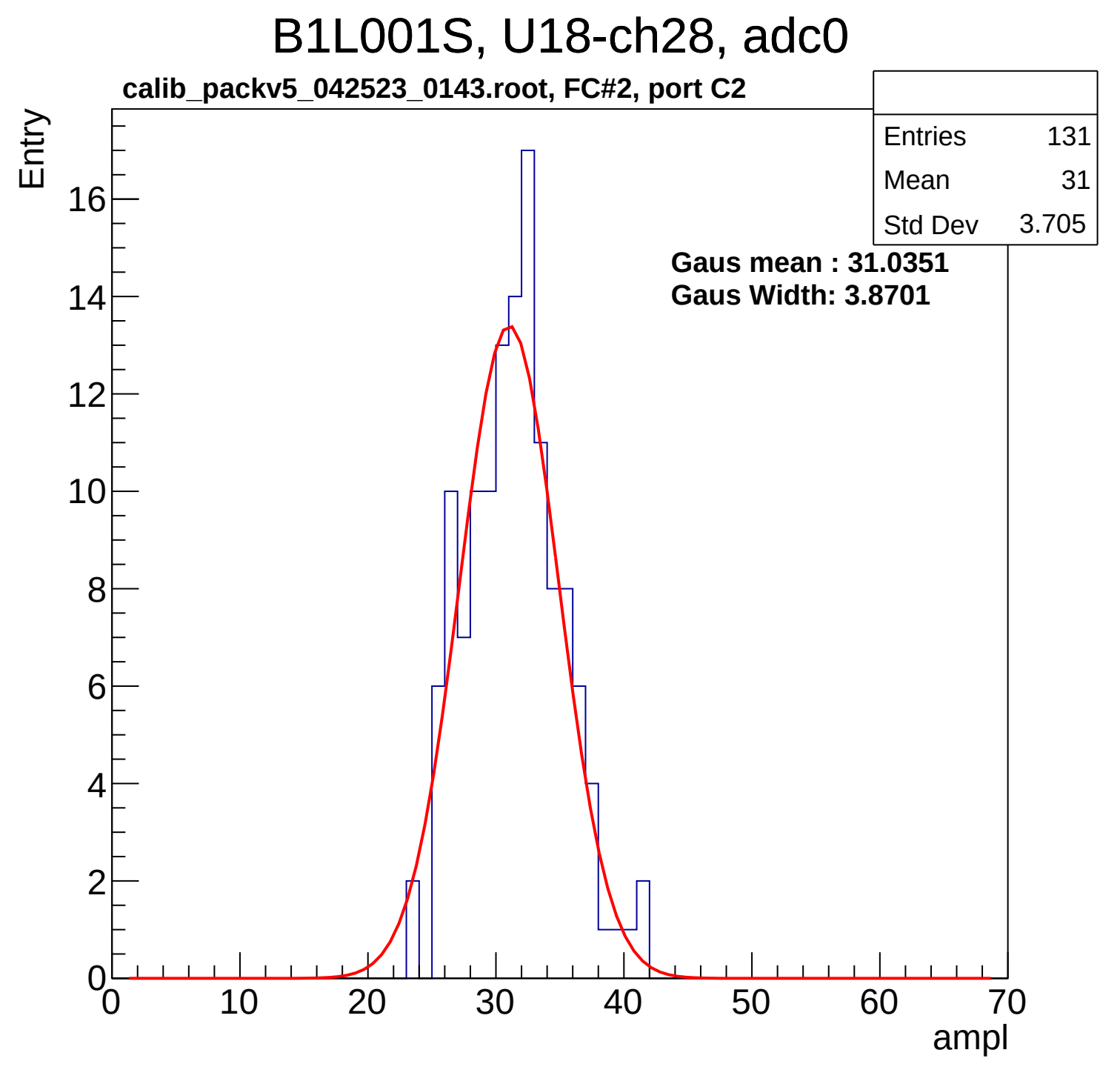

B1L001S, U18-ch27, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 126
Mean 51.13
Std Dev 3.399
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

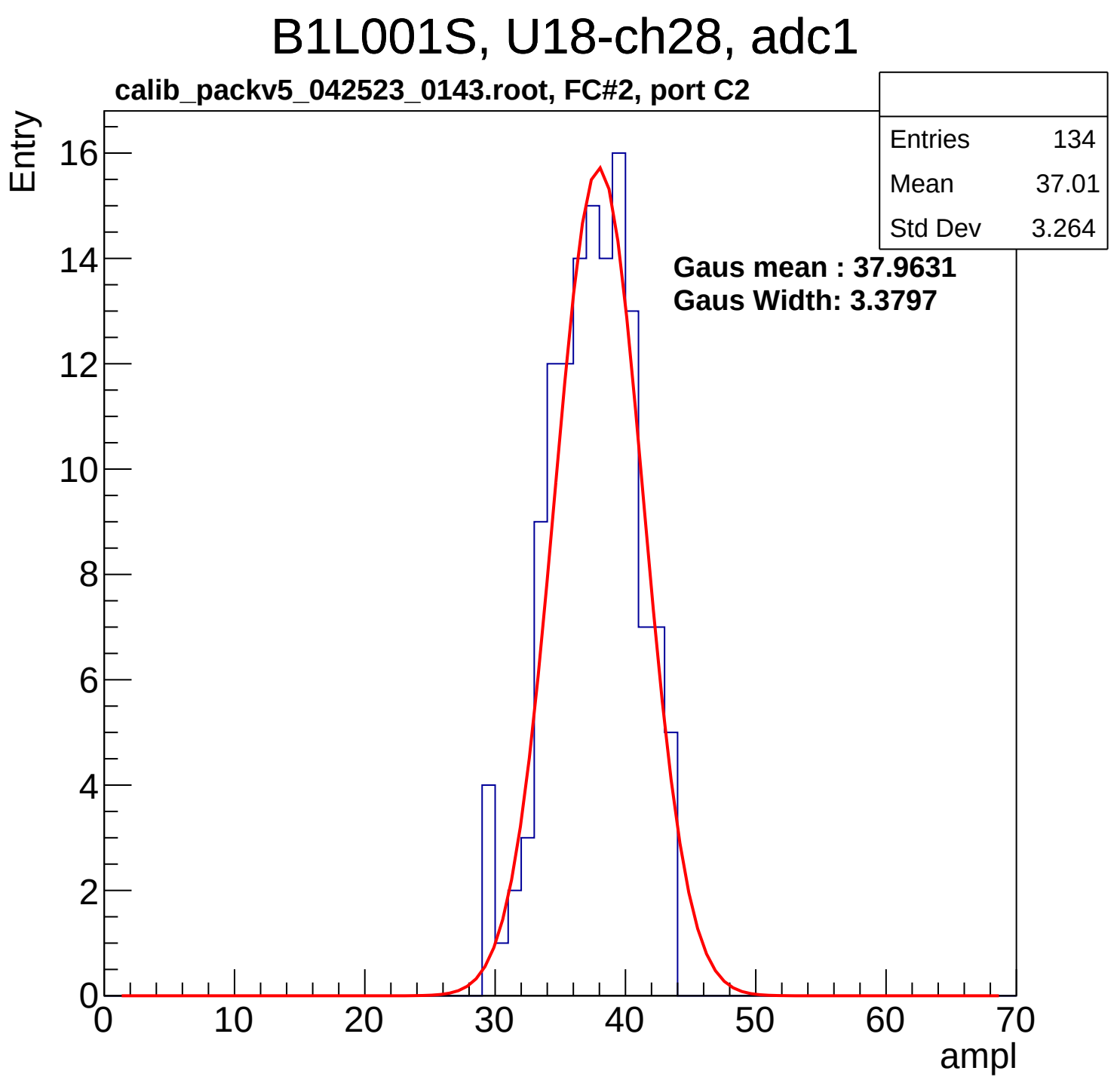

B1L001S, U18-ch27, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 102
Mean 56.61
Std Dev 3.172
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl

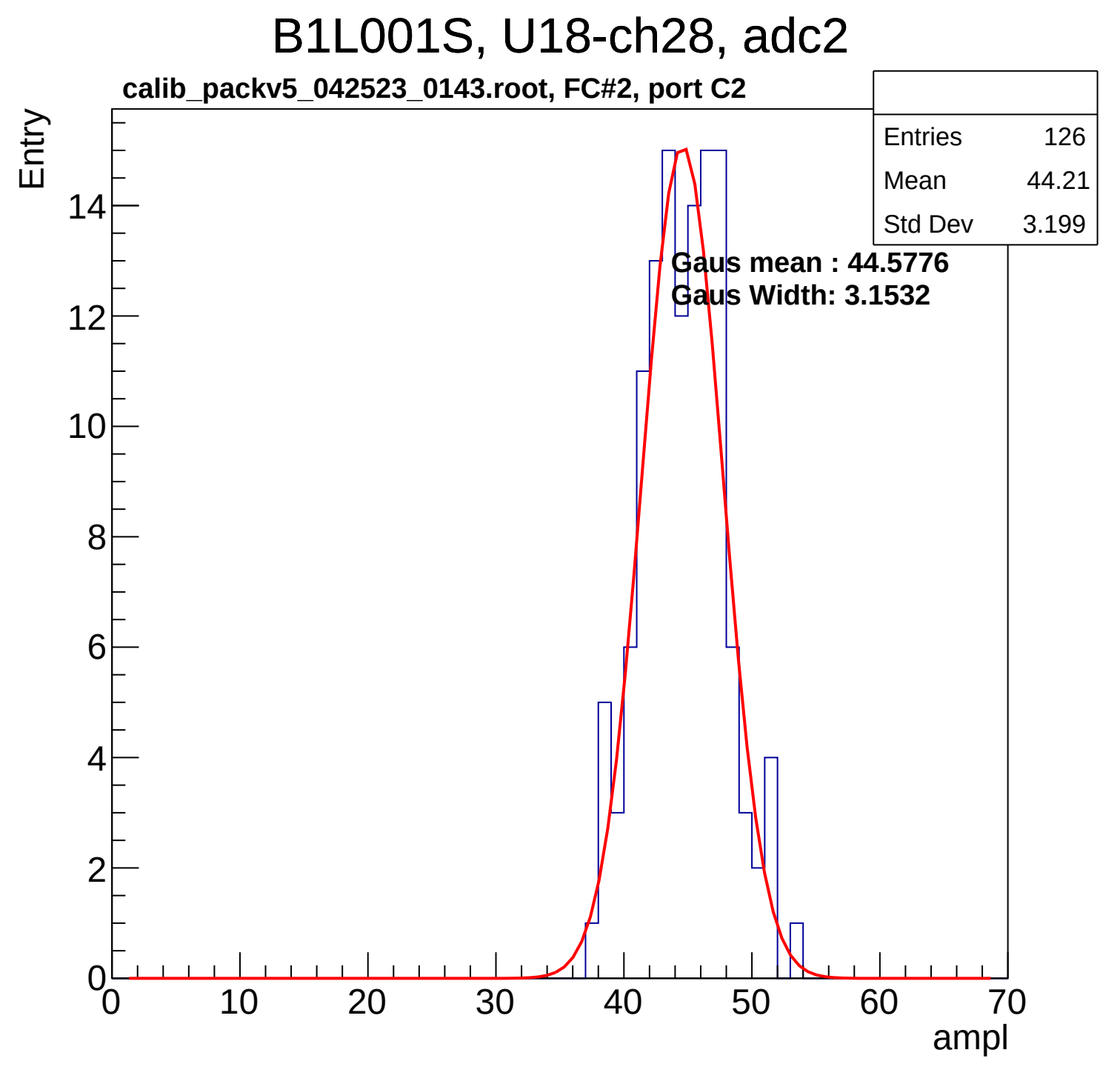

B1L001S, U18-ch27, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 82
Mean 58.88
Std Dev 9.56
Entry
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl

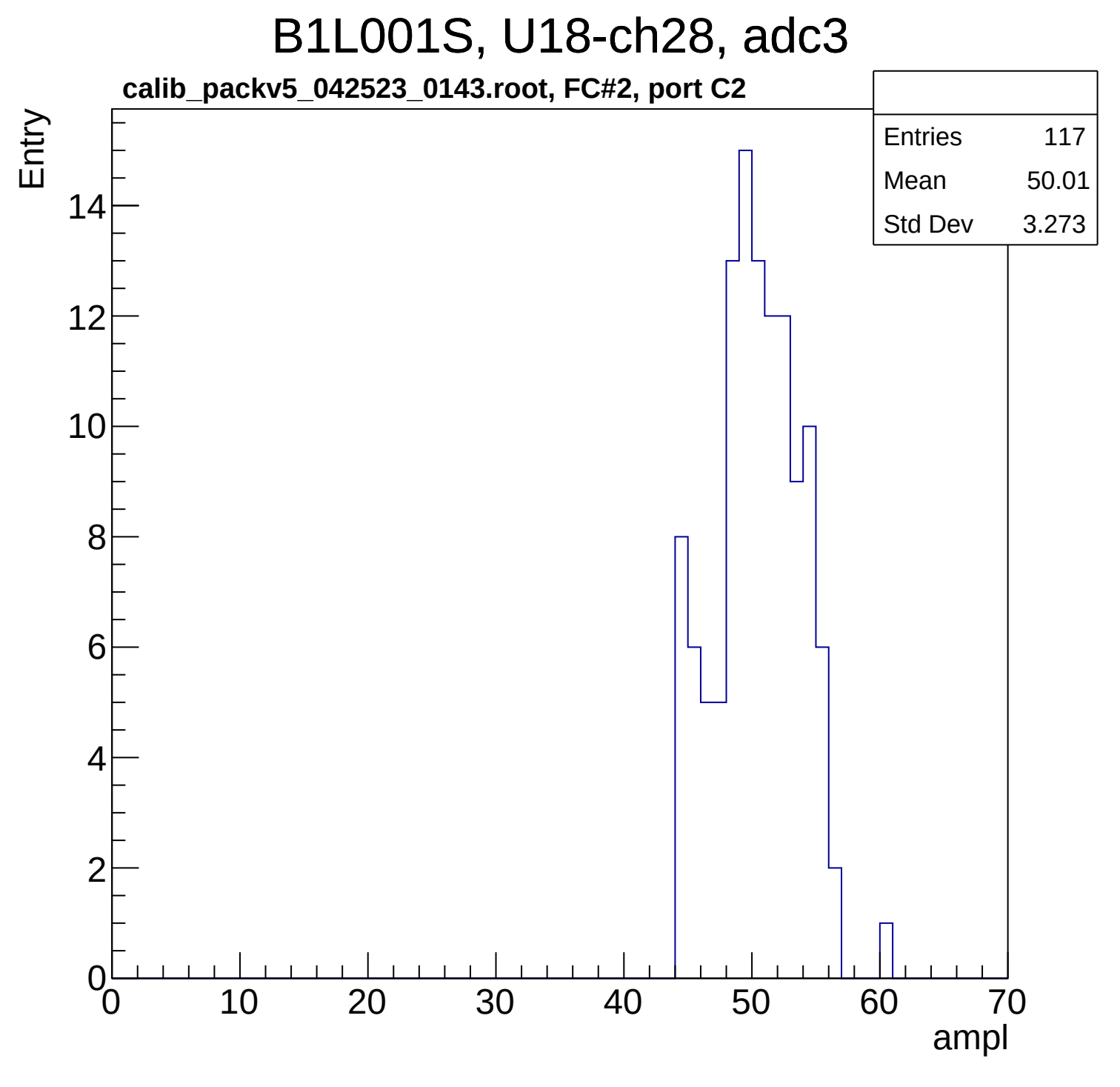

B1L001S, U18-ch27, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 5
Mean 62
Std Dev 0.8944
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

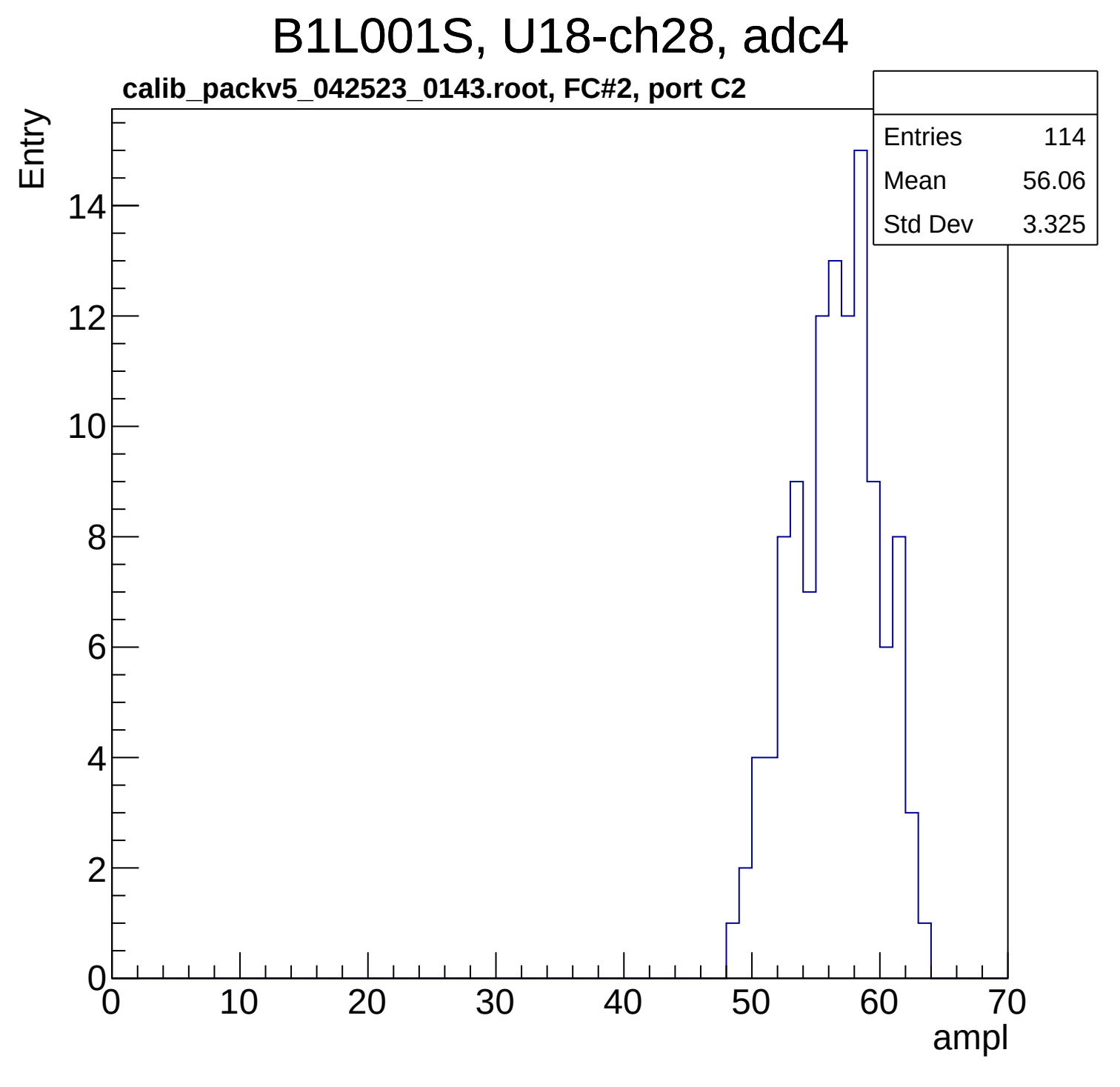

B1L001S, U18-ch27, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 11.5
Std Dev 11.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

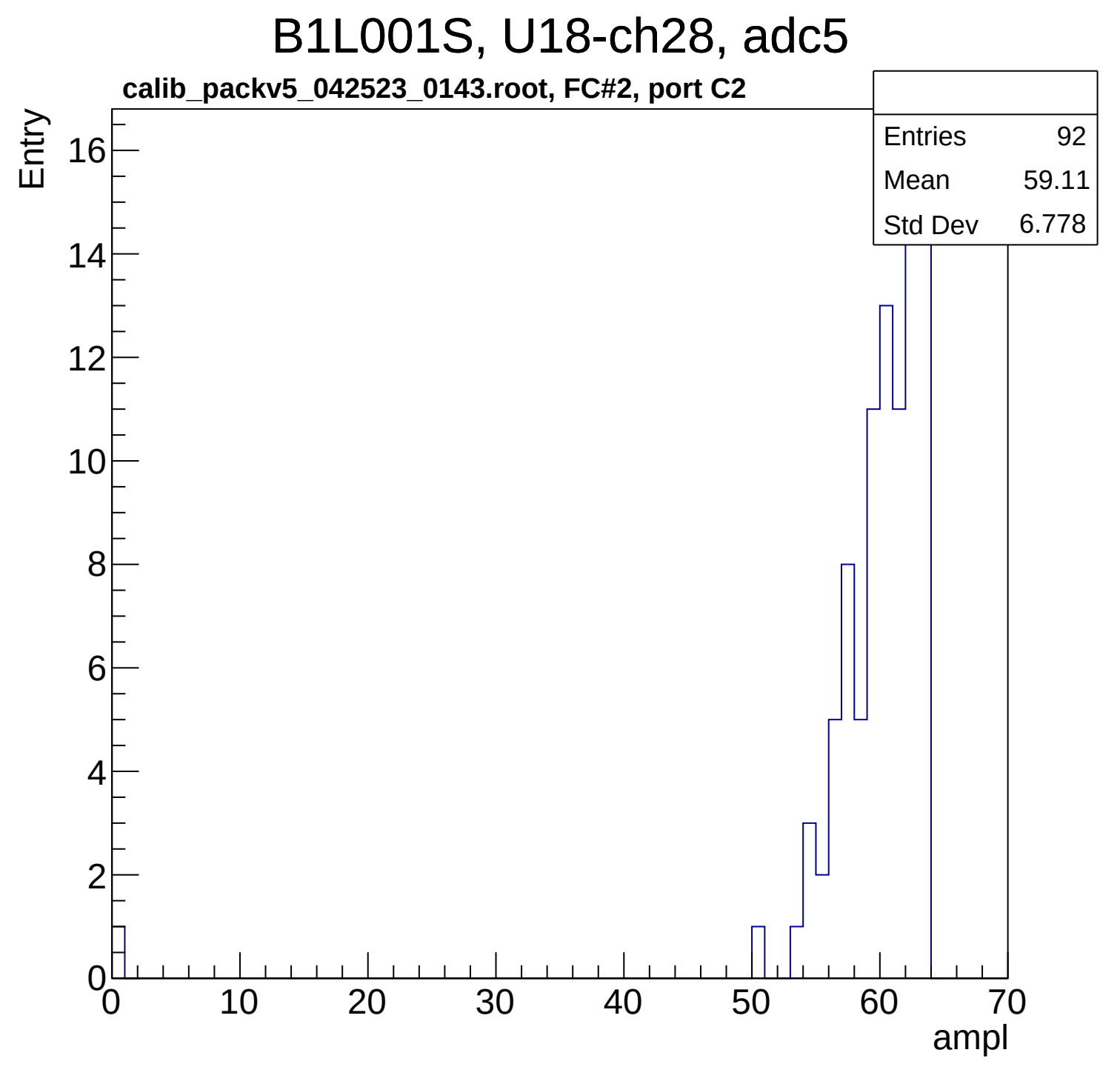

B1L001S, U18-ch28, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 131
Mean 31
Std Dev 3.705
Gaus mean : 31.0351
Gaus Width: 3.8701
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

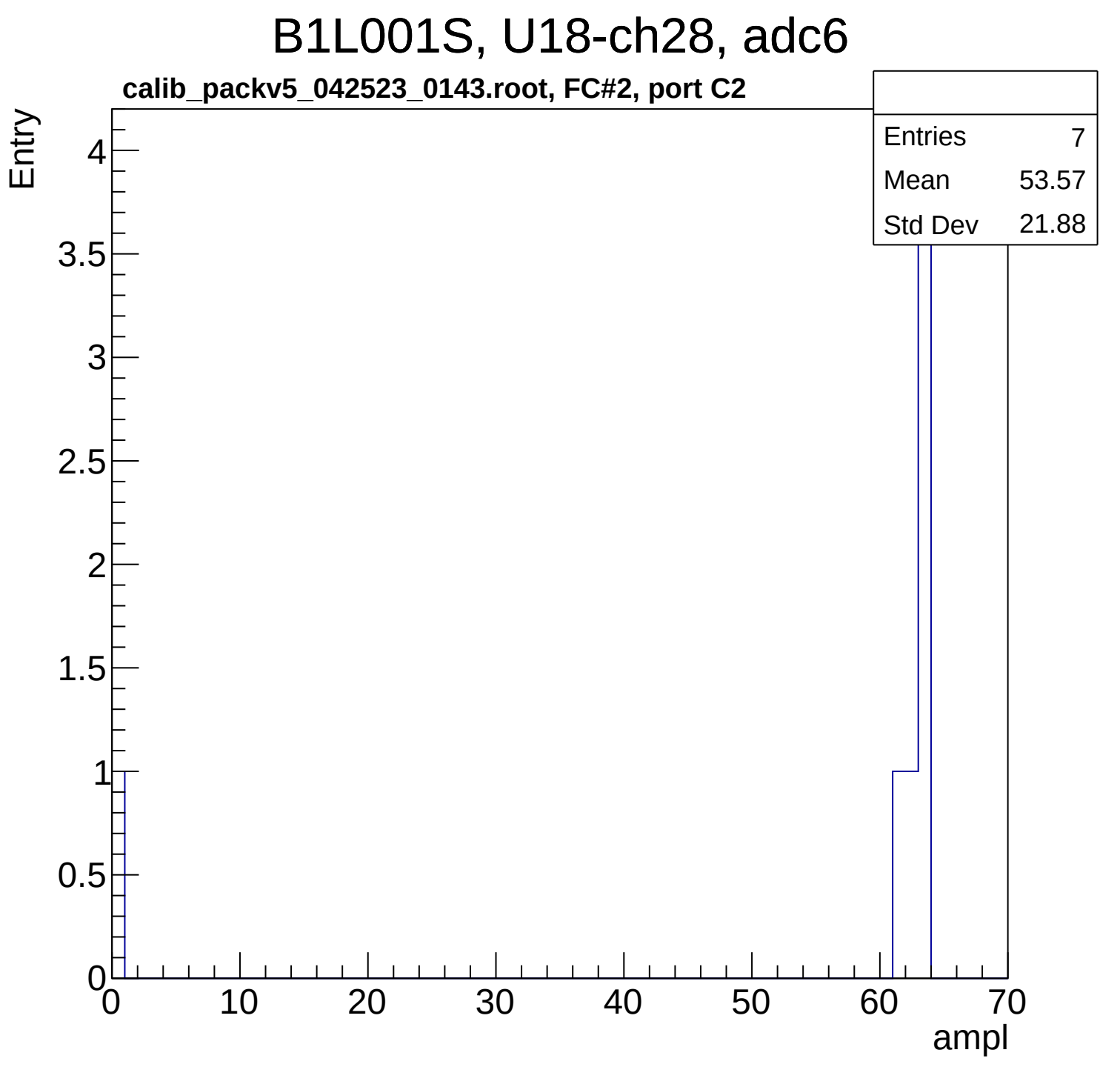

B1L001S, U18-ch28, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 134
Mean 37.01
Std Dev 3.264
Gaus mean : 37.9631
Gaus Width: 3.3797
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

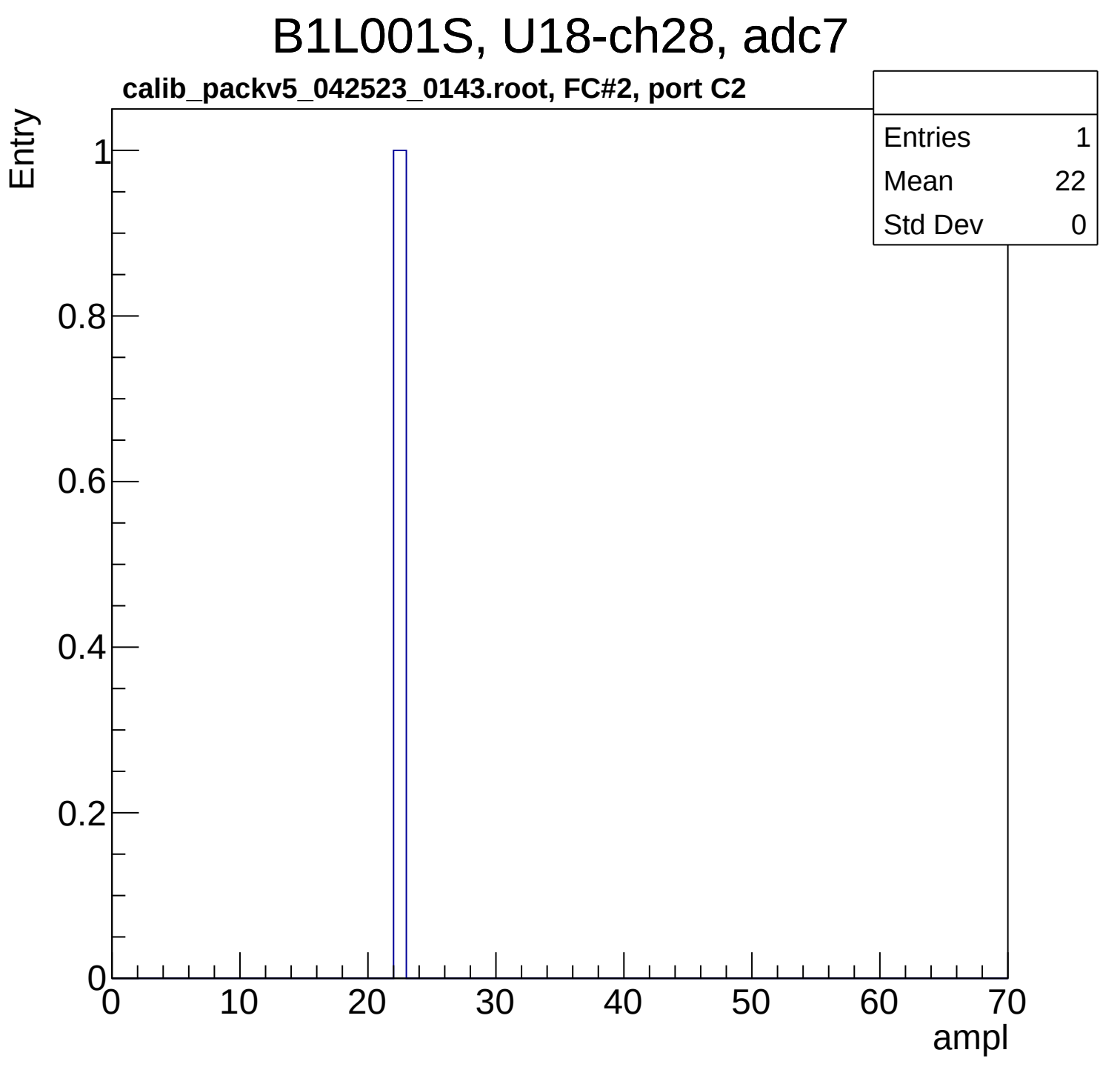

B1L001S, U18-ch28, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 126
Mean 44.21
Std Dev 3.199
Gaus mean : 44.5776
Gaus Width: 3.1532
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

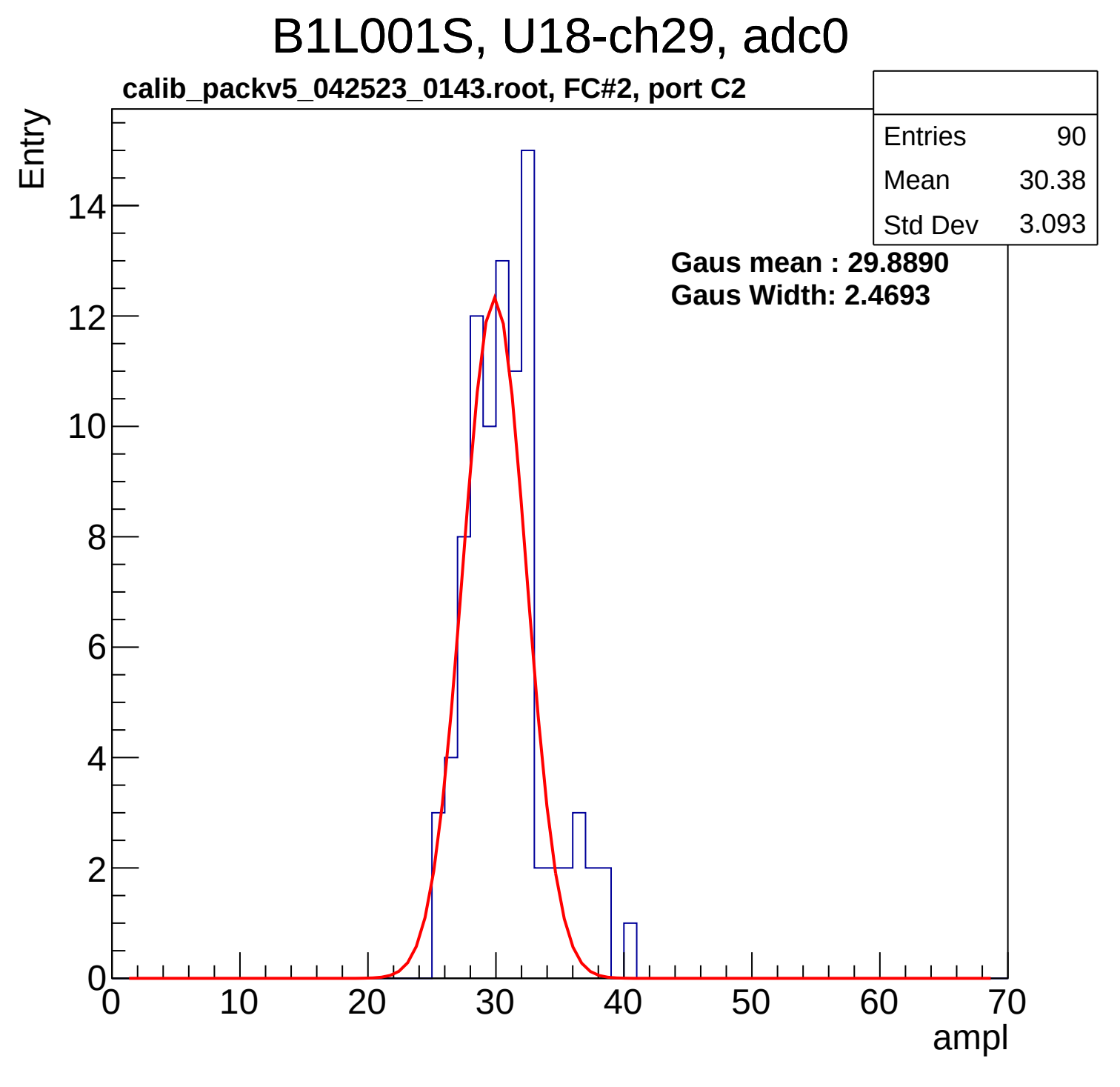

B1L001S, U18-ch28, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 117
Mean 50.01
Std Dev 3.273
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl

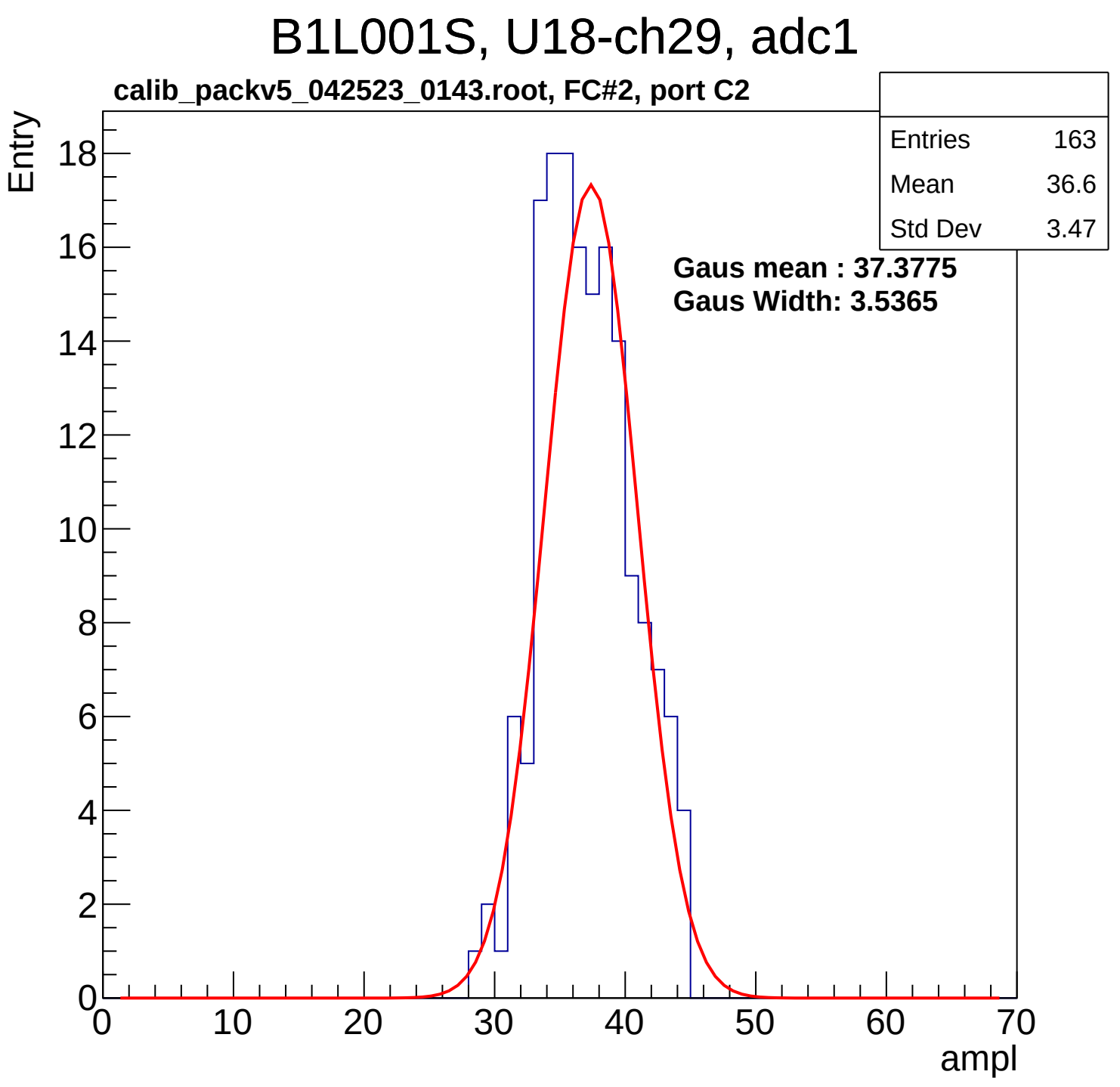

B1L001S, U18-ch28, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 114
Mean 56.06
Std Dev 3.325
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl

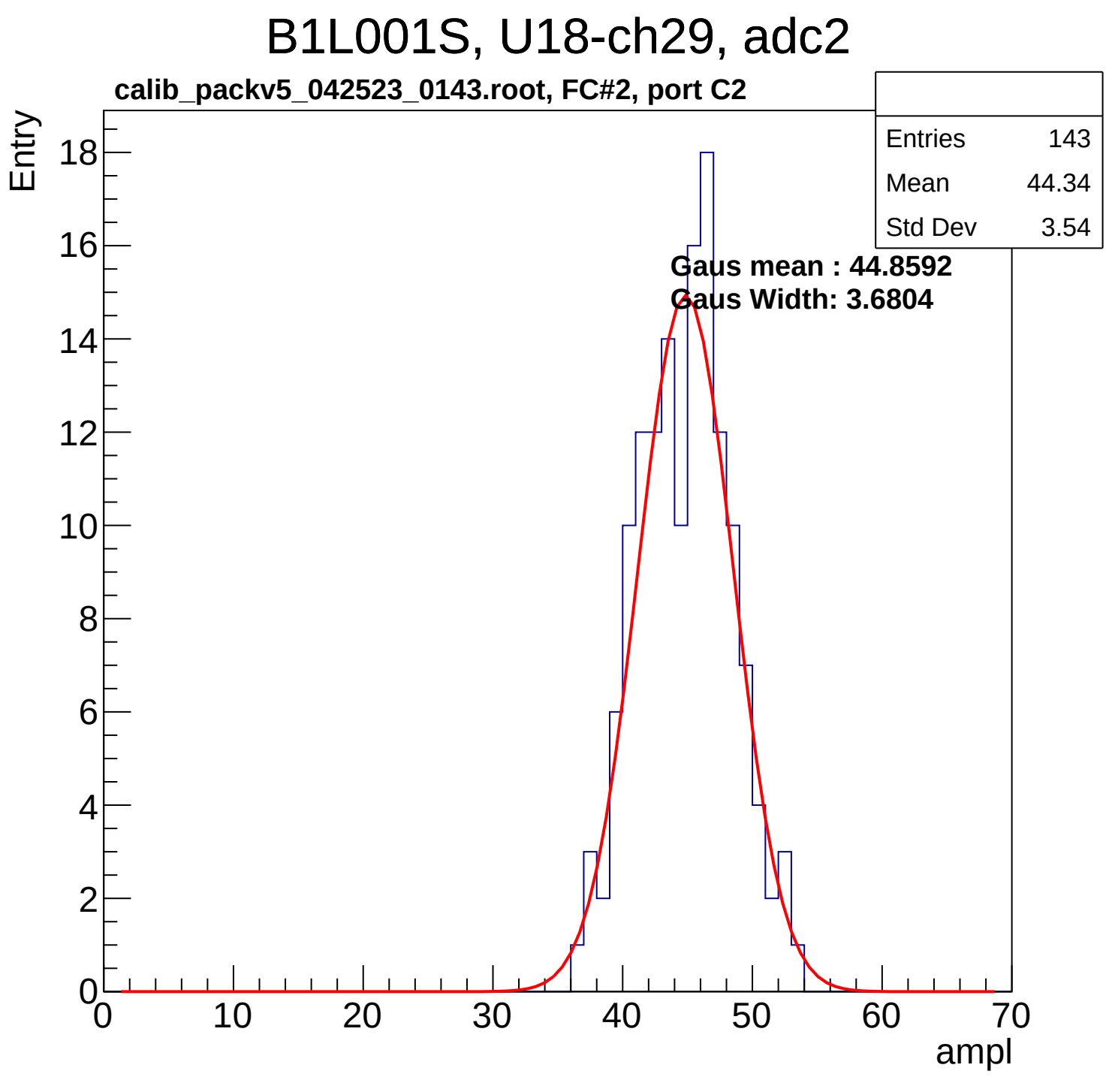

B1L001S, U18-ch28, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 92
Mean 59.11
Std Dev 6.778
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

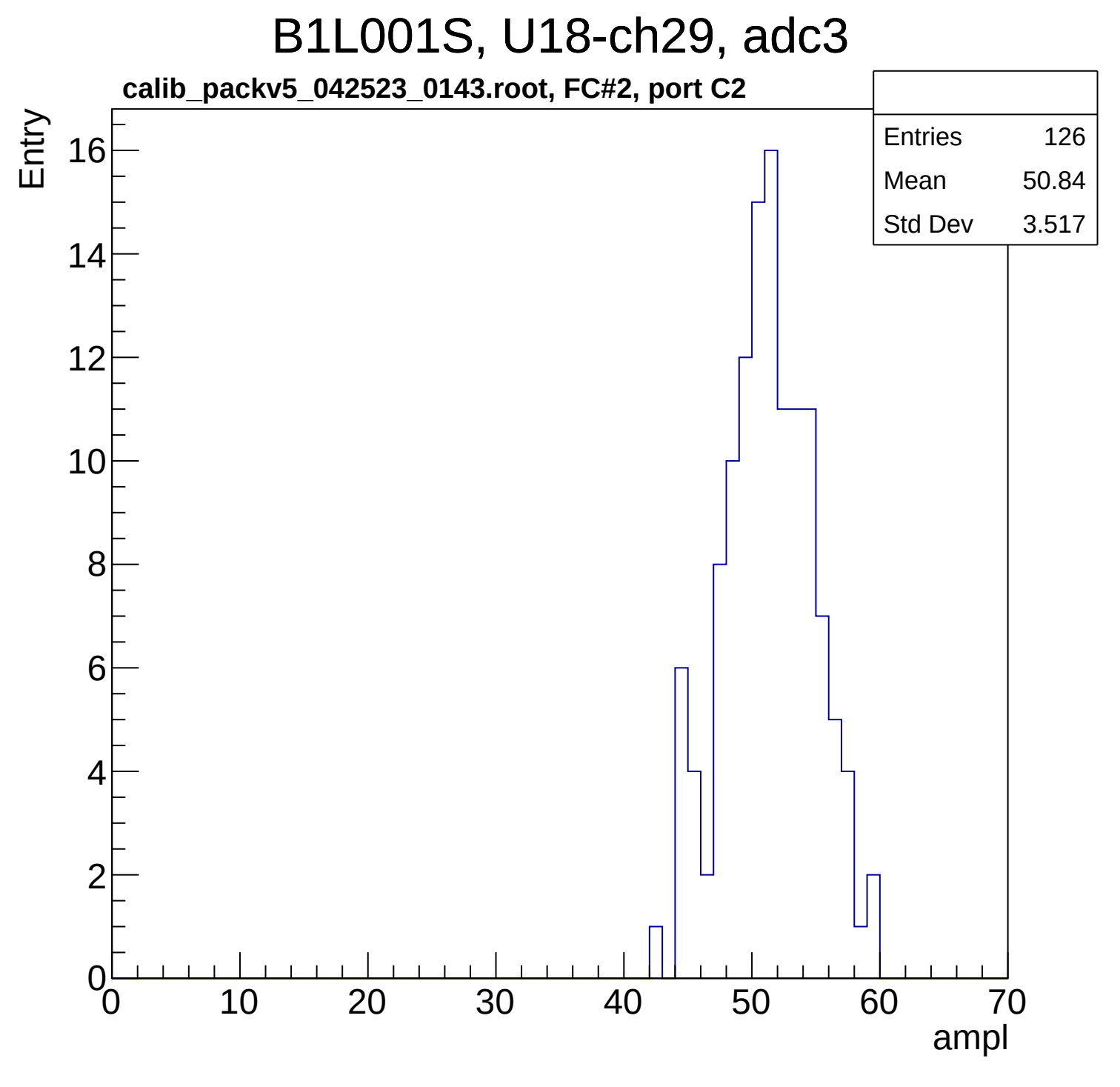

B1L001S, U18-ch28, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 7
Mean 53.57
Std Dev 21.88
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

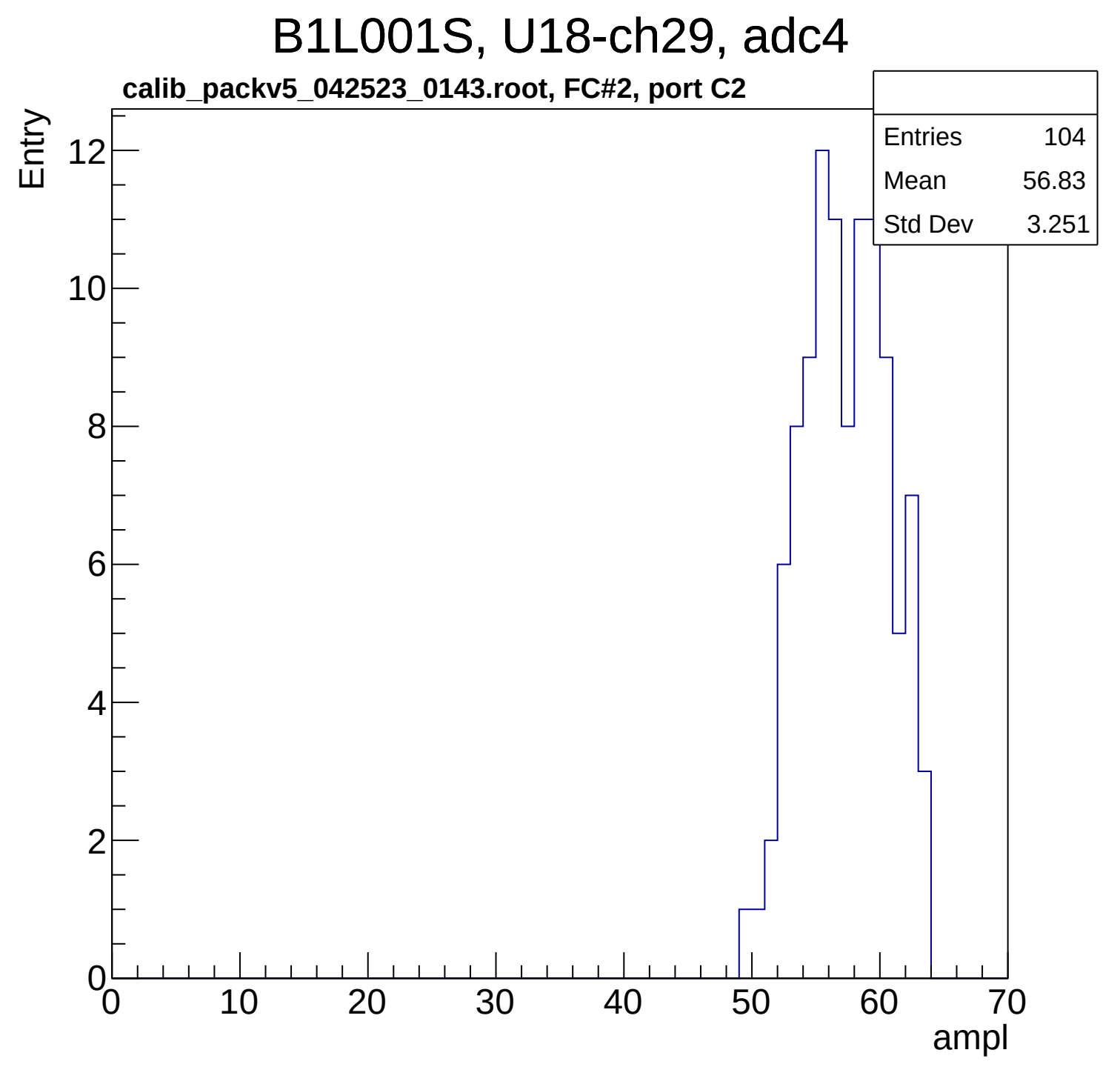

B1L001S, U18-ch28, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 22
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

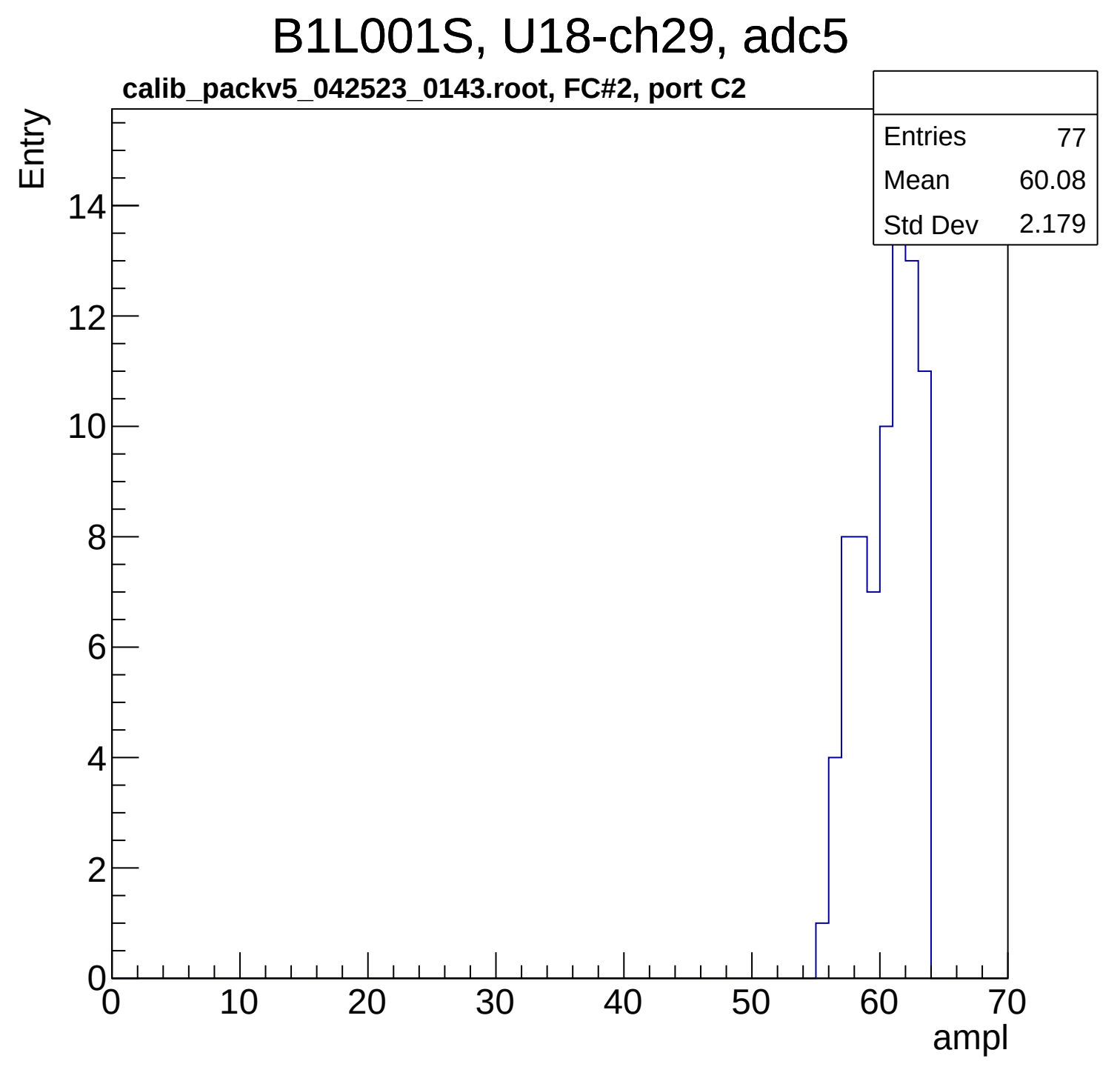

B1L001S, U18-ch29, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 90
Mean 30.38
Std Dev 3.093
Gaus mean : 29.8890
Gaus Width: 2.4693
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

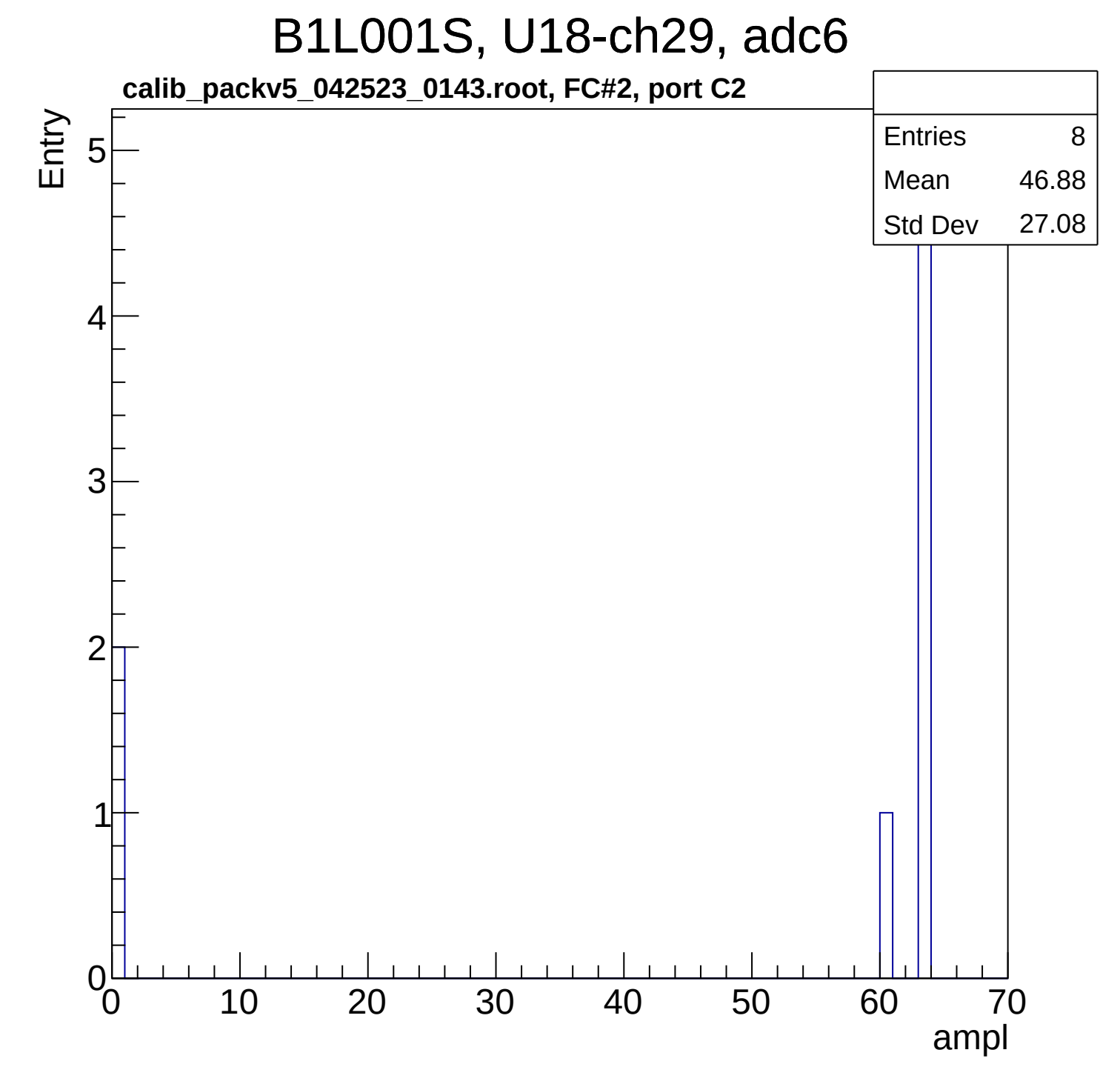

B1L001S, U18-ch29, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 163
Mean 36.6
Std Dev 3.47
Gaus mean : 37.3775
Gaus Width: 3.5365
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

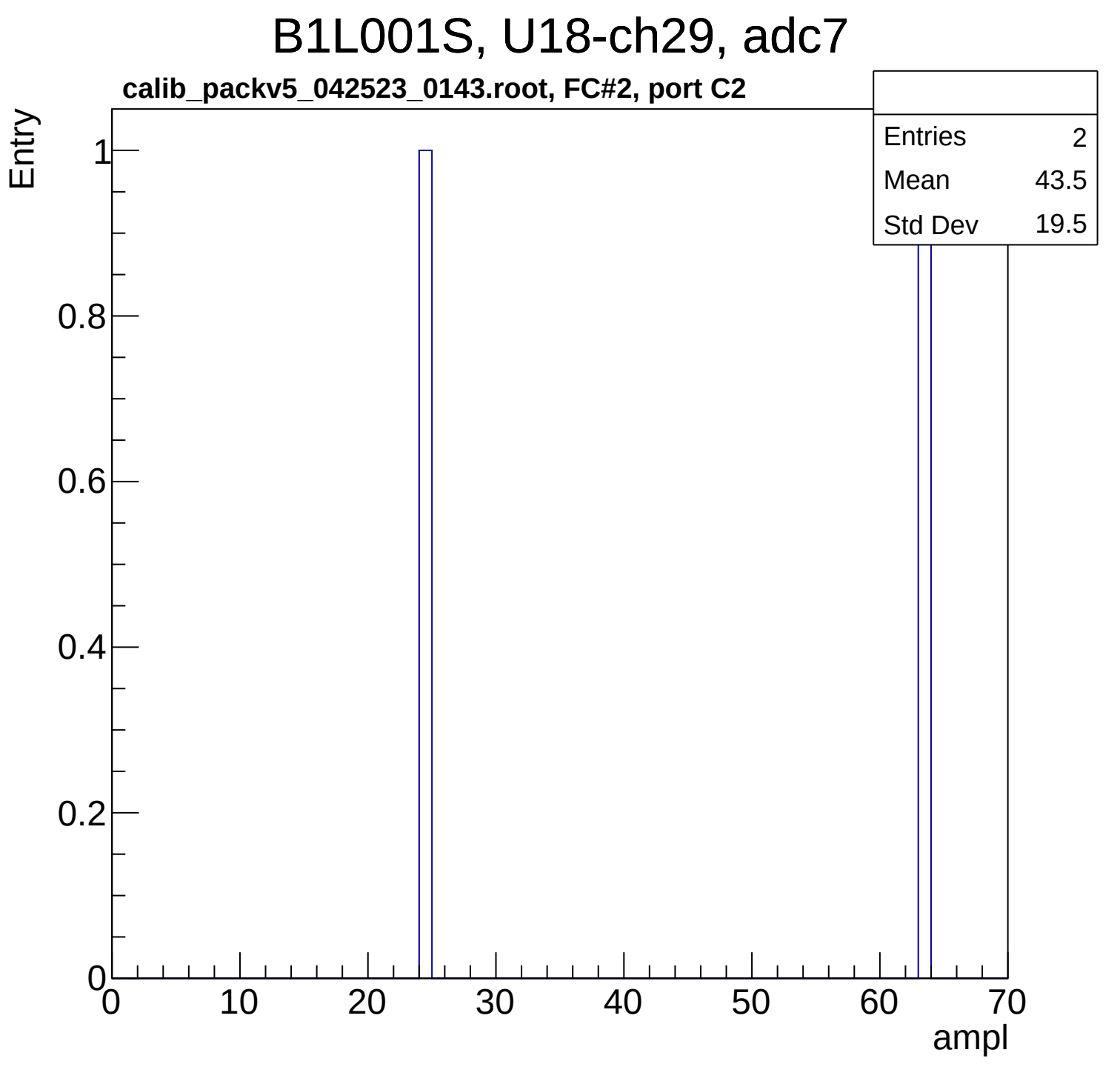

B1L001S, U18-ch29, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 143
Mean 44.34
Std Dev 3.54
Gaus mean : 44.8592
Gaus Width: 3.6804
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

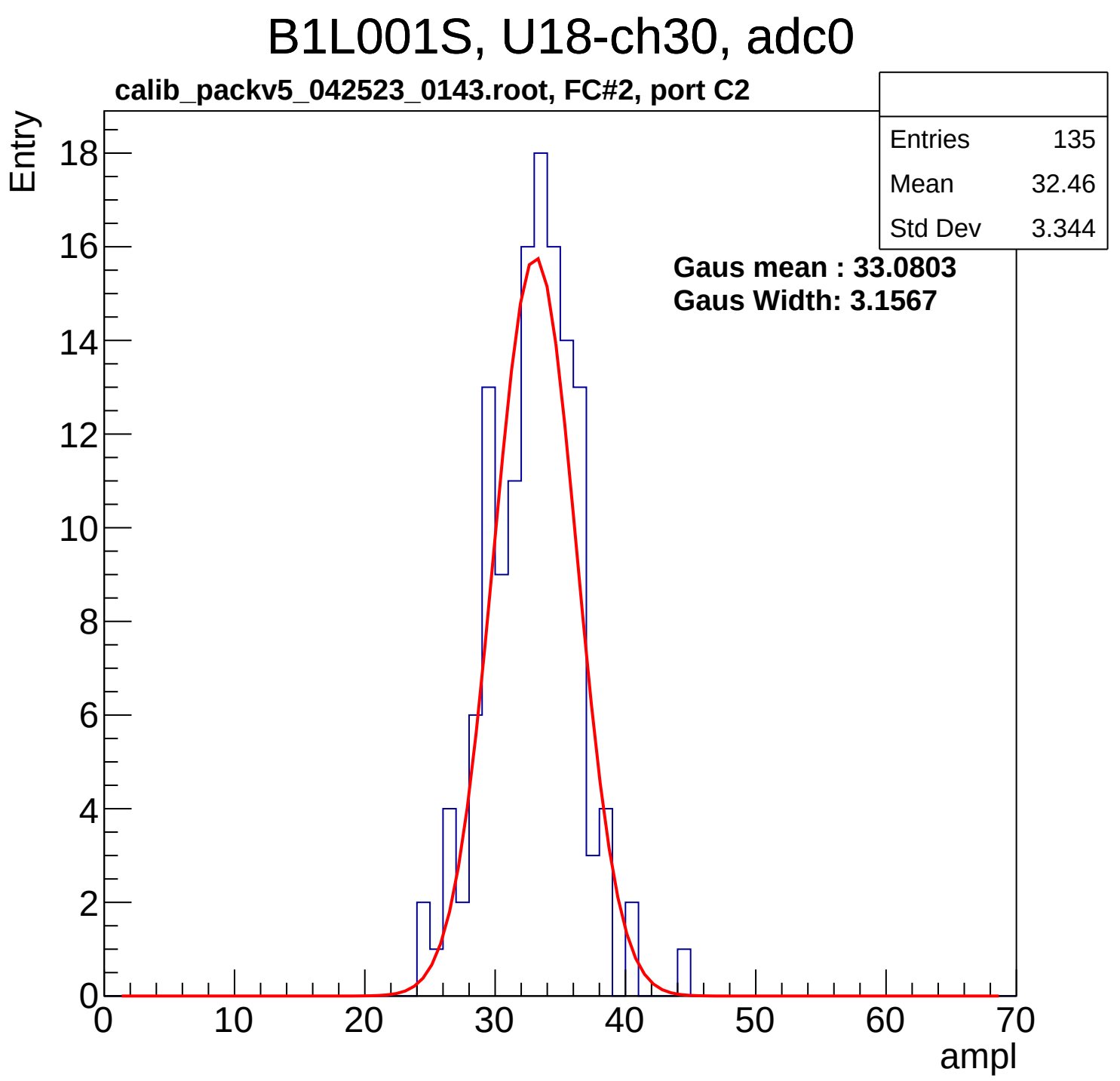

B1L001S, U18-ch29, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 126
Mean 50.84
Std Dev 3.517
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

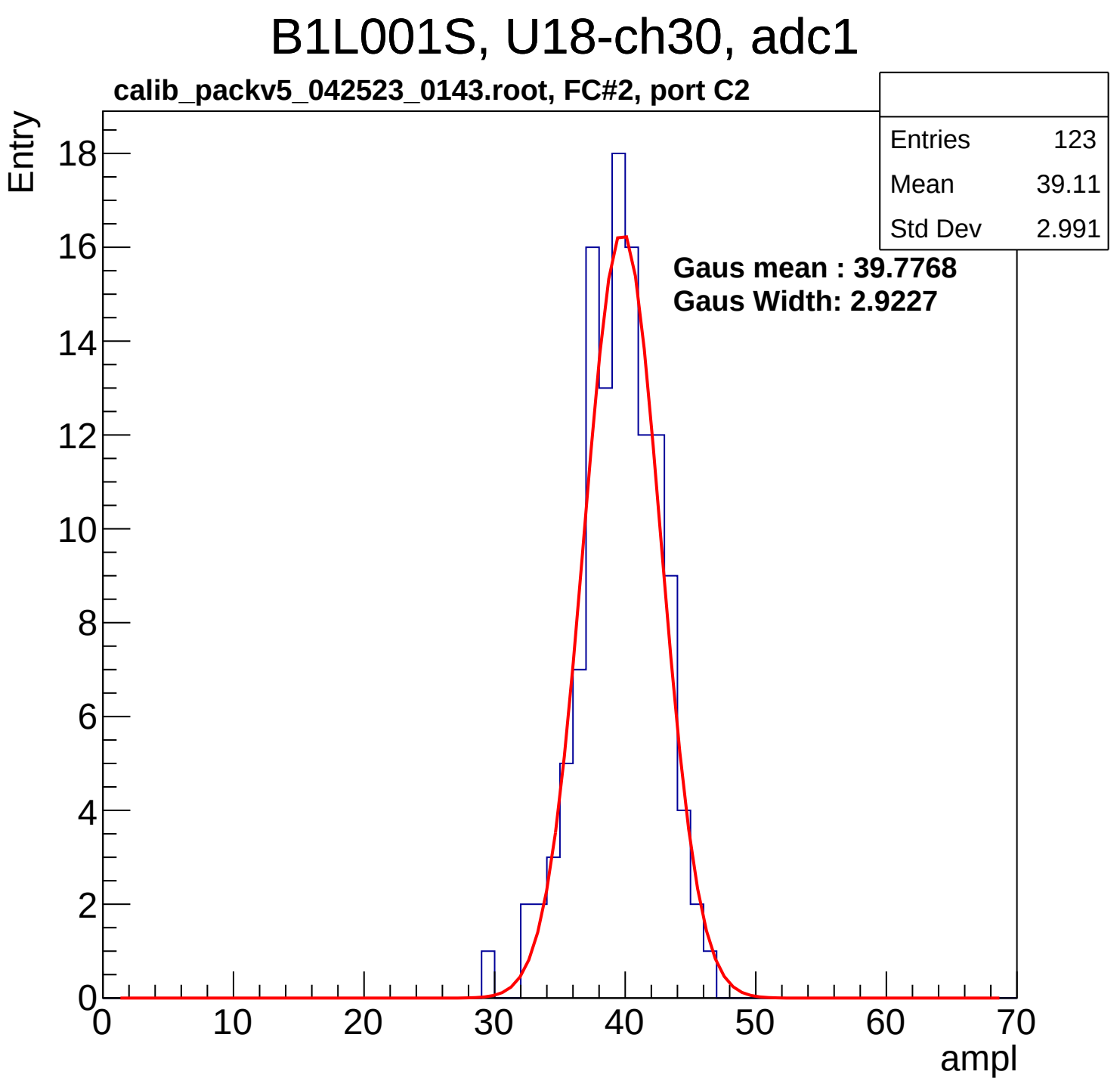

B1L001S, U18-ch29, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 104
Mean 56.83
Std Dev 3.251
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70

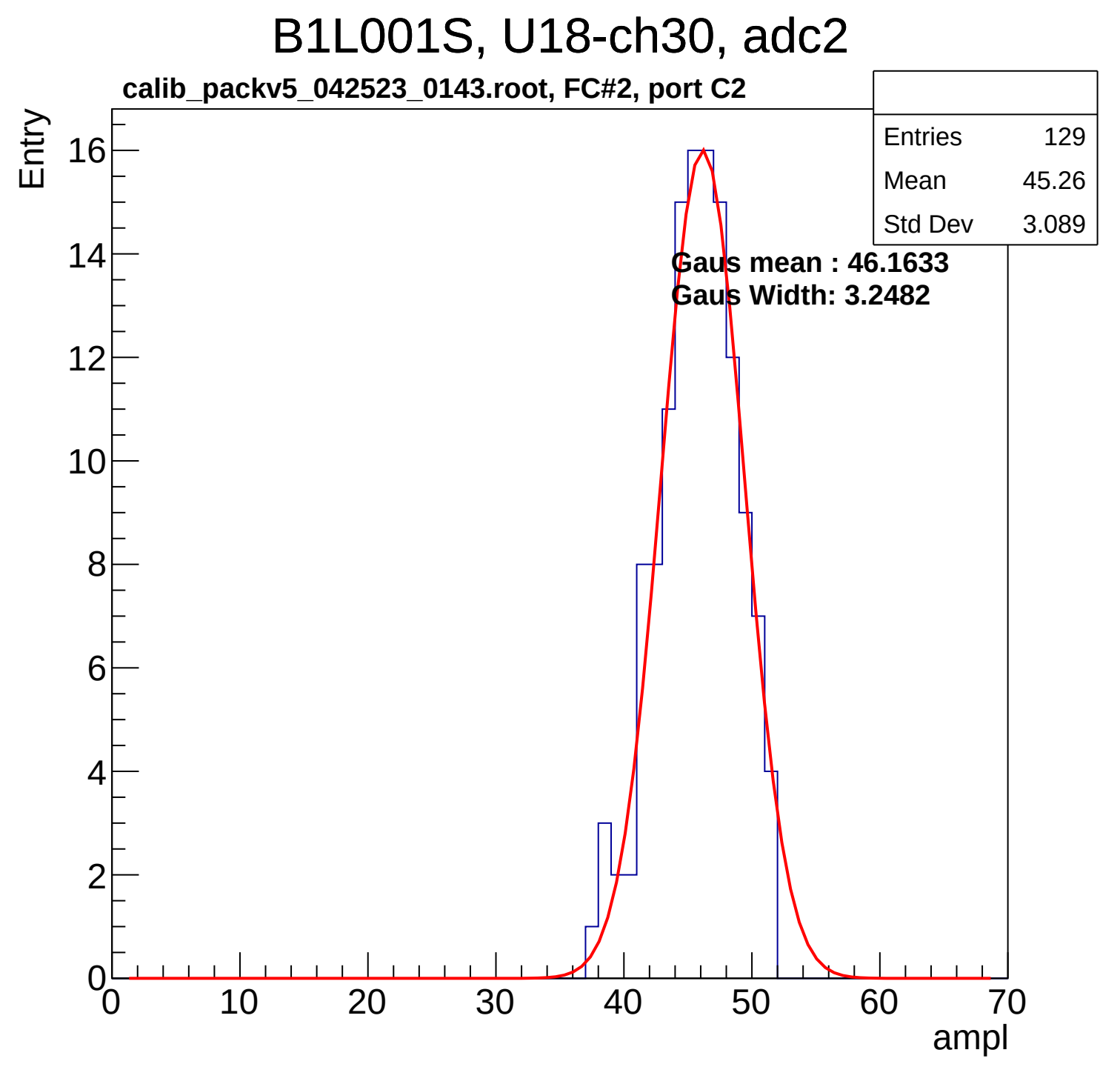

B1L001S, U18-ch29, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 77
Mean 60.08
Std Dev 2.179
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

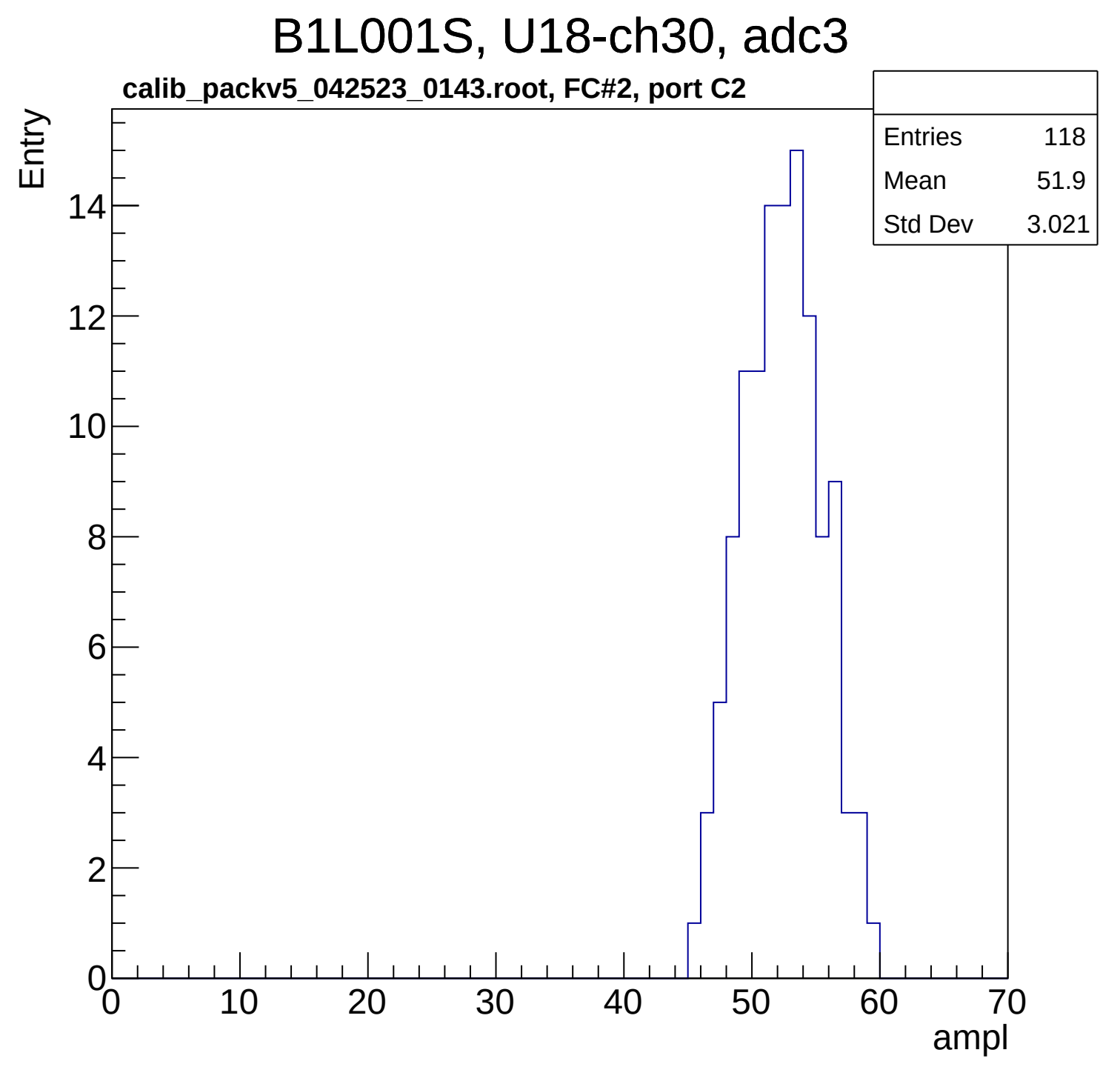

B1L001S, U18-ch29, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 8
Mean 46.88
Std Dev 27.08
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

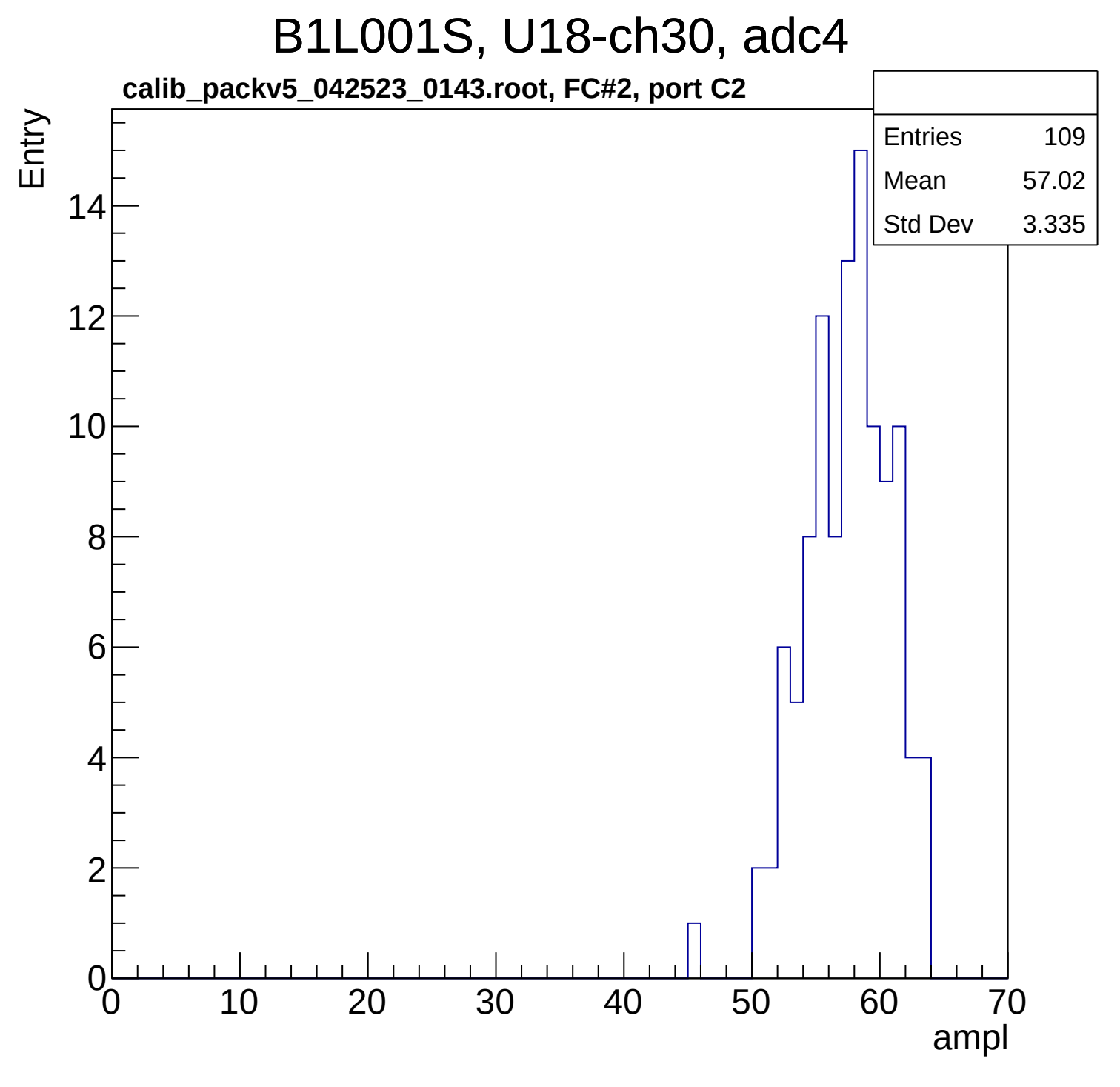

B1L001S, U18-ch29, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 43.5
Std Dev 19.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

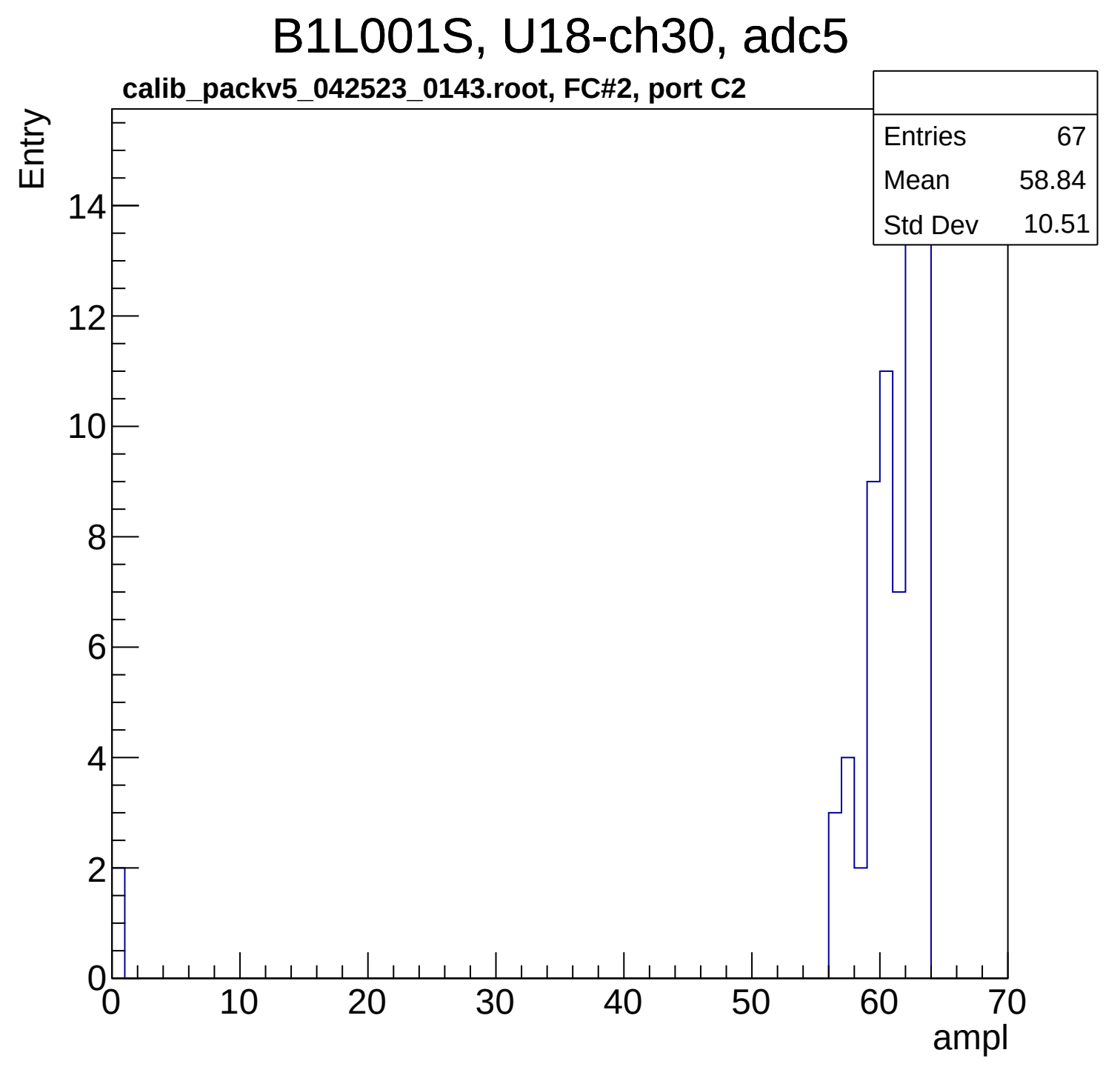

B1L001S, U18-ch30, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 135
Mean 32.46
Std Dev 3.344
Gaus mean : 33.0803
Gaus Width: 3.1567
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

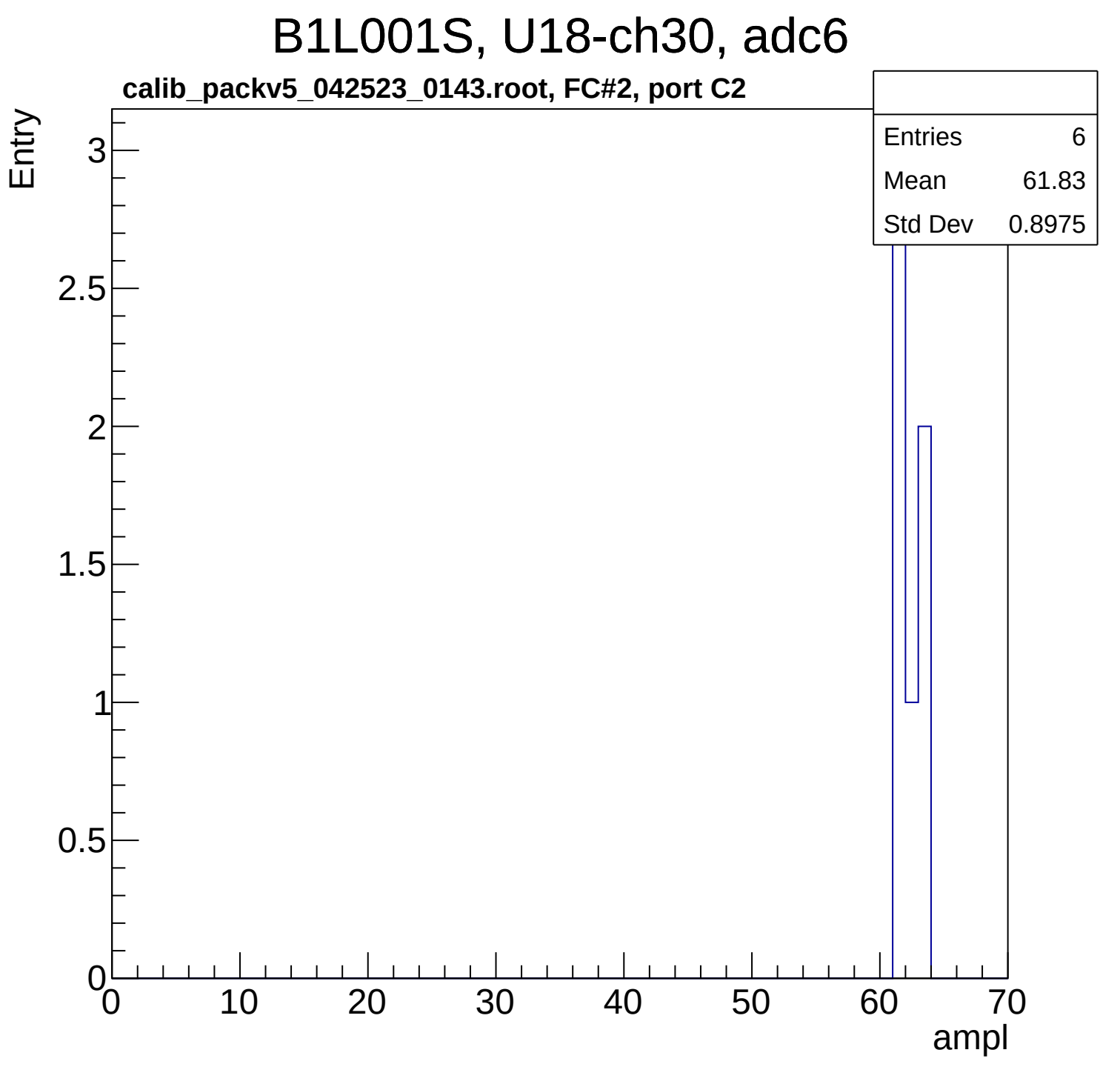

B1L001S, U18-ch30, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 123
Mean 39.11
Std Dev 2.991
Gaus mean : 39.7768
Gaus Width: 2.9227
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

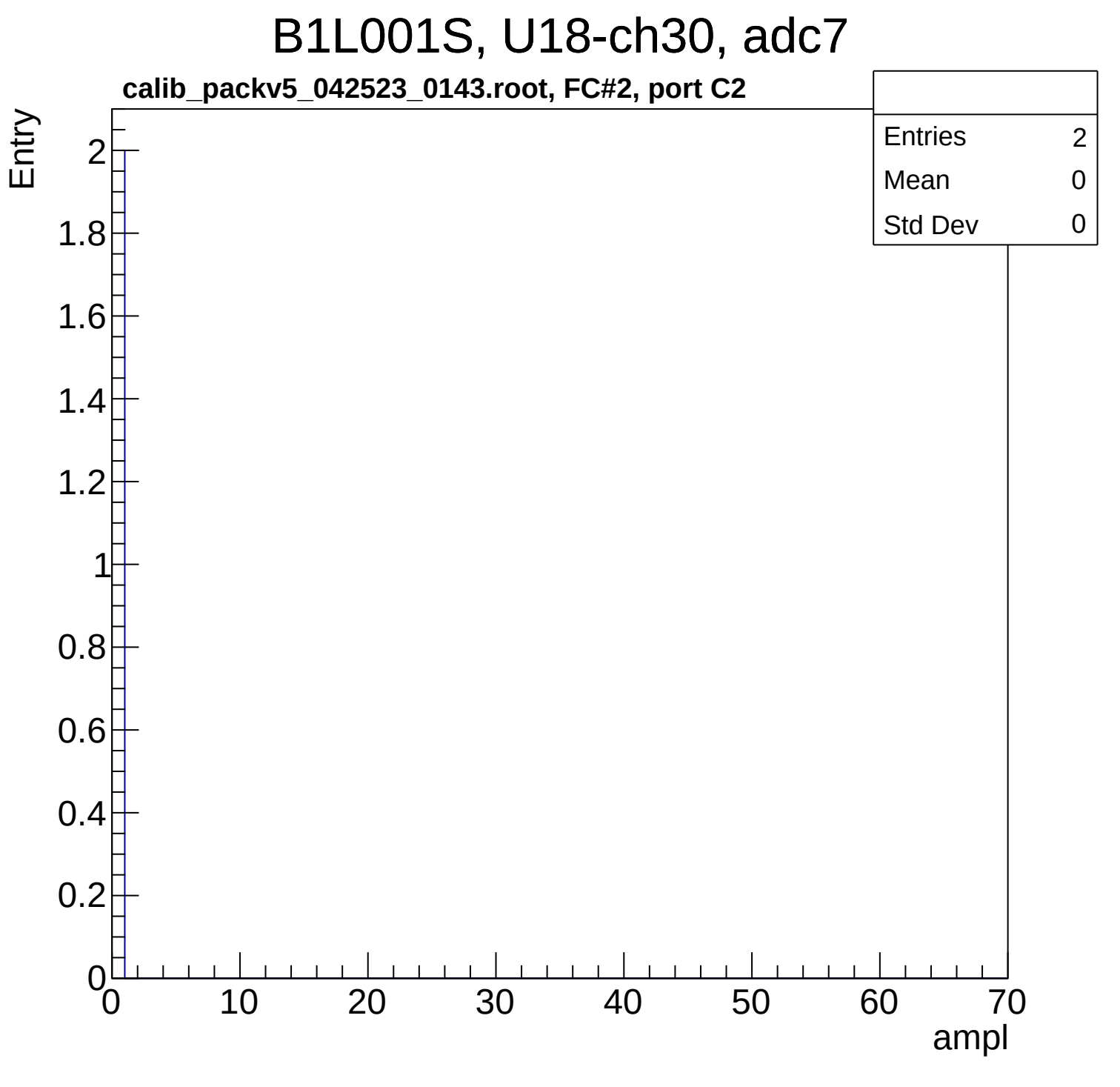

B1L001S, U18-ch30, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 129
Mean 45.26
Std Dev 3.089
Gaus mean : 46.1633
Gaus Width: 3.2482
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

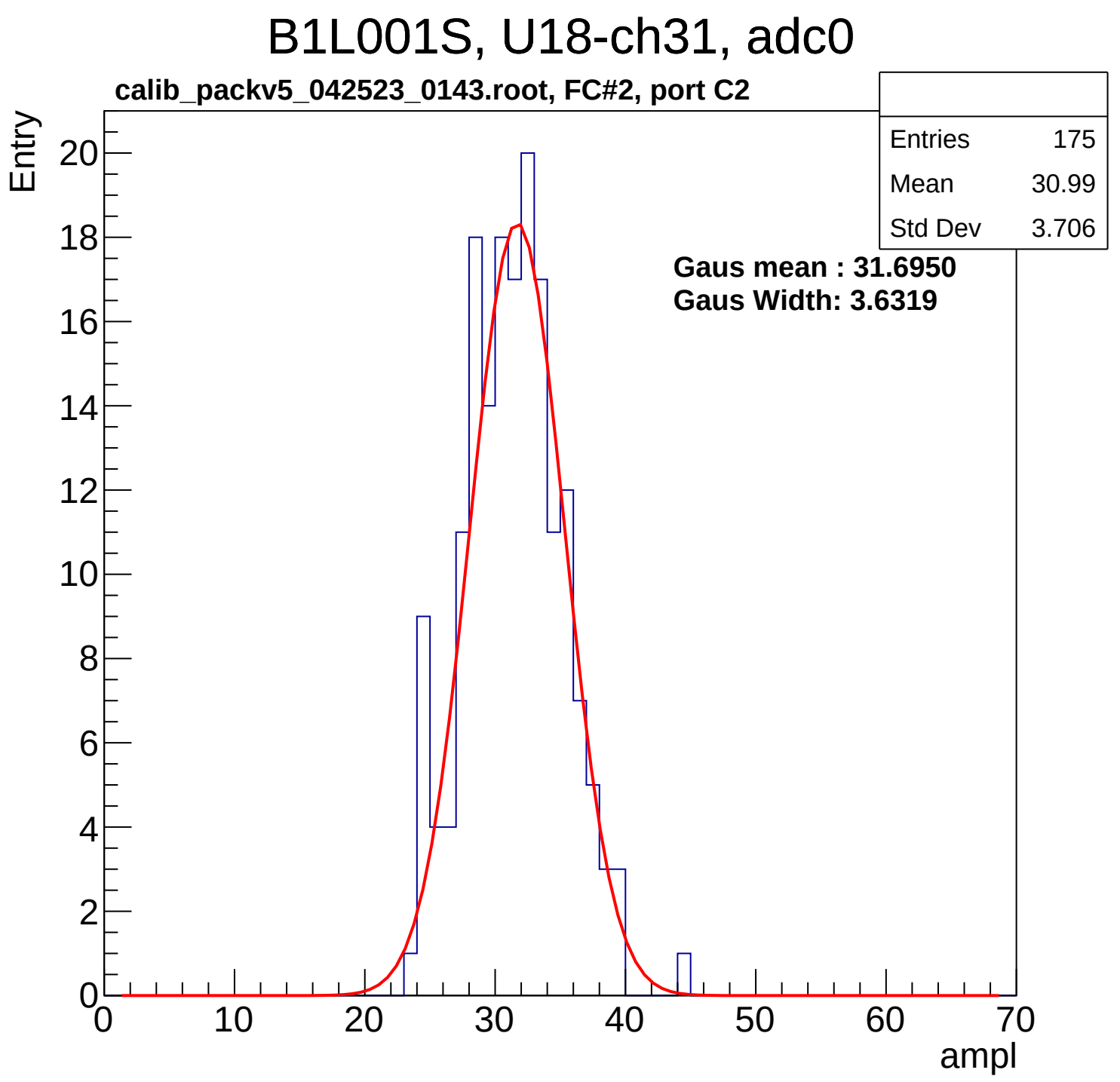

B1L001S, U18-ch30, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 118
Mean 51.9
Std Dev 3.021
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl

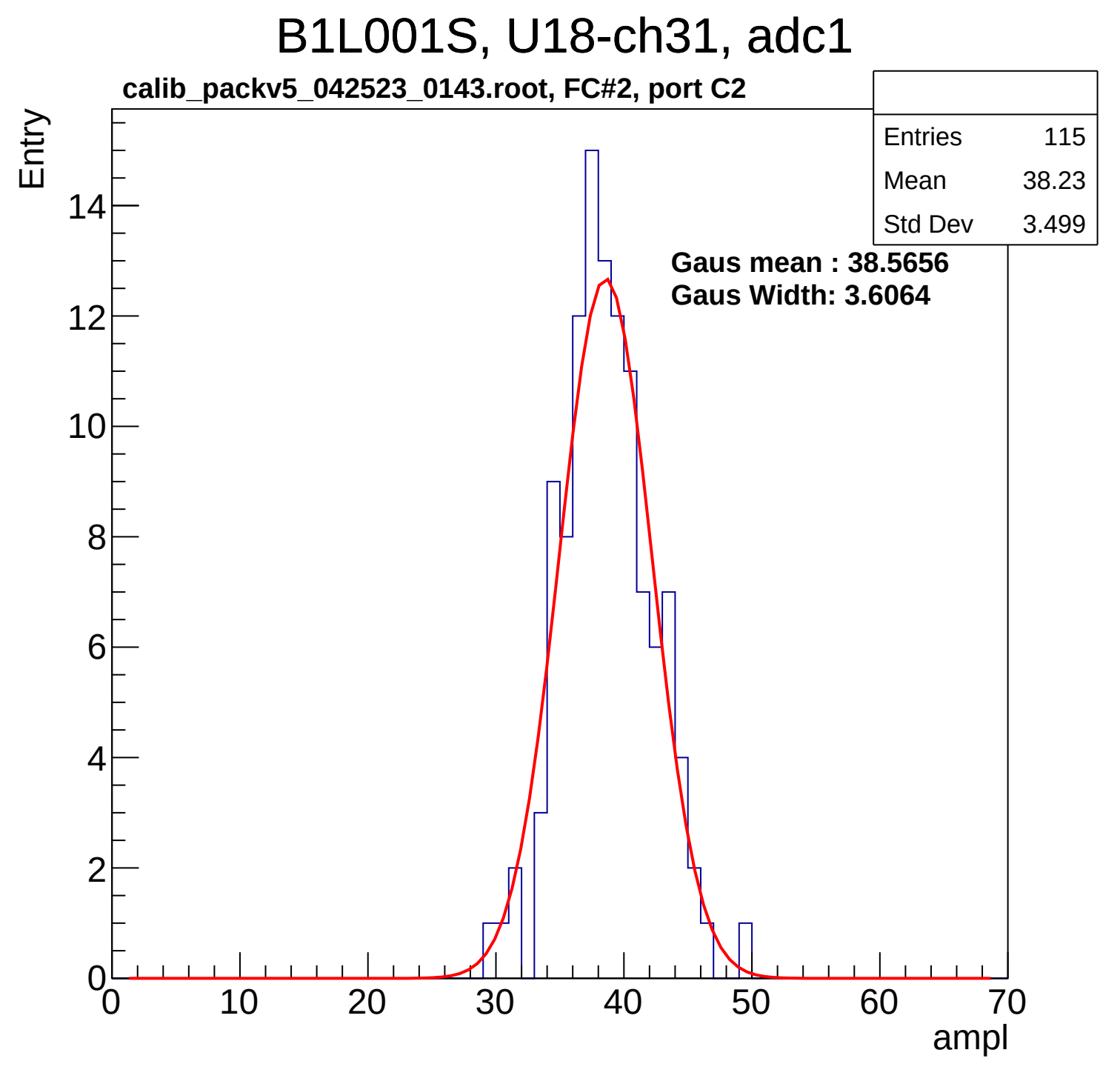

B1L001S, U18-ch30, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 109
Mean 57.02
Std Dev 3.335
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

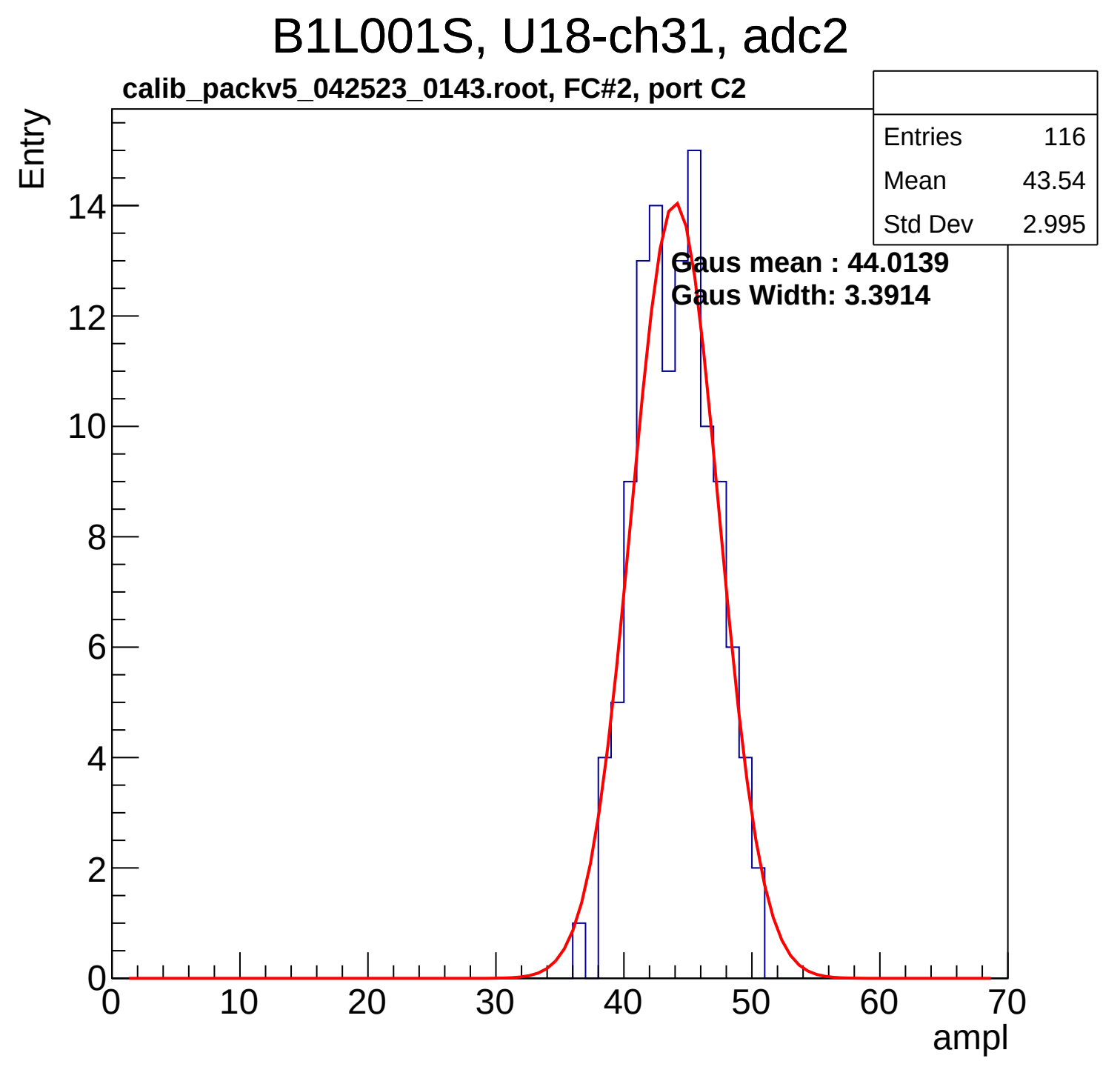

B1L001S, U18-ch30, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 67
Mean 58.84
Std Dev 10.51
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl

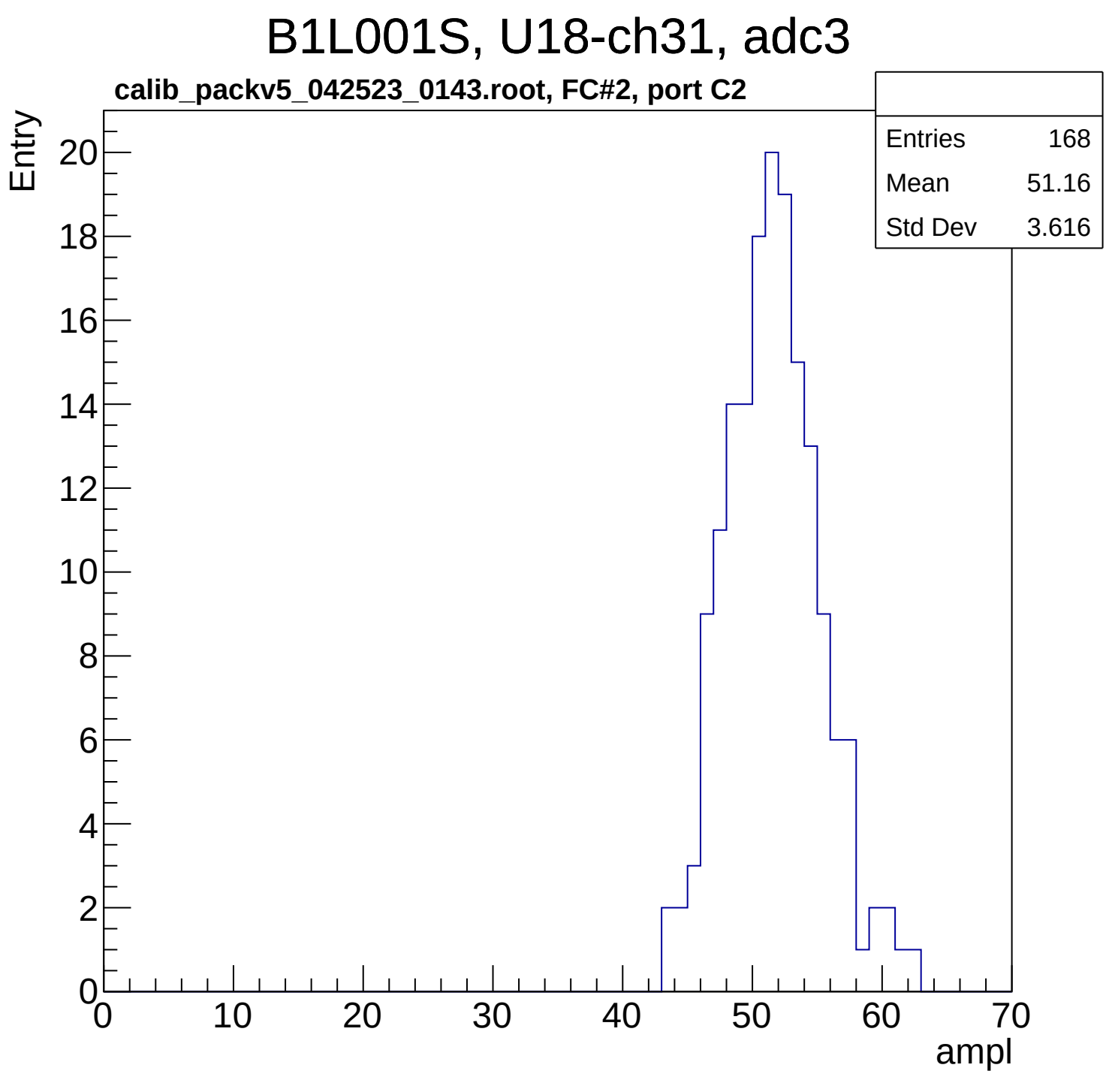

B1L001S, U18-ch30, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 6
Mean 61.83
Std Dev 0.8975
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

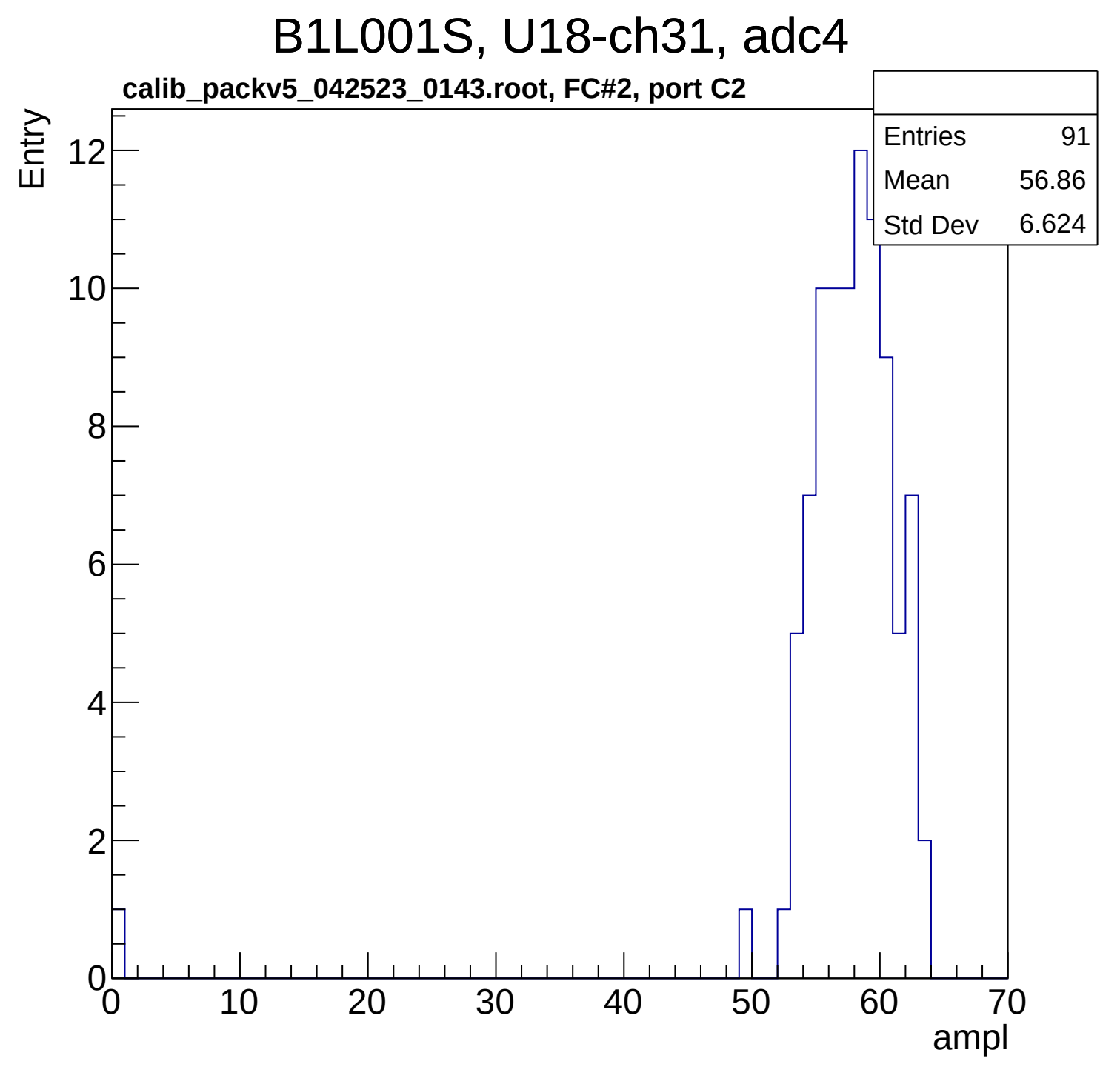

B1L001S, U18-ch30, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 0
Std Dev 0
Entry
2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

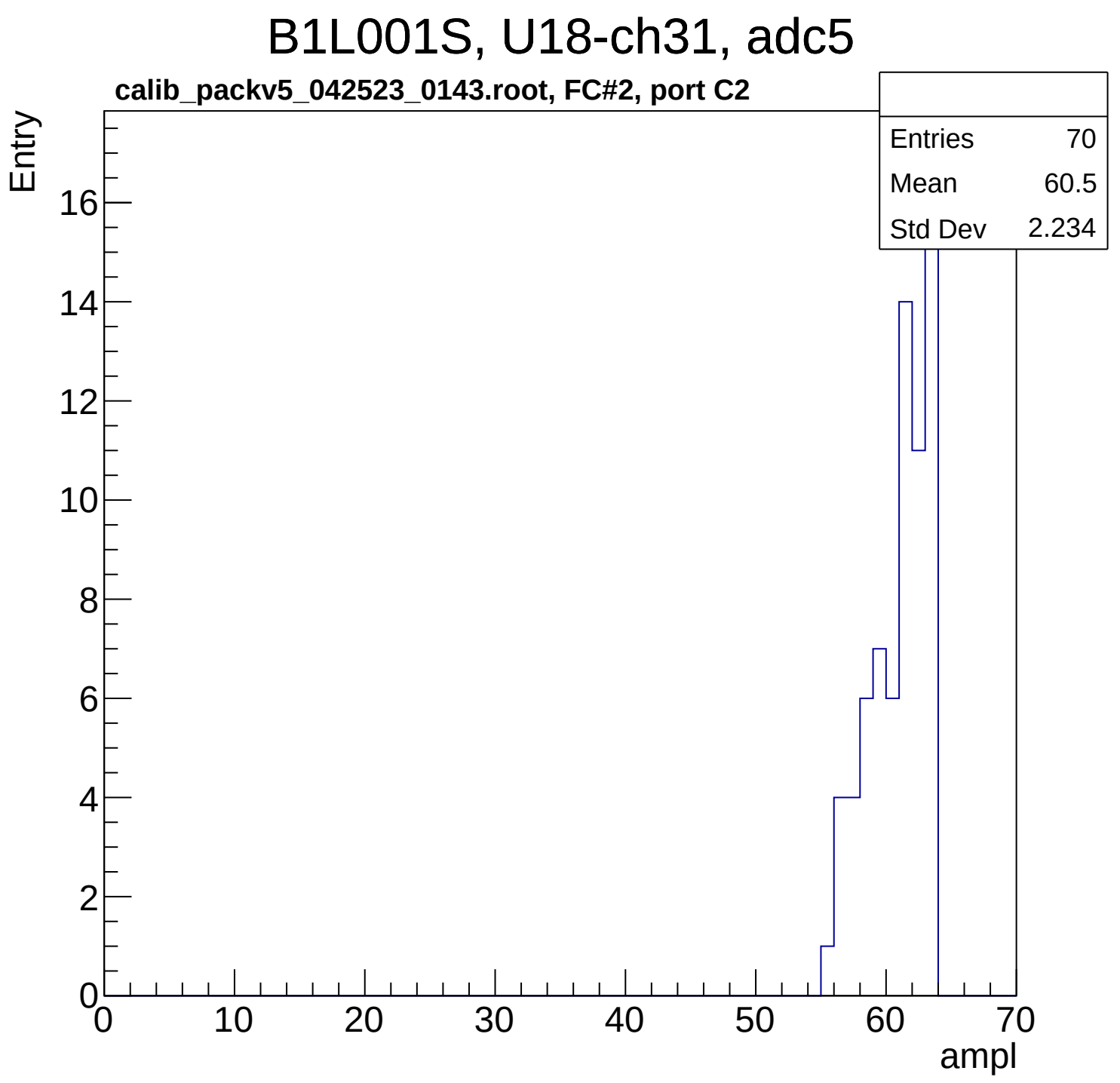

B1L001S, U18-ch31, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 175
Mean 30.99
Std Dev 3.706
Gaus mean : 31.6950
Gaus Width: 3.6319
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

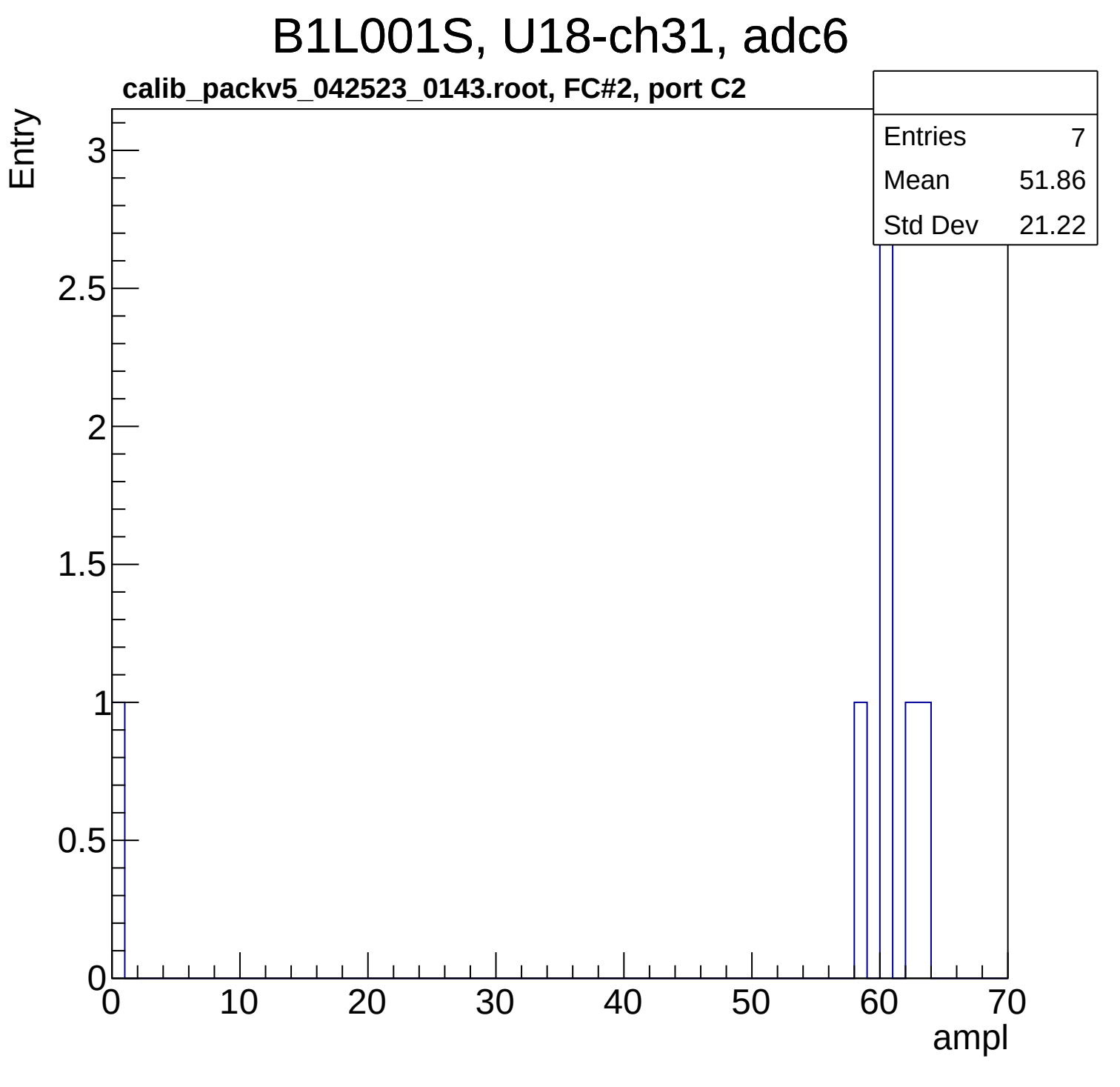

B1L001S, U18-ch31, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 115
Mean 38.23
Std Dev 3.499
Gaus mean : 38.5656
Gaus Width: 3.6064
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

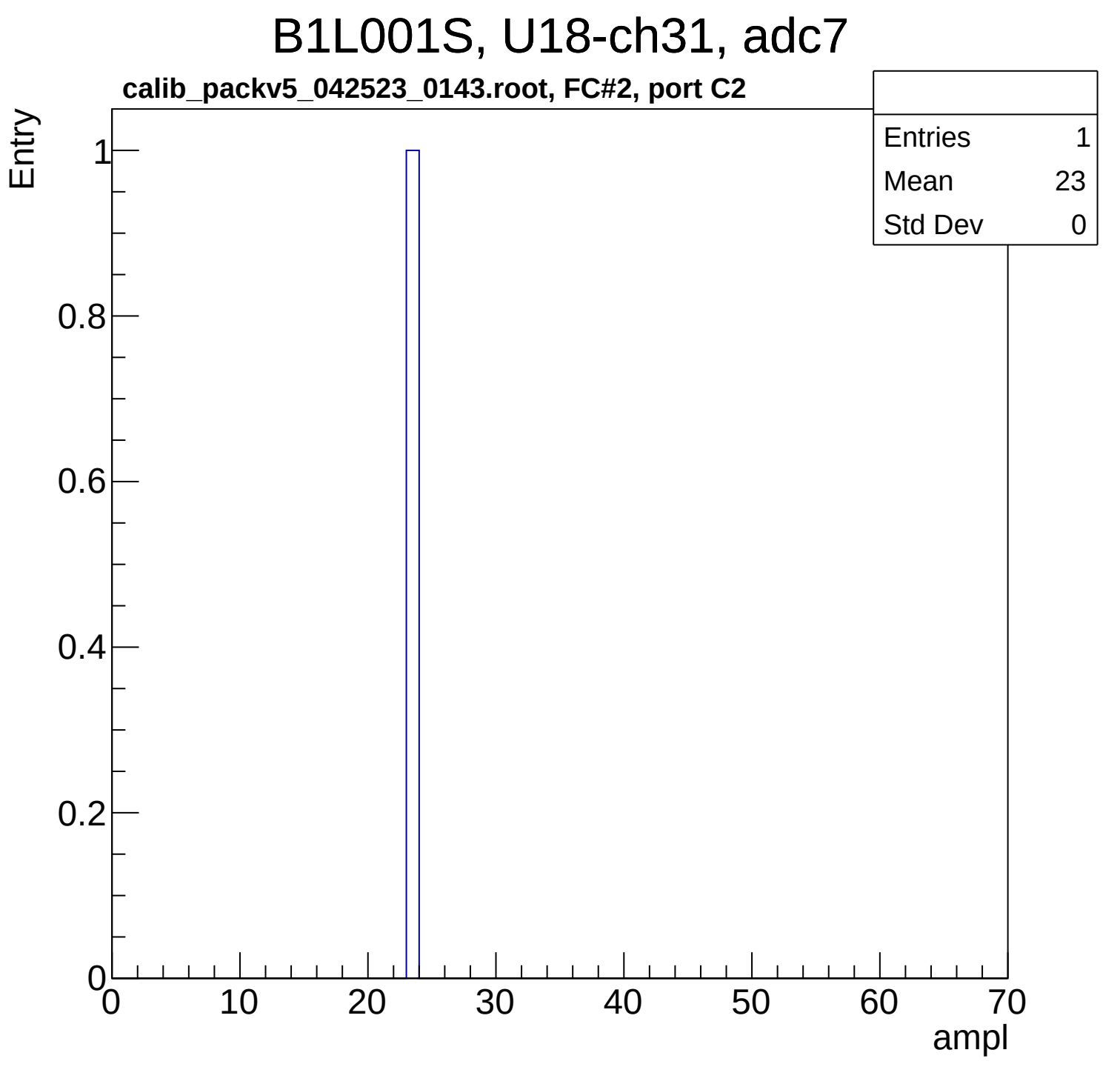

B1L001S, U18-ch31, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 116
Mean 43.54
Std Dev 2.995
Gaus mean : 44.0139
Gaus Width: 3.3914
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

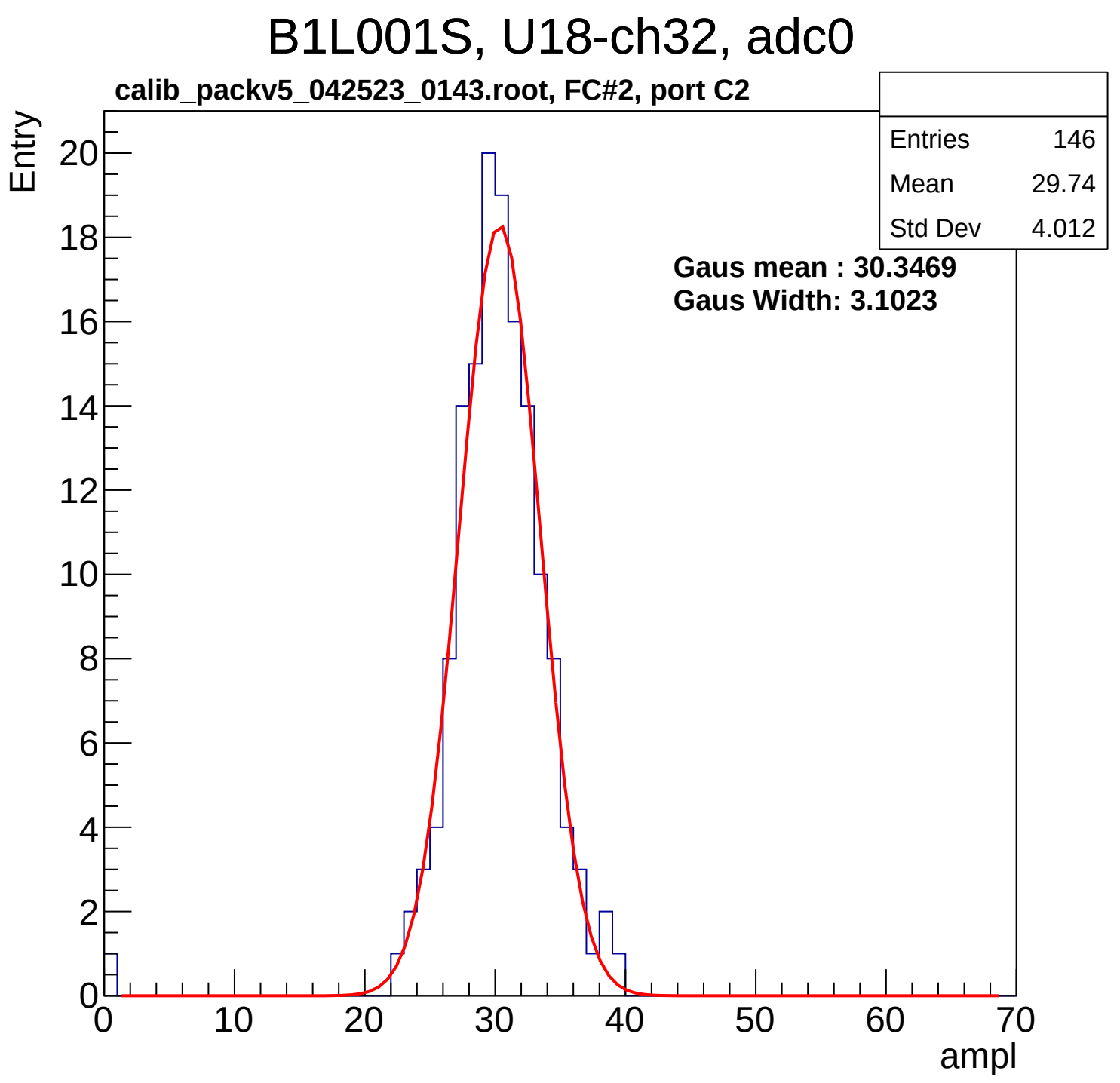

B1L001S, U18-ch31, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 168
Mean 51.16
Std Dev 3.616
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

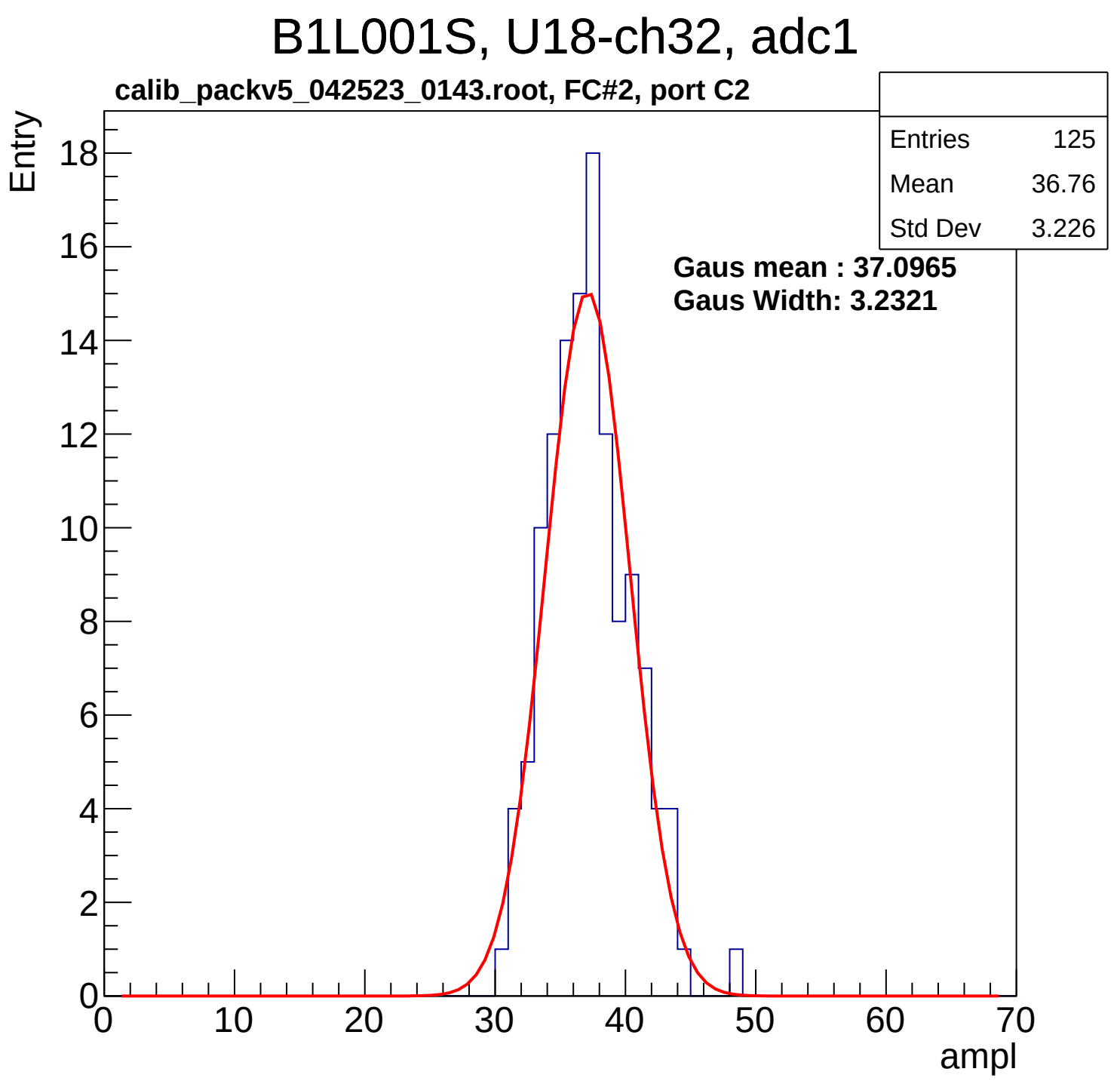

B1L001S, U18-ch31, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 91
Mean 56.86
Std Dev 6.624
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70

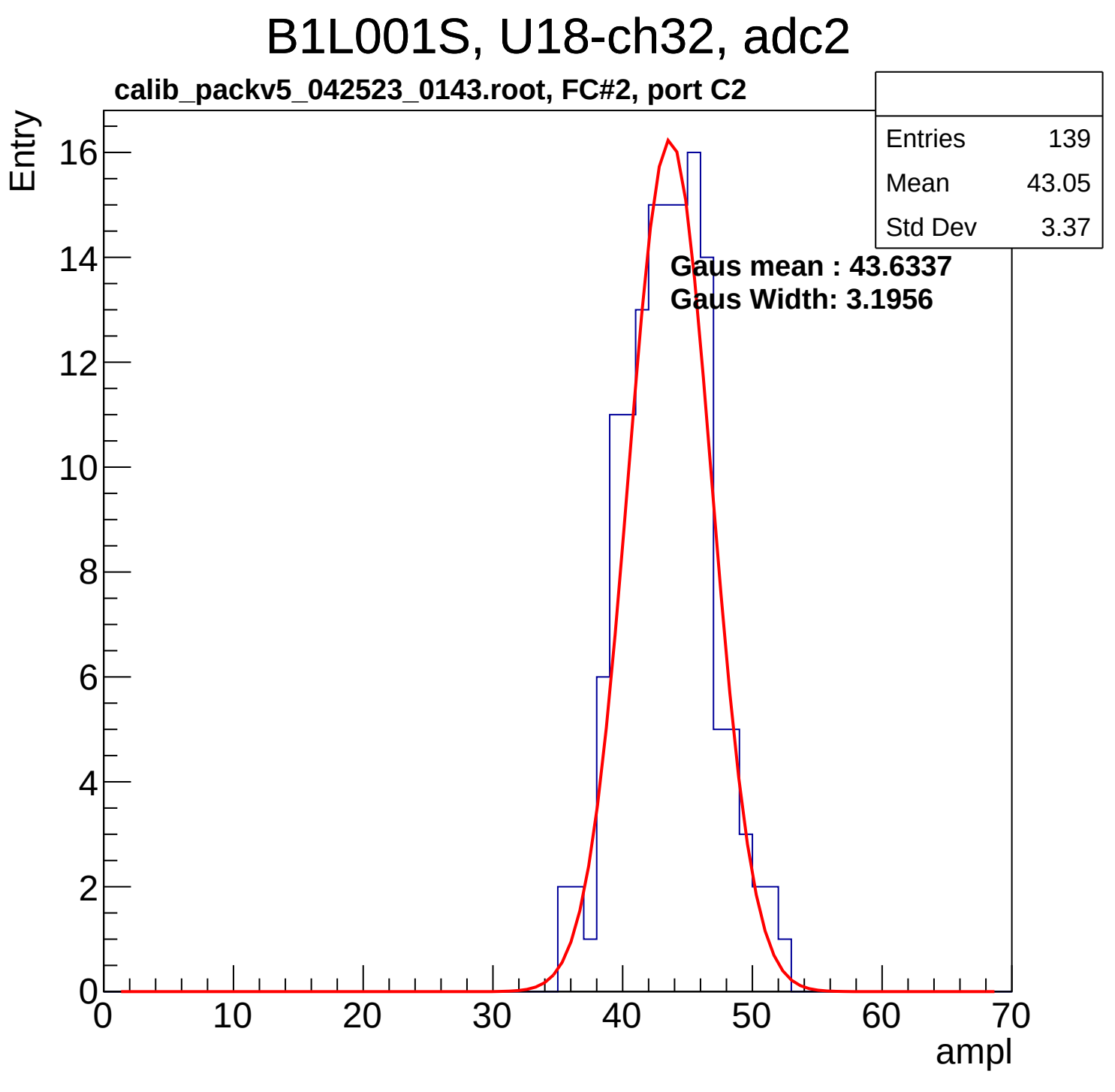

B1L001S, U18-ch31, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 70
Mean 60.5
Std Dev 2.234
Entry
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl

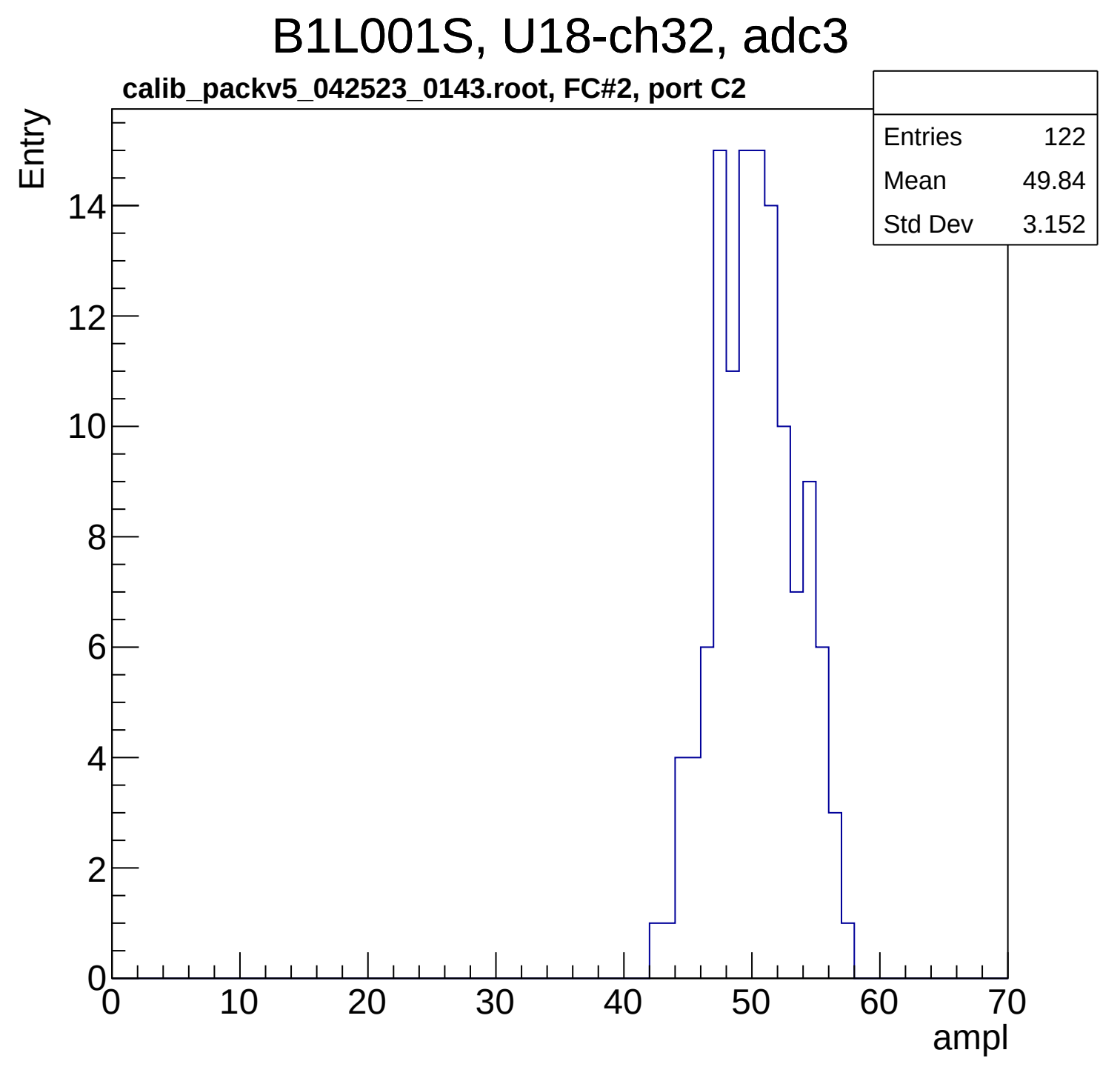

B1L001S, U18-ch31, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 7
Mean 51.86
Std Dev 21.22
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

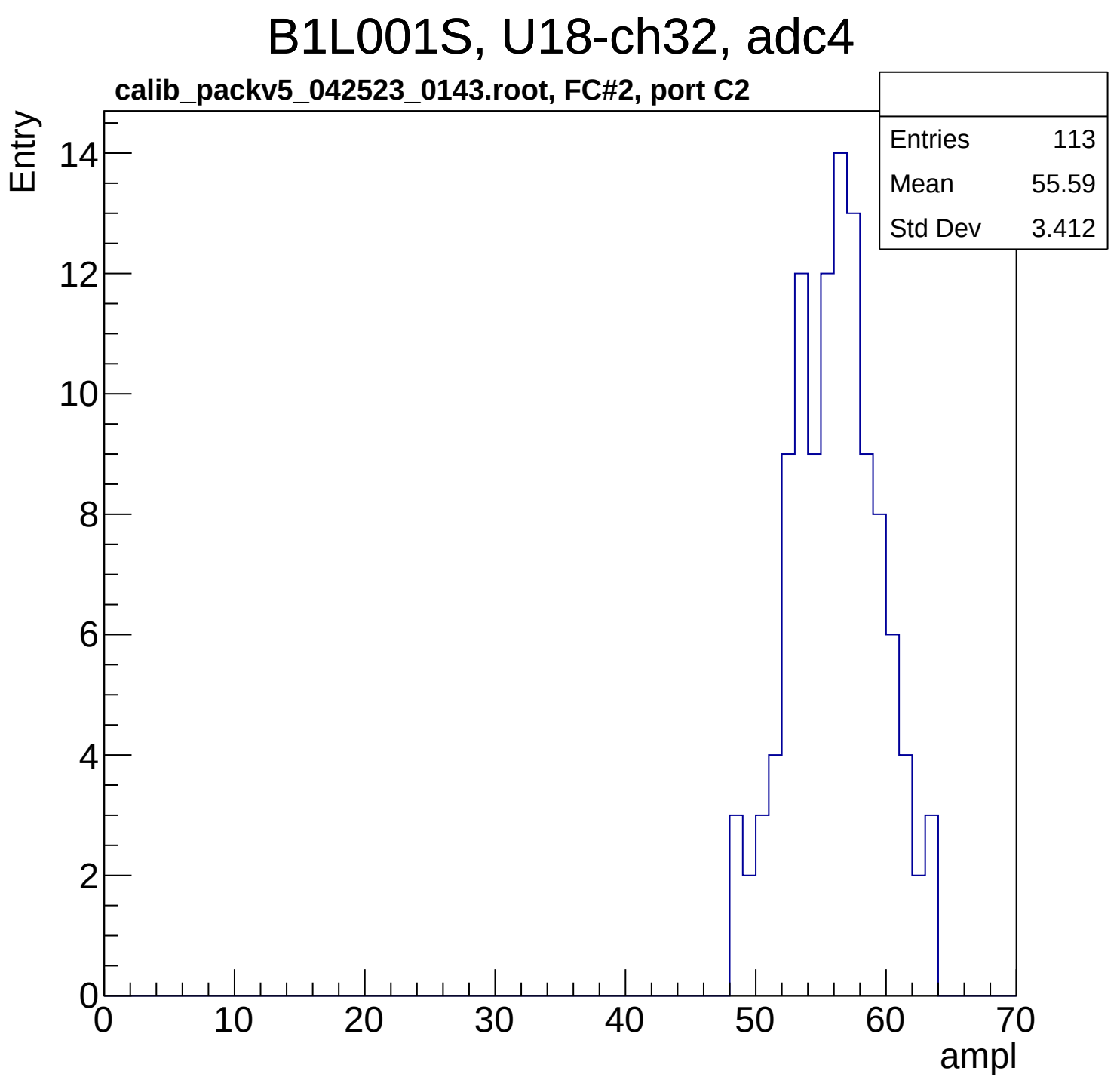

B1L001S, U18-ch31, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 23
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

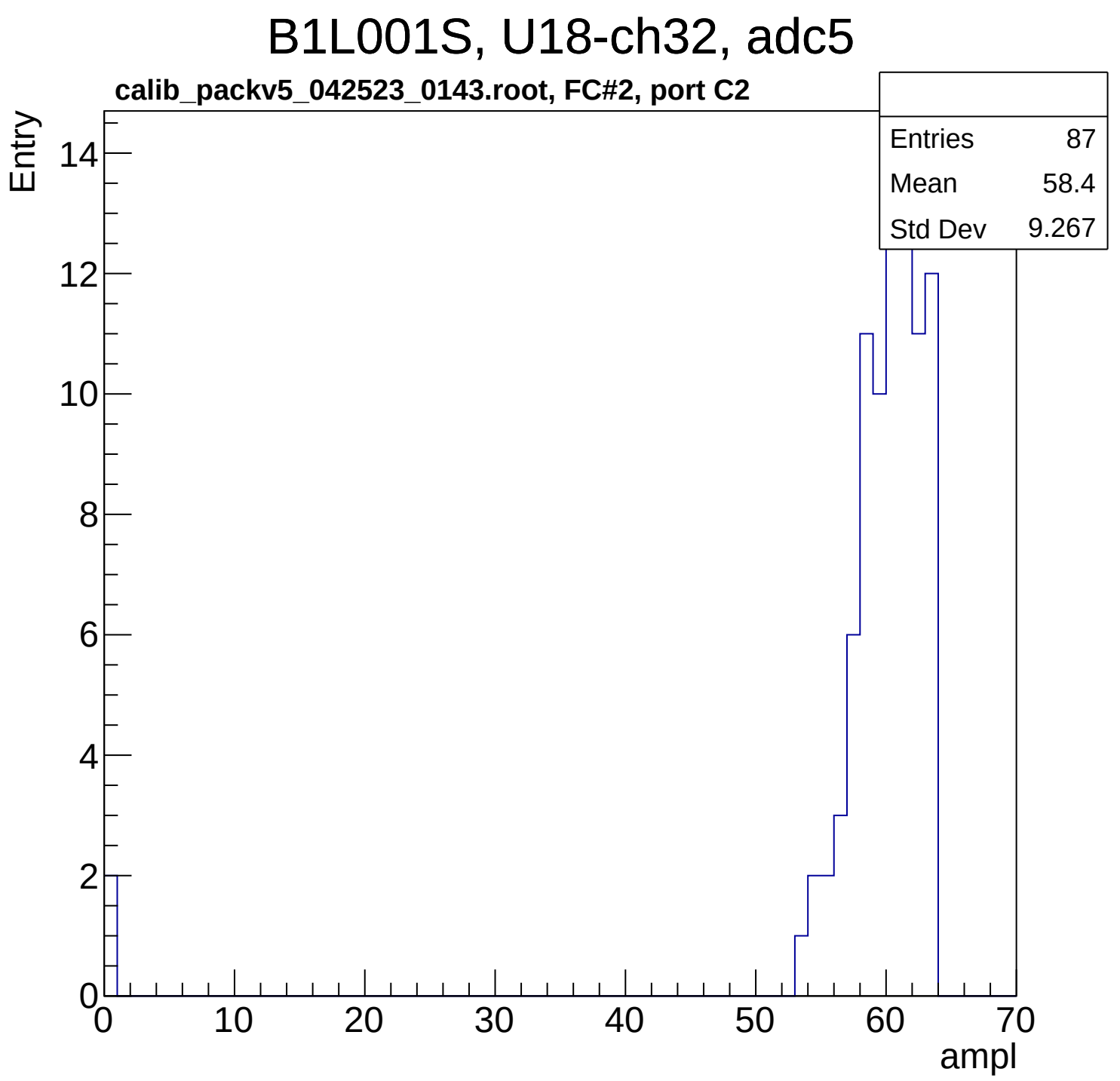

B1L001S, U18-ch32, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 146
Mean 29.74
Std Dev 4.012
Gaus mean : 30.3469
Gaus Width: 3.1023
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

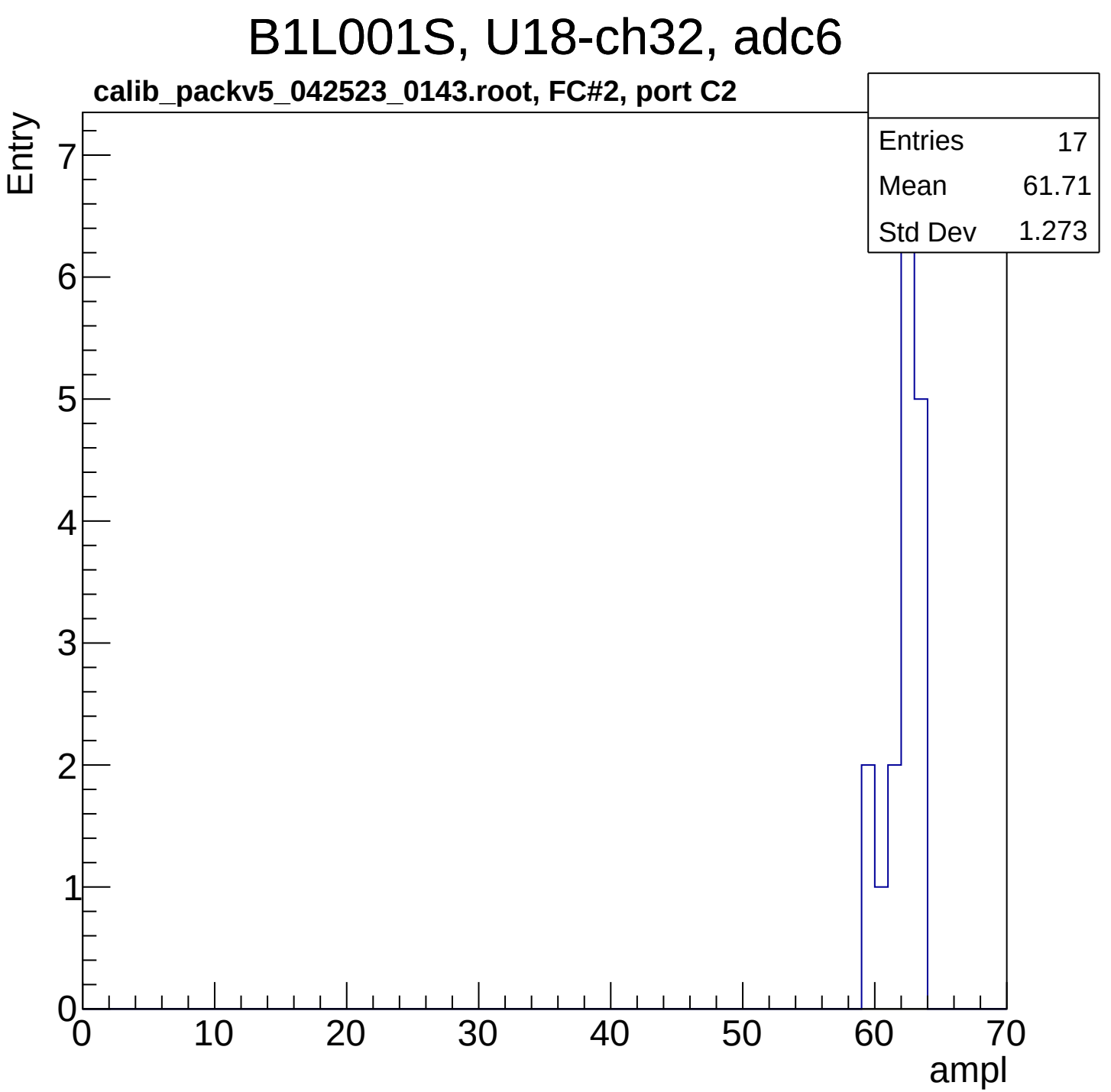

B1L001S, U18-ch32, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 125
Mean 36.76
Std Dev 3.226
Gaus mean : 37.0965
Gaus Width: 3.2321
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

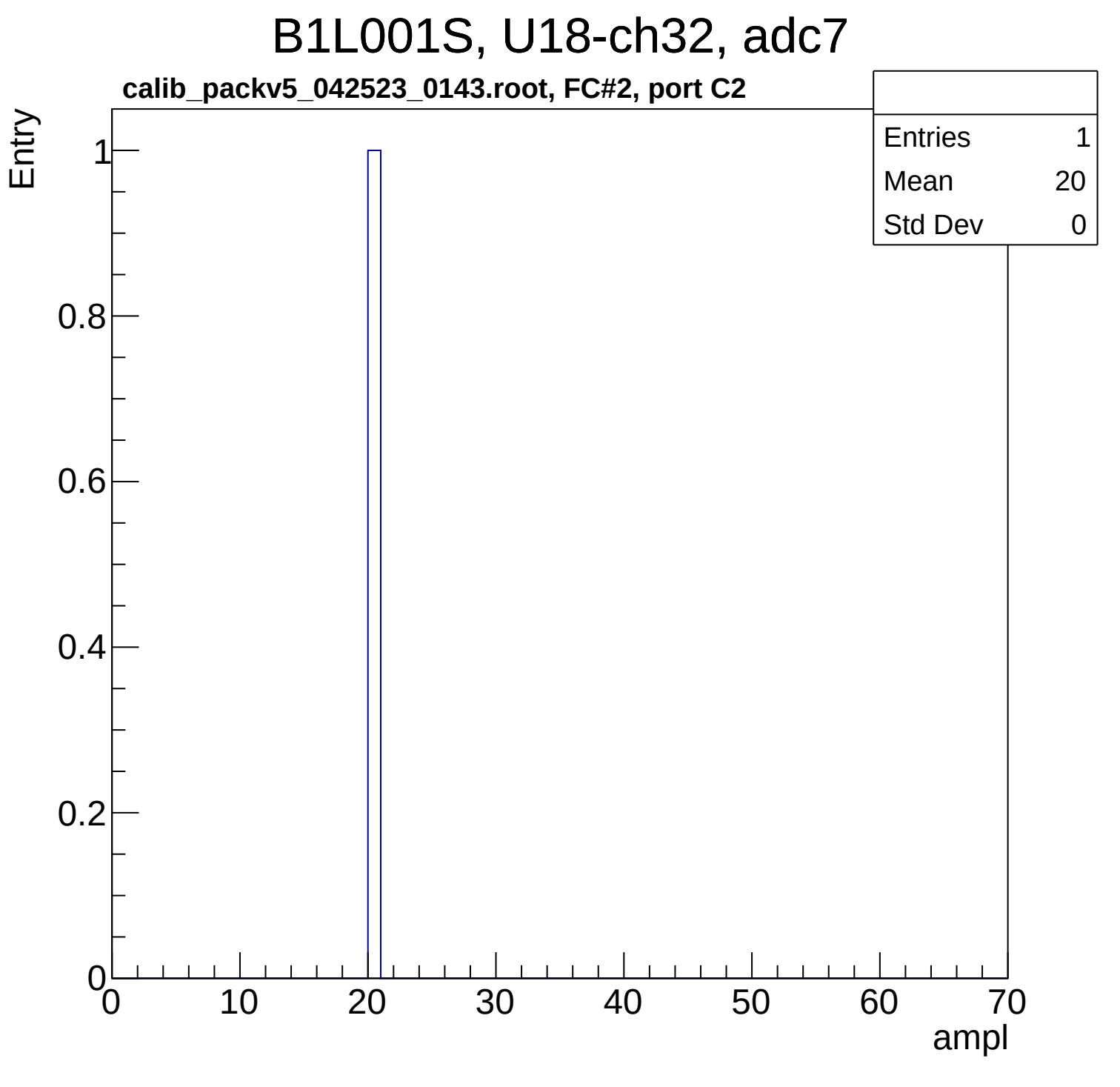

B1L001S, U18-ch32, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 139
Mean 43.05
Std Dev 3.37
Gaus mean : 43.6337
Gaus Width: 3.1956
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

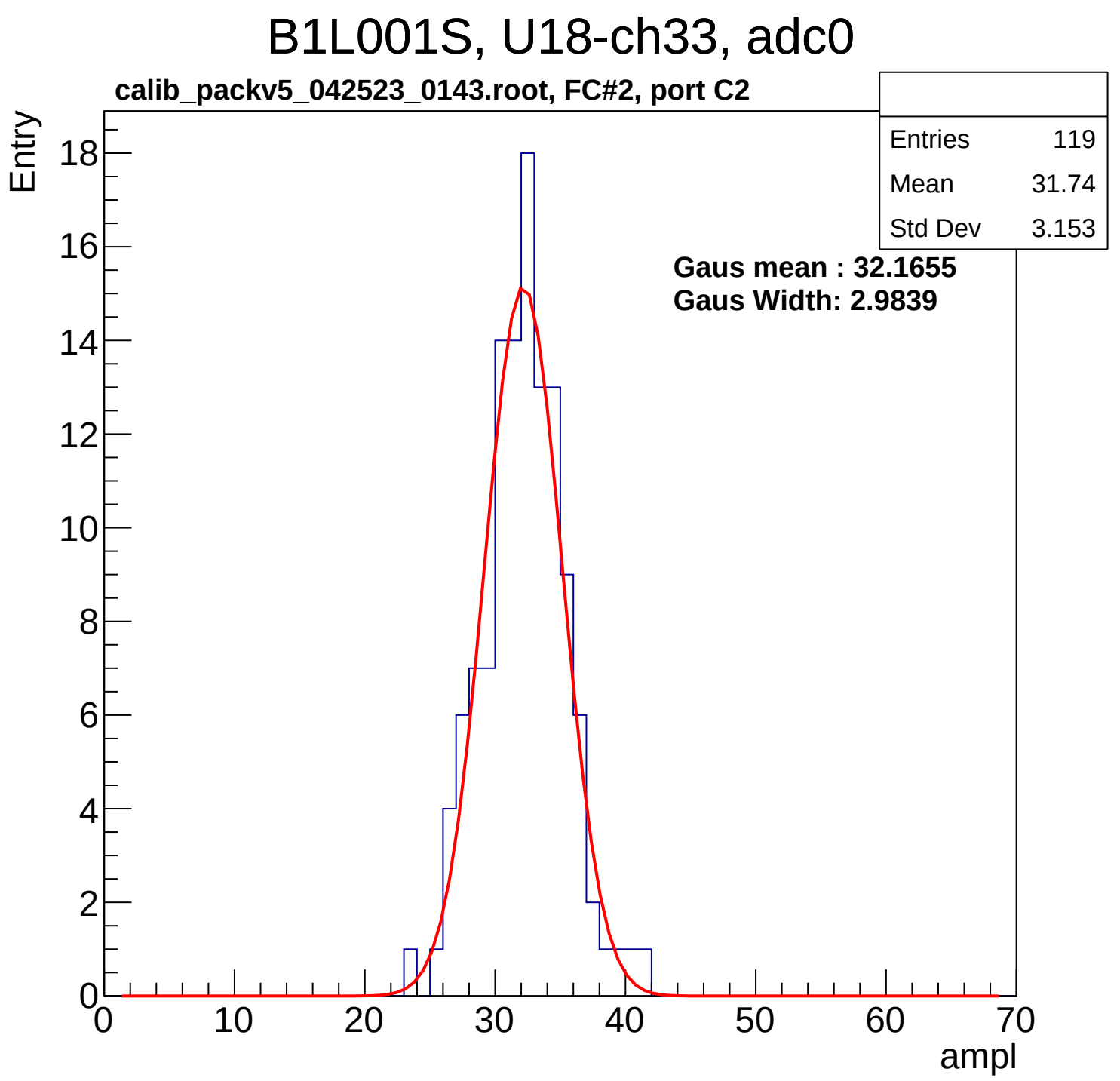

B1L001S, U18-ch32, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 122
Mean 49.84
Std Dev 3.152
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl

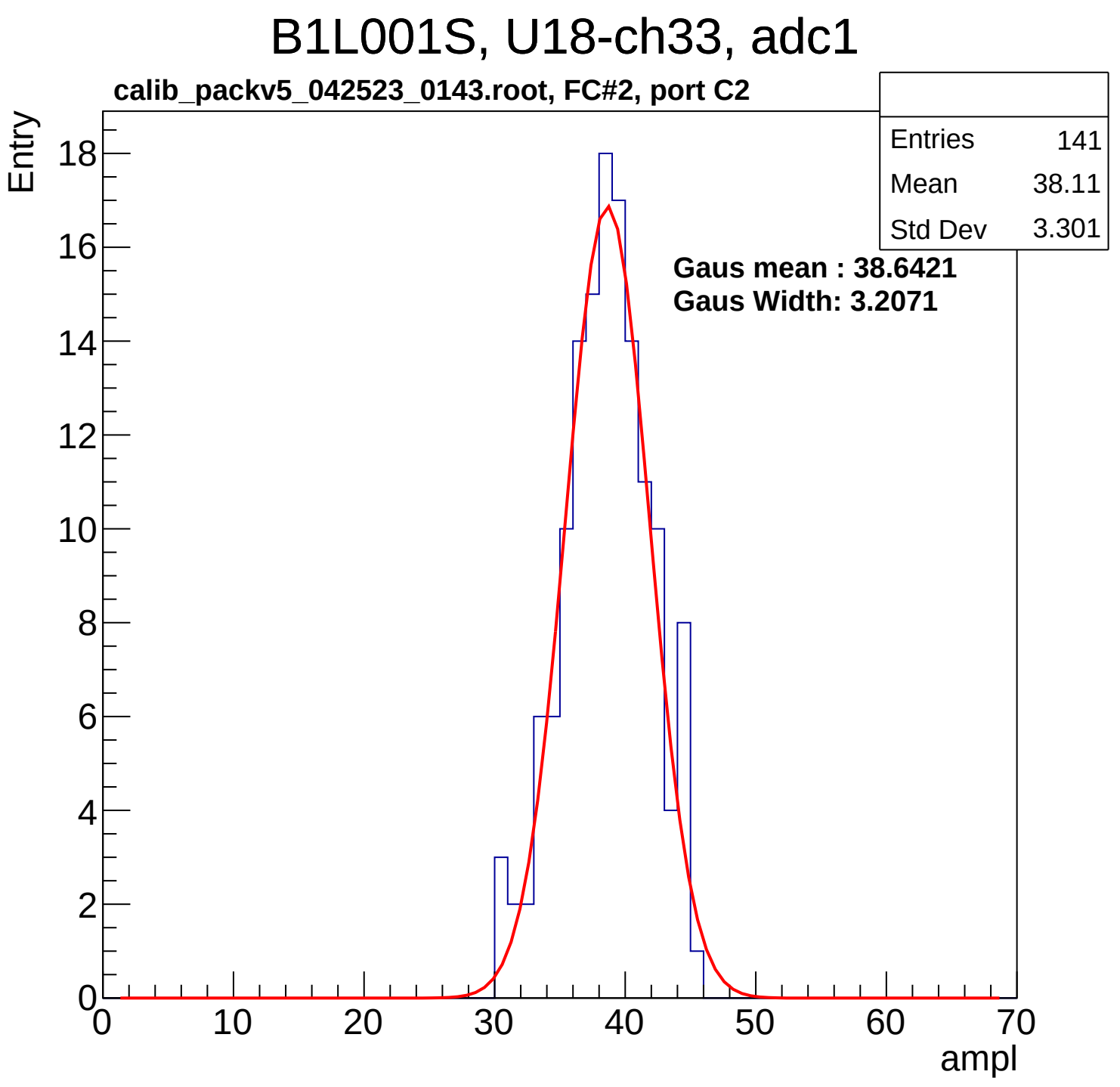

B1L001S, U18-ch32, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 113
Mean 55.59
Std Dev 3.412
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

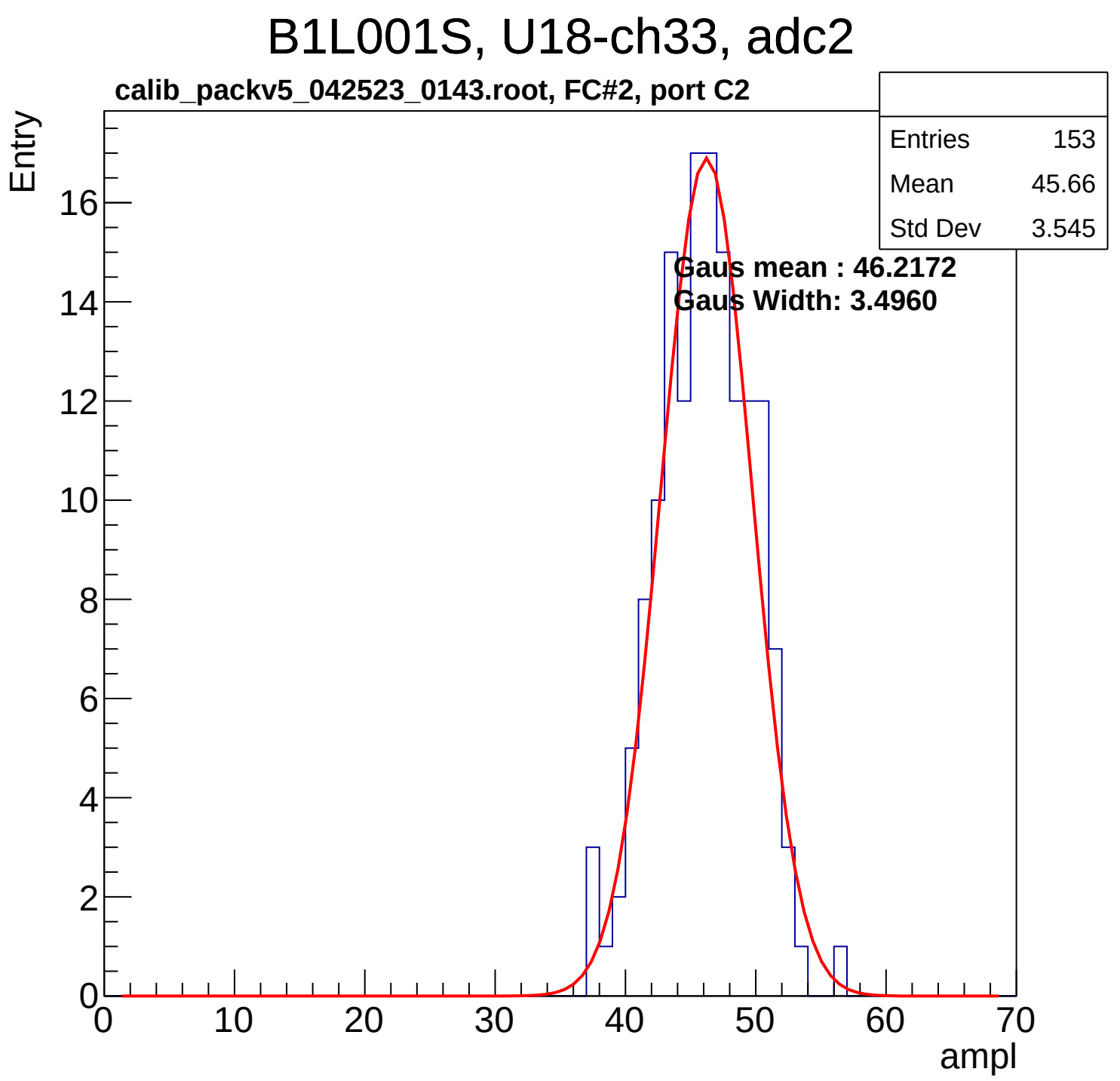

B1L001S, U18-ch32, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 87
Mean 58.4
Std Dev 9.267
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

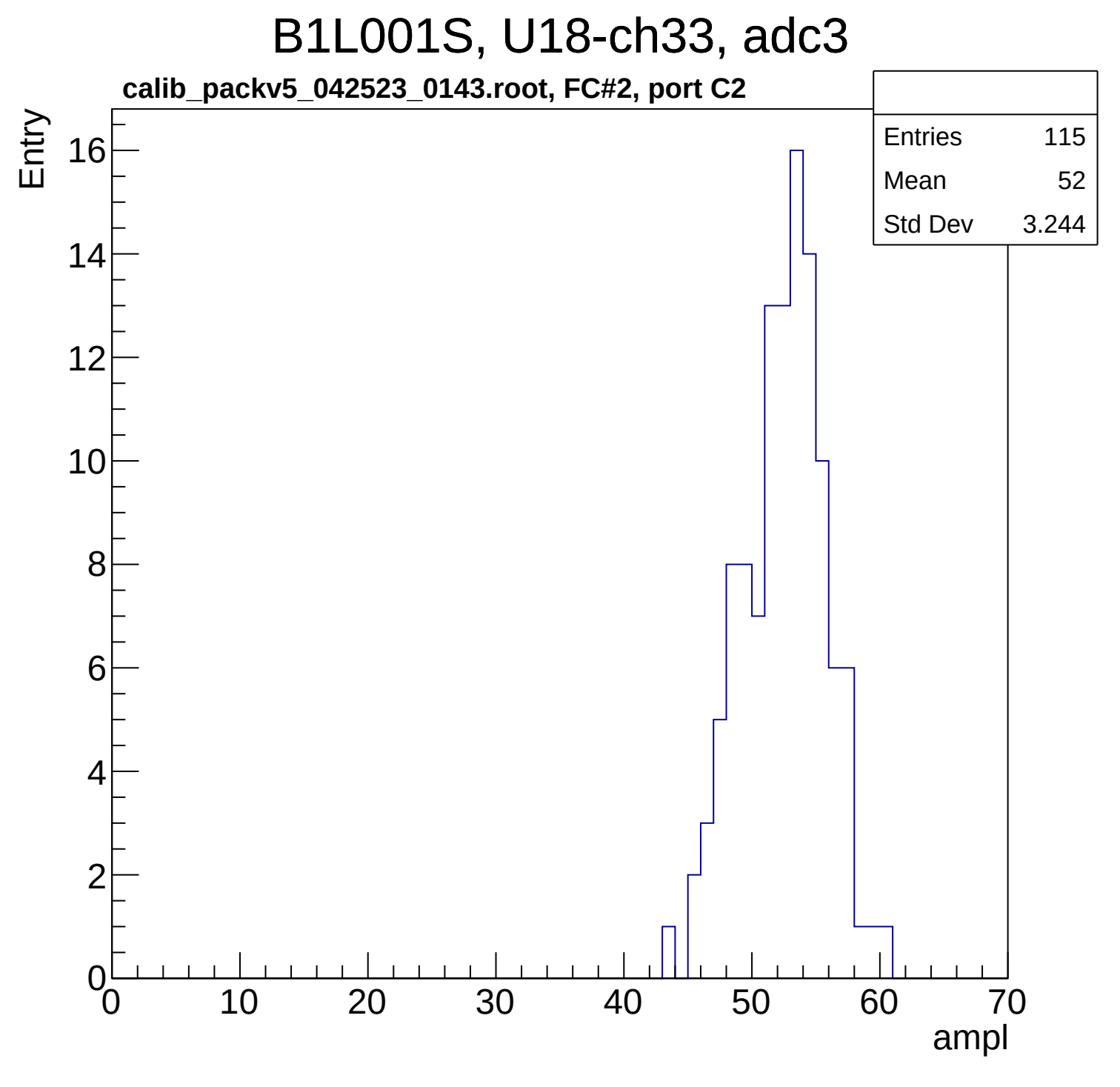

B1L001S, U18-ch32, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 17
Mean 61.71
Std Dev 1.273
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

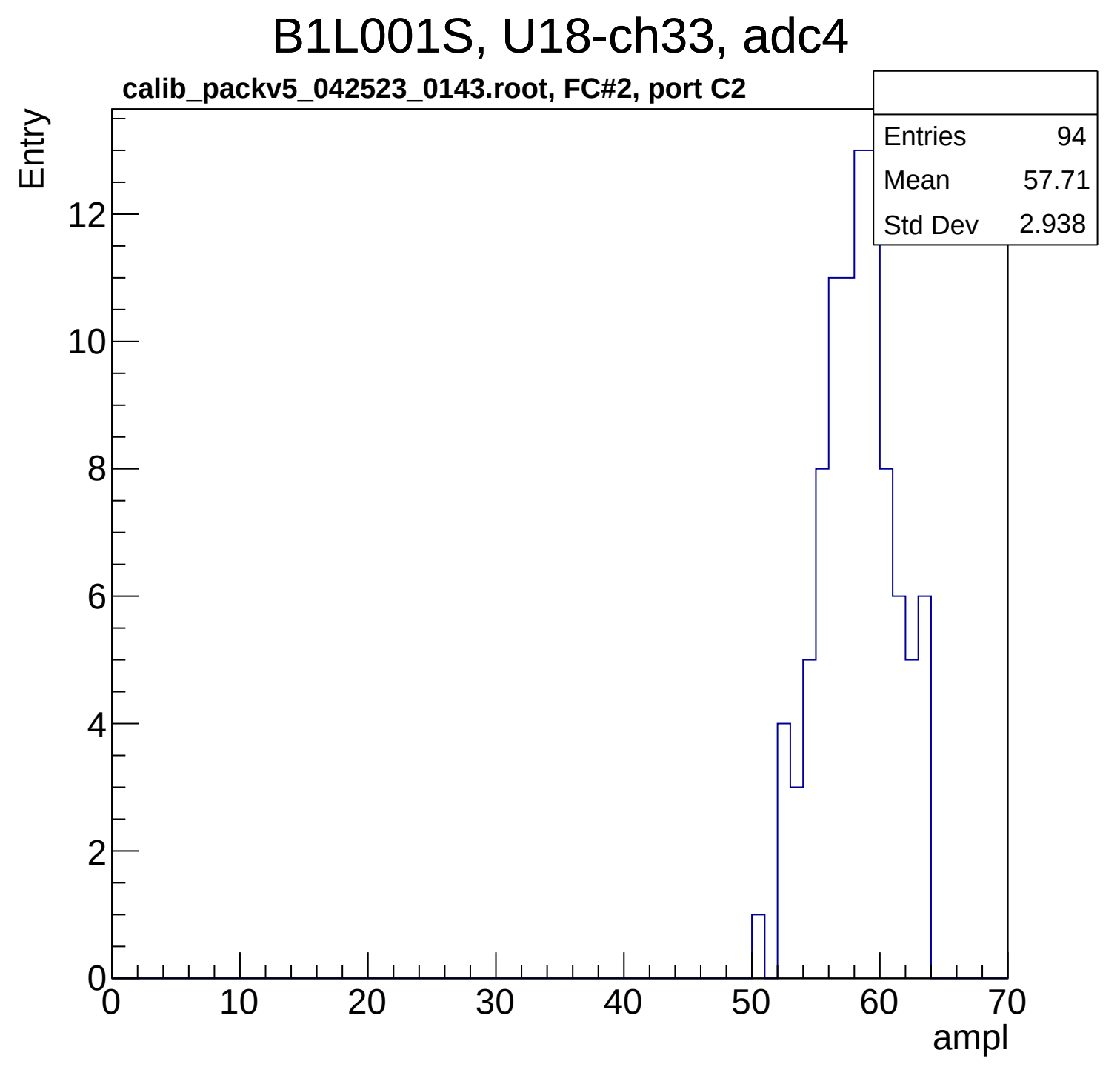

B1L001S, U18-ch32, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 20
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70

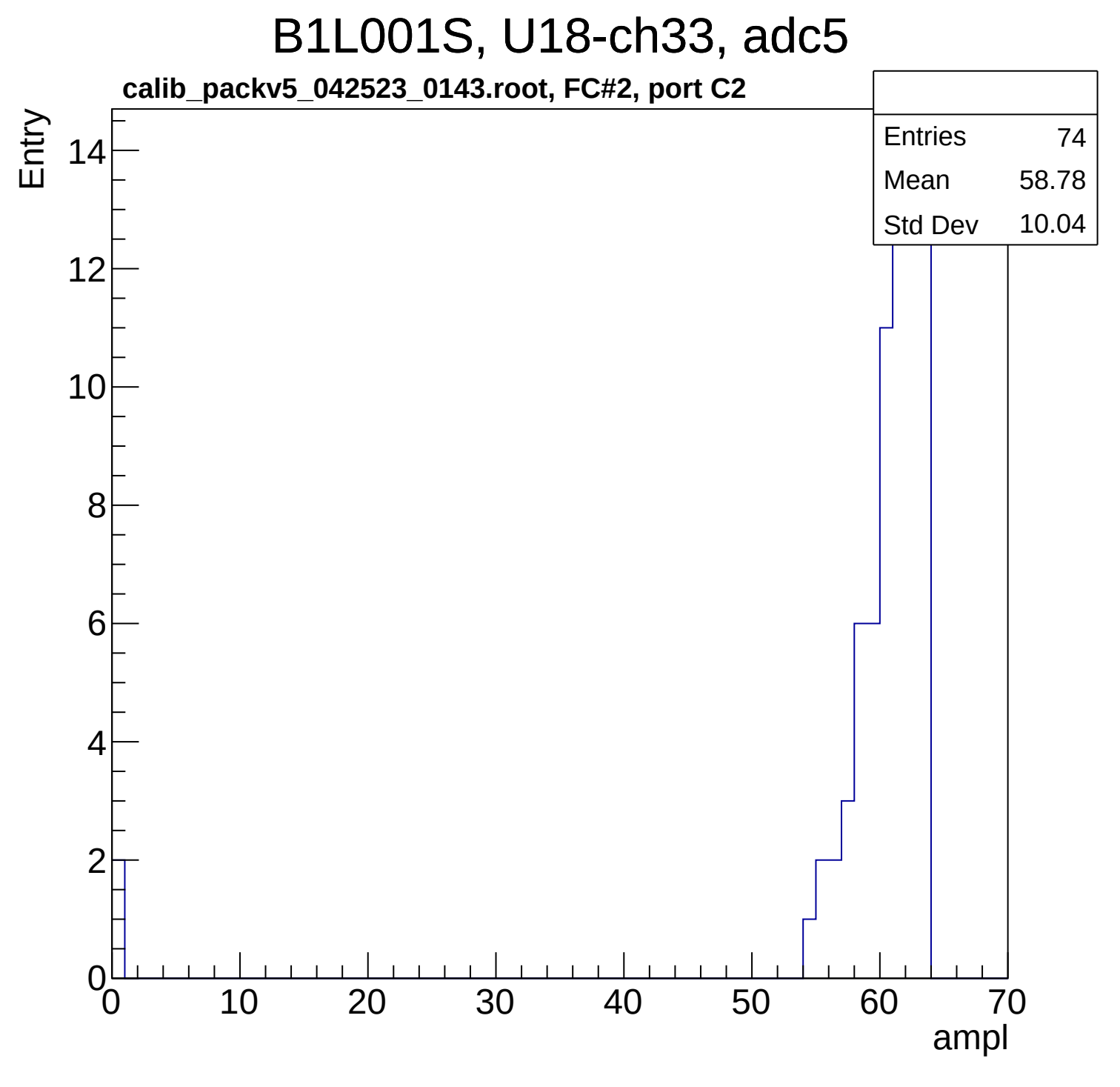

B1L001S, U18-ch33, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 119
Mean 31.74
Std Dev 3.153
Gaus mean : 32.1655
Gaus Width: 2.9839
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

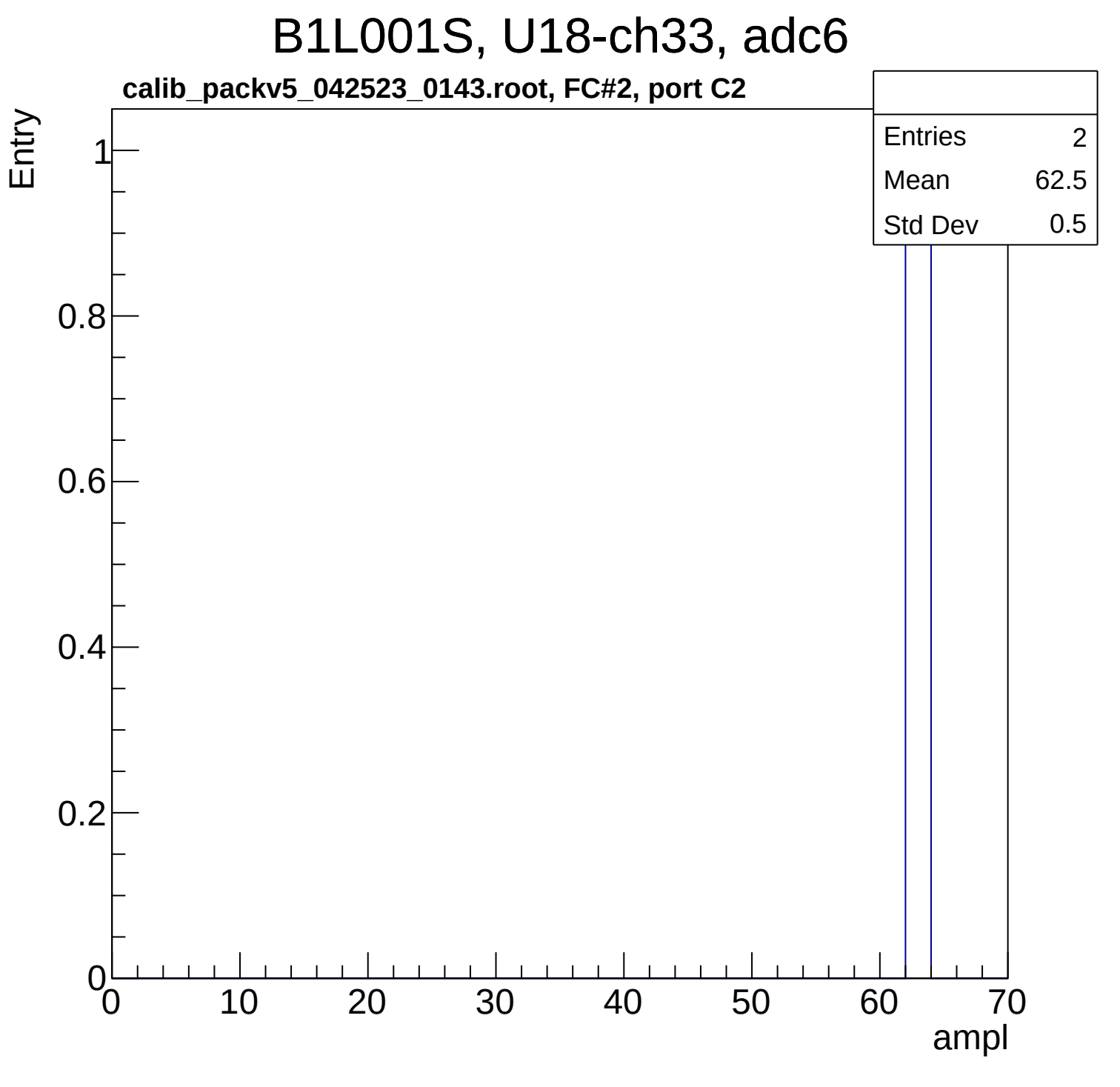

B1L001S, U18-ch33, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 141
Mean 38.11
Std Dev 3.301
Gaus mean : 38.6421
Gaus Width: 3.2071
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

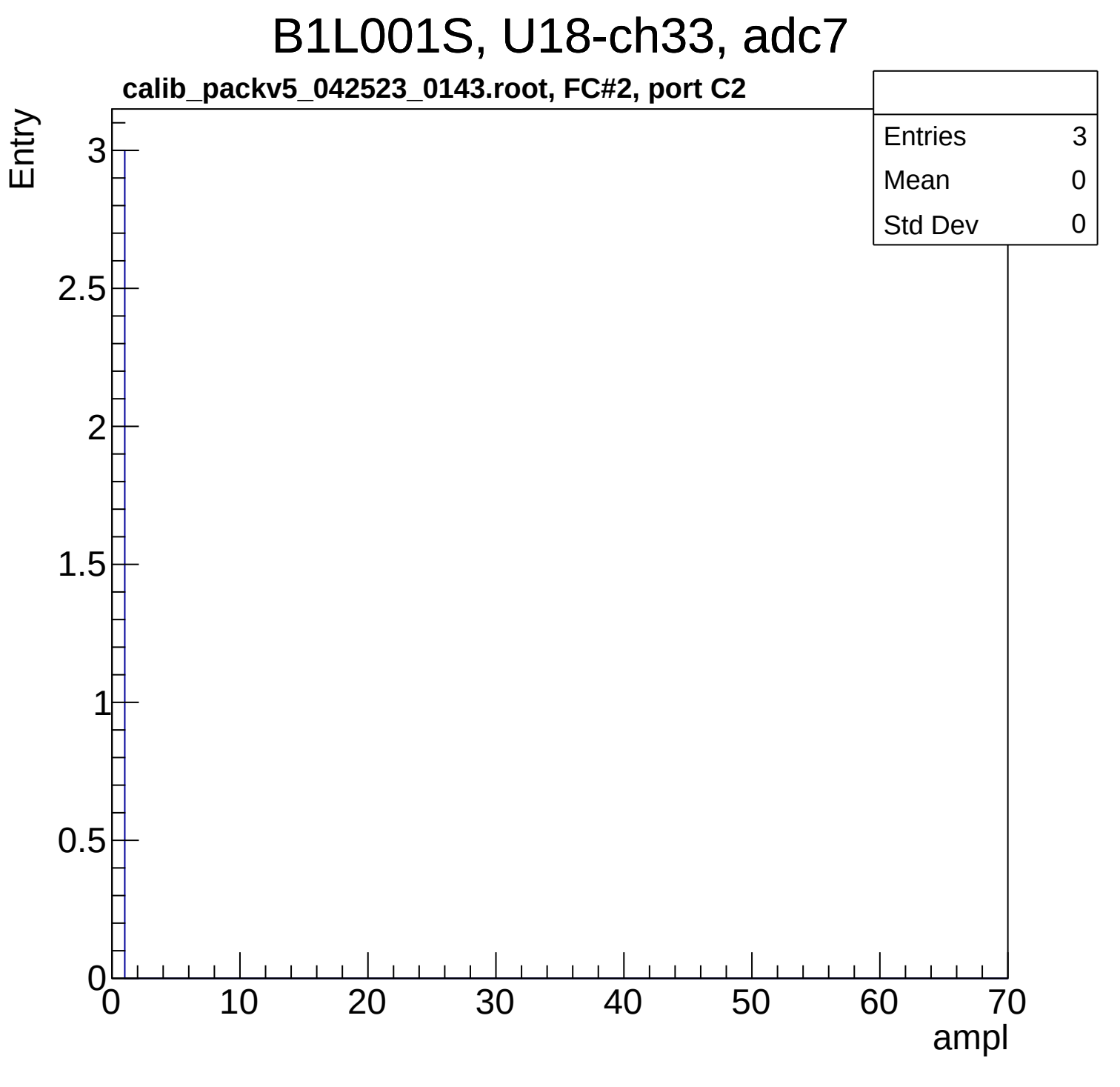

B1L001S, U18-ch33, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 153
Mean 45.66
Std Dev 3.545
Gaus mean : 46.2172
Gaus Width: 3.4960
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

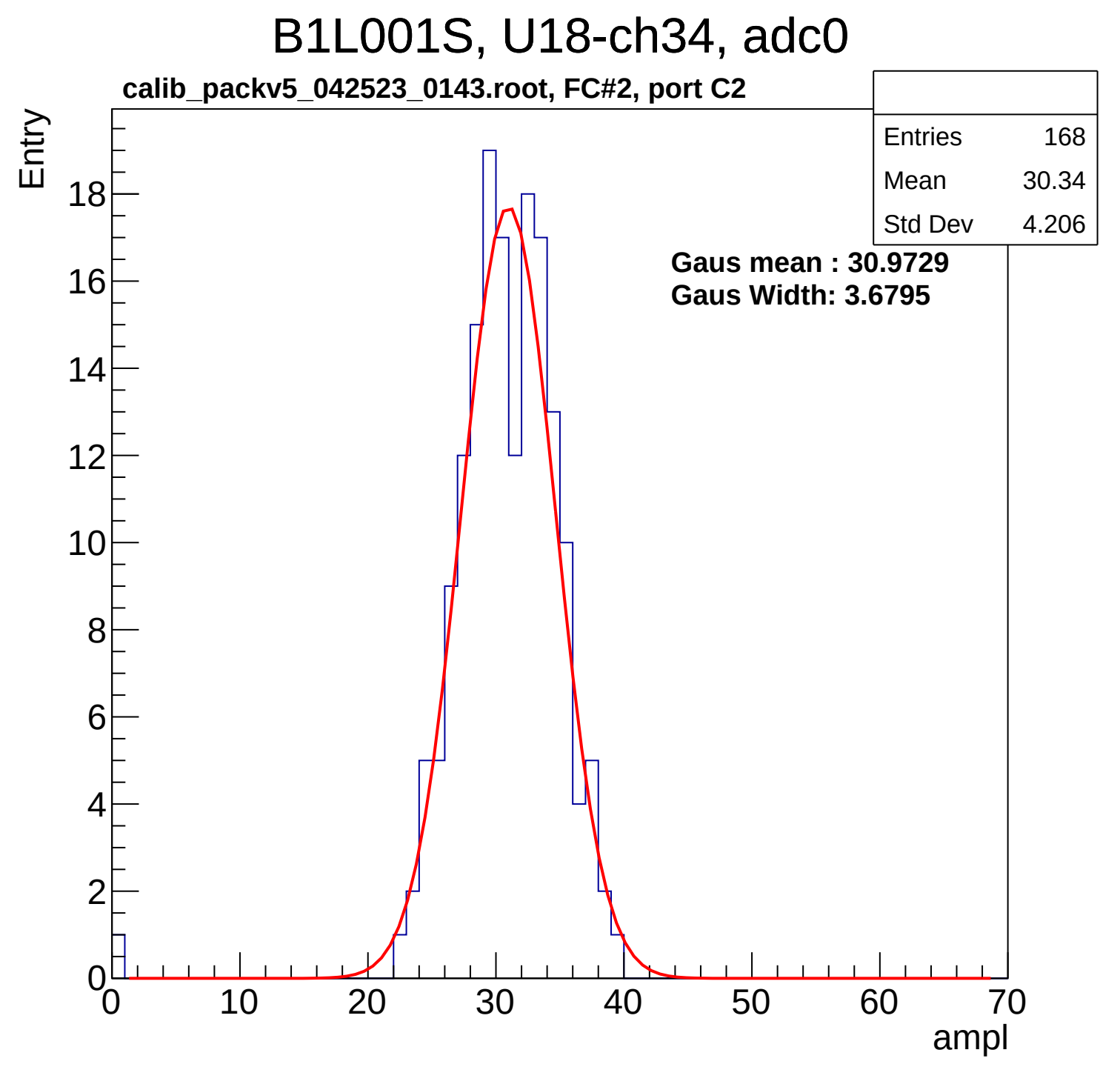

B1L001S, U18-ch33, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 115
Mean 52
Std Dev 3.244
Entry
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl

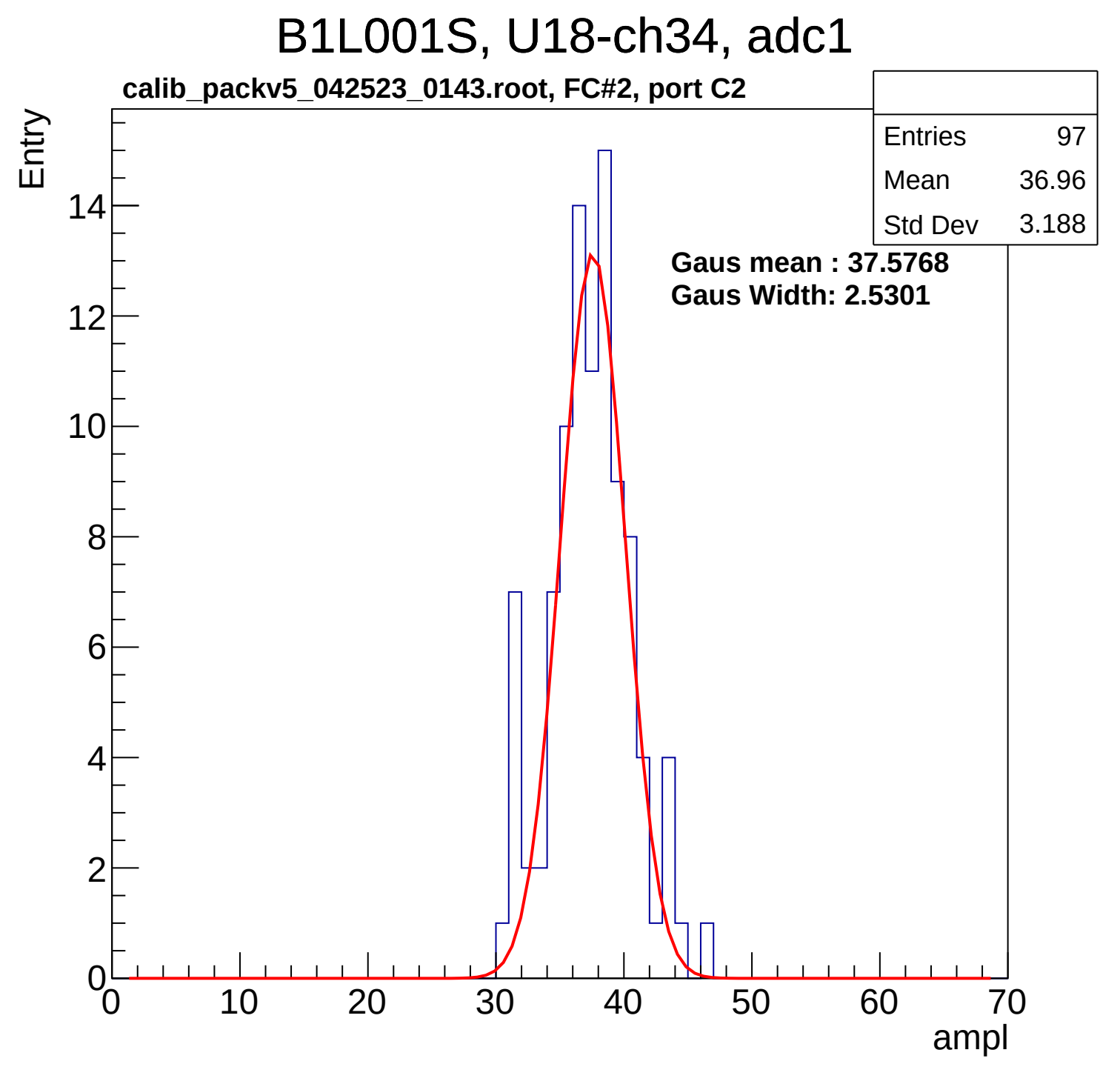

B1L001S, U18-ch33, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 94
Mean 57.71
Std Dev 2.938
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl

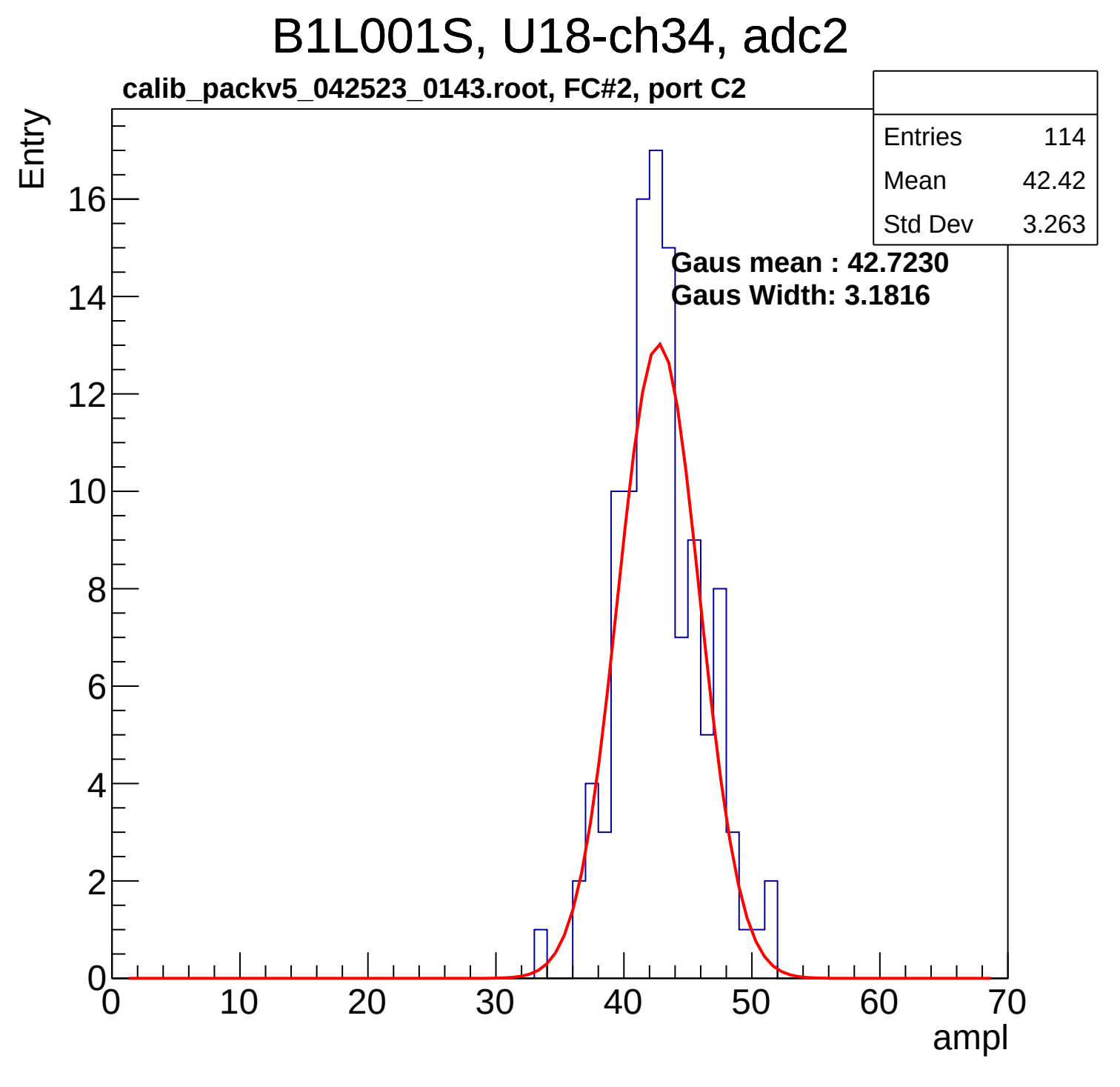

B1L001S, U18-ch33, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 74
Mean 58.78
Std Dev 10.04
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

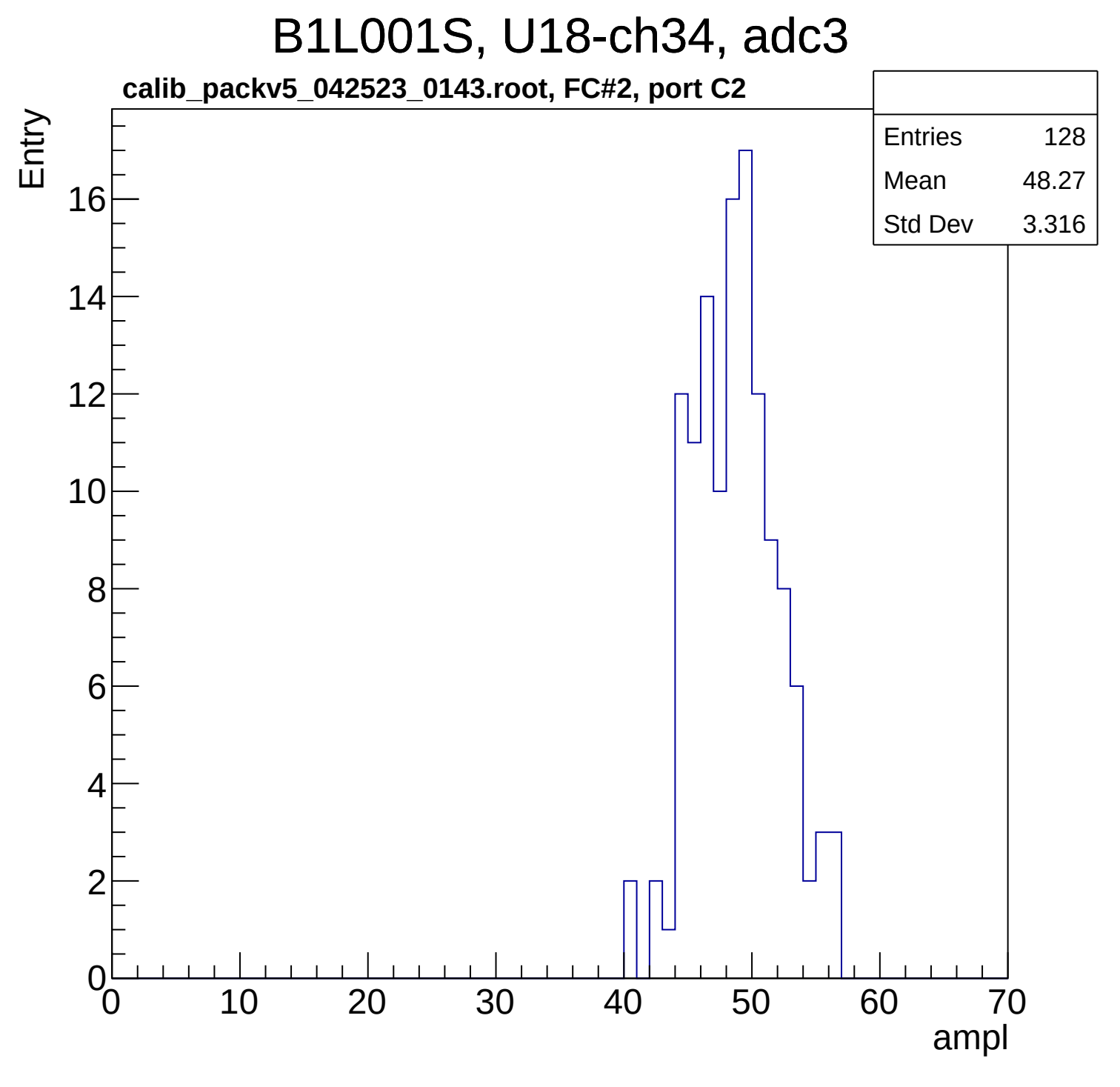

B1L001S, U18-ch33, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 62.5
Std Dev 0.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

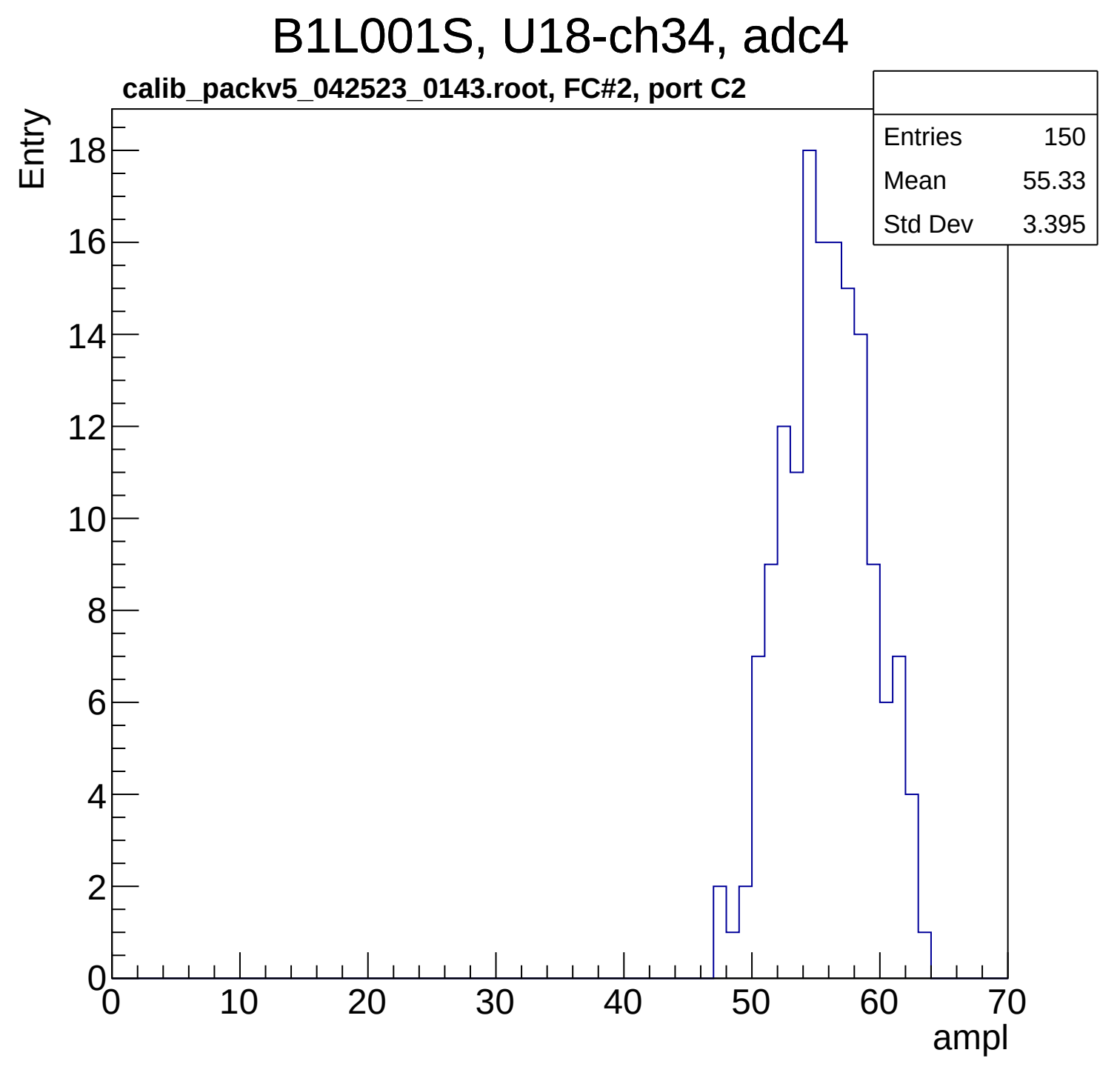

B1L001S, U18-ch33, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 3
Mean 0
Std Dev 0
Entry
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70
ampl

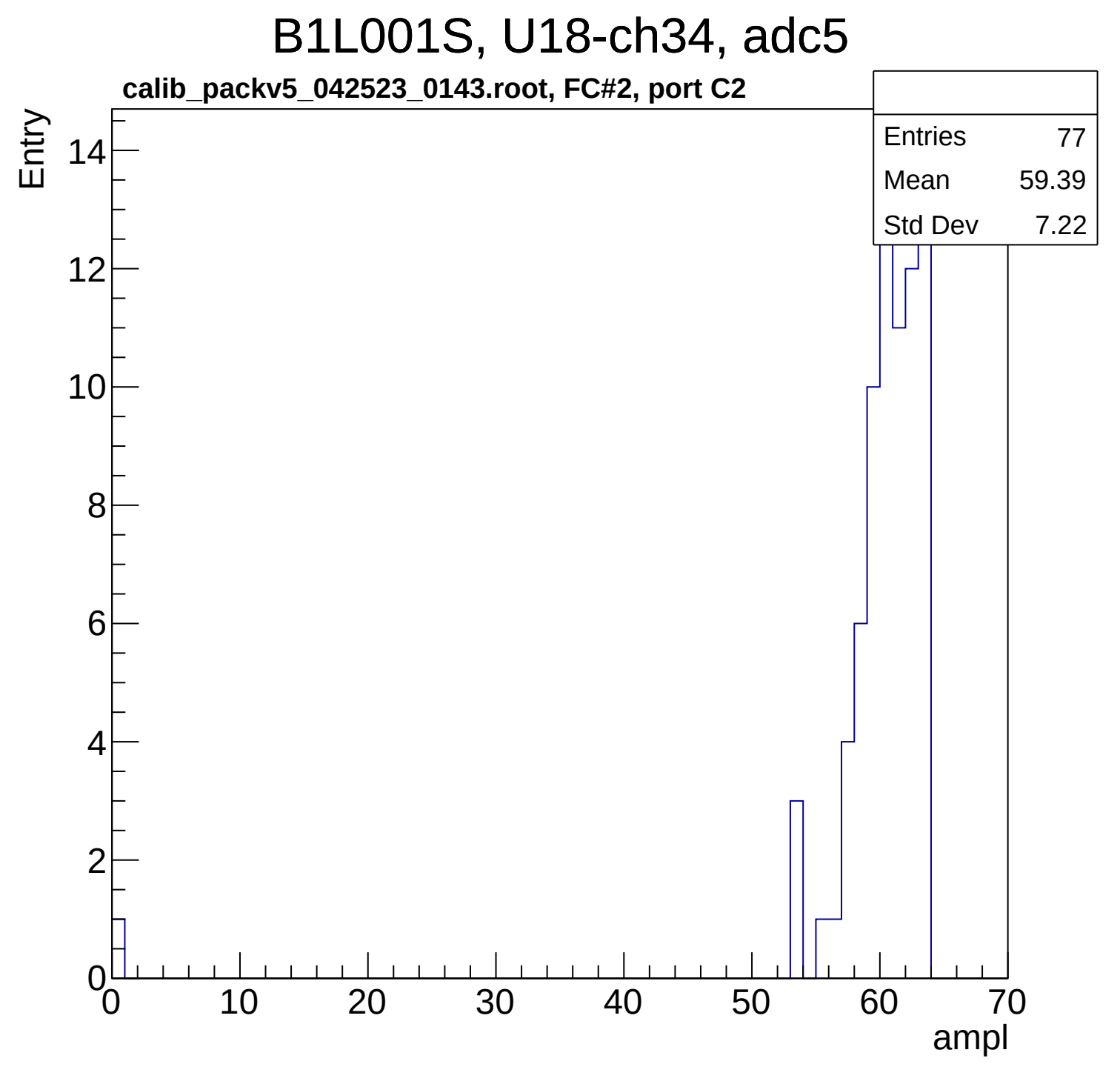

B1L001S, U18-ch34, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 168
Mean 30.34
Std Dev 4.206
Gaus mean : 30.9729
Gaus Width: 3.6795
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

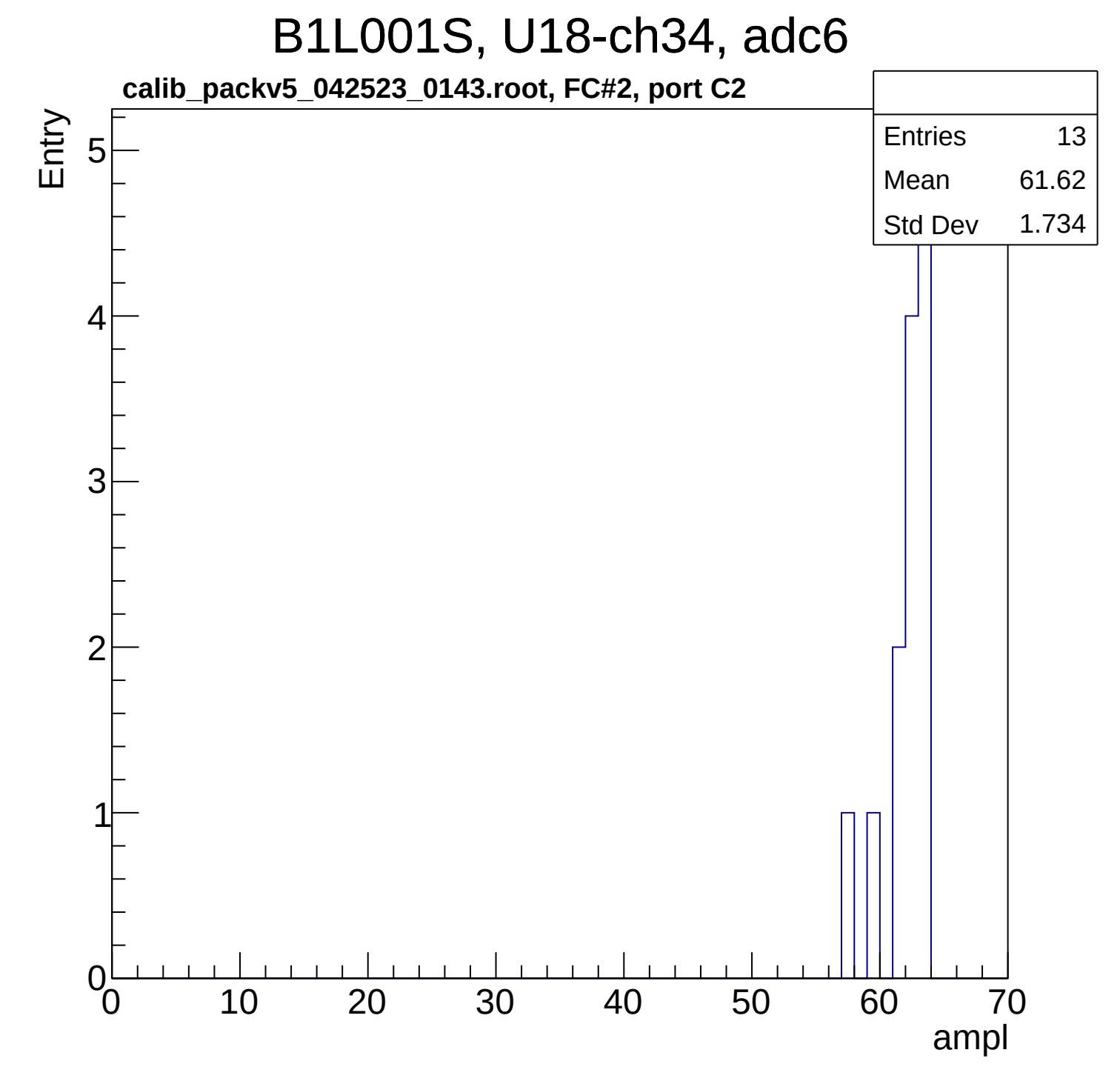

B1L001S, U18-ch34, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 97
Mean 36.96
Std Dev 3.188
Gaus mean : 37.5768
Gaus Width: 2.5301
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

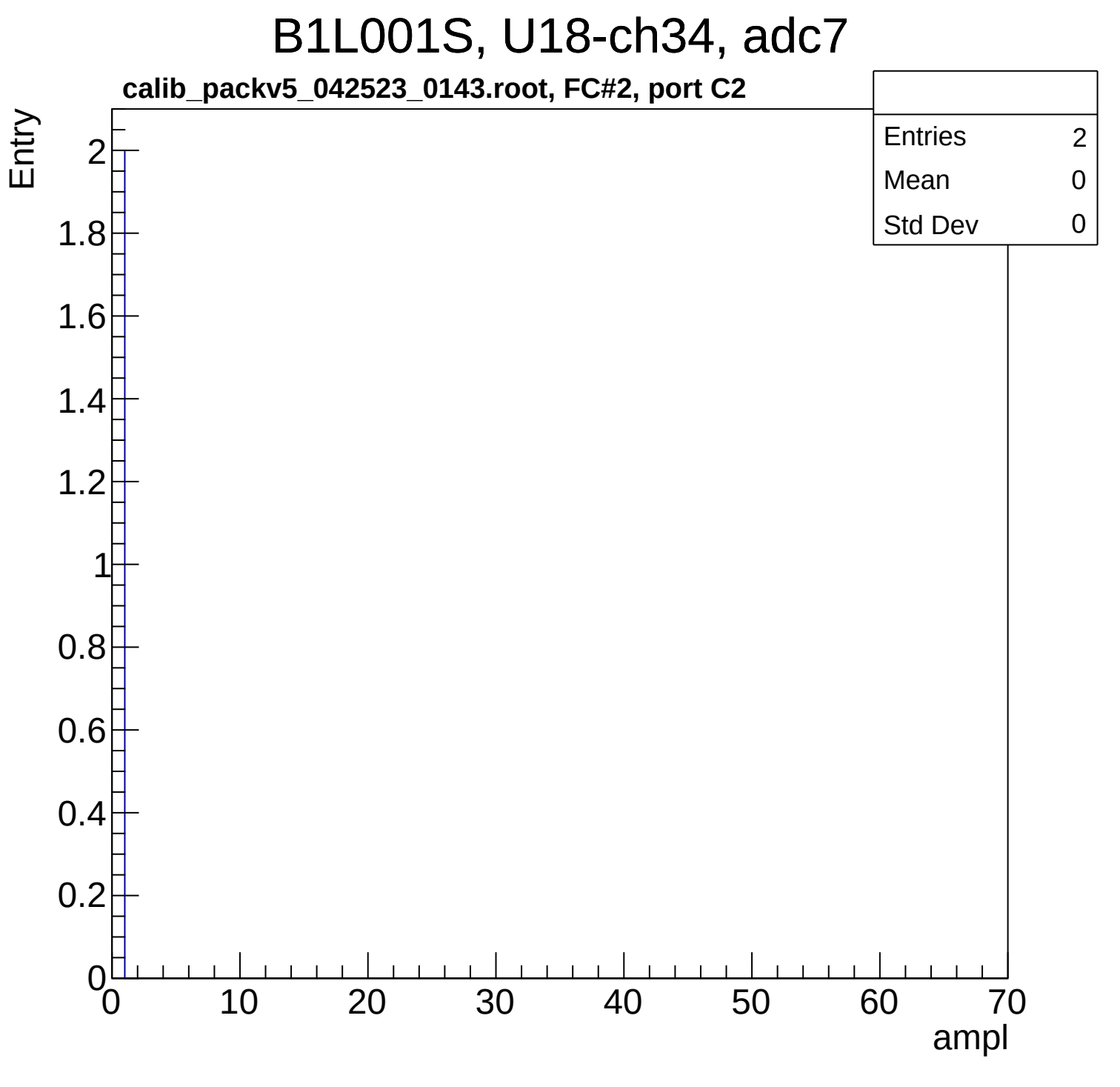

B1L001S, U18-ch34, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 114
Mean 42.42
Std Dev 3.263
Gaus mean : 42.7230
Gaus Width: 3.1816
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

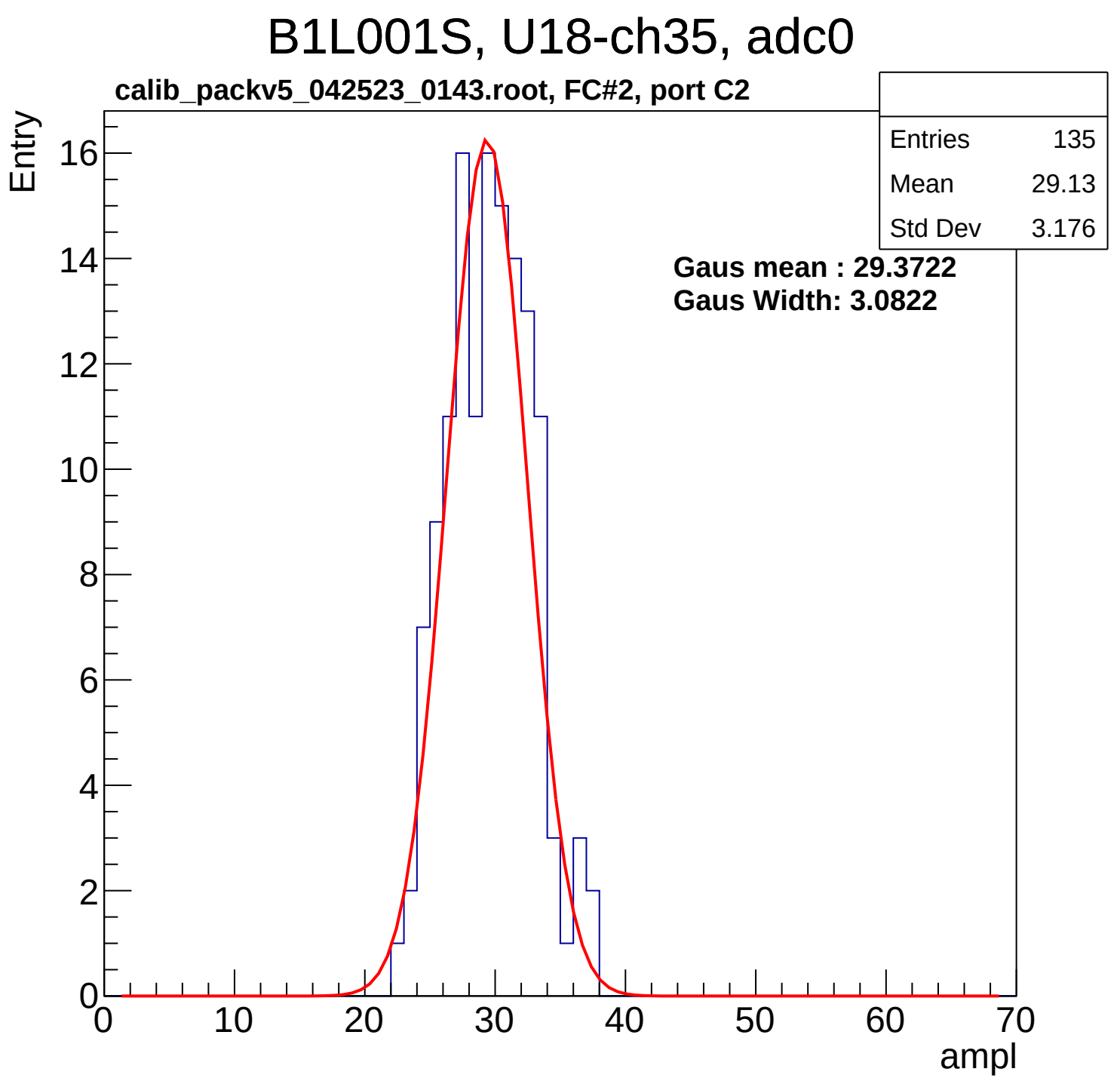

B1L001S, U18-ch34, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 128
Mean 48.27
Std Dev 3.316
Entry
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl

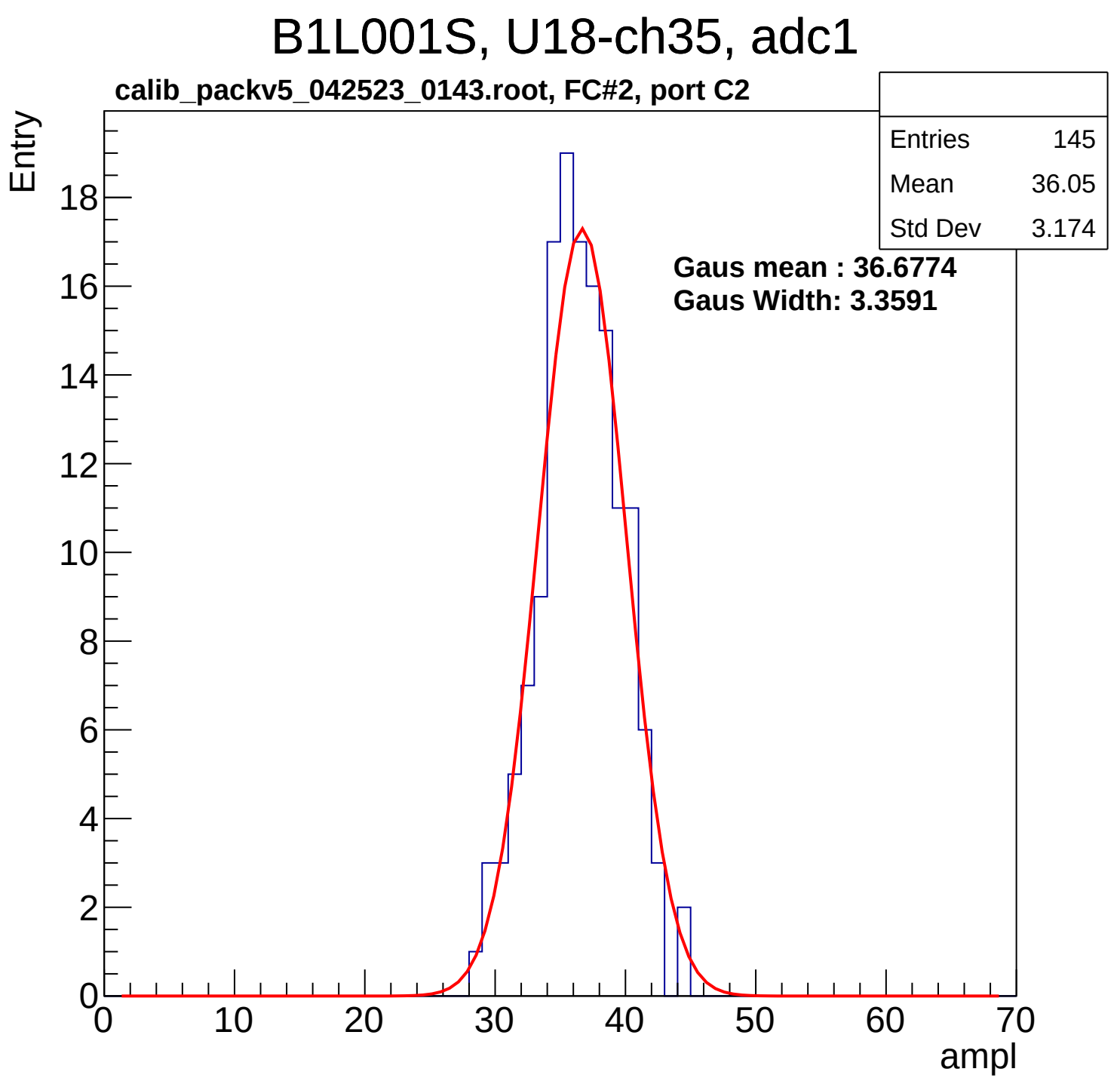

B1L001S, U18-ch34, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 150
Mean 55.33
Std Dev 3.395
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

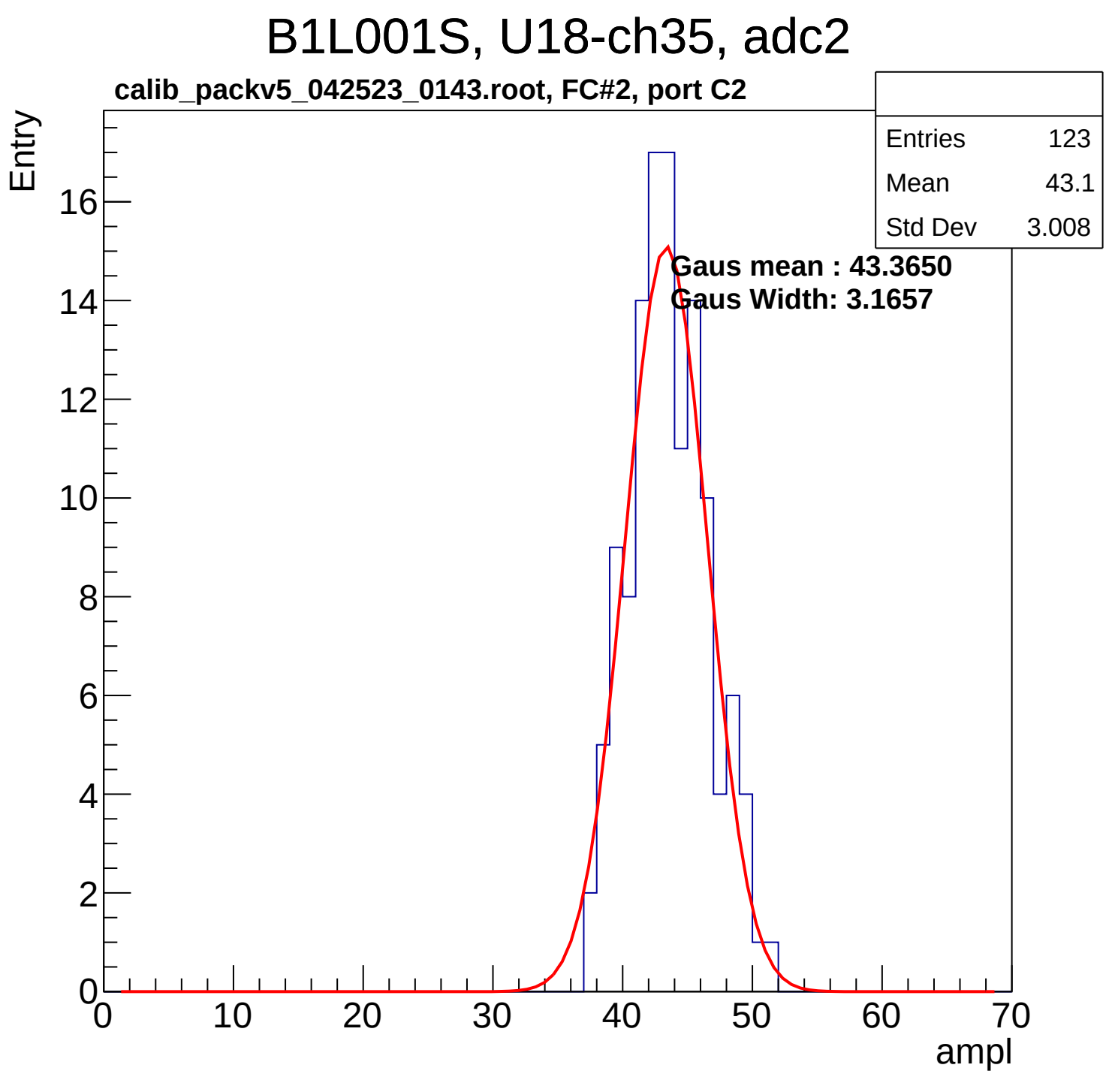

B1L001S, U18-ch34, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 77
Mean 59.39
Std Dev 7.22
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

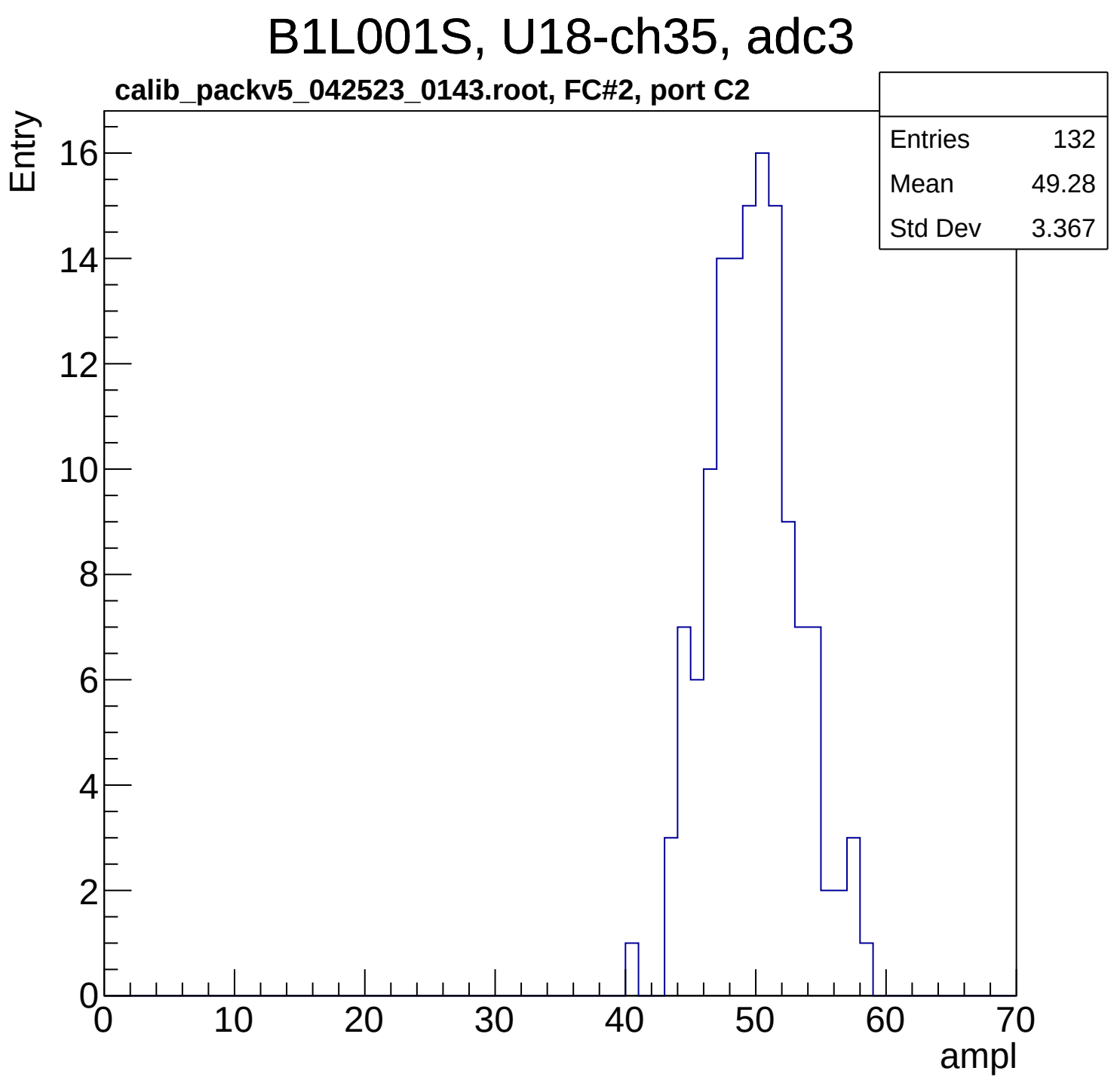

B1L001S, U18-ch34, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 13
Mean 61.62
Std Dev 1.734
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

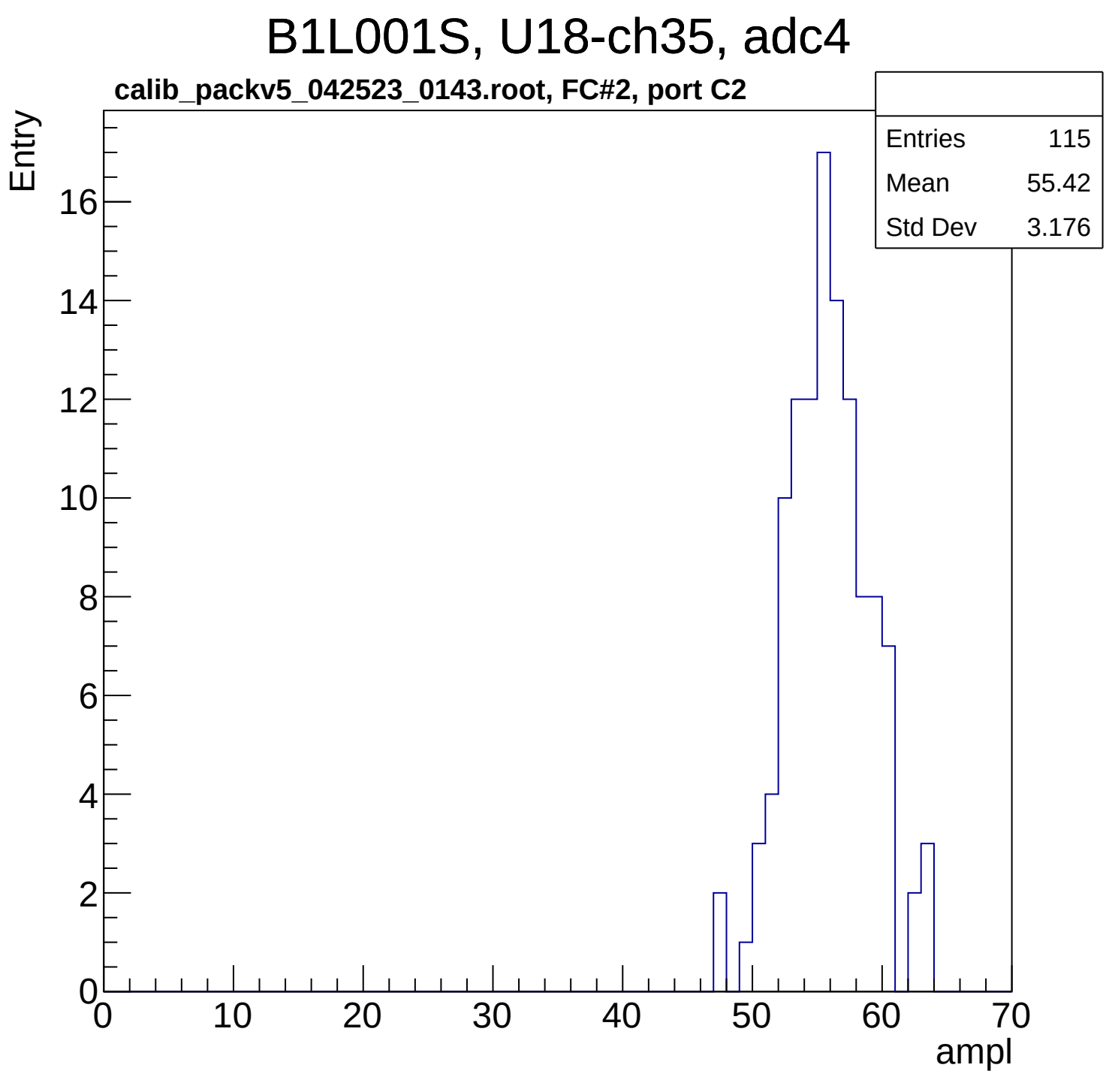

B1L001S, U18-ch34, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 0
Std Dev 0
Entry
2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

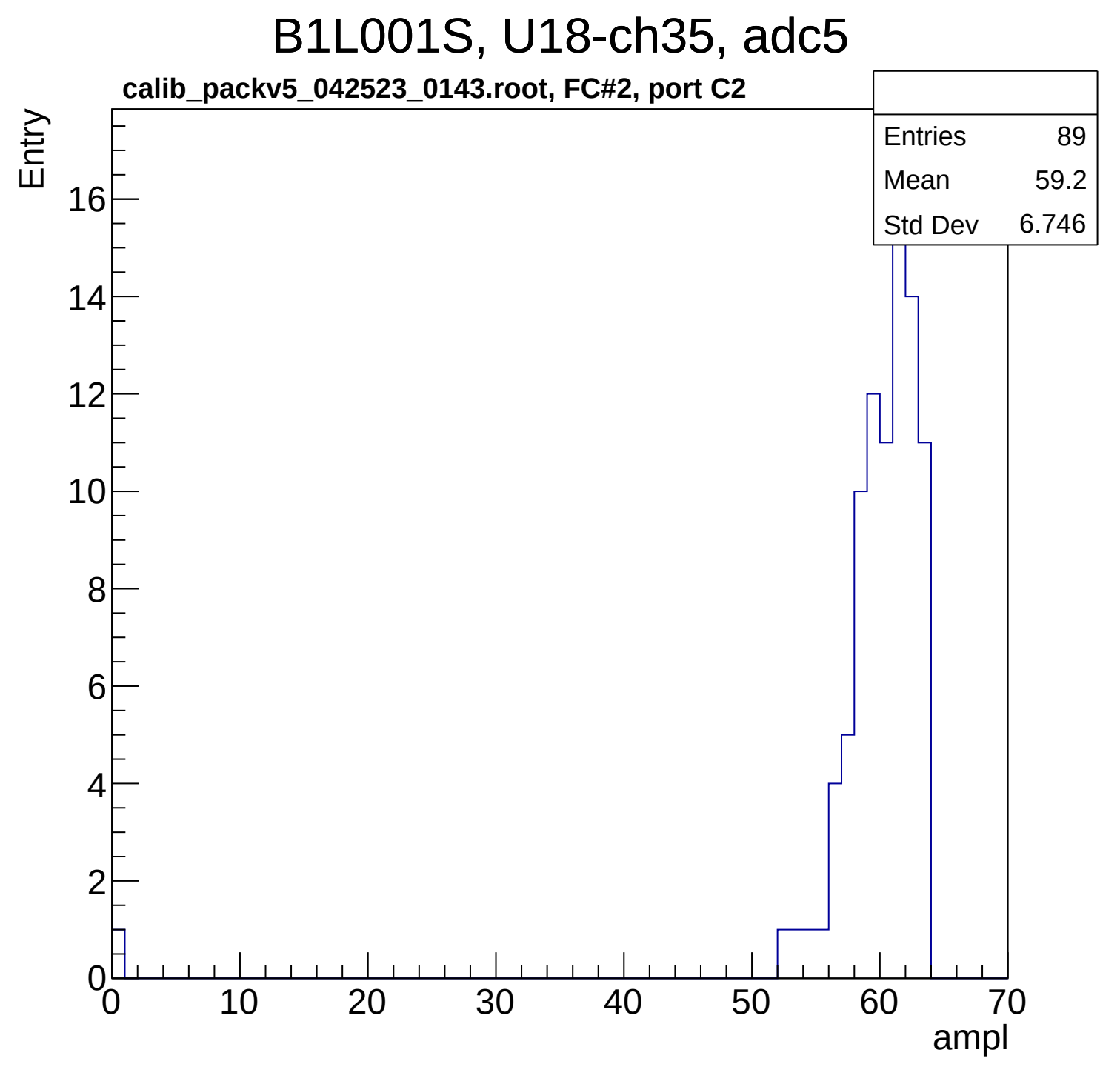

B1L001S, U18-ch35, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 135
Mean 29.13
Std Dev 3.176
Gaus mean : 29.3722
Gaus Width: 3.0822
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

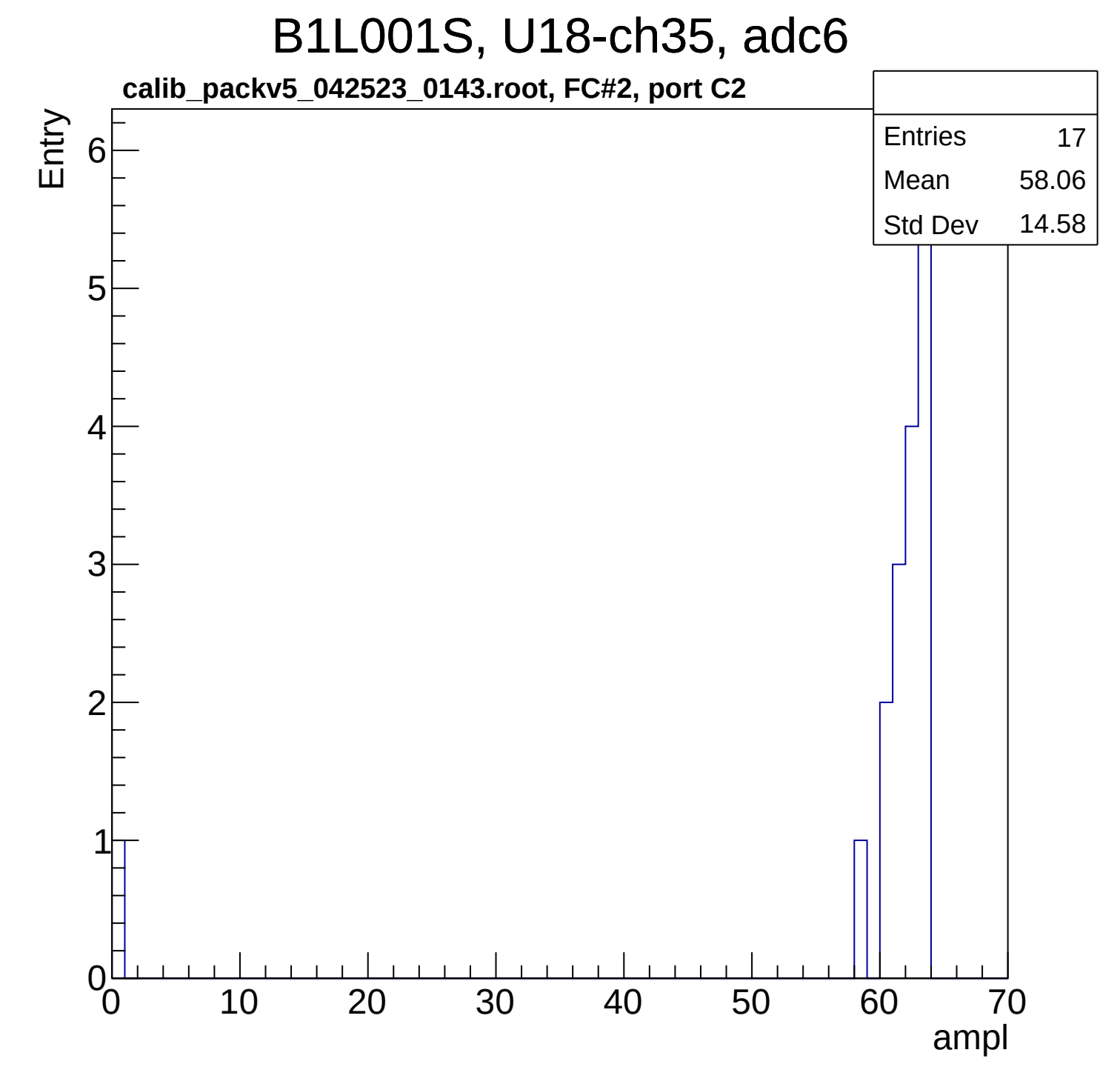

B1L001S, U18-ch35, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 145
Mean 36.05
Std Dev 3.174
Gaus mean : 36.6774
Gaus Width: 3.3591
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

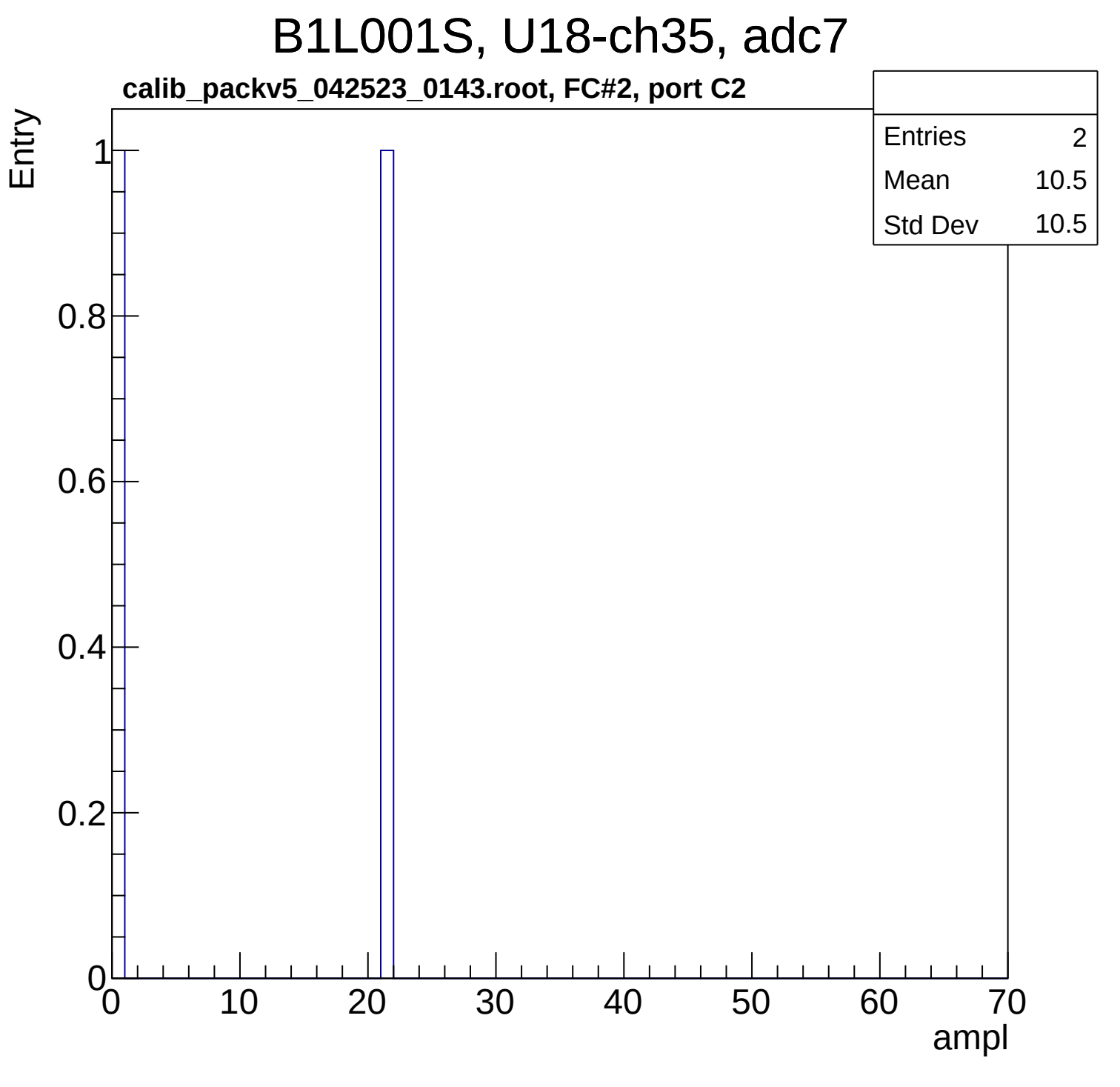

B1L001S, U18-ch35, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 123
Mean 43.1
Std Dev 3.008
Gaus mean : 43.3650
Gaus Width: 3.1657
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

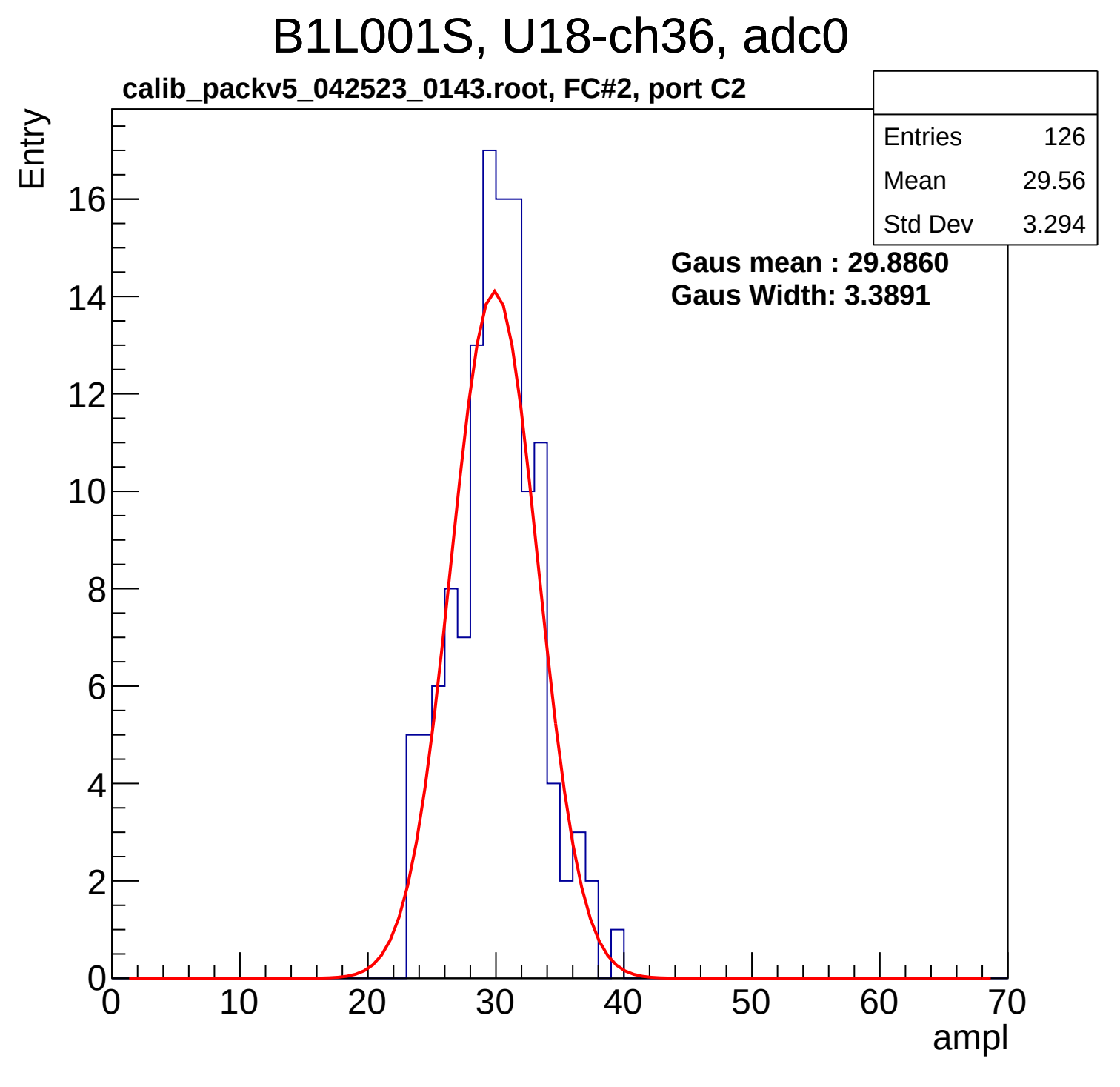

B1L001S, U18-ch35, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 132
Mean 49.28
Std Dev 3.367
Entry
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl

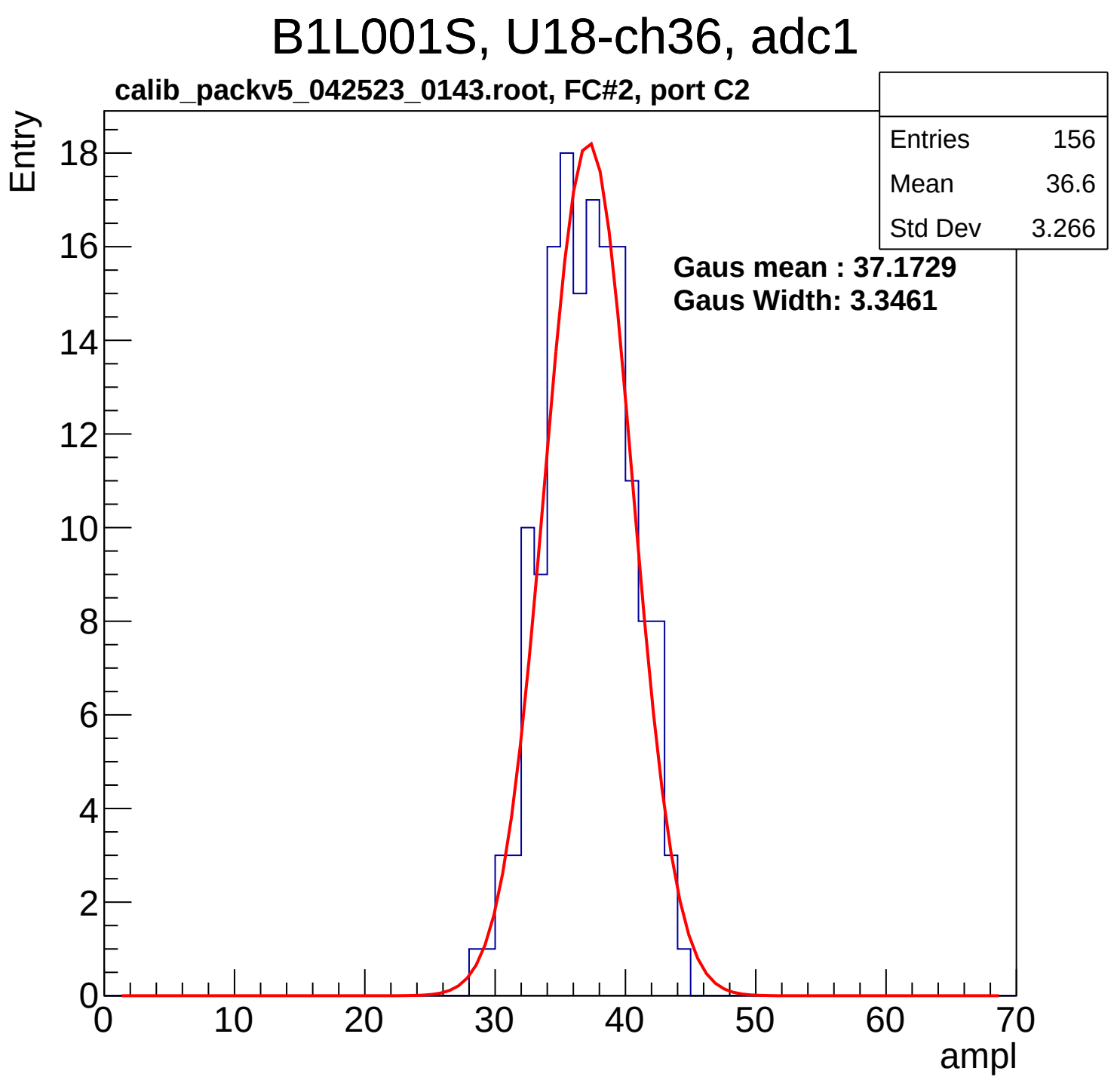

B1L001S, U18-ch35, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 115
Mean 55.42
Std Dev 3.176
Entry
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl

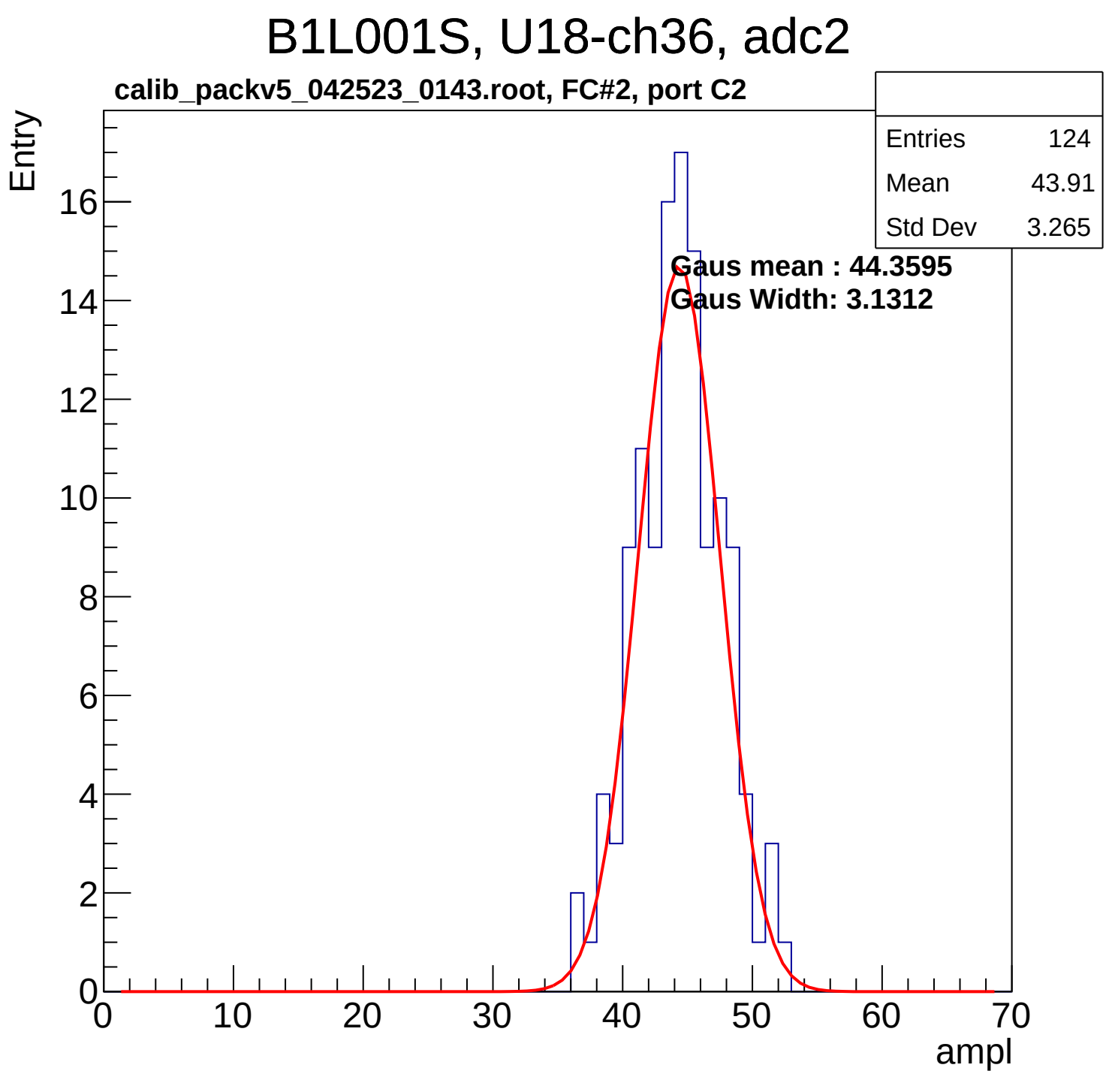

B1L001S, U18-ch35, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 89
Mean 59.2
Std Dev 6.746
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

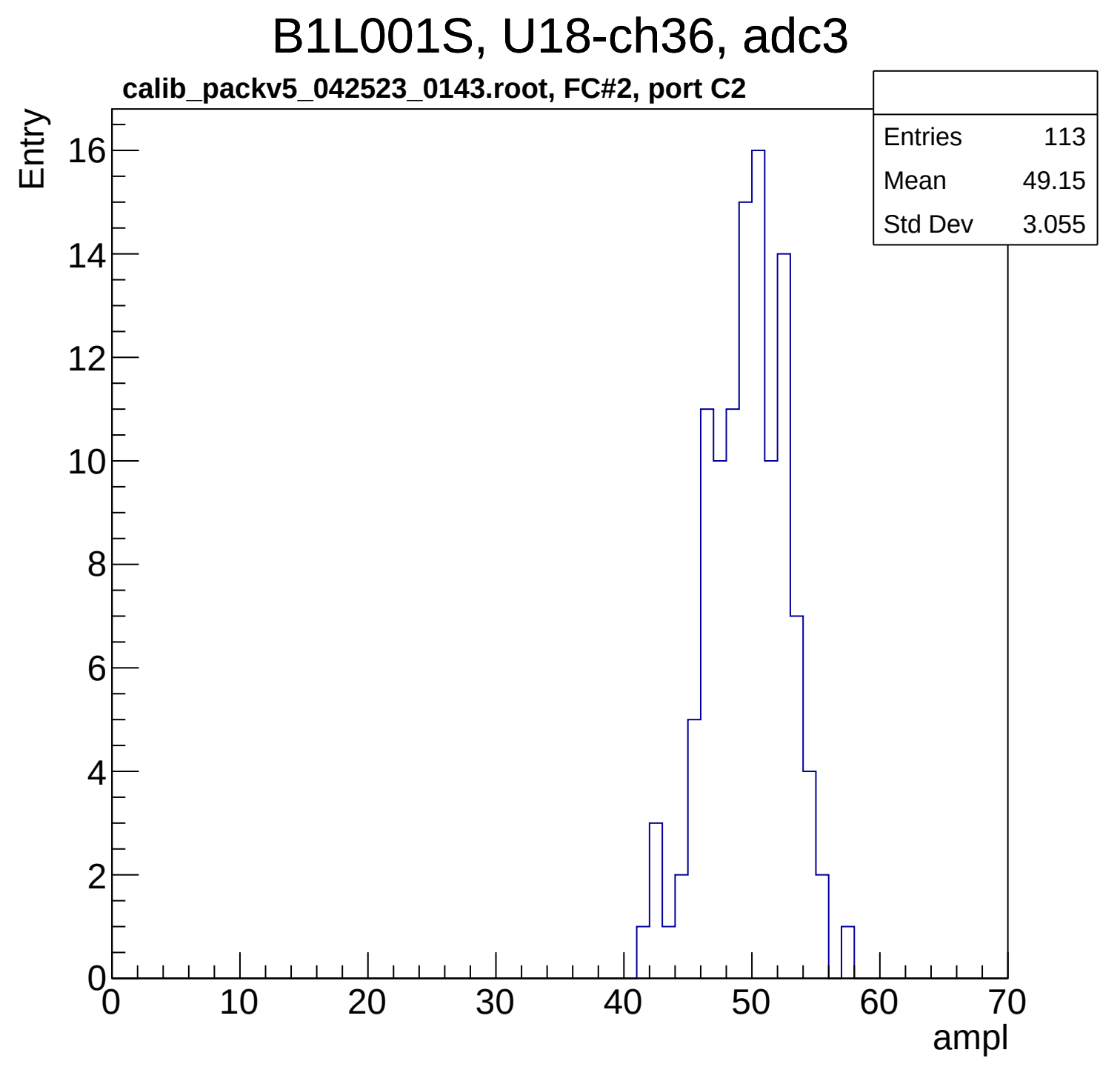

B1L001S, U18-ch35, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 17
Mean 58.06
Std Dev 14.58
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

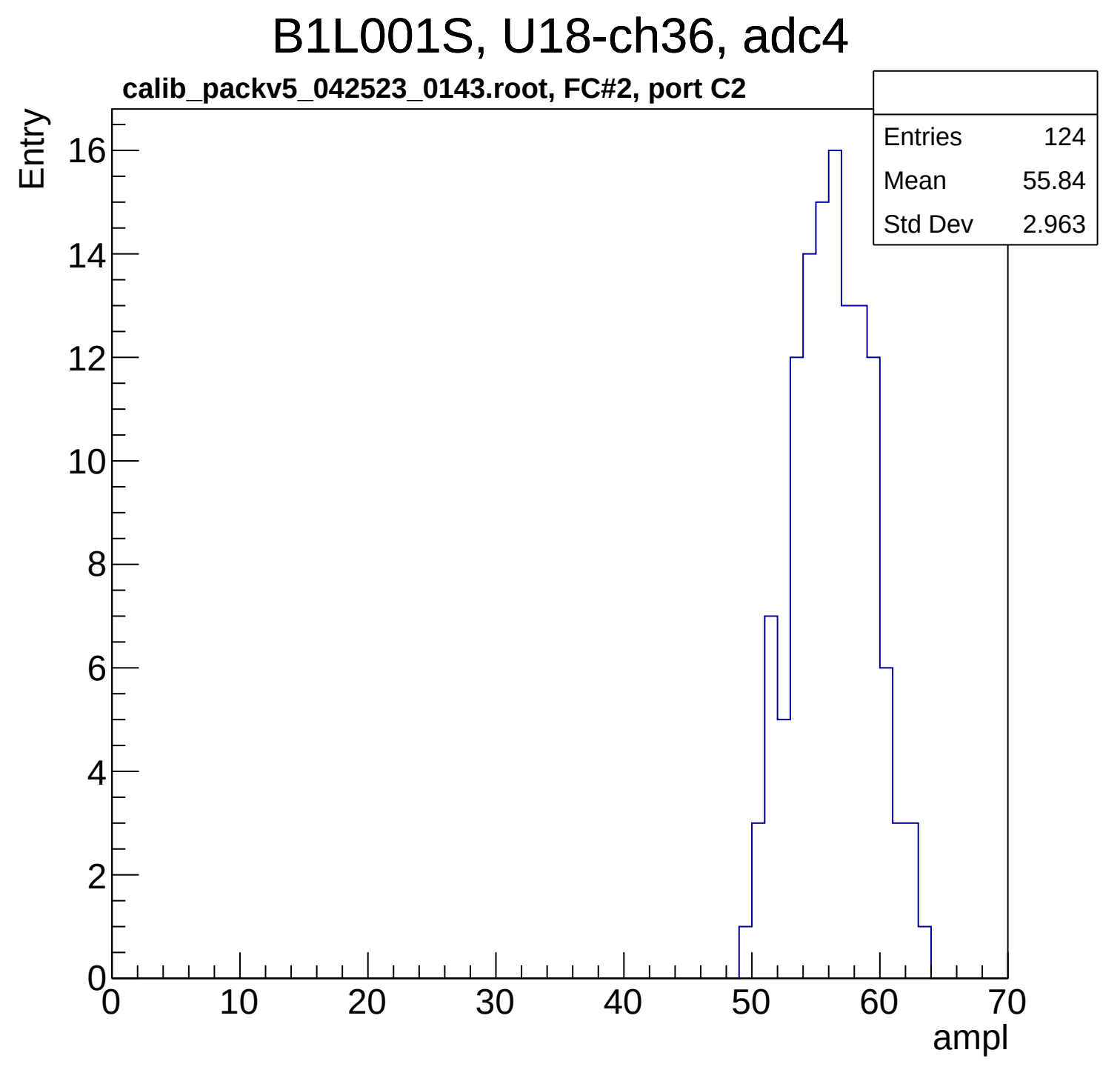

B1L001S, U18-ch35, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 10.5
Std Dev 10.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

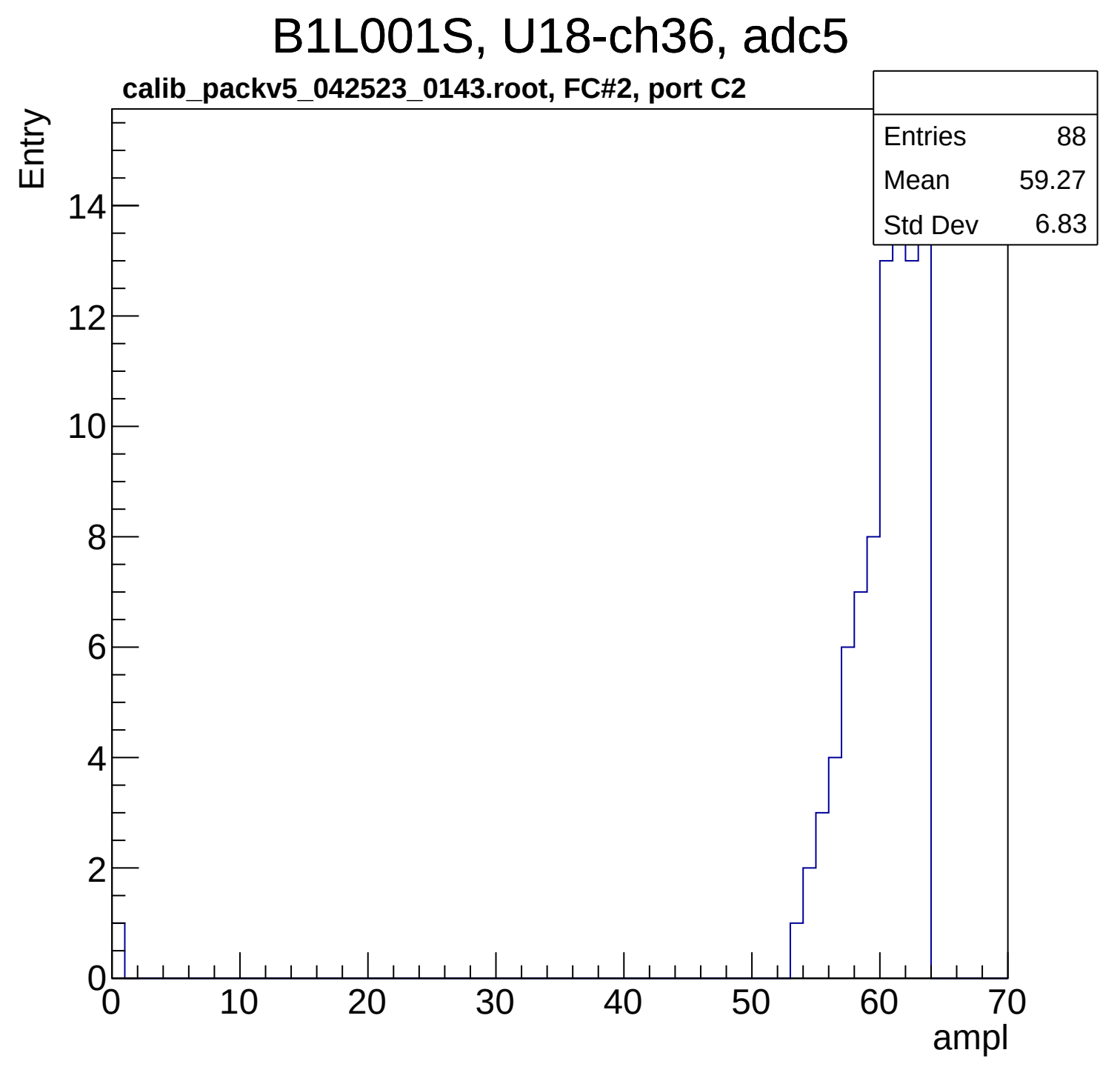

B1L001S, U18-ch36, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 126
Mean 29.56
Std Dev 3.294
Gaus mean : 29.8860
Gaus Width: 3.3891
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

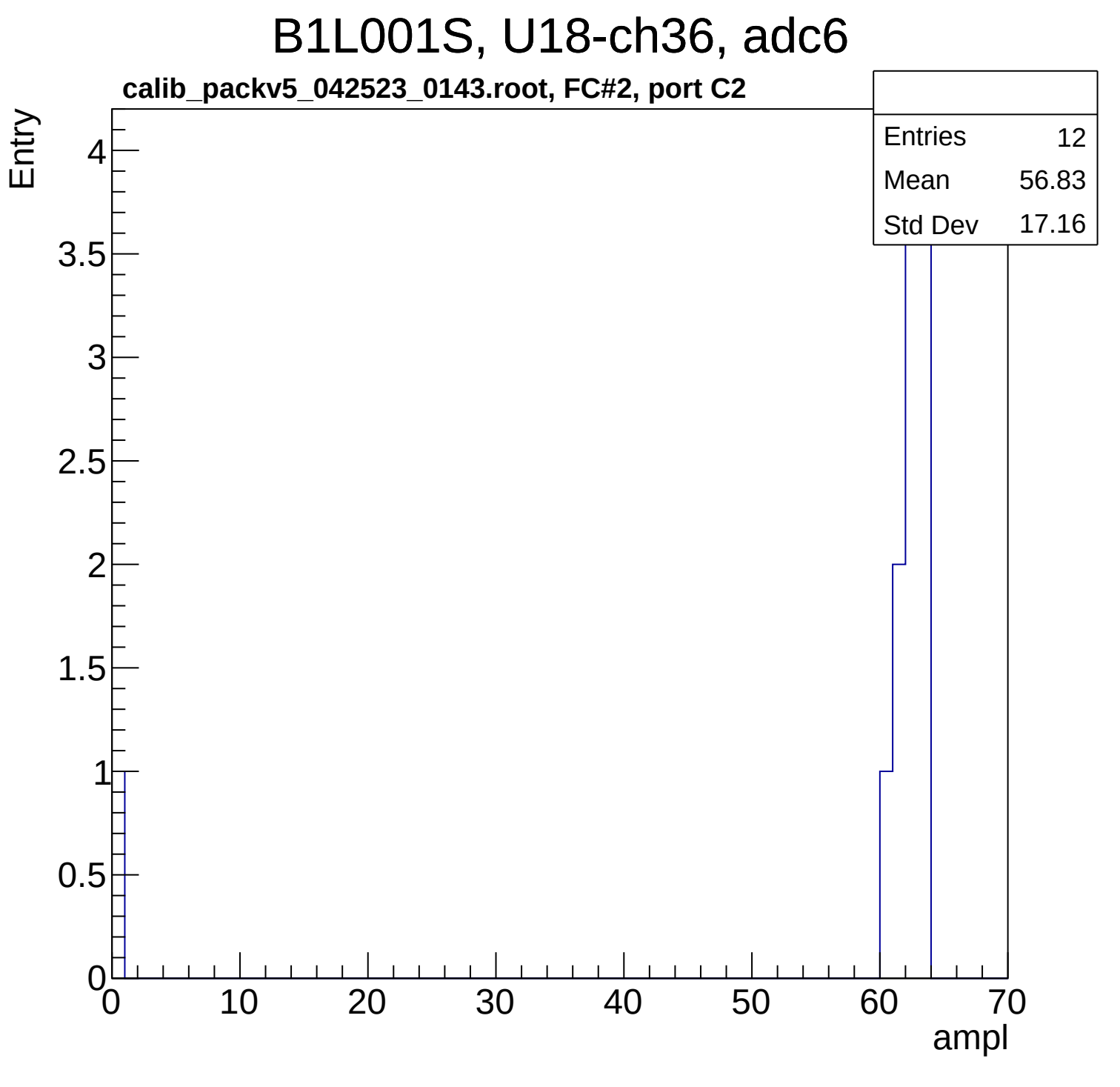

B1L001S, U18-ch36, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 156
Mean 36.6
Std Dev 3.266
Gaus mean : 37.1729
Gaus Width: 3.3461
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

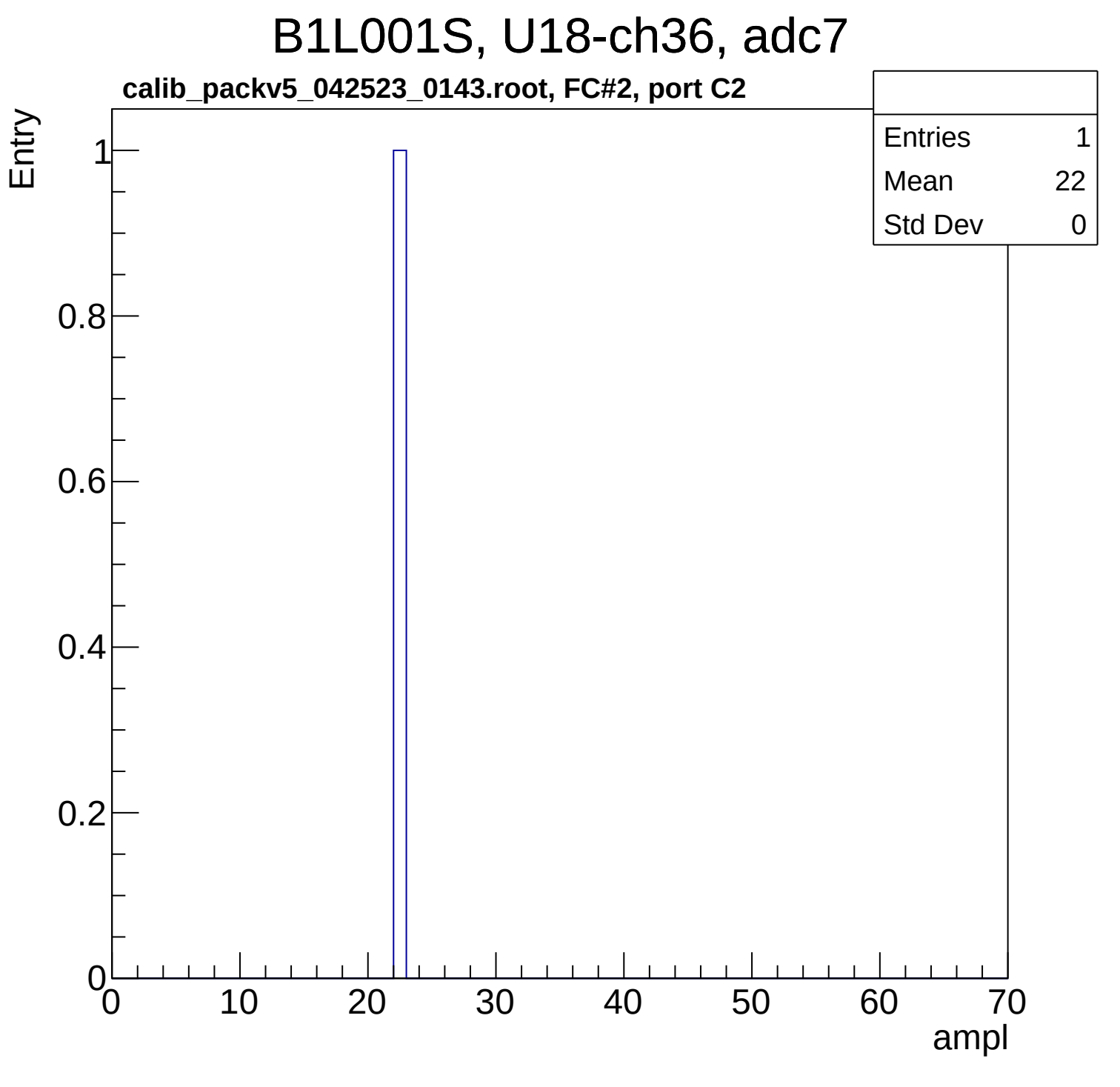

B1L001S, U18-ch36, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 124
Mean 43.91
Std Dev 3.265
Gaus mean : 44.3595
Gaus Width: 3.1312
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

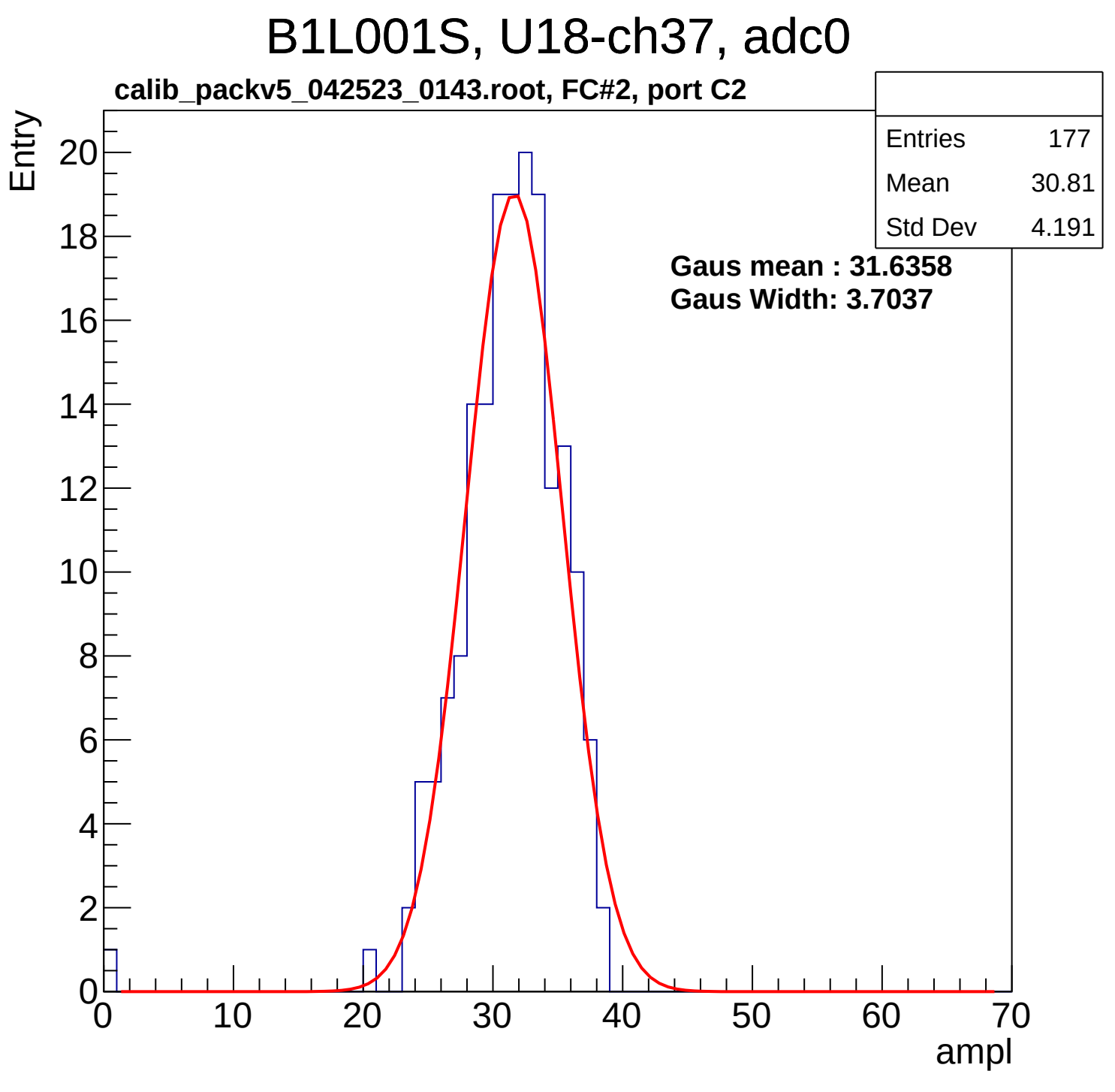

B1L001S, U18-ch36, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 113
Mean 49.15
Std Dev 3.055
Entry
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl

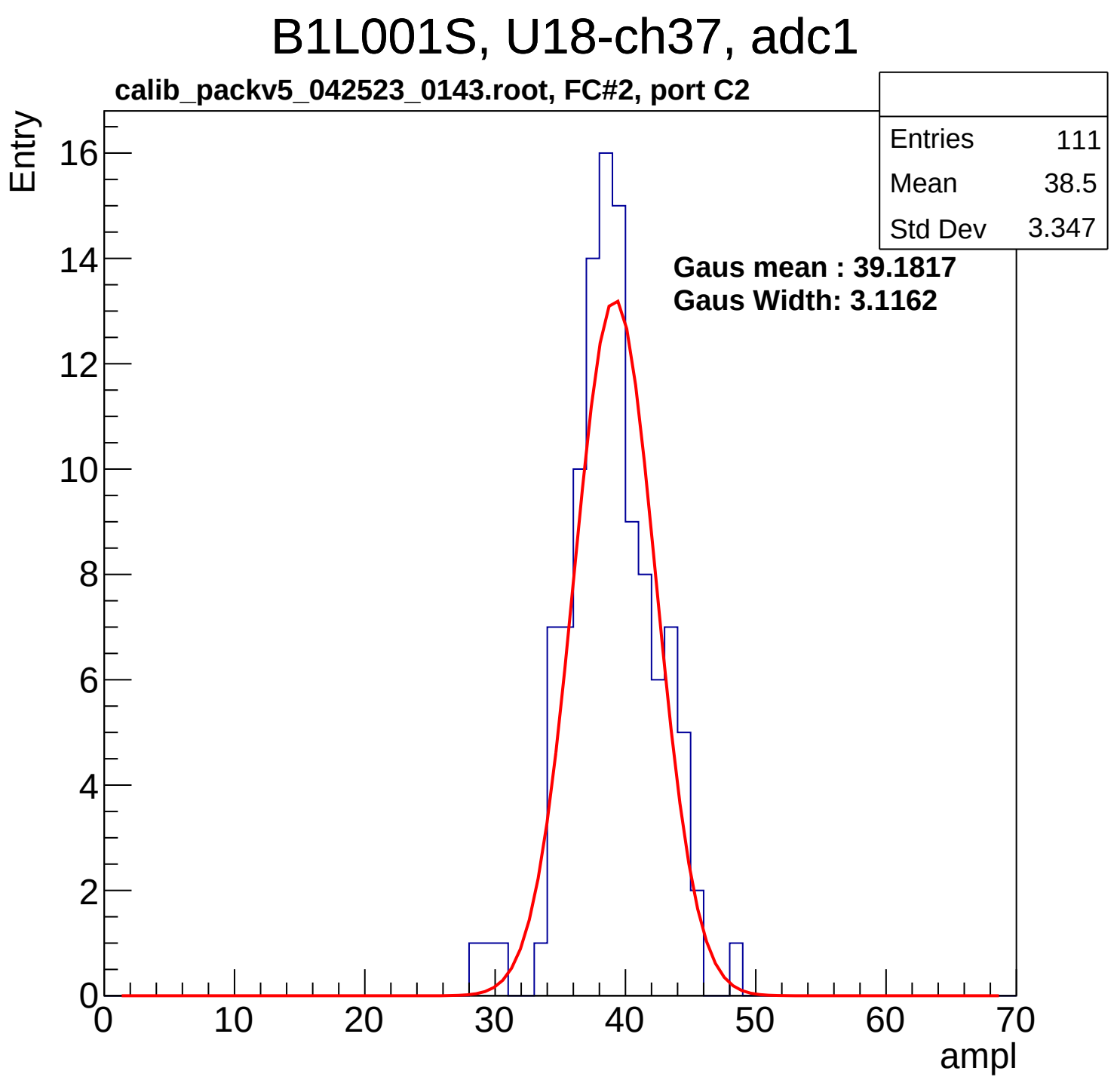

B1L001S, U18-ch36, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 124
Mean 55.84
Std Dev 2.963
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

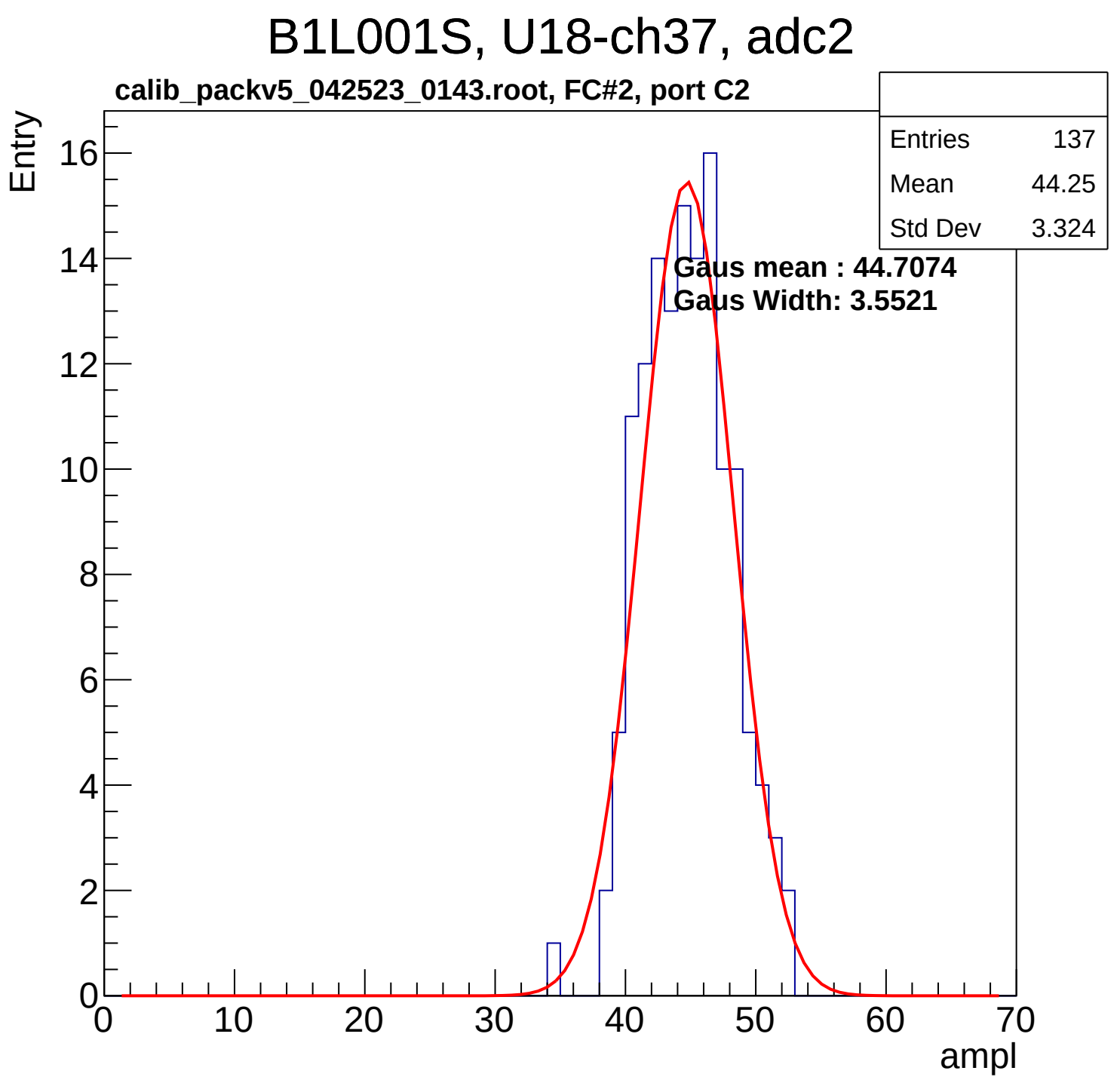

B1L001S, U18-ch36, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 88
Mean 59.27
Std Dev 6.83
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl

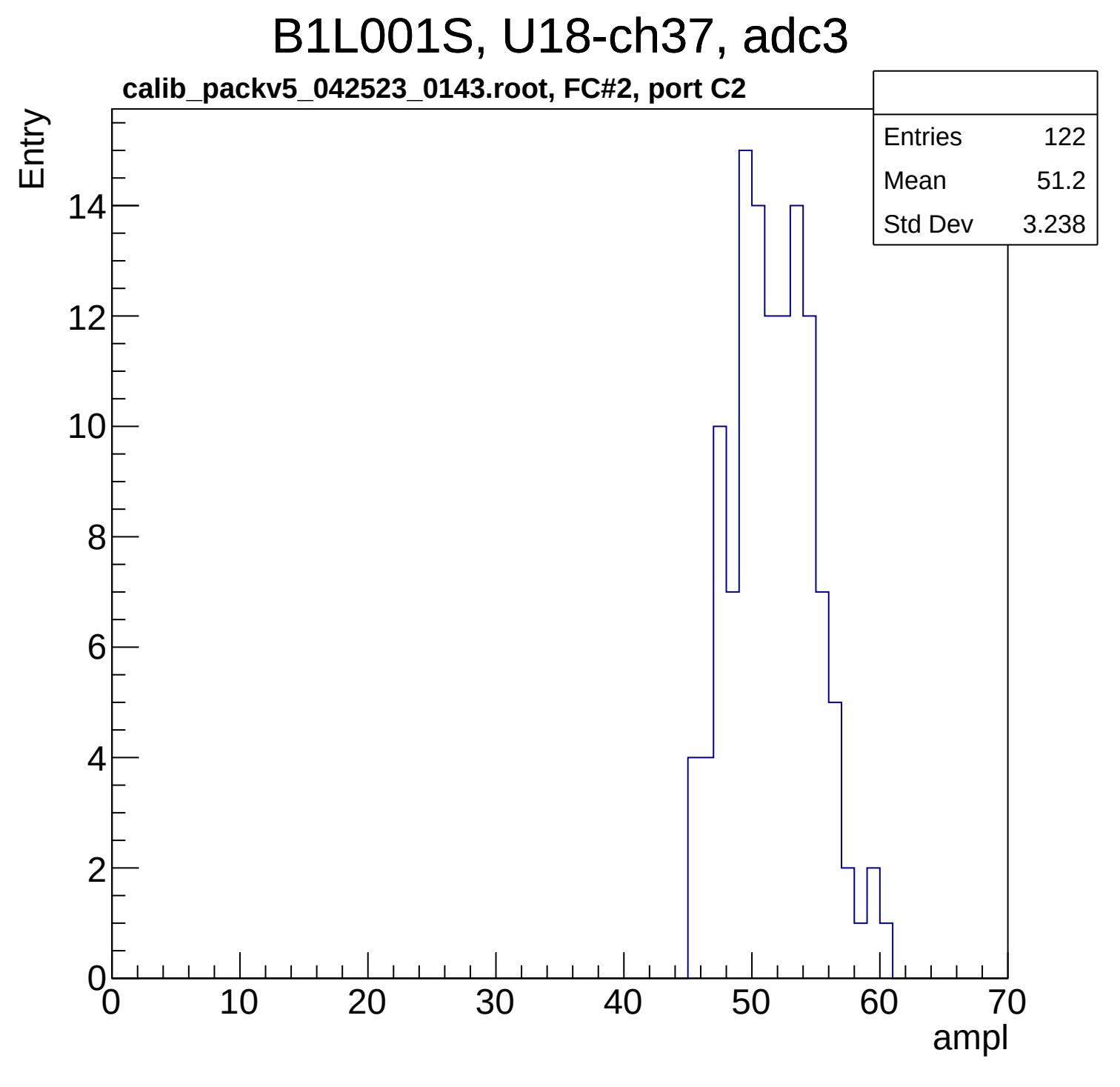

B1L001S, U18-ch36, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 12
Mean 56.83
Std Dev 17.16
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

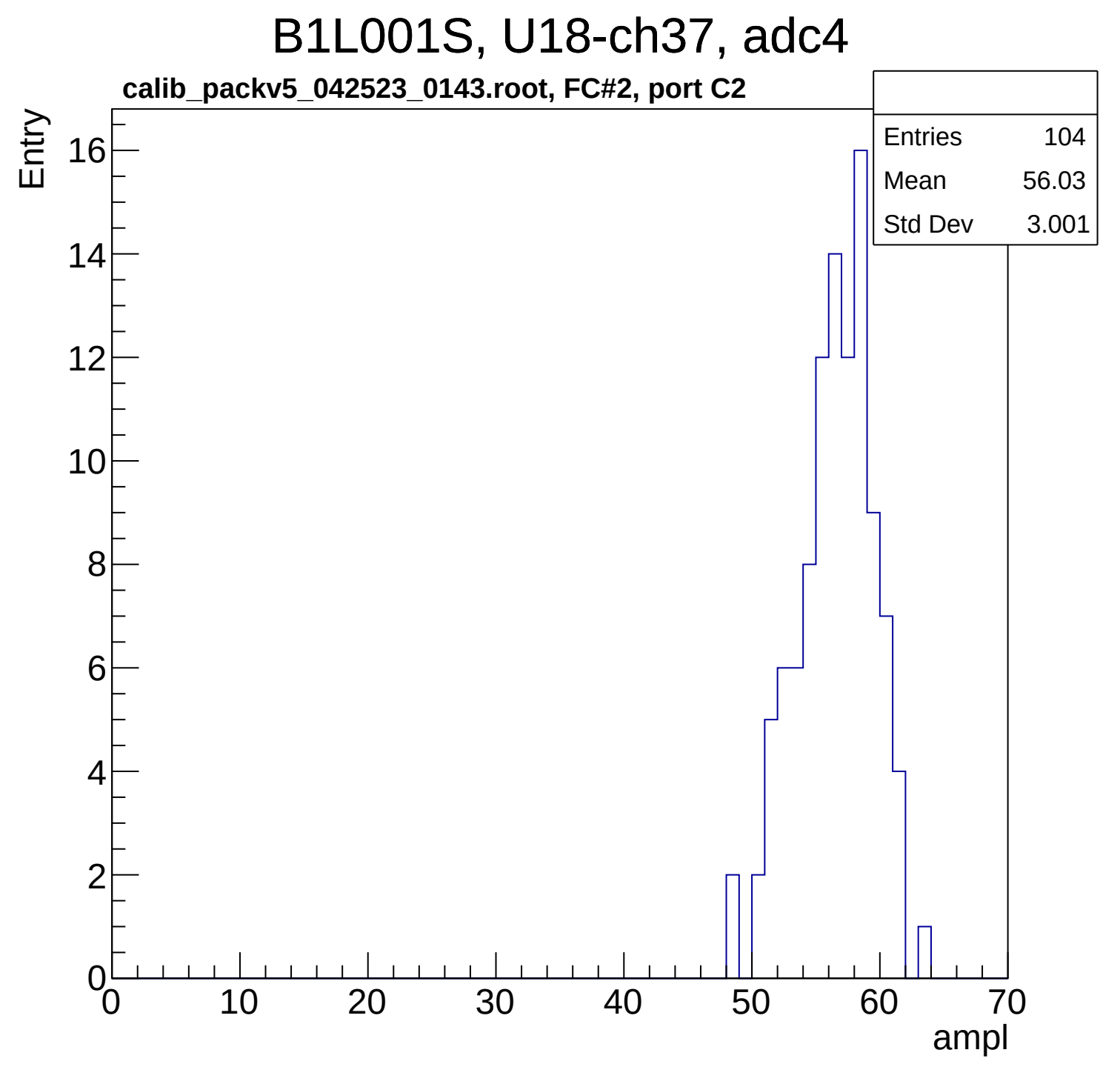

B1L001S, U18-ch36, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 22
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

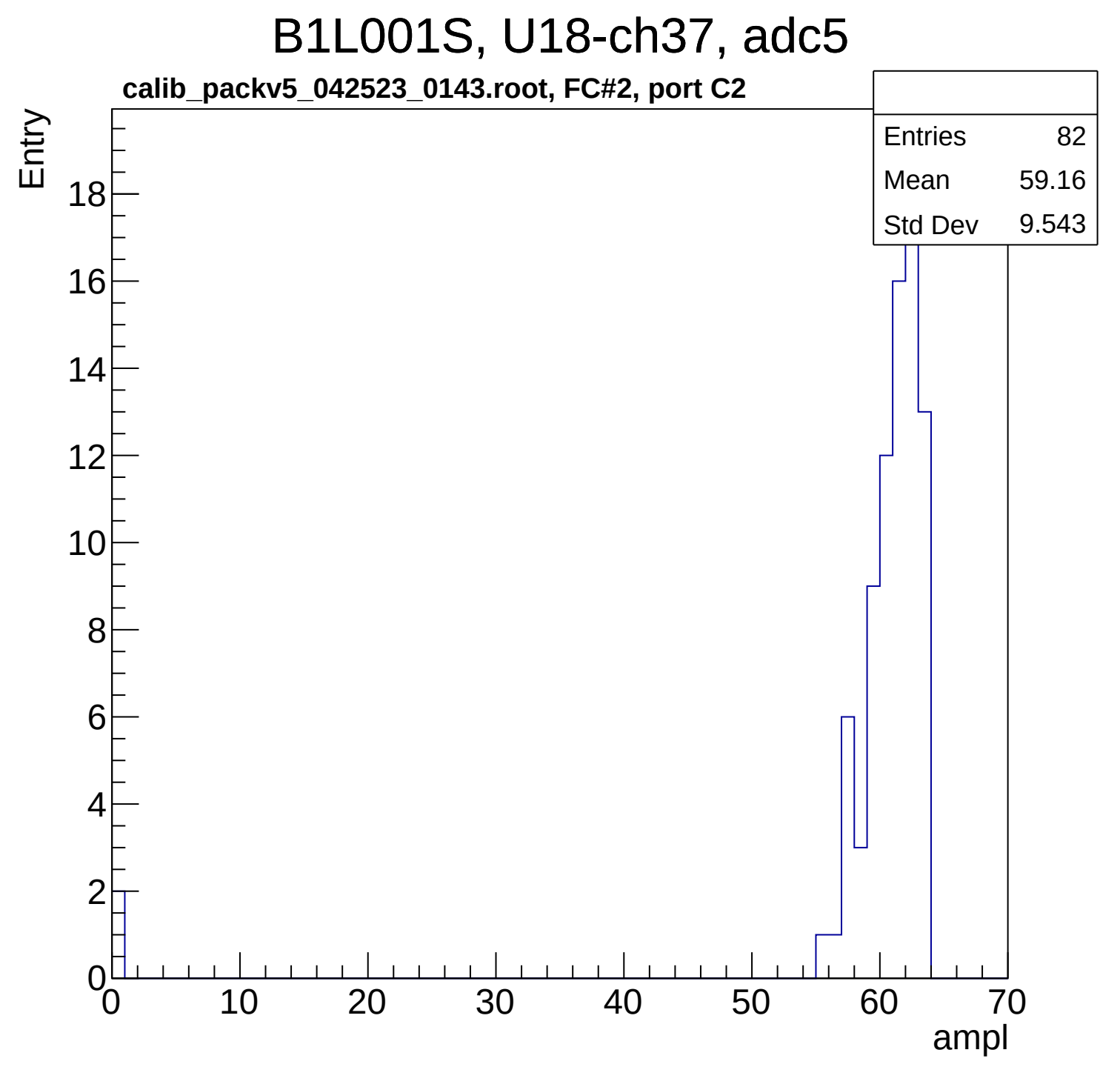

B1L001S, U18-ch37, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 177
Mean 30.81
Std Dev 4.191
Gaus mean : 31.6358
Gaus Width: 3.7037
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

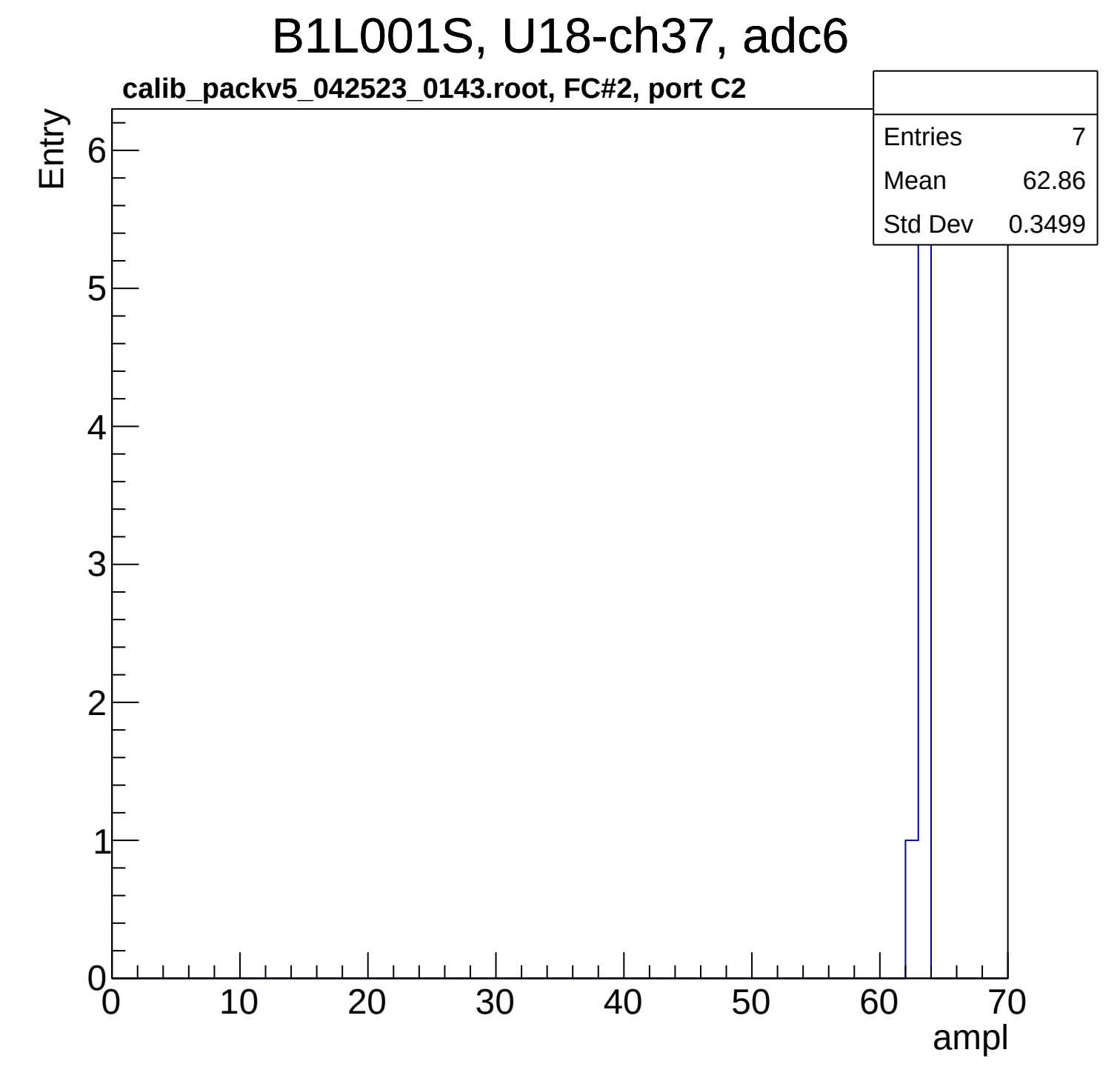

B1L001S, U18-ch37, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 111
Mean 38.5
Std Dev 3.347
Gaus mean : 39.1817
Gaus Width: 3.1162
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

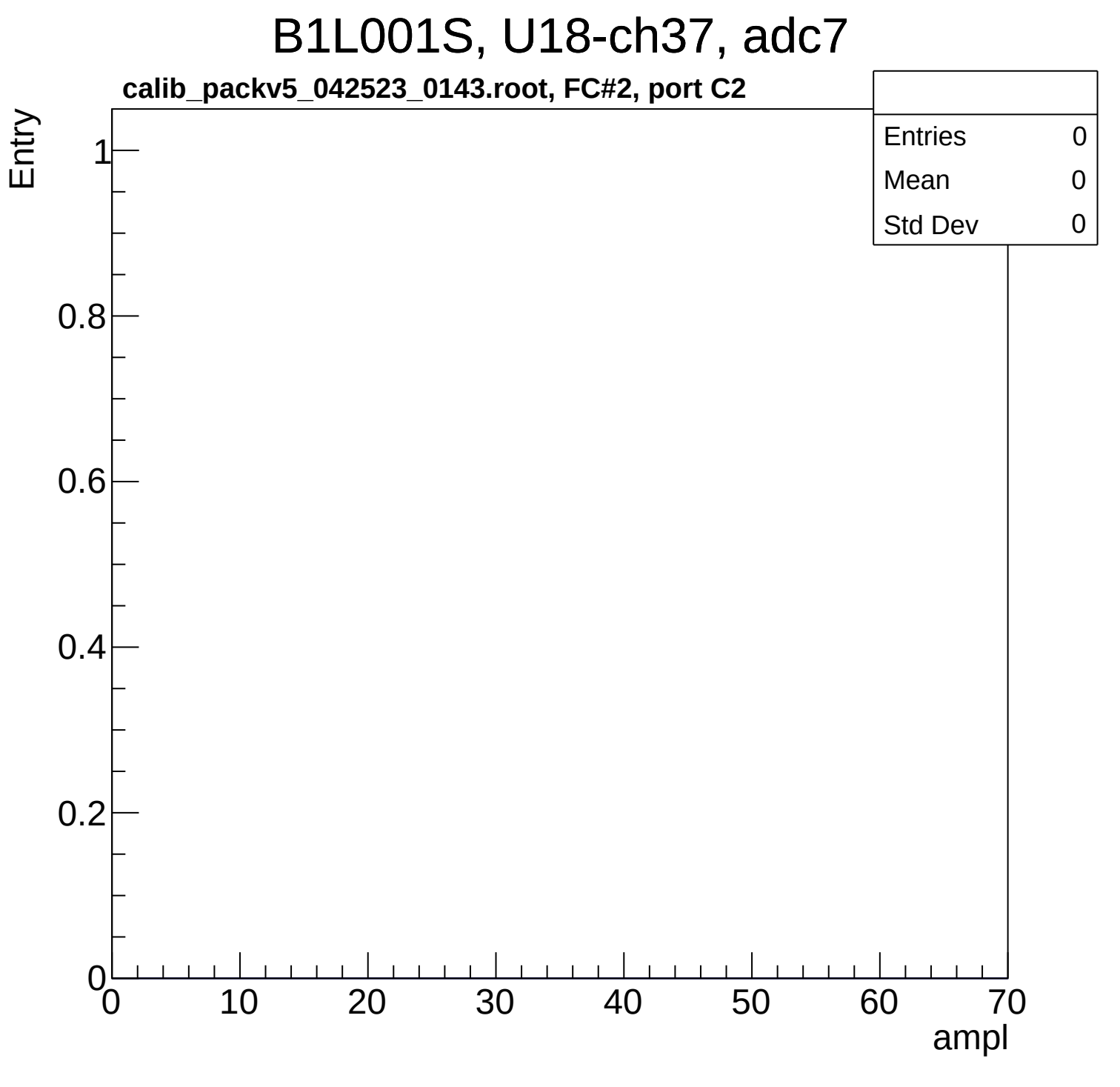

B1L001S, U18-ch37, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 137
Mean 44.25
Std Dev 3.324
Gaus mean : 44.7074
Gaus Width: 3.5521
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

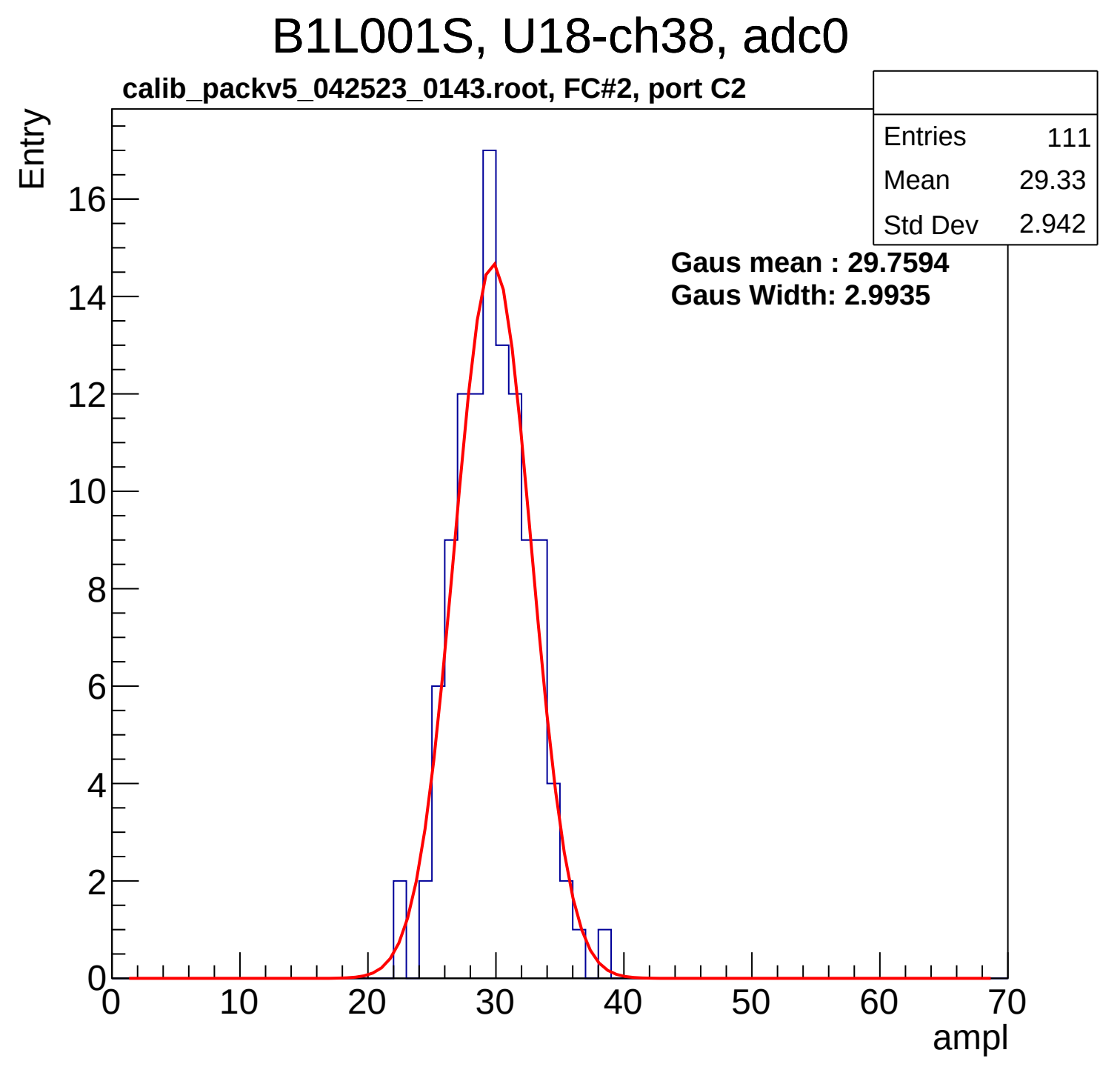

B1L001S, U18-ch37, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 122
Mean 51.2
Std Dev 3.238
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl

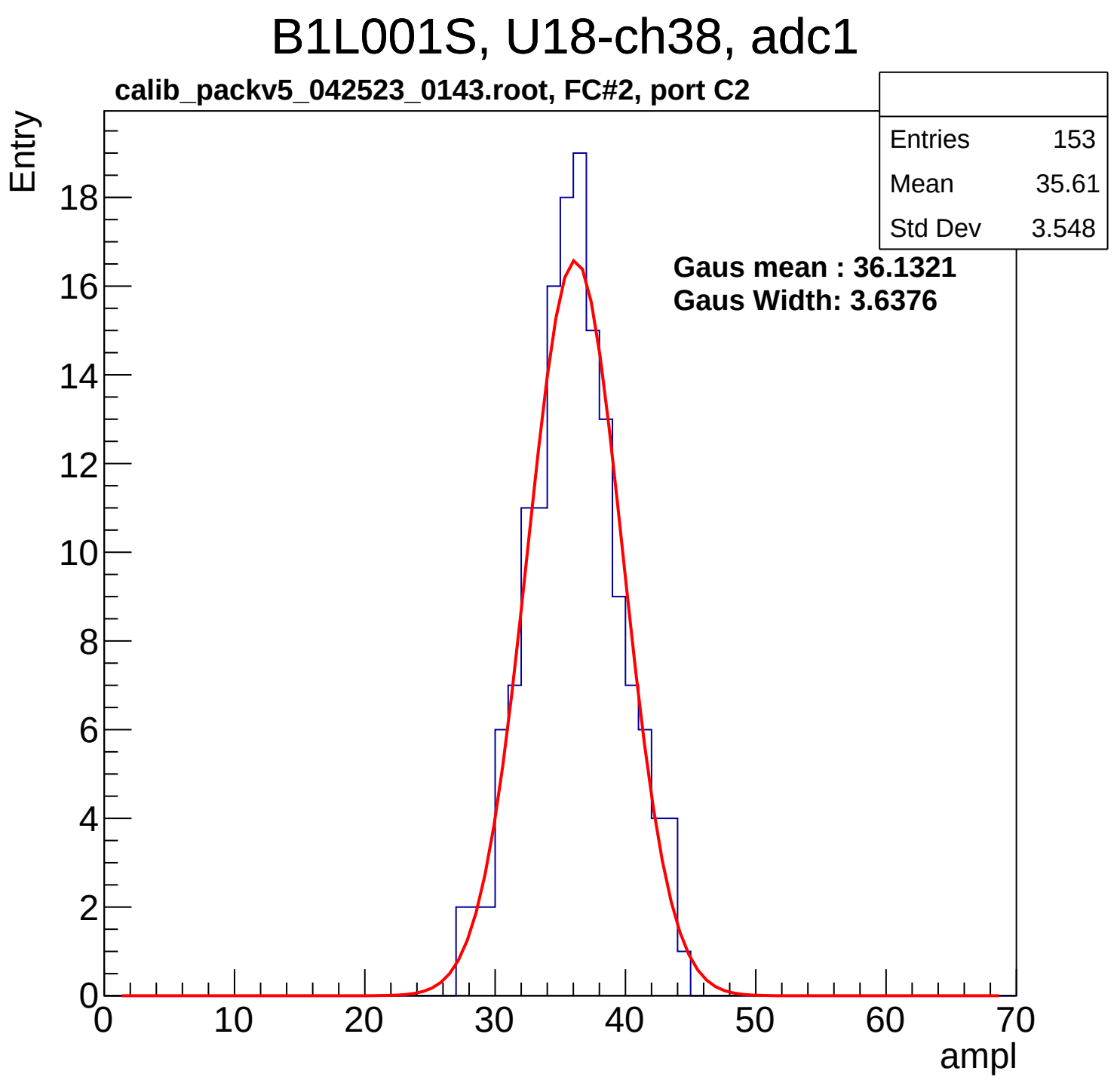

B1L001S, U18-ch37, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 104
Mean 56.03
Std Dev 3.001
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

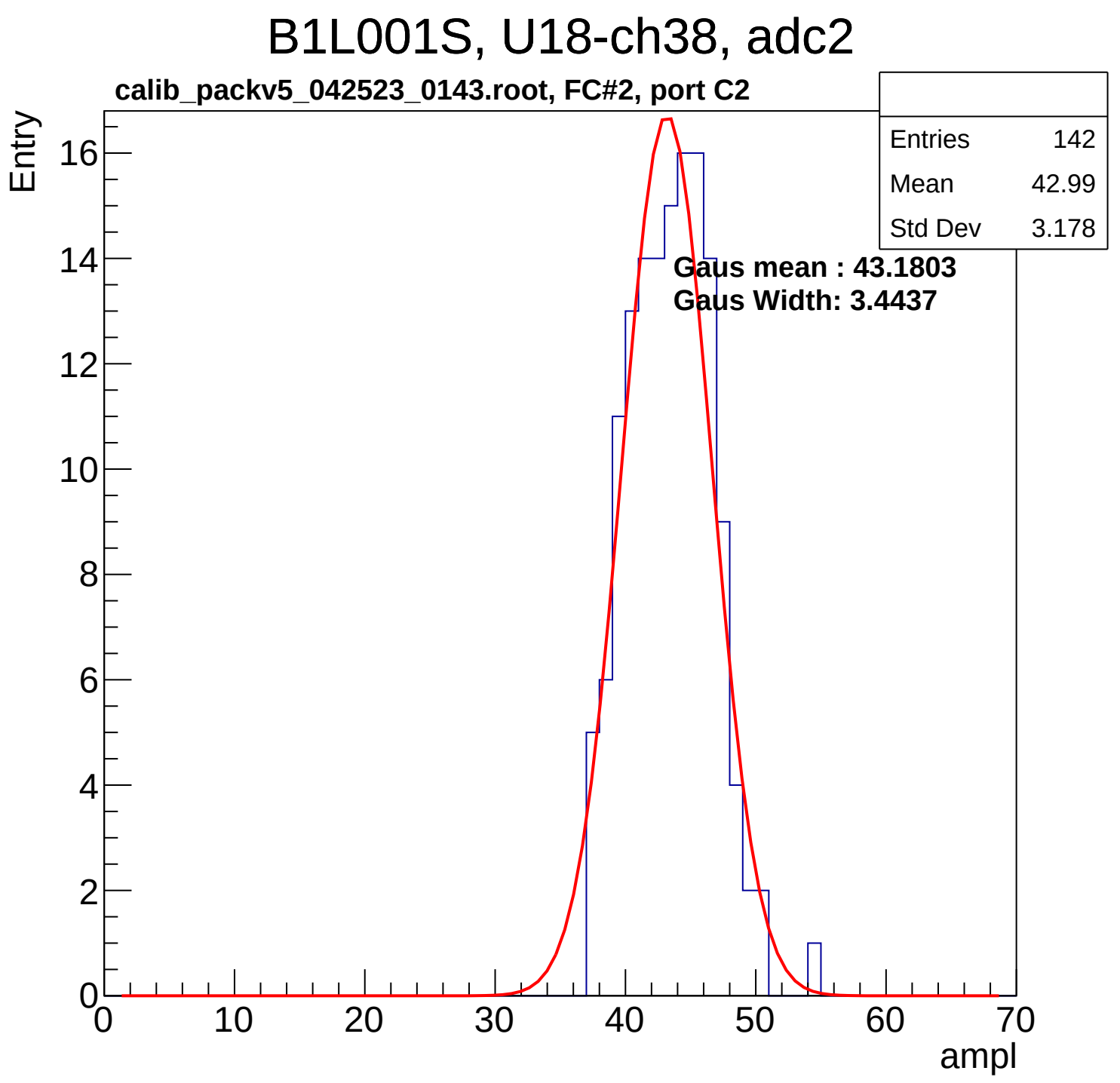

B1L001S, U18-ch37, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 82
Mean 59.16
Std Dev 9.543
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

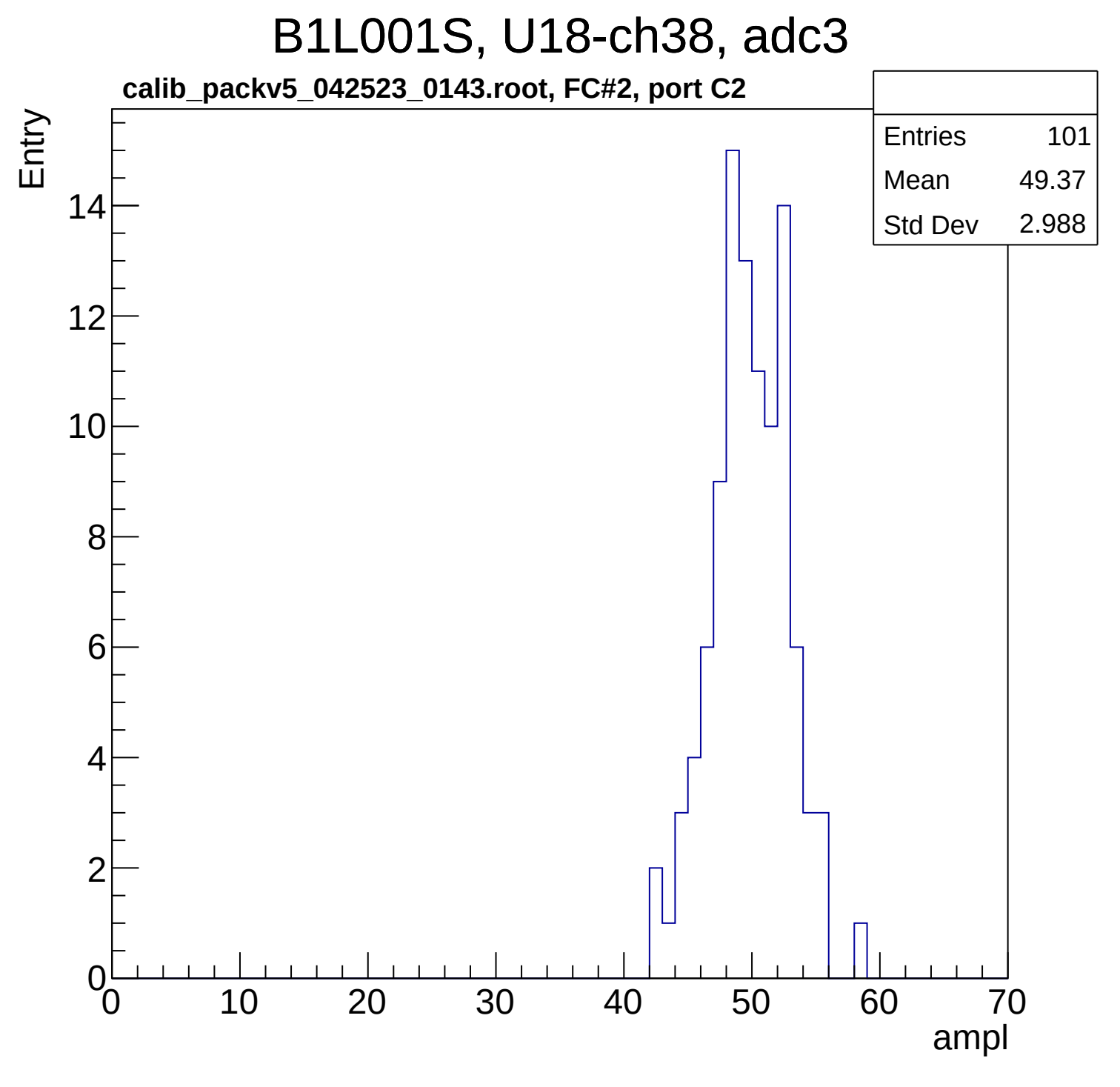

B1L001S, U18-ch37, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 7
Mean 62.86
Std Dev 0.3499
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl

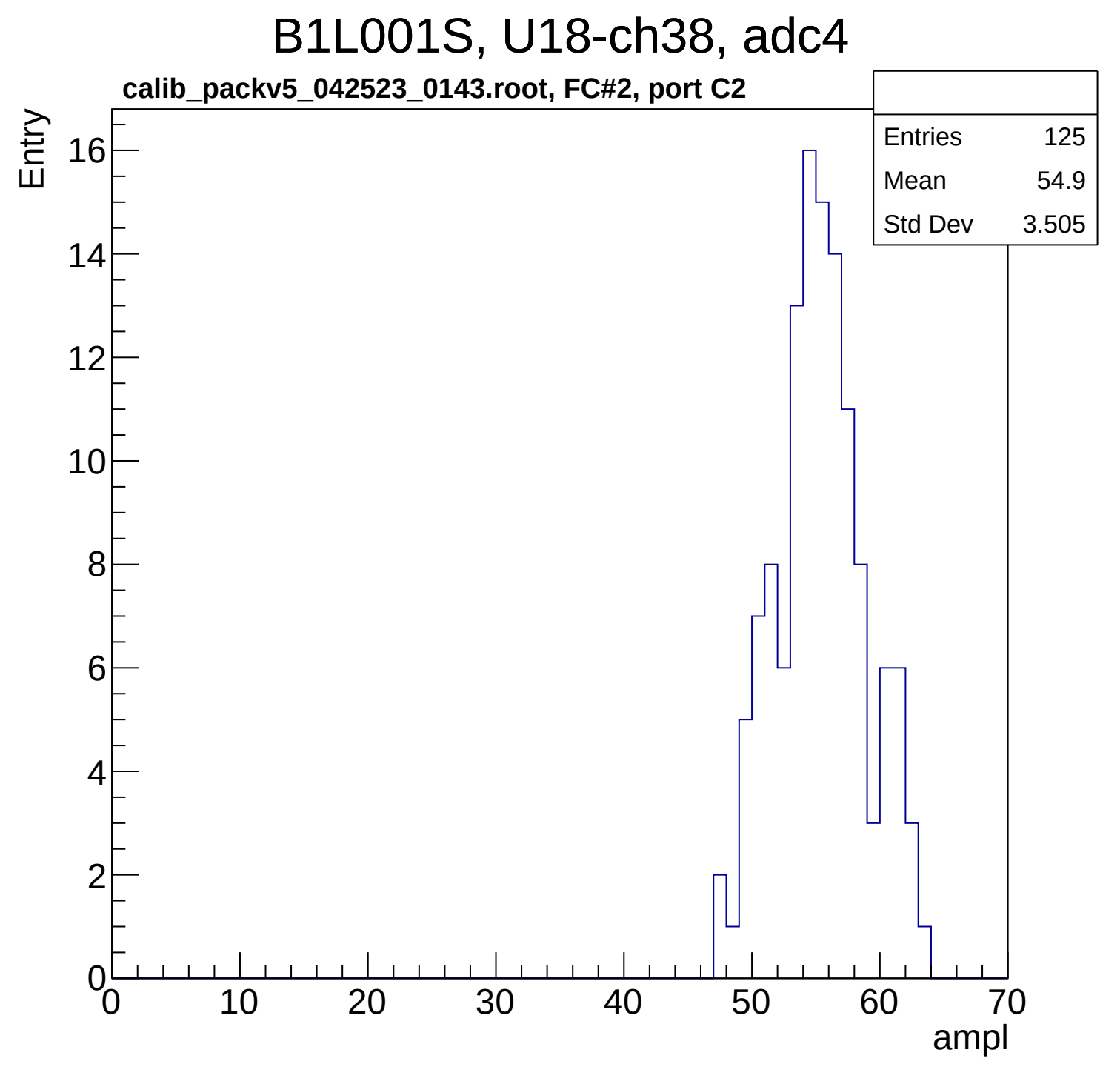

B1L001S, U18-ch37, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

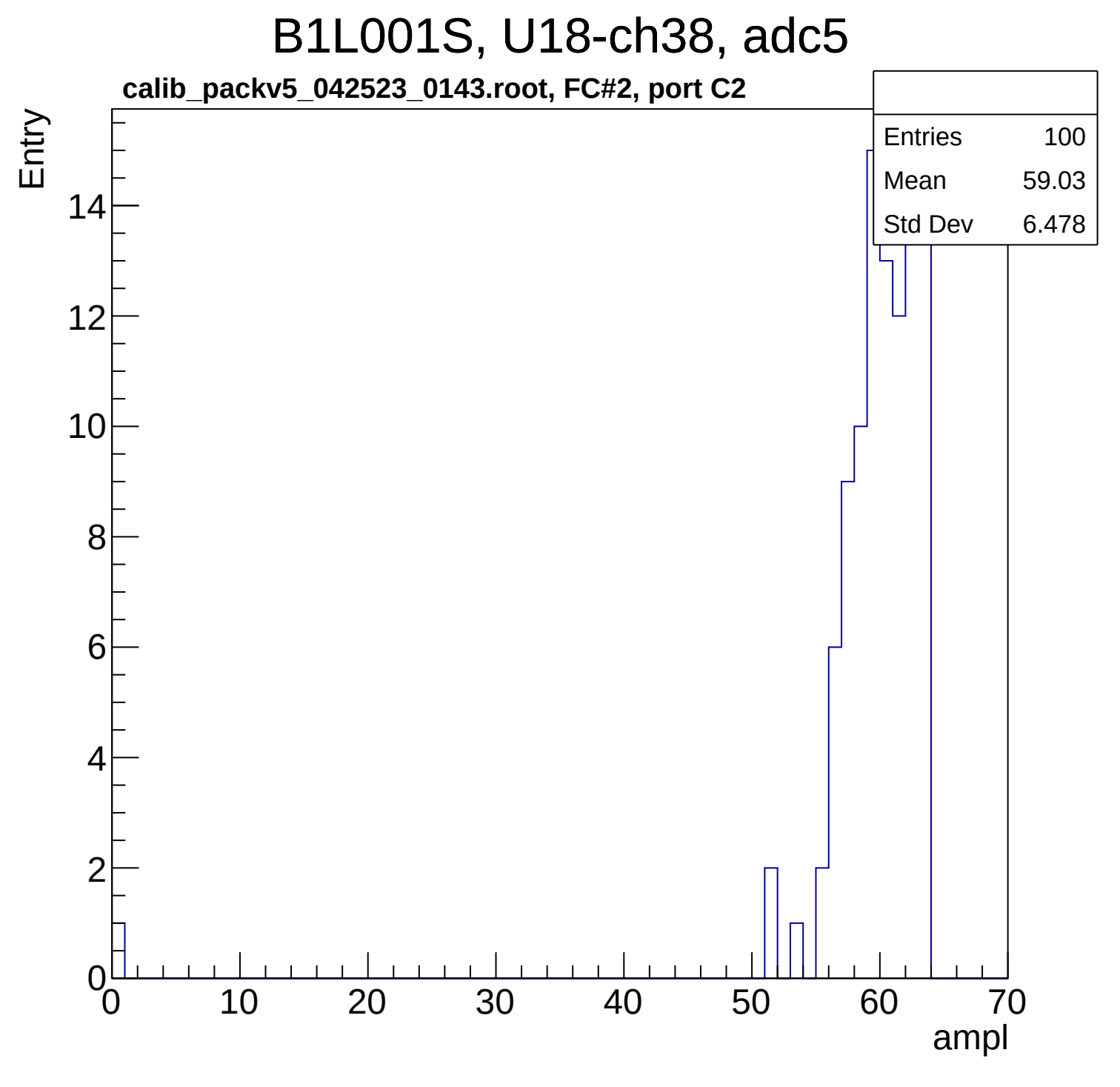

B1L001S, U18-ch38, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 111
Mean 29.33
Std Dev 2.942
Gaus mean : 29.7594
Gaus Width: 2.9935
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

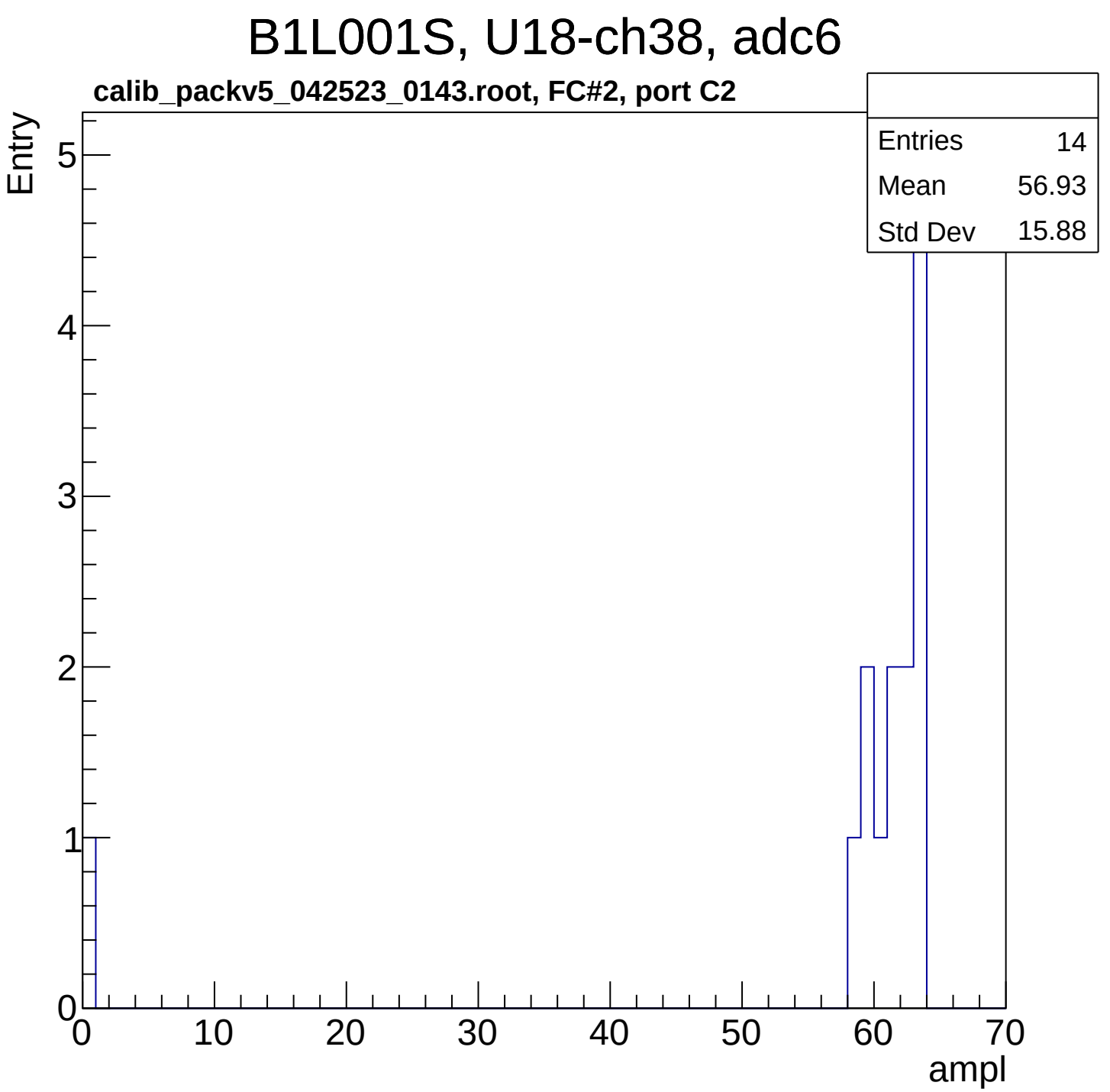

B1L001S, U18-ch38, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 153
Mean 35.61
Std Dev 3.548
Gaus mean : 36.1321
Gaus Width: 3.6376
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

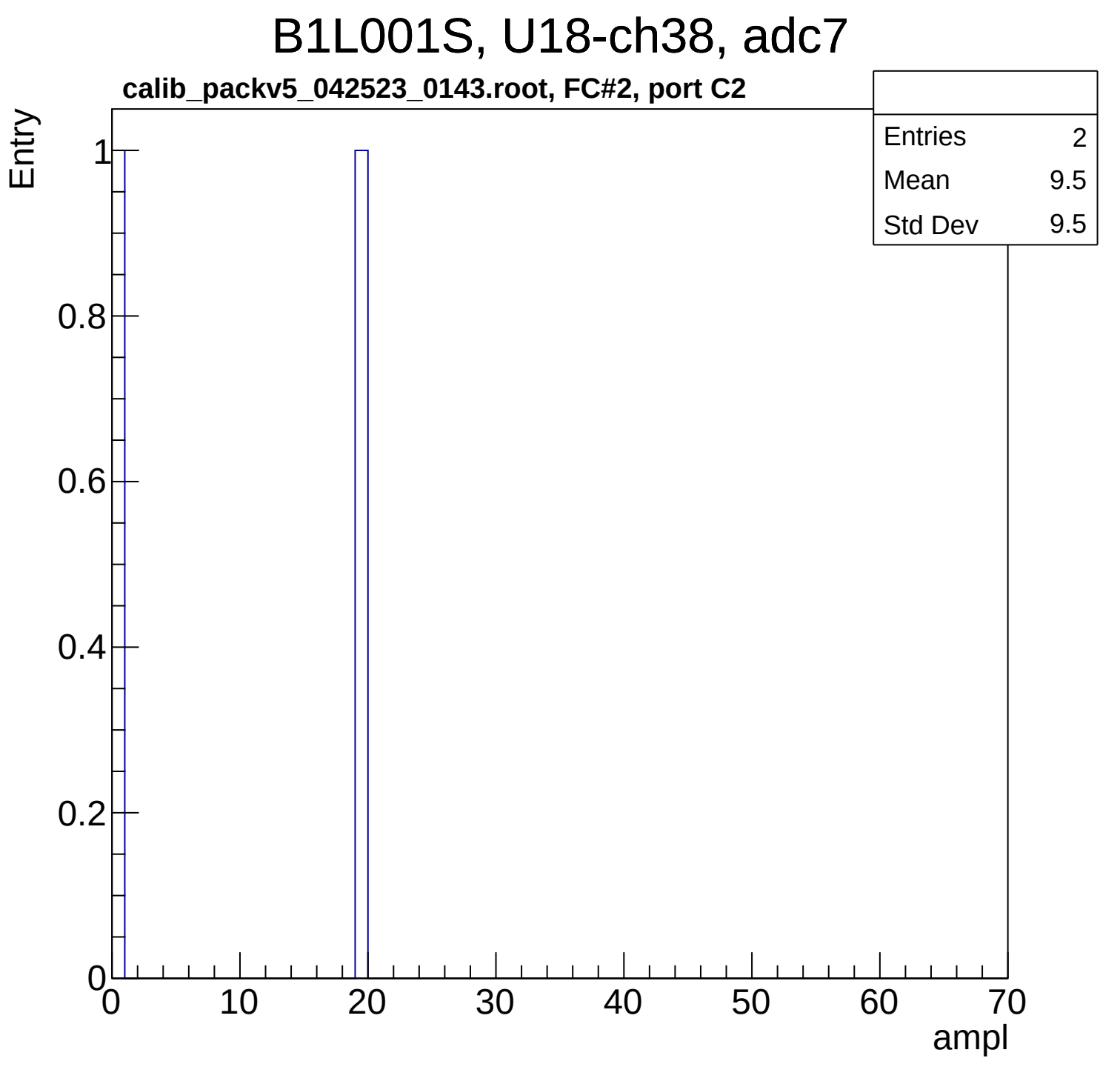

B1L001S, U18-ch38, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 142
Mean 42.99
Std Dev 3.178
Gaus mean : 43.1803
Gaus Width: 3.4437
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

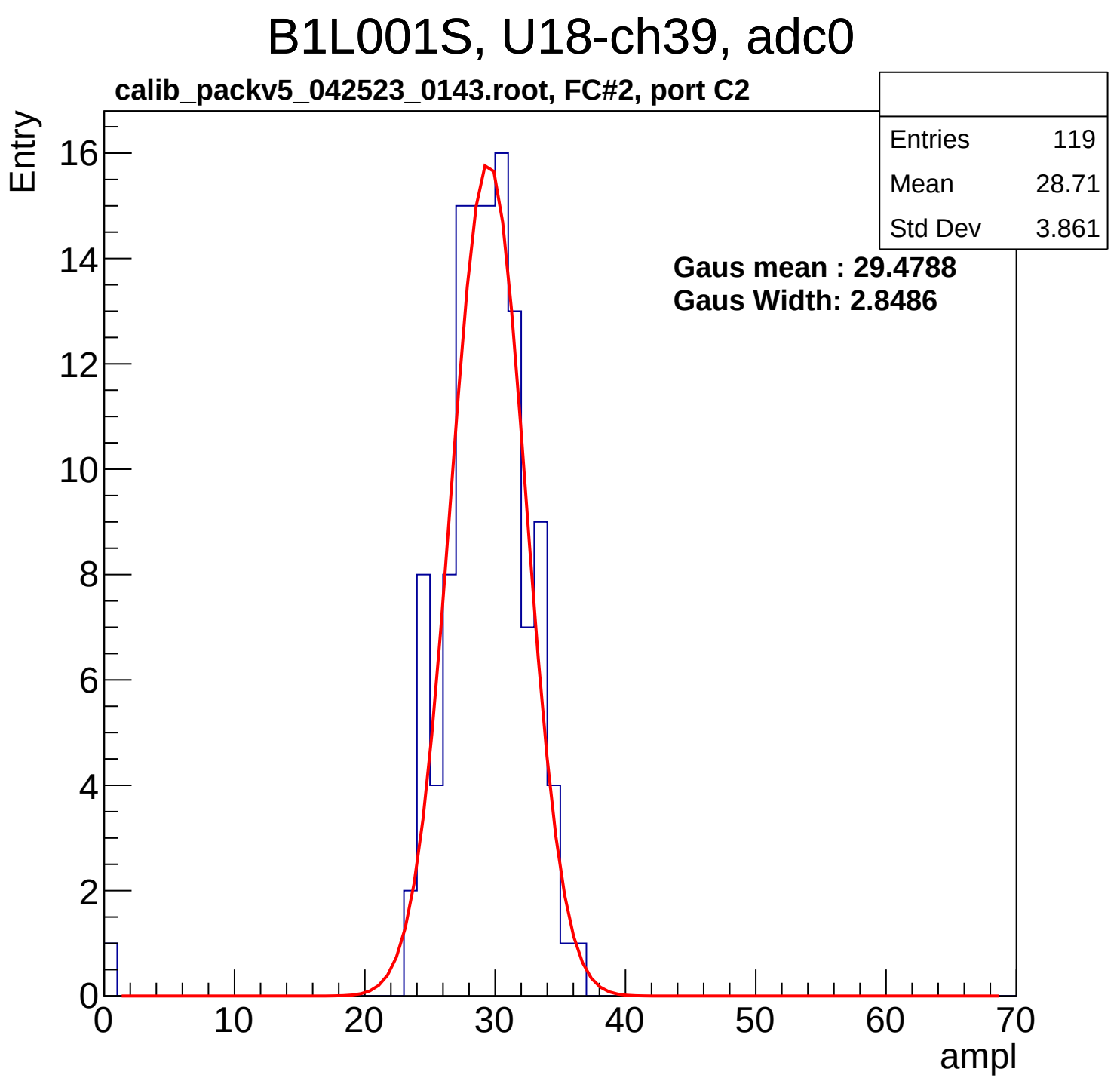

B1L001S, U18-ch38, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 101
Mean 49.37
Std Dev 2.988
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl

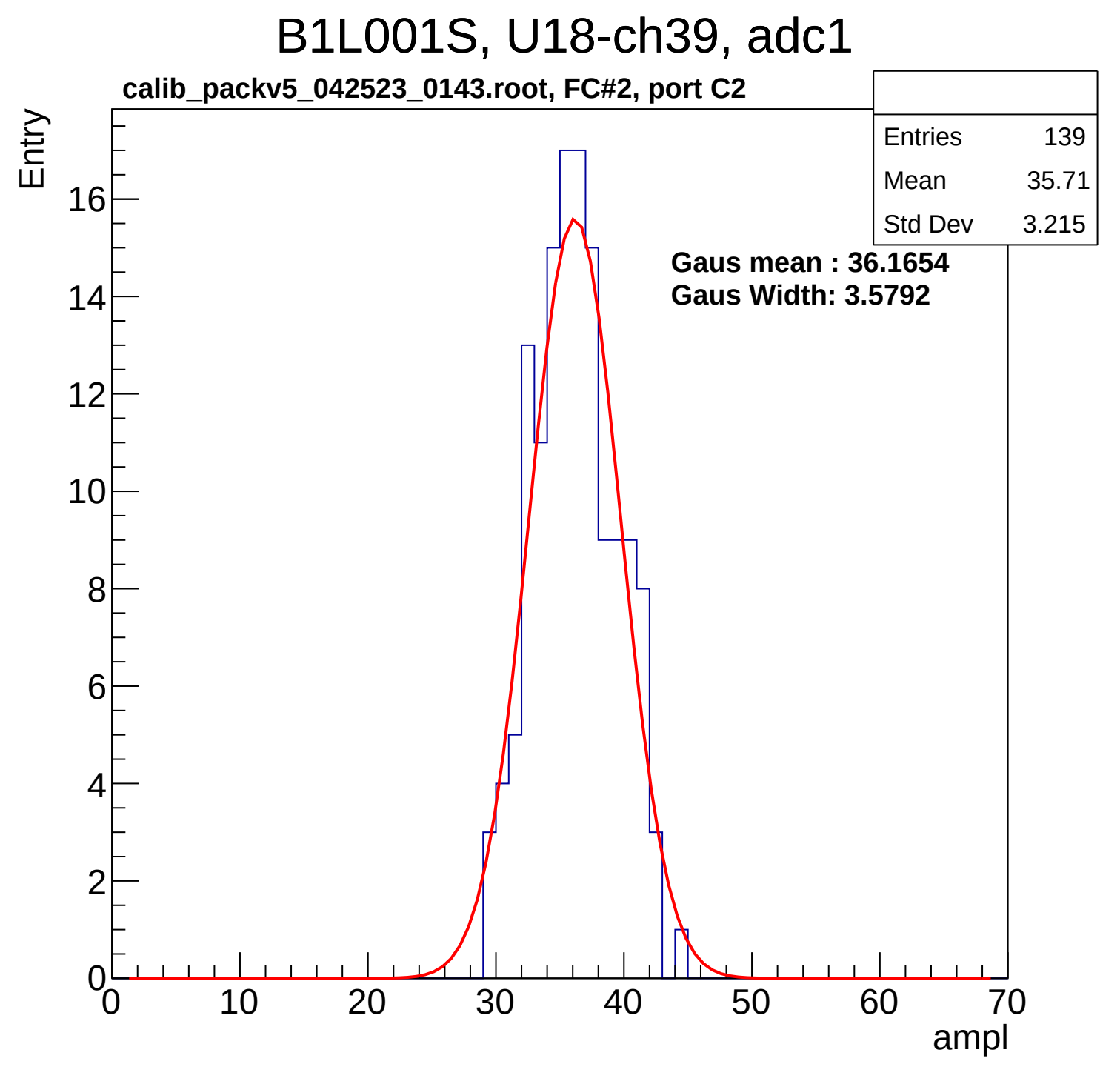

B1L001S, U18-ch38, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 125
Mean 54.9
Std Dev 3.505
Entry
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl

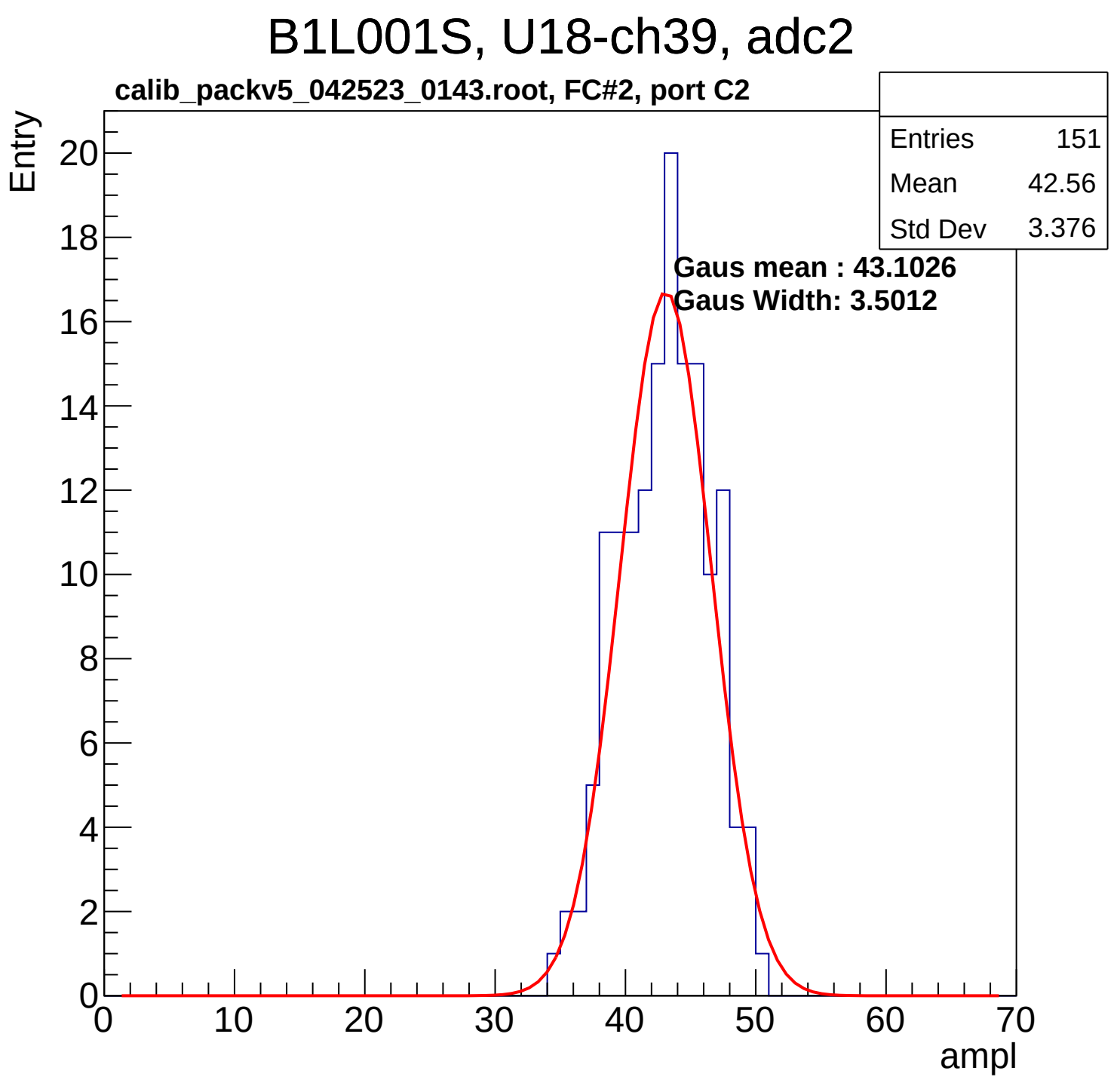

B1L001S, U18-ch38, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 100
Mean 59.03
Std Dev 6.478
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

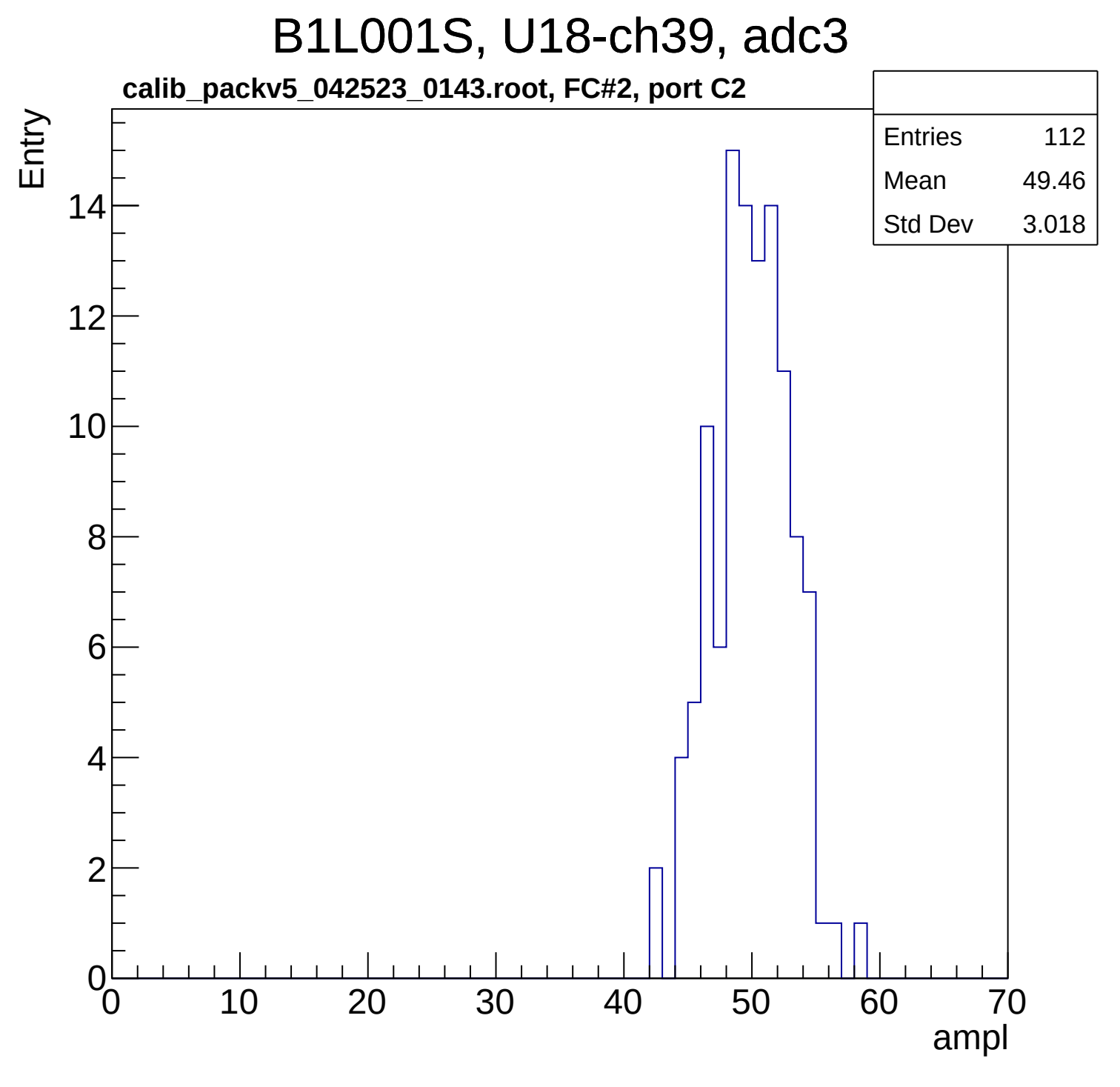

B1L001S, U18-ch38, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 14
Mean 56.93
Std Dev 15.88
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

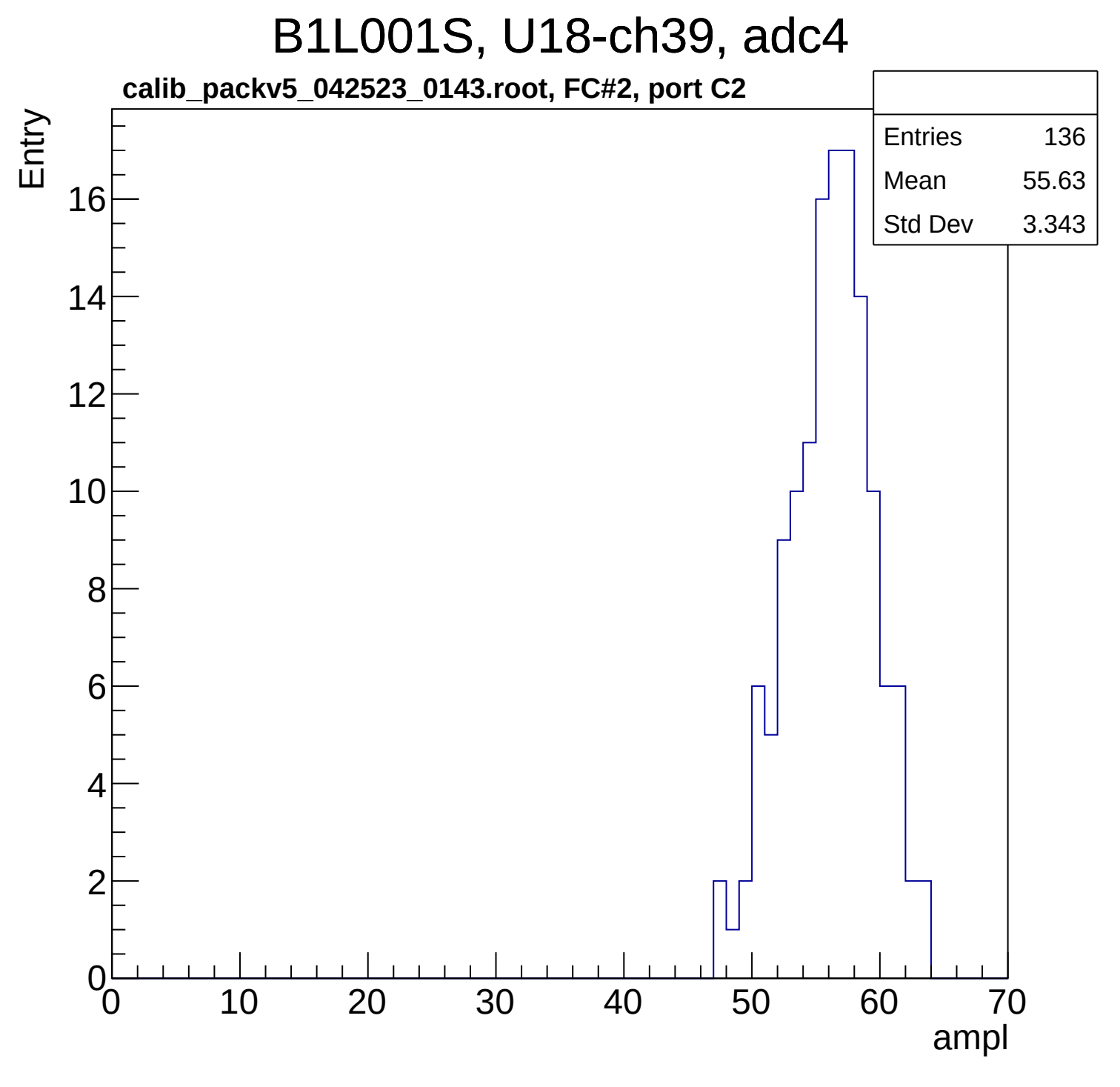

B1L001S, U18-ch38, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 9.5
Std Dev 9.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

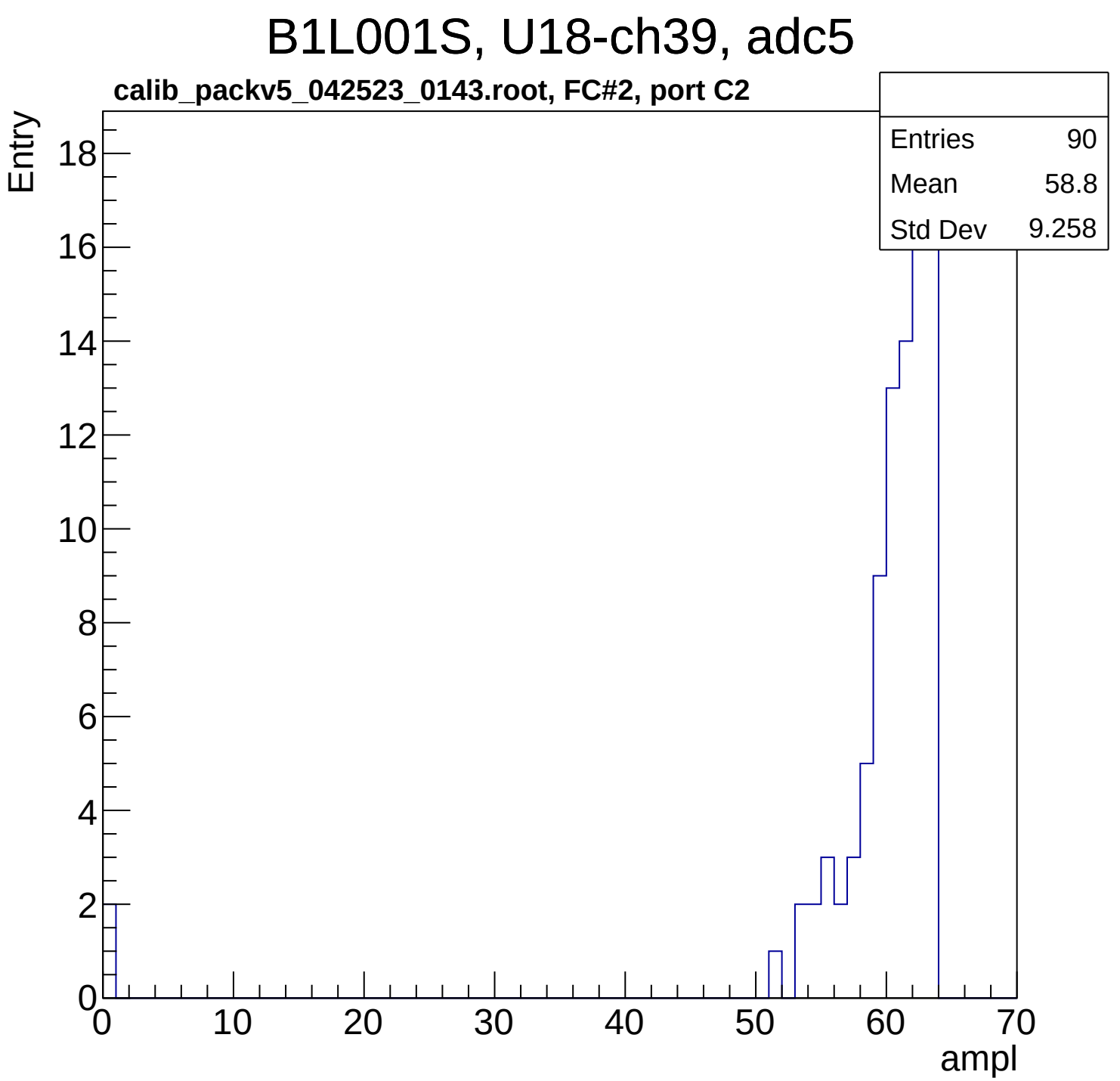

B1L001S, U18-ch39, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 119
Mean 28.71
Std Dev 3.861
Gaus mean : 29.4788
Gaus Width: 2.8486
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

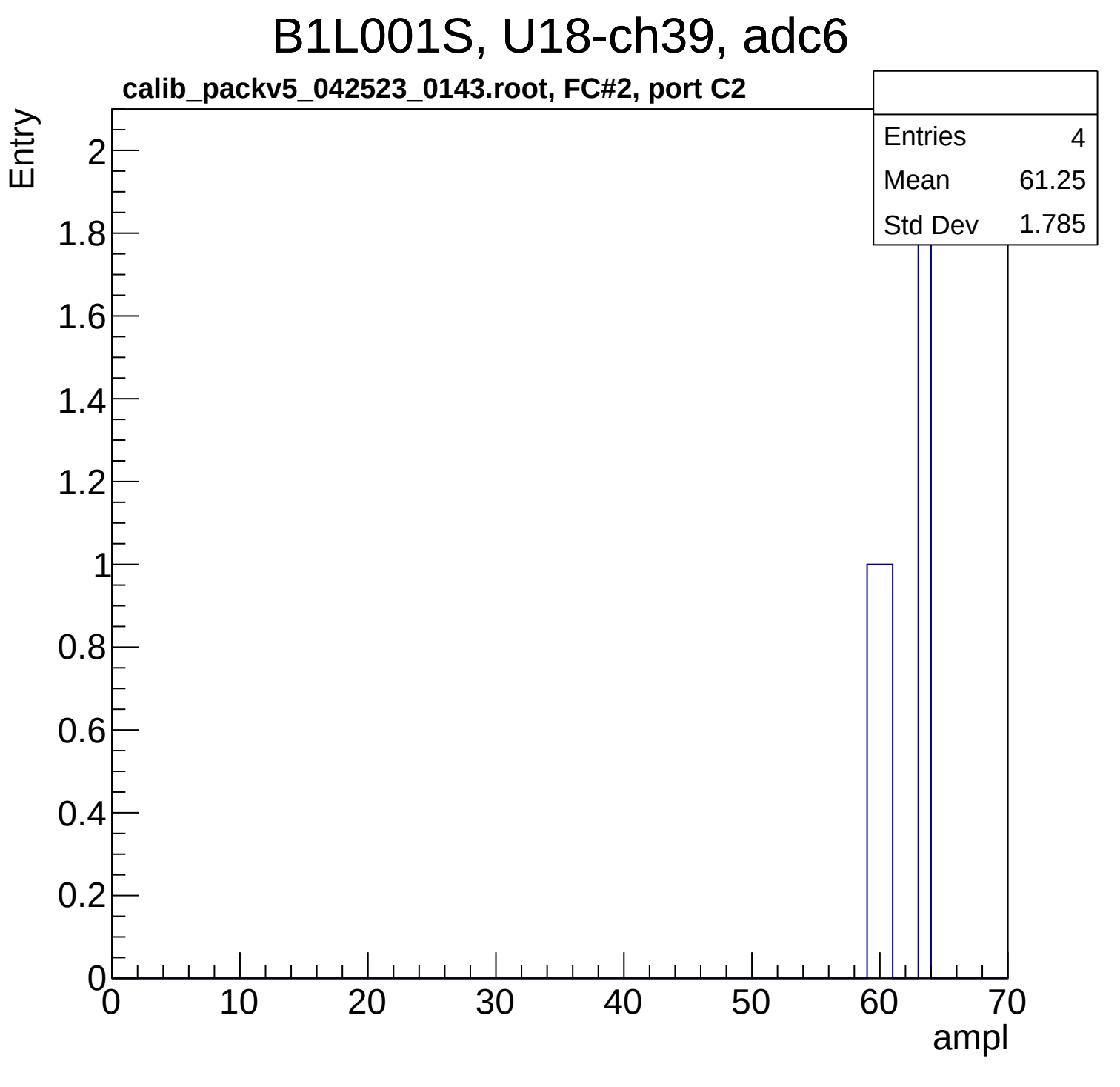

B1L001S, U18-ch39, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 139
Mean 35.71
Std Dev 3.215
Gaus mean : 36.1654
Gaus Width: 3.5792
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

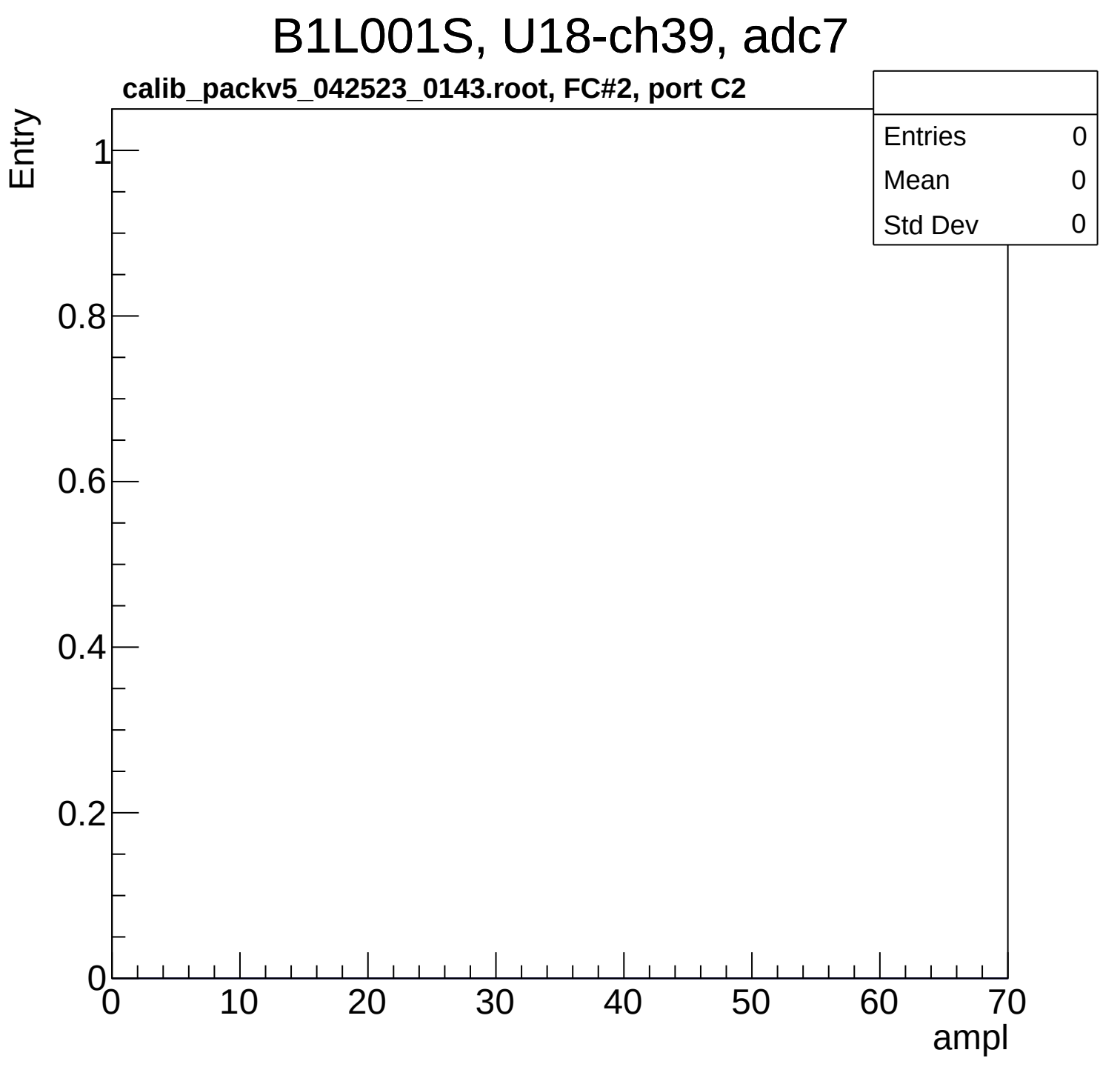

B1L001S, U18-ch39, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 151
Mean 42.56
Std Dev 3.376
Gaus mean : 43.1026
Gaus Width: 3.5012
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

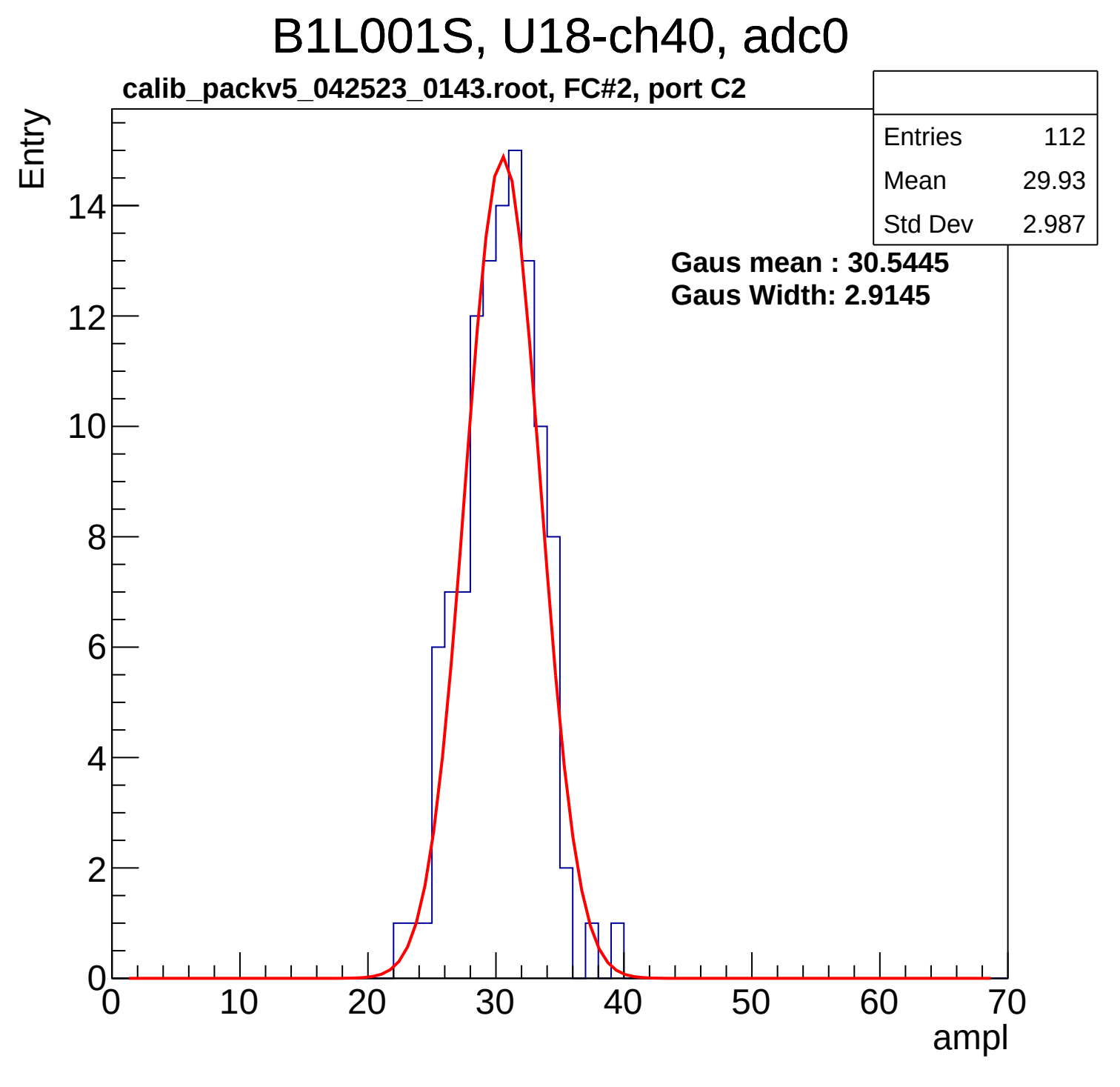

B1L001S, U18-ch39, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 112
Mean 49.46
Std Dev 3.018
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl

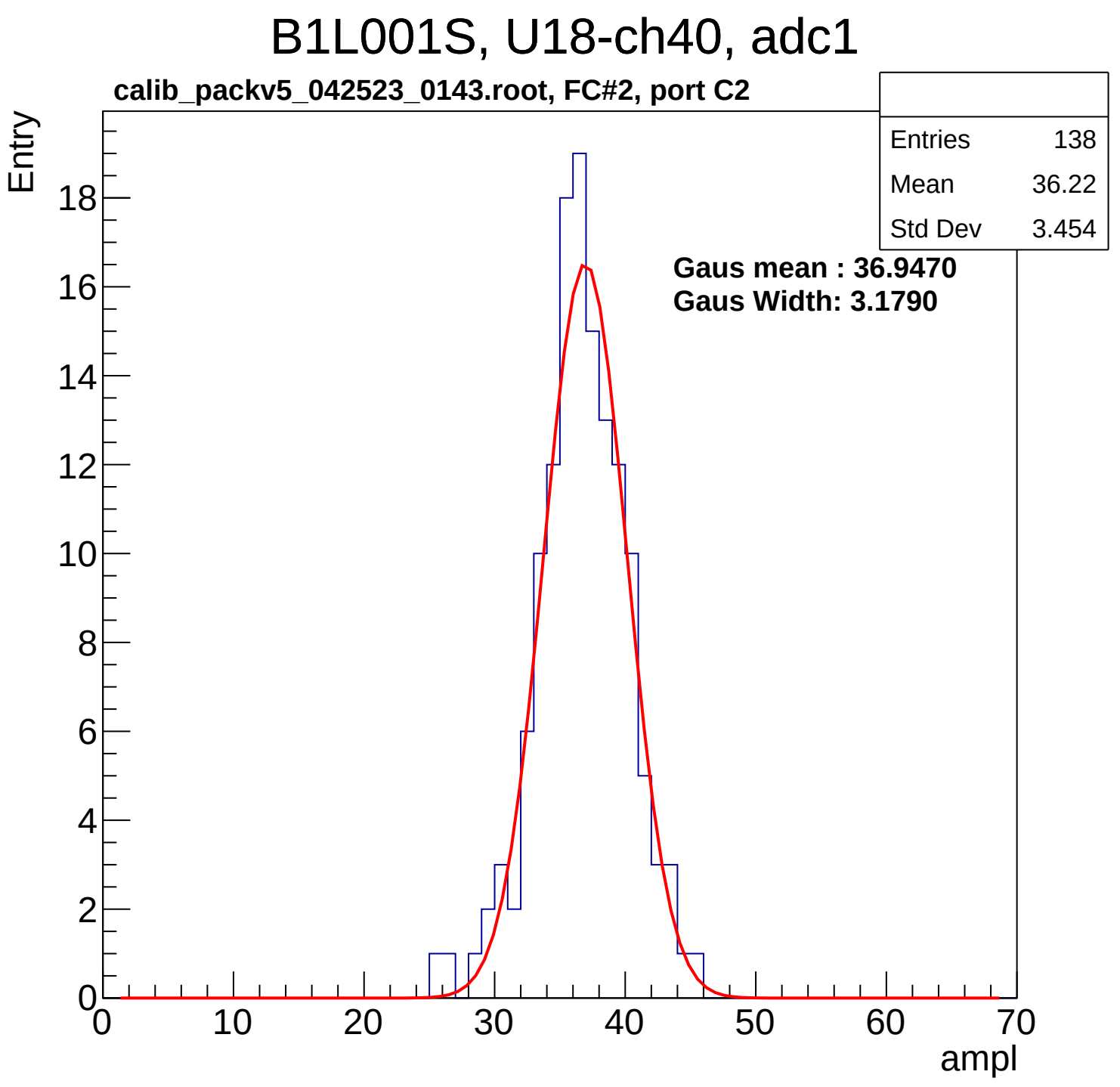

B1L001S, U18-ch39, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 136
Mean 55.63
Std Dev 3.343
Entry
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl

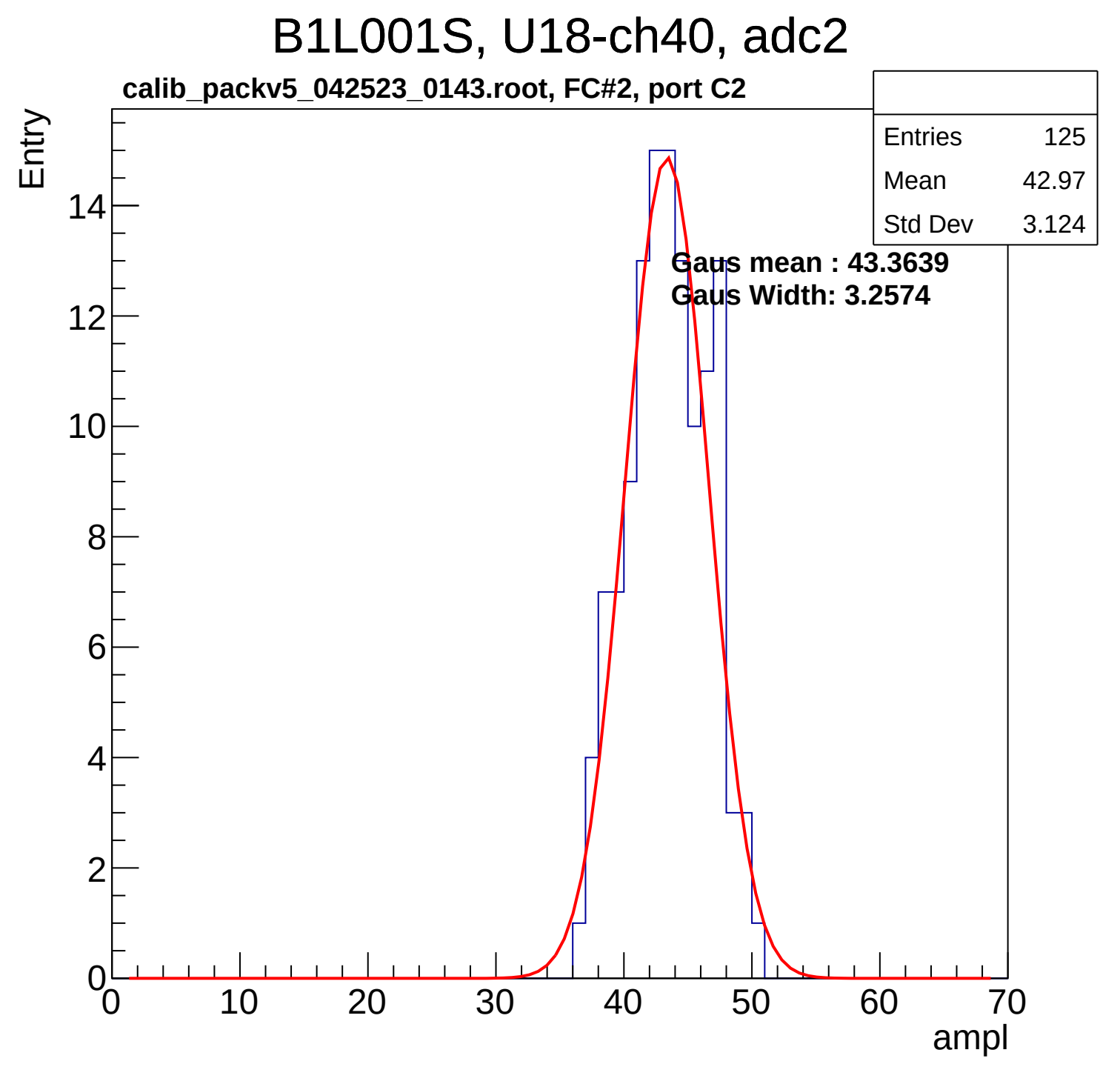

B1L001S, U18-ch39, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 90
Mean 58.8
Std Dev 9.258
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

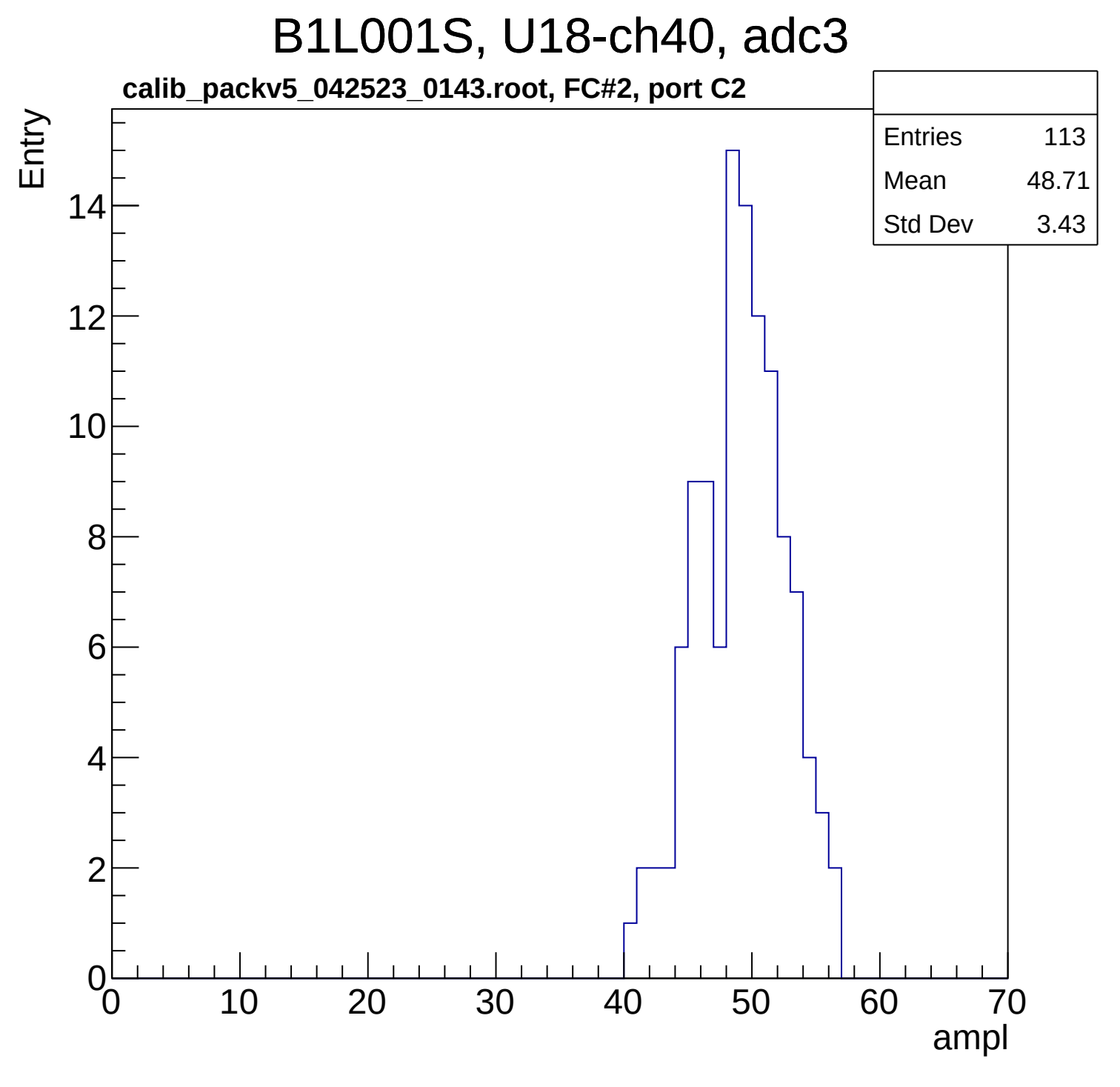

B1L001S, U18-ch39, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 4
Mean 61.25
Std Dev 1.785
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

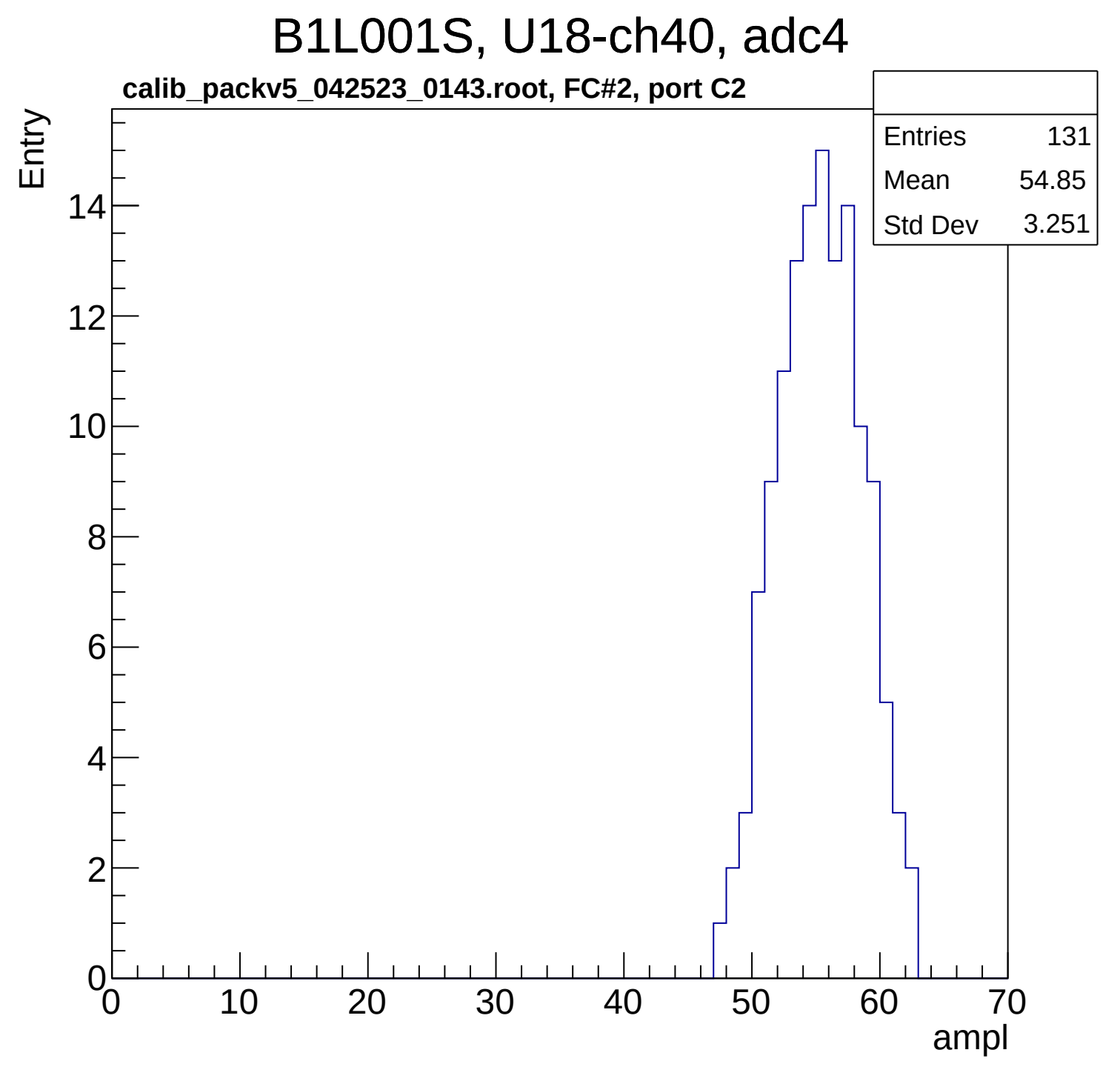

B1L001S, U18-ch39, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

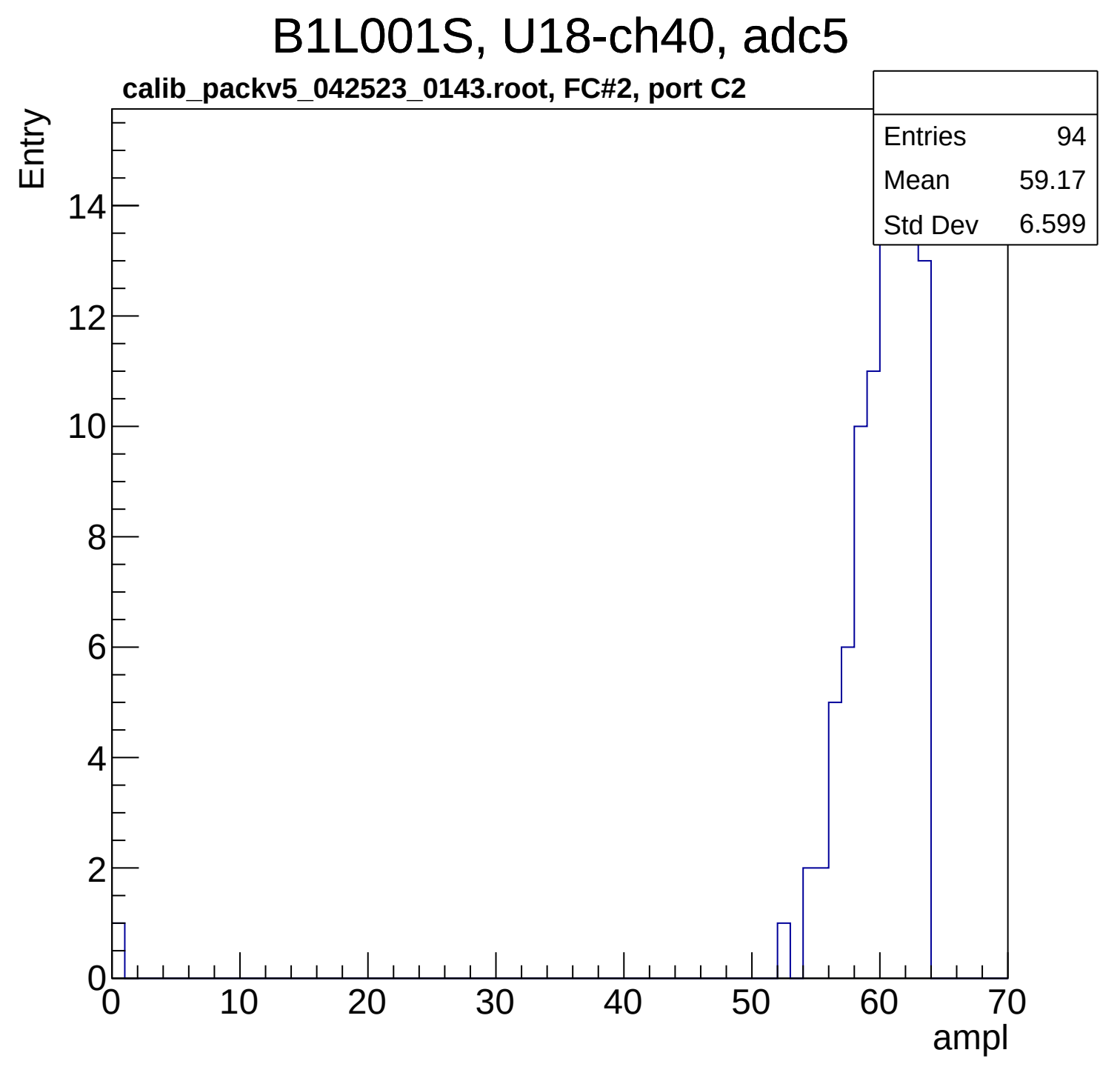

B1L001S, U18-ch40, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 112
Mean 29.93
Std Dev 2.987
Gaus mean : 30.5445
Gaus Width: 2.9145
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

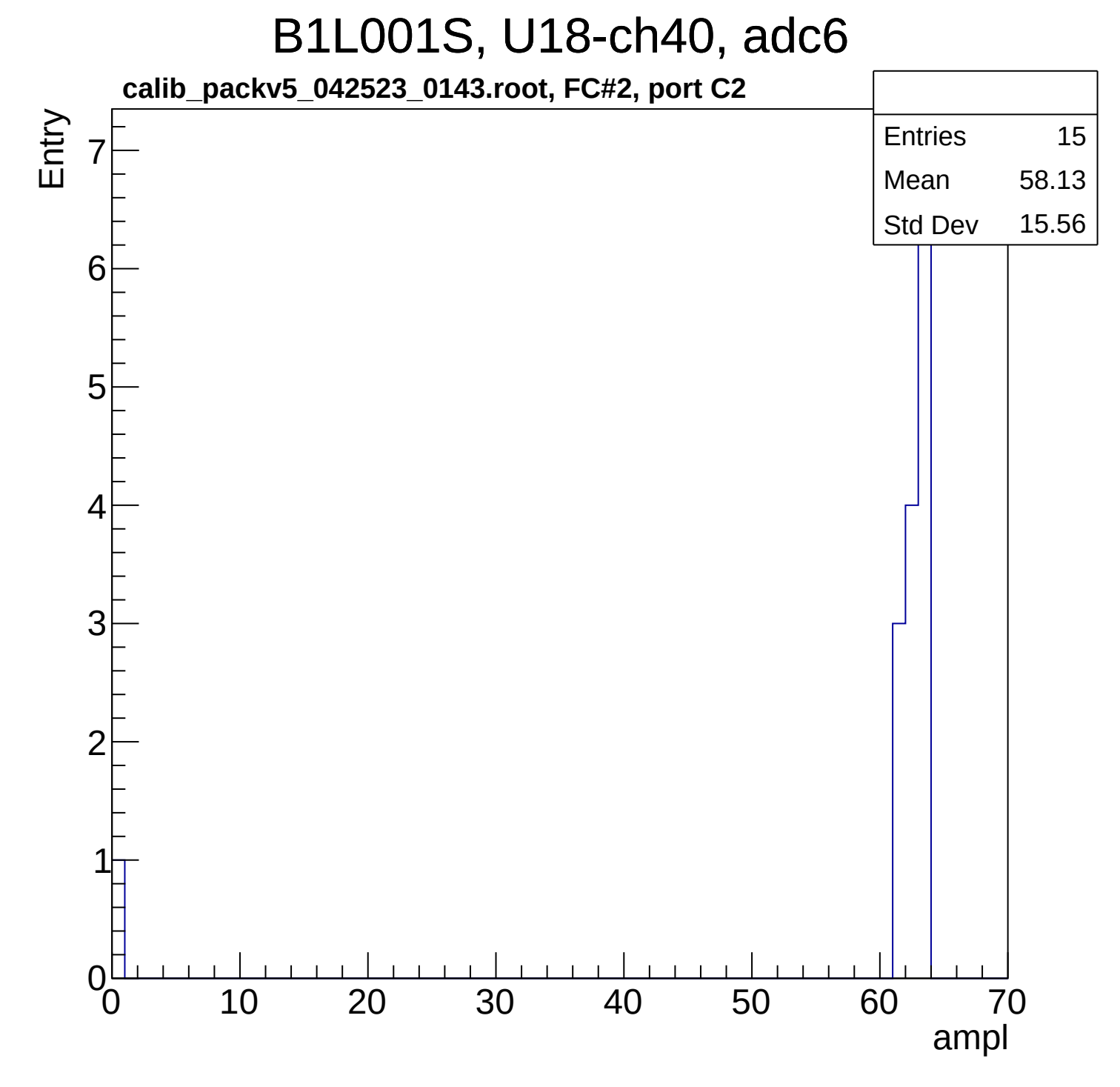

B1L001S, U18-ch40, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 138
Mean 36.22
Std Dev 3.454
Gaus mean : 36.9470
Gaus Width: 3.1790
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

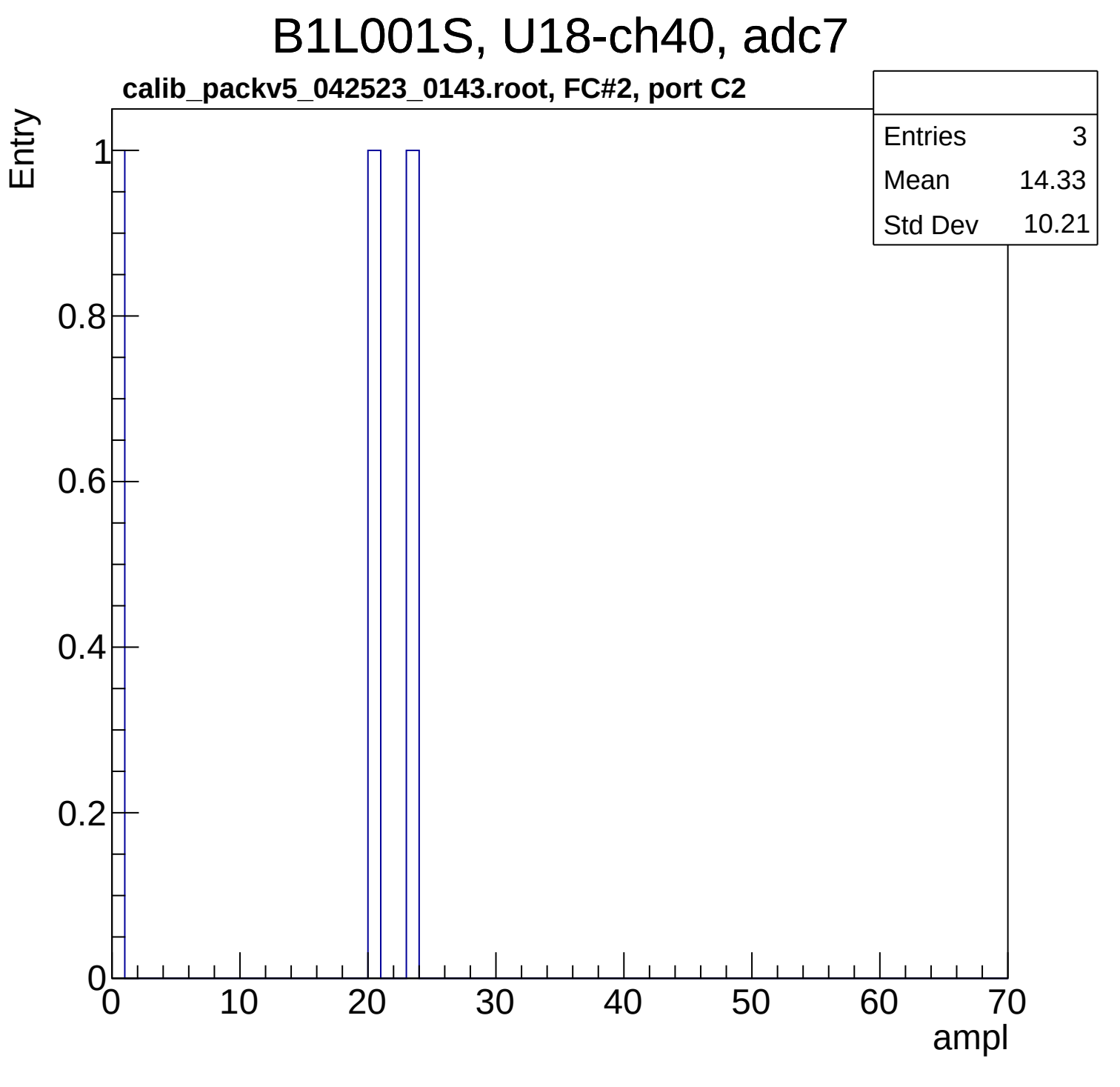

B1L001S, U18-ch40, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 125
Mean 42.97
Std Dev 3.124
Gaus mean : 43.3639
Gaus Width: 3.2574
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

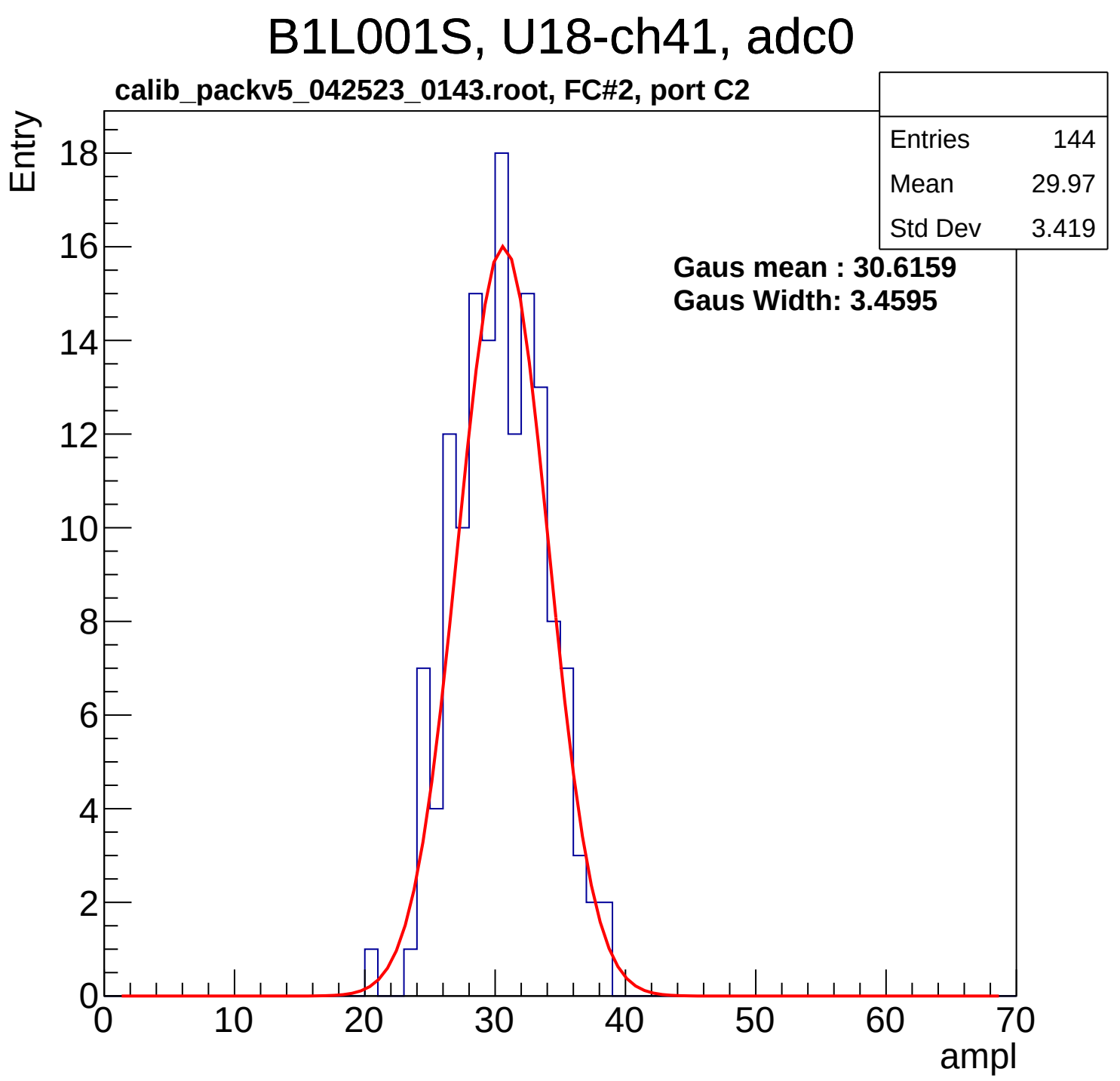

B1L001S, U18-ch40, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 113
Mean 48.71
Std Dev 3.43
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl

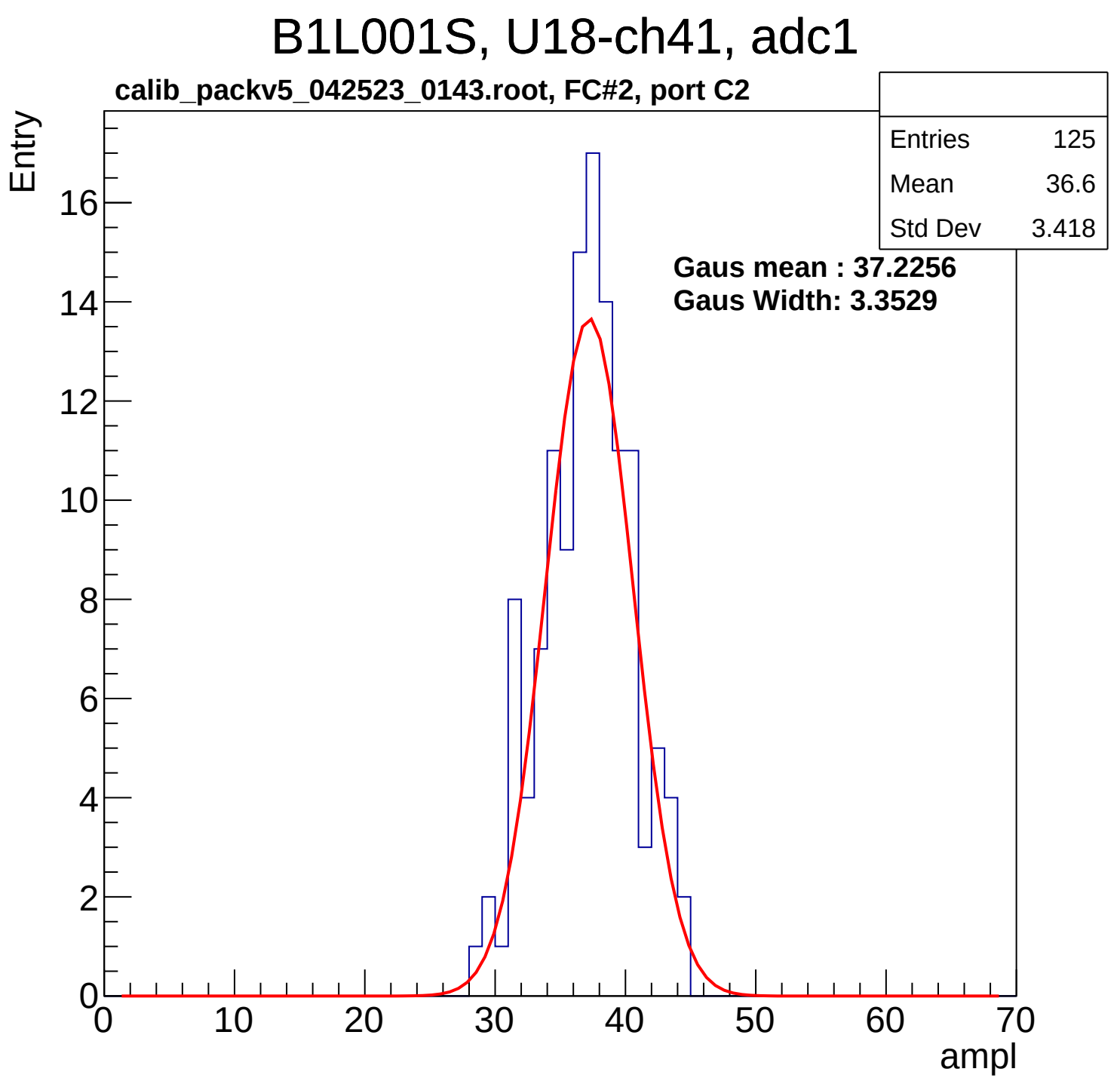

B1L001S, U18-ch40, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 131
Mean 54.85
Std Dev 3.251
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl

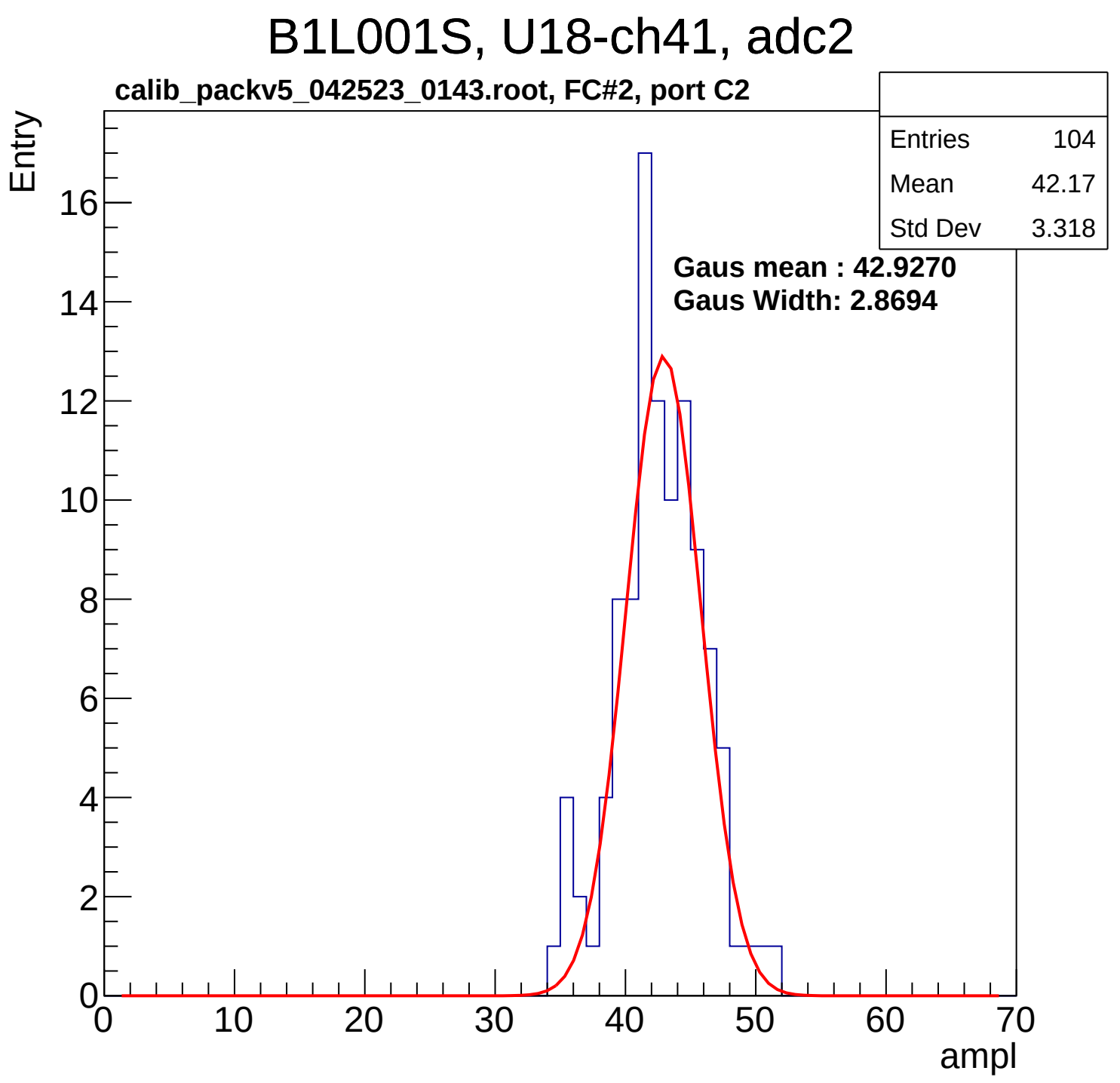

B1L001S, U18-ch40, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 94
Mean 59.17
Std Dev 6.599
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

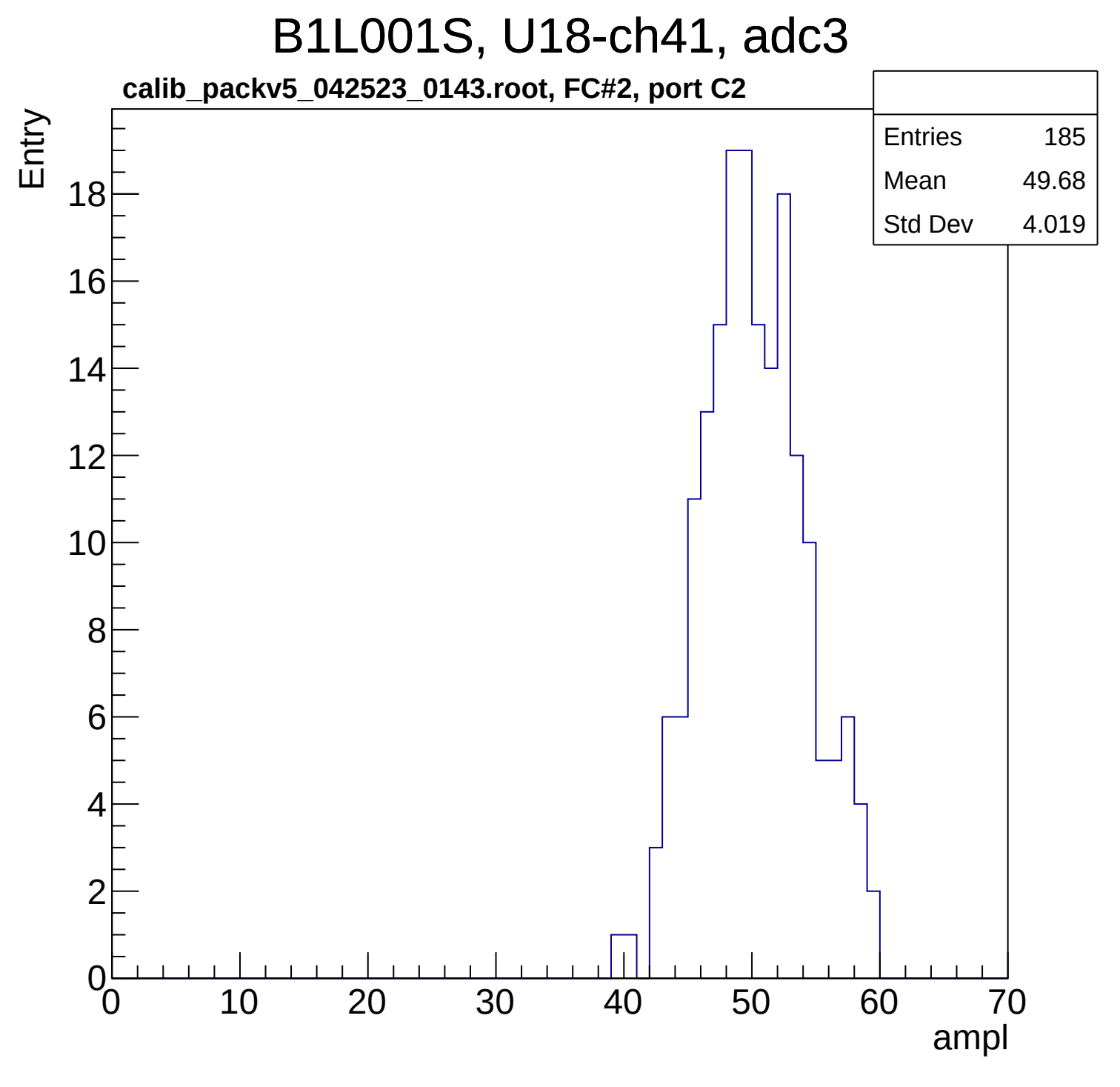

B1L001S, U18-ch40, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 15
Mean 58.13
Std Dev 15.56
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

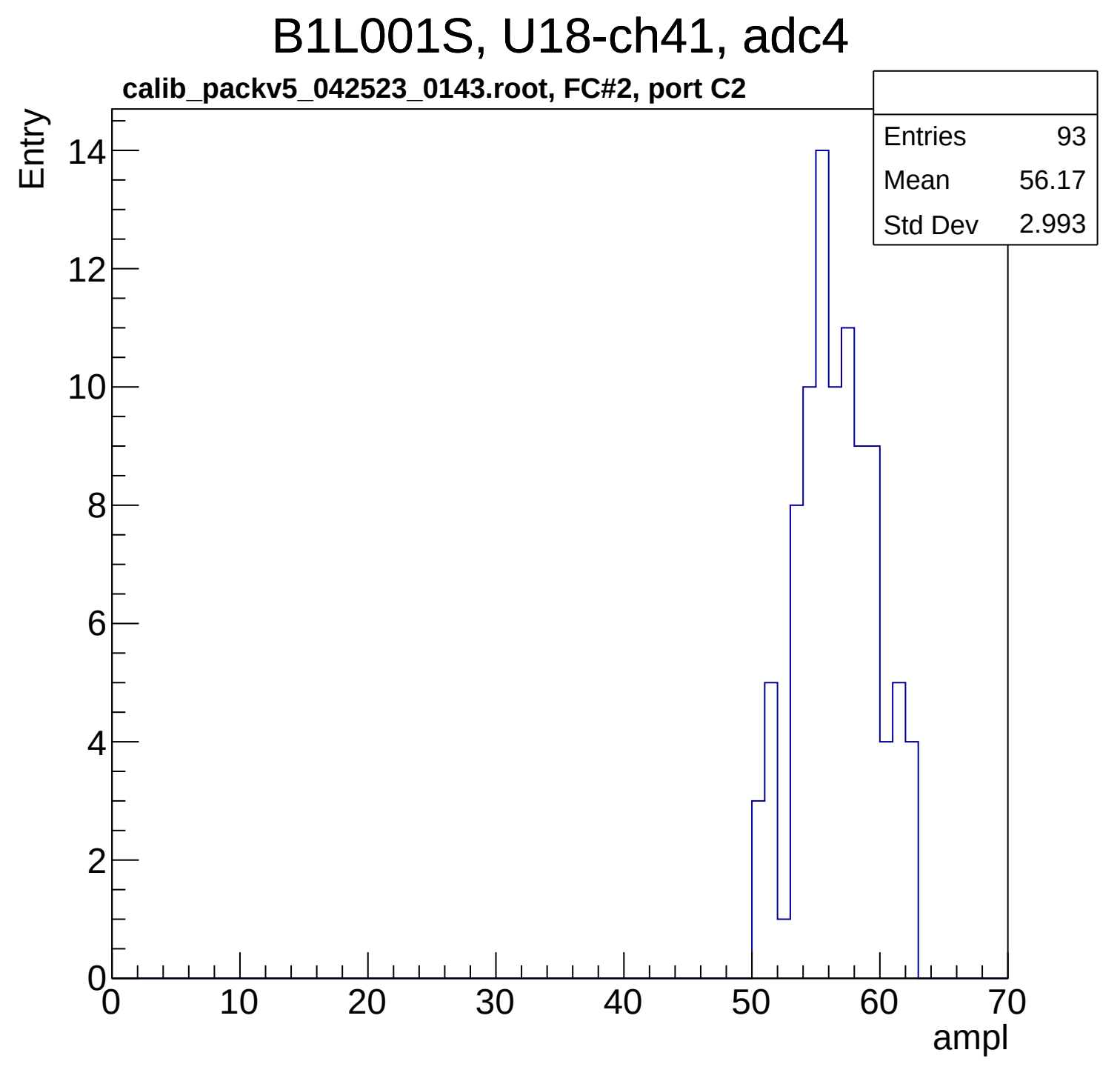

B1L001S, U18-ch40, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 3
Mean 14.33
Std Dev 10.21
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70

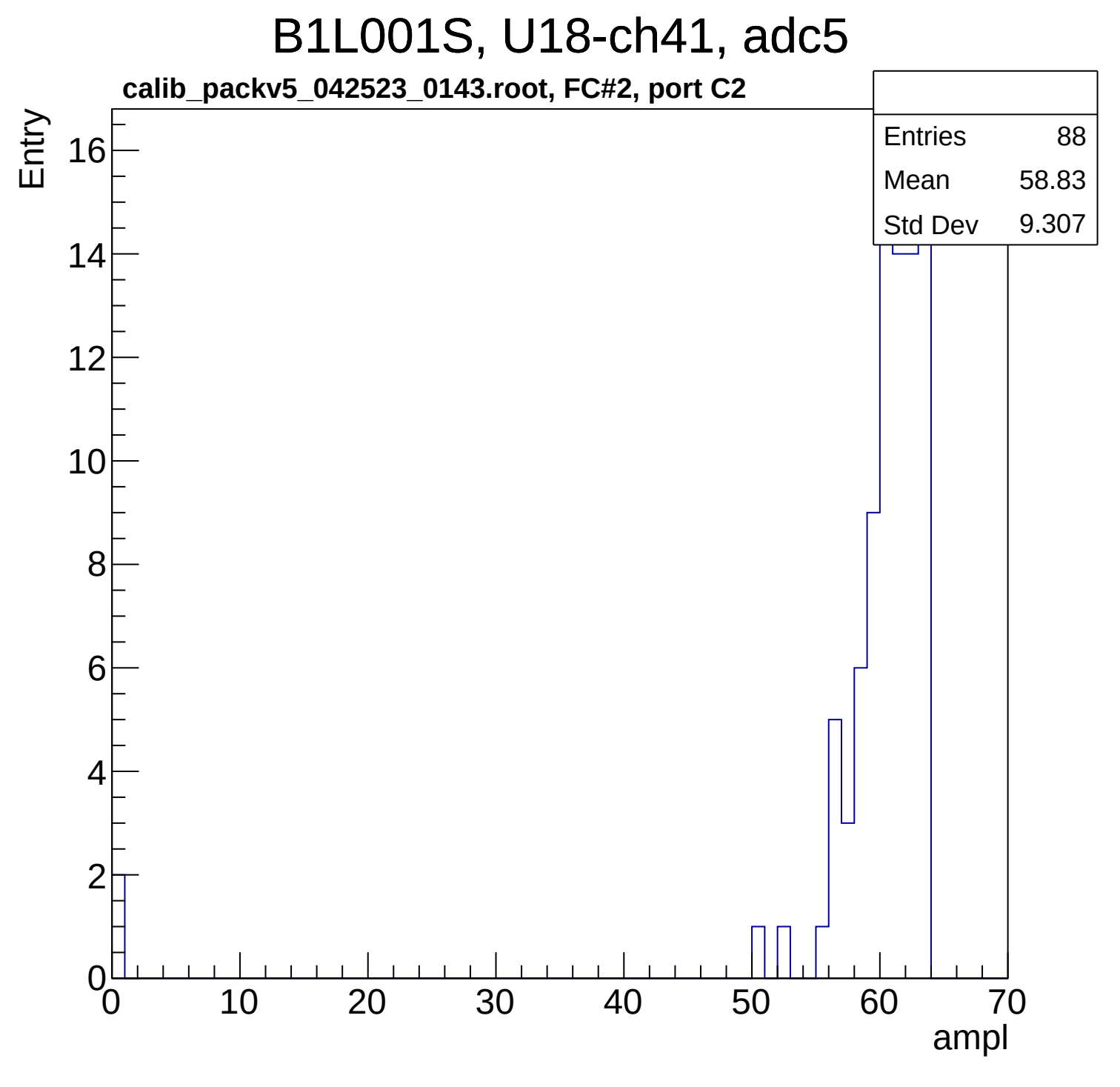

B1L001S, U18-ch41, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 144
Mean 29.97
Std Dev 3.419
Gaus mean : 30.6159
Gaus Width: 3.4595
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

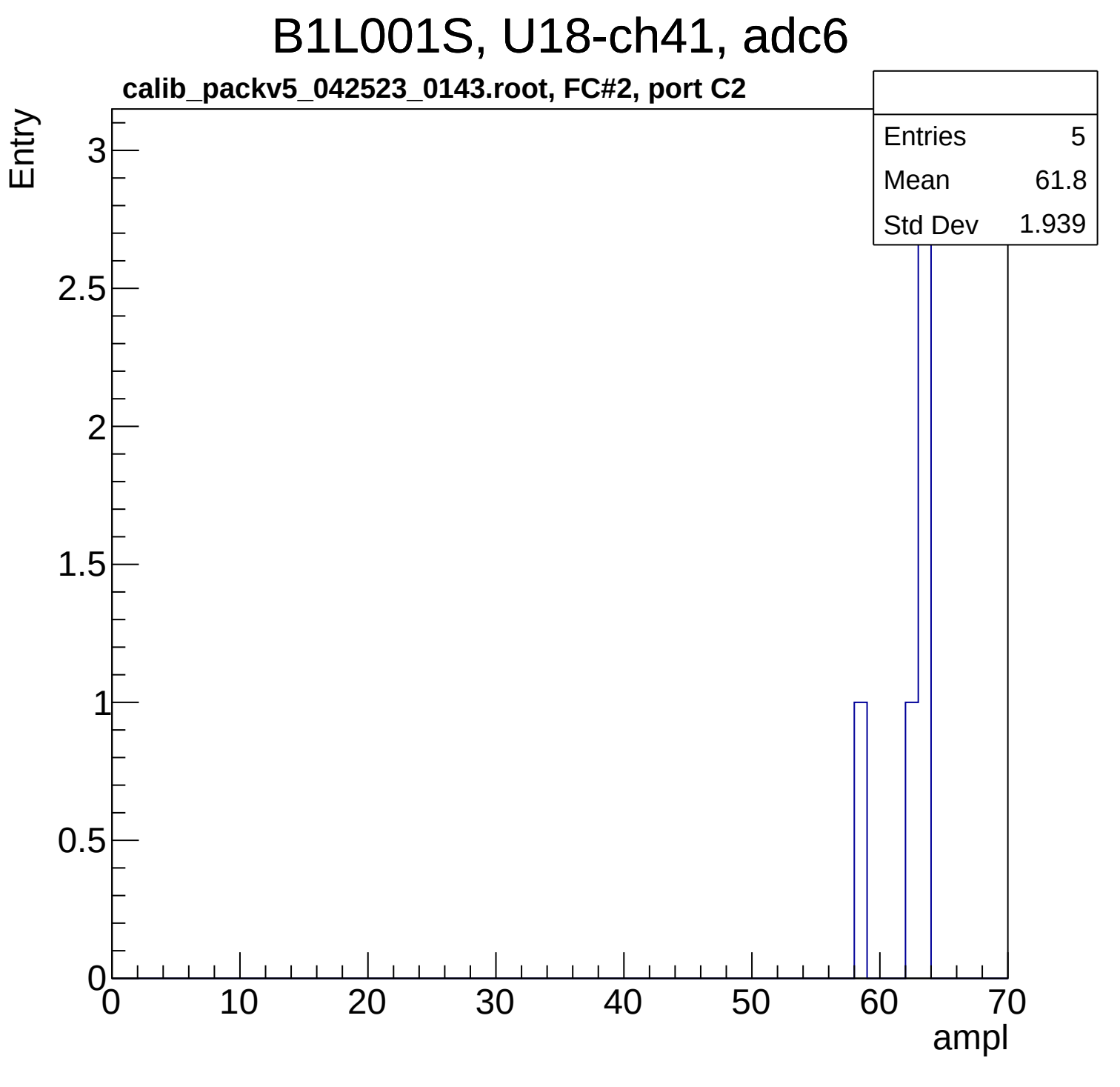

B1L001S, U18-ch41, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 125
Mean 36.6
Std Dev 3.418
Gaus mean : 37.2256
Gaus Width: 3.3529
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

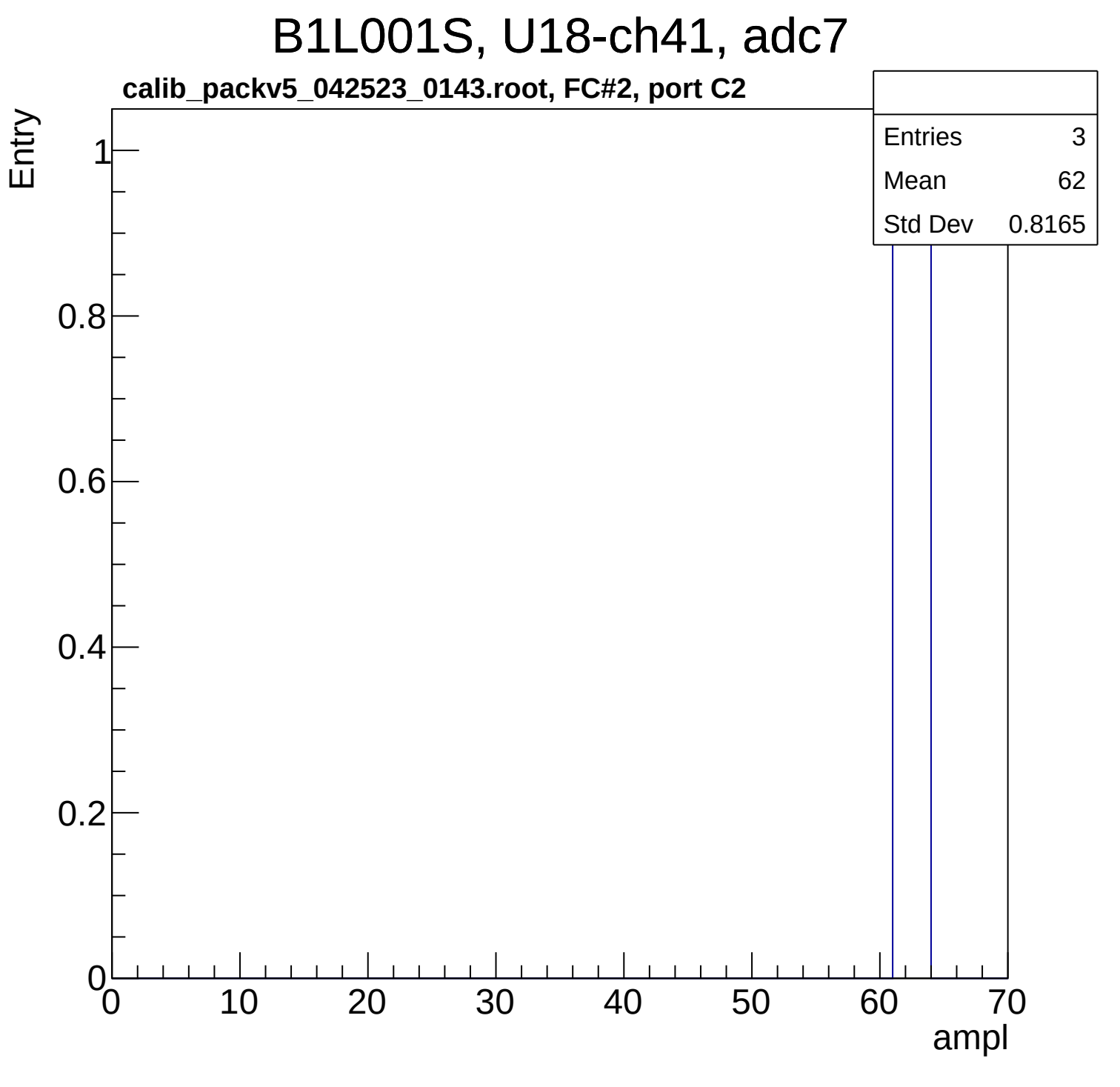

B1L001S, U18-ch41, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 104
Mean 42.17
Std Dev 3.318
Gaus mean : 42.9270
Gaus Width: 2.8694
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

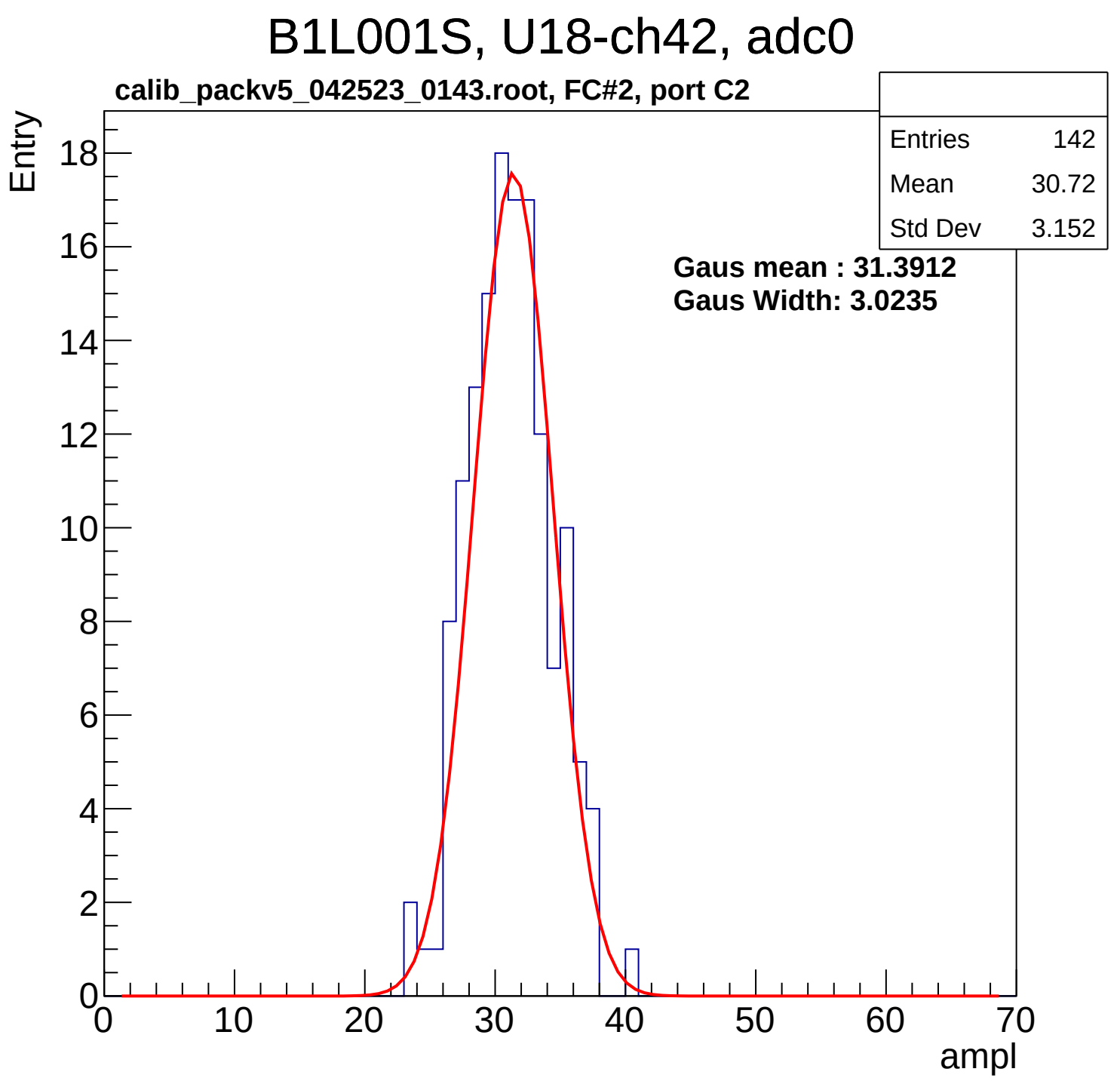

B1L001S, U18-ch41, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 185
Mean 49.68
Std Dev 4.019
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

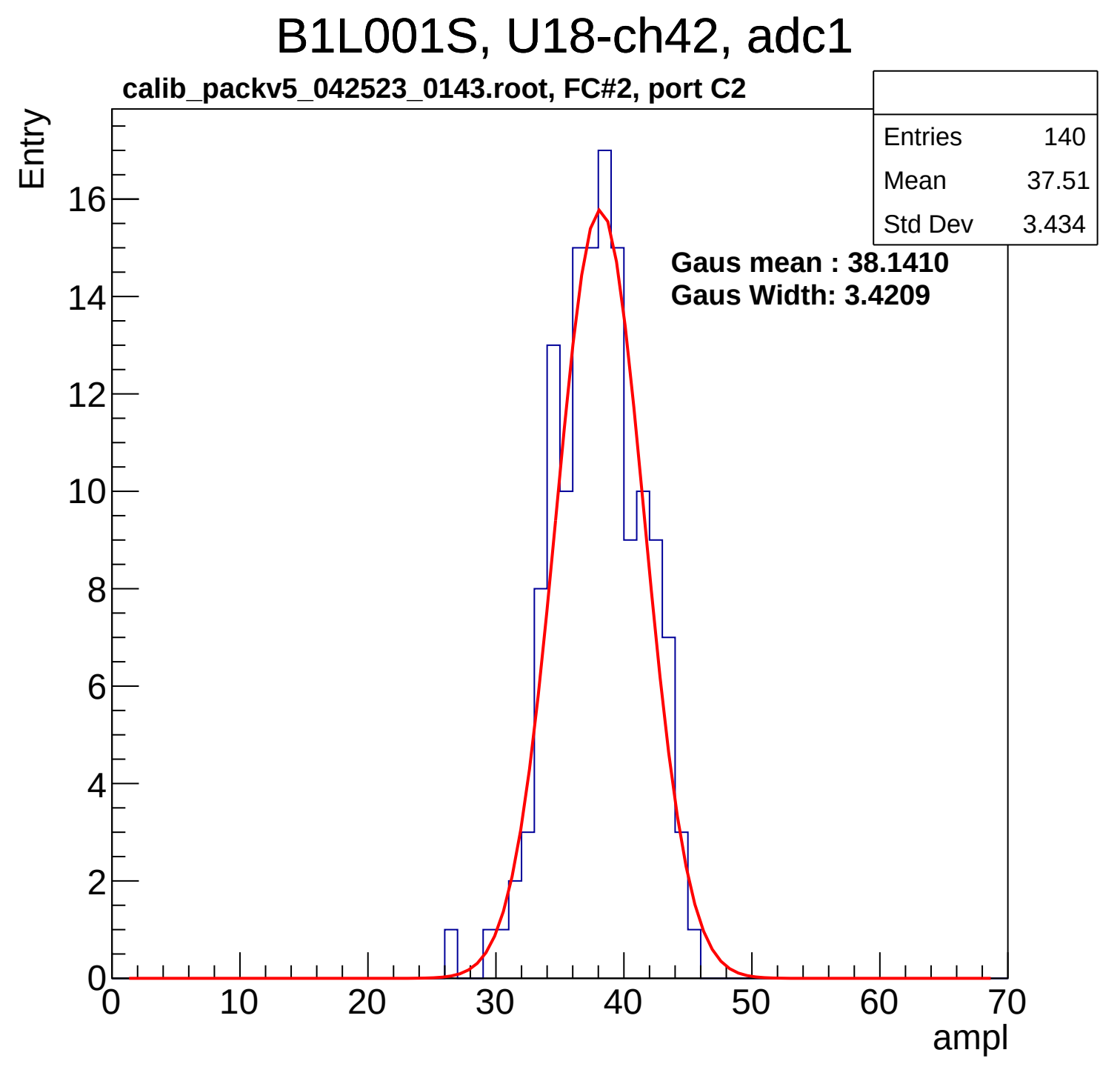

B1L001S, U18-ch41, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 93
Mean 56.17
Std Dev 2.993
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

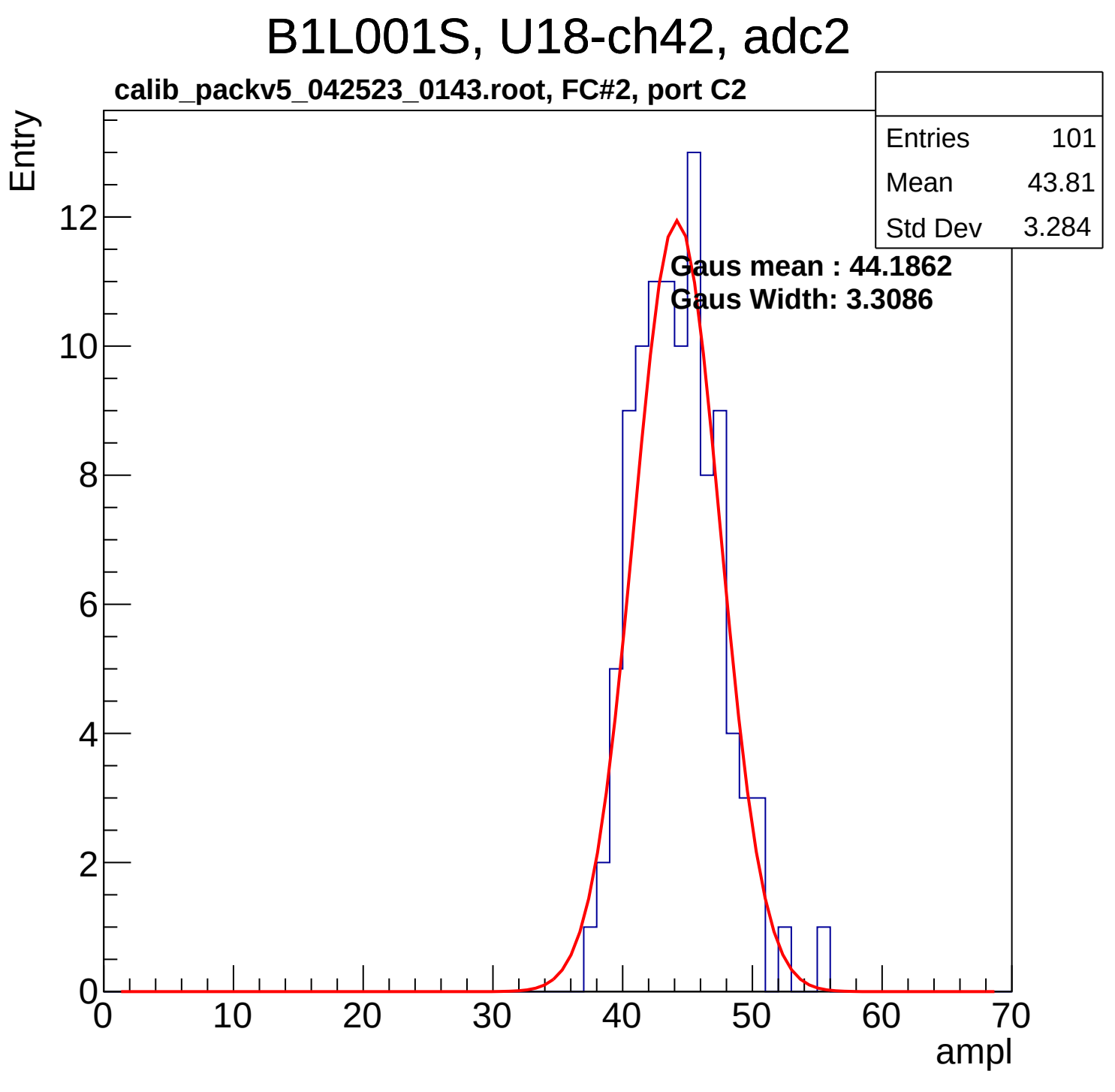

B1L001S, U18-ch41, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 88
Mean 58.83
Std Dev 9.307
Entry
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl

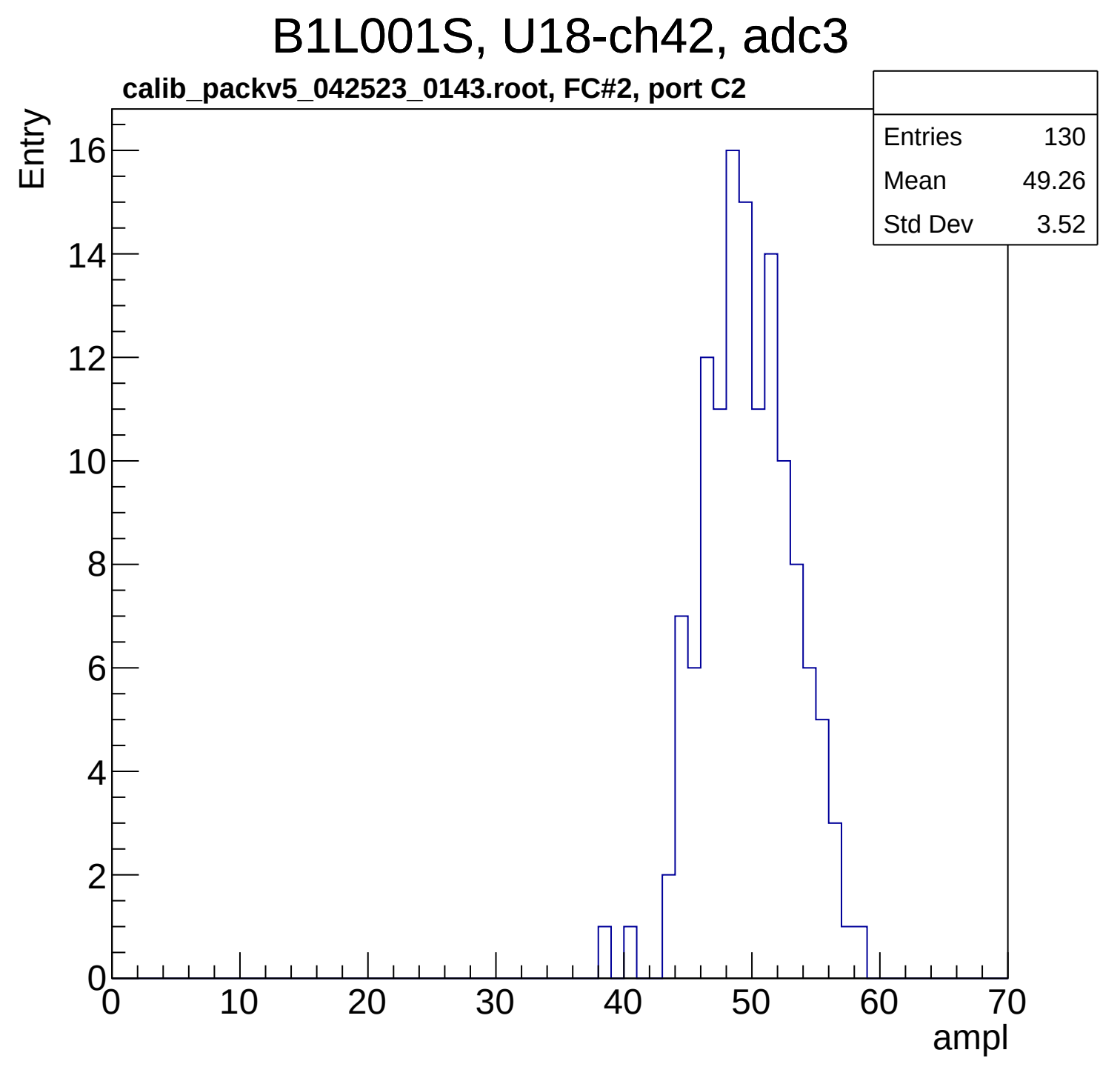

B1L001S, U18-ch41, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 5
Mean 61.8
Std Dev 1.939
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

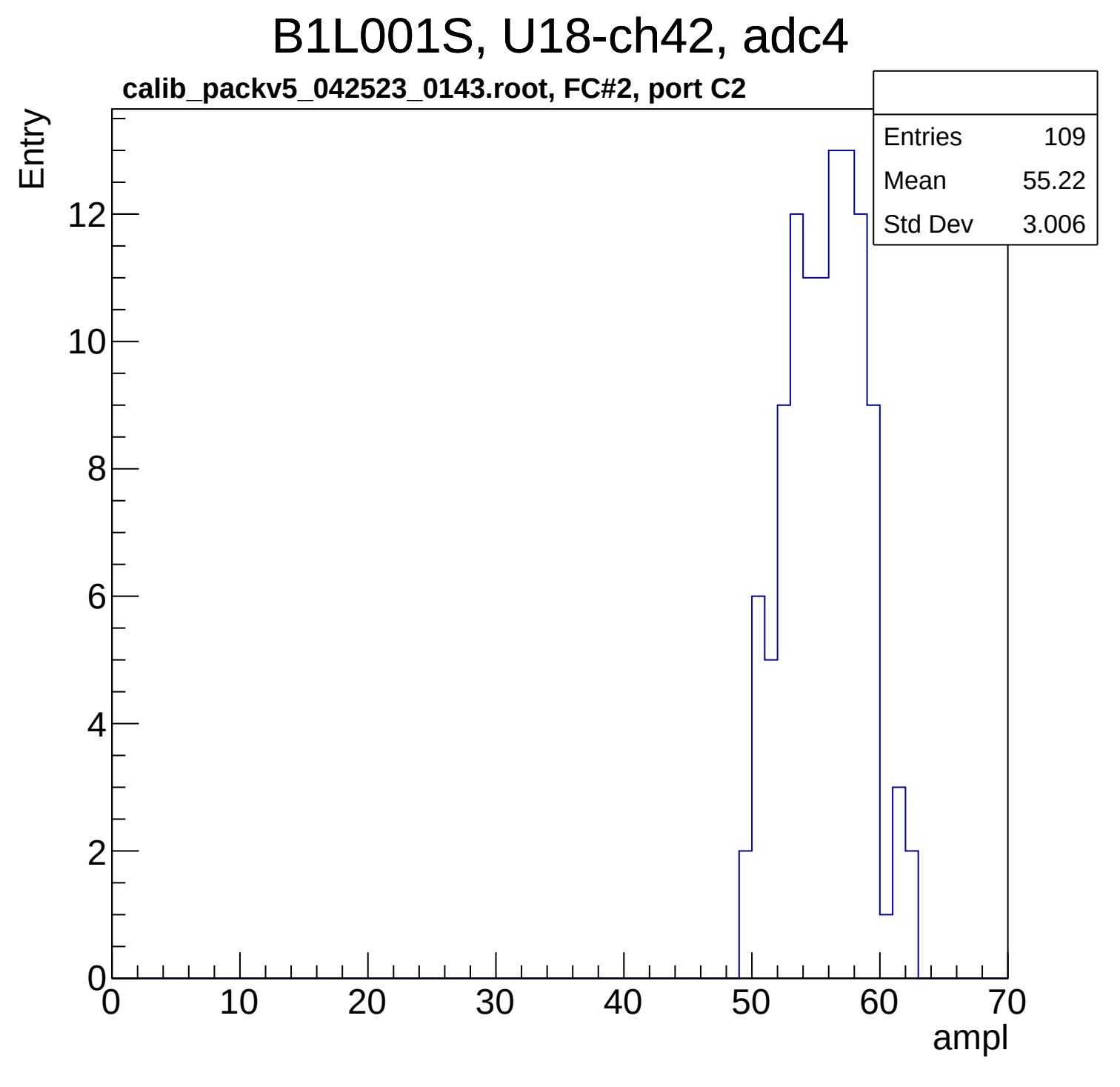

B1L001S, U18-ch41, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 3
Mean 62
Std Dev 0.8165
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

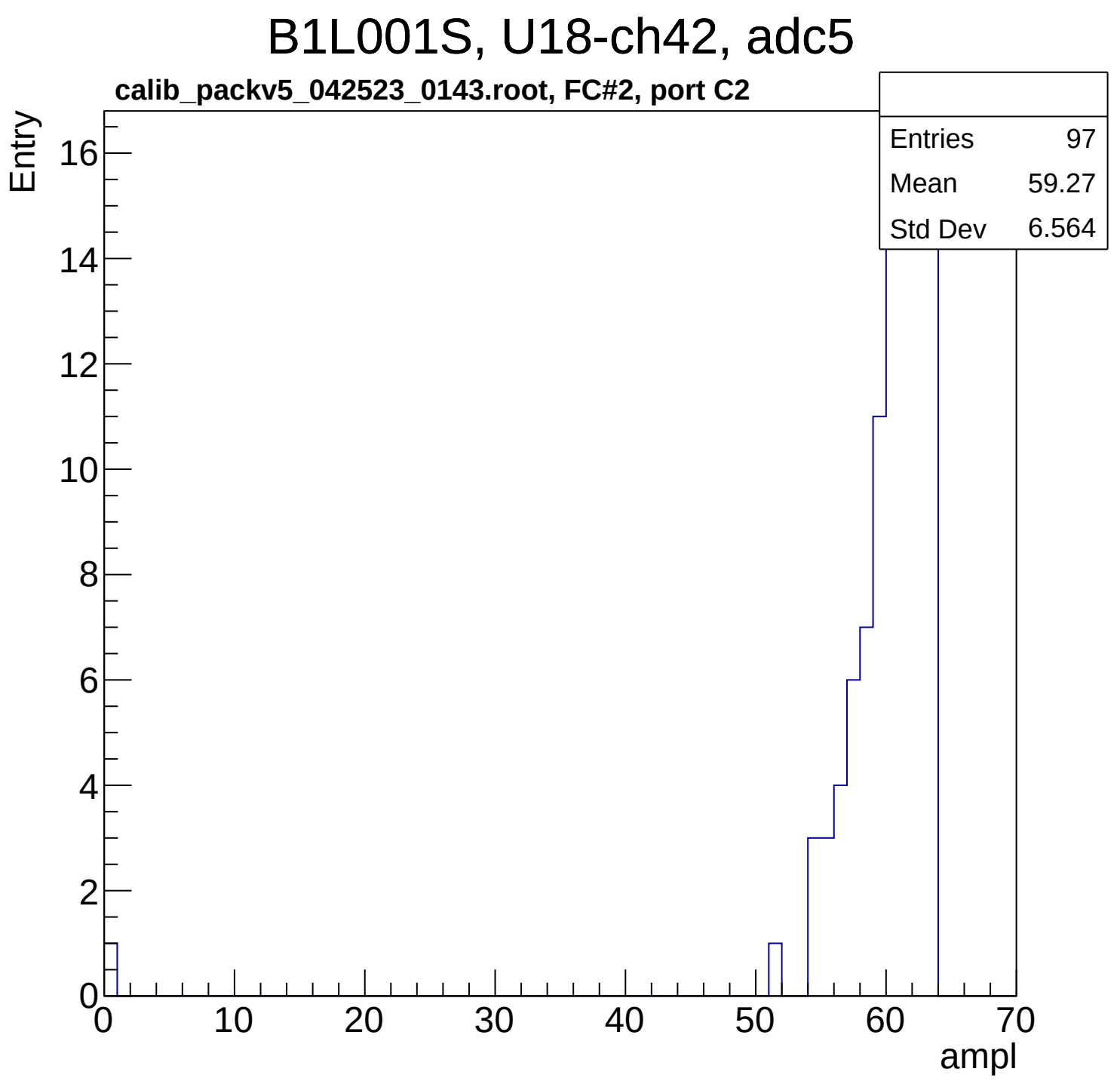

B1L001S, U18-ch42, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 142
Mean 30.72
Std Dev 3.152
Gaus mean : 31.3912
Gaus Width: 3.0235
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

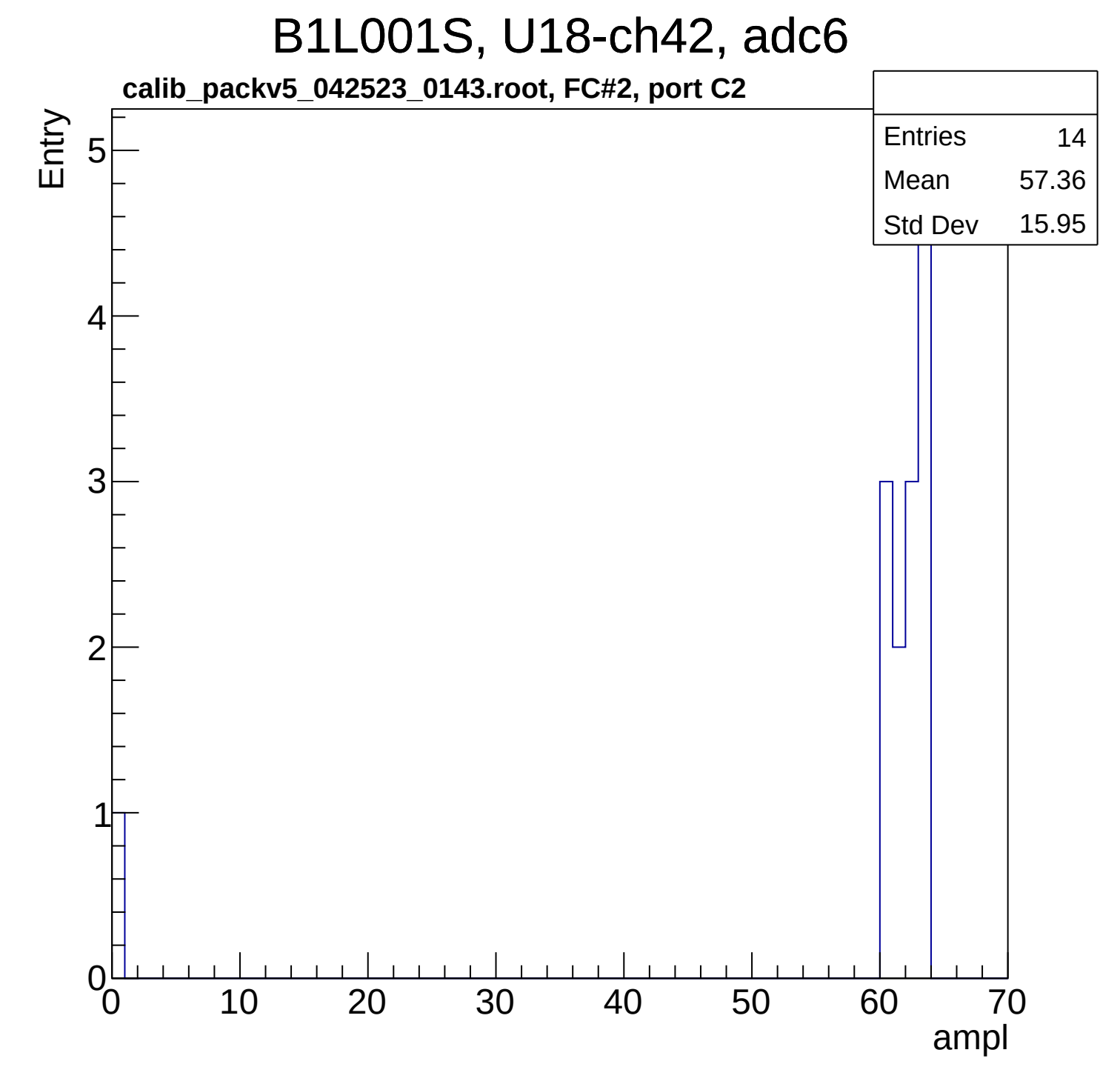

B1L001S, U18-ch42, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 140
Mean 37.51
Std Dev 3.434
Gaus mean : 38.1410
Gaus Width: 3.4209
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

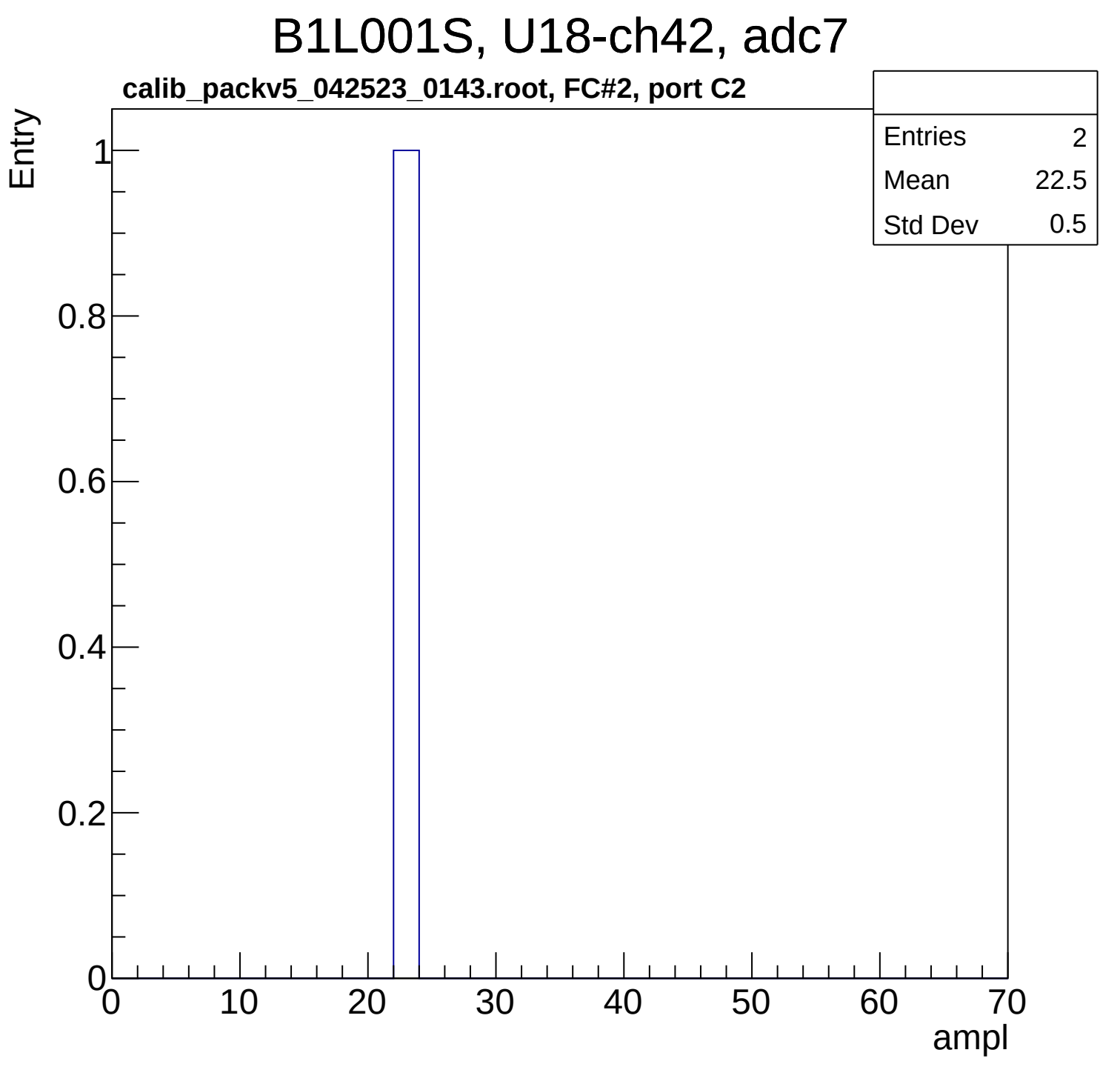

B1L001S, U18-ch42, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 101
Mean 43.81
Std Dev 3.284
Gaus mean : 44.1862
Gaus Width: 3.3086
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70

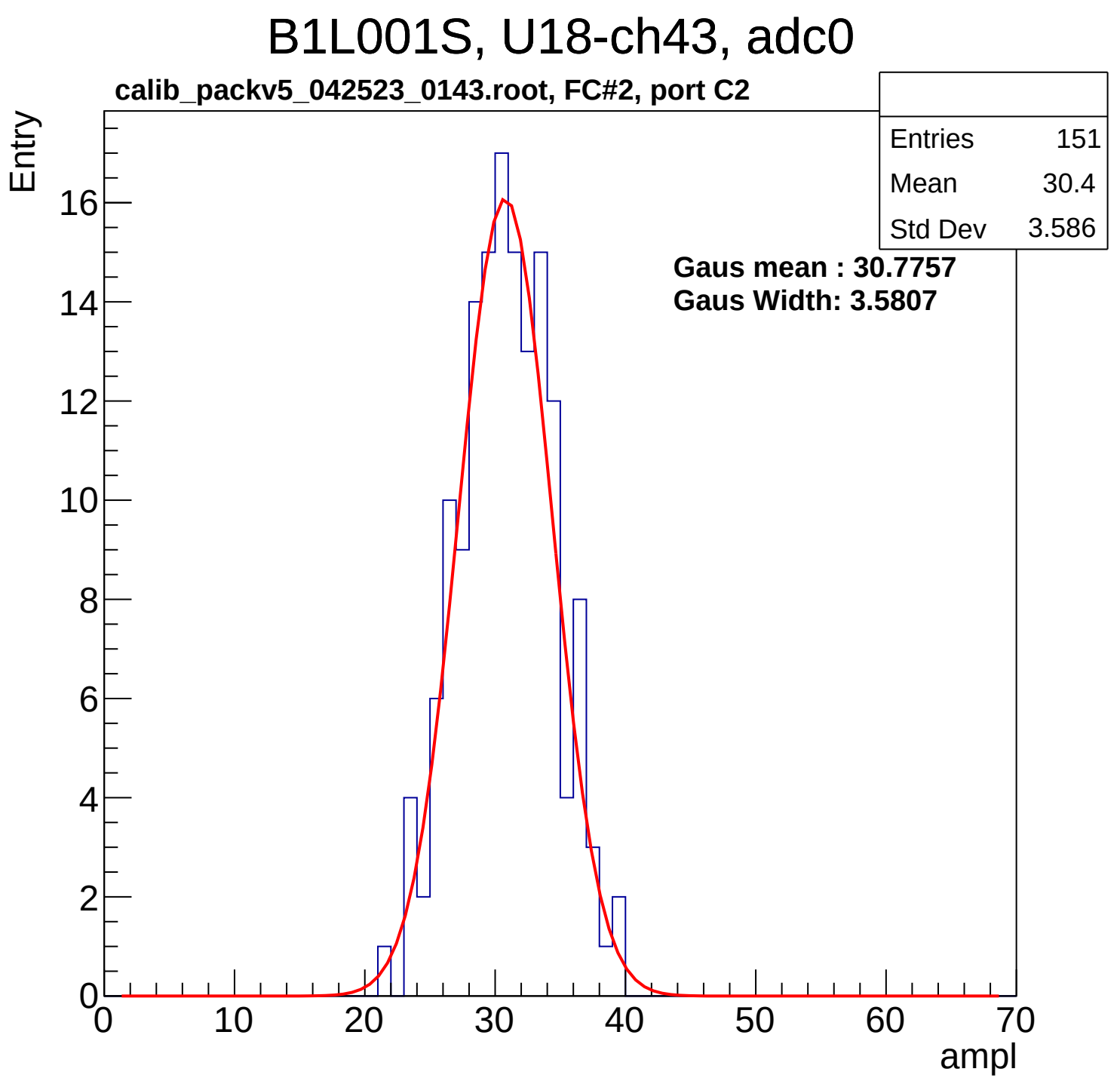

B1L001S, U18-ch42, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 130
Mean 49.26
Std Dev 3.52
Entry
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl

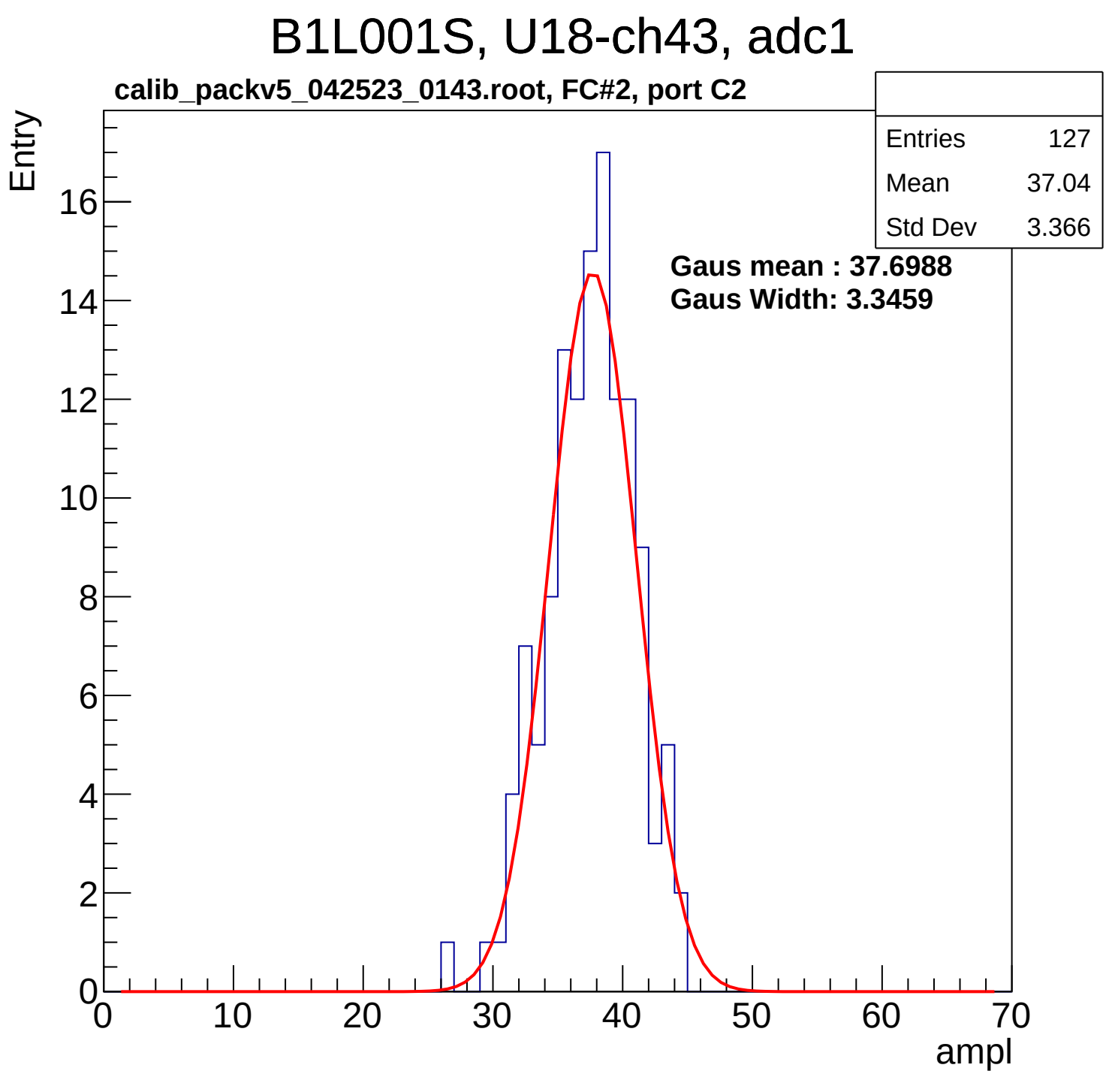

B1L001S, U18-ch42, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 109
Mean 55.22
Std Dev 3.006
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl

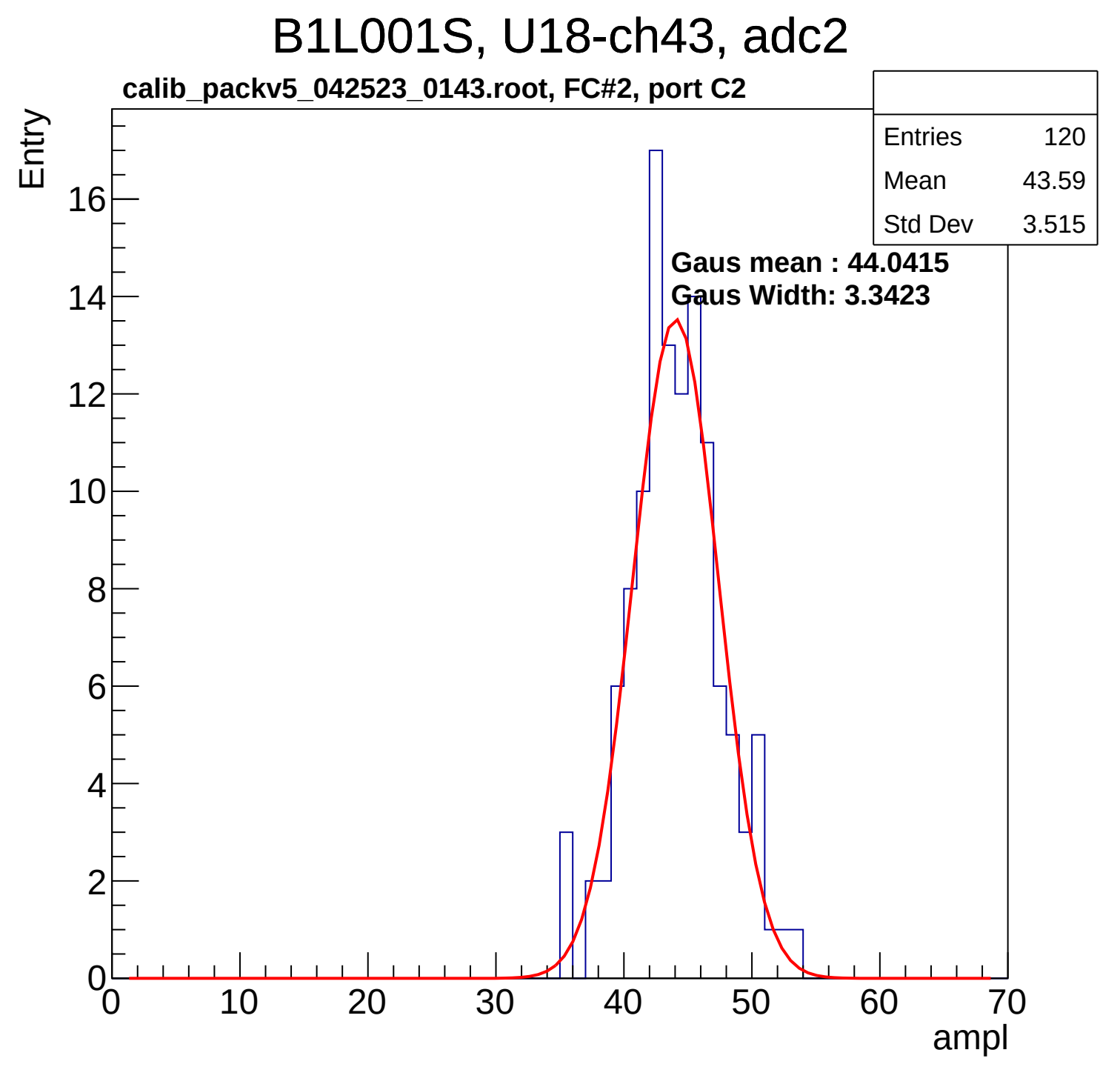

B1L001S, U18-ch42, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 97
Mean 59.27
Std Dev 6.564
Entry
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl

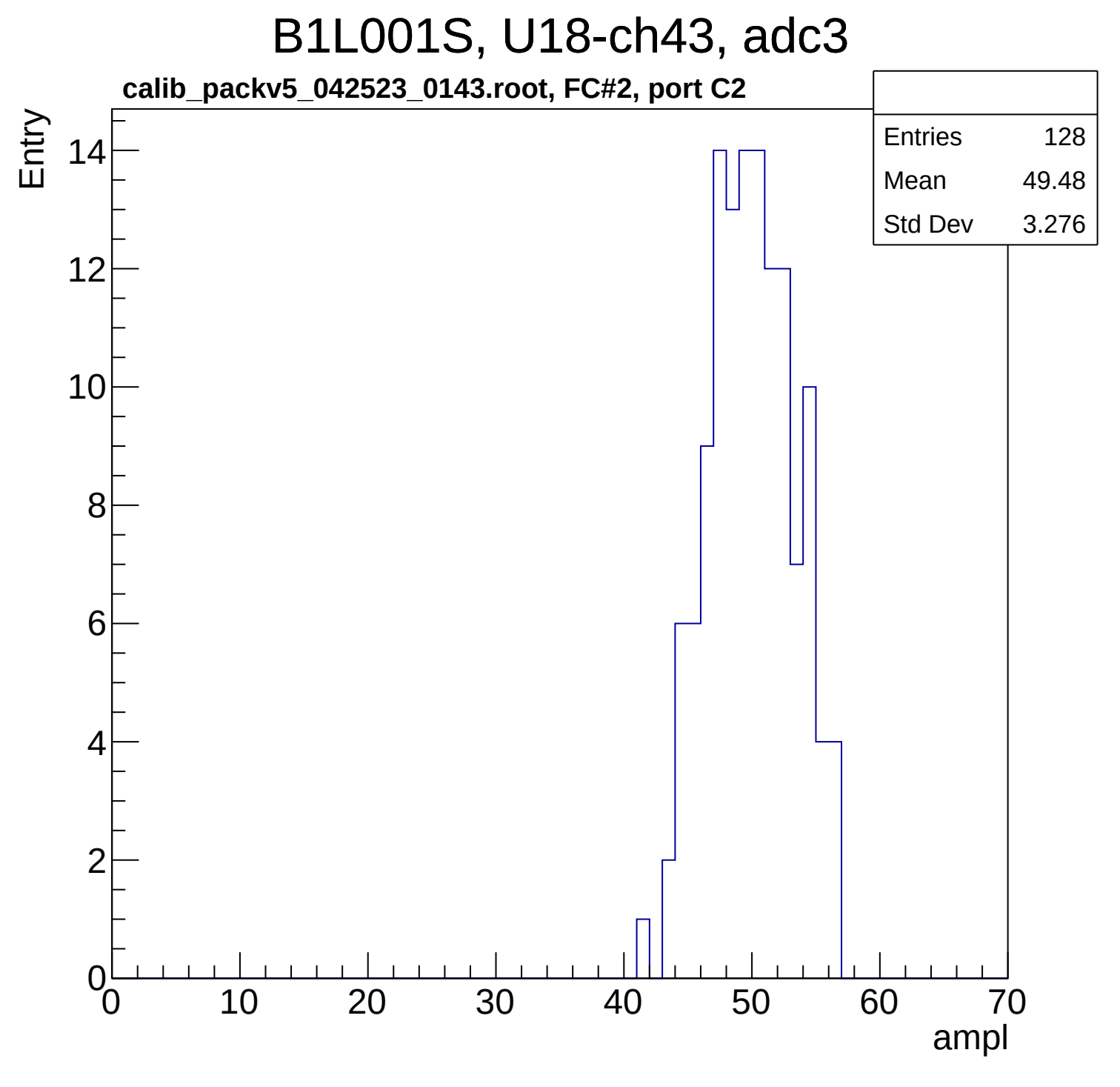

B1L001S, U18-ch42, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 14
Mean 57.36
Std Dev 15.95
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

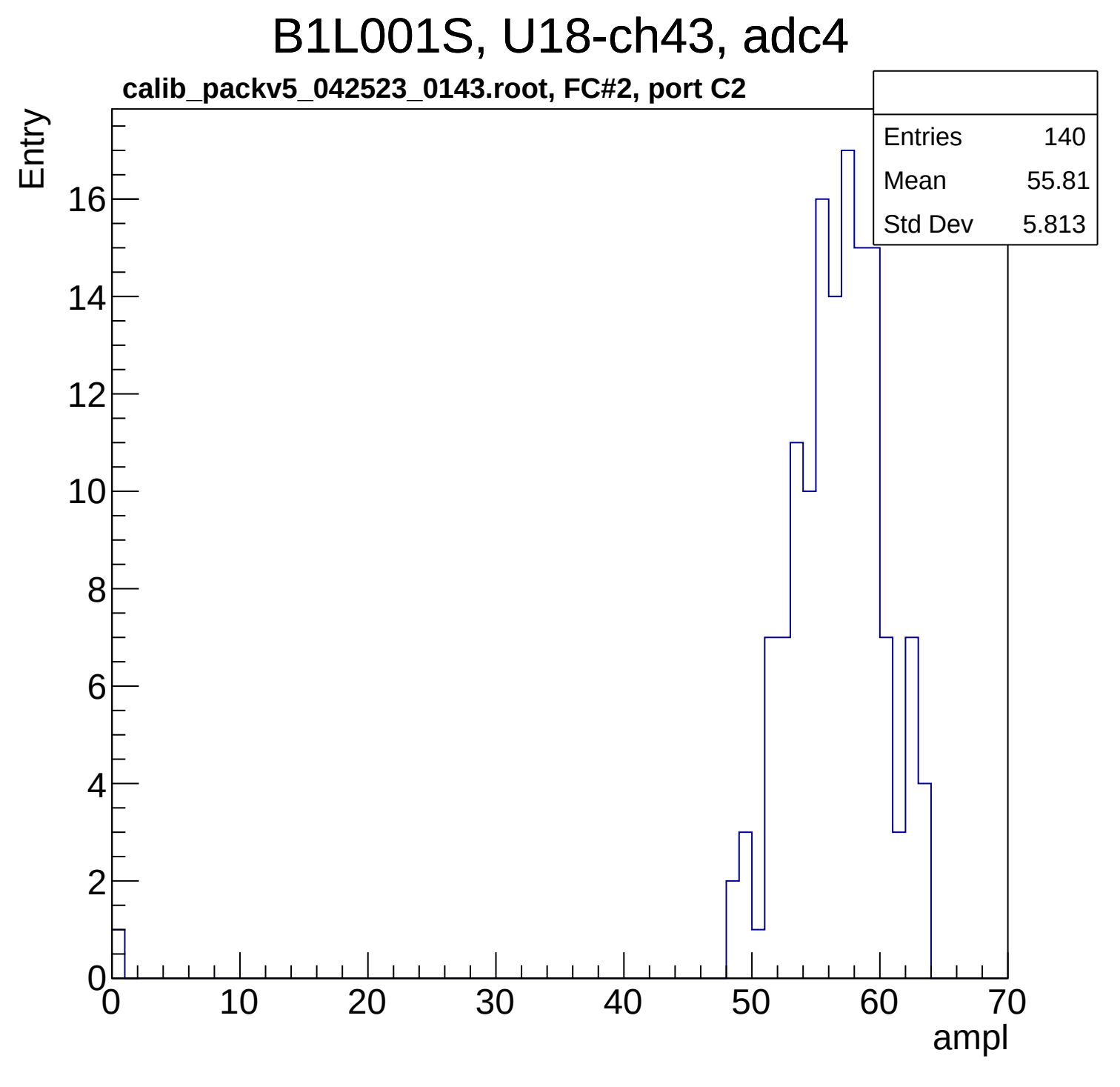

B1L001S, U18-ch42, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 22.5
Std Dev 0.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

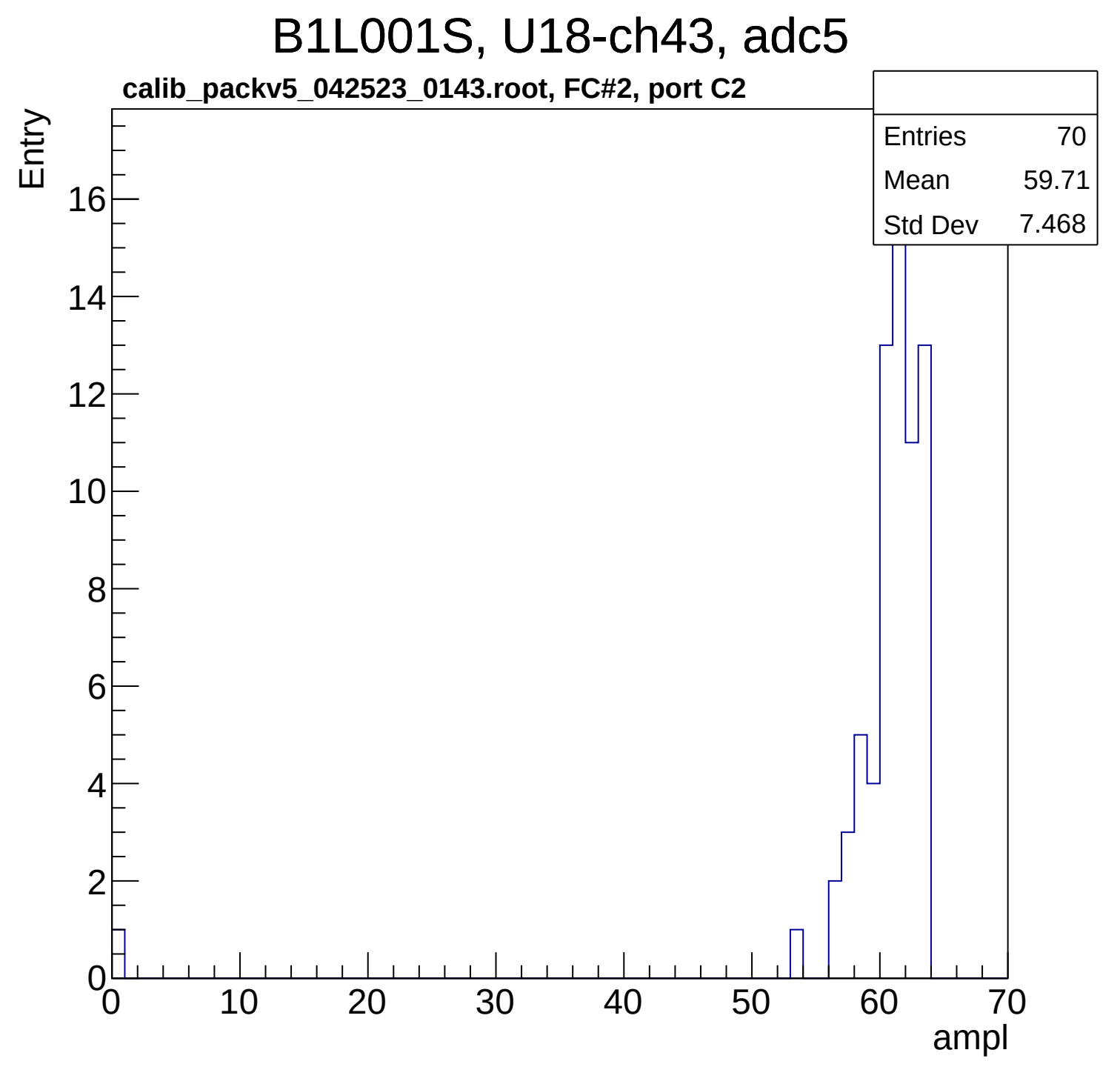

B1L001S, U18-ch43, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 151
Mean 30.4
Std Dev 3.586
Gaus mean : 30.7757
Gaus Width: 3.5807
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

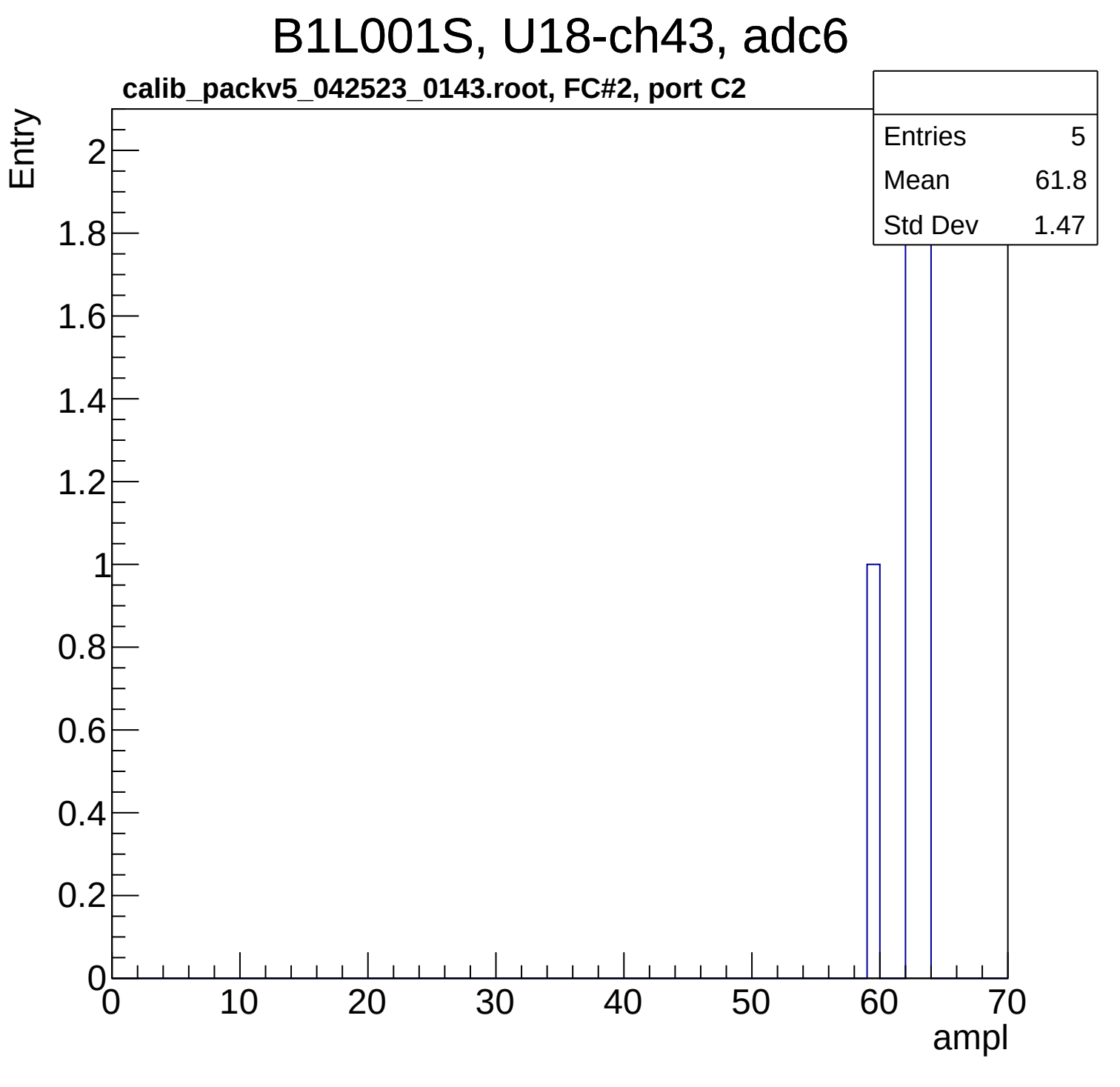

B1L001S, U18-ch43, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 127
Mean 37.04
Std Dev 3.366
Gaus mean : 37.6988
Gaus Width: 3.3459
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

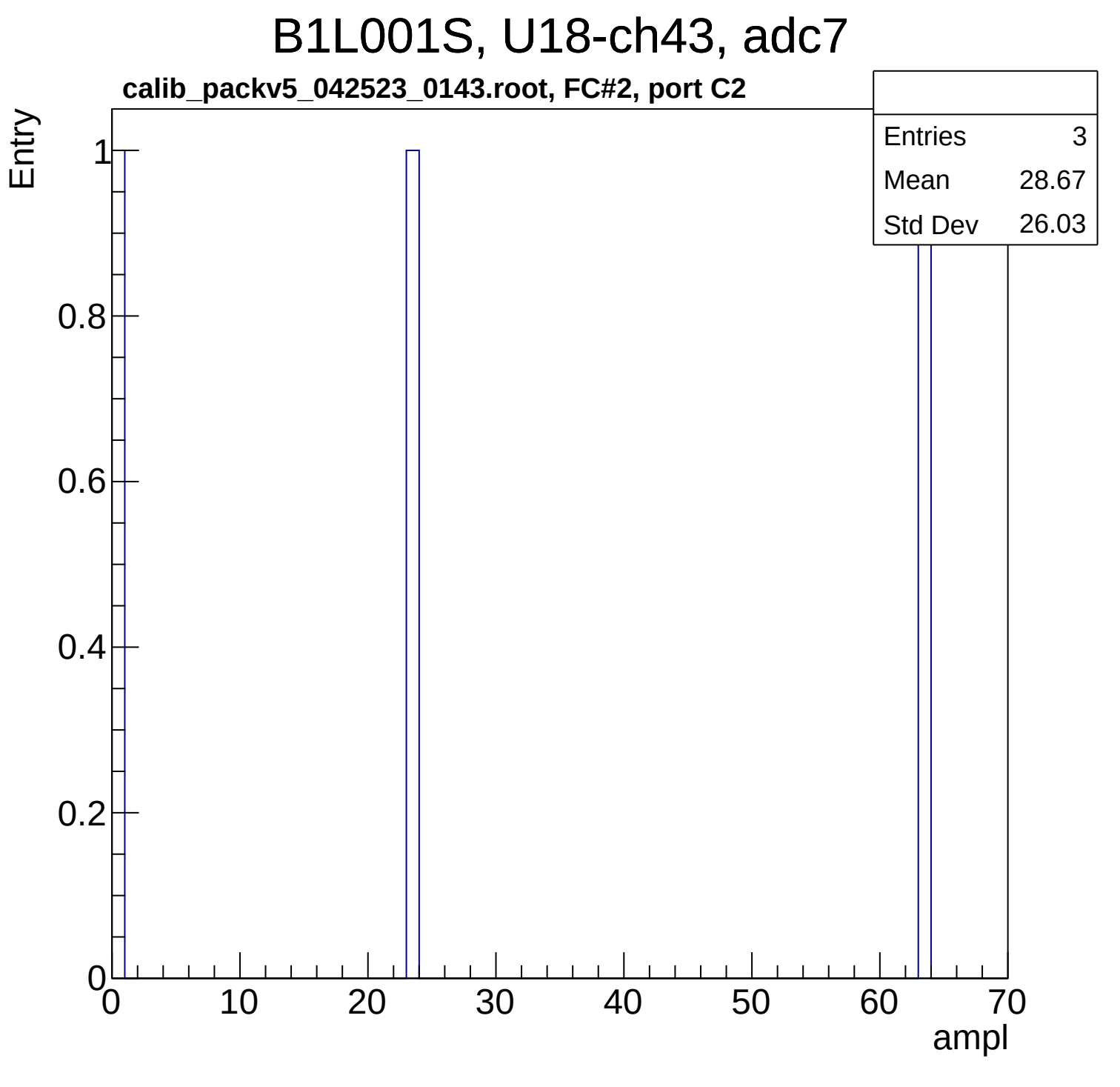

B1L001S, U18-ch43, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 120
Mean 43.59
Std Dev 3.515
Gaus mean : 44.0415
Gaus Width: 3.3423
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

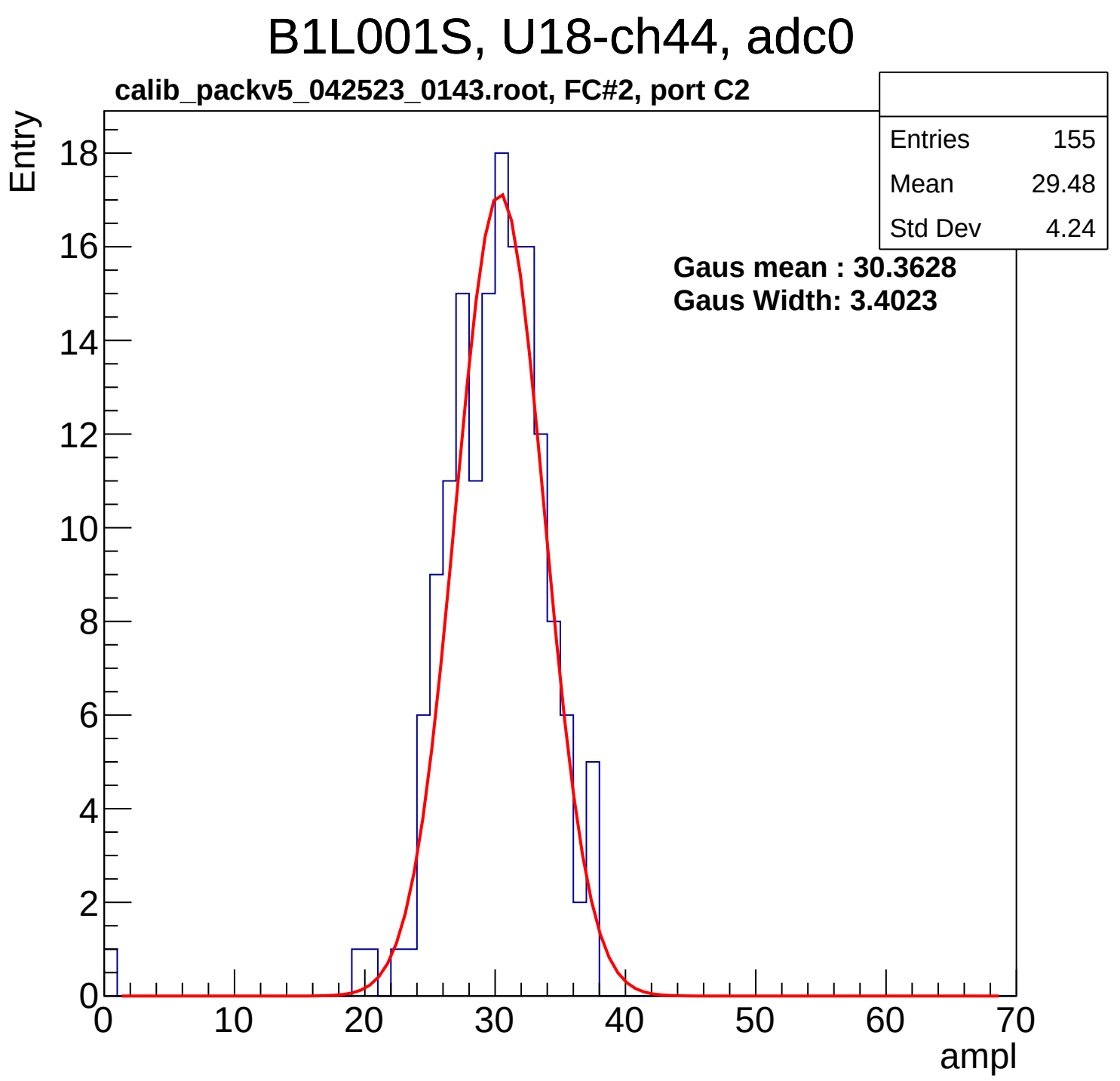

B1L001S, U18-ch43, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 128
Mean 49.48
Std Dev 3.276
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

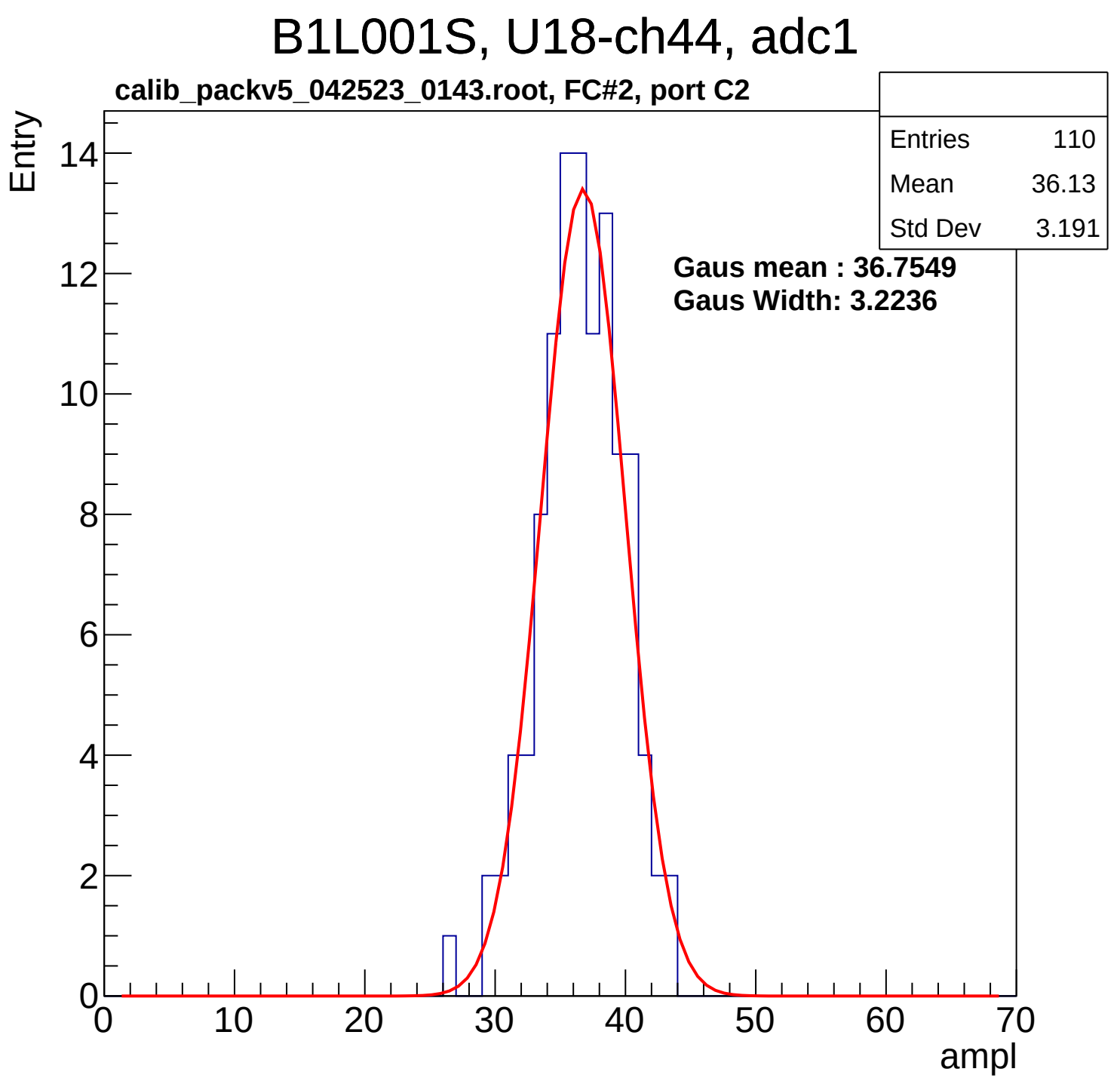

B1L001S, U18-ch43, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 140
Mean 55.81
Std Dev 5.813
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

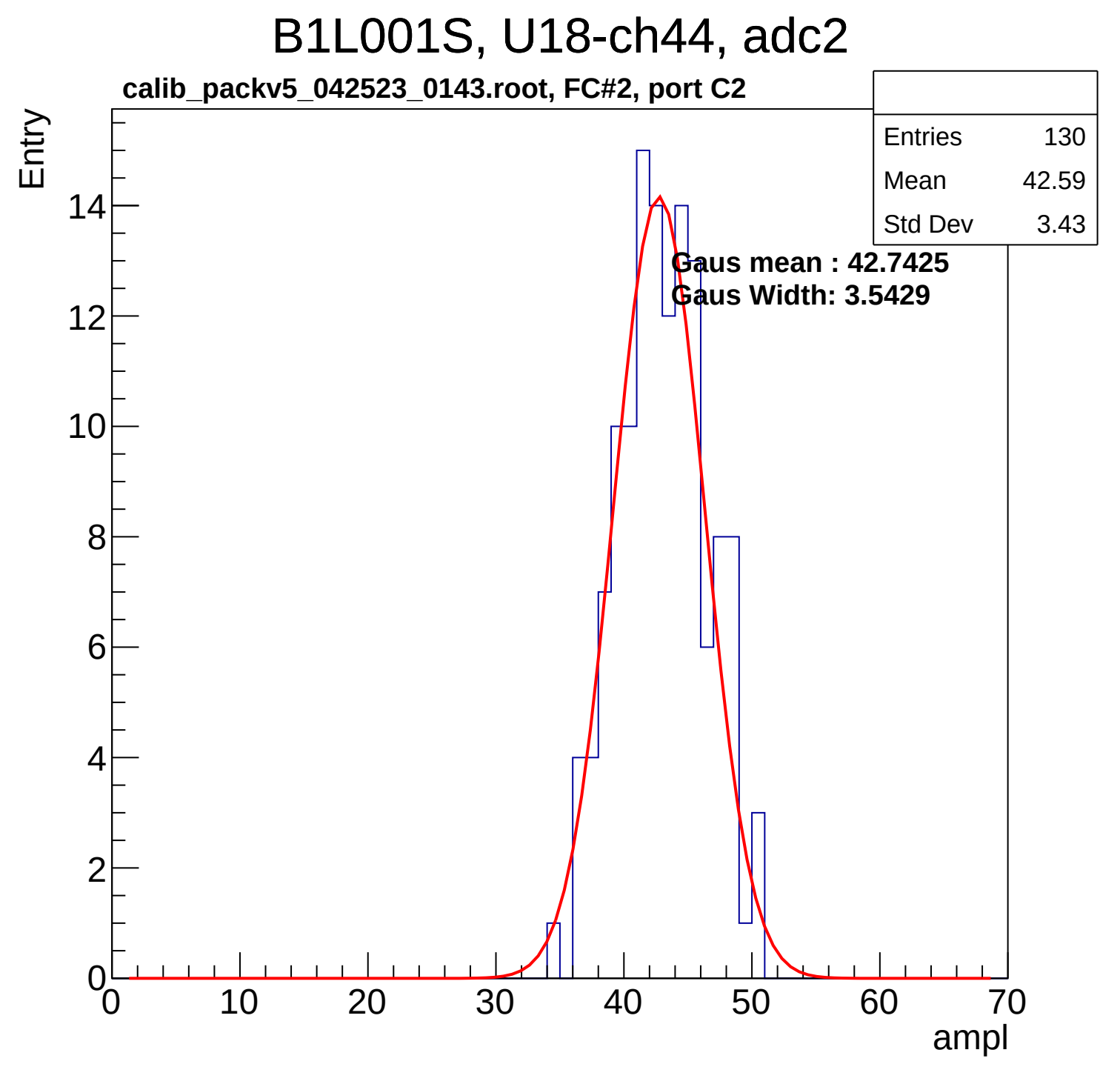

B1L001S, U18-ch43, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 70
Mean 59.71
Std Dev 7.468
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

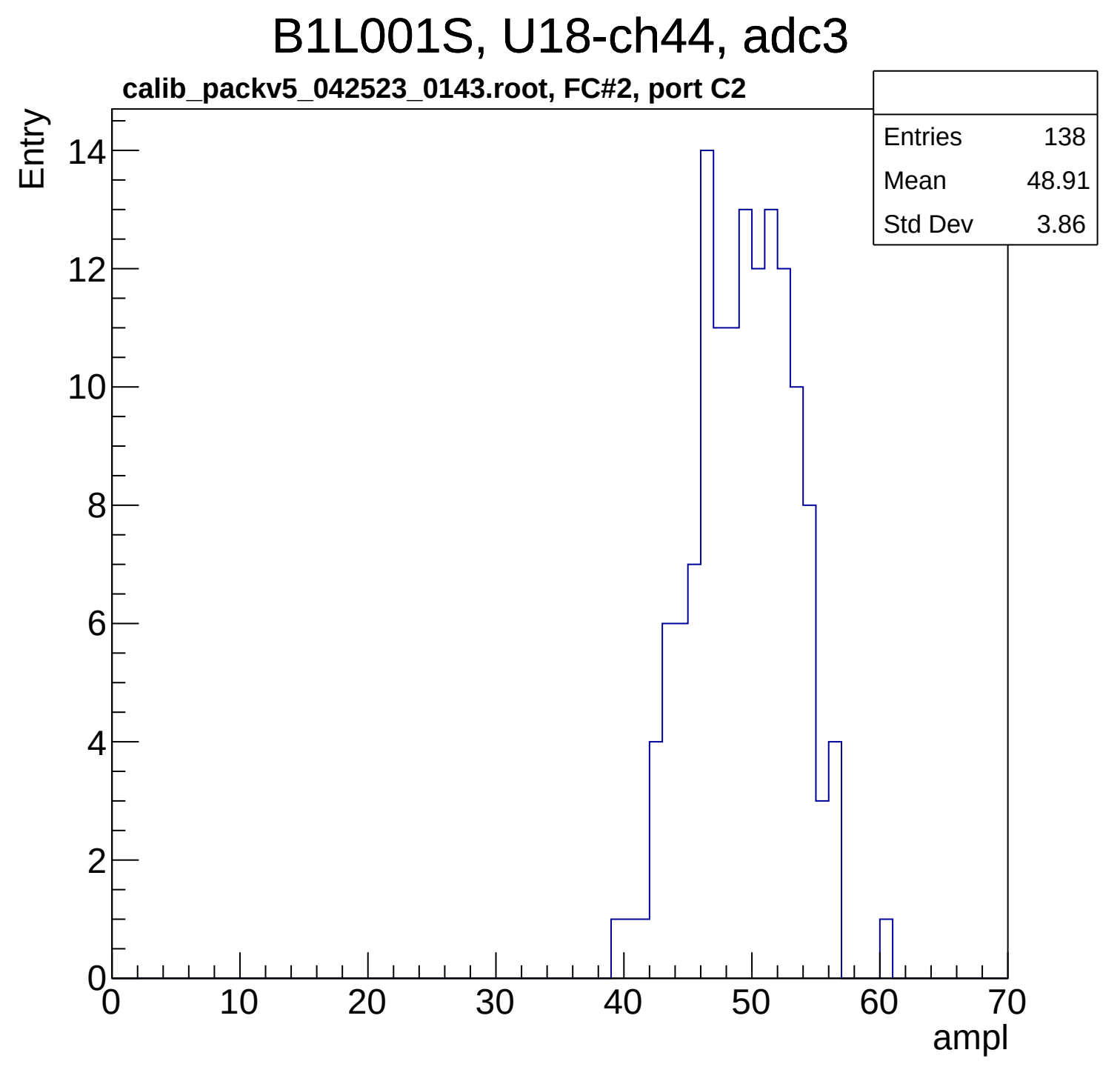

B1L001S, U18-ch43, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 5
Mean 61.8
Std Dev 1.47
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

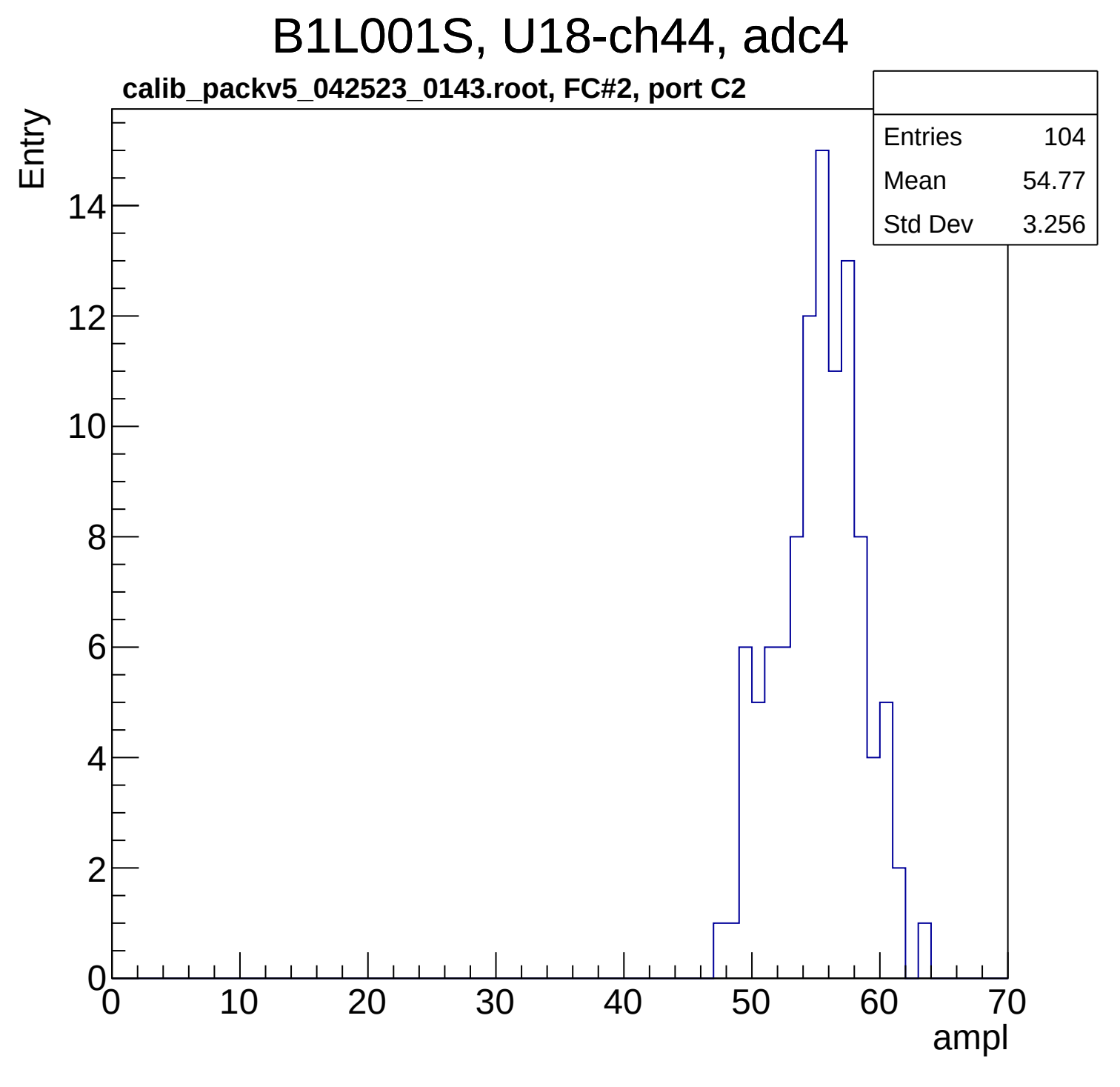

B1L001S, U18-ch43, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 3
Mean 28.67
Std Dev 26.03
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70

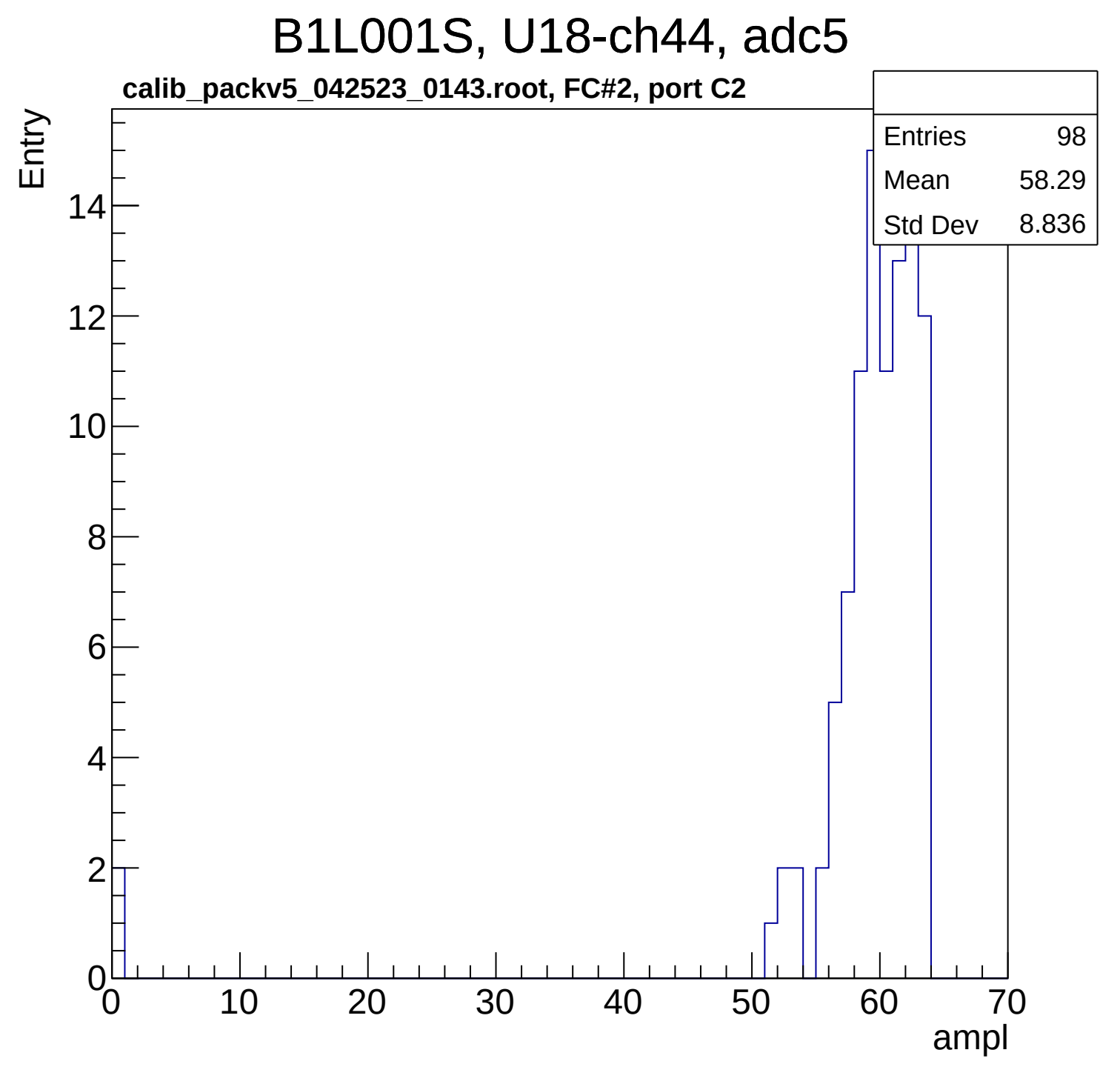

B1L001S, U18-ch44, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 155
Mean 29.48
Std Dev 4.24
Gaus mean : 30.3628
Gaus Width: 3.4023
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

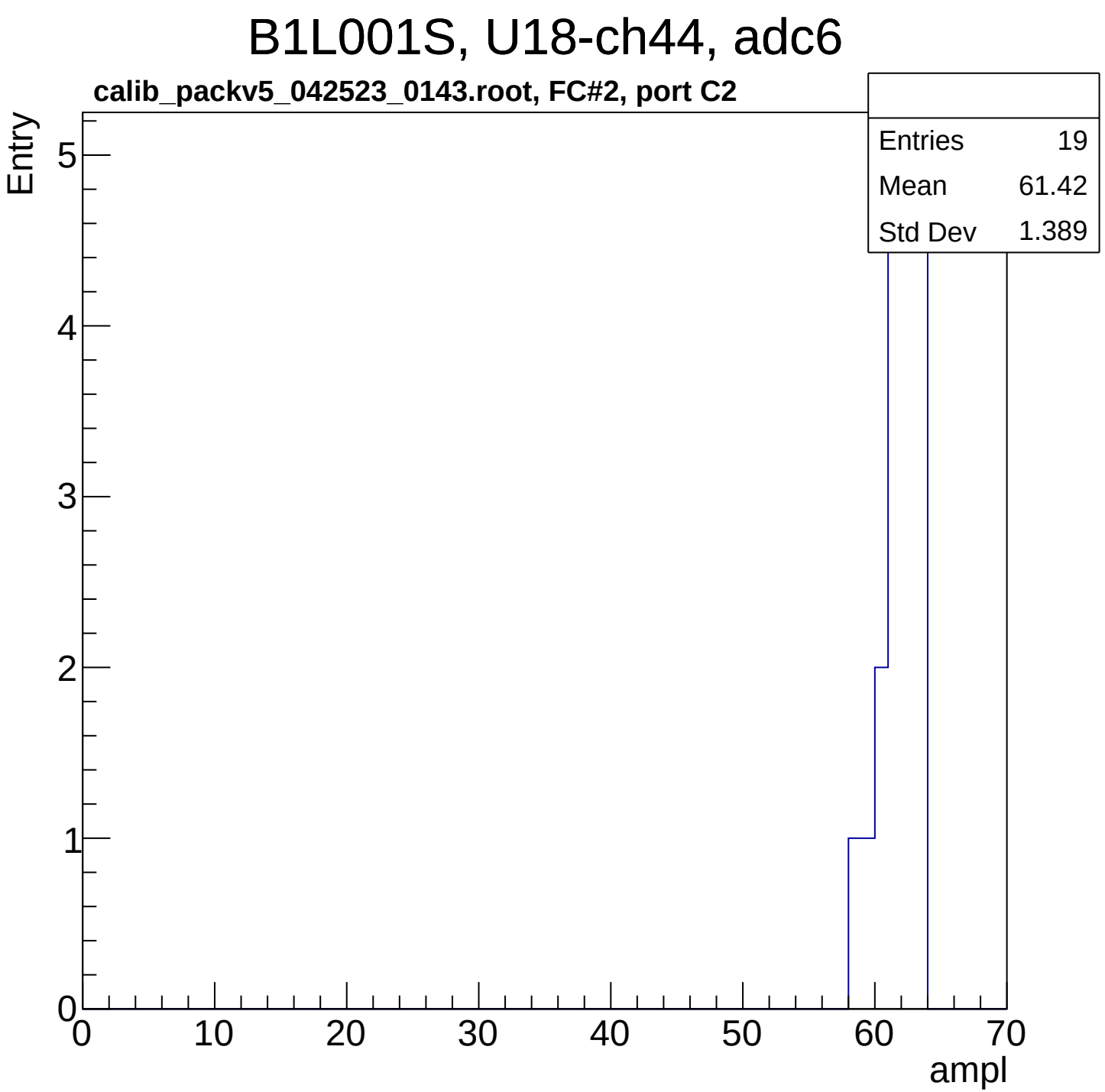

B1L001S, U18-ch44, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 110
Mean 36.13
Std Dev 3.191
Gaus mean : 36.7549
Gaus Width: 3.2236
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

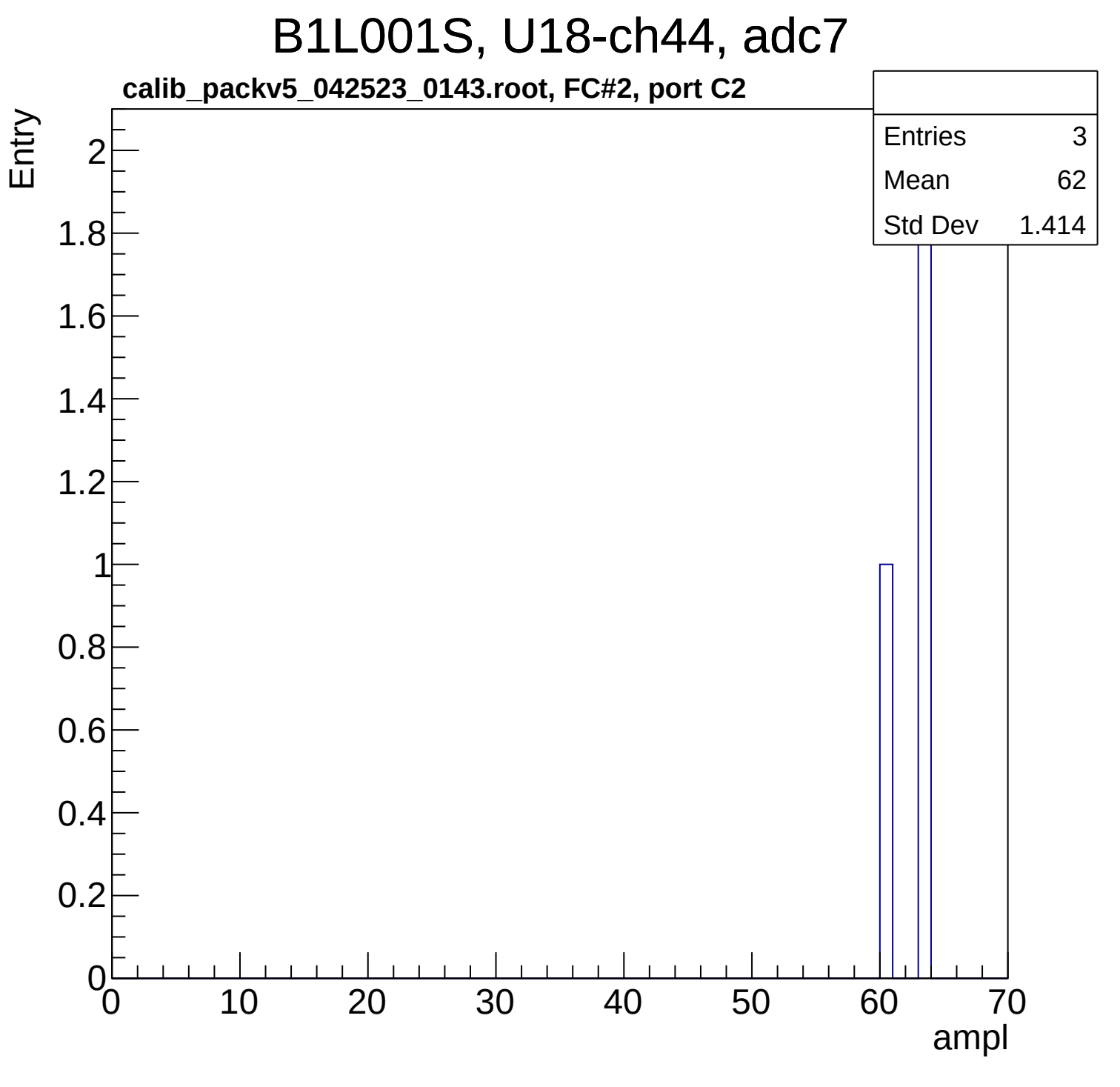

B1L001S, U18-ch44, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 130
Mean 42.59
Std Dev 3.43
Gaus mean : 42.7425
Gaus Width: 3.5429
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

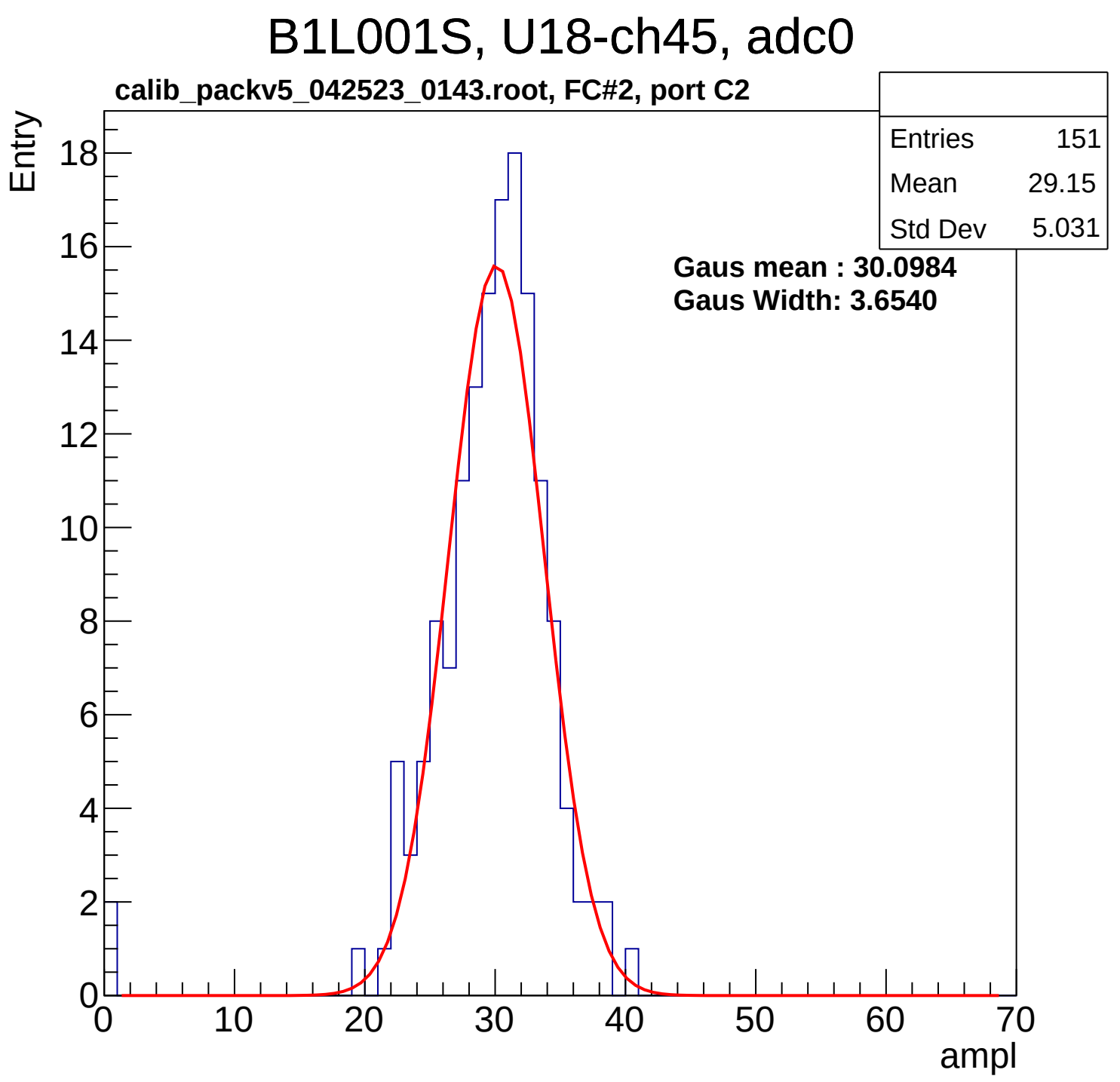

B1L001S, U18-ch44, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 138
Mean 48.91
Std Dev 3.86
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

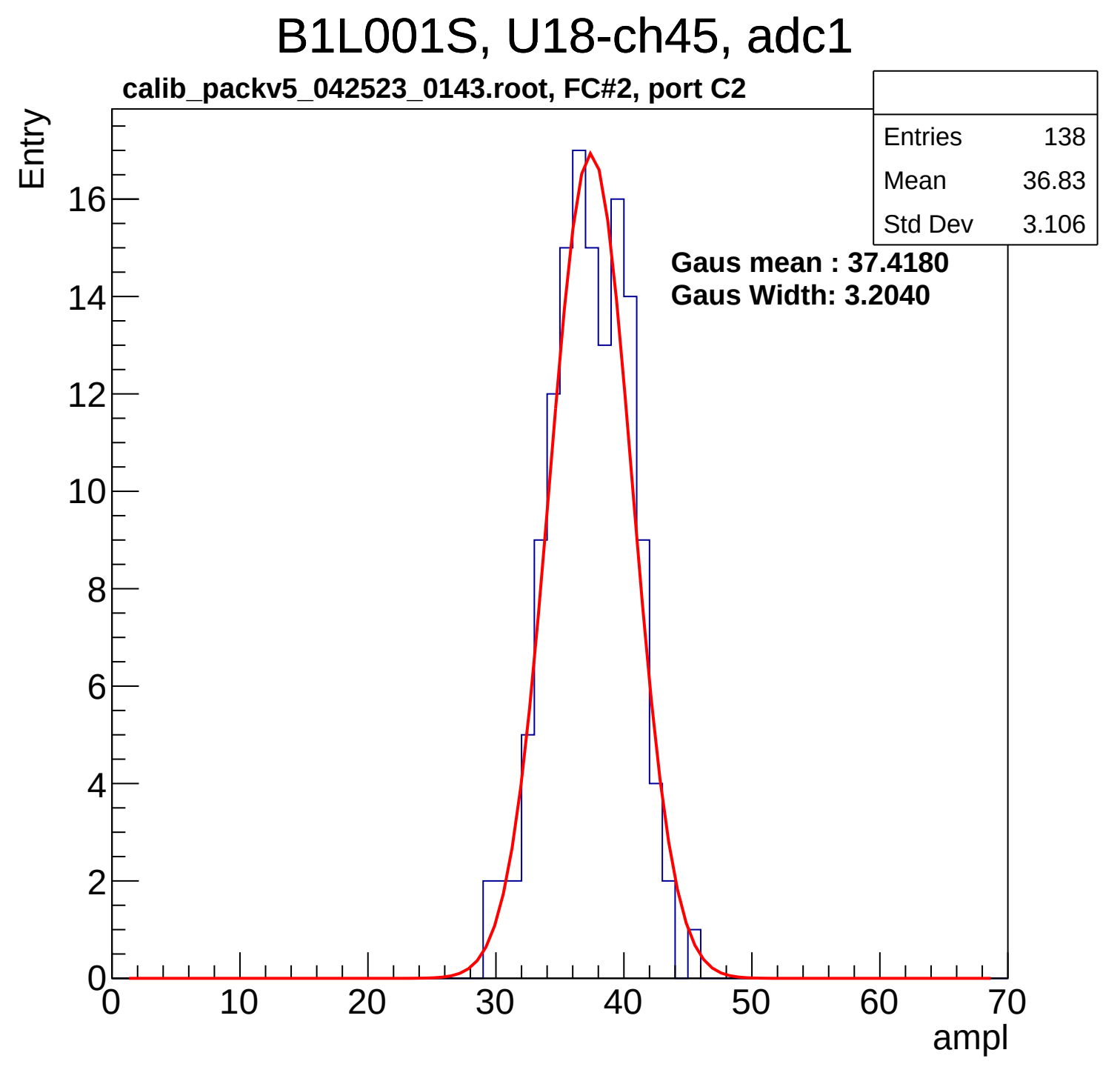

B1L001S, U18-ch44, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 104
Mean 54.77
Std Dev 3.256
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

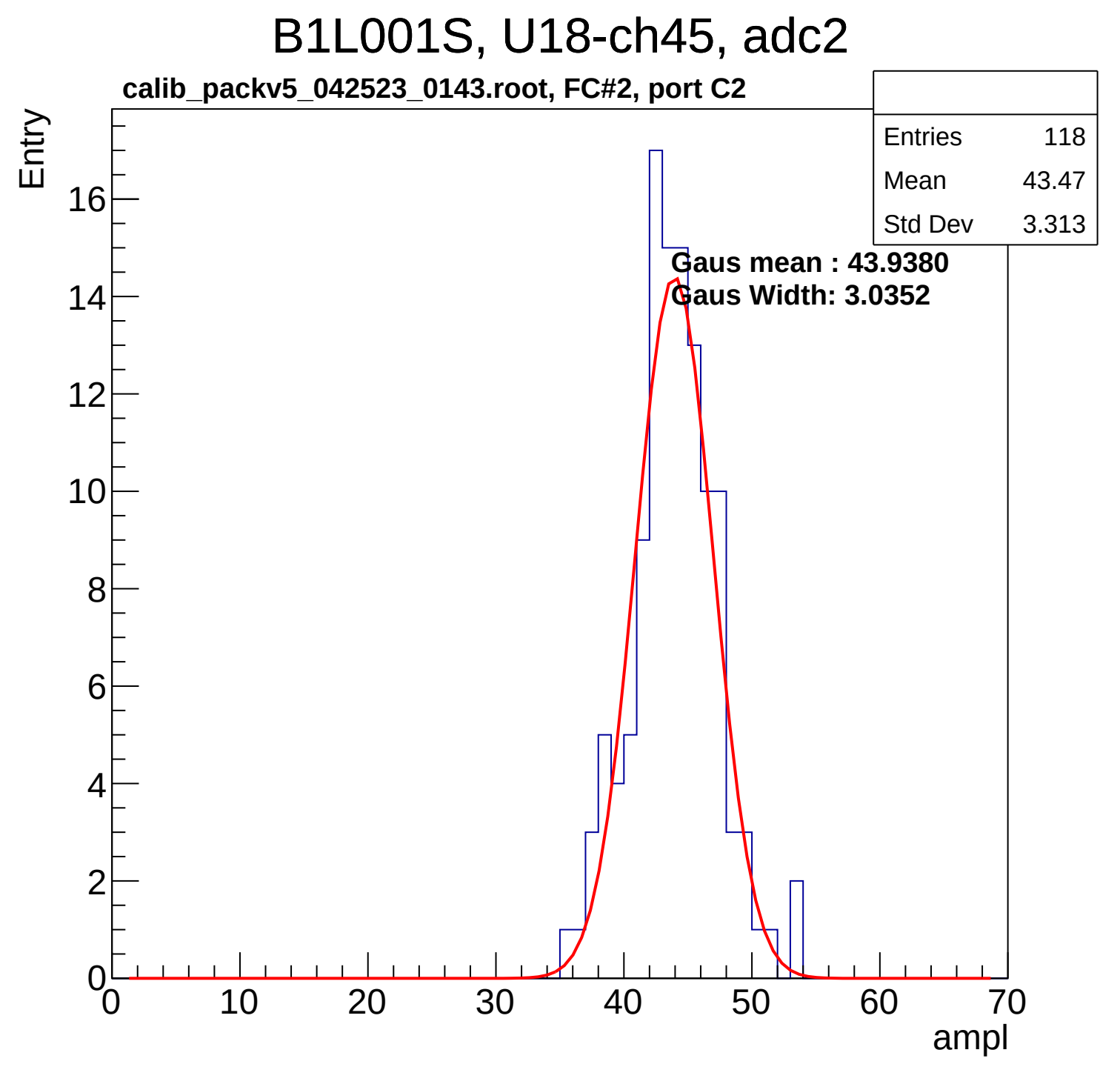

B1L001S, U18-ch44, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 98
Mean 58.29
Std Dev 8.836
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

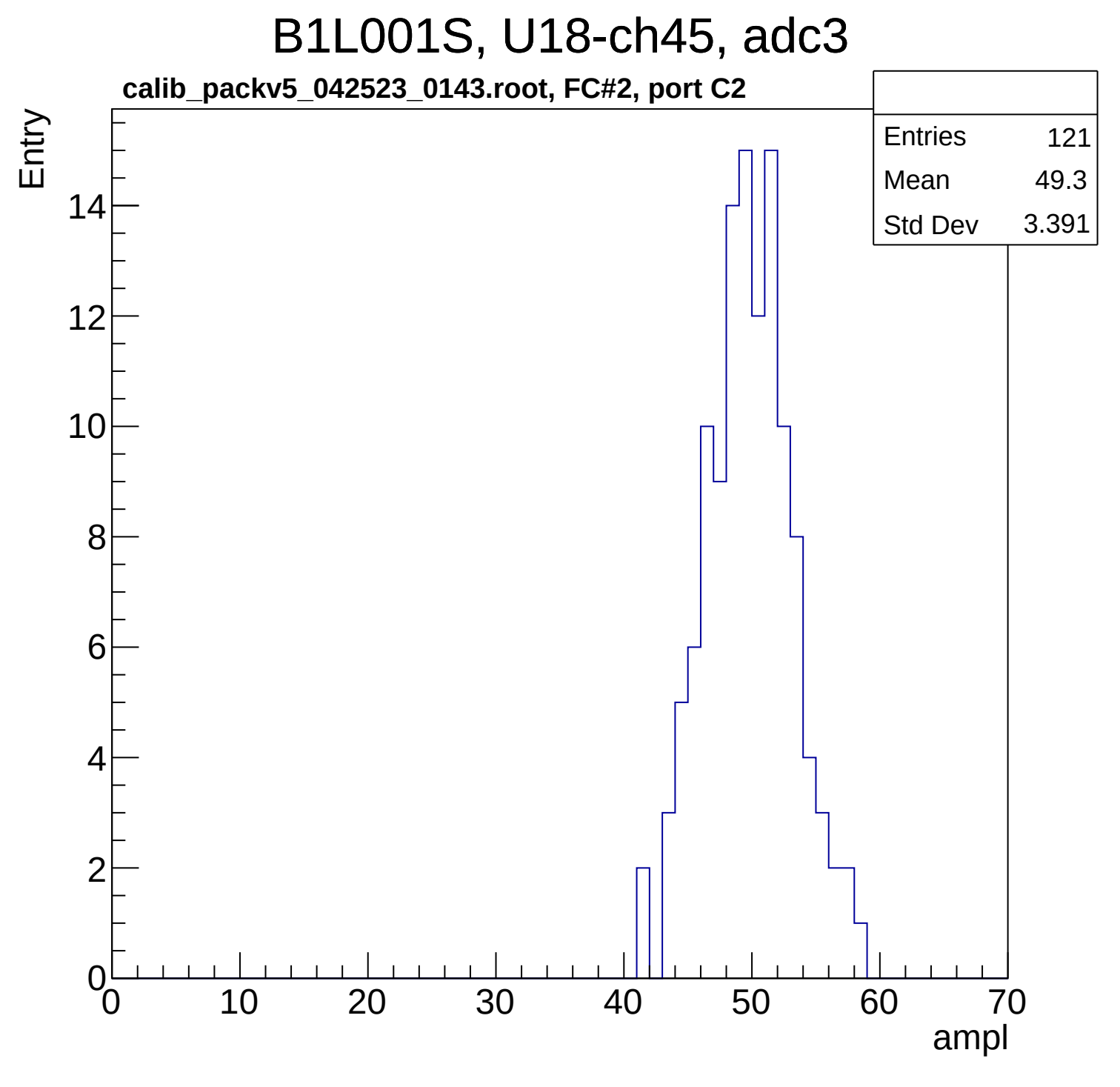

B1L001S, U18-ch44, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 19
Mean 61.42
Std Dev 1.389
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

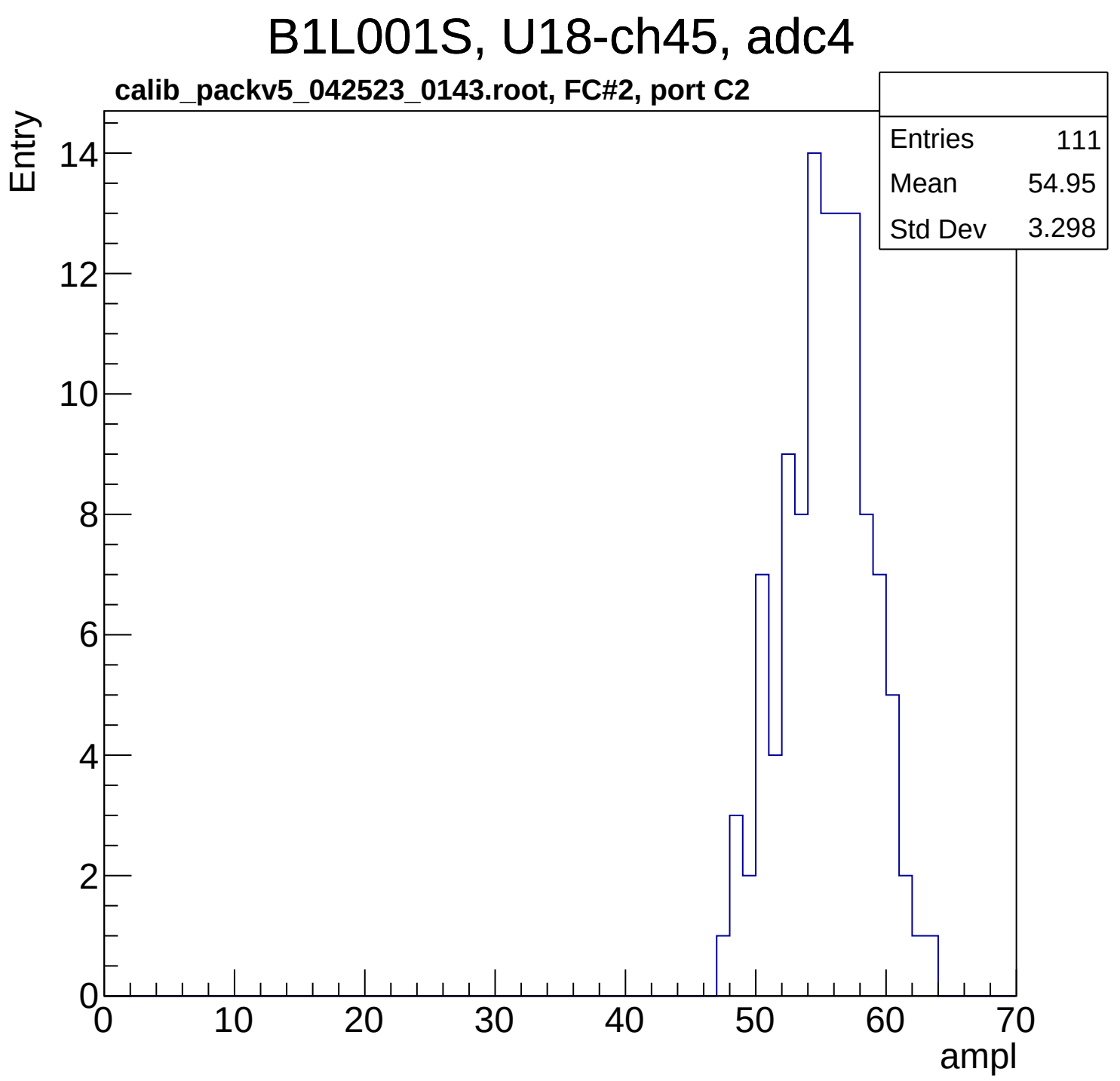

B1L001S, U18-ch44, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 3
Mean 62
Std Dev 1.414
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

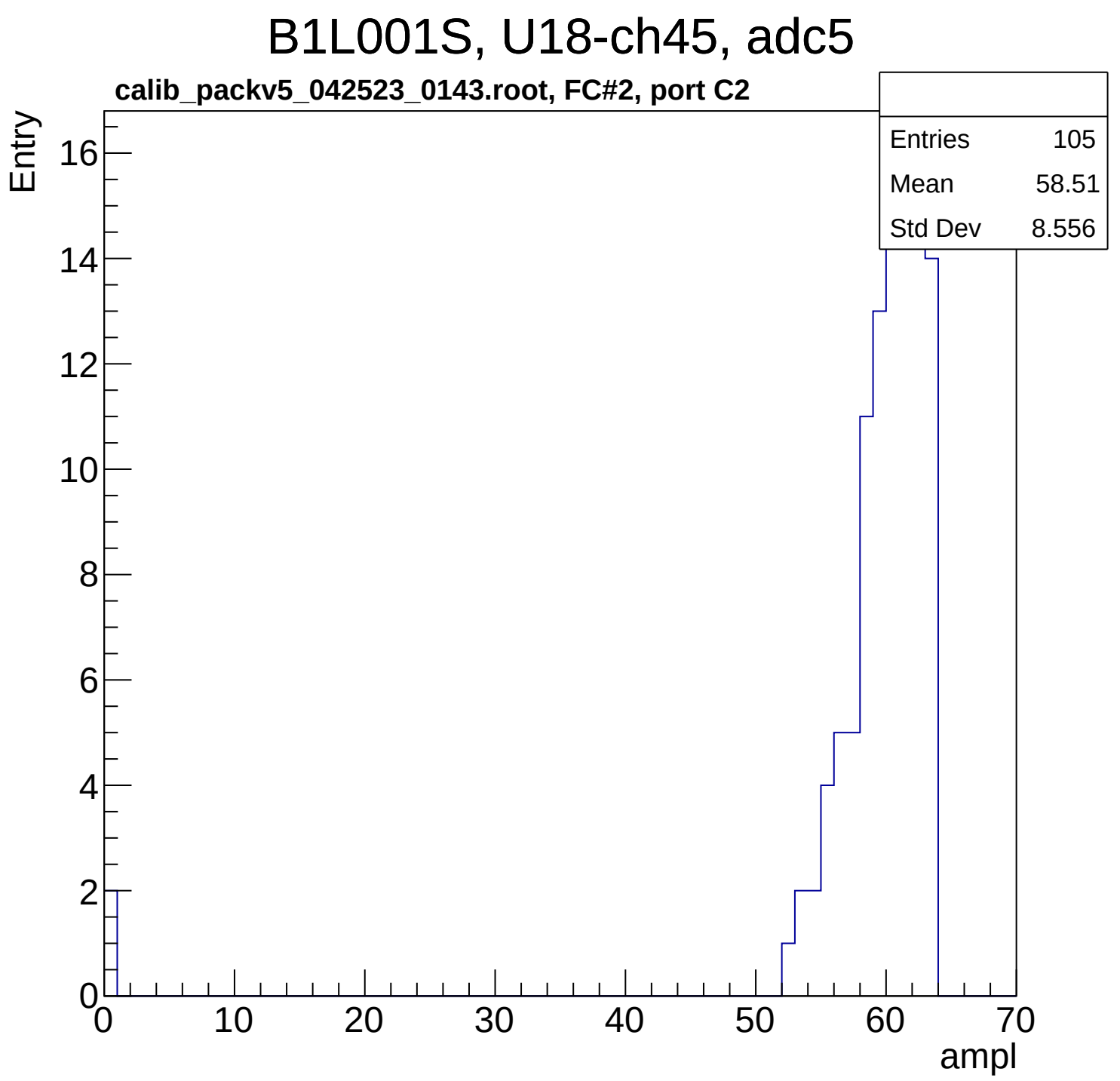

B1L001S, U18-ch45, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 151
Mean 29.15
Std Dev 5.031
Gaus mean : 30.0984
Gaus Width: 3.6540
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

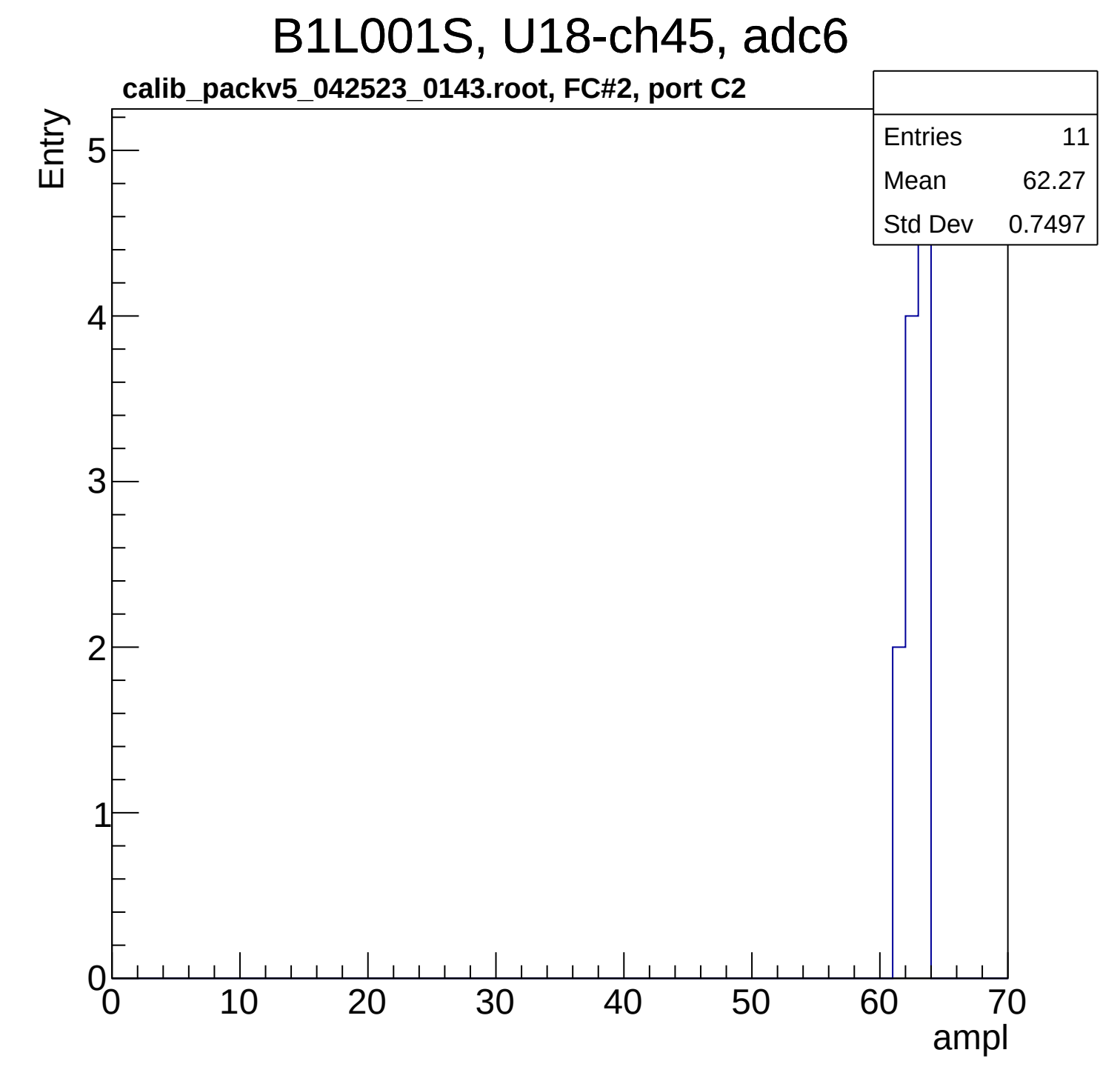

B1L001S, U18-ch45, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 138
Mean 36.83
Std Dev 3.106
Gaus mean : 37.4180
Gaus Width: 3.2040
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

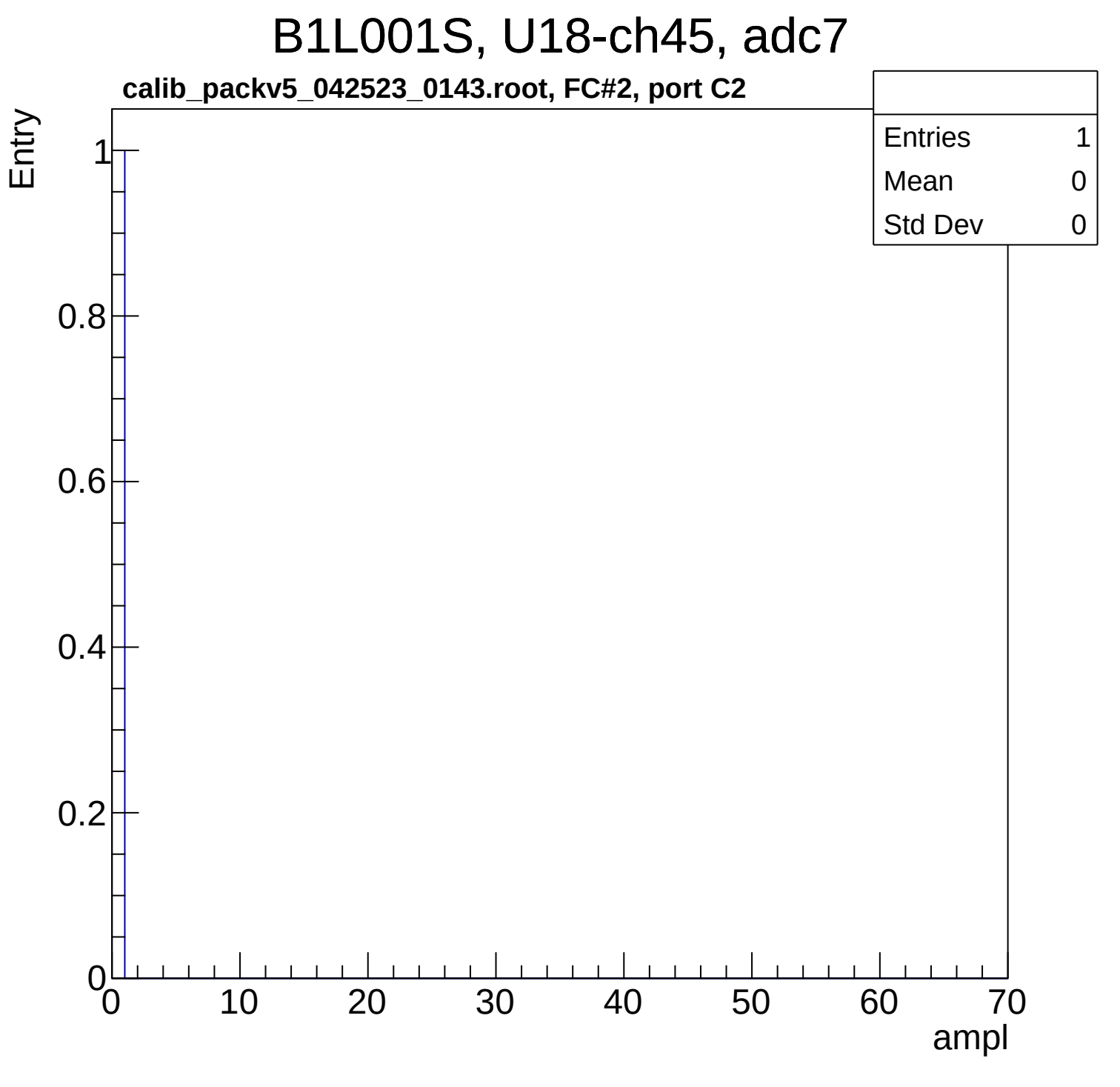

B1L001S, U18-ch45, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 118
Mean 43.47
Std Dev 3.313
Gaus mean : 43.9380
Gaus Width: 3.0352
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

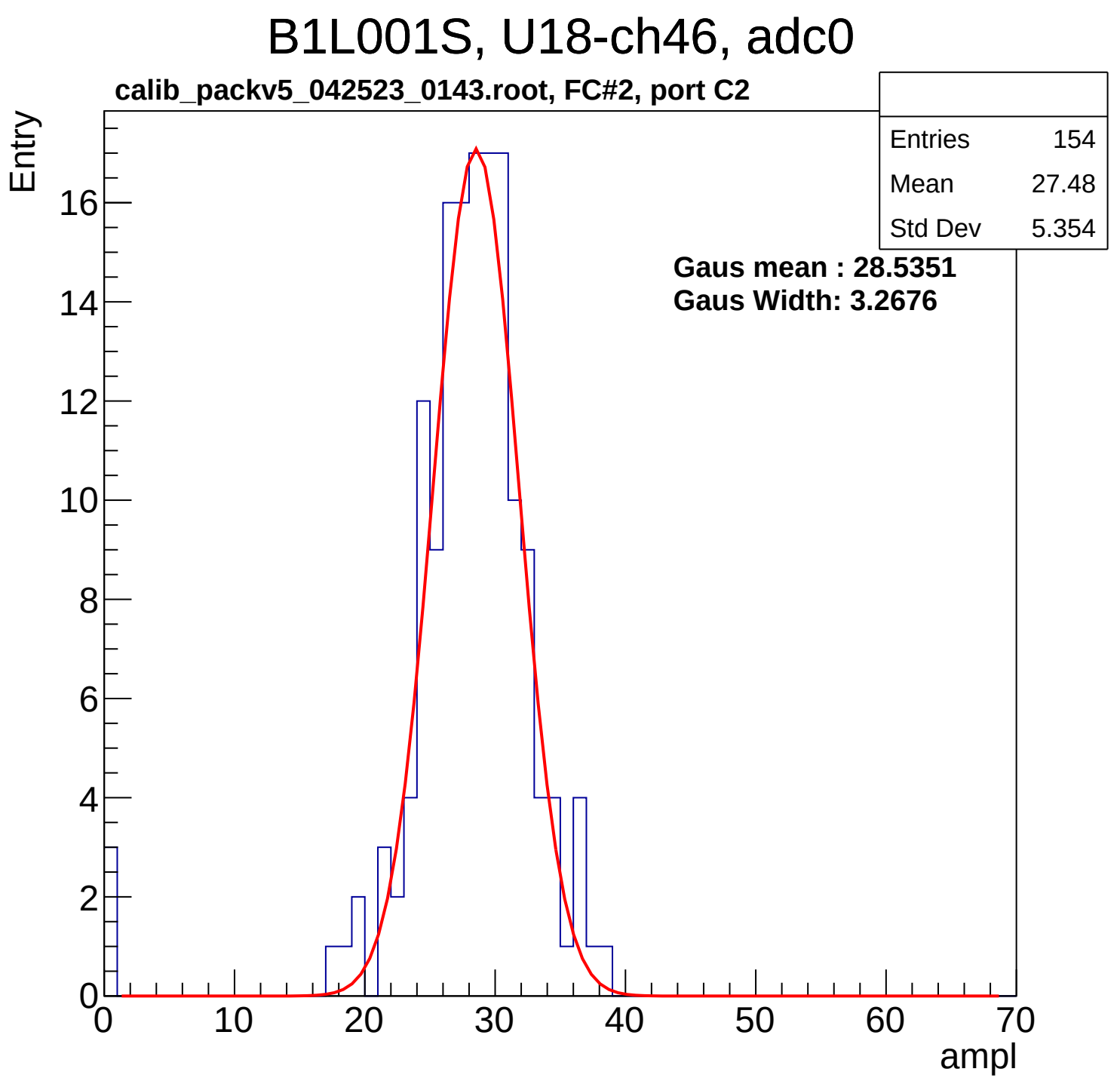

B1L001S, U18-ch45, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 121
Mean 49.3
Std Dev 3.391
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl

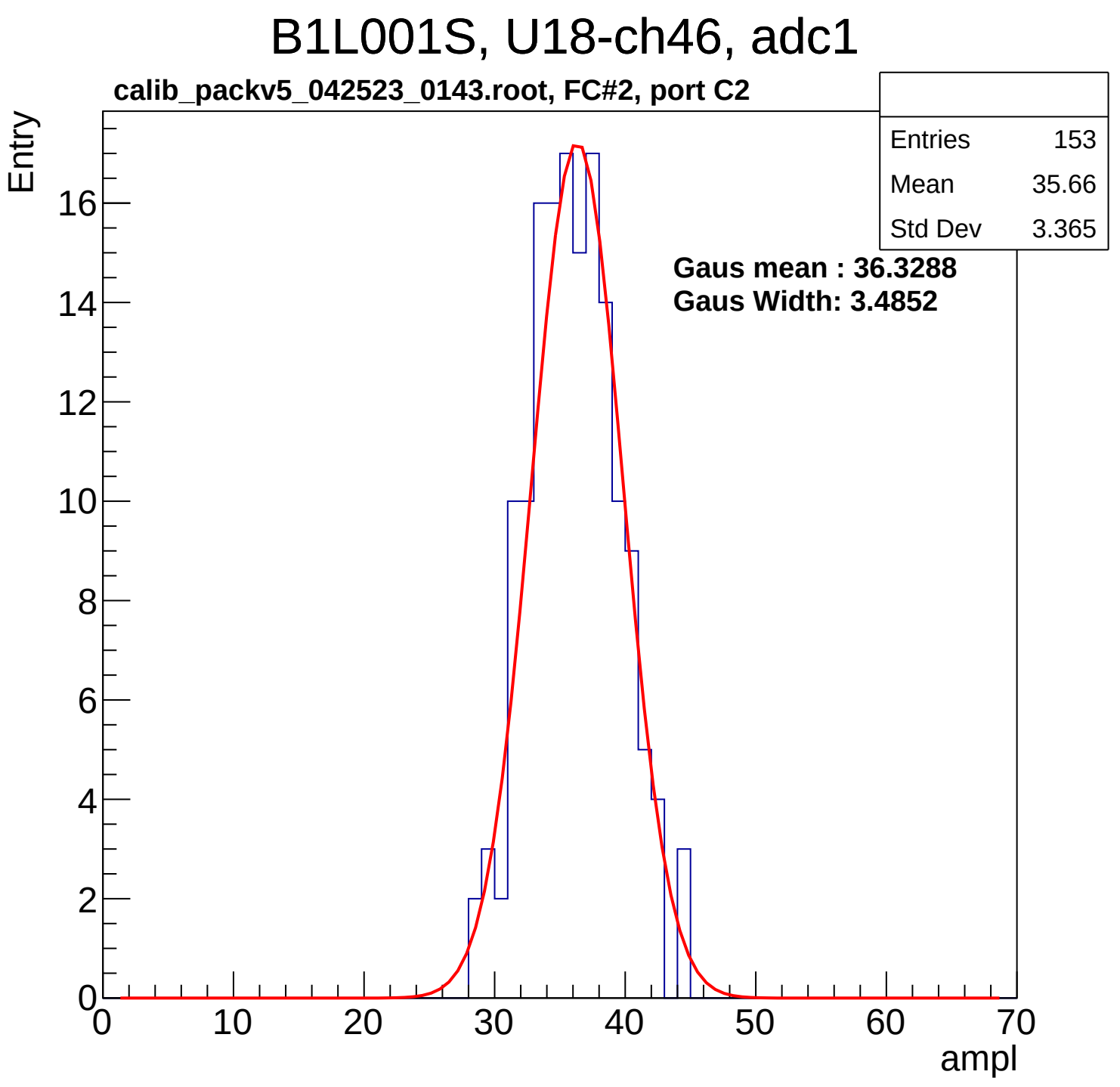

B1L001S, U18-ch45, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 111
Mean 54.95
Std Dev 3.298
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

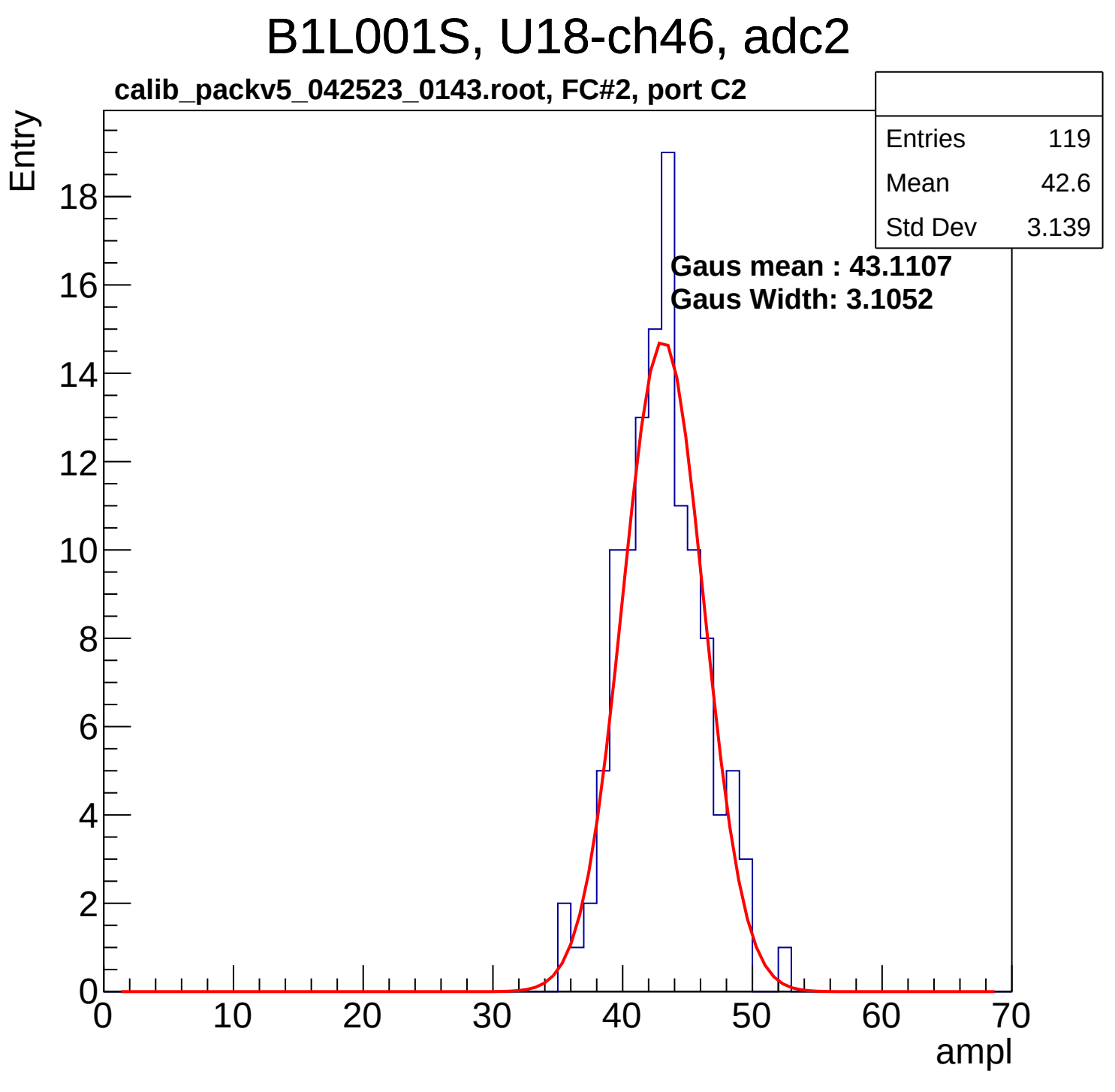

B1L001S, U18-ch45, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 105
Mean 58.51
Std Dev 8.556
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

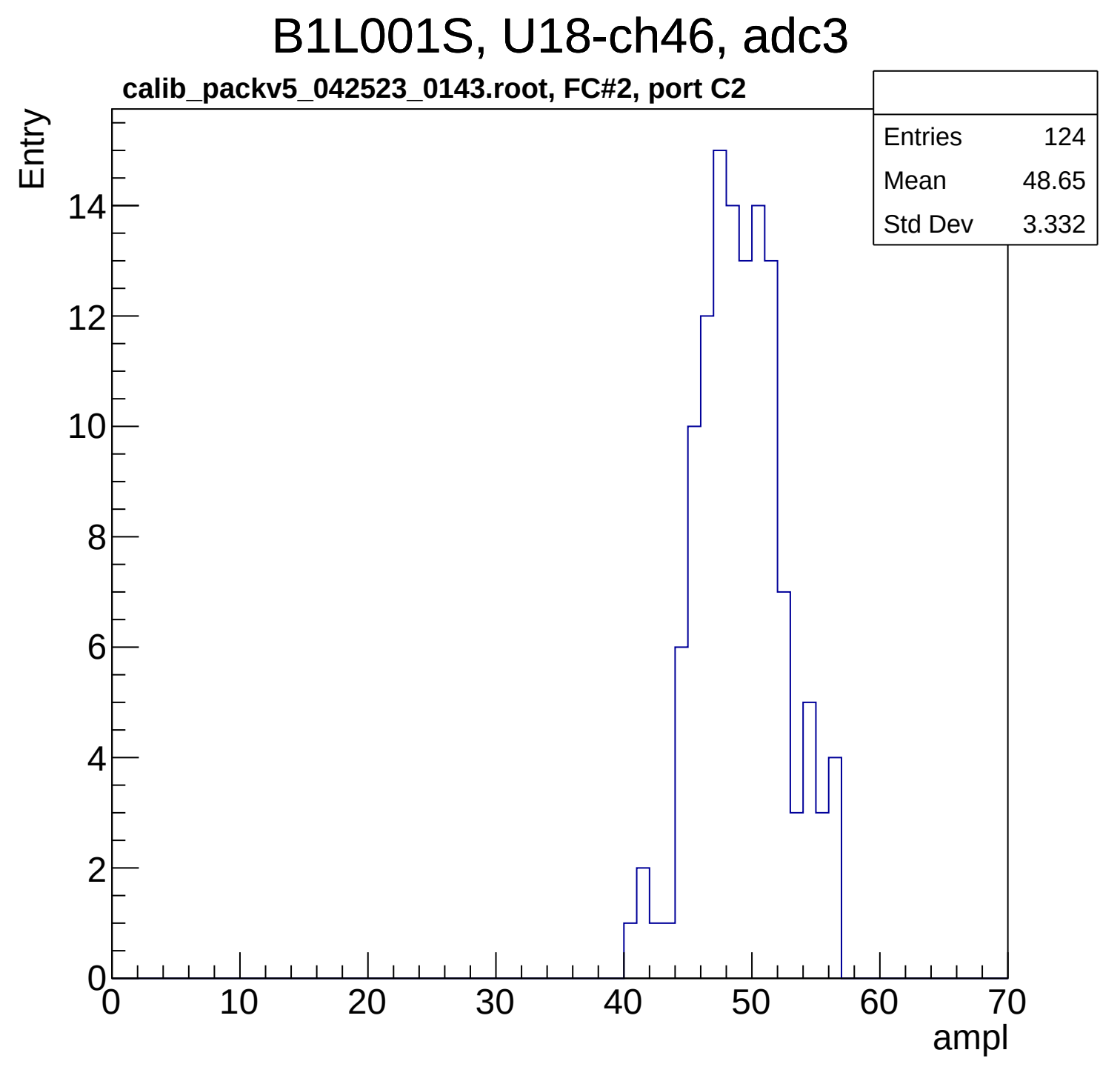

B1L001S, U18-ch45, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 11
Mean 62.27
Std Dev 0.7497
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

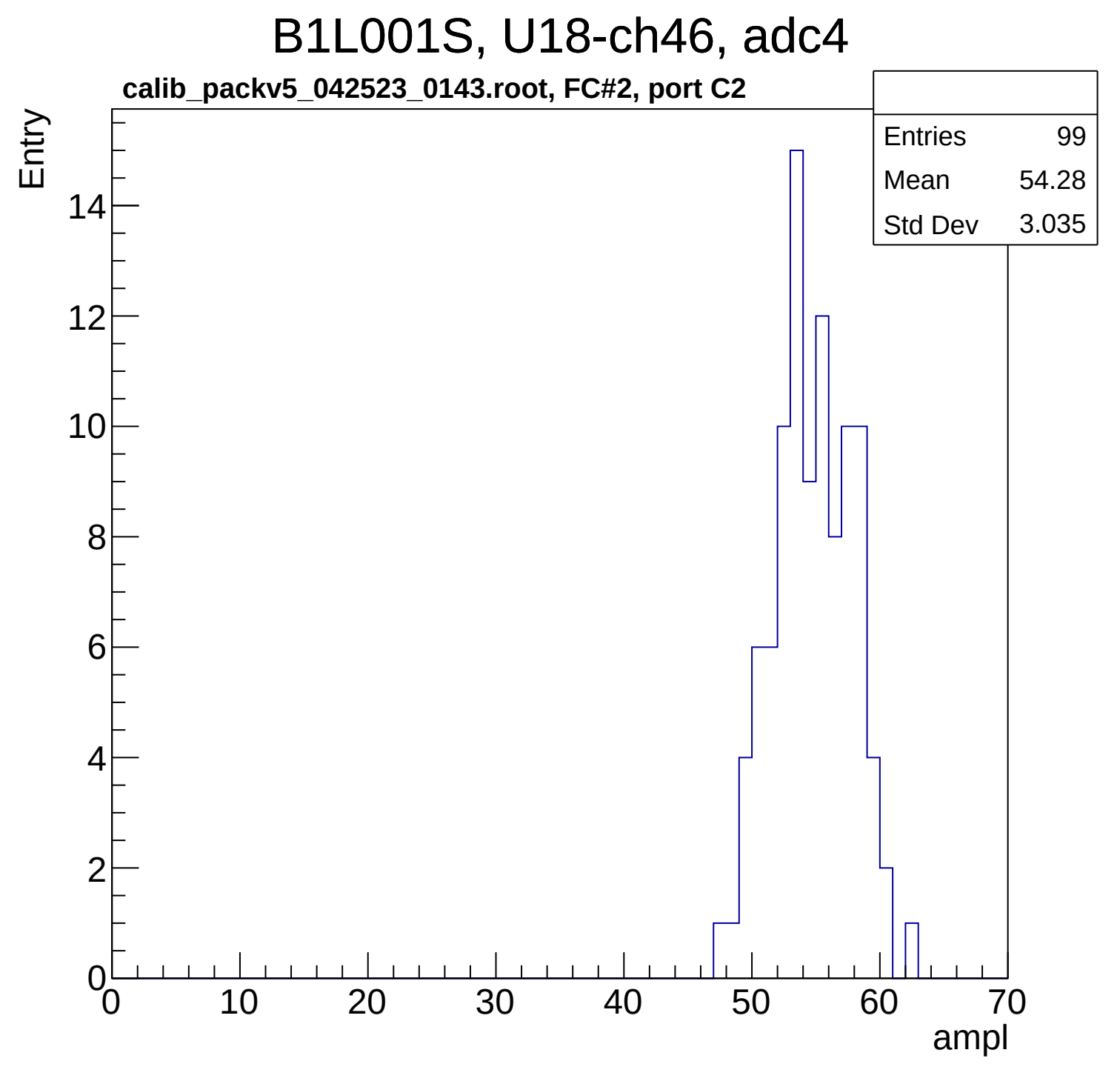

B1L001S, U18-ch45, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

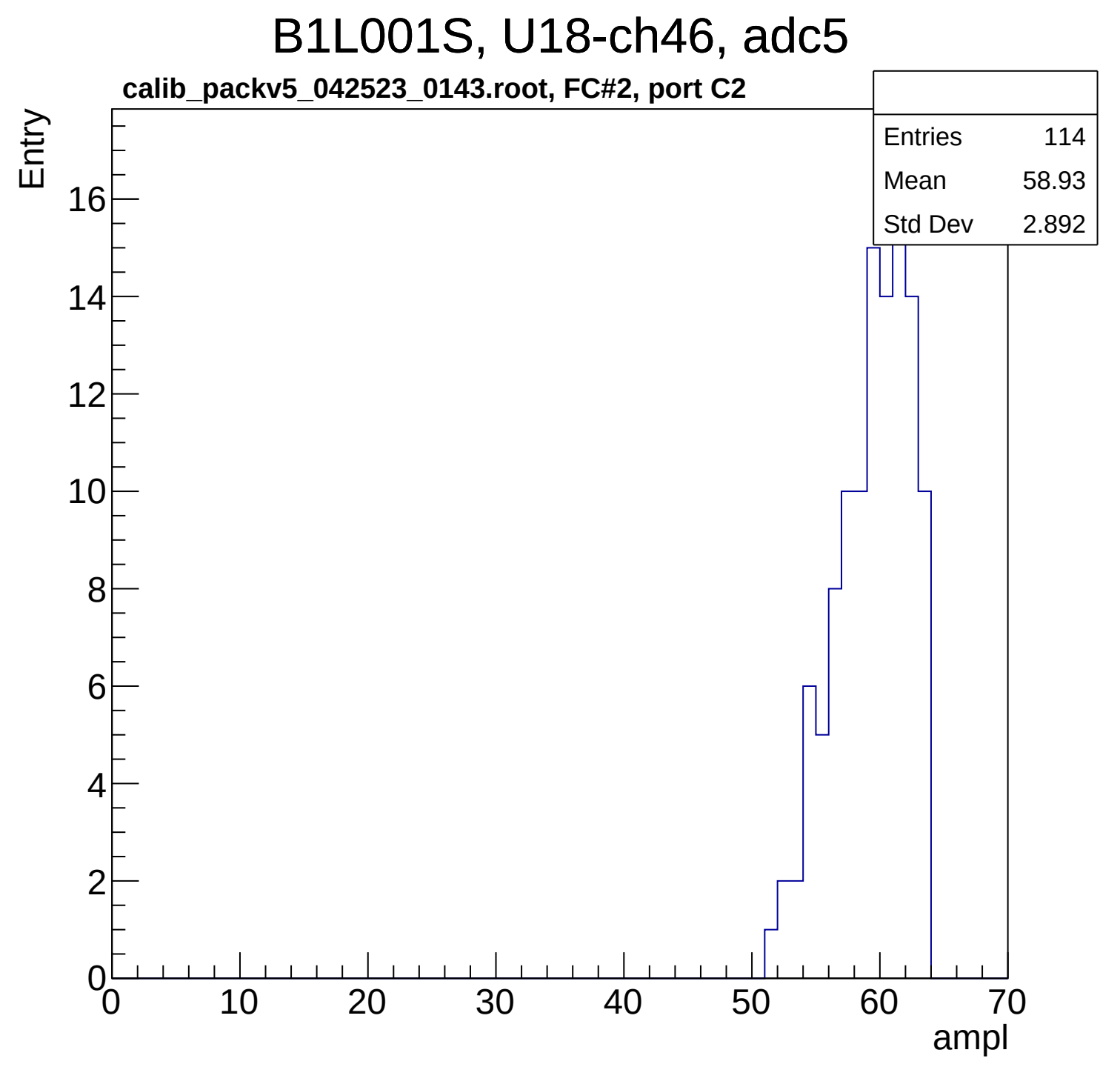

B1L001S, U18-ch46, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 154
Mean 27.48
Std Dev 5.354
Gaus mean : 28.5351
Gaus Width: 3.2676
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

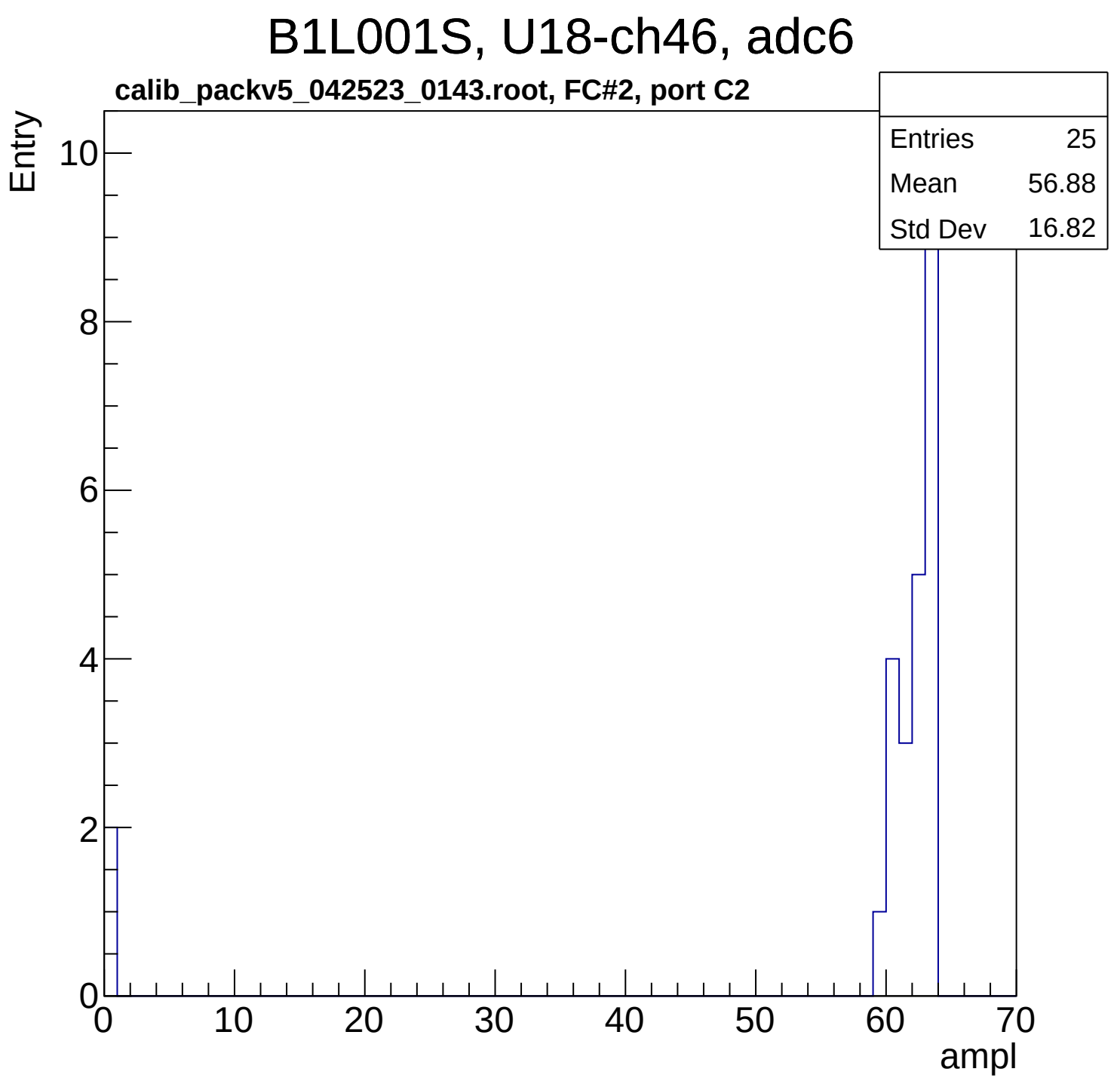

B1L001S, U18-ch46, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 153
Mean 35.66
Std Dev 3.365
Gaus mean : 36.3288
Gaus Width: 3.4852
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

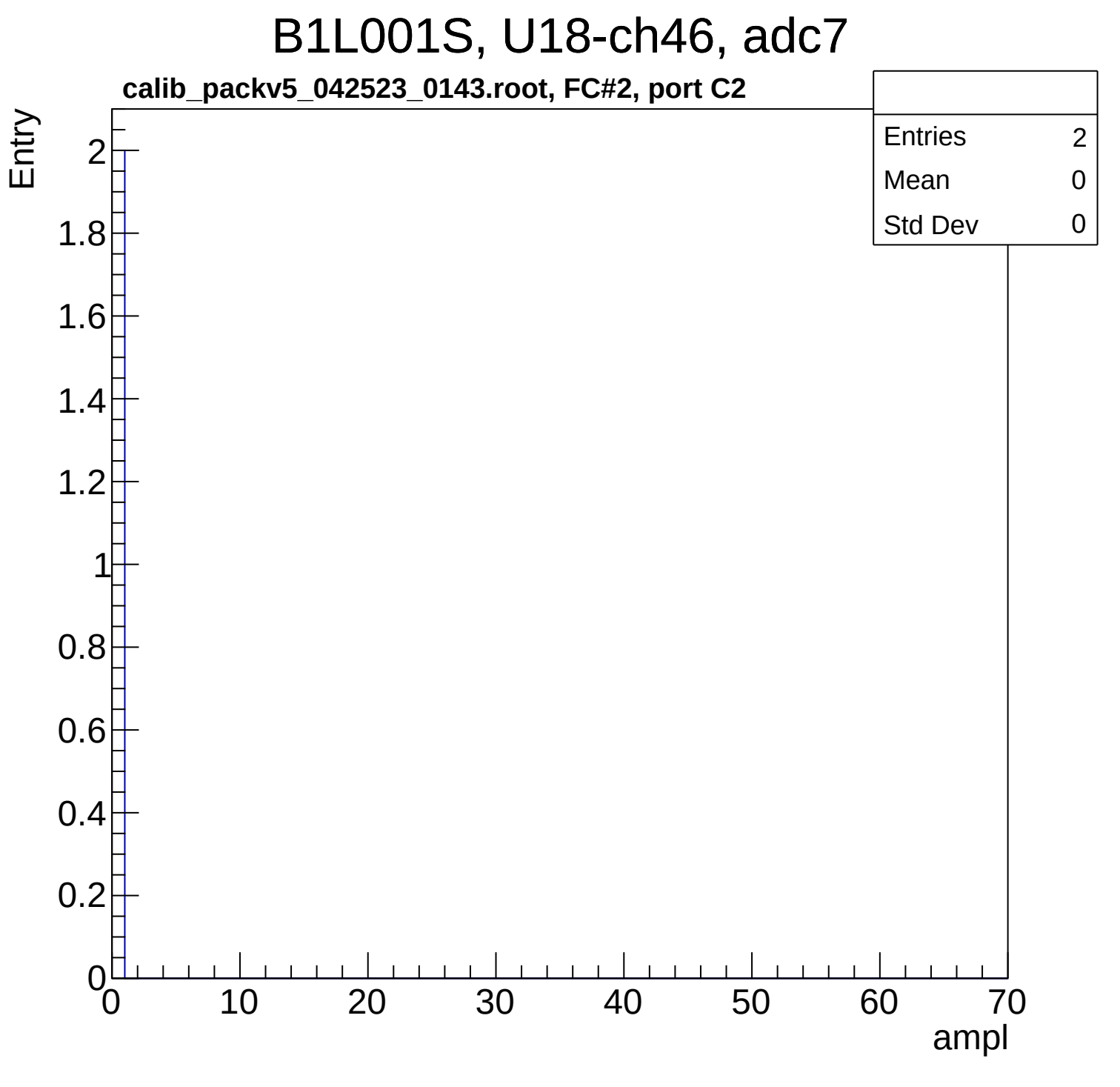

B1L001S, U18-ch46, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 119
Mean 42.6
Std Dev 3.139
Gaus mean : 43.1107
Gaus Width: 3.1052
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

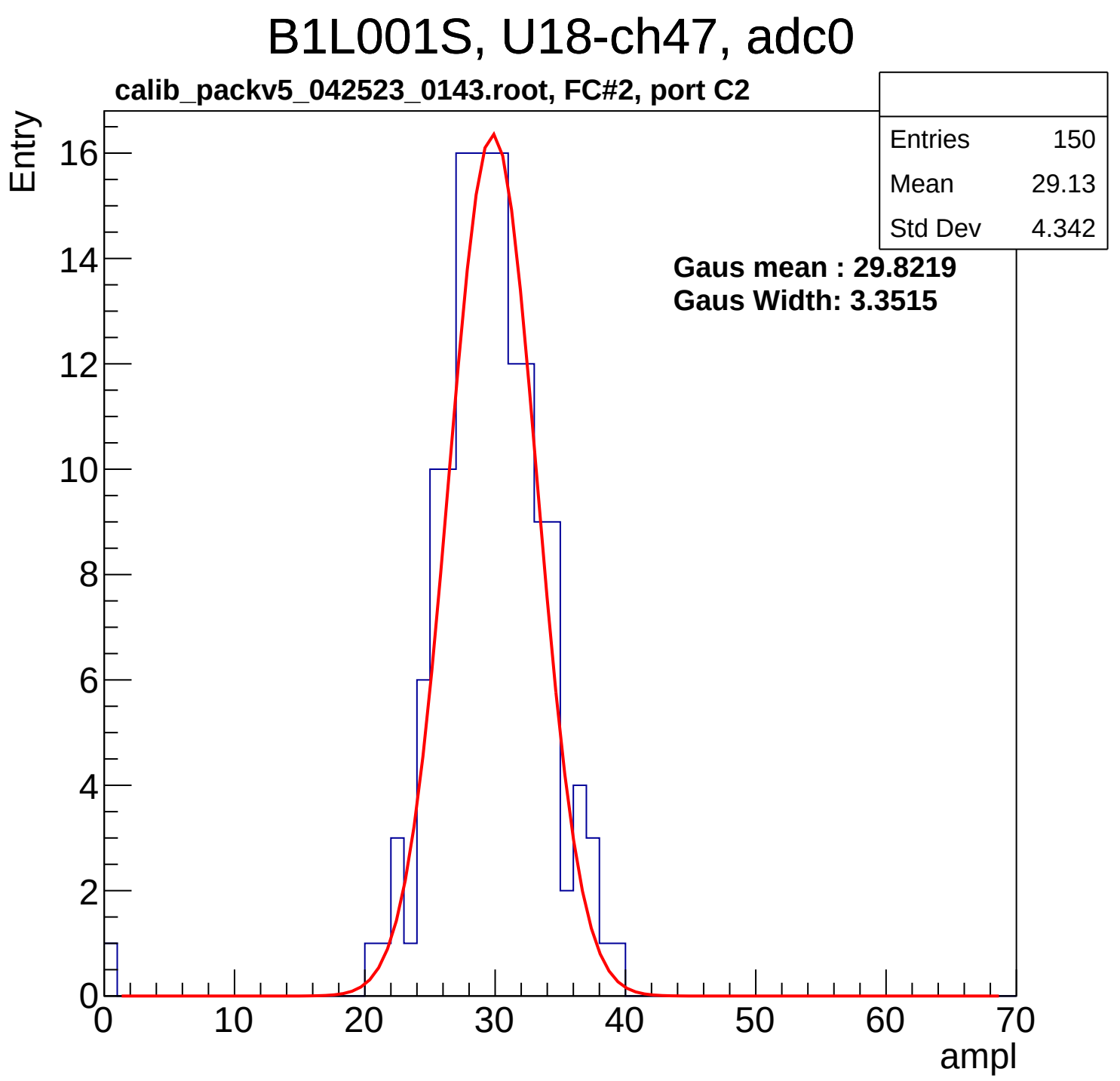

B1L001S, U18-ch46, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 124
Mean 48.65
Std Dev 3.332
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl

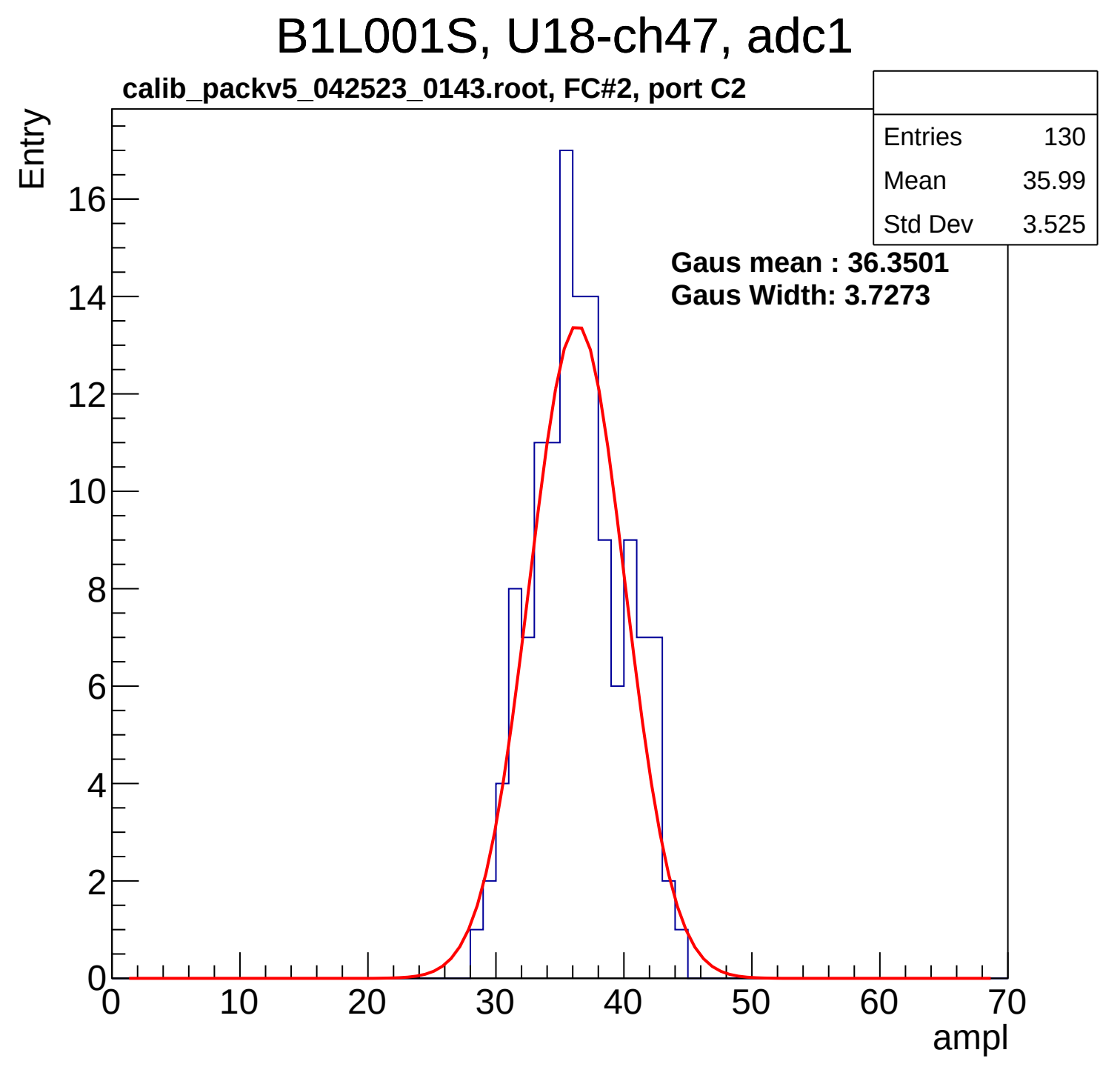

B1L001S, U18-ch46, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 99
Mean 54.28
Std Dev 3.035
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl

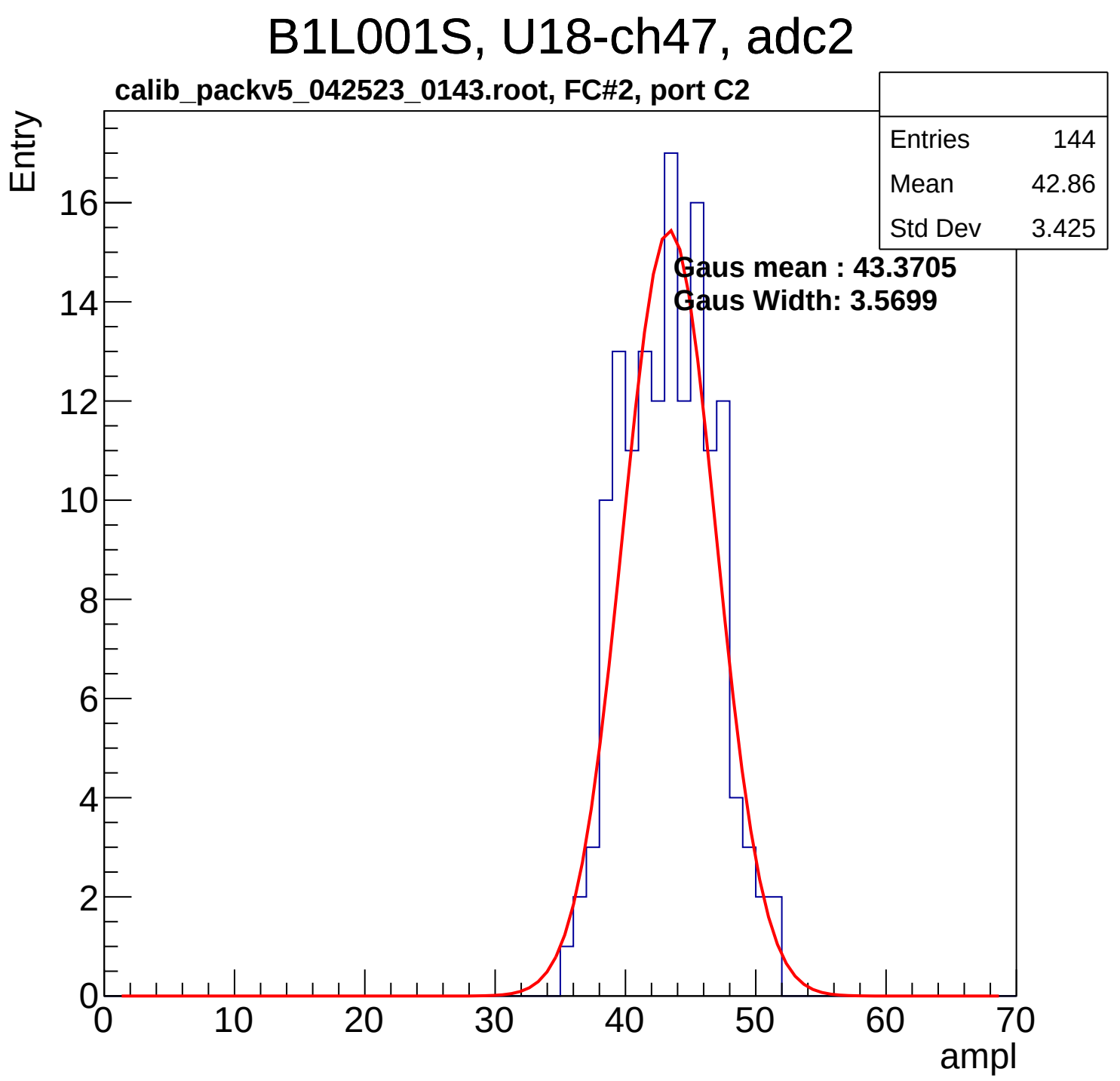

B1L001S, U18-ch46, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 114
Mean 58.93
Std Dev 2.892
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

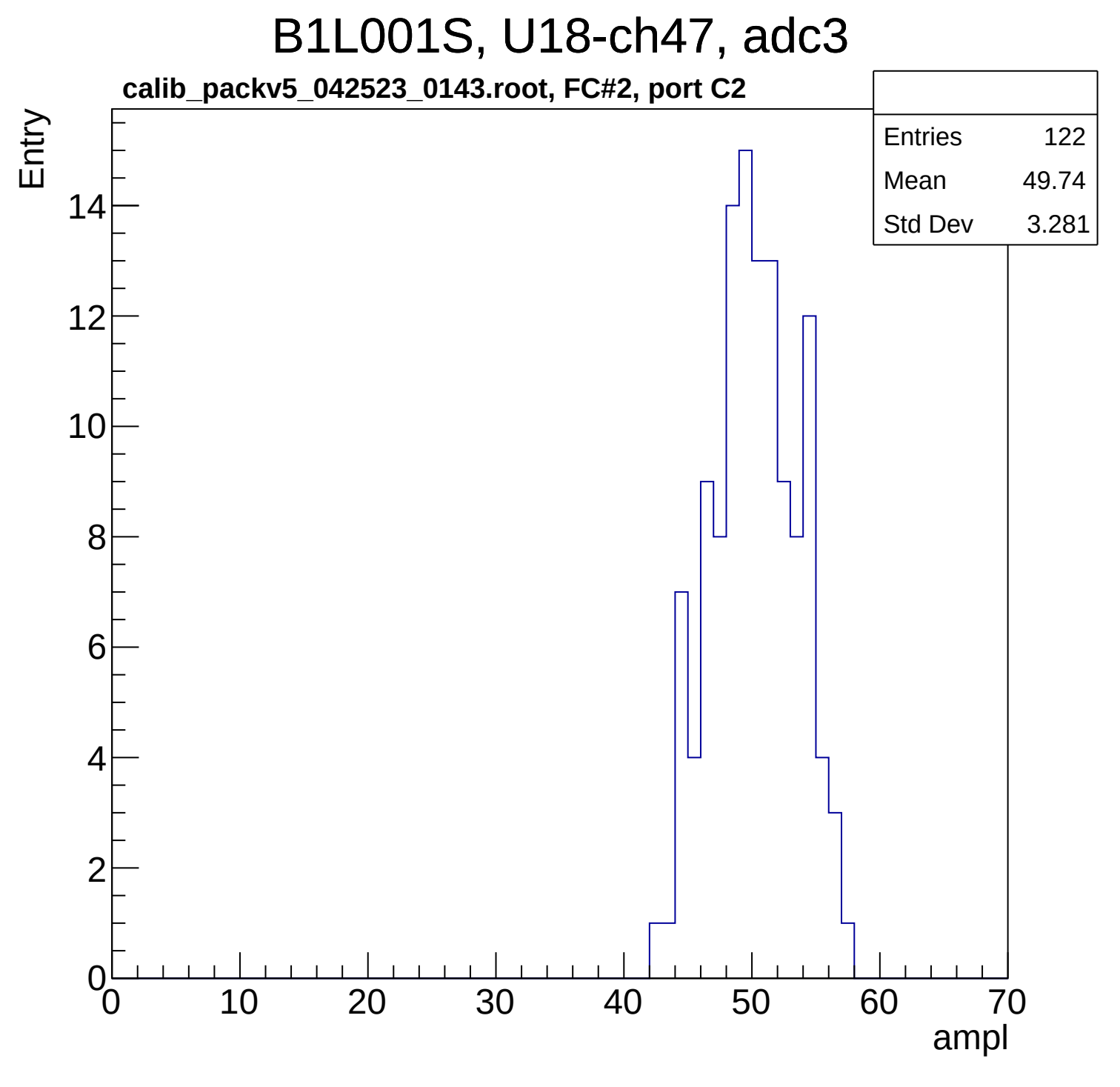

B1L001S, U18-ch46, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 25
Mean 56.88
Std Dev 16.82
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

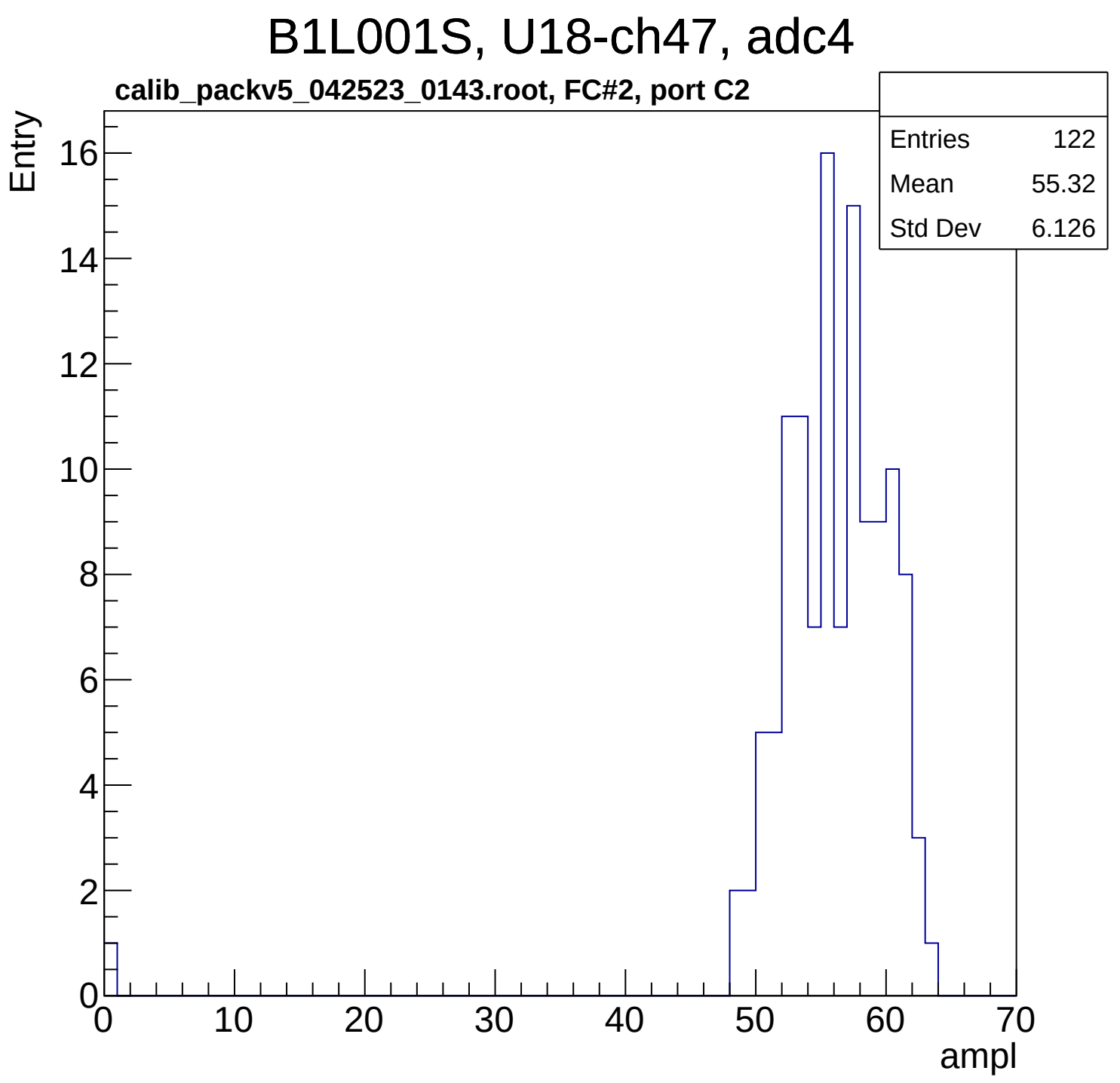

B1L001S, U18-ch46, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 0
Std Dev 0
Entry
2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

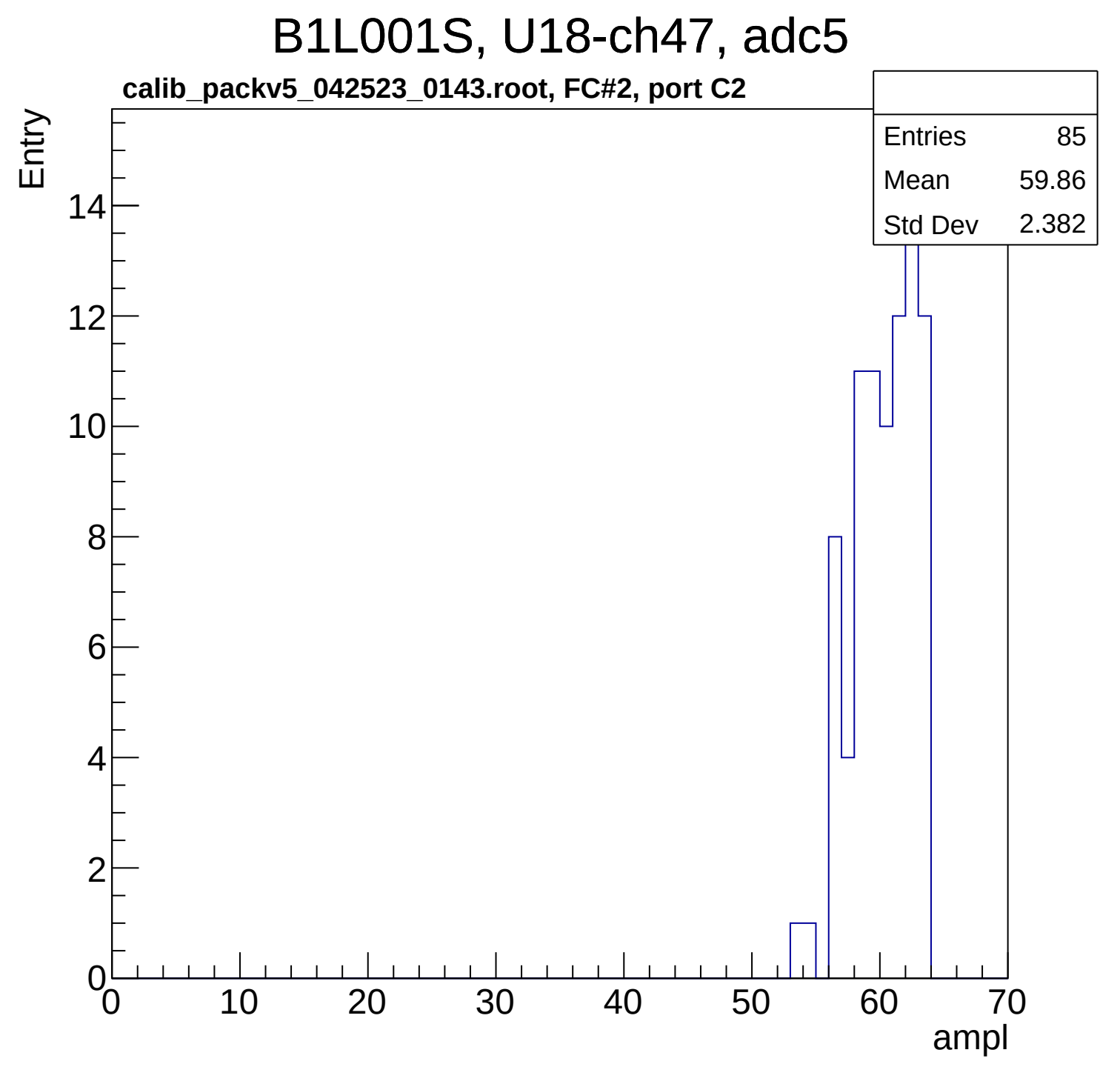

B1L001S, U18-ch47, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 150
Mean 29.13
Std Dev 4.342
Gaus mean : 29.8219
Gaus Width: 3.3515
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

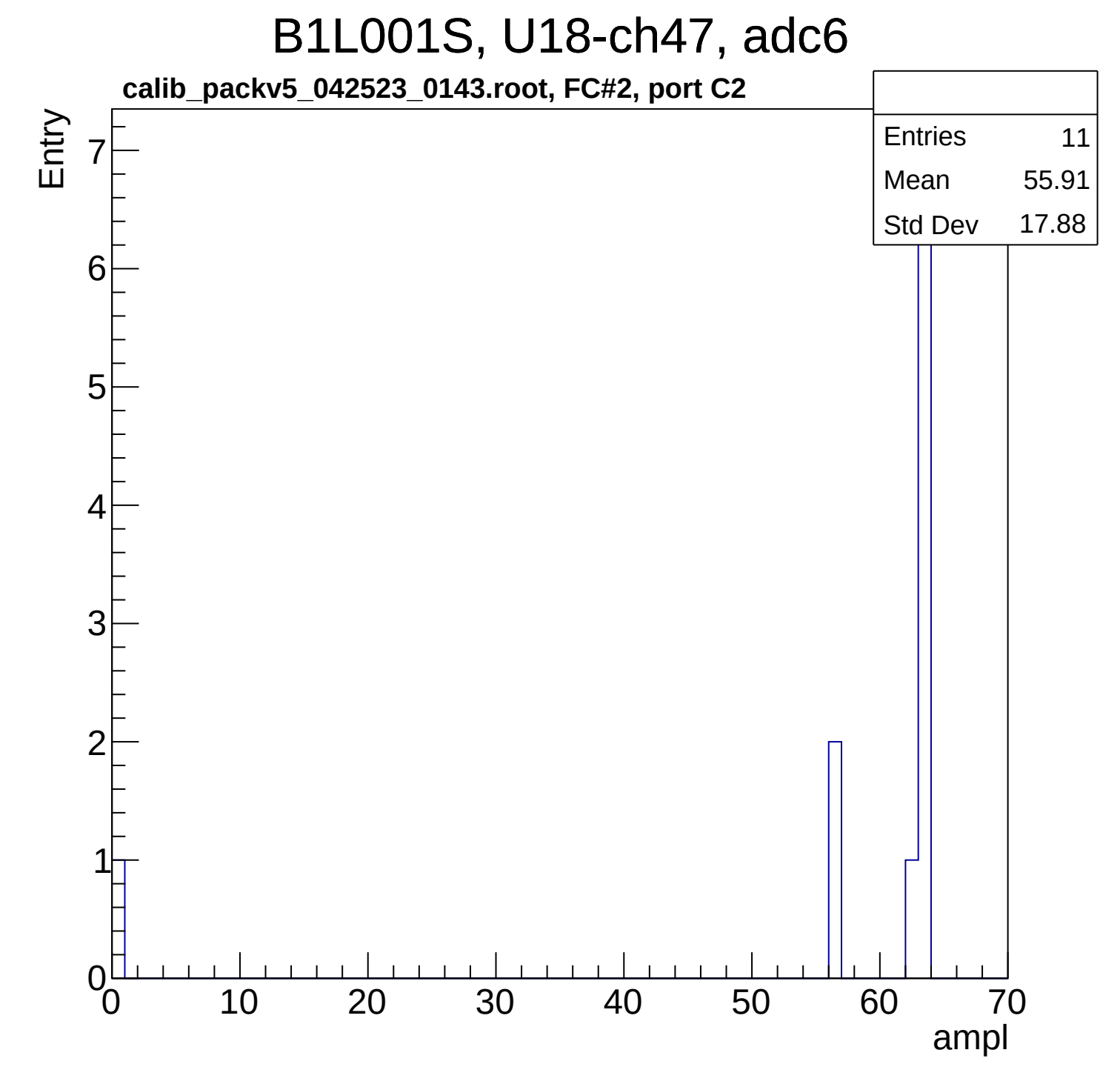

B1L001S, U18-ch47, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 130
Mean 35.99
Std Dev 3.525
Gaus mean : 36.3501
Gaus Width: 3.7273
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

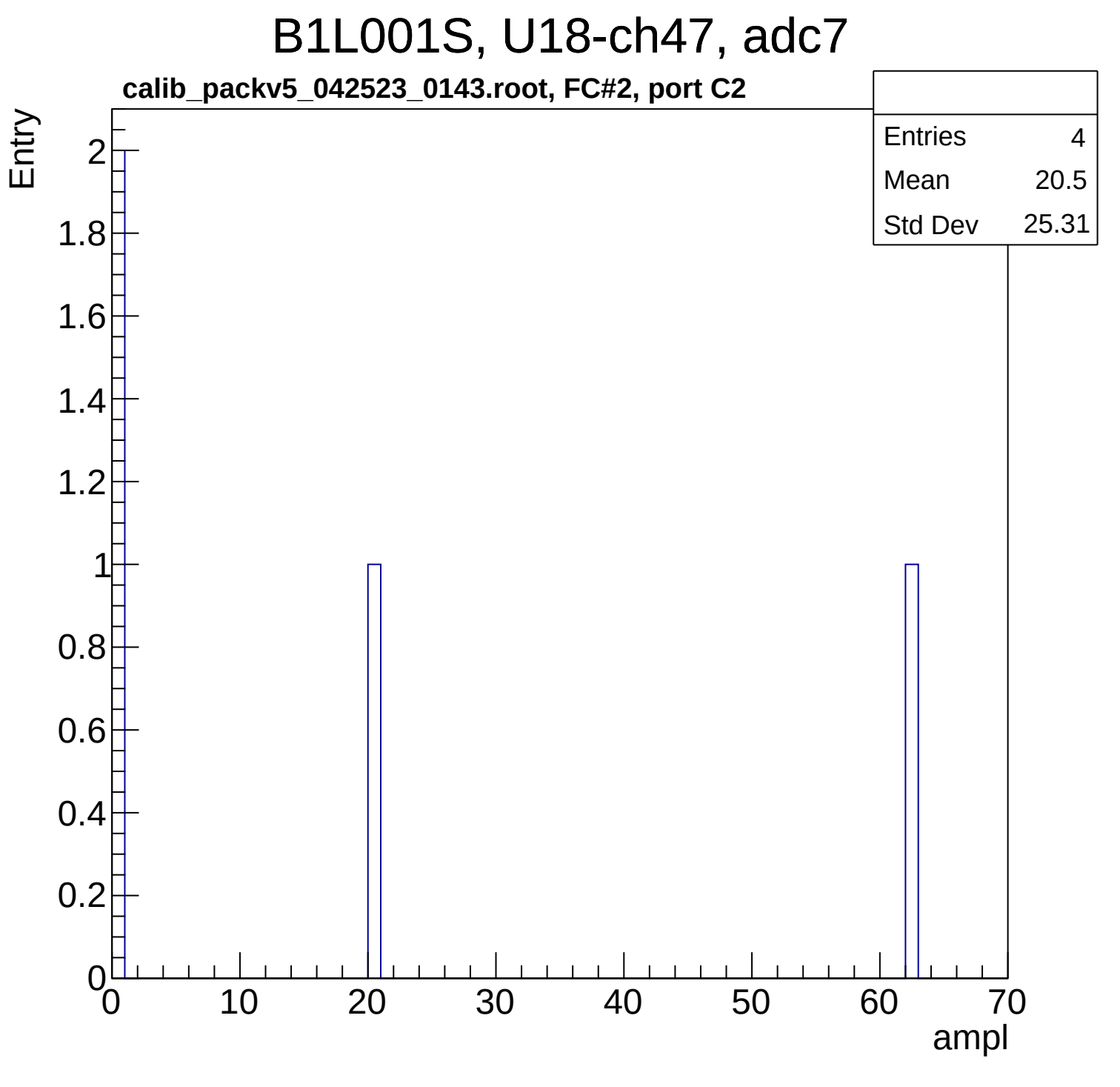

B1L001S, U18-ch47, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 144
Mean 42.86
Std Dev 3.425
Gaus mean : 43.3705
Gaus Width: 3.5699
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

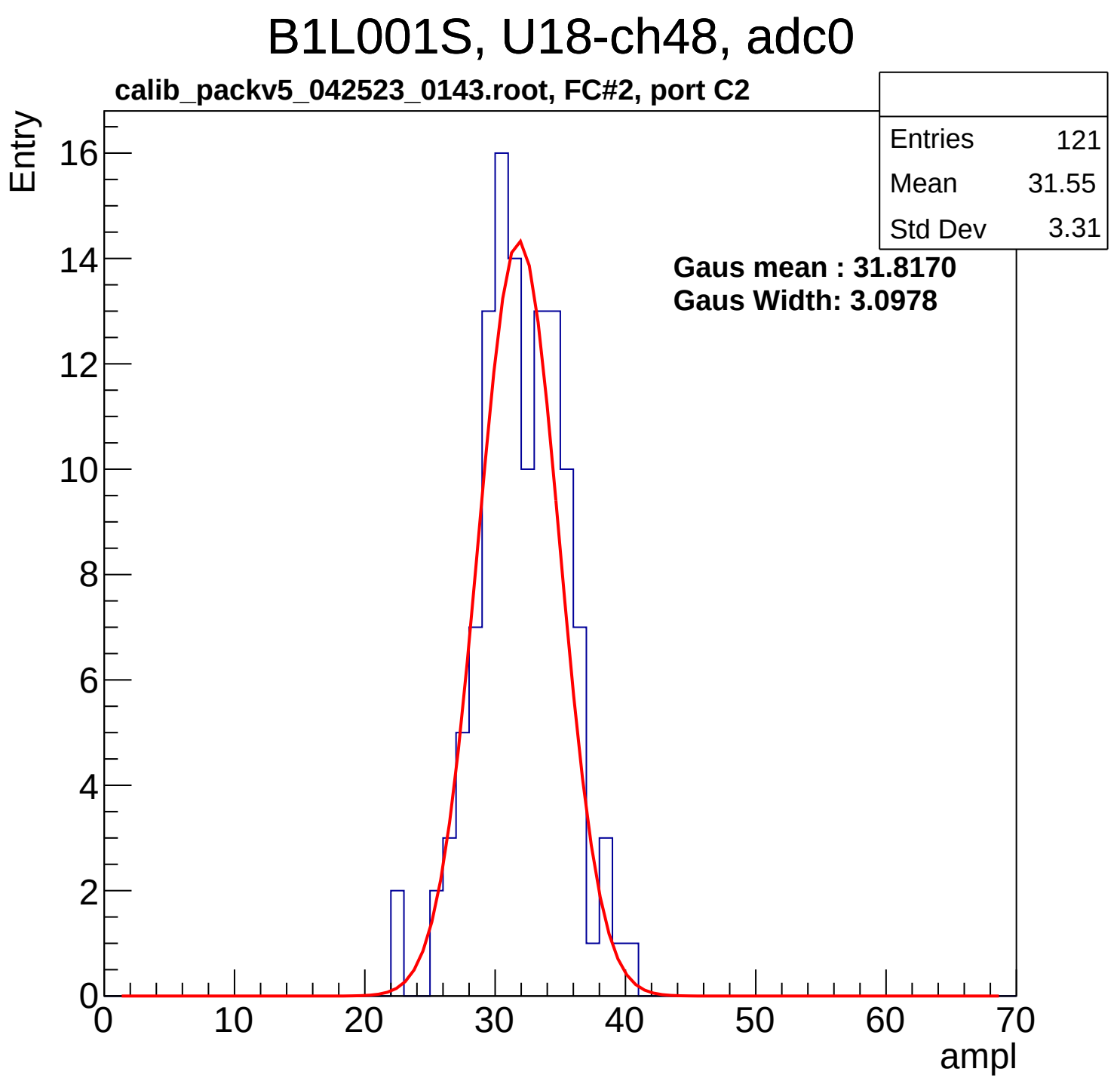

B1L001S, U18-ch47, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 122
Mean 49.74
Std Dev 3.281
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl

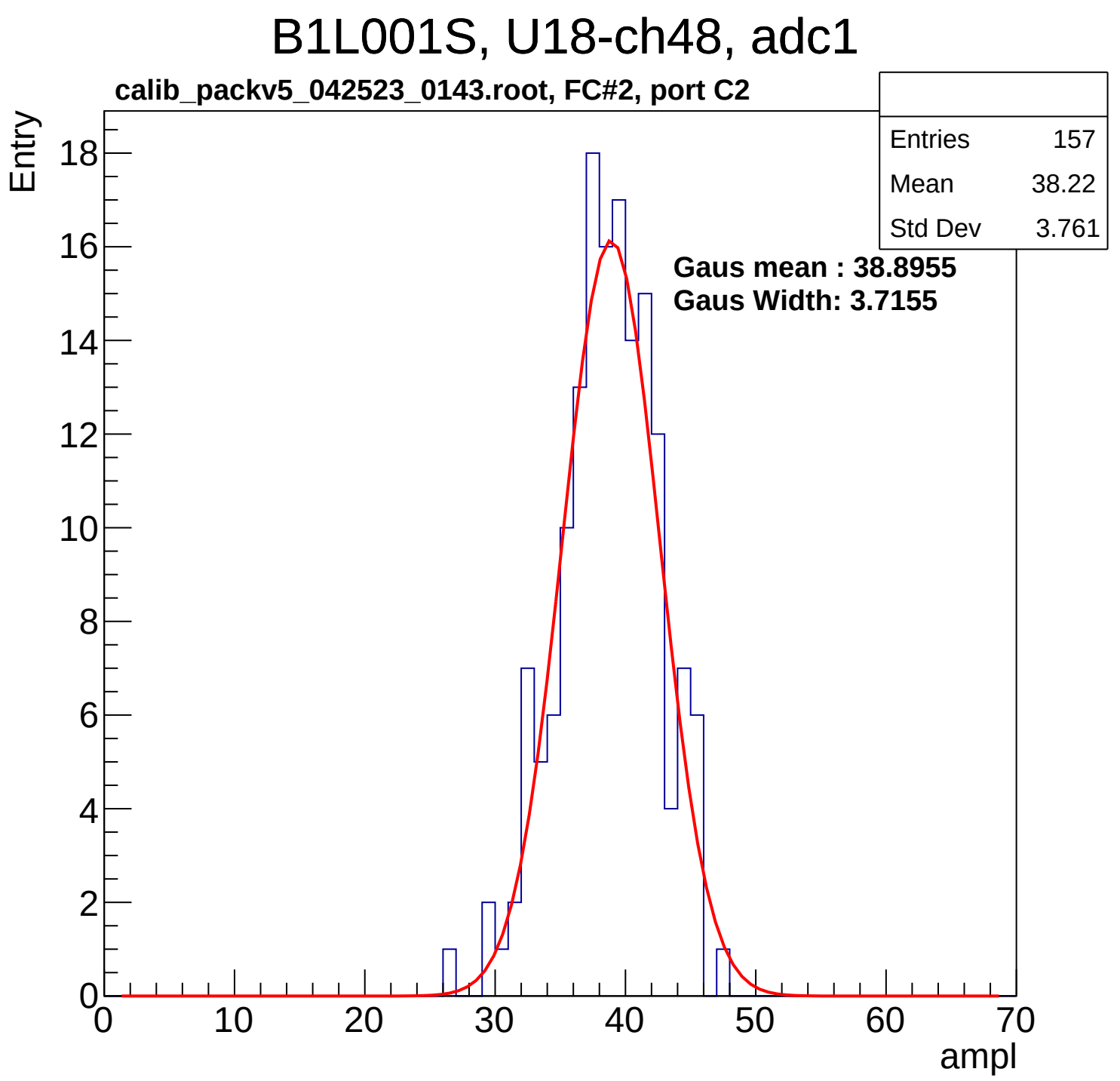

B1L001S, U18-ch47, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 122
Mean 55.32
Std Dev 6.126
Entry
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl

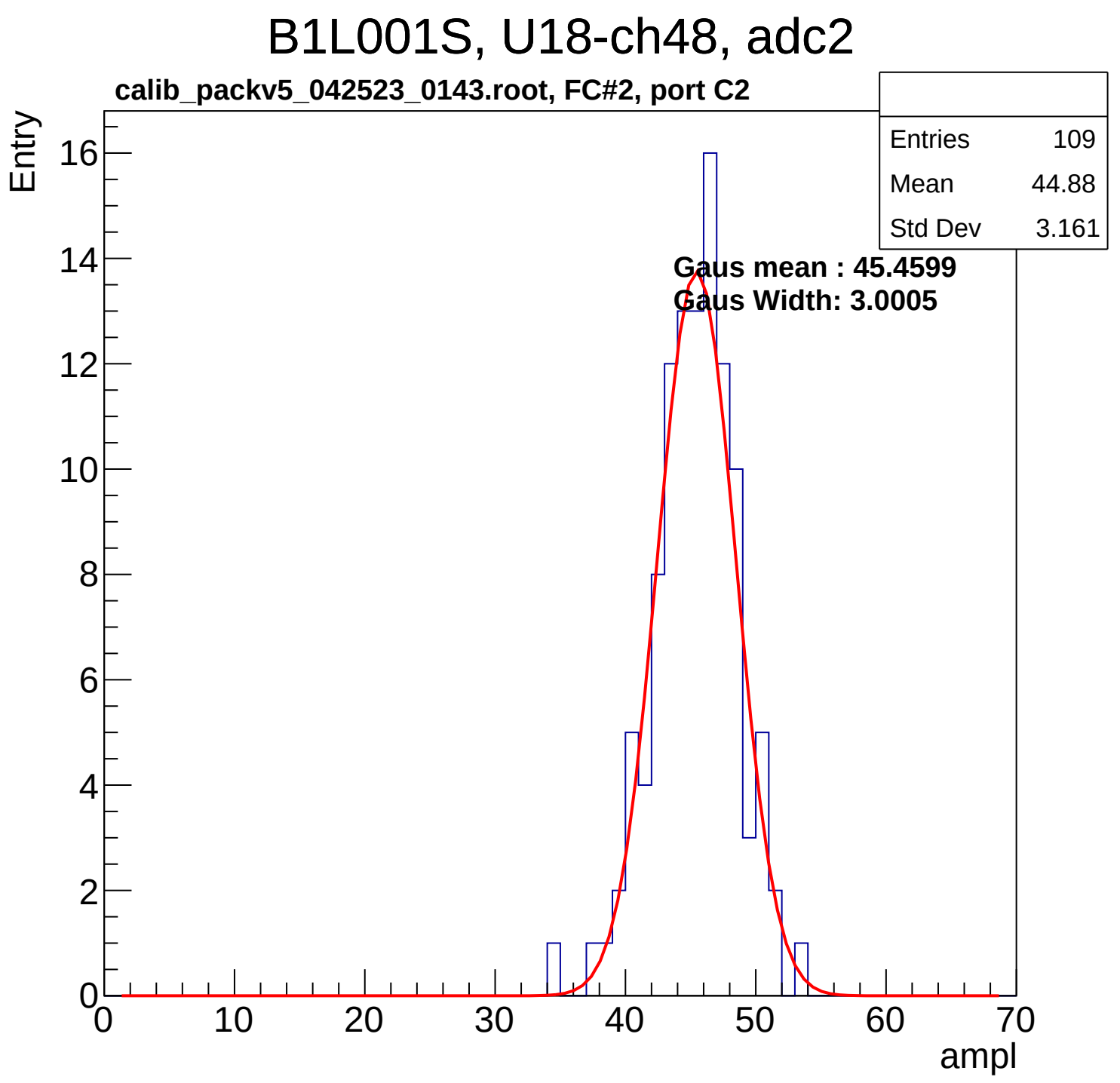

B1L001S, U18-ch47, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 85
Mean 59.86
Std Dev 2.382
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl

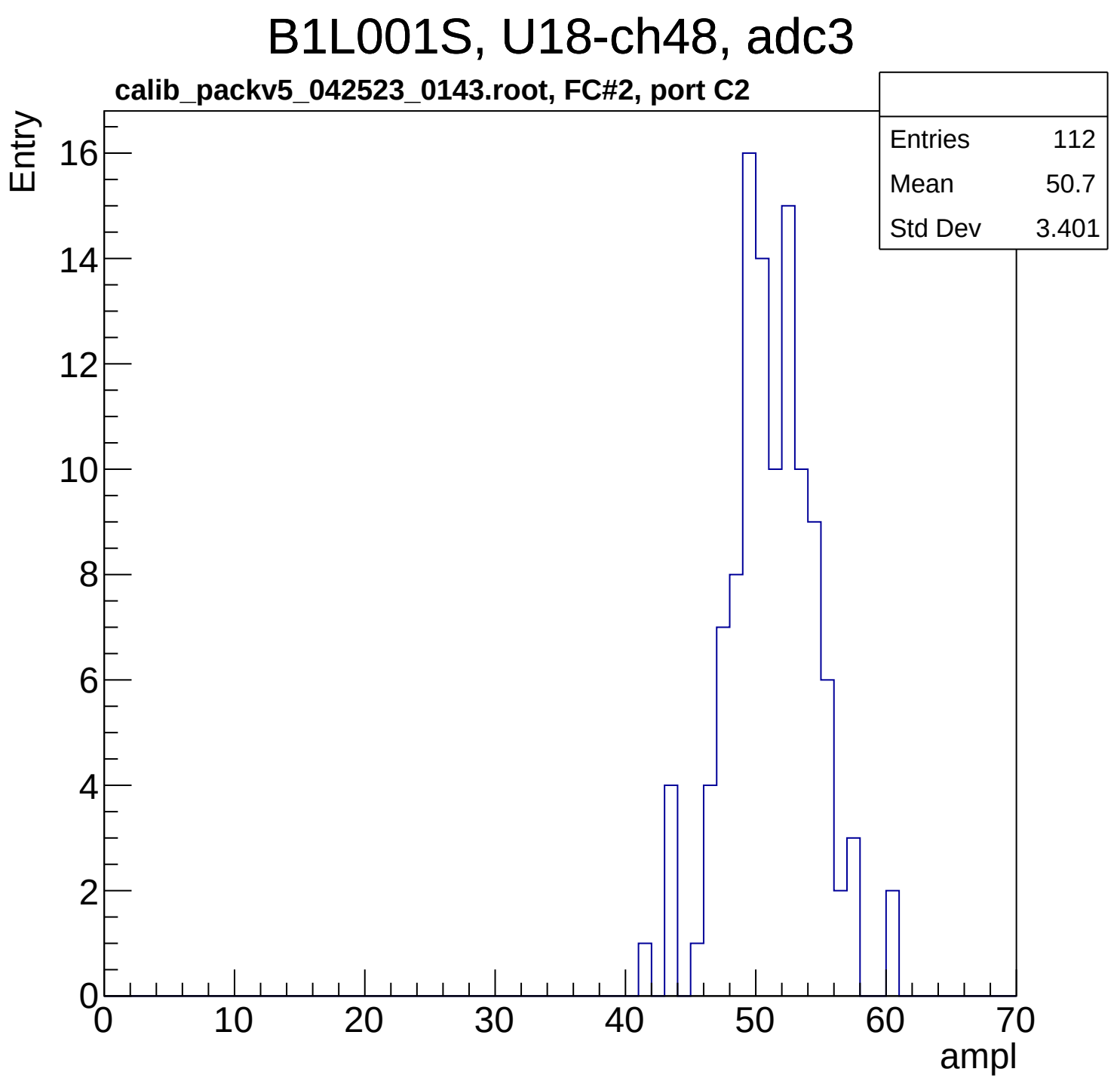

B1L001S, U18-ch47, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 11
Mean 55.91
Std Dev 17.88
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

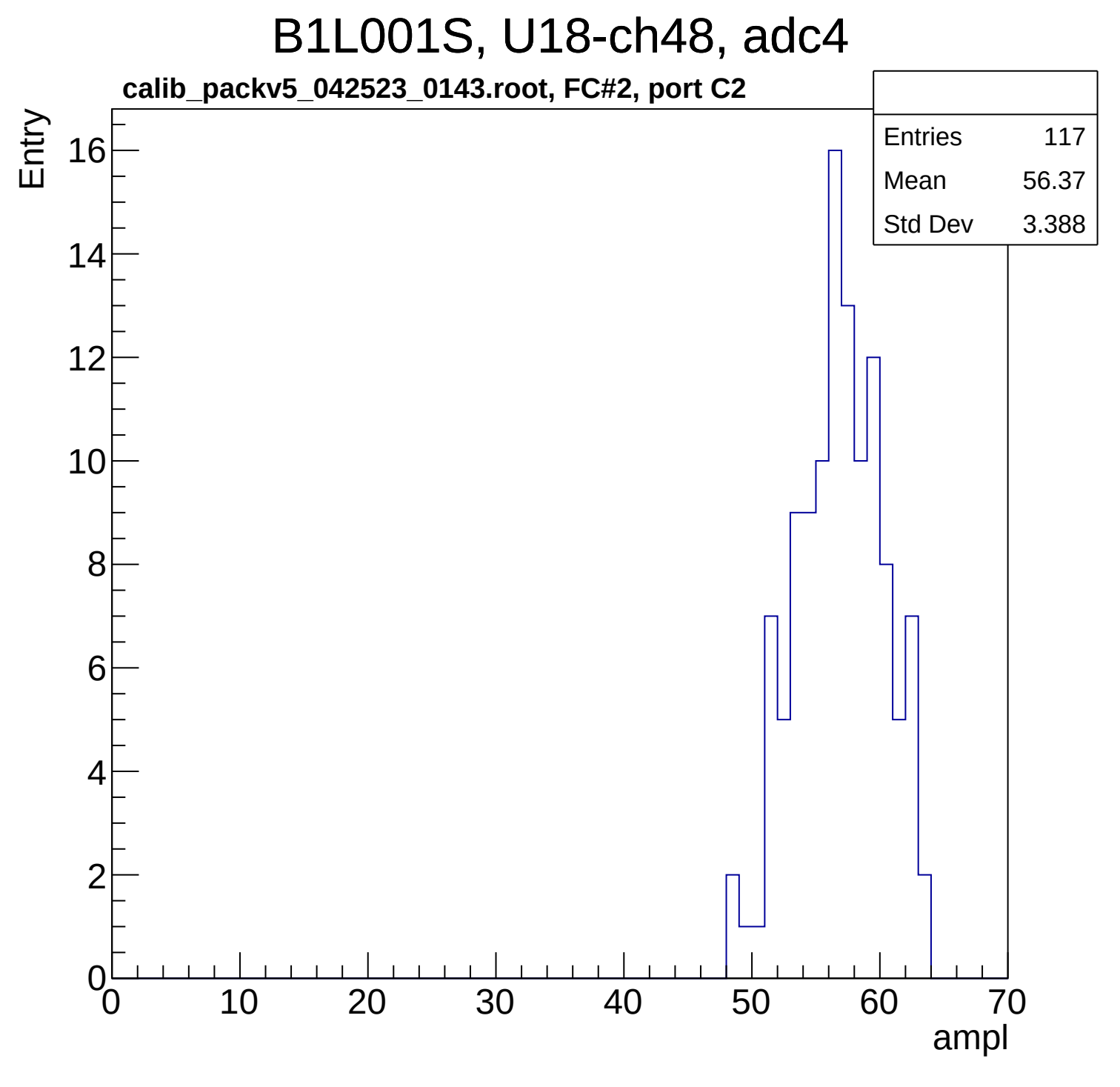

B1L001S, U18-ch47, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 4
Mean 20.5
Std Dev 25.31
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

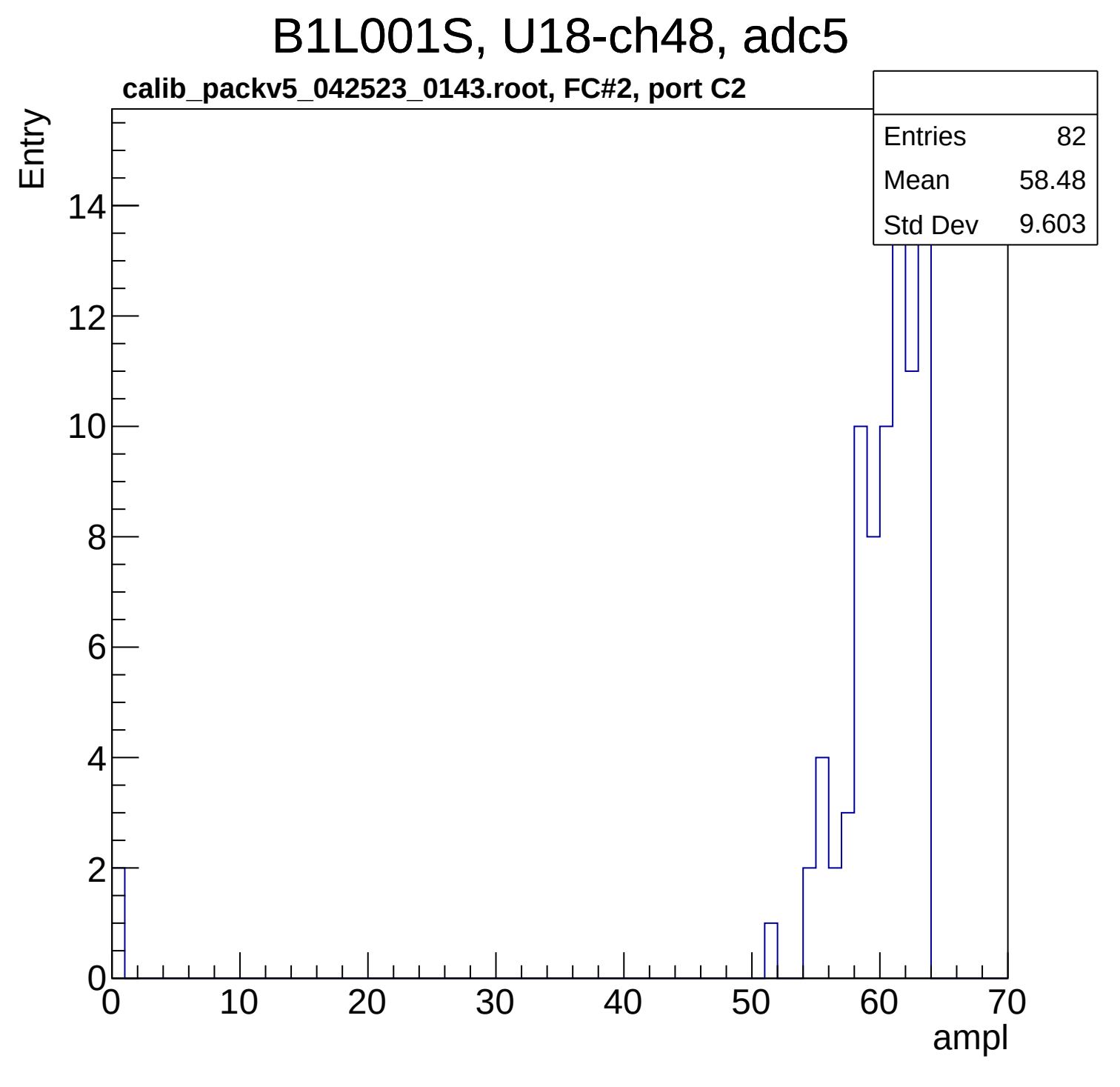

B1L001S, U18-ch48, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 121
Mean 31.55
Std Dev 3.31
Gaus mean : 31.8170
Gaus Width: 3.0978
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

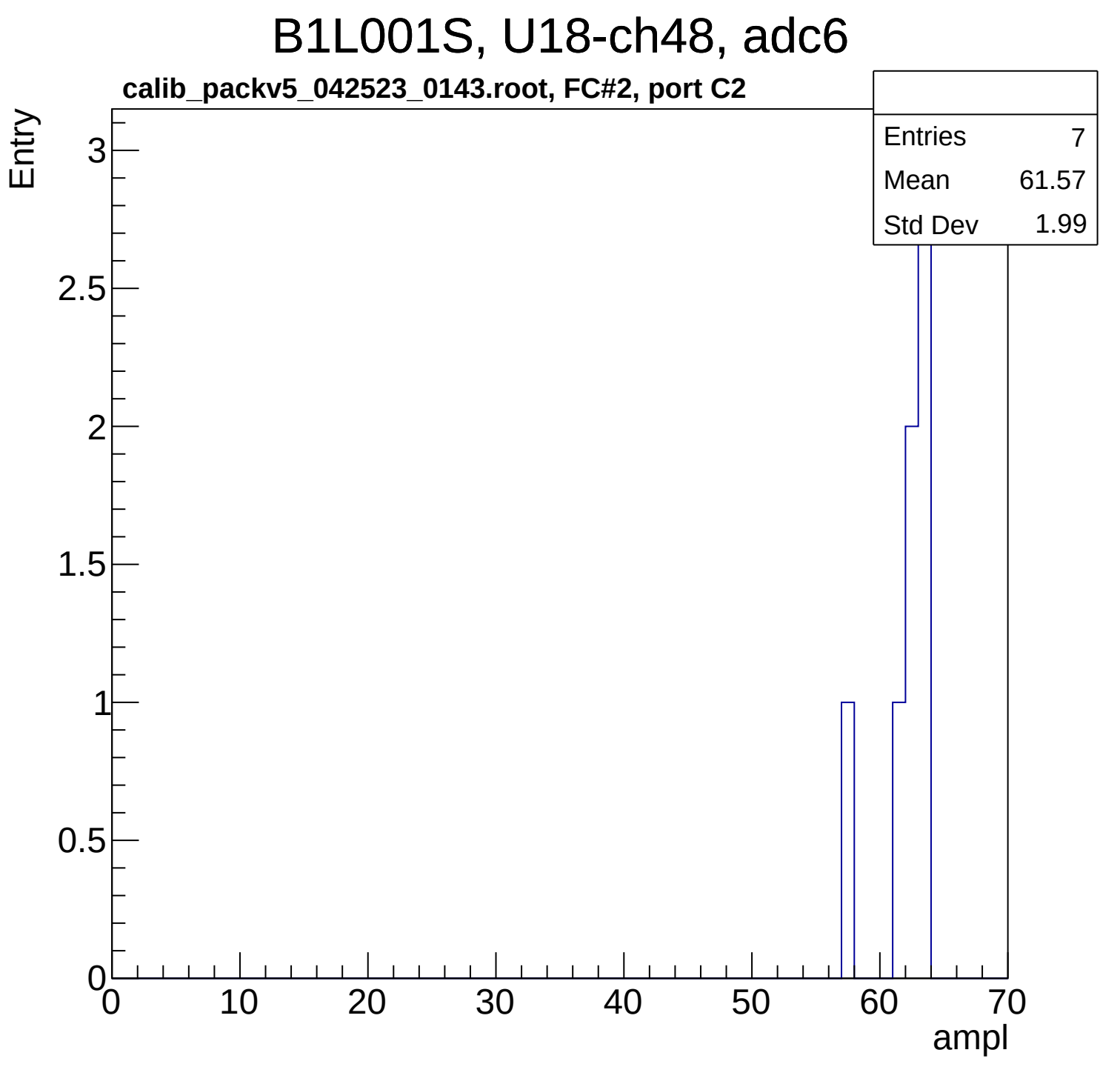

B1L001S, U18-ch48, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 157
Mean 38.22
Std Dev 3.761
Gaus mean : 38.8955
Gaus Width: 3.7155
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

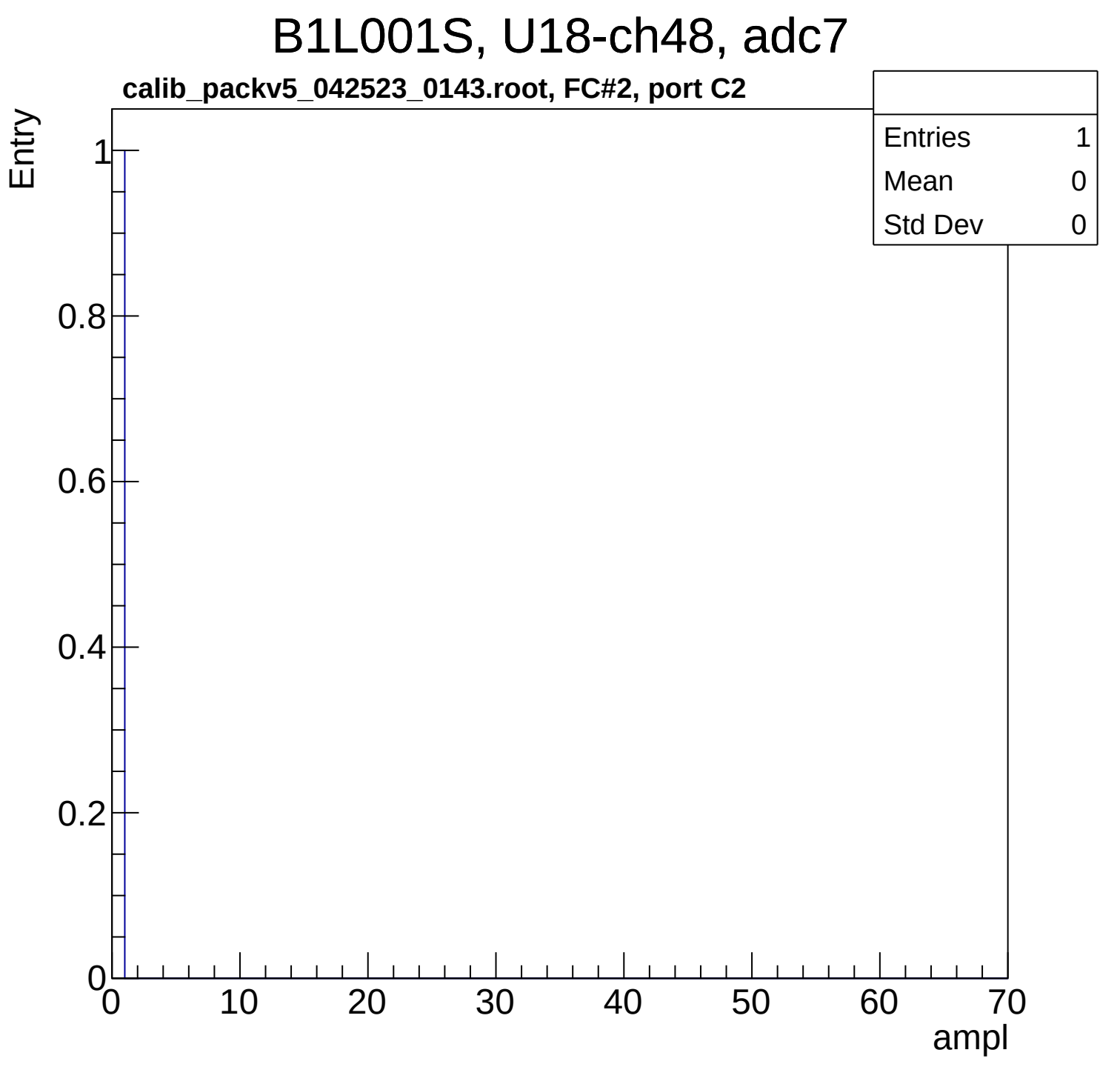

B1L001S, U18-ch48, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 109
Mean 44.88
Std Dev 3.161
Gaus mean : 45.4599
Gaus Width: 3.0005
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

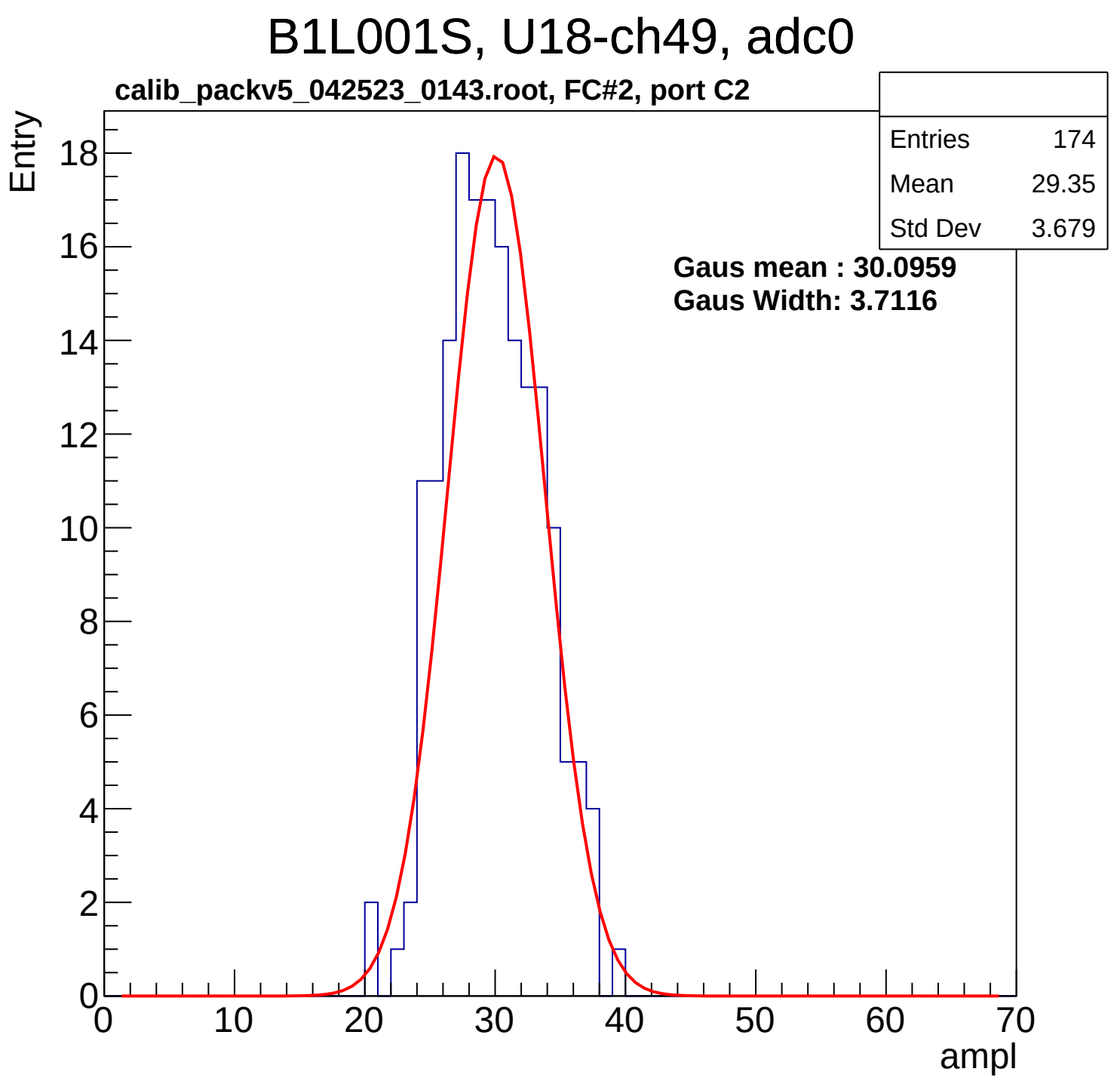

B1L001S, U18-ch48, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 112
Mean 50.7
Std Dev 3.401
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

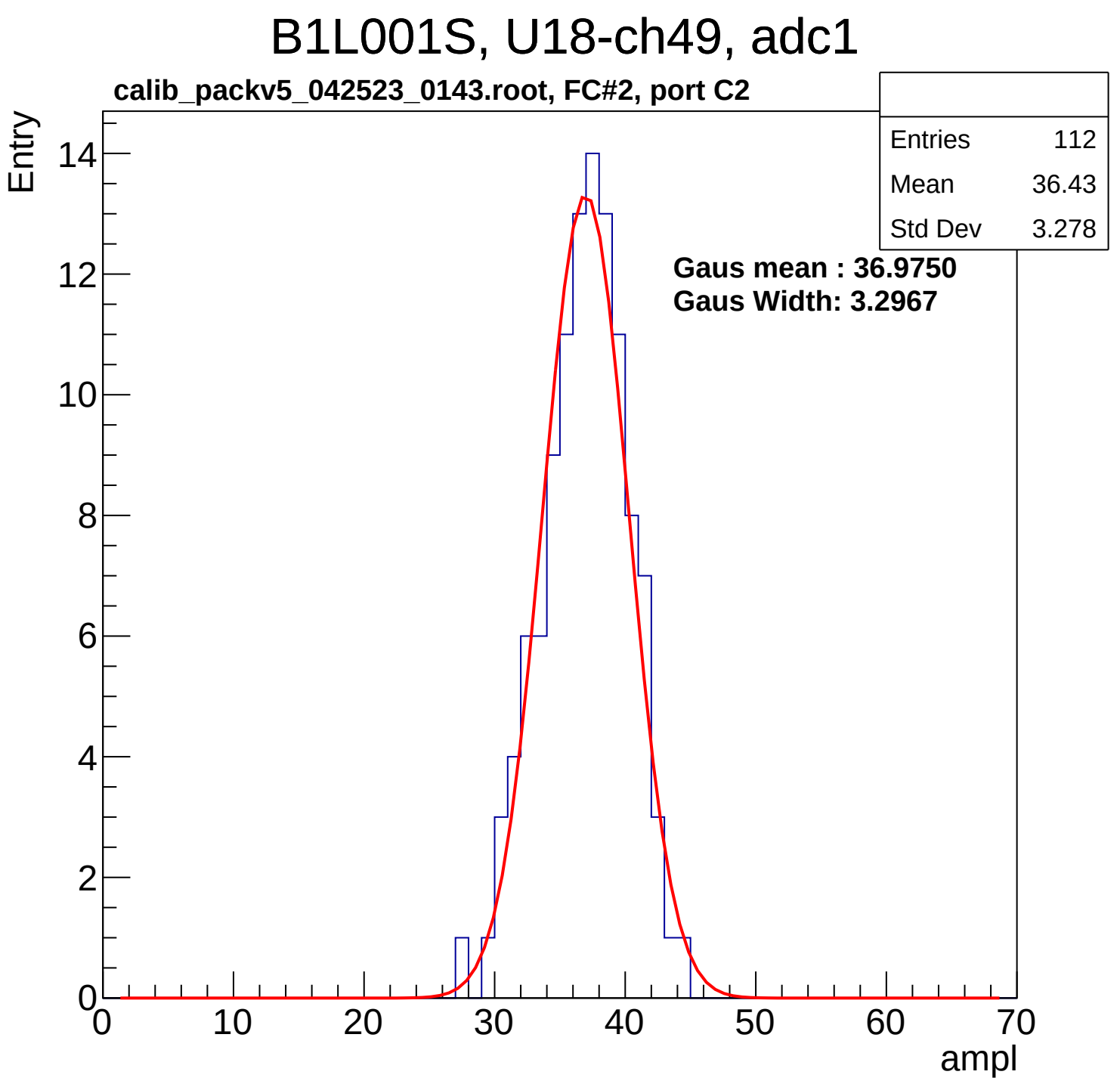

B1L001S, U18-ch48, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 117
Mean 56.37
Std Dev 3.388
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

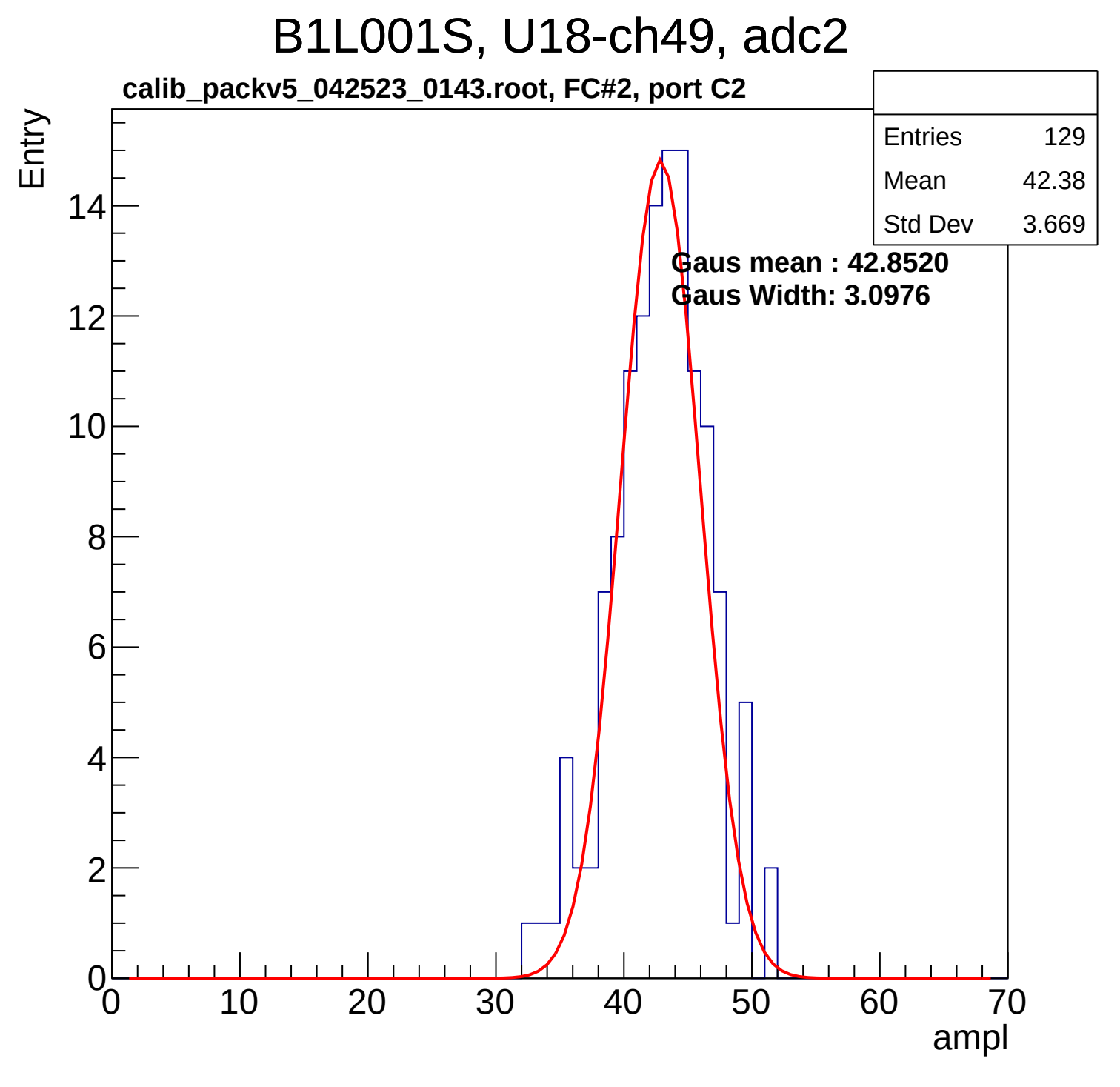

B1L001S, U18-ch48, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 82
Mean 58.48
Std Dev 9.603
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

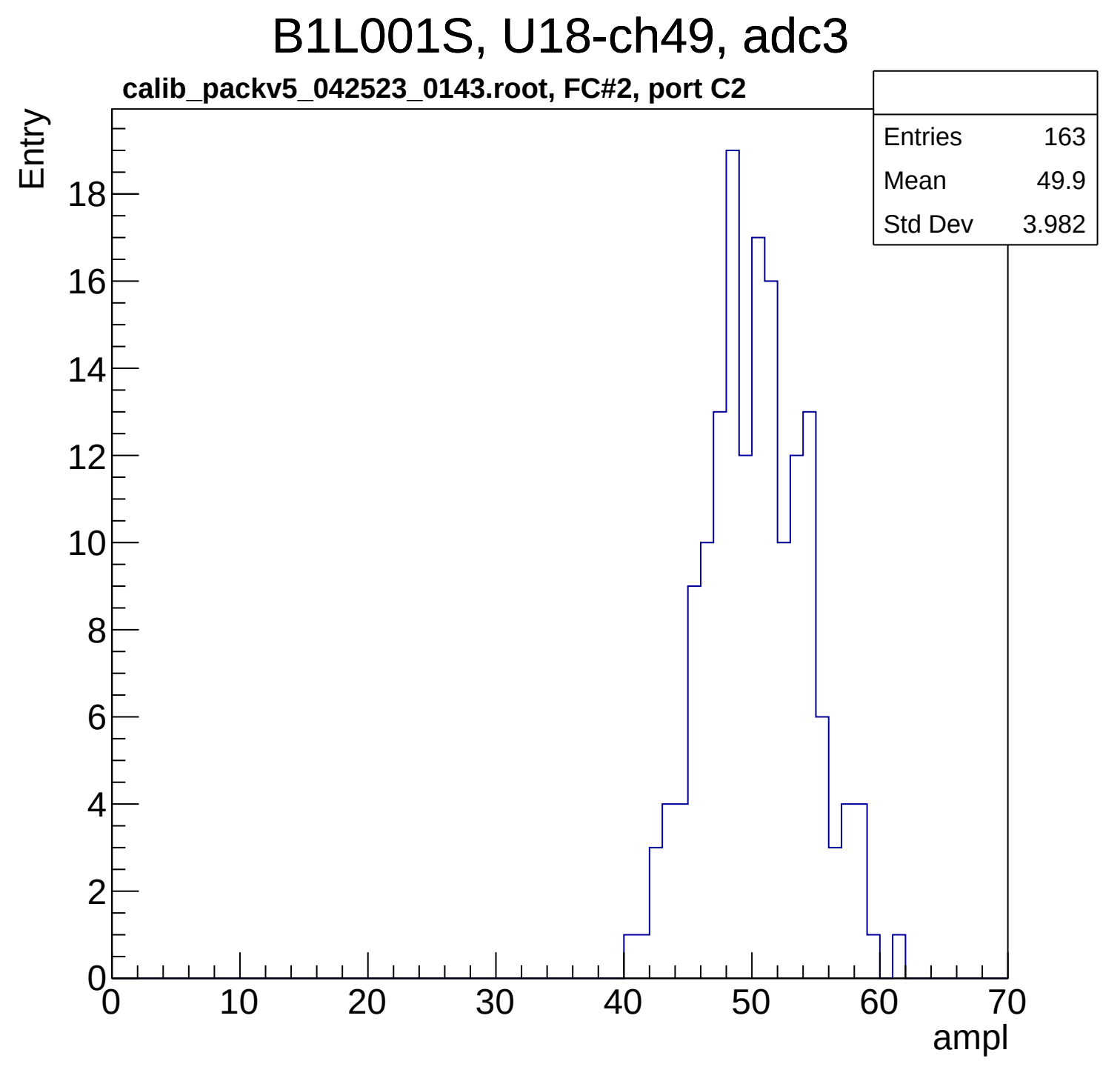

B1L001S, U18-ch48, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 7
Mean 61.57
Std Dev 1.99
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

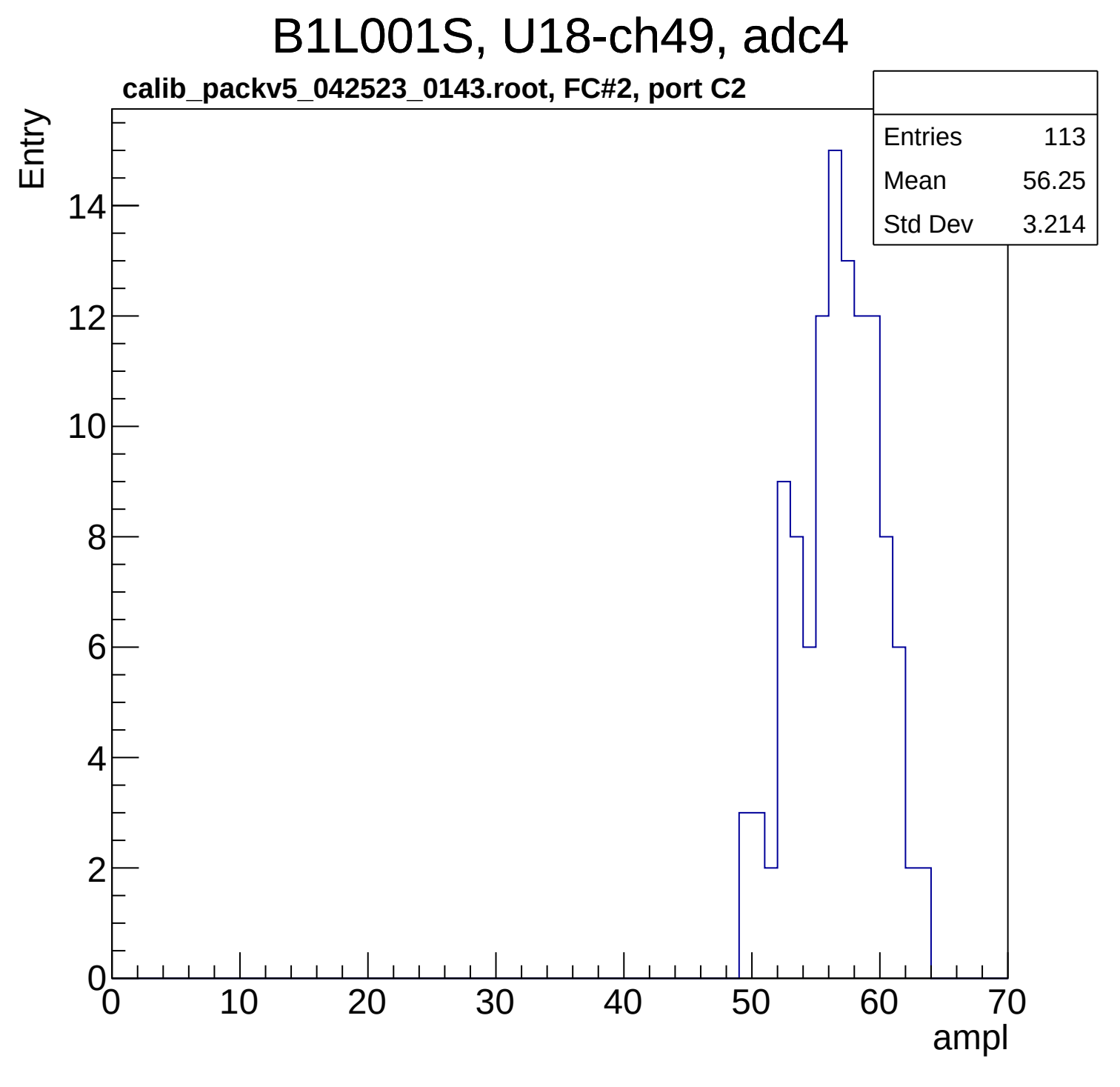

B1L001S, U18-ch48, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

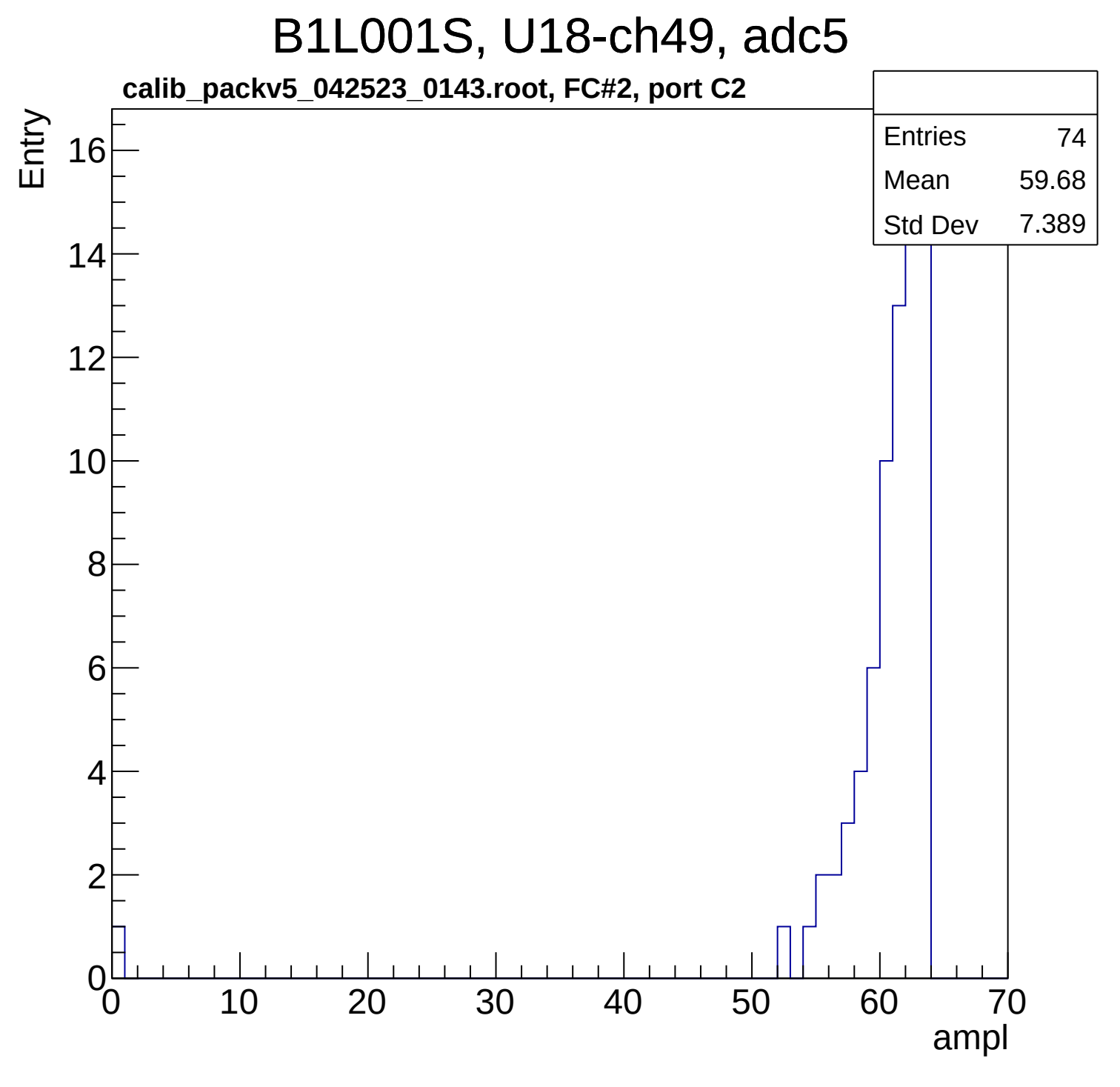

B1L001S, U18-ch49, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 174
Mean 29.35
Std Dev 3.679
Gaus mean : 30.0959
Gaus Width: 3.7116
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

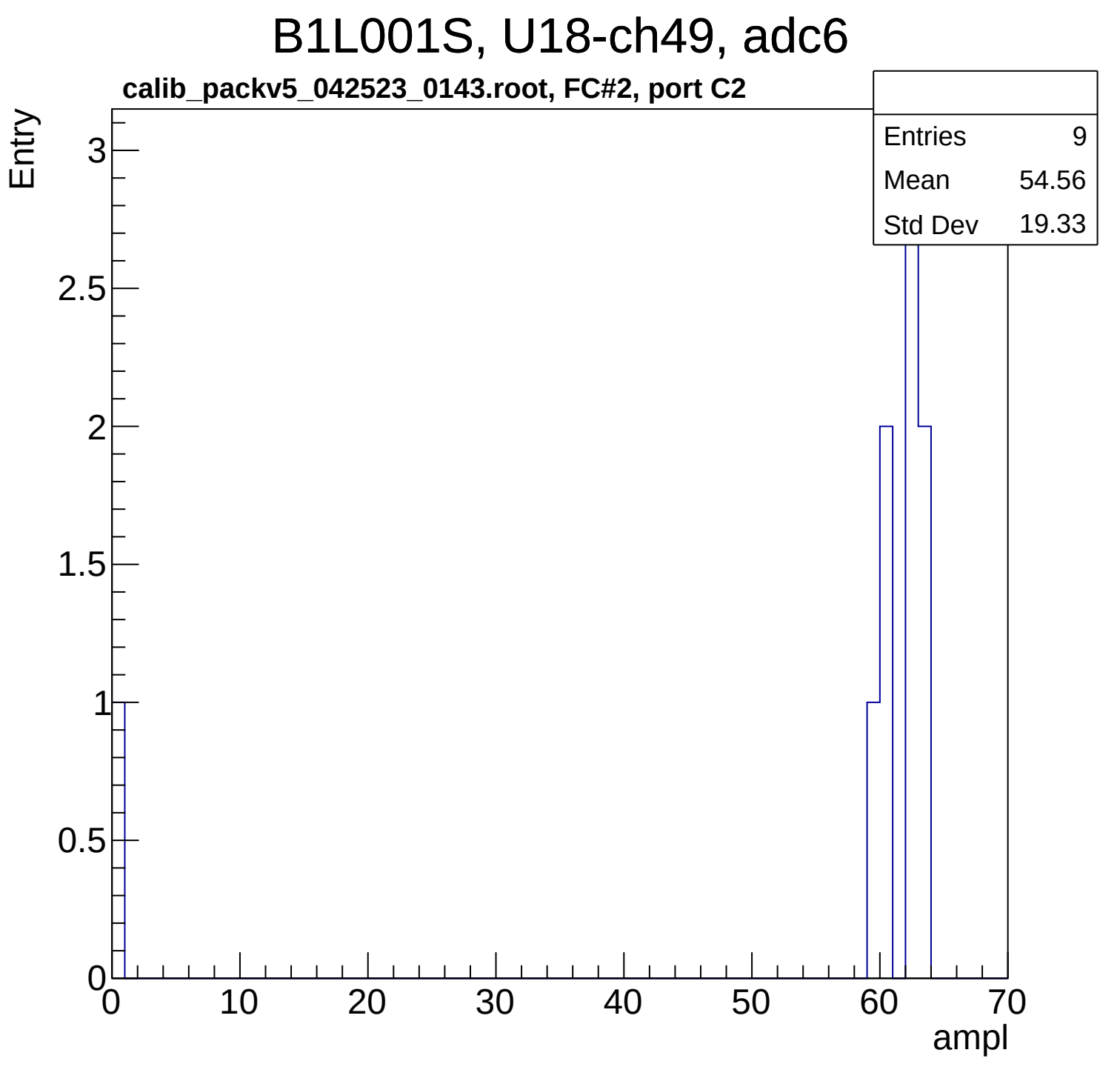

B1L001S, U18-ch49, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 112
Mean 36.43
Std Dev 3.278
Gaus mean : 36.9750
Gaus Width: 3.2967
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

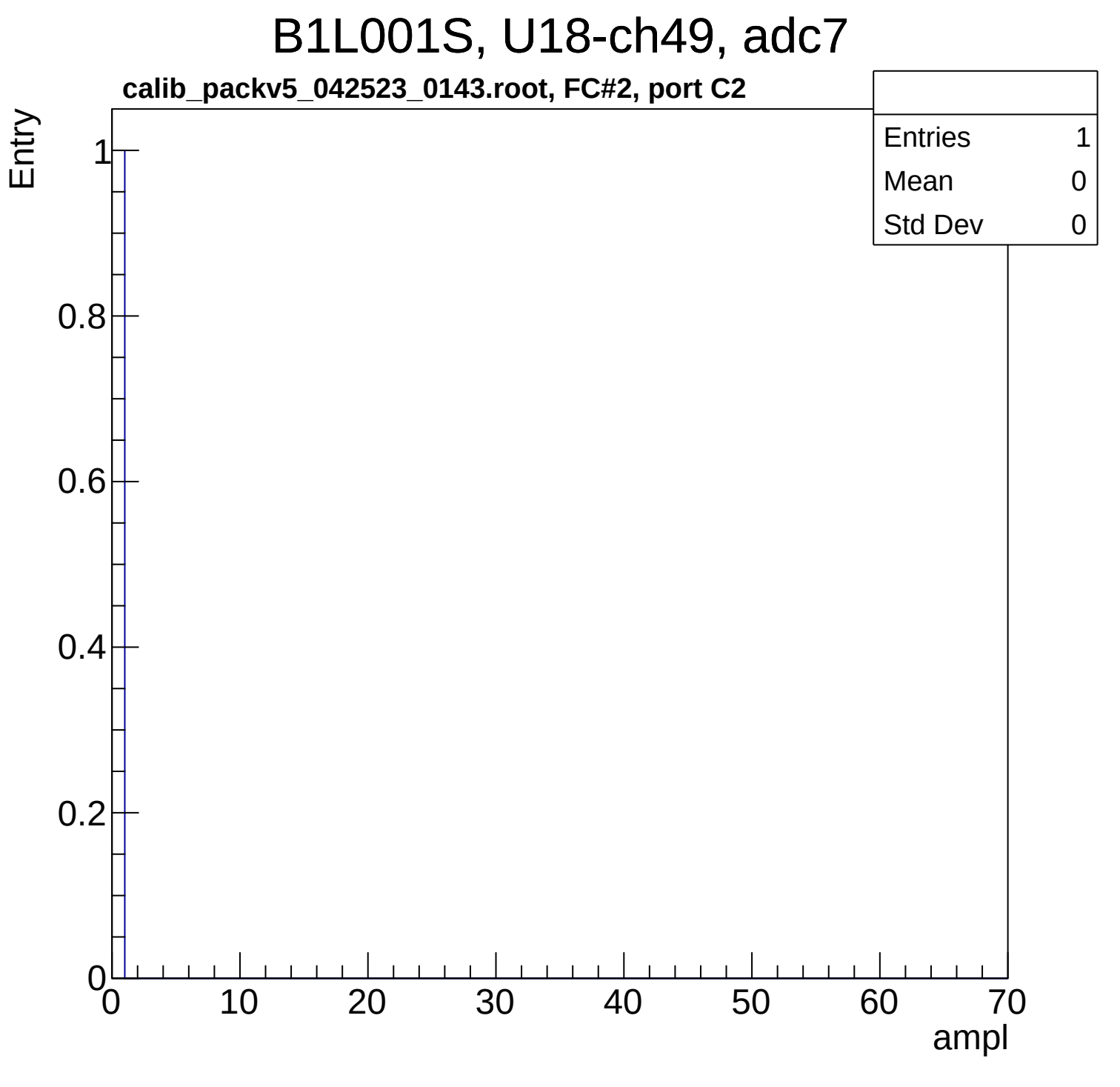

B1L001S, U18-ch49, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 129
Mean 42.38
Std Dev 3.669
Gaus mean : 42.8520
Gaus Width: 3.0976
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

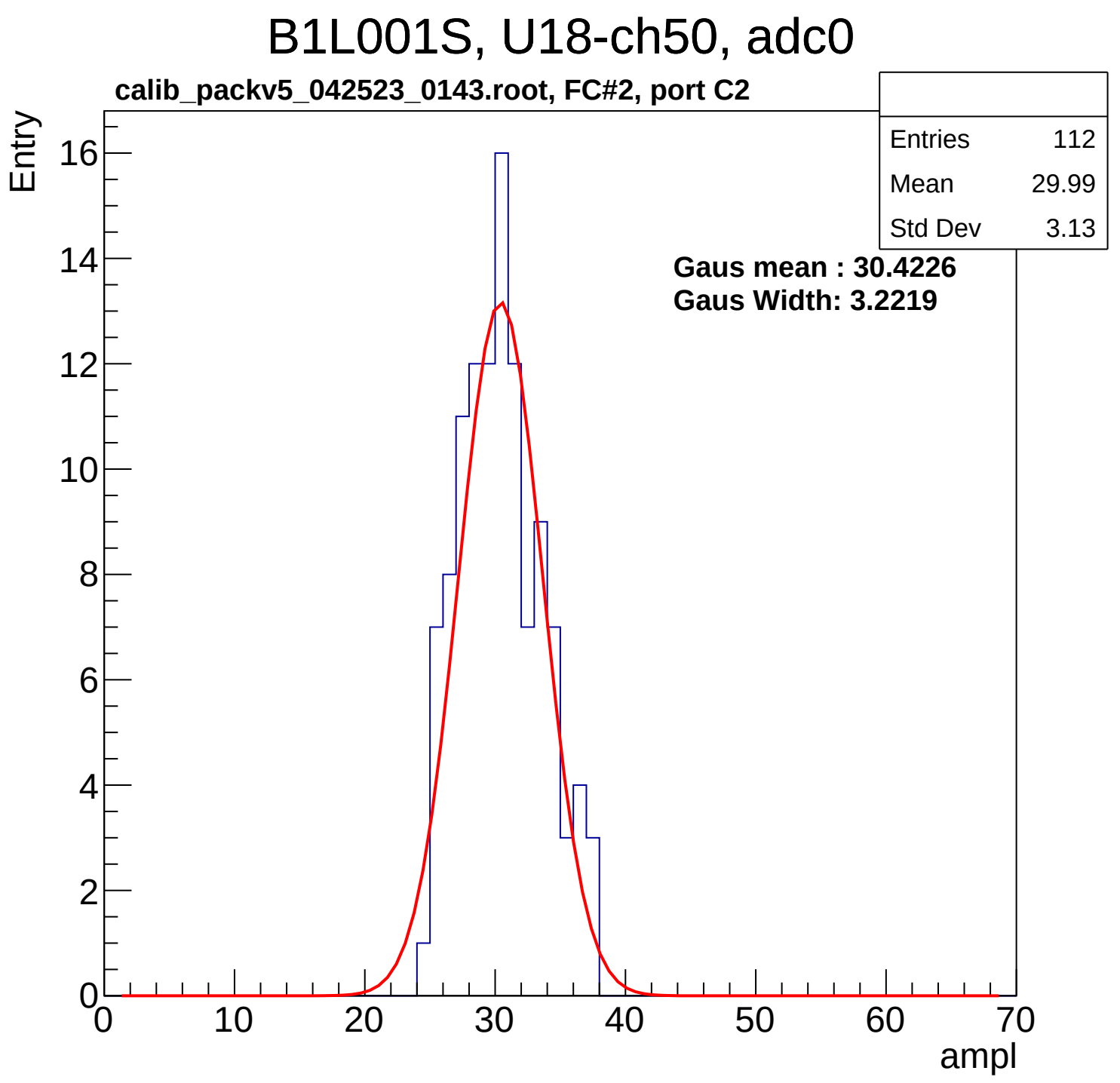

B1L001S, U18-ch49, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 163
Mean 49.9
Std Dev 3.982
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

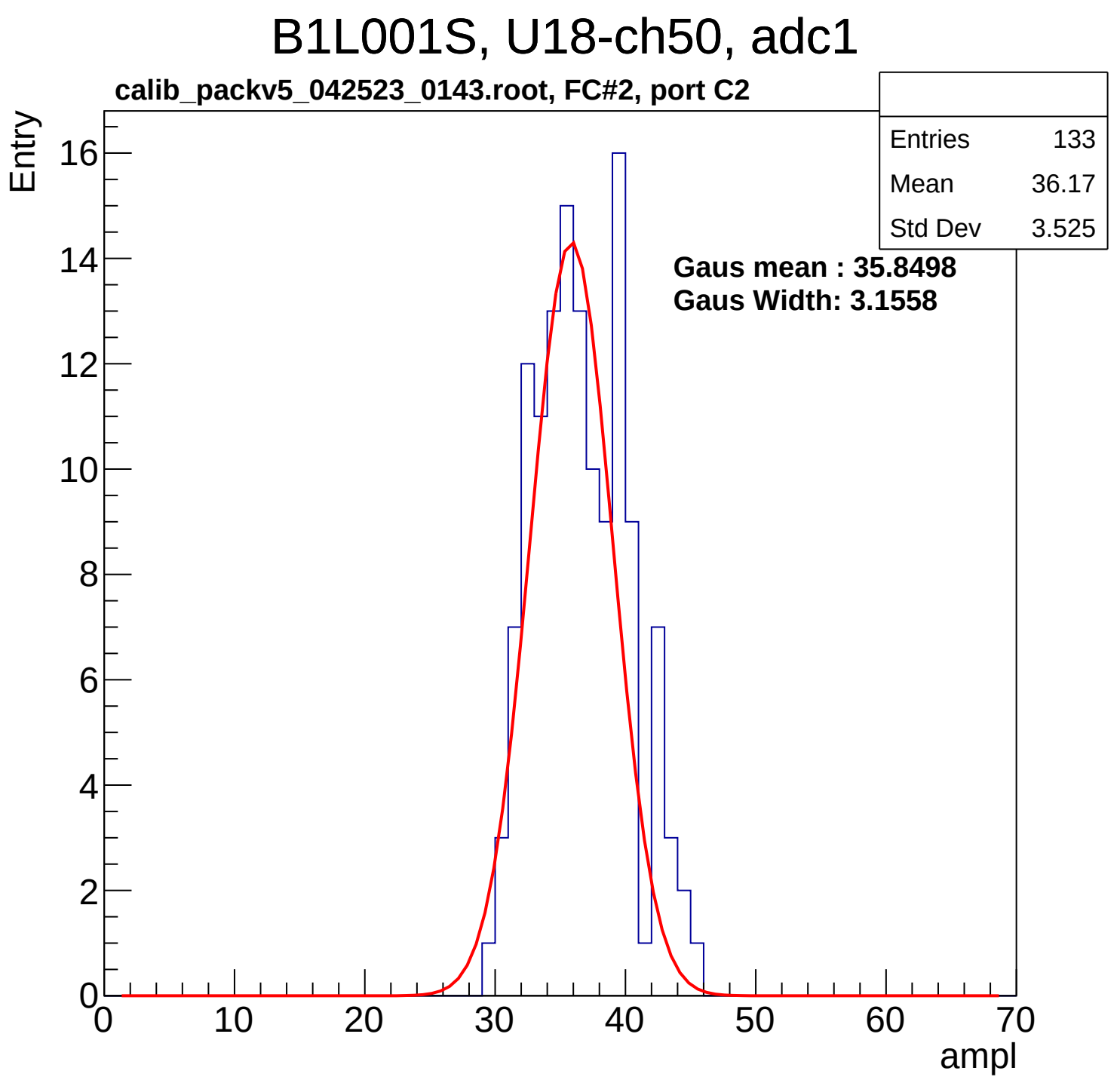

B1L001S, U18-ch49, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 113
Mean 56.25
Std Dev 3.214
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl

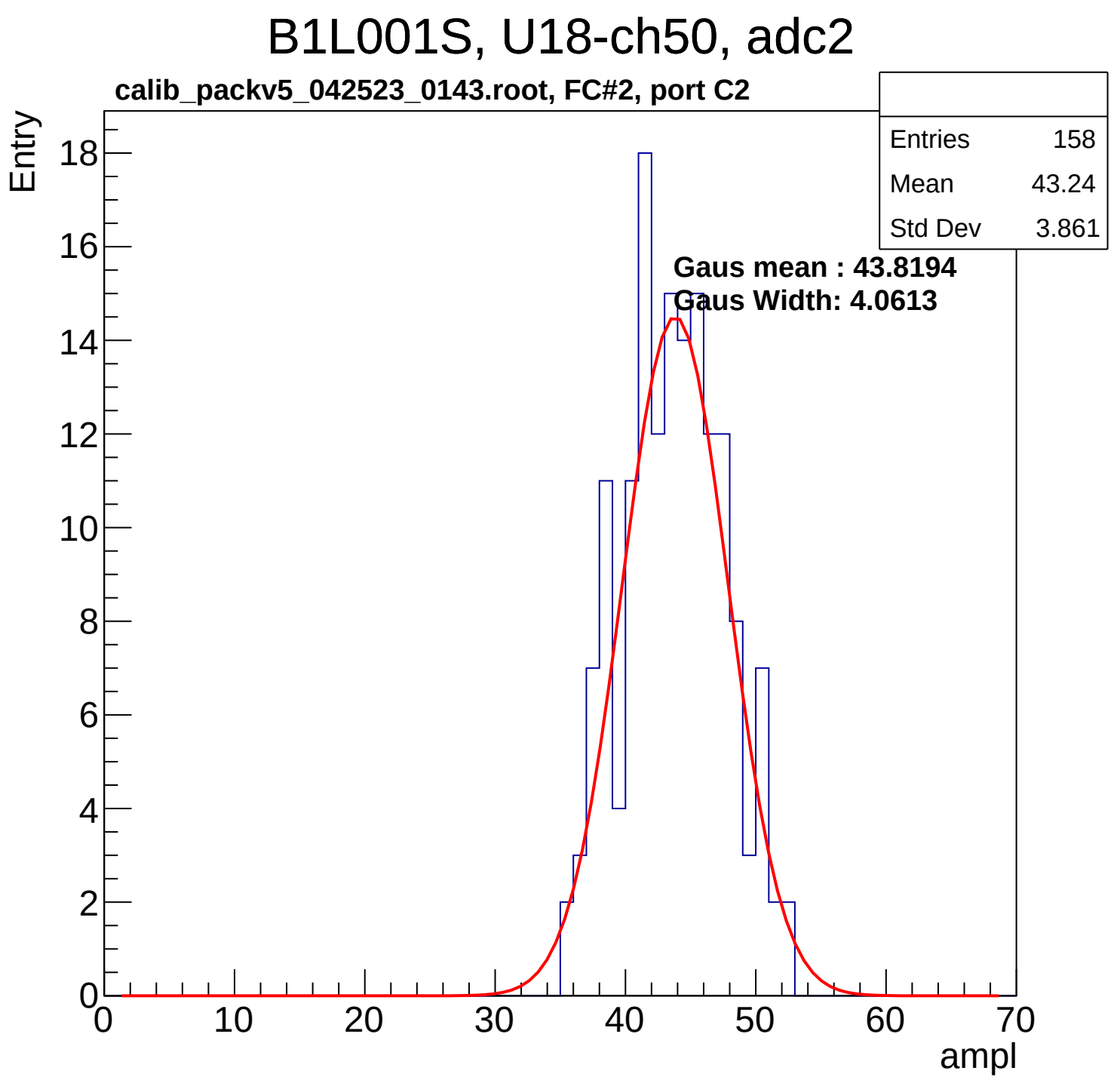

B1L001S, U18-ch49, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 74
Mean 59.68
Std Dev 7.389
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

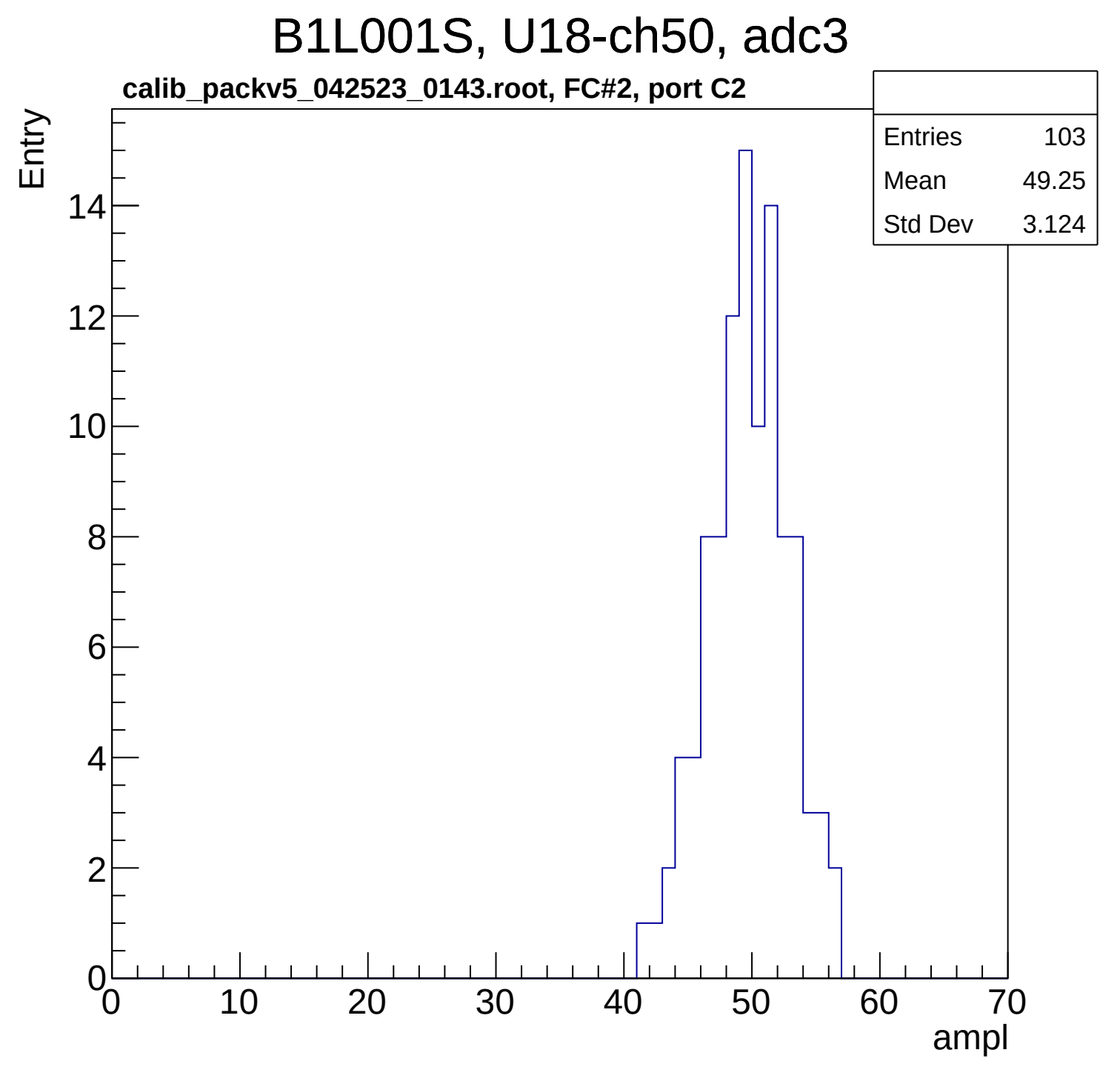

B1L001S, U18-ch49, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 9
Mean 54.56
Std Dev 19.33
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

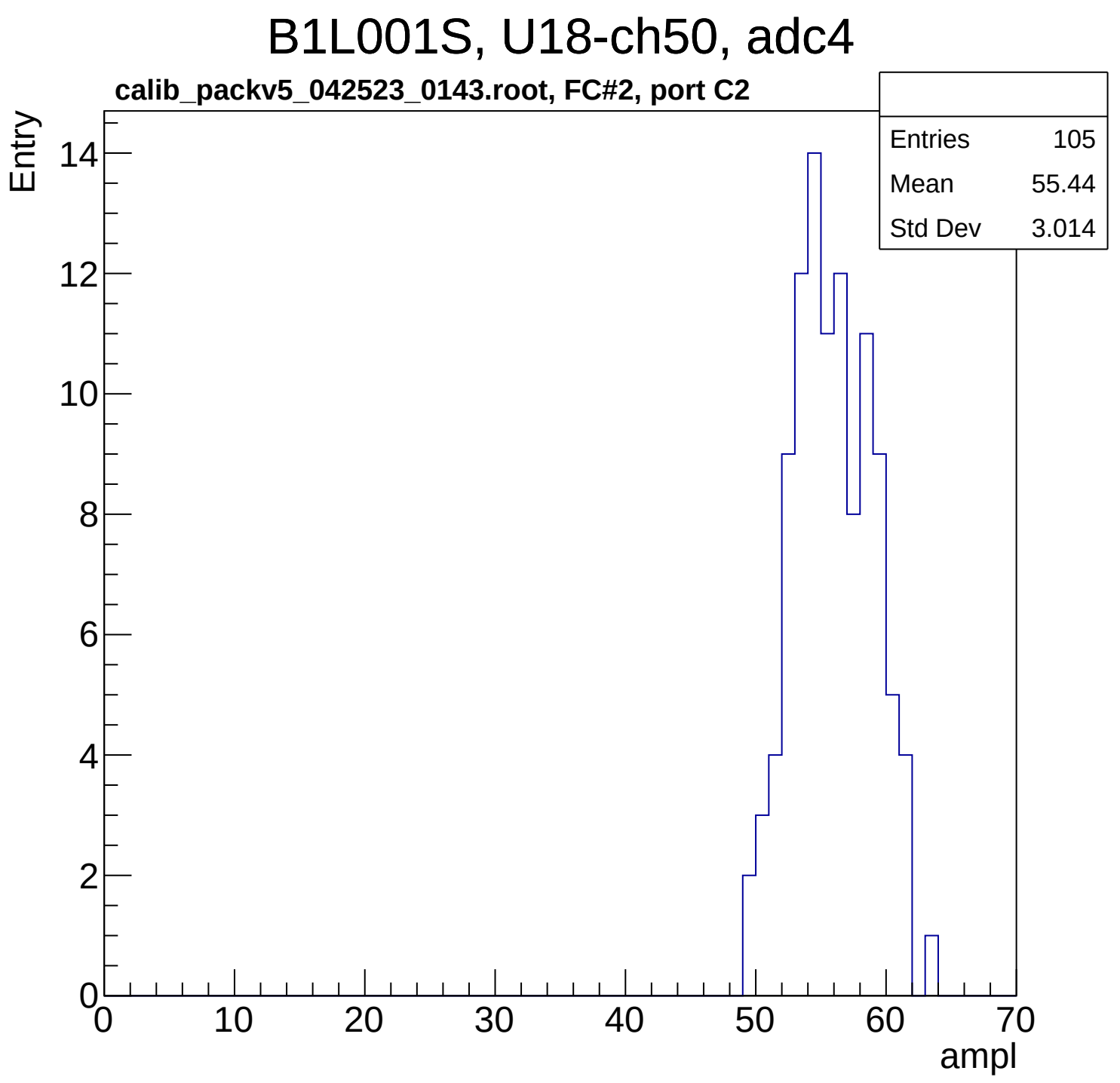

B1L001S, U18-ch49, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

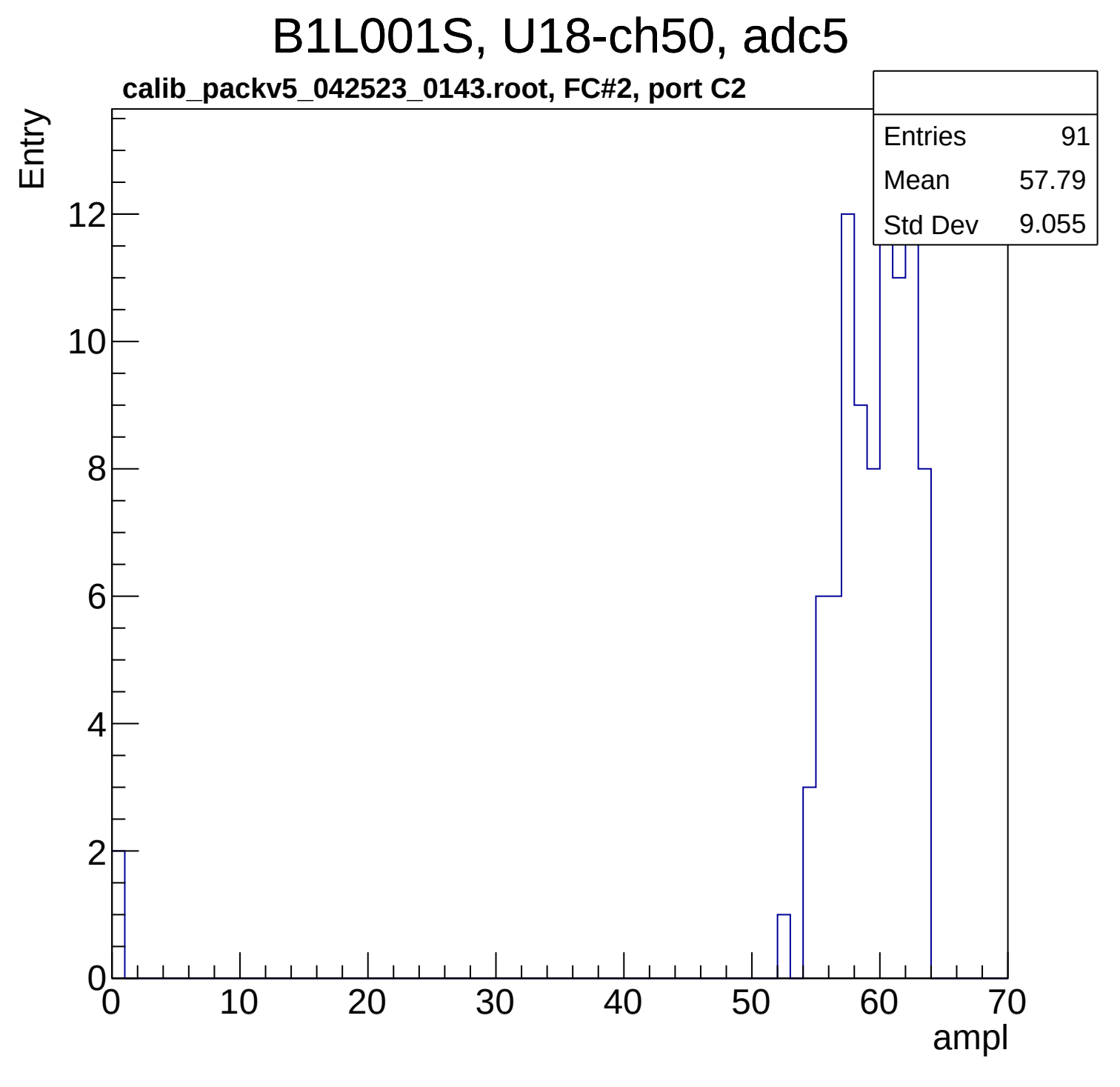

B1L001S, U18-ch50, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 112
Mean 29.99
Std Dev 3.13
Gaus mean : 30.4226
Gaus Width: 3.2219
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

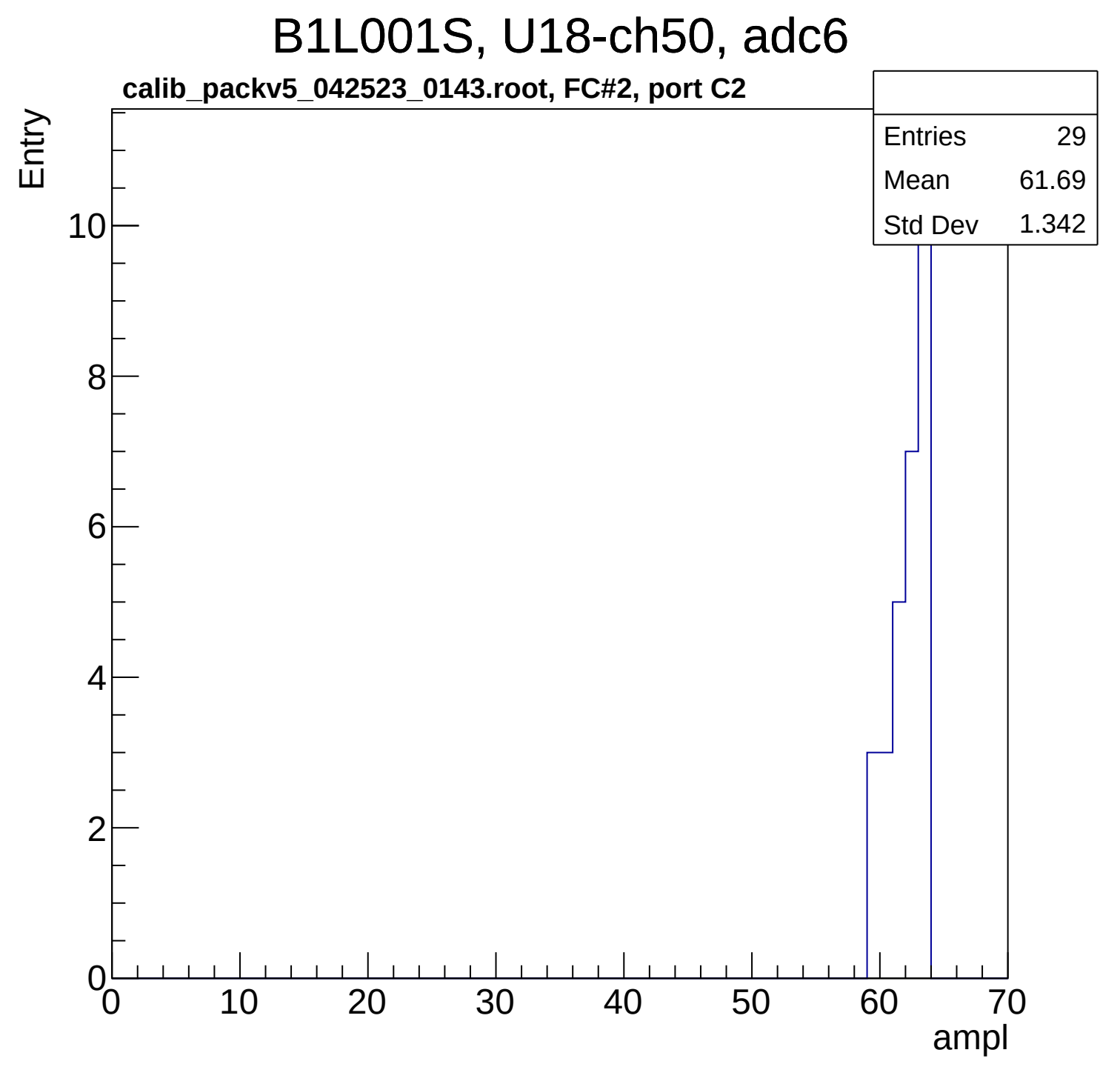

B1L001S, U18-ch50, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 133
Mean 36.17
Std Dev 3.525
Gaus mean : 35.8498
Gaus Width: 3.1558
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

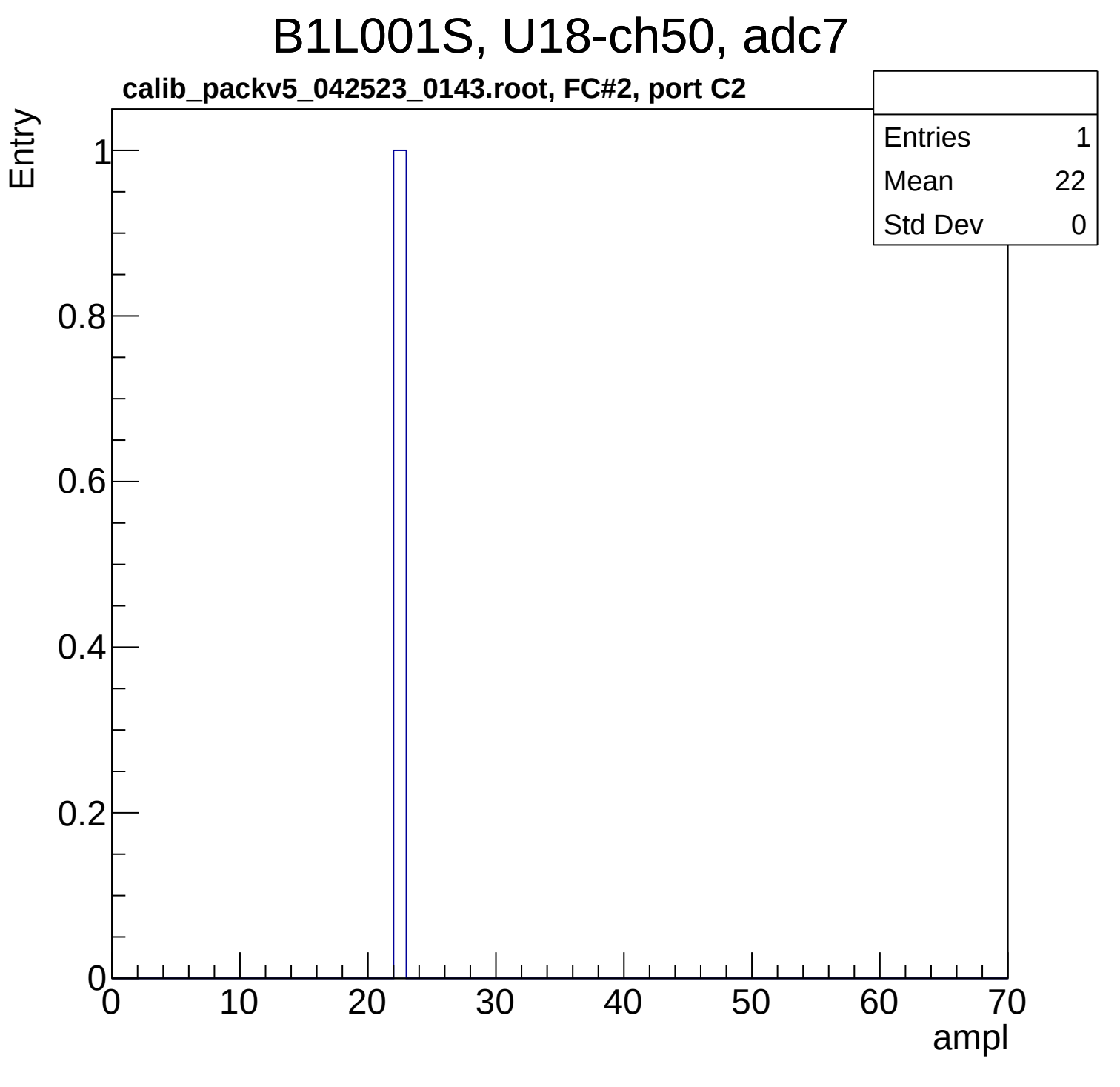

B1L001S, U18-ch50, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 158
Mean 43.24
Std Dev 3.861
Gaus mean : 43.8194
Gaus Width: 4.0613
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

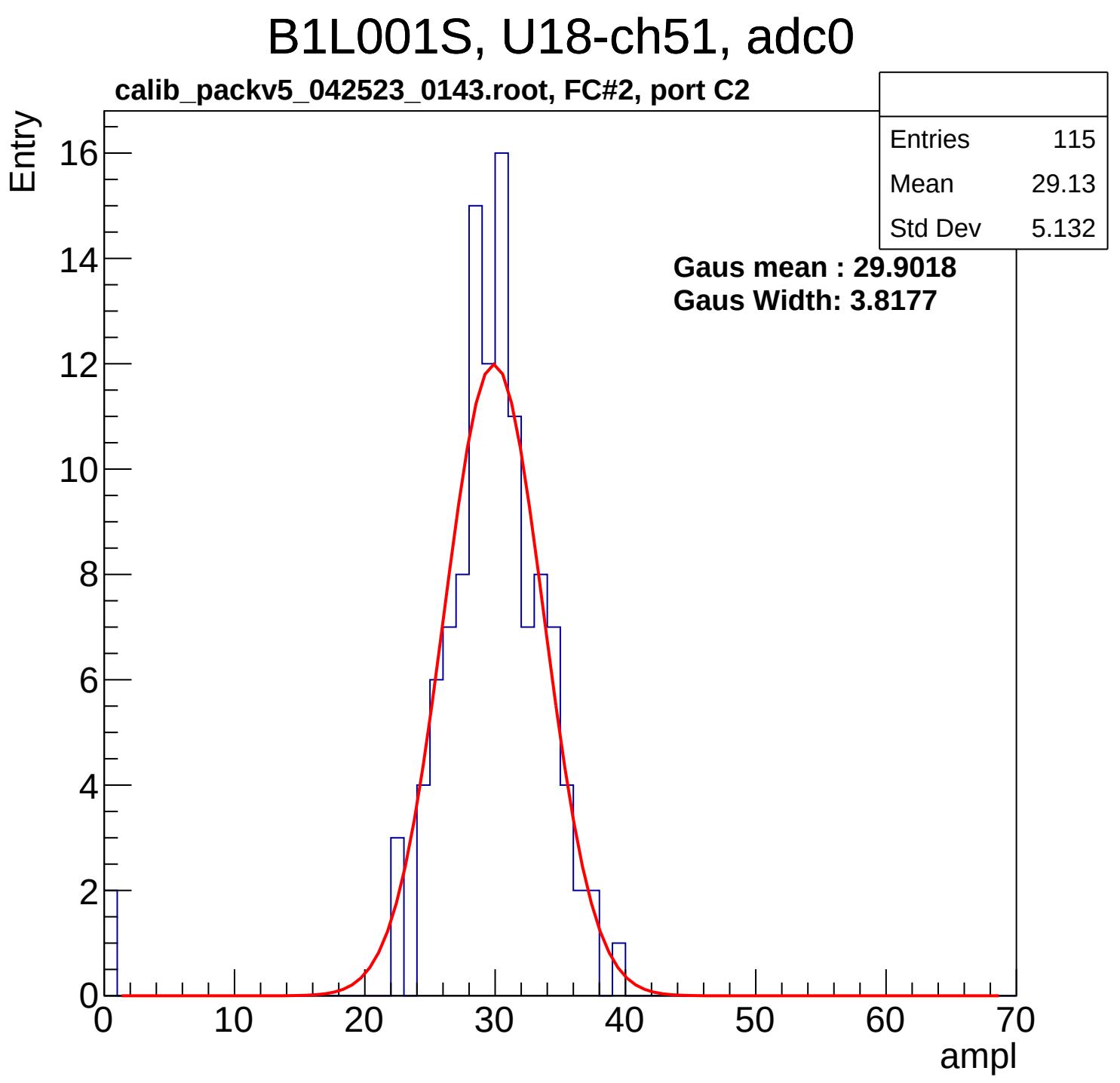

B1L001S, U18-ch50, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 103
Mean 49.25
Std Dev 3.124
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl

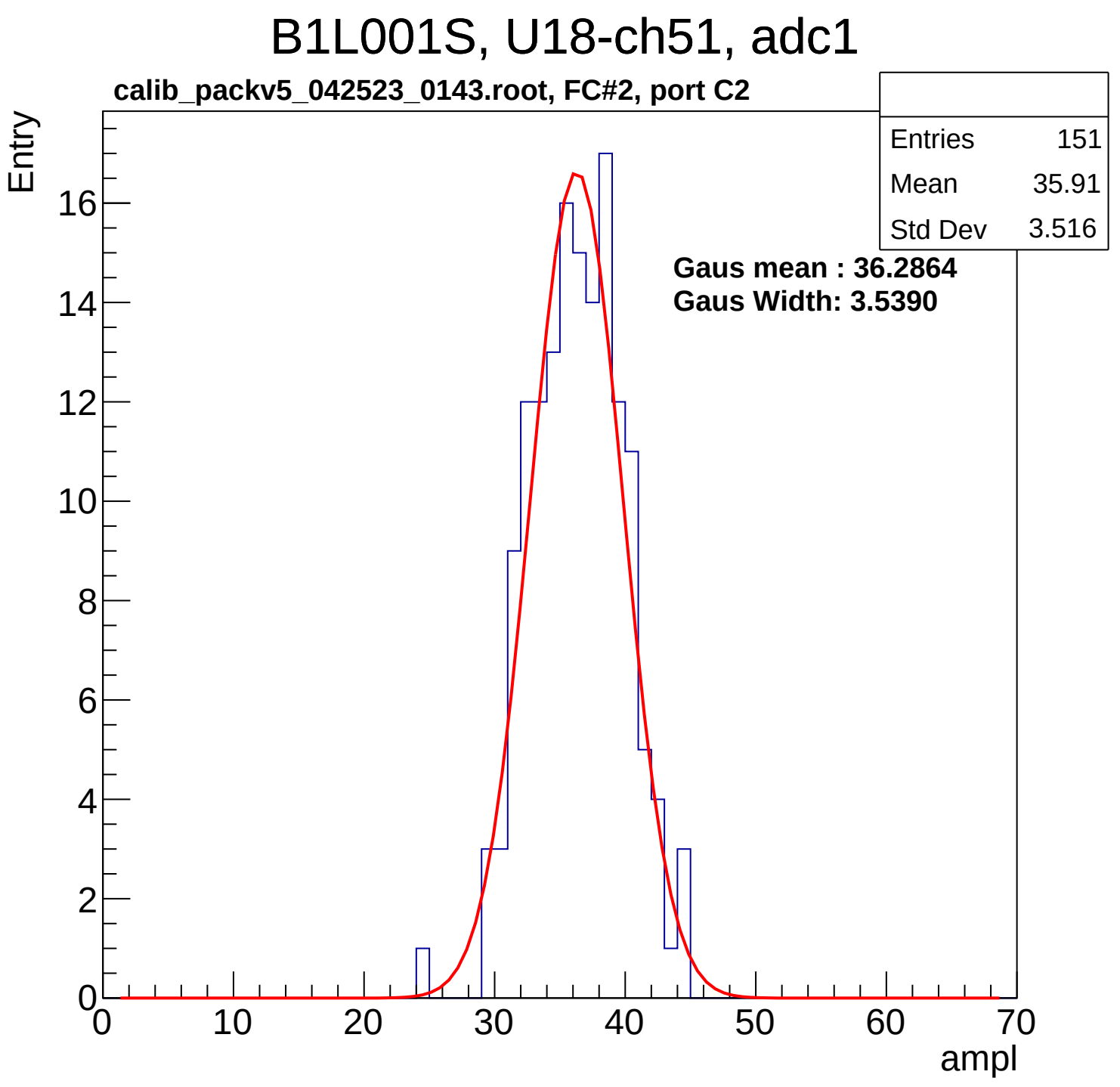

B1L001S, U18-ch50, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 105
Mean 55.44
Std Dev 3.014
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl

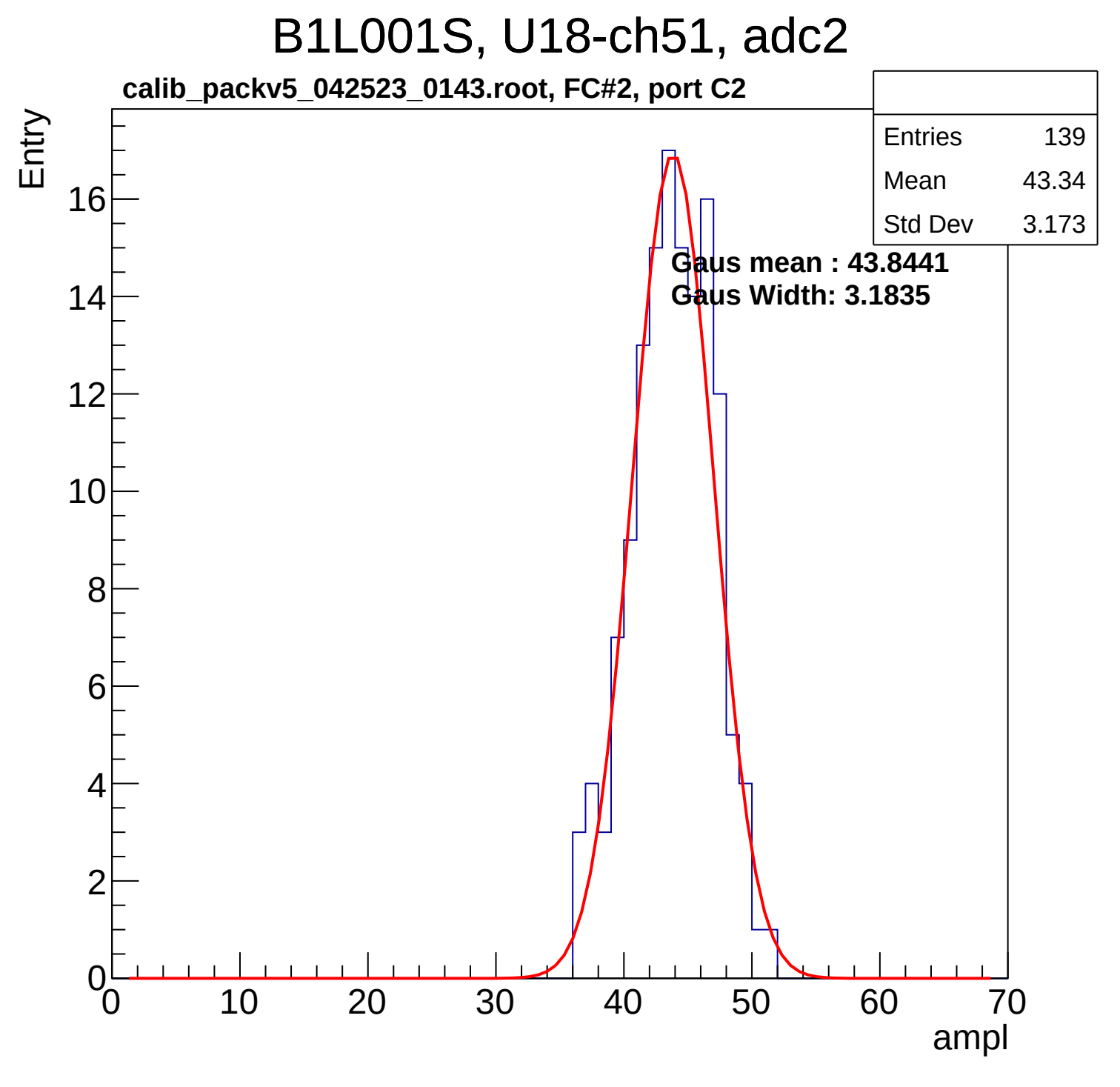

B1L001S, U18-ch50, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 91
Mean 57.79
Std Dev 9.055
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70

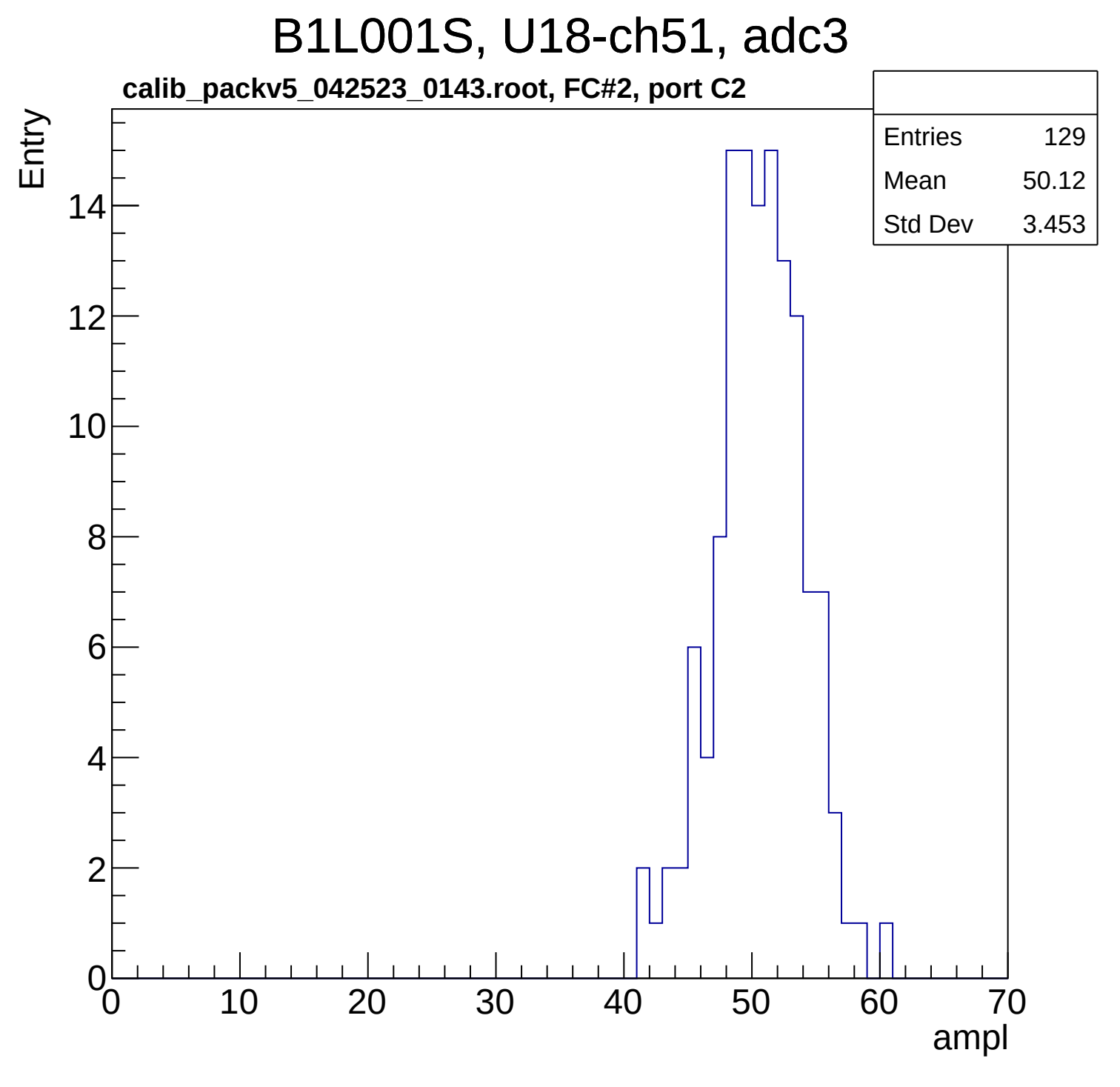

B1L001S, U18-ch50, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 29
Mean 61.69
Std Dev 1.342
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

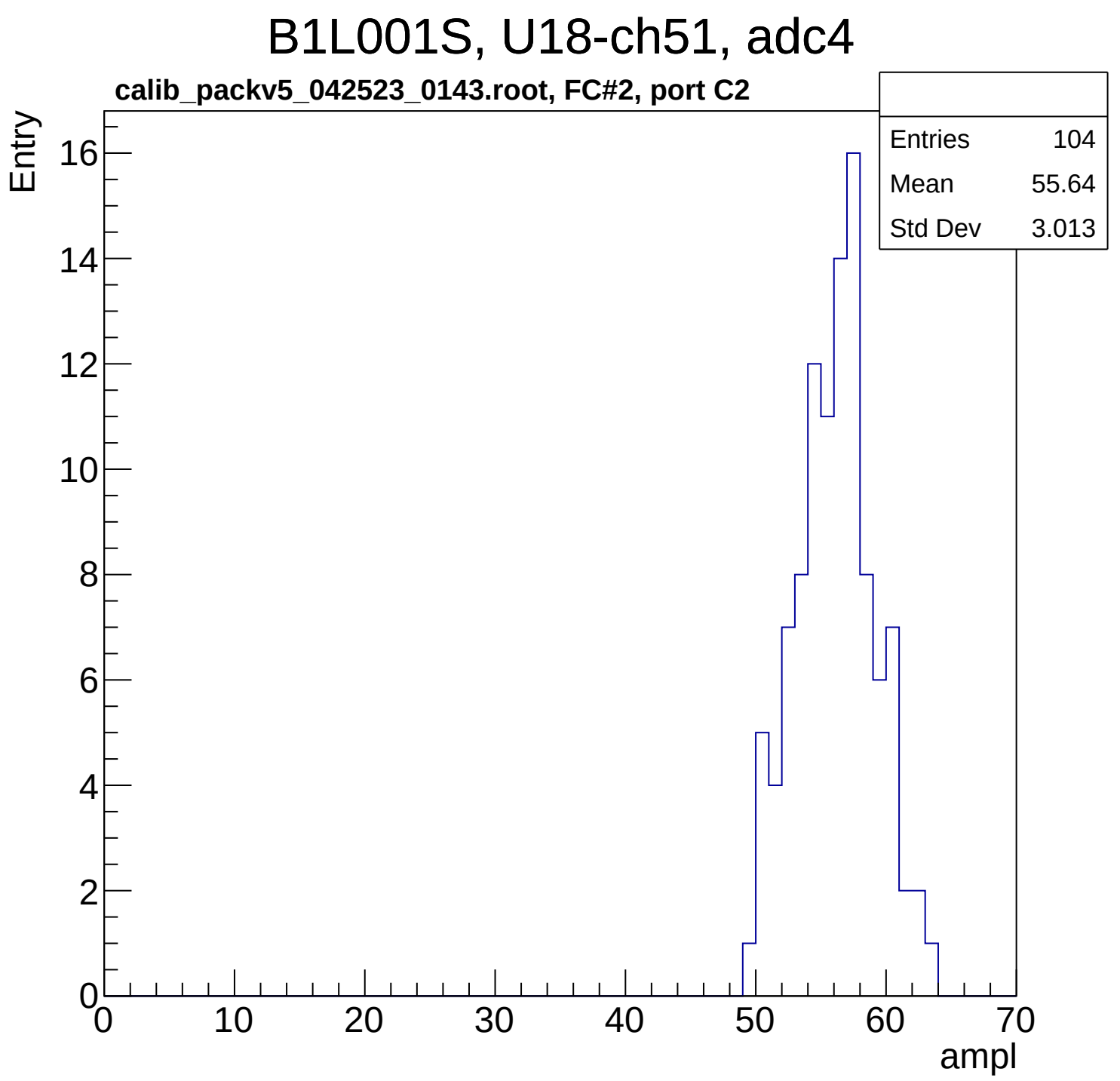

B1L001S, U18-ch50, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 22
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

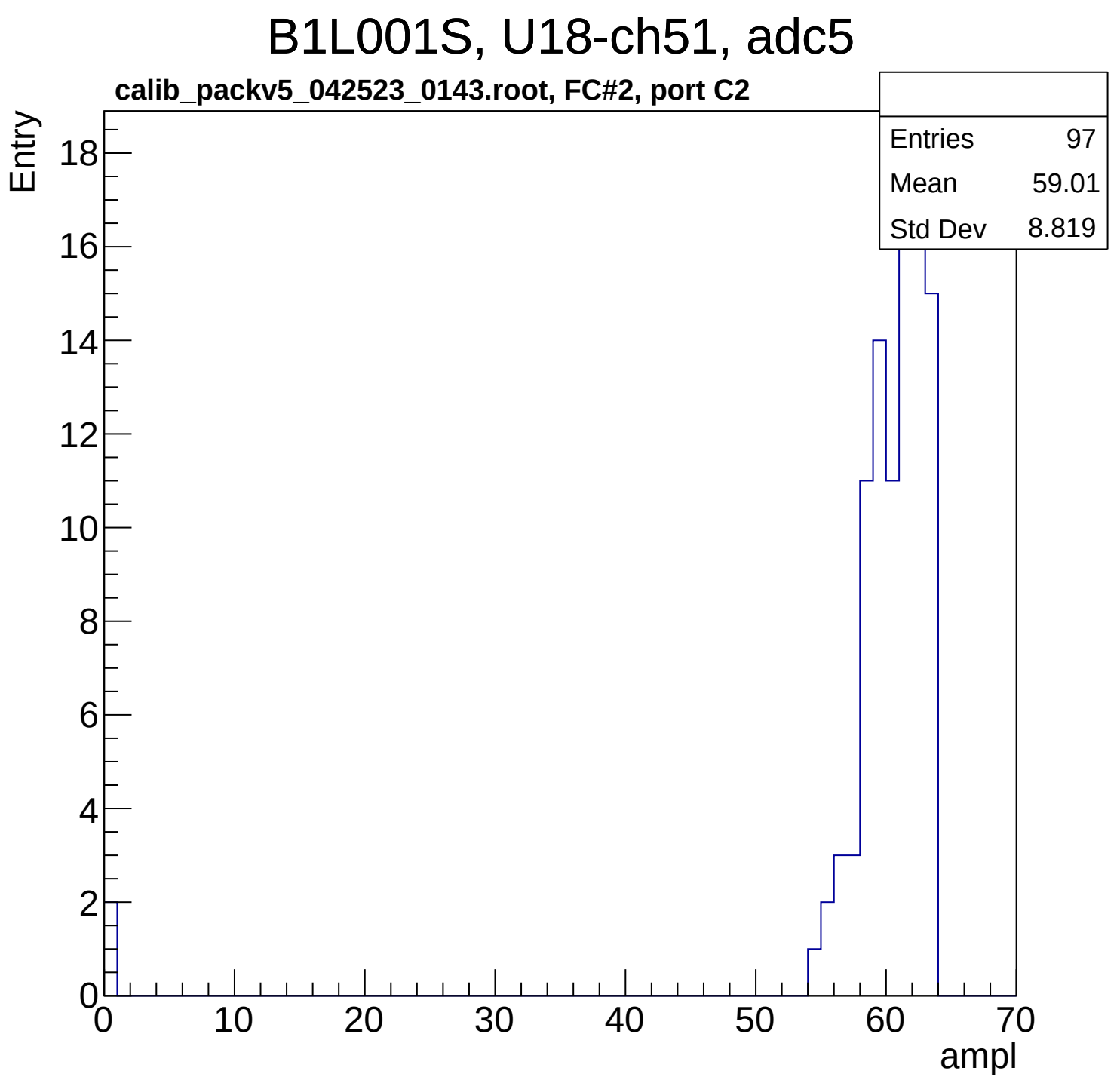

B1L001S, U18-ch51, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 115
Mean 29.13
Std Dev 5.132
Gaus mean : 29.9018
Gaus Width: 3.8177
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

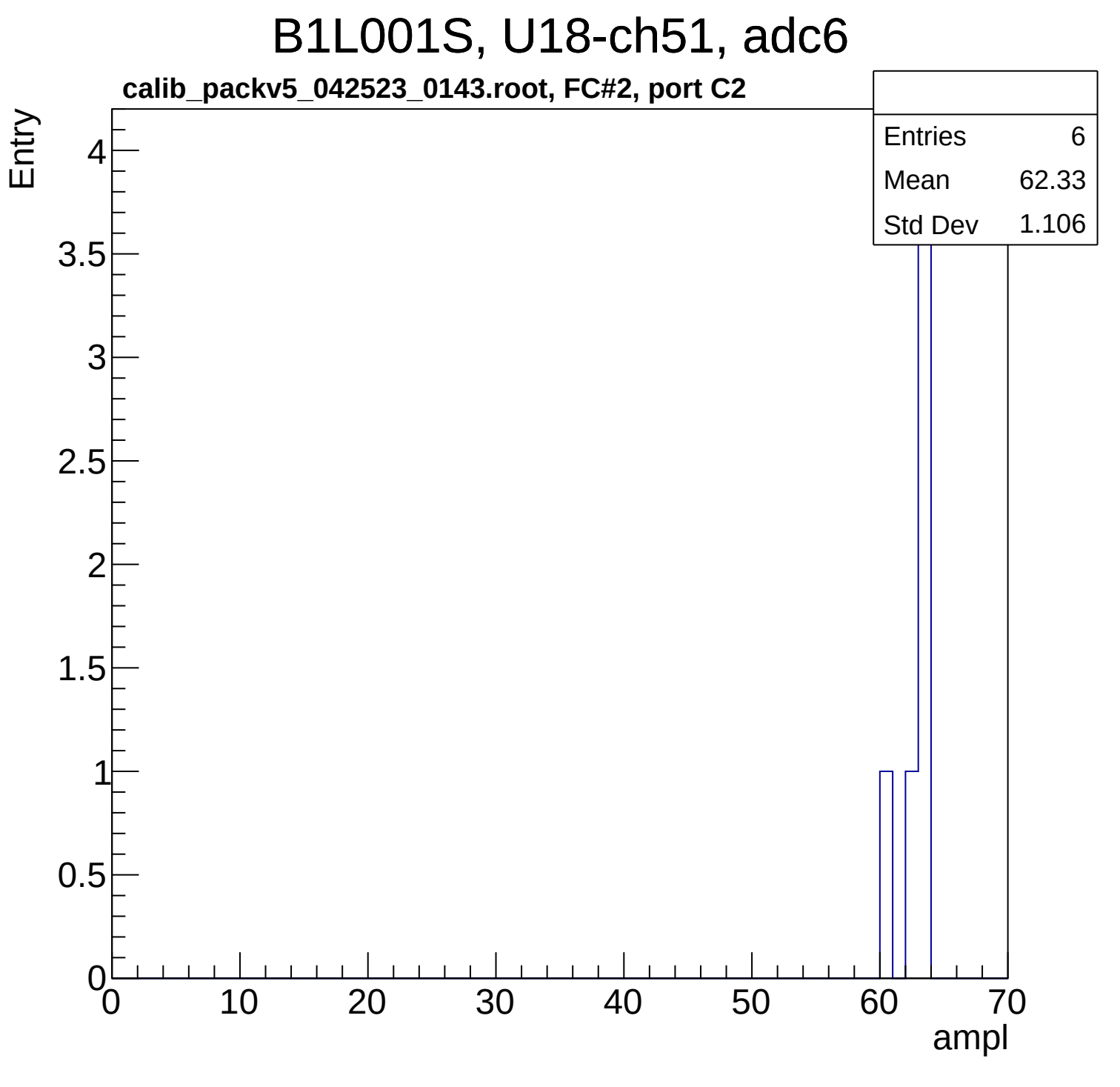

B1L001S, U18-ch51, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 151
Mean 35.91
Std Dev 3.516
Gaus mean : 36.2864
Gaus Width: 3.5390
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

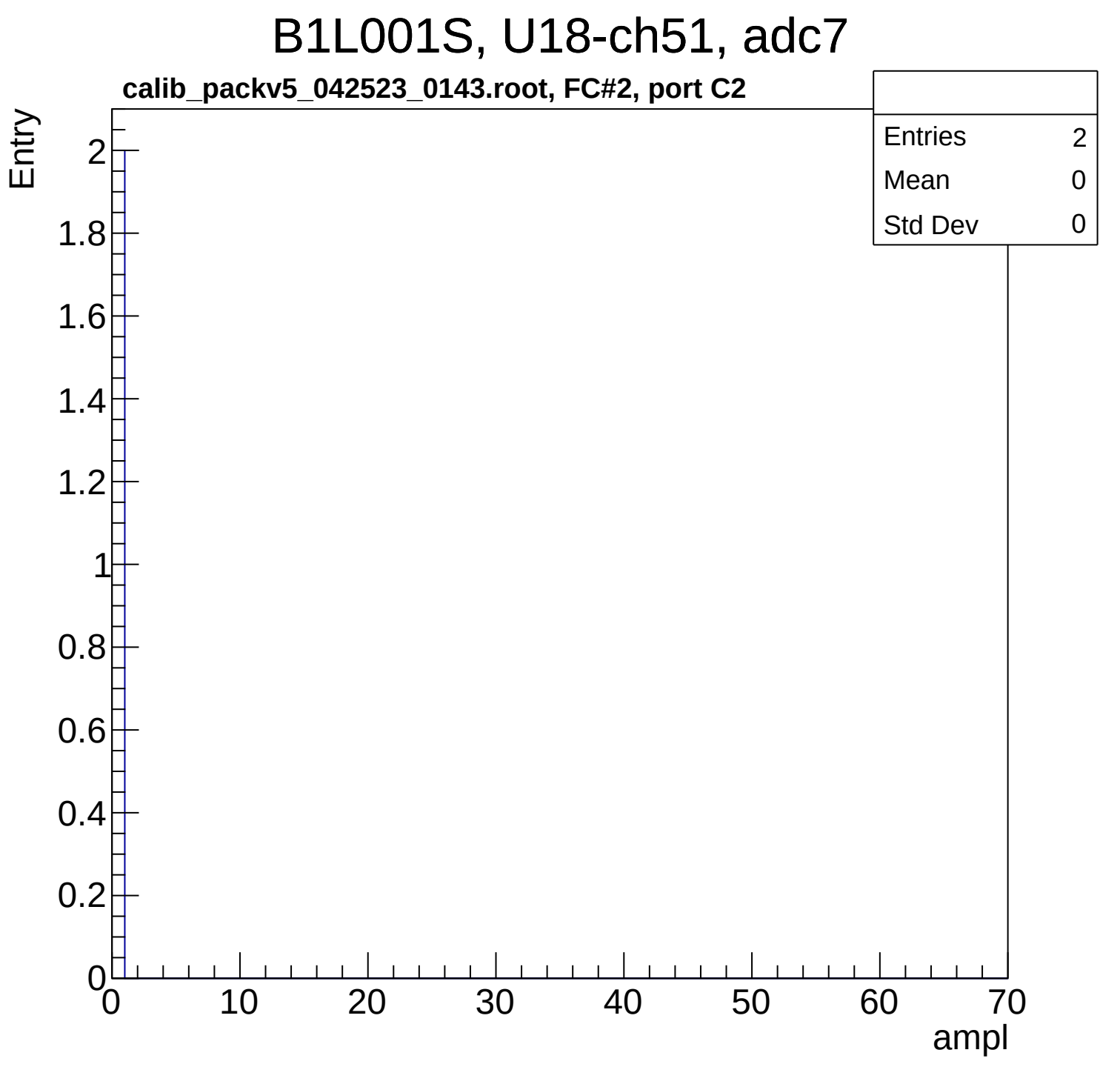

B1L001S, U18-ch51, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 139
Mean 43.34
Std Dev 3.173
Gaus mean : 43.8441
Gaus Width: 3.1835
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

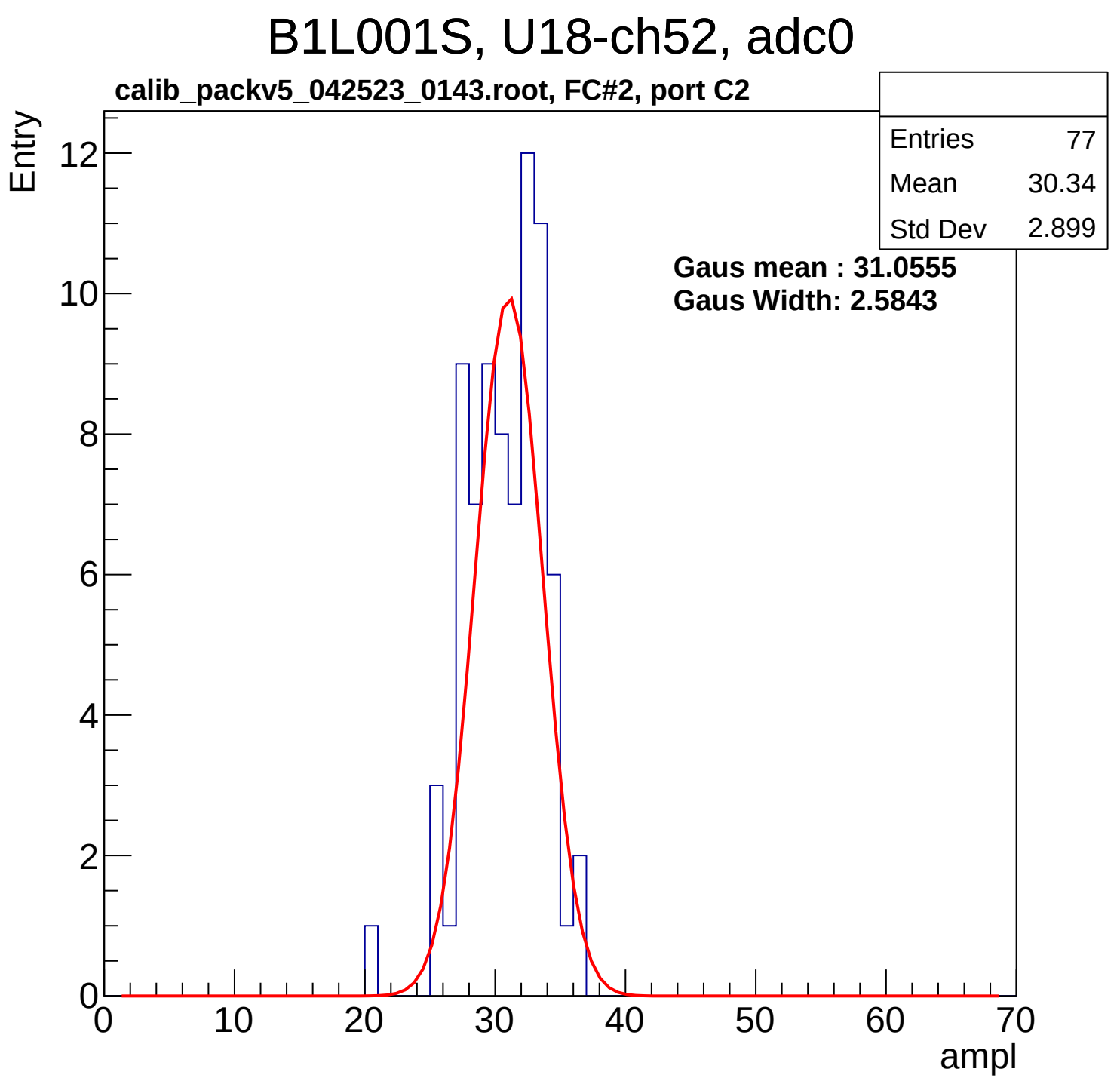

B1L001S, U18-ch51, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 129
Mean 50.12
Std Dev 3.453
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl

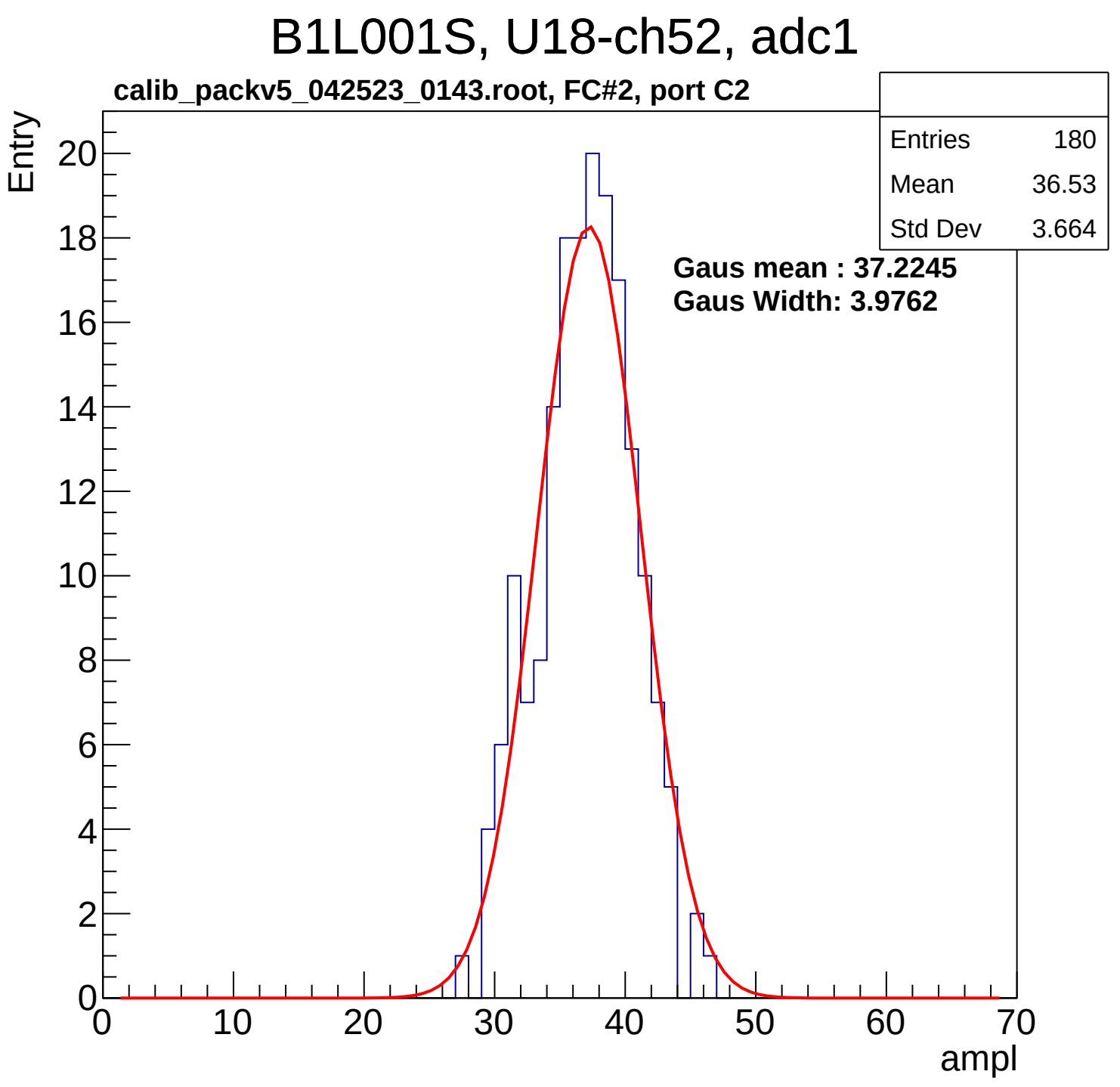

B1L001S, U18-ch51, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 104
Mean 55.64
Std Dev 3.013
Entry
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl

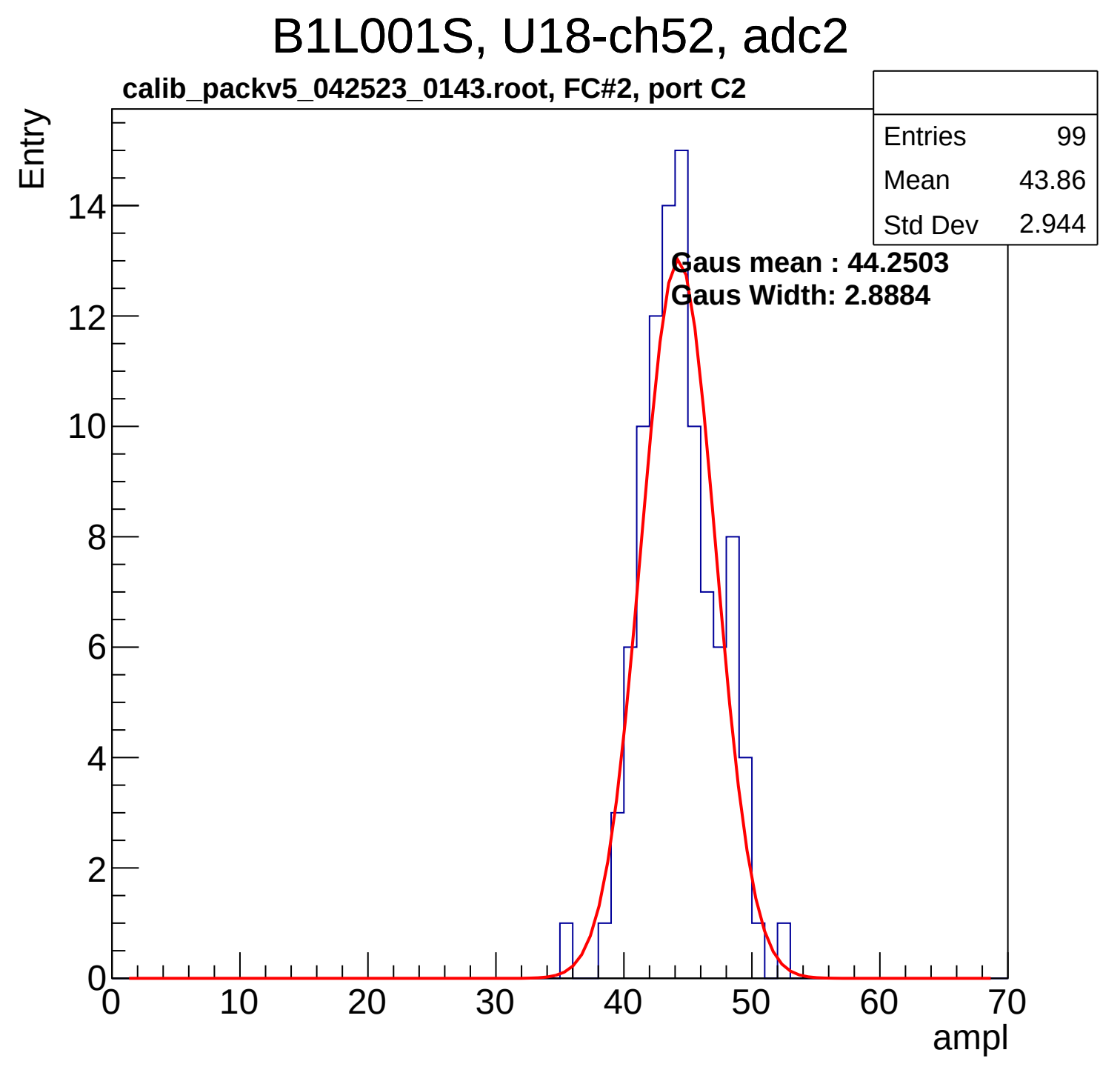

B1L001S, U18-ch51, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 97
Mean 59.01
Std Dev 8.819
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

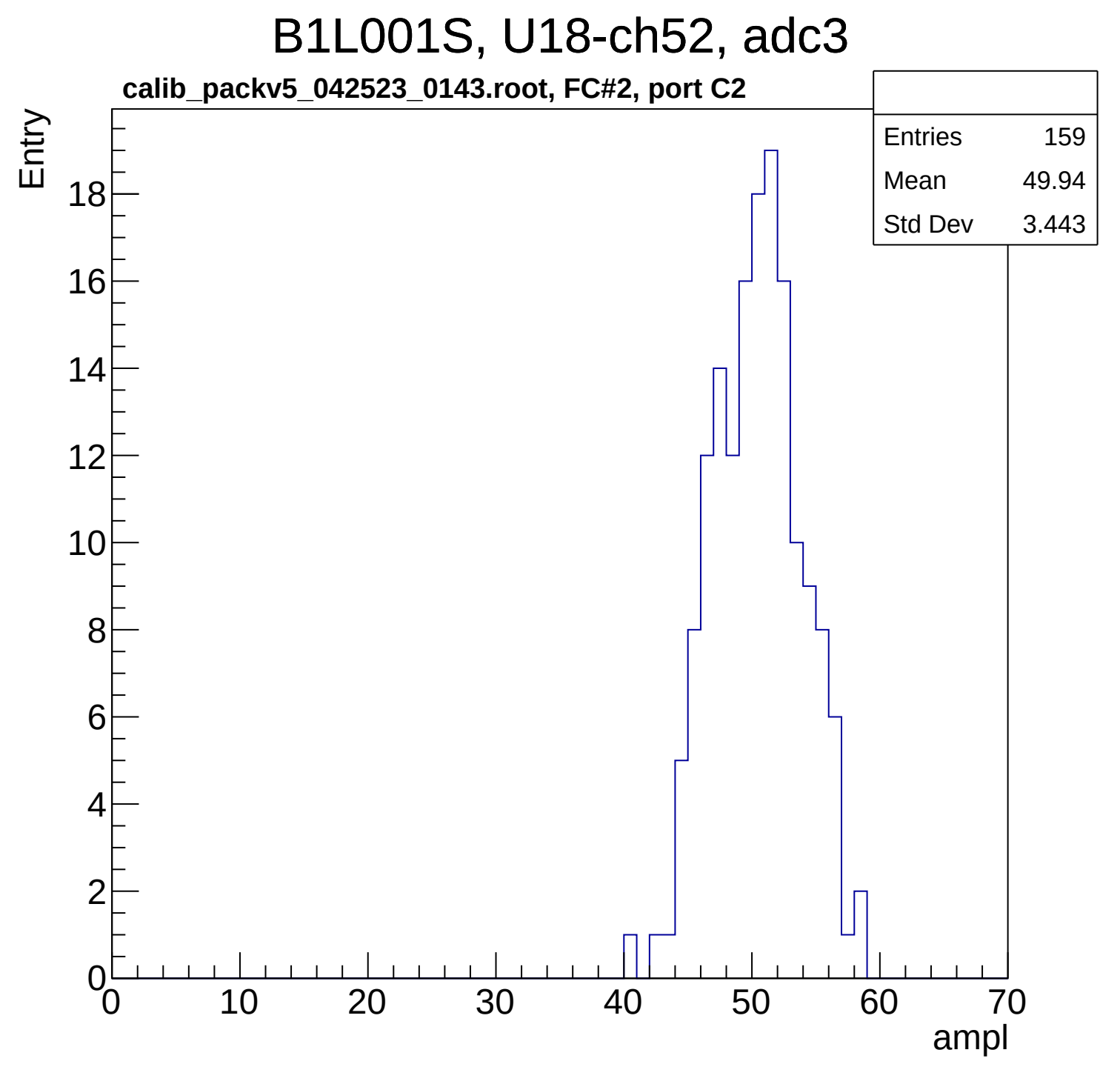

B1L001S, U18-ch51, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 6
Mean 62.33
Std Dev 1.106
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

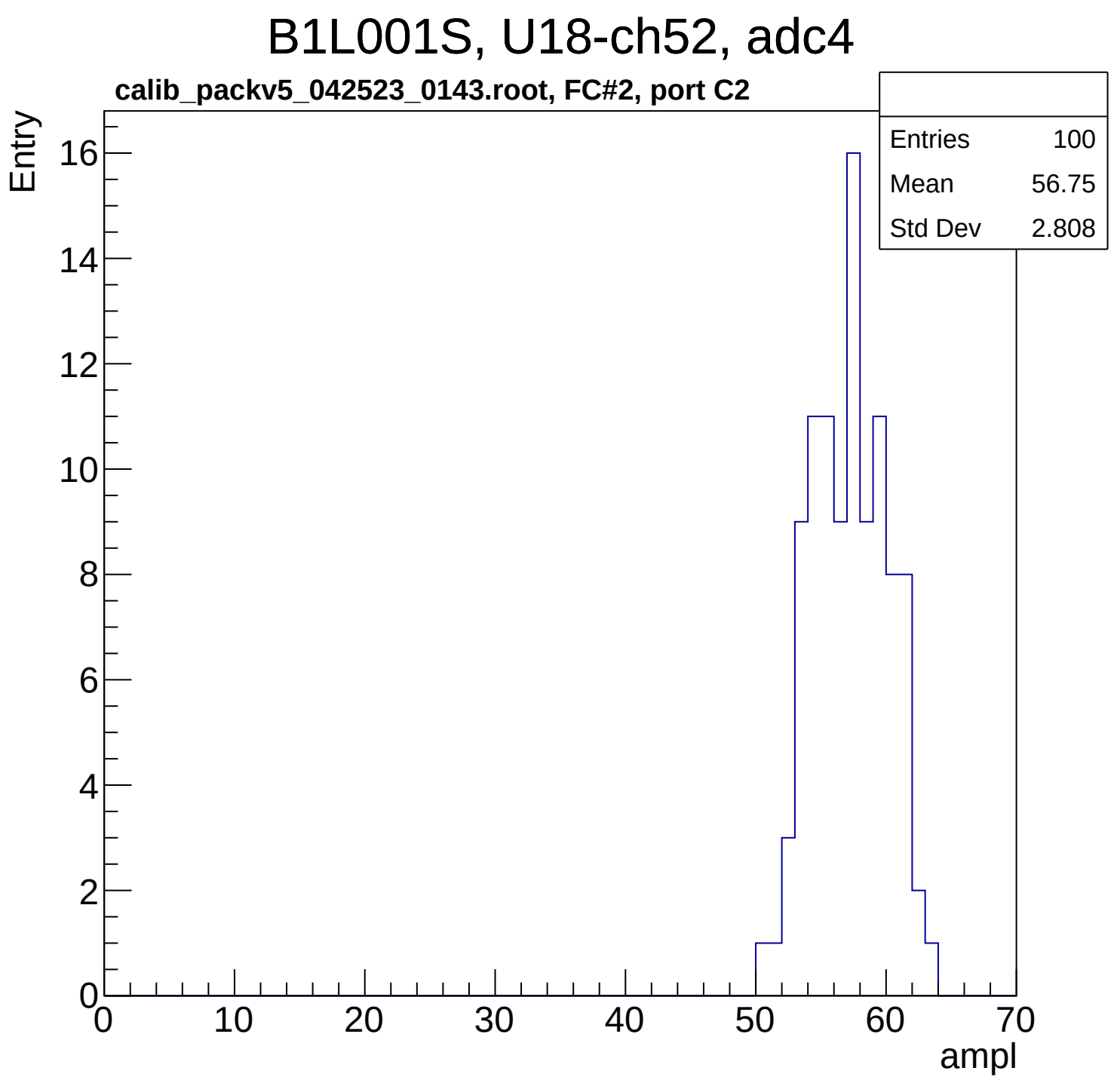

B1L001S, U18-ch51, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 0
Std Dev 0
Entry
2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

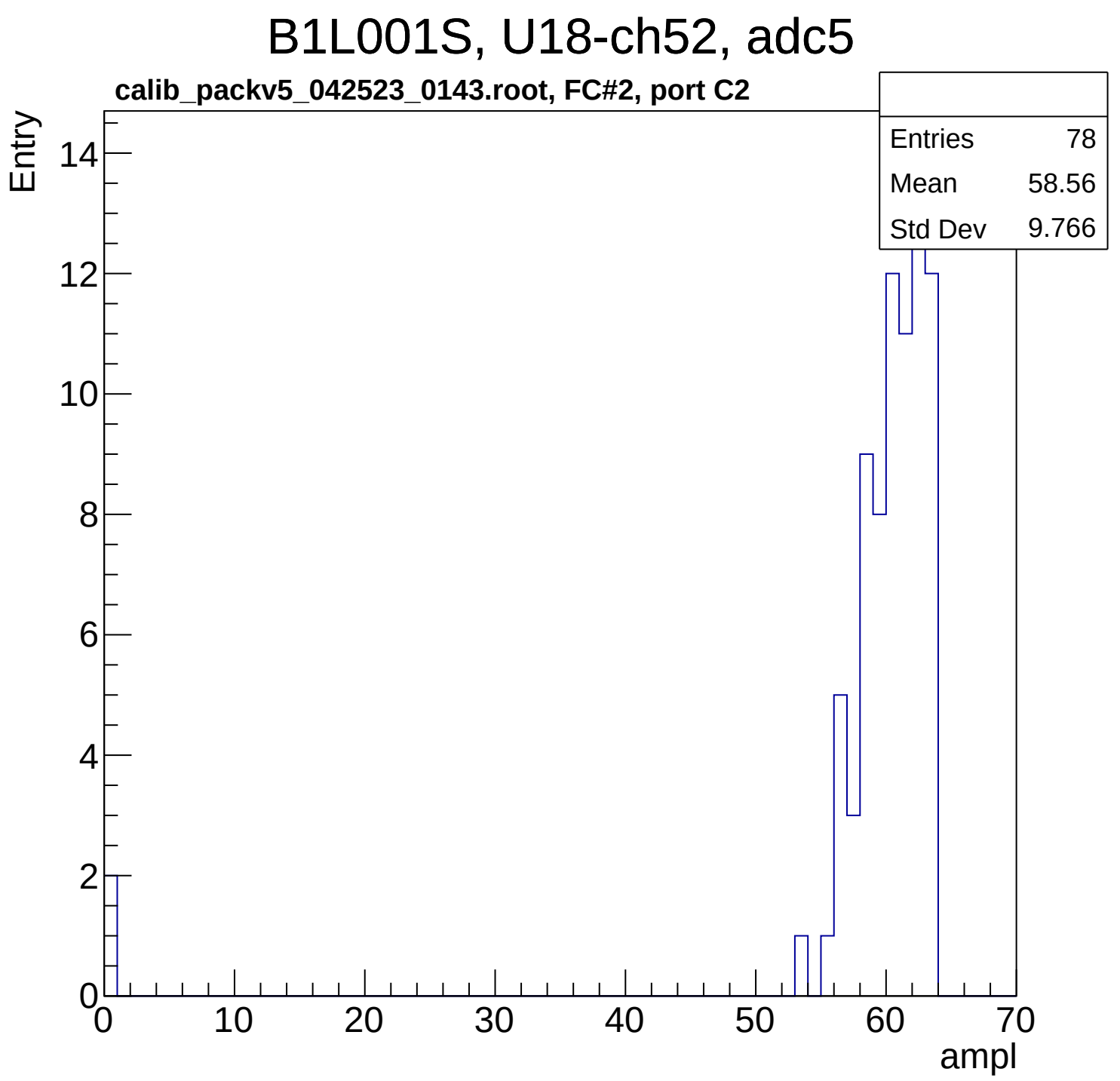

B1L001S, U18-ch52, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 77
Mean 30.34
Std Dev 2.899
Gaus mean : 31.0555
Gaus Width: 2.5843
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70

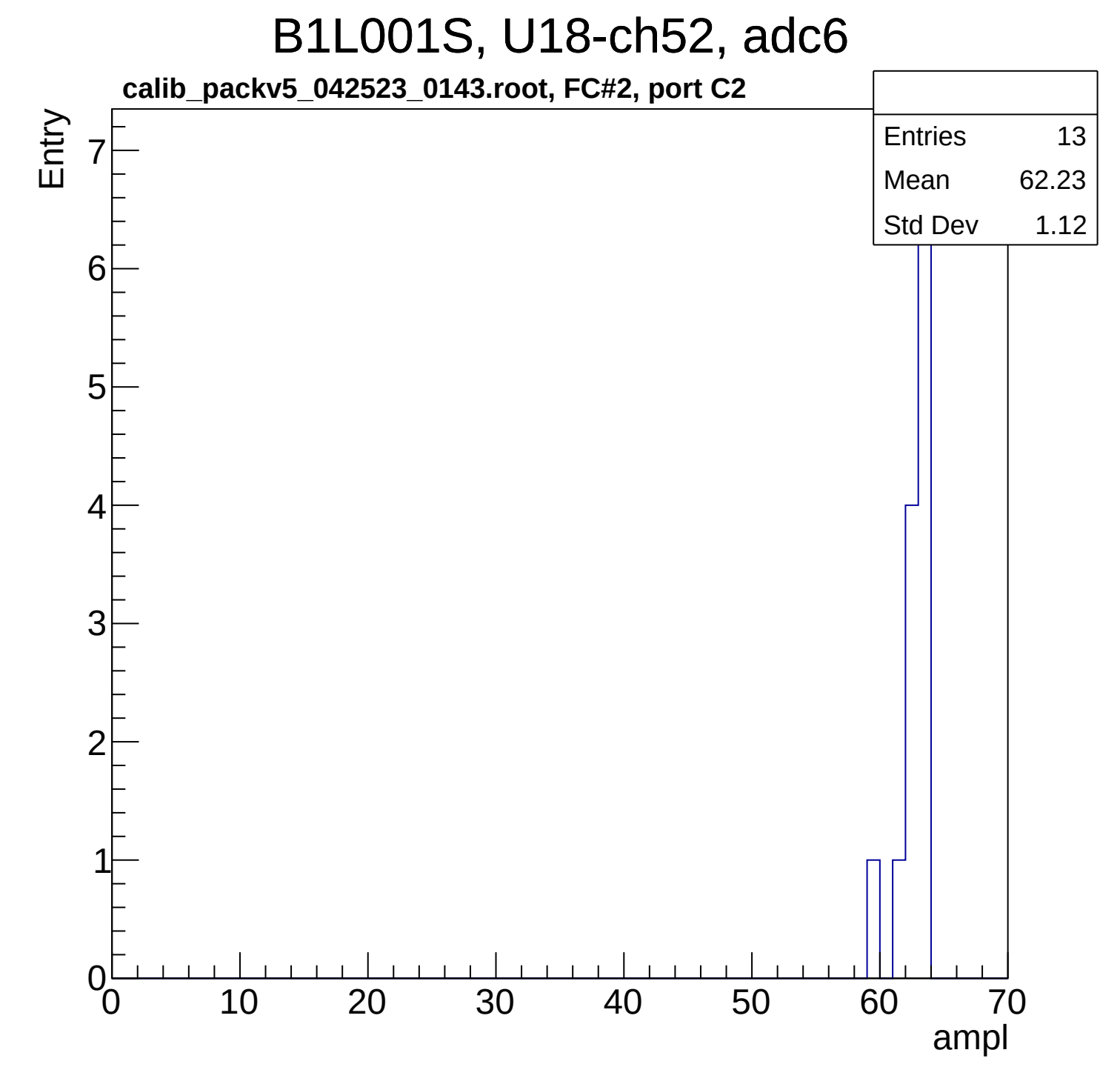

B1L001S, U18-ch52, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 180
Mean 36.53
Std Dev 3.664
Gaus mean : 37.2245
Gaus Width: 3.9762
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

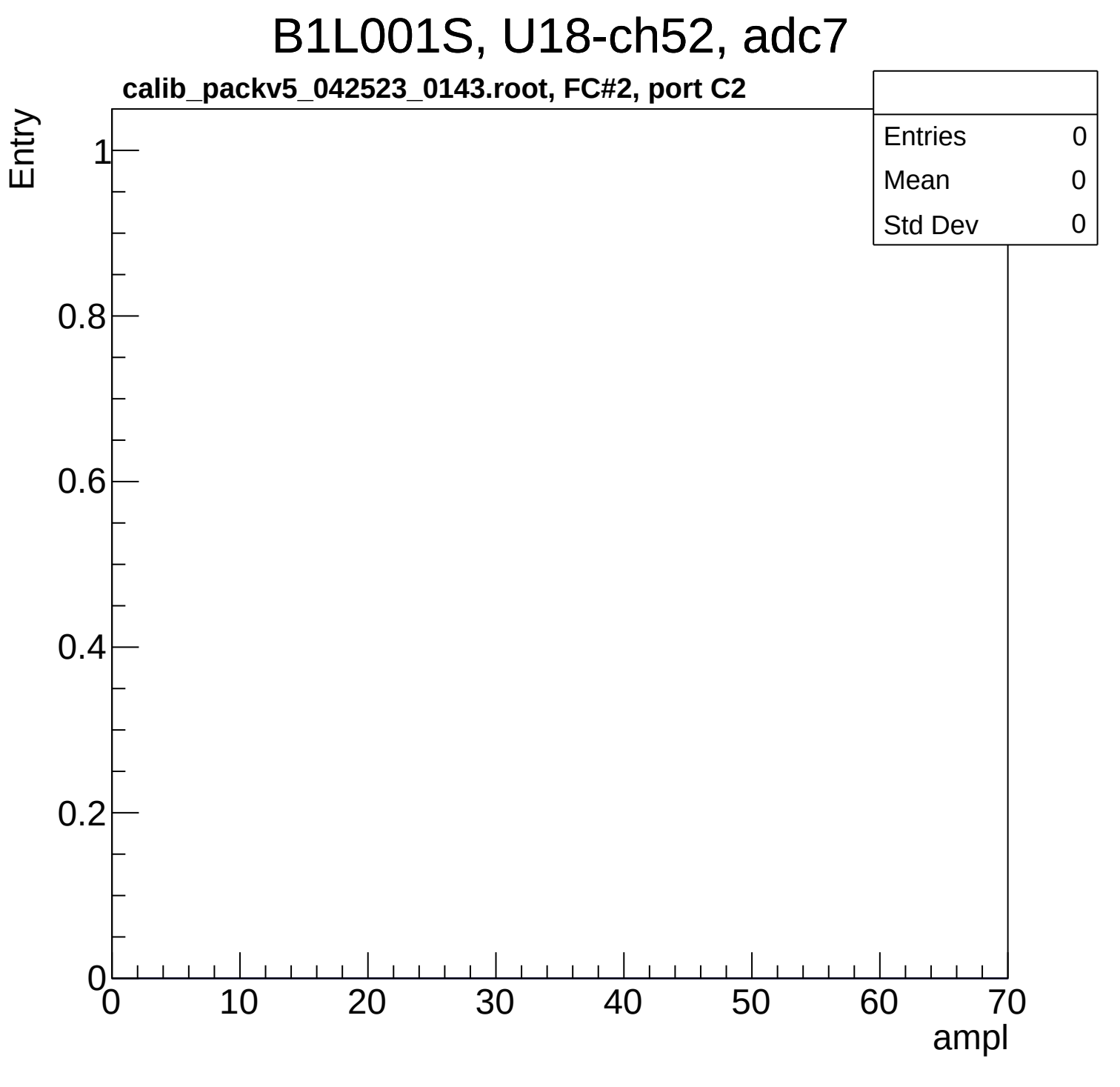

B1L001S, U18-ch52, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 99
Mean 43.86
Std Dev 2.944
Gaus mean : 44.2503
Gaus Width: 2.8884
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

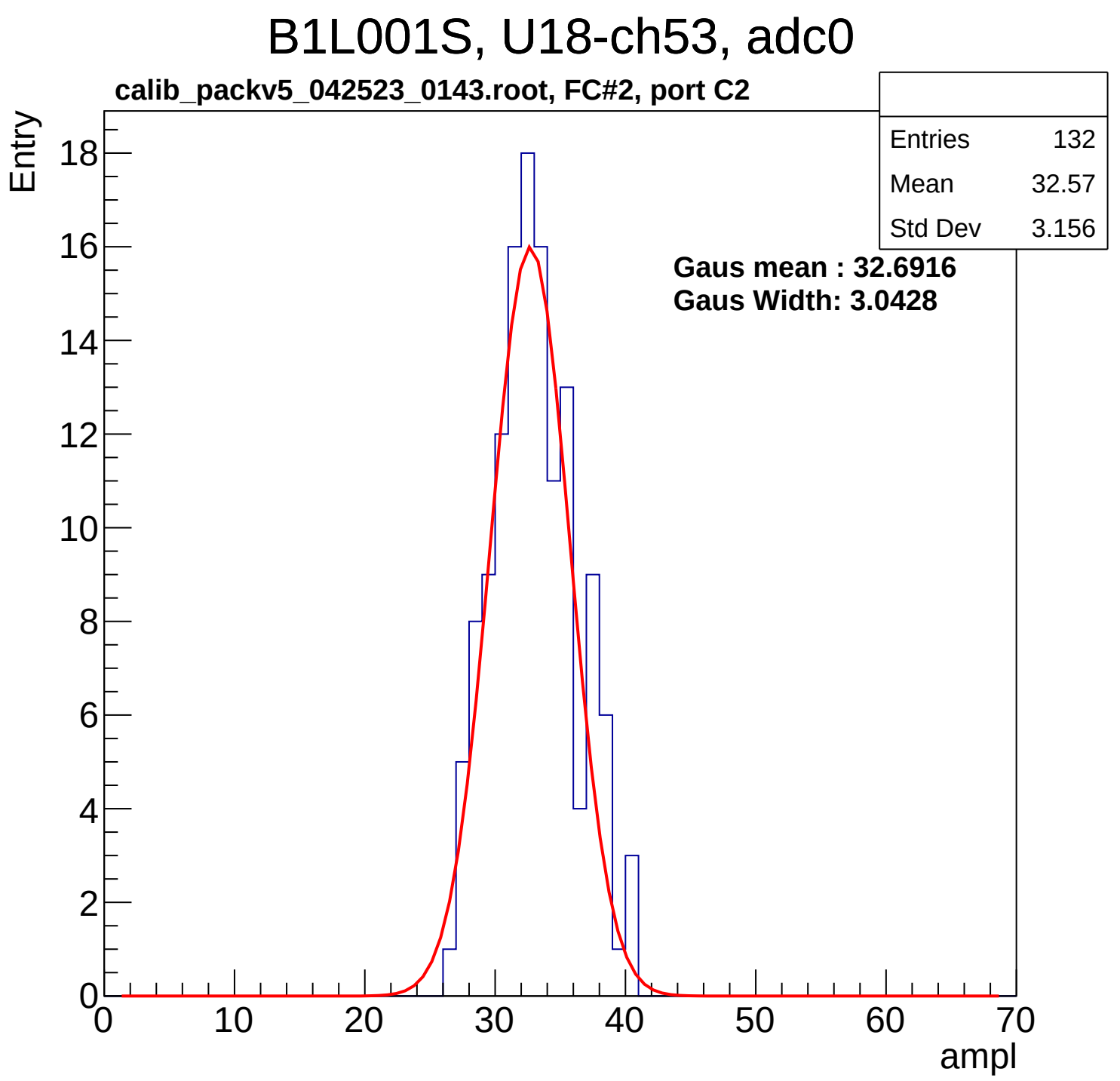

B1L001S, U18-ch52, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 159
Mean 49.94
Std Dev 3.443
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

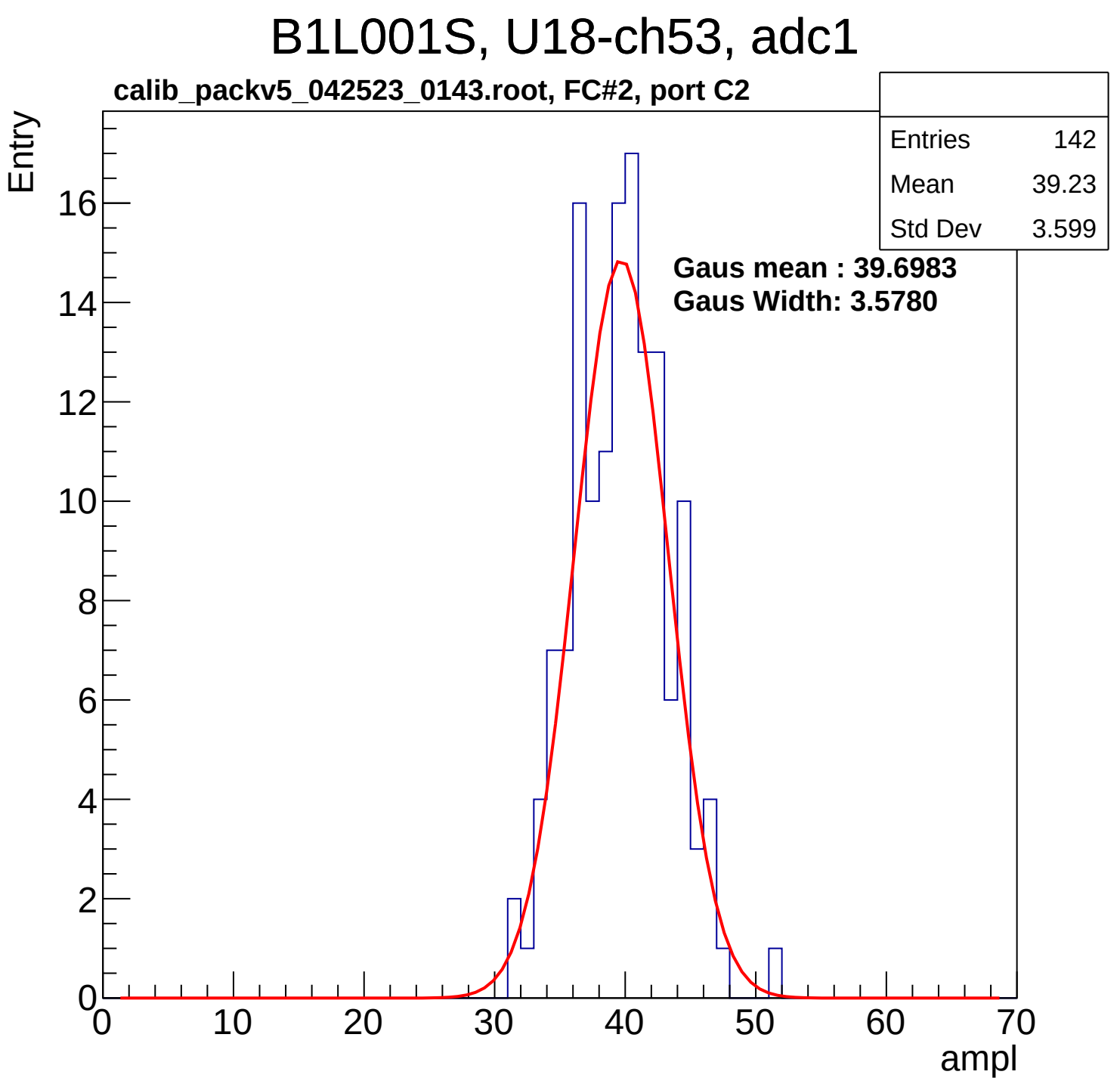

B1L001S, U18-ch52, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 100
Mean 56.75
Std Dev 2.808
Entry
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl

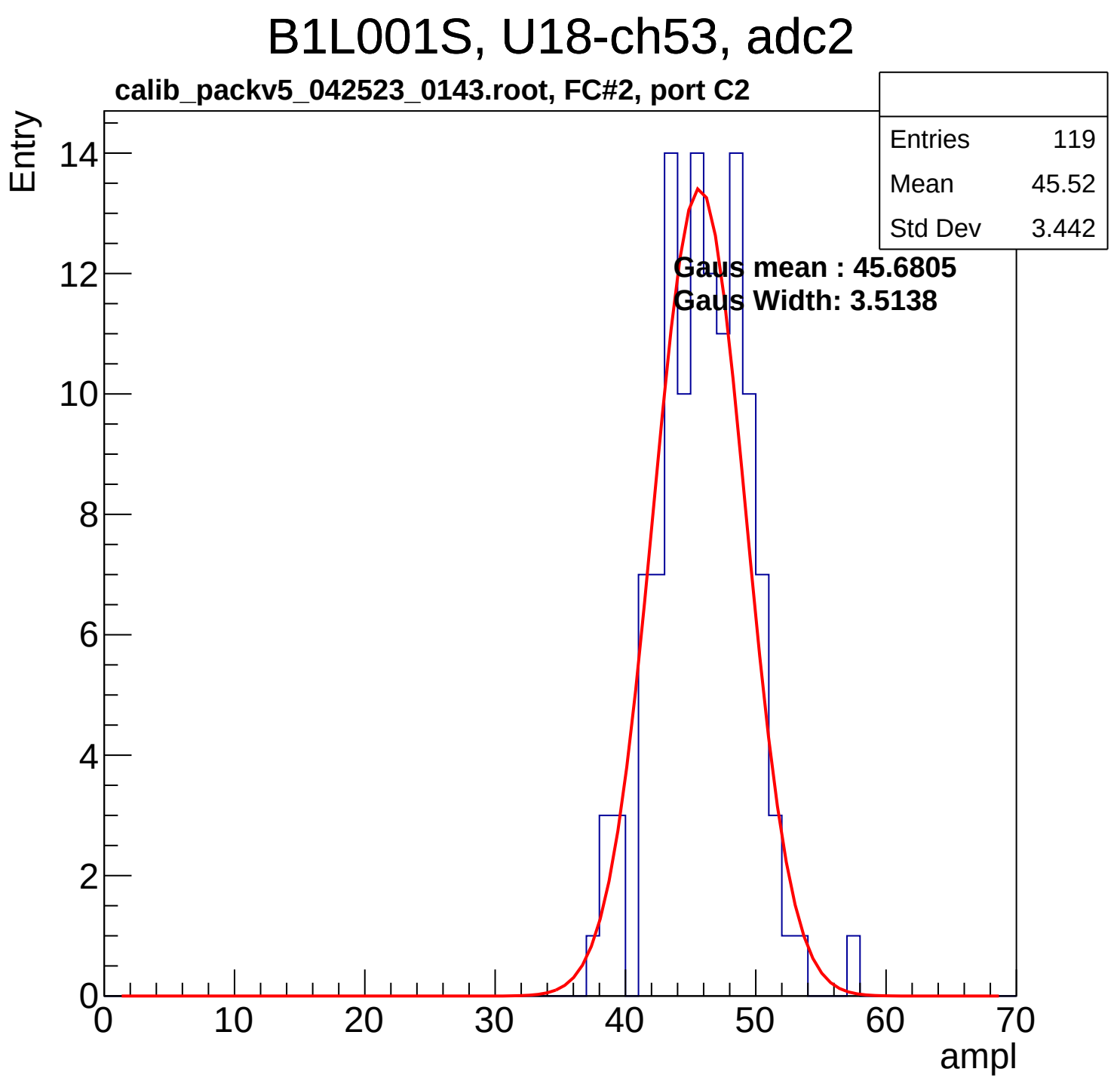

B1L001S, U18-ch52, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 78
Mean 58.56
Std Dev 9.766
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

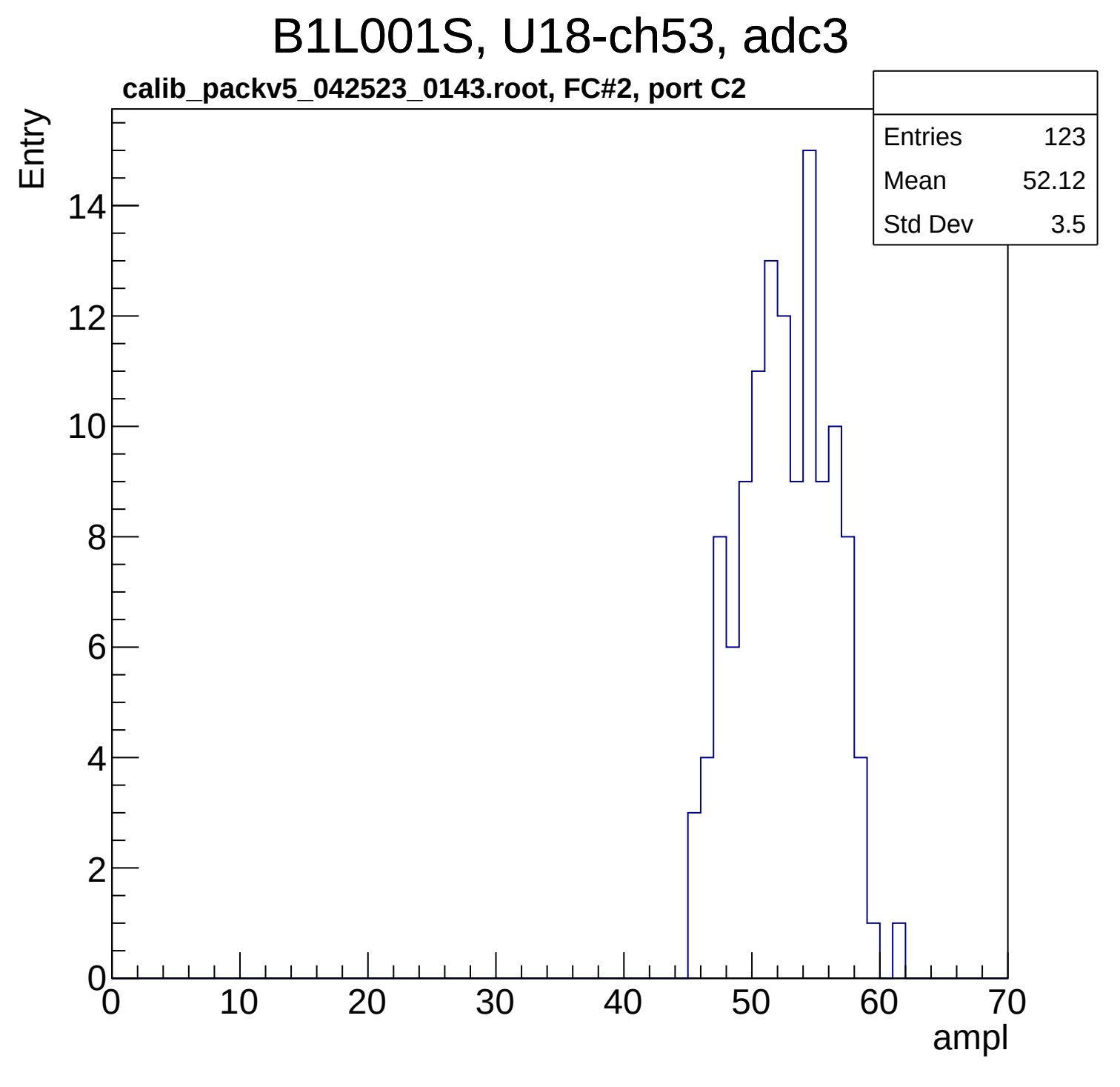

B1L001S, U18-ch52, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 13
Mean 62.23
Std Dev 1.12
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

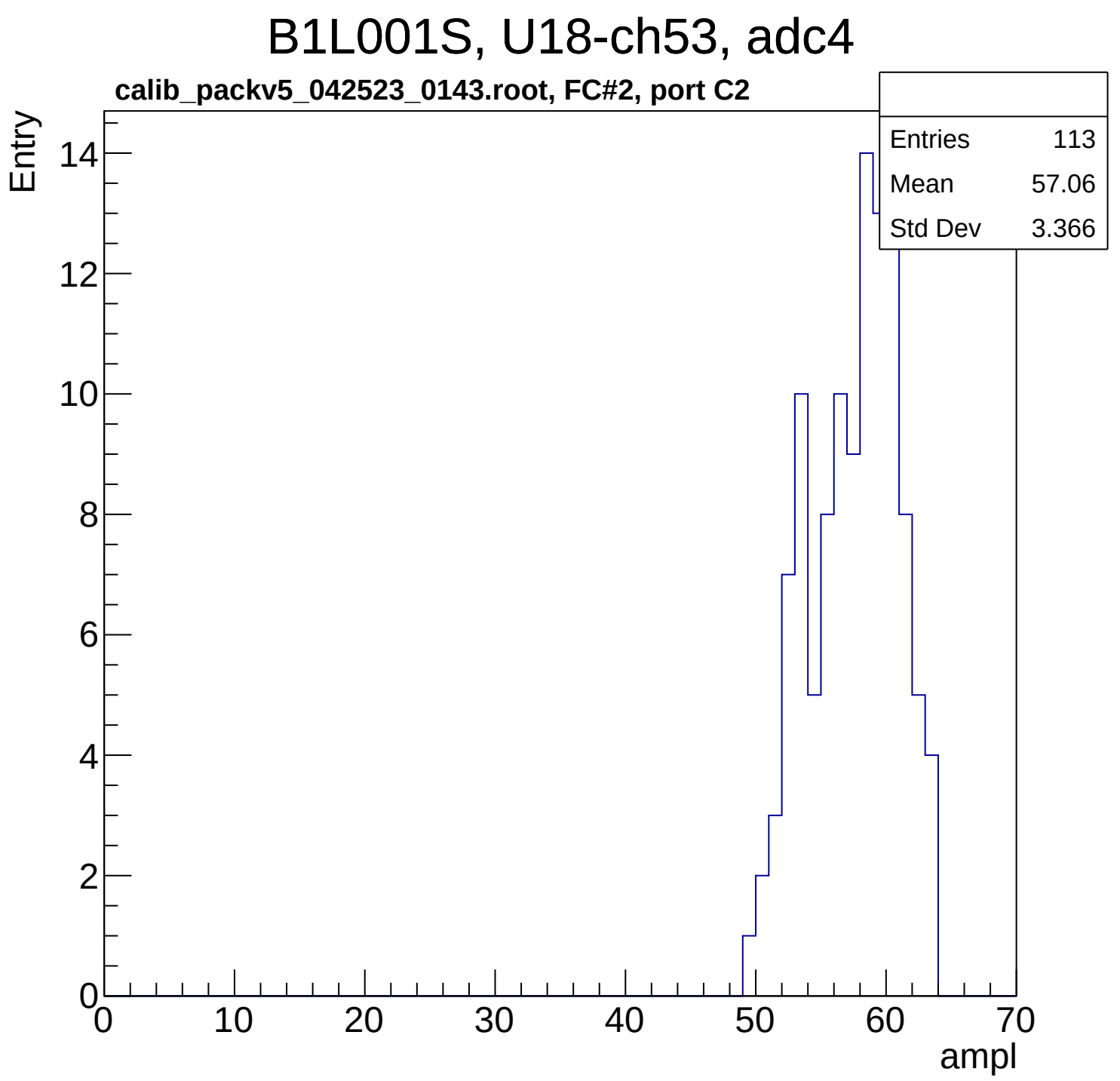

B1L001S, U18-ch52, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

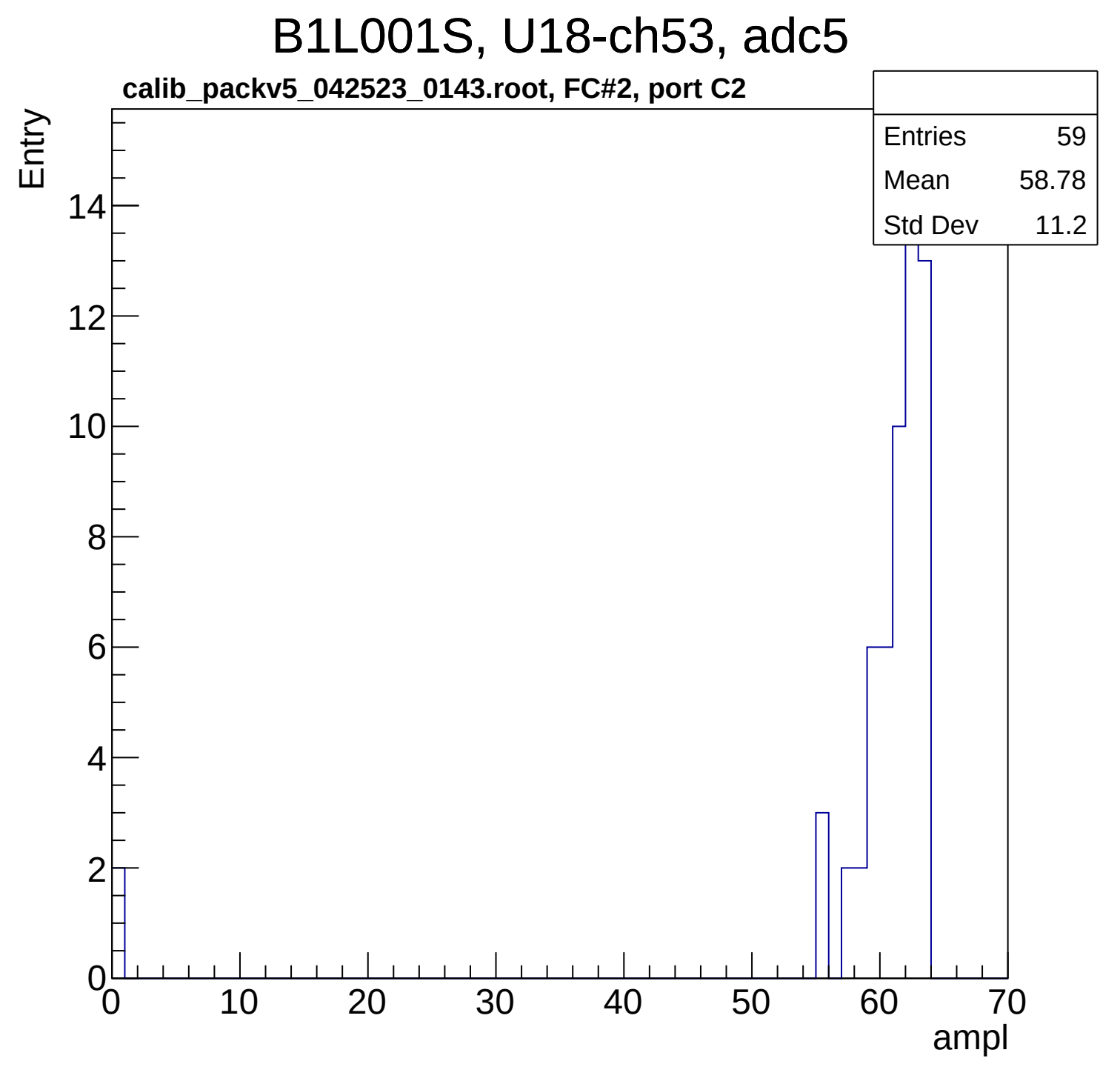

B1L001S, U18-ch53, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 132
Mean 32.57
Std Dev 3.156
Gaus mean : 32.6916
Gaus Width: 3.0428
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

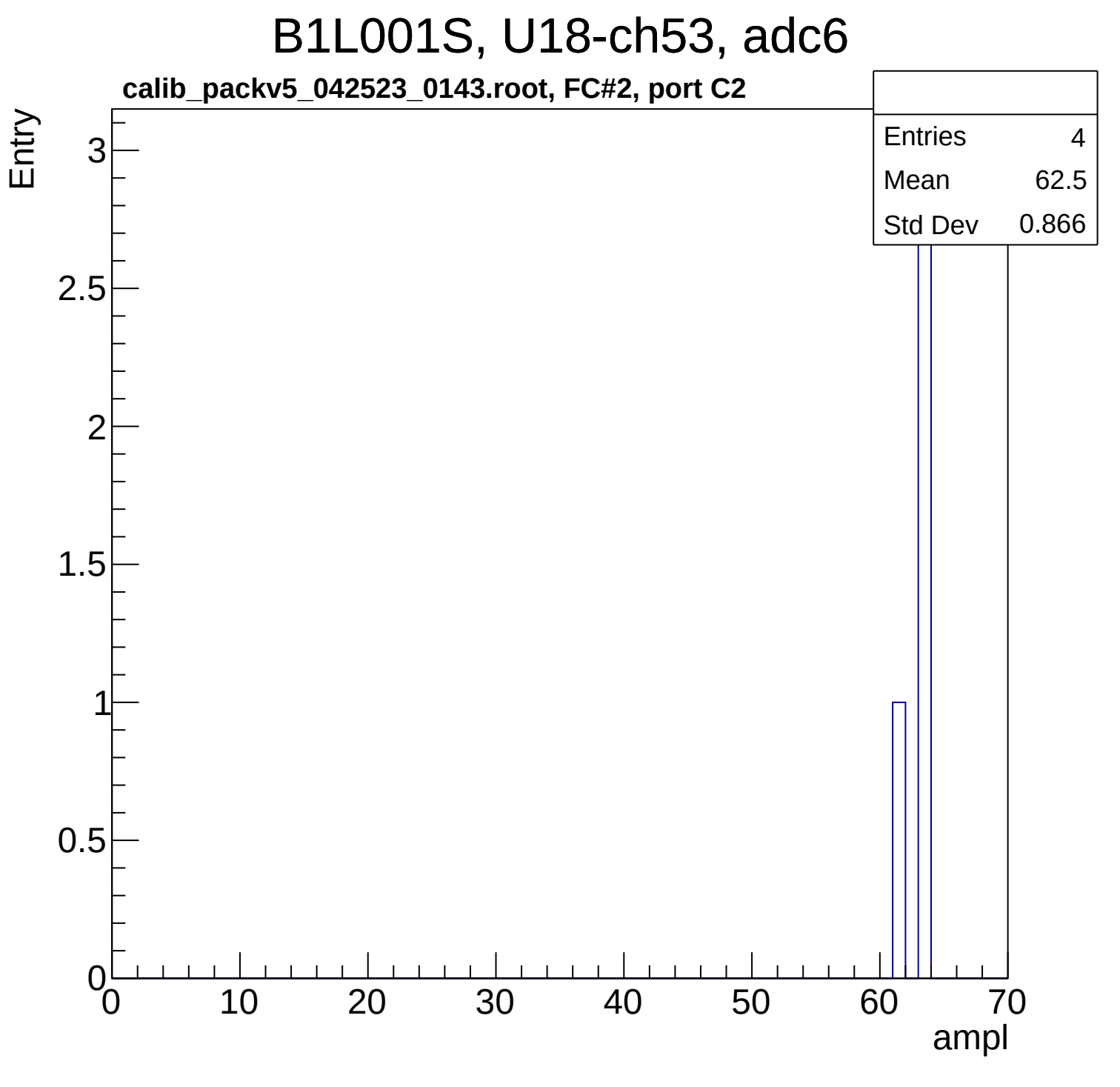

B1L001S, U18-ch53, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 142
Mean 39.23
Std Dev 3.599
Gaus mean : 39.6983
Gaus Width: 3.5780
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

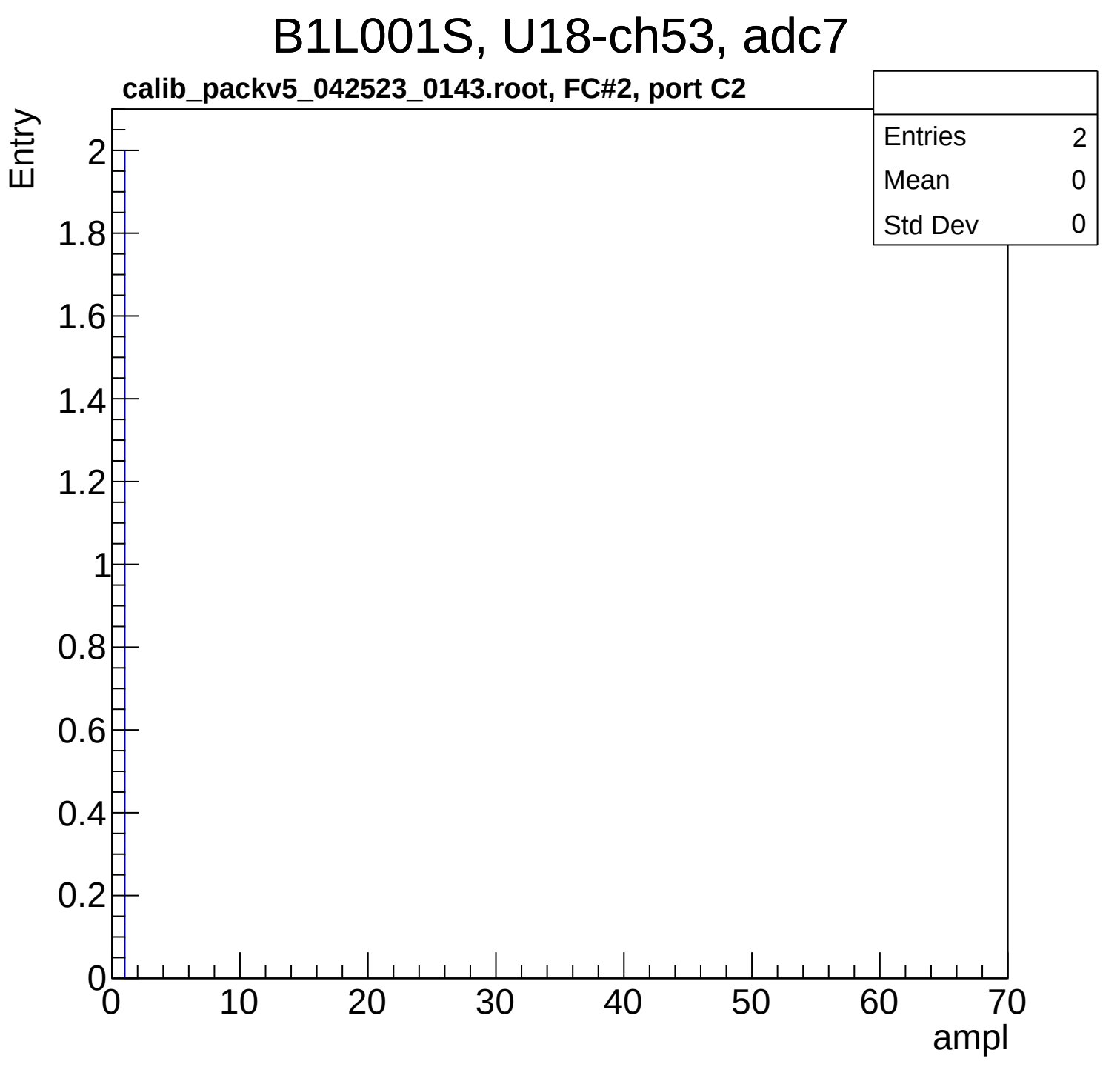

B1L001S, U18-ch53, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 119
Mean 45.52
Std Dev 3.442
Gaus mean : 45.6805
Gaus Width: 3.5138
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

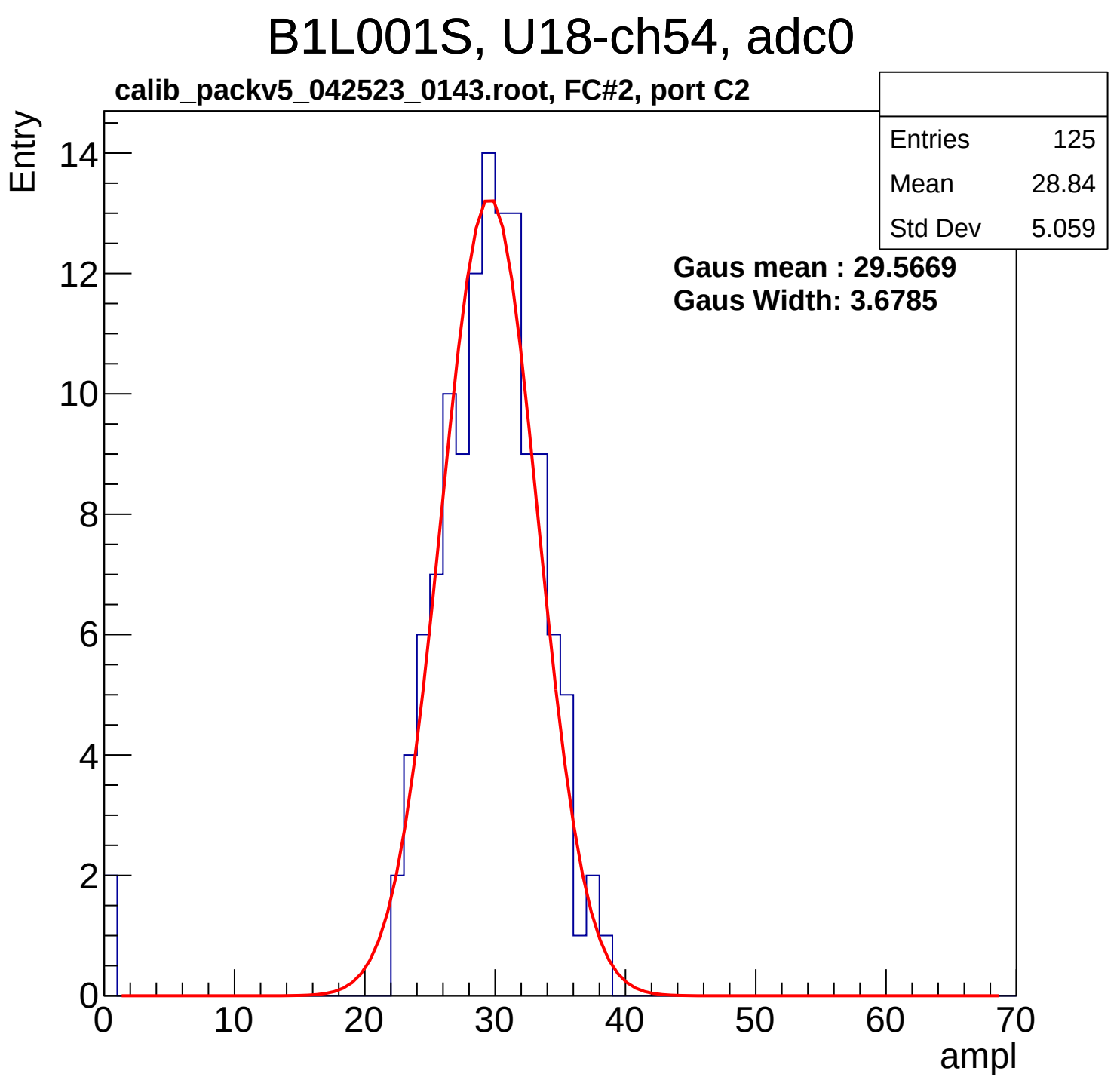

B1L001S, U18-ch53, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 123
Mean 52.12
Std Dev 3.5
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl

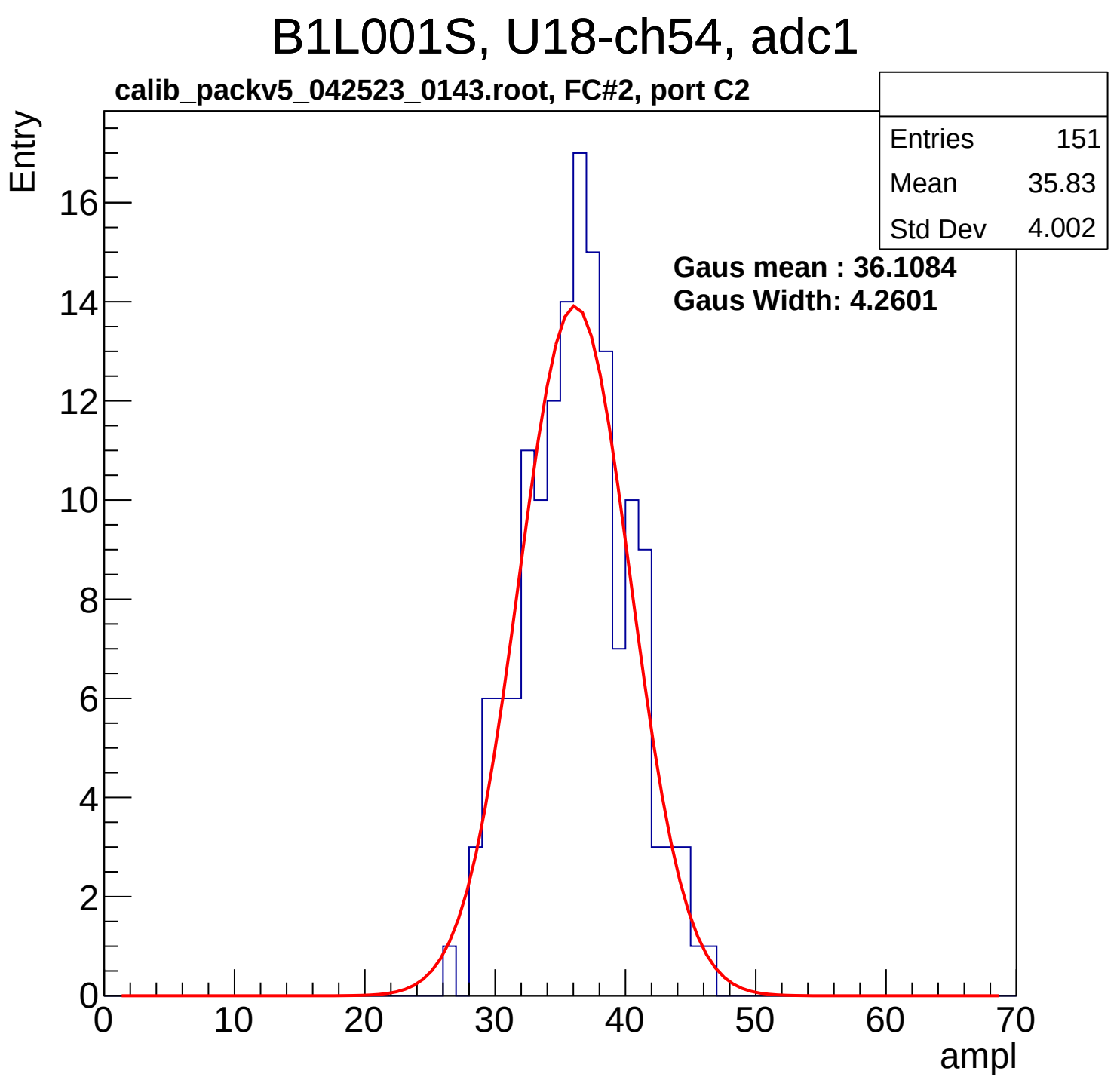

B1L001S, U18-ch53, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 113
Mean 57.06
Std Dev 3.366
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

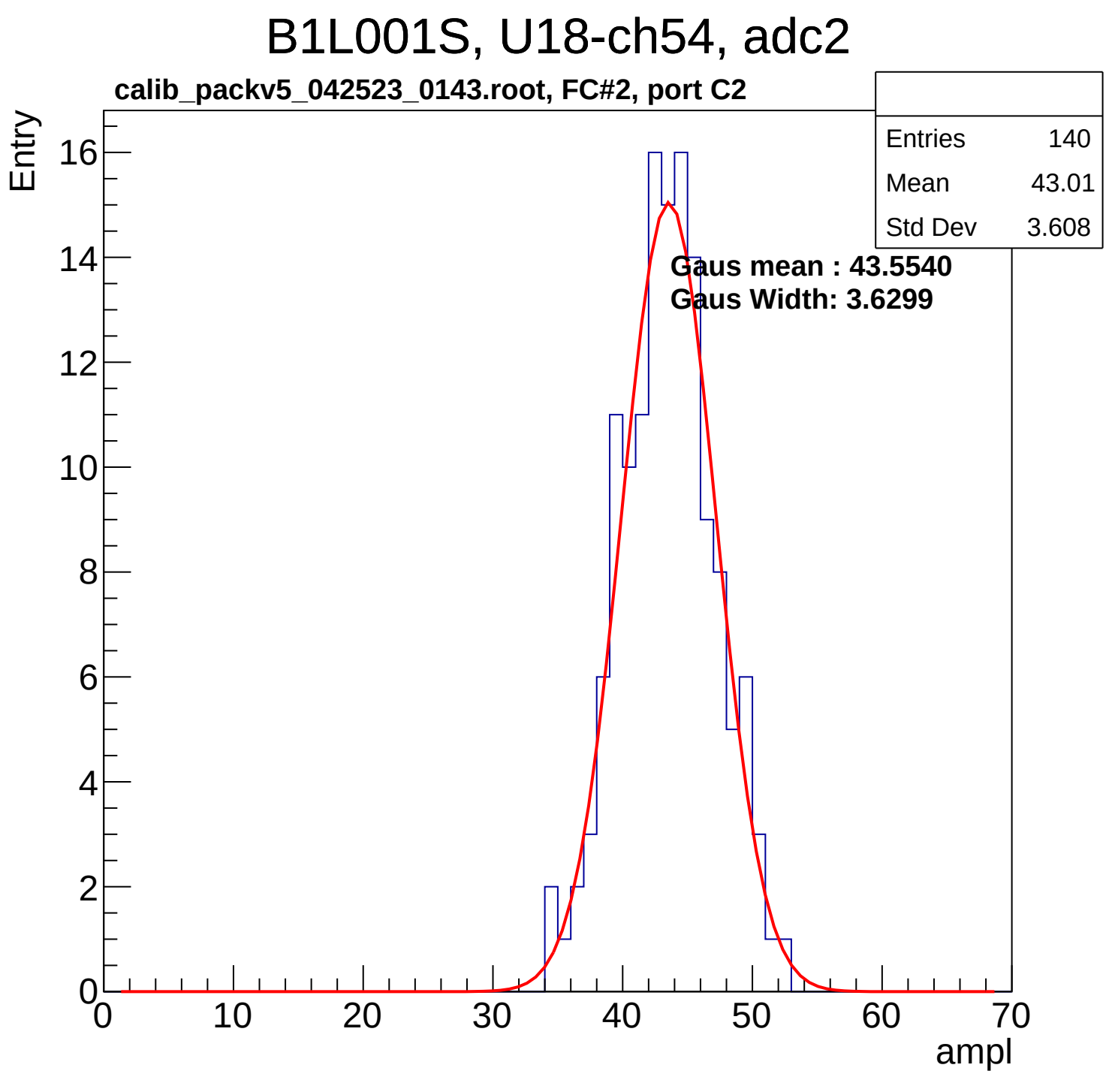

B1L001S, U18-ch53, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 59
Mean 58.78
Std Dev 11.2
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl

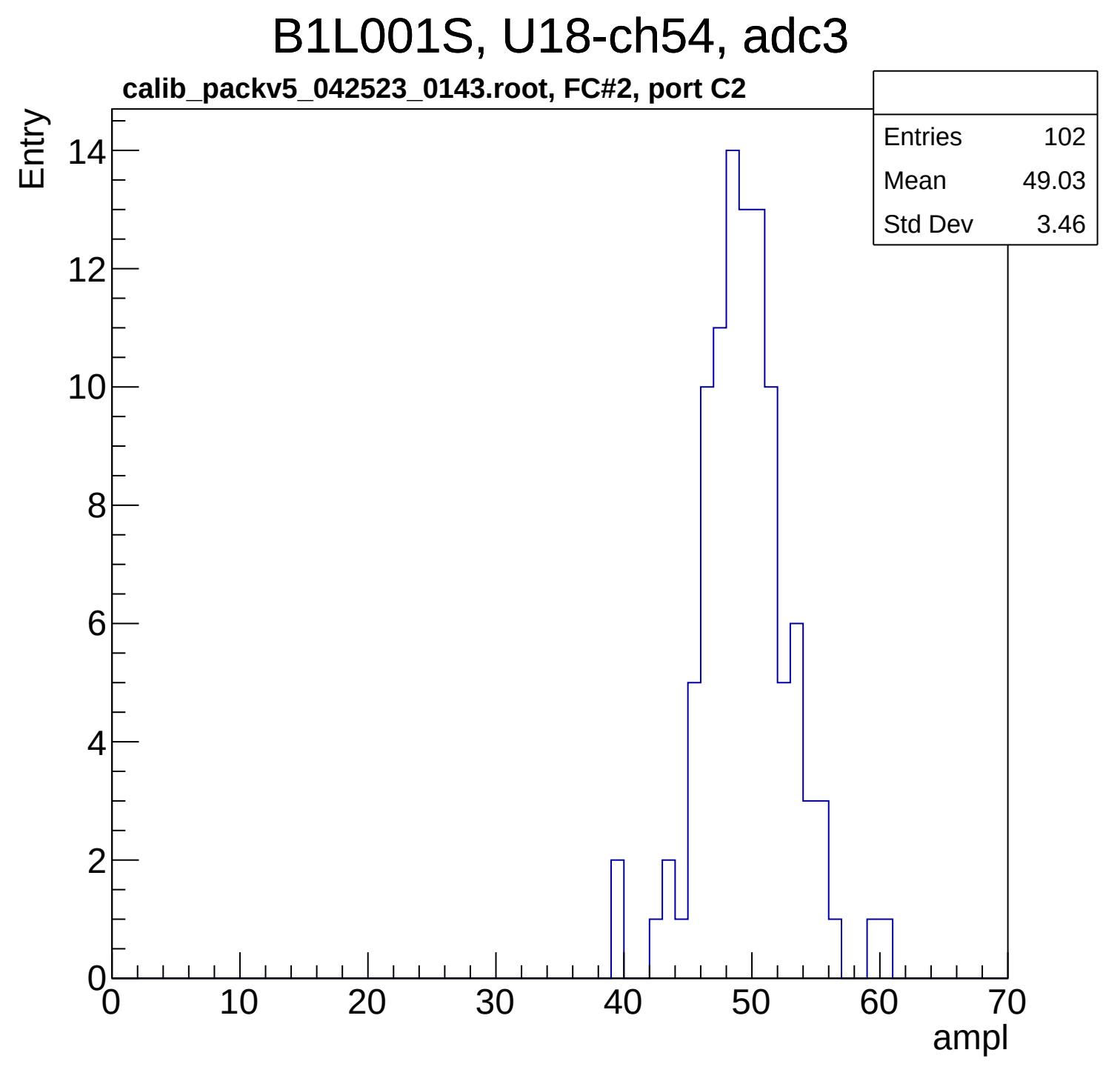

B1L001S, U18-ch53, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 4
Mean 62.5
Std Dev 0.866
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

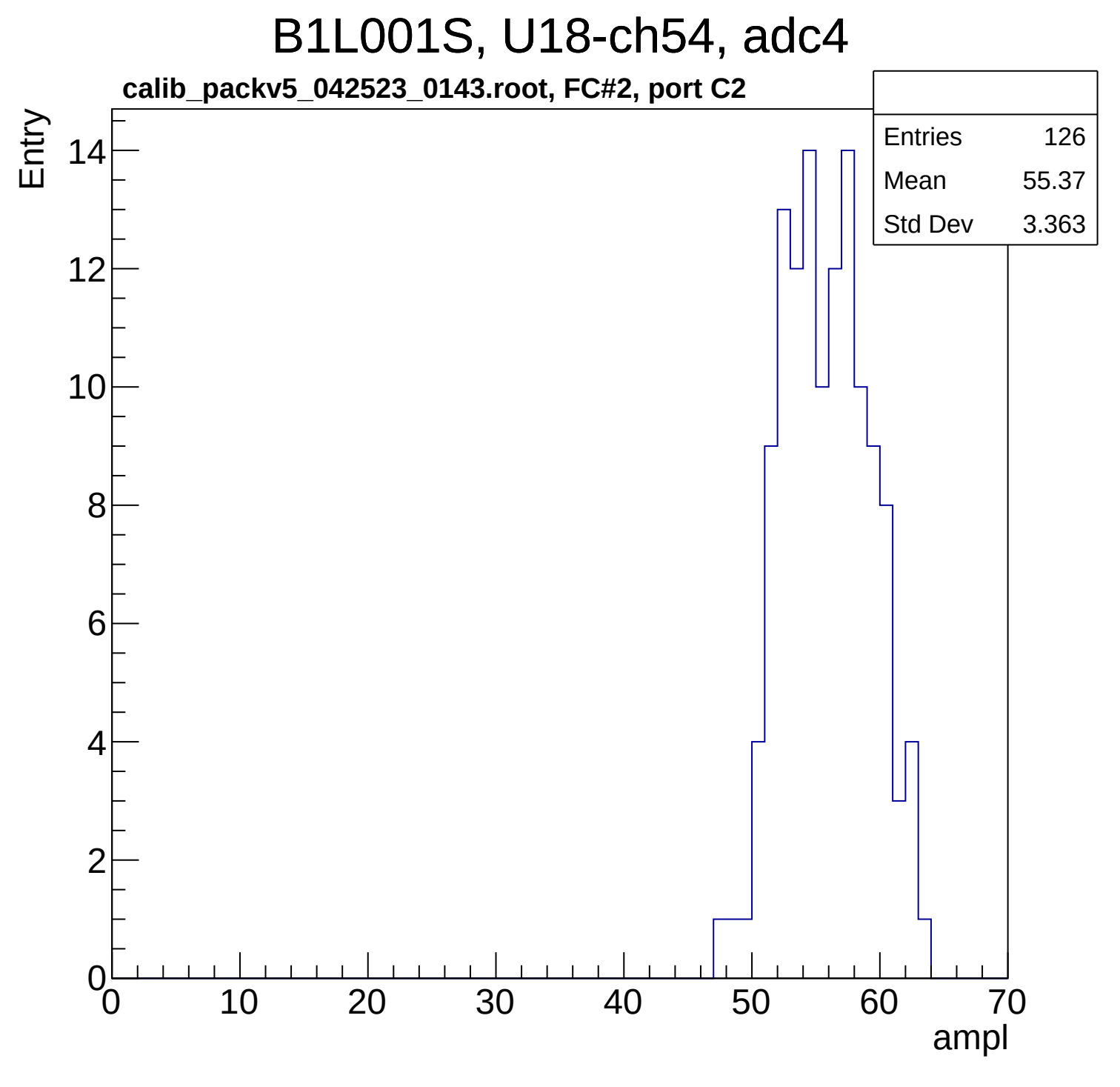

B1L001S, U18-ch53, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 0
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

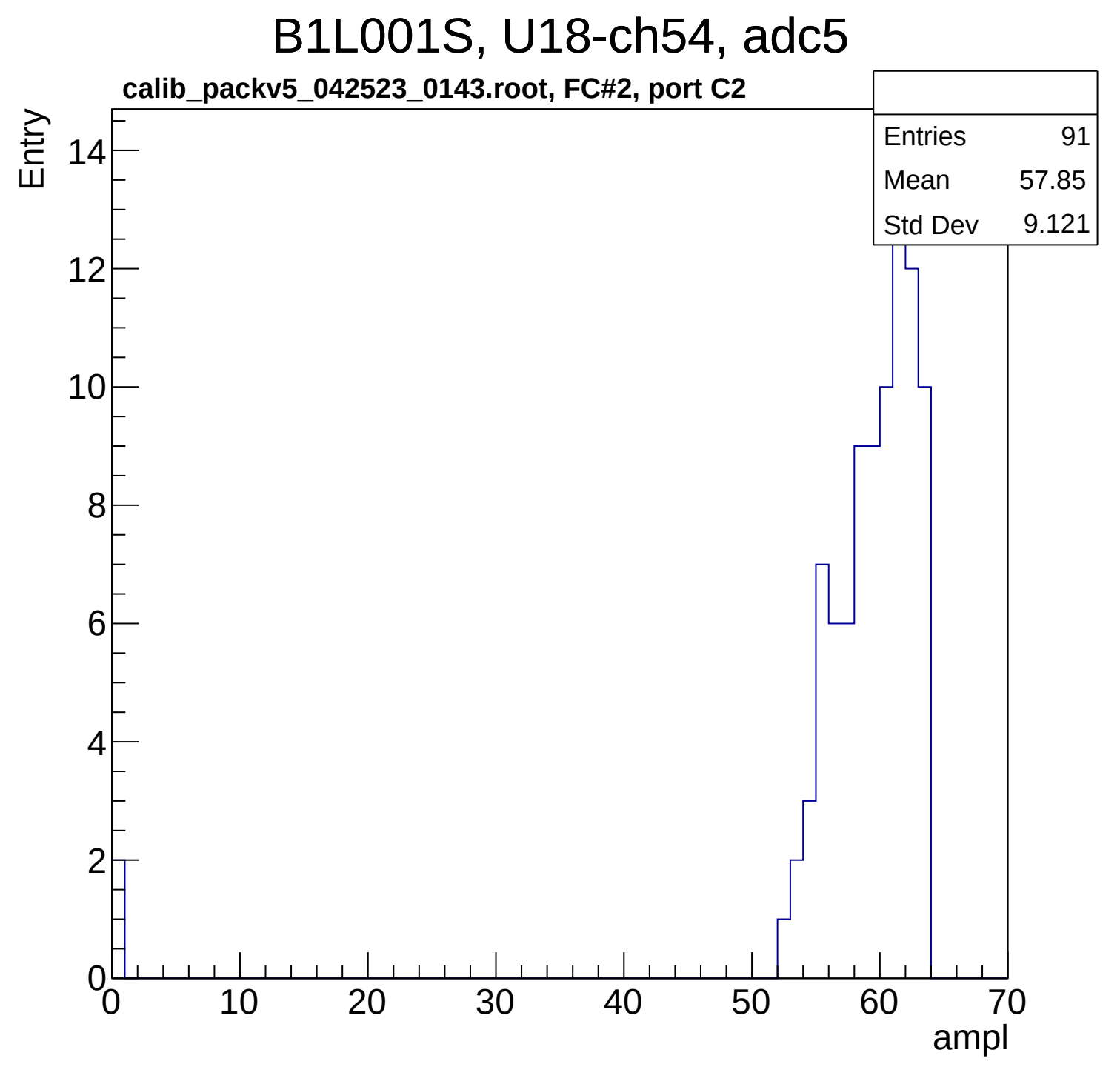

B1L001S, U18-ch54, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 125
Mean 28.84
Std Dev 5.059
Gaus mean : 29.5669
Gaus Width: 3.6785
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

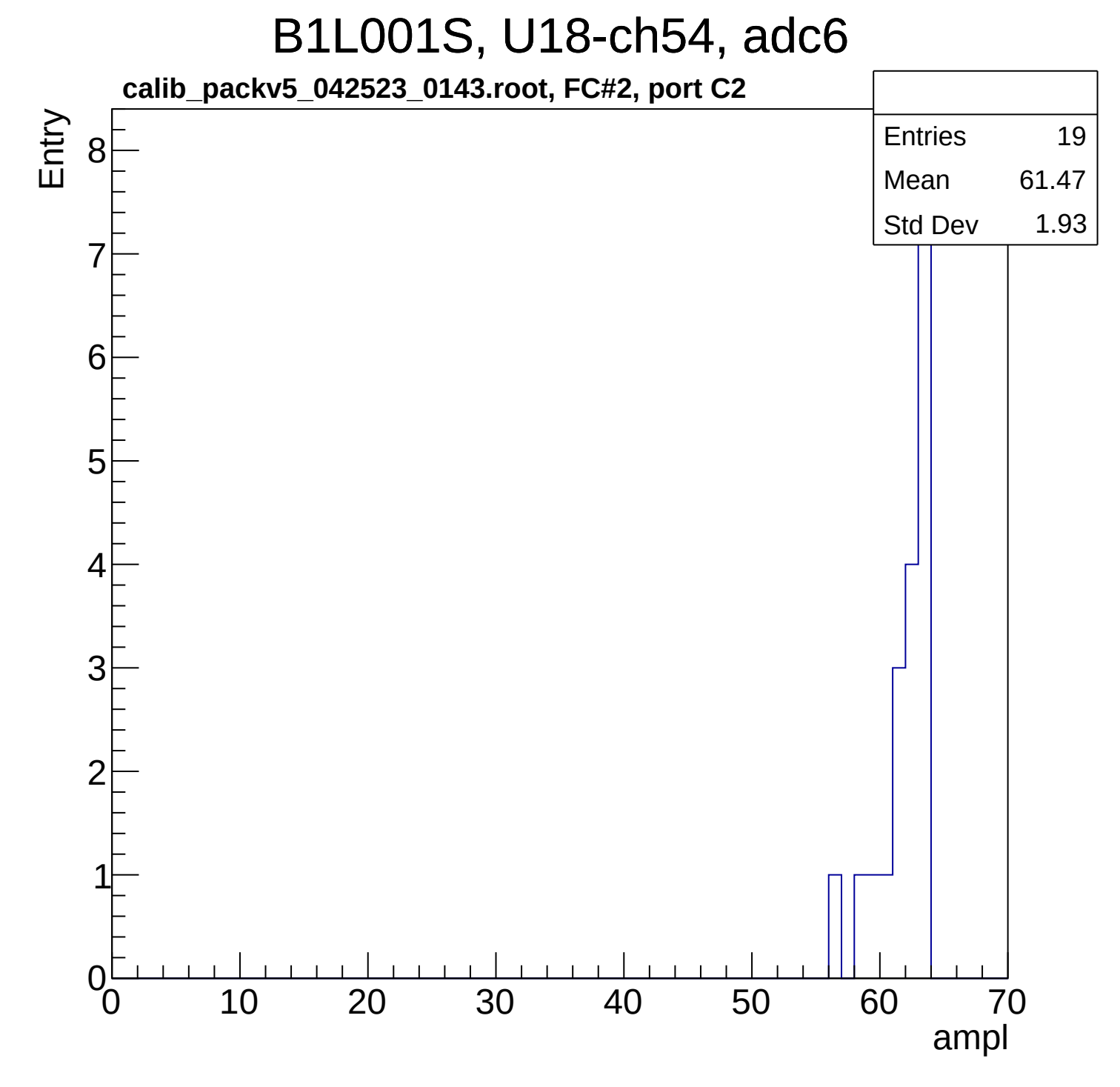

B1L001S, U18-ch54, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 151
Mean 35.83
Std Dev 4.002
Gaus mean : 36.1084
Gaus Width: 4.2601
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

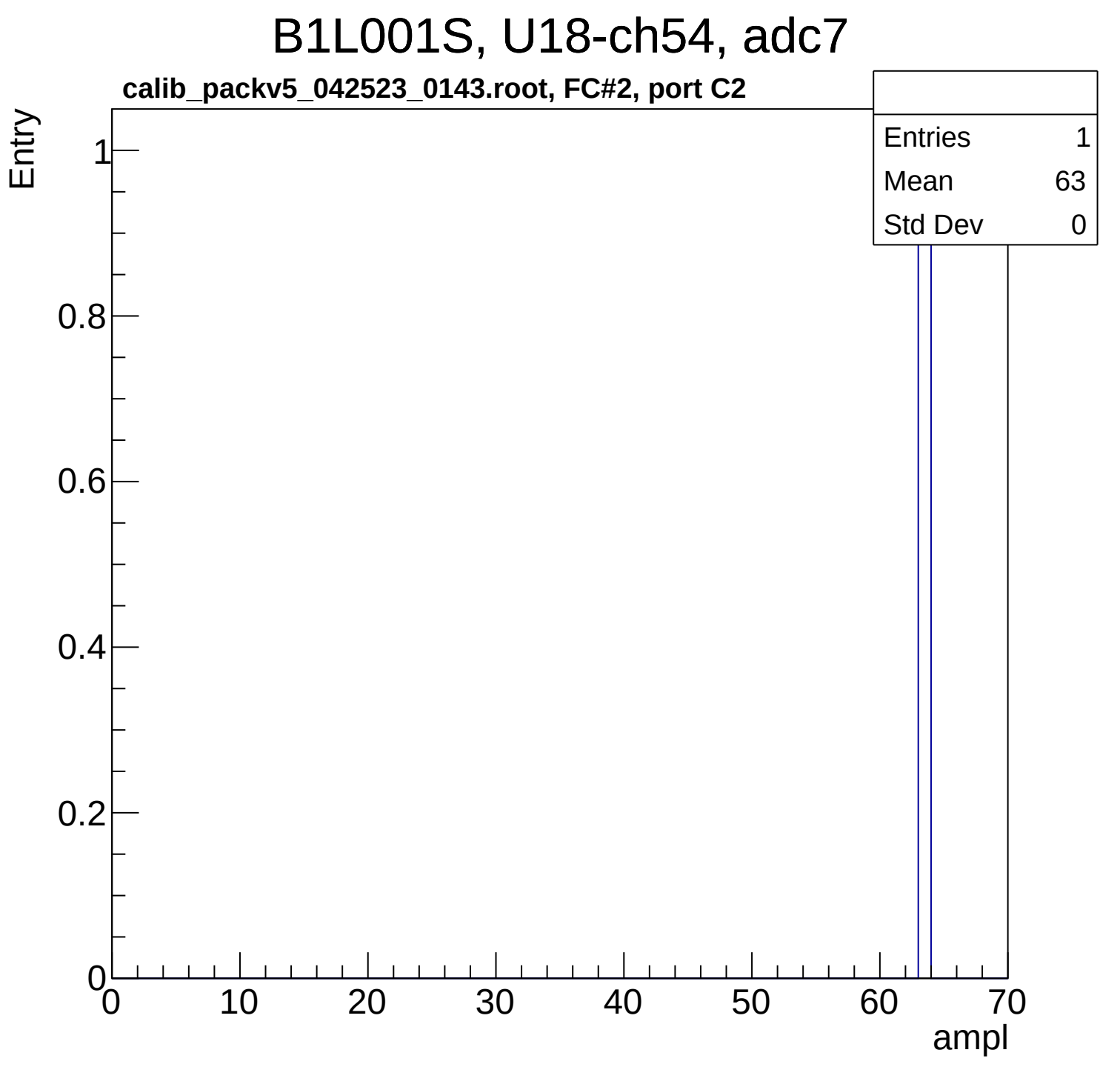

B1L001S, U18-ch54, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 140
Mean 43.01
Std Dev 3.608
Gaus mean : 43.5540
Gaus Width: 3.6299
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

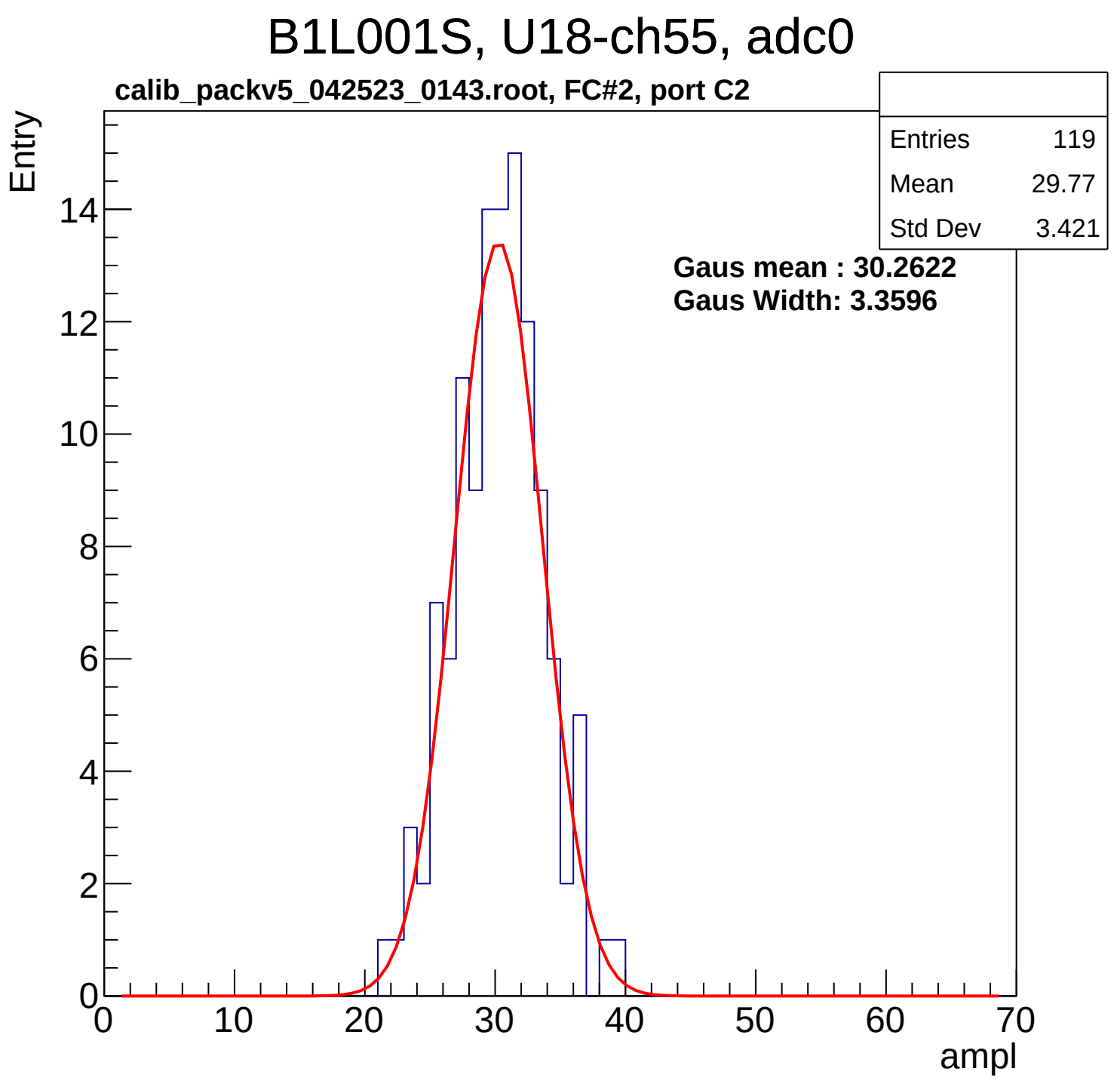

B1L001S, U18-ch54, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 102
Mean 49.03
Std Dev 3.46
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

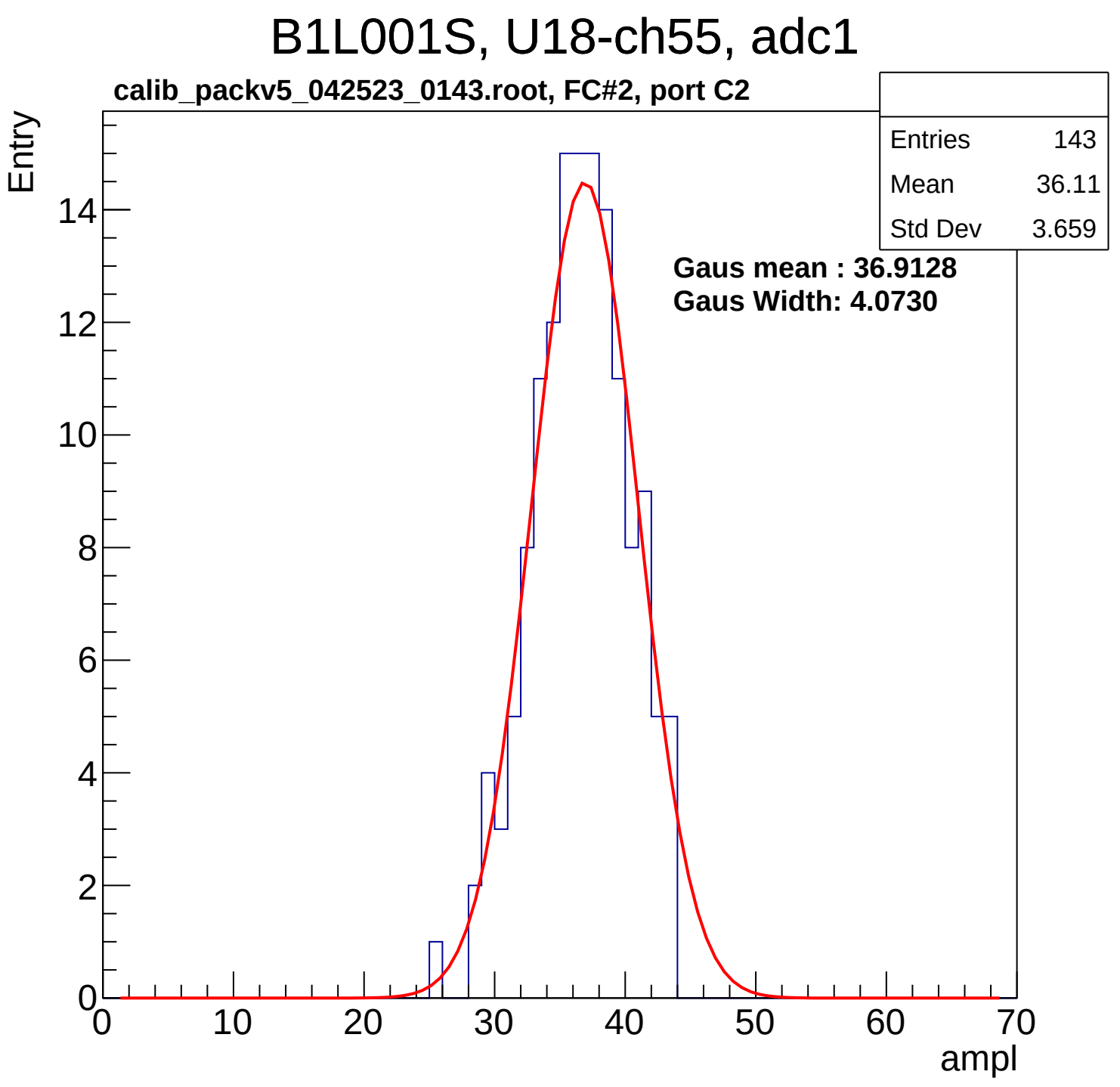

B1L001S, U18-ch54, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 126
Mean 55.37
Std Dev 3.363
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

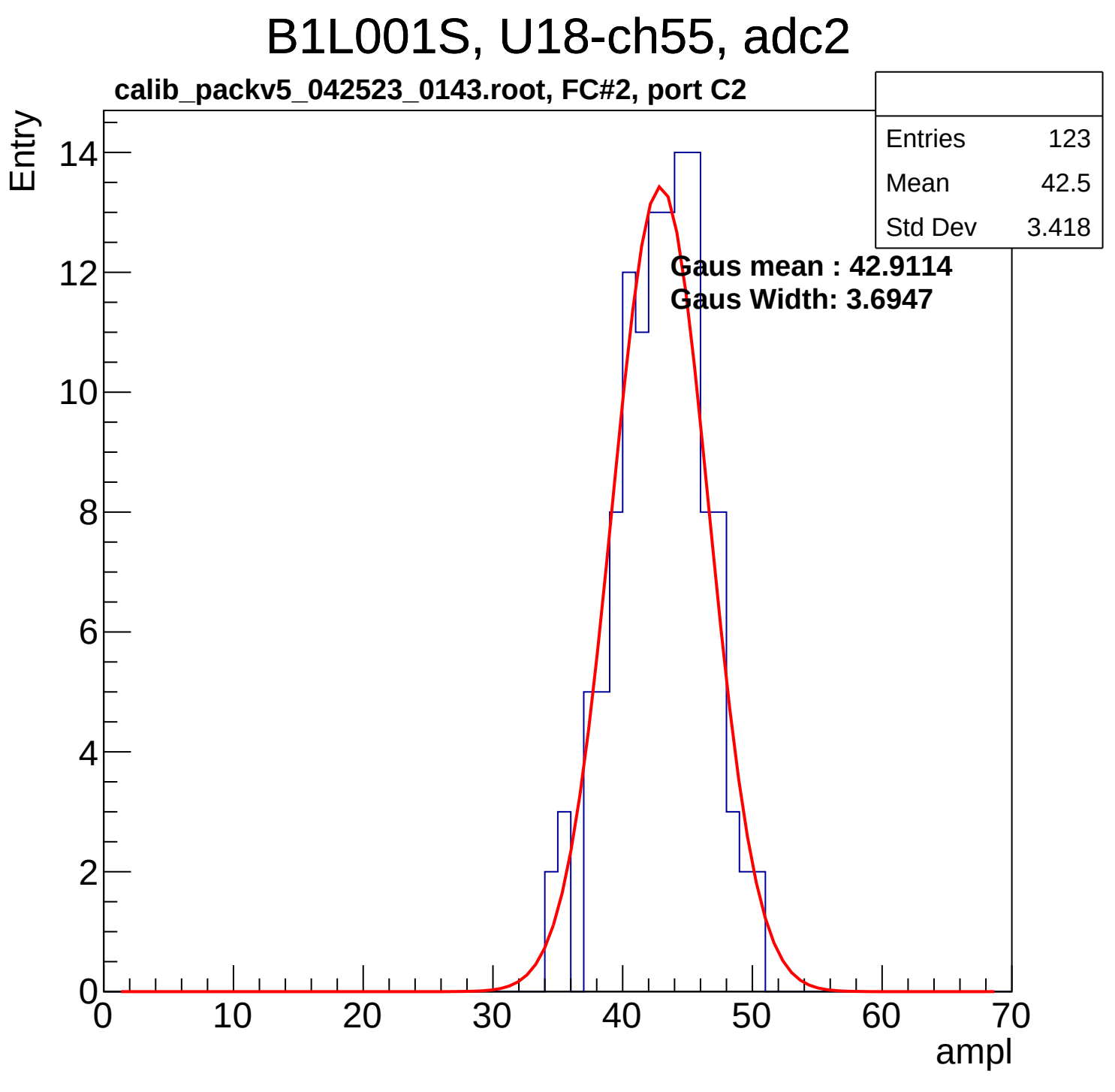

B1L001S, U18-ch54, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 91
Mean 57.85
Std Dev 9.121
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

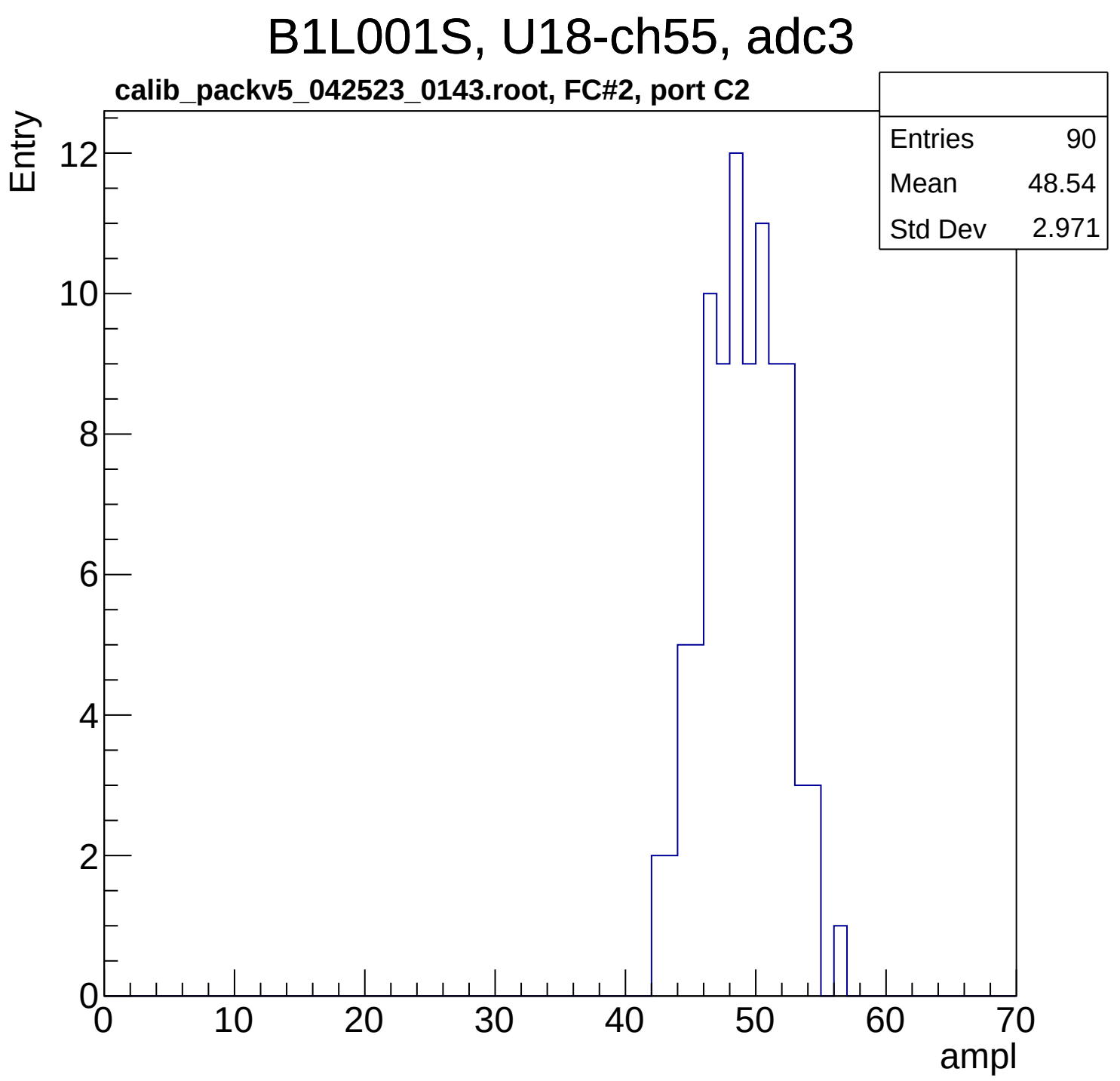

B1L001S, U18-ch54, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 19
Mean 61.47
Std Dev 1.93
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

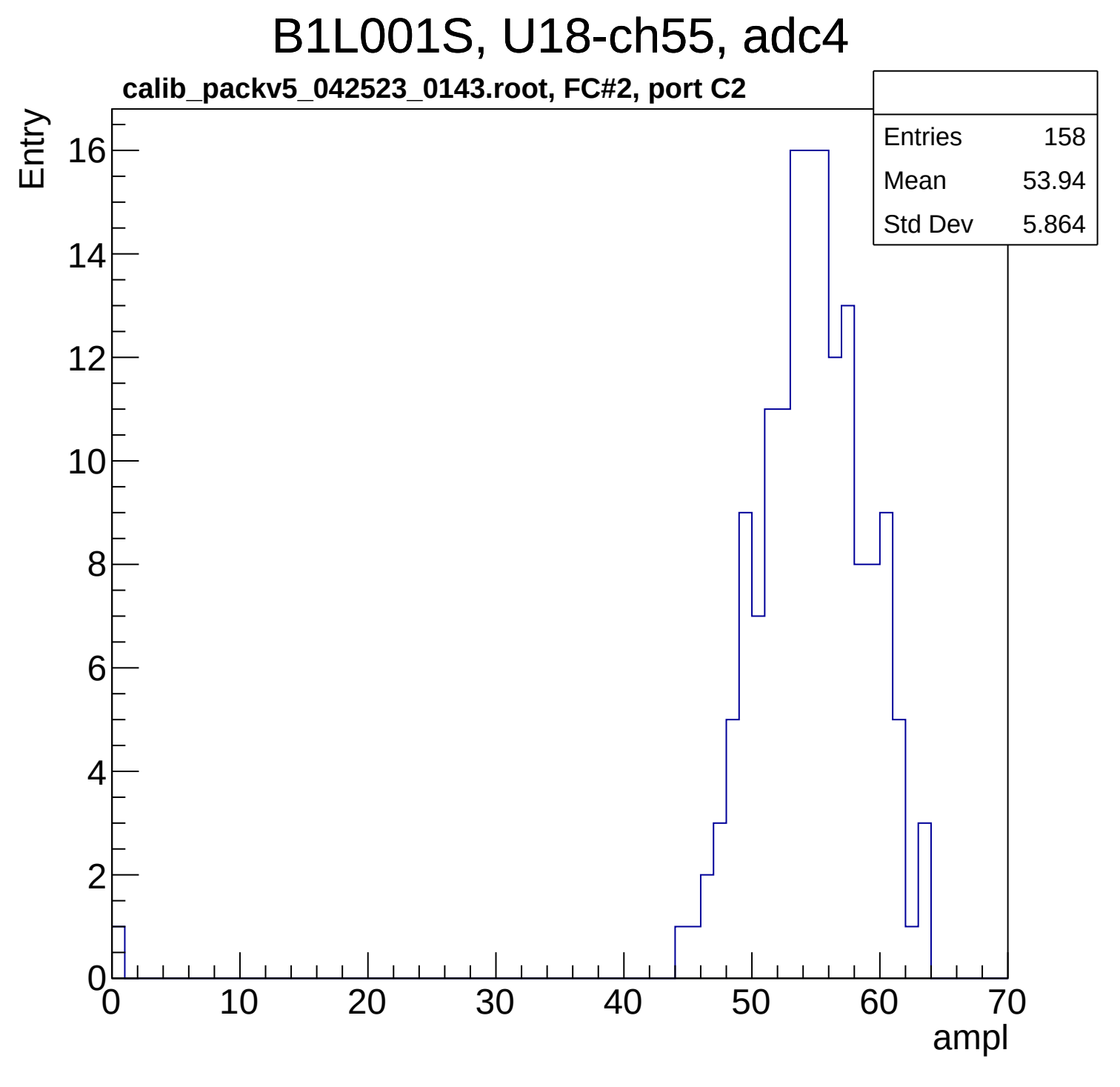

B1L001S, U18-ch54, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 63
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

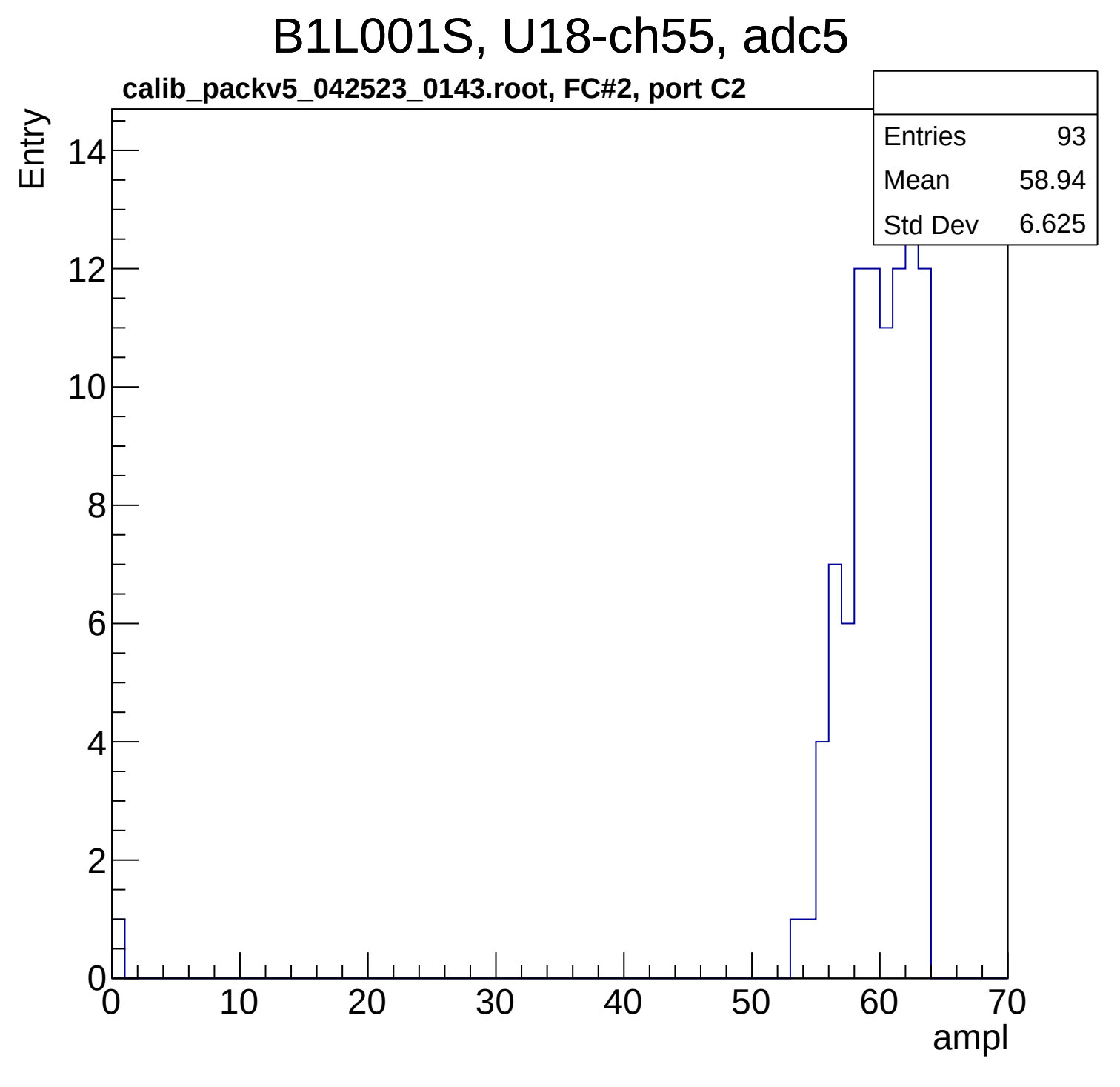

B1L001S, U18-ch55, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 119
Mean 29.77
Std Dev 3.421
Gaus mean : 30.2622
Gaus Width: 3.3596
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

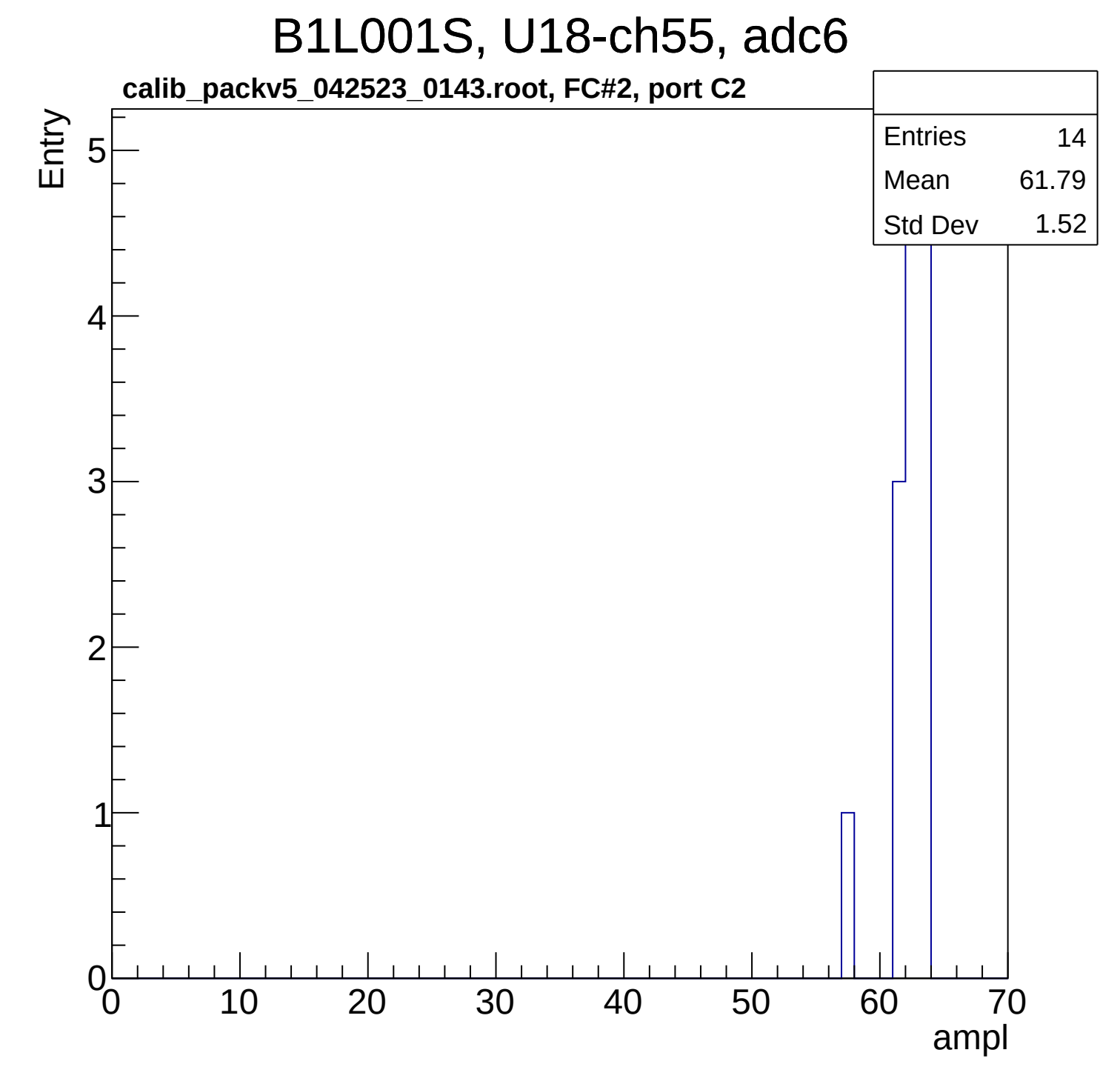

B1L001S, U18-ch55, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 143
Mean 36.11
Std Dev 3.659
Gaus mean : 36.9128
Gaus Width: 4.0730
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

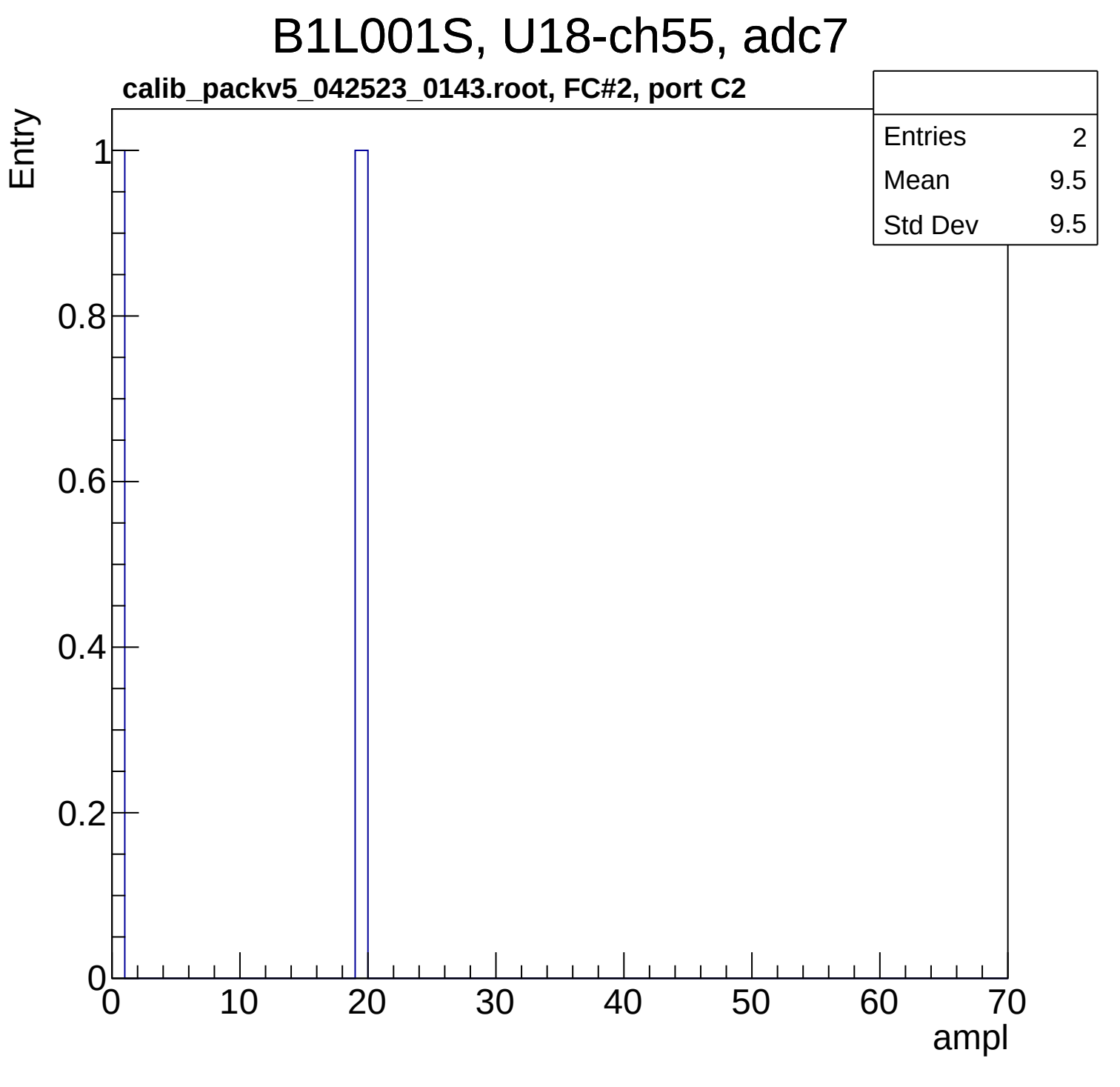

B1L001S, U18-ch55, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 123
Mean 42.5
Std Dev 3.418
Gaus mean : 42.9114
Gaus Width: 3.6947
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

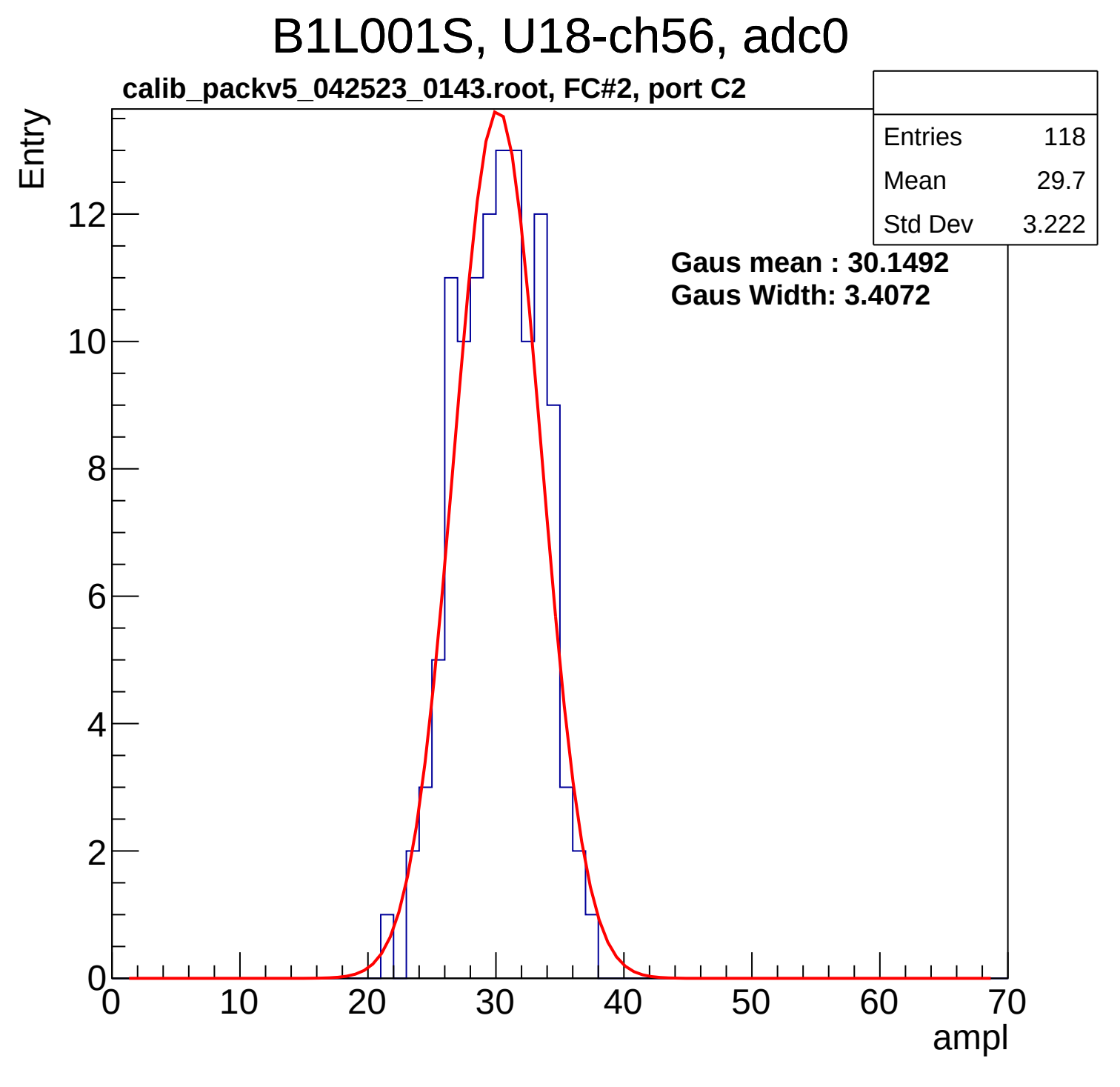

B1L001S, U18-ch55, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 90
Mean 48.54
Std Dev 2.971
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl

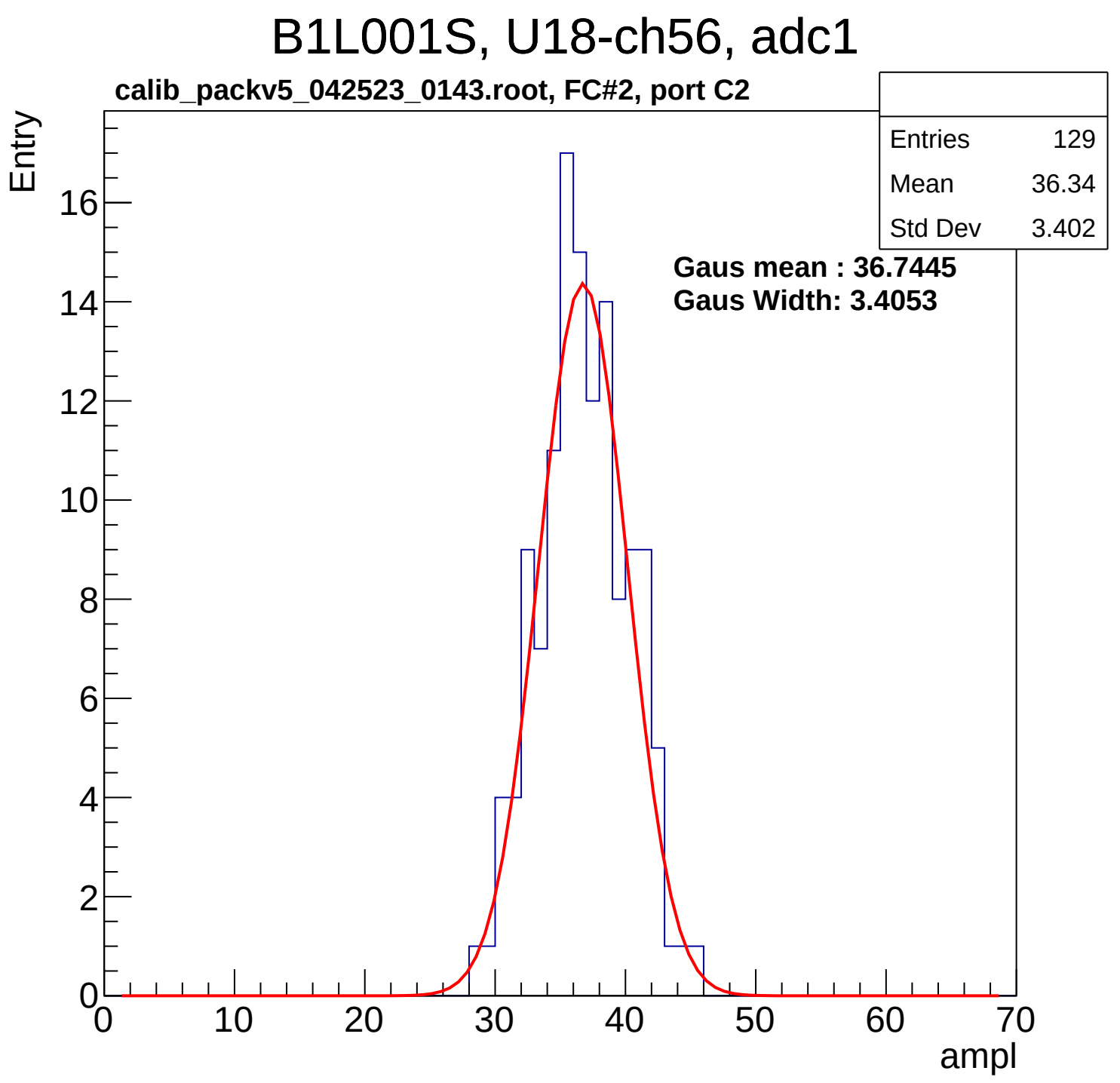

B1L001S, U18-ch55, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 158
Mean 53.94
Std Dev 5.864
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

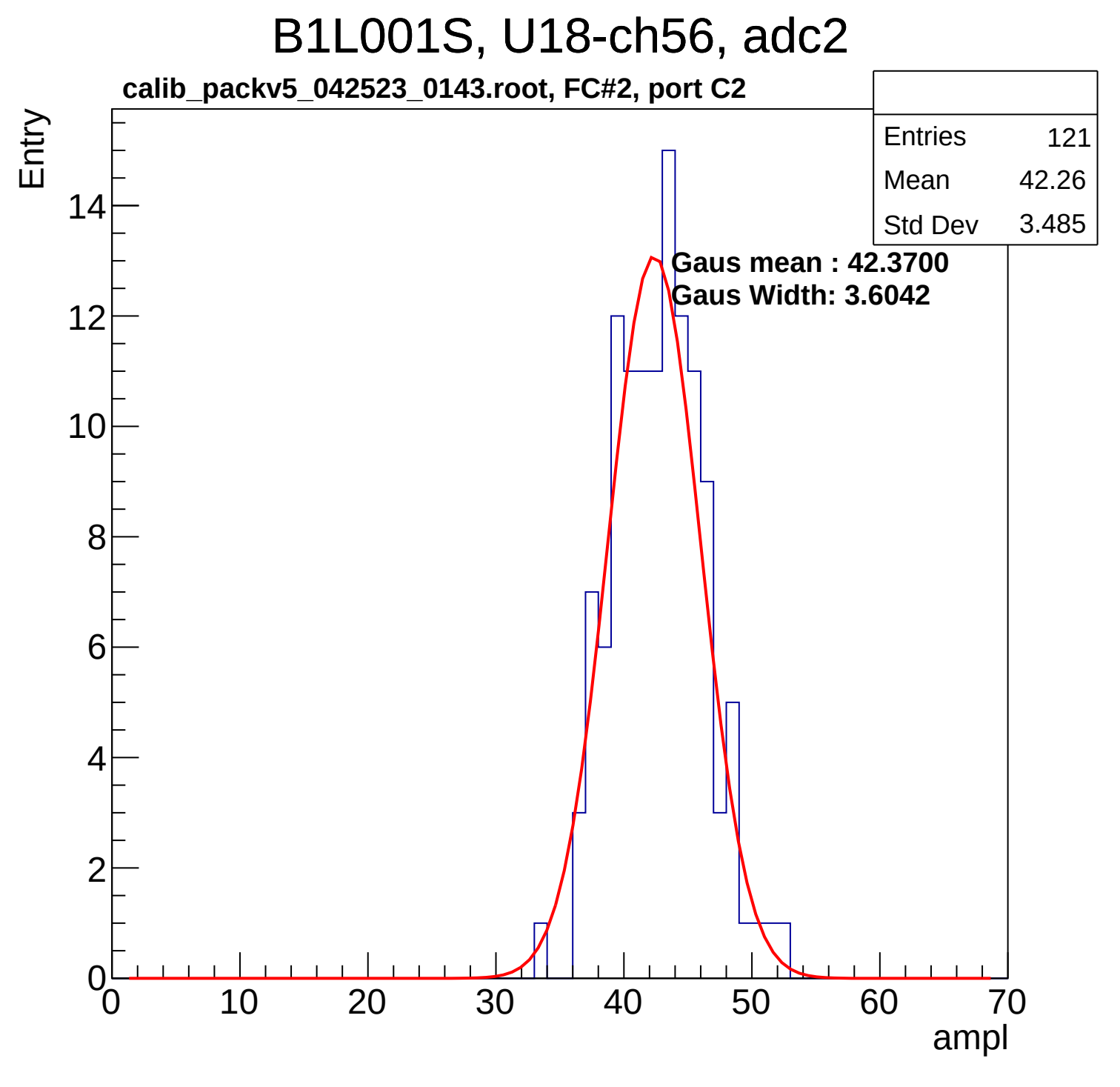

B1L001S, U18-ch55, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 93
Mean 58.94
Std Dev 6.625
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

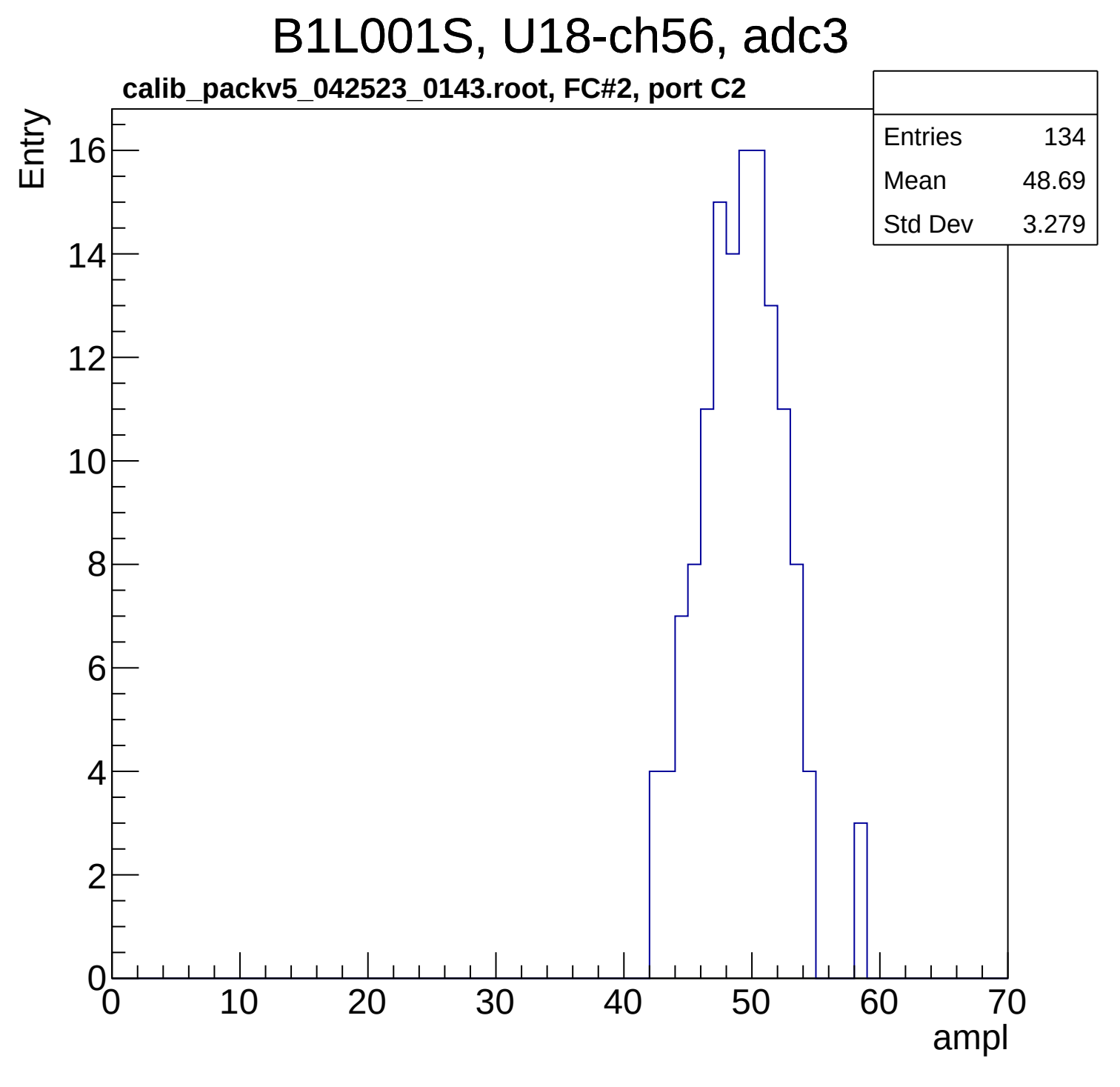

B1L001S, U18-ch55, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 14
Mean 61.79
Std Dev 1.52
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

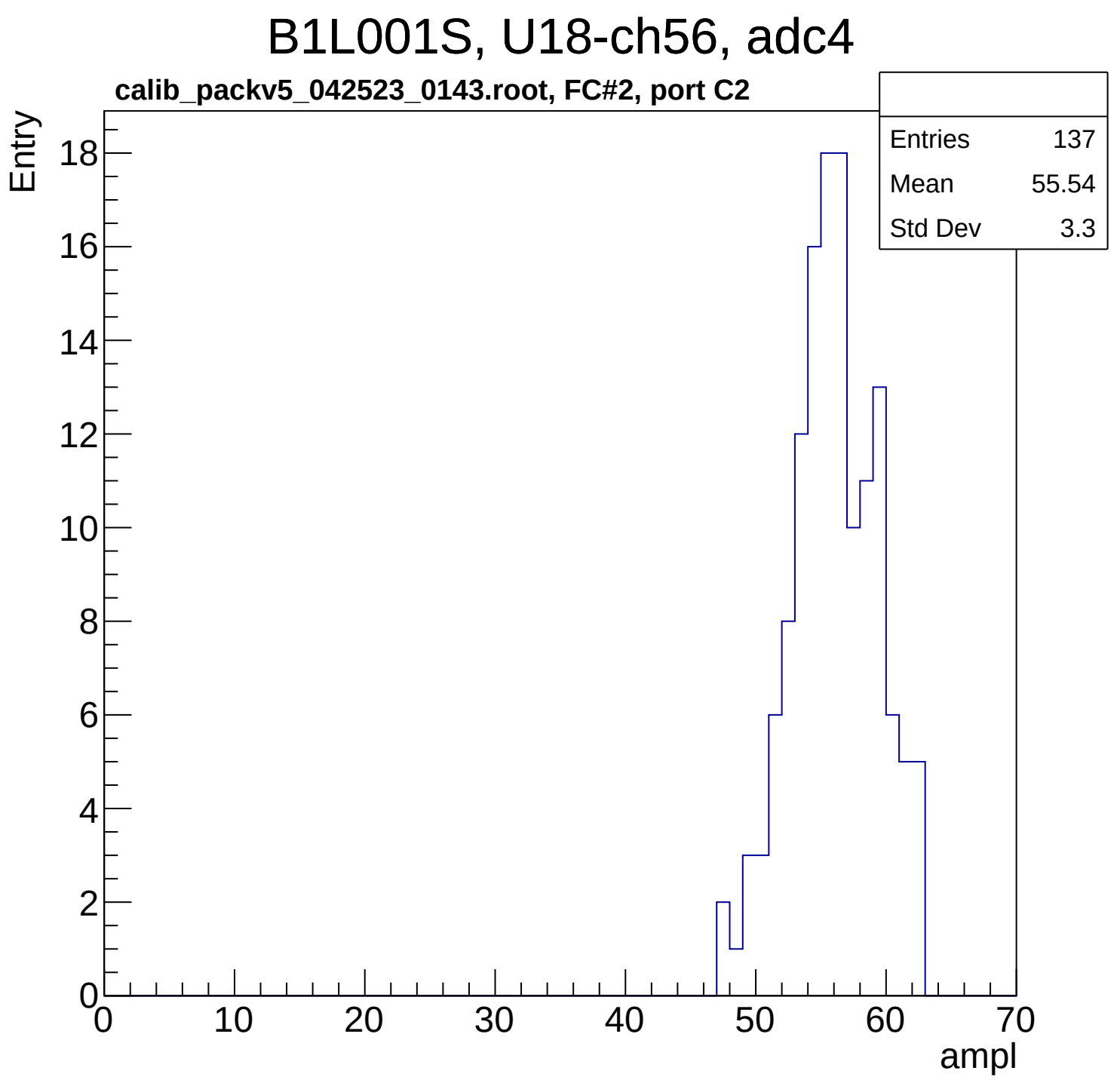

B1L001S, U18-ch55, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 9.5
Std Dev 9.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

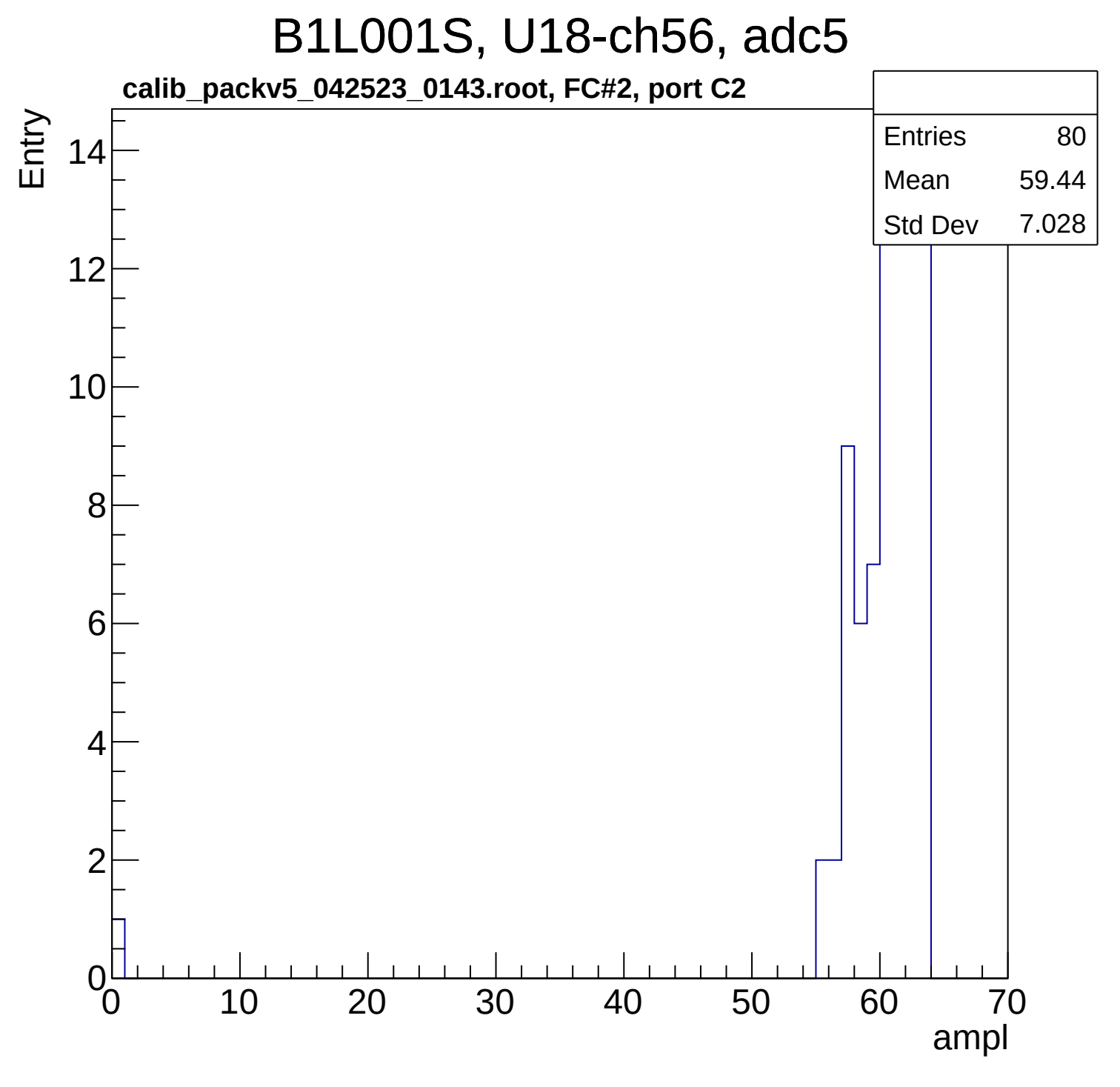

B1L001S, U18-ch56, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 118
Mean 29.7
Std Dev 3.222
Gaus mean : 30.1492
Gaus Width: 3.4072
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70

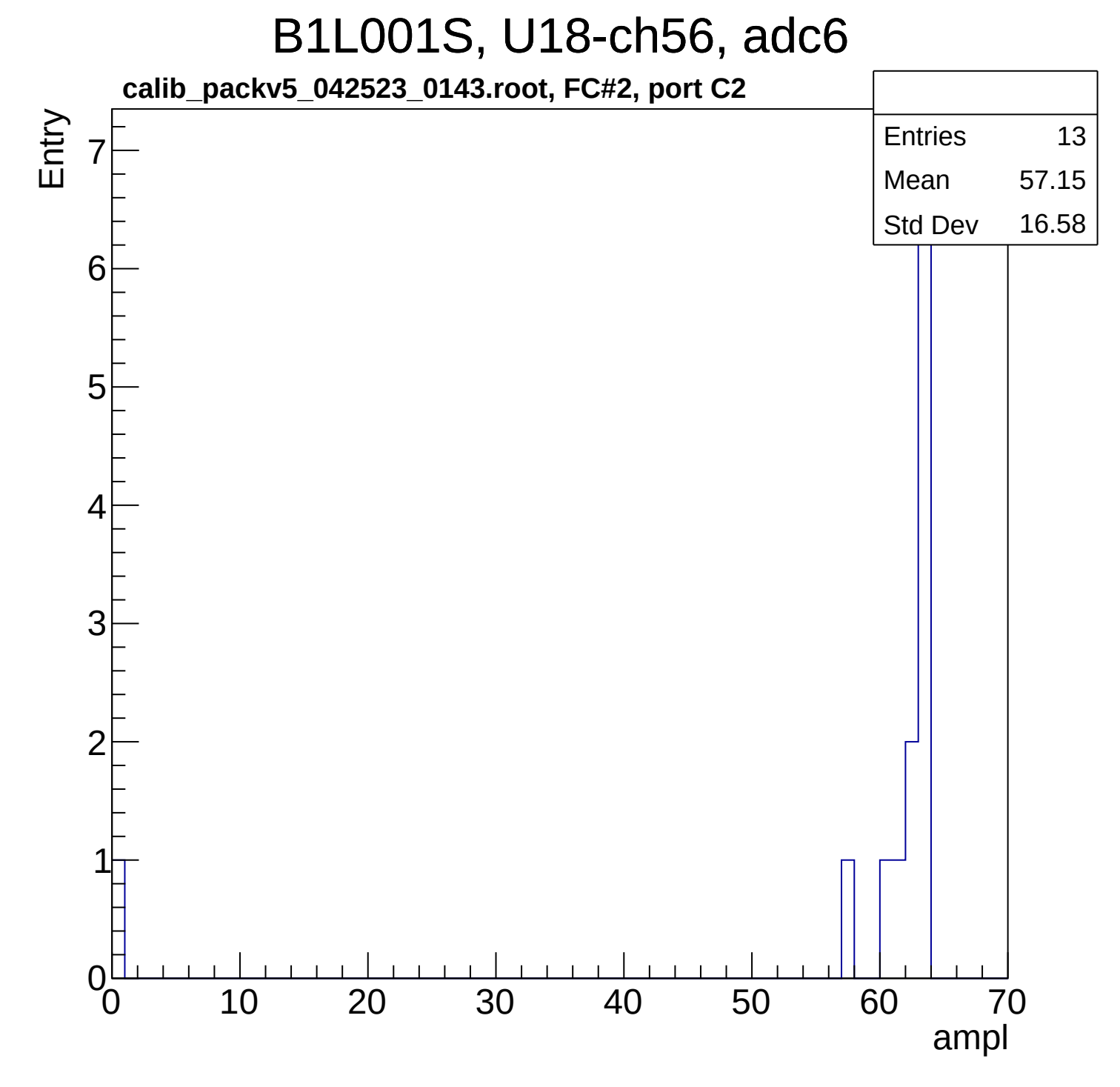

B1L001S, U18-ch56, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 129
Mean 36.34
Std Dev 3.402
Gaus mean : 36.7445
Gaus Width: 3.4053
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

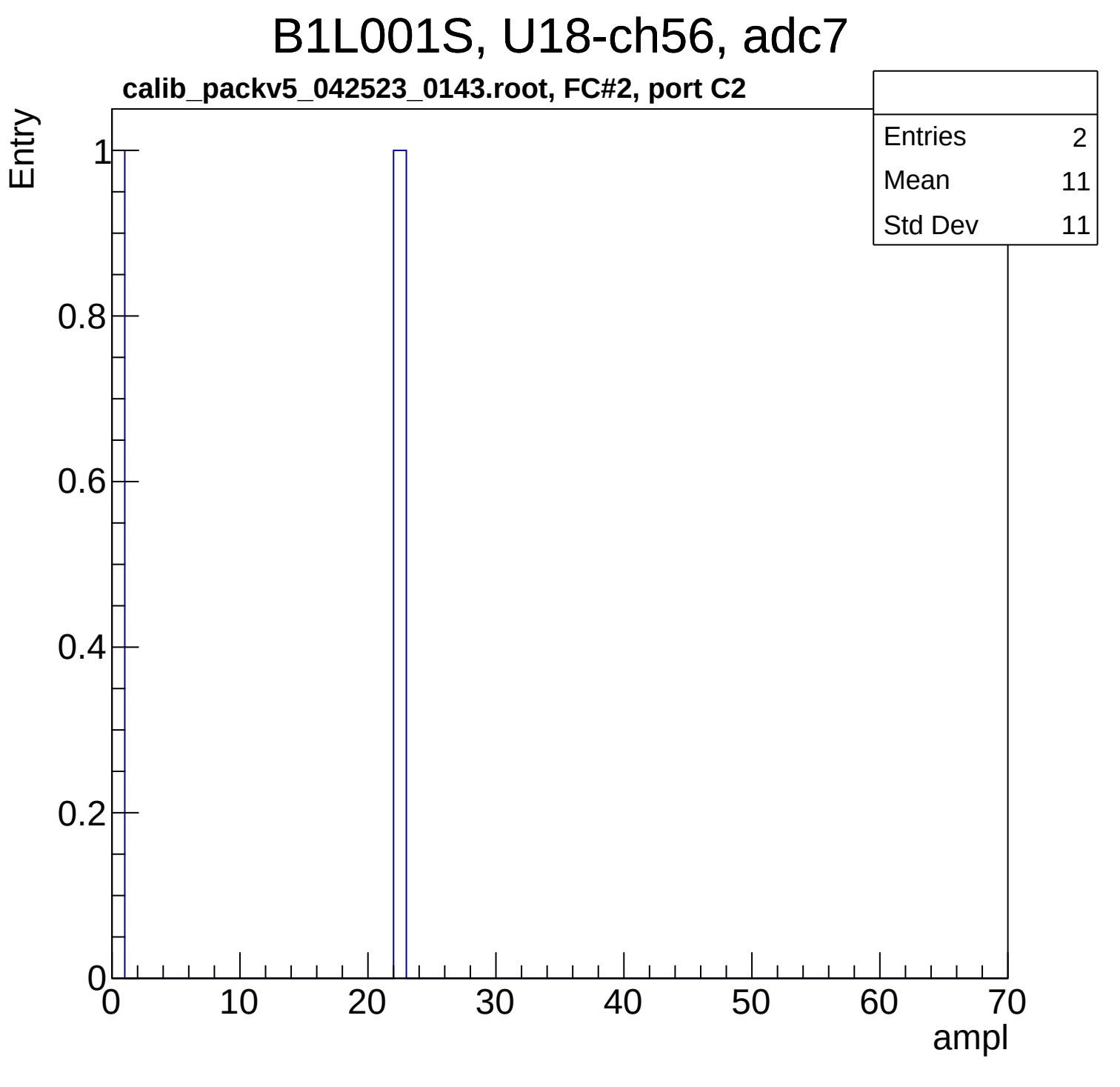

B1L001S, U18-ch56, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 121
Mean 42.26
Std Dev 3.485
Gaus mean : 42.3700
Gaus Width: 3.6042
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

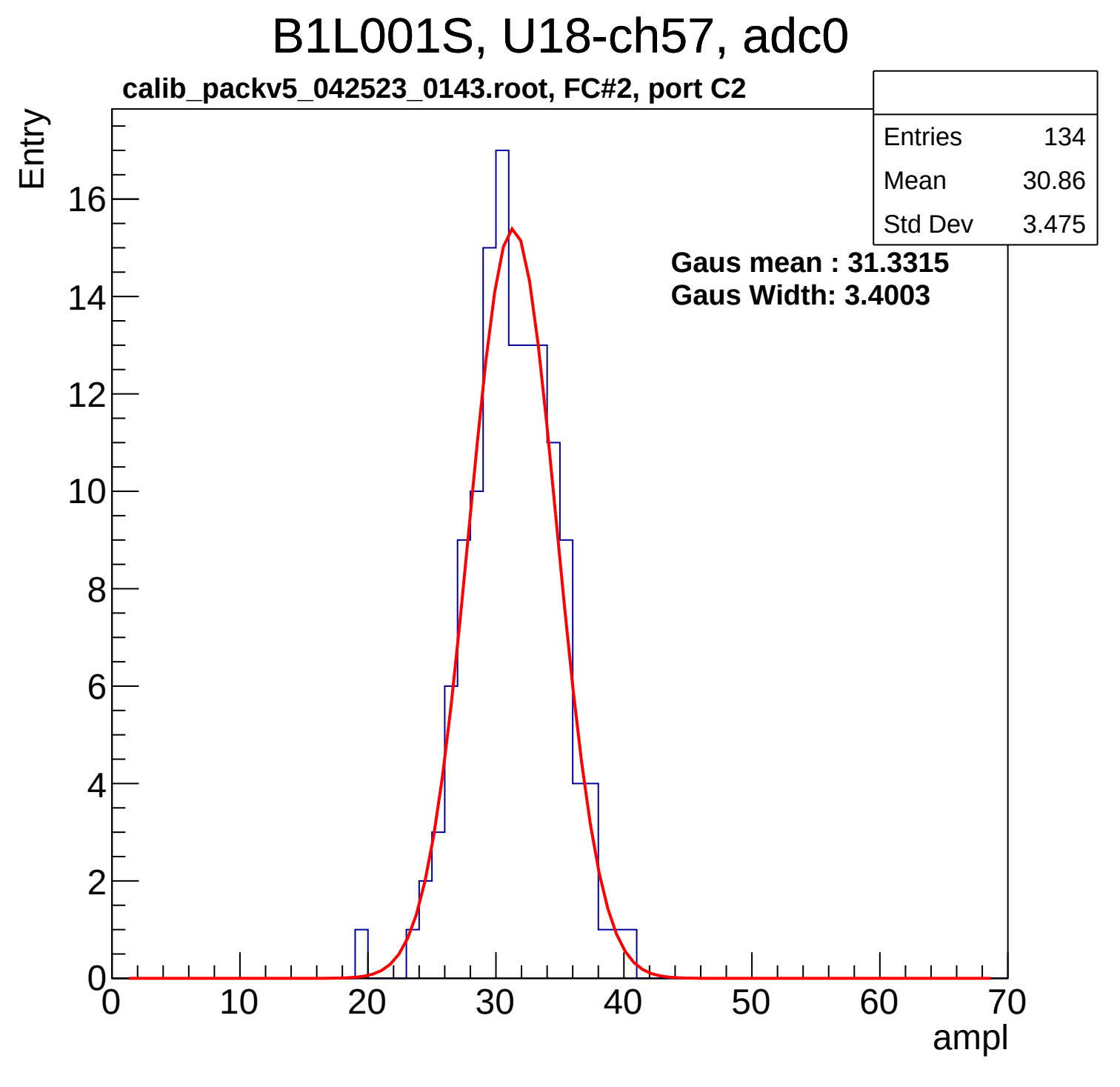

B1L001S, U18-ch56, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 134
Mean 48.69
Std Dev 3.279
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

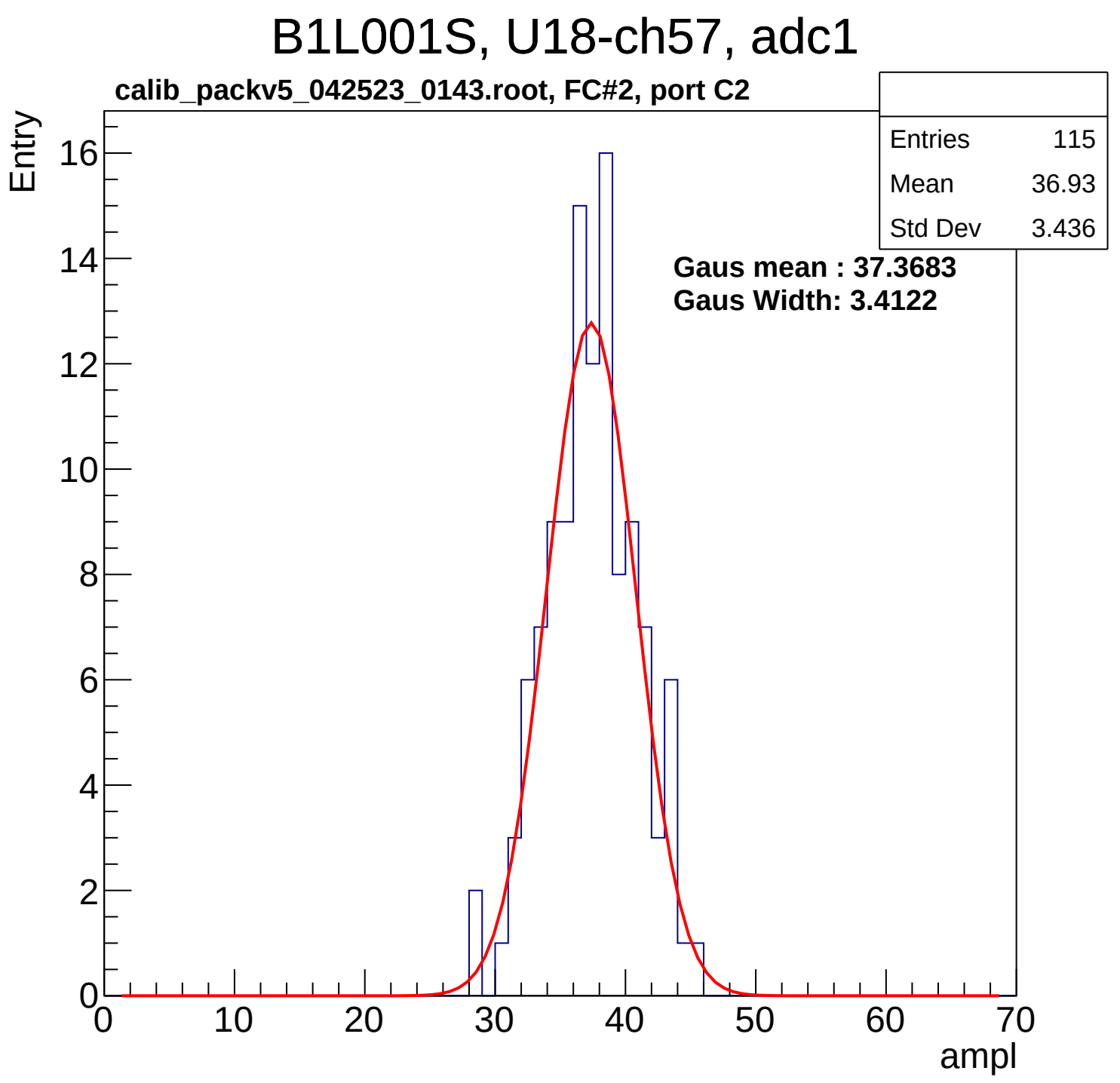

B1L001S, U18-ch56, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 137
Mean 55.54
Std Dev 3.3
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

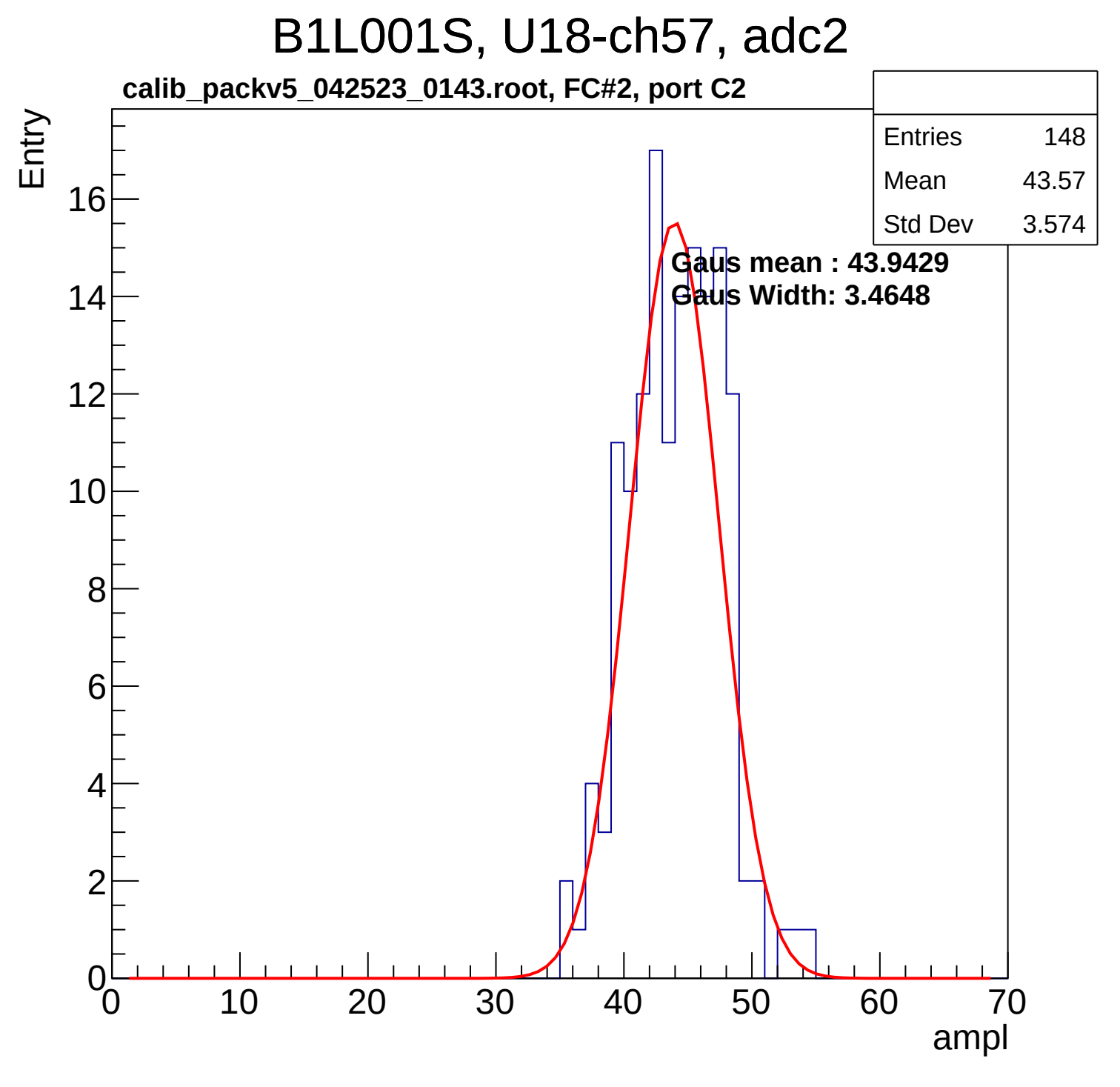

B1L001S, U18-ch56, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 80
Mean 59.44
Std Dev 7.028
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

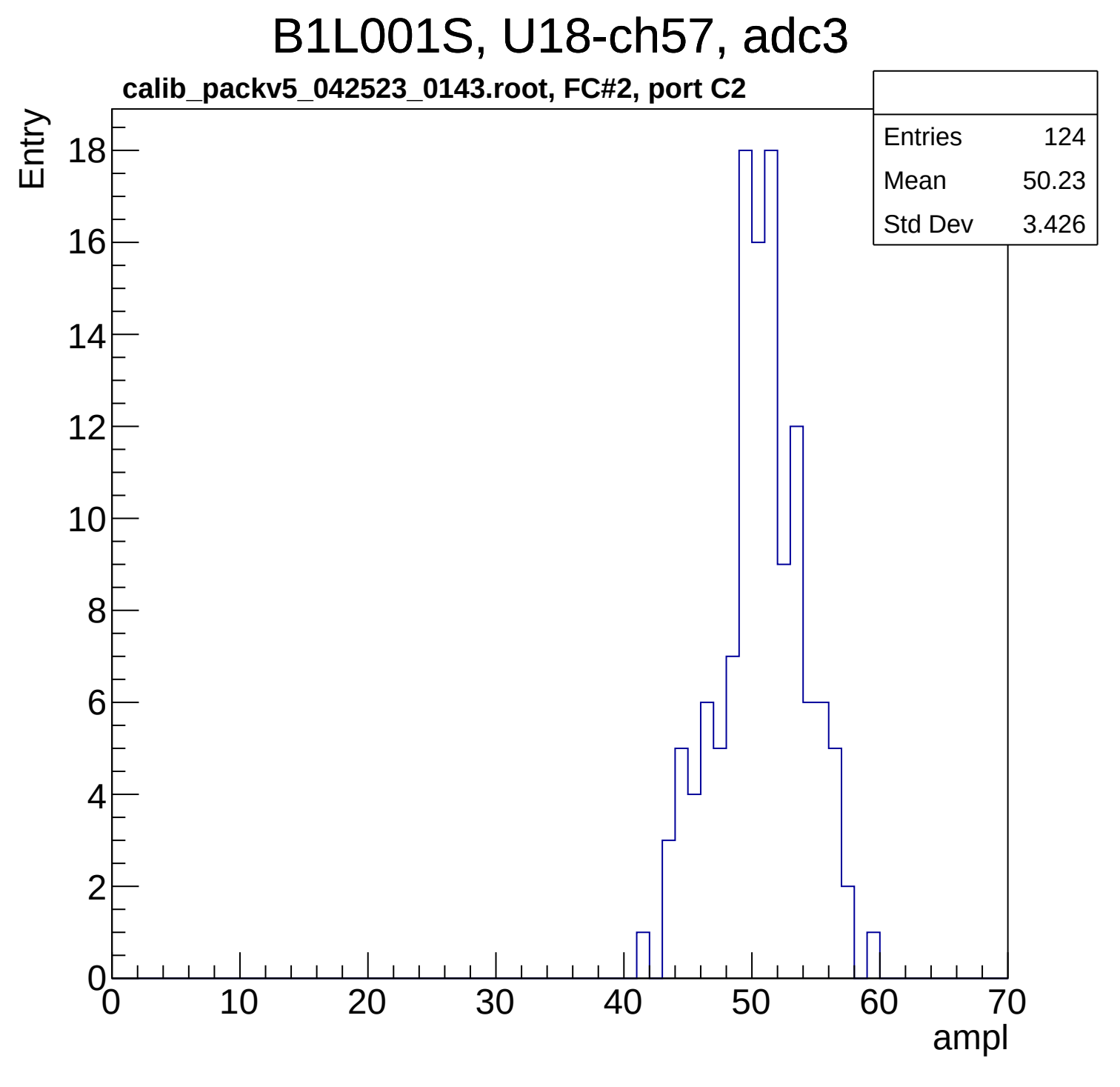

B1L001S, U18-ch56, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 13
Mean 57.15
Std Dev 16.58
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

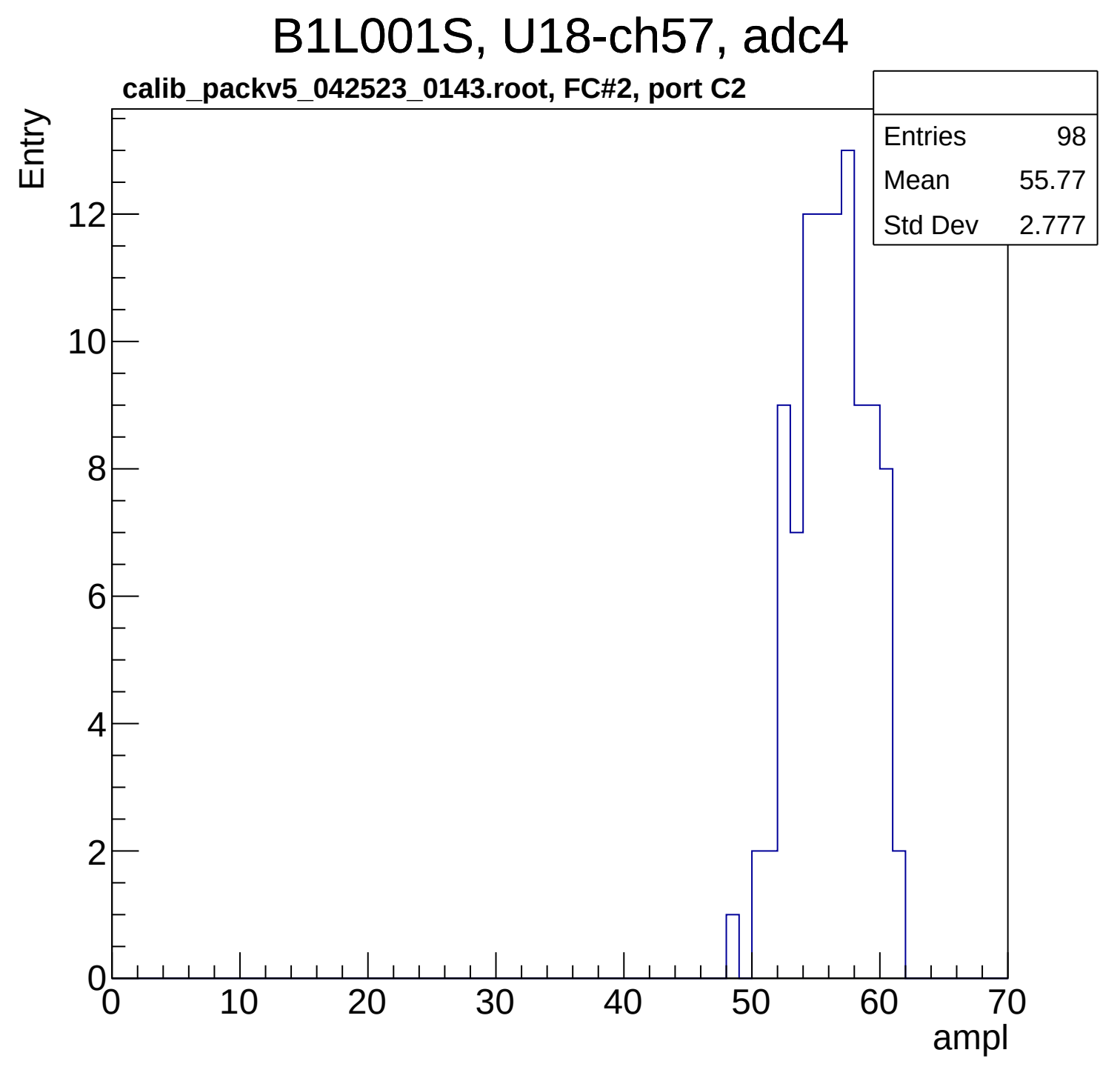

B1L001S, U18-ch56, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 11
Std Dev 11
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70

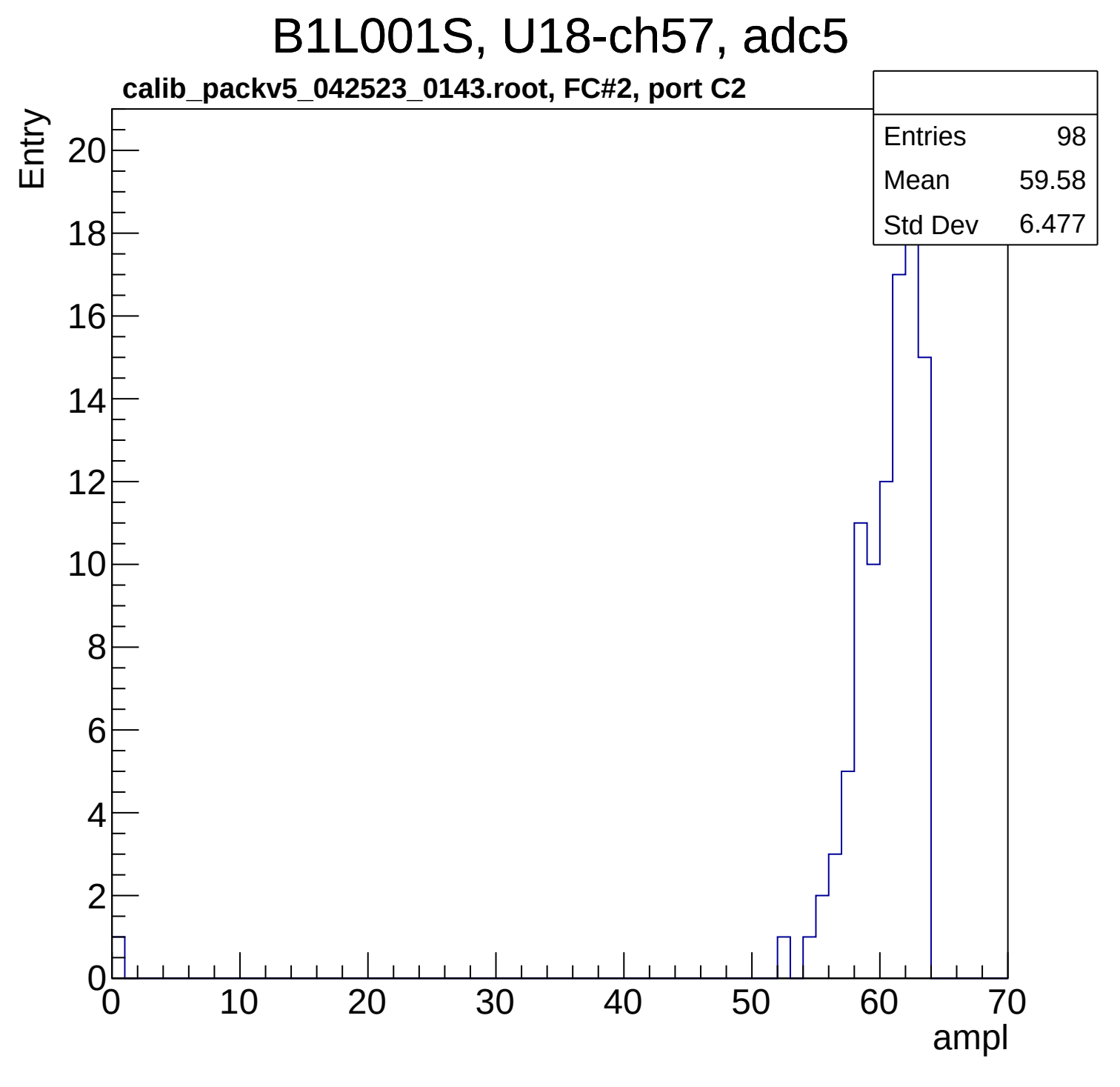

B1L001S, U18-ch57, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 134
Mean 30.86
Std Dev 3.475
Gaus mean : 31.3315
Gaus Width: 3.4003
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

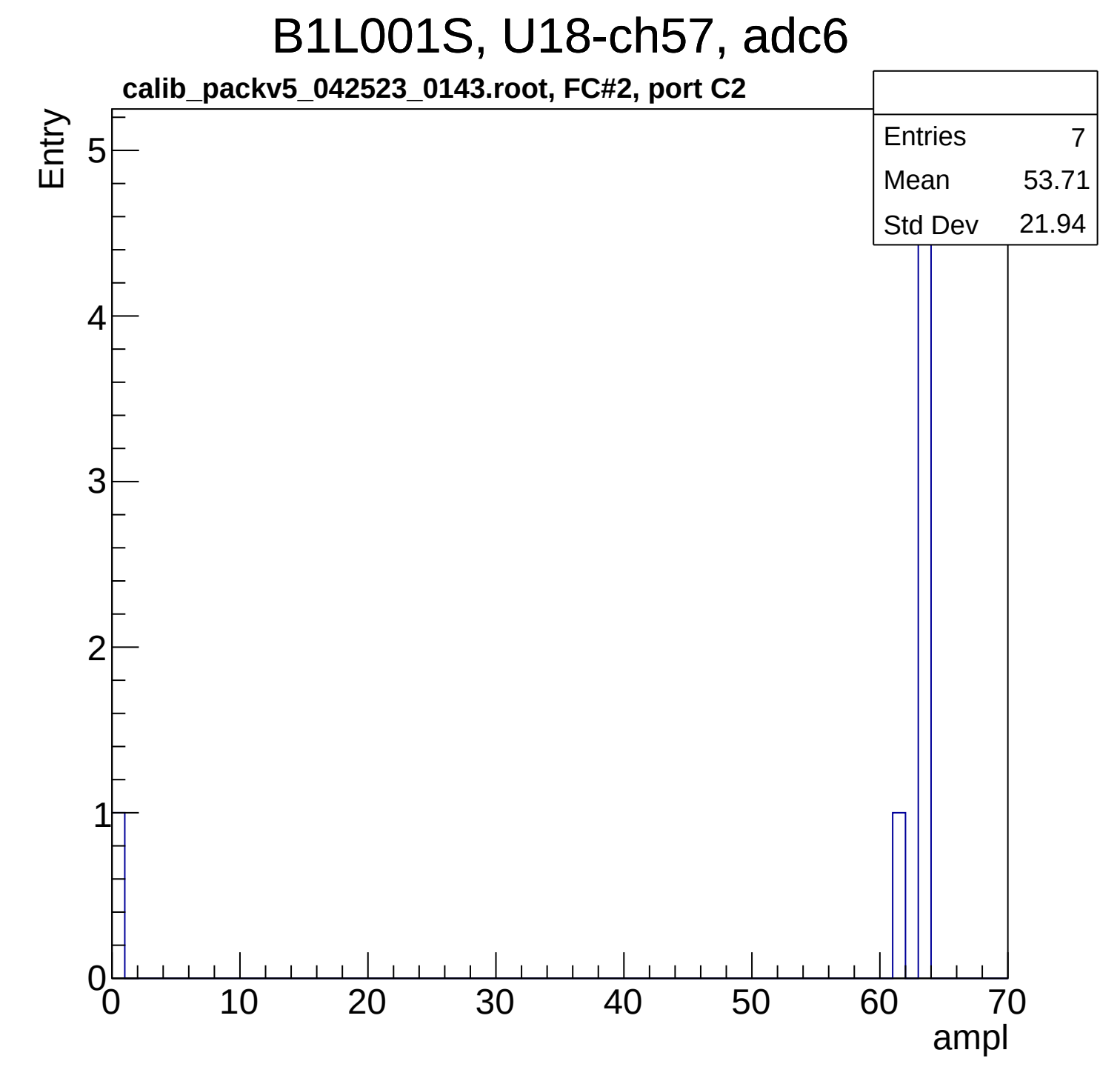

B1L001S, U18-ch57, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 115
Mean 36.93
Std Dev 3.436
Gaus mean : 37.3683
Gaus Width: 3.4122
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

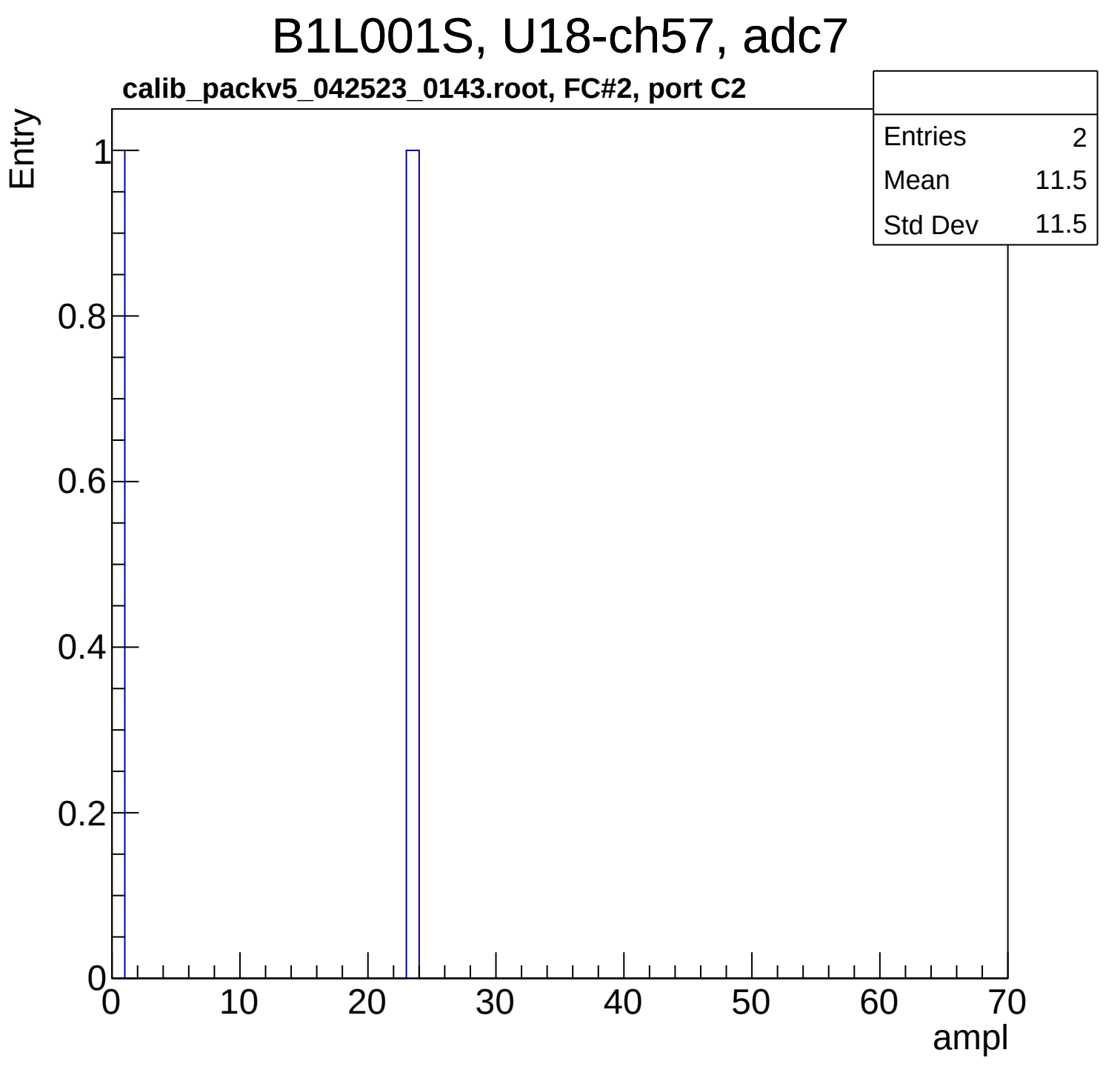

B1L001S, U18-ch57, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 148
Mean 43.57
Std Dev 3.574
Gaus mean : 43.9429
Gaus Width: 3.4648
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

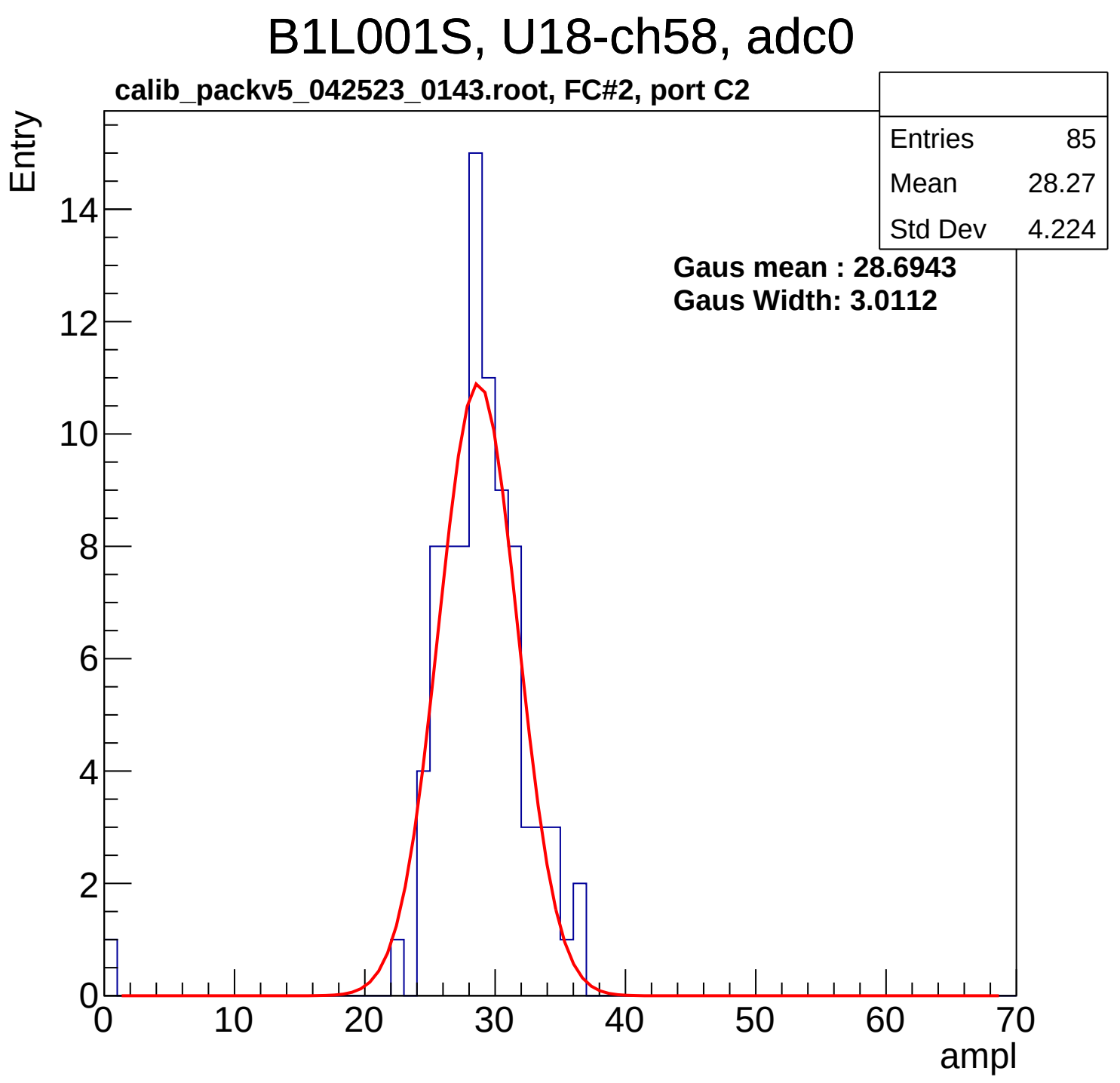

B1L001S, U18-ch57, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 124
Mean 50.23
Std Dev 3.426
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

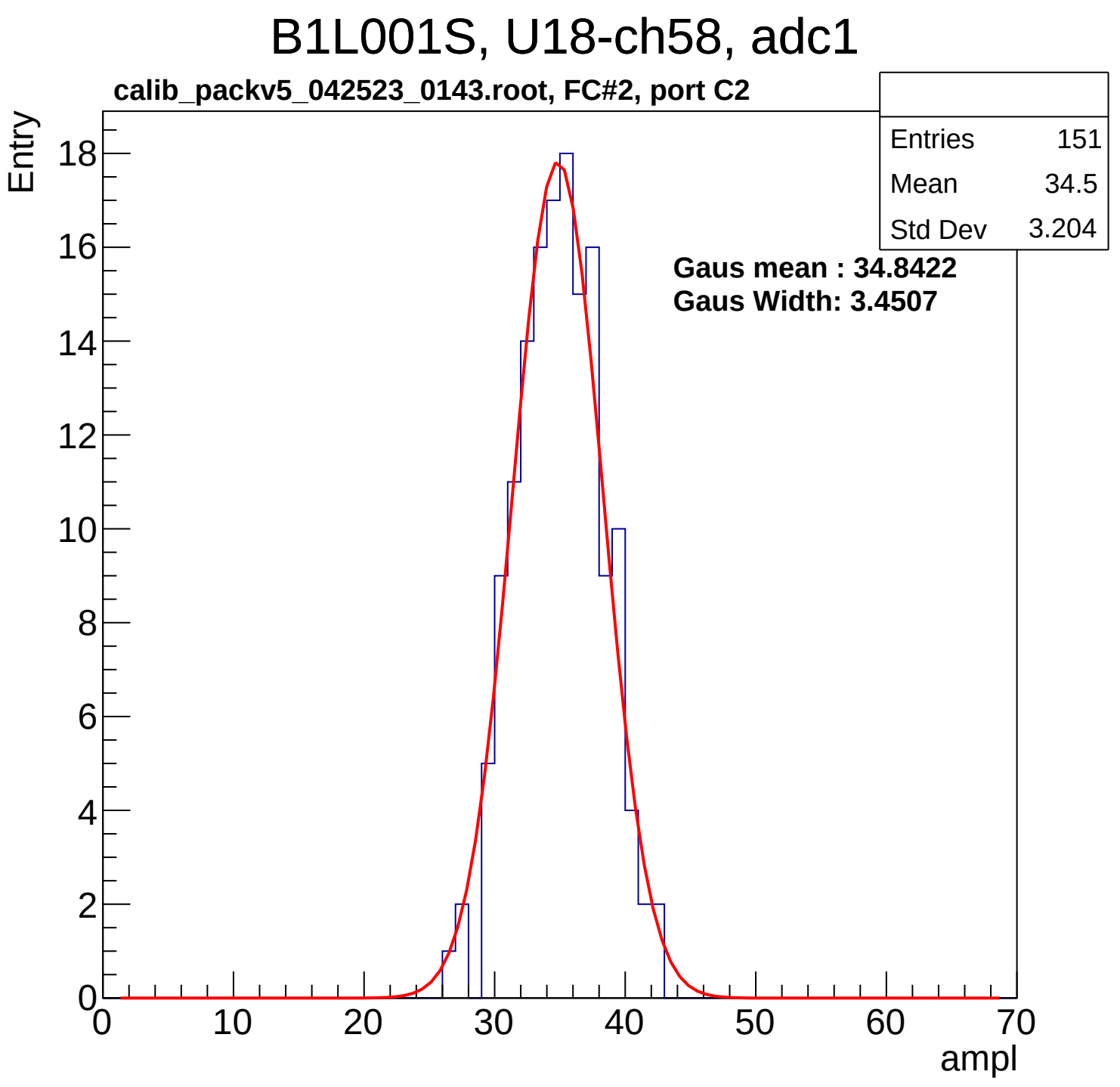

B1L001S, U18-ch57, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 98
Mean 55.77
Std Dev 2.777
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70

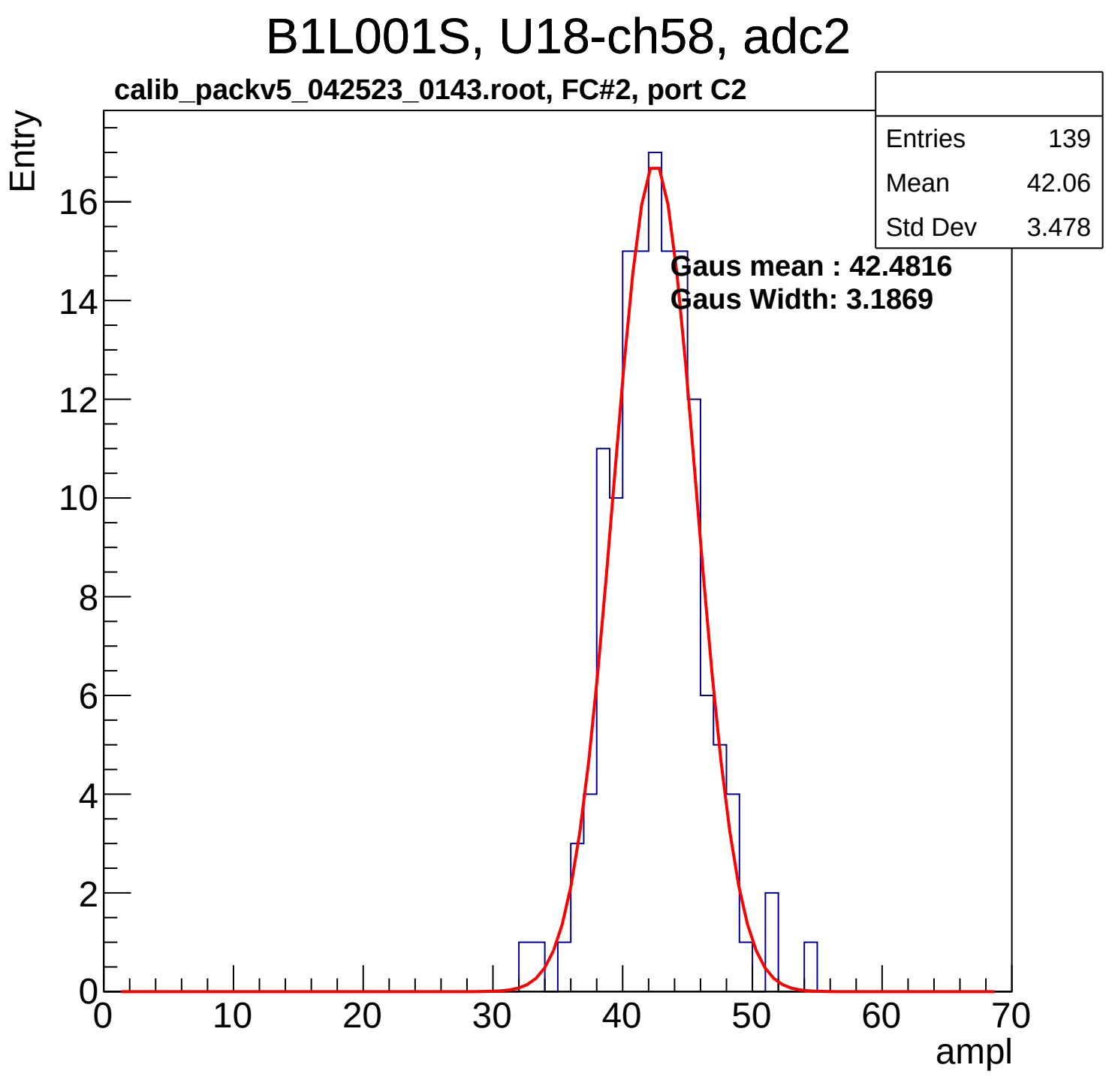

B1L001S, U18-ch57, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 98
Mean 59.58
Std Dev 6.477
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

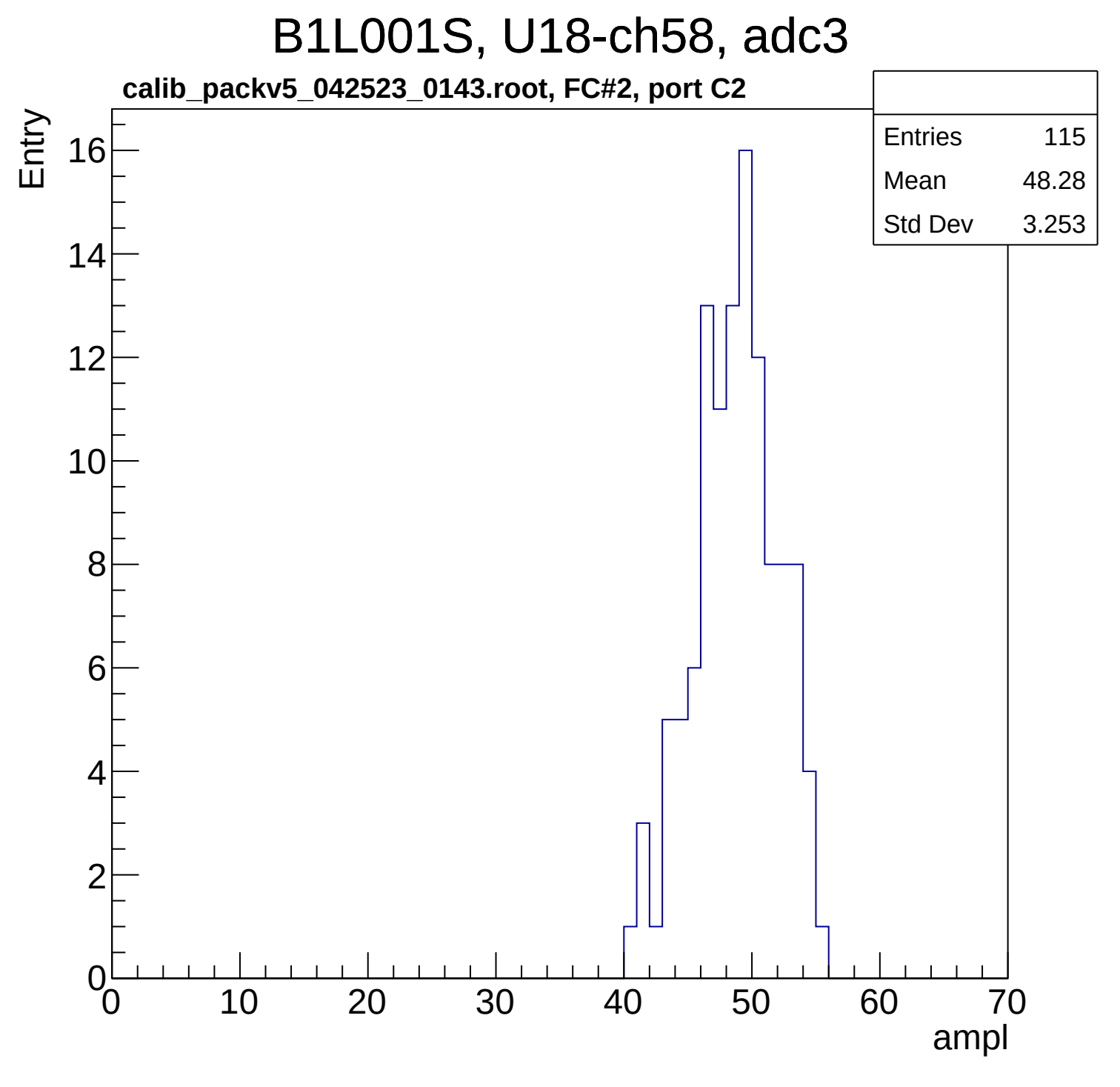

B1L001S, U18-ch57, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 7
Mean 53.71
Std Dev 21.94
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

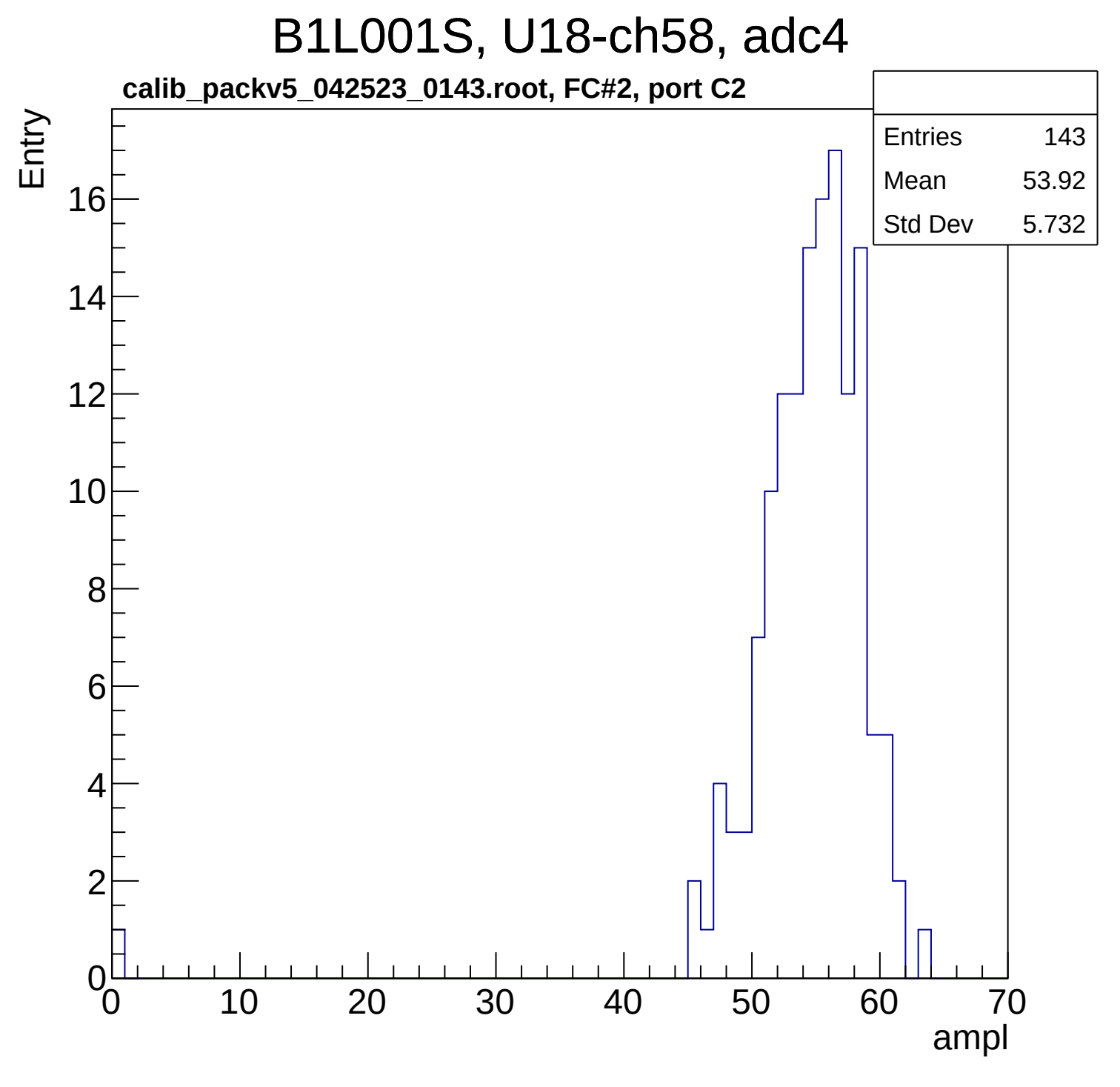

B1L001S, U18-ch57, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 11.5
Std Dev 11.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

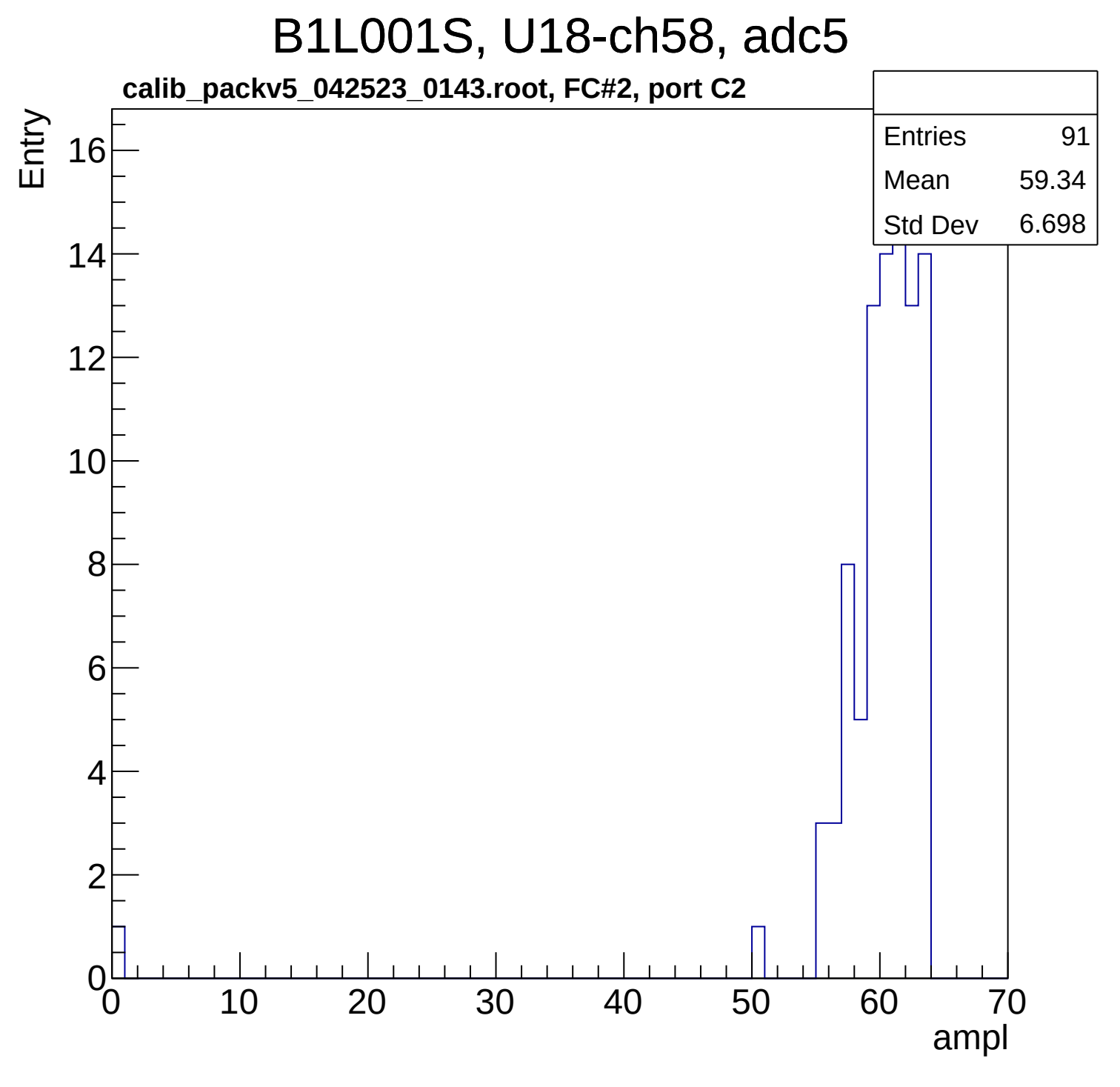

B1L001S, U18-ch58, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 85
Mean 28.27
Std Dev 4.224
Gaus mean : 28.6943
Gaus Width: 3.0112
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

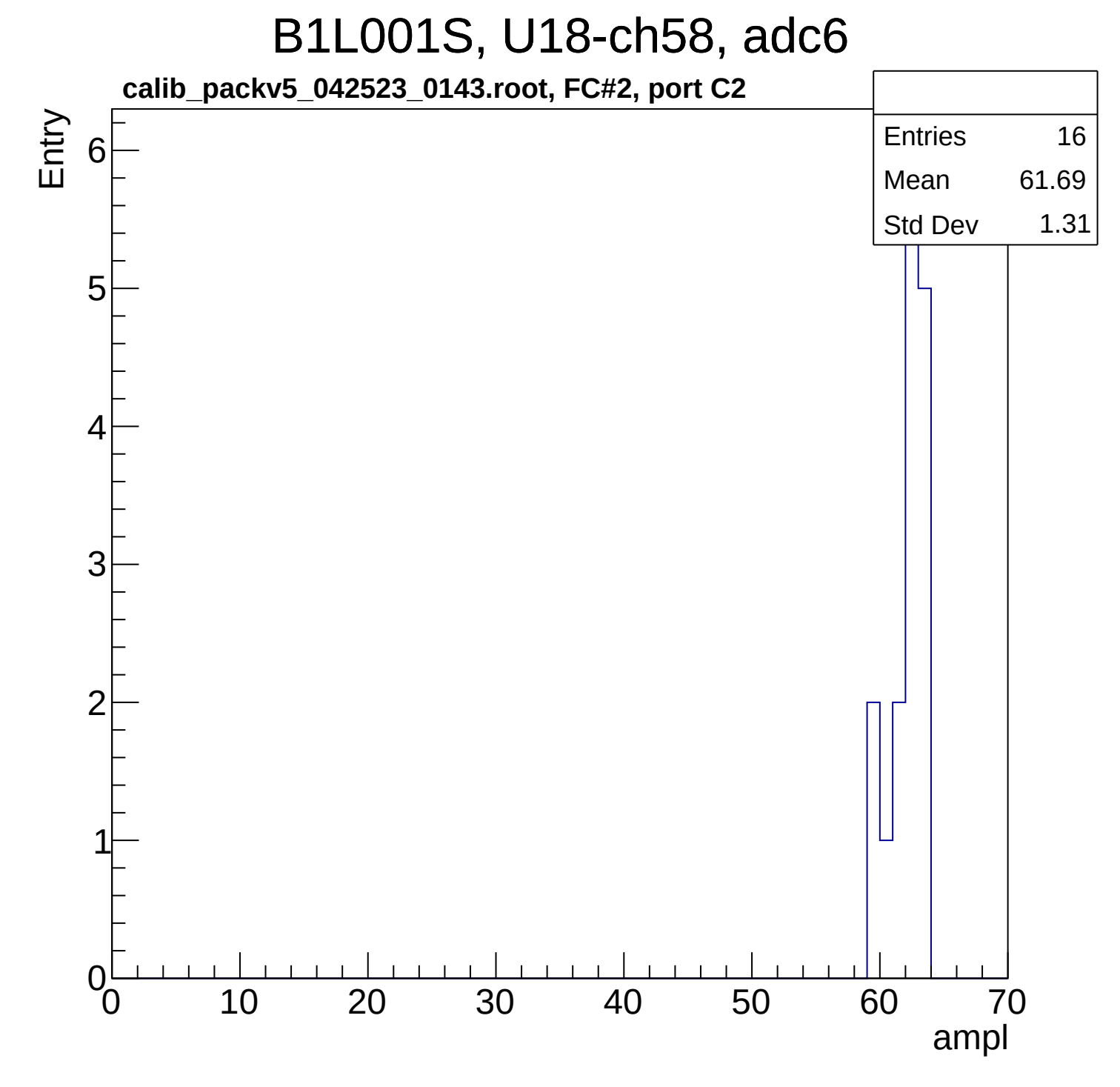

B1L001S, U18-ch58, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 151
Mean 34.5
Std Dev 3.204
Gaus mean : 34.8422
Gaus Width: 3.4507
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

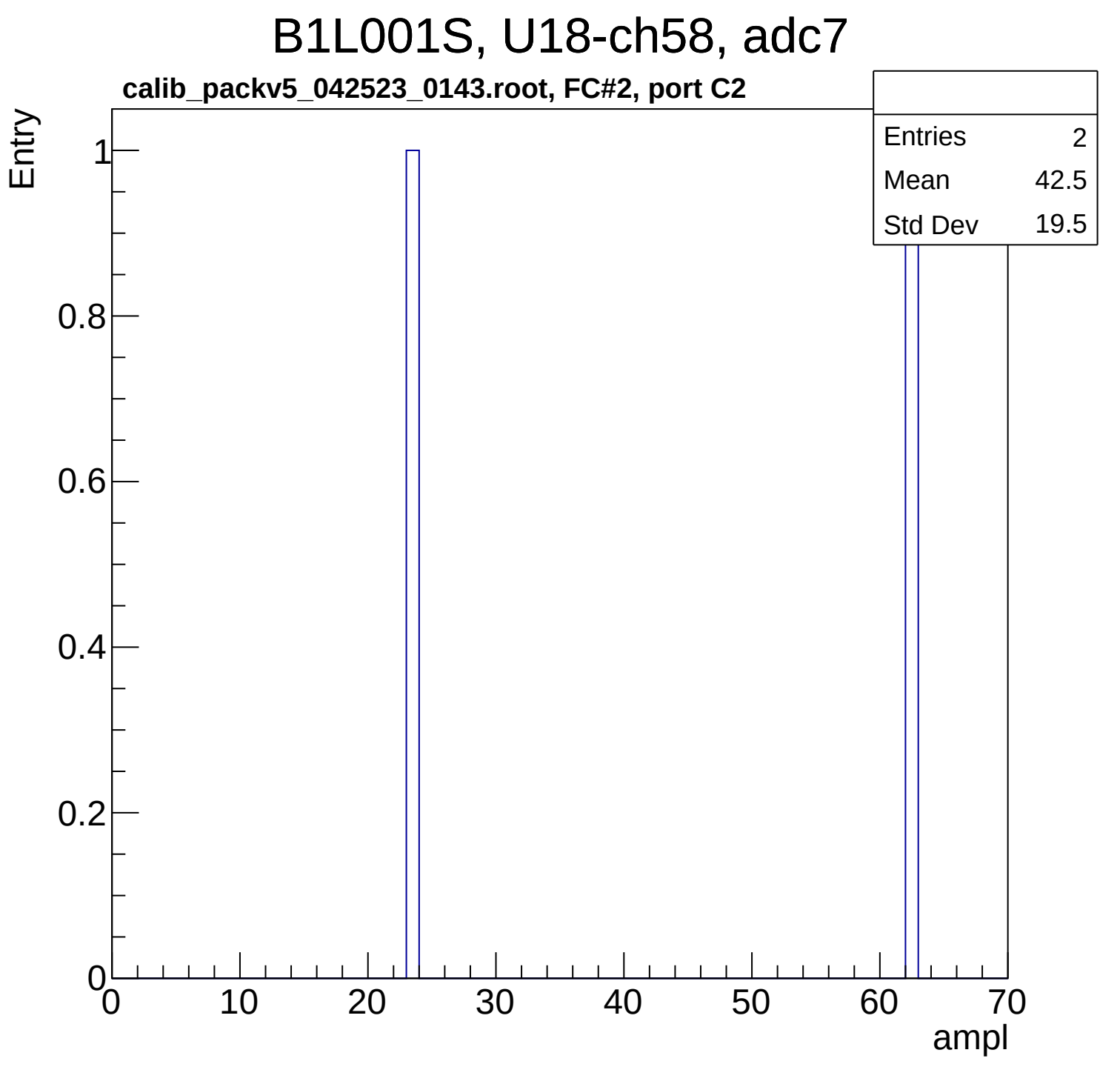

B1L001S, U18-ch58, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 139
Mean 42.06
Std Dev 3.478
Gaus mean : 42.4816
Gaus Width: 3.1869
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

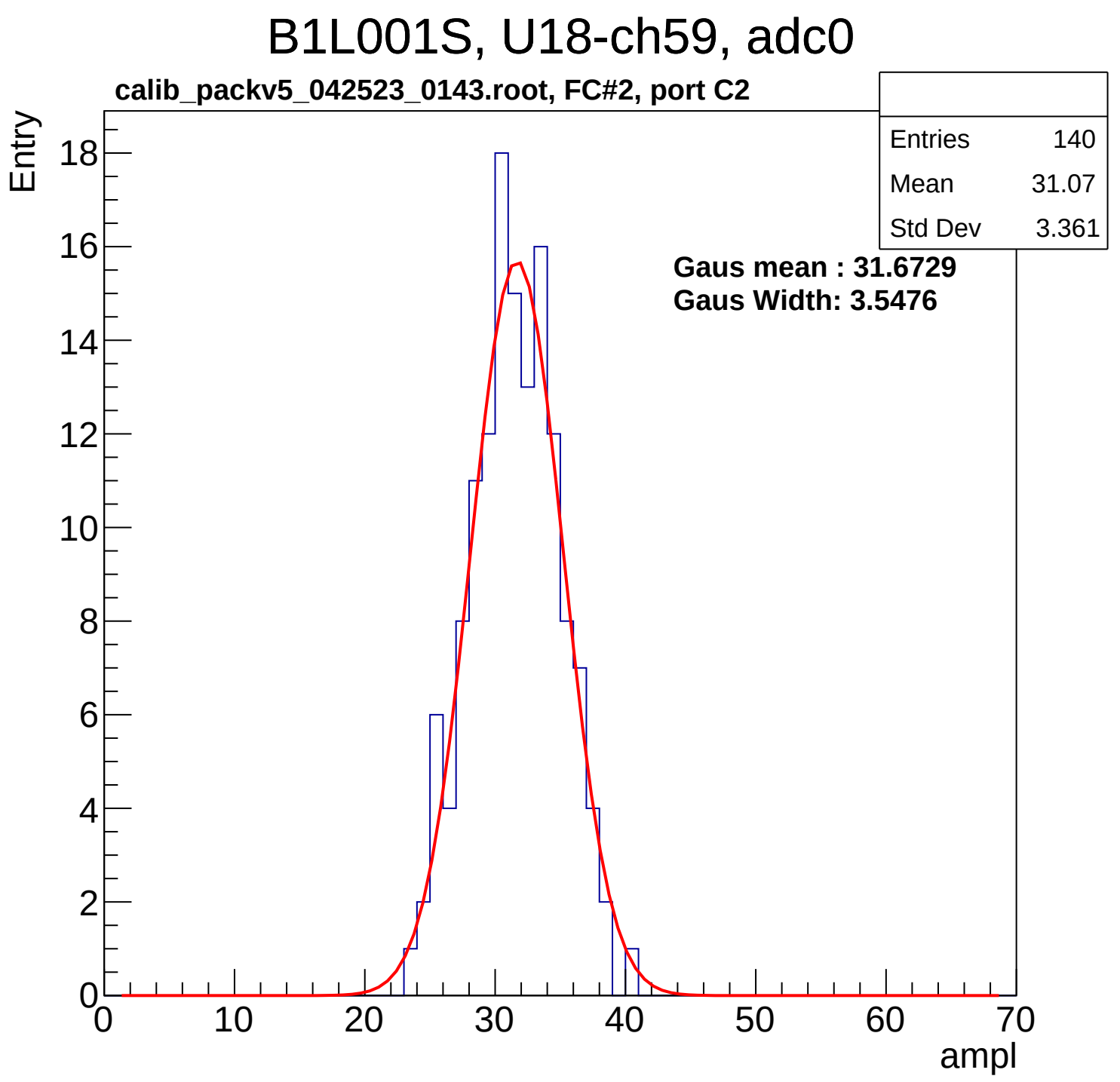

B1L001S, U18-ch58, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 115
Mean 48.28
Std Dev 3.253
Entry
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl

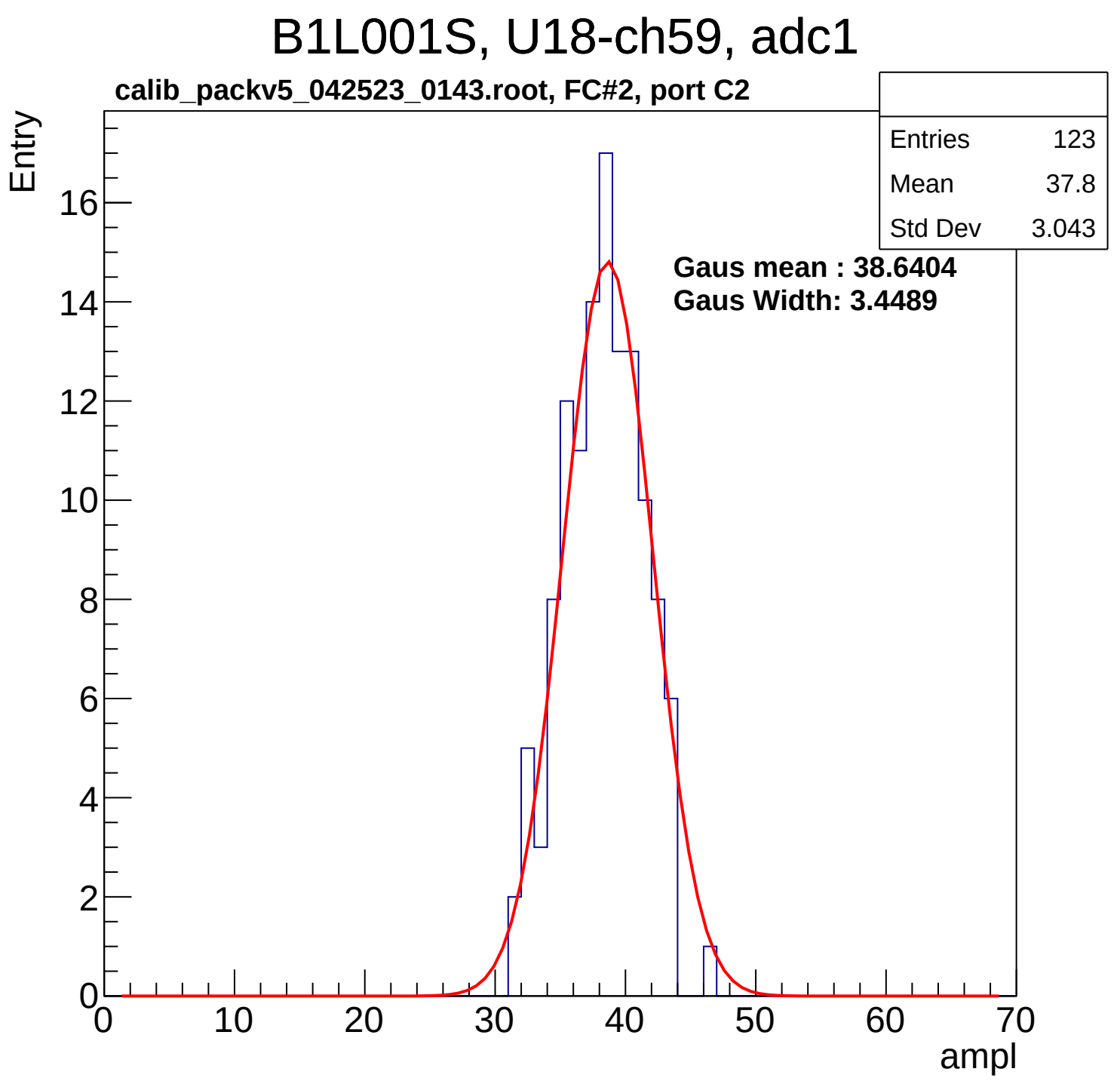

B1L001S, U18-ch58, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 143
Mean 53.92
Std Dev 5.732
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

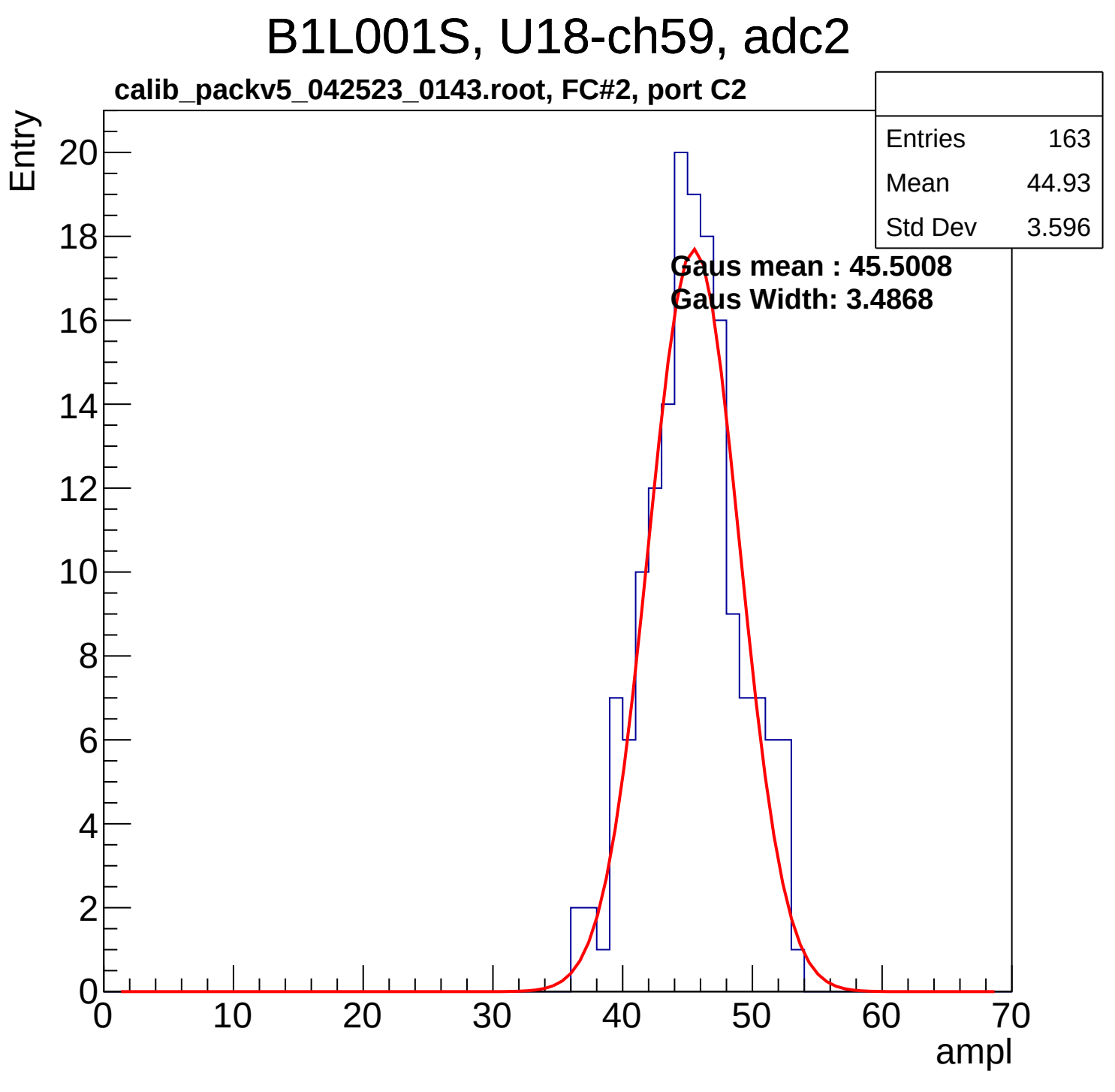

B1L001S, U18-ch58, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 91
Mean 59.34
Std Dev 6.698
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

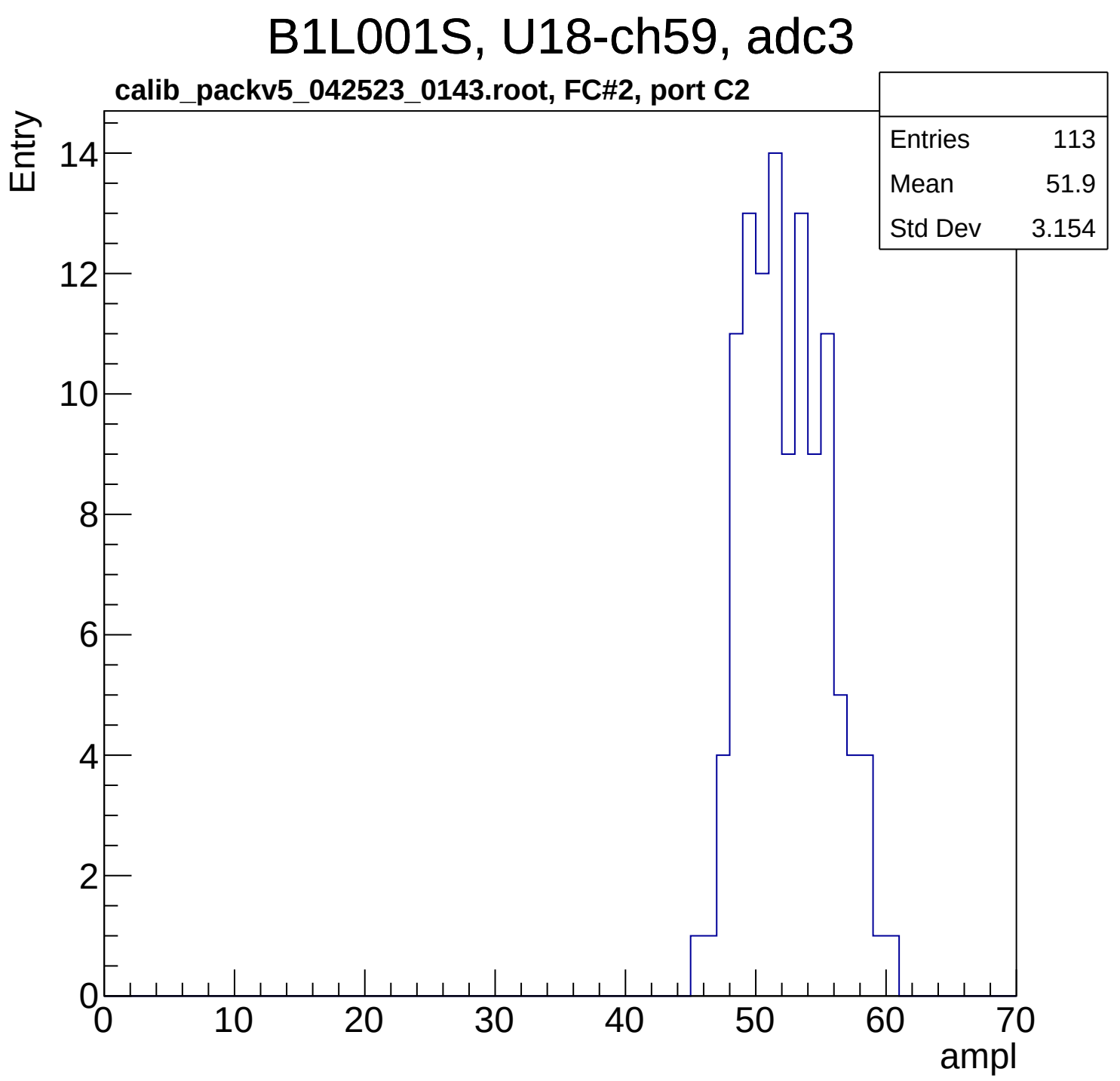

B1L001S, U18-ch58, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 16
Mean 61.69
Std Dev 1.31
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

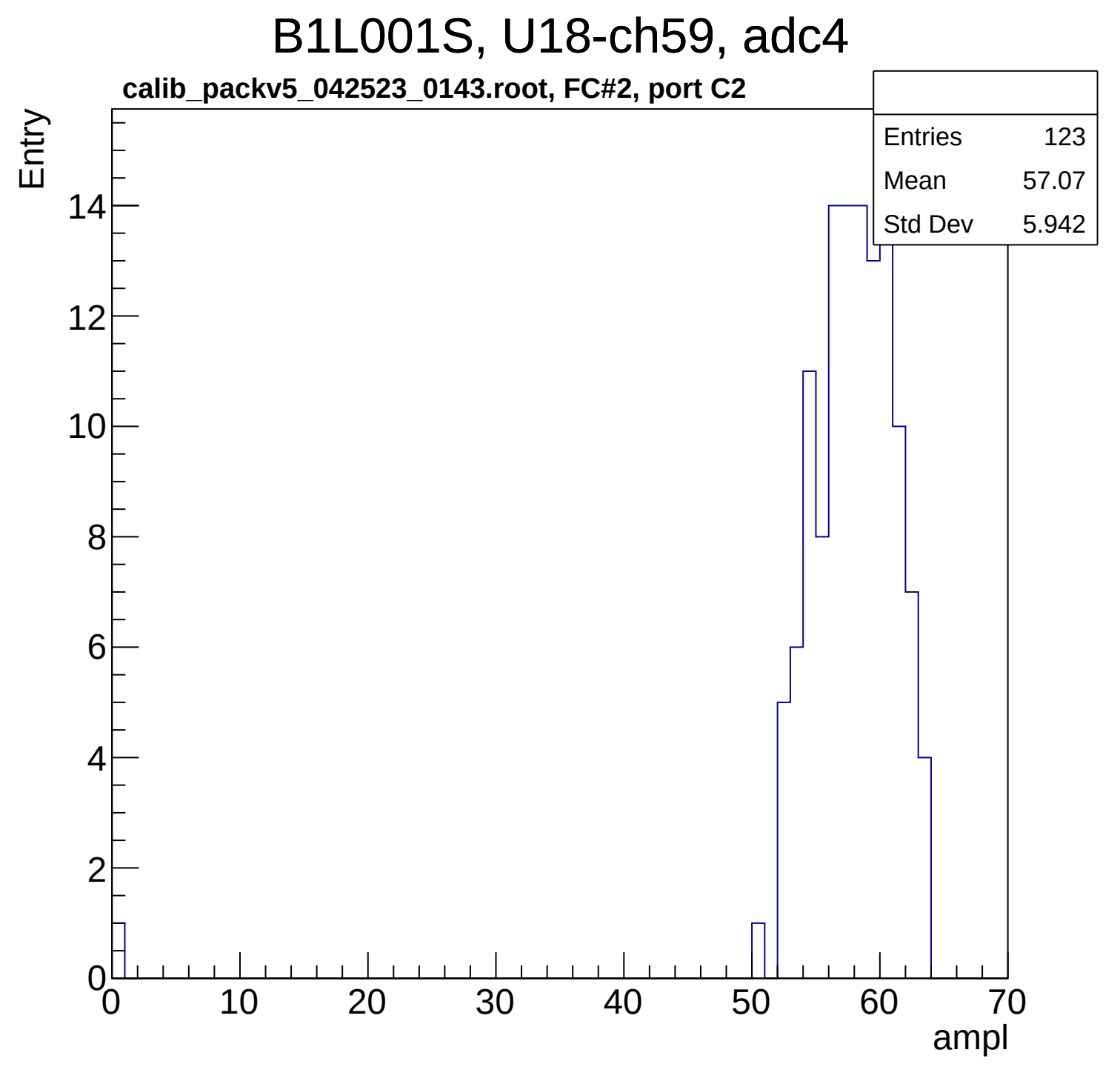

B1L001S, U18-ch58, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 42.5
Std Dev 19.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

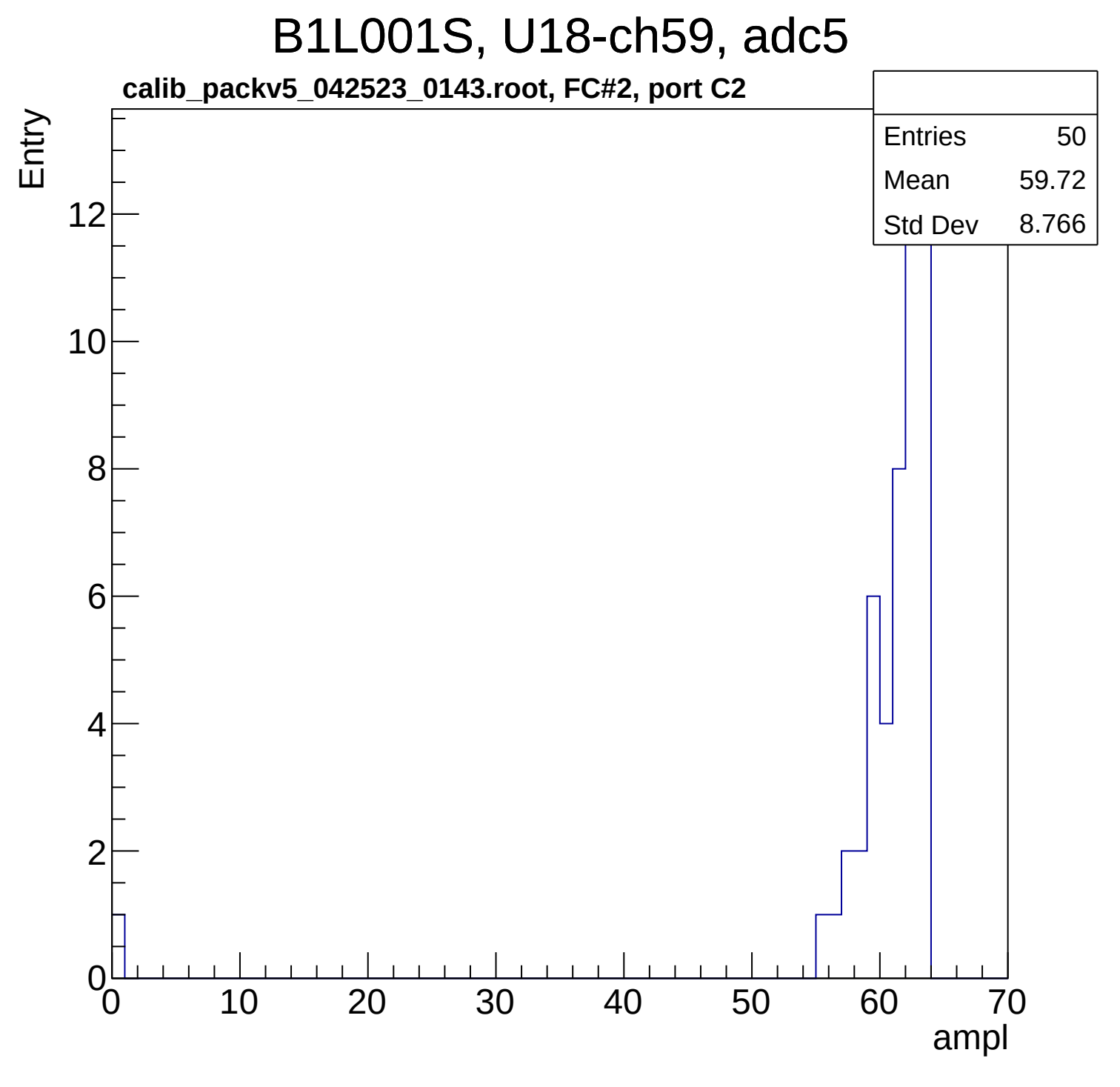

B1L001S, U18-ch59, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 140
Mean 31.07
Std Dev 3.361
Gaus mean : 31.6729
Gaus Width: 3.5476
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

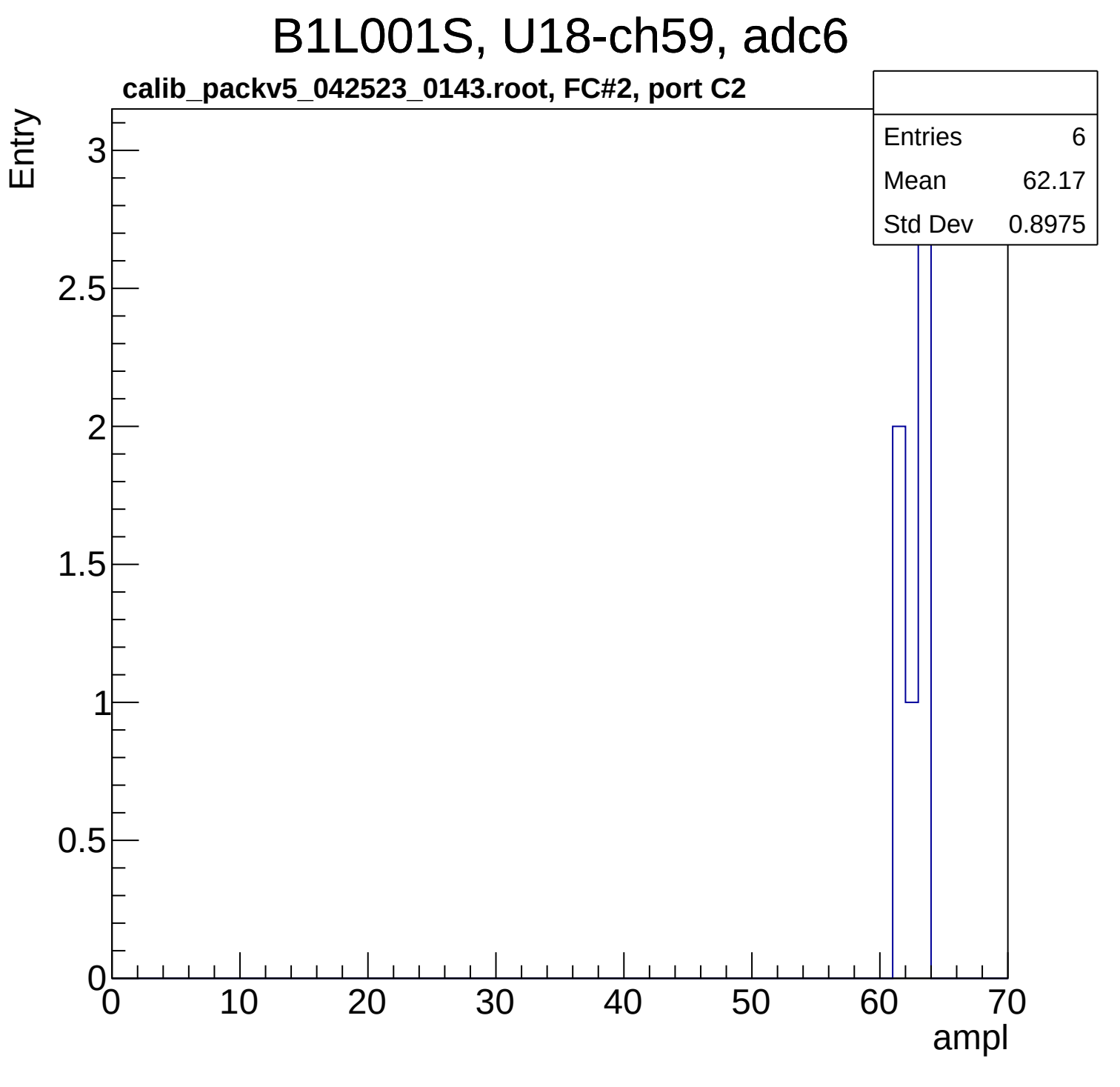

B1L001S, U18-ch59, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 123
Mean 37.8
Std Dev 3.043
Gaus mean : 38.6404
Gaus Width: 3.4489
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

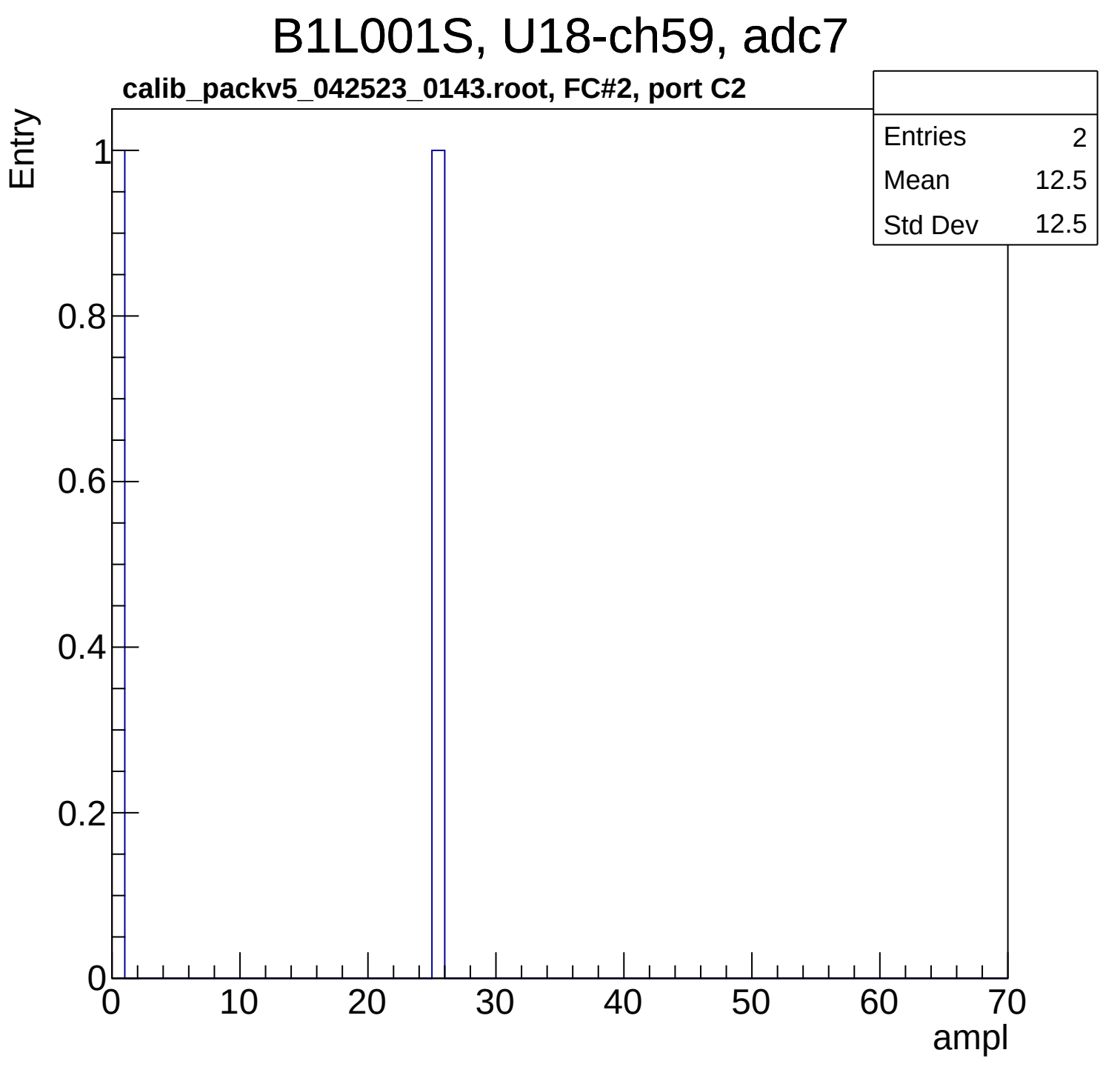

B1L001S, U18-ch59, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 163
Mean 44.93
Std Dev 3.596
Gaus mean : 45.5008
Gaus Width: 3.4868
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

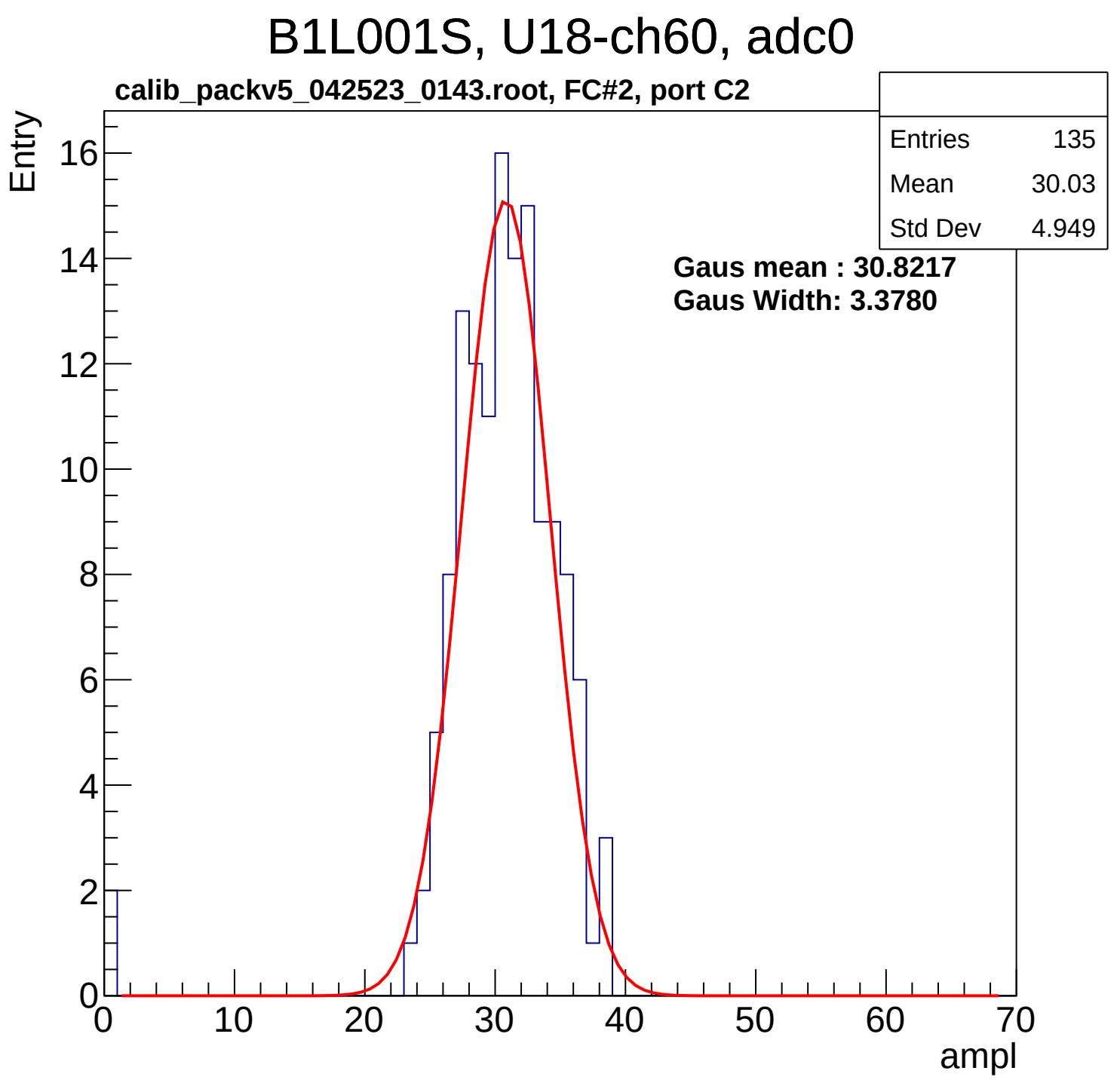

B1L001S, U18-ch59, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 113
Mean 51.9
Std Dev 3.154
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl

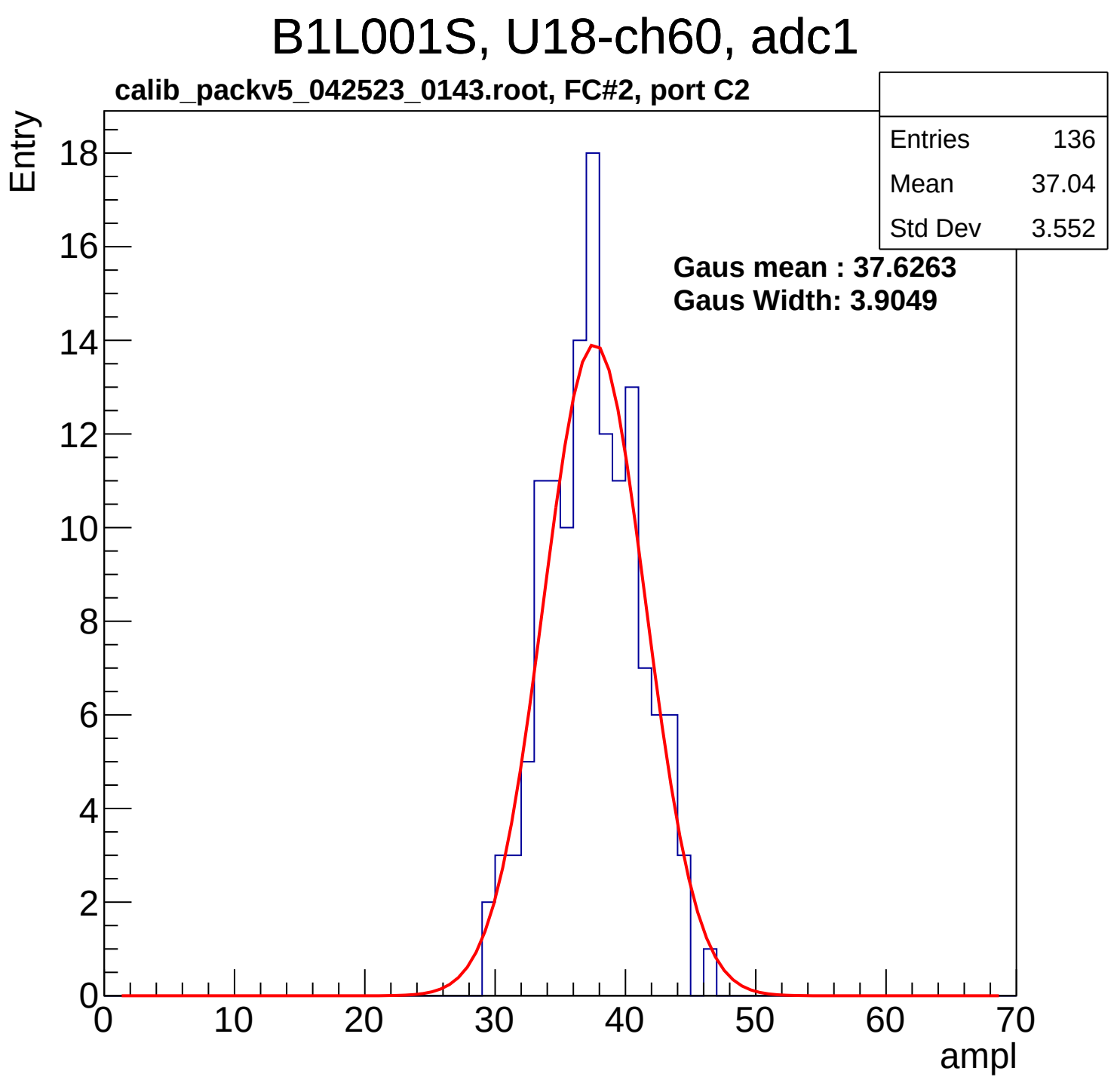

B1L001S, U18-ch59, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 123
Mean 57.07
Std Dev 5.942
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

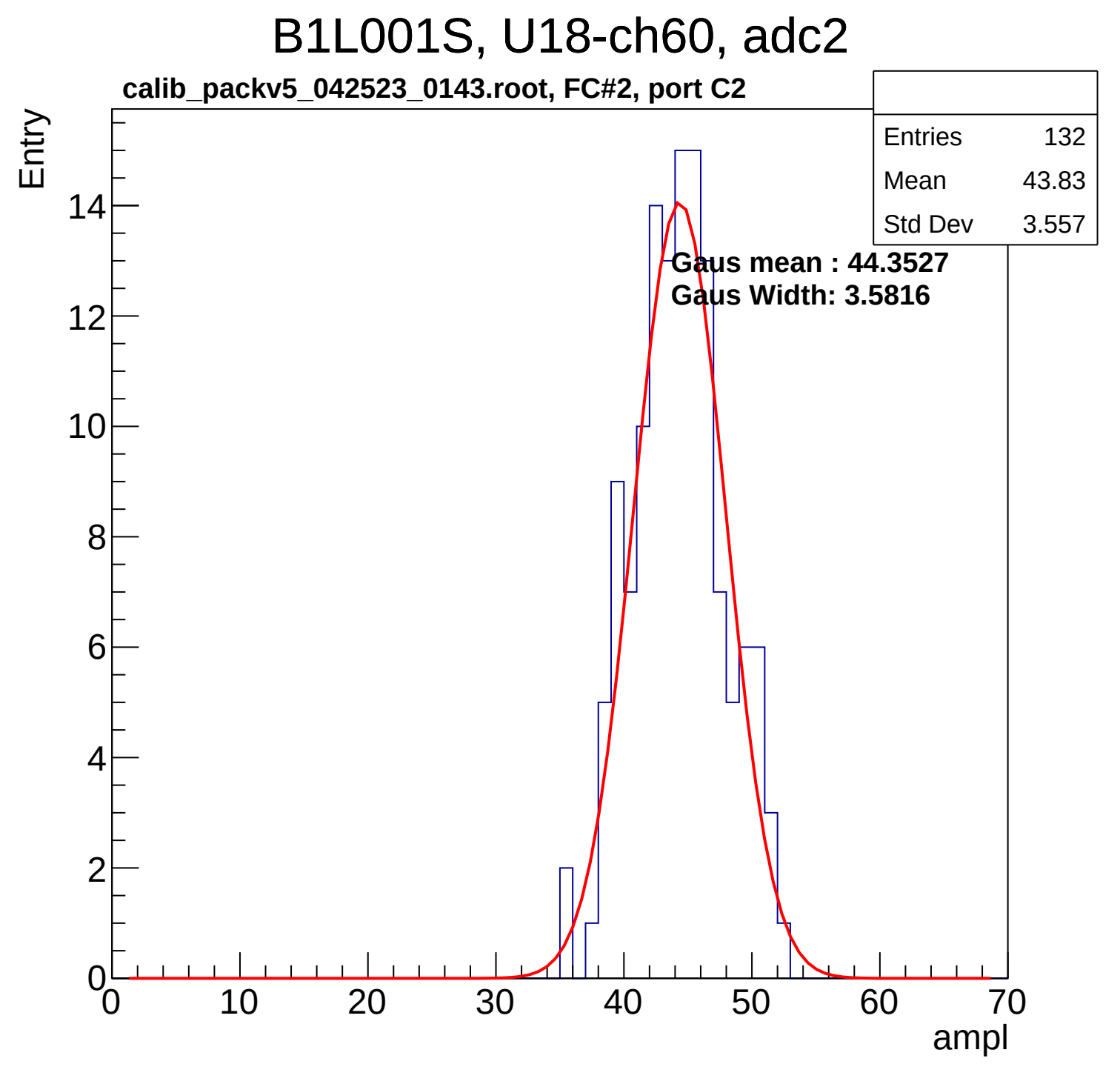

B1L001S, U18-ch59, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 50
Mean 59.72
Std Dev 8.766
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl

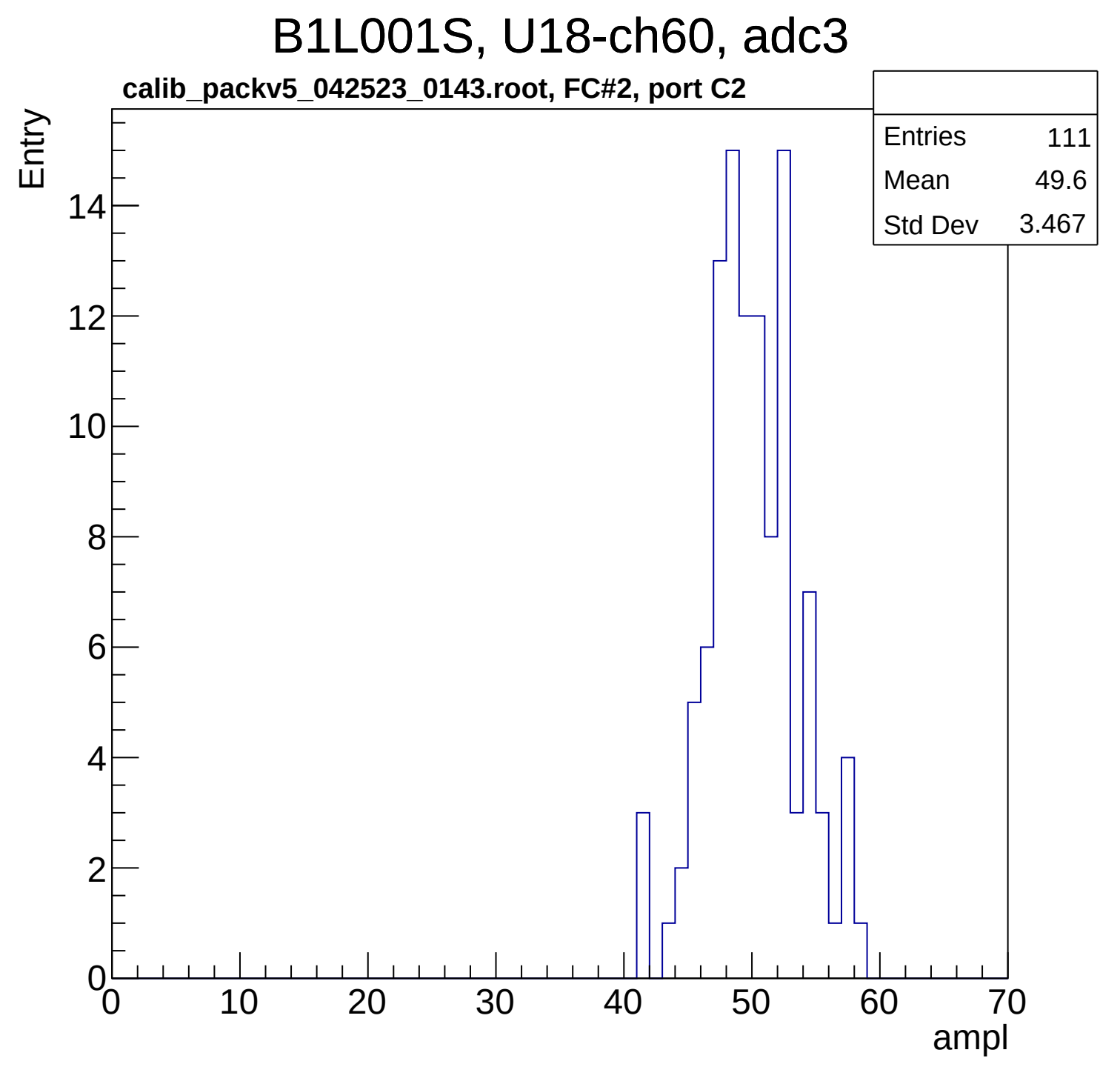

B1L001S, U18-ch59, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 6
Mean 62.17
Std Dev 0.8975
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

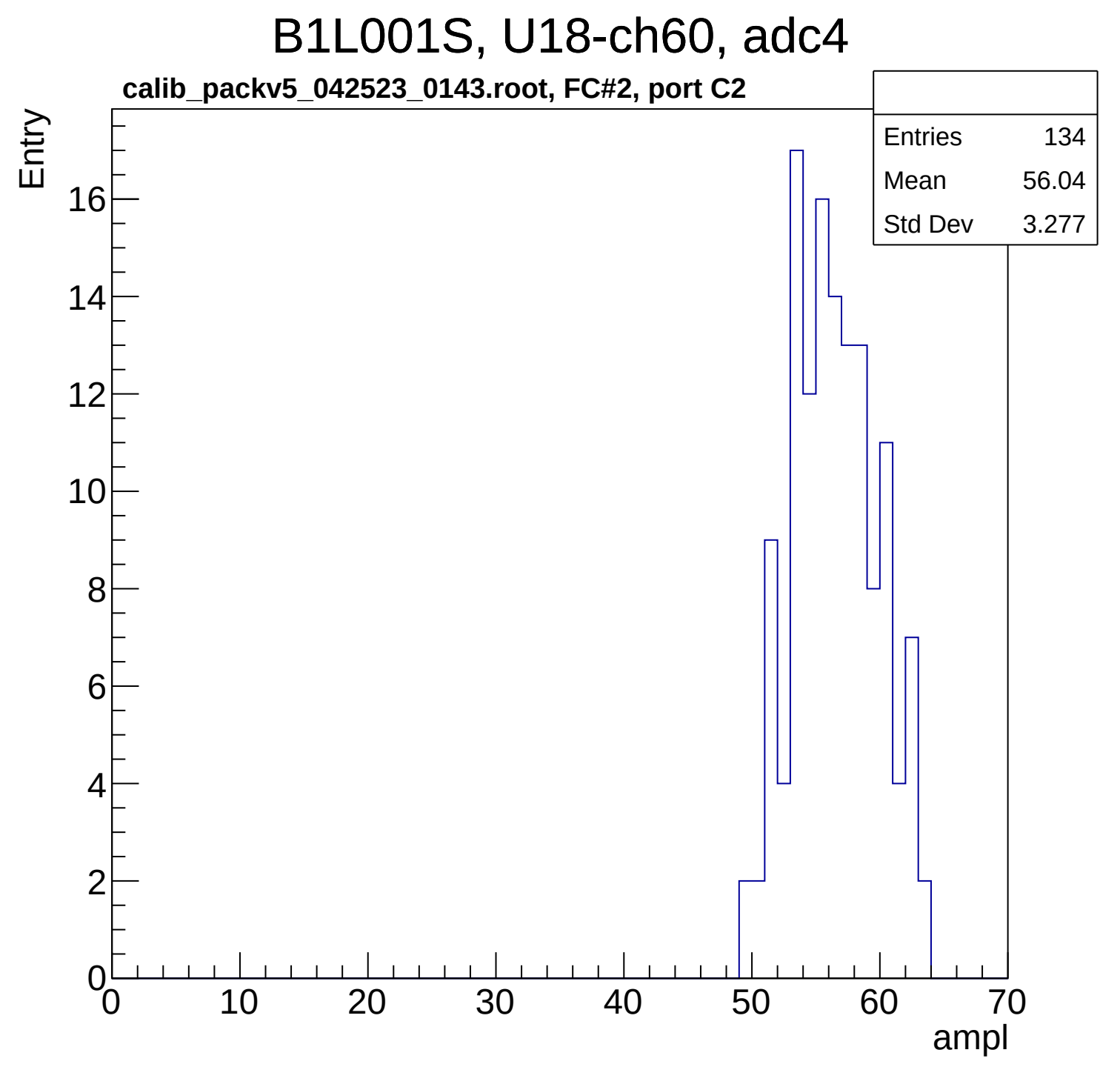

B1L001S, U18-ch59, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 12.5
Std Dev 12.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

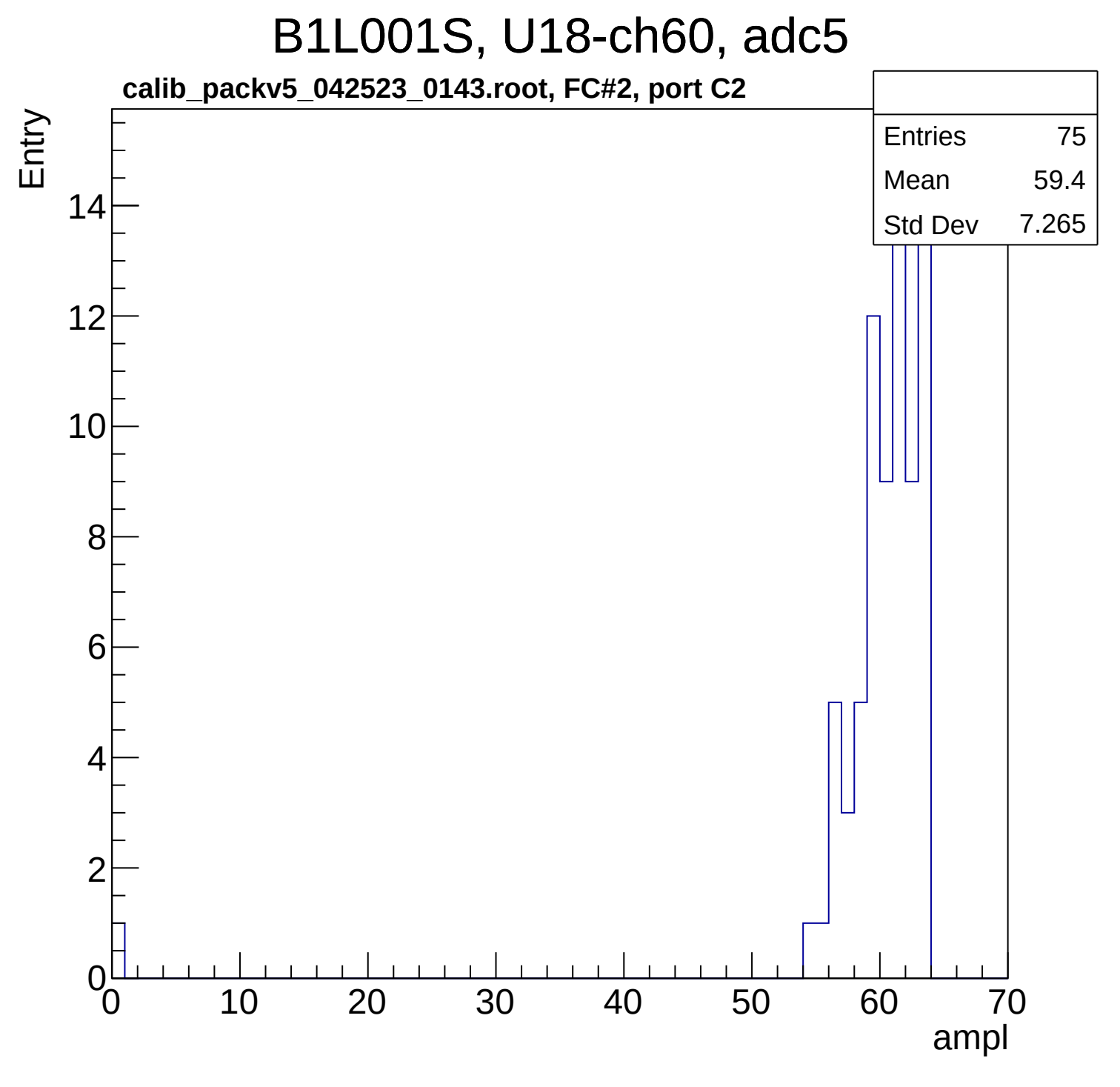

B1L001S, U18-ch60, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 135
Mean 30.03
Std Dev 4.949
Gaus mean : 30.8217
Gaus Width: 3.3780
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

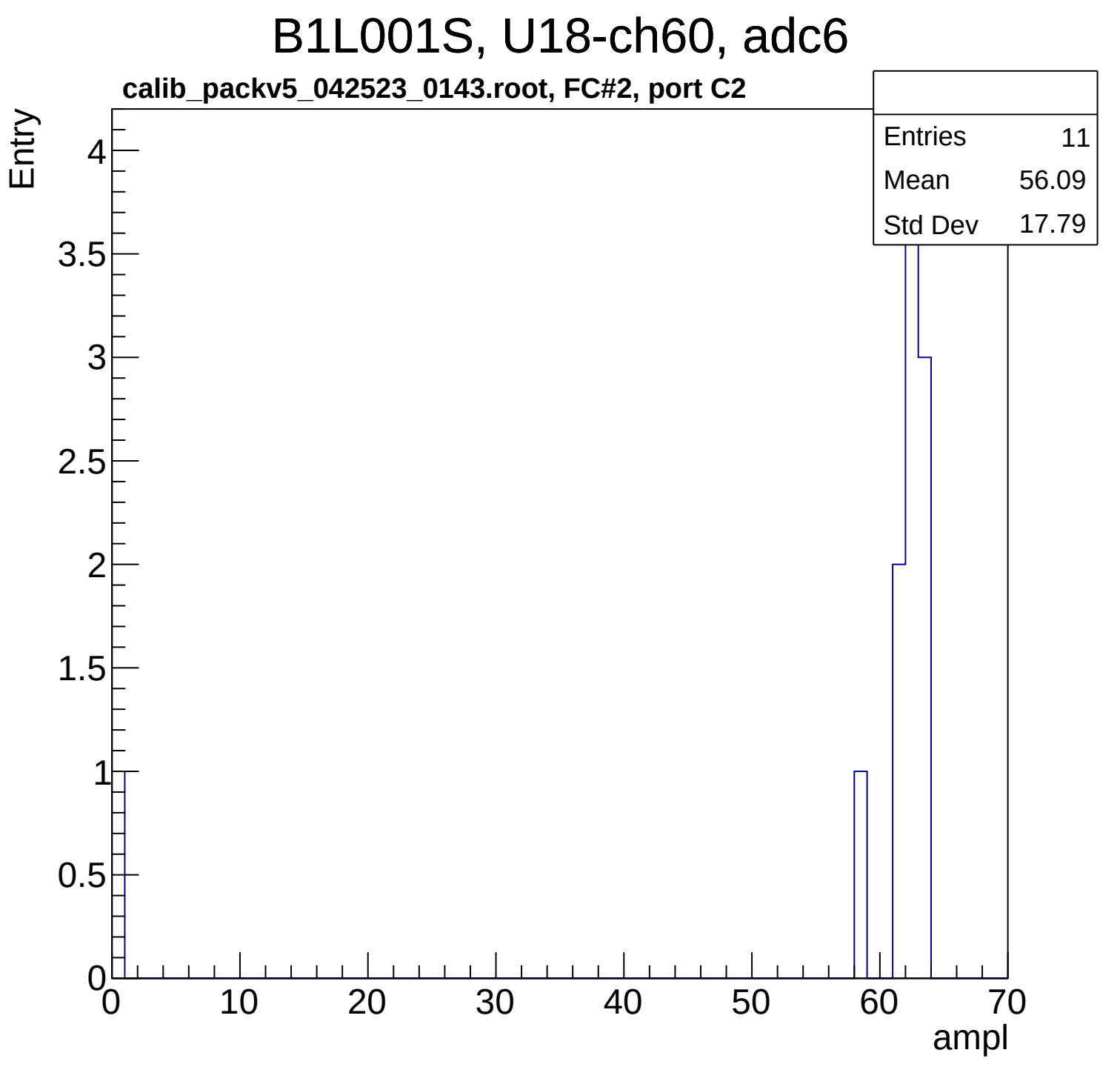

B1L001S, U18-ch60, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 136
Mean 37.04
Std Dev 3.552
Gaus mean : 37.6263
Gaus Width: 3.9049
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

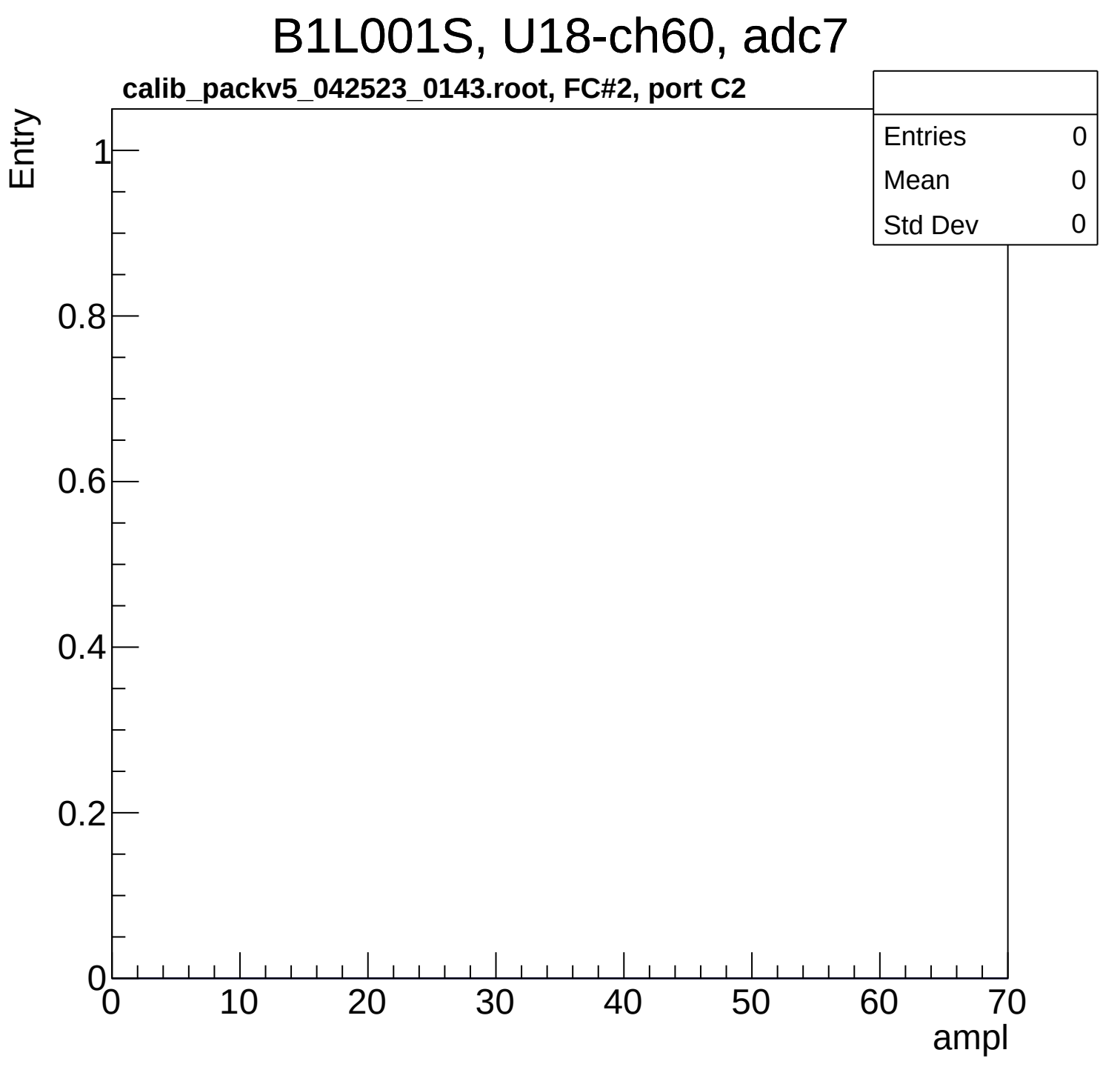

B1L001S, U18-ch60, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 132
Mean 43.83
Std Dev 3.557
Gaus mean : 44.3527
Gaus Width: 3.5816
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

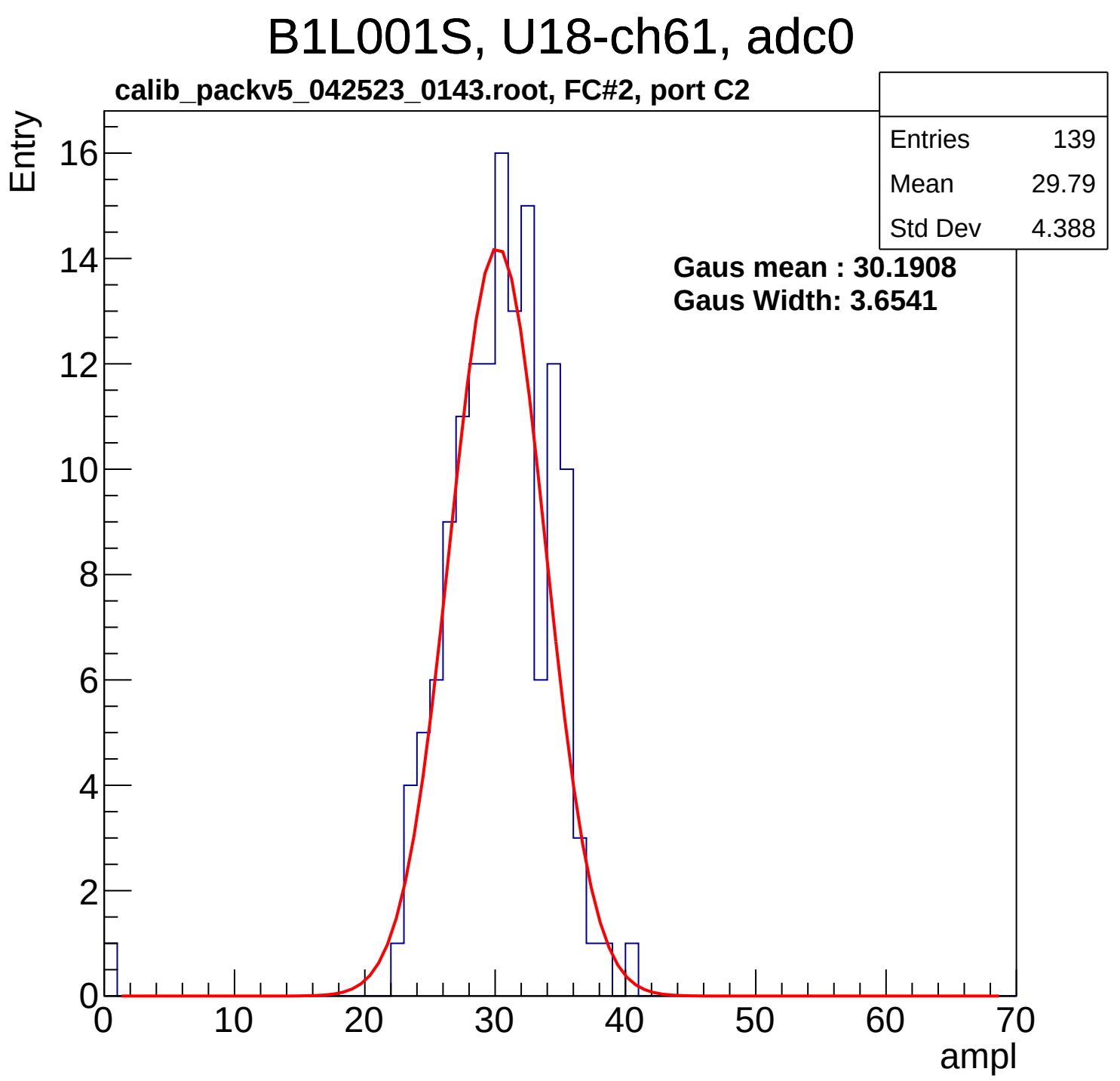

B1L001S, U18-ch60, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 111
Mean 49.6
Std Dev 3.467
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

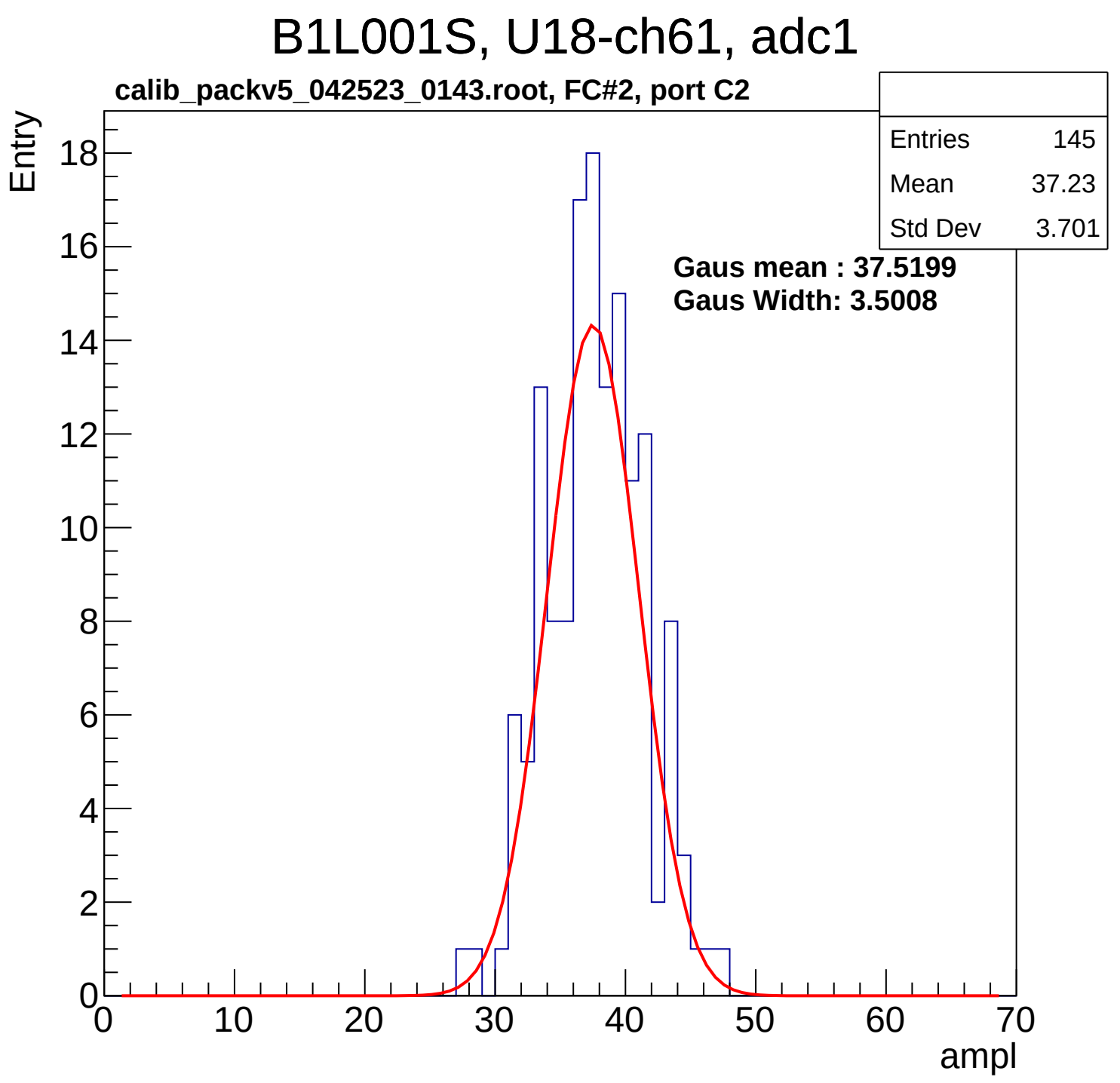

B1L001S, U18-ch60, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 134
Mean 56.04
Std Dev 3.277
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

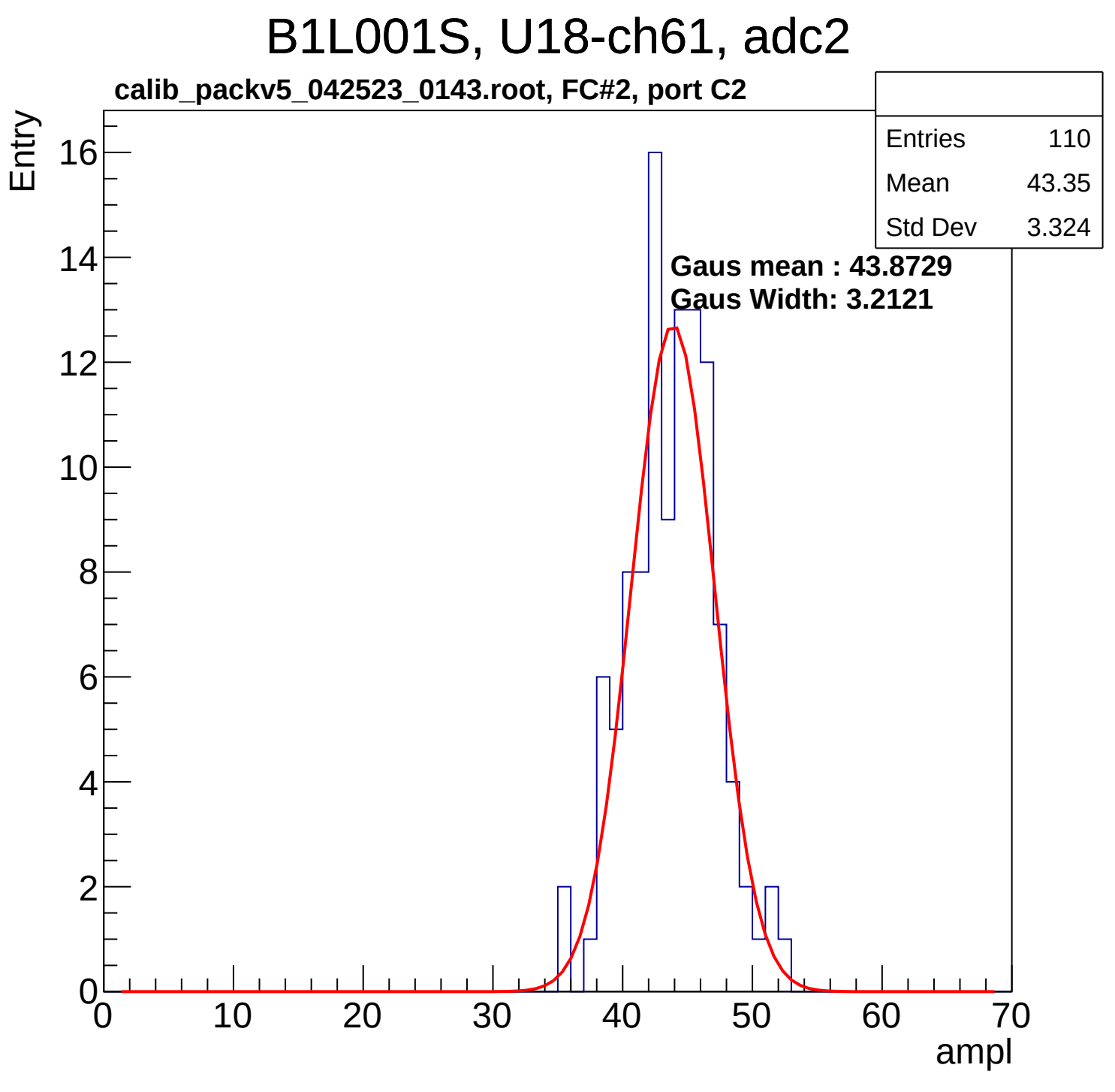

B1L001S, U18-ch60, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 75
Mean 59.4
Std Dev 7.265
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

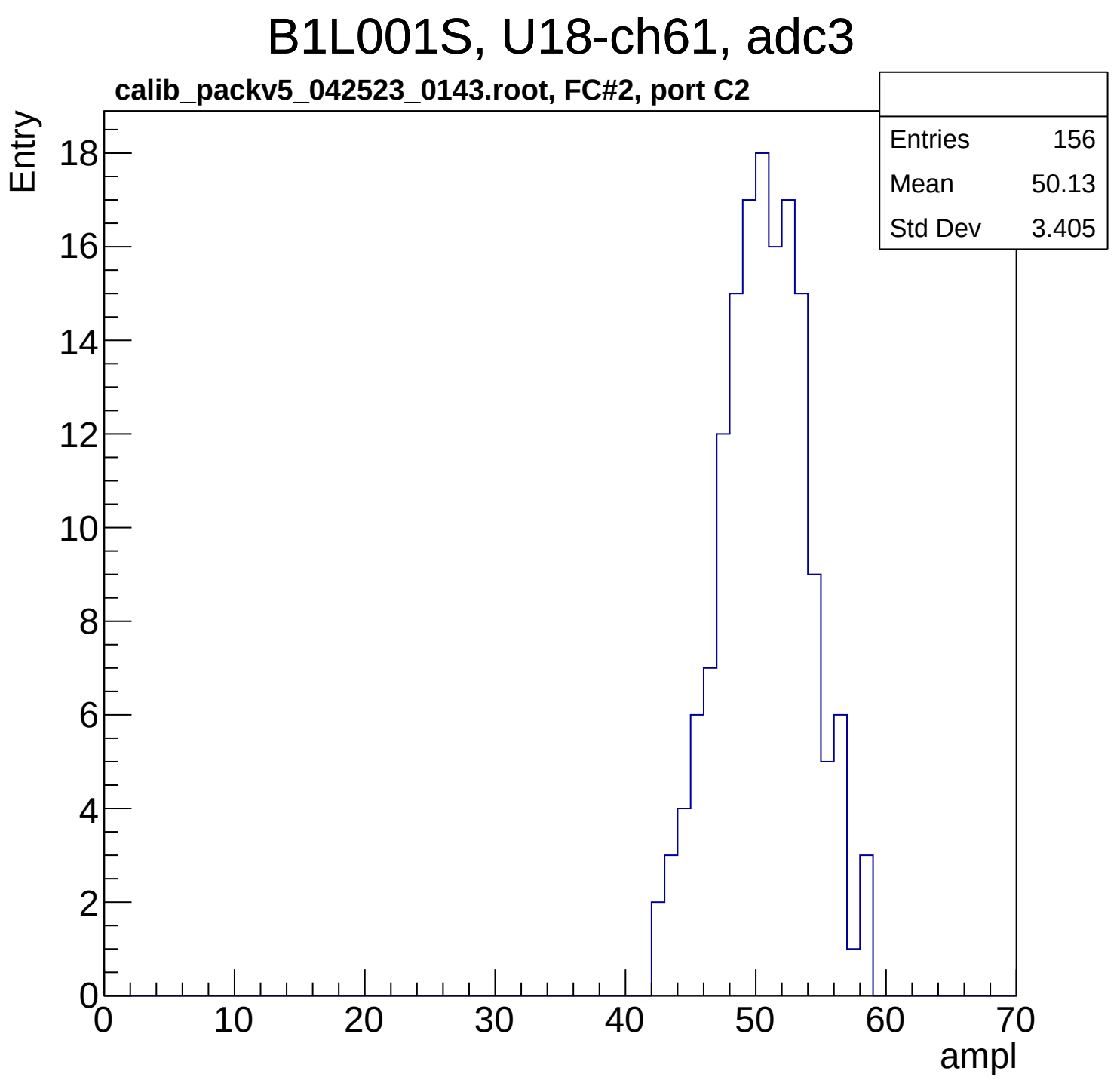

B1L001S, U18-ch60, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 11
Mean 56.09
Std Dev 17.79
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

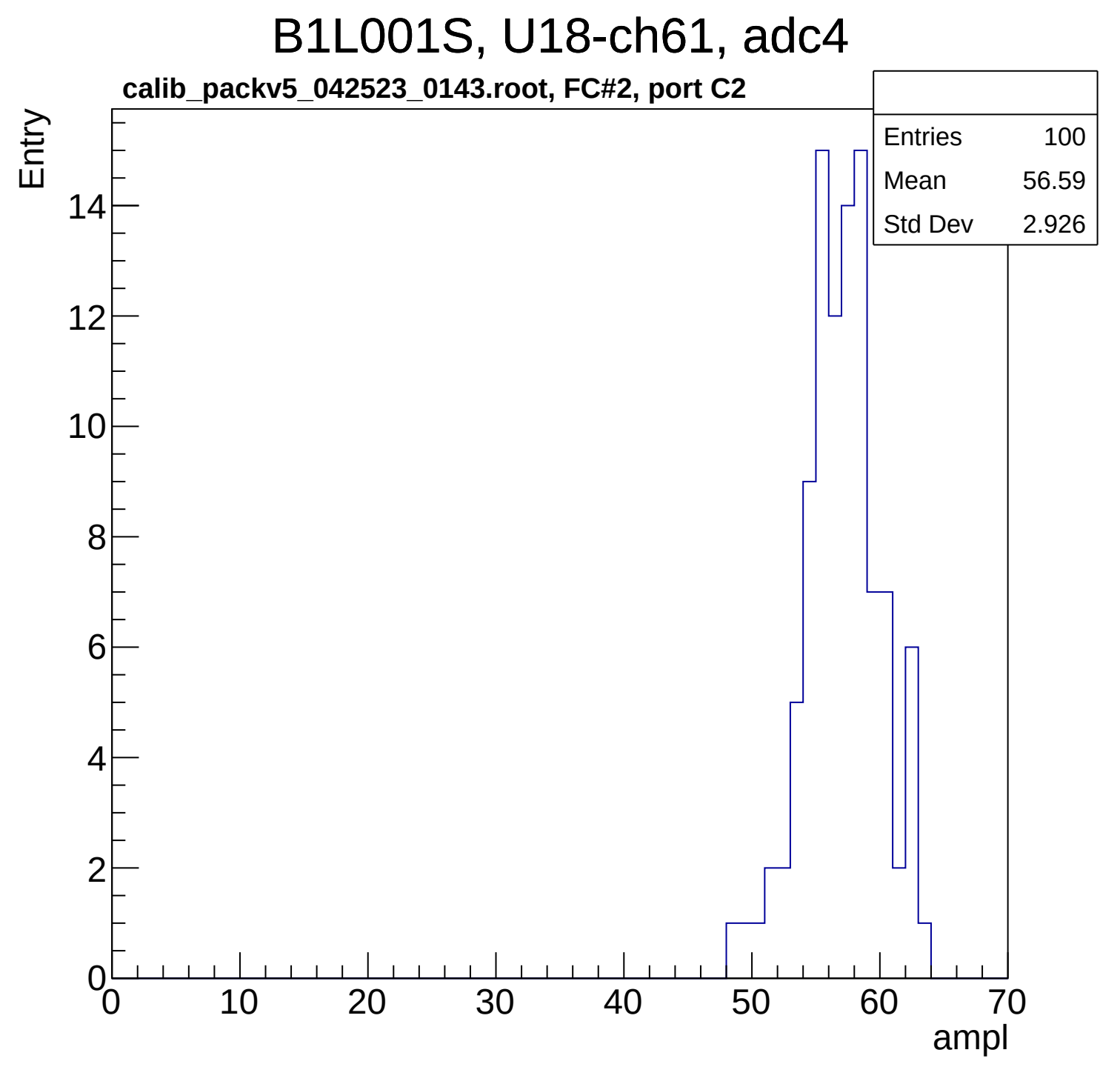

B1L001S, U18-ch60, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

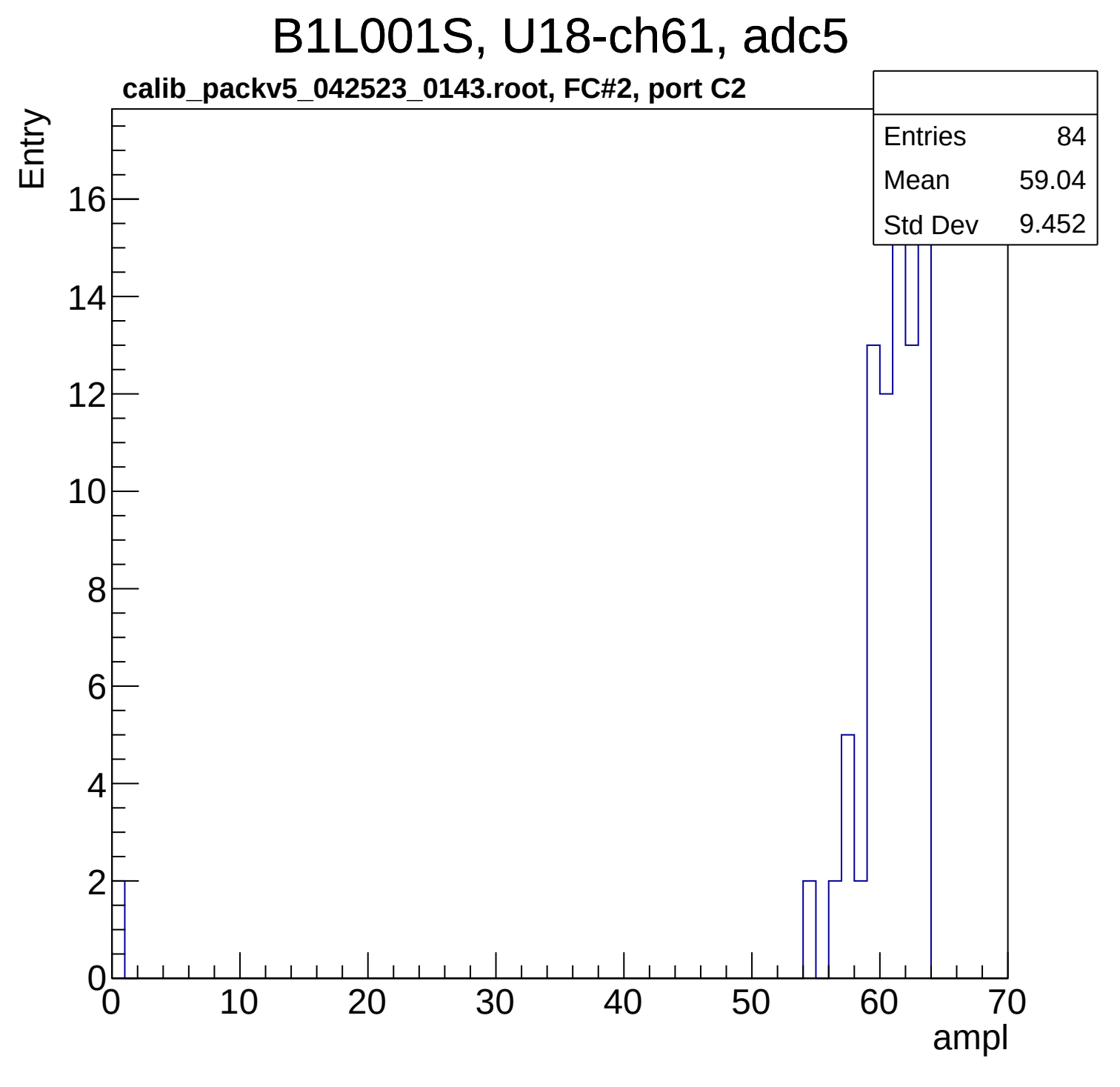

B1L001S, U18-ch61, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 139
Mean 29.79
Std Dev 4.388
Gaus mean : 30.1908
Gaus Width: 3.6541
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

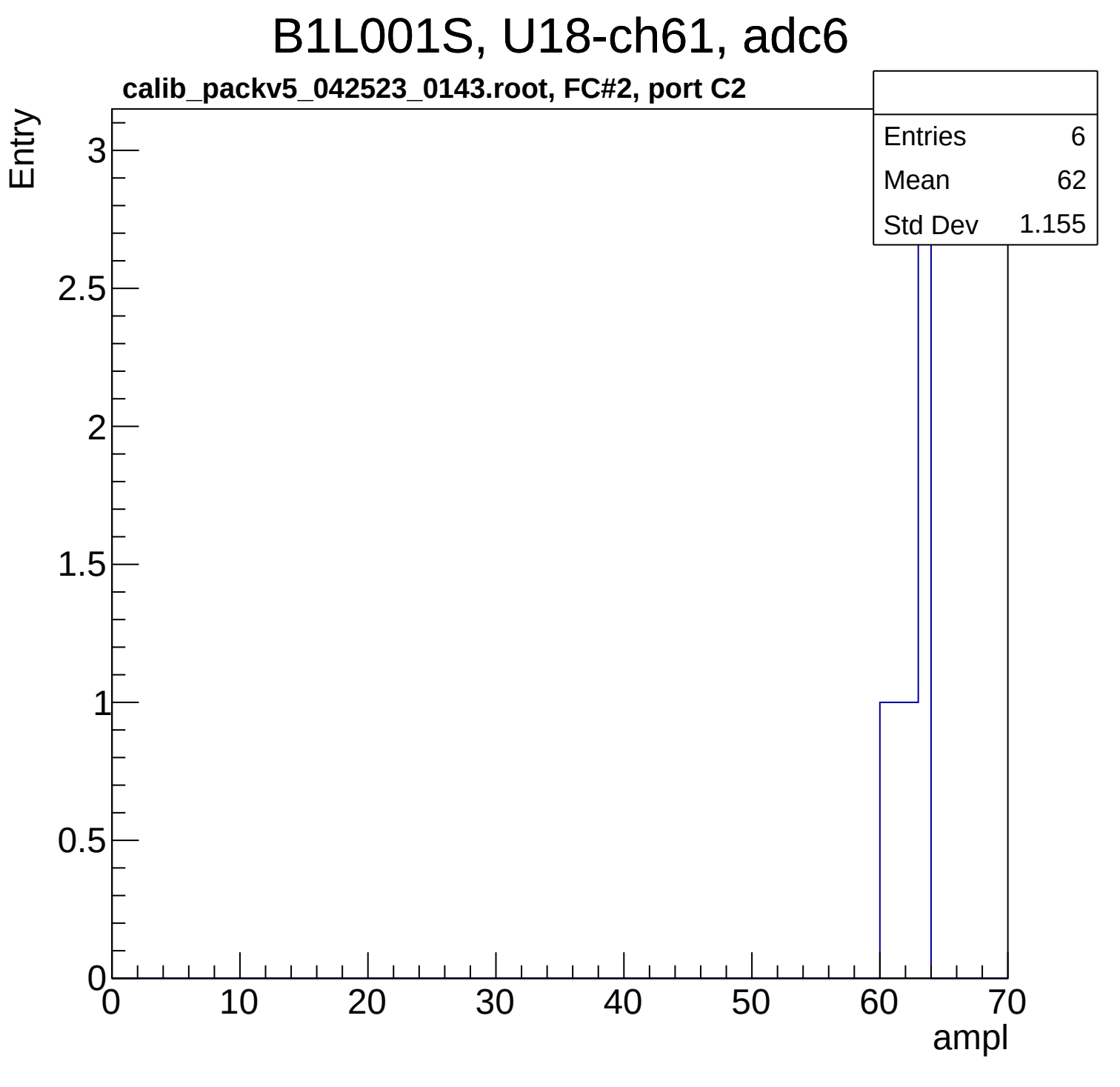

B1L001S, U18-ch61, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 145
Mean 37.23
Std Dev 3.701
Gaus mean : 37.5199
Gaus Width: 3.5008
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

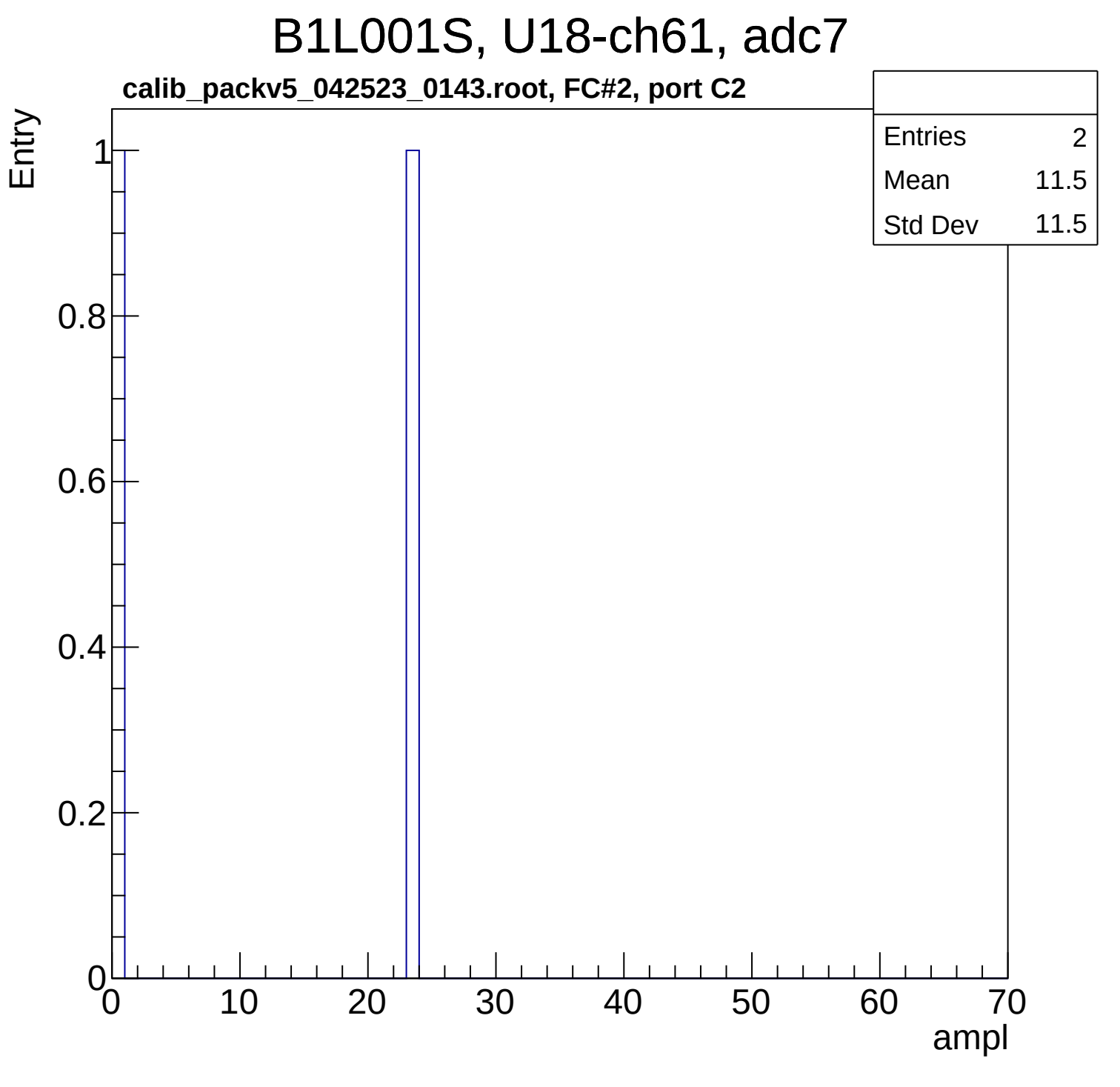

B1L001S, U18-ch61, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 110
Mean 43.35
Std Dev 3.324
Gaus mean : 43.8729
Gaus Width: 3.2121
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

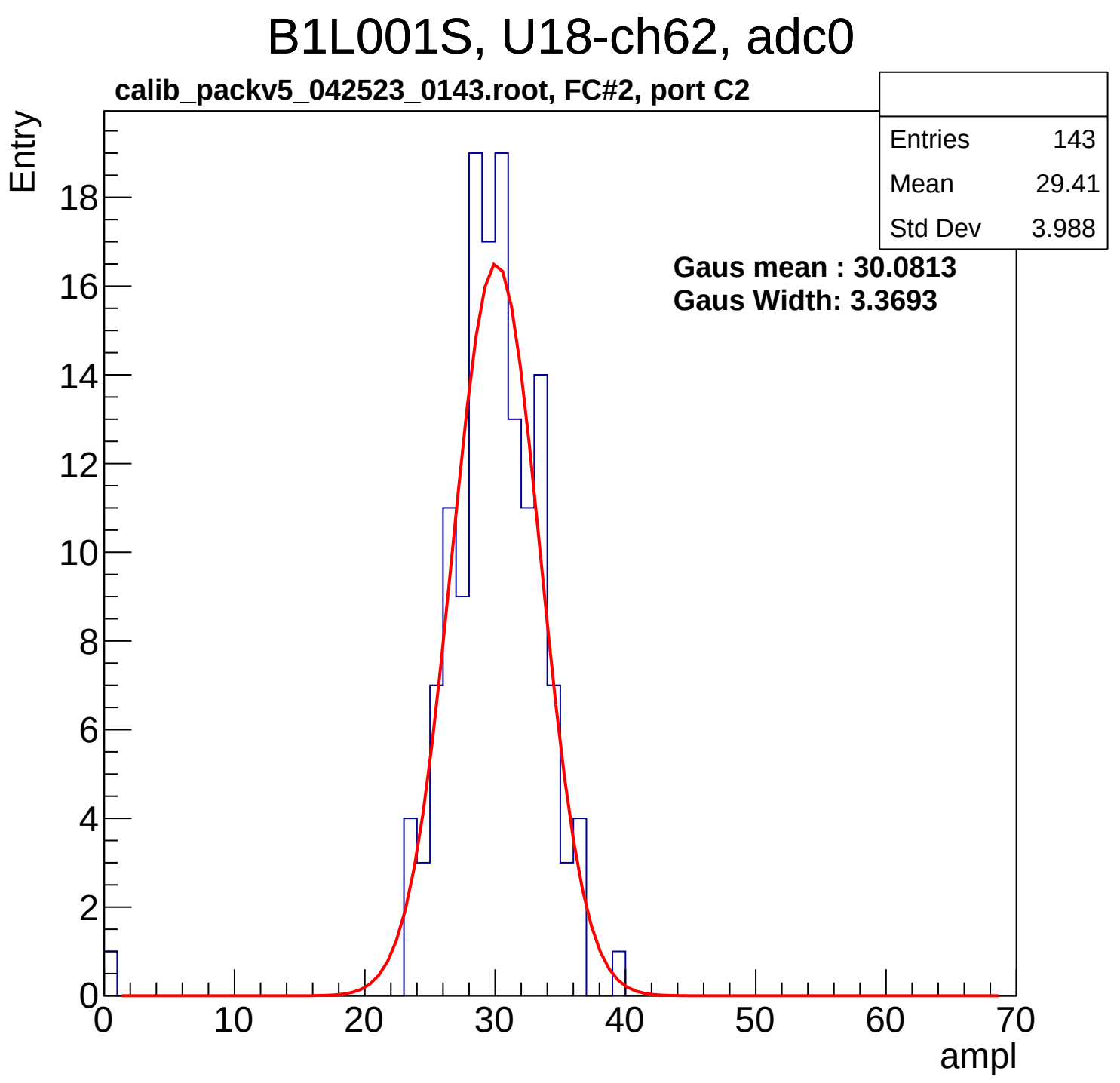

B1L001S, U18-ch61, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 156
Mean 50.13
Std Dev 3.405
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

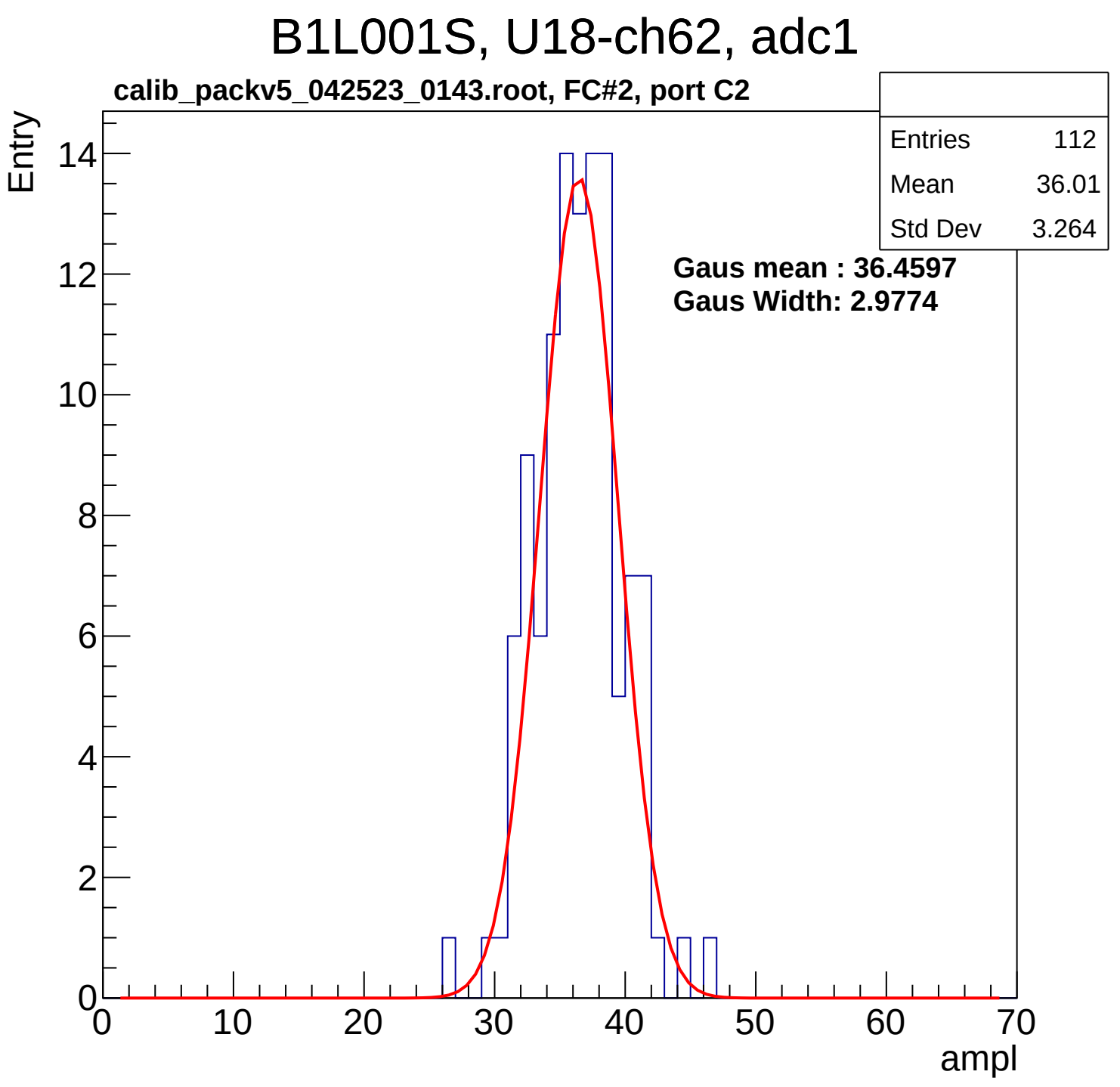

B1L001S, U18-ch61, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 100
Mean 56.59
Std Dev 2.926
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

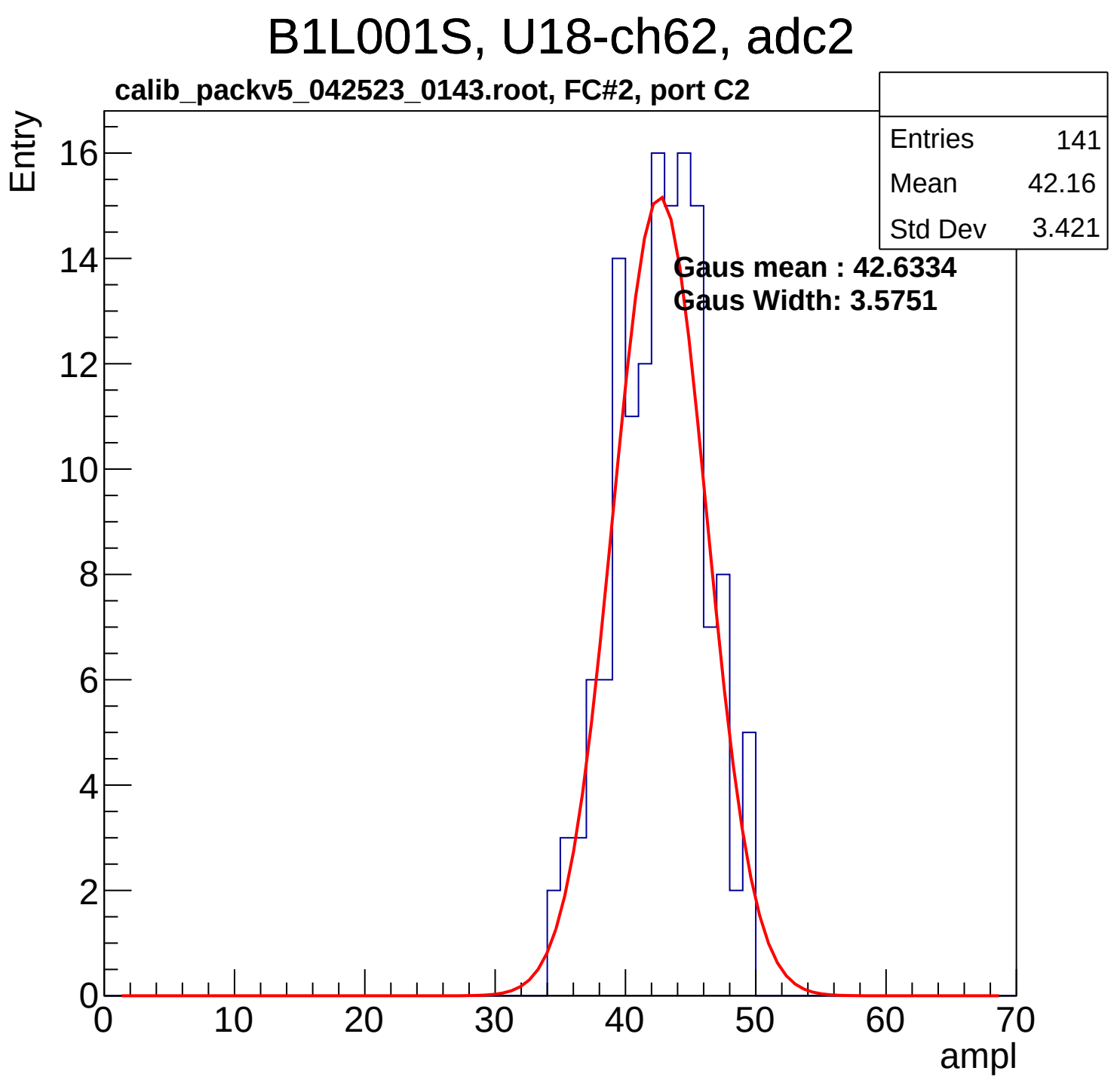

B1L001S, U18-ch61, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 84
Mean 59.04
Std Dev 9.452
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

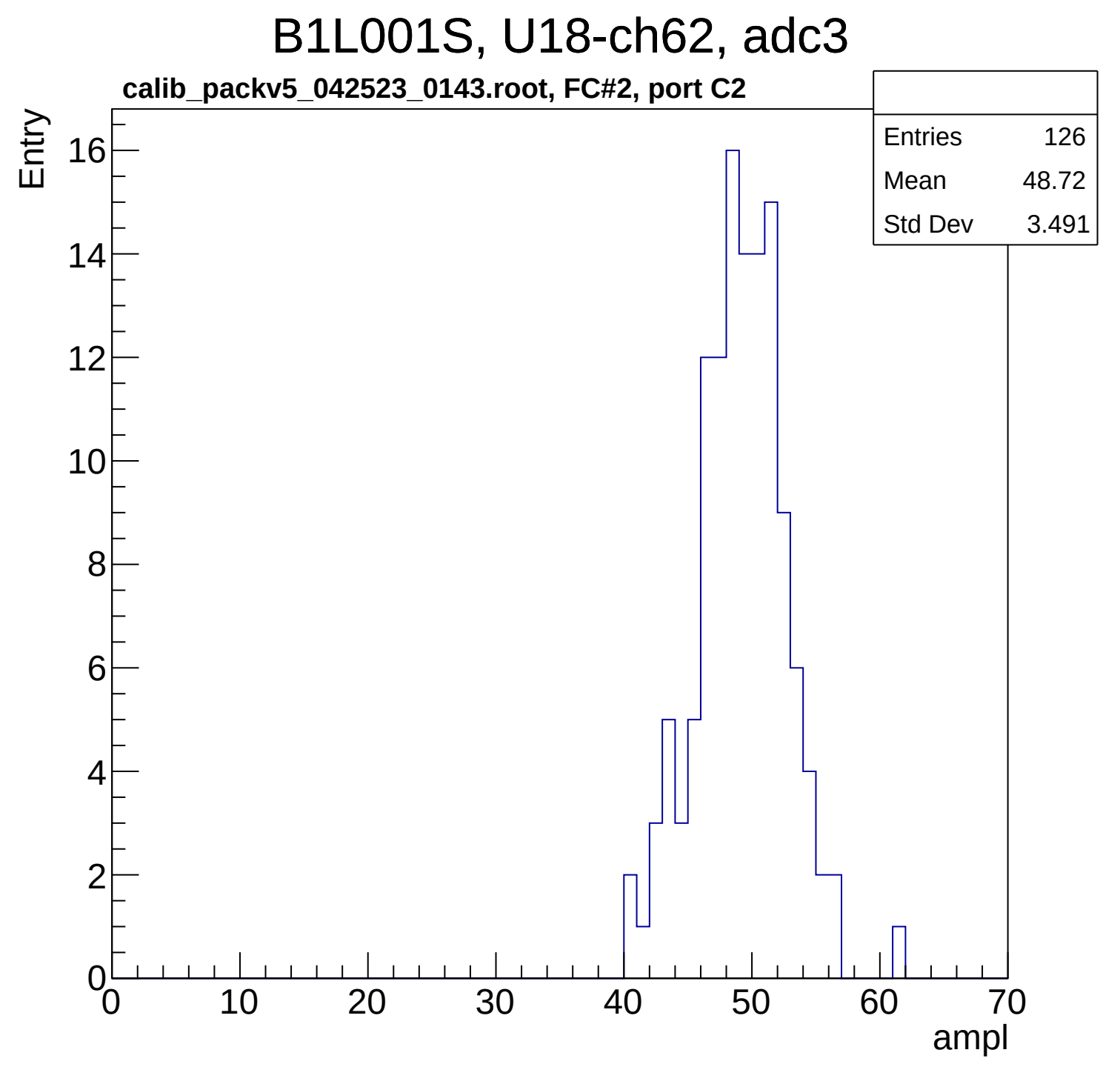

B1L001S, U18-ch61, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 6
Mean 62
Std Dev 1.155
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

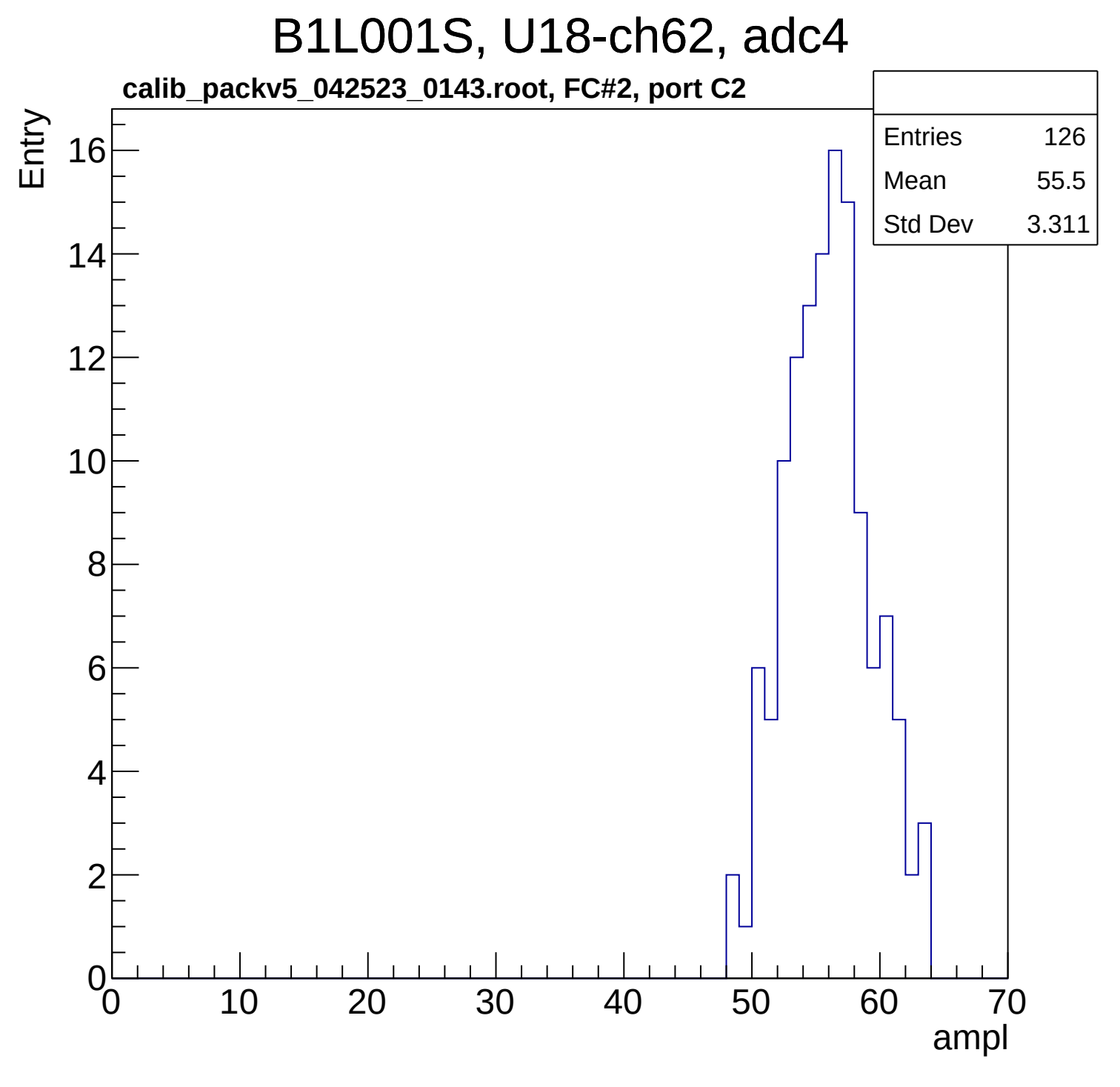

B1L001S, U18-ch61, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 11.5
Std Dev 11.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

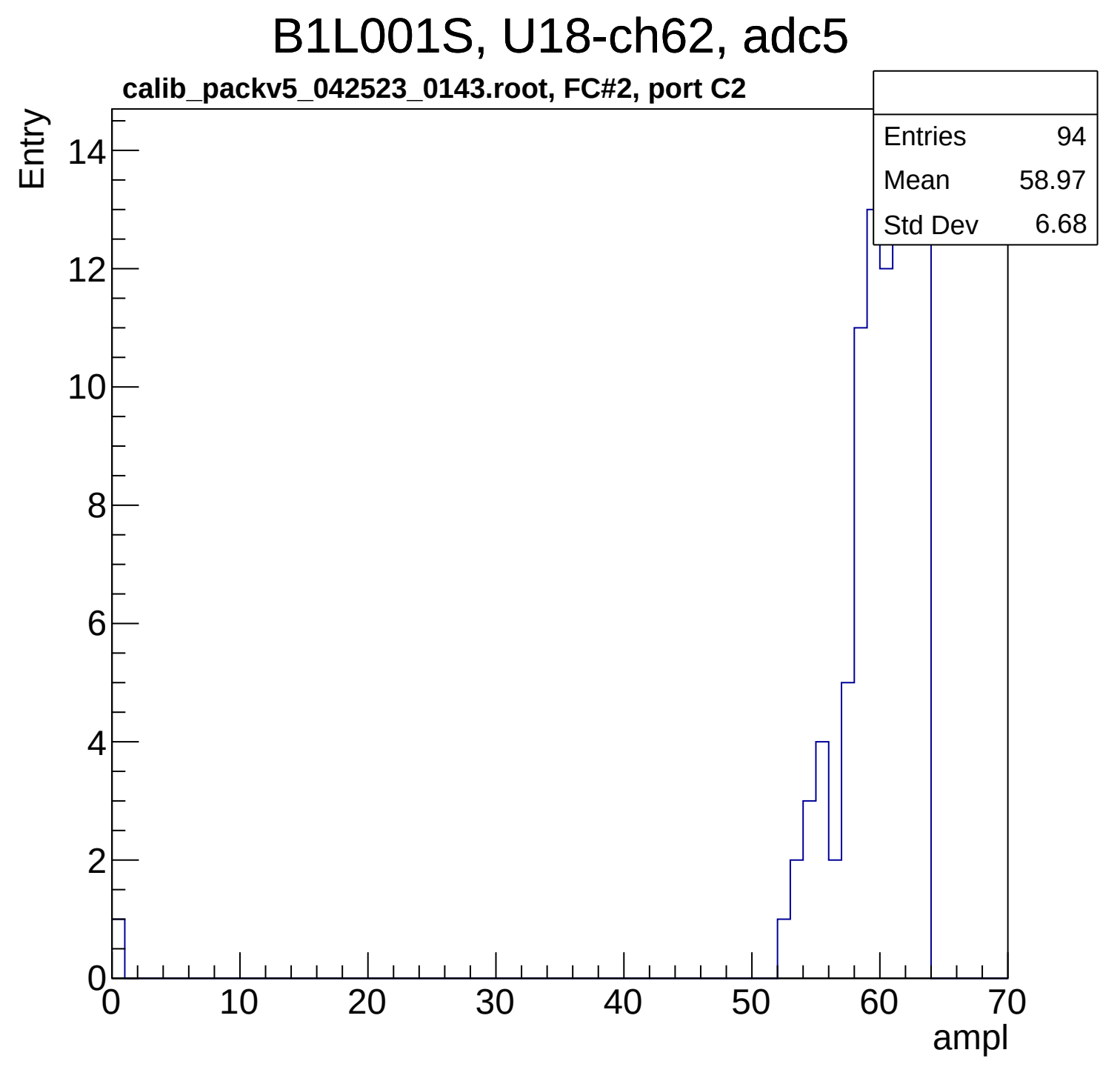

B1L001S, U18-ch62, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 143
Mean 29.41
Std Dev 3.988
Gaus mean : 30.0813
Gaus Width: 3.3693
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

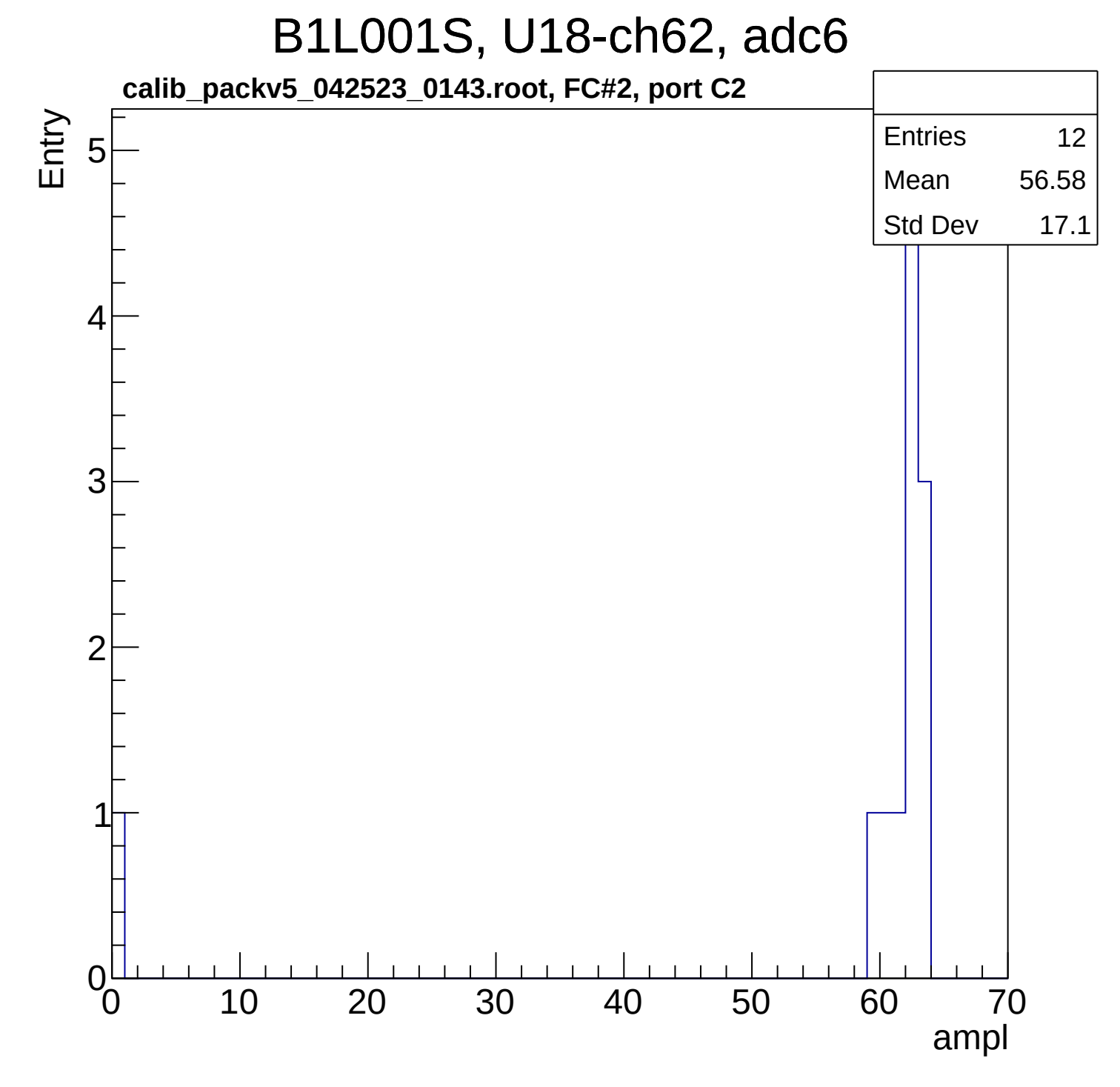

B1L001S, U18-ch62, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 112
Mean 36.01
Std Dev 3.264
Gaus mean : 36.4597
Gaus Width: 2.9774
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

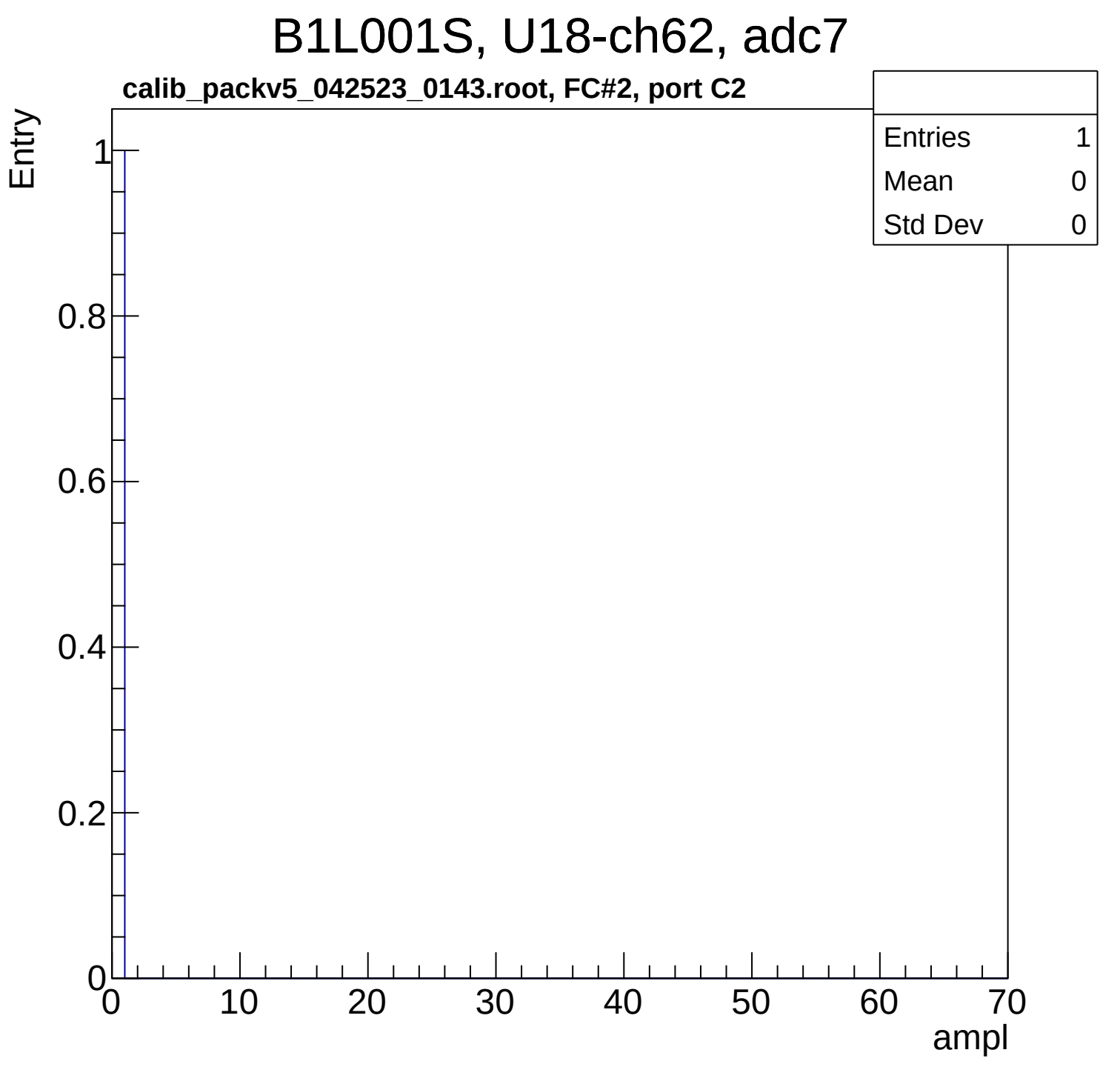

B1L001S, U18-ch62, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 141
Mean 42.16
Std Dev 3.421
Gaus mean : 42.6334
Gaus Width: 3.5751
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

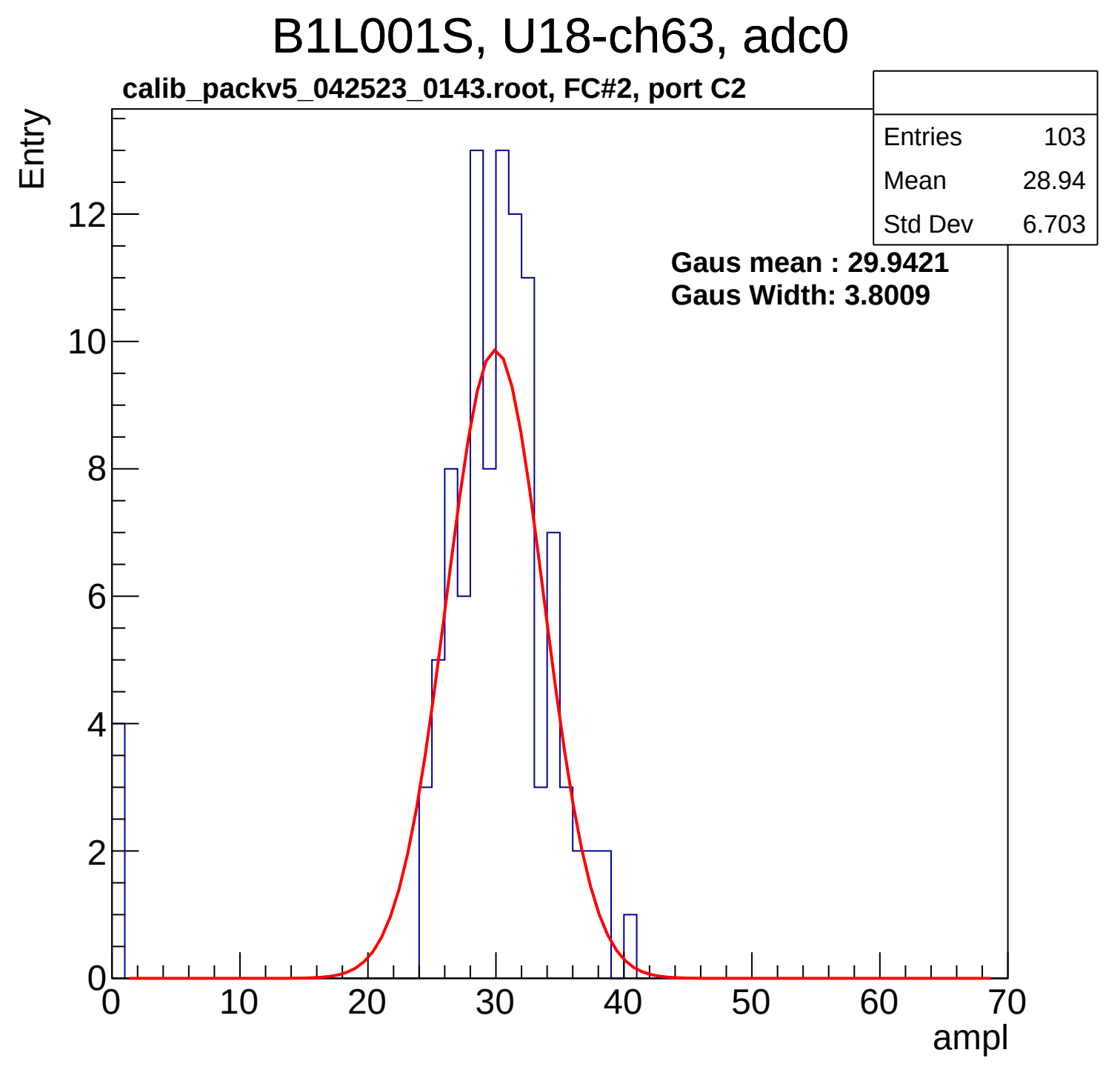

B1L001S, U18-ch62, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 126
Mean 48.72
Std Dev 3.491
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

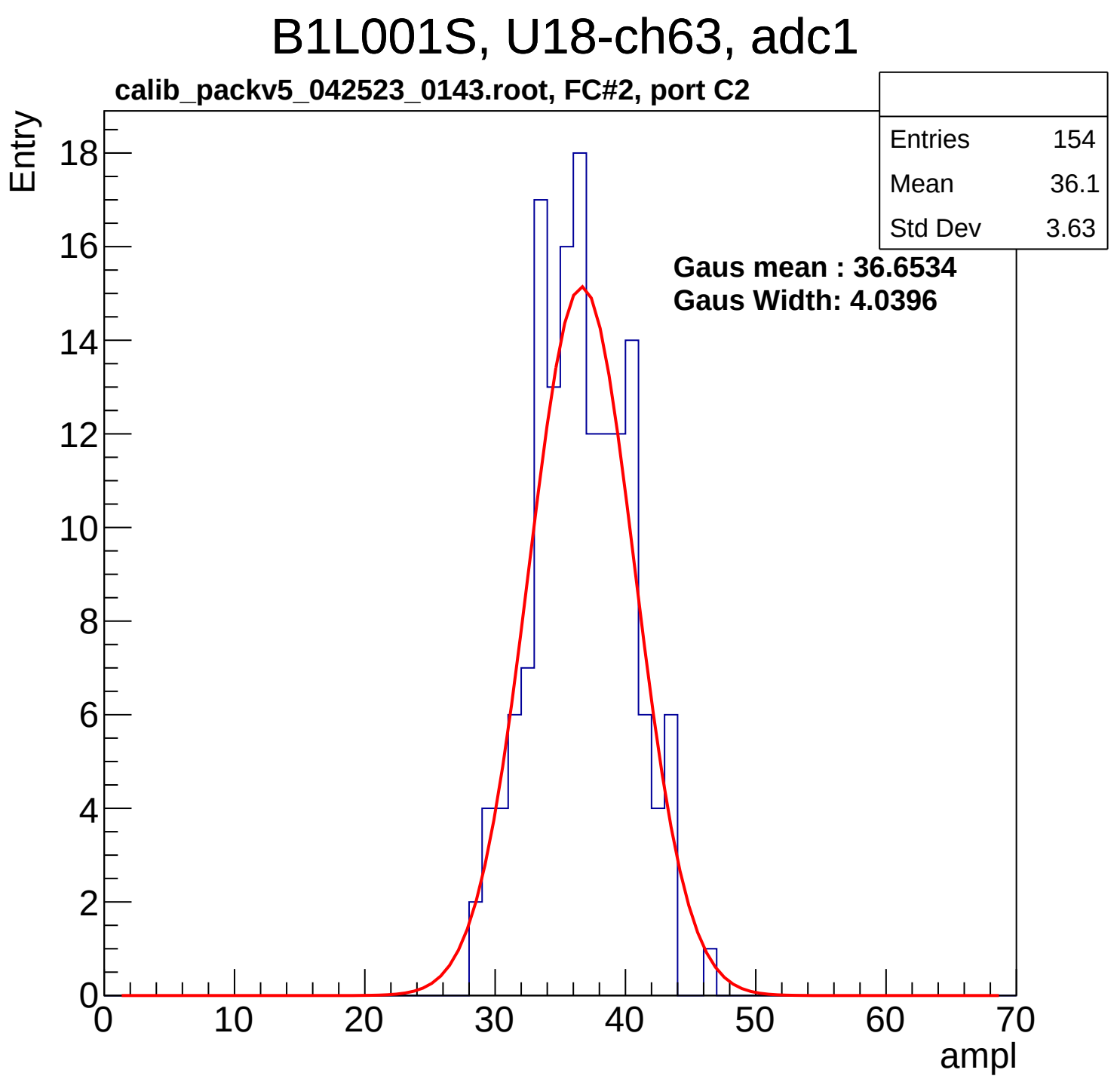

B1L001S, U18-ch62, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 126
Mean 55.5
Std Dev 3.311
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

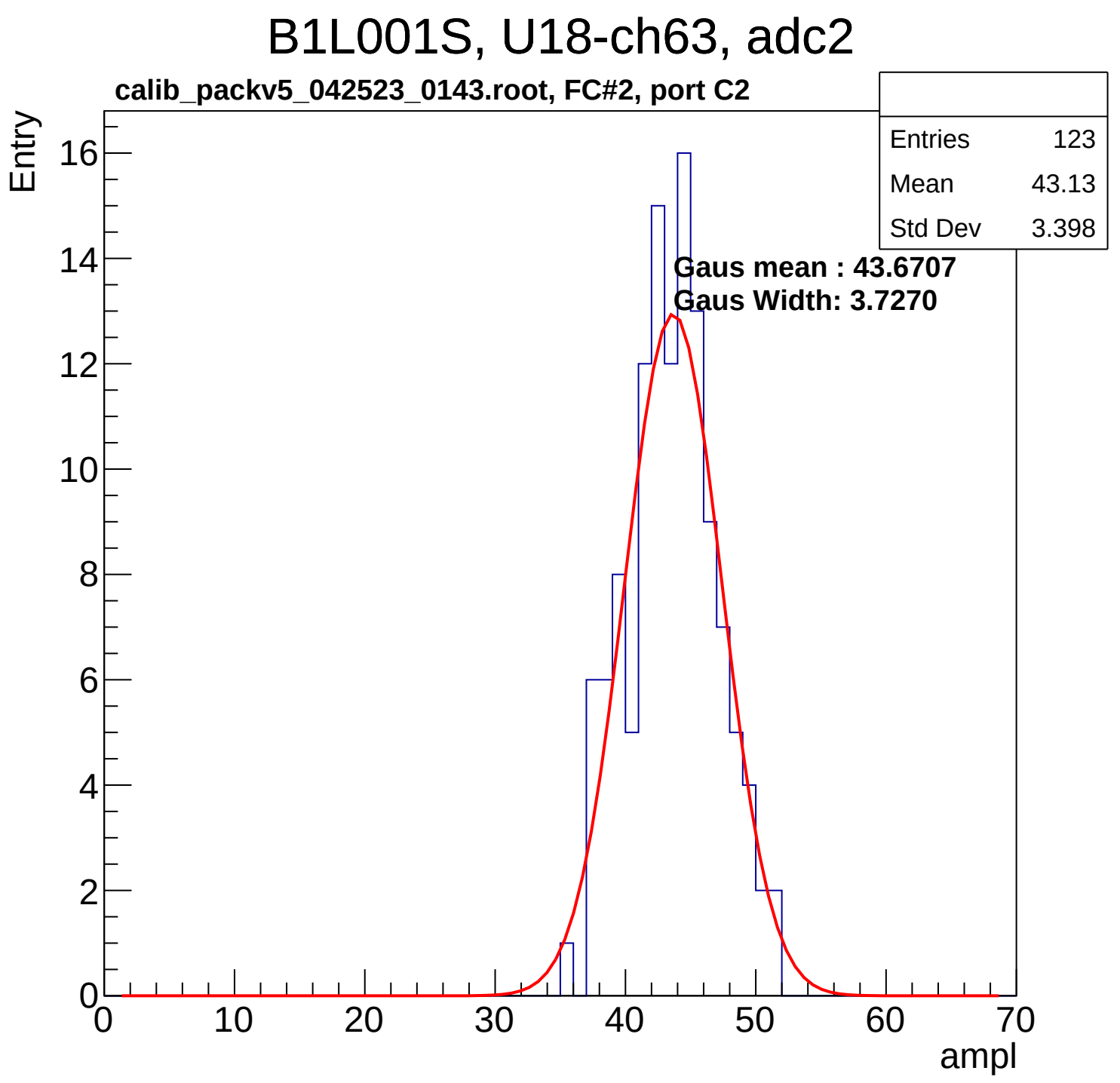

B1L001S, U18-ch62, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 94
Mean 58.97
Std Dev 6.68
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

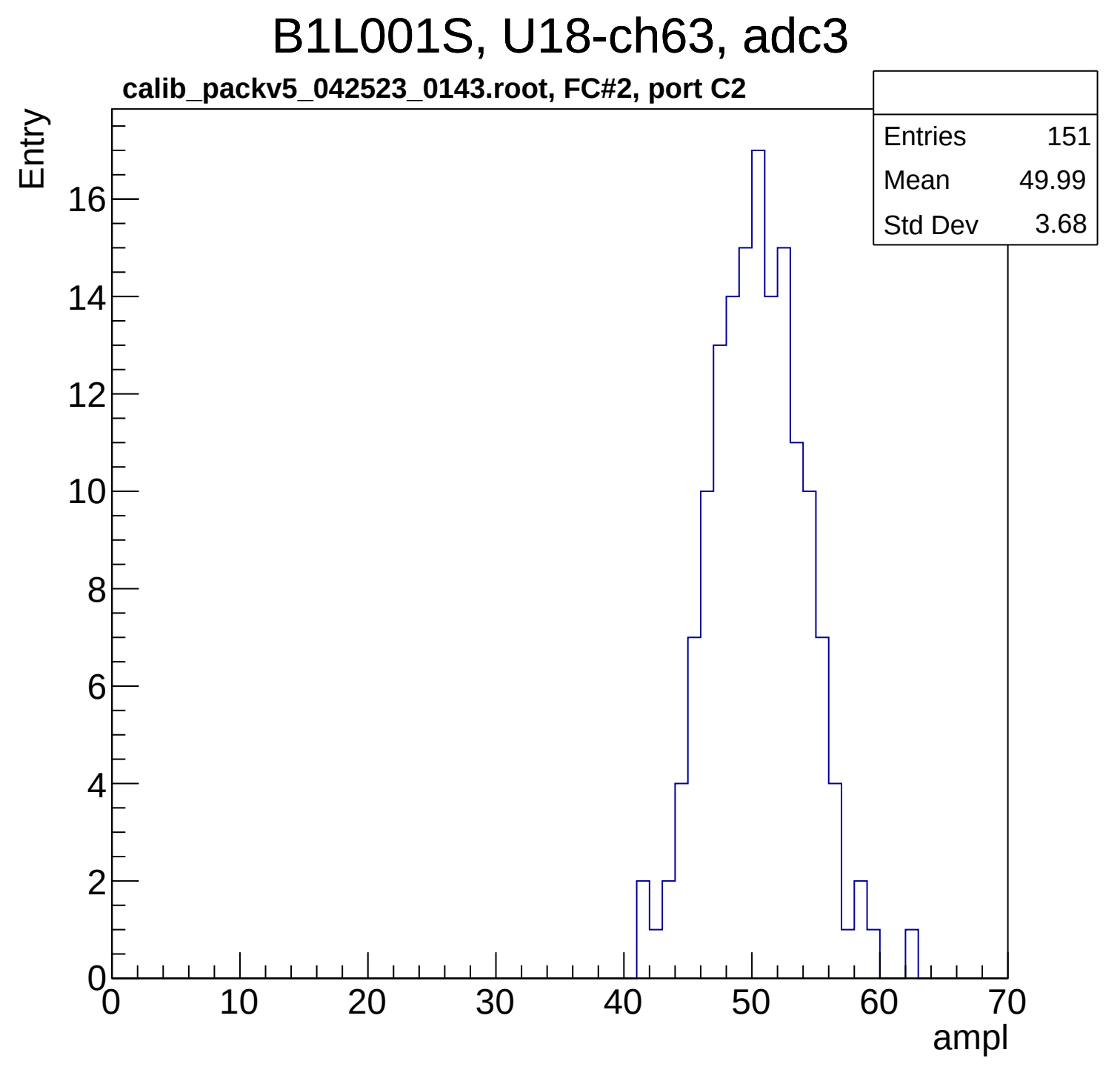

B1L001S, U18-ch62, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 12
Mean 56.58
Std Dev 17.1
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

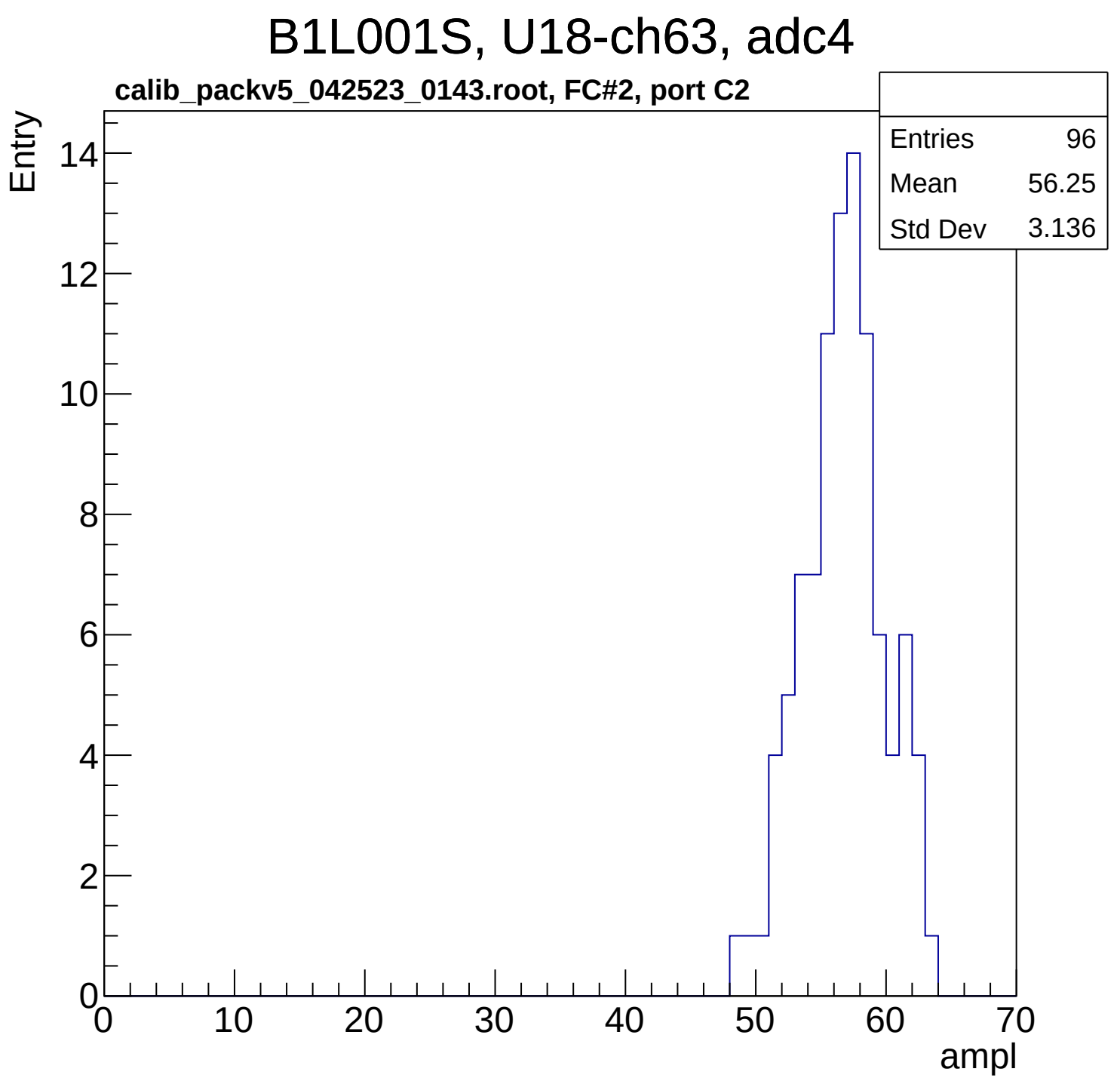

B1L001S, U18-ch62, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

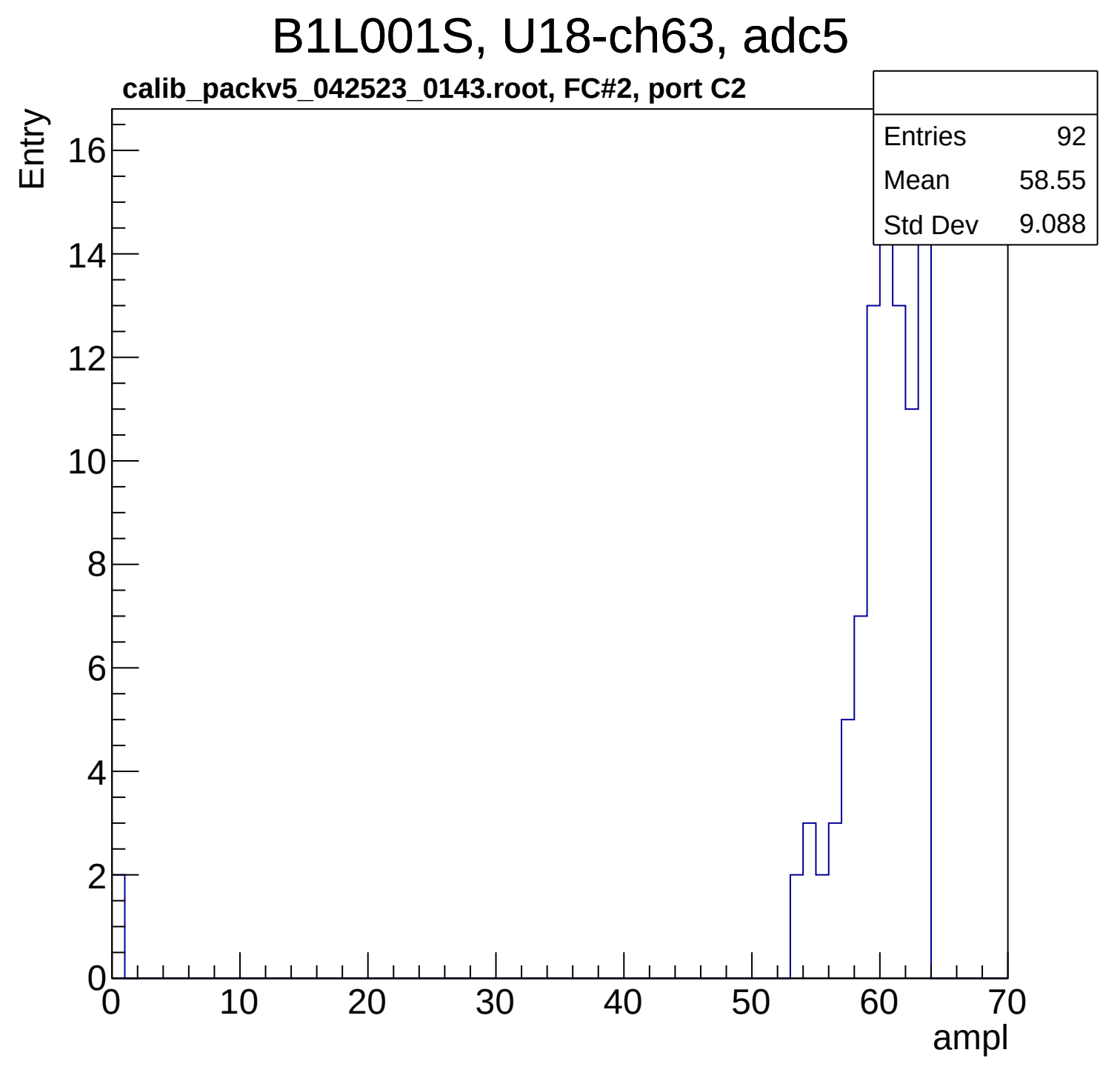

B1L001S, U18-ch63, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 103
Mean 28.94
Std Dev 6.703
Gaus mean : 29.9421
Gaus Width: 3.8009
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70

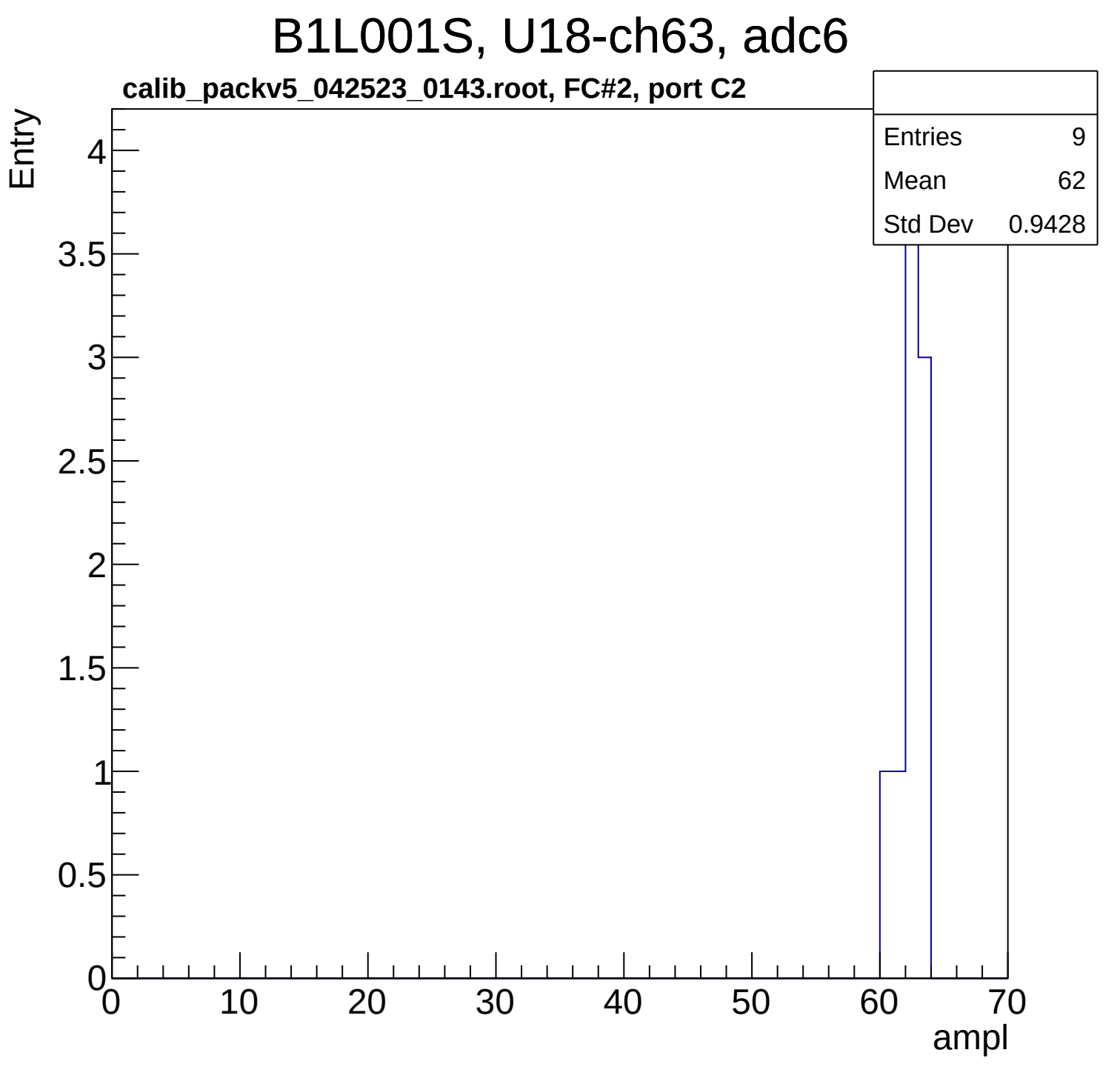

B1L001S, U18-ch63, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 154
Mean 36.1
Std Dev 3.63
Gaus mean : 36.6534
Gaus Width: 4.0396
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

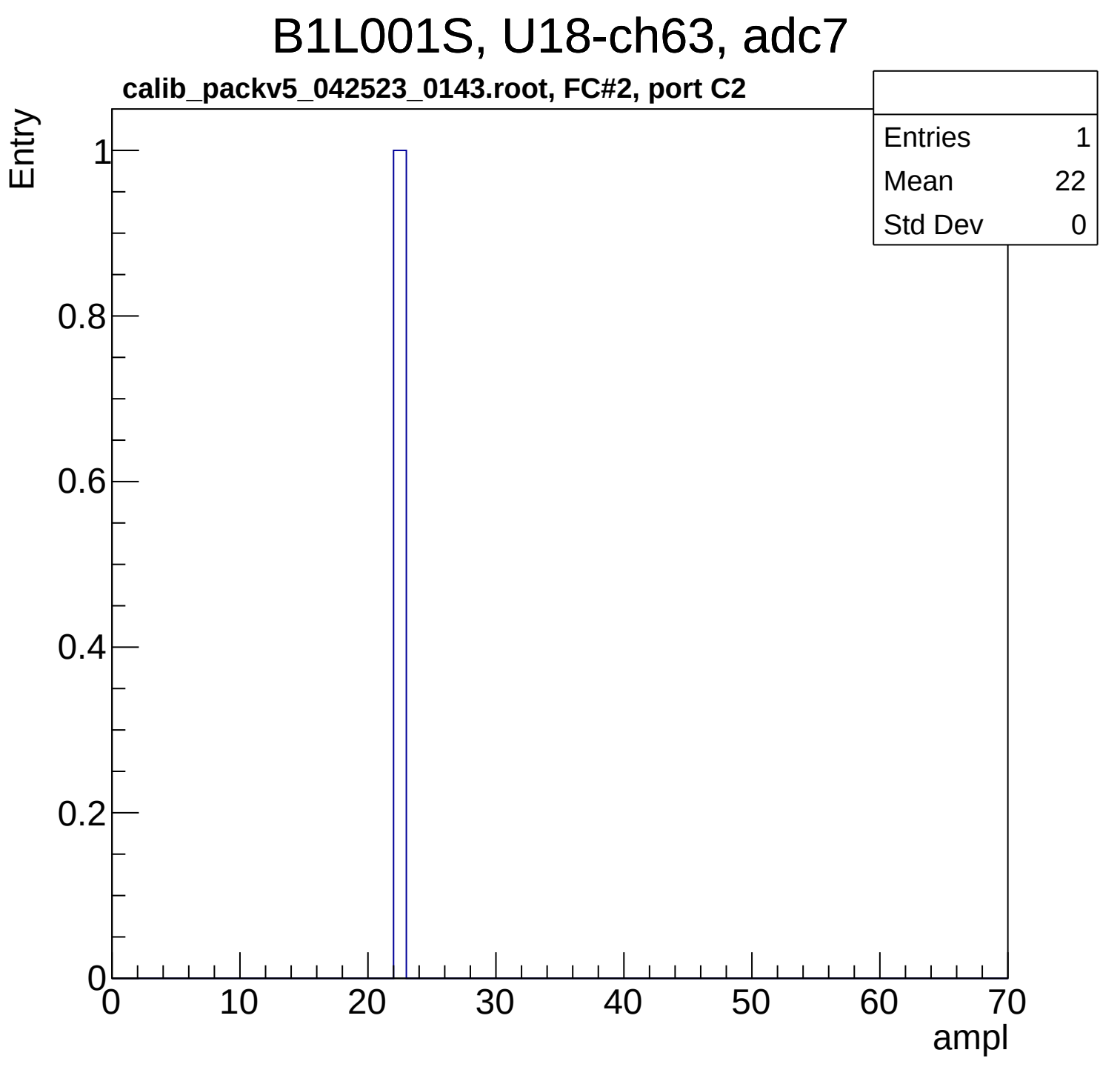

B1L001S, U18-ch63, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 123
Mean 43.13
Std Dev 3.398
Gaus mean : 43.6707
Gaus Width: 3.7270
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

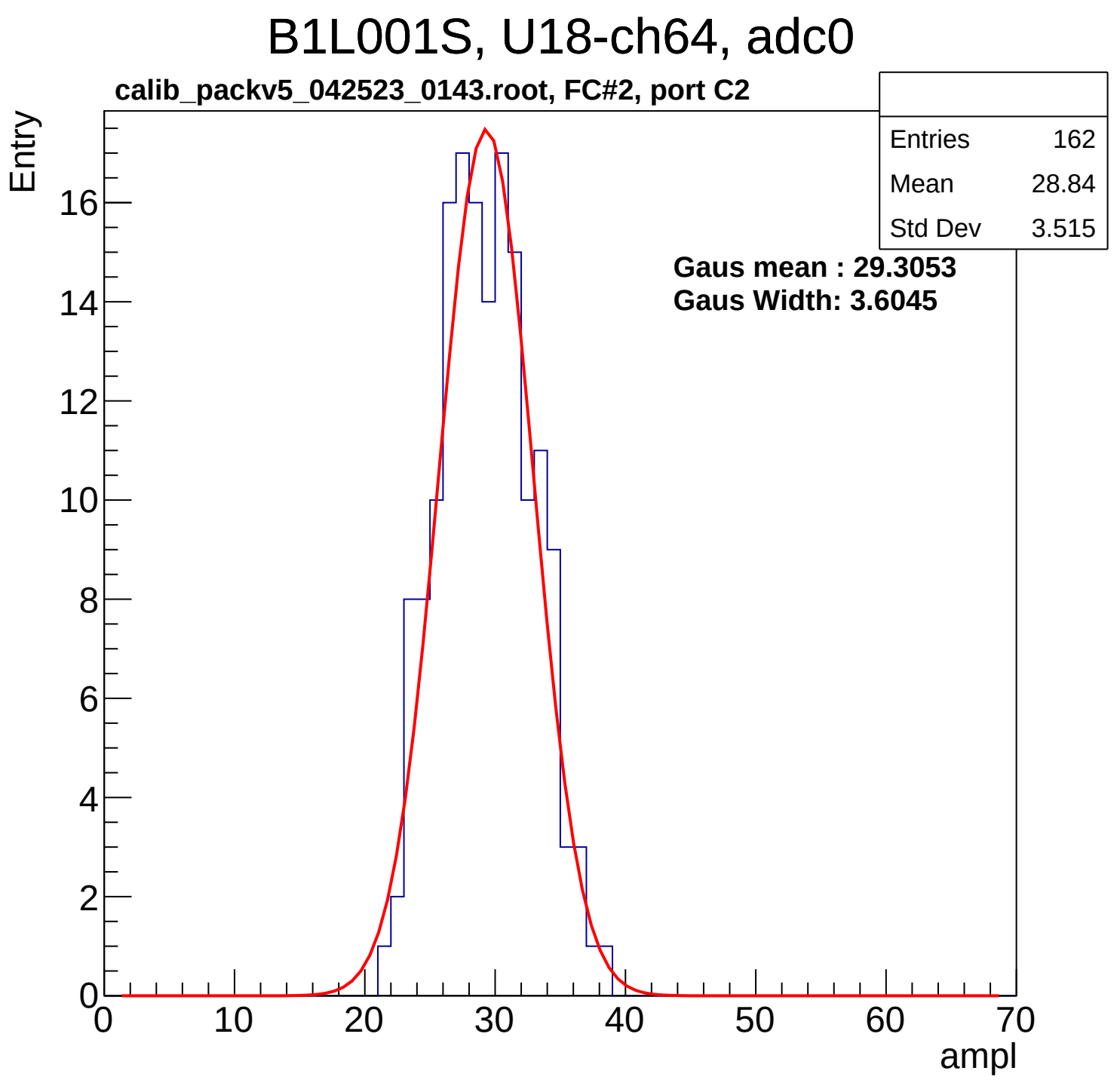

B1L001S, U18-ch63, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 151
Mean 49.99
Std Dev 3.68
Entry
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl

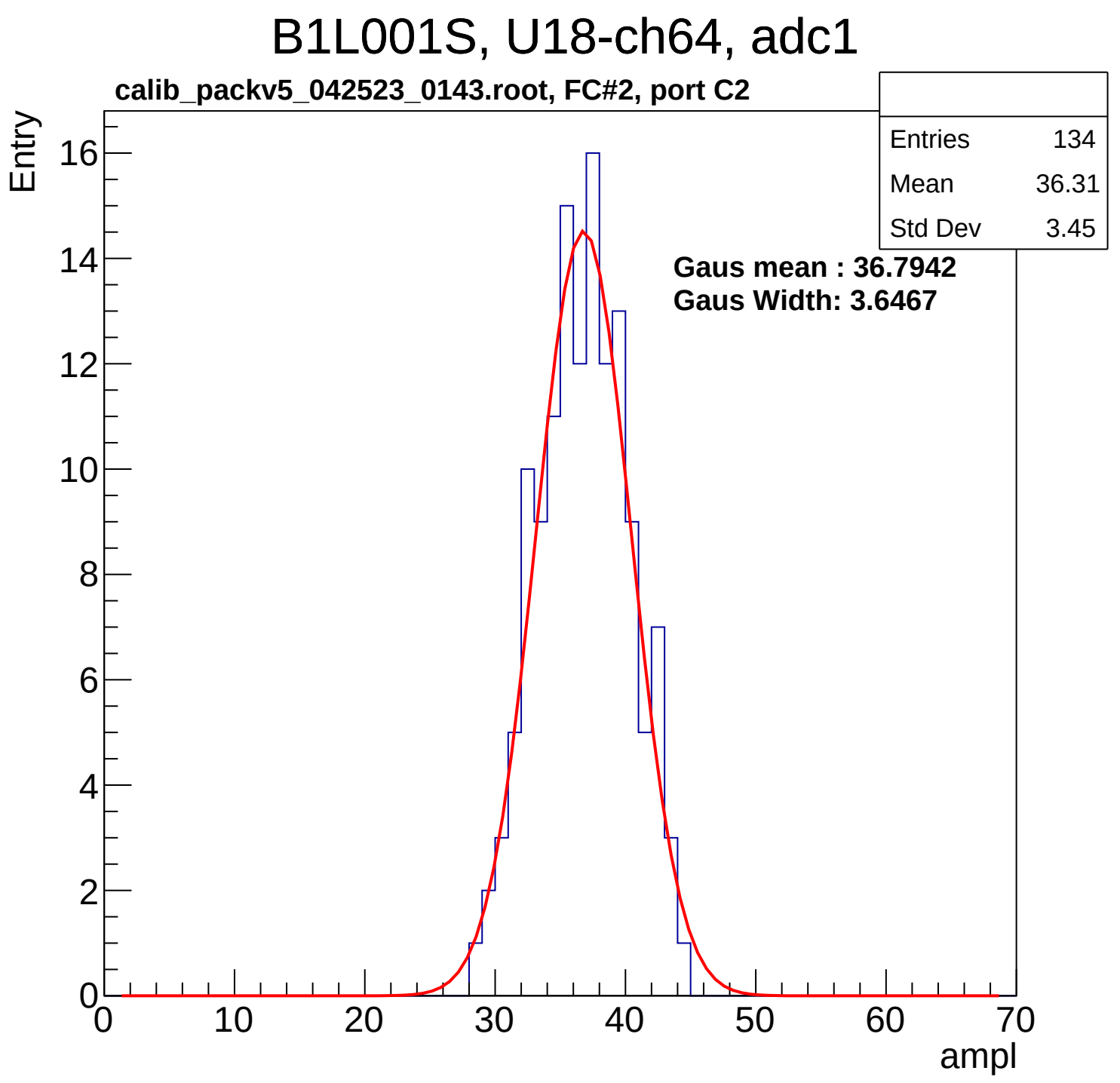

B1L001S, U18-ch63, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 96
Mean 56.25
Std Dev 3.136
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

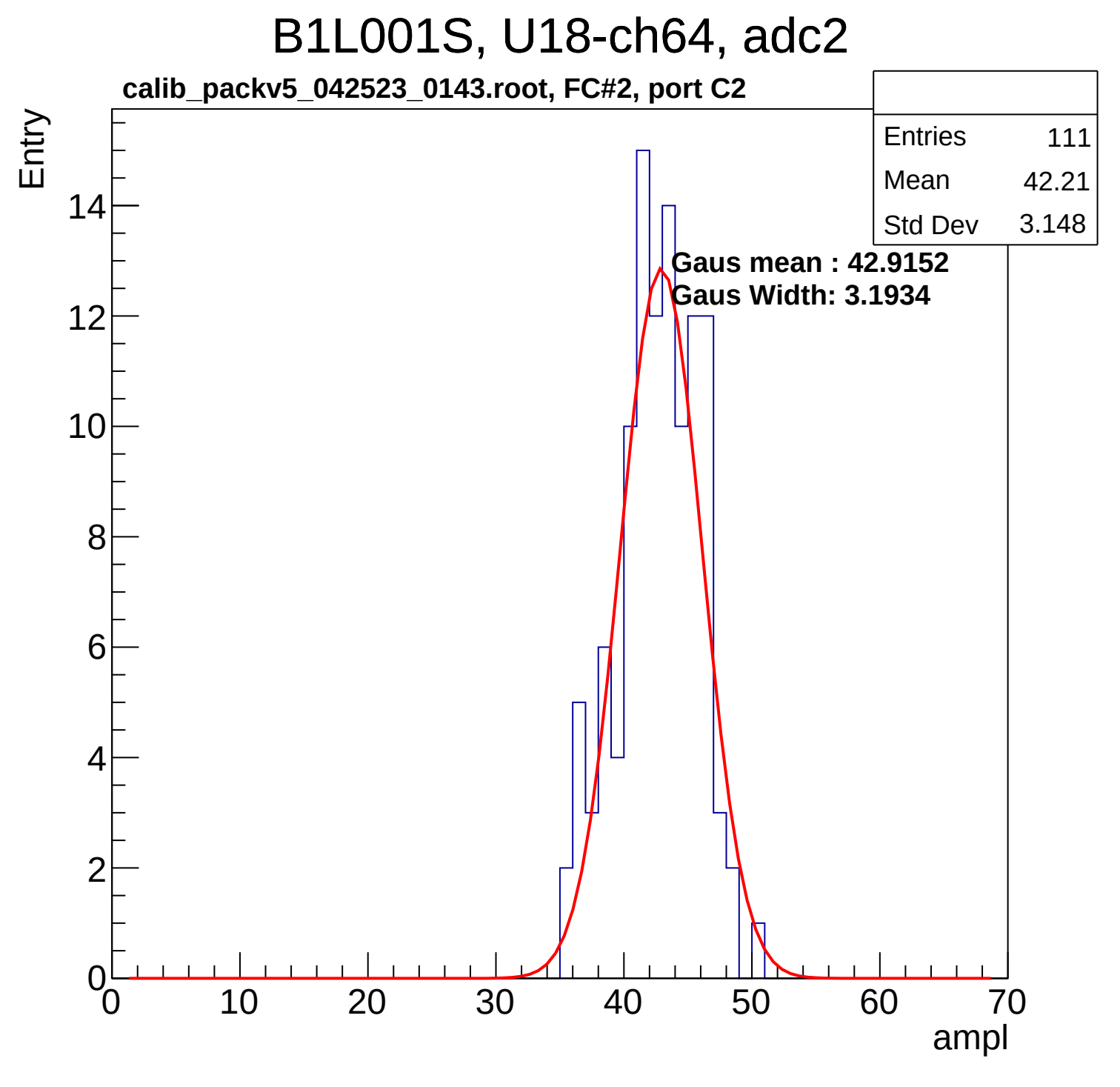

B1L001S, U18-ch63, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 92
Mean 58.55
Std Dev 9.088
Entry
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl

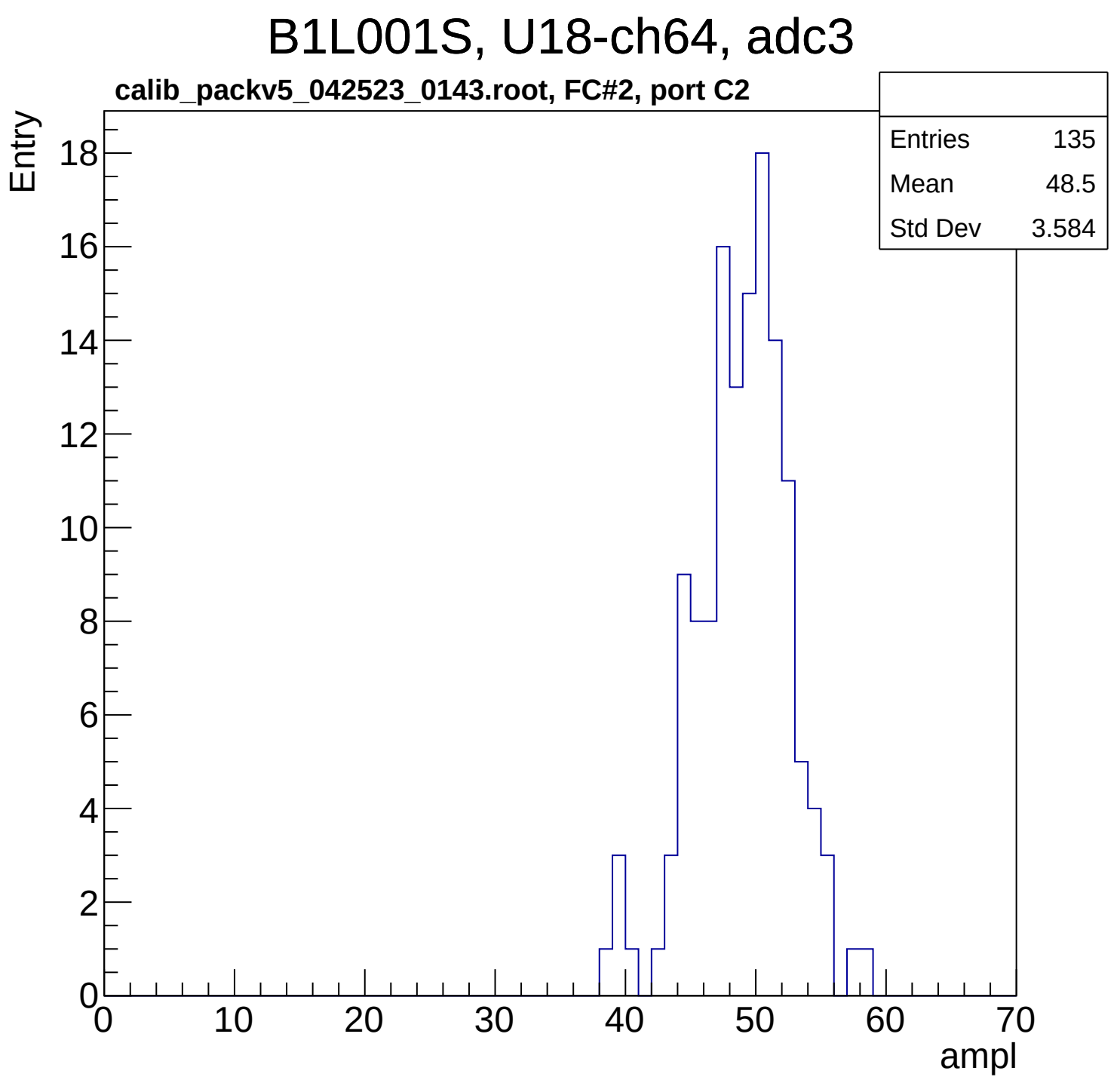

B1L001S, U18-ch63, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 9
Mean 62
Std Dev 0.9428
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

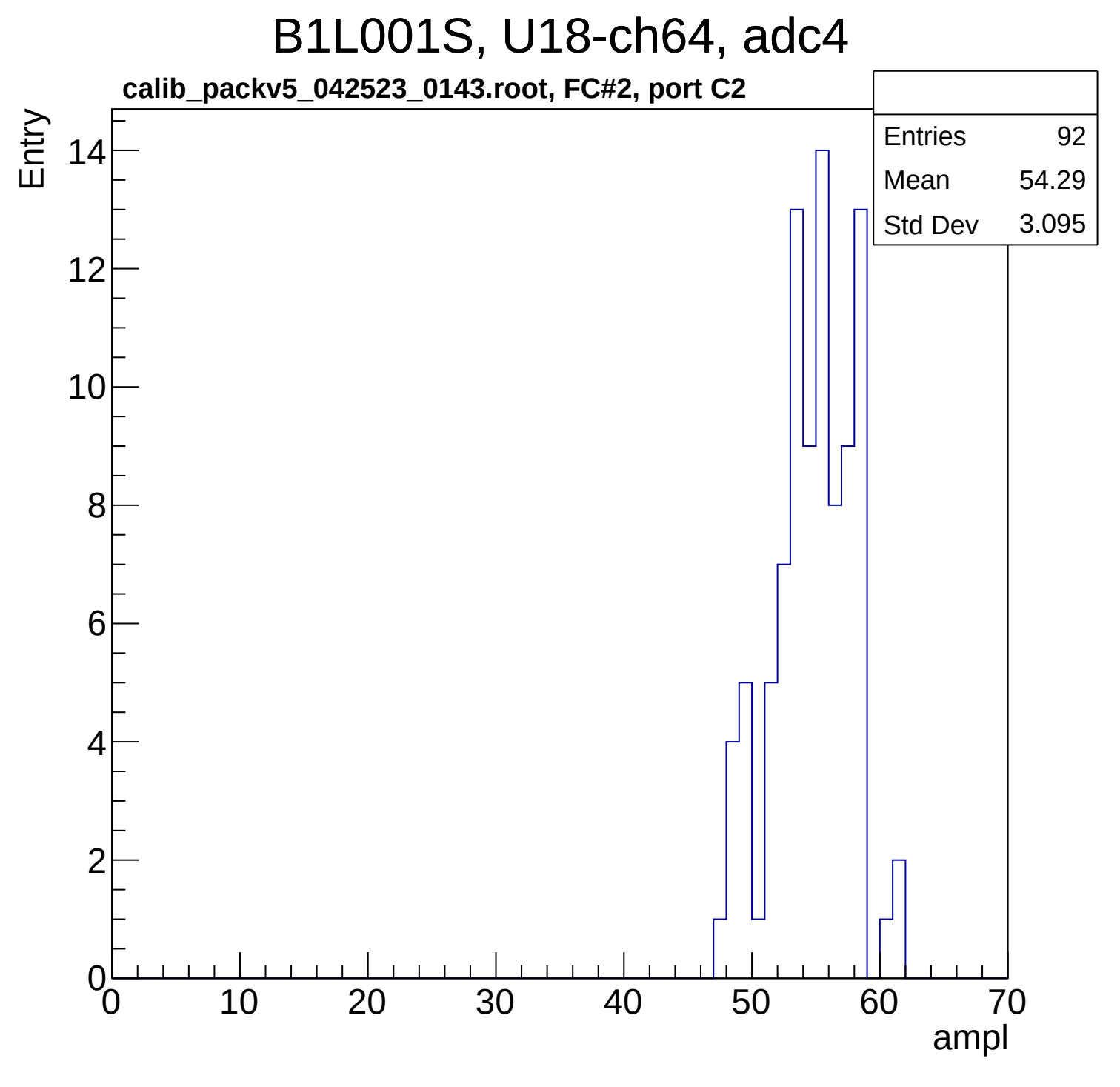

B1L001S, U18-ch63, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 22
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

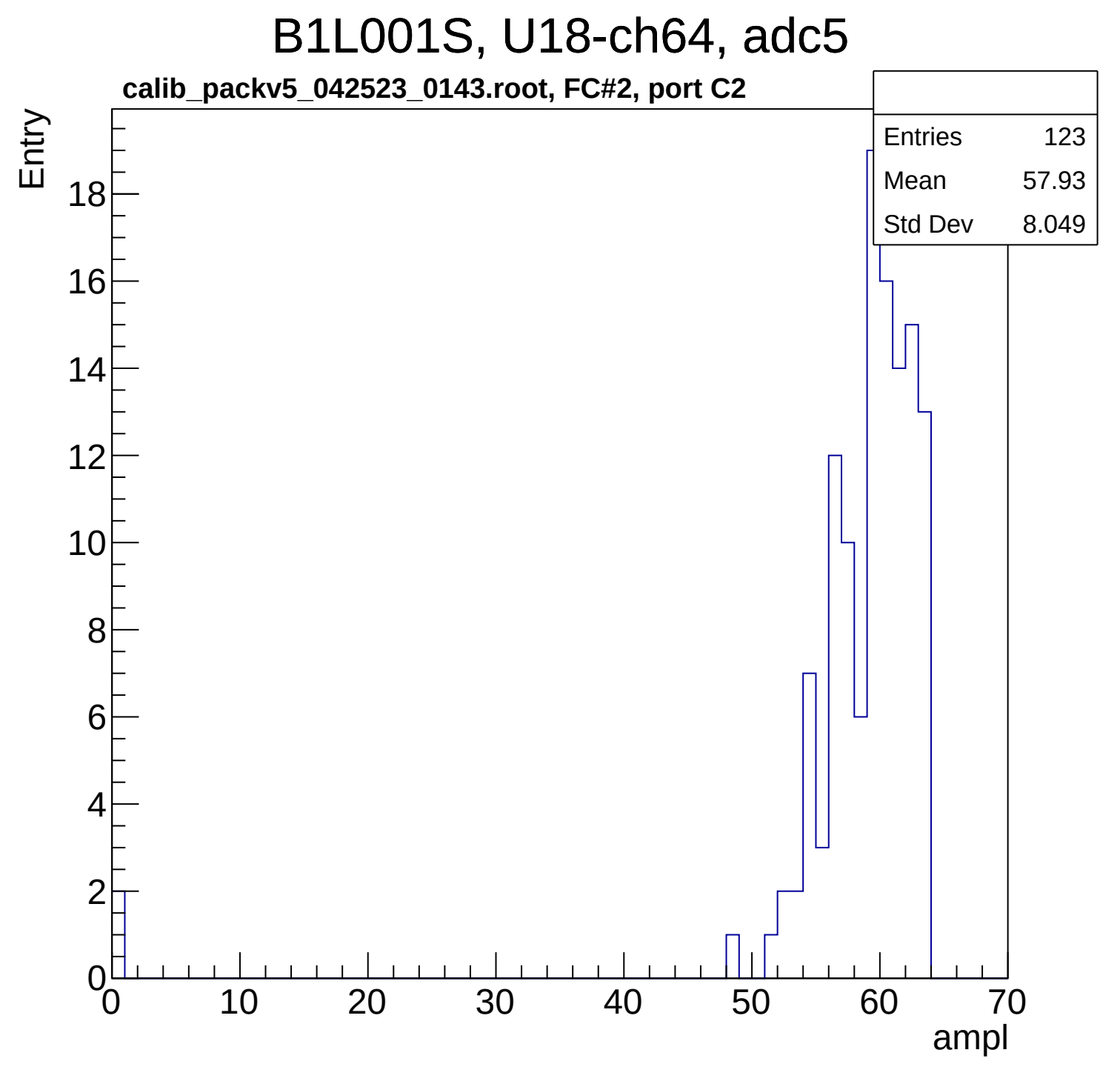

B1L001S, U18-ch64, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 162
Mean 28.84
Std Dev 3.515
Gaus mean : 29.3053
Gaus Width: 3.6045
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

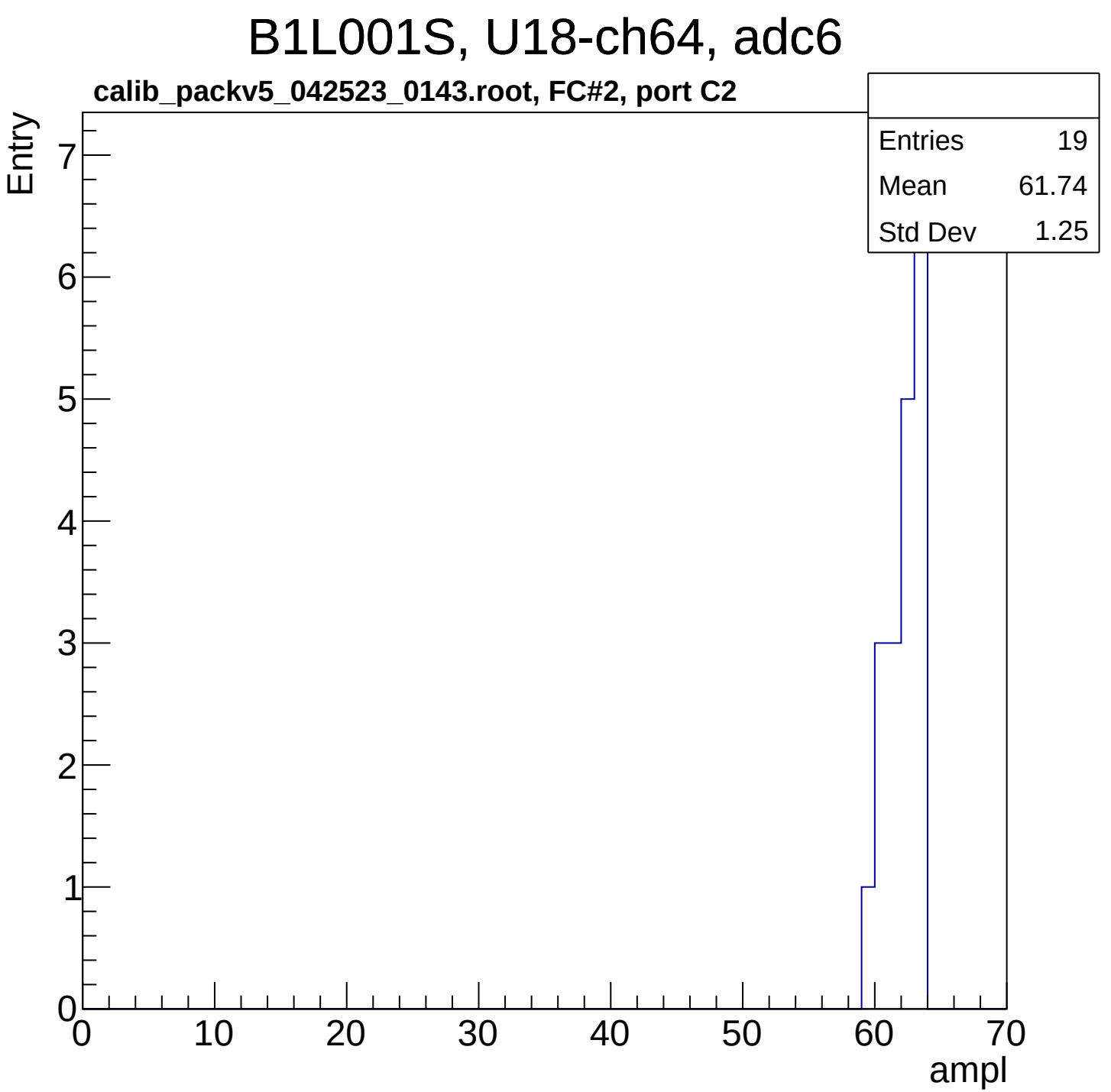

B1L001S, U18-ch64, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 134
Mean 36.31
Std Dev 3.45
Gaus mean : 36.7942
Gaus Width: 3.6467
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

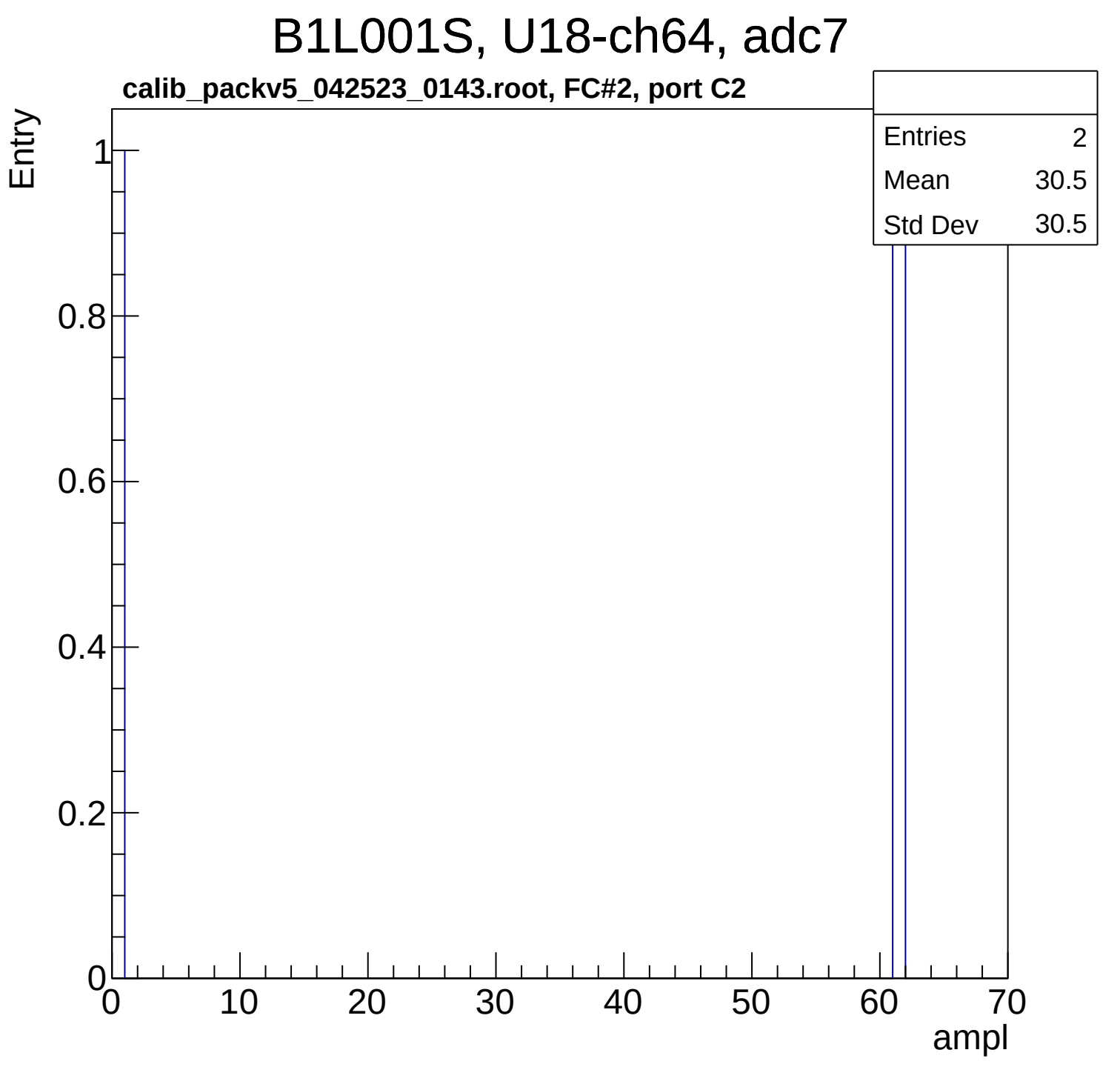

B1L001S, U18-ch64, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 111
Mean 42.21
Std Dev 3.148
Gaus mean : 42.9152
Gaus Width: 3.1934
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

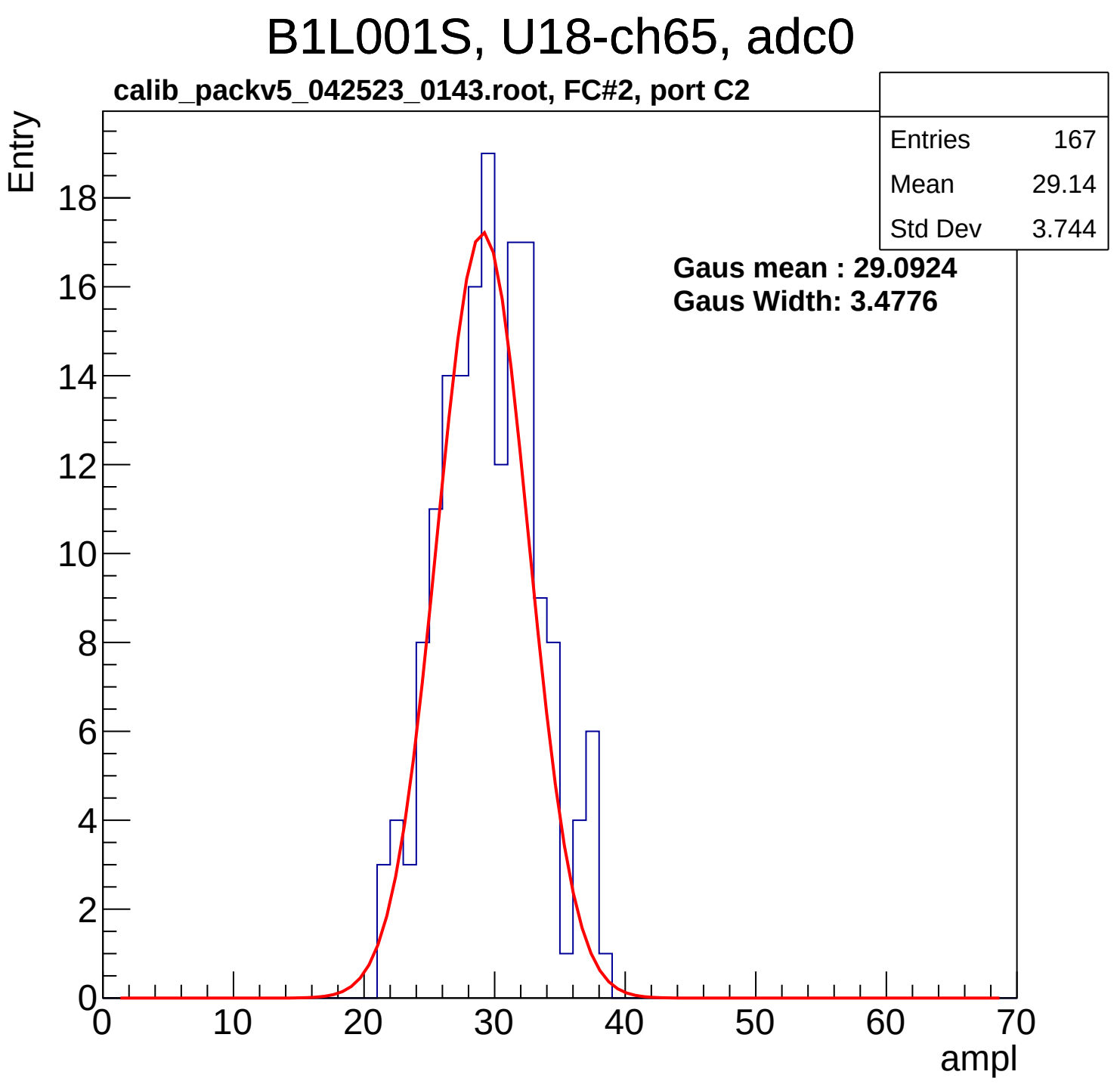

B1L001S, U18-ch64, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 135
Mean 48.5
Std Dev 3.584
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

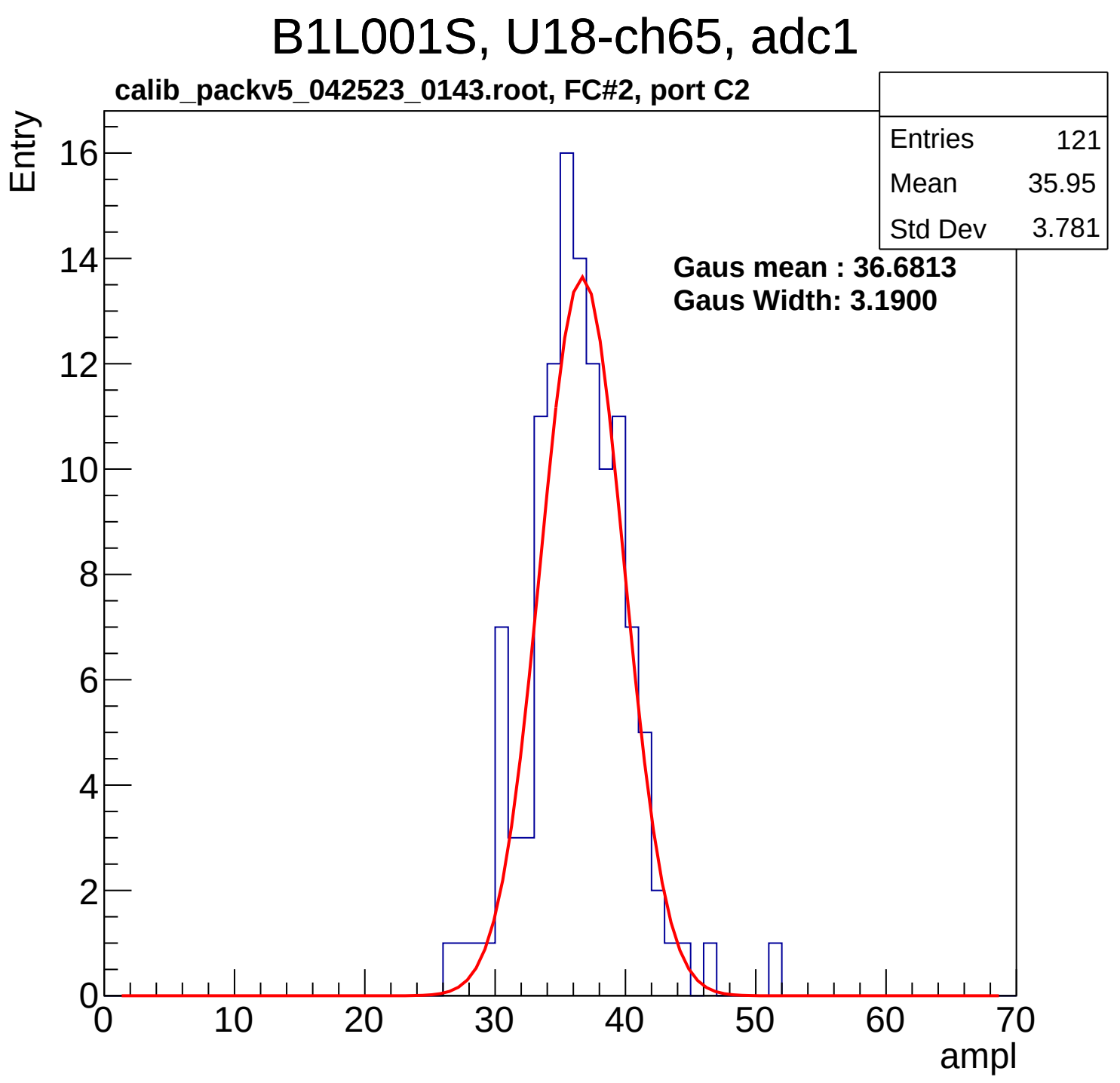

B1L001S, U18-ch64, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 92
Mean 54.29
Std Dev 3.095
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

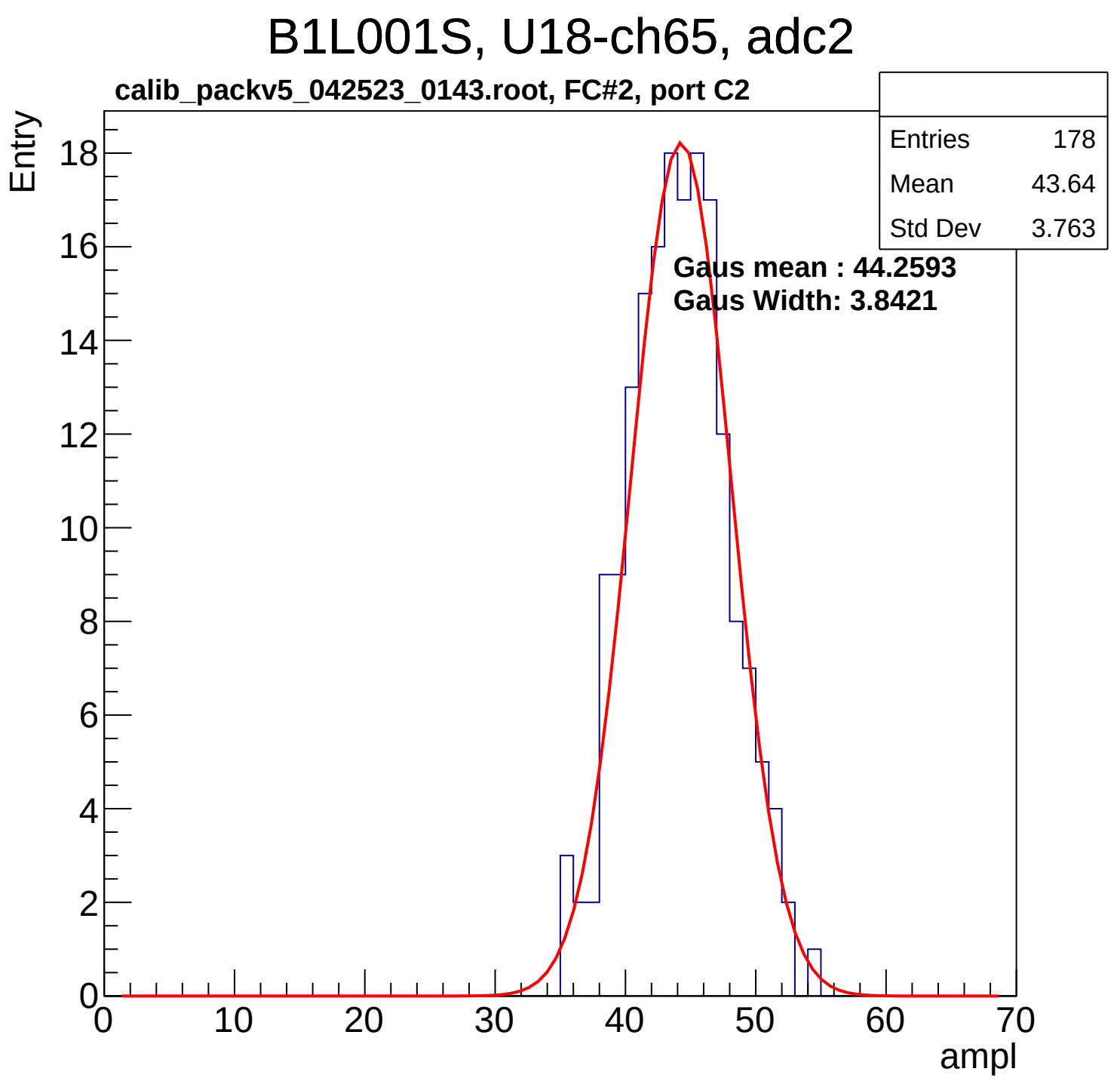

B1L001S, U18-ch64, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 123
Mean 57.93
Std Dev 8.049
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

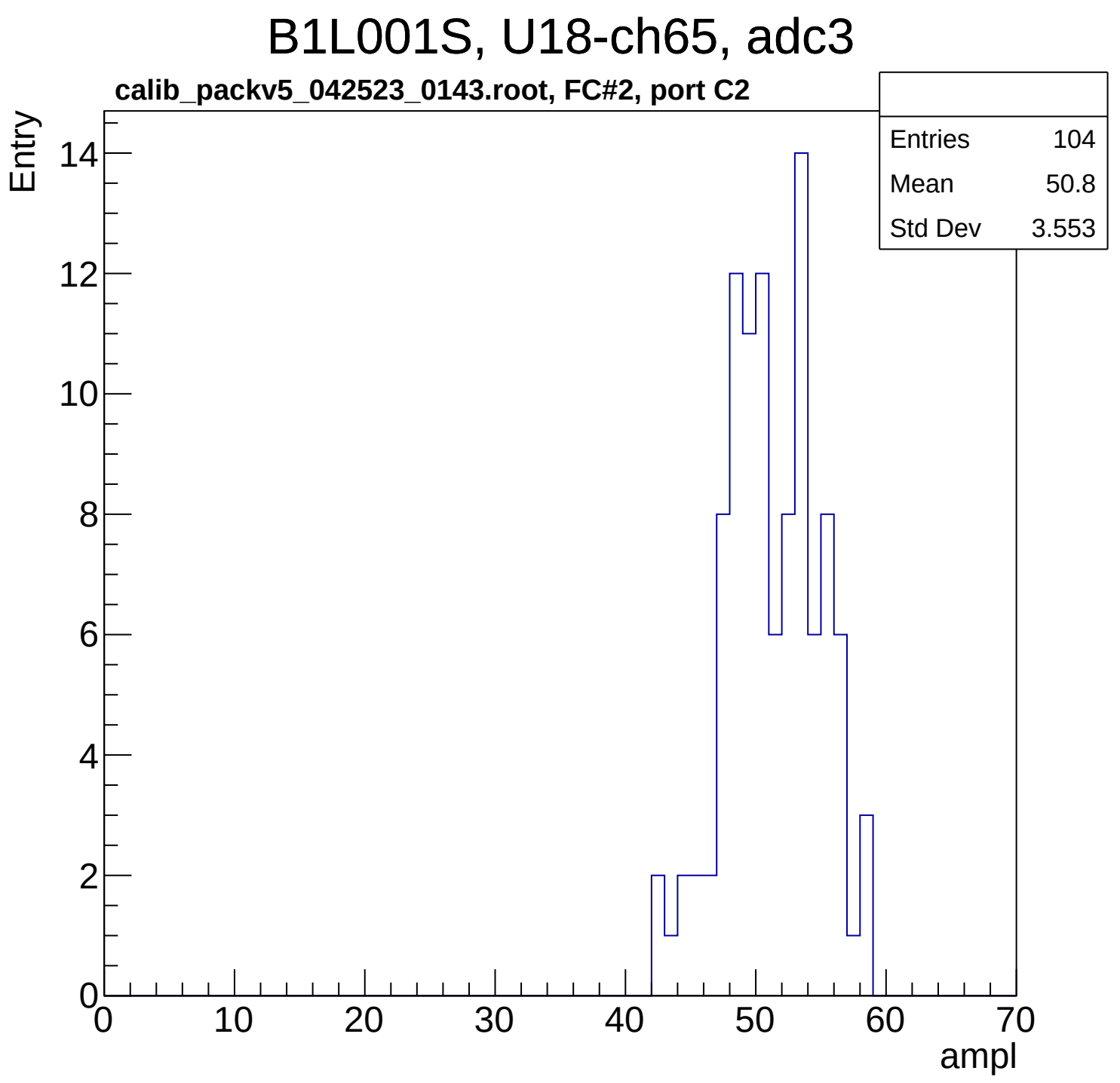

B1L001S, U18-ch64, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 19
Mean 61.74
Std Dev 1.25
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

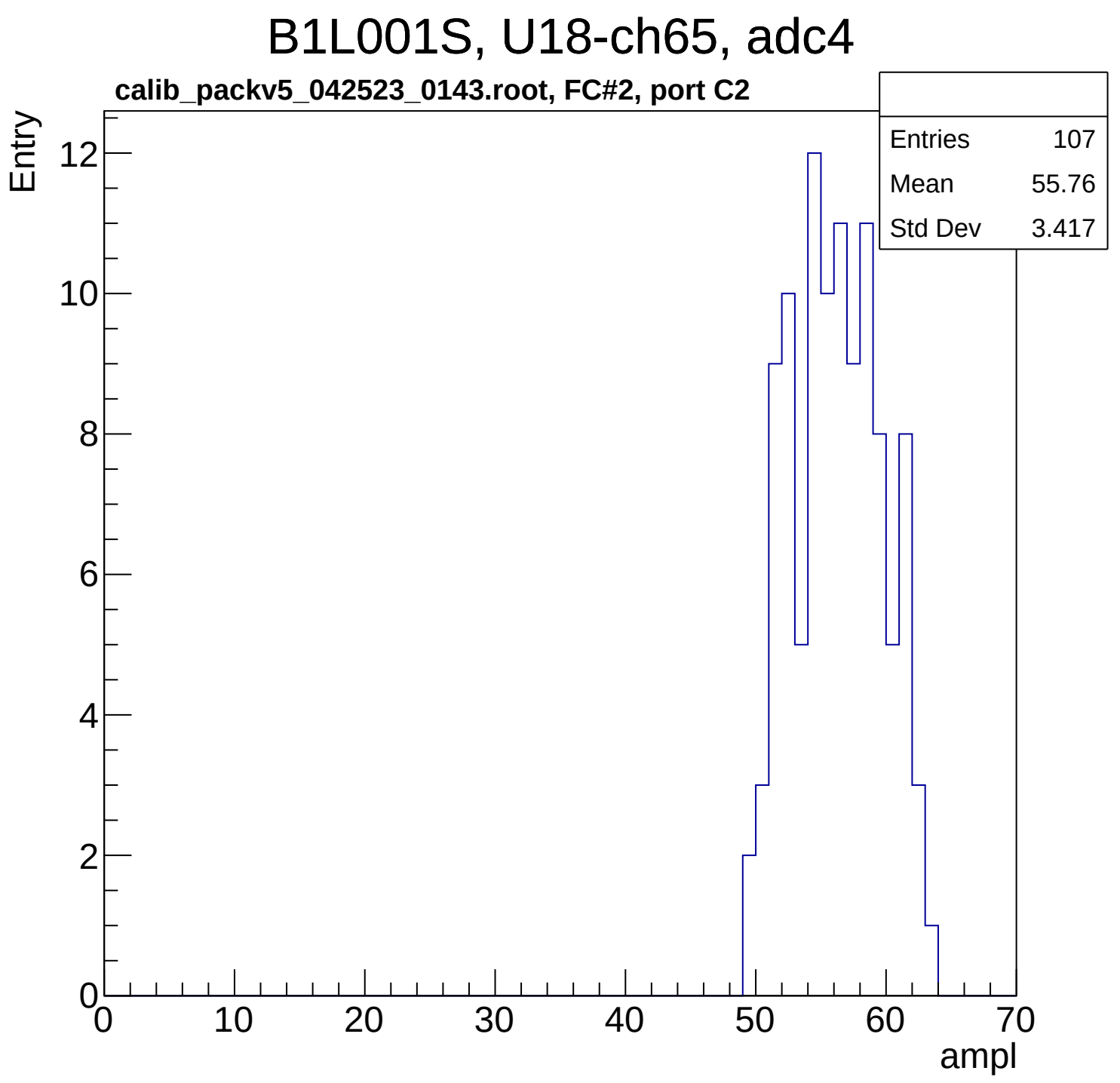

B1L001S, U18-ch64, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 30.5
Std Dev 30.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

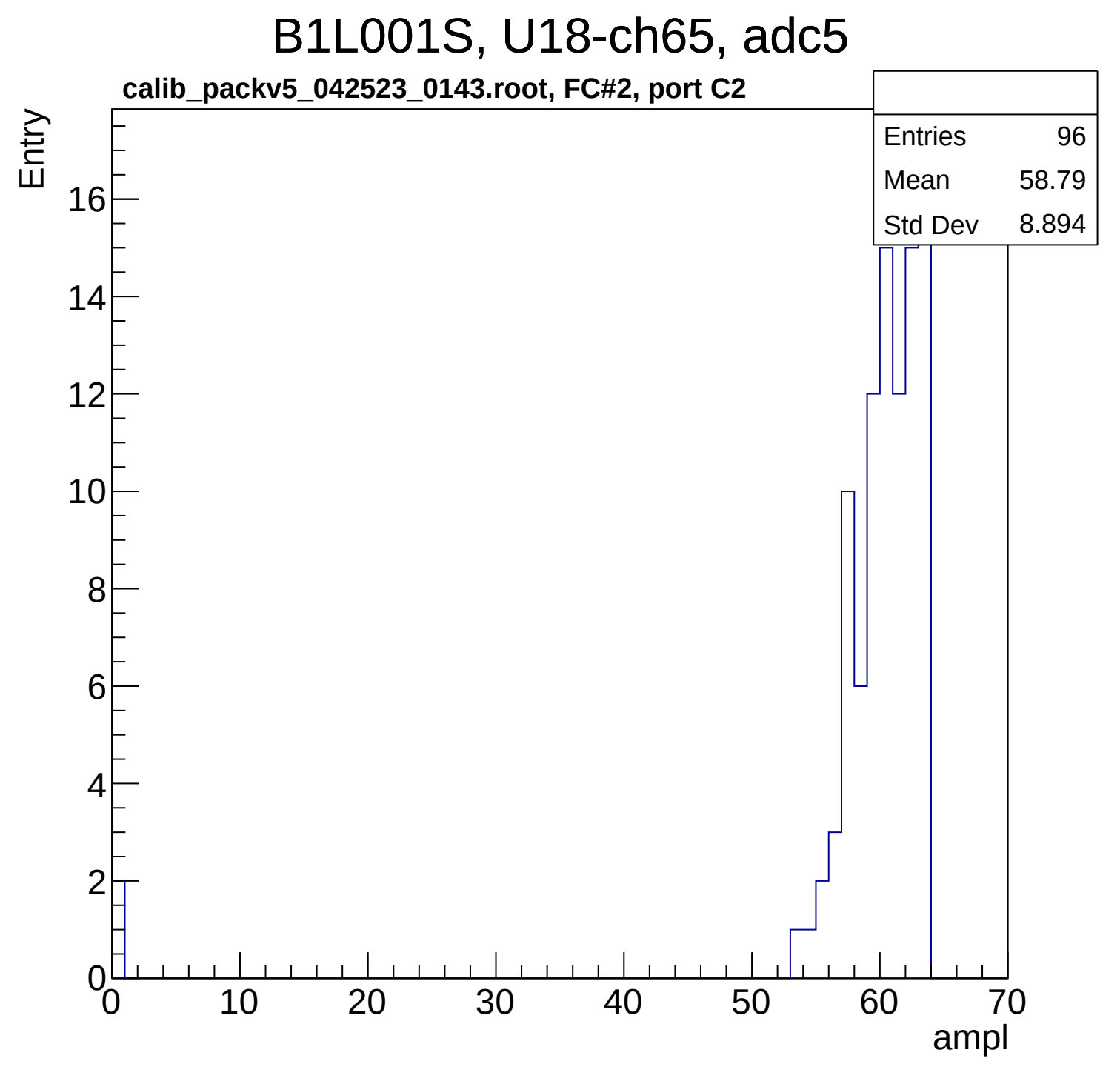

B1L001S, U18-ch65, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 167
Mean 29.14
Std Dev 3.744
Gaus mean : 29.0924
Gaus Width: 3.4776
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

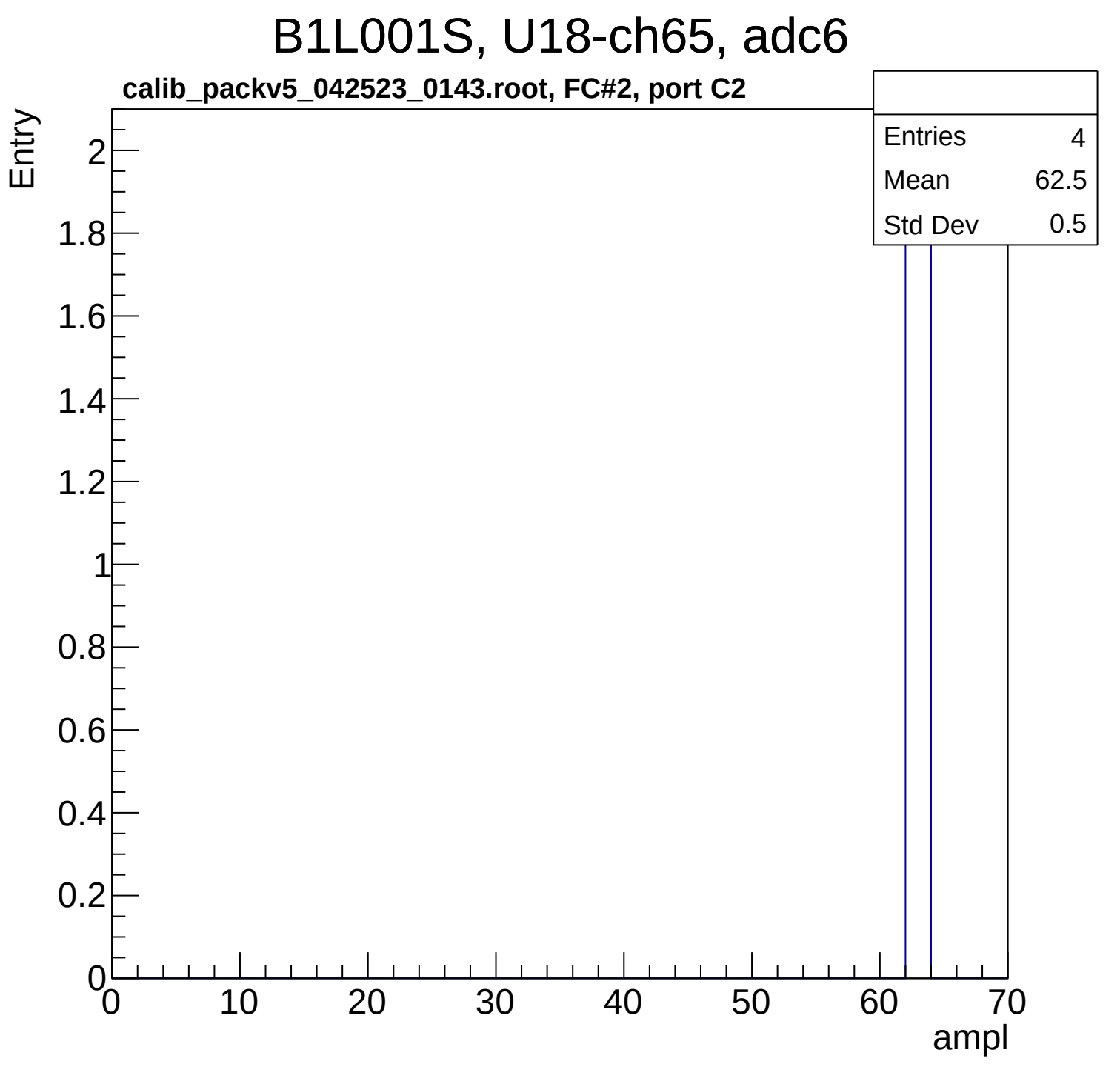

B1L001S, U18-ch65, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 121
Mean 35.95
Std Dev 3.781
Gaus mean : 36.6813
Gaus Width: 3.1900
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

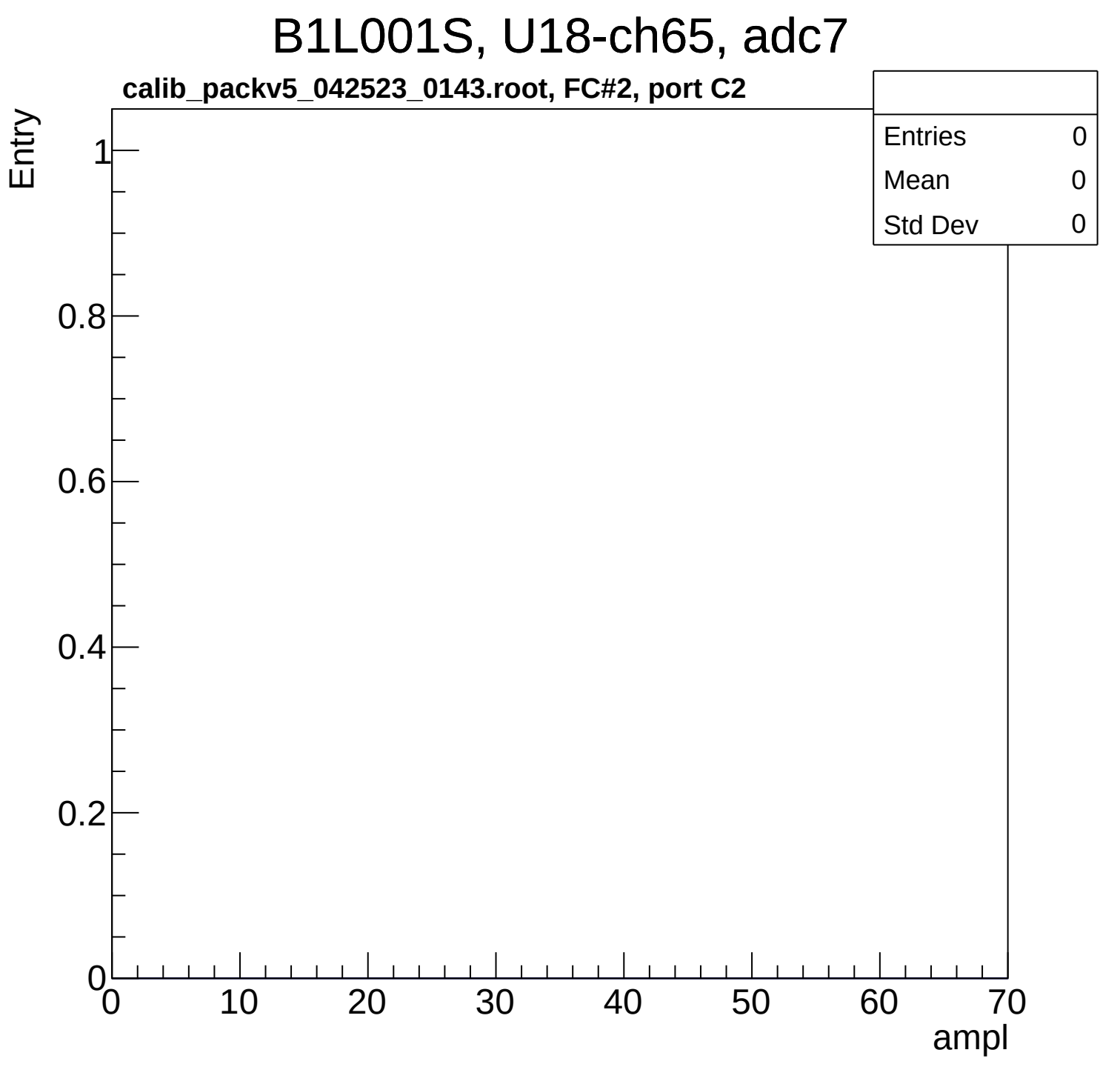

B1L001S, U18-ch65, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 178
Mean 43.64
Std Dev 3.763
Gaus mean : 44.2593
Gaus Width: 3.8421
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

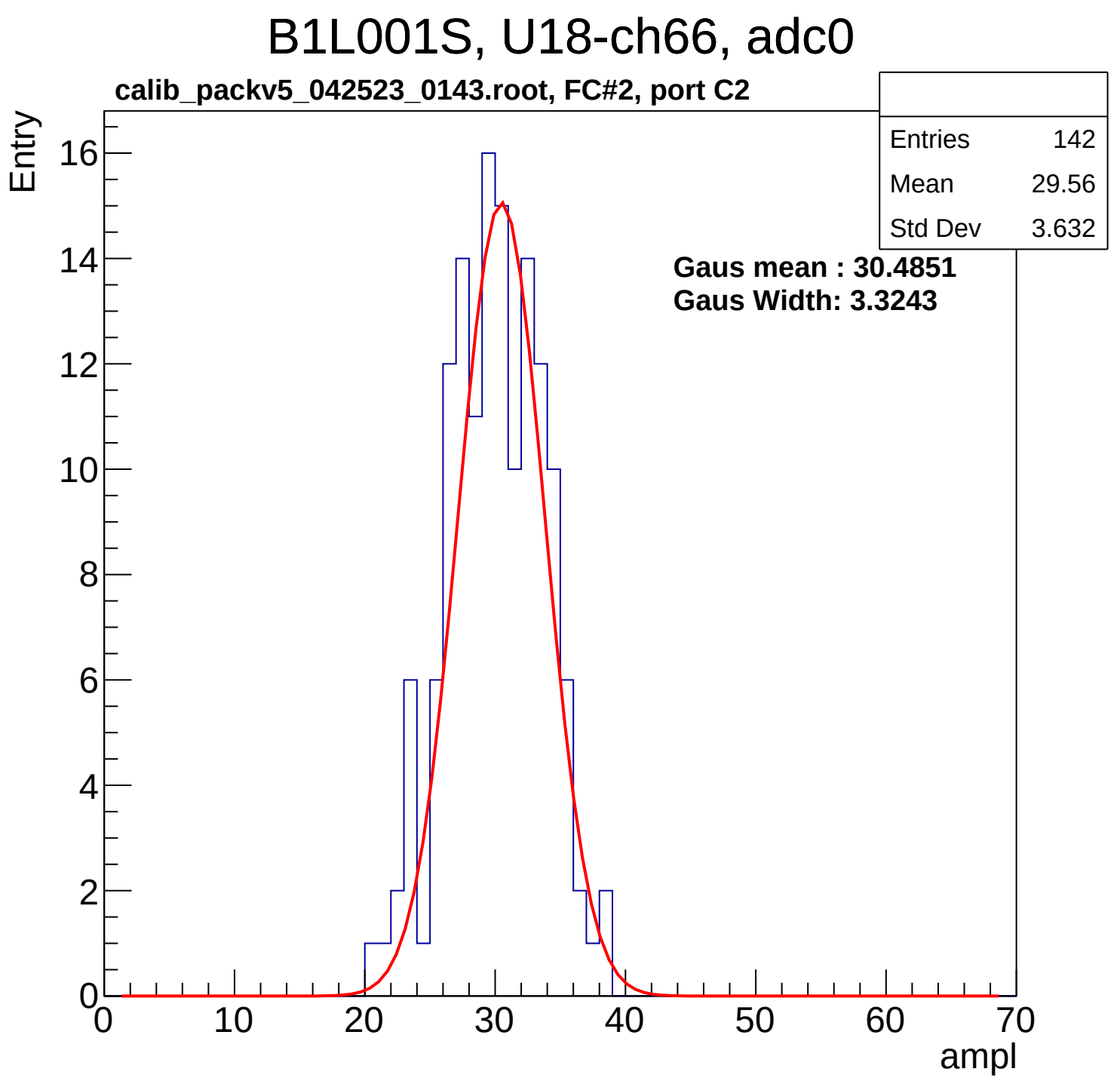

B1L001S, U18-ch65, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 104
Mean 50.8
Std Dev 3.553
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

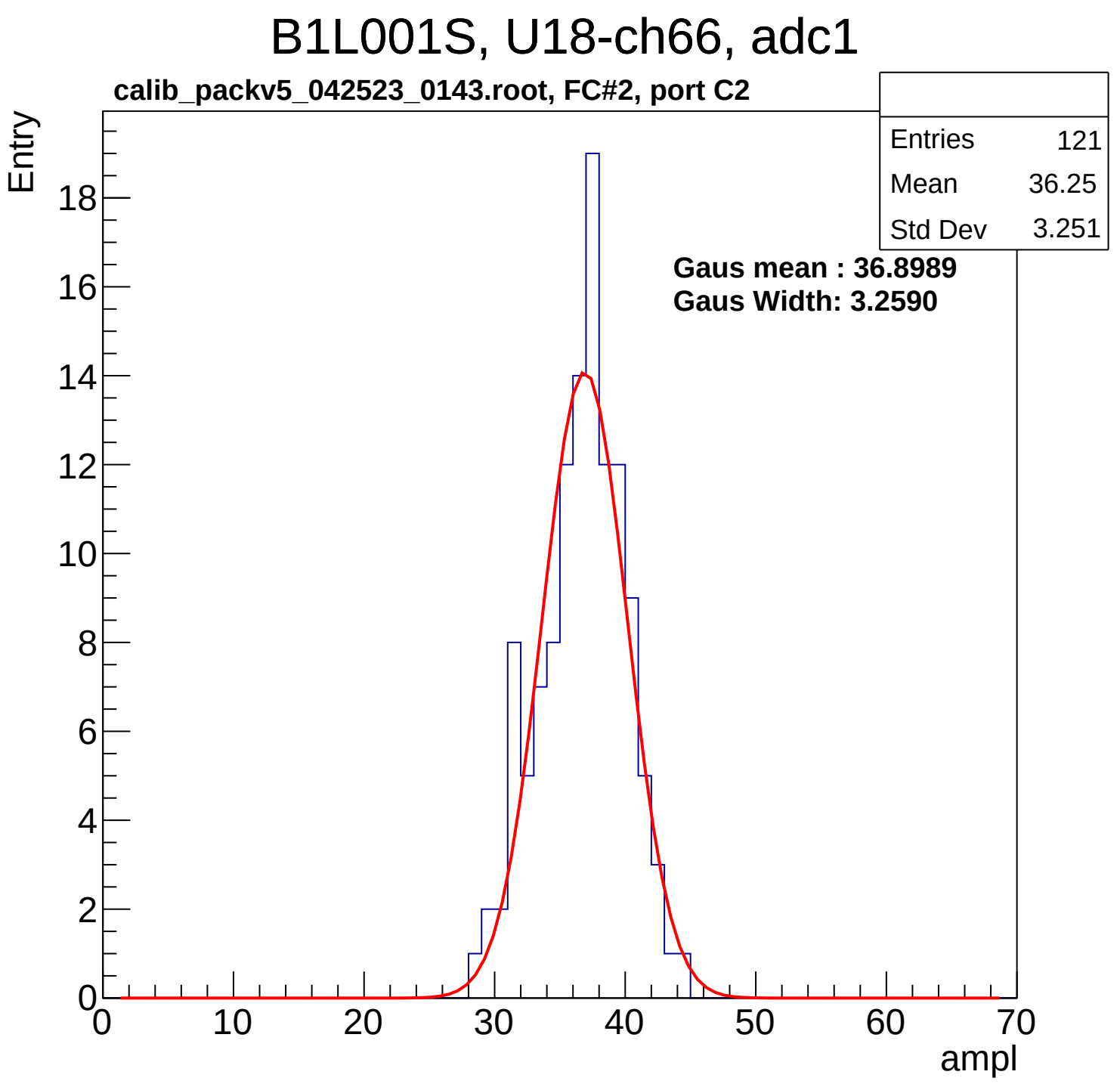

B1L001S, U18-ch65, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 107
Mean 55.76
Std Dev 3.417
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70

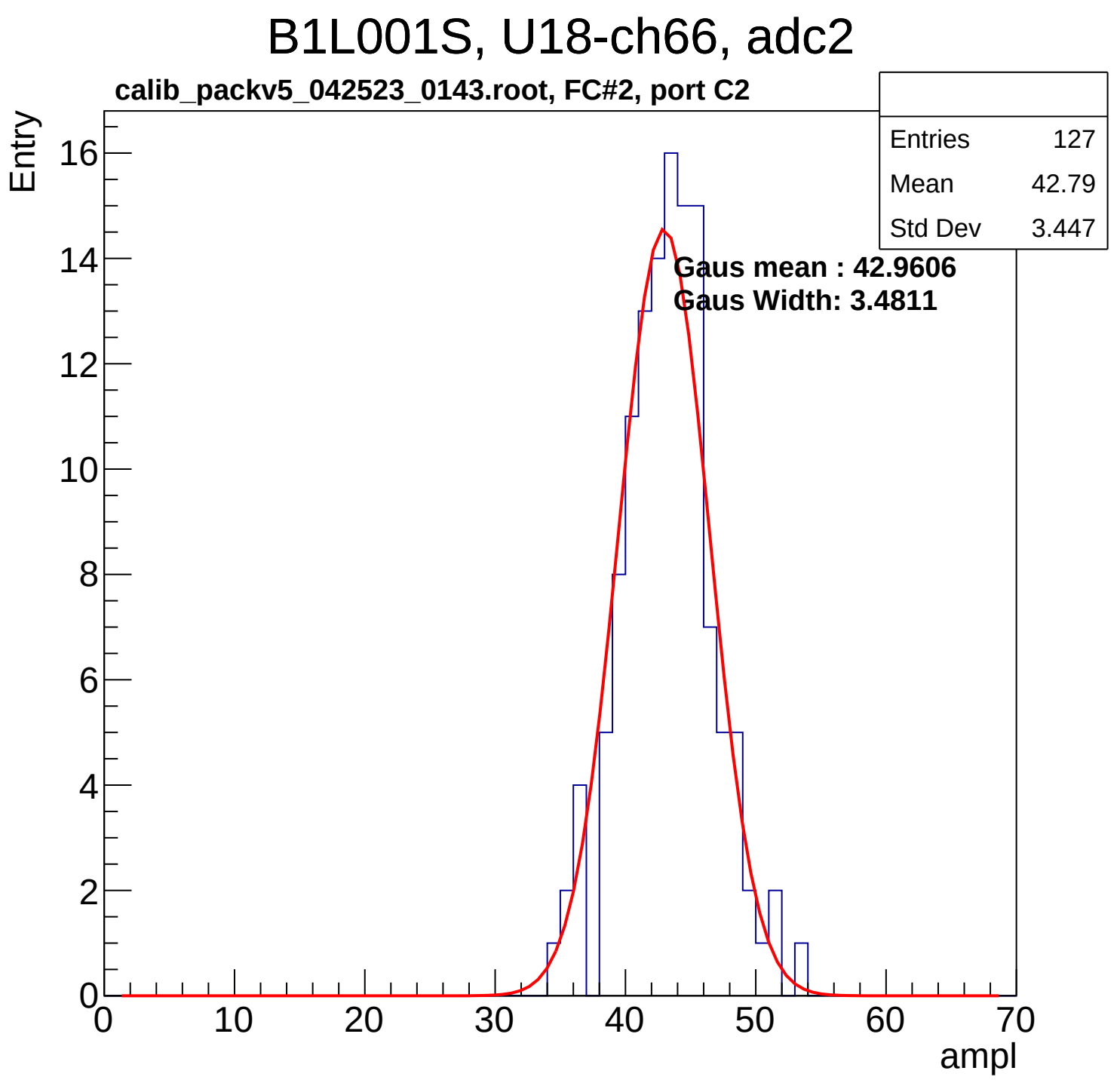

B1L001S, U18-ch65, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 96
Mean 58.79
Std Dev 8.894
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

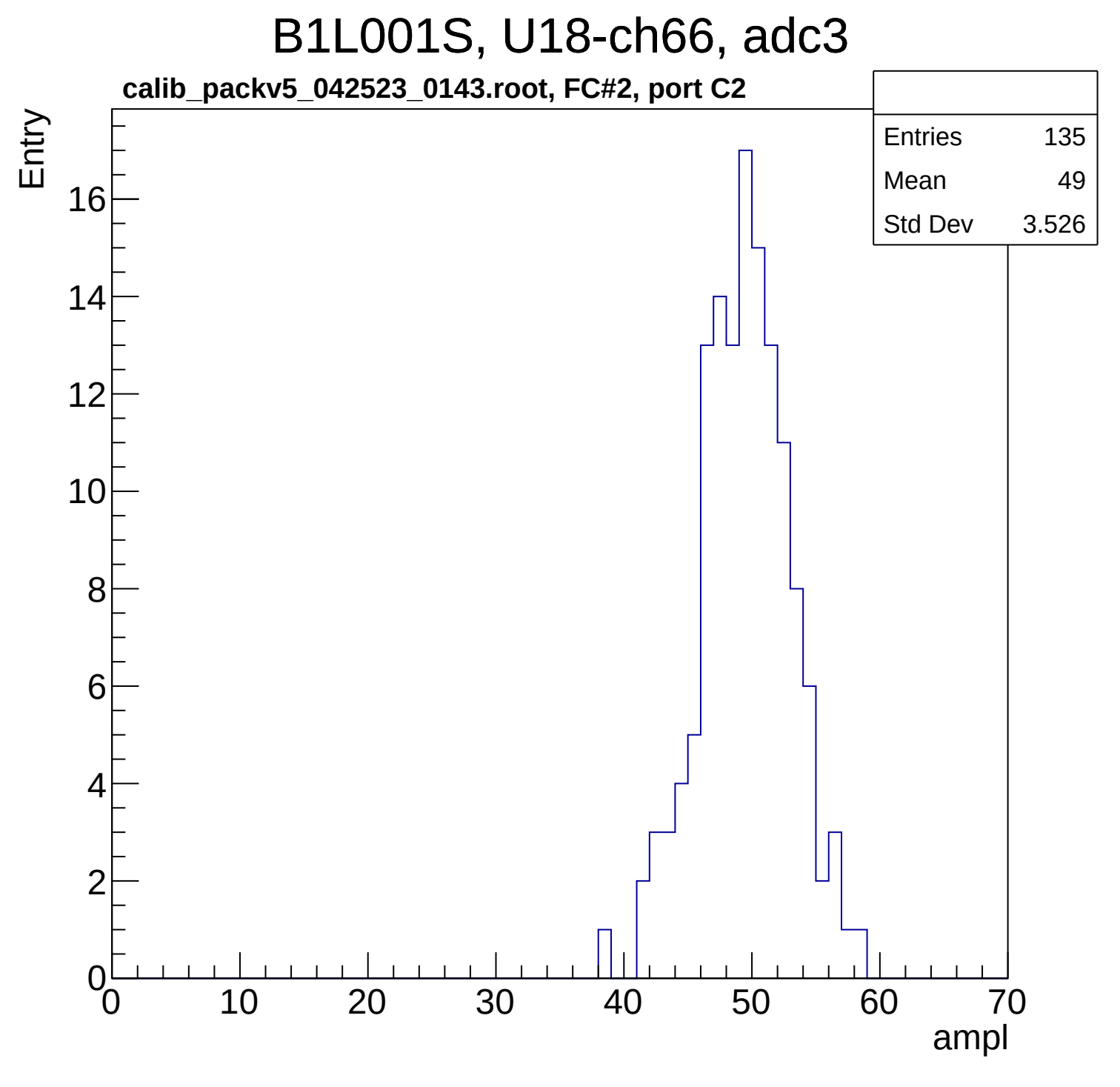

B1L001S, U18-ch65, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 4
Mean 62.5
Std Dev 0.5
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

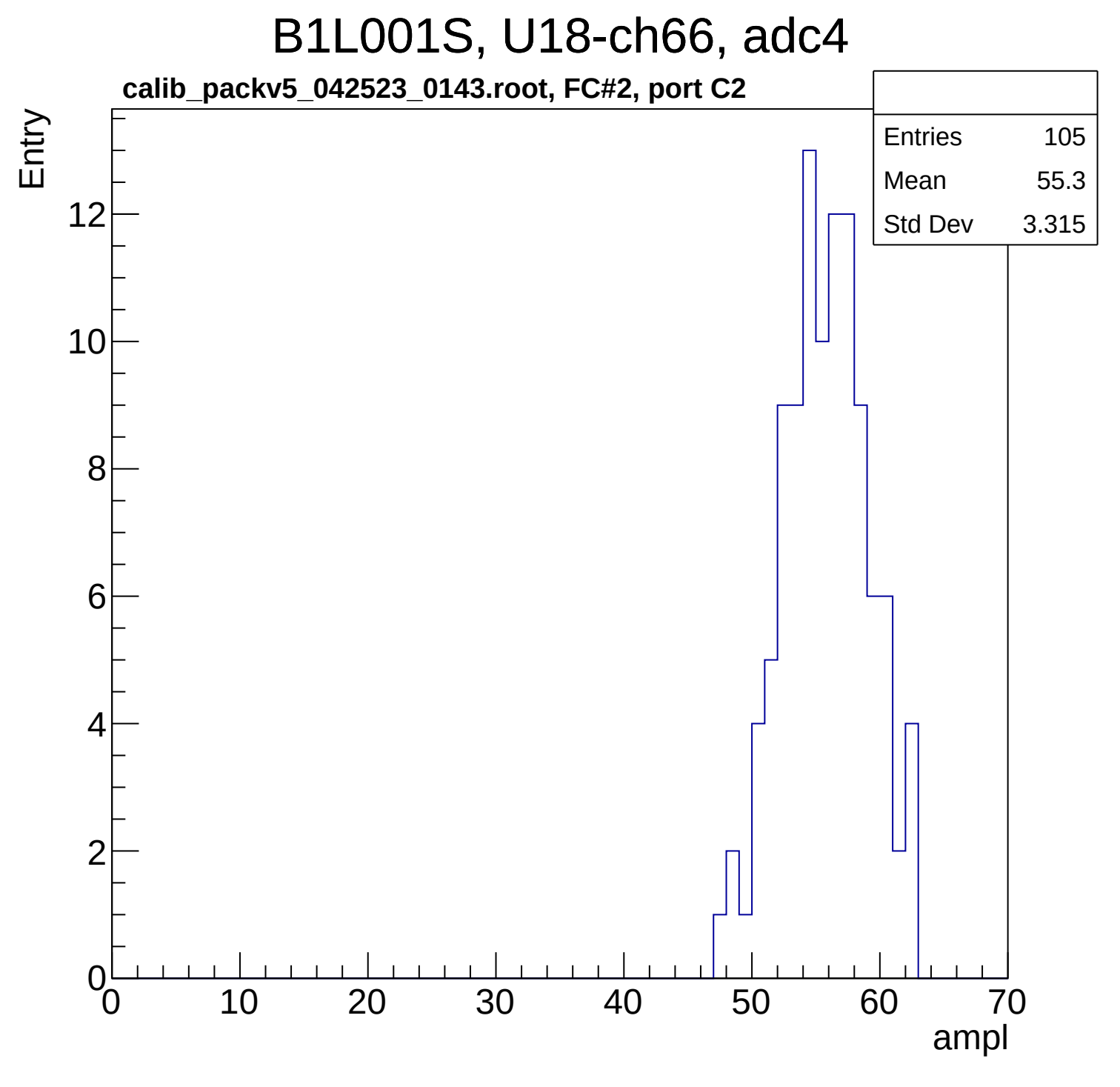

B1L001S, U18-ch65, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

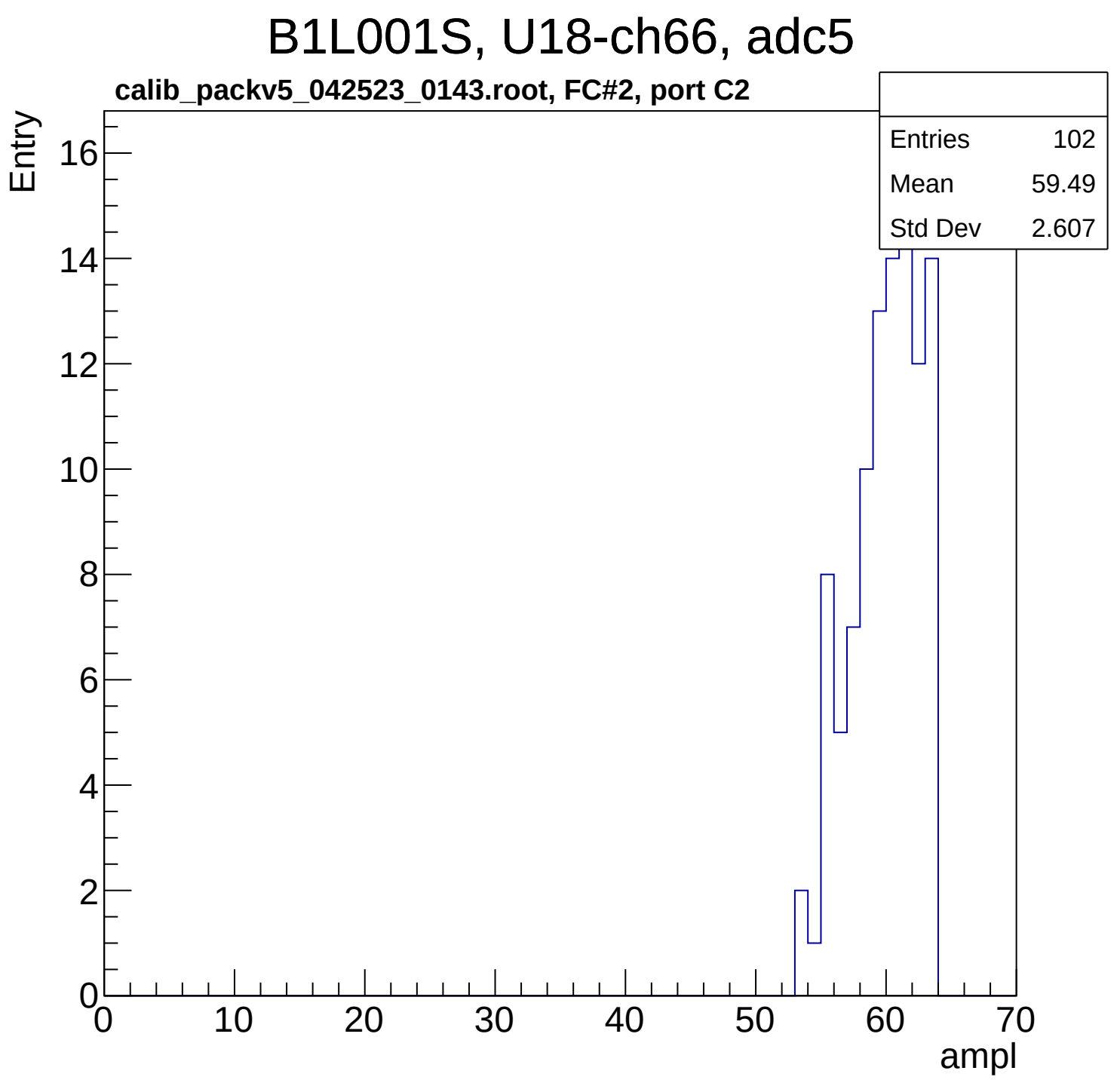

B1L001S, U18-ch66, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 142
Mean 29.56
Std Dev 3.632
Gaus mean : 30.4851
Gaus Width: 3.3243
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

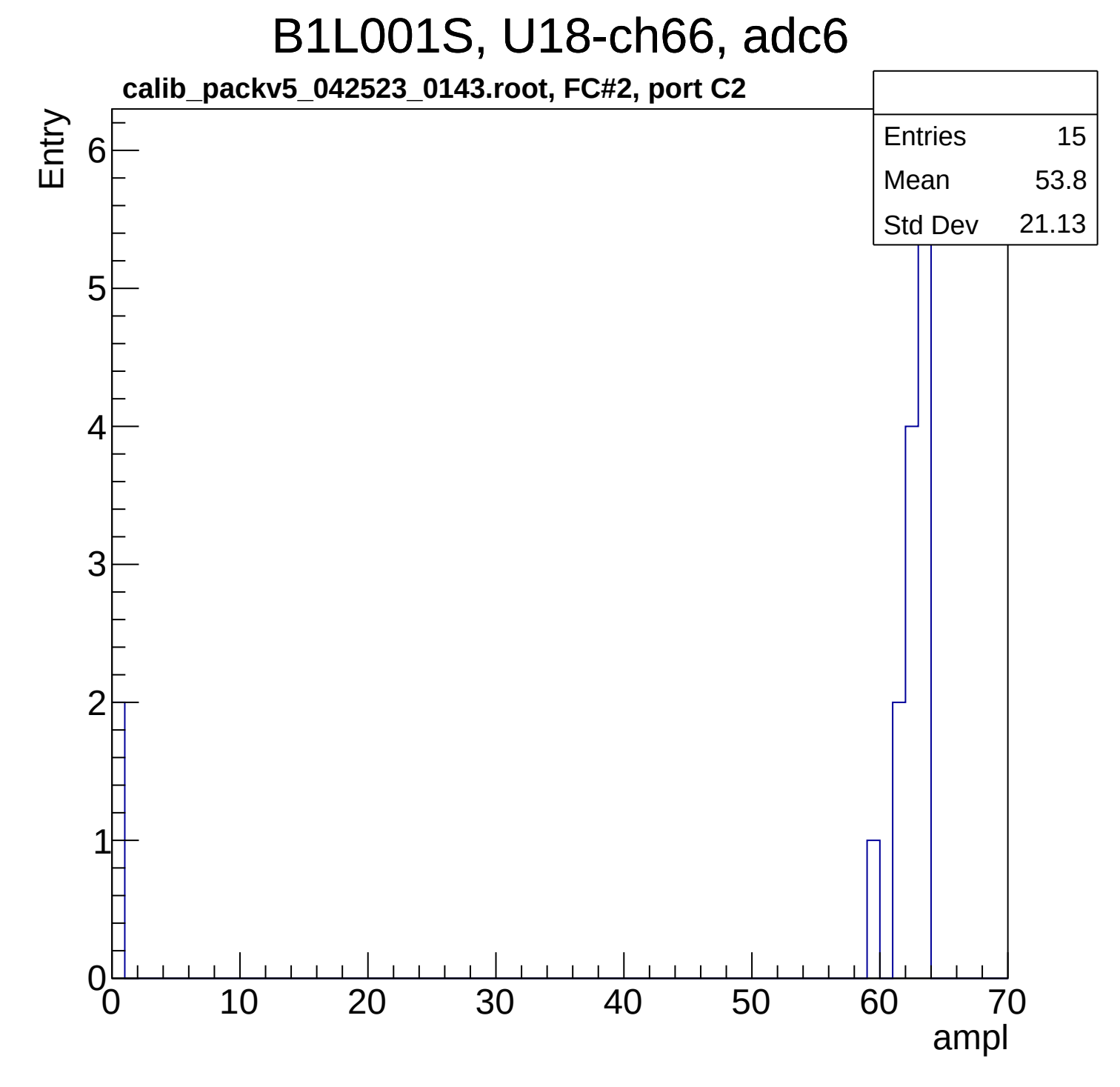

B1L001S, U18-ch66, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 121
Mean 36.25
Std Dev 3.251
Gaus mean : 36.8989
Gaus Width: 3.2590
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

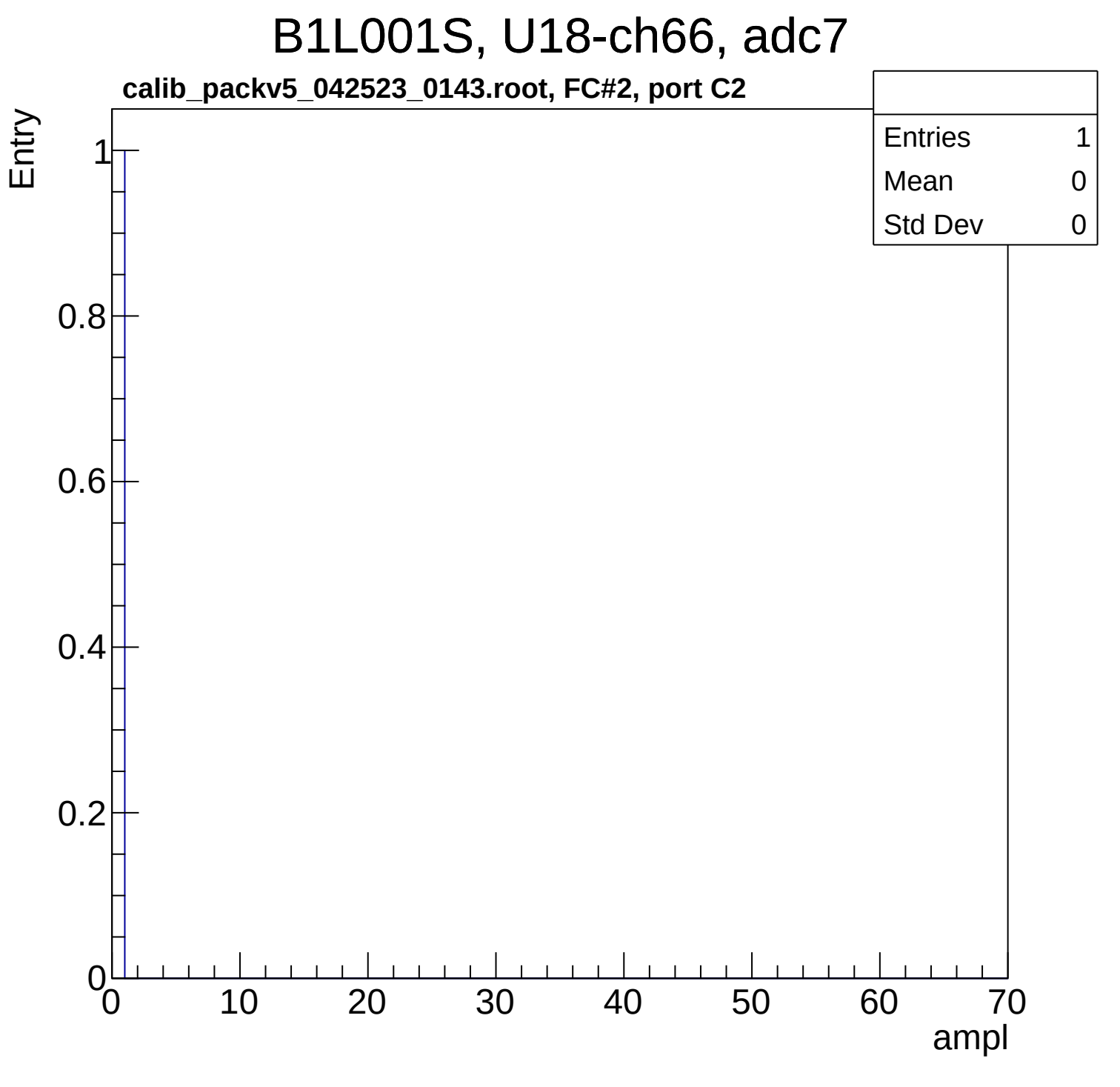

B1L001S, U18-ch66, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 127
Mean 42.79
Std Dev 3.447
Gaus mean : 42.9606
Gaus Width: 3.4811
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

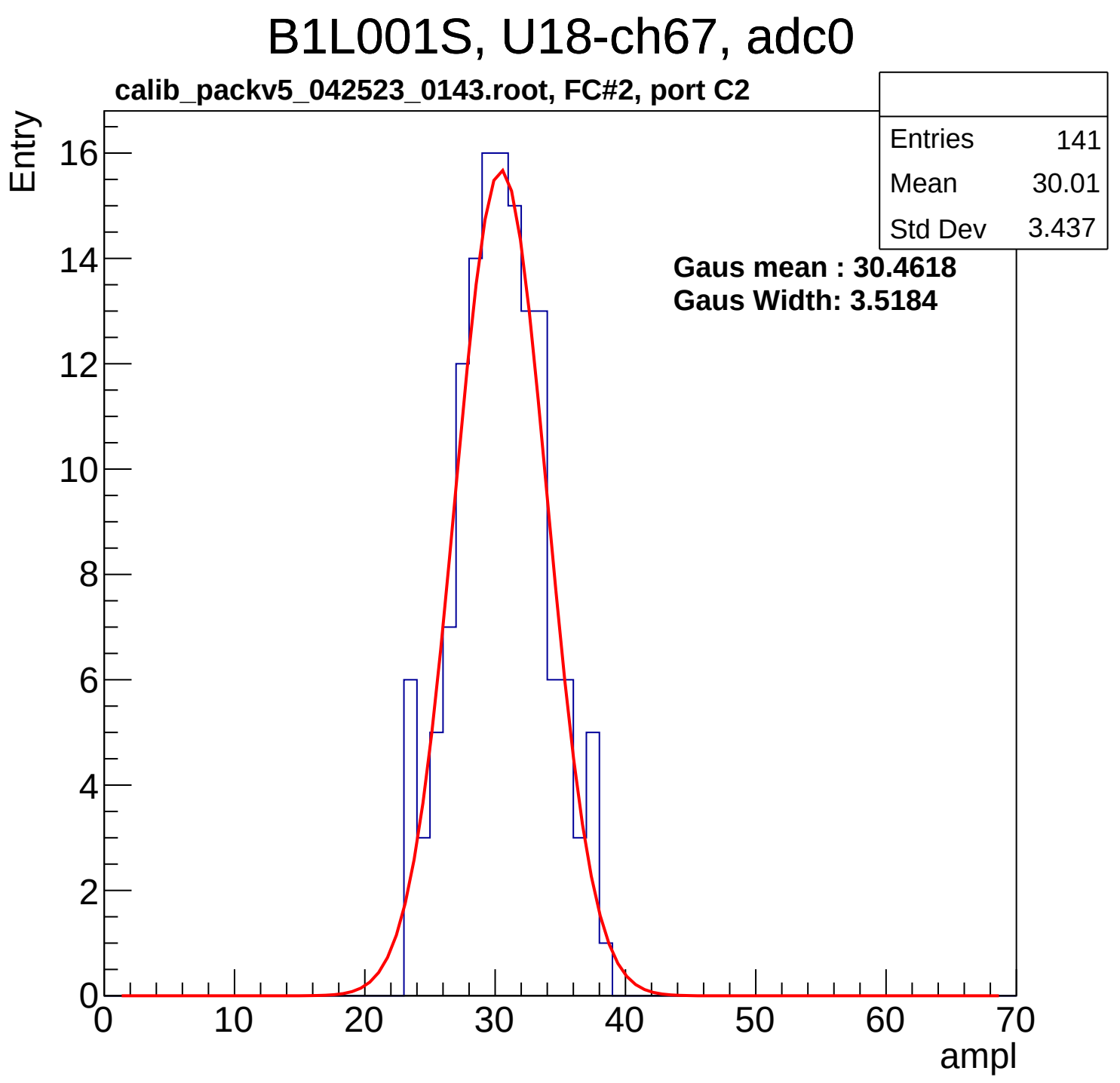

B1L001S, U18-ch66, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 135
Mean 49
Std Dev 3.526
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

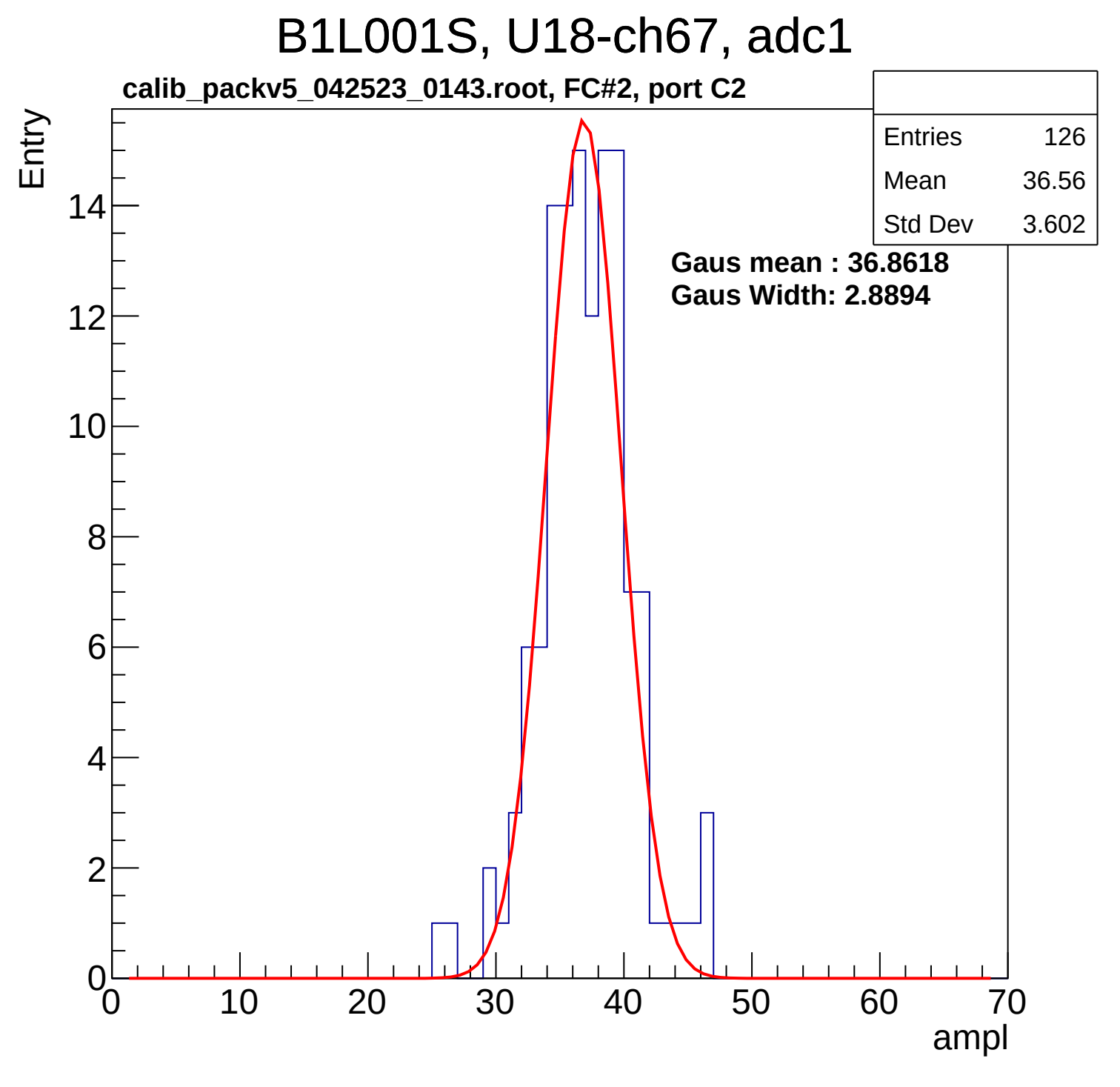

B1L001S, U18-ch66, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 105
Mean 55.3
Std Dev 3.315
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl

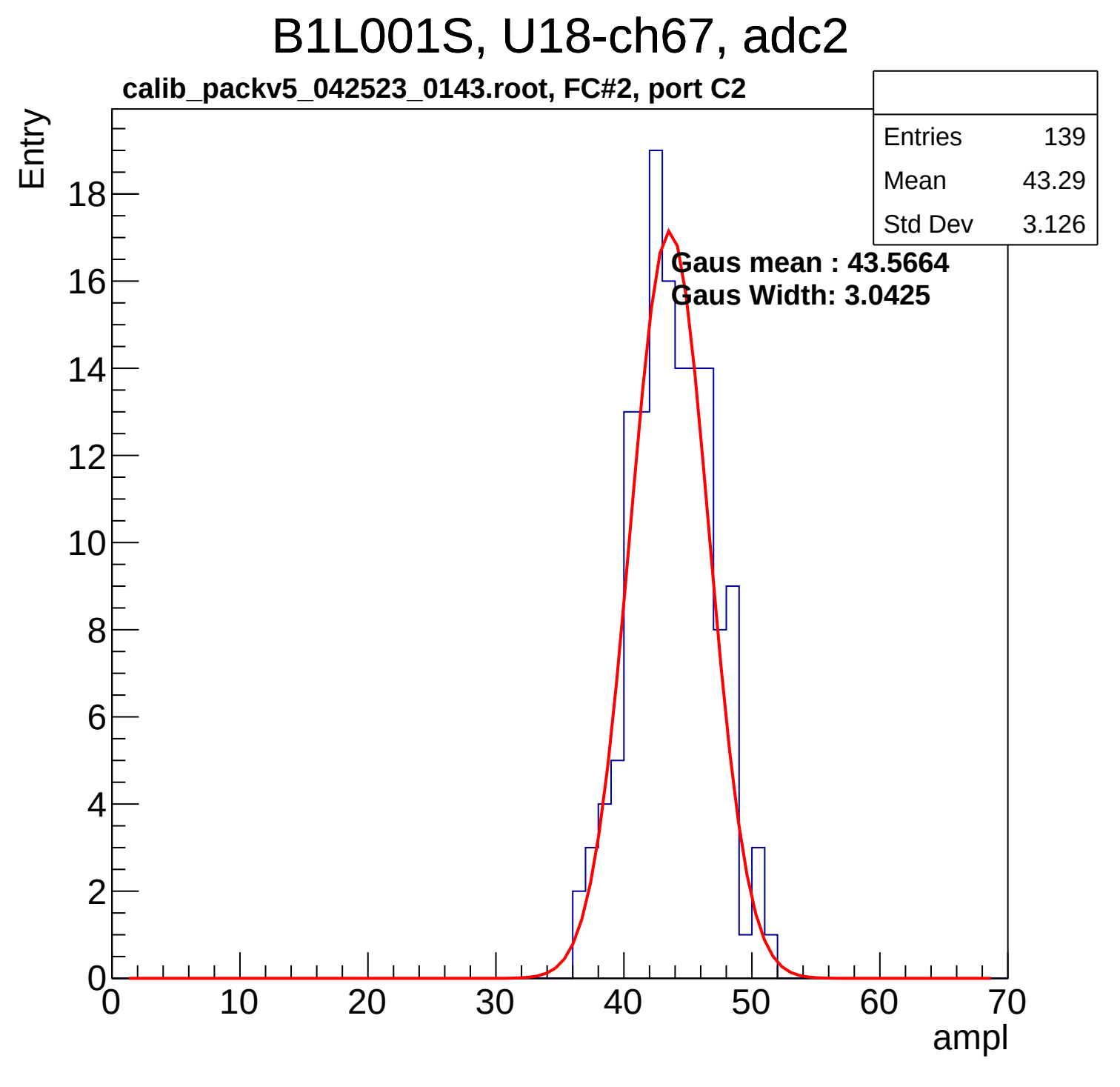

B1L001S, U18-ch66, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 102
Mean 59.49
Std Dev 2.607
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

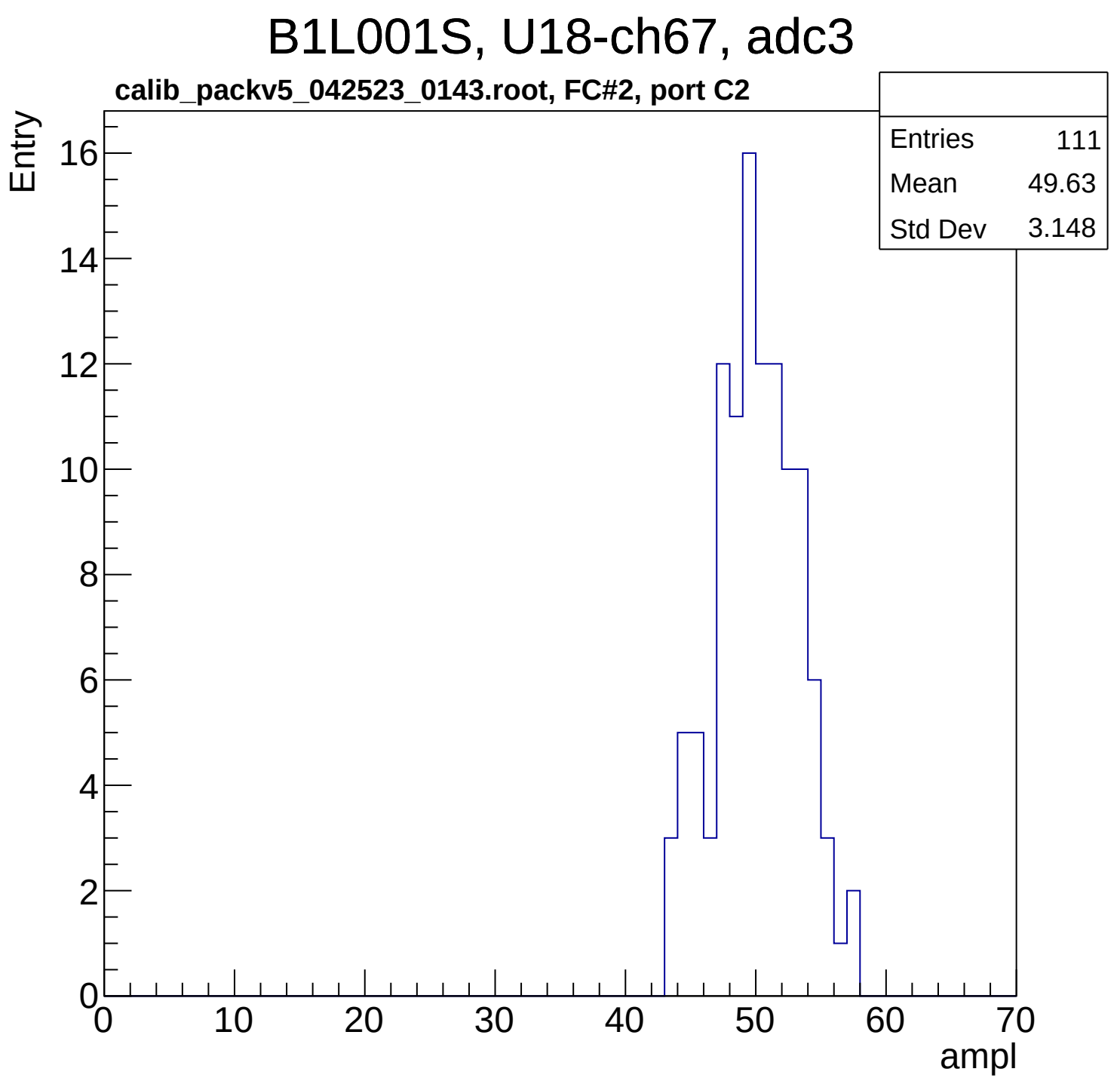

B1L001S, U18-ch66, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 15
Mean 53.8
Std Dev 21.13
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl

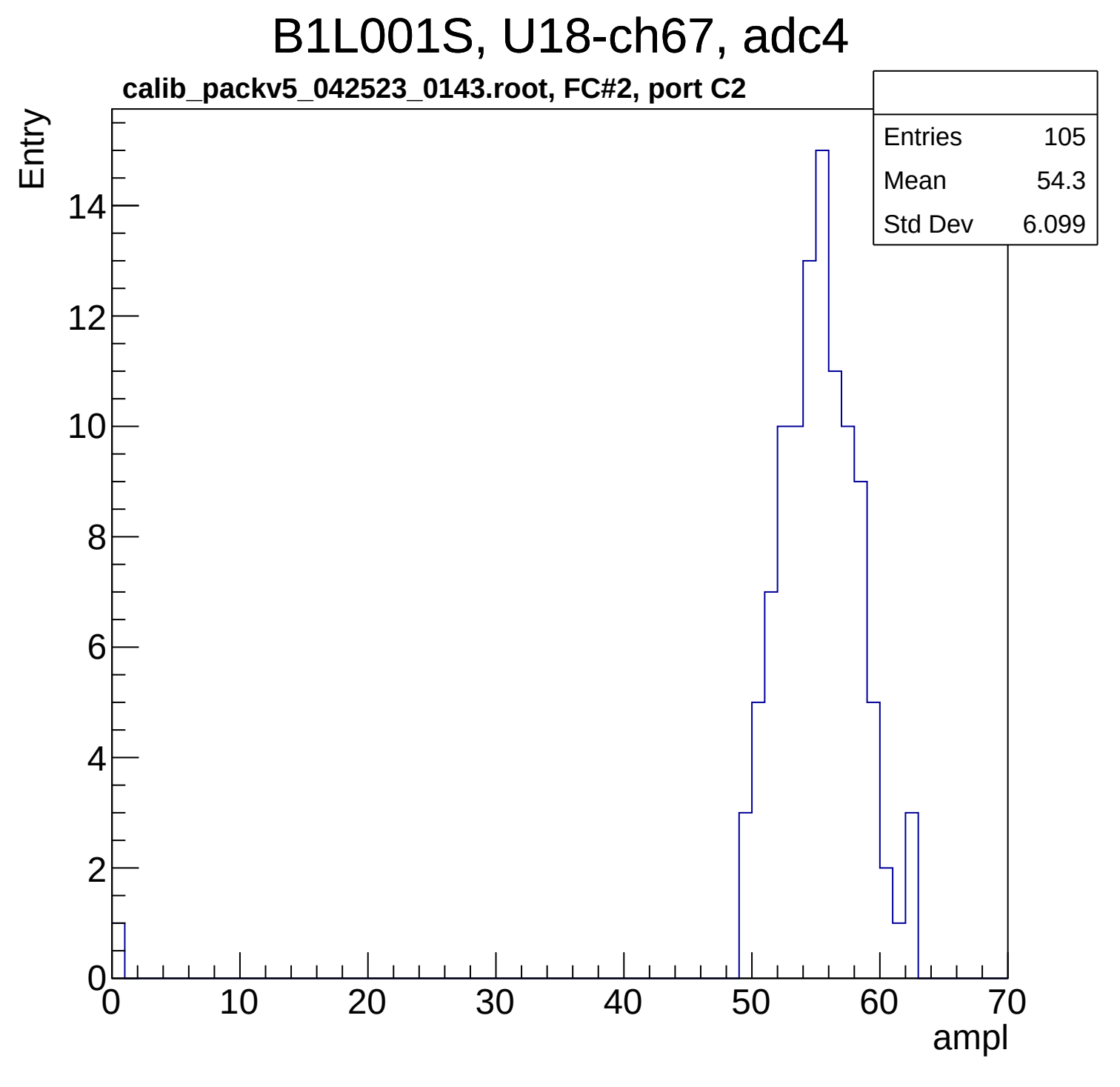

B1L001S, U18-ch66, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

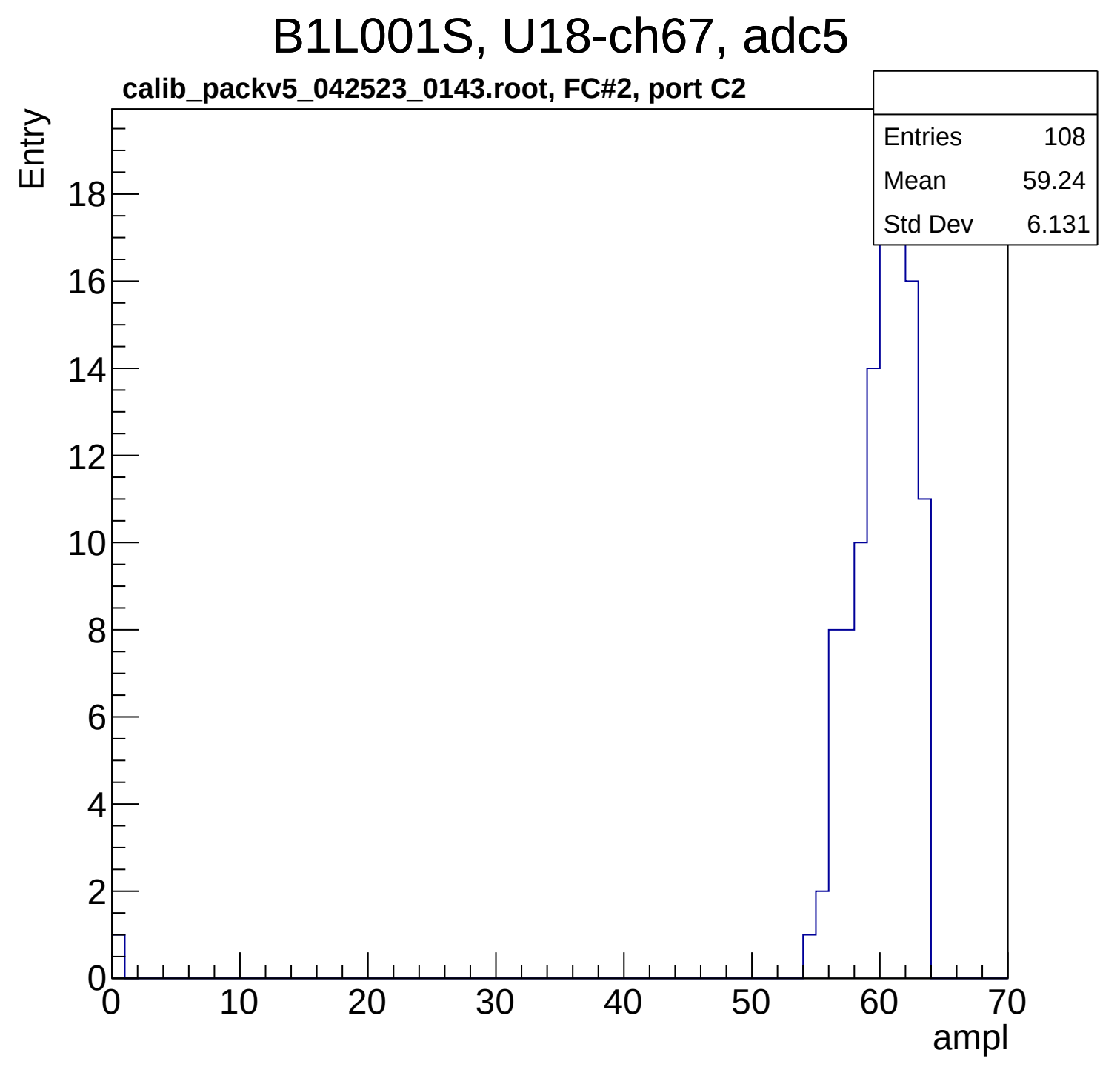

B1L001S, U18-ch67, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 141
Mean 30.01
Std Dev 3.437
Gaus mean : 30.4618
Gaus Width: 3.5184
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

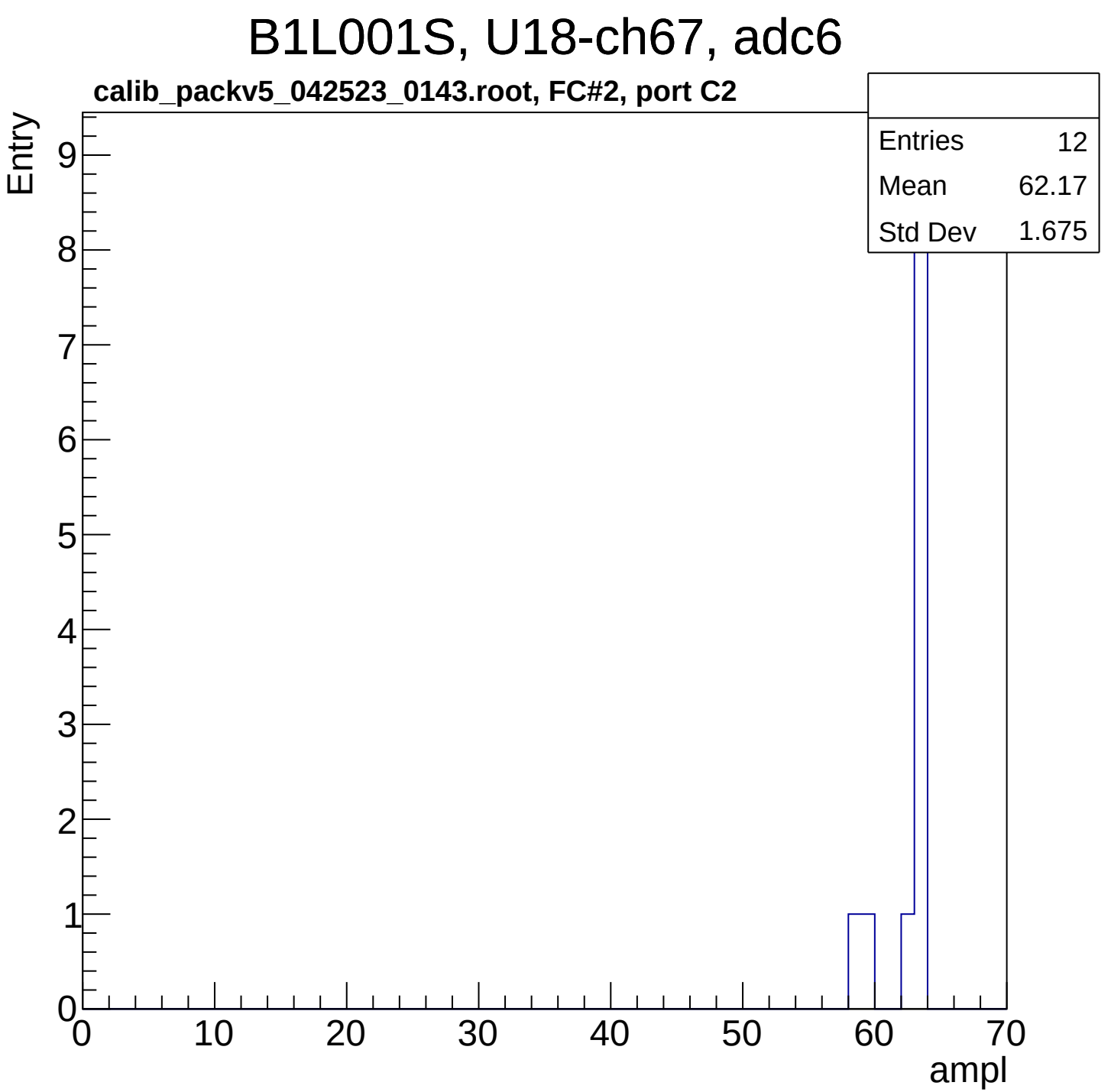

B1L001S, U18-ch67, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 126
Mean 36.56
Std Dev 3.602
Gaus mean : 36.8618
Gaus Width: 2.8894
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

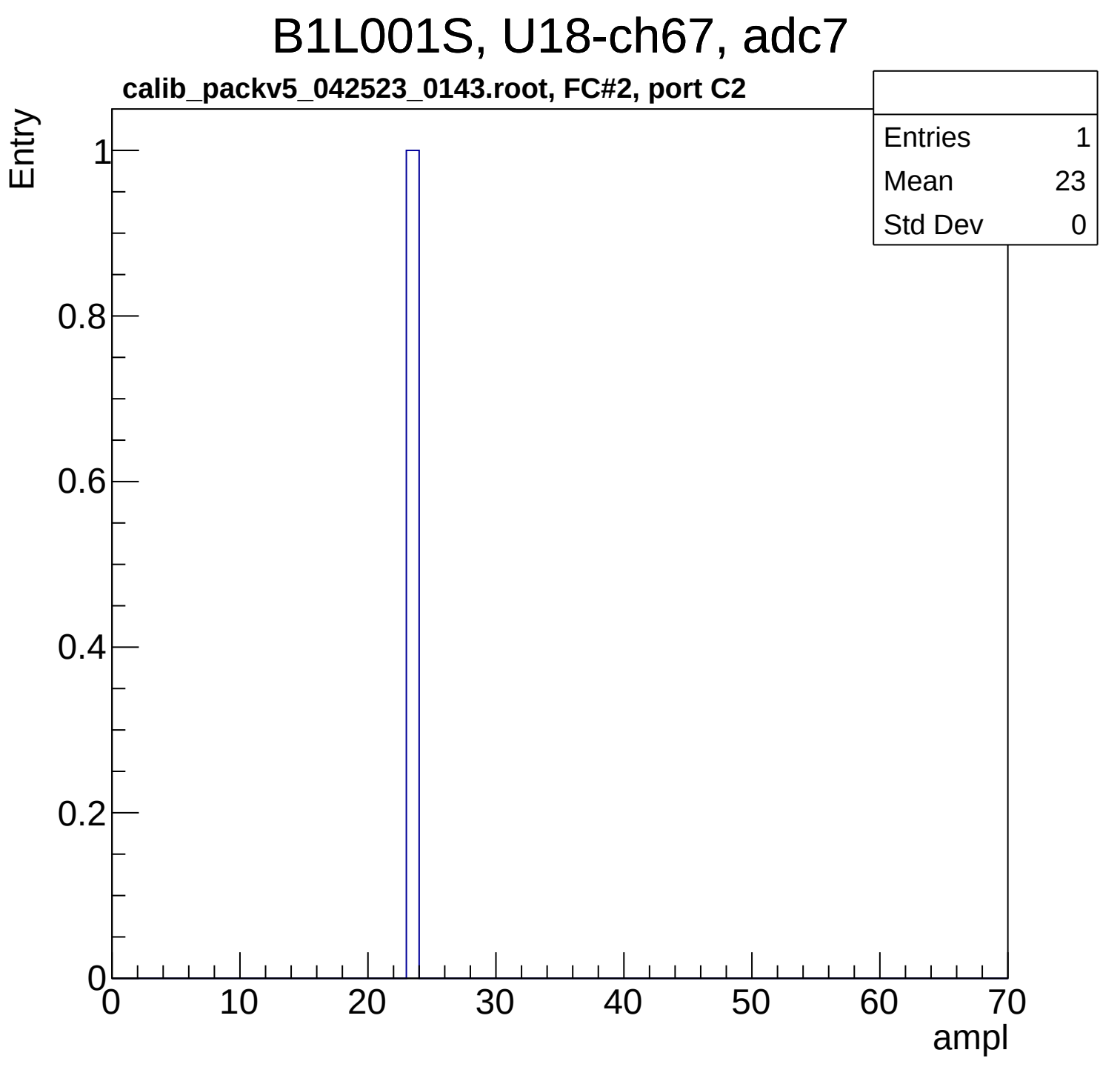

B1L001S, U18-ch67, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 139
Mean 43.29
Std Dev 3.126
Gaus mean : 43.5664
Gaus Width: 3.0425
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

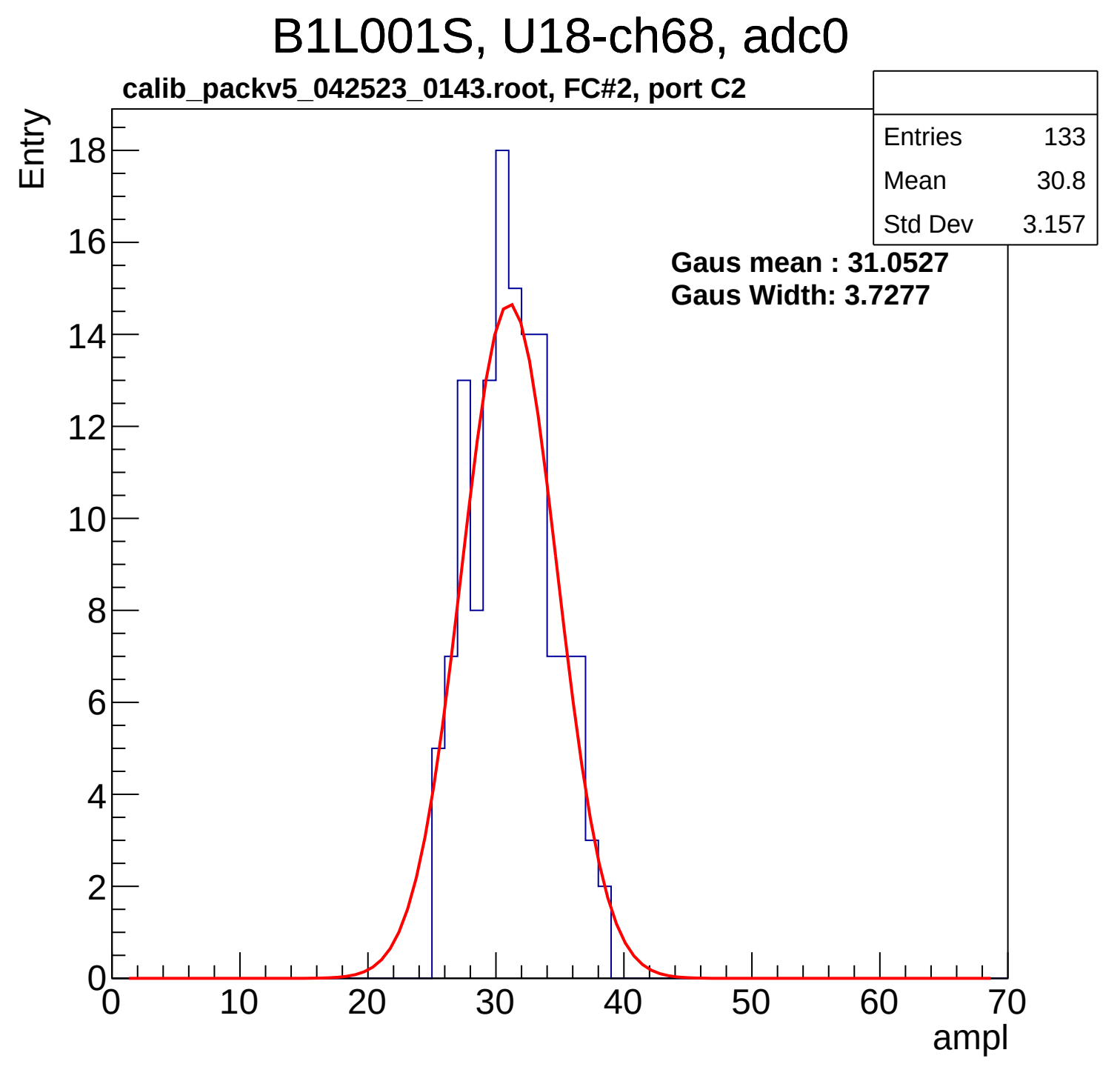

B1L001S, U18-ch67, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 111
Mean 49.63
Std Dev 3.148
Entry
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl

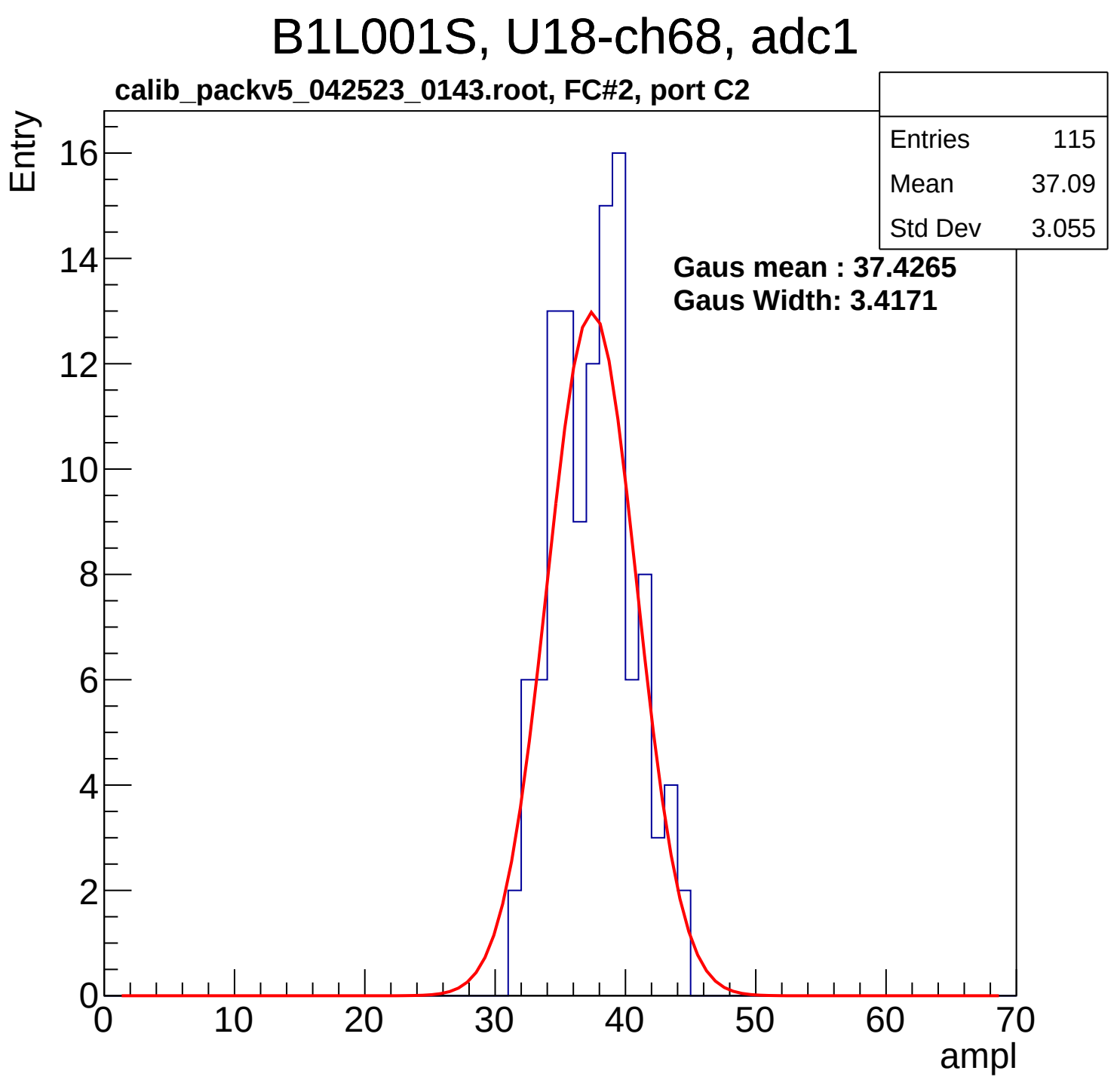

B1L001S, U18-ch67, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 105
Mean 54.3
Std Dev 6.099
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl

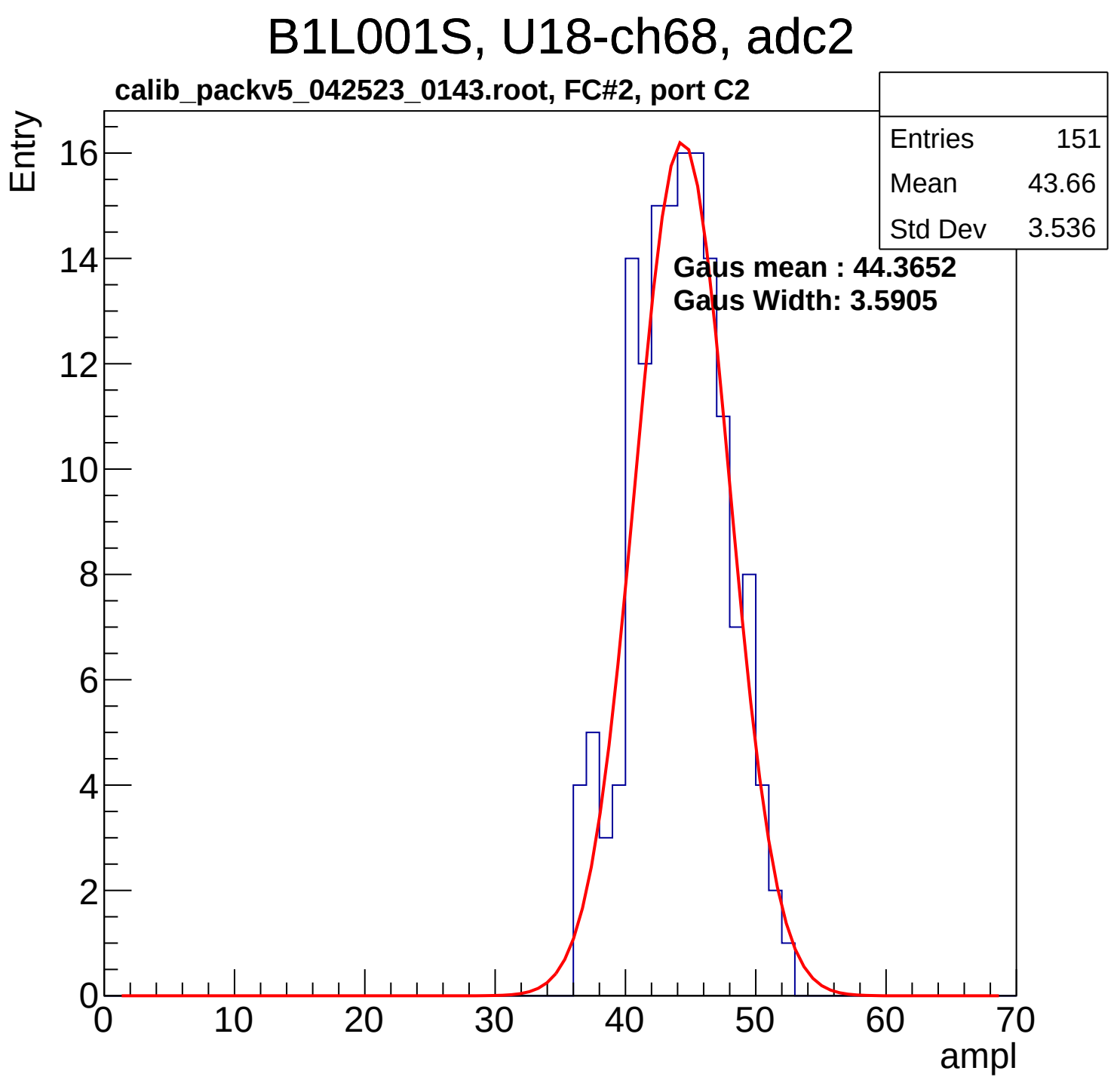

B1L001S, U18-ch67, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 108
Mean 59.24
Std Dev 6.131
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

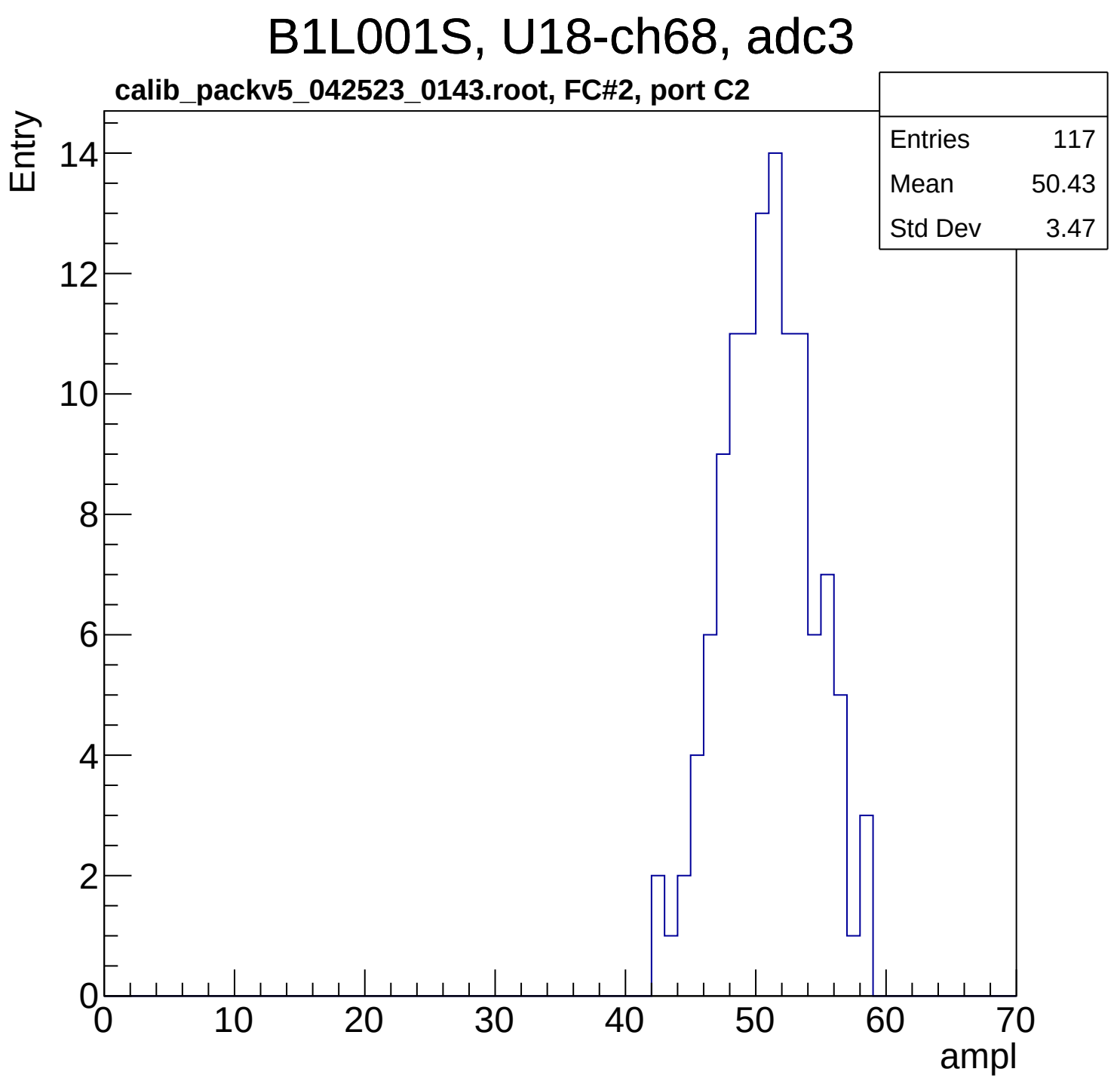

B1L001S, U18-ch67, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 12
Mean 62.17
Std Dev 1.675
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

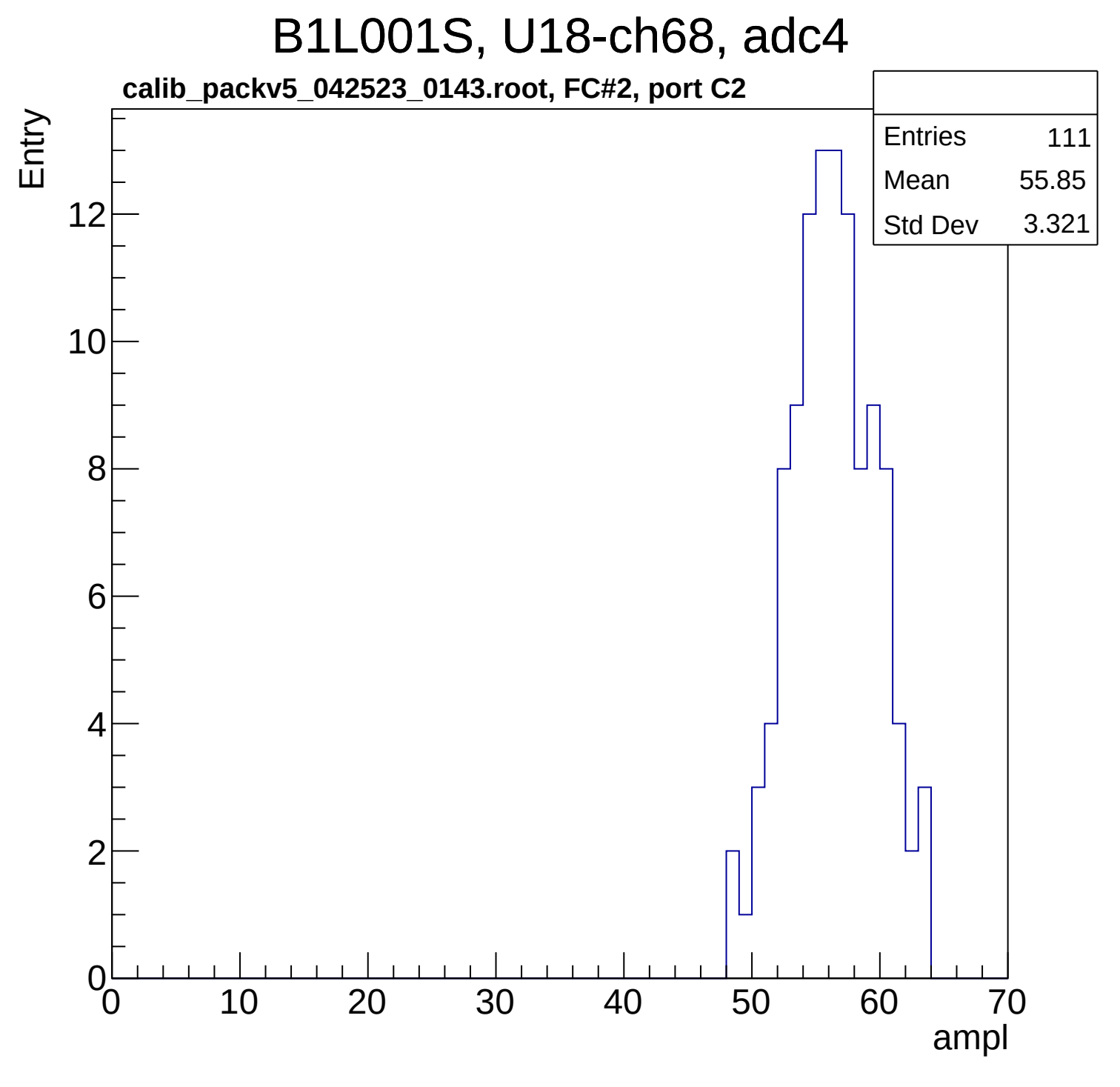

B1L001S, U18-ch67, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 23
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

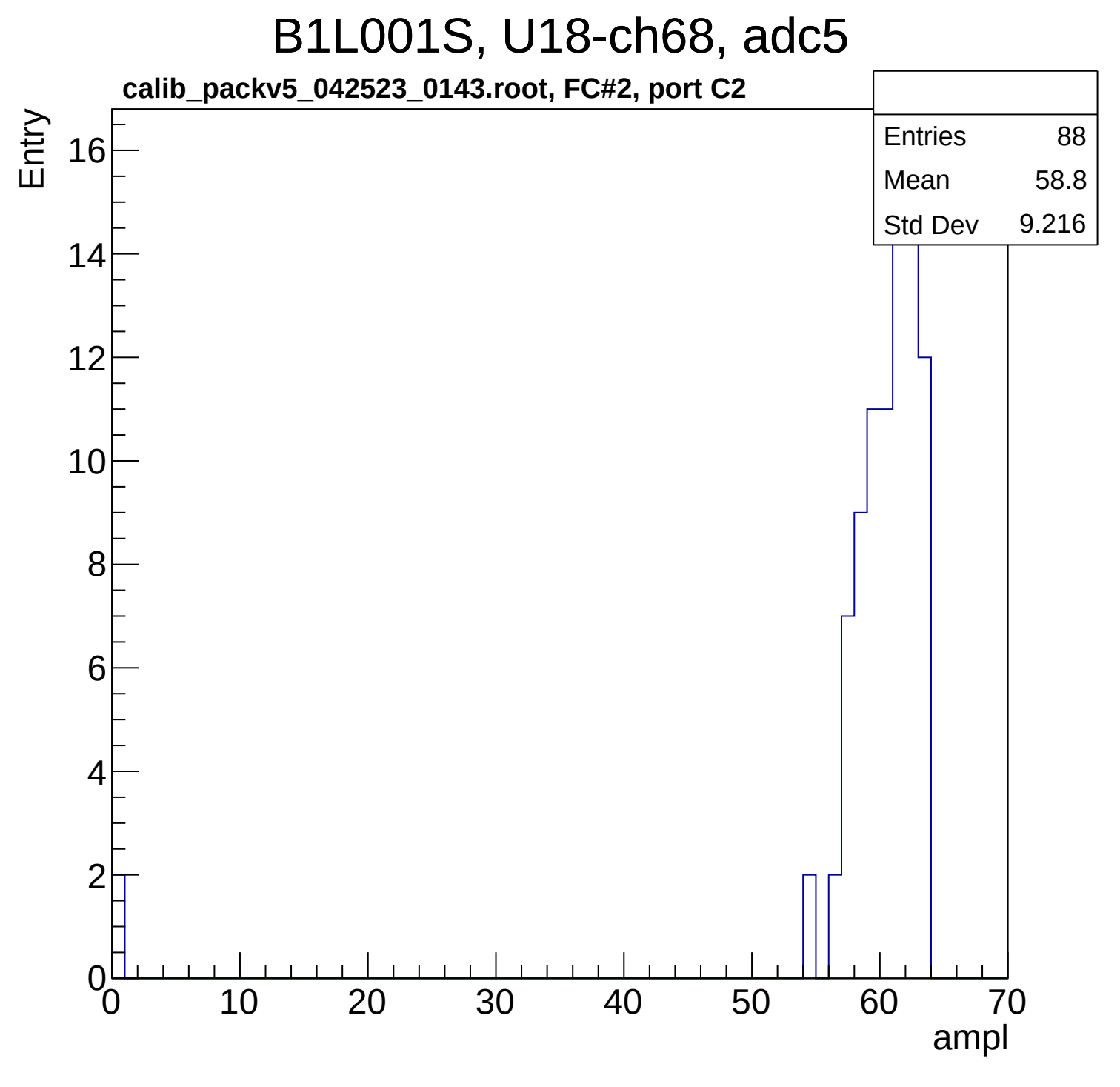

B1L001S, U18-ch68, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 133
Mean 30.8
Std Dev 3.157
Gaus mean : 31.0527
Gaus Width: 3.7277
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

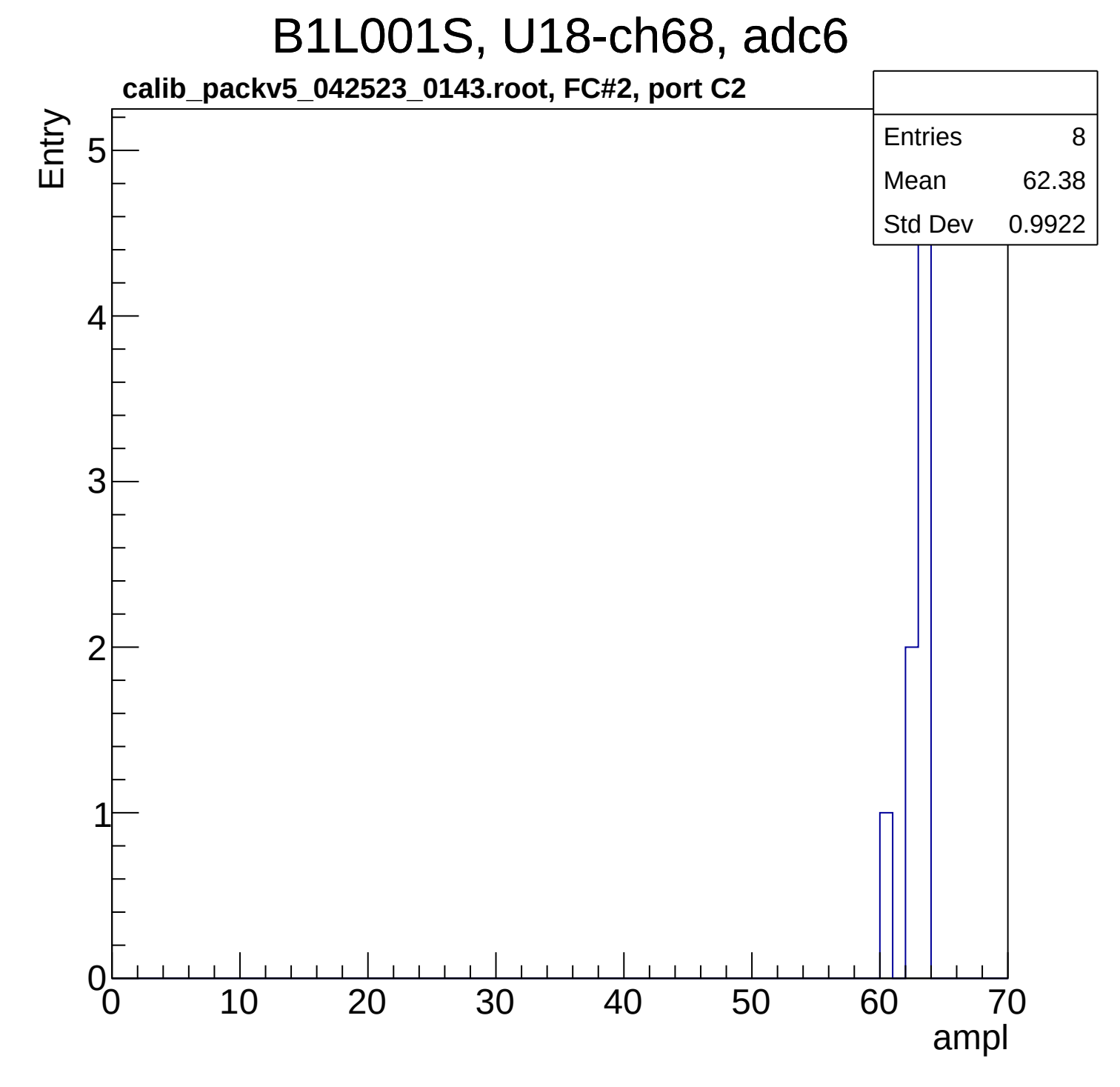

B1L001S, U18-ch68, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 115
Mean 37.09
Std Dev 3.055
Gaus mean : 37.4265
Gaus Width: 3.4171
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

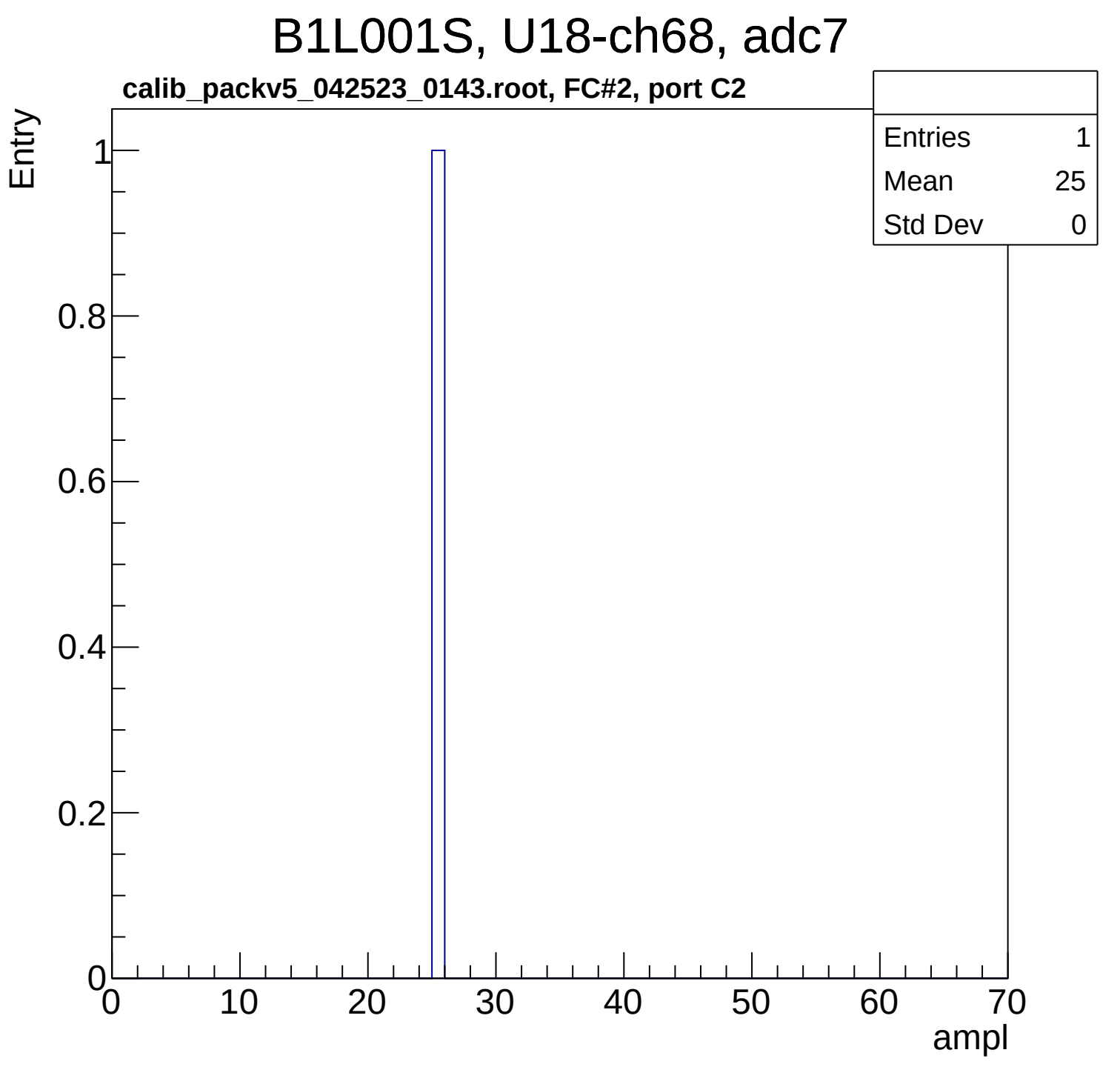

B1L001S, U18-ch68, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 151
Mean 43.66
Std Dev 3.536
Gaus mean : 44.3652
Gaus Width: 3.5905
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

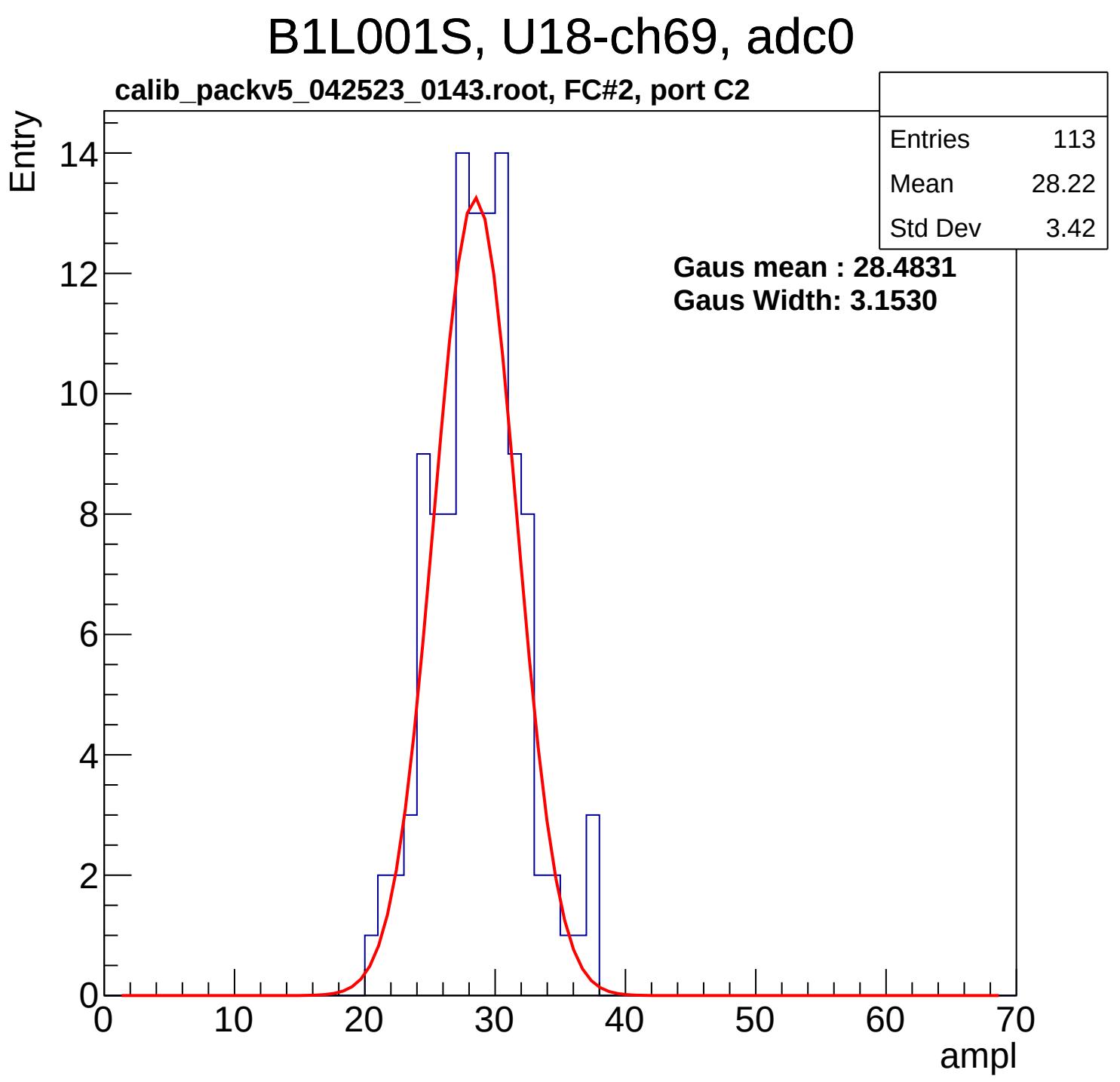

B1L001S, U18-ch68, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 117
Mean 50.43
Std Dev 3.47
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

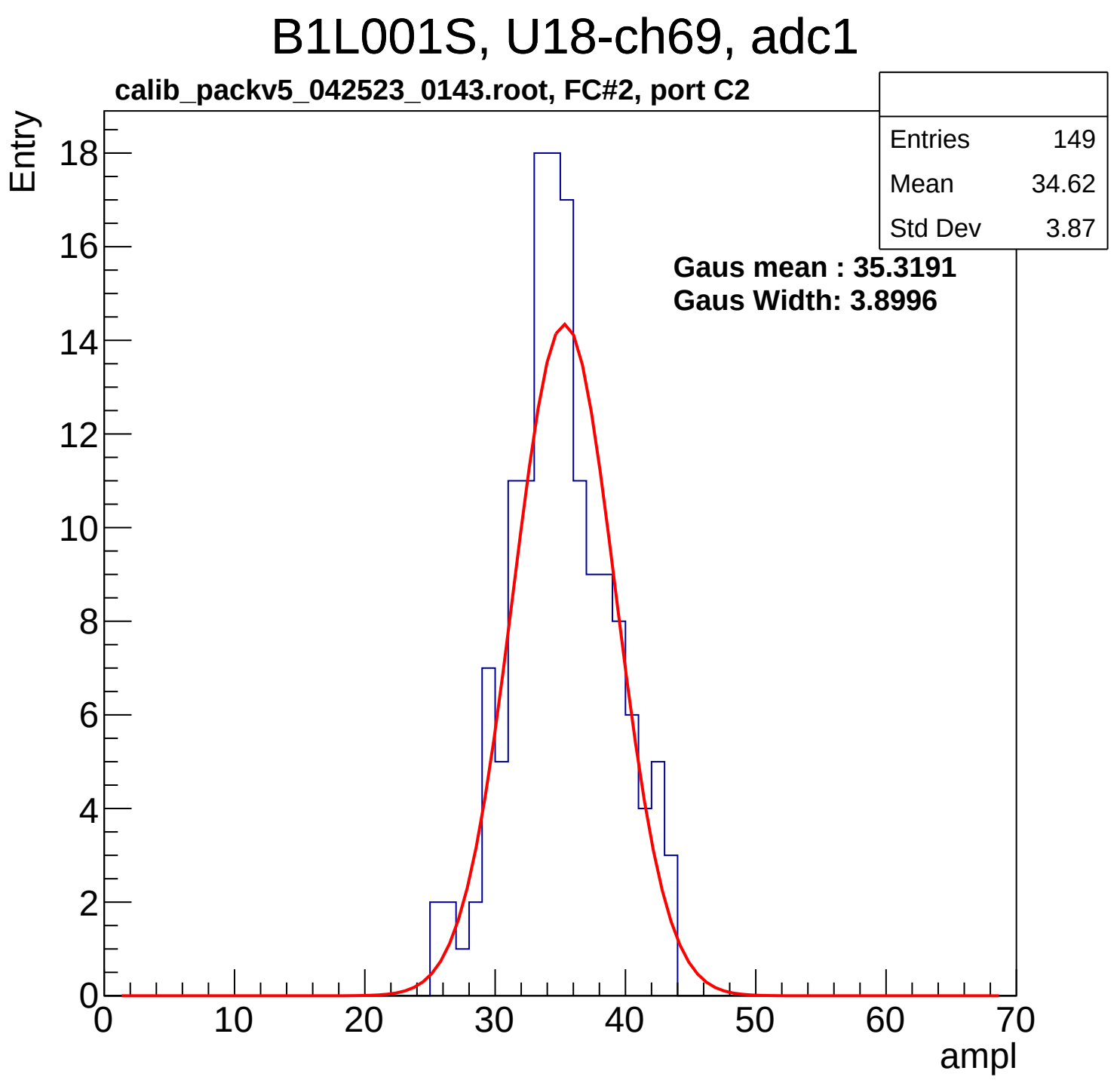

B1L001S, U18-ch68, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 111
Mean 55.85
Std Dev 3.321
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl

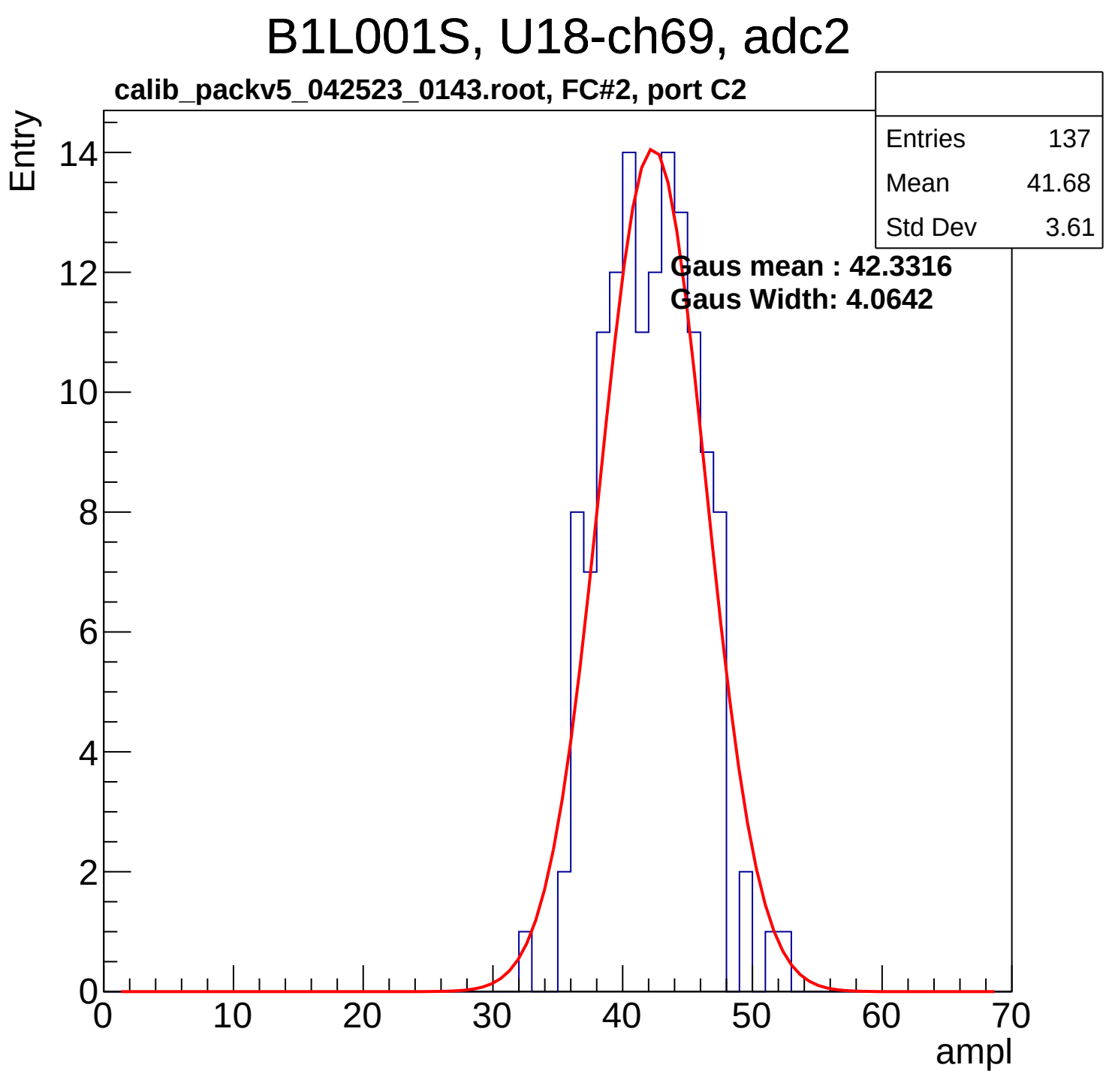

B1L001S, U18-ch68, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 88
Mean 58.8
Std Dev 9.216
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

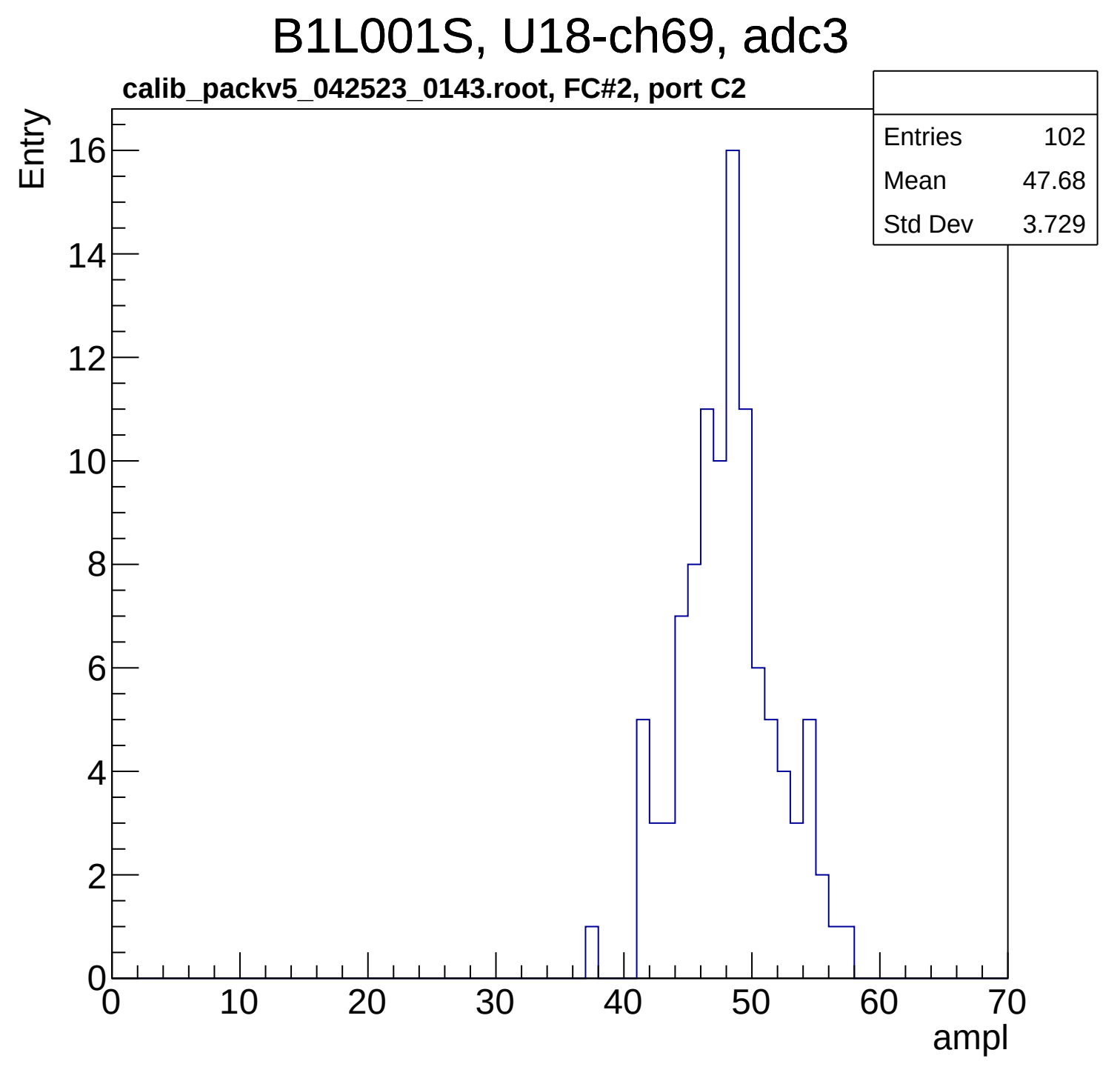

B1L001S, U18-ch68, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 8
Mean 62.38
Std Dev 0.9922
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

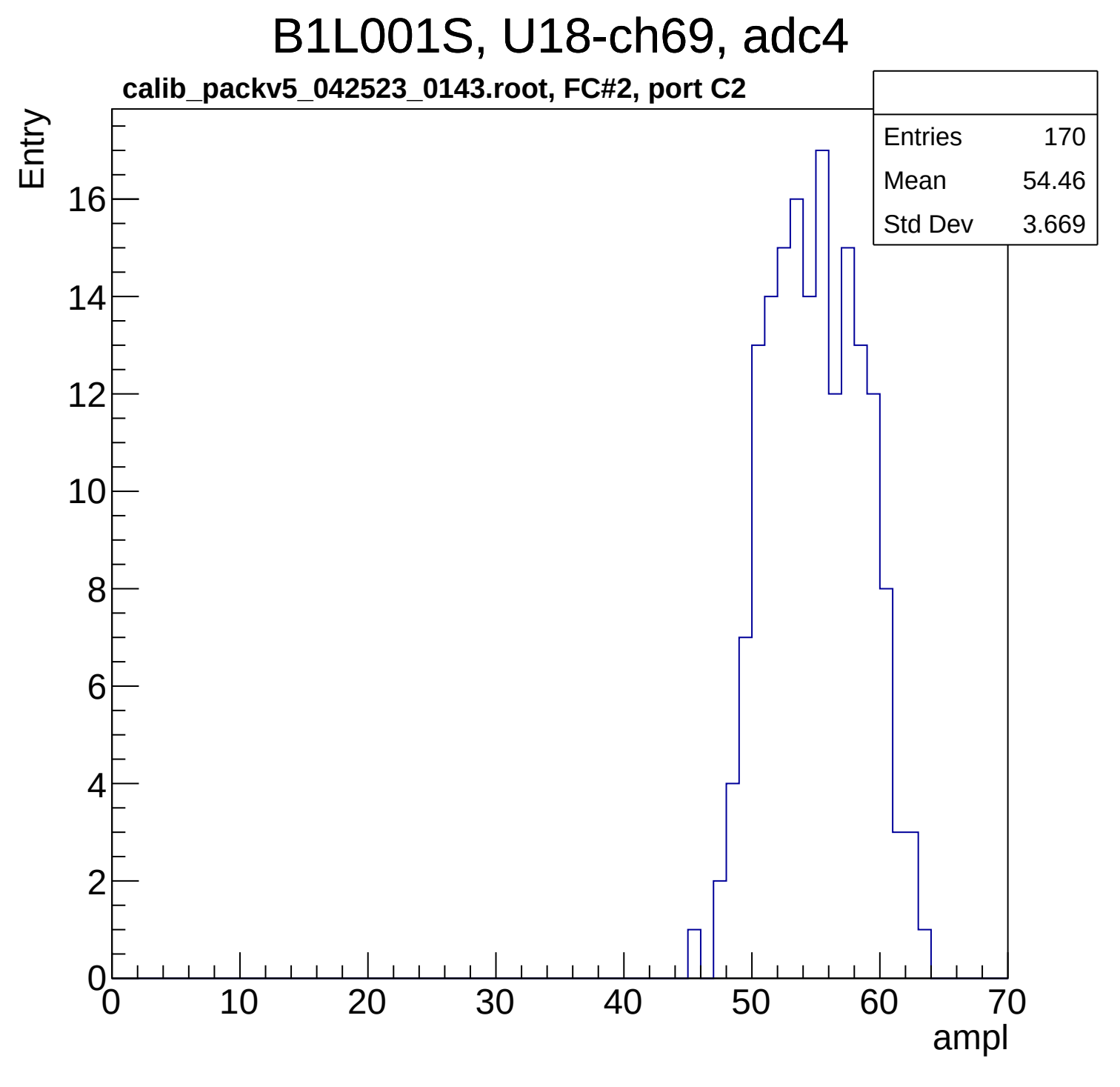

B1L001S, U18-ch68, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 25
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

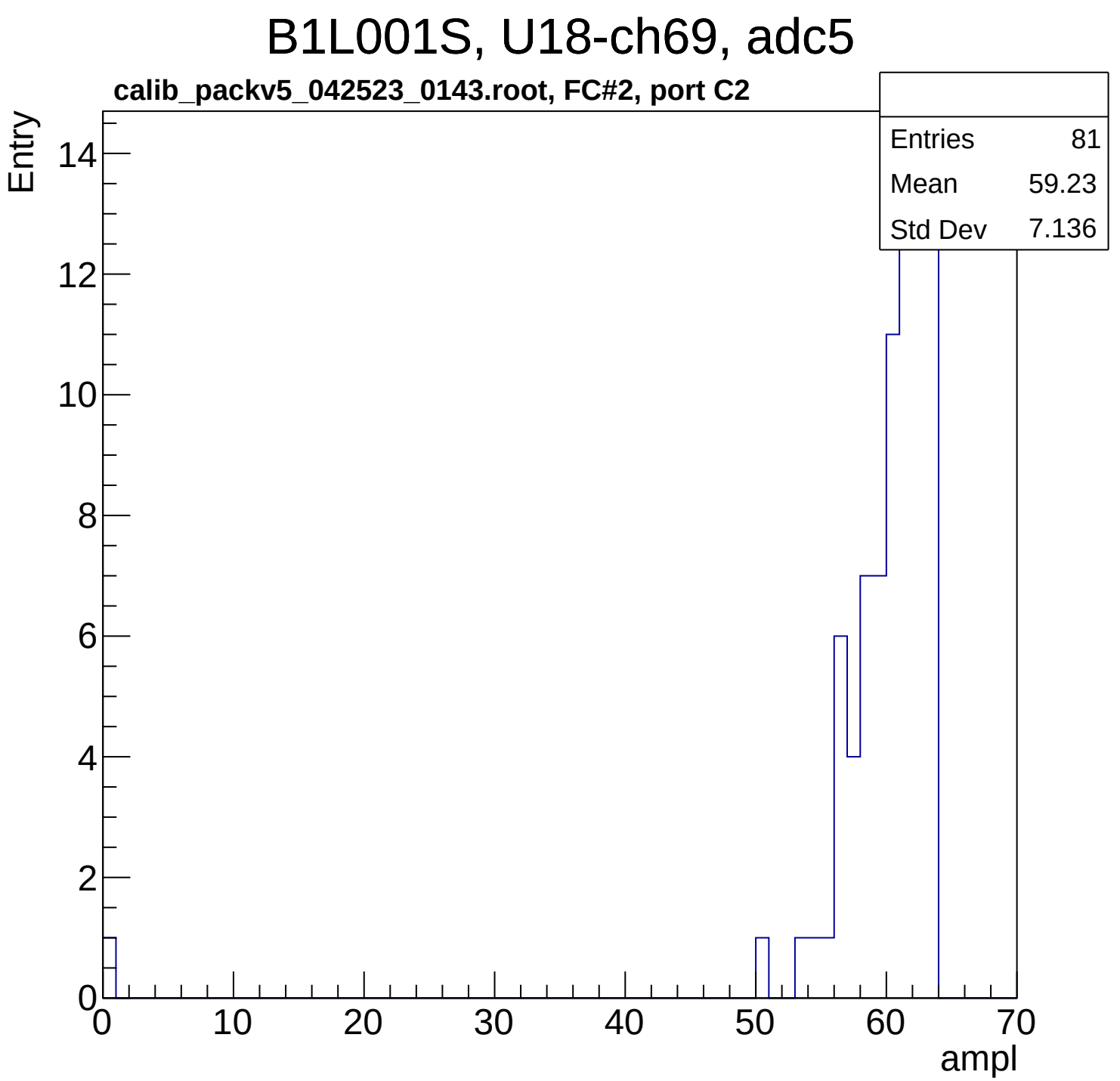

B1L001S, U18-ch69, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 113
Mean 28.22
Std Dev 3.42
Gaus mean : 28.4831
Gaus Width: 3.1530
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

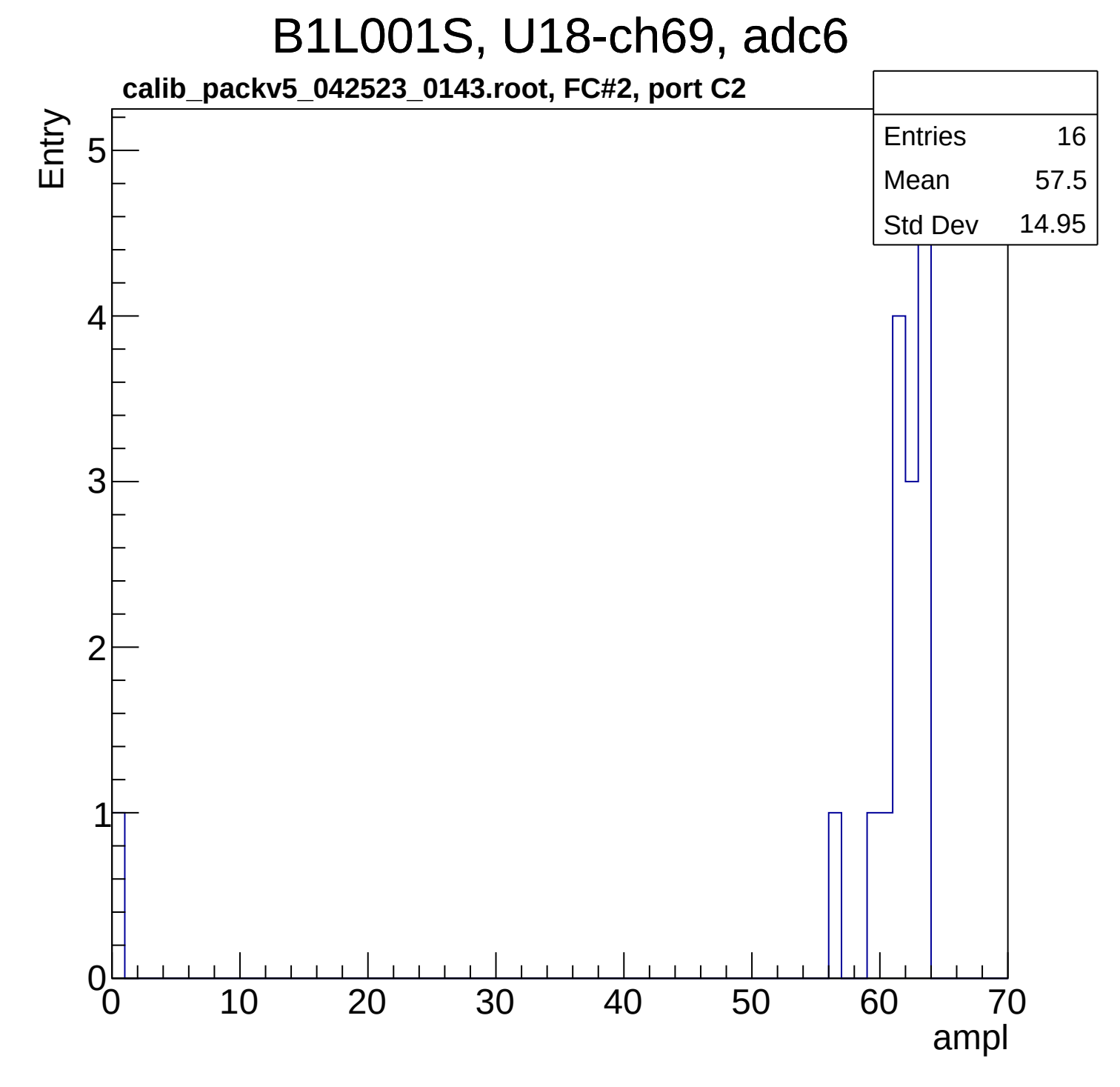

B1L001S, U18-ch69, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 149
Mean 34.62
Std Dev 3.87
Gaus mean : 35.3191
Gaus Width: 3.8996
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

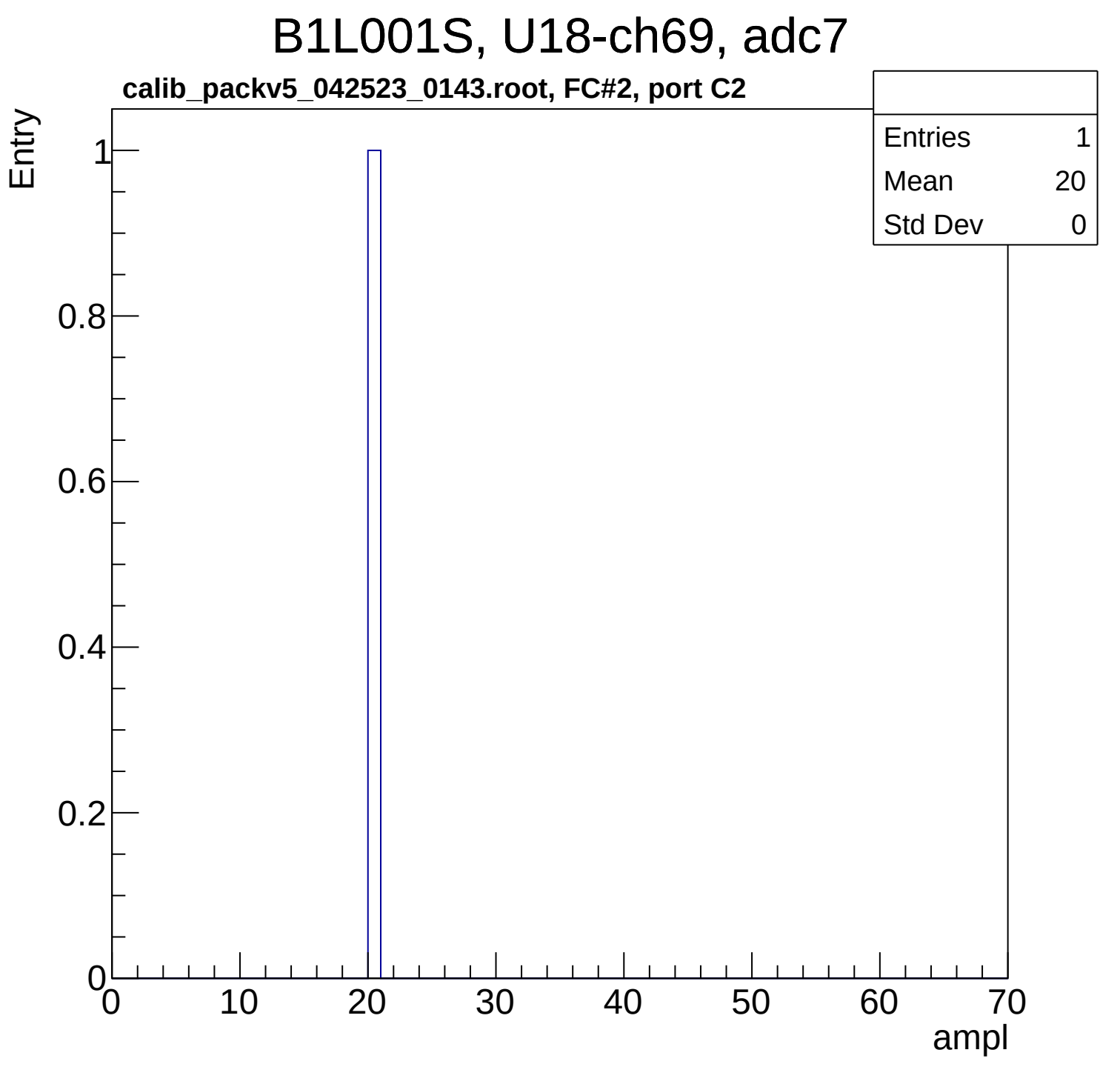

B1L001S, U18-ch69, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 137
Mean 41.68
Std Dev 3.61
Gaus mean : 42.3316
Gaus Width: 4.0642
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

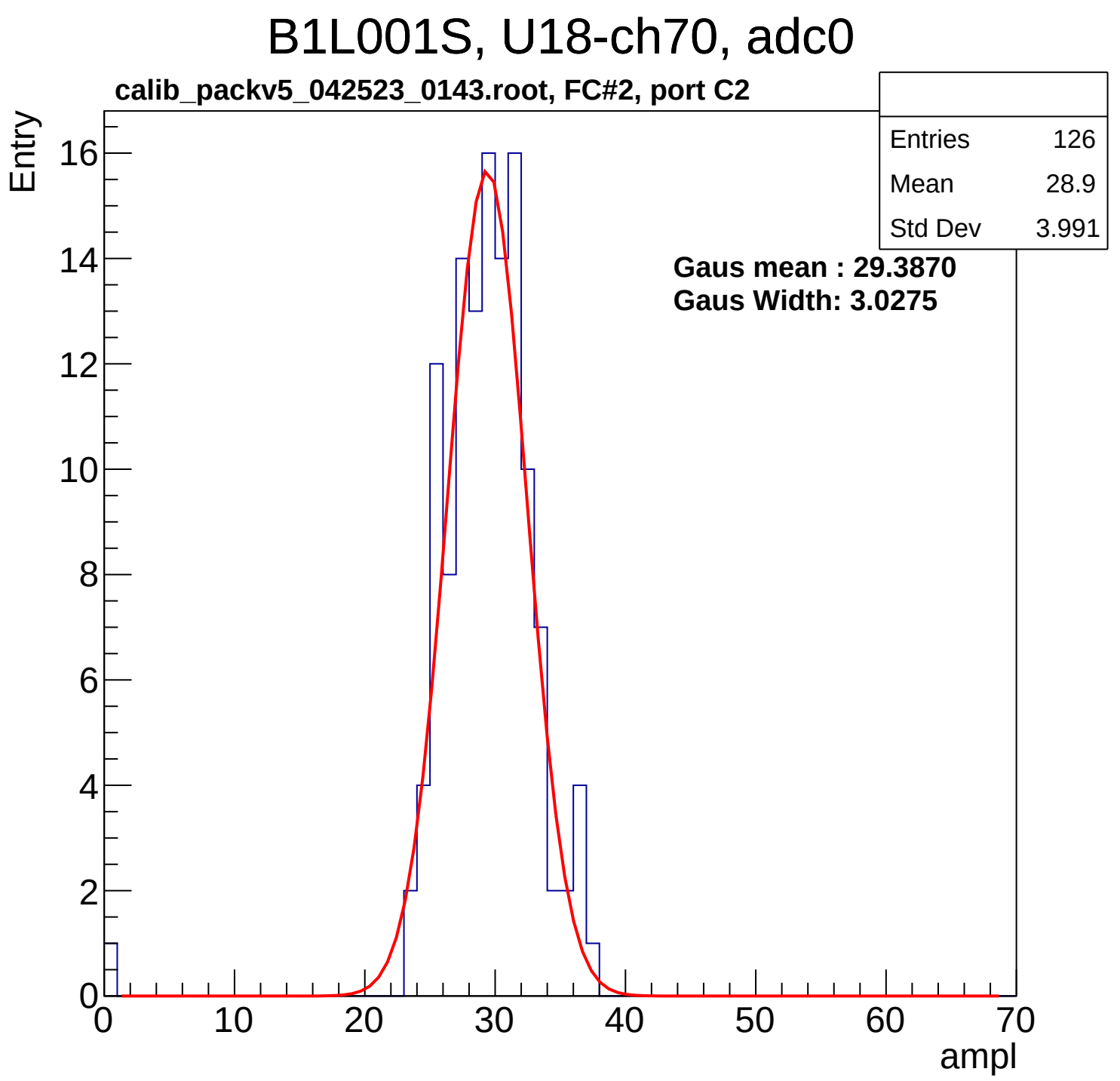

B1L001S, U18-ch69, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 102
Mean 47.68
Std Dev 3.729
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

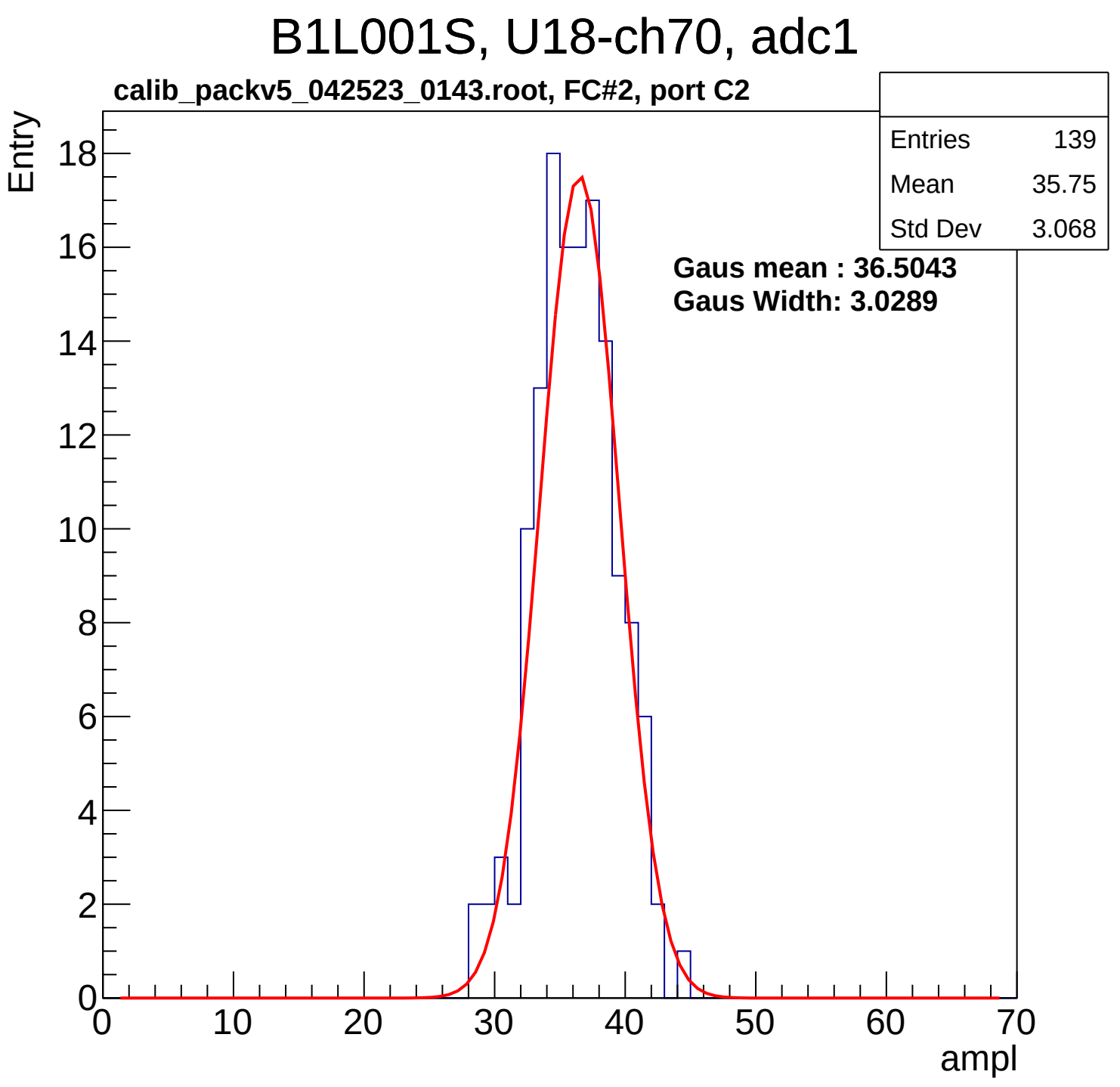

B1L001S, U18-ch69, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 170
Mean 54.46
Std Dev 3.669
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

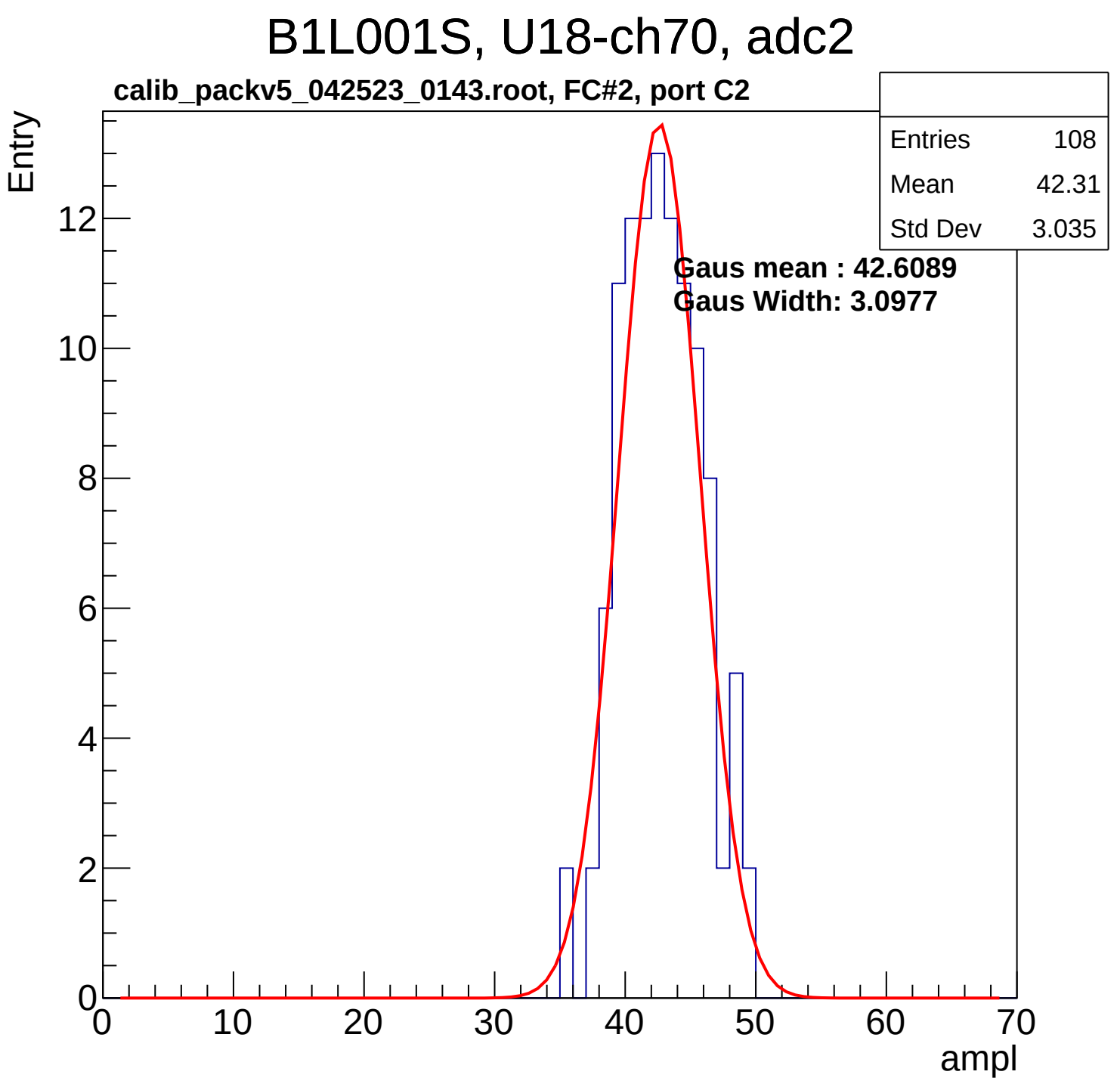

B1L001S, U18-ch69, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 81
Mean 59.23
Std Dev 7.136
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

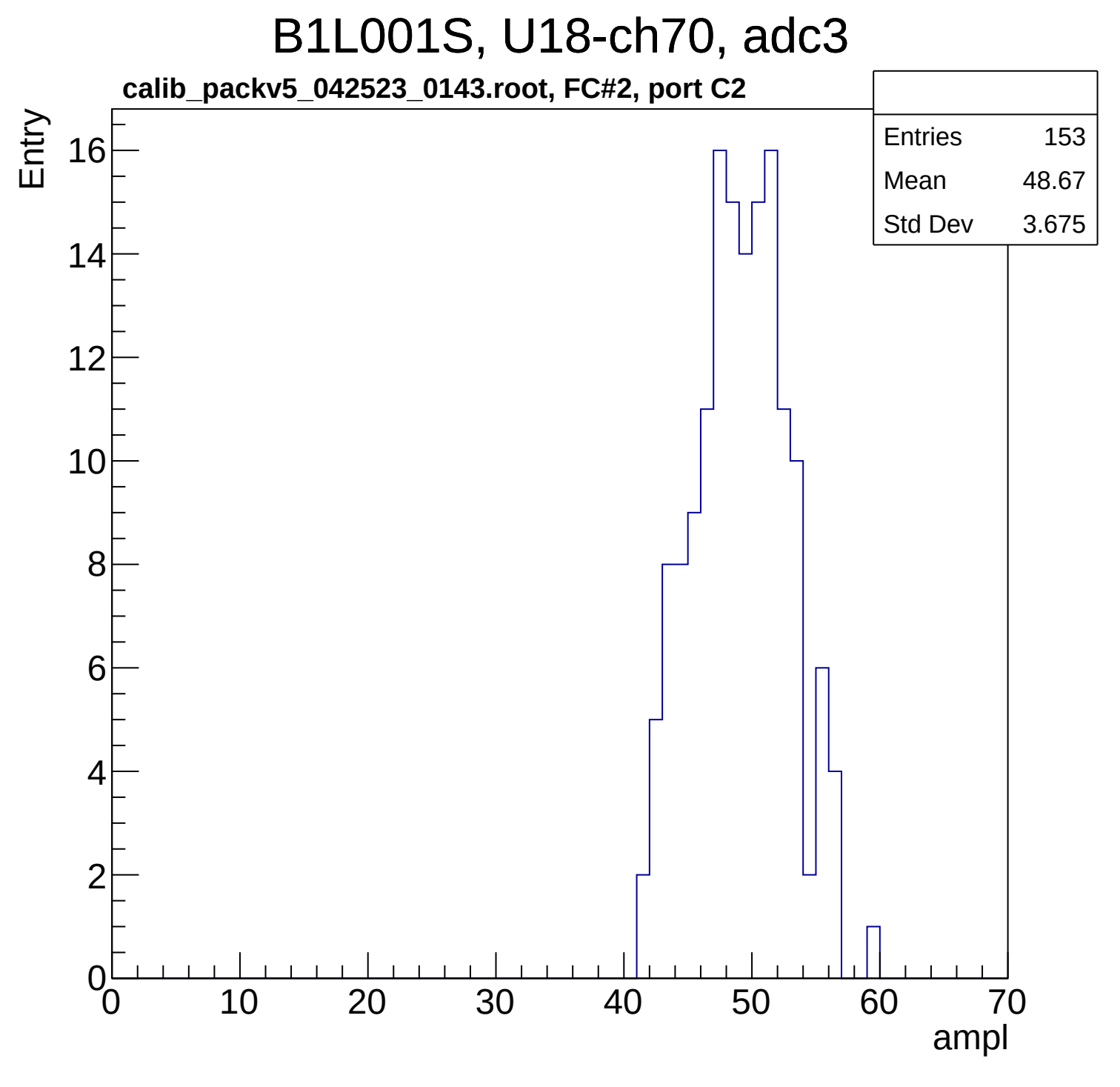

B1L001S, U18-ch69, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 16
Mean 57.5
Std Dev 14.95
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

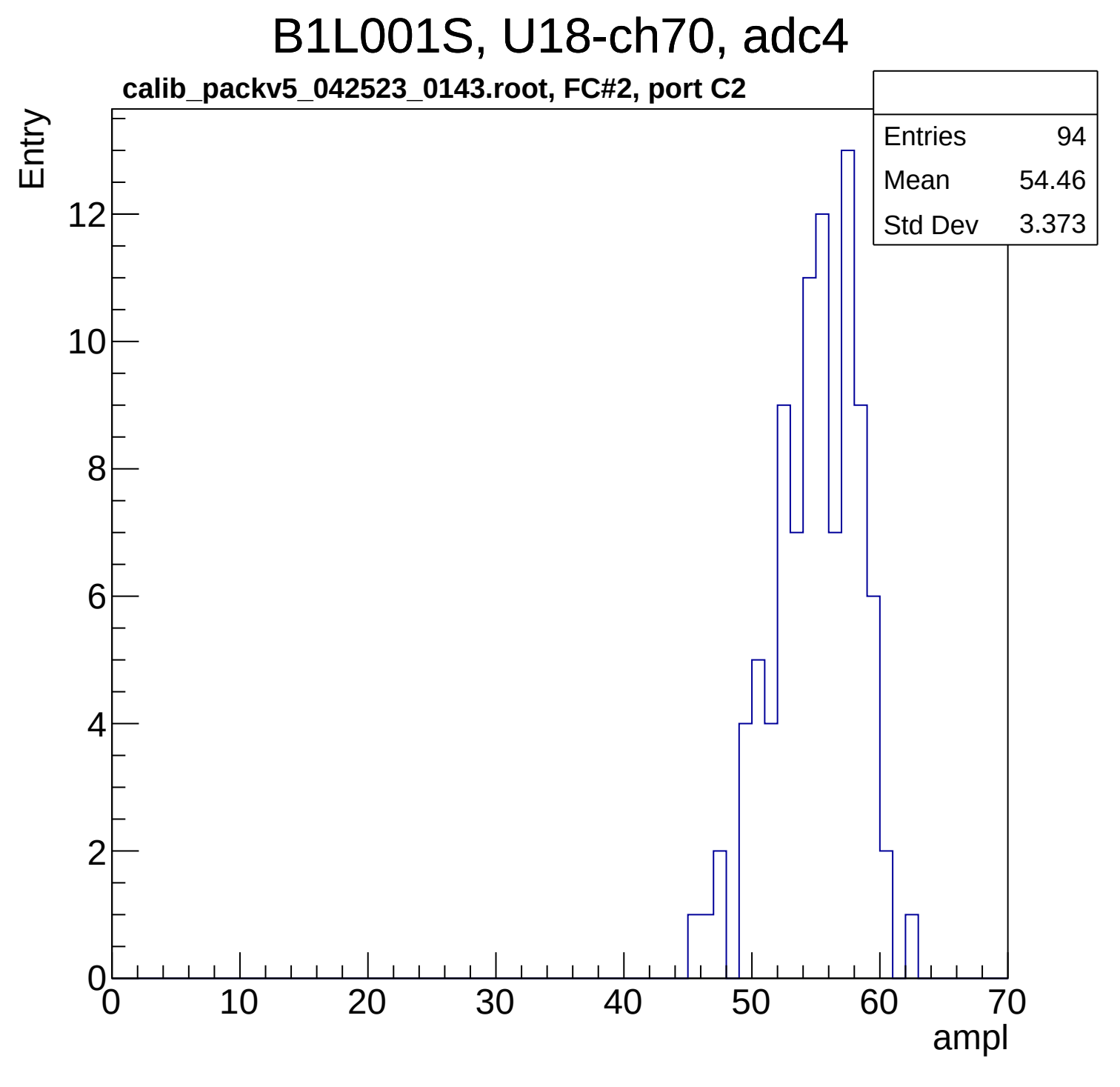

B1L001S, U18-ch69, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 20
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70

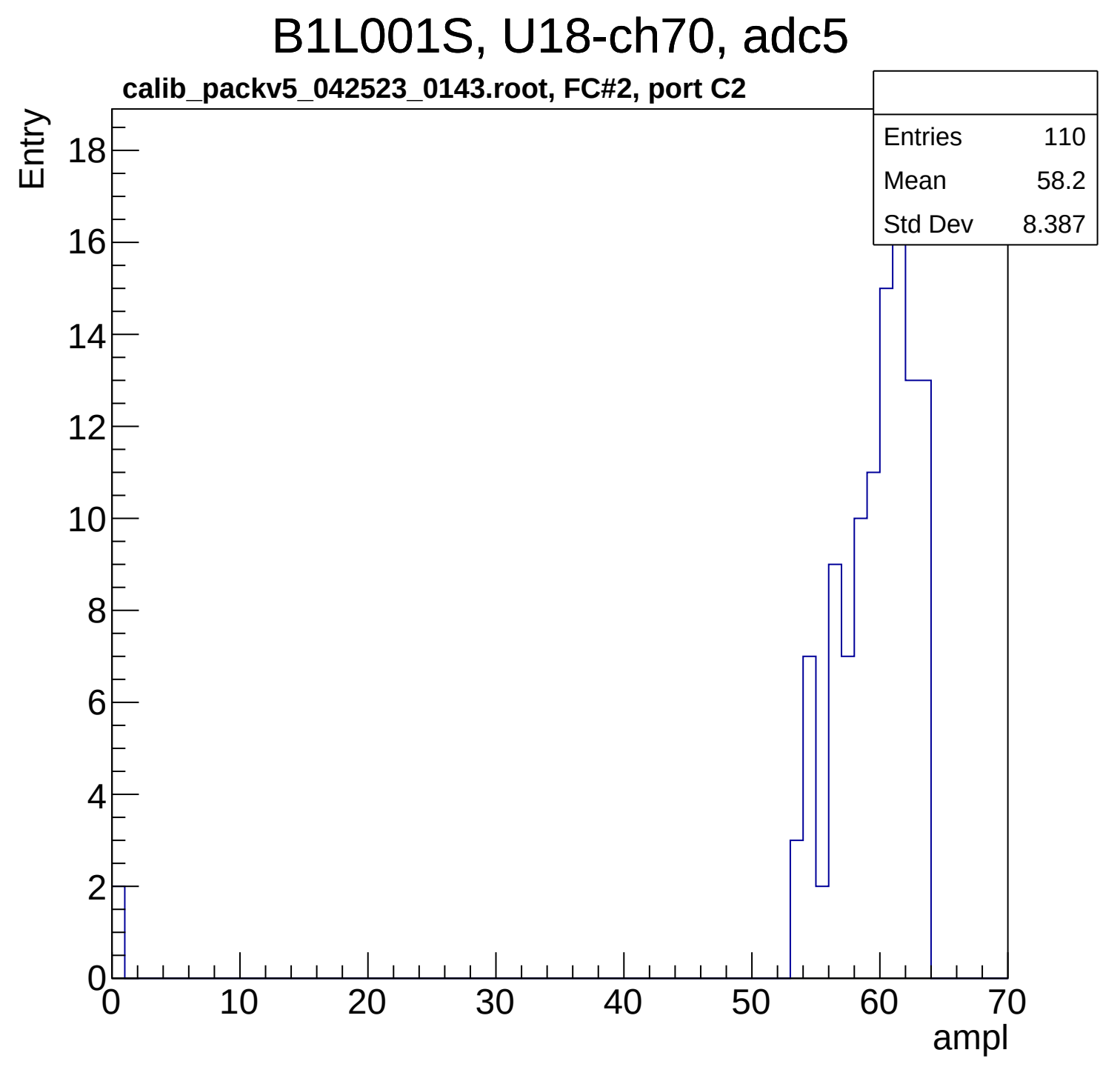

B1L001S, U18-ch70, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 126
Mean 28.9
Std Dev 3.991
Gaus mean : 29.3870
Gaus Width: 3.0275
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

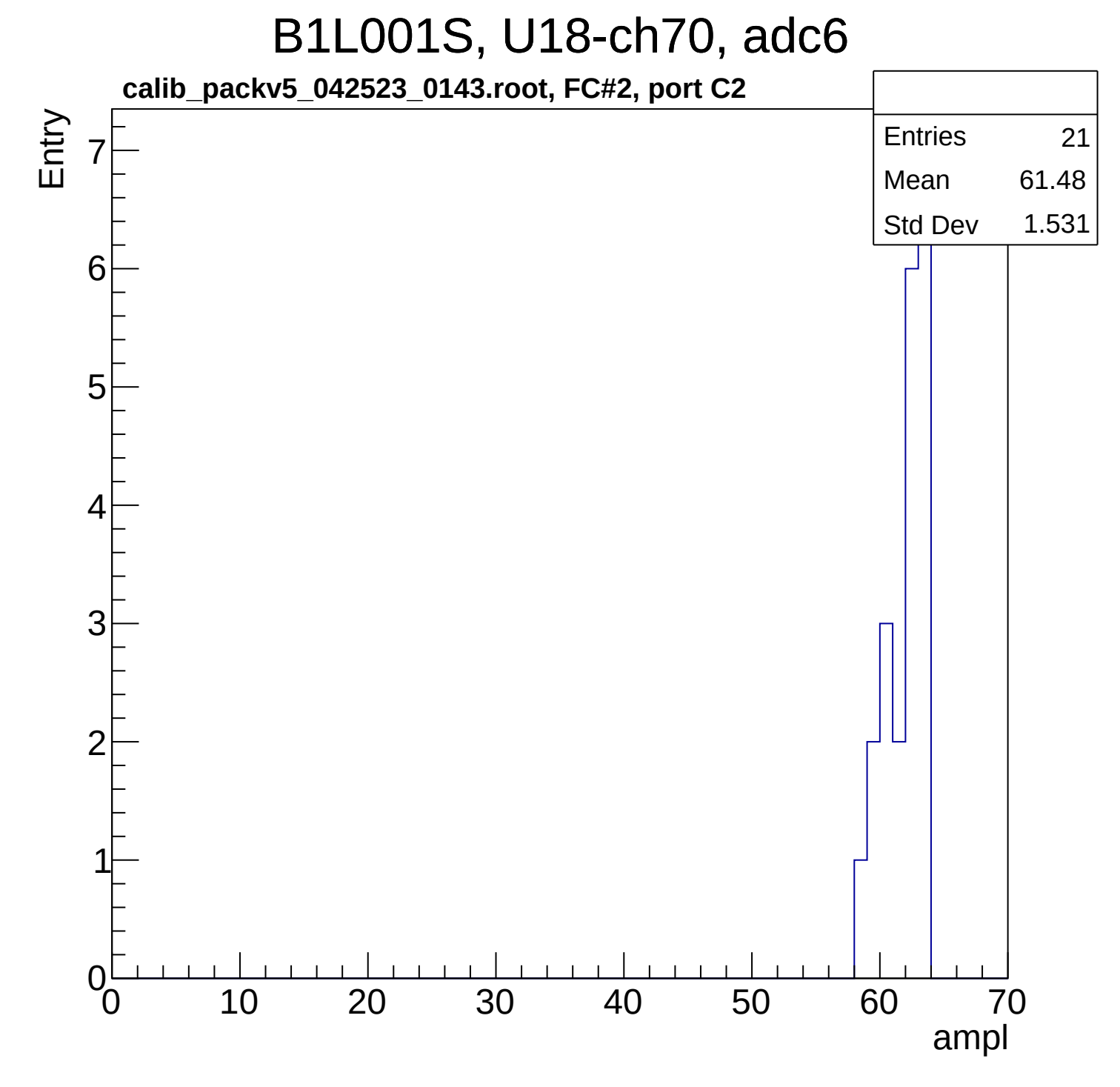

B1L001S, U18-ch70, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 139
Mean 35.75
Std Dev 3.068
Gaus mean : 36.5043
Gaus Width: 3.0289
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

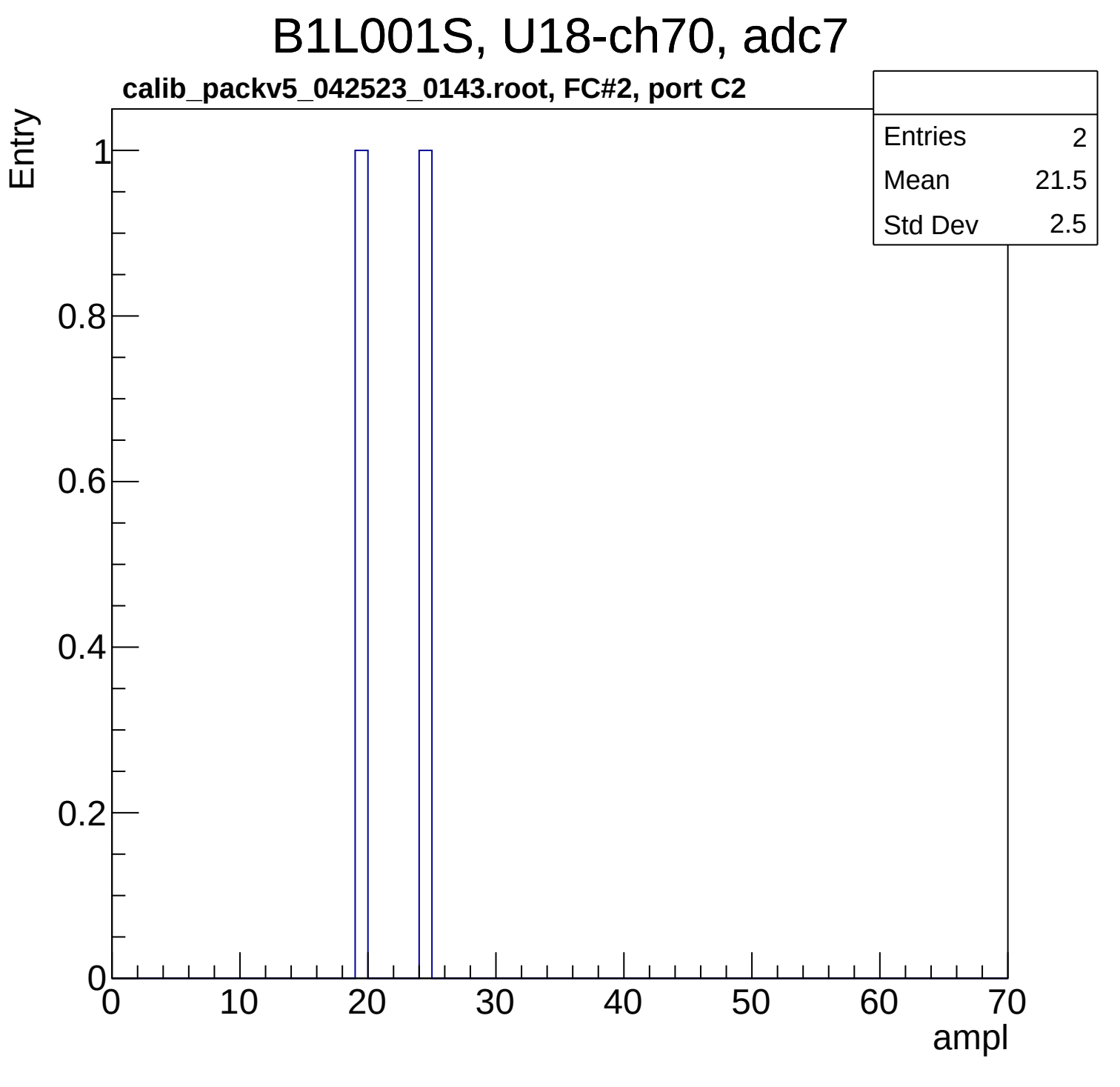

B1L001S, U18-ch70, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 108
Mean 42.31
Std Dev 3.035
Gaus mean : 42.6089
Gaus Width: 3.0977
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70

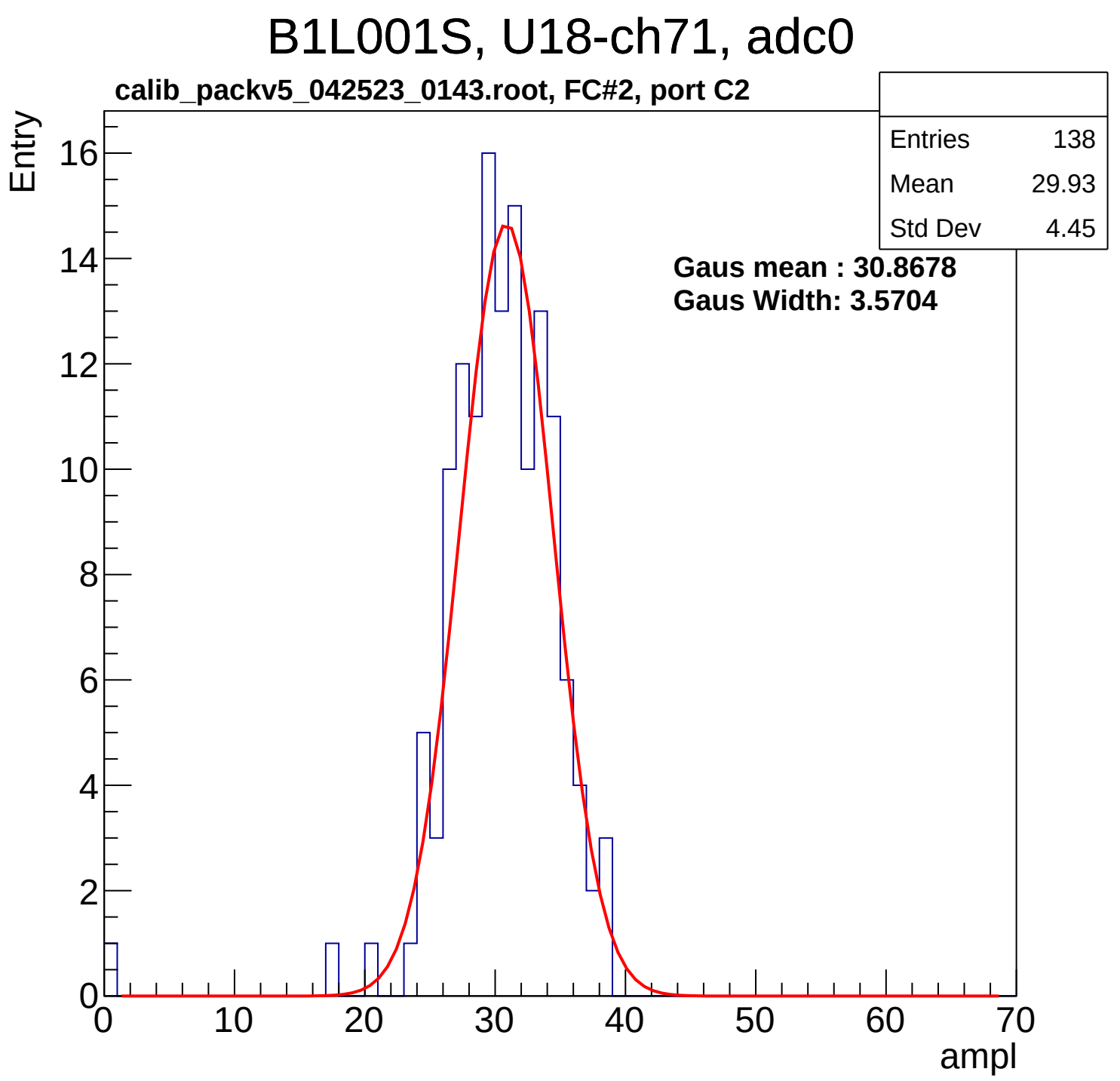

B1L001S, U18-ch70, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 153
Mean 48.67
Std Dev 3.675
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

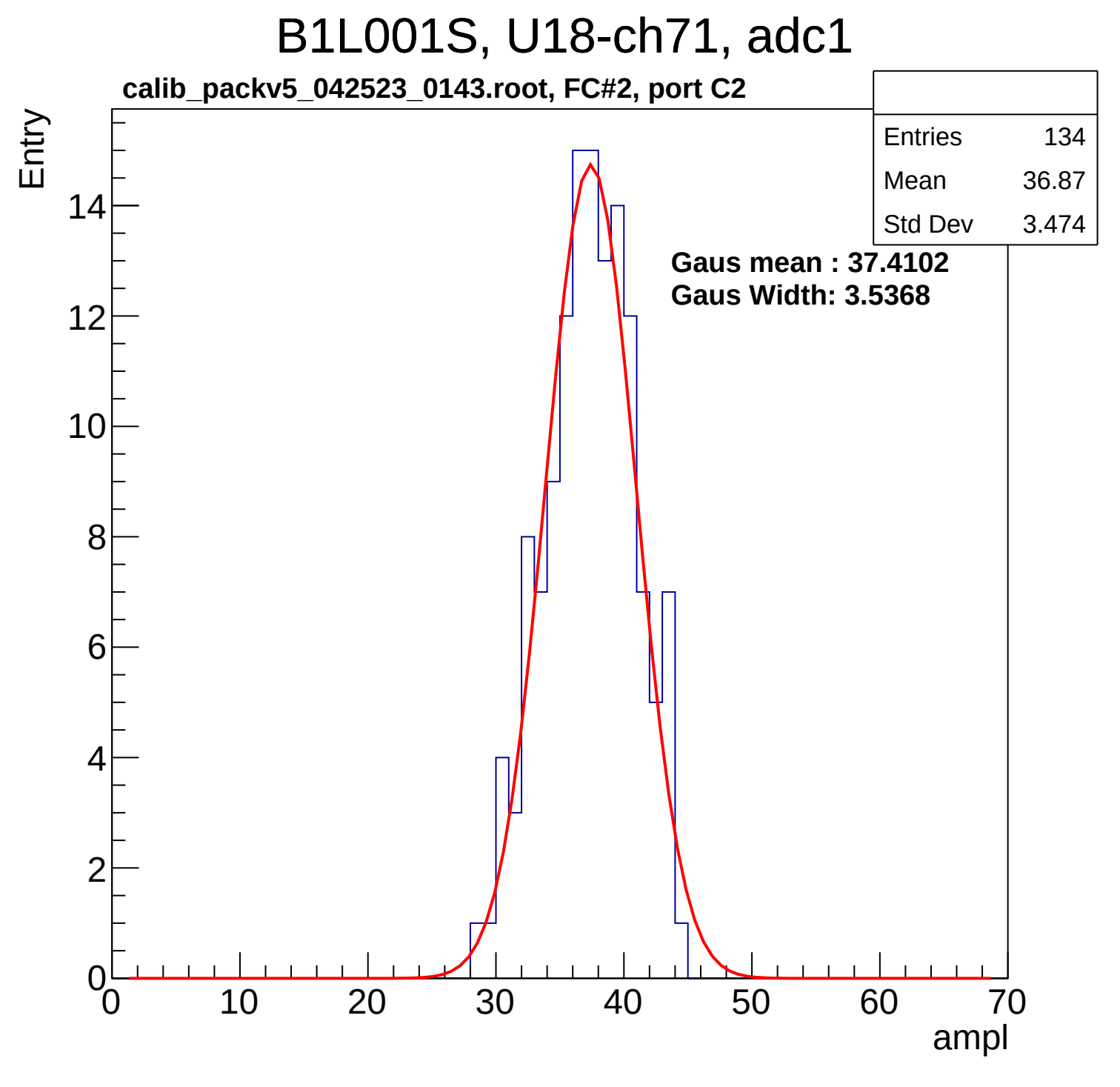

B1L001S, U18-ch70, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 94
Mean 54.46
Std Dev 3.373
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70

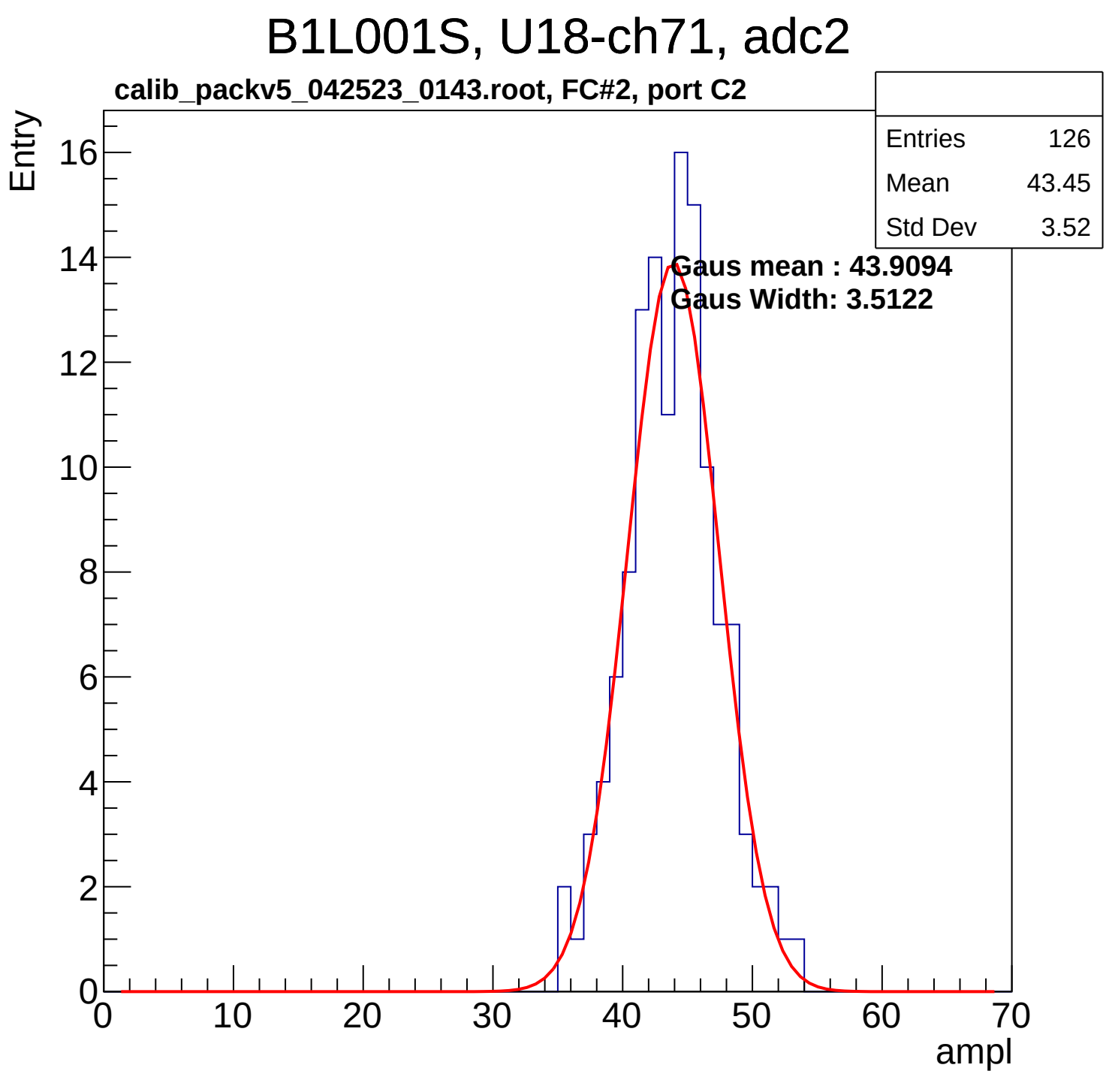

B1L001S, U18-ch70, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 110
Mean 58.2
Std Dev 8.387
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

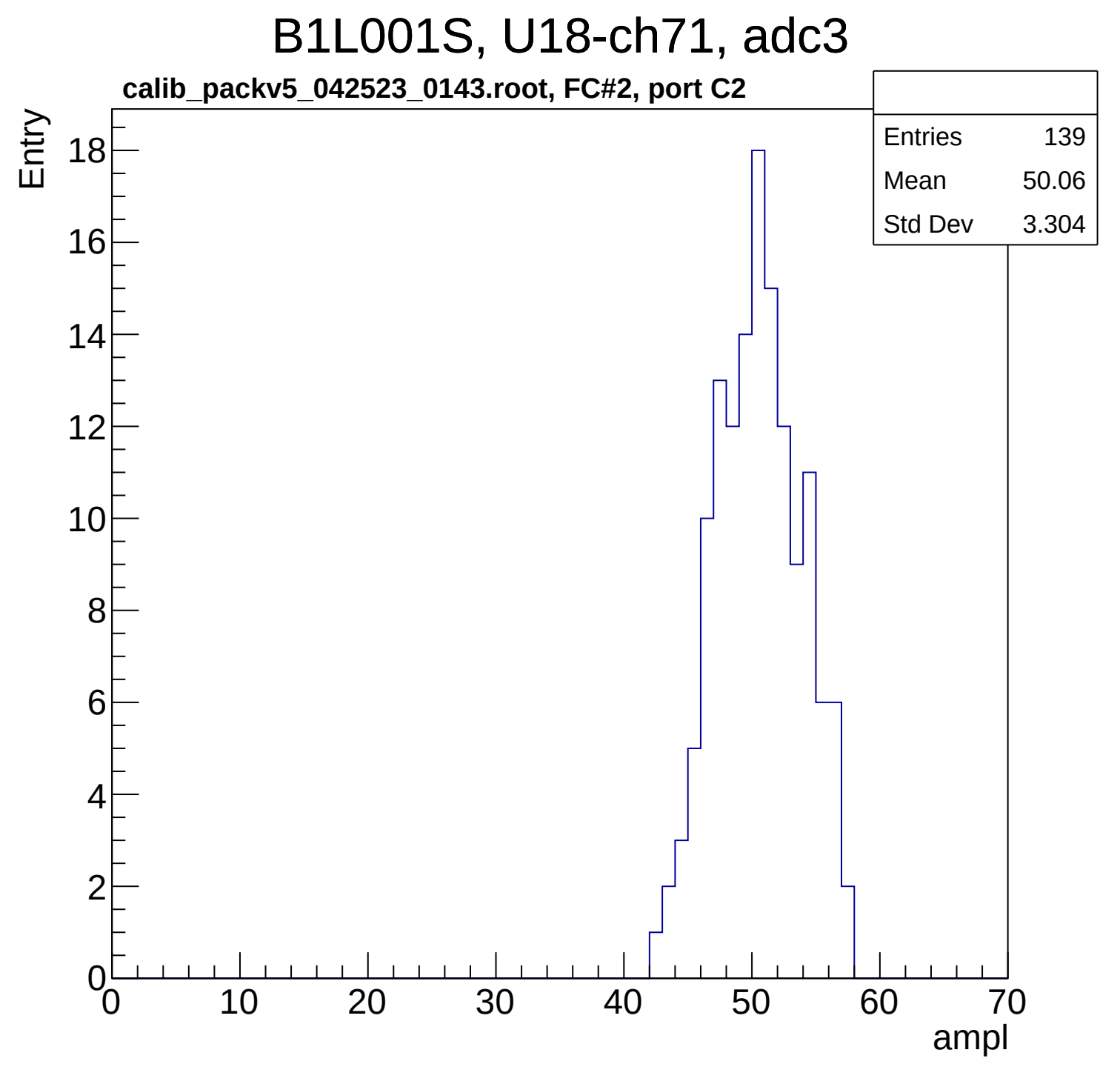

B1L001S, U18-ch70, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 21
Mean 61.48
Std Dev 1.531
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

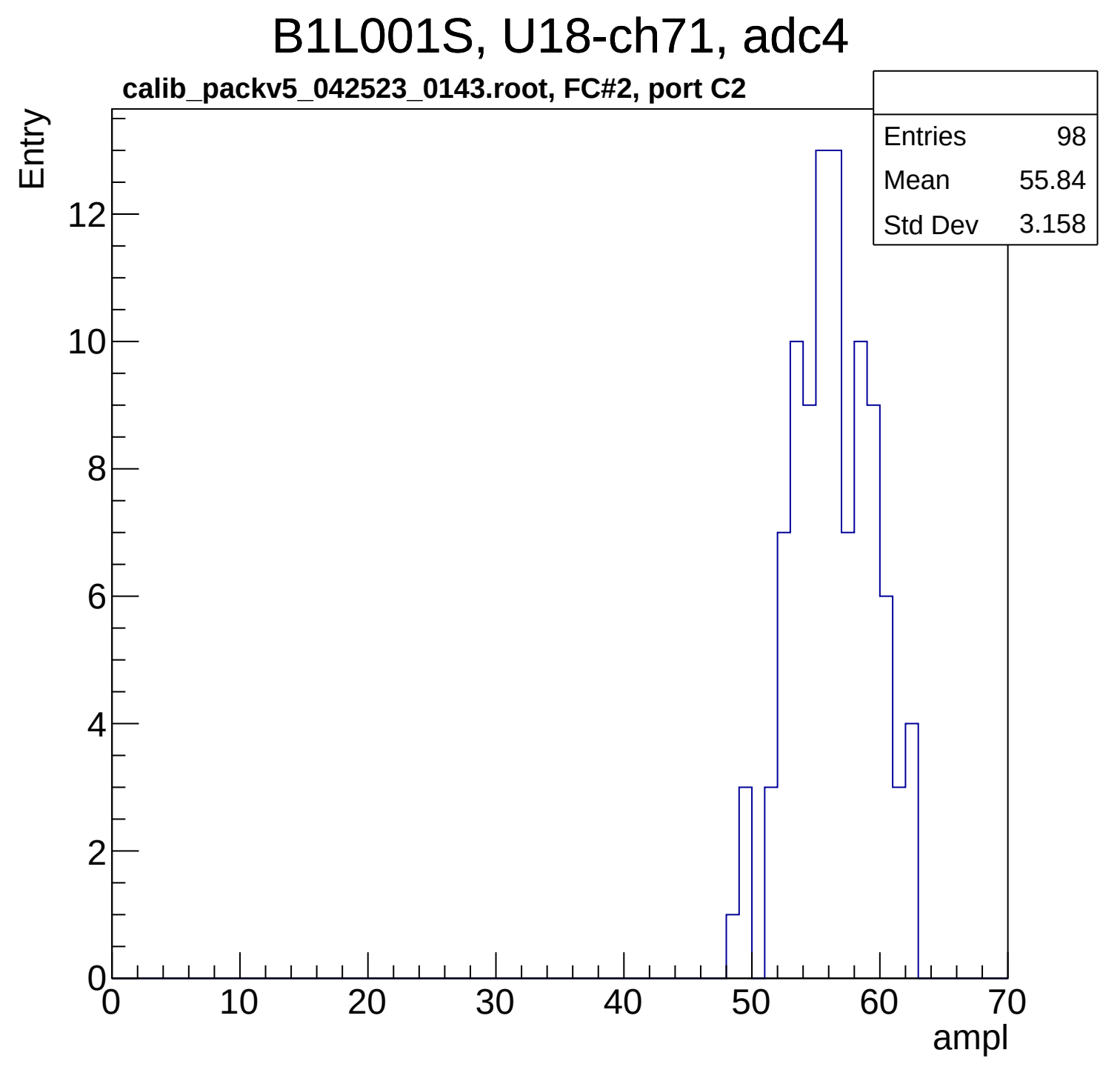

B1L001S, U18-ch70, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 21.5
Std Dev 2.5
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70

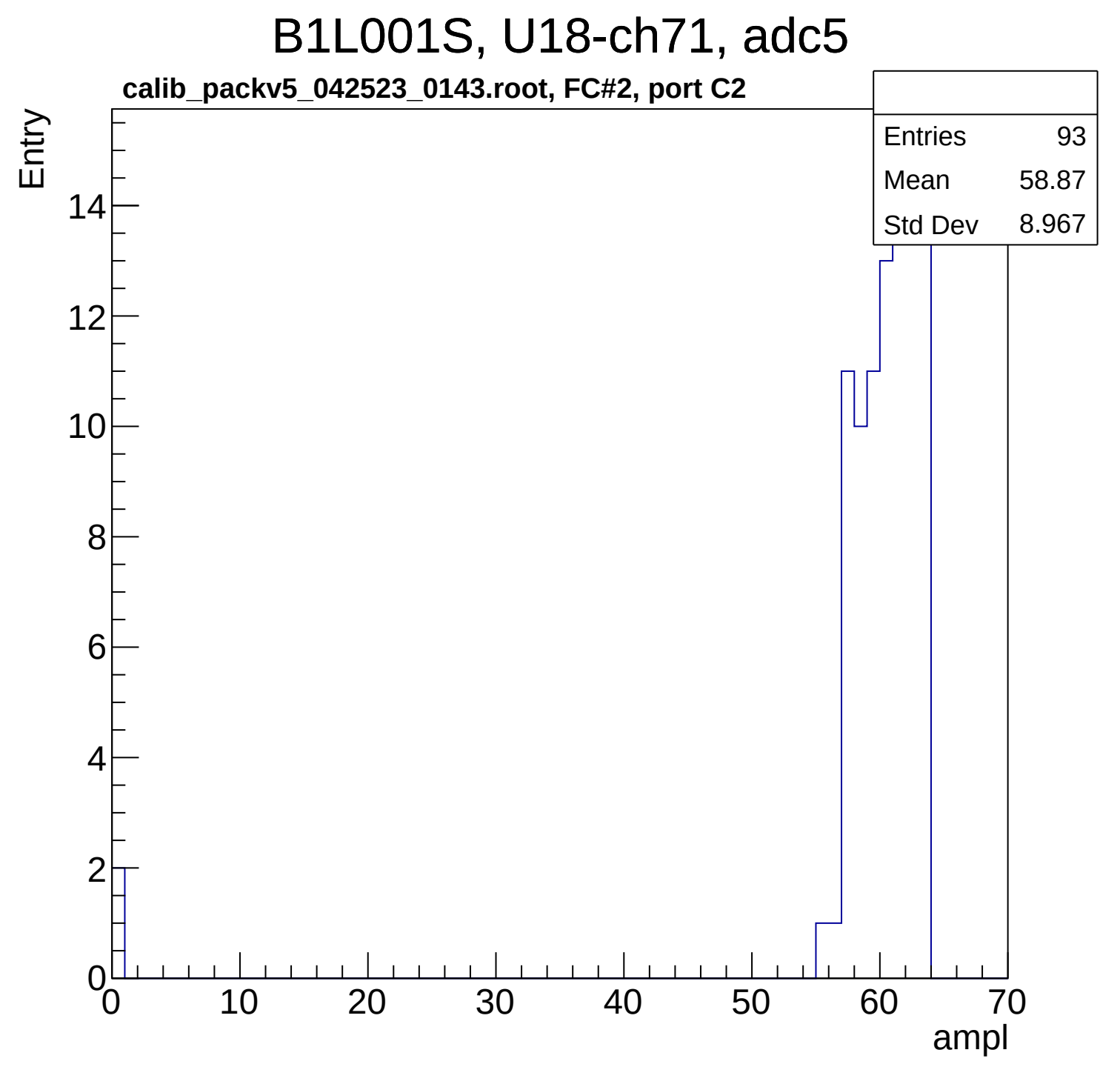

B1L001S, U18-ch71, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 138
Mean 29.93
Std Dev 4.45
Gaus mean : 30.8678
Gaus Width: 3.5704
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

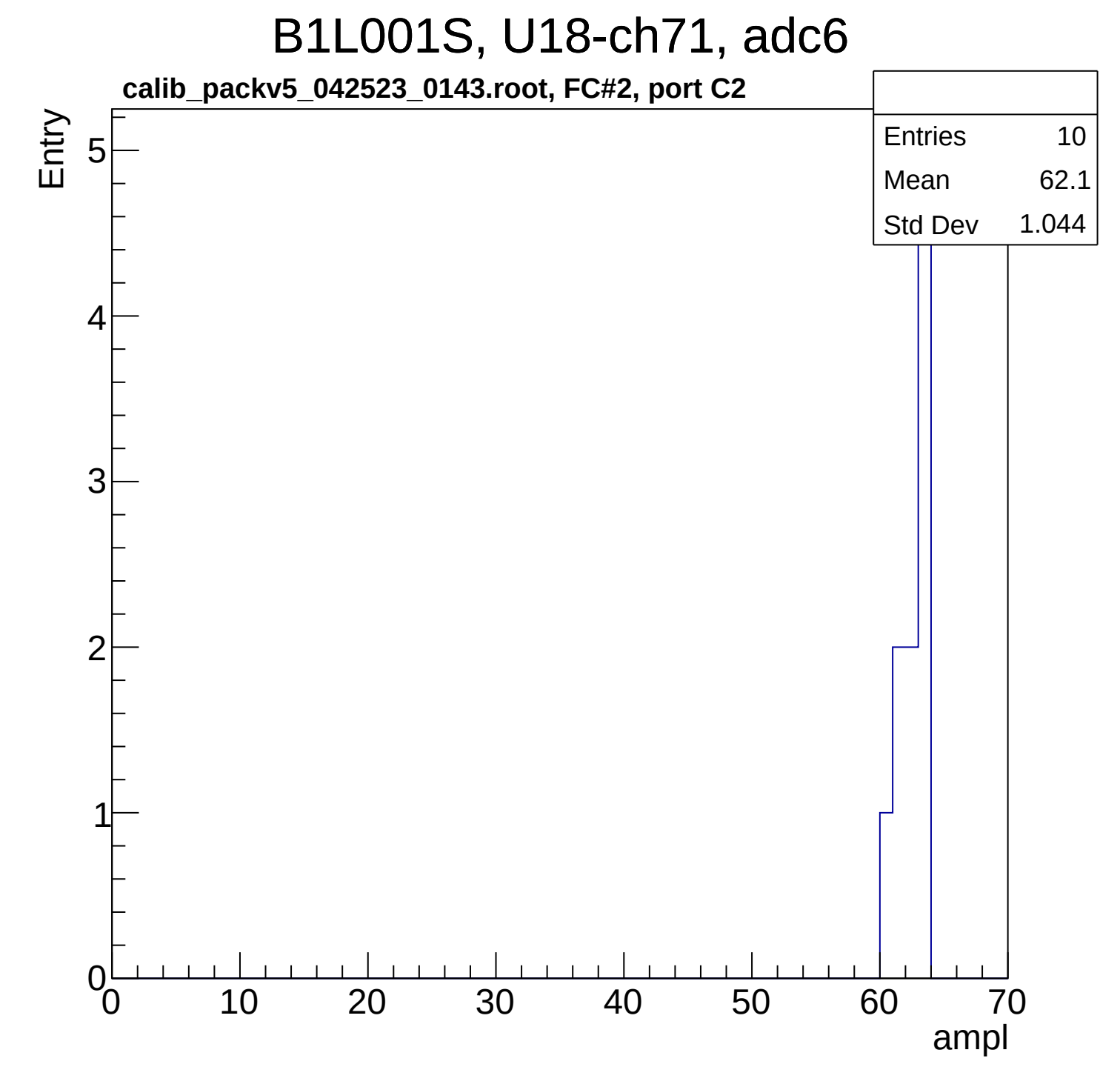

B1L001S, U18-ch71, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 134
Mean 36.87
Std Dev 3.474
Gaus mean : 37.4102
Gaus Width: 3.5368
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

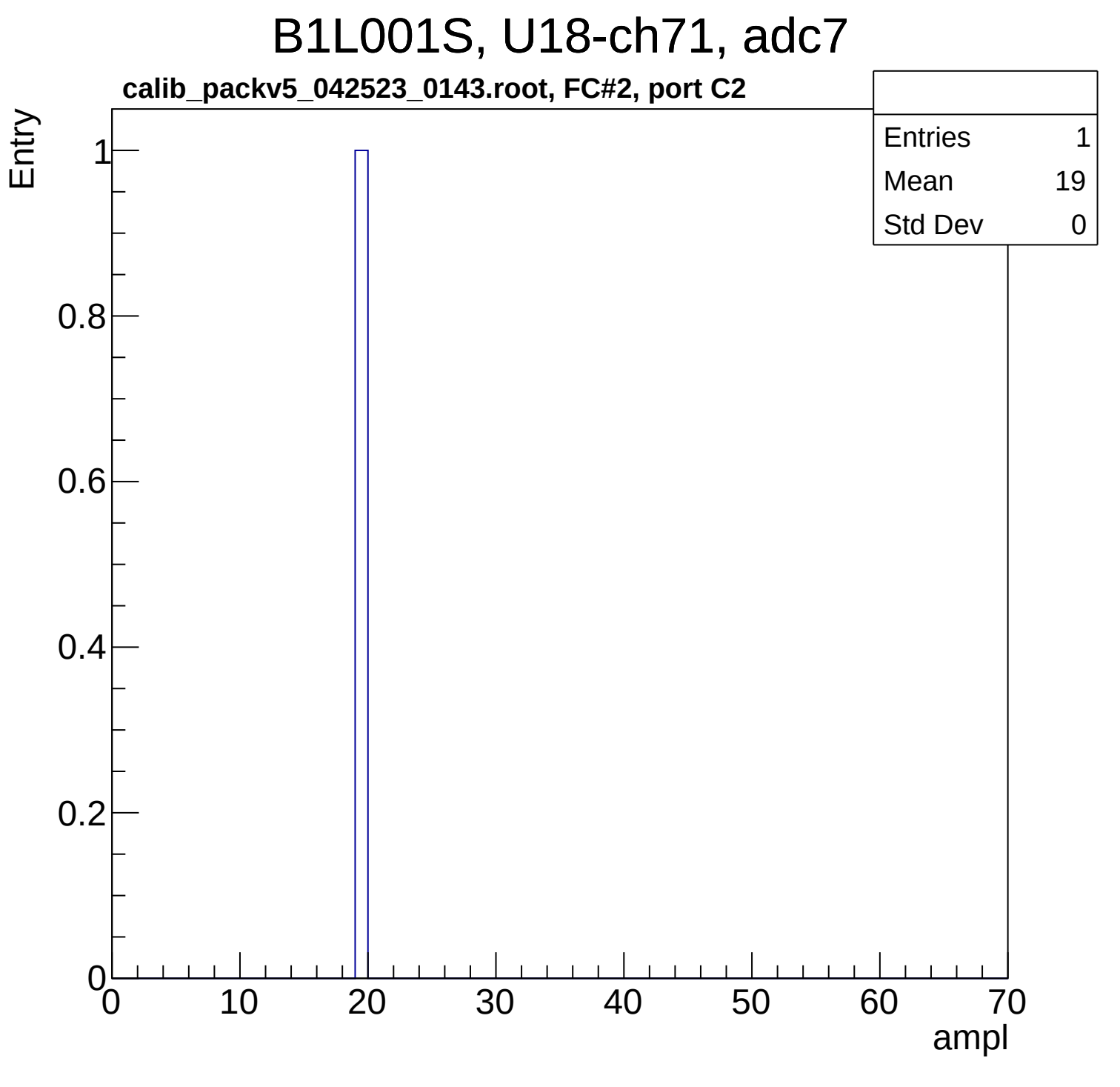

B1L001S, U18-ch71, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 126
Mean 43.45
Std Dev 3.52
Gaus mean : 43.9094
Gaus Width: 3.5122
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

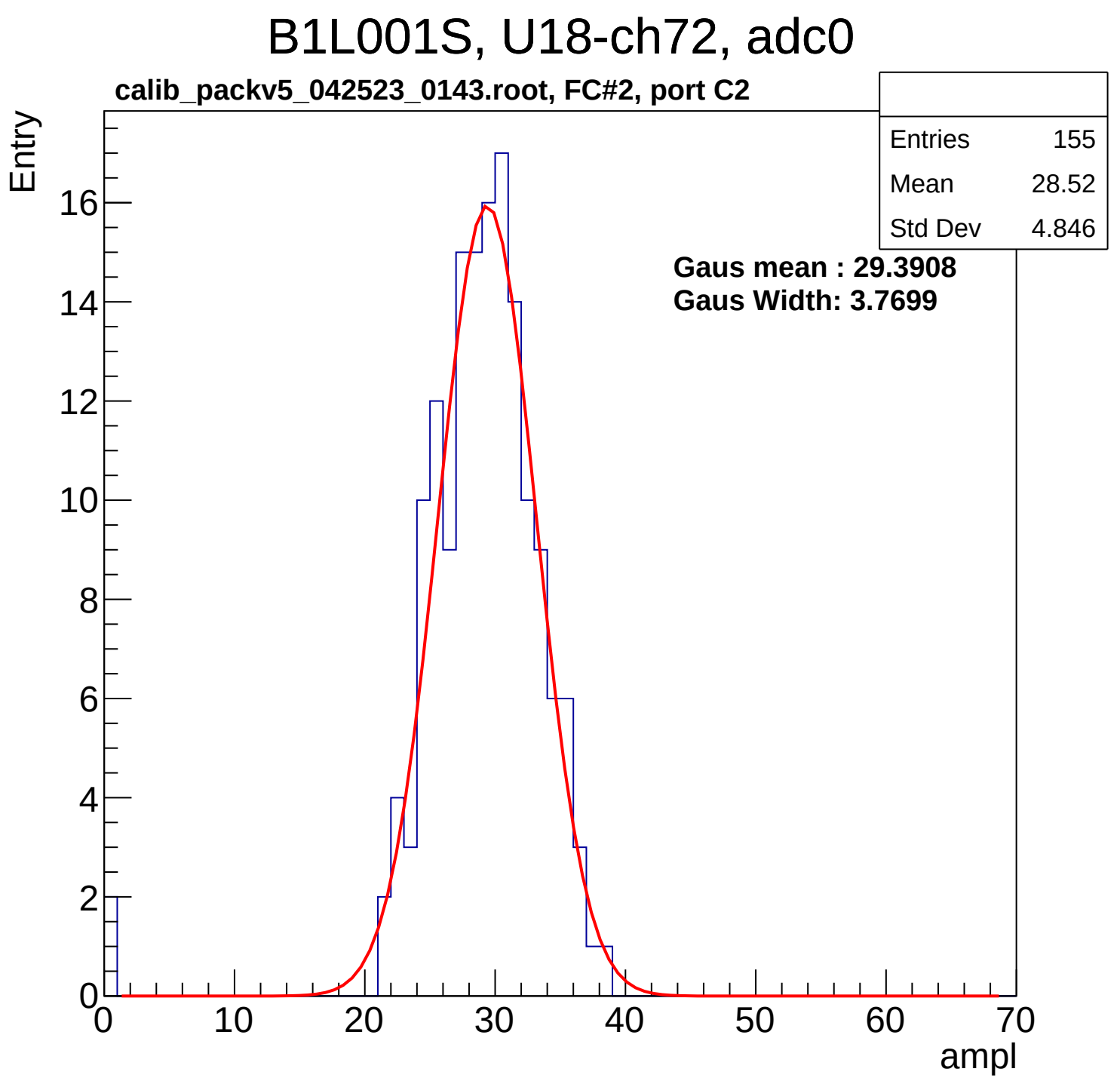

B1L001S, U18-ch71, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 139
Mean 50.06
Std Dev 3.304
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

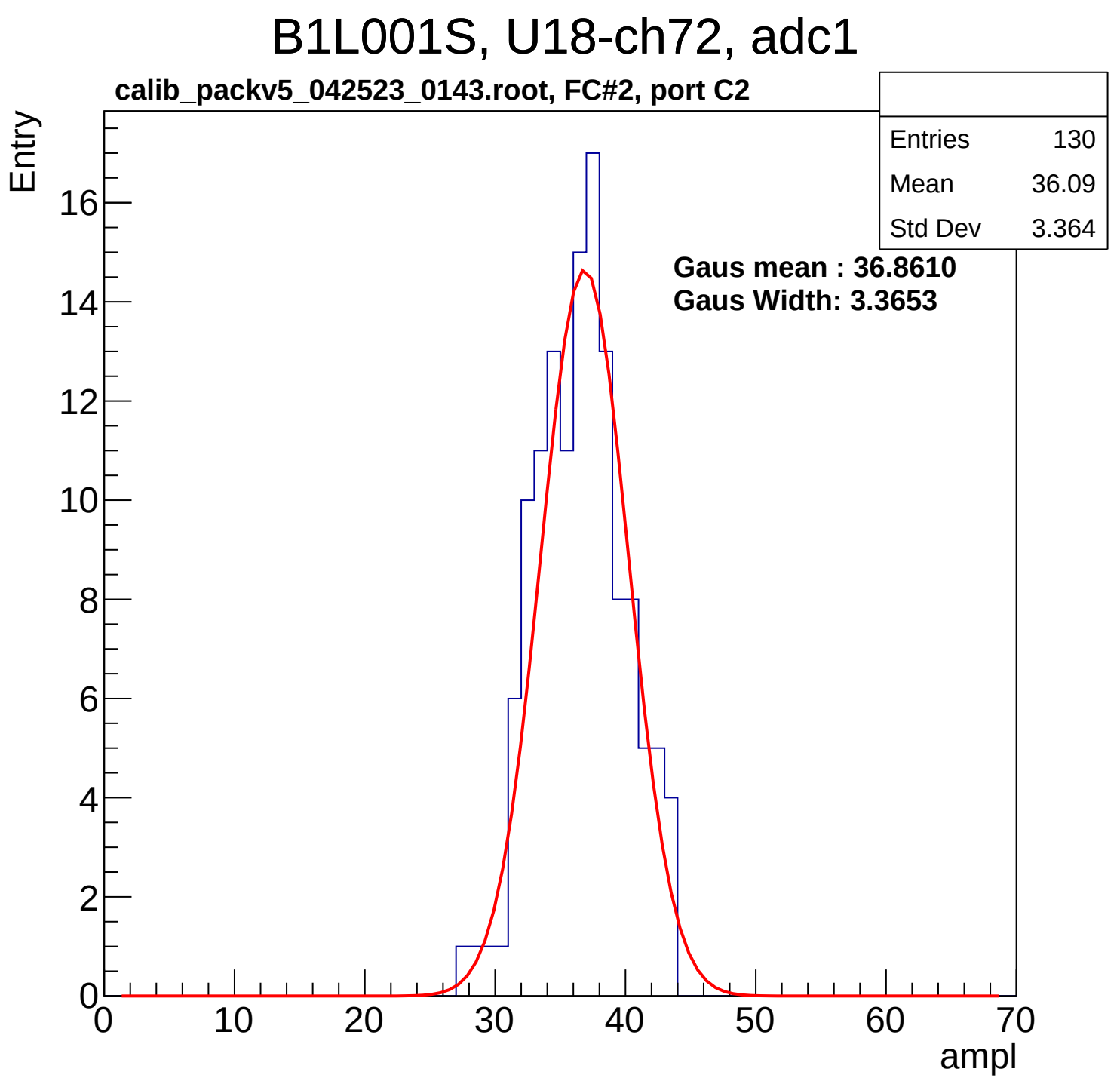

B1L001S, U18-ch71, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 98
Mean 55.84
Std Dev 3.158
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl

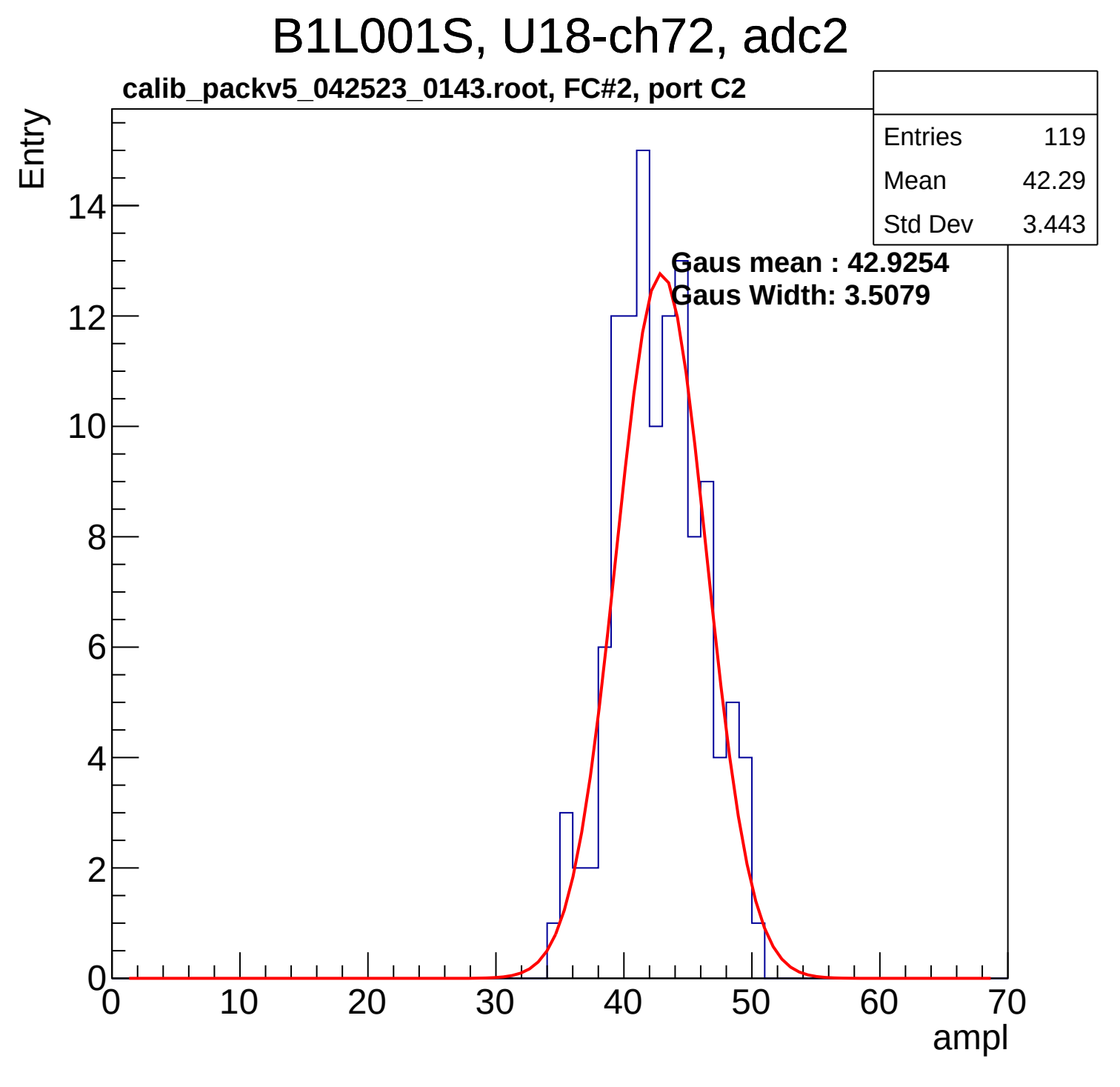

B1L001S, U18-ch71, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 93
Mean 58.87
Std Dev 8.967
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

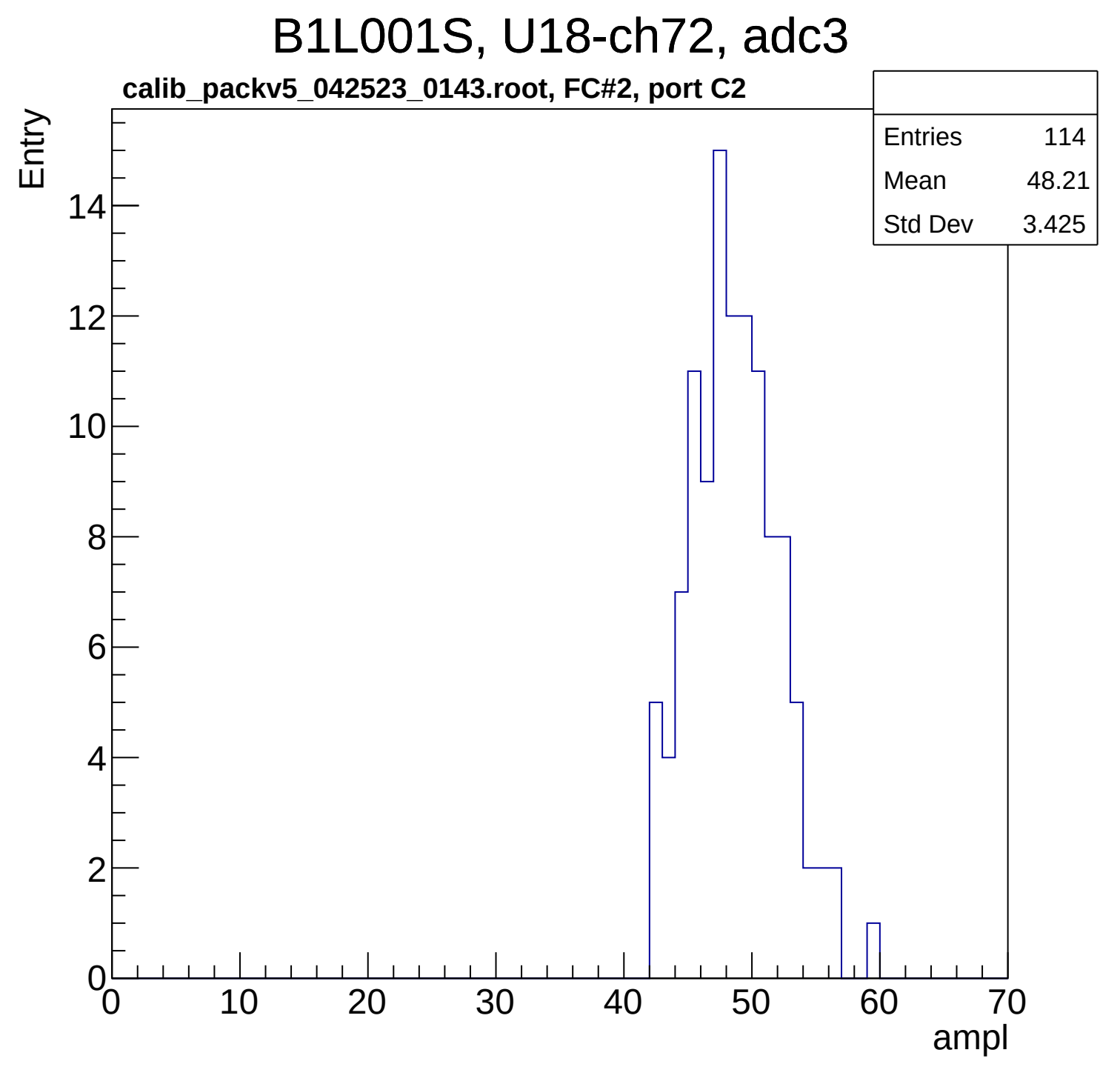

B1L001S, U18-ch71, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 10
Mean 62.1
Std Dev 1.044
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

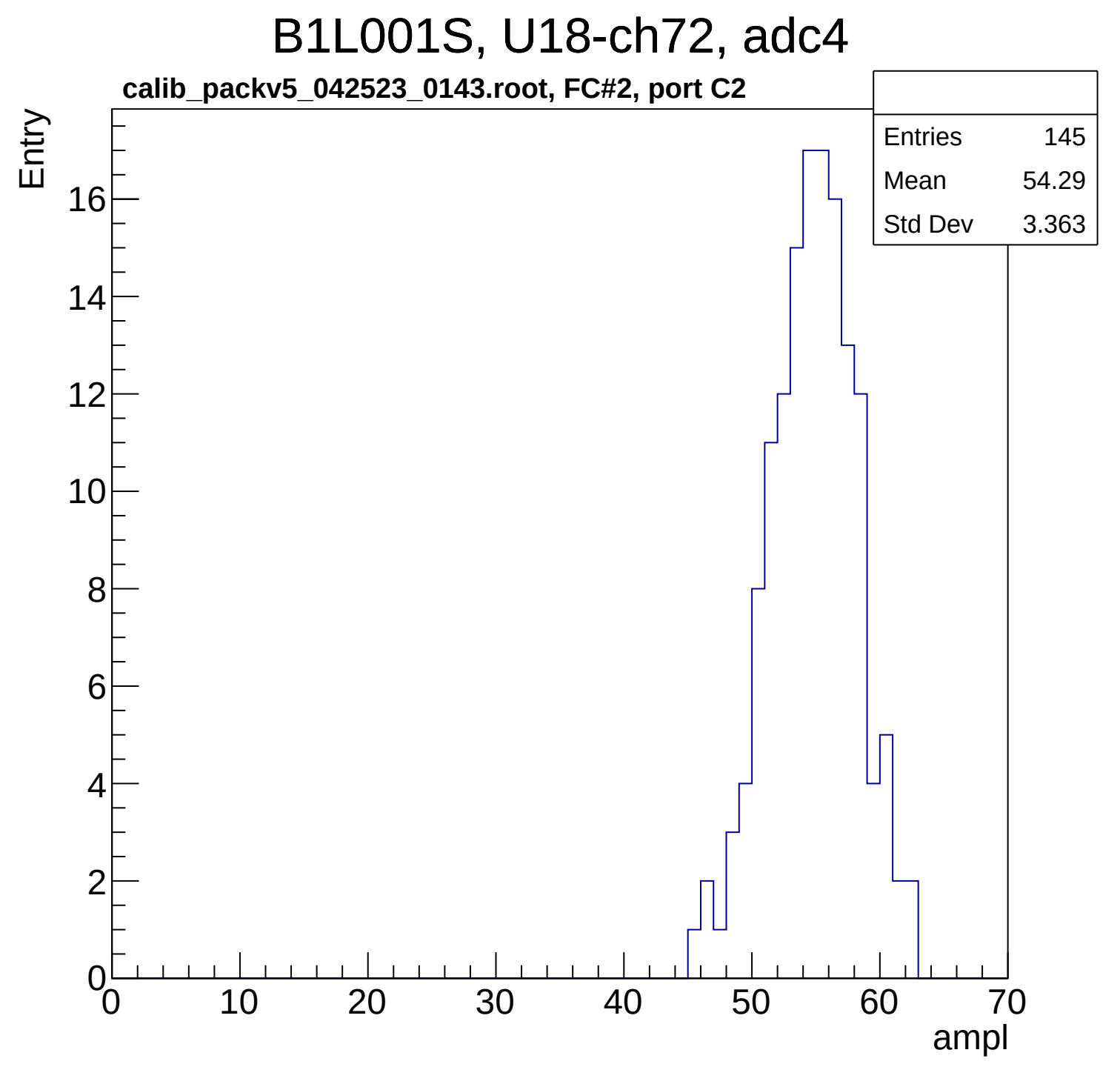

B1L001S, U18-ch71, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 19
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70

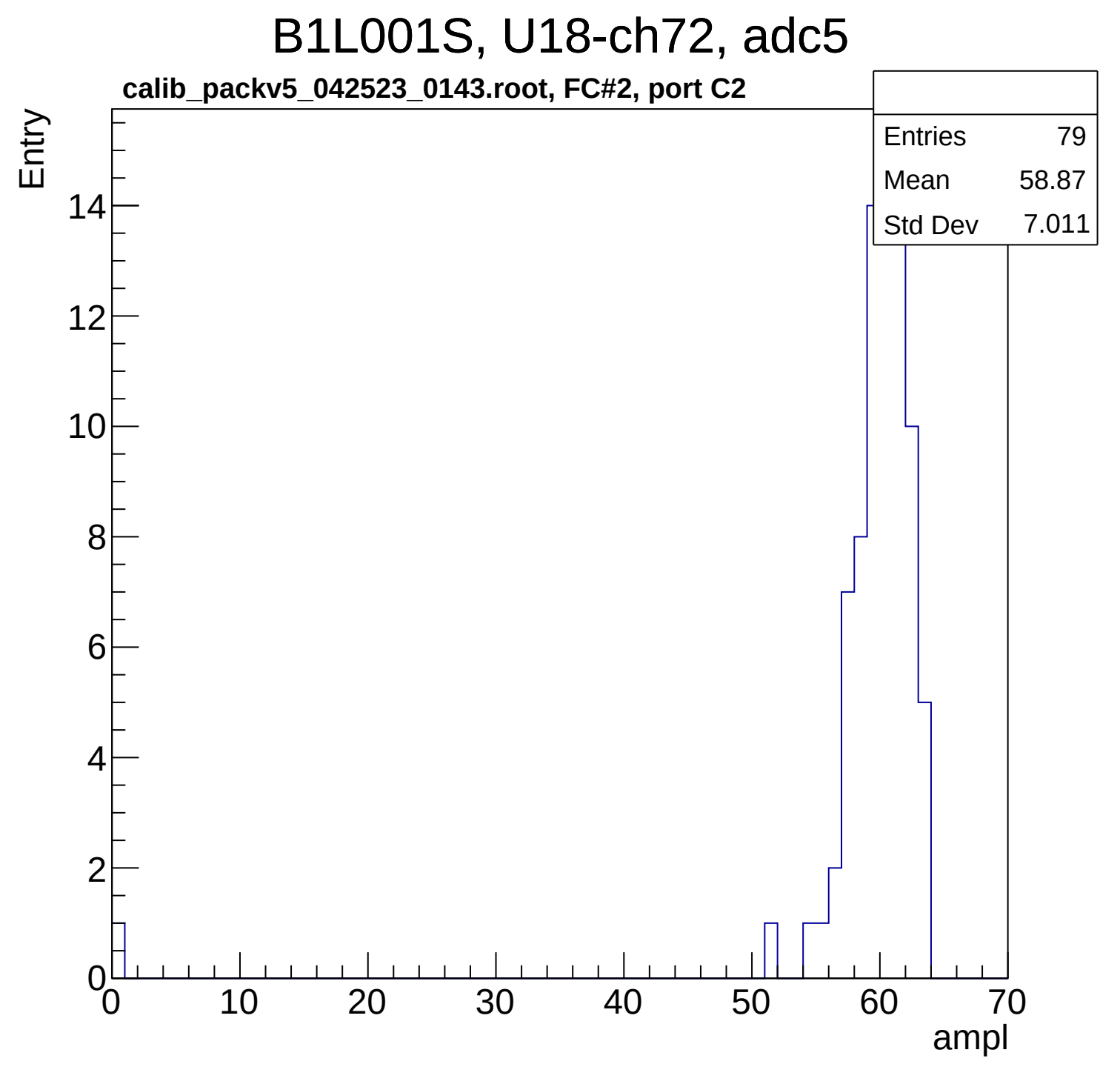

B1L001S, U18-ch72, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 155
Mean 28.52
Std Dev 4.846
Gaus mean : 29.3908
Gaus Width: 3.7699
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

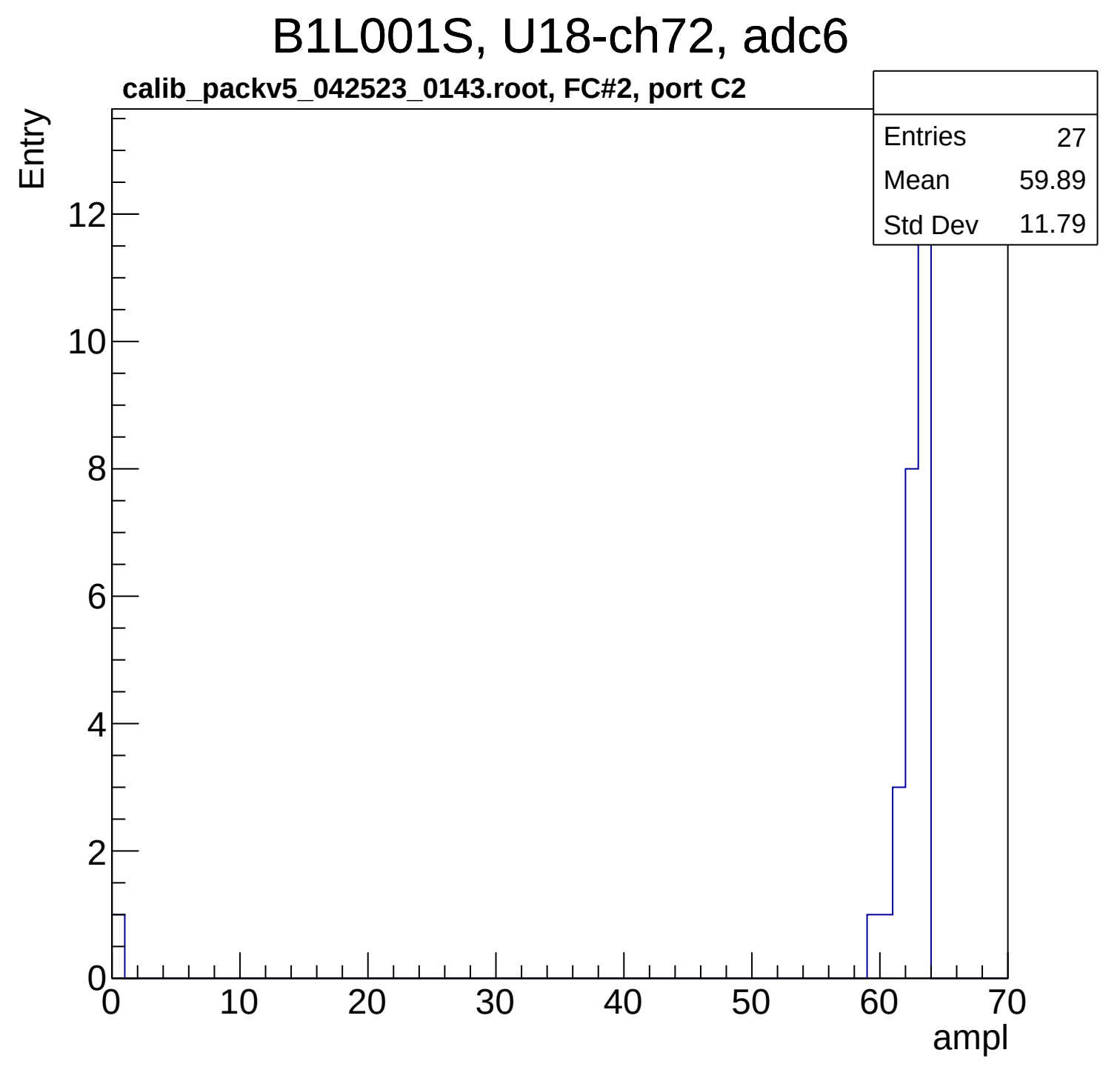

B1L001S, U18-ch72, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 130
Mean 36.09
Std Dev 3.364
Gaus mean : 36.8610
Gaus Width: 3.3653
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

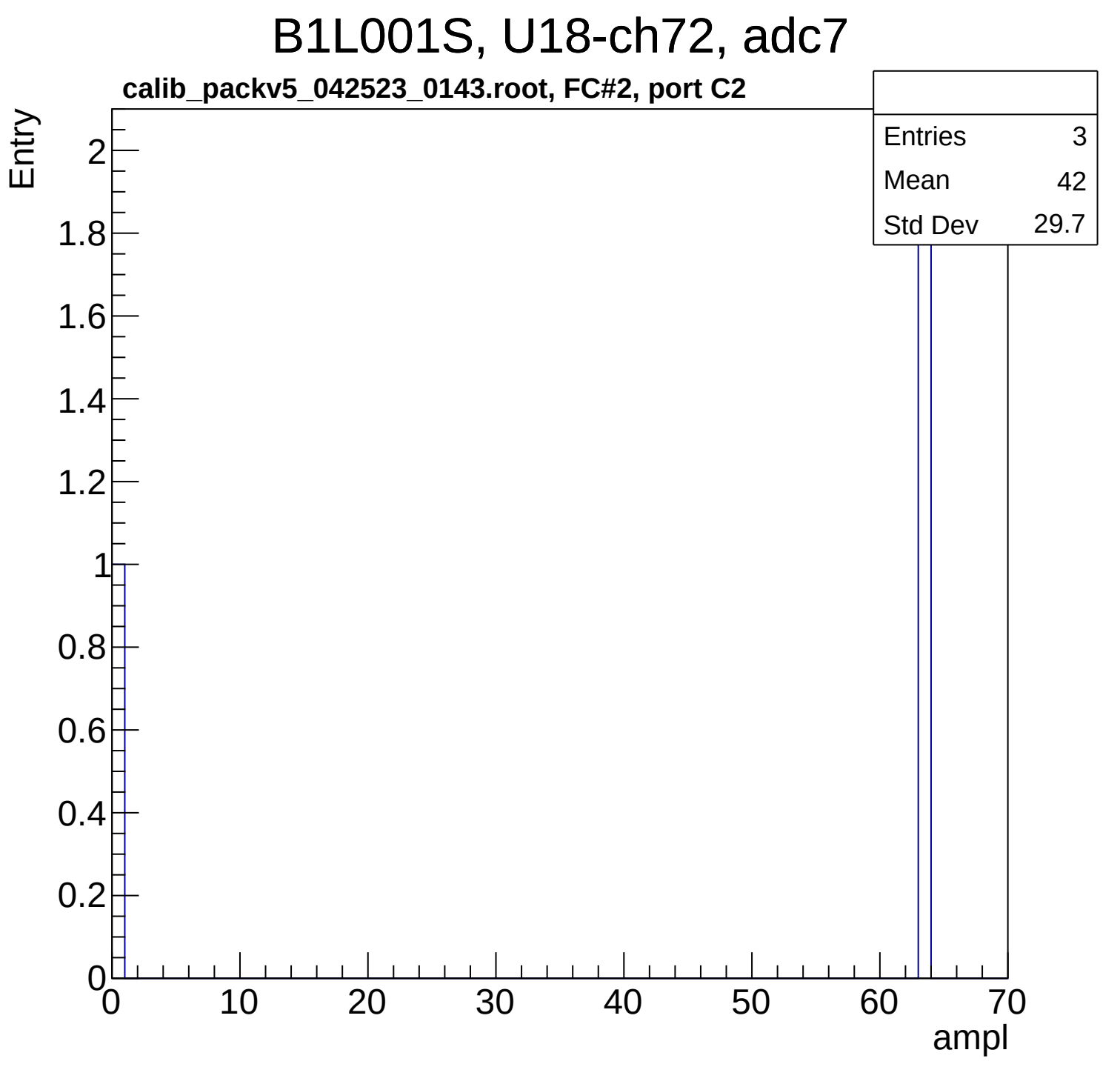

B1L001S, U18-ch72, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 119
Mean 42.29
Std Dev 3.443
Gaus mean : 42.9254
Gaus Width: 3.5079
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

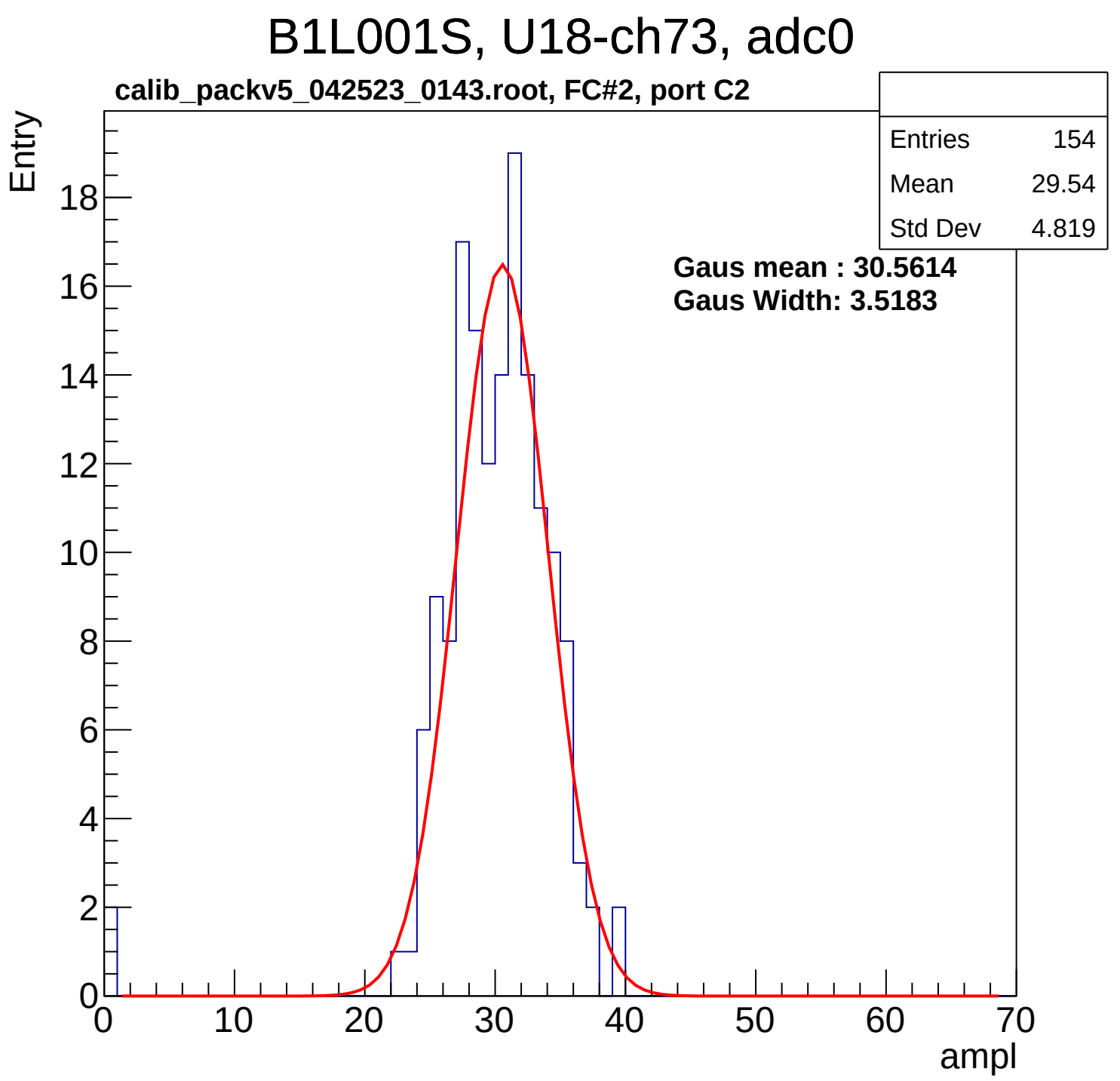

B1L001S, U18-ch72, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 114
Mean 48.21
Std Dev 3.425
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

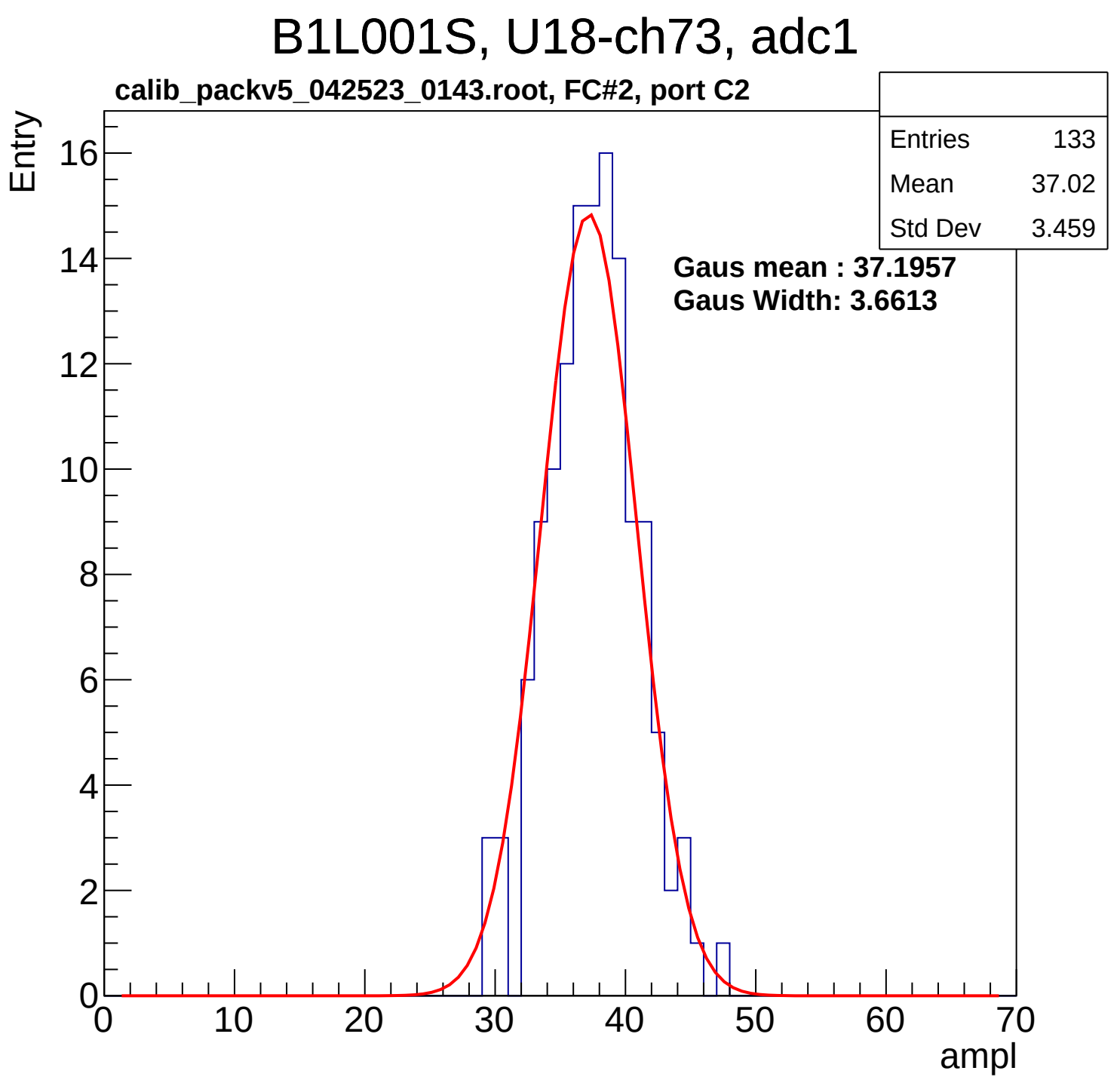

B1L001S, U18-ch72, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 145
Mean 54.29
Std Dev 3.363
Entry
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl

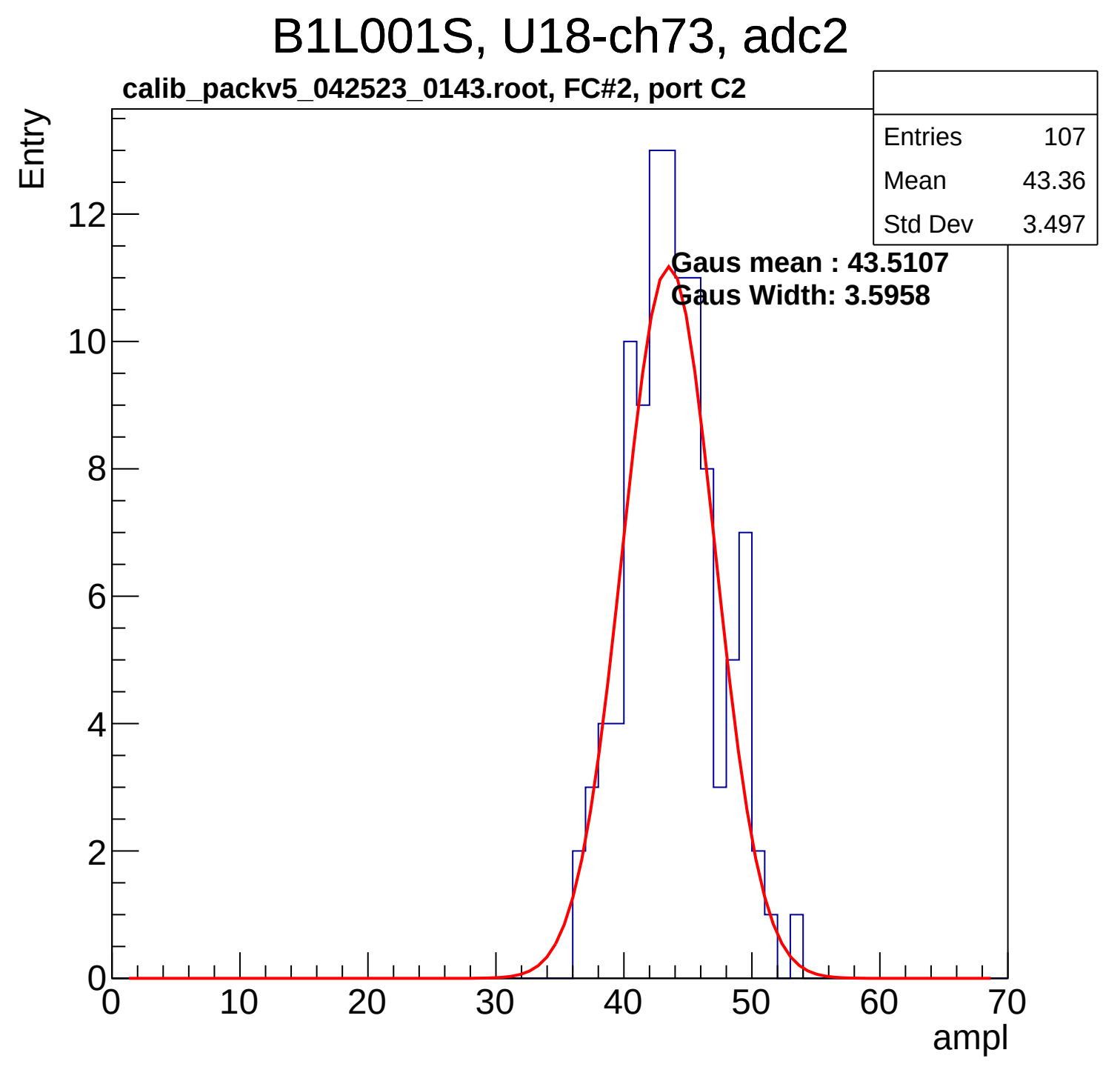

B1L001S, U18-ch72, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 79
Mean 58.87
Std Dev 7.011
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

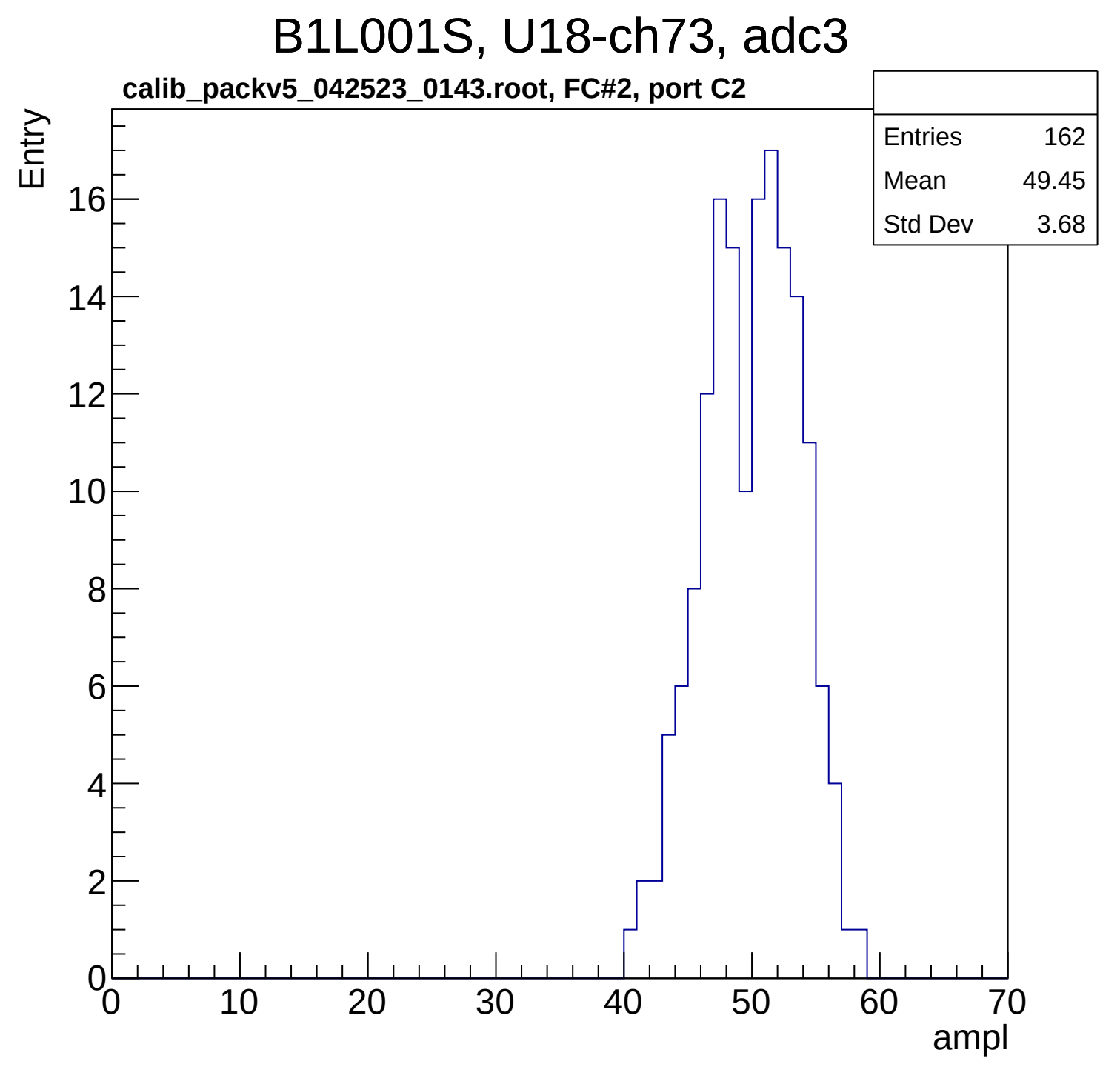

B1L001S, U18-ch72, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 27
Mean 59.89
Std Dev 11.79
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl

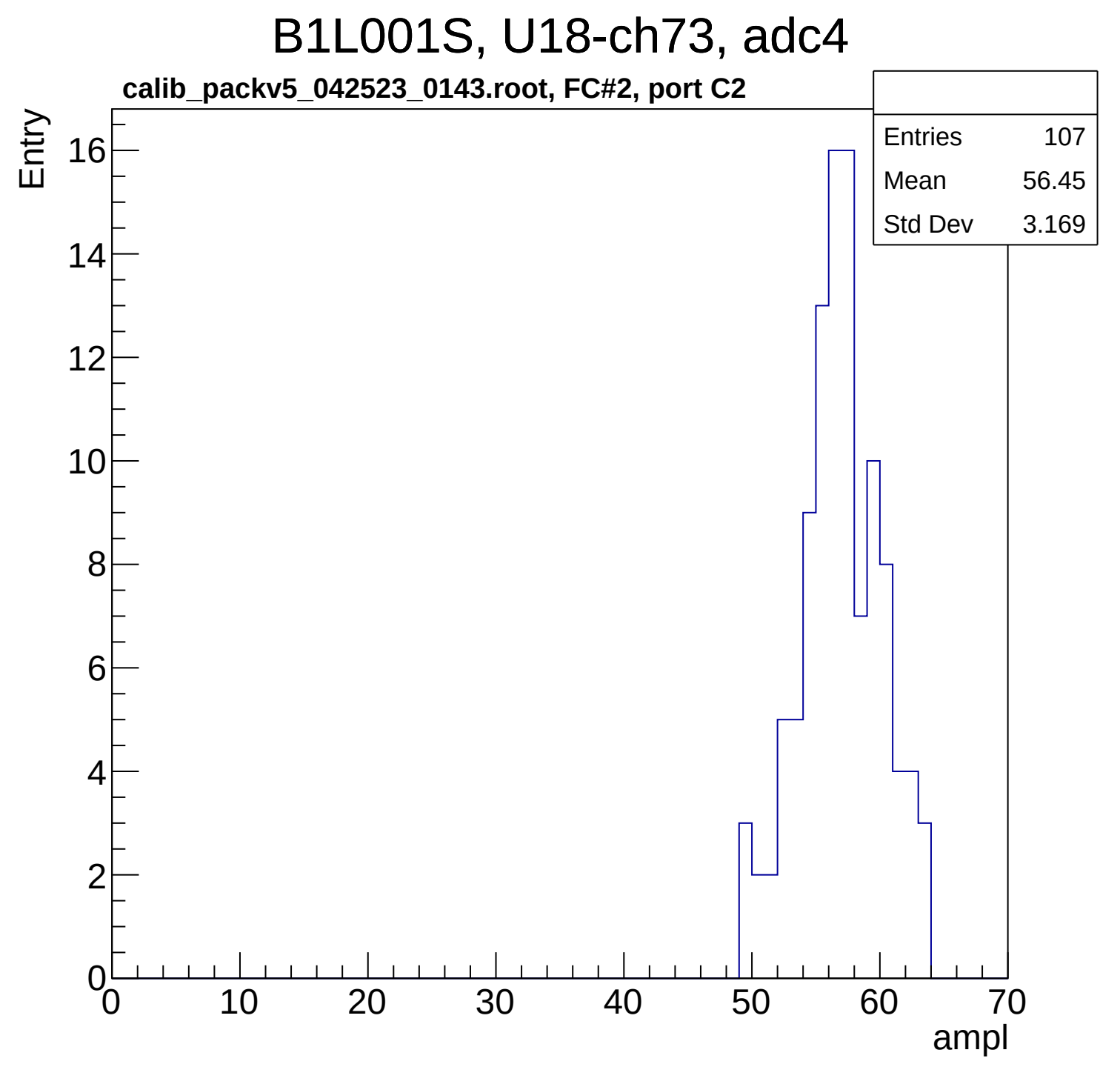

B1L001S, U18-ch72, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 3
Mean 42
Std Dev 29.7
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

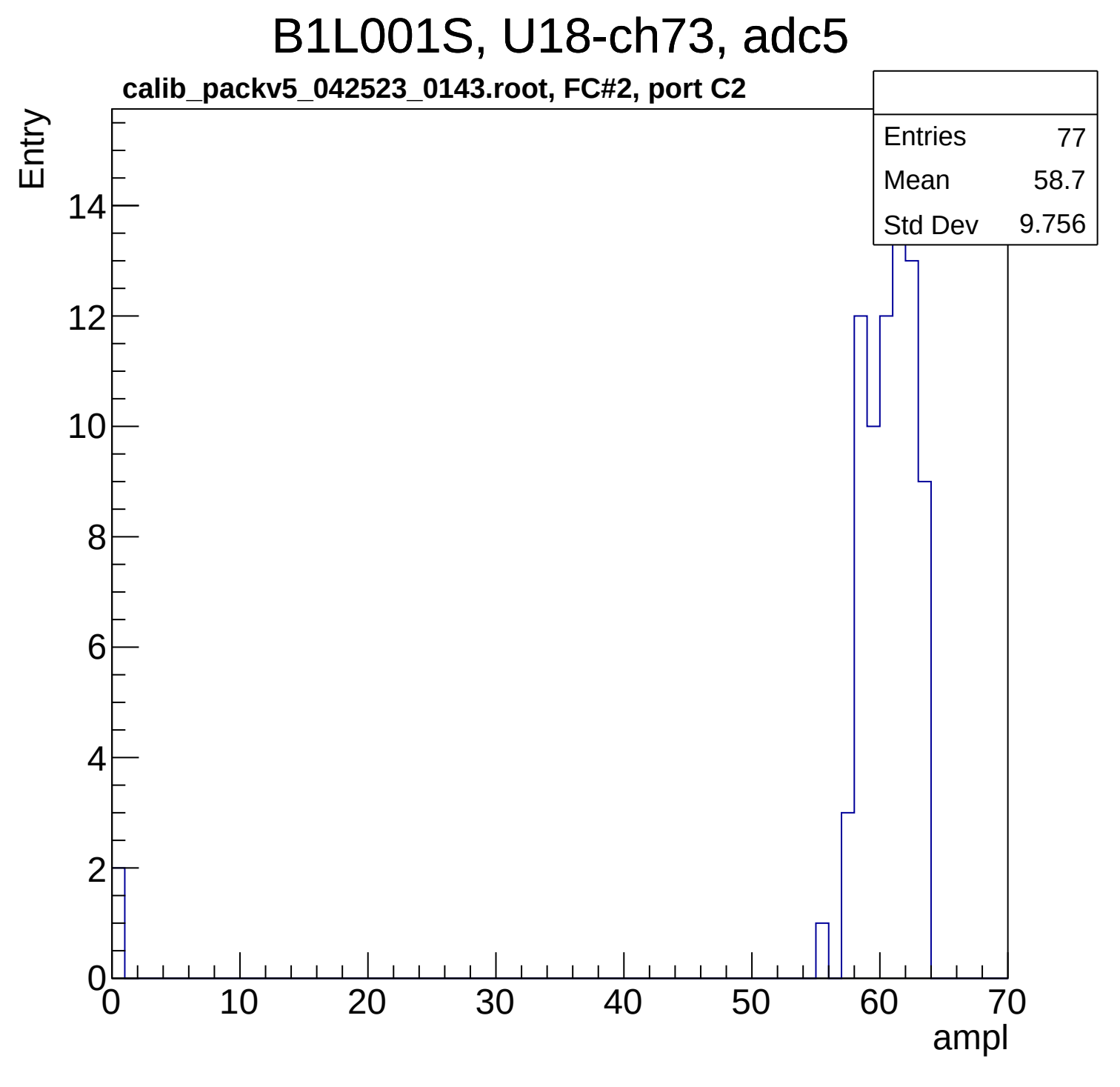

B1L001S, U18-ch73, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 154
Mean 29.54
Std Dev 4.819
Gaus mean : 30.5614
Gaus Width: 3.5183
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

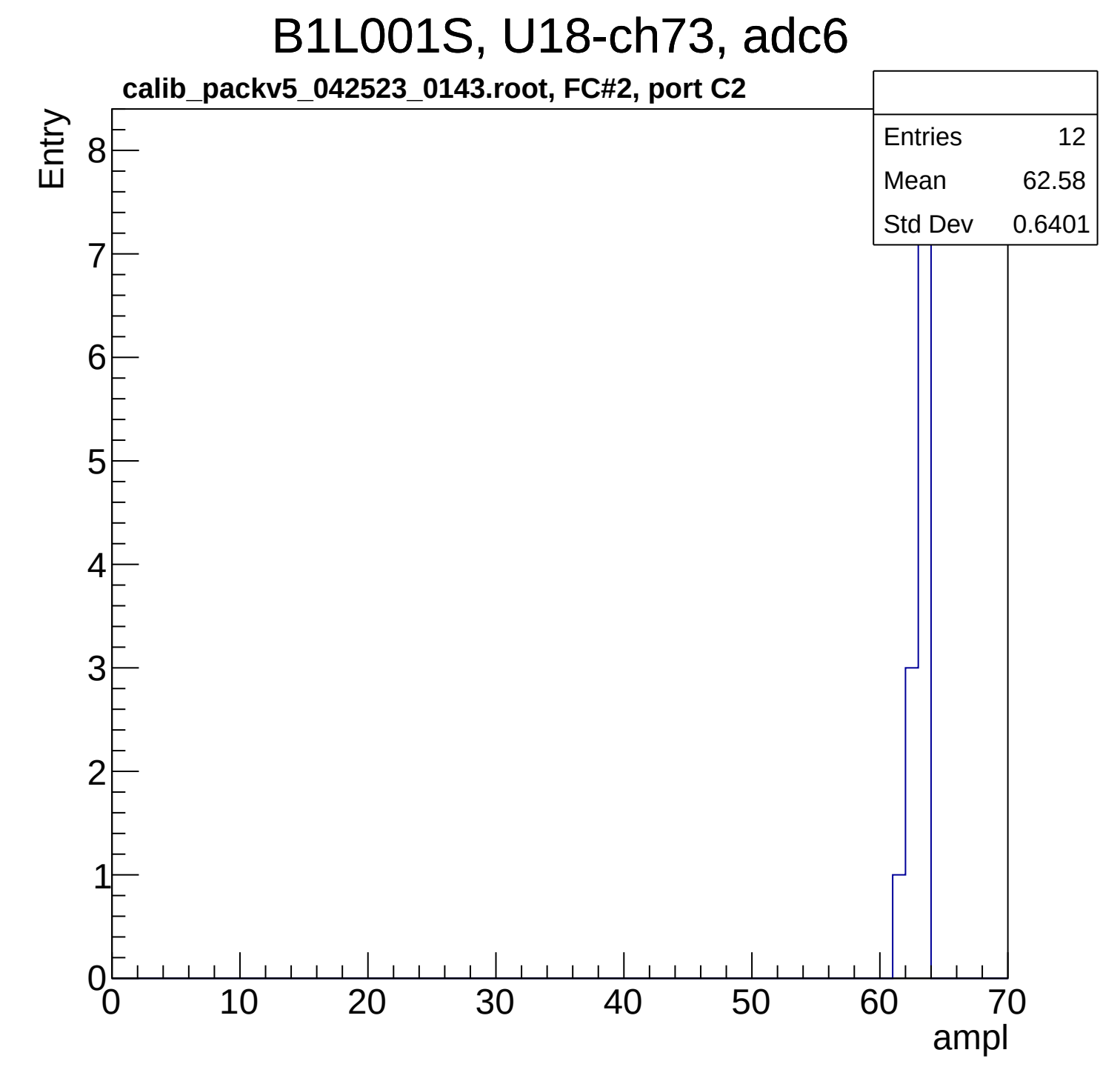

B1L001S, U18-ch73, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 133
Mean 37.02
Std Dev 3.459
Gaus mean : 37.1957
Gaus Width: 3.6613
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

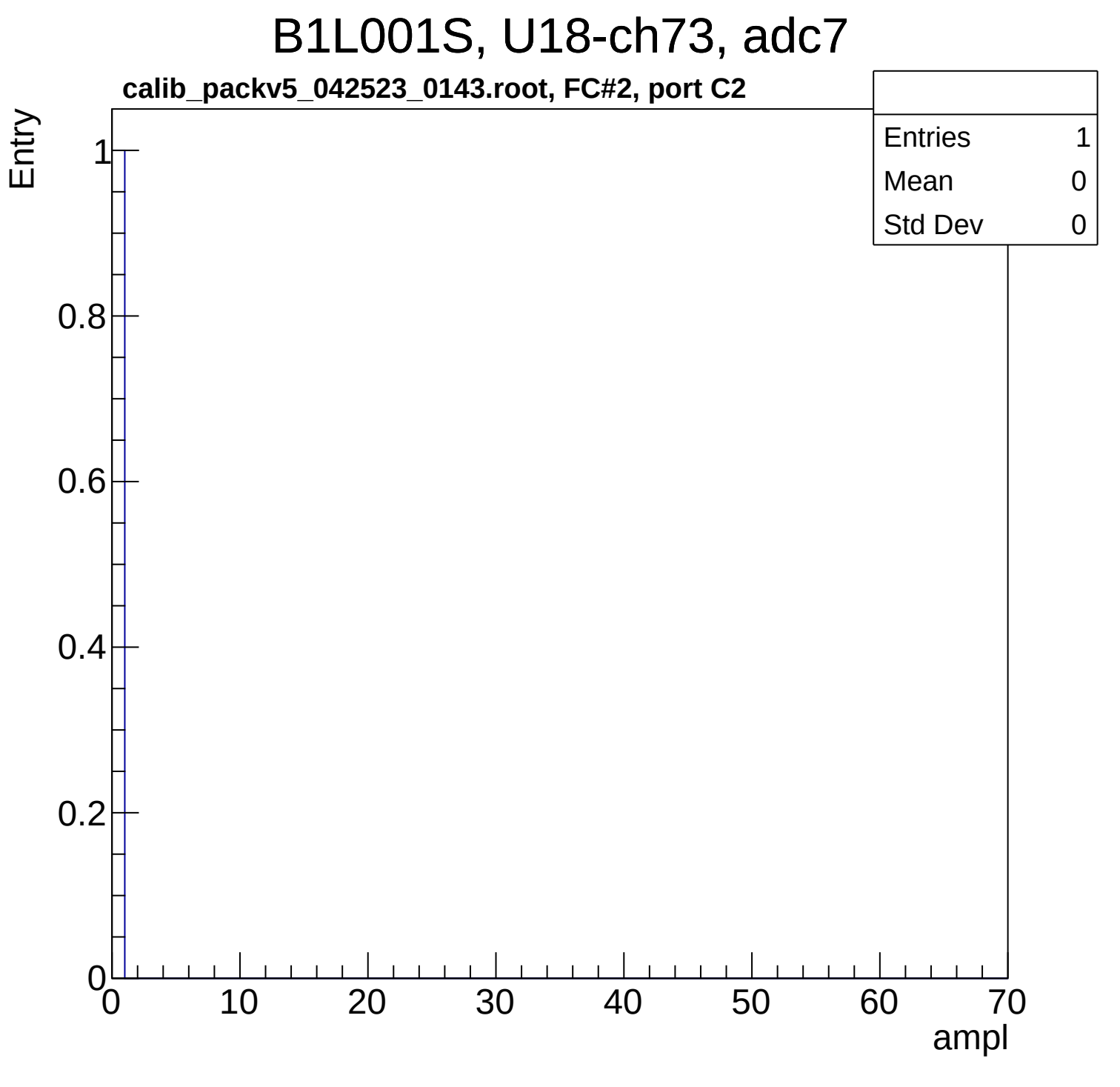

B1L001S, U18-ch73, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 107
Mean 43.36
Std Dev 3.497
Gaus mean : 43.5107
Gaus Width: 3.5958
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70

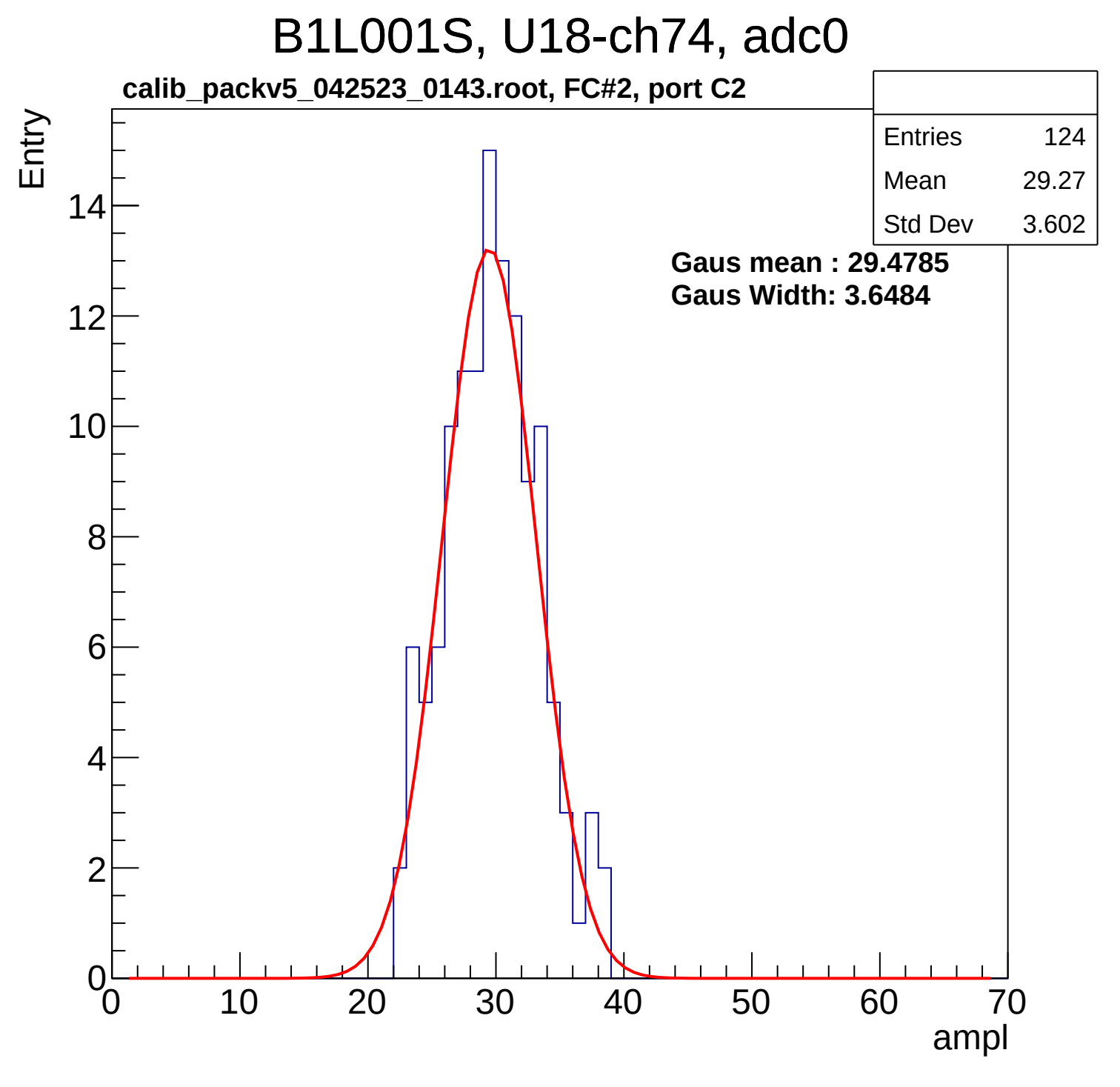

B1L001S, U18-ch73, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 162
Mean 49.45
Std Dev 3.68
Entry
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl

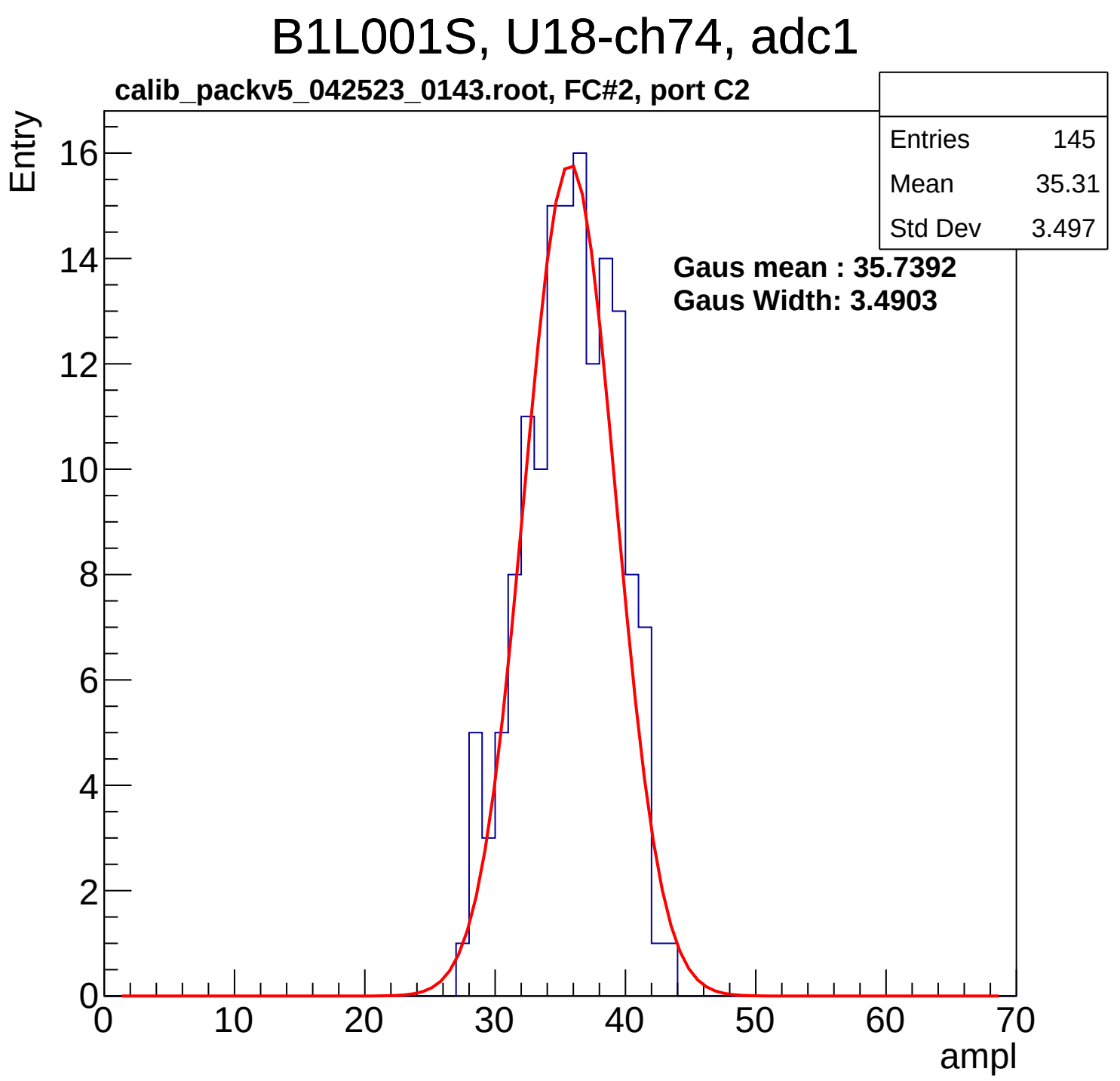

B1L001S, U18-ch73, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 107
Mean 56.45
Std Dev 3.169
Entry
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl

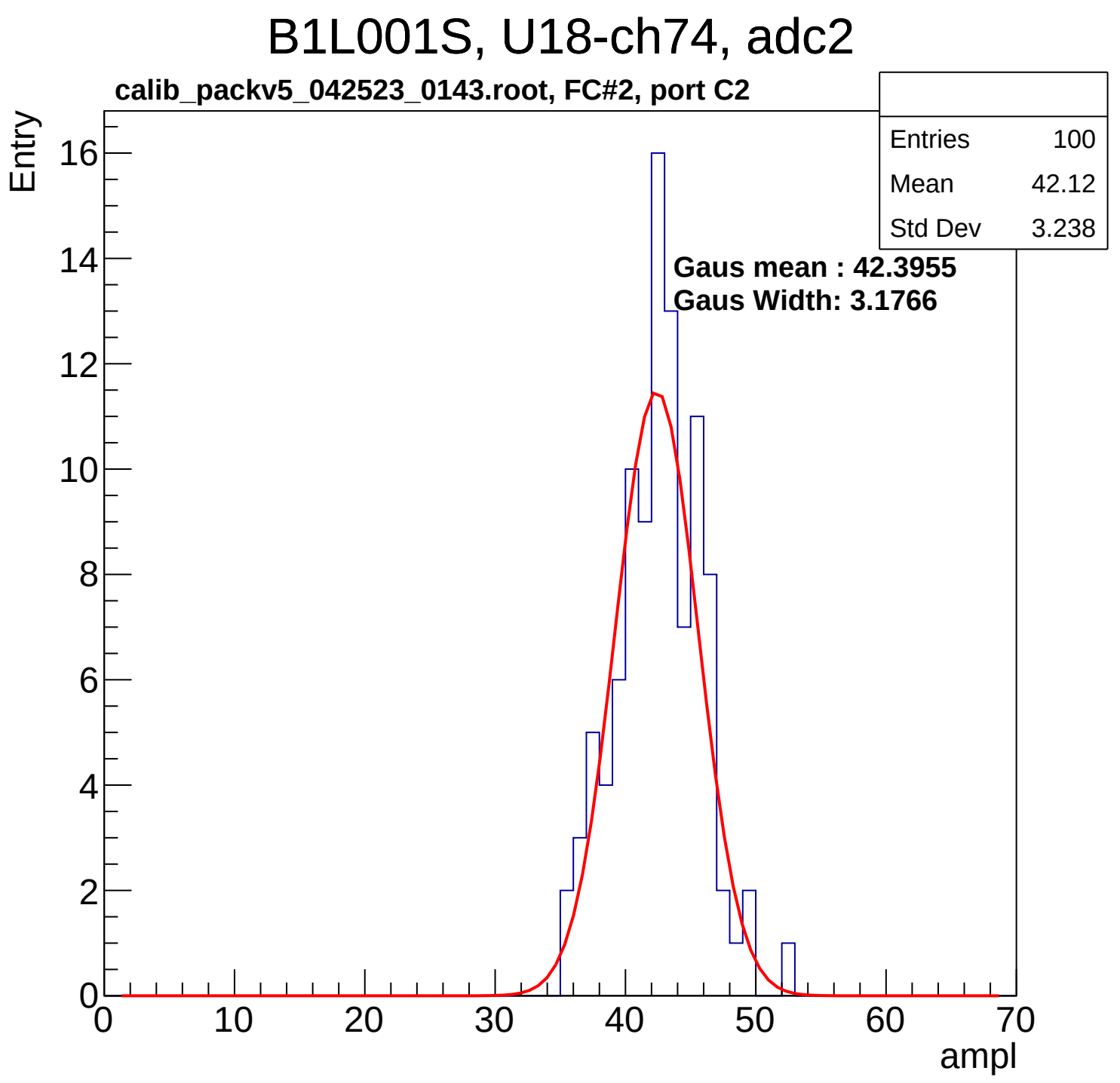

B1L001S, U18-ch73, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 77
Mean 58.7
Std Dev 9.756
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

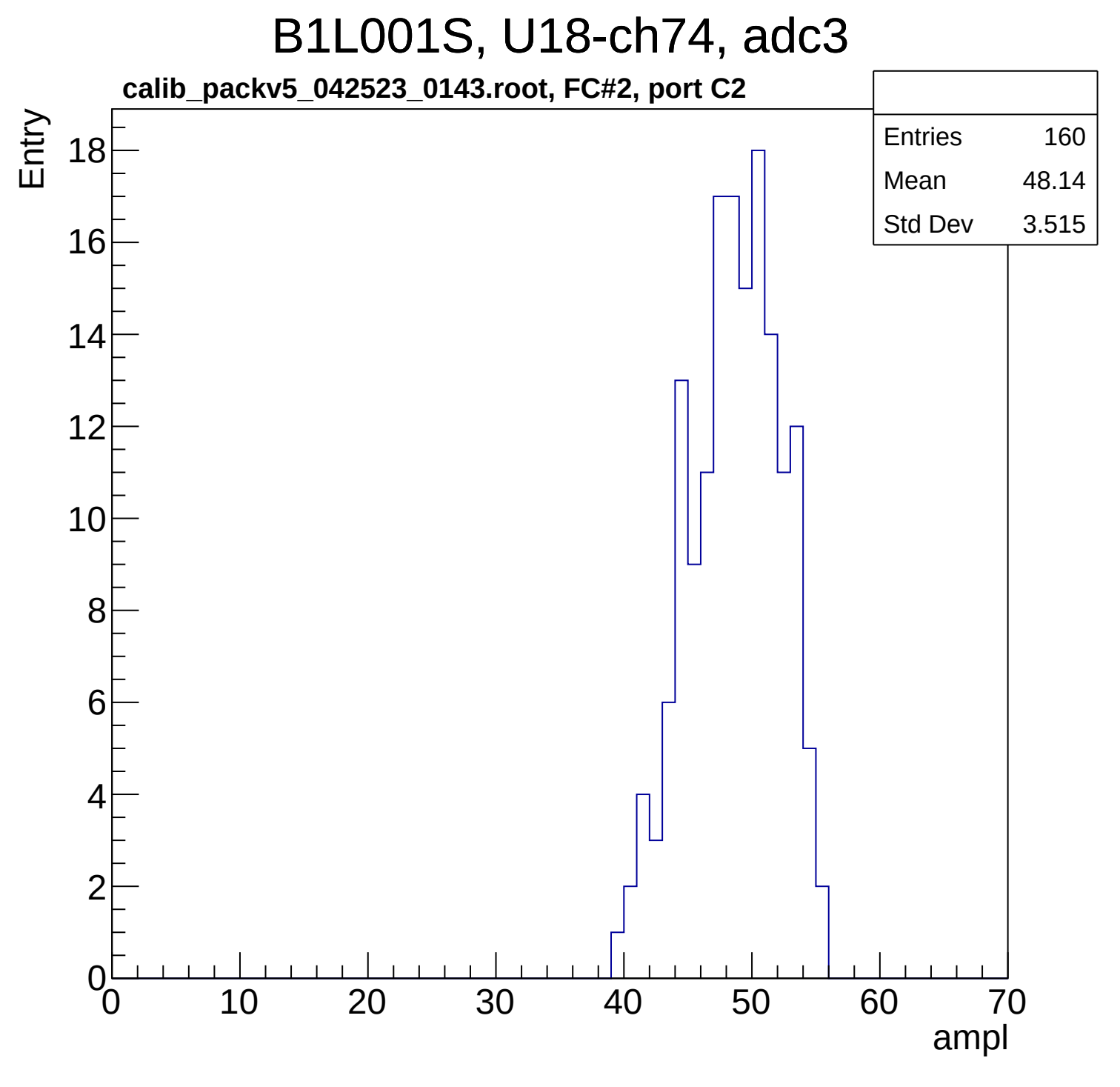

B1L001S, U18-ch73, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 12
Mean 62.58
Std Dev 0.6401
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

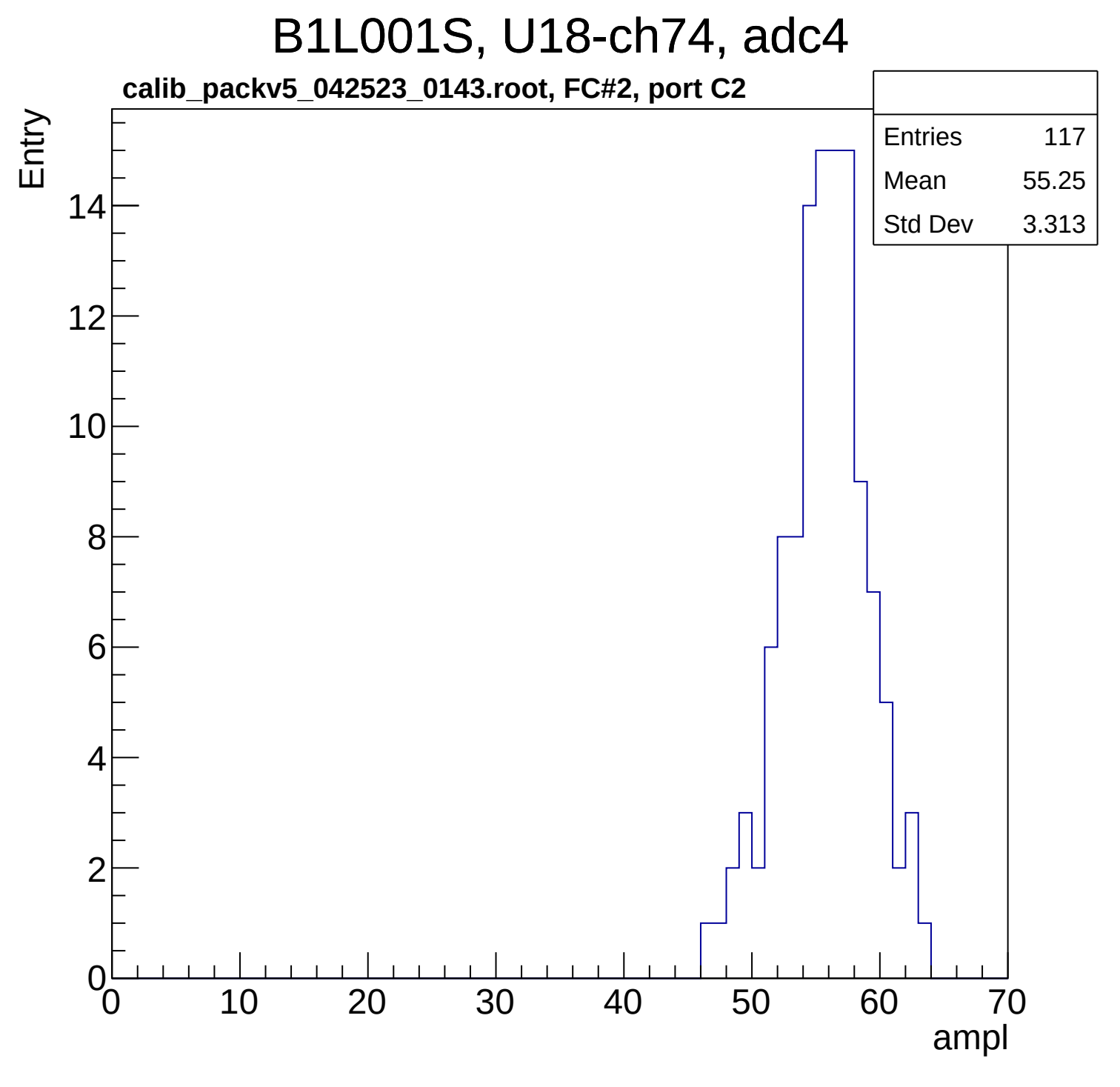

B1L001S, U18-ch73, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

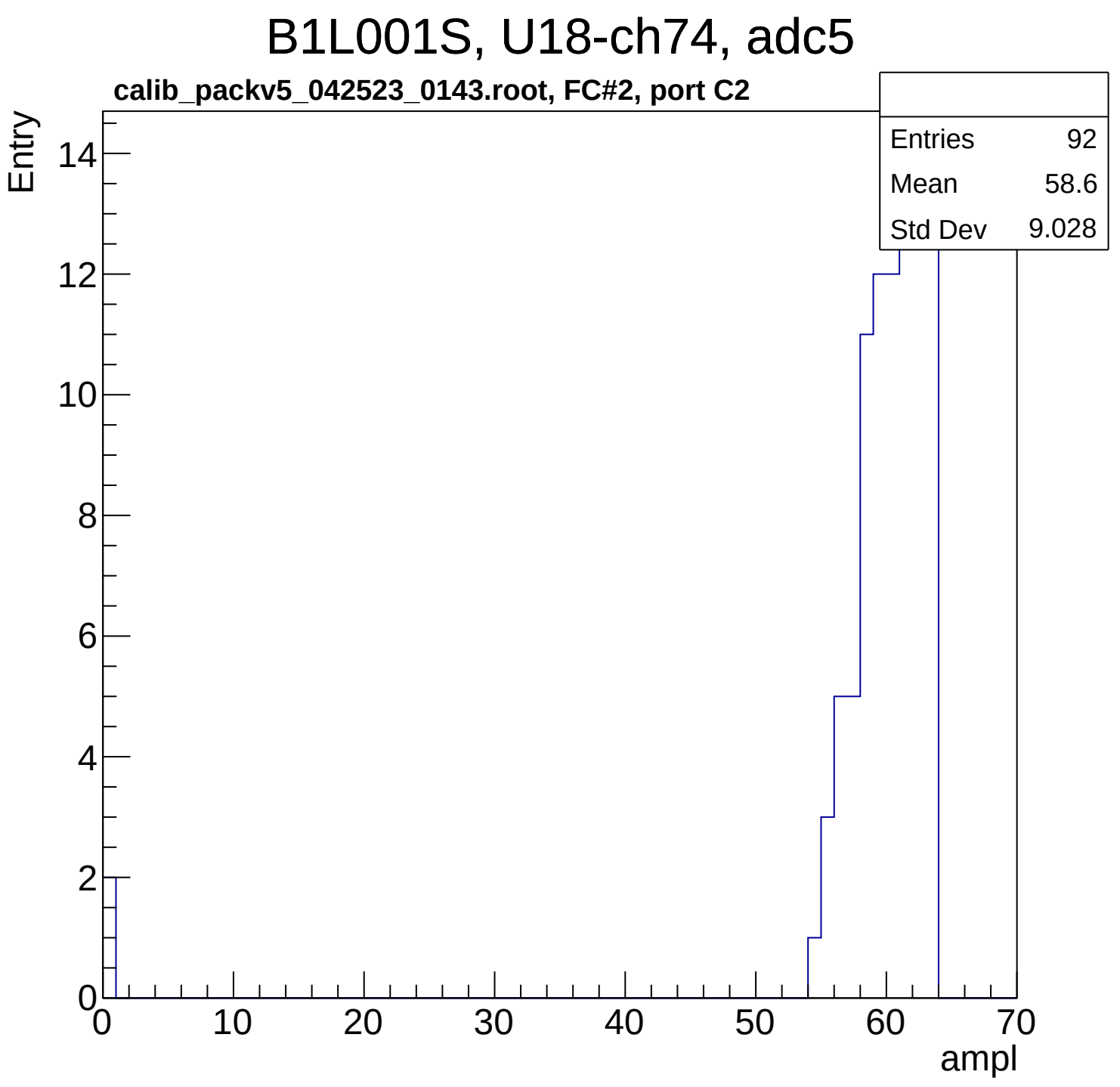

B1L001S, U18-ch74, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 124
Mean 29.27
Std Dev 3.602
Gaus mean : 29.4785
Gaus Width: 3.6484
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

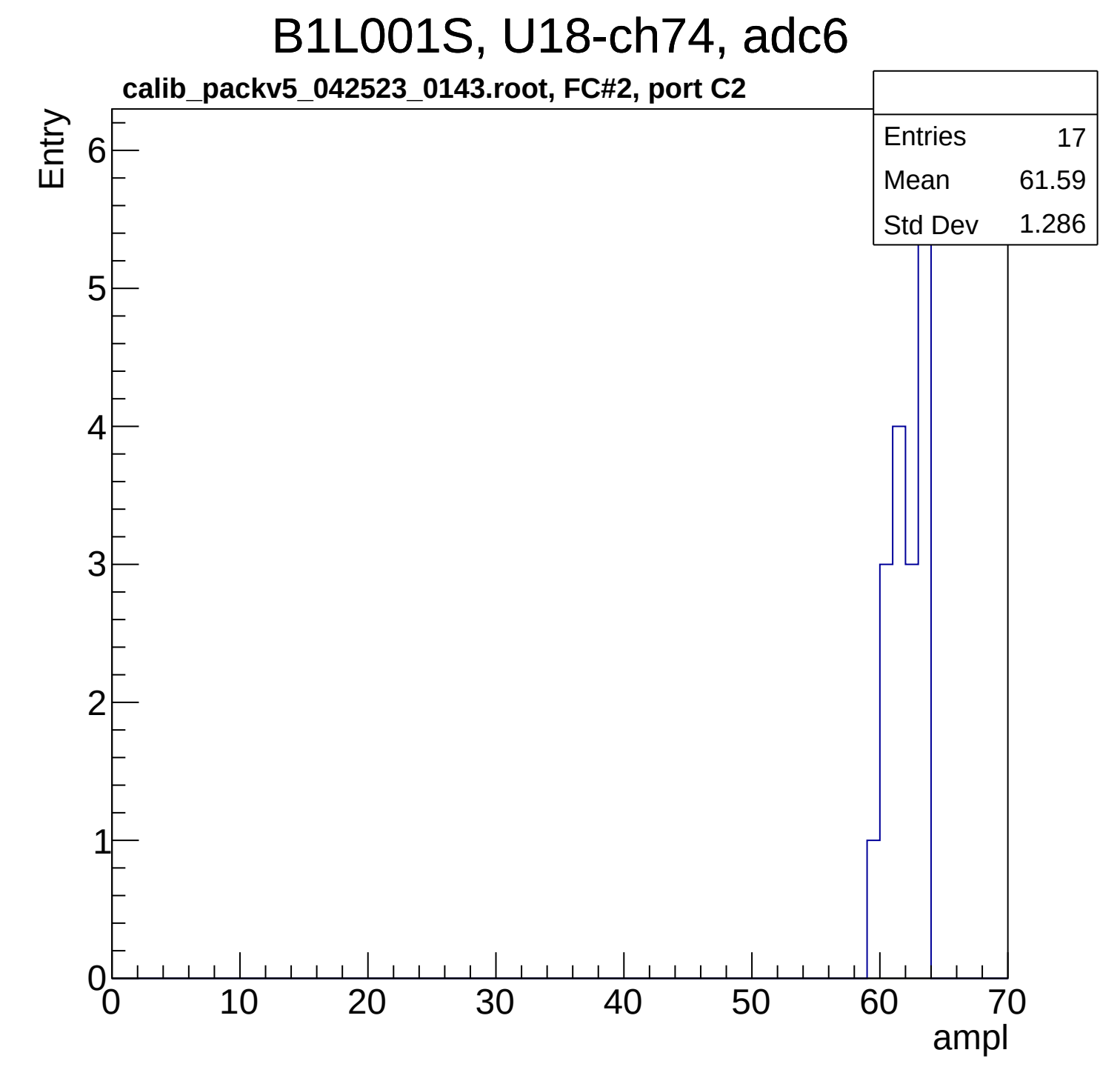

B1L001S, U18-ch74, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 145
Mean 35.31
Std Dev 3.497
Gaus mean : 35.7392
Gaus Width: 3.4903
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

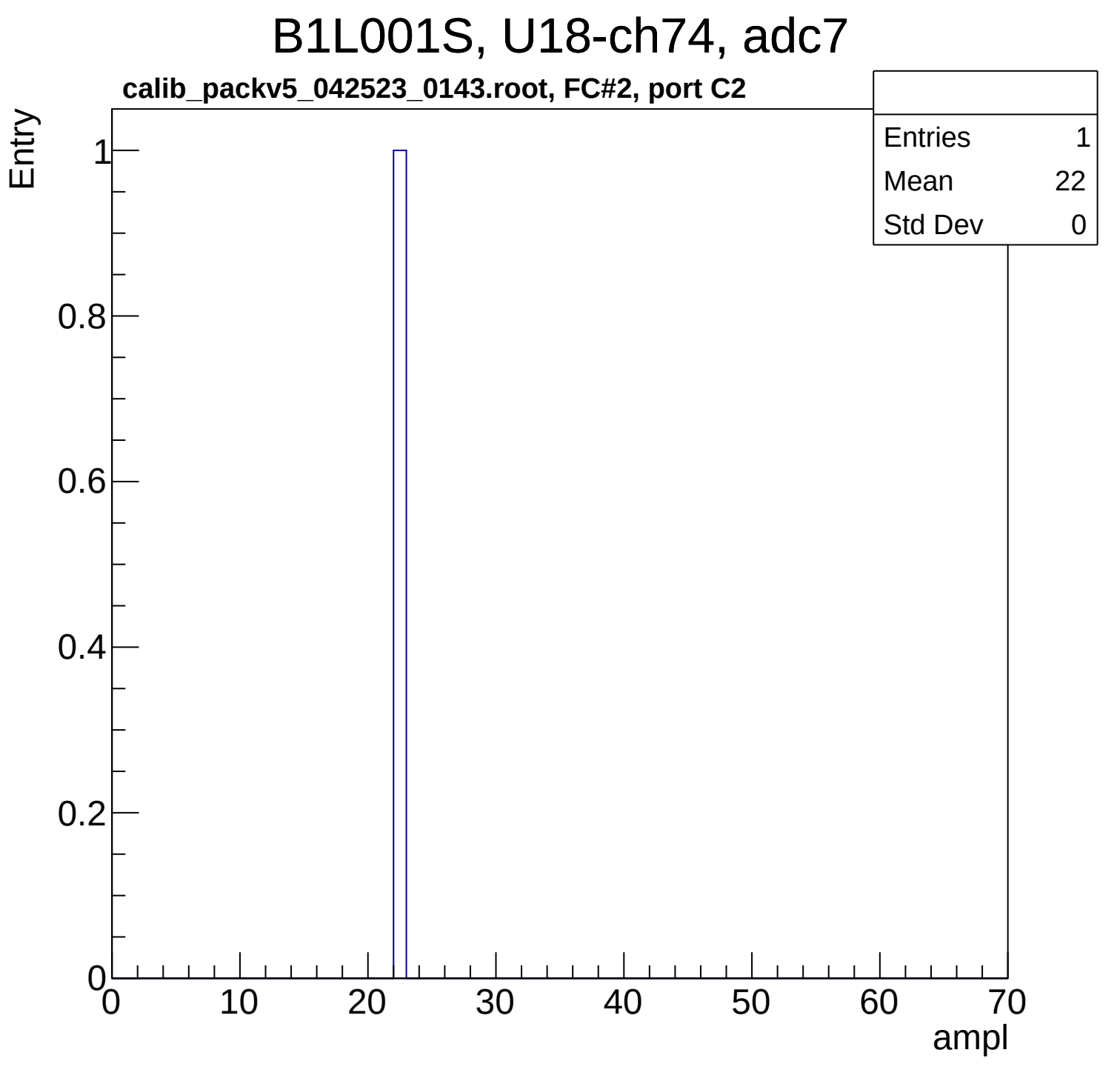

B1L001S, U18-ch74, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 100
Mean 42.12
Std Dev 3.238
Gaus mean : 42.3955
Gaus Width: 3.1766
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

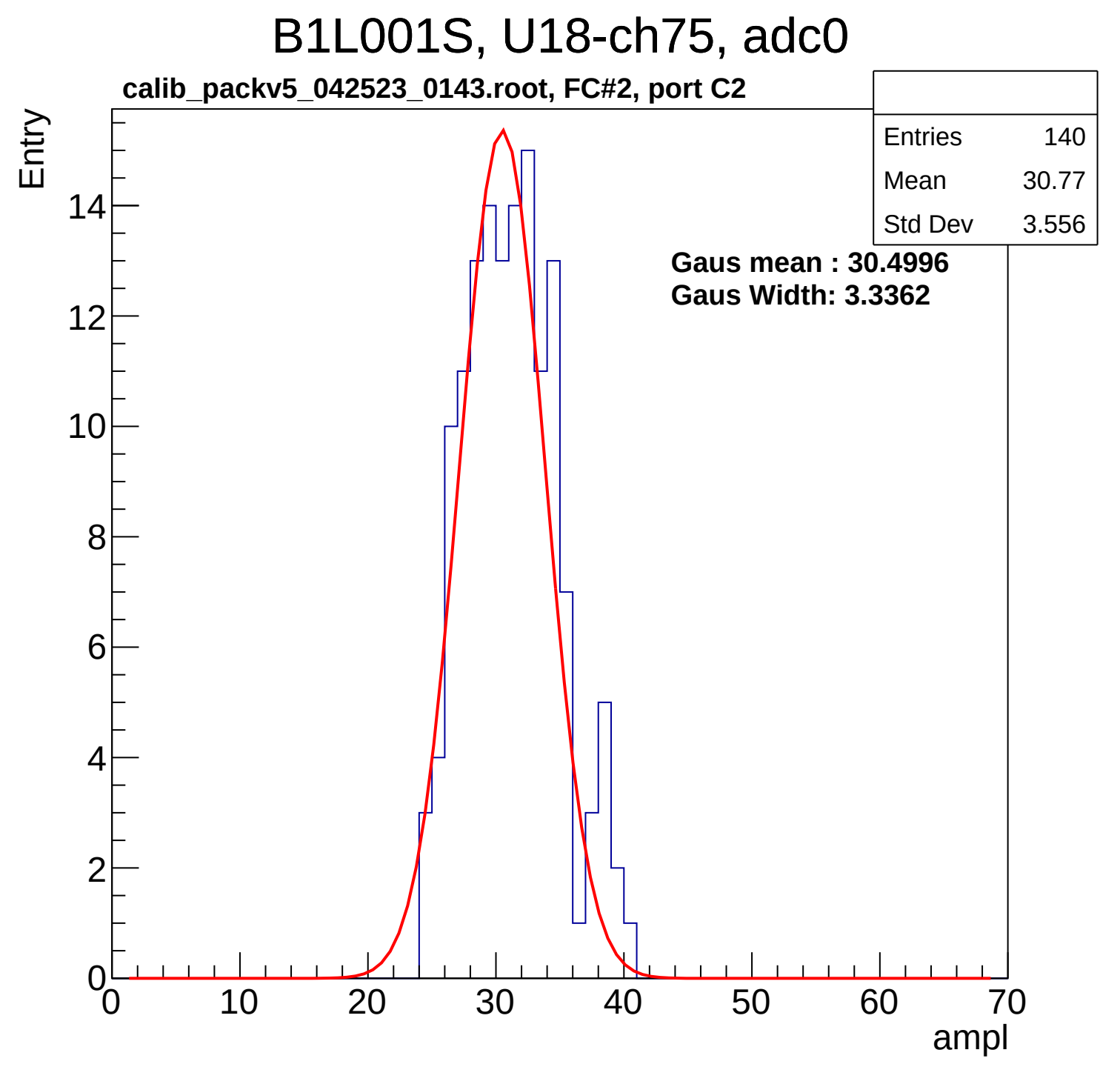

B1L001S, U18-ch74, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 160
Mean 48.14
Std Dev 3.515
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

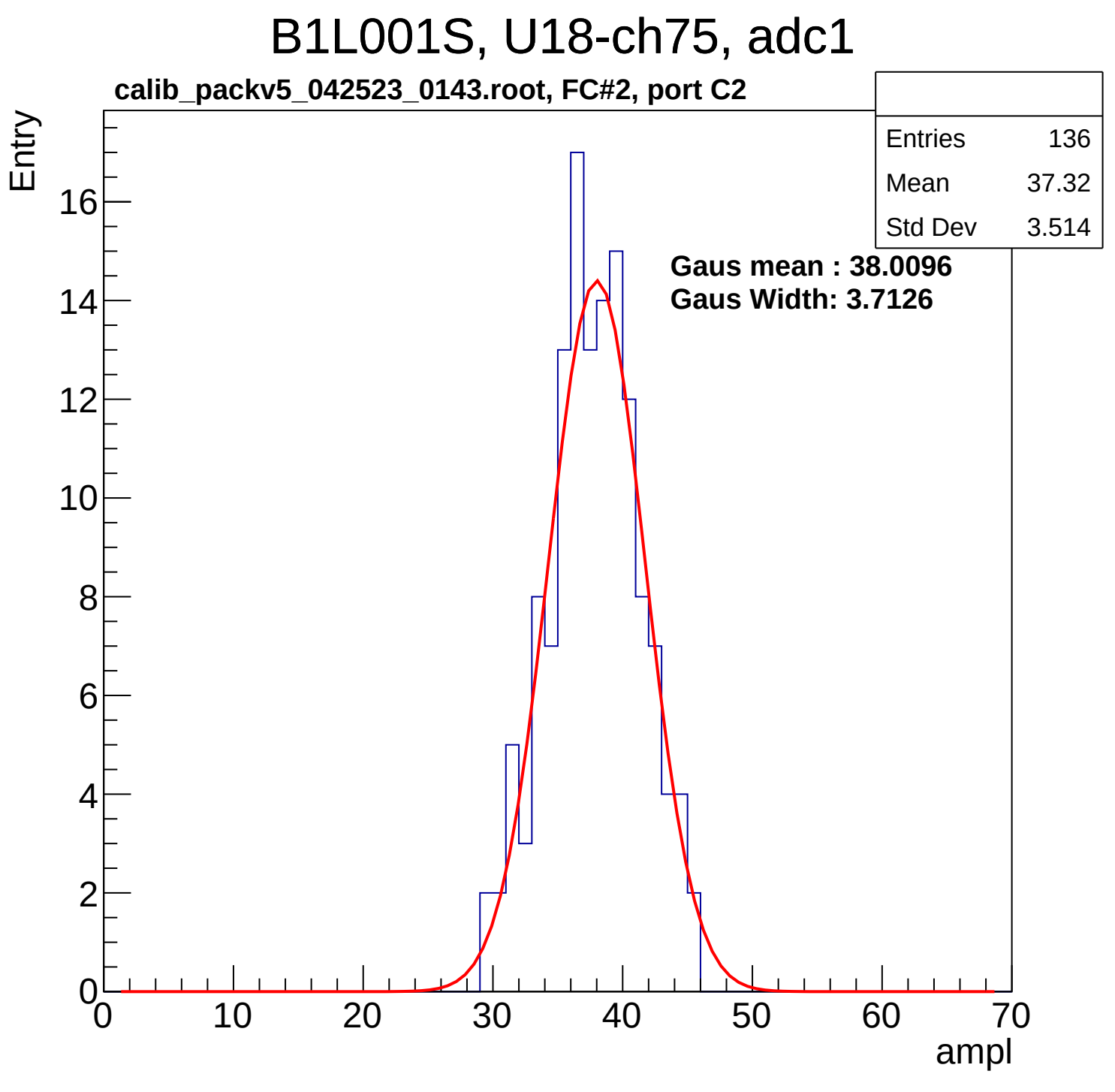

B1L001S, U18-ch74, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 117
Mean 55.25
Std Dev 3.313
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl

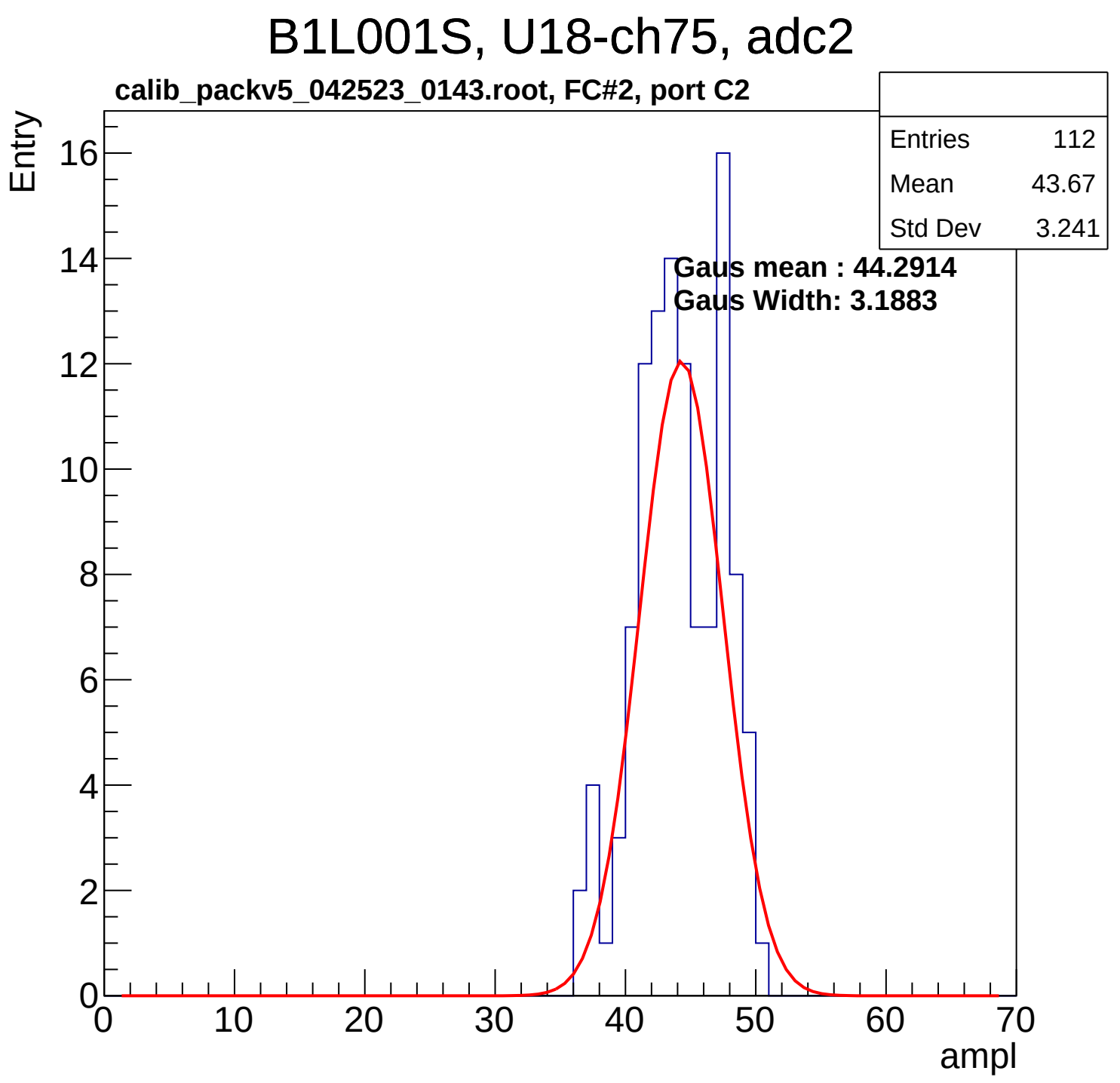

B1L001S, U18-ch74, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 92
Mean 58.6
Std Dev 9.028
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

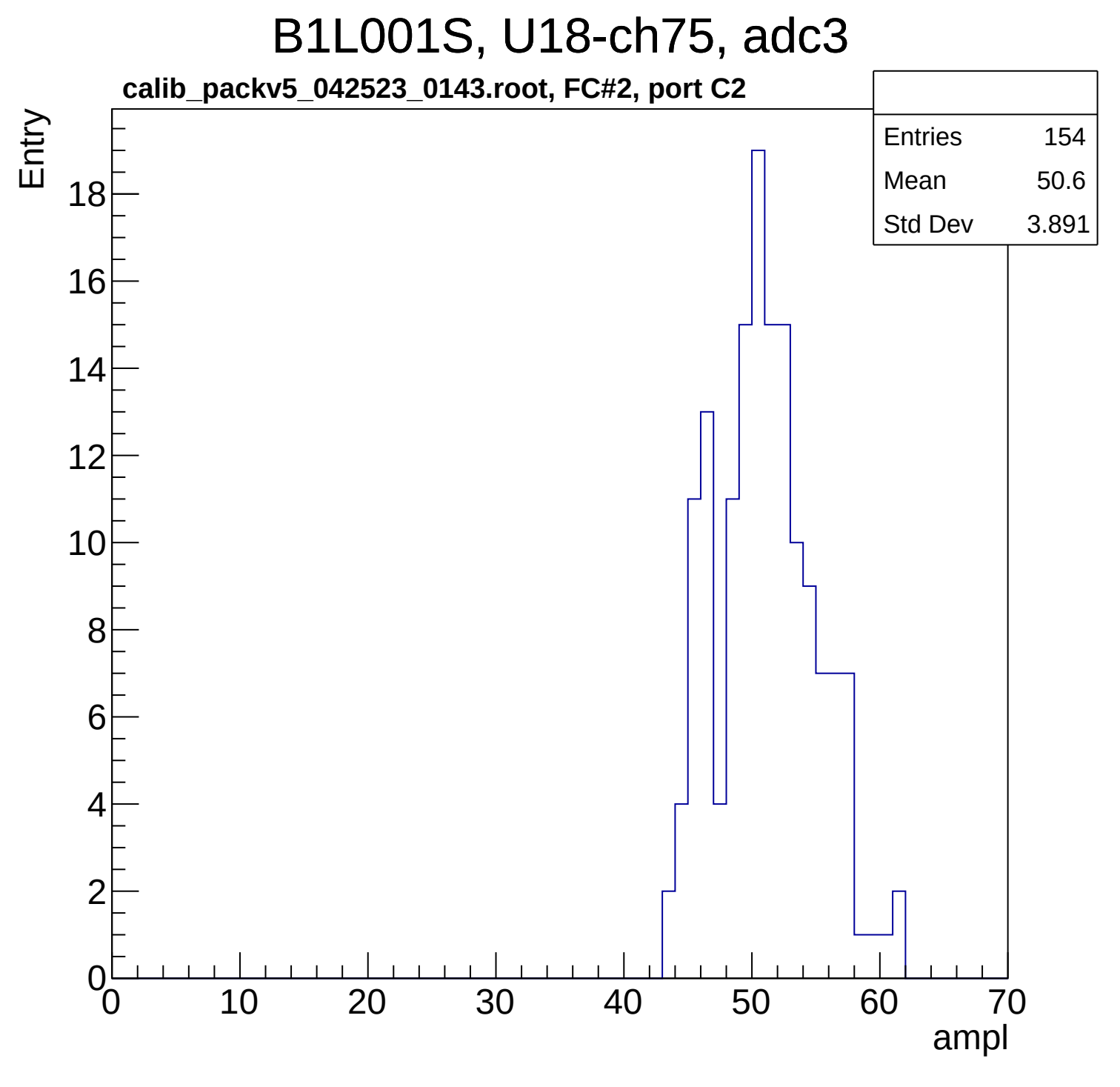

B1L001S, U18-ch74, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 17
Mean 61.59
Std Dev 1.286
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

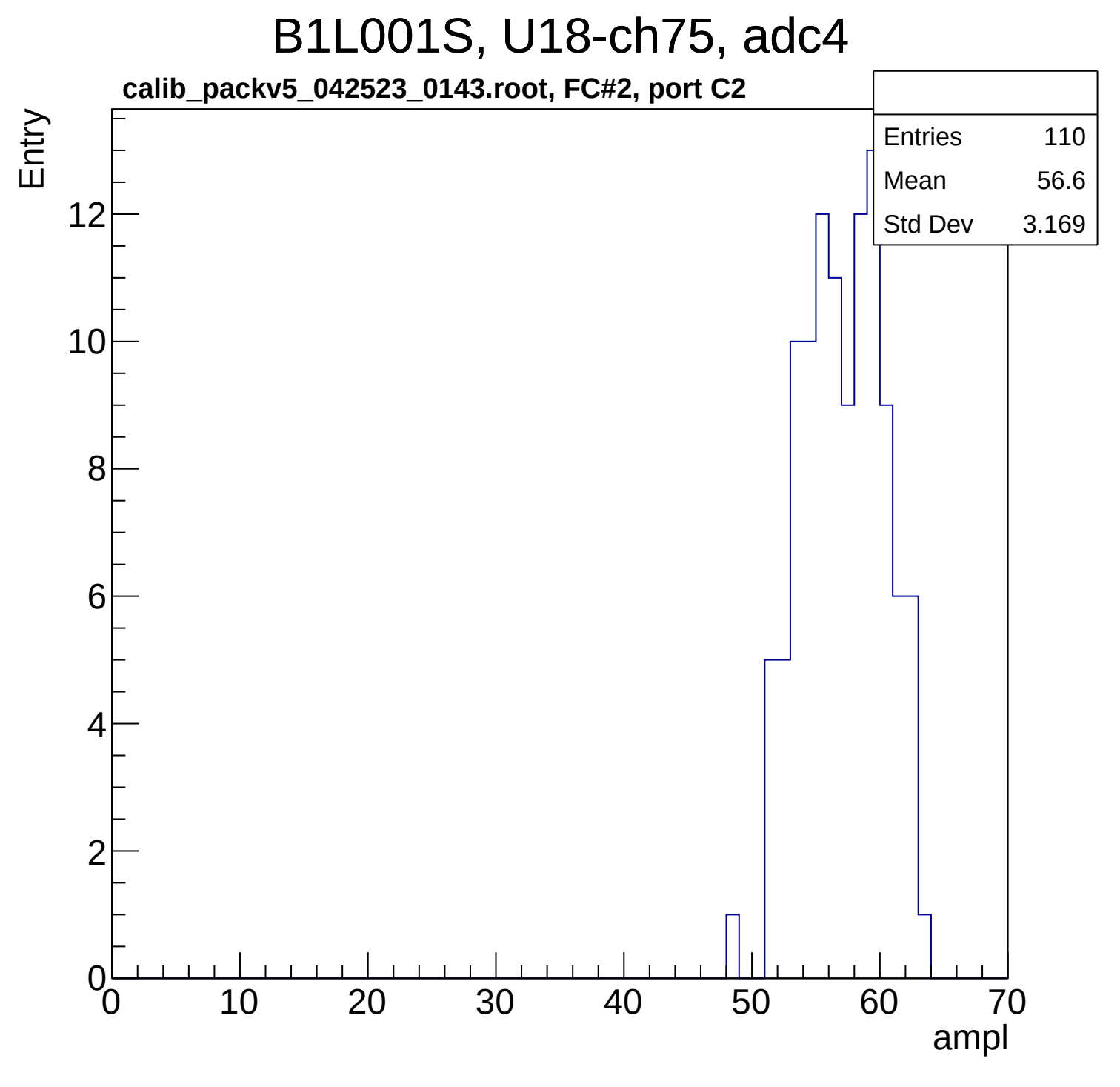

B1L001S, U18-ch74, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 22
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

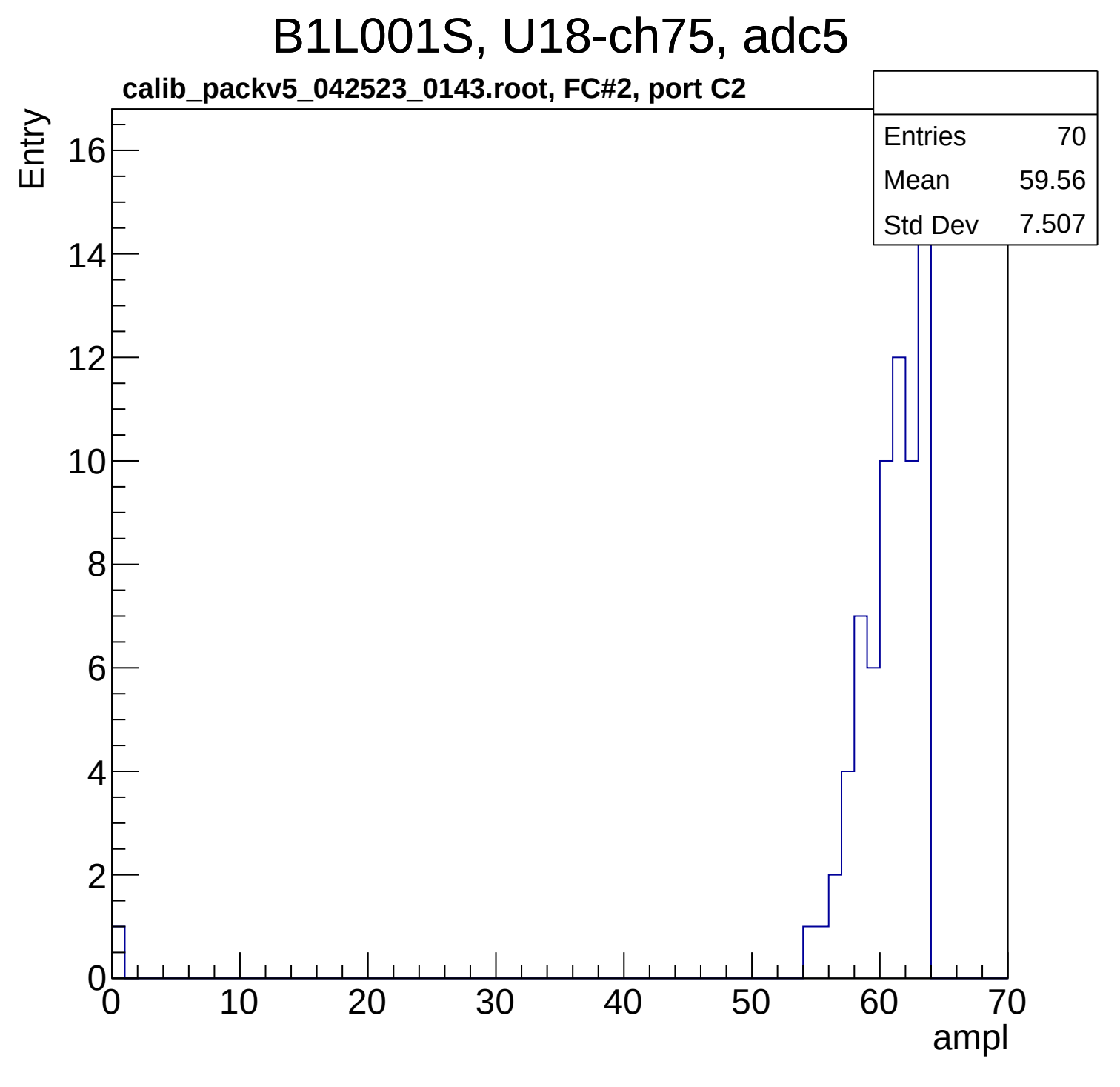

B1L001S, U18-ch75, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 140
Mean 30.77
Std Dev 3.556
Gaus mean : 30.4996
Gaus Width: 3.3362
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

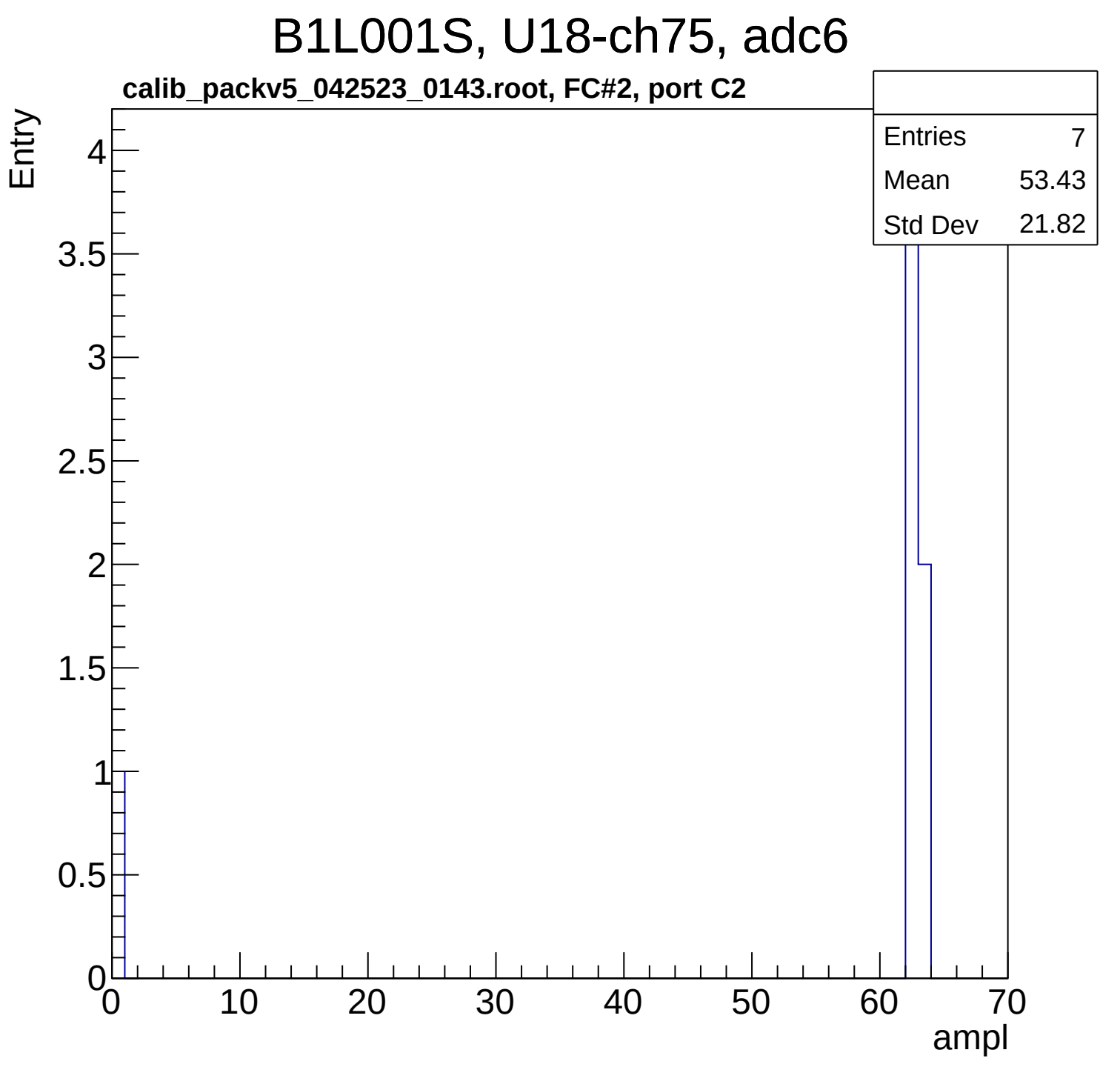

B1L001S, U18-ch75, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 136
Mean 37.32
Std Dev 3.514
Gaus mean : 38.0096
Gaus Width: 3.7126
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

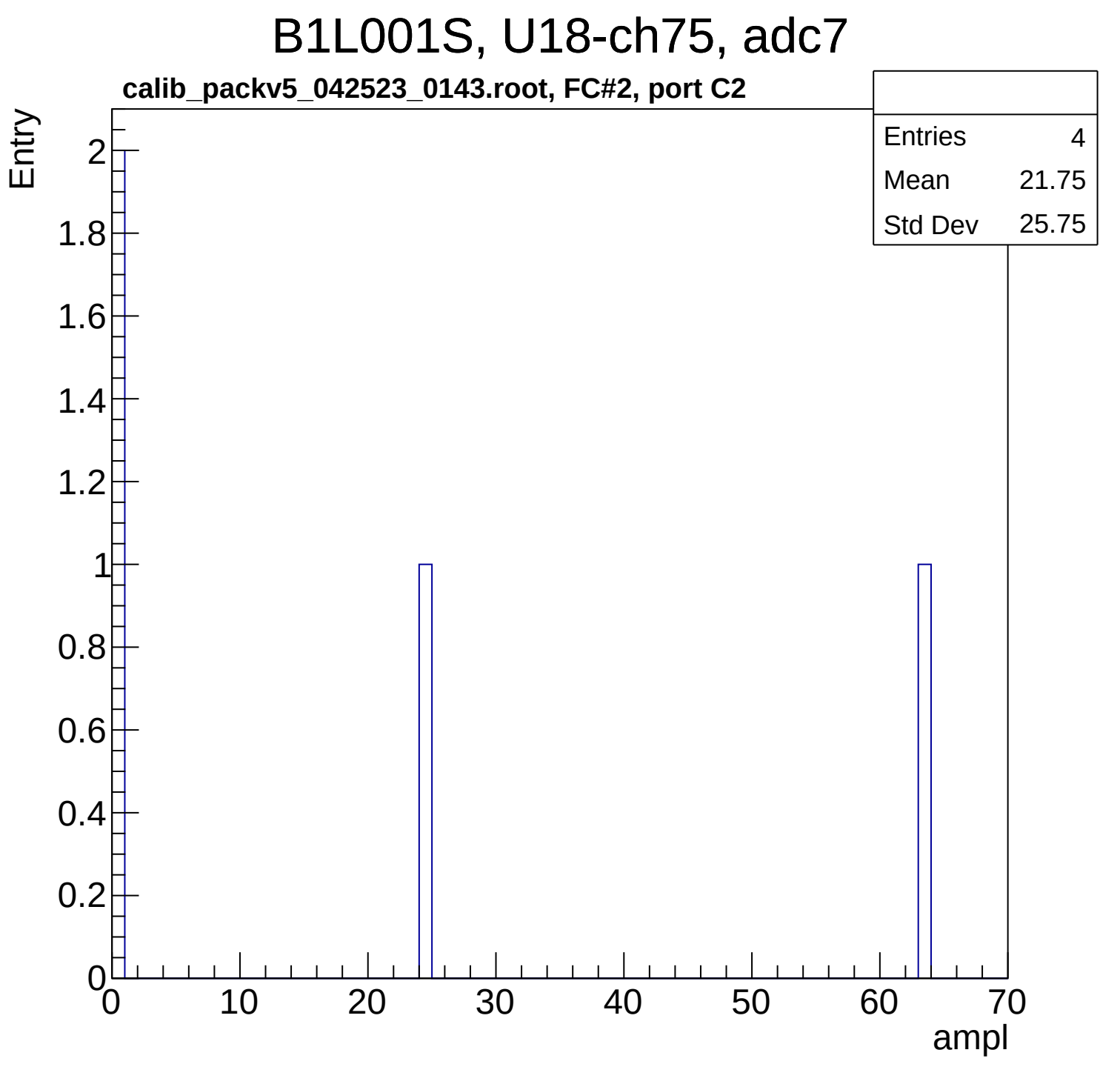

B1L001S, U18-ch75, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 112
Mean 43.67
Std Dev 3.241
Gaus mean : 44.2914
Gaus Width: 3.1883
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

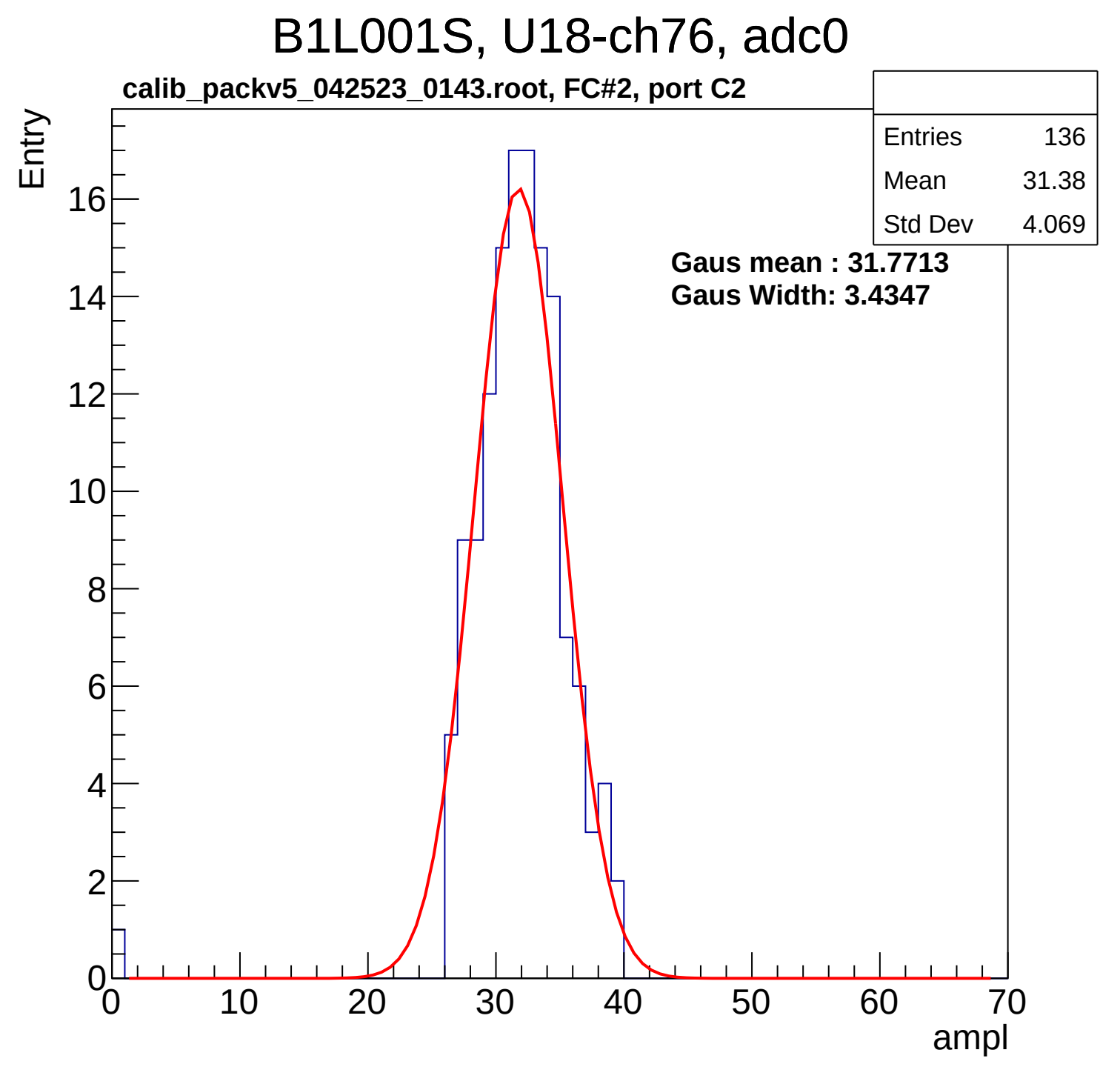

B1L001S, U18-ch75, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 154
Mean 50.6
Std Dev 3.891
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

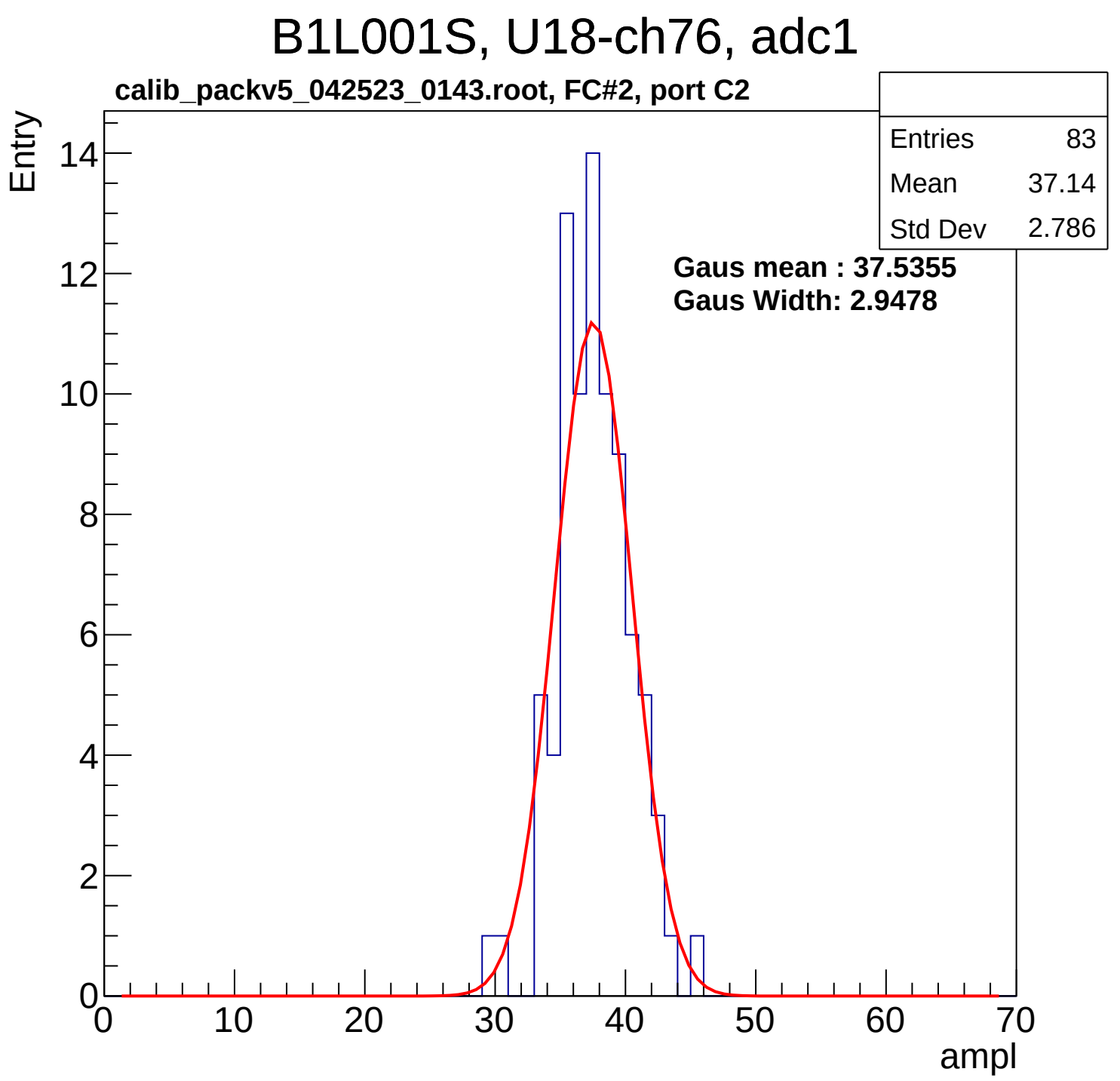

B1L001S, U18-ch75, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 110
Mean 56.6
Std Dev 3.169
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70

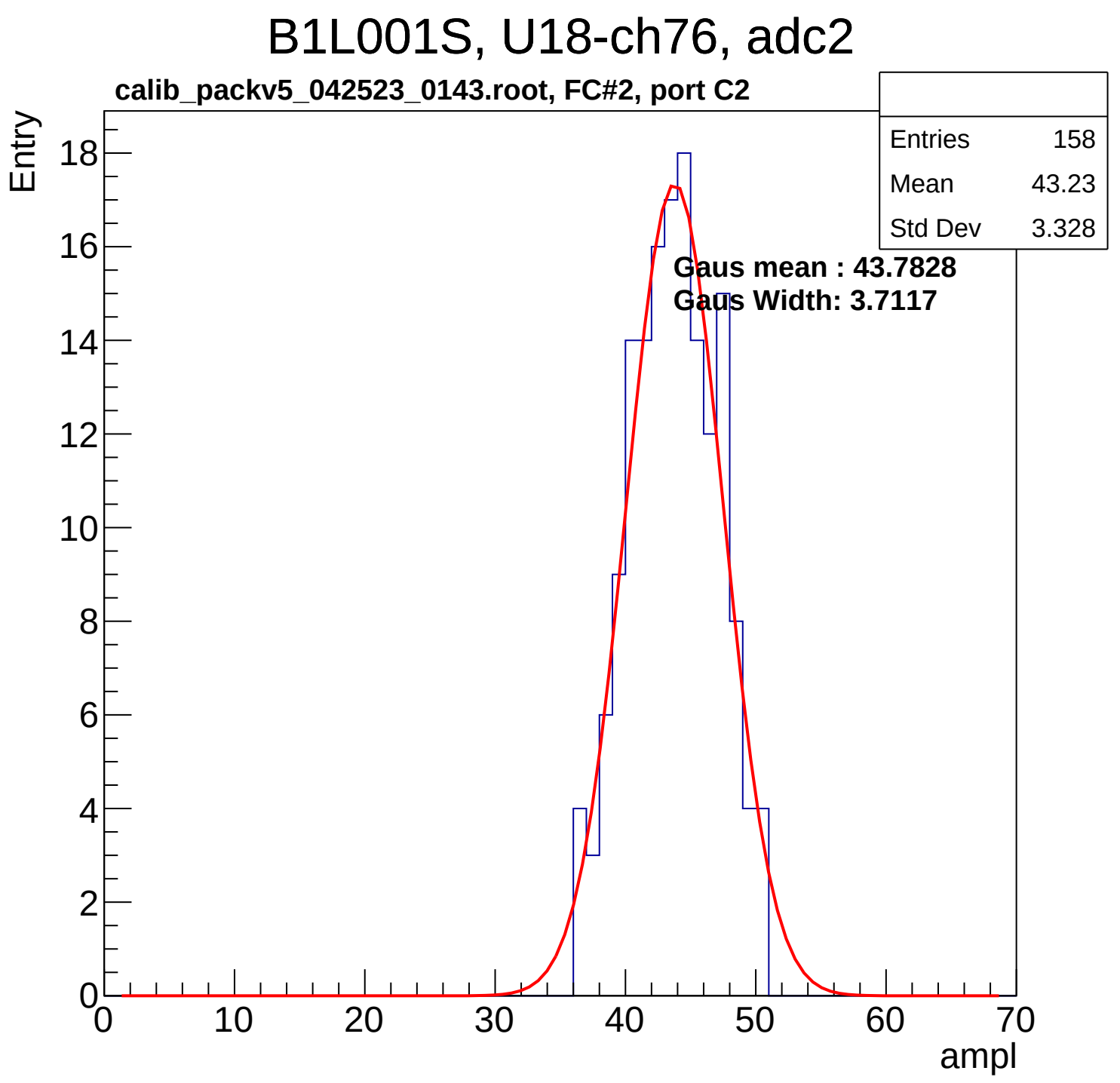

B1L001S, U18-ch75, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 70
Mean 59.56
Std Dev 7.507
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

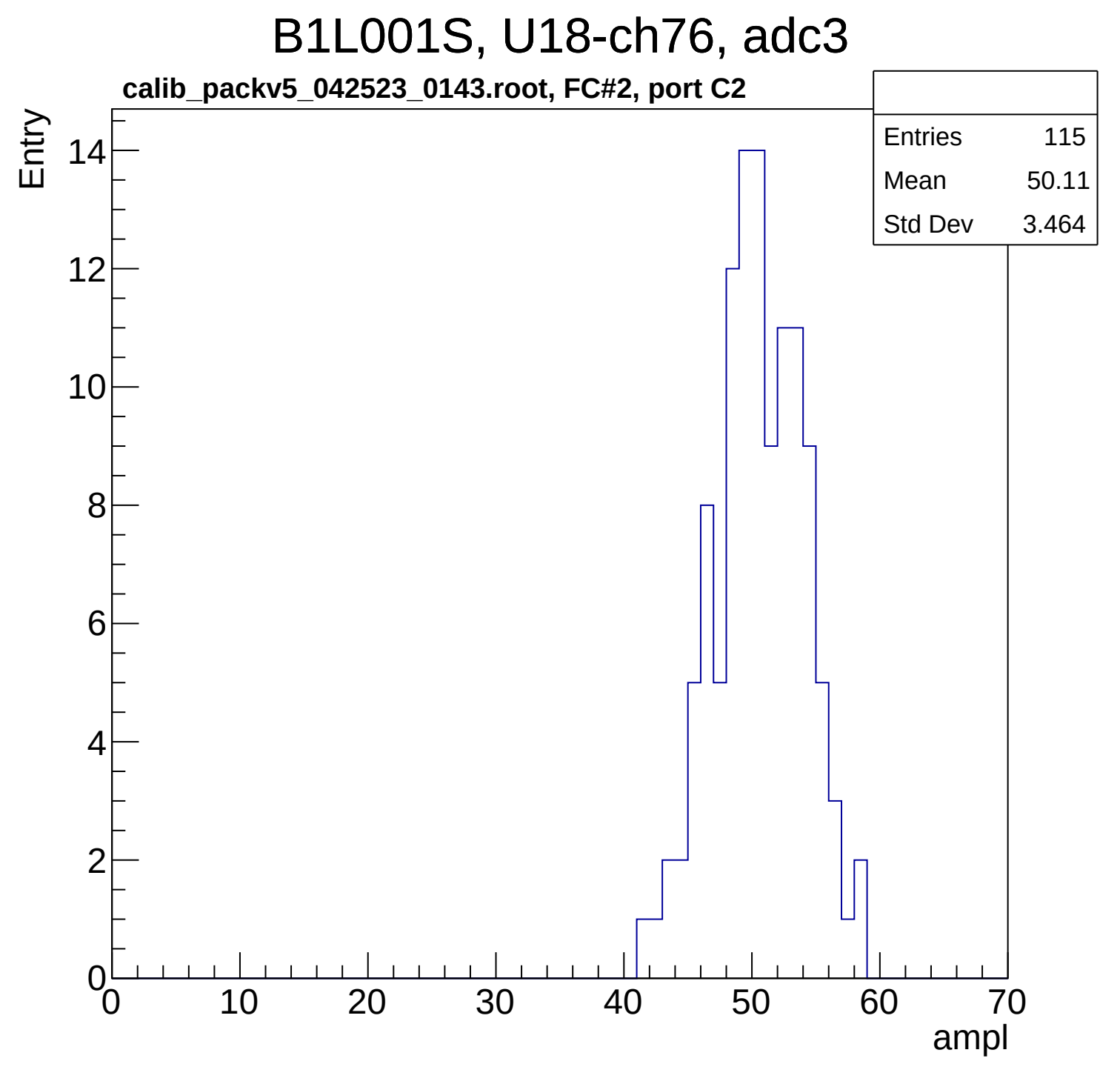

B1L001S, U18-ch75, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 7
Mean 53.43
Std Dev 21.82
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

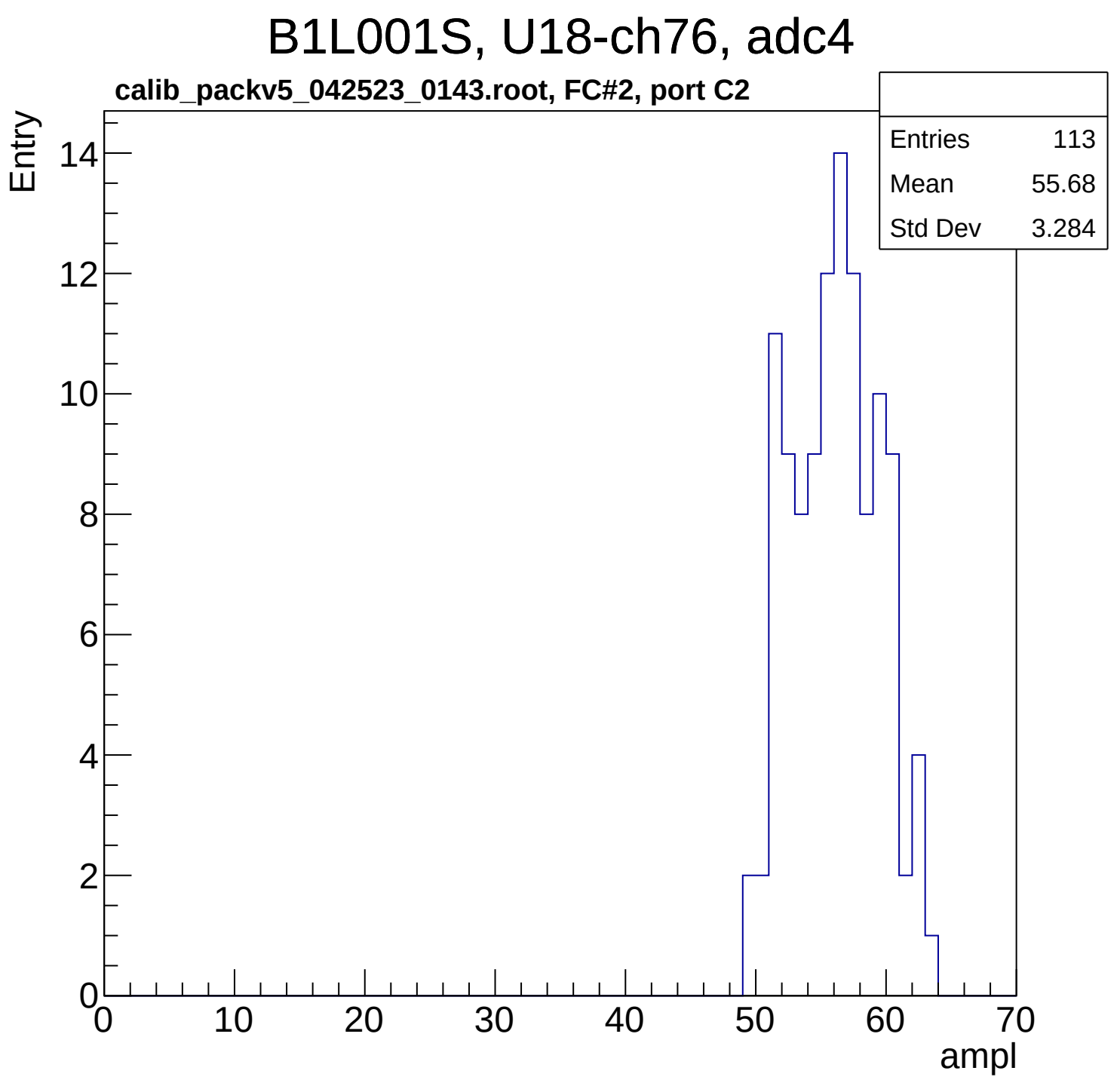

B1L001S, U18-ch75, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 4
Mean 21.75
Std Dev 25.75
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

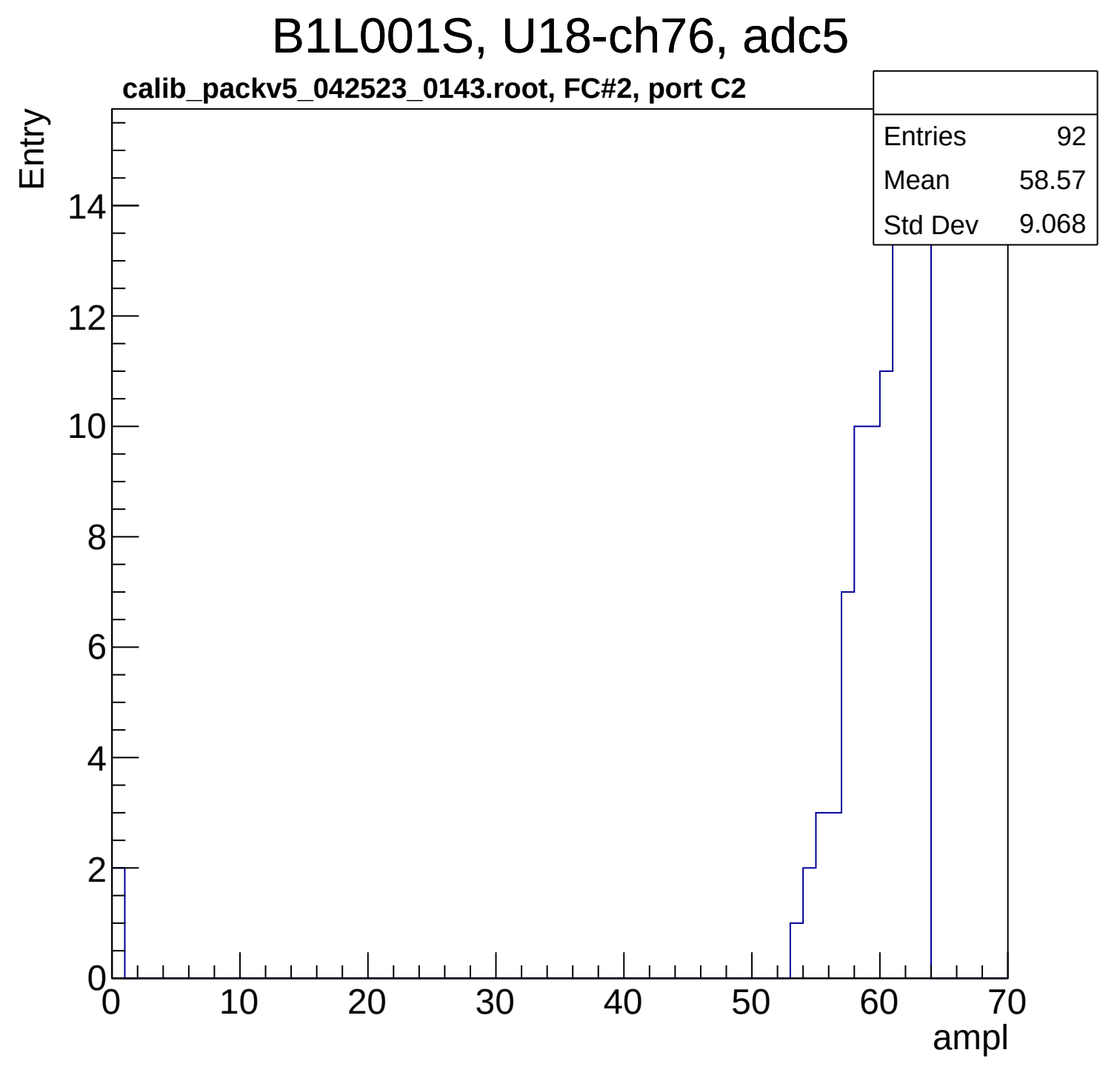

B1L001S, U18-ch76, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 136
Mean 31.38
Std Dev 4.069
Gaus mean : 31.7713
Gaus Width: 3.4347
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

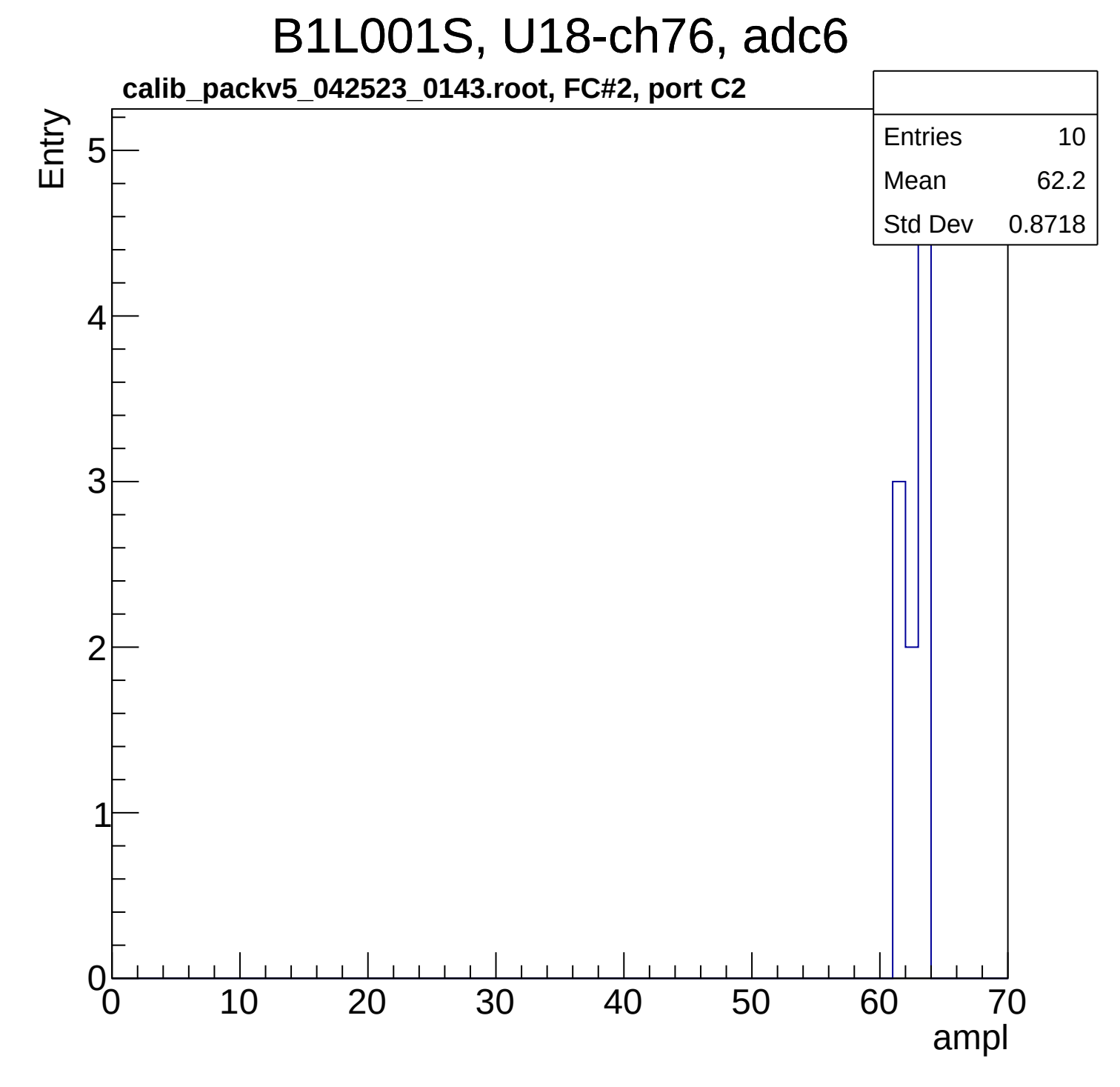

B1L001S, U18-ch76, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 83
Mean 37.14
Std Dev 2.786
Gaus mean : 37.5355
Gaus Width: 2.9478
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

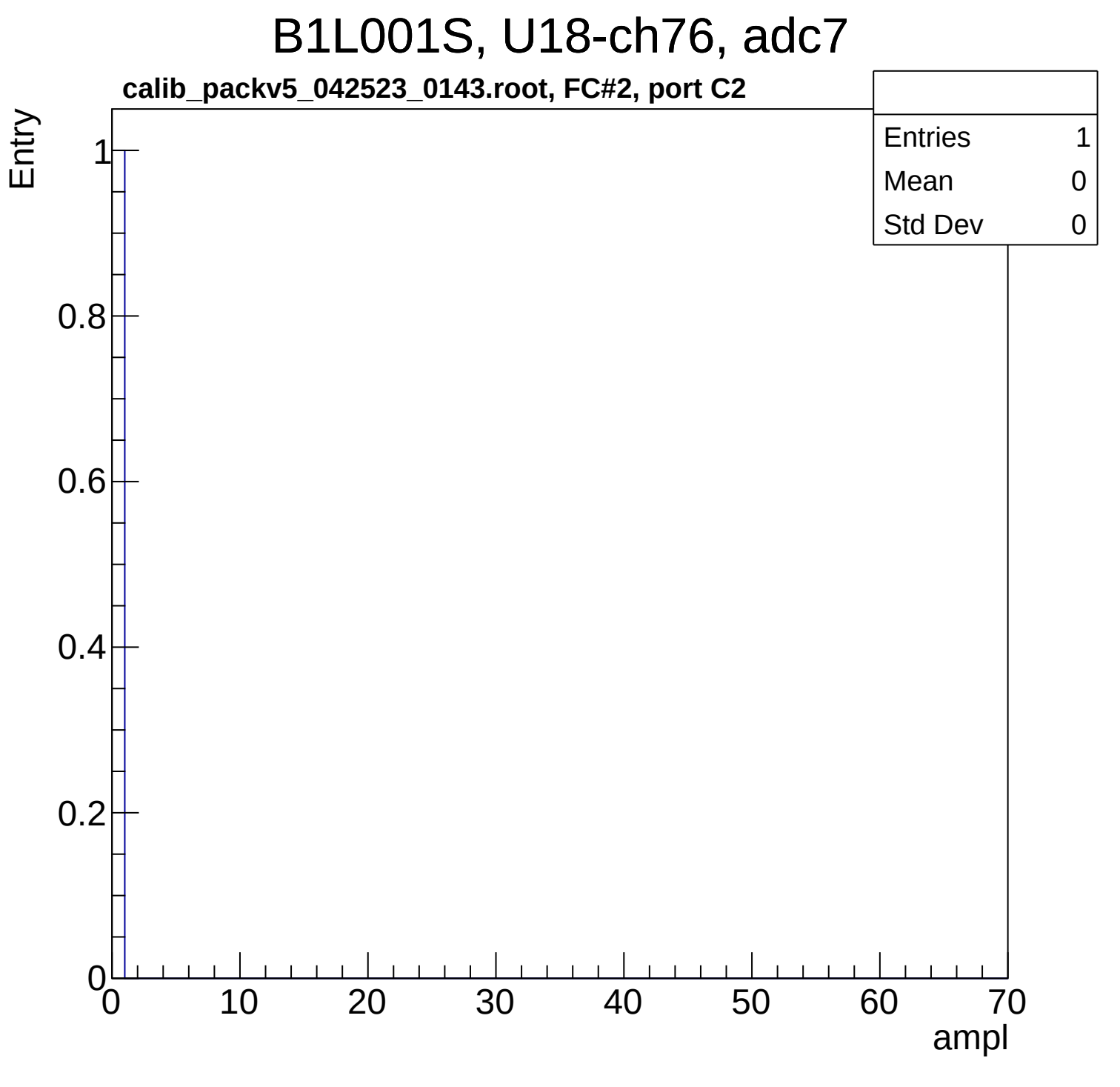

B1L001S, U18-ch76, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 158
Mean 43.23
Std Dev 3.328
Gaus mean : 43.7828
Gaus Width: 3.7117
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

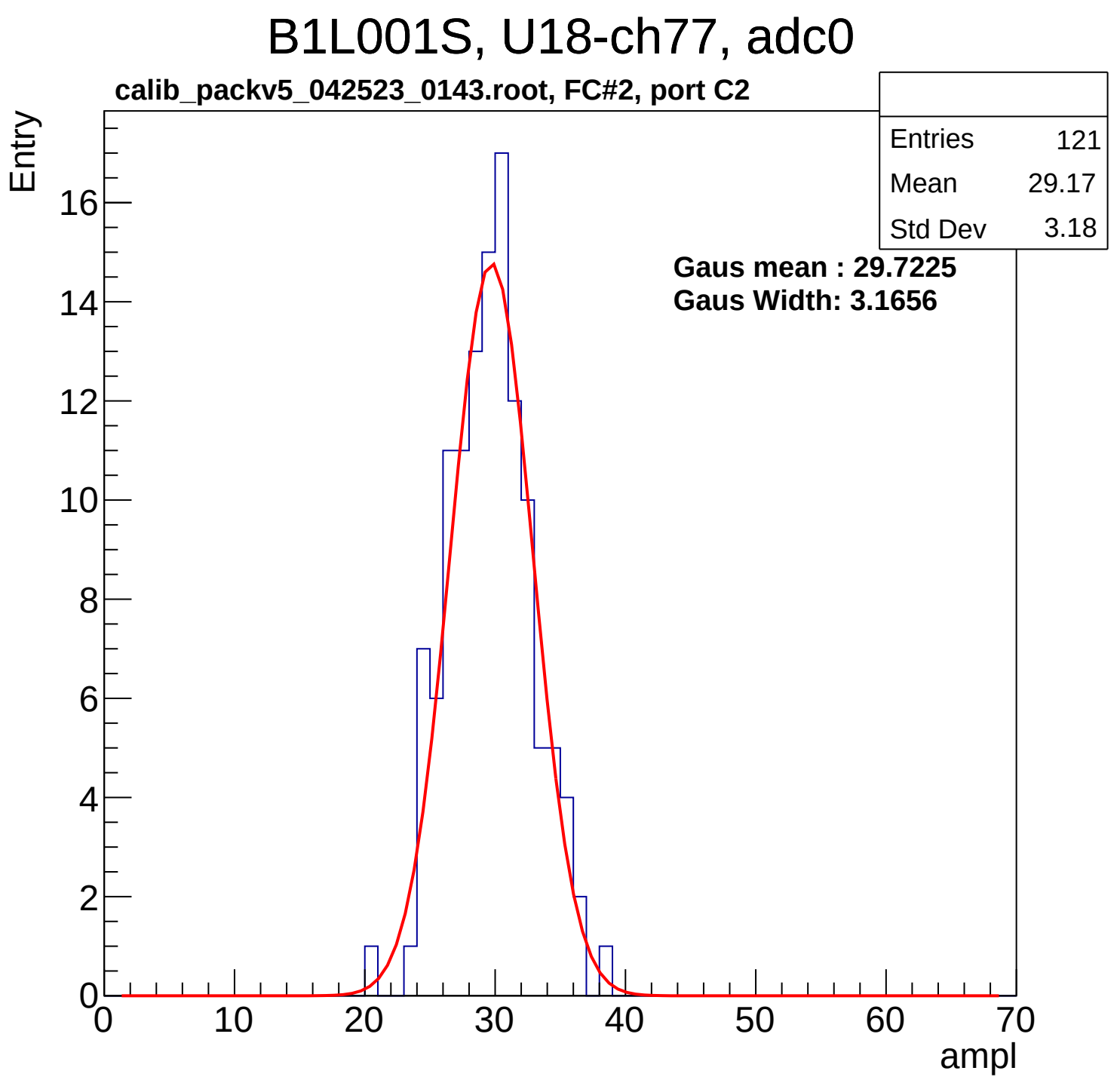

B1L001S, U18-ch76, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 115
Mean 50.11
Std Dev 3.464
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

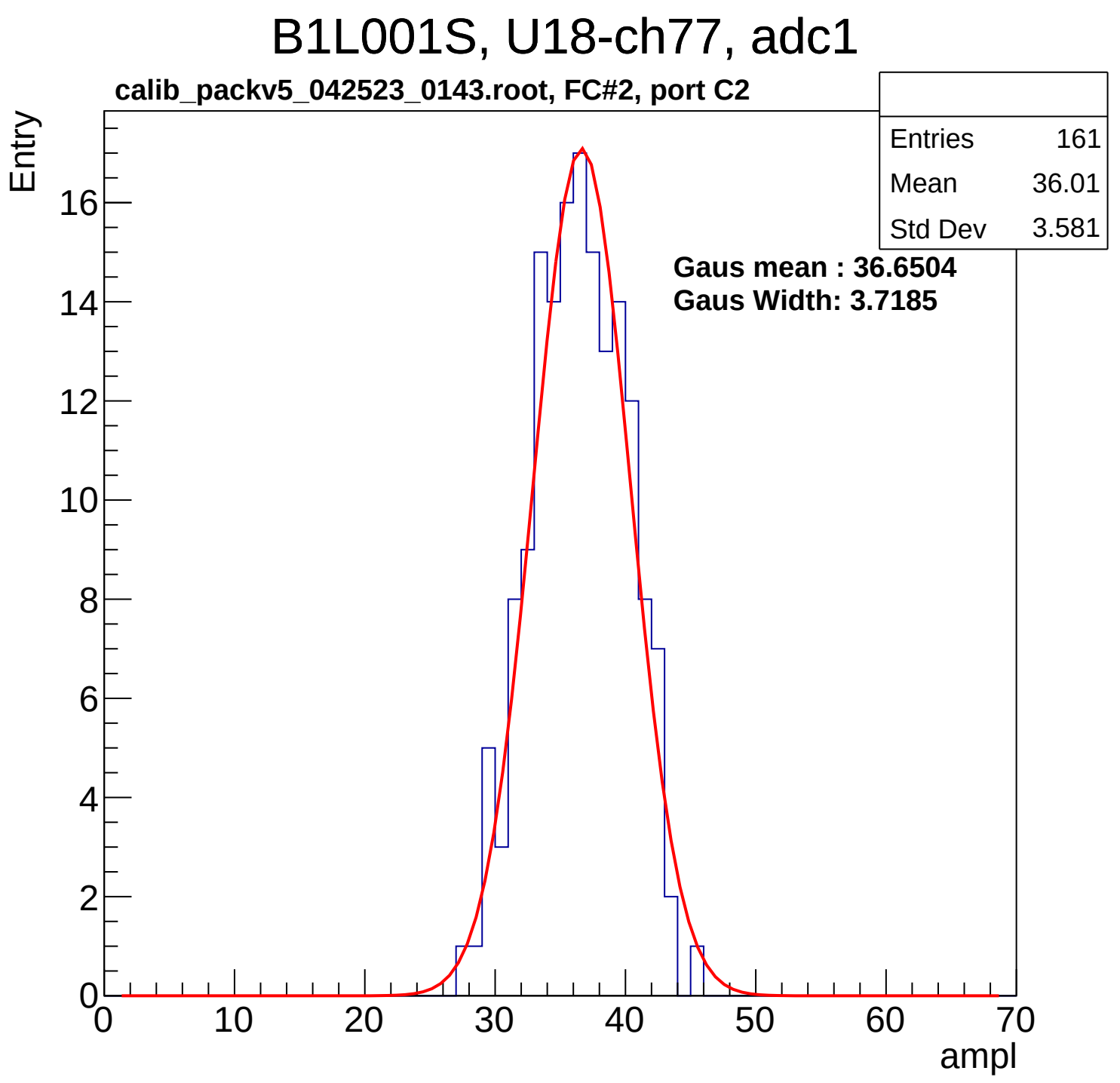

B1L001S, U18-ch76, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 113
Mean 55.68
Std Dev 3.284
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

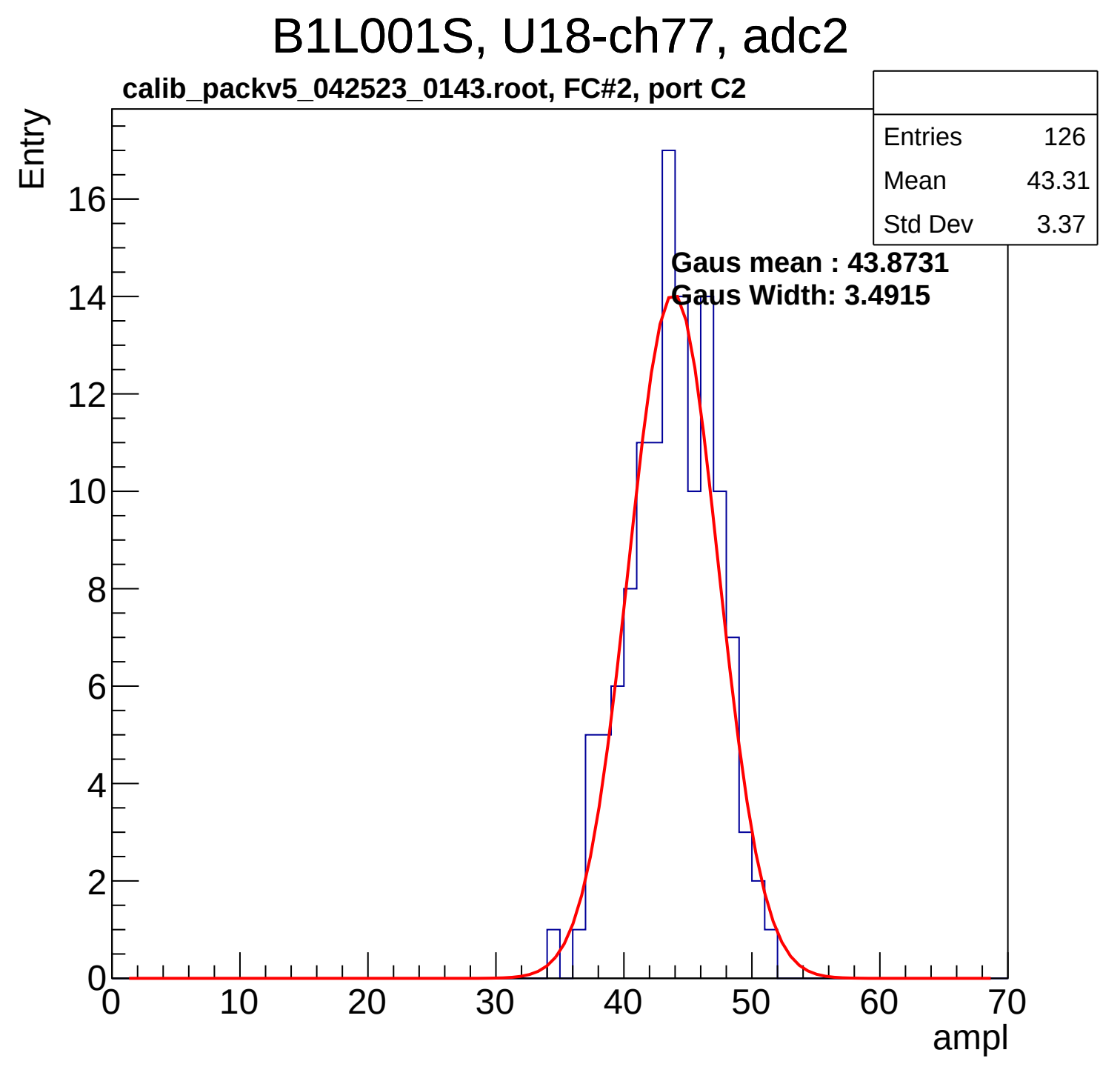

B1L001S, U18-ch76, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 92
Mean 58.57
Std Dev 9.068
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl

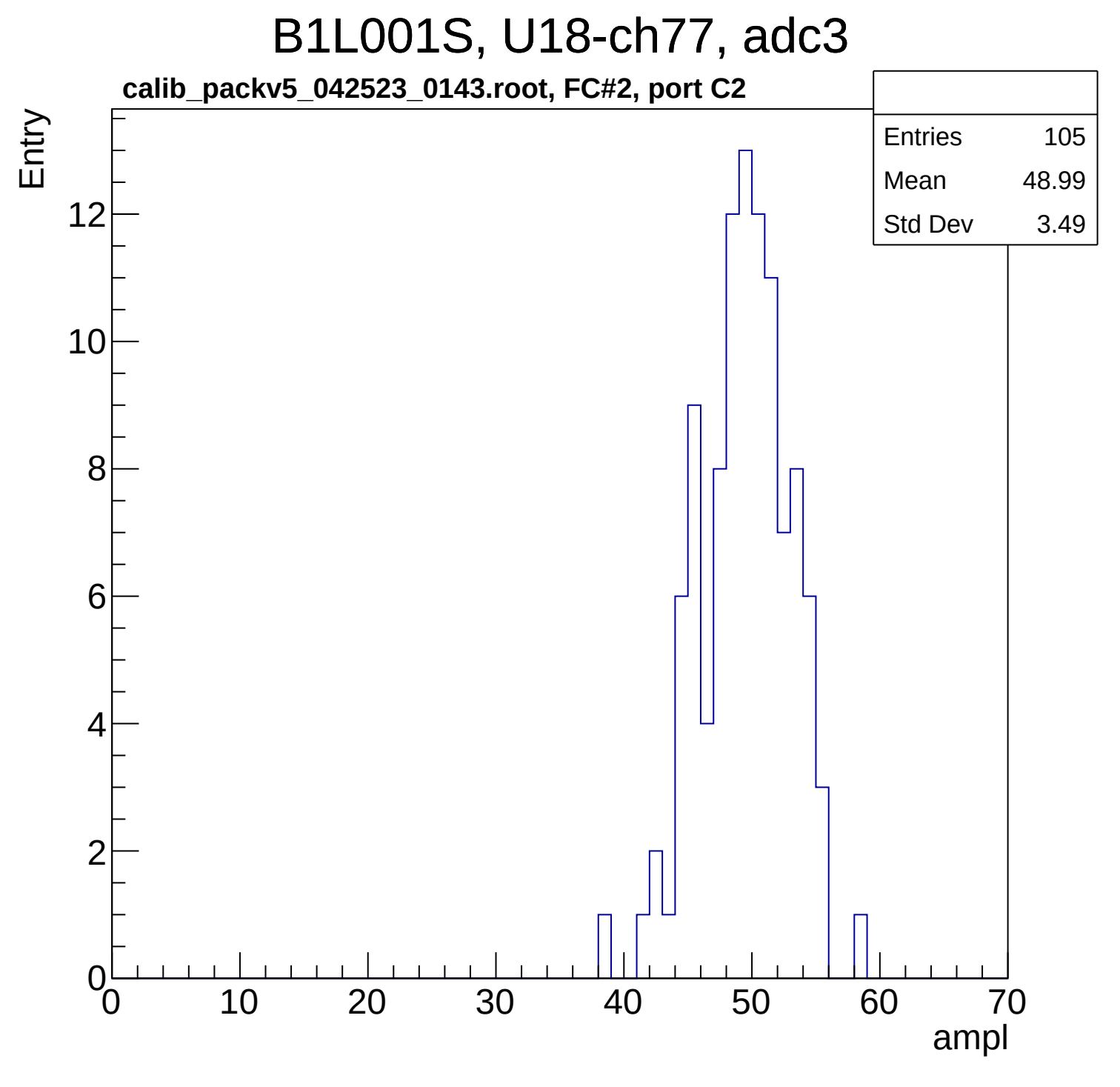

B1L001S, U18-ch76, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 10
Mean 62.2
Std Dev 0.8718
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

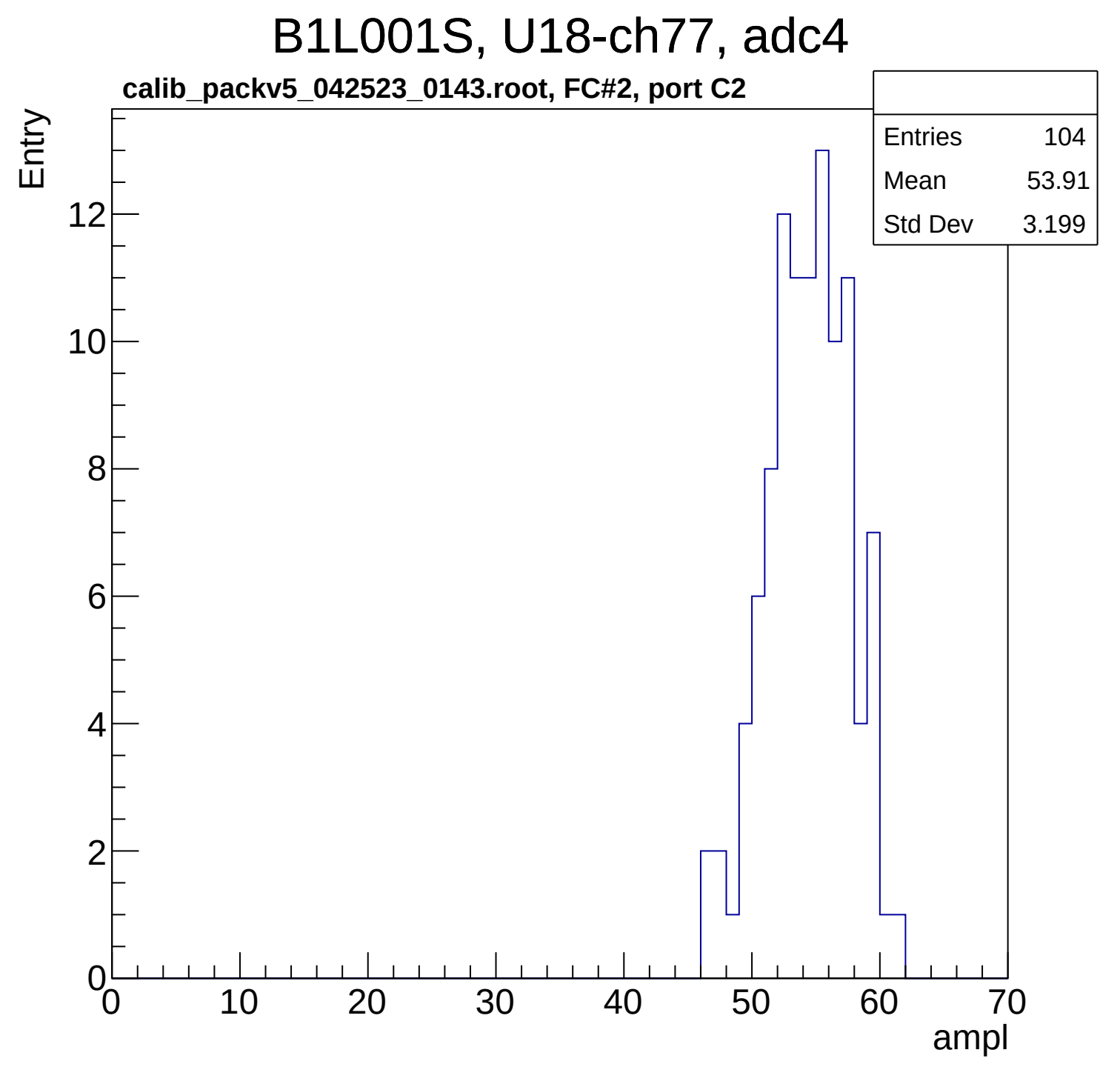

B1L001S, U18-ch76, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

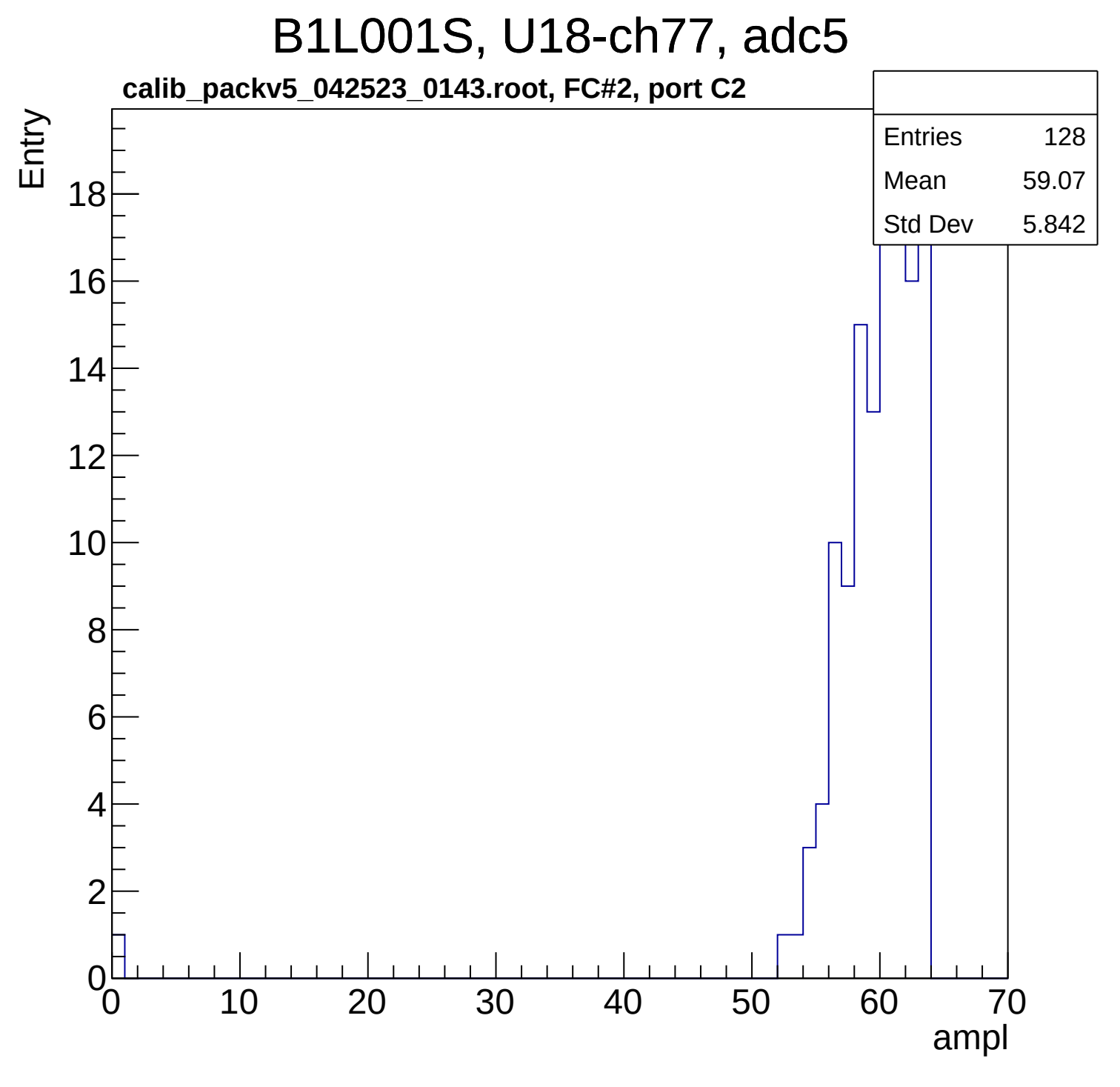

B1L001S, U18-ch77, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 121
Mean 29.17
Std Dev 3.18
Gaus mean : 29.7225
Gaus Width: 3.1656
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

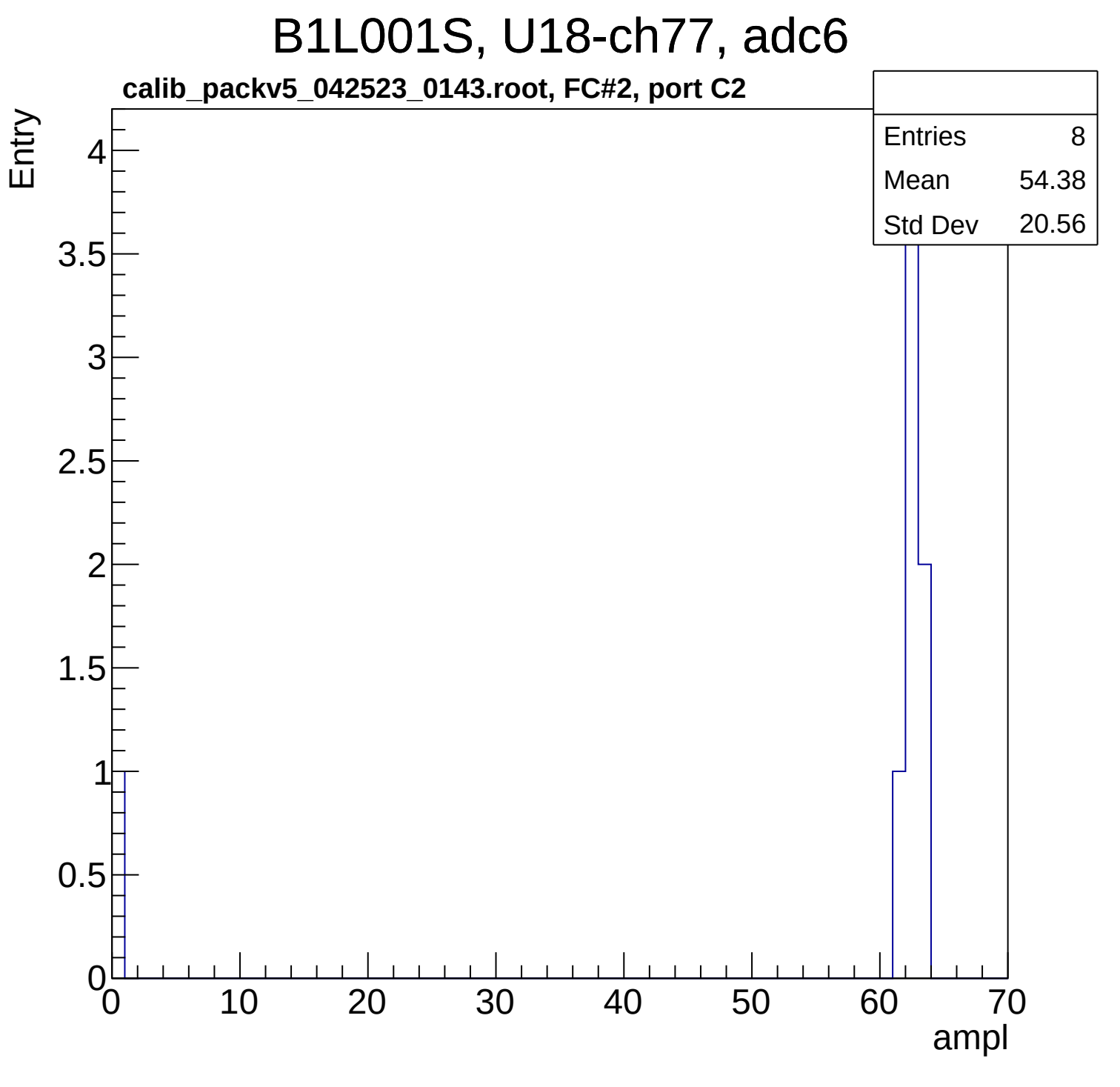

B1L001S, U18-ch77, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 161
Mean 36.01
Std Dev 3.581
Gaus mean : 36.6504
Gaus Width: 3.7185
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

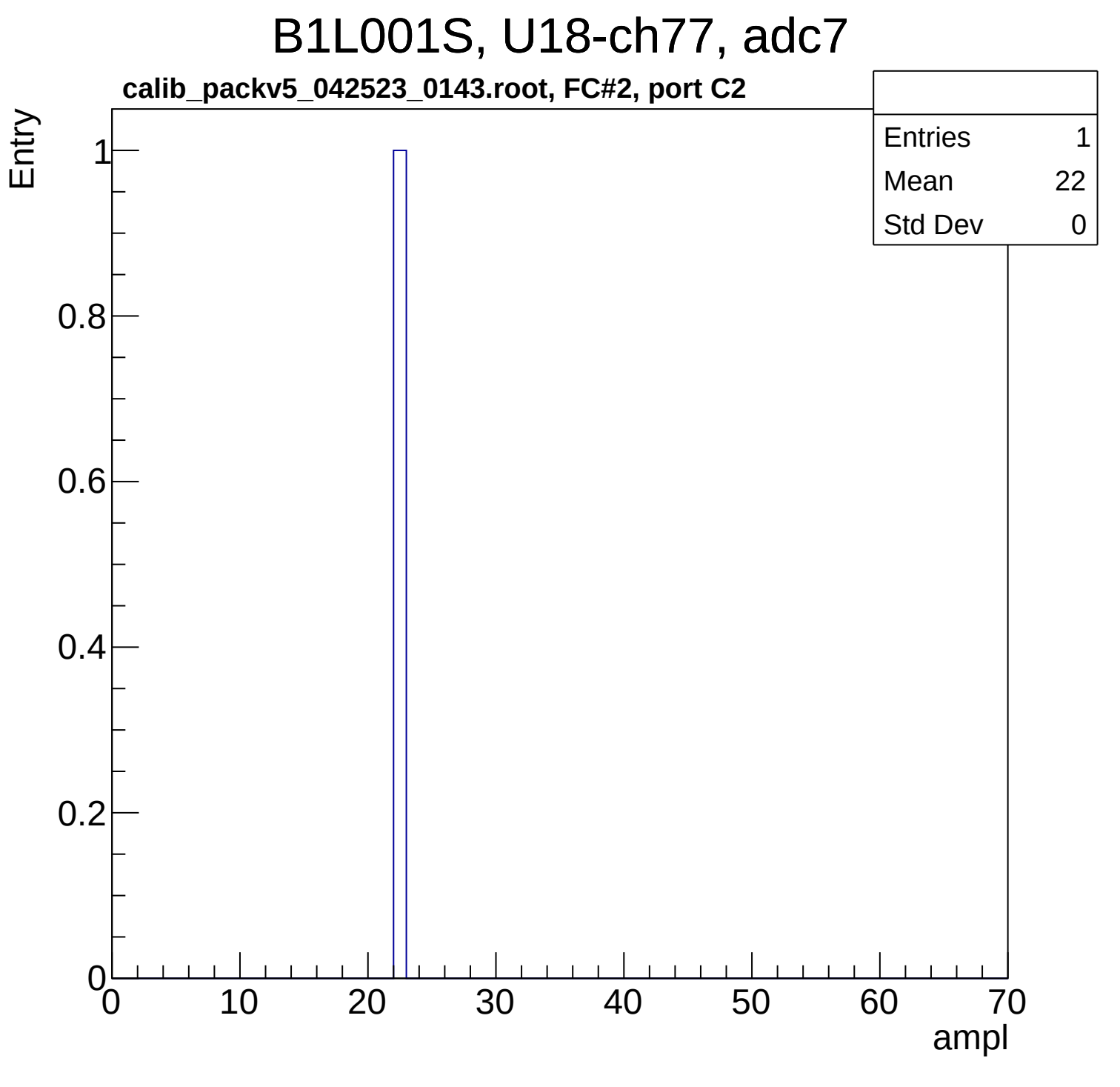

B1L001S, U18-ch77, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 126
Mean 43.31
Std Dev 3.37
Gaus mean : 43.8731
Gaus Width: 3.4915
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

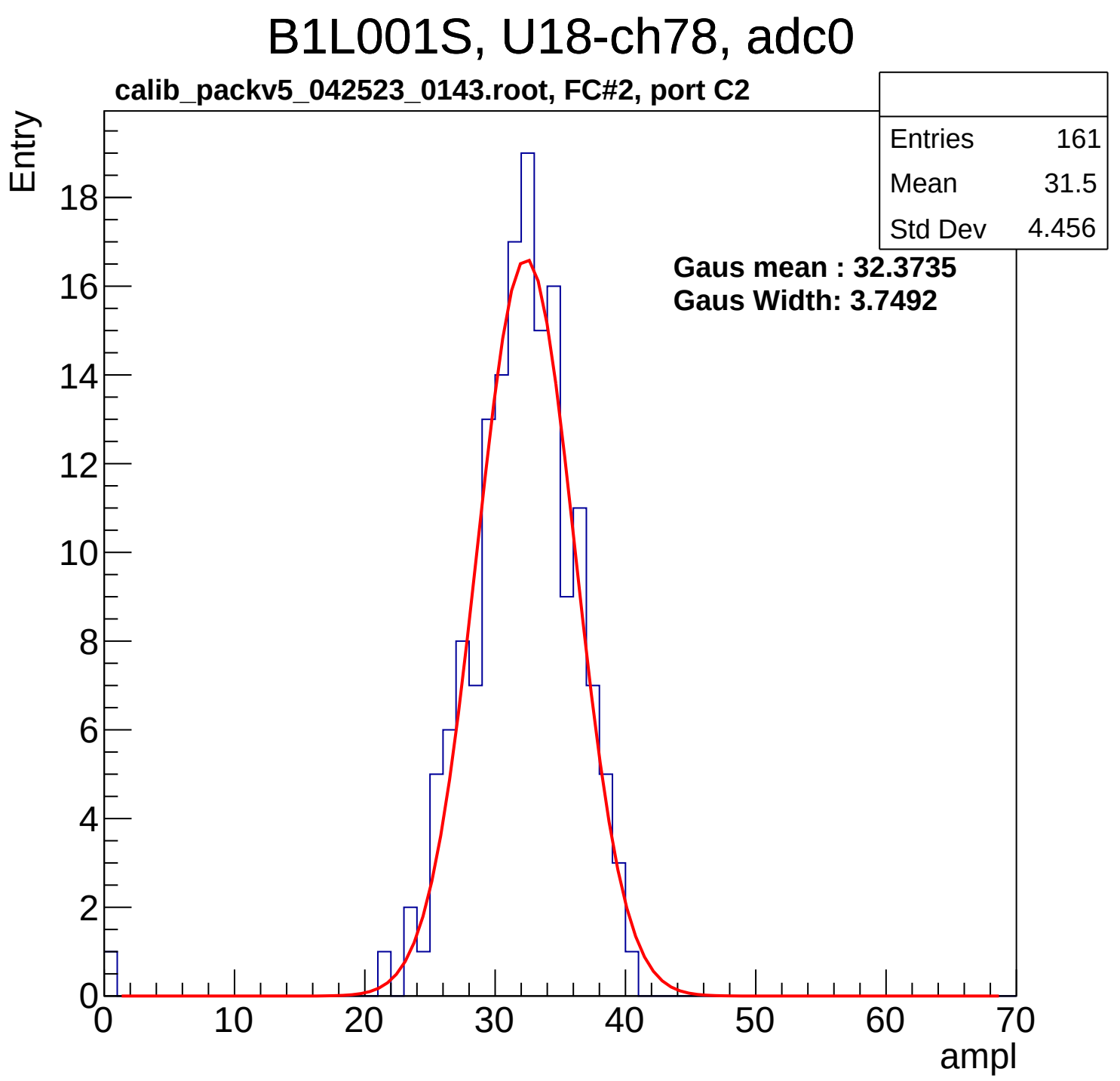

B1L001S, U18-ch77, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 105
Mean 48.99
Std Dev 3.49
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl

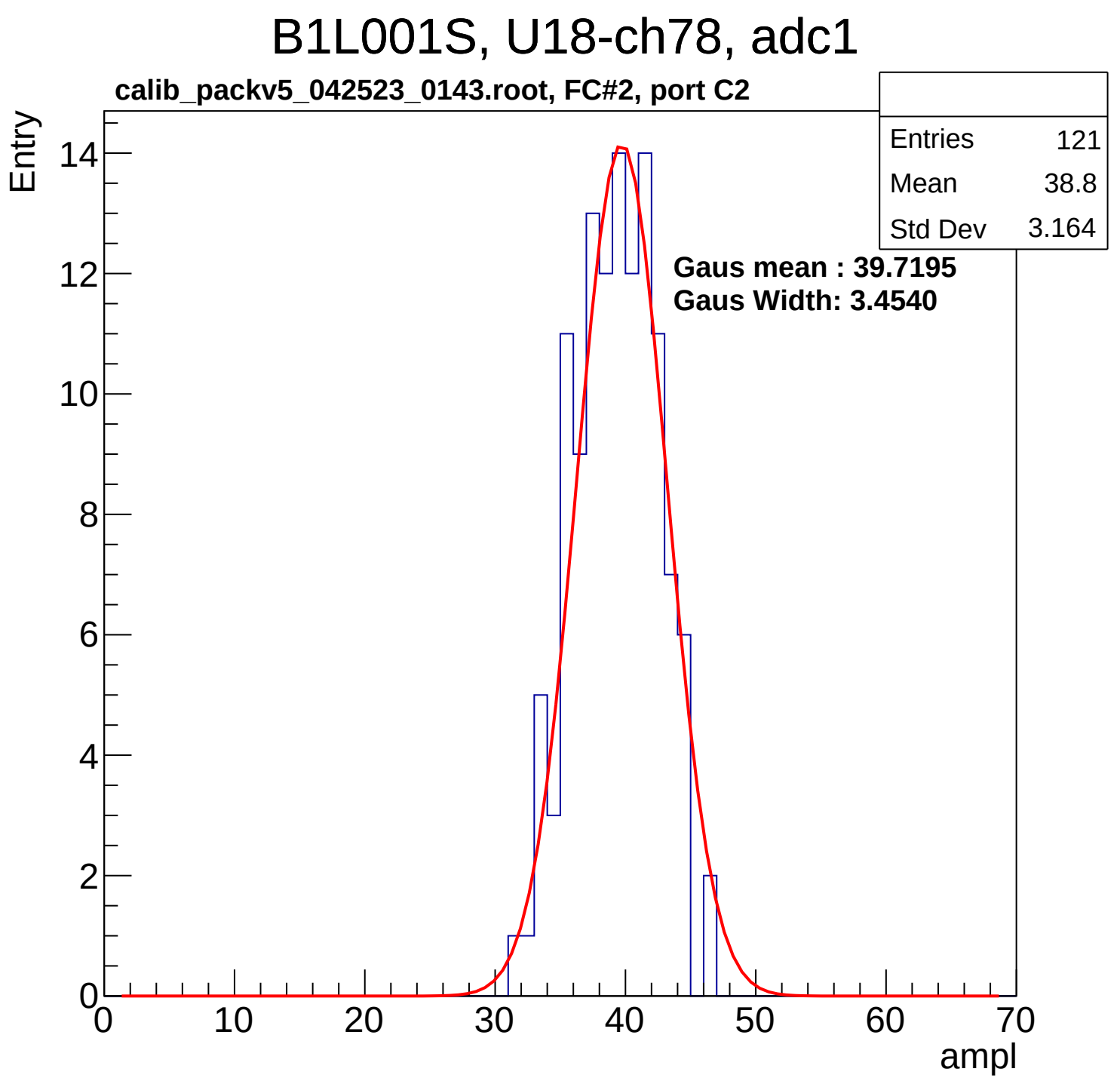

B1L001S, U18-ch77, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 104
Mean 53.91
Std Dev 3.199
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl

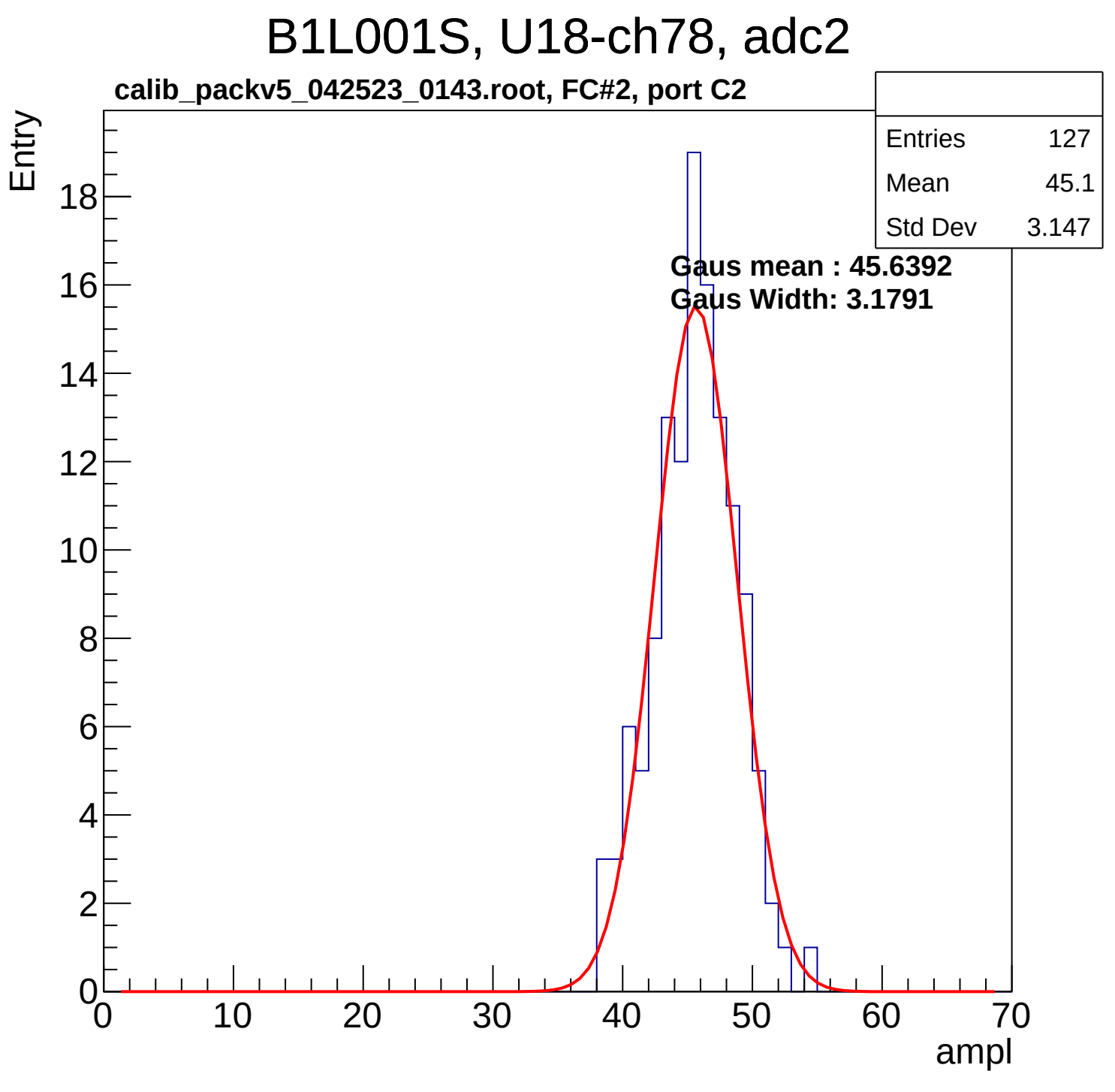

B1L001S, U18-ch77, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 128
Mean 59.07
Std Dev 5.842
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

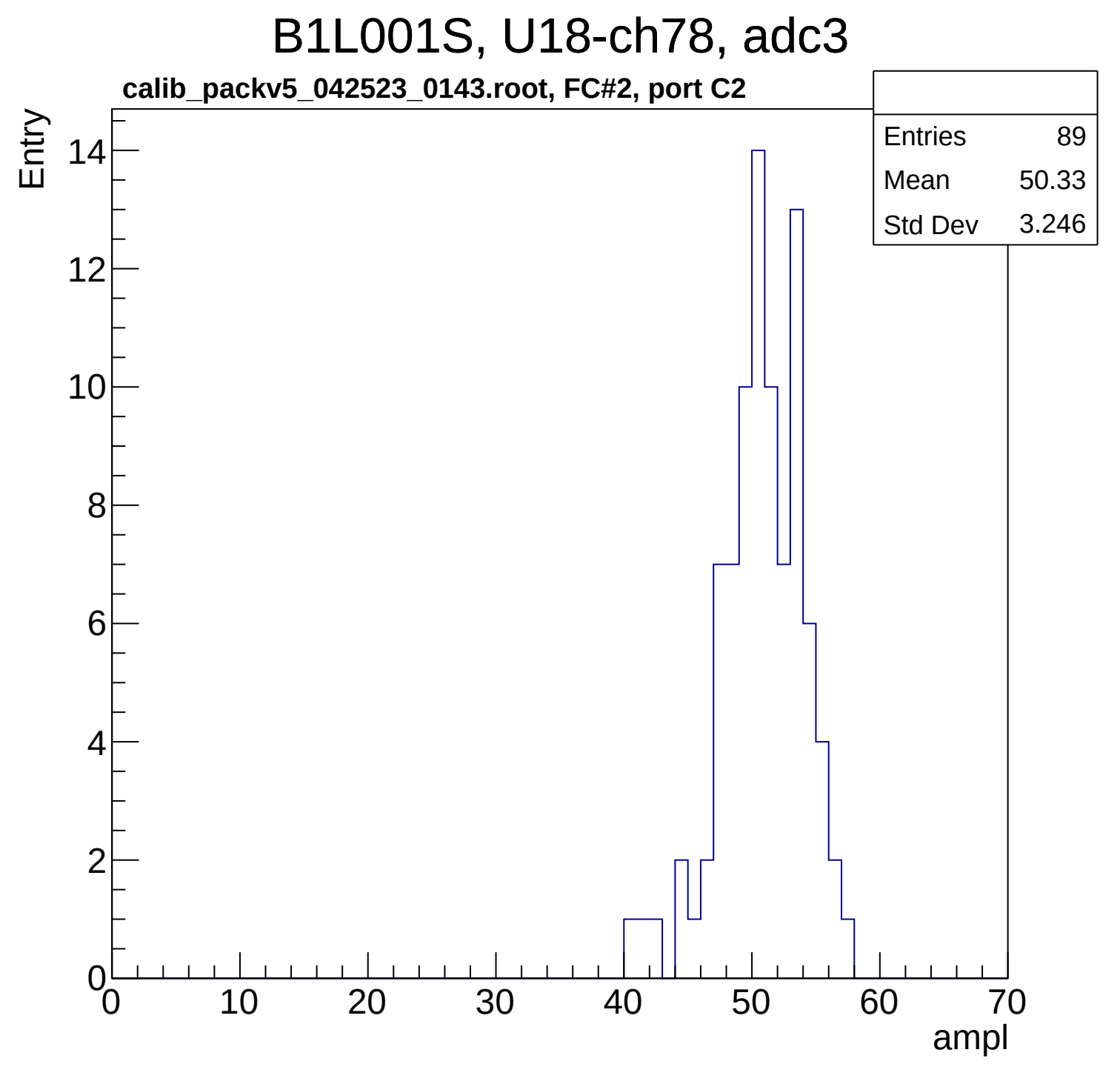

B1L001S, U18-ch77, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 8
Mean 54.38
Std Dev 20.56
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

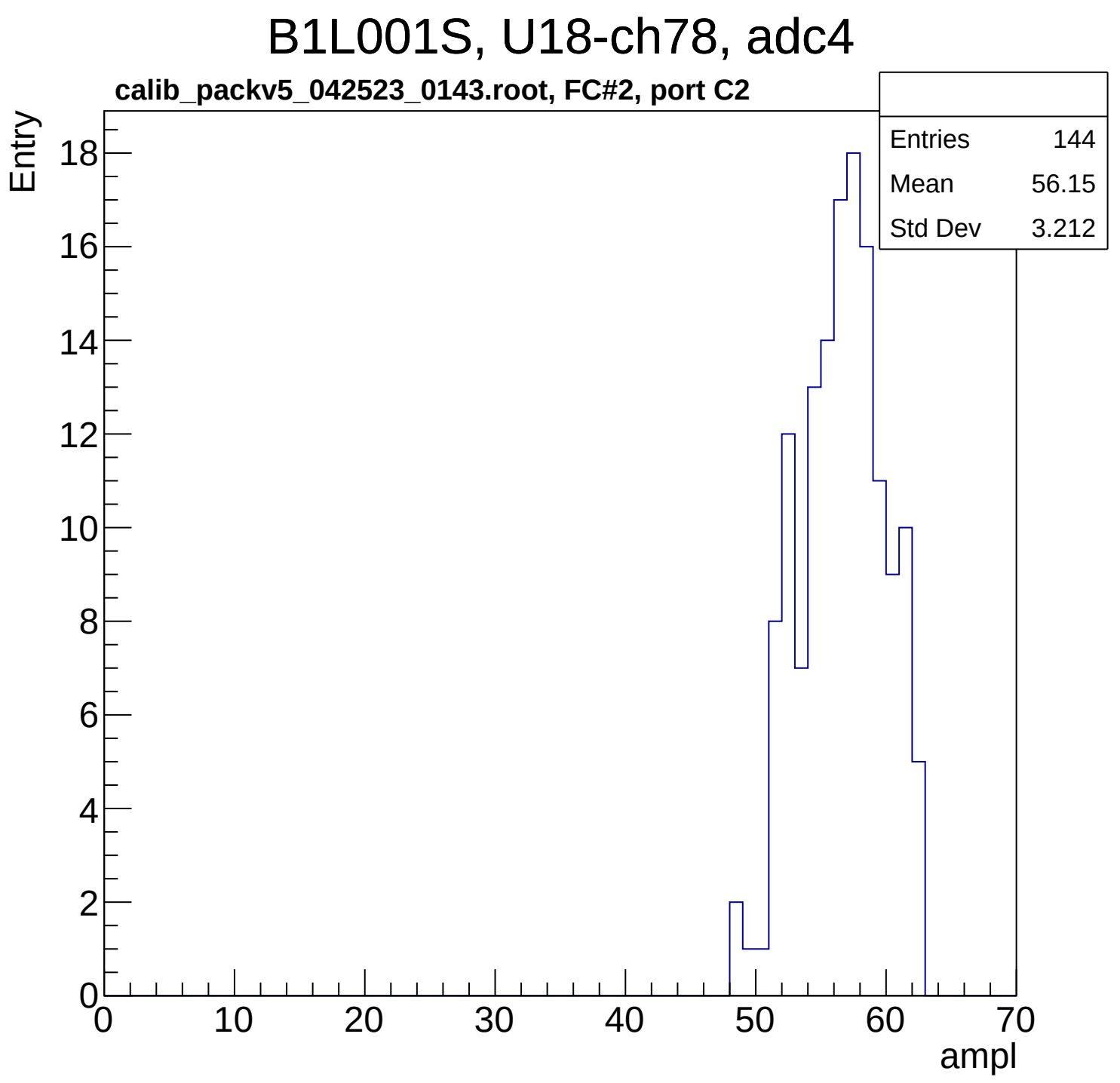

B1L001S, U18-ch77, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 22
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

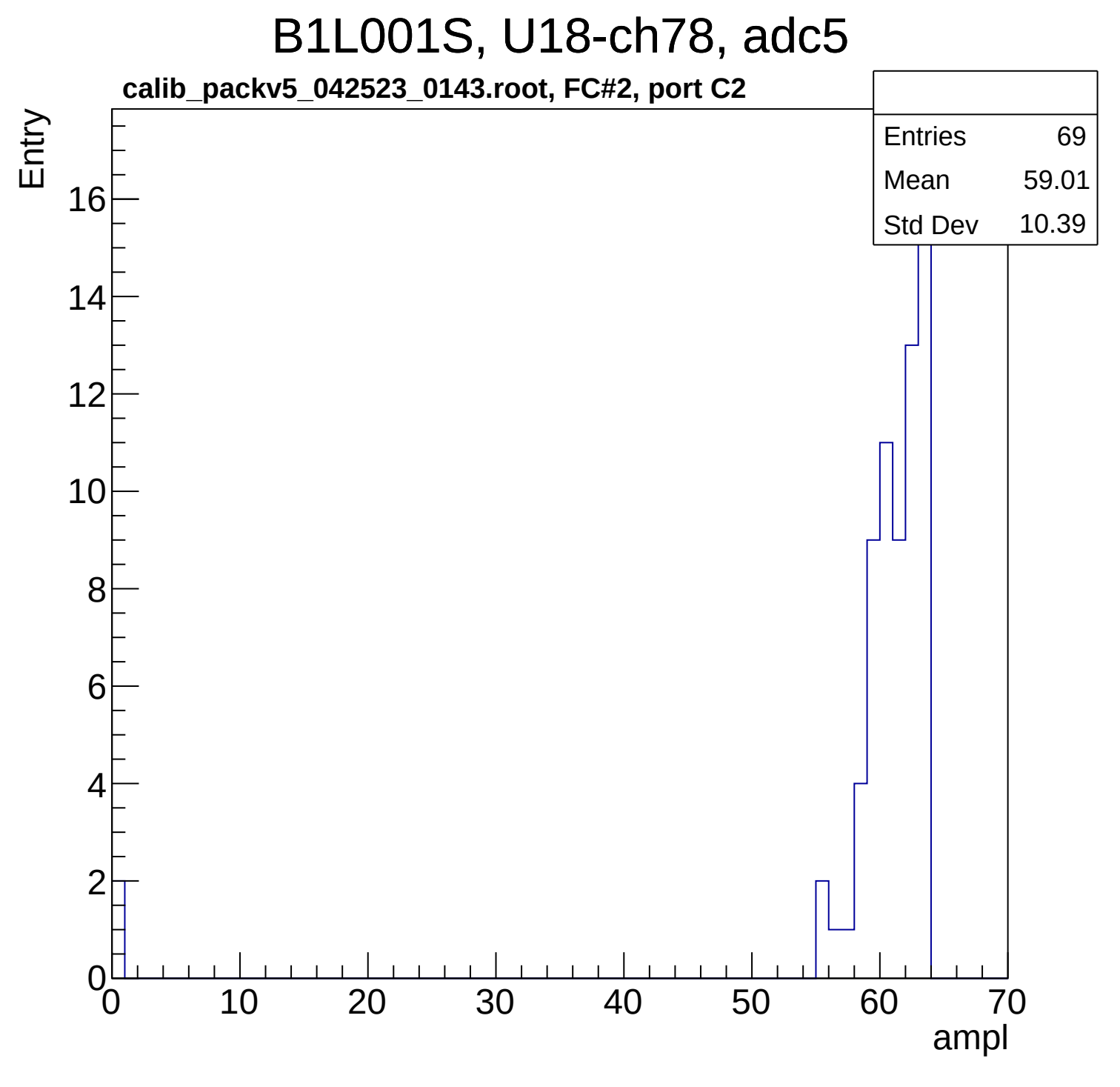

B1L001S, U18-ch78, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 161
Mean 31.5
Std Dev 4.456
Gaus mean : 32.3735
Gaus Width: 3.7492
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

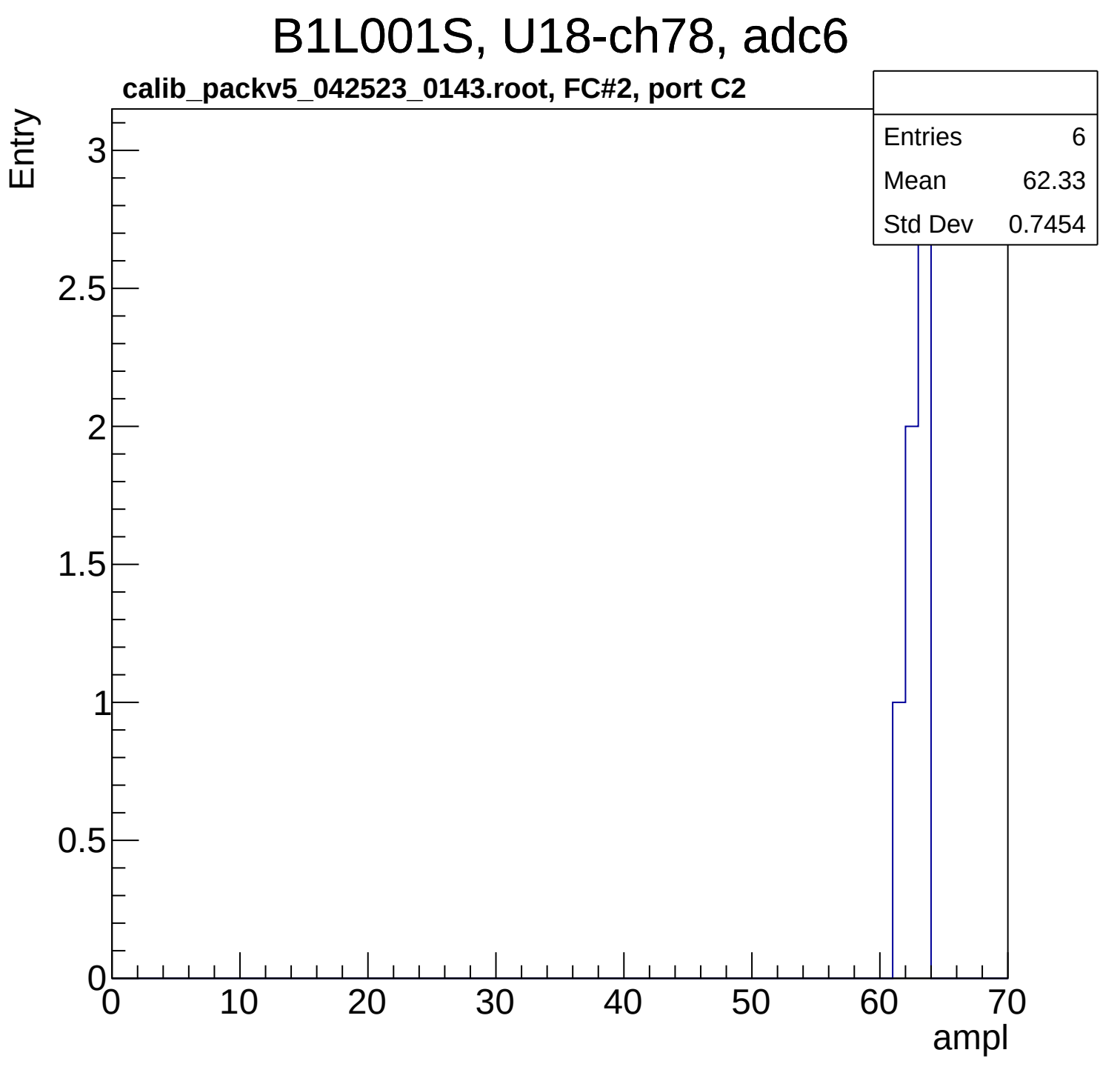

B1L001S, U18-ch78, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 121
Mean 38.8
Std Dev 3.164
Gaus mean : 39.7195
Gaus Width: 3.4540
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

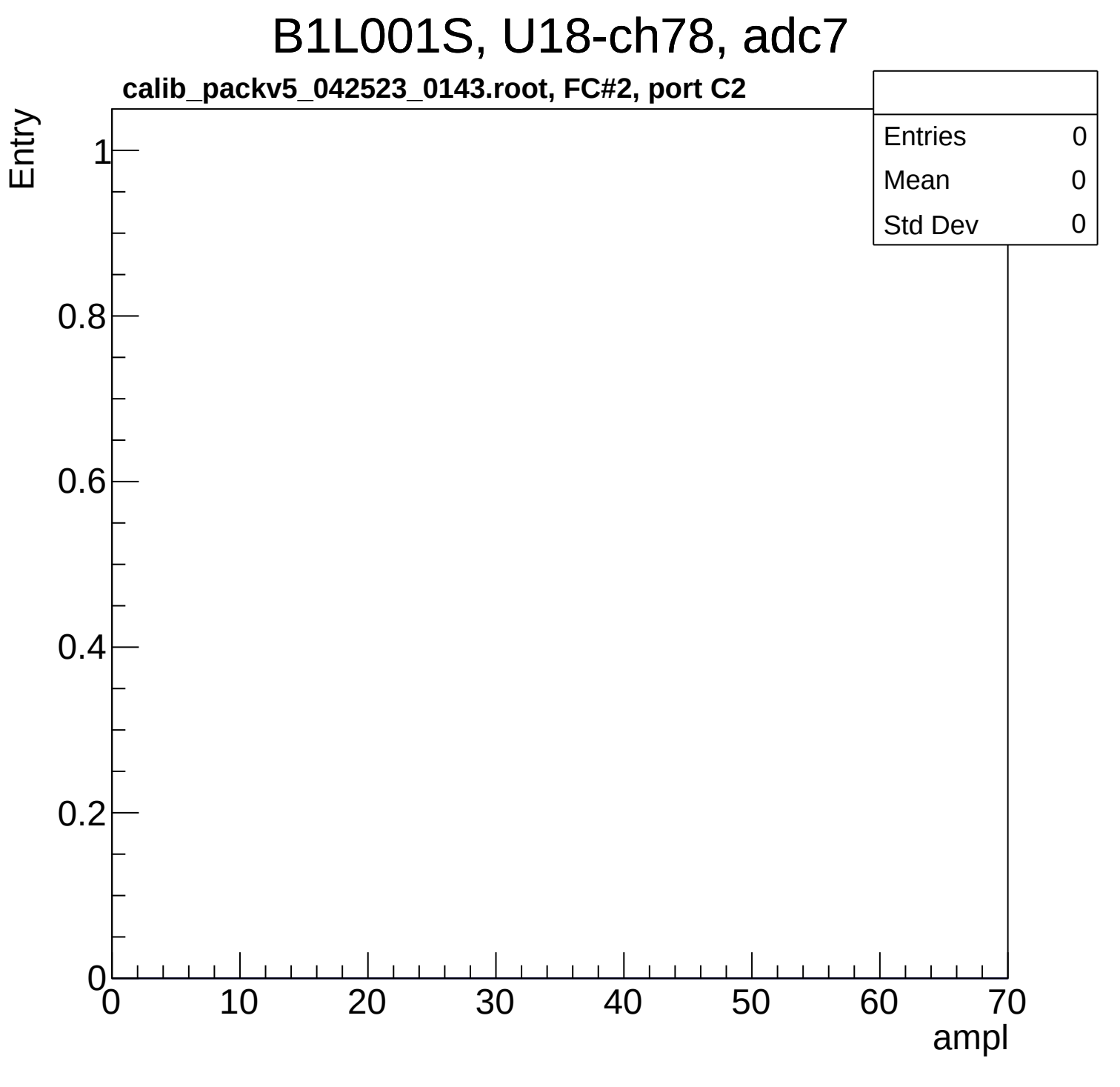

B1L001S, U18-ch78, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 127
Mean 45.1
Std Dev 3.147
Gaus mean : 45.6392
Gaus Width: 3.1791
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

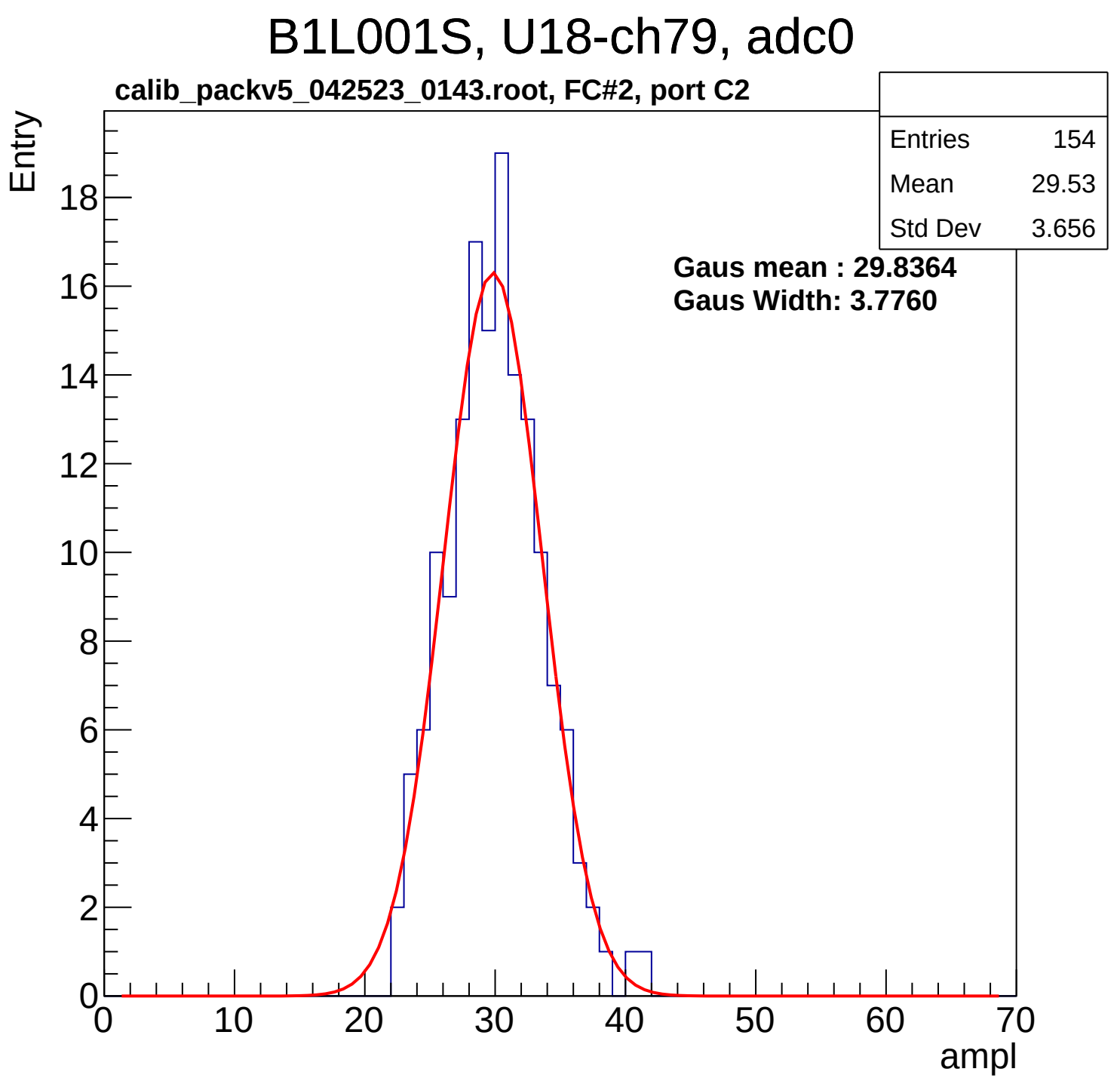

B1L001S, U18-ch78, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 89
Mean 50.33
Std Dev 3.246
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

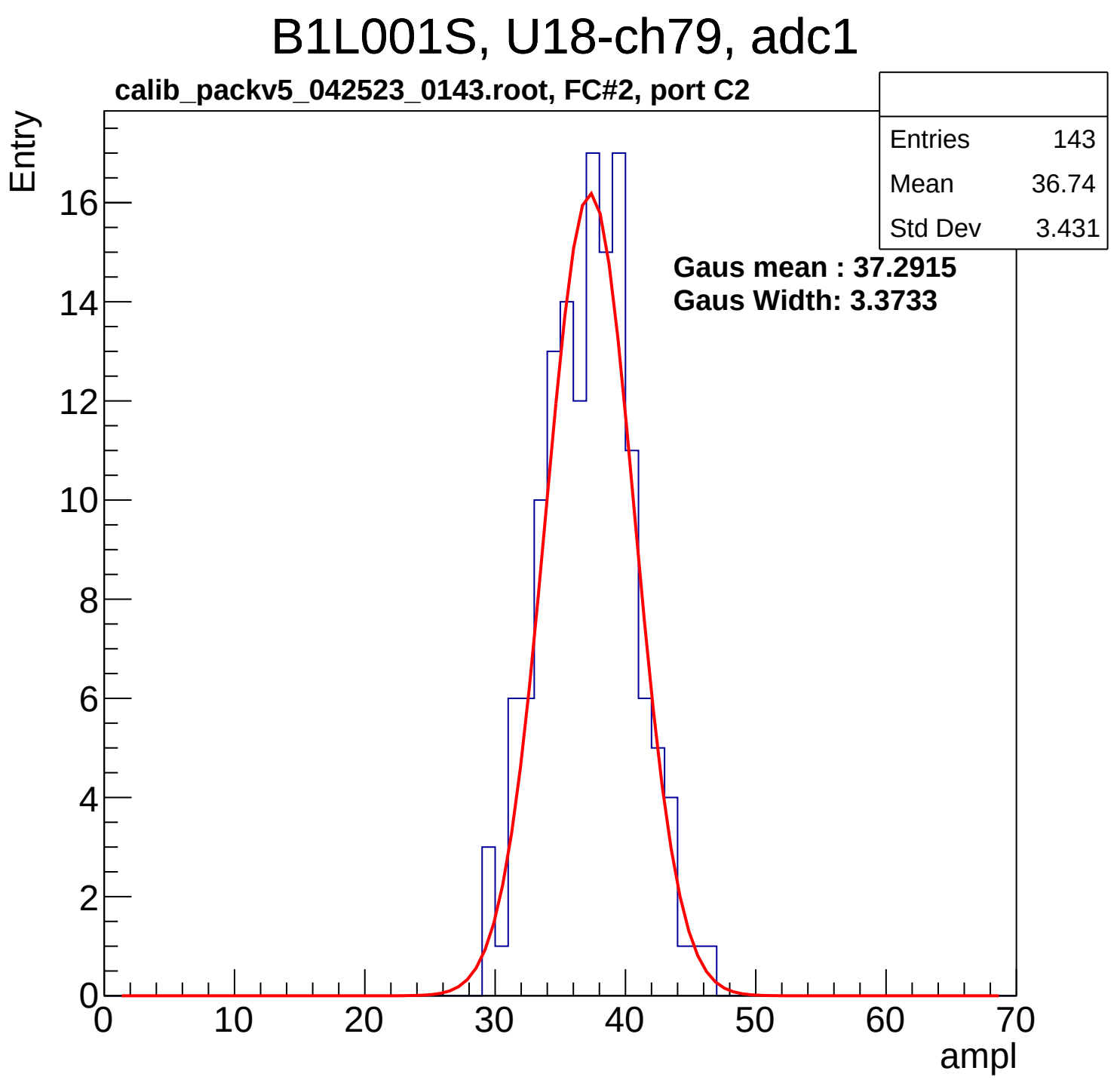

B1L001S, U18-ch78, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 144
Mean 56.15
Std Dev 3.212
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

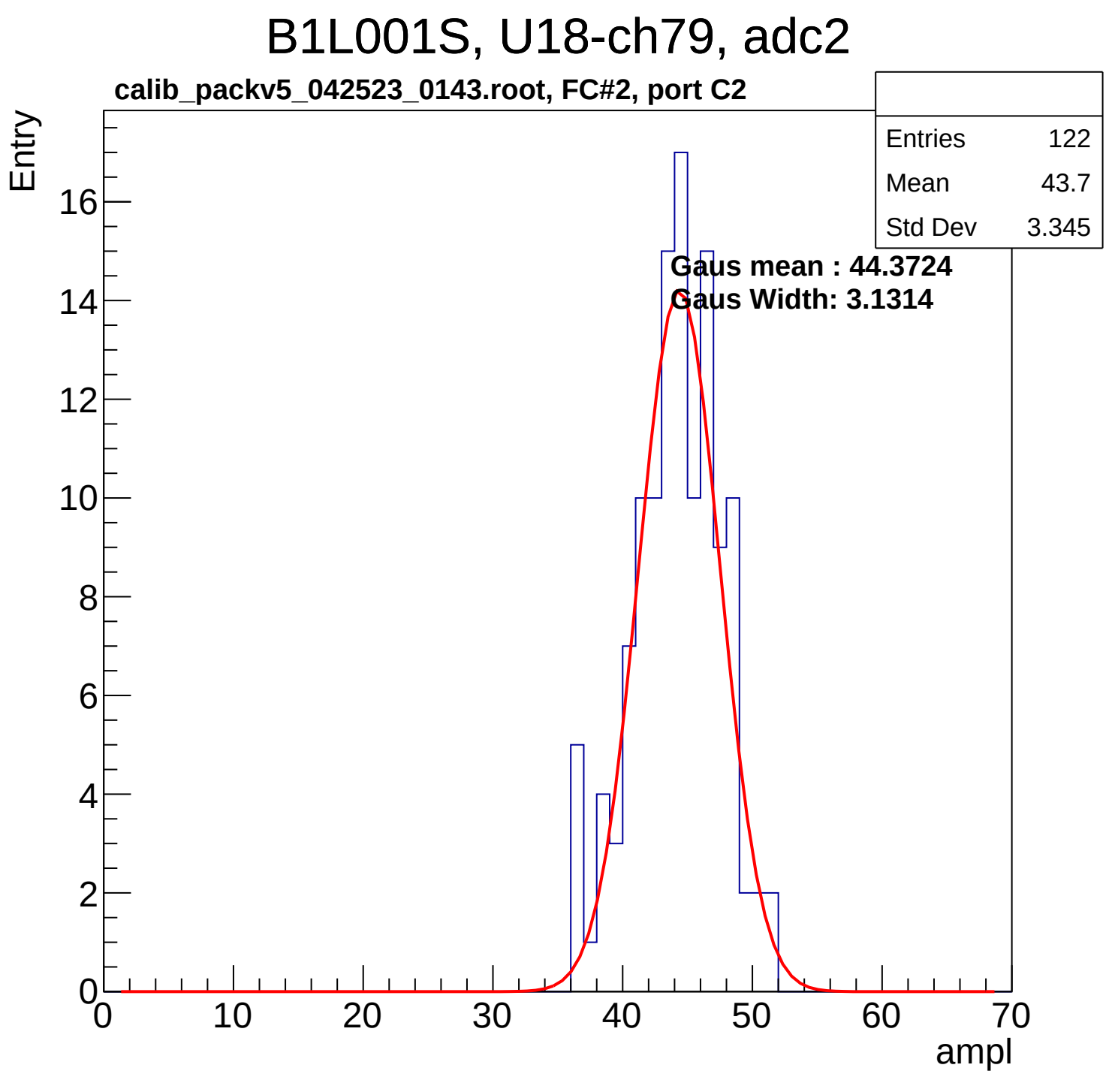

B1L001S, U18-ch78, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 69
Mean 59.01
Std Dev 10.39
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

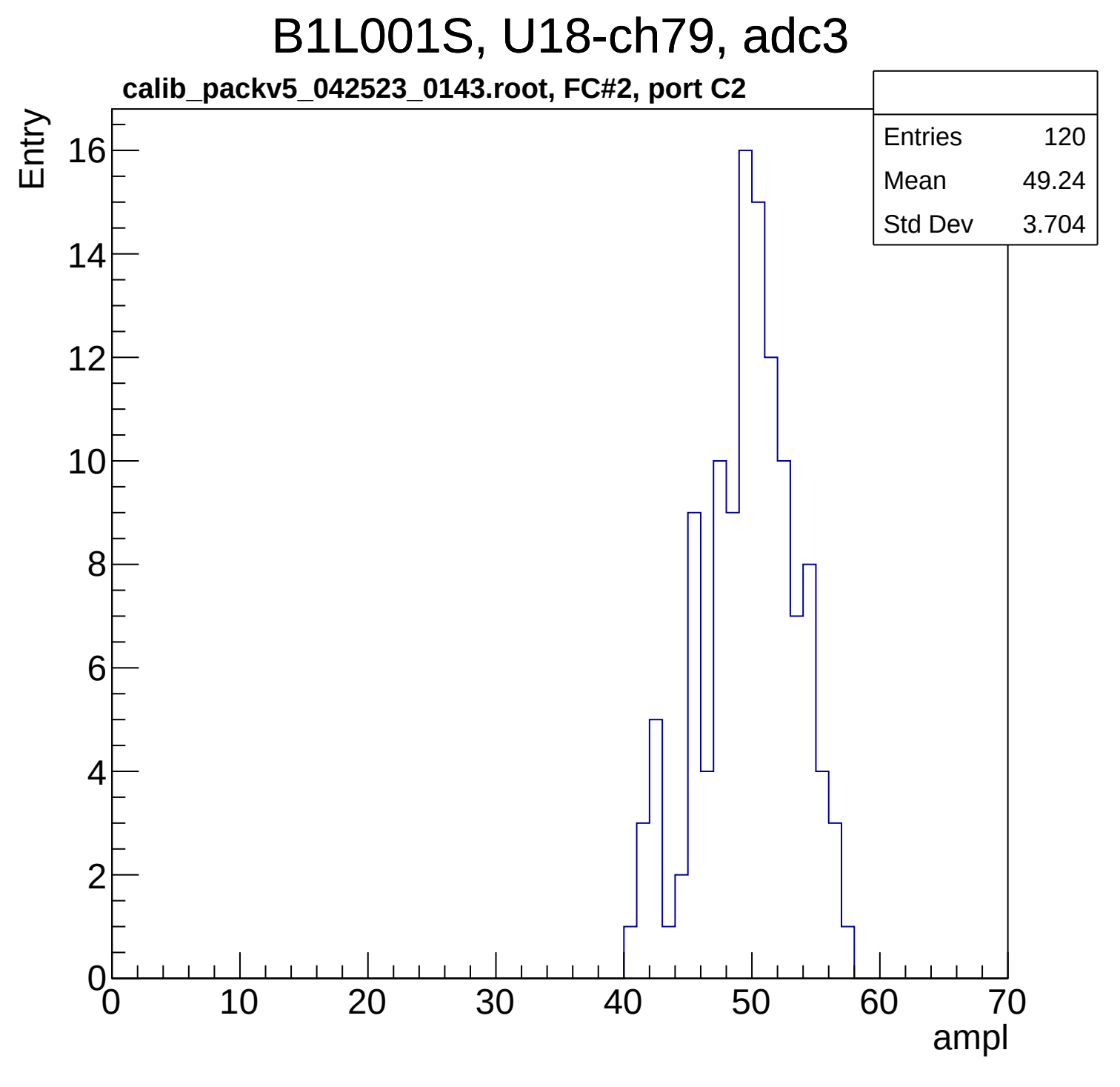

B1L001S, U18-ch78, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 6
Mean 62.33
Std Dev 0.7454
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

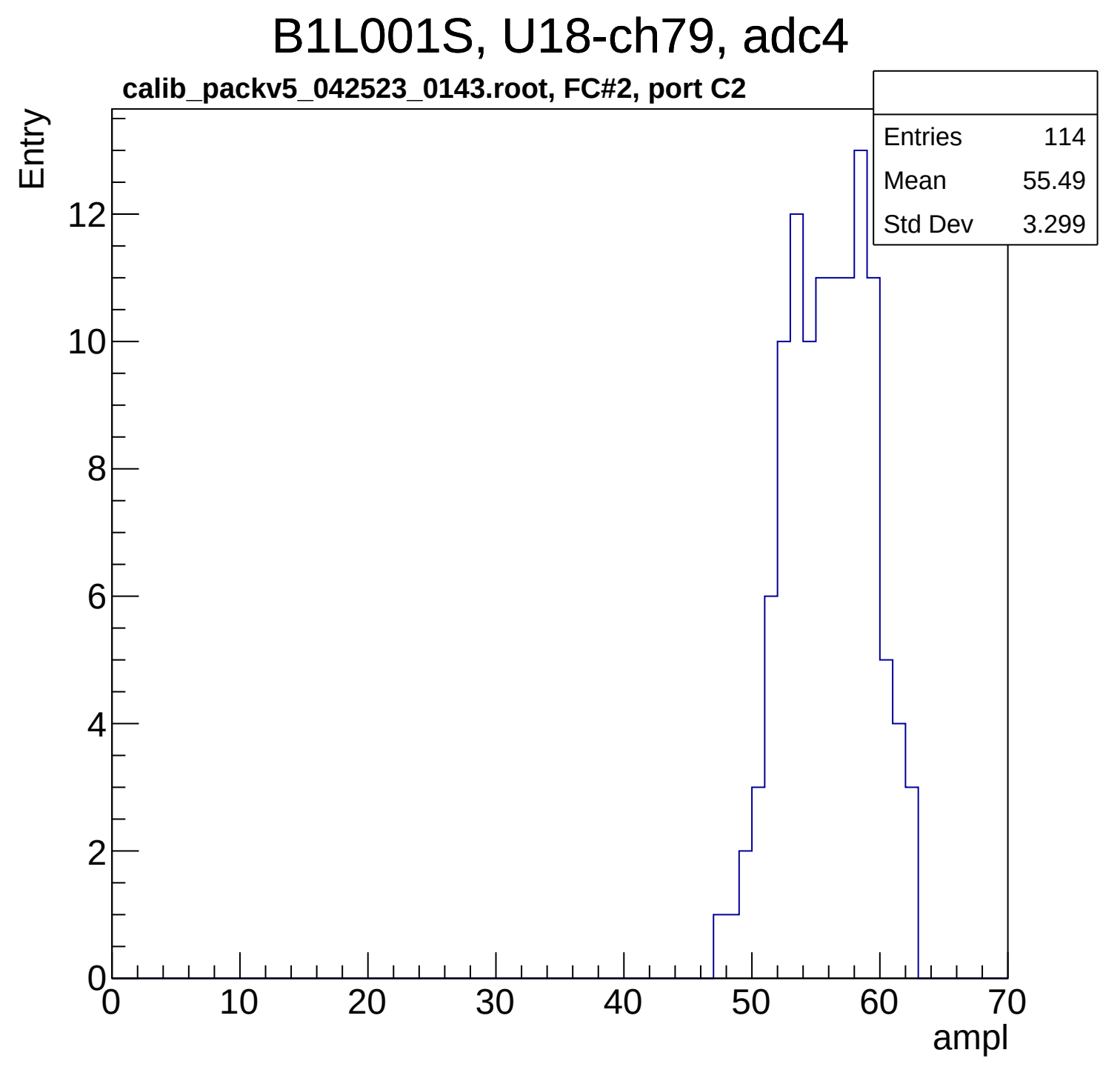

B1L001S, U18-ch78, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

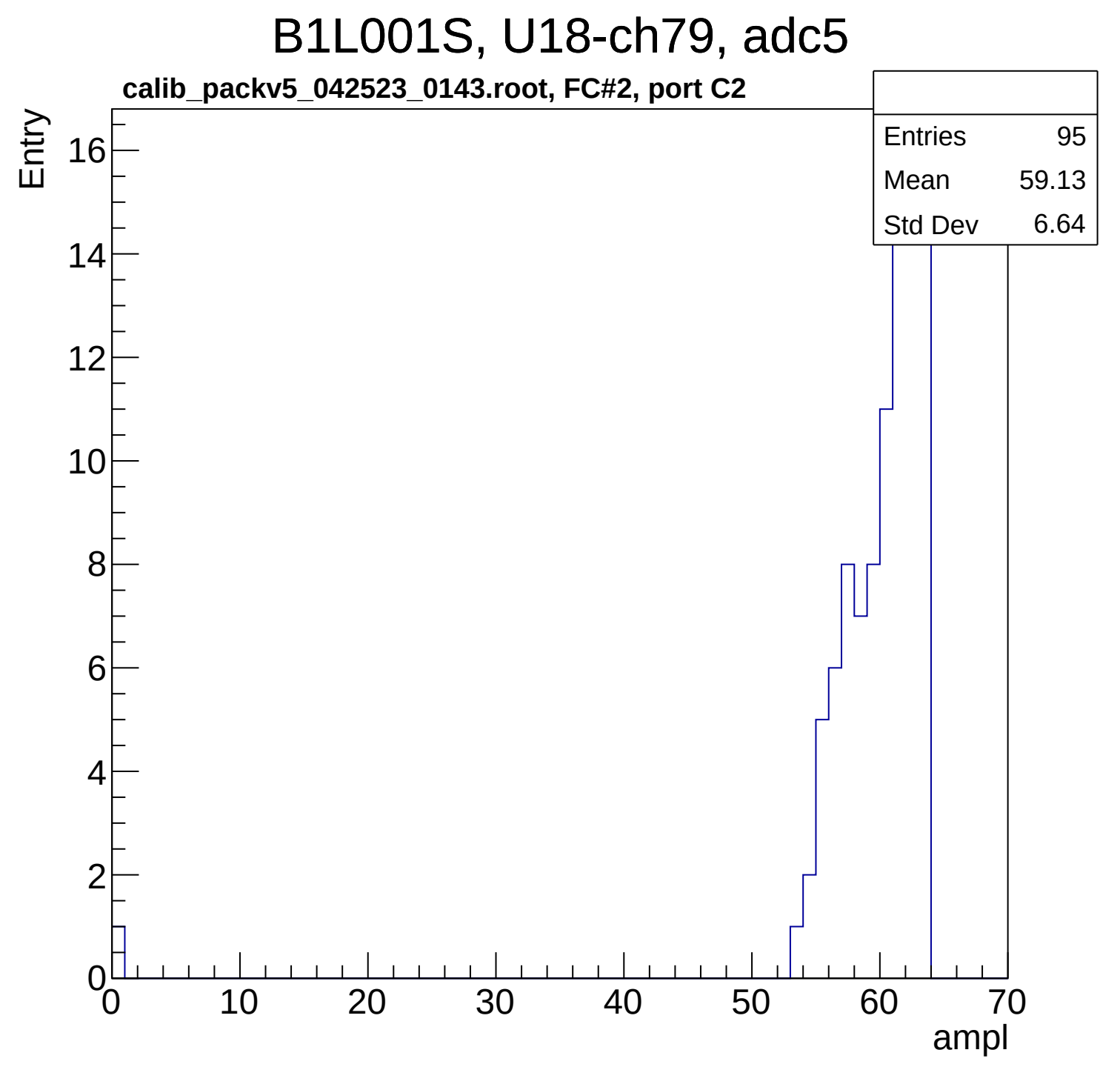

B1L001S, U18-ch79, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 154
Mean 29.53
Std Dev 3.656
Gaus mean : 29.8364
Gaus Width: 3.7760
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

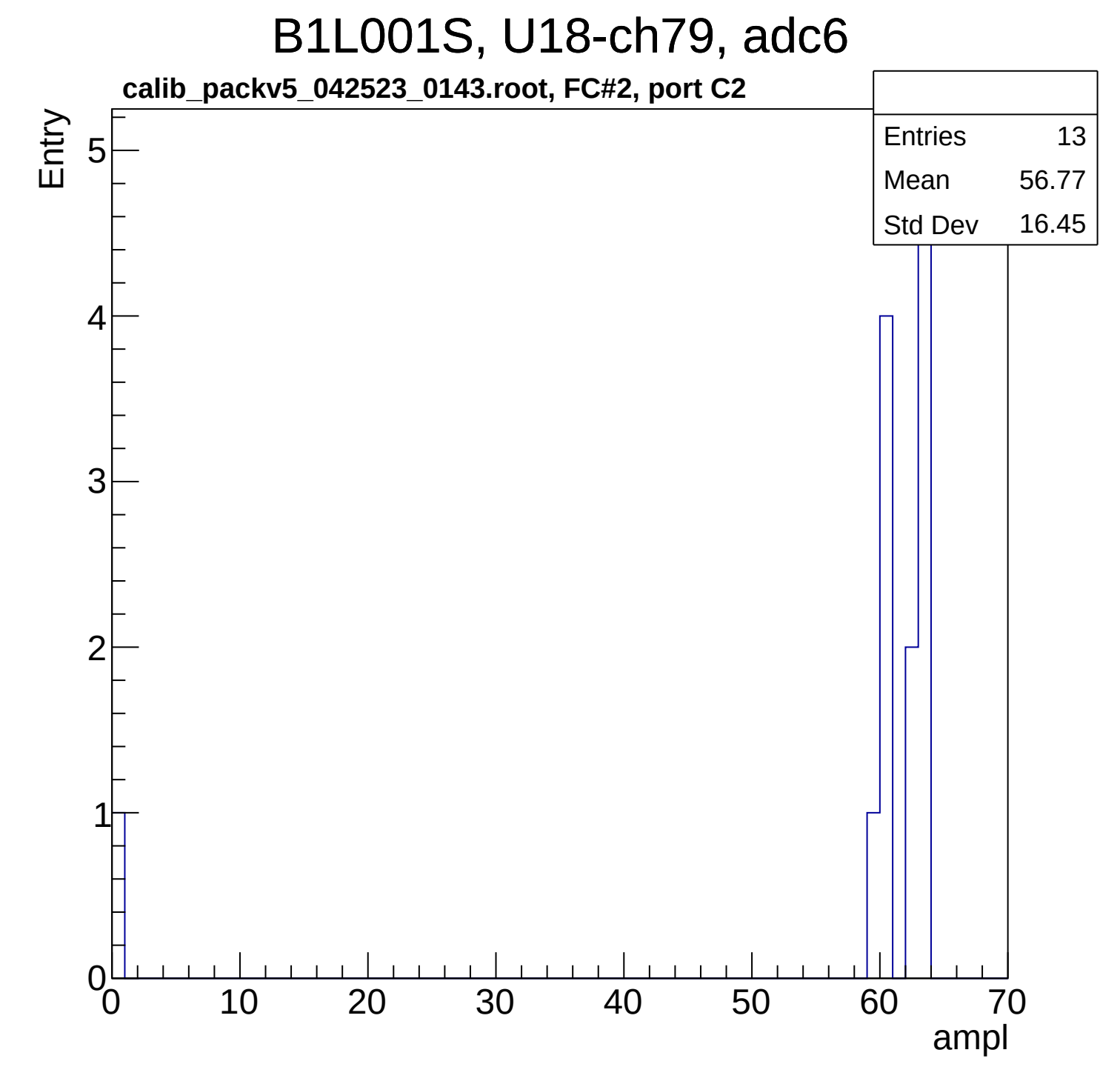

B1L001S, U18-ch79, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 143
Mean 36.74
Std Dev 3.431
Gaus mean : 37.2915
Gaus Width: 3.3733
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

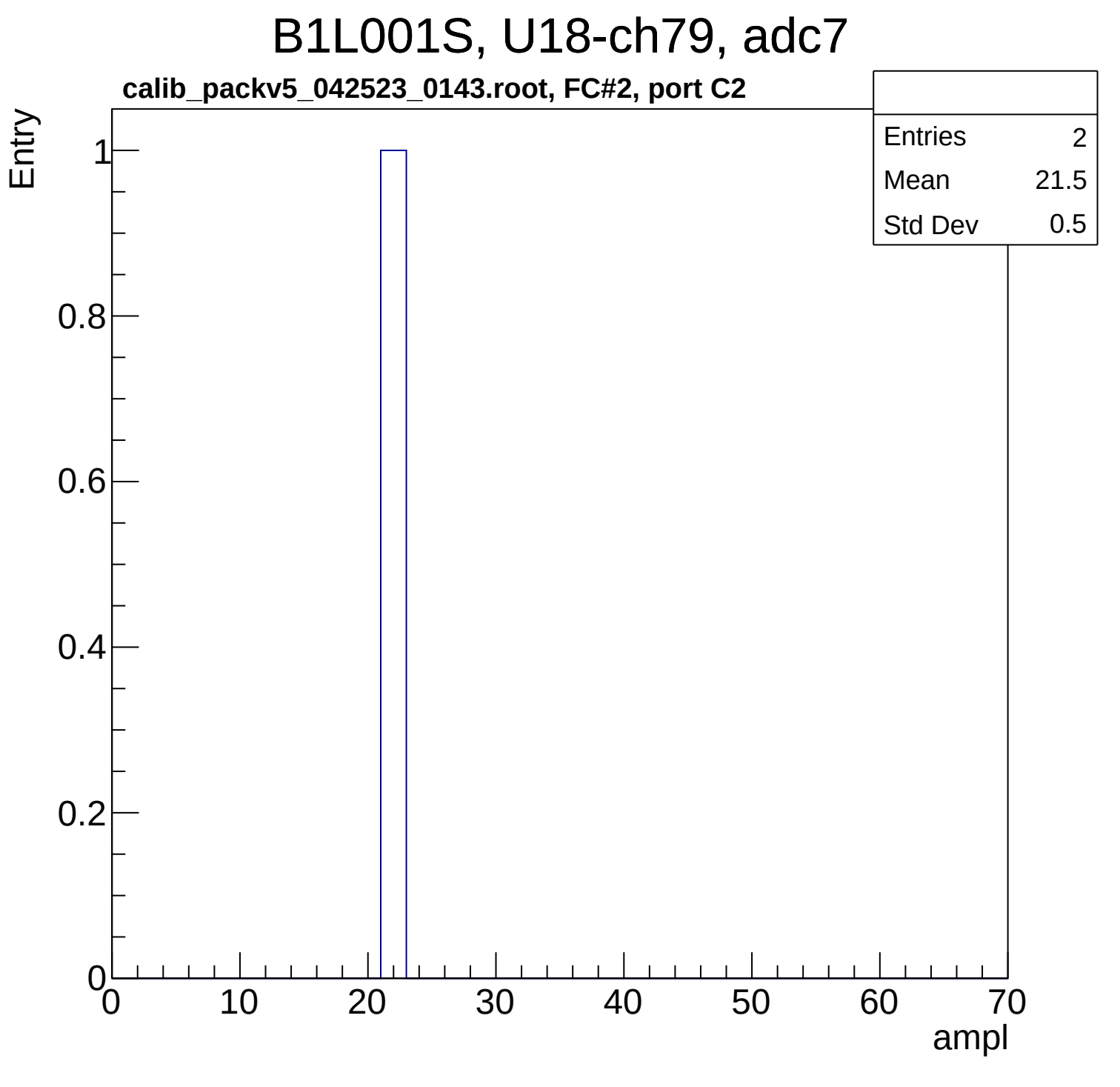

B1L001S, U18-ch79, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 122
Mean 43.7
Std Dev 3.345
Gaus mean : 44.3724
Gaus Width: 3.1314
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

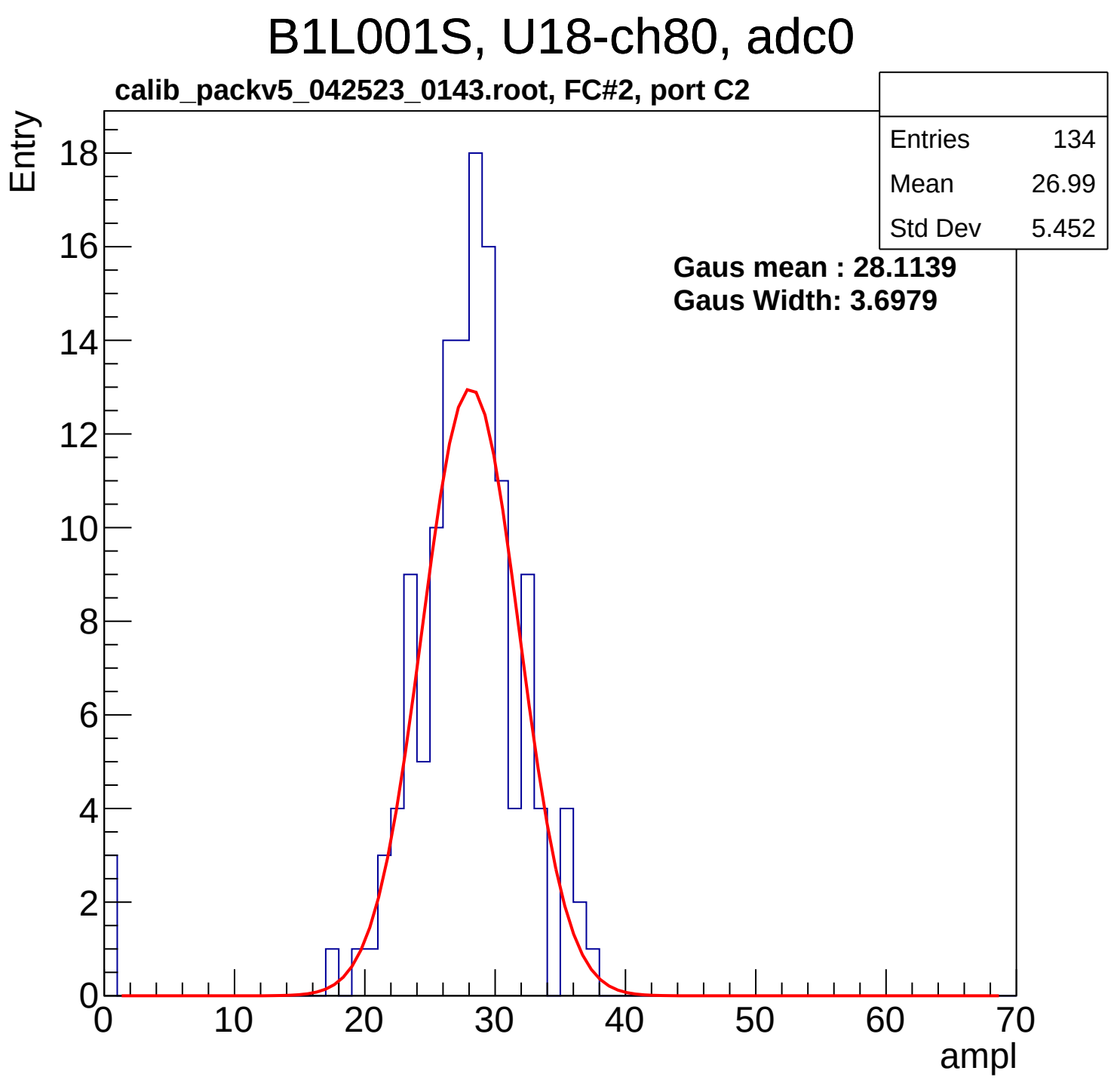

B1L001S, U18-ch79, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 120
Mean 49.24
Std Dev 3.704
Entry
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl

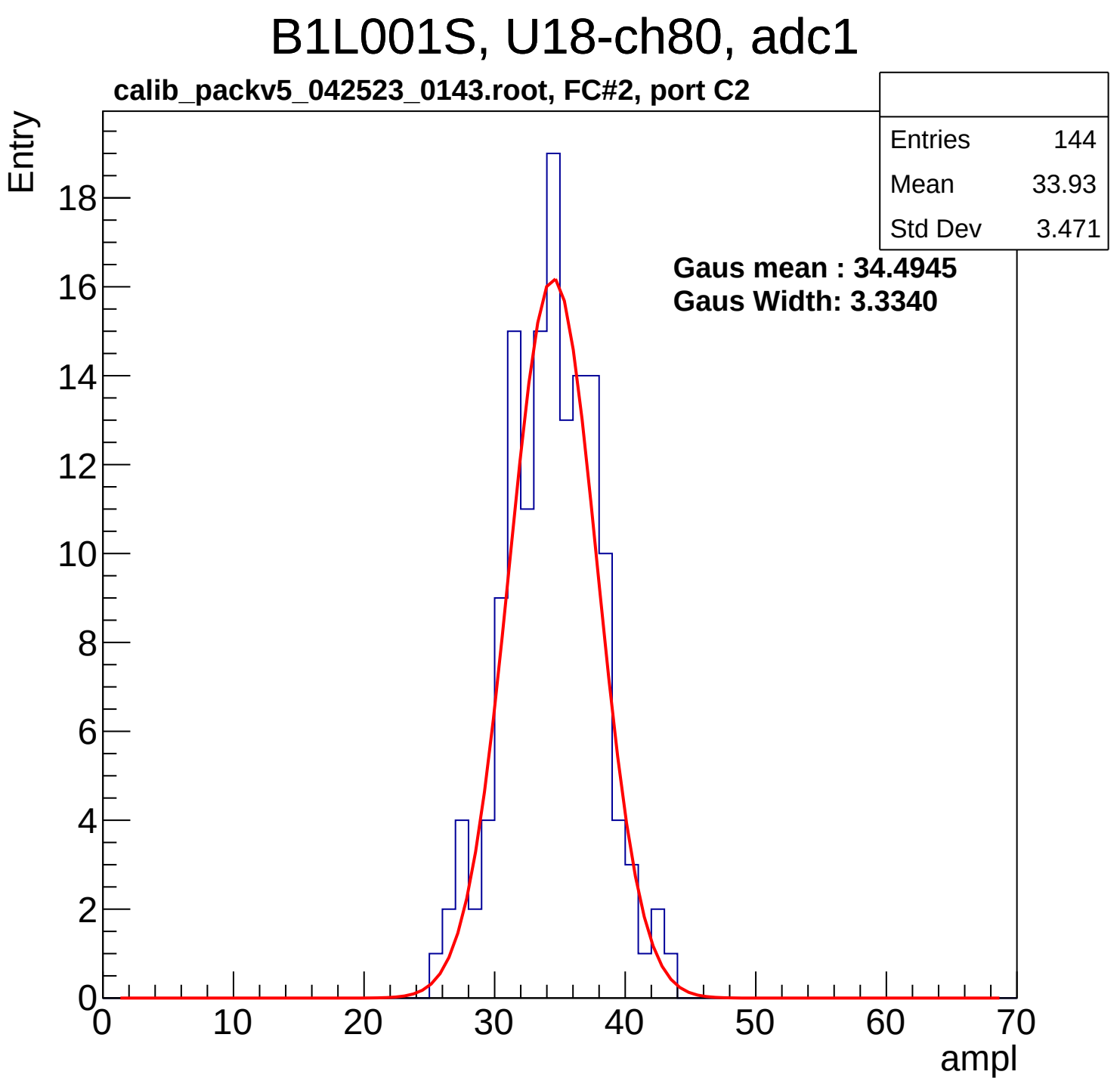

B1L001S, U18-ch79, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 114
Mean 55.49
Std Dev 3.299
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl

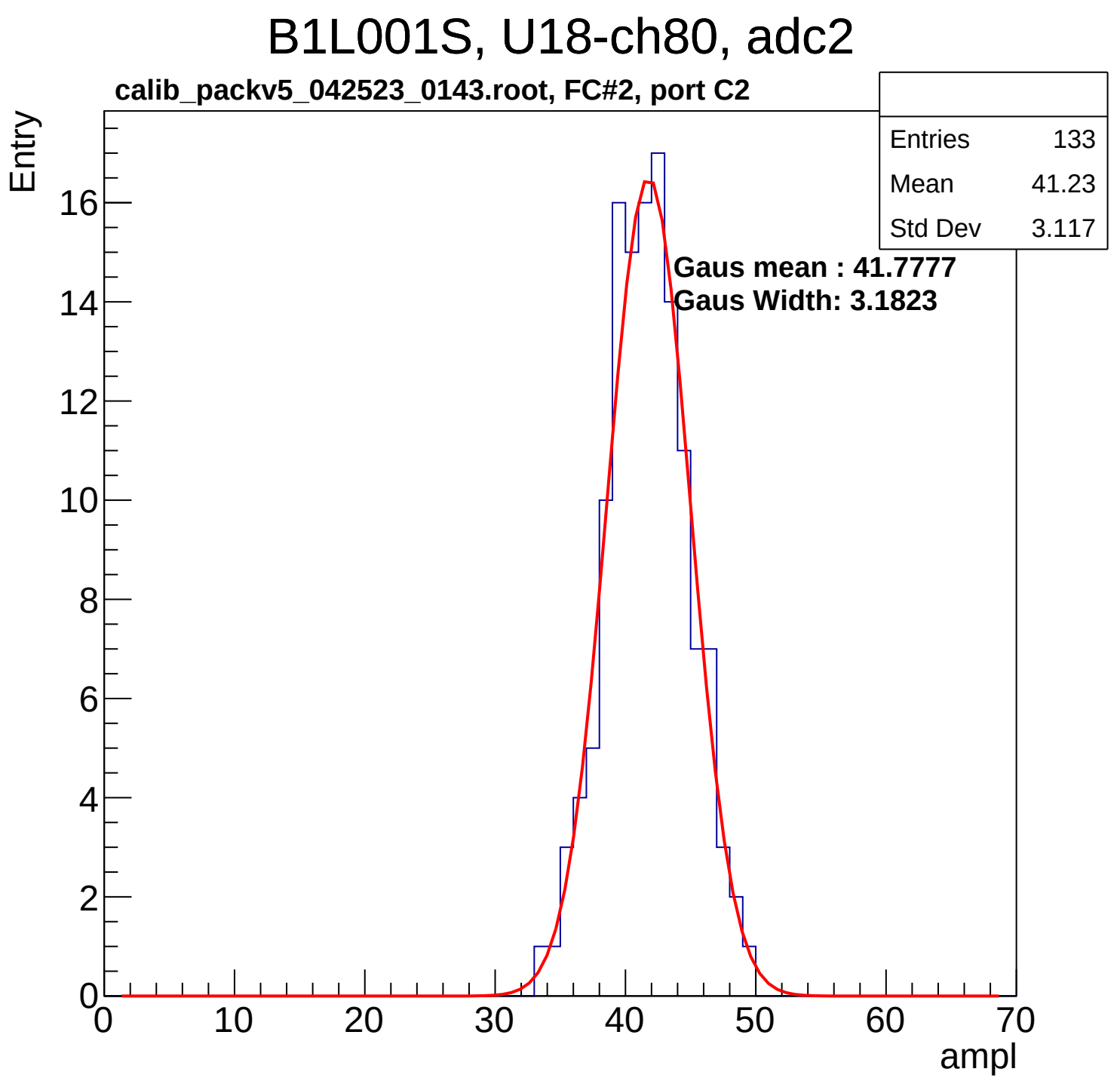

B1L001S, U18-ch79, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 95
Mean 59.13
Std Dev 6.64
Entry
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl

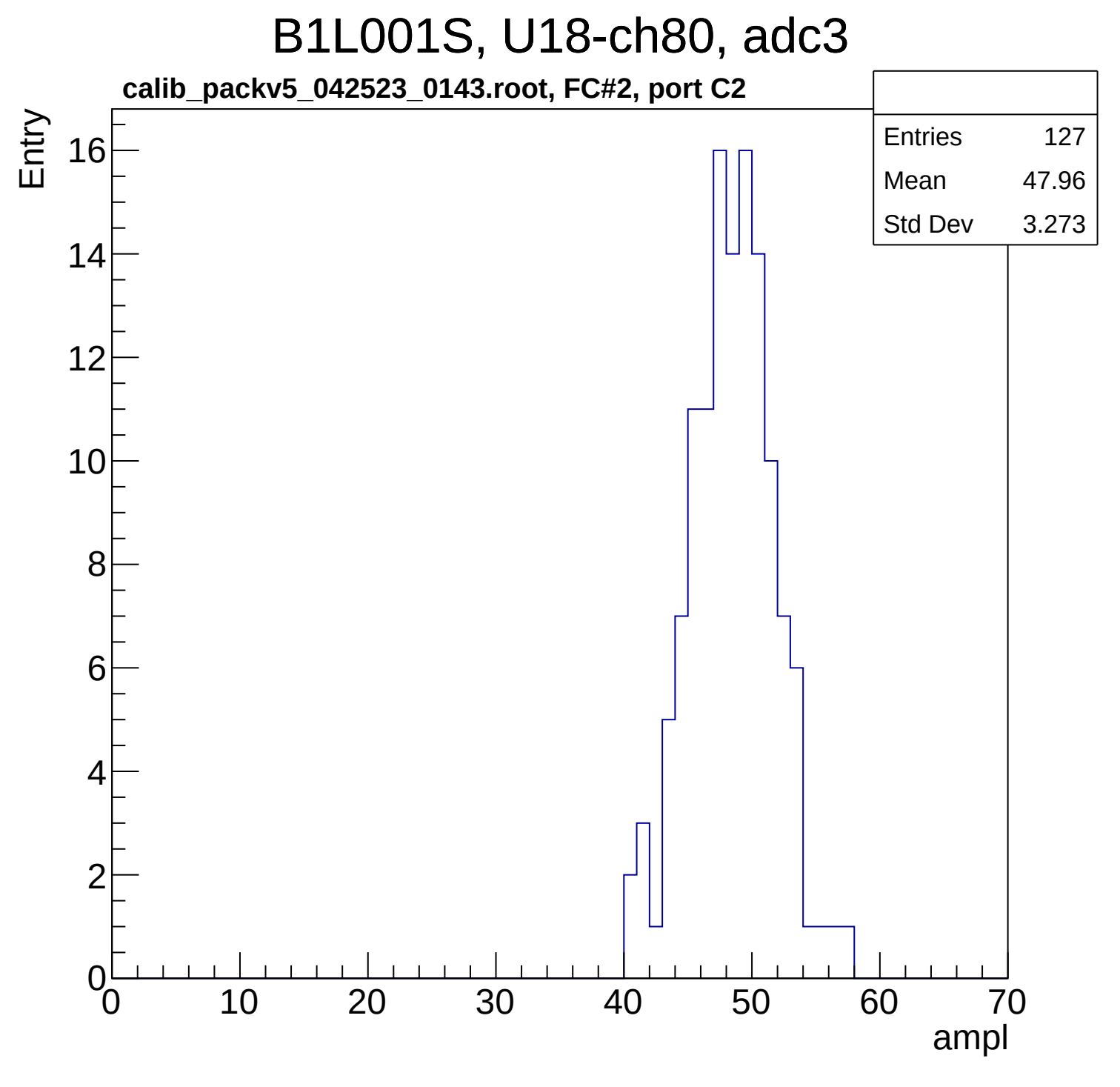

B1L001S, U18-ch79, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 13
Mean 56.77
Std Dev 16.45
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

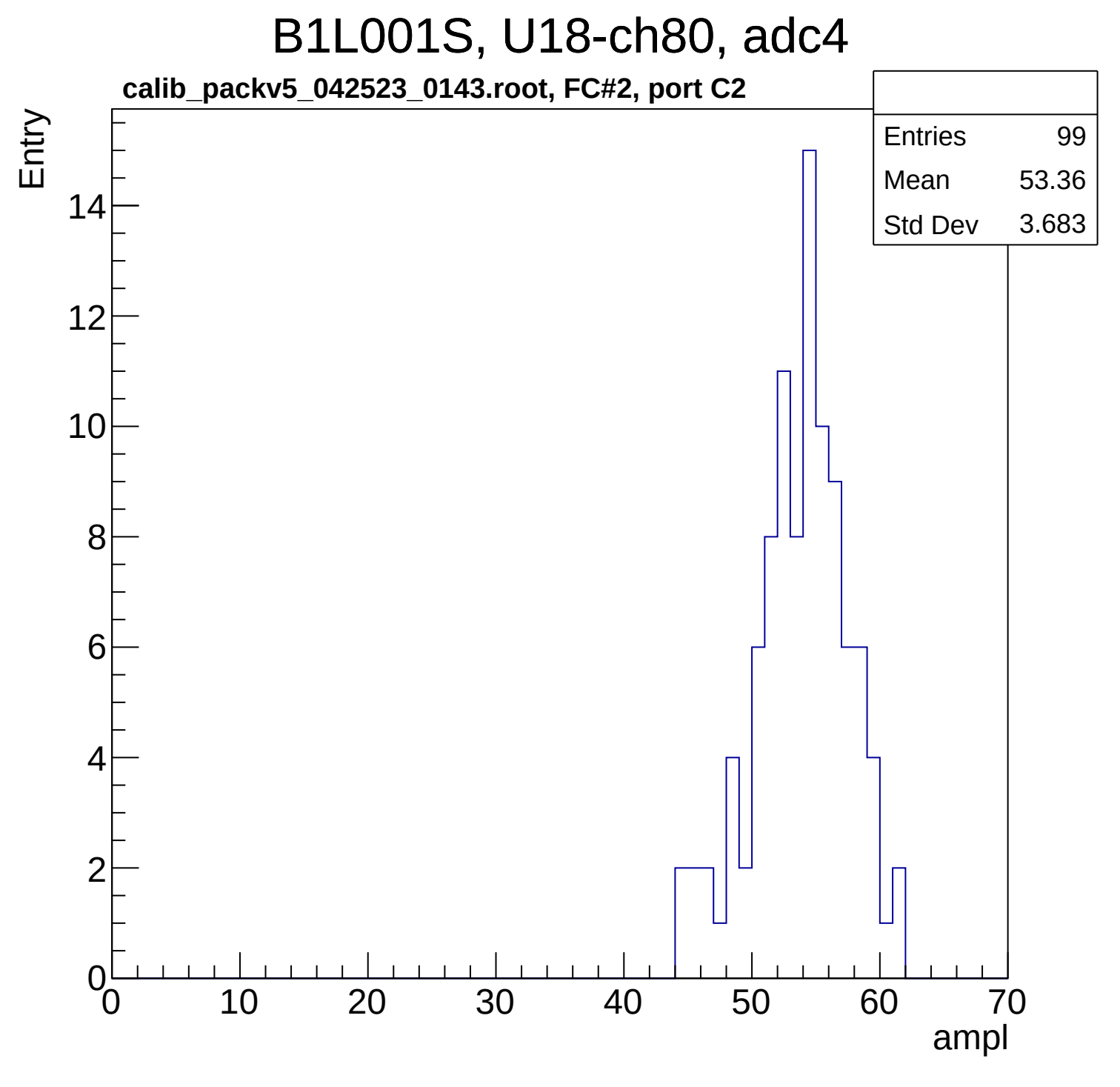

B1L001S, U18-ch79, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 21.5
Std Dev 0.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

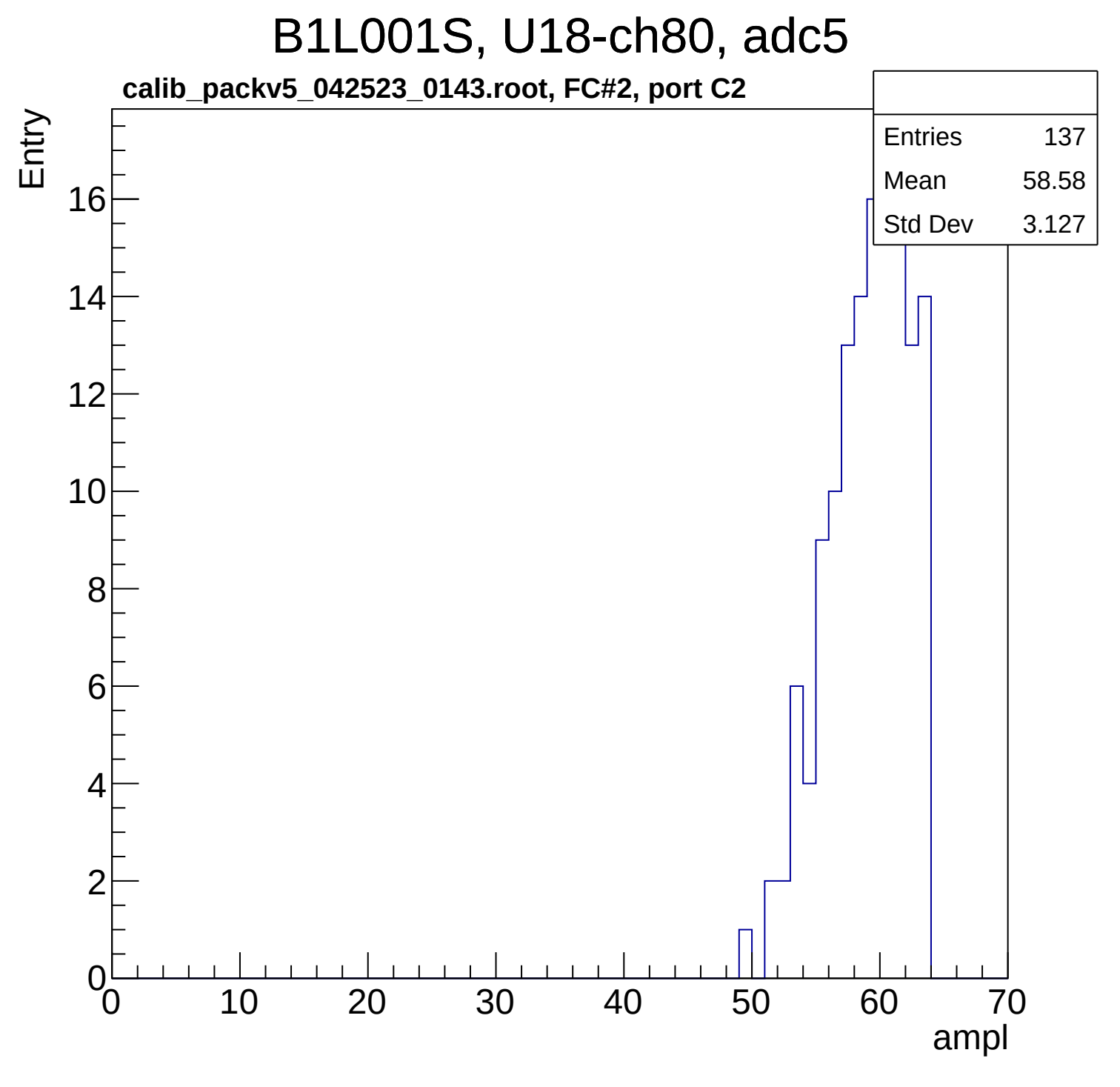

B1L001S, U18-ch80, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 134
Mean 26.99
Std Dev 5.452
Gaus mean : 28.1139
Gaus Width: 3.6979
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

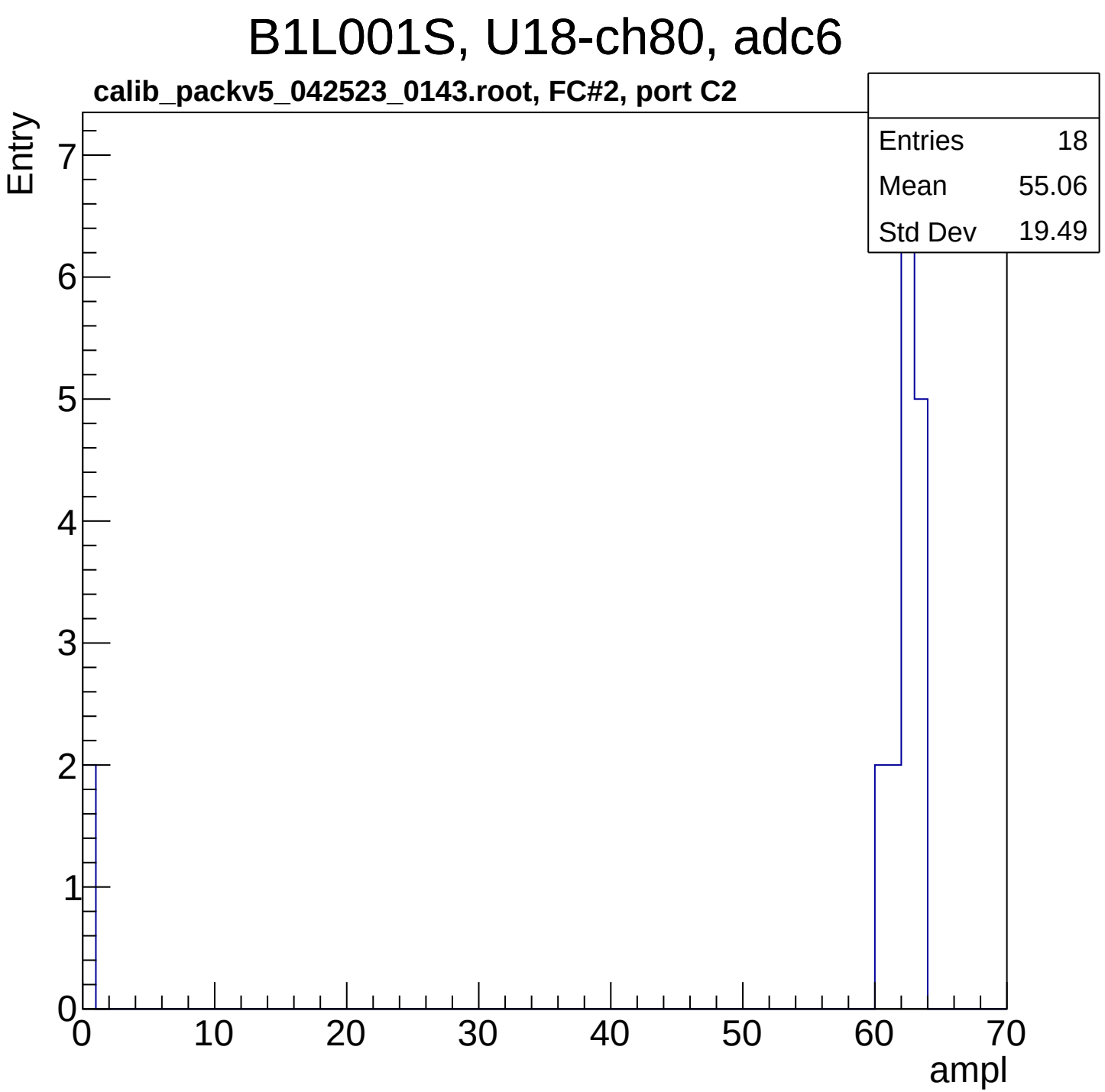

B1L001S, U18-ch80, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 144
Mean 33.93
Std Dev 3.471
Gaus mean : 34.4945
Gaus Width: 3.3340
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

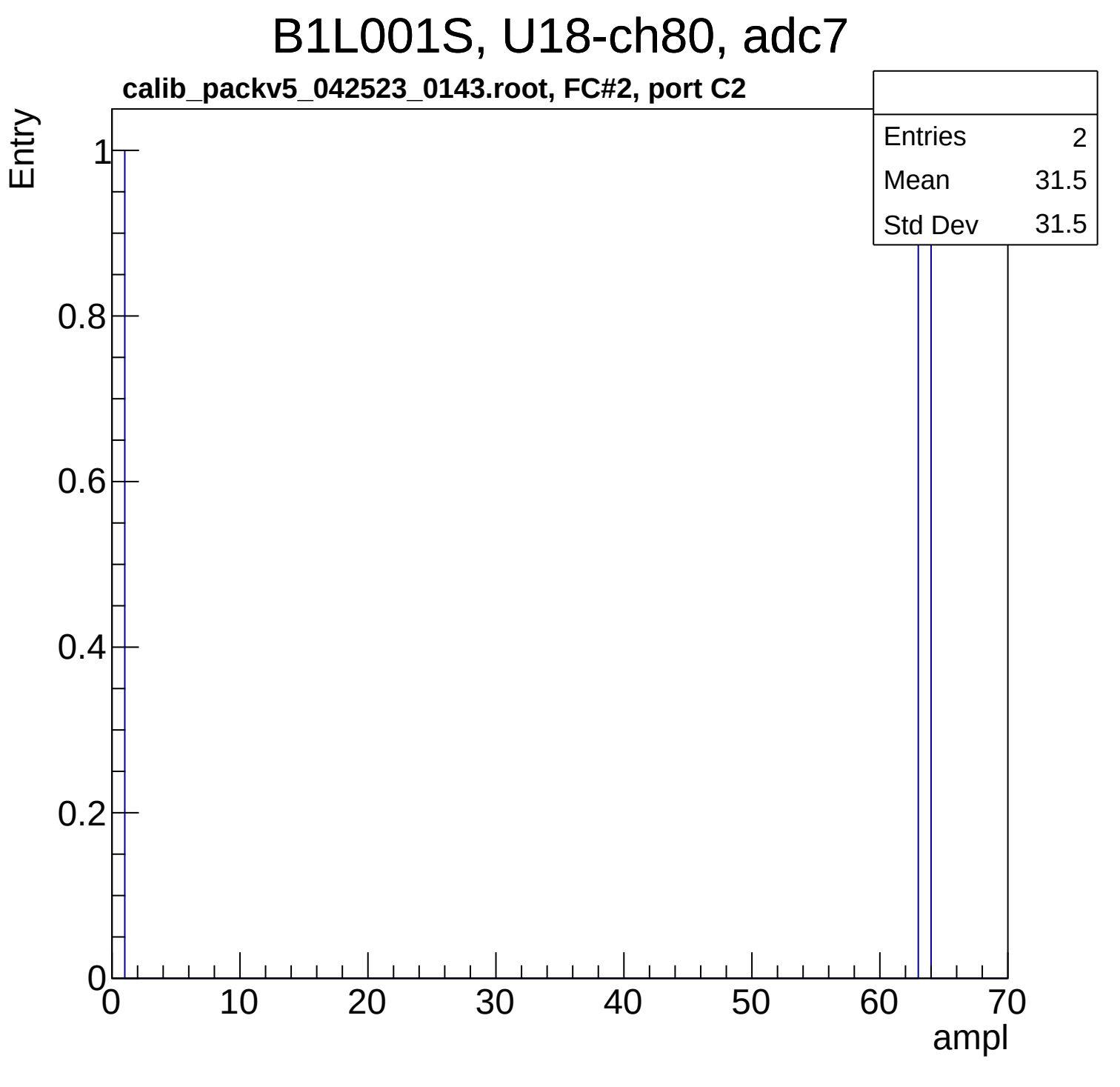

B1L001S, U18-ch80, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 133
Mean 41.23
Std Dev 3.117
Gaus mean : 41.7777
Gaus Width: 3.1823
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

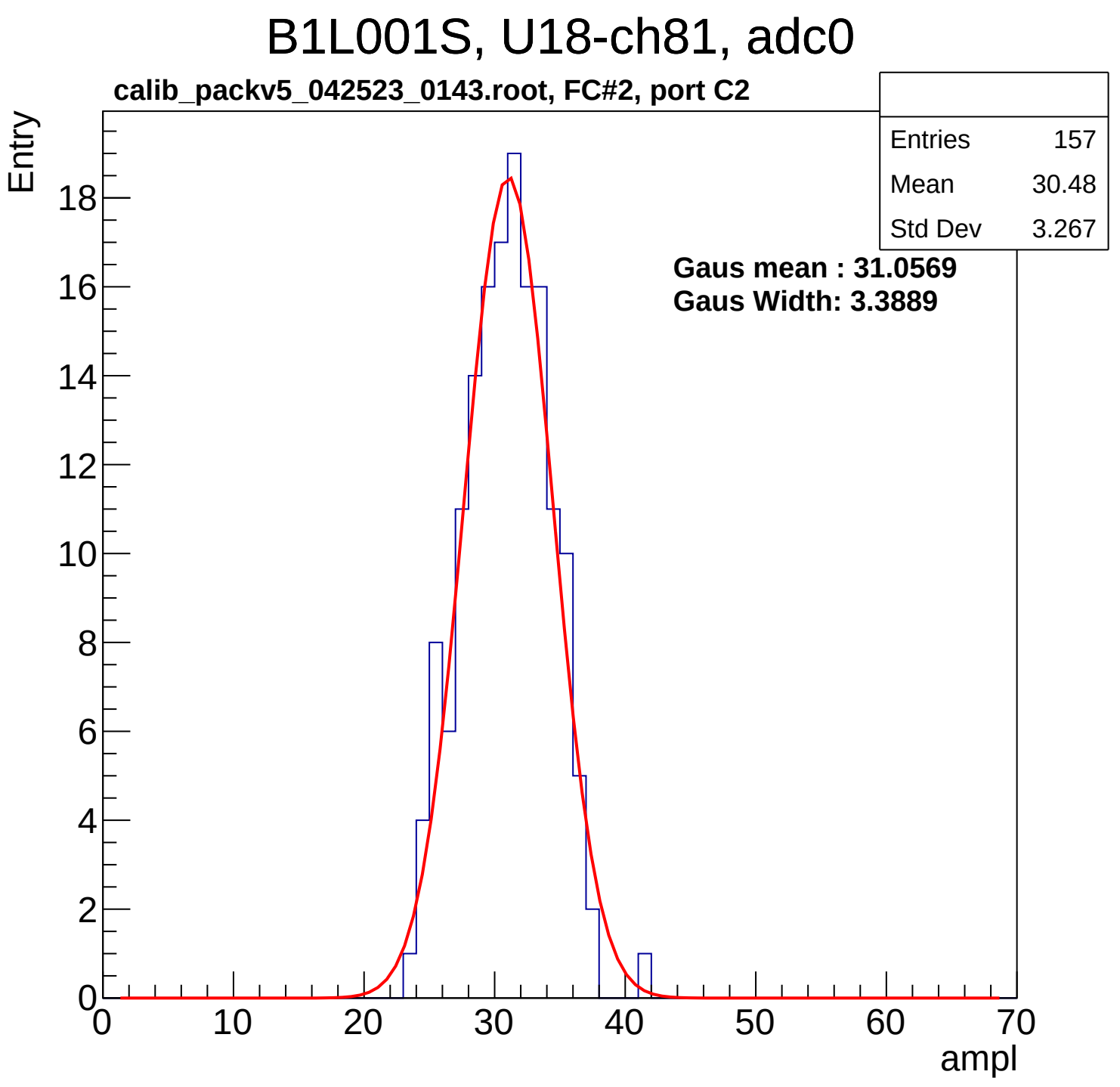

B1L001S, U18-ch80, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 127
Mean 47.96
Std Dev 3.273
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

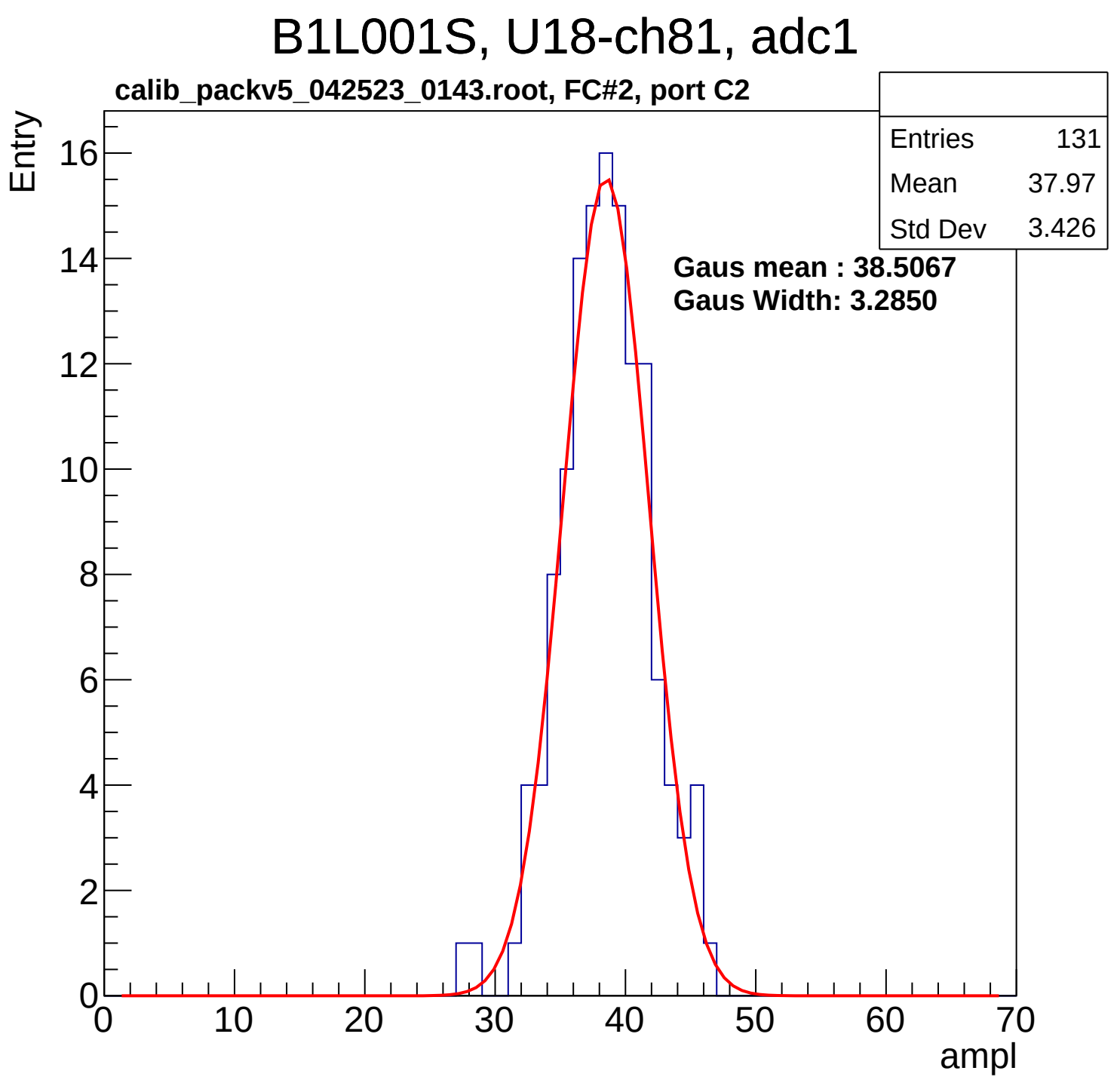

B1L001S, U18-ch80, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 99
Mean 53.36
Std Dev 3.683
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl

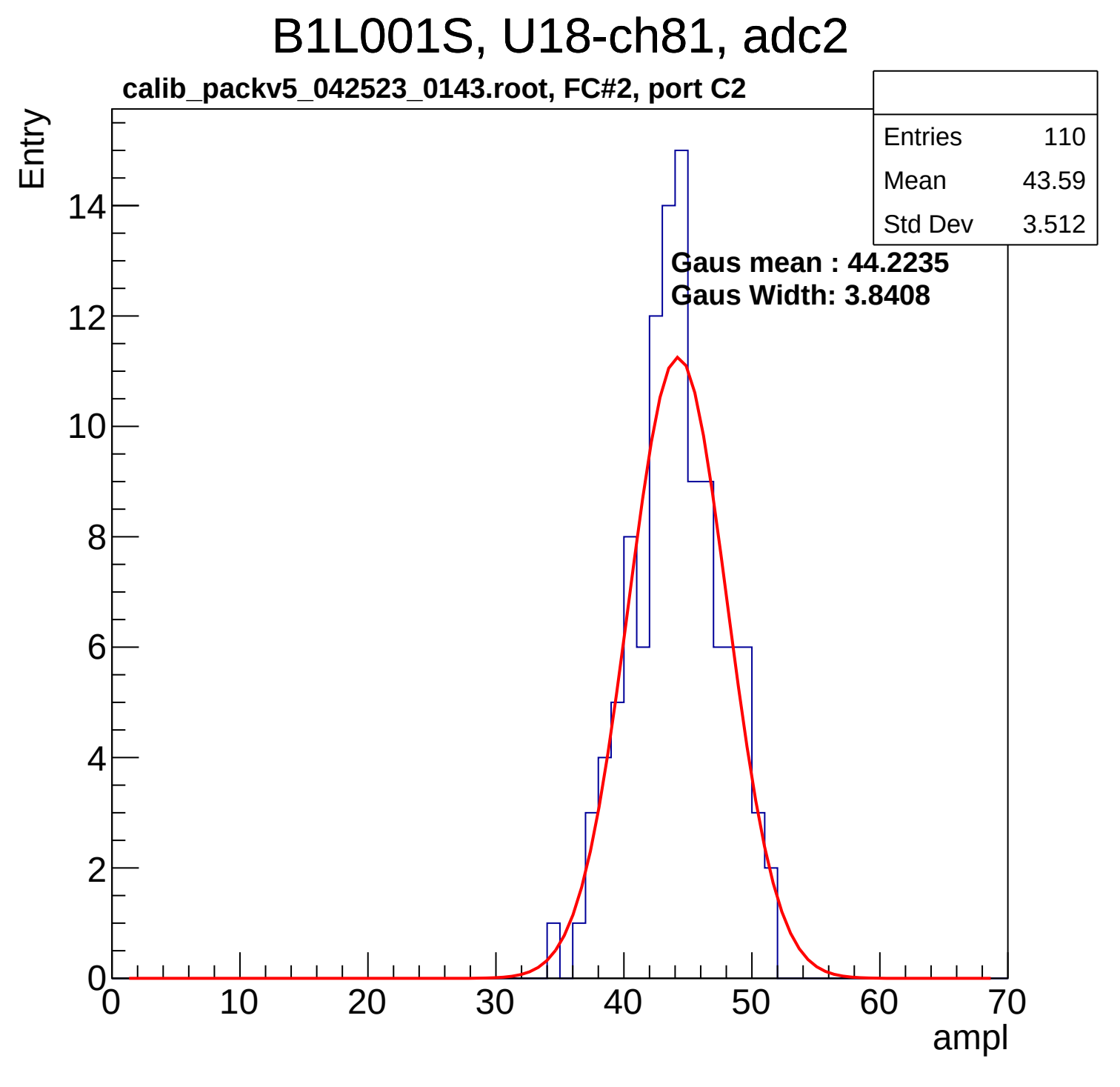

B1L001S, U18-ch80, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 137
Mean 58.58
Std Dev 3.127
Entry
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl

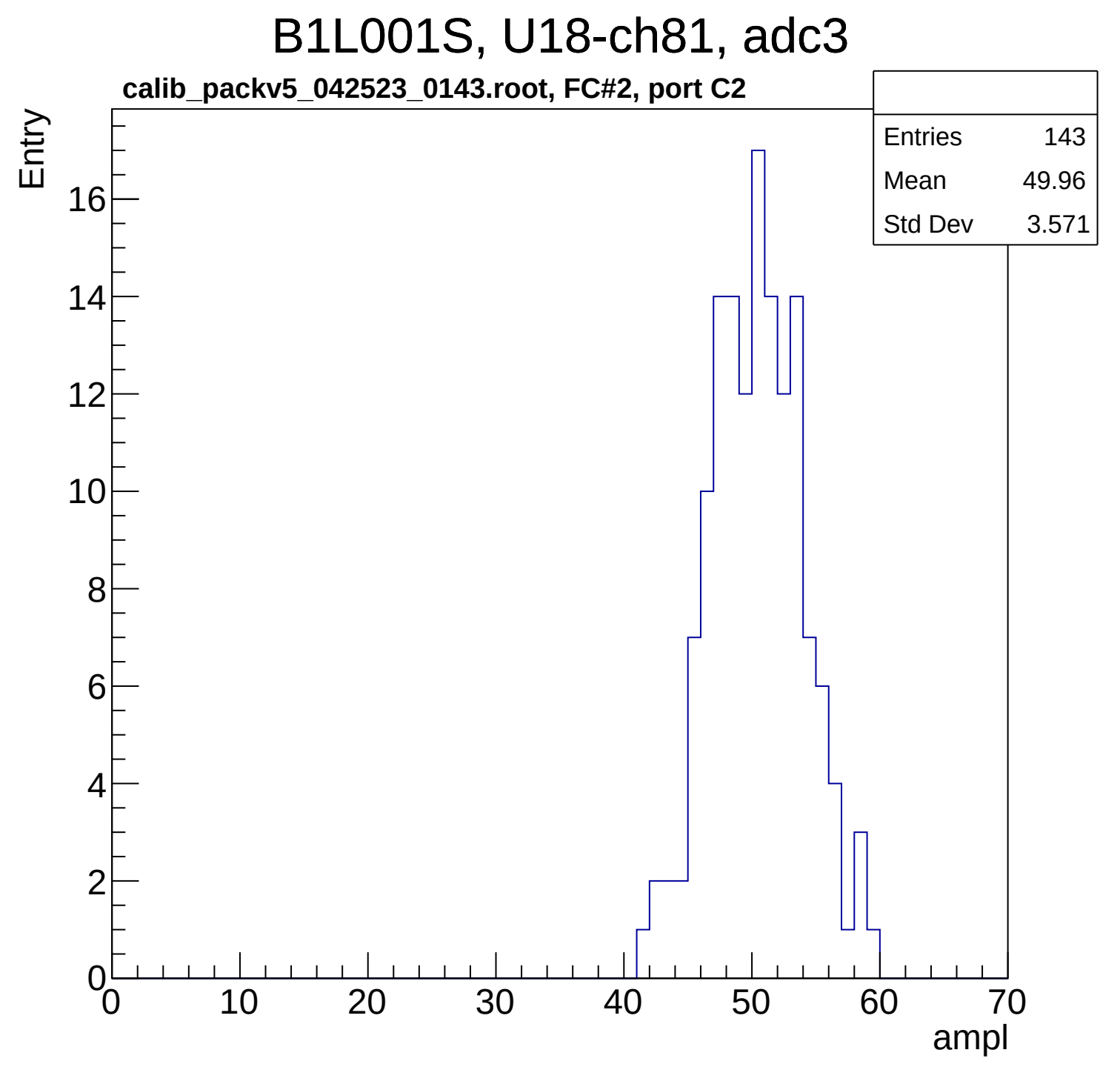

B1L001S, U18-ch80, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 18
Mean 55.06
Std Dev 19.49
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

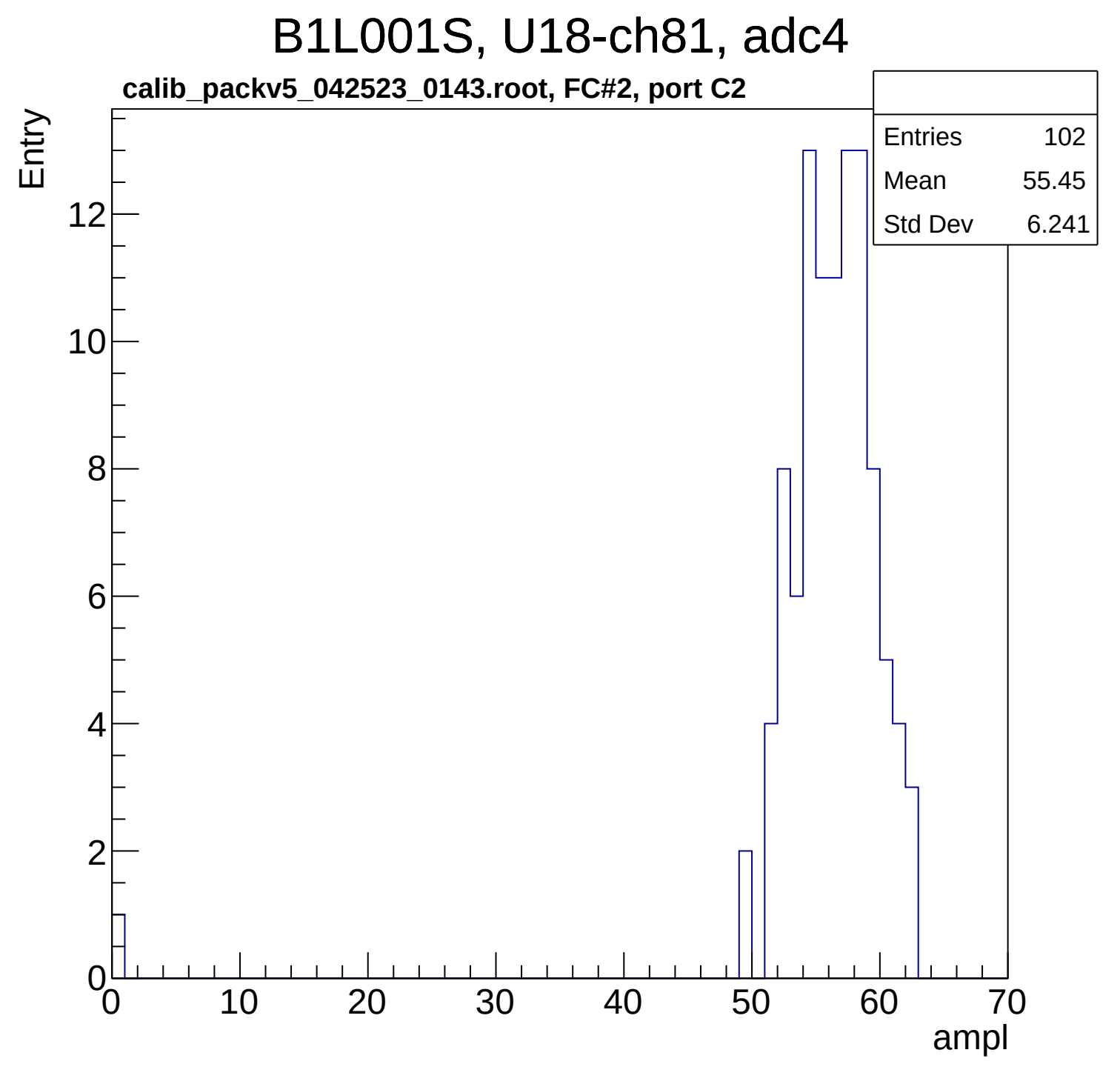

B1L001S, U18-ch80, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 31.5
Std Dev 31.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

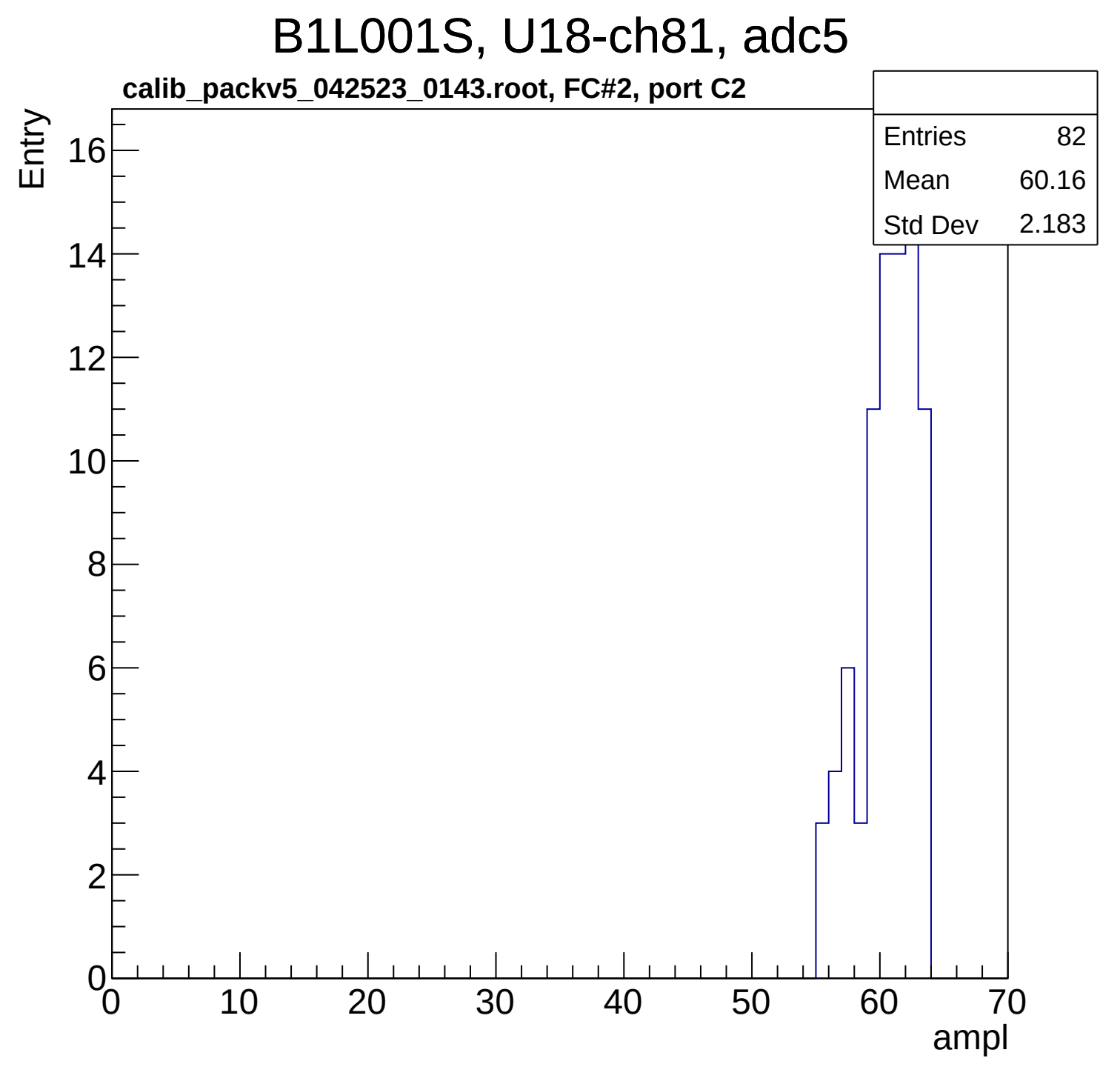

B1L001S, U18-ch81, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 157
Mean 30.48
Std Dev 3.267
Gaus mean : 31.0569
Gaus Width: 3.3889
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

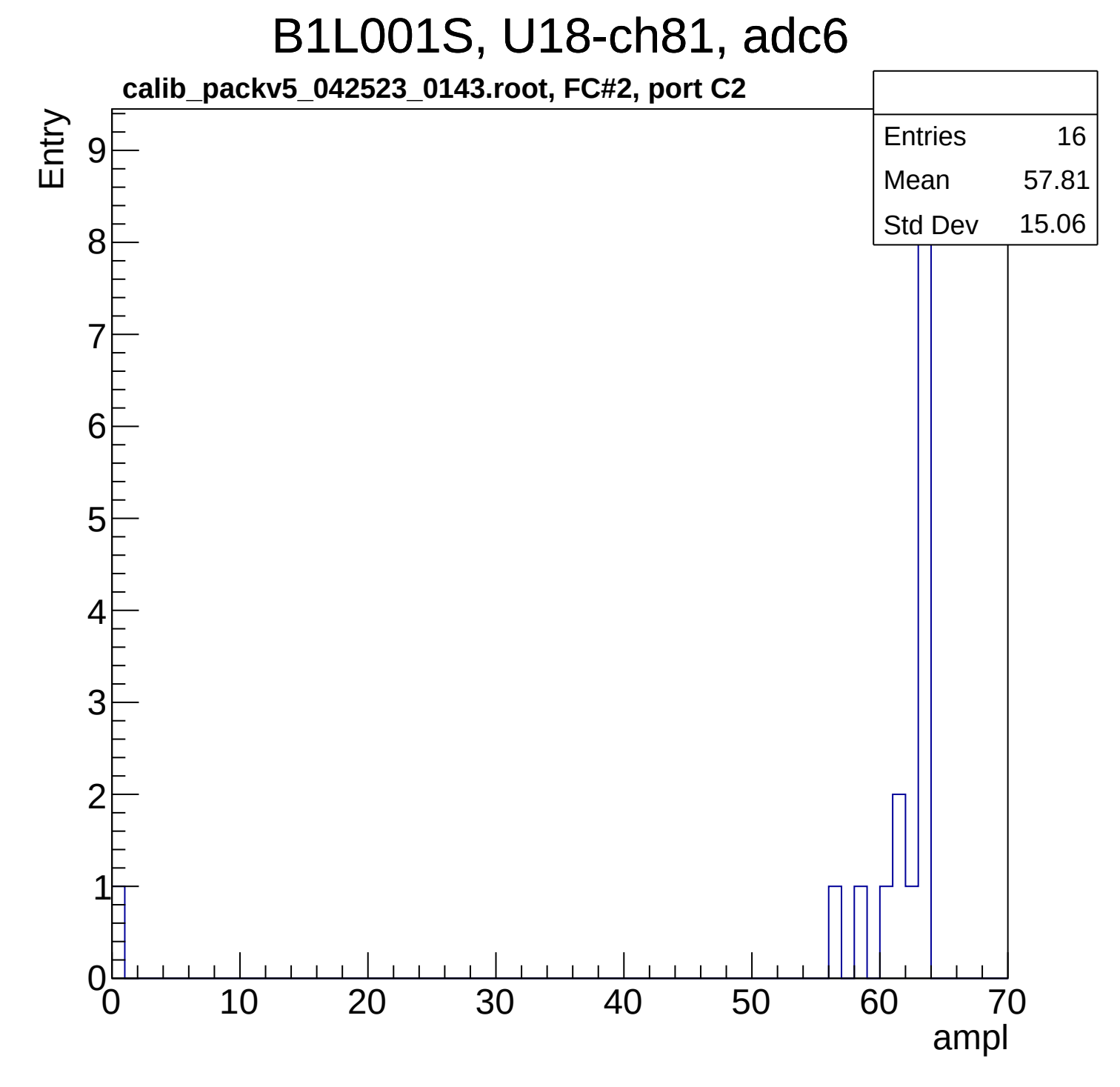

B1L001S, U18-ch81, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 131
Mean 37.97
Std Dev 3.426
Gaus mean : 38.5067
Gaus Width: 3.2850
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

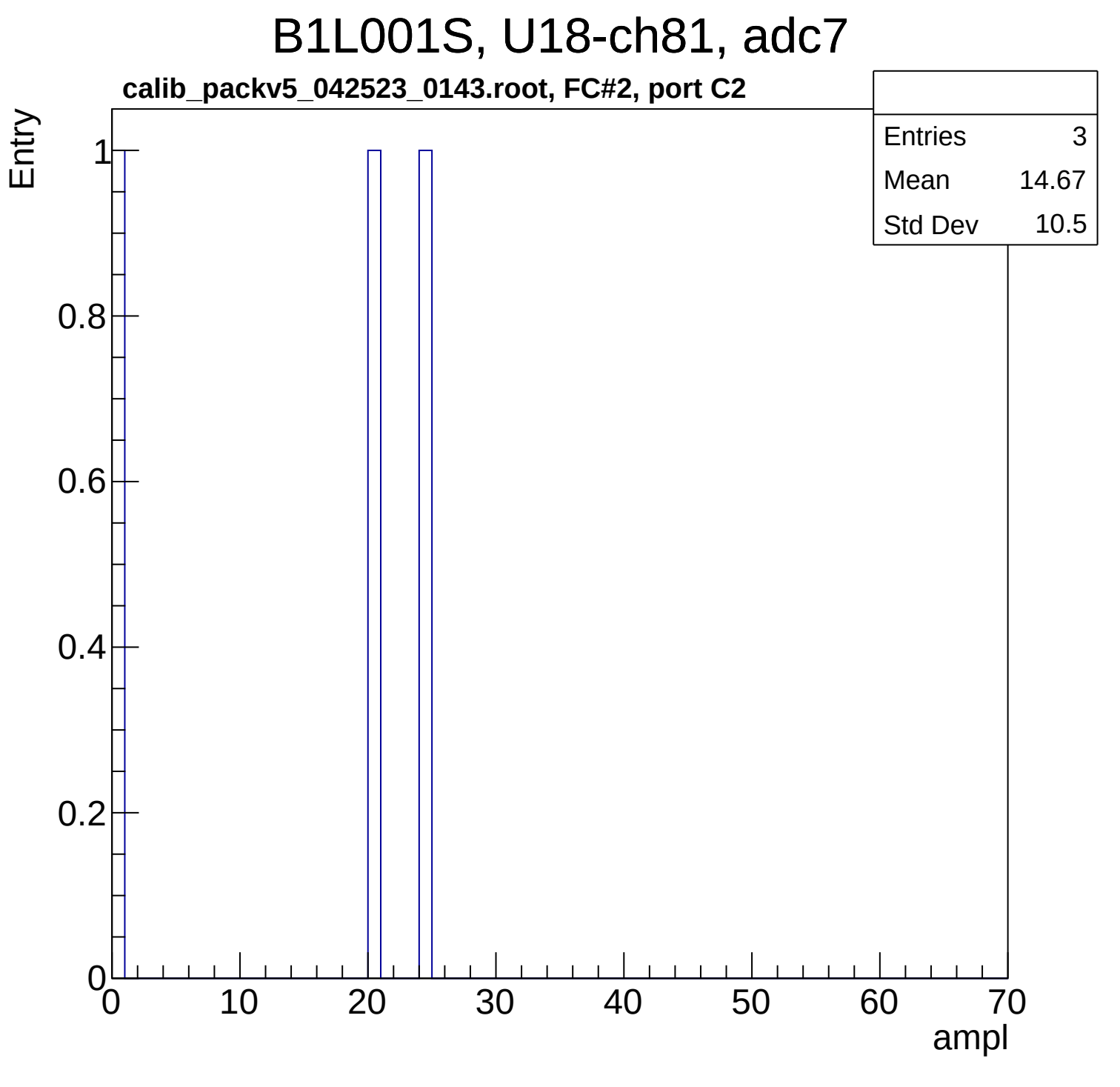

B1L001S, U18-ch81, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 110
Mean 43.59
Std Dev 3.512
Gaus mean : 44.2235
Gaus Width: 3.8408
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

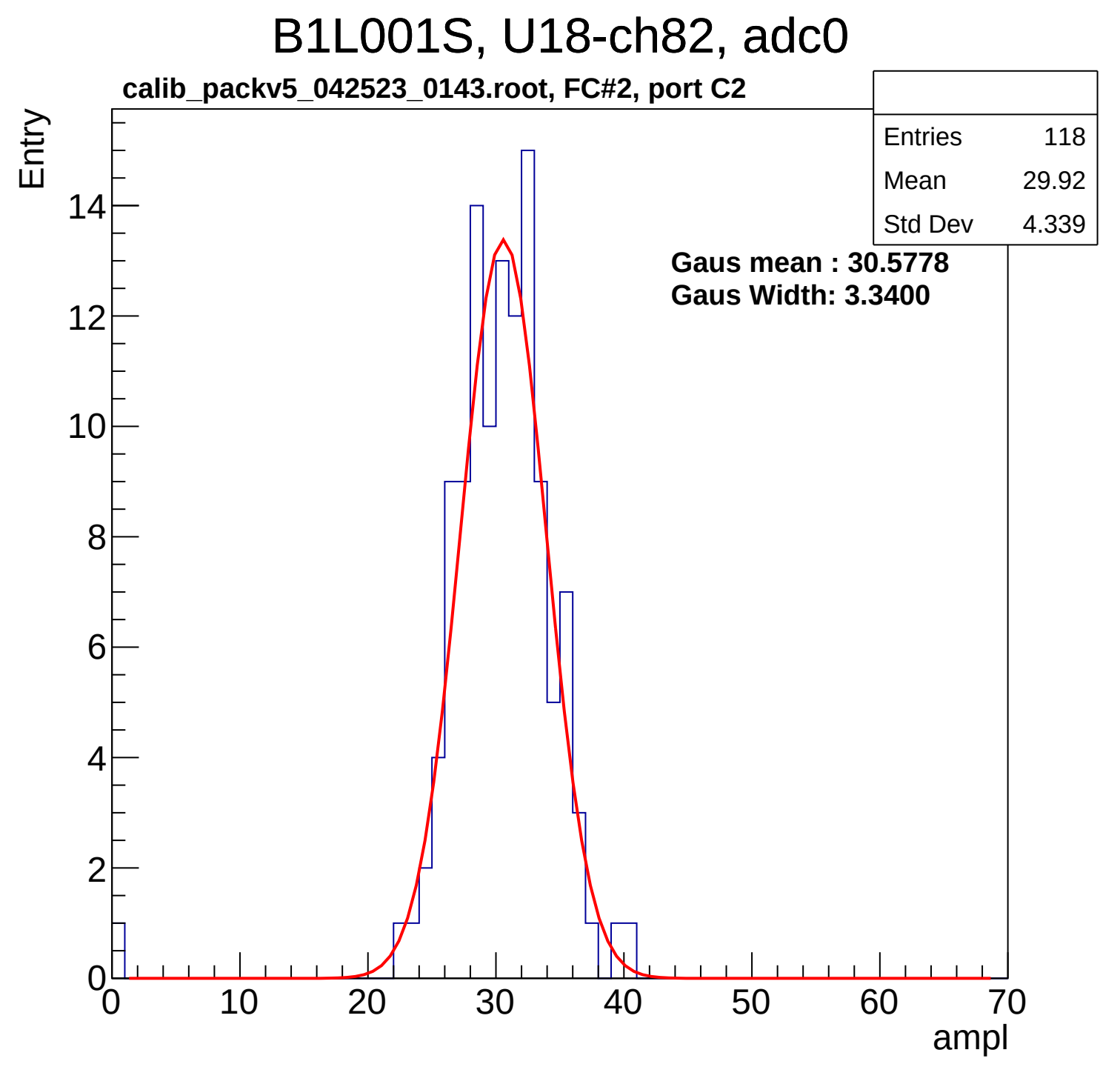

B1L001S, U18-ch81, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 143
Mean 49.96
Std Dev 3.571
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

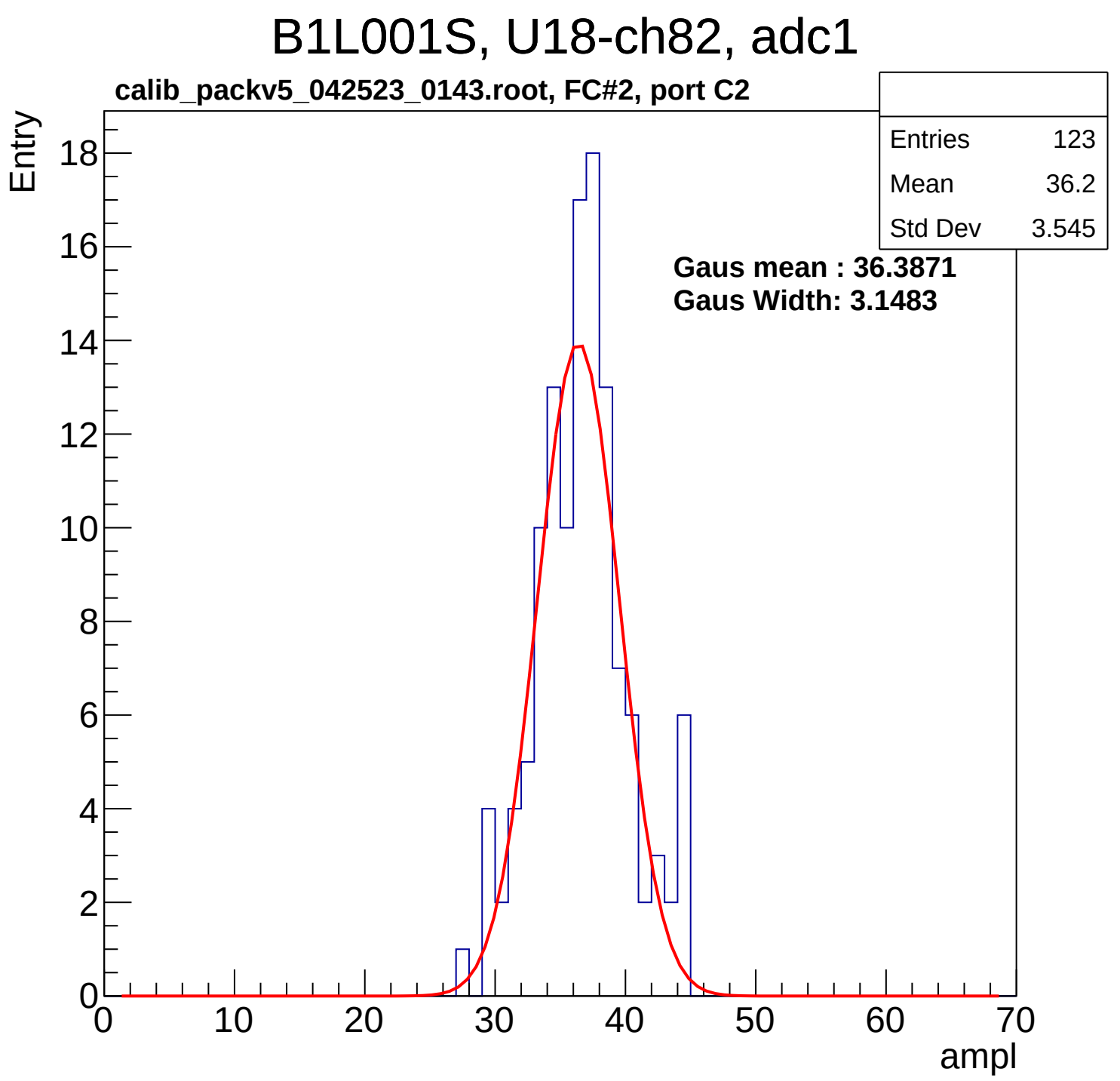

B1L001S, U18-ch81, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 102
Mean 55.45
Std Dev 6.241
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70

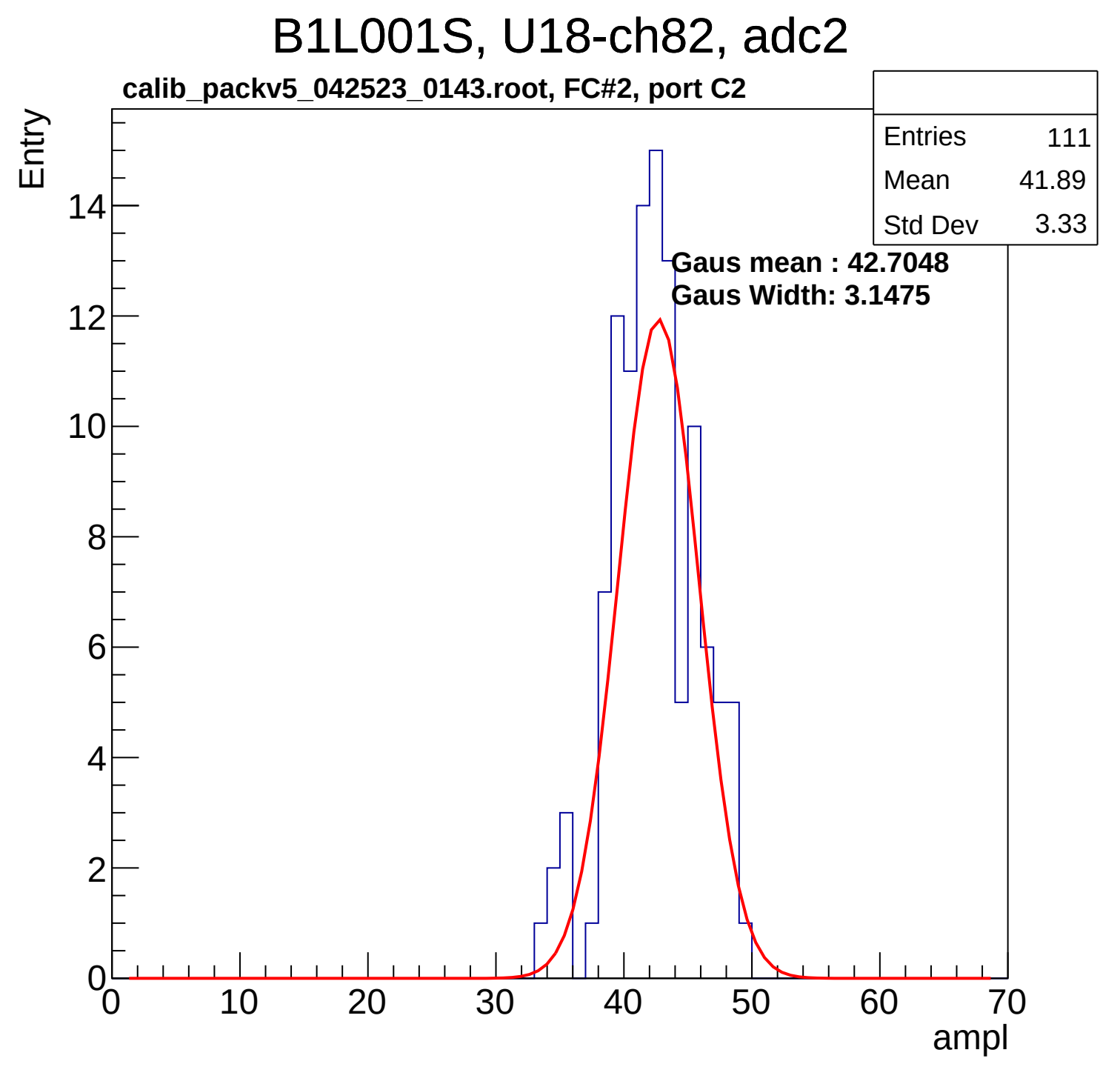

B1L001S, U18-ch81, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 82
Mean 60.16
Std Dev 2.183
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

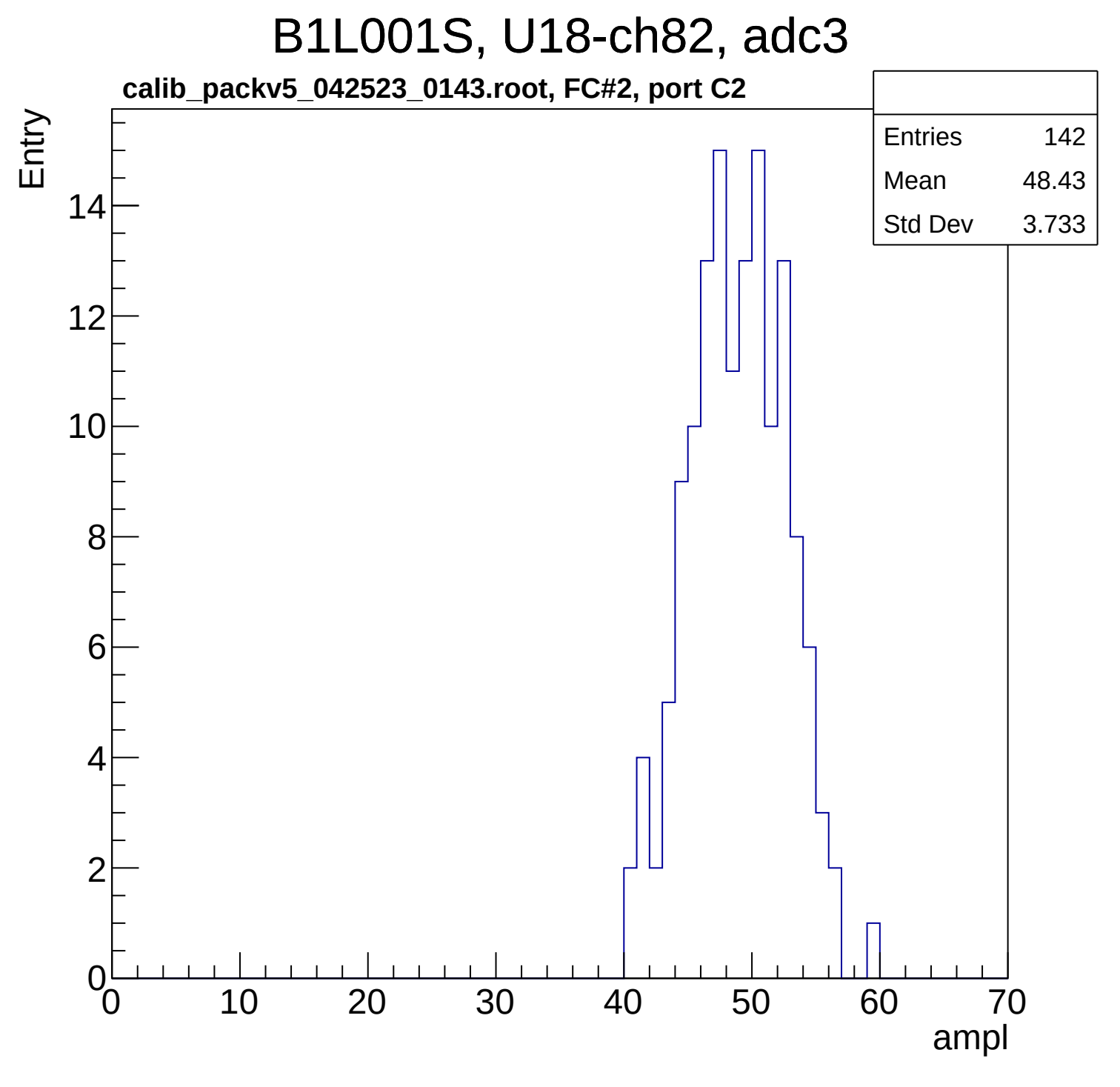

B1L001S, U18-ch81, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 16
Mean 57.81
Std Dev 15.06
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

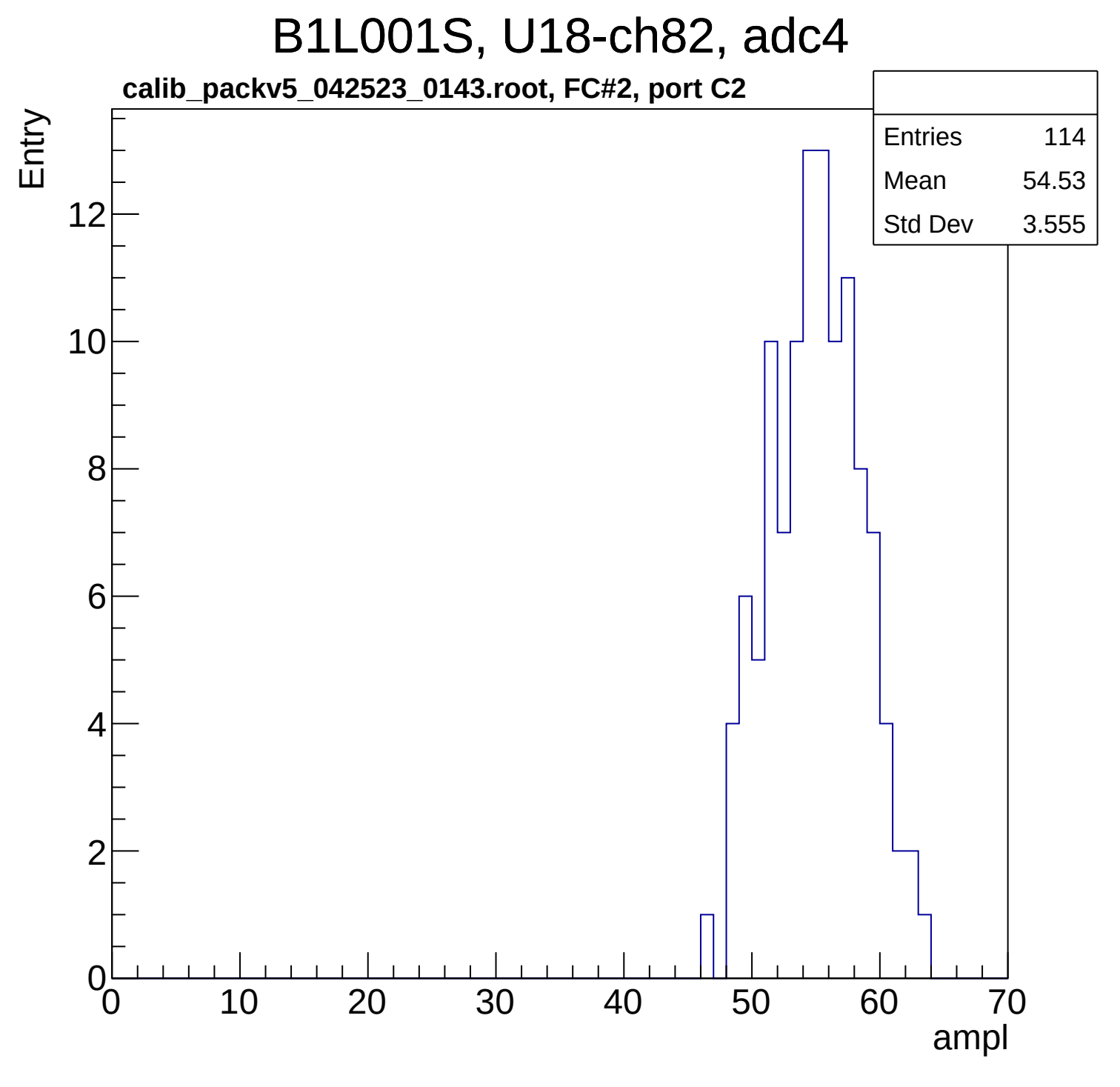

B1L001S, U18-ch81, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 3
Mean 14.67
Std Dev 10.5
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70

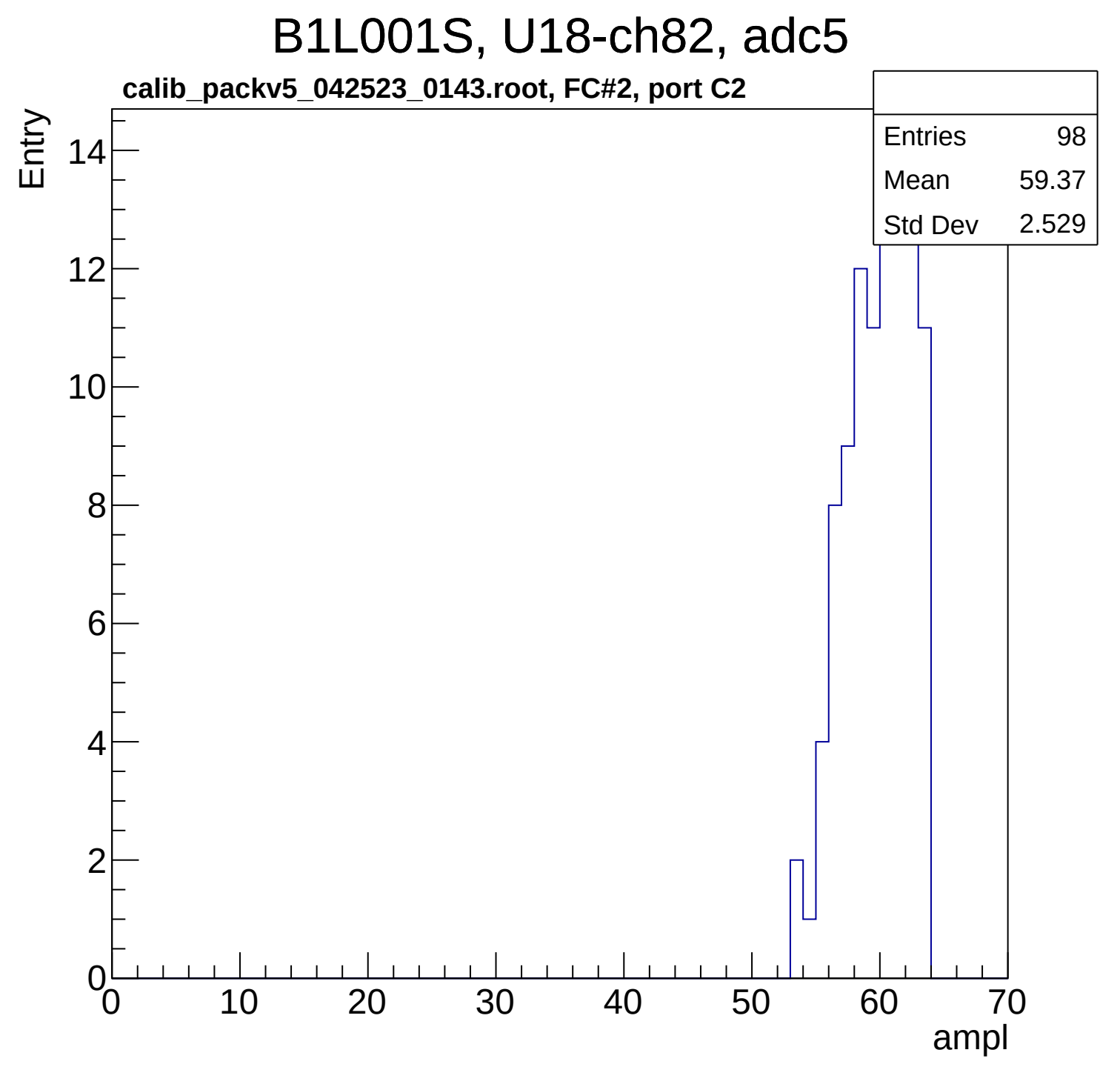

B1L001S, U18-ch82, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 118
Mean 29.92
Std Dev 4.339
Gaus mean : 30.5778
Gaus Width: 3.3400
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

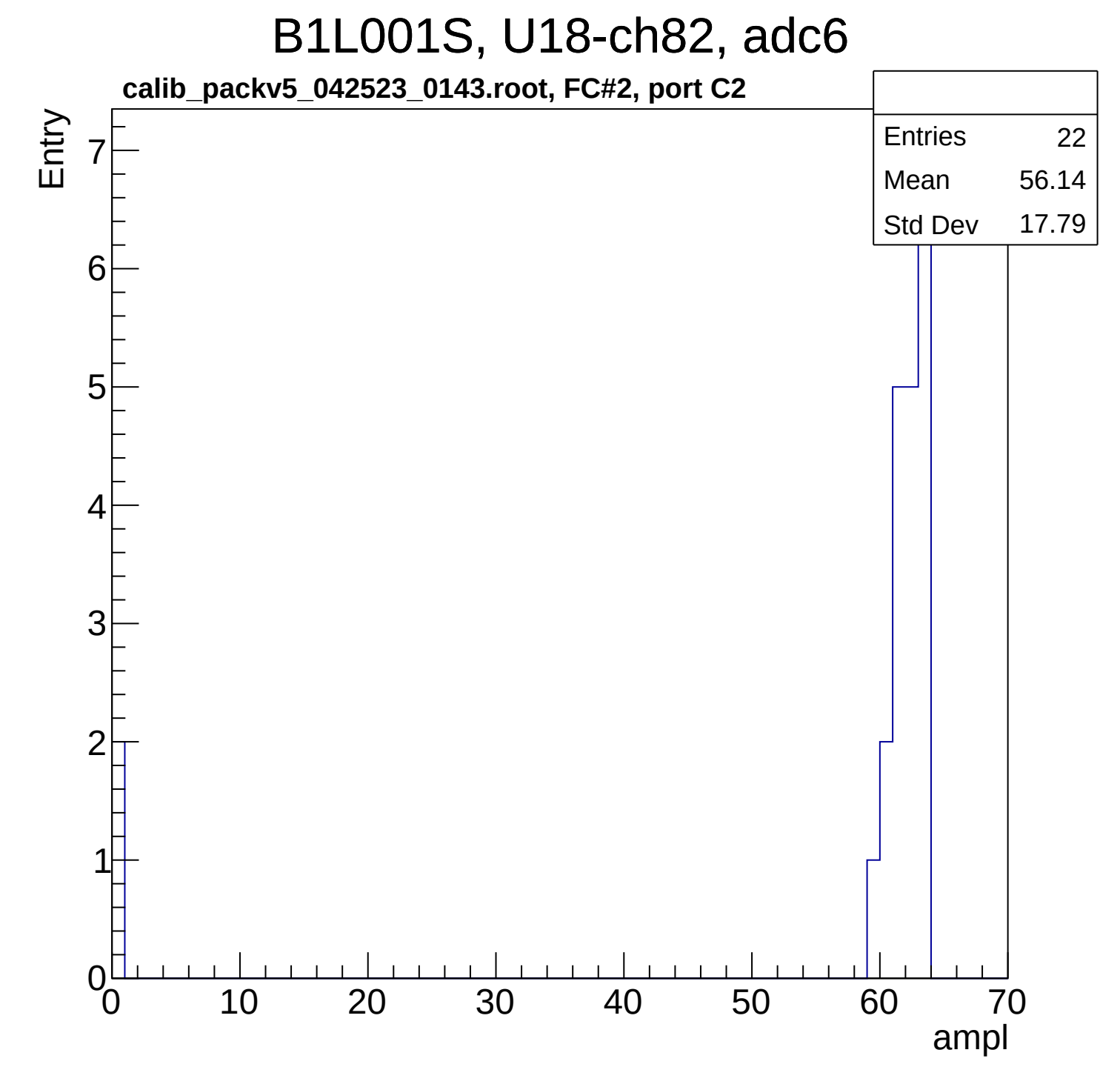

B1L001S, U18-ch82, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 123
Mean 36.2
Std Dev 3.545
Gaus mean : 36.3871
Gaus Width: 3.1483
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

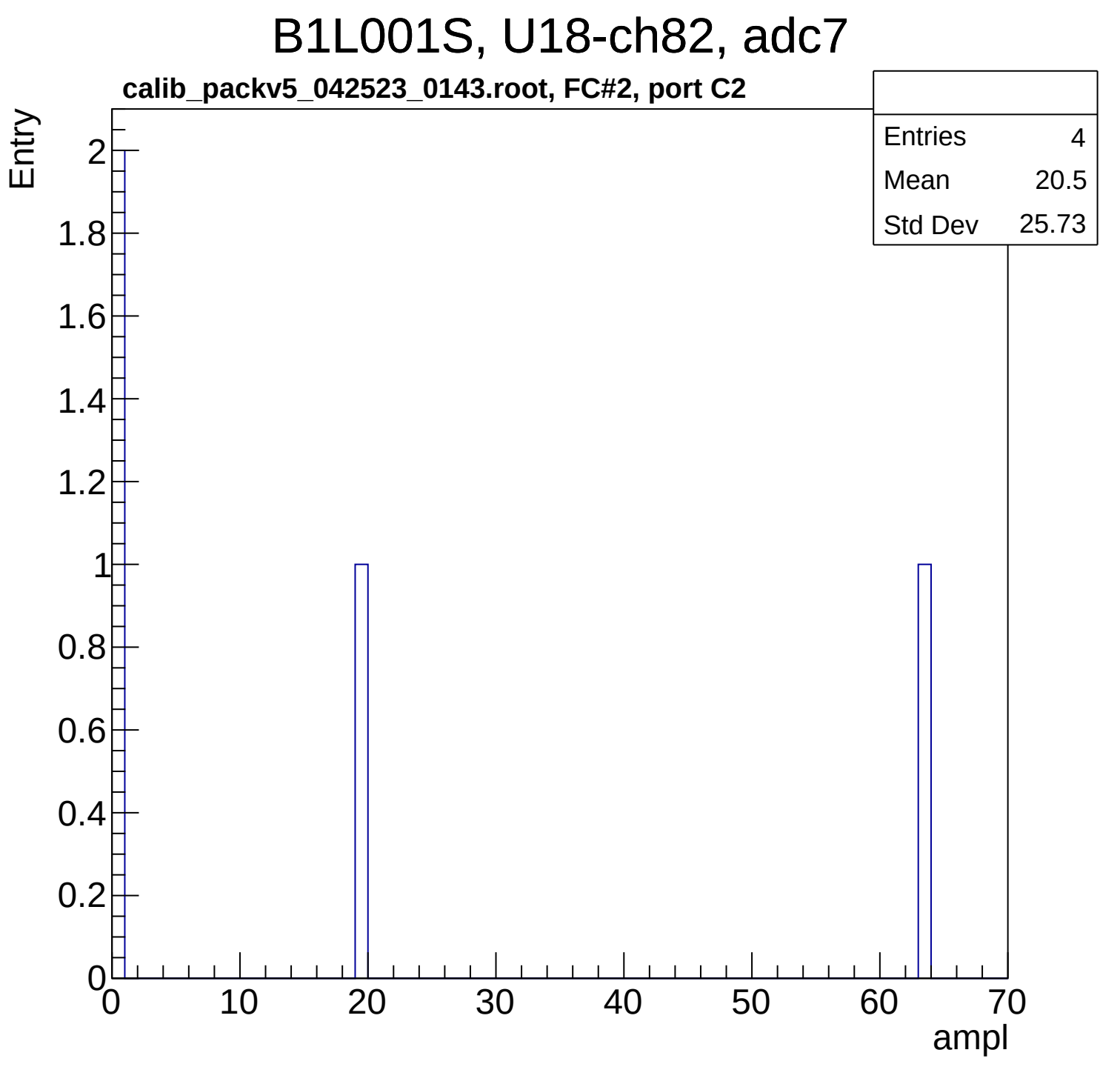

B1L001S, U18-ch82, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 111
Mean 41.89
Std Dev 3.33
Gaus mean : 42.7048
Gaus Width: 3.1475
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

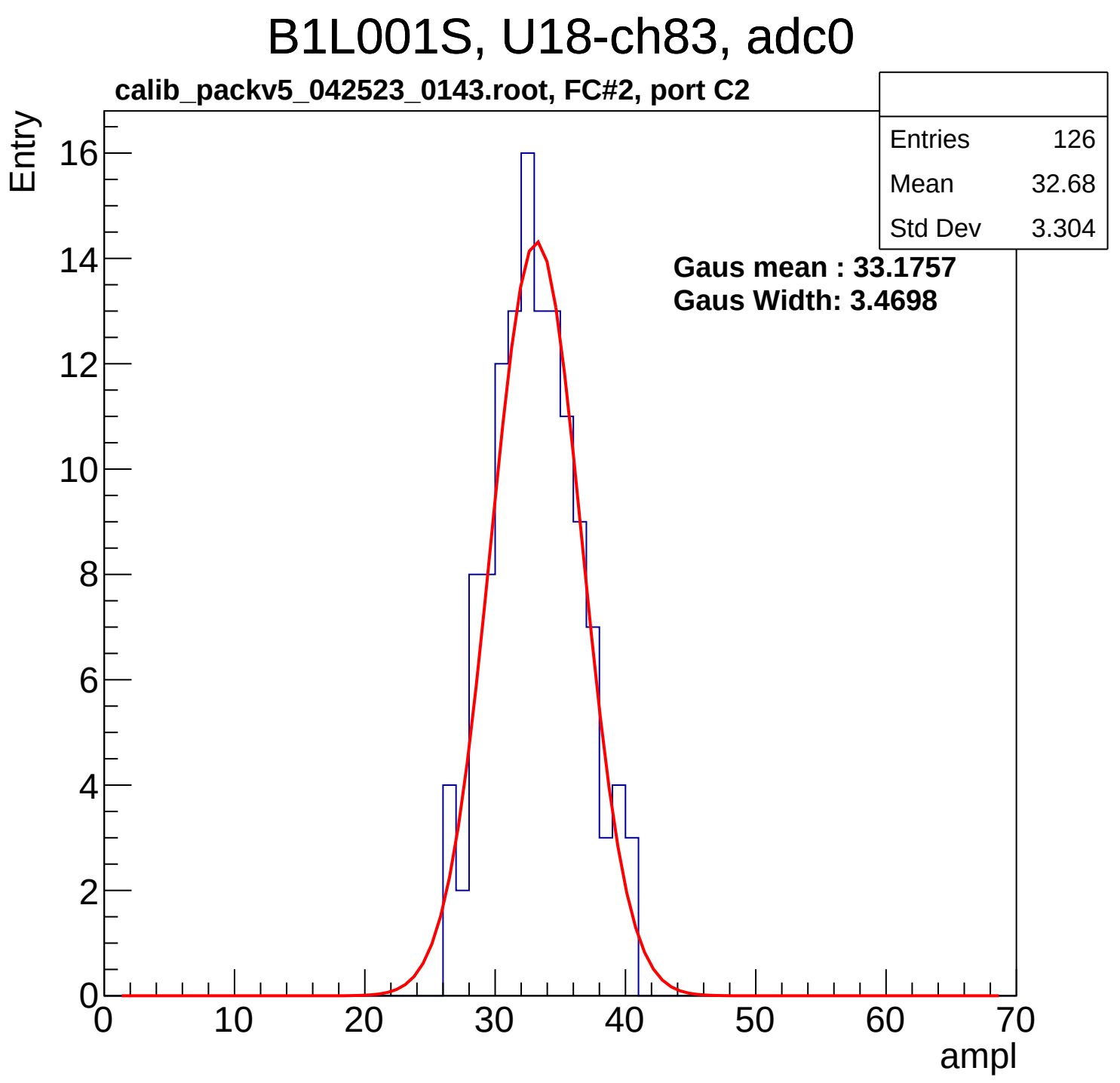

B1L001S, U18-ch82, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 142
Mean 48.43
Std Dev 3.733
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

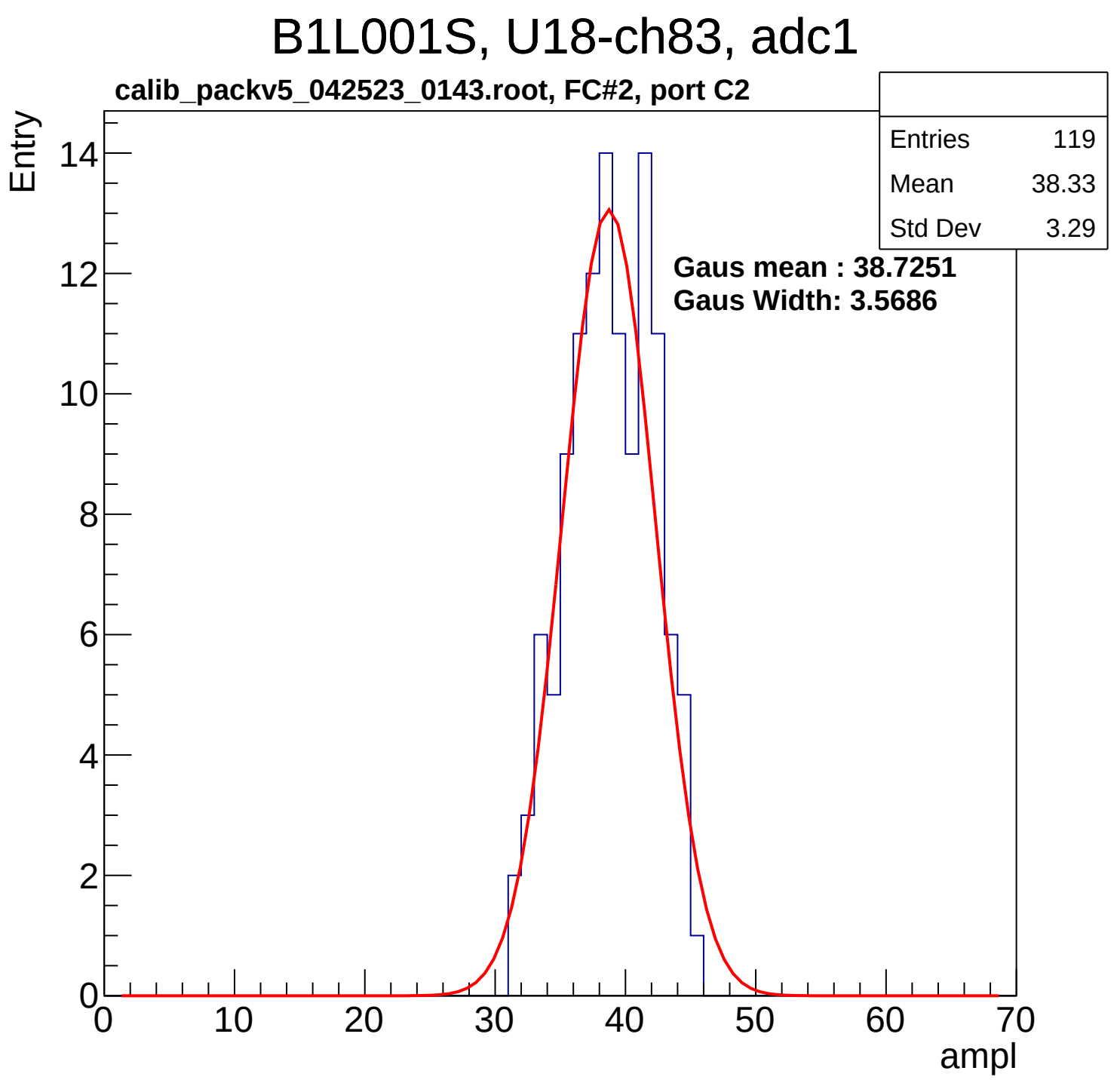

B1L001S, U18-ch82, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 114
Mean 54.53
Std Dev 3.555
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl

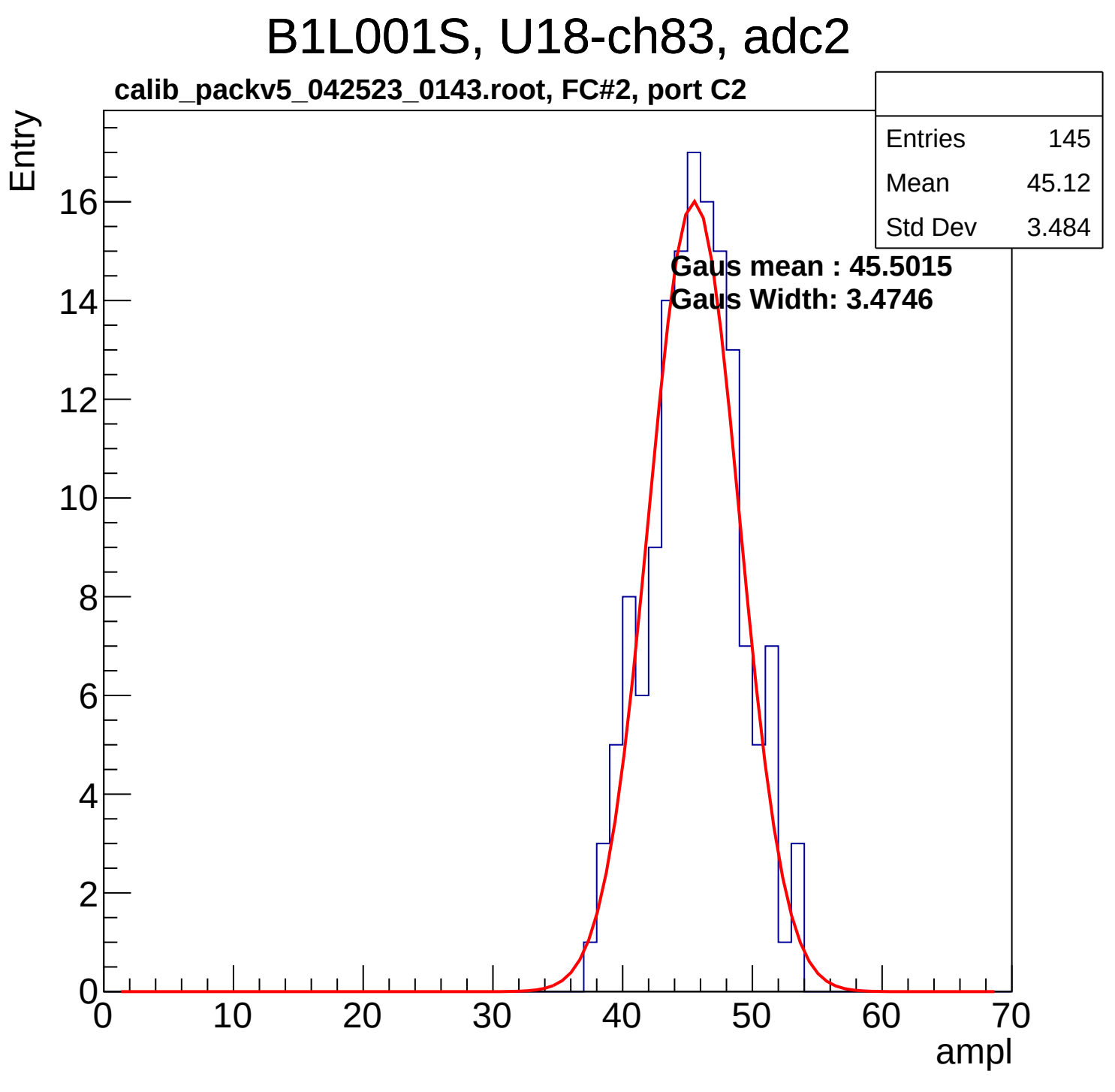

B1L001S, U18-ch82, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 98
Mean 59.37
Std Dev 2.529
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

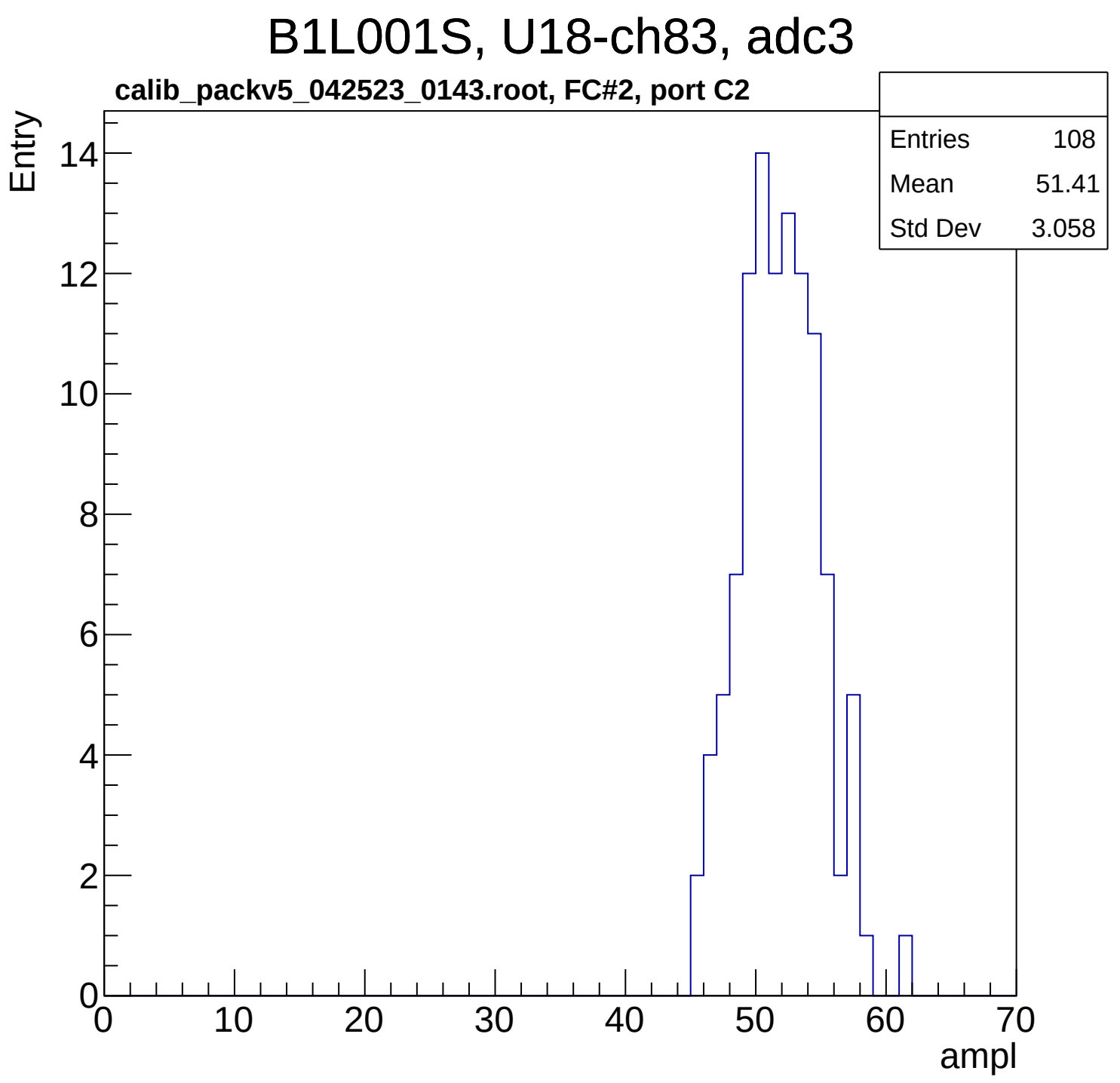

B1L001S, U18-ch82, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 22
Mean 56.14
Std Dev 17.79
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

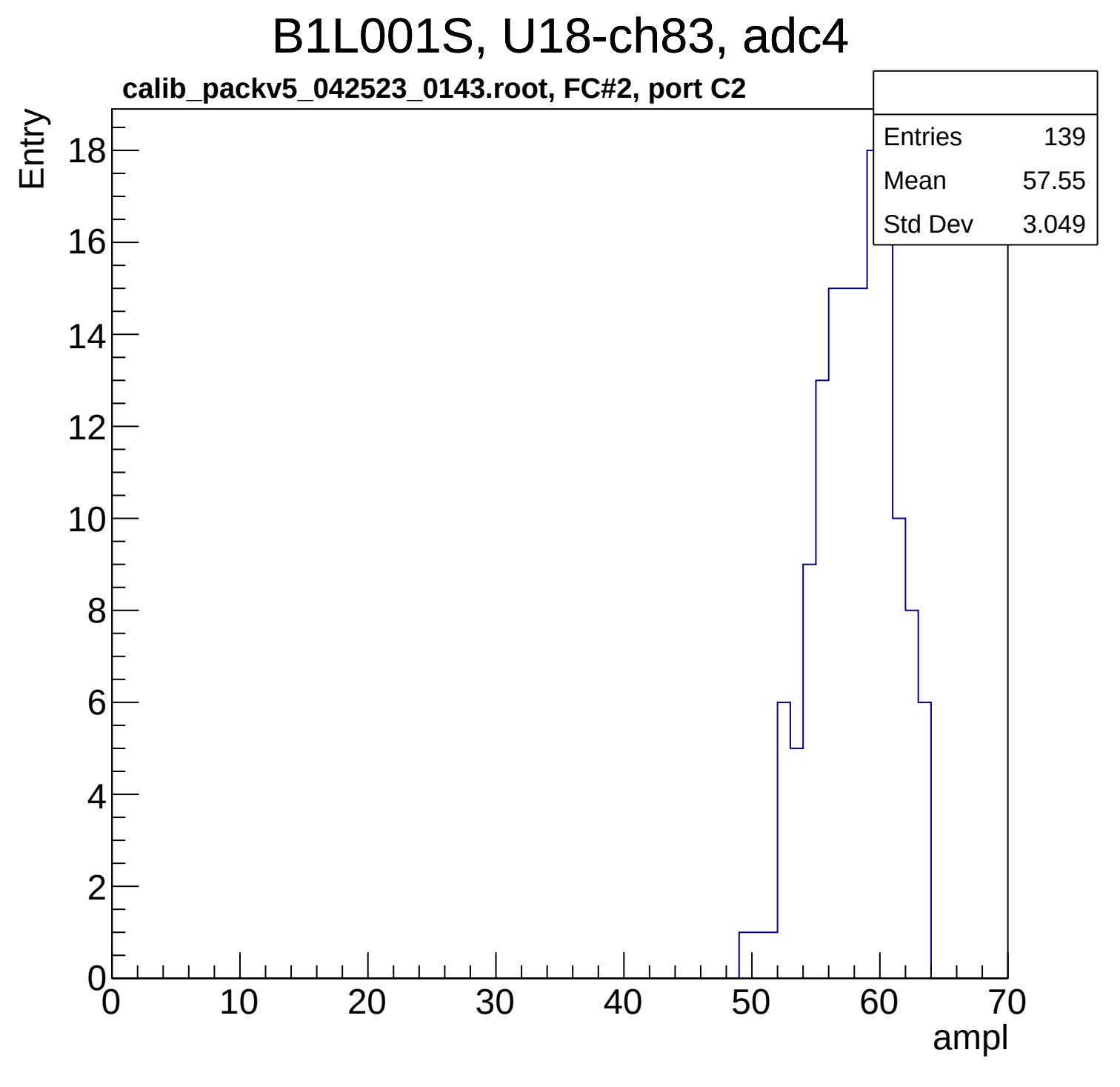

B1L001S, U18-ch82, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 4
Mean 20.5
Std Dev 25.73
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

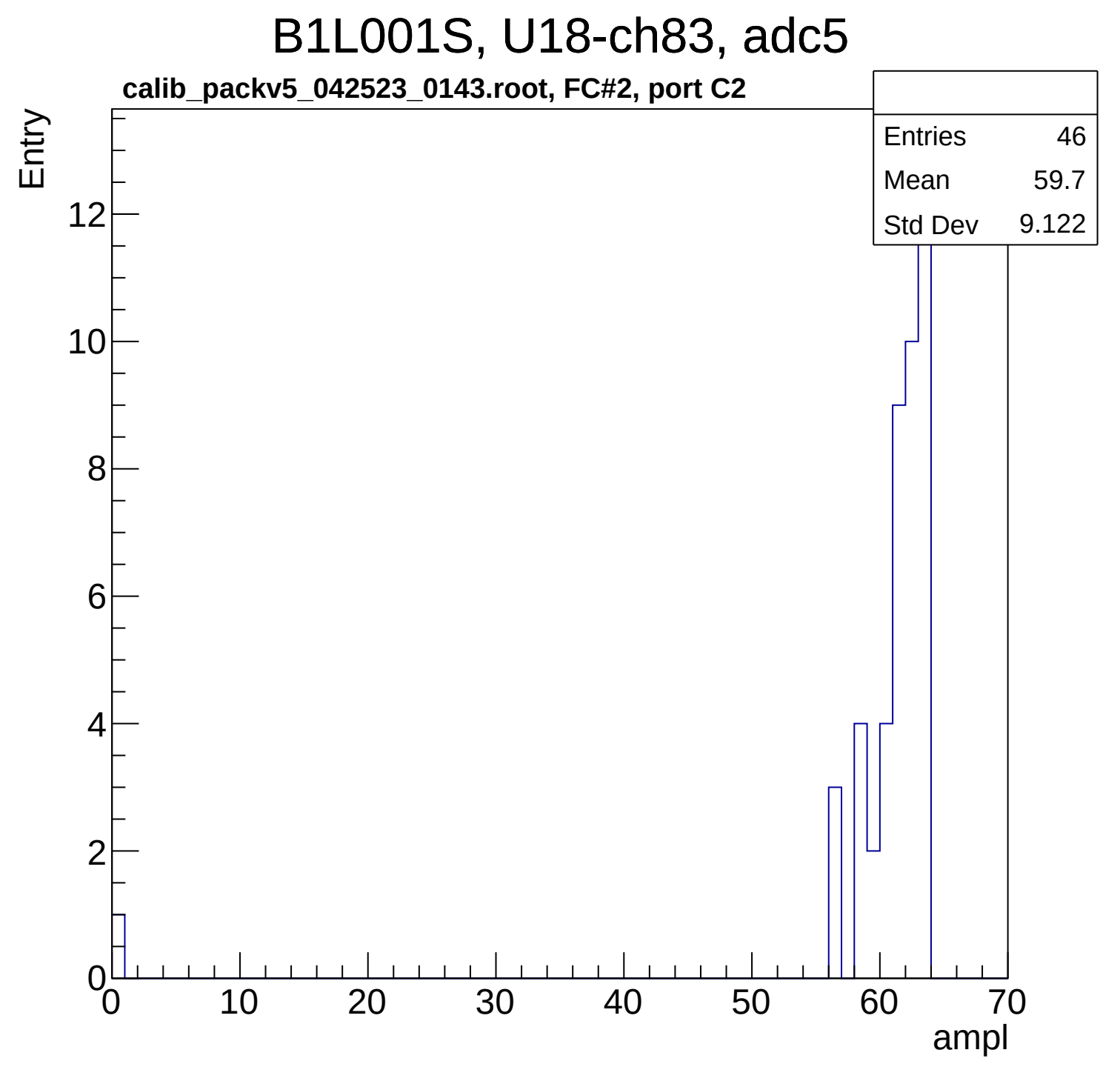

B1L001S, U18-ch83, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 126
Mean 32.68
Std Dev 3.304
Gaus mean : 33.1757
Gaus Width: 3.4698
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

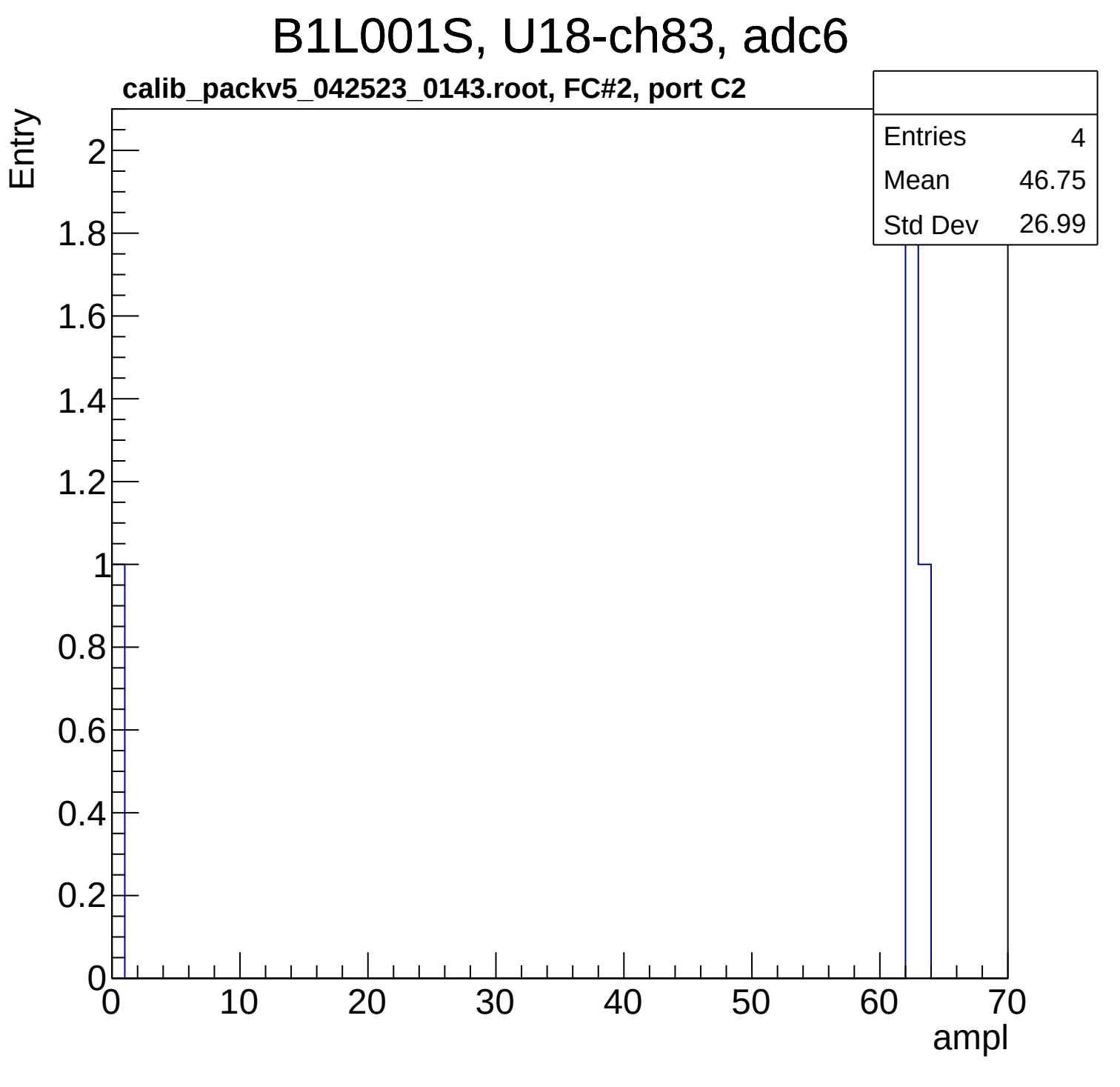

B1L001S, U18-ch83, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 119
Mean 38.33
Std Dev 3.29
Gaus mean : 38.7251
Gaus Width: 3.5686
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

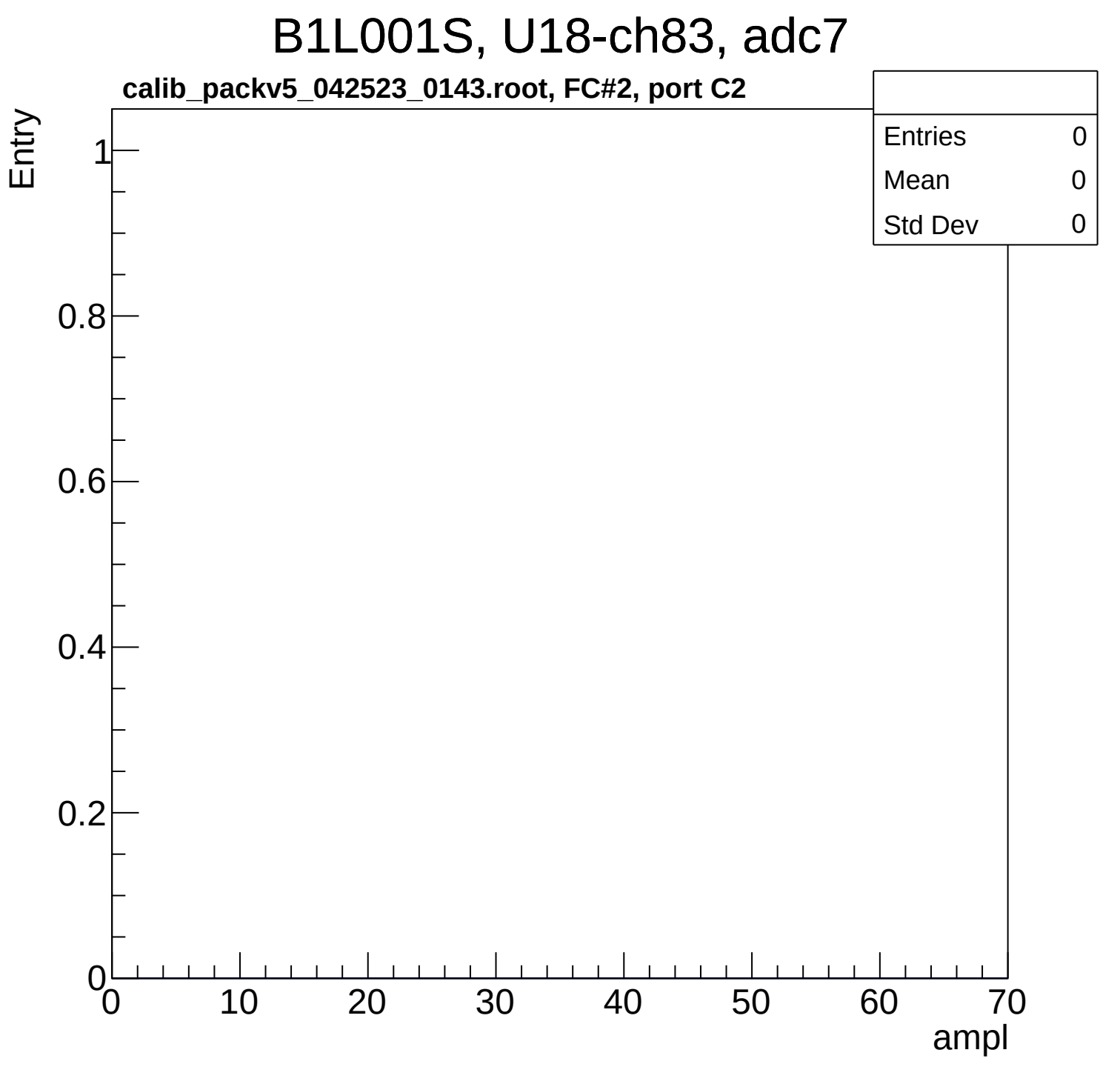

B1L001S, U18-ch83, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 145
Mean 45.12
Std Dev 3.484
Gaus mean : 45.5015
Gaus Width: 3.4746
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

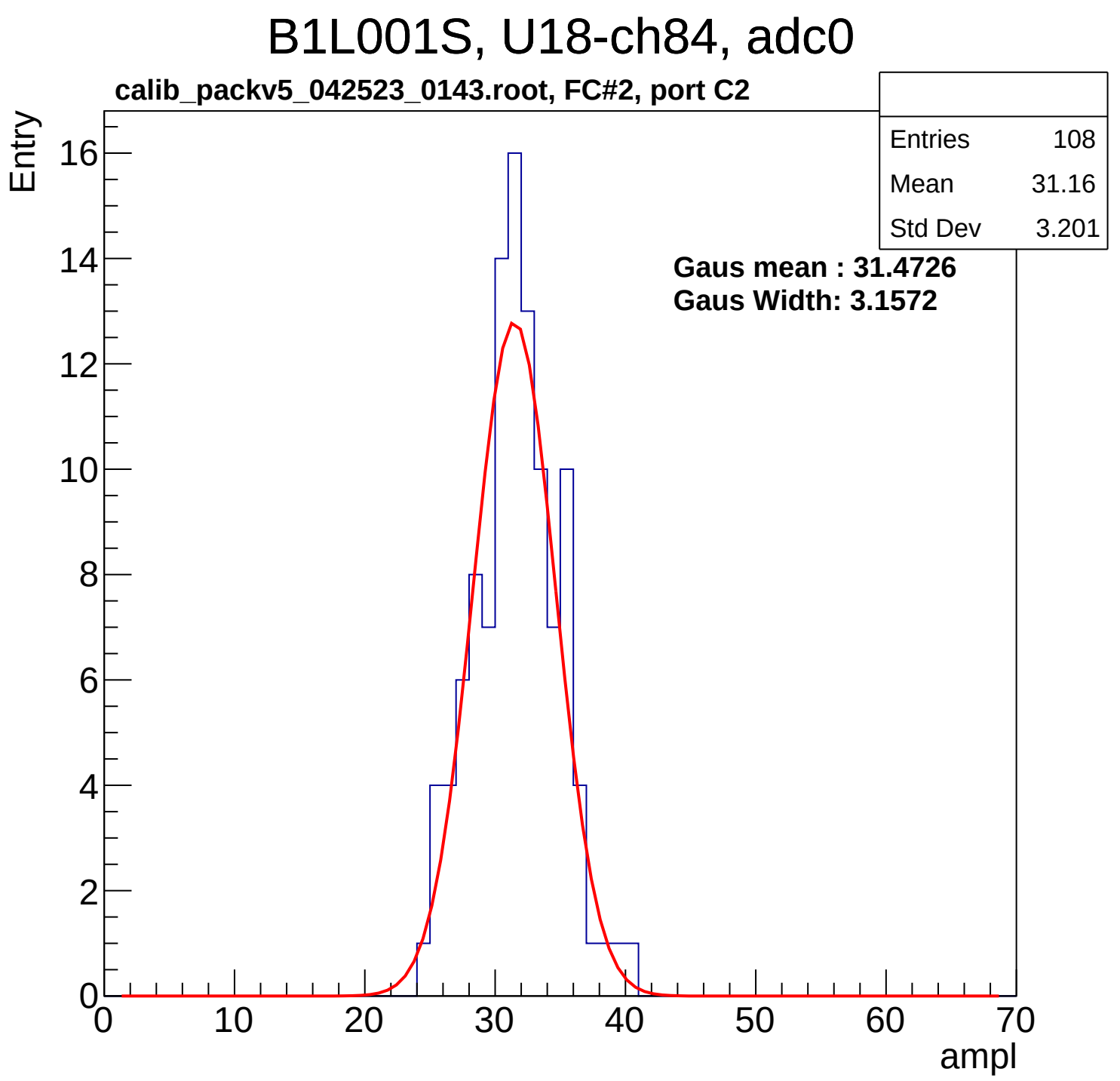

B1L001S, U18-ch83, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 108
Mean 51.41
Std Dev 3.058
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

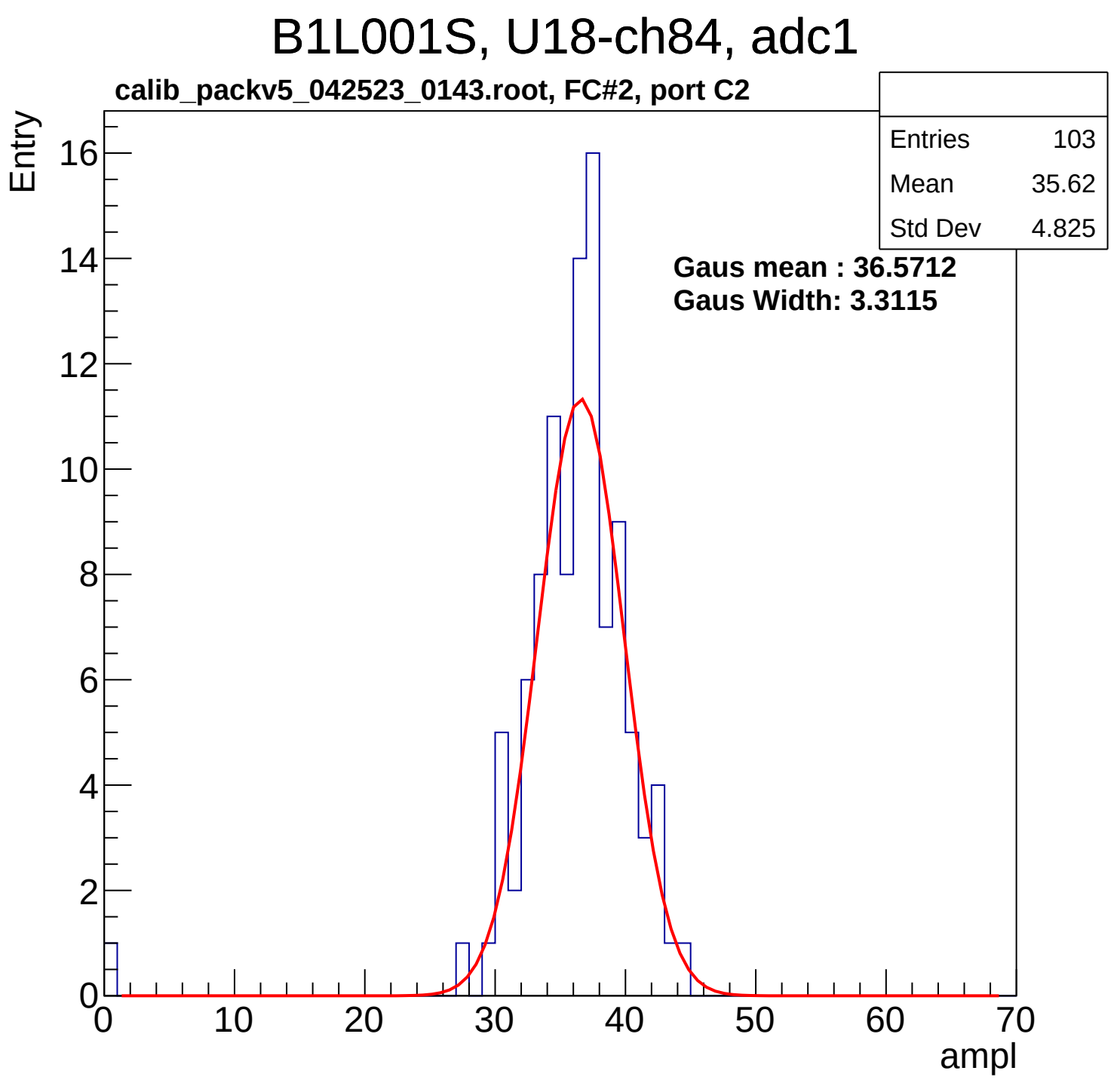

B1L001S, U18-ch83, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 139
Mean 57.55
Std Dev 3.049
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

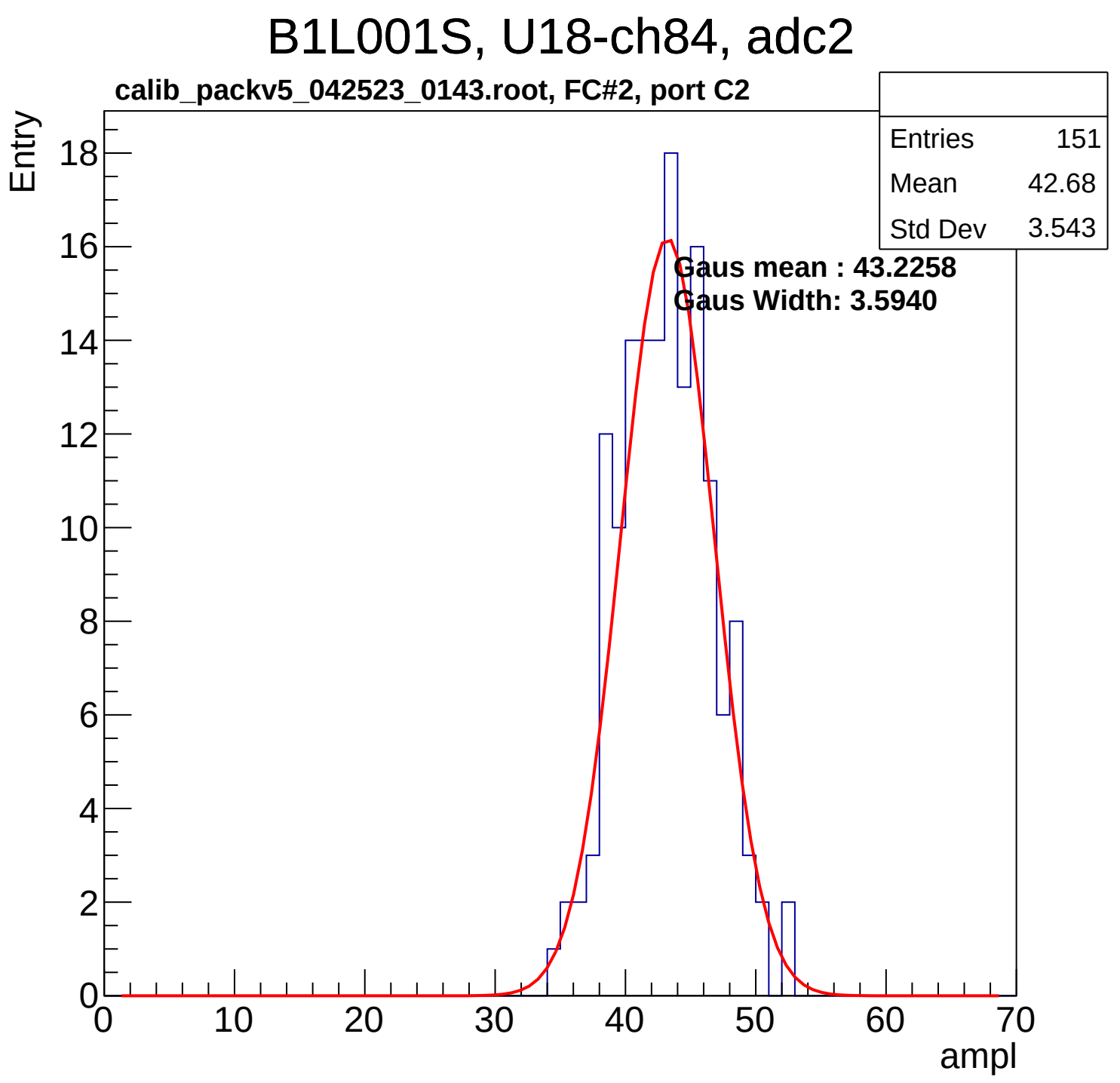

B1L001S, U18-ch83, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 46
Mean 59.7
Std Dev 9.122
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70

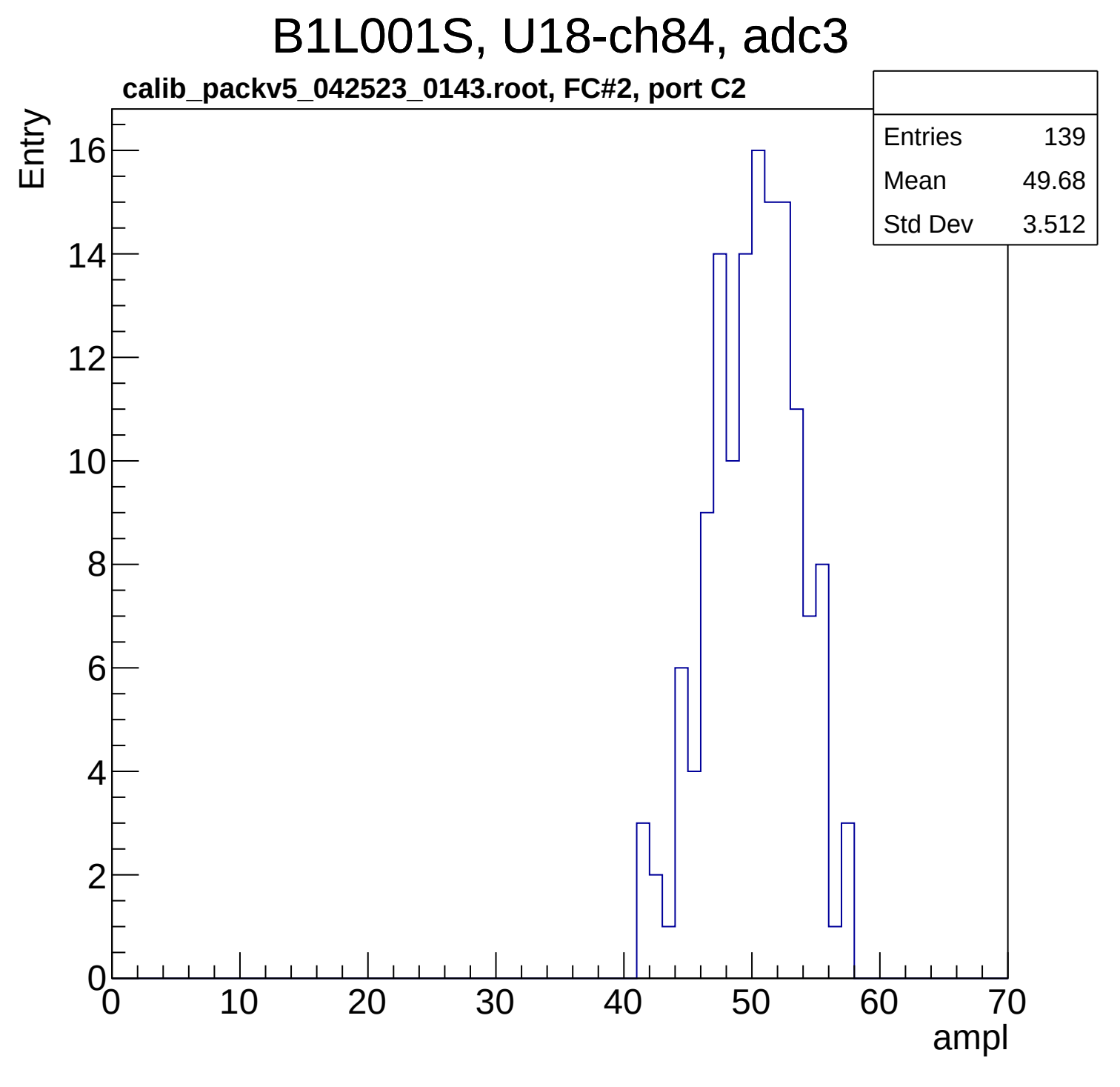

B1L001S, U18-ch83, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 4
Mean 46.75
Std Dev 26.99
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

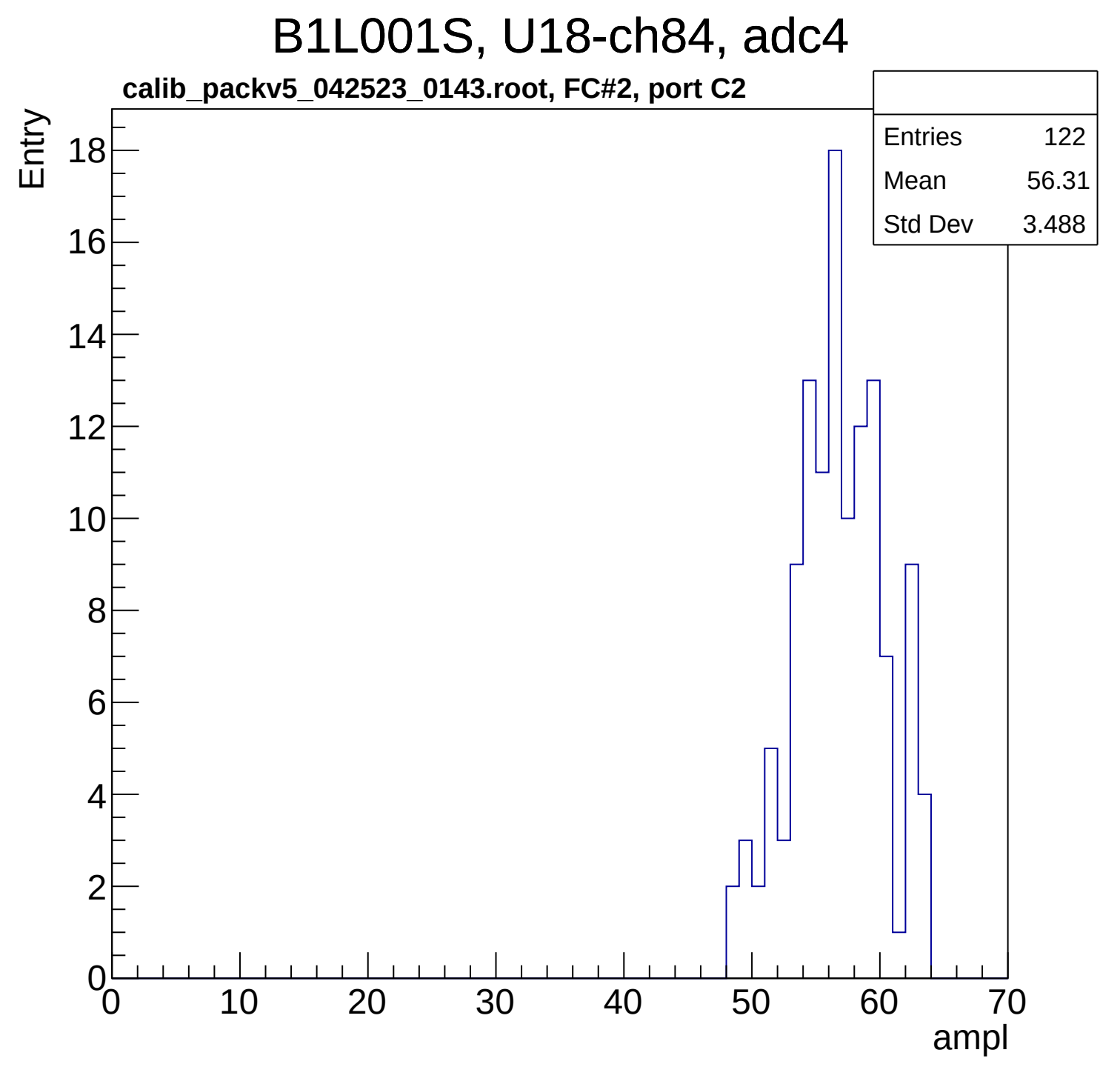

B1L001S, U18-ch83, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

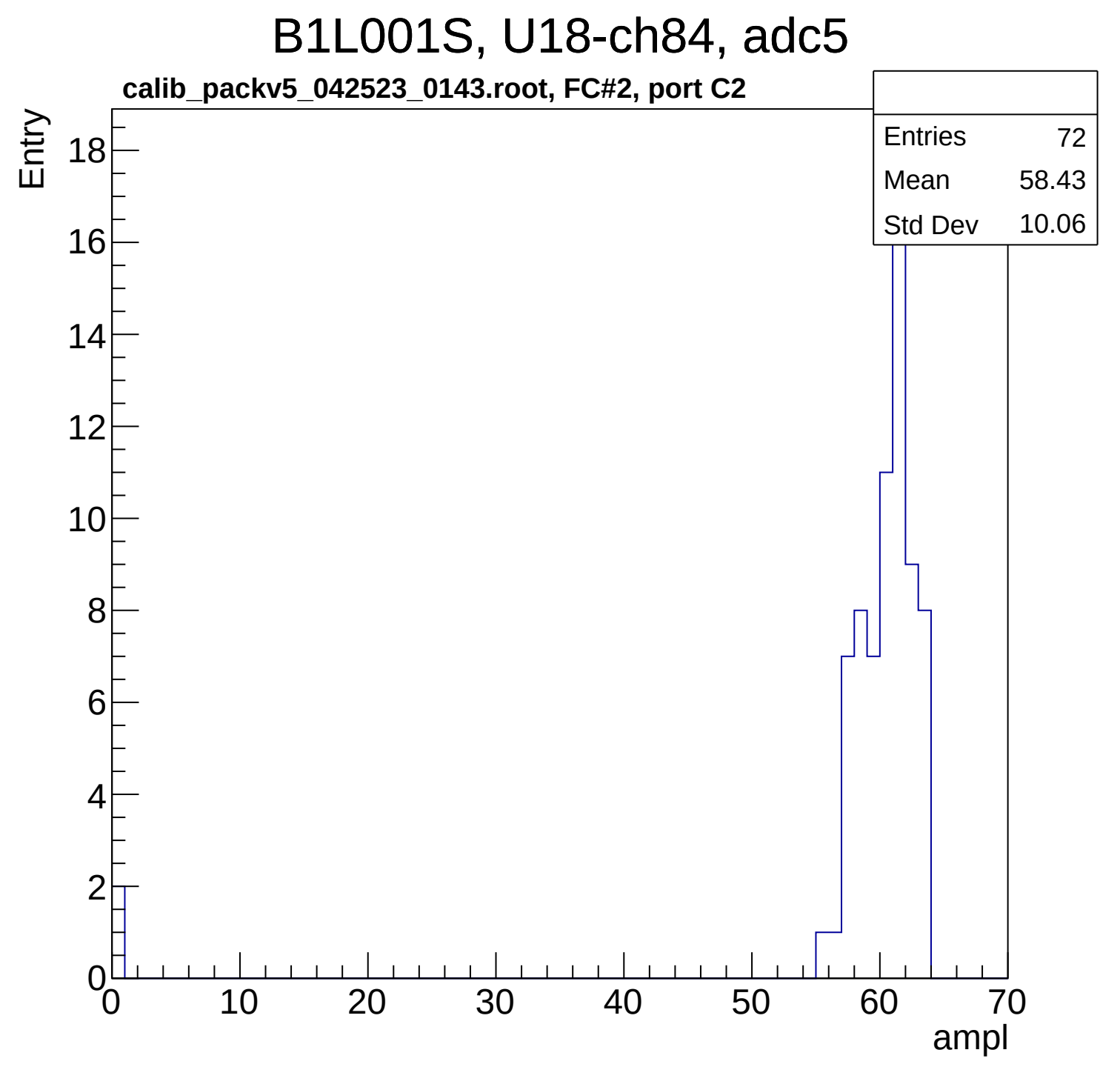

B1L001S, U18-ch84, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 108
Mean 31.16
Std Dev 3.201
Gaus mean : 31.4726
Gaus Width: 3.1572
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

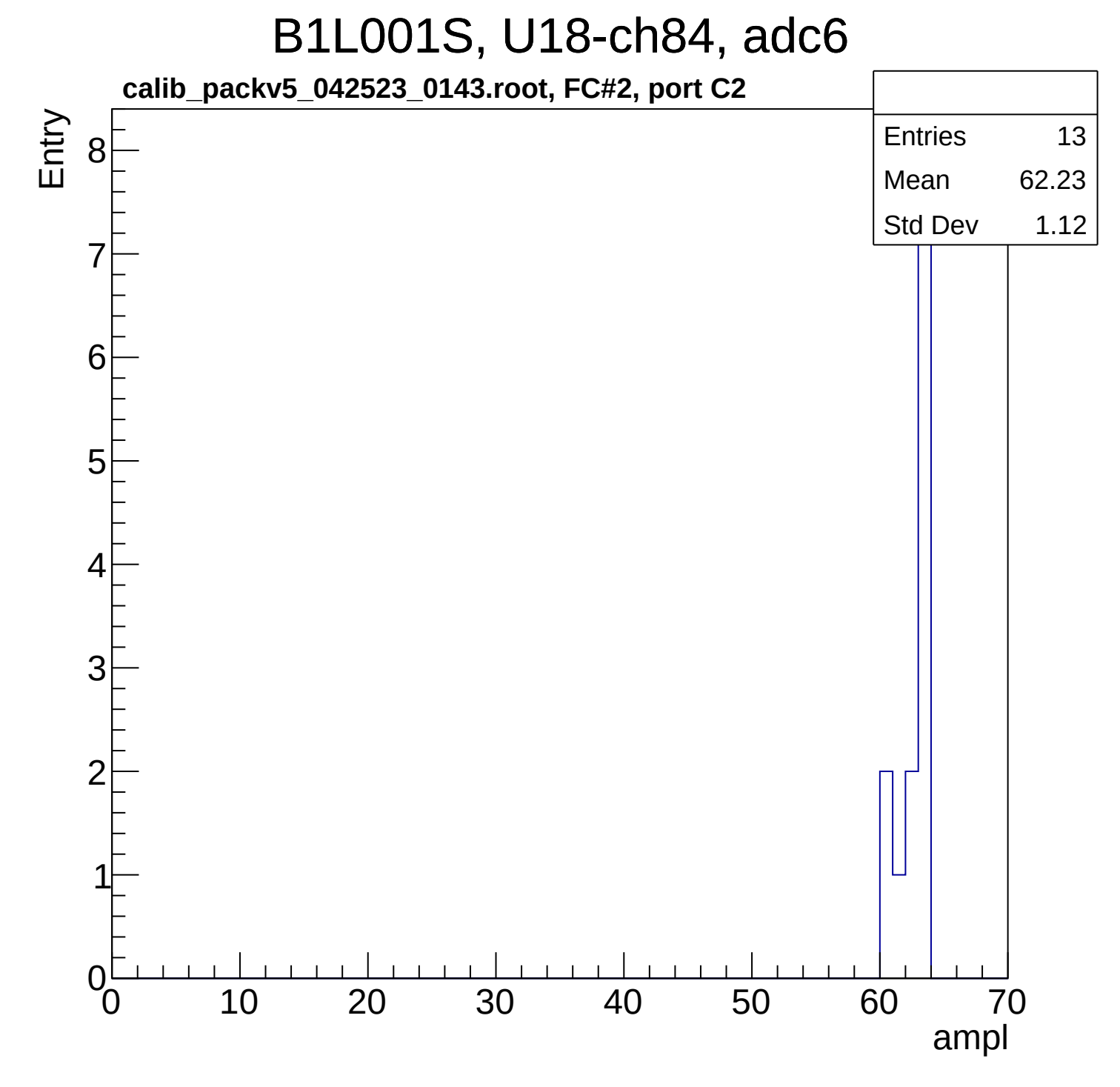

B1L001S, U18-ch84, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 103
Mean 35.62
Std Dev 4.825
Gaus mean : 36.5712
Gaus Width: 3.3115
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

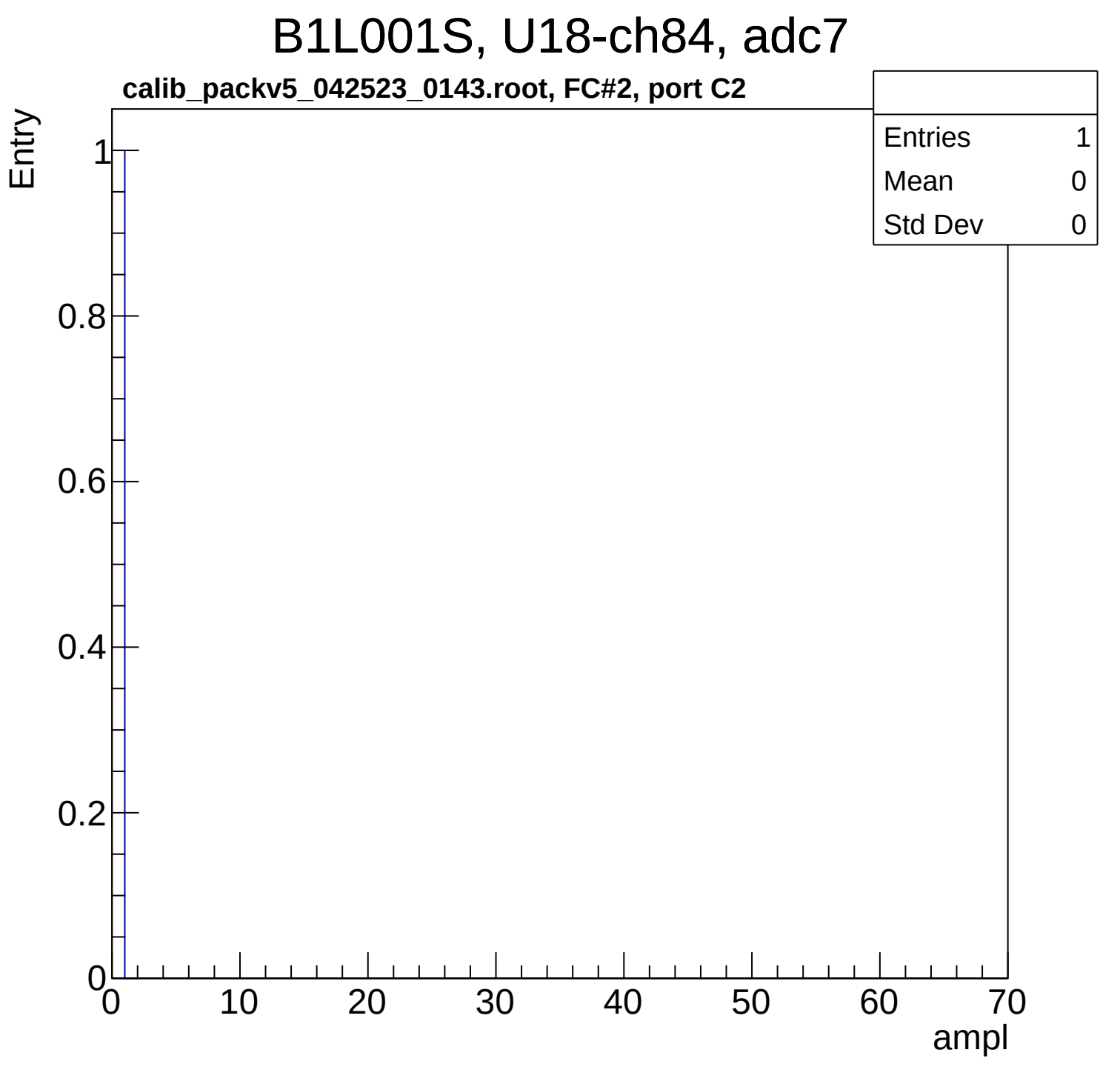

B1L001S, U18-ch84, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 151
Mean 42.68
Std Dev 3.543
Gaus mean : 43.2258
Gaus Width: 3.5940
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

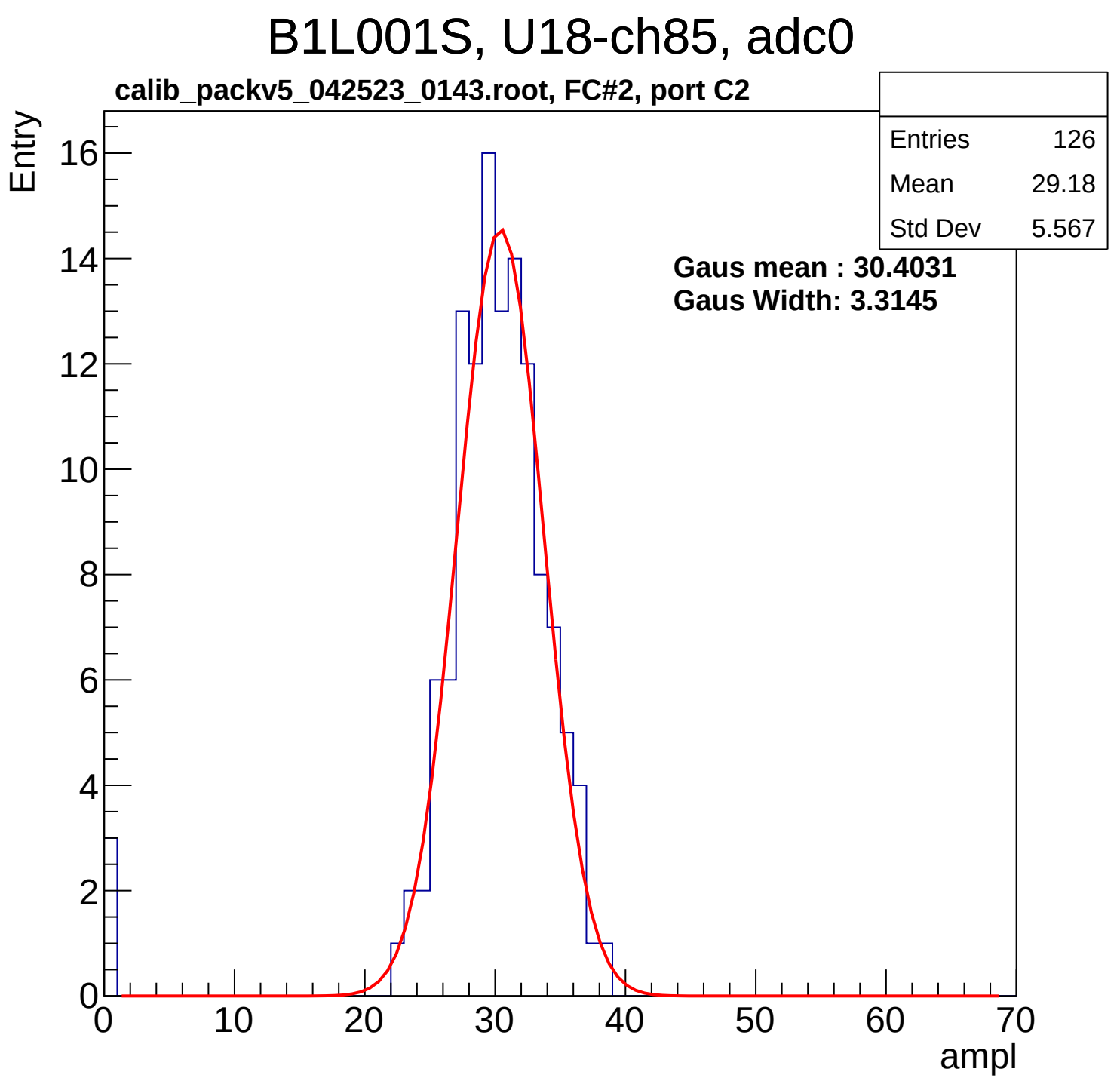

B1L001S, U18-ch84, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 139
Mean 49.68
Std Dev 3.512
Entry
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl

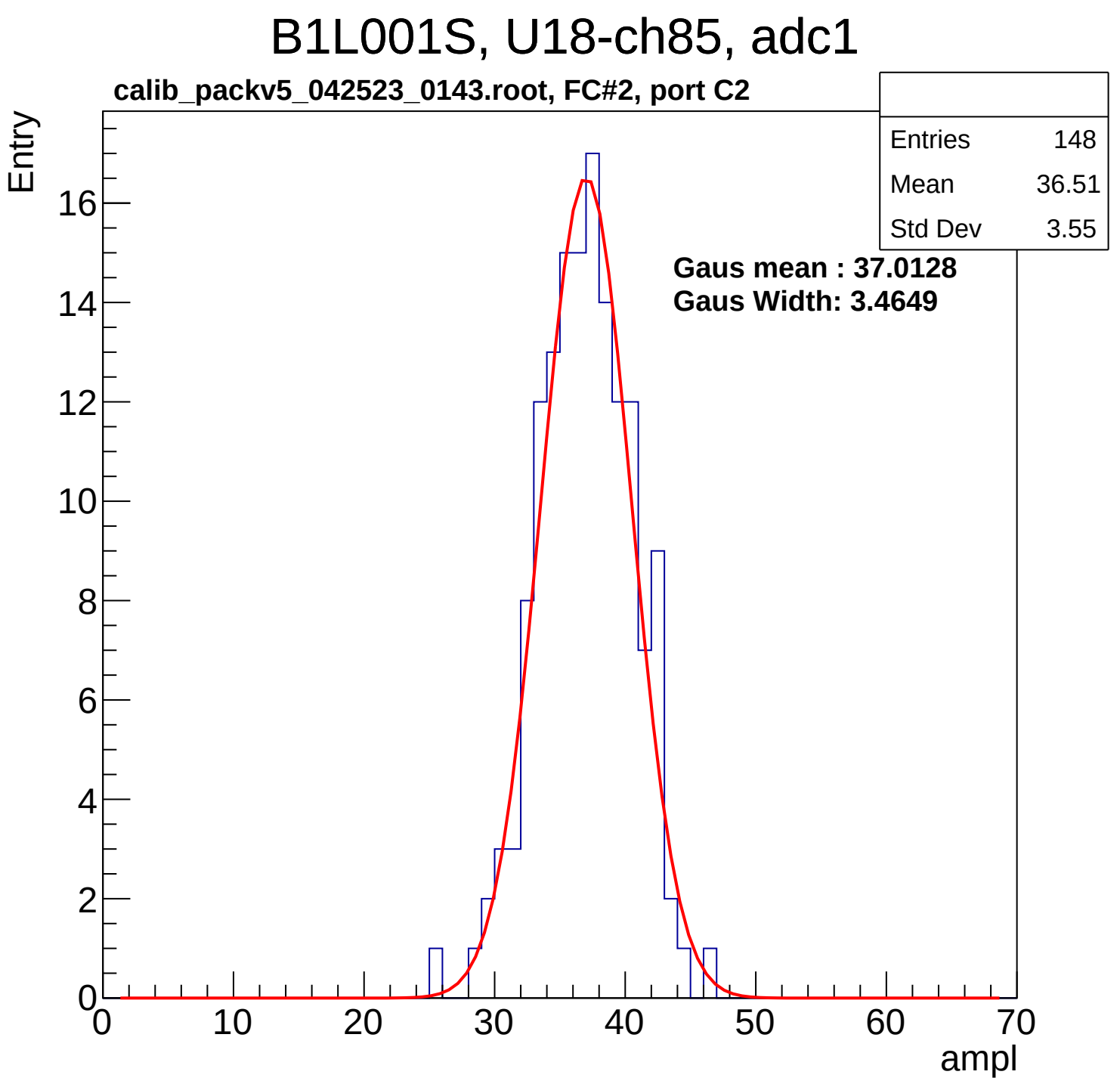

B1L001S, U18-ch84, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 122
Mean 56.31
Std Dev 3.488
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

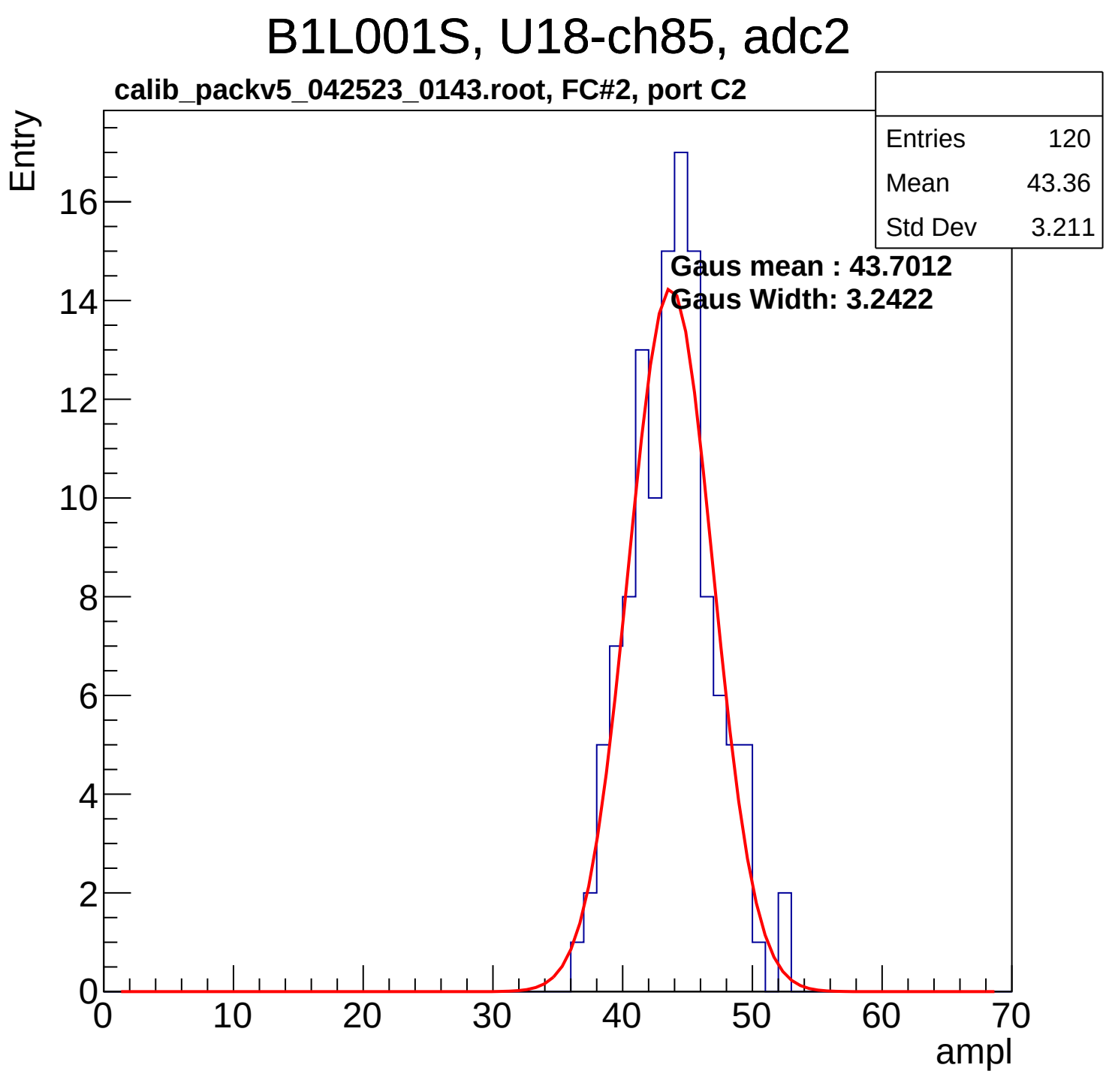

B1L001S, U18-ch84, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 72
Mean 58.43
Std Dev 10.06
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

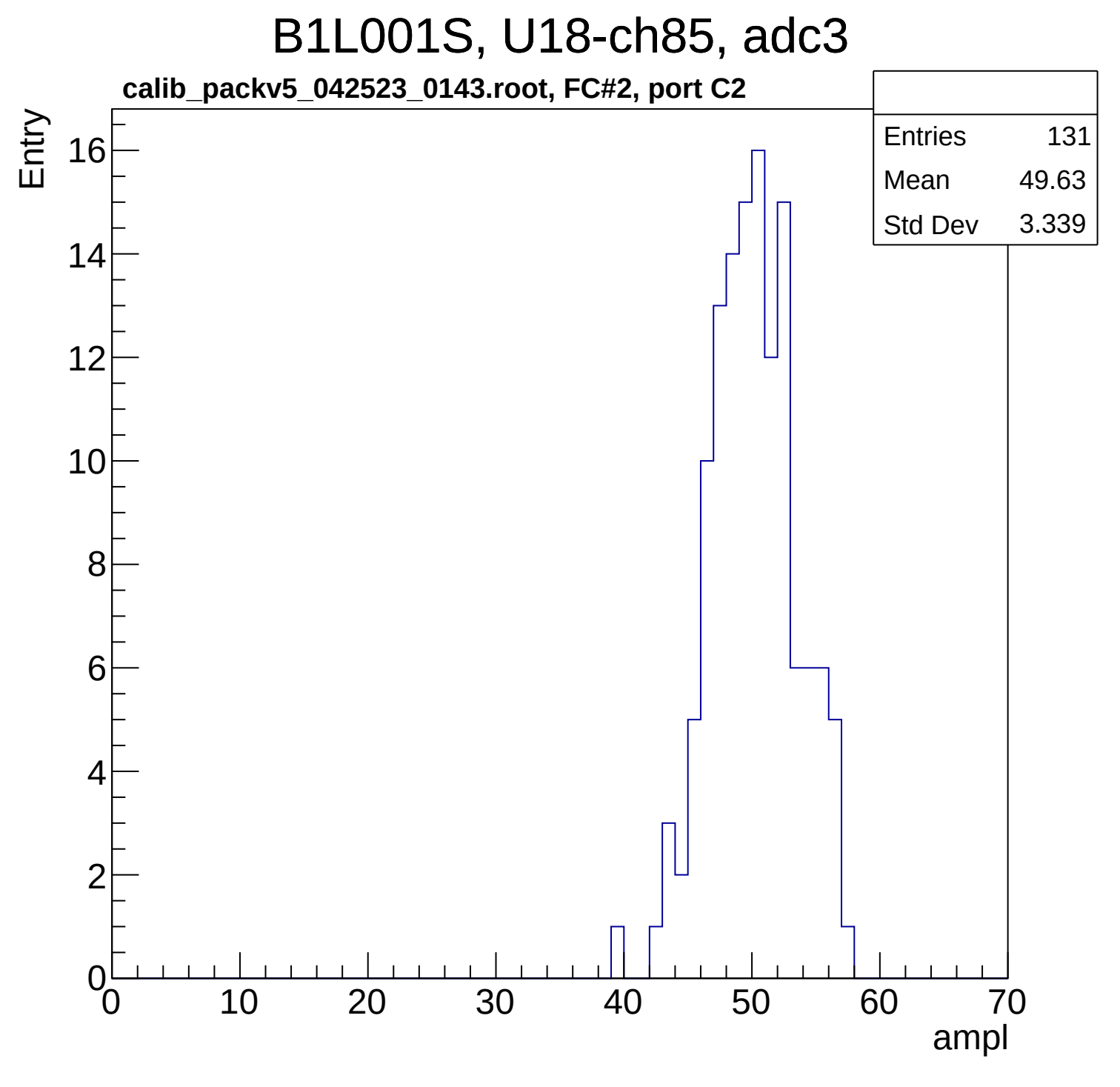

B1L001S, U18-ch84, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 13
Mean 62.23
Std Dev 1.12
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

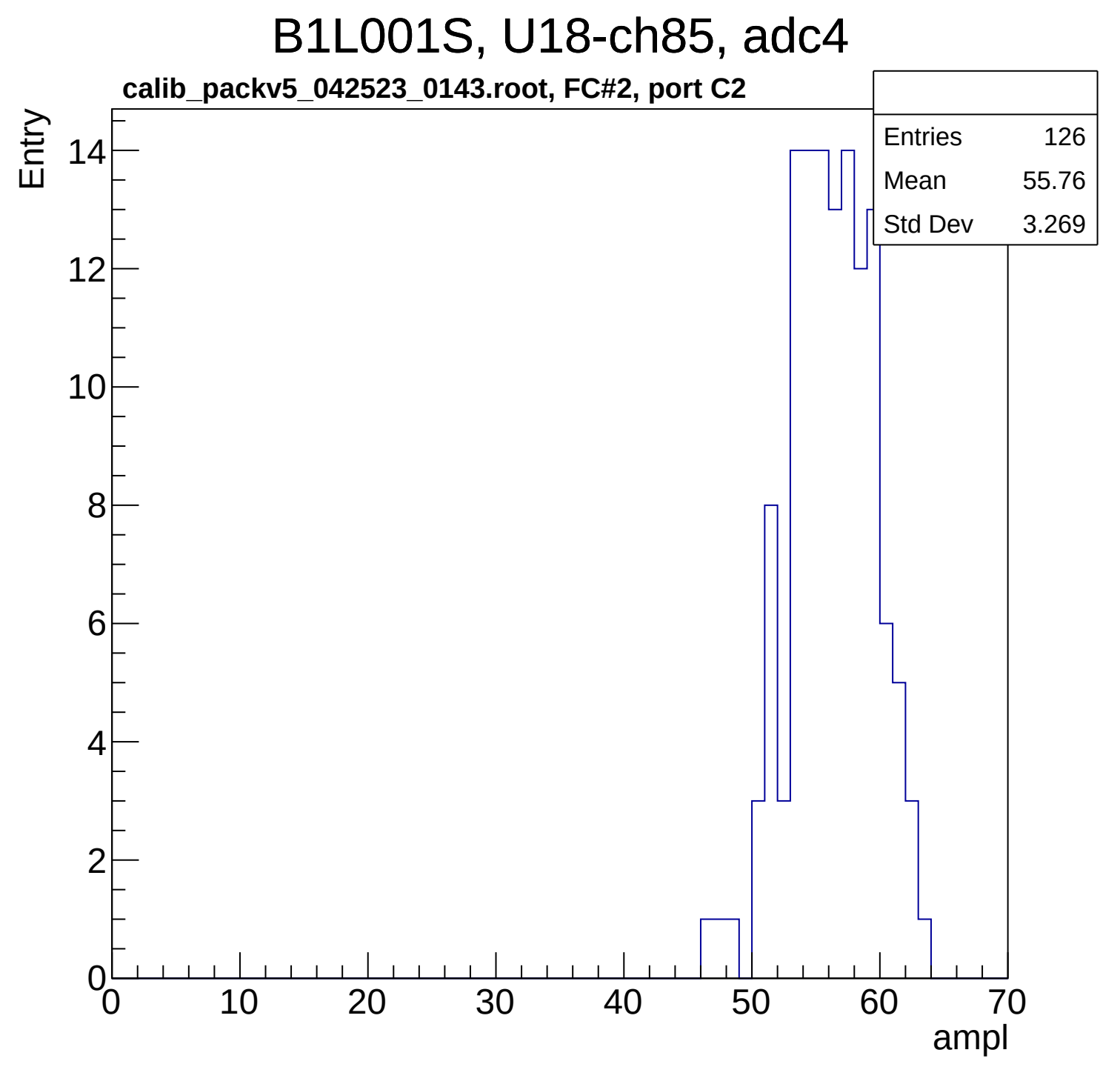

B1L001S, U18-ch84, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

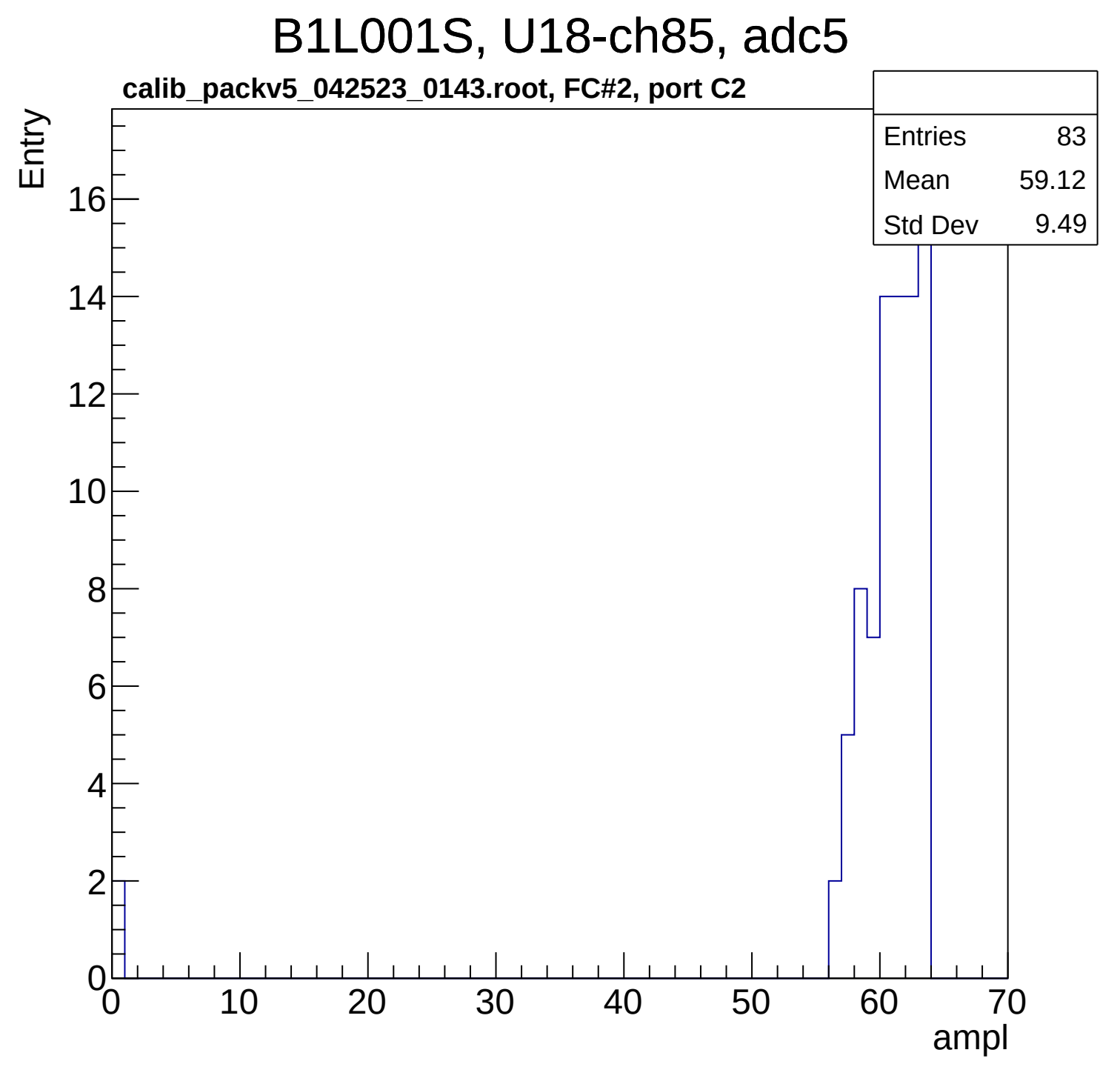

B1L001S, U18-ch85, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 126
Mean 29.18
Std Dev 5.567
Gaus mean : 30.4031
Gaus Width: 3.3145
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

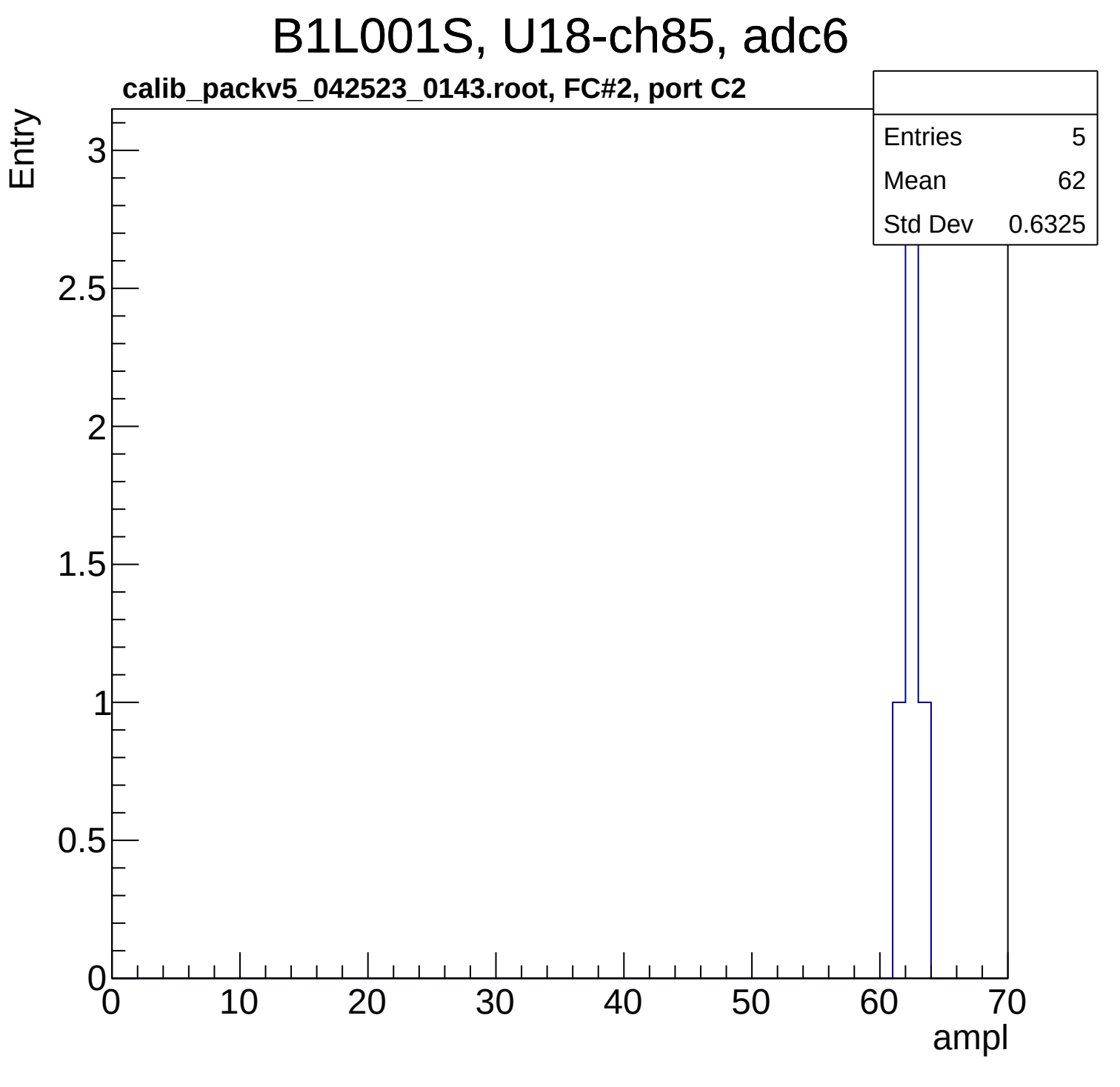

B1L001S, U18-ch85, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 148
Mean 36.51
Std Dev 3.55
Gaus mean : 37.0128
Gaus Width: 3.4649
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

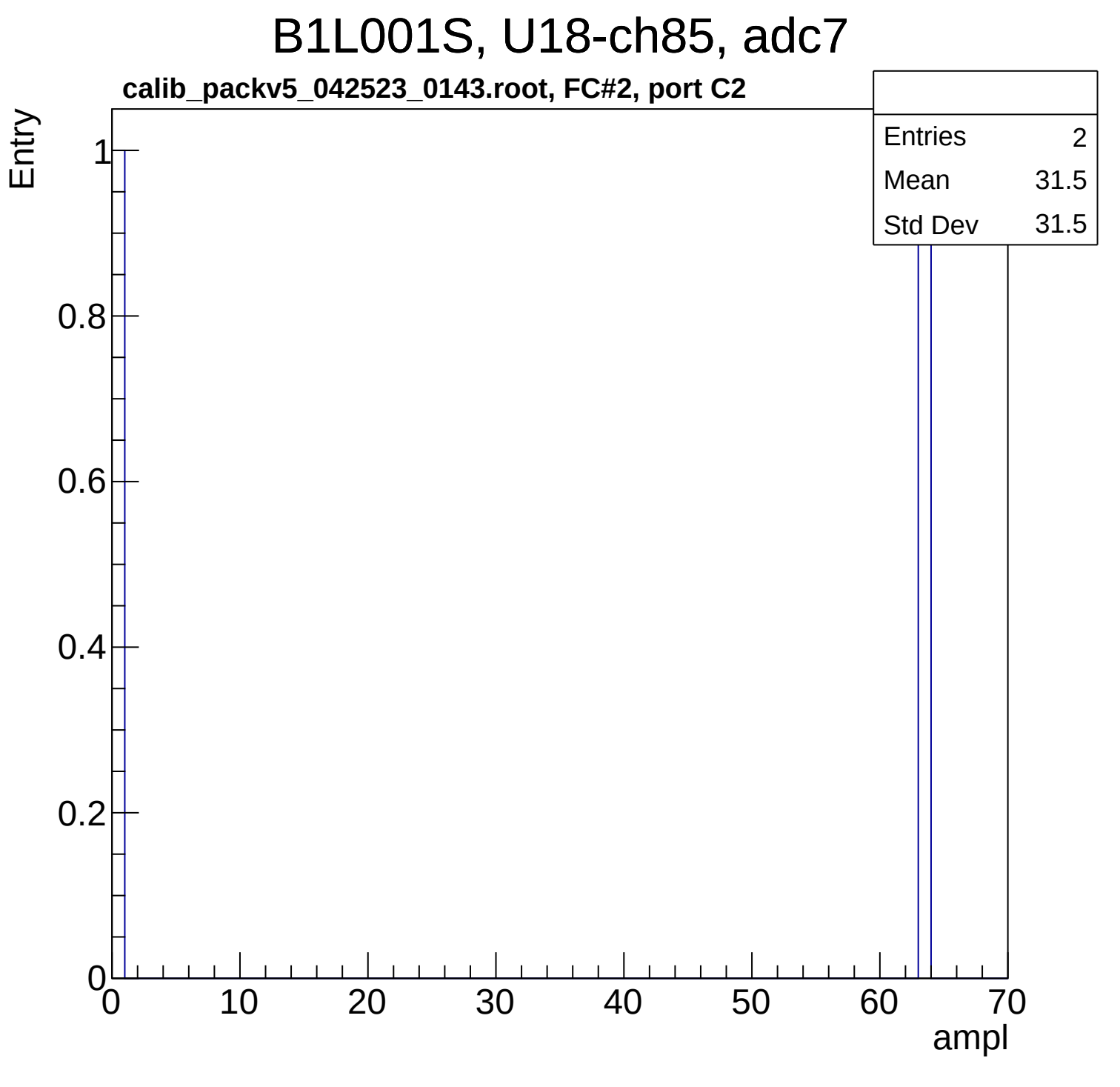

B1L001S, U18-ch85, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 120
Mean 43.36
Std Dev 3.211
Gaus mean : 43.7012
Gaus Width: 3.2422
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

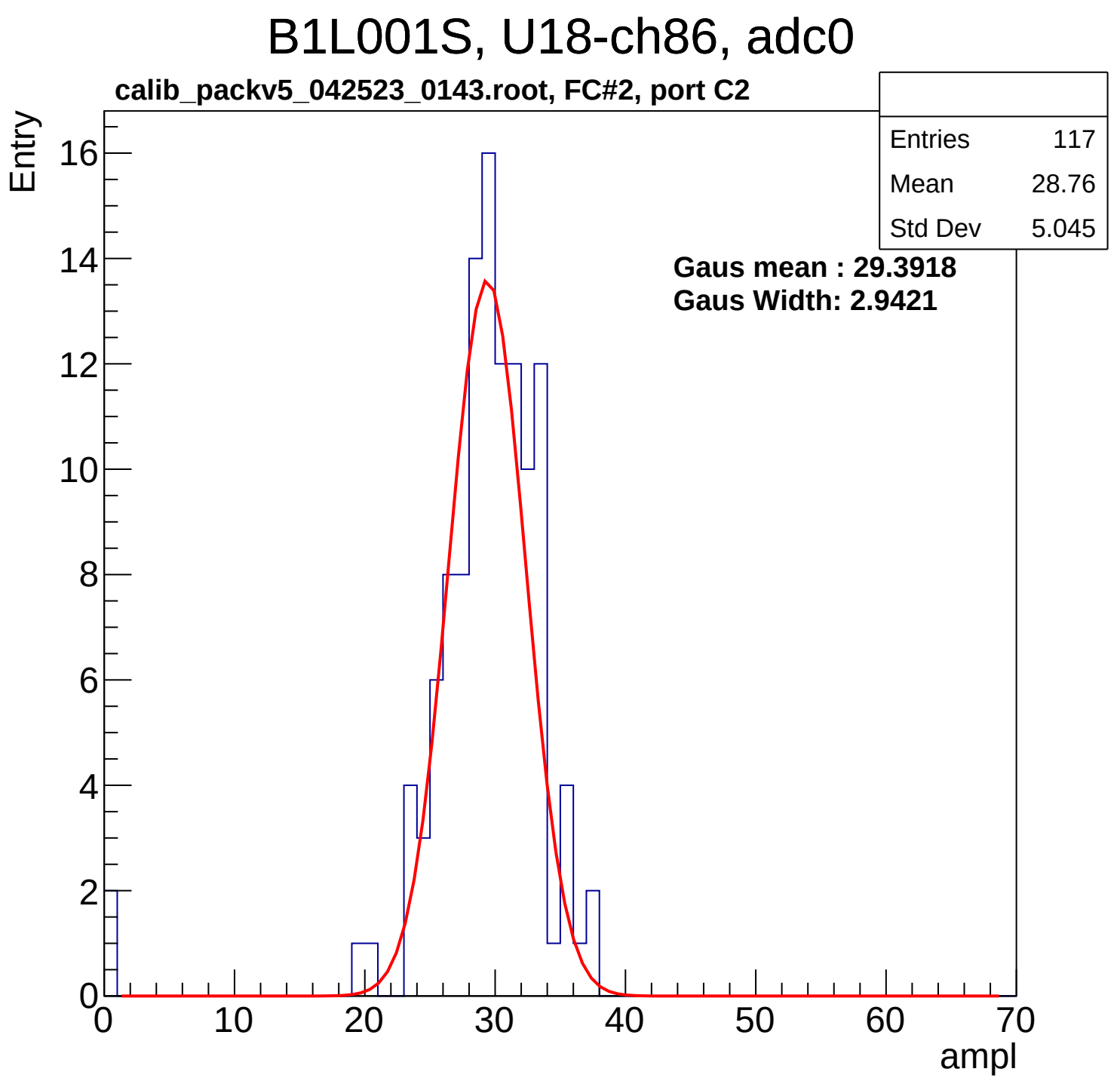

B1L001S, U18-ch85, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 131
Mean 49.63
Std Dev 3.339
Entry
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl

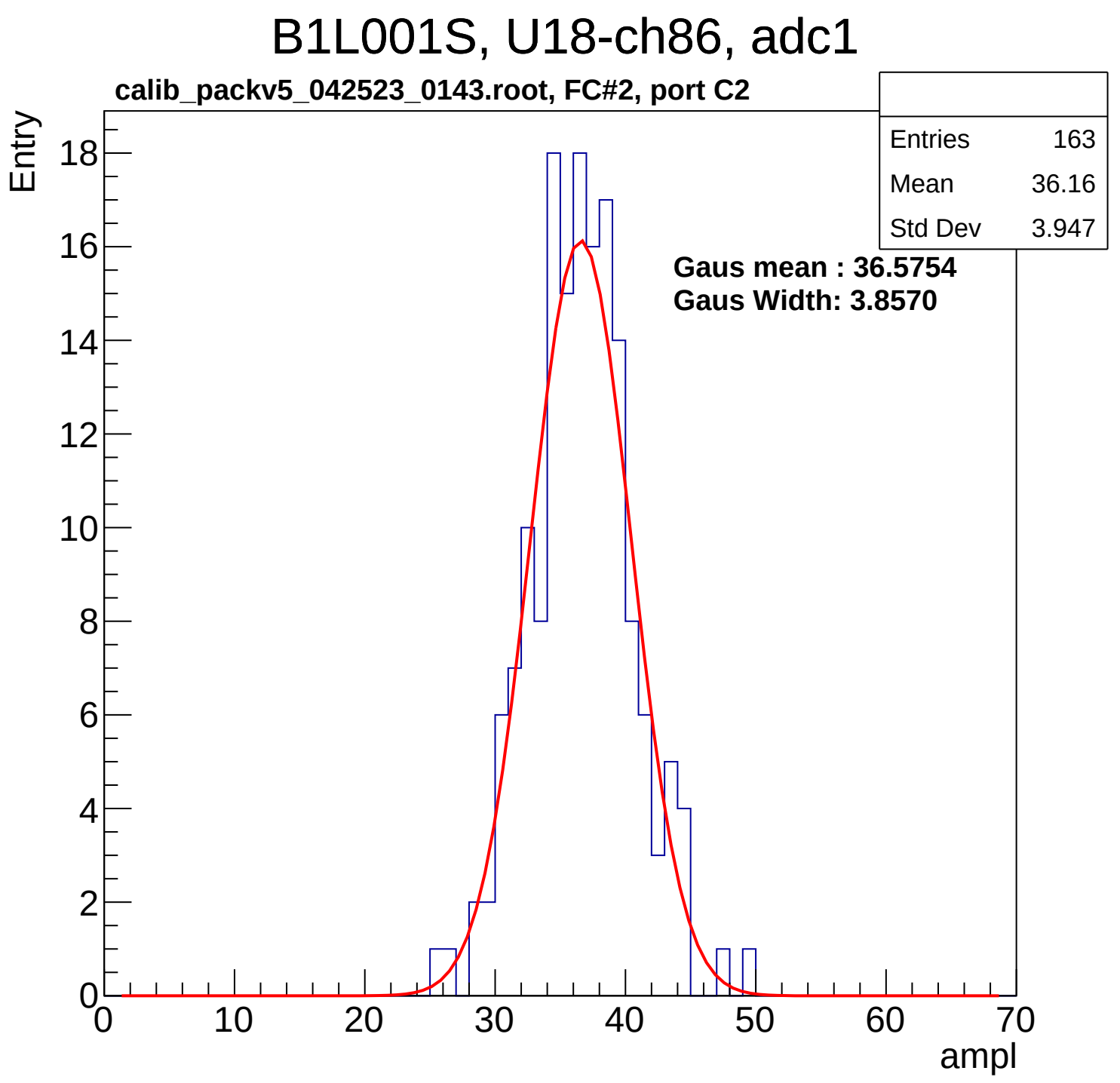

B1L001S, U18-ch85, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 126
Mean 55.76
Std Dev 3.269
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

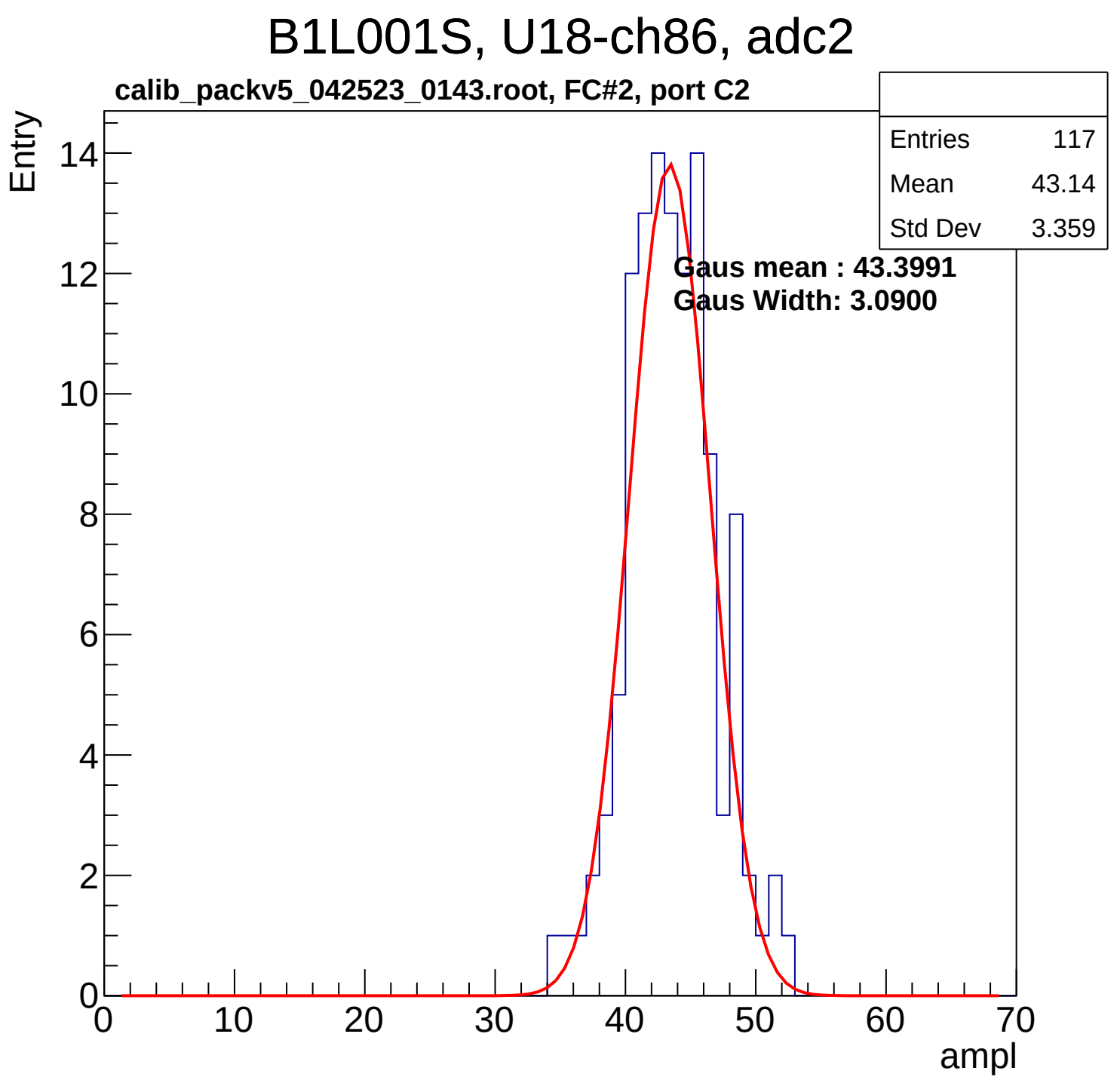

B1L001S, U18-ch85, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 83
Mean 59.12
Std Dev 9.49
Entry
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl

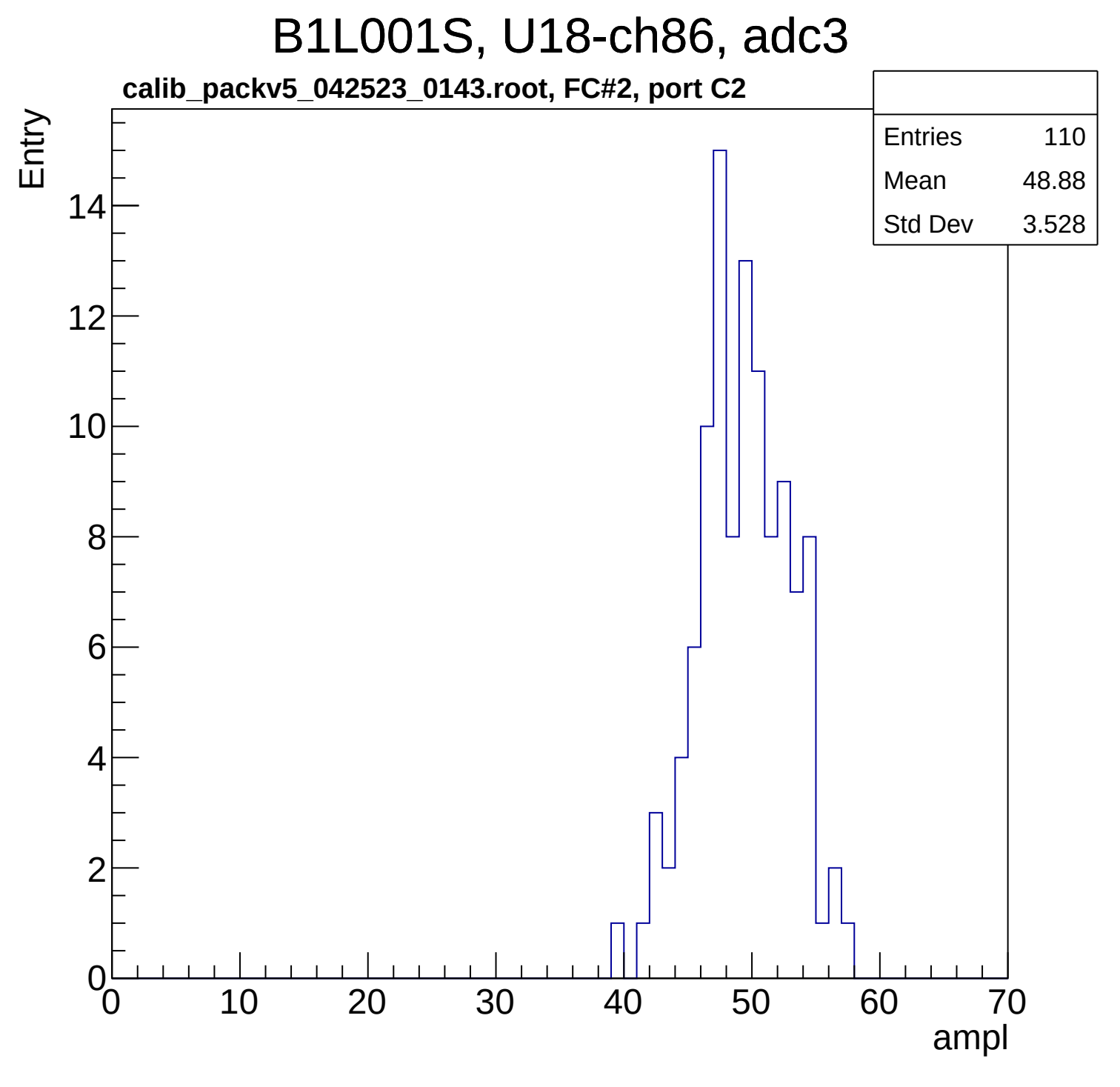

B1L001S, U18-ch85, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 5
Mean 62
Std Dev 0.6325
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

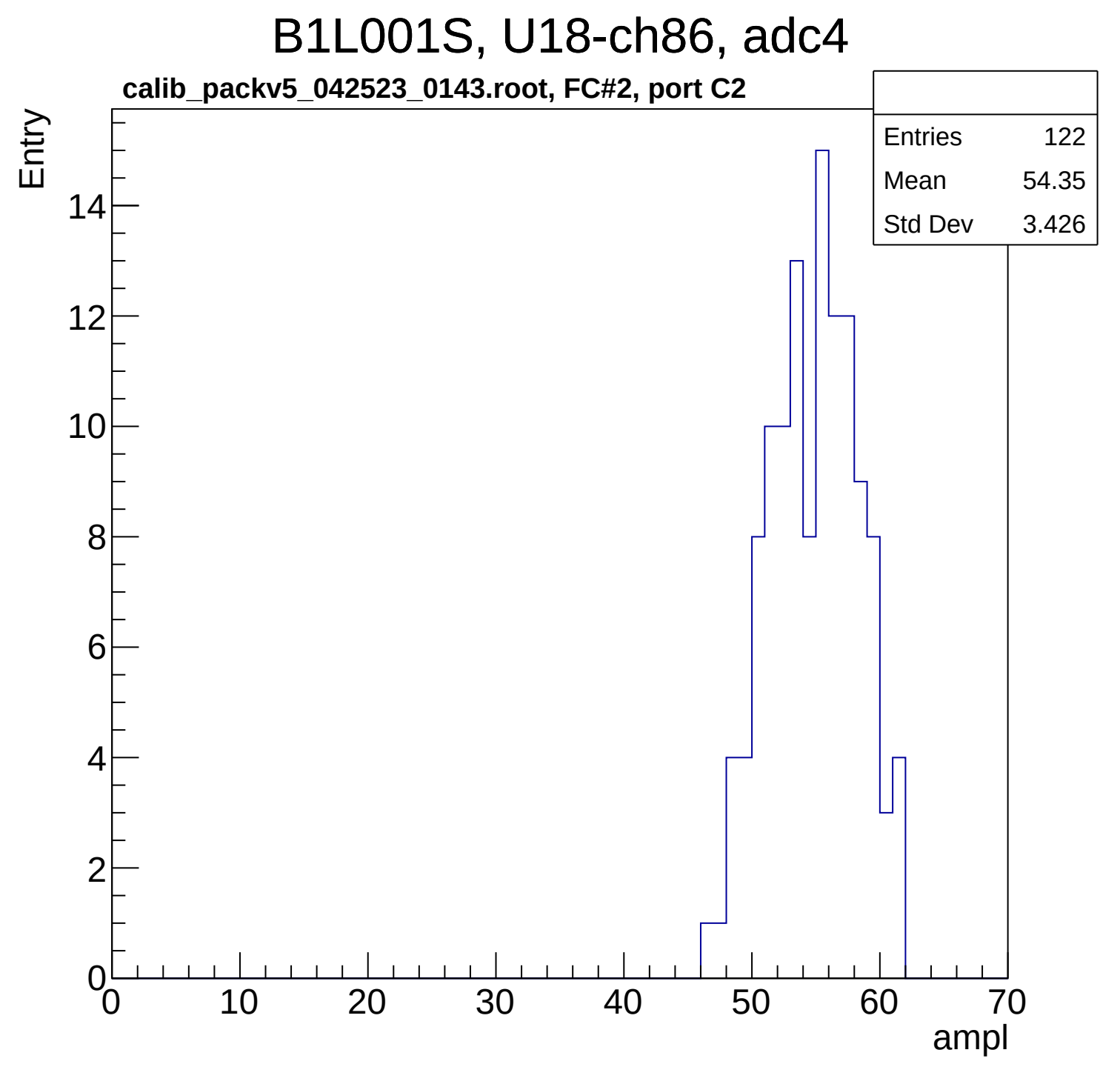

B1L001S, U18-ch85, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 31.5
Std Dev 31.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

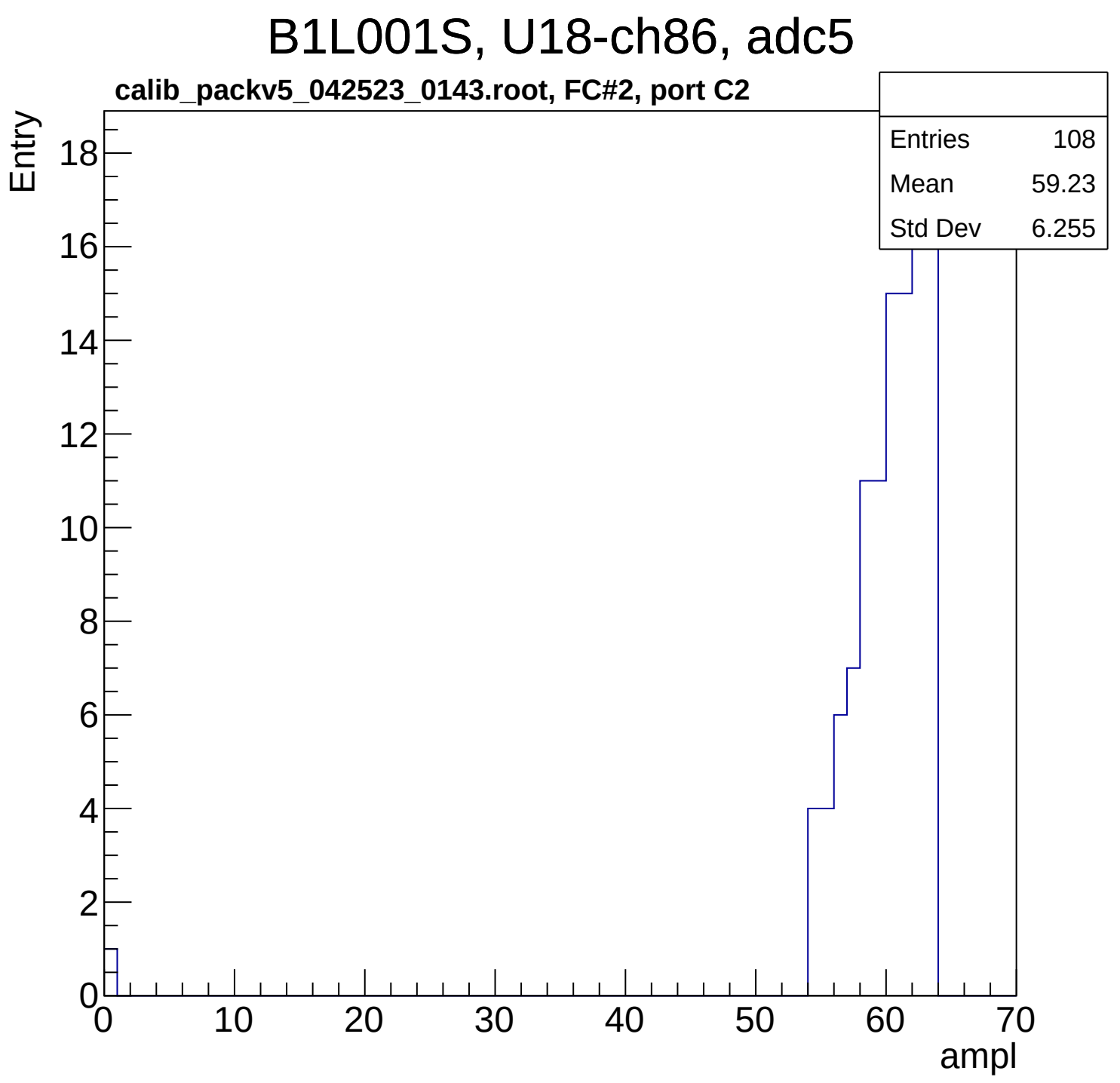

B1L001S, U18-ch86, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 117
Mean 28.76
Std Dev 5.045
Gaus mean : 29.3918
Gaus Width: 2.9421
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

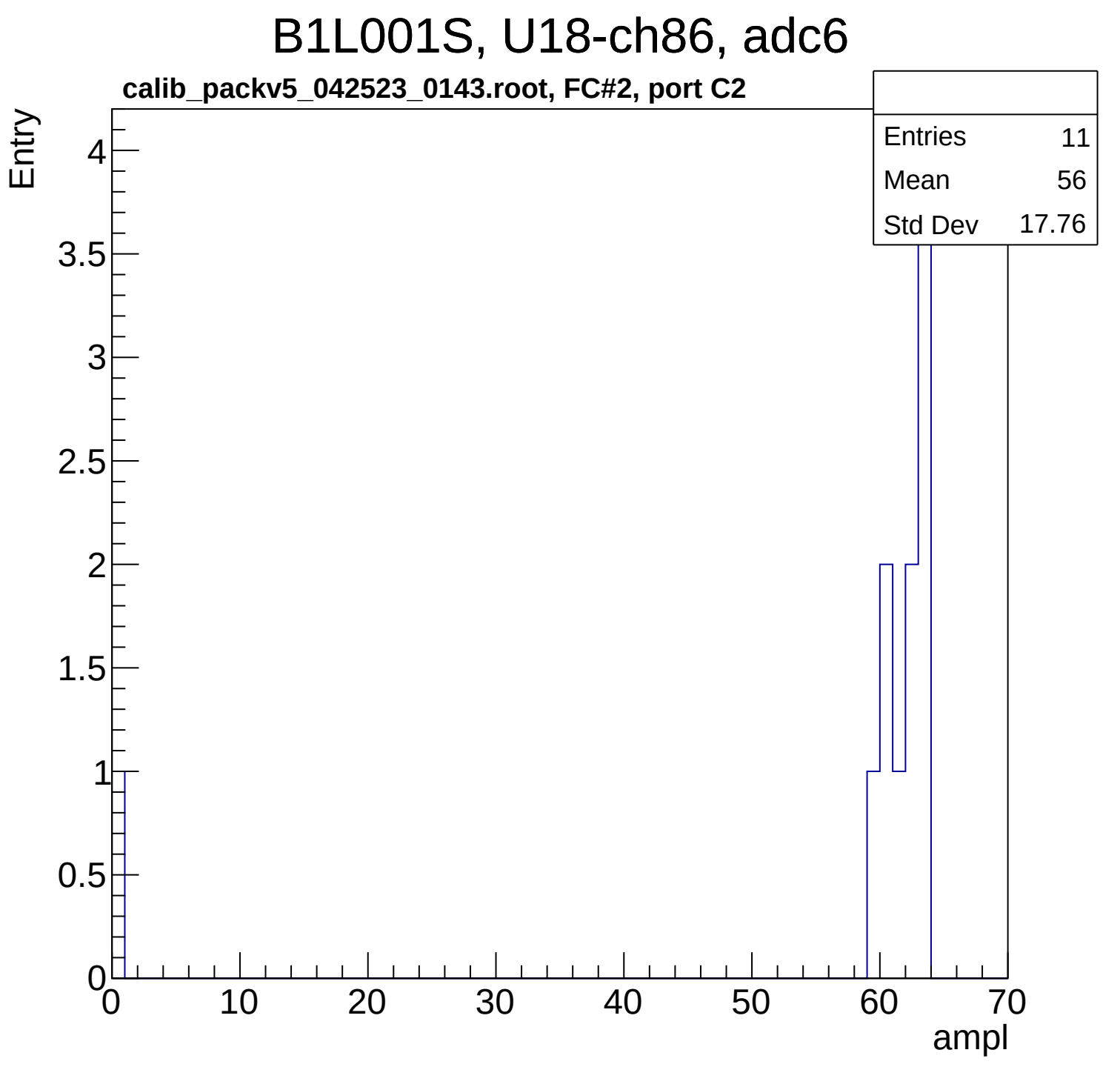

B1L001S, U18-ch86, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 163
Mean 36.16
Std Dev 3.947
Gaus mean : 36.5754
Gaus Width: 3.8570
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

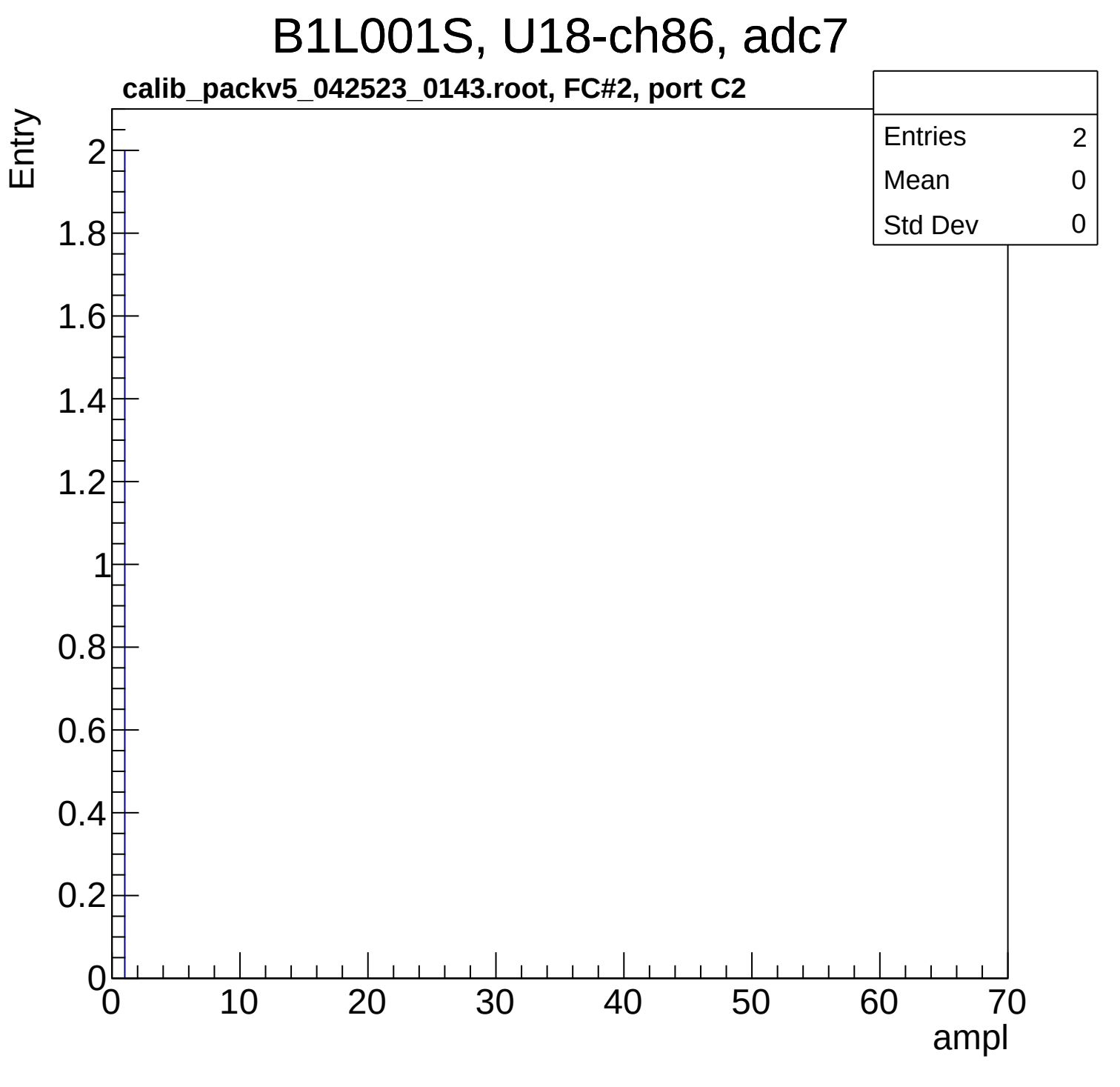

B1L001S, U18-ch86, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 117
Mean 43.14
Std Dev 3.359
Gaus mean : 43.3991
Gaus Width: 3.0900
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

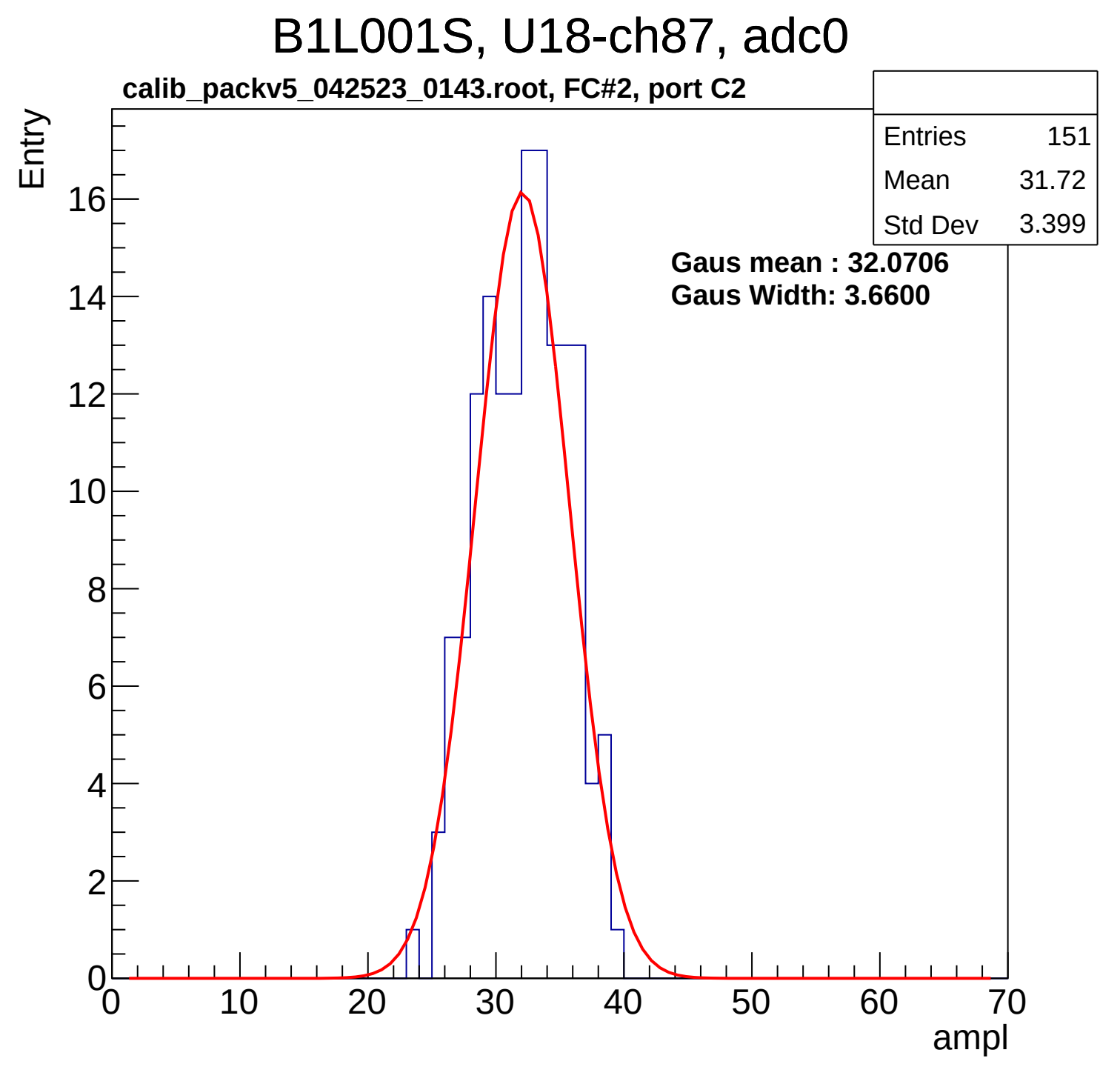

B1L001S, U18-ch86, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 110
Mean 48.88
Std Dev 3.528
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl

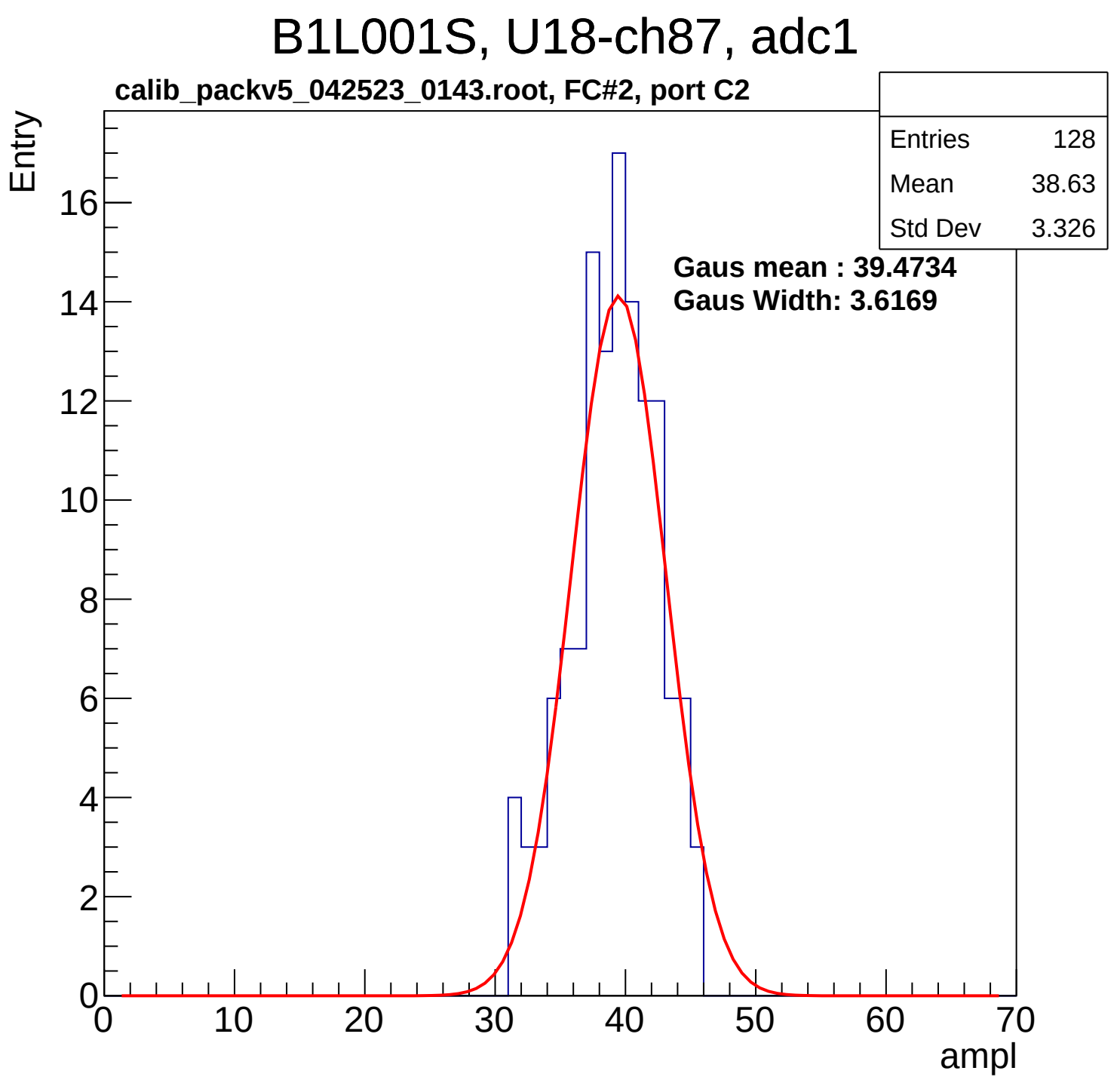

B1L001S, U18-ch86, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 122
Mean 54.35
Std Dev 3.426
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

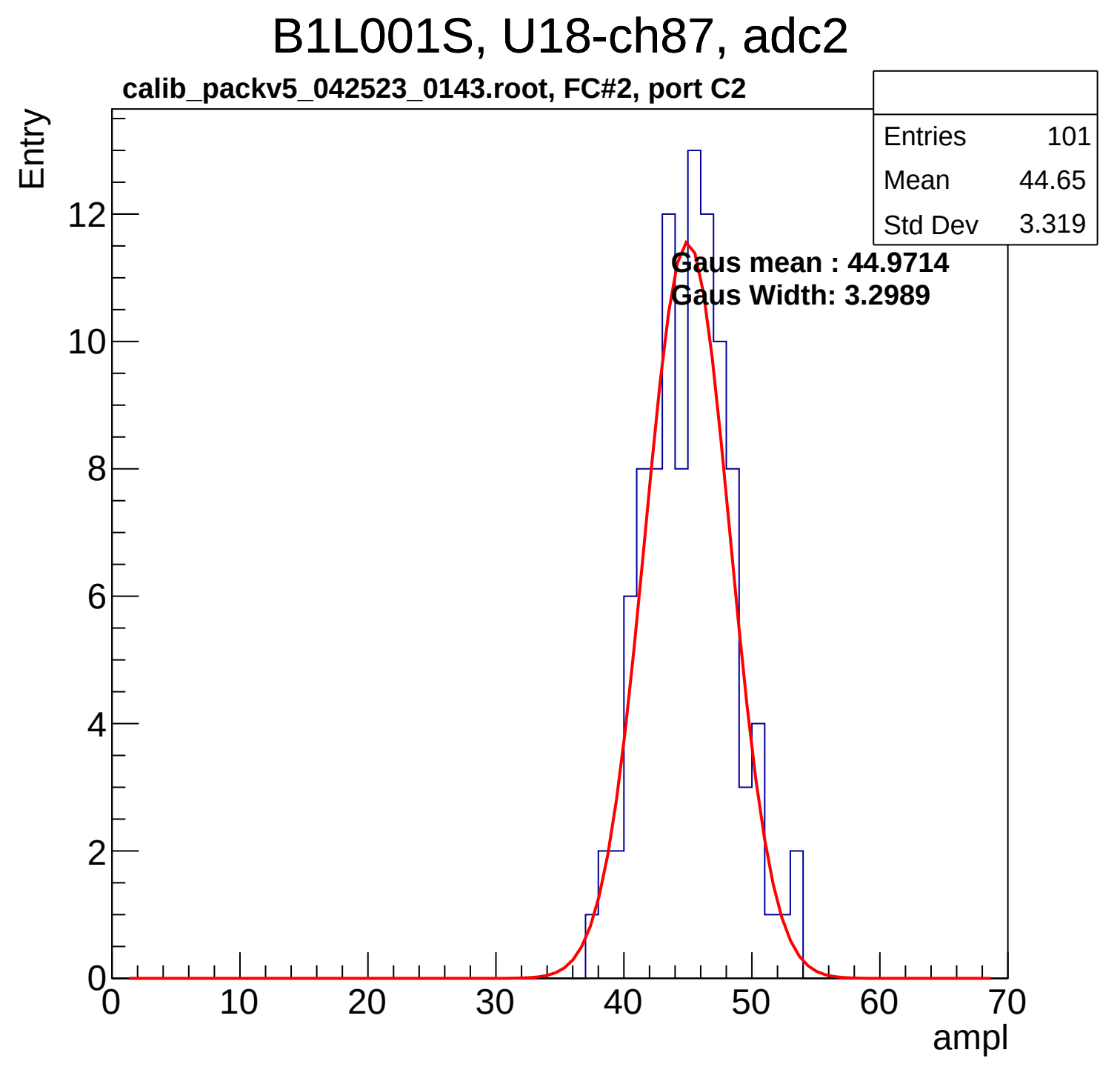

B1L001S, U18-ch86, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 108
Mean 59.23
Std Dev 6.255
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

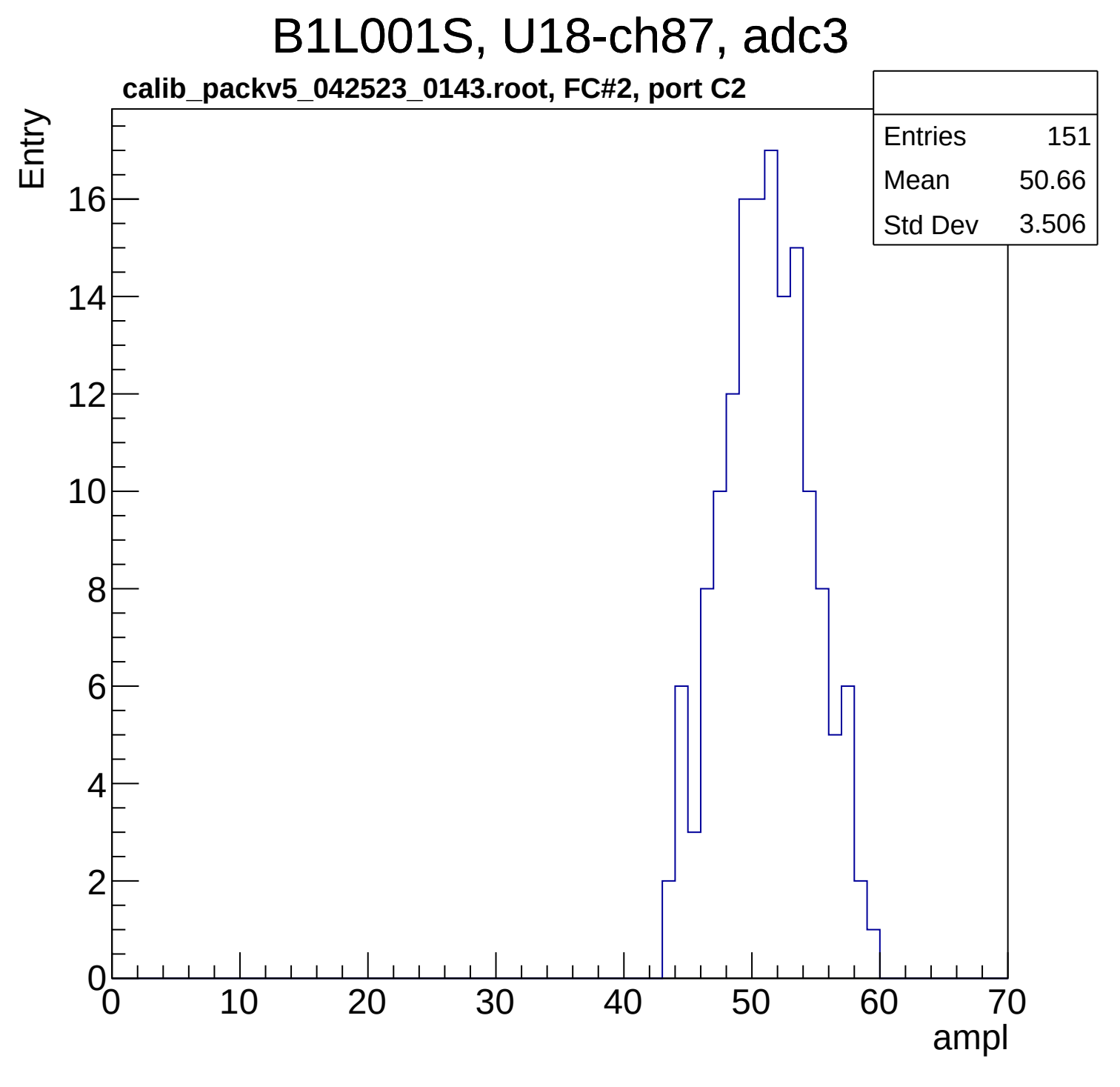

B1L001S, U18-ch86, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 11
Mean 56
Std Dev 17.76
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

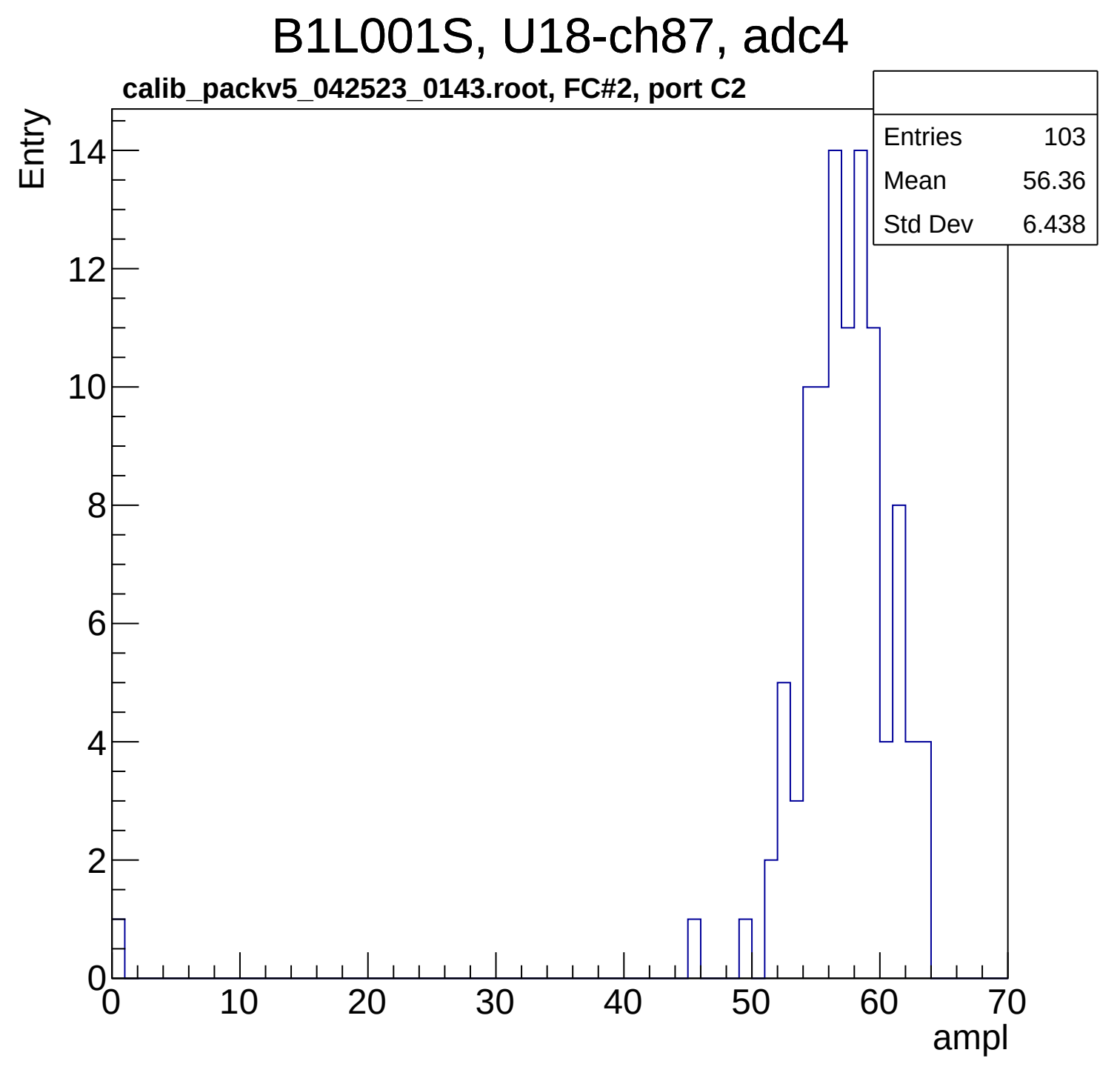

B1L001S, U18-ch86, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 0
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

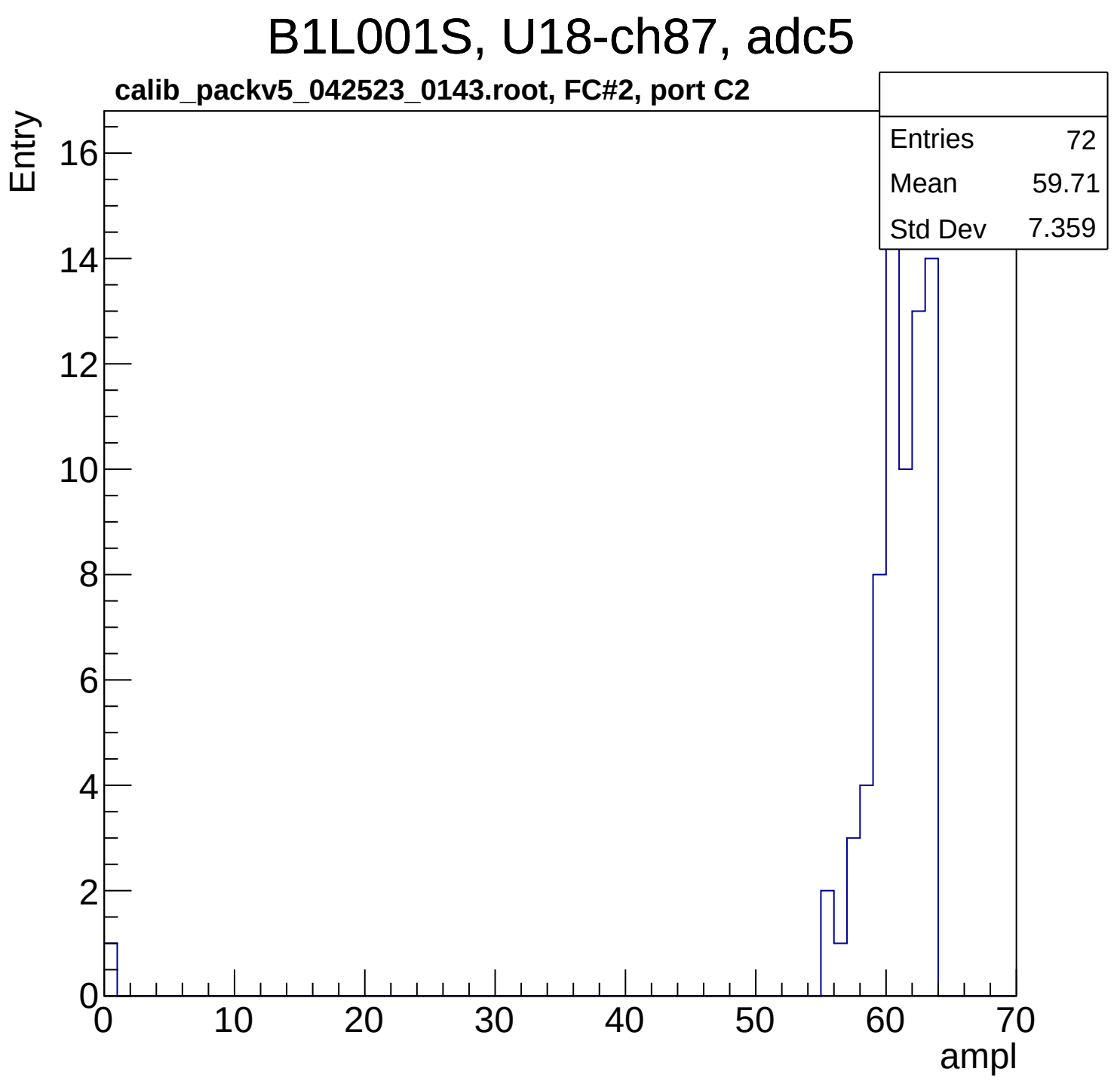

B1L001S, U18-ch87, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 151
Mean 31.72
Std Dev 3.399
Gaus mean : 32.0706
Gaus Width: 3.6600
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

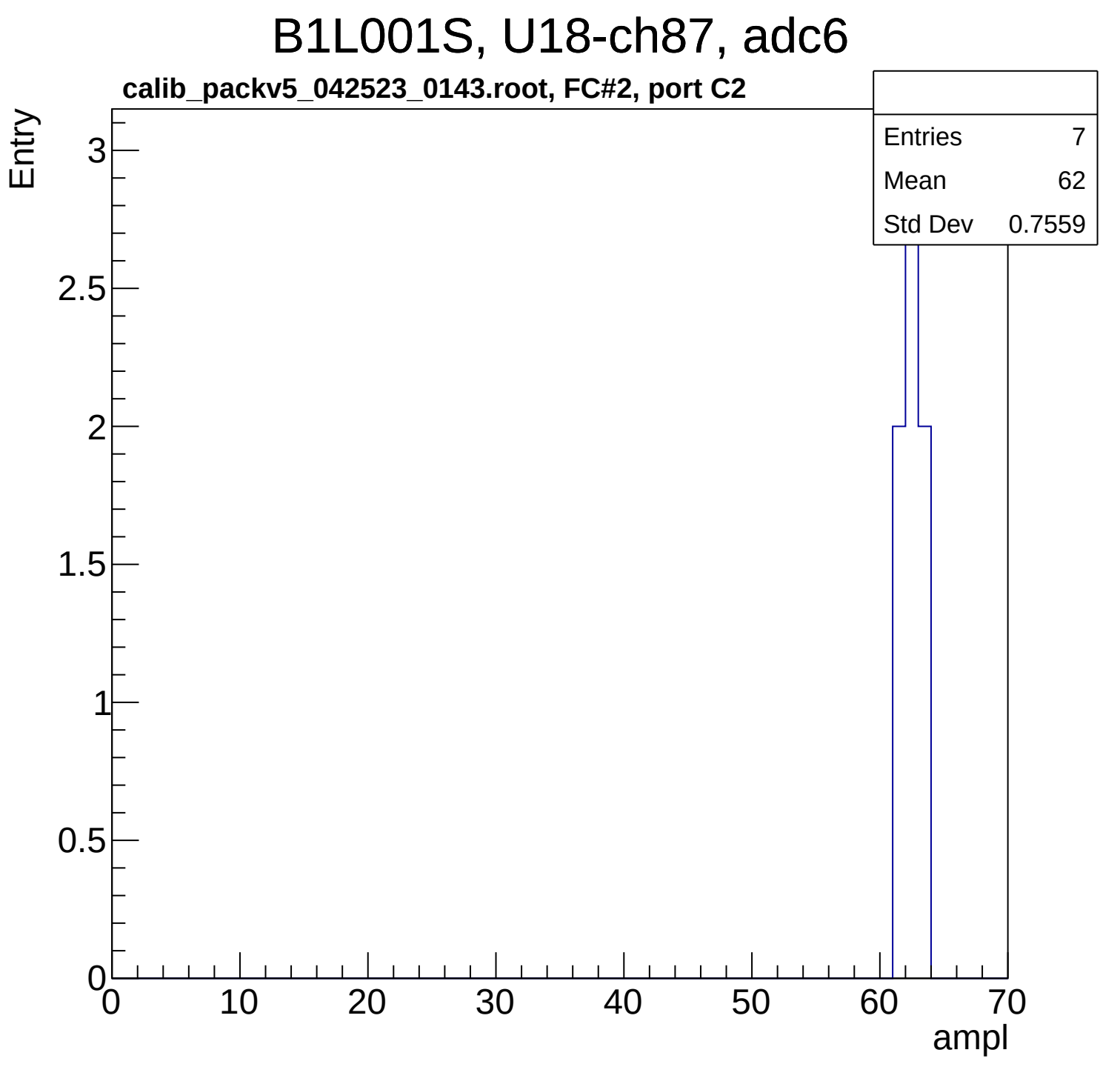

B1L001S, U18-ch87, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 128
Mean 38.63
Std Dev 3.326
Gaus mean : 39.4734
Gaus Width: 3.6169
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

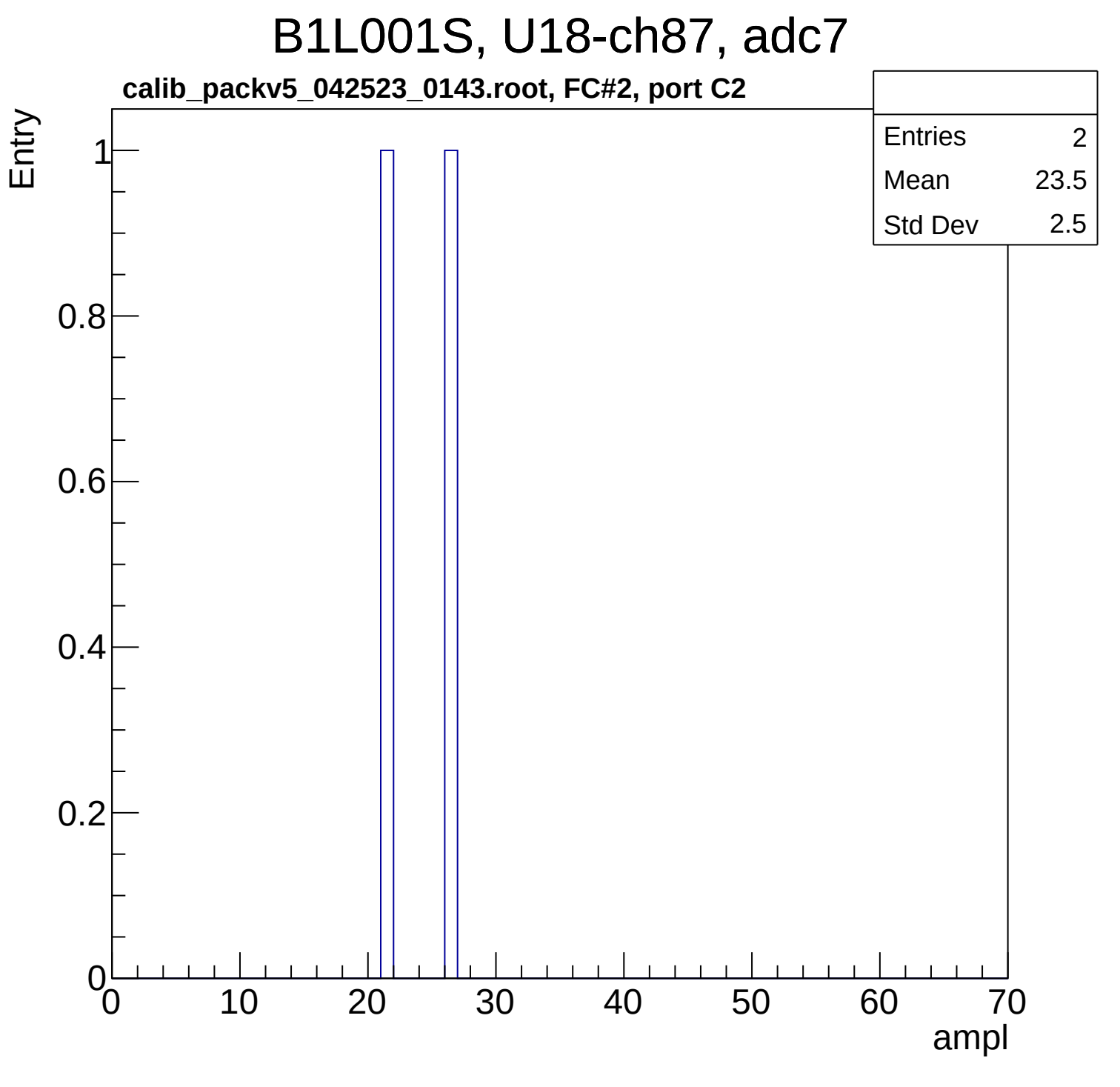

B1L001S, U18-ch87, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 101
Mean 44.65
Std Dev 3.319
Gaus mean : 44.9714
Gaus Width: 3.2989
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70

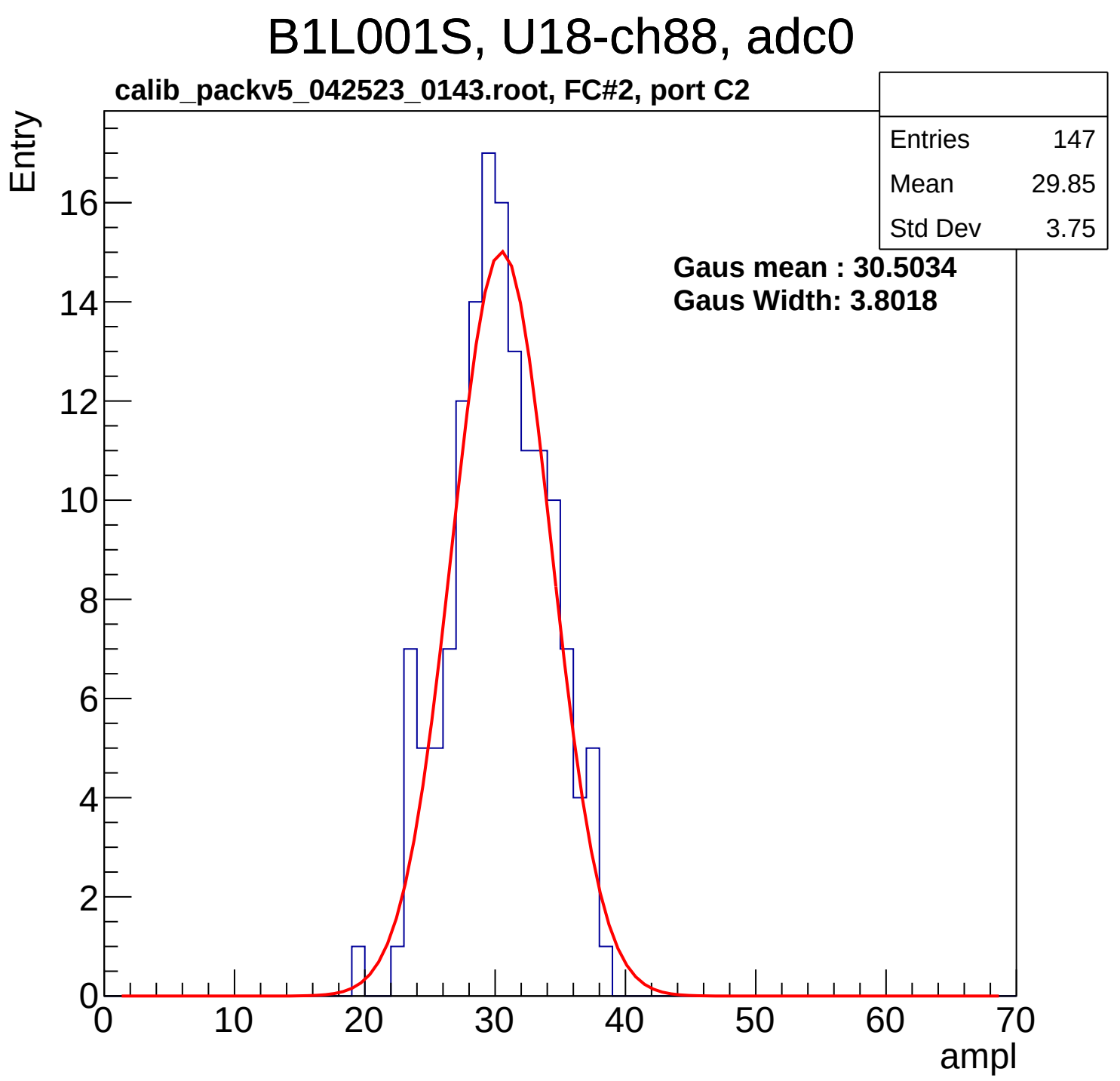

B1L001S, U18-ch87, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 151
Mean 50.66
Std Dev 3.506
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

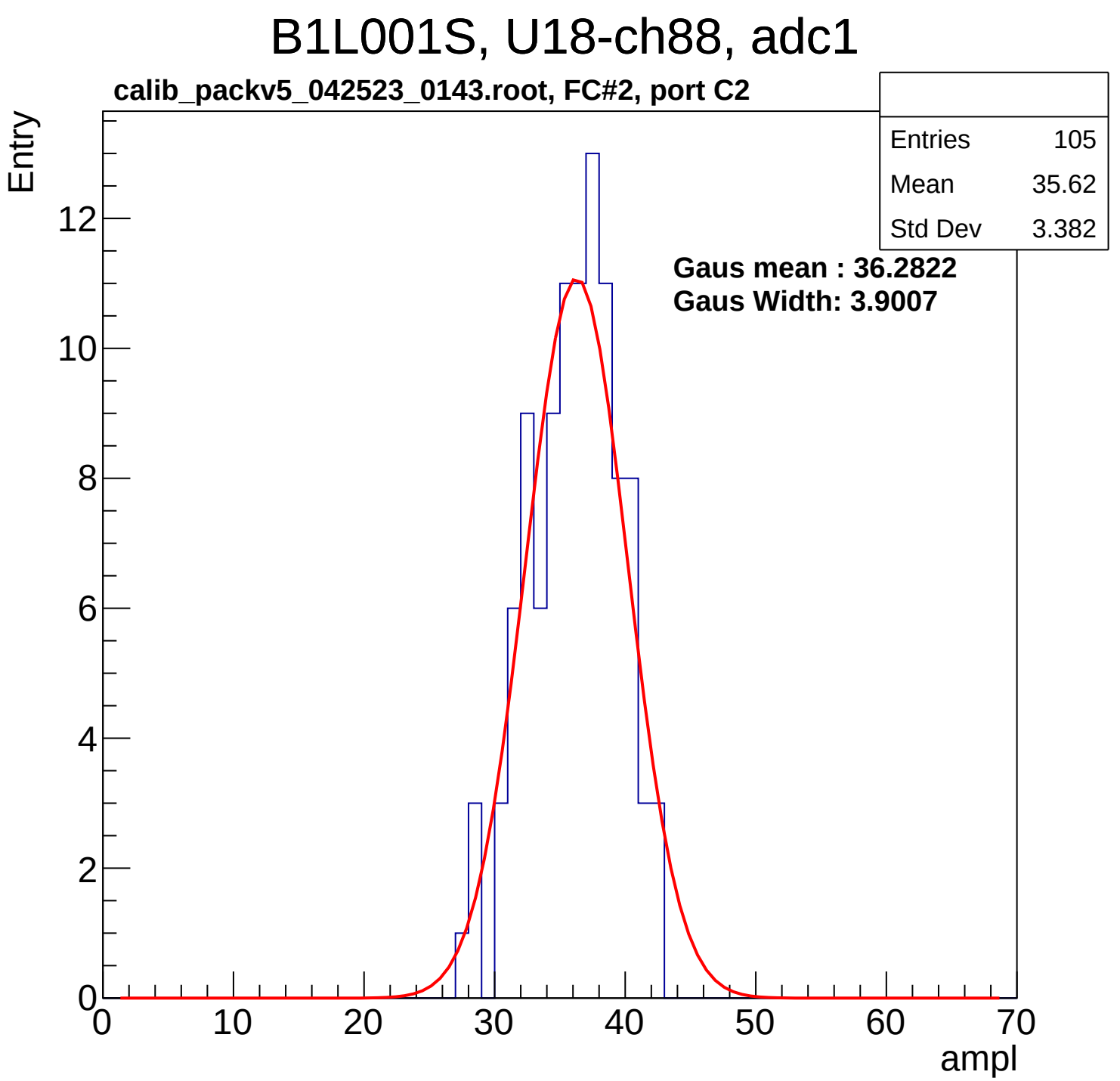

B1L001S, U18-ch87, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 103
Mean 56.36
Std Dev 6.438
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

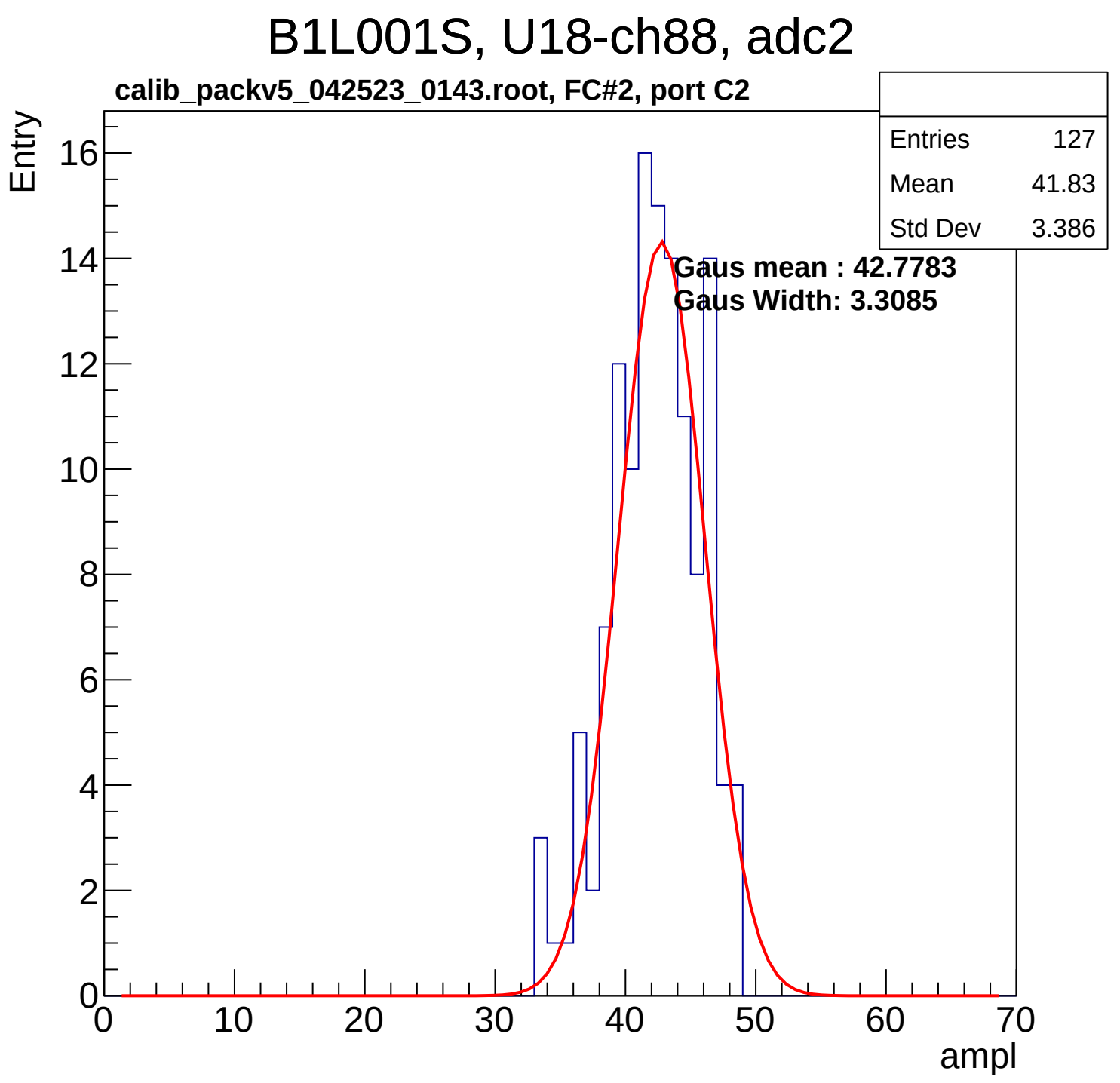

B1L001S, U18-ch87, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 72
Mean 59.71
Std Dev 7.359
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

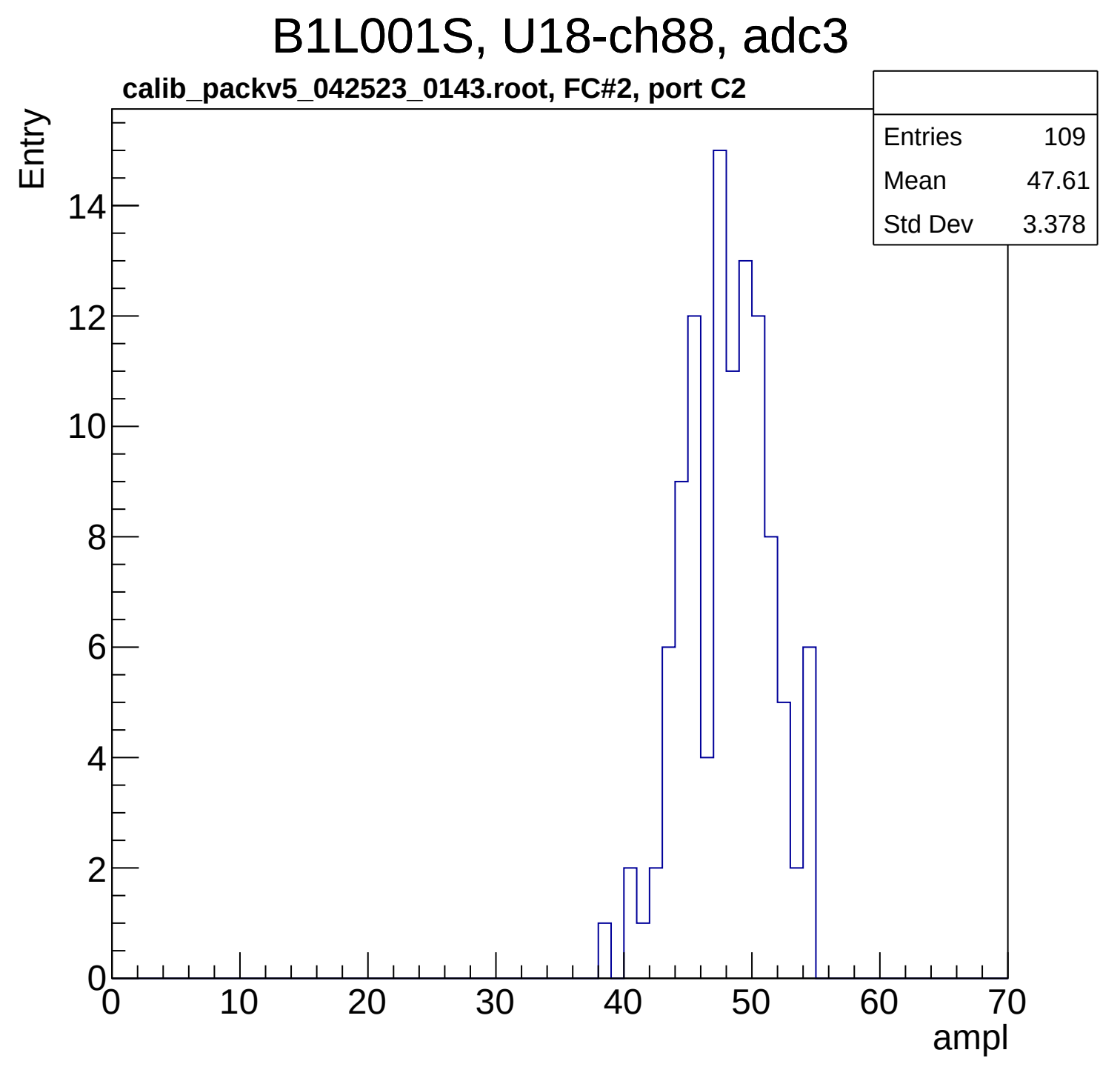

B1L001S, U18-ch87, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 7
Mean 62
Std Dev 0.7559
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

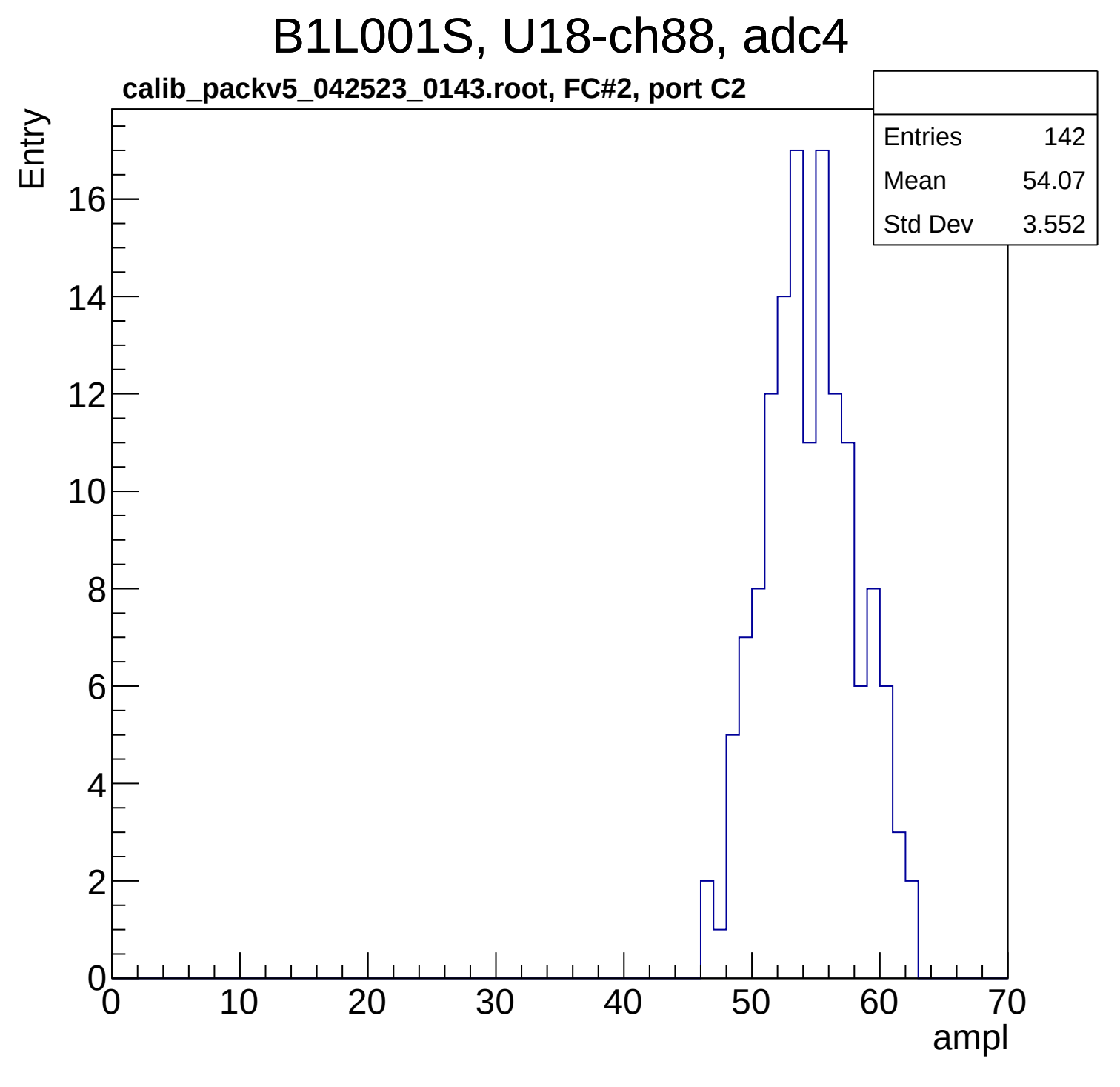

B1L001S, U18-ch87, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 23.5
Std Dev 2.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

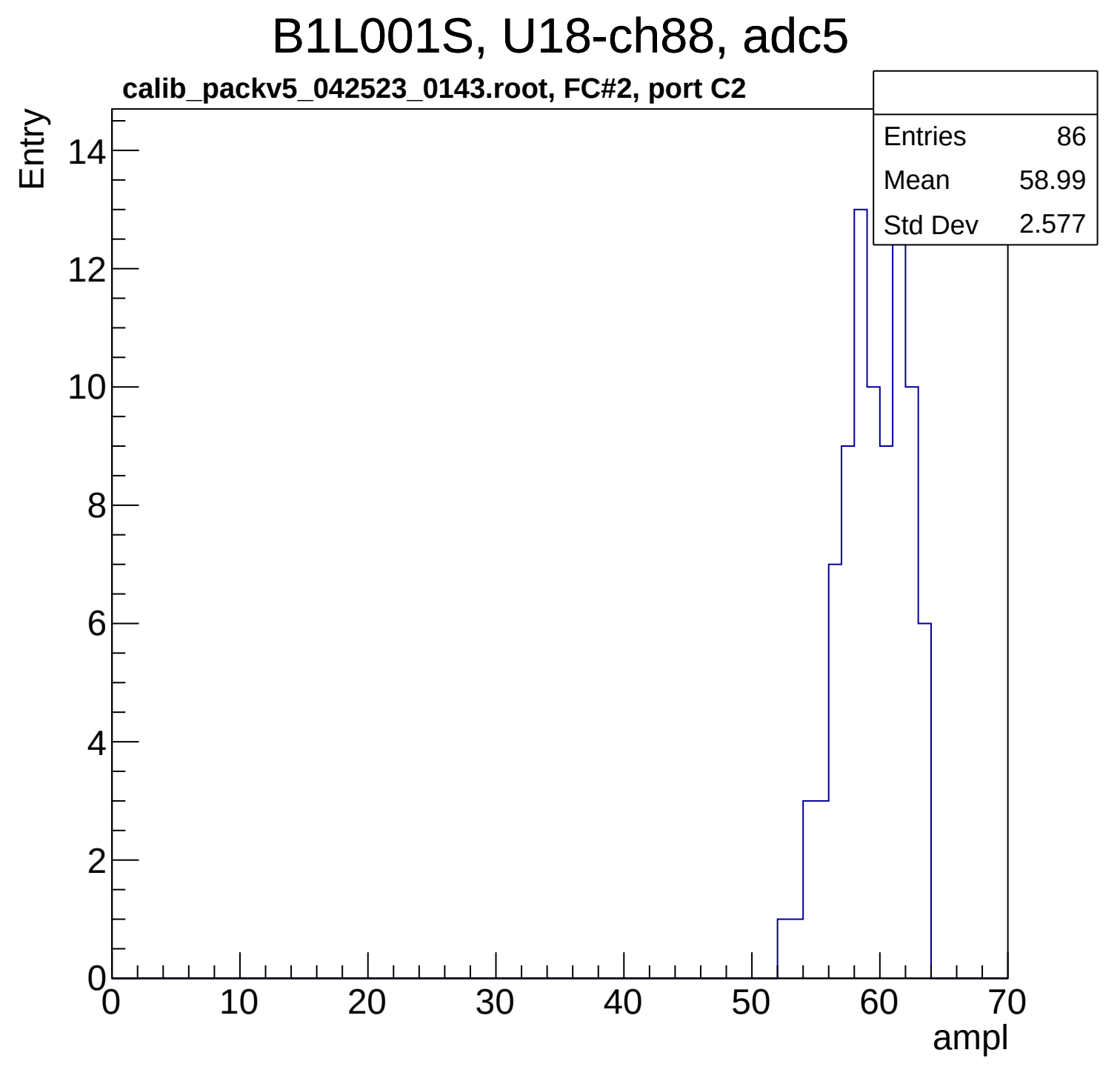

B1L001S, U18-ch88, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 147
Mean 29.85
Std Dev 3.75
Gaus mean : 30.5034
Gaus Width: 3.8018
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

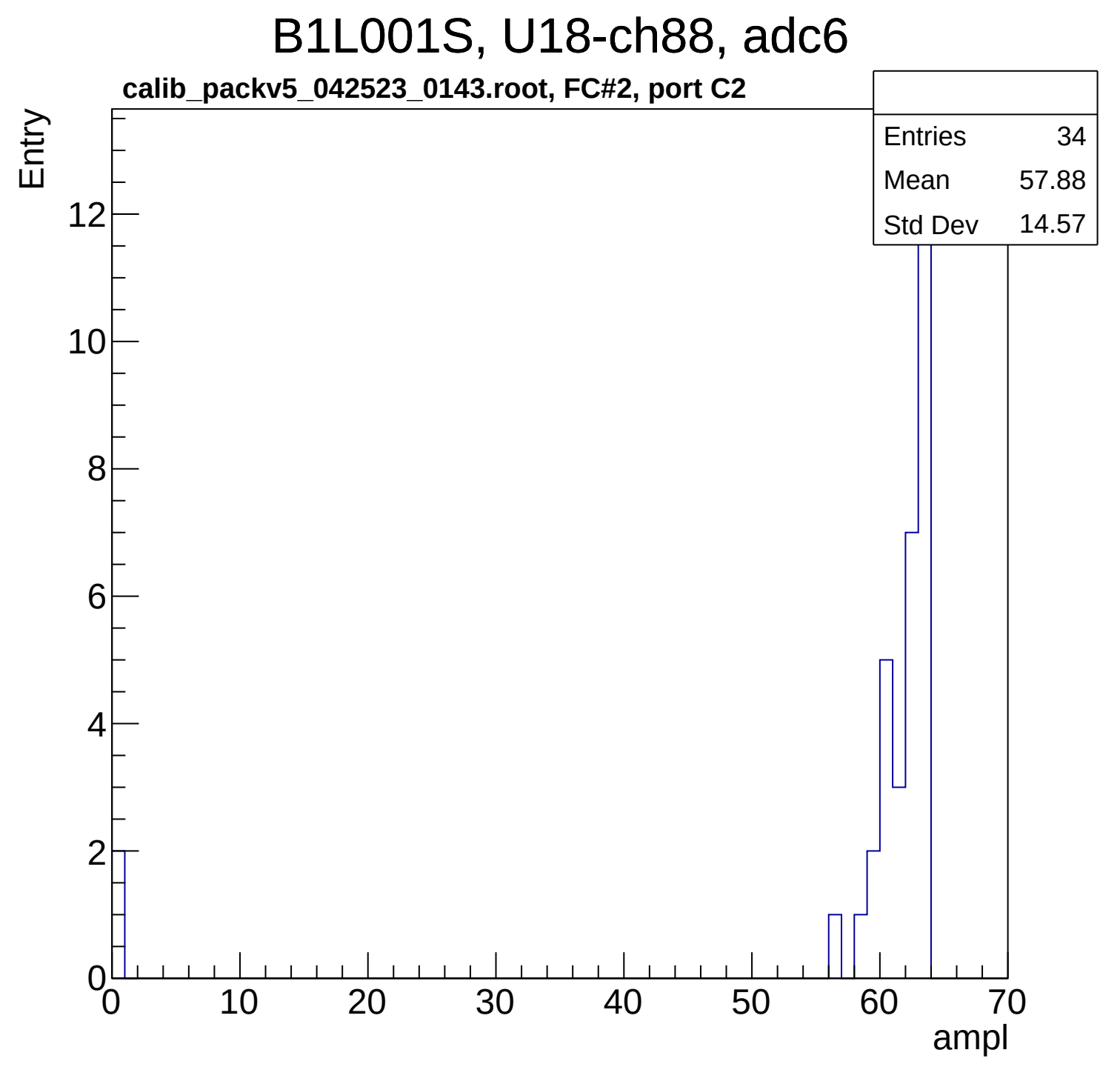

B1L001S, U18-ch88, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 105
Mean 35.62
Std Dev 3.382
Gaus mean : 36.2822
Gaus Width: 3.9007
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70

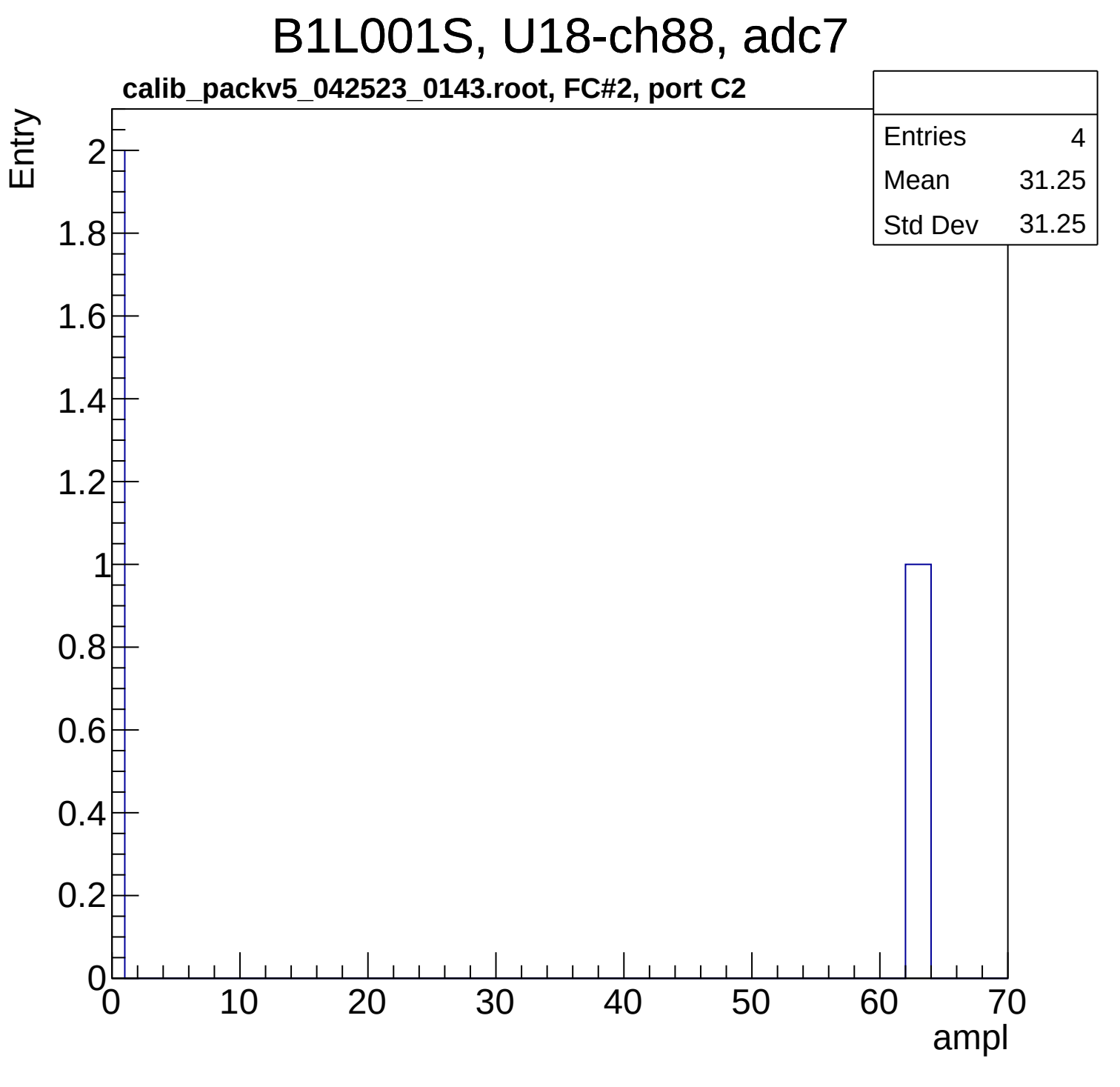

B1L001S, U18-ch88, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 127
Mean 41.83
Std Dev 3.386
Gaus mean : 42.7783
Gaus Width: 3.3085
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

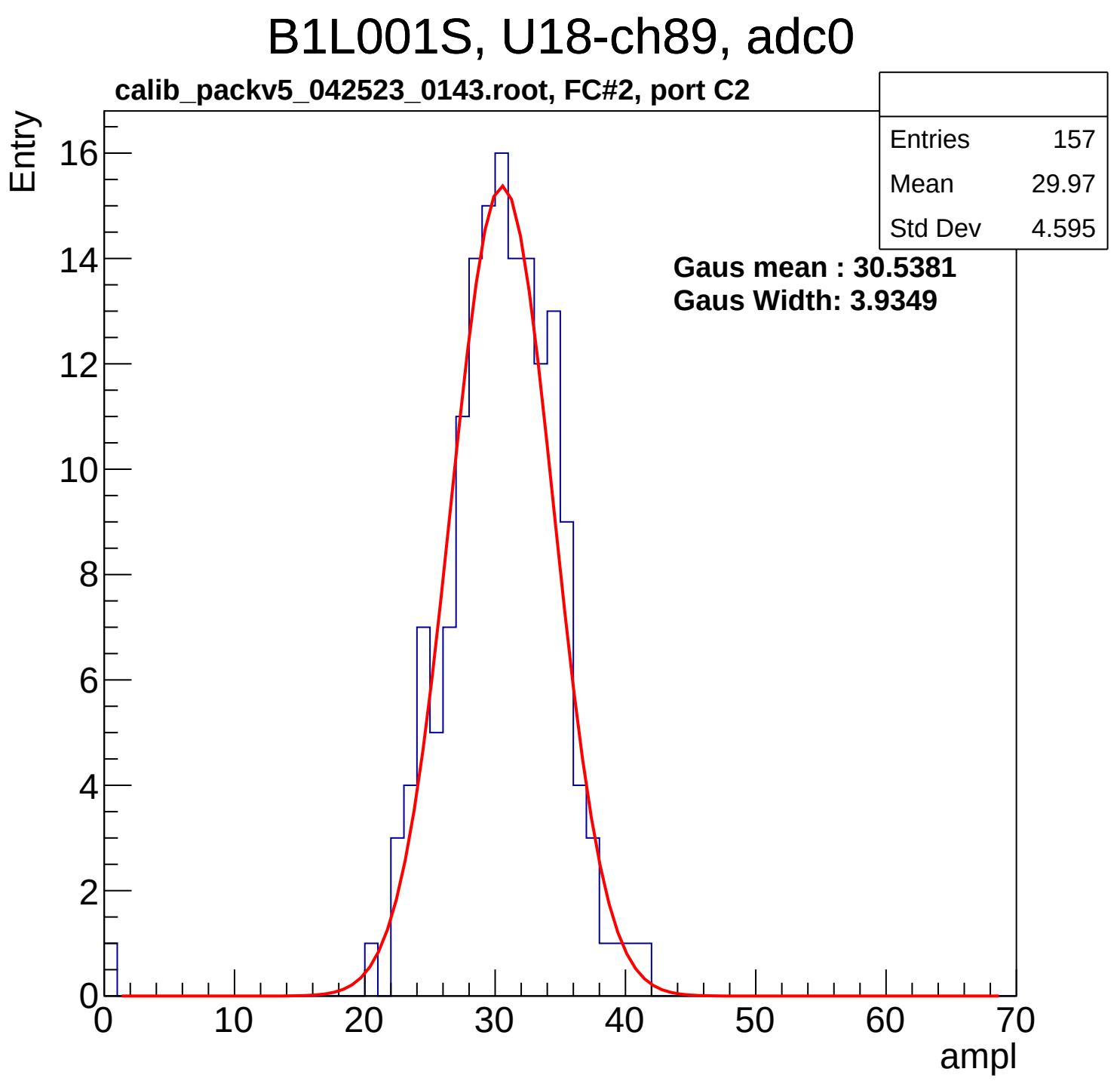

B1L001S, U18-ch88, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 109
Mean 47.61
Std Dev 3.378
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

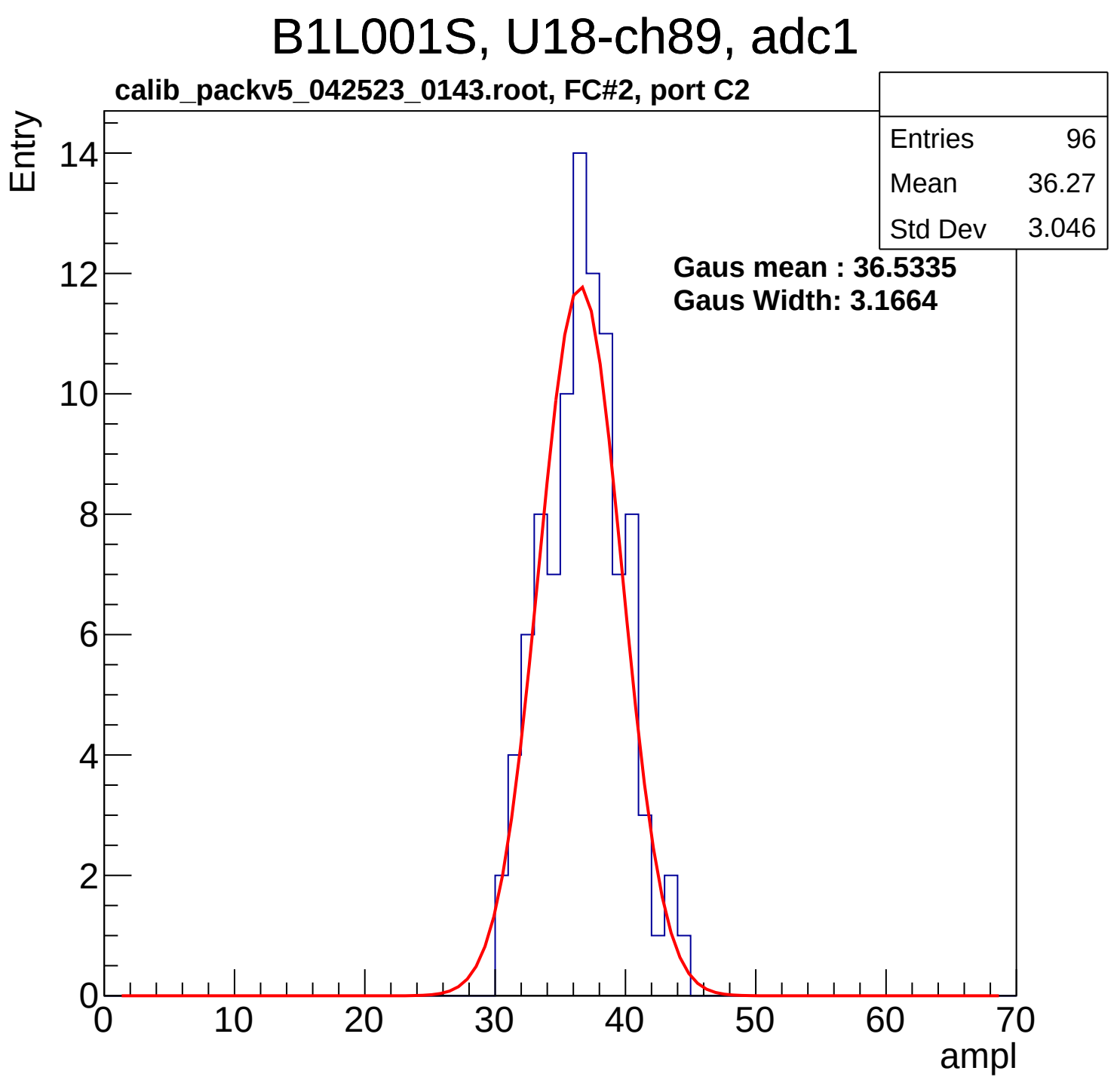

B1L001S, U18-ch88, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 142
Mean 54.07
Std Dev 3.552
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

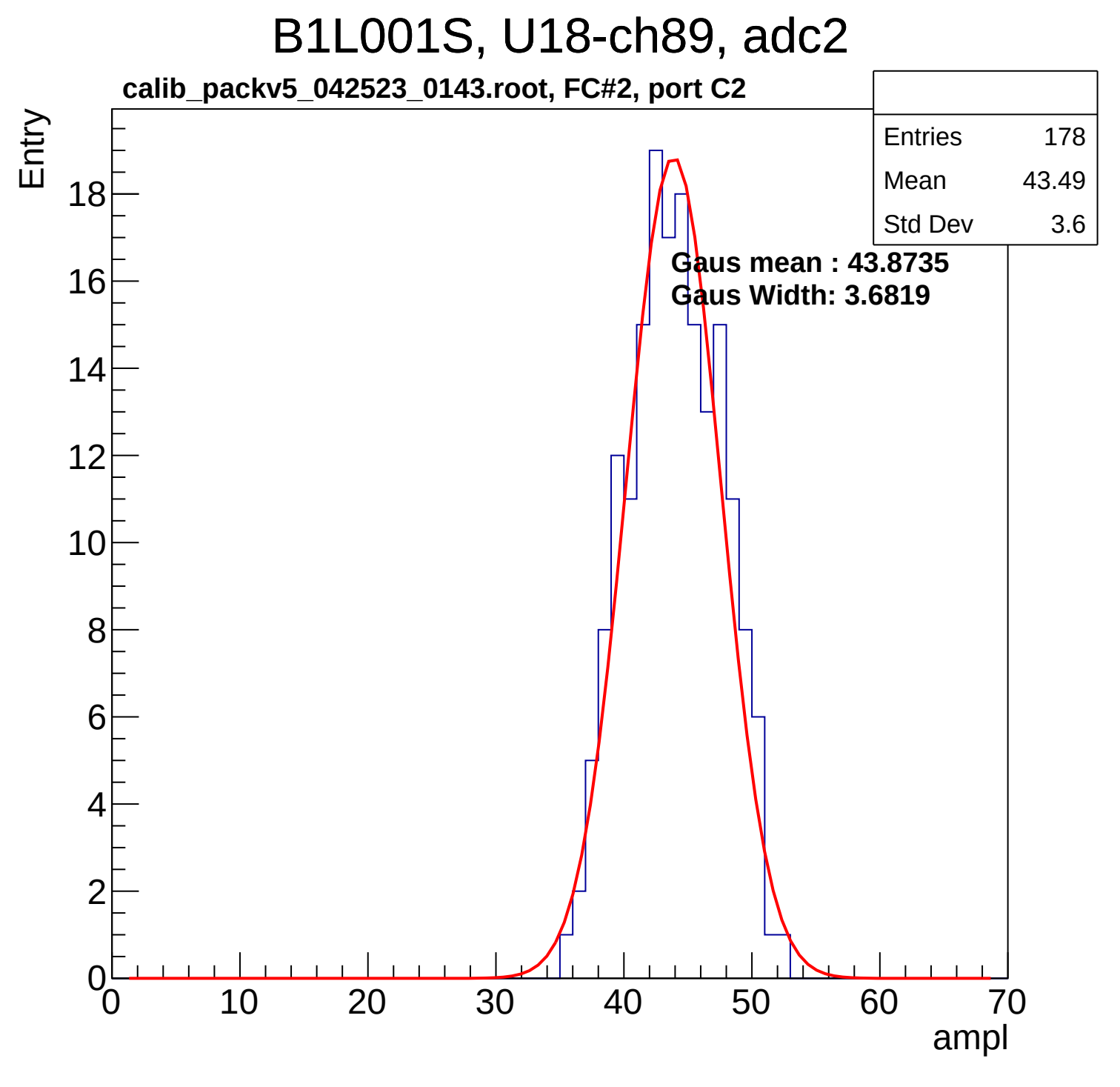

B1L001S, U18-ch88, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 86
Mean 58.99
Std Dev 2.577
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

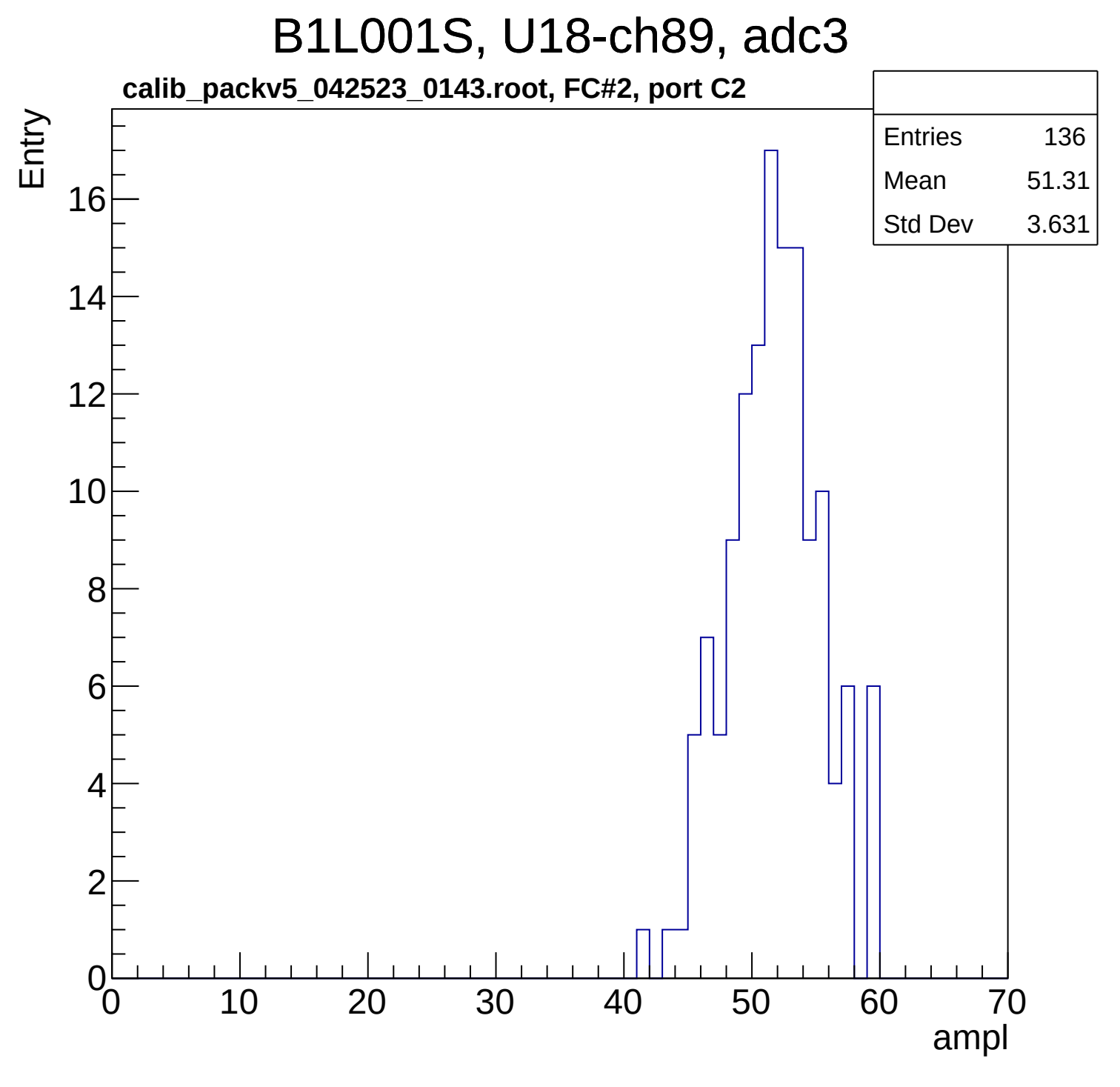

B1L001S, U18-ch88, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 34
Mean 57.88
Std Dev 14.57
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl

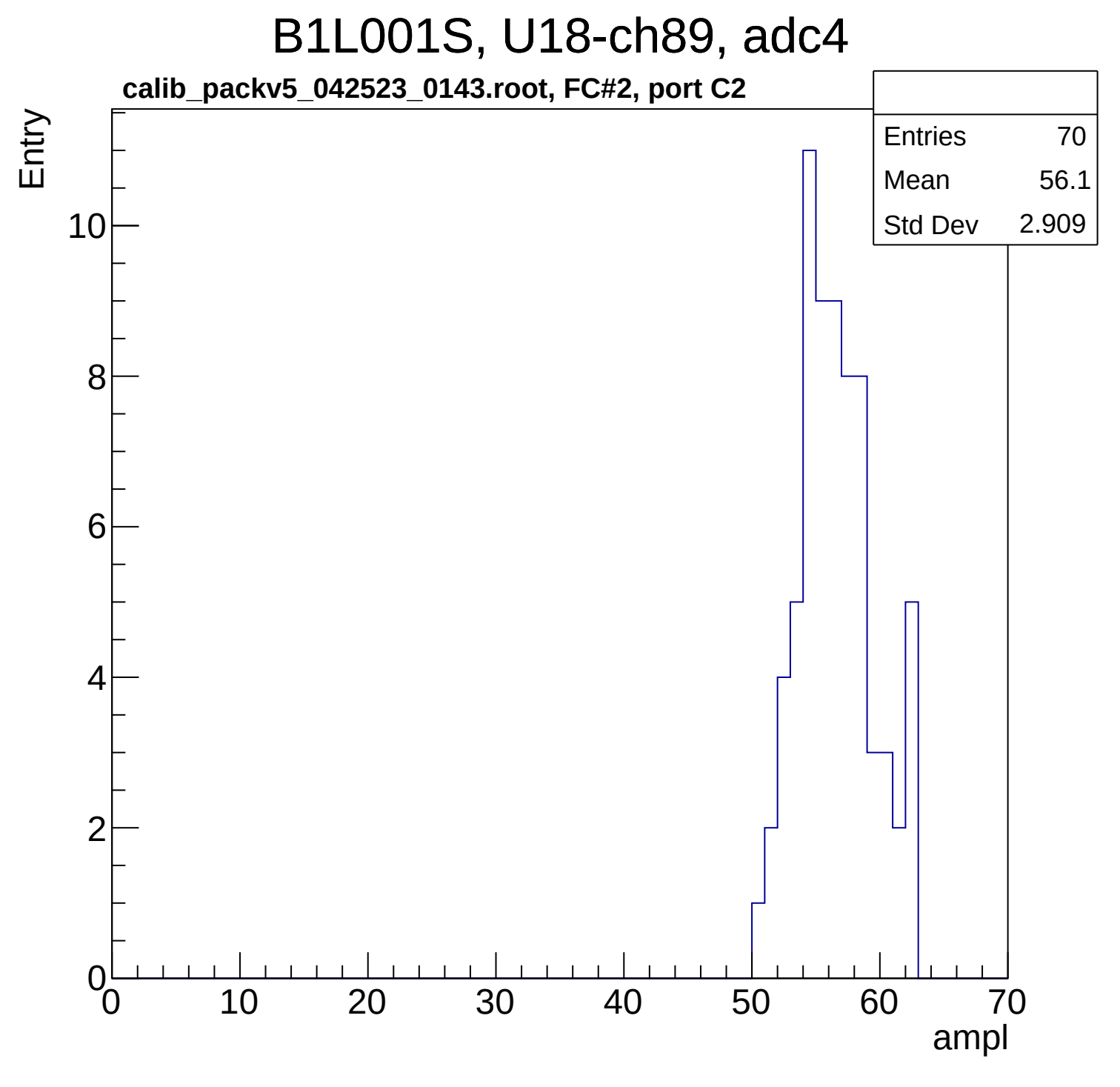

B1L001S, U18-ch88, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 4
Mean 31.25
Std Dev 31.25
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

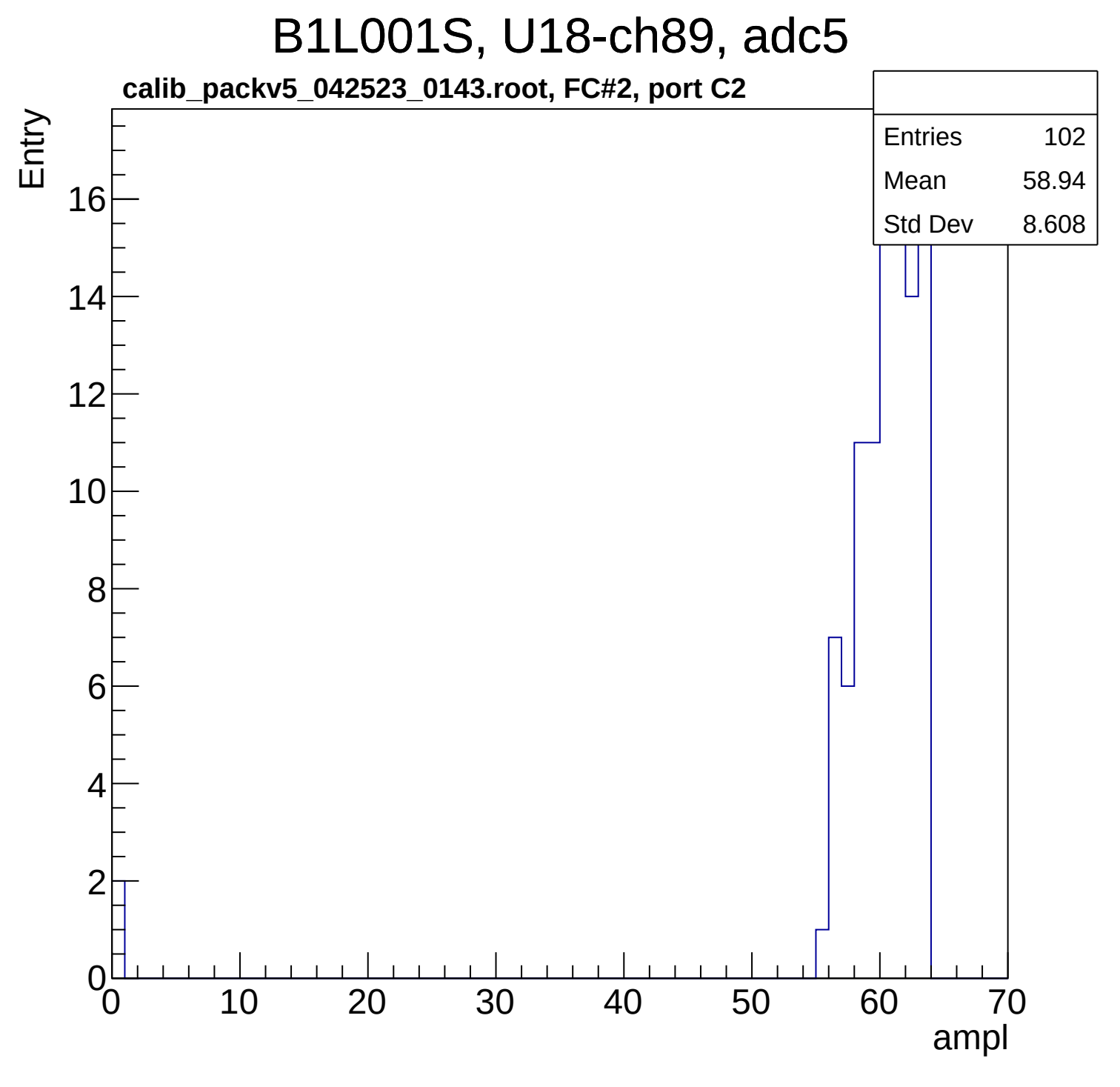

B1L001S, U18-ch89, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 157
Mean 29.97
Std Dev 4.595
Gaus mean : 30.5381
Gaus Width: 3.9349
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

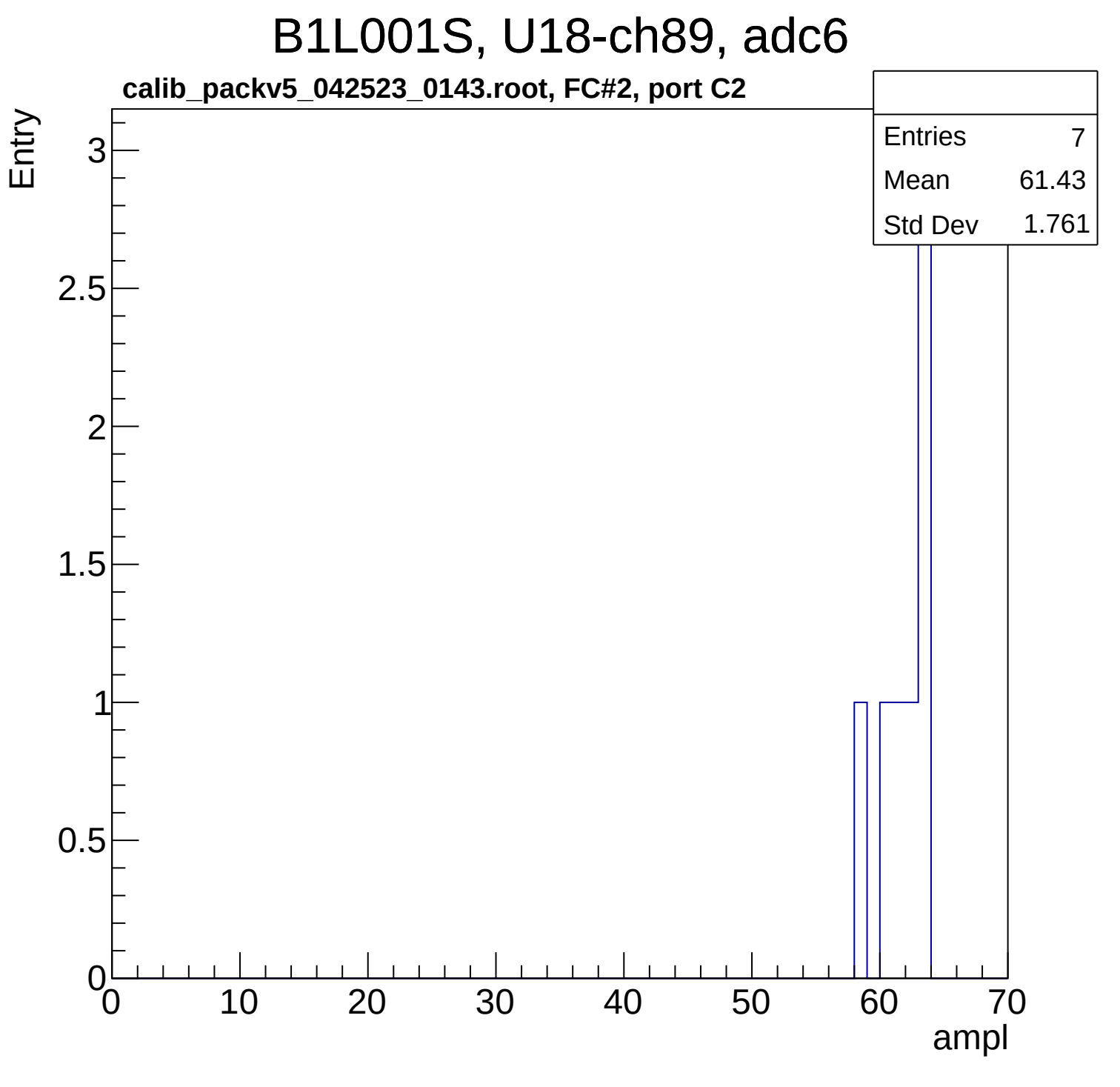

B1L001S, U18-ch89, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 96
Mean 36.27
Std Dev 3.046
Gaus mean : 36.5335
Gaus Width: 3.1664
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

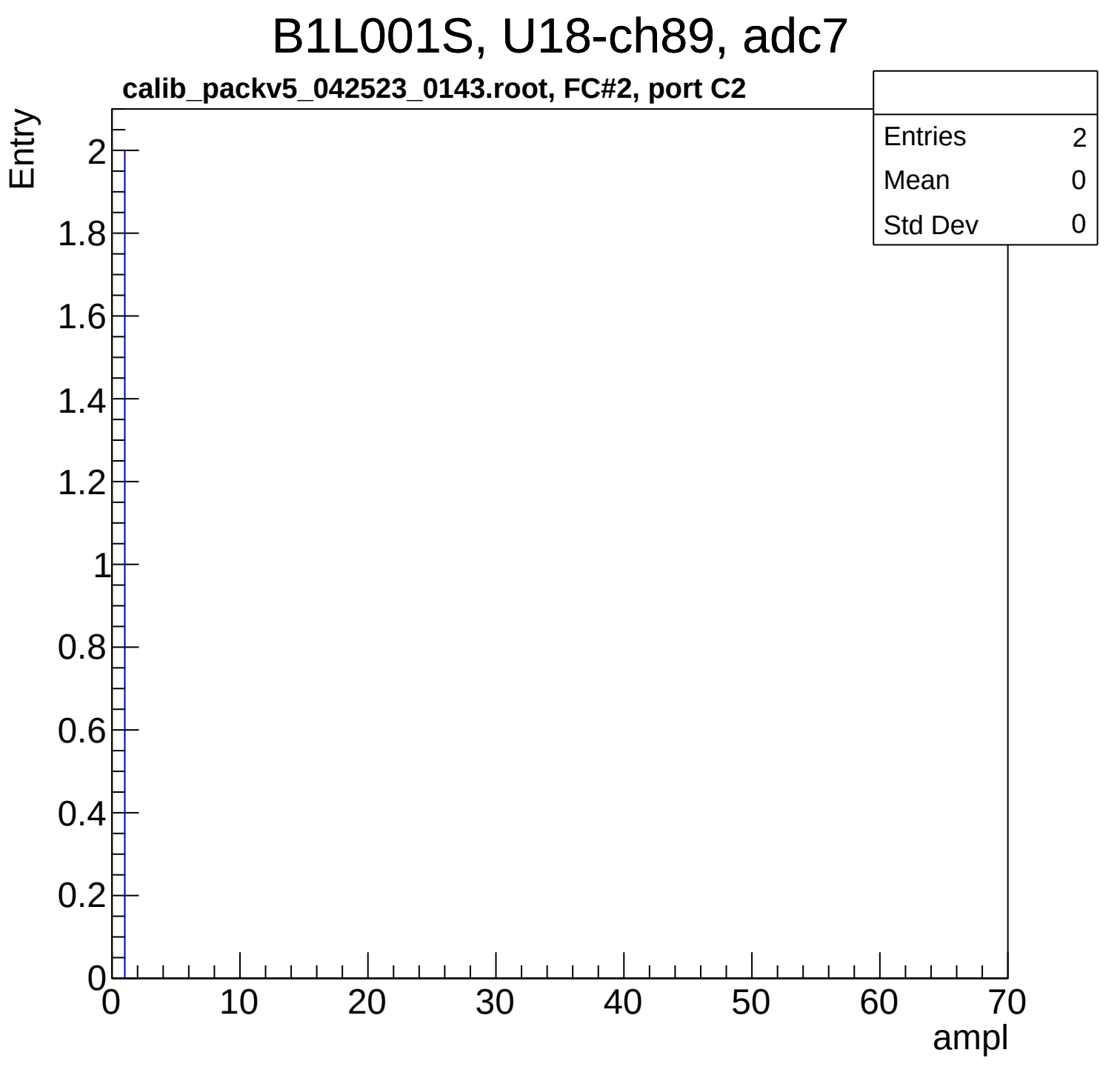

B1L001S, U18-ch89, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 178
Mean 43.49
Std Dev 3.6
Gaus mean : 43.8735
Gaus Width: 3.6819
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

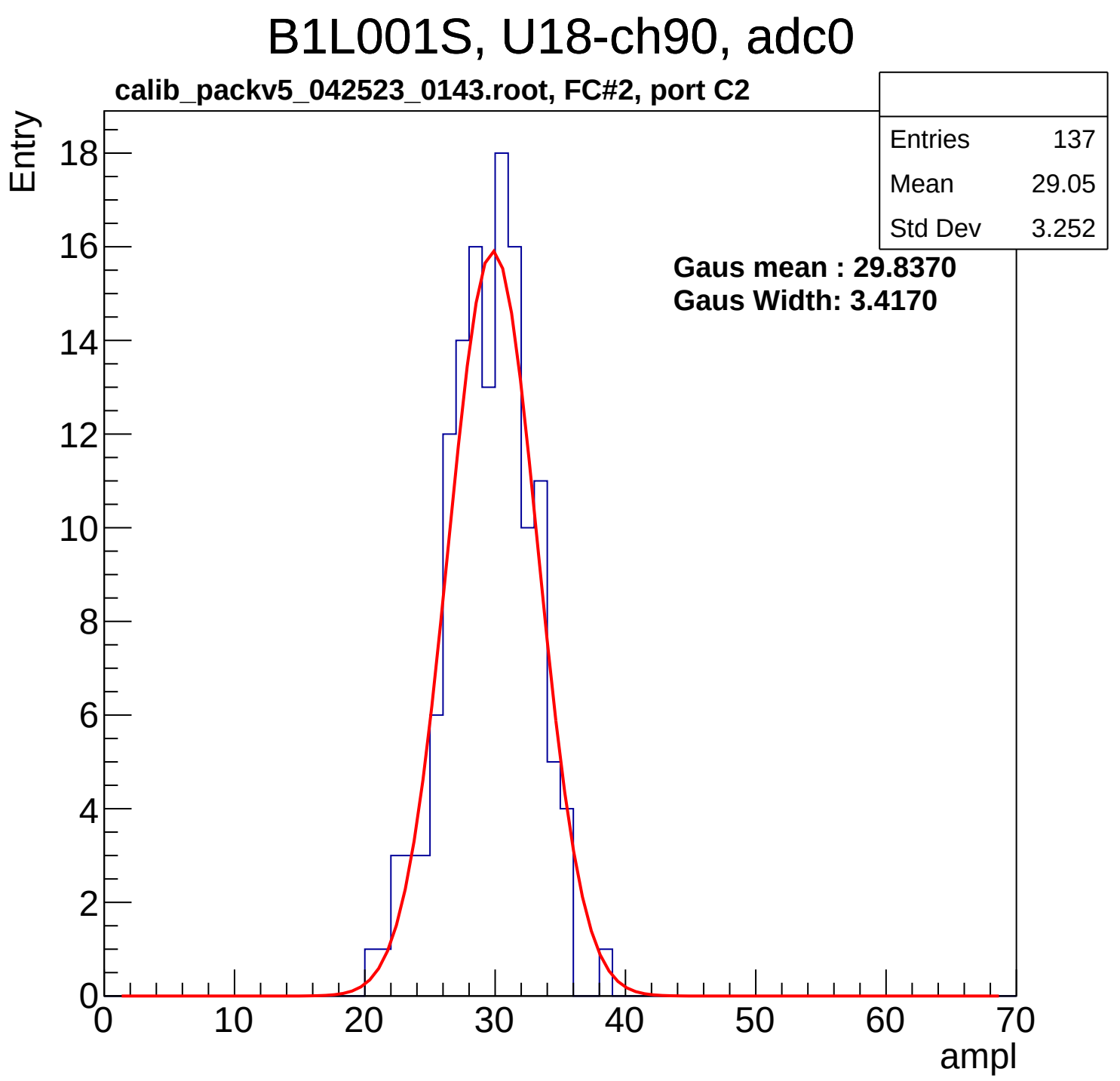

B1L001S, U18-ch89, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 136
Mean 51.31
Std Dev 3.631
Entry
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl

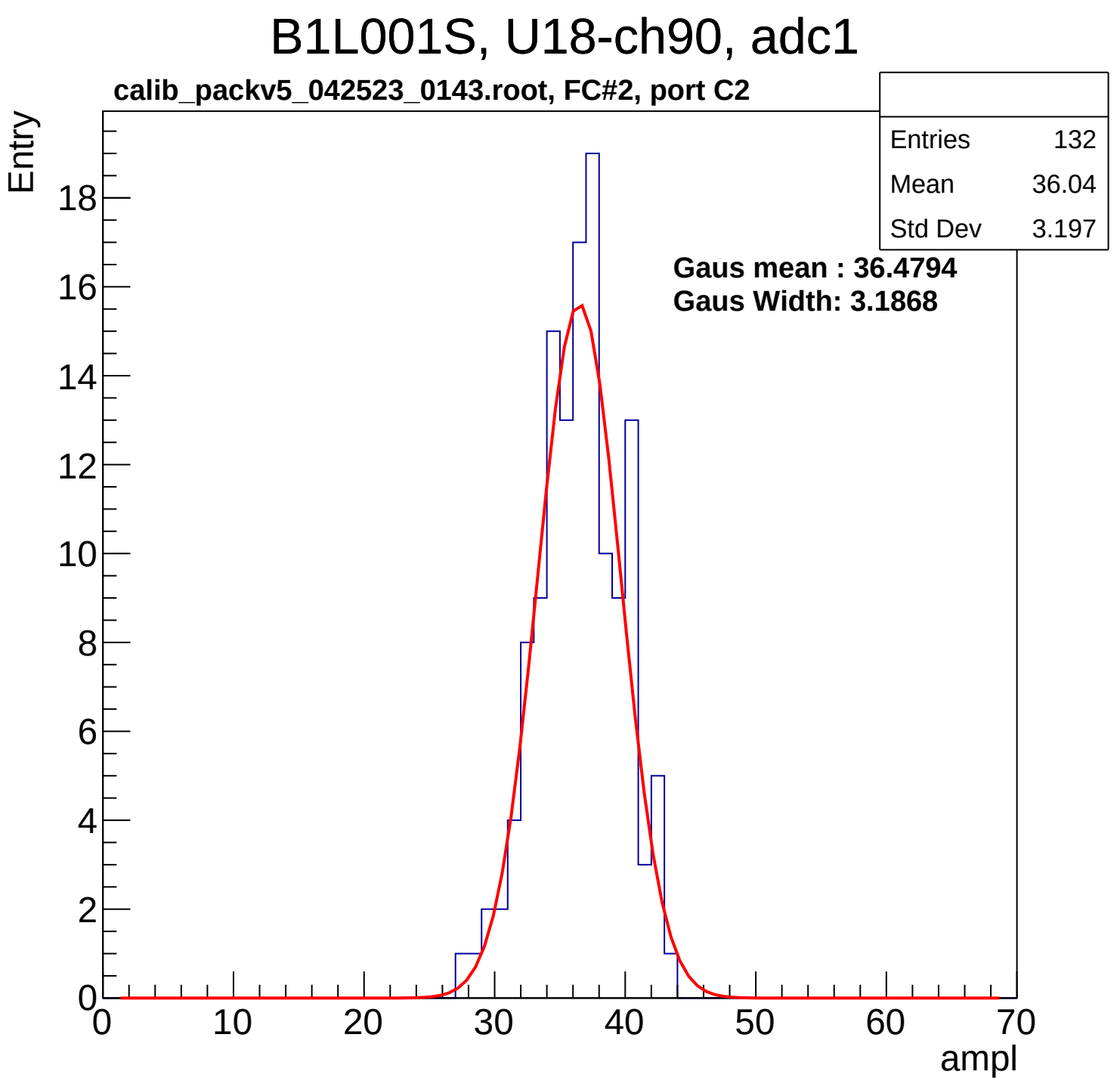

B1L001S, U18-ch89, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 70
Mean 56.1
Std Dev 2.909
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

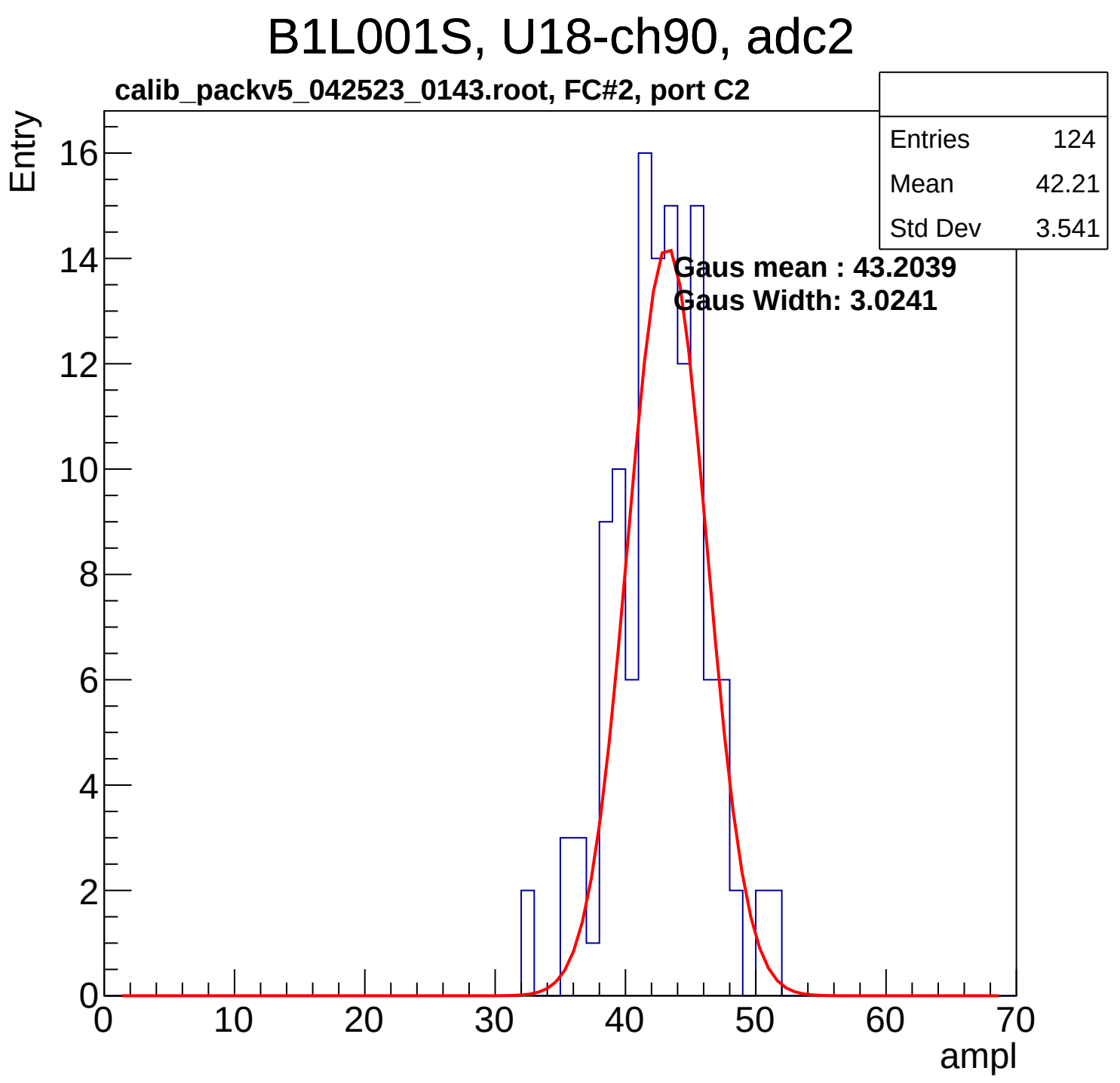

B1L001S, U18-ch89, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 102
Mean 58.94
Std Dev 8.608
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

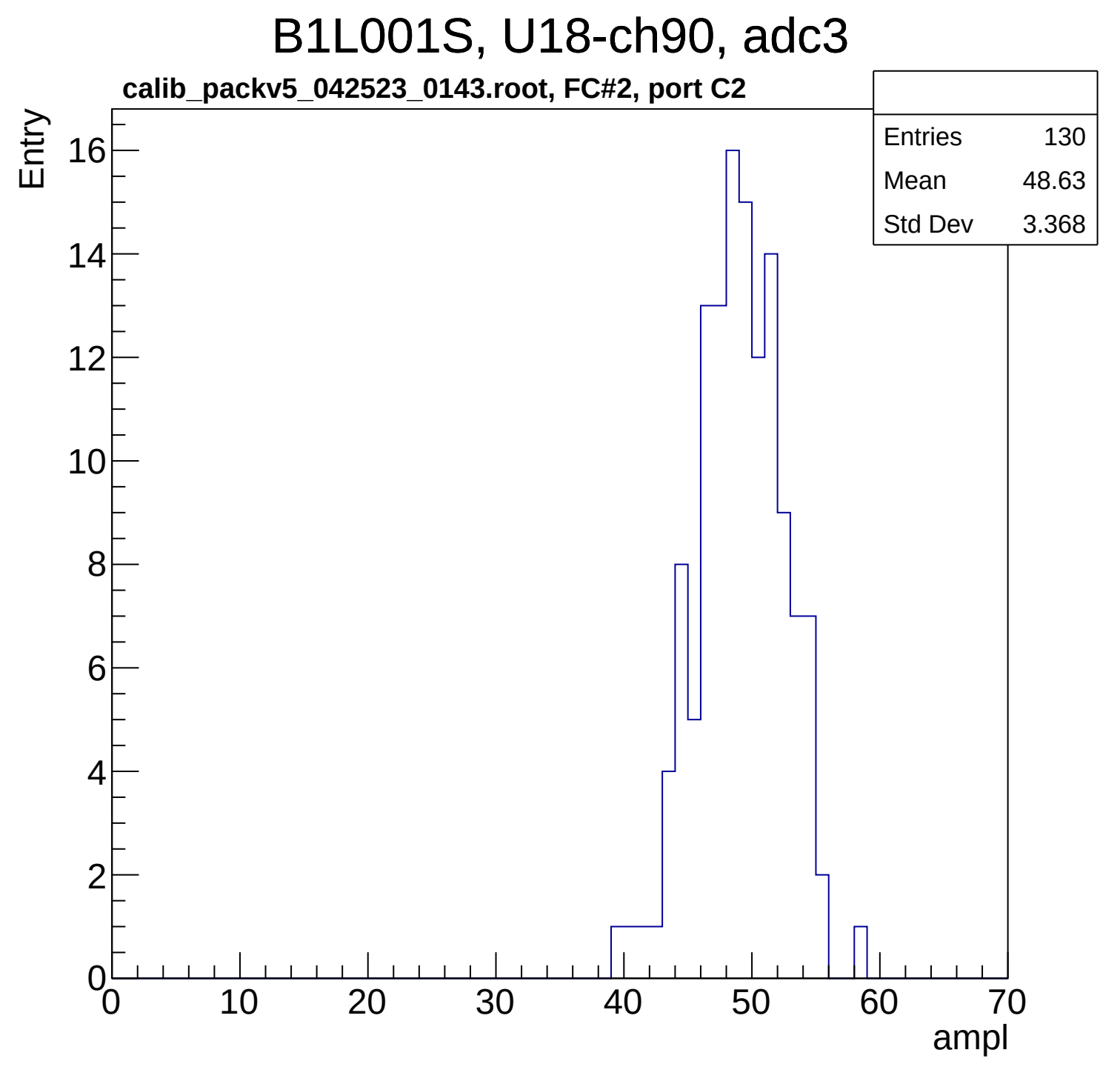

B1L001S, U18-ch89, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 7
Mean 61.43
Std Dev 1.761
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

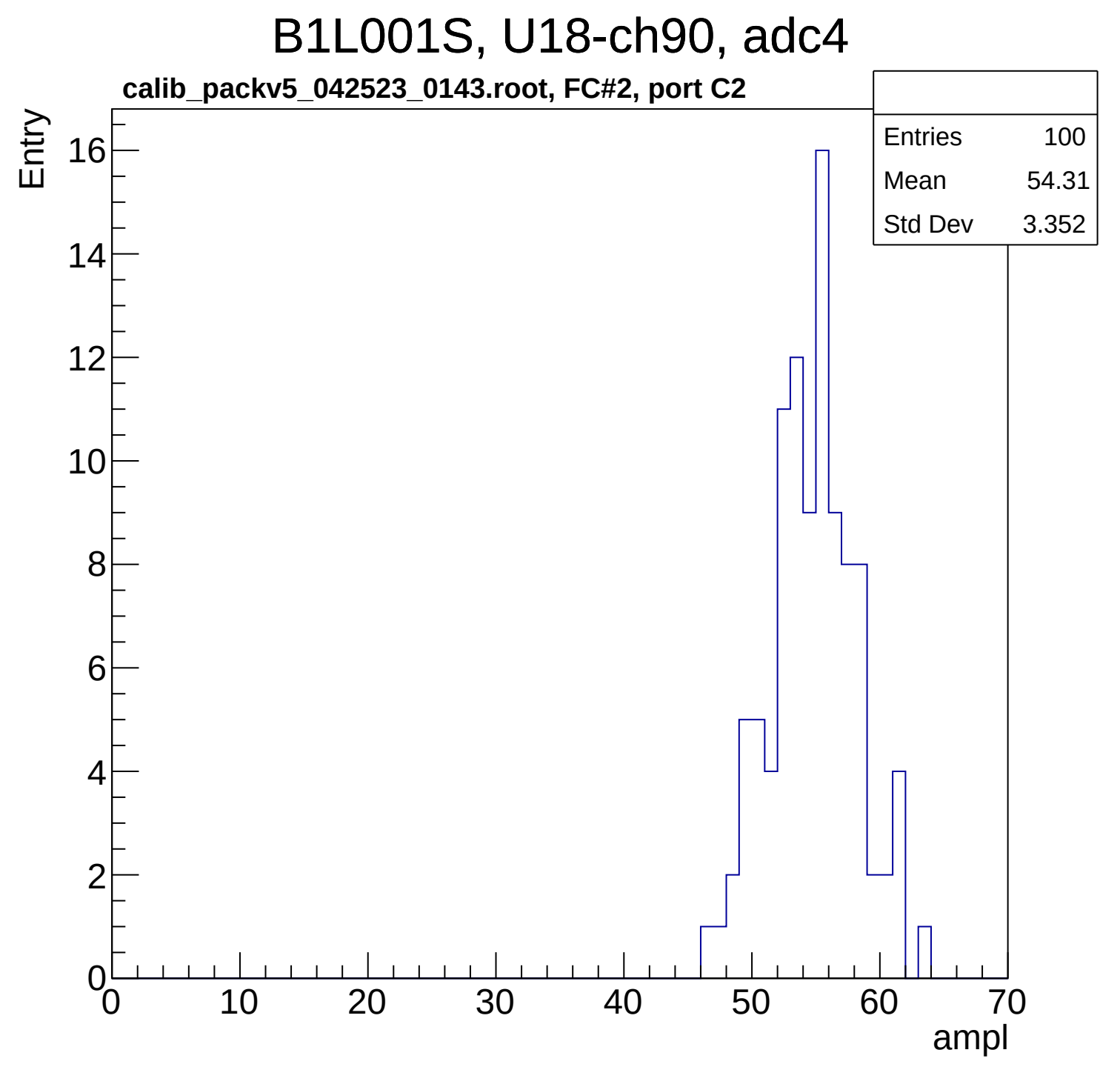

B1L001S, U18-ch89, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 0
Std Dev 0
Entry
2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

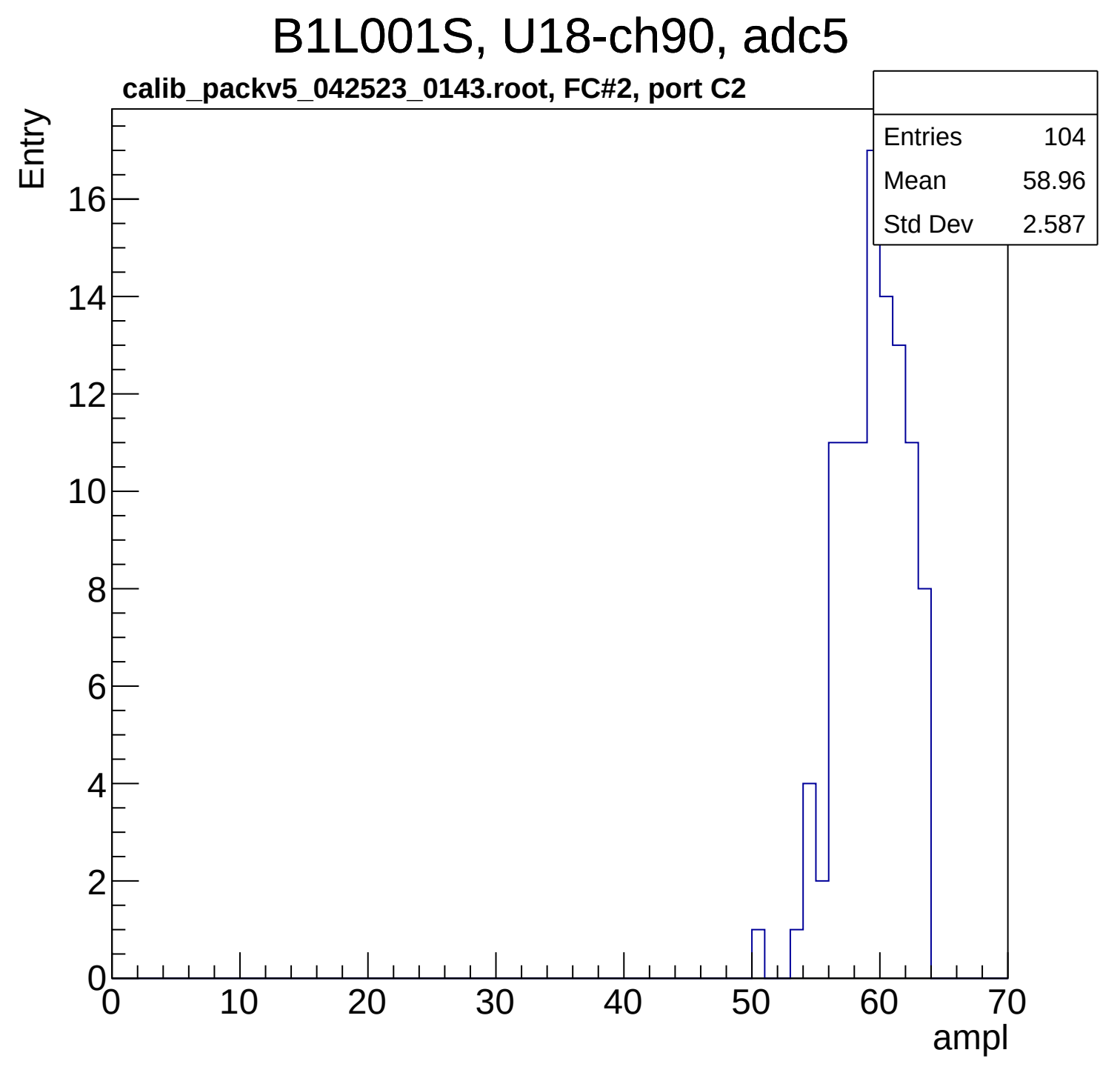

B1L001S, U18-ch90, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 137
Mean 29.05
Std Dev 3.252
Gaus mean : 29.8370
Gaus Width: 3.4170
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

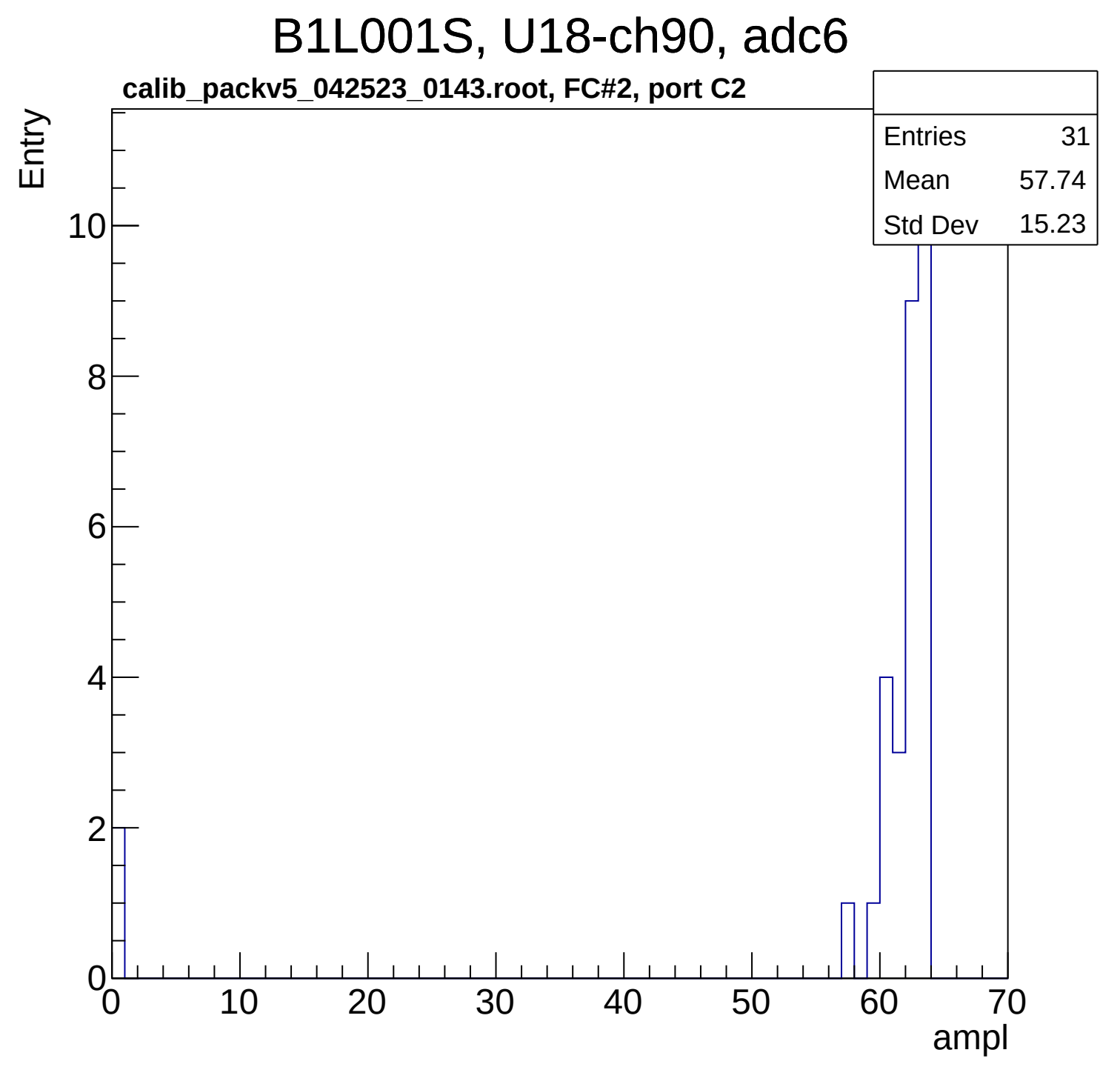

B1L001S, U18-ch90, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 132
Mean 36.04
Std Dev 3.197
Gaus mean : 36.4794
Gaus Width: 3.1868
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

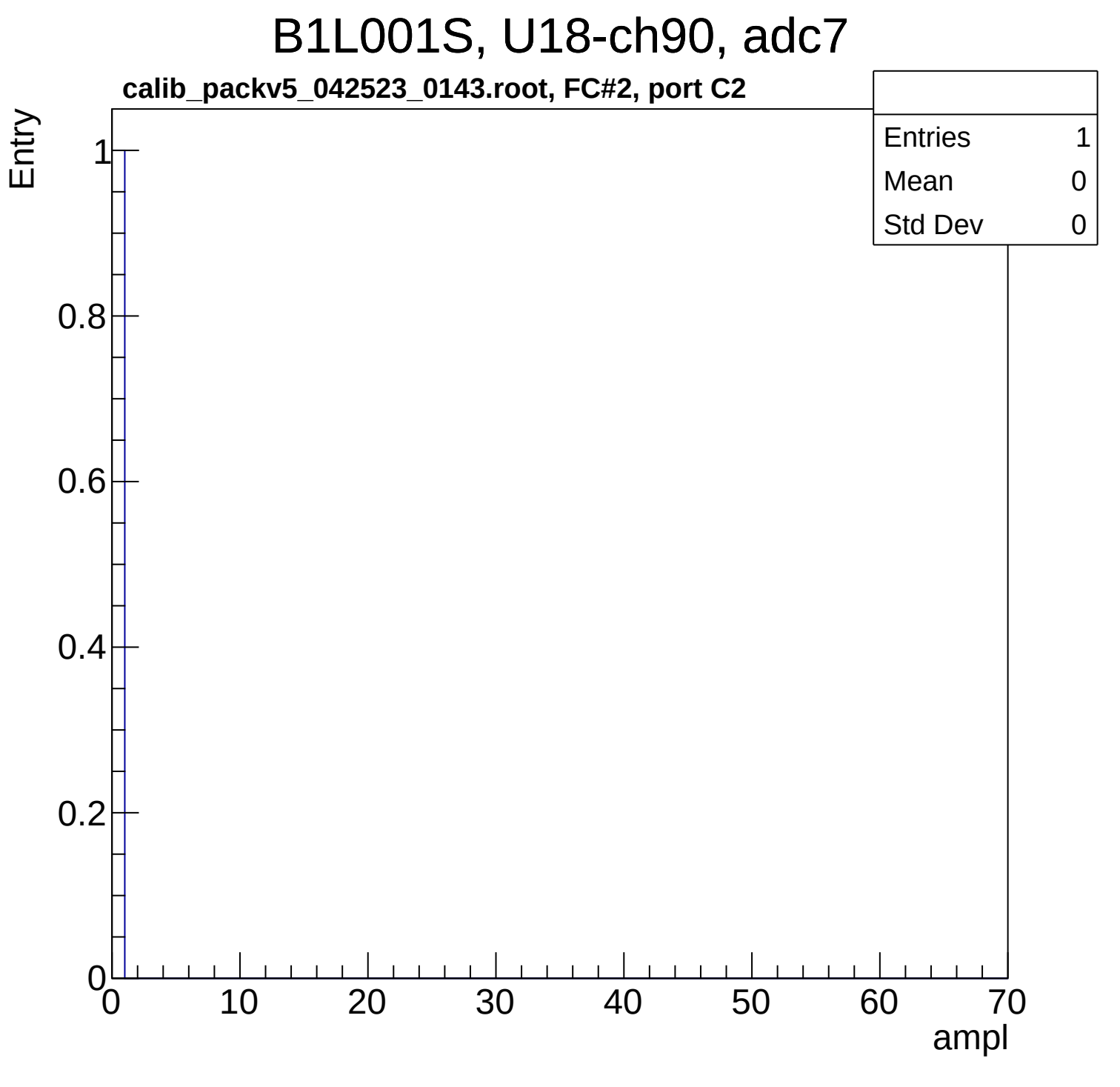

B1L001S, U18-ch90, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 124
Mean 42.21
Std Dev 3.541
Gaus mean : 43.2039
Gaus Width: 3.0241
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

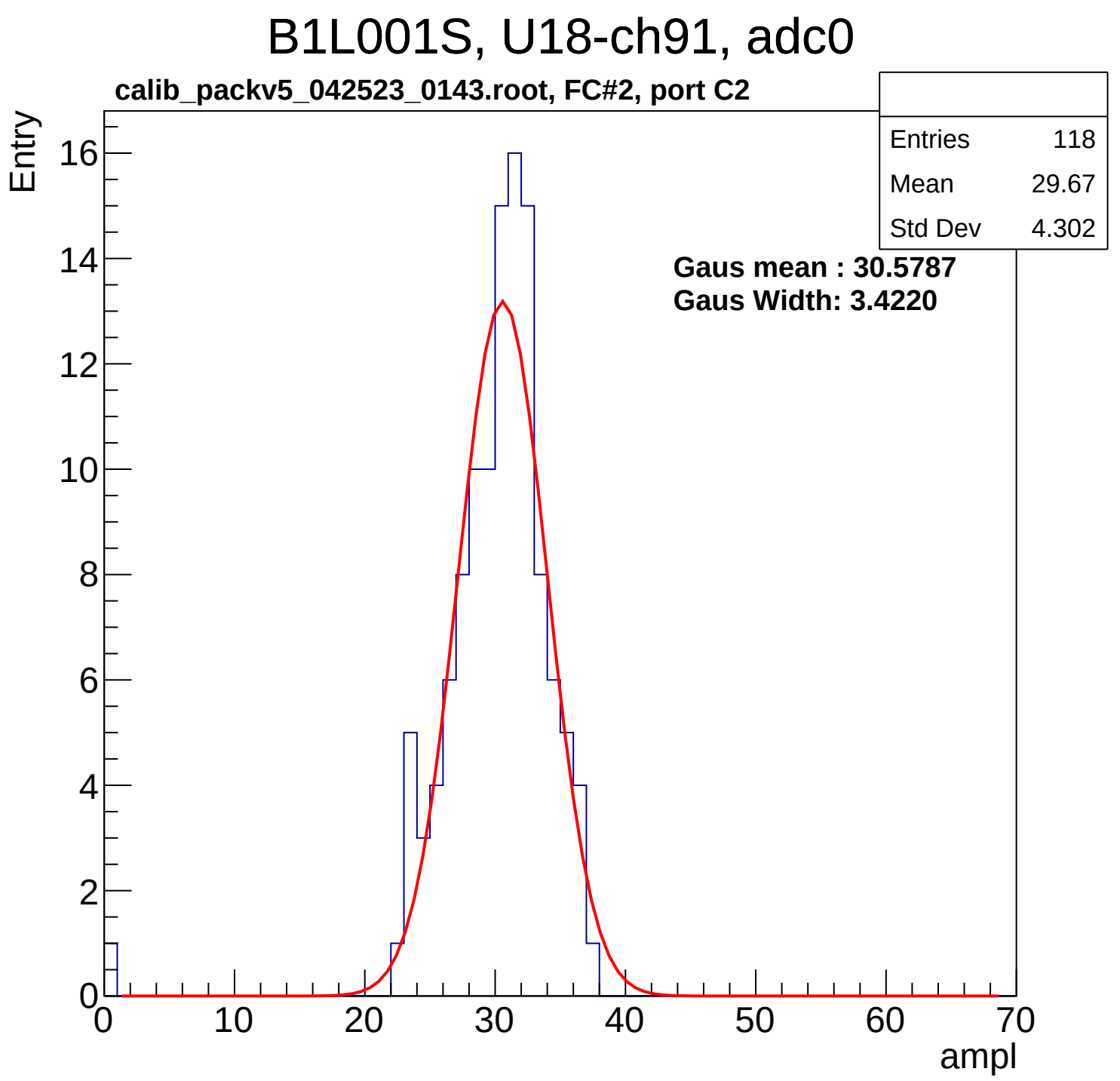

B1L001S, U18-ch90, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 130
Mean 48.63
Std Dev 3.368
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

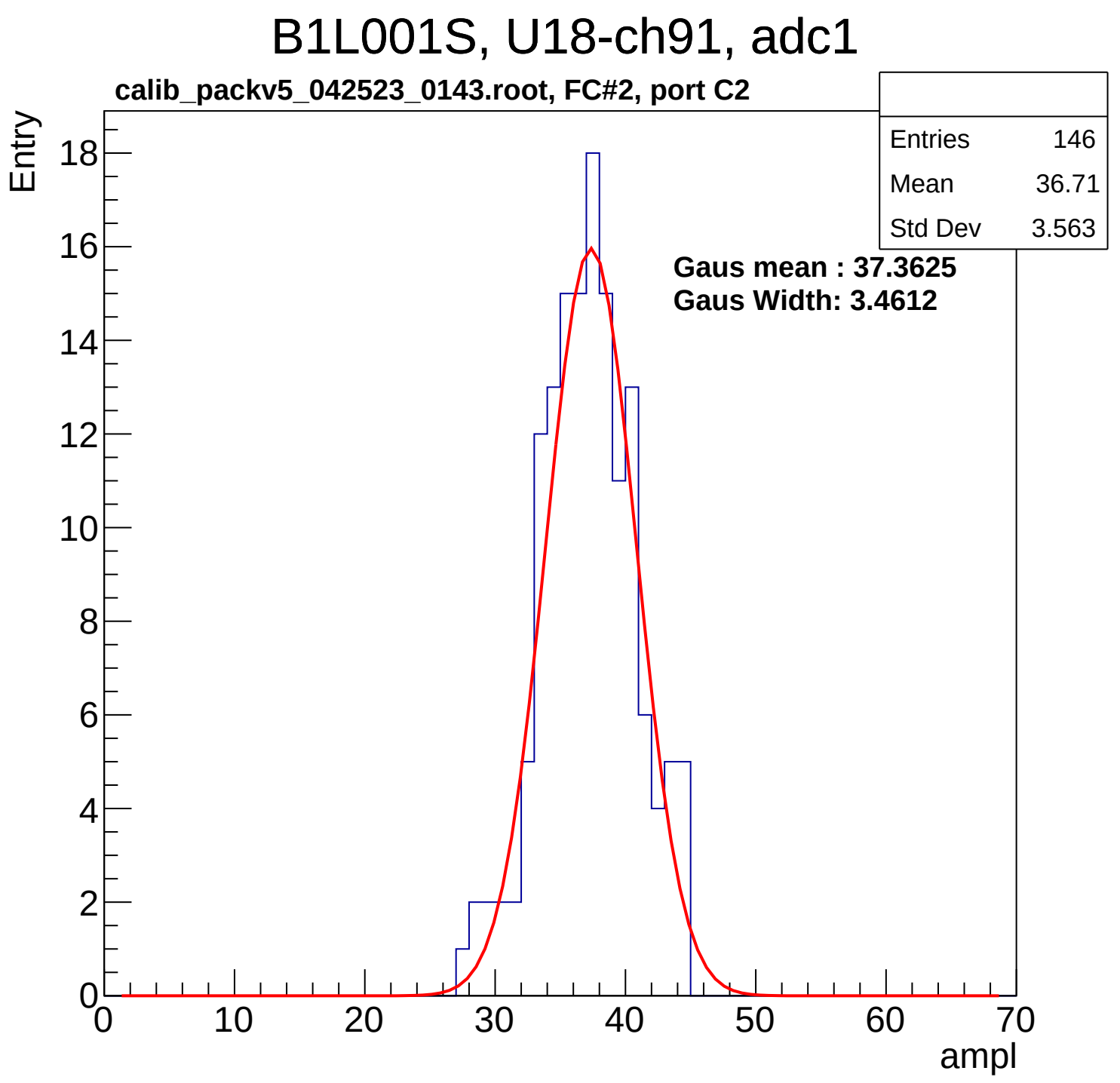

B1L001S, U18-ch90, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 100
Mean 54.31
Std Dev 3.352
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

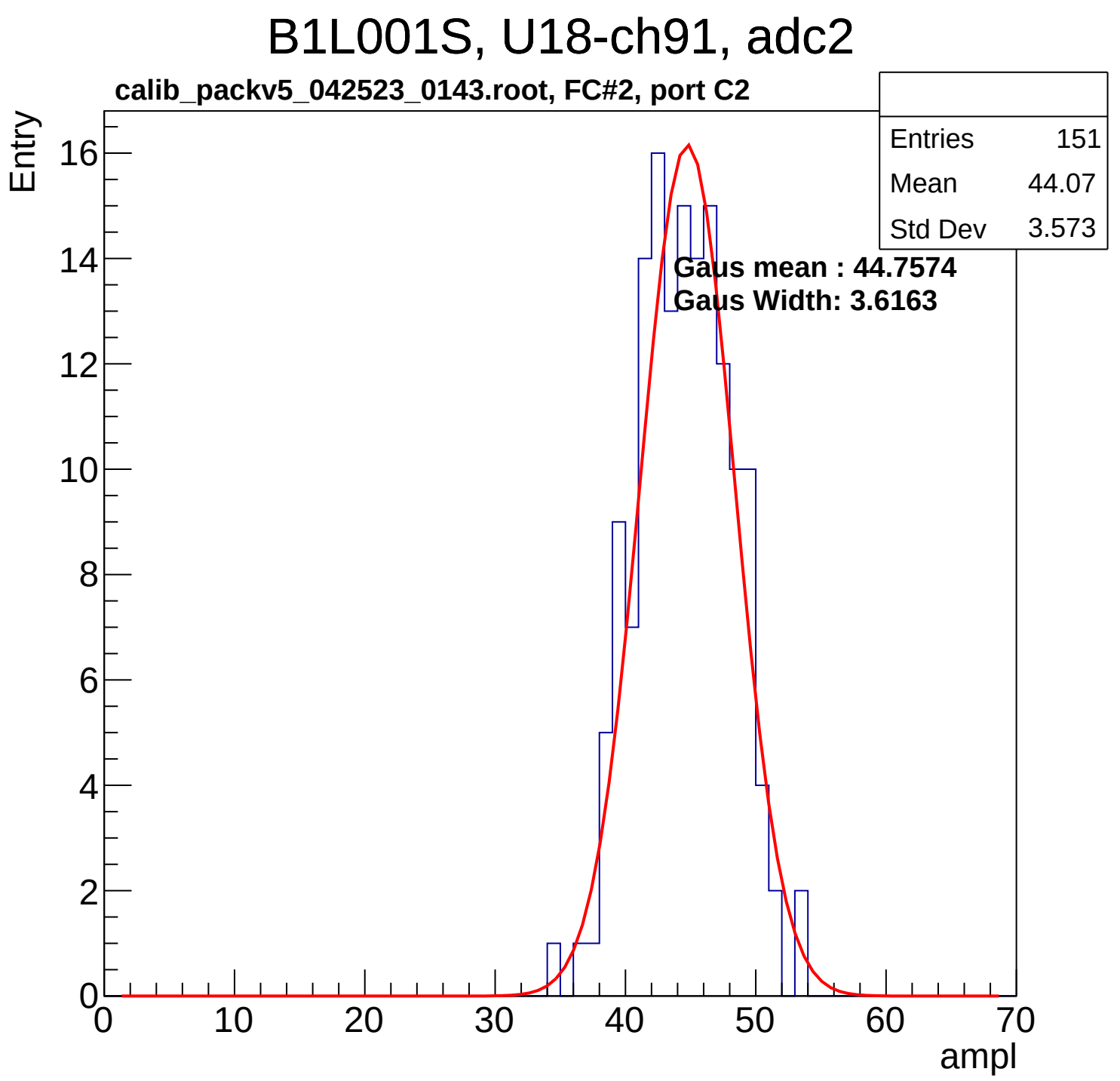

B1L001S, U18-ch90, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 104
Mean 58.96
Std Dev 2.587
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

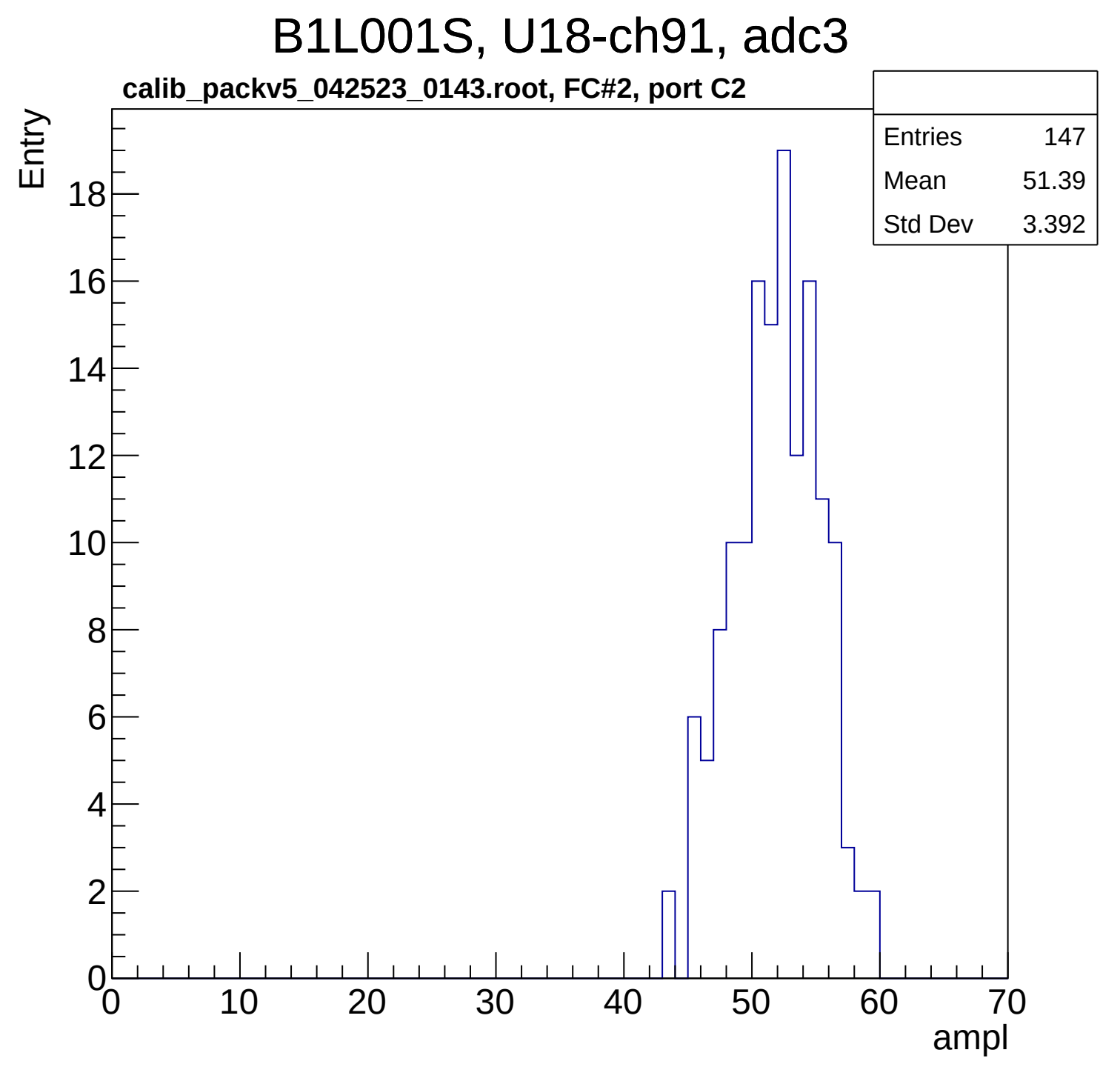

B1L001S, U18-ch90, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 31
Mean 57.74
Std Dev 15.23
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

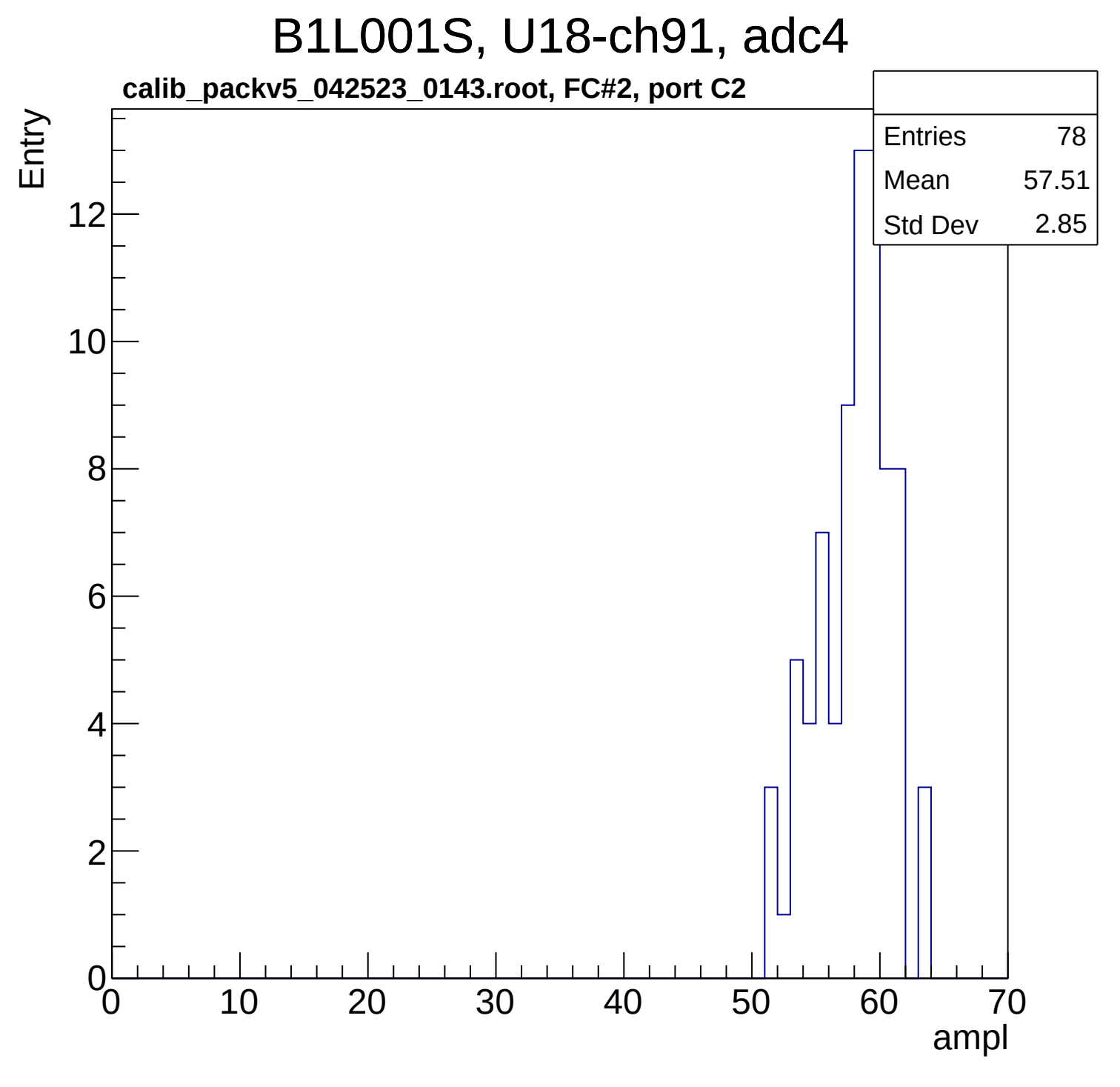

B1L001S, U18-ch90, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

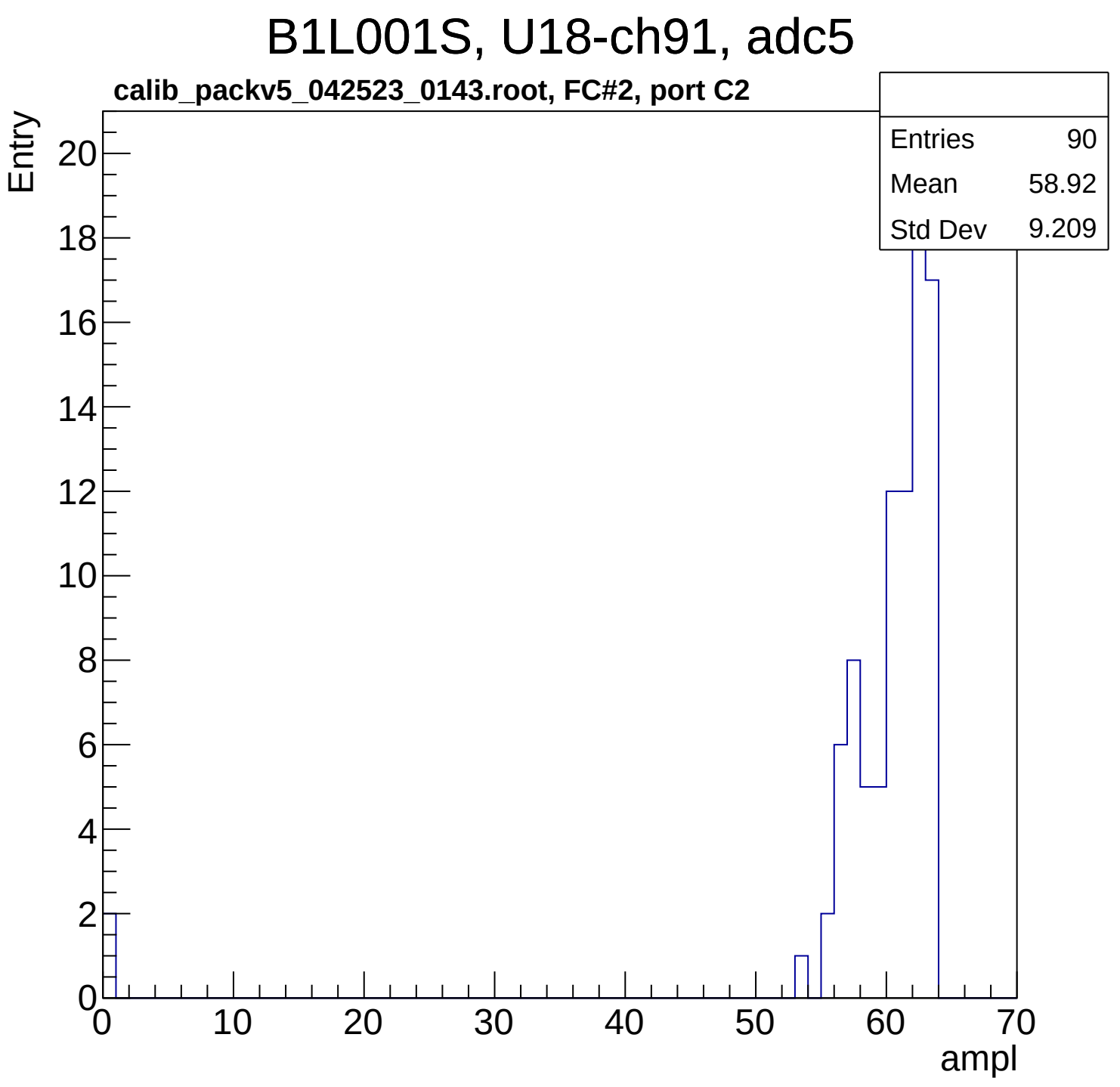

B1L001S, U18-ch91, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 118
Mean 29.67
Std Dev 4.302
Gaus mean : 30.5787
Gaus Width: 3.4220
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

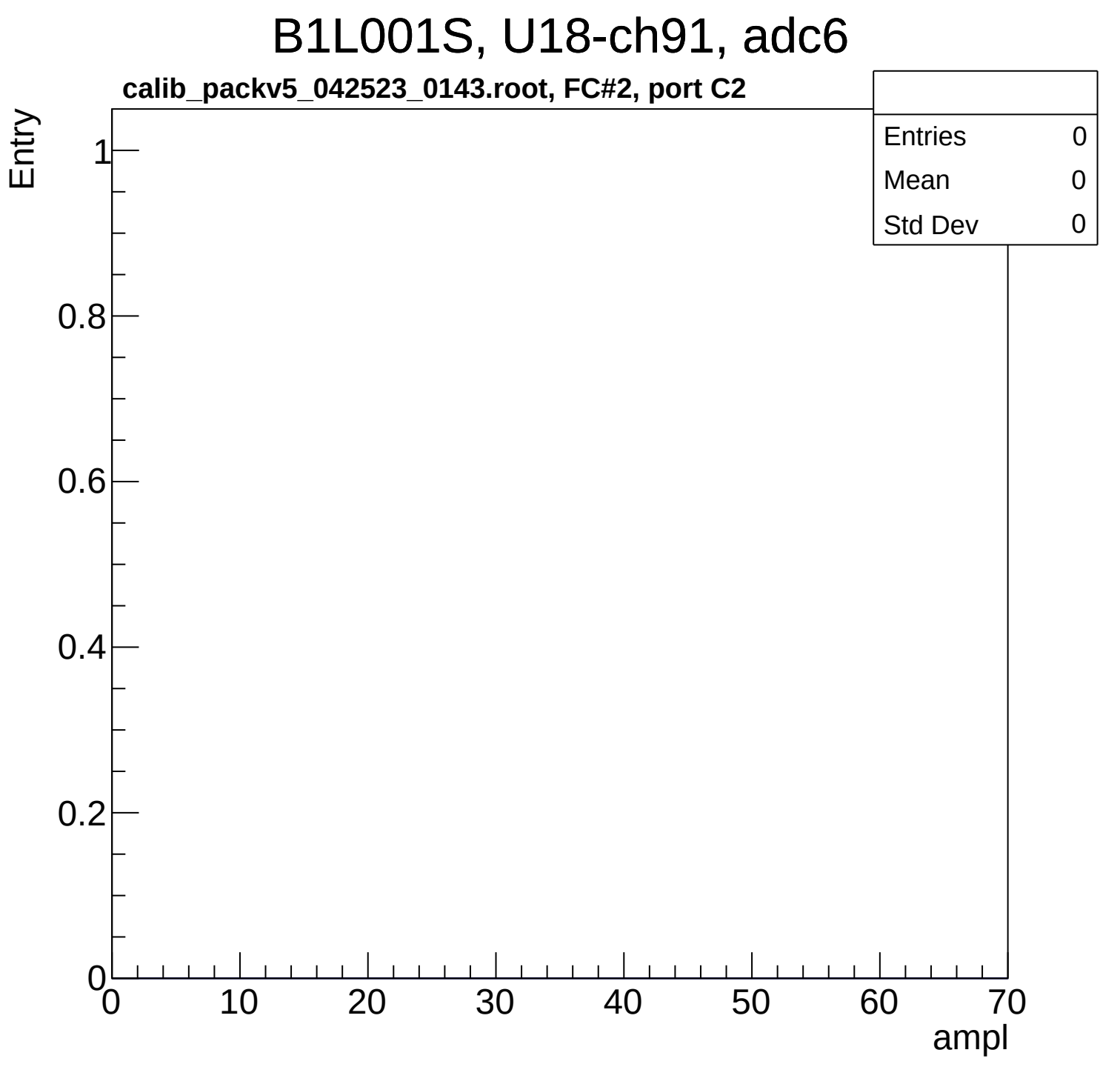

B1L001S, U18-ch91, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 146
Mean 36.71
Std Dev 3.563
Gaus mean : 37.3625
Gaus Width: 3.4612
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

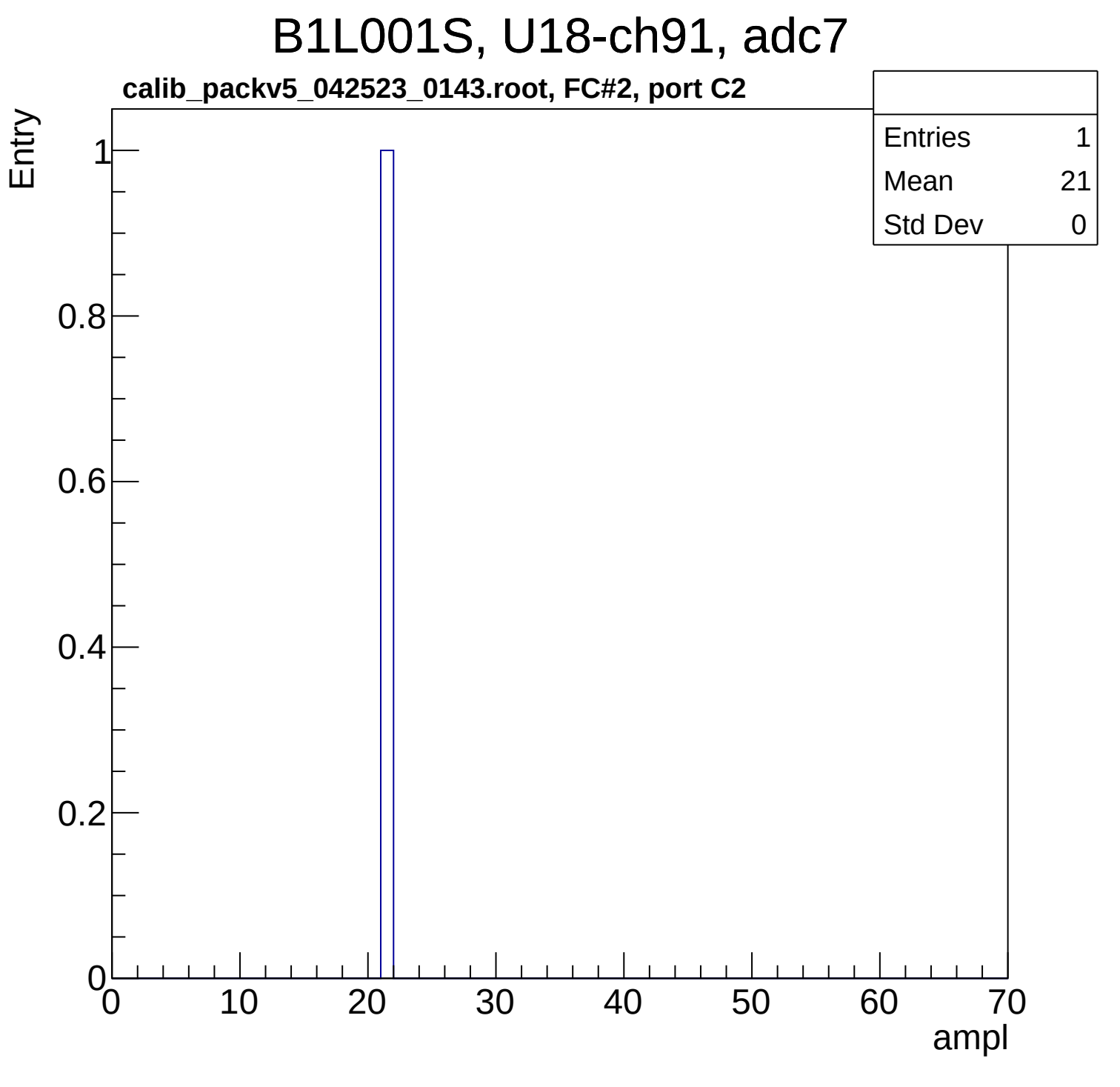

B1L001S, U18-ch91, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 151
Mean 44.07
Std Dev 3.573
Gaus mean : 44.7574
Gaus Width: 3.6163
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

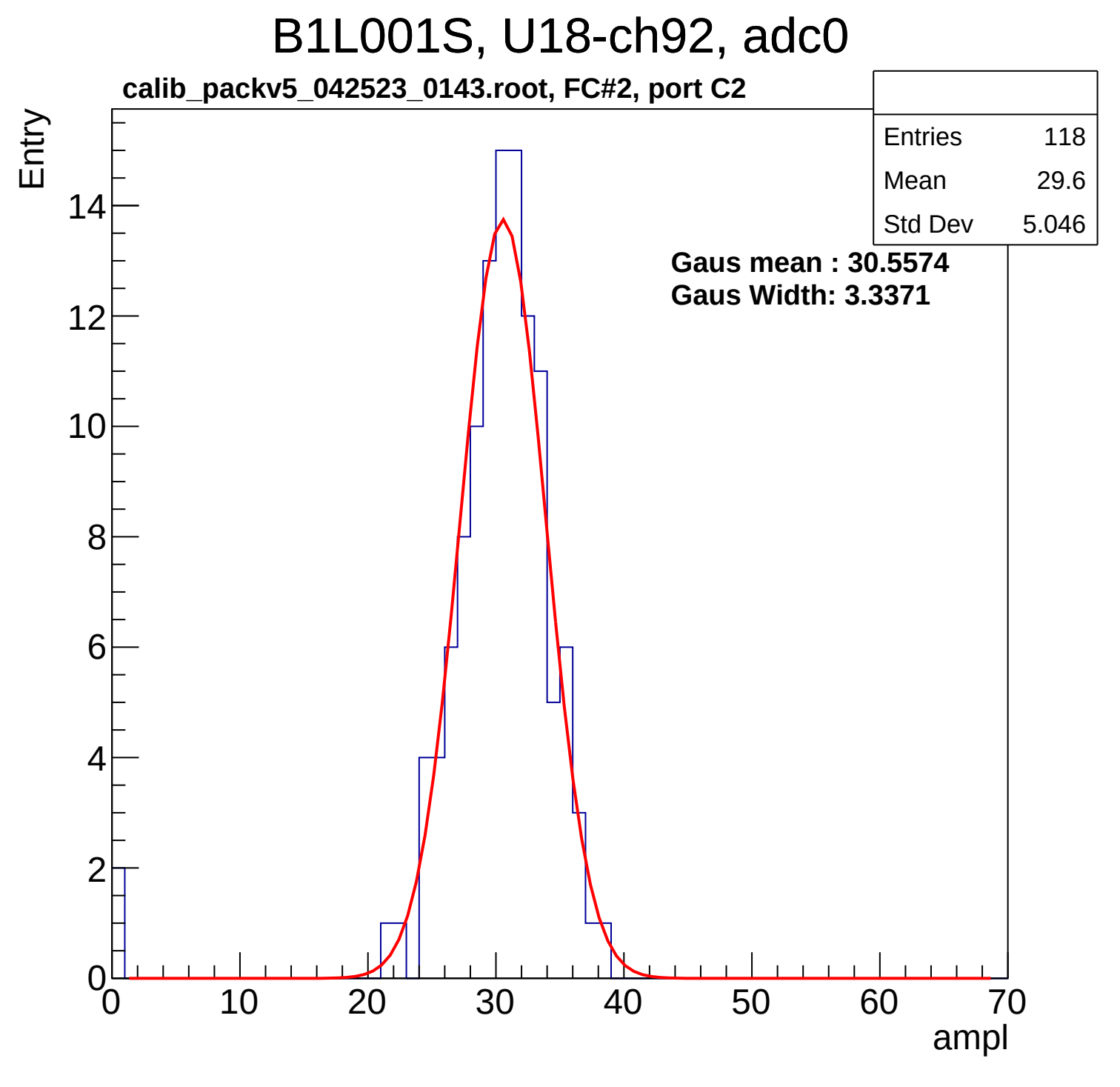

B1L001S, U18-ch91, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 147
Mean 51.39
Std Dev 3.392
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

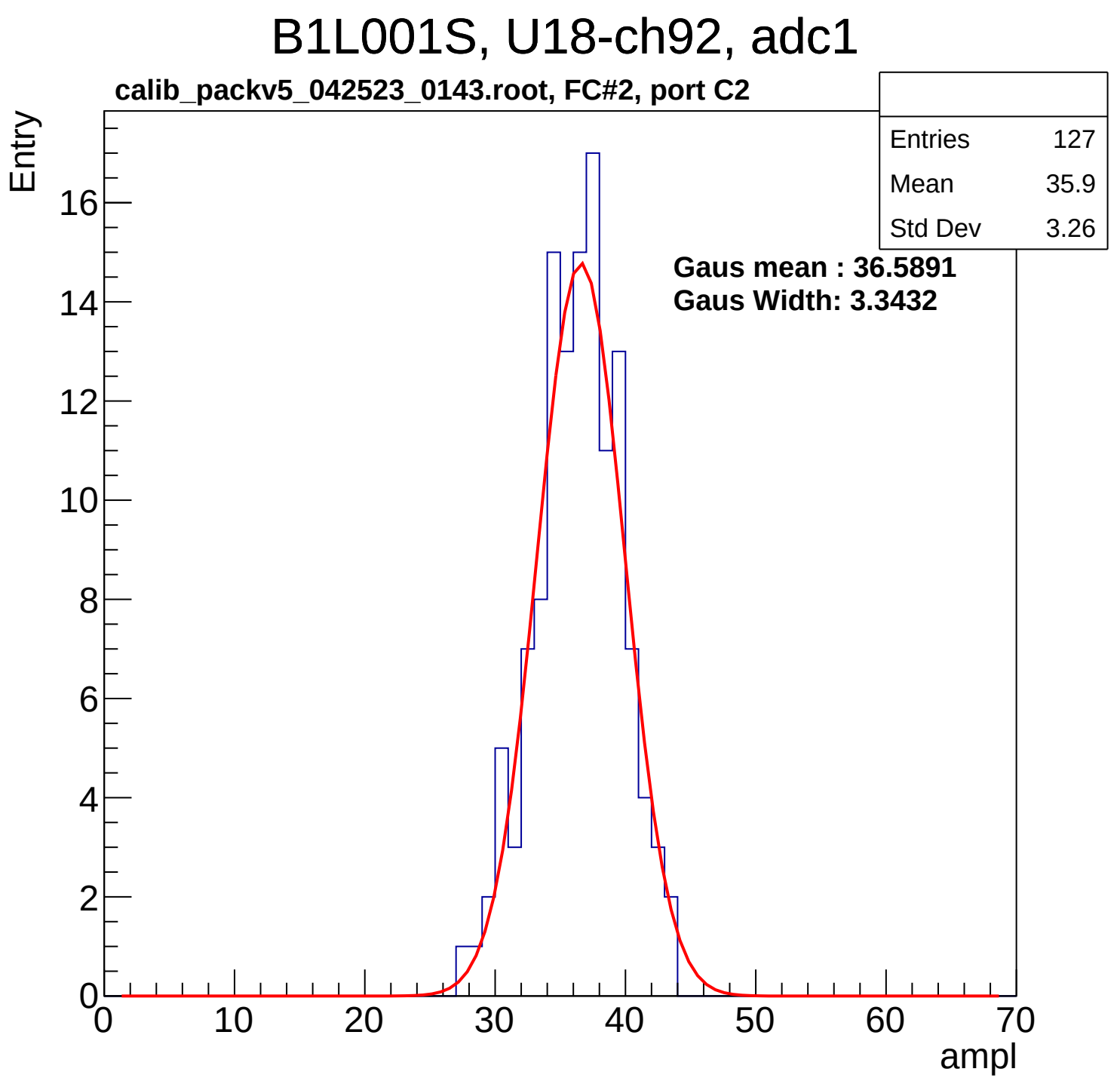

B1L001S, U18-ch91, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 78
Mean 57.51
Std Dev 2.85
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70

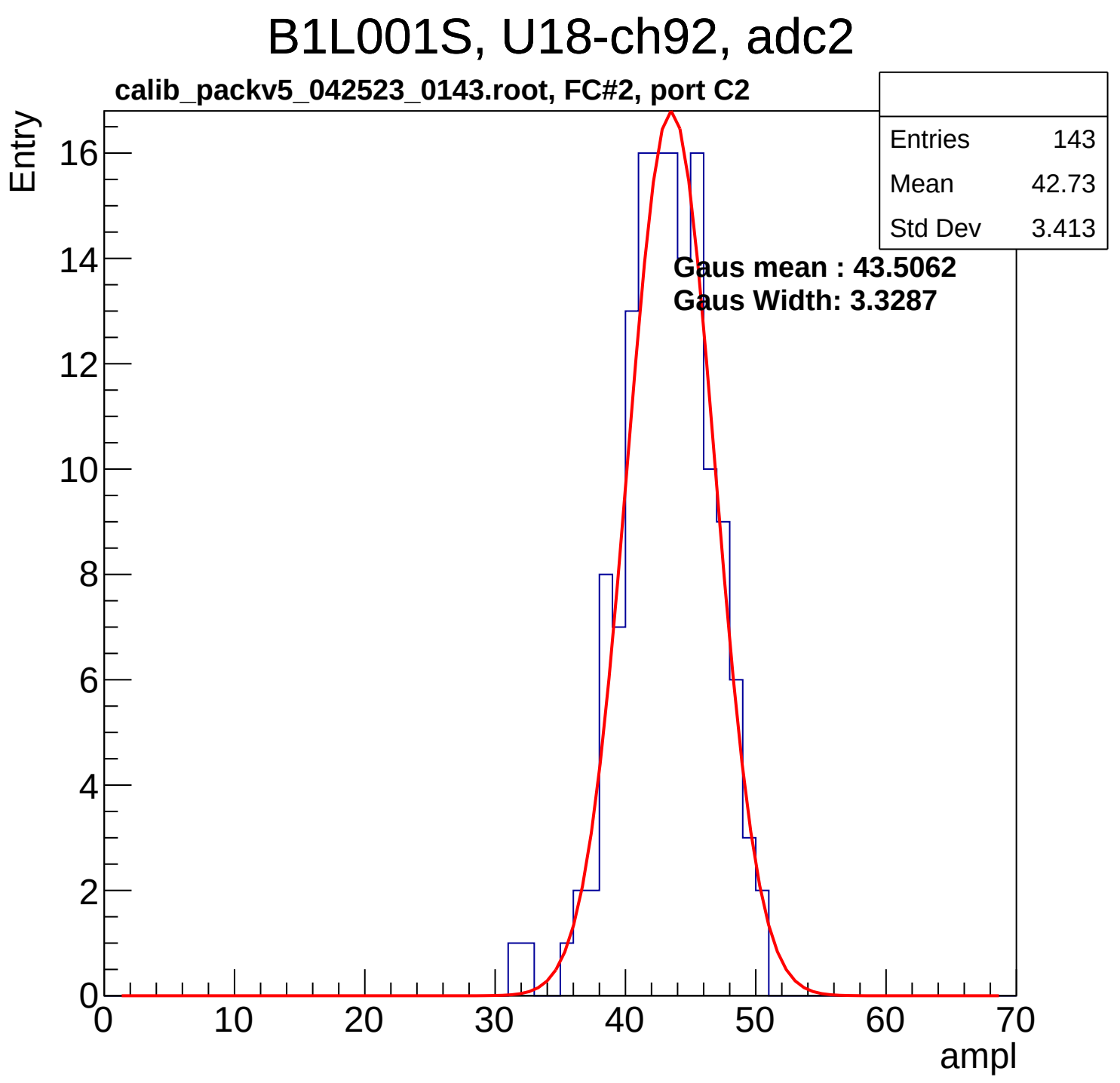

B1L001S, U18-ch91, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 90
Mean 58.92
Std Dev 9.209
Entry
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70
ampl

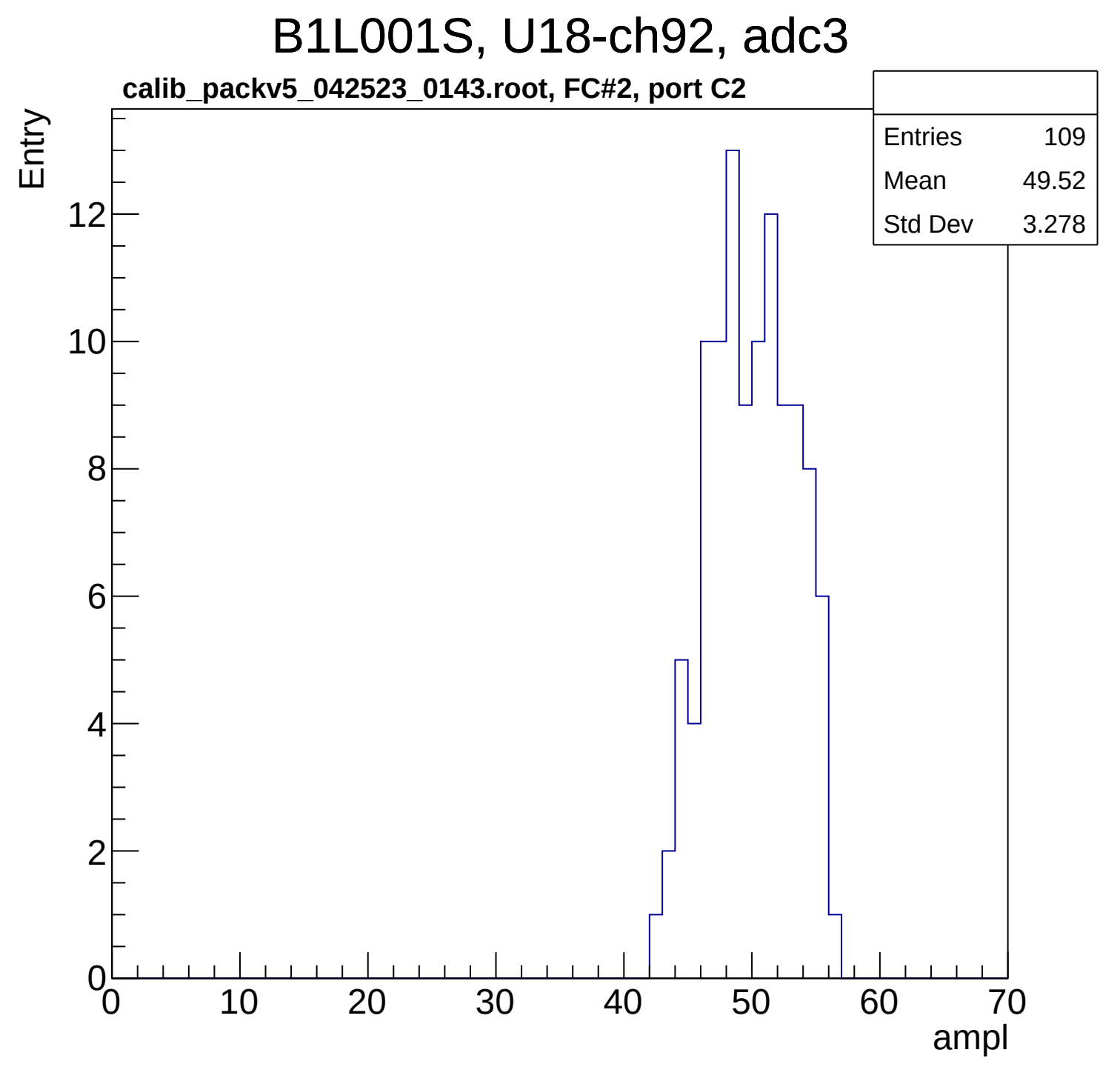

B1L001S, U18-ch91, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

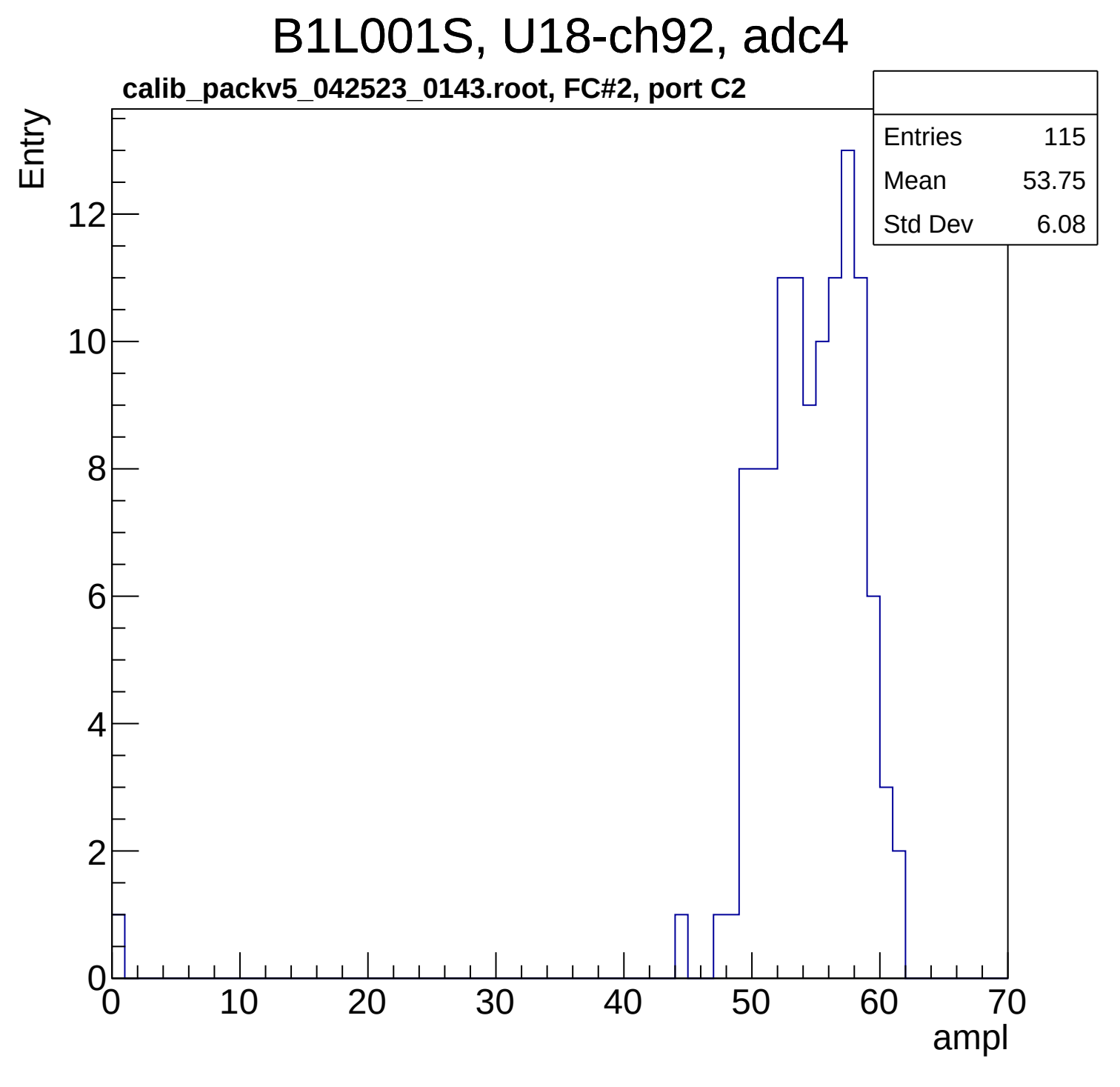

B1L001S, U18-ch91, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 21
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

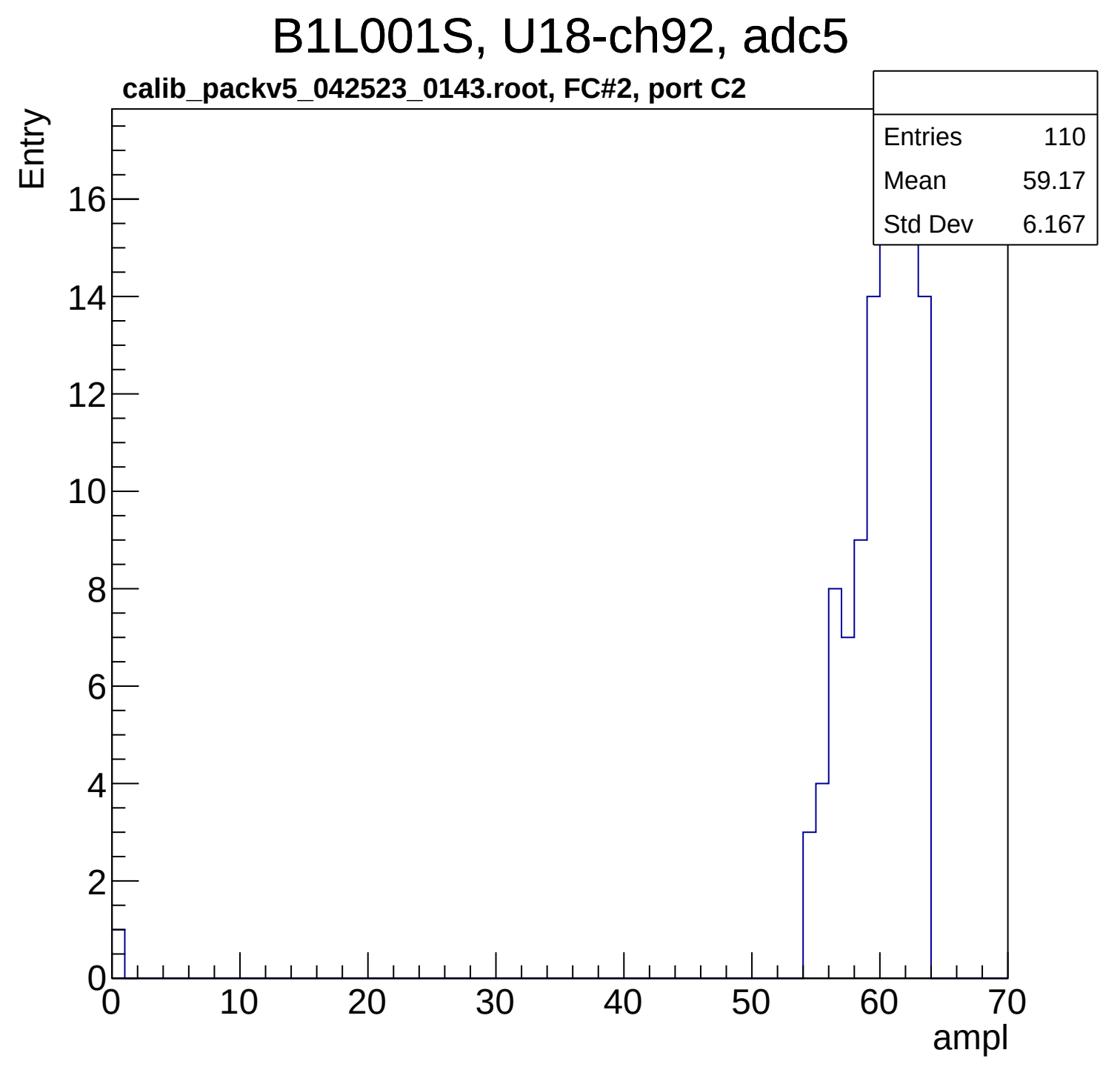

B1L001S, U18-ch92, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 118
Mean 29.6
Std Dev 5.046
Gaus mean : 30.5574
Gaus Width: 3.3371
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

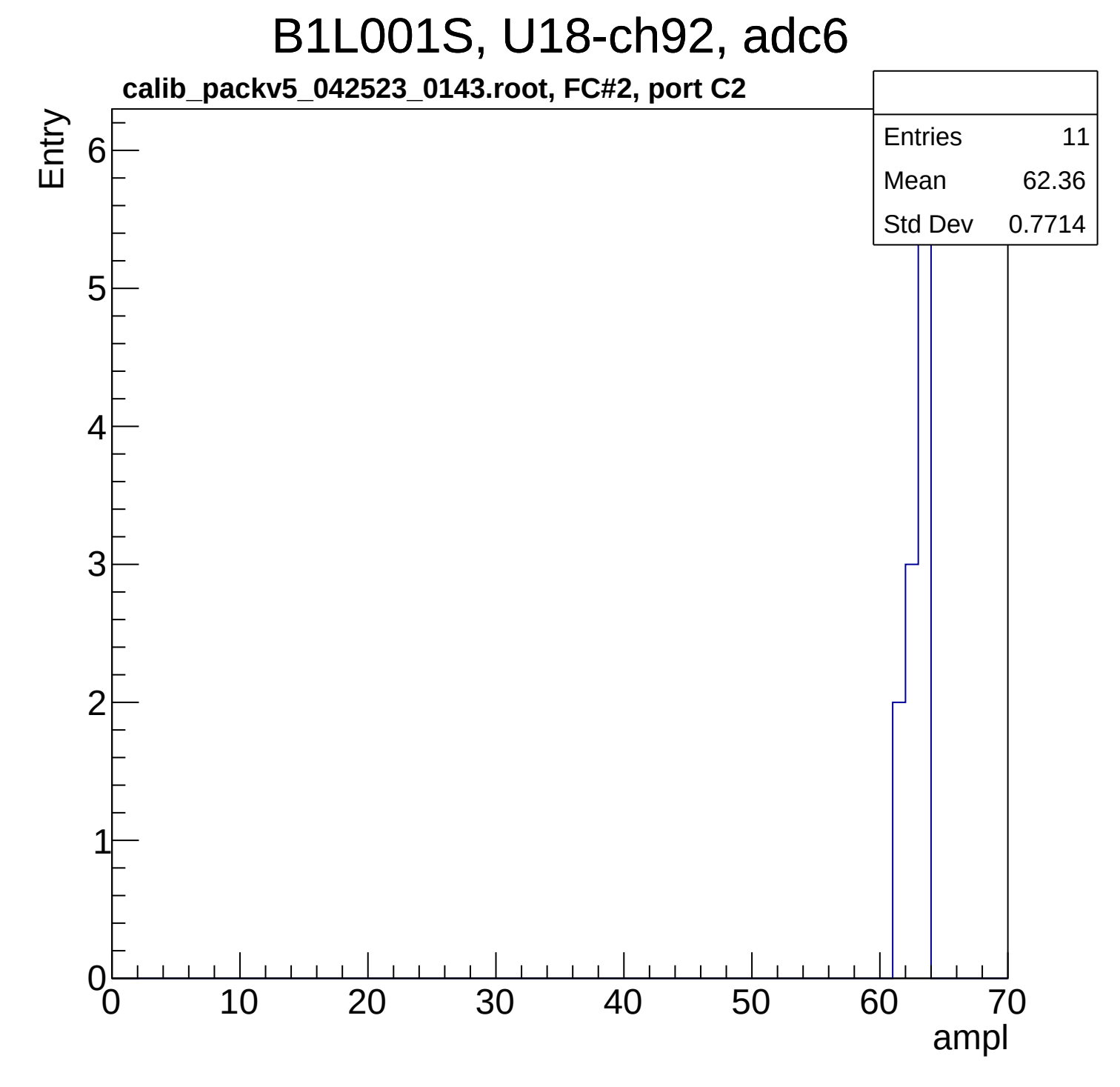

B1L001S, U18-ch92, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 127
Mean 35.9
Std Dev 3.26
Gaus mean : 36.5891
Gaus Width: 3.3432
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

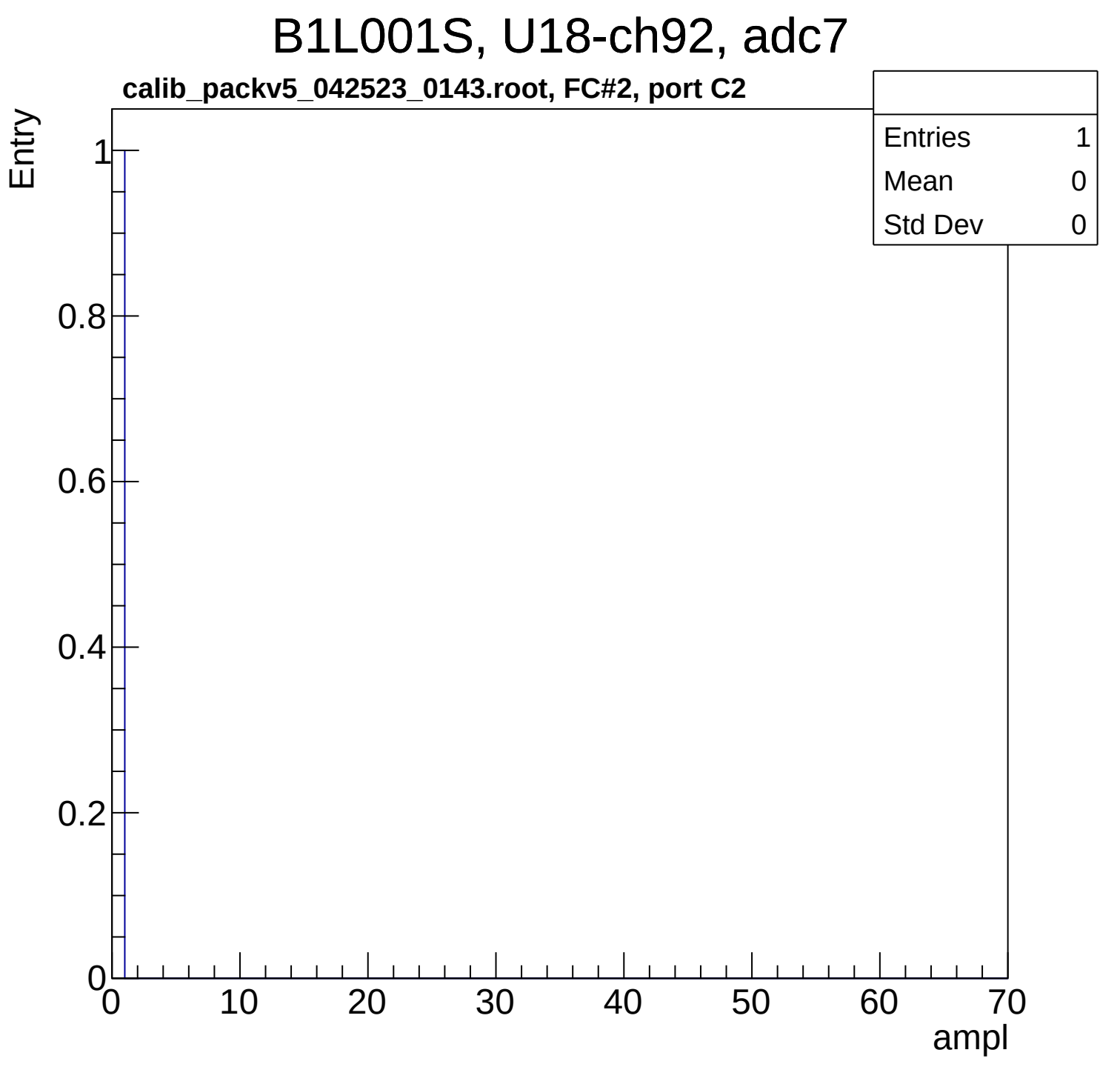

B1L001S, U18-ch92, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 143
Mean 42.73
Std Dev 3.413
Gaus mean : 43.5062
Gaus Width: 3.3287
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

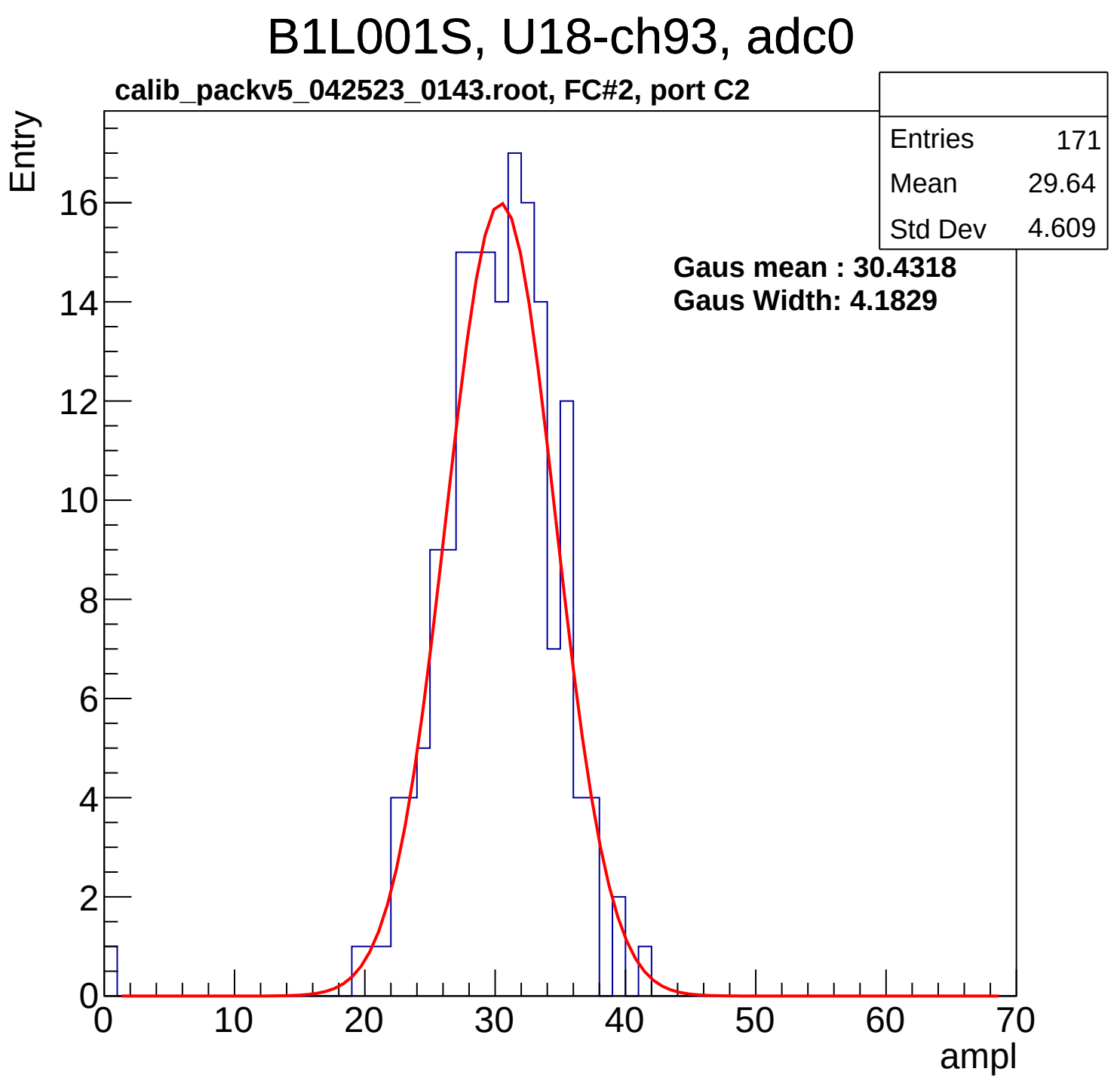

B1L001S, U18-ch92, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 109
Mean 49.52
Std Dev 3.278
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl

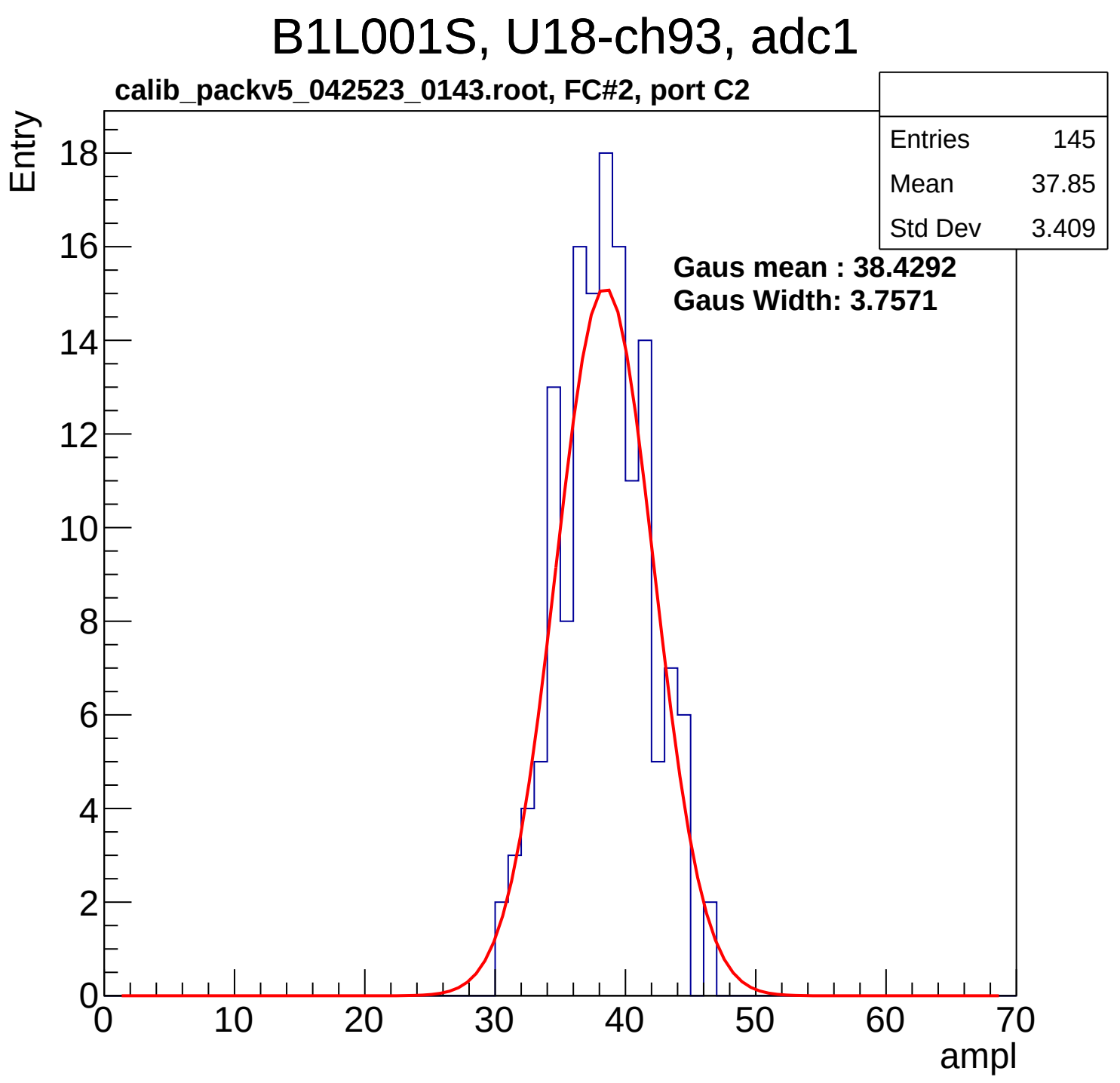

B1L001S, U18-ch92, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 115
Mean 53.75
Std Dev 6.08
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70

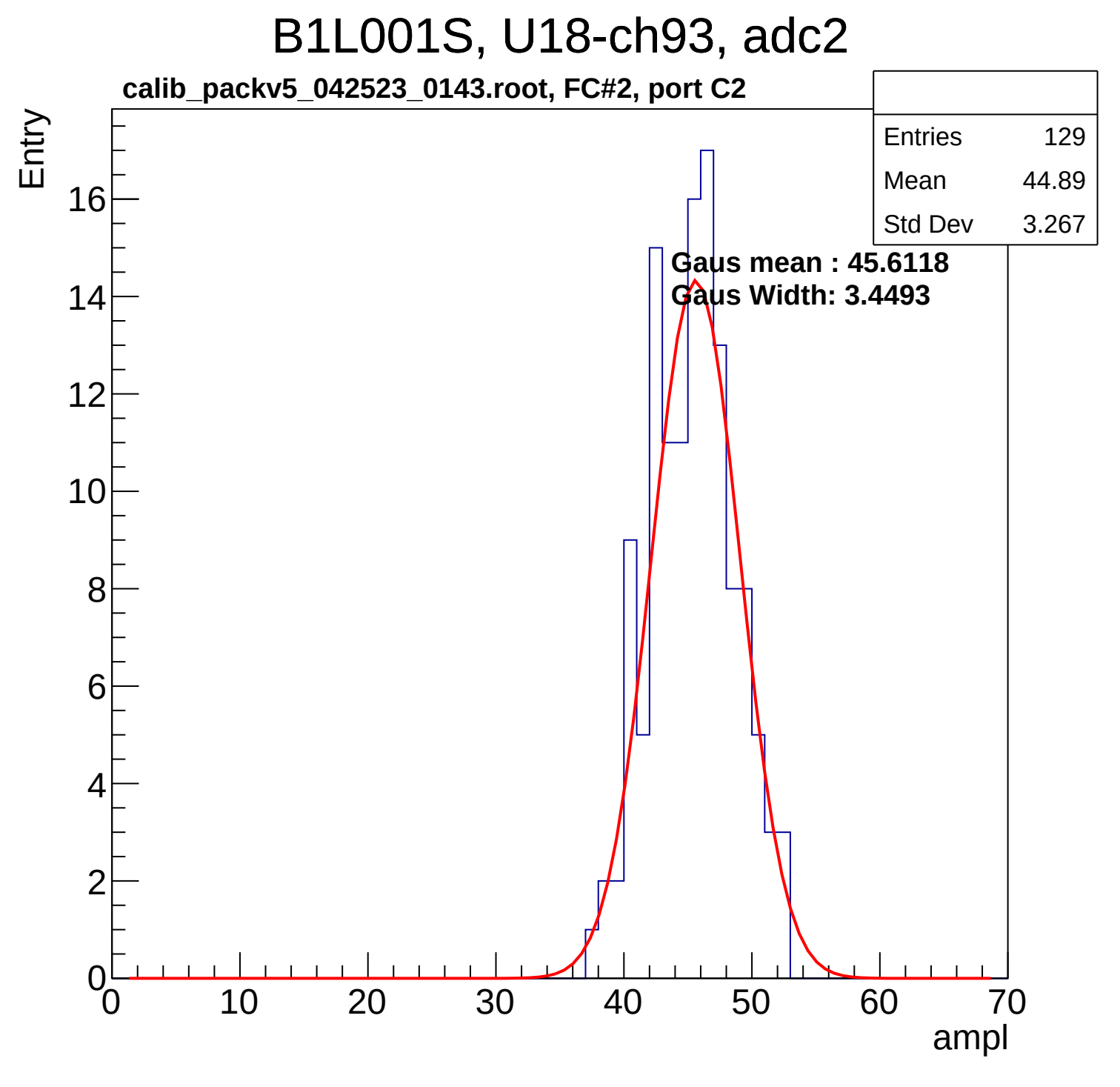

B1L001S, U18-ch92, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 110
Mean 59.17
Std Dev 6.167
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

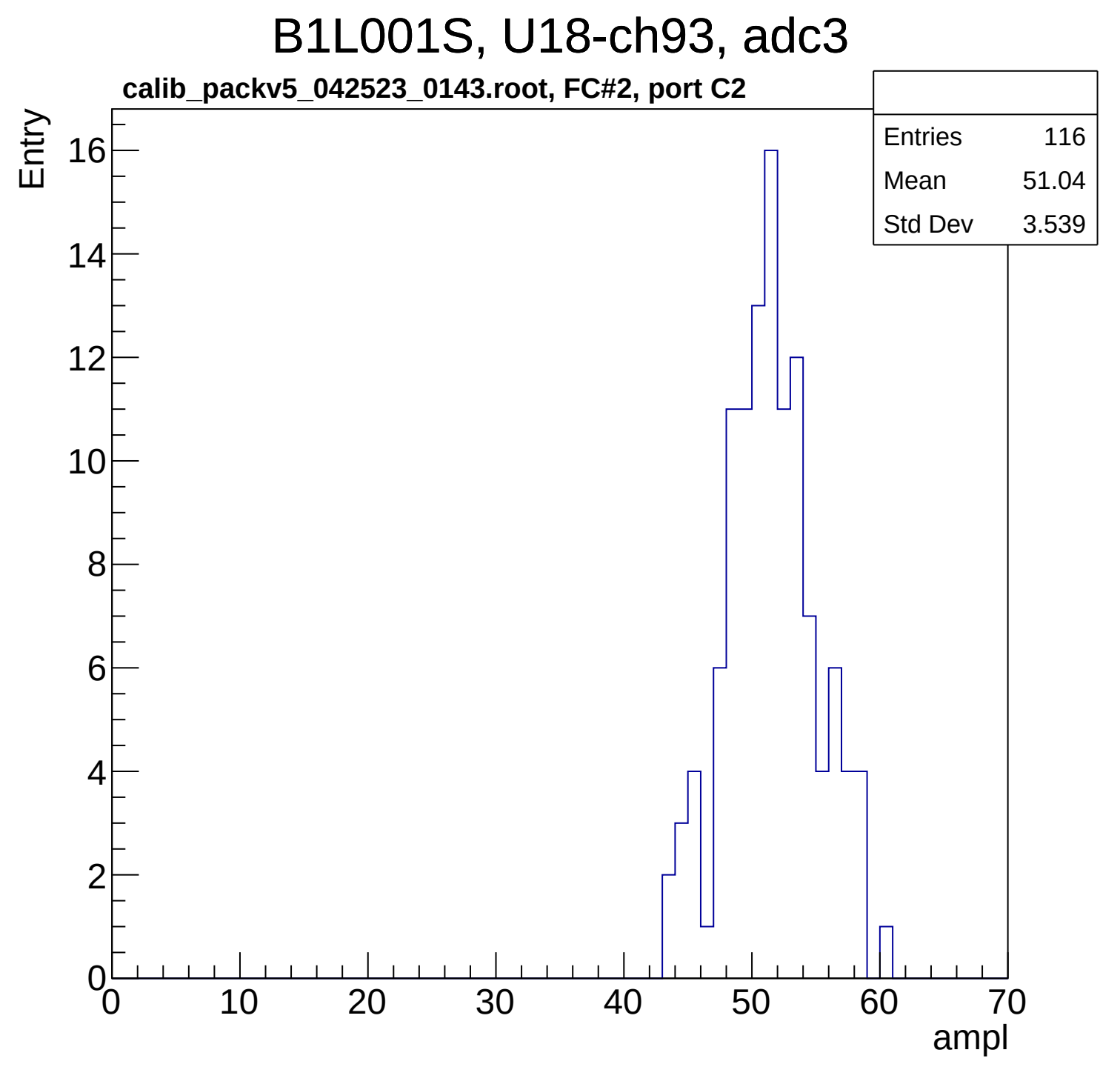

B1L001S, U18-ch92, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 11
Mean 62.36
Std Dev 0.7714
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

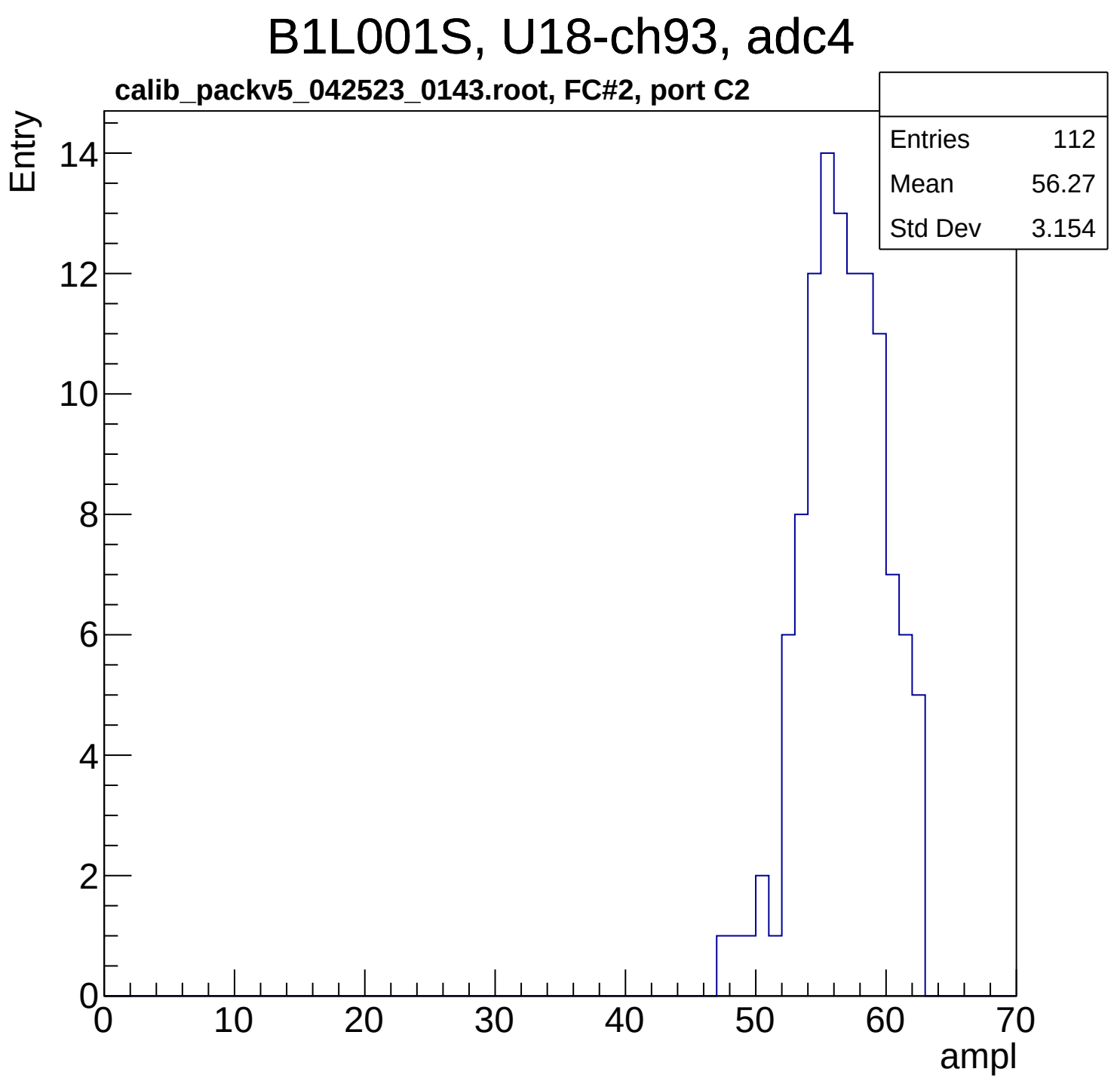

B1L001S, U18-ch92, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

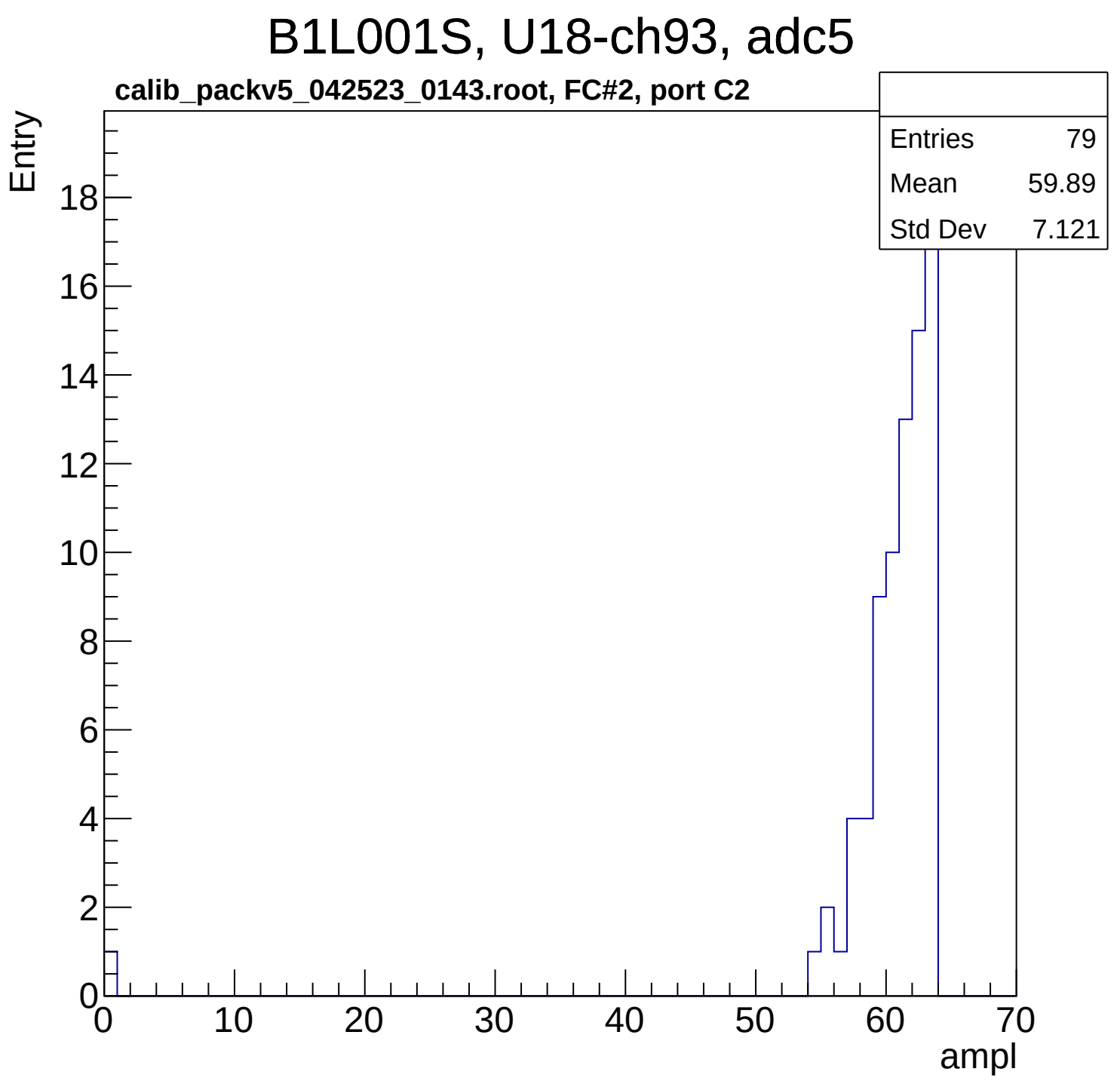

B1L001S, U18-ch93, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 171
Mean 29.64
Std Dev 4.609
Gaus mean : 30.4318
Gaus Width: 4.1829
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

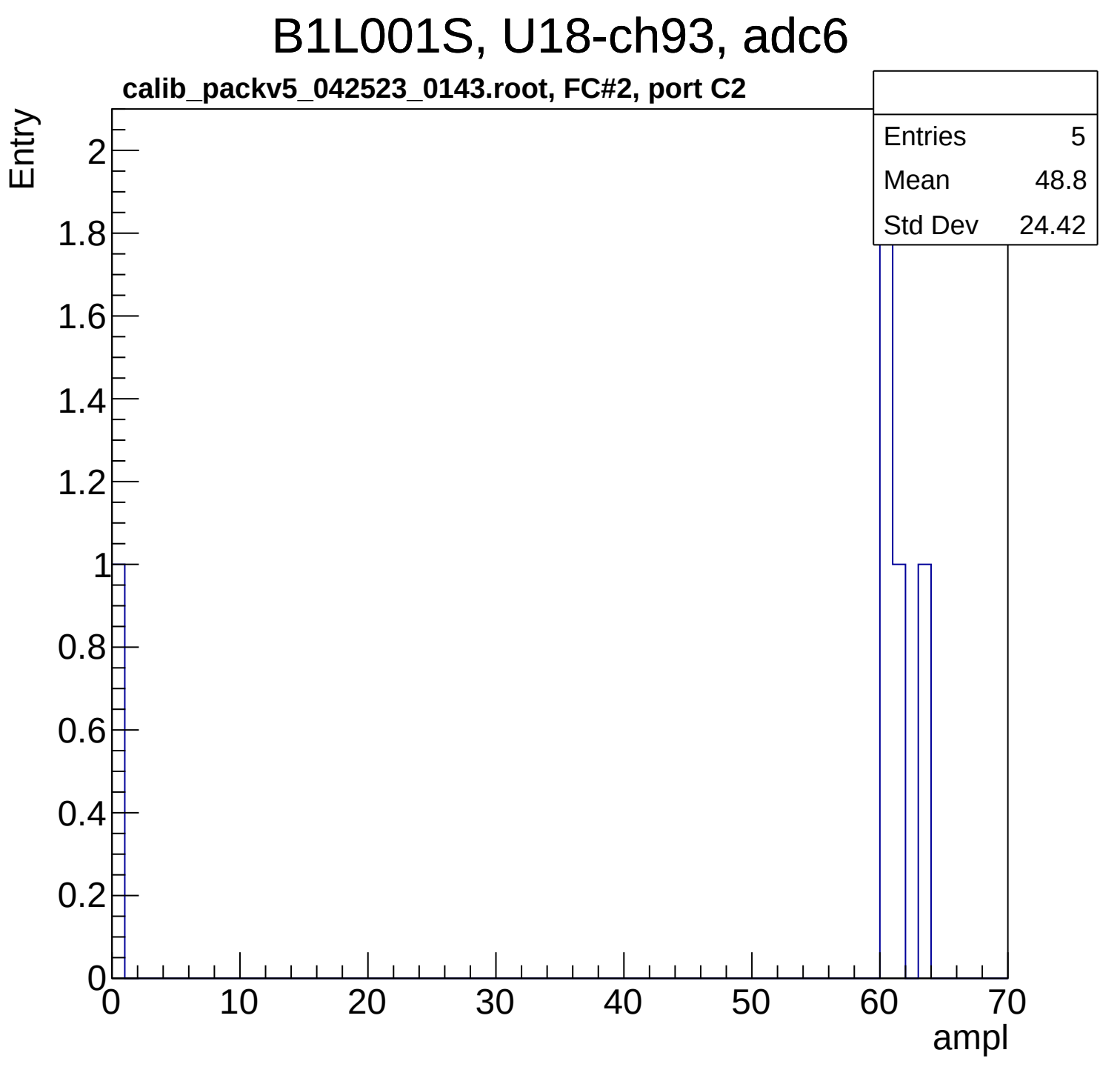

B1L001S, U18-ch93, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 145
Mean 37.85
Std Dev 3.409
Gaus mean : 38.4292
Gaus Width: 3.7571
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

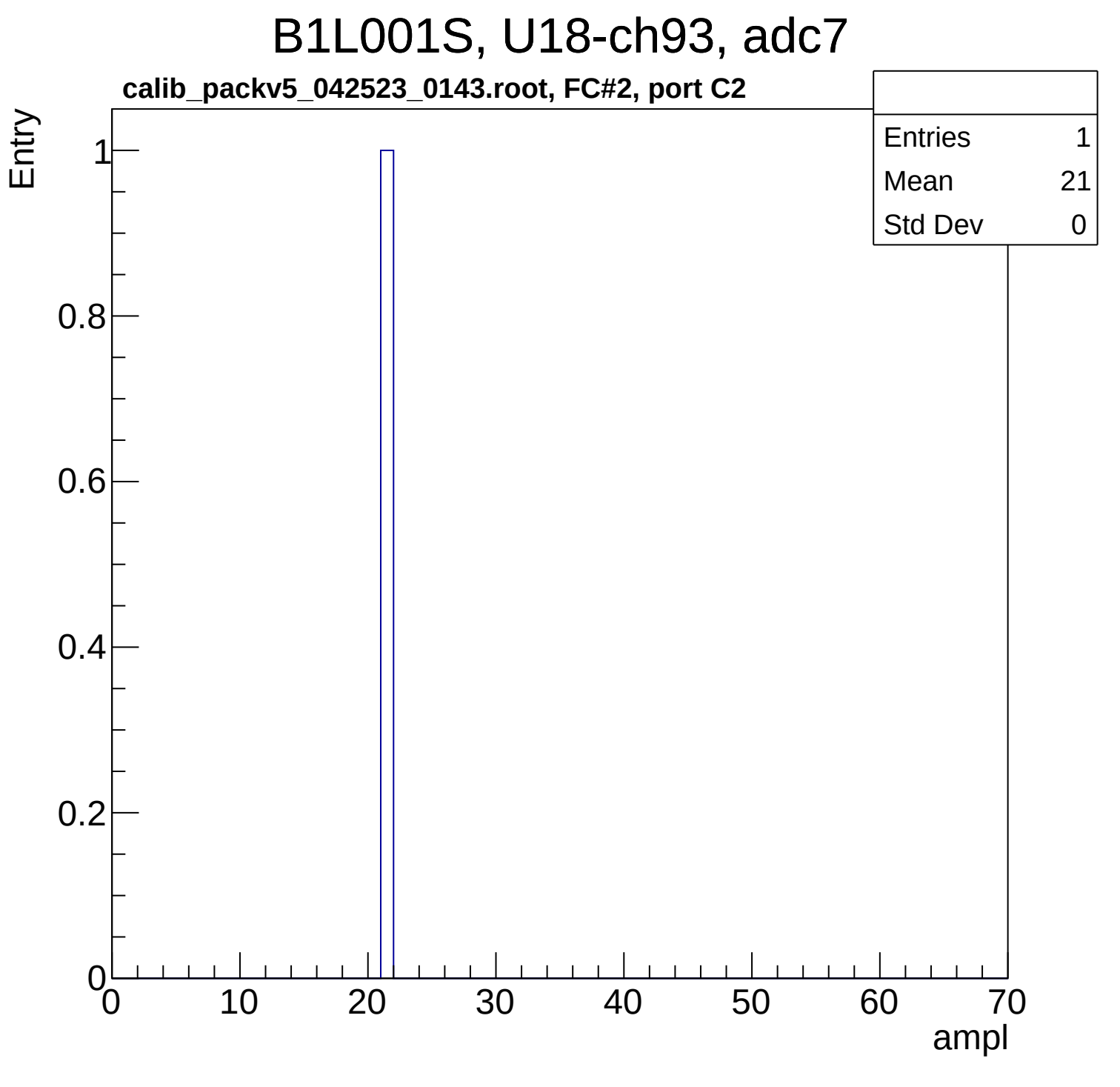

B1L001S, U18-ch93, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 129
Mean 44.89
Std Dev 3.267
Gaus mean : 45.6118
Gaus Width: 3.4493
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

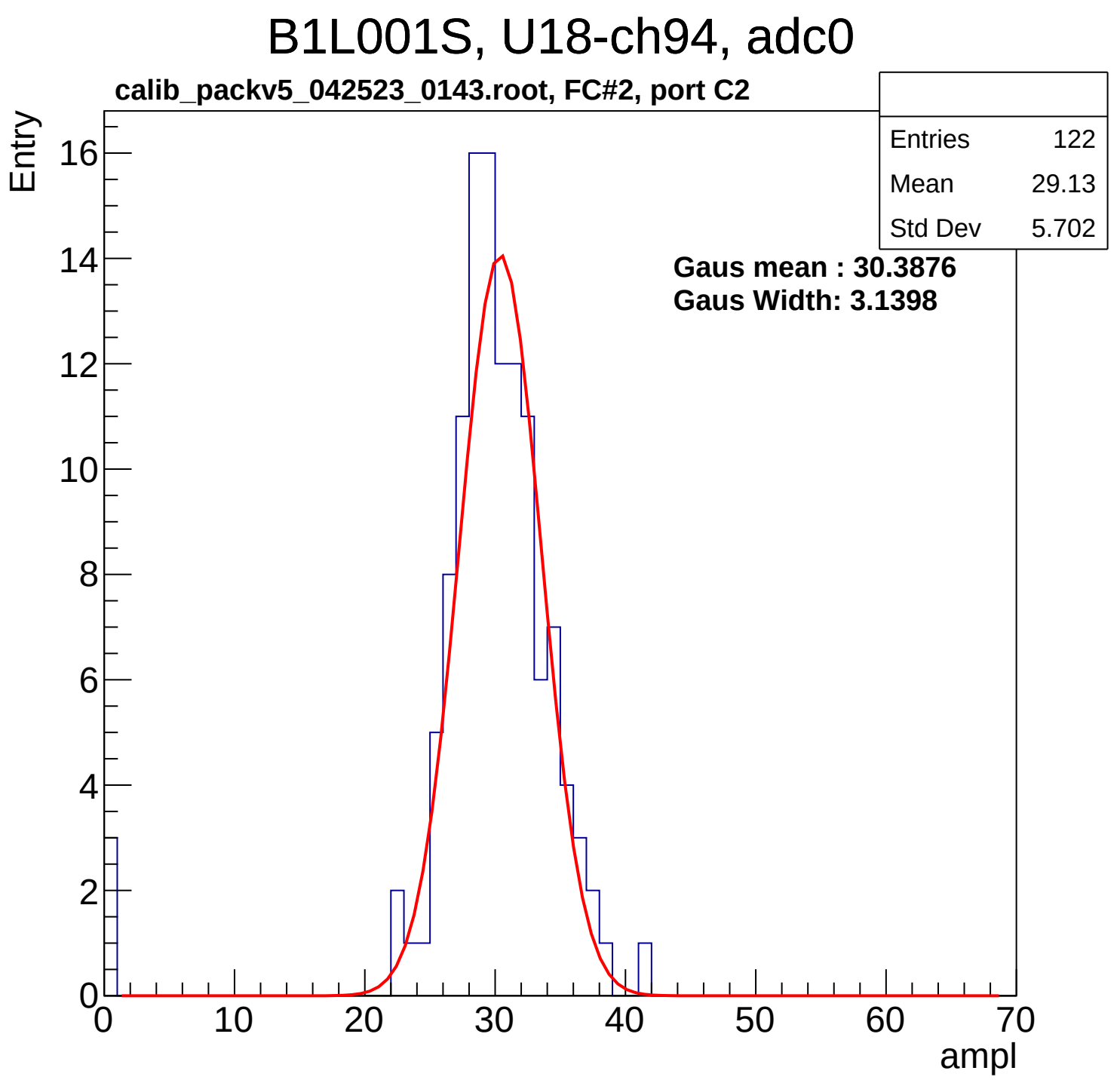

B1L001S, U18-ch93, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 116
Mean 51.04
Std Dev 3.539
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

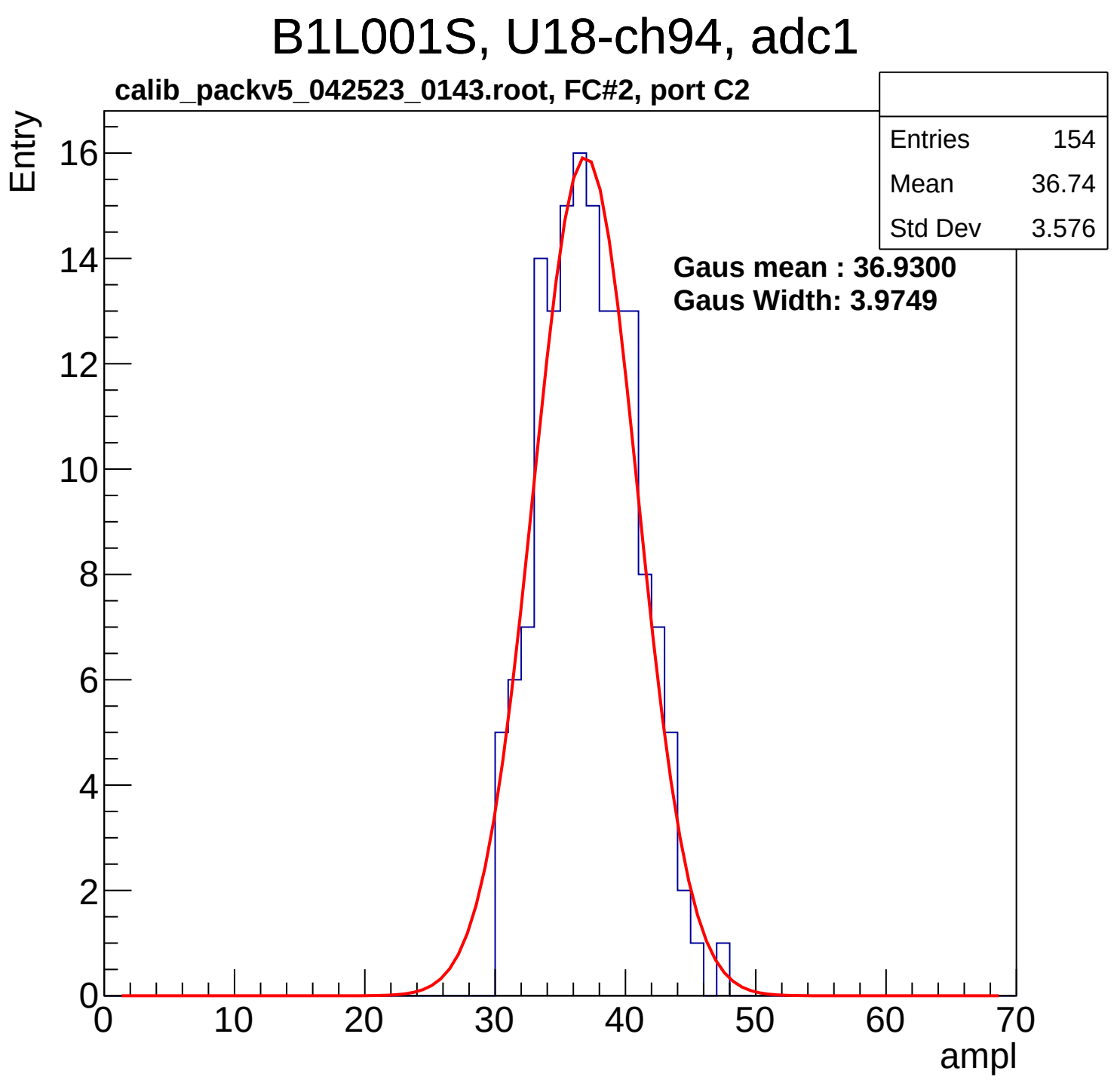

B1L001S, U18-ch93, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 112
Mean 56.27
Std Dev 3.154
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

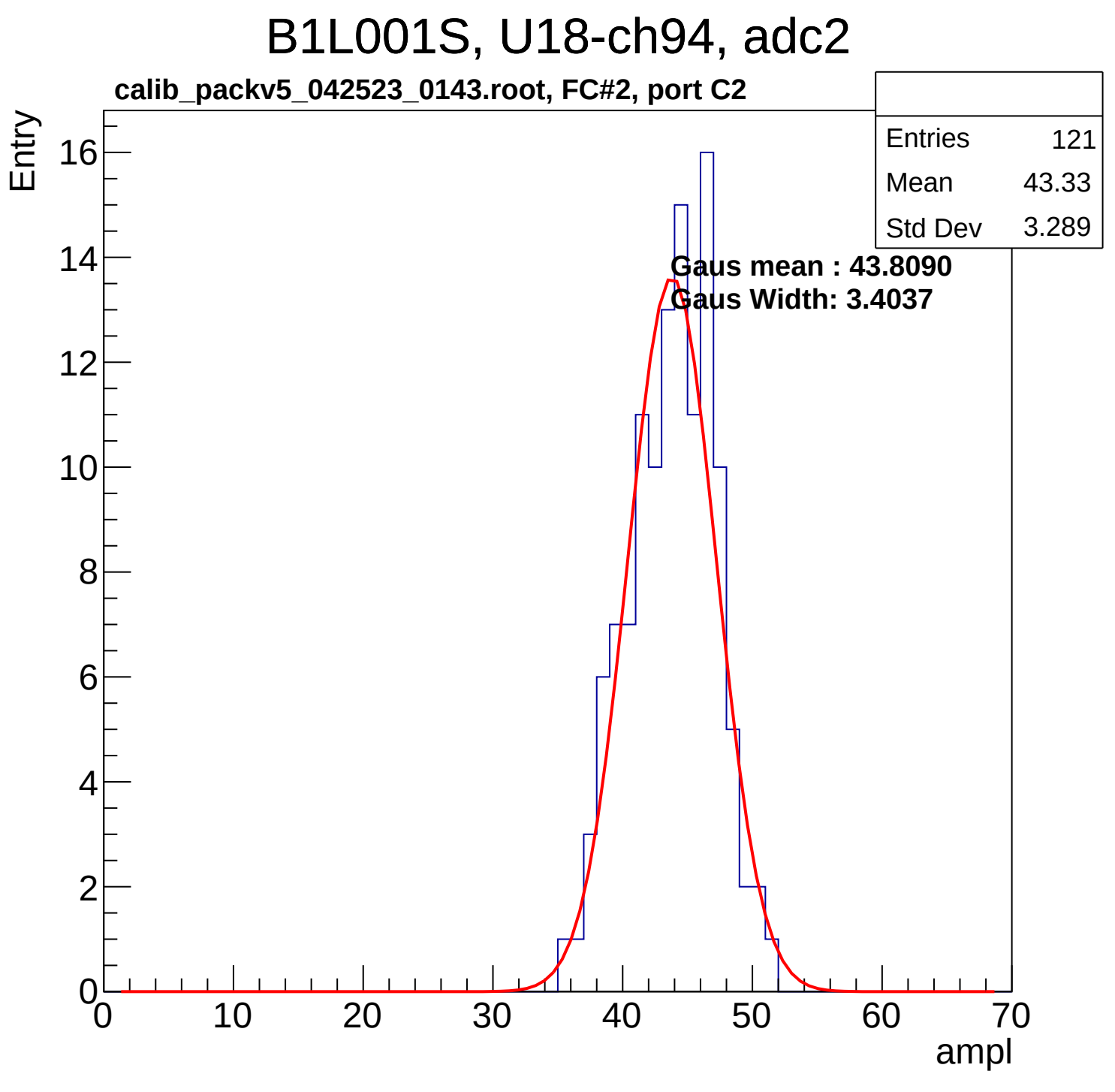

B1L001S, U18-ch93, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 79
Mean 59.89
Std Dev 7.121
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

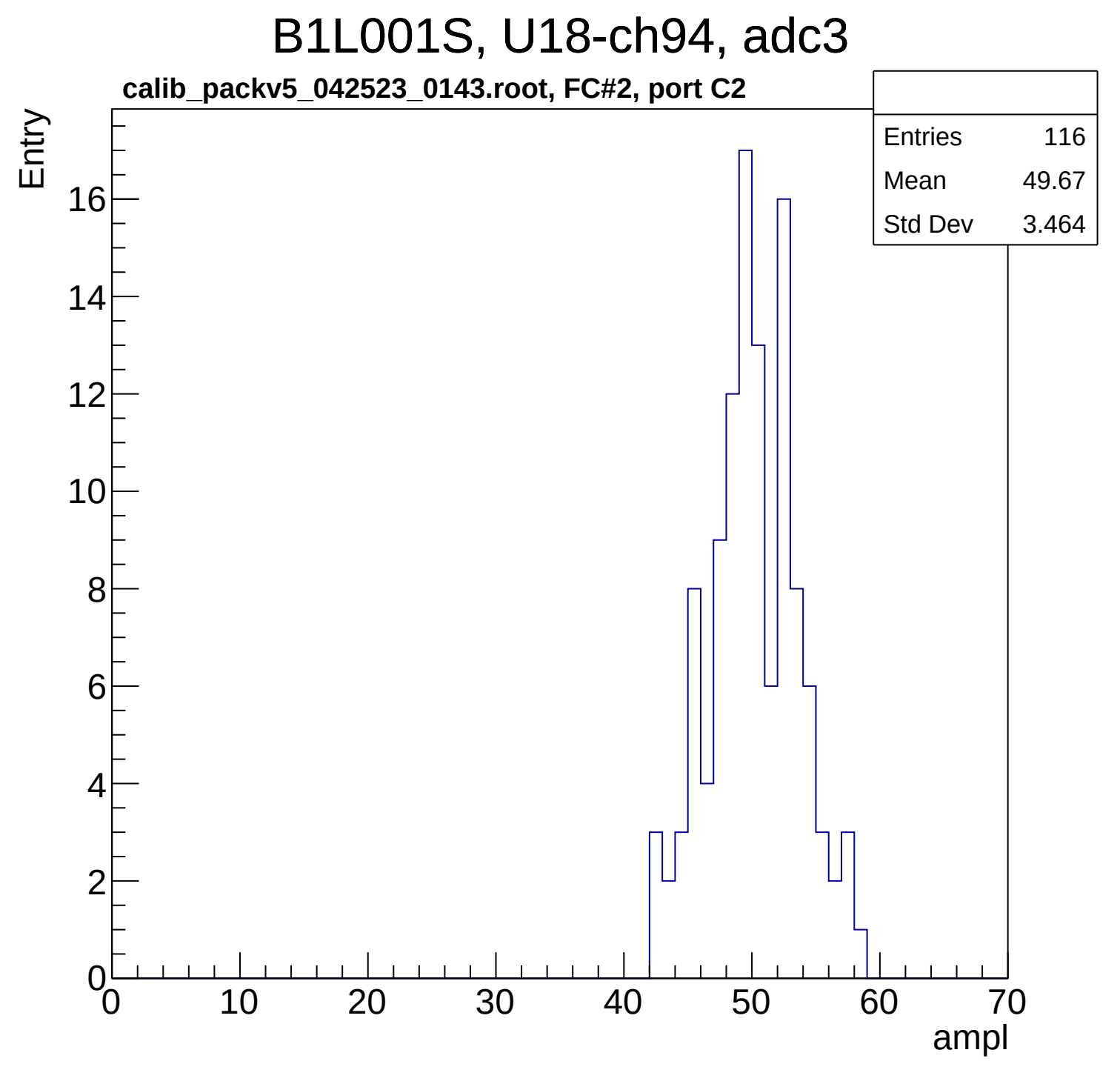

B1L001S, U18-ch93, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 5
Mean 48.8
Std Dev 24.42
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

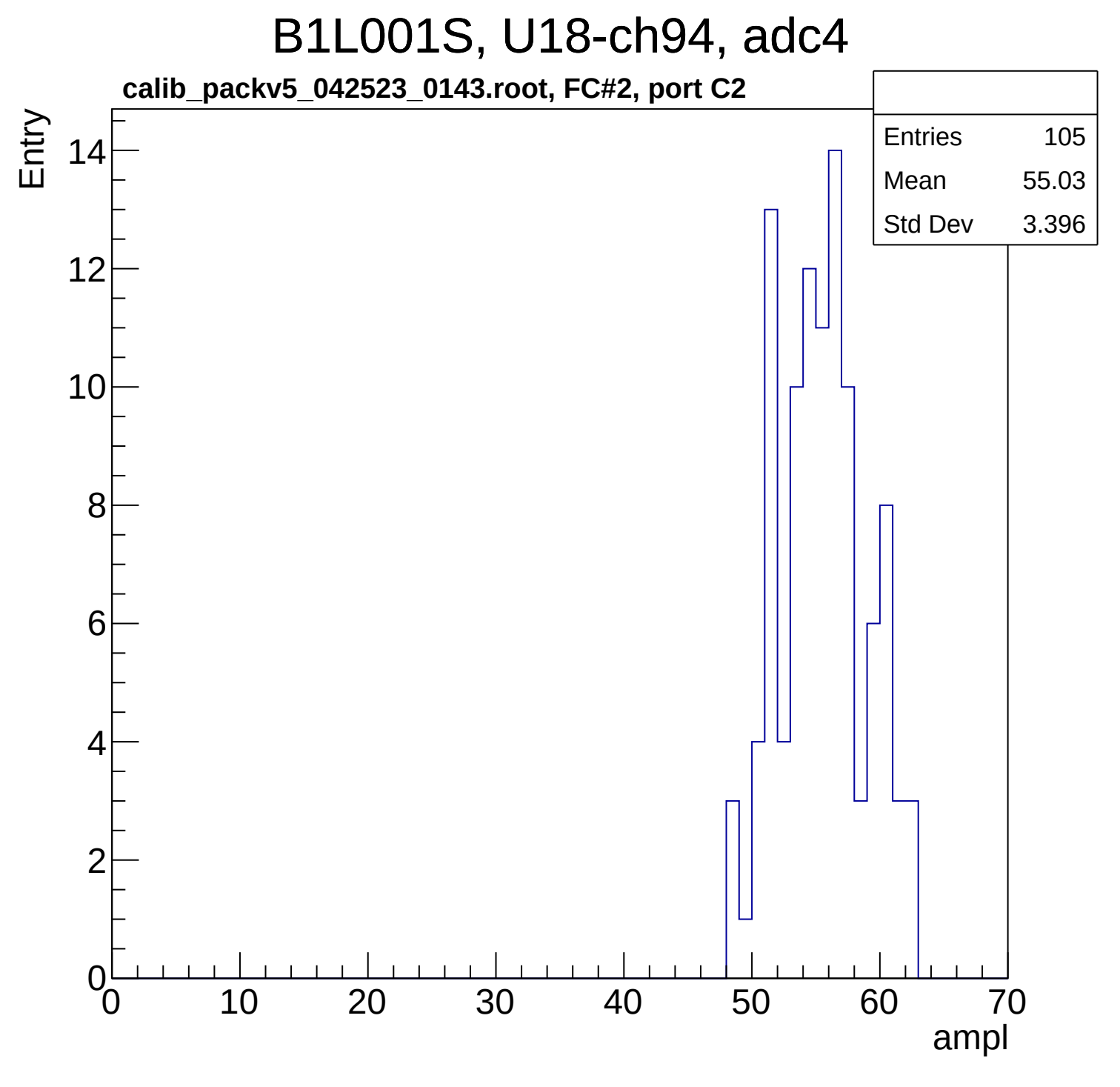

B1L001S, U18-ch93, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 21
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

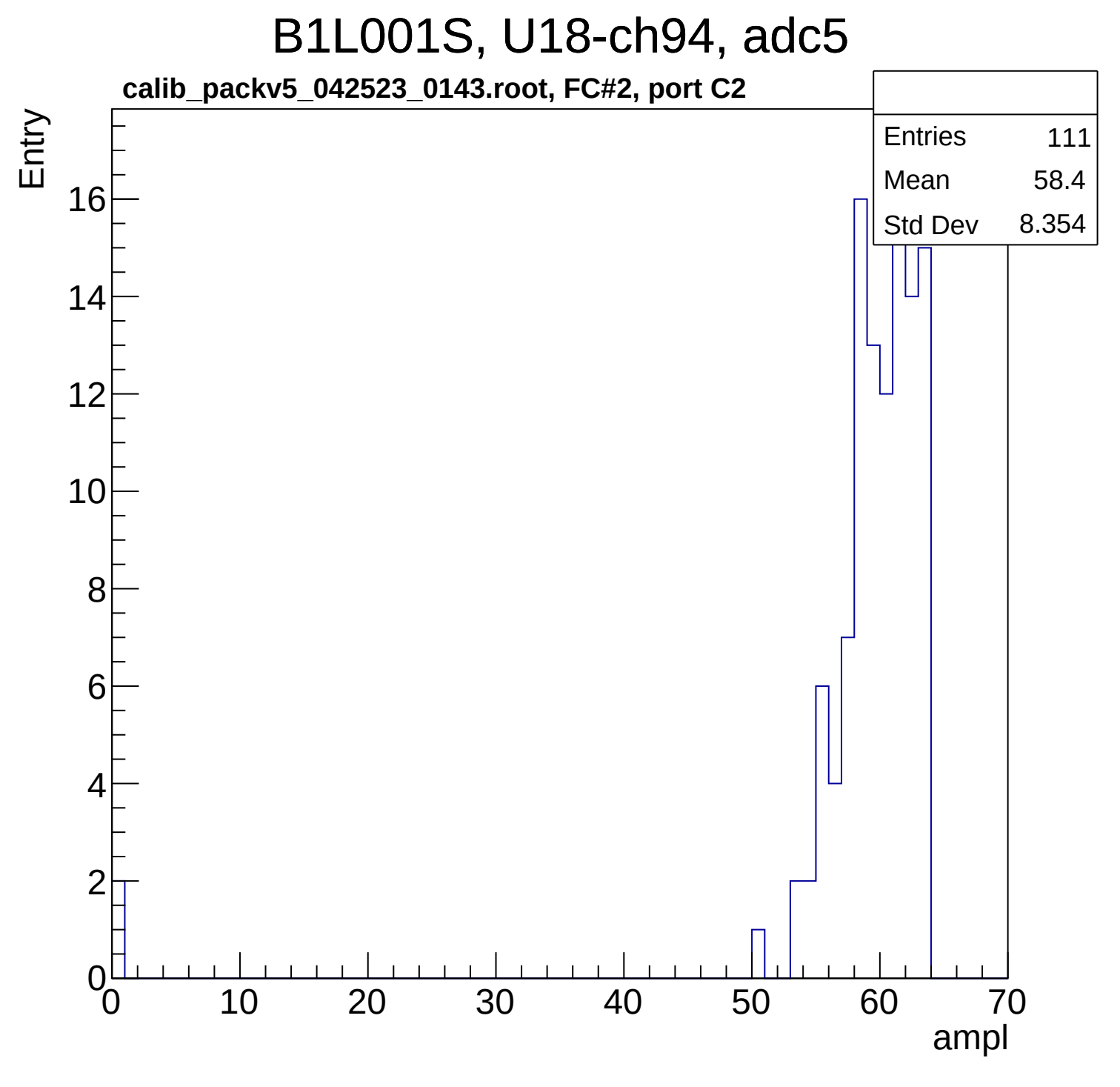

B1L001S, U18-ch94, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 122
Mean 29.13
Std Dev 5.702
Gaus mean : 30.3876
Gaus Width: 3.1398
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

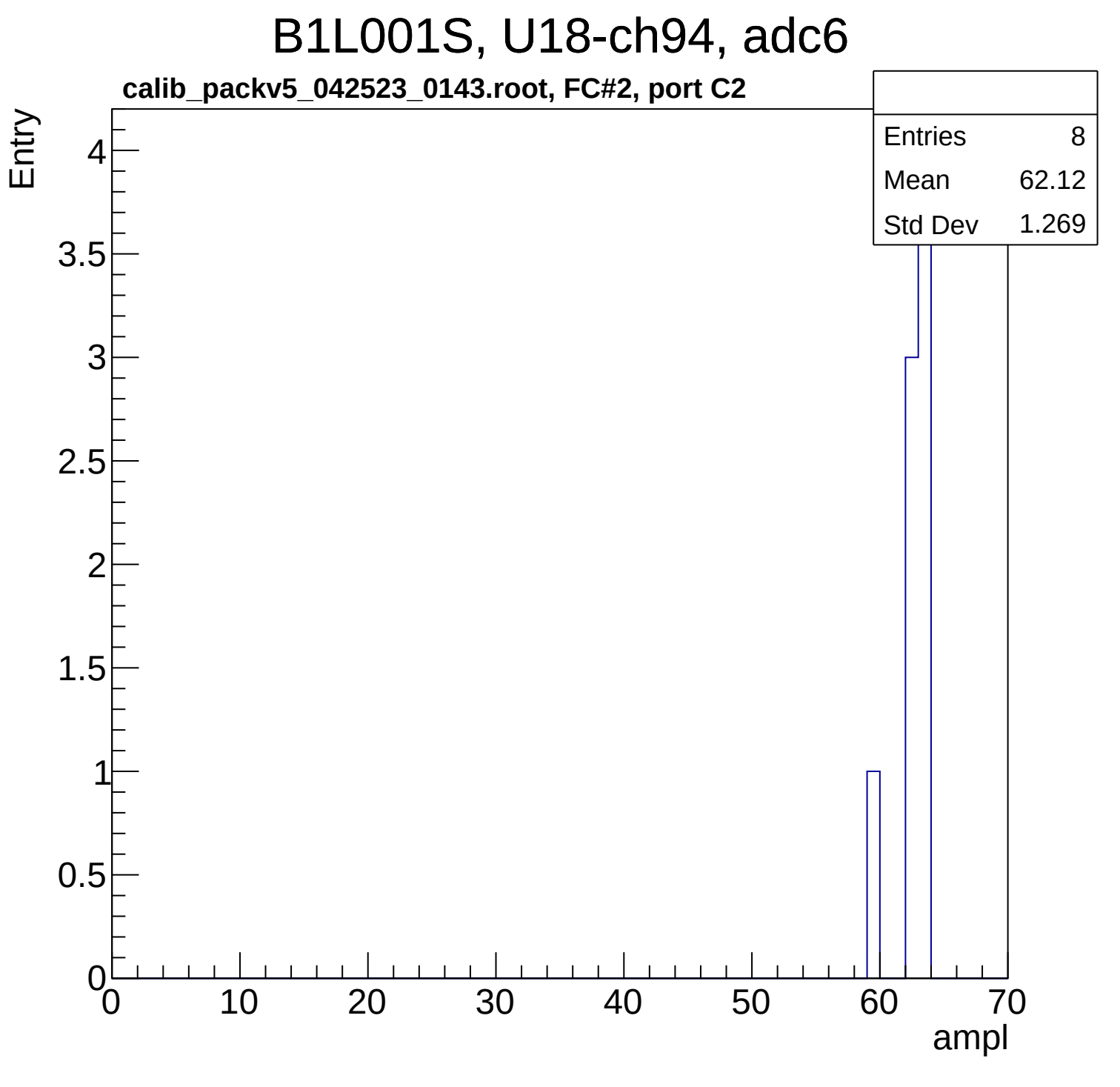

B1L001S, U18-ch94, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 154
Mean 36.74
Std Dev 3.576
Gaus mean : 36.9300
Gaus Width: 3.9749
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

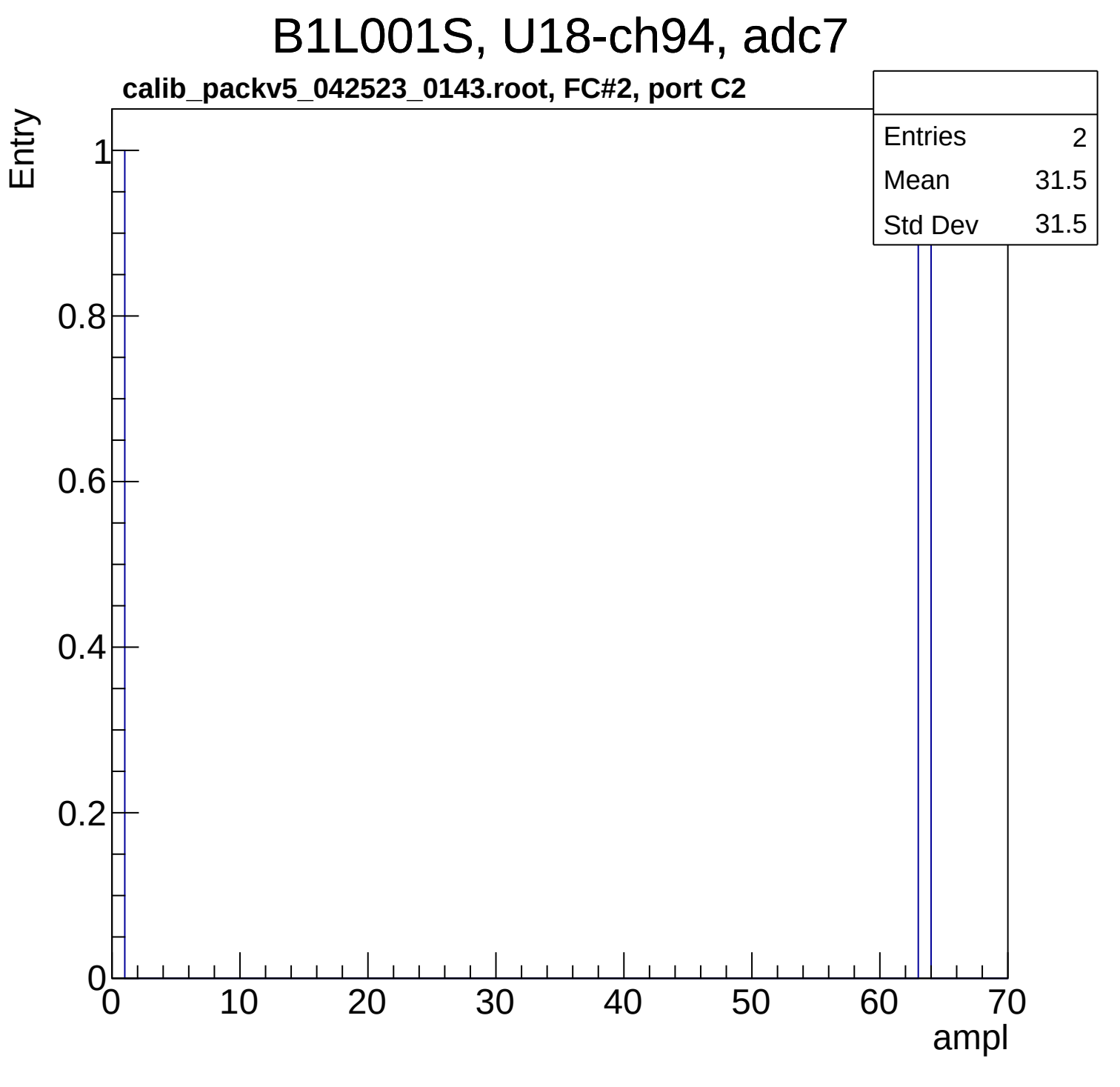

B1L001S, U18-ch94, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 121
Mean 43.33
Std Dev 3.289
Gaus mean : 43.8090
Gaus Width: 3.4037
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

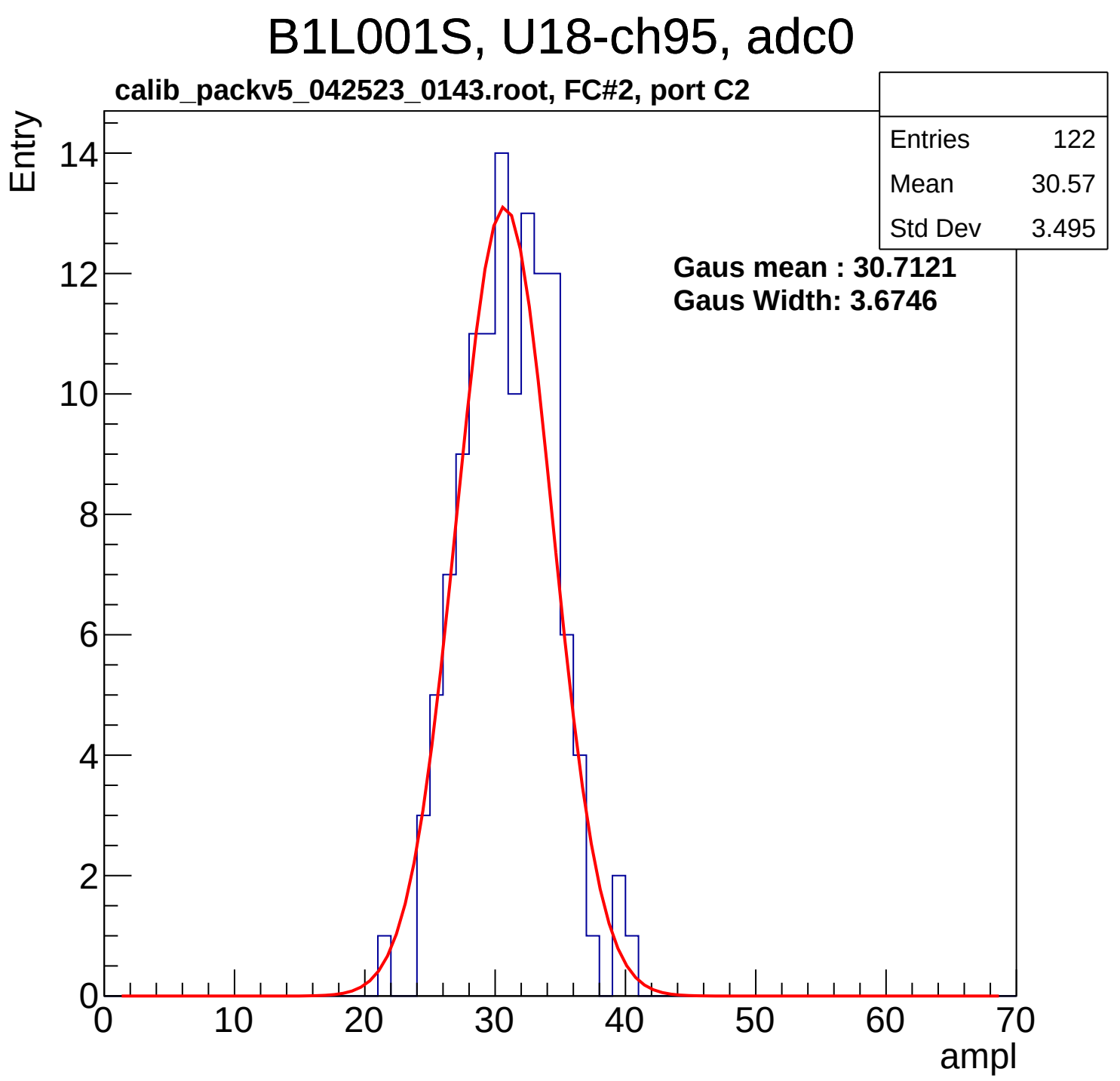

B1L001S, U18-ch94, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 116
Mean 49.67
Std Dev 3.464
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

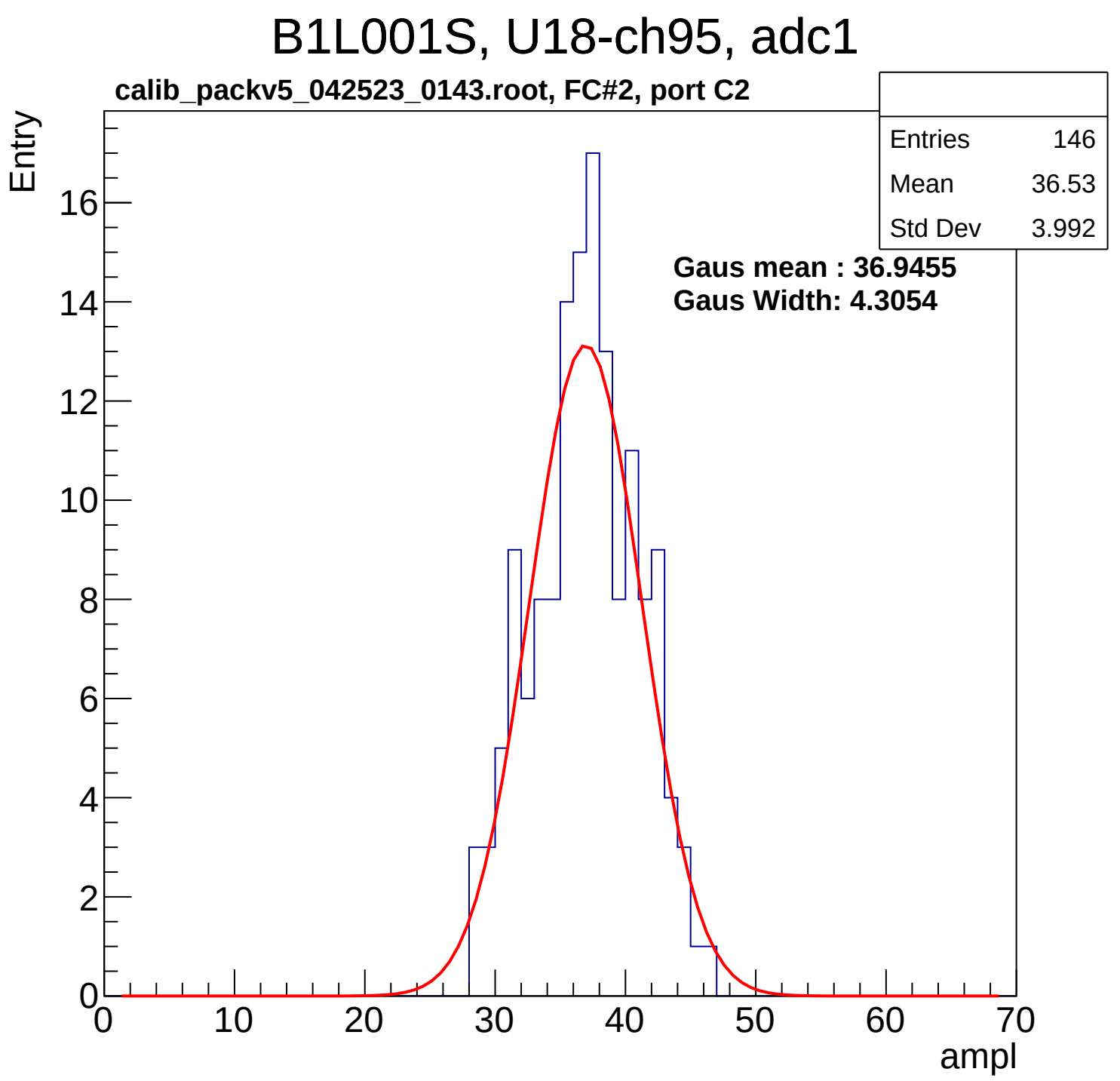

B1L001S, U18-ch94, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 105
Mean 55.03
Std Dev 3.396
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

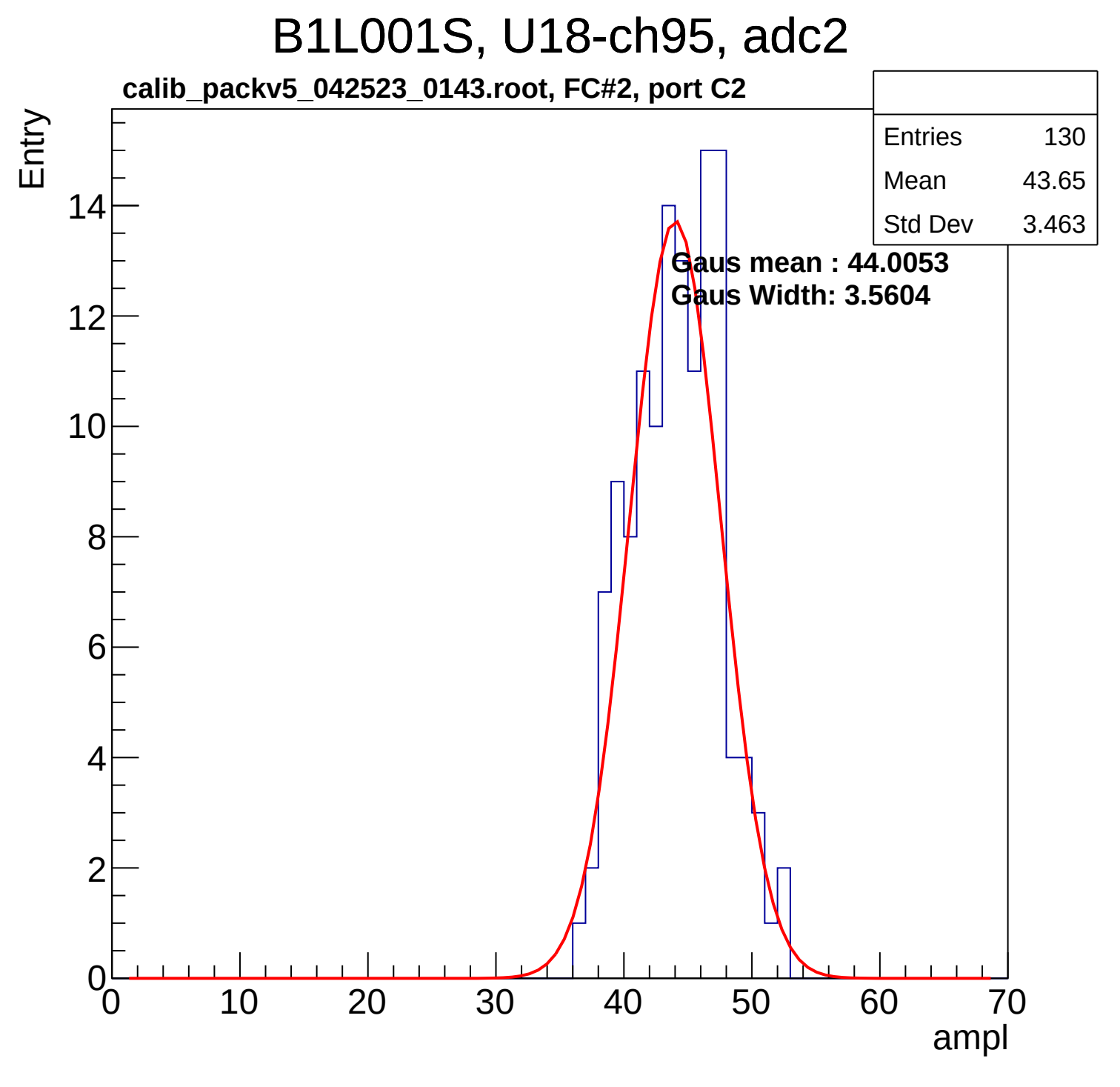

B1L001S, U18-ch94, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 111
Mean 58.4
Std Dev 8.354
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

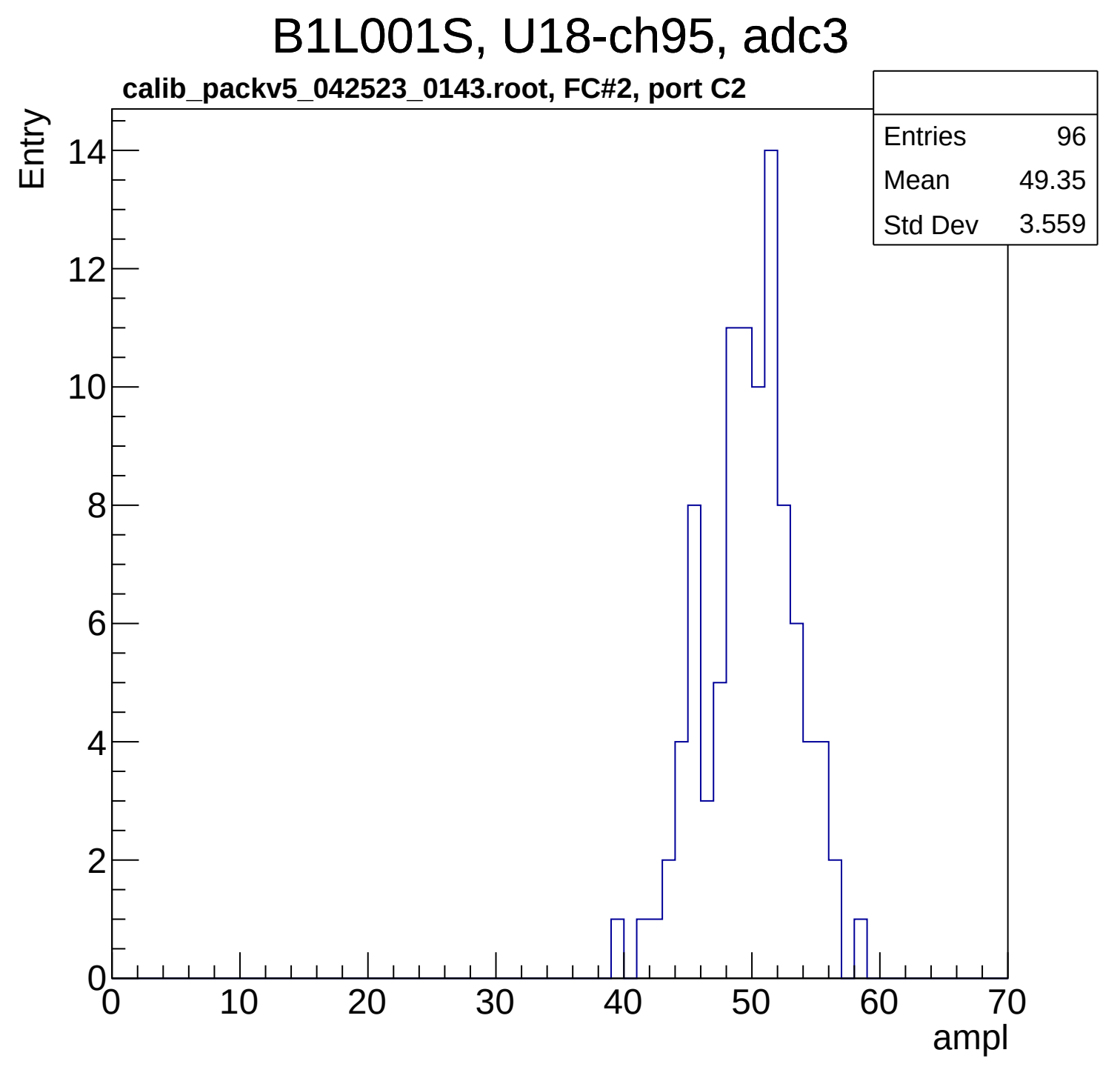

B1L001S, U18-ch94, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 8
Mean 62.12
Std Dev 1.269
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

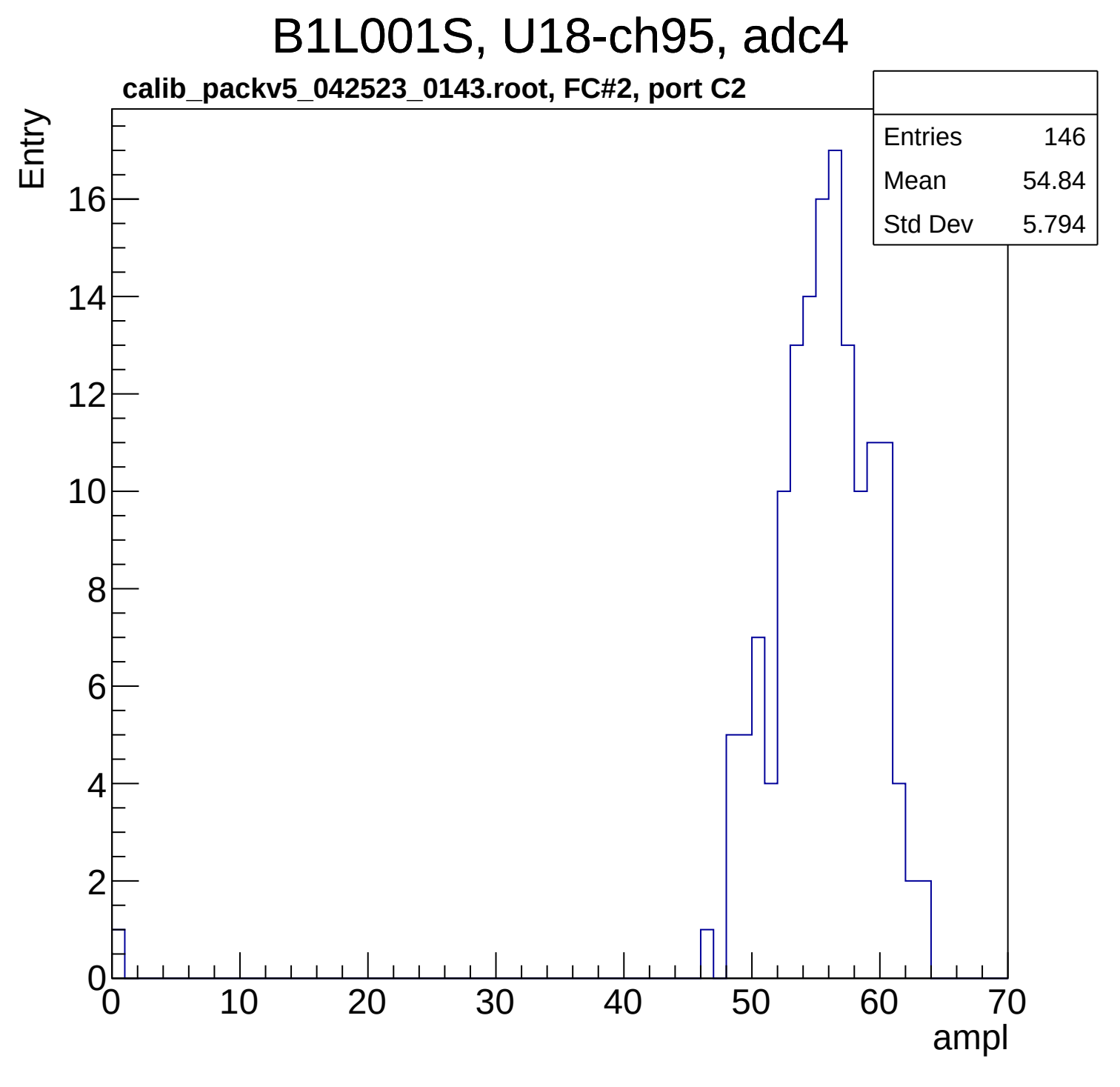

B1L001S, U18-ch94, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 31.5
Std Dev 31.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

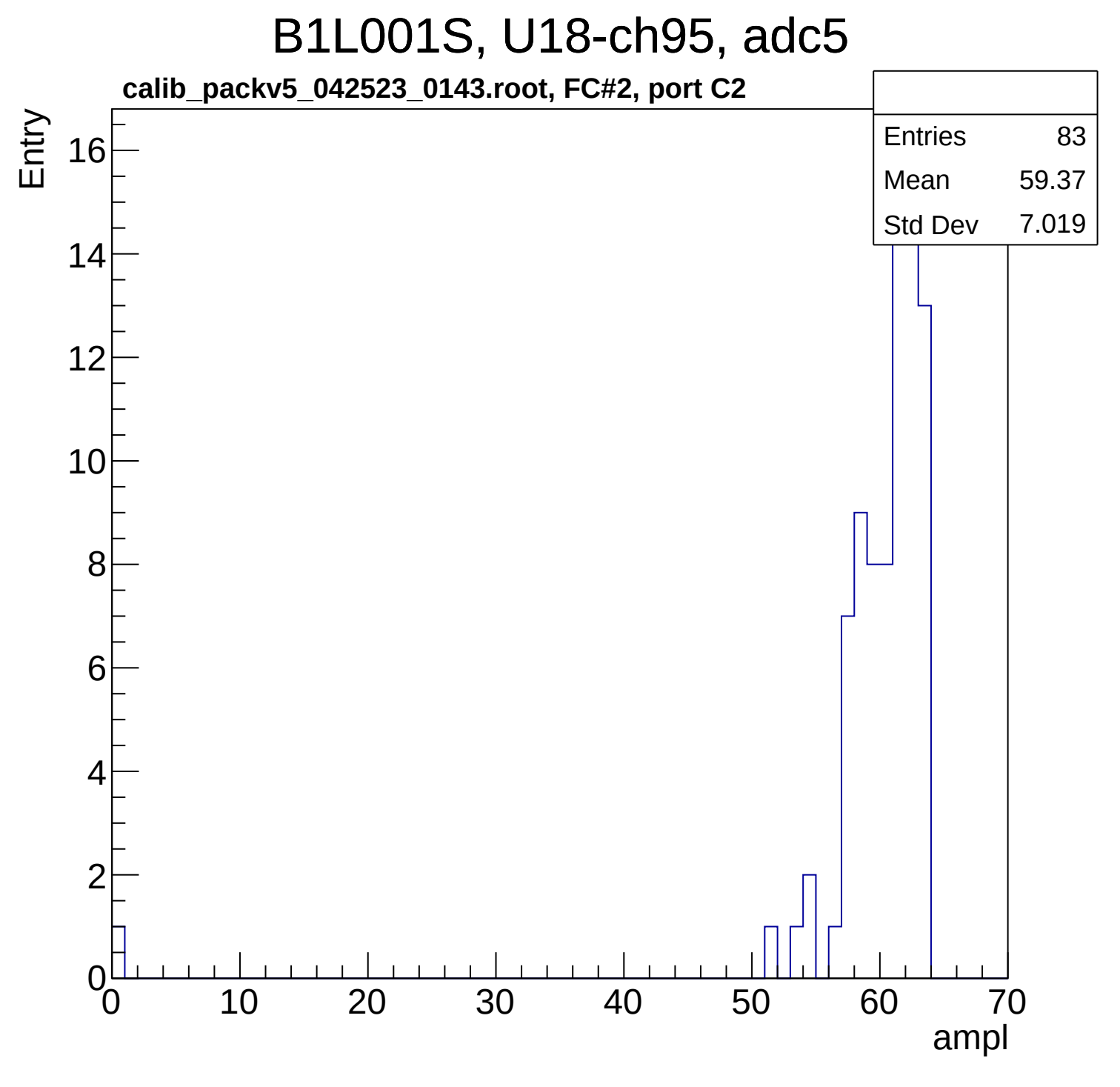

B1L001S, U18-ch95, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 122
Mean 30.57
Std Dev 3.495
Gaus mean : 30.7121
Gaus Width: 3.6746
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

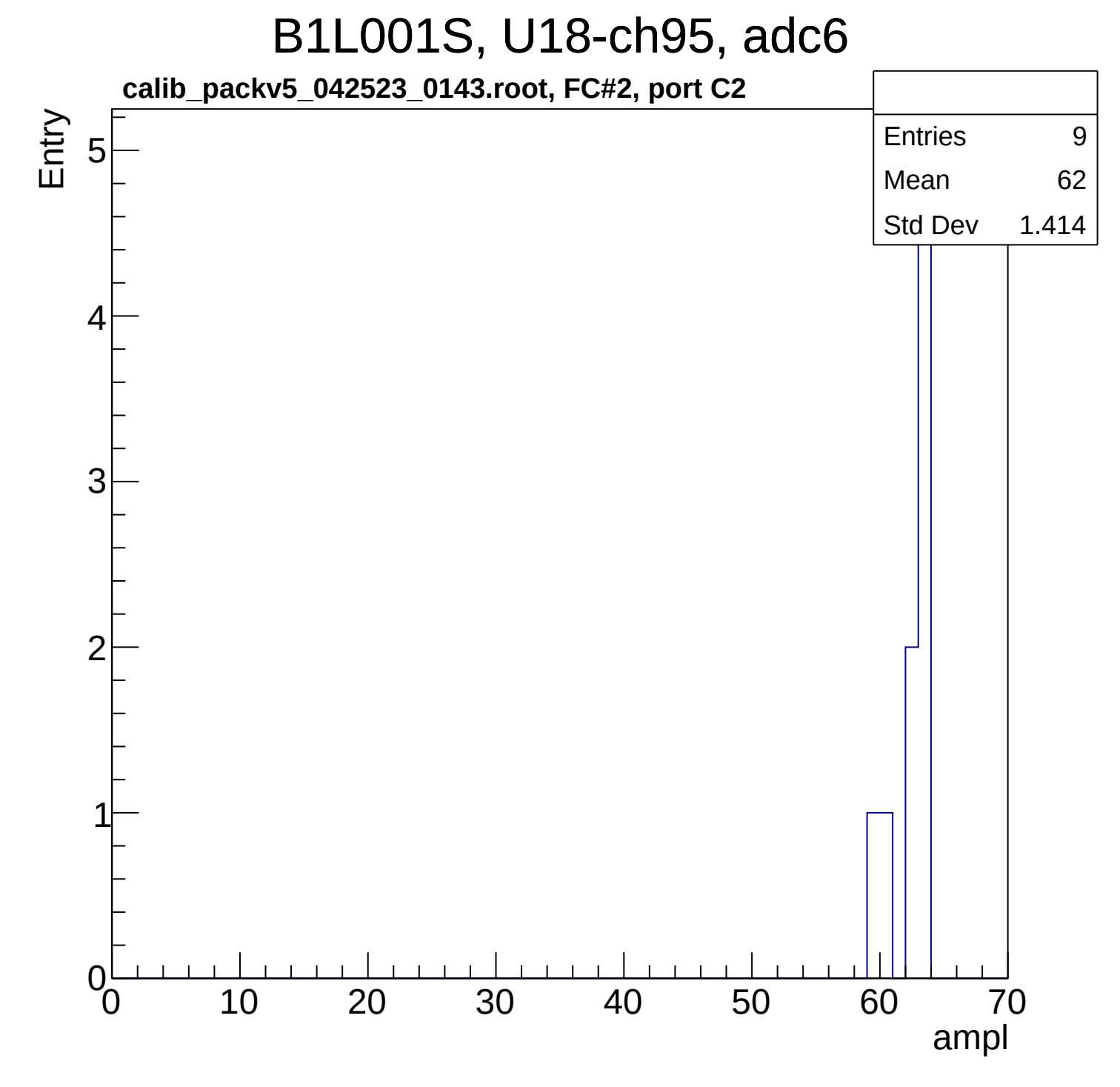

B1L001S, U18-ch95, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 146
Mean 36.53
Std Dev 3.992
Gaus mean : 36.9455
Gaus Width: 4.3054
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

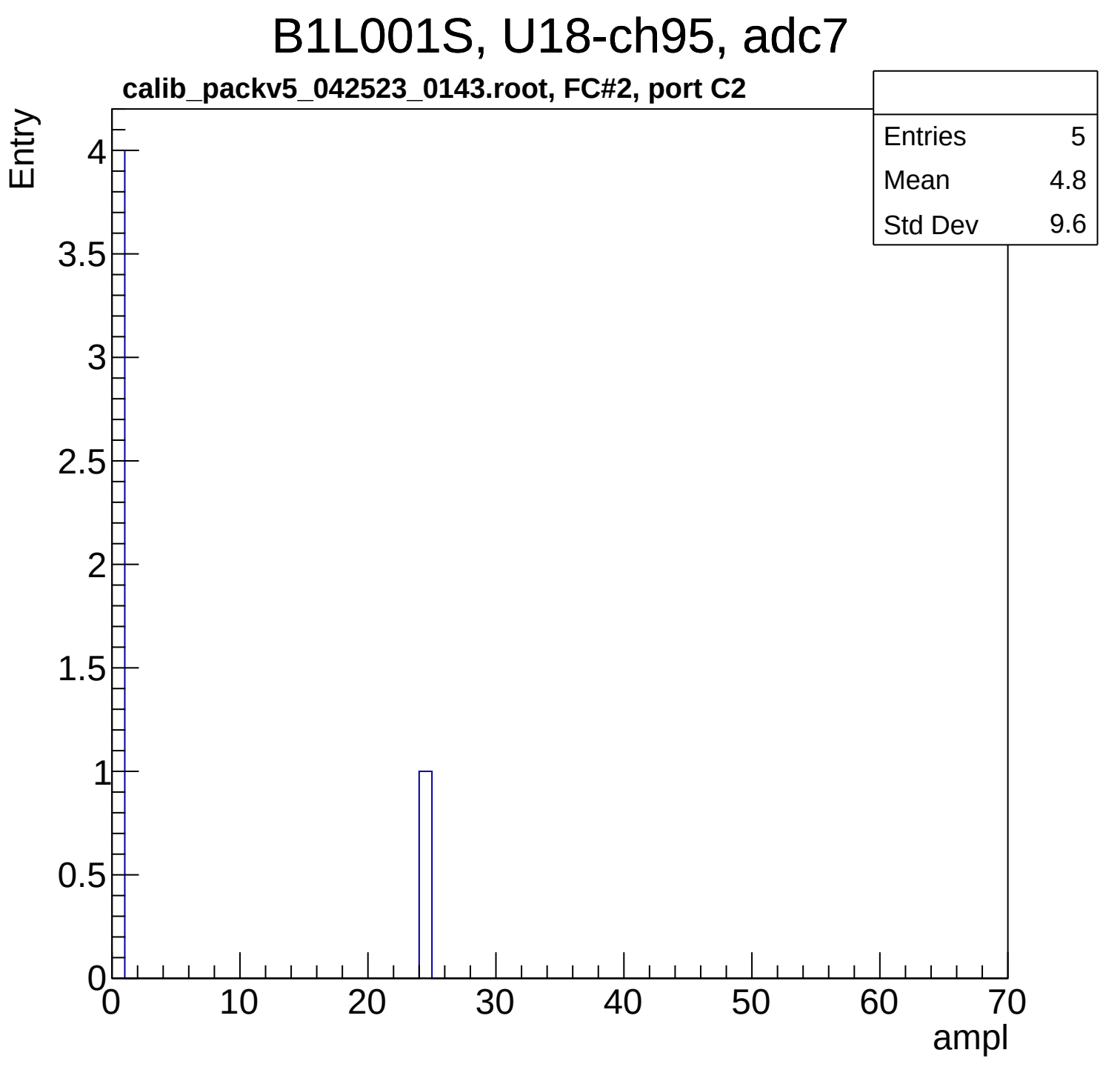

B1L001S, U18-ch95, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 130
Mean 43.65
Std Dev 3.463
Gaus mean : 44.0053
Gaus Width: 3.5604
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

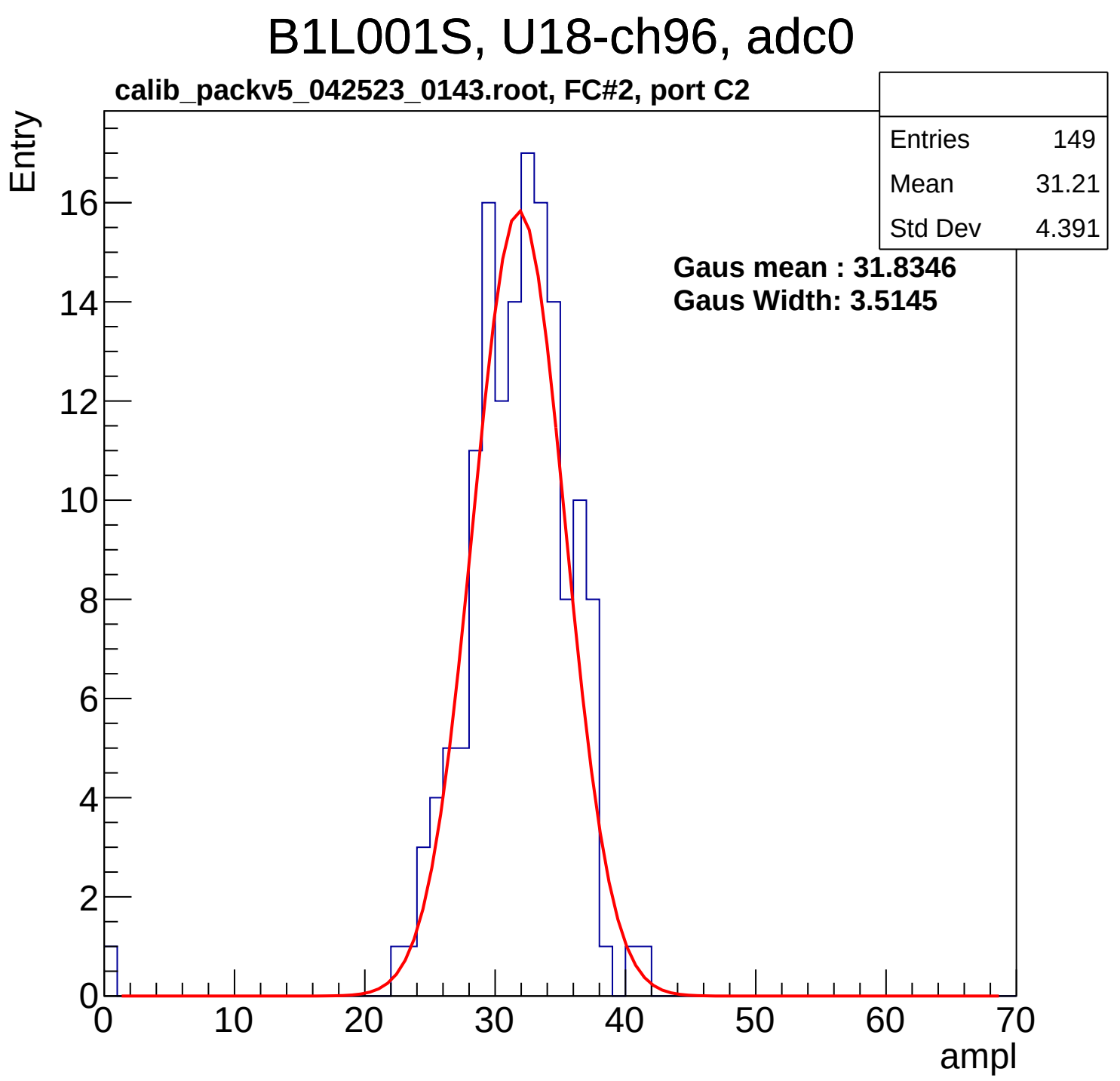

B1L001S, U18-ch95, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 96
Mean 49.35
Std Dev 3.559
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

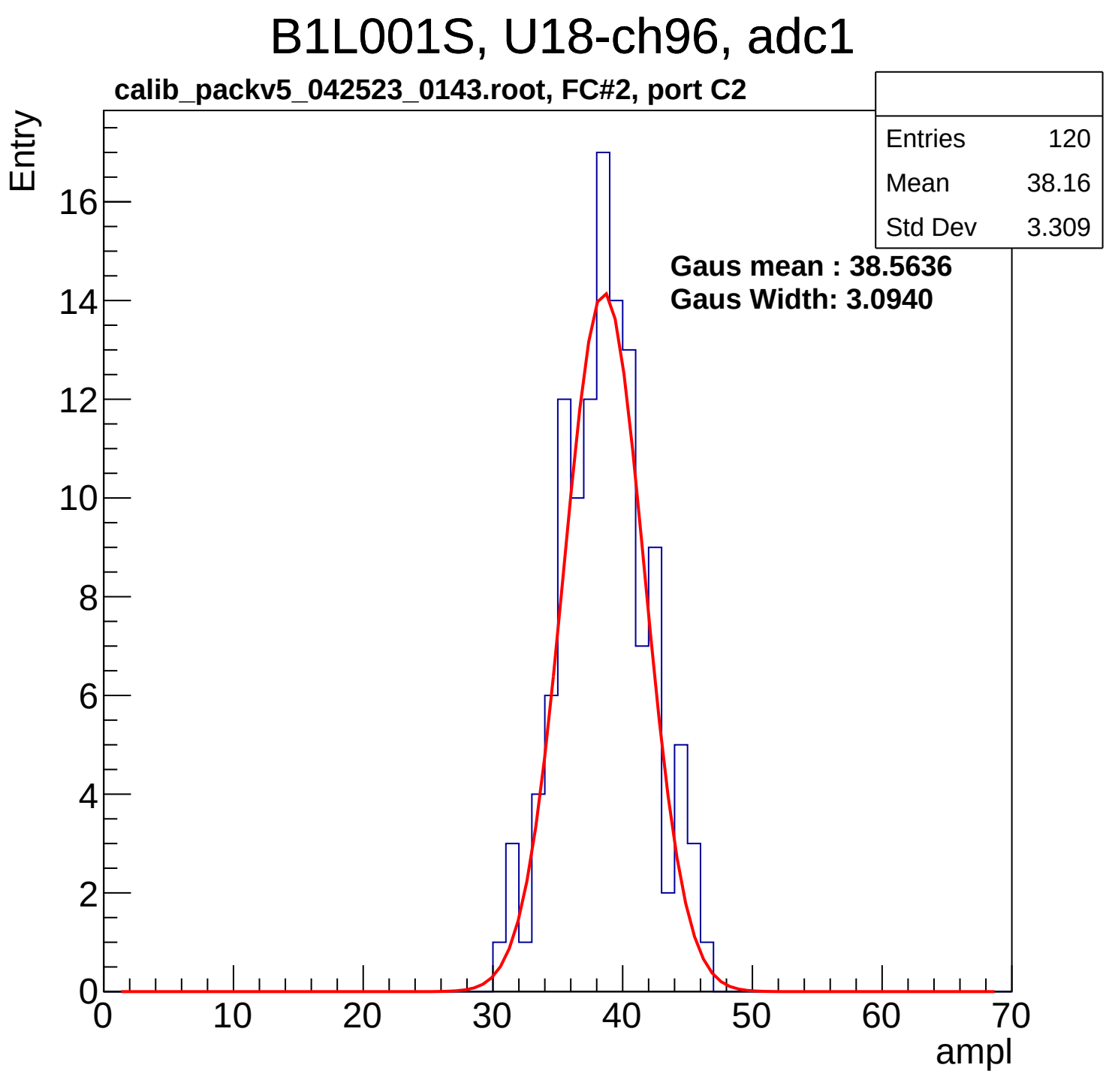

B1L001S, U18-ch95, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 146
Mean 54.84
Std Dev 5.794
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

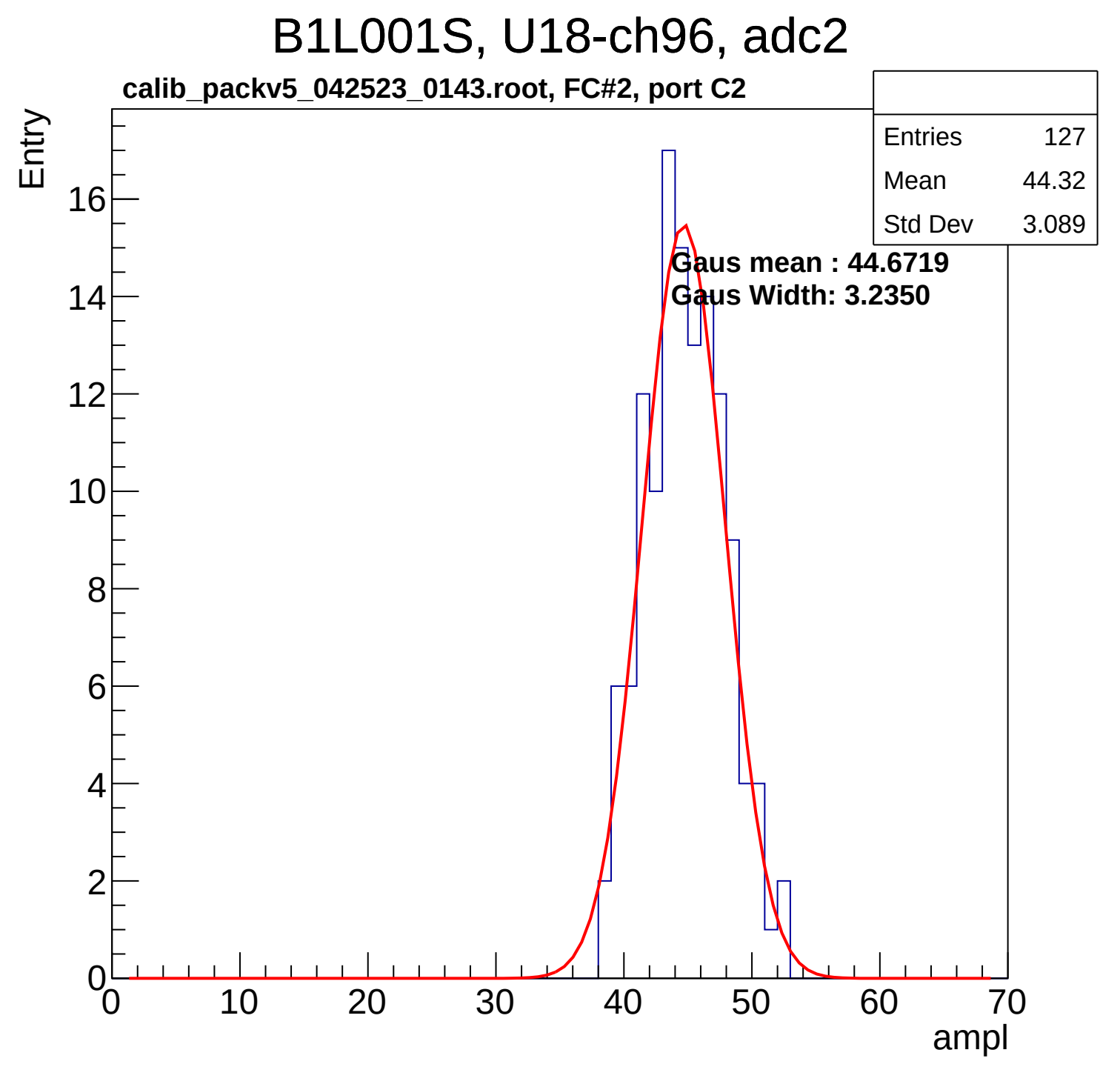

B1L001S, U18-ch95, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 83
Mean 59.37
Std Dev 7.019
Entry
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl

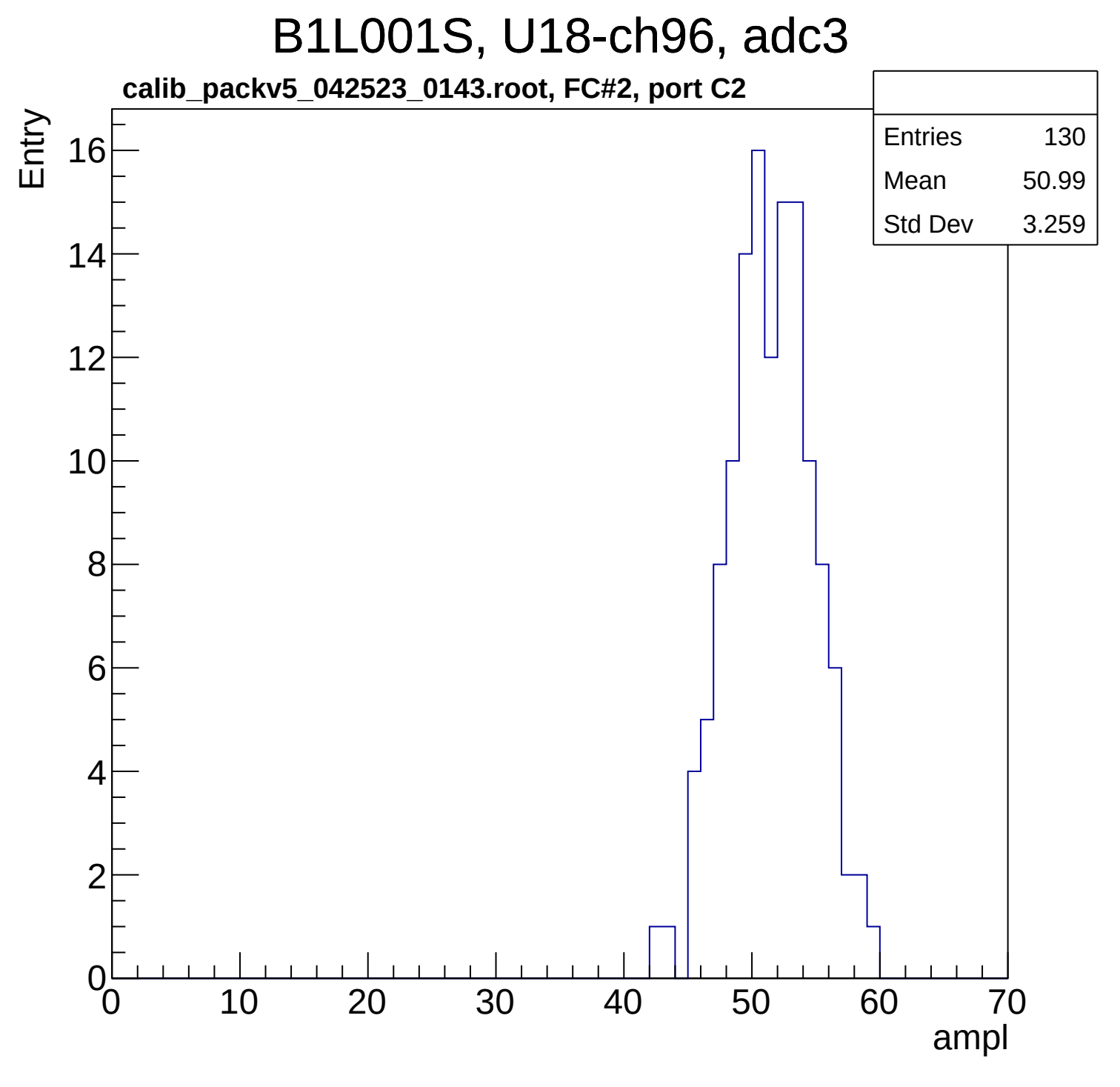

B1L001S, U18-ch95, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 9
Mean 62
Std Dev 1.414
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

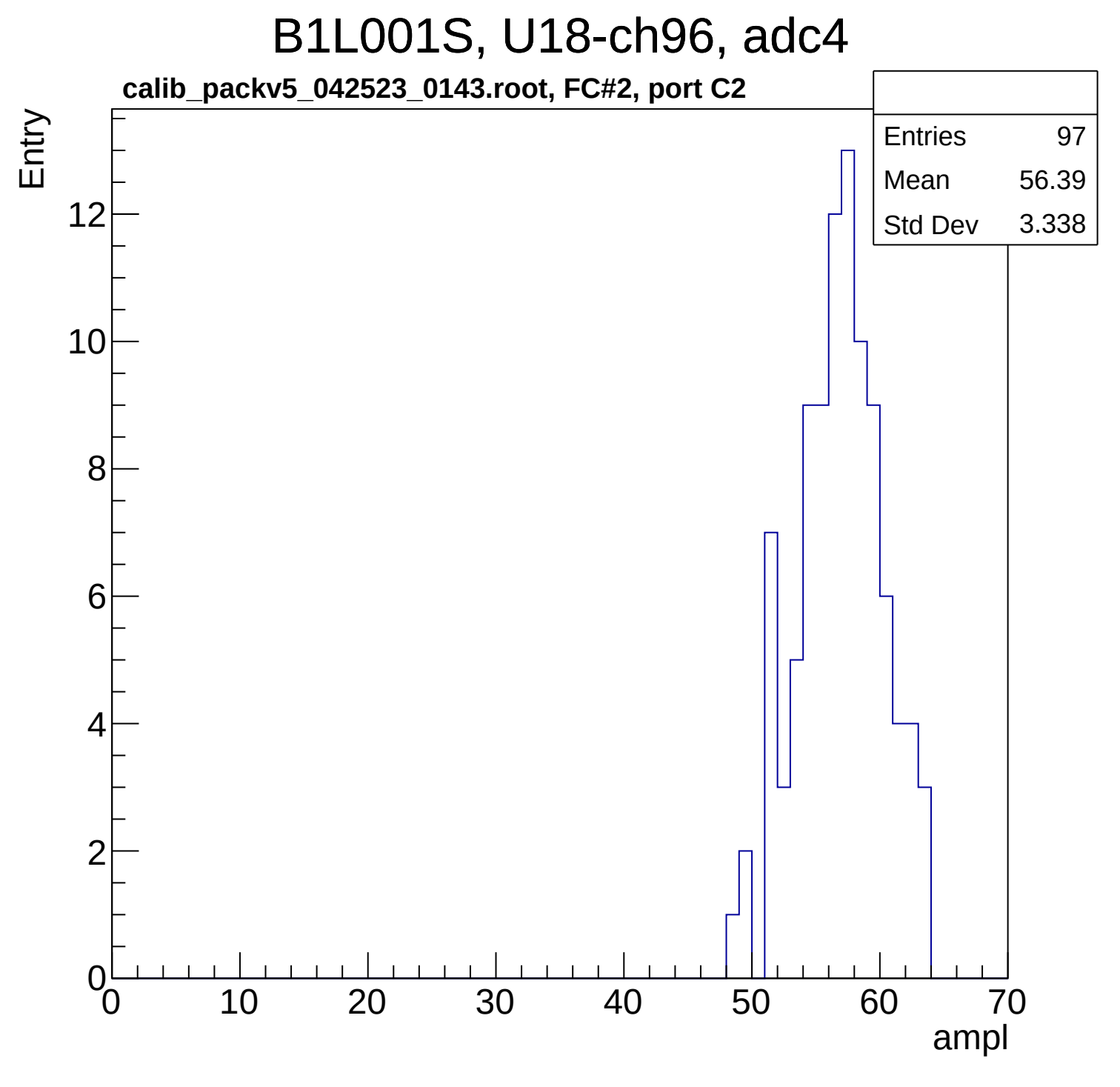

B1L001S, U18-ch95, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 5
Mean 4.8
Std Dev 9.6
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

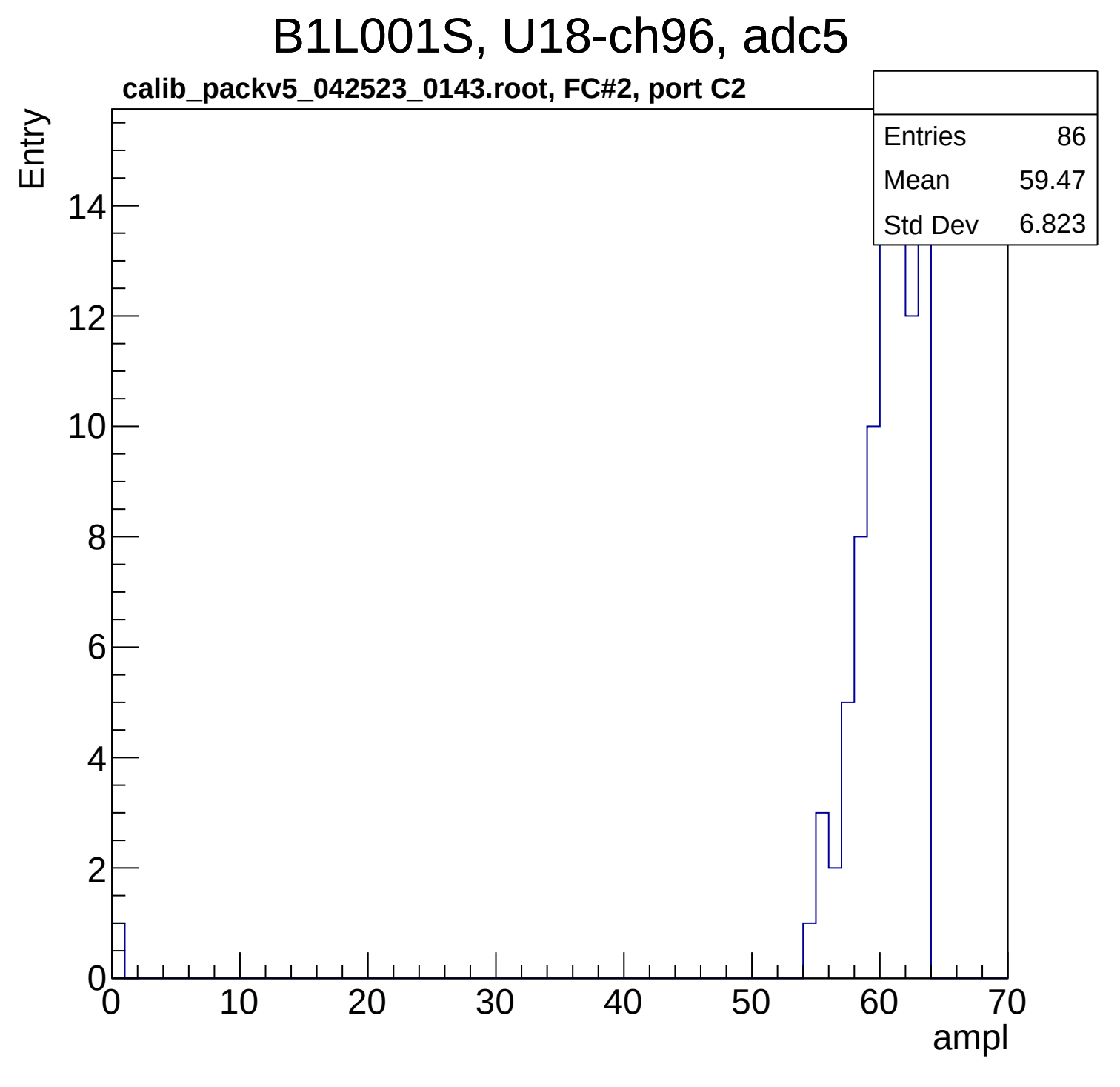

B1L001S, U18-ch96, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 149
Mean 31.21
Std Dev 4.391
Gaus mean : 31.8346
Gaus Width: 3.5145
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

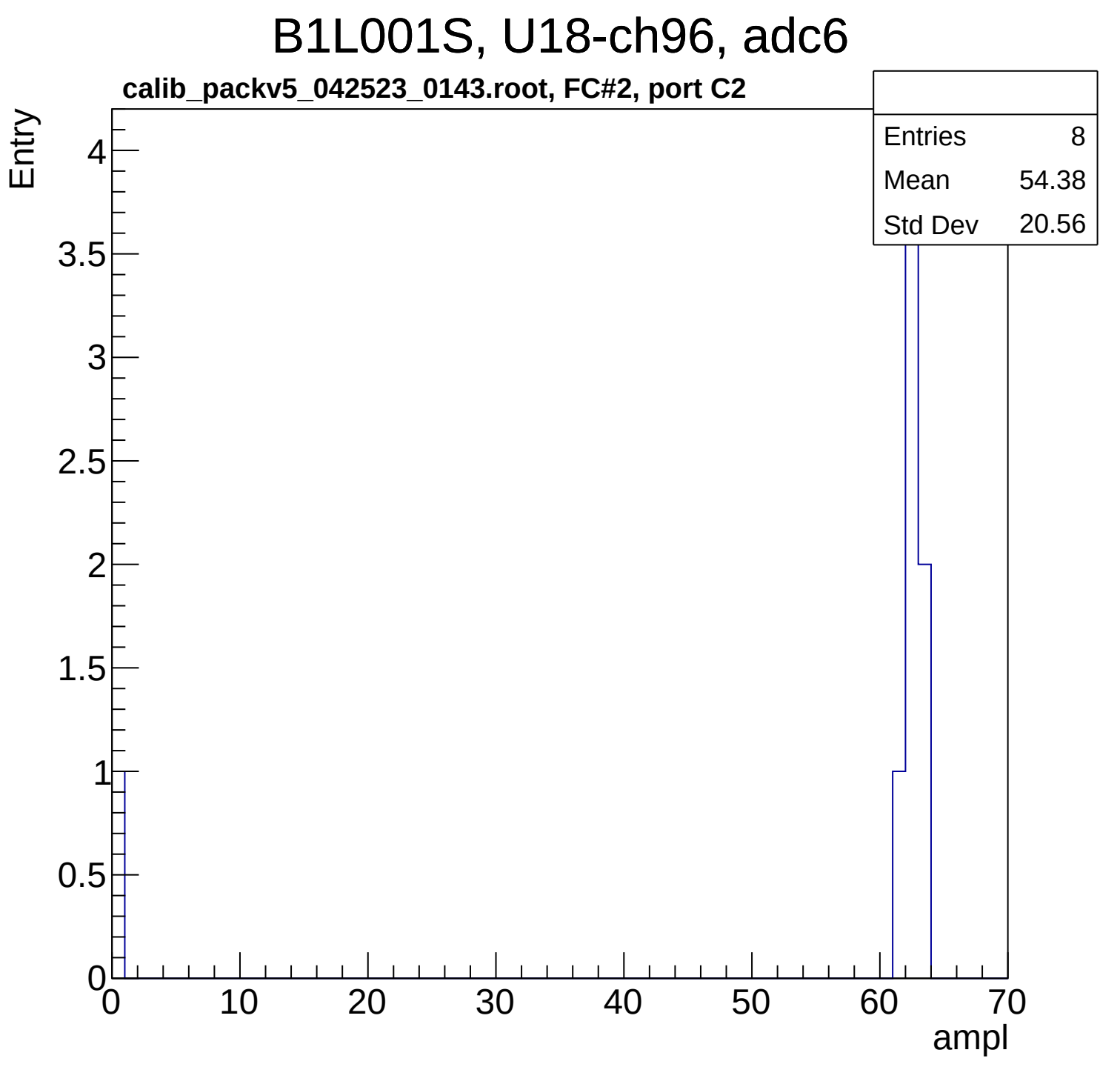

B1L001S, U18-ch96, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 120
Mean 38.16
Std Dev 3.309
Gaus mean : 38.5636
Gaus Width: 3.0940
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

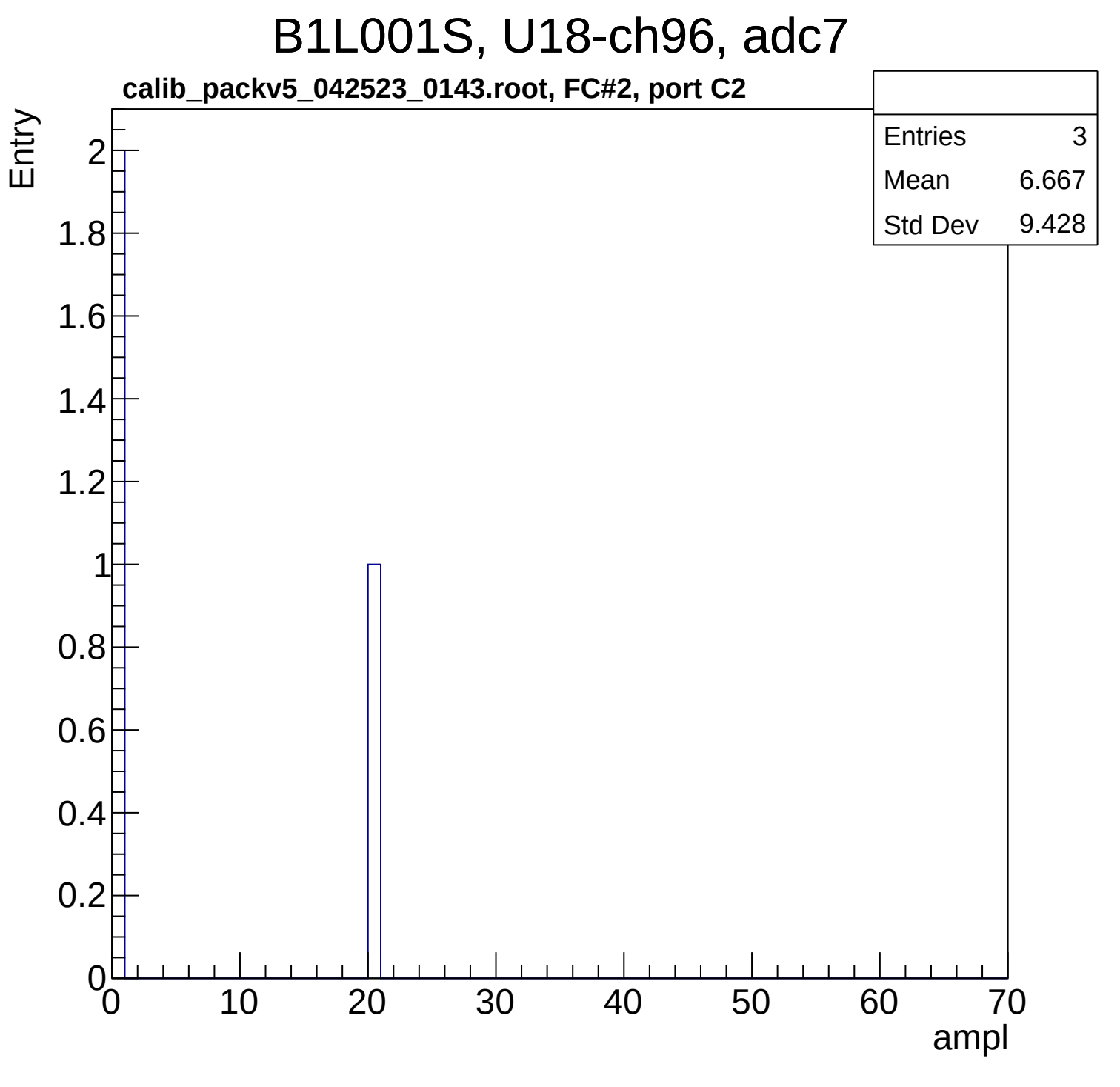

B1L001S, U18-ch96, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 127
Mean 44.32
Std Dev 3.089
Gaus mean : 44.6719
Gaus Width: 3.2350
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

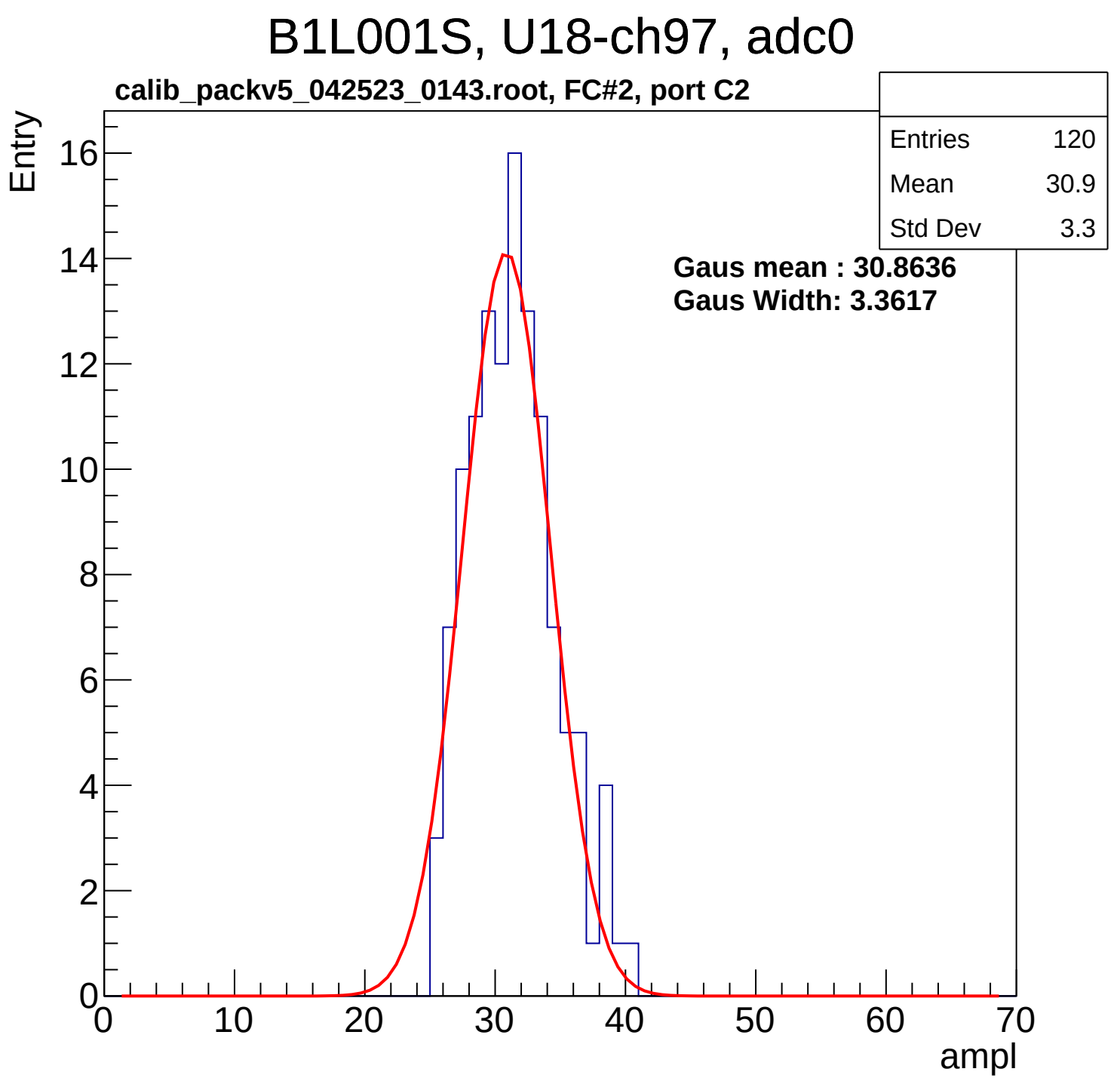

B1L001S, U18-ch96, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 130
Mean 50.99
Std Dev 3.259
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

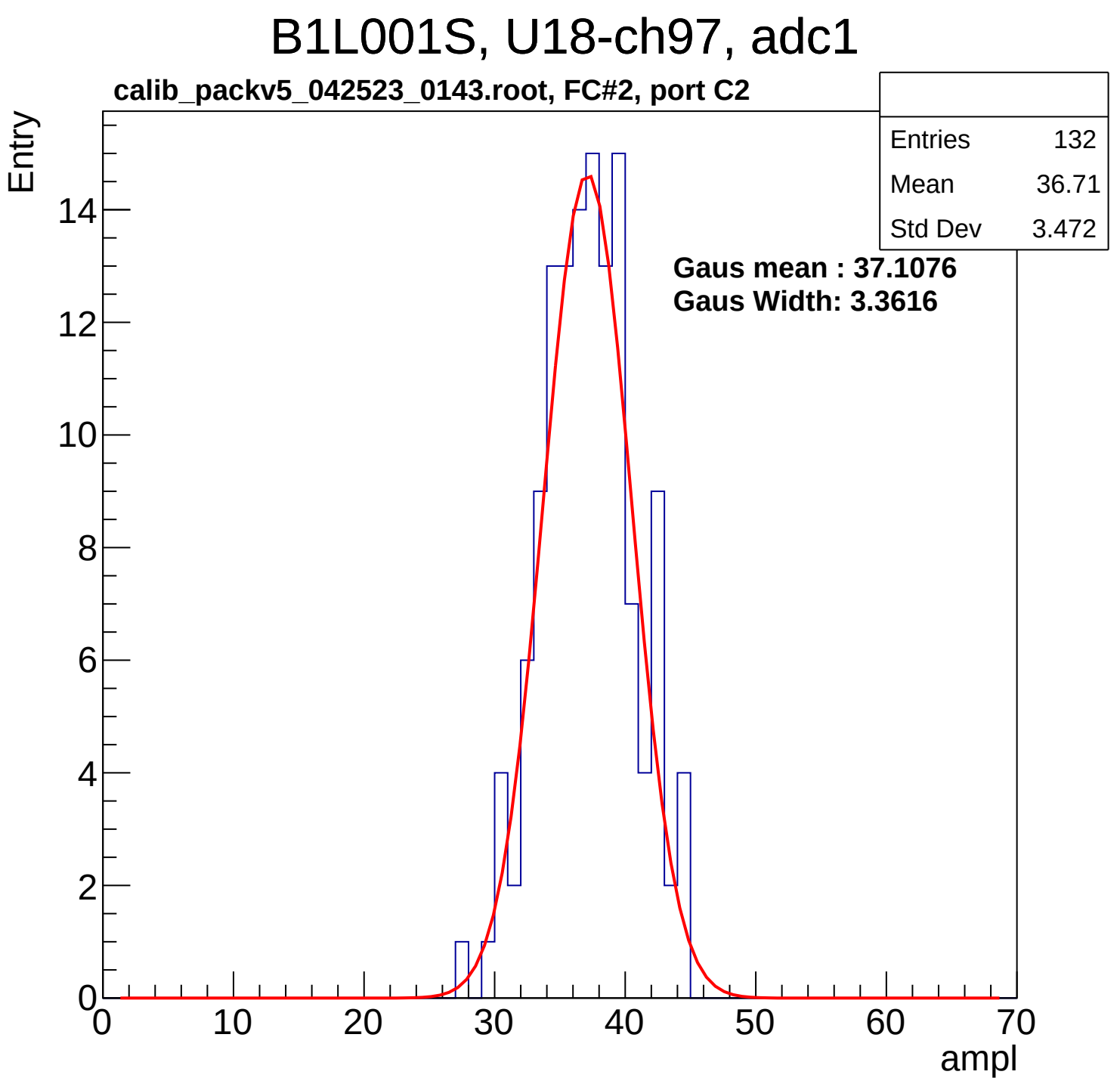

B1L001S, U18-ch96, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 97
Mean 56.39
Std Dev 3.338
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70

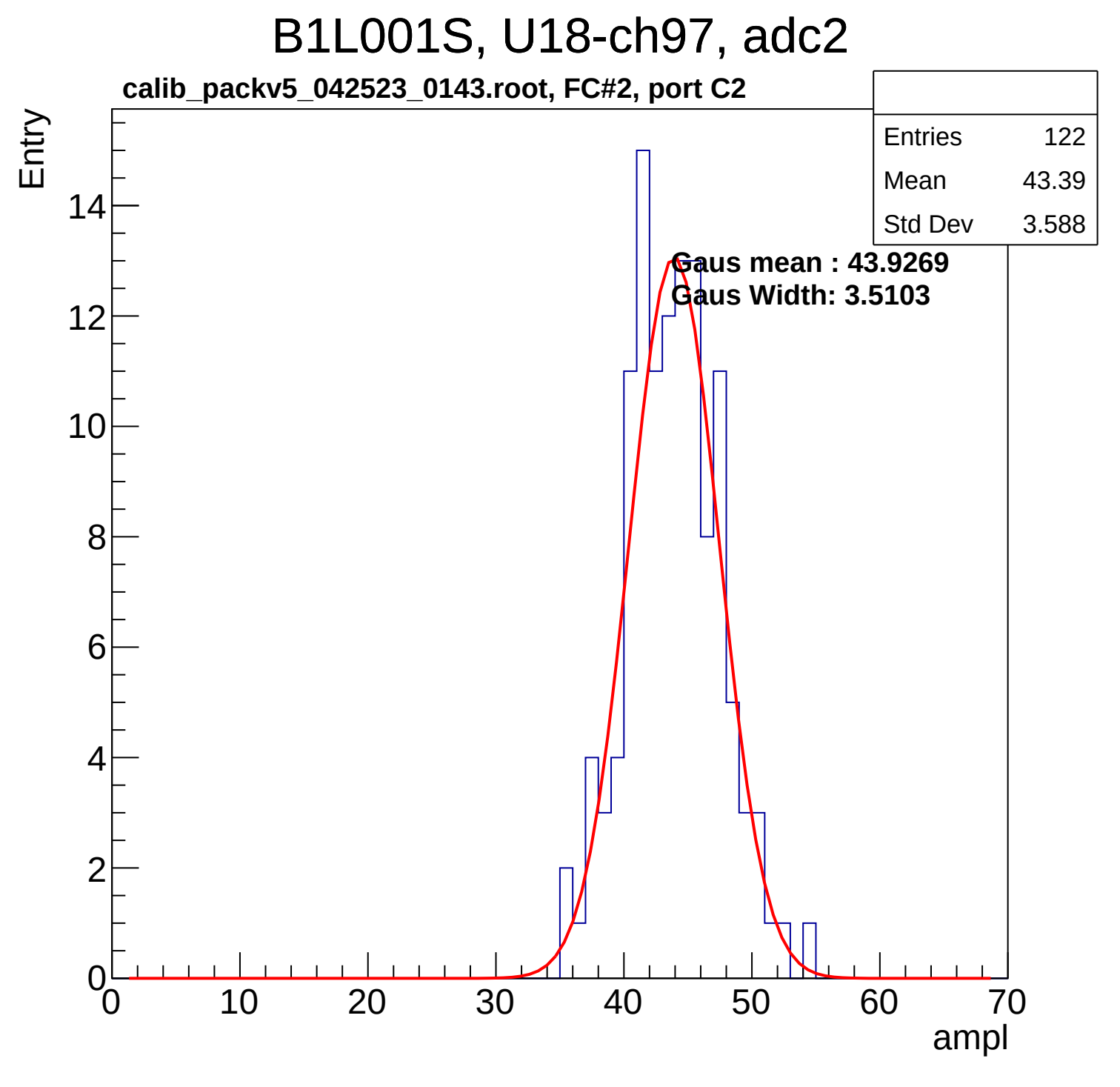

B1L001S, U18-ch96, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 86
Mean 59.47
Std Dev 6.823
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

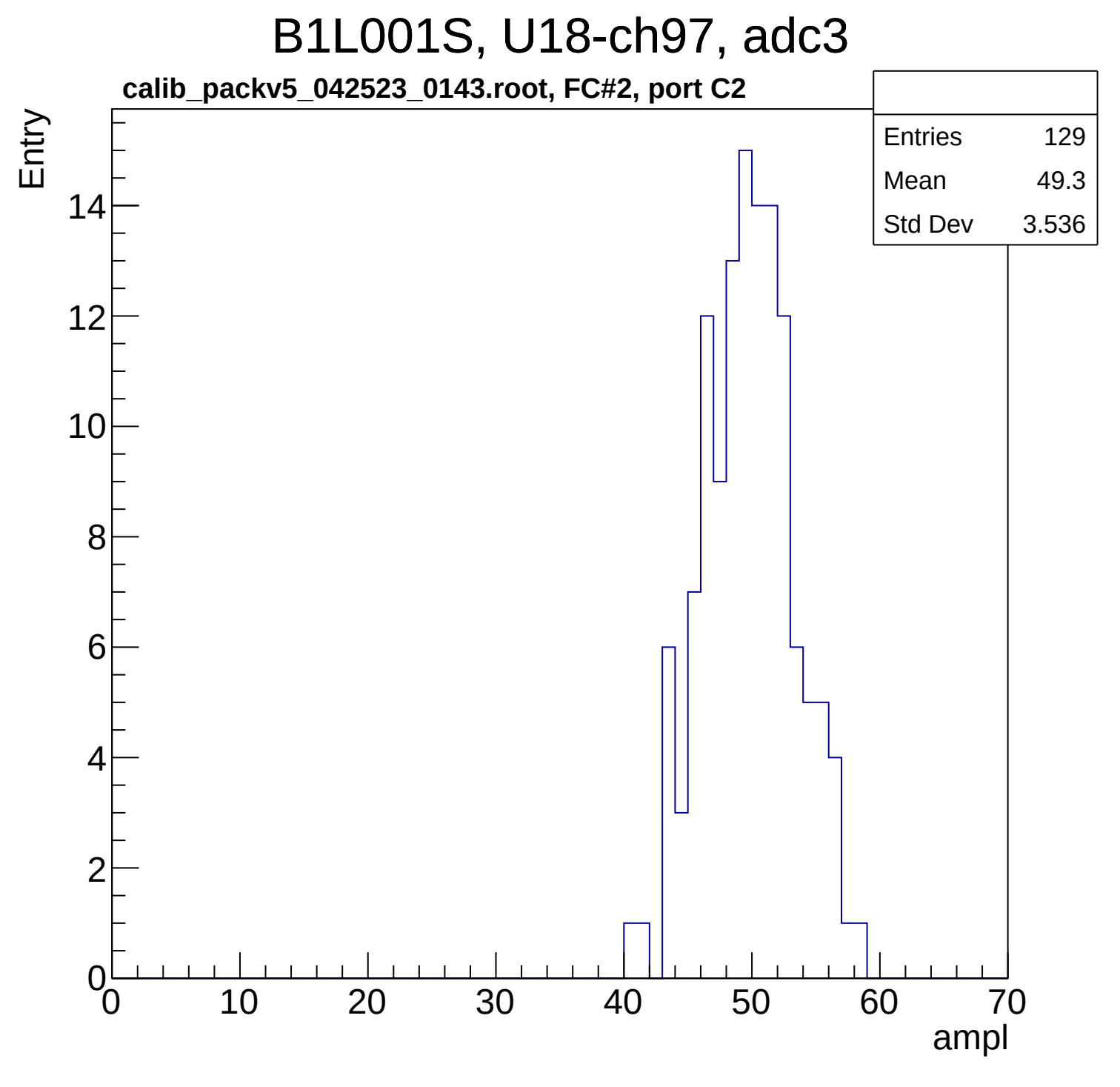

B1L001S, U18-ch96, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 8
Mean 54.38
Std Dev 20.56
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

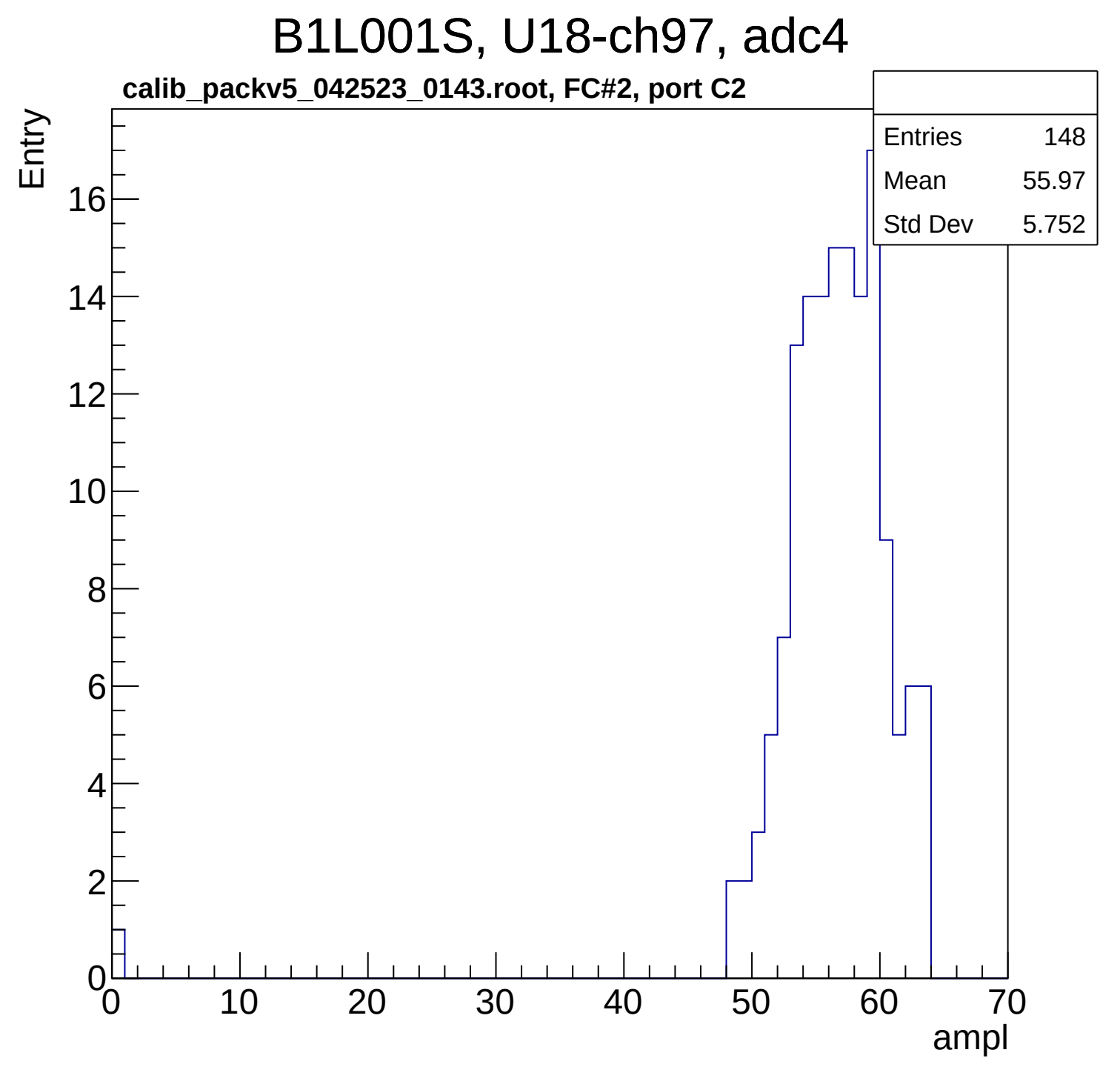

B1L001S, U18-ch96, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 3
Mean 6.667
Std Dev 9.428
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

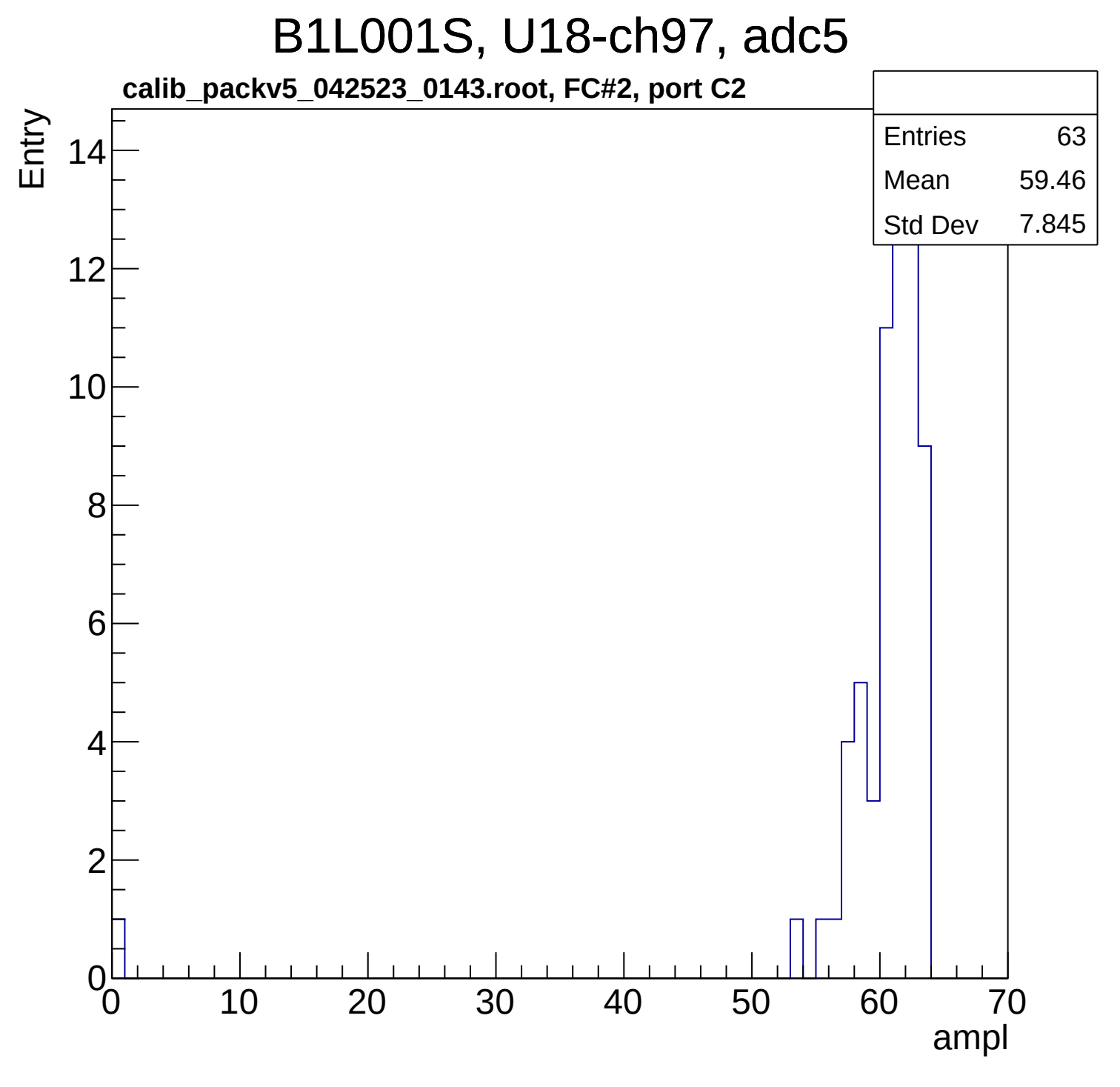

B1L001S, U18-ch97, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 120
Mean 30.9
Std Dev 3.3
Gaus mean : 30.8636
Gaus Width: 3.3617
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

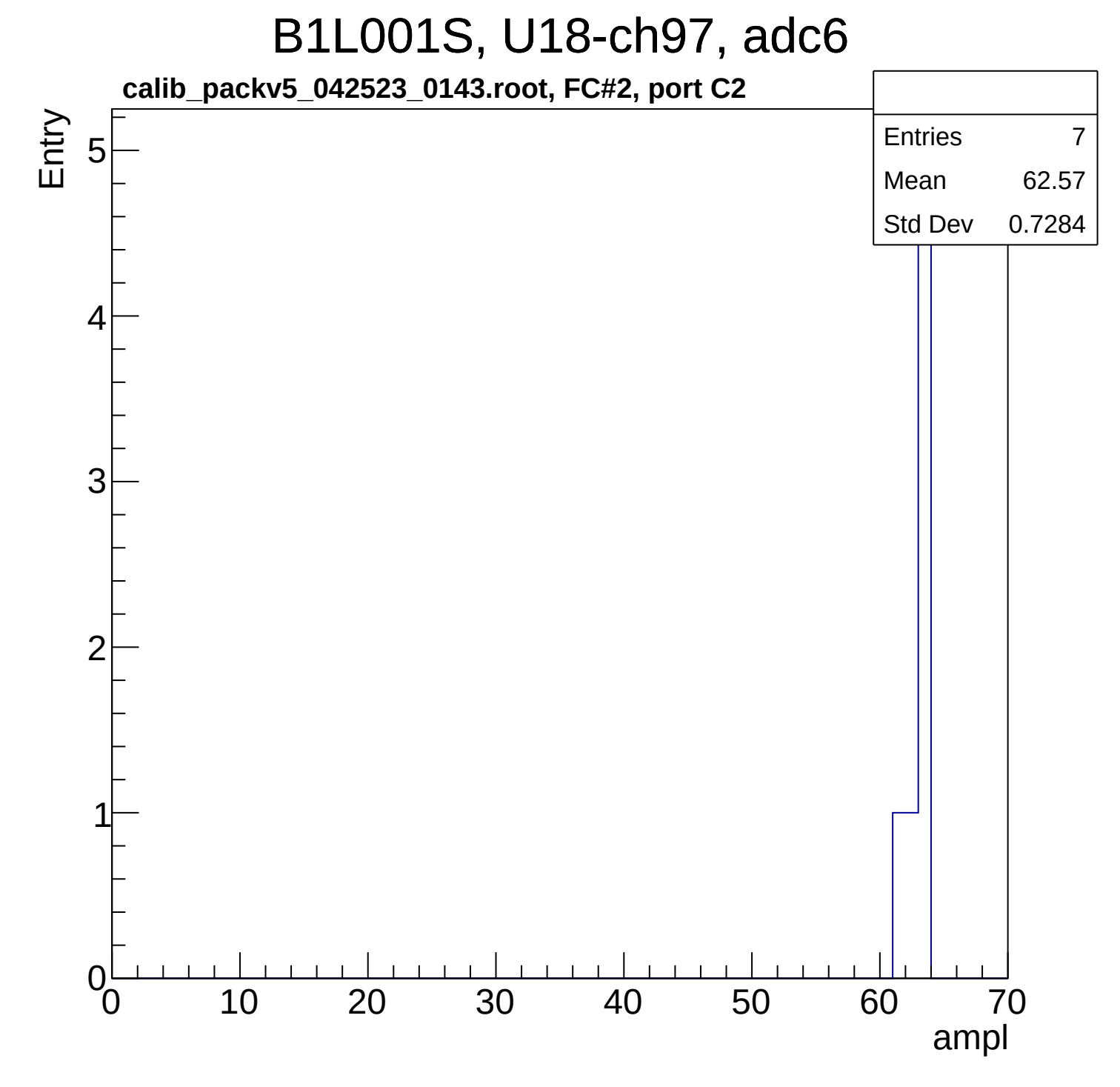

B1L001S, U18-ch97, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 132
Mean 36.71
Std Dev 3.472
Gaus mean : 37.1076
Gaus Width: 3.3616
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

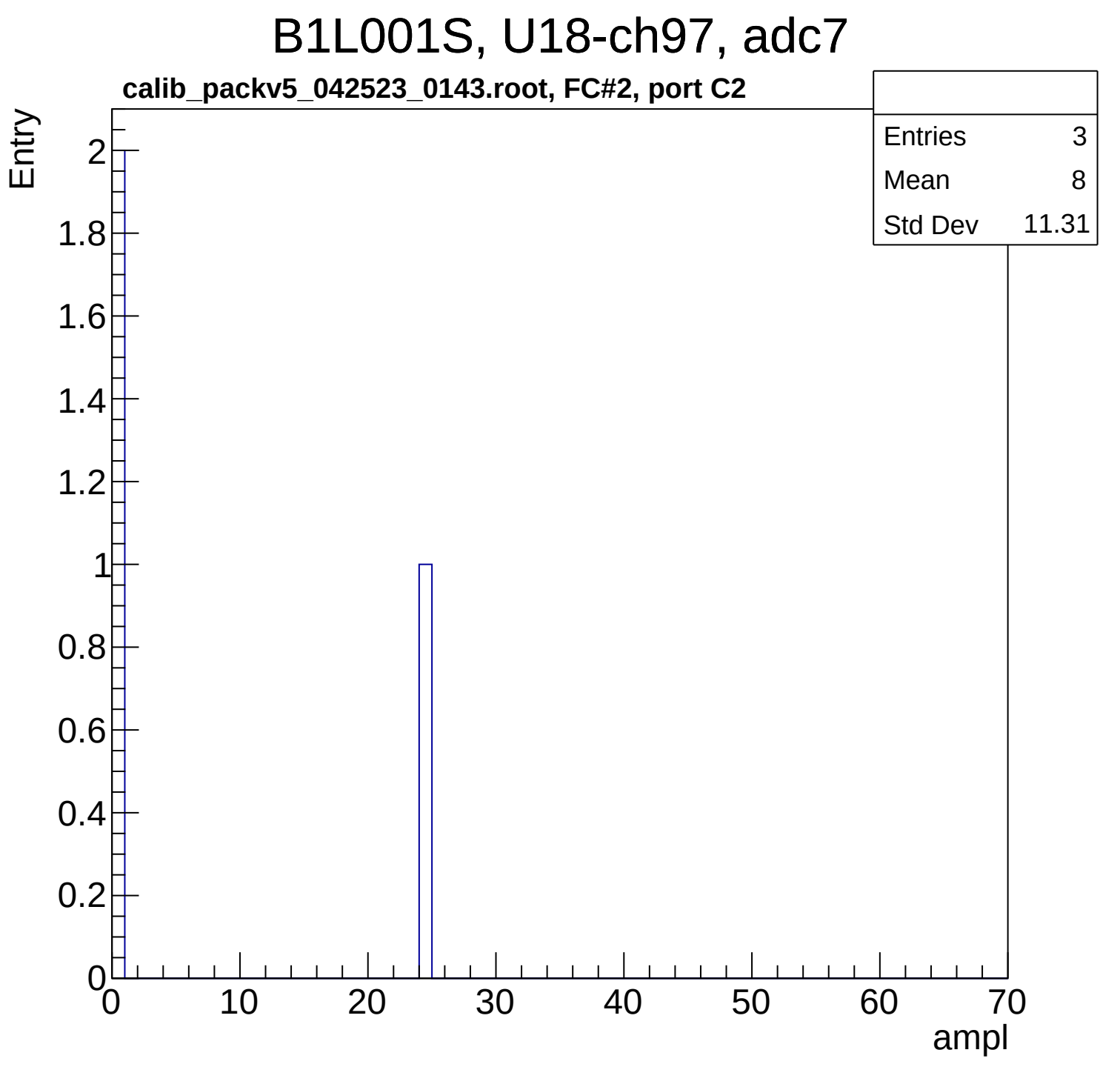

B1L001S, U18-ch97, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 122
Mean 43.39
Std Dev 3.588
Gaus mean : 43.9269
Gaus Width: 3.5103
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

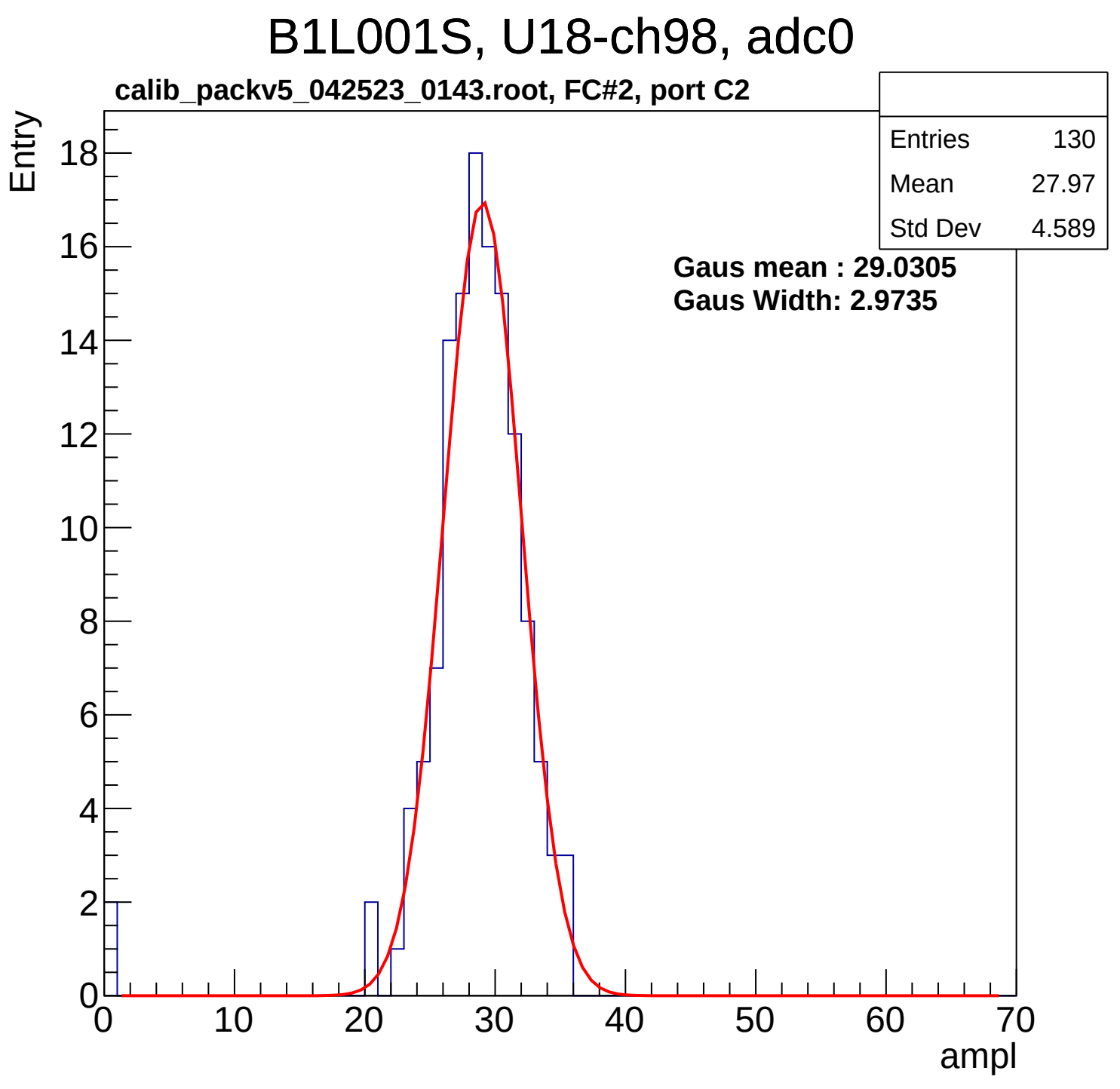

B1L001S, U18-ch97, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 129
Mean 49.3
Std Dev 3.536
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

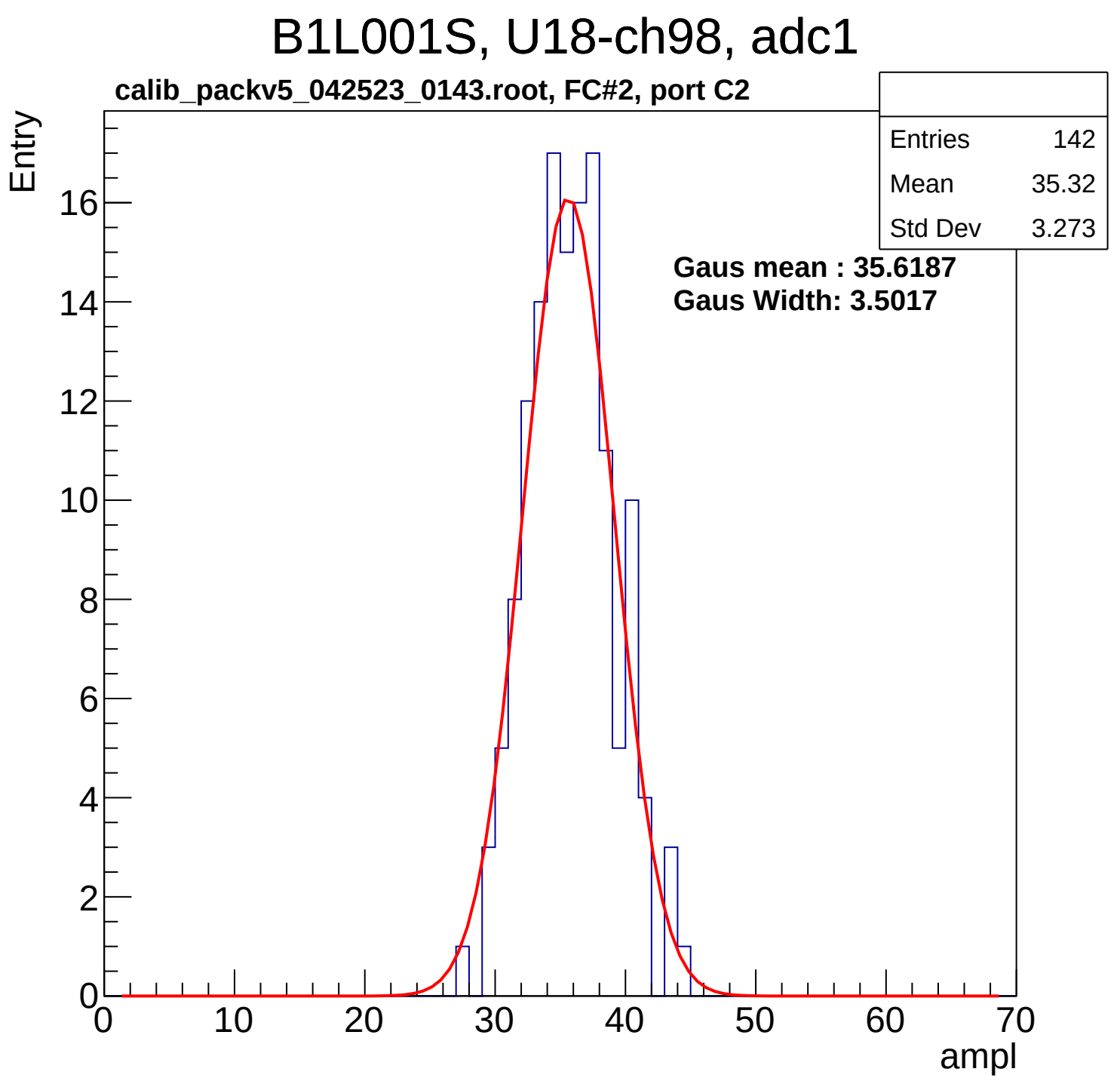

B1L001S, U18-ch97, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 148
Mean 55.97
Std Dev 5.752
Entry
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl

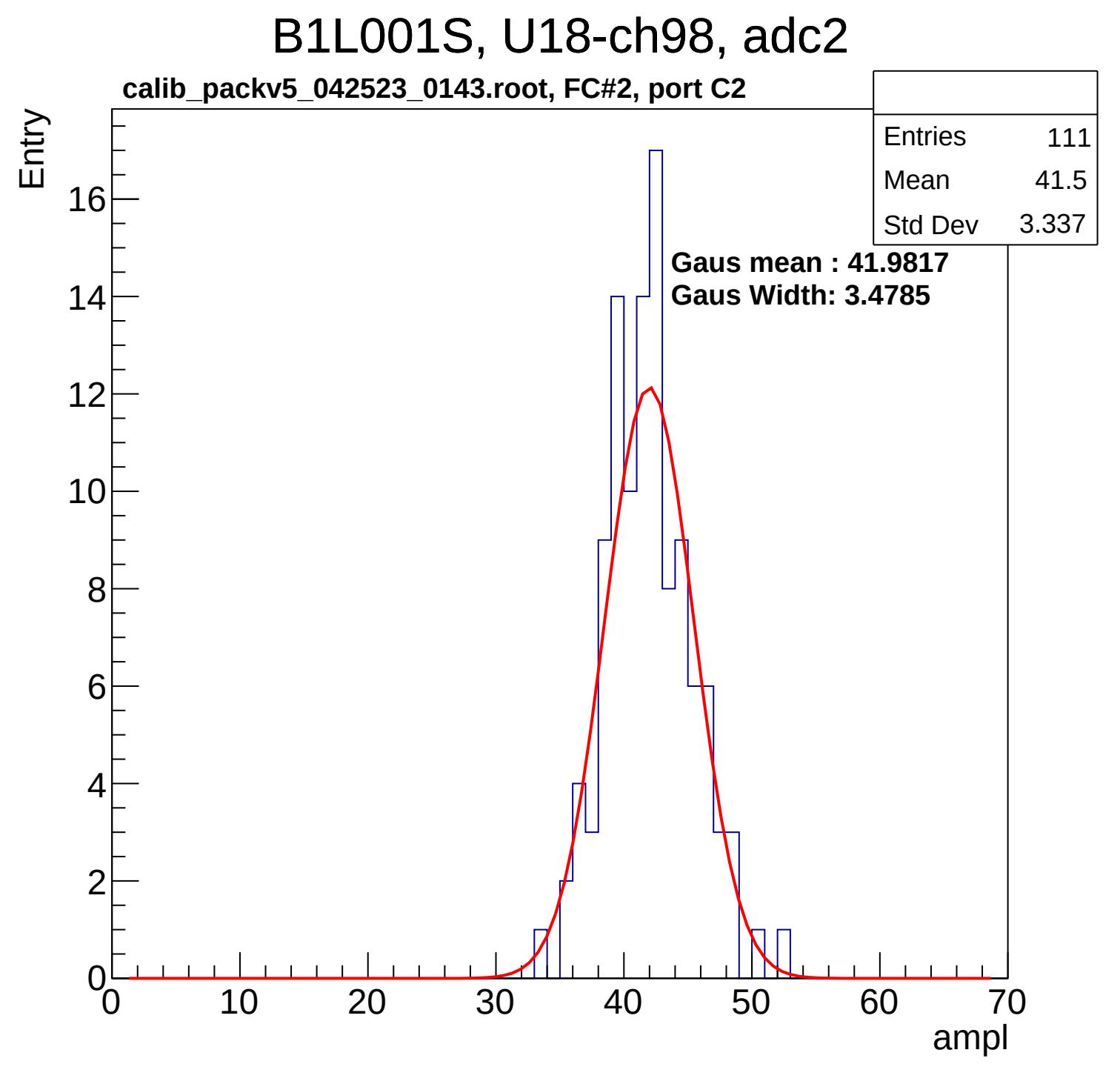

B1L001S, U18-ch97, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 63
Mean 59.46
Std Dev 7.845
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

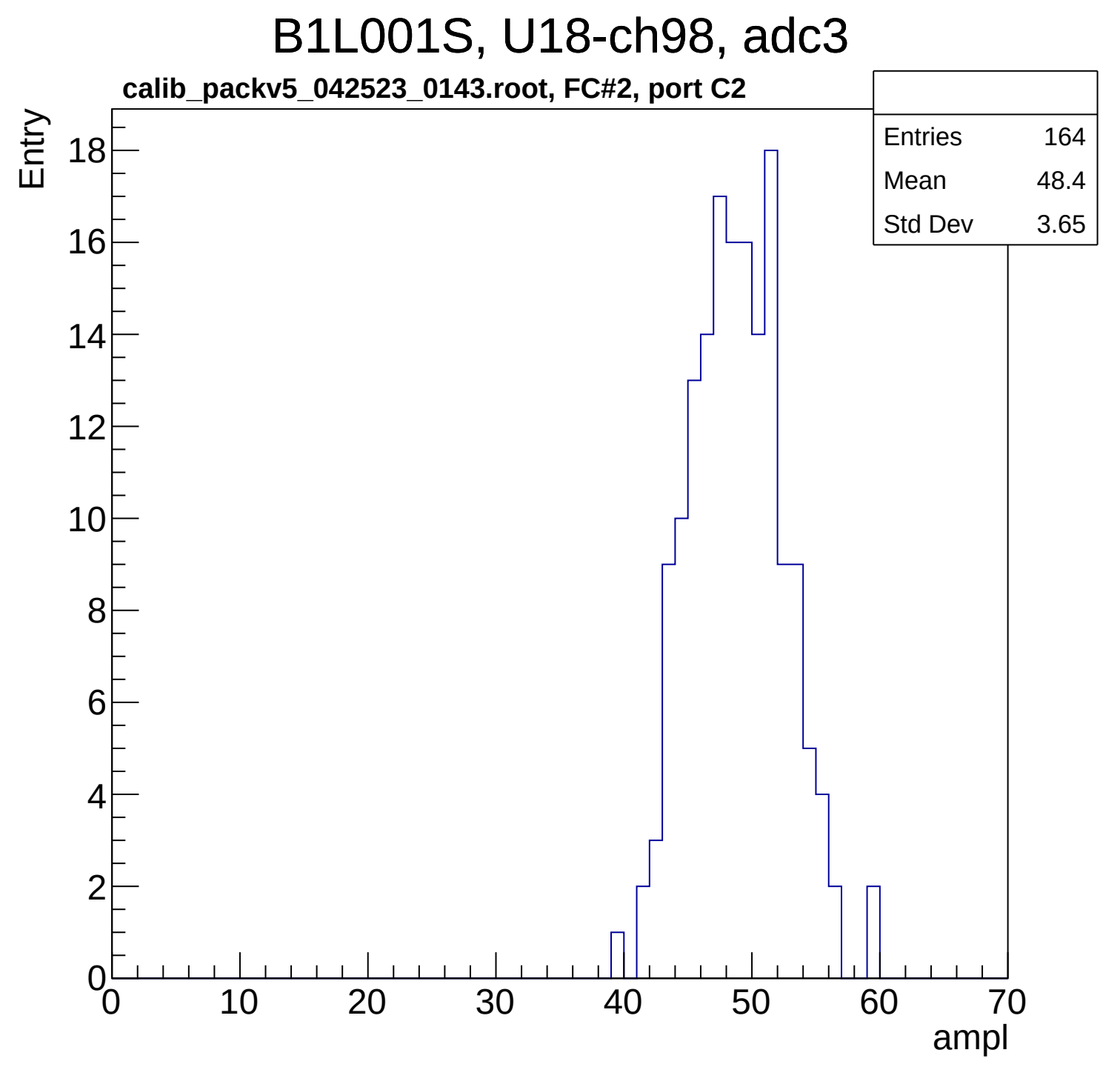

B1L001S, U18-ch97, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 7
Mean 62.57
Std Dev 0.7284
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

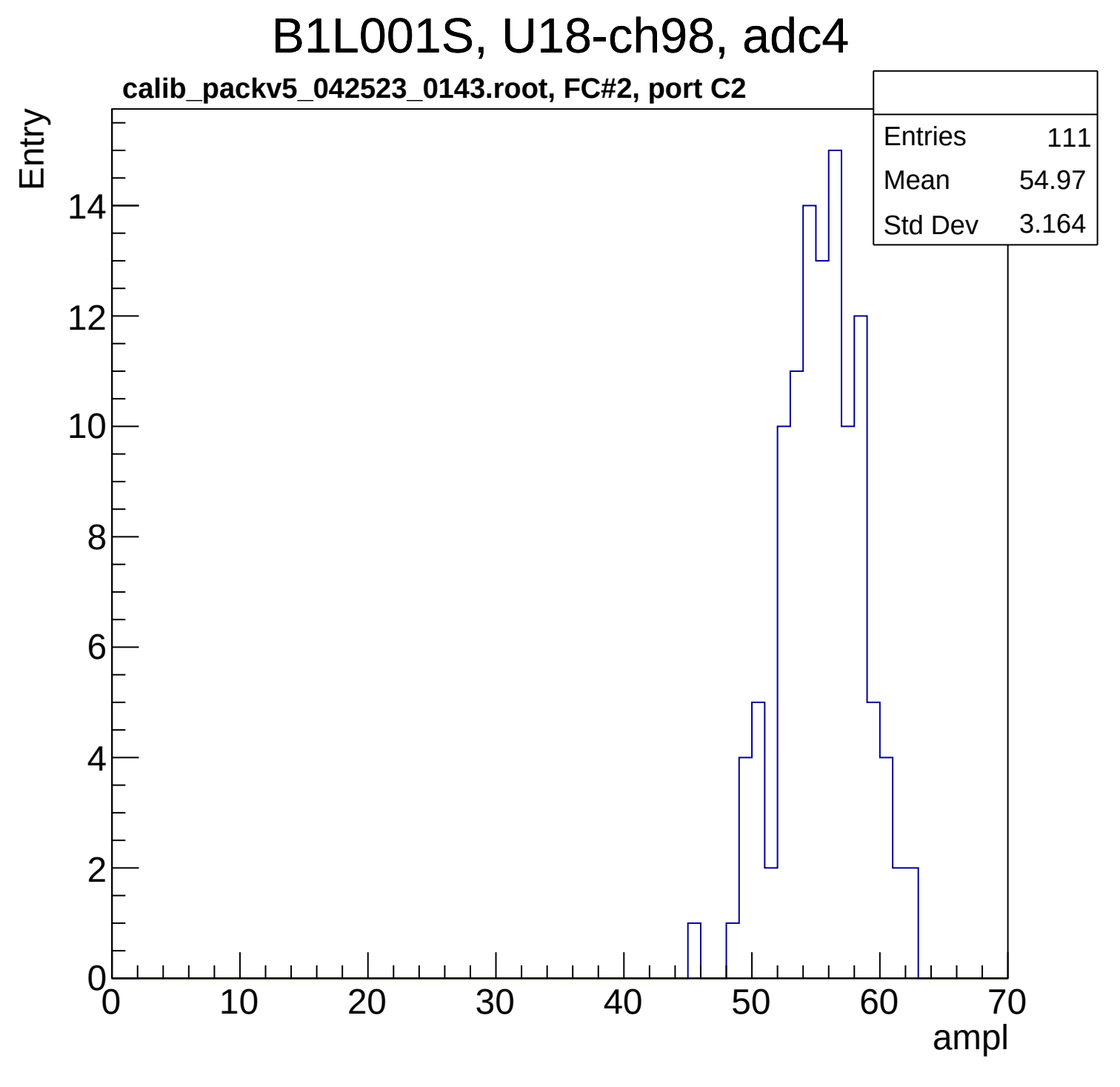

B1L001S, U18-ch97, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 3
Mean 8
Std Dev 11.31
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

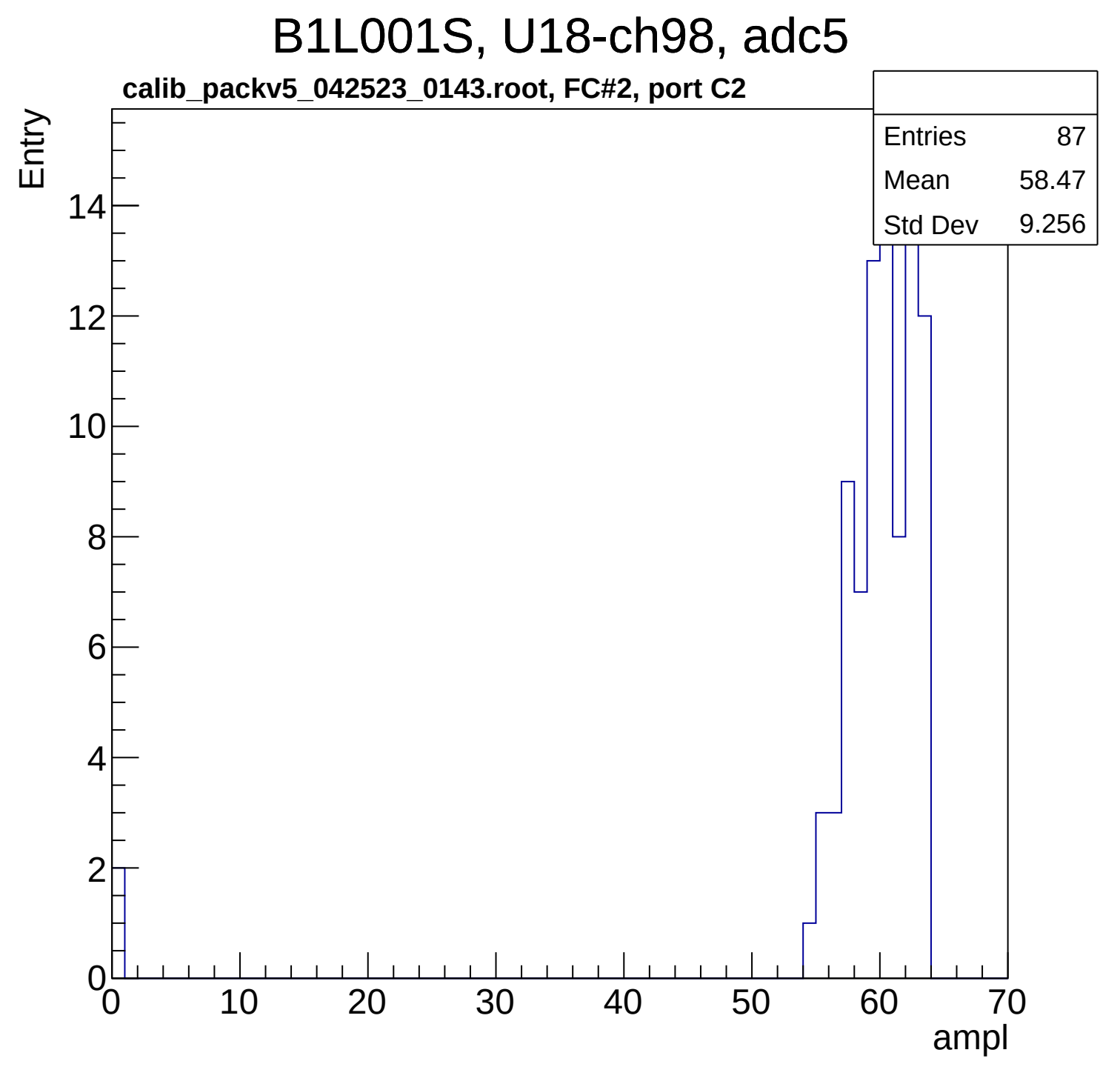

B1L001S, U18-ch98, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 130
Mean 27.97
Std Dev 4.589
Gaus mean : 29.0305
Gaus Width: 2.9735
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

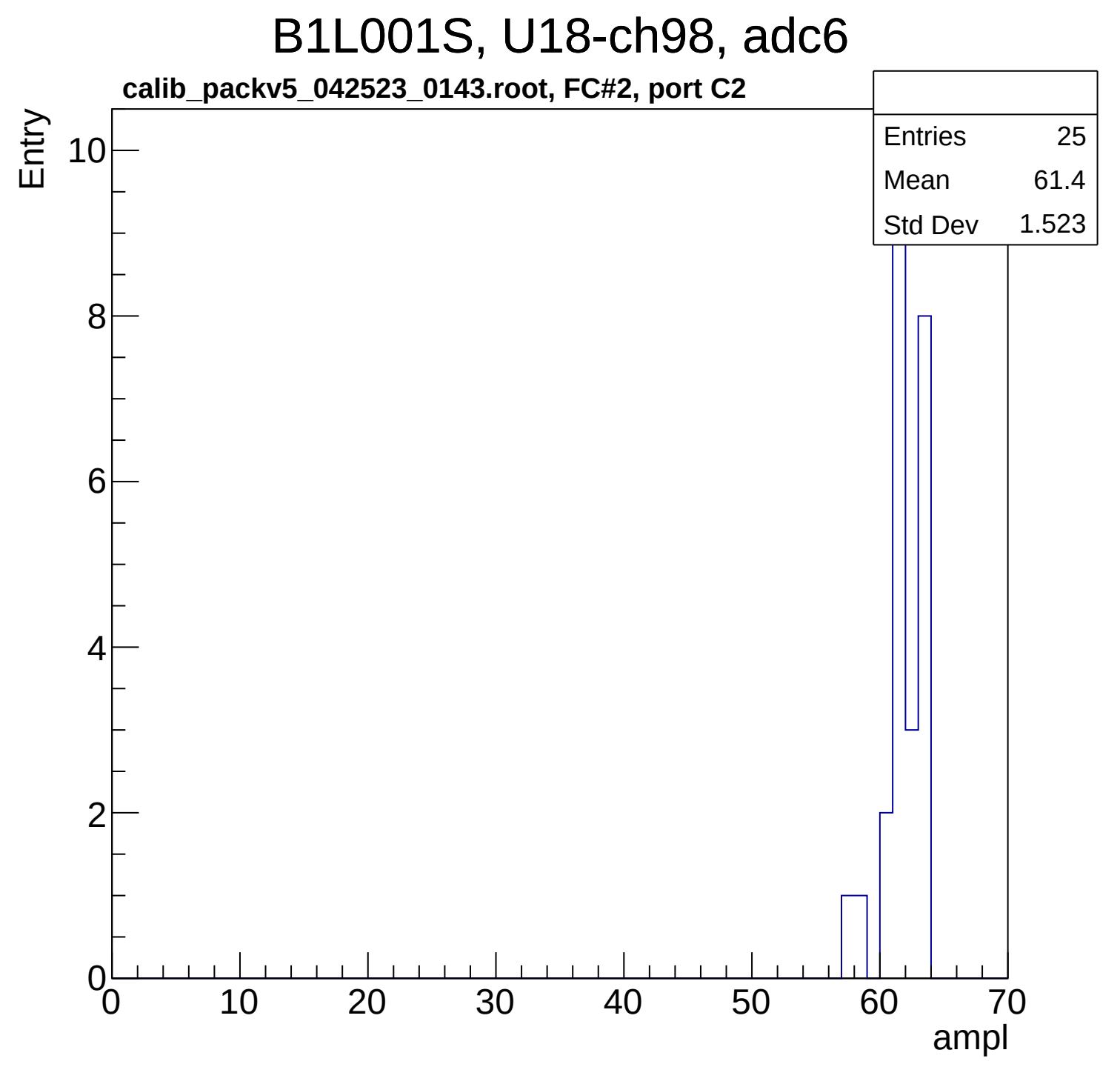

B1L001S, U18-ch98, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 142
Mean 35.32
Std Dev 3.273
Gaus mean : 35.6187
Gaus Width: 3.5017
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

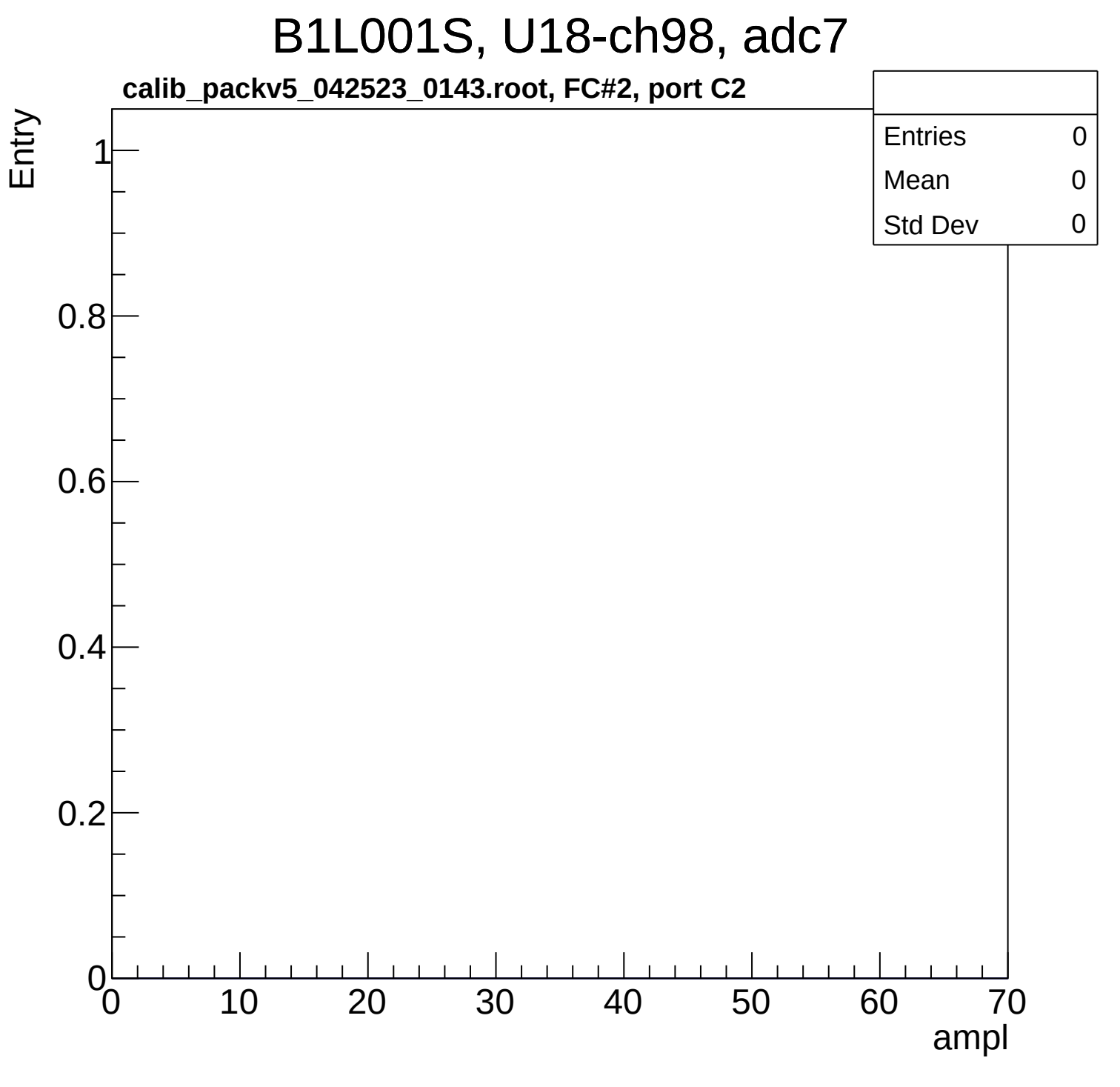

B1L001S, U18-ch98, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 111
Mean 41.5
Std Dev 3.337
Gaus mean : 41.9817
Gaus Width: 3.4785
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

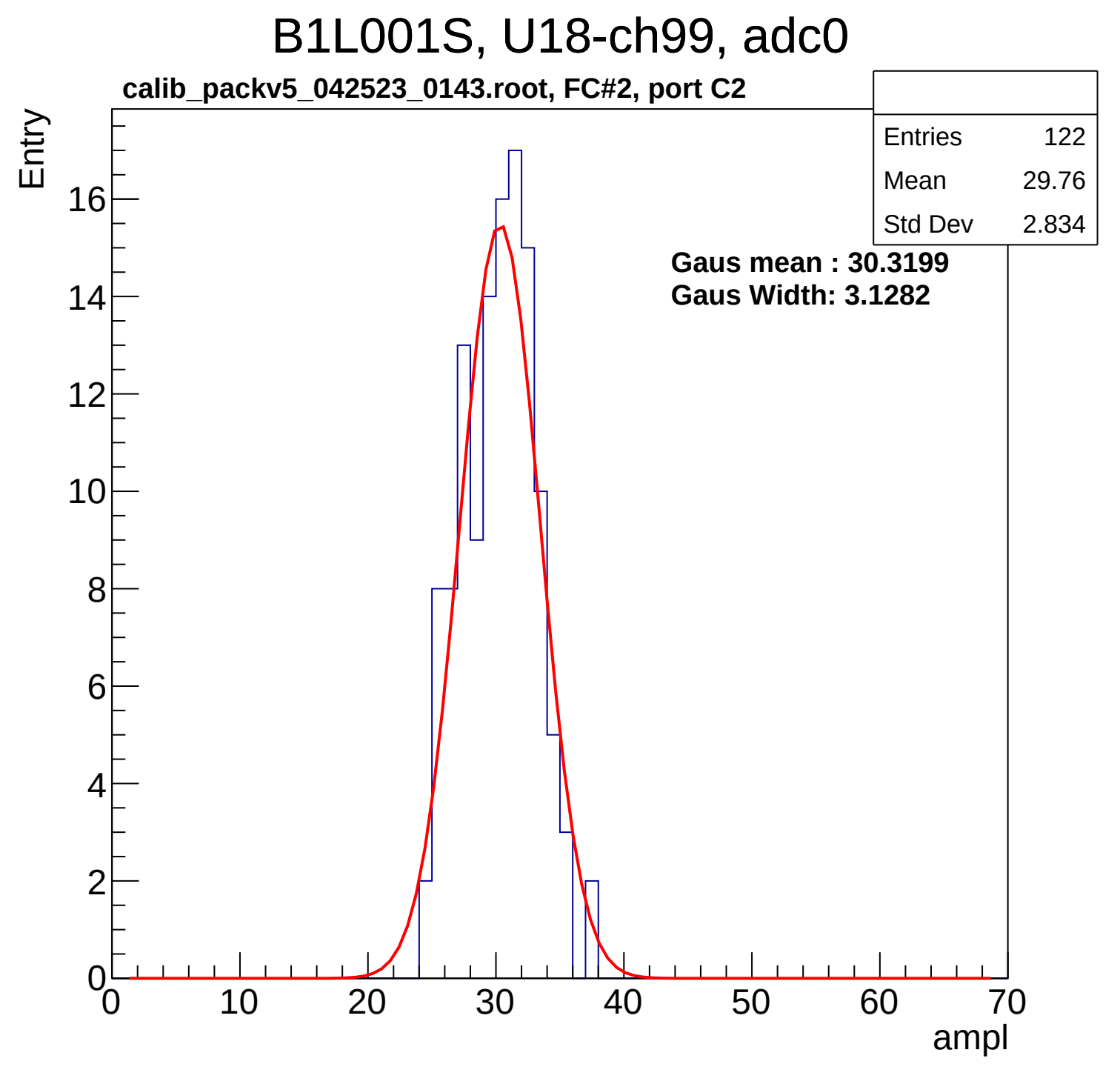

B1L001S, U18-ch98, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 164
Mean 48.4
Std Dev 3.65
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

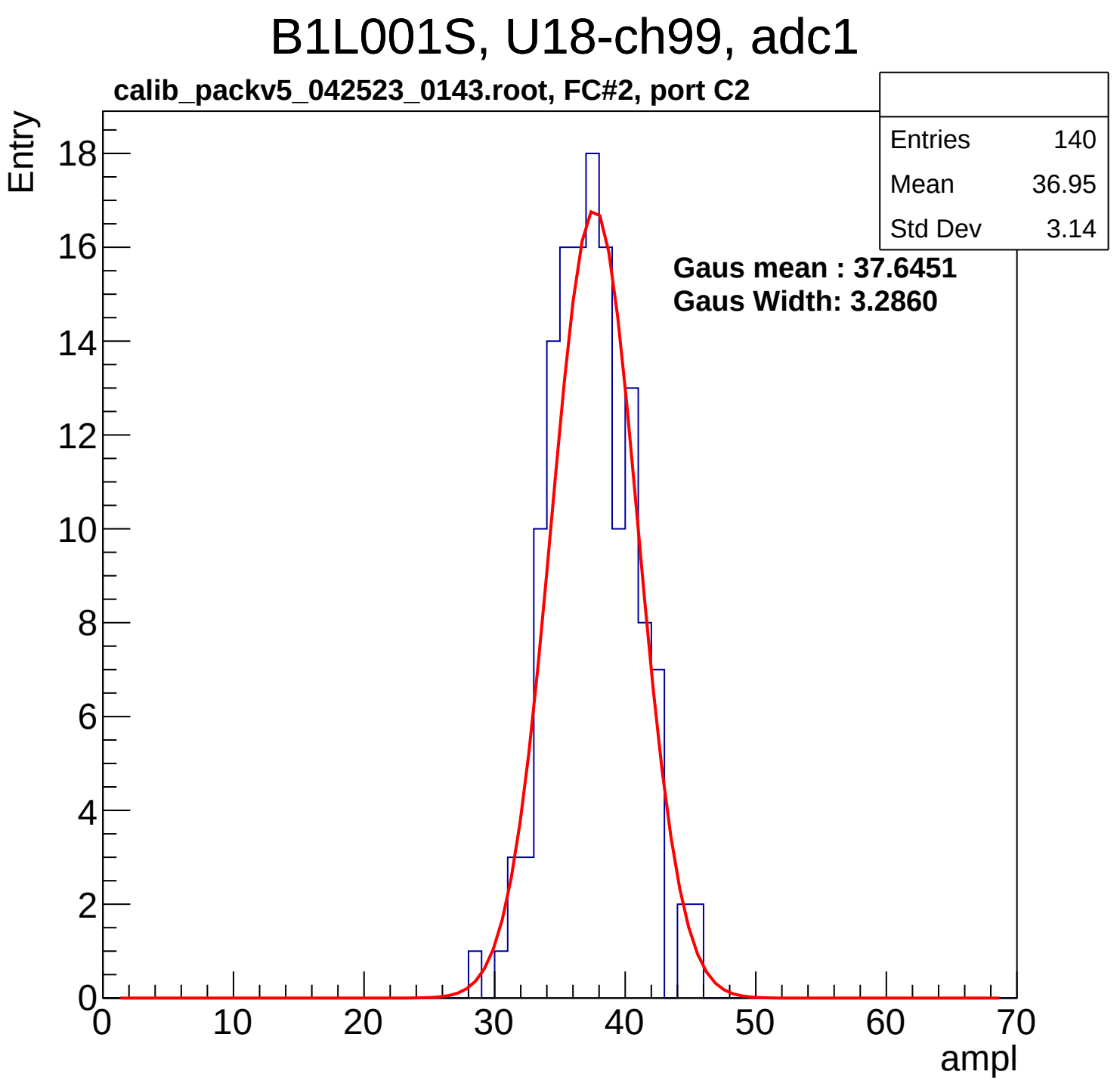

B1L001S, U18-ch98, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 111
Mean 54.97
Std Dev 3.164
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl

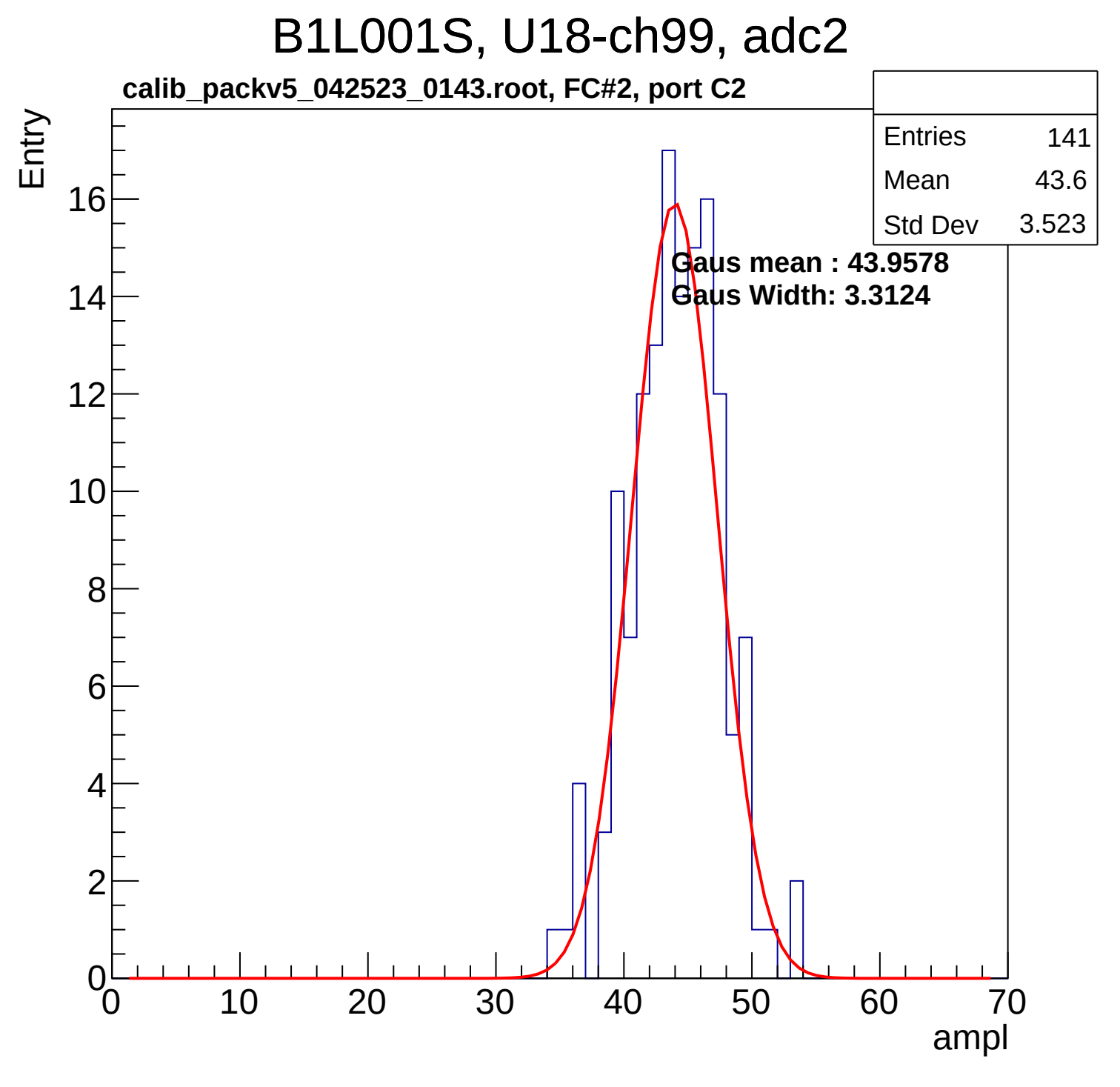

B1L001S, U18-ch98, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 87
Mean 58.47
Std Dev 9.256
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

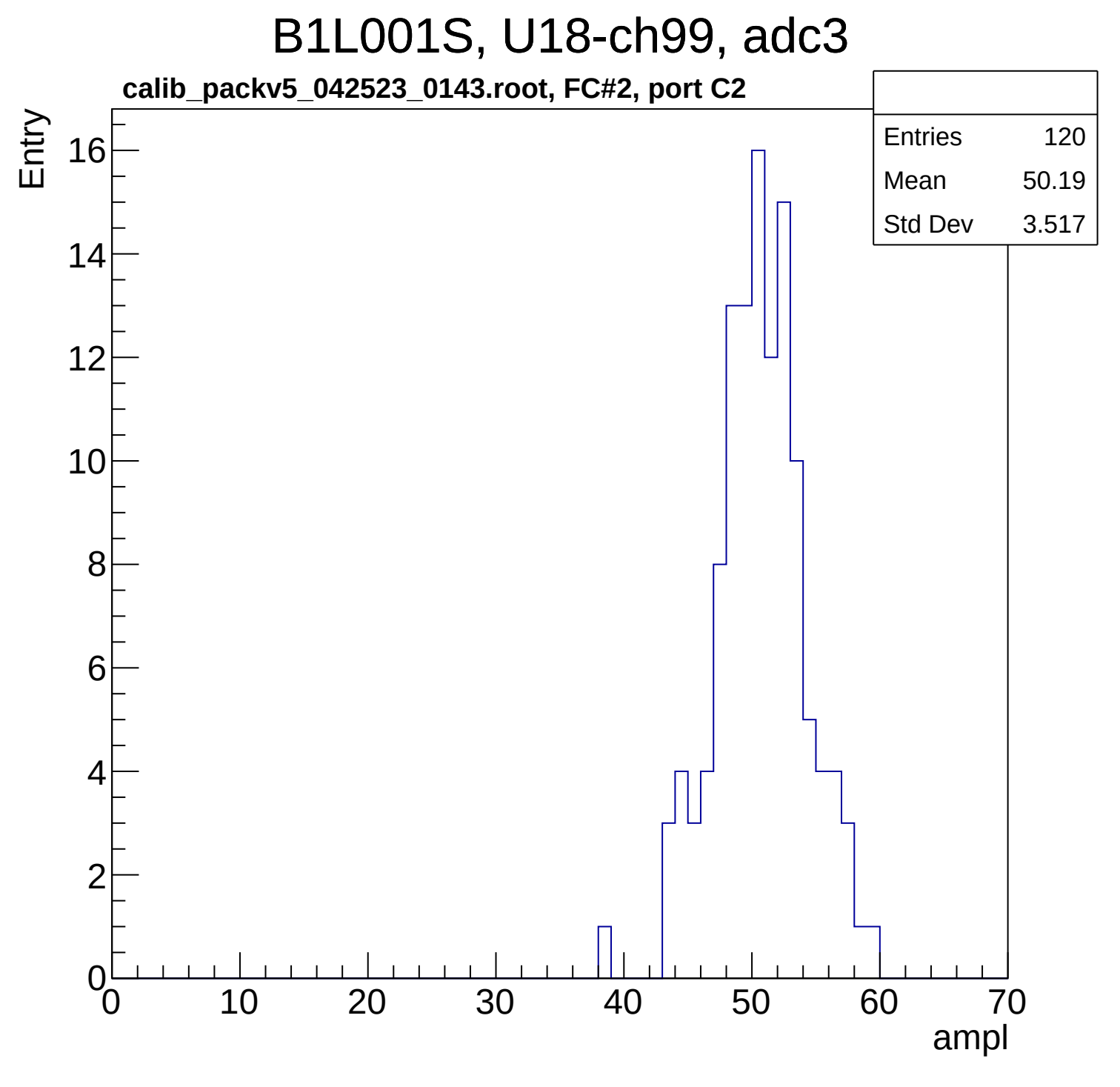

B1L001S, U18-ch98, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 25
Mean 61.4
Std Dev 1.523
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

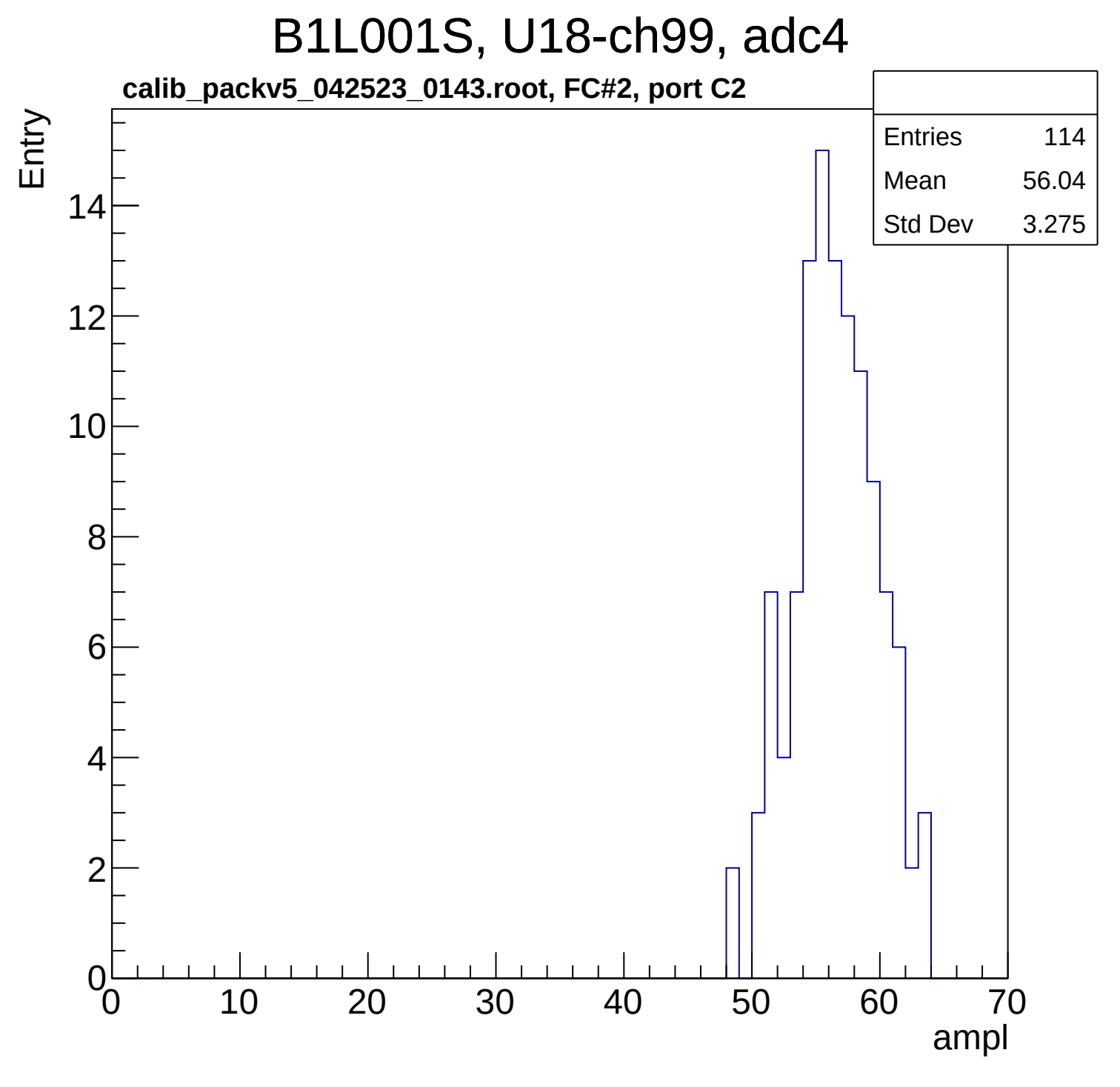

B1L001S, U18-ch98, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

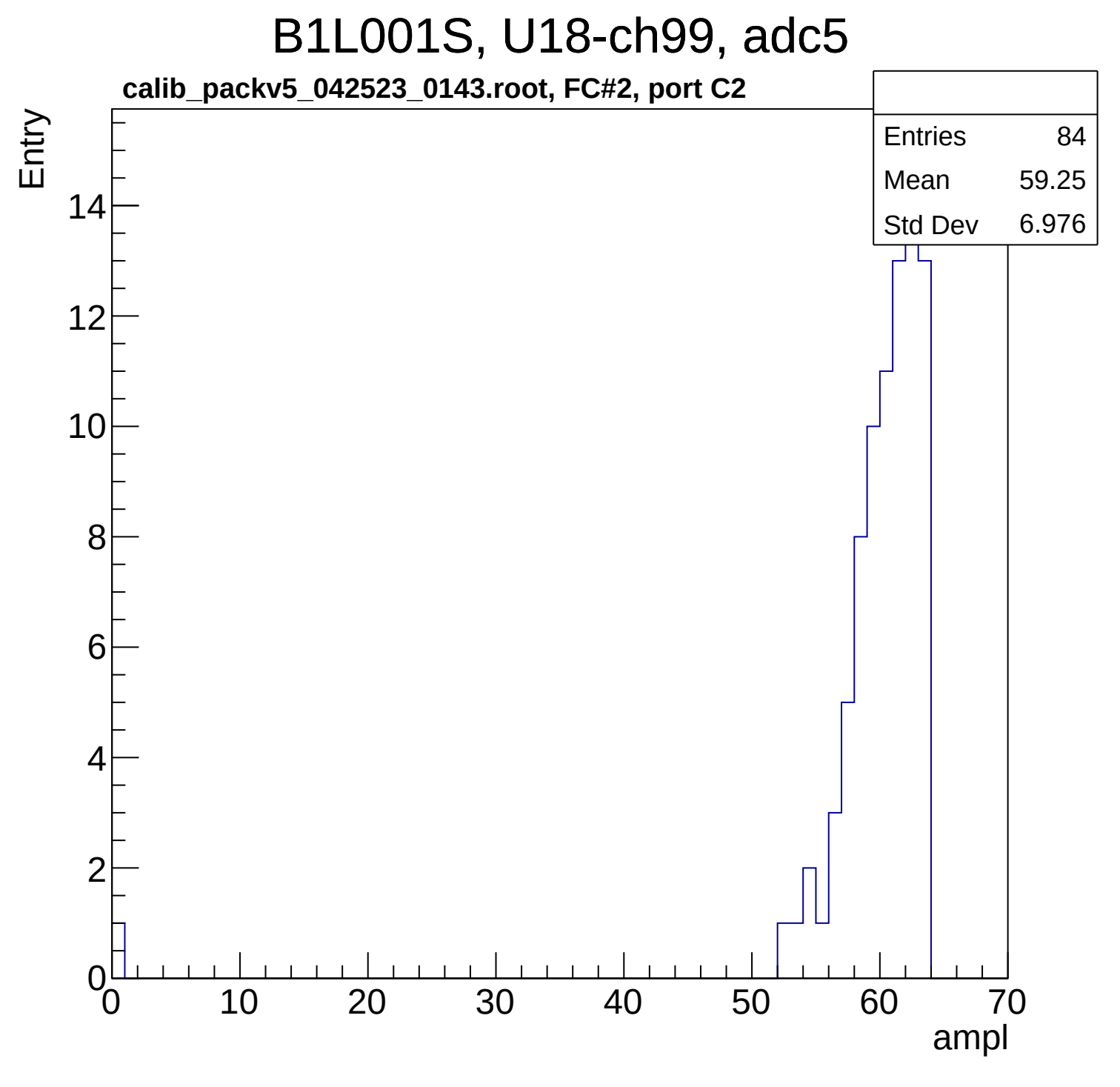

B1L001S, U18-ch99, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 122
Mean 29.76
Std Dev 2.834
Gaus mean : 30.3199
Gaus Width: 3.1282
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

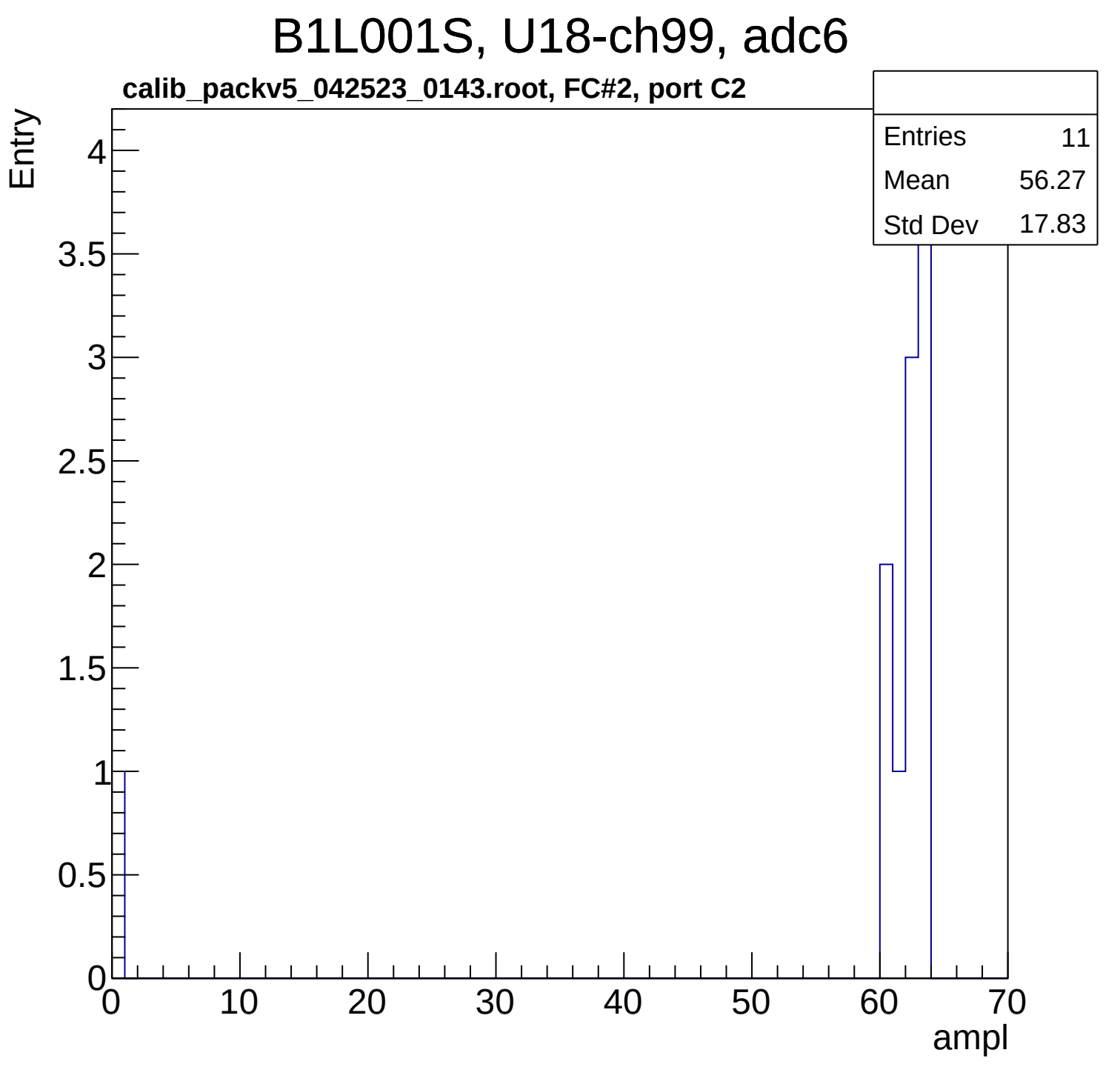

B1L001S, U18-ch99, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 140
Mean 36.95
Std Dev 3.14
Gaus mean : 37.6451
Gaus Width: 3.2860
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

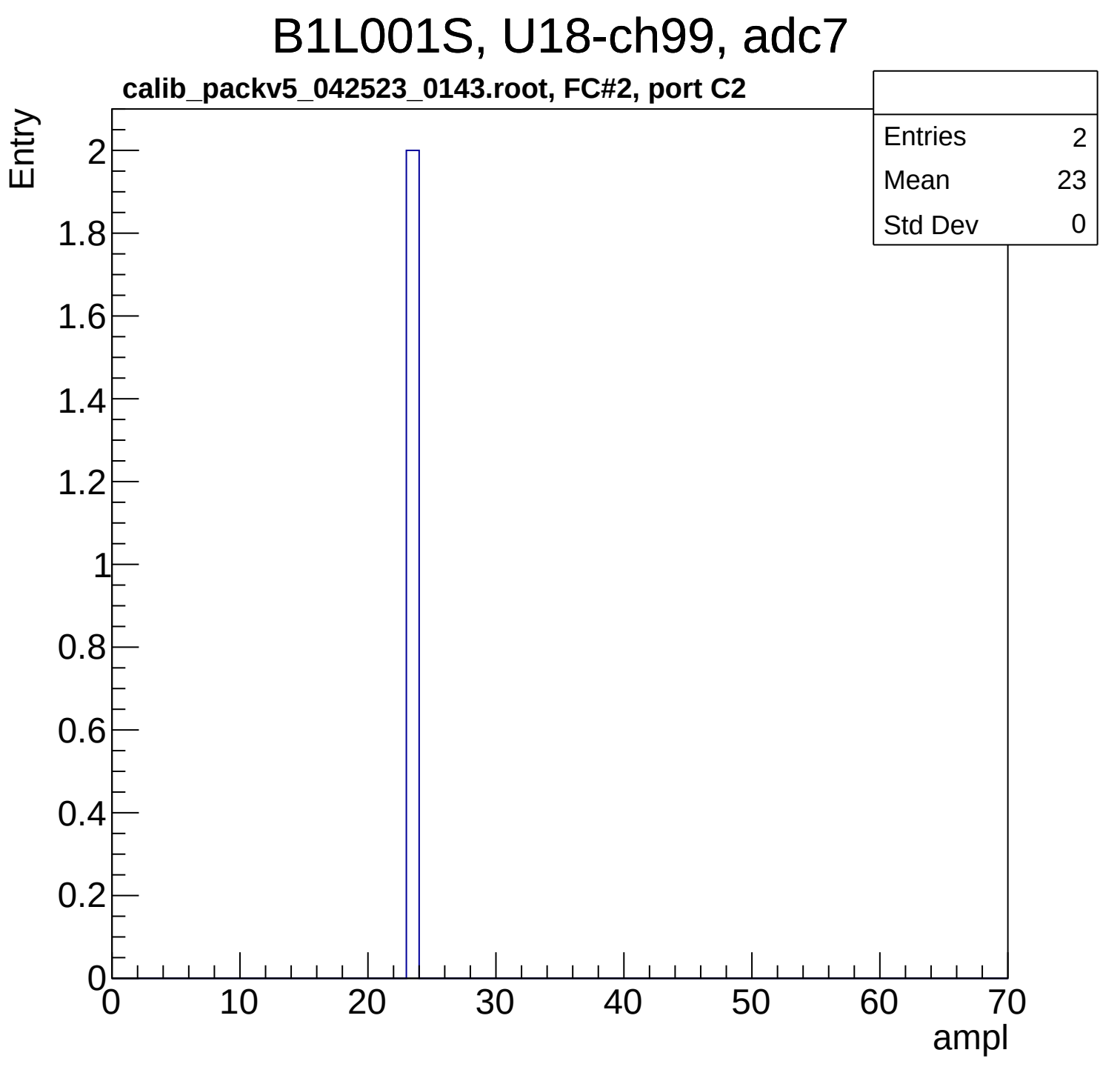

B1L001S, U18-ch99, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 141
Mean 43.6
Std Dev 3.523
Gaus mean : 43.9578
Gaus Width: 3.3124
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

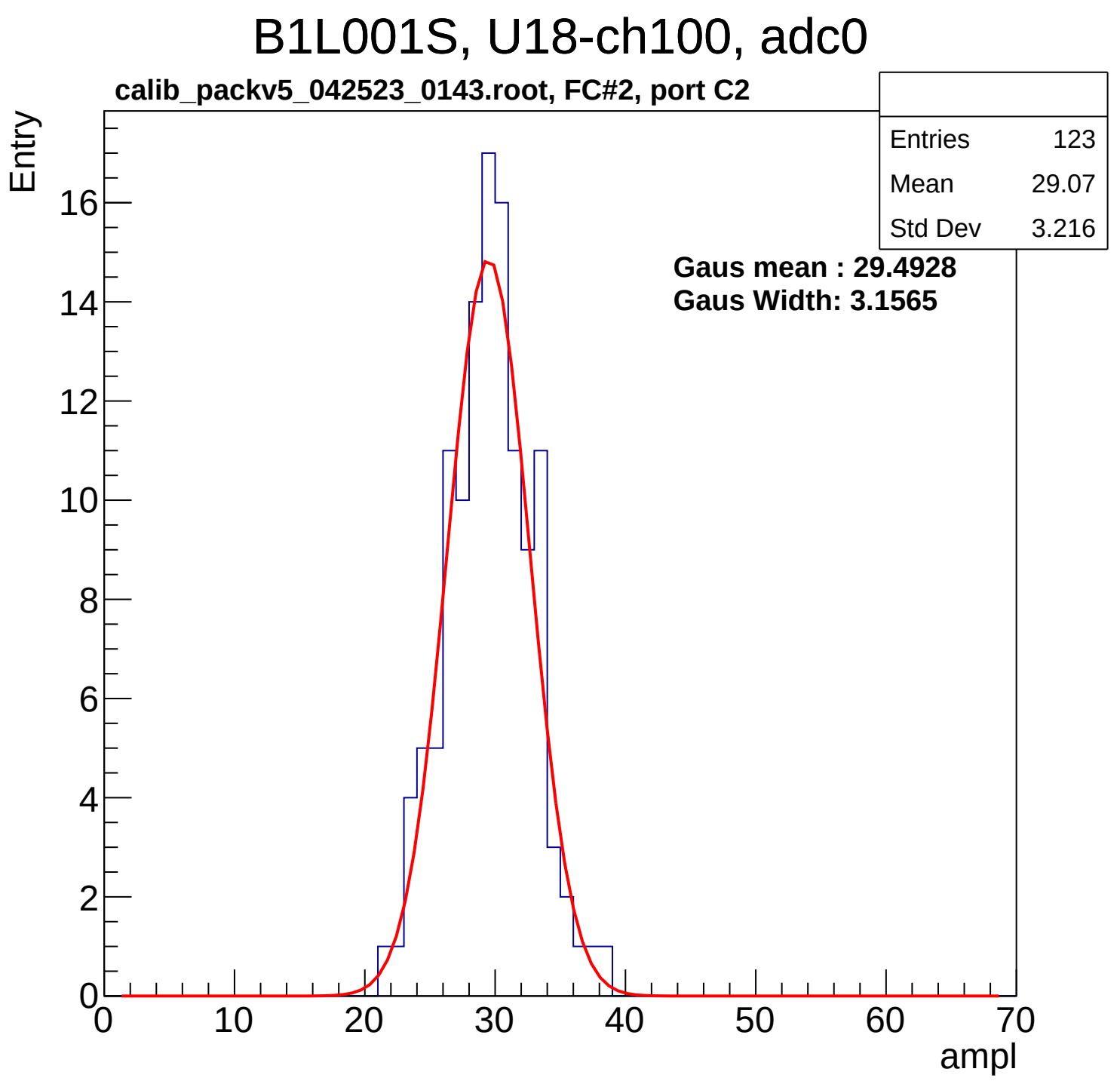

B1L001S, U18-ch99, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 120
Mean 50.19
Std Dev 3.517
Entry
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl

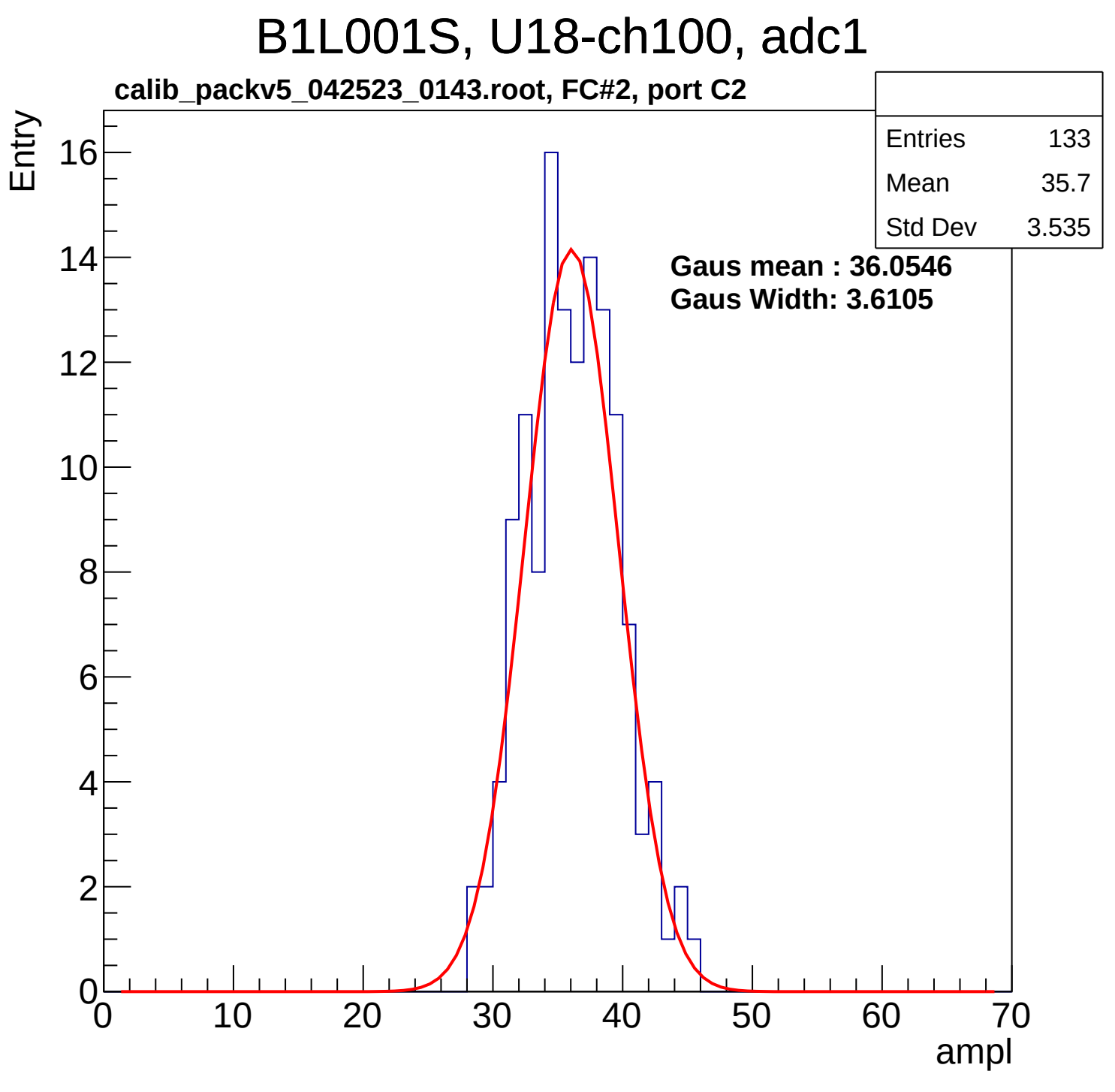

B1L001S, U18-ch99, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 114
Mean 56.04
Std Dev 3.275
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

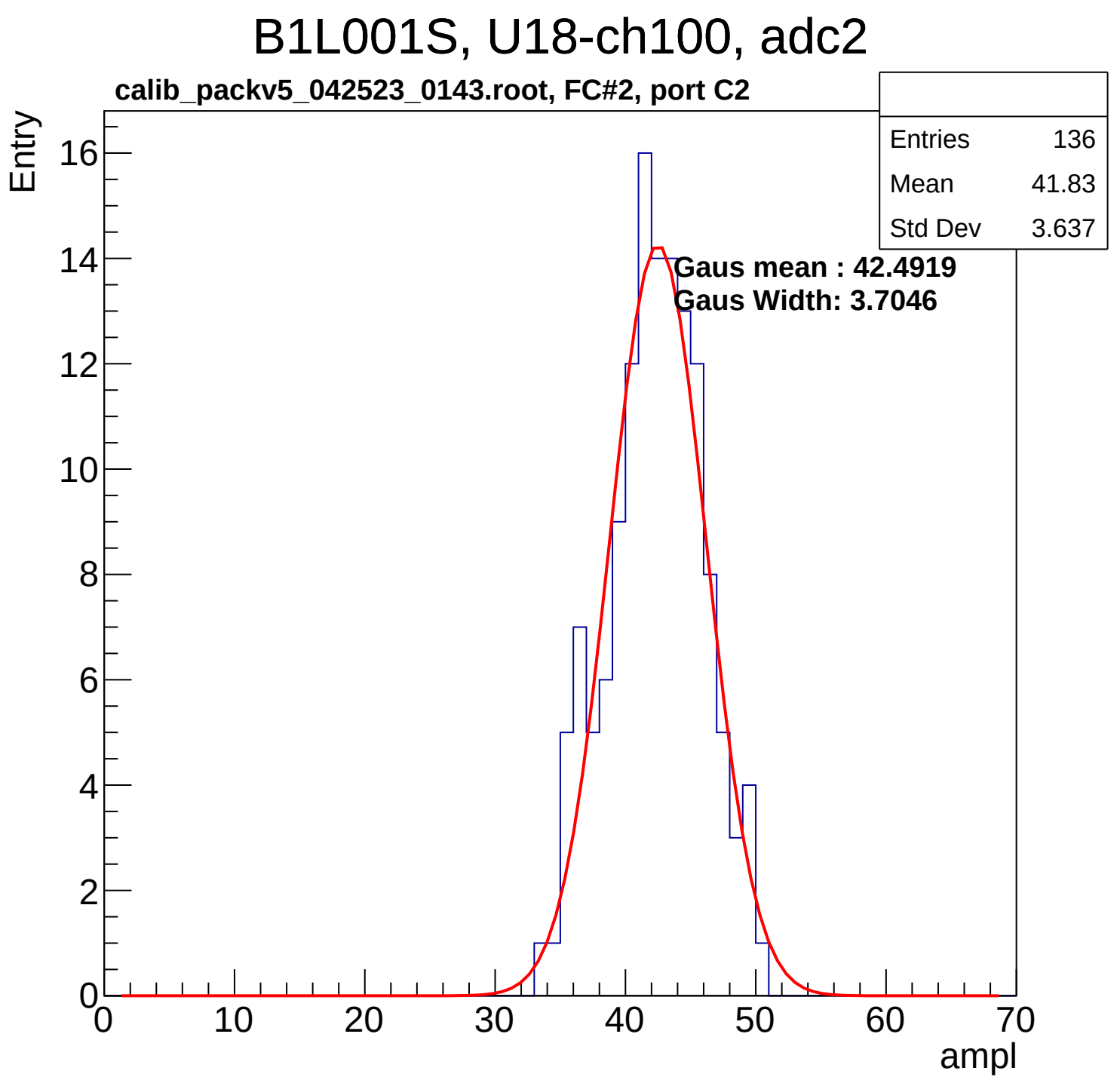

B1L001S, U18-ch99, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 84
Mean 59.25
Std Dev 6.976
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

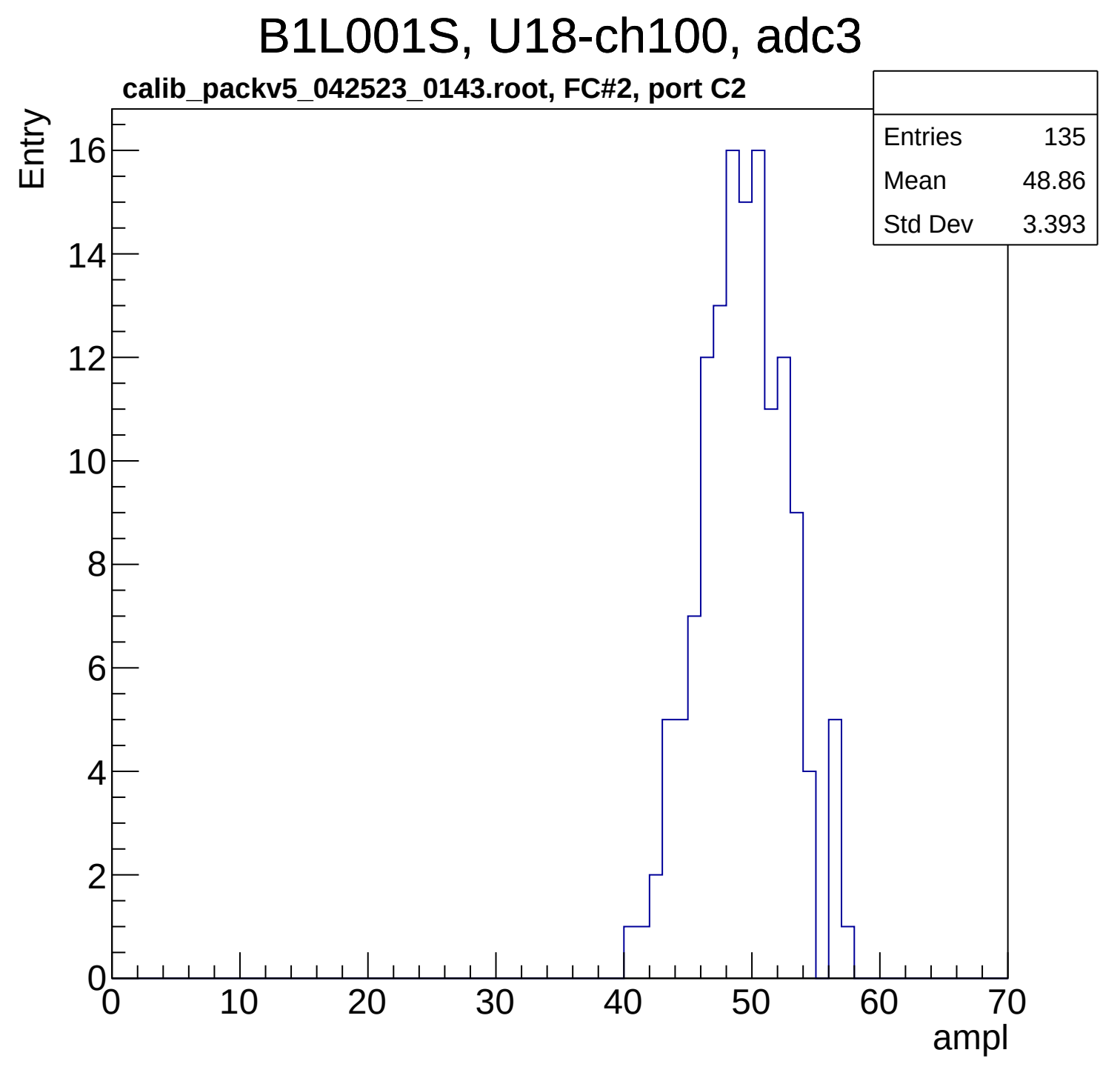

B1L001S, U18-ch99, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 11
Mean 56.27
Std Dev 17.83
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

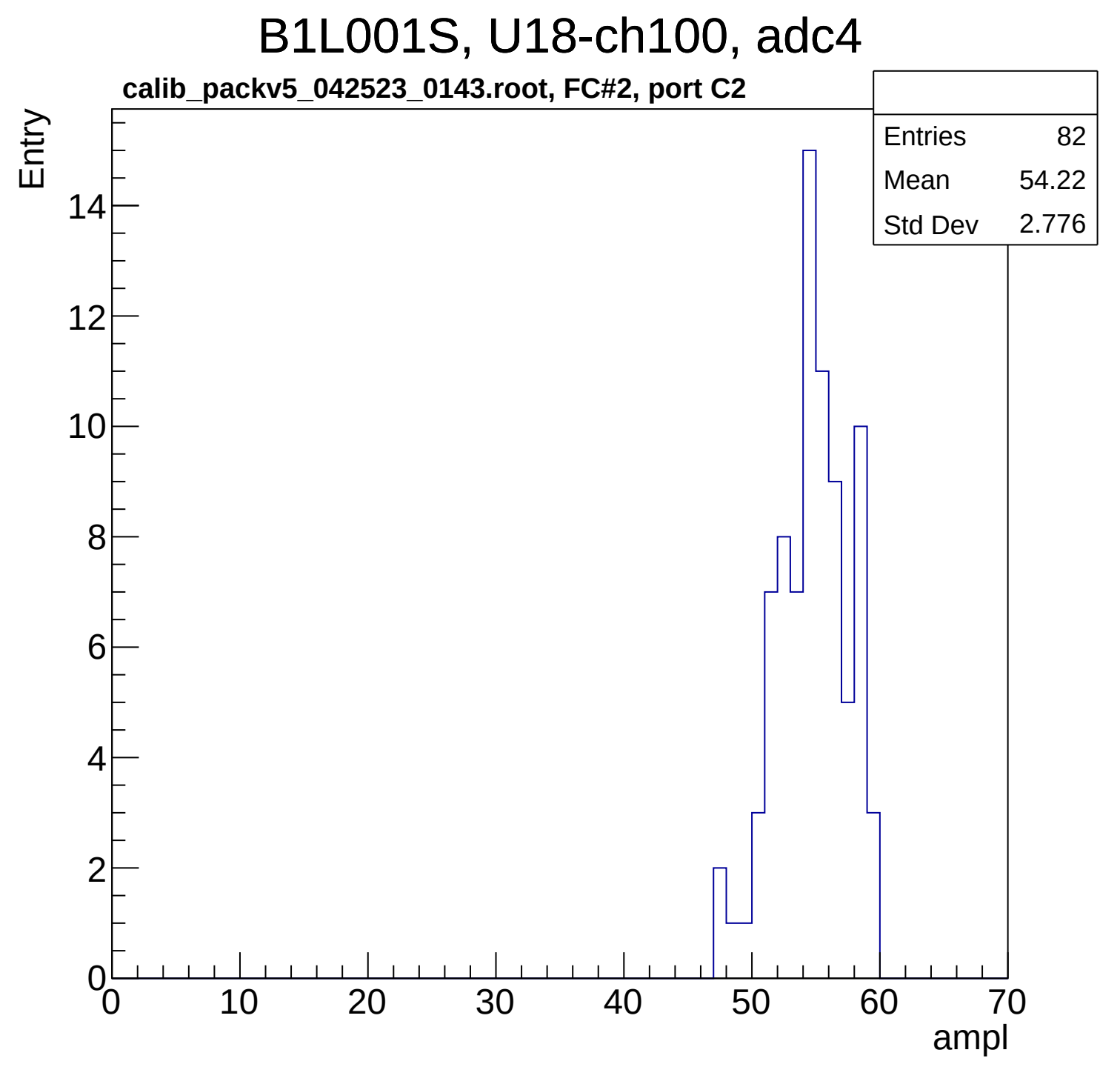

B1L001S, U18-ch99, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 23
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

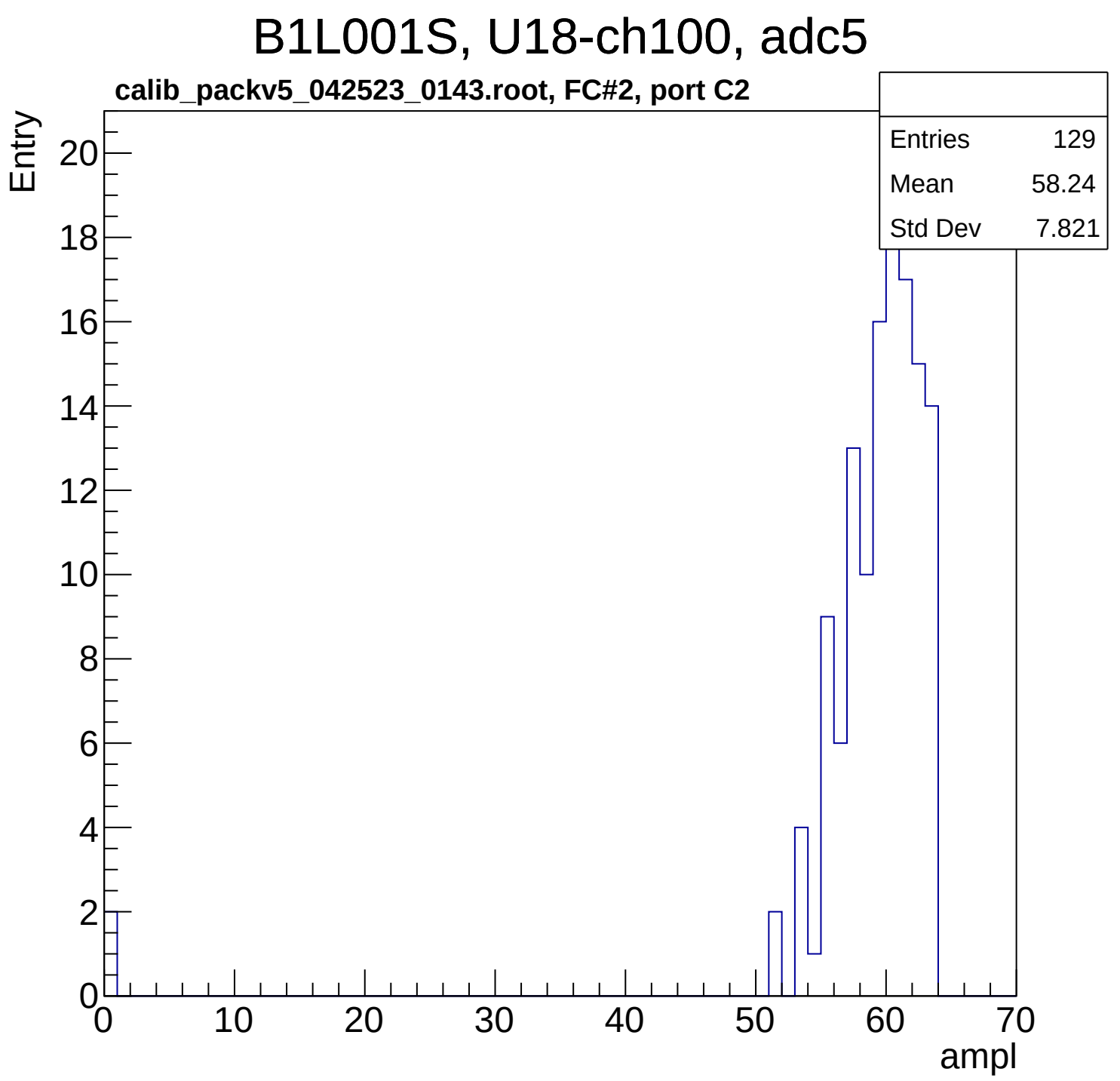

B1L001S, U18-ch100, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 123
Mean 29.07
Std Dev 3.216
Gaus mean : 29.4928
Gaus Width: 3.1565
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

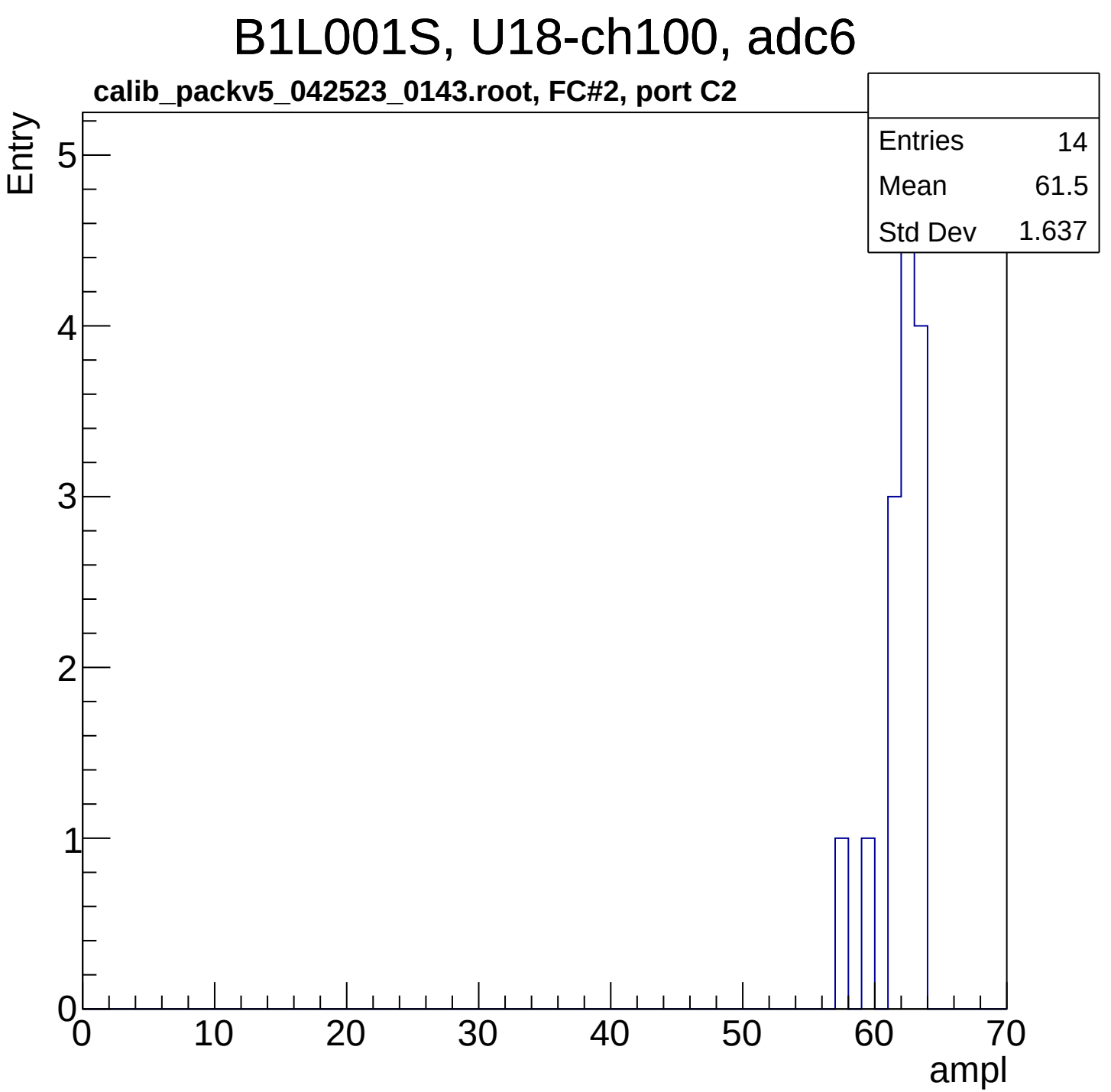

B1L001S, U18-ch100, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 133
Mean 35.7
Std Dev 3.535
Gaus mean : 36.0546
Gaus Width: 3.6105
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

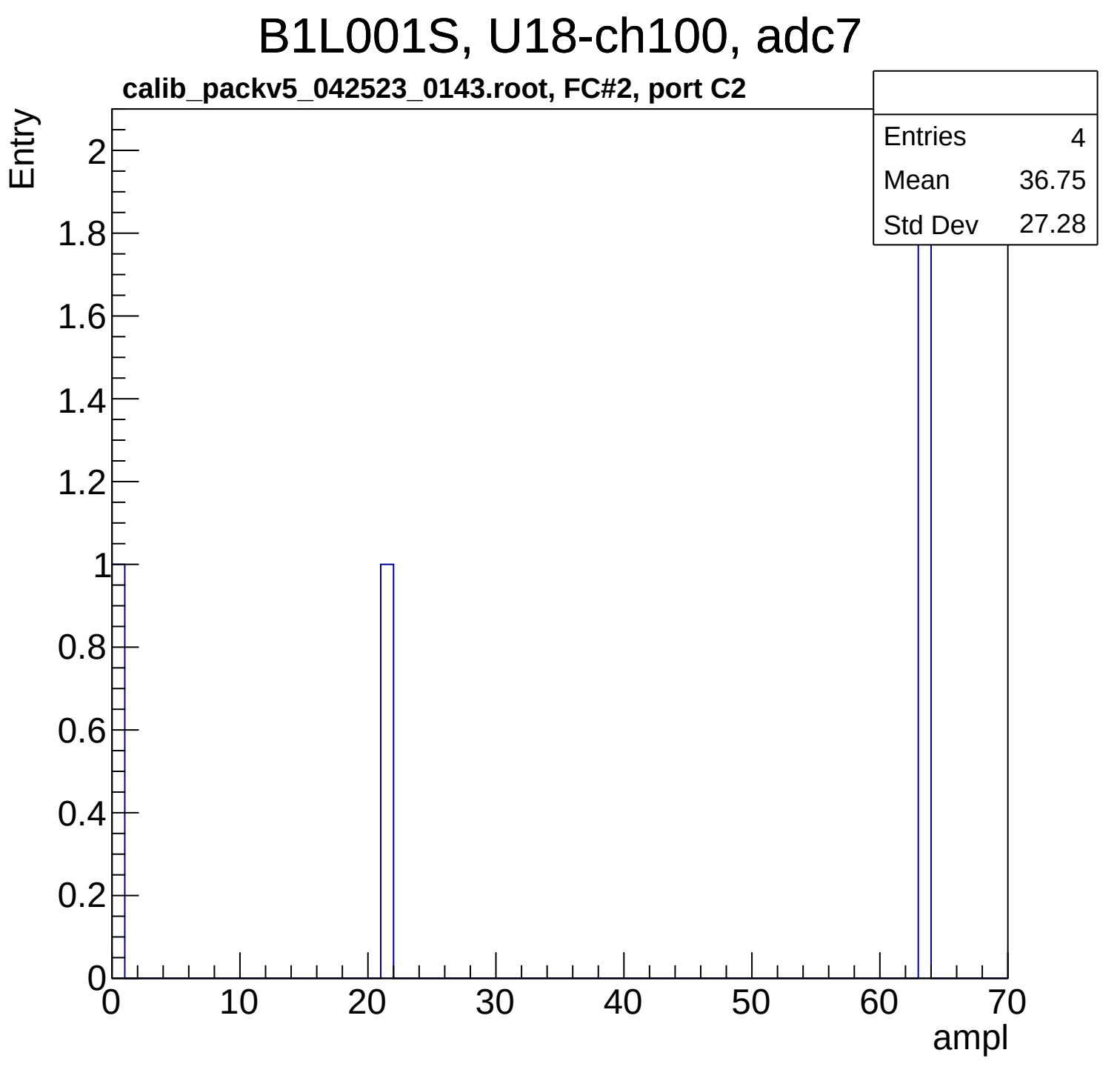

B1L001S, U18-ch100, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 136
Mean 41.83
Std Dev 3.637
Gaus mean : 42.4919
Gaus Width: 3.7046
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

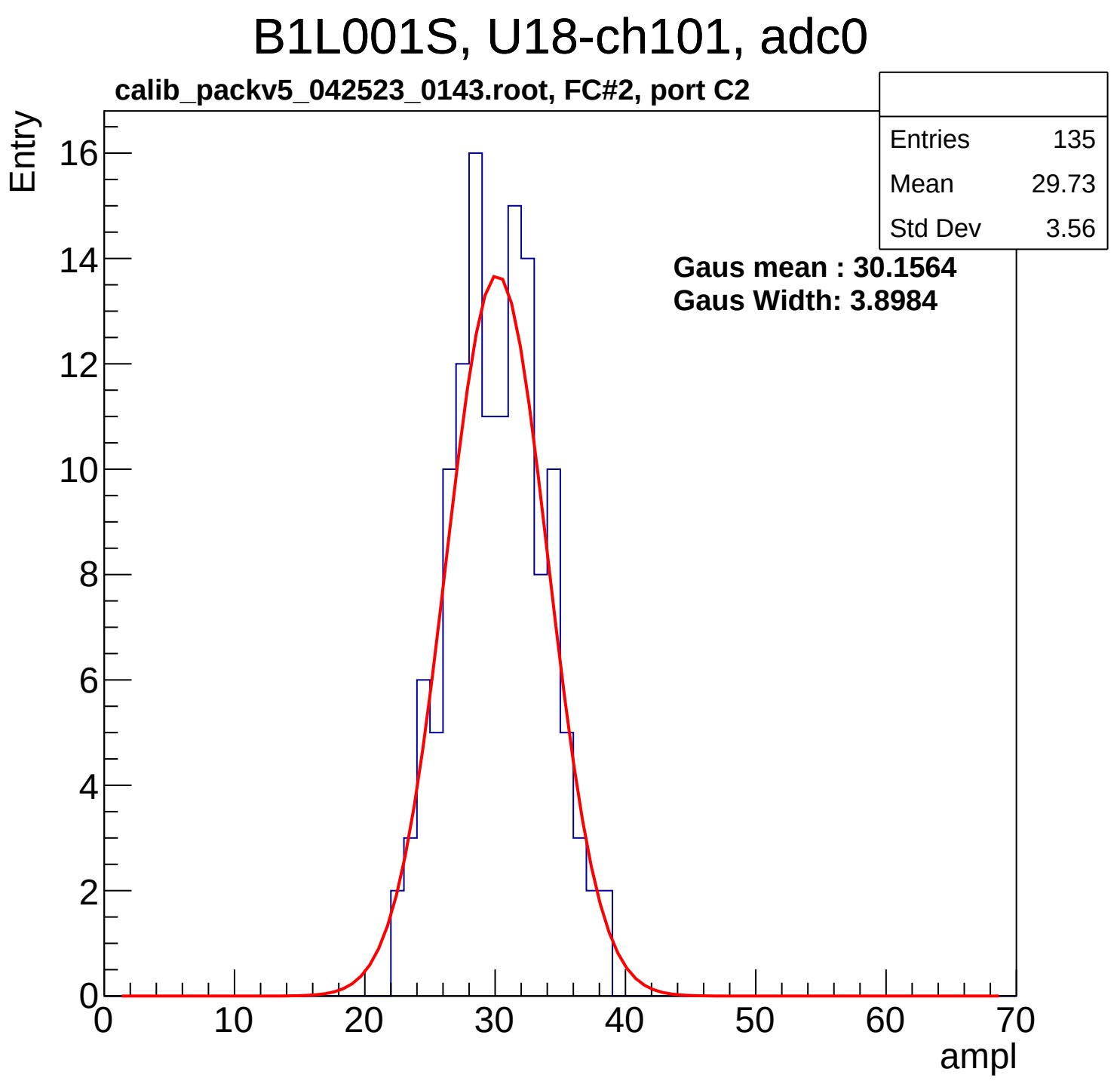

B1L001S, U18-ch100, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 135
Mean 48.86
Std Dev 3.393
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

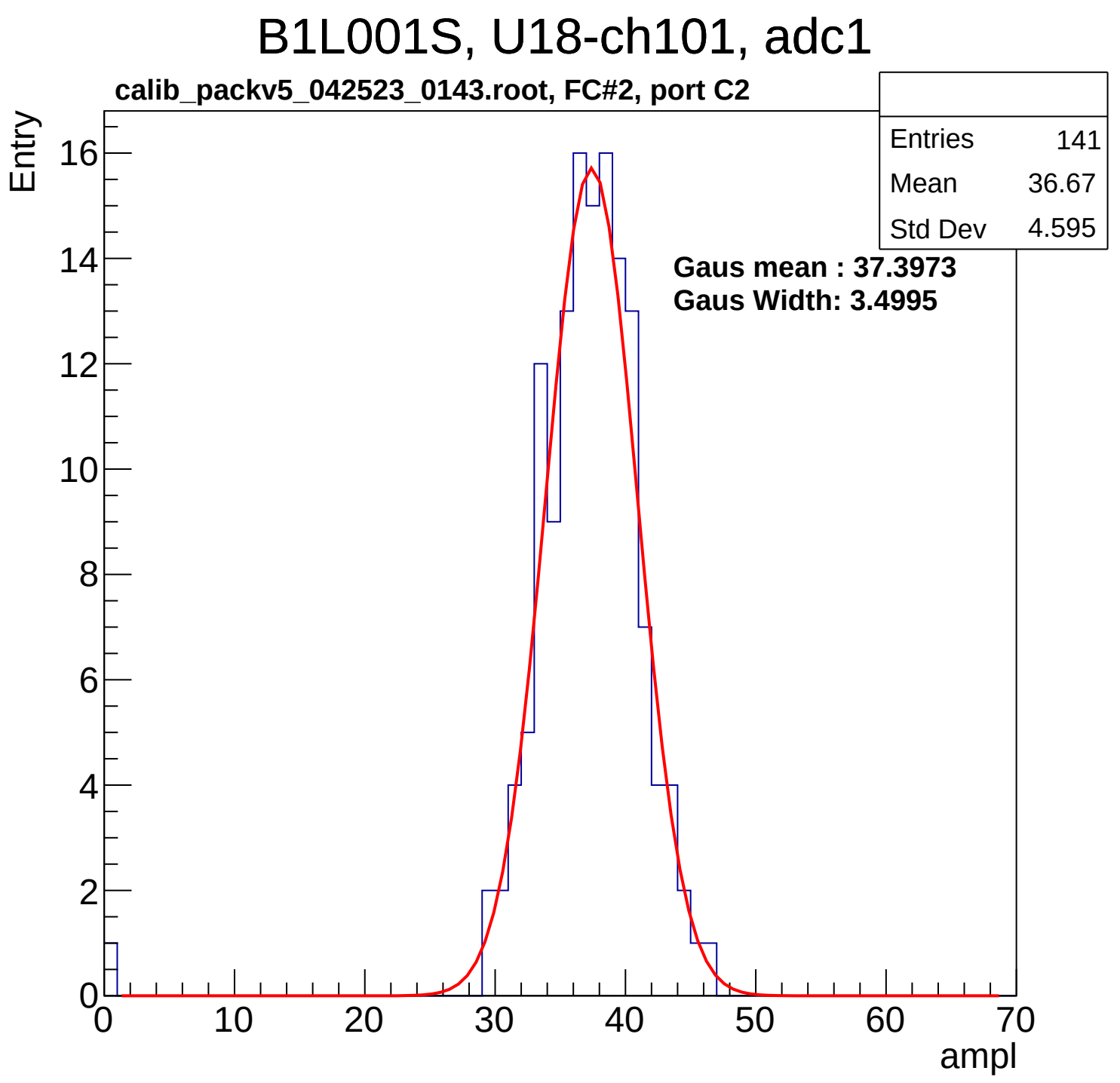

B1L001S, U18-ch100, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 82
Mean 54.22
Std Dev 2.776
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl

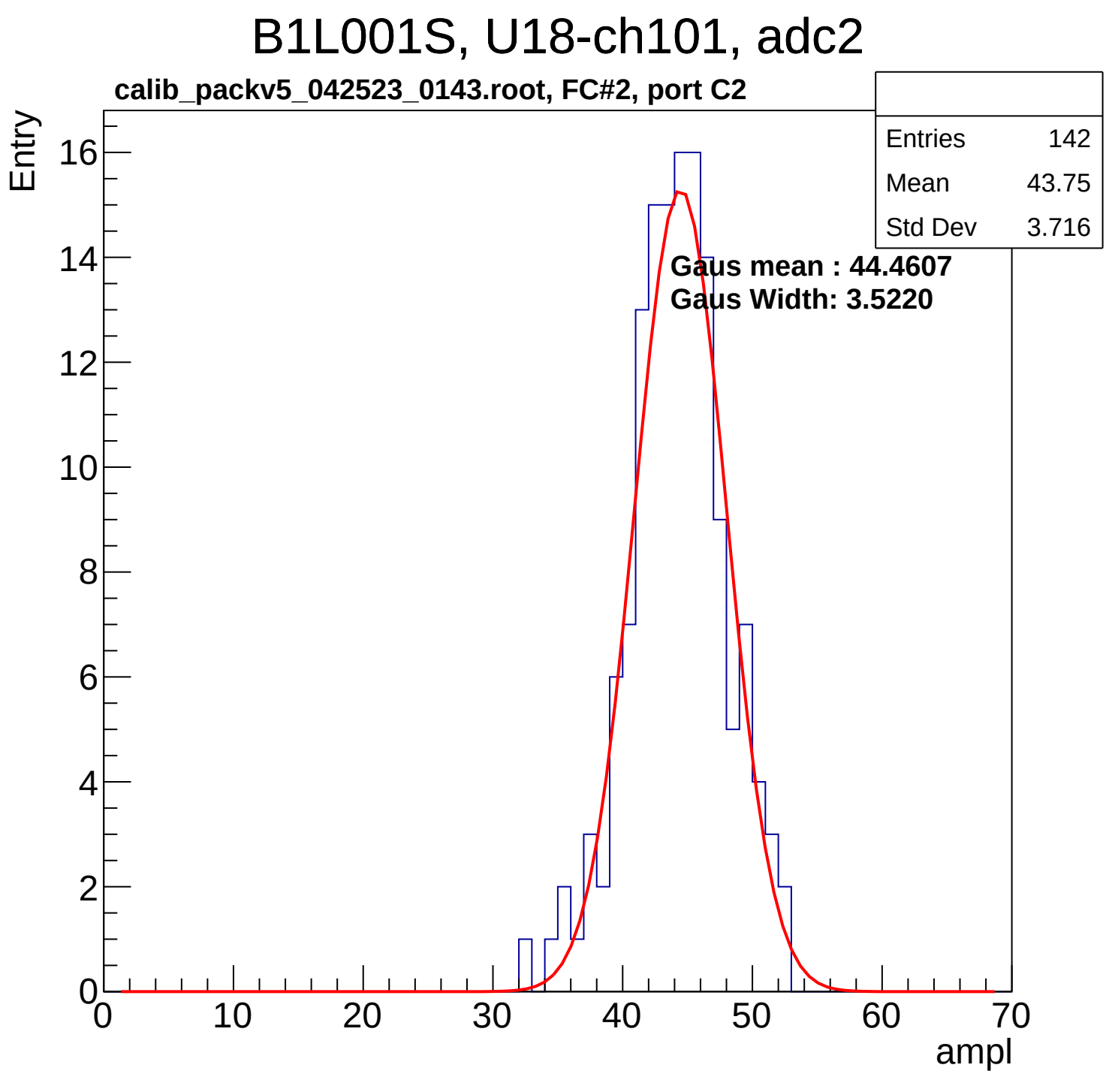

B1L001S, U18-ch100, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 129
Mean 58.24
Std Dev 7.821
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

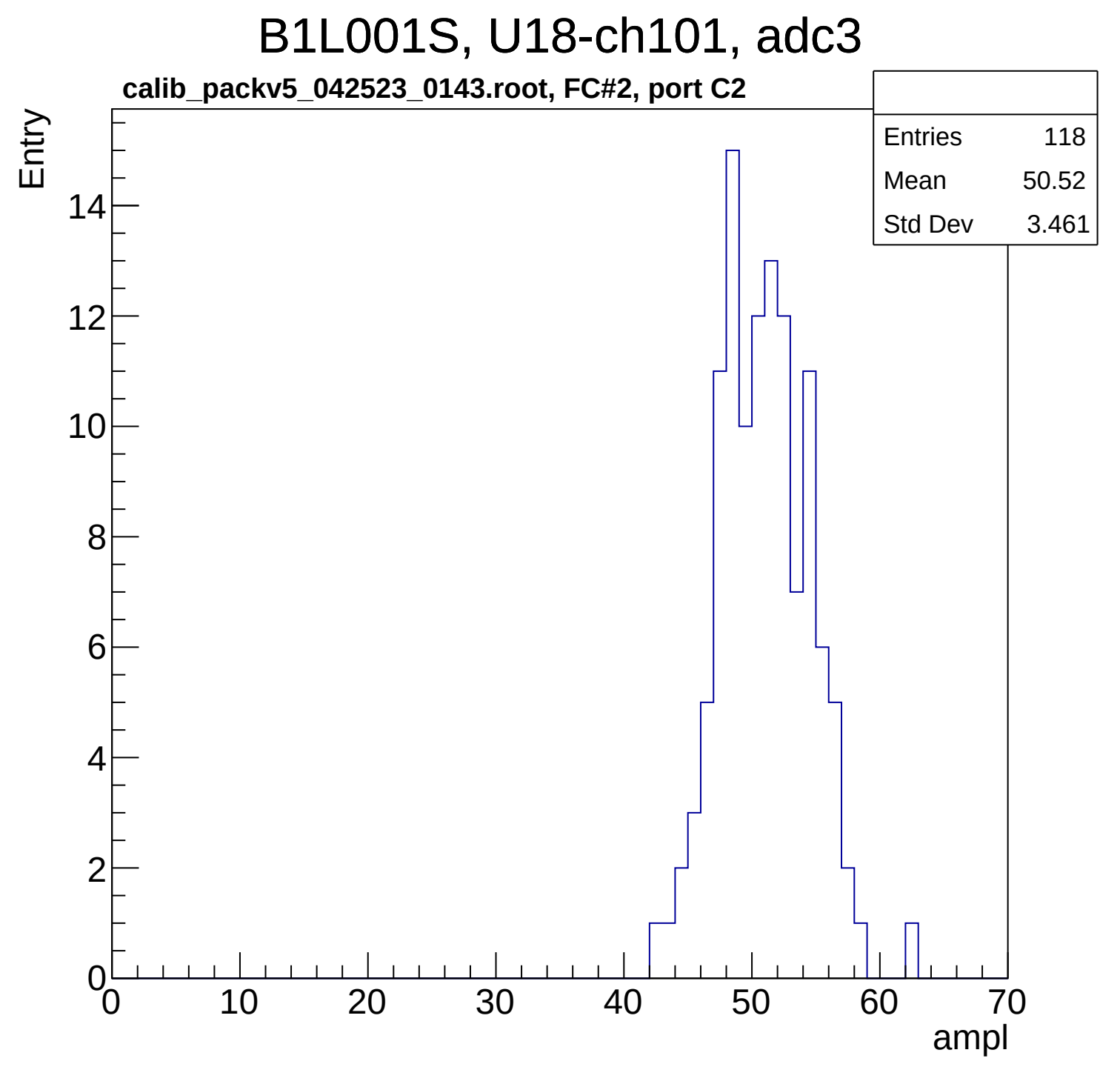

B1L001S, U18-ch100, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 14
Mean 61.5
Std Dev 1.637
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

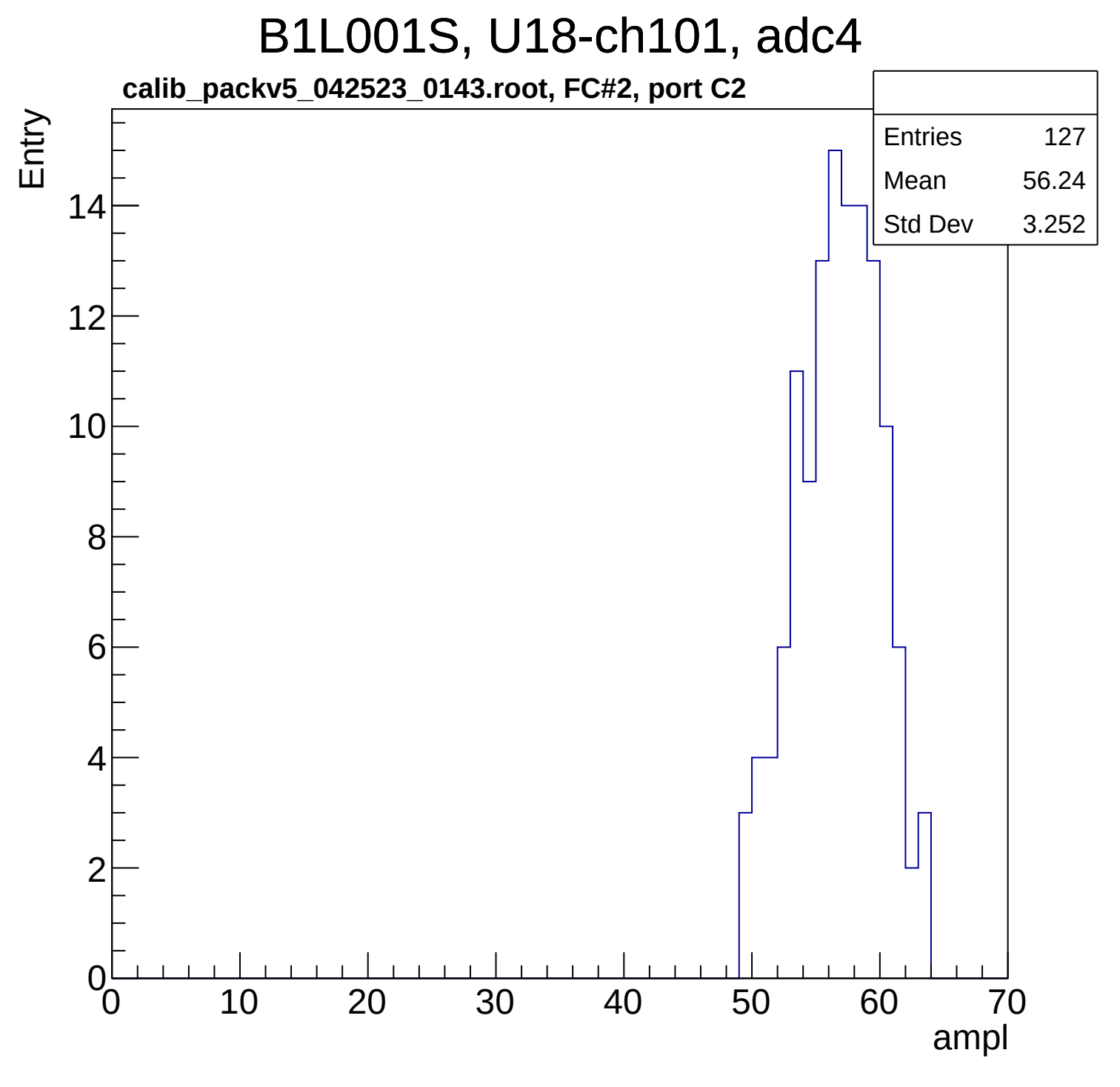

B1L001S, U18-ch100, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 4
Mean 36.75
Std Dev 27.28
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

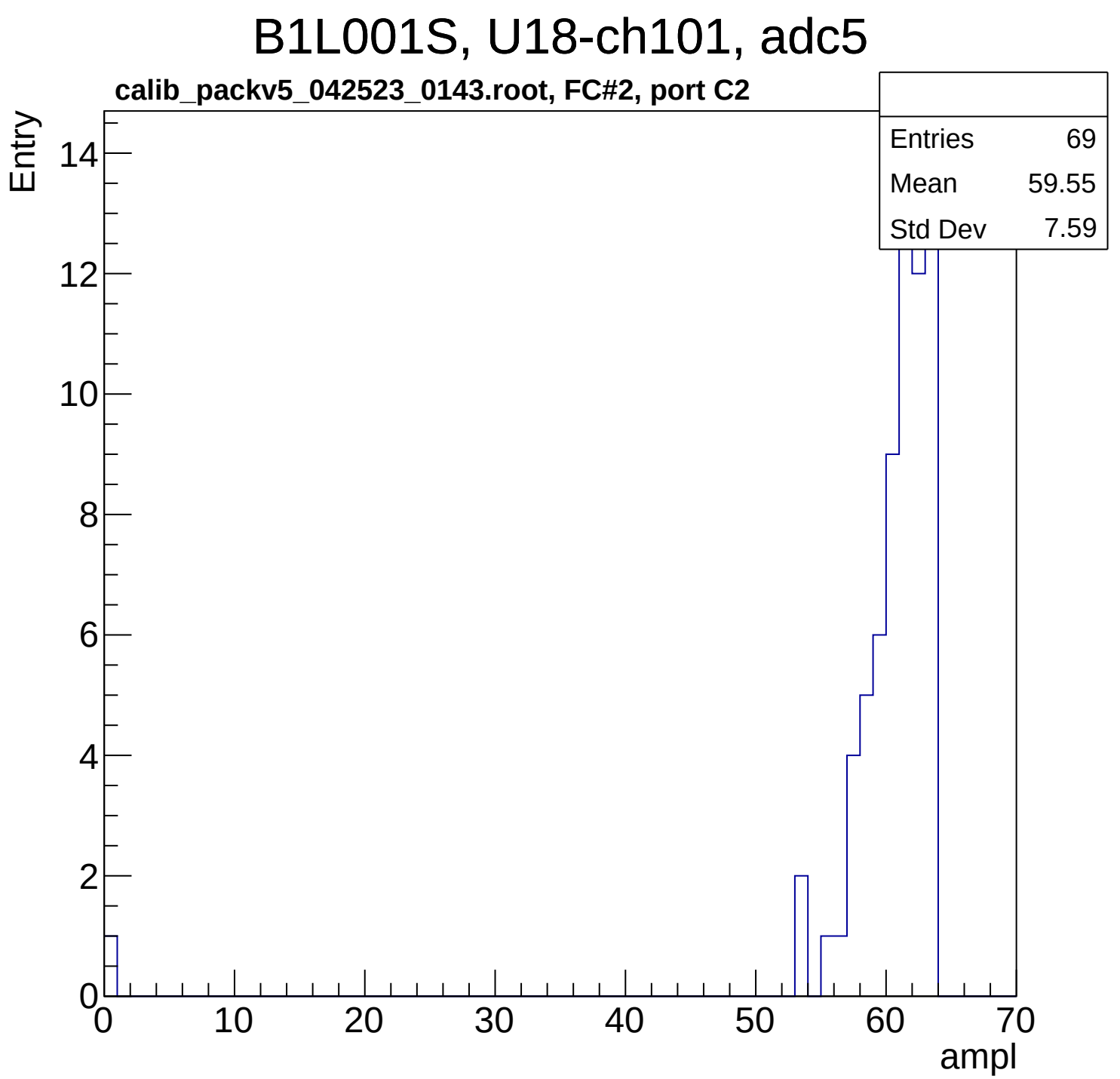

B1L001S, U18-ch101, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 135
Mean 29.73
Std Dev 3.56
Gaus mean : 30.1564
Gaus Width: 3.8984
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

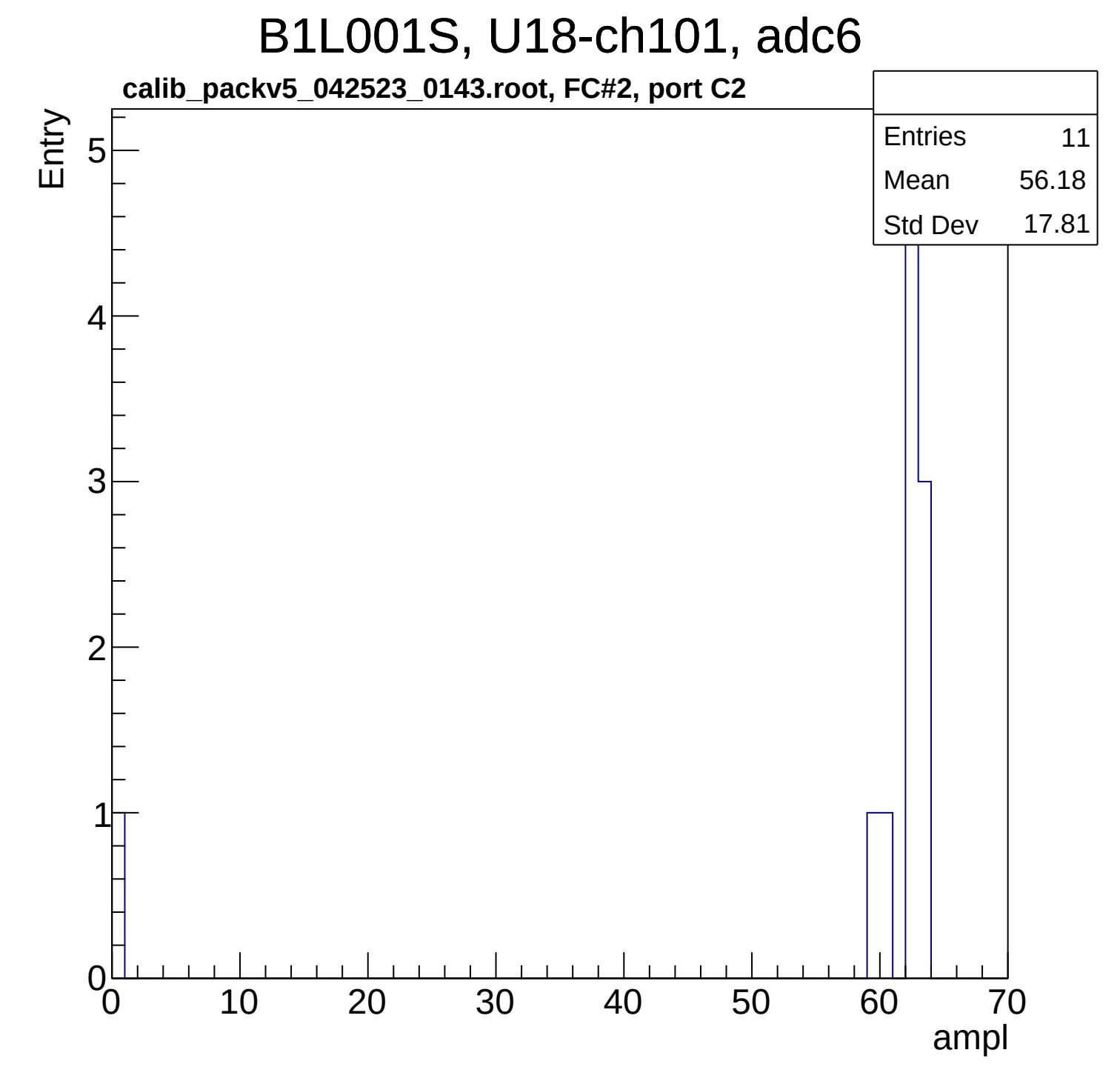

B1L001S, U18-ch101, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 141
Mean 36.67
Std Dev 4.595
Gaus mean : 37.3973
Gaus Width: 3.4995
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

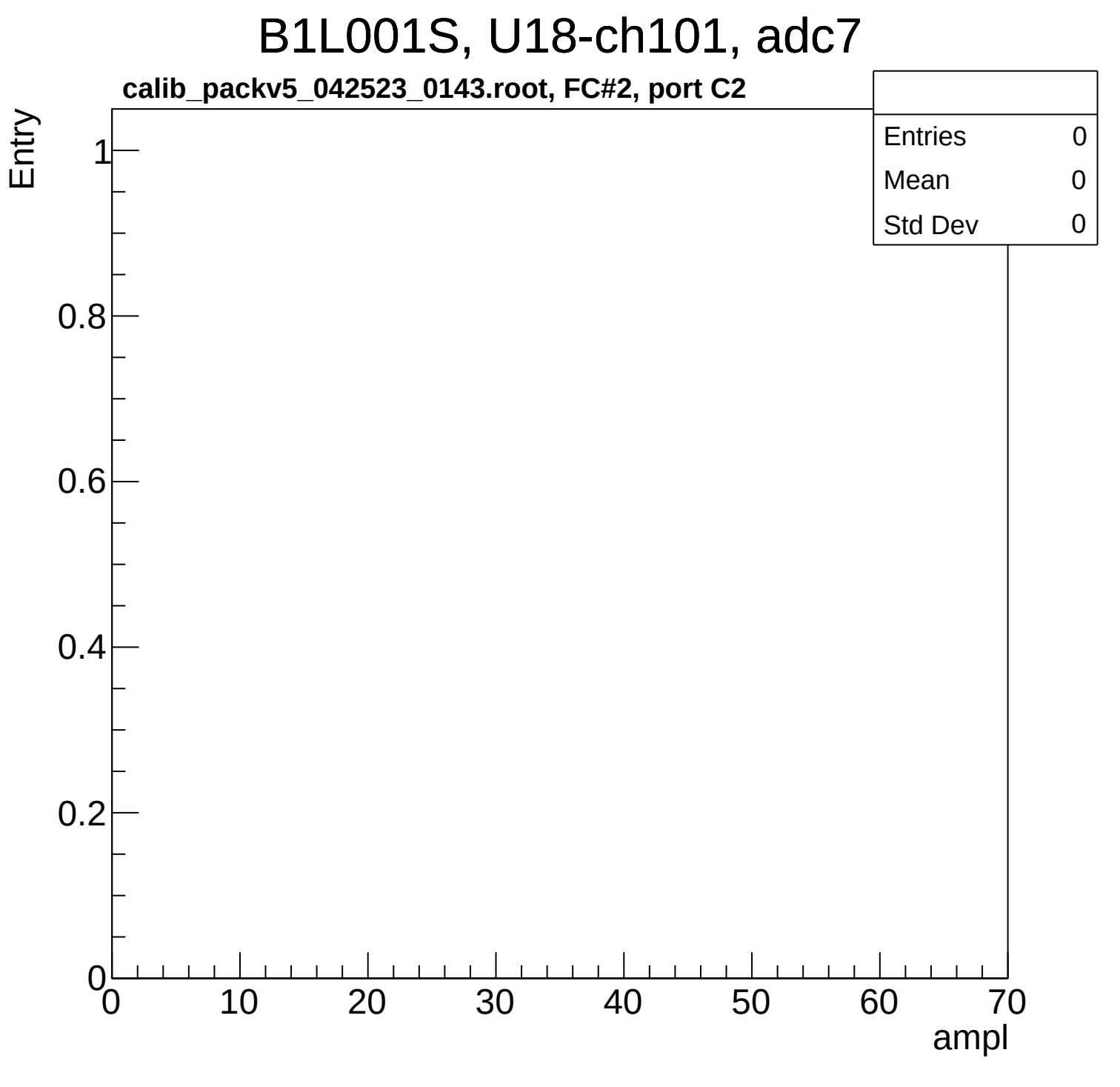

B1L001S, U18-ch101, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 142
Mean 43.75
Std Dev 3.716
Gaus mean : 44.4607
Gaus Width: 3.5220
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

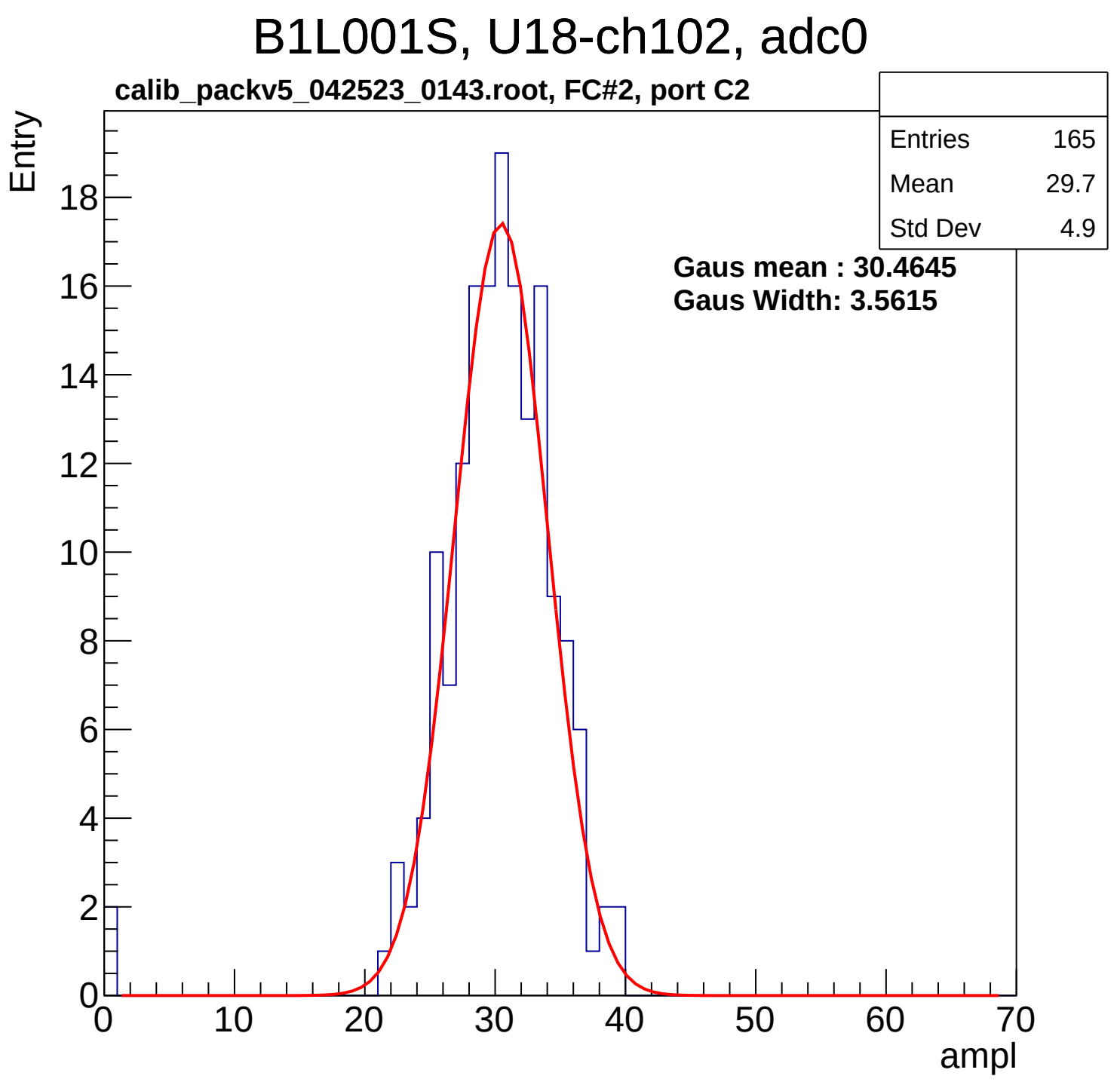

B1L001S, U18-ch101, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 118
Mean 50.52
Std Dev 3.461
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl

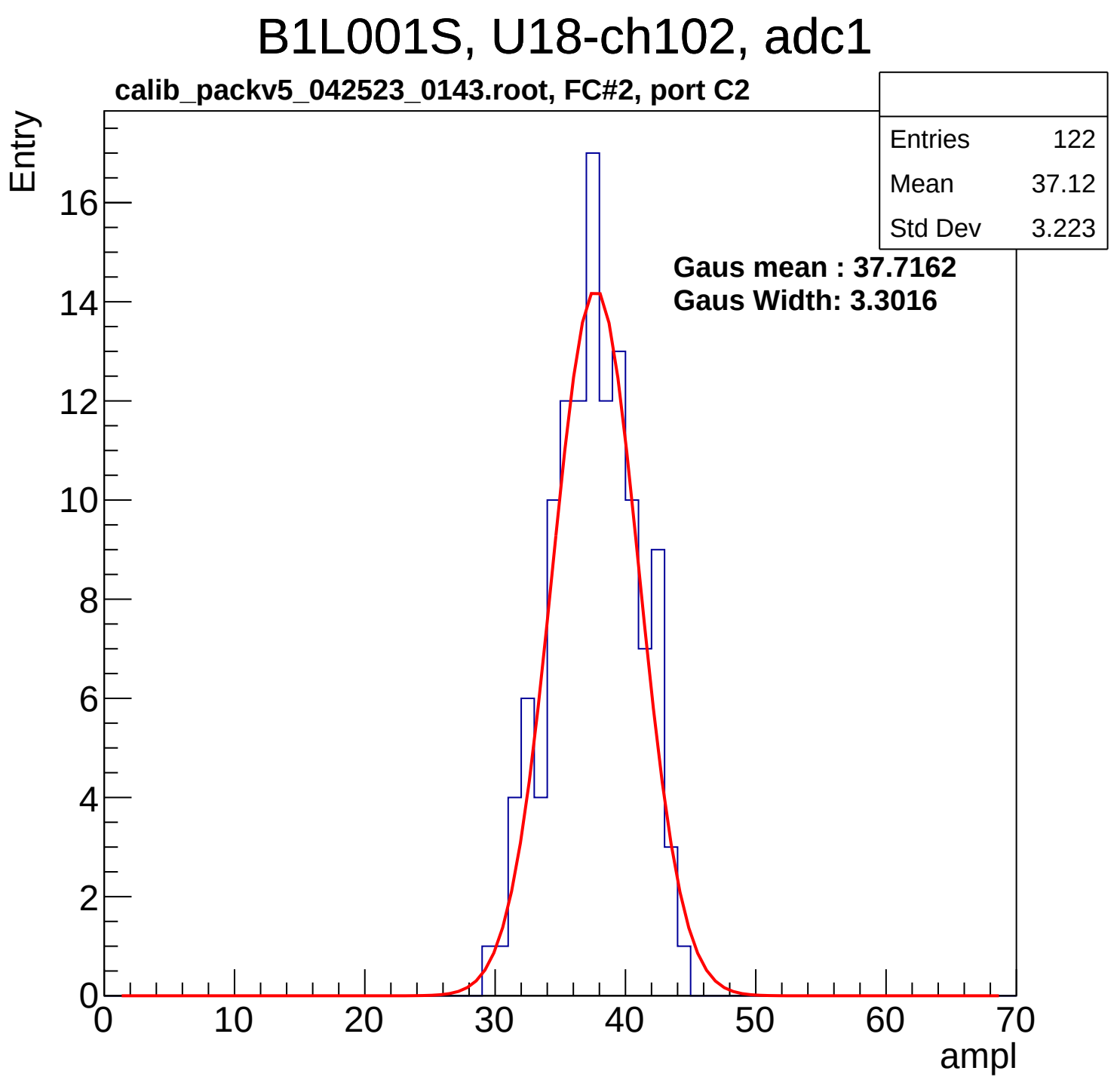

B1L001S, U18-ch101, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 127
Mean 56.24
Std Dev 3.252
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

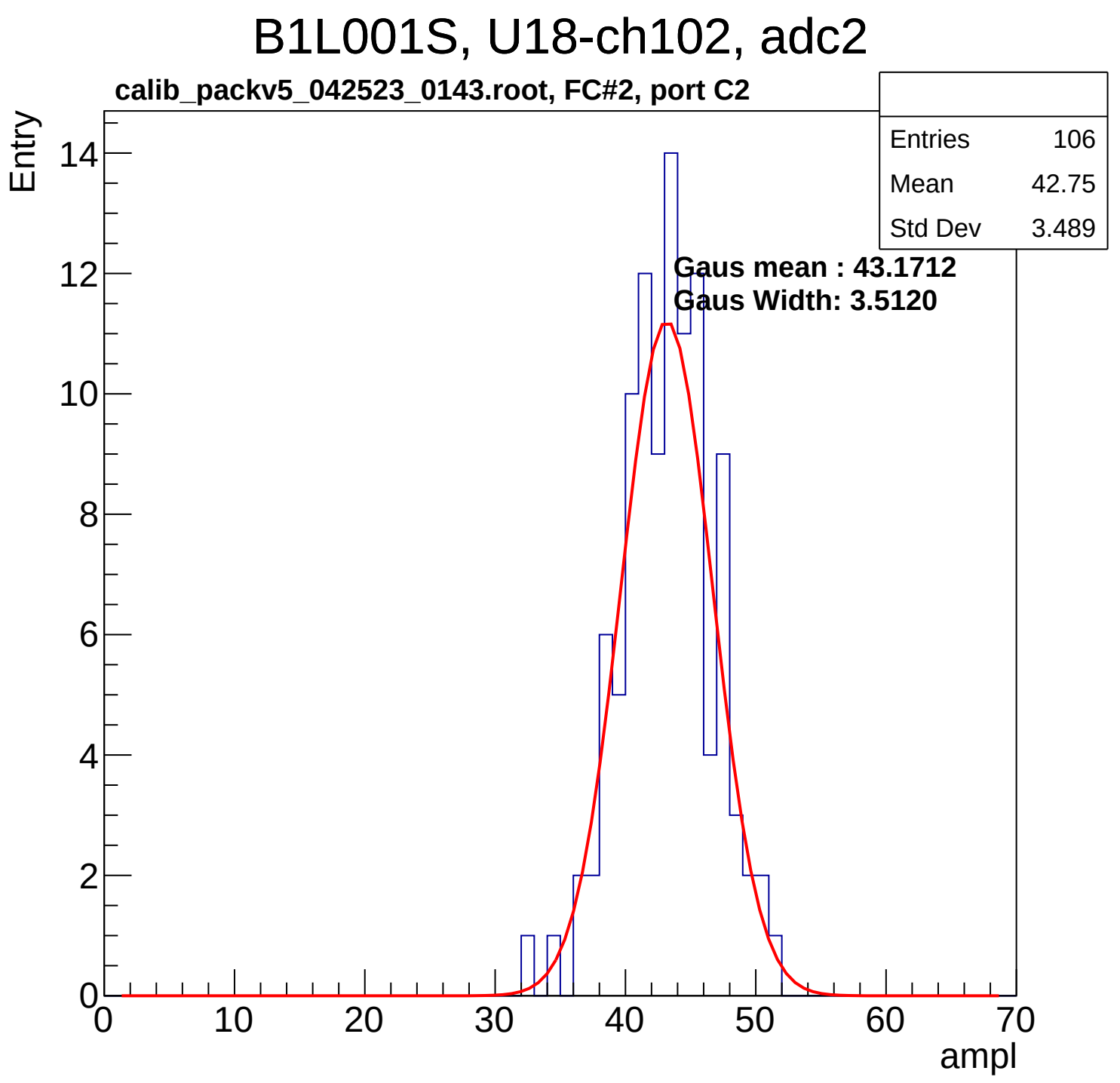

B1L001S, U18-ch101, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 69
Mean 59.55
Std Dev 7.59
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

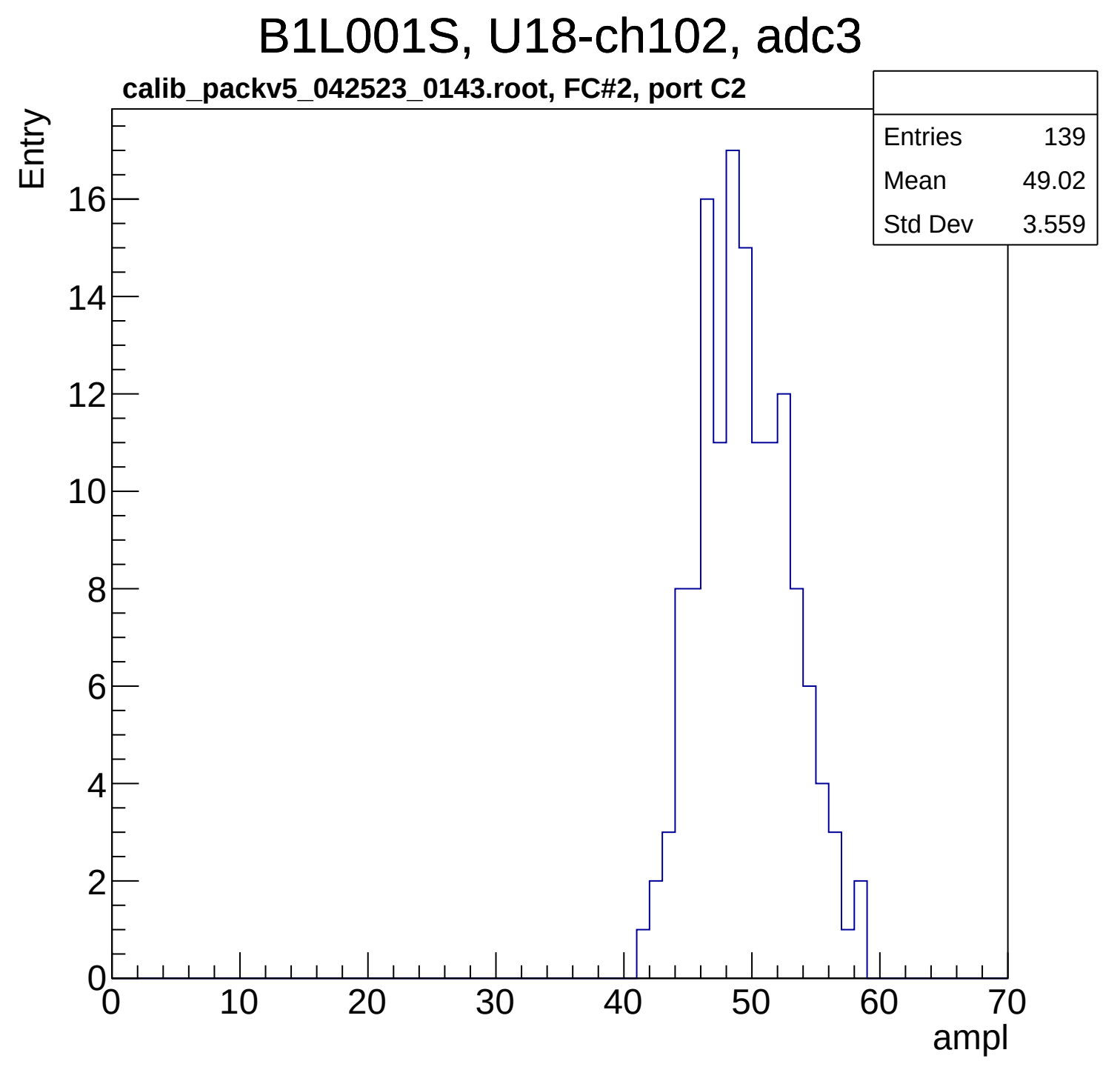

B1L001S, U18-ch101, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 11
Mean 56.18
Std Dev 17.81
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

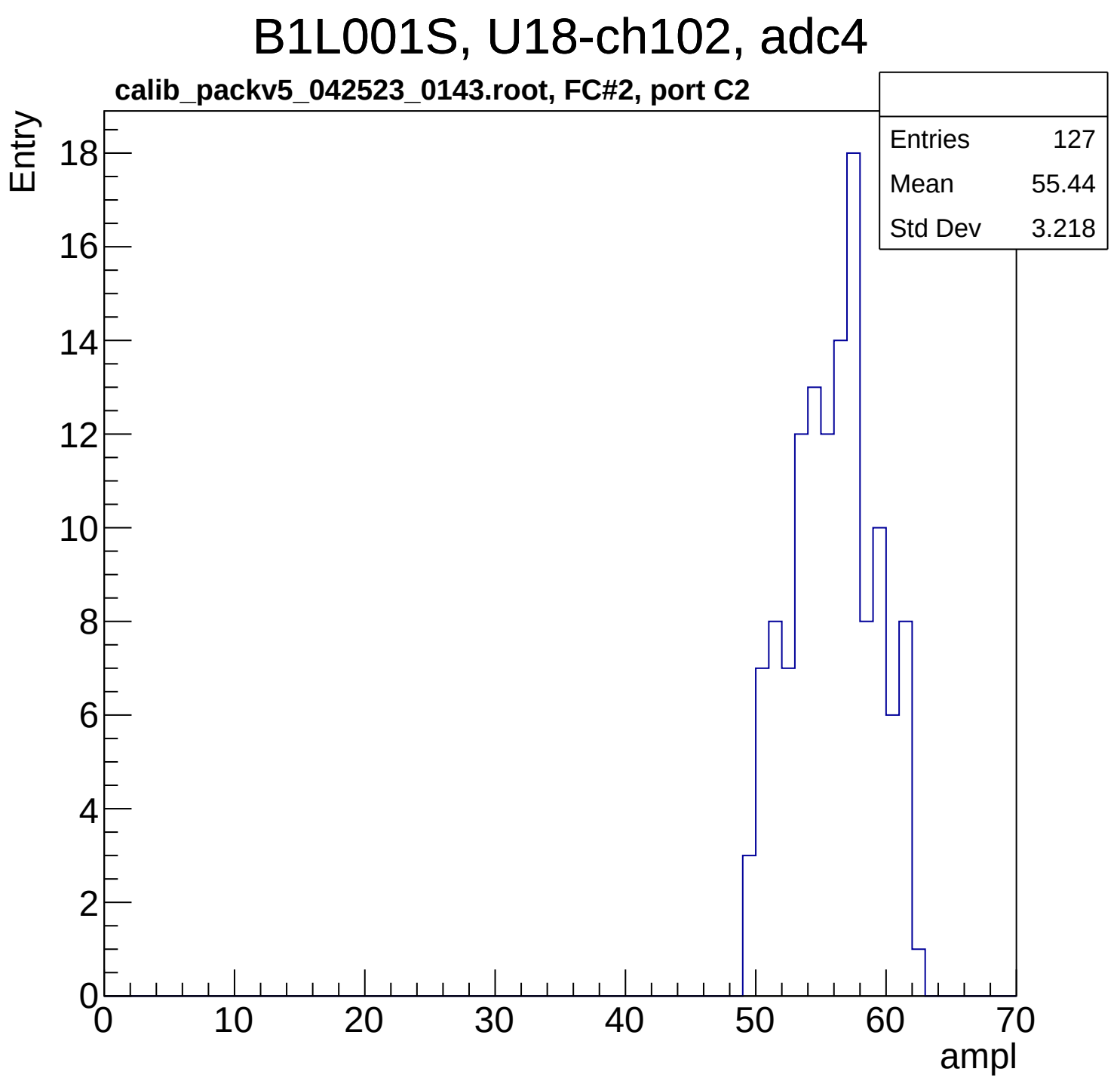

B1L001S, U18-ch101, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

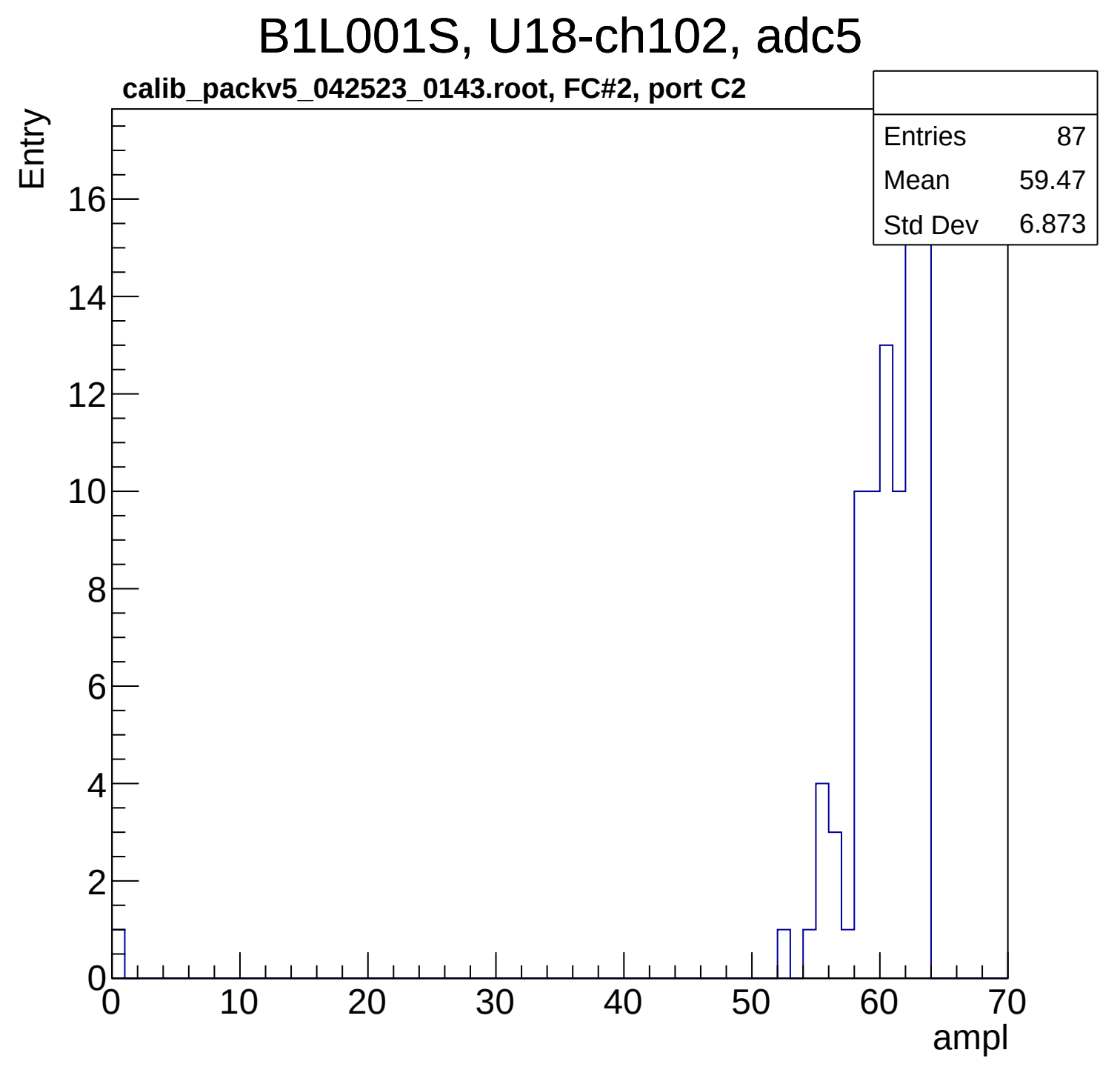

B1L001S, U18-ch102, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 165
Mean 29.7
Std Dev 4.9
Gaus mean : 30.4645
Gaus Width: 3.5615
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

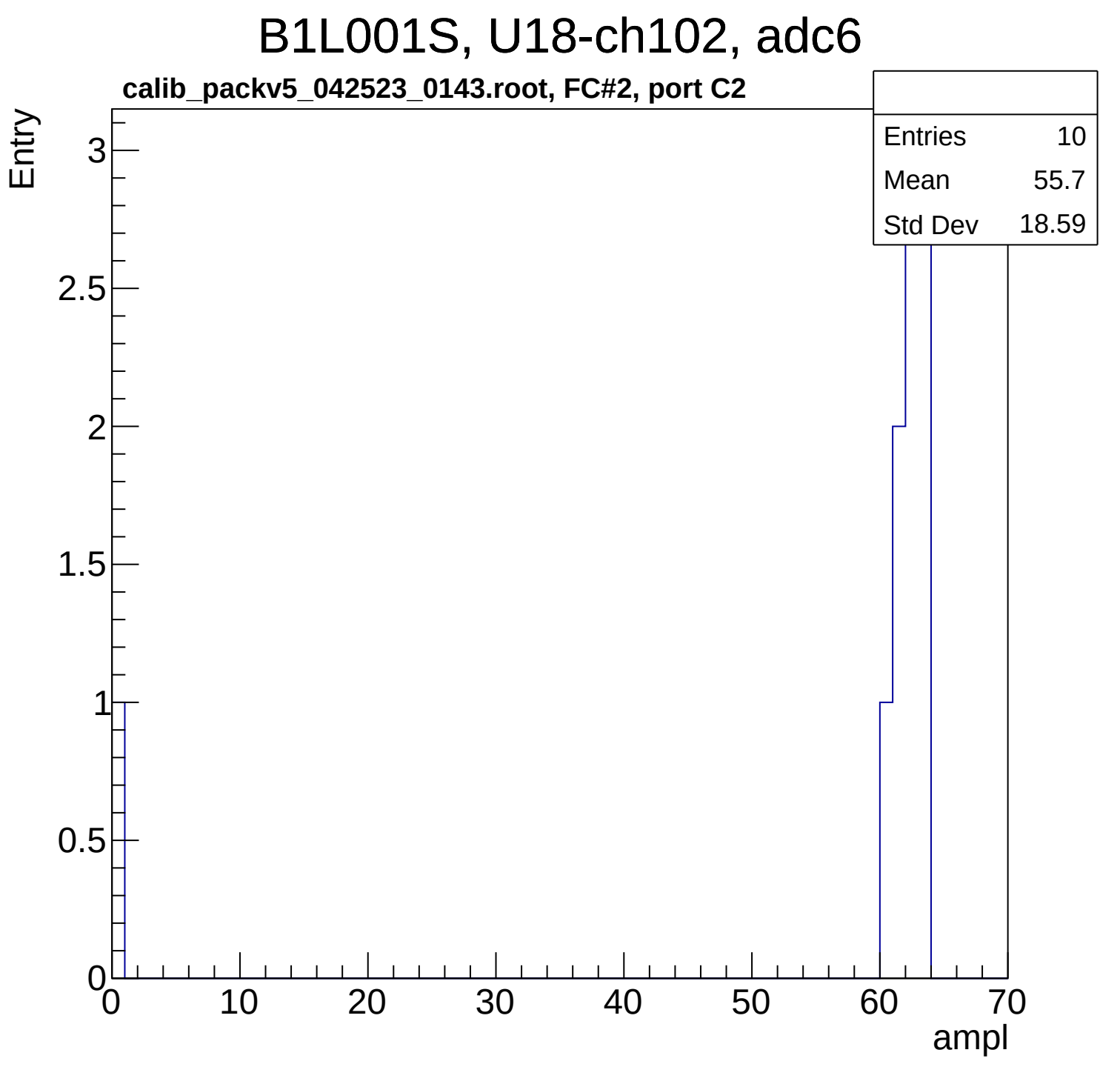

B1L001S, U18-ch102, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 122
Mean 37.12
Std Dev 3.223
Gaus mean : 37.7162
Gaus Width: 3.3016
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

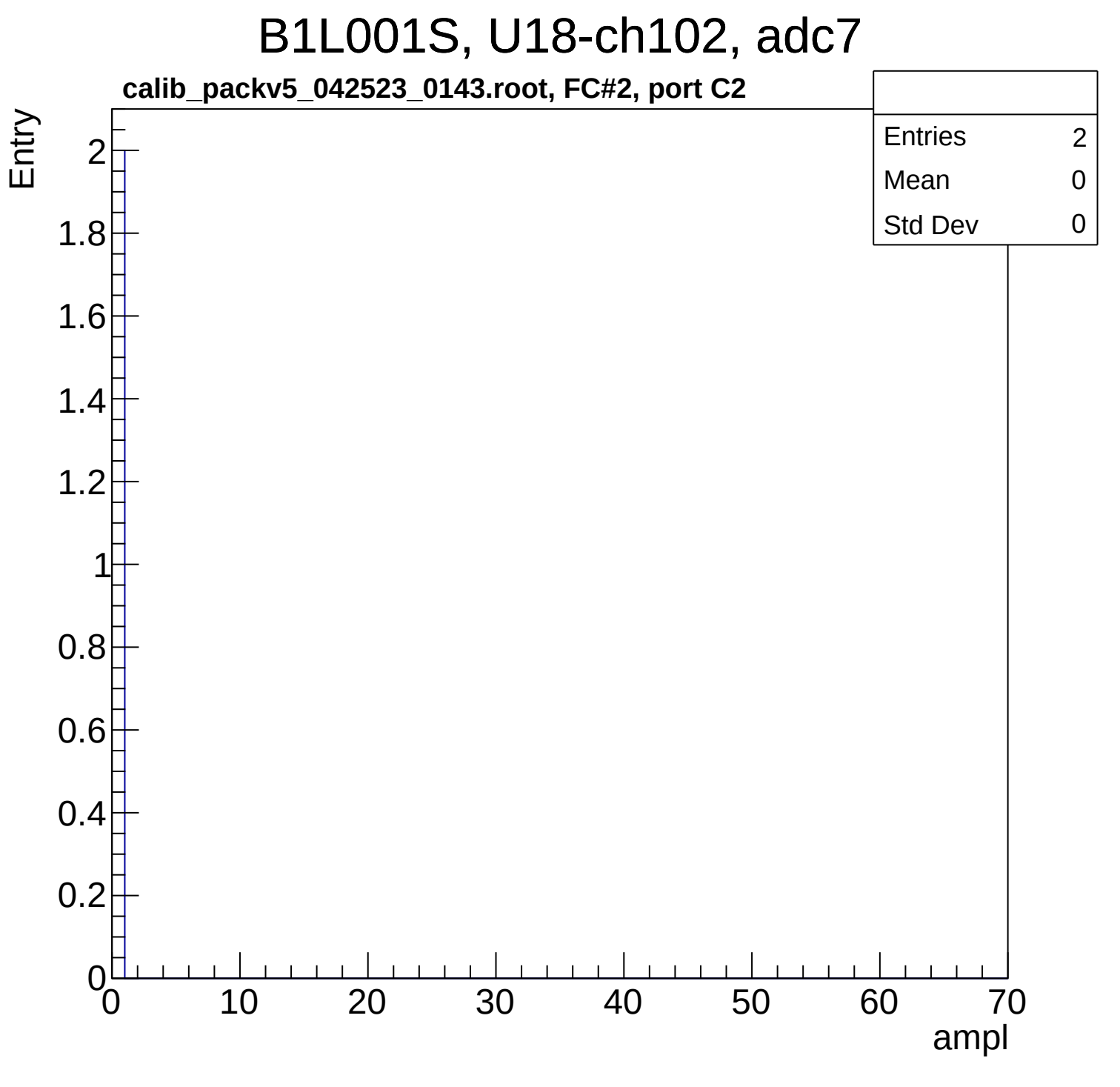

B1L001S, U18-ch102, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 106
Mean 42.75
Std Dev 3.489
Gaus mean : 43.1712
Gaus Width: 3.5120
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

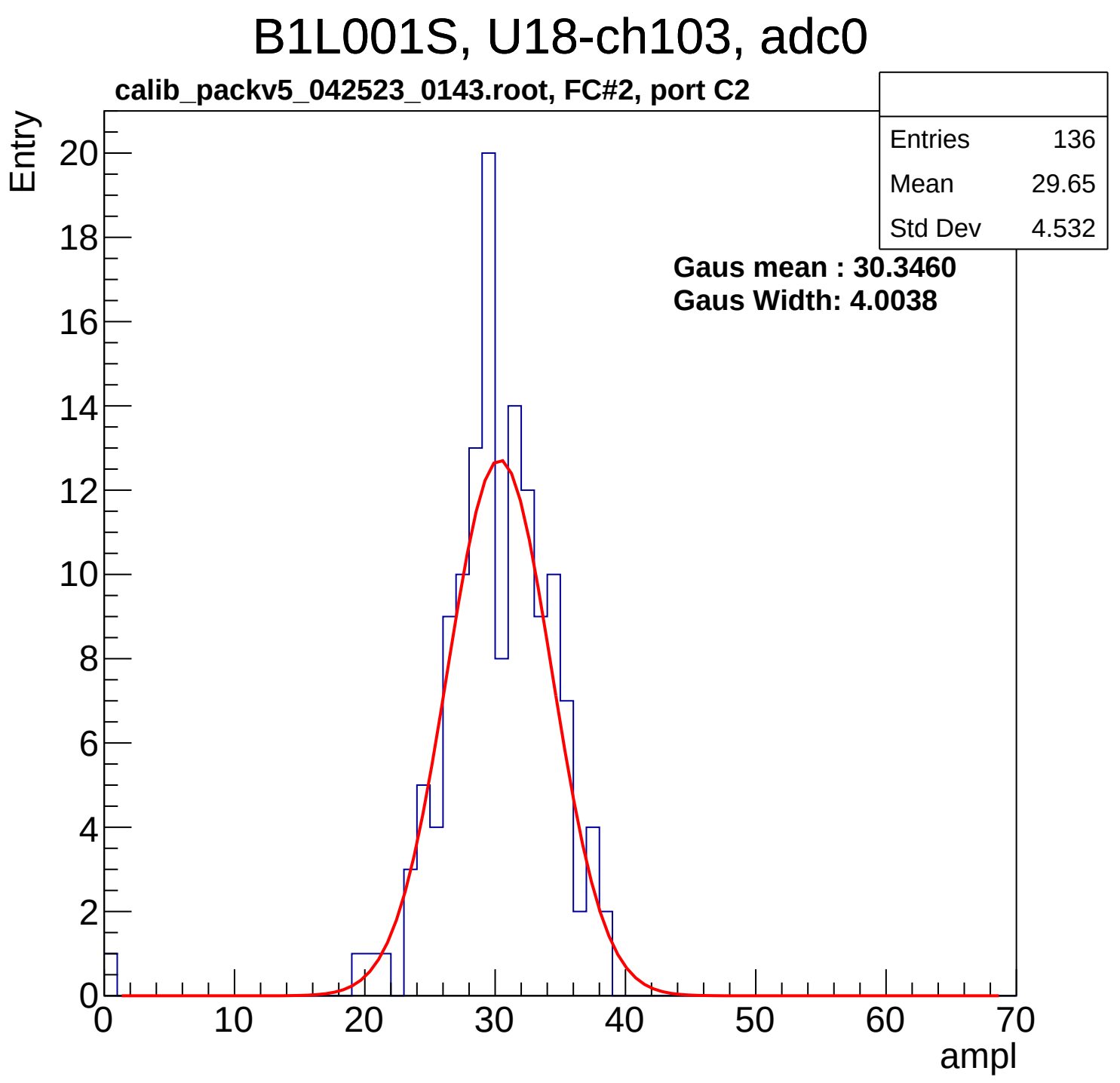

B1L001S, U18-ch102, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 139
Mean 49.02
Std Dev 3.559
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

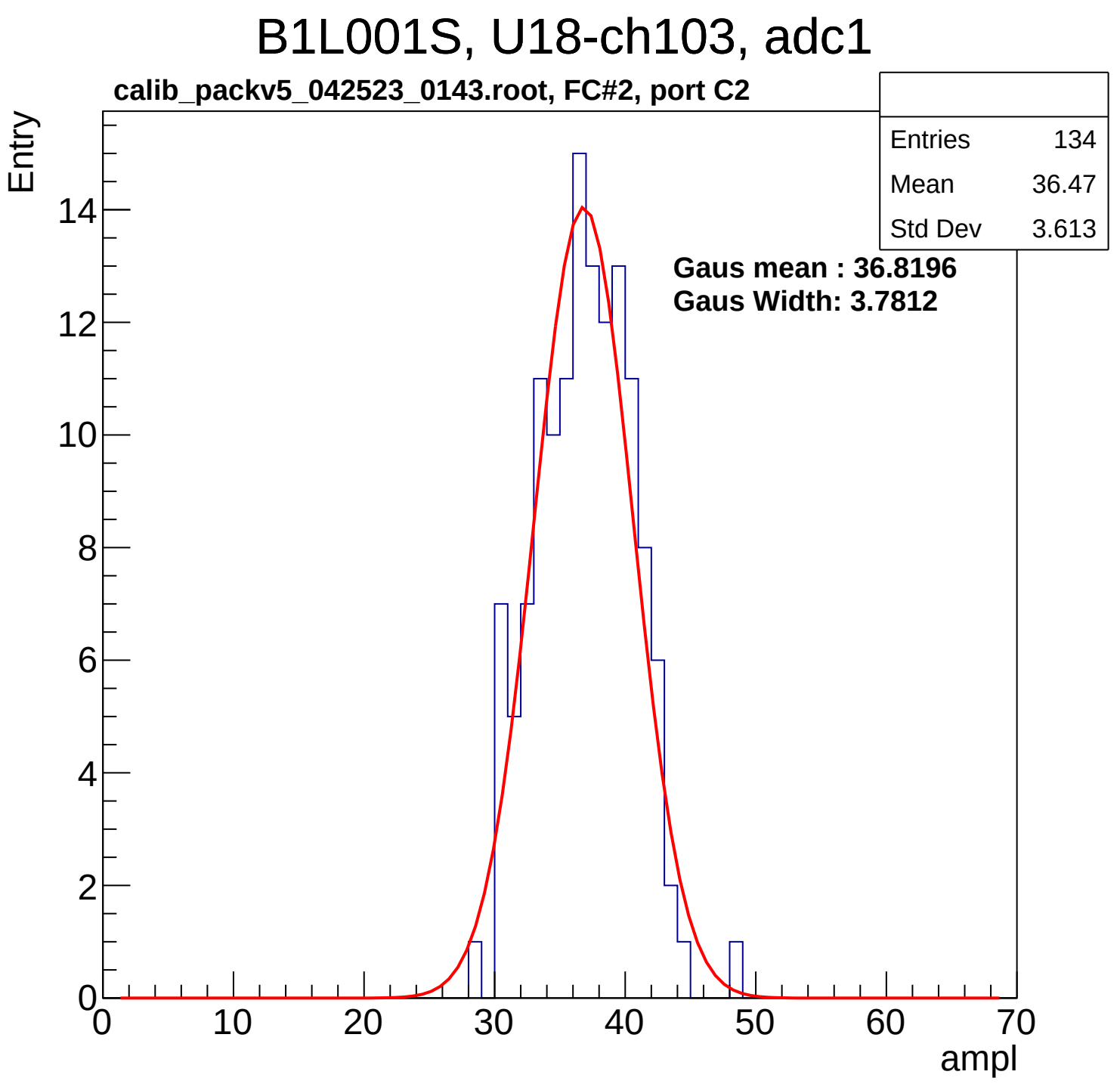

B1L001S, U18-ch102, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 127
Mean 55.44
Std Dev 3.218
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

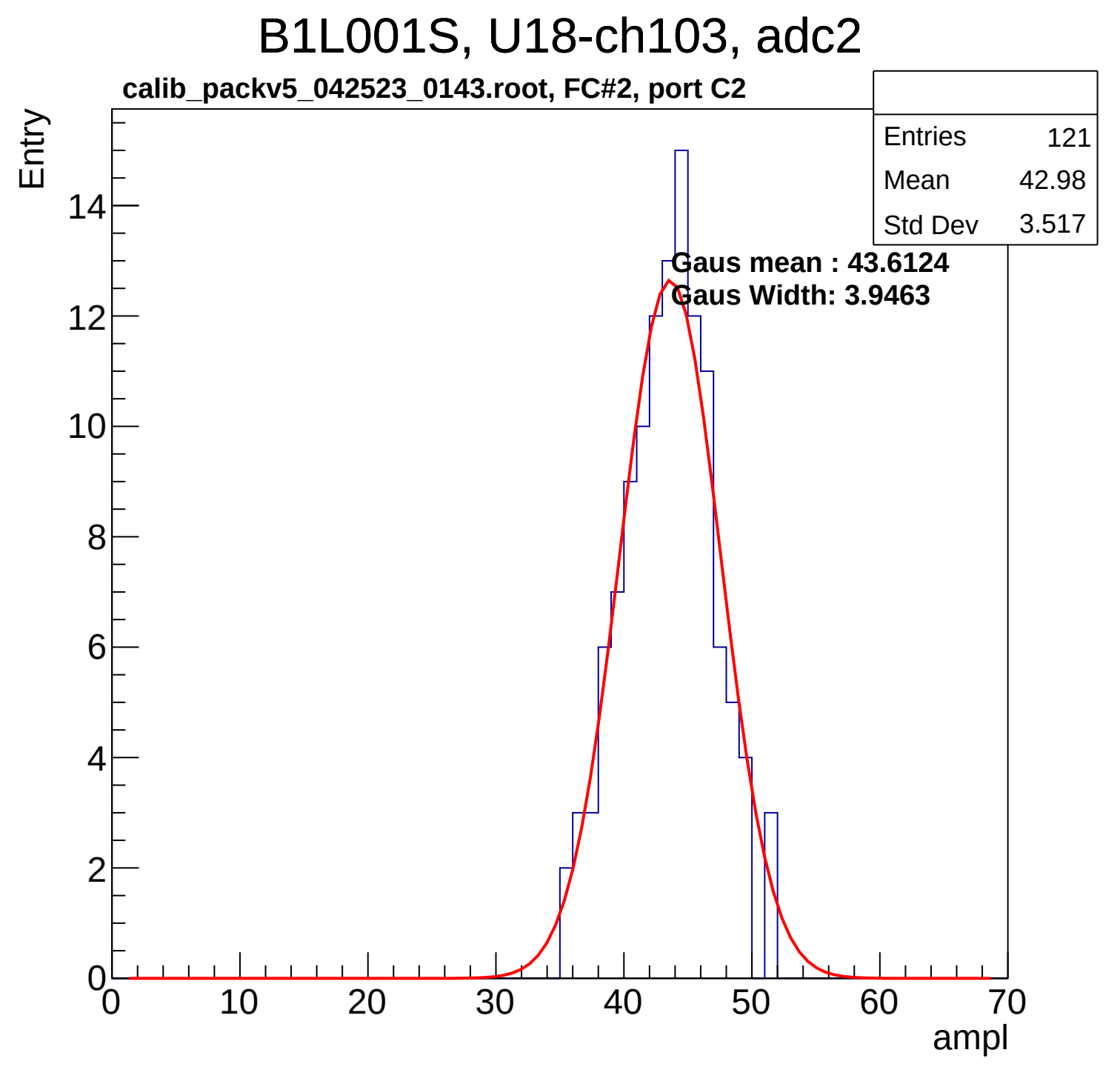

B1L001S, U18-ch102, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 87
Mean 59.47
Std Dev 6.873
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

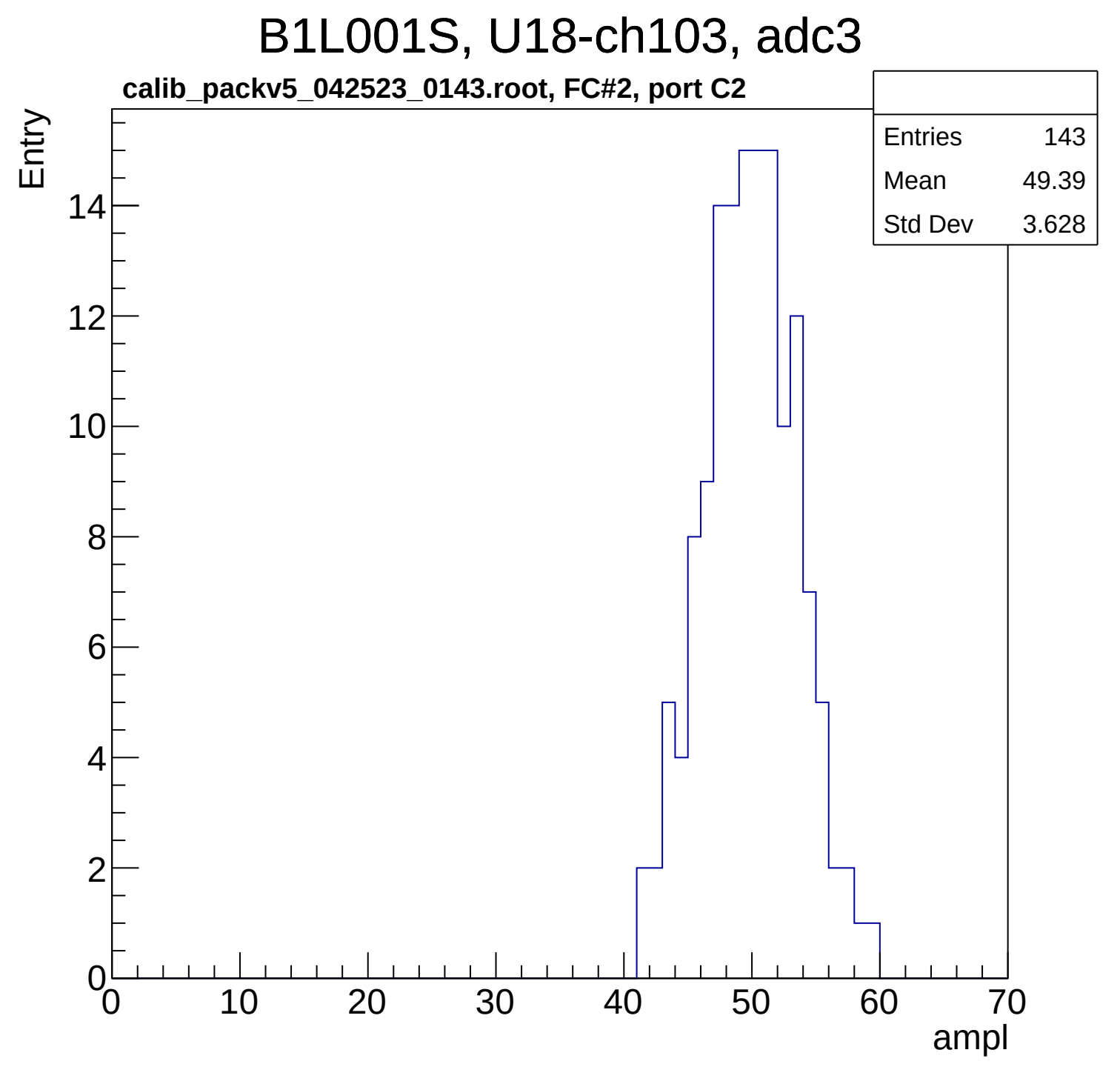

B1L001S, U18-ch102, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 10
Mean 55.7
Std Dev 18.59
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

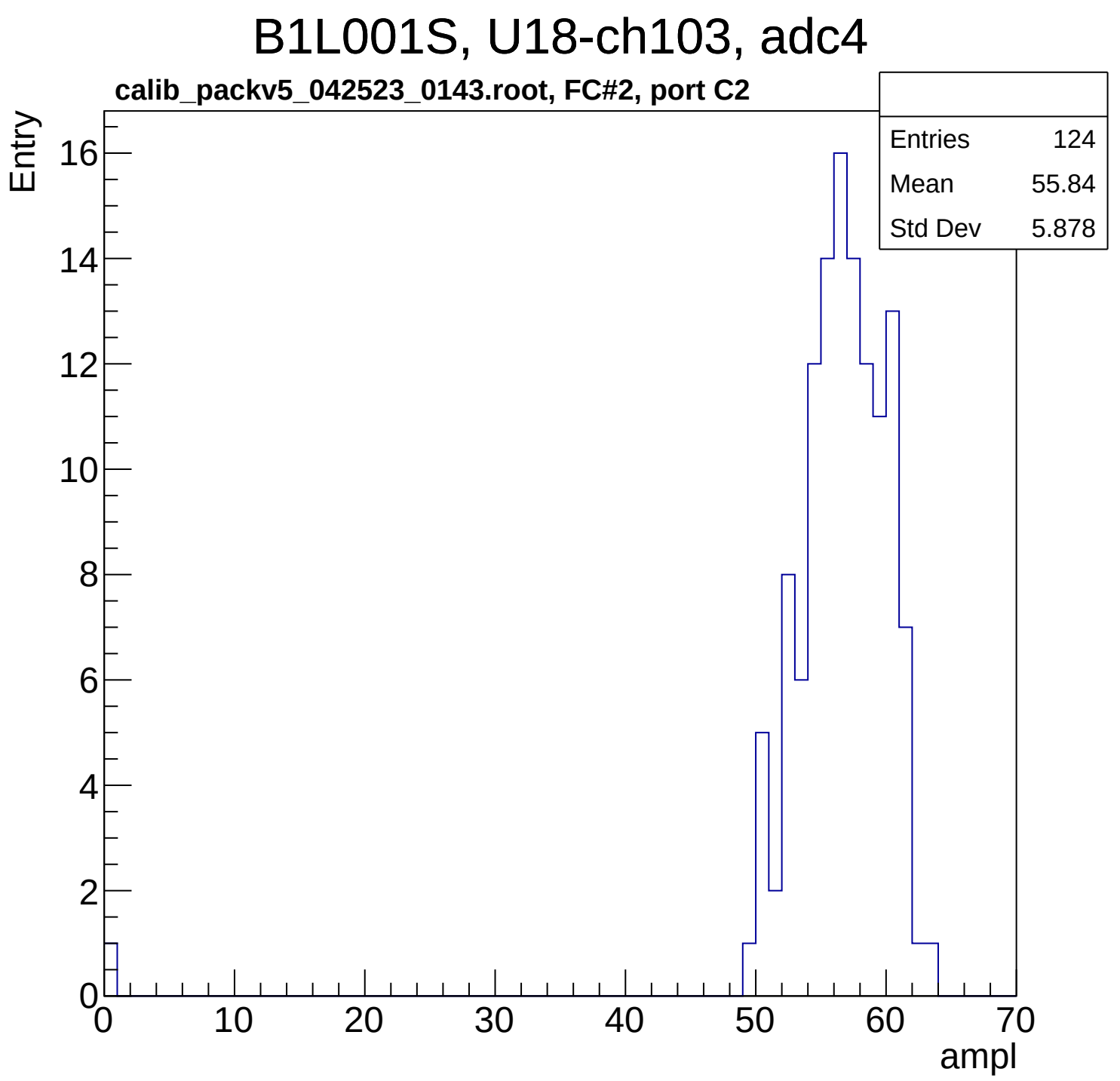

B1L001S, U18-ch102, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 0
Std Dev 0
Entry
2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

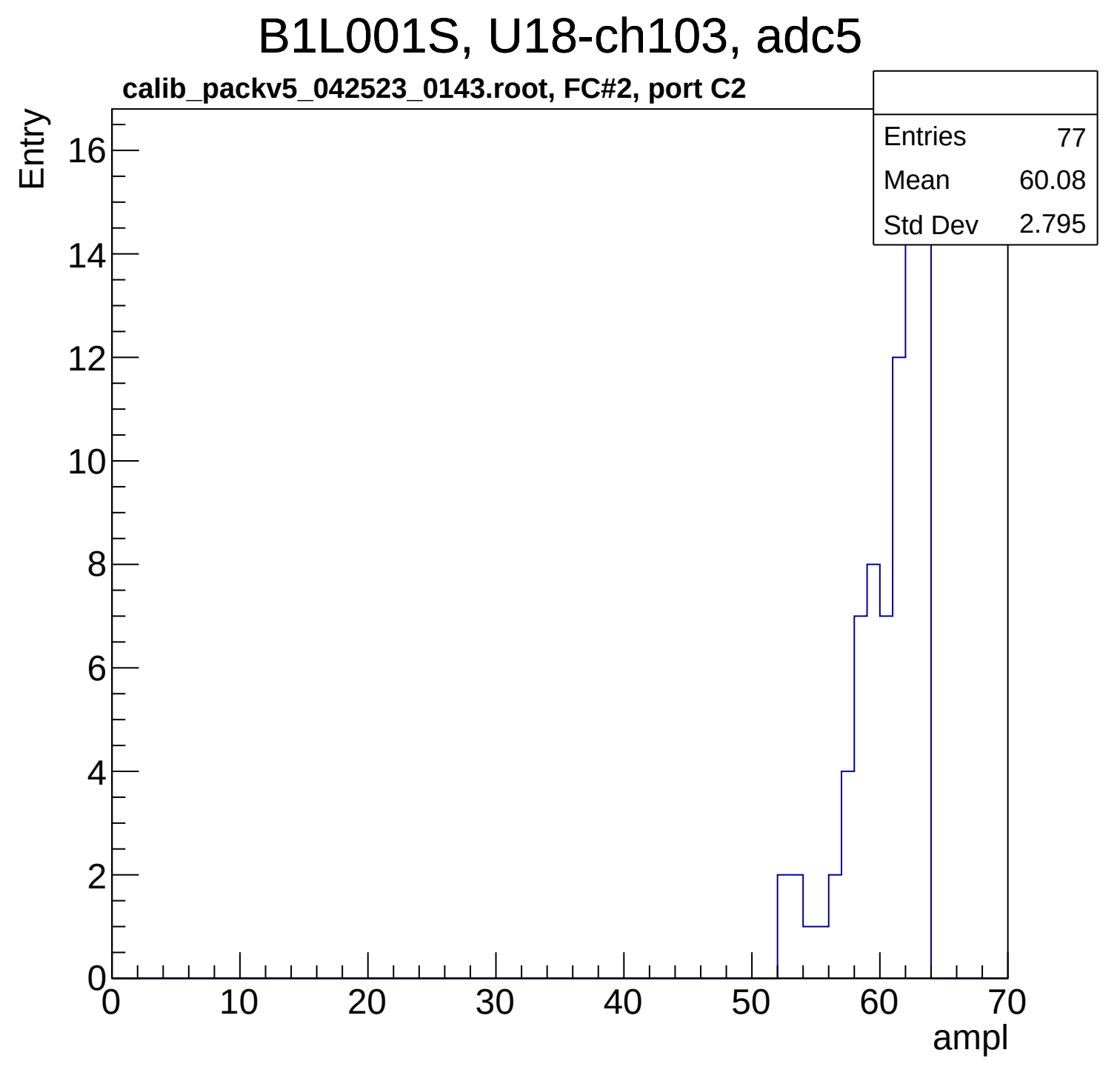

B1L001S, U18-ch103, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 136
Mean 29.65
Std Dev 4.532
Gaus mean : 30.3460
Gaus Width: 4.0038
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

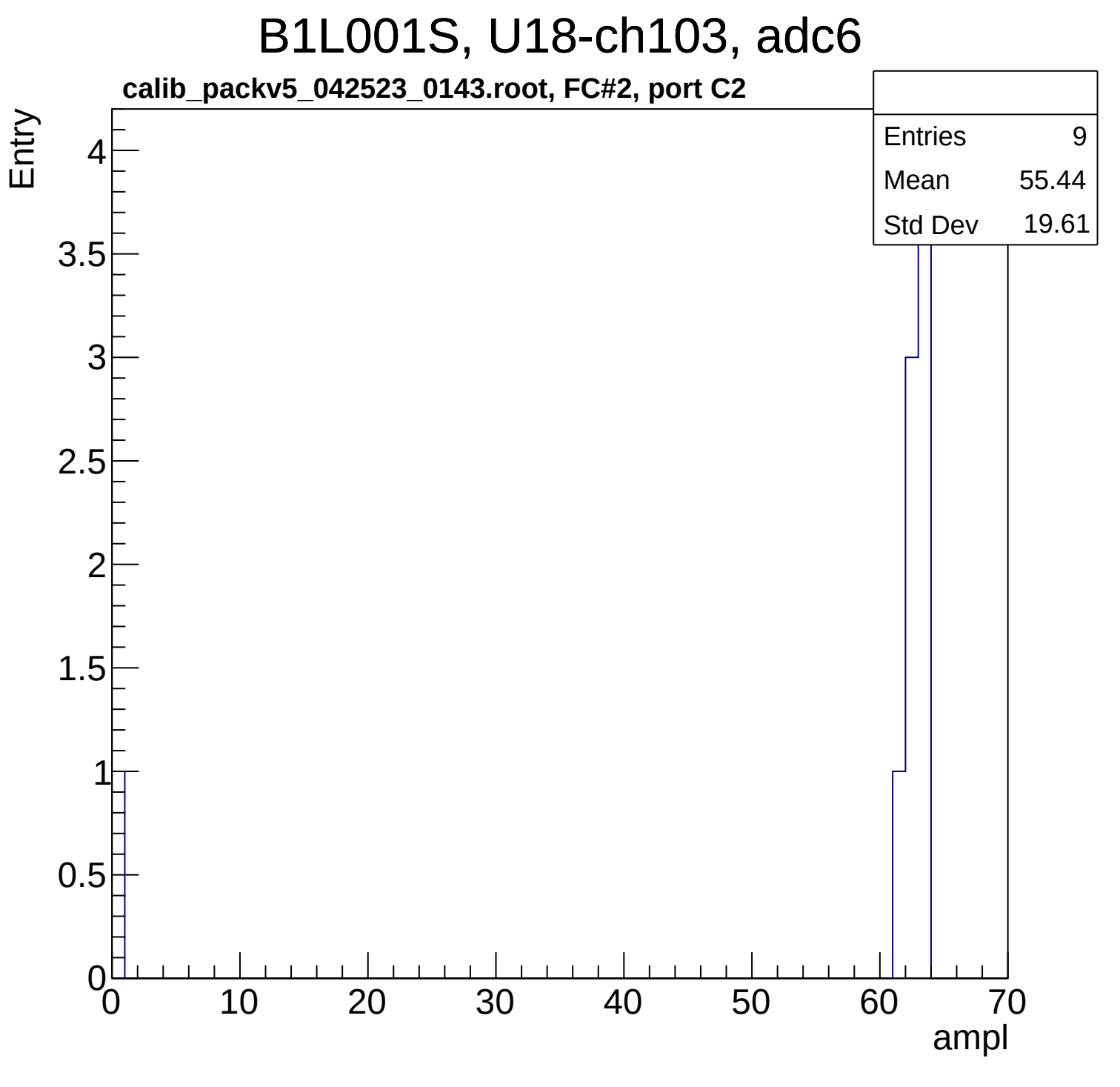

B1L001S, U18-ch103, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 134
Mean 36.47
Std Dev 3.613
Gaus mean : 36.8196
Gaus Width: 3.7812
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

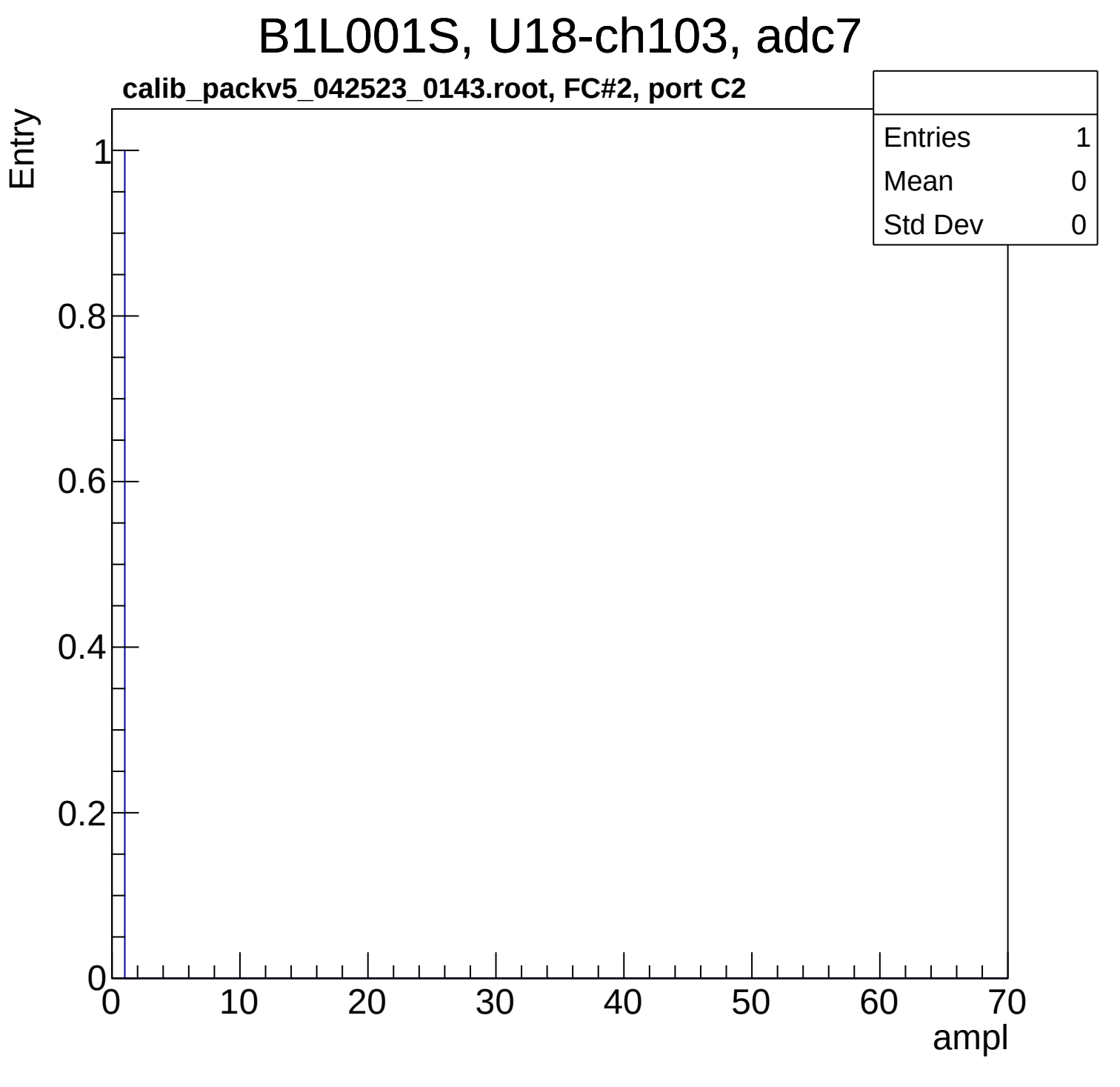

B1L001S, U18-ch103, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 121
Mean 42.98
Std Dev 3.517
Gaus mean : 43.6124
Gaus Width: 3.9463
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

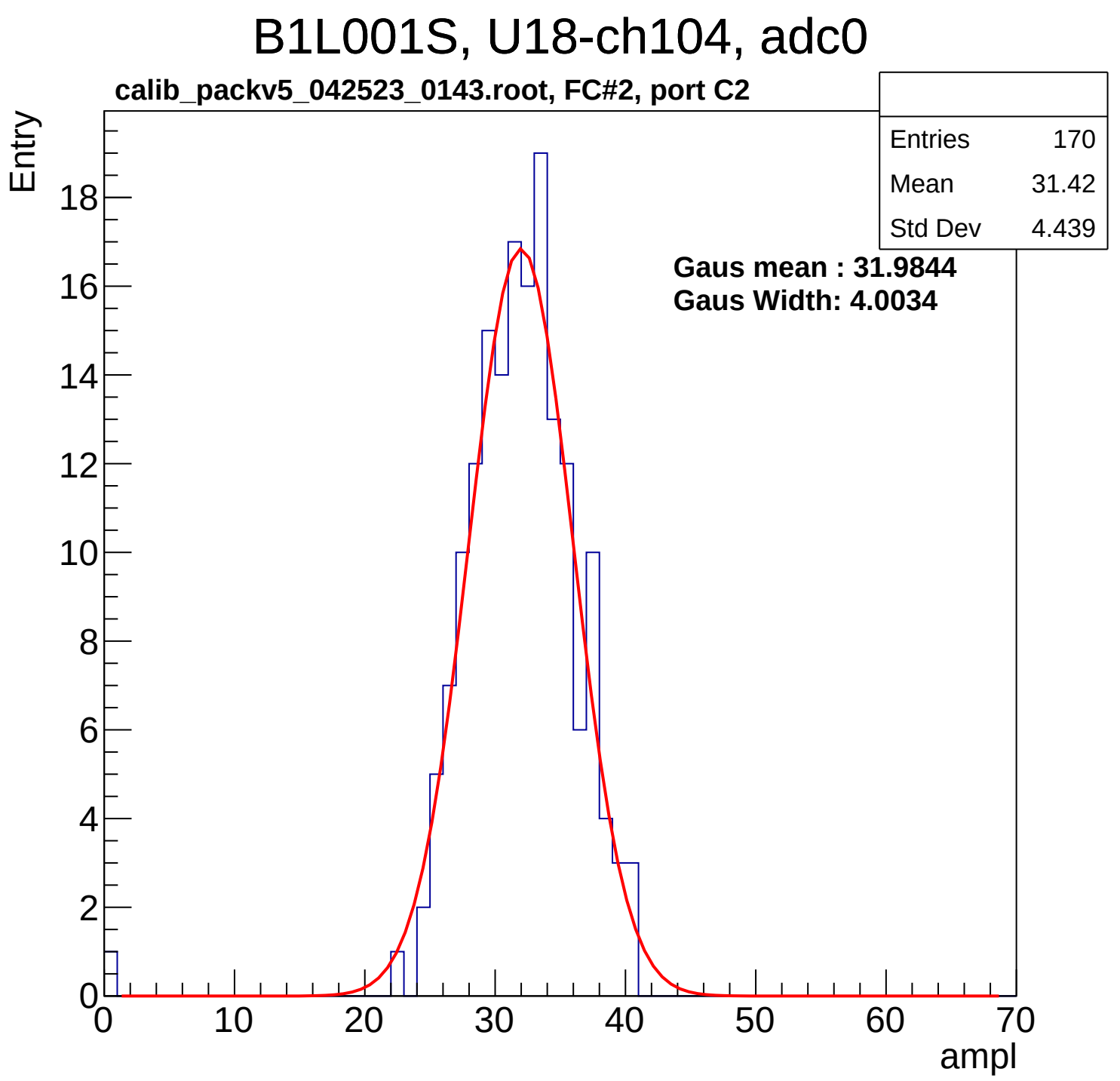

B1L001S, U18-ch103, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 143
Mean 49.39
Std Dev 3.628
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl

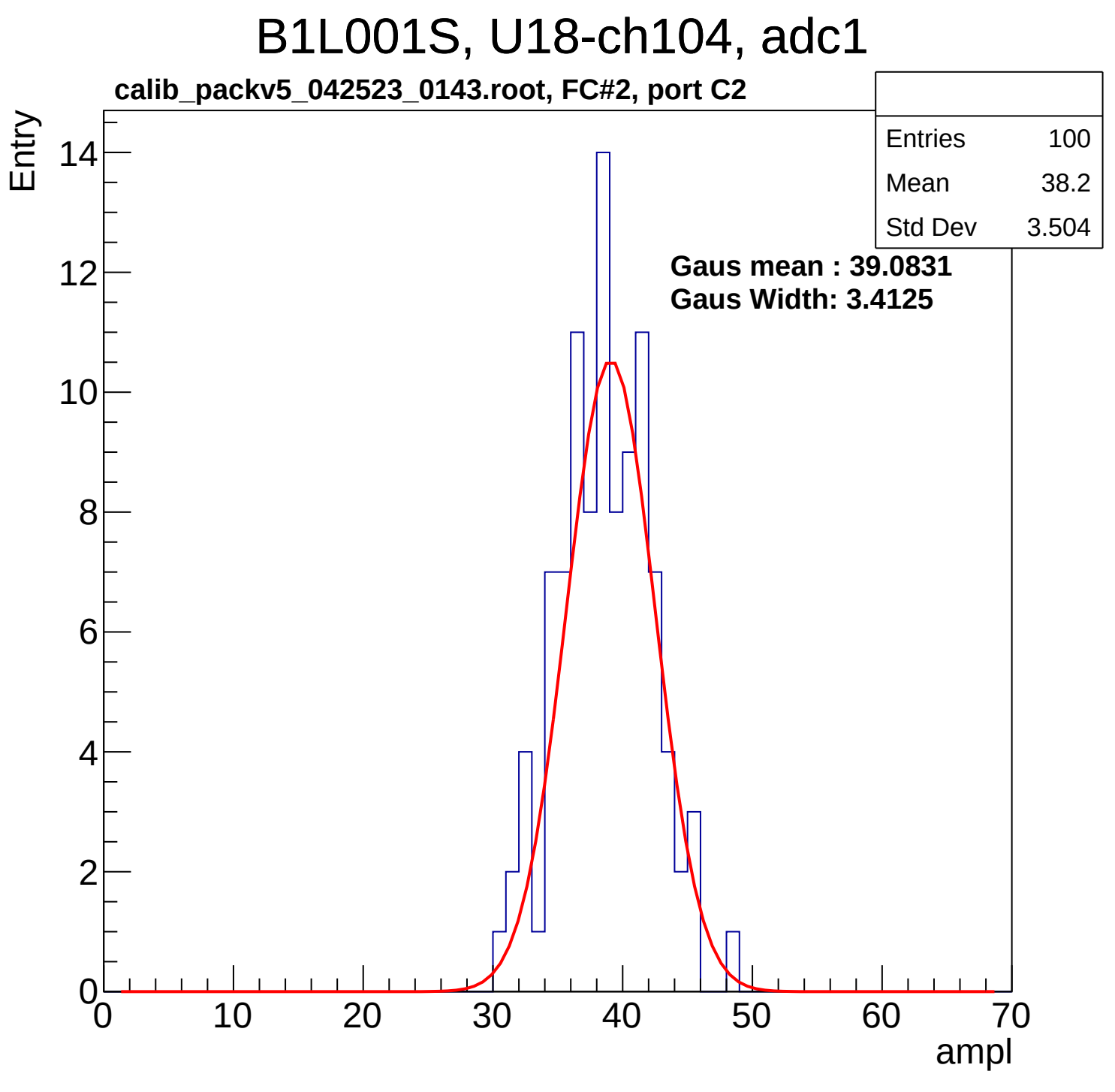

B1L001S, U18-ch103, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 124
Mean 55.84
Std Dev 5.878
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

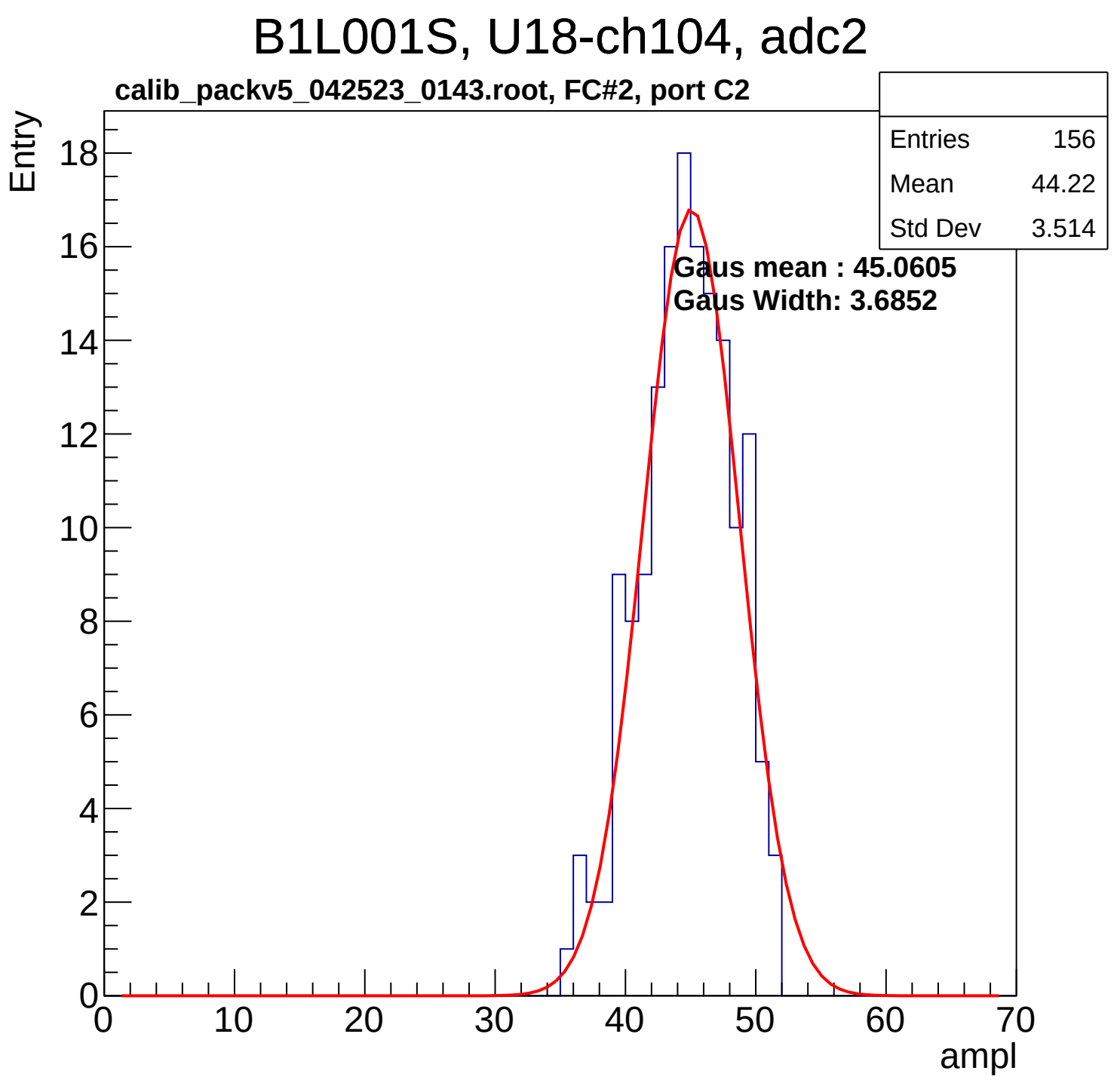

B1L001S, U18-ch103, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 77
Mean 60.08
Std Dev 2.795
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

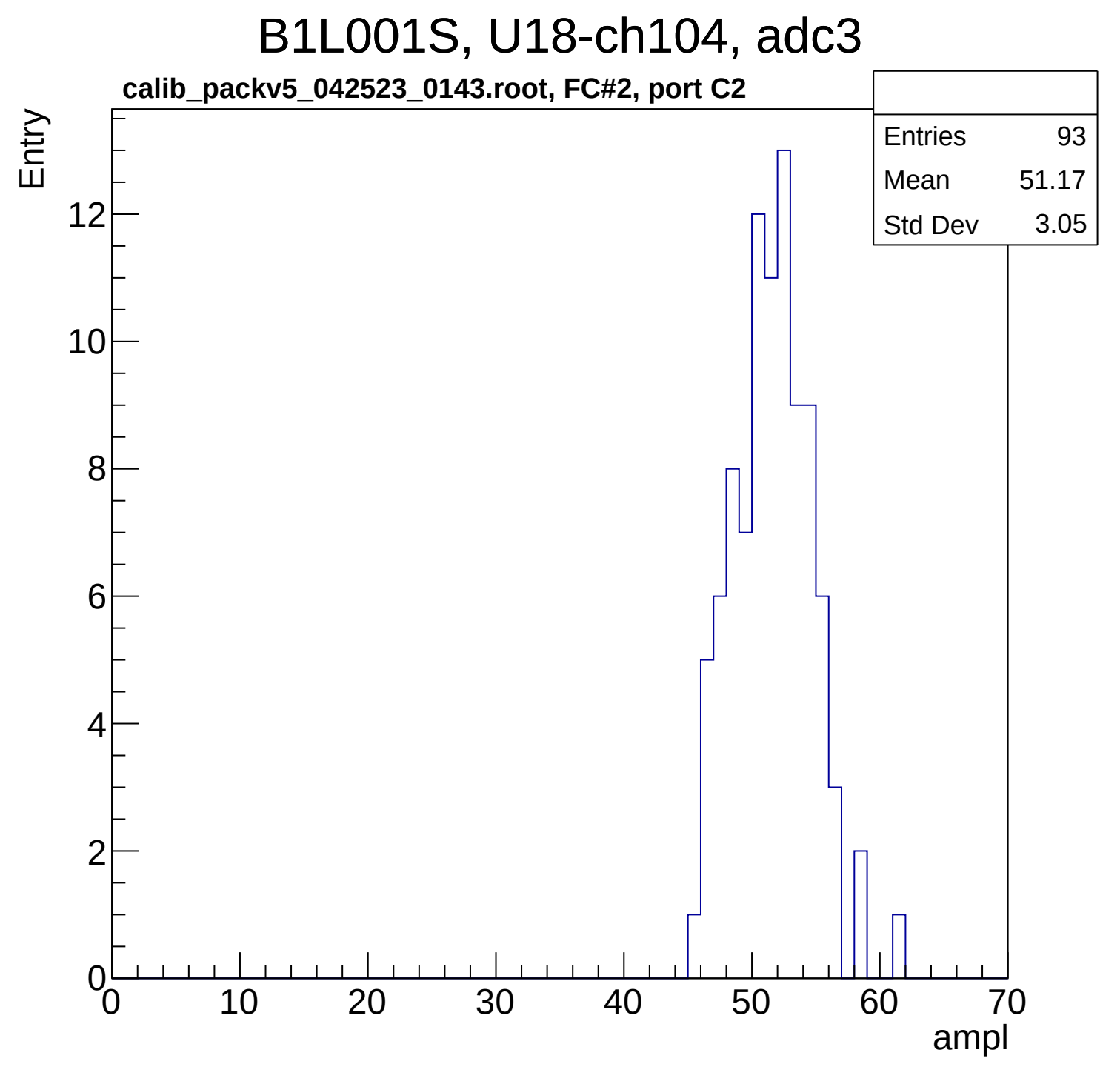

B1L001S, U18-ch103, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 9
Mean 55.44
Std Dev 19.61
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

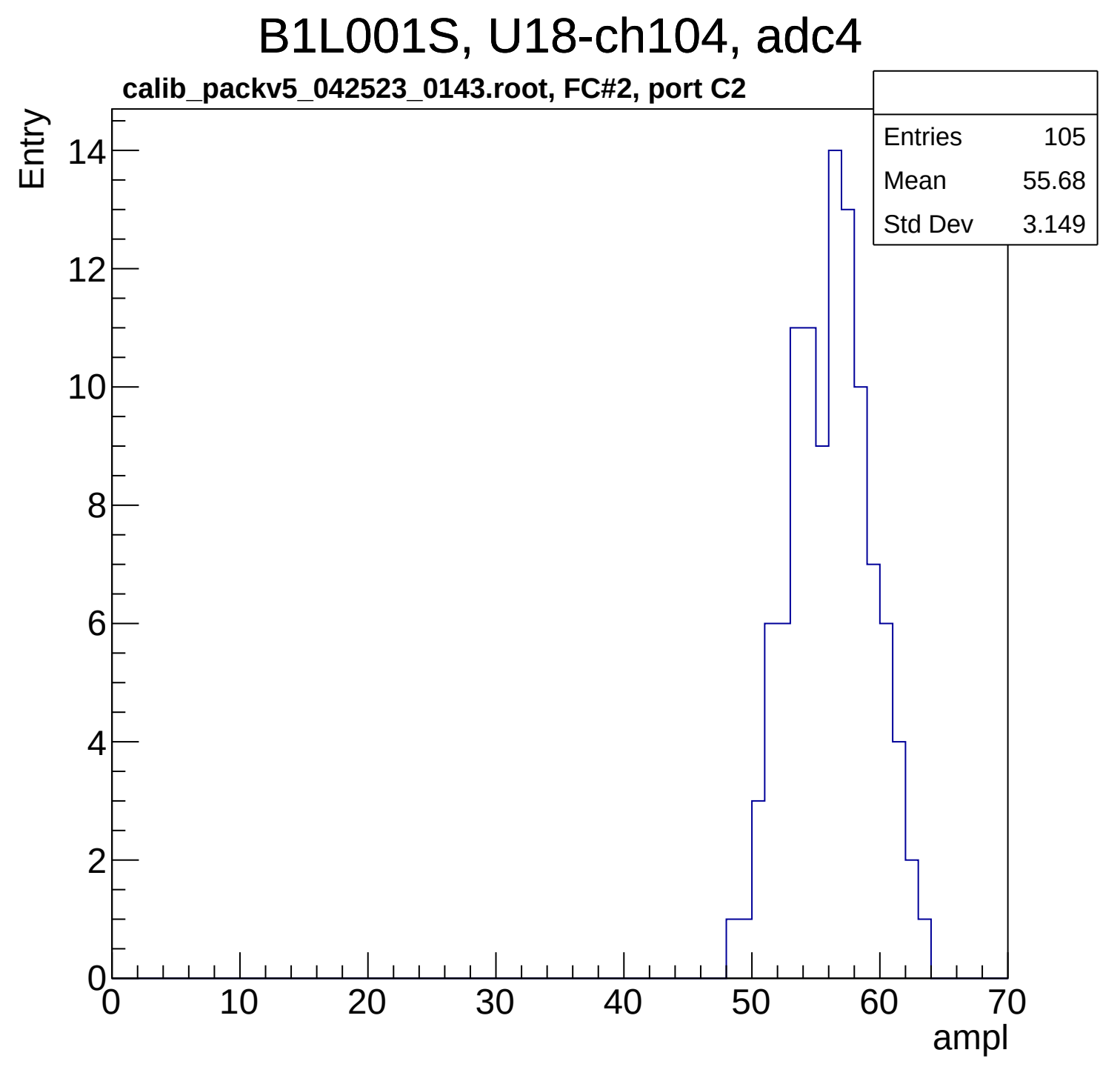

B1L001S, U18-ch103, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

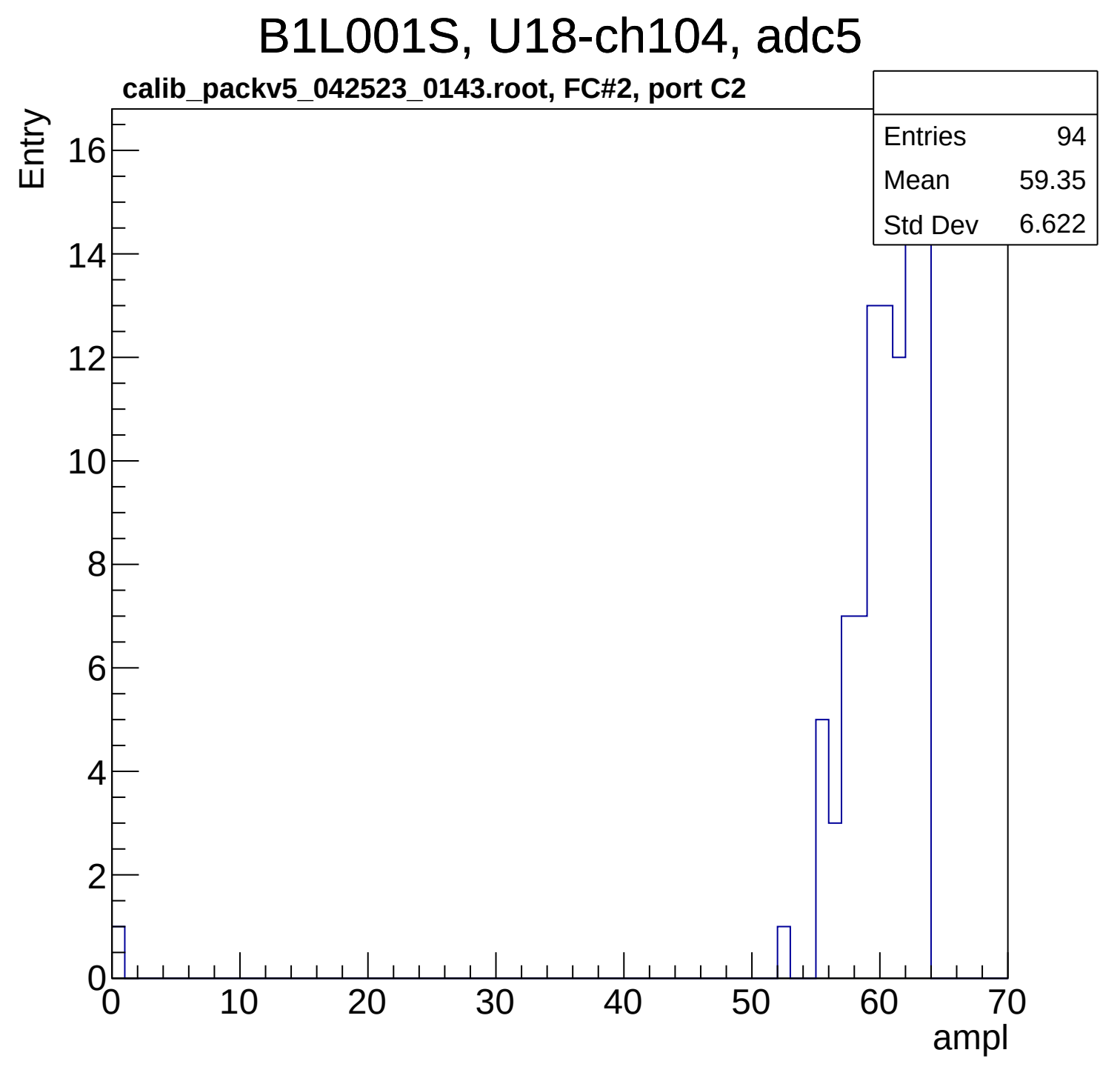

B1L001S, U18-ch104, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 170
Mean 31.42
Std Dev 4.439
Gaus mean : 31.9844
Gaus Width: 4.0034
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

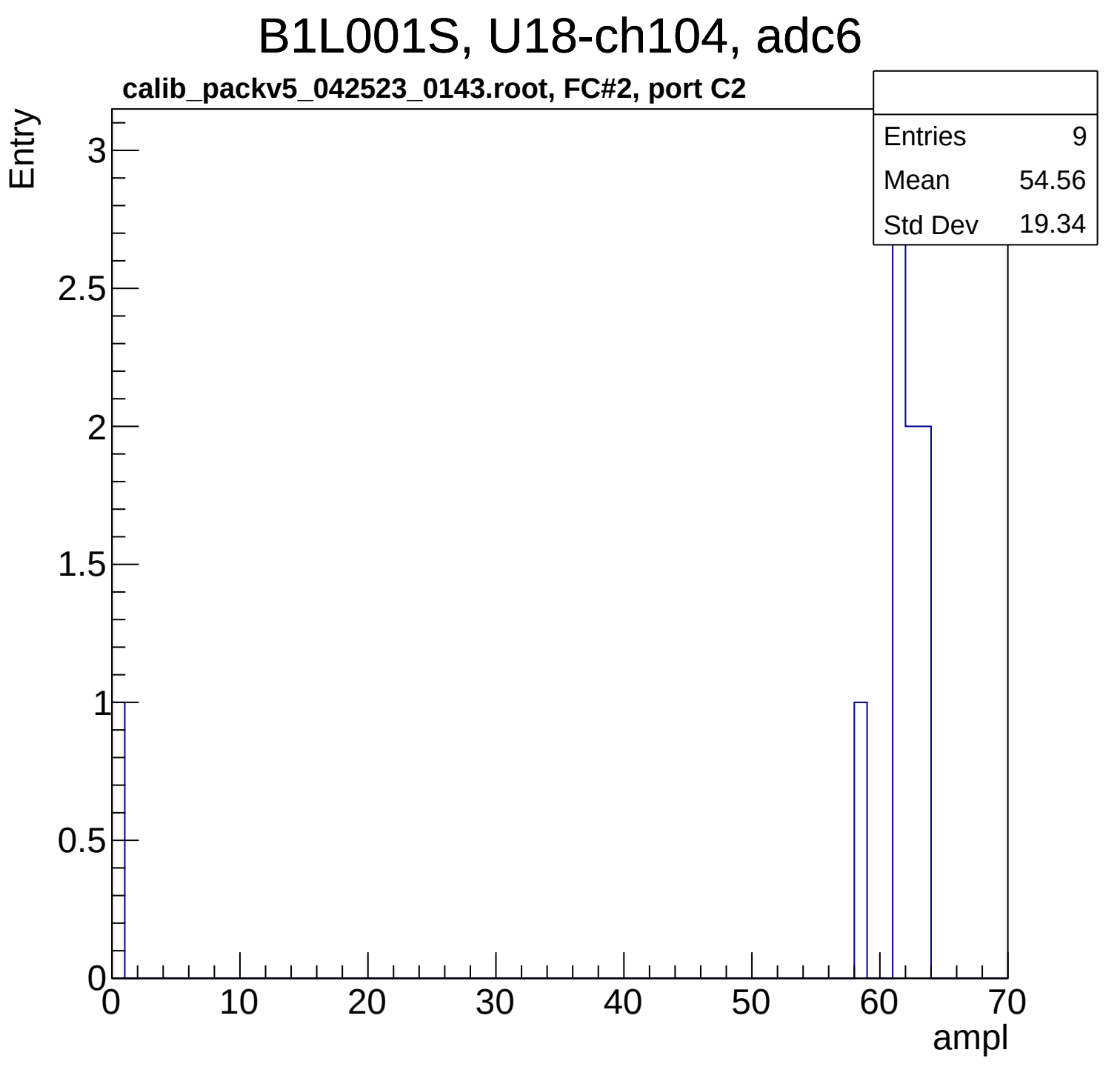

B1L001S, U18-ch104, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 100
Mean 38.2
Std Dev 3.504
Gaus mean : 39.0831
Gaus Width: 3.4125
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

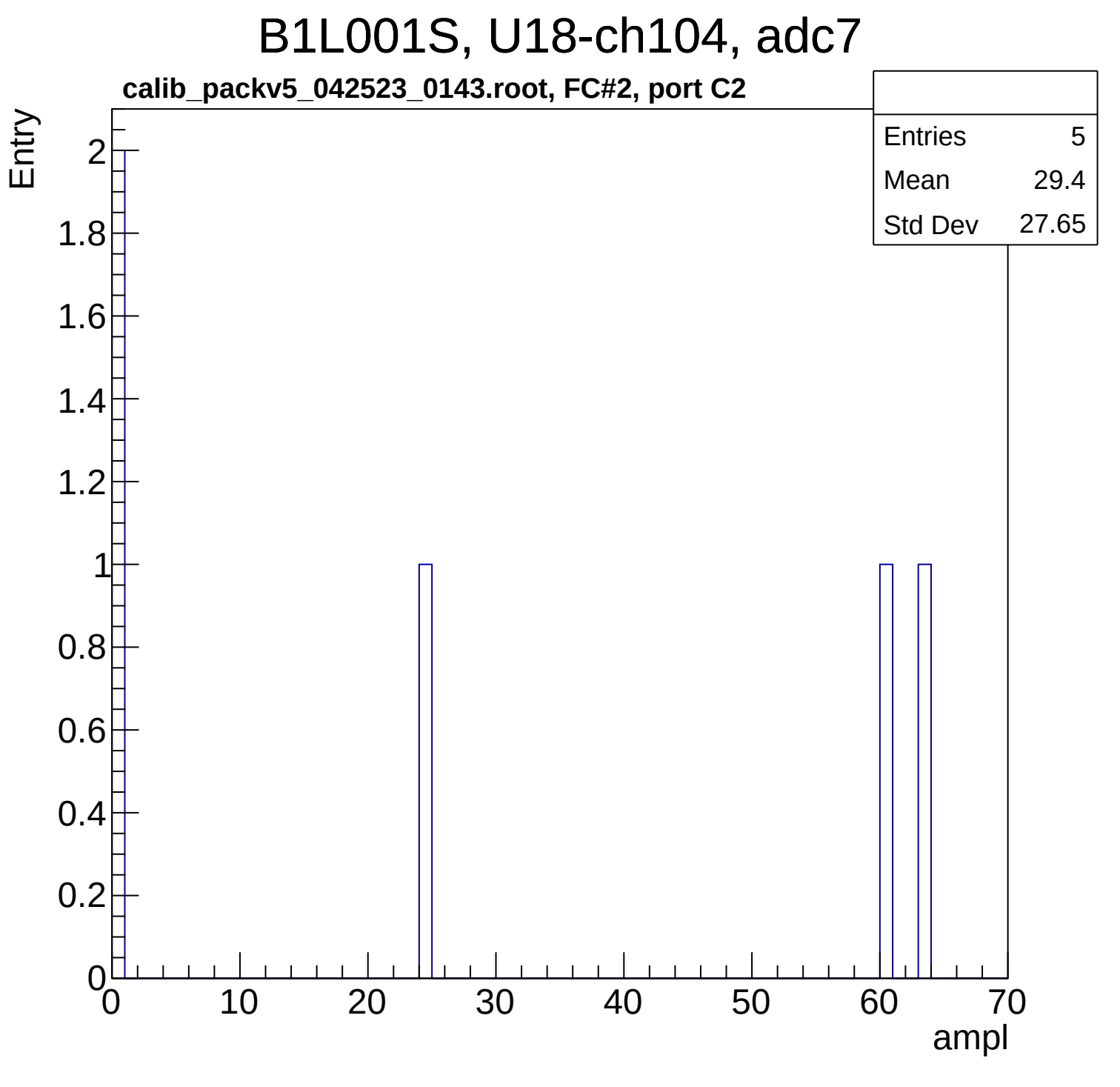

B1L001S, U18-ch104, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 156
Mean 44.22
Std Dev 3.514
Gaus mean : 45.0605
Gaus Width: 3.6852
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

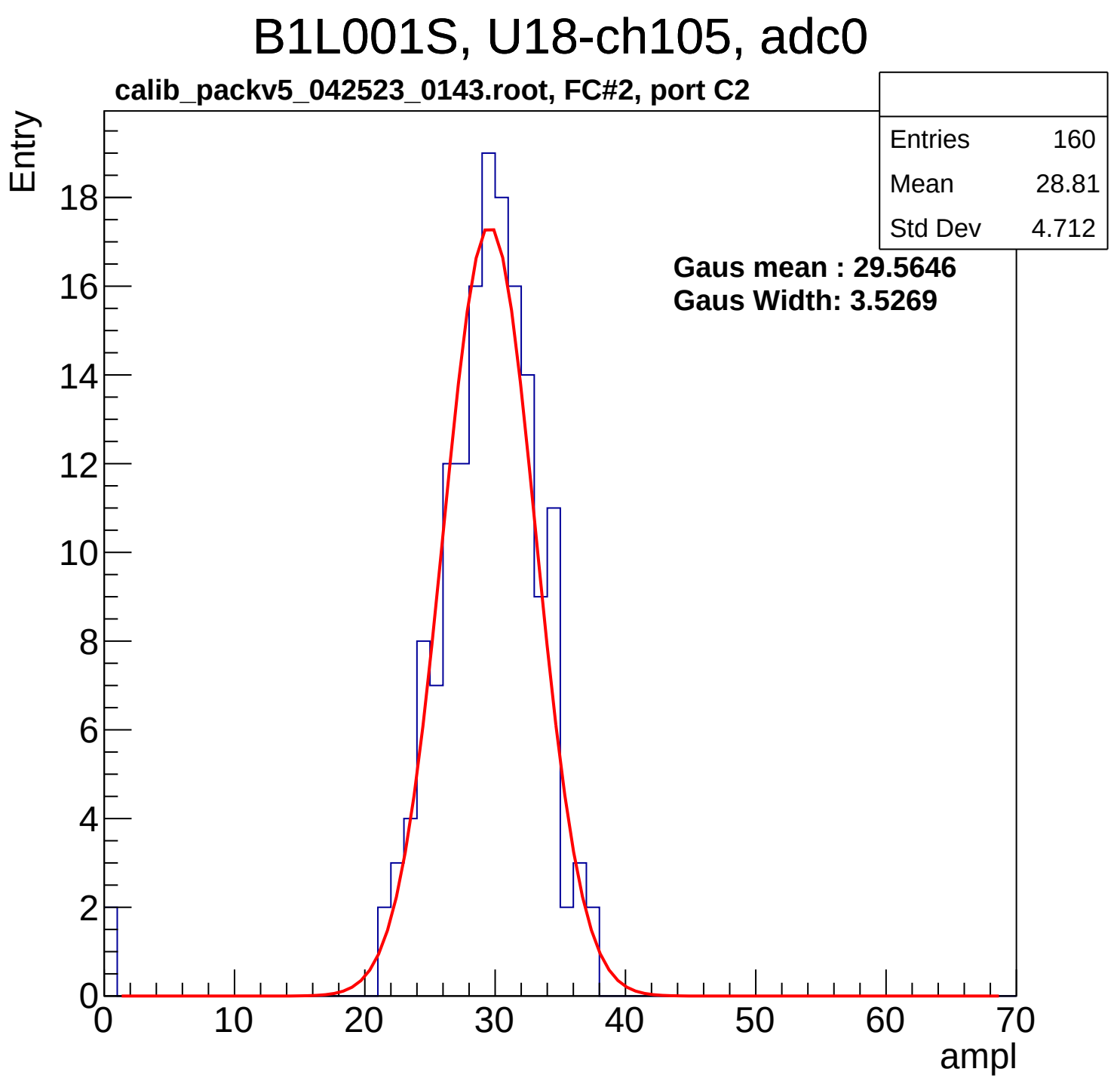

B1L001S, U18-ch104, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 93
Mean 51.17
Std Dev 3.05
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl

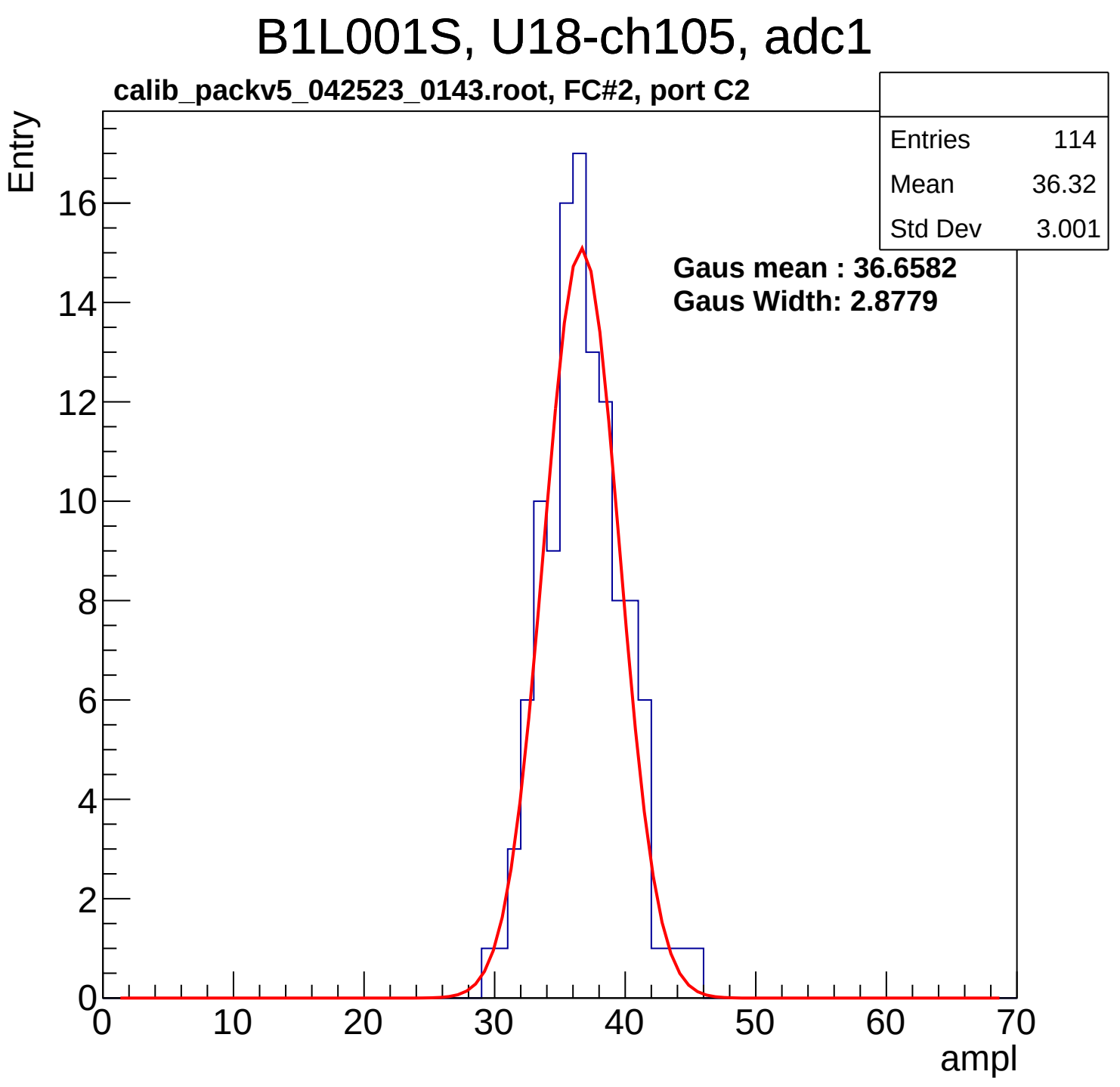

B1L001S, U18-ch104, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 105
Mean 55.68
Std Dev 3.149
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

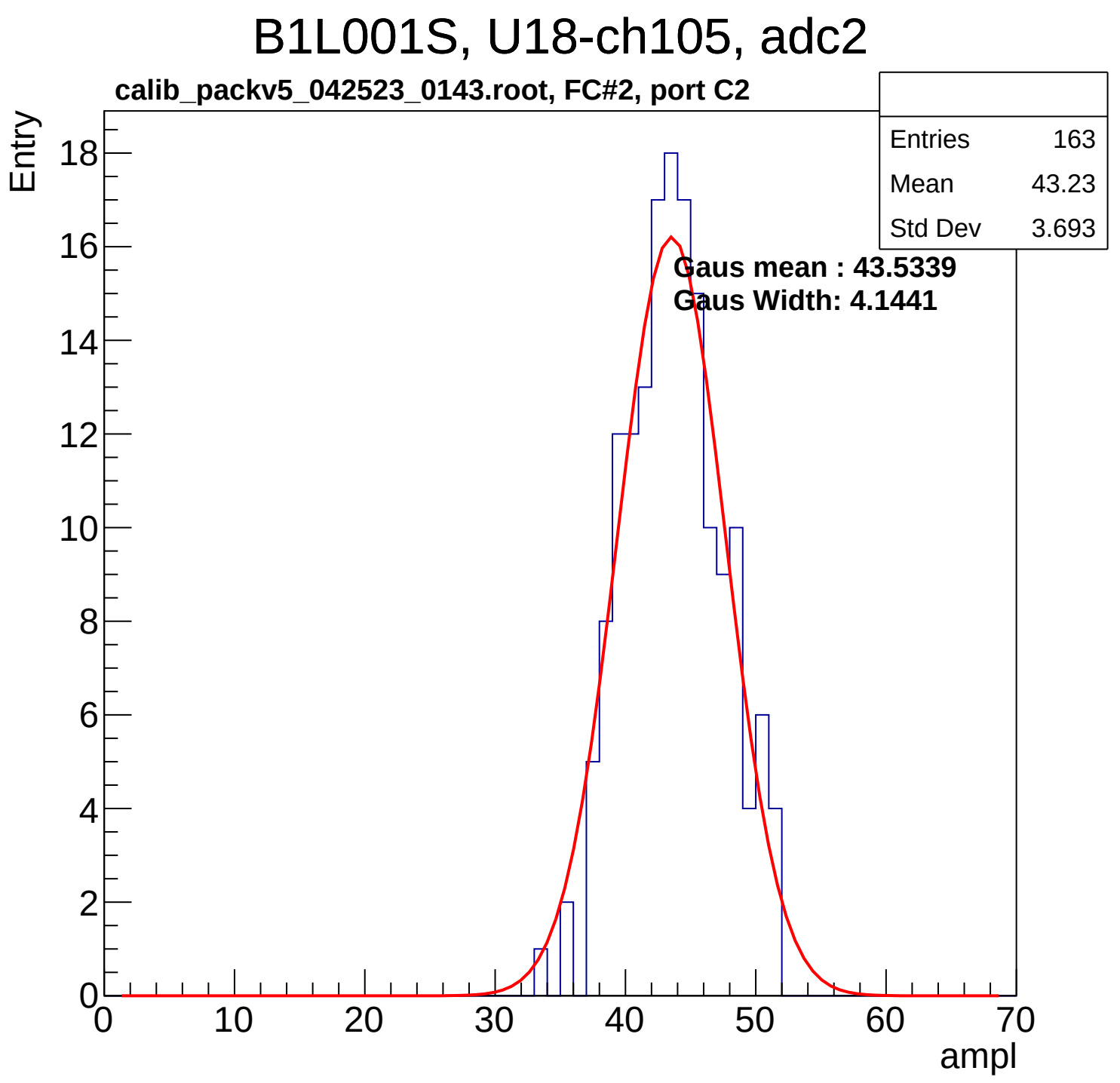

B1L001S, U18-ch104, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 94
Mean 59.35
Std Dev 6.622
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

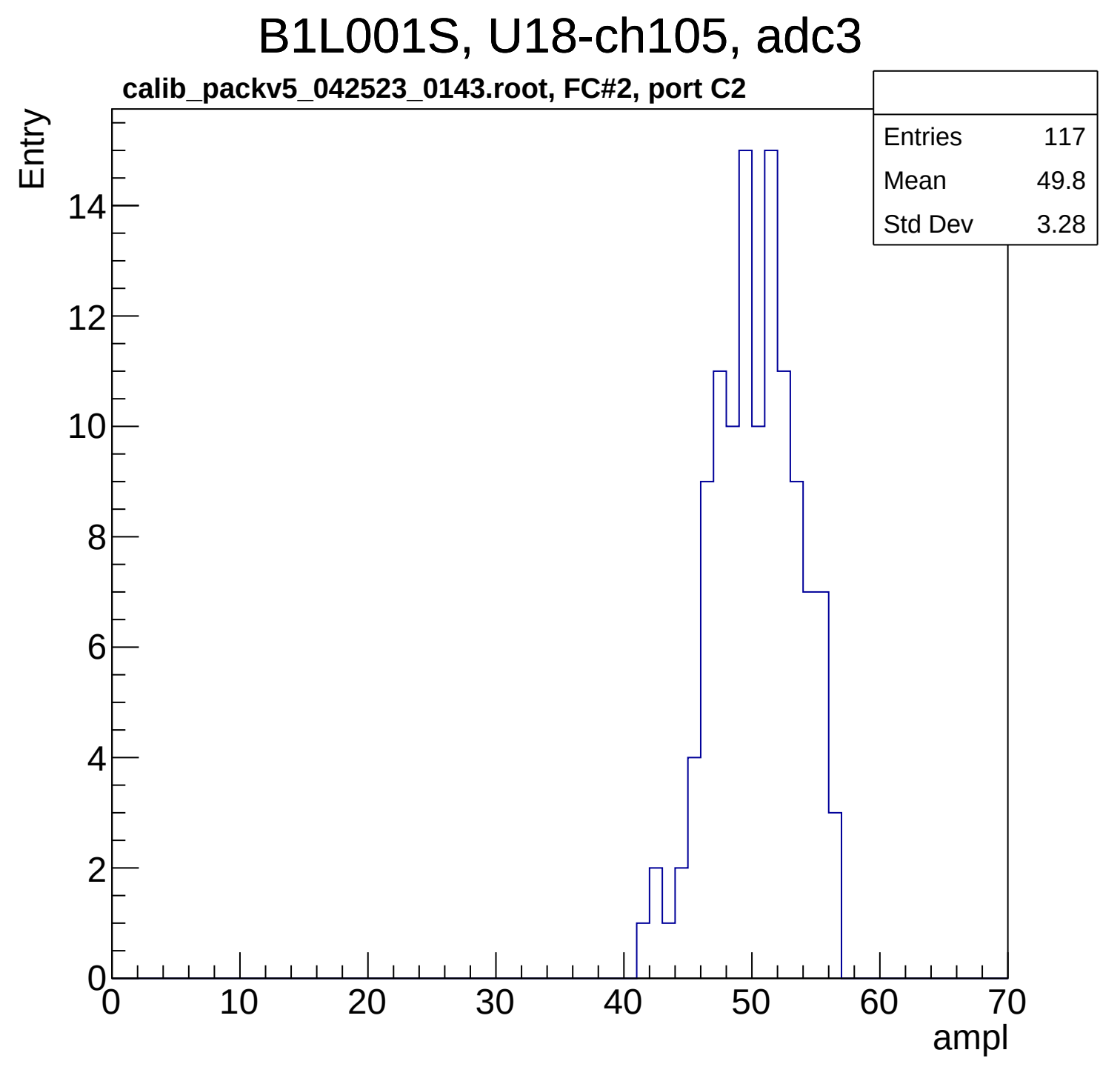

B1L001S, U18-ch104, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 9
Mean 54.56
Std Dev 19.34
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

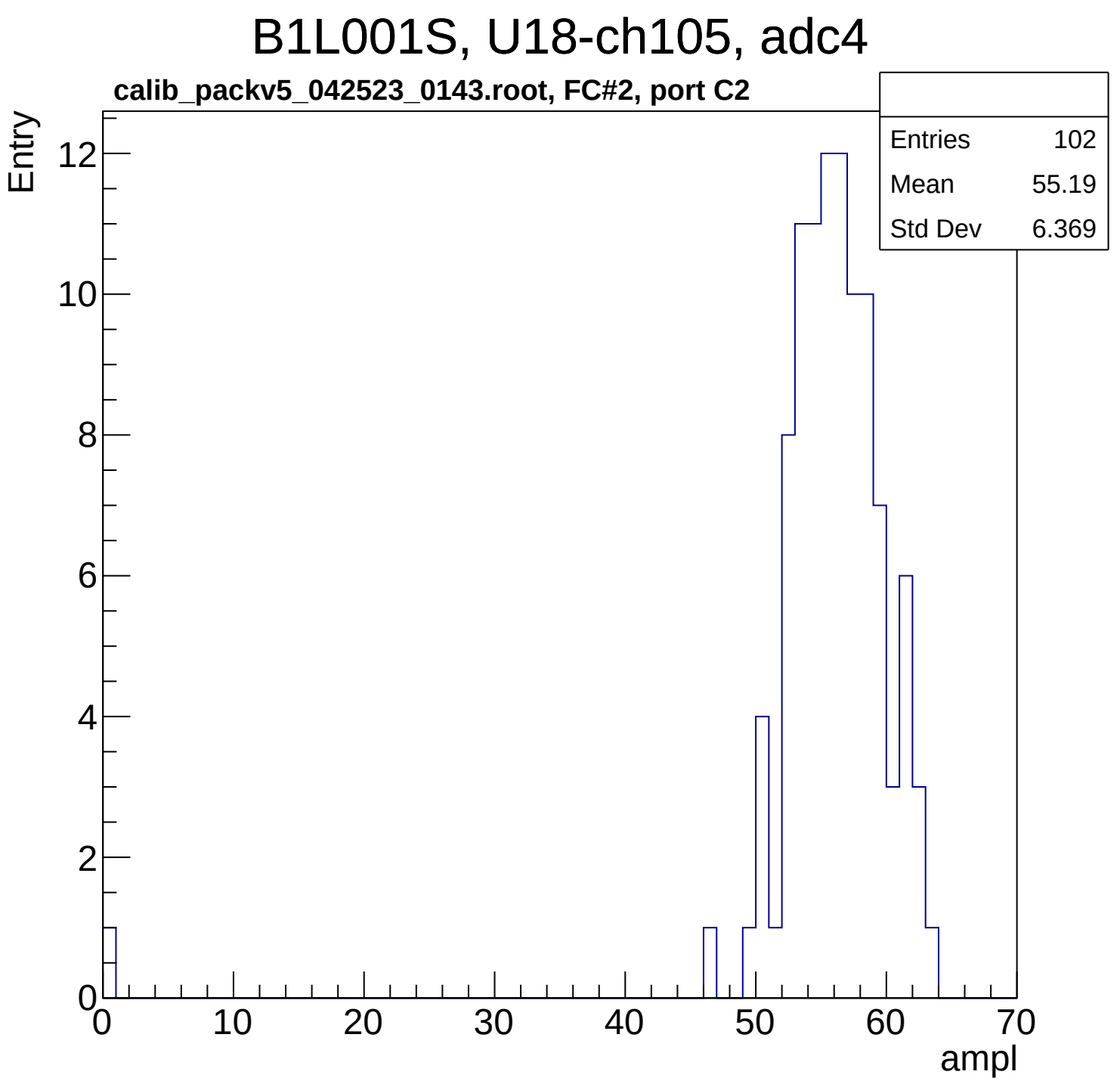

B1L001S, U18-ch104, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 5
Mean 29.4
Std Dev 27.65
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

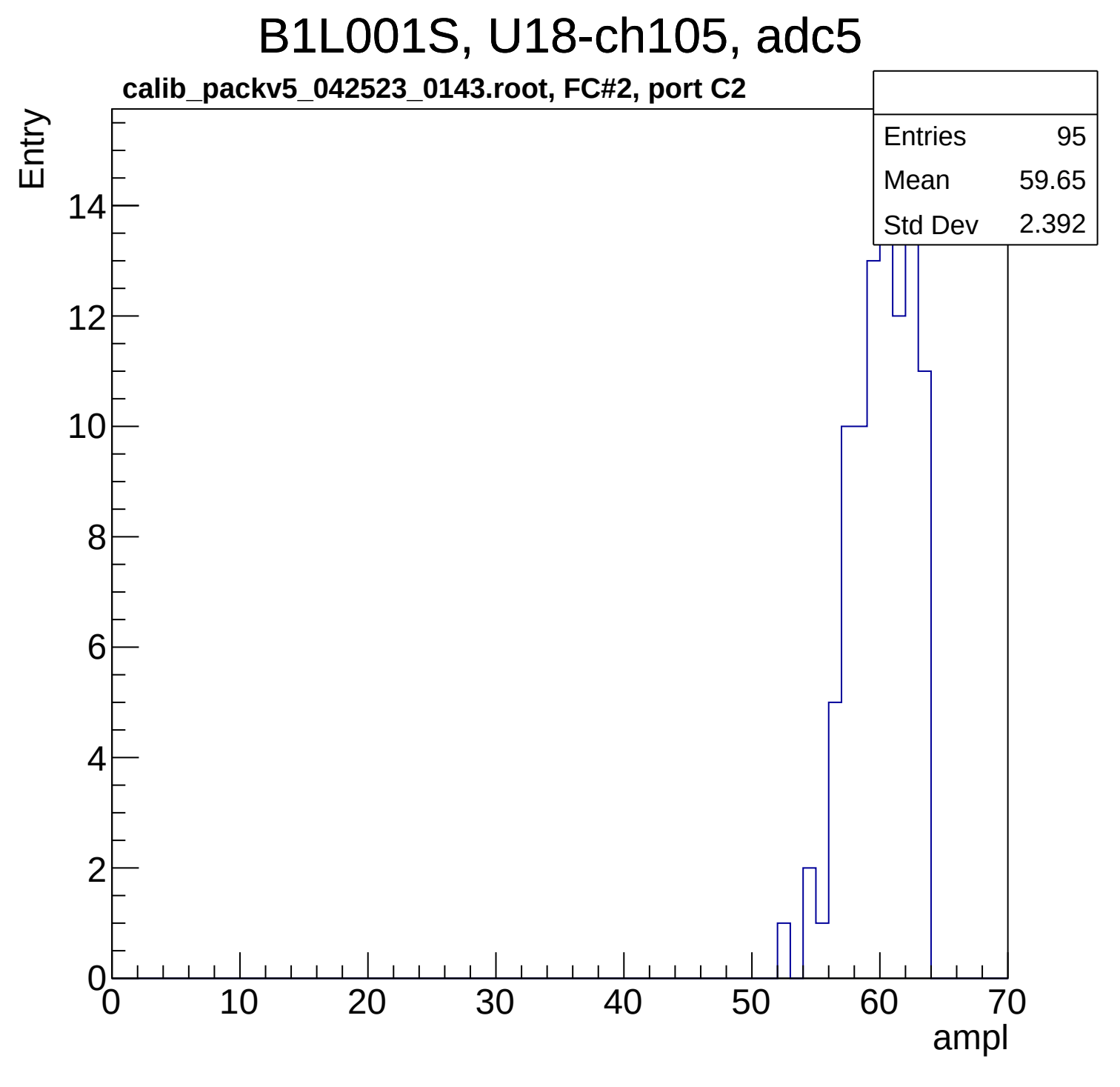

B1L001S, U18-ch105, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 160
Mean 28.81
Std Dev 4.712
Gaus mean : 29.5646
Gaus Width: 3.5269
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

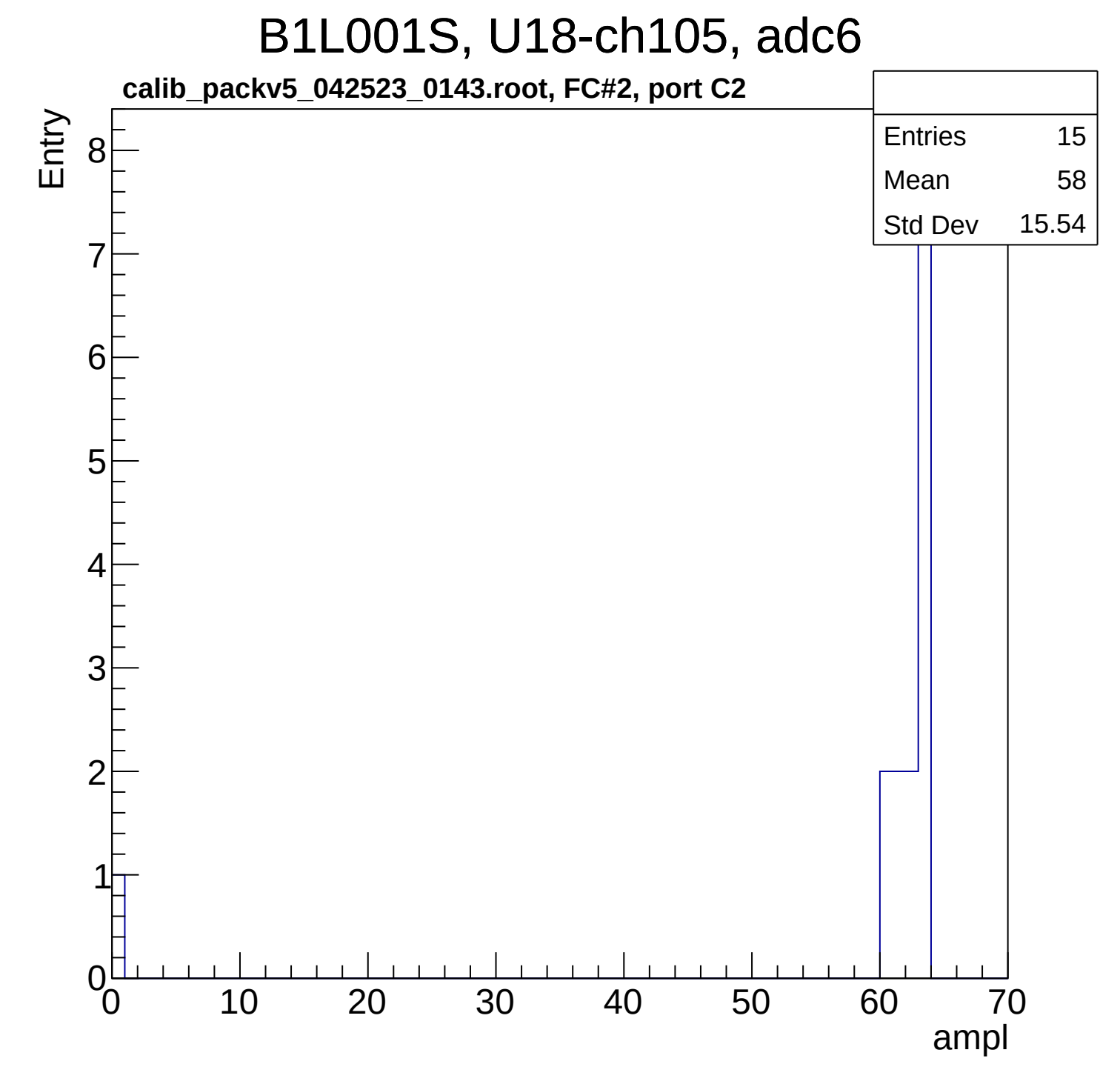

B1L001S, U18-ch105, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 114
Mean 36.32
Std Dev 3.001
Gaus mean : 36.6582
Gaus Width: 2.8779
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

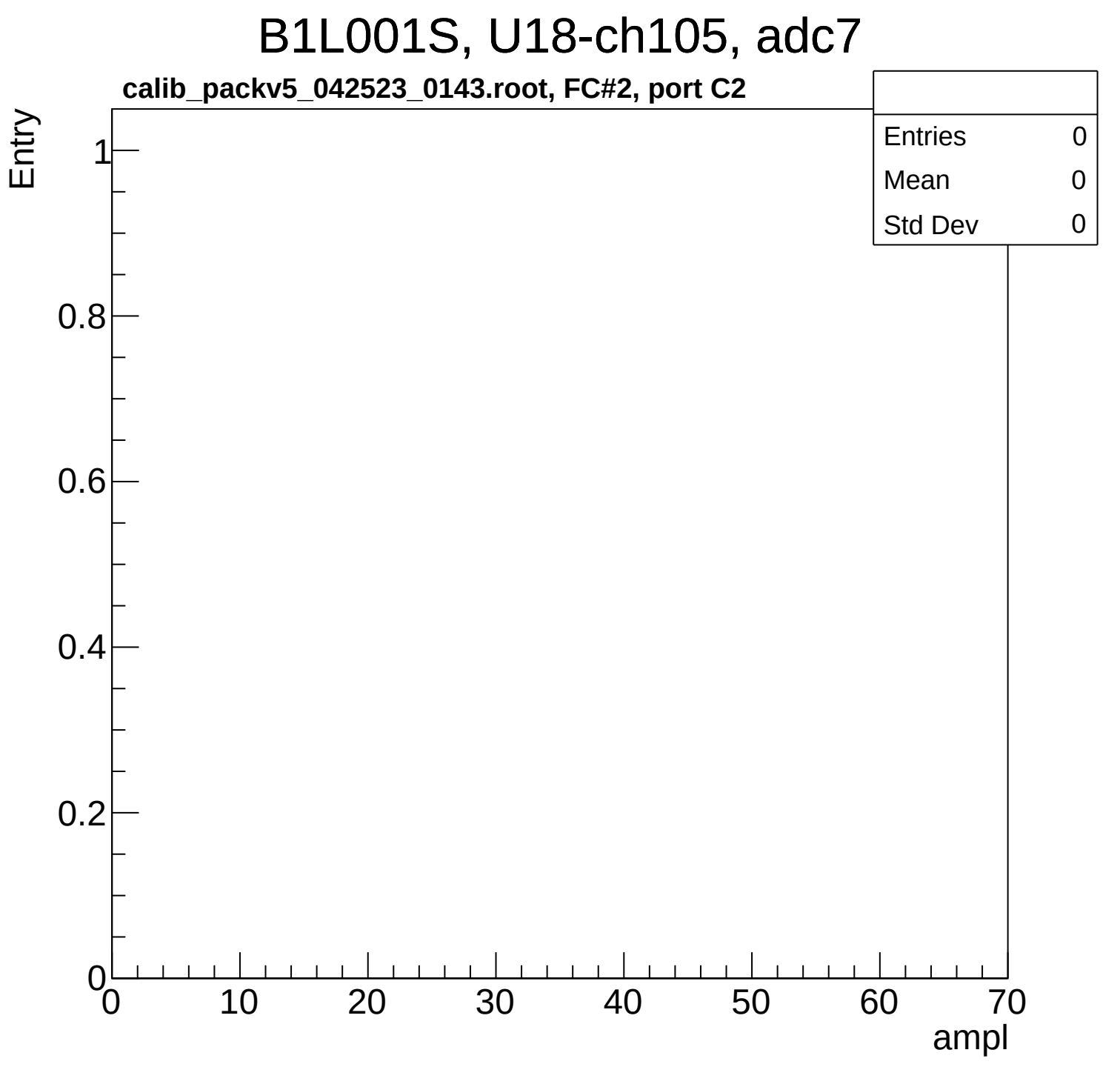

B1L001S, U18-ch105, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 163
Mean 43.23
Std Dev 3.693
Gaus mean : 43.5339
Gaus Width: 4.1441
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

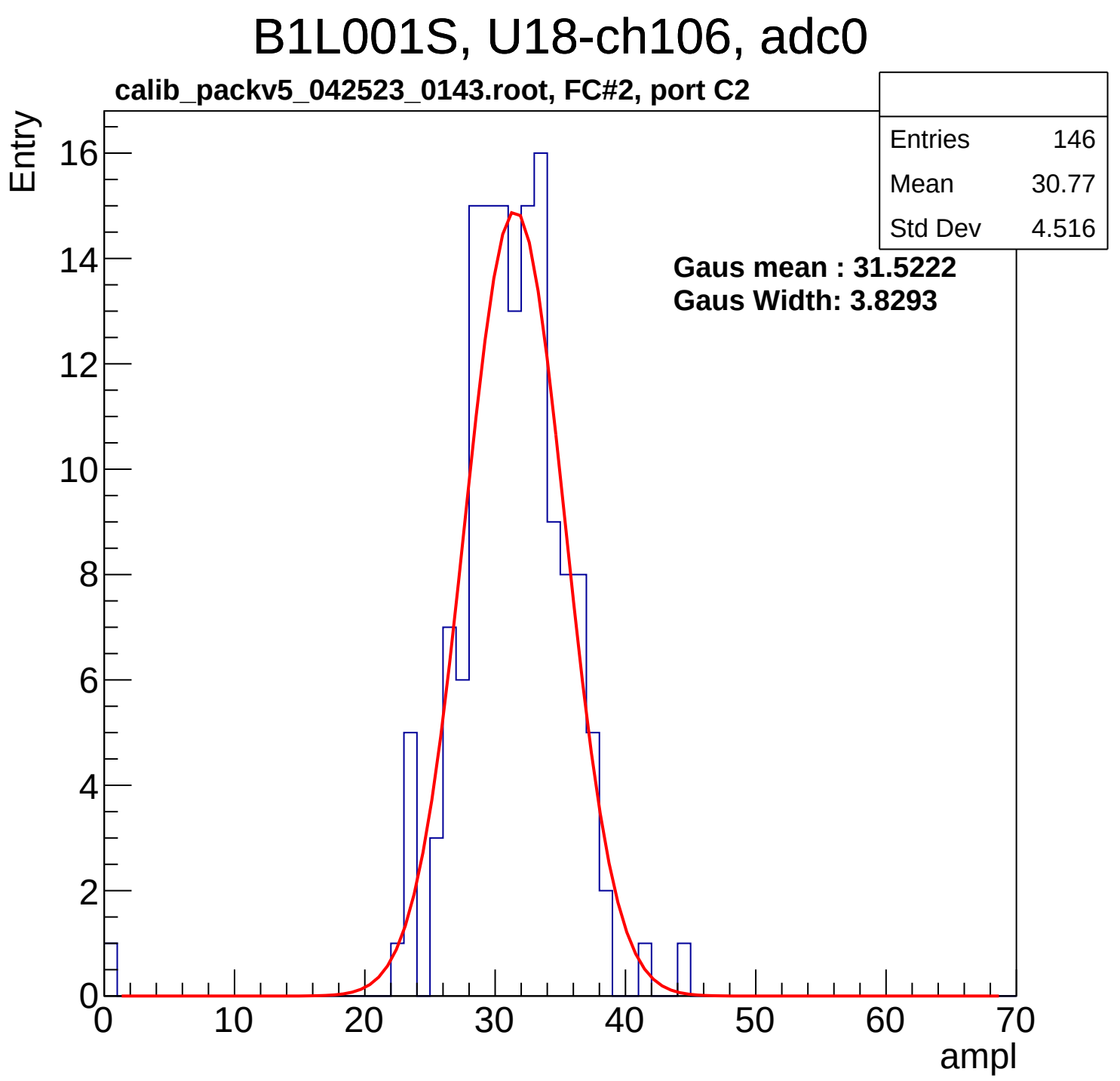

B1L001S, U18-ch105, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 117
Mean 49.8
Std Dev 3.28
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl

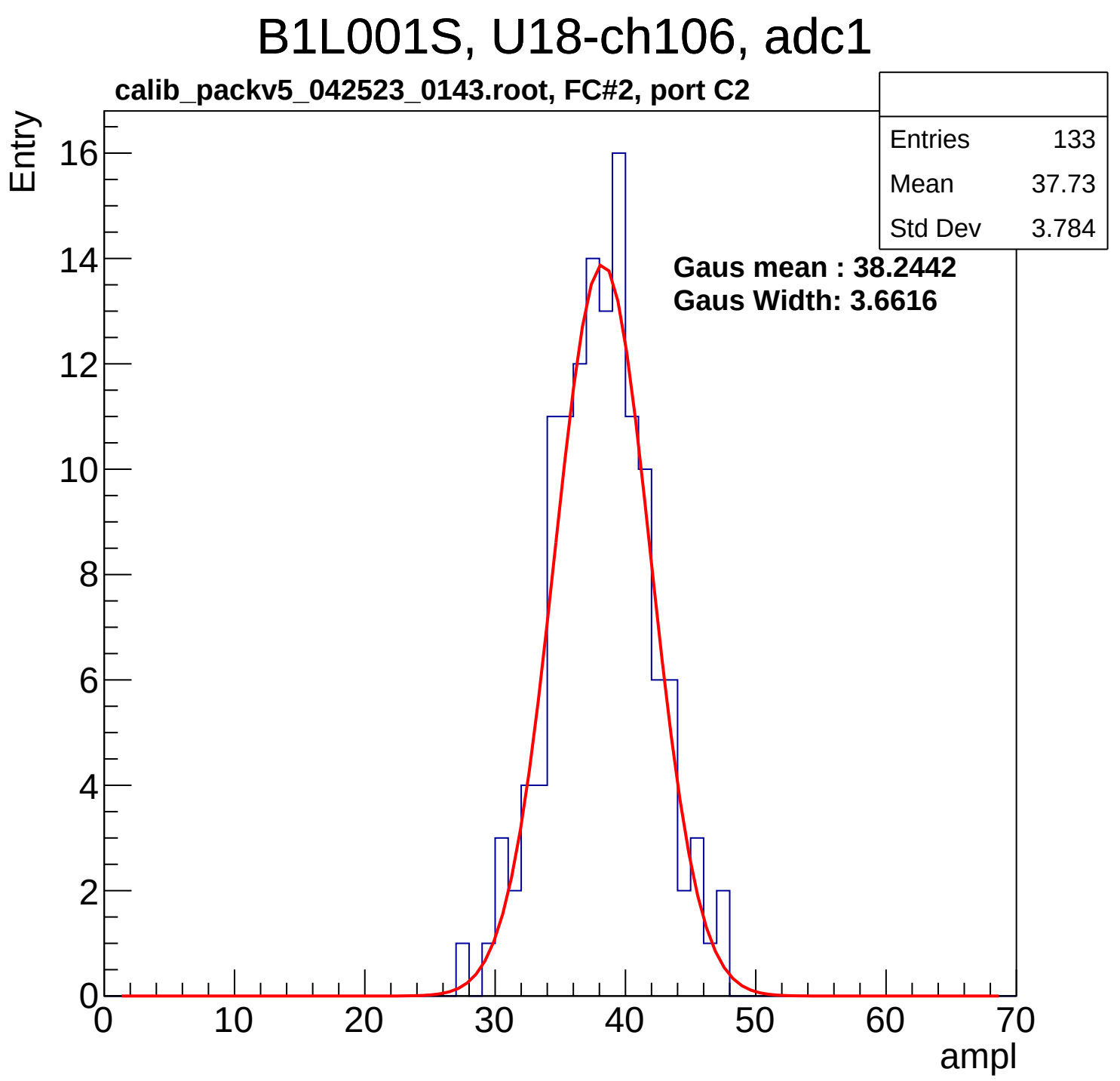

B1L001S, U18-ch105, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 102
Mean 55.19
Std Dev 6.369
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70

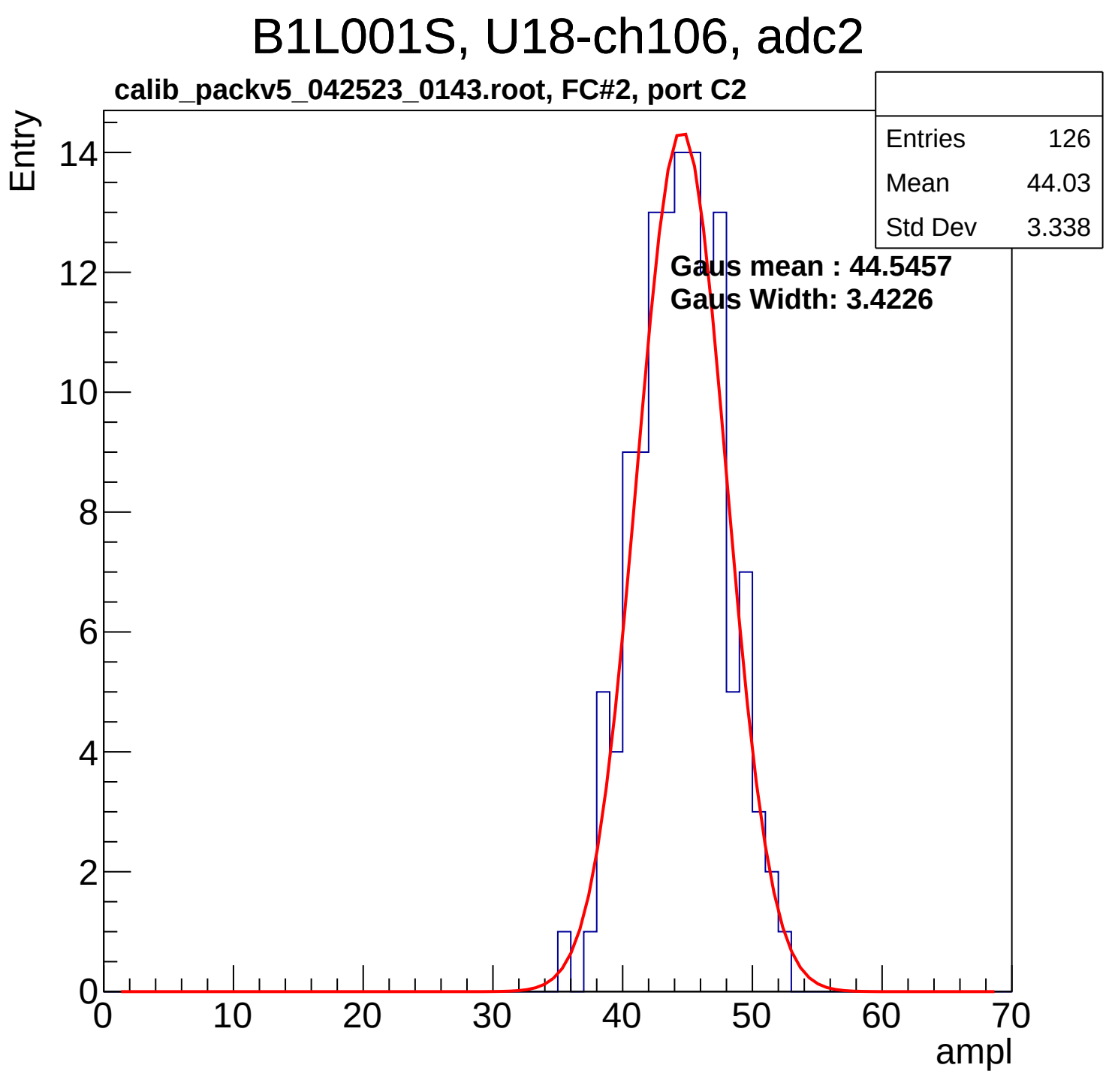

B1L001S, U18-ch105, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 95
Mean 59.65
Std Dev 2.392
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

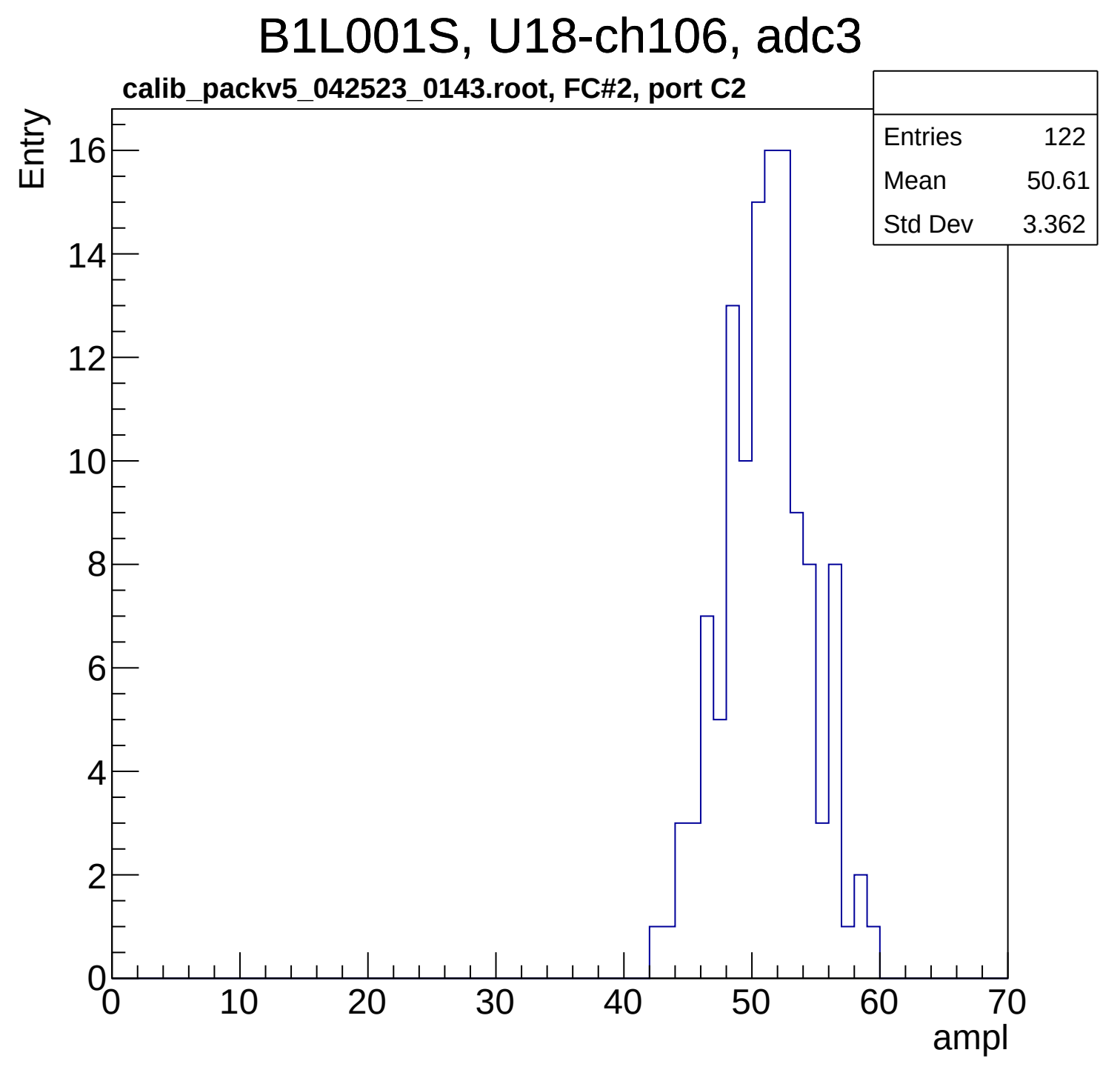

B1L001S, U18-ch105, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 15
Mean 58
Std Dev 15.54
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

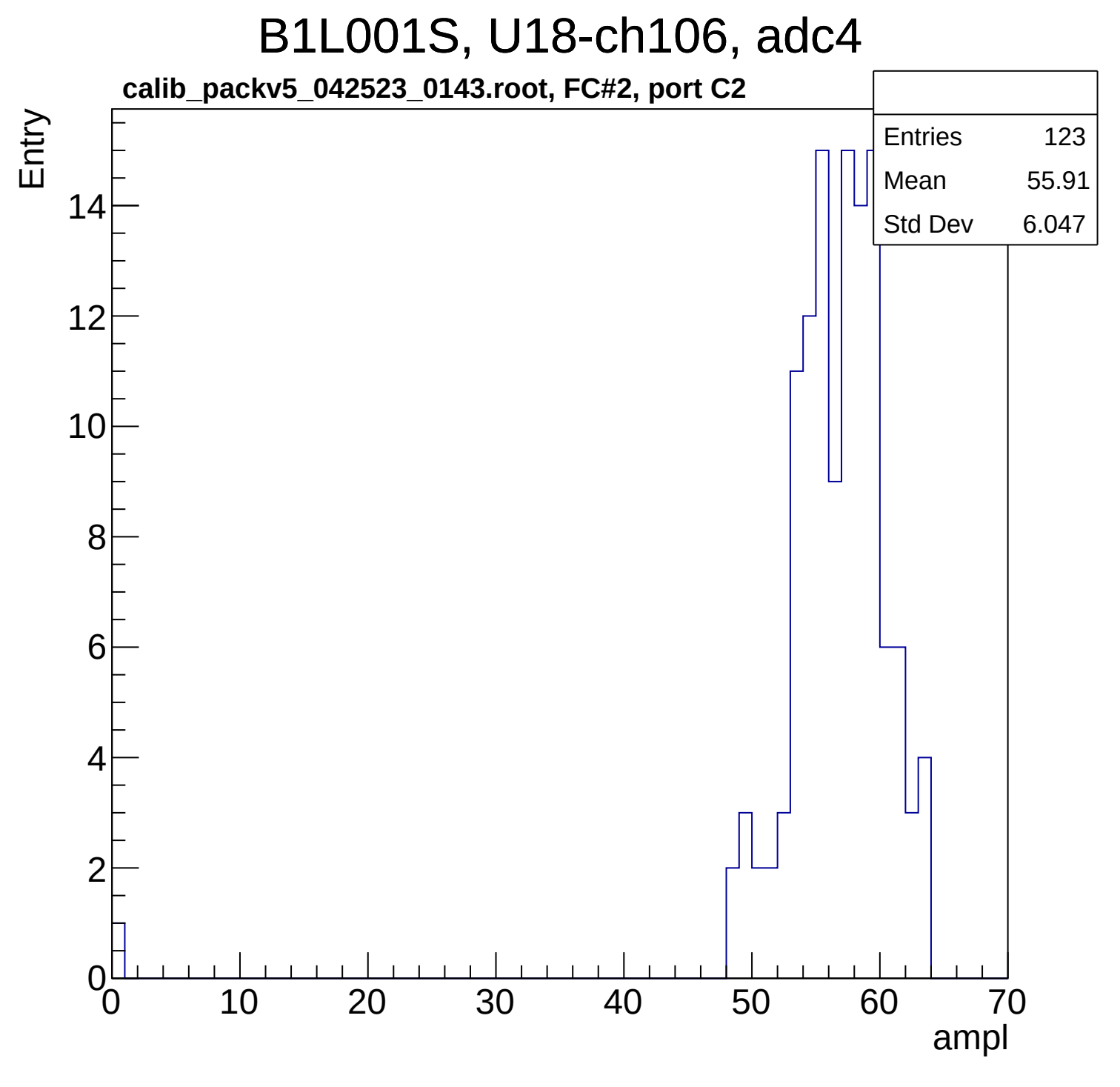

B1L001S, U18-ch105, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

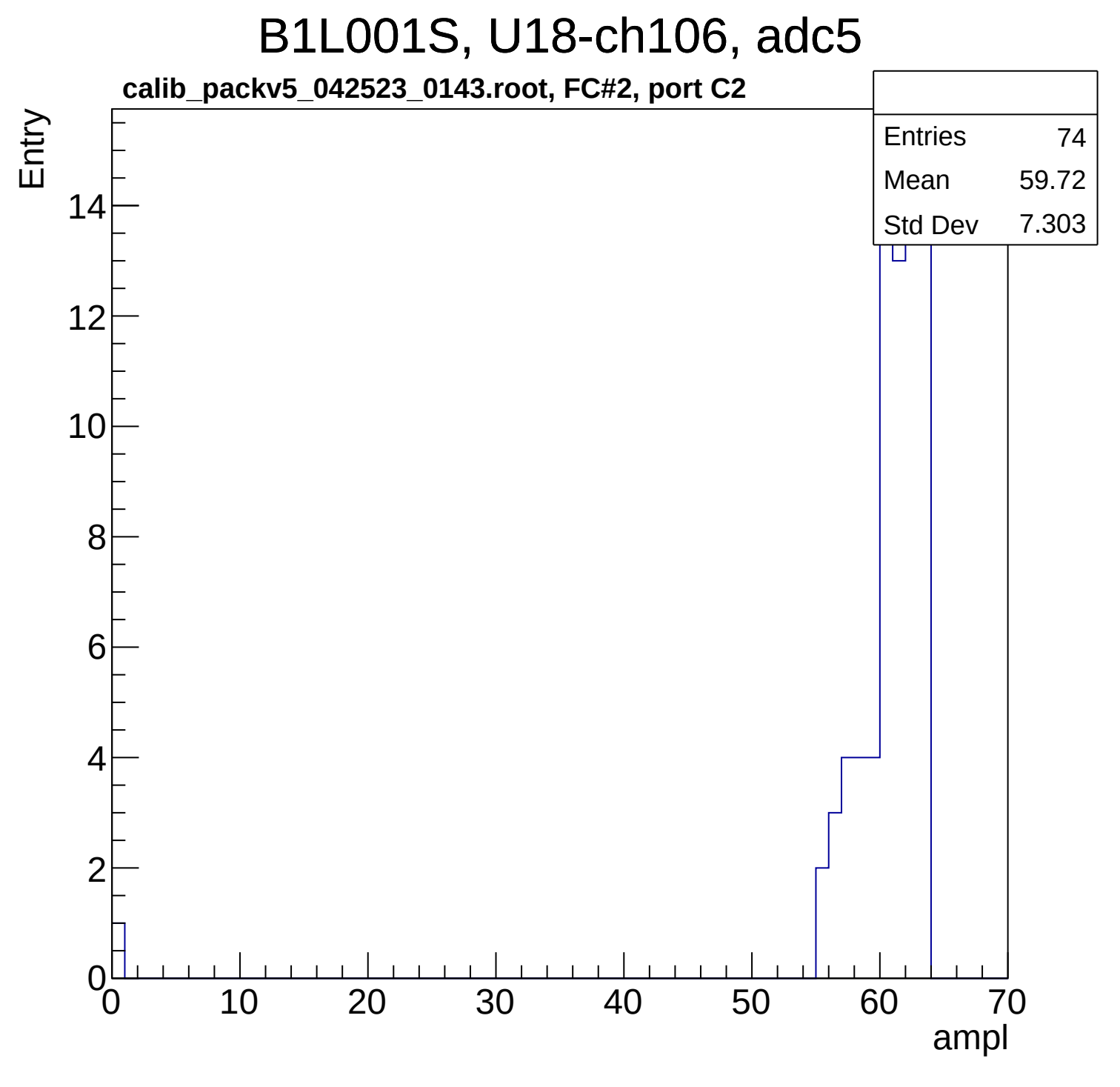

B1L001S, U18-ch106, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 146
Mean 30.77
Std Dev 4.516
Gaus mean : 31.5222
Gaus Width: 3.8293
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

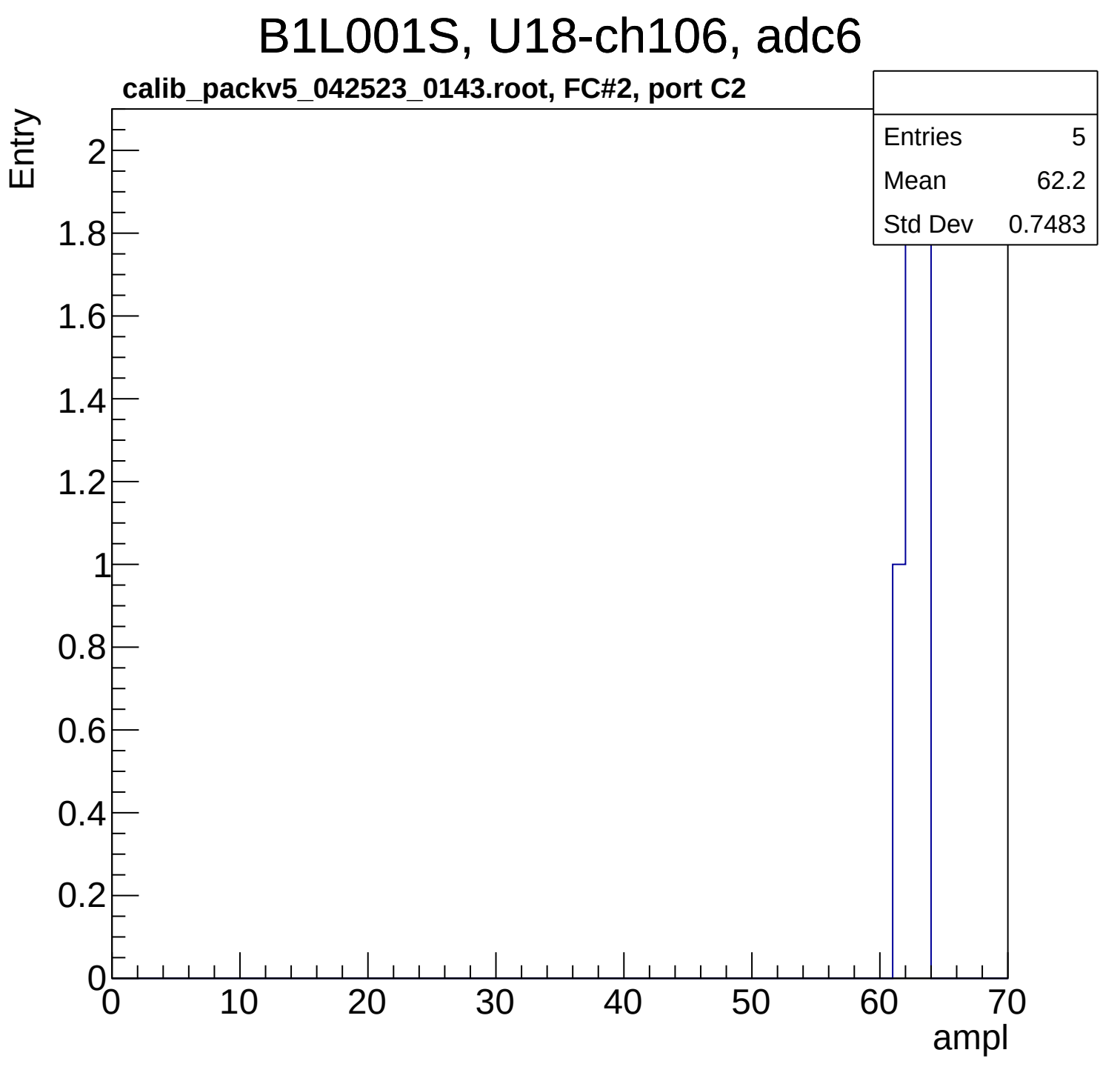

B1L001S, U18-ch106, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 133
Mean 37.73
Std Dev 3.784
Gaus mean : 38.2442
Gaus Width: 3.6616
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

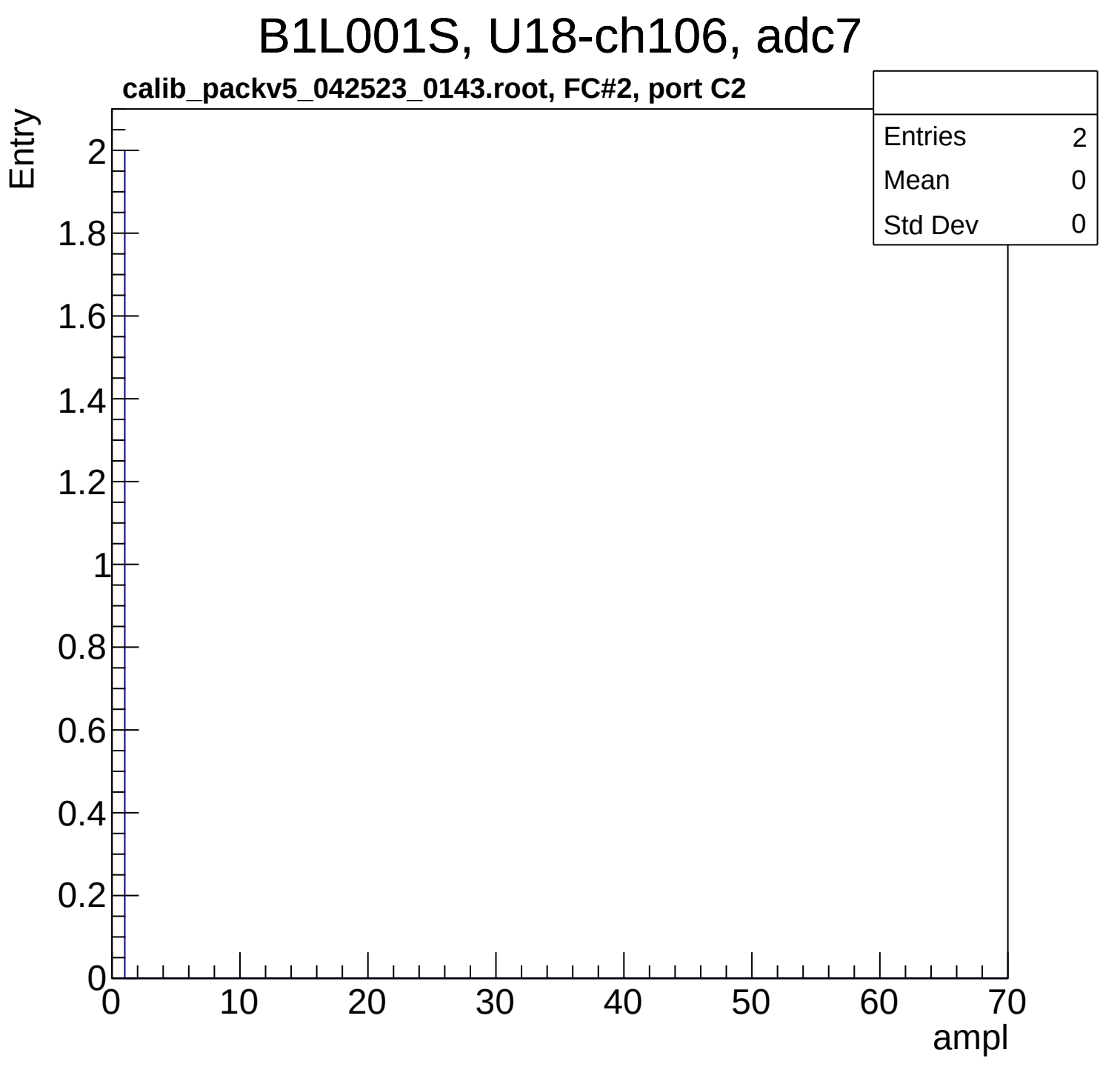

B1L001S, U18-ch106, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 126
Mean 44.03
Std Dev 3.338
Gaus mean : 44.5457
Gaus Width: 3.4226
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

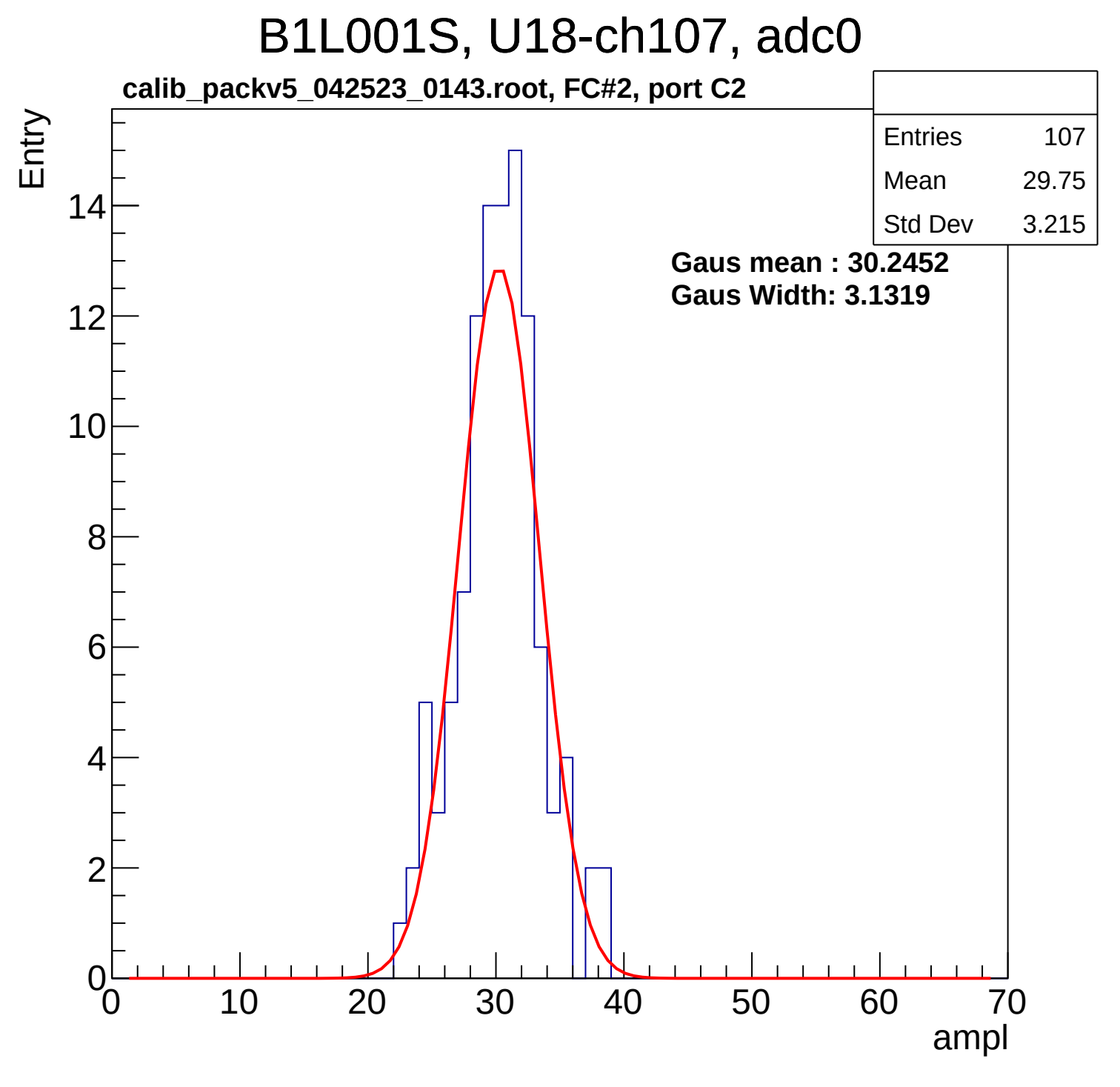

B1L001S, U18-ch106, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 122
Mean 50.61
Std Dev 3.362
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

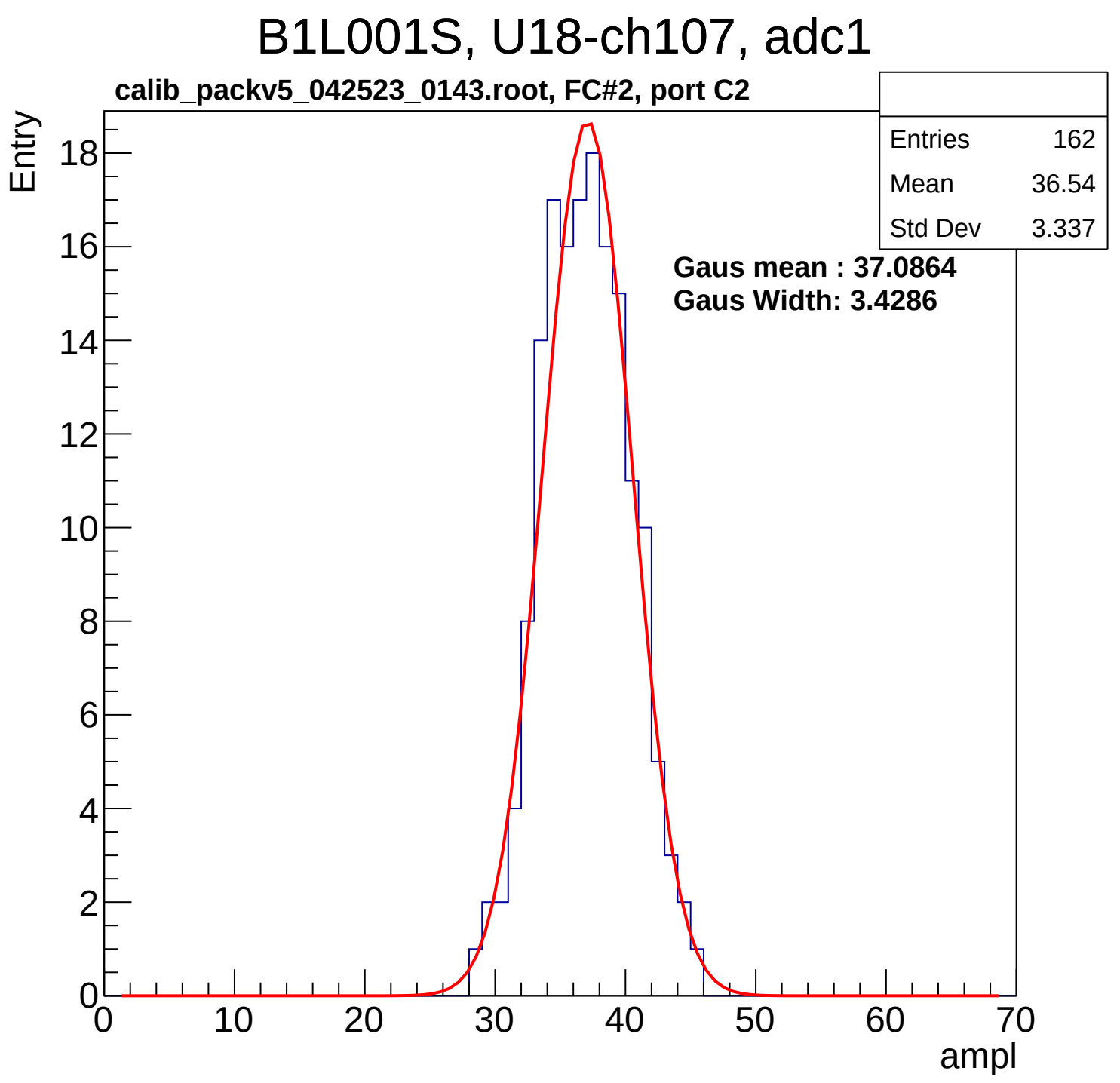

B1L001S, U18-ch106, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 123
Mean 55.91
Std Dev 6.047
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

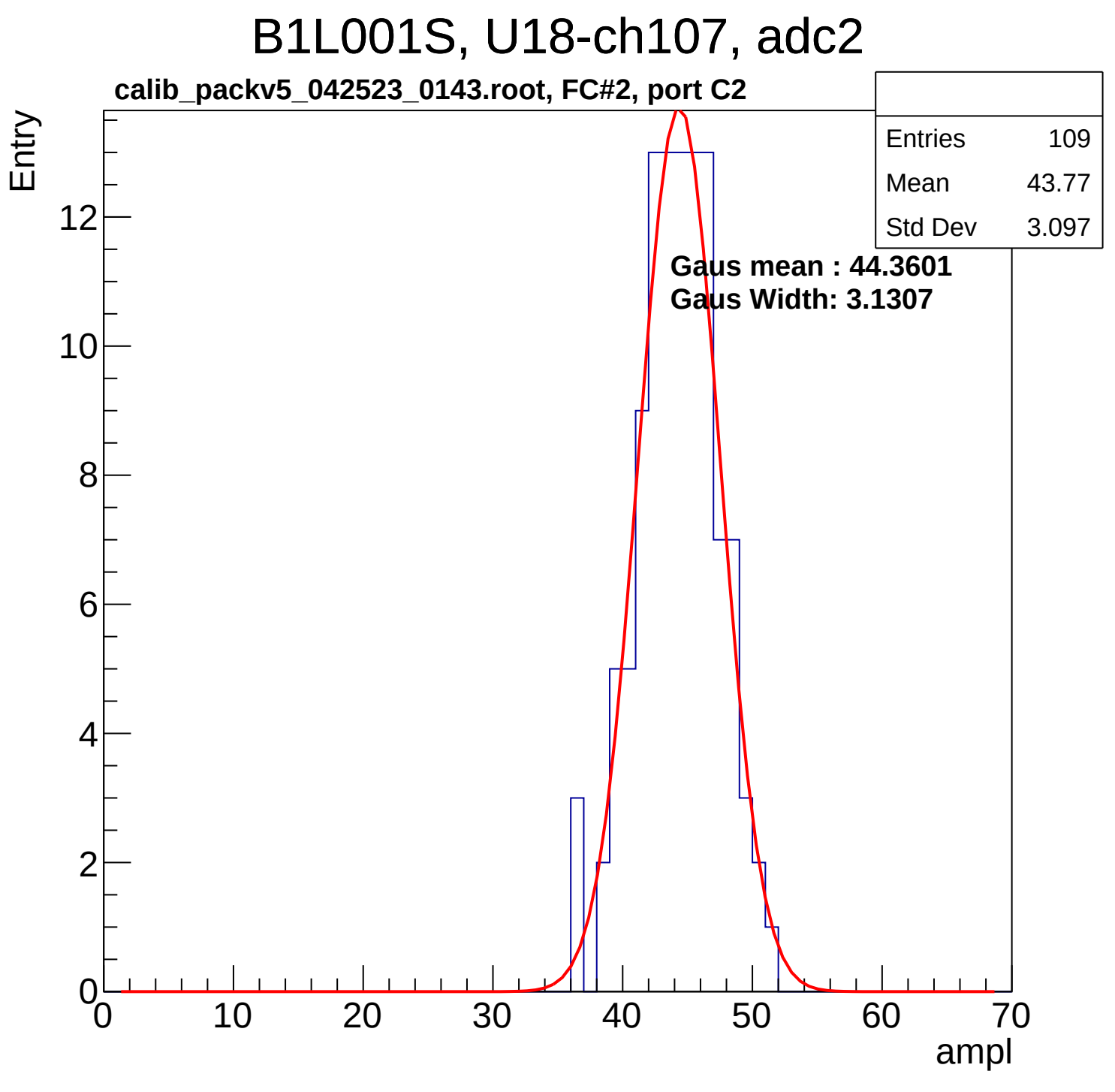

B1L001S, U18-ch106, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 74
Mean 59.72
Std Dev 7.303
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl

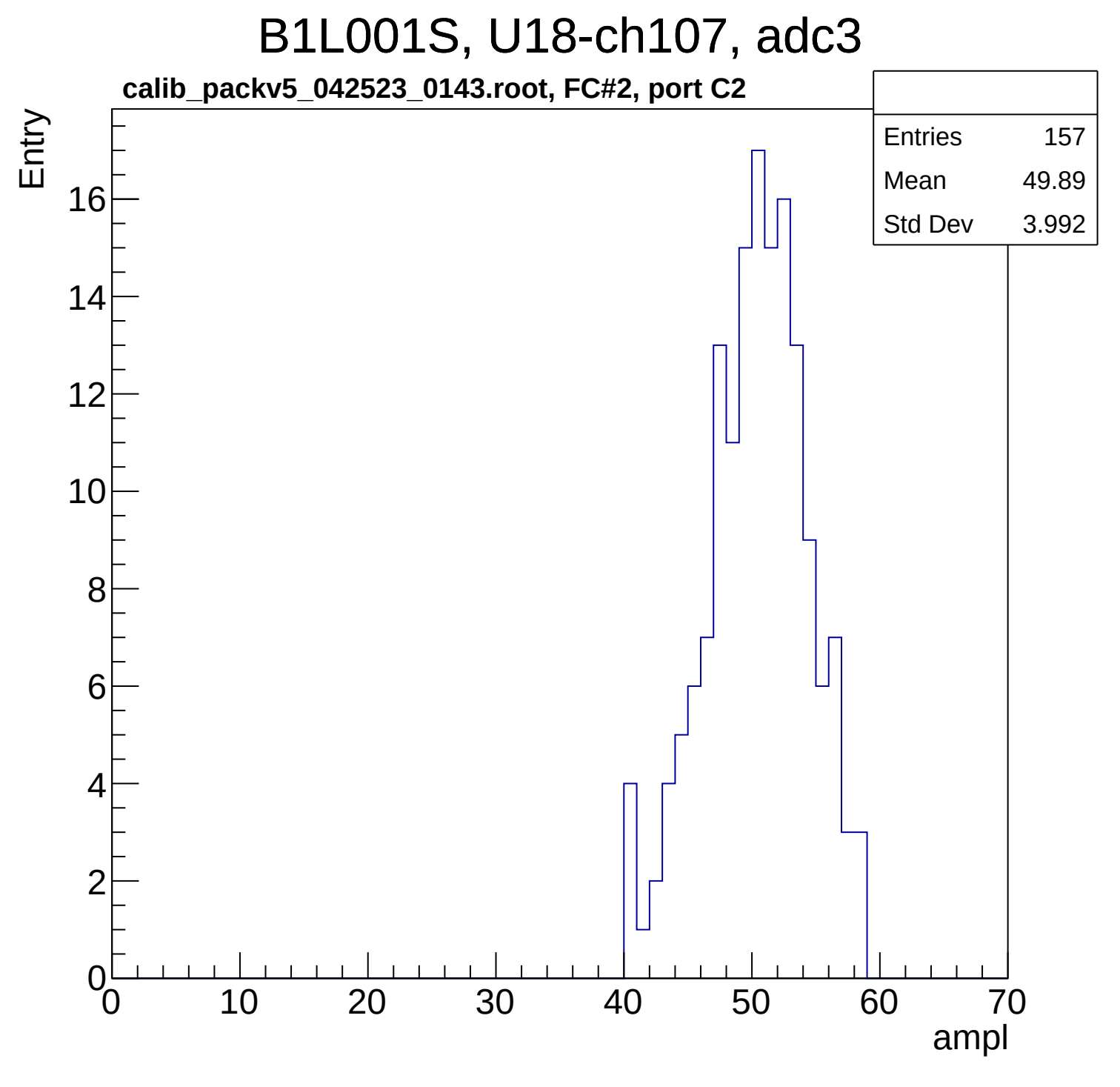

B1L001S, U18-ch106, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 5
Mean 62.2
Std Dev 0.7483
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

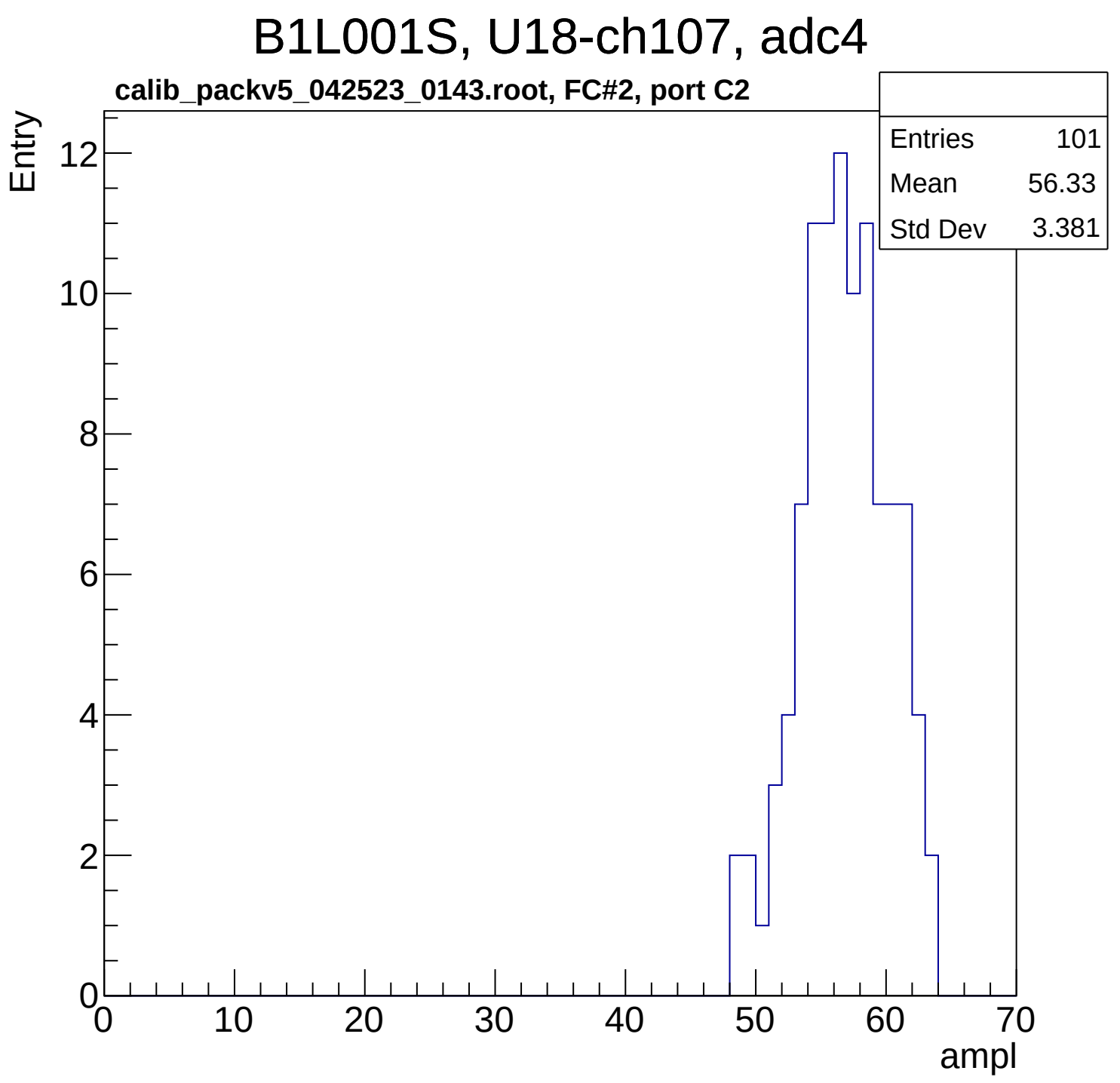

B1L001S, U18-ch106, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 0
Std Dev 0
Entry
2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

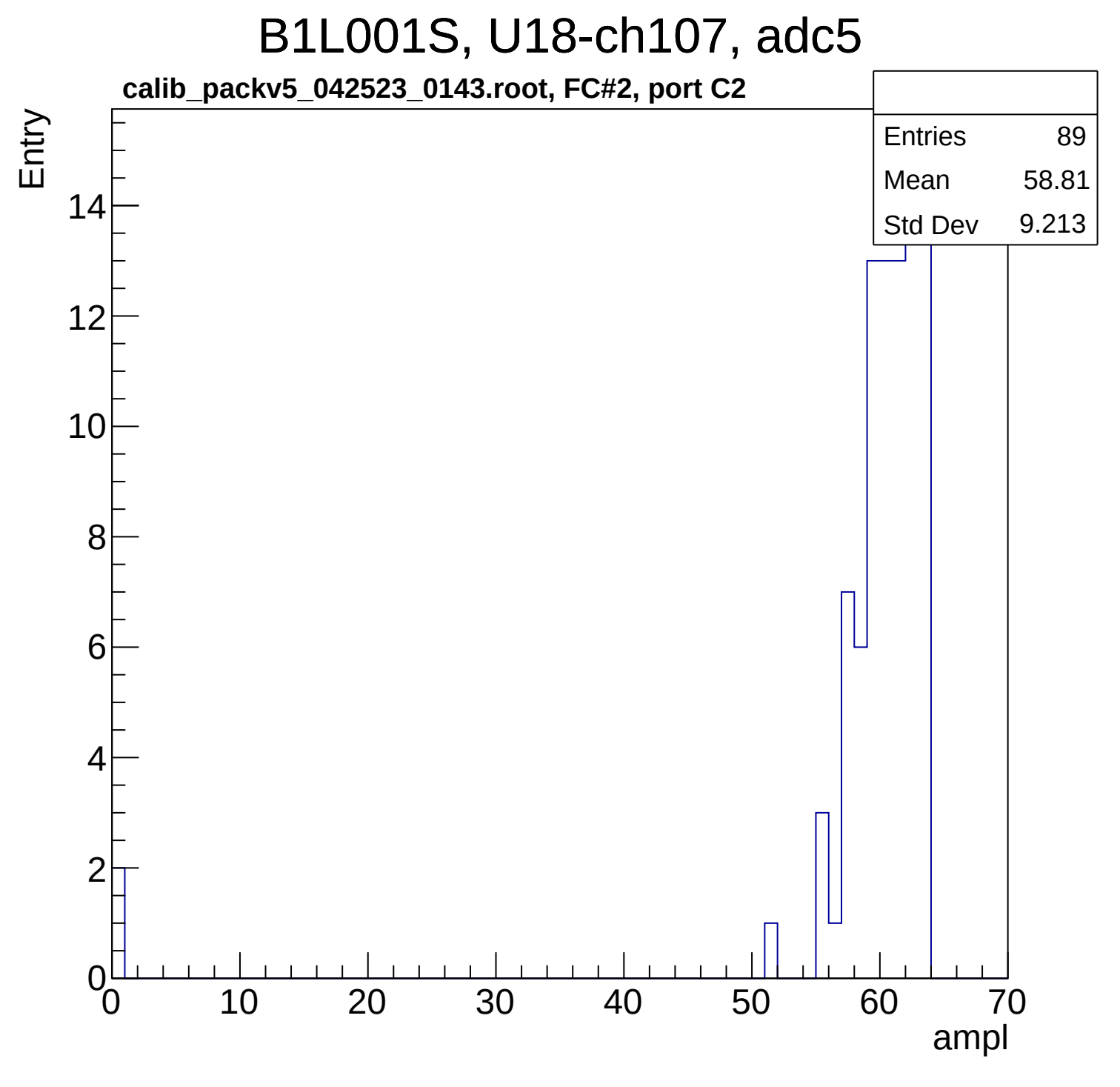

B1L001S, U18-ch107, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 107
Mean 29.75
Std Dev 3.215
Gaus mean : 30.2452
Gaus Width: 3.1319
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

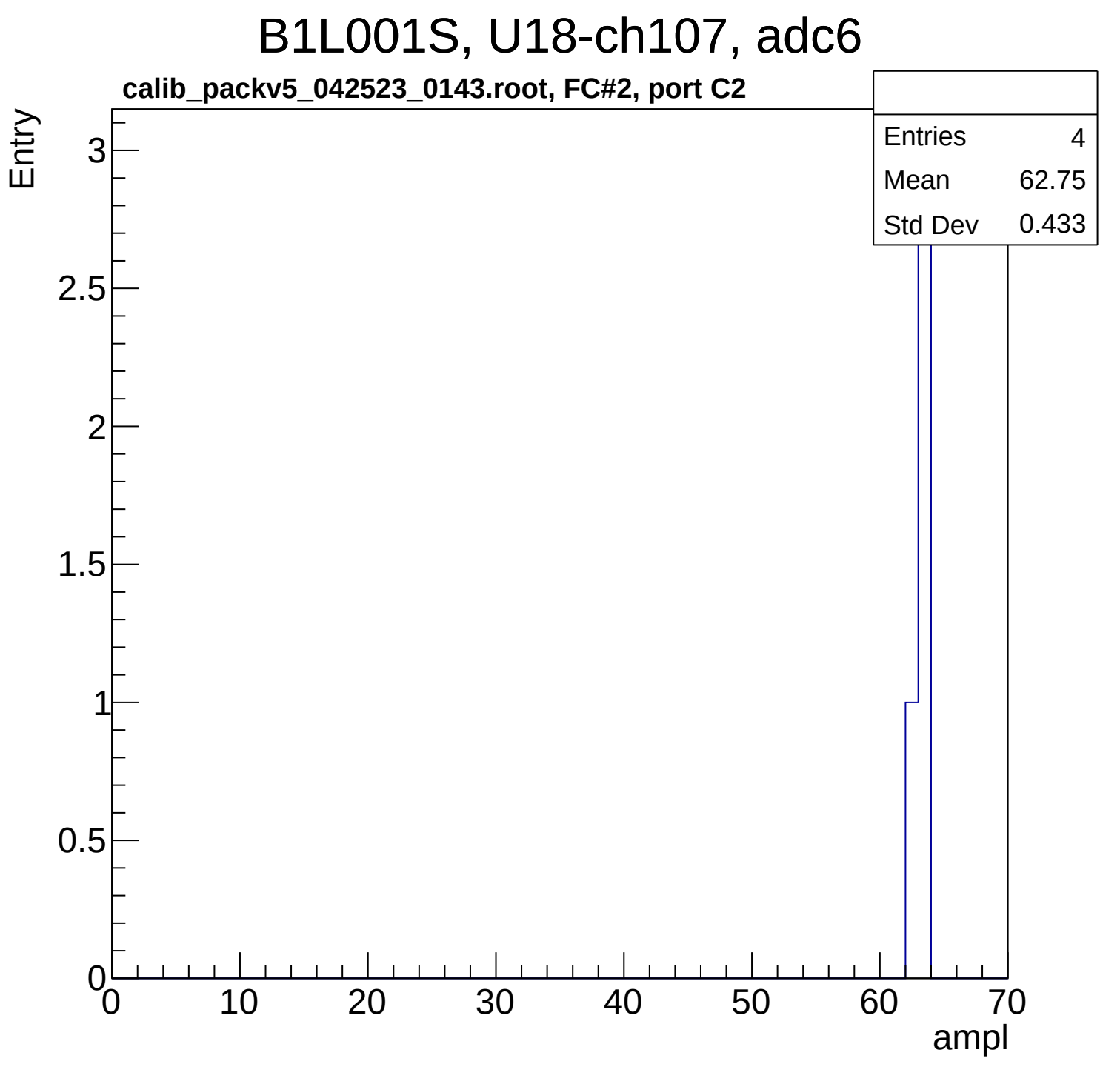

B1L001S, U18-ch107, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 162
Mean 36.54
Std Dev 3.337
Gaus mean : 37.0864
Gaus Width: 3.4286
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

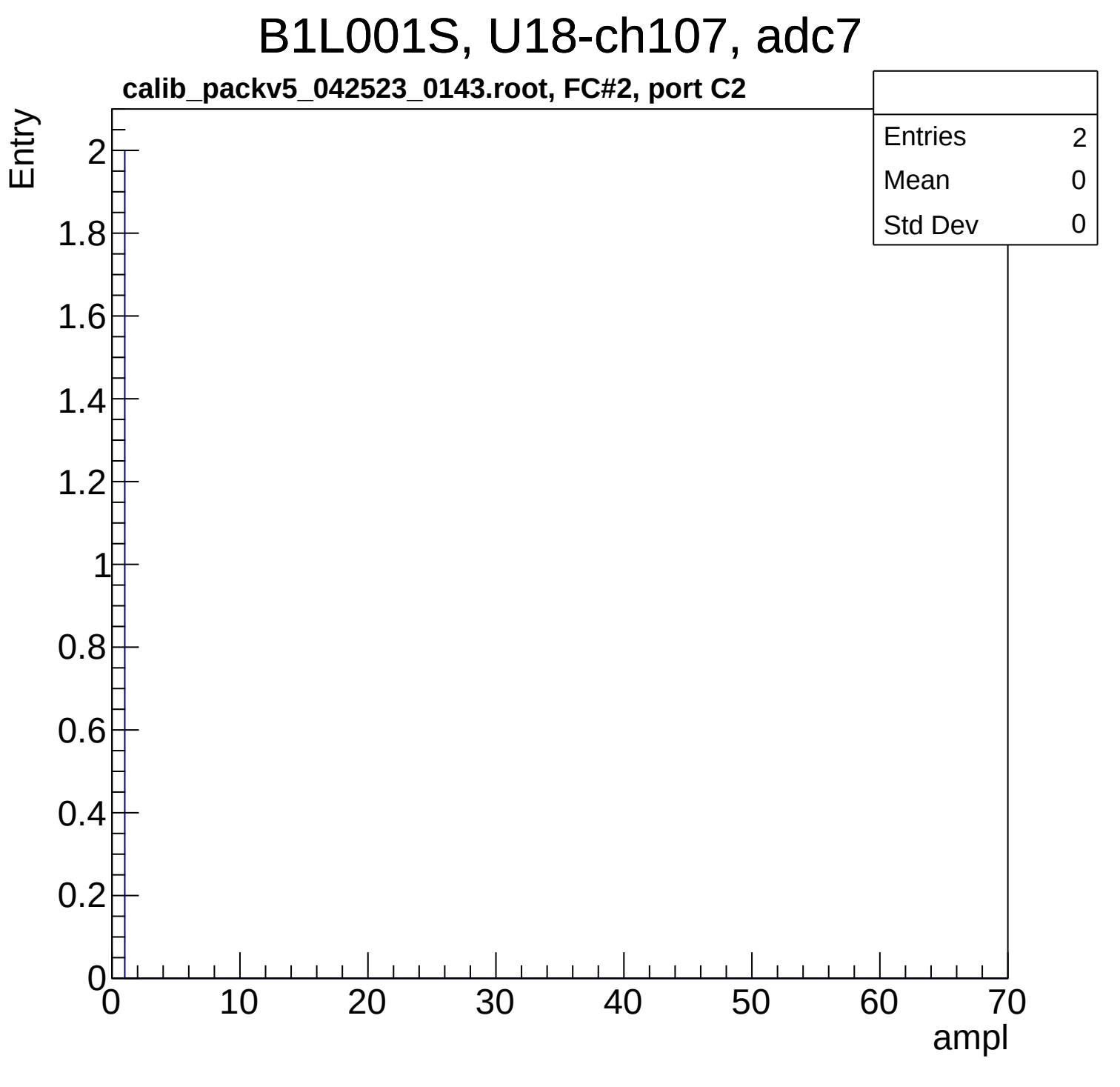

B1L001S, U18-ch107, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 109
Mean 43.77
Std Dev 3.097
Gaus mean : 44.3601
Gaus Width: 3.1307
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70

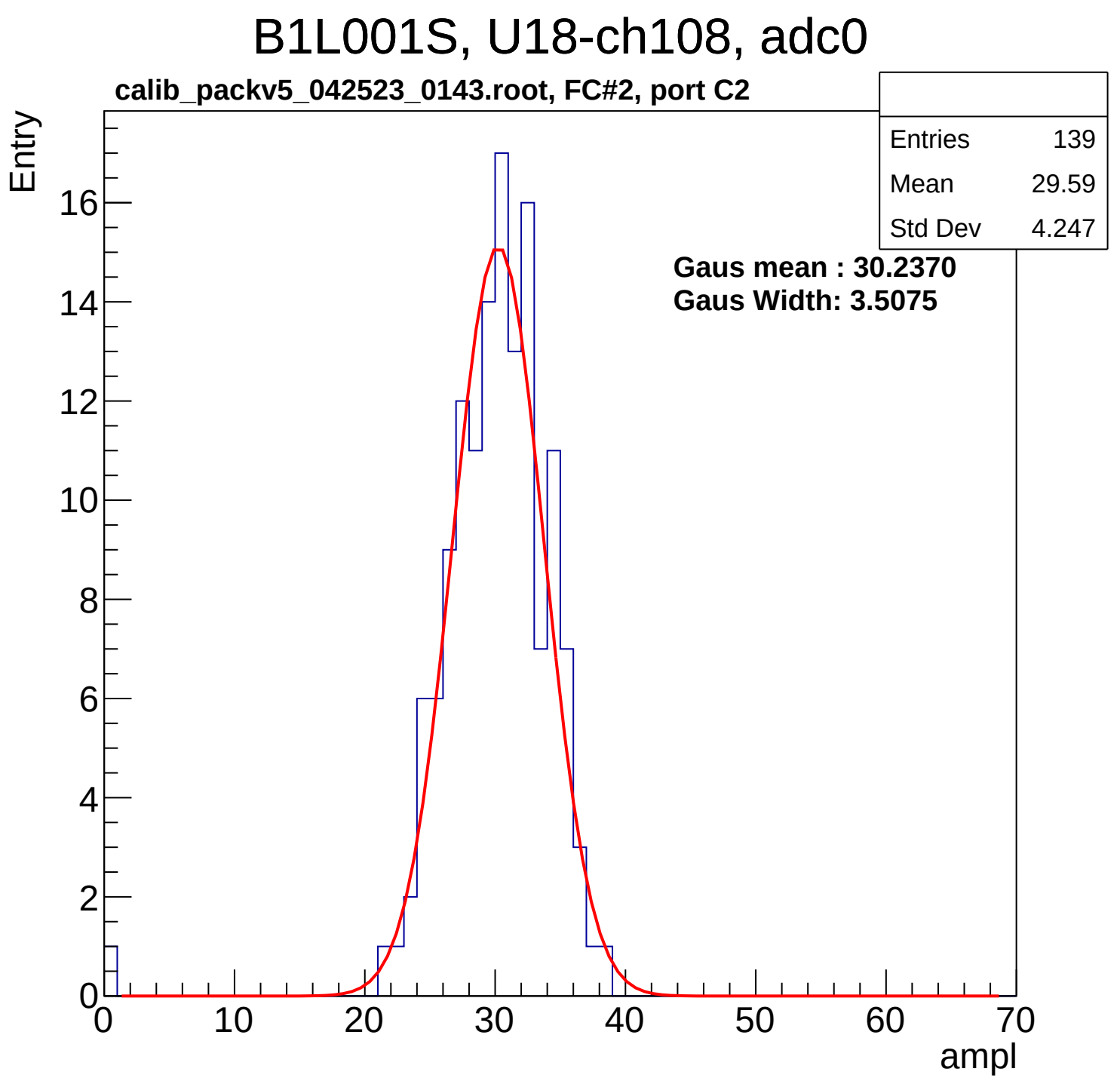

B1L001S, U18-ch107, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 157
Mean 49.89
Std Dev 3.992
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

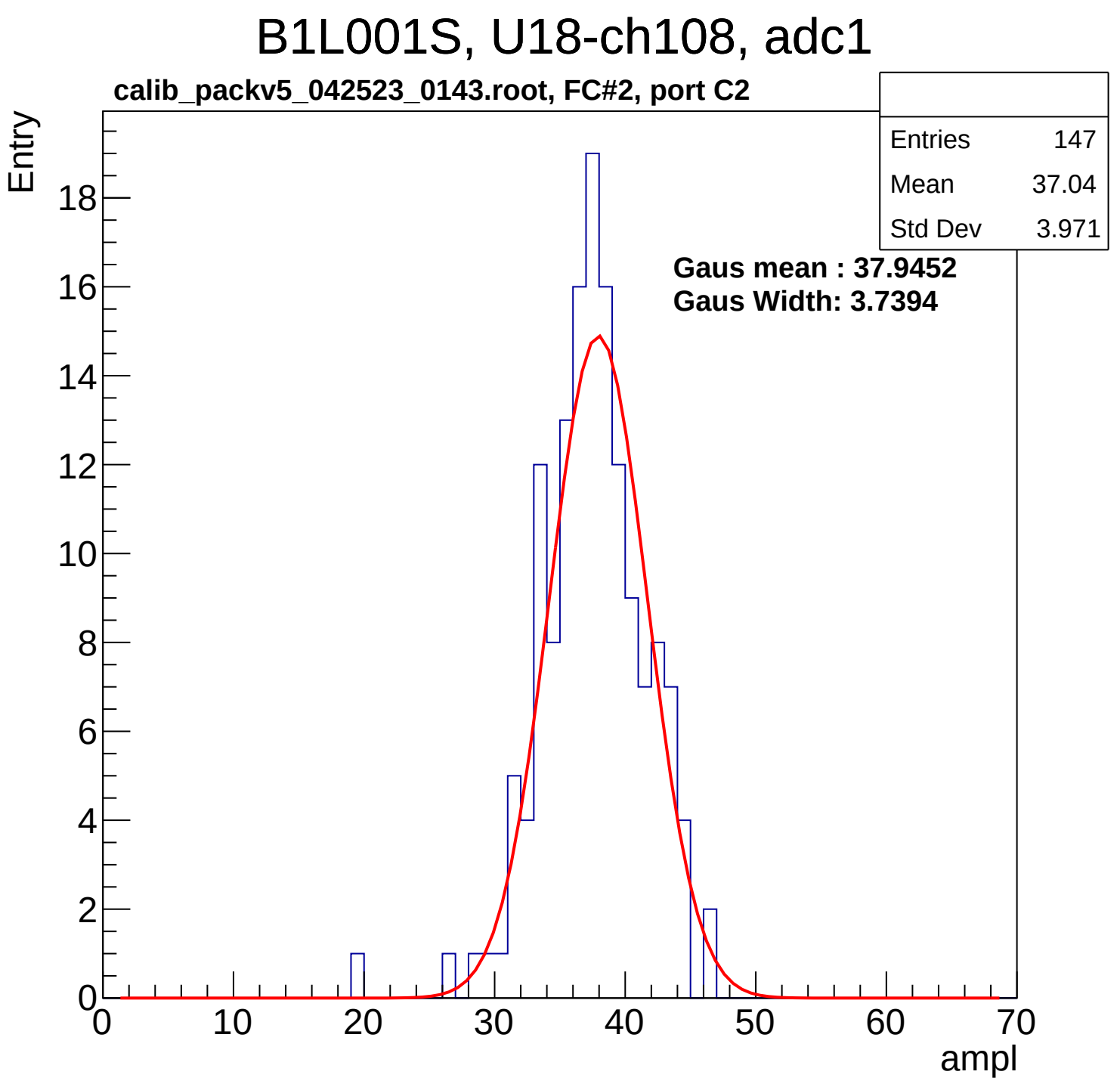

B1L001S, U18-ch107, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 101
Mean 56.33
Std Dev 3.381
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70

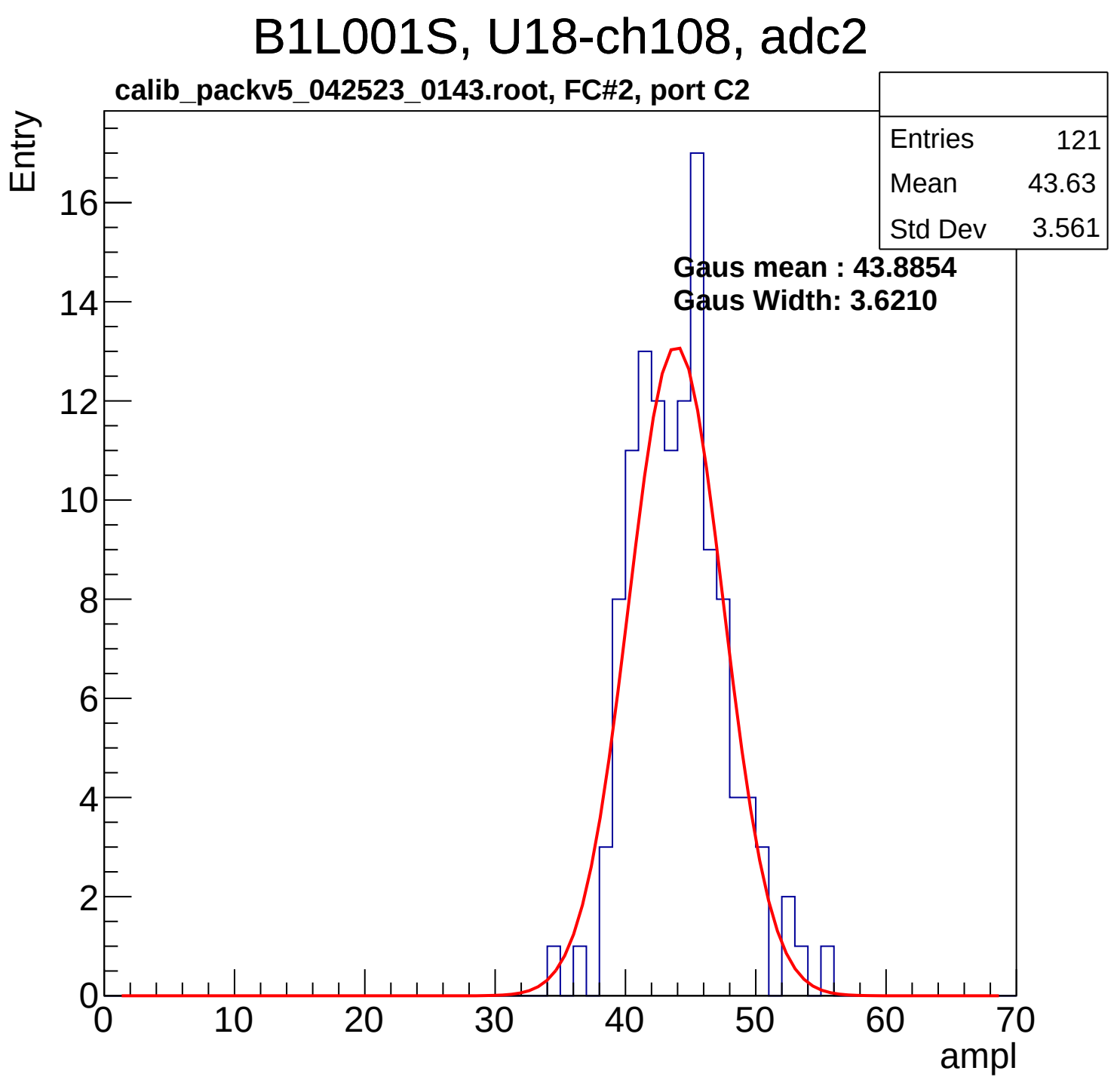

B1L001S, U18-ch107, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 89
Mean 58.81
Std Dev 9.213
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl

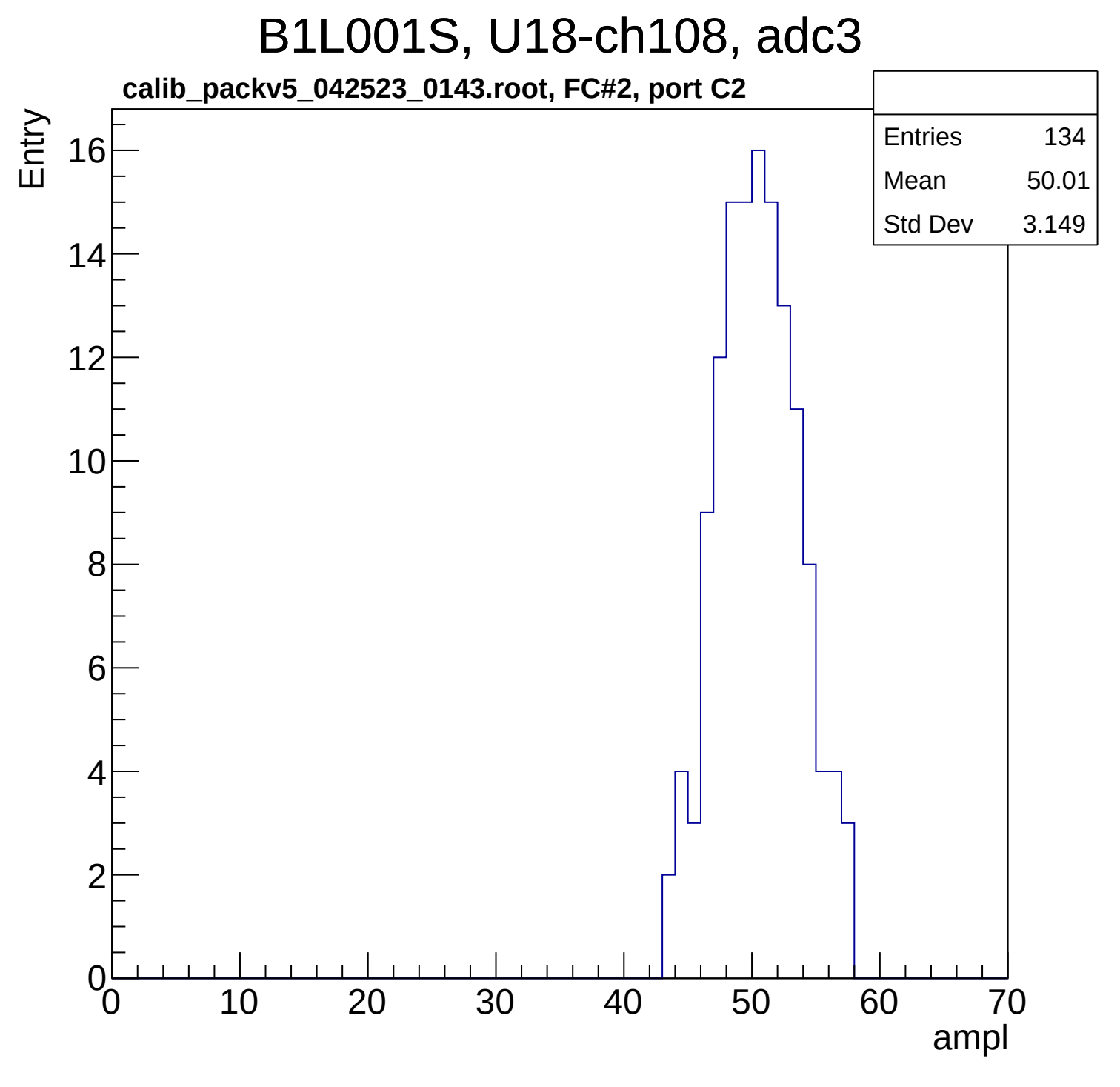

B1L001S, U18-ch107, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 4
Mean 62.75
Std Dev 0.433
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

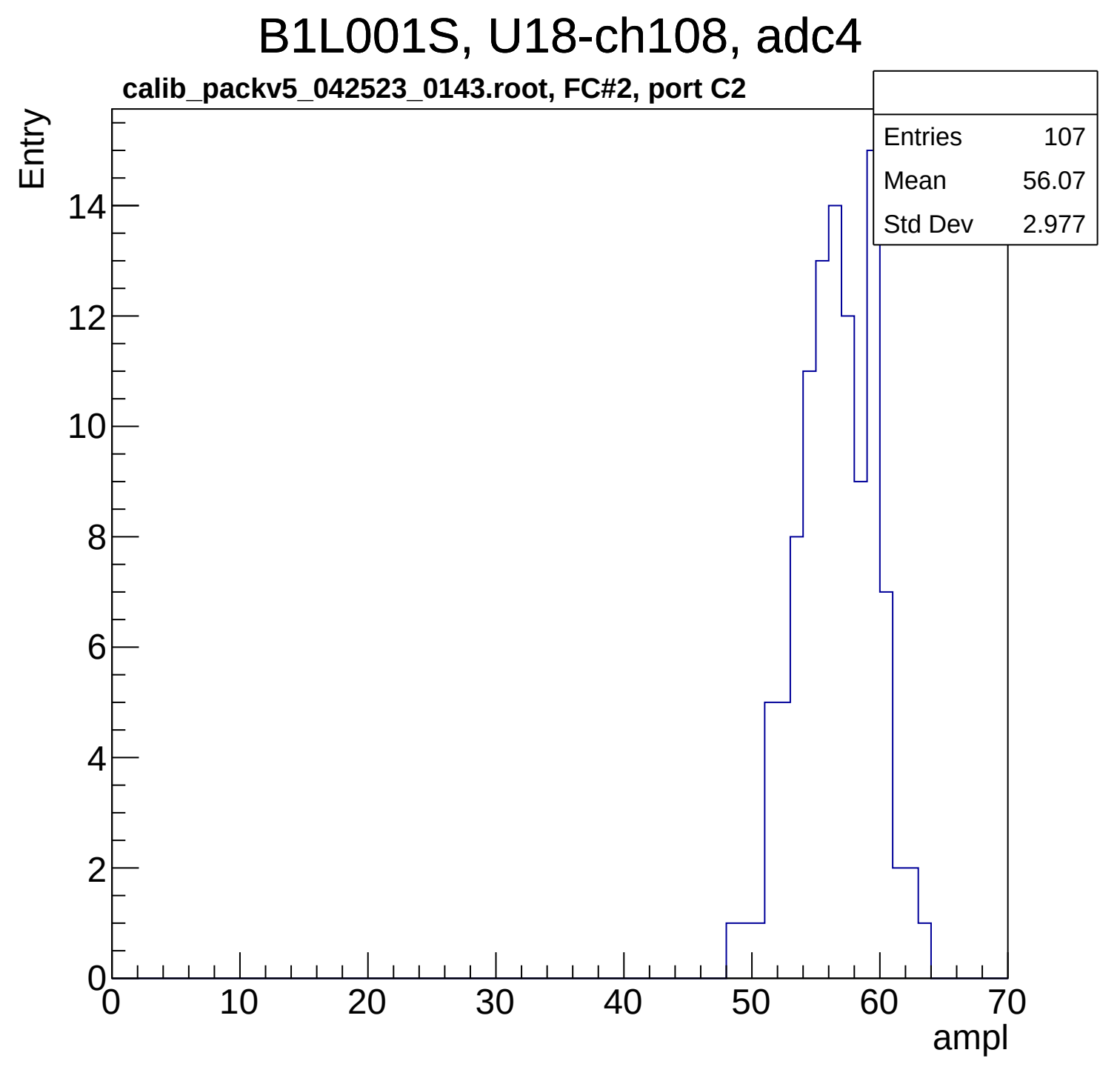

B1L001S, U18-ch107, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 0
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

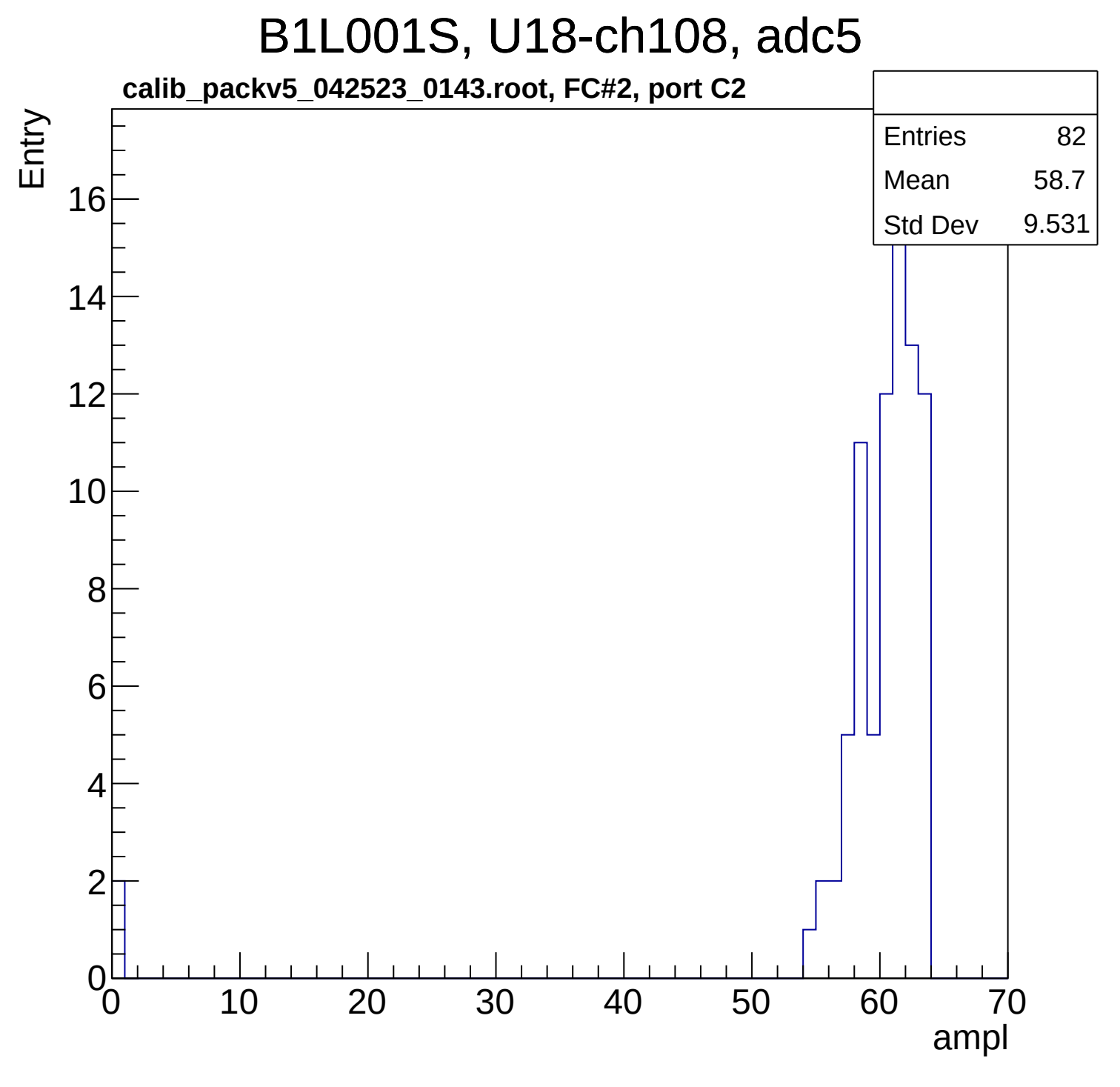

B1L001S, U18-ch108, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 139
Mean 29.59
Std Dev 4.247
Gaus mean : 30.2370
Gaus Width: 3.5075
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

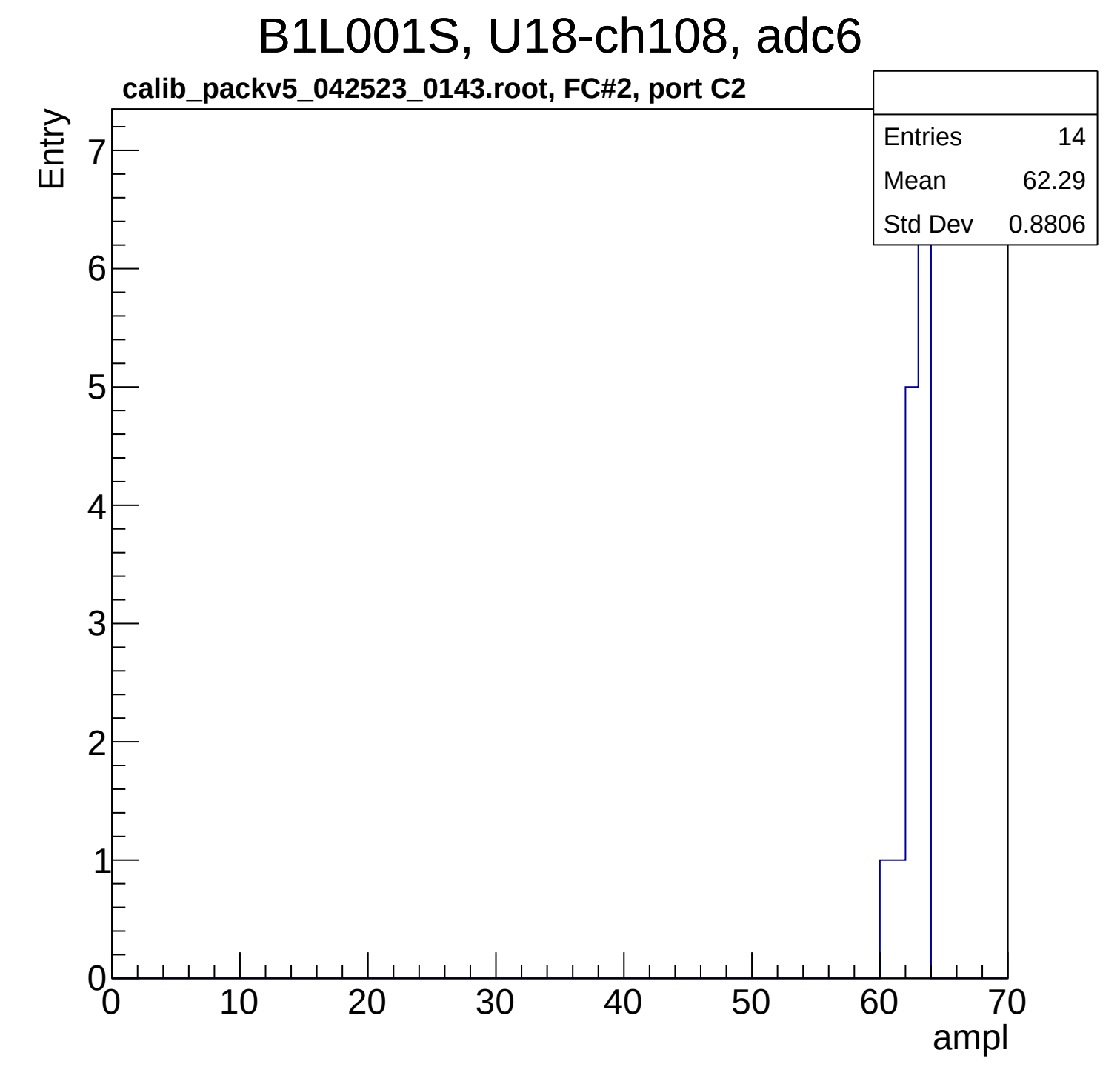

B1L001S, U18-ch108, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 147
Mean 37.04
Std Dev 3.971
Gaus mean : 37.9452
Gaus Width: 3.7394
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

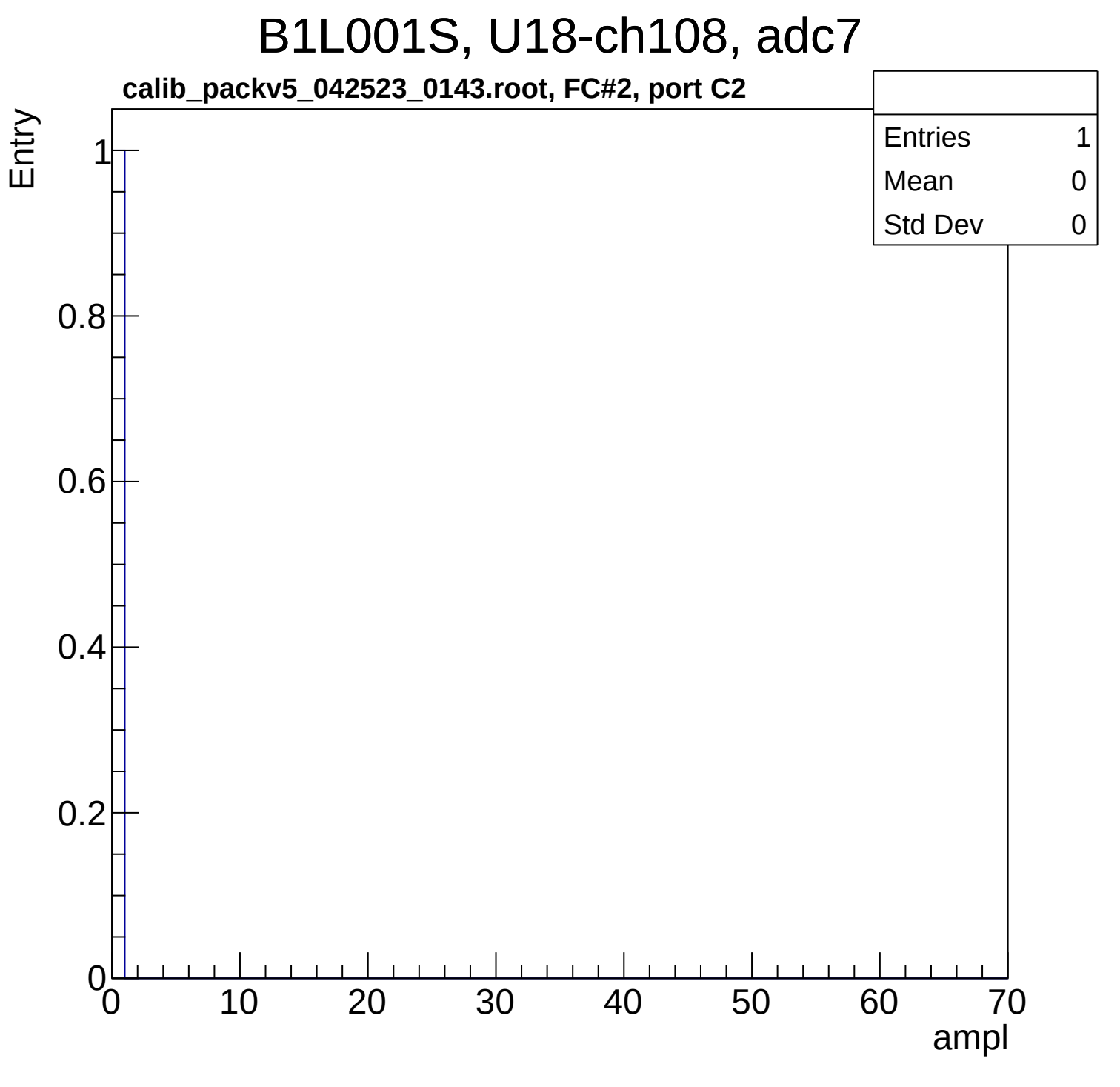

B1L001S, U18-ch108, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 121
Mean 43.63
Std Dev 3.561
Gaus mean : 43.8854
Gaus Width: 3.6210
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

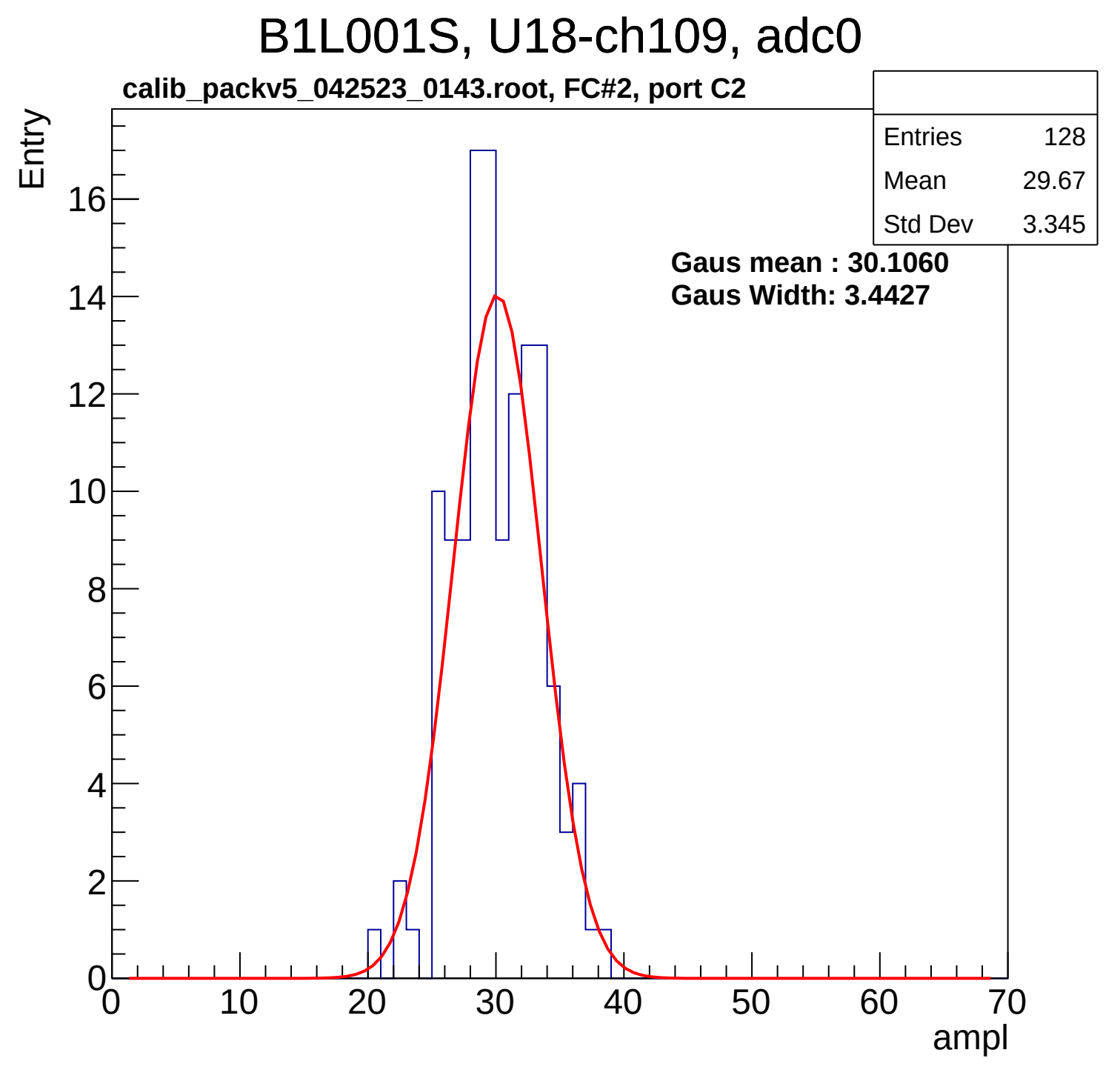

B1L001S, U18-ch108, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 134
Mean 50.01
Std Dev 3.149
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

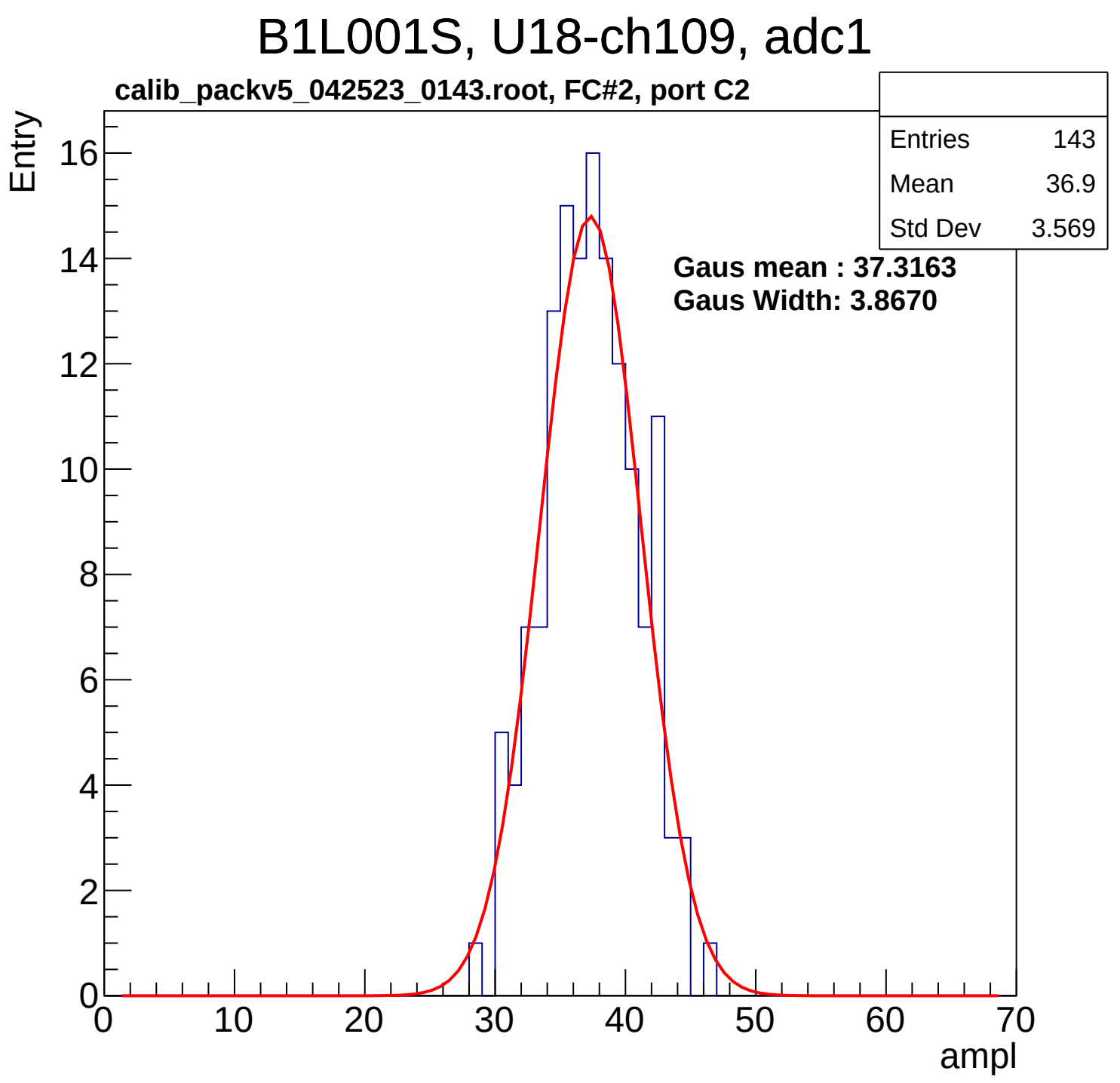

B1L001S, U18-ch108, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 107
Mean 56.07
Std Dev 2.977
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl

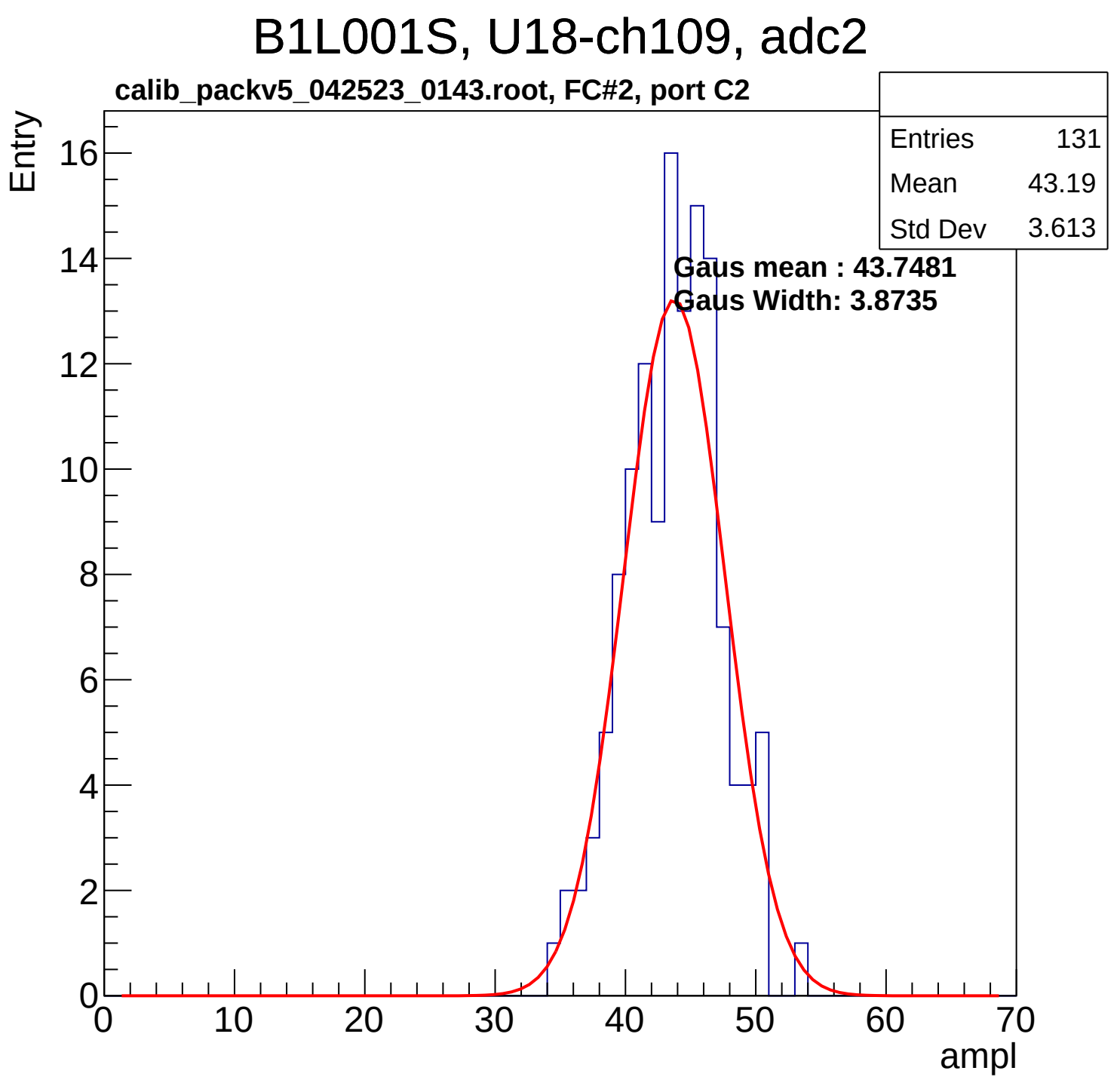

B1L001S, U18-ch108, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 82
Mean 58.7
Std Dev 9.531
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

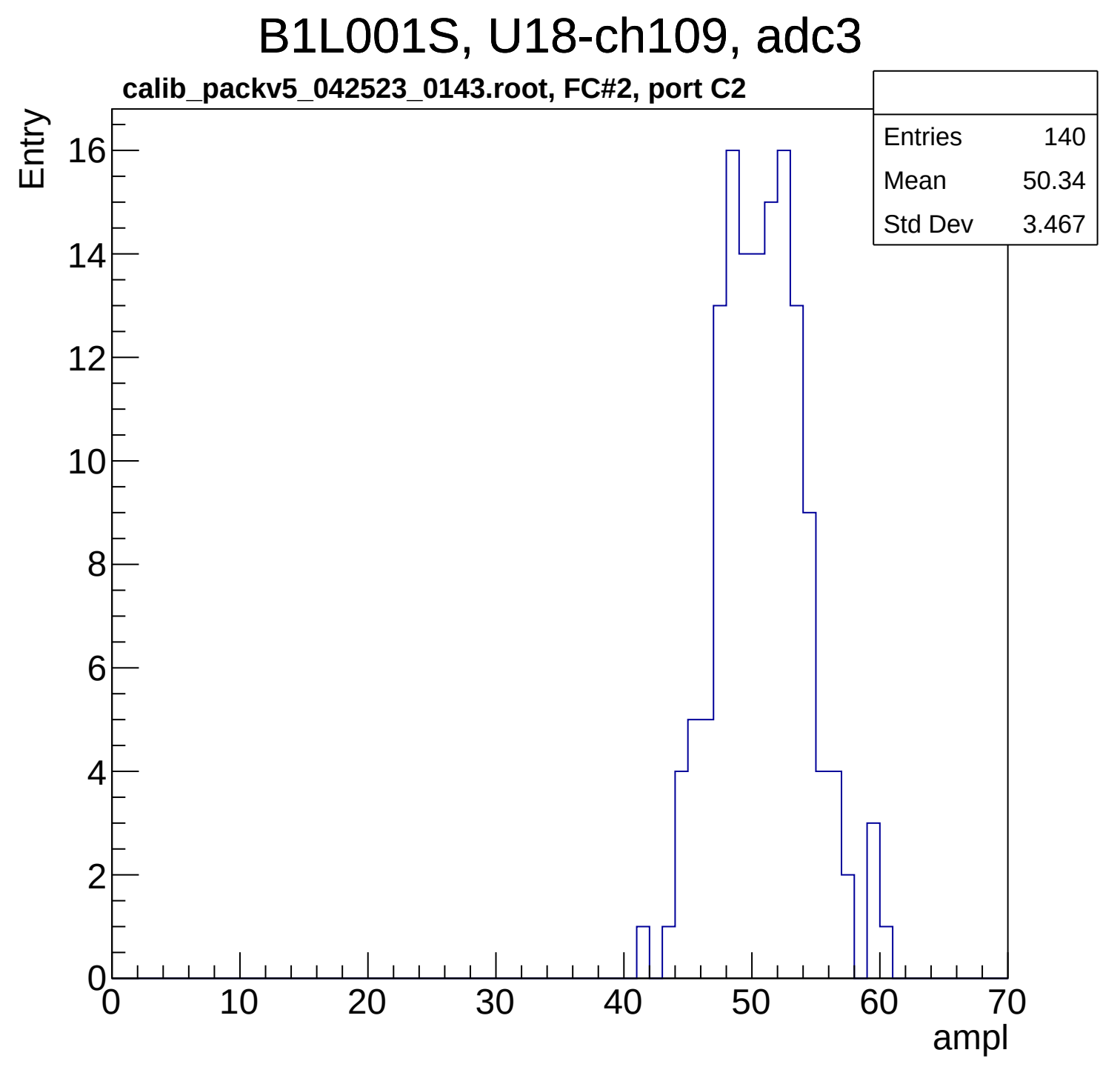

B1L001S, U18-ch108, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 14
Mean 62.29
Std Dev 0.8806
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

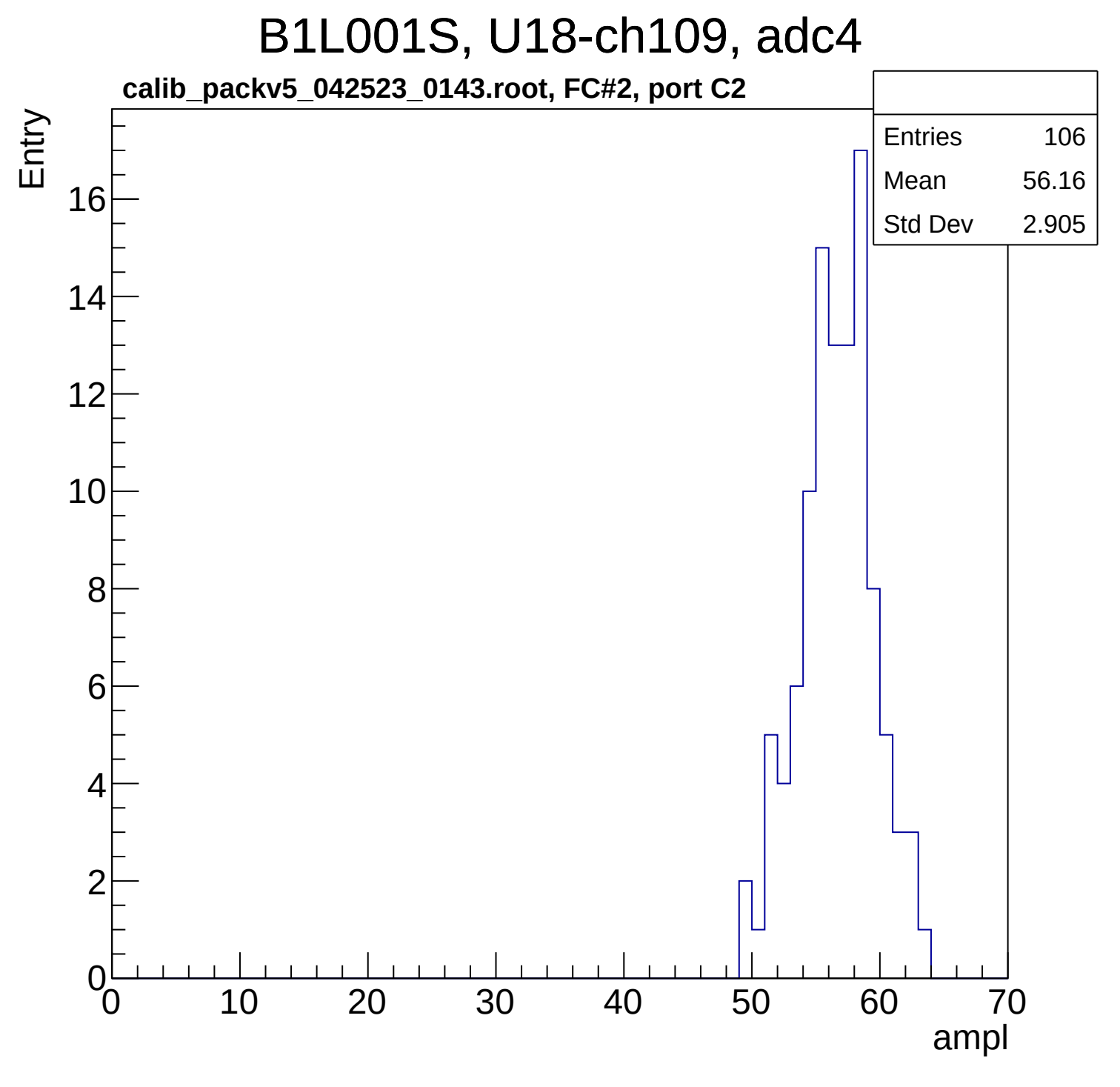

B1L001S, U18-ch108, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

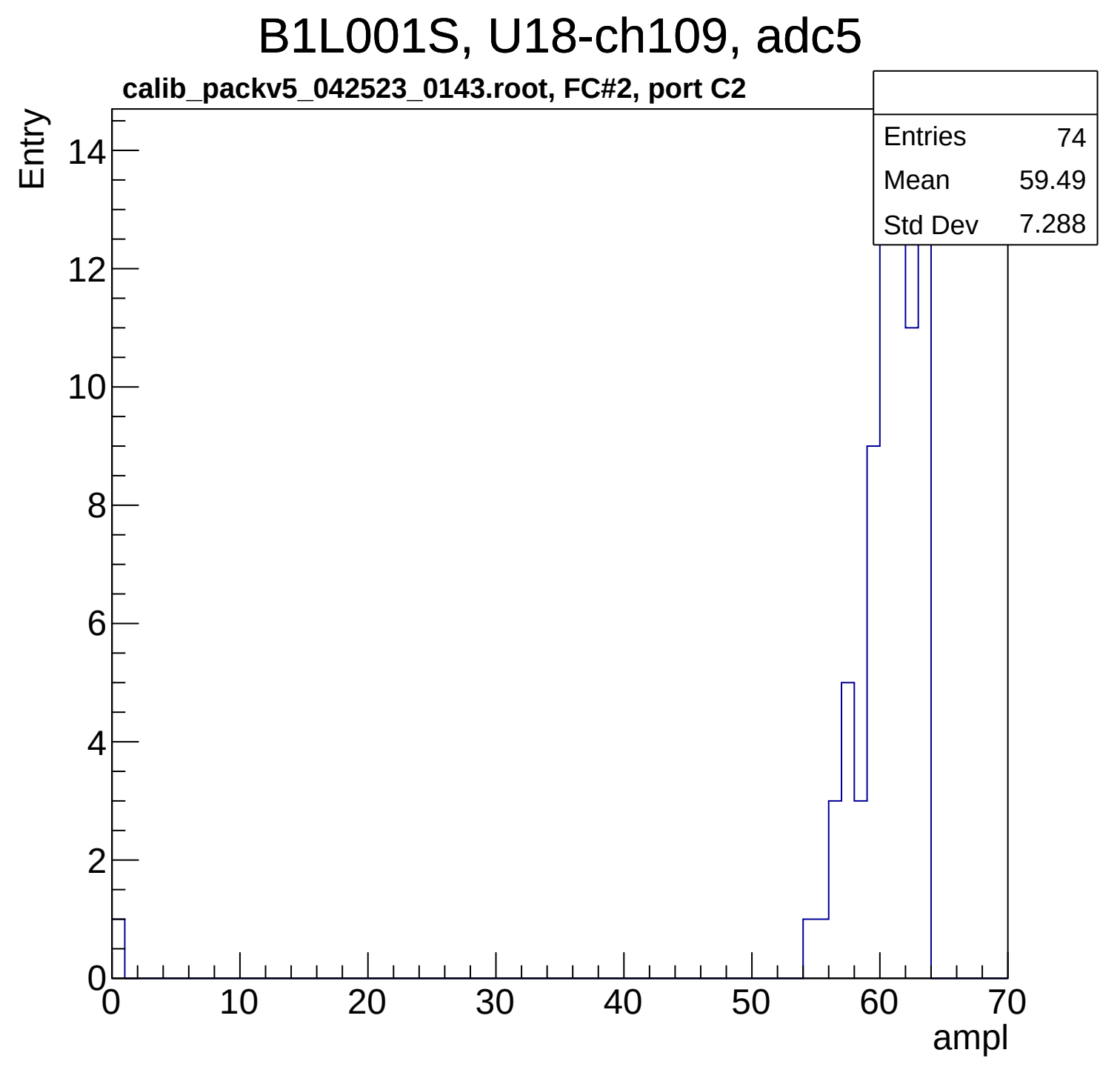

B1L001S, U18-ch109, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 128
Mean 29.67
Std Dev 3.345
Gaus mean : 30.1060
Gaus Width: 3.4427
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

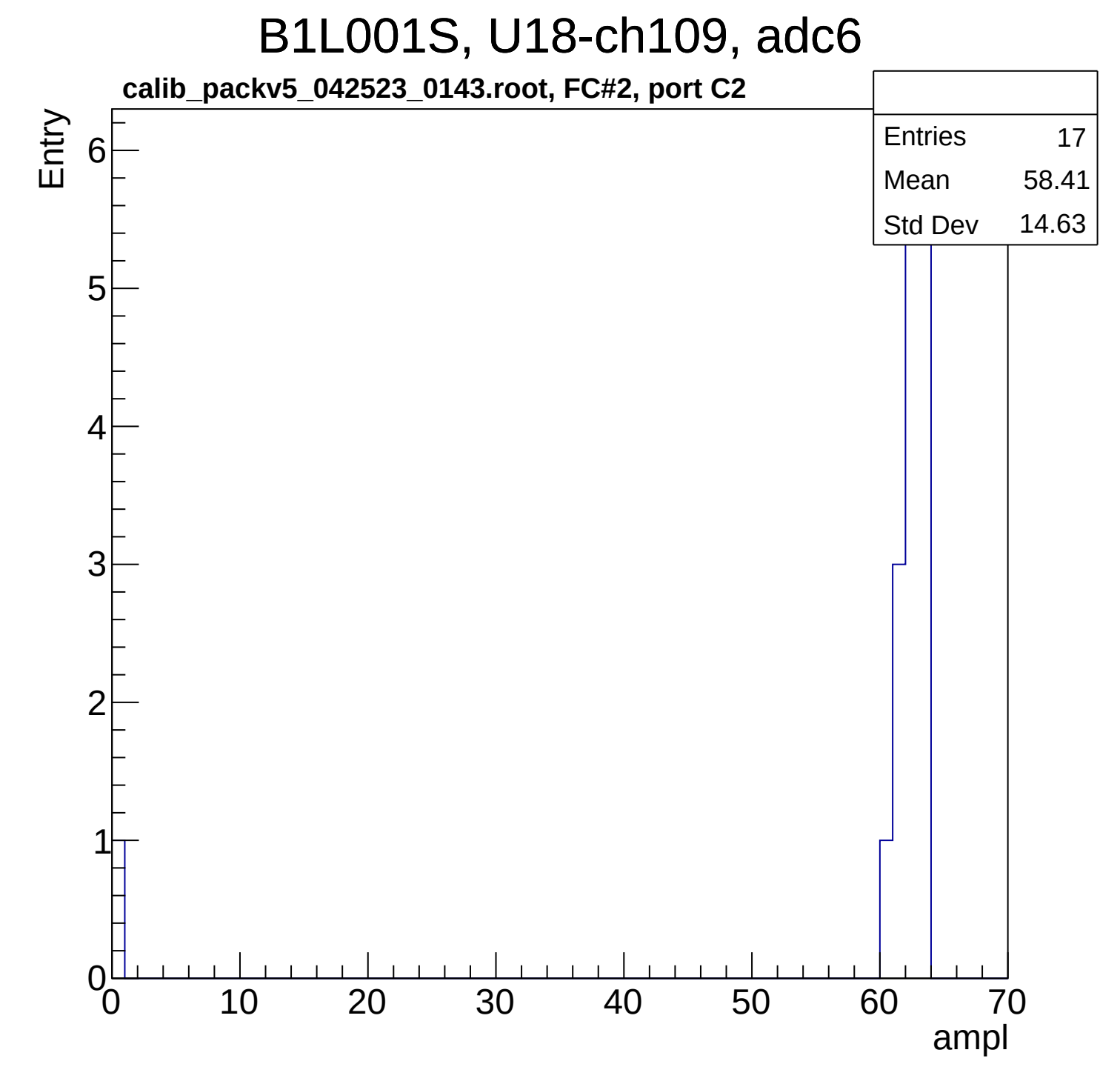

B1L001S, U18-ch109, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 143
Mean 36.9
Std Dev 3.569
Gaus mean : 37.3163
Gaus Width: 3.8670
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

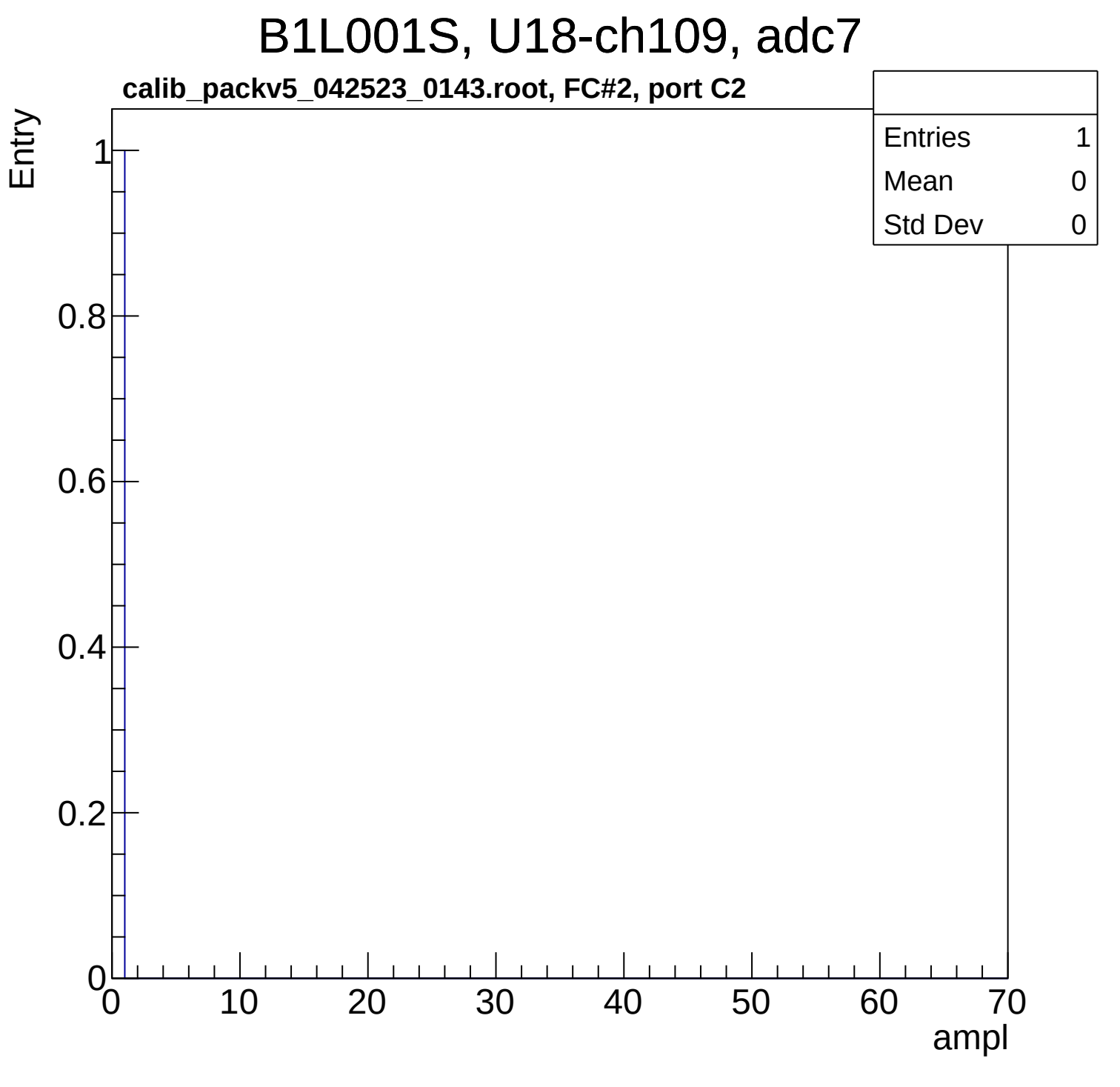

B1L001S, U18-ch109, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 131
Mean 43.19
Std Dev 3.613
Gaus mean : 43.7481
Gaus Width: 3.8735
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

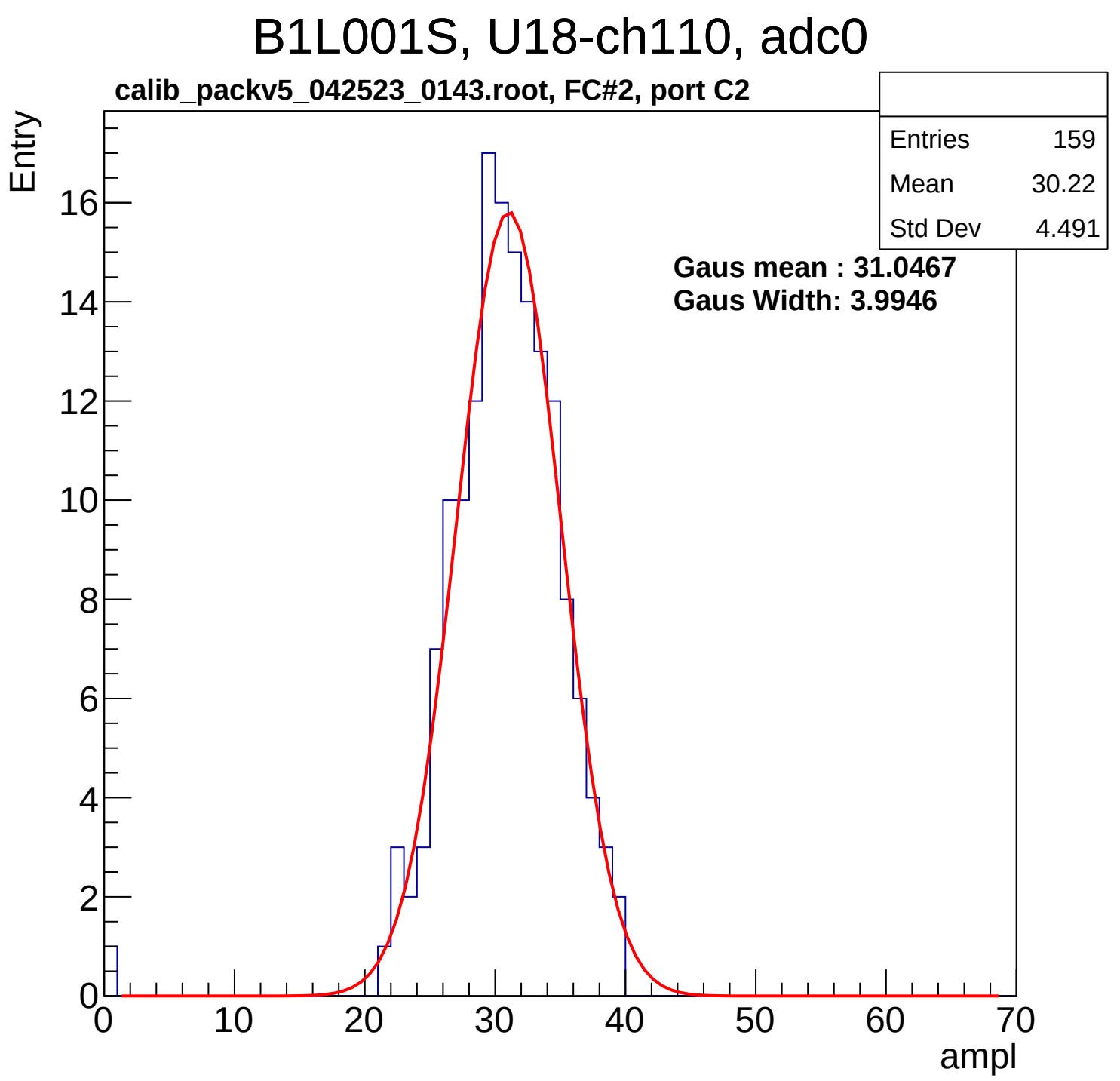

B1L001S, U18-ch109, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 140
Mean 50.34
Std Dev 3.467
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

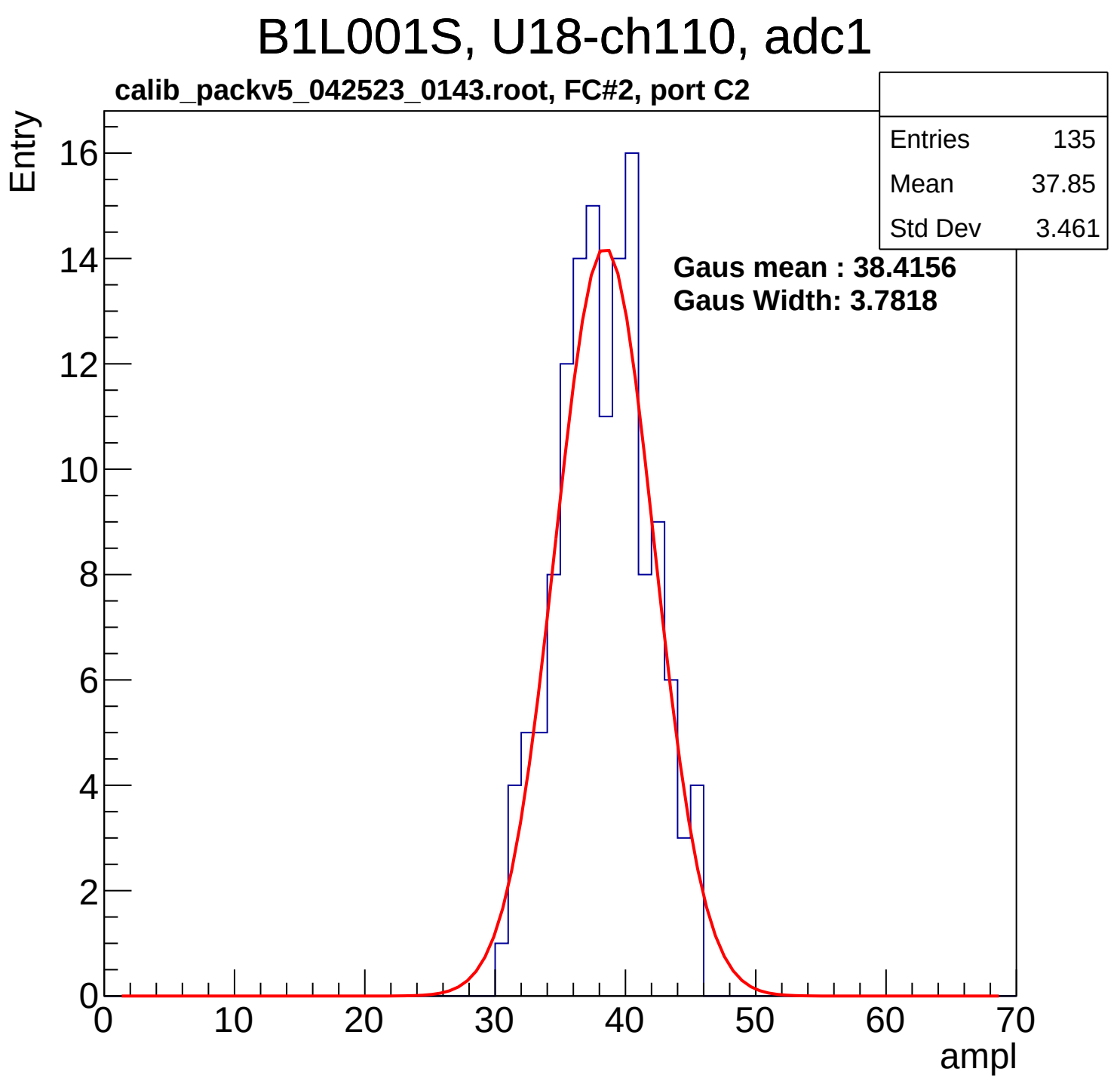

B1L001S, U18-ch109, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 106
Mean 56.16
Std Dev 2.905
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

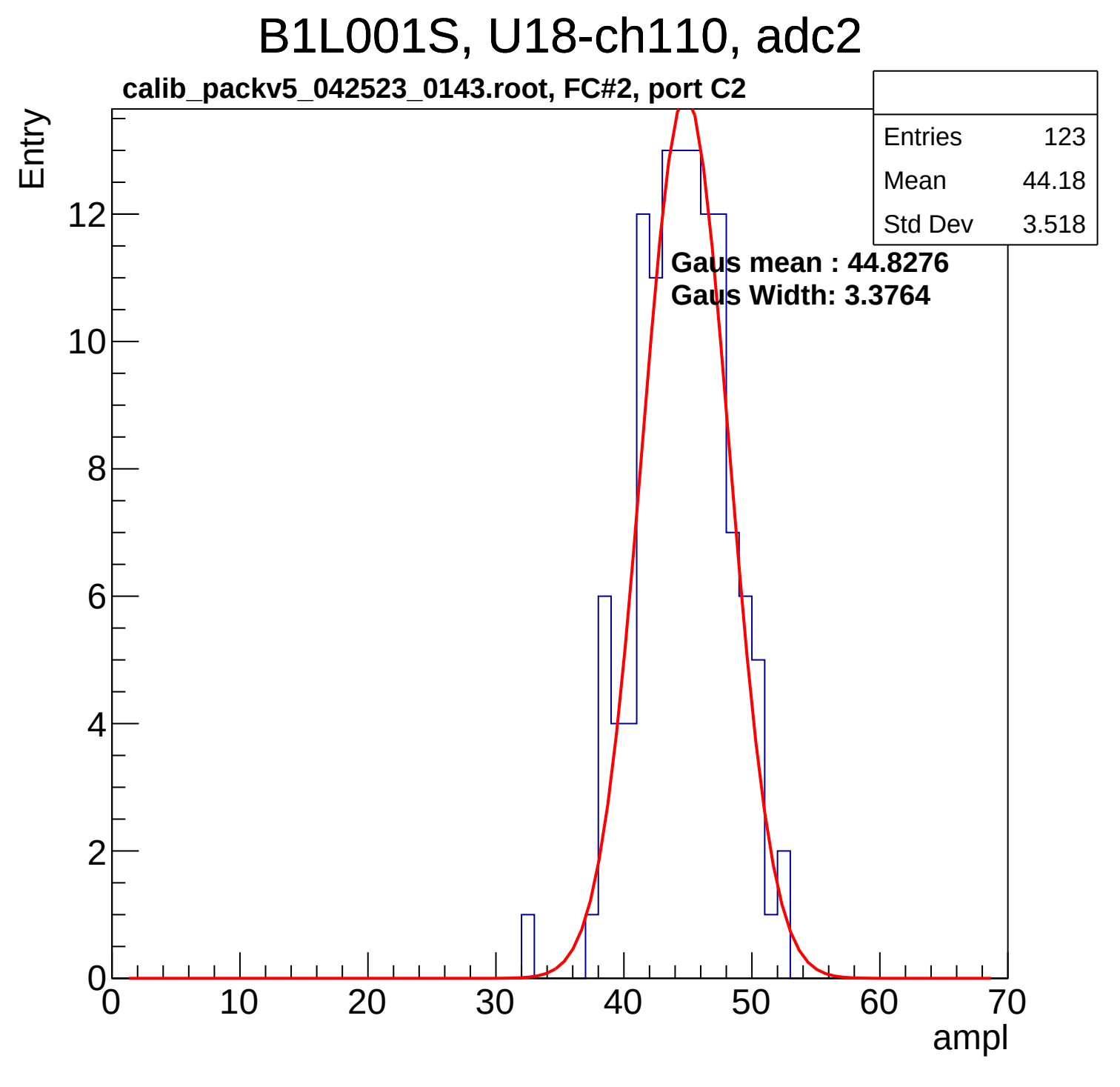

B1L001S, U18-ch109, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 74
Mean 59.49
Std Dev 7.288
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

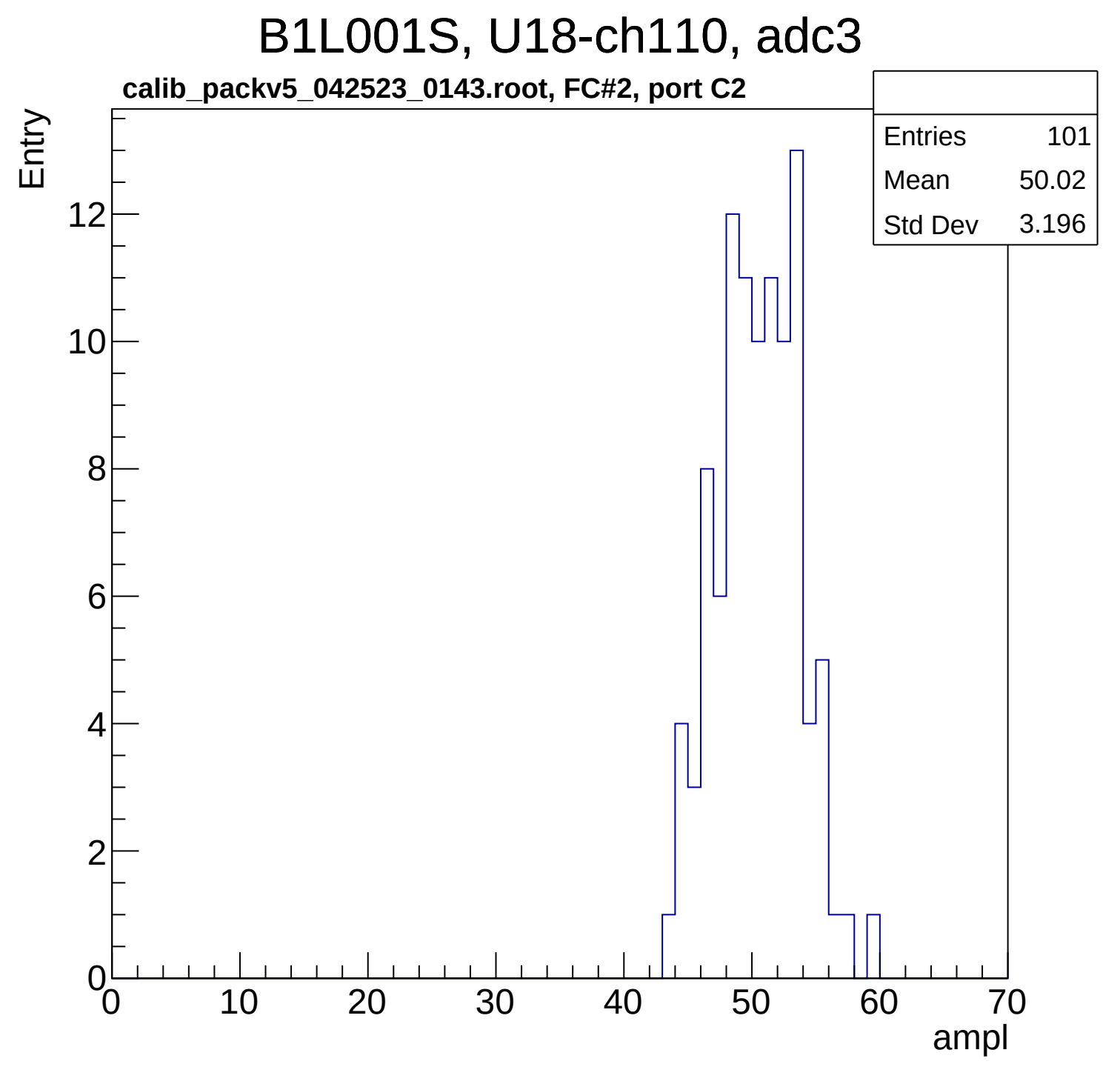

B1L001S, U18-ch109, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 17
Mean 58.41
Std Dev 14.63
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

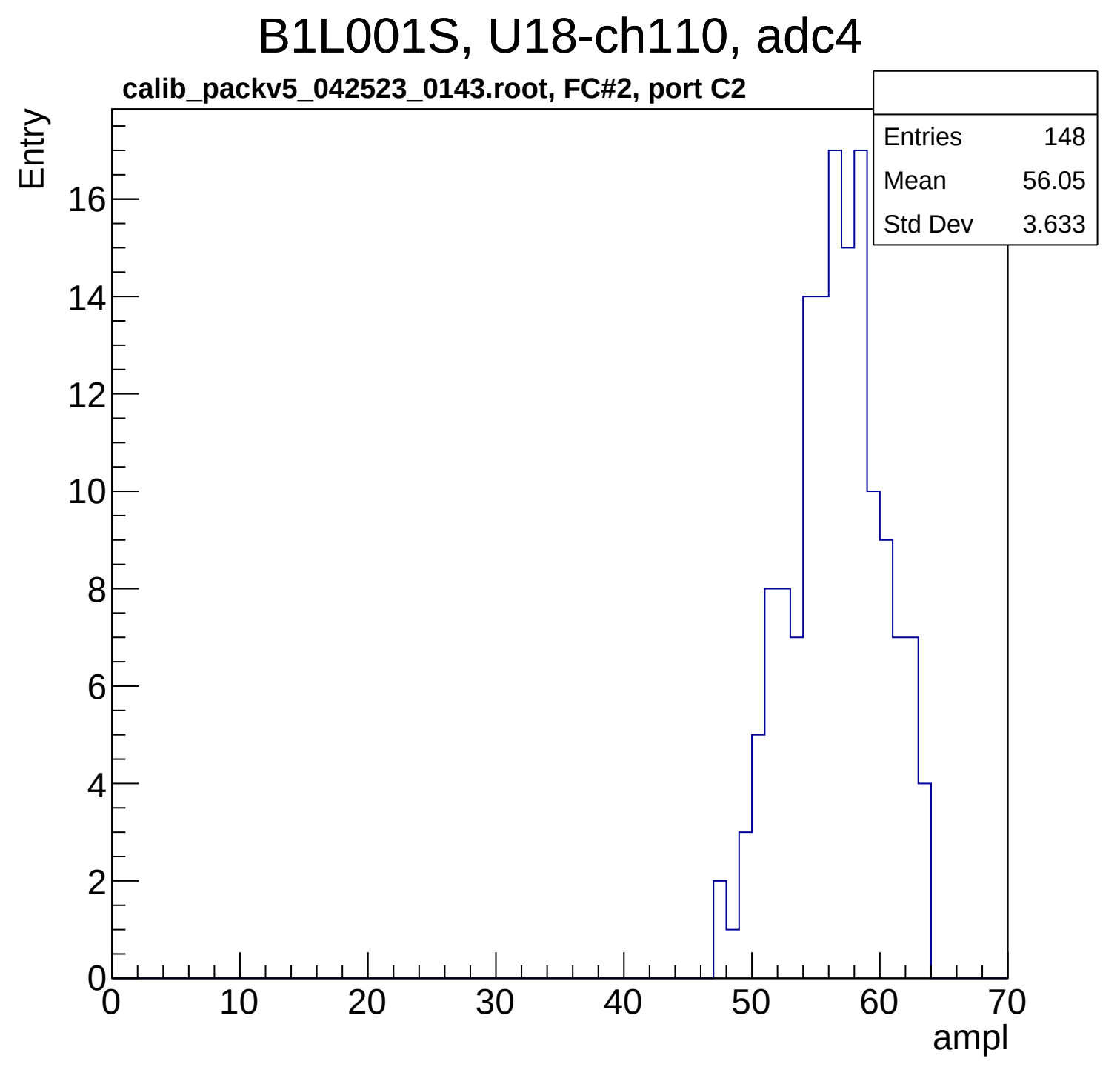

B1L001S, U18-ch109, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

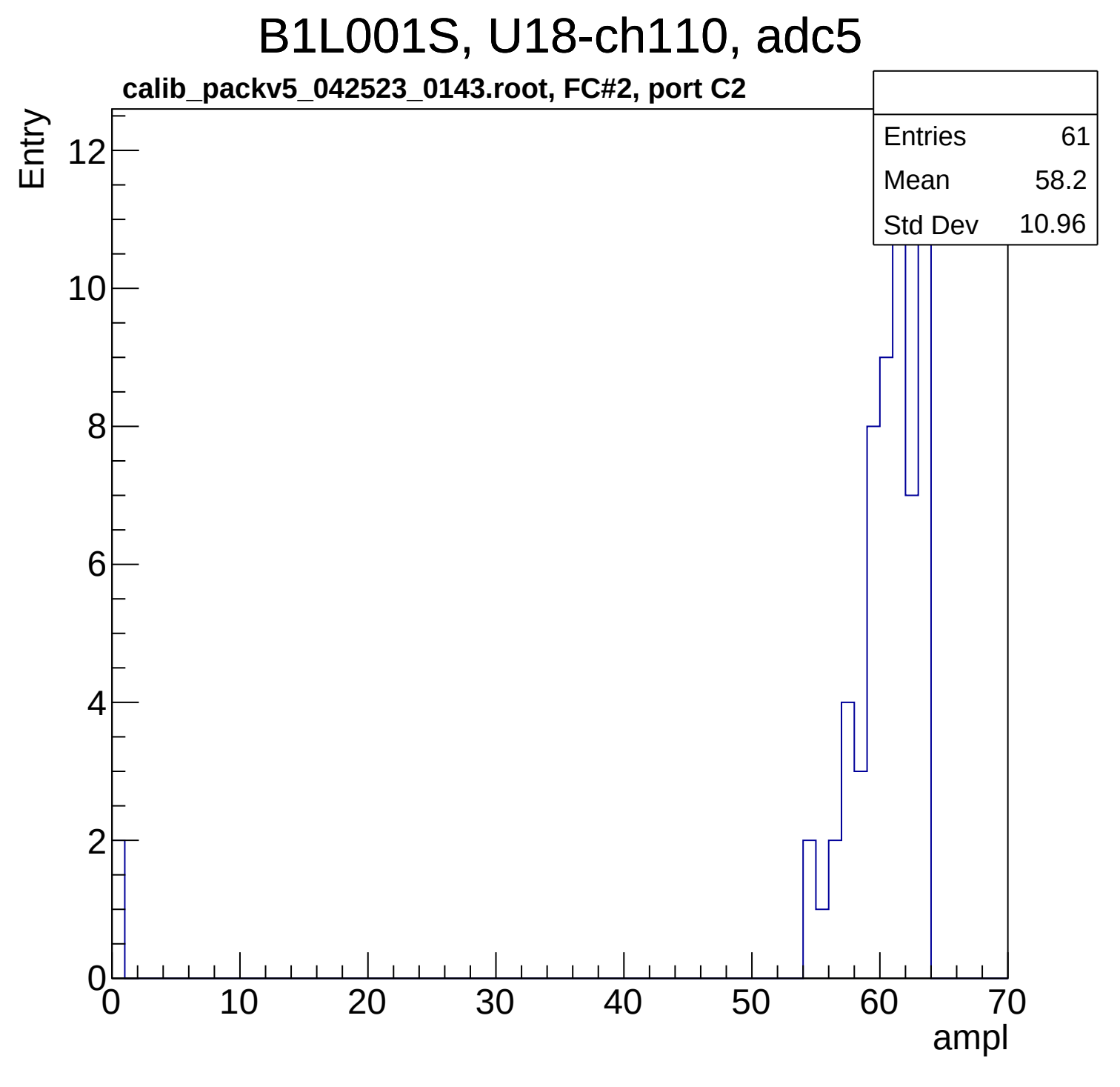

B1L001S, U18-ch110, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 159
Mean 30.22
Std Dev 4.491
Gaus mean : 31.0467
Gaus Width: 3.9946
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

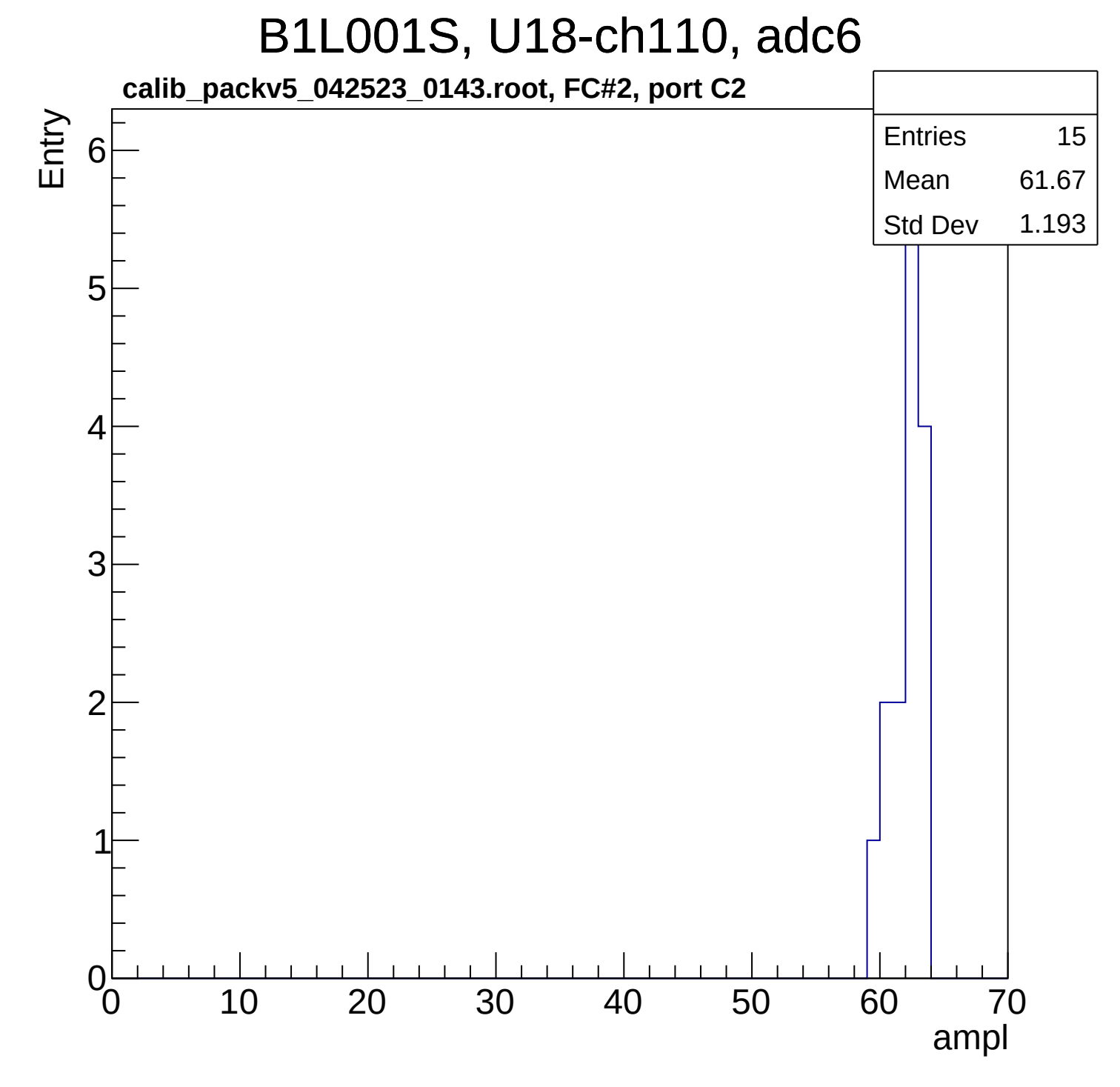

B1L001S, U18-ch110, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 135
Mean 37.85
Std Dev 3.461
Gaus mean : 38.4156
Gaus Width: 3.7818
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

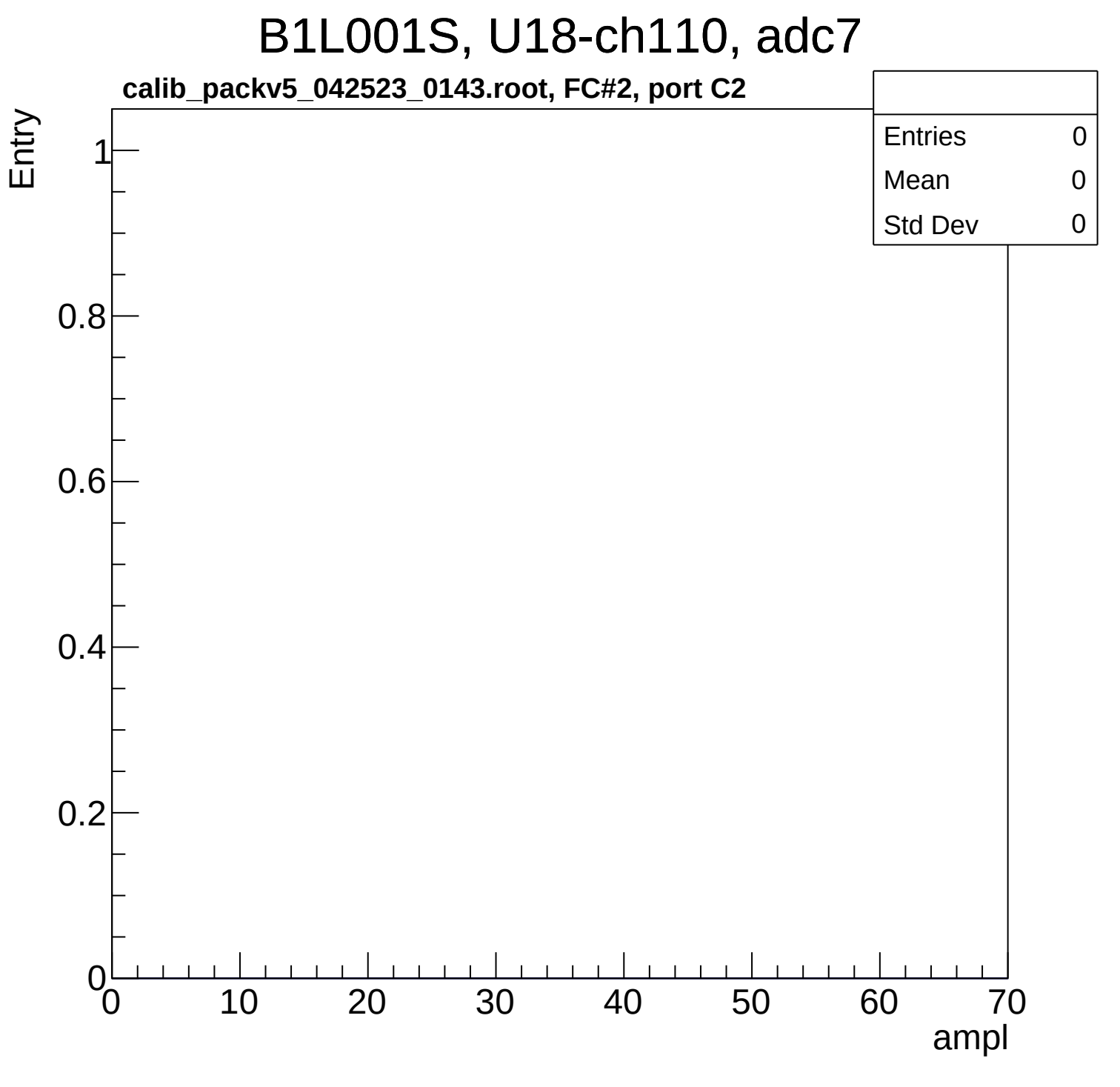

B1L001S, U18-ch110, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 123
Mean 44.18
Std Dev 3.518
Gaus mean : 44.8276
Gaus Width: 3.3764
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70

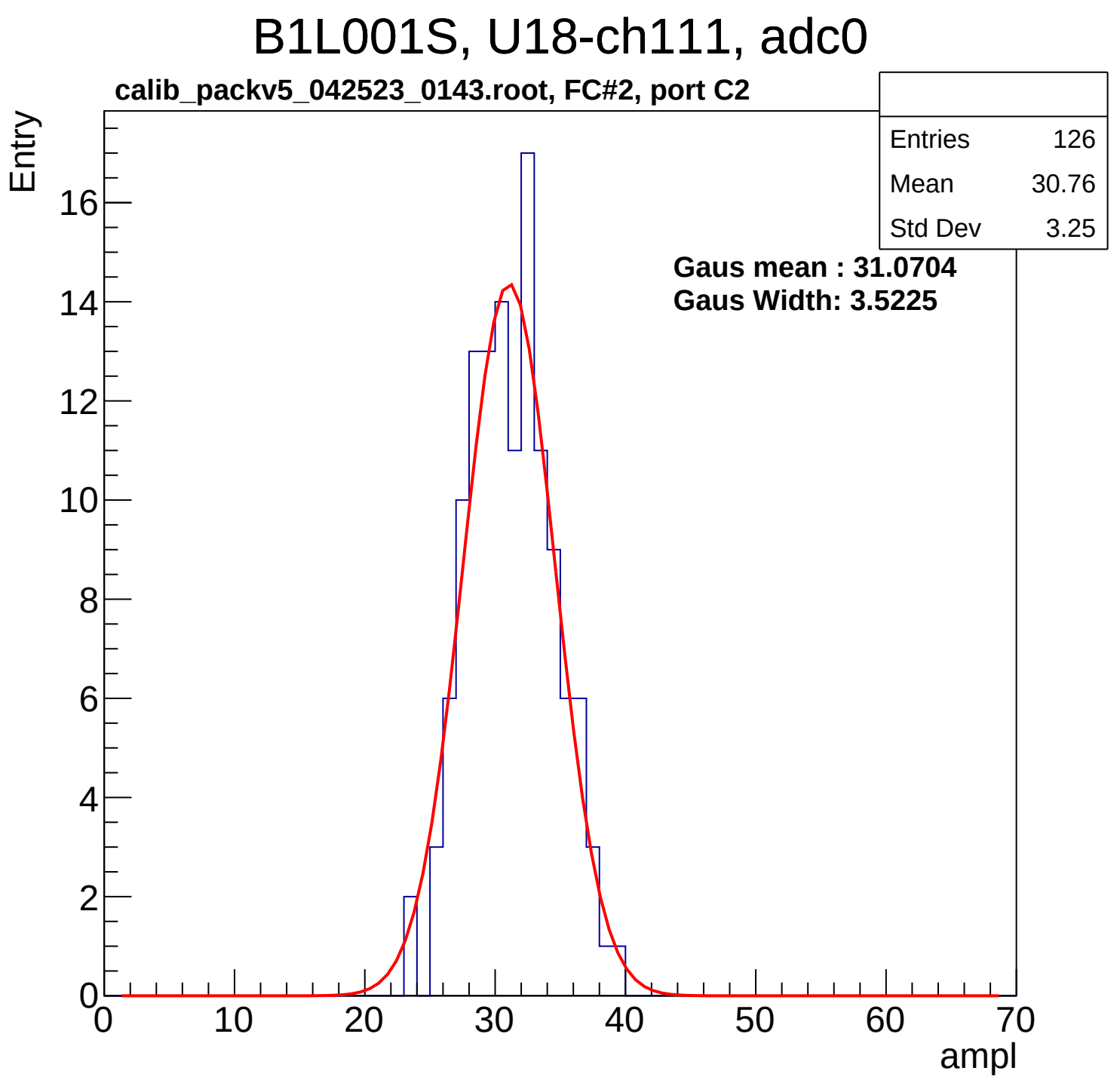

B1L001S, U18-ch110, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 101
Mean 50.02
Std Dev 3.196
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70

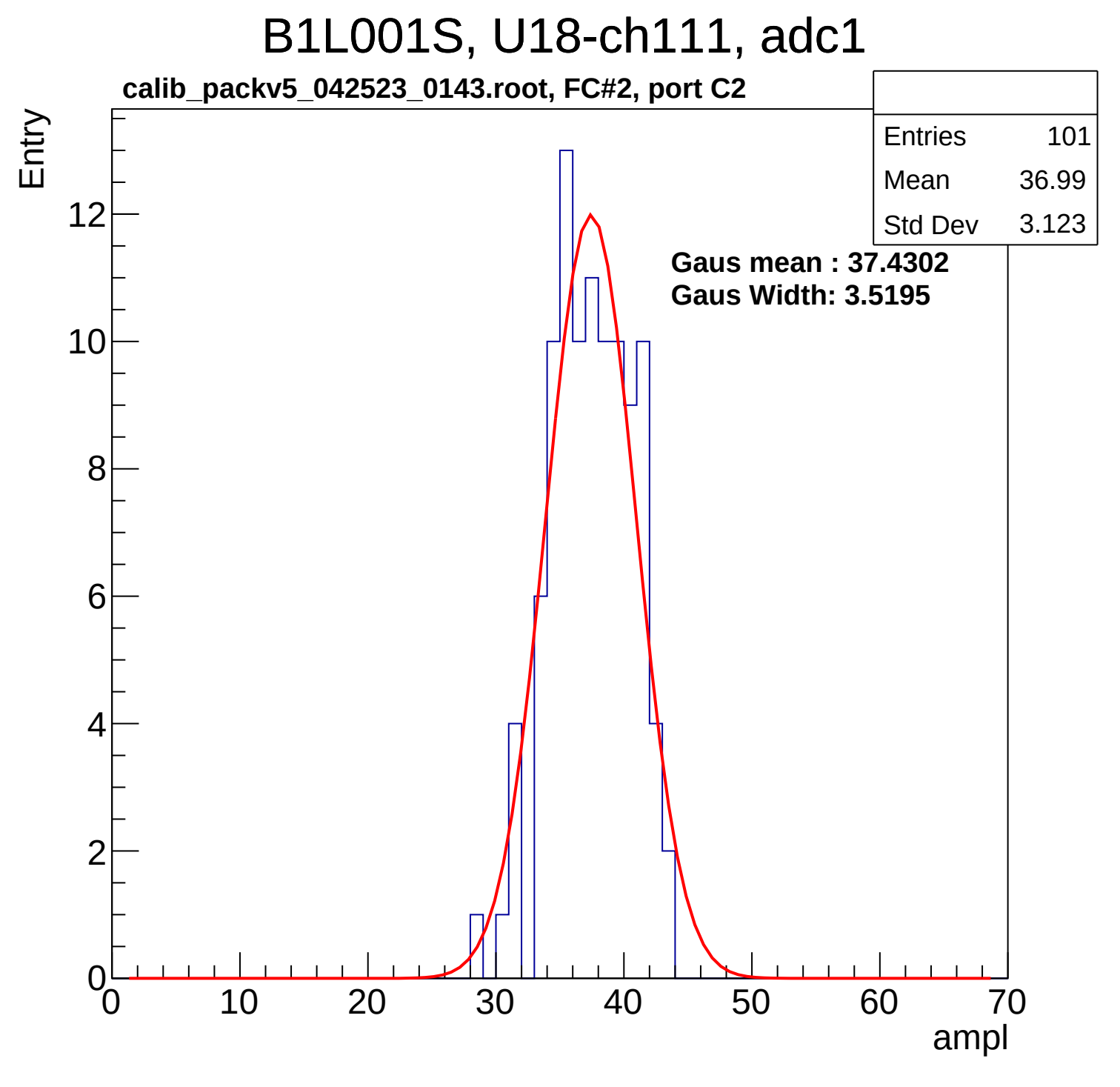

B1L001S, U18-ch110, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 148
Mean 56.05
Std Dev 3.633
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

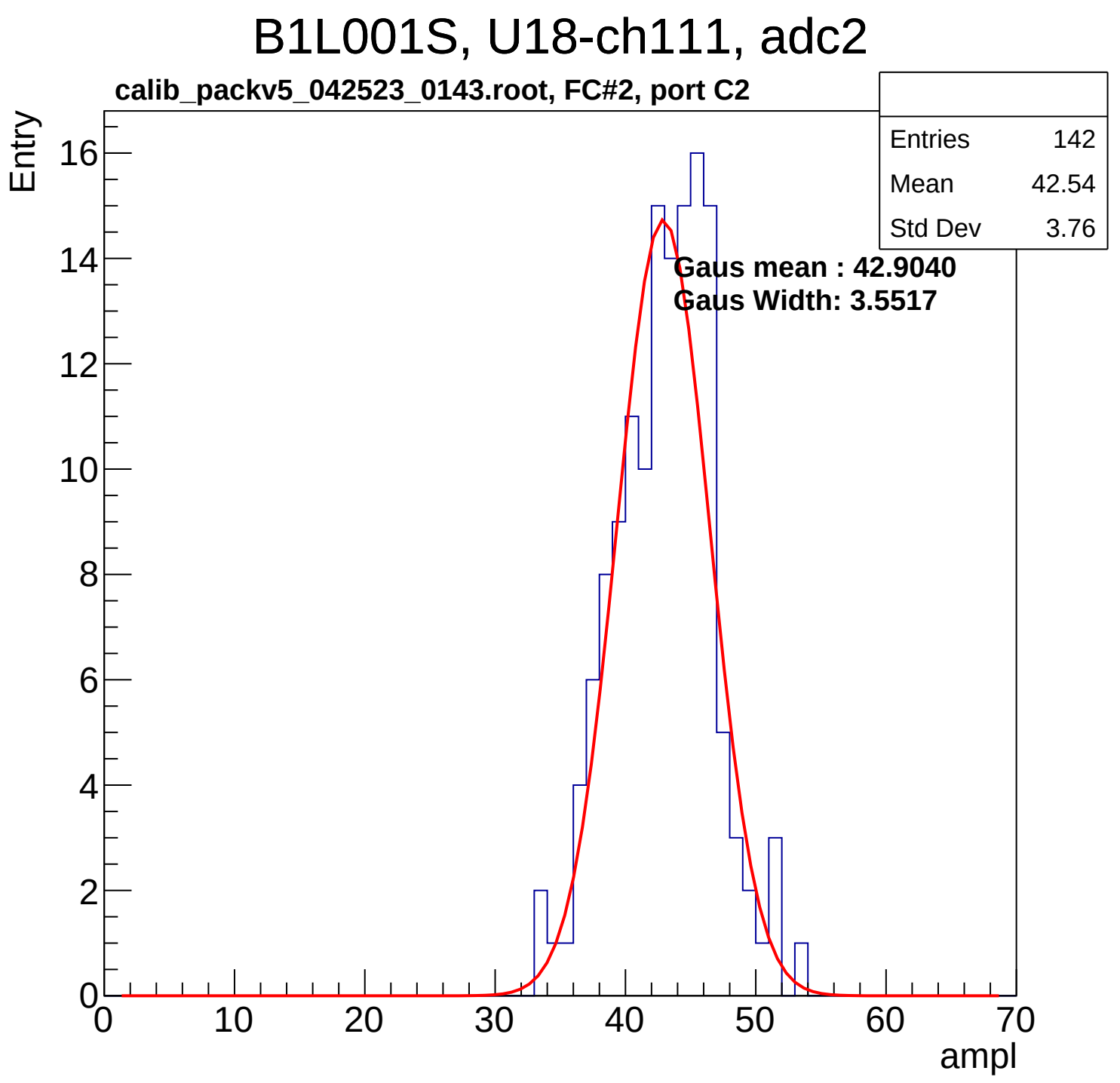

B1L001S, U18-ch110, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 61
Mean 58.2
Std Dev 10.96
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl

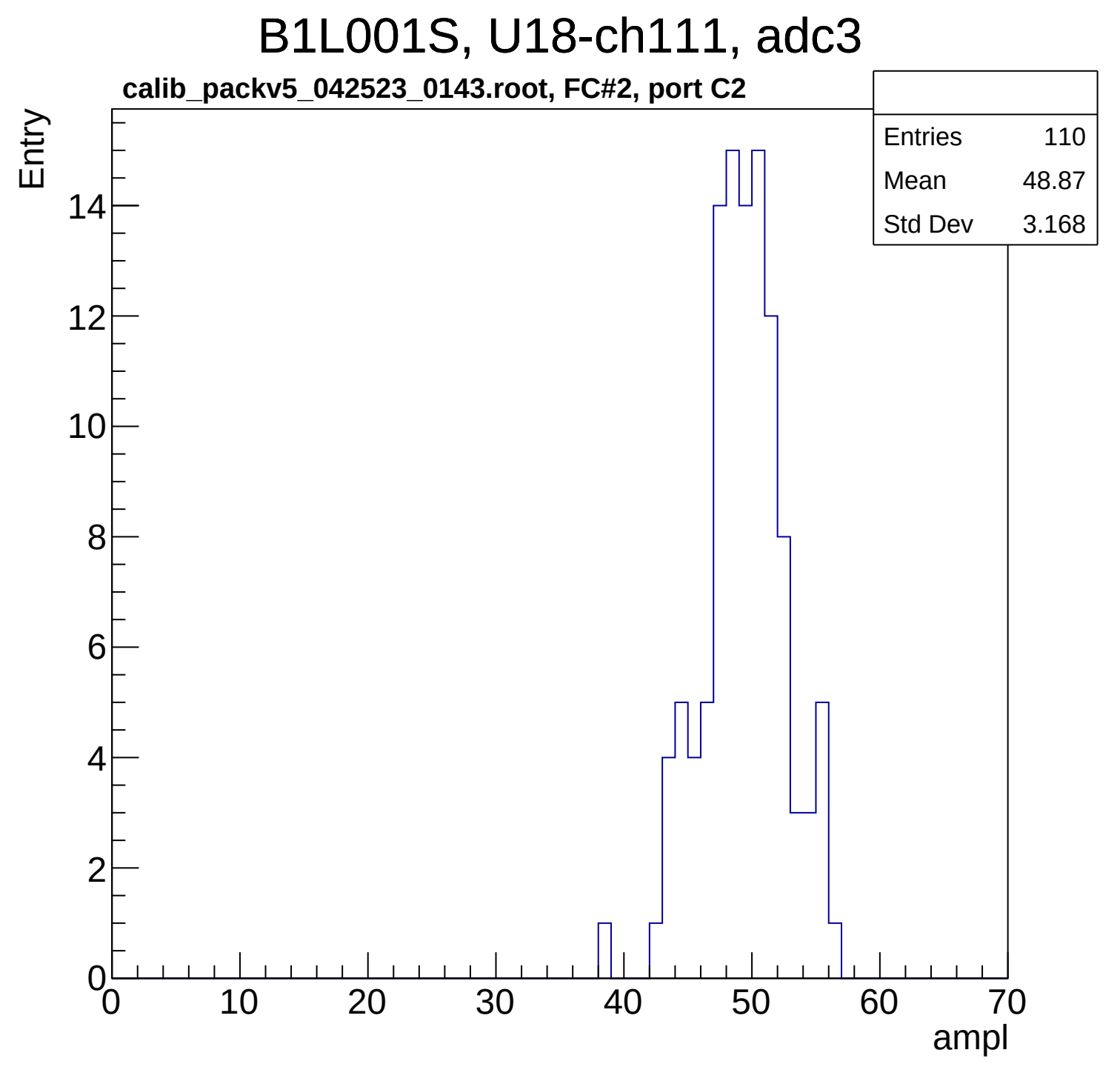

B1L001S, U18-ch110, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 15
Mean 61.67
Std Dev 1.193
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl

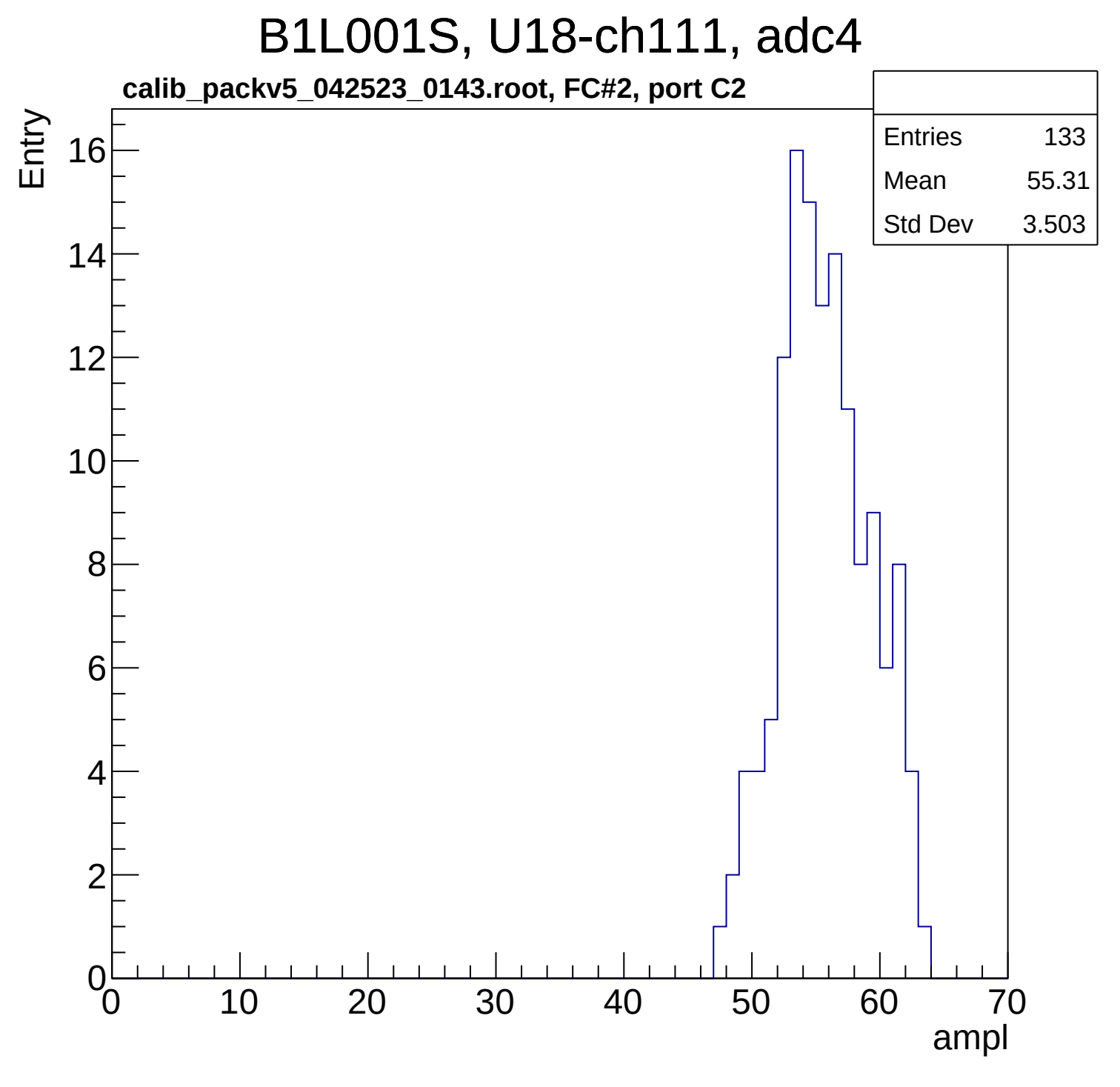

B1L001S, U18-ch110, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

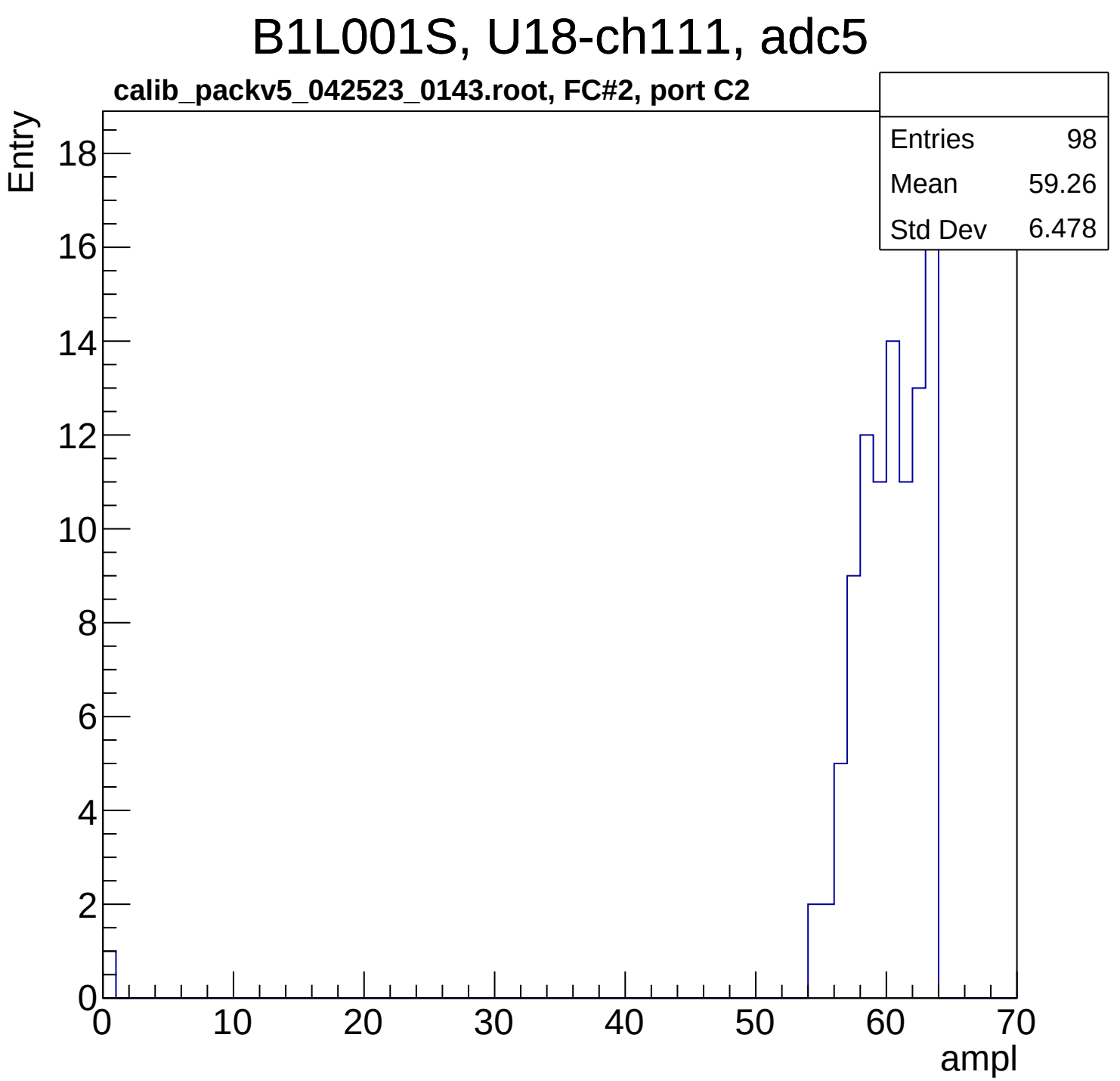

B1L001S, U18-ch111, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 126
Mean 30.76
Std Dev 3.25
Gaus mean : 31.0704
Gaus Width: 3.5225
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

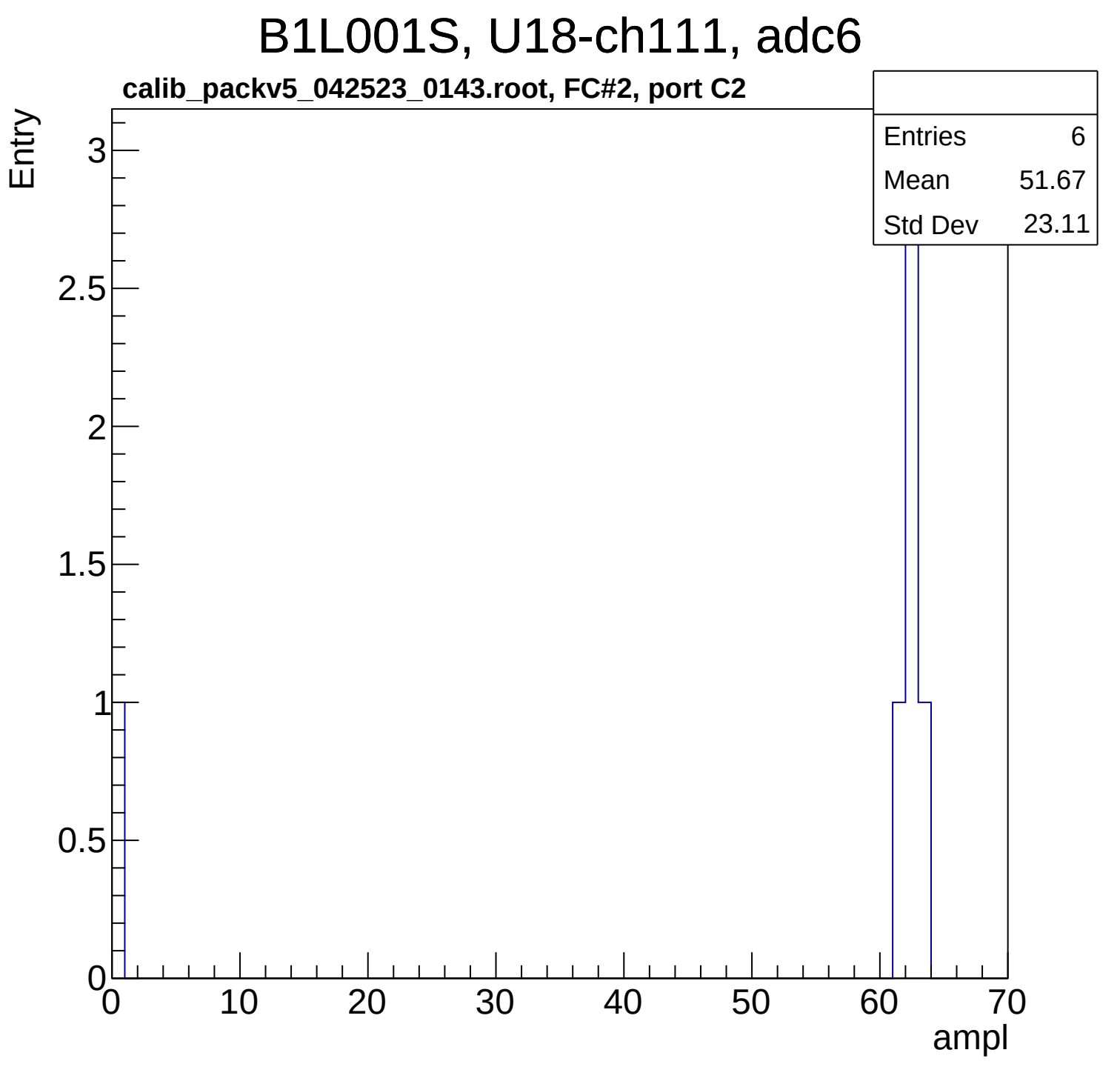

B1L001S, U18-ch111, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 101
Mean 36.99
Std Dev 3.123
Gaus mean : 37.4302
Gaus Width: 3.5195
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70

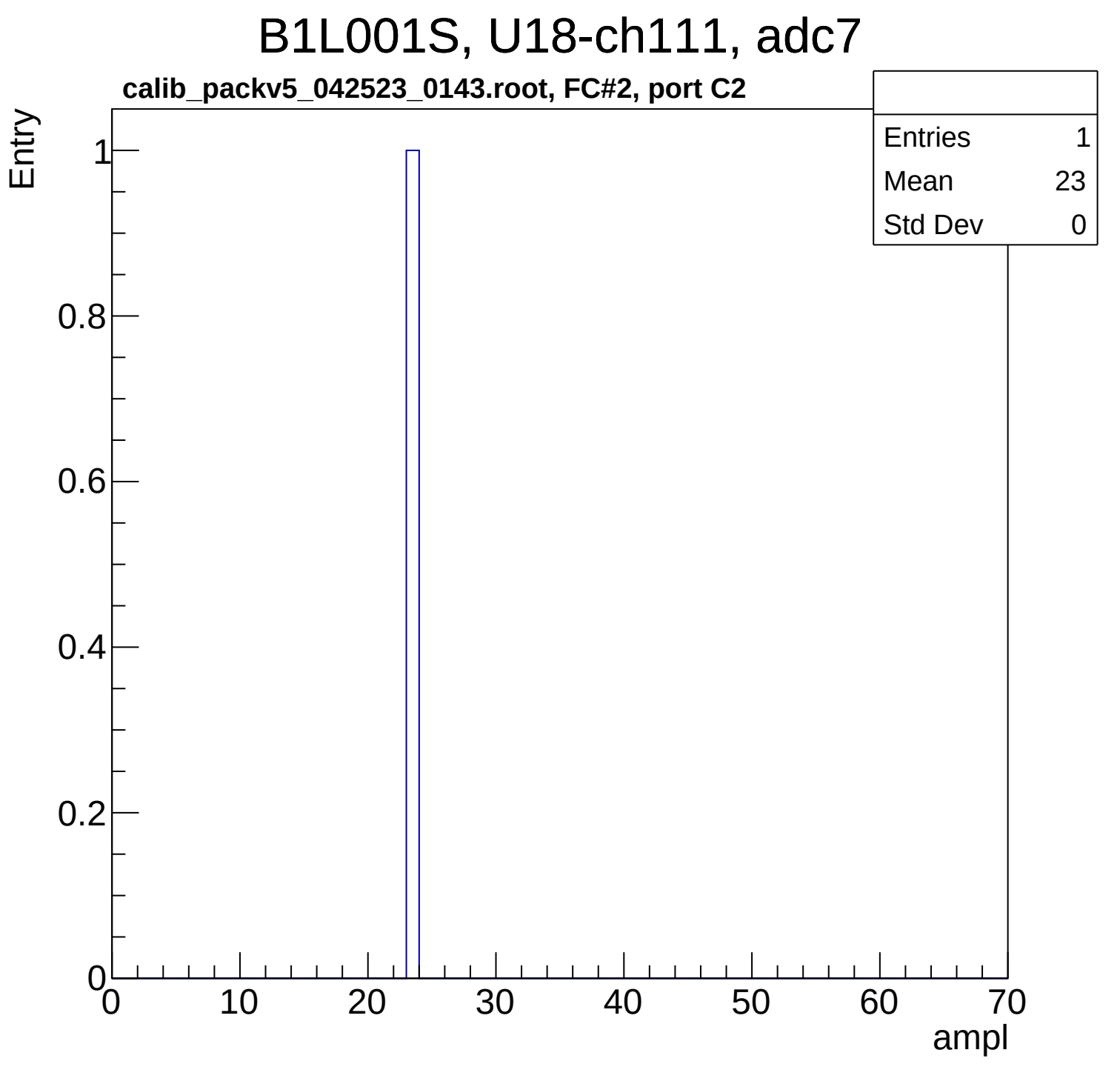

B1L001S, U18-ch111, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 142
Mean 42.54
Std Dev 3.76
Gaus mean : 42.9040
Gaus Width: 3.5517
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

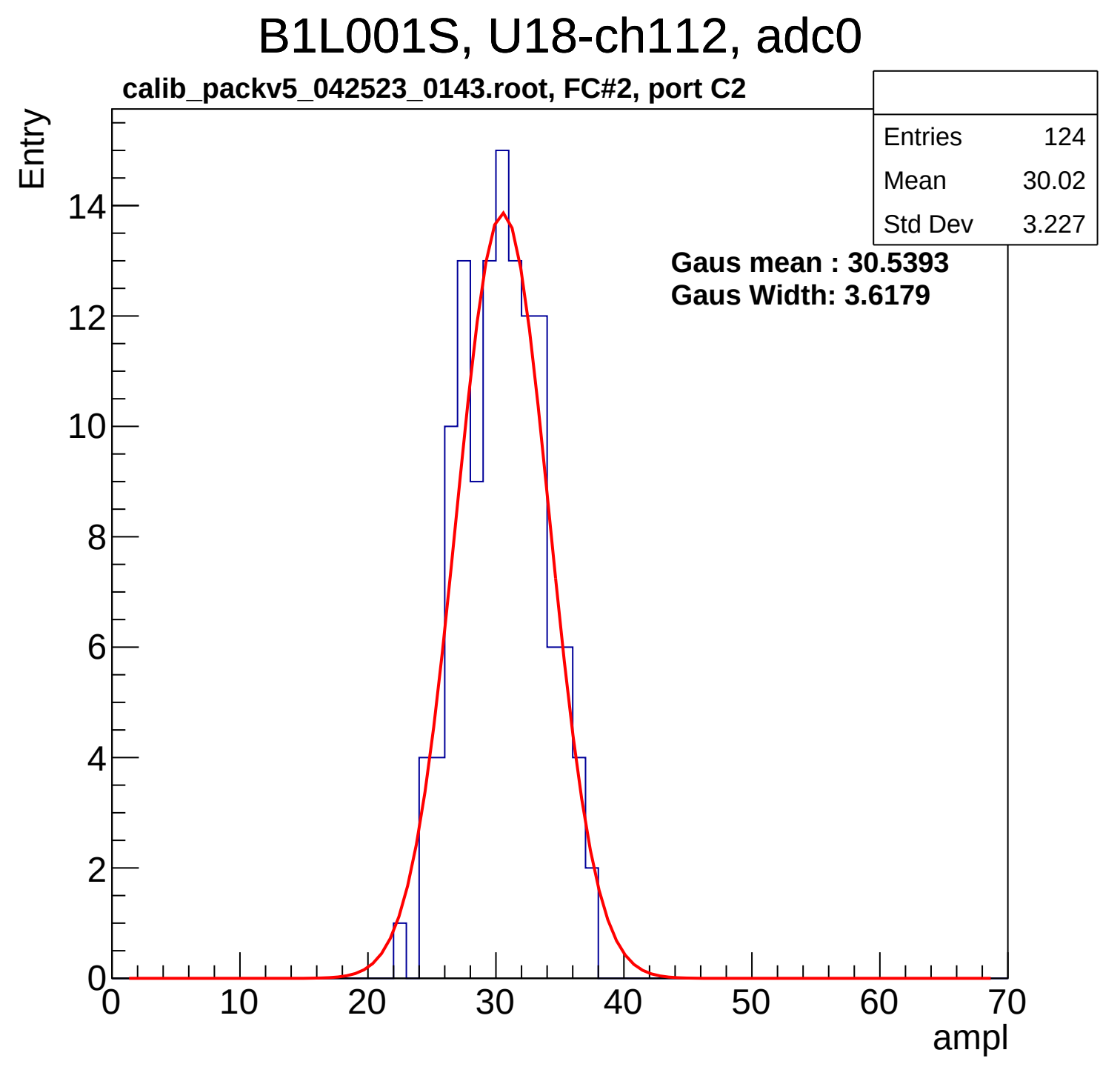

B1L001S, U18-ch111, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 110
Mean 48.87
Std Dev 3.168
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

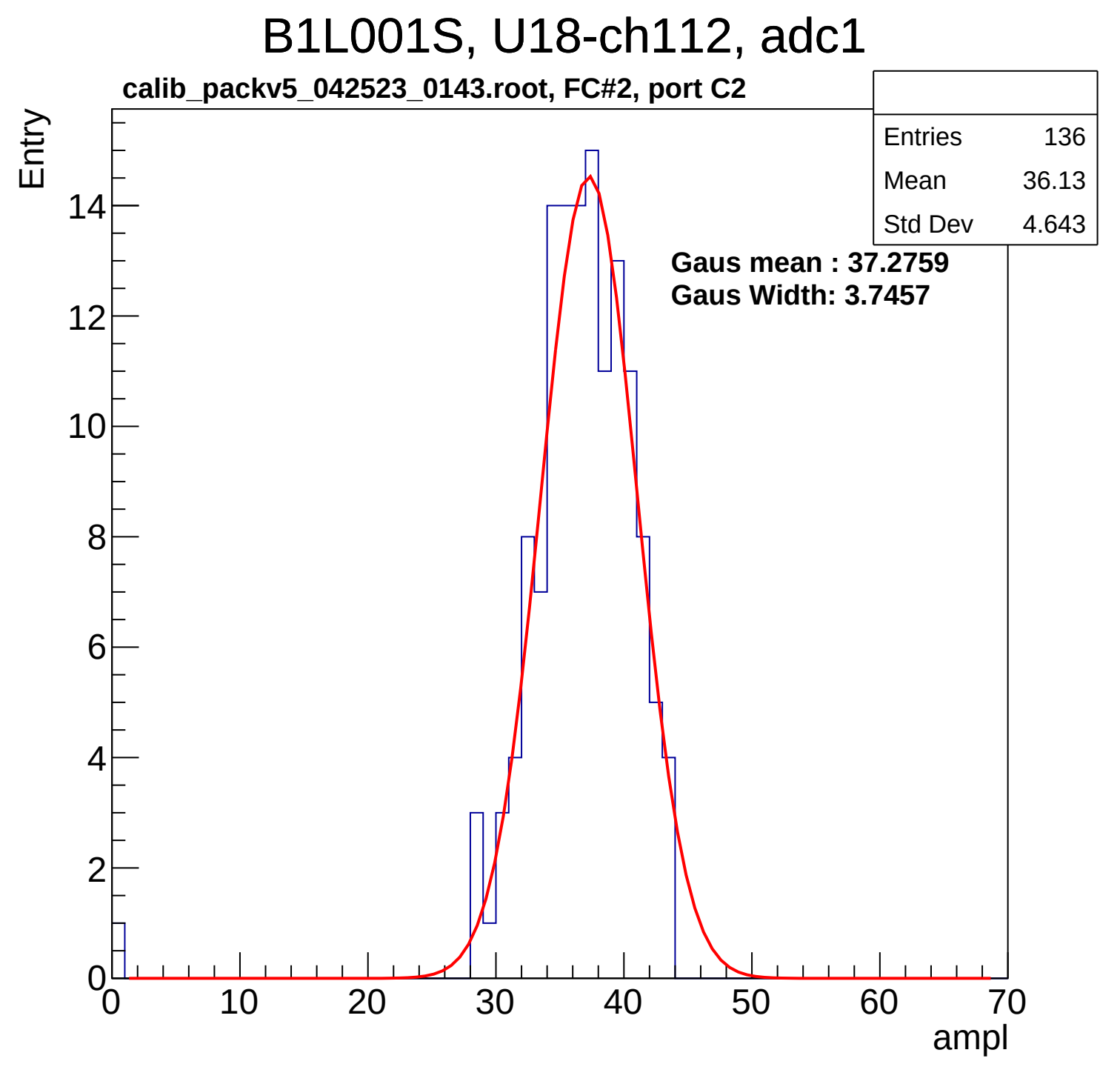

B1L001S, U18-ch111, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 133
Mean 55.31
Std Dev 3.503
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

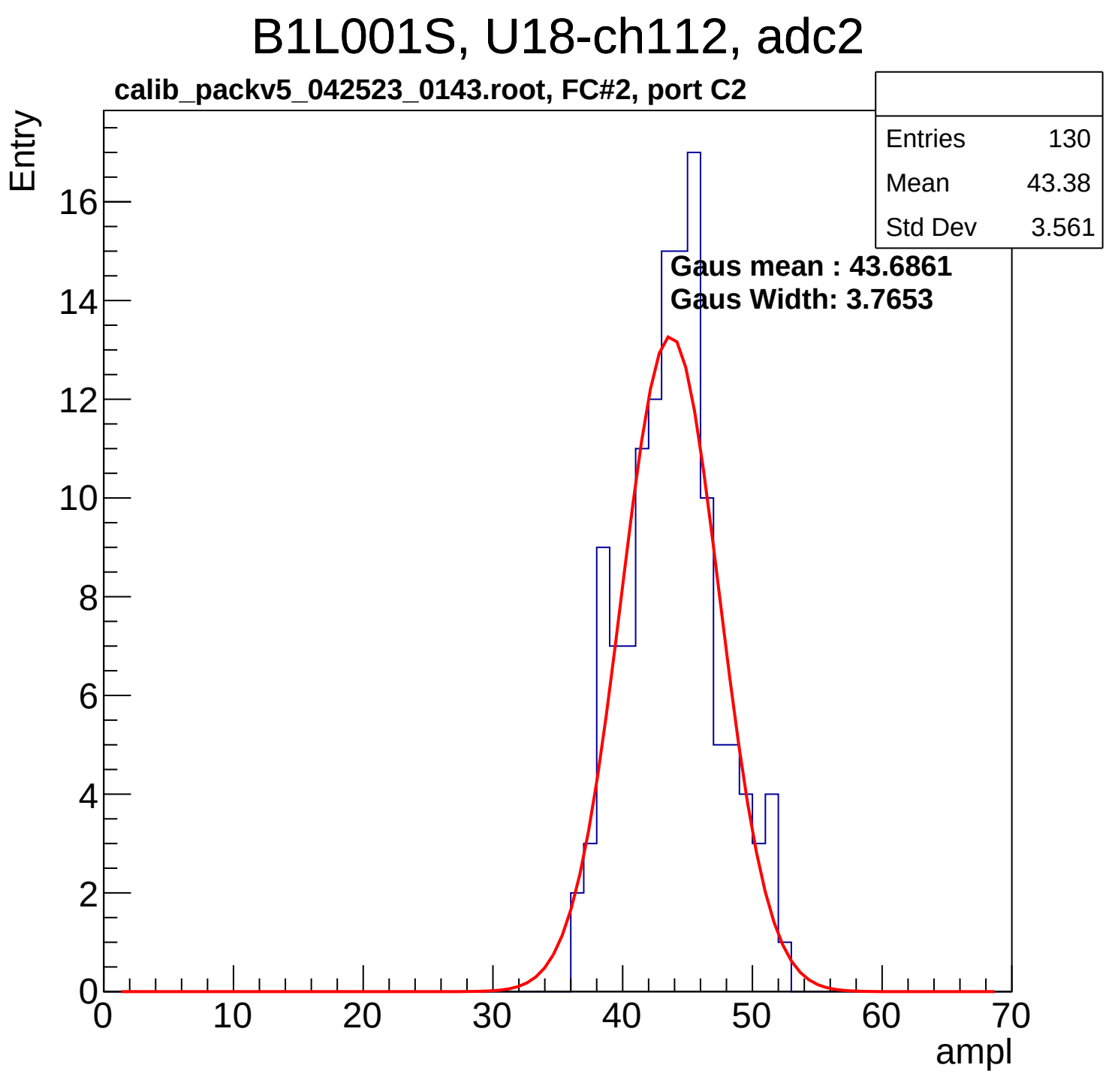

B1L001S, U18-ch111, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 98
Mean 59.26
Std Dev 6.478
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

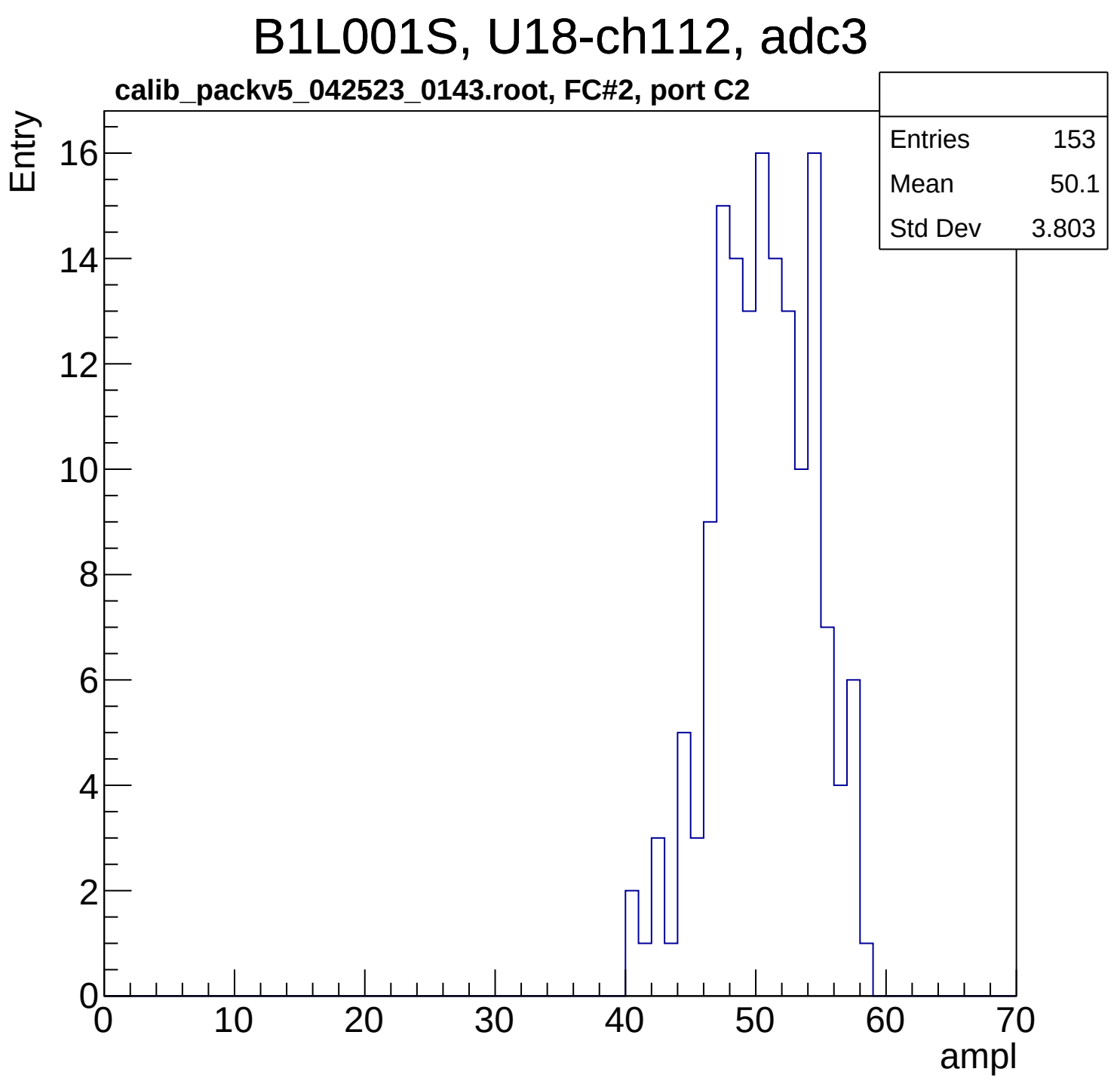

B1L001S, U18-ch111, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 6
Mean 51.67
Std Dev 23.11
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

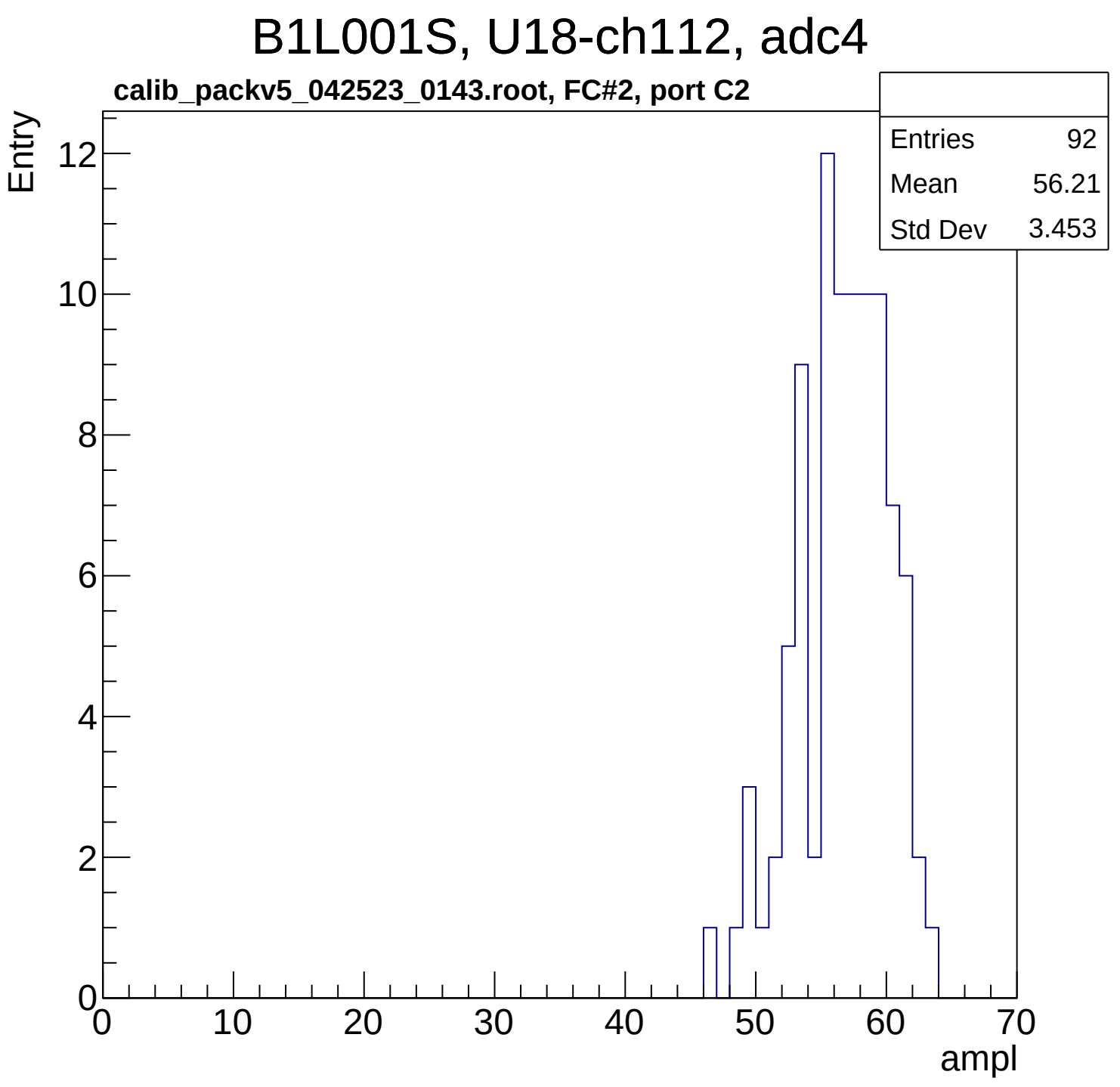

B1L001S, U18-ch111, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 23
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

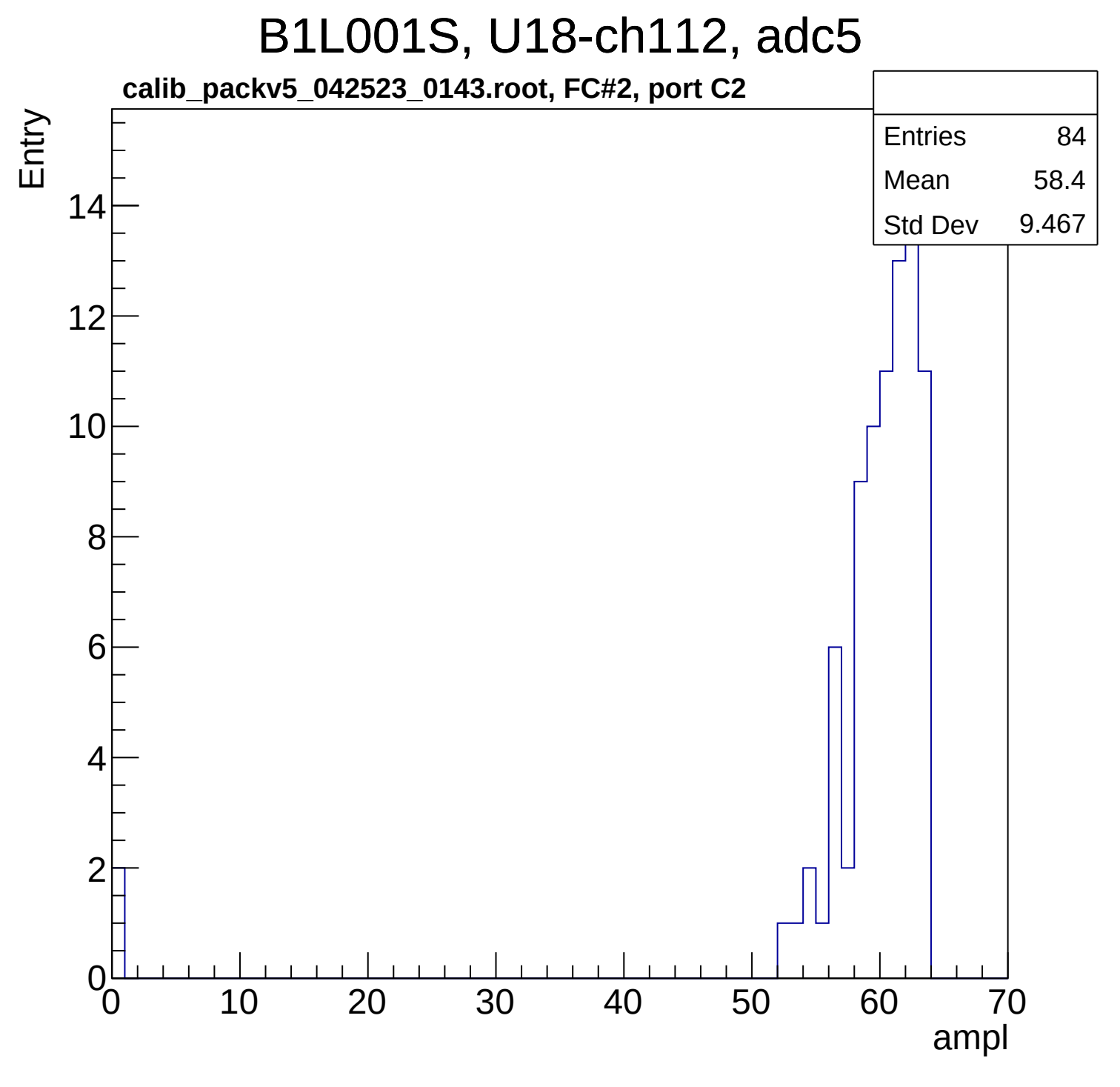

B1L001S, U18-ch112, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 124
Mean 30.02
Std Dev 3.227
Gaus mean : 30.5393
Gaus Width: 3.6179
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

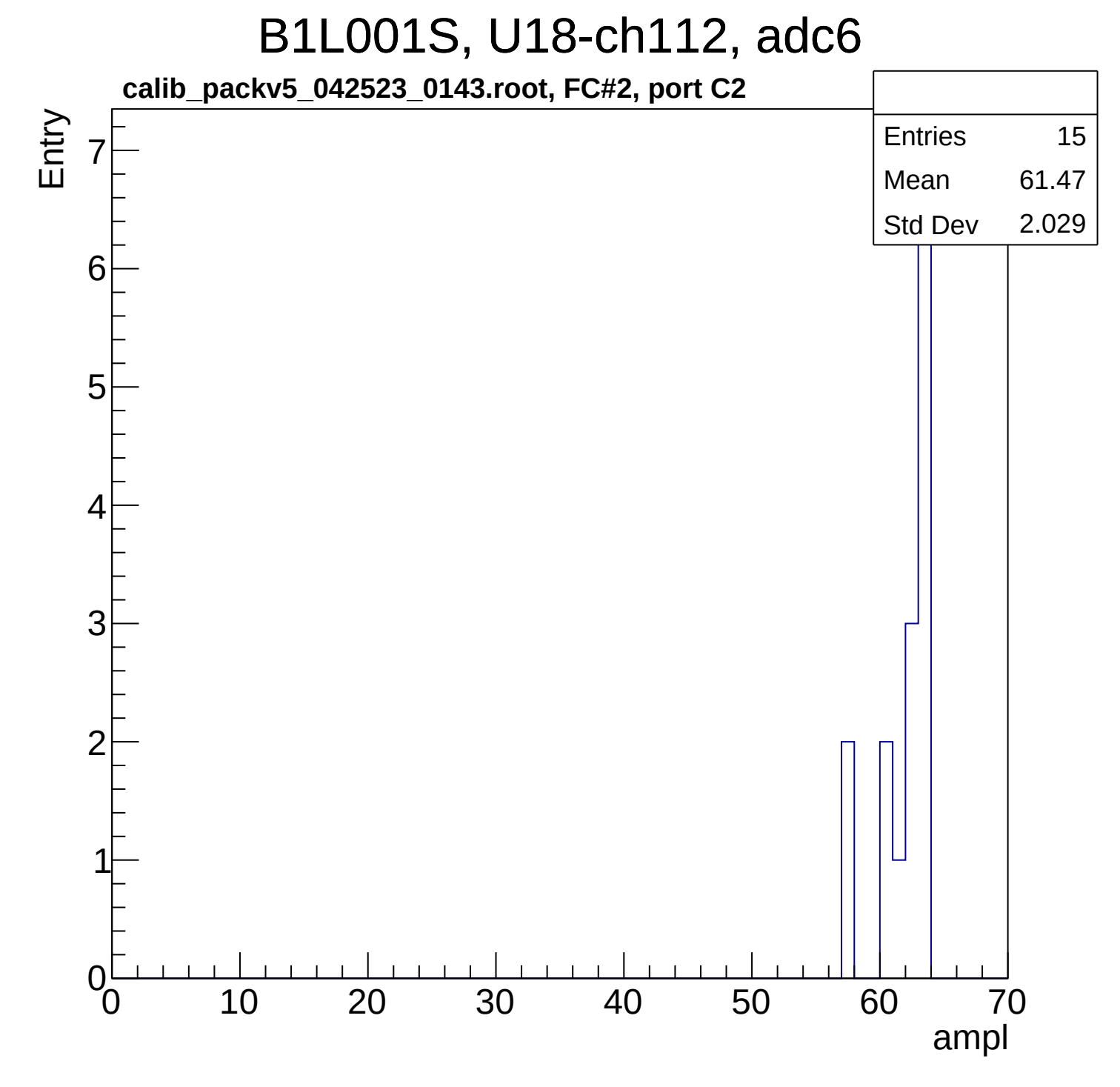

B1L001S, U18-ch112, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 136
Mean 36.13
Std Dev 4.643
Gaus mean : 37.2759
Gaus Width: 3.7457
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

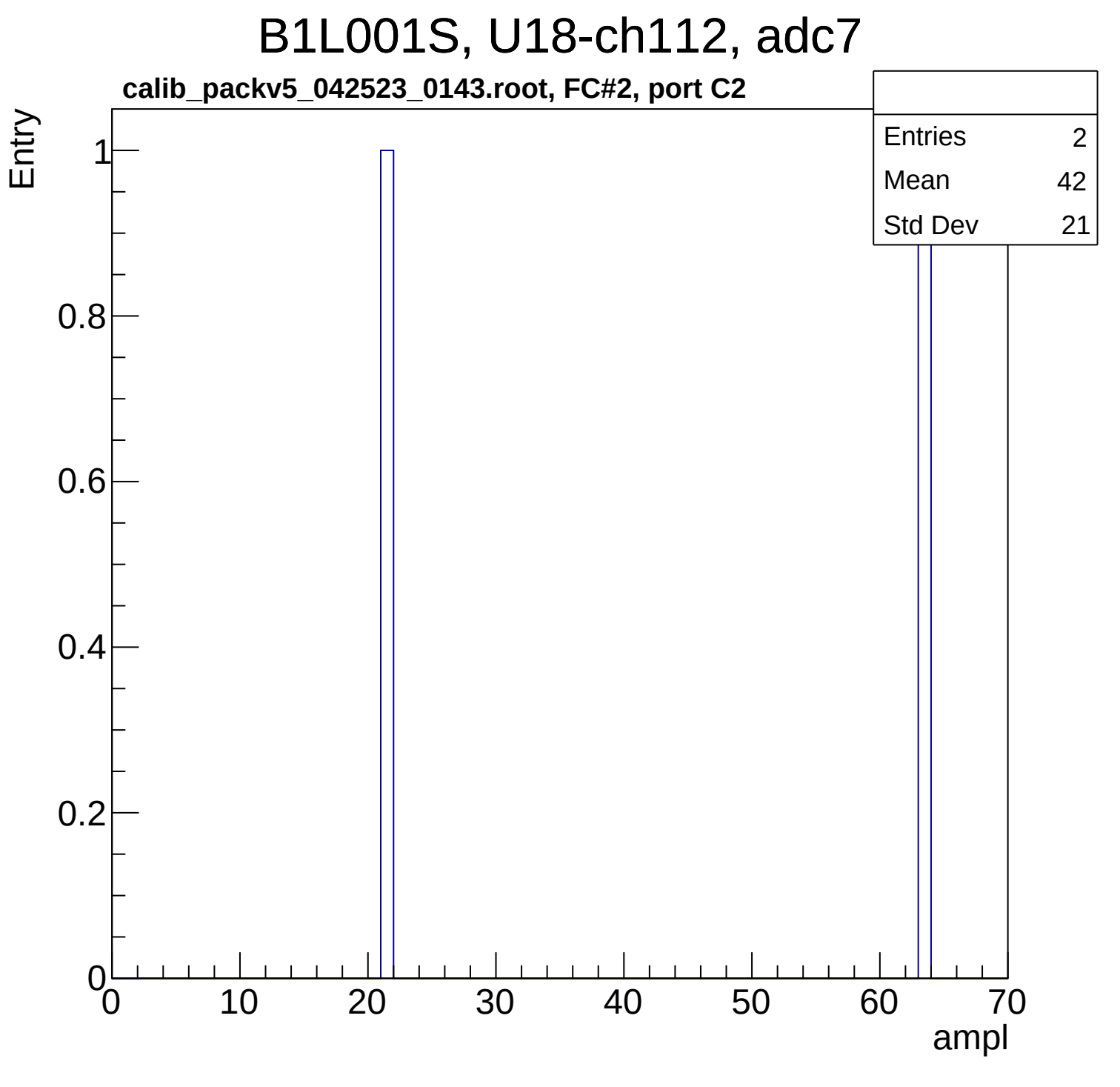

B1L001S, U18-ch112, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 130
Mean 43.38
Std Dev 3.561
Gaus mean : 43.6861
Gaus Width: 3.7653
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

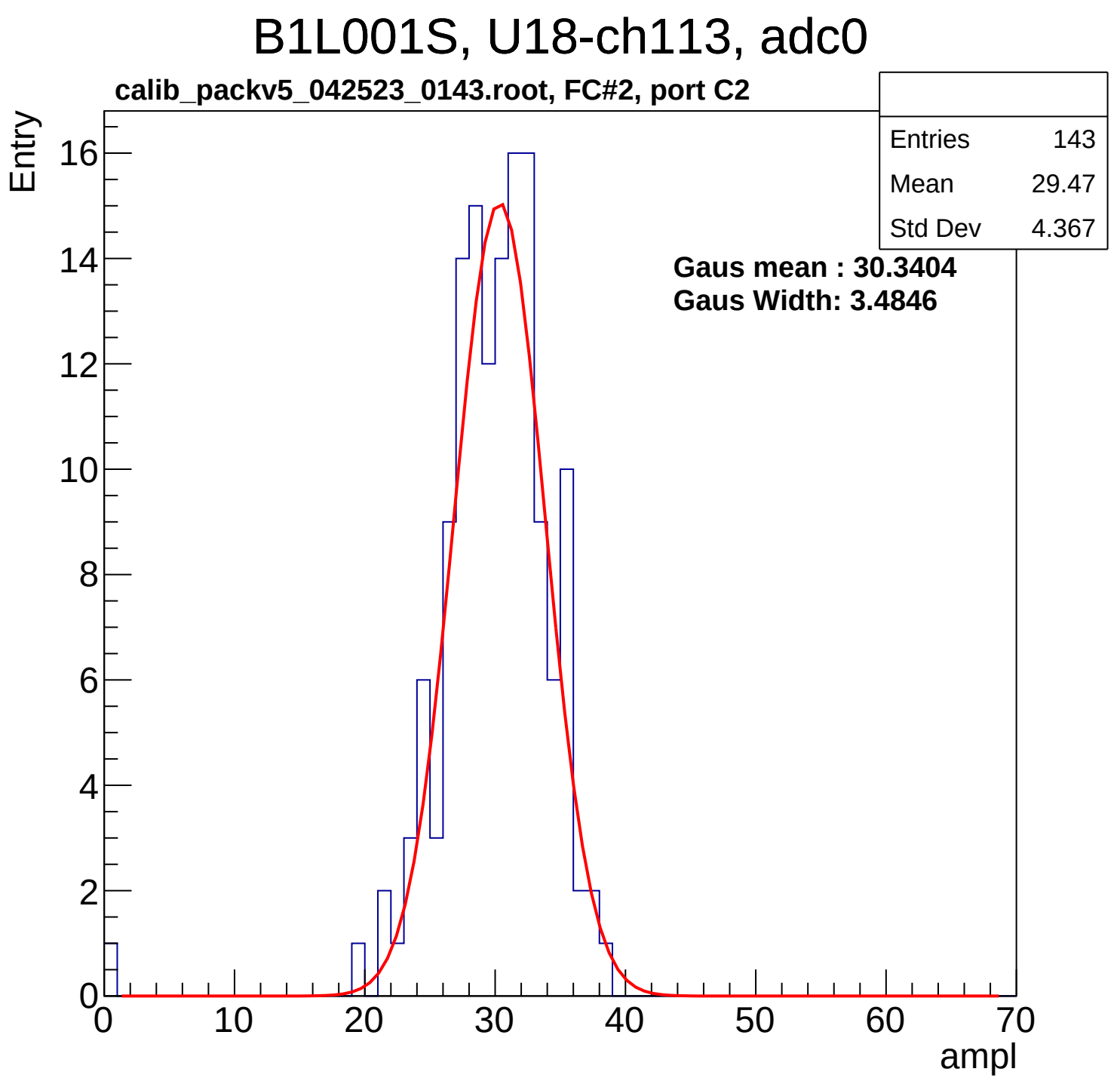

B1L001S, U18-ch112, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 153
Mean 50.1
Std Dev 3.803
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

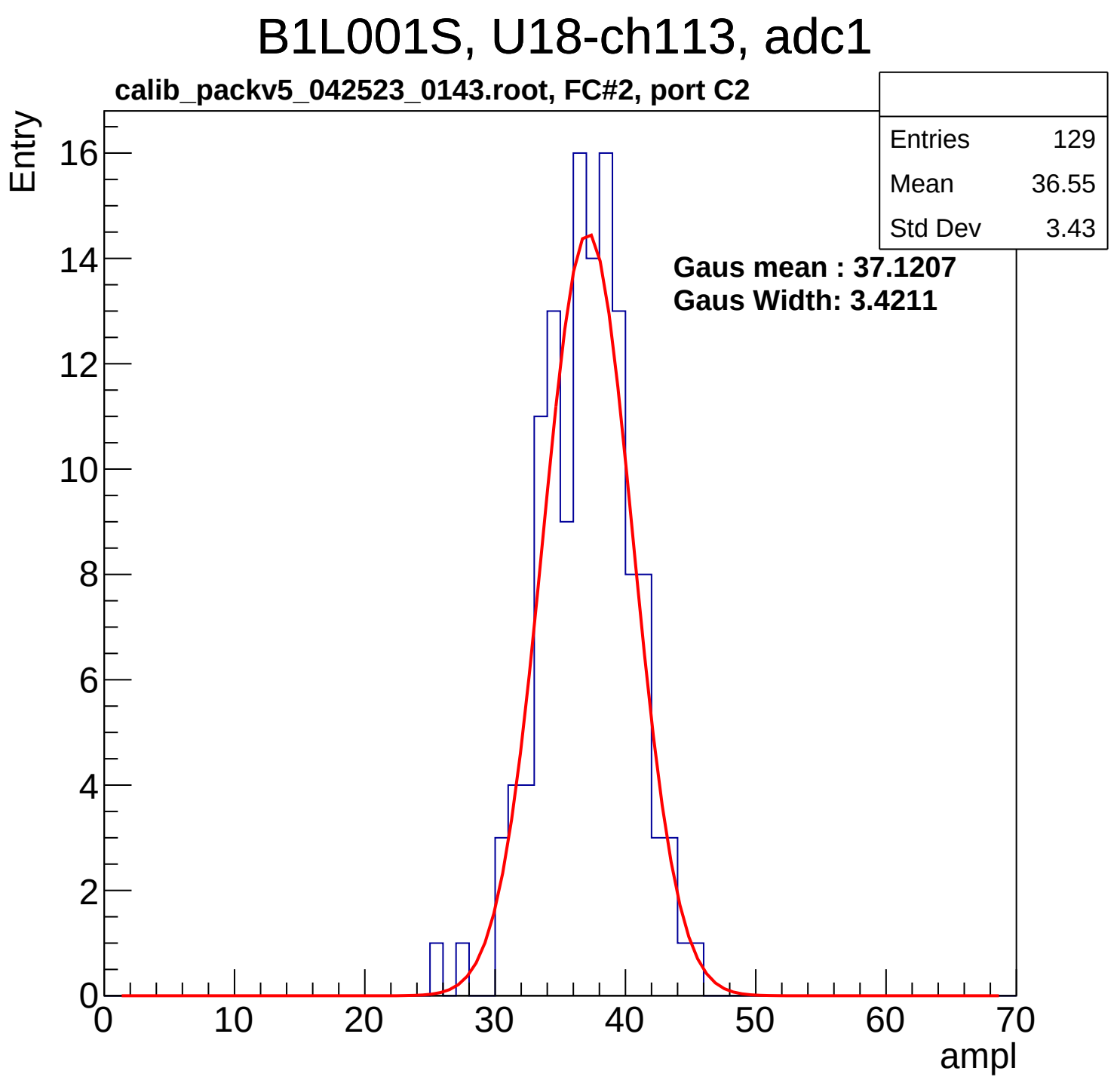

B1L001S, U18-ch112, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 92
Mean 56.21
Std Dev 3.453
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl

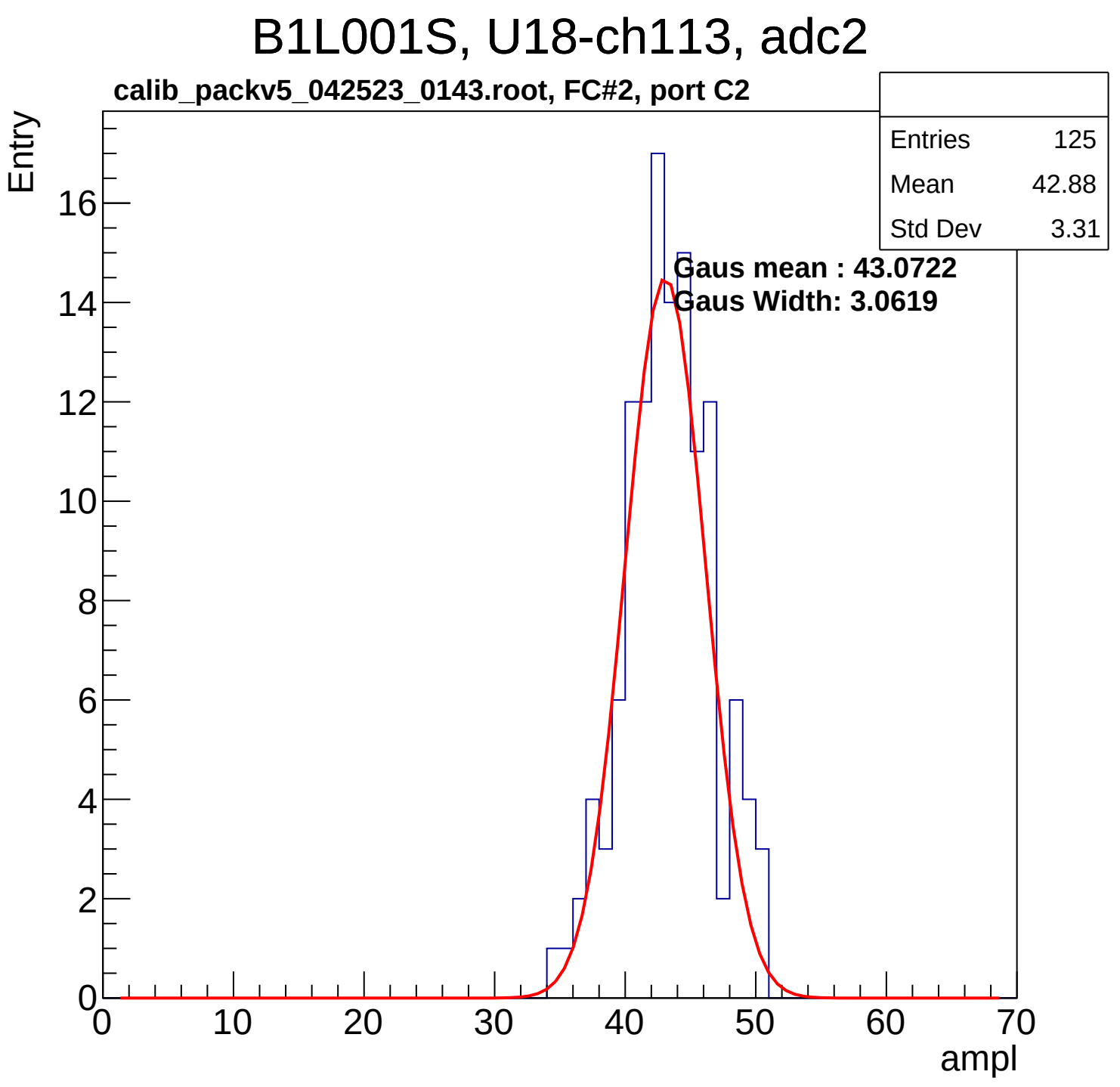

B1L001S, U18-ch112, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 84
Mean 58.4
Std Dev 9.467
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl

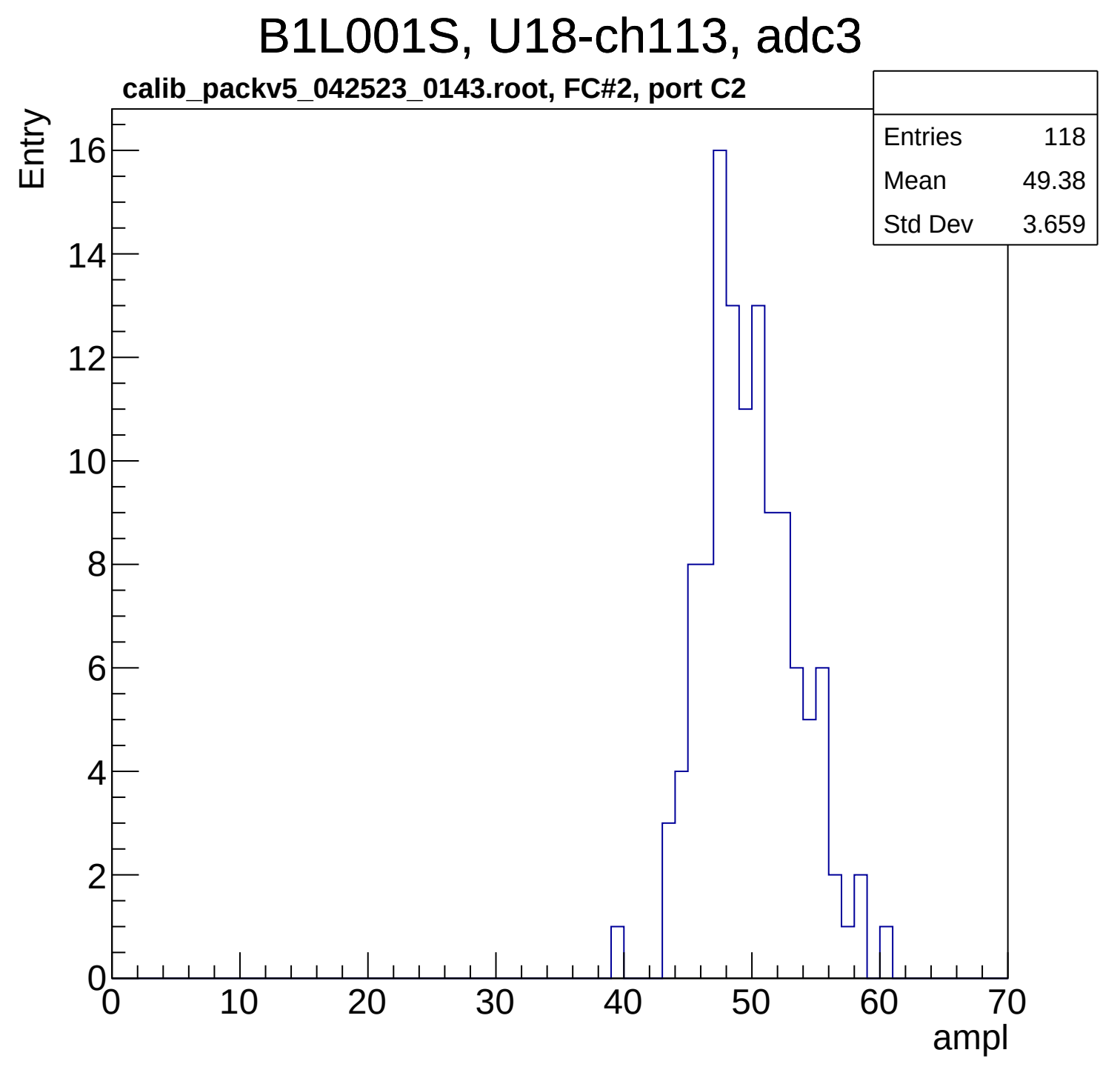

B1L001S, U18-ch112, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 15
Mean 61.47
Std Dev 2.029
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

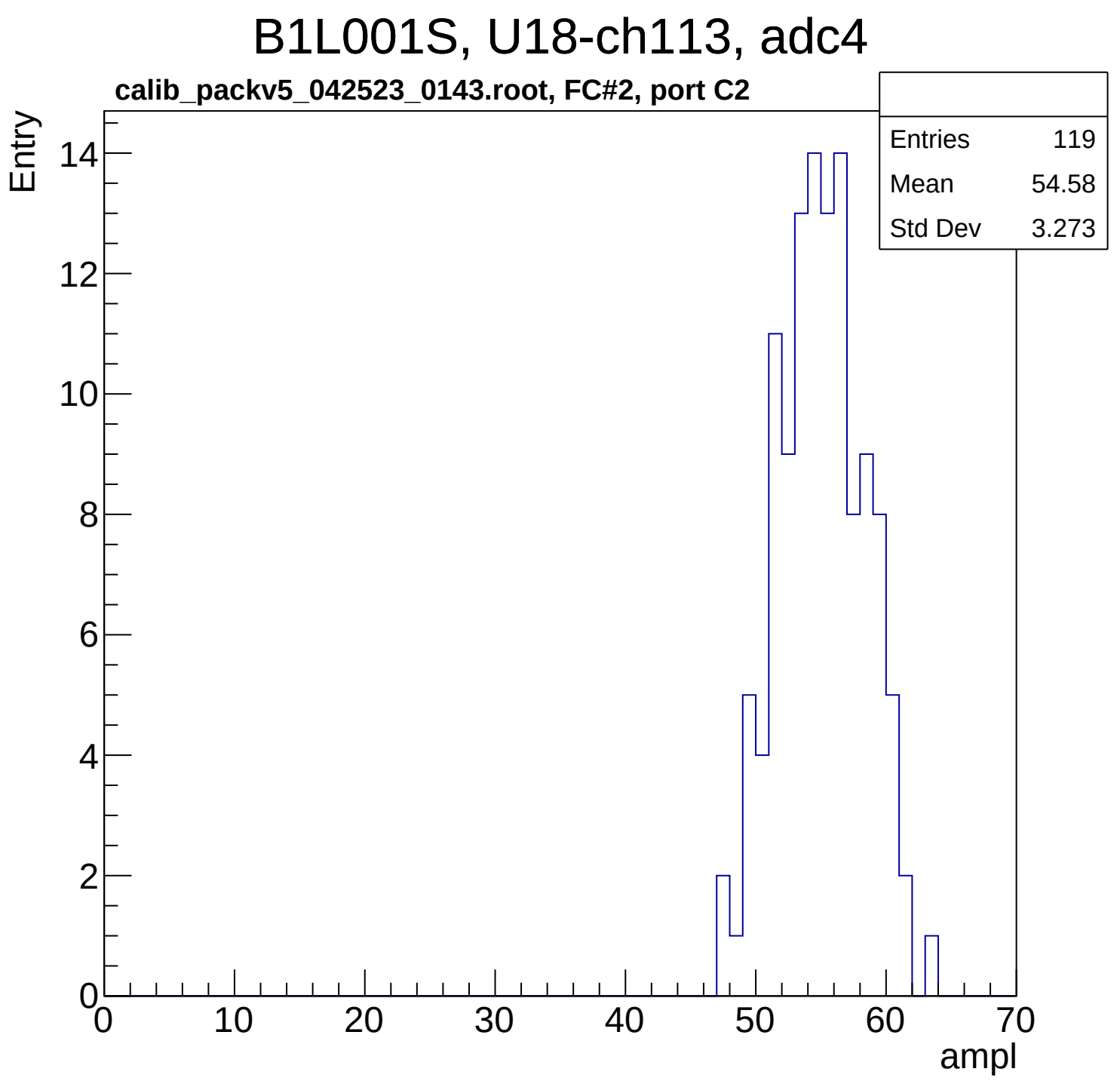

B1L001S, U18-ch112, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 42
Std Dev 21
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70

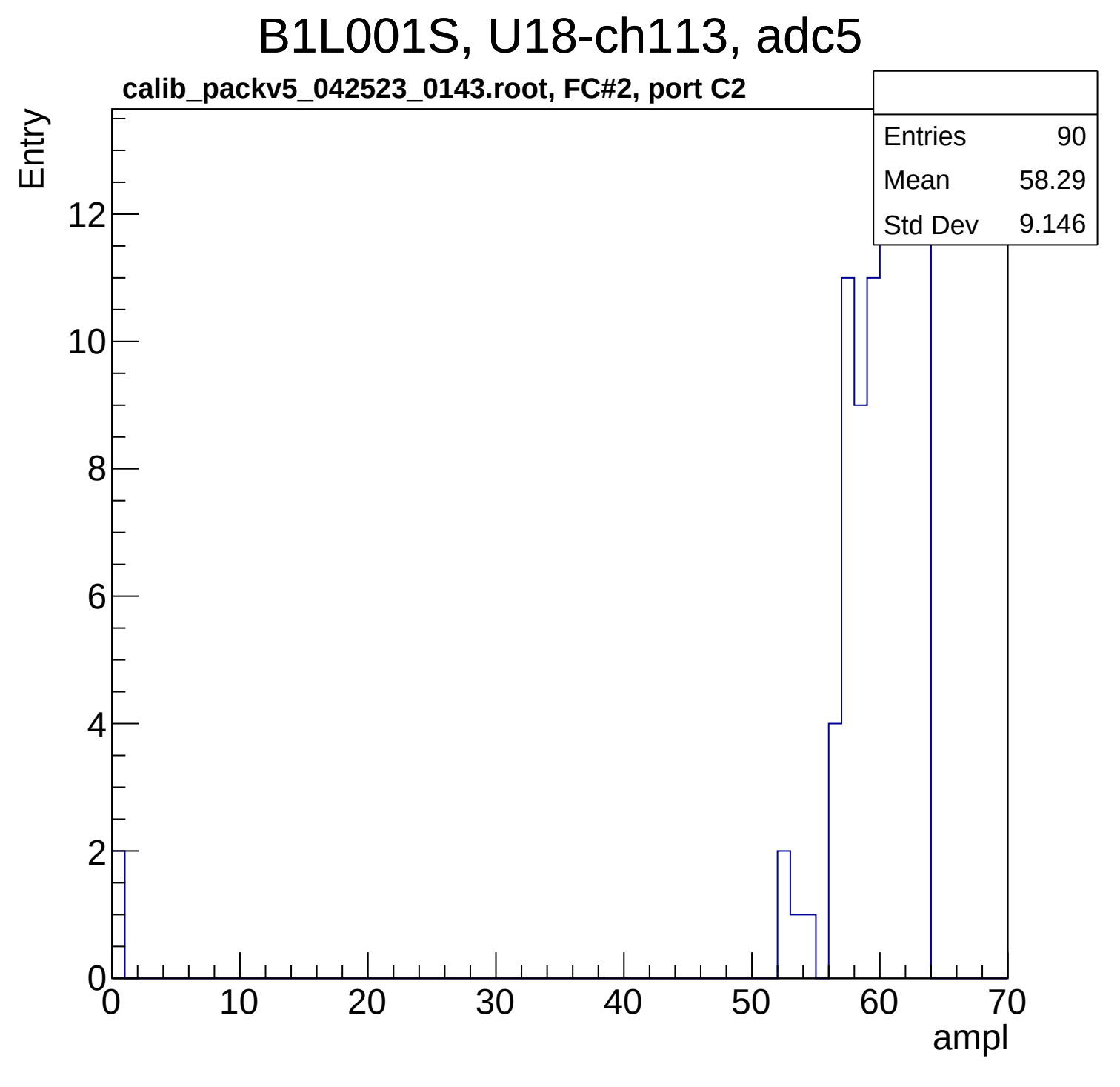

B1L001S, U18-ch113, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 143
Mean 29.47
Std Dev 4.367
Gaus mean : 30.3404
Gaus Width: 3.4846
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

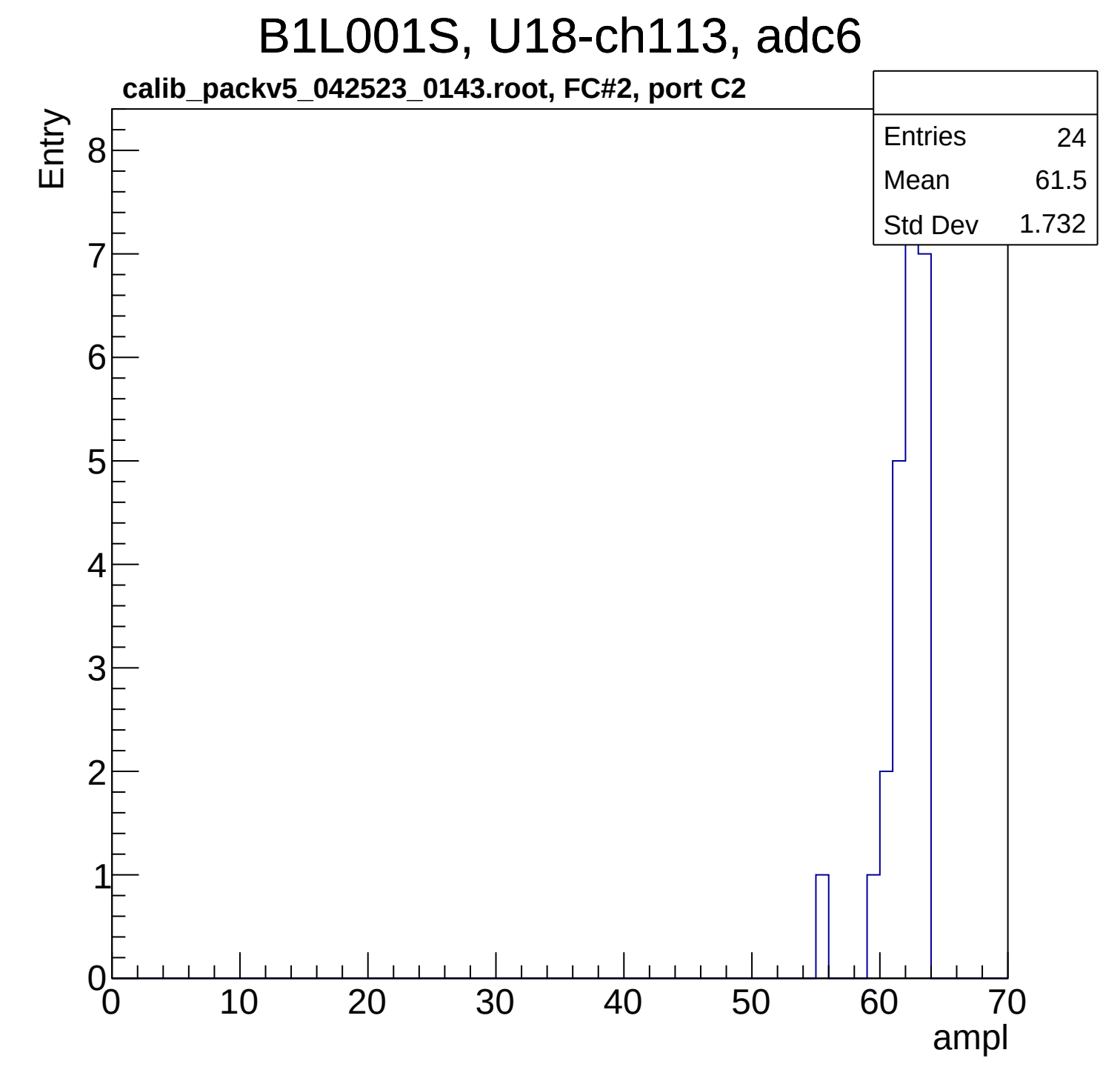

B1L001S, U18-ch113, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 129
Mean 36.55
Std Dev 3.43
Gaus mean : 37.1207
Gaus Width: 3.4211
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

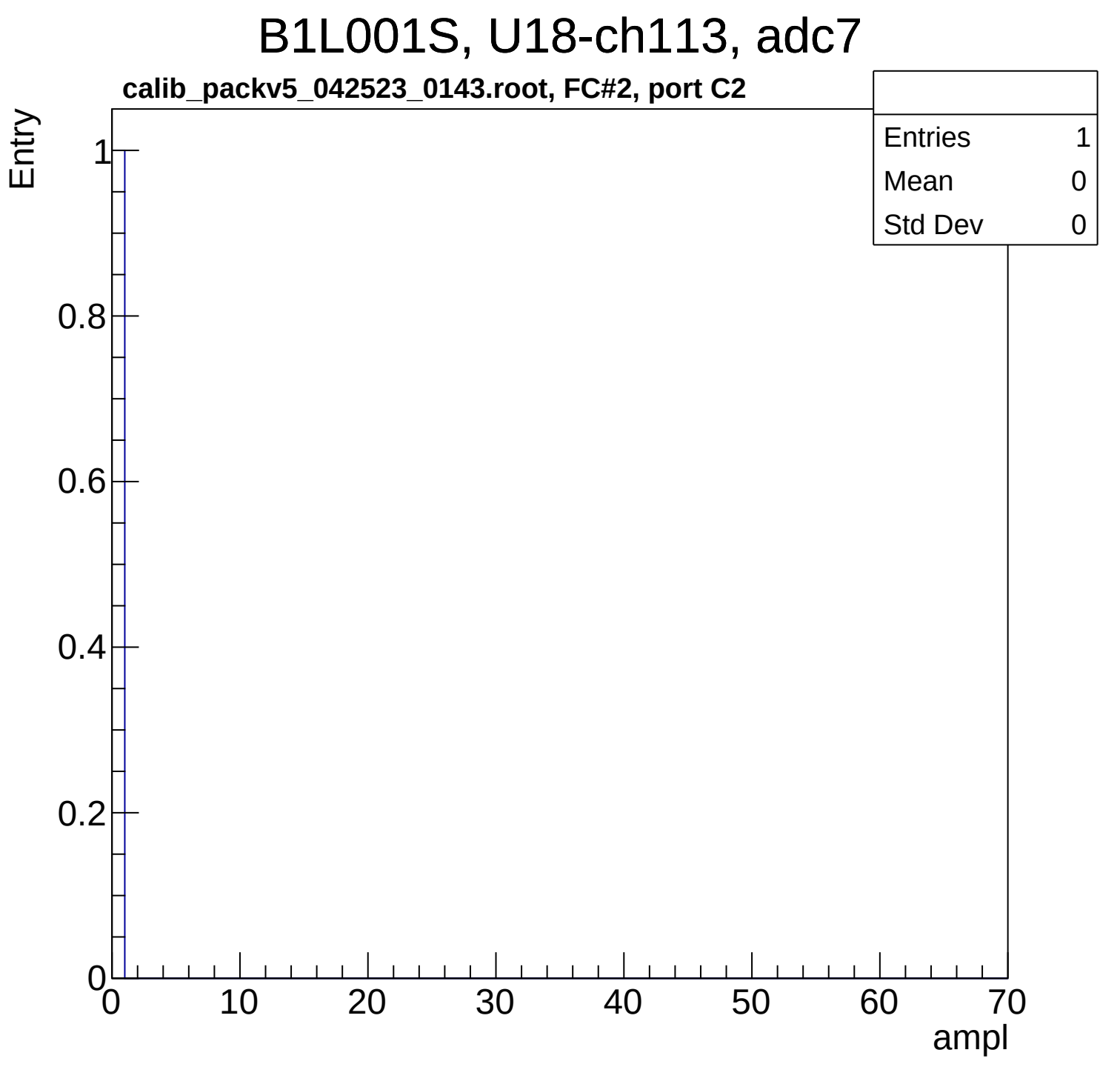

B1L001S, U18-ch113, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 125
Mean 42.88
Std Dev 3.31
Gaus mean : 43.0722
Gaus Width: 3.0619
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

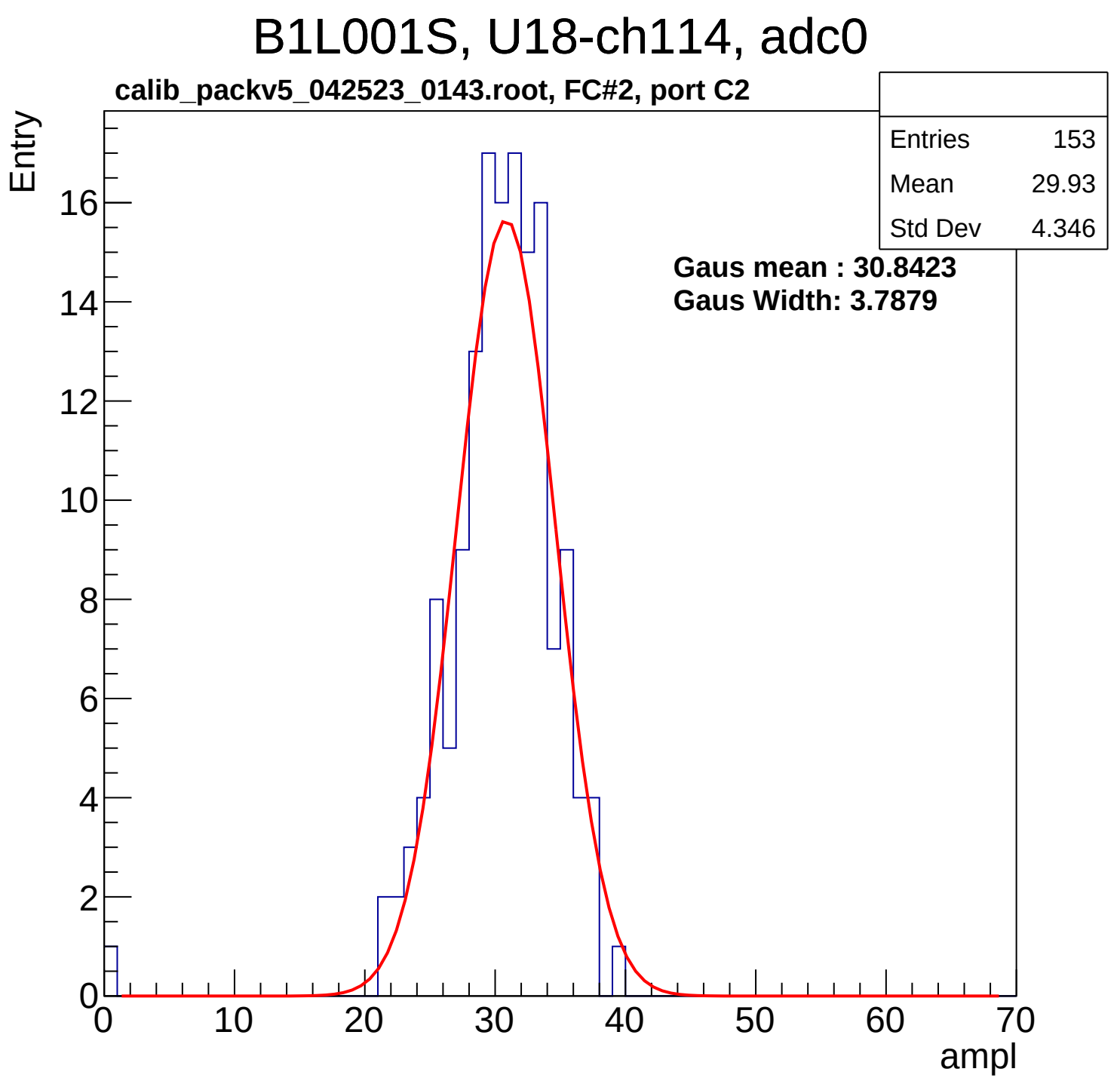

B1L001S, U18-ch113, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 118
Mean 49.38
Std Dev 3.659
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

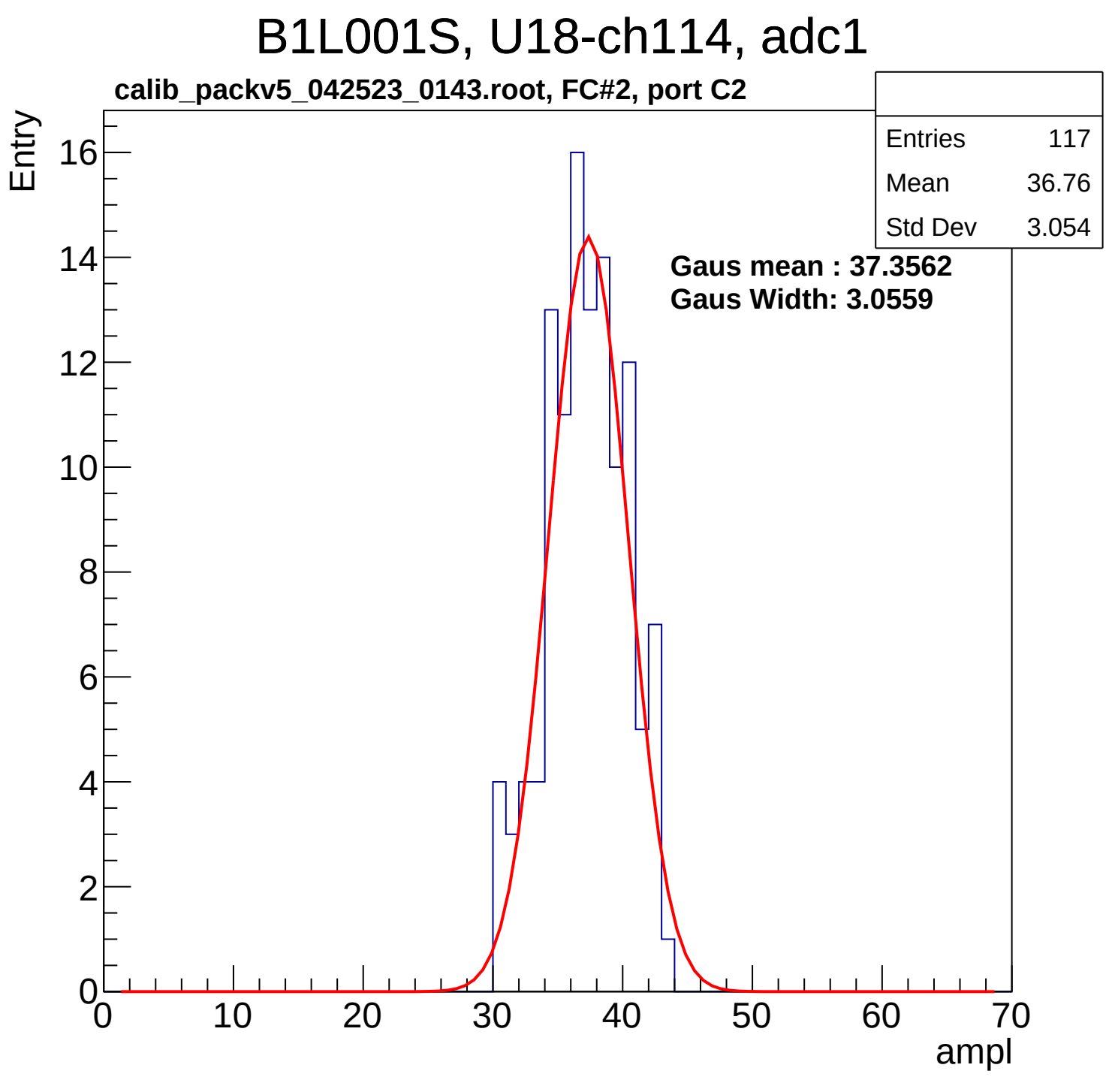

B1L001S, U18-ch113, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 119
Mean 54.58
Std Dev 3.273
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl

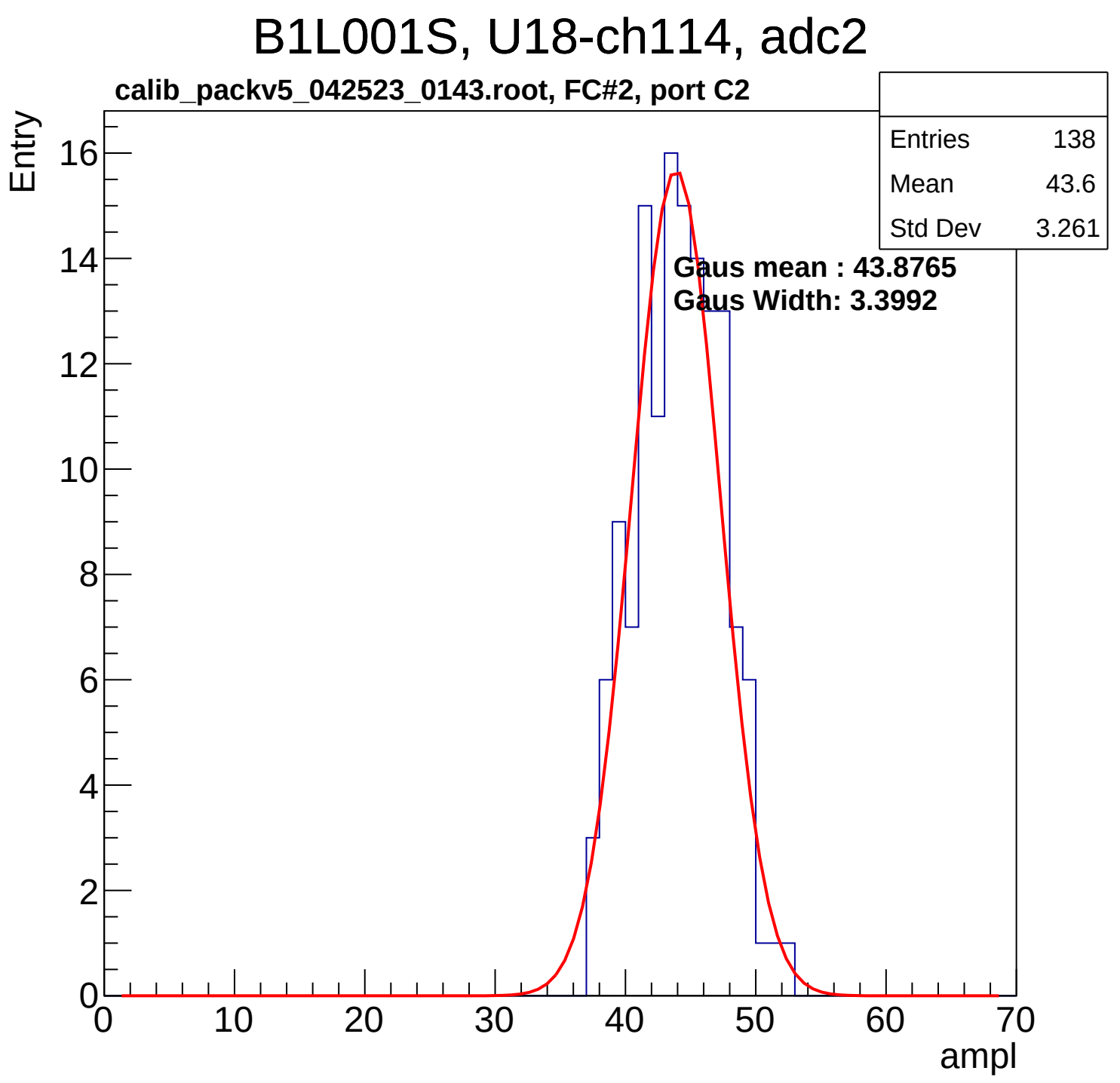

B1L001S, U18-ch113, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 90
Mean 58.29
Std Dev 9.146
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70

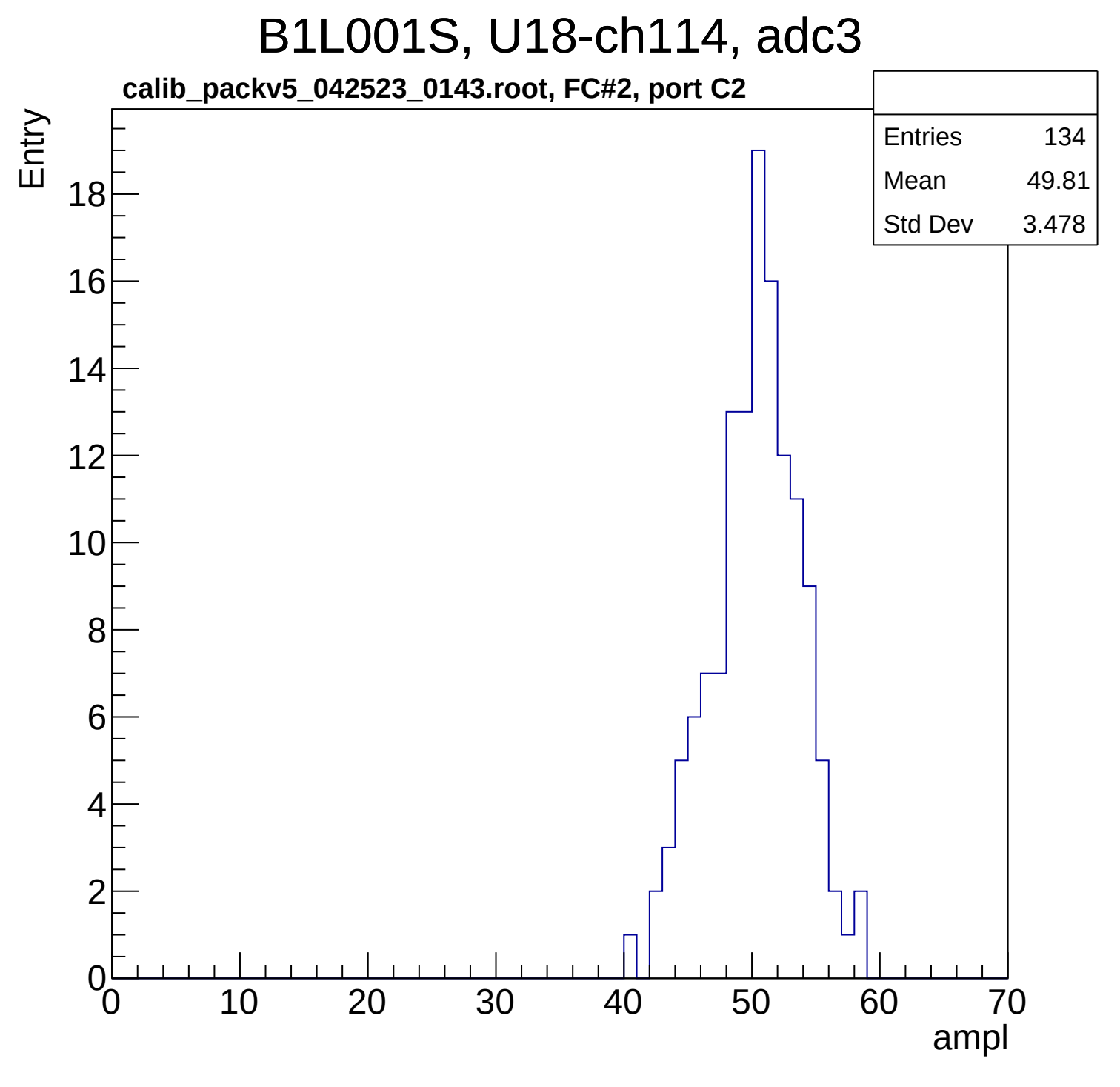

B1L001S, U18-ch113, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 24
Mean 61.5
Std Dev 1.732
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

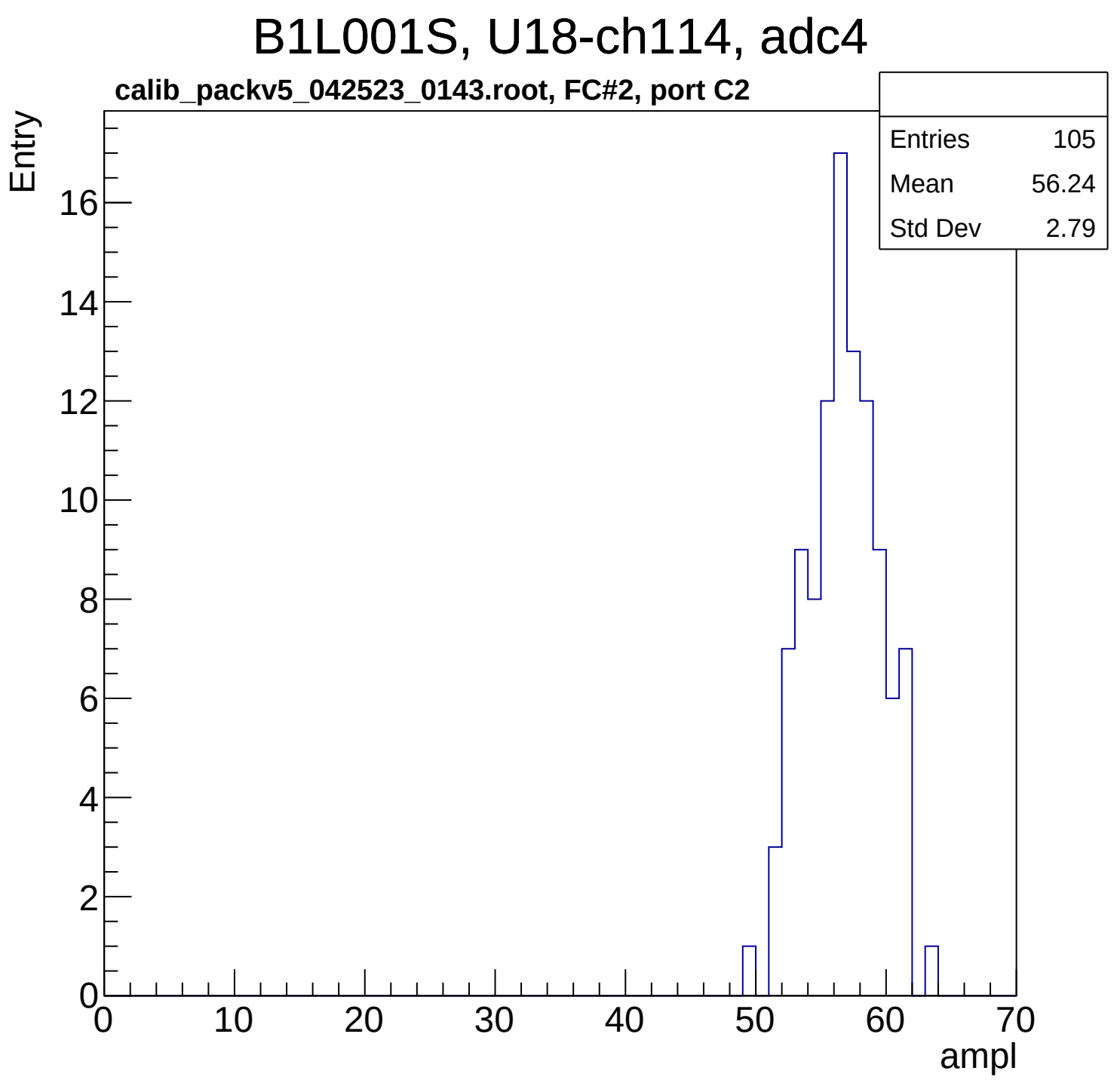

B1L001S, U18-ch113, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

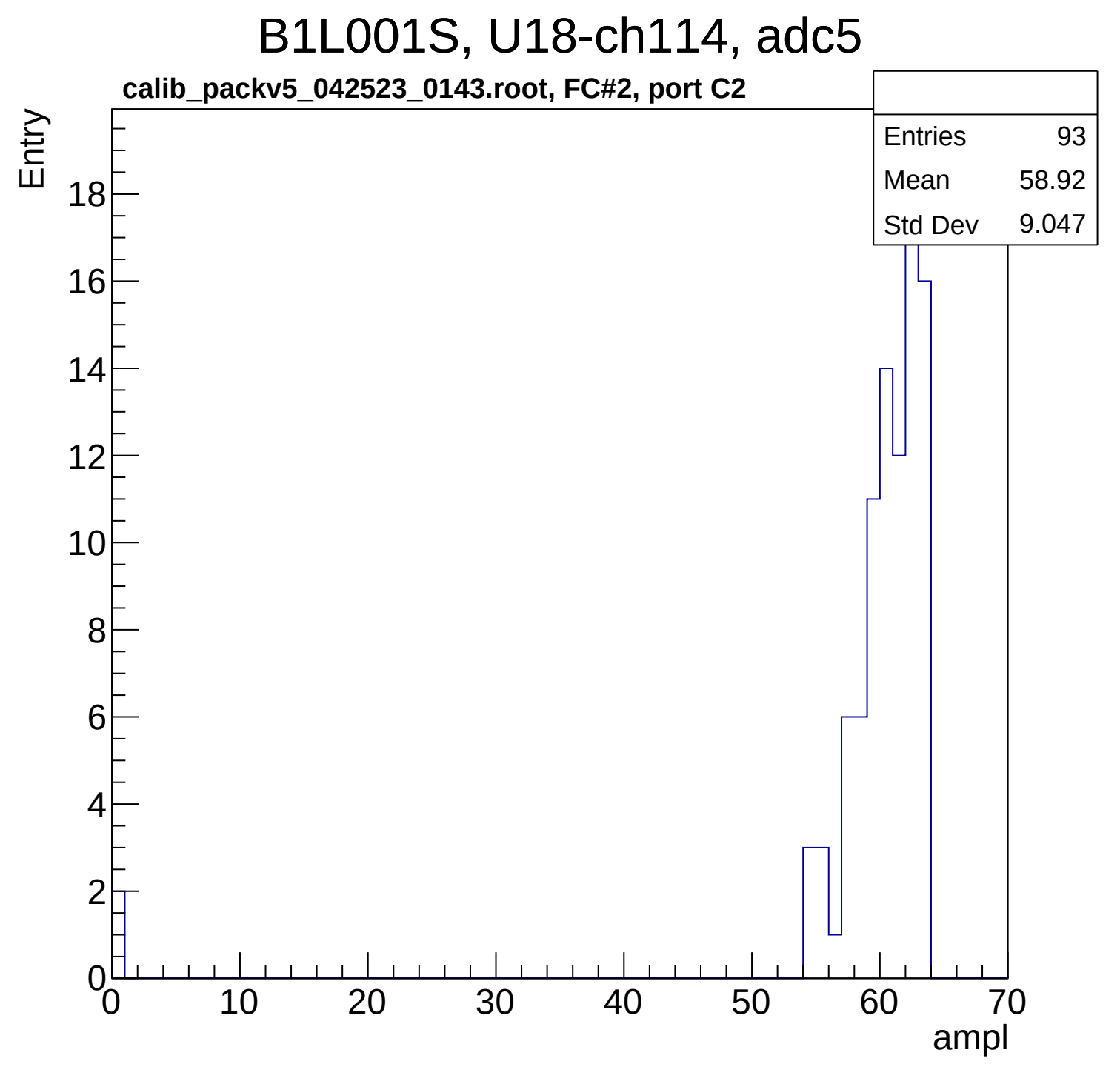

B1L001S, U18-ch114, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 153
Mean 29.93
Std Dev 4.346
Gaus mean : 30.8423
Gaus Width: 3.7879
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

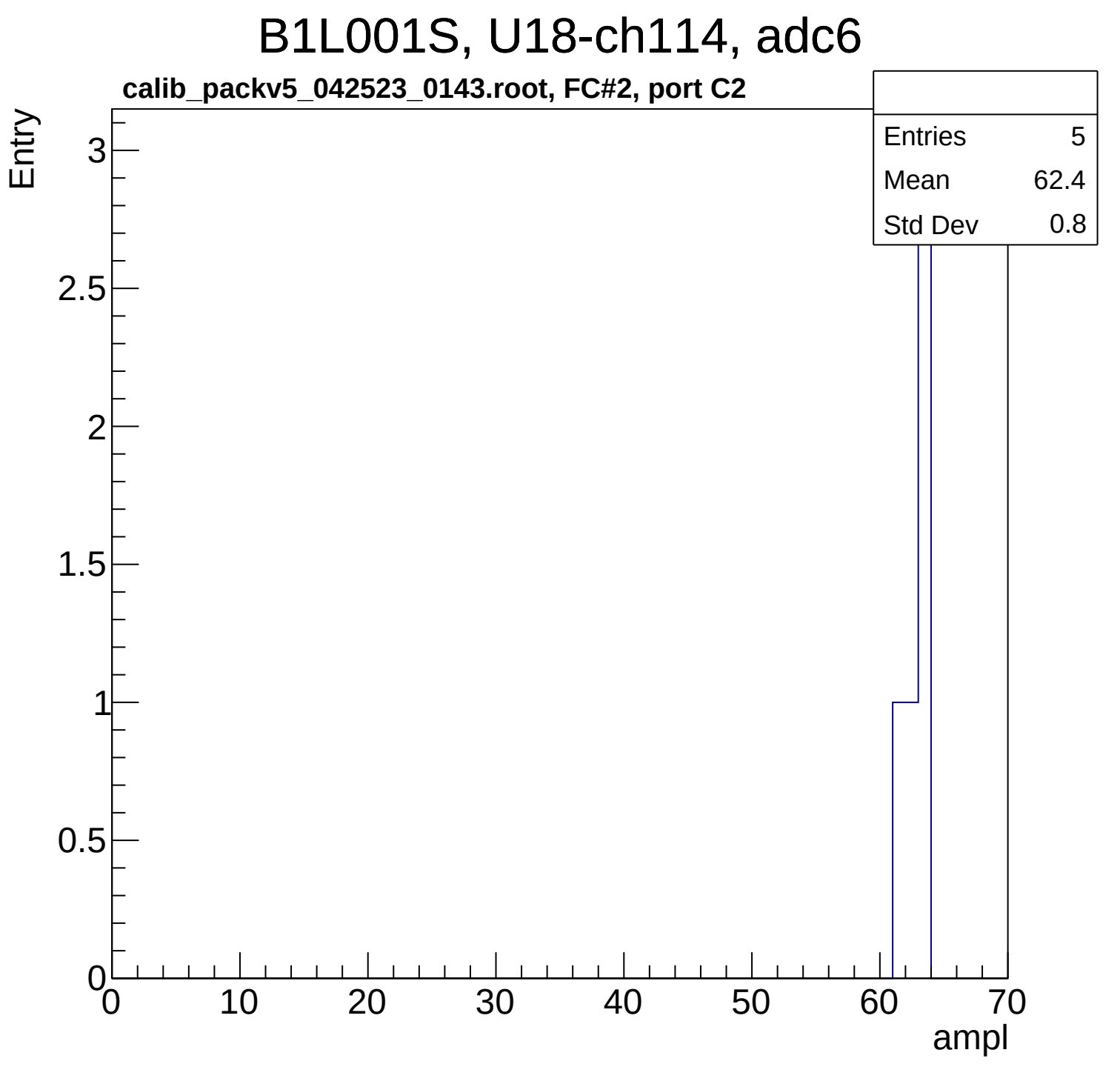

B1L001S, U18-ch114, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 117
Mean 36.76
Std Dev 3.054
Gaus mean : 37.3562
Gaus Width: 3.0559
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

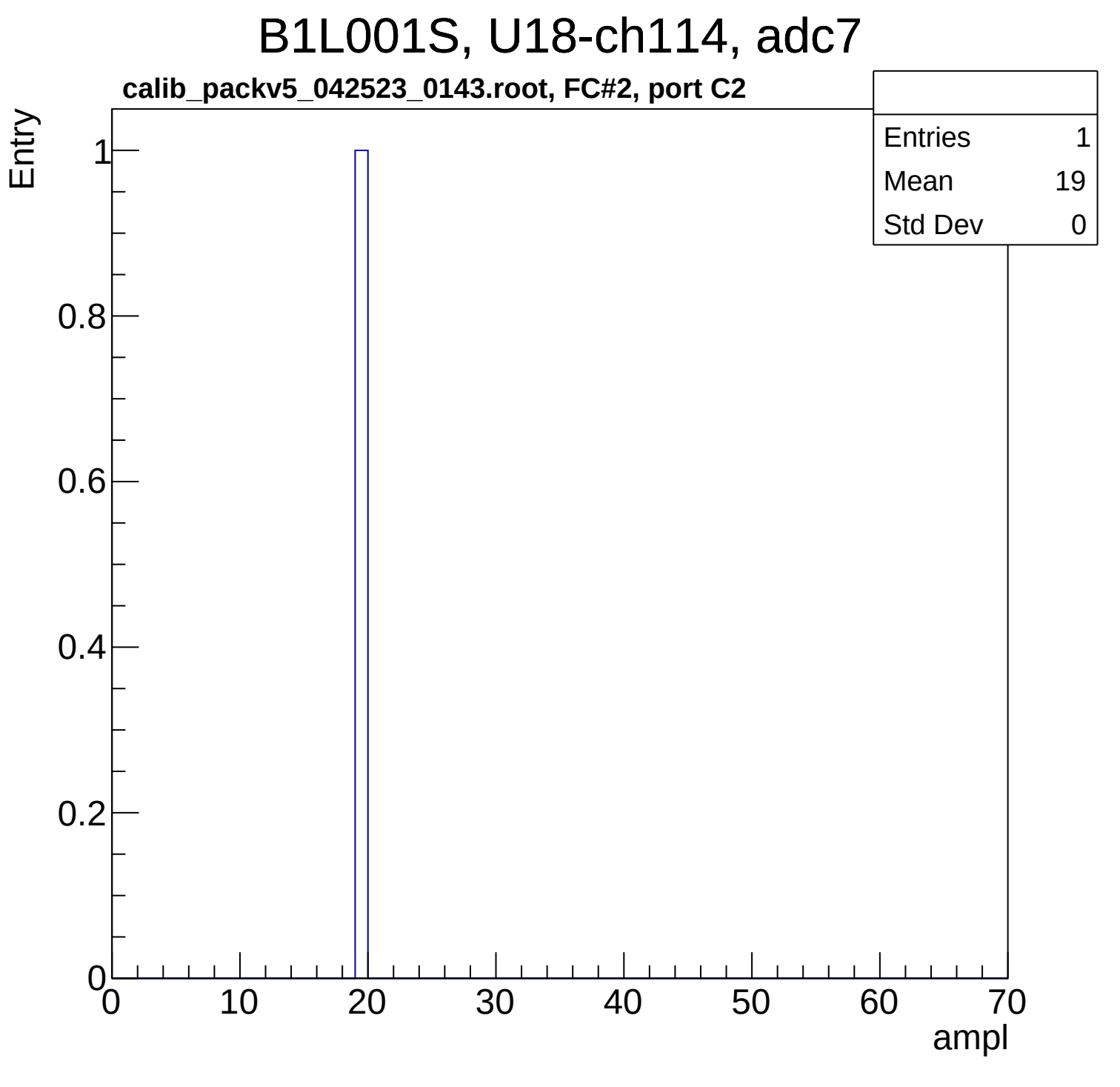

B1L001S, U18-ch114, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 138
Mean 43.6
Std Dev 3.261
Gaus mean : 43.8765
Gaus Width: 3.3992
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

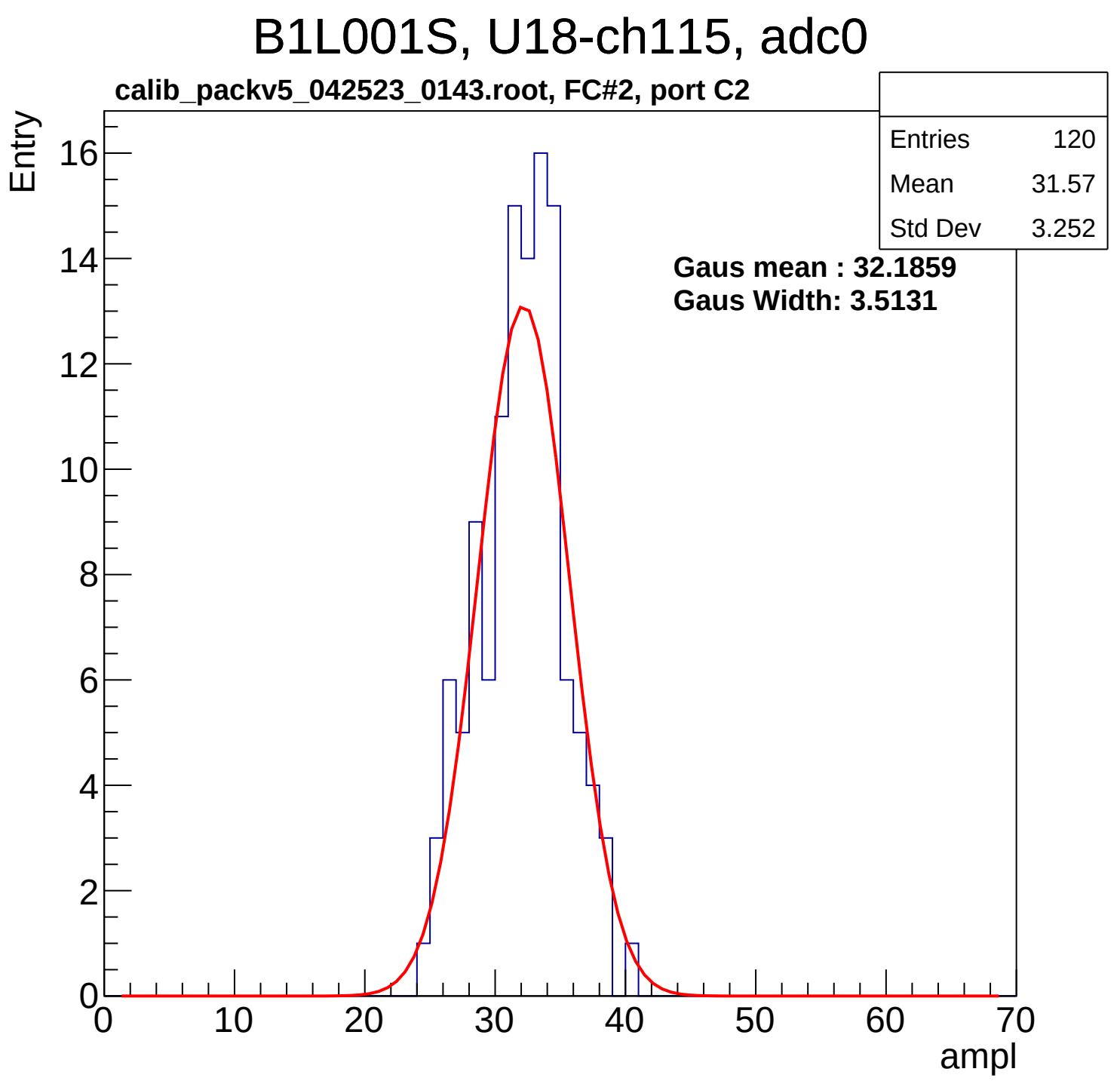

B1L001S, U18-ch114, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 134
Mean 49.81
Std Dev 3.478
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

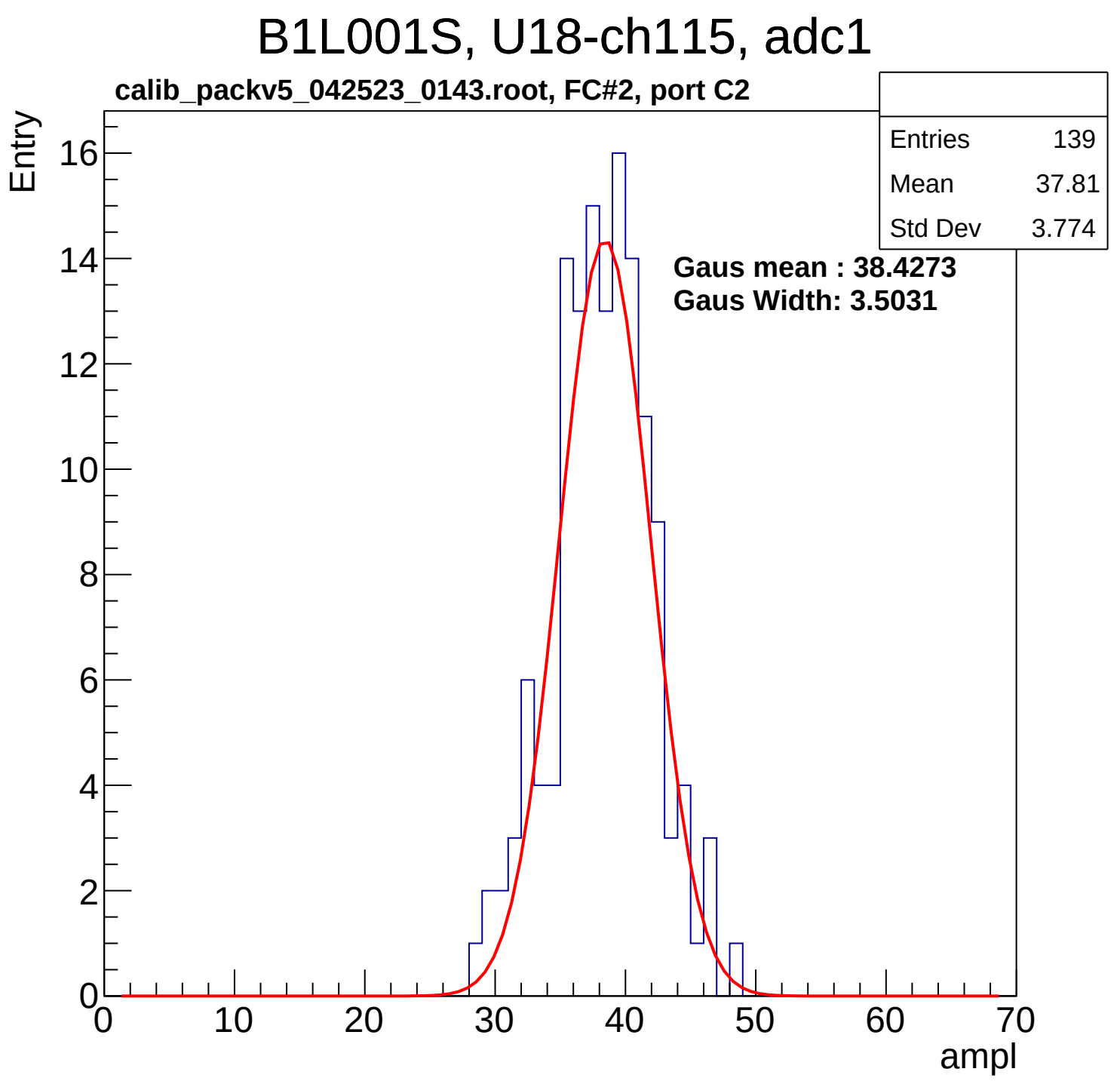

B1L001S, U18-ch114, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 105
Mean 56.24
Std Dev 2.79
Entry
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl

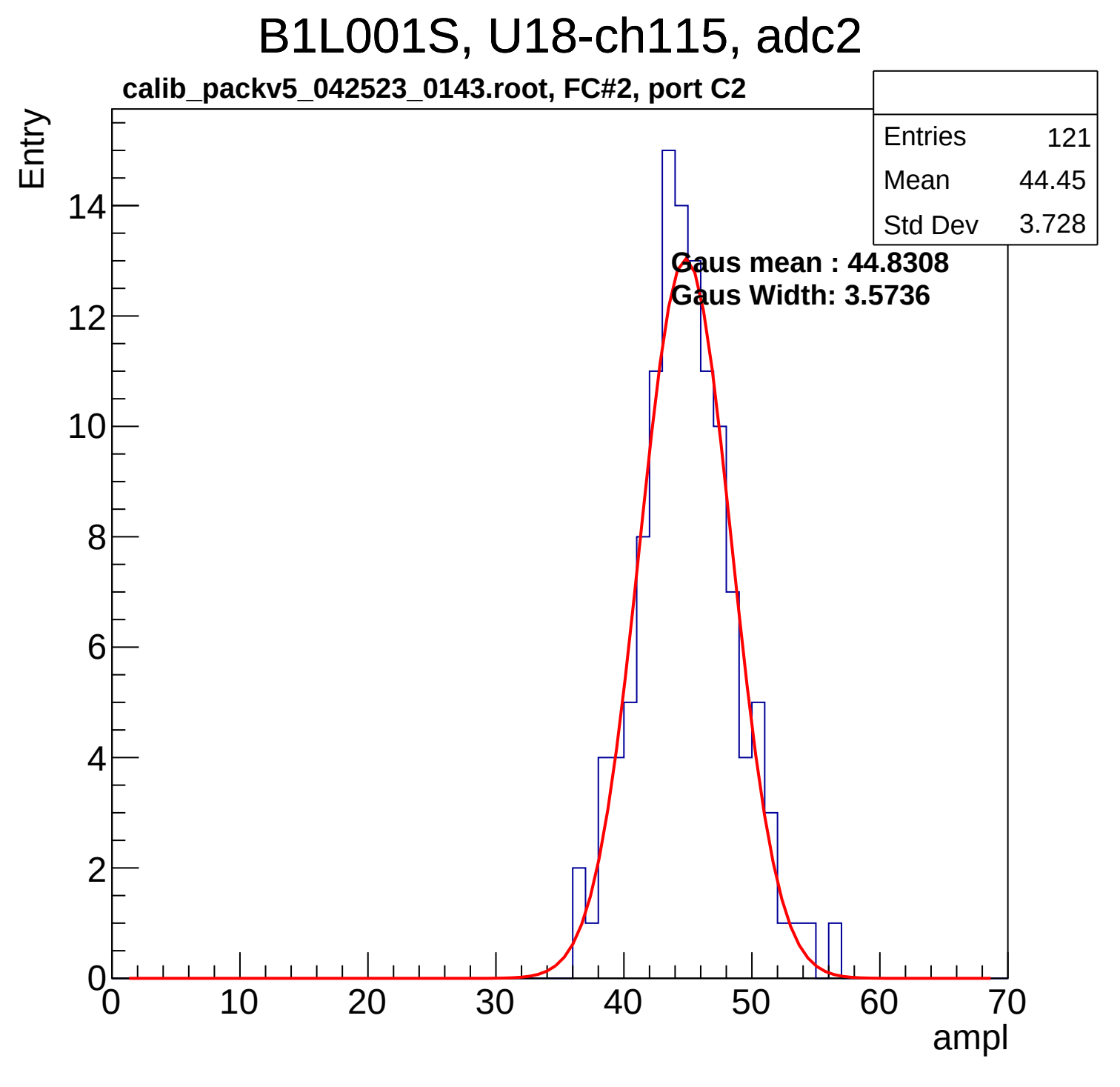

B1L001S, U18-ch114, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 93
Mean 58.92
Std Dev 9.047
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

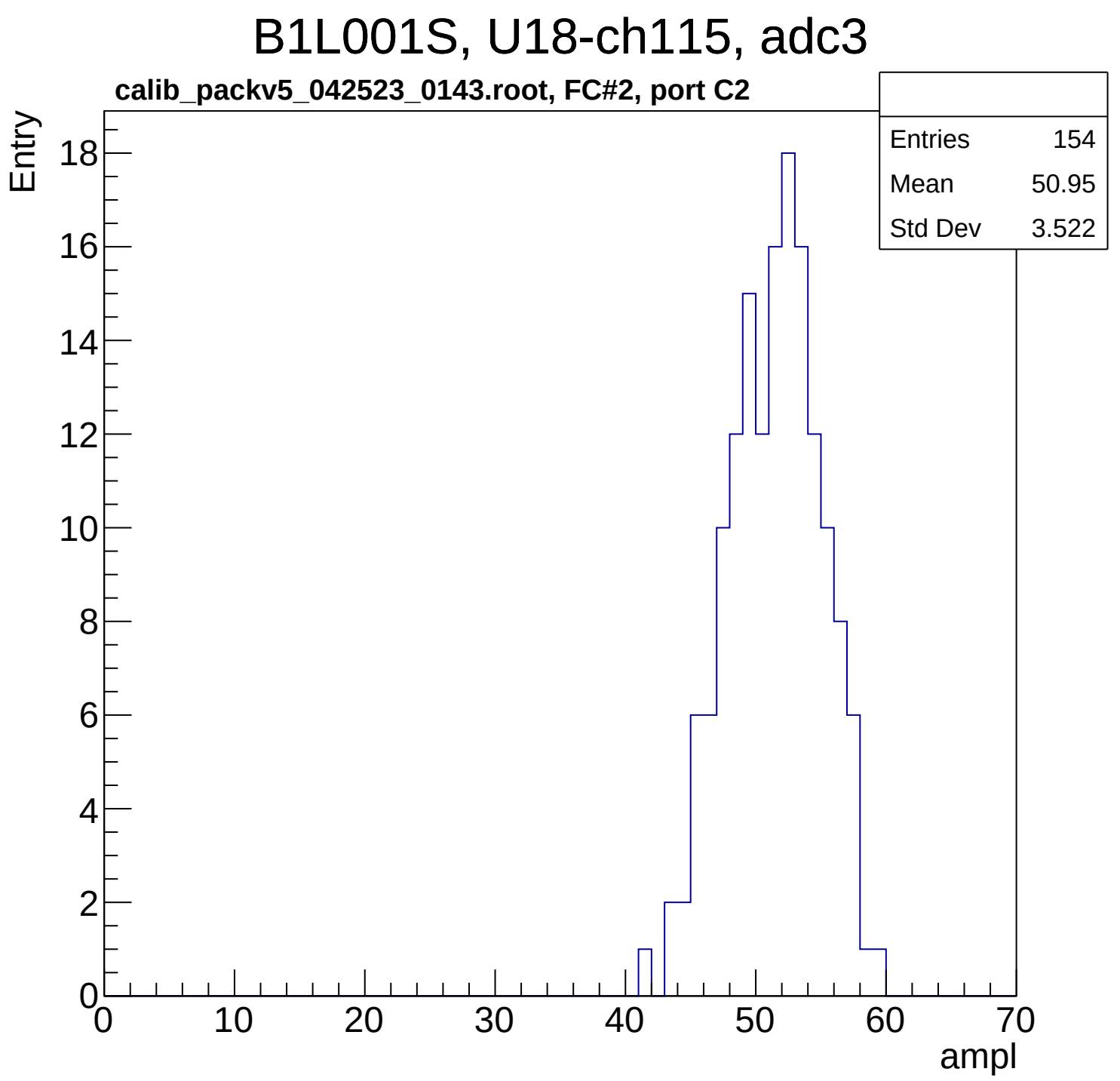

B1L001S, U18-ch114, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 5
Mean 62.4
Std Dev 0.8
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

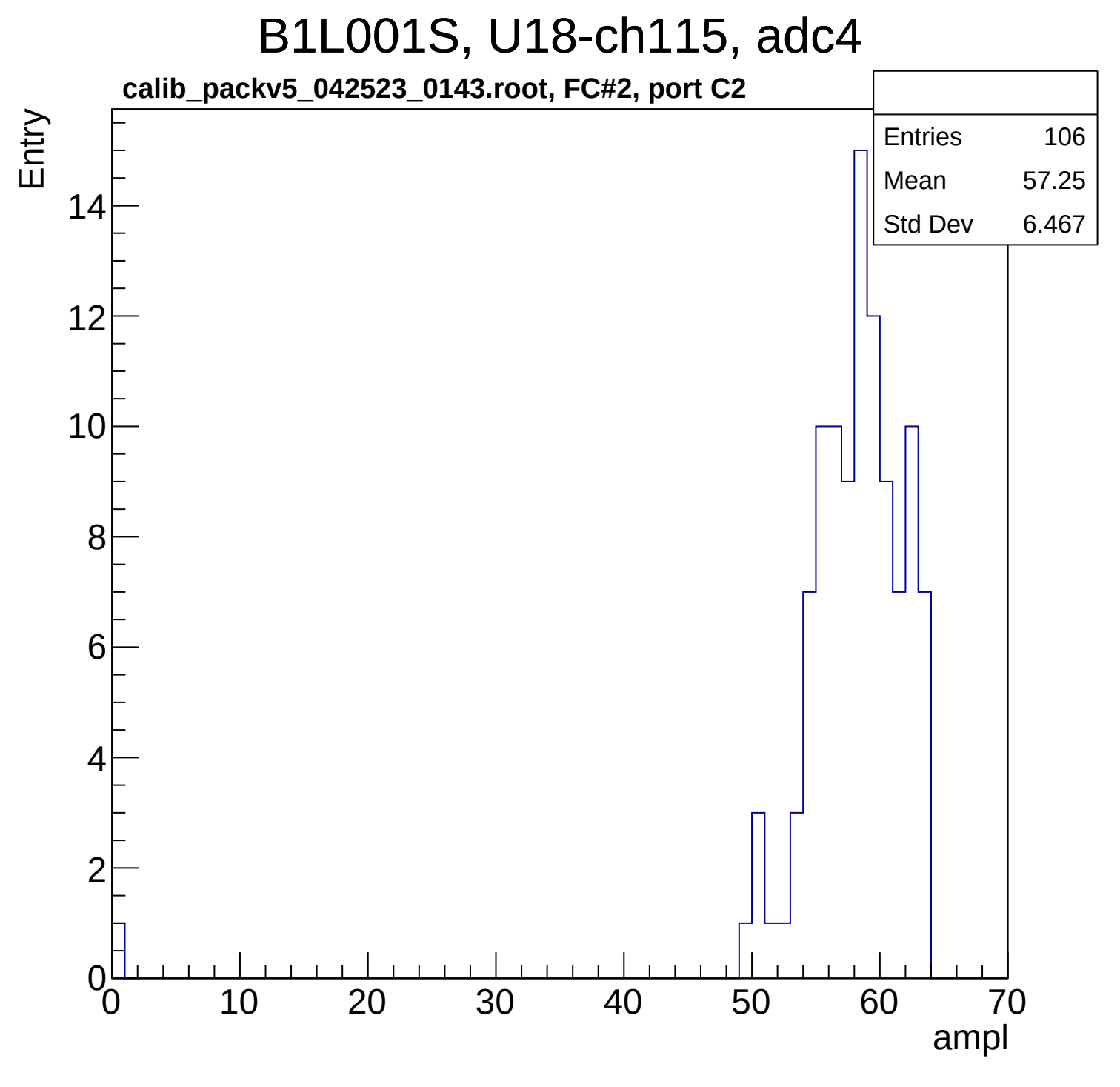

B1L001S, U18-ch114, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 19
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

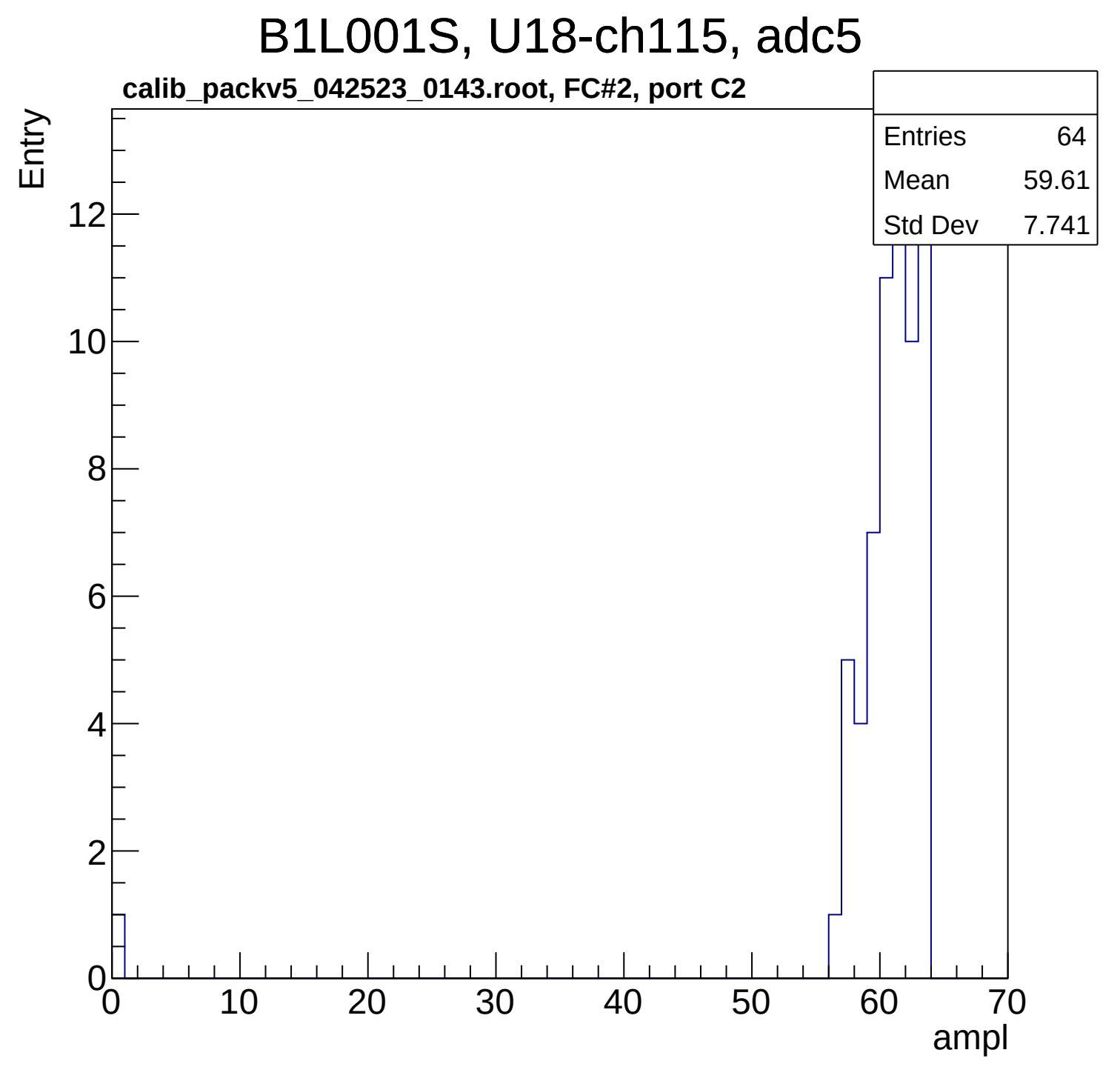

B1L001S, U18-ch115, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 120
Mean 31.57
Std Dev 3.252
Gaus mean : 32.1859
Gaus Width: 3.5131
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

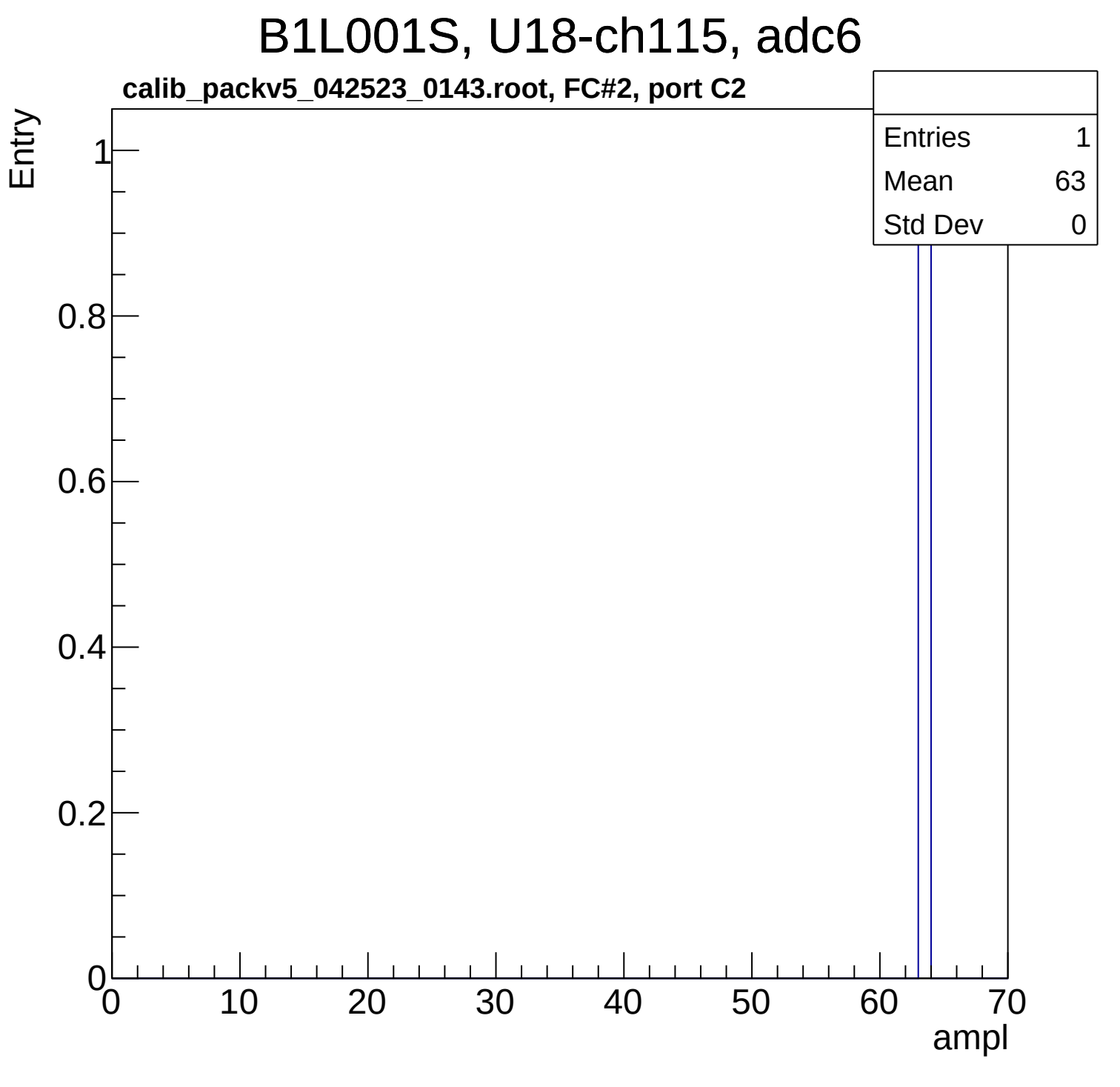

B1L001S, U18-ch115, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 139
Mean 37.81
Std Dev 3.774
Gaus mean : 38.4273
Gaus Width: 3.5031
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

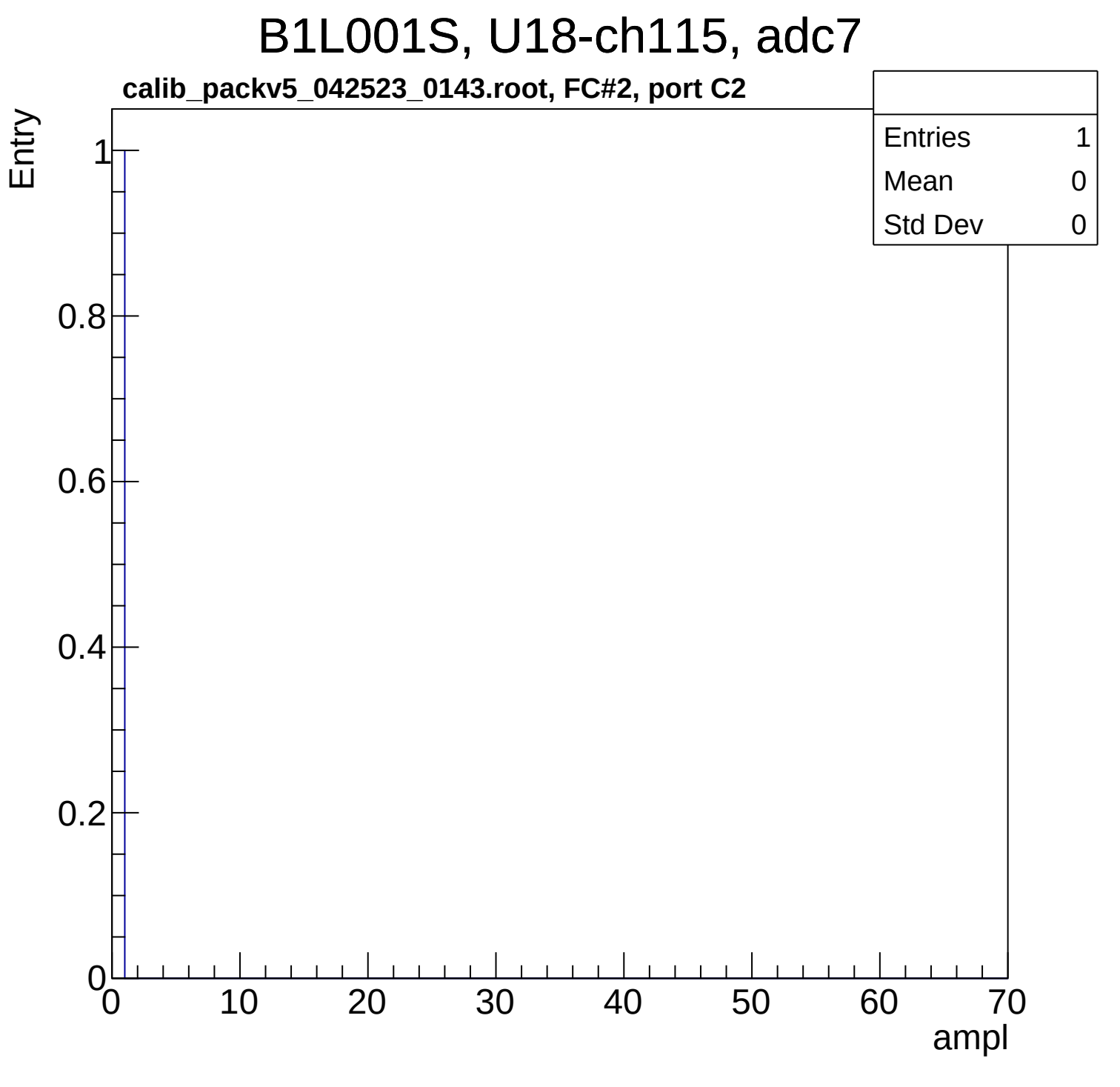

B1L001S, U18-ch115, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 121
Mean 44.45
Std Dev 3.728
Gaus mean : 44.8308
Gaus Width: 3.5736
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

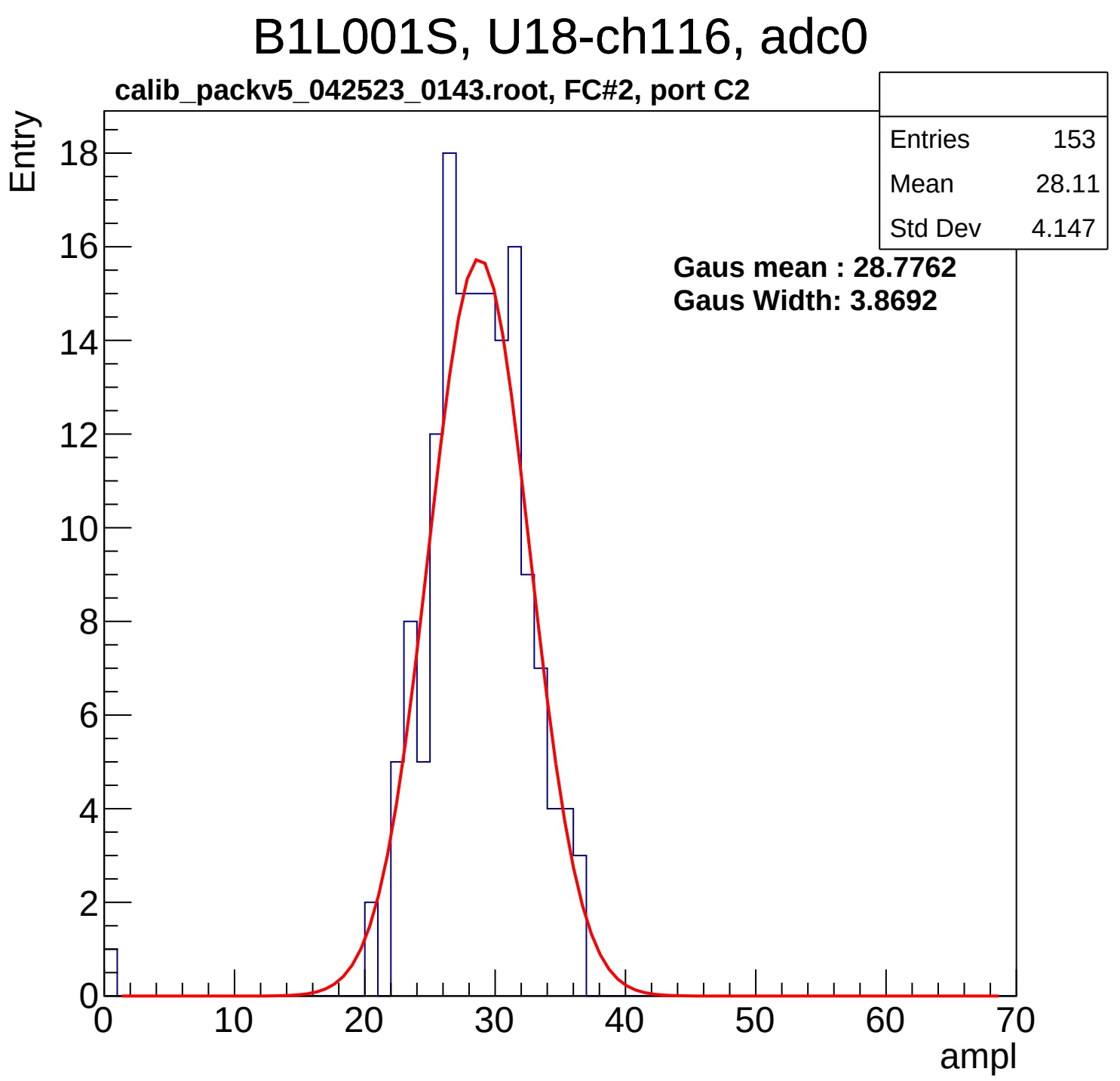

B1L001S, U18-ch115, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 154
Mean 50.95
Std Dev 3.522
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

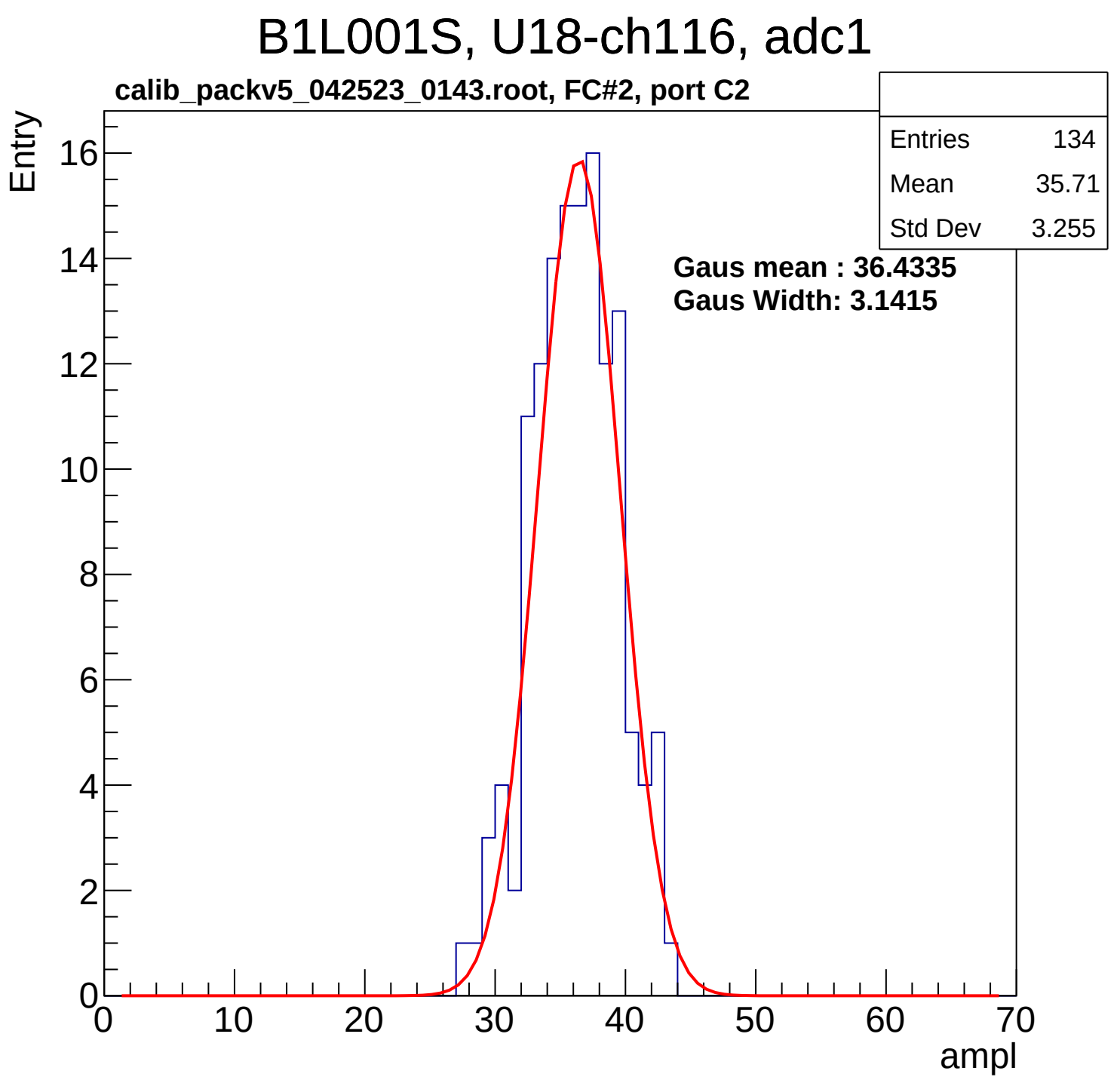

B1L001S, U18-ch115, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 106
Mean 57.25
Std Dev 6.467
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

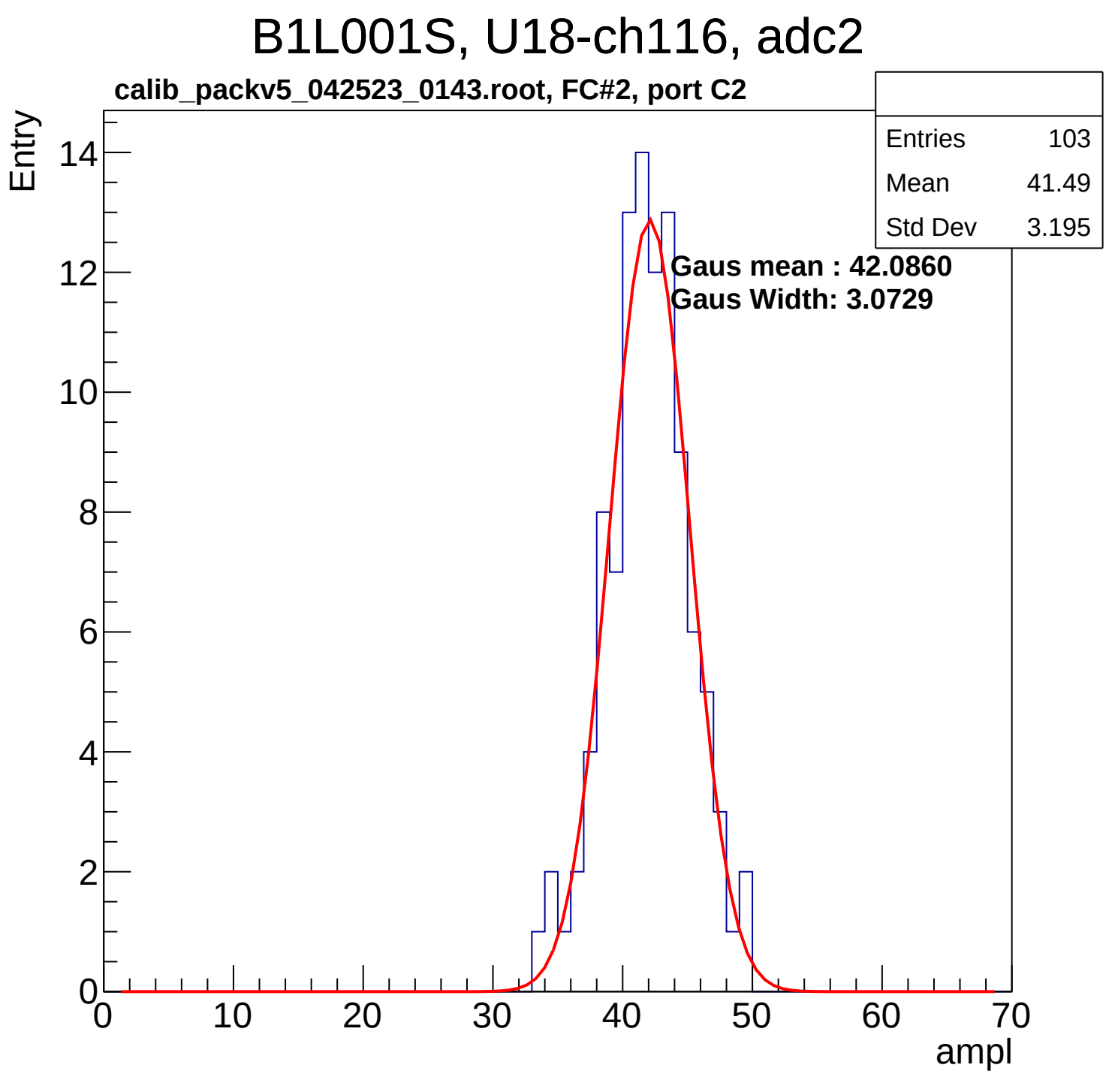

B1L001S, U18-ch115, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 64
Mean 59.61
Std Dev 7.741
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70

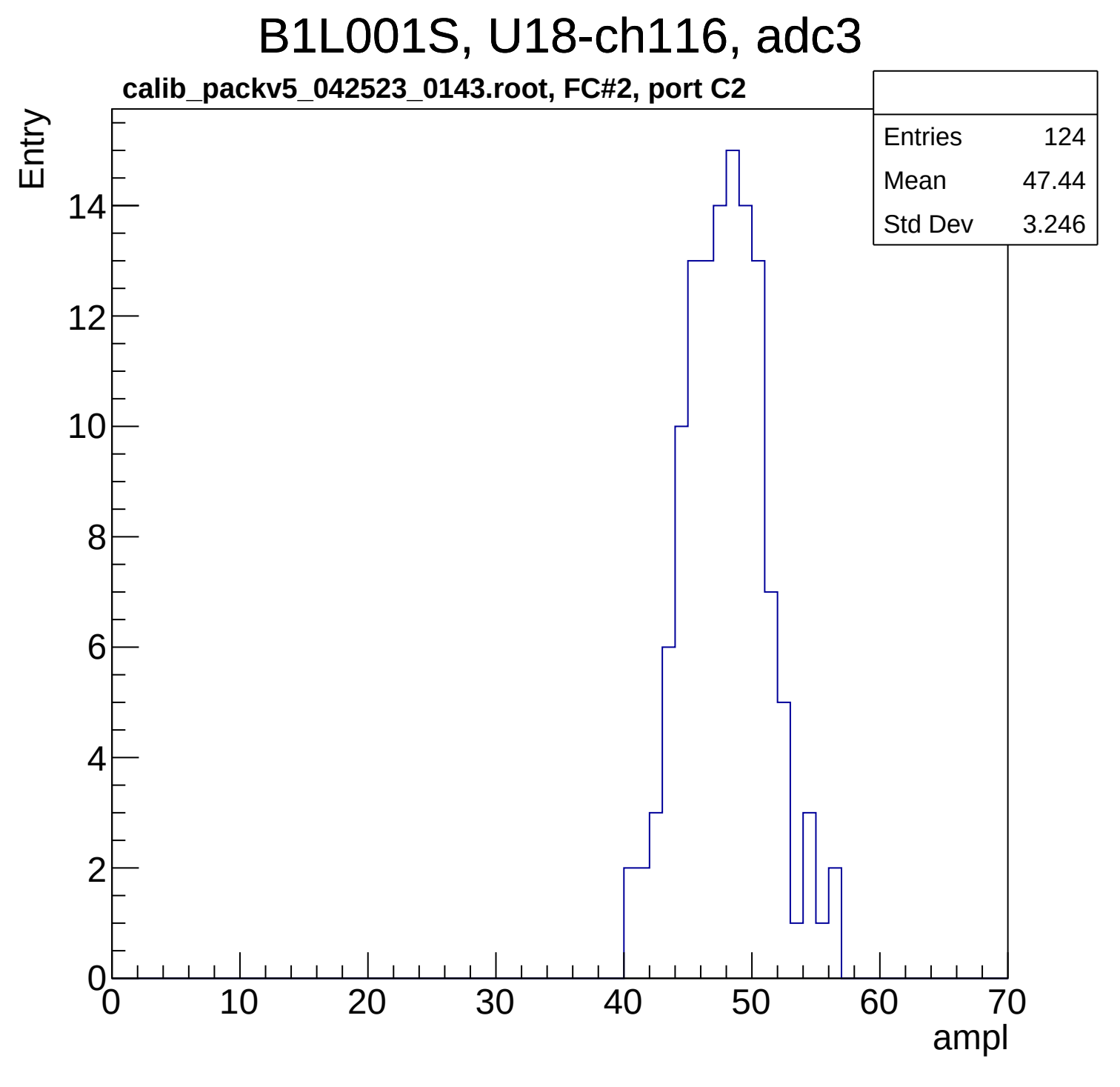

B1L001S, U18-ch115, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 63
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

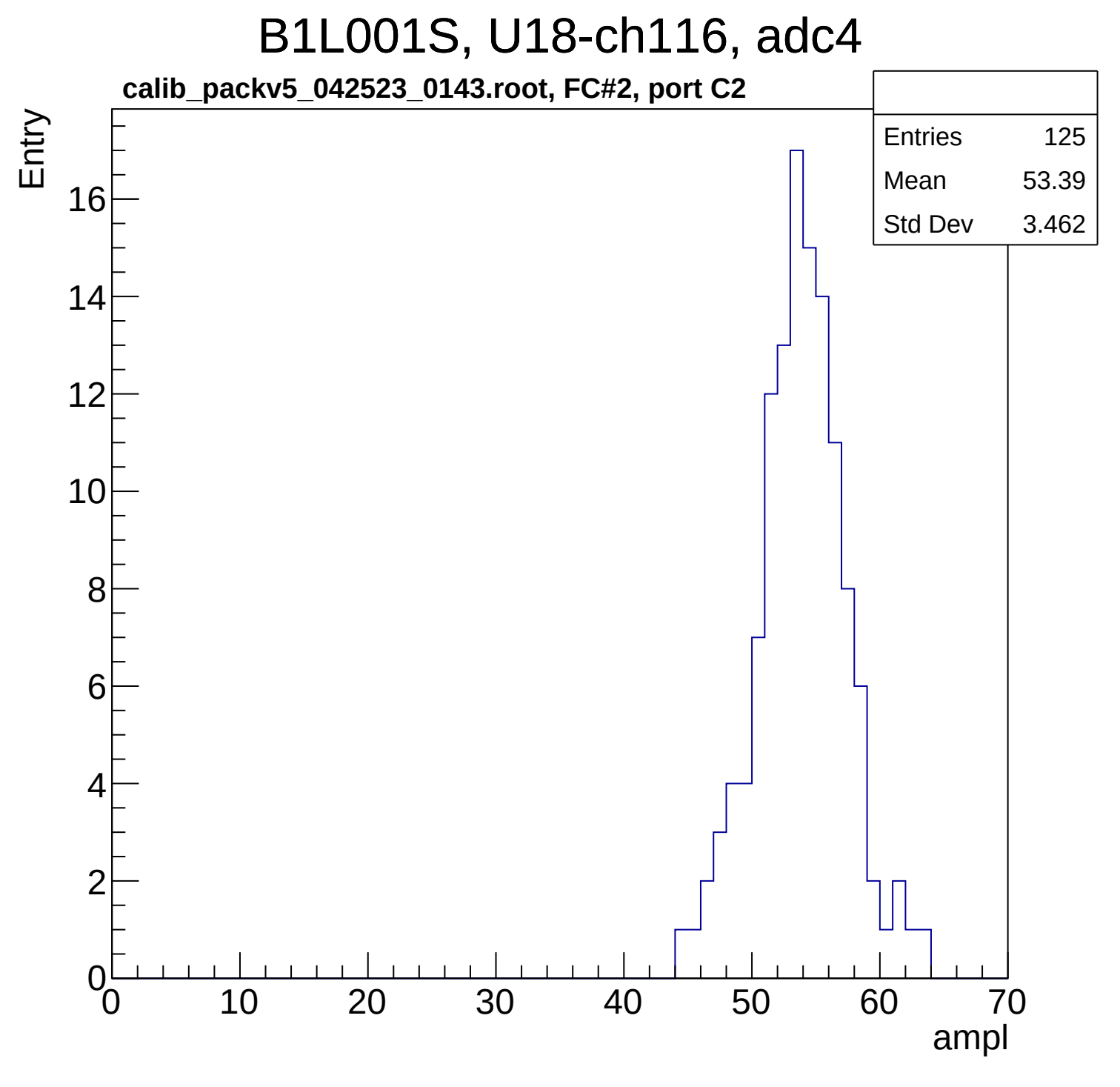

B1L001S, U18-ch115, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

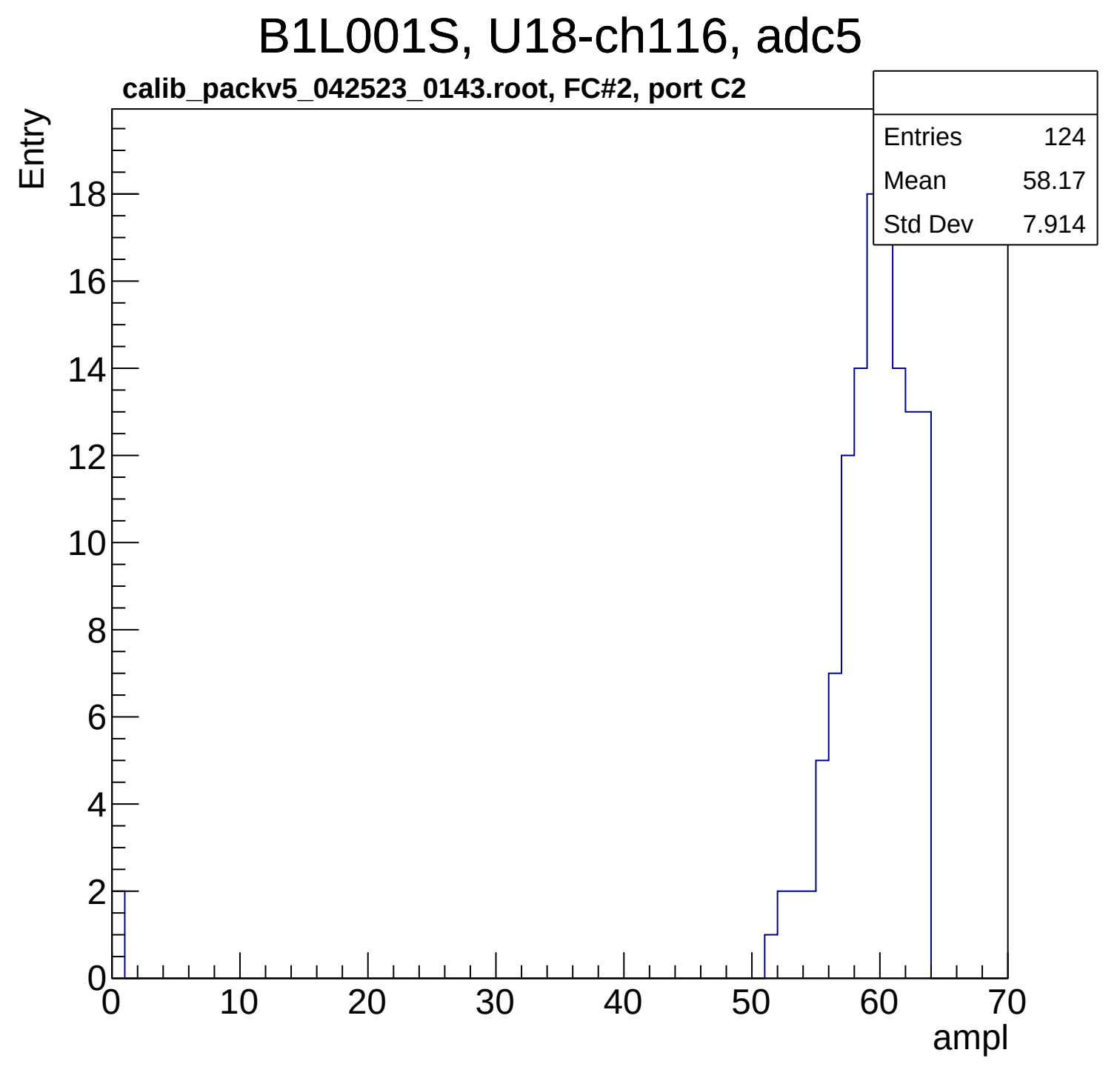

B1L001S, U18-ch116, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 153
Mean 28.11
Std Dev 4.147
Gaus mean : 28.7762
Gaus Width: 3.8692
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

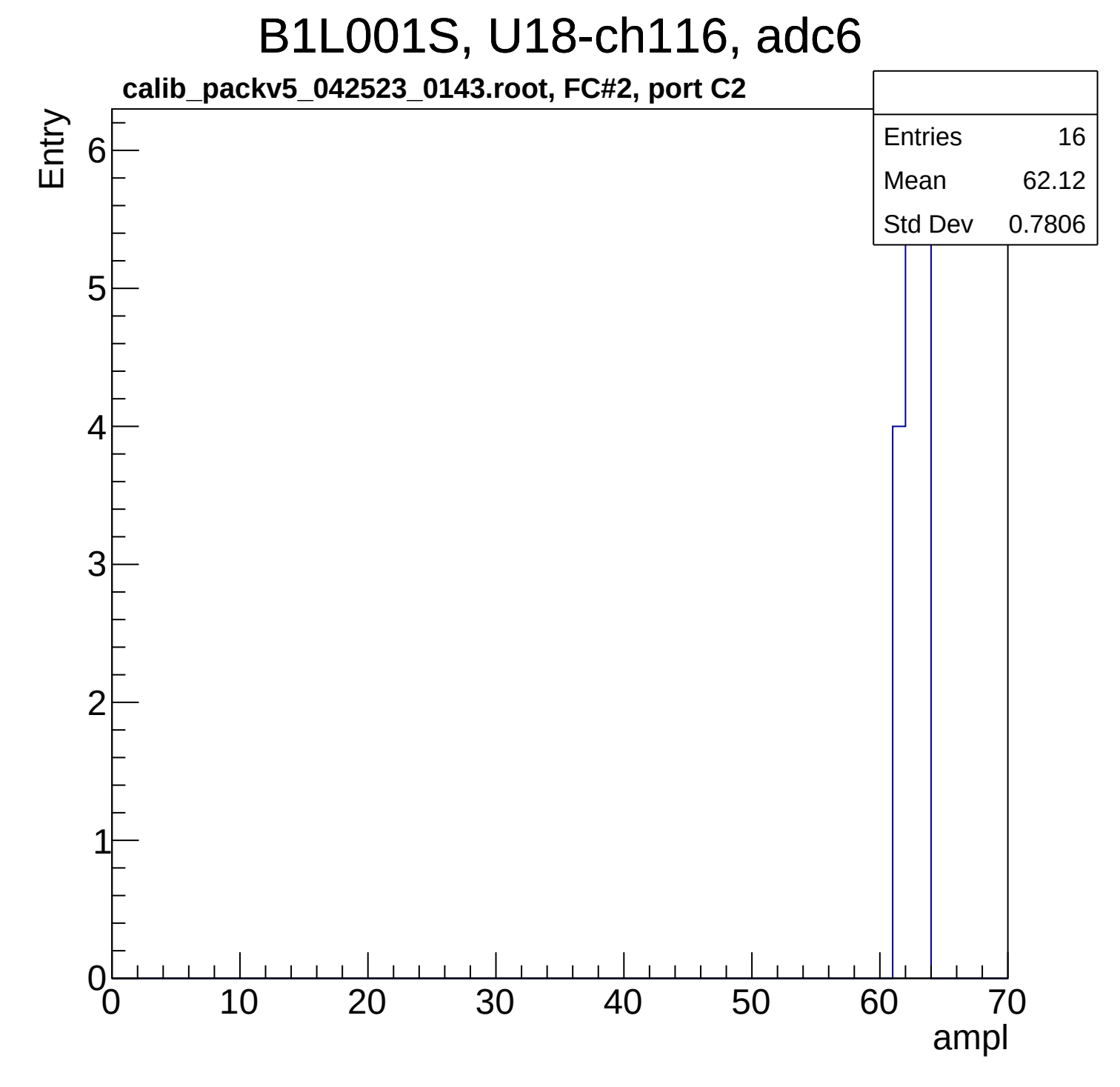

B1L001S, U18-ch116, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 134
Mean 35.71
Std Dev 3.255
Gaus mean : 36.4335
Gaus Width: 3.1415
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

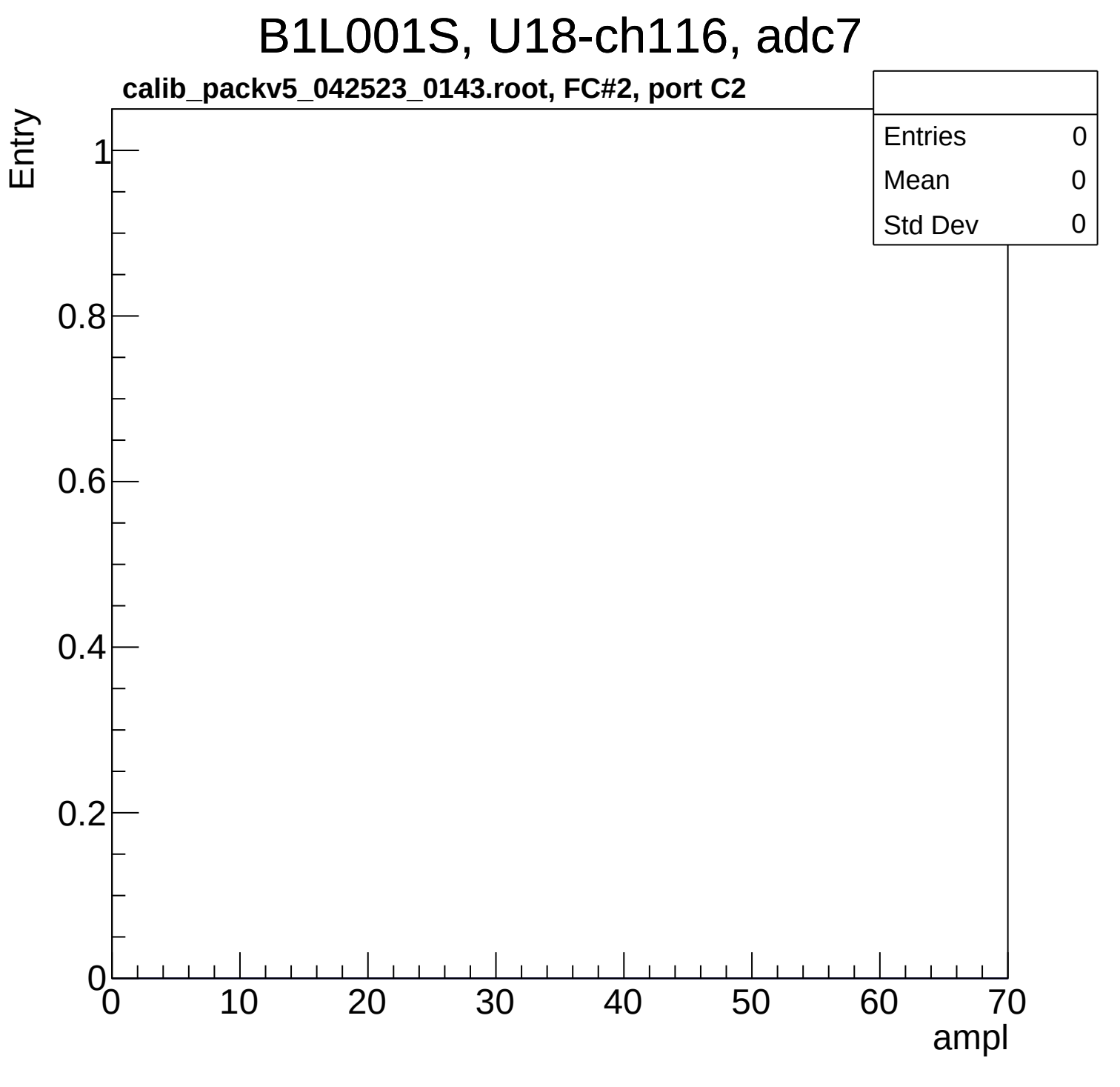

B1L001S, U18-ch116, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 103
Mean 41.49
Std Dev 3.195
Gaus mean : 42.0860
Gaus Width: 3.0729
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

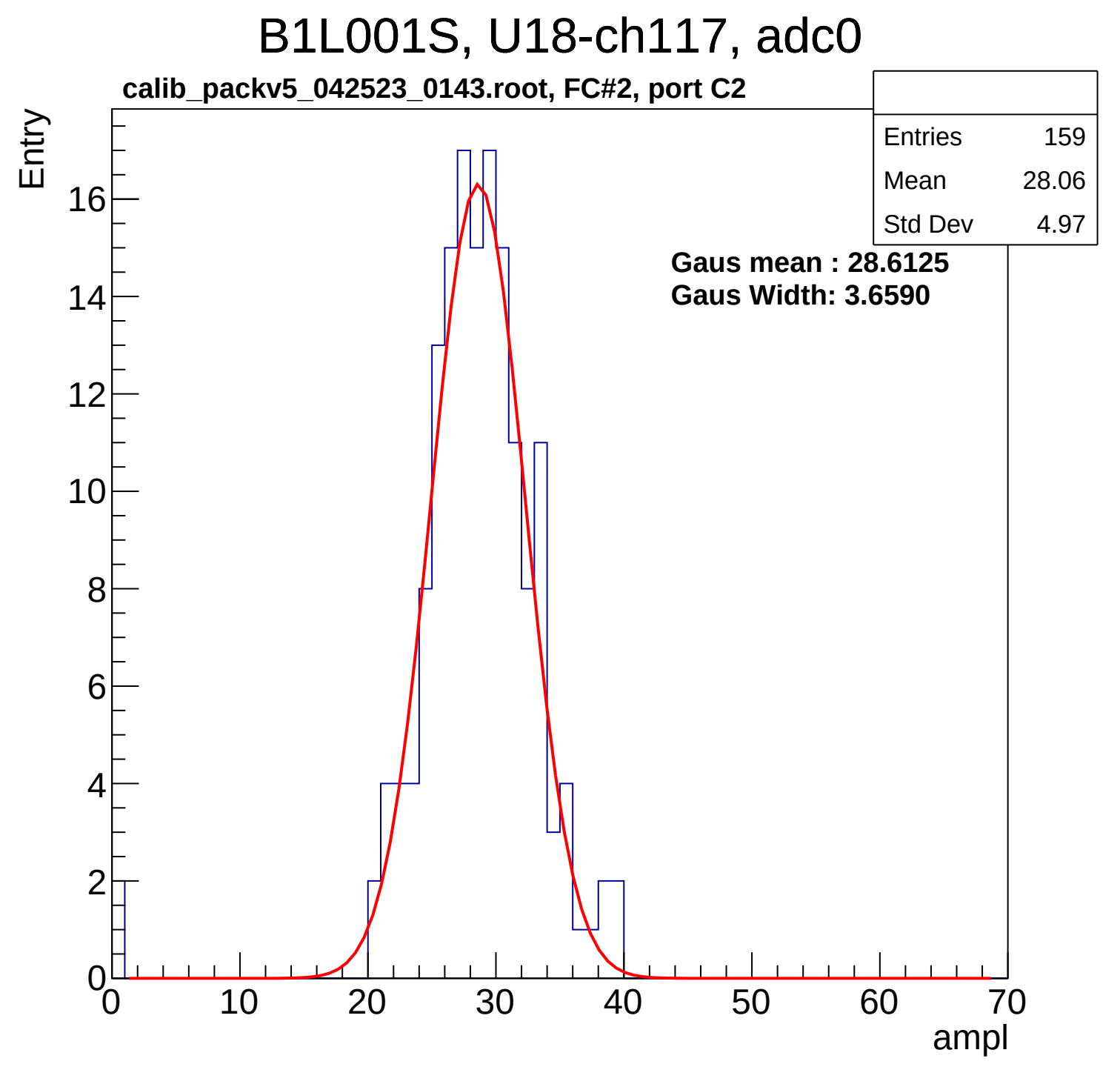

B1L001S, U18-ch116, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 124
Mean 47.44
Std Dev 3.246
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

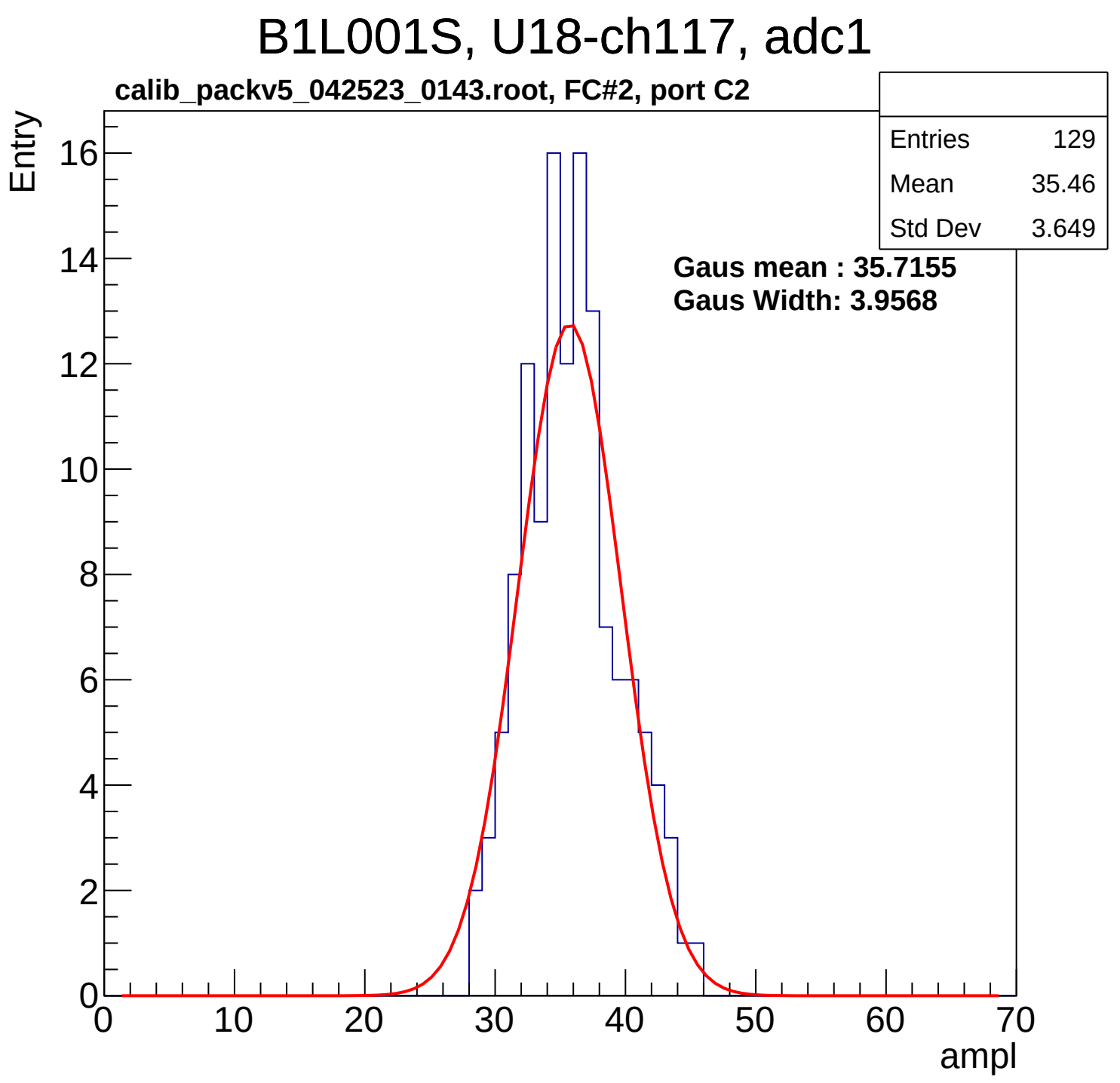

B1L001S, U18-ch116, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 125
Mean 53.39
Std Dev 3.462
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

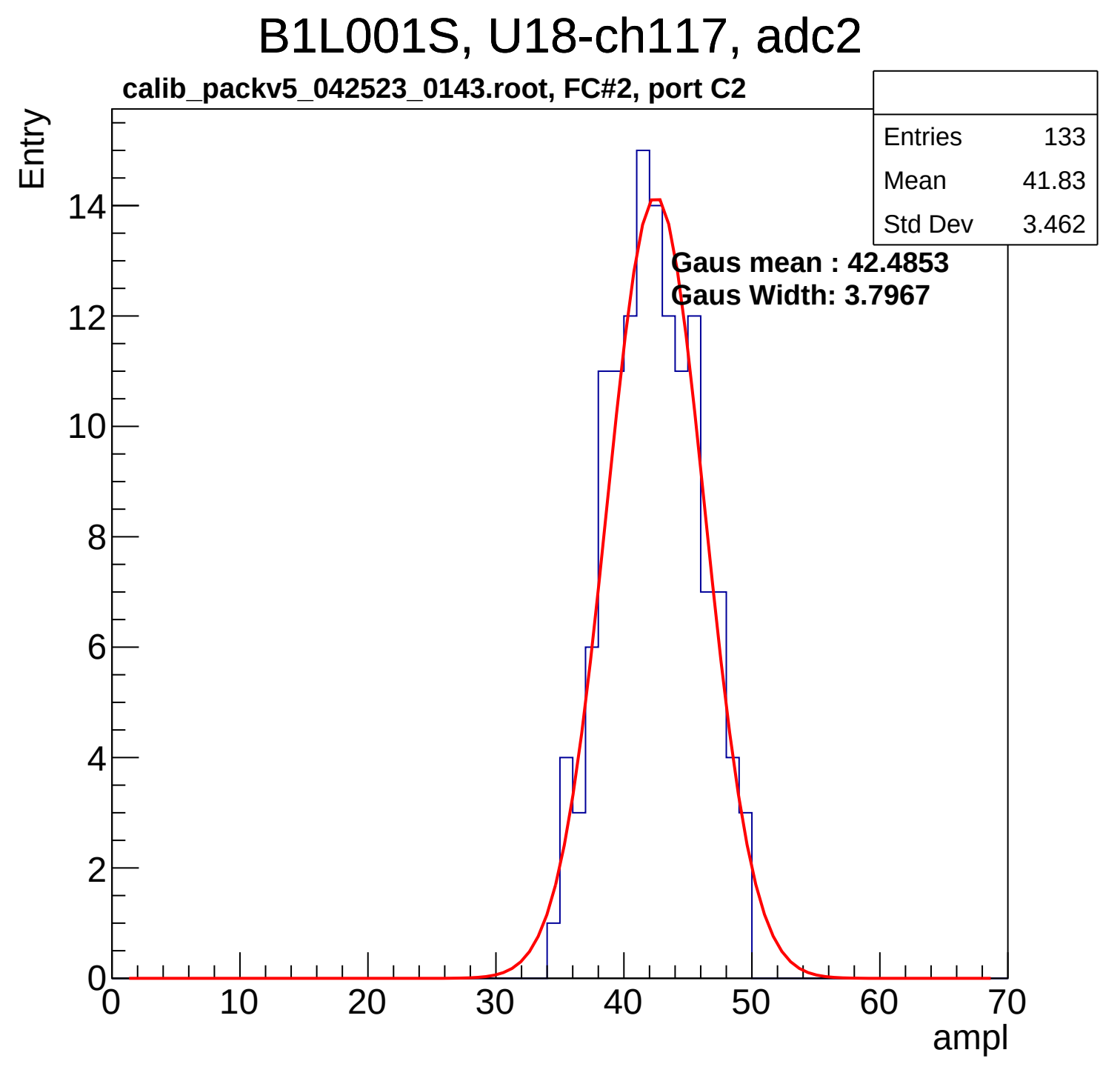

B1L001S, U18-ch116, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 124
Mean 58.17
Std Dev 7.914
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

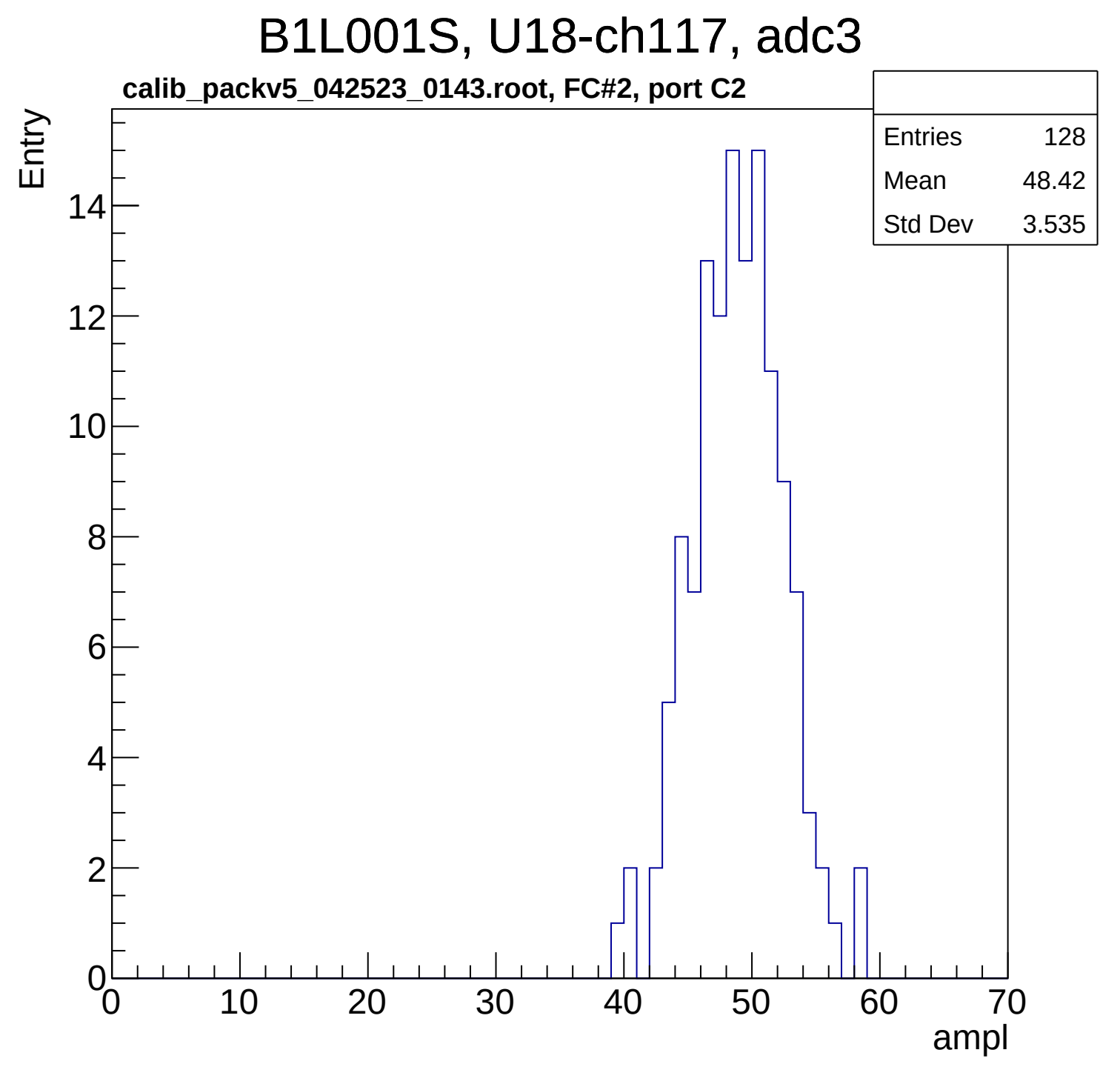

B1L001S, U18-ch116, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 16
Mean 62.12
Std Dev 0.7806
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl

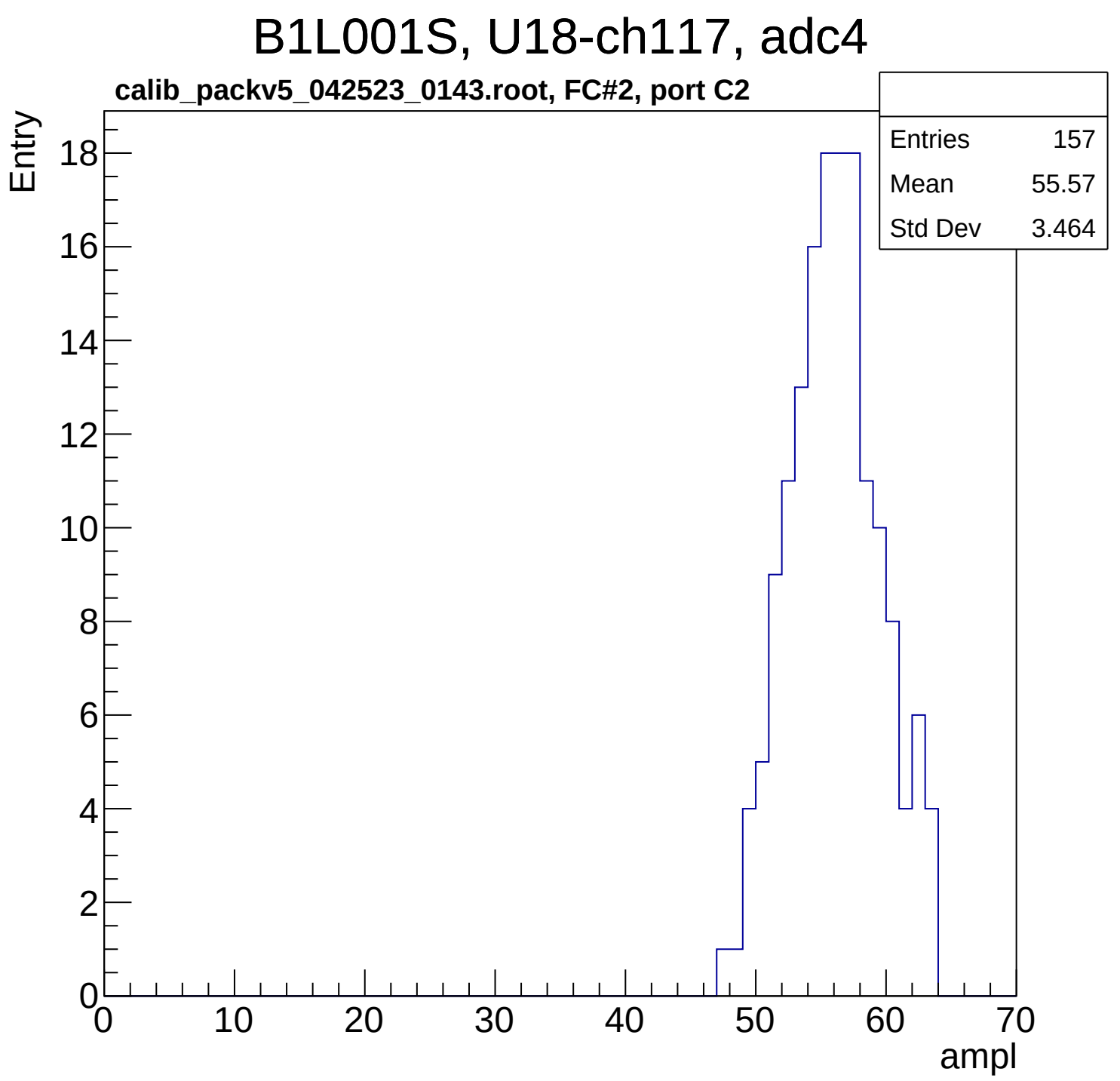

B1L001S, U18-ch116, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

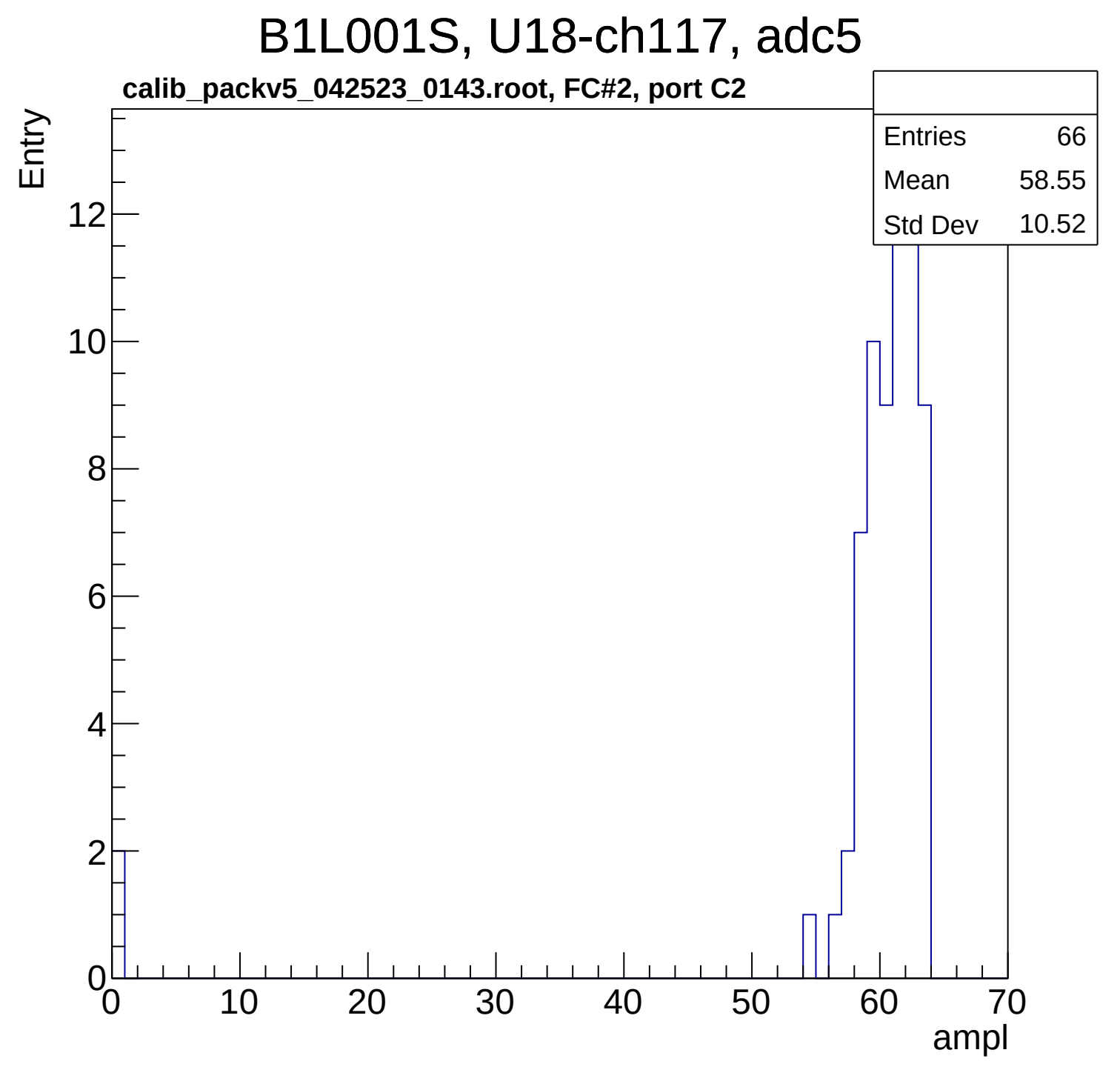

B1L001S, U18-ch117, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 159
Mean 28.06
Std Dev 4.97
Gaus mean : 28.6125
Gaus Width: 3.6590
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

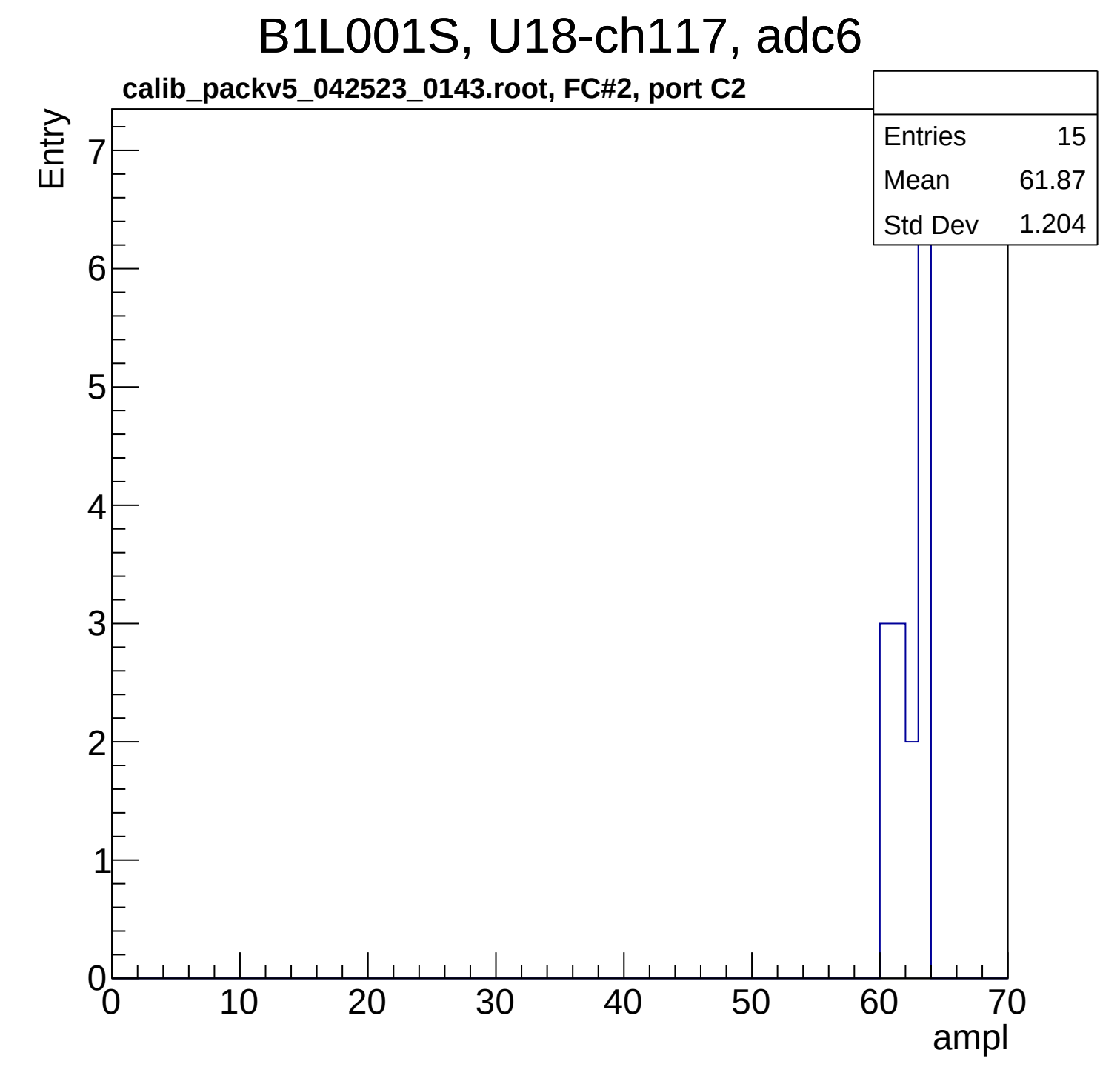

B1L001S, U18-ch117, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 129
Mean 35.46
Std Dev 3.649
Gaus mean : 35.7155
Gaus Width: 3.9568
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

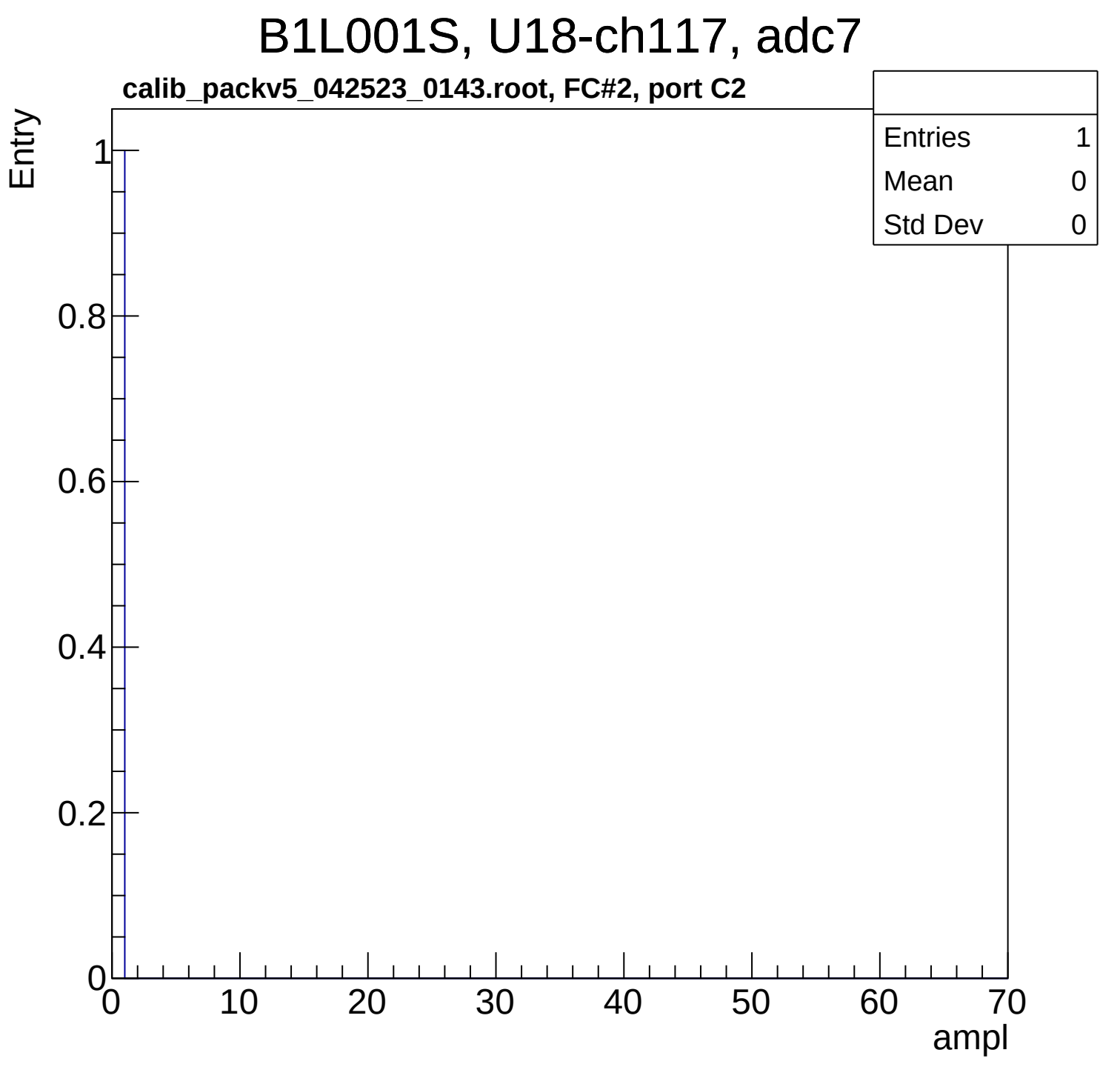

B1L001S, U18-ch117, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 133
Mean 41.83
Std Dev 3.462
Gaus mean : 42.4853
Gaus Width: 3.7967
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

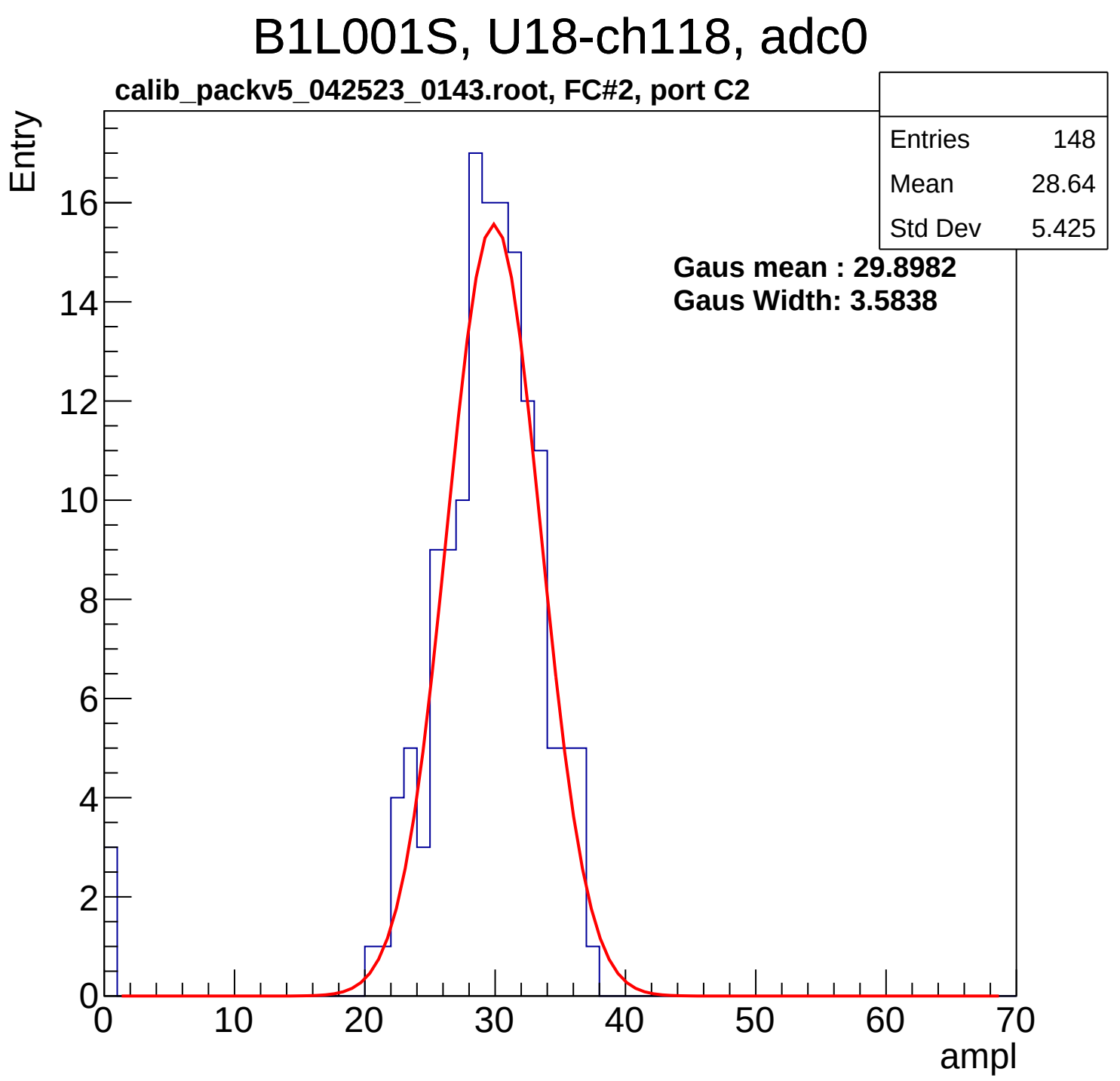

B1L001S, U18-ch117, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 128
Mean 48.42
Std Dev 3.535
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

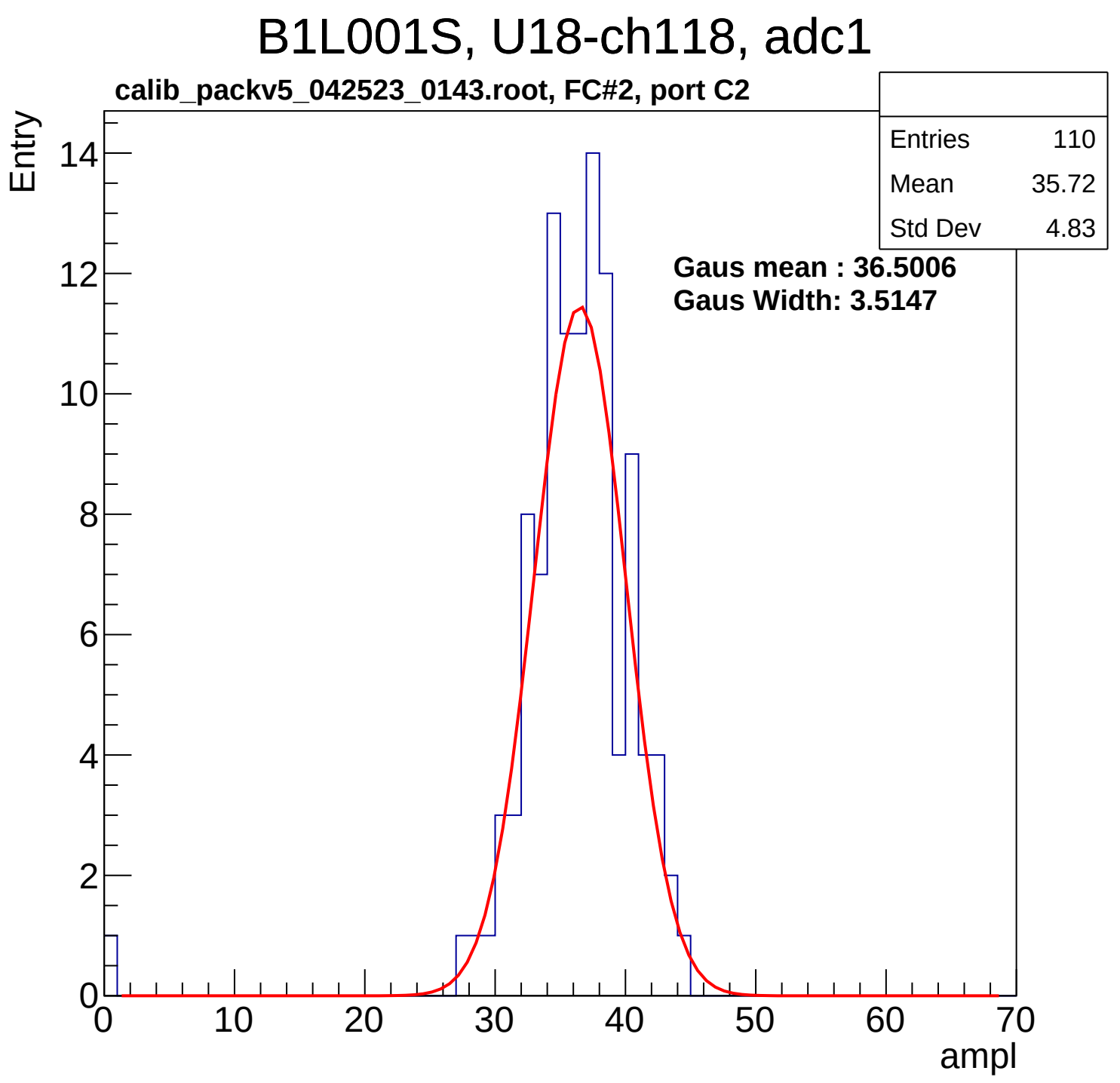

B1L001S, U18-ch117, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 157
Mean 55.57
Std Dev 3.464
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

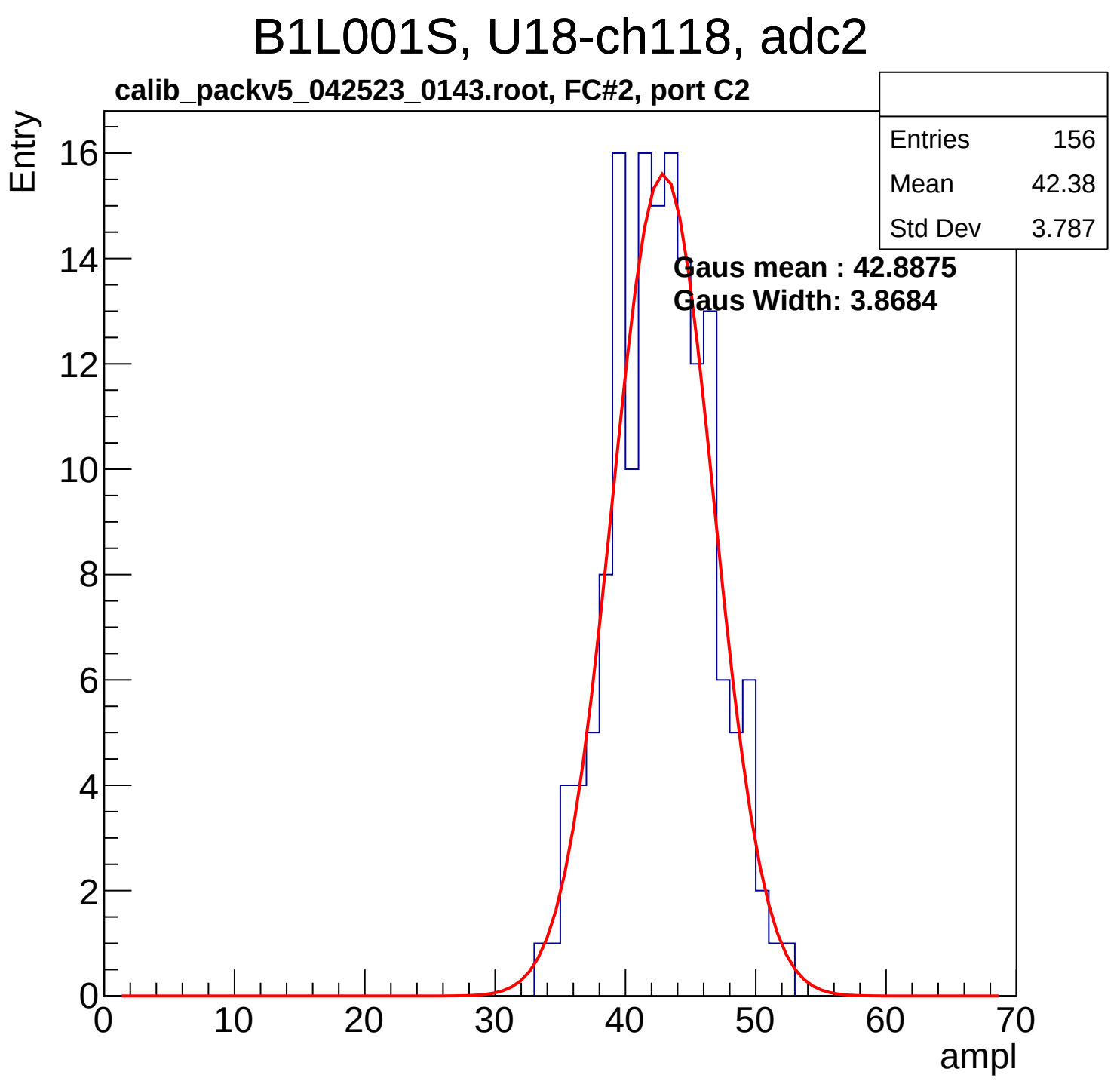

B1L001S, U18-ch117, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 66
Mean 58.55
Std Dev 10.52
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70

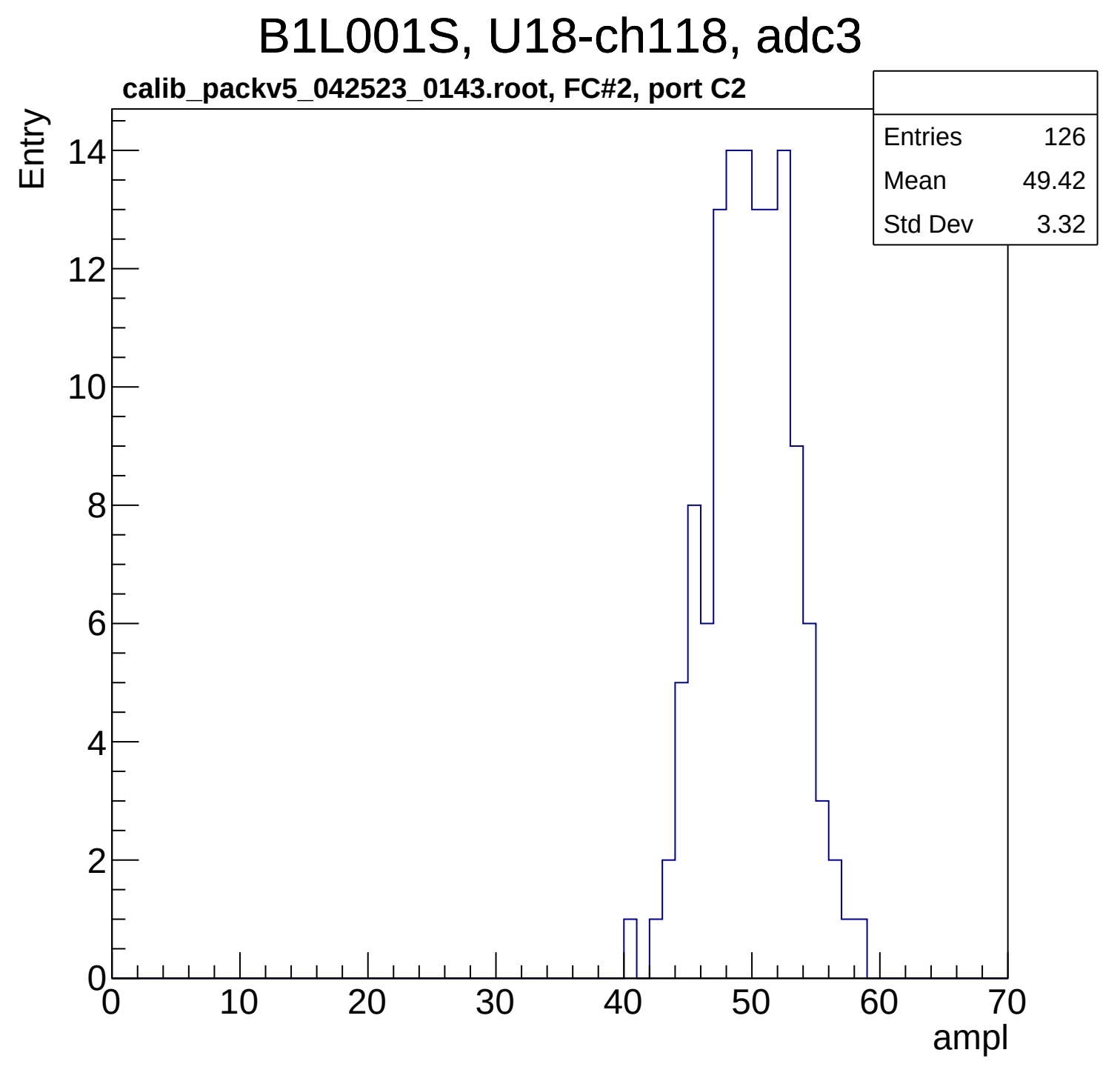

B1L001S, U18-ch117, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 15
Mean 61.87
Std Dev 1.204
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

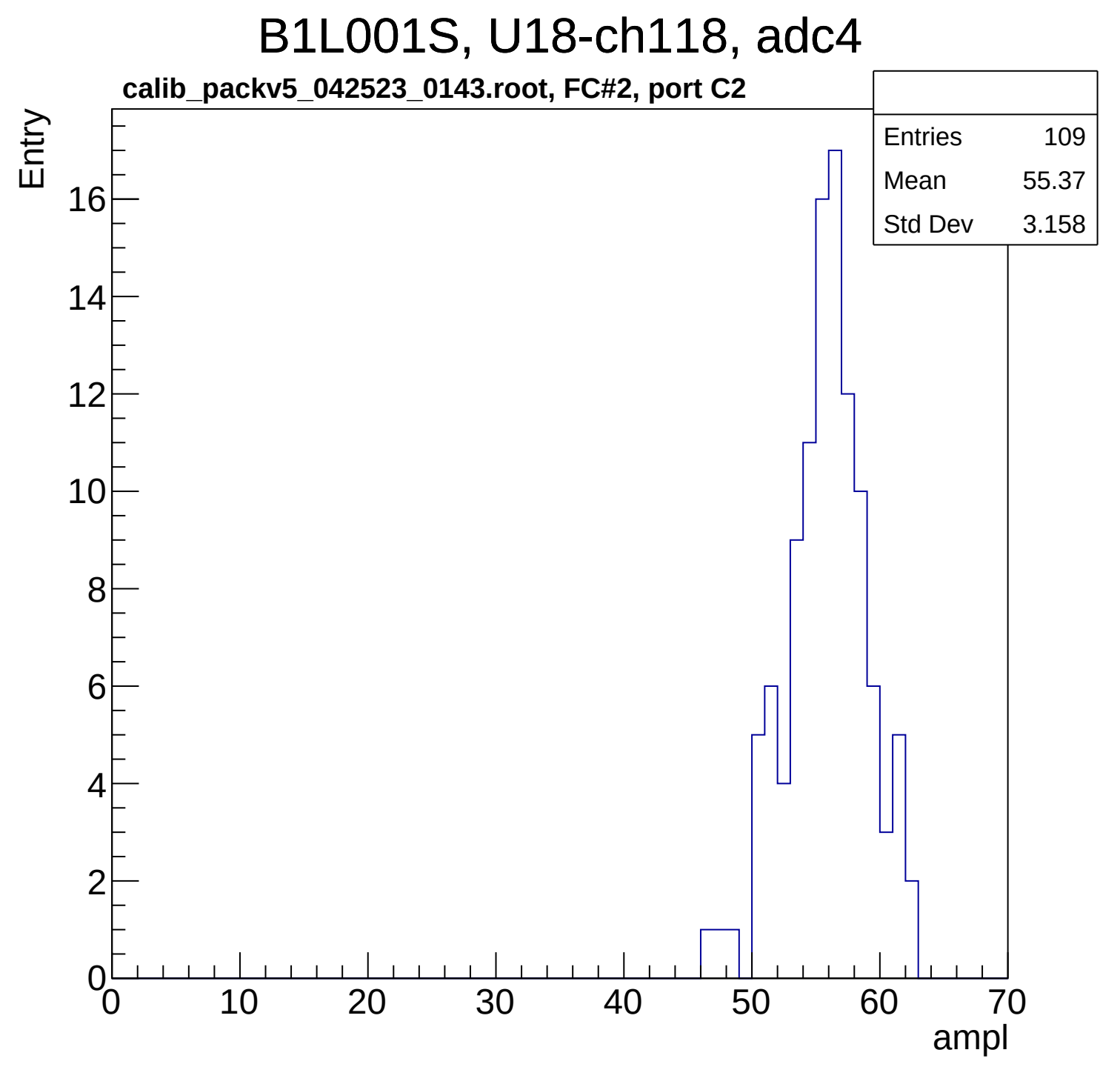

B1L001S, U18-ch117, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

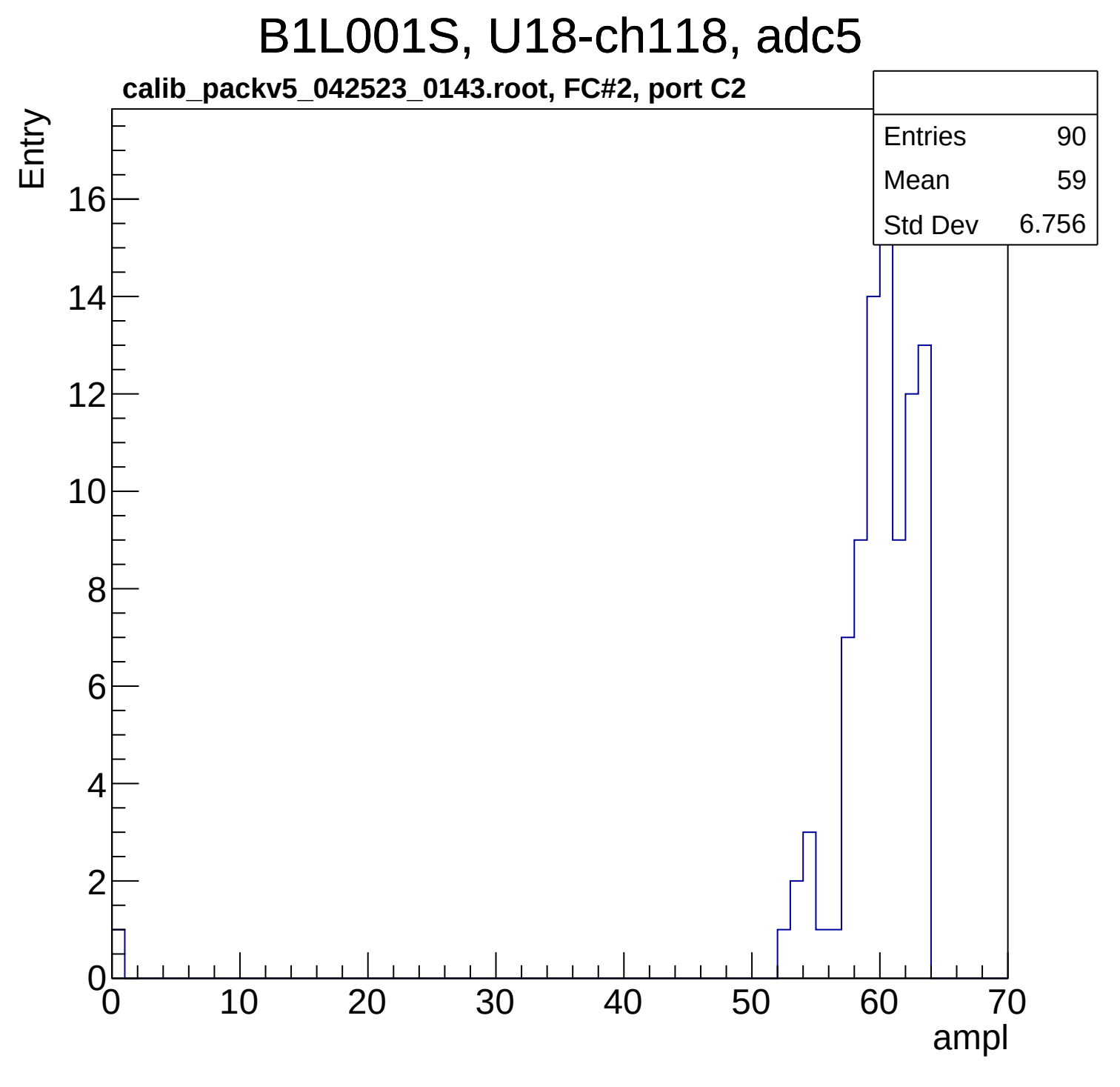

B1L001S, U18-ch118, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 148
Mean 28.64
Std Dev 5.425
Gaus mean : 29.8982
Gaus Width: 3.5838
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

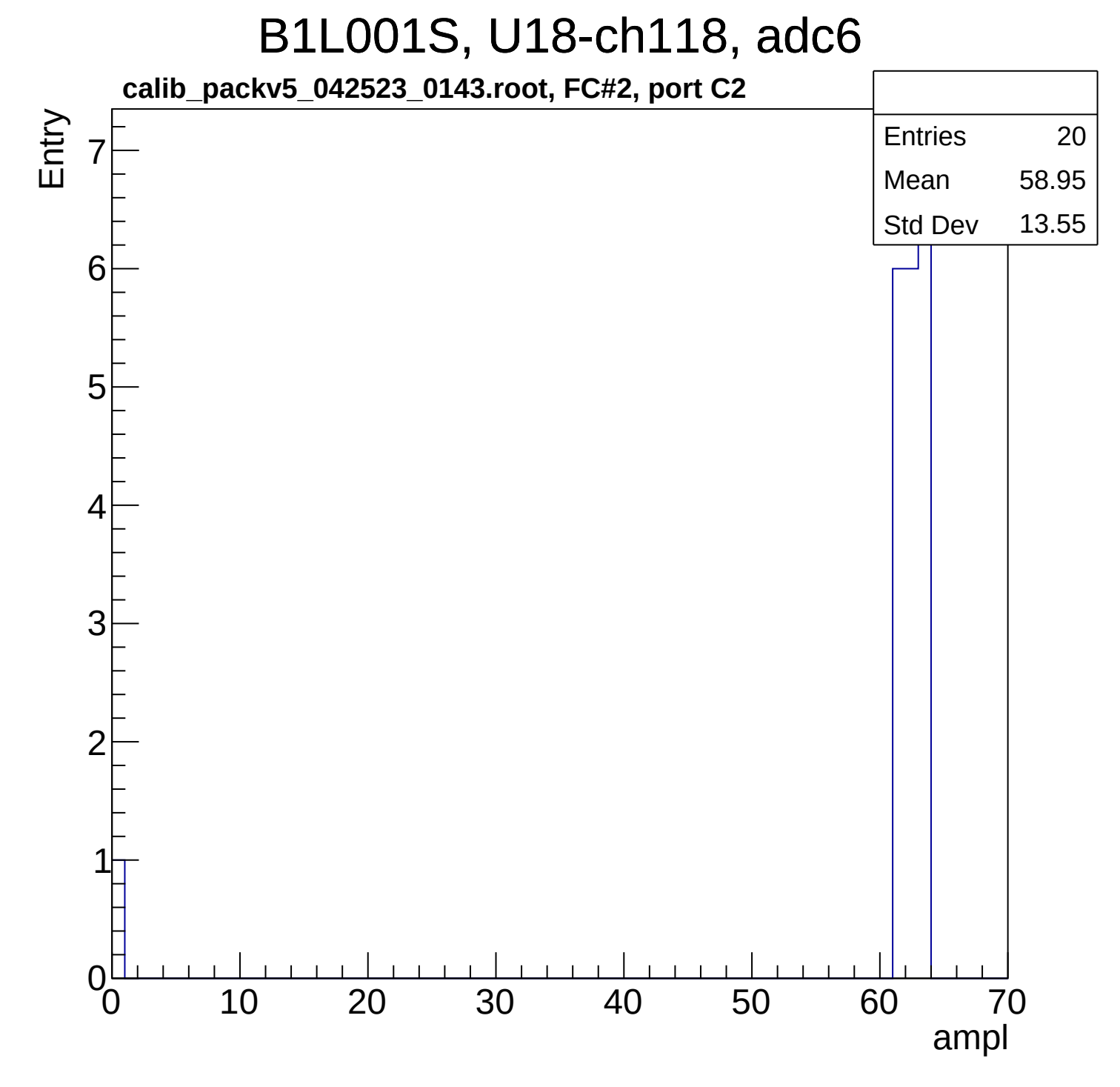

B1L001S, U18-ch118, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 110
Mean 35.72
Std Dev 4.83
Gaus mean : 36.5006
Gaus Width: 3.5147
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

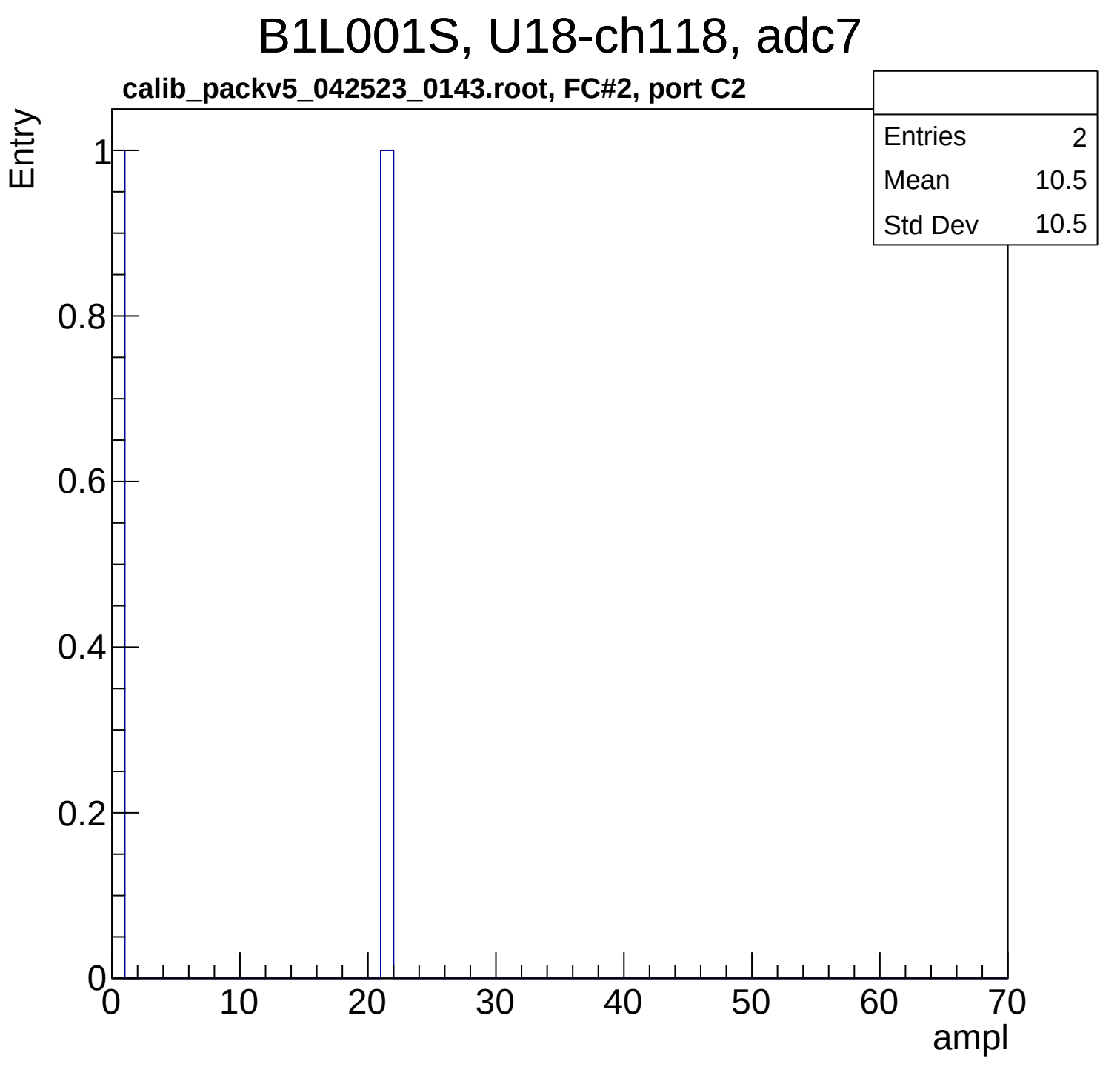

B1L001S, U18-ch118, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 156
Mean 42.38
Std Dev 3.787
Gaus mean : 42.8875
Gaus Width: 3.8684
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

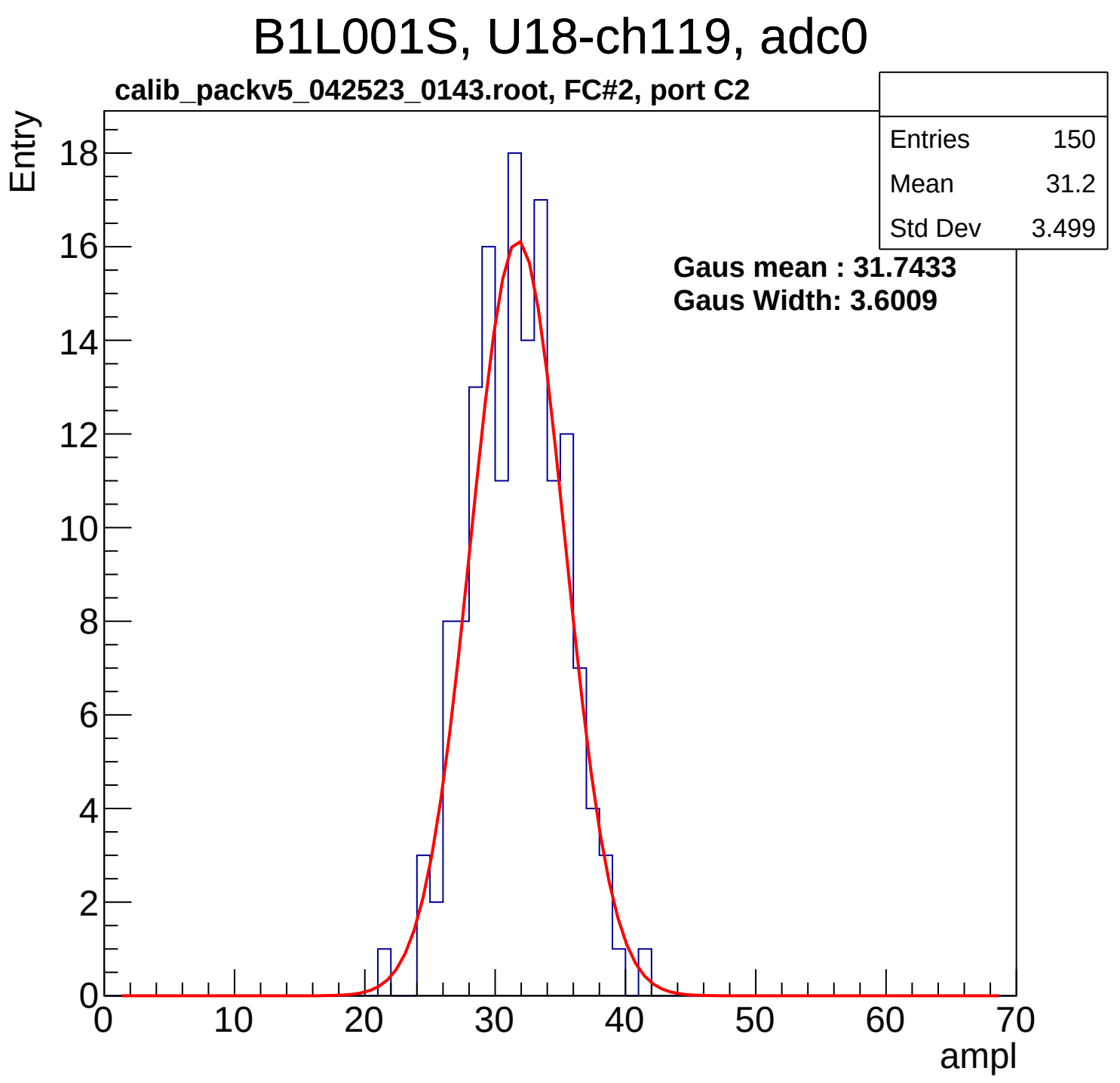

B1L001S, U18-ch118, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 126
Mean 49.42
Std Dev 3.32
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

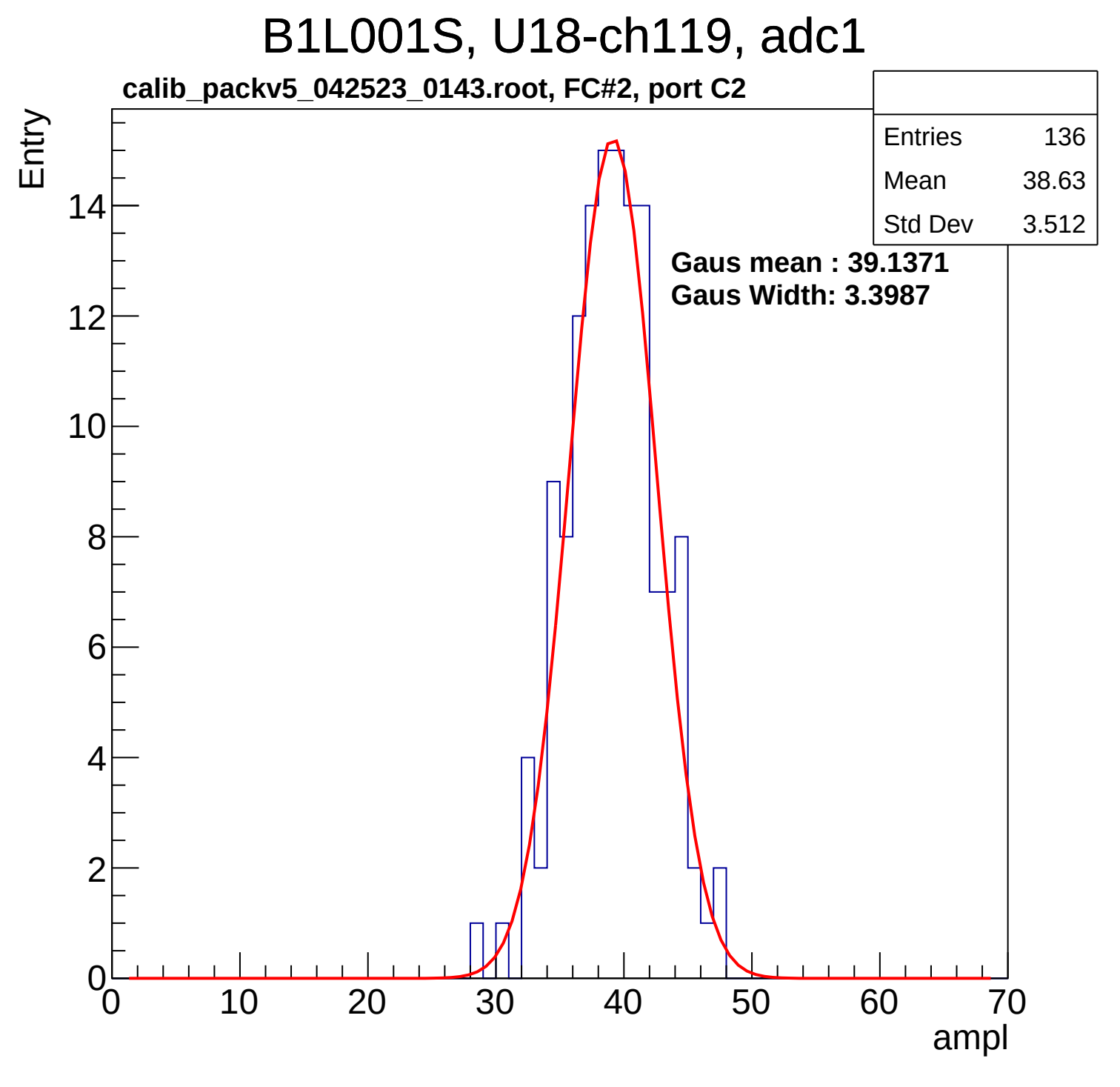

B1L001S, U18-ch118, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 109
Mean 55.37
Std Dev 3.158
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

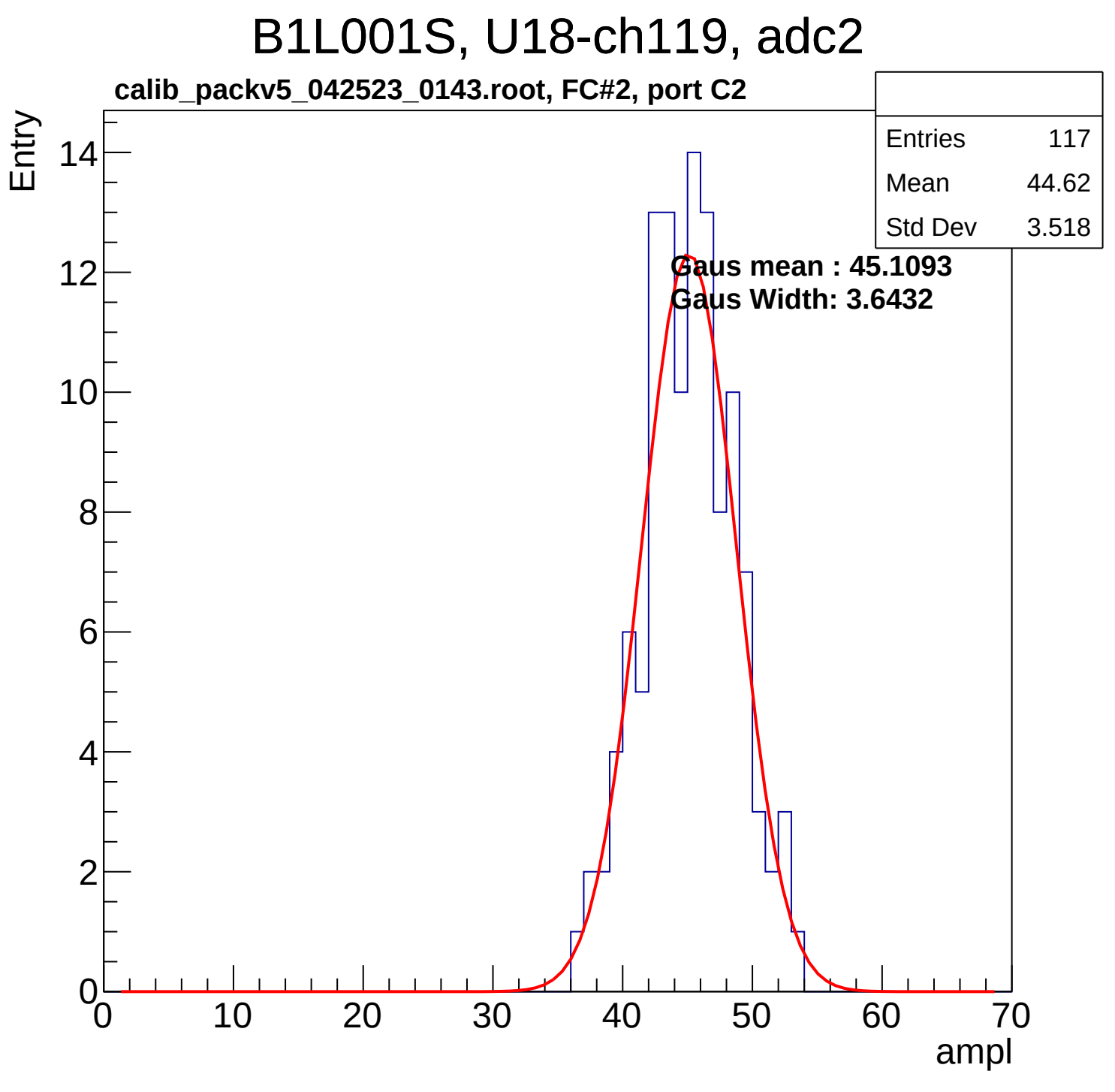

B1L001S, U18-ch118, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 90
Mean 59
Std Dev 6.756
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

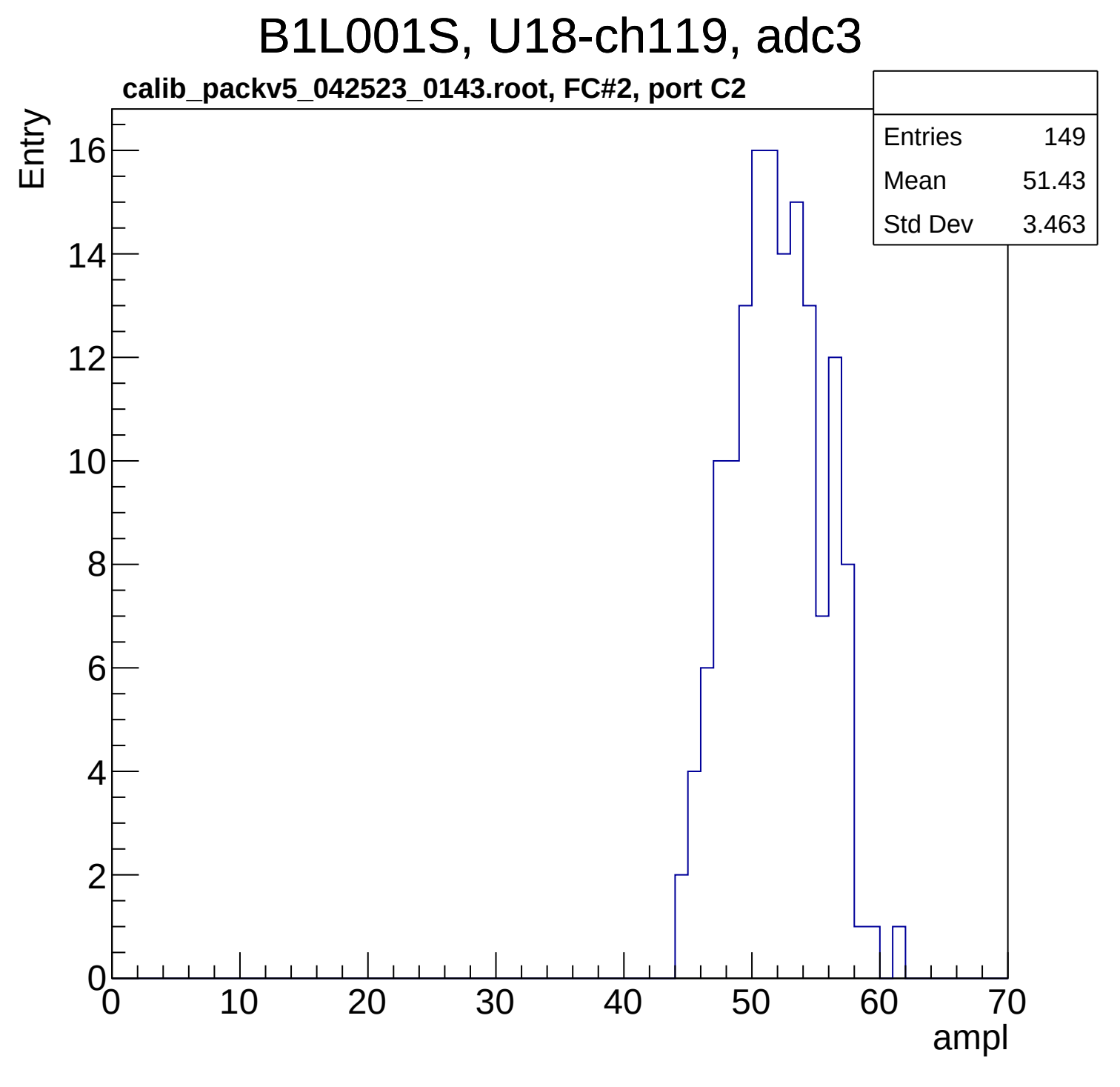

B1L001S, U18-ch118, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 20
Mean 58.95
Std Dev 13.55
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

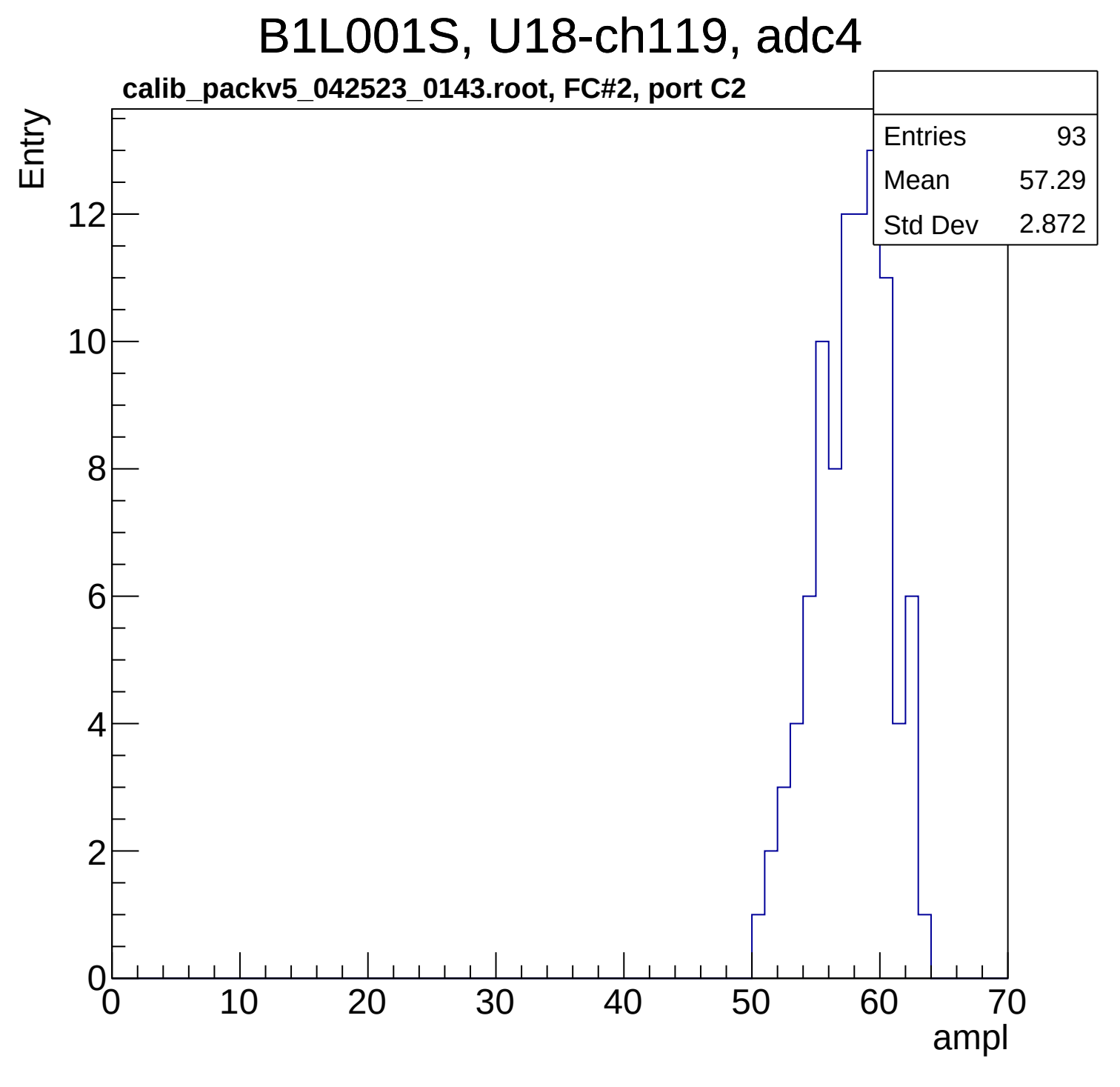

B1L001S, U18-ch118, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 10.5
Std Dev 10.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

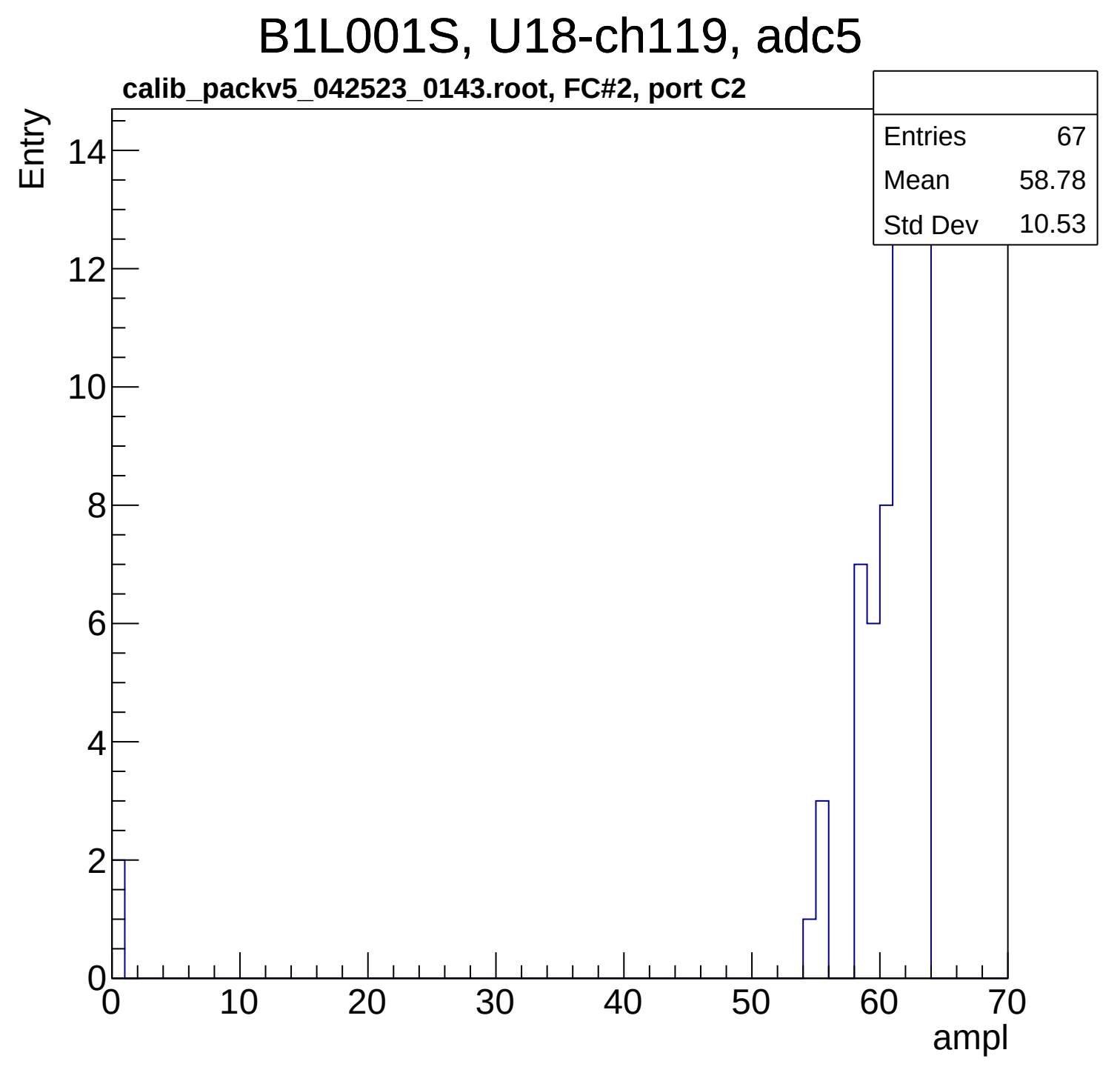

B1L001S, U18-ch119, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 150
Mean 31.2
Std Dev 3.499
Gaus mean : 31.7433
Gaus Width: 3.6009
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

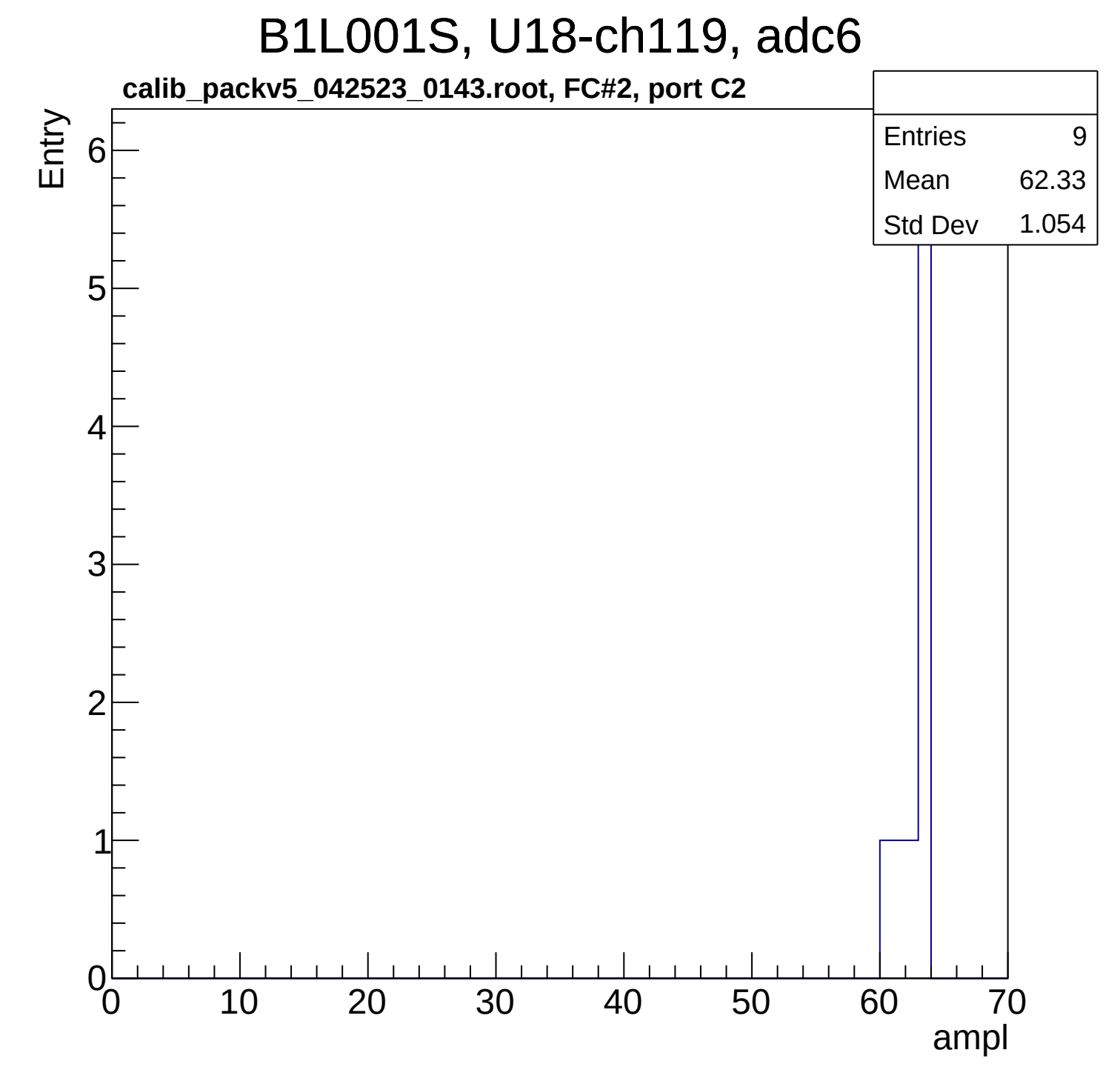

B1L001S, U18-ch119, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 136
Mean 38.63
Std Dev 3.512
Gaus mean : 39.1371
Gaus Width: 3.3987
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

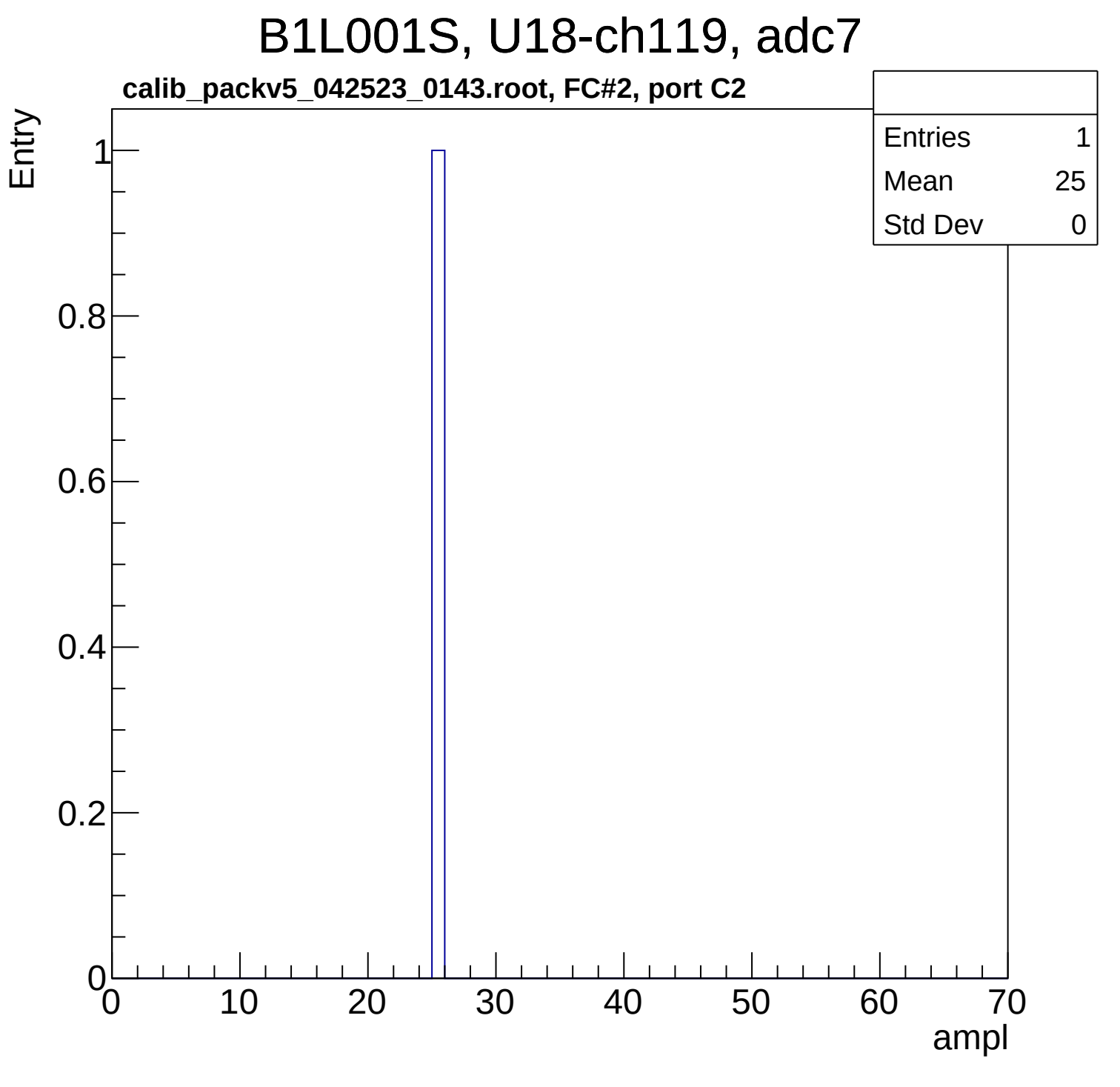

B1L001S, U18-ch119, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 117
Mean 44.62
Std Dev 3.518
Gaus mean : 45.1093
Gaus Width: 3.6432
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

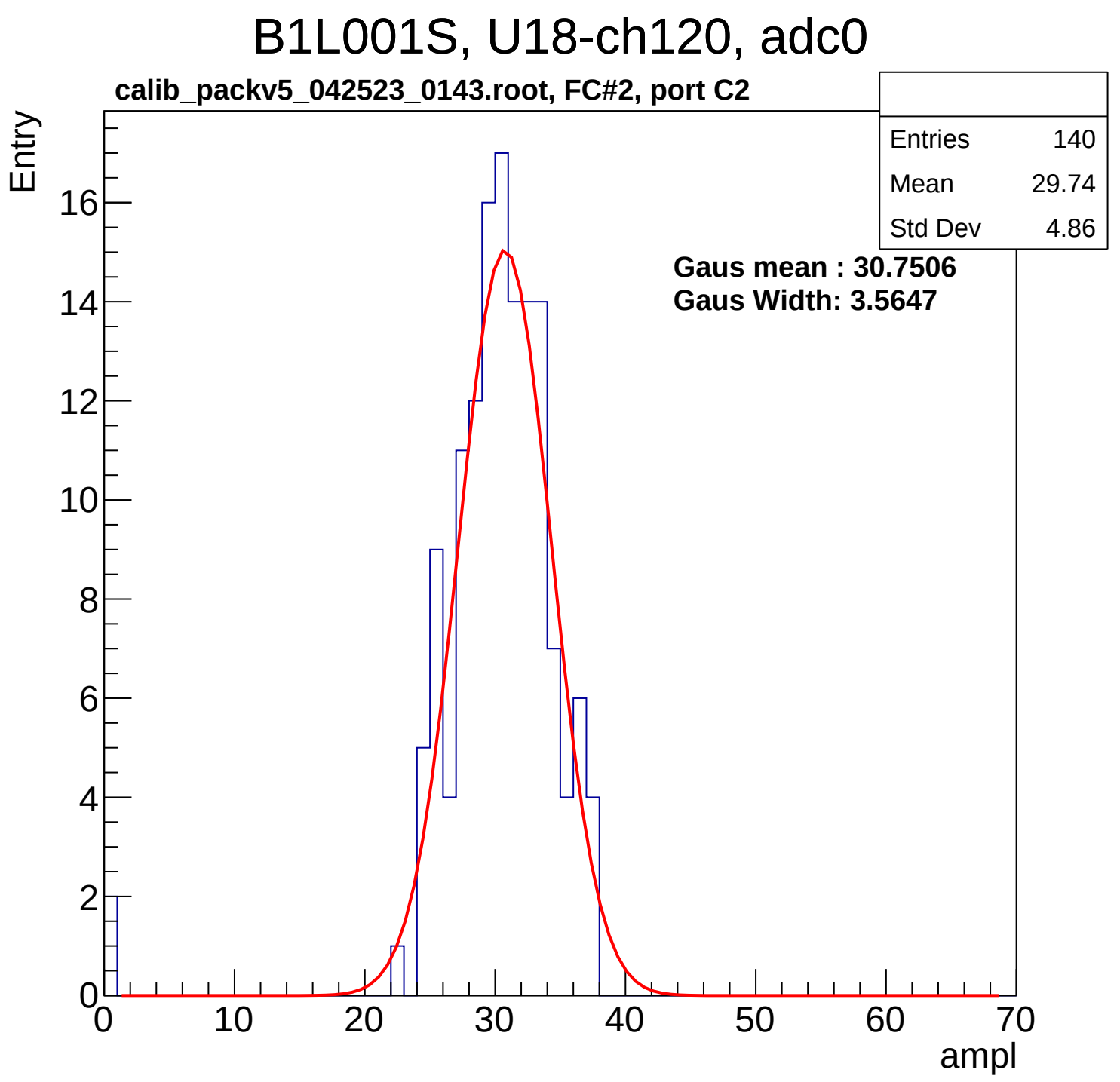

B1L001S, U18-ch119, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 149
Mean 51.43
Std Dev 3.463
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

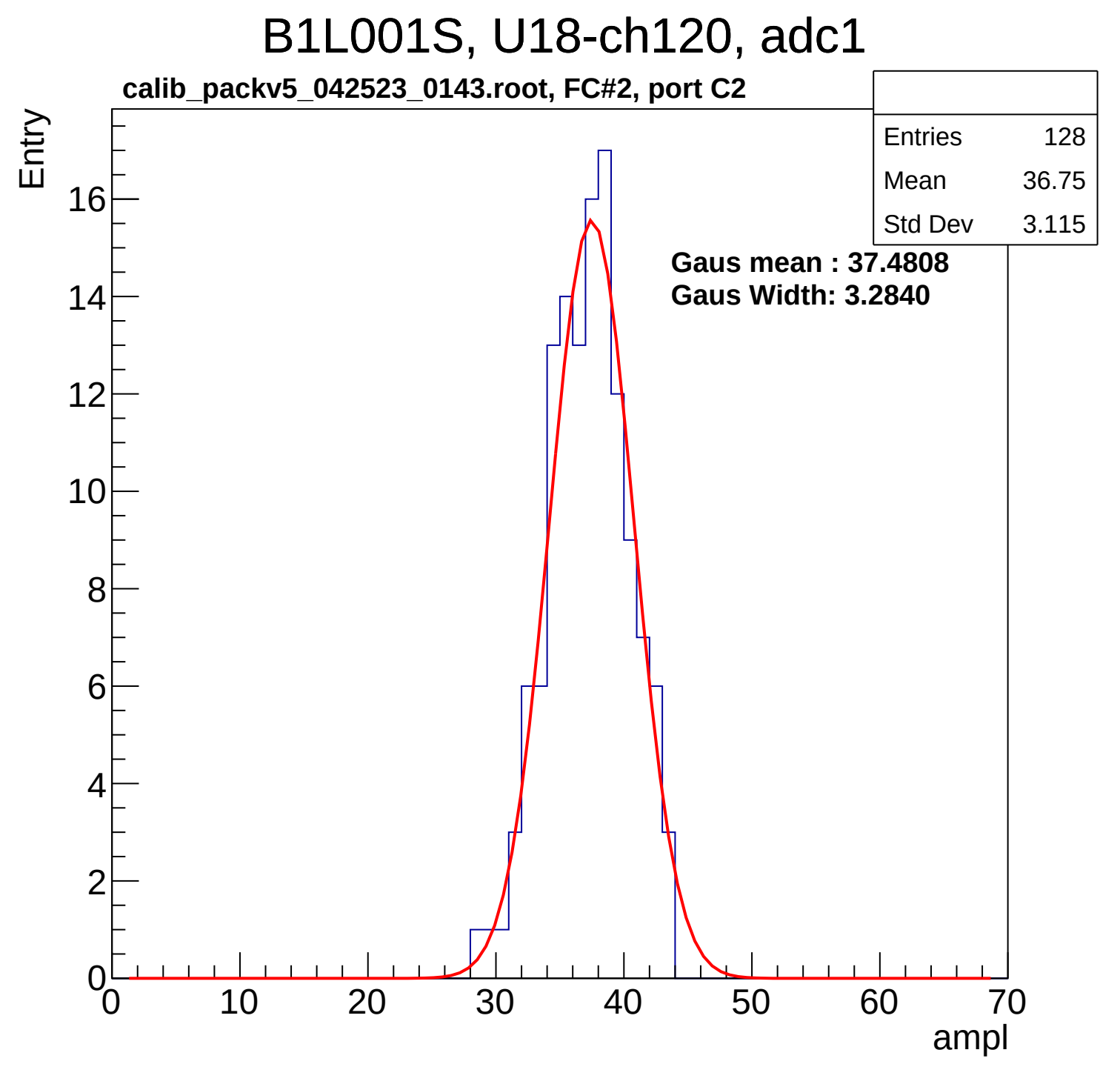

B1L001S, U18-ch119, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 93
Mean 57.29
Std Dev 2.872
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70

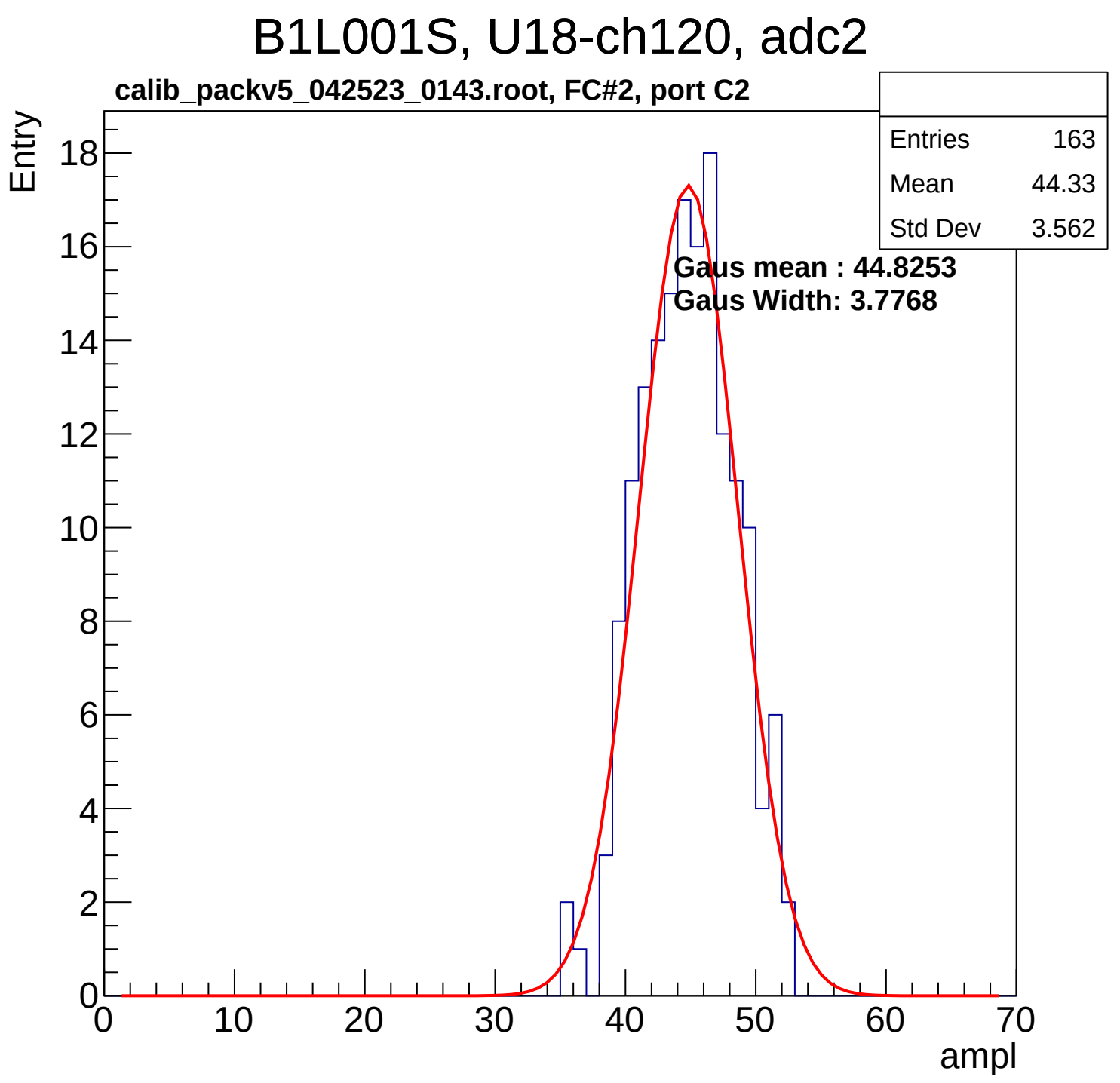

B1L001S, U18-ch119, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 67
Mean 58.78
Std Dev 10.53
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

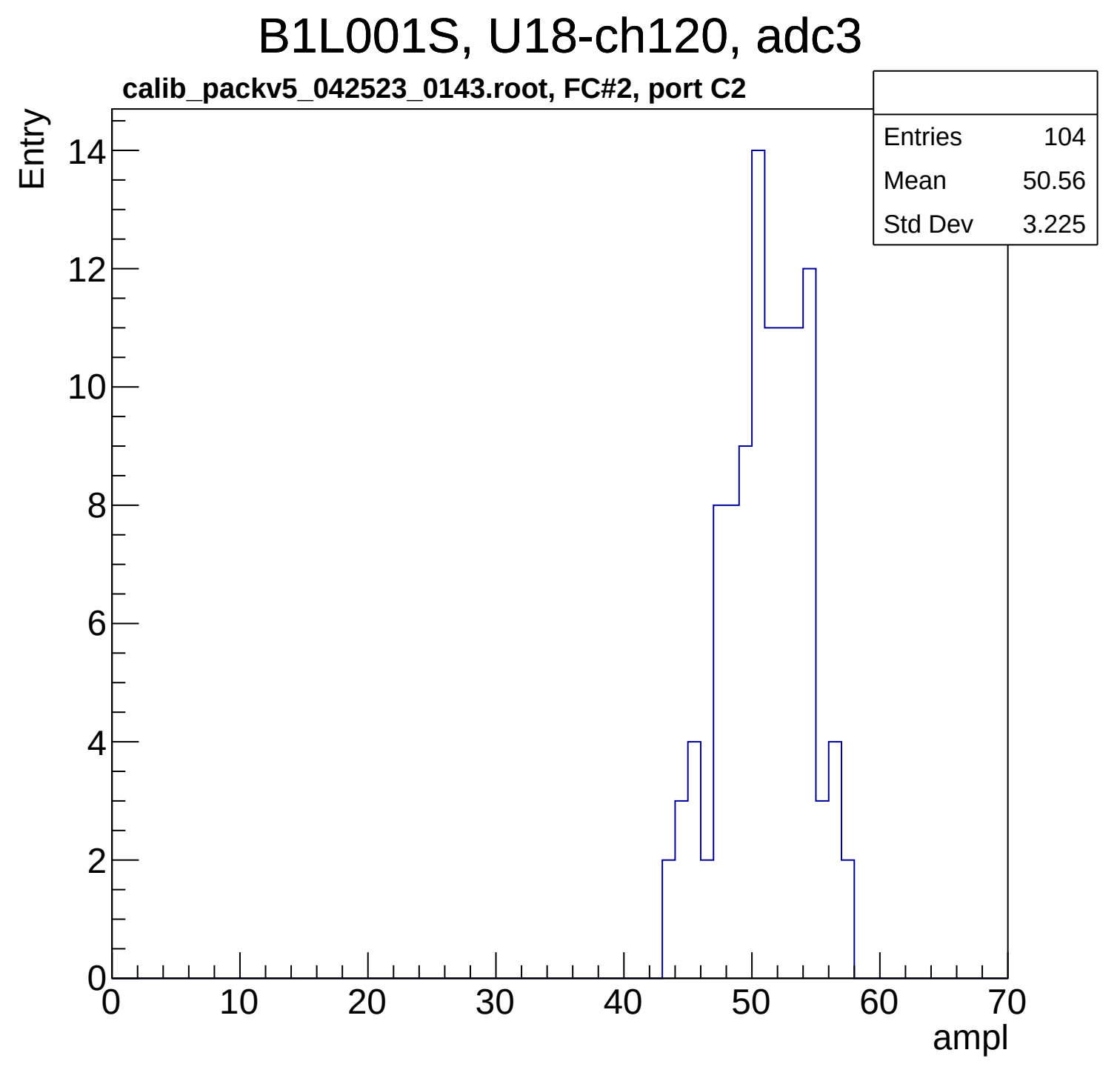

B1L001S, U18-ch119, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 9
Mean 62.33
Std Dev 1.054
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl

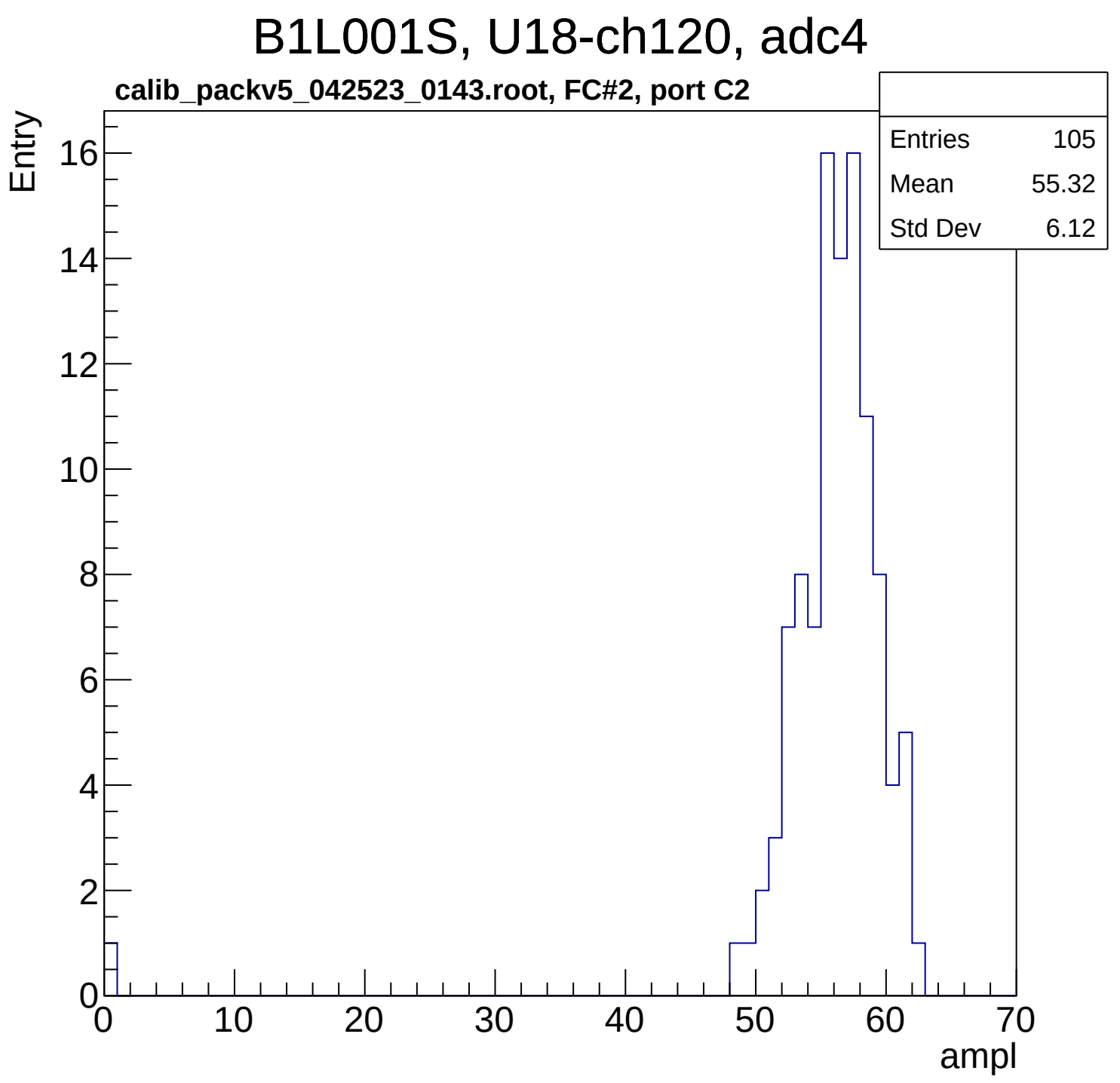

B1L001S, U18-ch119, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 25
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

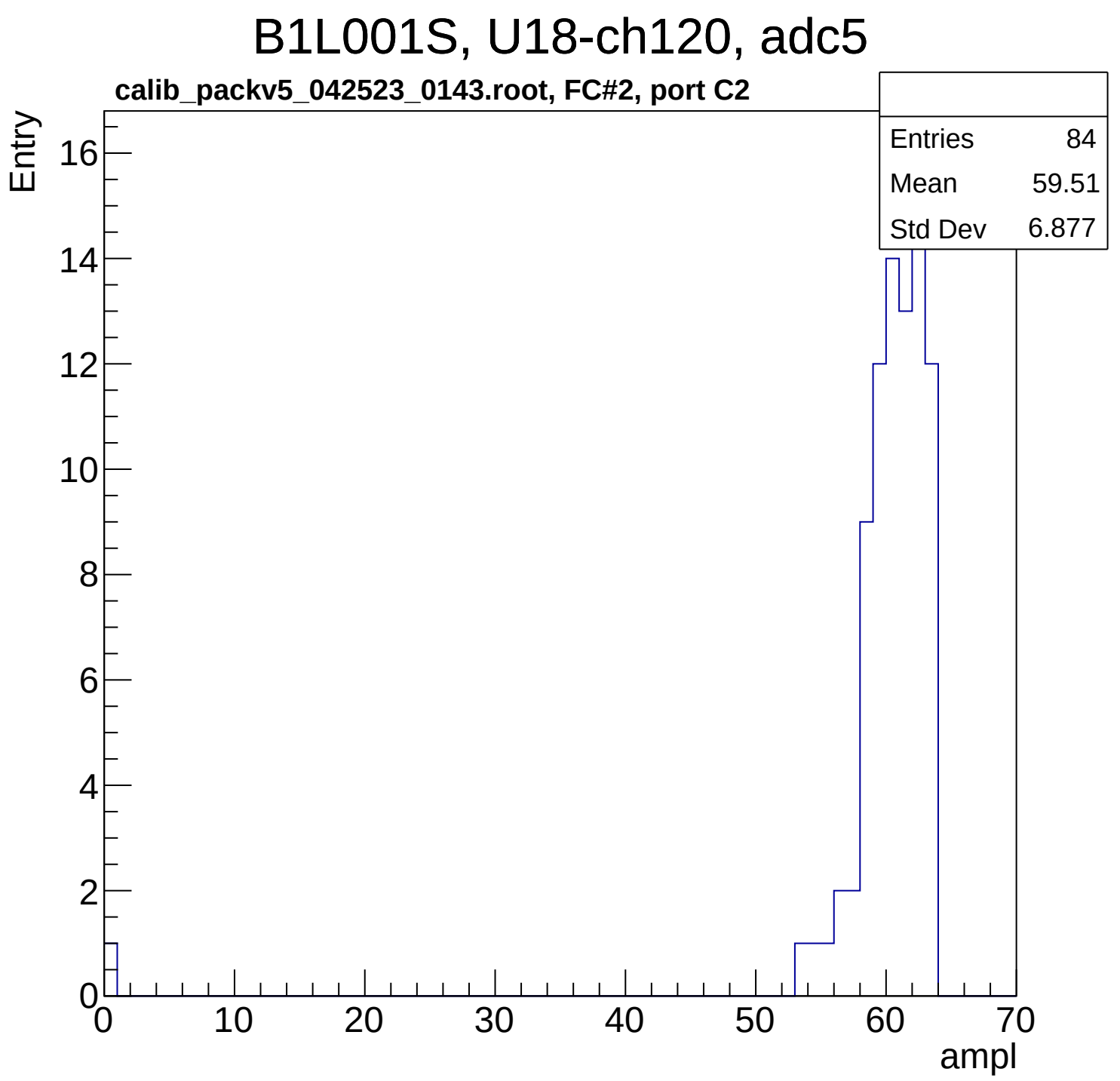

B1L001S, U18-ch120, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 140
Mean 29.74
Std Dev 4.86
Gaus mean : 30.7506
Gaus Width: 3.5647
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

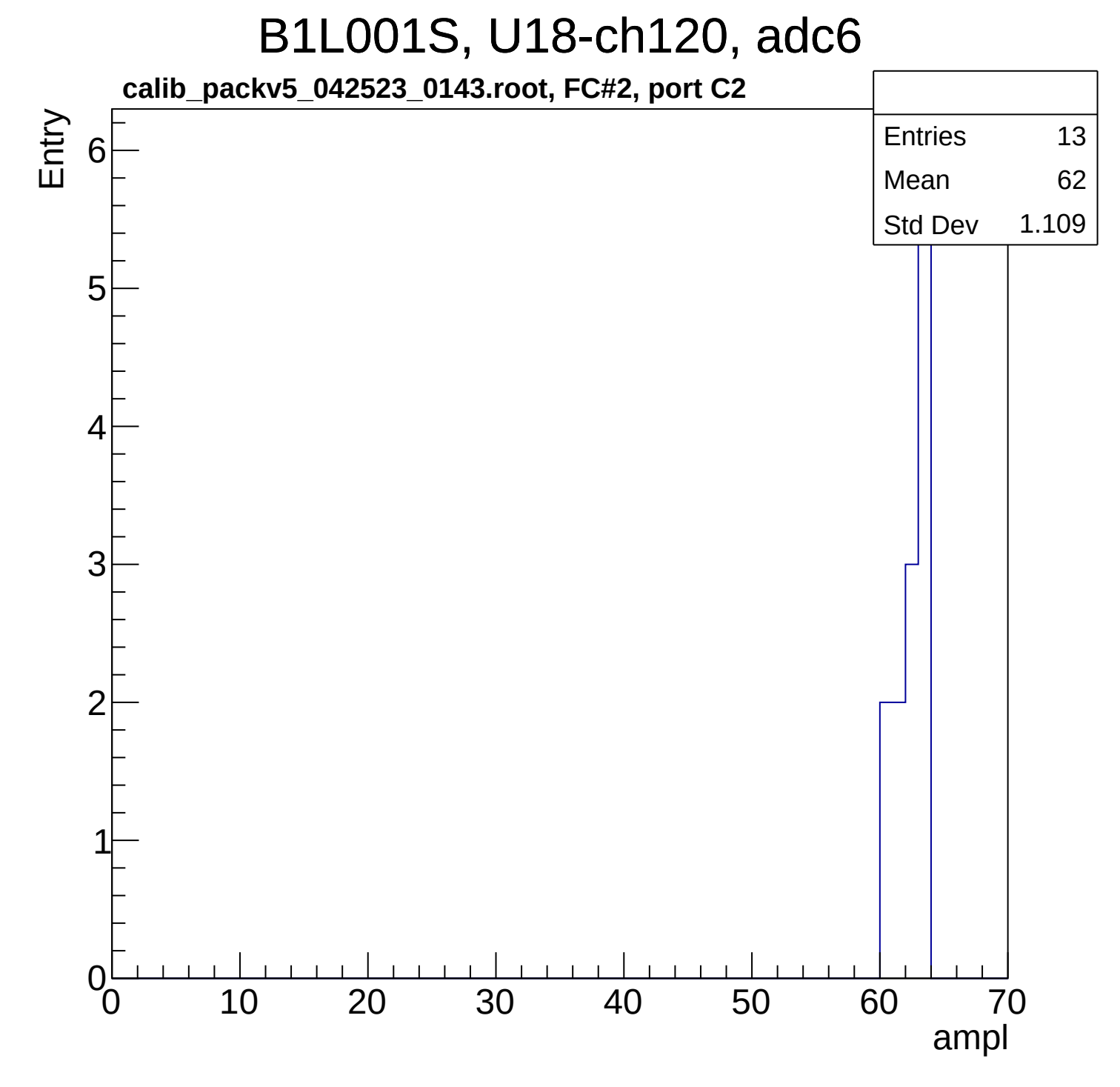

B1L001S, U18-ch120, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 128
Mean 36.75
Std Dev 3.115
Gaus mean : 37.4808
Gaus Width: 3.2840
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

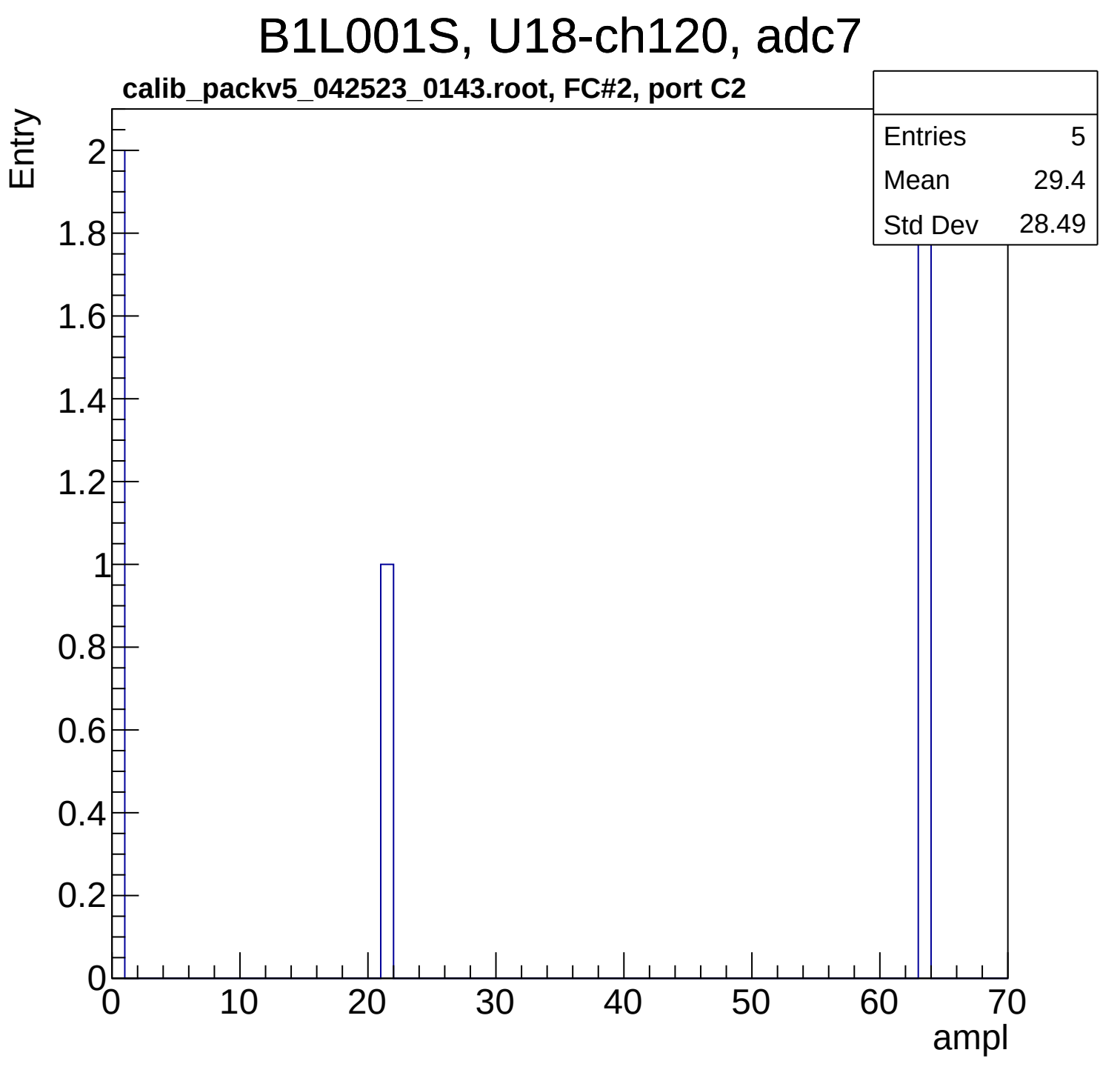

B1L001S, U18-ch120, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 163
Mean 44.33
Std Dev 3.562
Gaus mean : 44.8253
Gaus Width: 3.7768
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

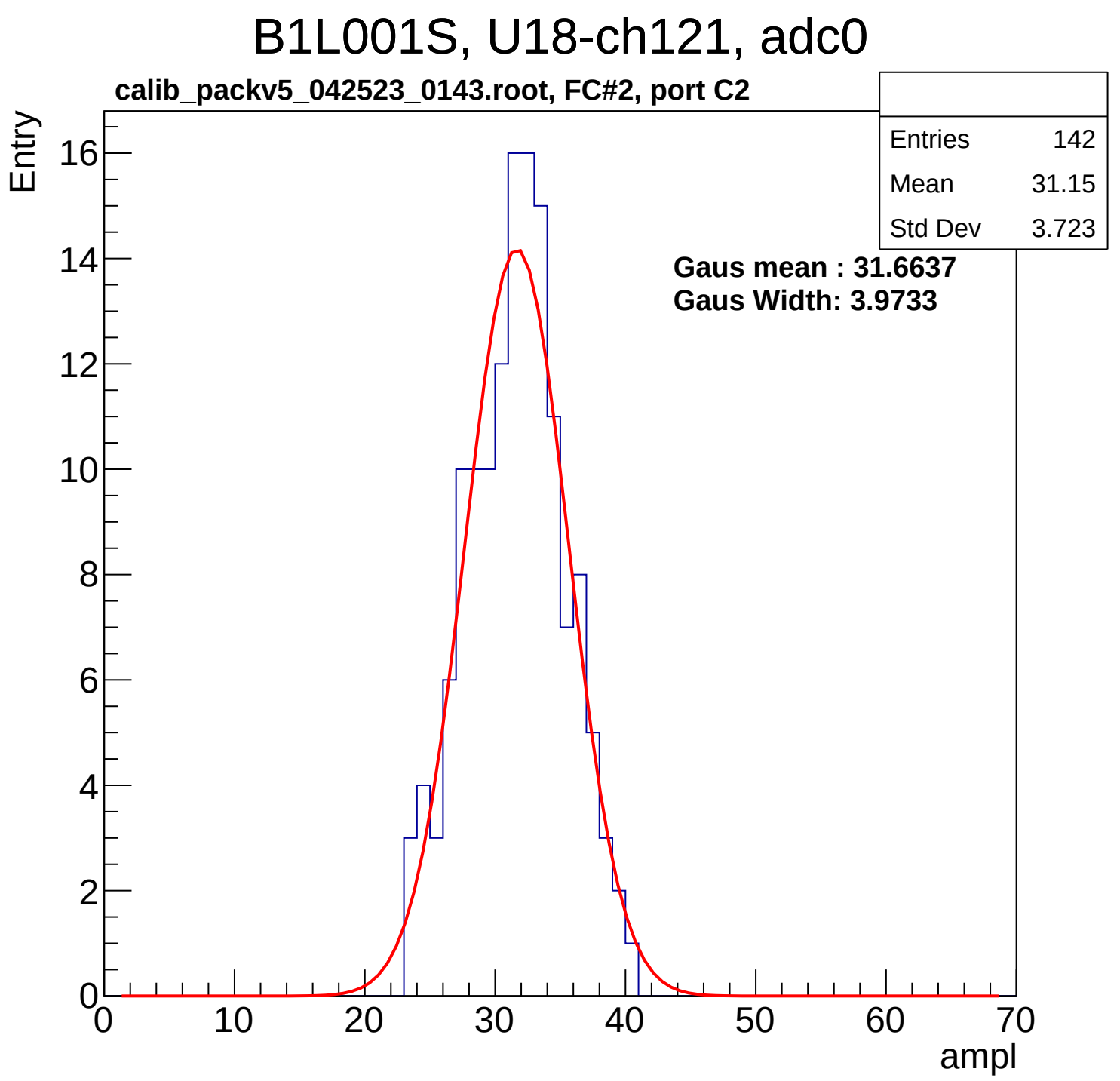

B1L001S, U18-ch120, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 104
Mean 50.56
Std Dev 3.225
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

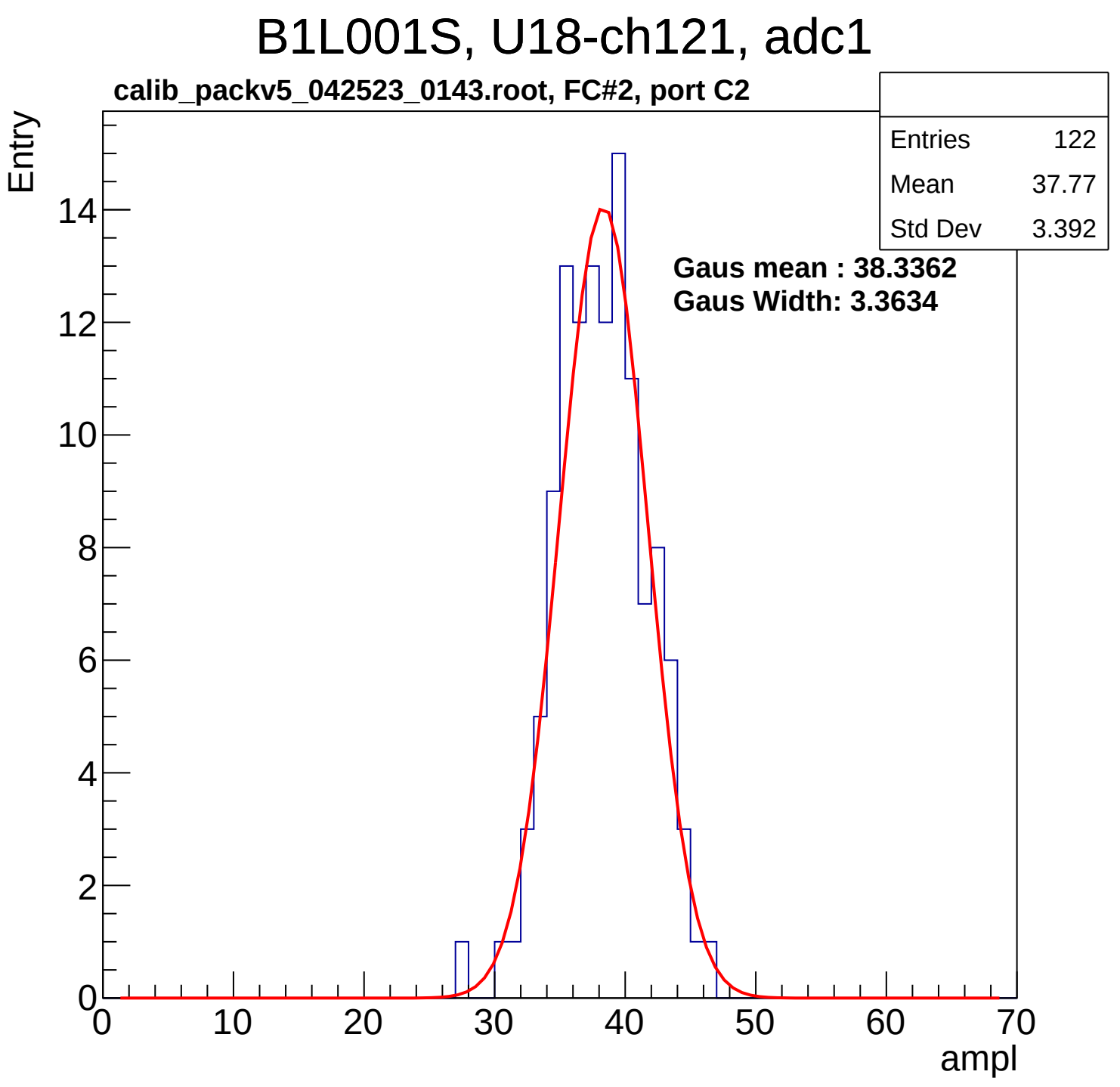

B1L001S, U18-ch120, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 105
Mean 55.32
Std Dev 6.12
Entry
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl

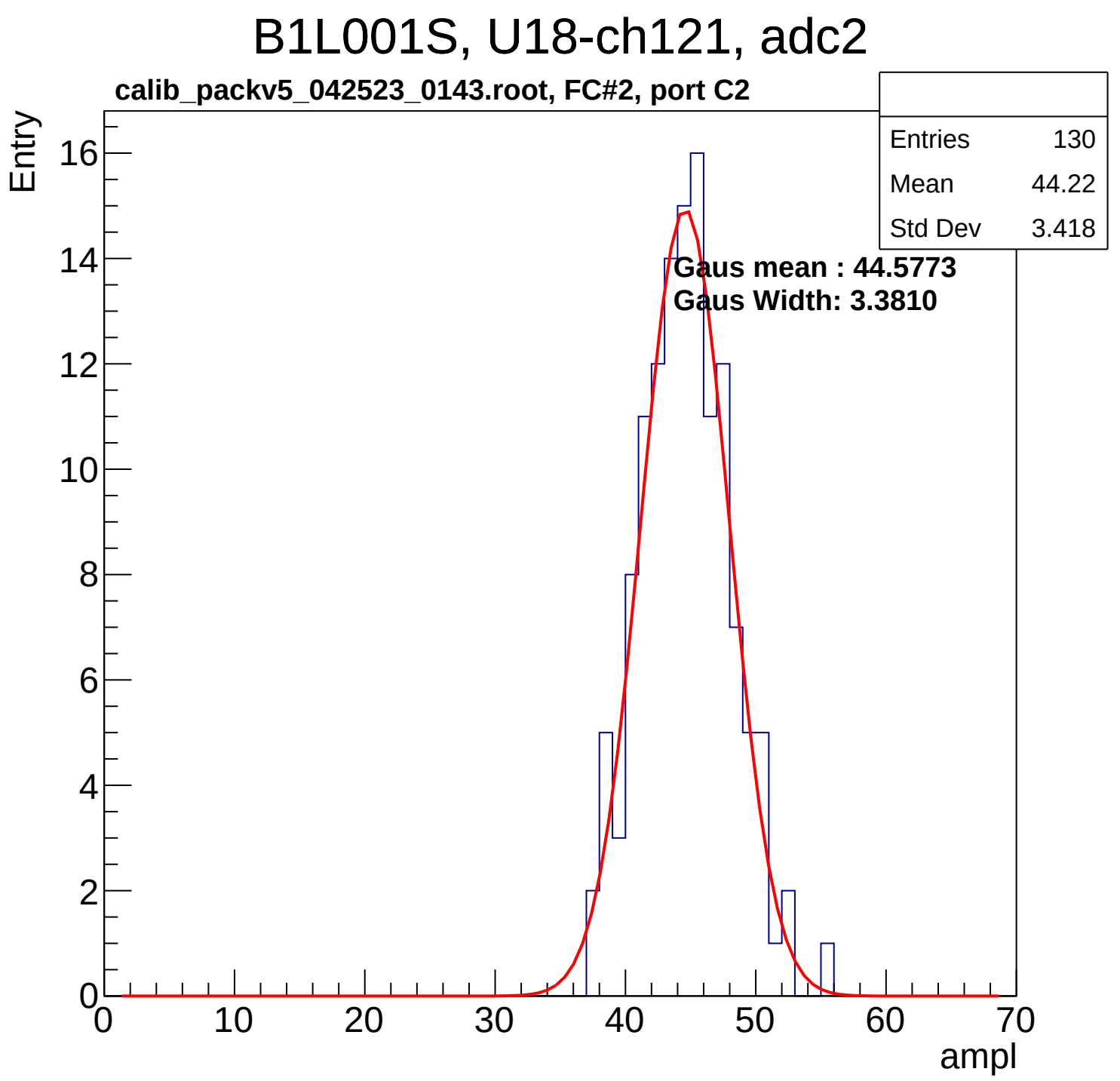

B1L001S, U18-ch120, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 84
Mean 59.51
Std Dev 6.877
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

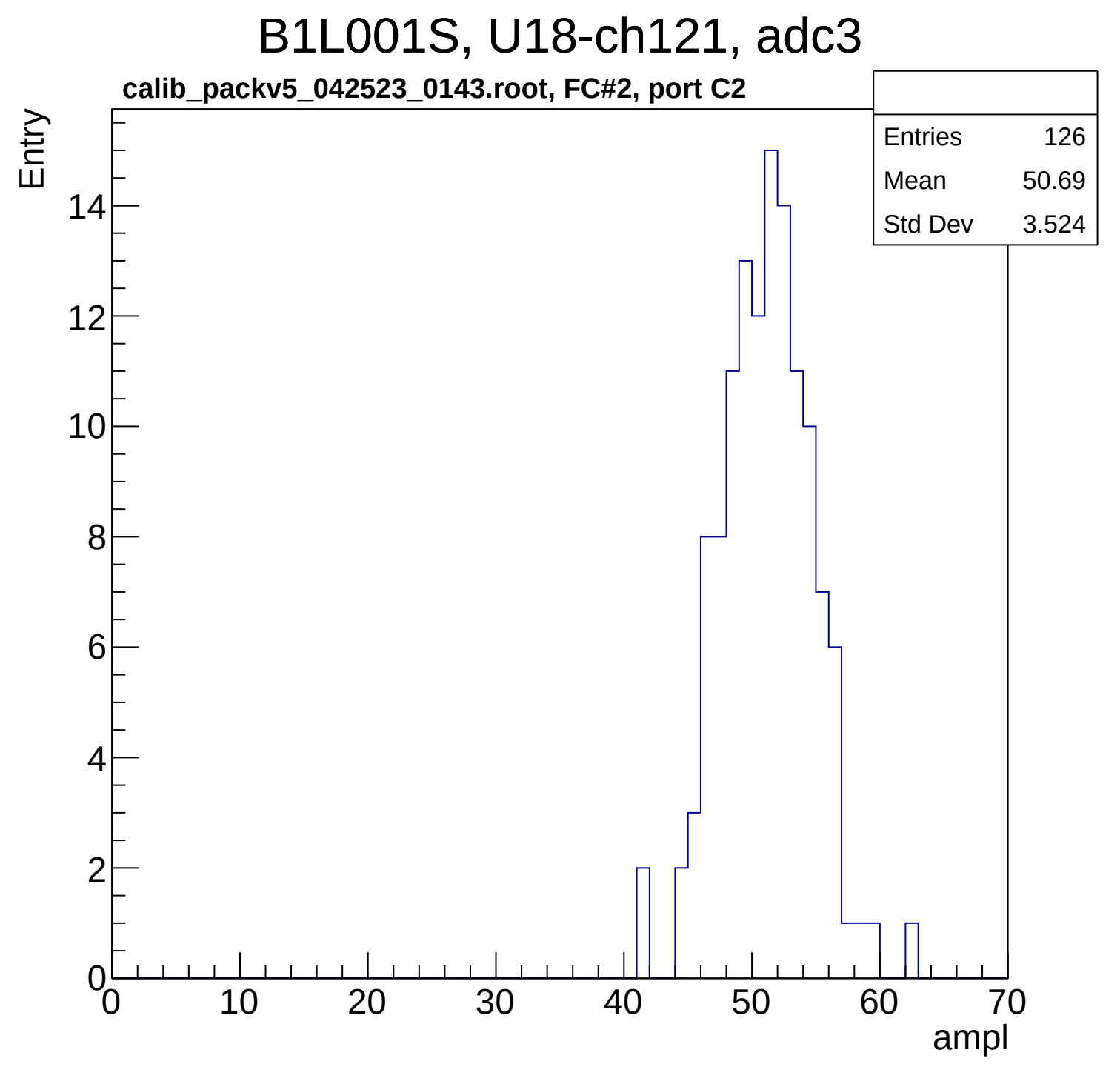

B1L001S, U18-ch120, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 13
Mean 62
Std Dev 1.109
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl

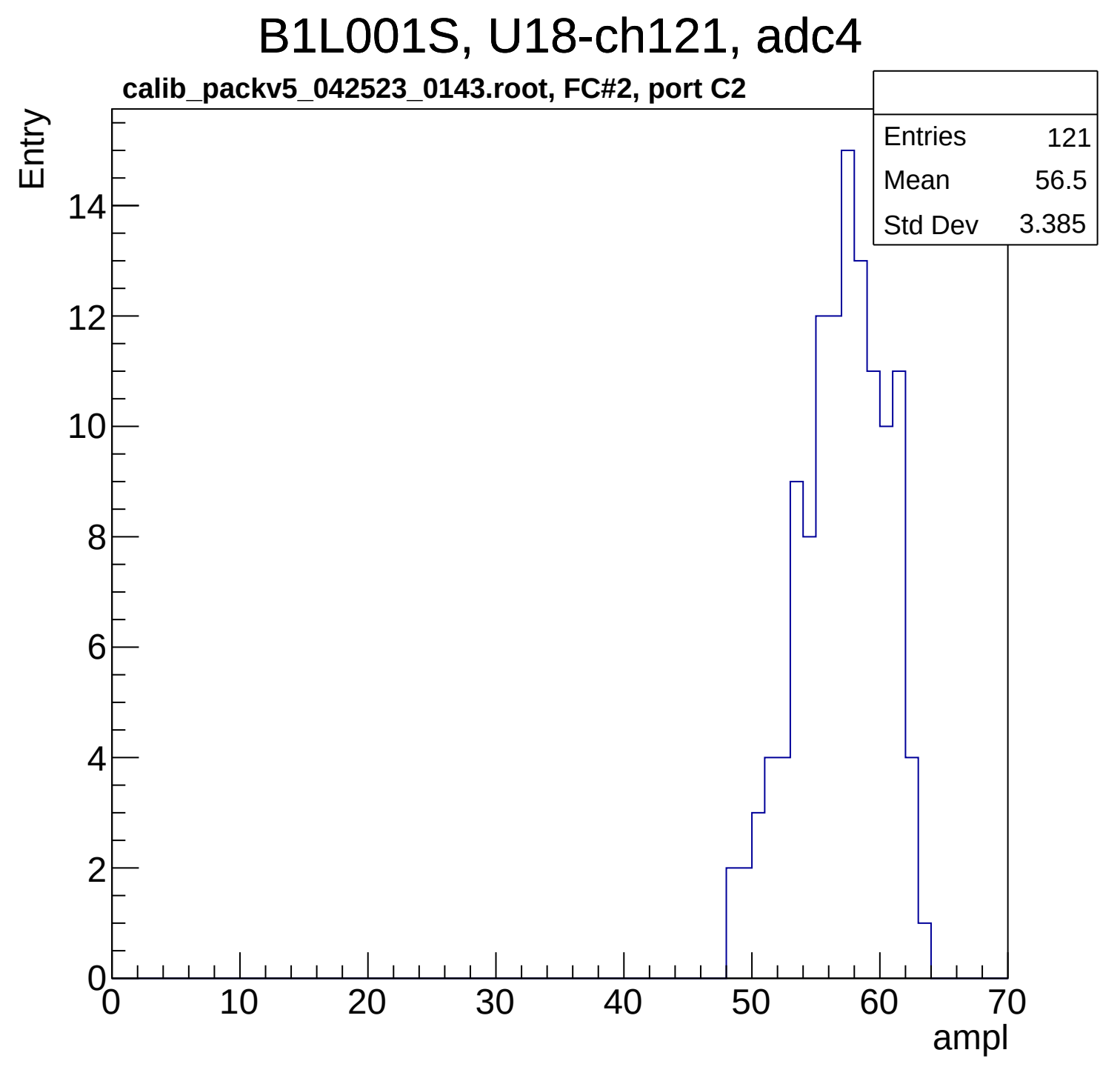

B1L001S, U18-ch120, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 5
Mean 29.4
Std Dev 28.49
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

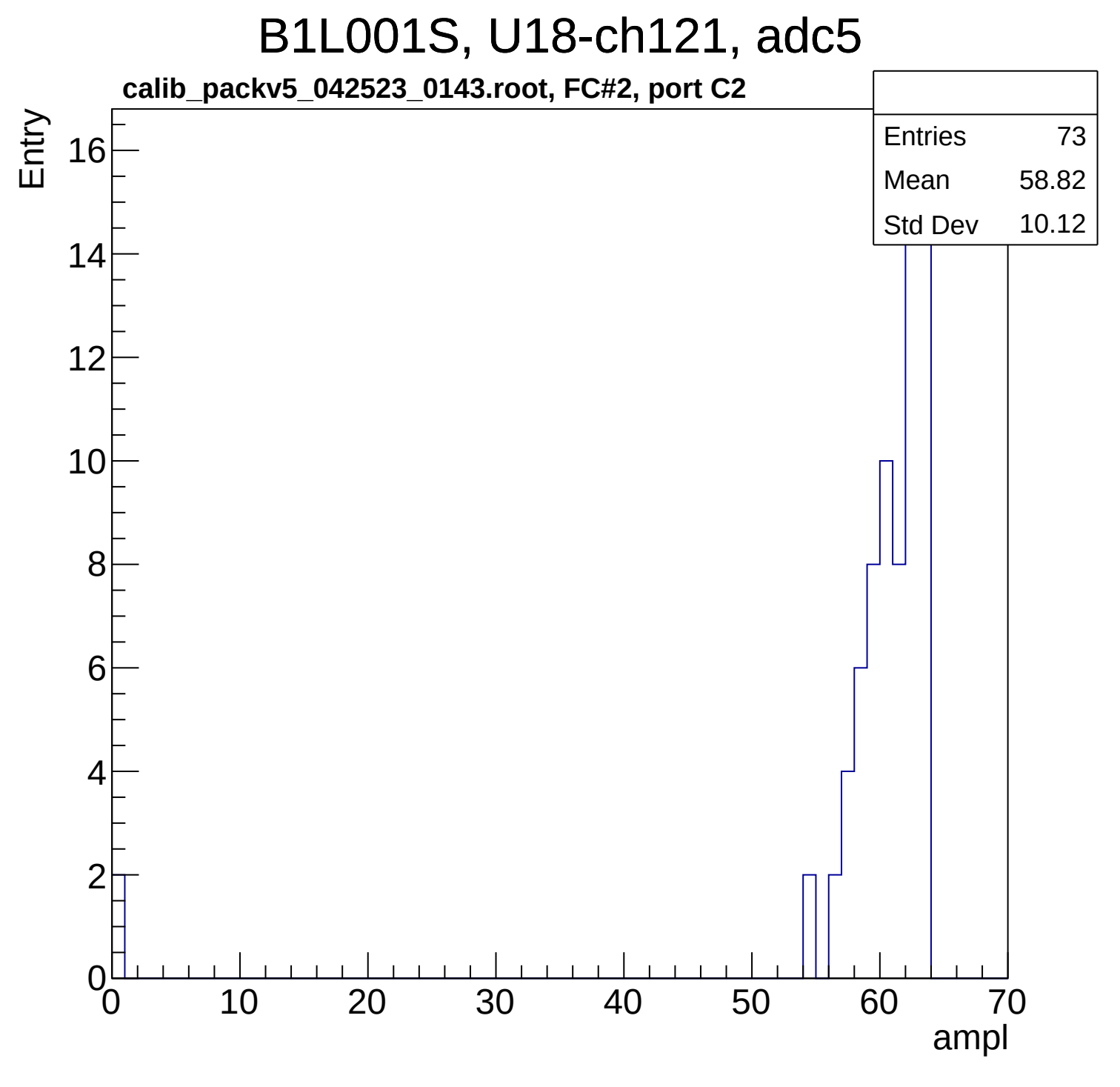

B1L001S, U18-ch121, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 142
Mean 31.15
Std Dev 3.723
Gaus mean : 31.6637
Gaus Width: 3.9733
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

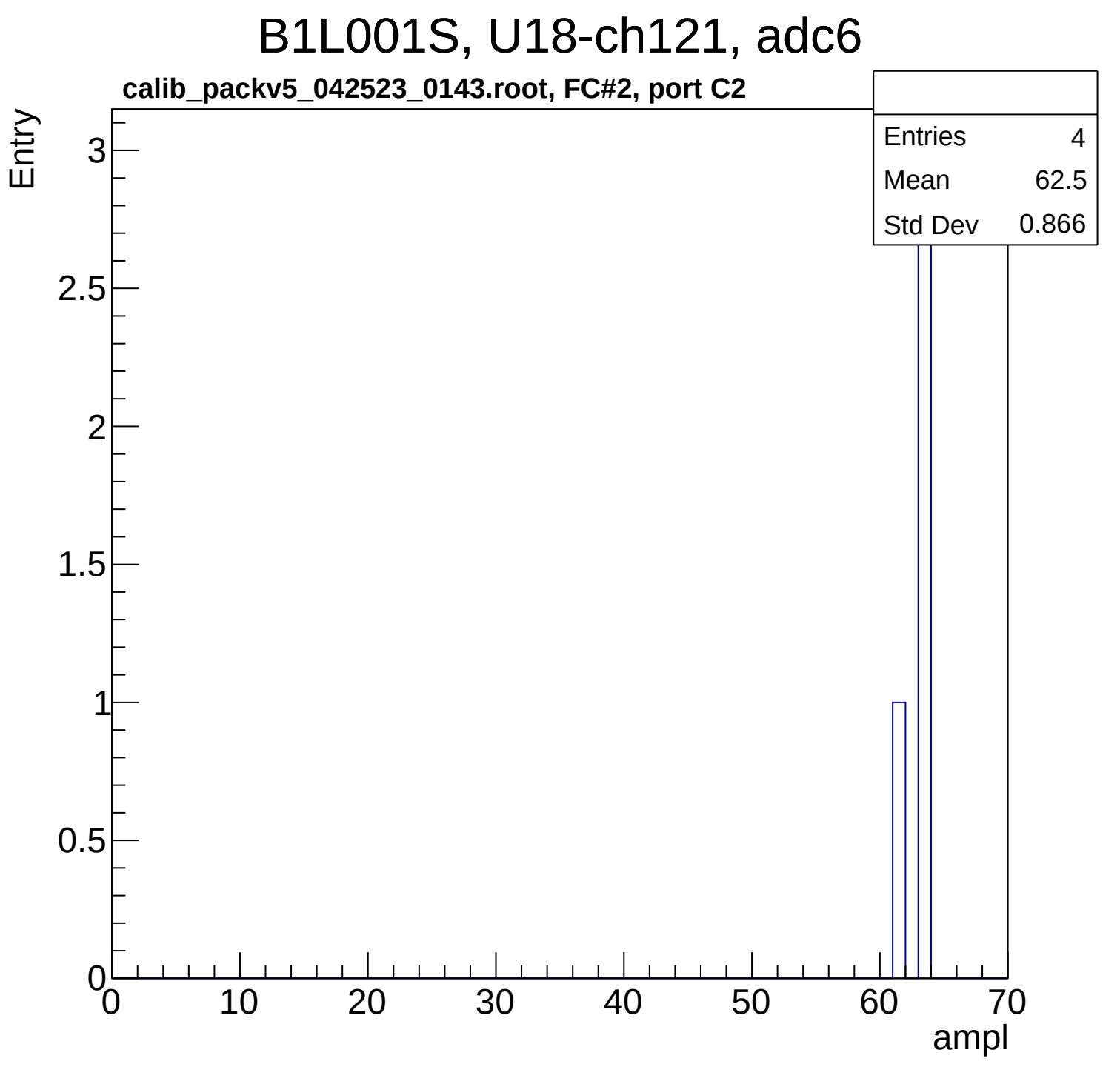

B1L001S, U18-ch121, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 122
Mean 37.77
Std Dev 3.392
Gaus mean : 38.3362
Gaus Width: 3.3634
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

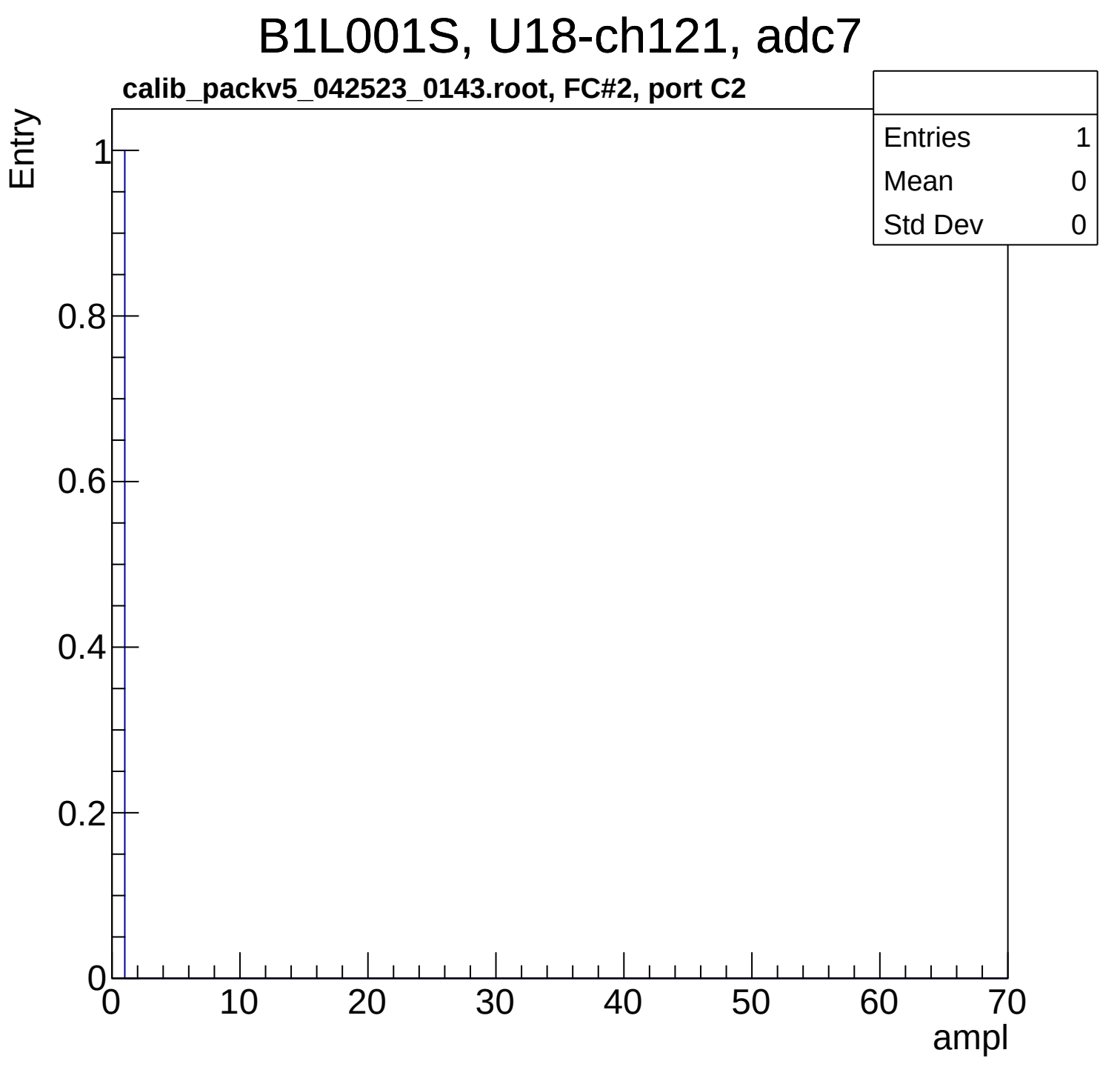

B1L001S, U18-ch121, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 130
Mean 44.22
Std Dev 3.418
Gaus mean : 44.5773
Gaus Width: 3.3810
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

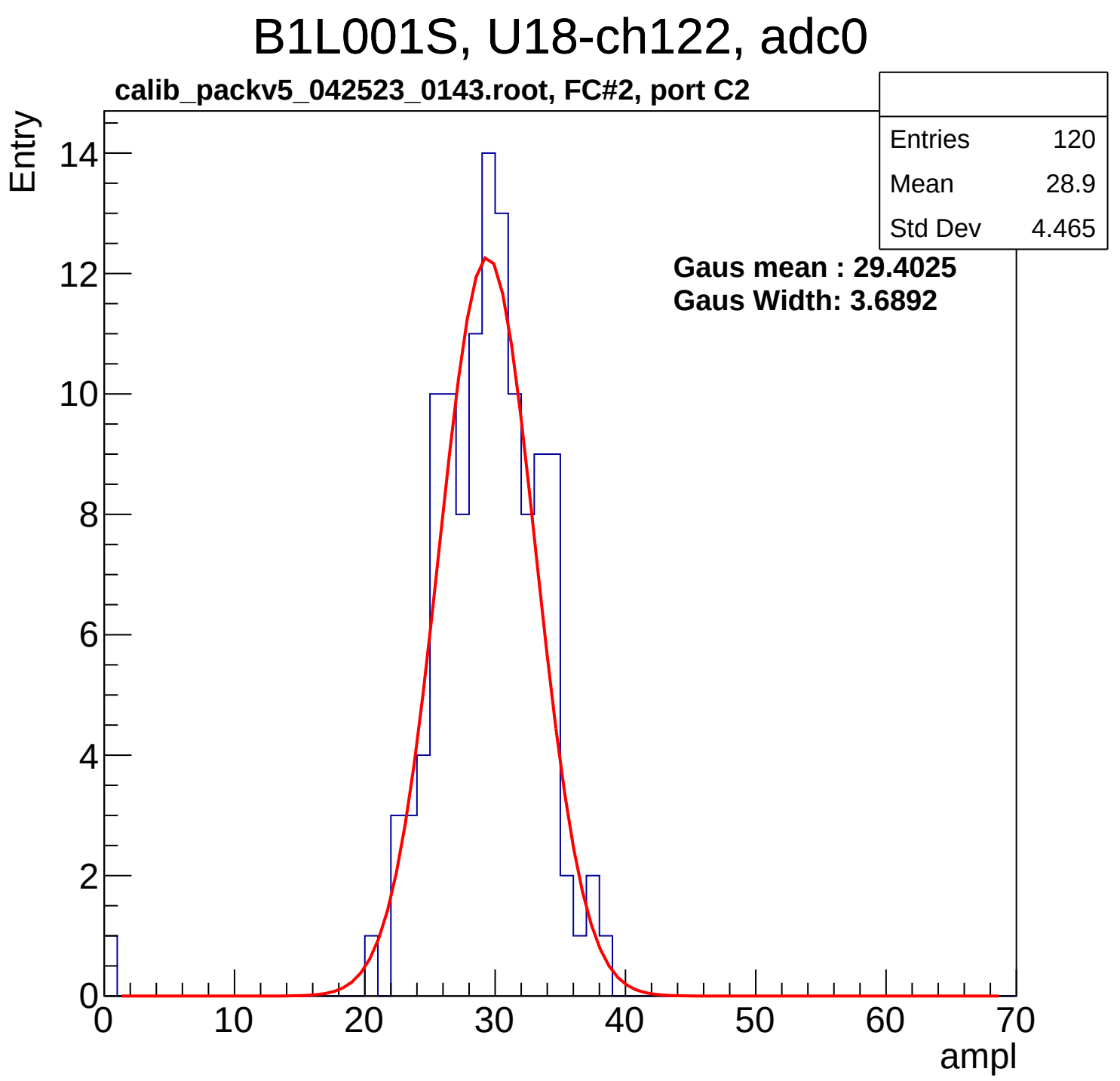

B1L001S, U18-ch121, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 126
Mean 50.69
Std Dev 3.524
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl

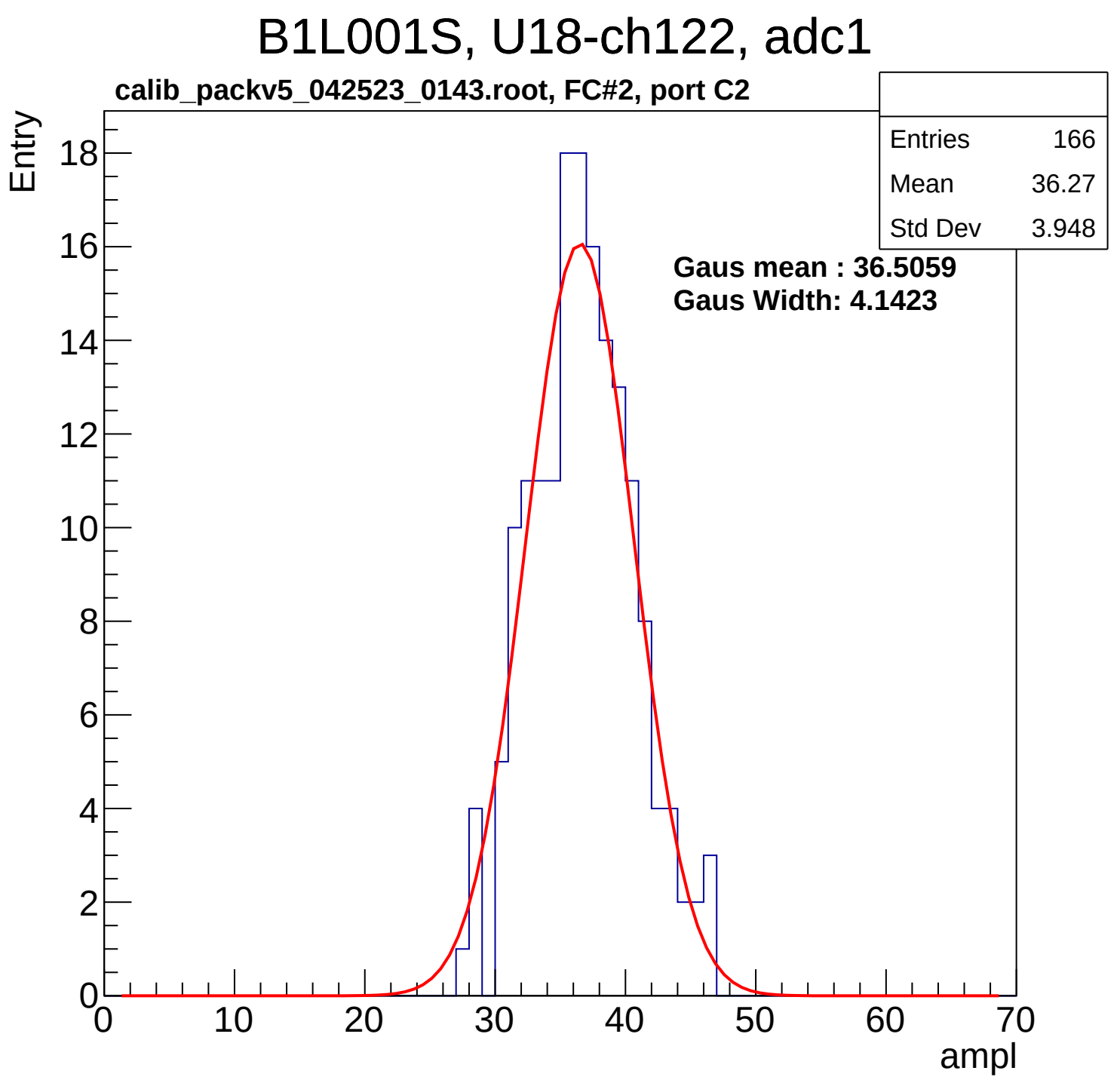

B1L001S, U18-ch121, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 121
Mean 56.5
Std Dev 3.385
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl

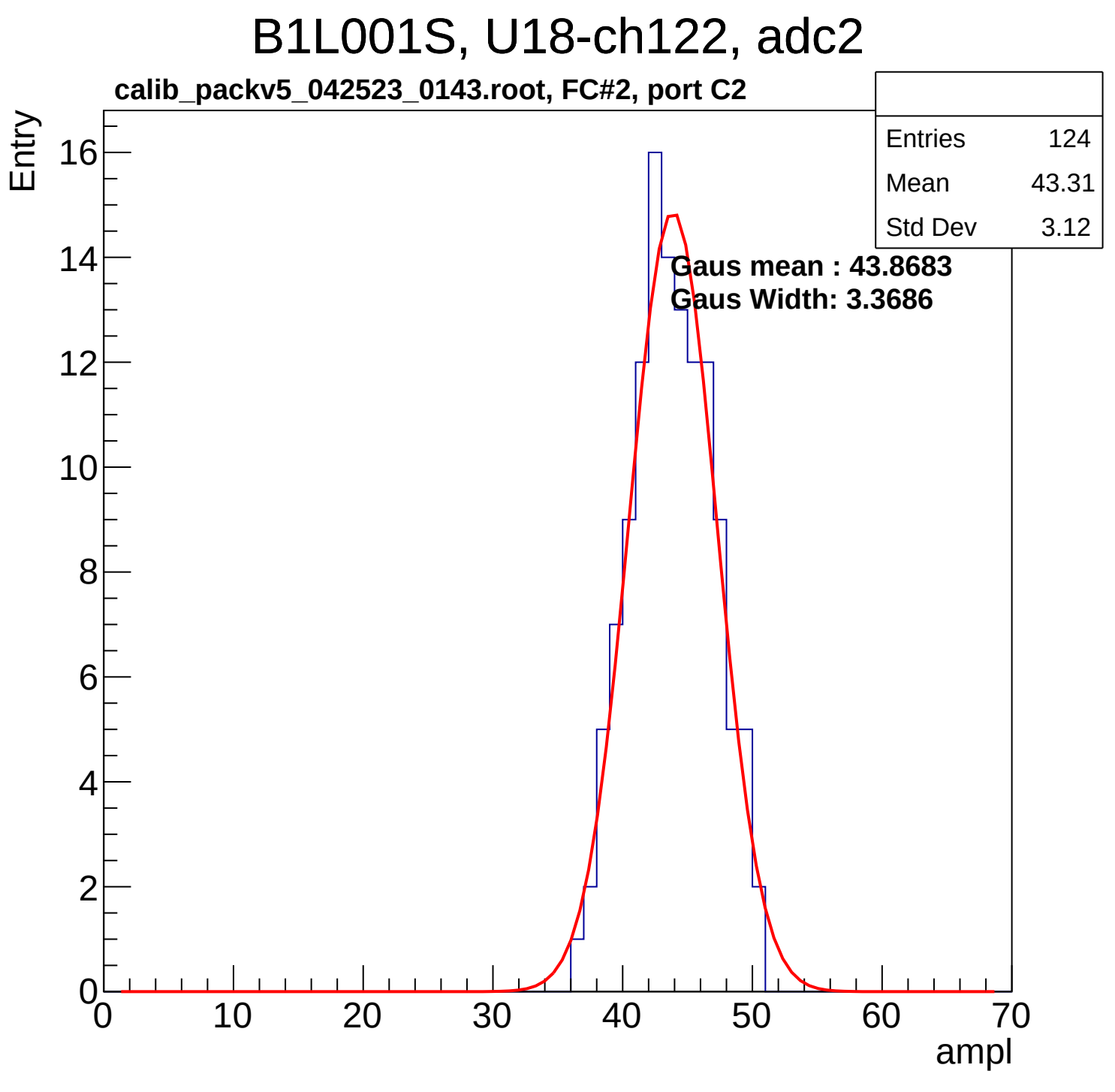

B1L001S, U18-ch121, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 73
Mean 58.82
Std Dev 10.12
Entry
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl

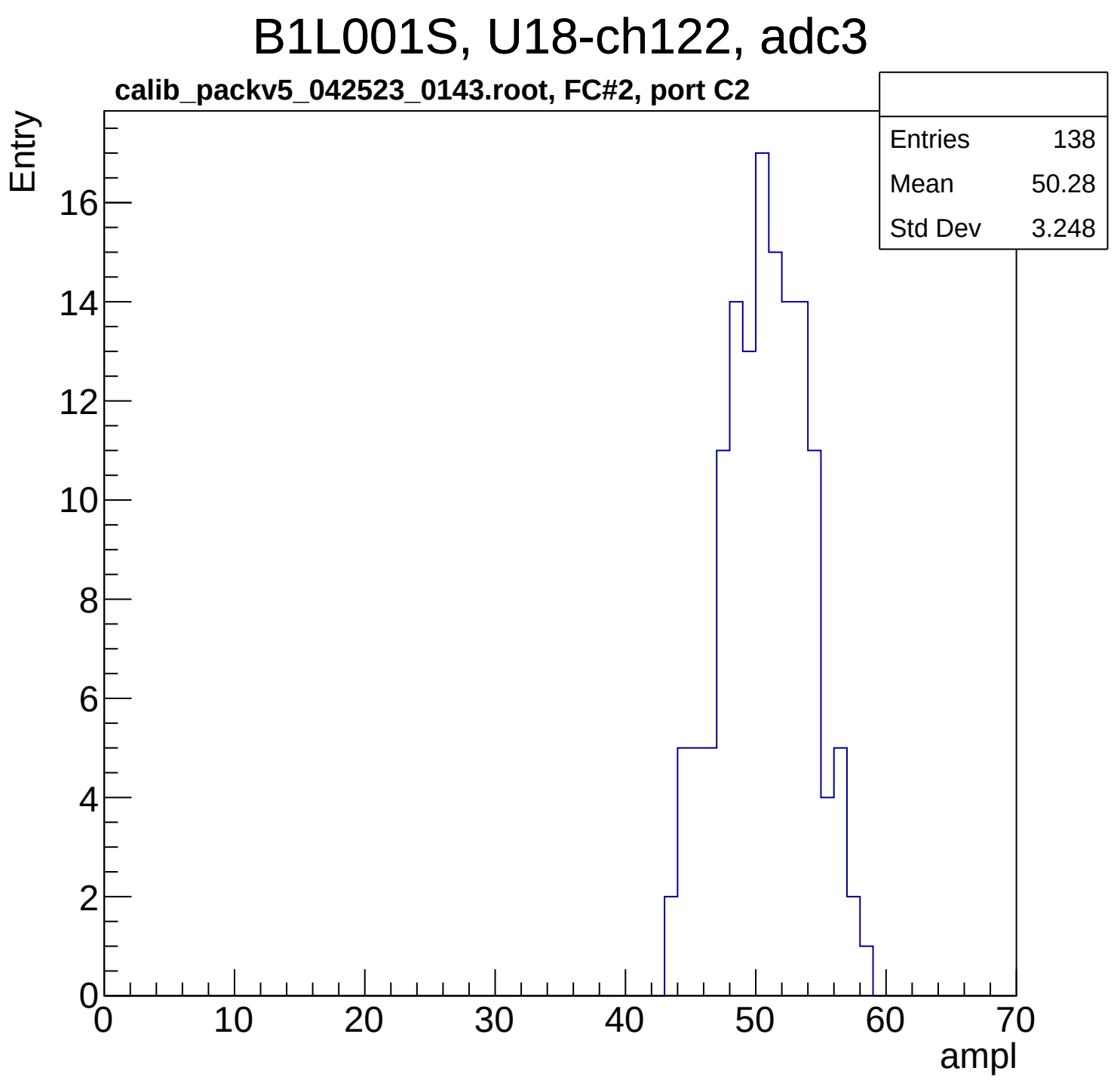

B1L001S, U18-ch121, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 4
Mean 62.5
Std Dev 0.866
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

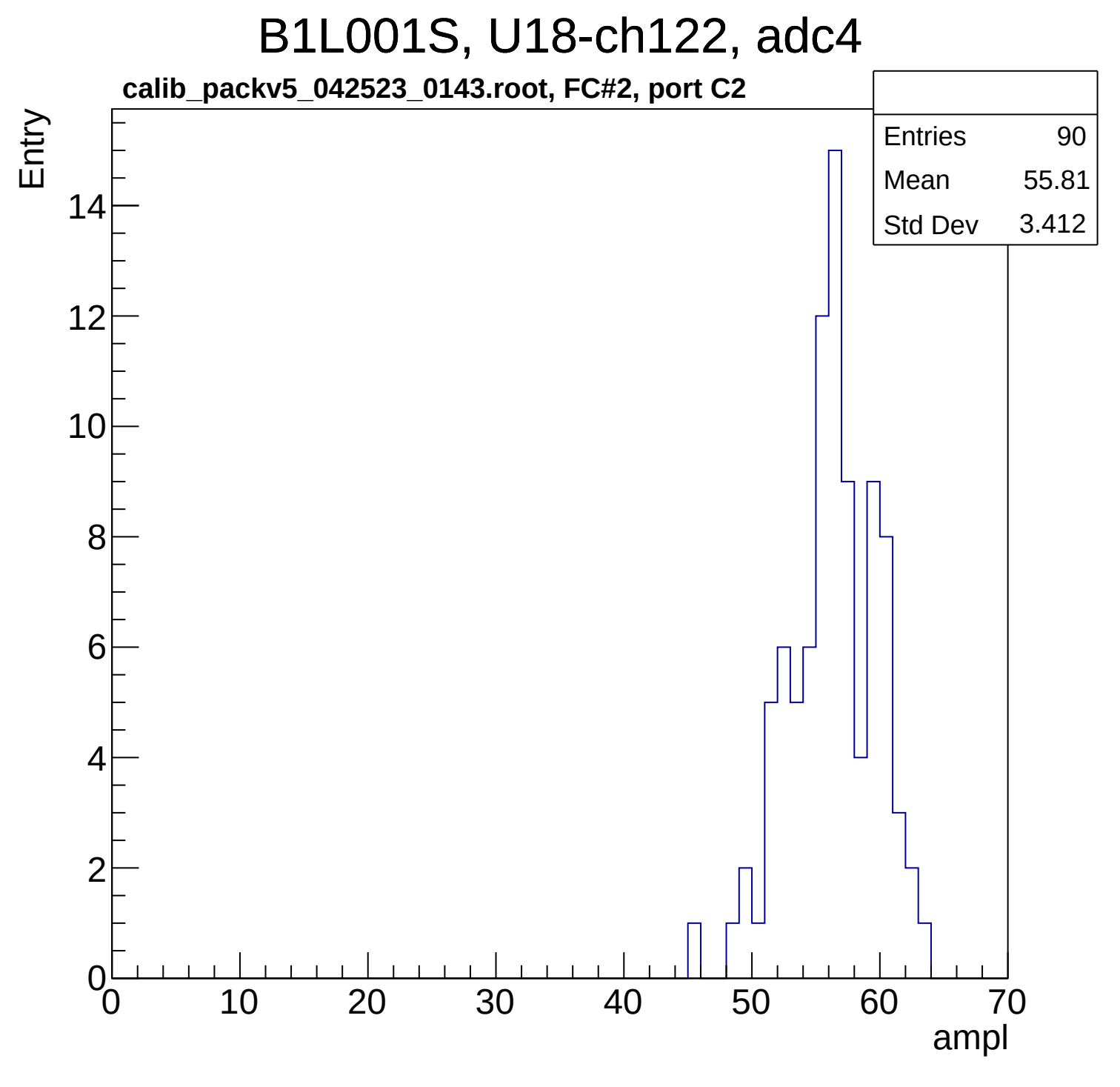

B1L001S, U18-ch121, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

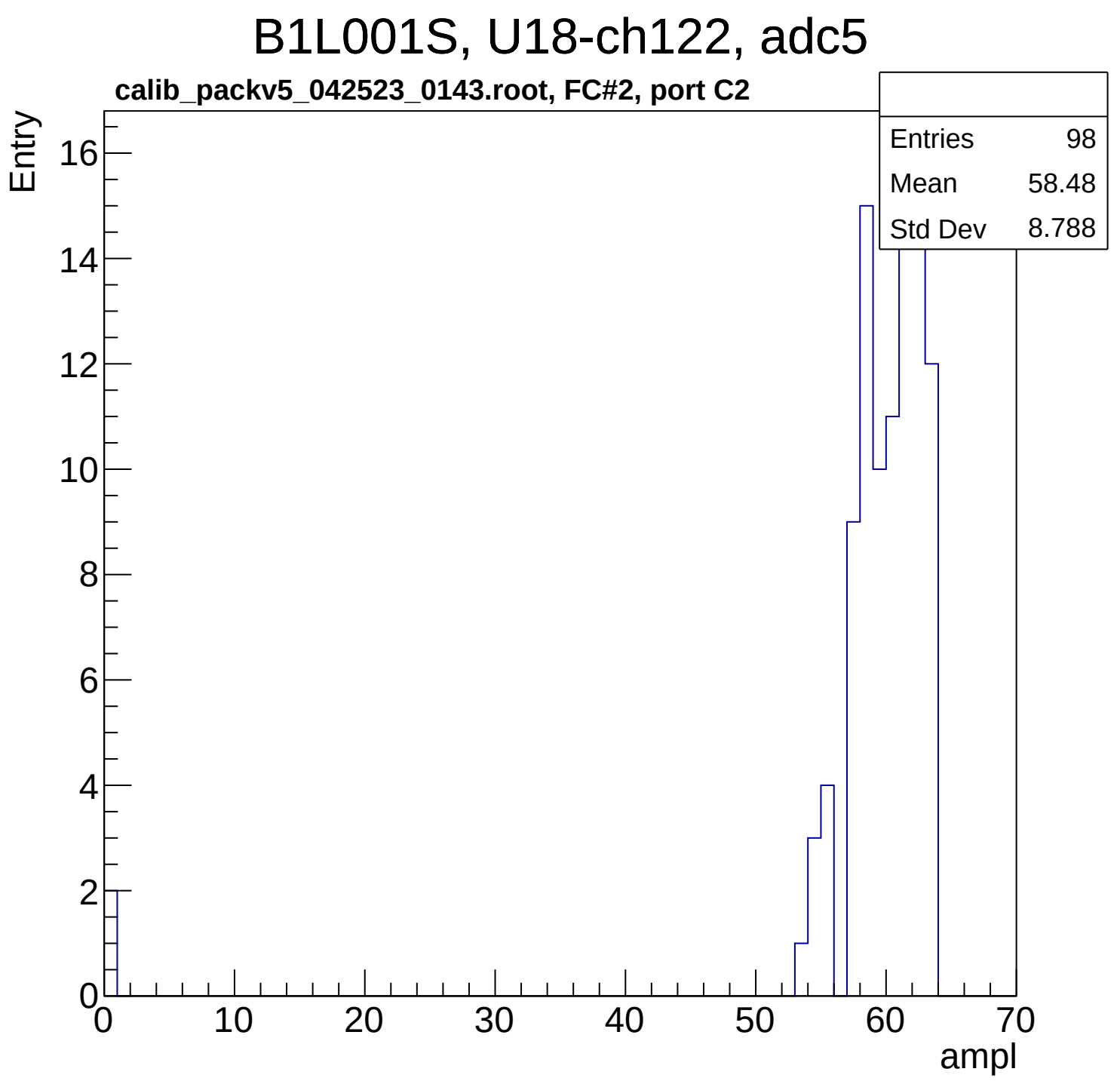

B1L001S, U18-ch122, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 120
Mean 28.9
Std Dev 4.465
Gaus mean : 29.4025
Gaus Width: 3.6892
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

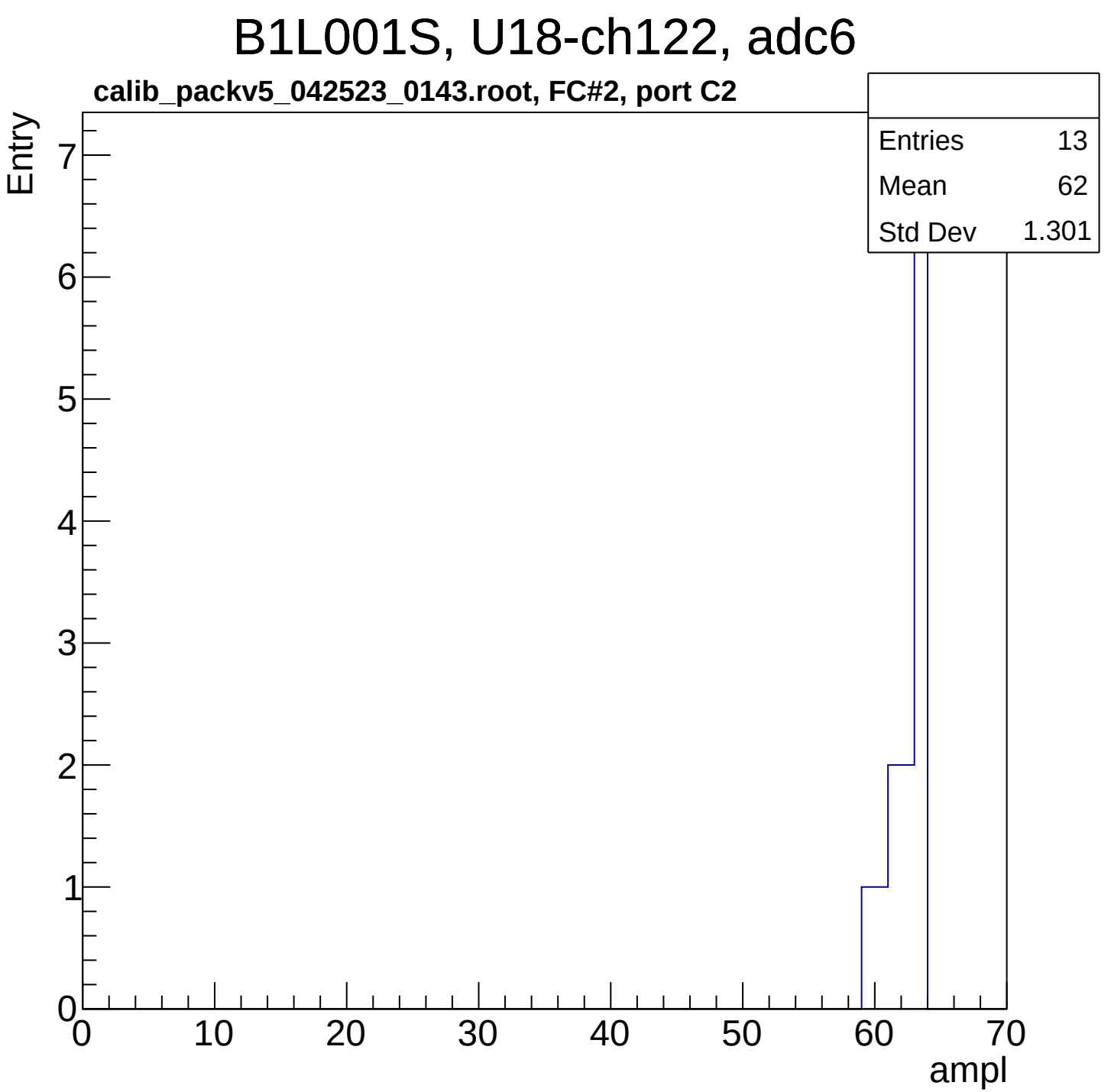

B1L001S, U18-ch122, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 166
Mean 36.27
Std Dev 3.948
Gaus mean : 36.5059
Gaus Width: 4.1423
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

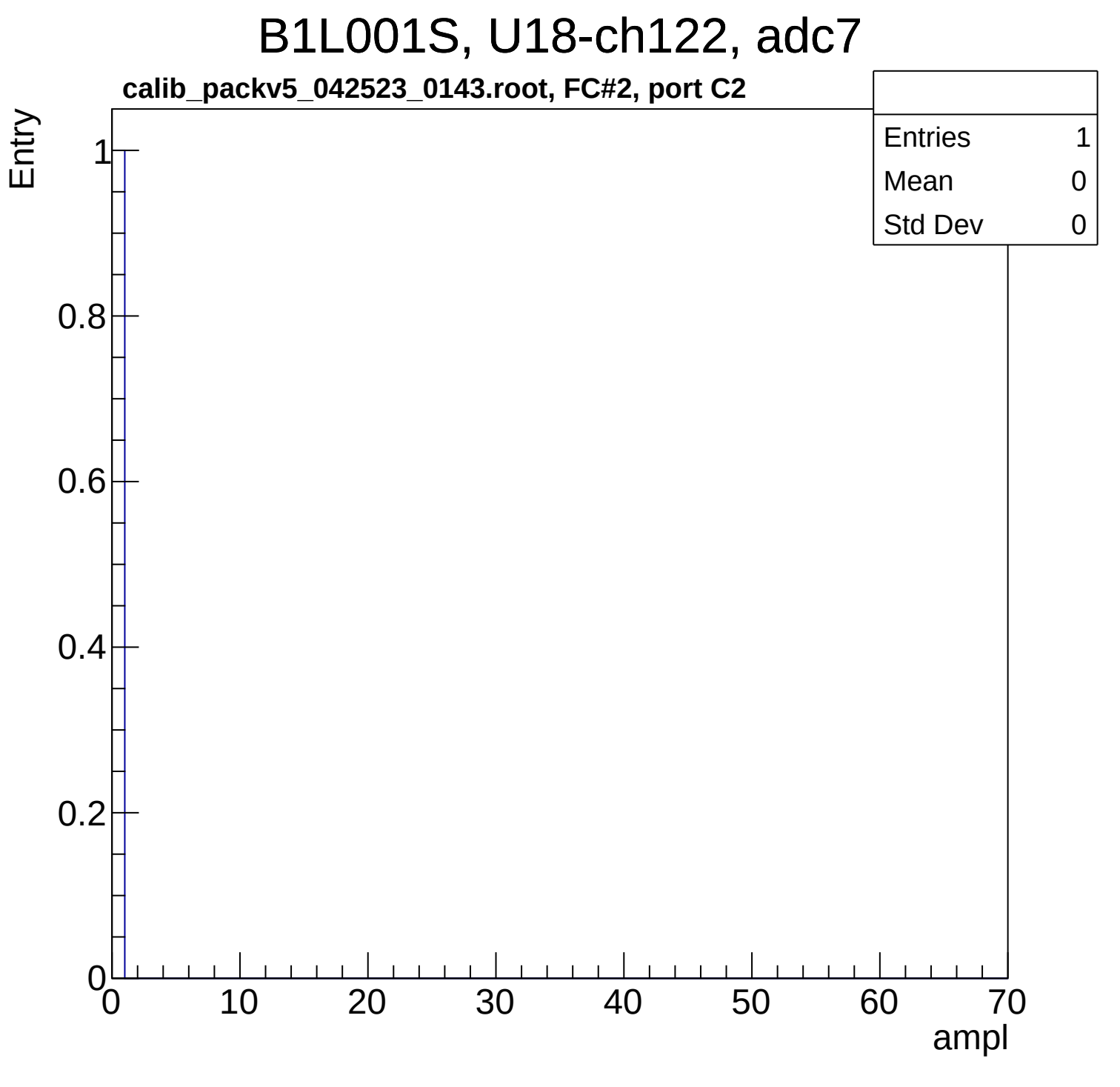

B1L001S, U18-ch122, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 124
Mean 43.31
Std Dev 3.12
Gaus mean : 43.8683
Gaus Width: 3.3686
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

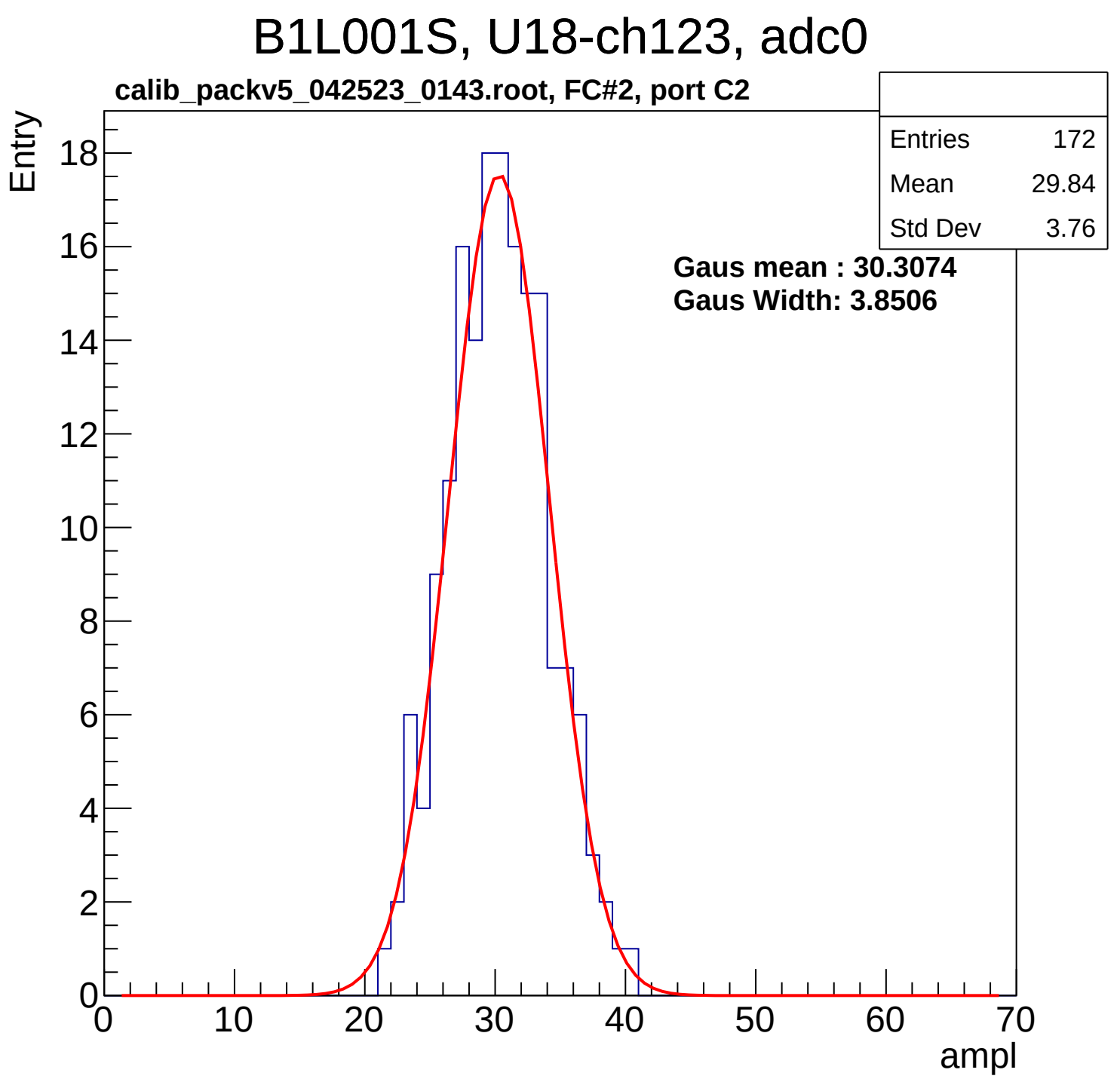

B1L001S, U18-ch122, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 138
Mean 50.28
Std Dev 3.248
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

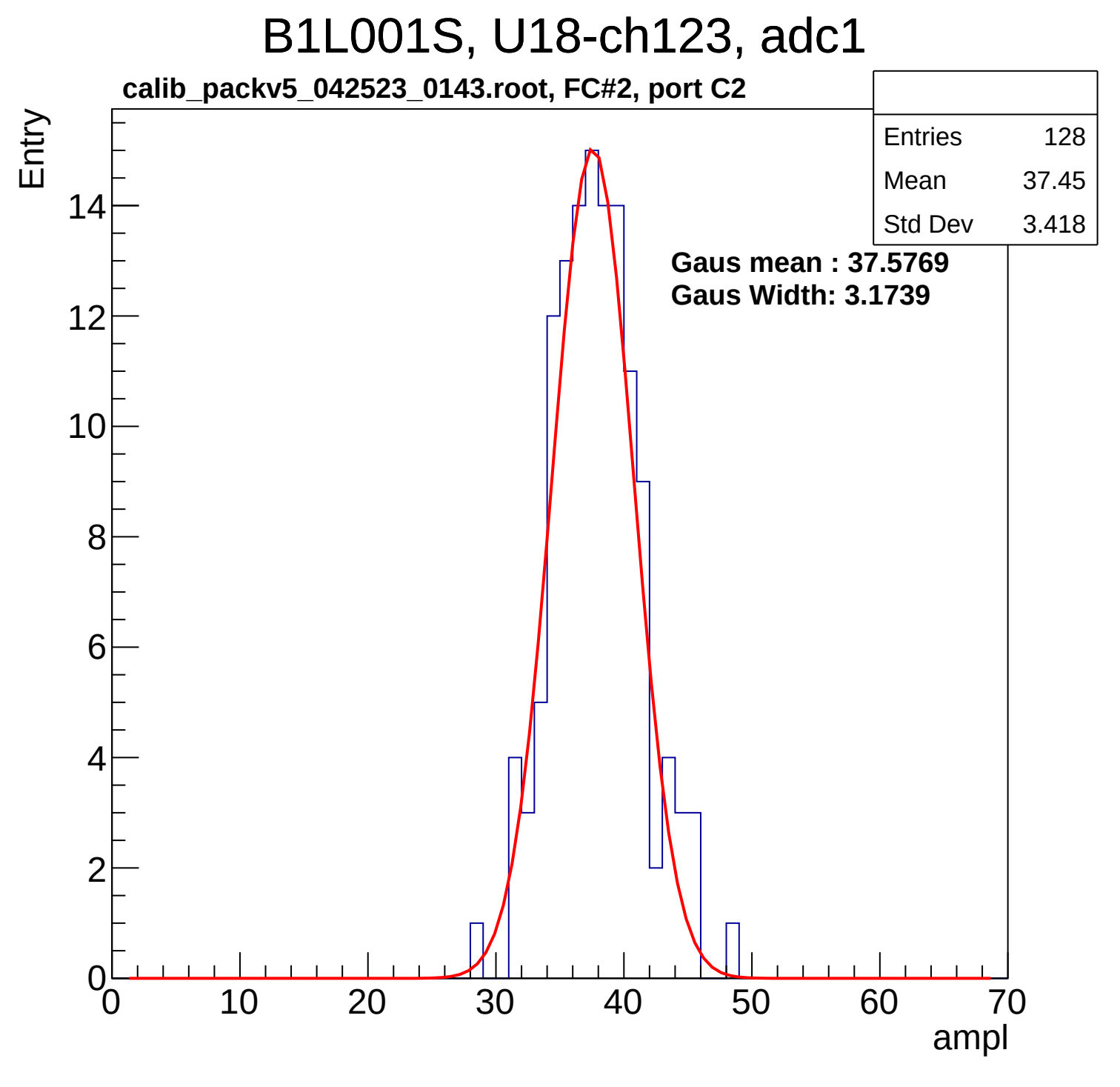

B1L001S, U18-ch122, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 90
Mean 55.81
Std Dev 3.412
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl

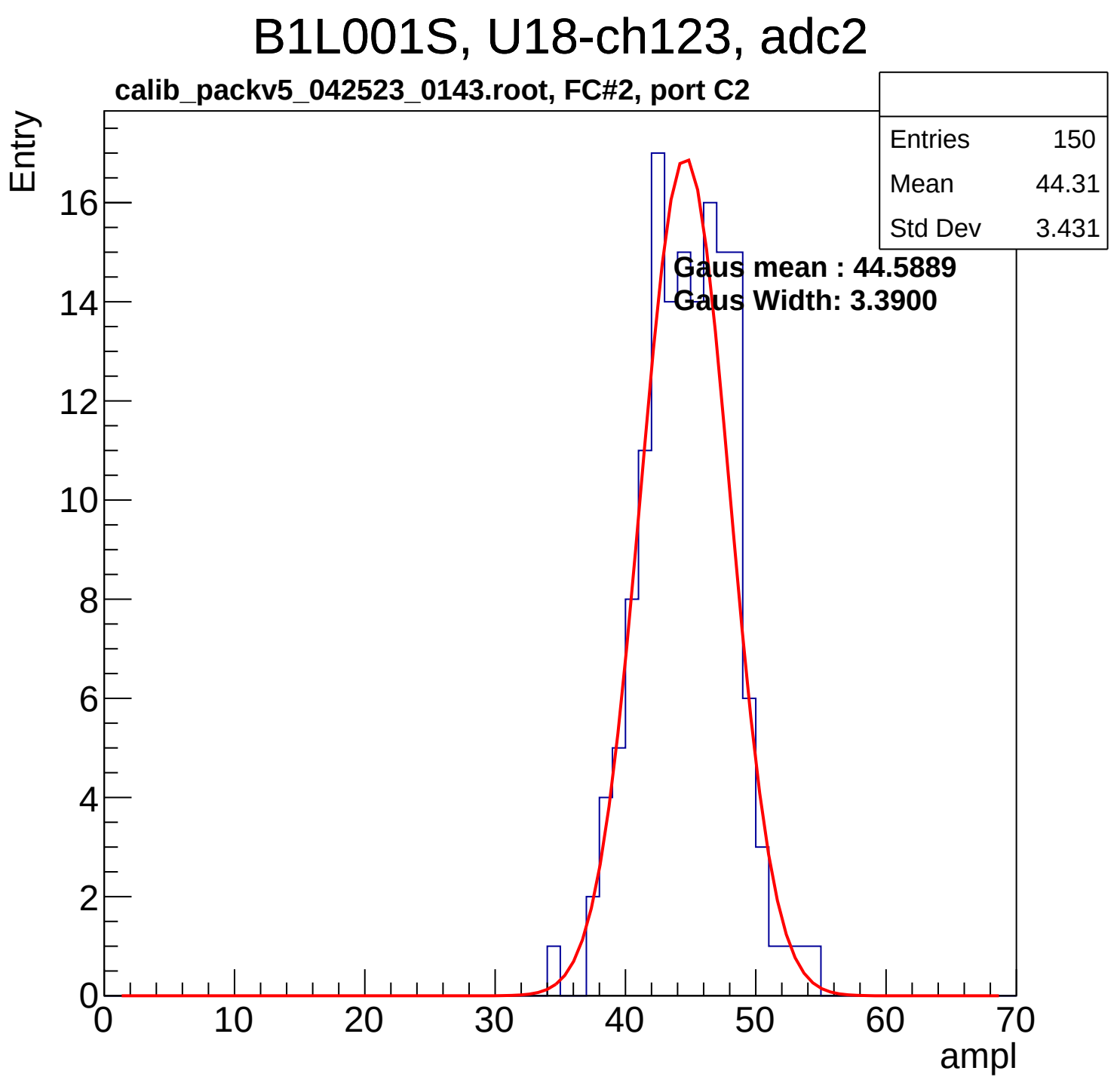

B1L001S, U18-ch122, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 98
Mean 58.48
Std Dev 8.788
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

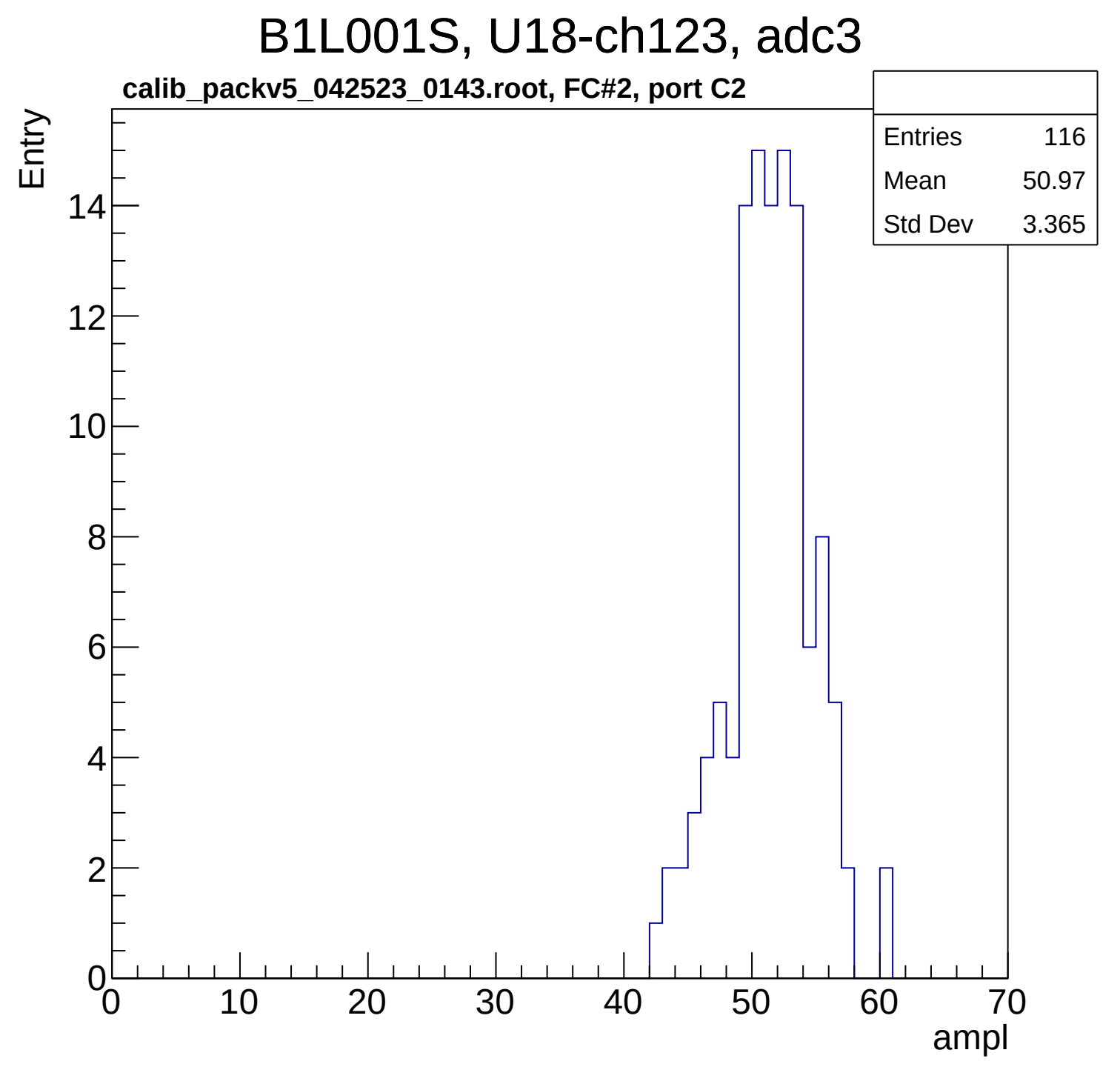

B1L001S, U18-ch122, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 13
Mean 62
Std Dev 1.301
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

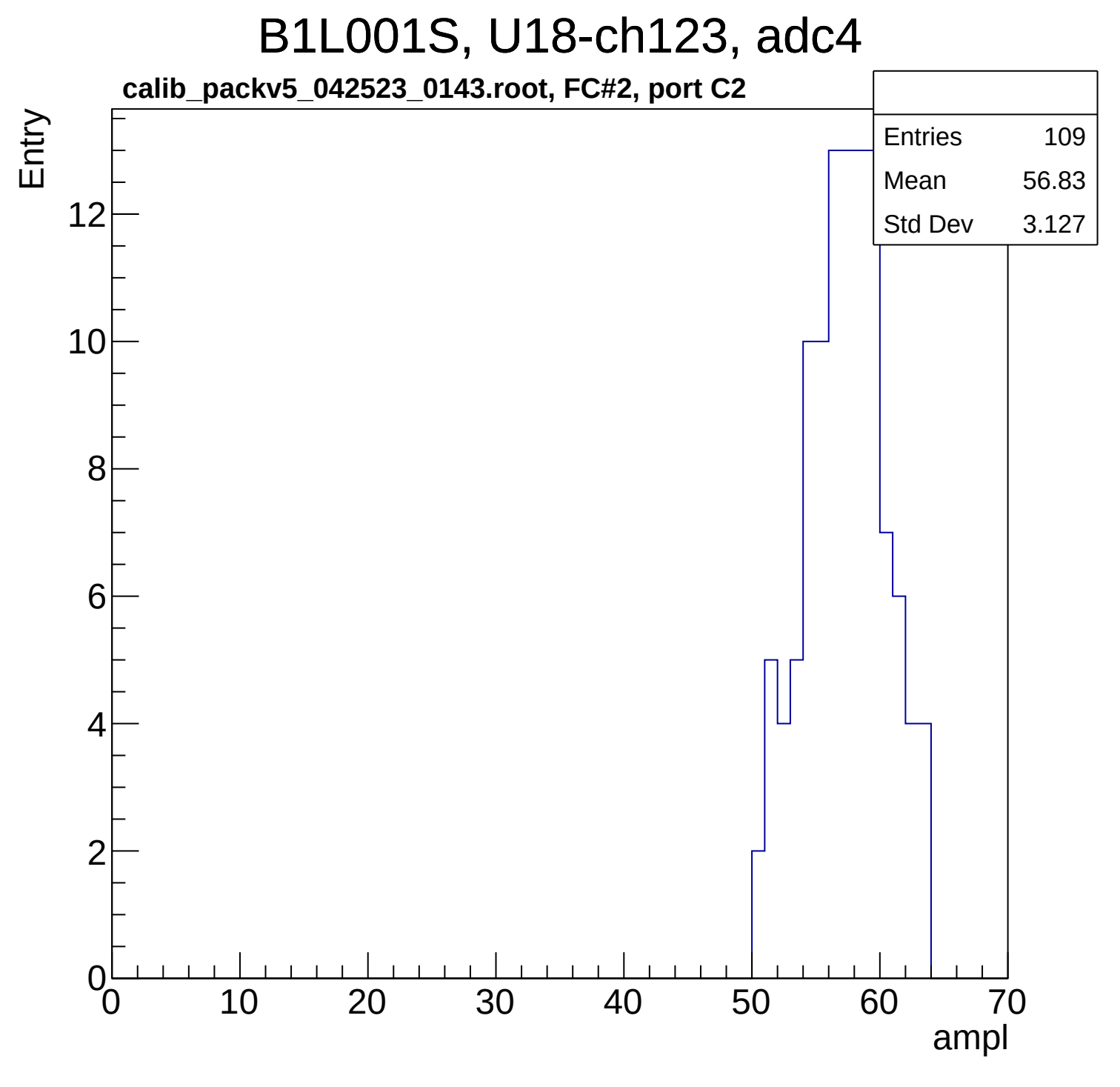

B1L001S, U18-ch122, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

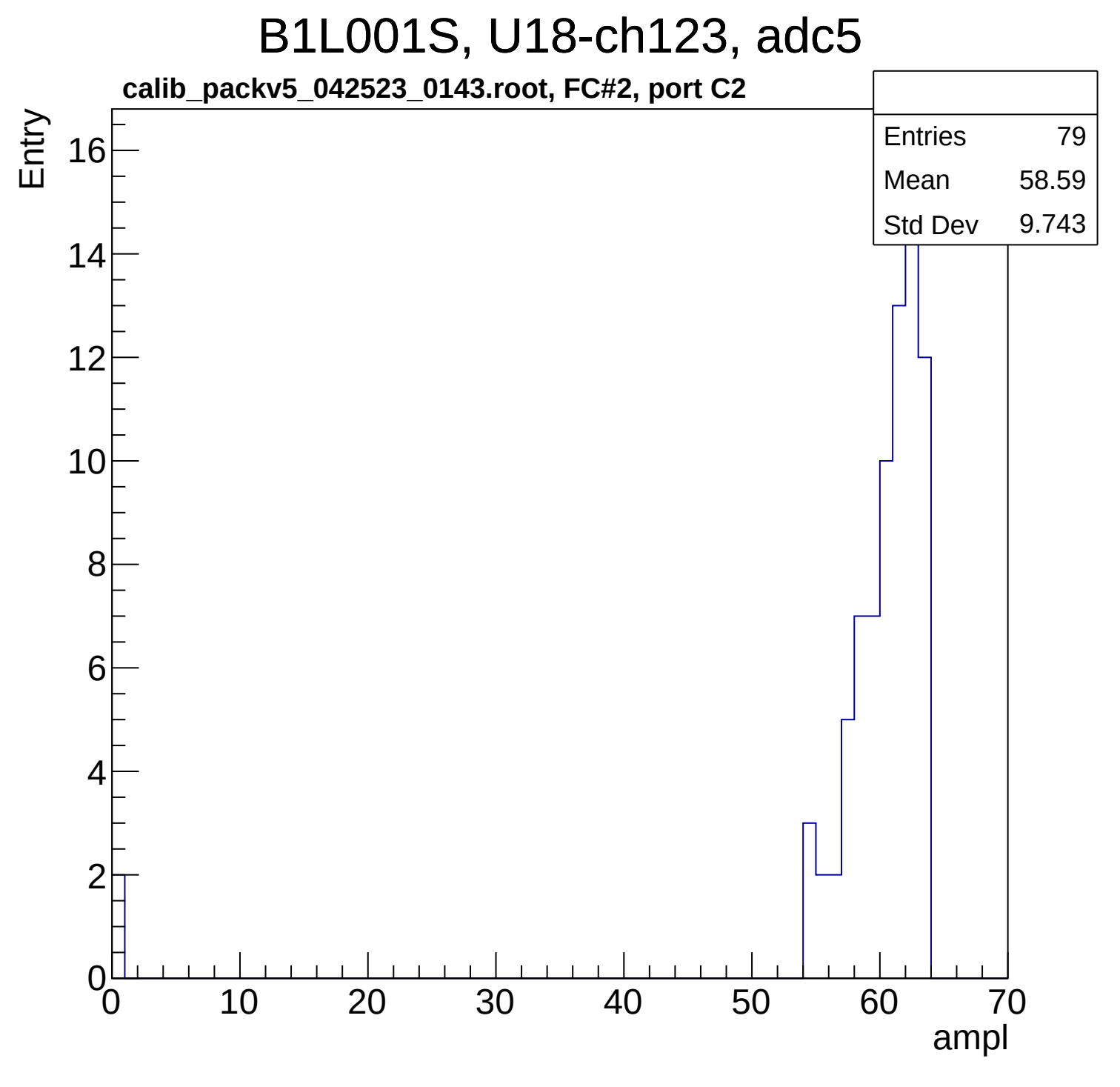

B1L001S, U18-ch123, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 172
Mean 29.84
Std Dev 3.76
Gaus mean : 30.3074
Gaus Width: 3.8506
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

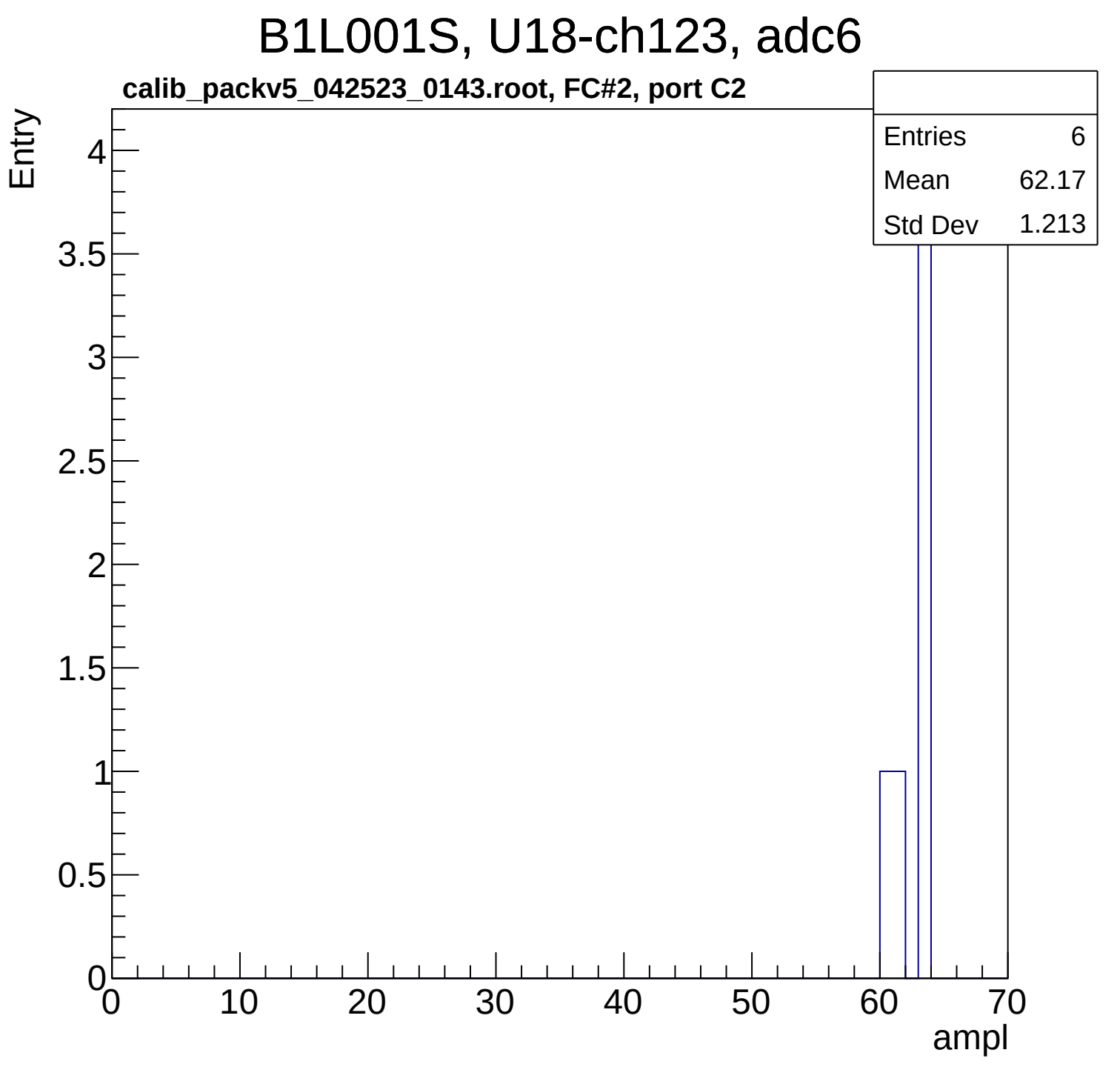

B1L001S, U18-ch123, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 128
Mean 37.45
Std Dev 3.418
Gaus mean : 37.5769
Gaus Width: 3.1739
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

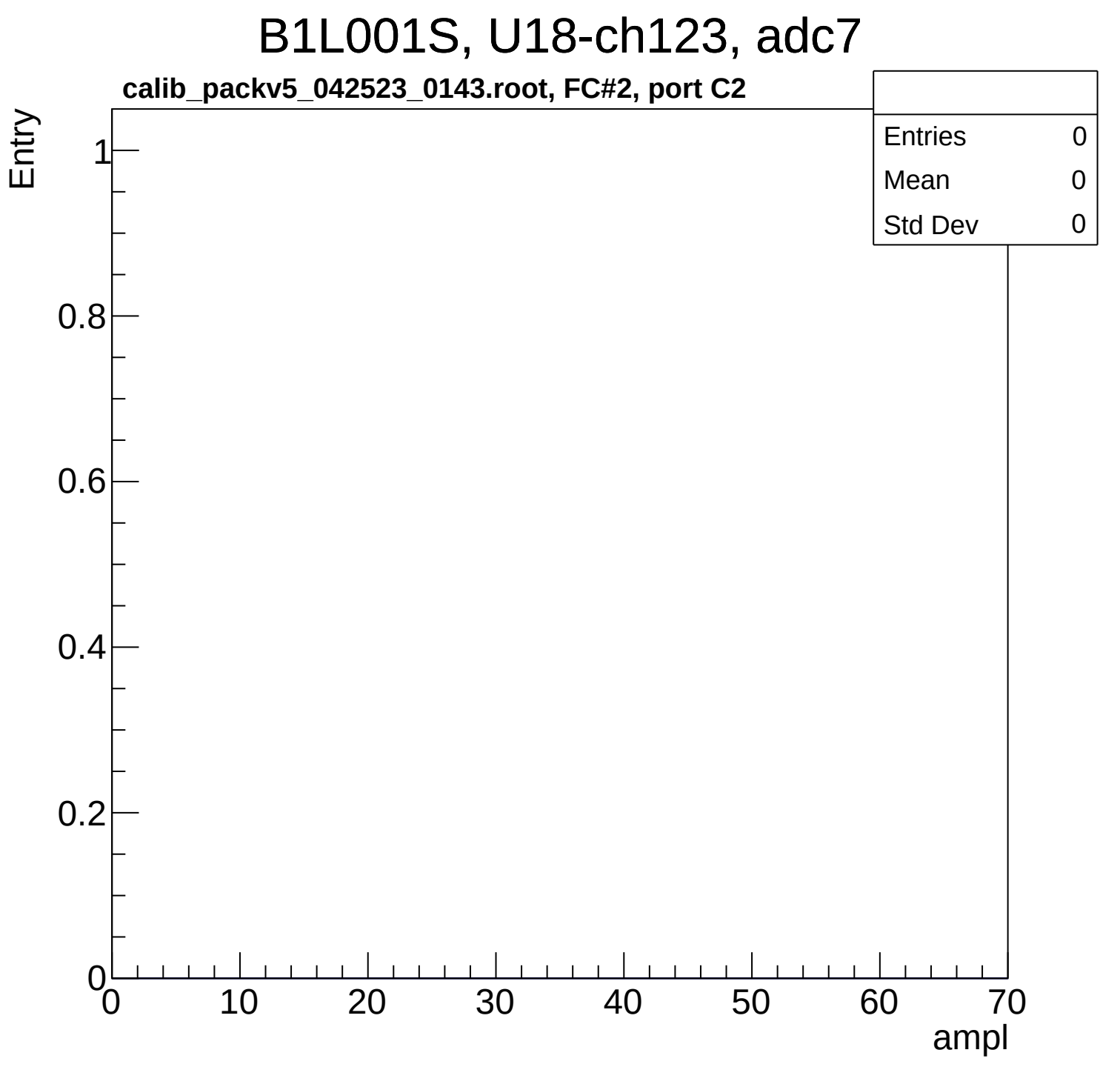

B1L001S, U18-ch123, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 150
Mean 44.31
Std Dev 3.431
Gaus mean : 44.5889
Gaus Width: 3.3900
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

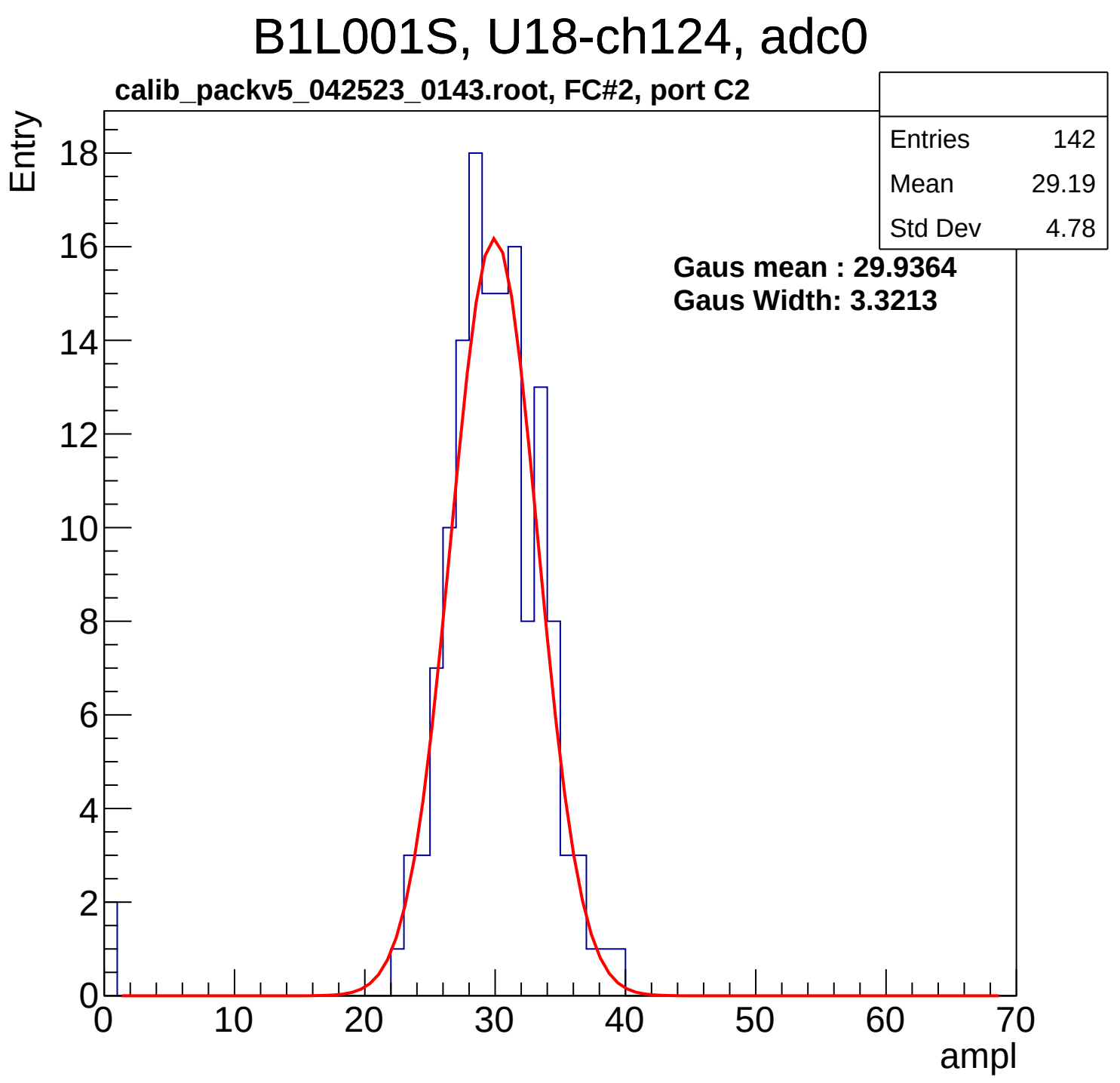

B1L001S, U18-ch123, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 116
Mean 50.97
Std Dev 3.365
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl

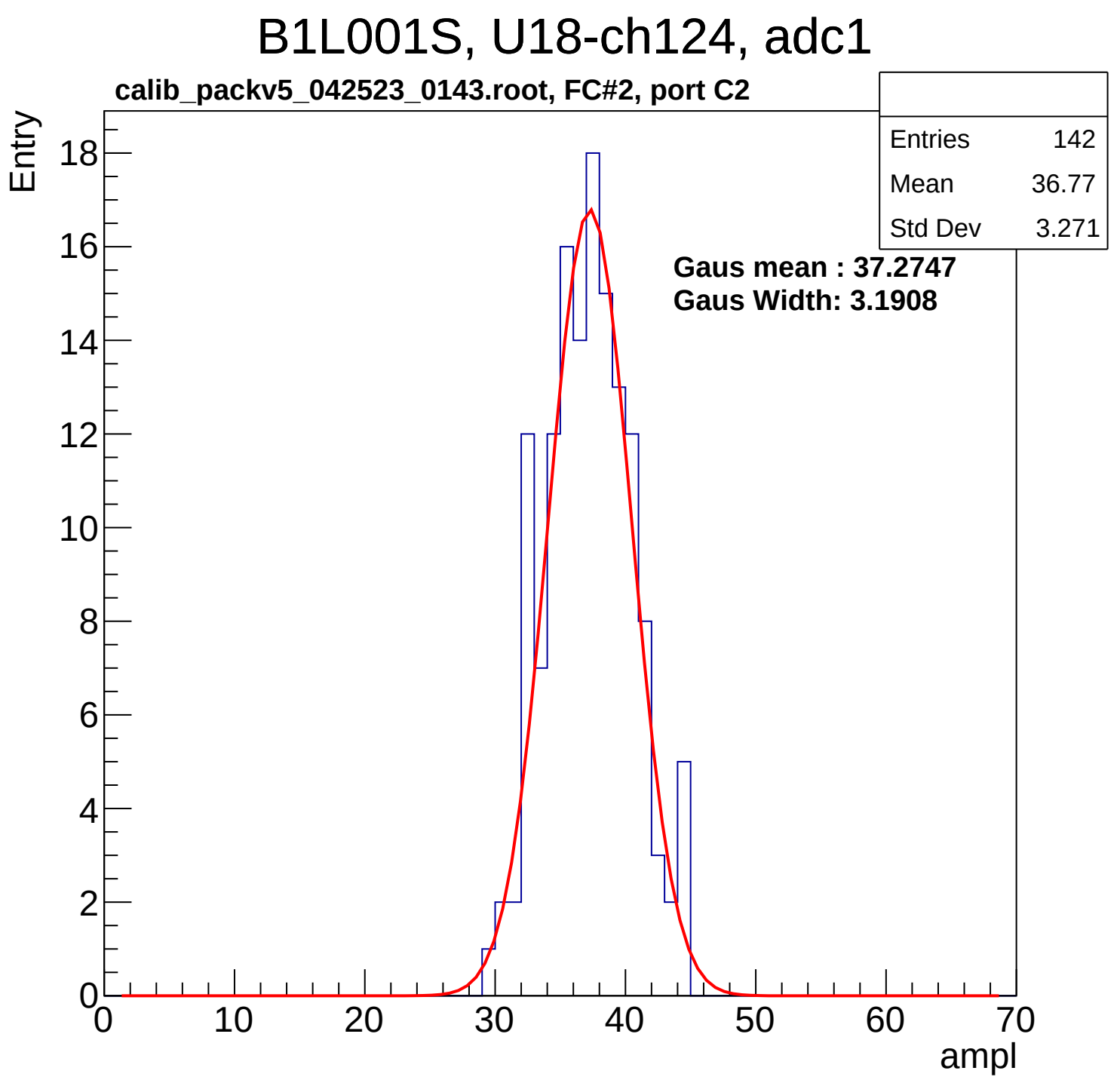

B1L001S, U18-ch123, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 109
Mean 56.83
Std Dev 3.127
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl

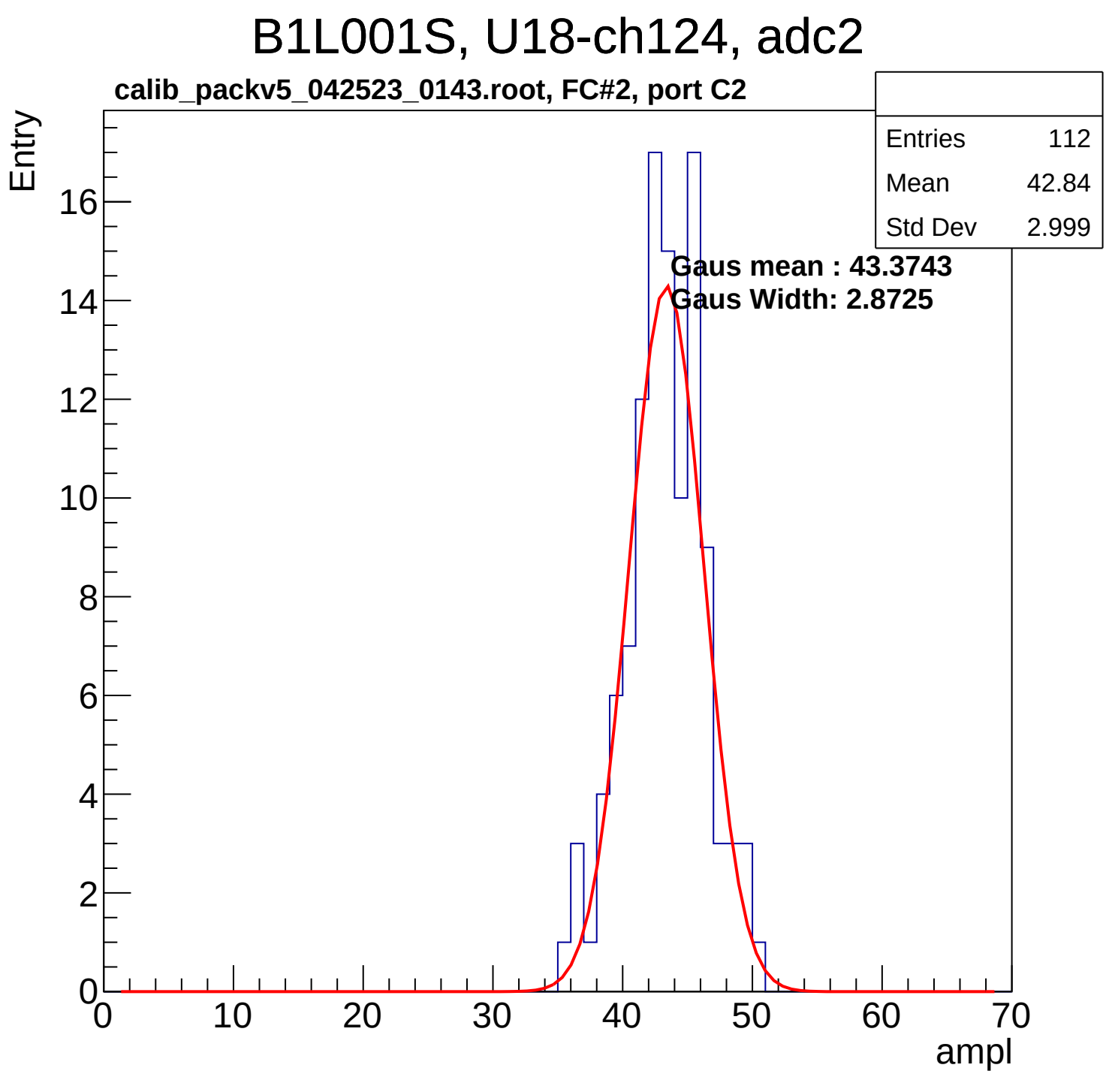

B1L001S, U18-ch123, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 79
Mean 58.59
Std Dev 9.743
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

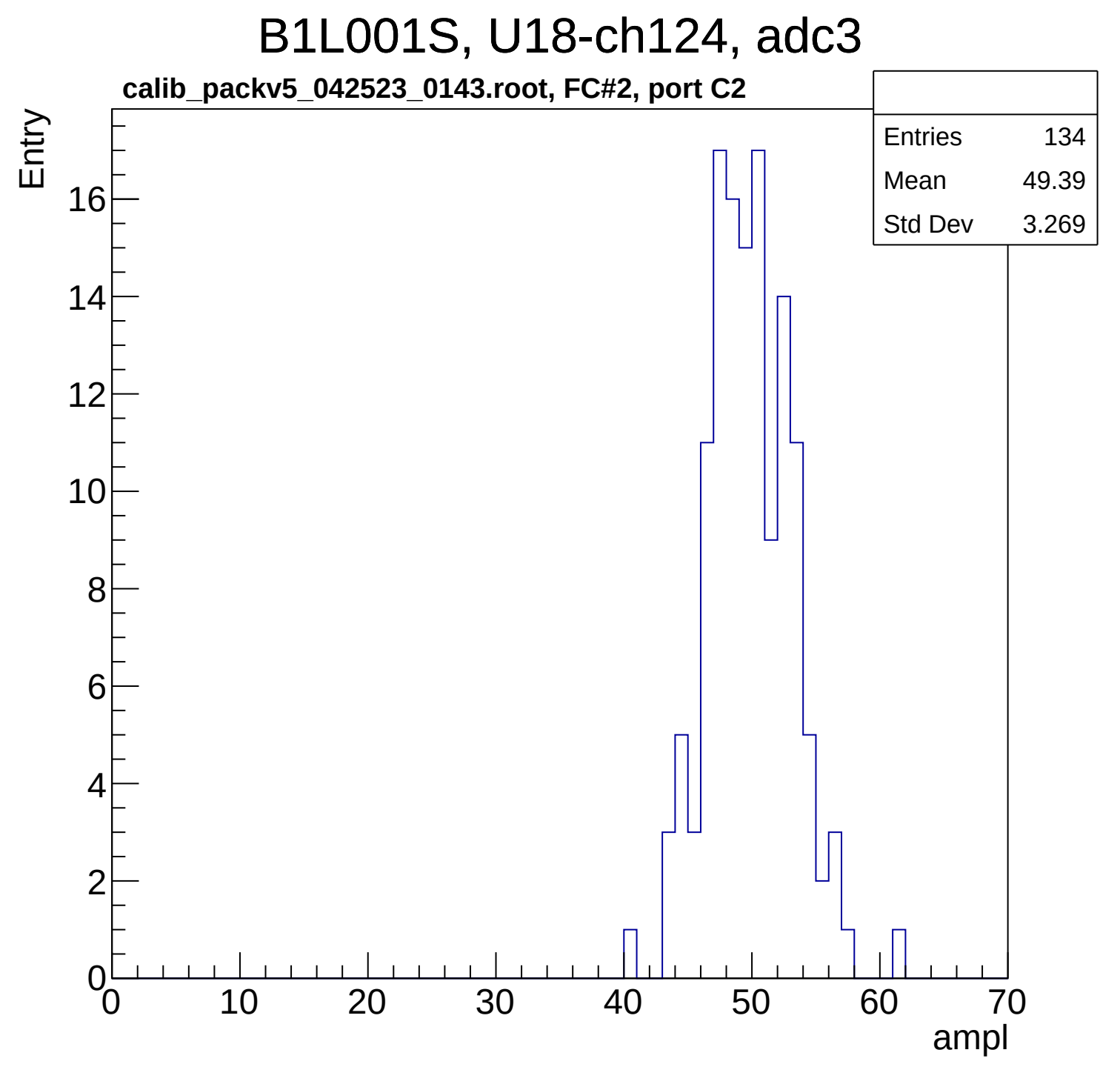

B1L001S, U18-ch123, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 6
Mean 62.17
Std Dev 1.213
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

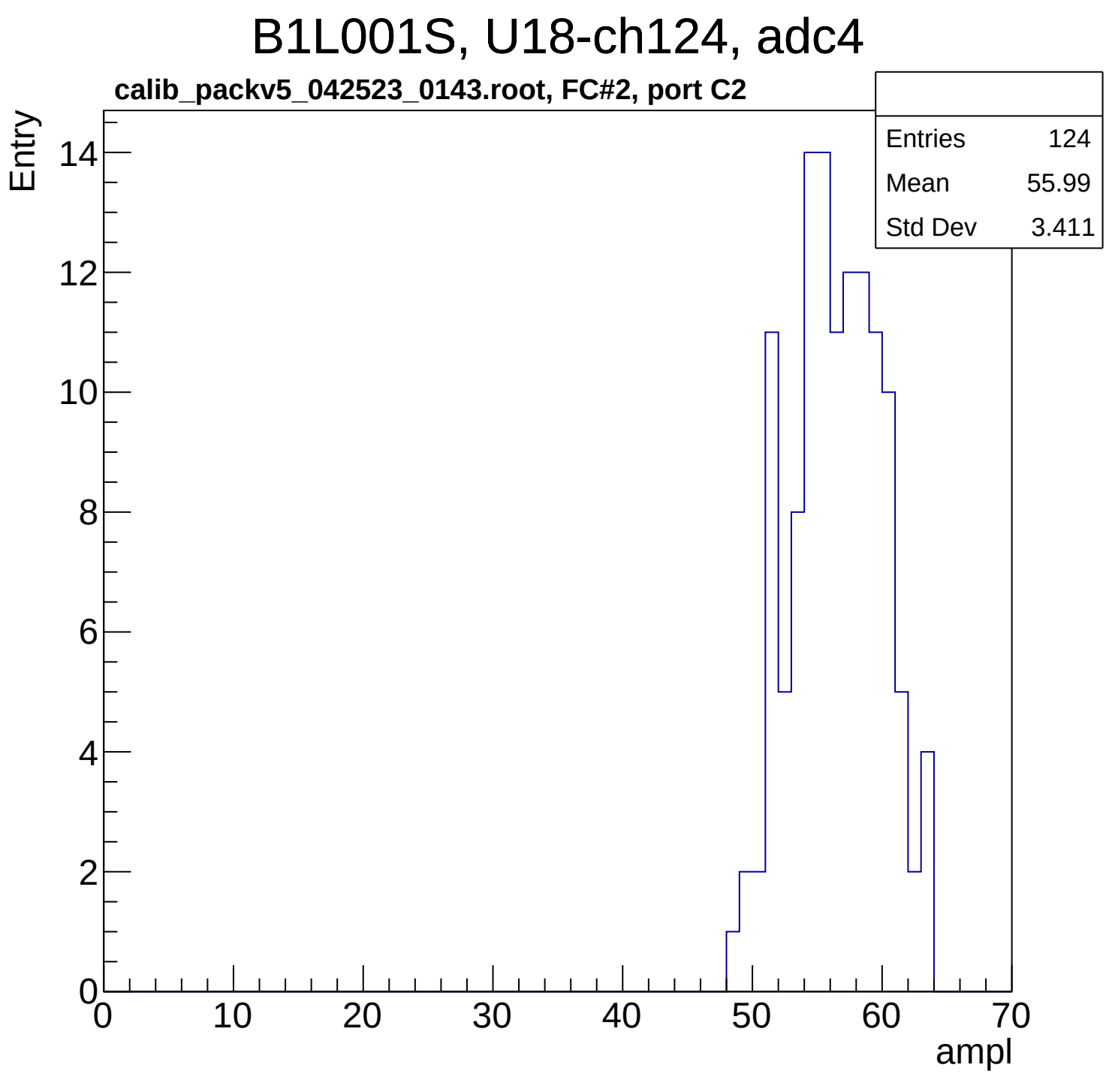

B1L001S, U18-ch123, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

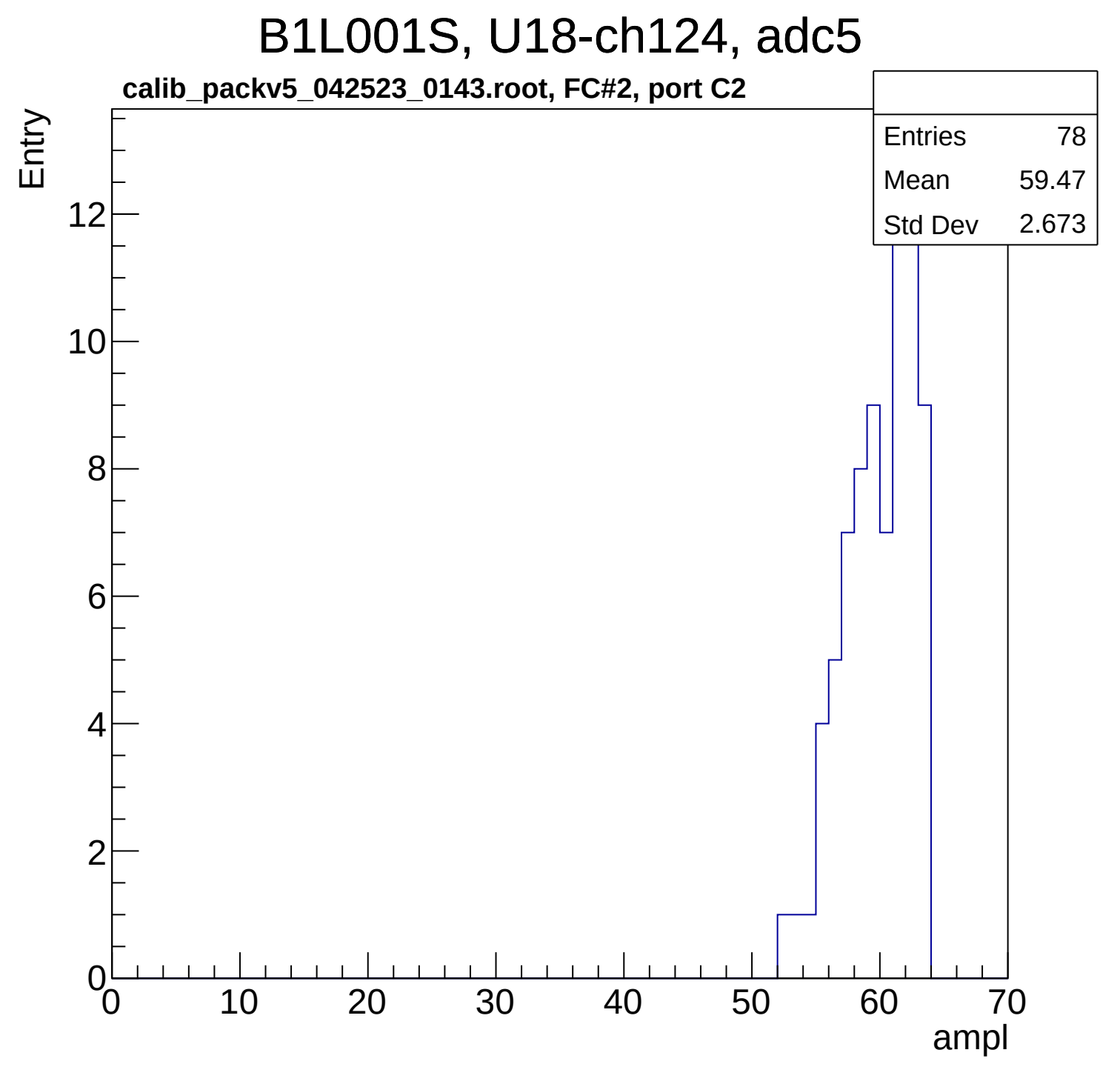

B1L001S, U18-ch124, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 142
Mean 29.19
Std Dev 4.78
Gaus mean : 29.9364
Gaus Width: 3.3213
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

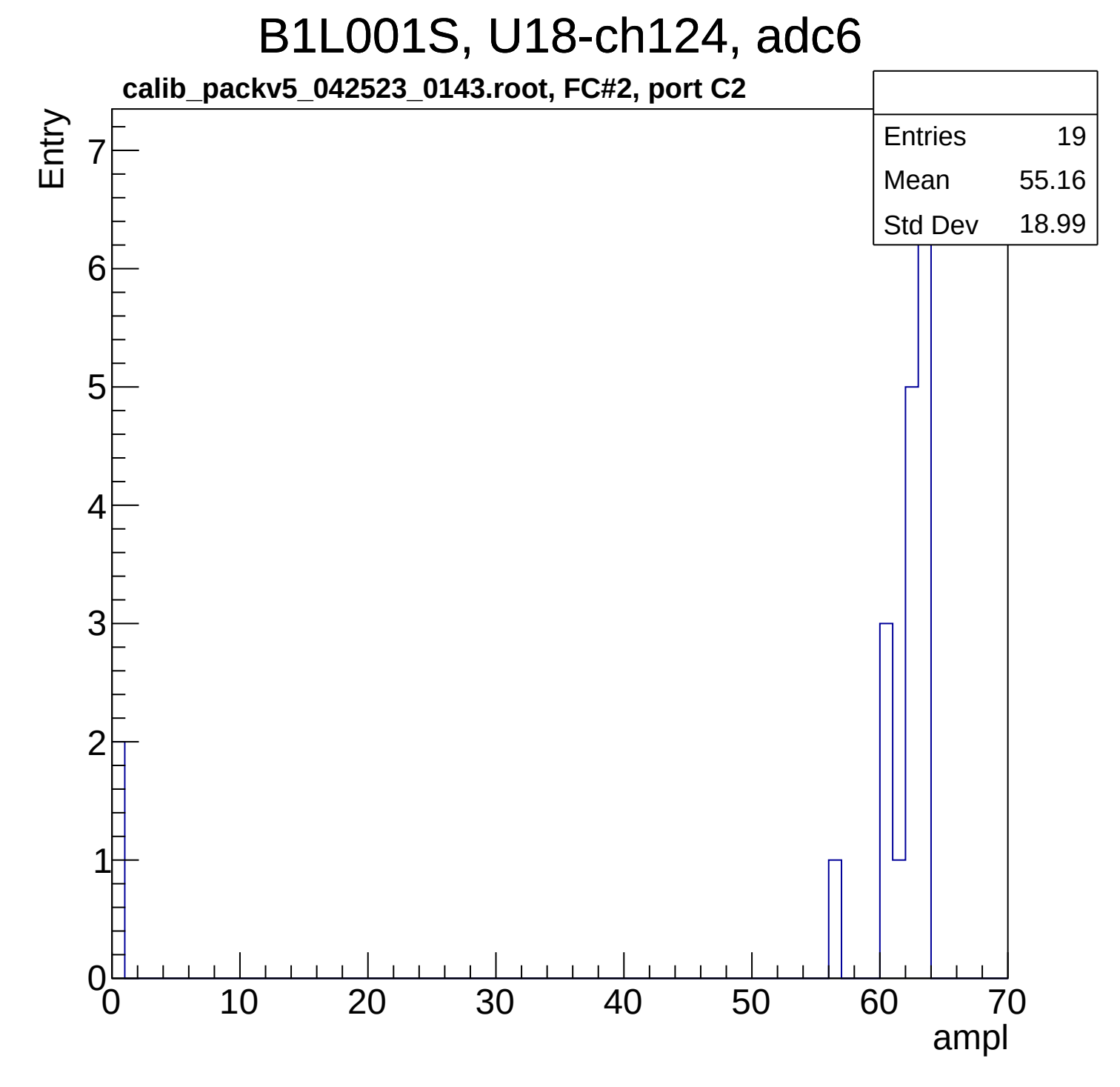

B1L001S, U18-ch124, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 142
Mean 36.77
Std Dev 3.271
Gaus mean : 37.2747
Gaus Width: 3.1908
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

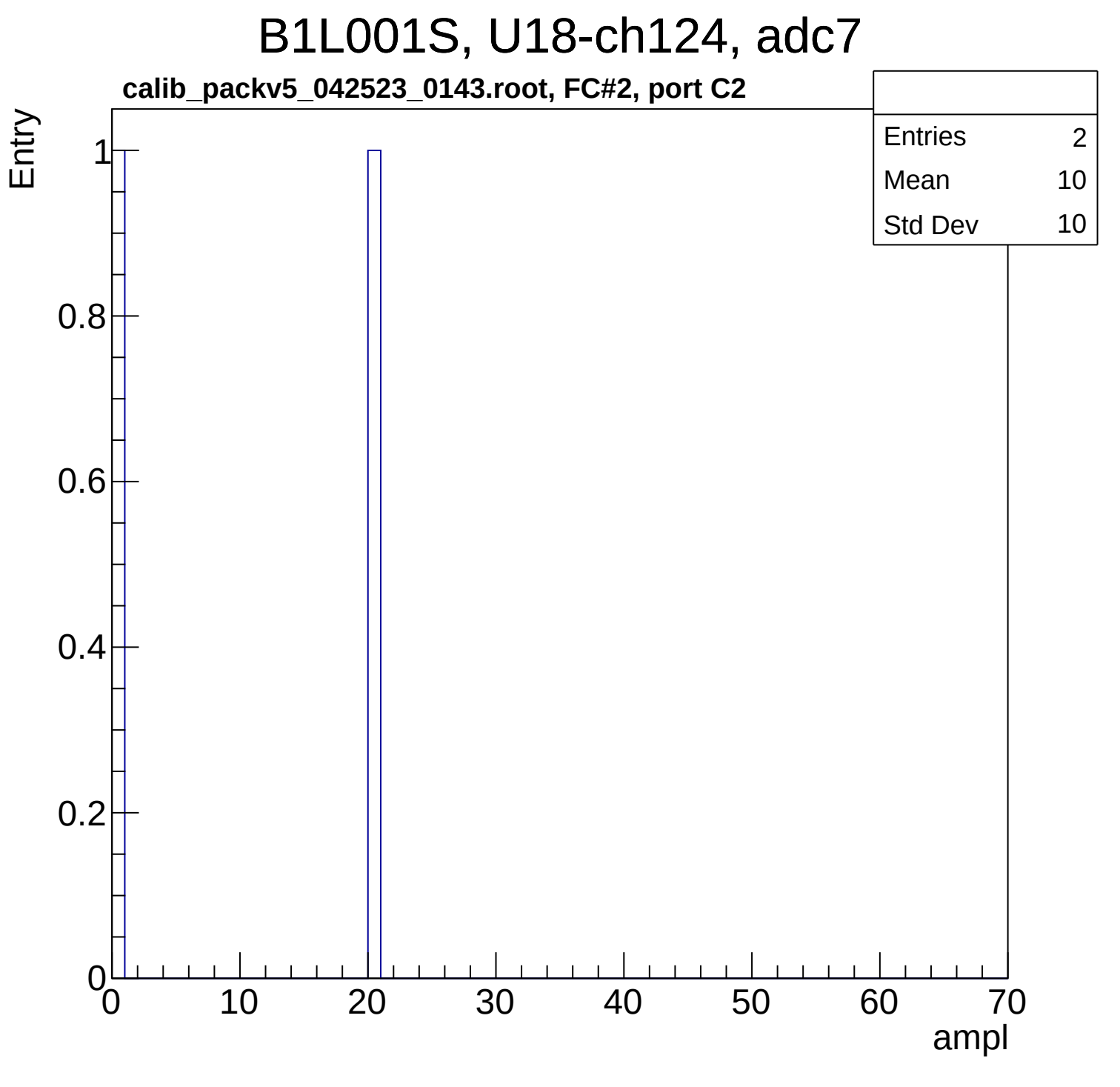

B1L001S, U18-ch124, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 112
Mean 42.84
Std Dev 2.999
Gaus mean : 43.3743
Gaus Width: 2.8725
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

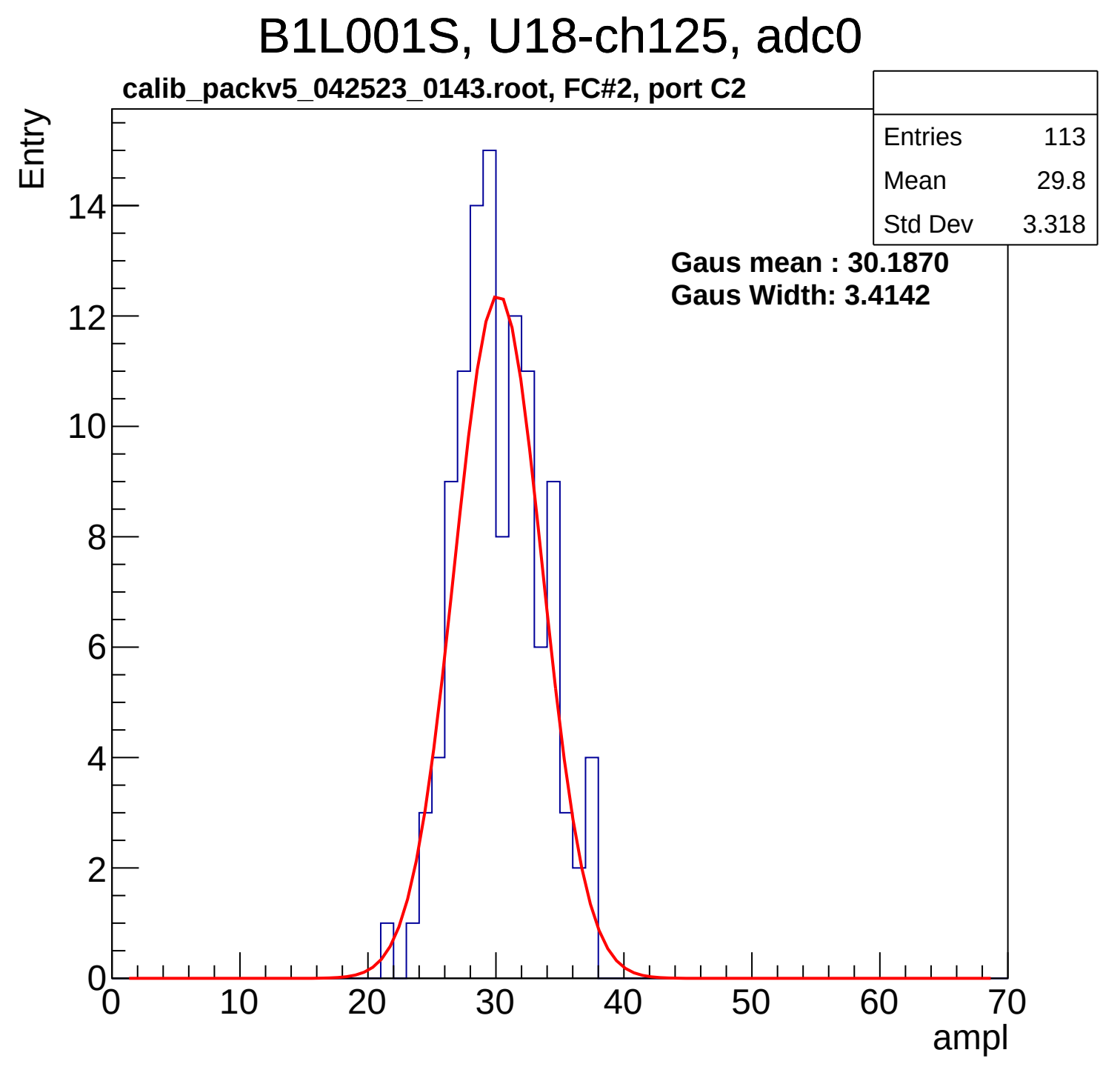

B1L001S, U18-ch124, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 134
Mean 49.39
Std Dev 3.269
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

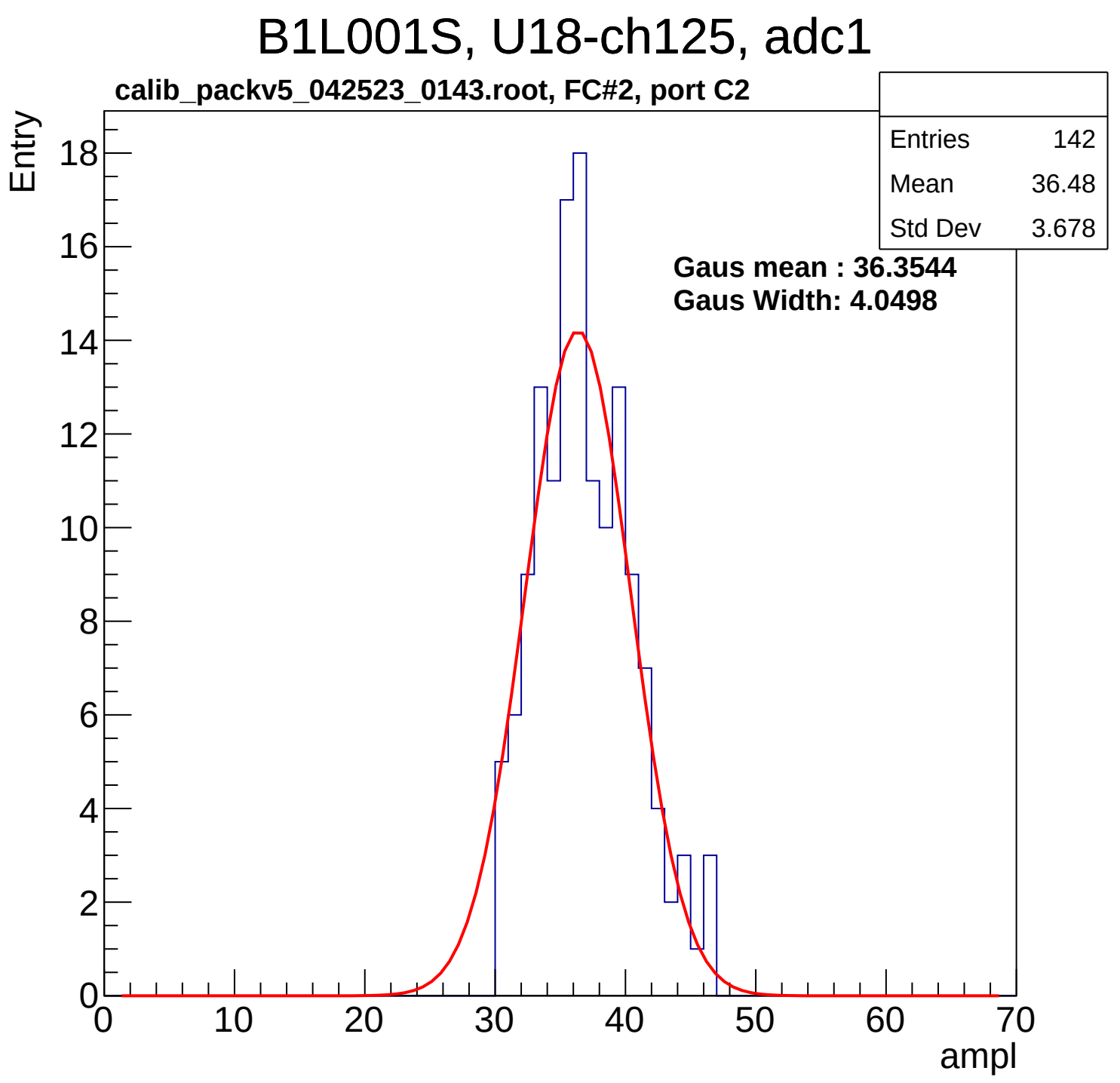

B1L001S, U18-ch124, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 124
Mean 55.99
Std Dev 3.411
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

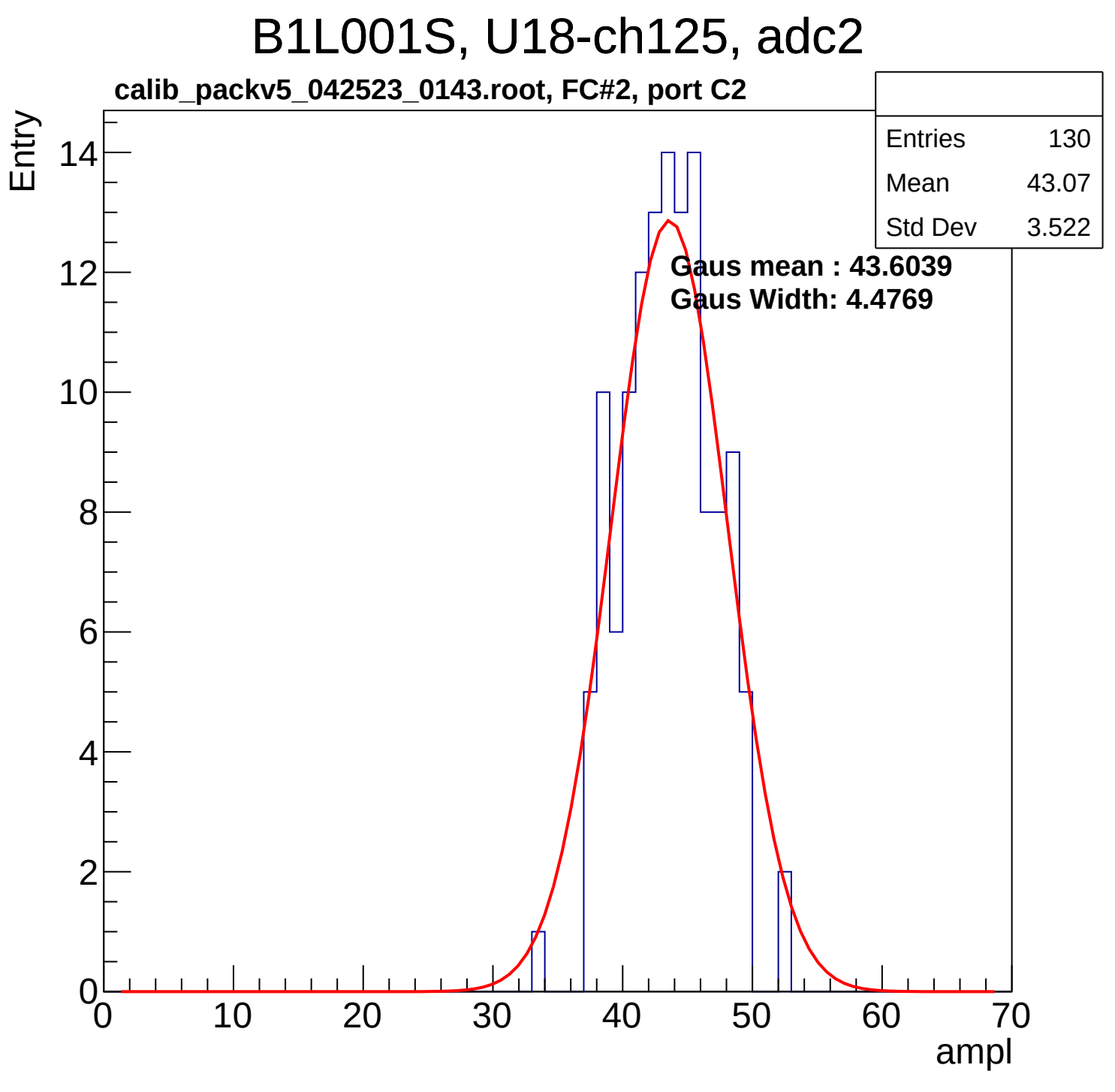

B1L001S, U18-ch124, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 78
Mean 59.47
Std Dev 2.673
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl

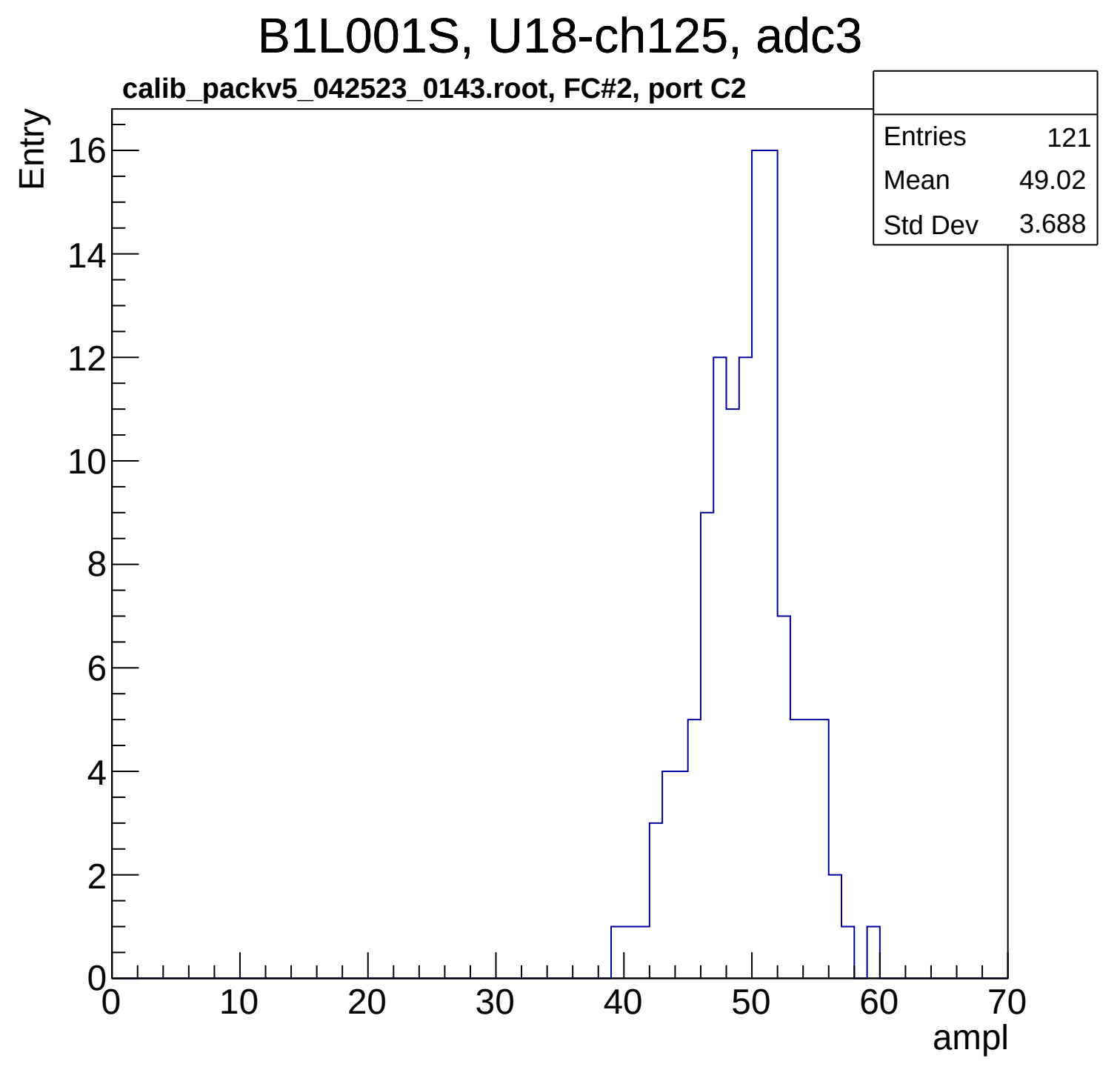

B1L001S, U18-ch124, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 19
Mean 55.16
Std Dev 18.99
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

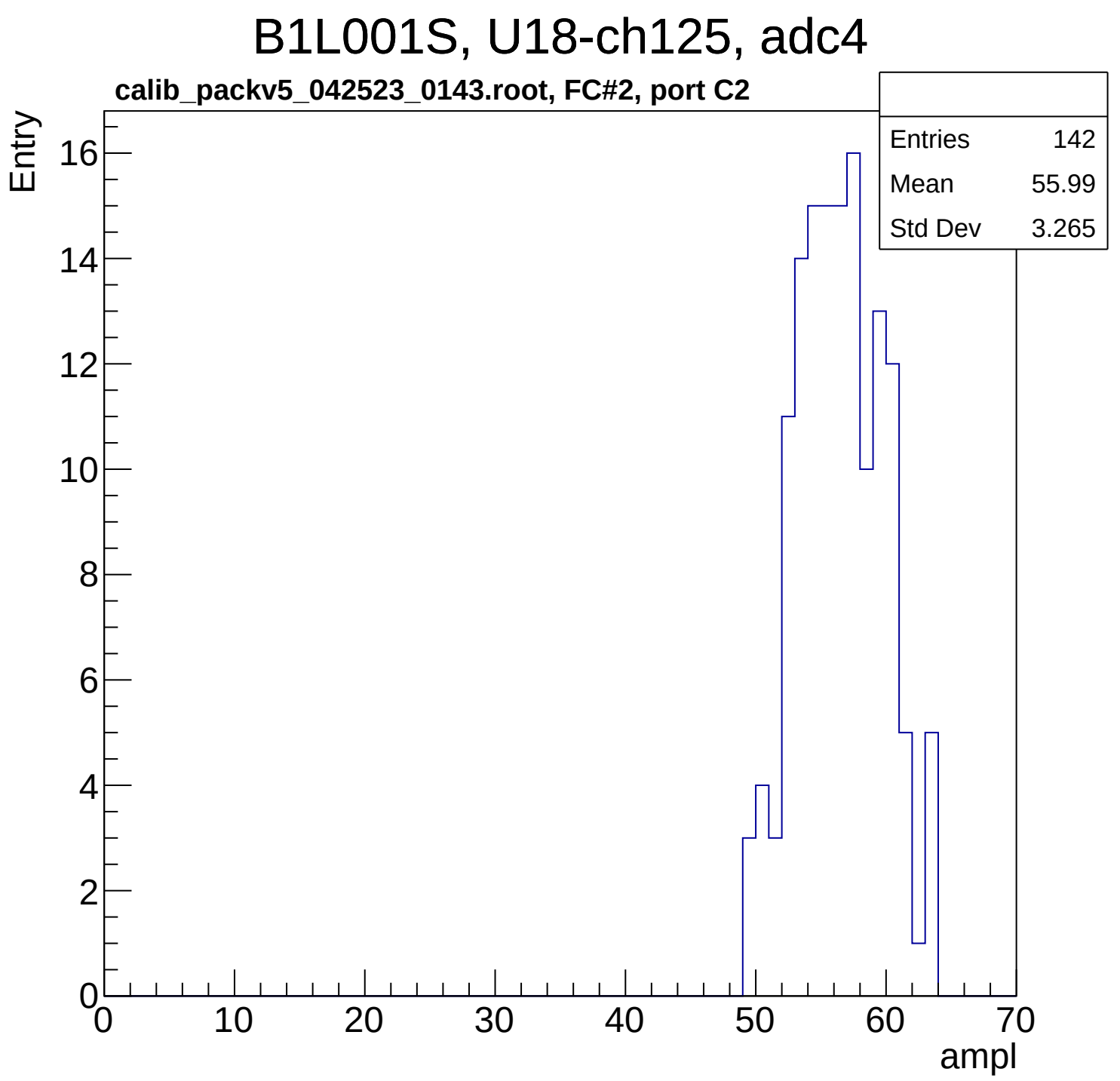

B1L001S, U18-ch124, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 10
Std Dev 10
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

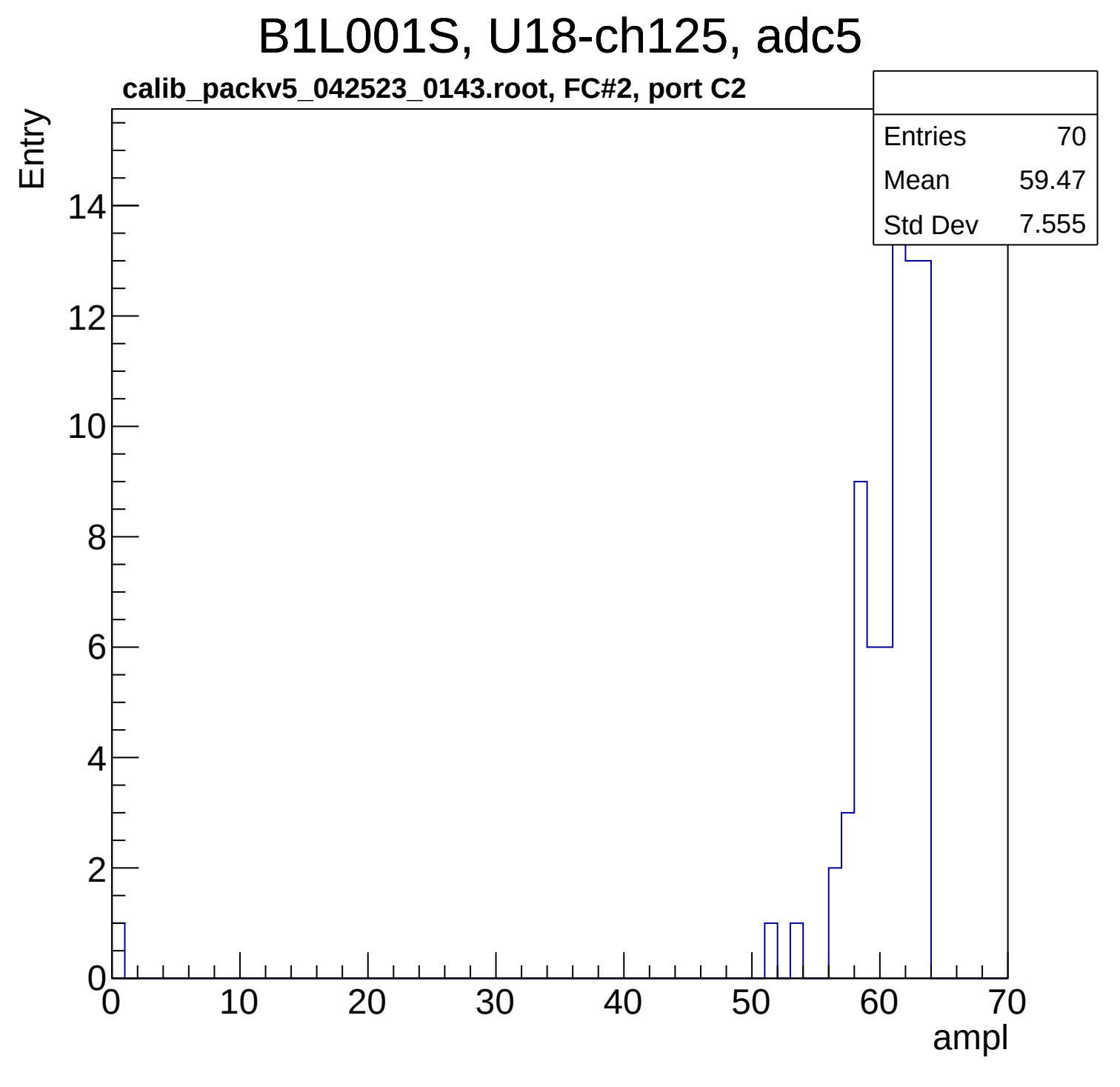

B1L001S, U18-ch125, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 113
Mean 29.8
Std Dev 3.318
Gaus mean : 30.1870
Gaus Width: 3.4142
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

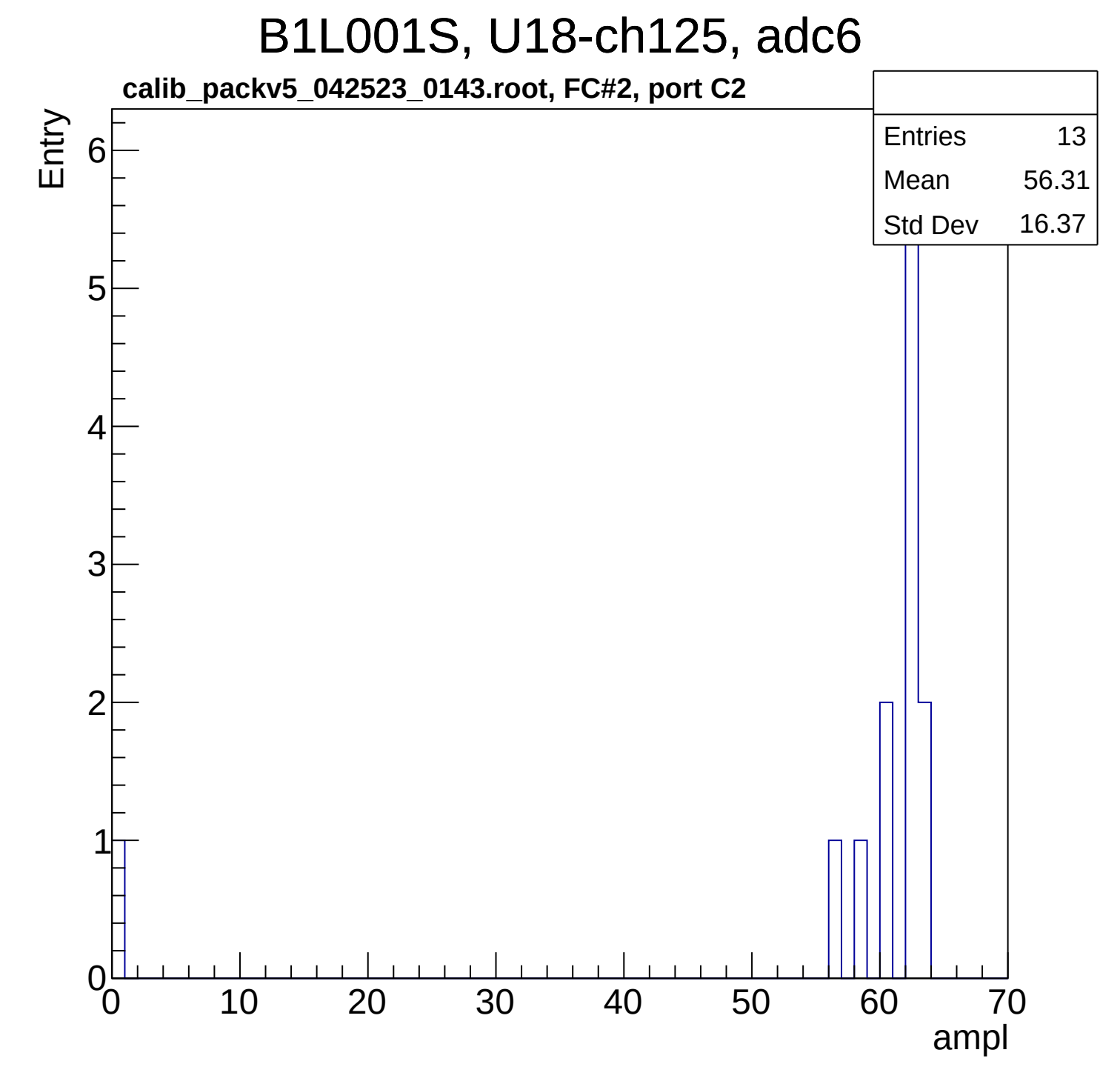

B1L001S, U18-ch125, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 142
Mean 36.48
Std Dev 3.678
Gaus mean : 36.3544
Gaus Width: 4.0498
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

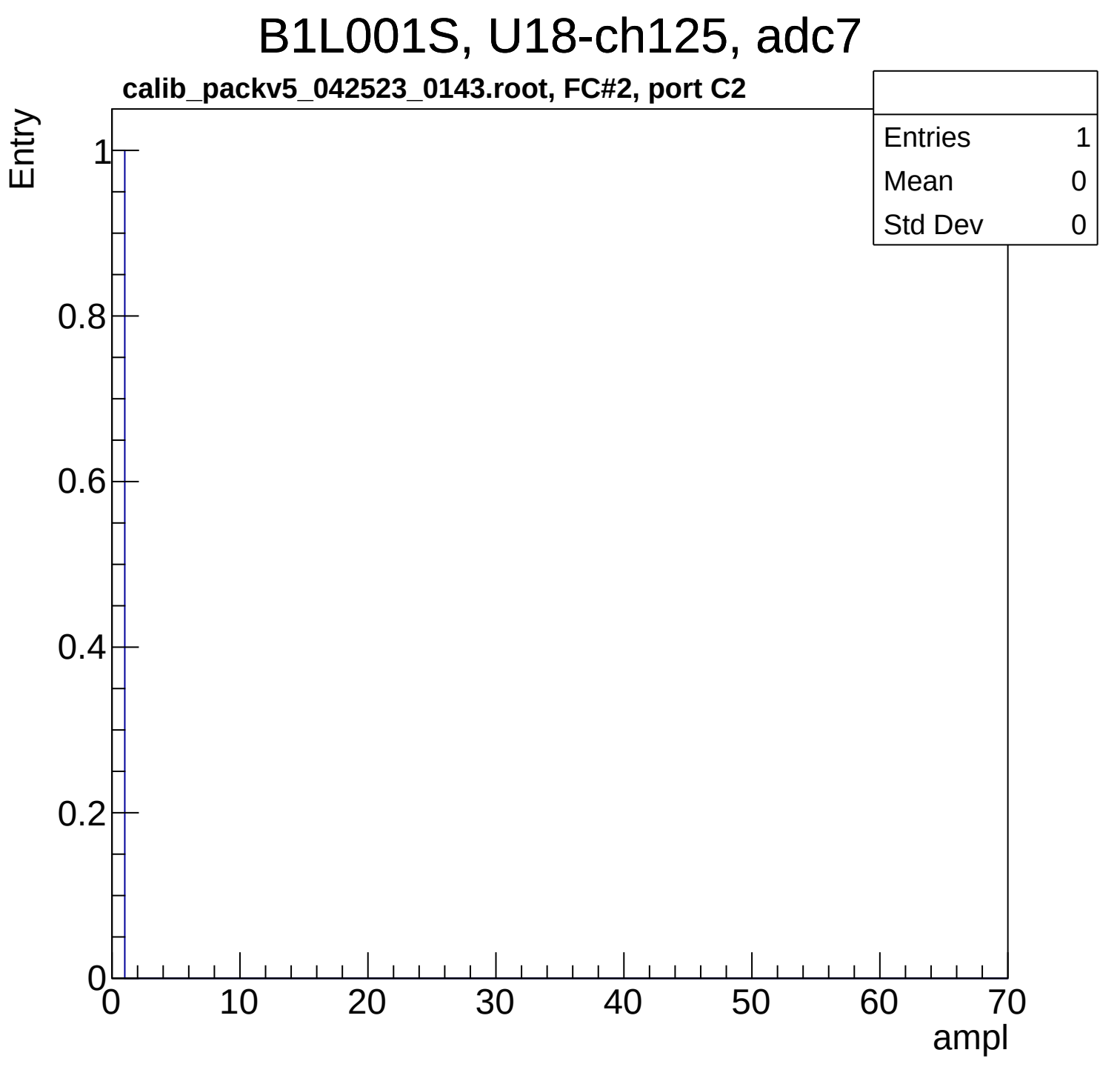

B1L001S, U18-ch125, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 130
Mean 43.07
Std Dev 3.522
Gaus mean : 43.6039
Gaus Width: 4.4769
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

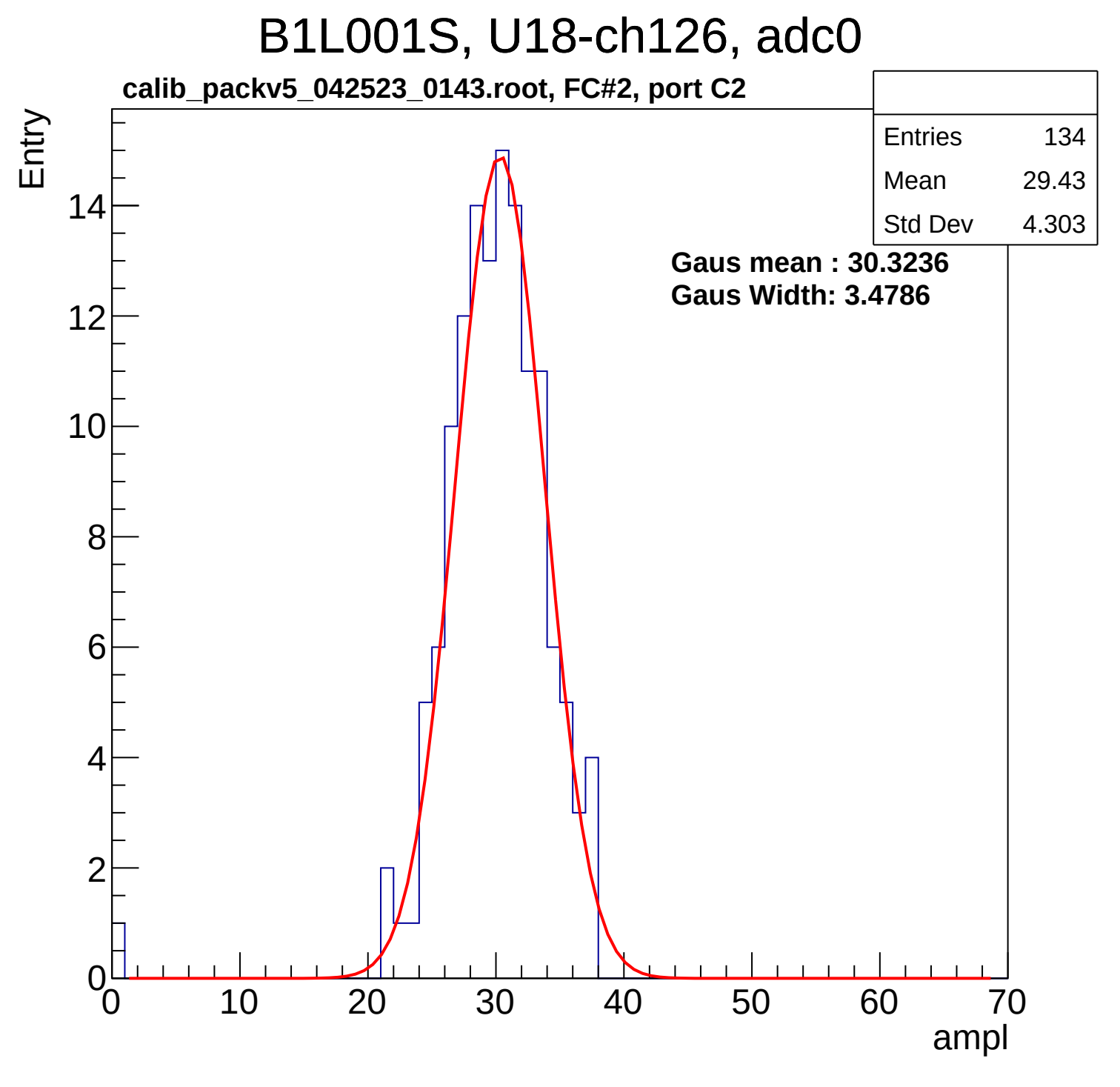

B1L001S, U18-ch125, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 121
Mean 49.02
Std Dev 3.688
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

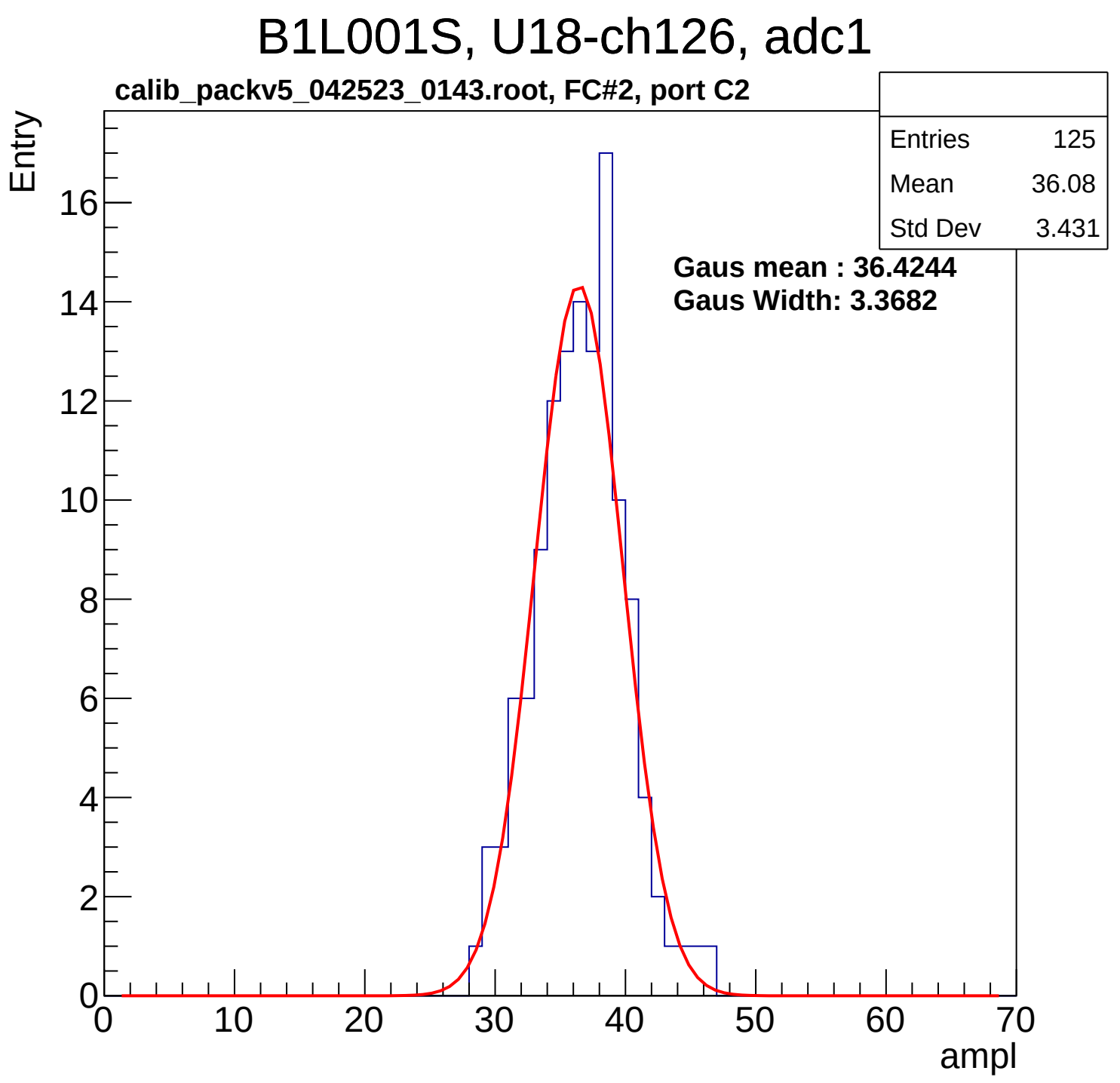

B1L001S, U18-ch125, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 142
Mean 55.99
Std Dev 3.265
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

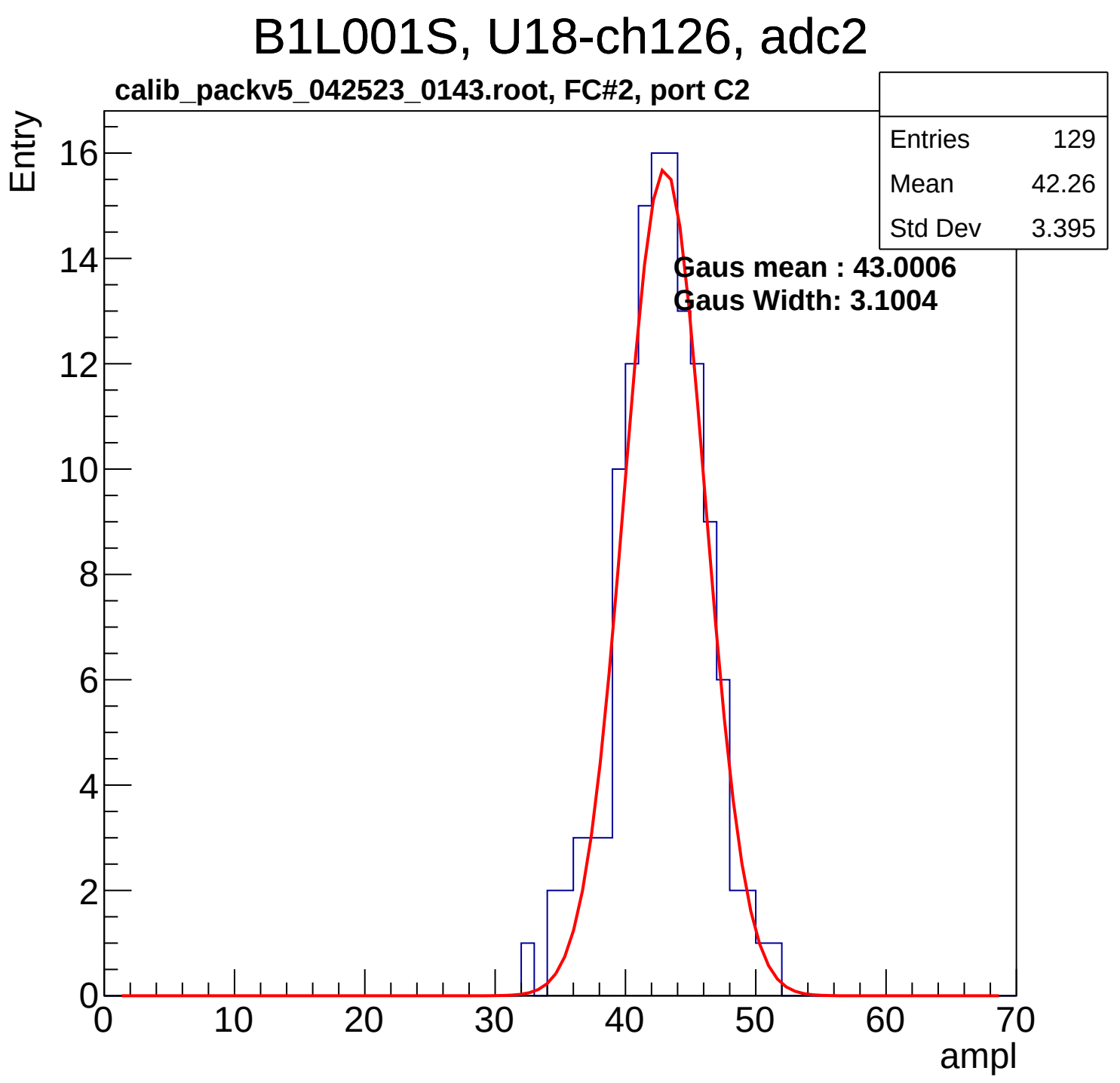

B1L001S, U18-ch125, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 70
Mean 59.47
Std Dev 7.555
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl

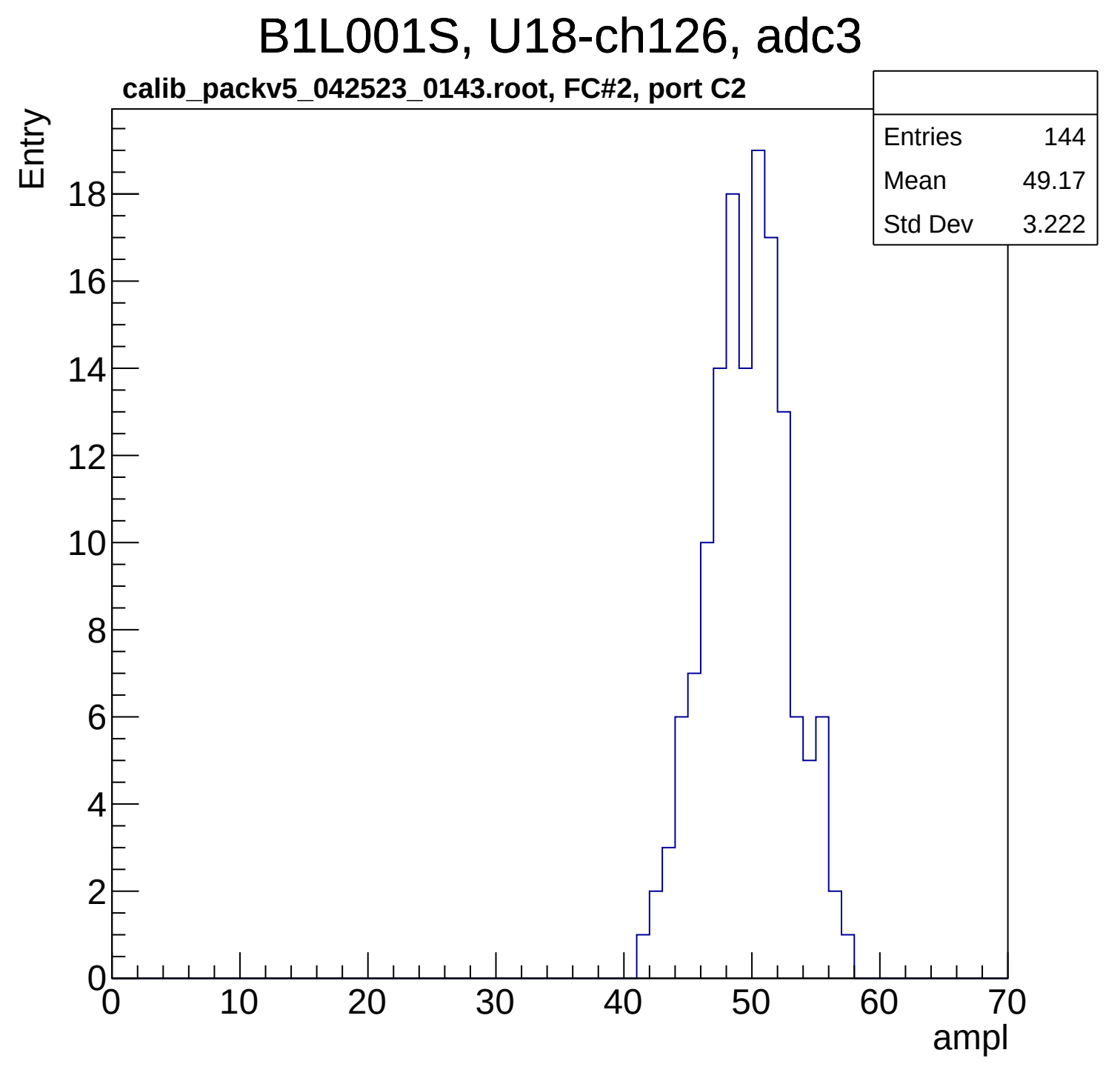

B1L001S, U18-ch125, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 13
Mean 56.31
Std Dev 16.37
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

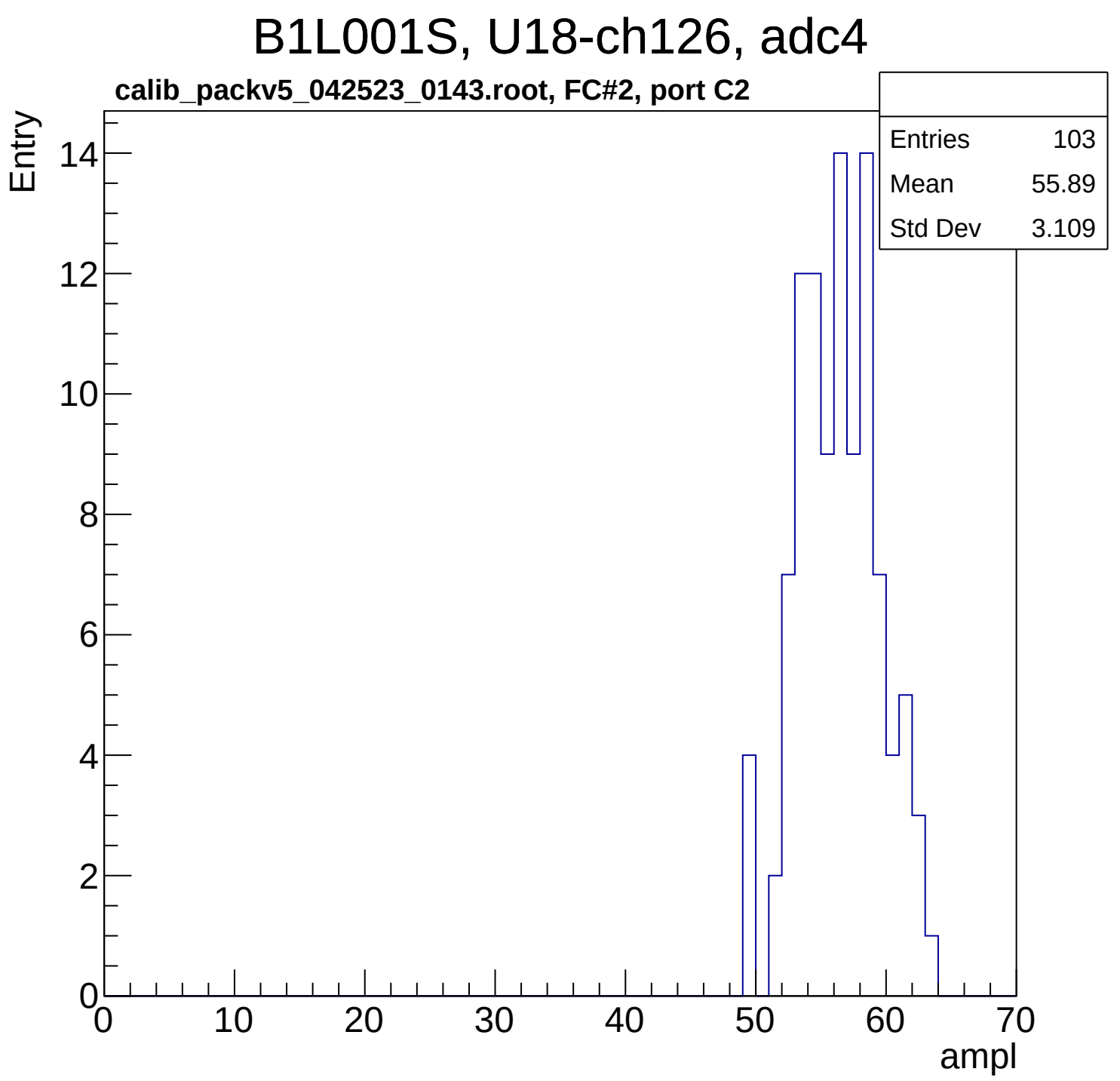

B1L001S, U18-ch125, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

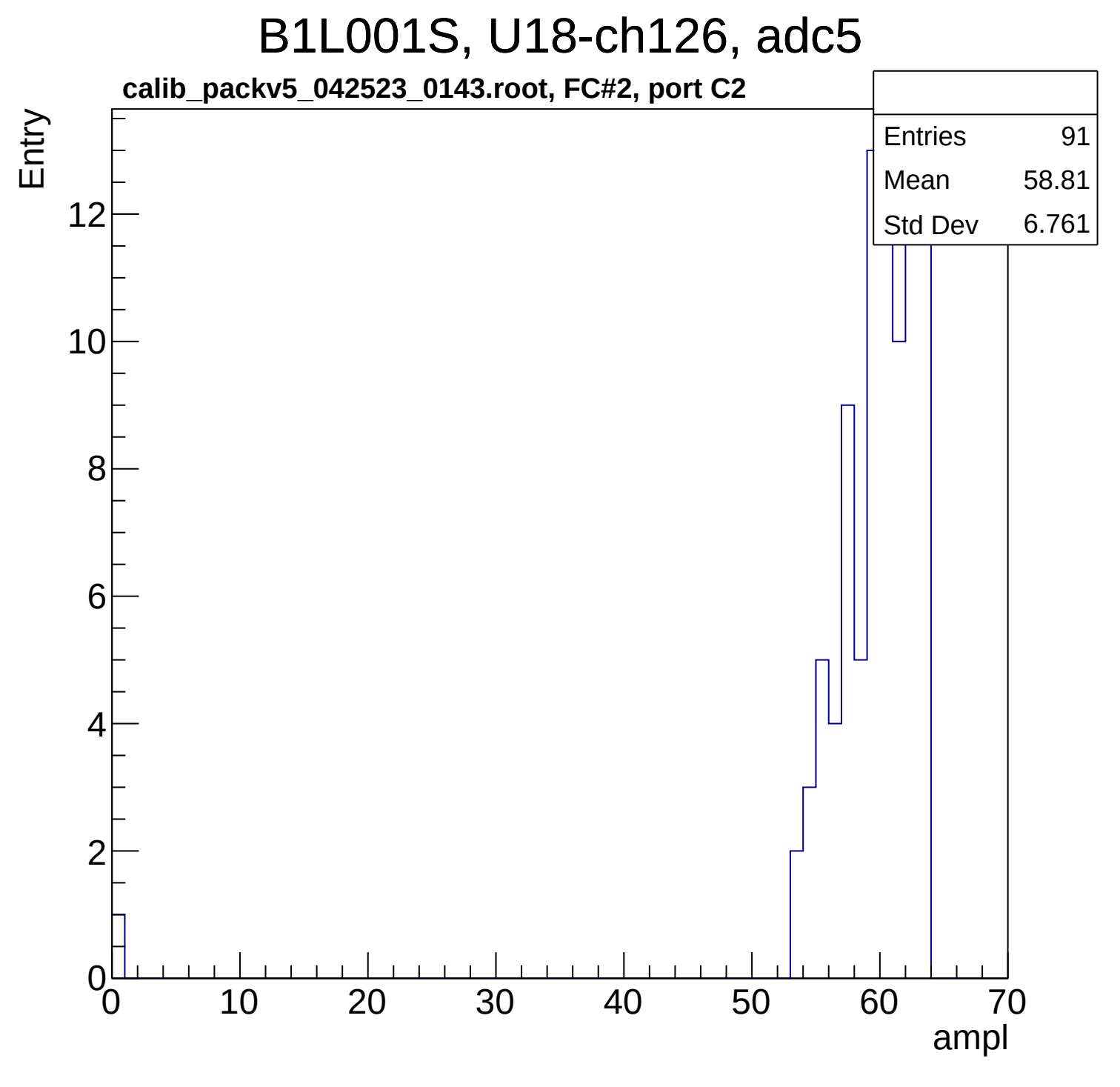

B1L001S, U18-ch126, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 134
Mean 29.43
Std Dev 4.303
Gaus mean : 30.3236
Gaus Width: 3.4786
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

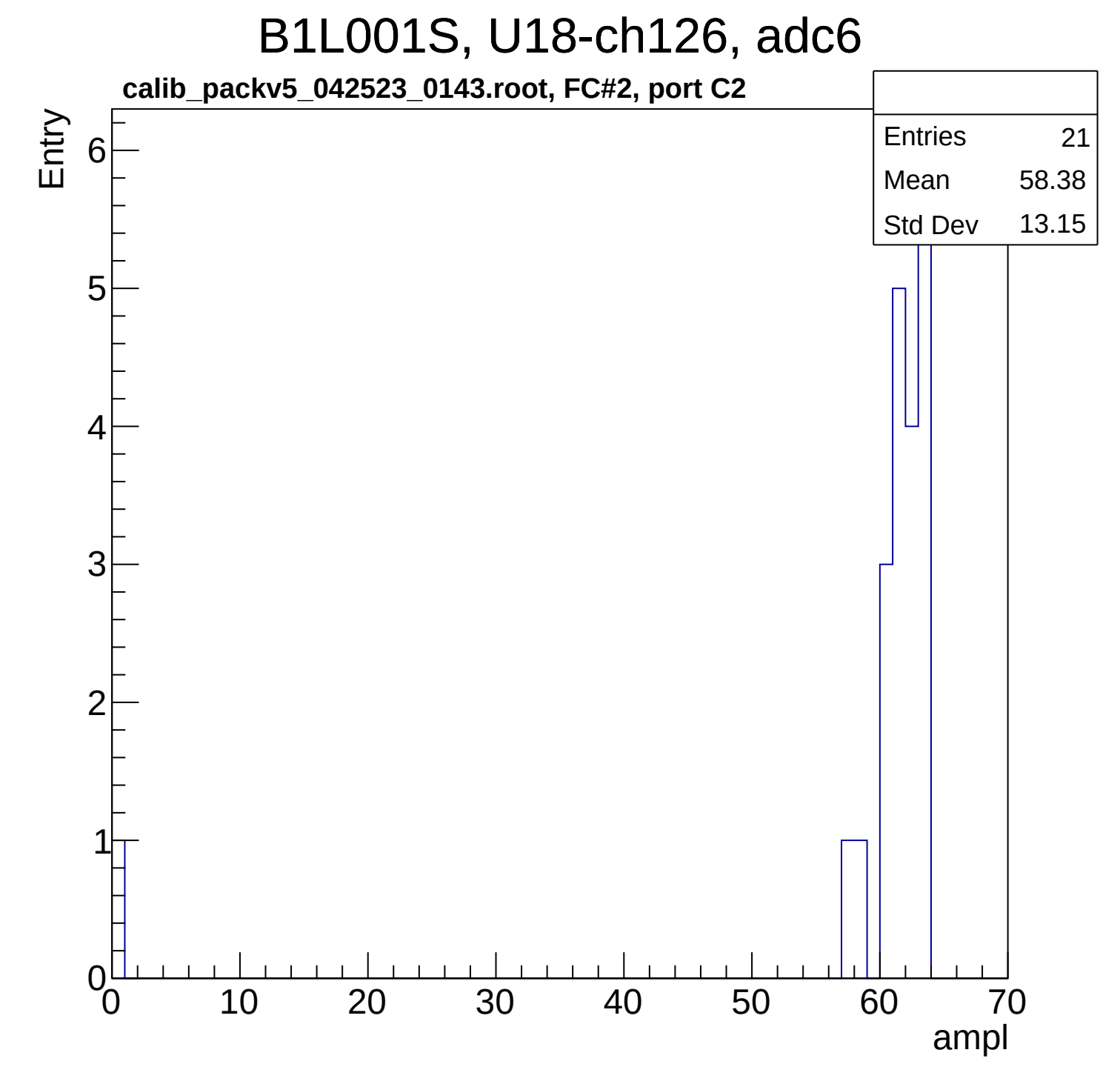

B1L001S, U18-ch126, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 125
Mean 36.08
Std Dev 3.431
Gaus mean : 36.4244
Gaus Width: 3.3682
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

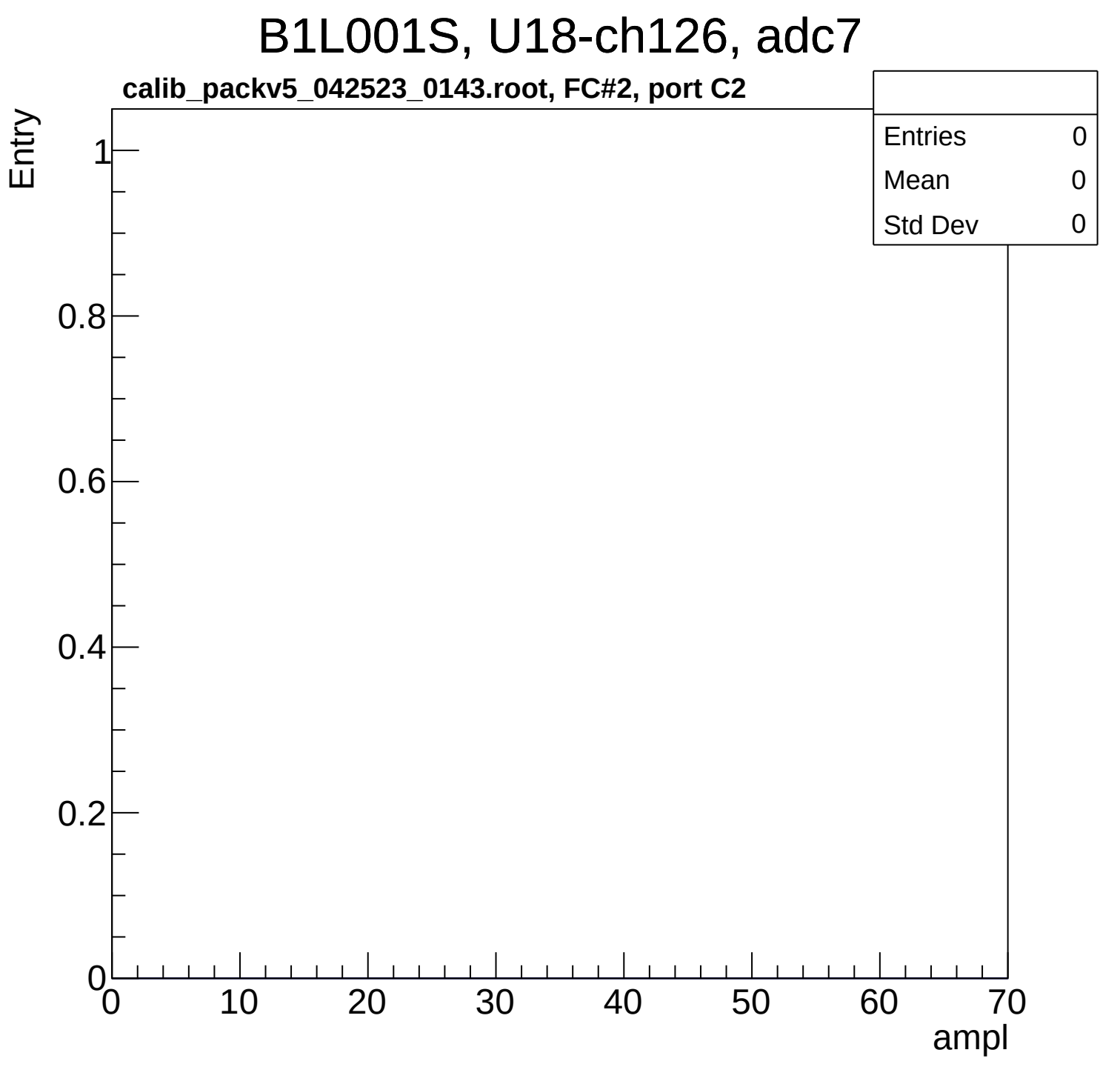

B1L001S, U18-ch126, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 129
Mean 42.26
Std Dev 3.395
Gaus mean : 43.0006
Gaus Width: 3.1004
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

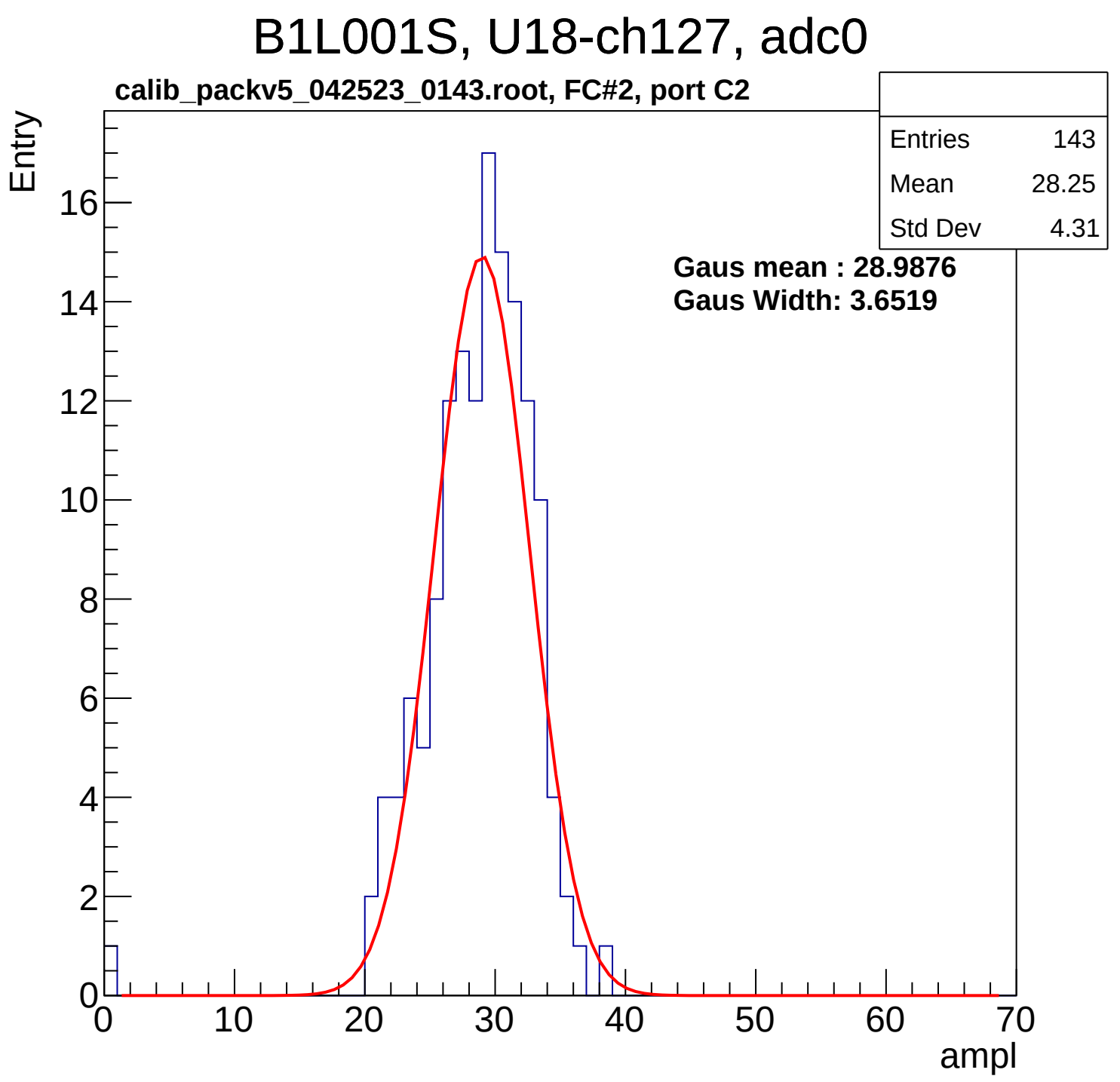

B1L001S, U18-ch126, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 144
Mean 49.17
Std Dev 3.222
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

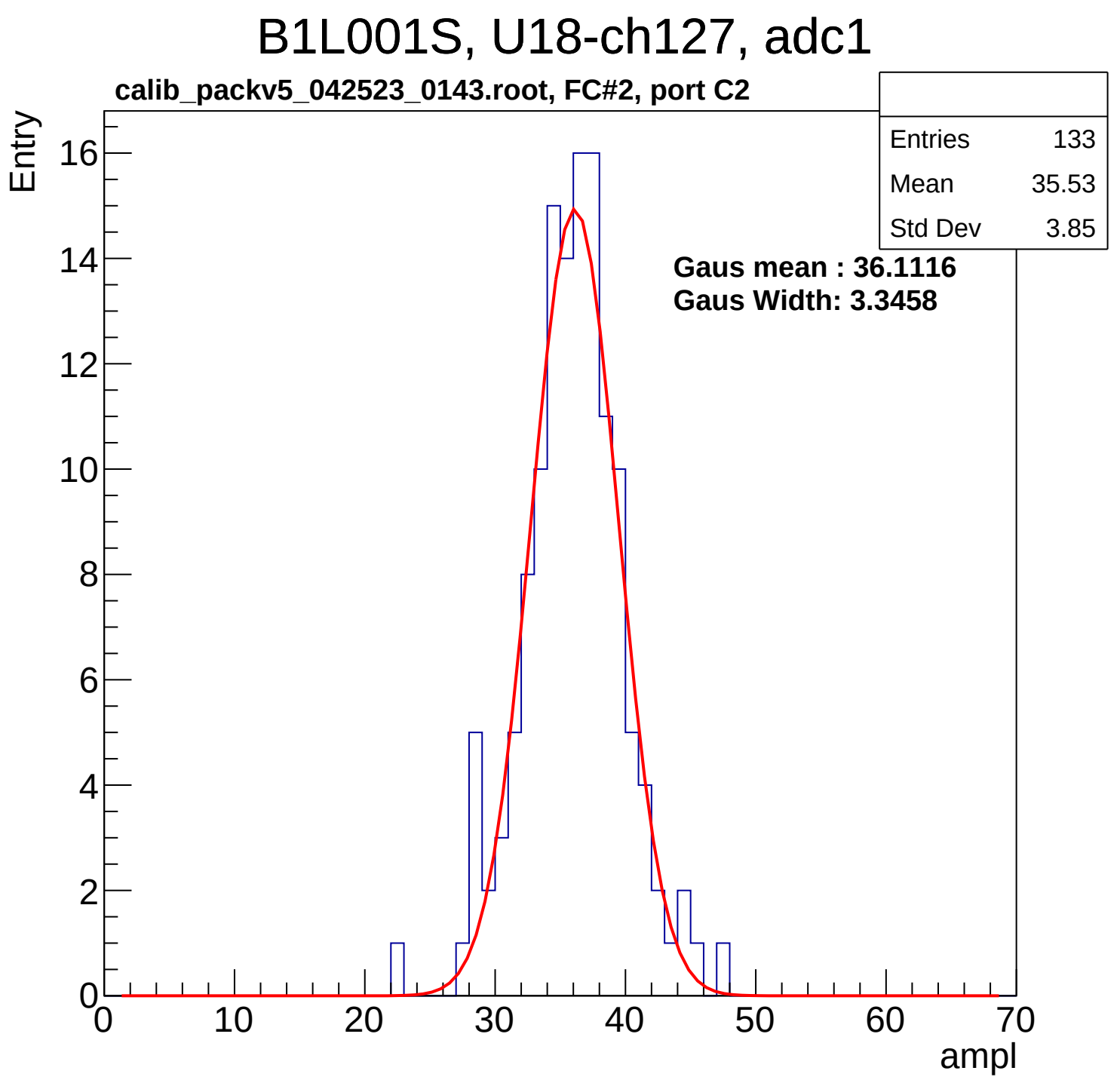

B1L001S, U18-ch126, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 103
Mean 55.89
Std Dev 3.109
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

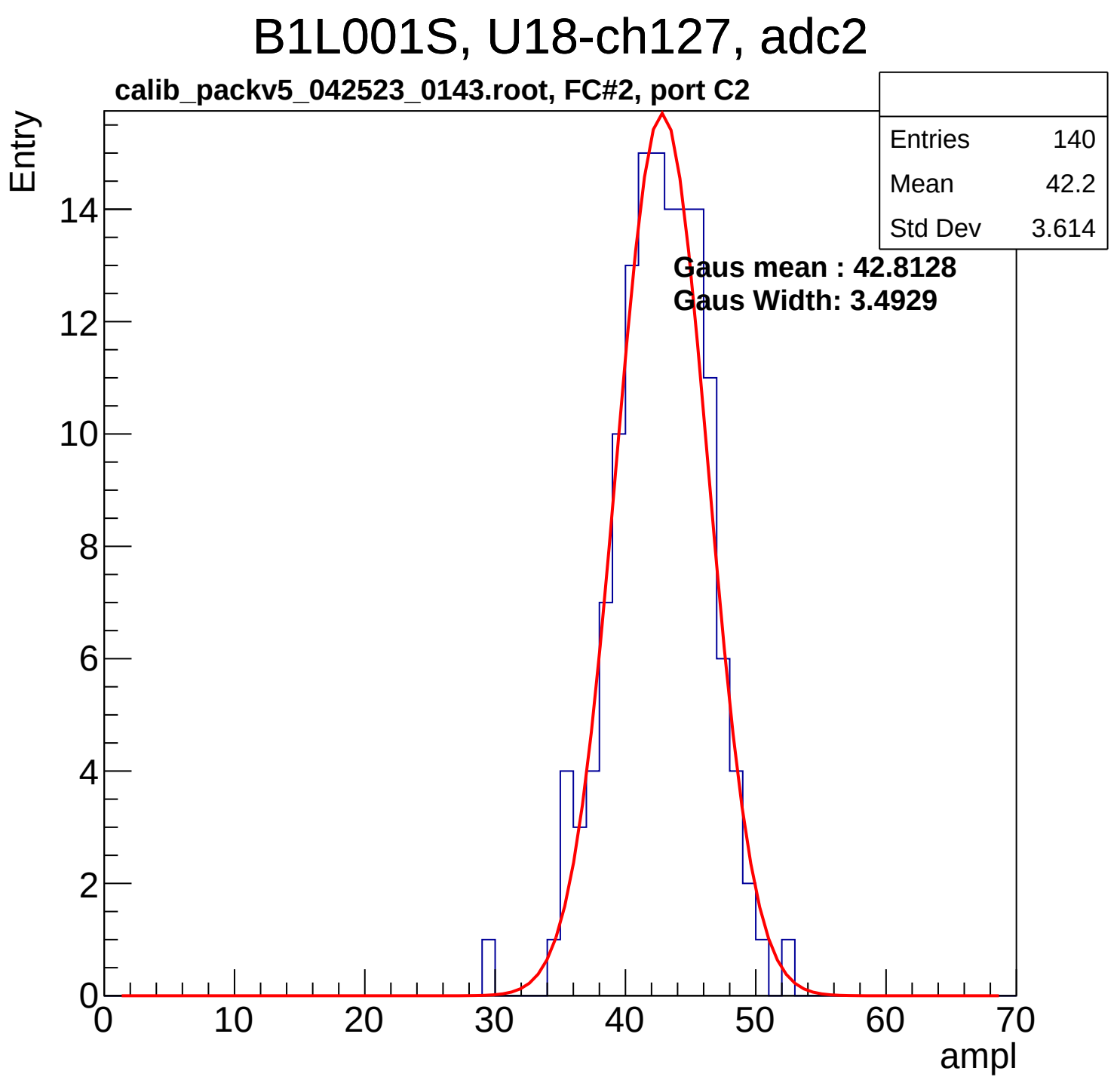

B1L001S, U18-ch126, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 91
Mean 58.81
Std Dev 6.761
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70

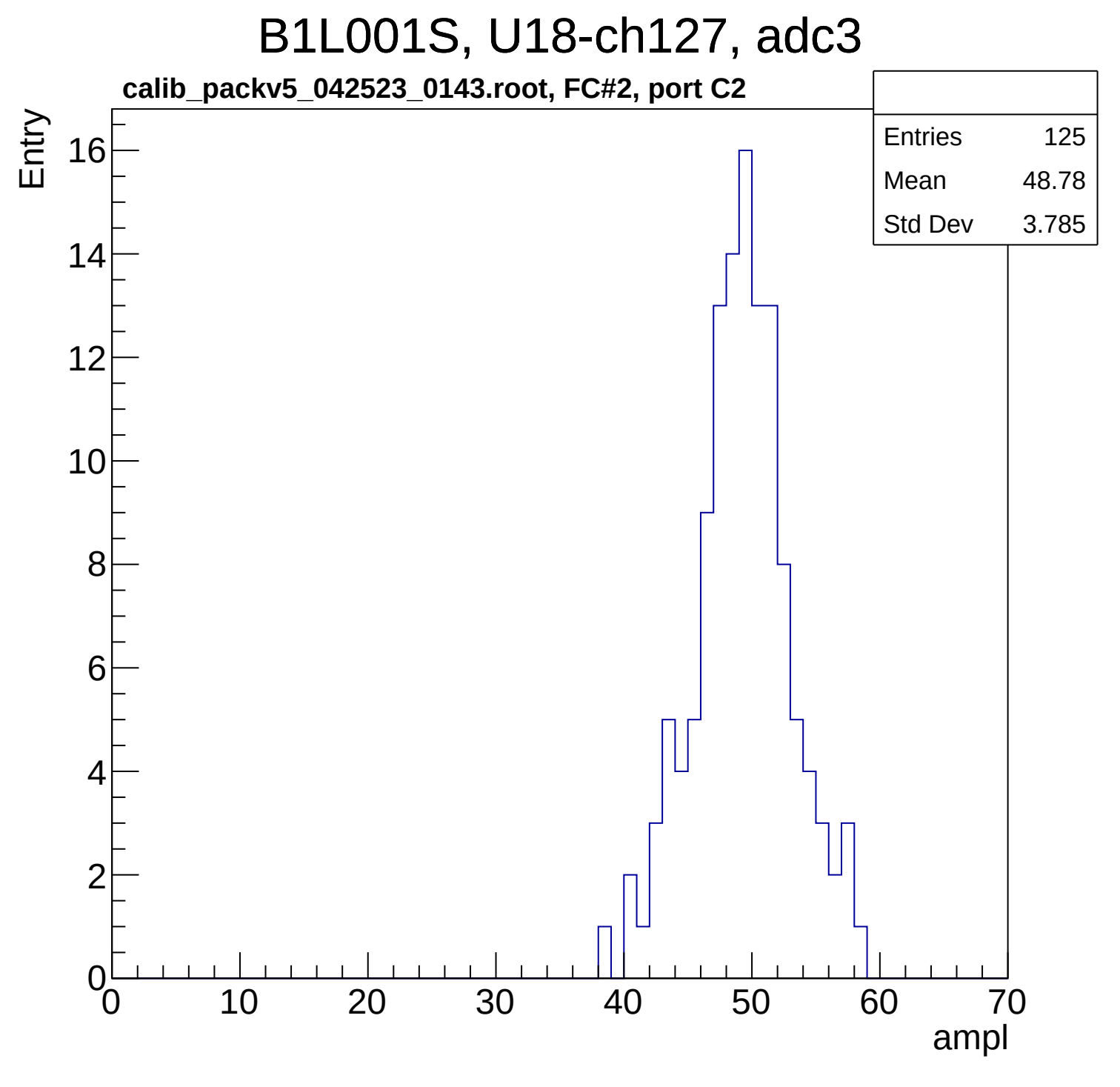

B1L001S, U18-ch126, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 21
Mean 58.38
Std Dev 13.15
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

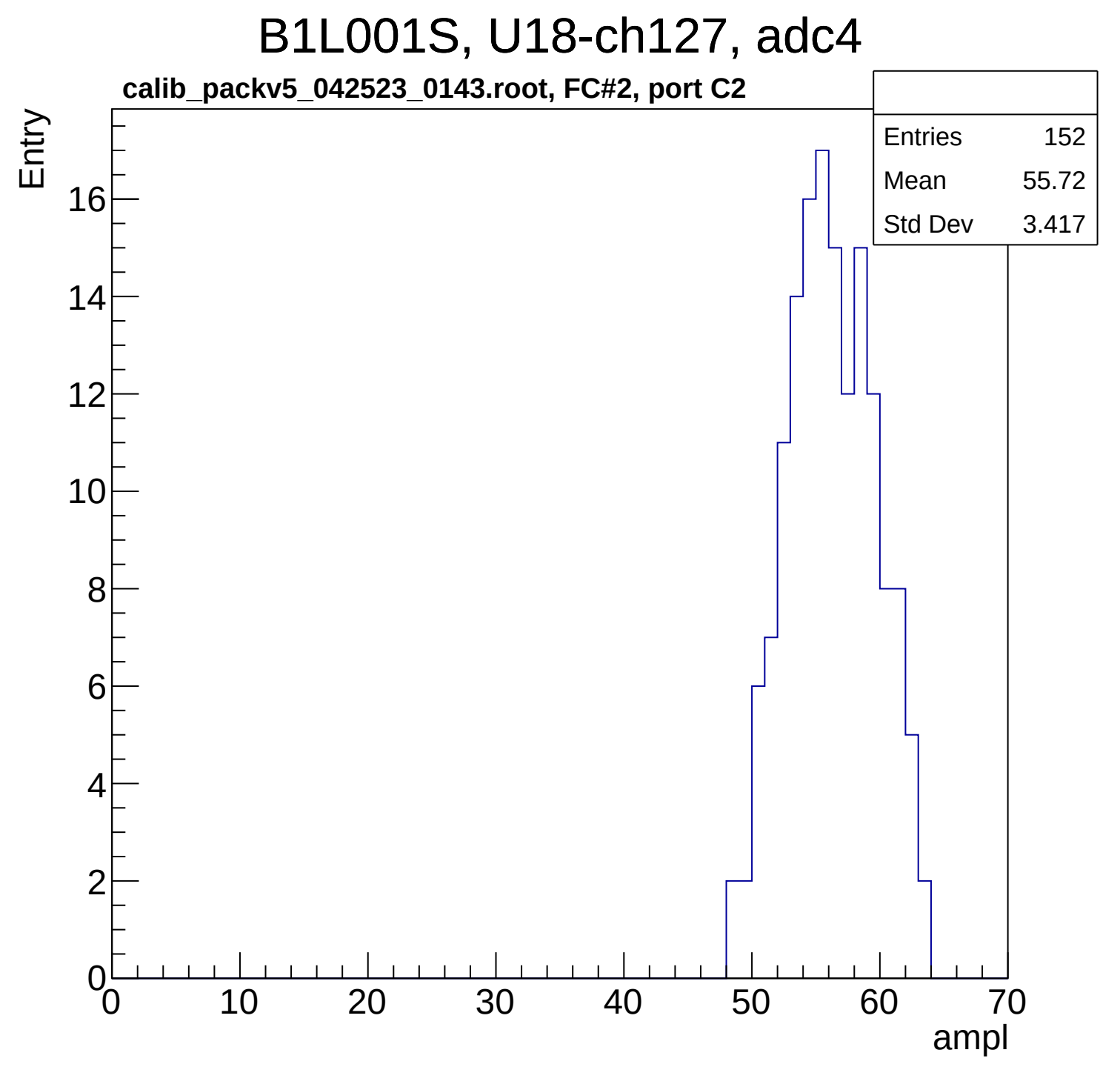

B1L001S, U18-ch126, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

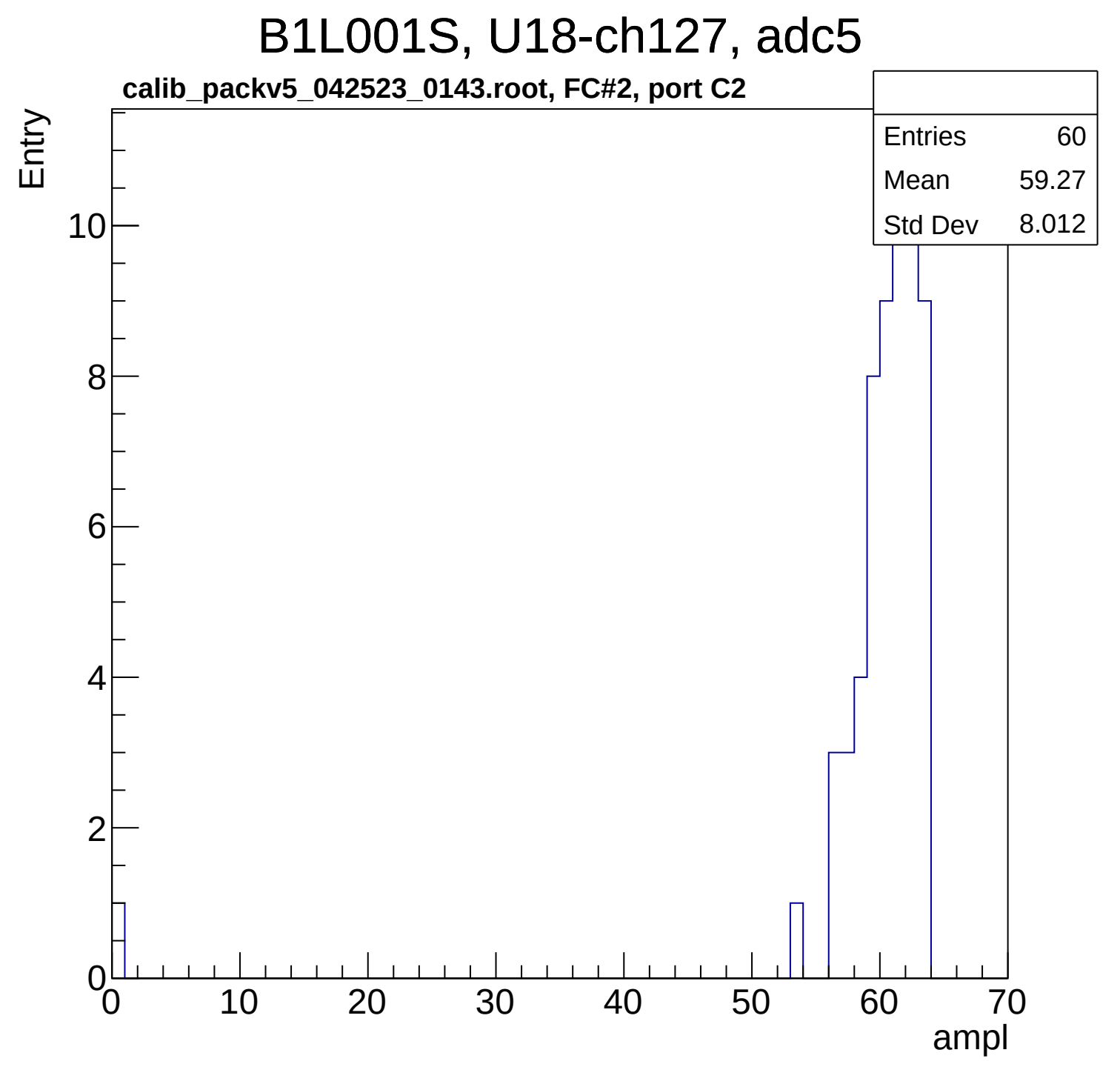

B1L001S, U18-ch127, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 143
Mean 28.25
Std Dev 4.31
Gaus mean : 28.9876
Gaus Width: 3.6519
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

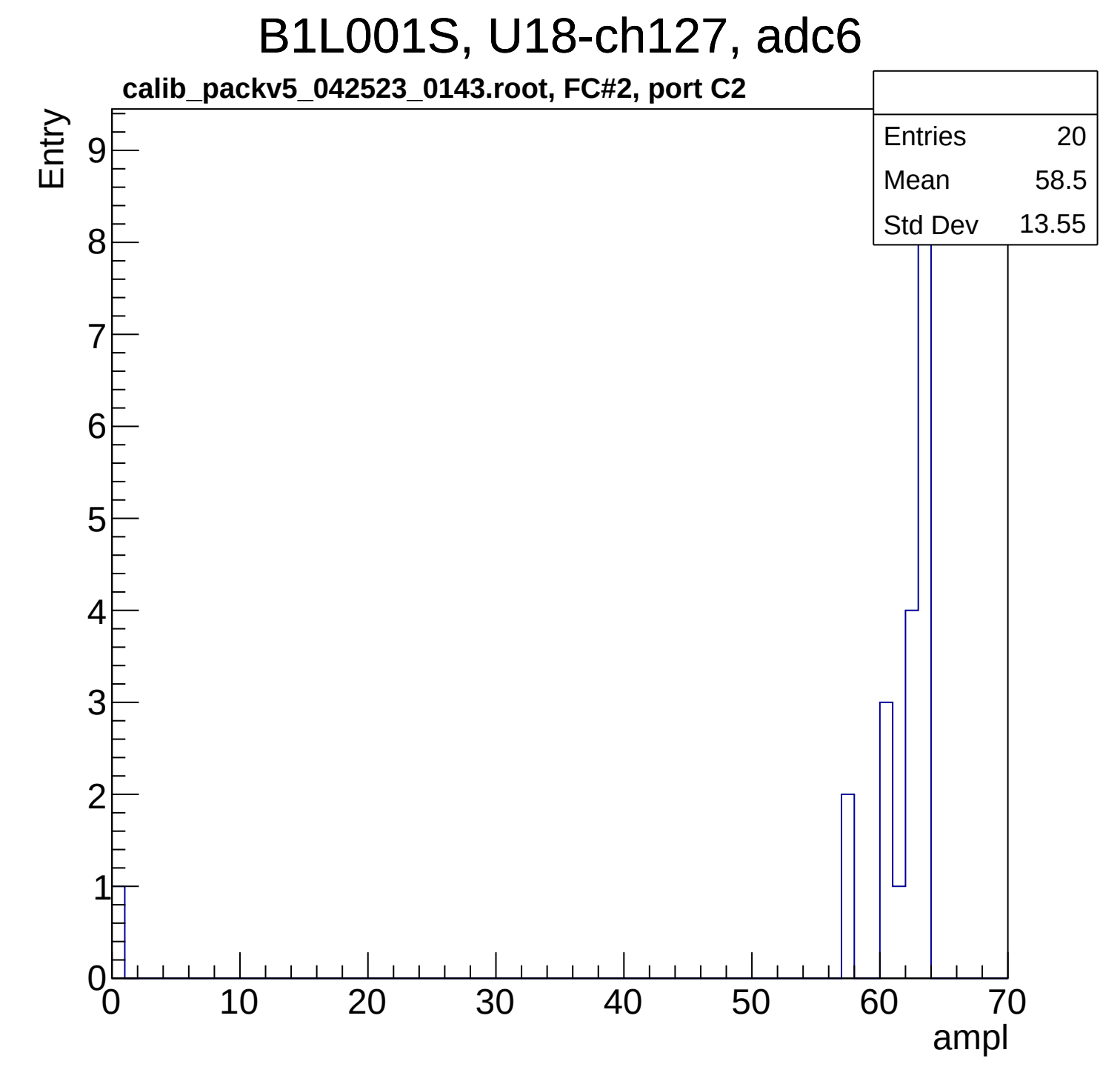

B1L001S, U18-ch127, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 133
Mean 35.53
Std Dev 3.85
Gaus mean : 36.1116
Gaus Width: 3.3458
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

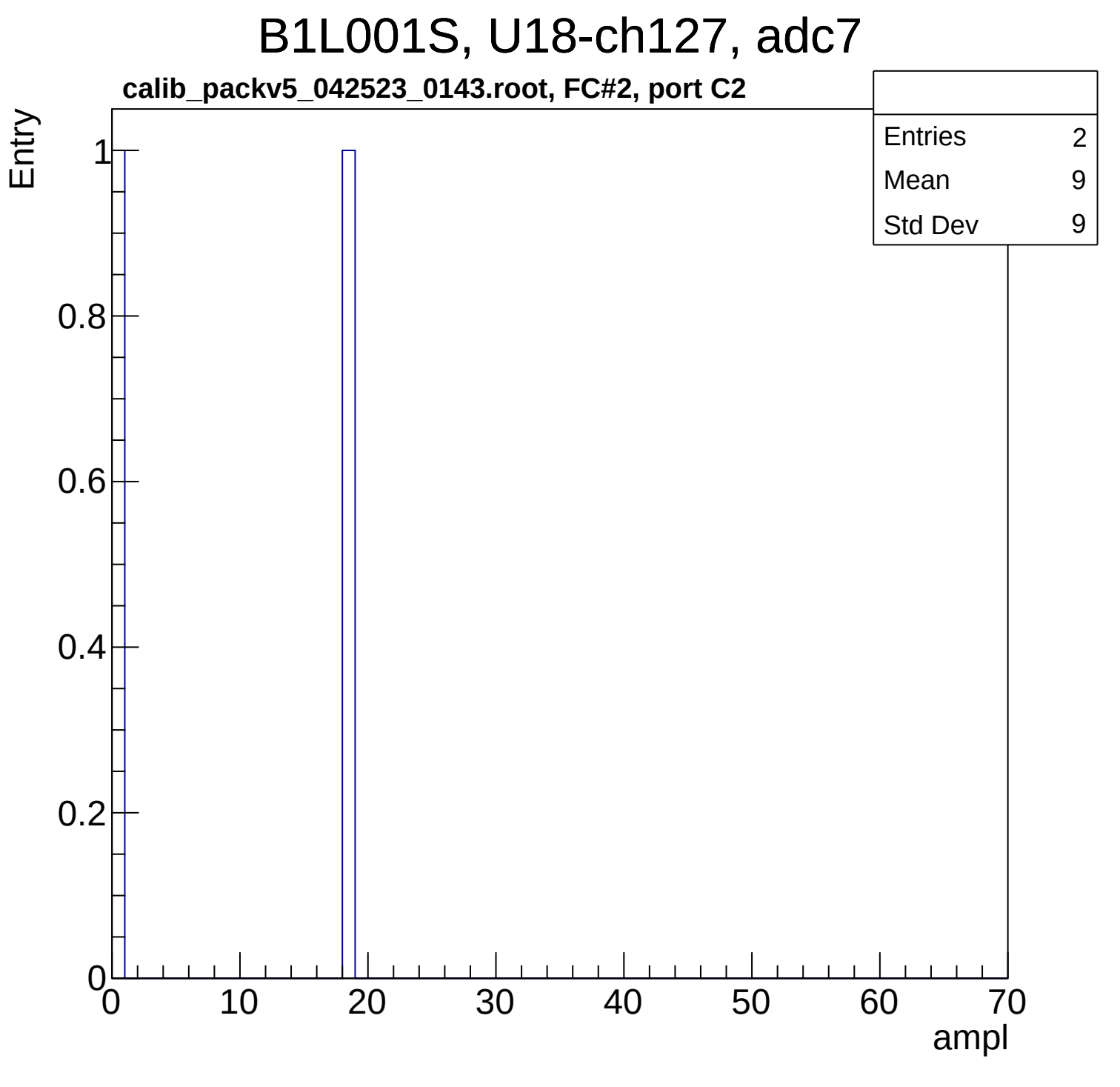

B1L001S, U18-ch127, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 140
Mean 42.2
Std Dev 3.614
Gaus mean : 42.8128
Gaus Width: 3.4929
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

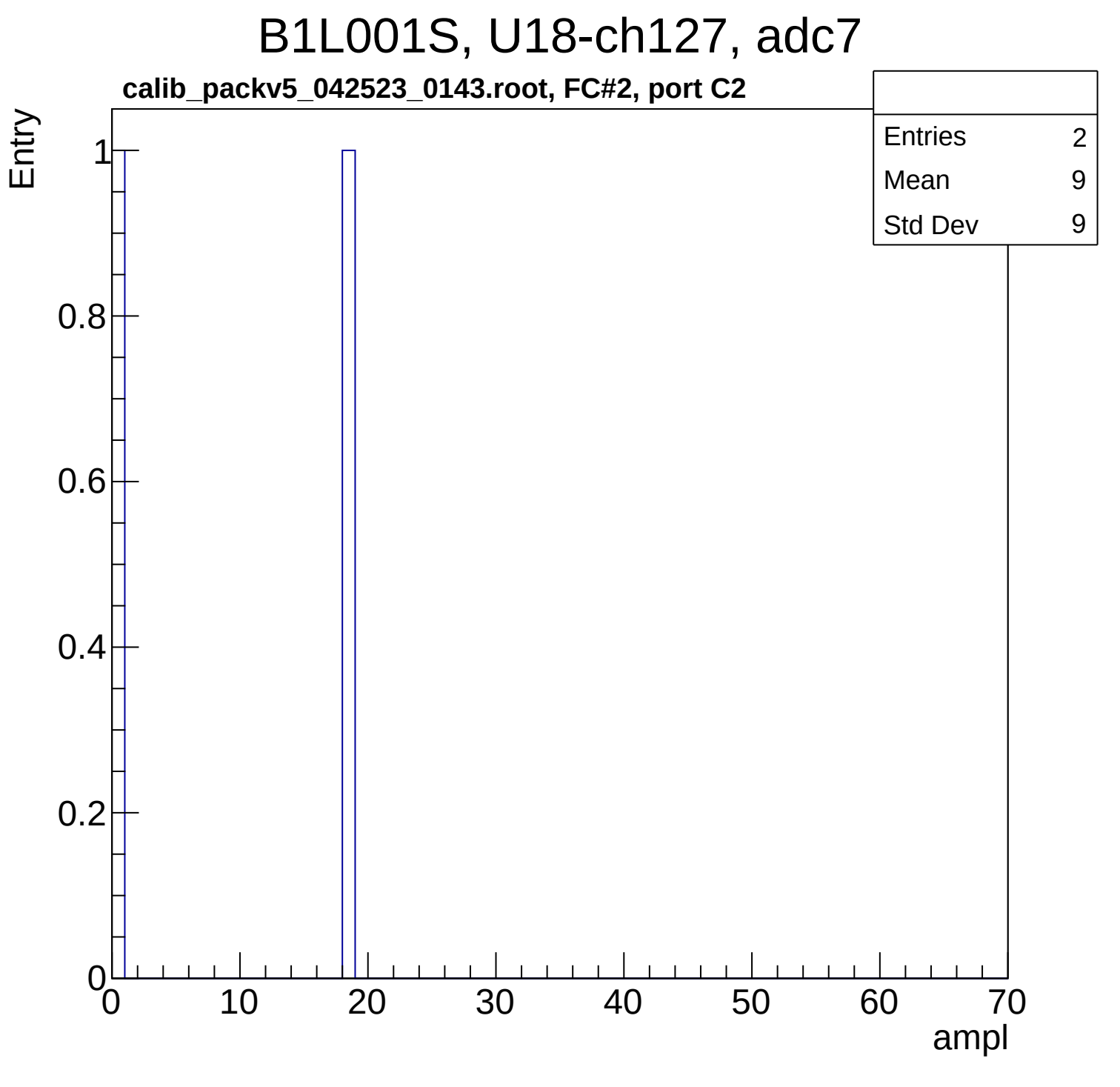

B1L001S, U18-ch127, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 125
Mean 48.78
Std Dev 3.785
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70


B1L001S, U18-ch127, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 152
Mean 55.72
Std Dev 3.417
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70


B1L001S, U18-ch127, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 60
Mean 59.27
Std Dev 8.012
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L001S, U18-ch127, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 20
Mean 58.5
Std Dev 13.55
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L001S, U18-ch127, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 9
Std Dev 9
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L001S, U18-ch127, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 9
Std Dev 9
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl