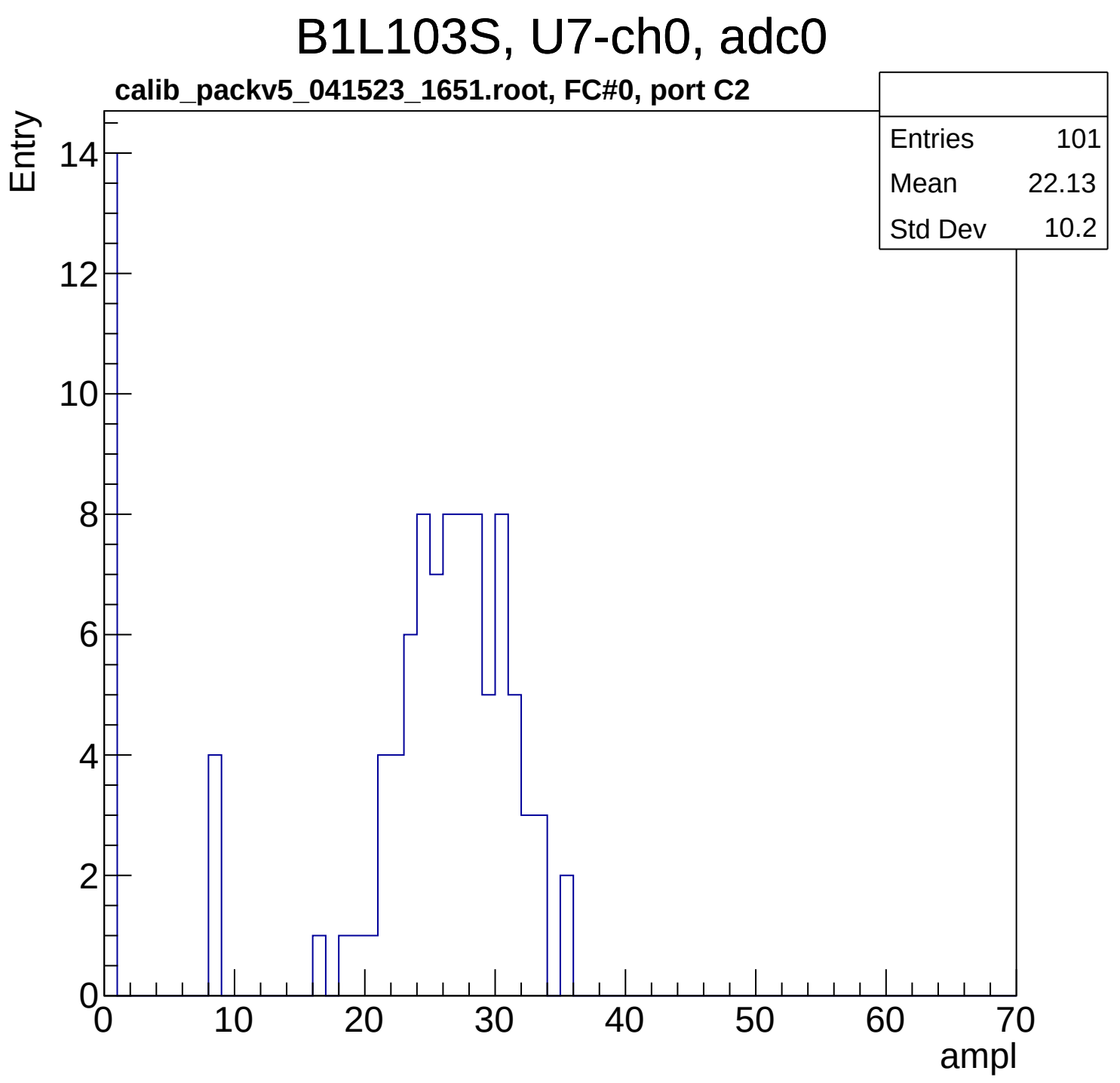
B1L103S, U7-ch0, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 101
Mean 22.13
Std Dev 10.2
Entry
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4
6
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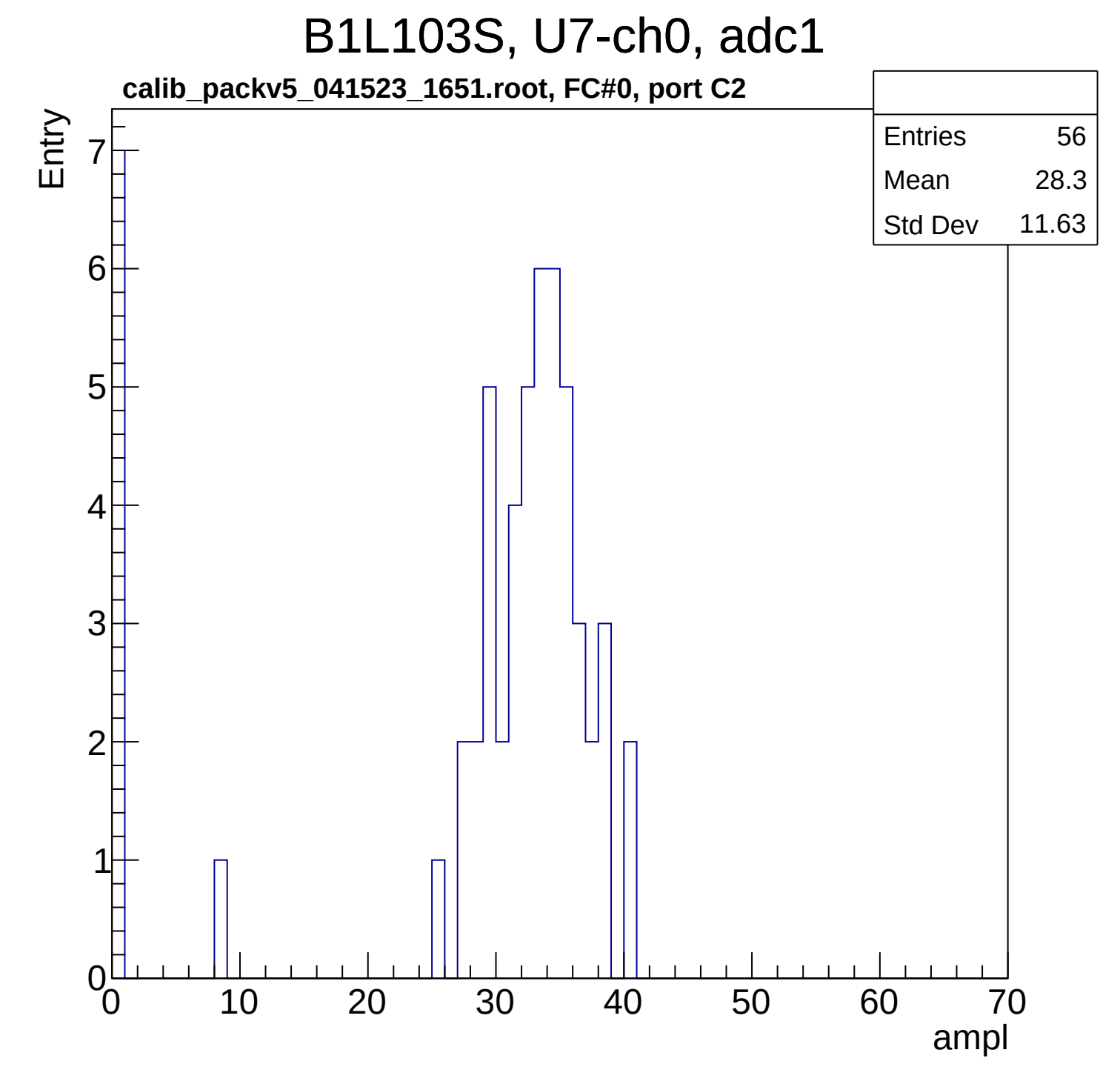
70
ampl


B1L103S, U7-ch0, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 28.3
Std Dev 11.63
Entry
ampl
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4
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0
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40
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60
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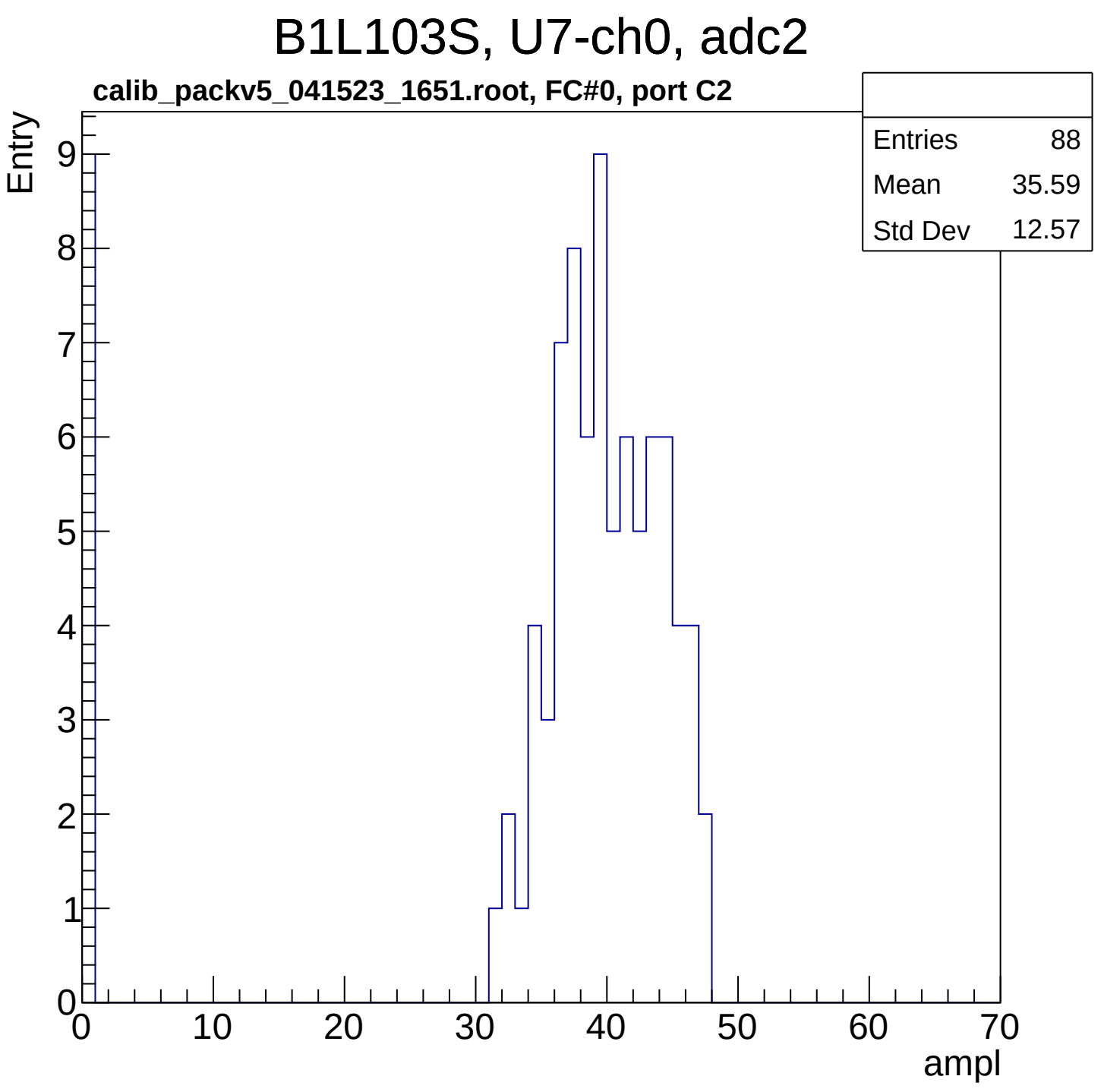
B1L103S, U7-ch0, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 88
Mean 35.59
Std Dev 12.57
Entry
ampl
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3
4
5
6
7
8
9
0
10
20
30
40
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60
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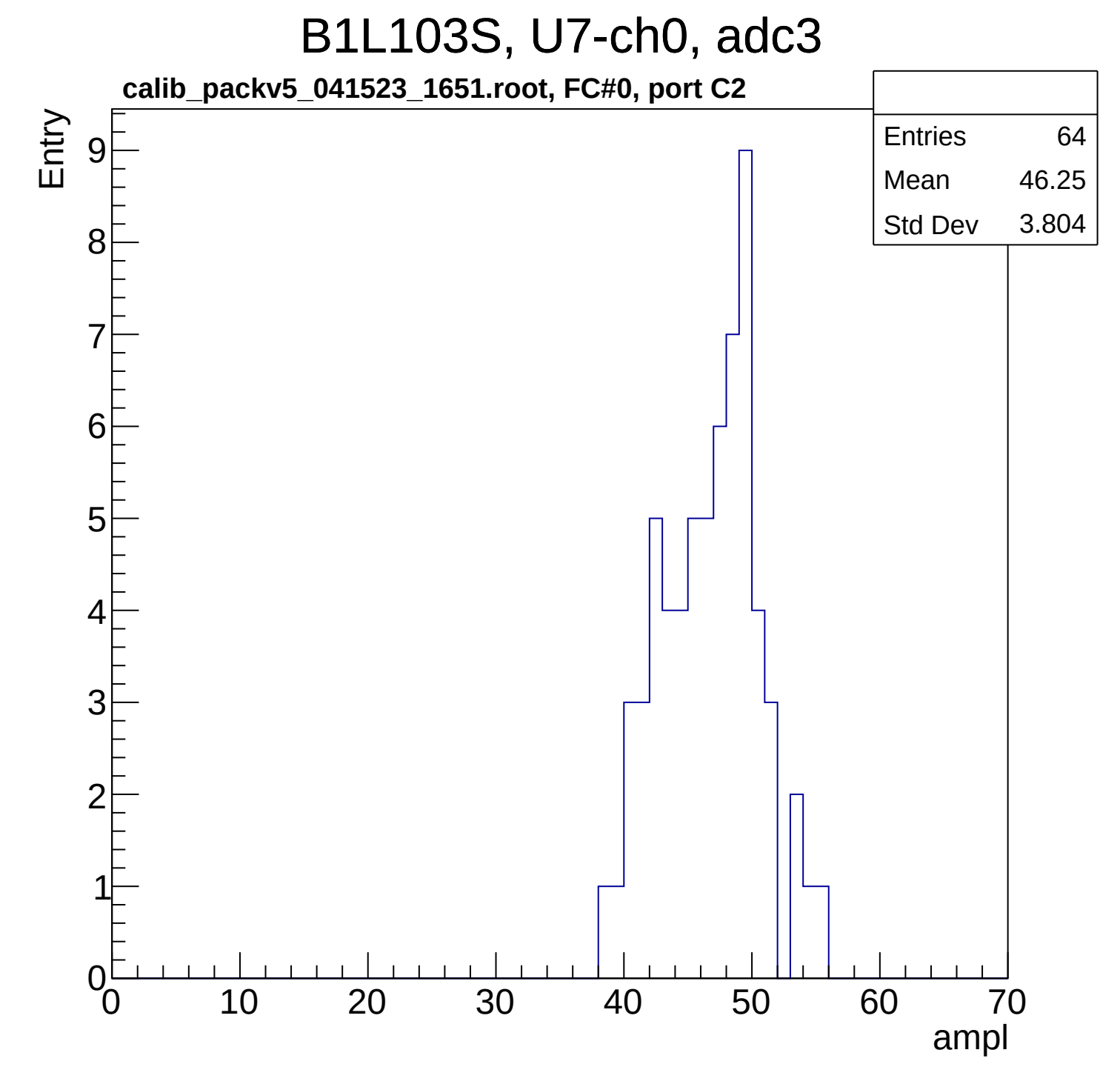
B1L103S, U7-ch0, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 46.25
Std Dev 3.804
Entry
ampl
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3
4
5
6
7
8
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0
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60
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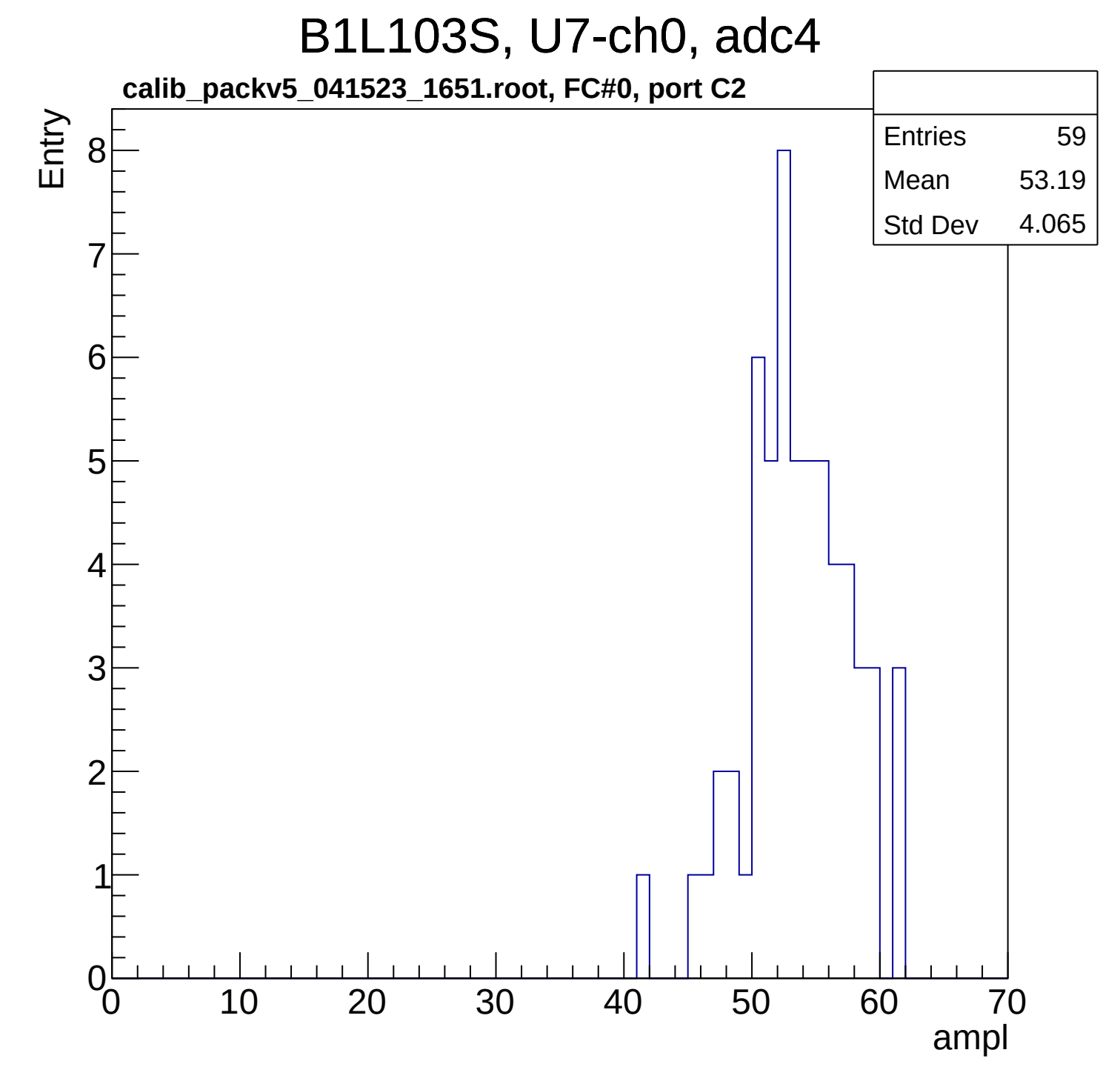
B1L103S, U7-ch0, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 53.19
Std Dev 4.065
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
30
40
50
60
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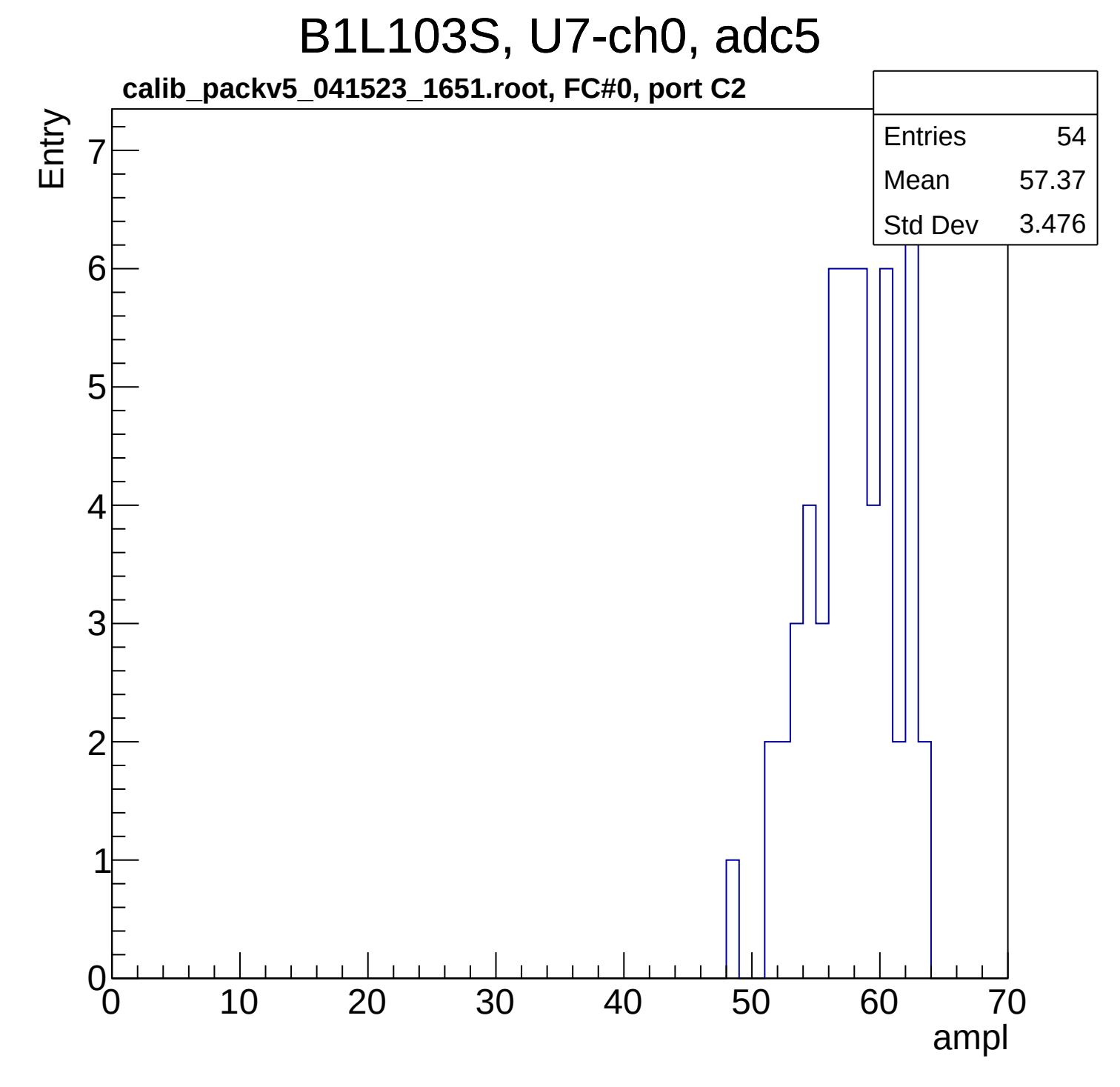
B1L103S, U7-ch0, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 57.37
Std Dev 3.476
Entry
ampl
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2
3
4
5
6
7
0
10
20
30
40
50
60
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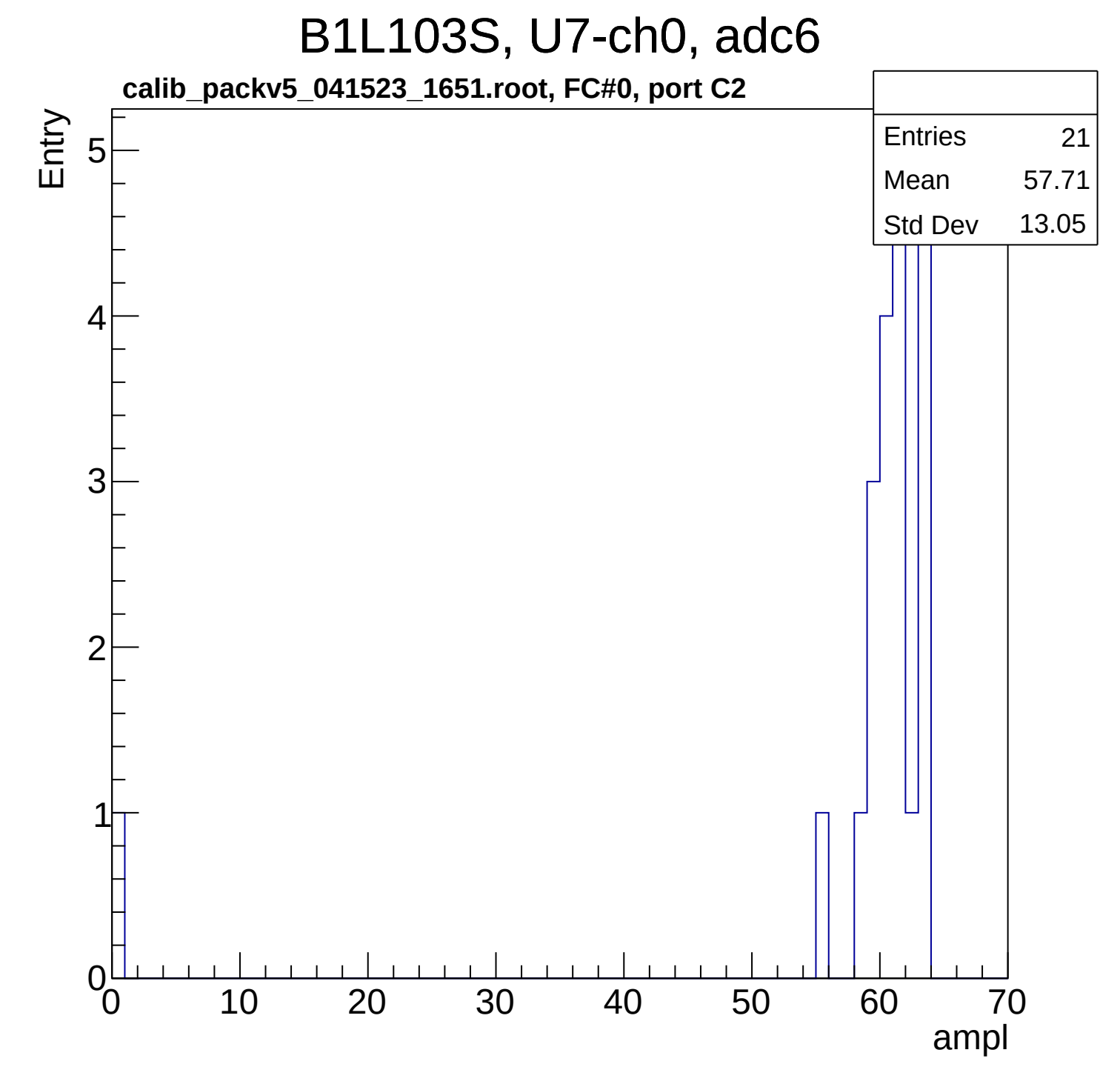
B1L103S, U7-ch0, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 57.71
Std Dev 13.05
Entry
ampl
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2
3
4
5
0
10
20
30
40
50
60
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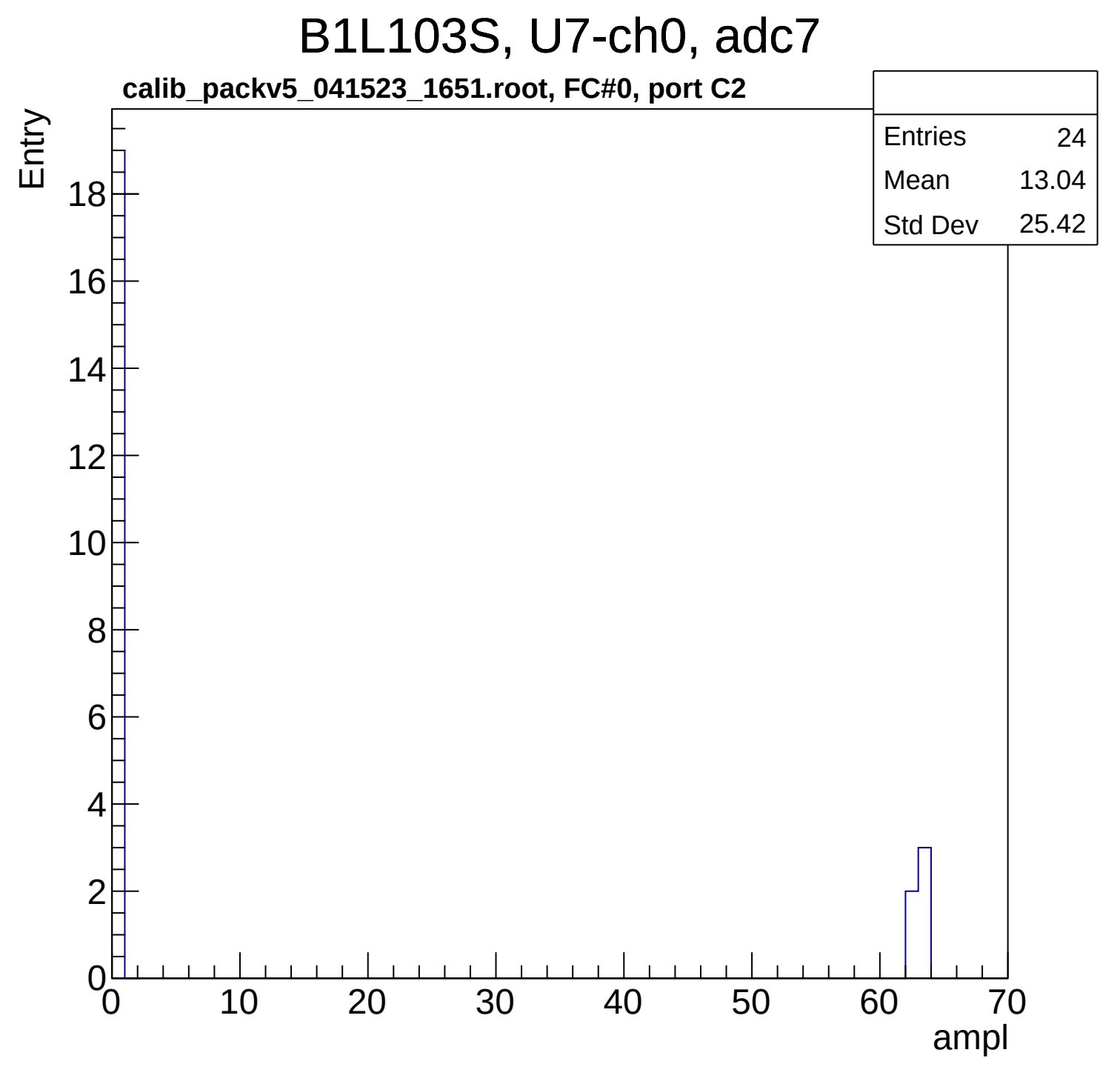
B1L103S, U7-ch0, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 24
Mean 13.04
Std Dev 25.42
Entry
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6
8
10
12
14
16
18
0
10
20
30
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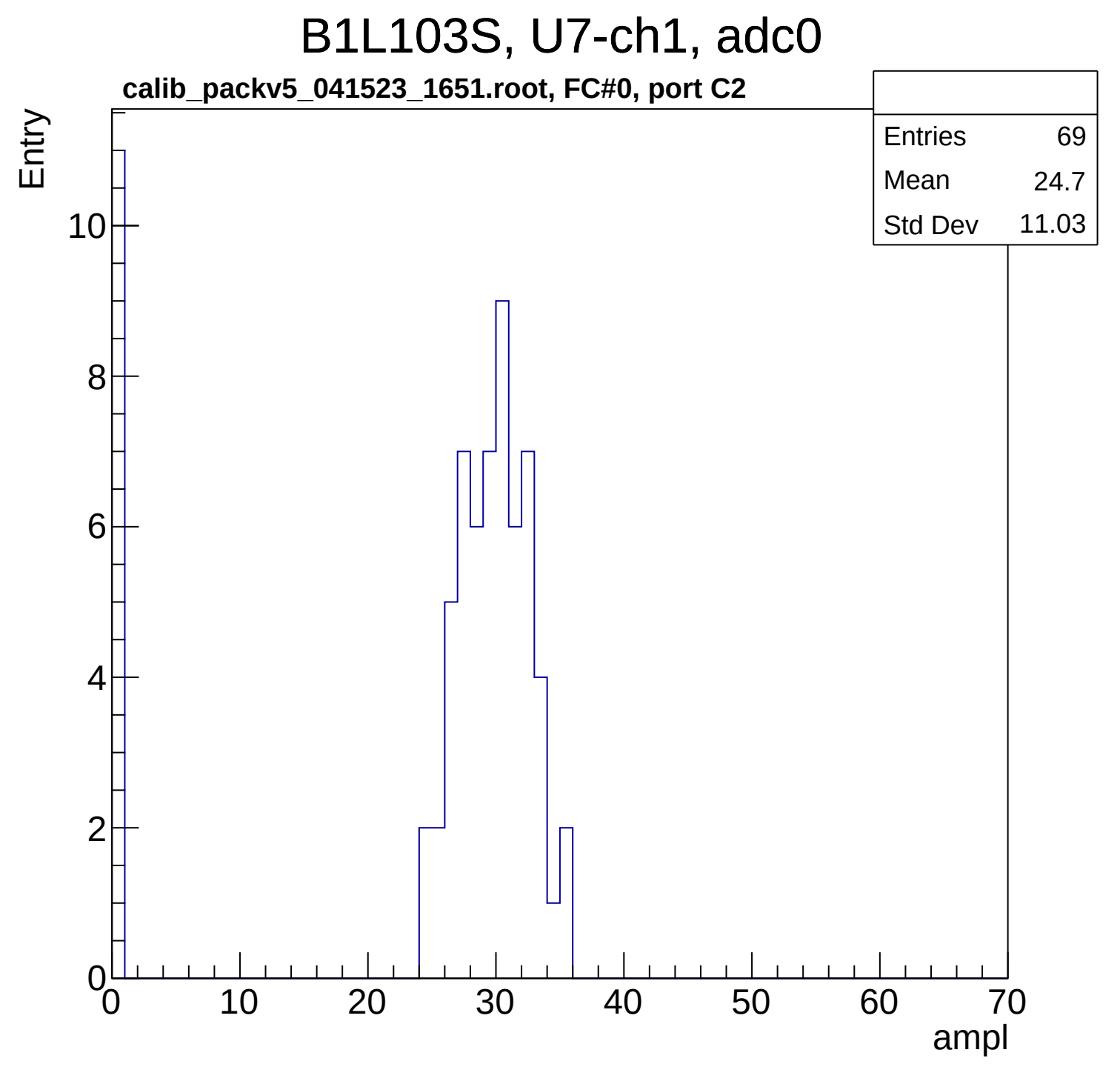
50
60
70
ampl


B1L103S, U7-ch1, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 24.7
Std Dev 11.03
Entry
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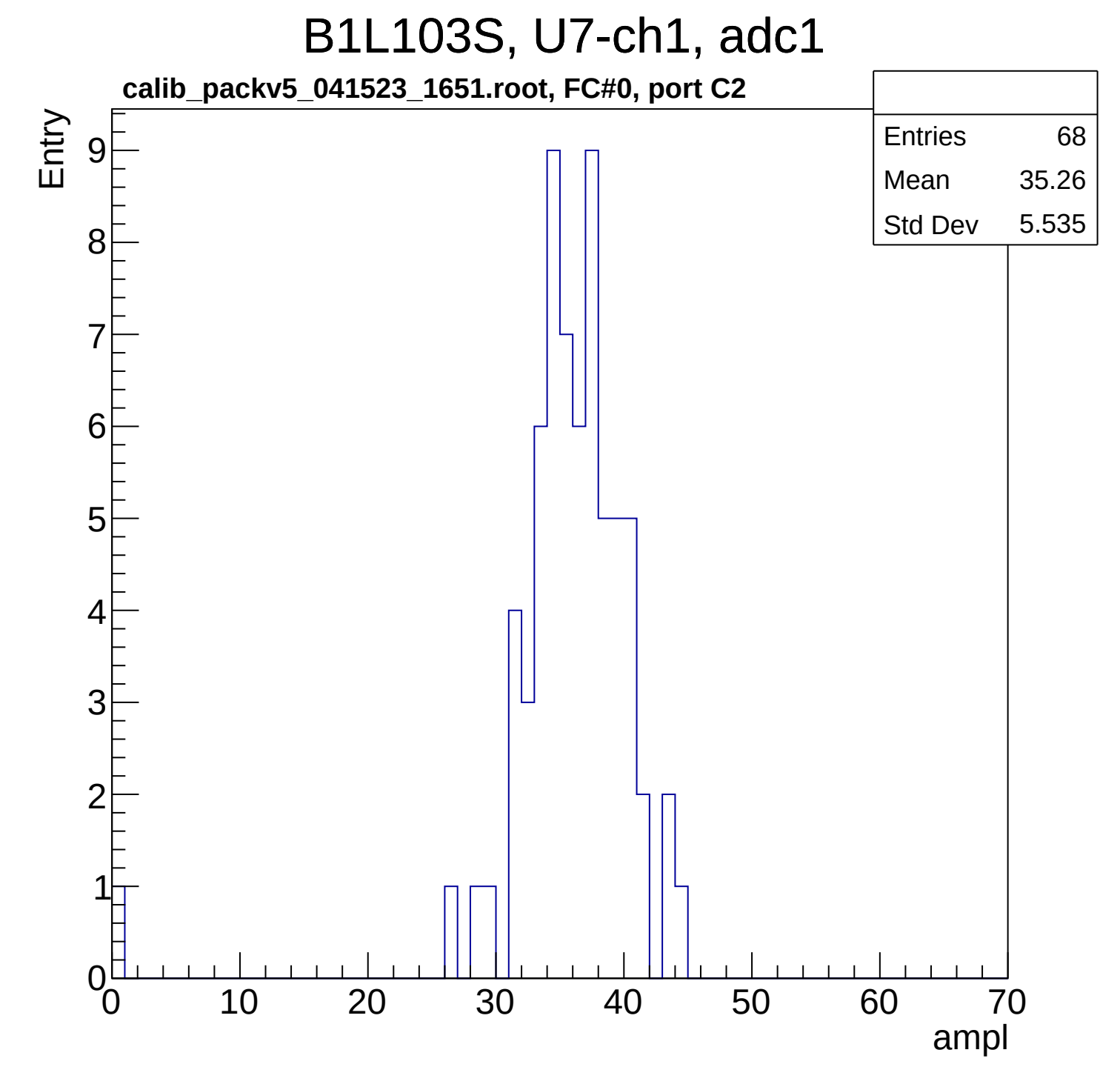
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch1, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 35.26
Std Dev 5.535
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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60
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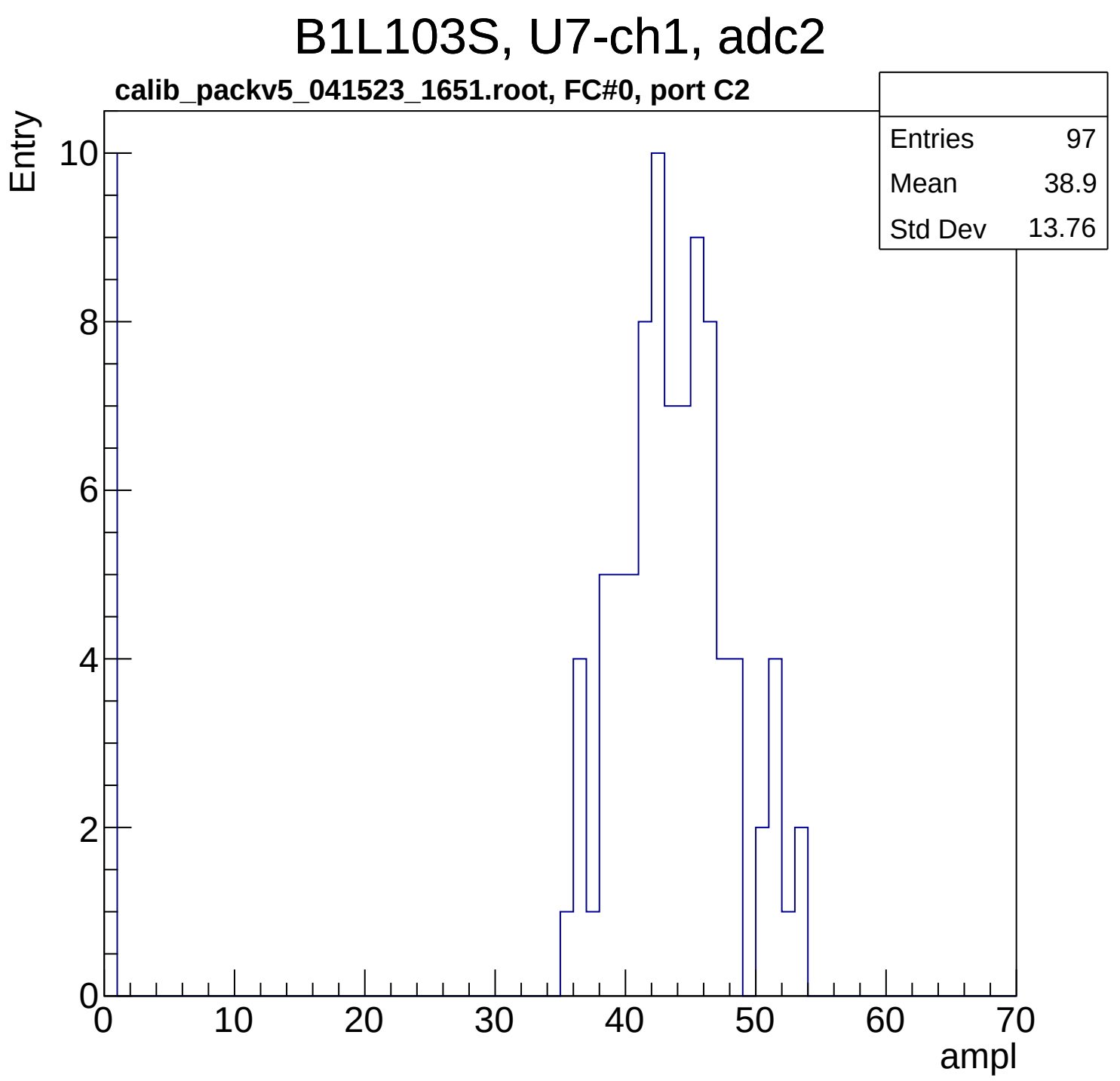
B1L103S, U7-ch1, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 97
Mean 38.9
Std Dev 13.76
Entry
ampl
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4
6
8
10
0
10
20
30
40
50
60
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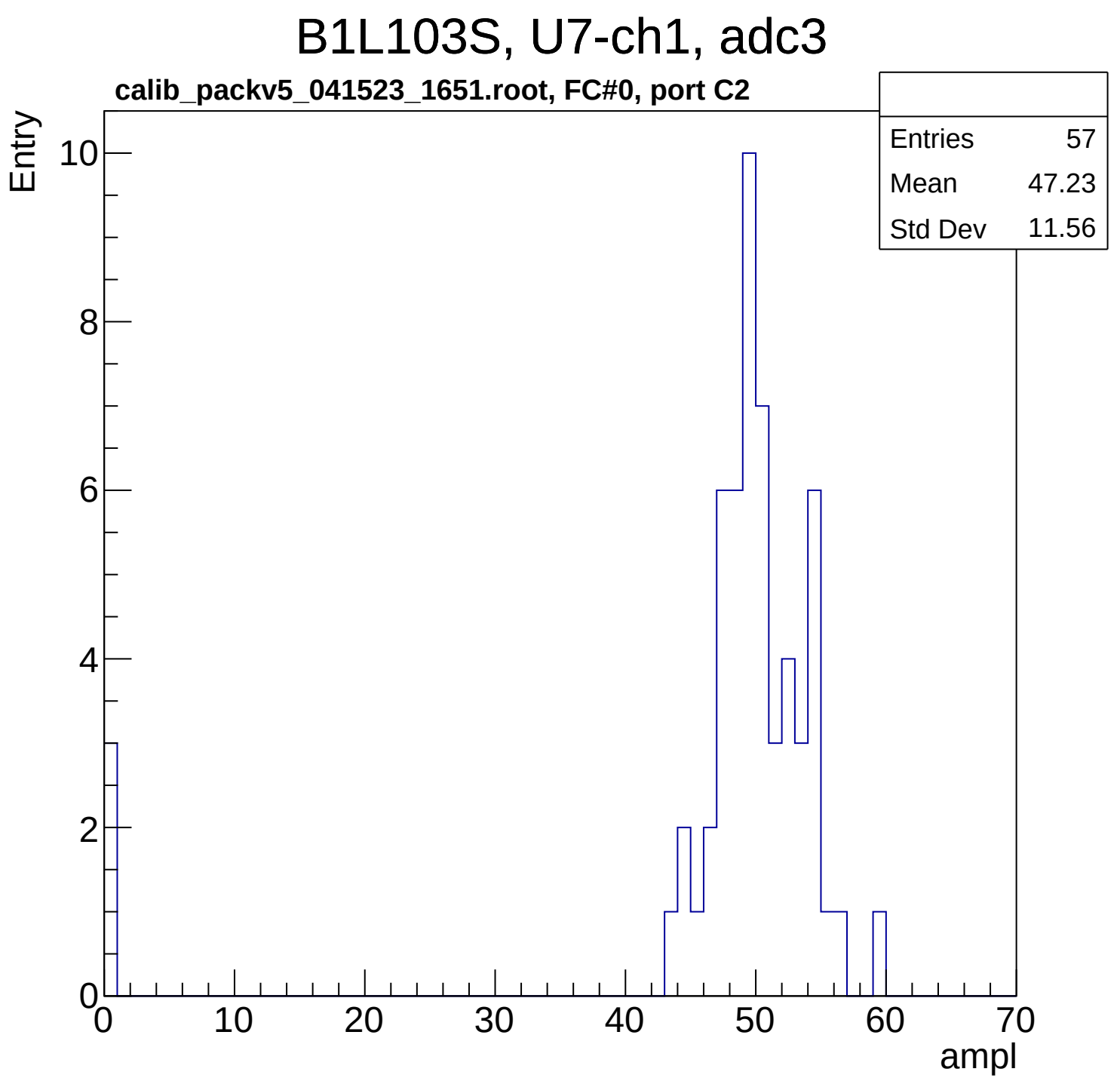
B1L103S, U7-ch1, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 47.23
Std Dev 11.56
Entry
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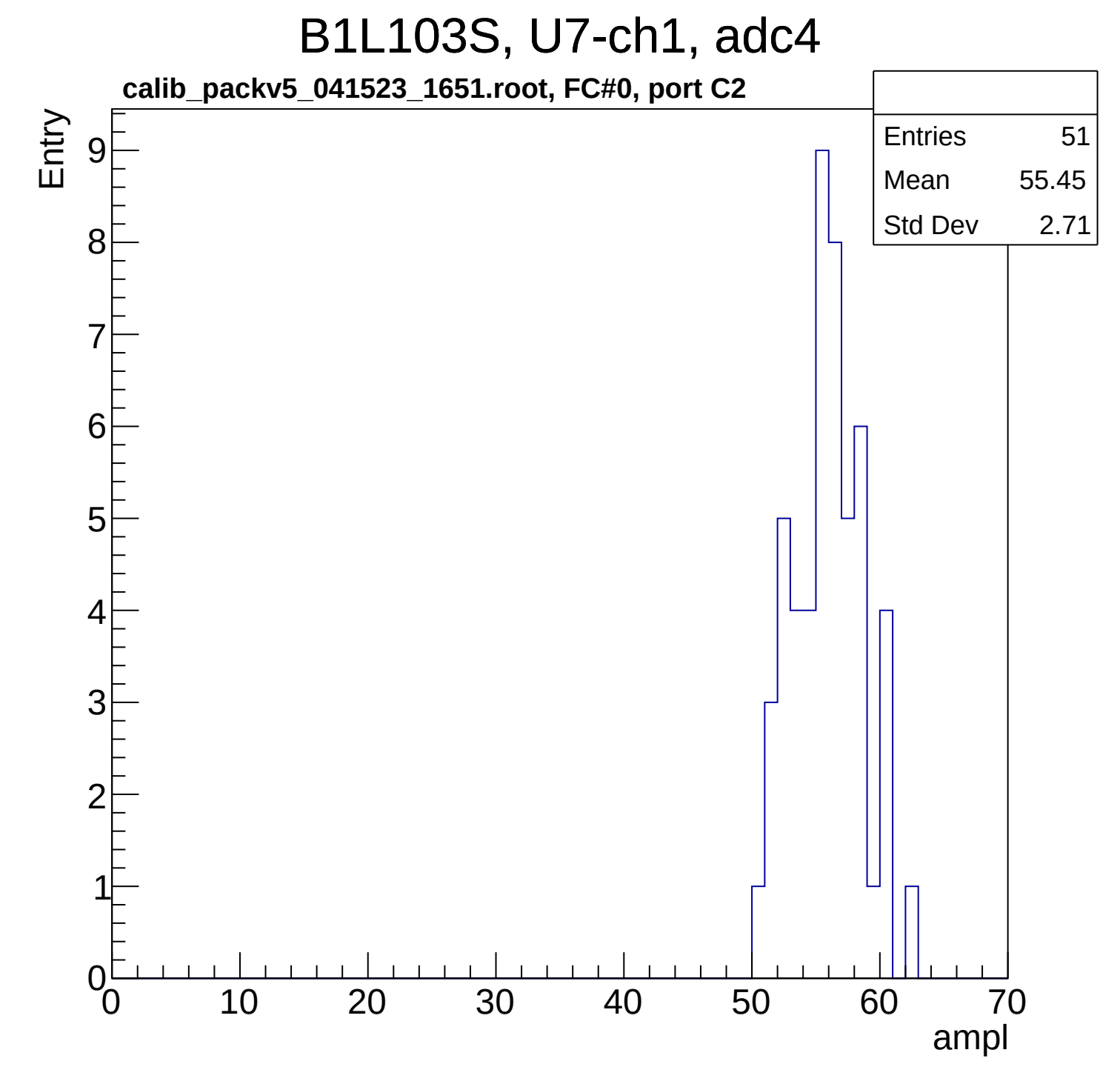
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch1, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 55.45
Std Dev 2.71
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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60
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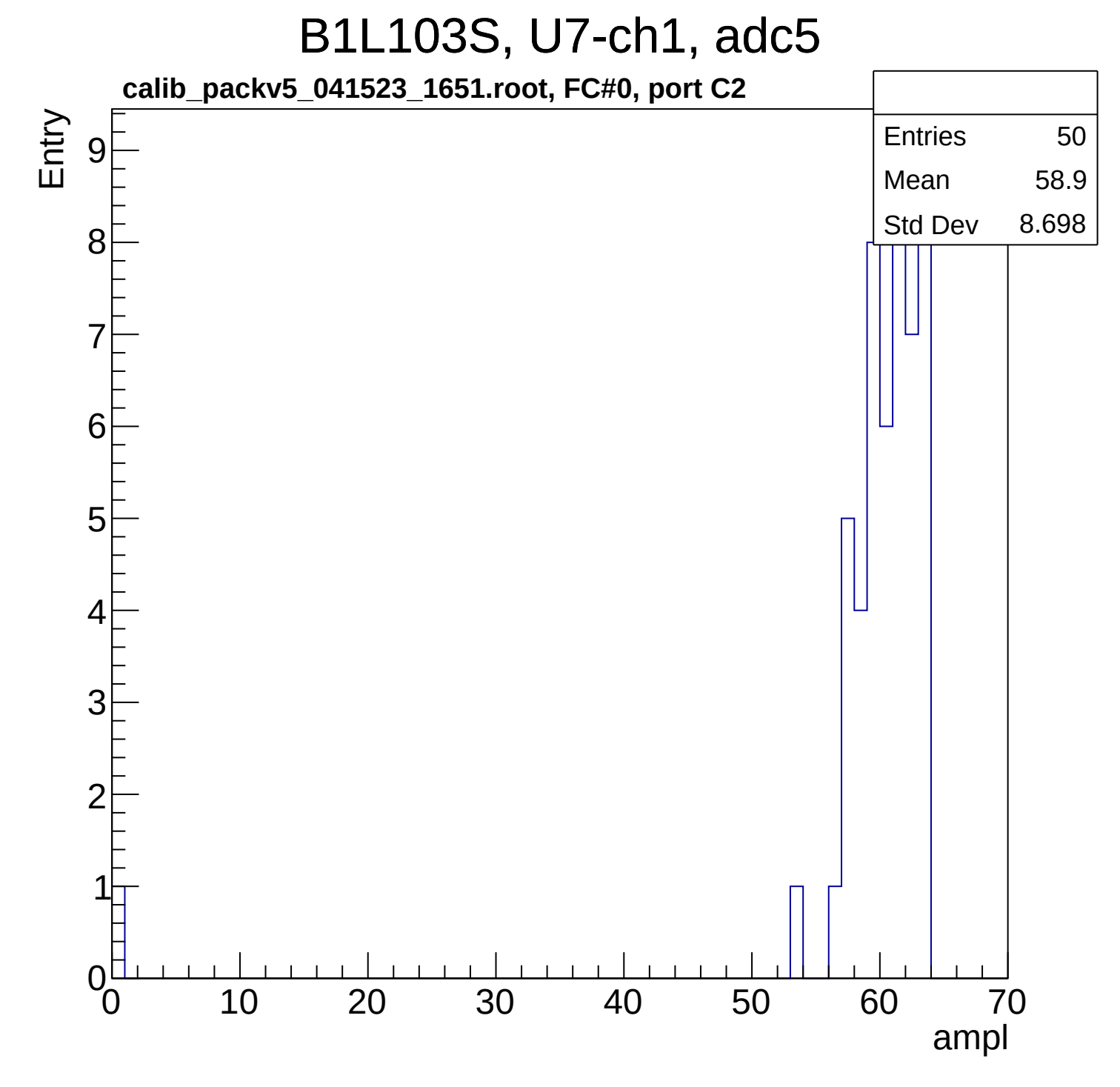
B1L103S, U7-ch1, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 58.9
Std Dev 8.698
Entry
ampl
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2
3
4
5
6
7
8
9
0
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60
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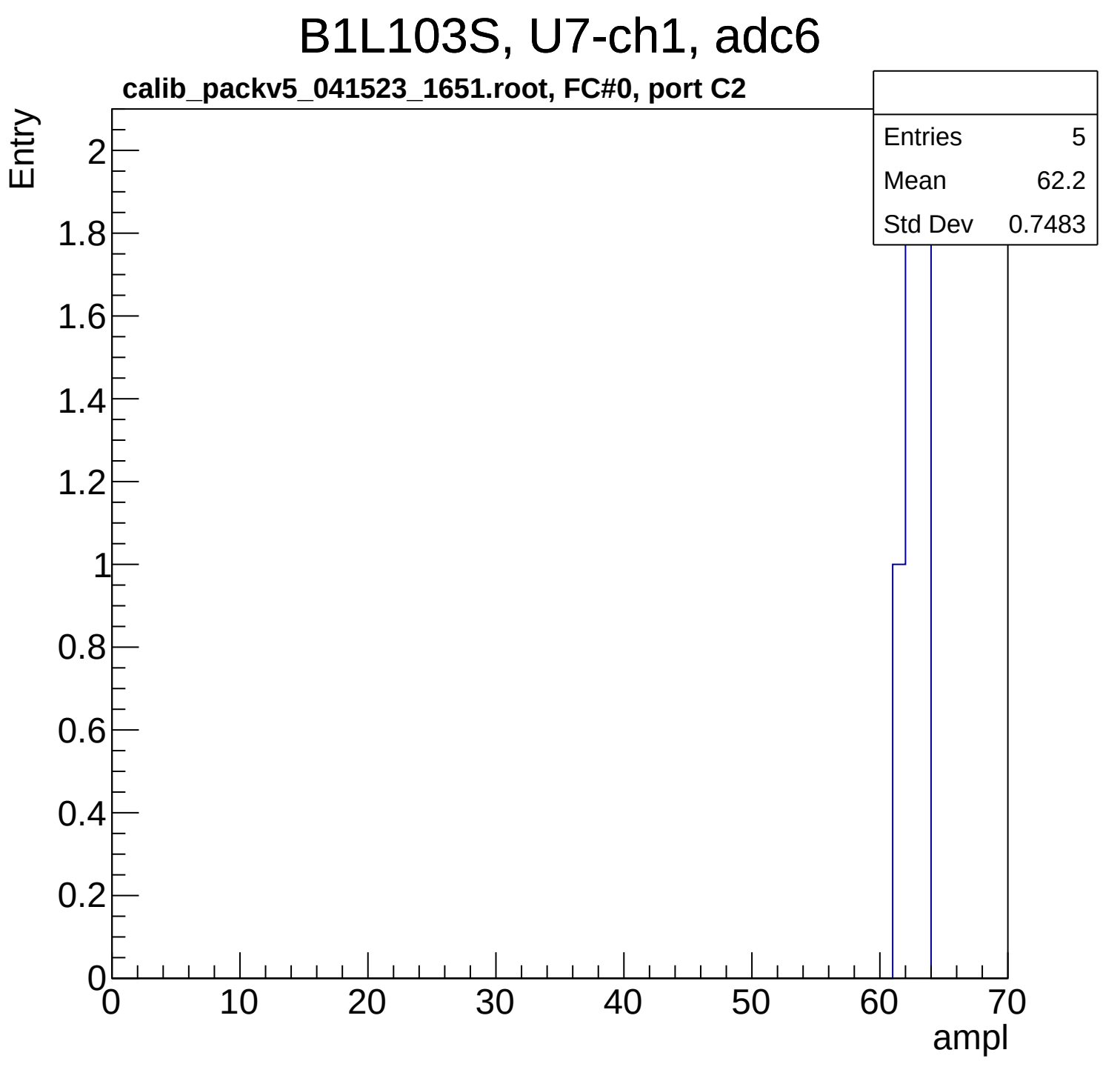
B1L103S, U7-ch1, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 5
Mean 62.2
Std Dev 0.7483
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
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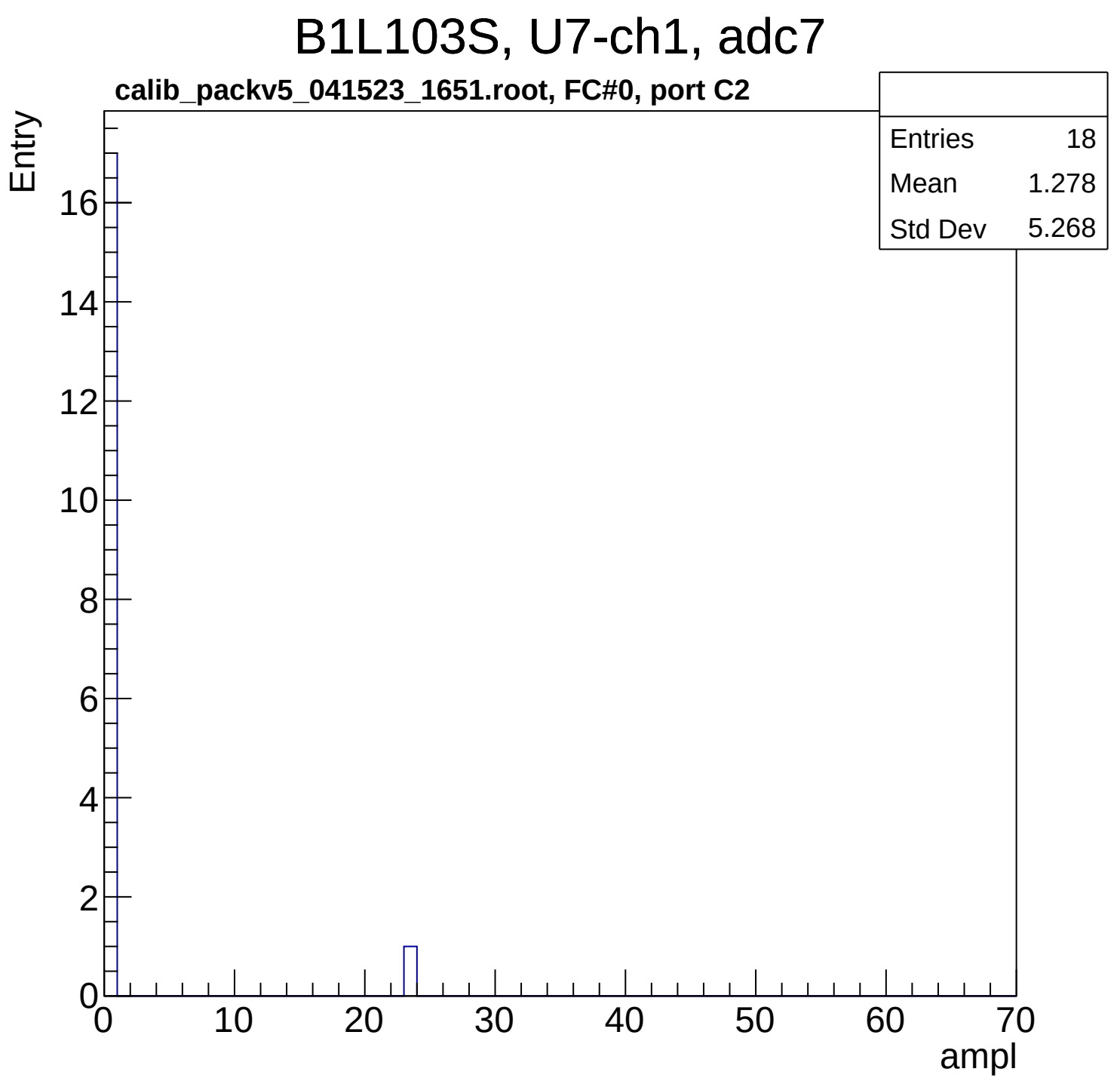
B1L103S, U7-ch1, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 1.278
Std Dev 5.268
Entry
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4
6
8
10
12
14
16
0
10
20
30
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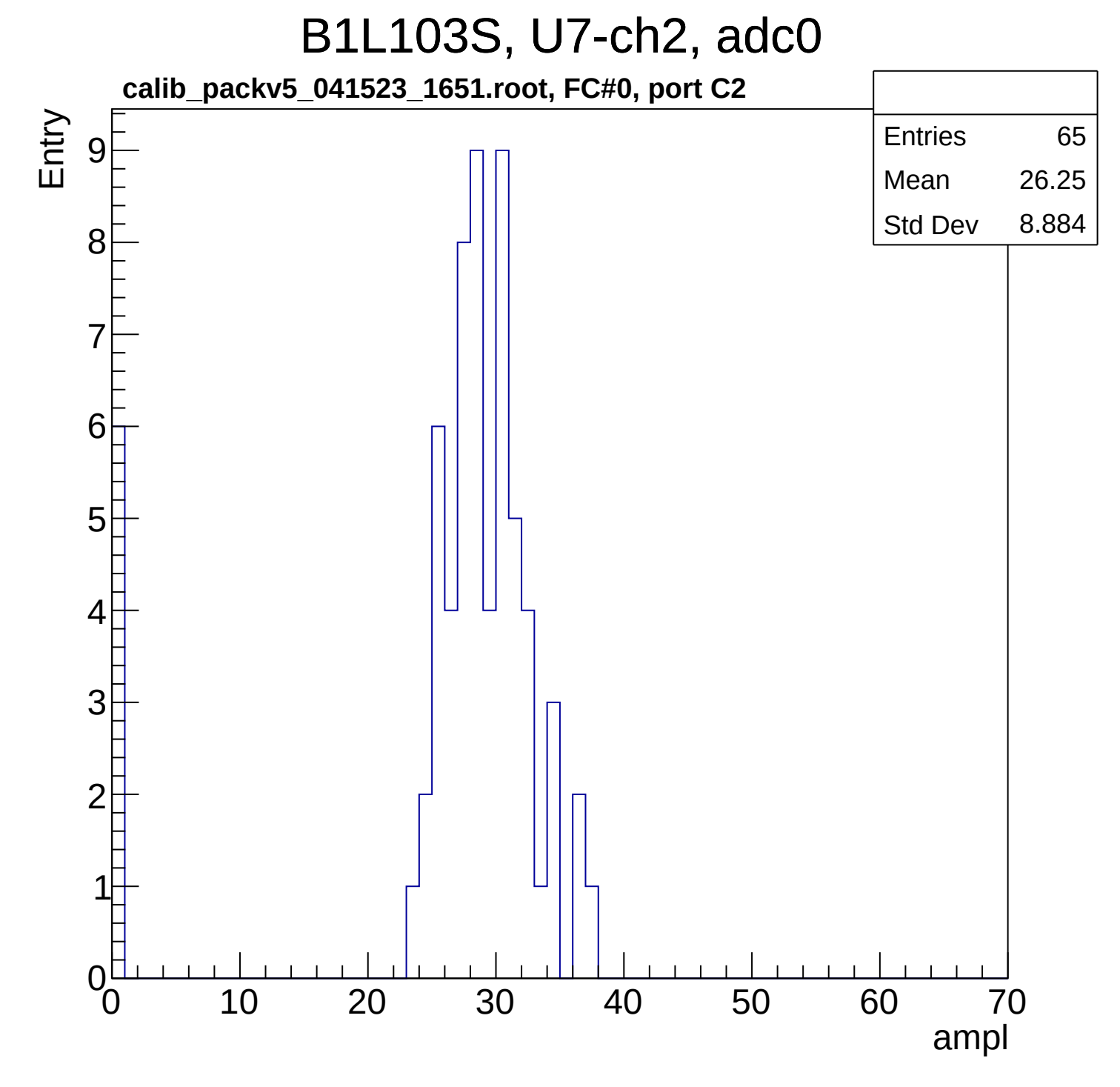
50
60
70
ampl


B1L103S, U7-ch2, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 26.25
Std Dev 8.884
Entry
ampl
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3
4
5
6
7
8
9
0
10
20
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40
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60
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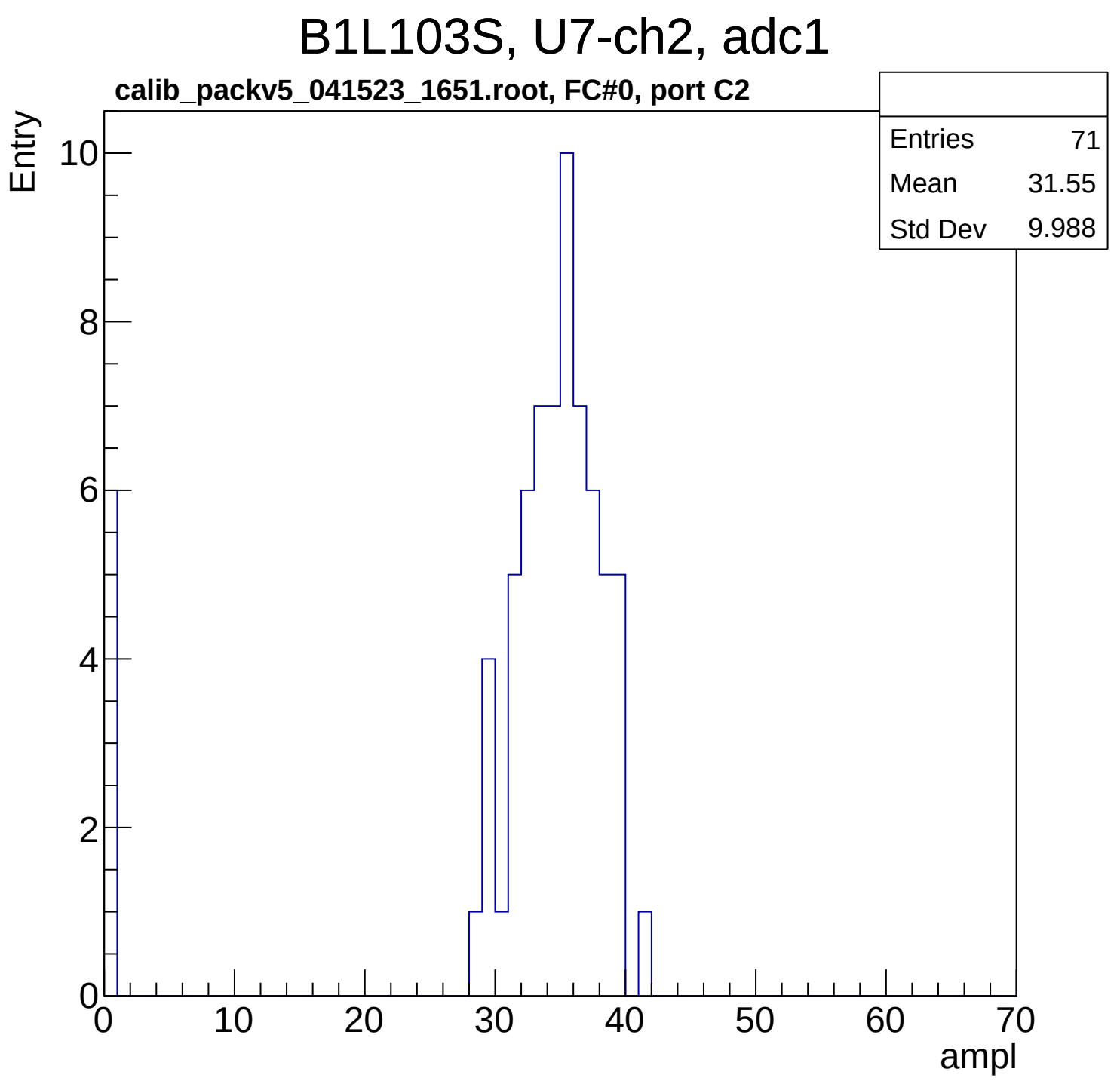
B1L103S, U7-ch2, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 31.55
Std Dev 9.988
Entry
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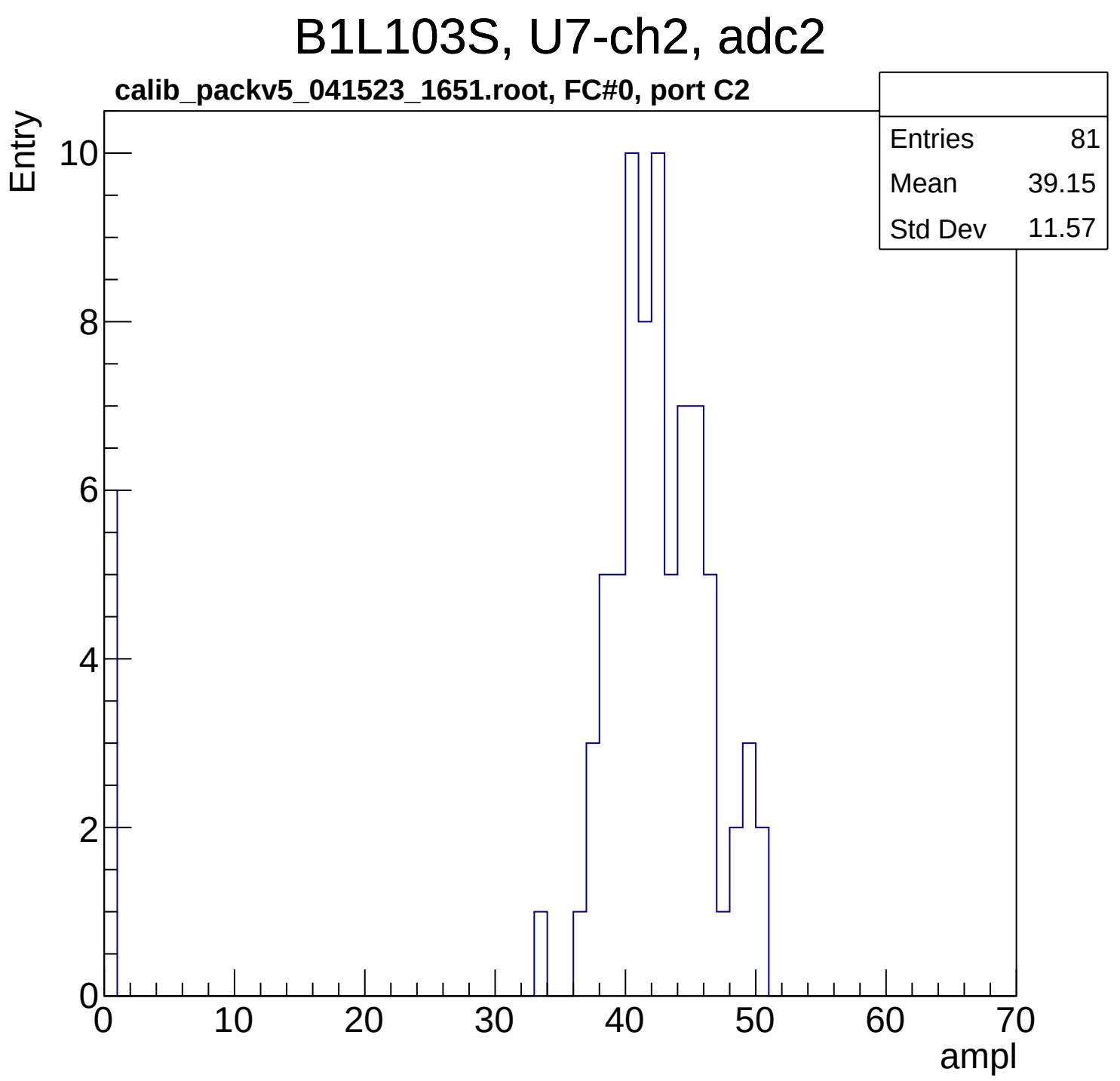
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch2, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 39.15
Std Dev 11.57
Entry
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4
6
8
10
0
10
20
30
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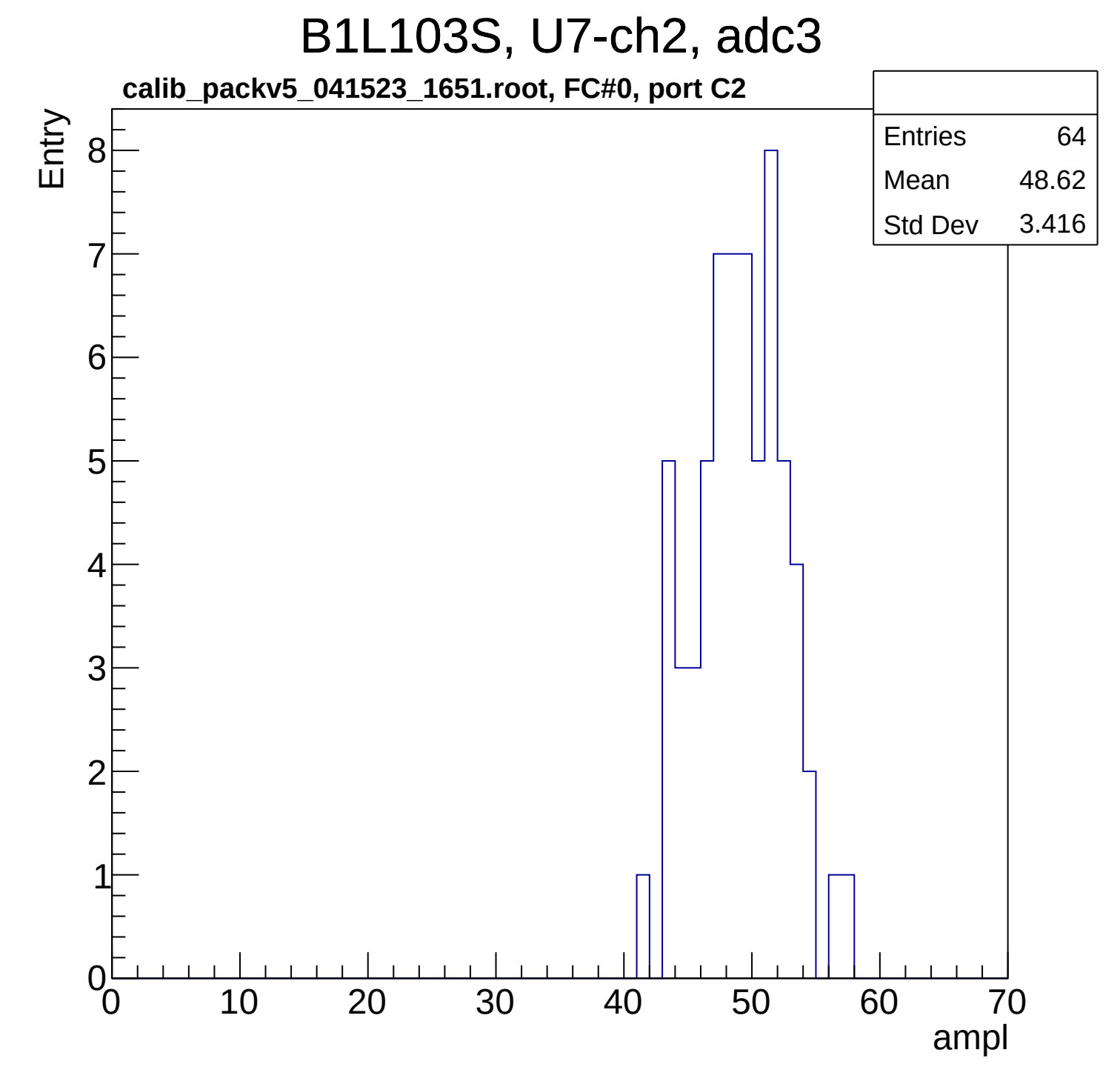
50
60
70
ampl


B1L103S, U7-ch2, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 48.62
Std Dev 3.416
Entry
ampl
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7
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60
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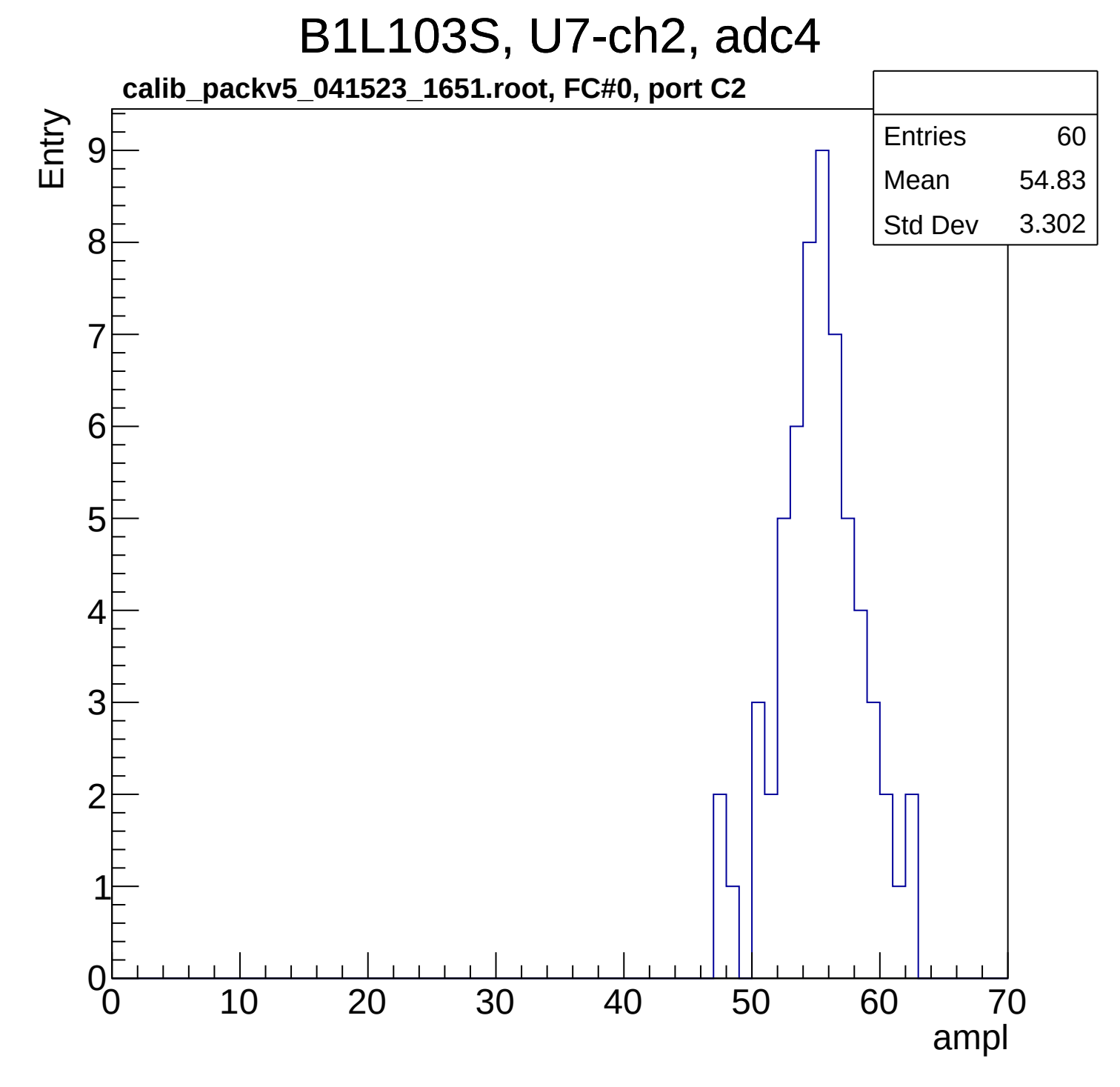
B1L103S, U7-ch2, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 54.83
Std Dev 3.302
Entry
ampl
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4
5
6
7
8
9
0
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60
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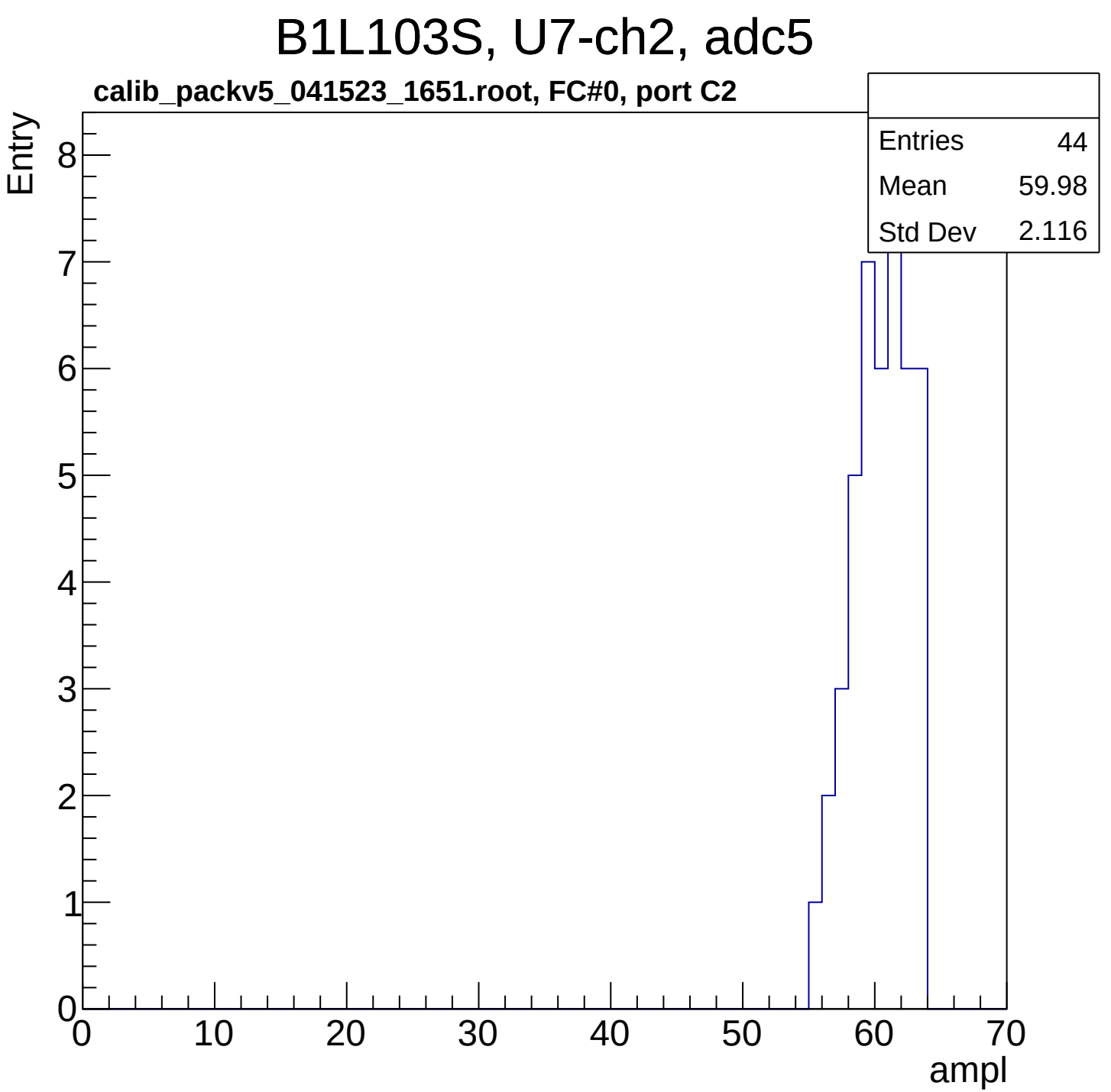
B1L103S, U7-ch2, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 59.98
Std Dev 2.116
Entry
ampl
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2
3
4
5
6
7
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0
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60
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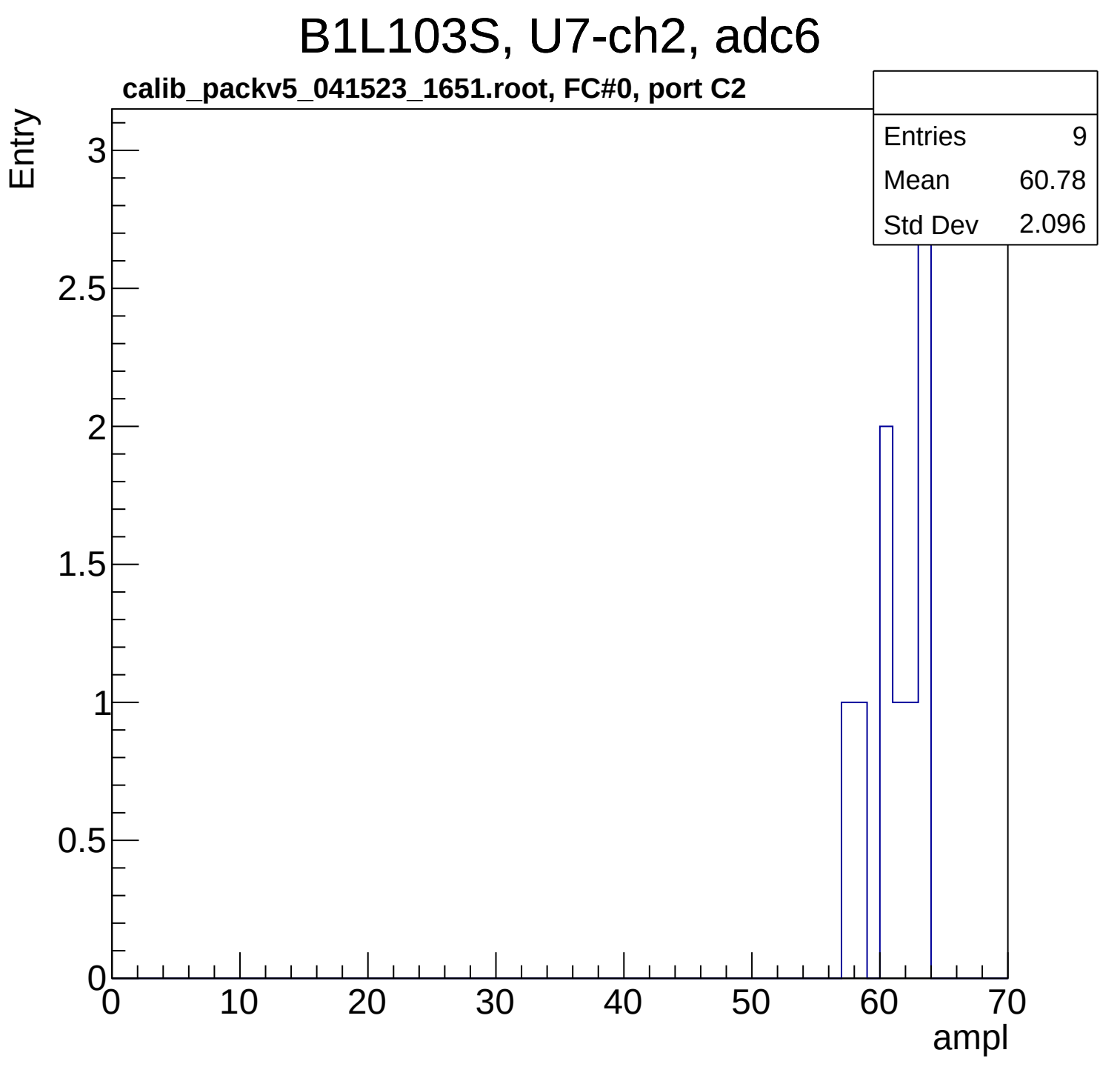
B1L103S, U7-ch2, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 9
Mean 60.78
Std Dev 2.096
Entry
ampl
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1
1.5
2
2.5
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0
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60
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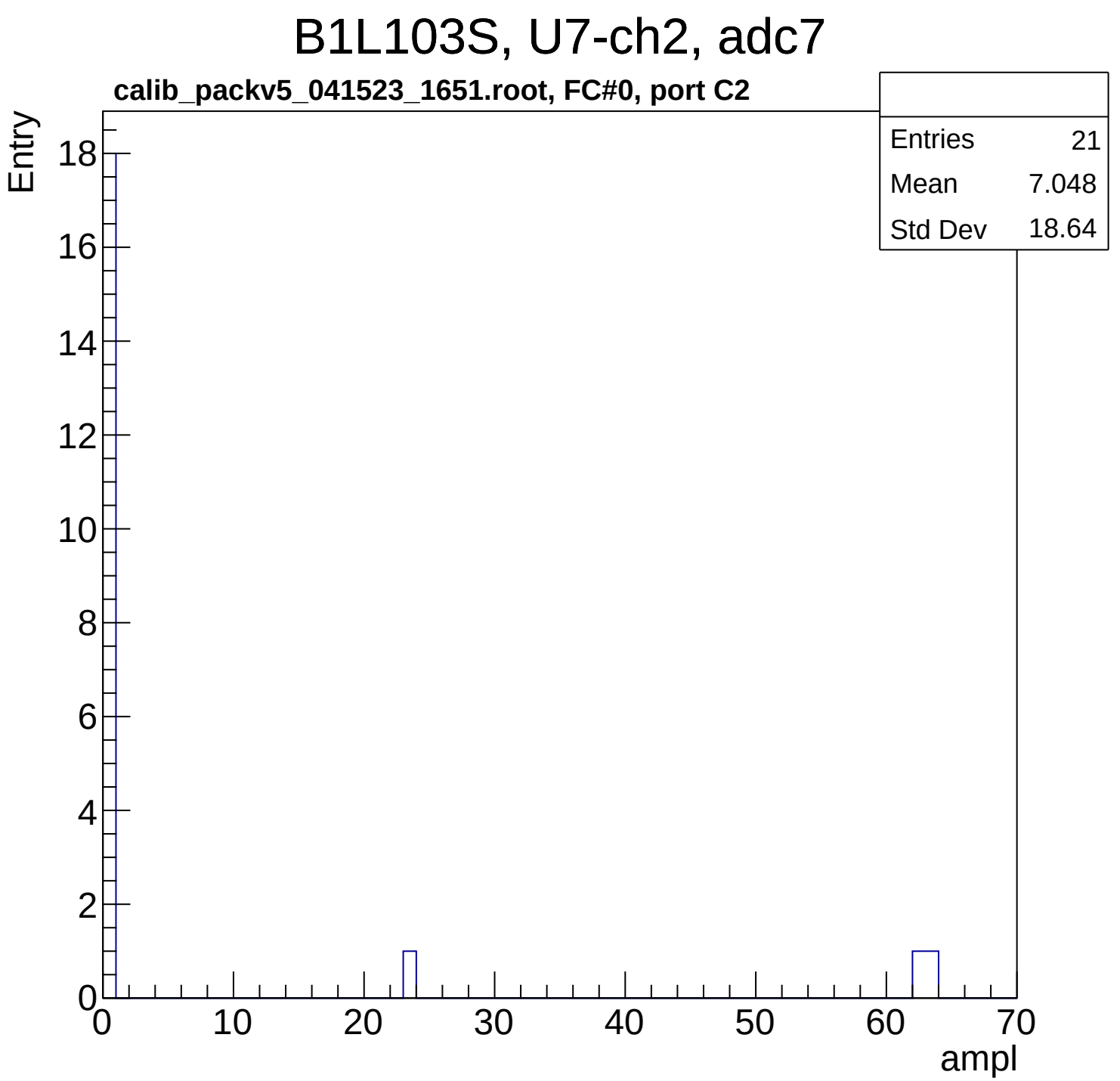
B1L103S, U7-ch2, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 7.048
Std Dev 18.64
Entry
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10
12
14
16
18
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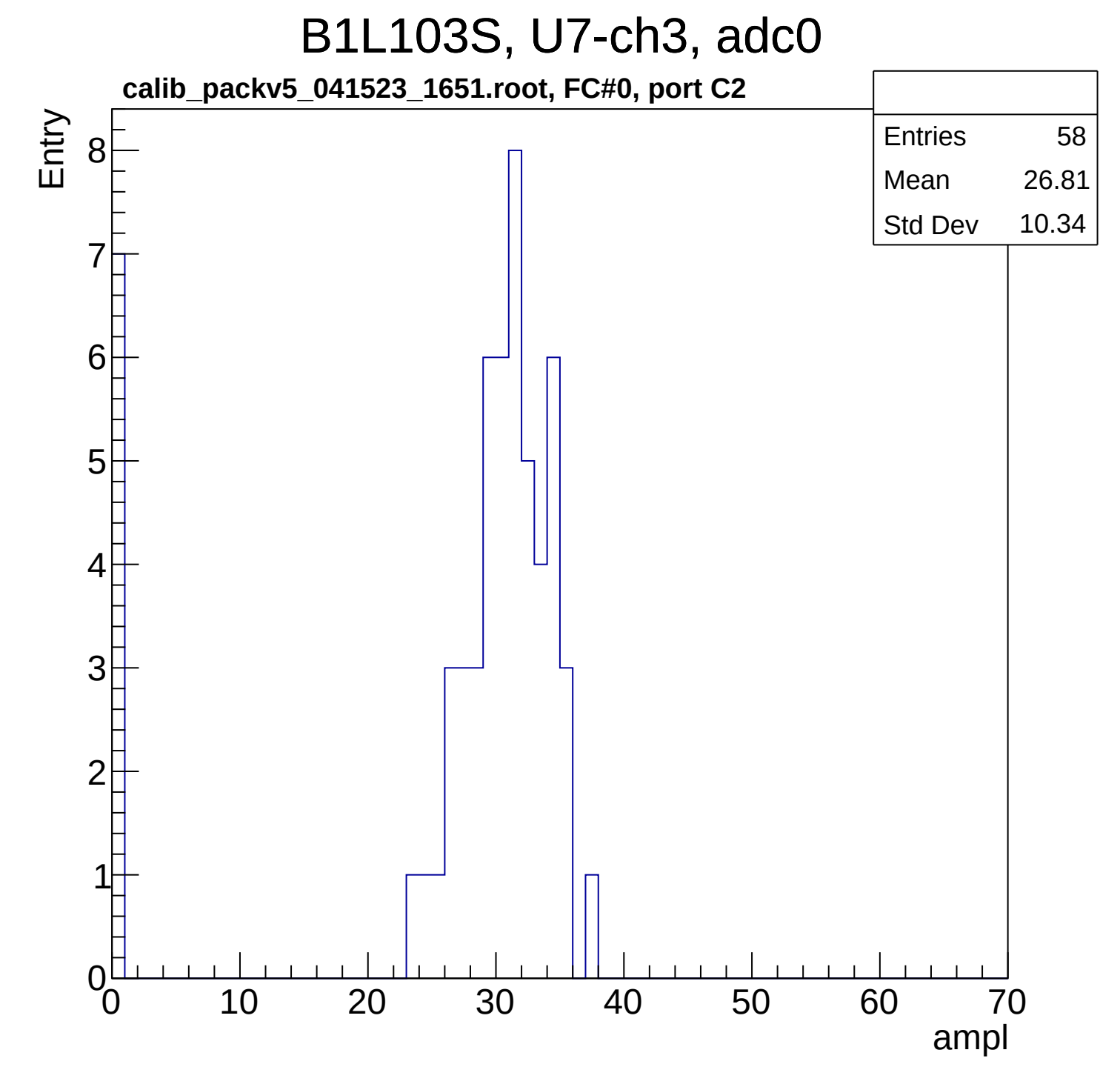
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch3, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 26.81
Std Dev 10.34
Entry
ampl
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4
5
6
7
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0
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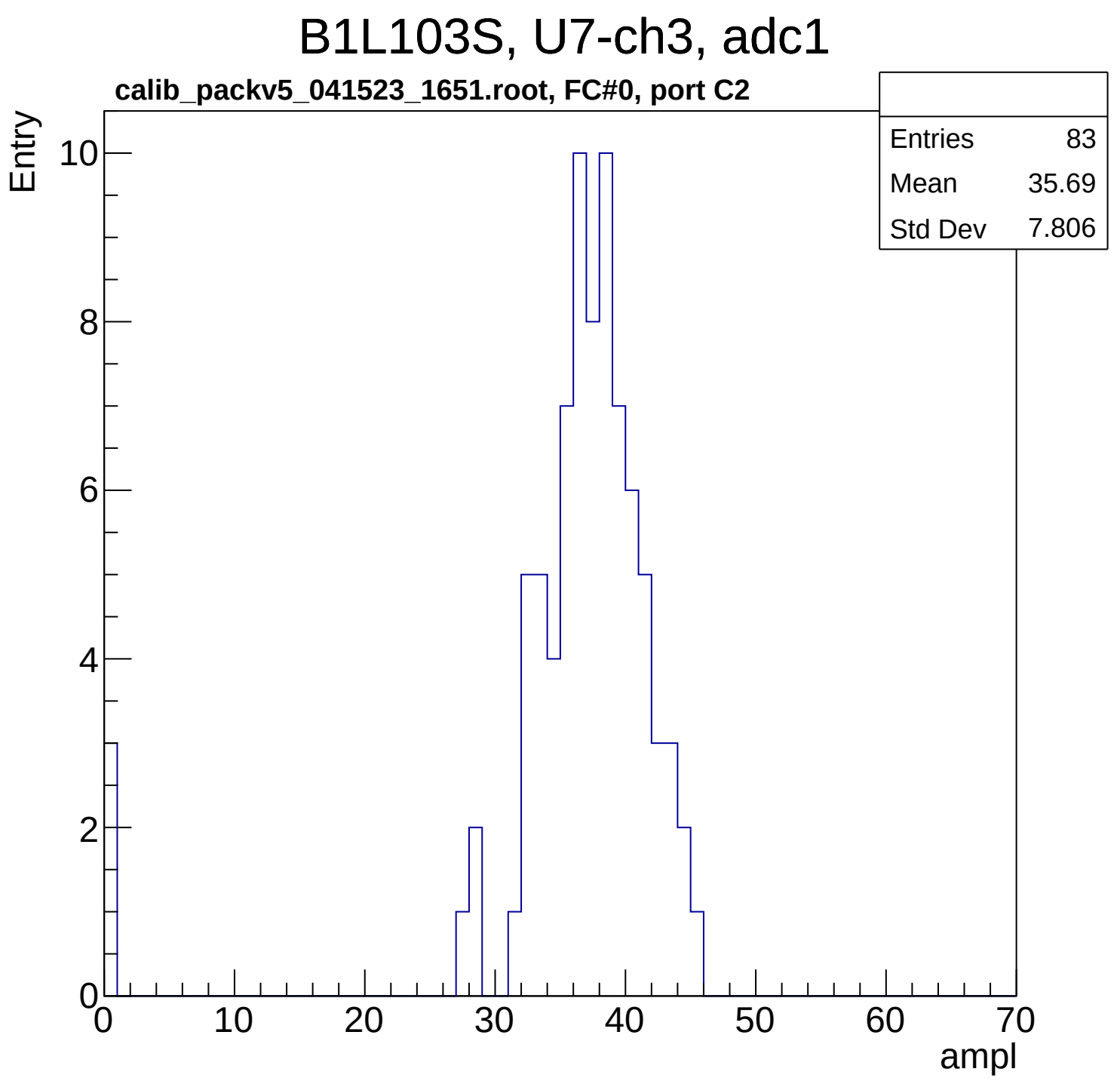
B1L103S, U7-ch3, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 35.69
Std Dev 7.806
Entry
ampl
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0
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40
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60
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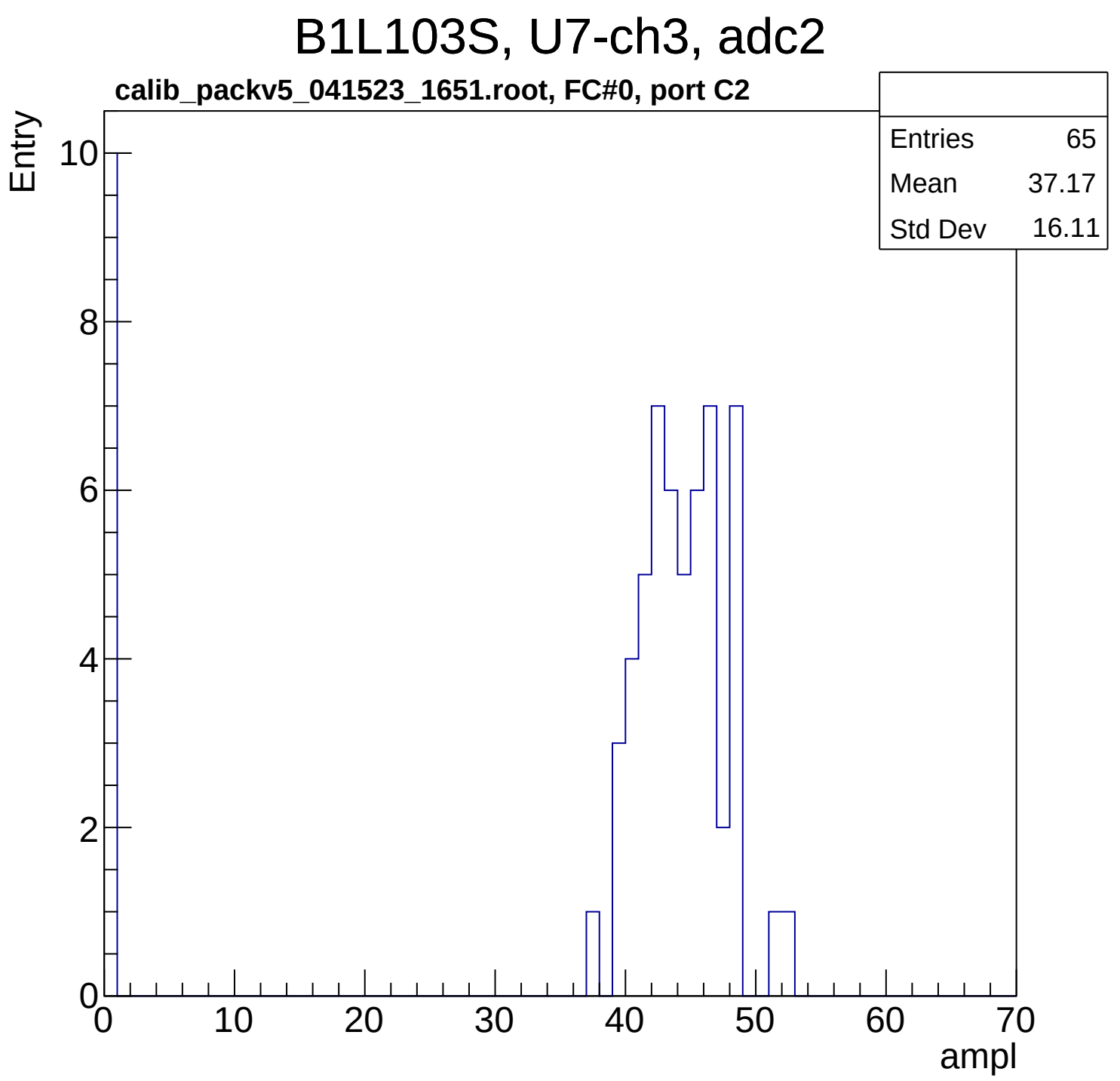
B1L103S, U7-ch3, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 37.17
Std Dev 16.11
Entry
ampl
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0
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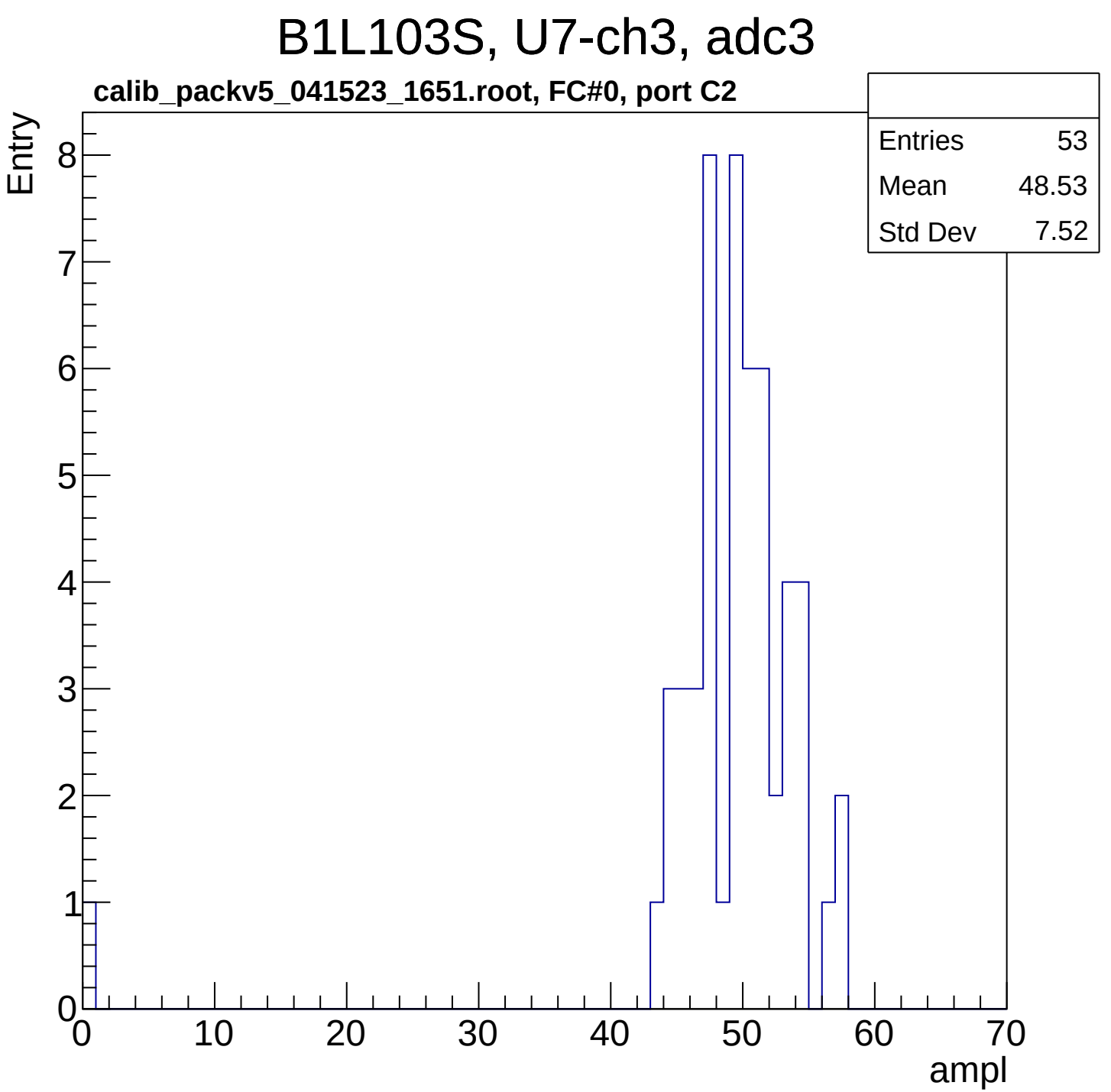
50
60
70


B1L103S, U7-ch3, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 48.53
Std Dev 7.52
Entry
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6
7
8
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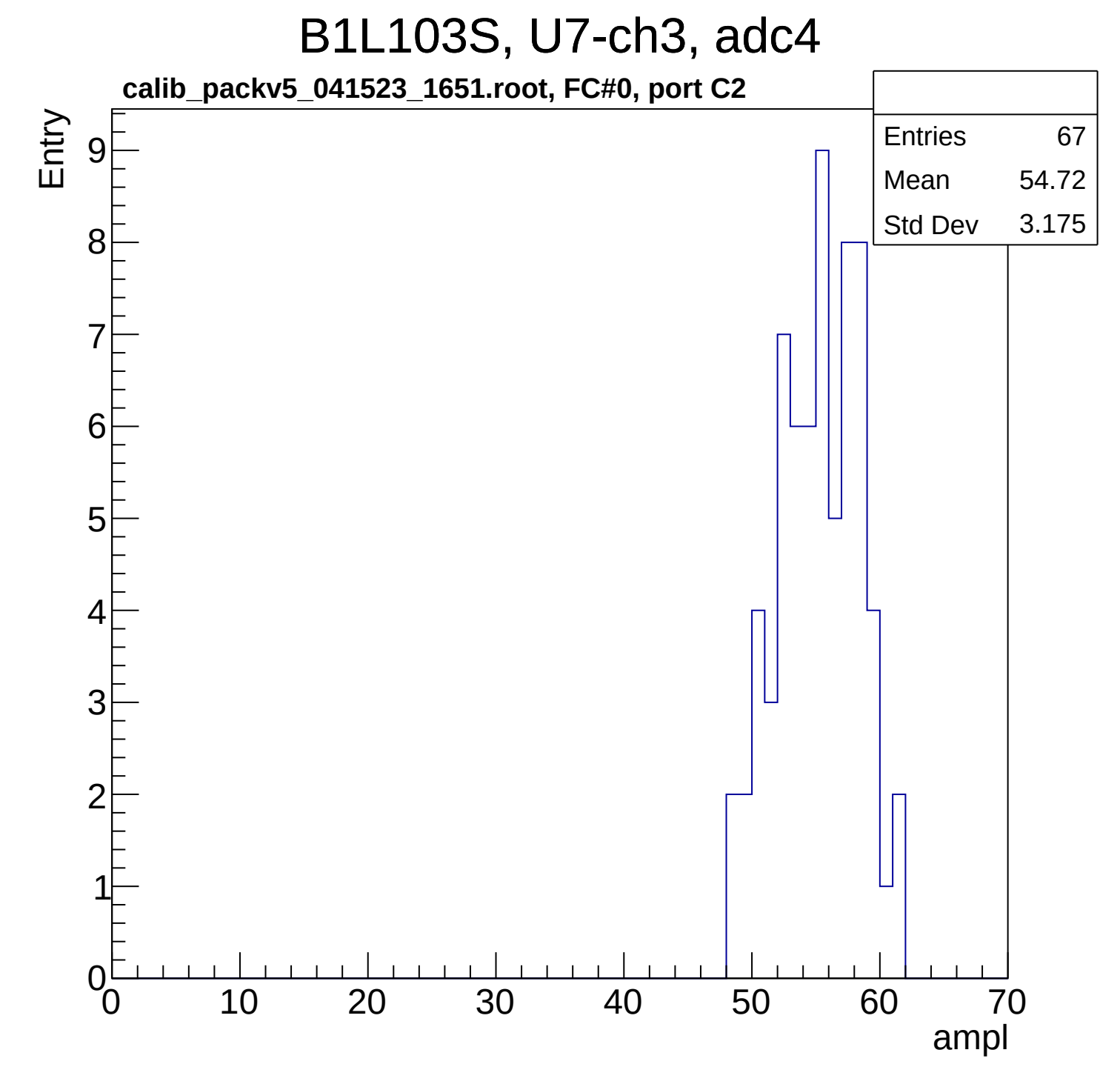
50
60
70
ampl


B1L103S, U7-ch3, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 54.72
Std Dev 3.175
Entry
ampl
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5
6
7
8
9
0
10
20
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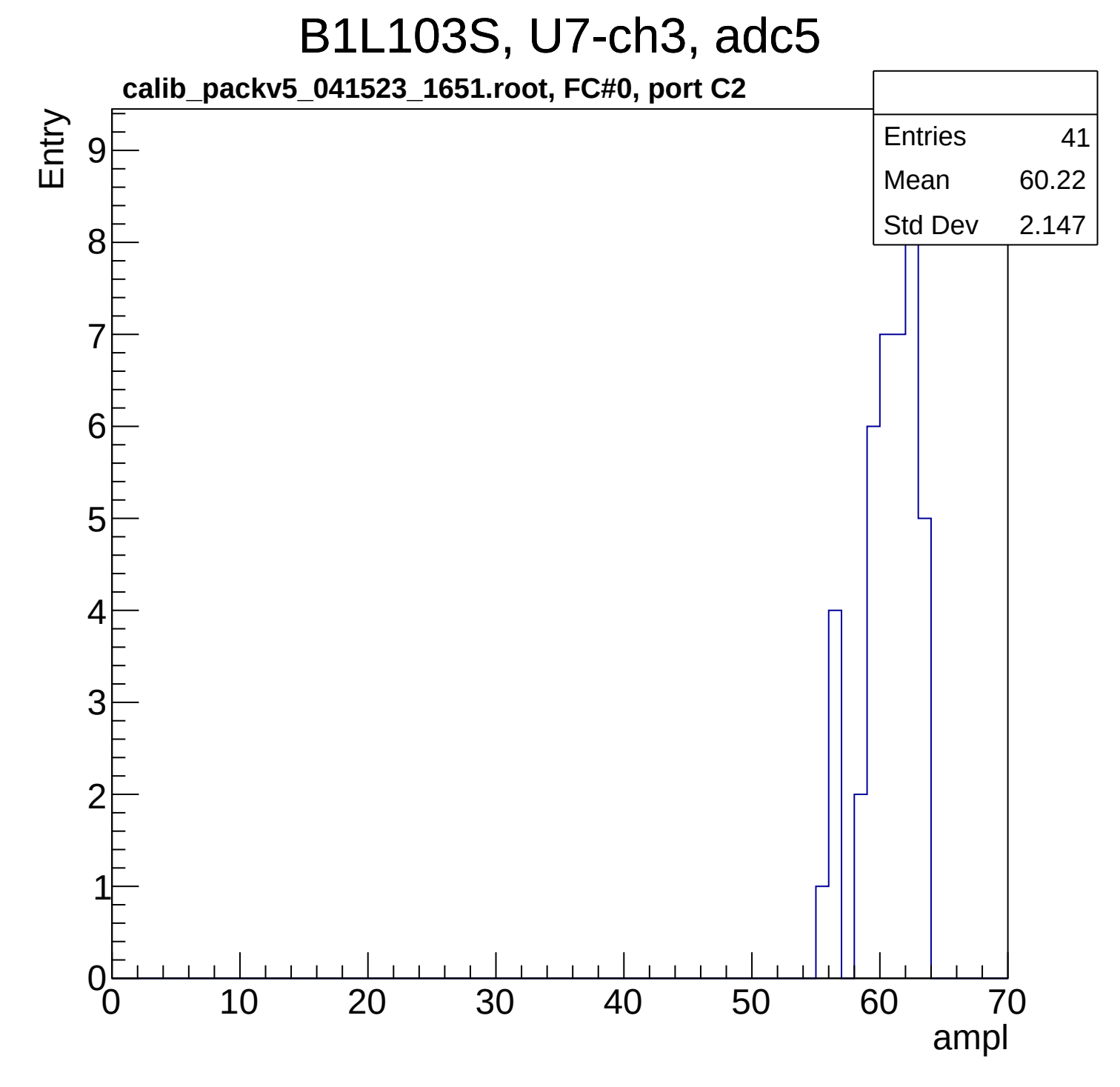
40
50
60
70


B1L103S, U7-ch3, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 41
Mean 60.22
Std Dev 2.147
Entry
ampl
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3
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6
7
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0
10
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60
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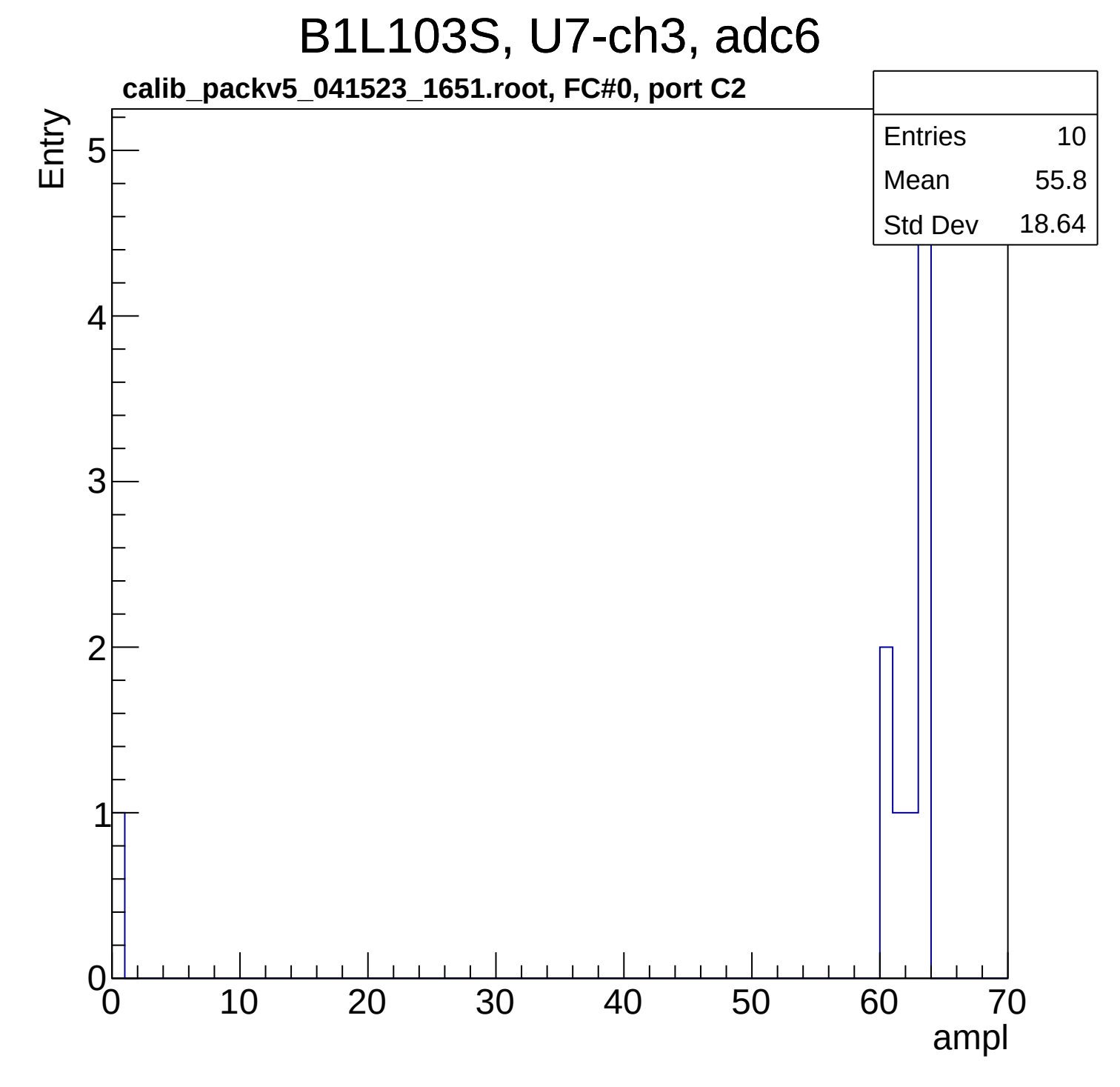
B1L103S, U7-ch3, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 55.8
Std Dev 18.64
Entry
ampl
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60
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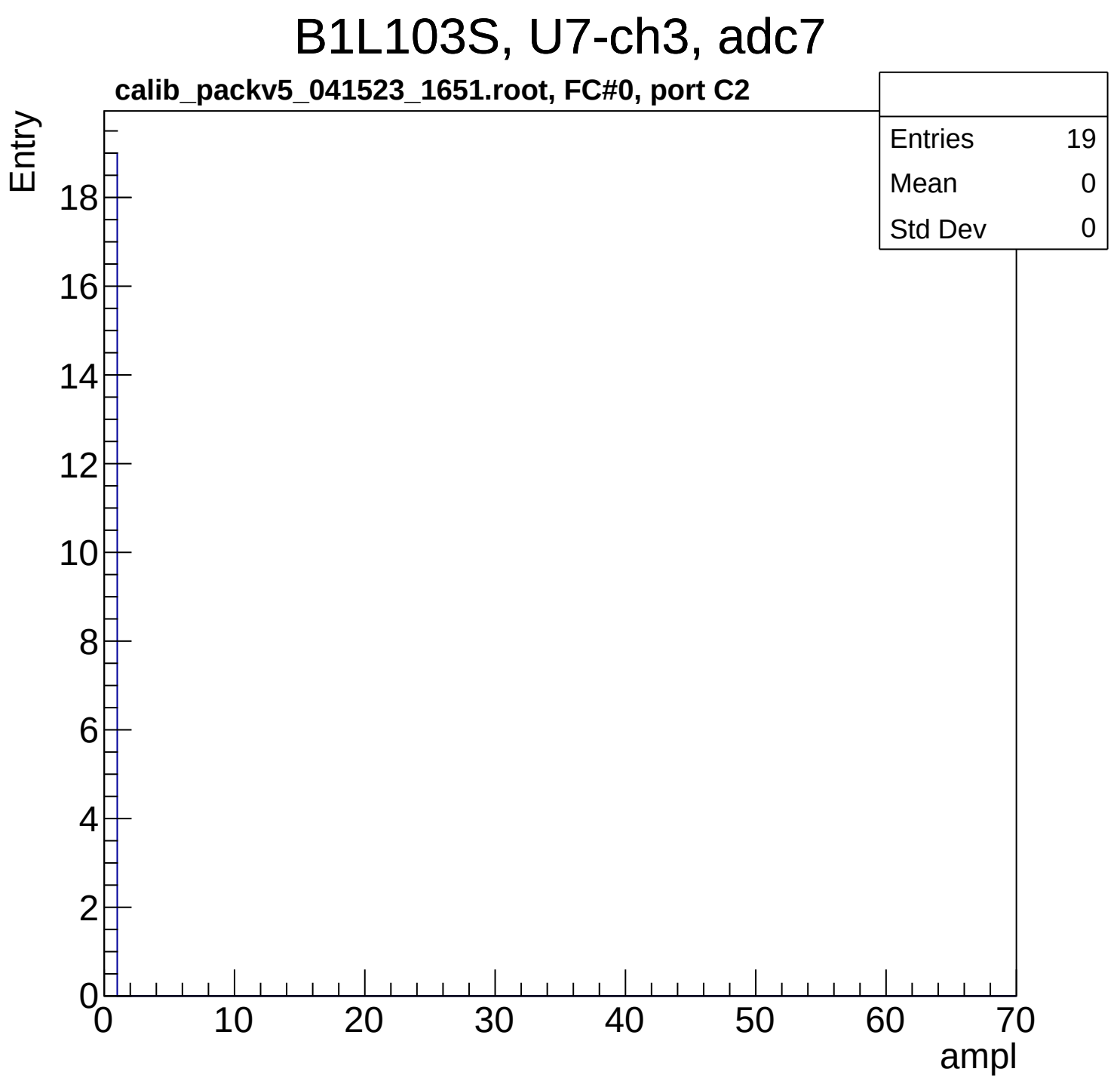
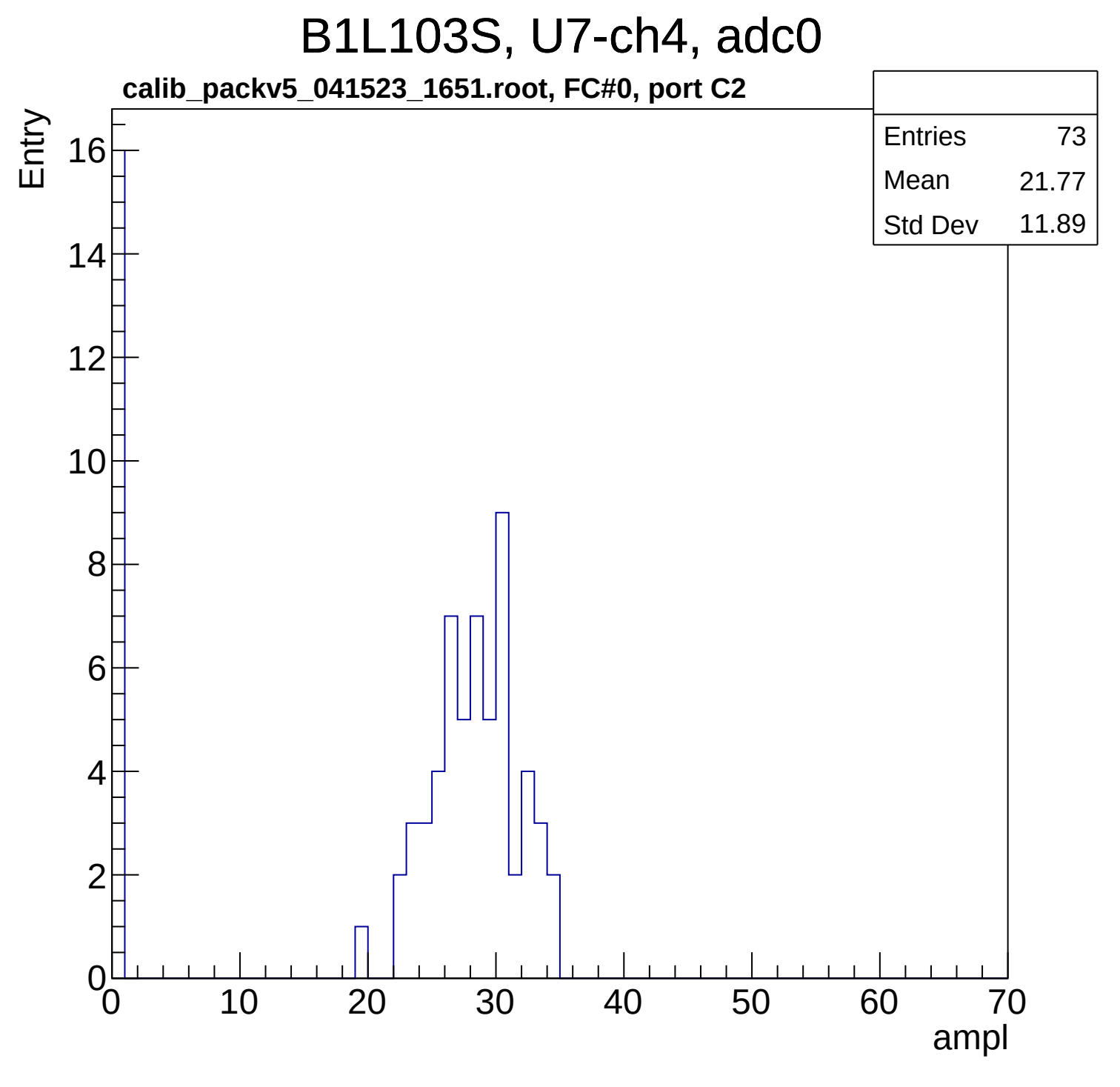

B1L103S, U7-ch3, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch4, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 21.77
Std Dev 11.89
Entry
ampl
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2
4
6
8
10
12
14
16
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60
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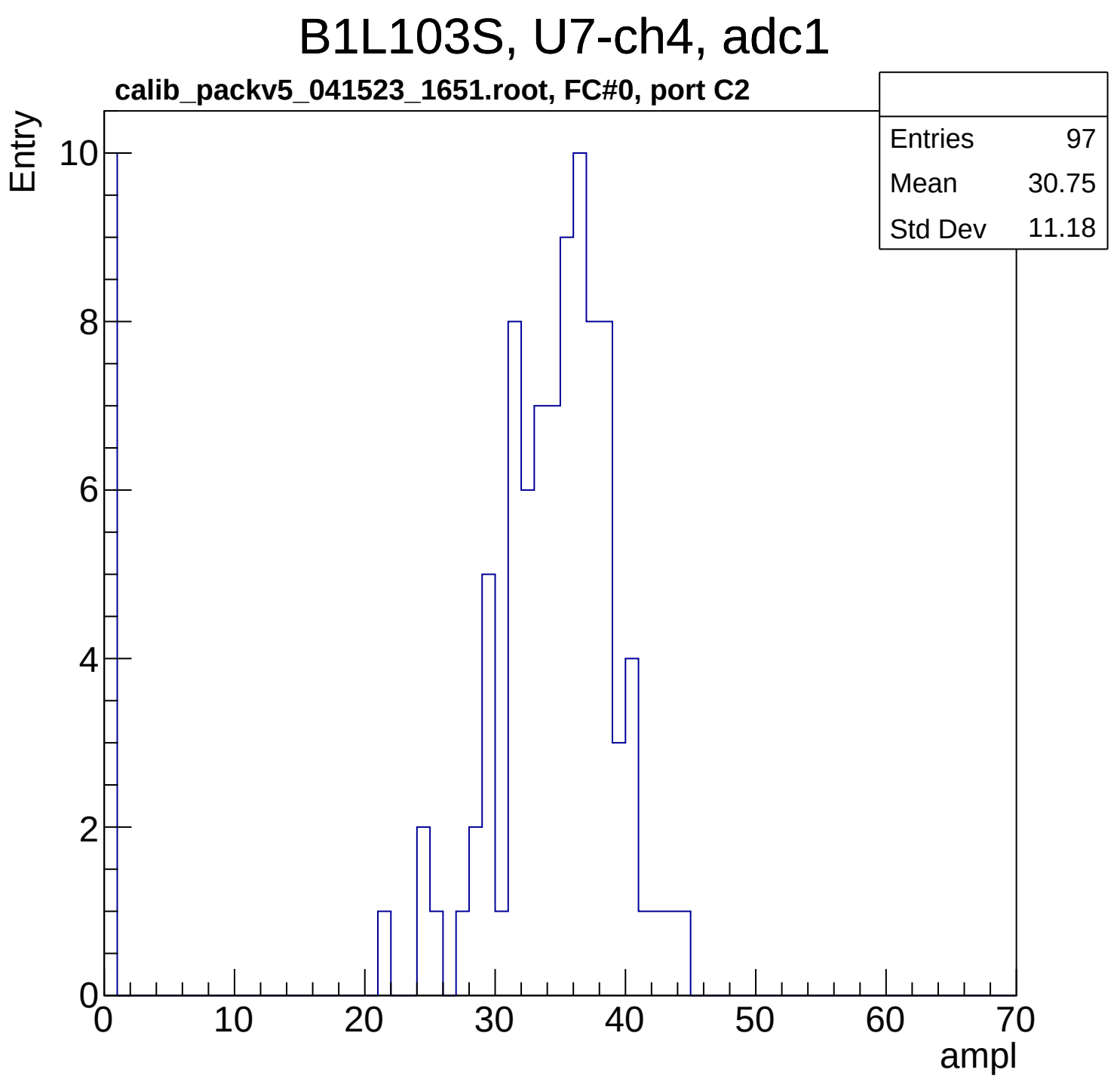
B1L103S, U7-ch4, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 97
Mean 30.75
Std Dev 11.18
Entry
ampl
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2
4
6
8
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0
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20
30
40
50
60
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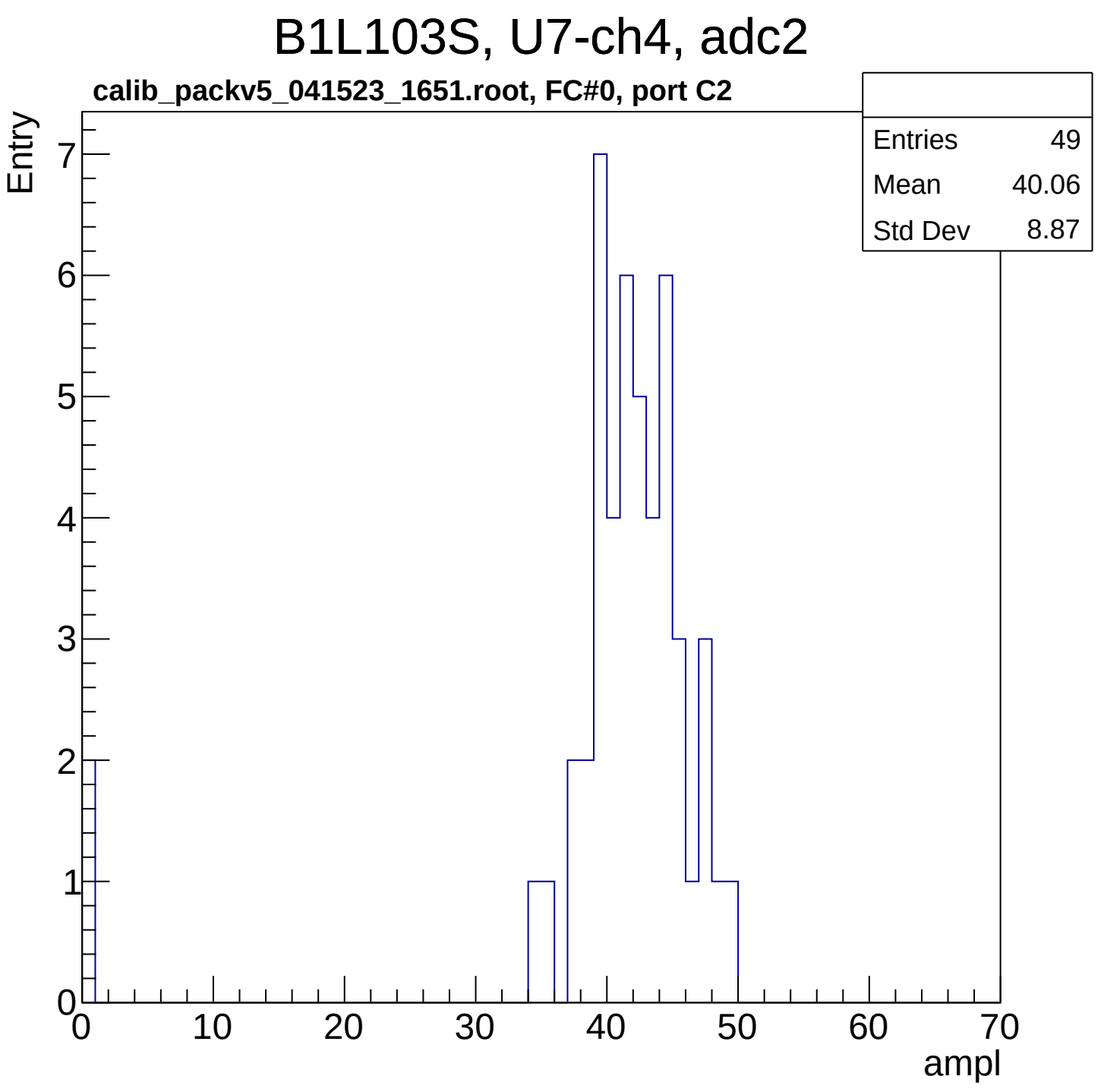
B1L103S, U7-ch4, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 40.06
Std Dev 8.87
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
30
40
50
60
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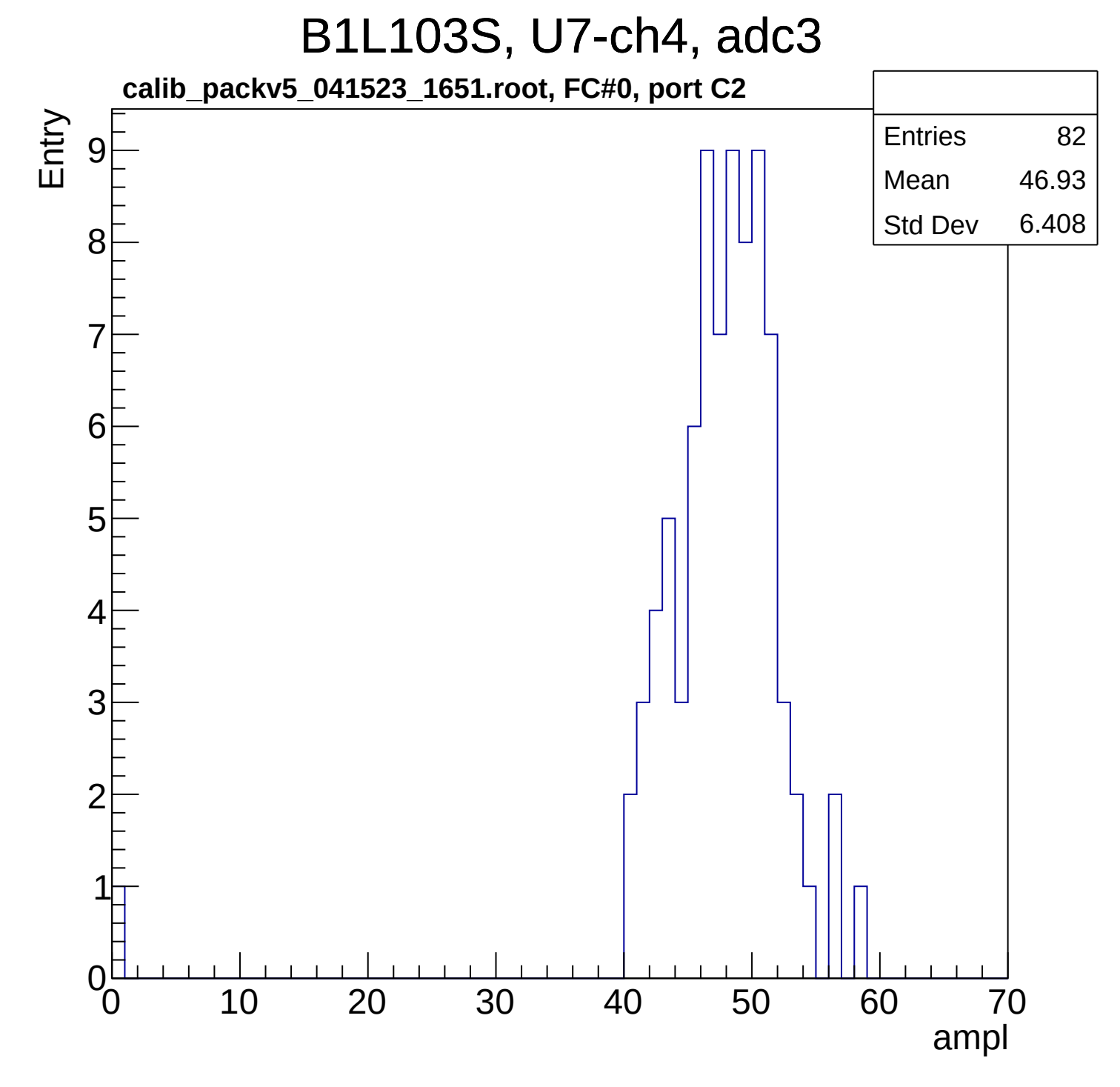
B1L103S, U7-ch4, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 46.93
Std Dev 6.408
Entry
ampl
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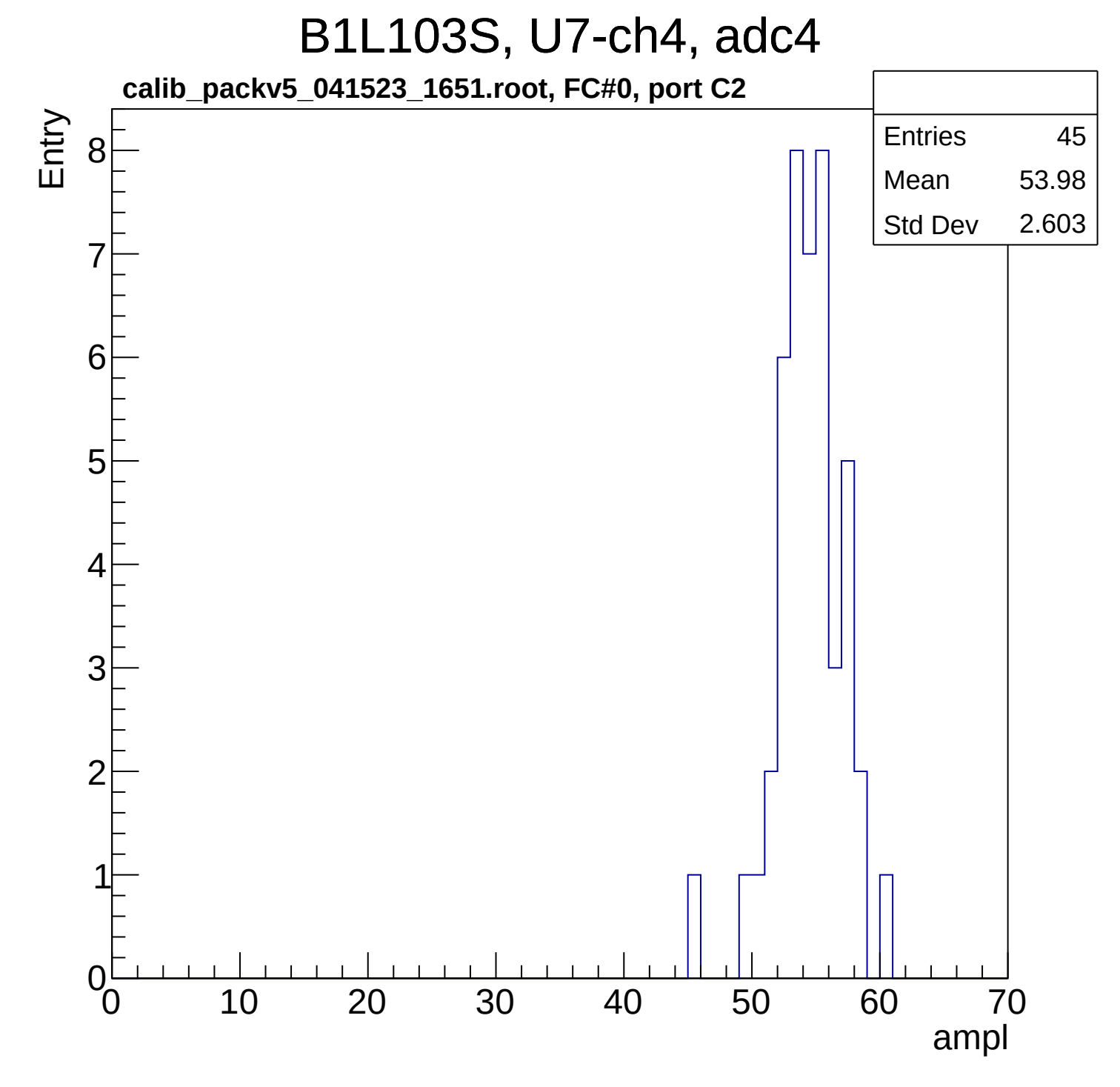
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U7-ch4, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 53.98
Std Dev 2.603
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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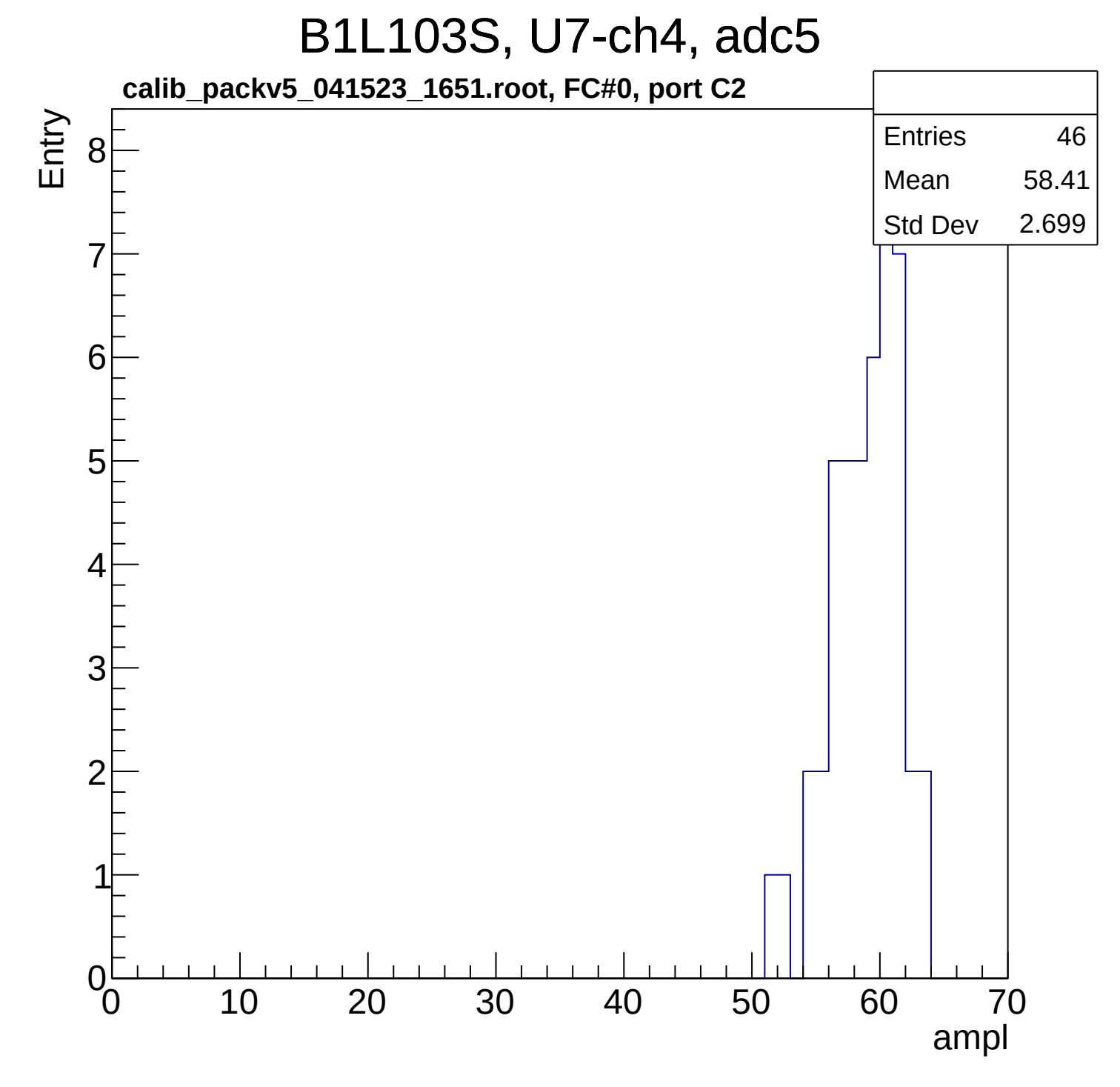
B1L103S, U7-ch4, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 58.41
Std Dev 2.699
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
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60
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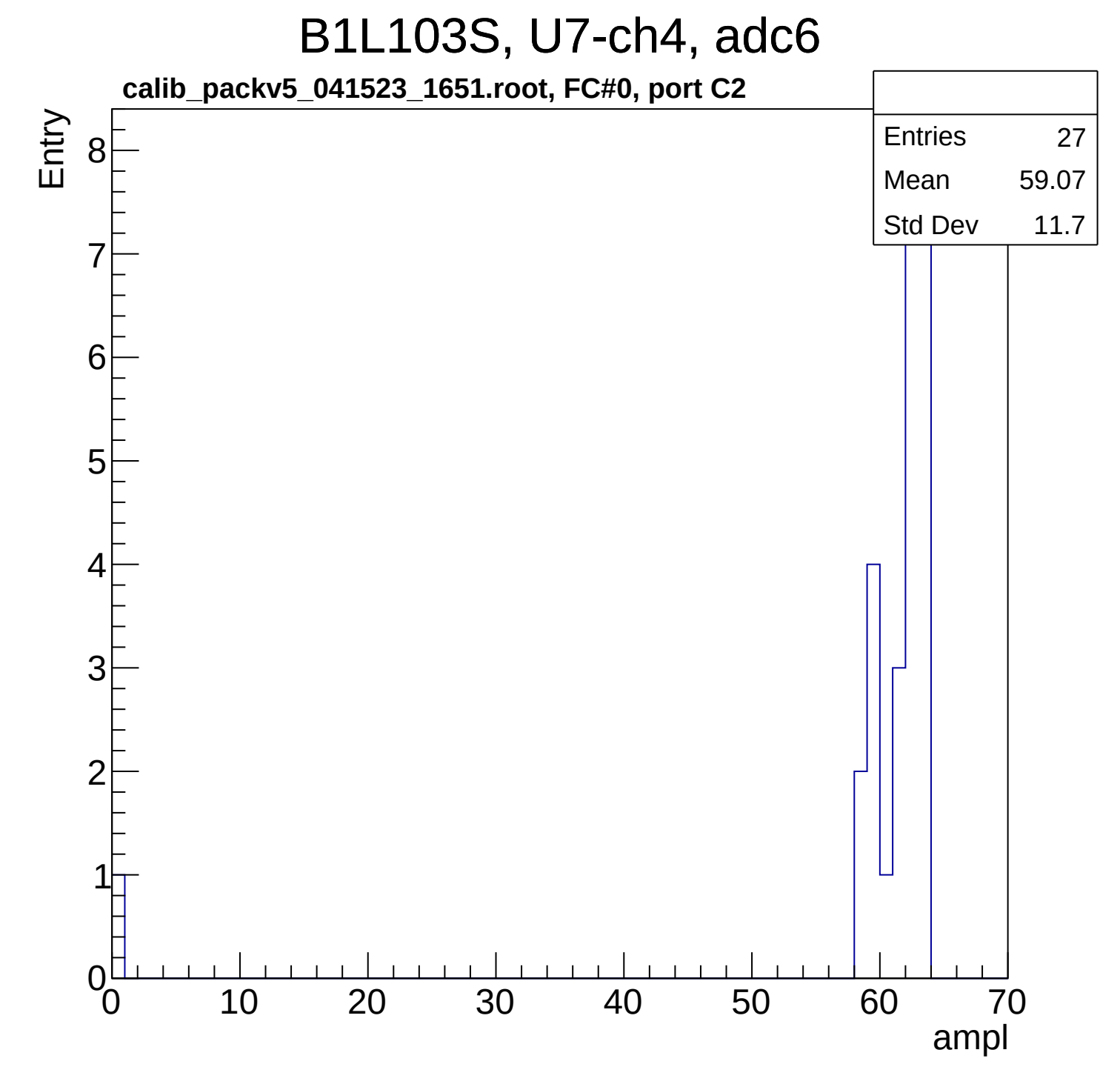
B1L103S, U7-ch4, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 27
Mean 59.07
Std Dev 11.7
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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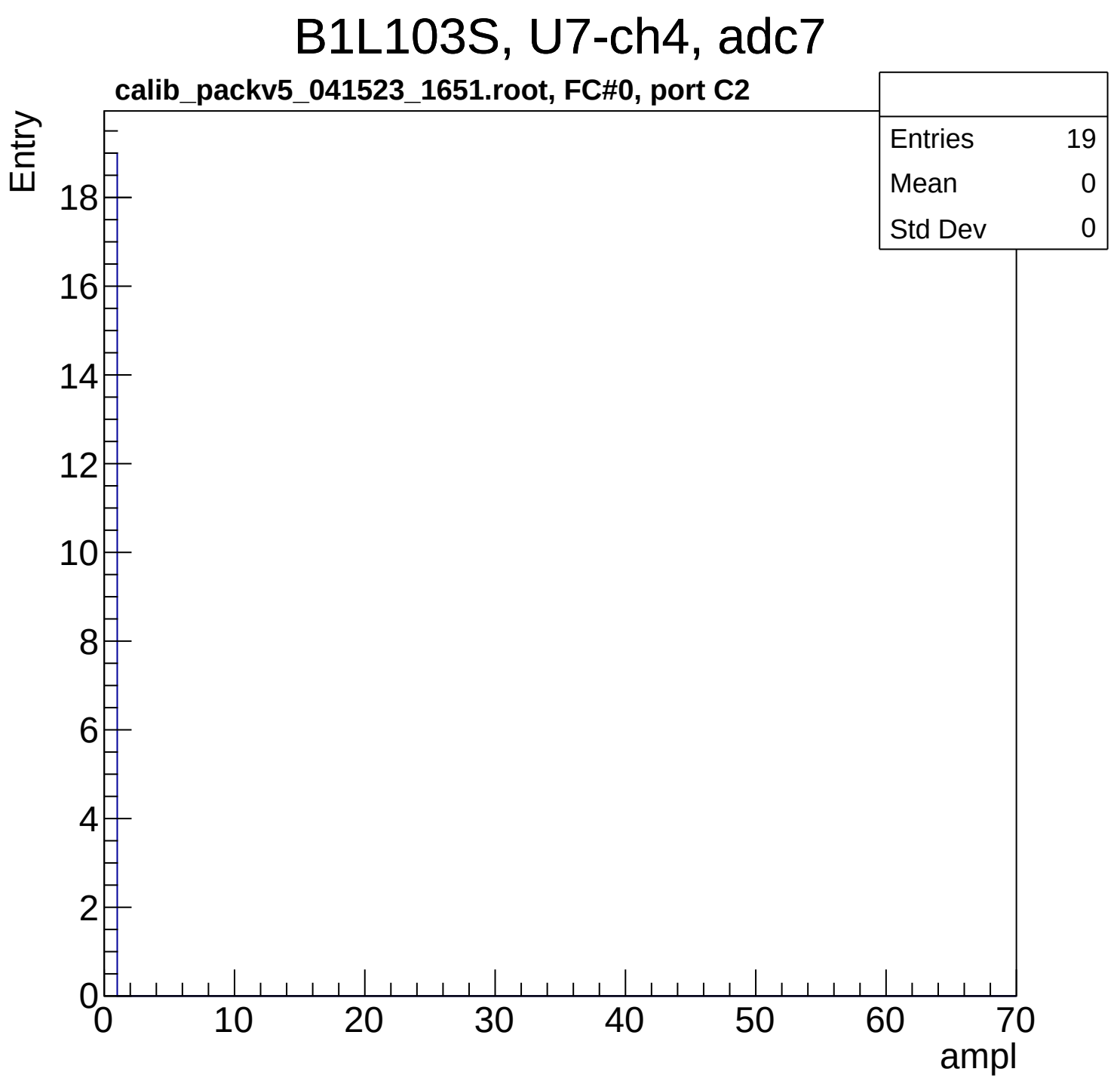
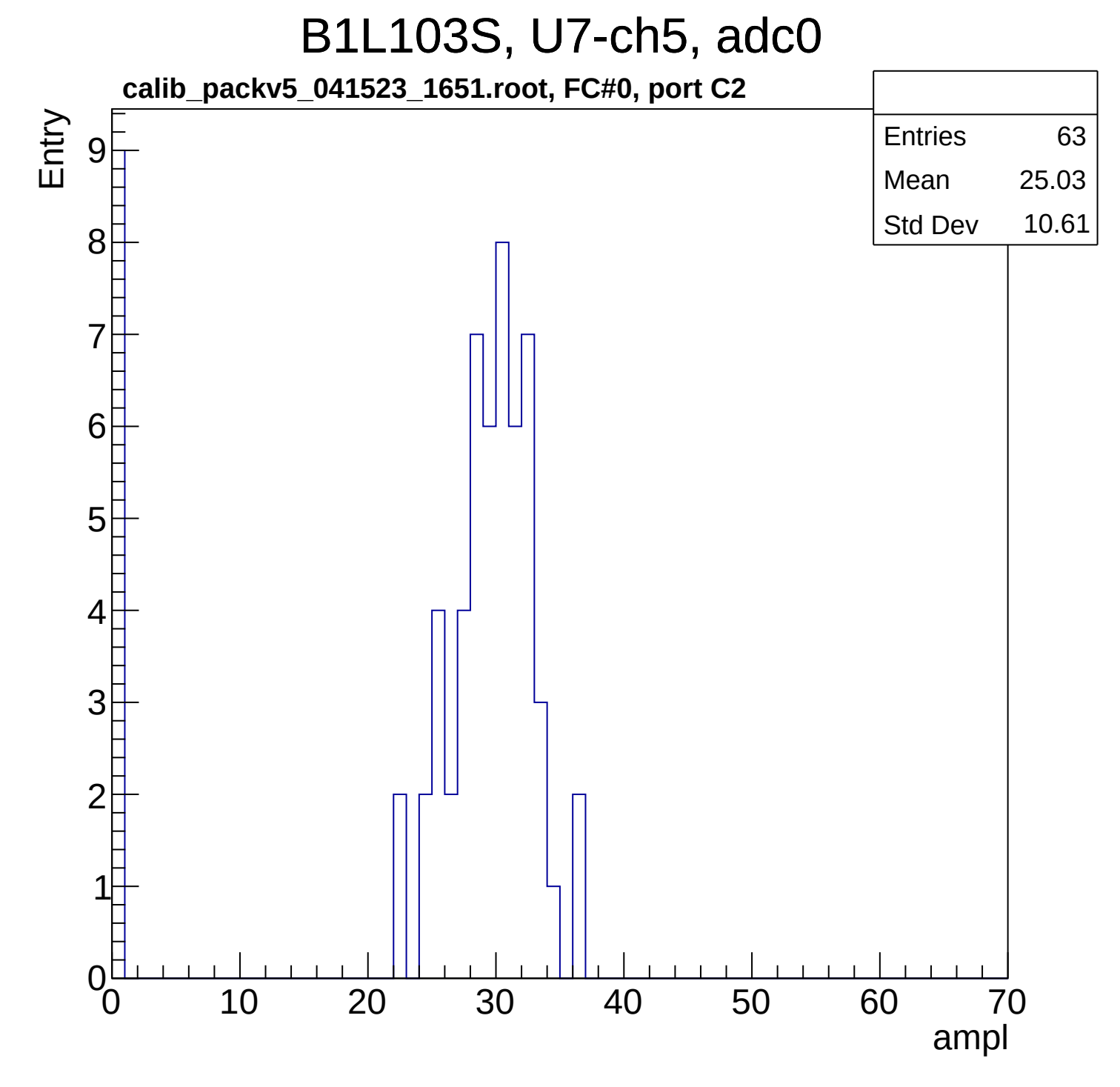
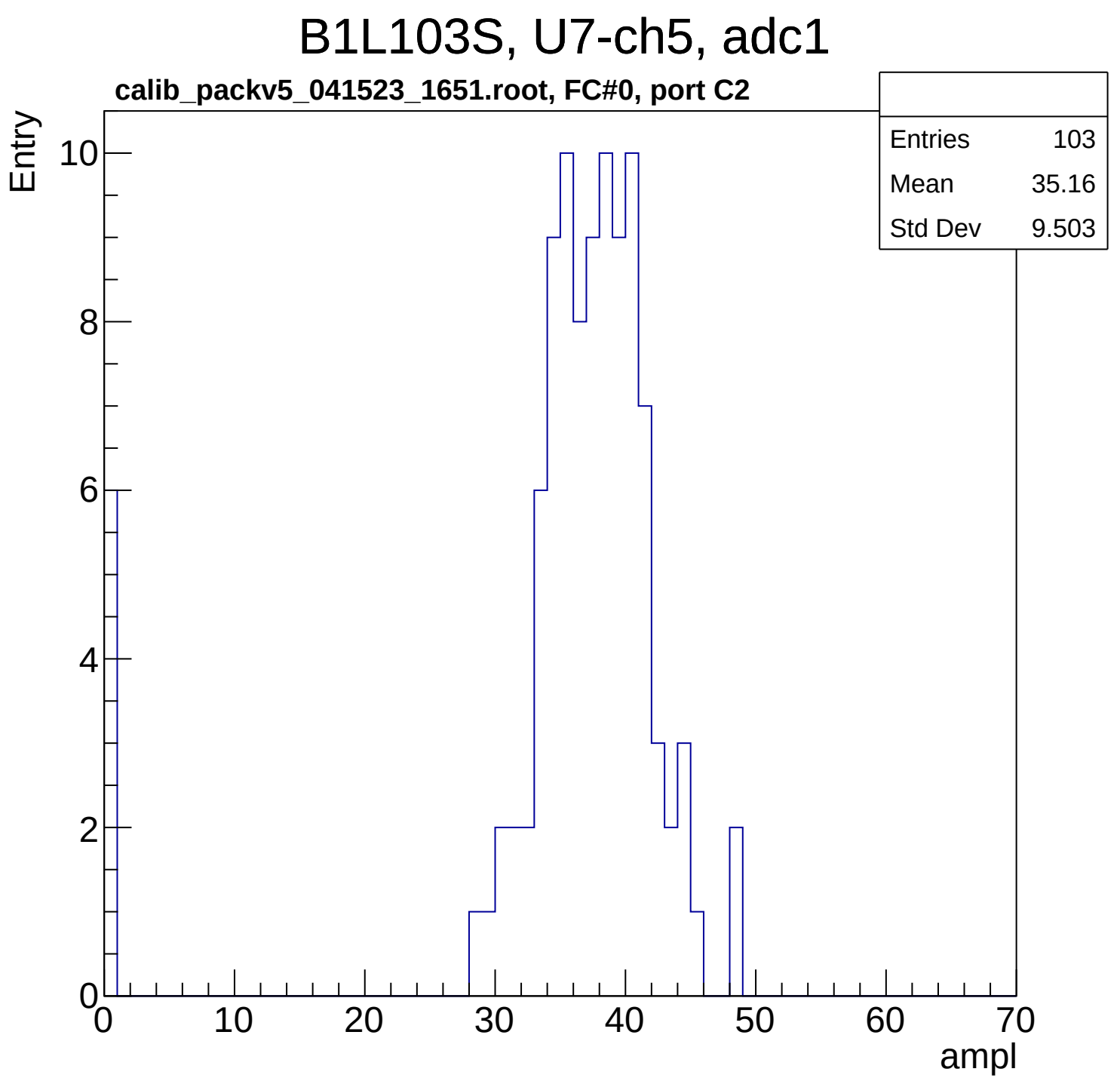
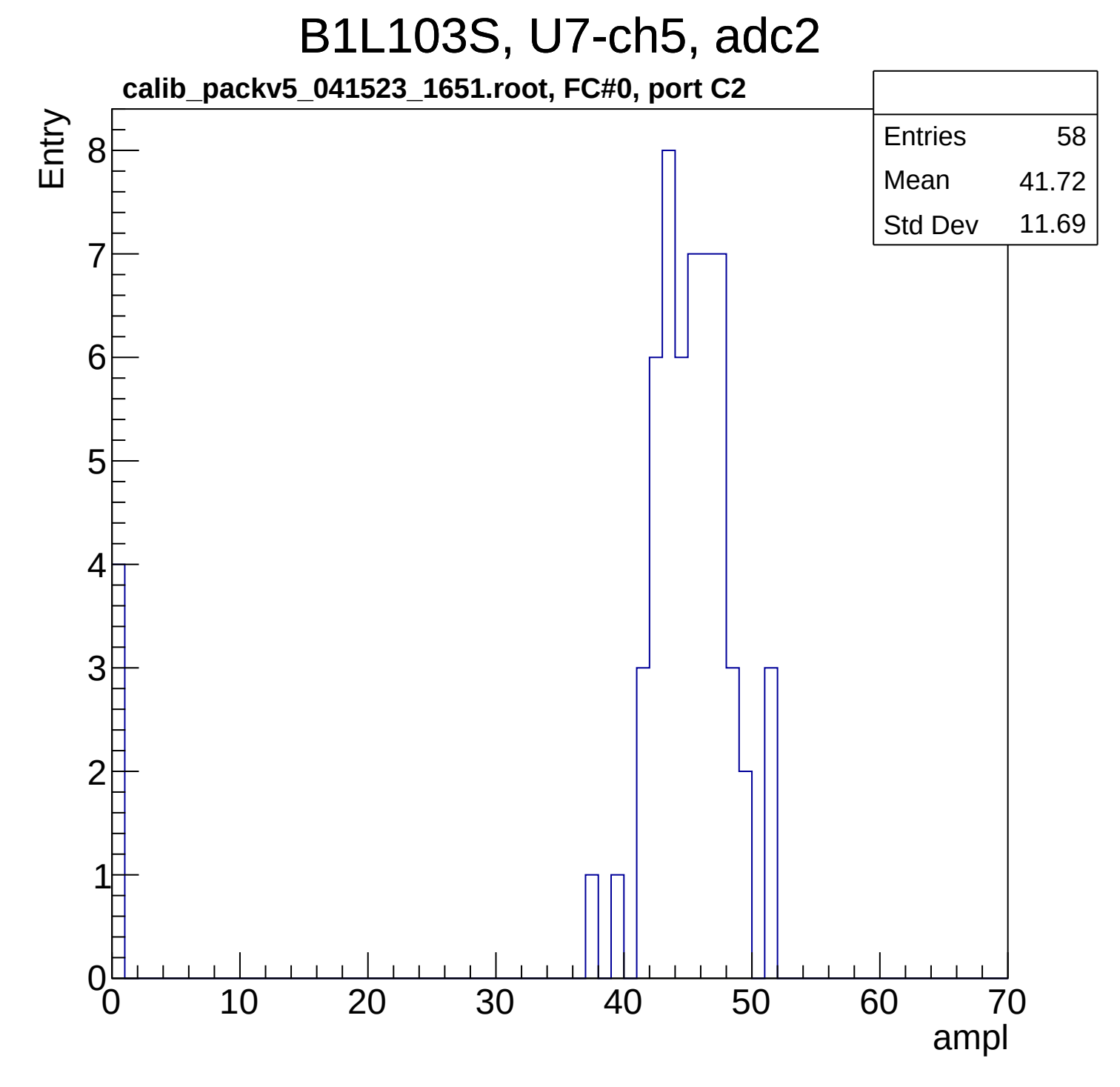

B1L103S, U7-ch4, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch5, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 25.03
Std Dev 10.61
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U7-ch5, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 103
Mean 35.16
Std Dev 9.503
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U7-ch5, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 41.72
Std Dev 11.69
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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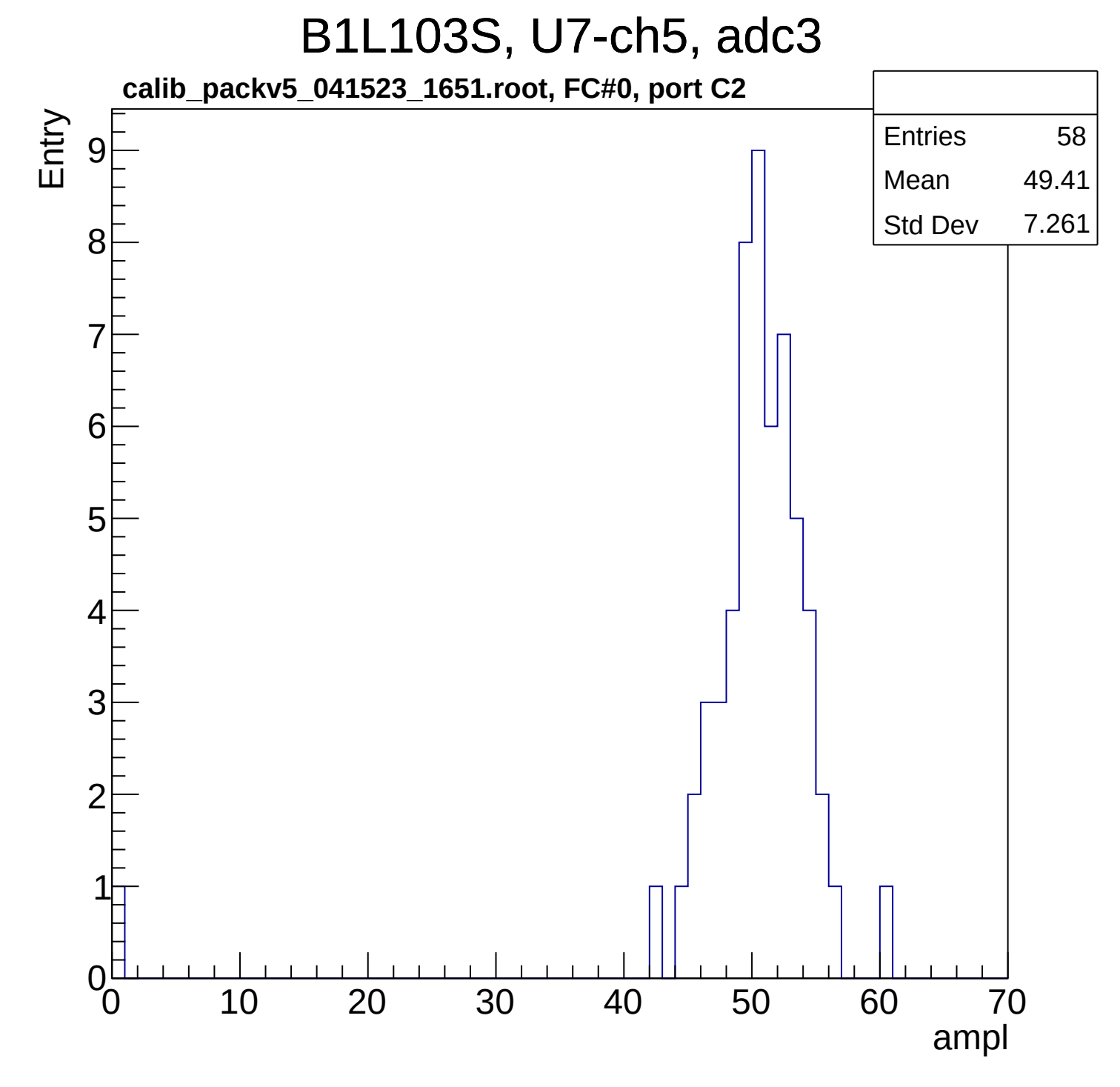
B1L103S, U7-ch5, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 49.41
Std Dev 7.261
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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40
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60
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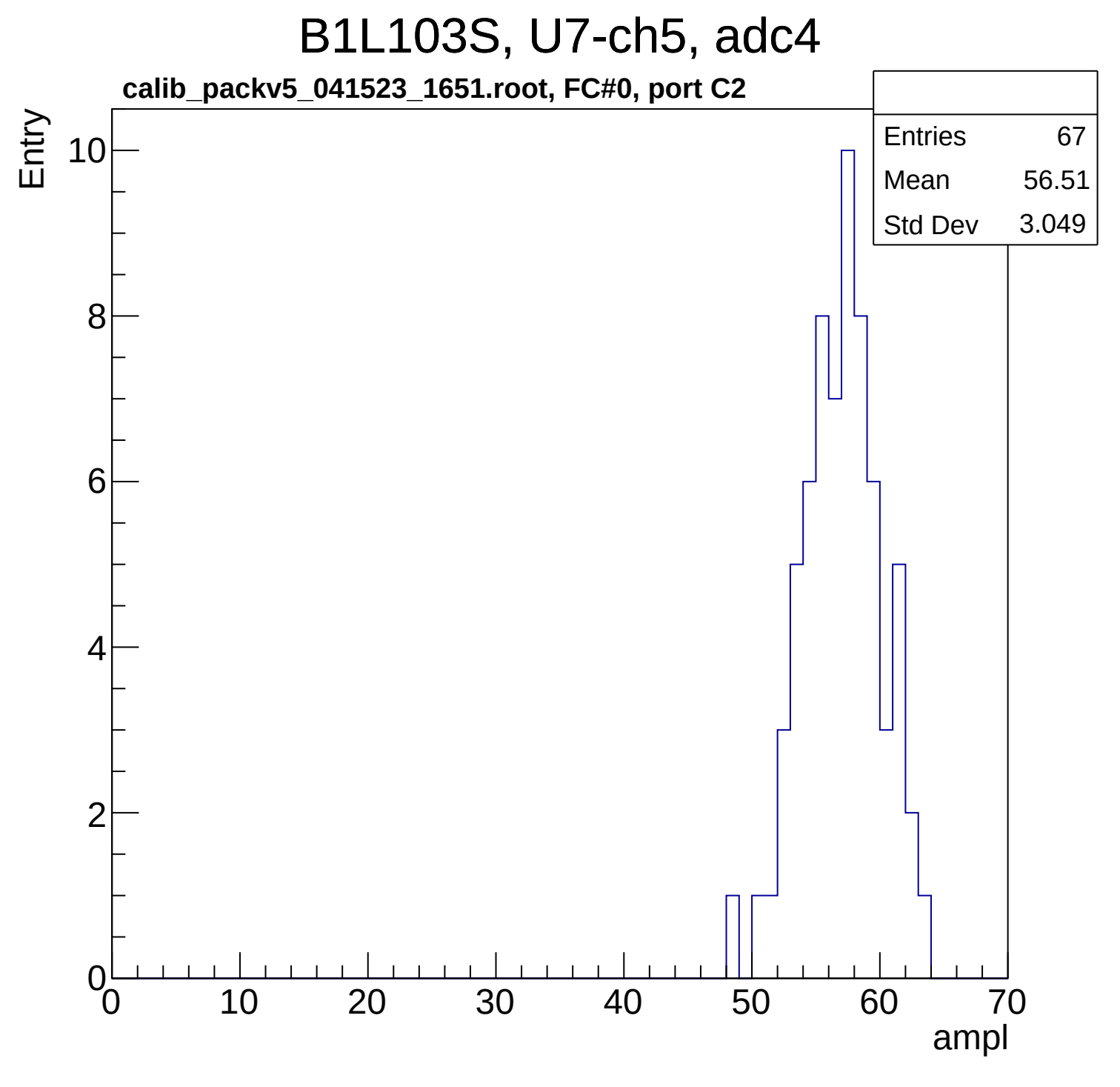
B1L103S, U7-ch5, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 56.51
Std Dev 3.049
Entry
ampl
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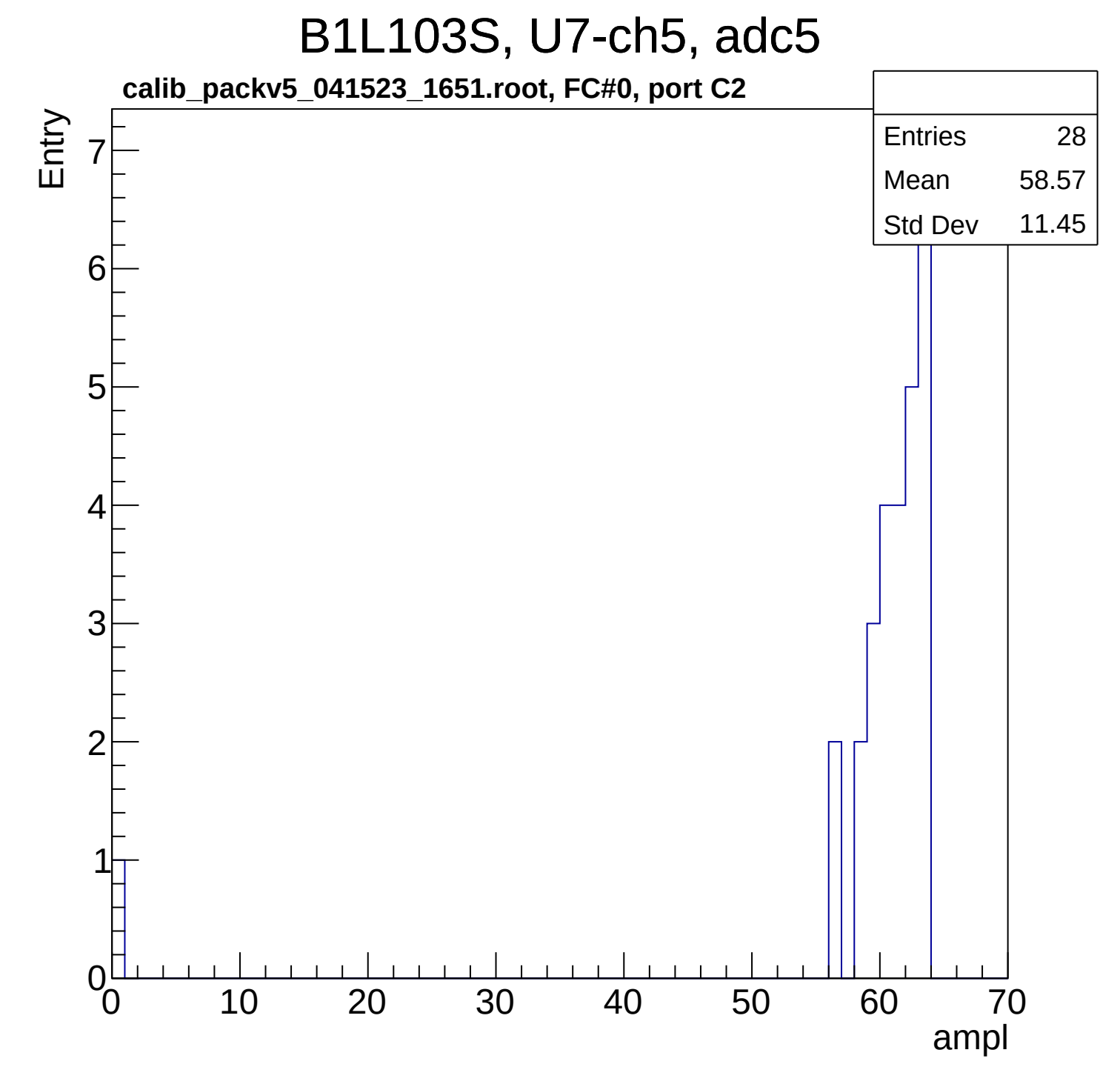
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U7-ch5, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 28
Mean 58.57
Std Dev 11.45
Entry
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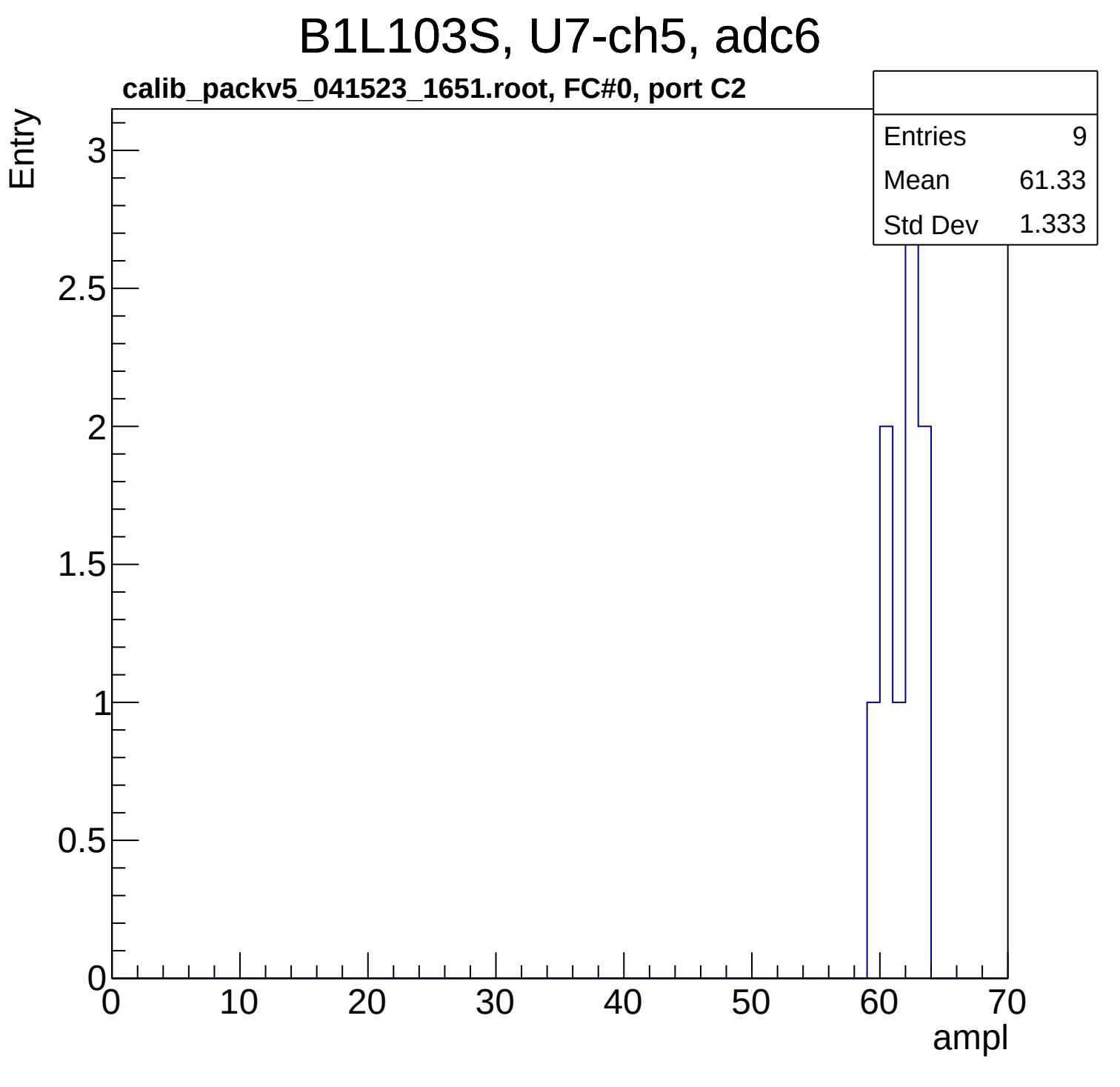
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch5, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 9
Mean 61.33
Std Dev 1.333
Entry
ampl
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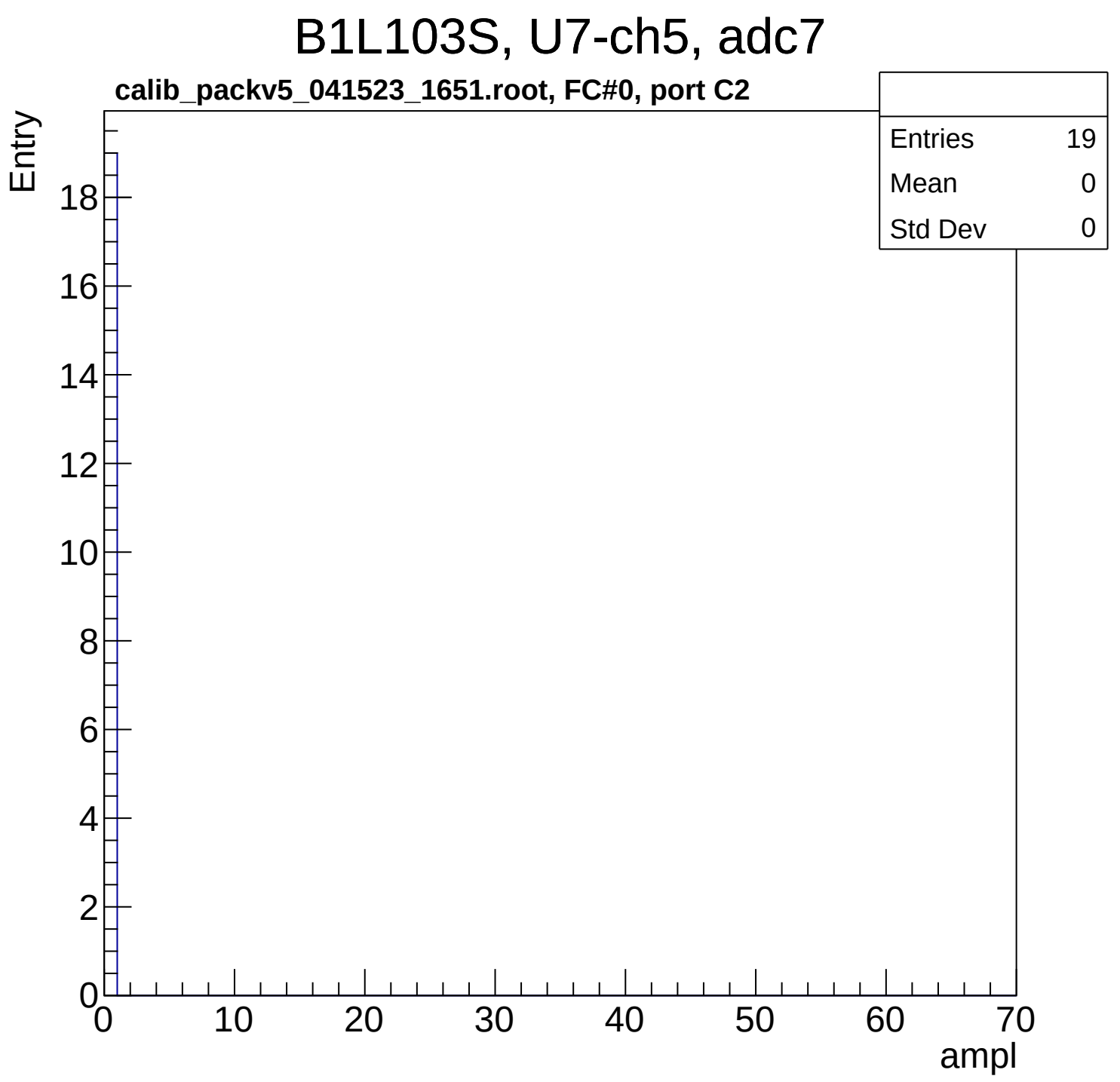
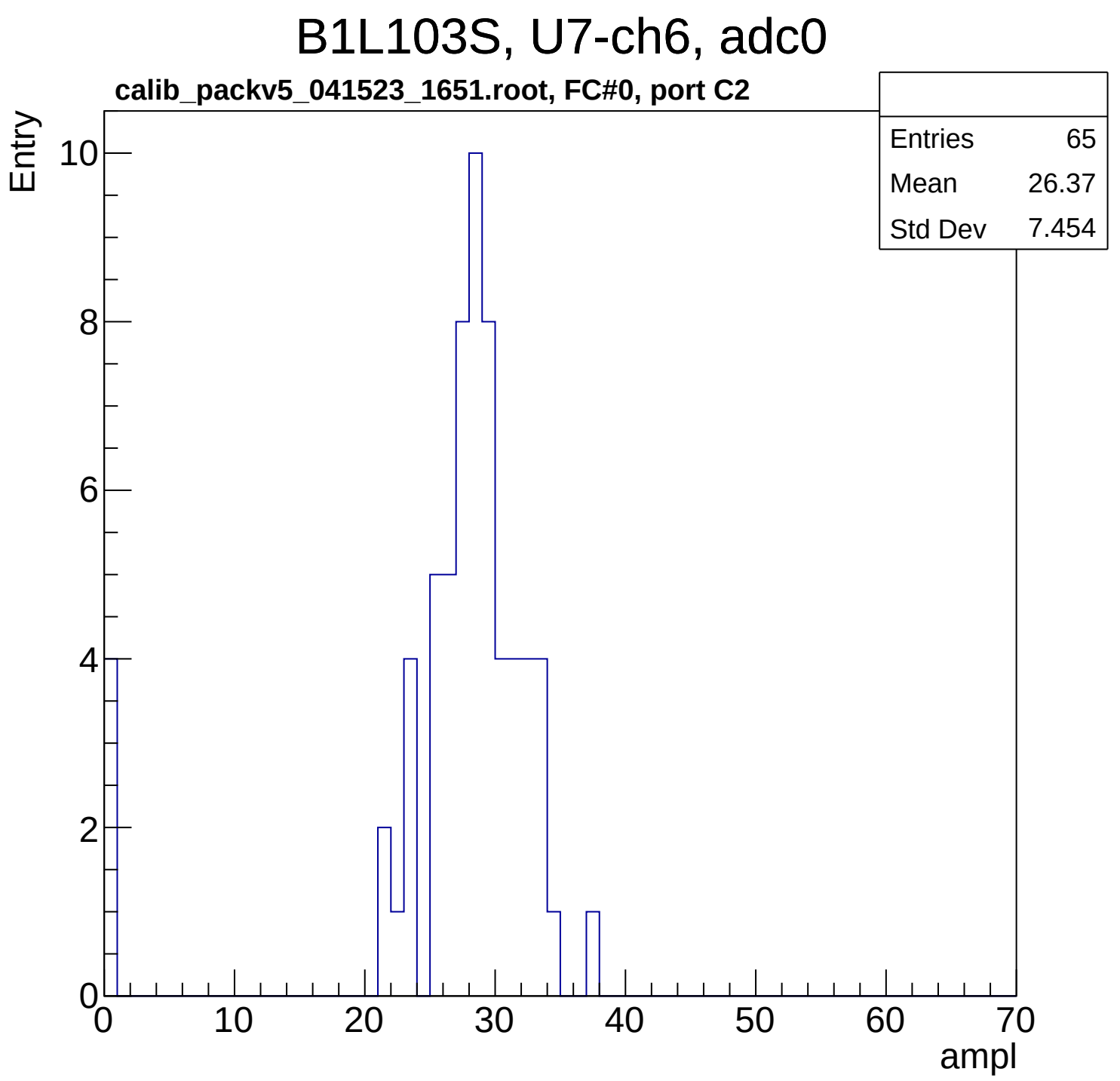
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U7-ch5, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch6, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 26.37
Std Dev 7.454
Entry
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2
4
6
8
10
0
10
20
30
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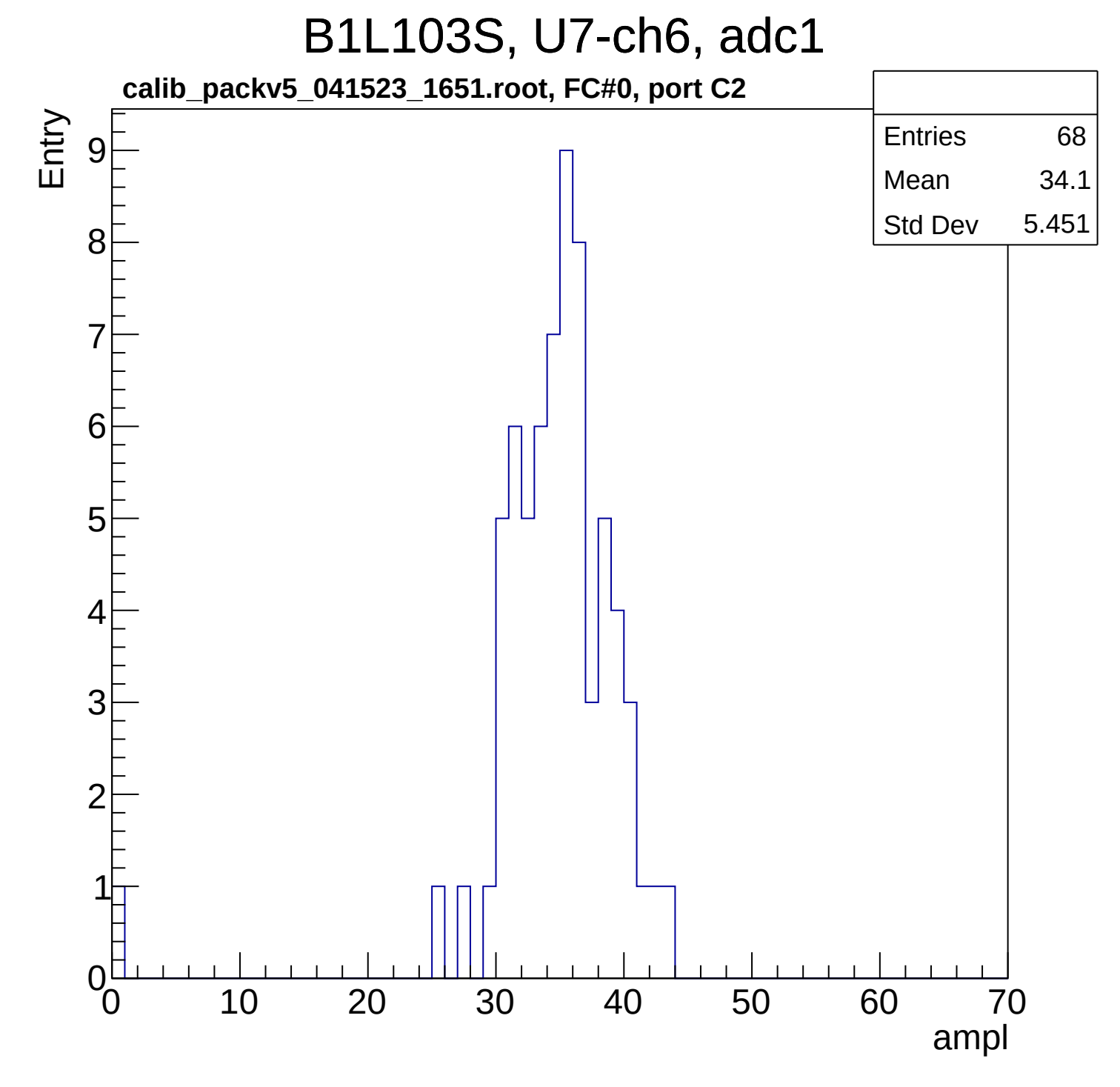
50
60
70
ampl


B1L103S, U7-ch6, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 34.1
Std Dev 5.451
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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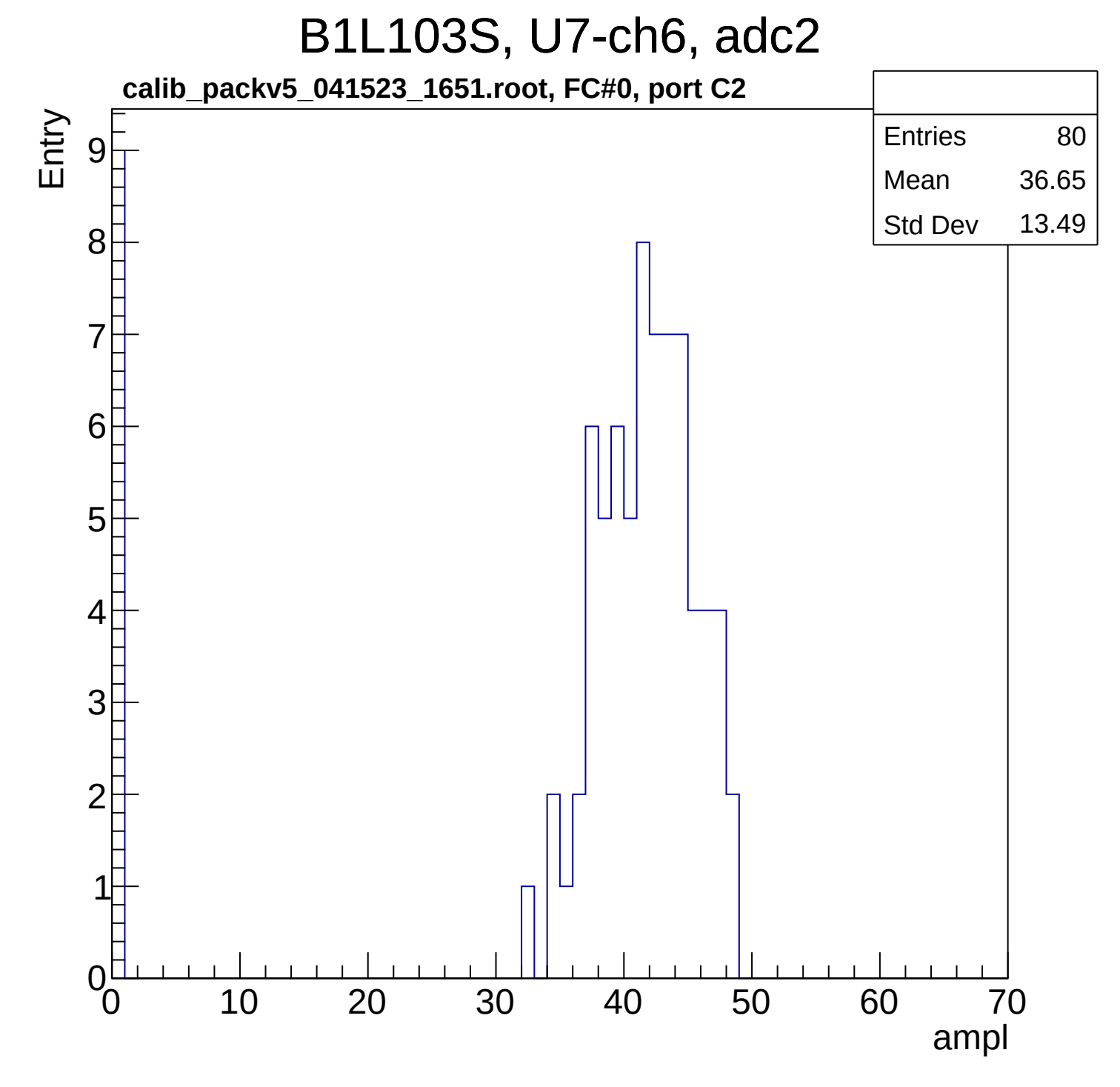
40
50
60
70


B1L103S, U7-ch6, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 36.65
Std Dev 13.49
Entry
ampl
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2
3
4
5
6
7
8
9
0
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40
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60
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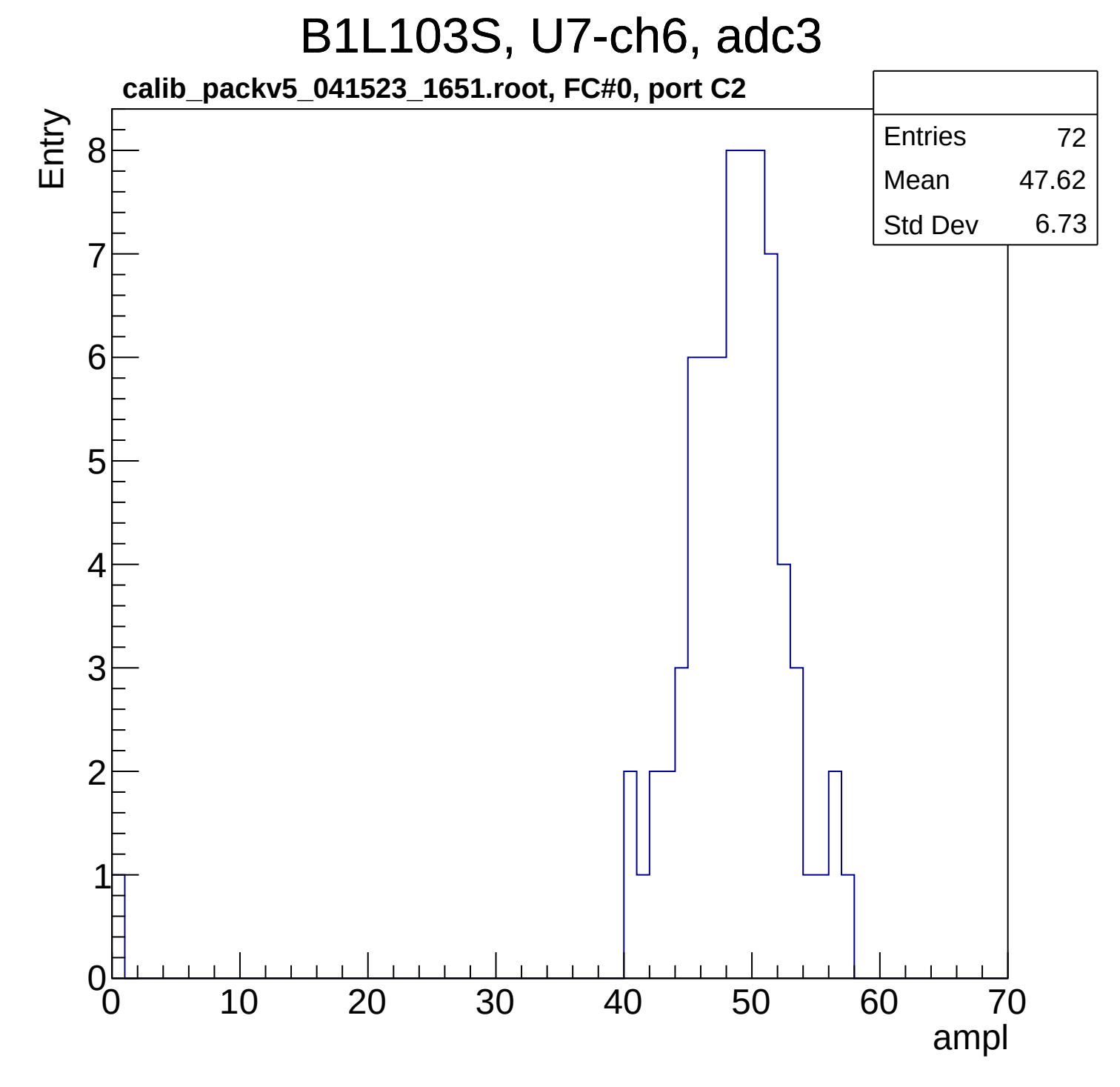
B1L103S, U7-ch6, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 47.62
Std Dev 6.73
Entry
ampl
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2
3
4
5
6
7
8
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60
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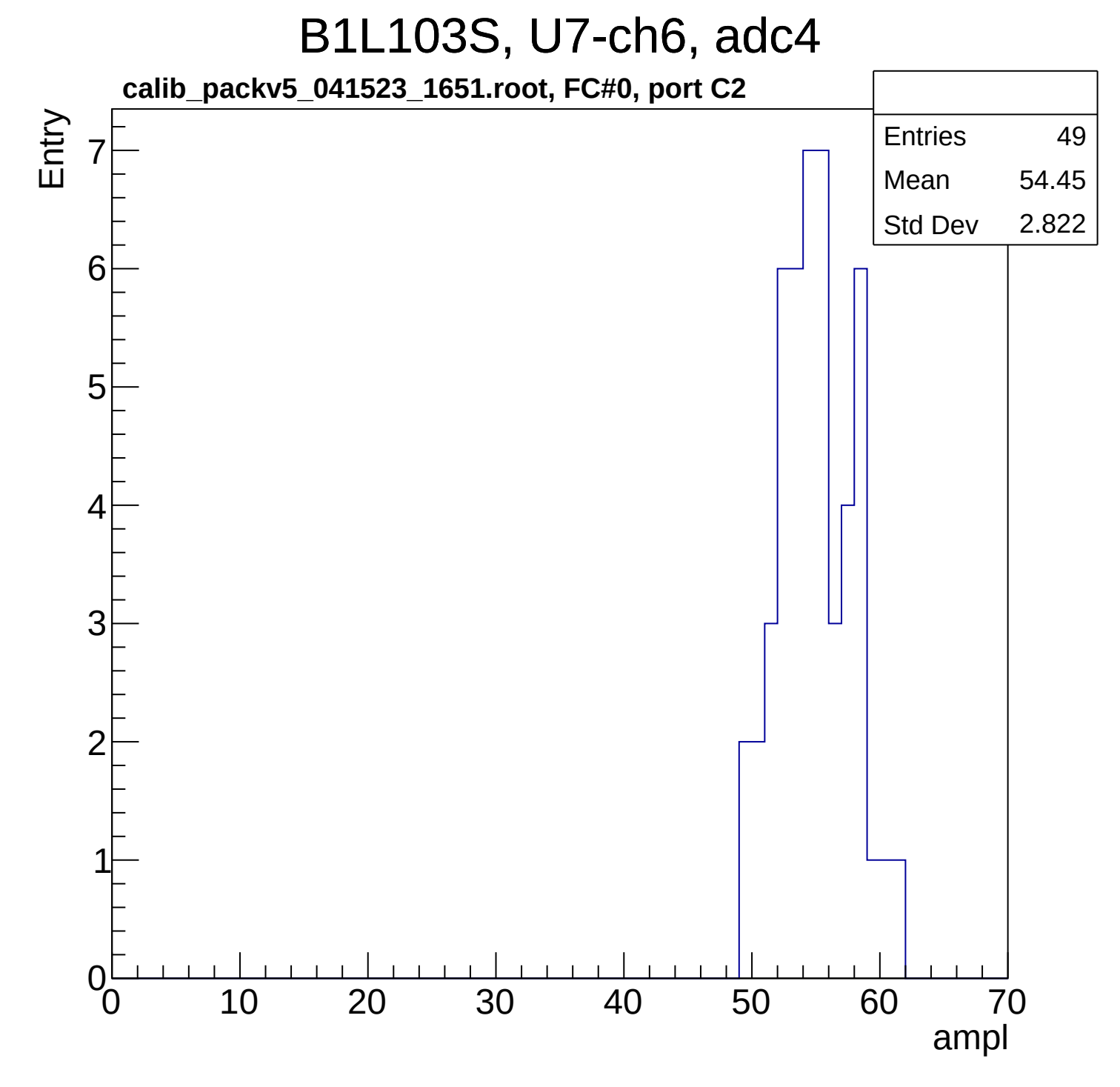
B1L103S, U7-ch6, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 54.45
Std Dev 2.822
Entry
ampl
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3
4
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0
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40
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60
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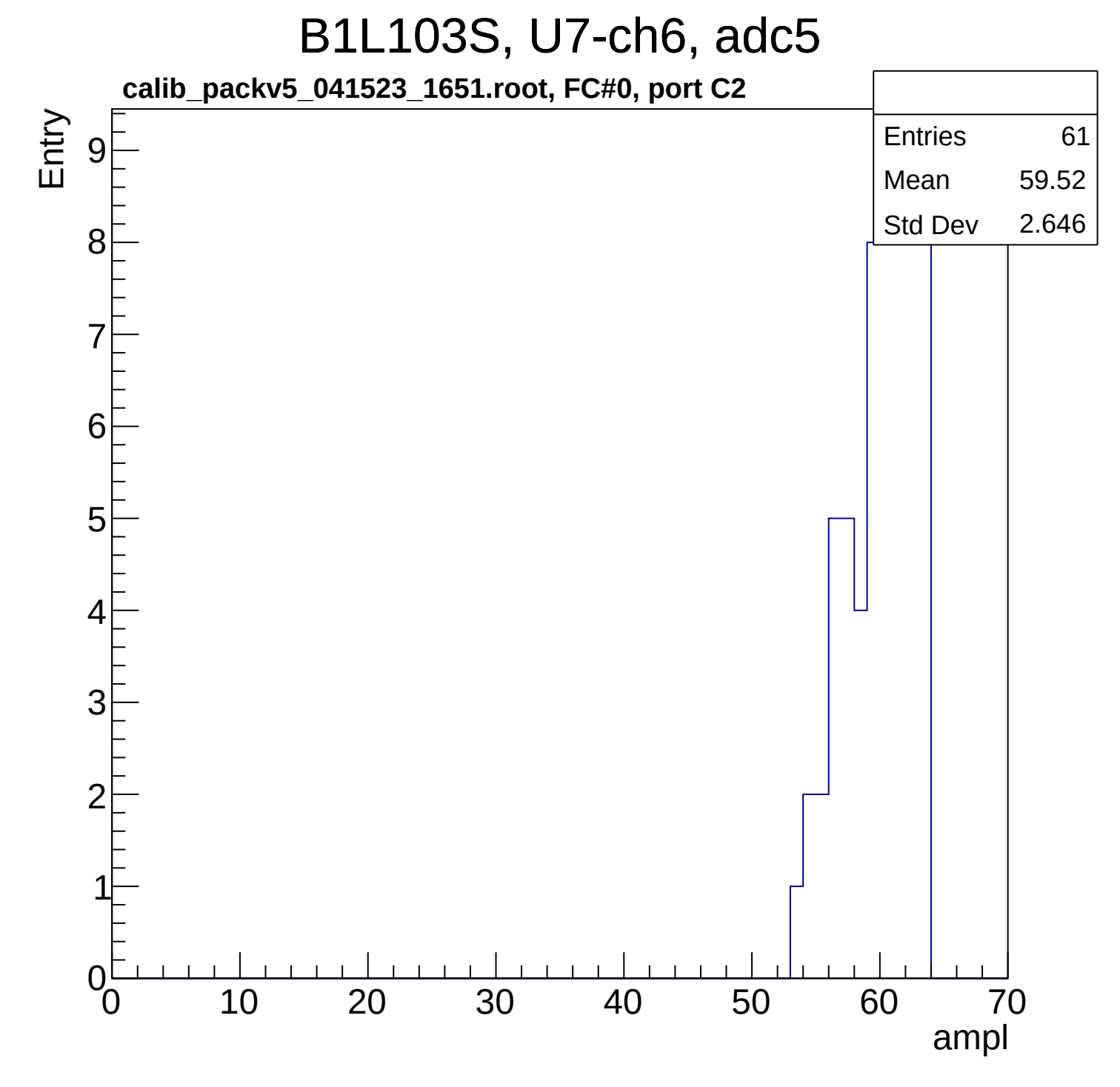
B1L103S, U7-ch6, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 59.52
Std Dev 2.646
Entry
ampl
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2
3
4
5
6
7
8
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0
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60
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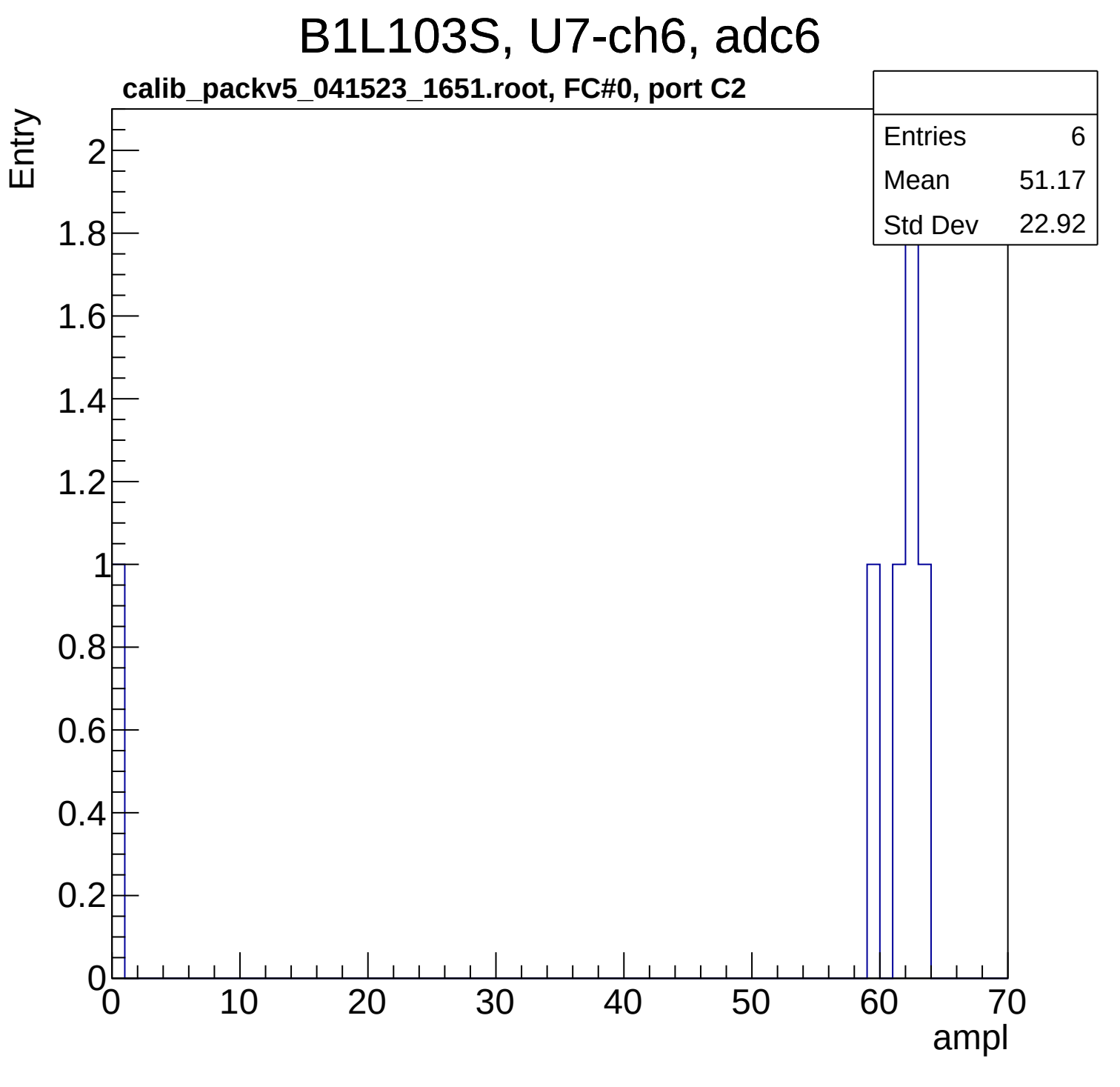
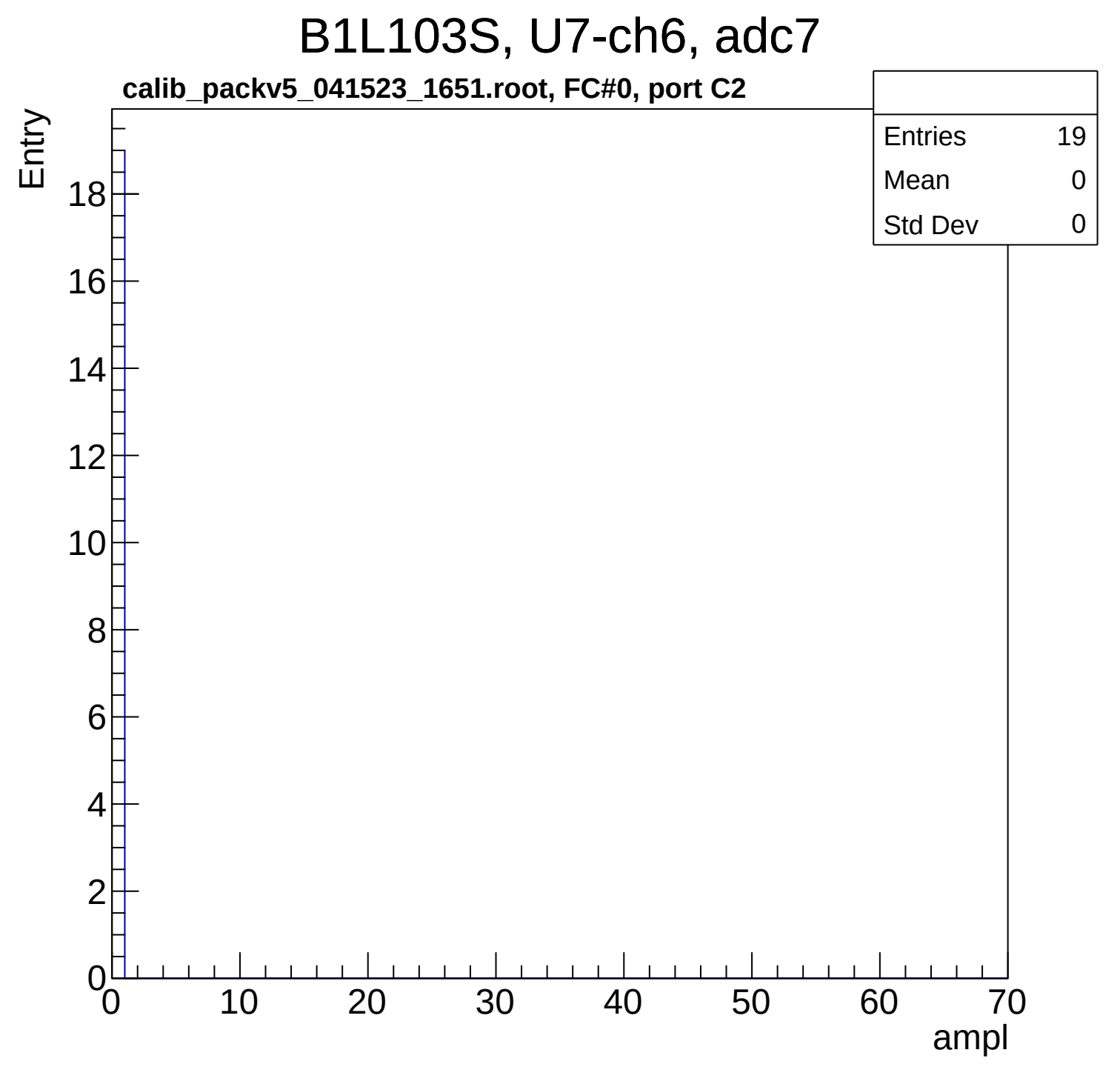
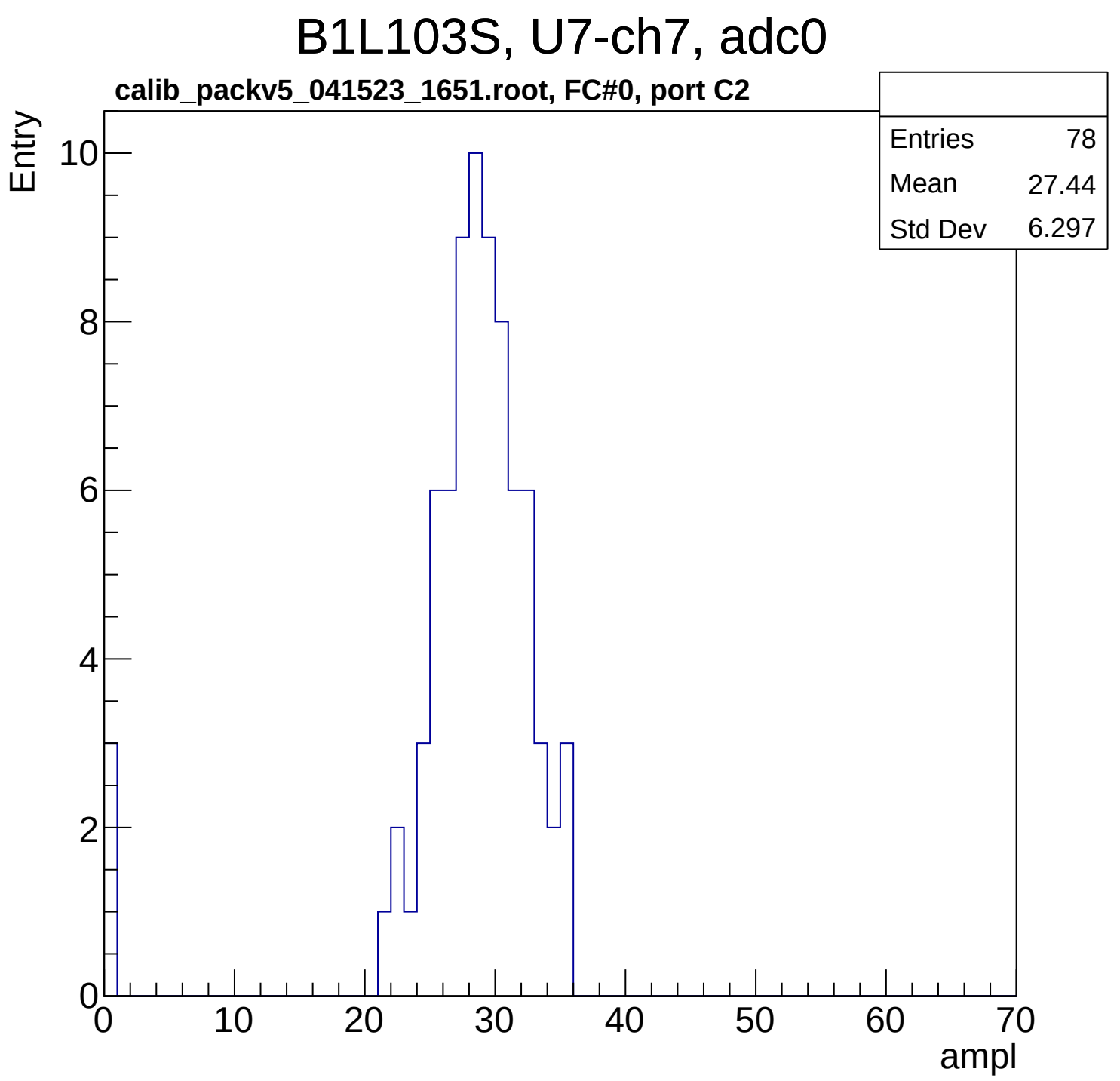

B1L103S, U7-ch6, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 51.17
Std Dev 22.92
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U7-ch6, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch7, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 27.44
Std Dev 6.297
Entry
ampl
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4
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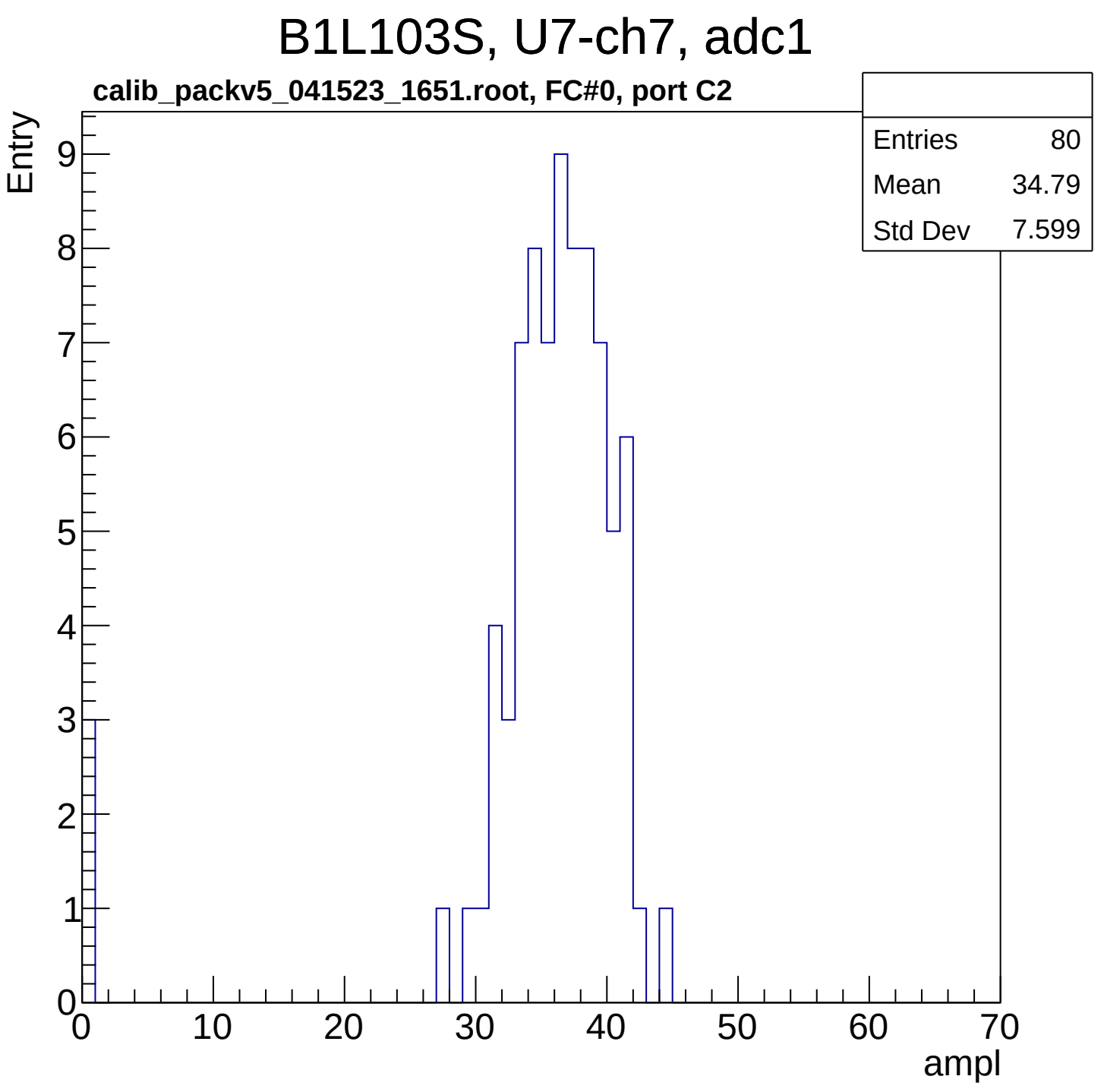
8
10
0
10
20
30
40
50
60
70


B1L103S, U7-ch7, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 34.79
Std Dev 7.599
Entry
ampl
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2
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4
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6
7
8
9
0
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40
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60
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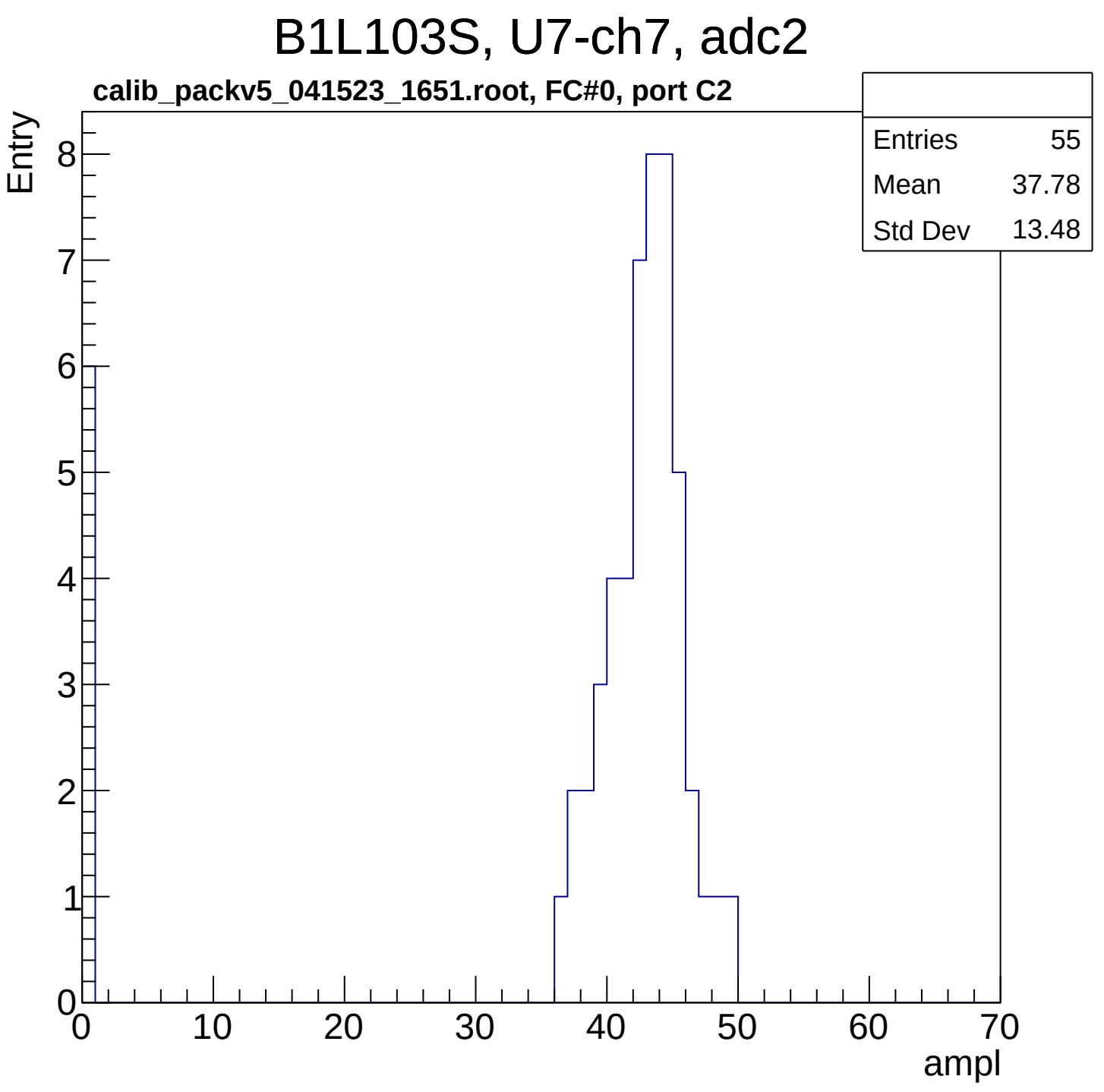
B1L103S, U7-ch7, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 37.78
Std Dev 13.48
Entry
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5
6
7
8
0
10
20
30
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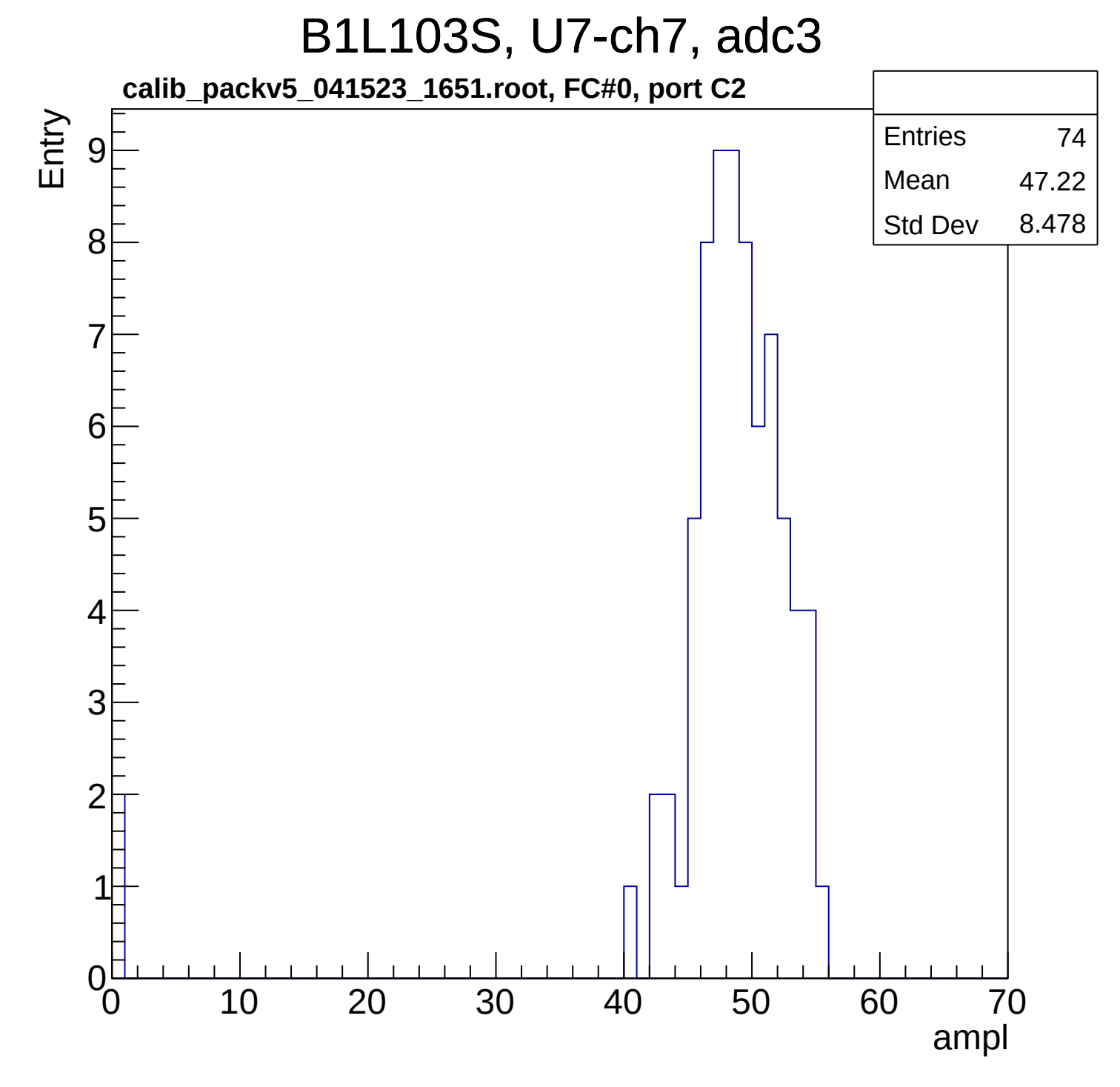
50
60
70
ampl


B1L103S, U7-ch7, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 47.22
Std Dev 8.478
Entry
ampl
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6
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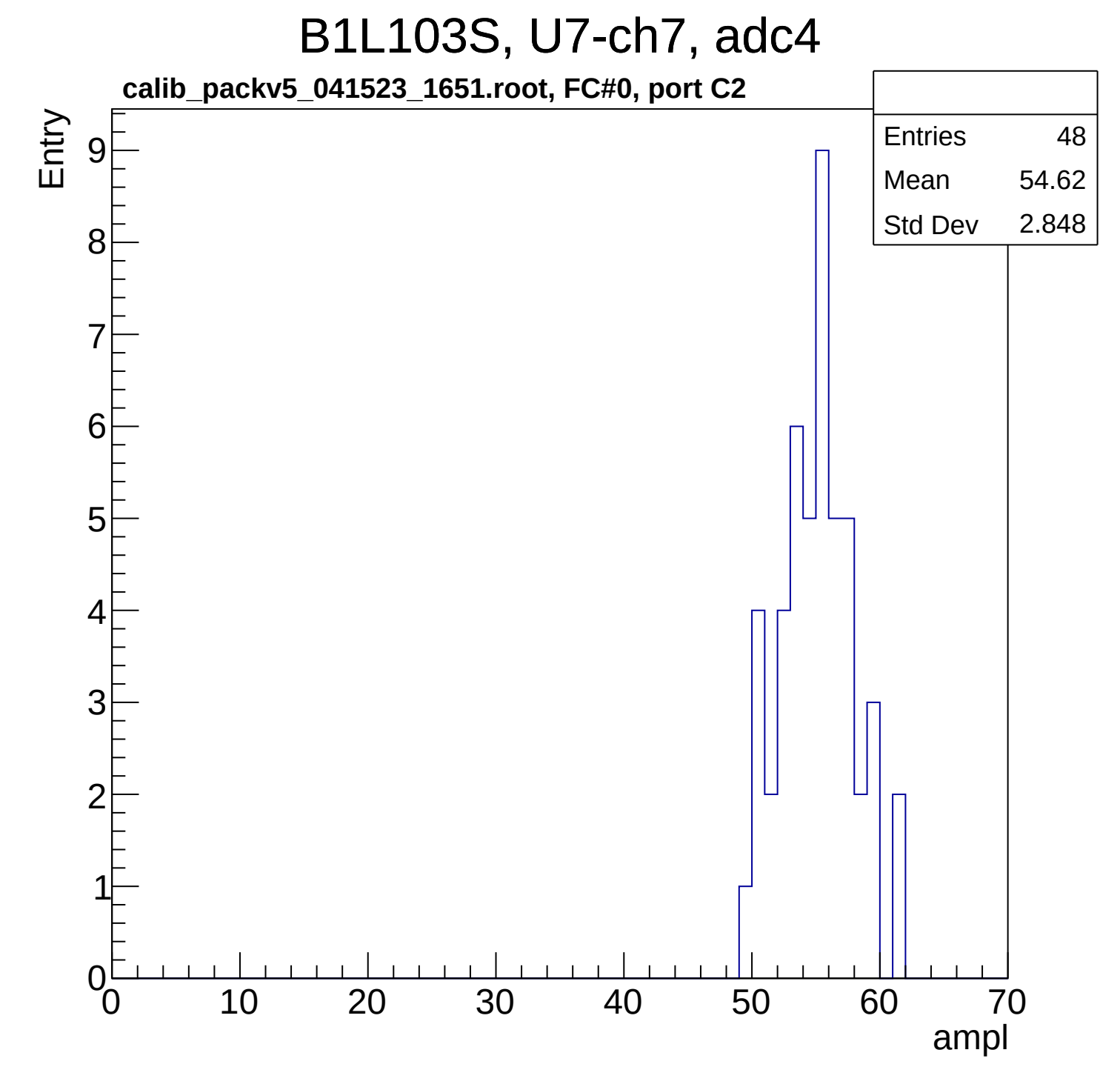
B1L103S, U7-ch7, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 54.62
Std Dev 2.848
Entry
ampl
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3
4
5
6
7
8
9
0
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40
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60
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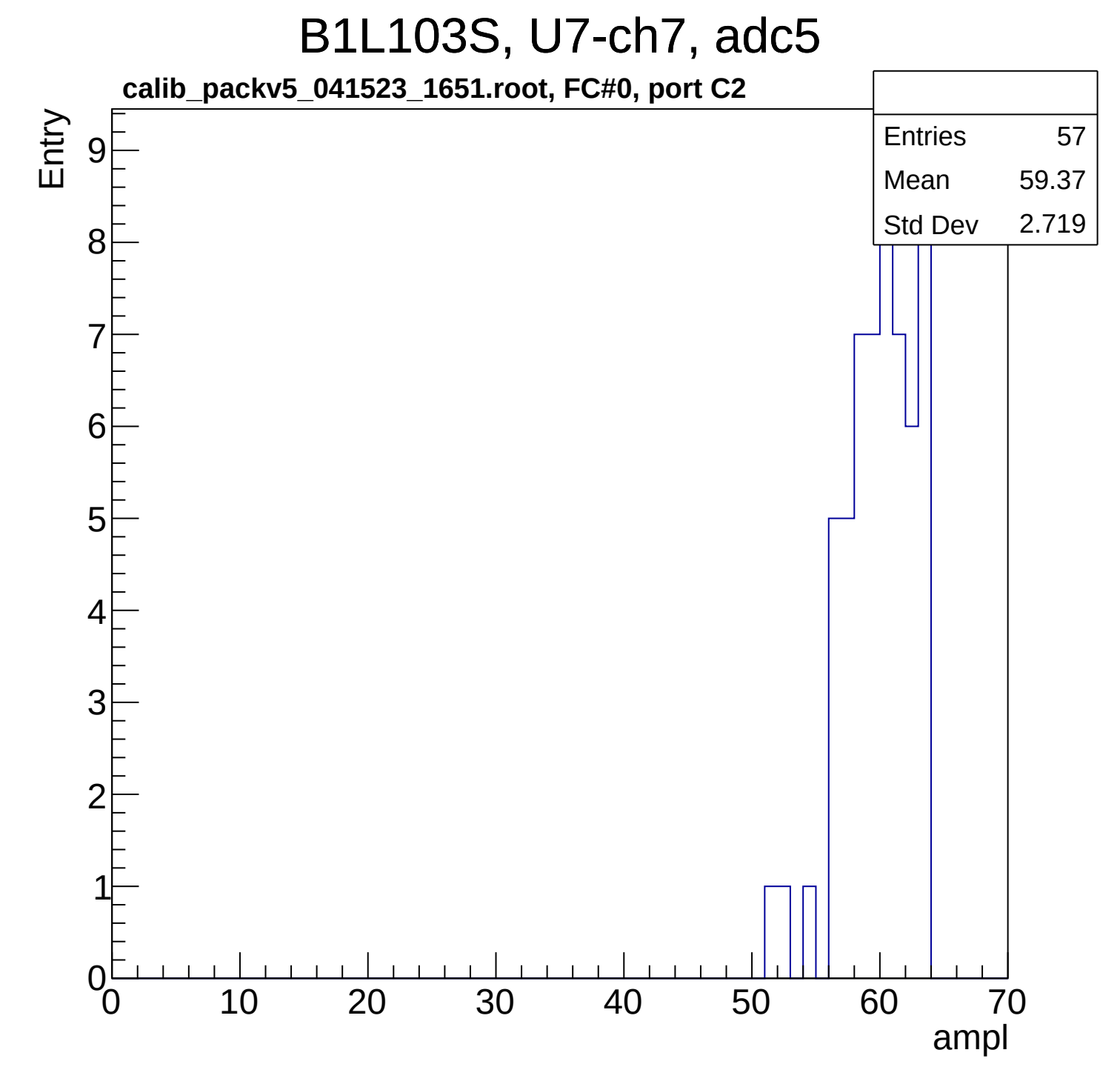
B1L103S, U7-ch7, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 59.37
Std Dev 2.719
Entry
ampl
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4
5
6
7
8
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0
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40
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60
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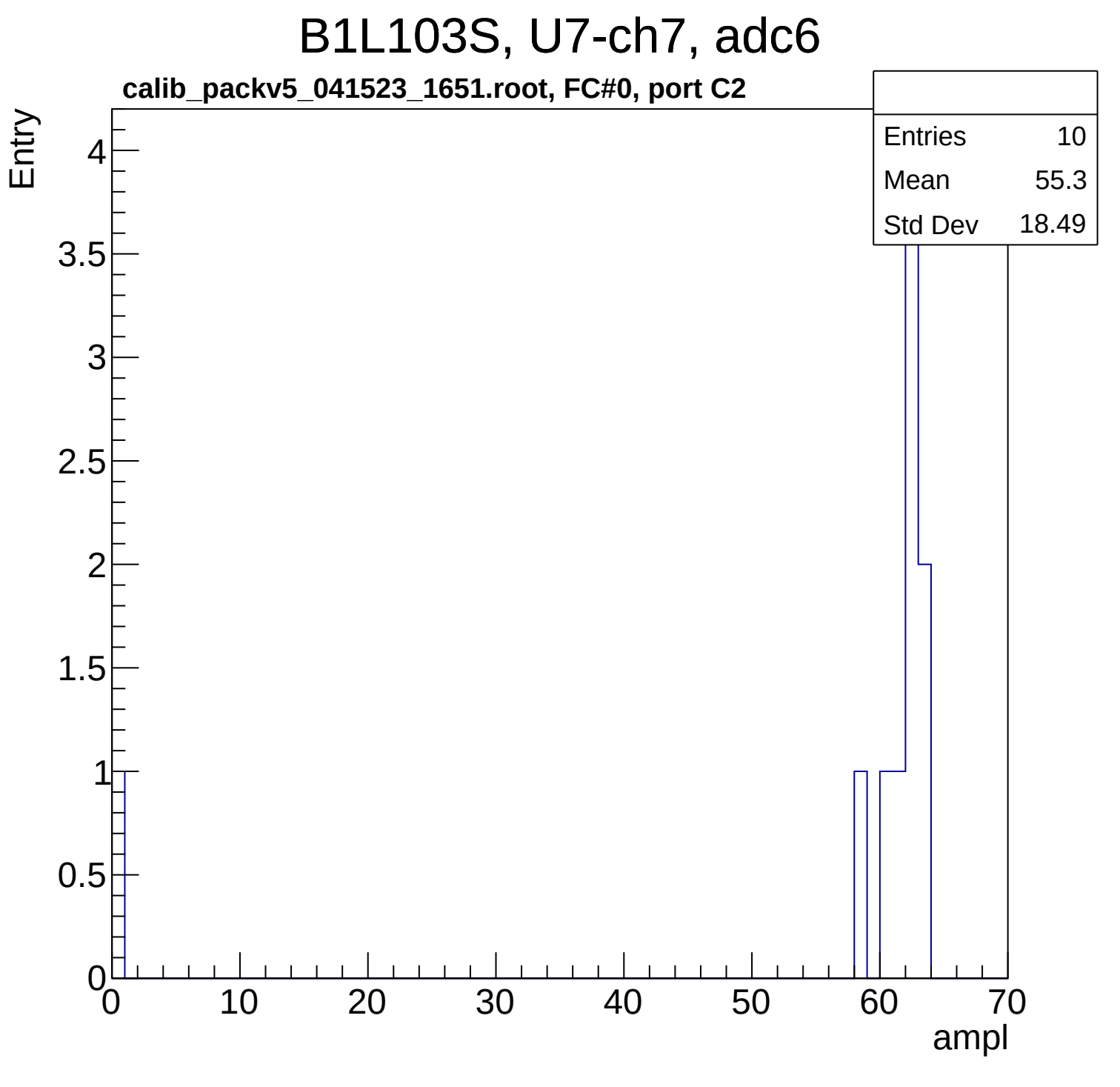
B1L103S, U7-ch7, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 55.3
Std Dev 18.49
Entry
ampl
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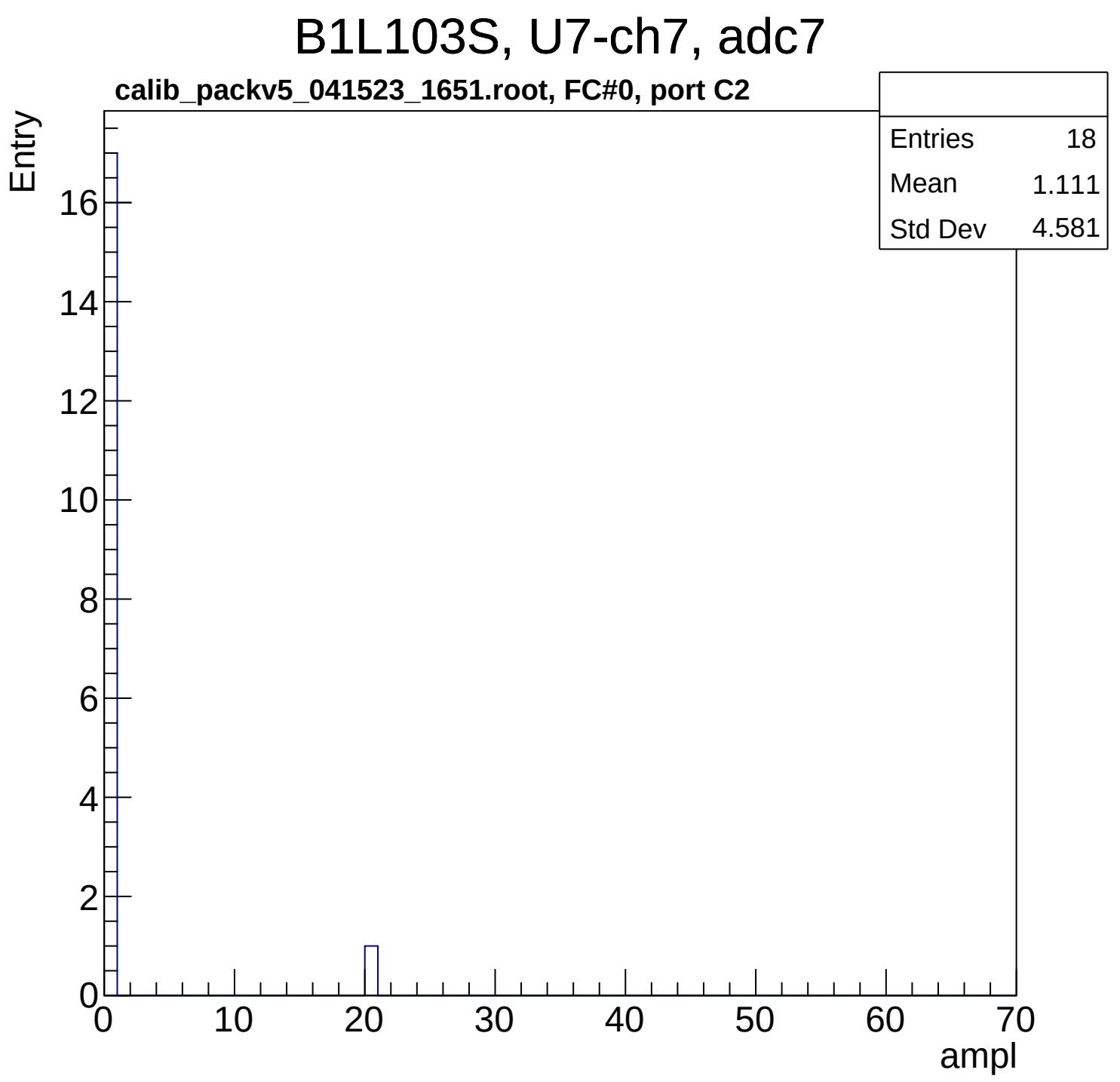
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U7-ch7, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 1.111
Std Dev 4.581
Entry
0
2
4
6
8
10
12
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16
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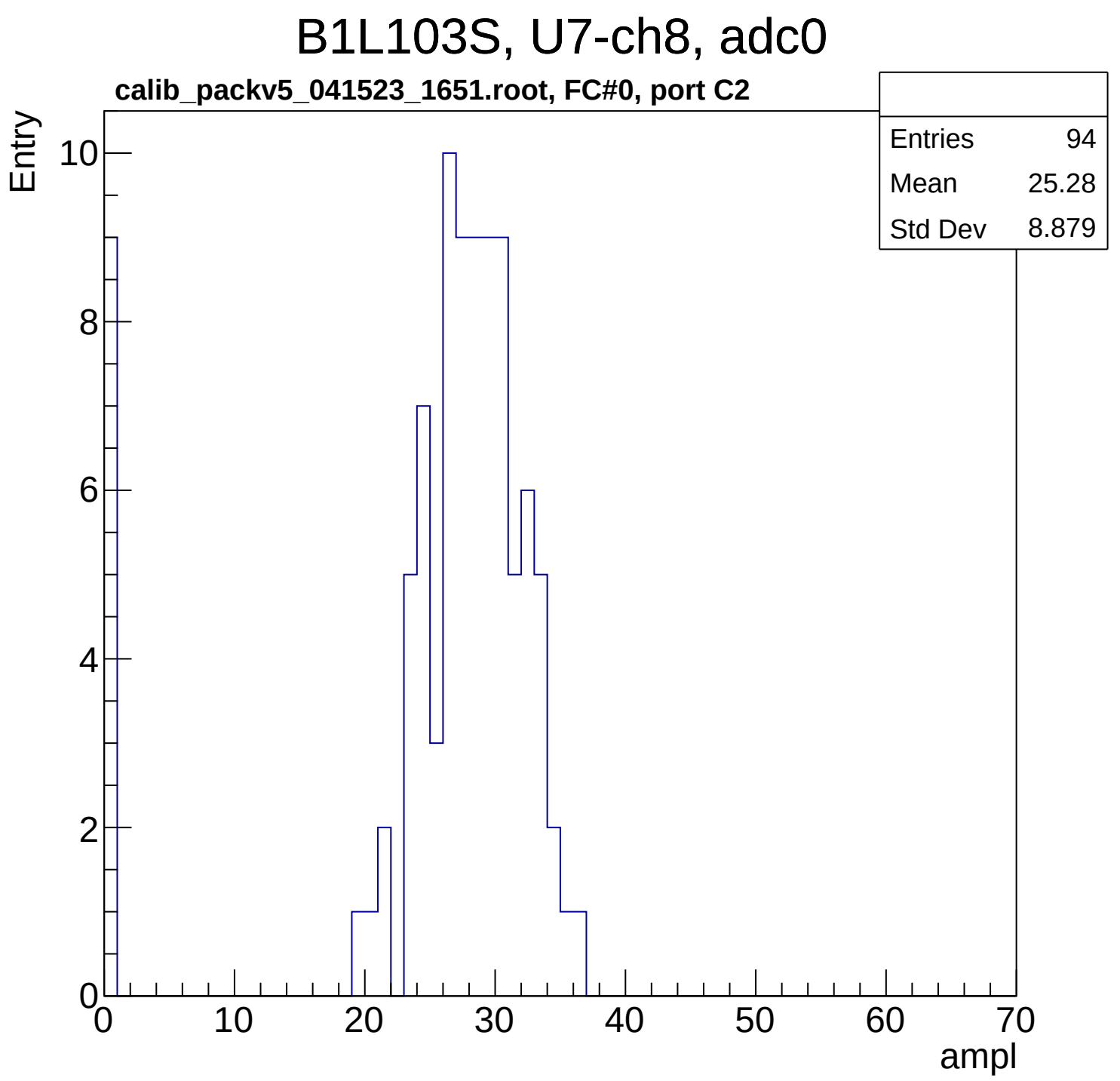
50
60
70
ampl


B1L103S, U7-ch8, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 94
Mean 25.28
Std Dev 8.879
Entry
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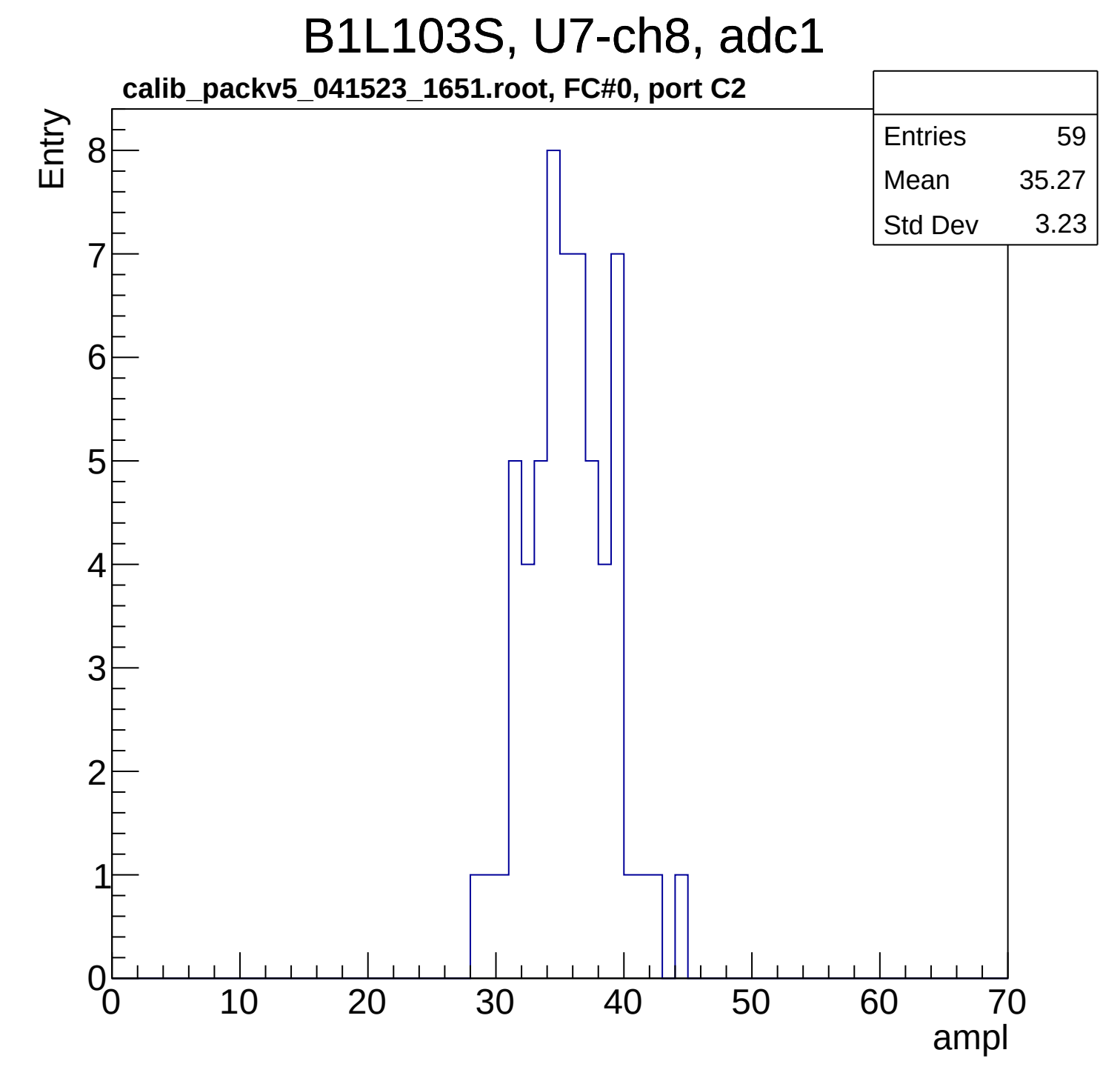
ampl


B1L103S, U7-ch8, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 35.27
Std Dev 3.23
Entry
ampl
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2
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4
5
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40
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60
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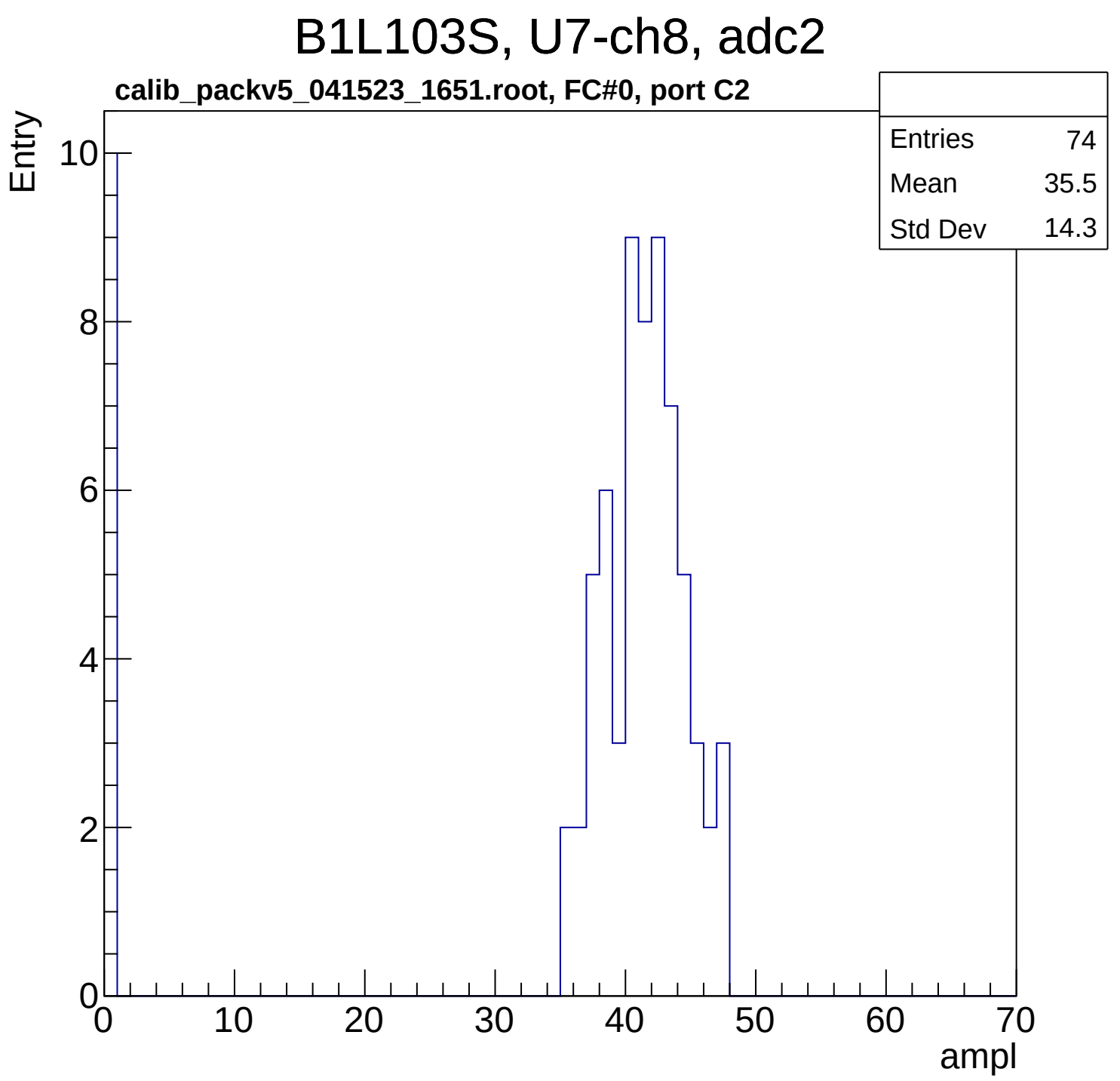
B1L103S, U7-ch8, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 35.5
Std Dev 14.3
Entry
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4
6
8
10
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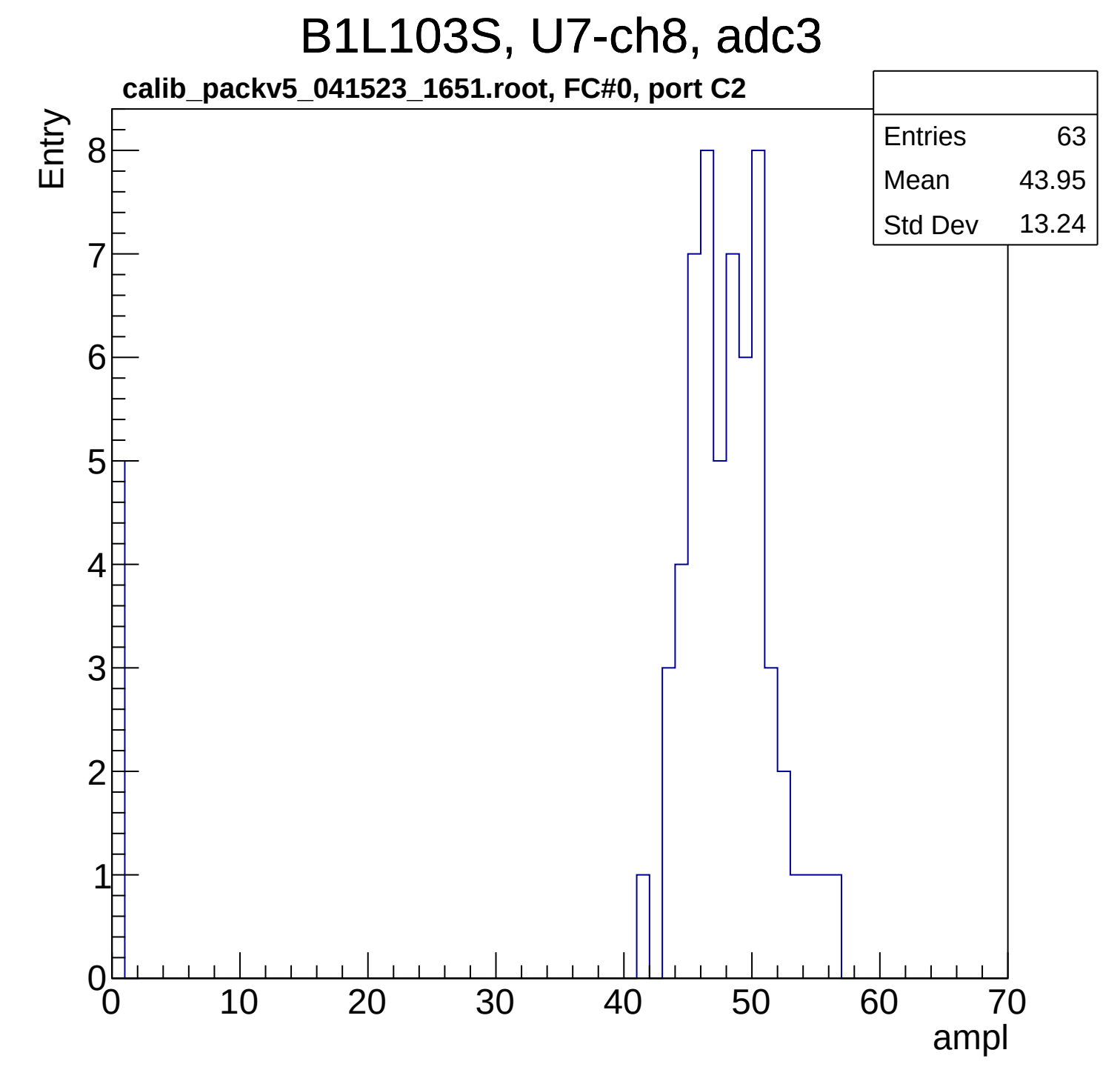
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch8, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 43.95
Std Dev 13.24
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
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40
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60
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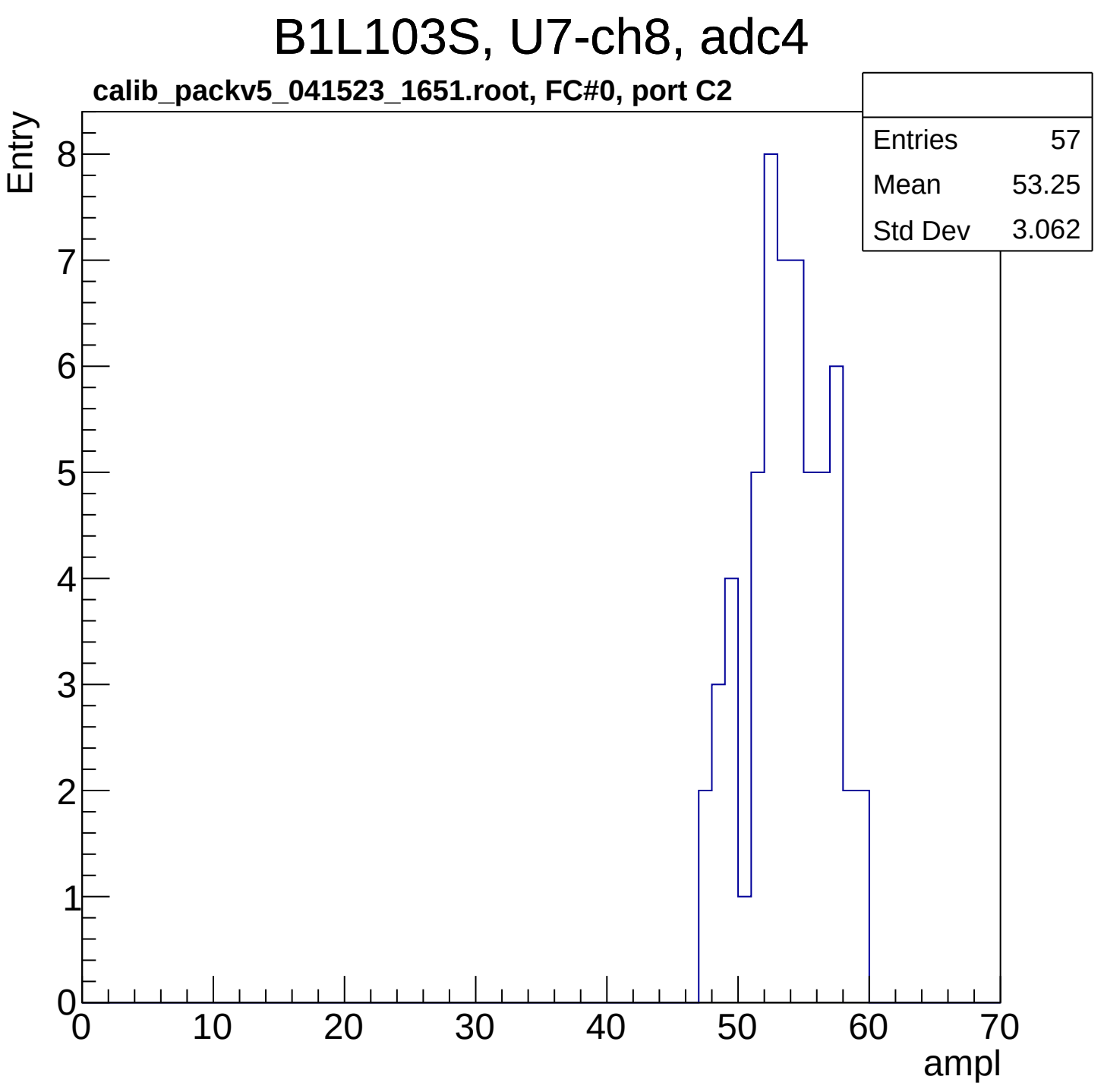
B1L103S, U7-ch8, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 53.25
Std Dev 3.062
Entry
ampl
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2
3
4
5
6
7
8
0
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40
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60
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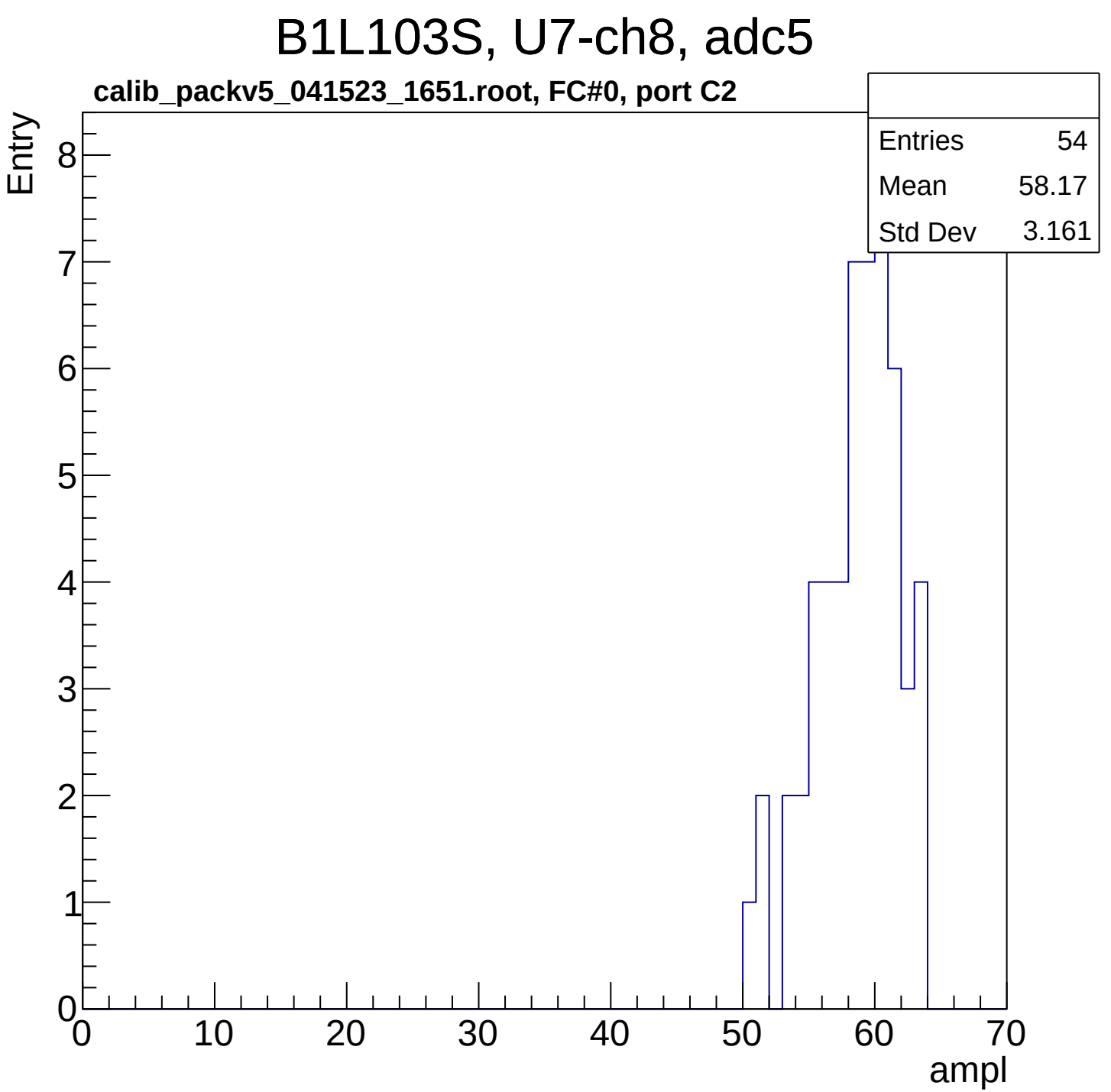
B1L103S, U7-ch8, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 58.17
Std Dev 3.161
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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40
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60
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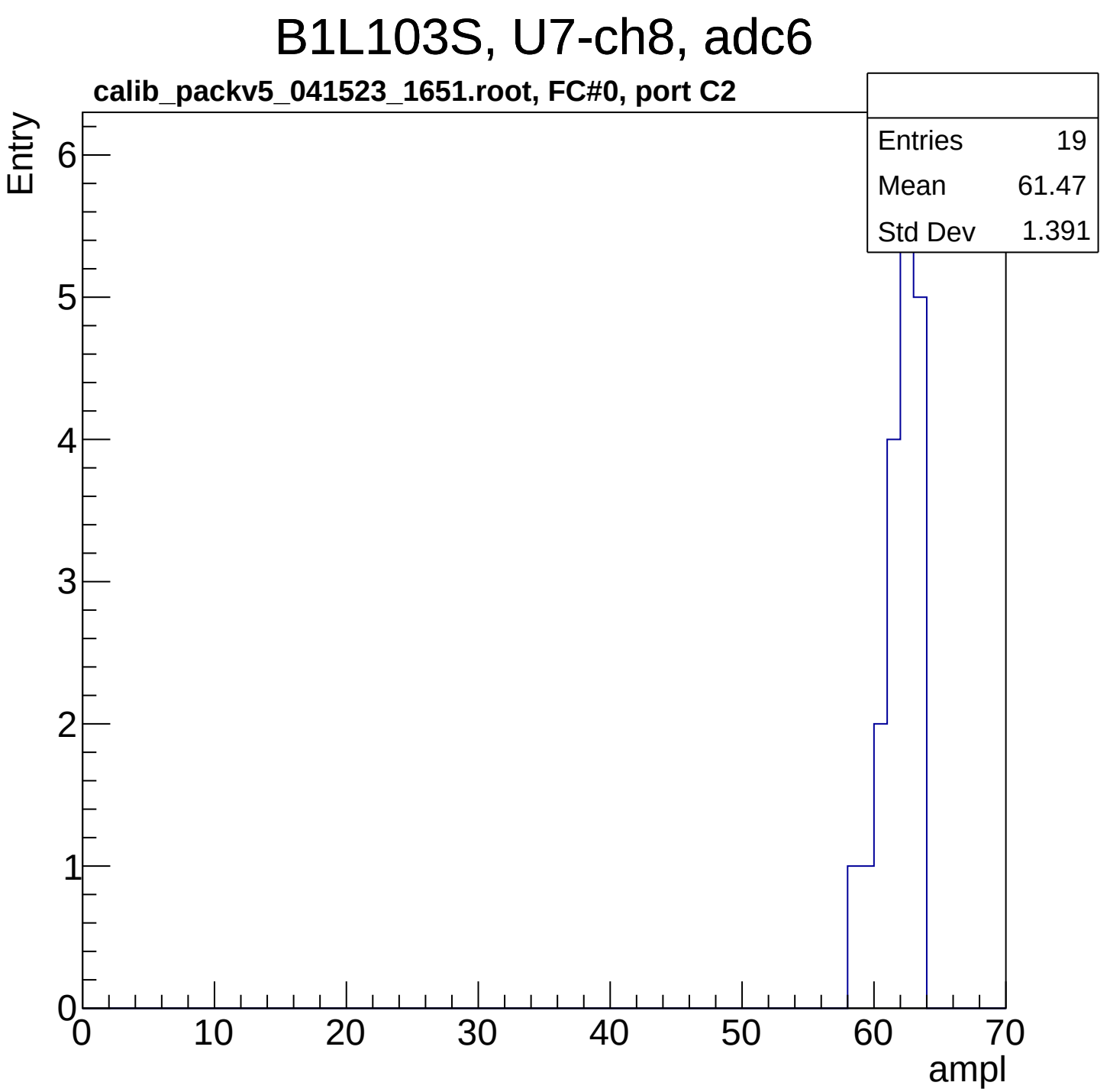
B1L103S, U7-ch8, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 61.47
Std Dev 1.391
Entry
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2
3
4
5
6
0
10
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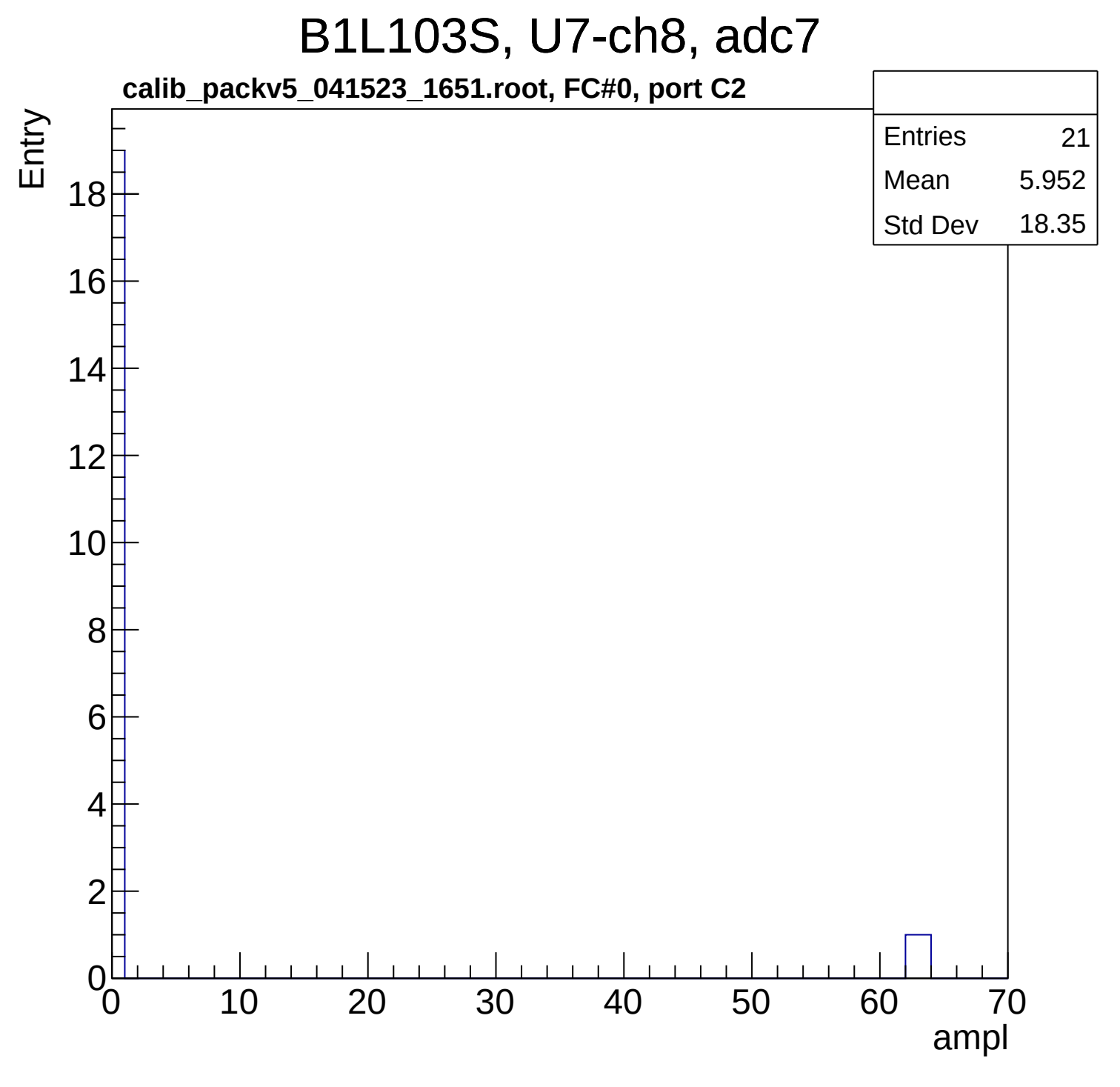
50
60
70
ampl


B1L103S, U7-ch8, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 5.952
Std Dev 18.35
Entry
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6
8
10
12
14
16
18
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10
20
30
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50
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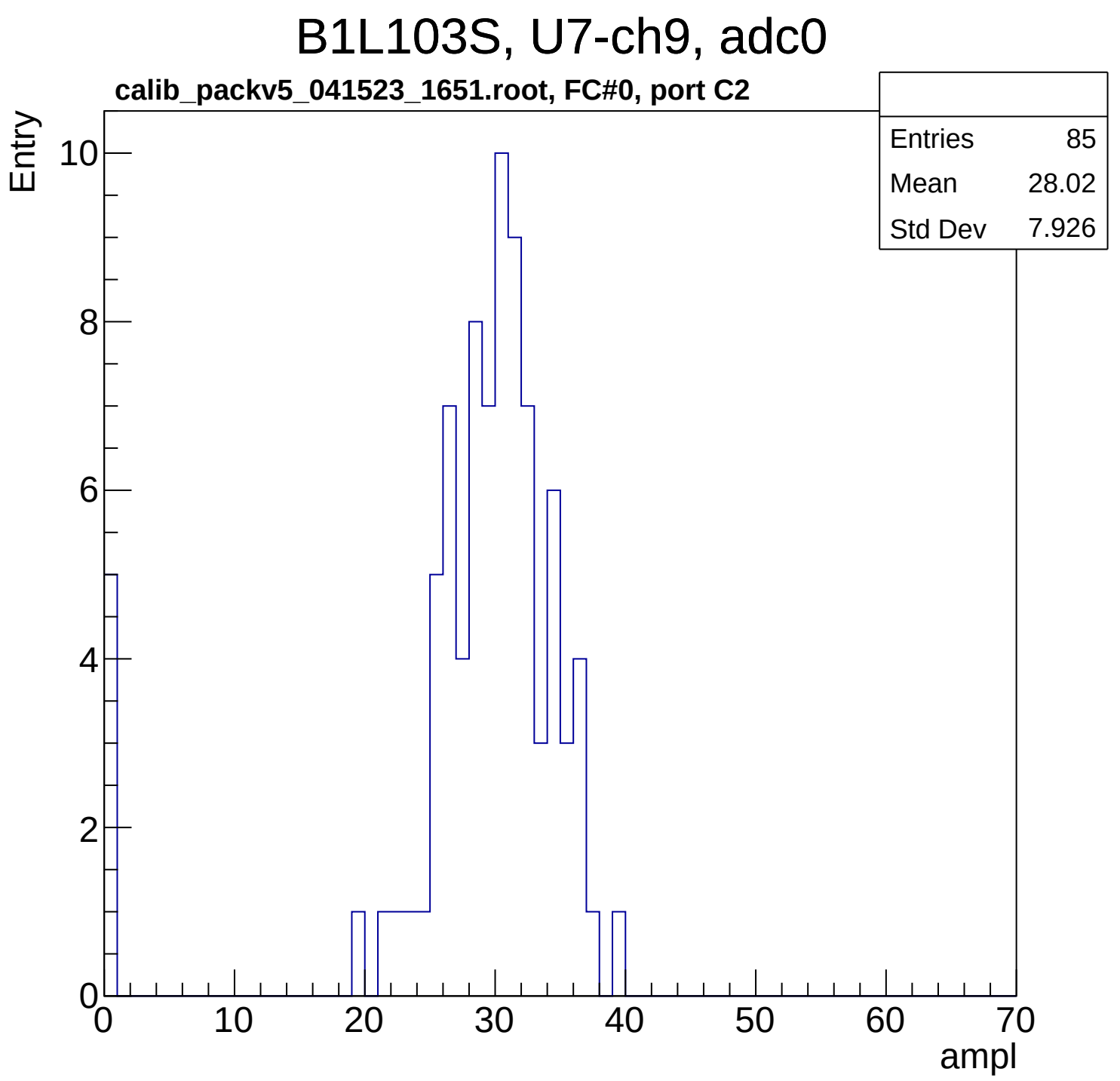
70
ampl


B1L103S, U7-ch9, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 28.02
Std Dev 7.926
Entry
ampl
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2
4
6
8
10
0
10
20
30
40
50
60
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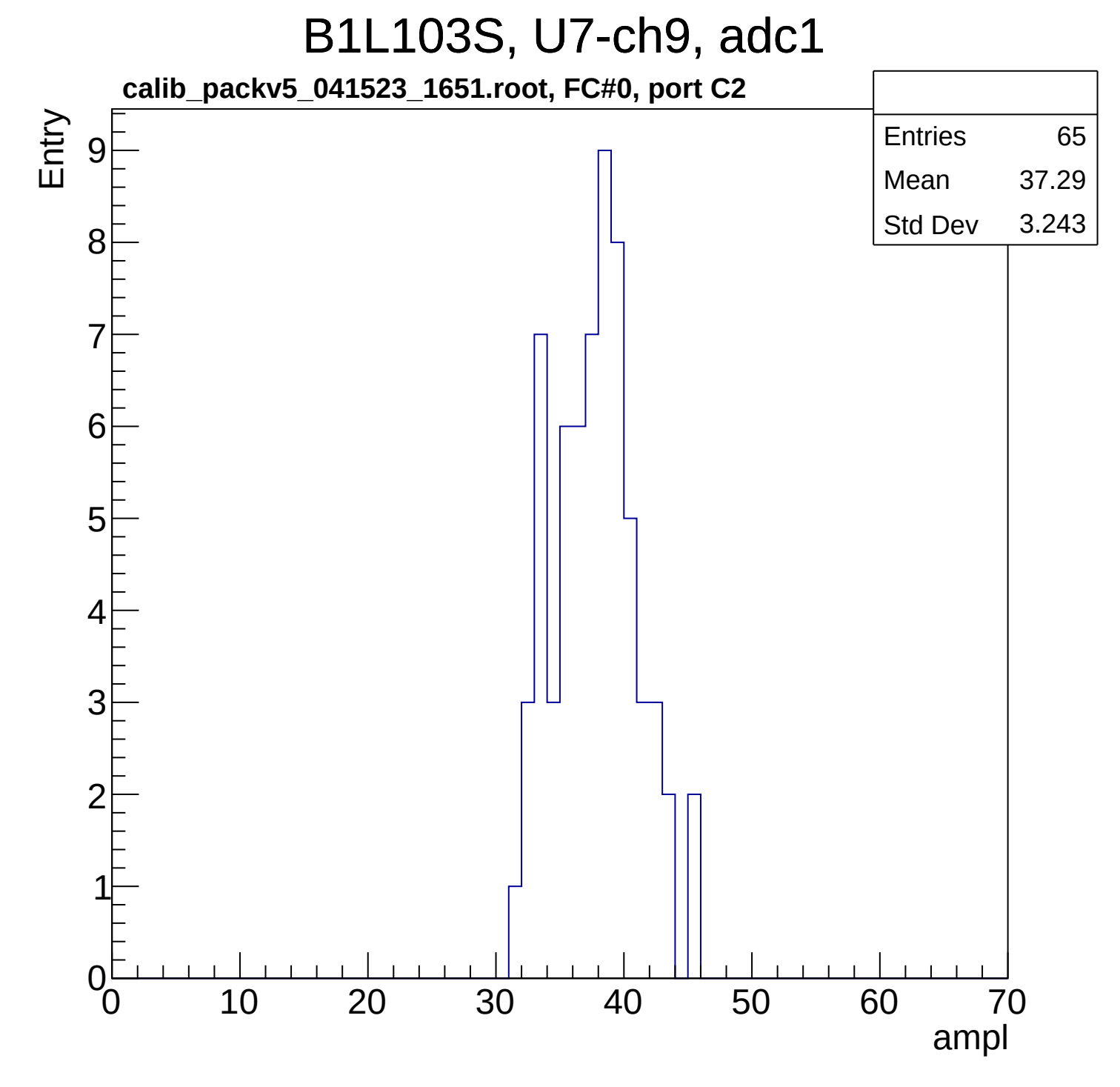
B1L103S, U7-ch9, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 37.29
Std Dev 3.243
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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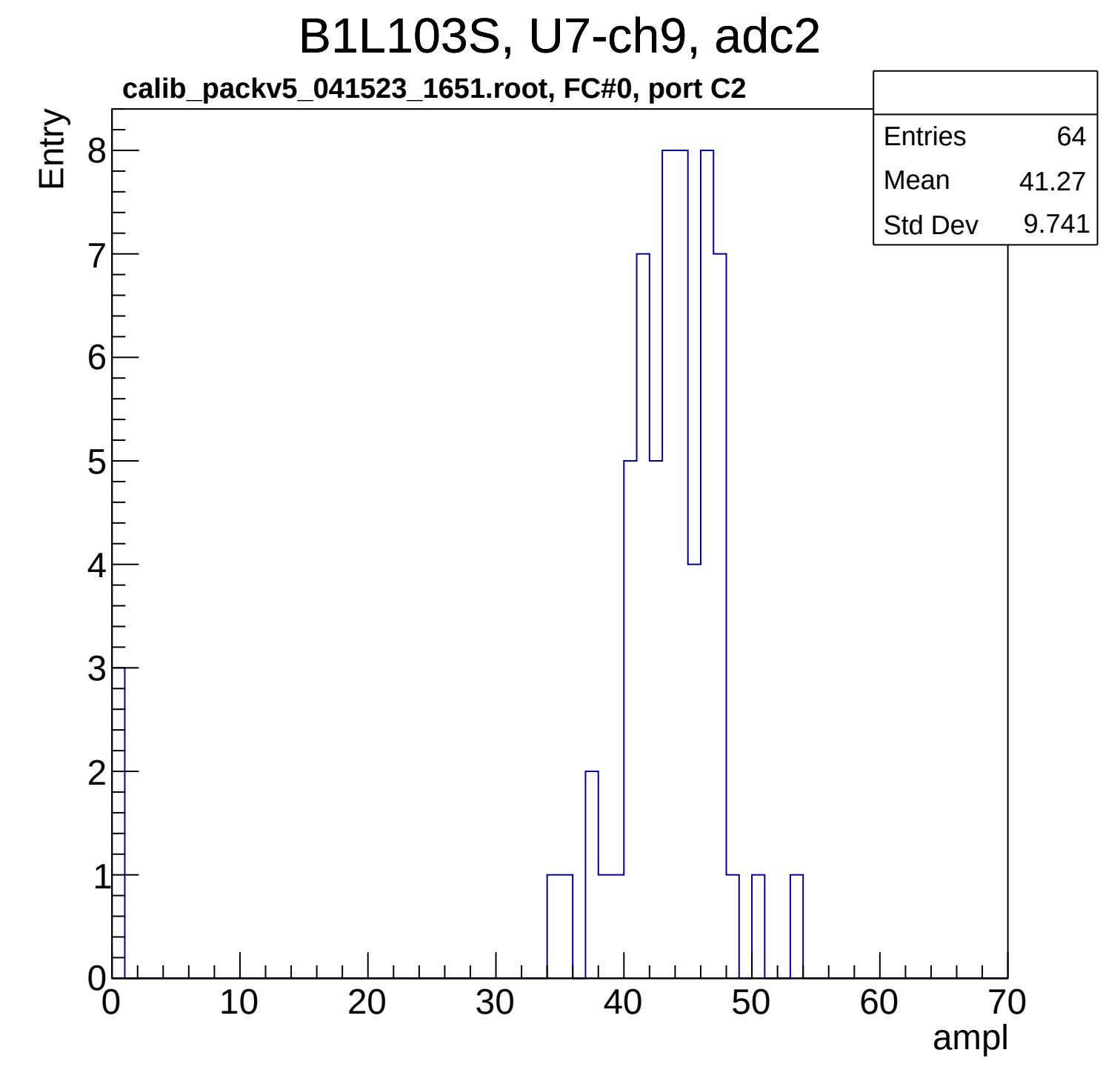
B1L103S, U7-ch9, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 41.27
Std Dev 9.741
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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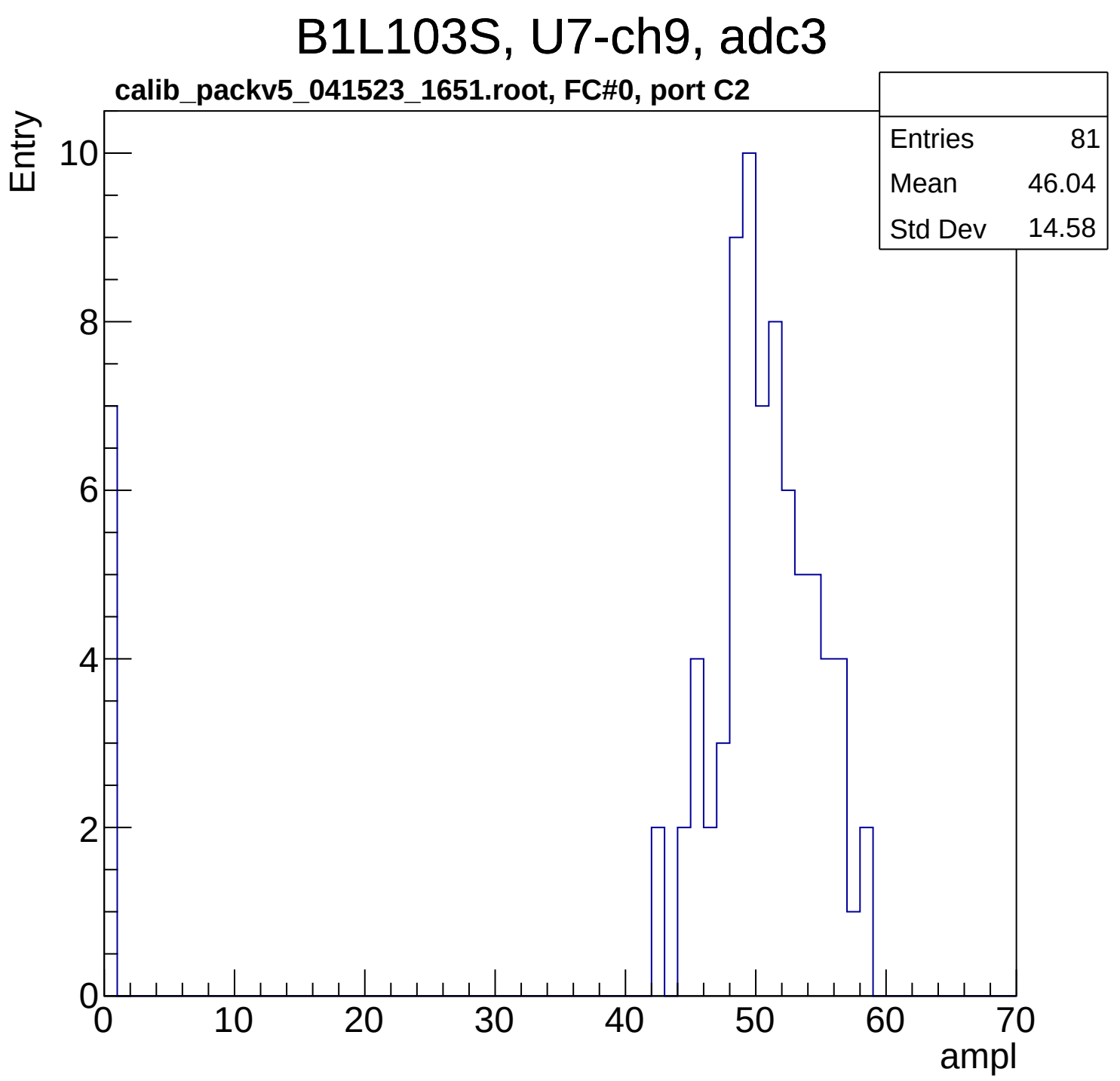
B1L103S, U7-ch9, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 46.04
Std Dev 14.58
Entry
ampl
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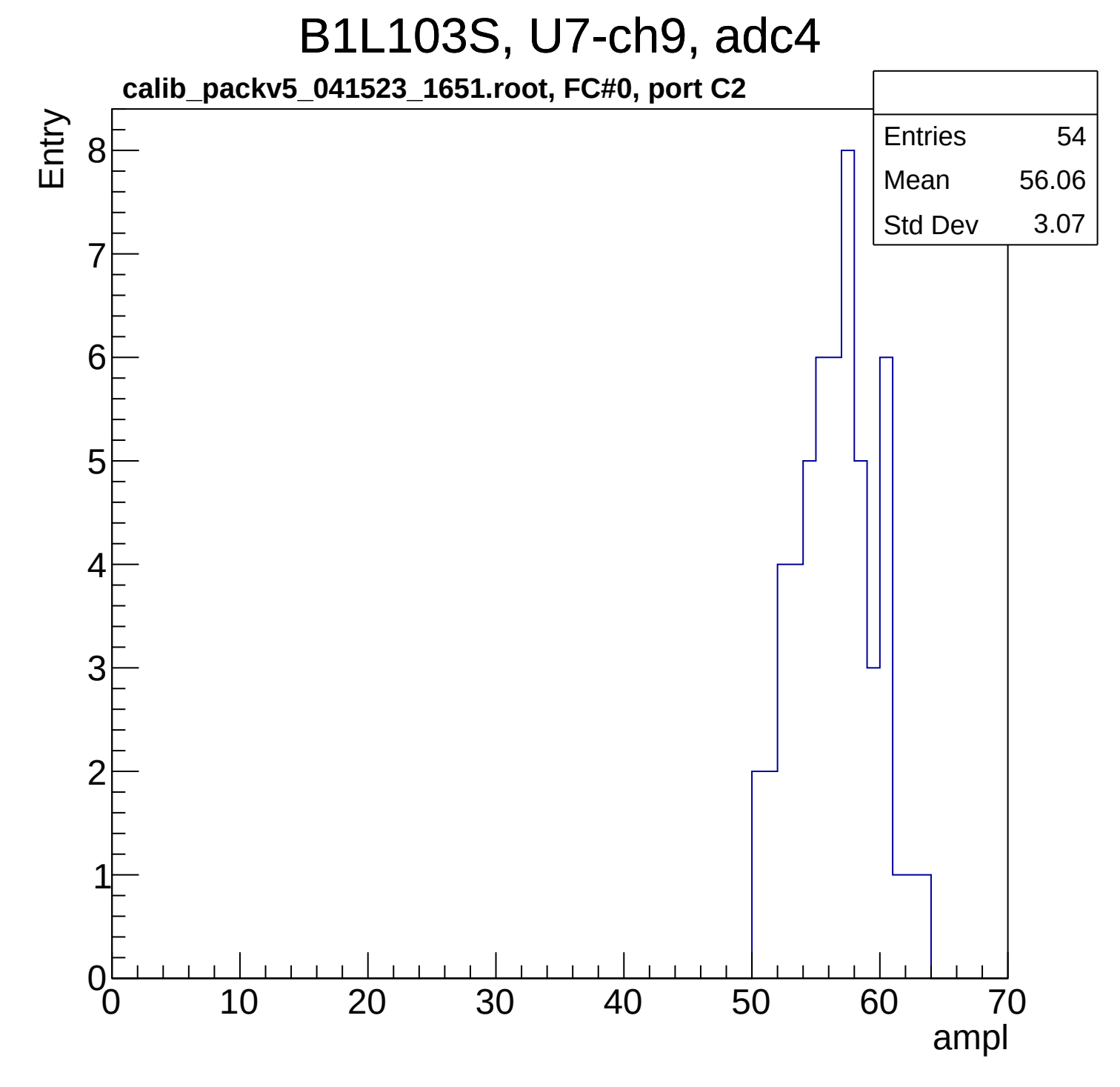
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U7-ch9, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 56.06
Std Dev 3.07
Entry
ampl
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2
3
4
5
6
7
8
0
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60
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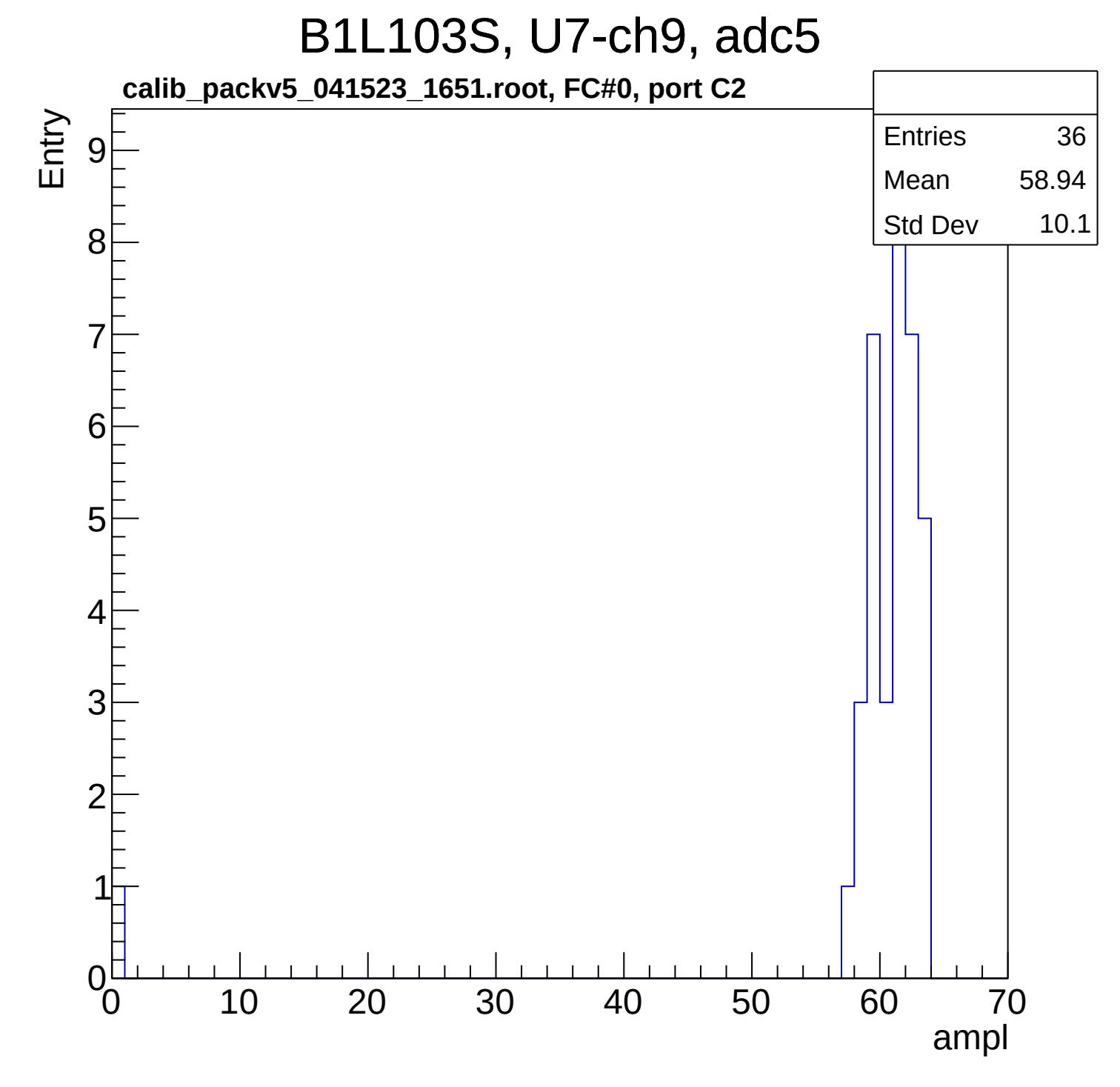
B1L103S, U7-ch9, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 36
Mean 58.94
Std Dev 10.1
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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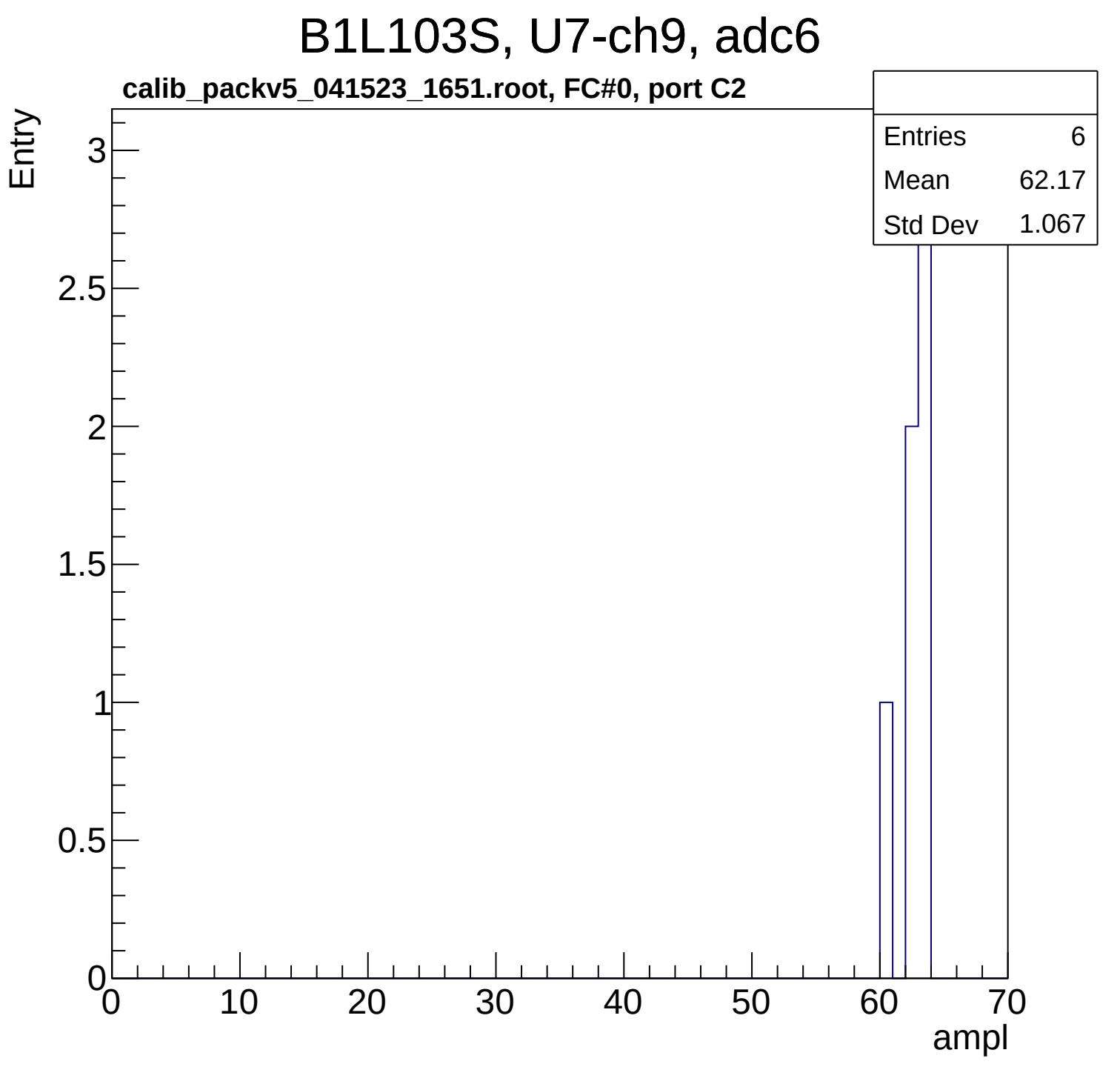
40
50
60
70


B1L103S, U7-ch9, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 62.17
Std Dev 1.067
Entry
ampl
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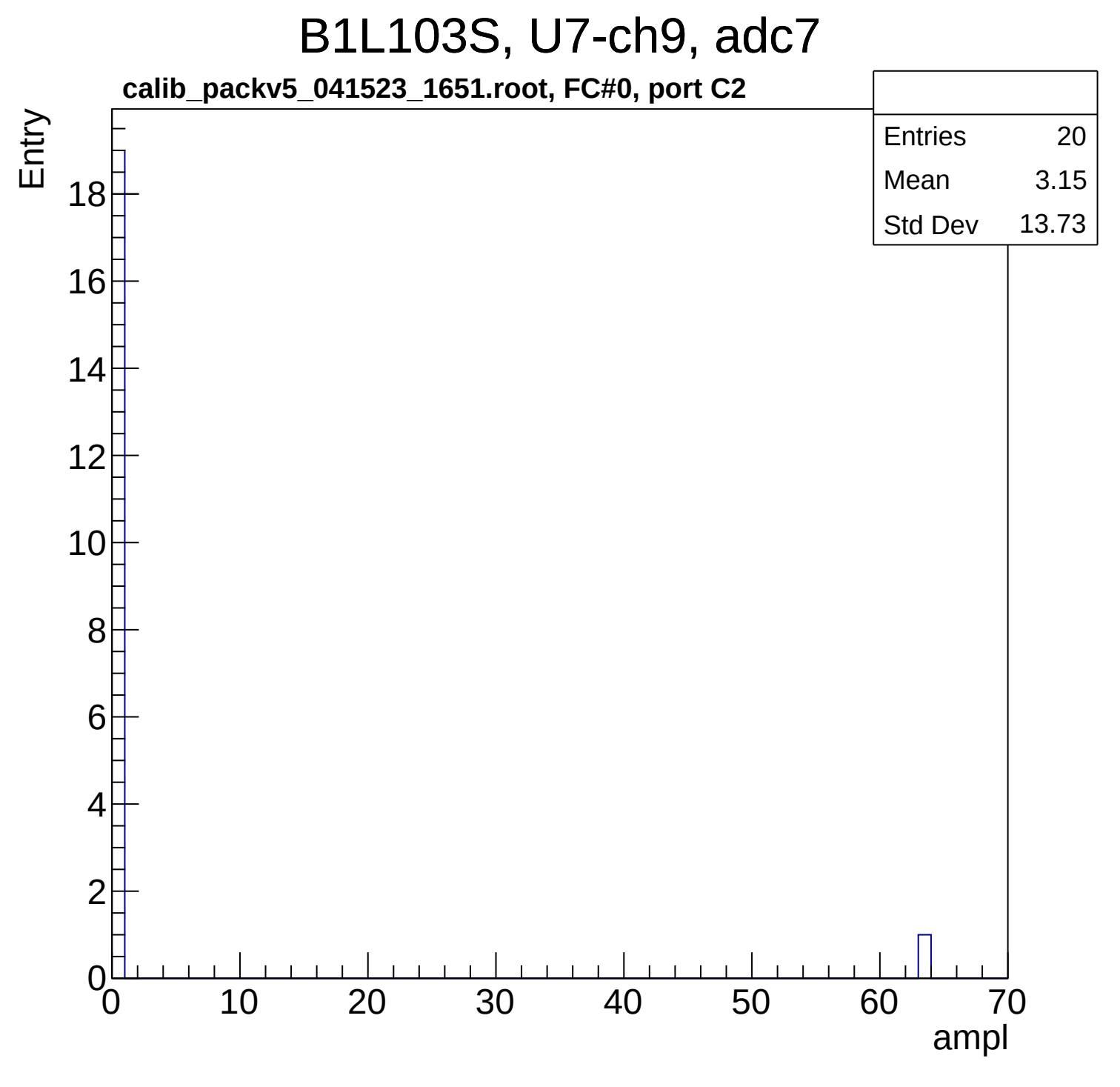
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U7-ch9, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
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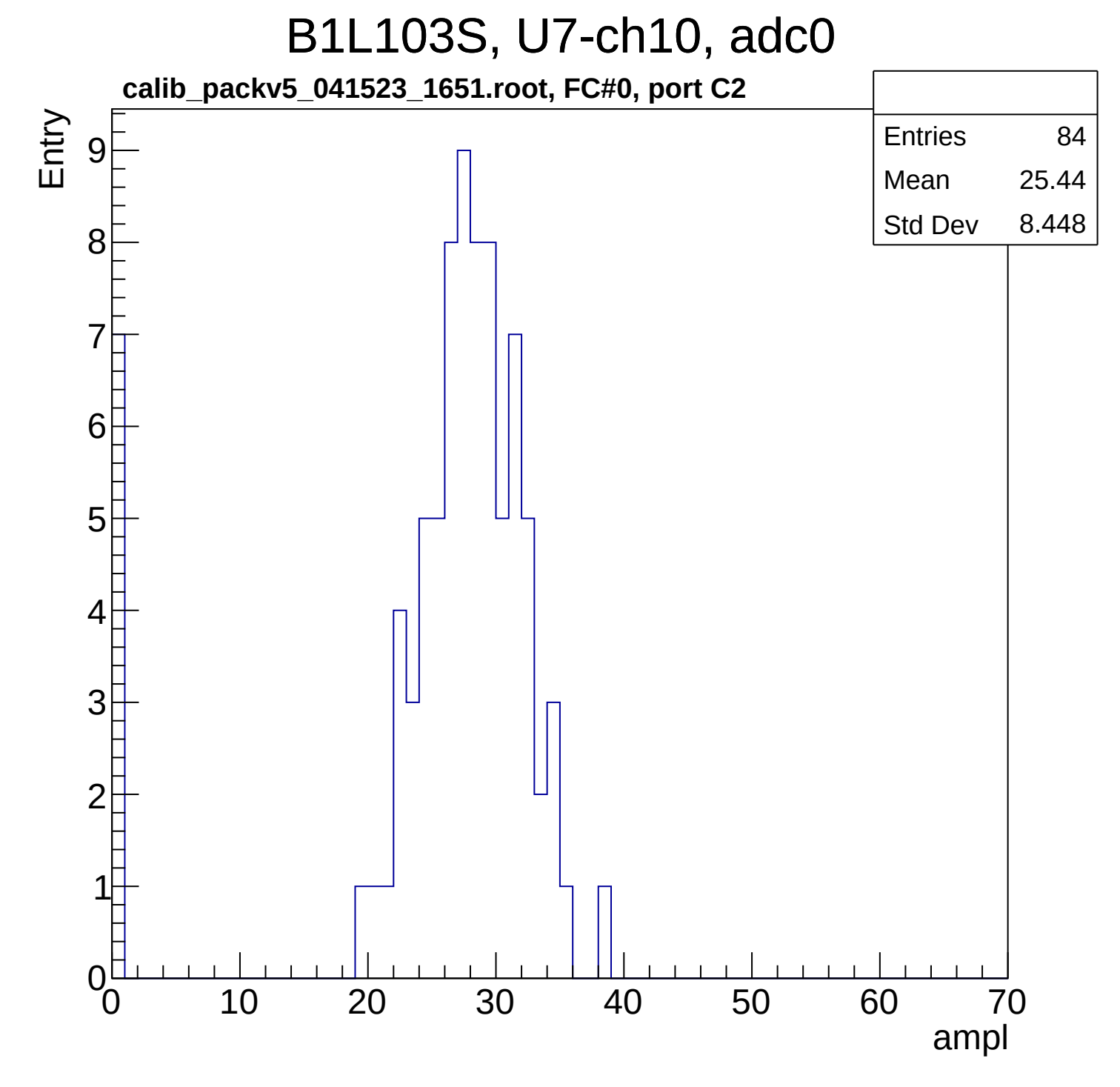
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch10, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 25.44
Std Dev 8.448
Entry
ampl
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3
4
5
6
7
8
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0
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60
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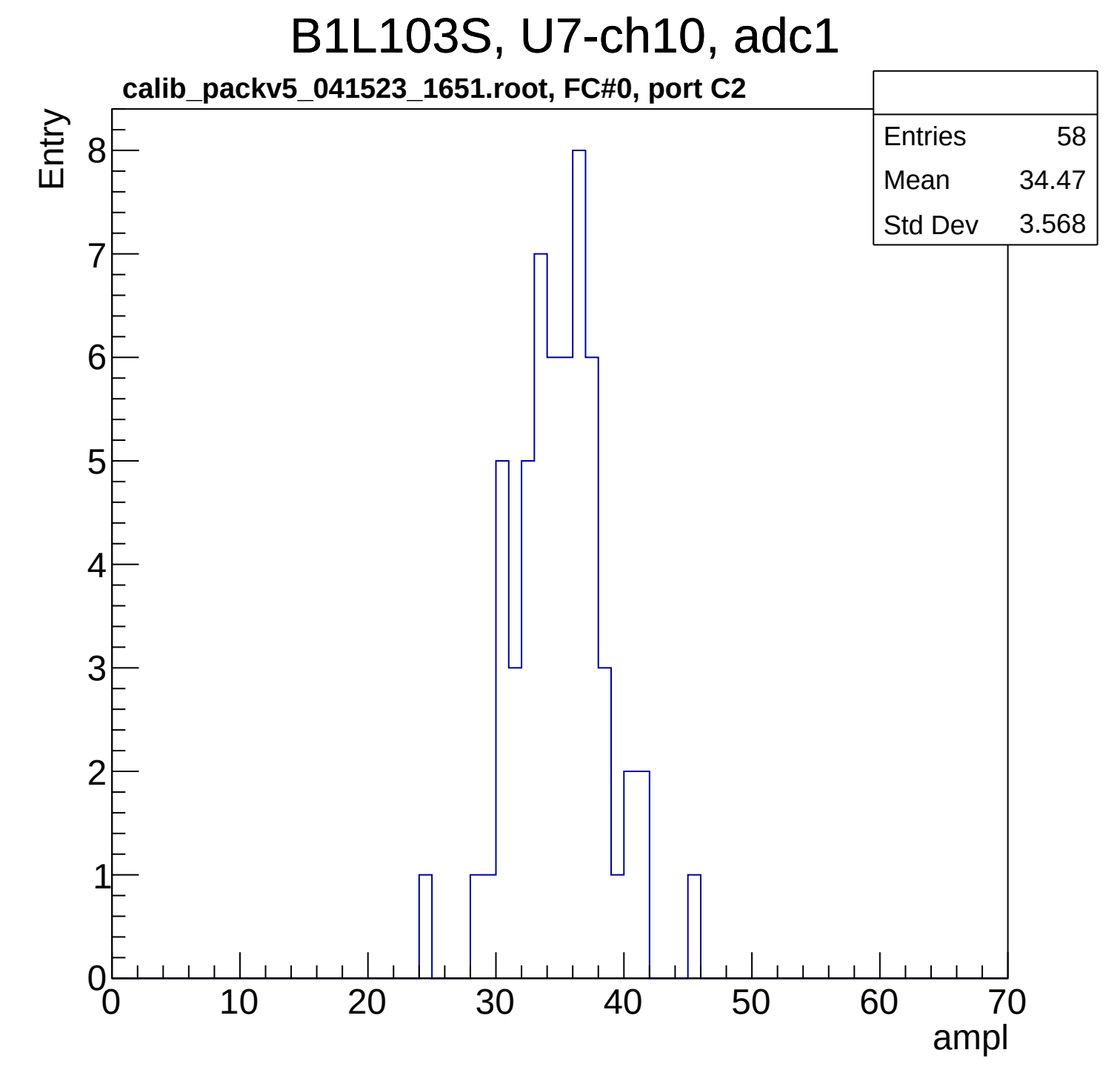
B1L103S, U7-ch10, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 34.47
Std Dev 3.568
Entry
ampl
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1
2
3
4
5
6
7
8
0
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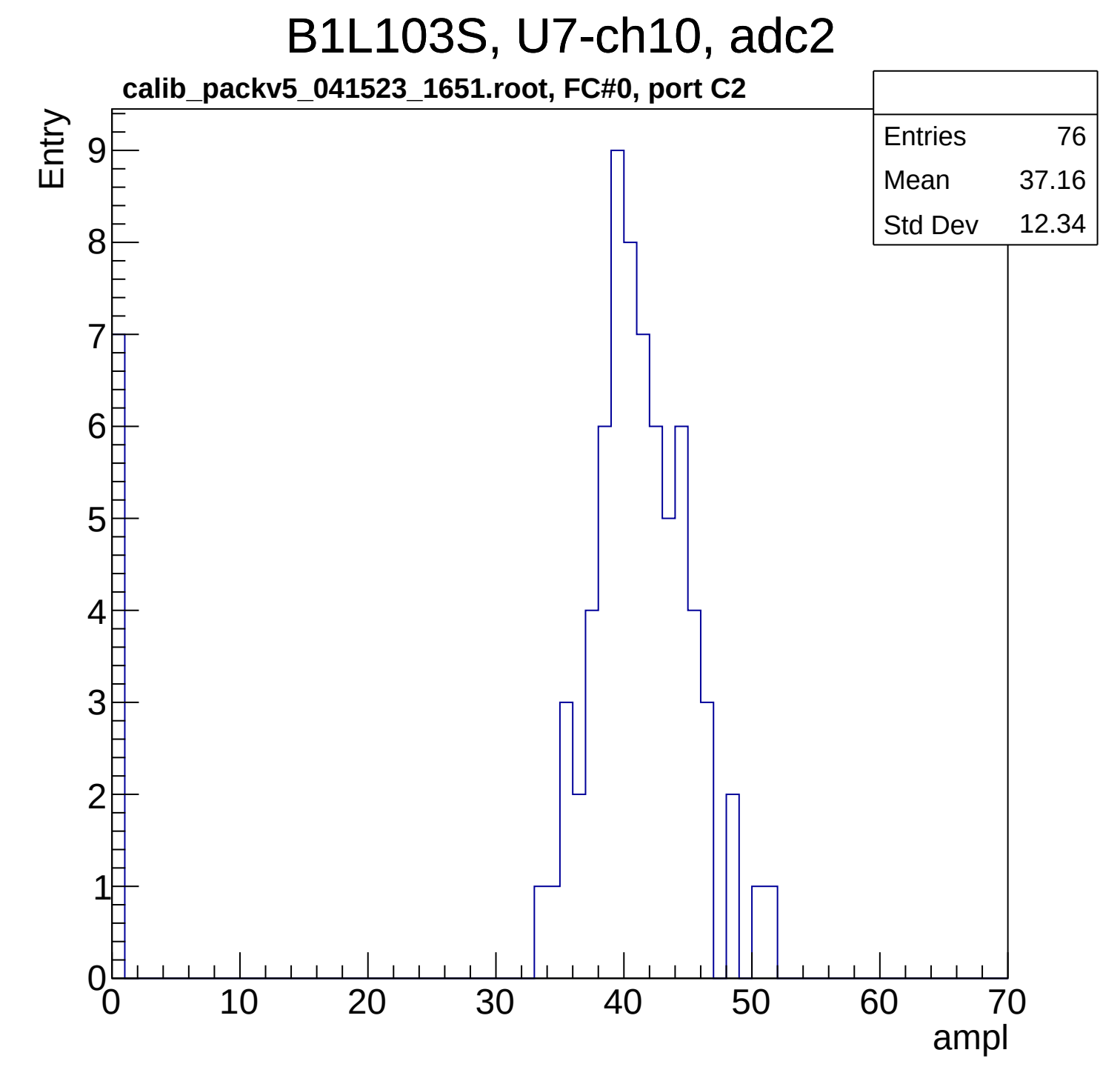
20
30
40
50
60
70


B1L103S, U7-ch10, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 37.16
Std Dev 12.34
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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40
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60
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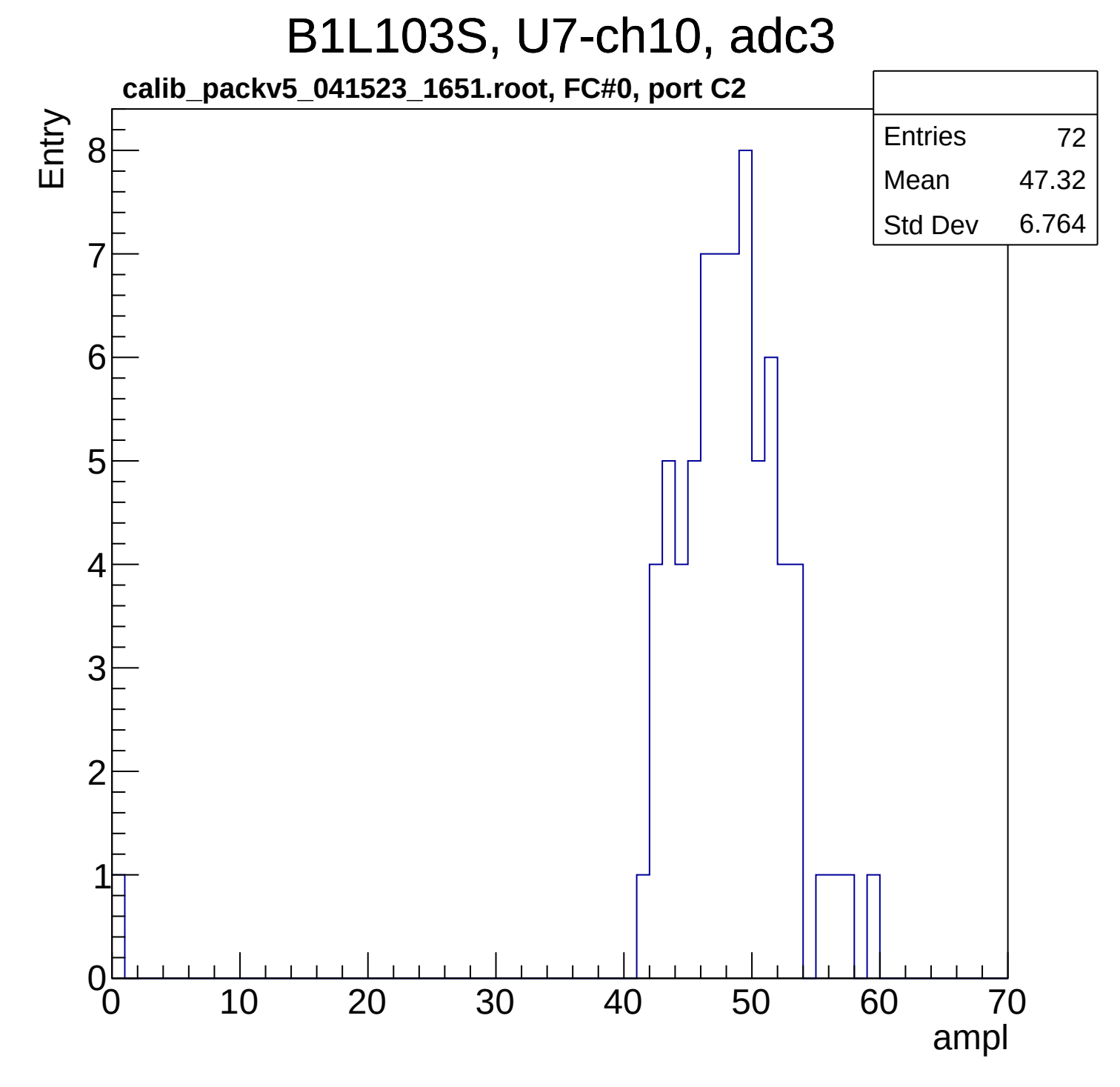
B1L103S, U7-ch10, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 47.32
Std Dev 6.764
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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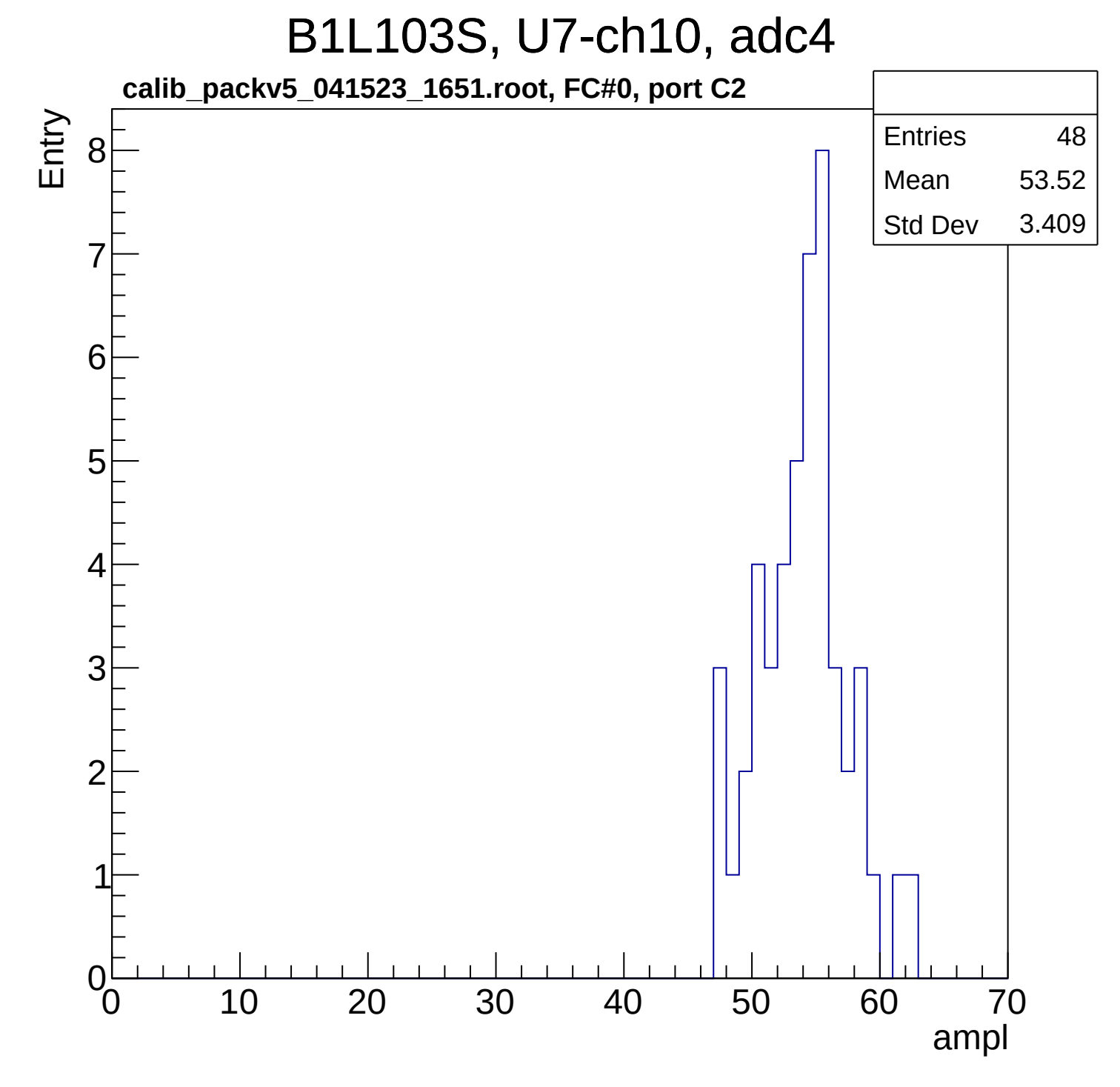
60
70


B1L103S, U7-ch10, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 53.52
Std Dev 3.409
Entry
ampl
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2
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4
5
6
7
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0
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60
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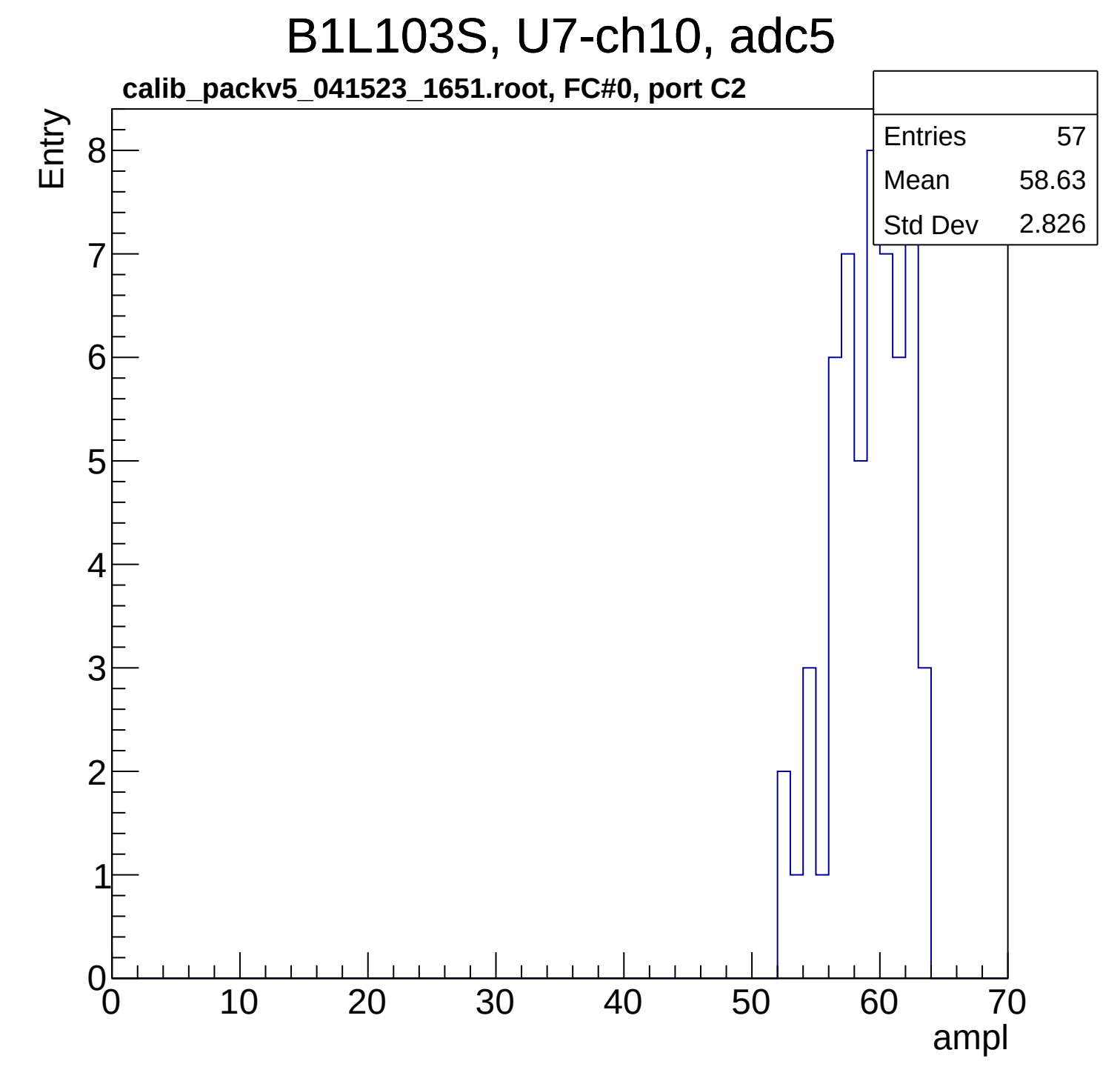
B1L103S, U7-ch10, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 58.63
Std Dev 2.826
Entry
ampl
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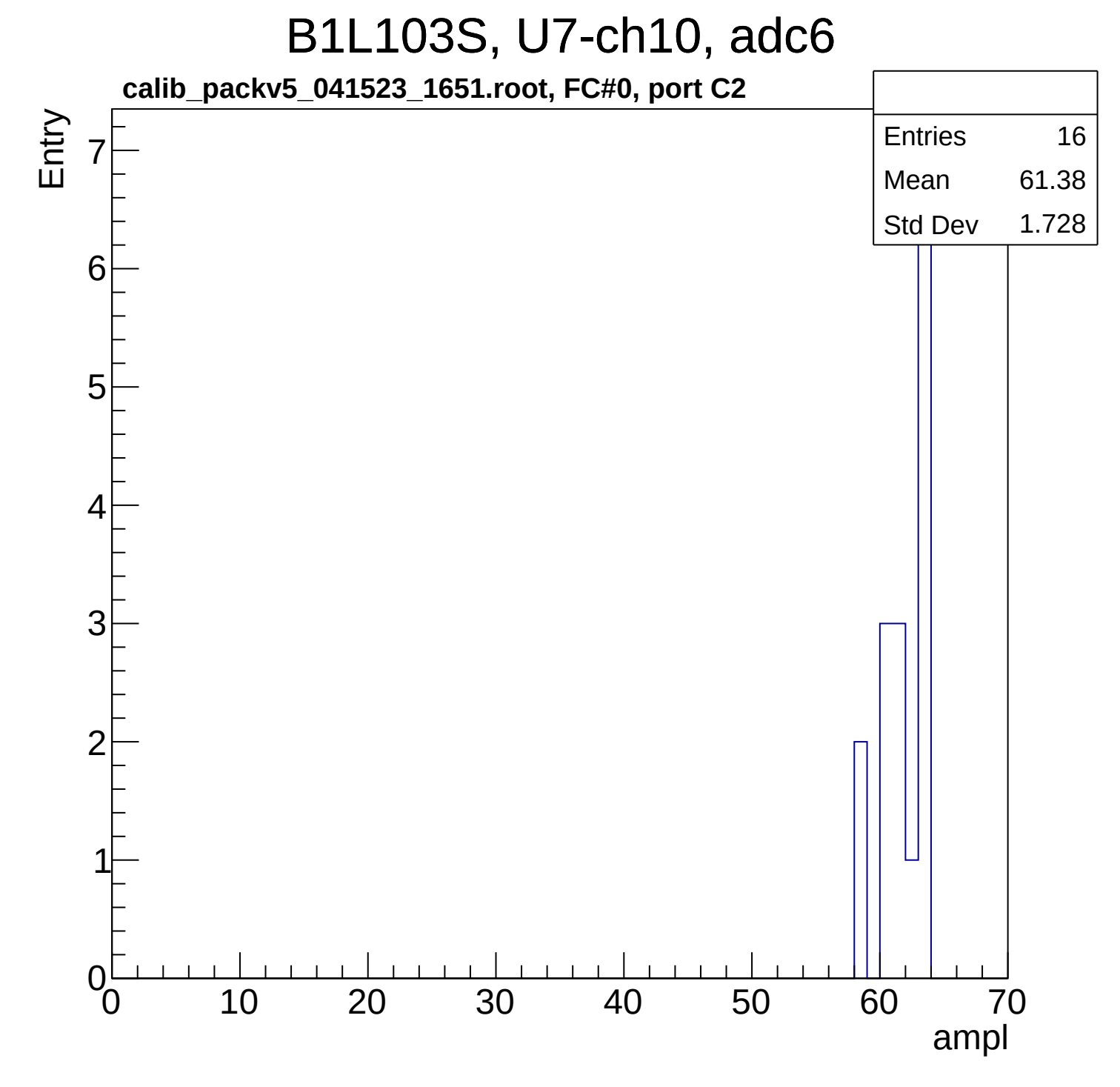
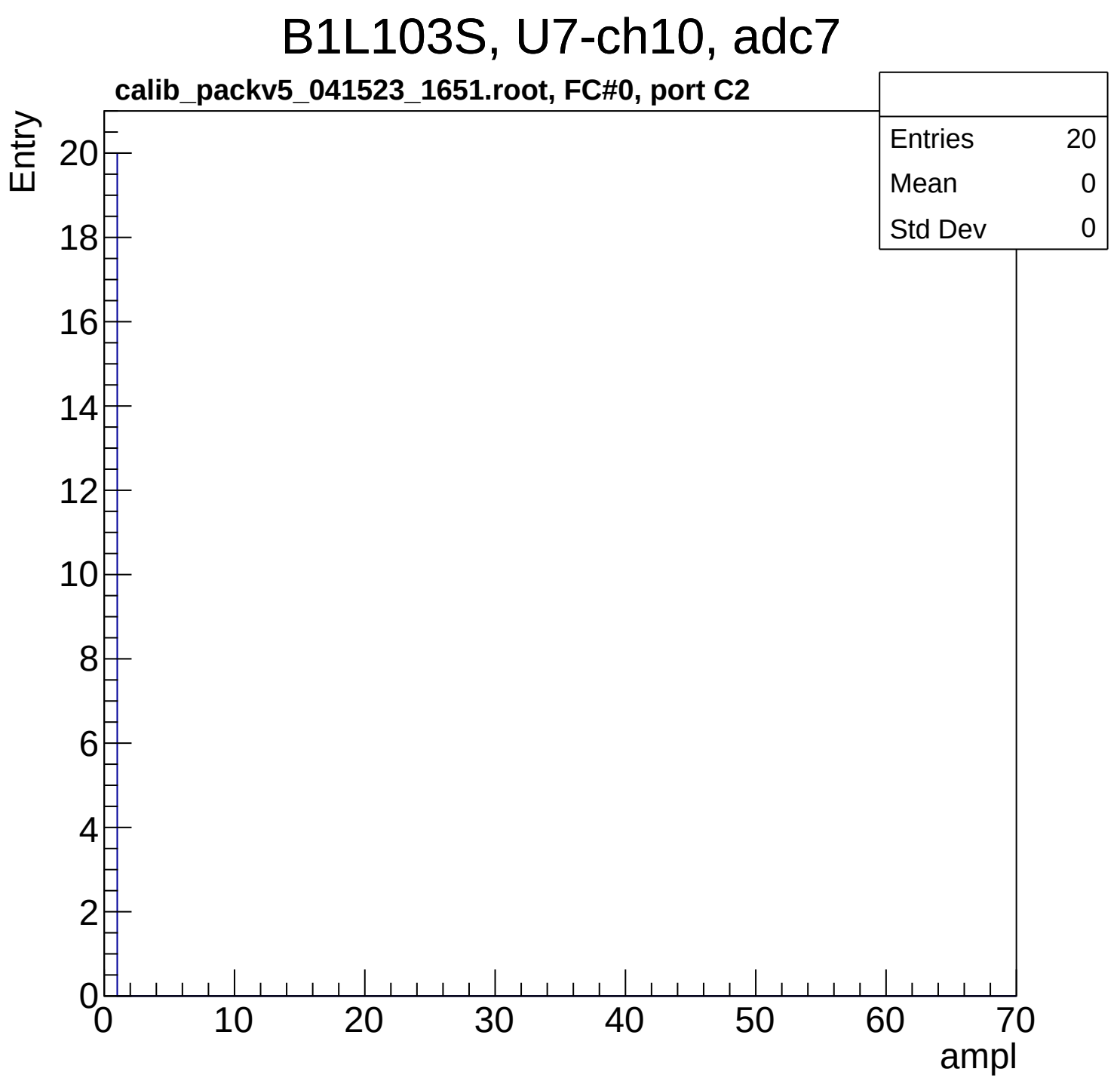
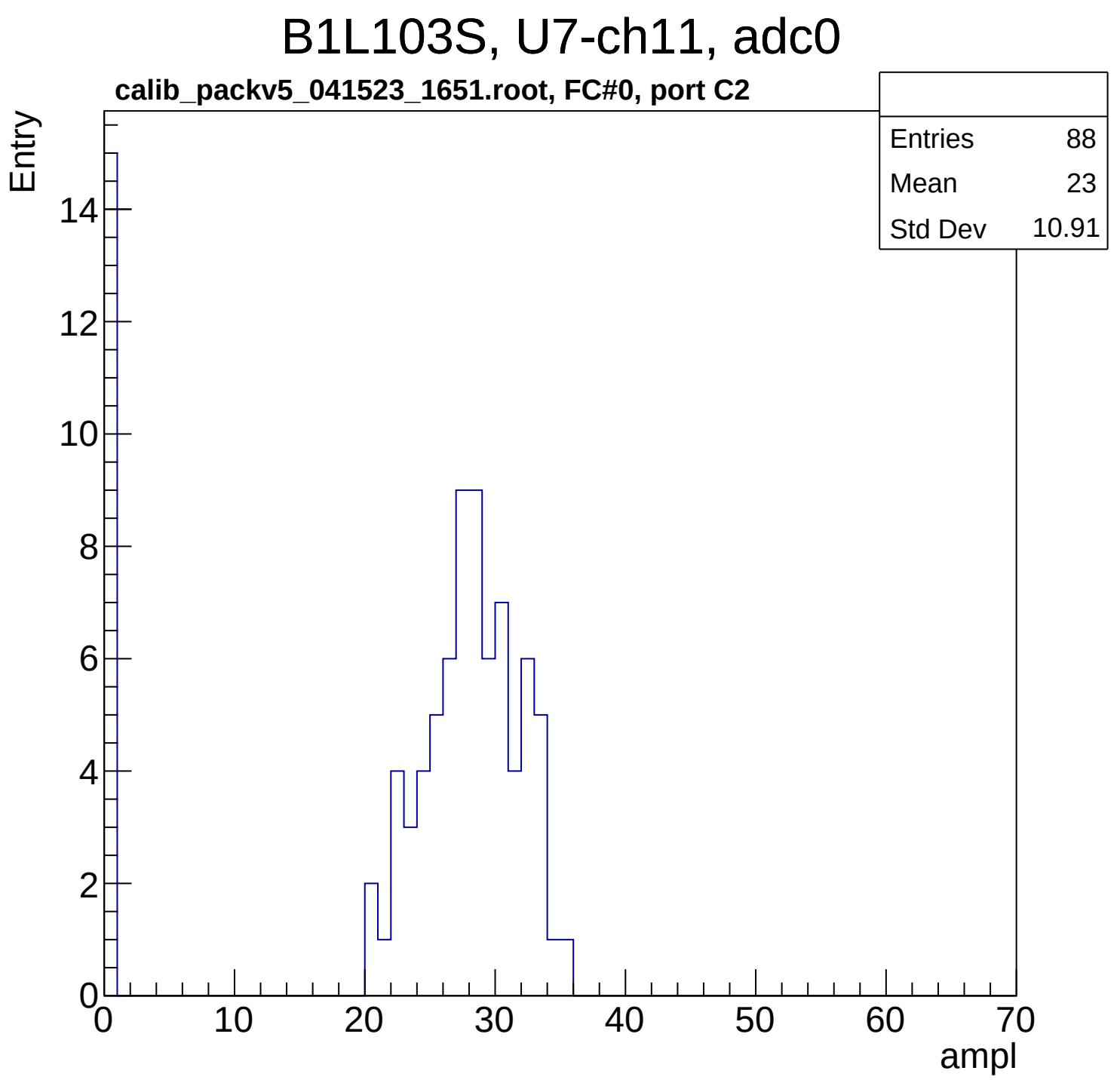
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch10, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 16
Mean 61.38
Std Dev 1.728
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U7-ch10, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch11, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 88
Mean 23
Std Dev 10.91
Entry
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6
8
10
12
14
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10
20
30
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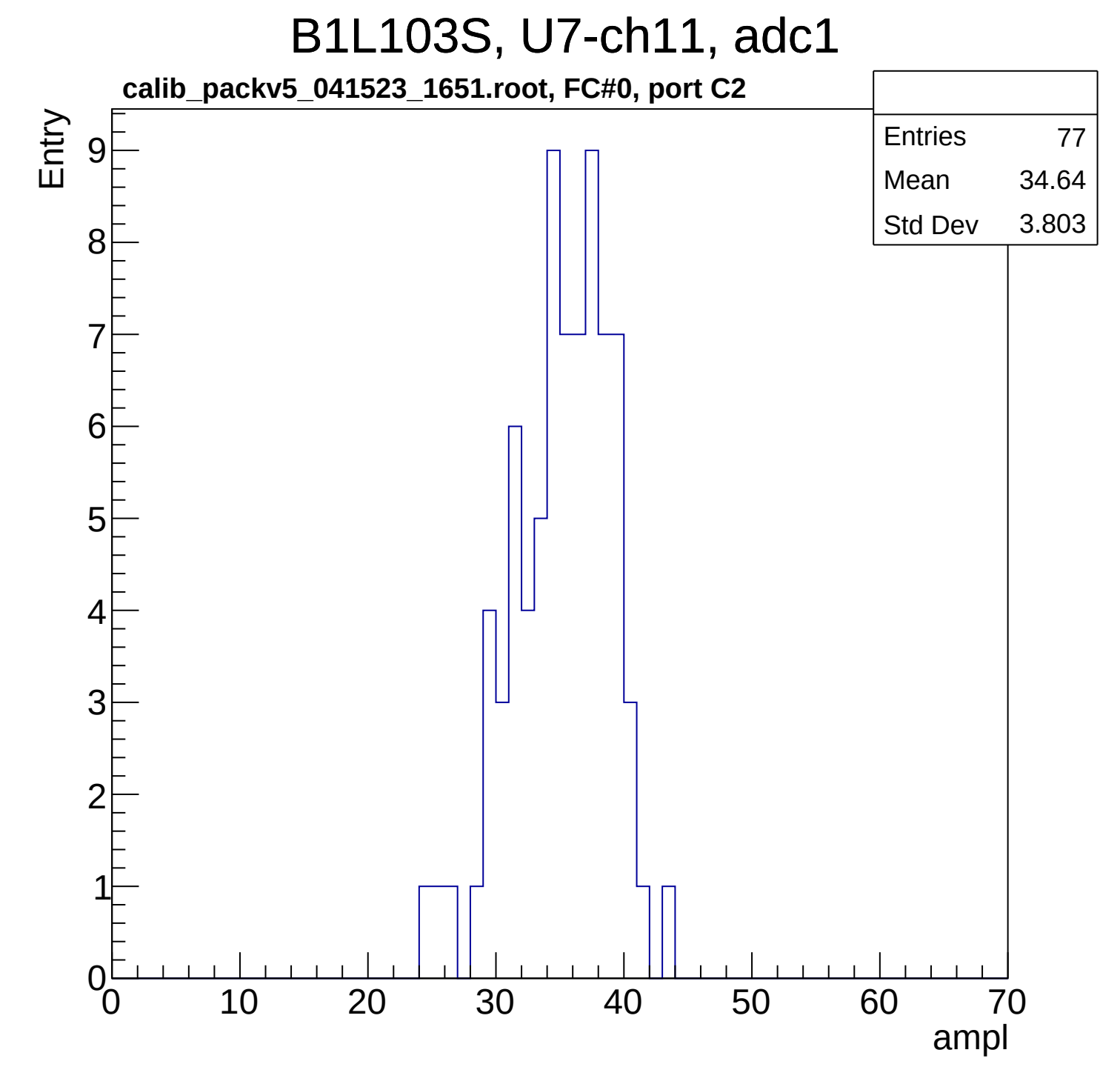
50
60
70
ampl


B1L103S, U7-ch11, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 34.64
Std Dev 3.803
Entry
ampl
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4
5
6
7
8
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0
10
20
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40
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60
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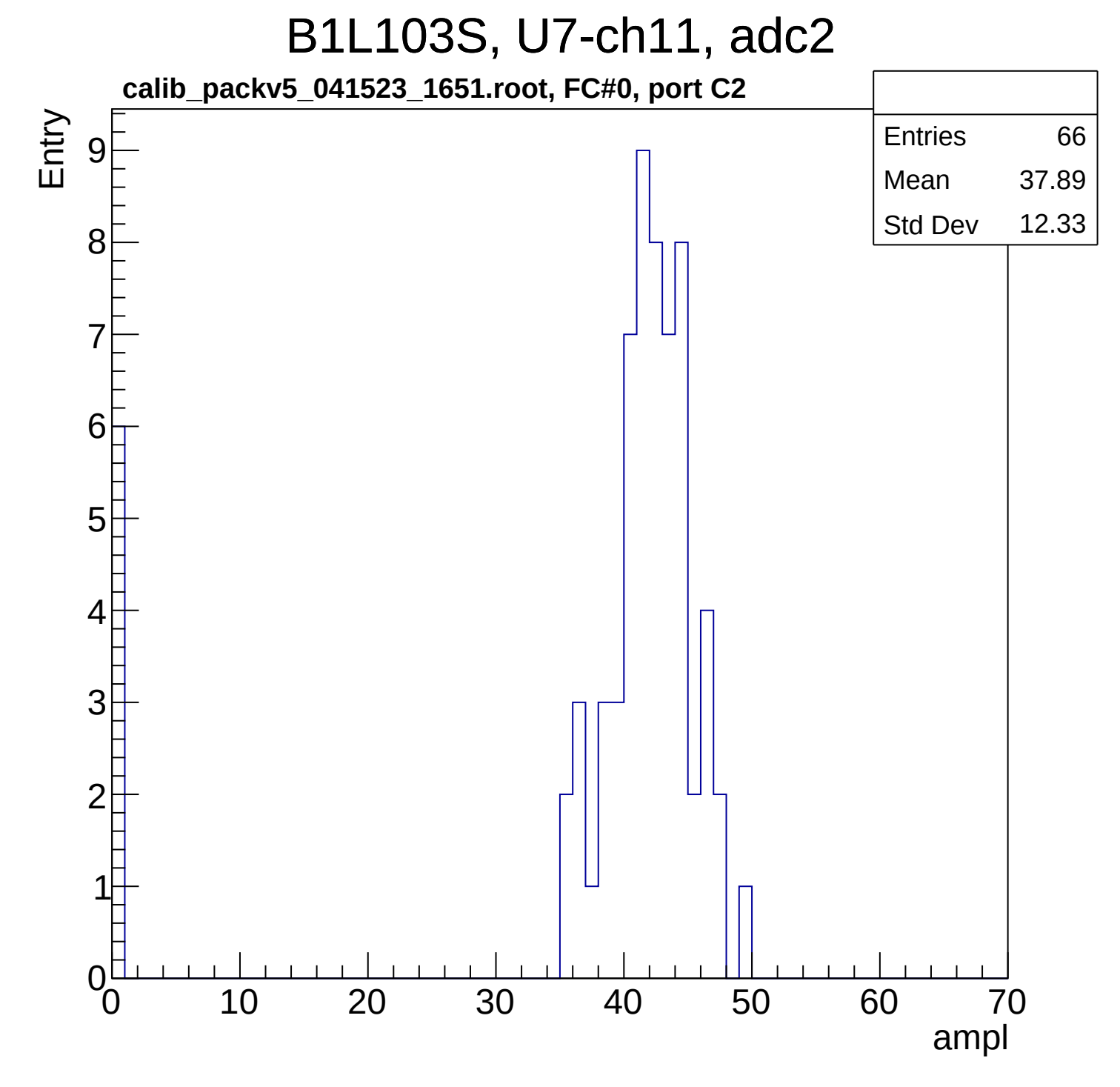
B1L103S, U7-ch11, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 37.89
Std Dev 12.33
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
50
60
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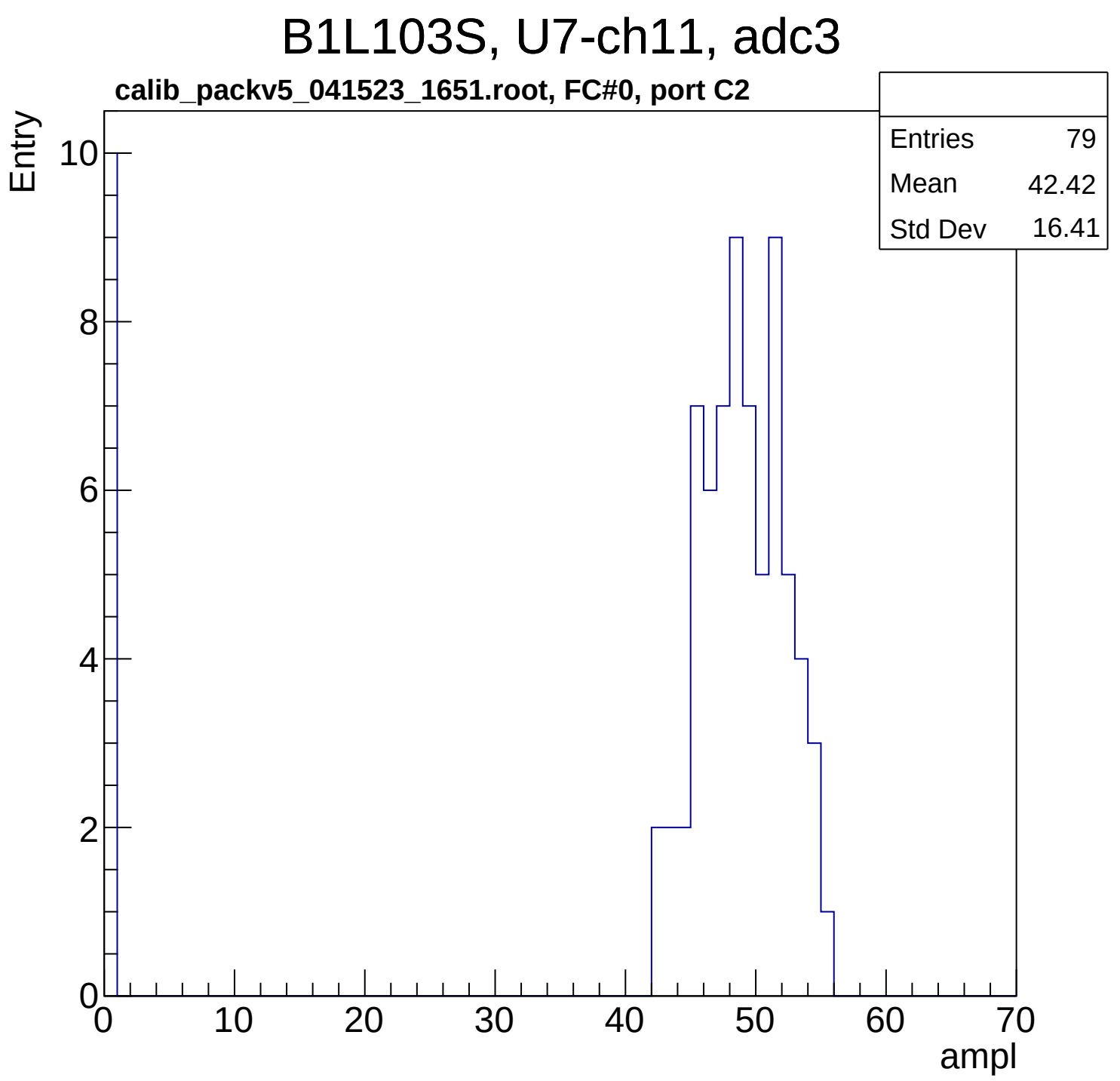
B1L103S, U7-ch11, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 42.42
Std Dev 16.41
Entry
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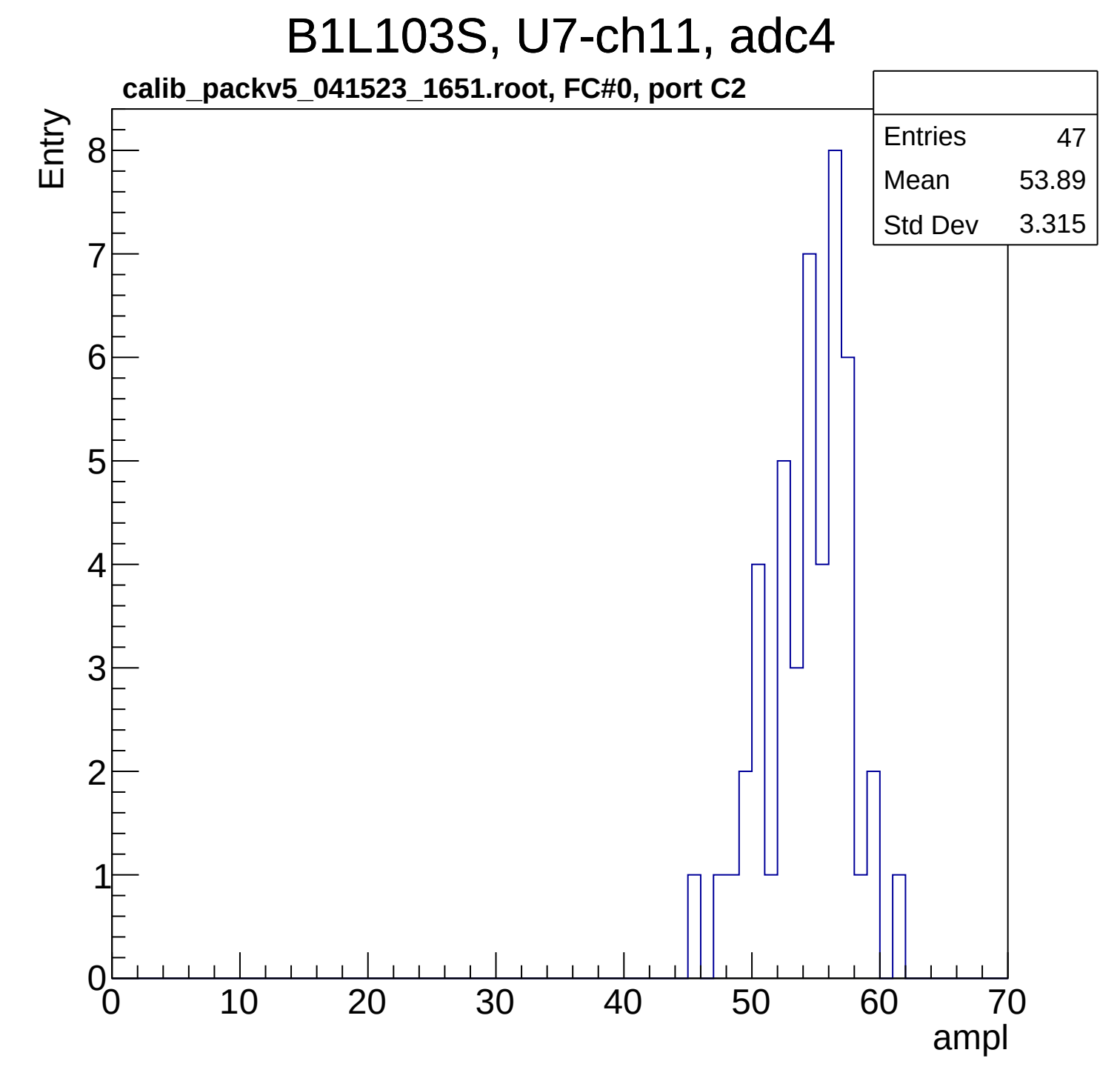
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch11, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 53.89
Std Dev 3.315
Entry
ampl
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7
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40
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60
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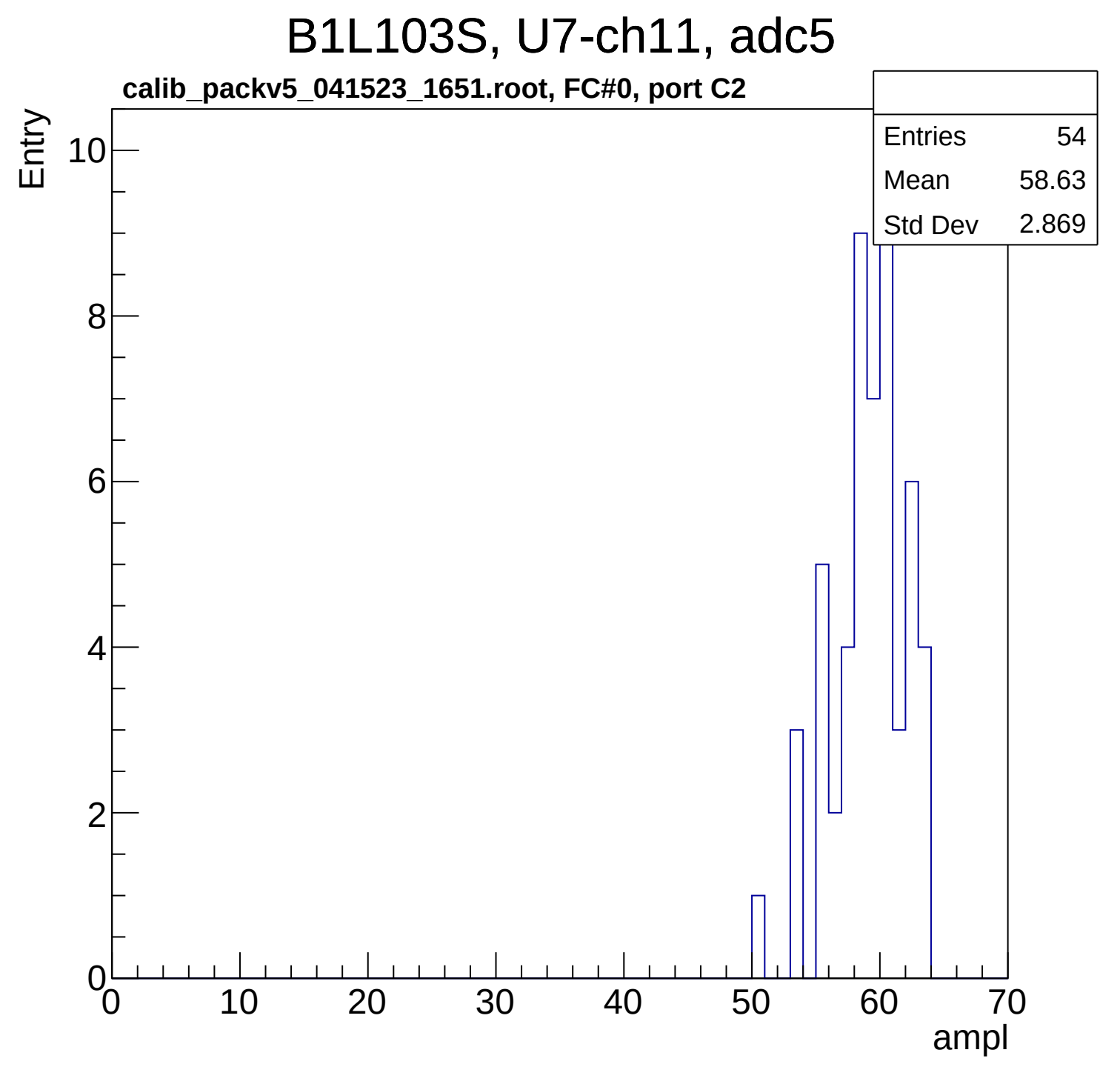
B1L103S, U7-ch11, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 58.63
Std Dev 2.869
Entry
ampl
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10
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10
20
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40
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60
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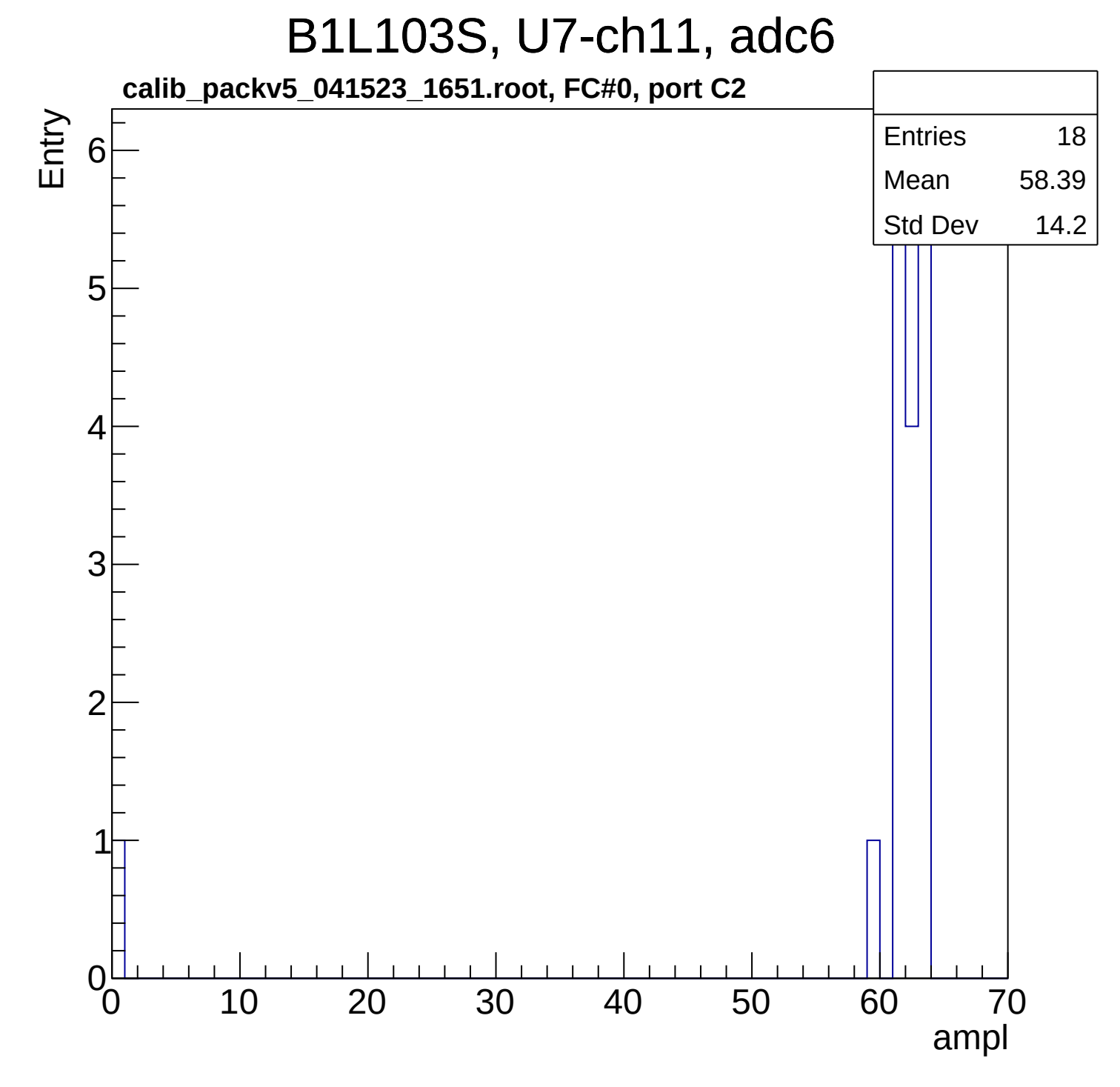
B1L103S, U7-ch11, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 58.39
Std Dev 14.2
Entry
ampl
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2
3
4
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0
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20
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40
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60
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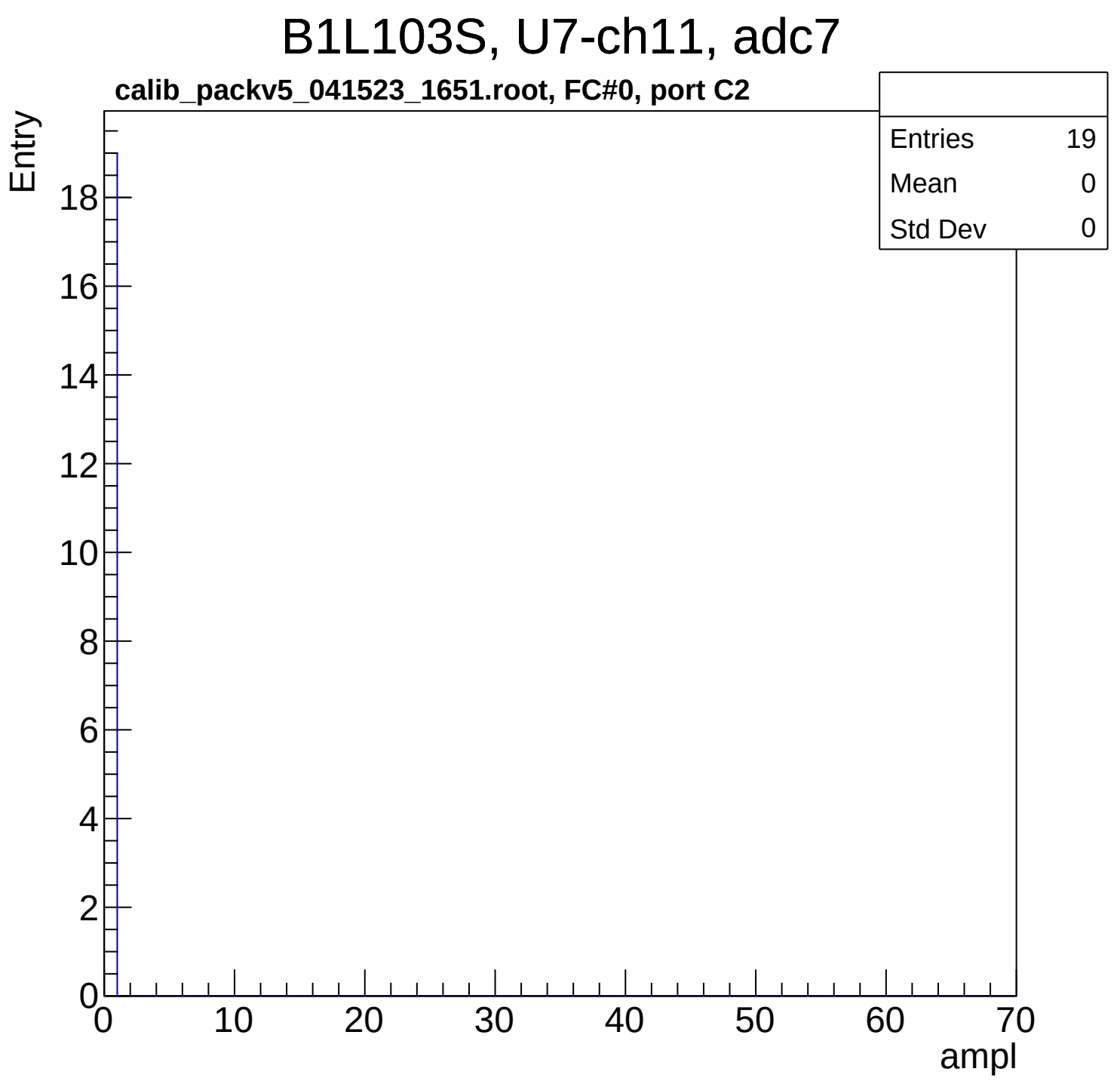
B1L103S, U7-ch11, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
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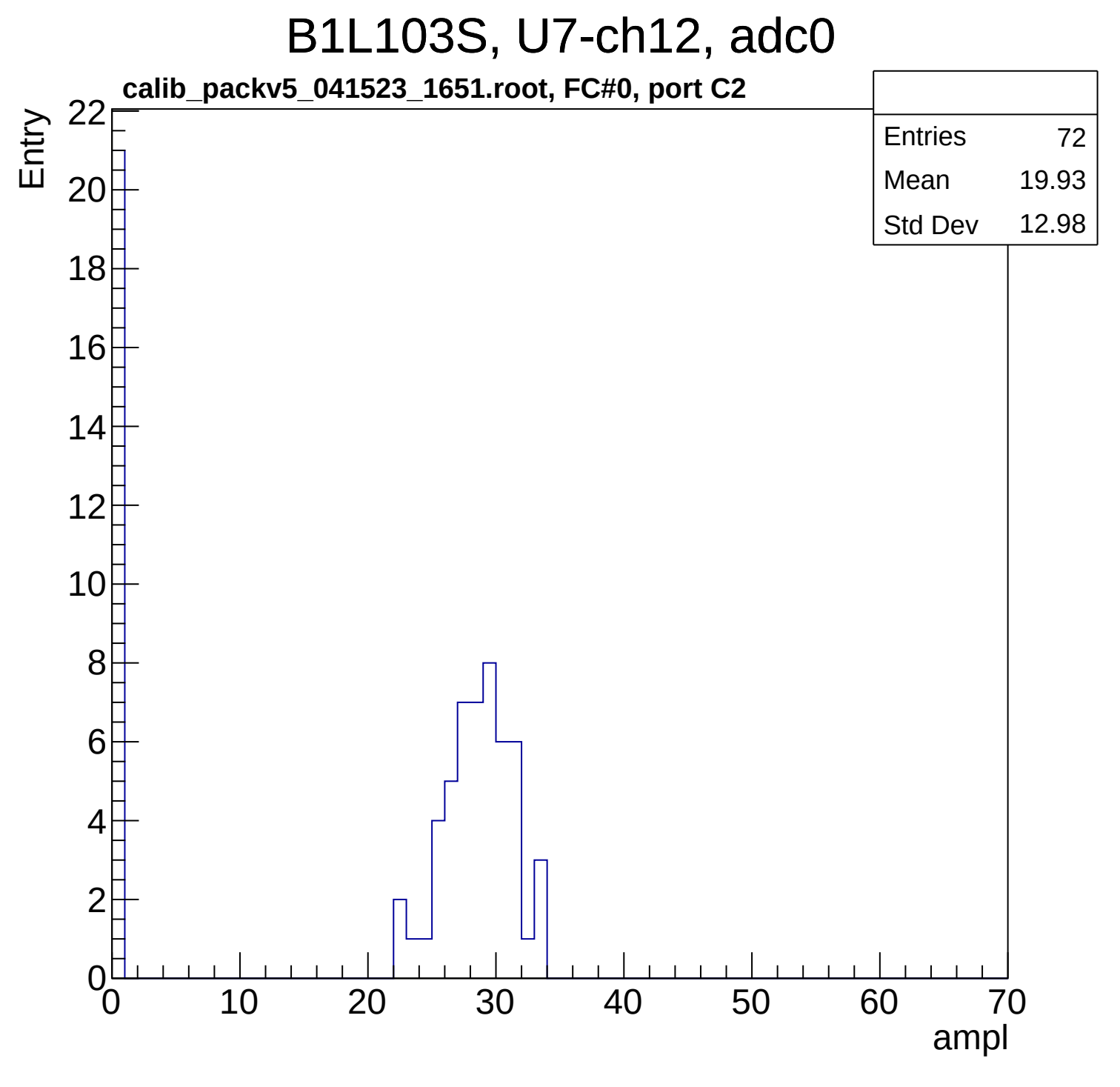
50
60
70
ampl


B1L103S, U7-ch12, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 19.93
Std Dev 12.98
Entry
ampl
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8
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12
14
16
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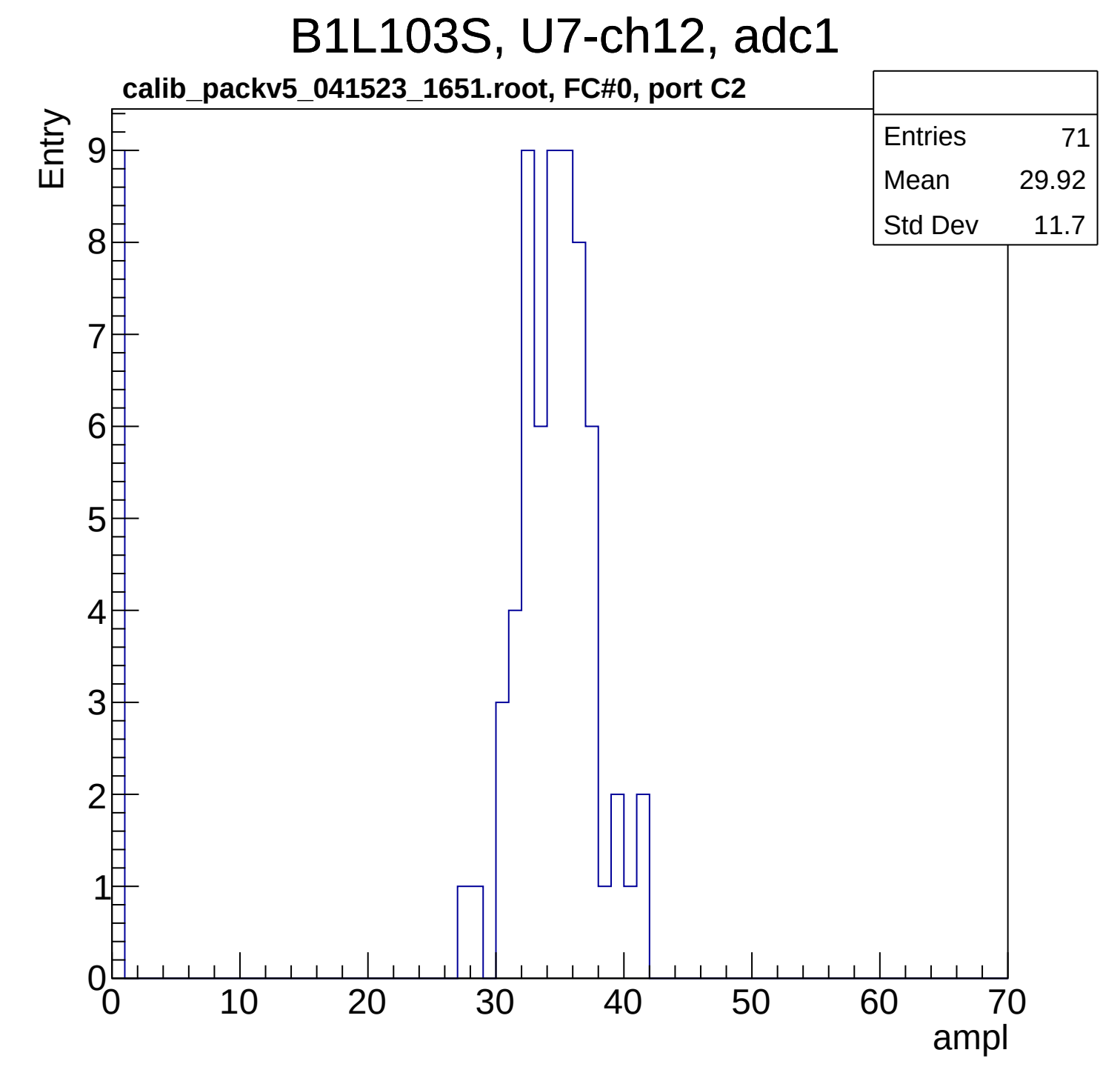
B1L103S, U7-ch12, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 29.92
Std Dev 11.7
Entry
ampl
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3
4
5
6
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0
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60
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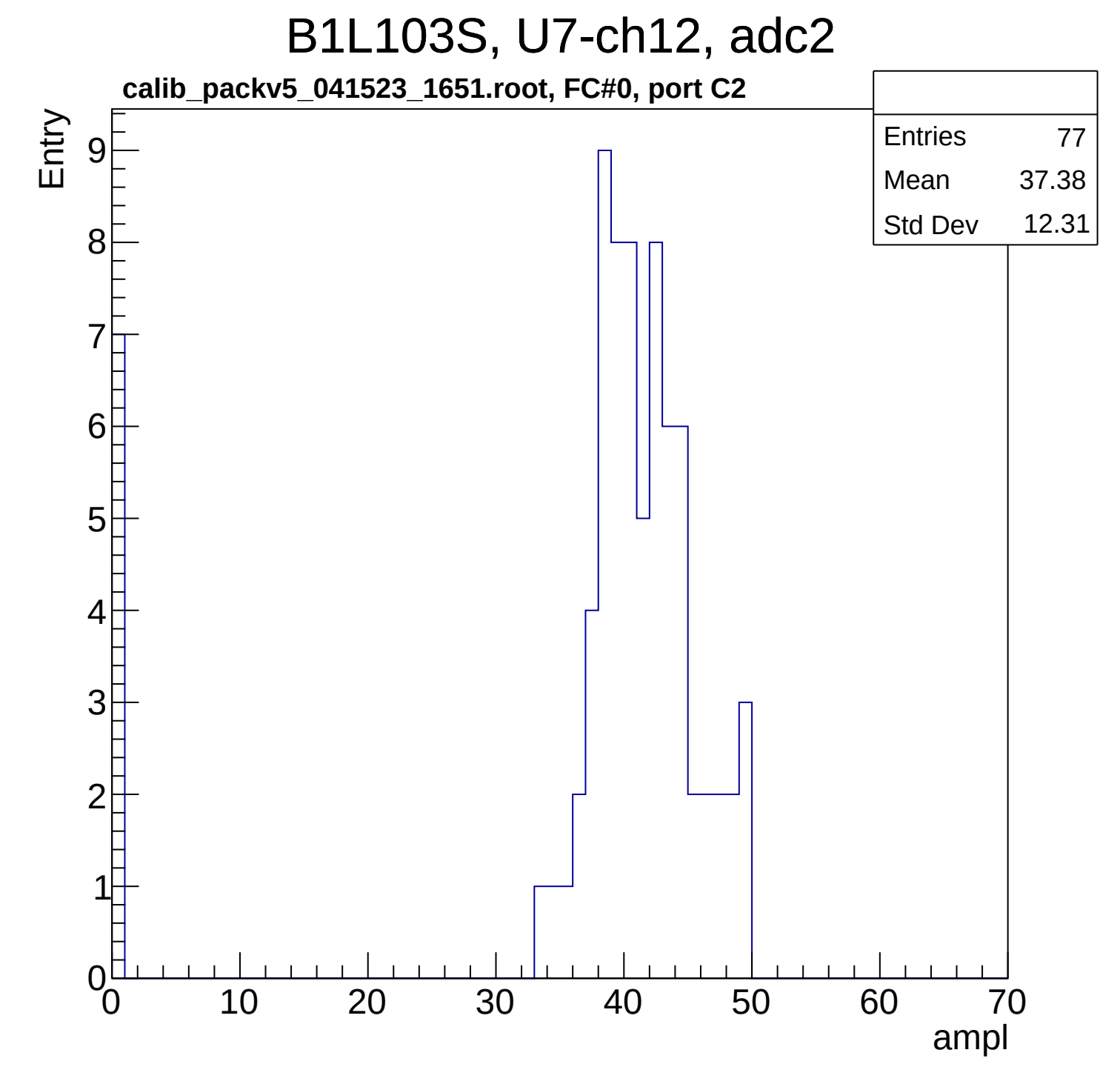
B1L103S, U7-ch12, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 37.38
Std Dev 12.31
Entry
ampl
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3
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8
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0
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60
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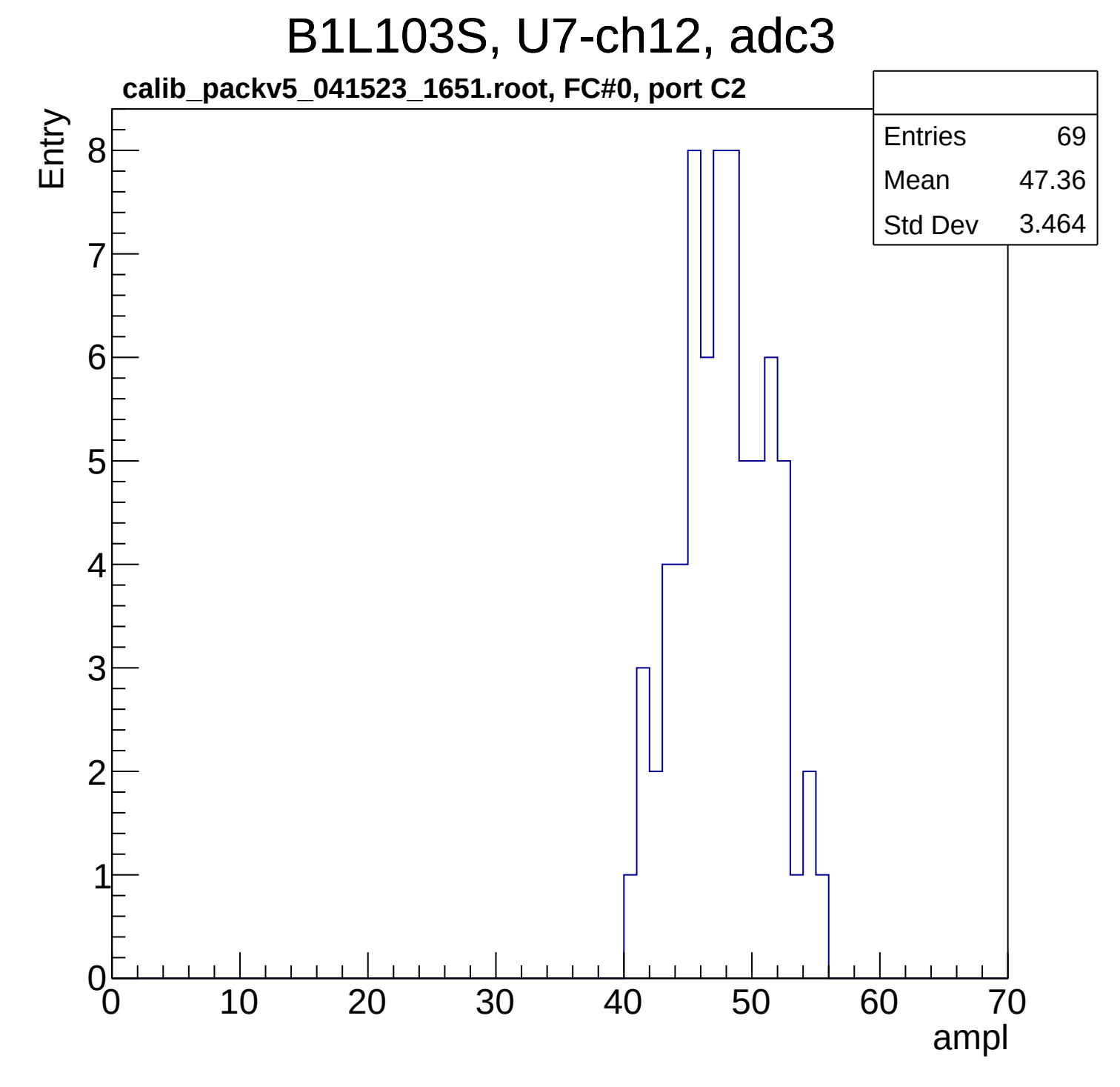
B1L103S, U7-ch12, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 47.36
Std Dev 3.464
Entry
ampl
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2
3
4
5
6
7
8
0
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20
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40
50
60
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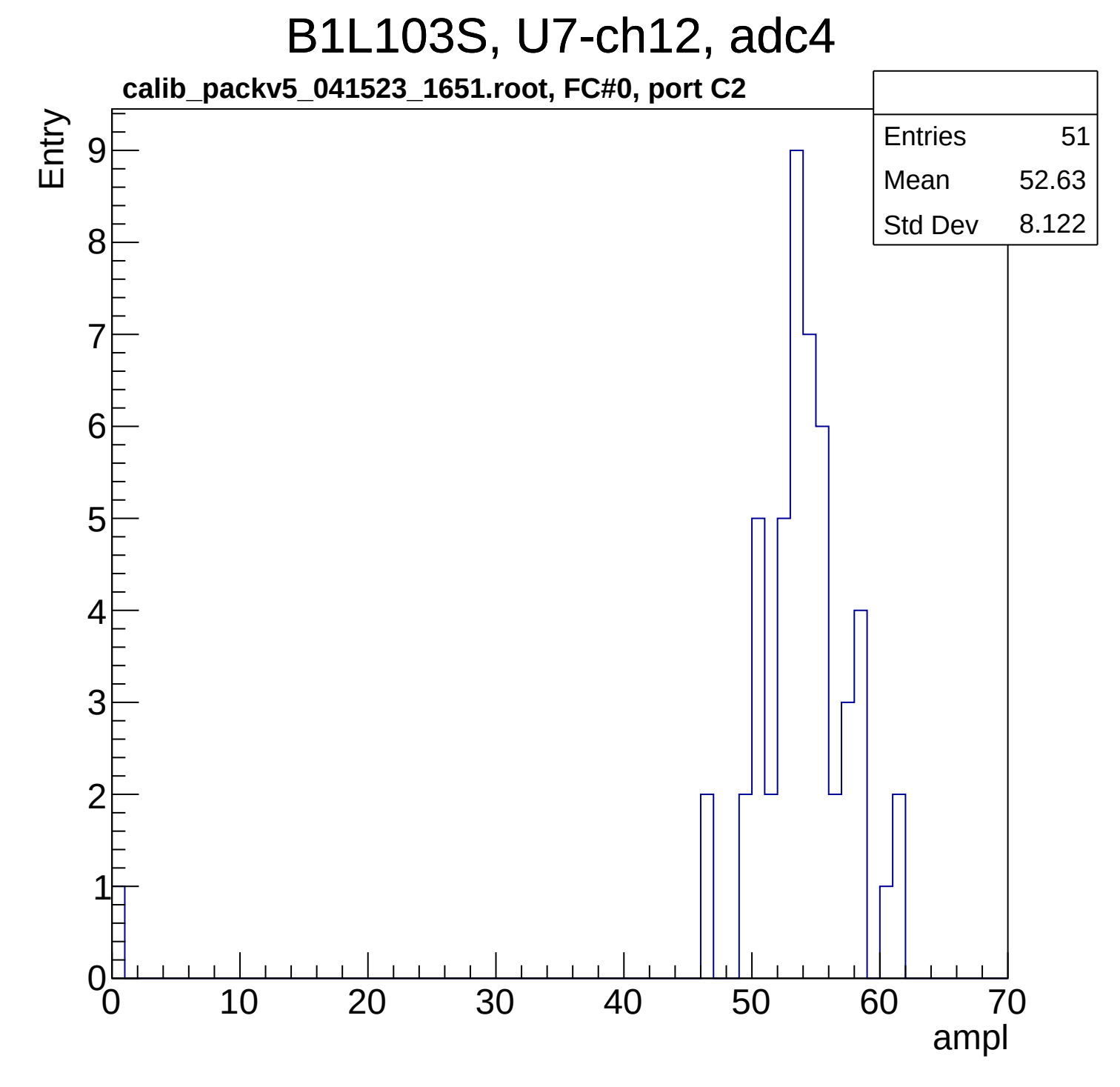
B1L103S, U7-ch12, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 52.63
Std Dev 8.122
Entry
ampl
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3
4
5
6
7
8
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0
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40
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60
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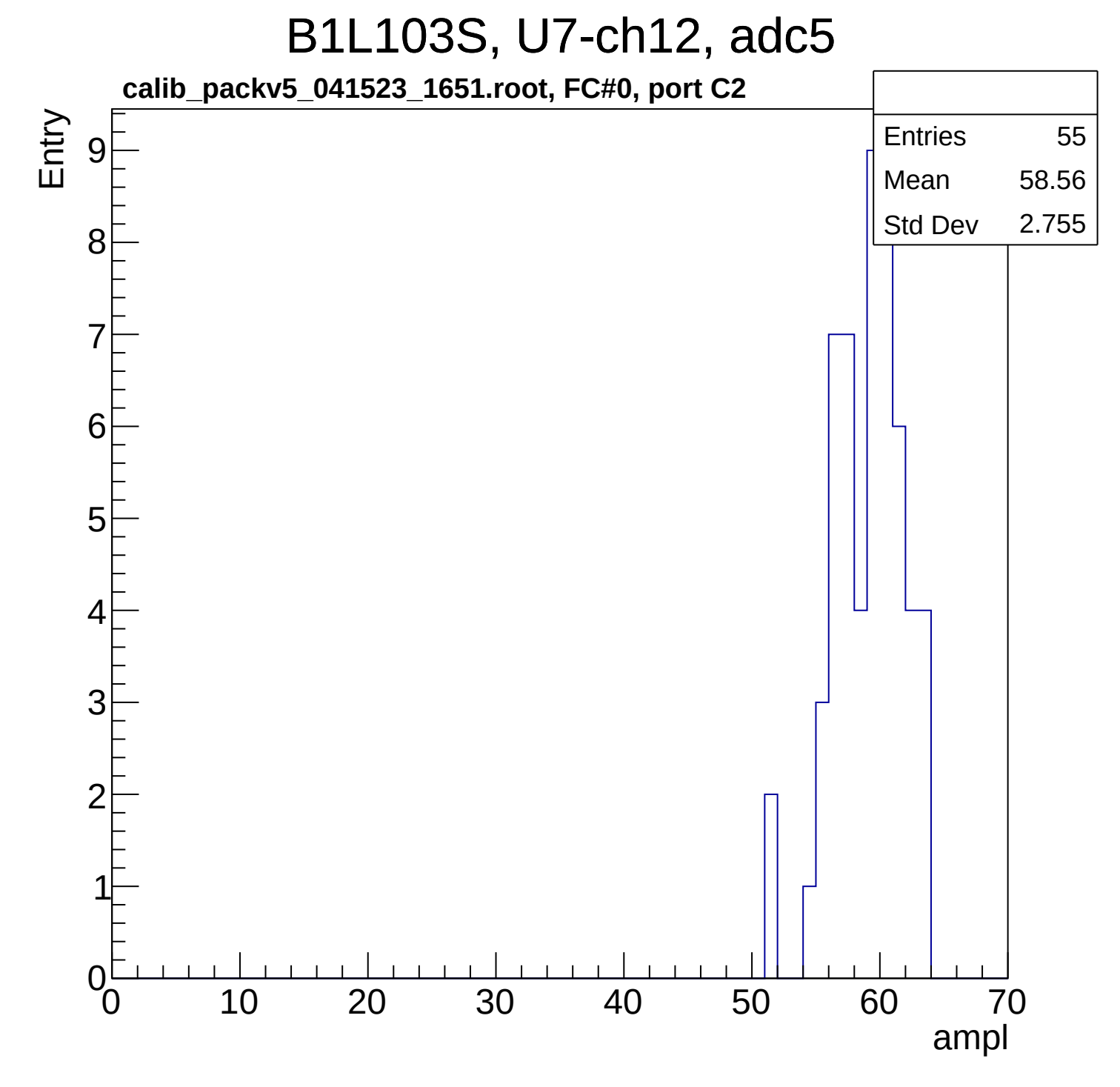
B1L103S, U7-ch12, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 58.56
Std Dev 2.755
Entry
ampl
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5
6
7
8
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0
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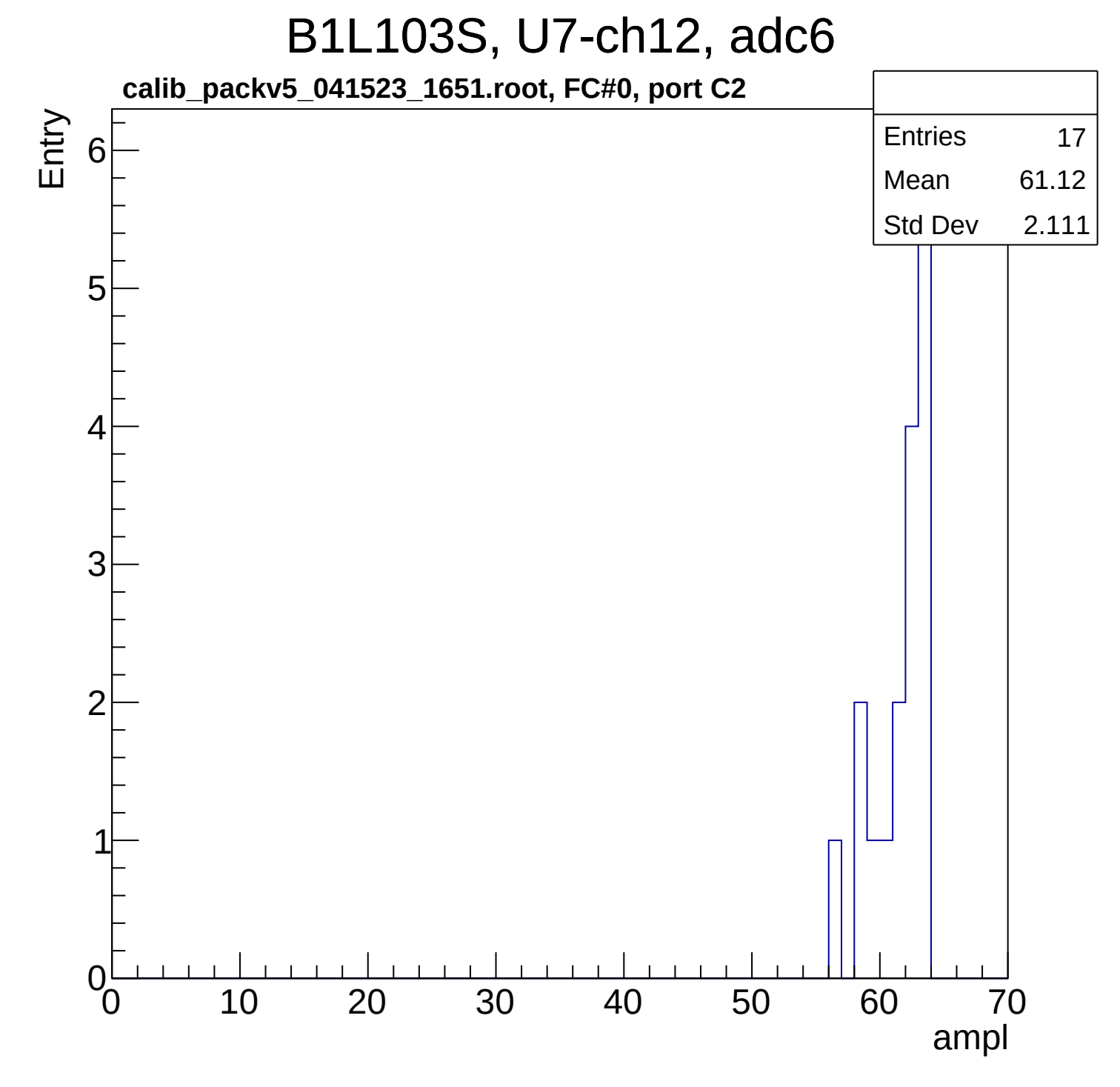
B1L103S, U7-ch12, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 17
Mean 61.12
Std Dev 2.111
Entry
ampl
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2
3
4
5
6
0
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20
30
40
50
60
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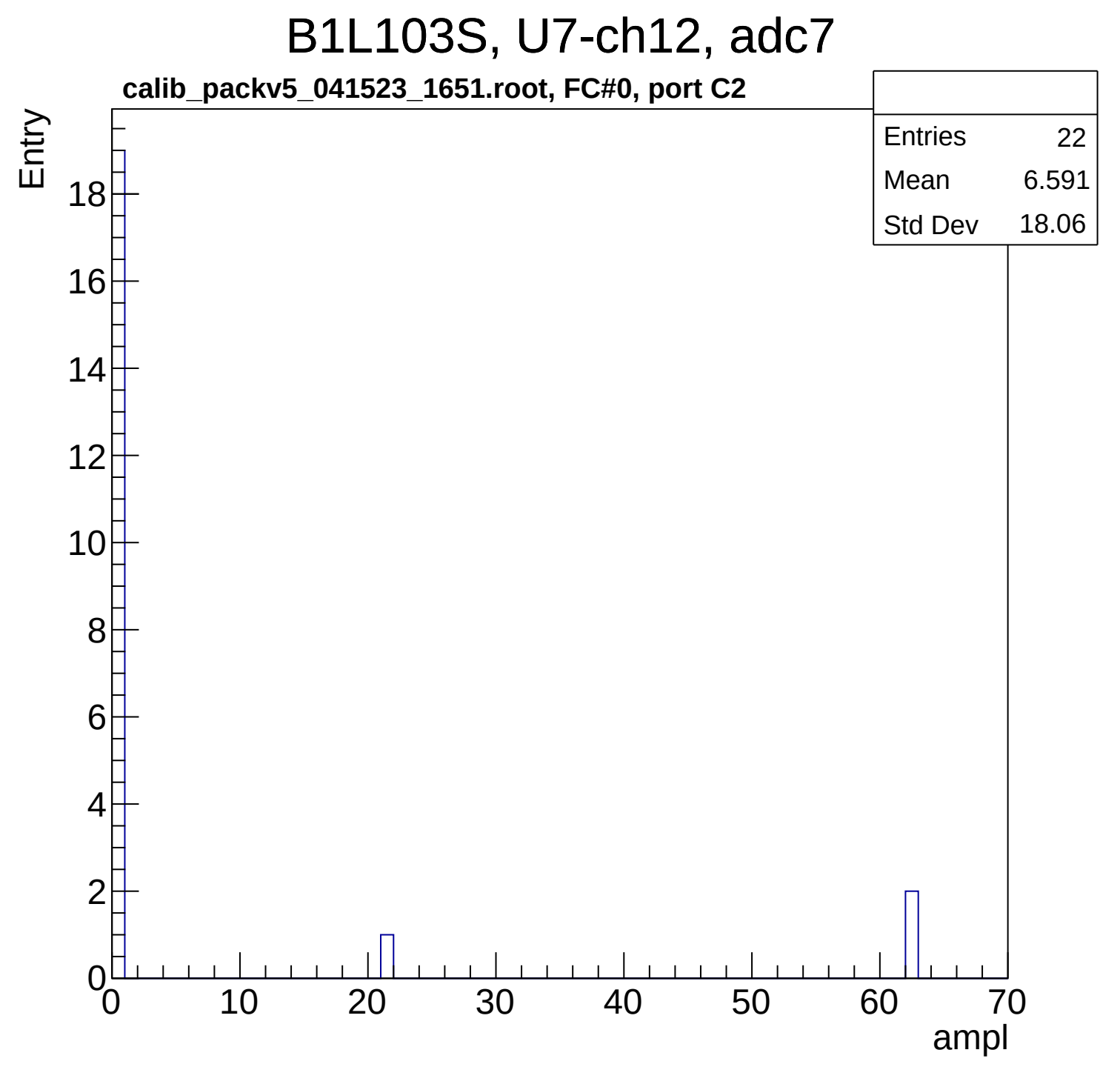
B1L103S, U7-ch12, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 6.591
Std Dev 18.06
Entry
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6
8
10
12
14
16
18
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10
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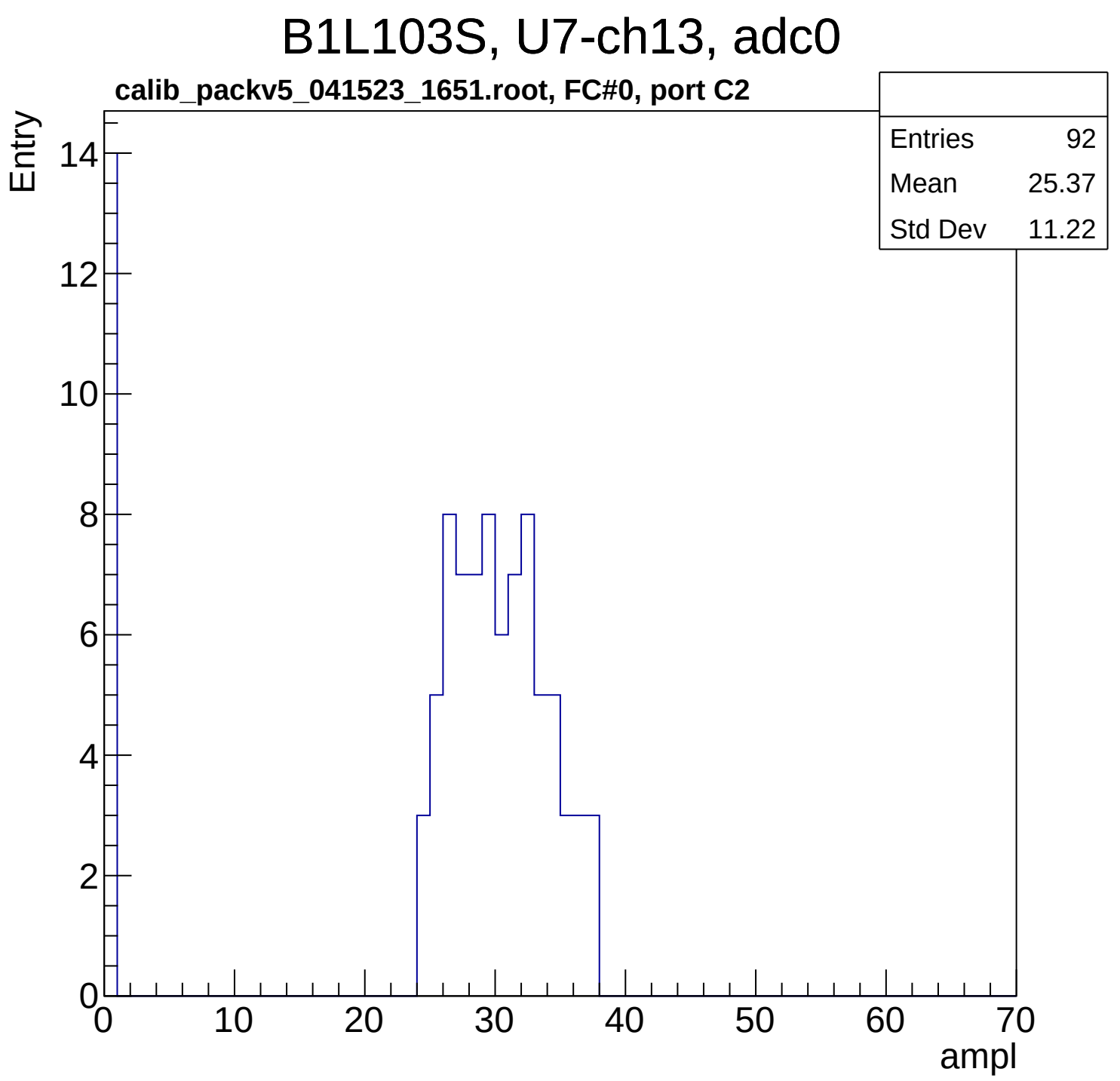
30
40
50
60
70
ampl


B1L103S, U7-ch13, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 92
Mean 25.37
Std Dev 11.22
Entry
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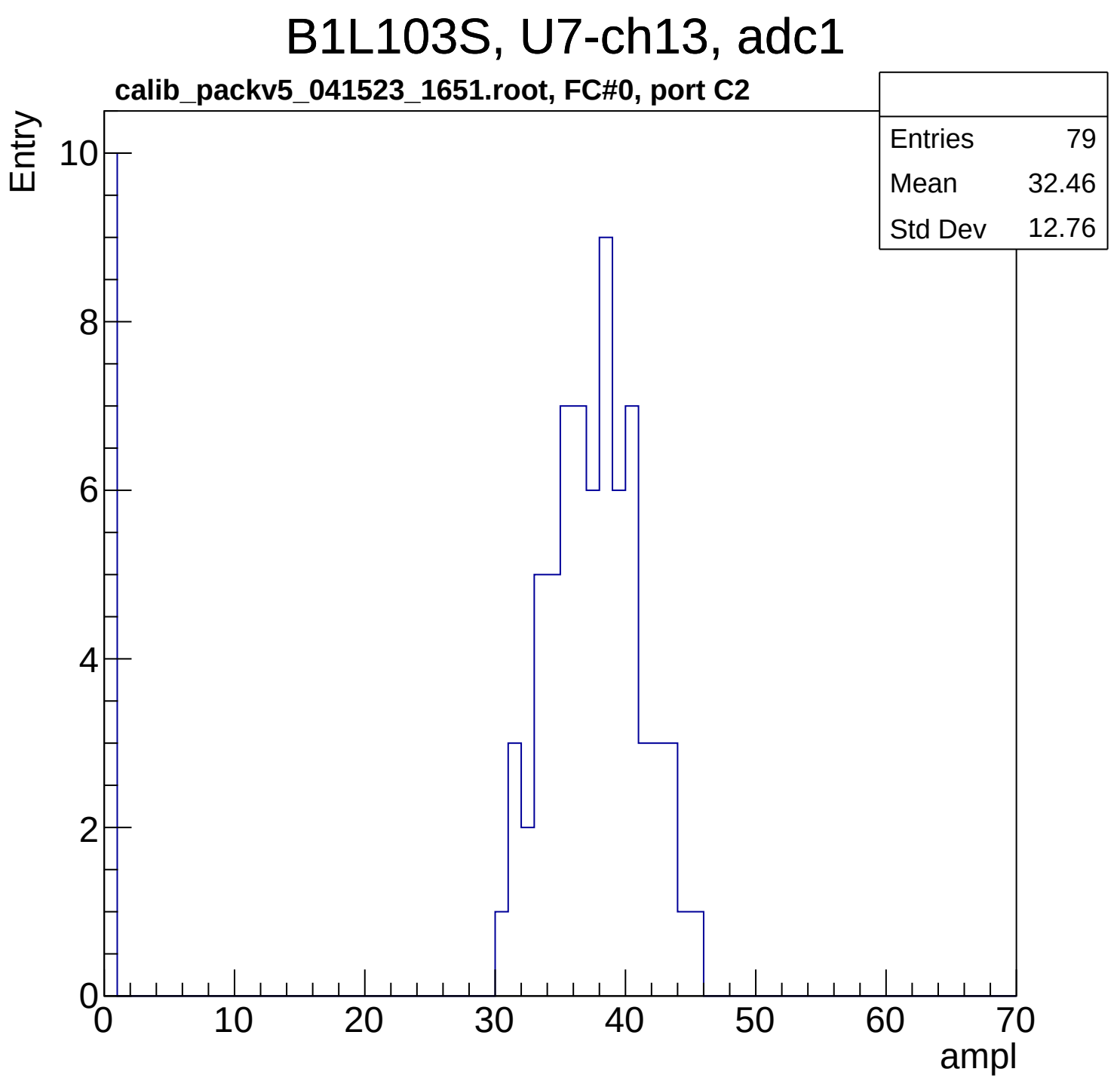
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch13, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 32.46
Std Dev 12.76
Entry
ampl
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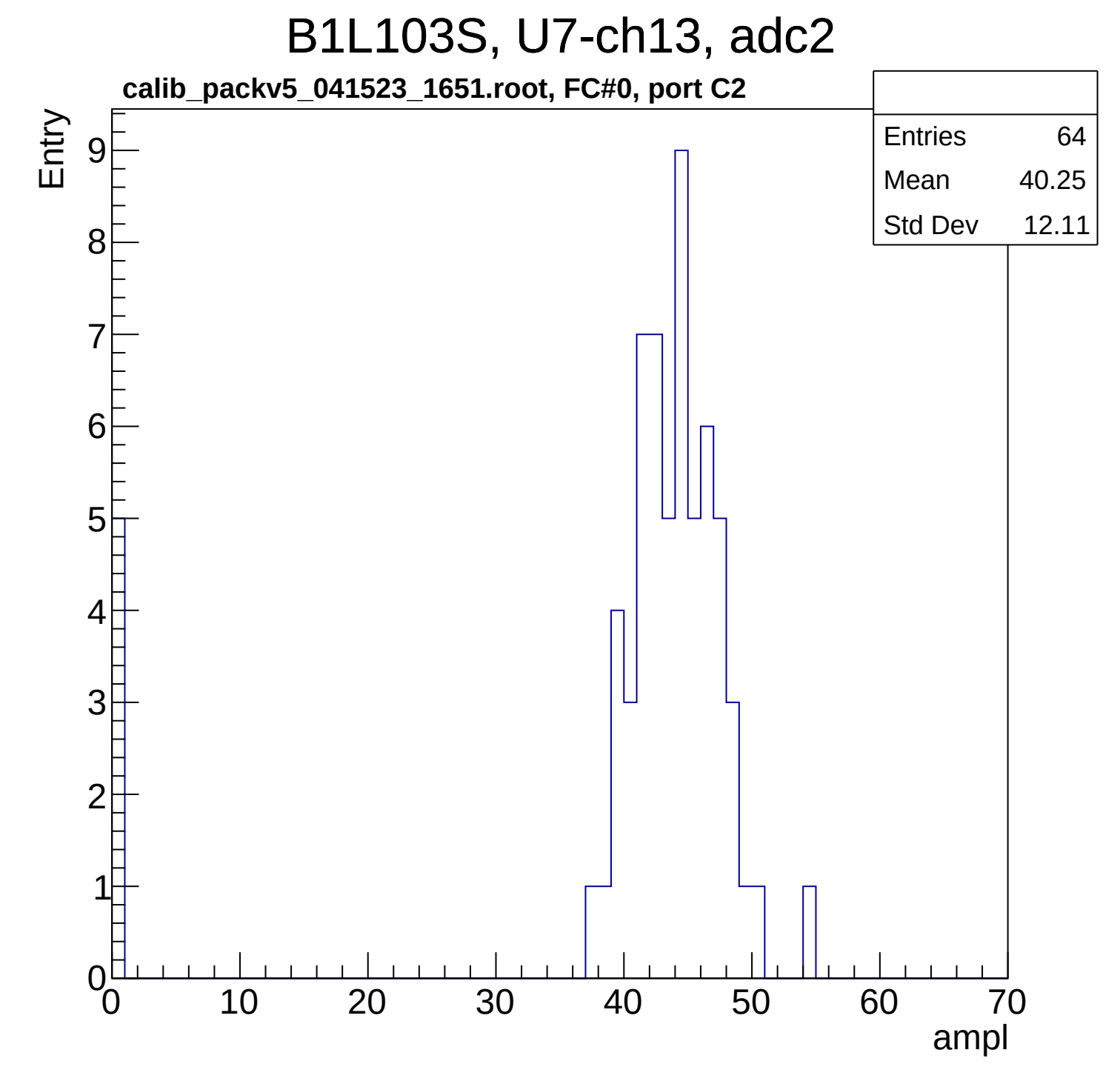
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U7-ch13, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 40.25
Std Dev 12.11
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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40
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60
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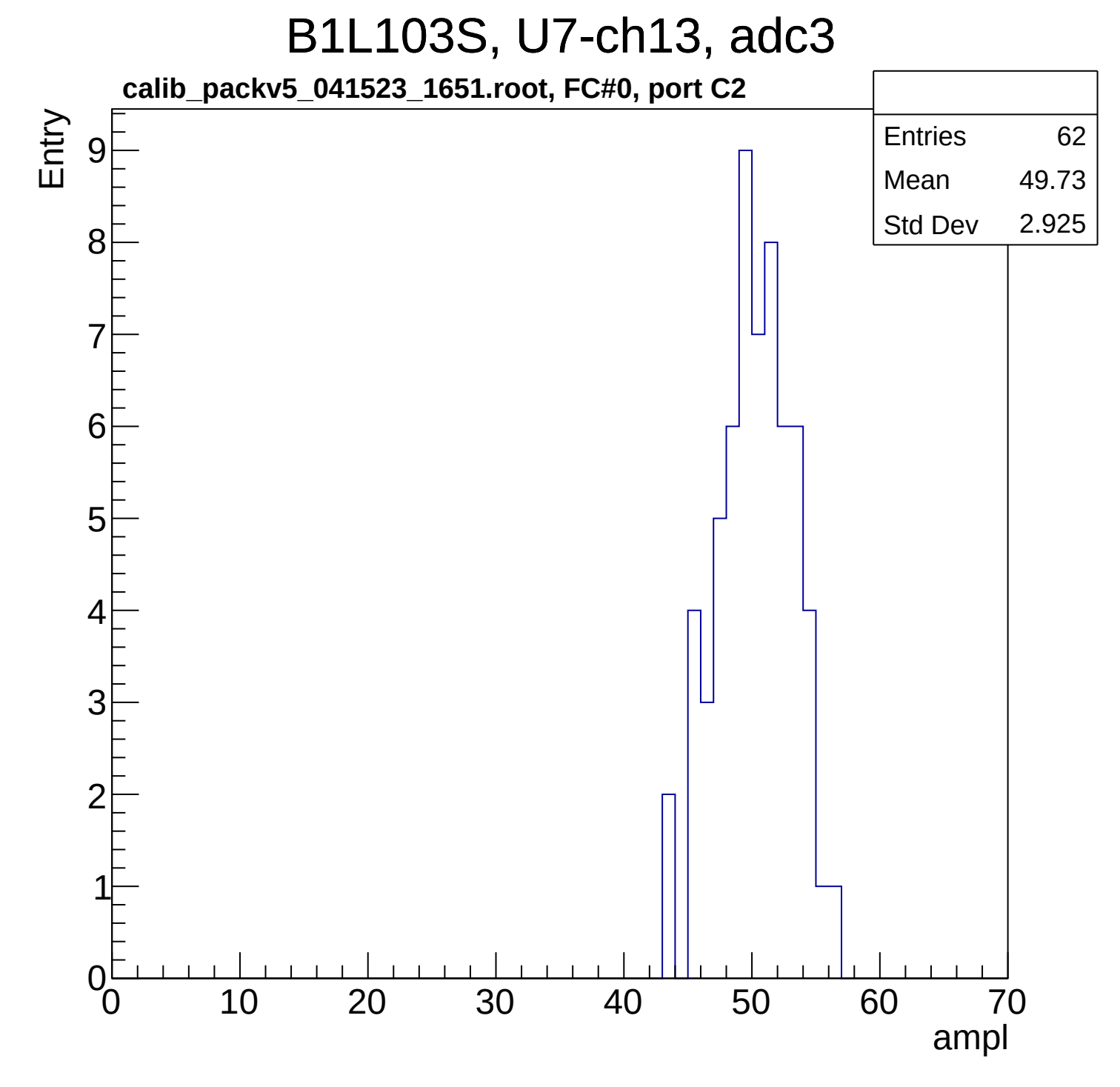
B1L103S, U7-ch13, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 49.73
Std Dev 2.925
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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40
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60
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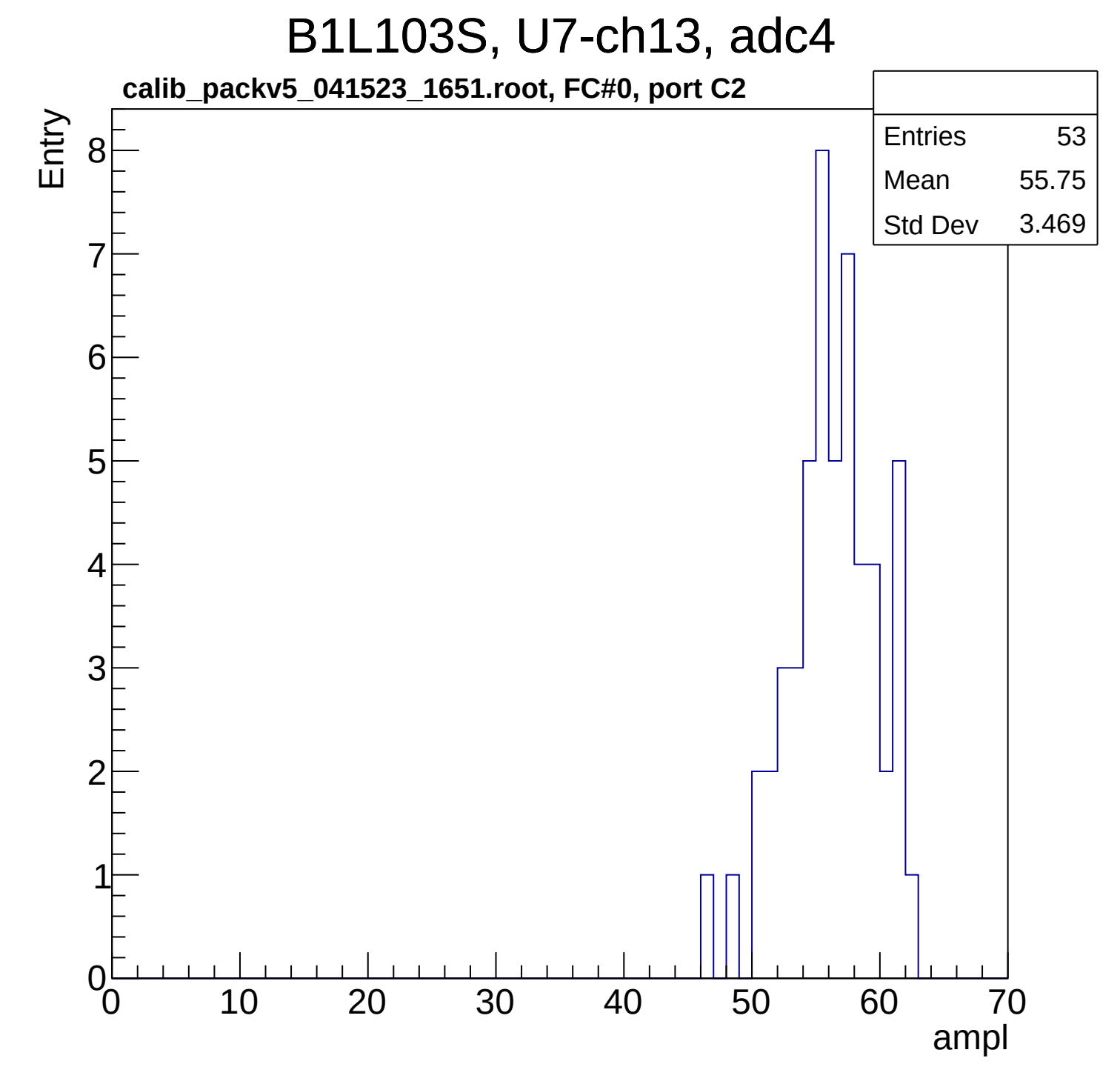
B1L103S, U7-ch13, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 55.75
Std Dev 3.469
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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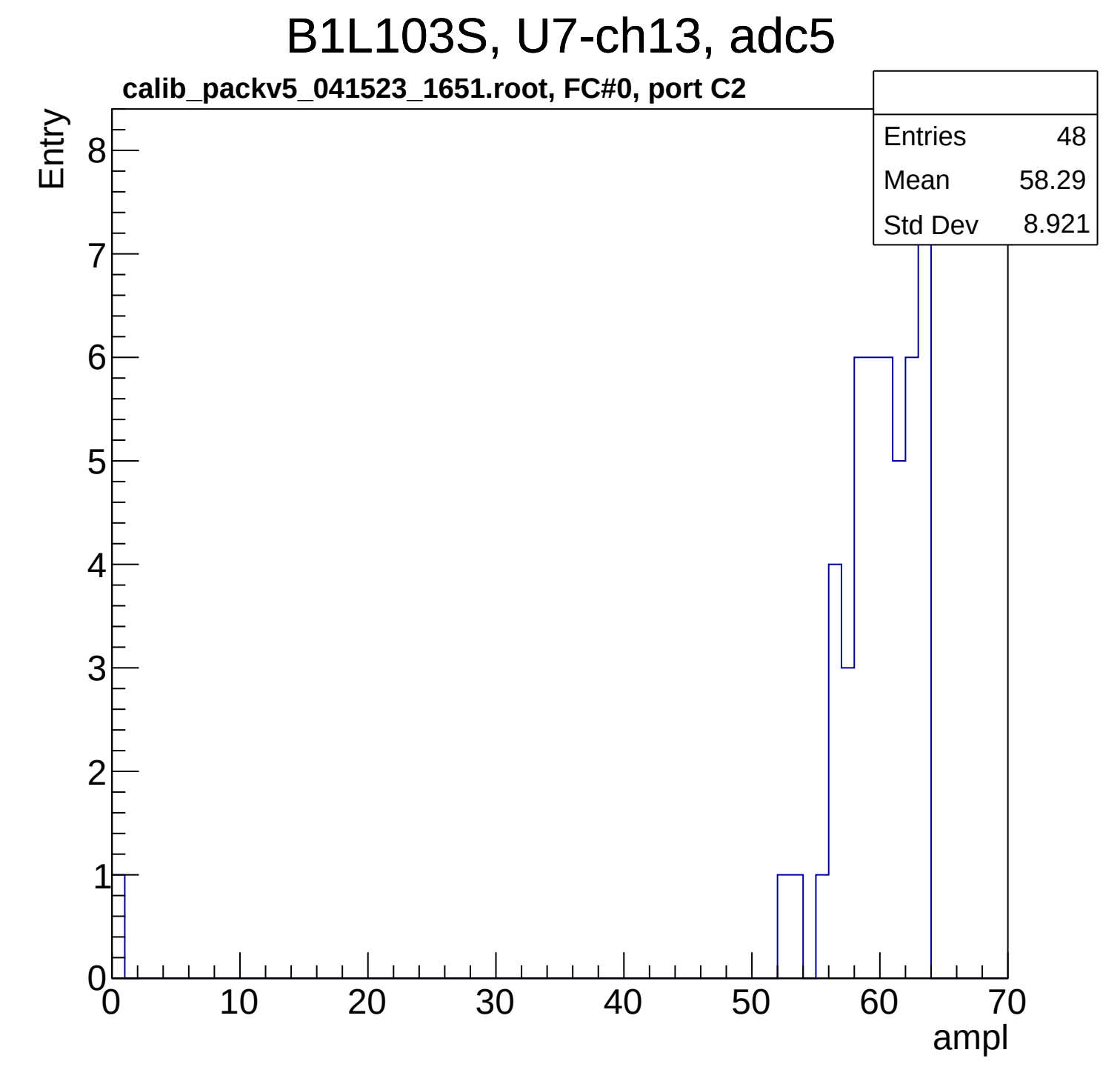
B1L103S, U7-ch13, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 58.29
Std Dev 8.921
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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40
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60
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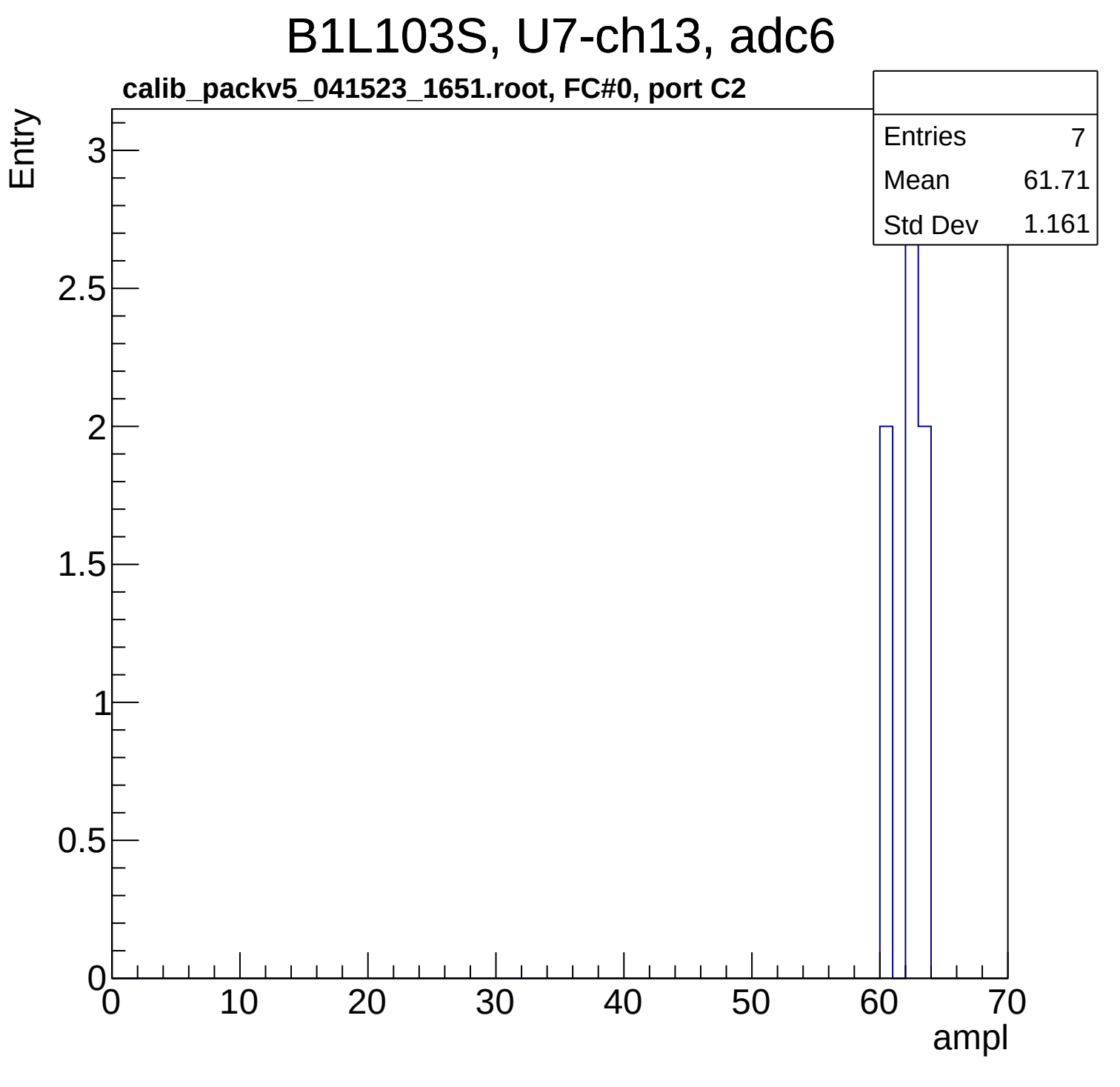
B1L103S, U7-ch13, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 61.71
Std Dev 1.161
Entry
ampl
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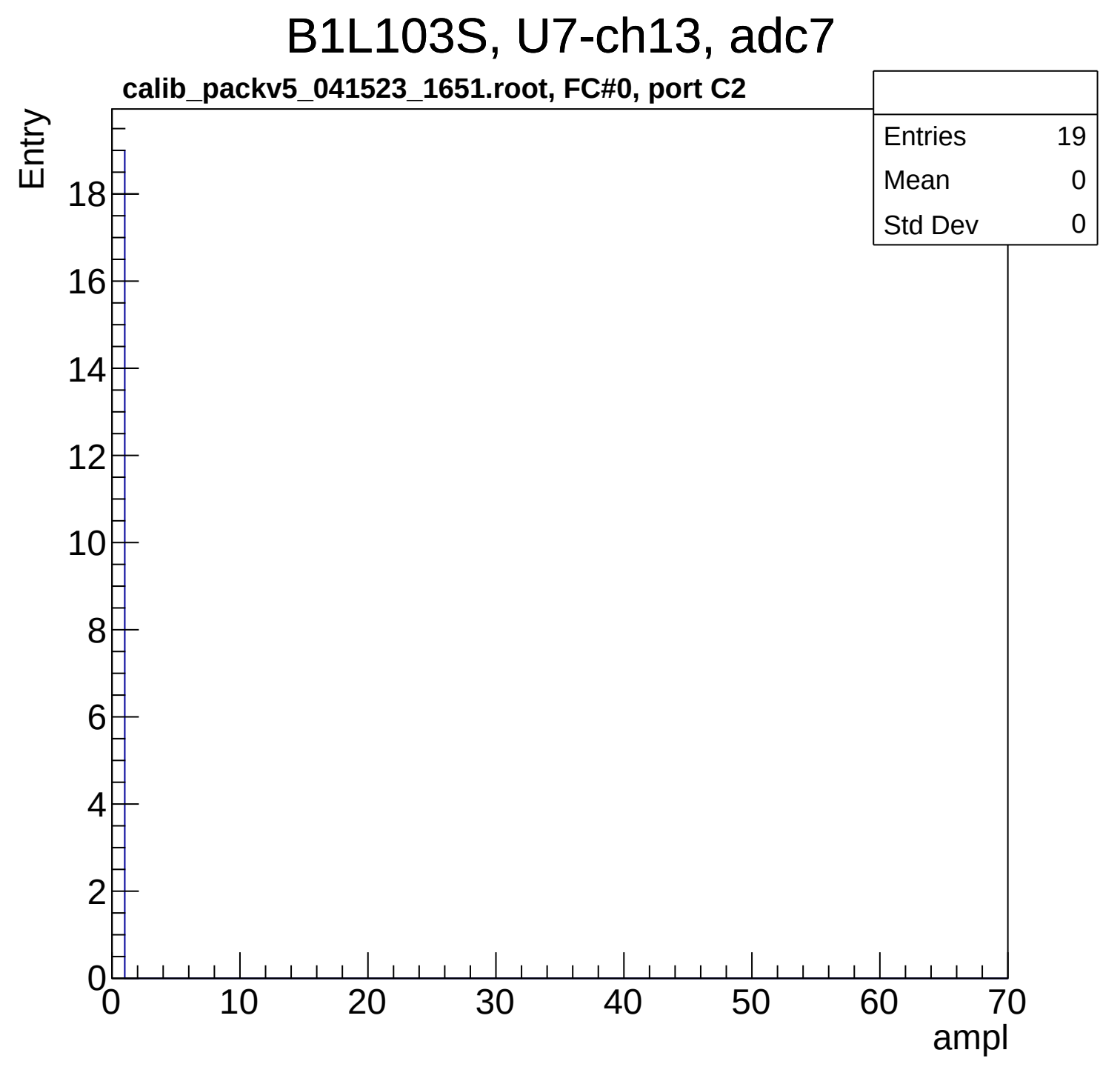
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U7-ch13, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
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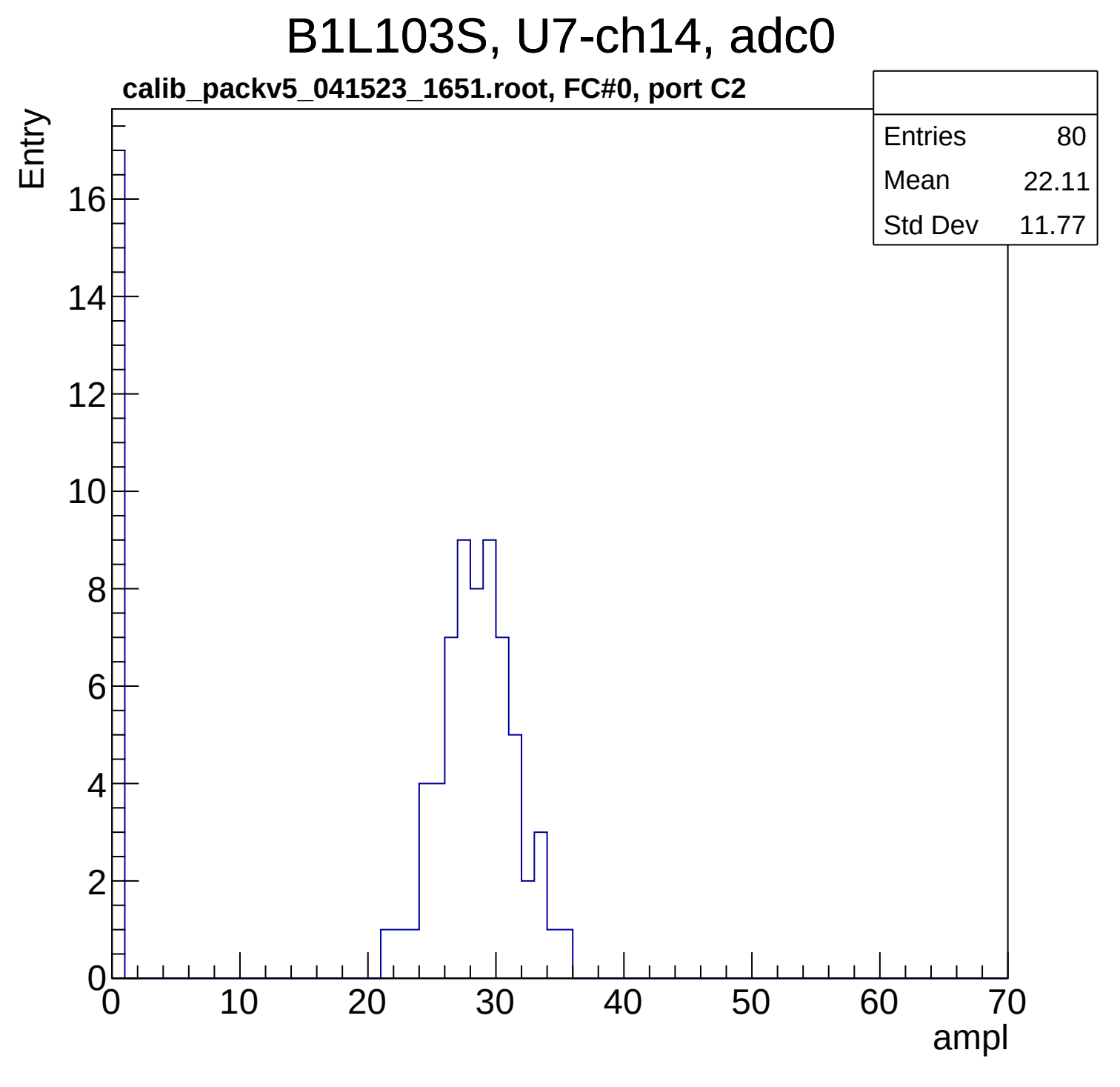
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch14, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 22.11
Std Dev 11.77
Entry
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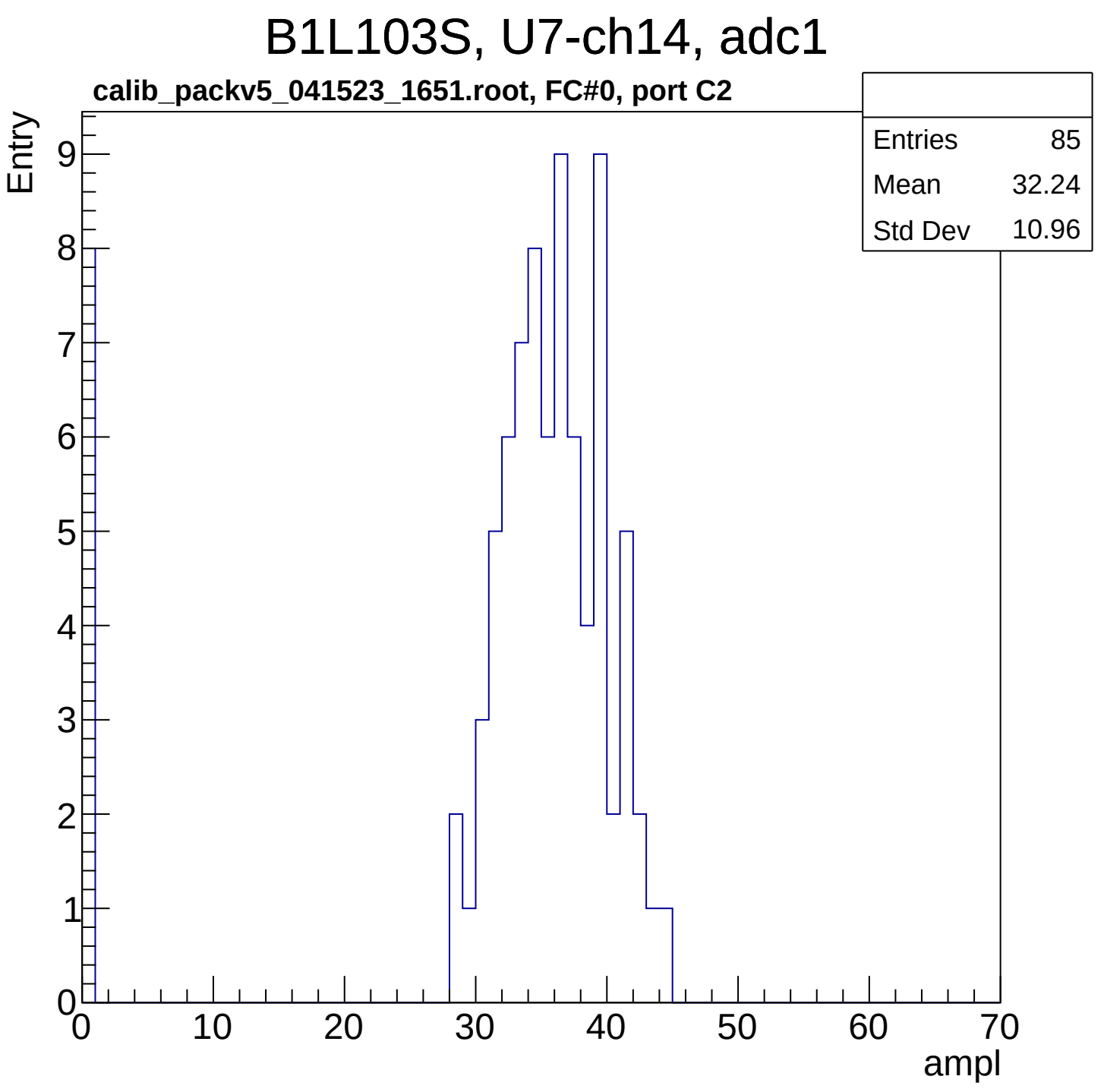
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch14, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 32.24
Std Dev 10.96
Entry
ampl
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4
5
6
7
8
9
0
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20
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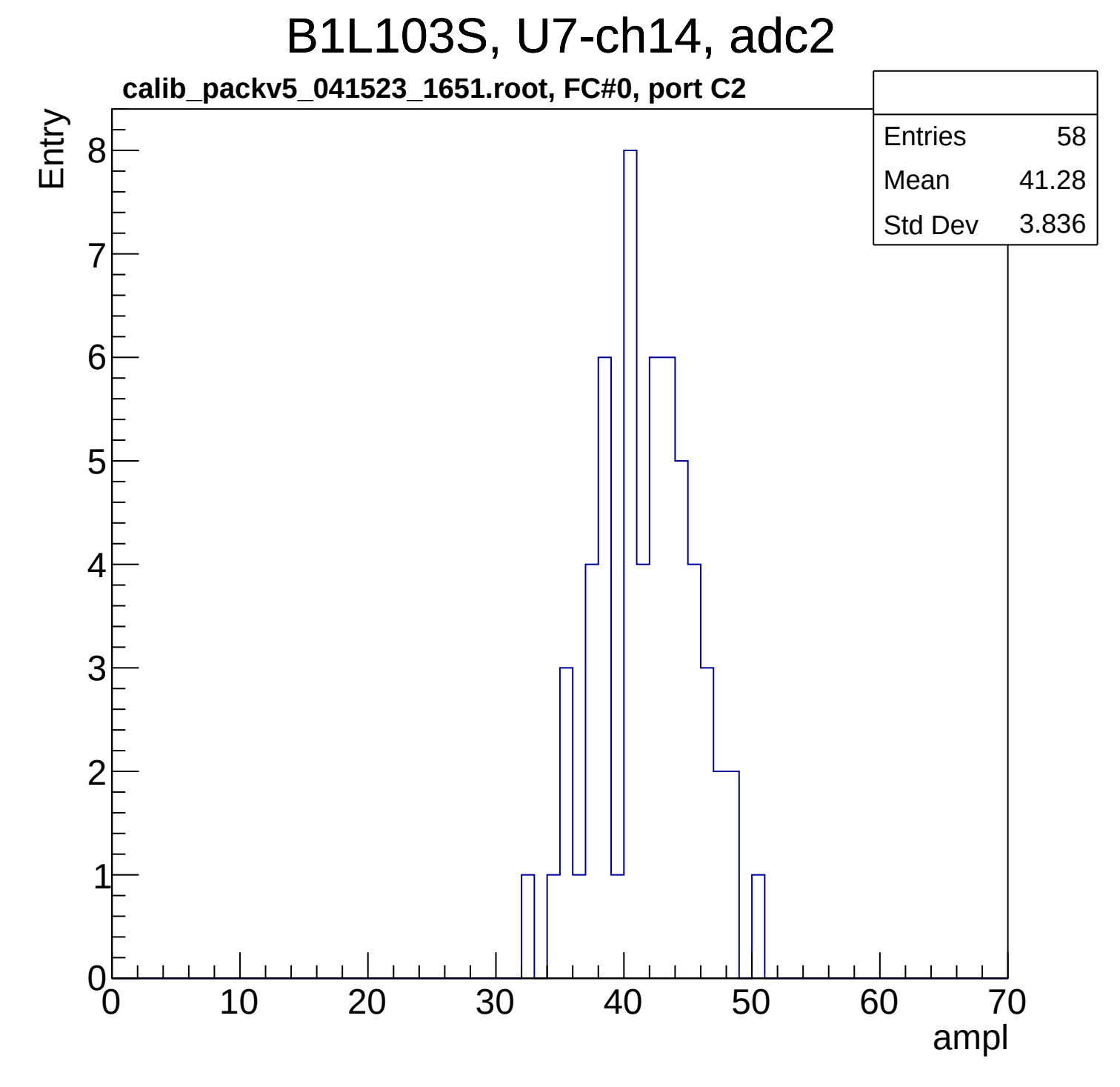
40
50
60
70


B1L103S, U7-ch14, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 41.28
Std Dev 3.836
Entry
ampl
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2
3
4
5
6
7
8
0
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20
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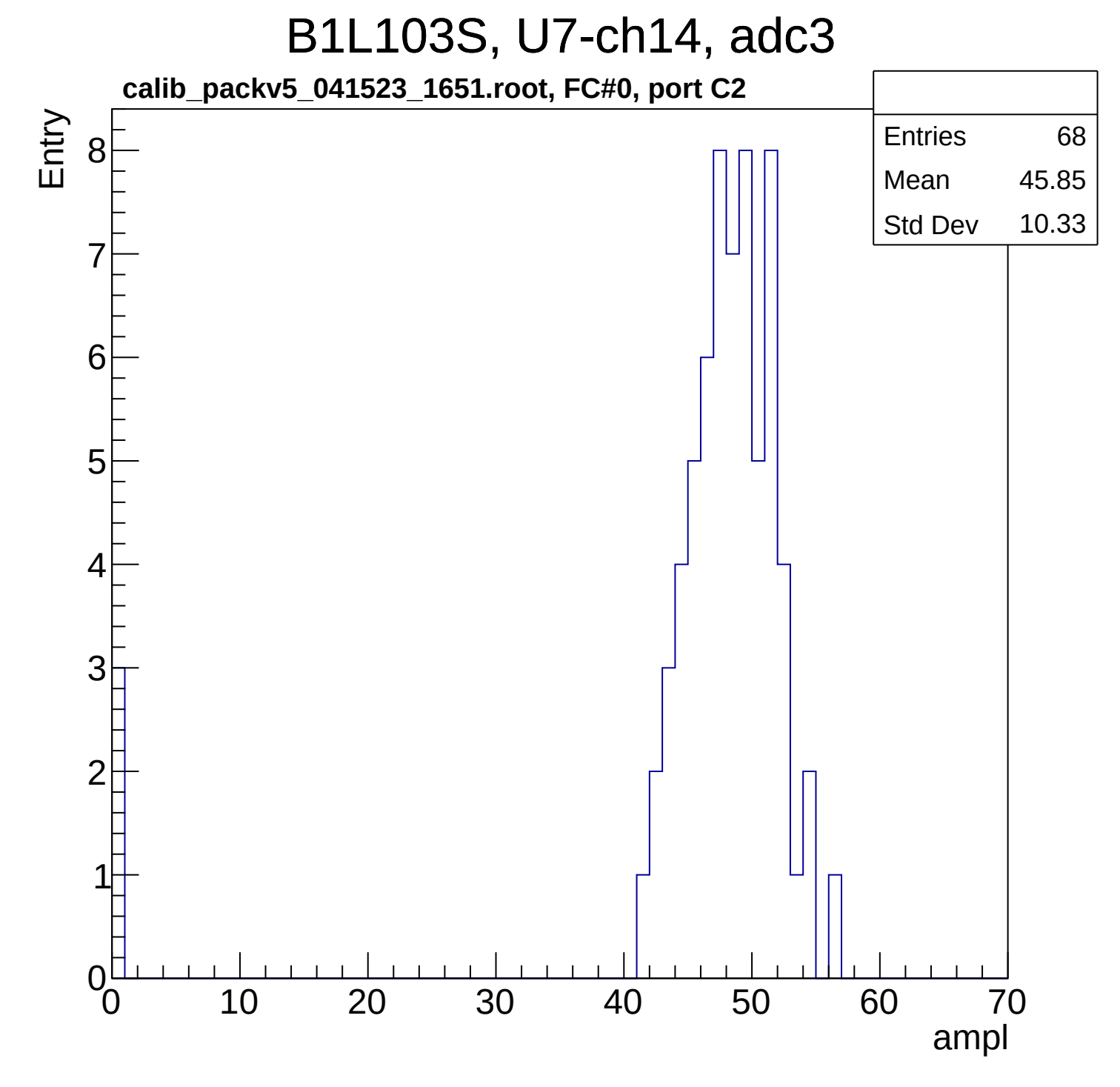
40
50
60
70


B1L103S, U7-ch14, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 45.85
Std Dev 10.33
Entry
ampl
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2
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4
5
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0
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60
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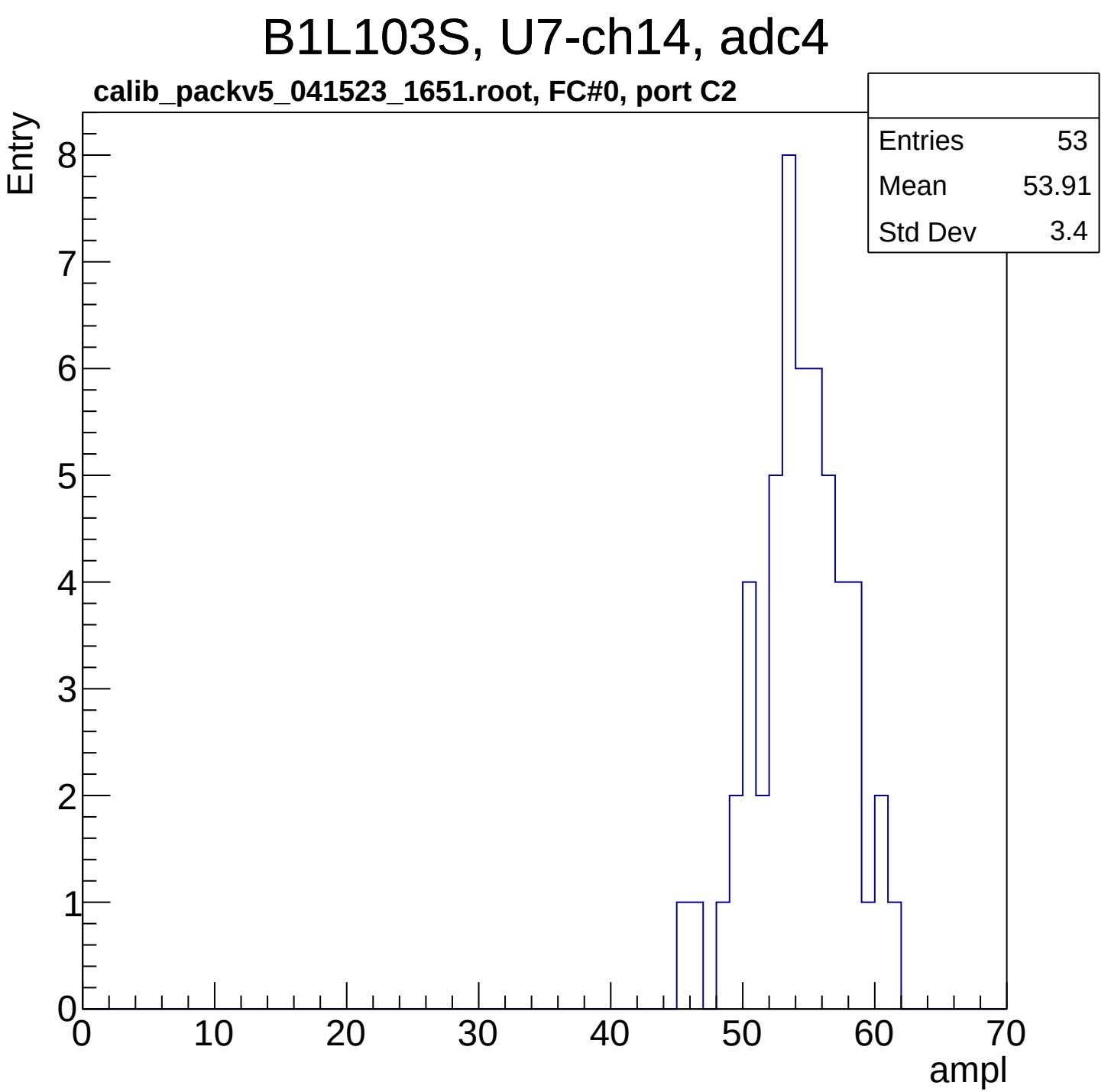
B1L103S, U7-ch14, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 53.91
Std Dev 3.4
Entry
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3
4
5
6
7
8
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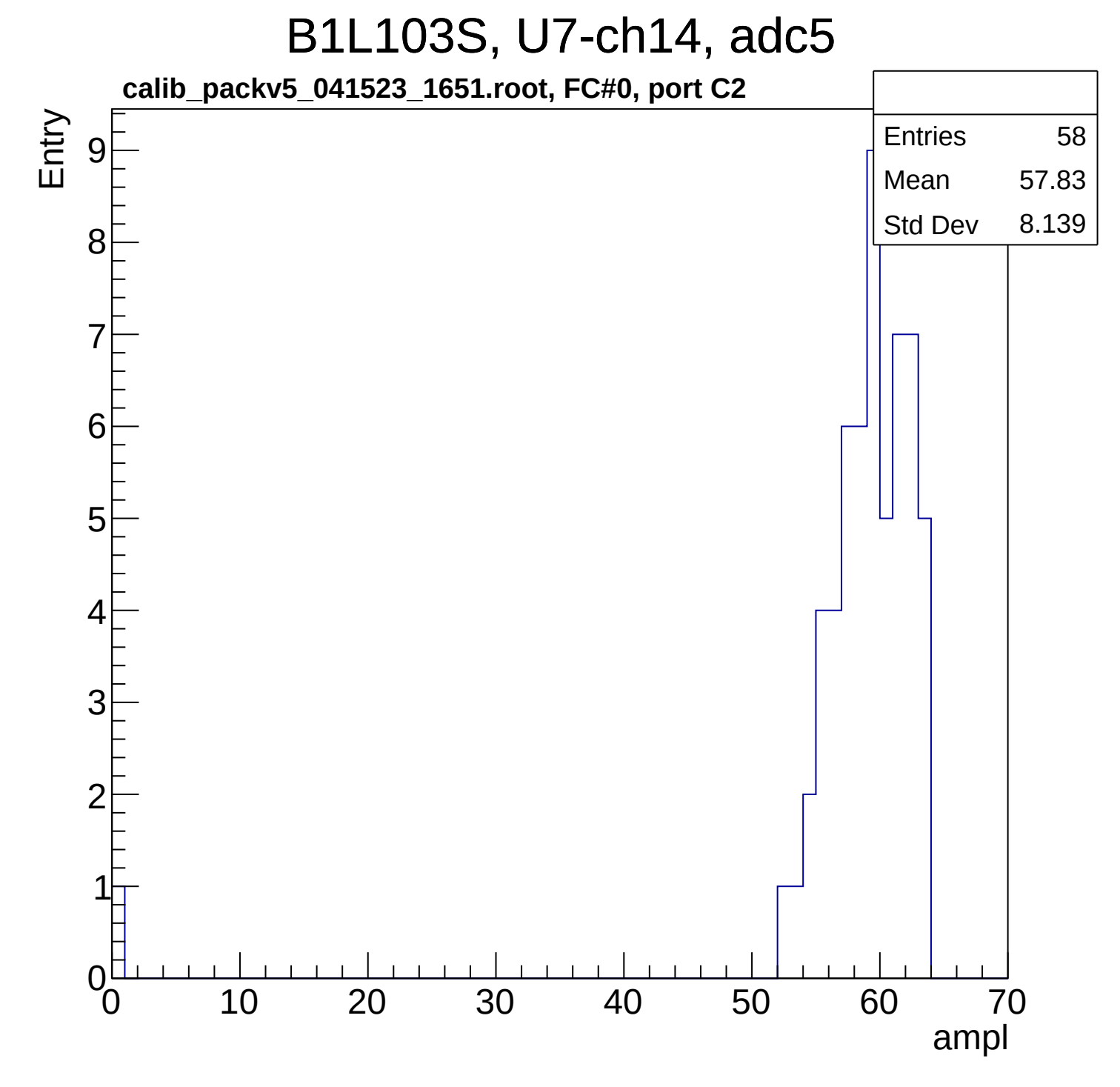
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch14, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 57.83
Std Dev 8.139
Entry
ampl
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3
4
5
6
7
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0
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60
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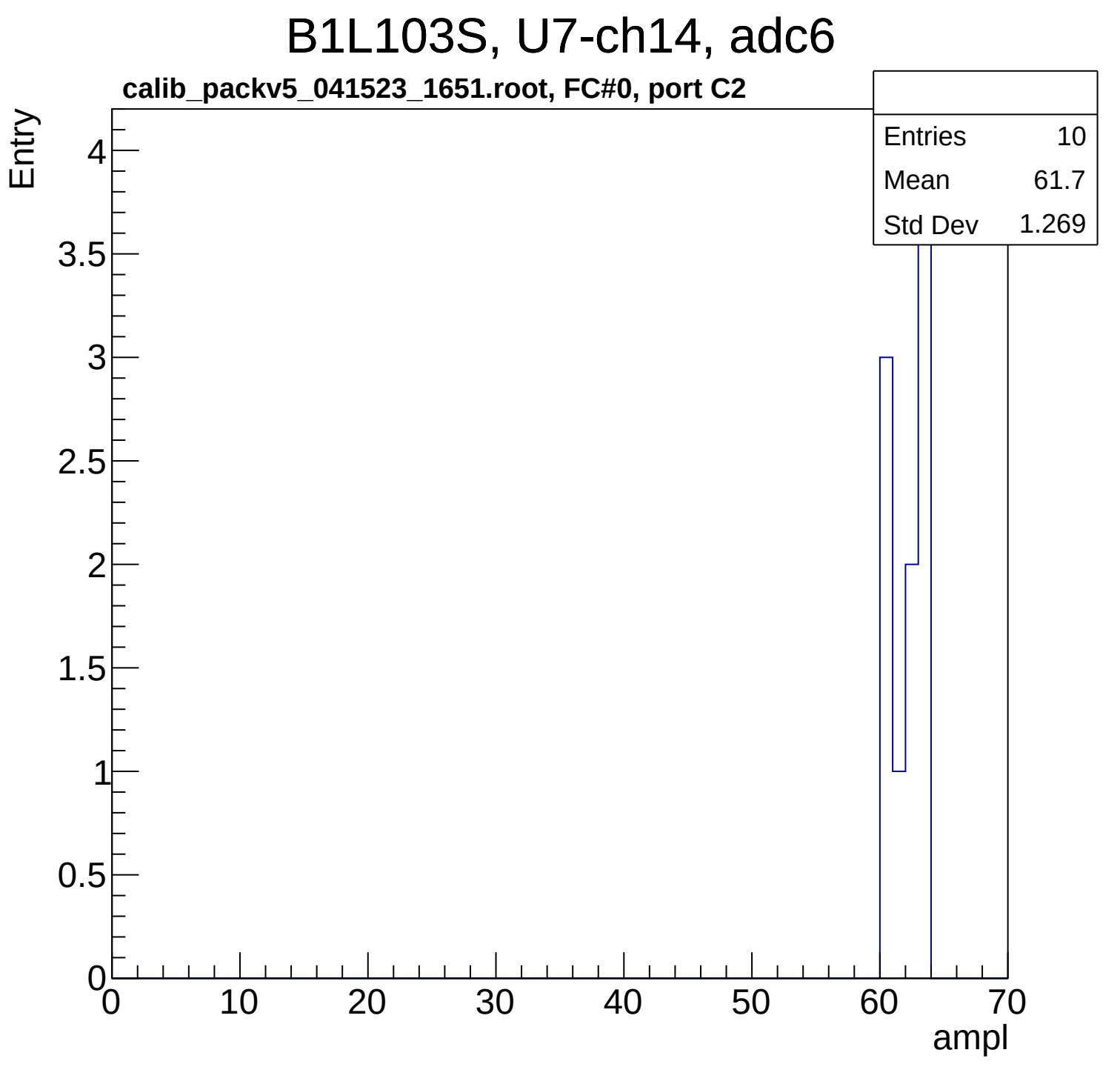
B1L103S, U7-ch14, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 61.7
Std Dev 1.269
Entry
ampl
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1.5
2
2.5
3
3.5
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0
10
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60
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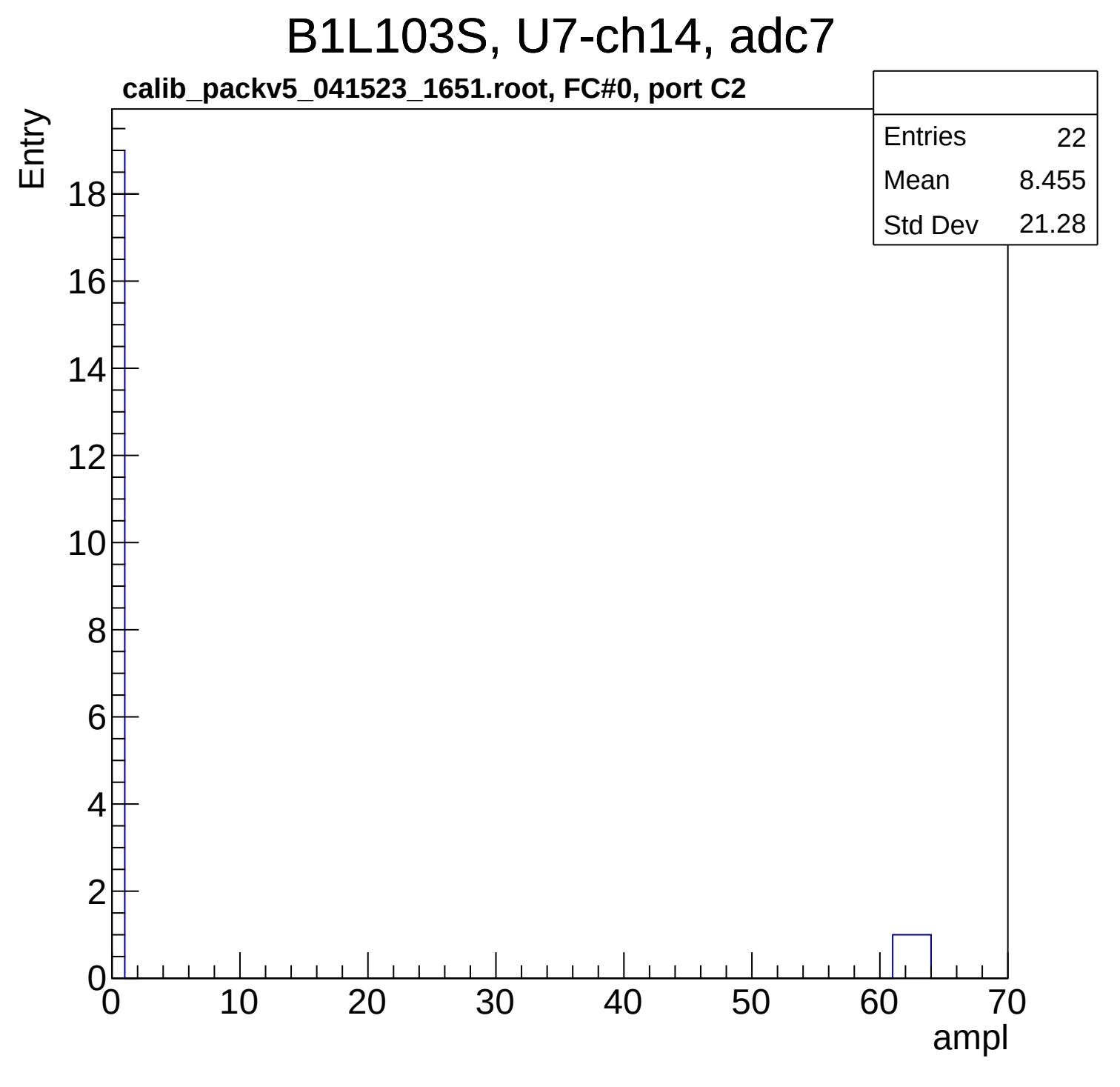
B1L103S, U7-ch14, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 8.455
Std Dev 21.28
Entry
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6
8
10
12
14
16
18
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10
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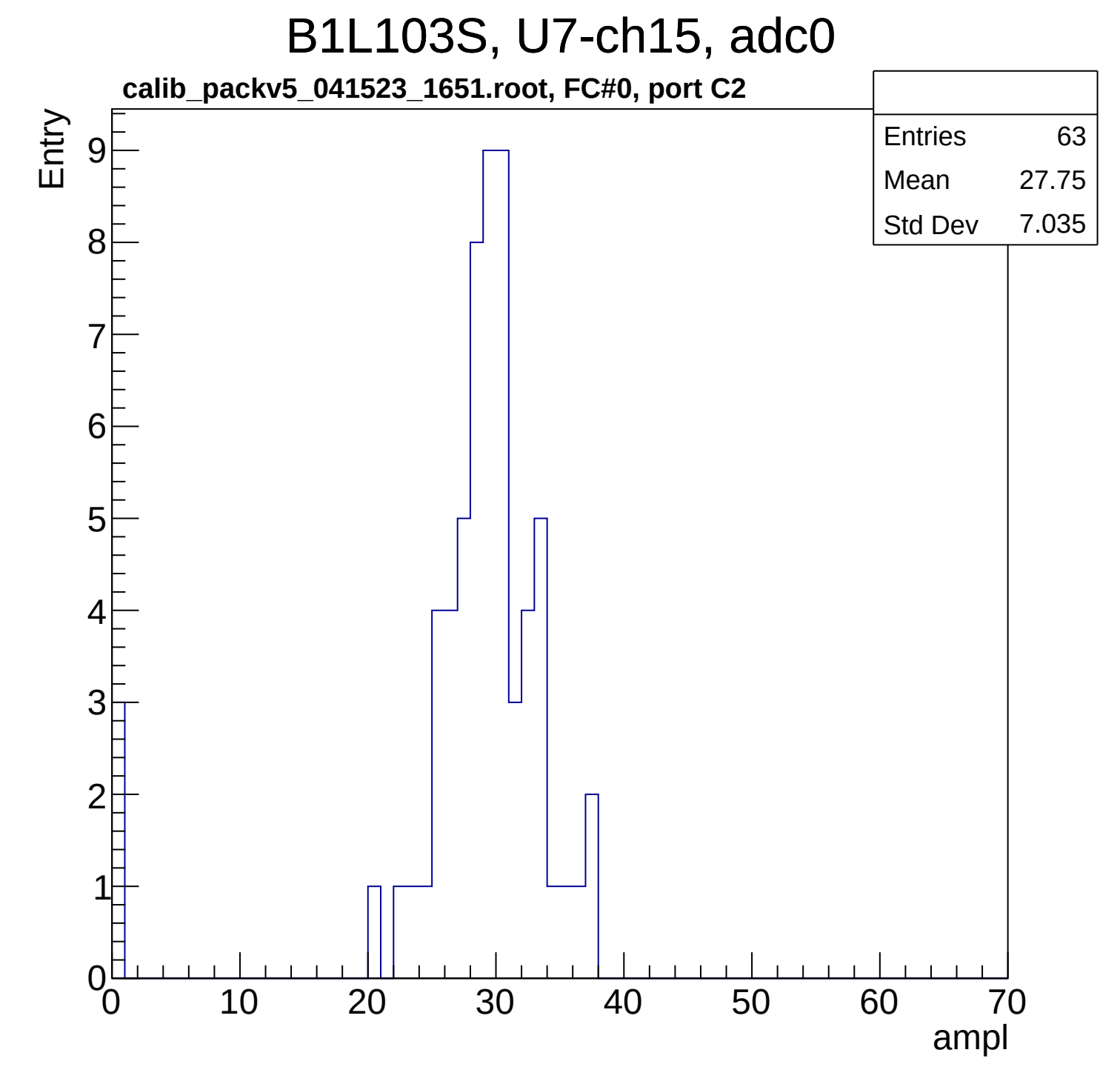
50
60
70
ampl


B1L103S, U7-ch15, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 27.75
Std Dev 7.035
Entry
ampl
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4
5
6
7
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0
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60
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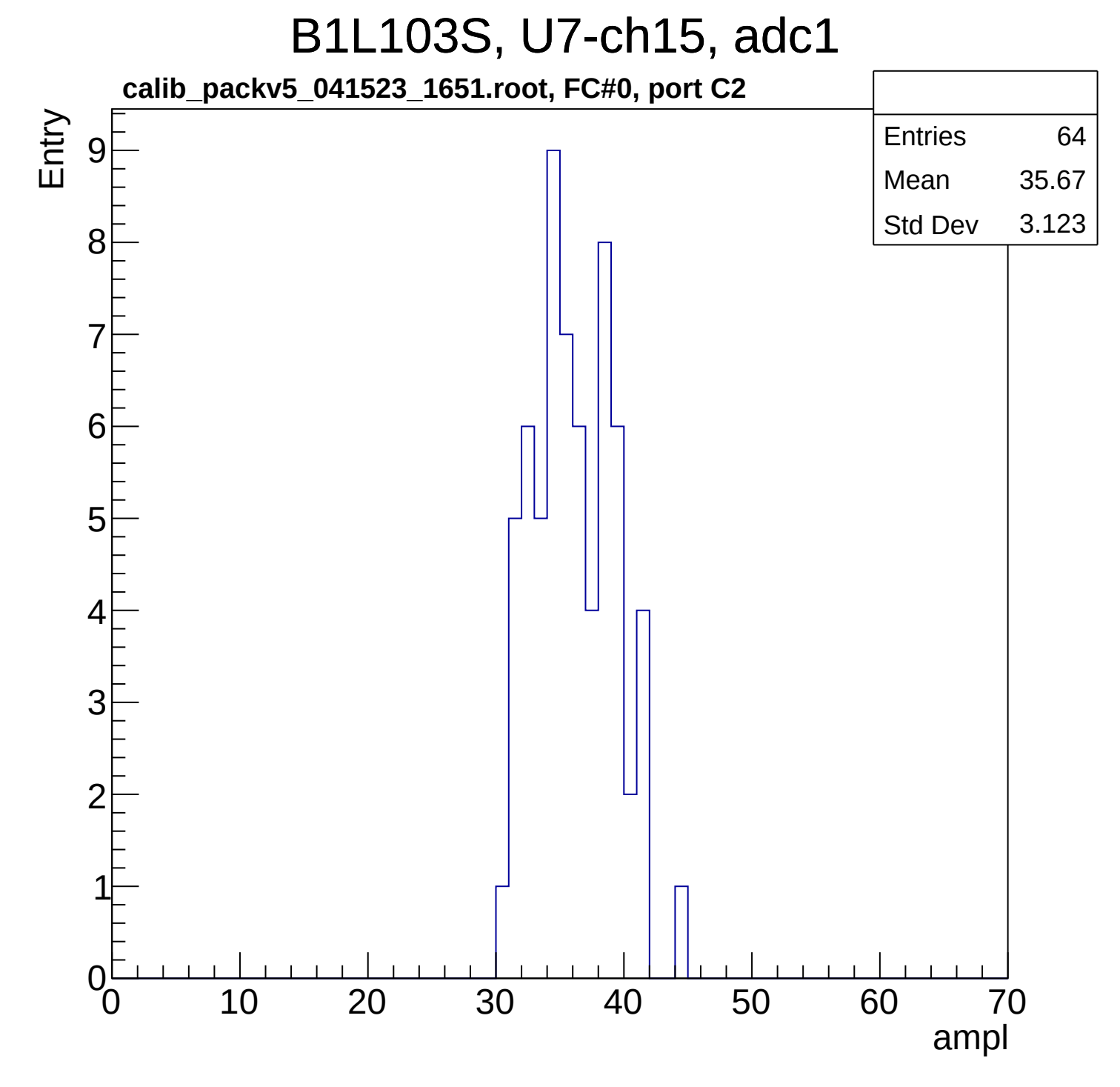
B1L103S, U7-ch15, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 35.67
Std Dev 3.123
Entry
ampl
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3
4
5
6
7
8
9
0
10
20
30
40
50
60
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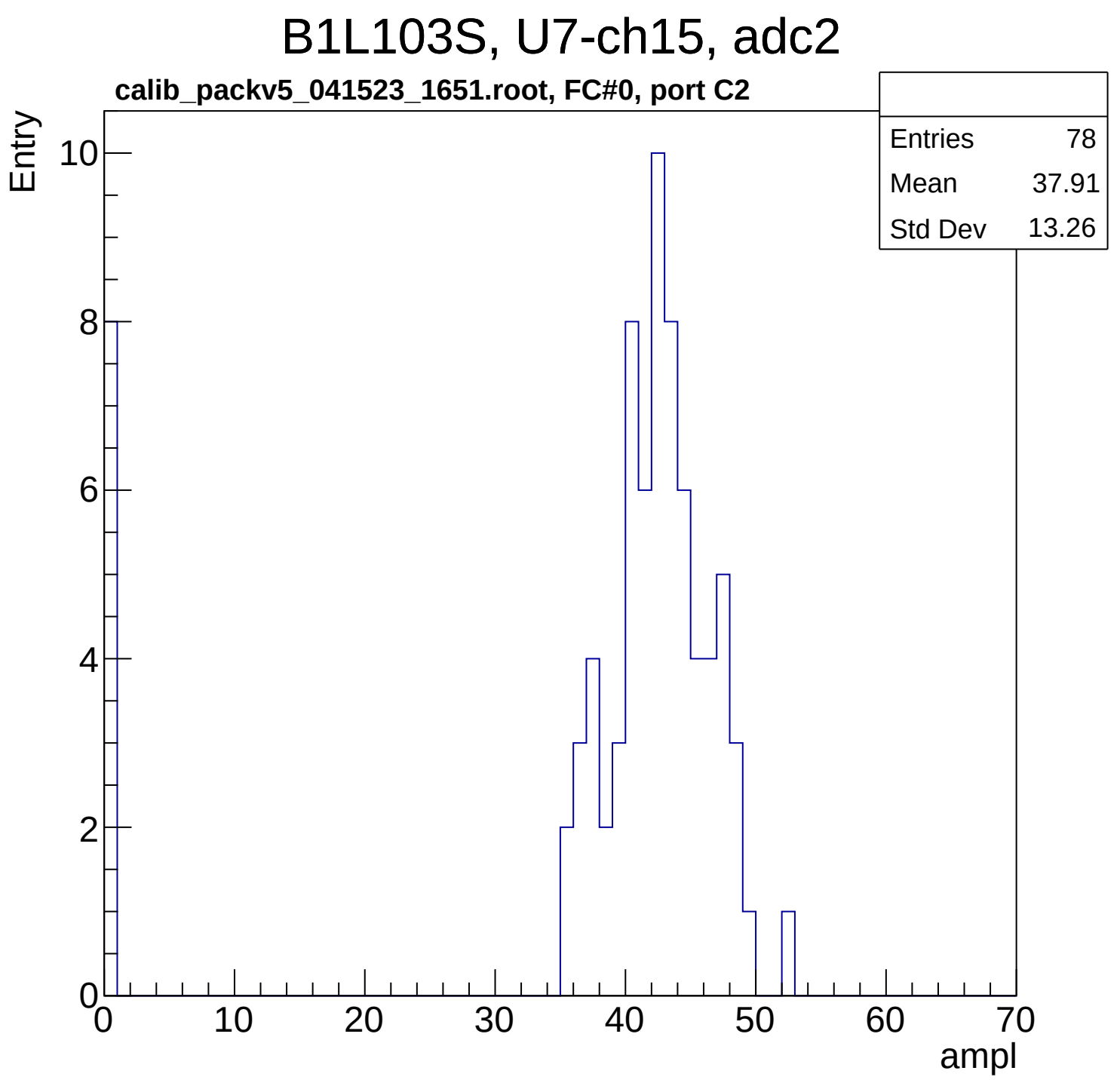
B1L103S, U7-ch15, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 37.91
Std Dev 13.26
Entry
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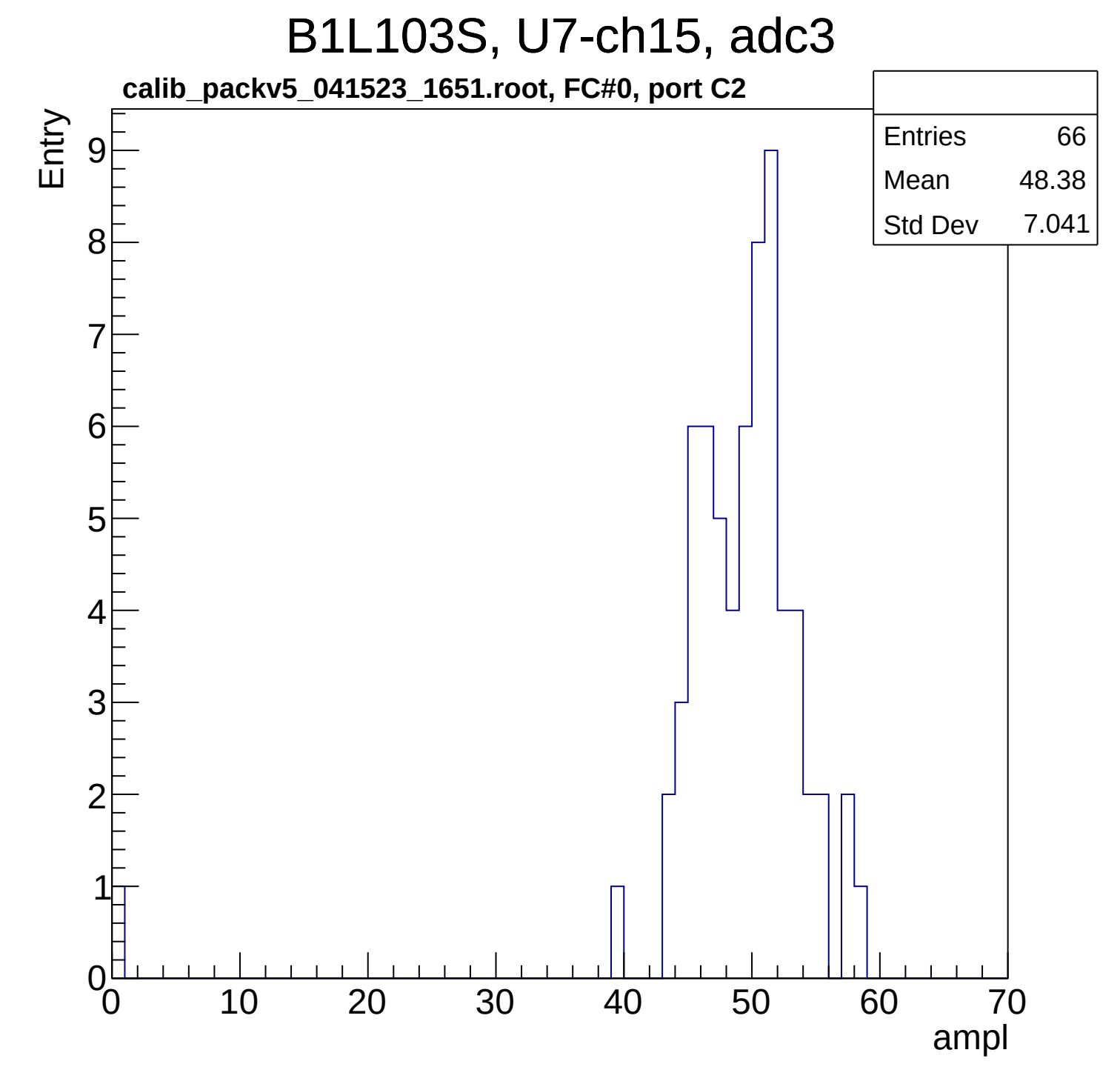
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch15, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 48.38
Std Dev 7.041
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
50
60
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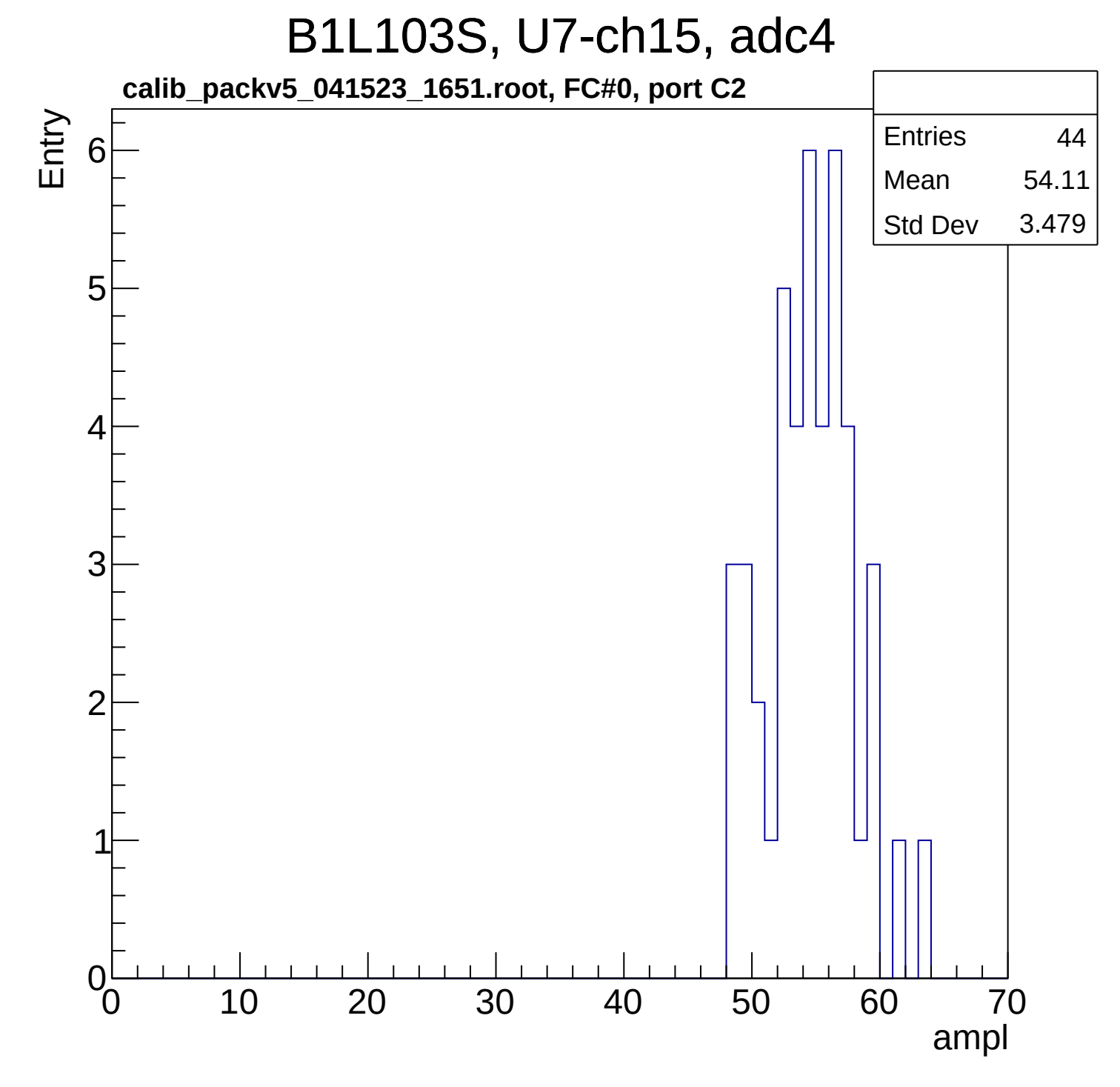
B1L103S, U7-ch15, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 54.11
Std Dev 3.479
Entry
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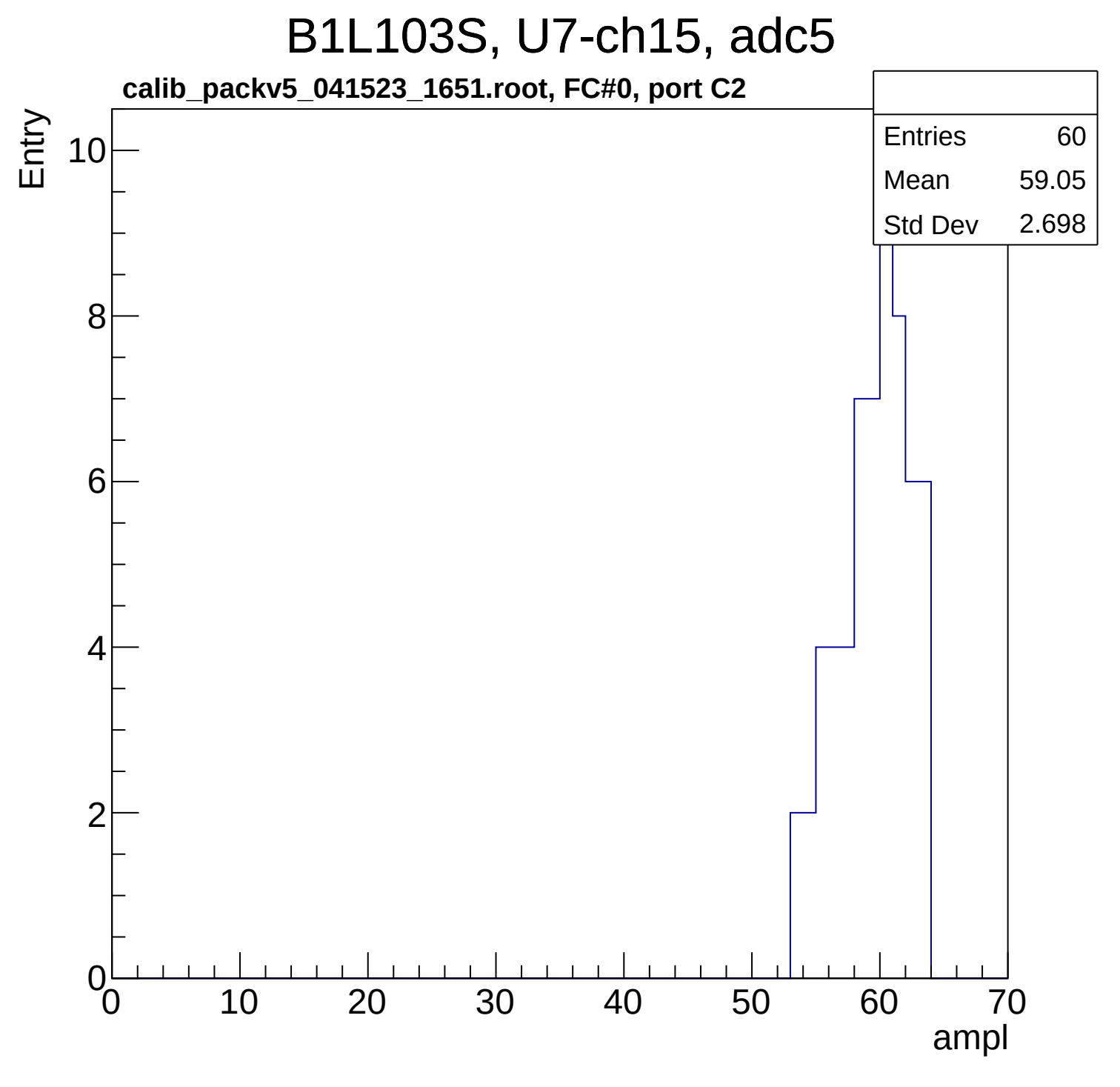
70
ampl


B1L103S, U7-ch15, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 59.05
Std Dev 2.698
Entry
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4
6
8
10
0
10
20
30
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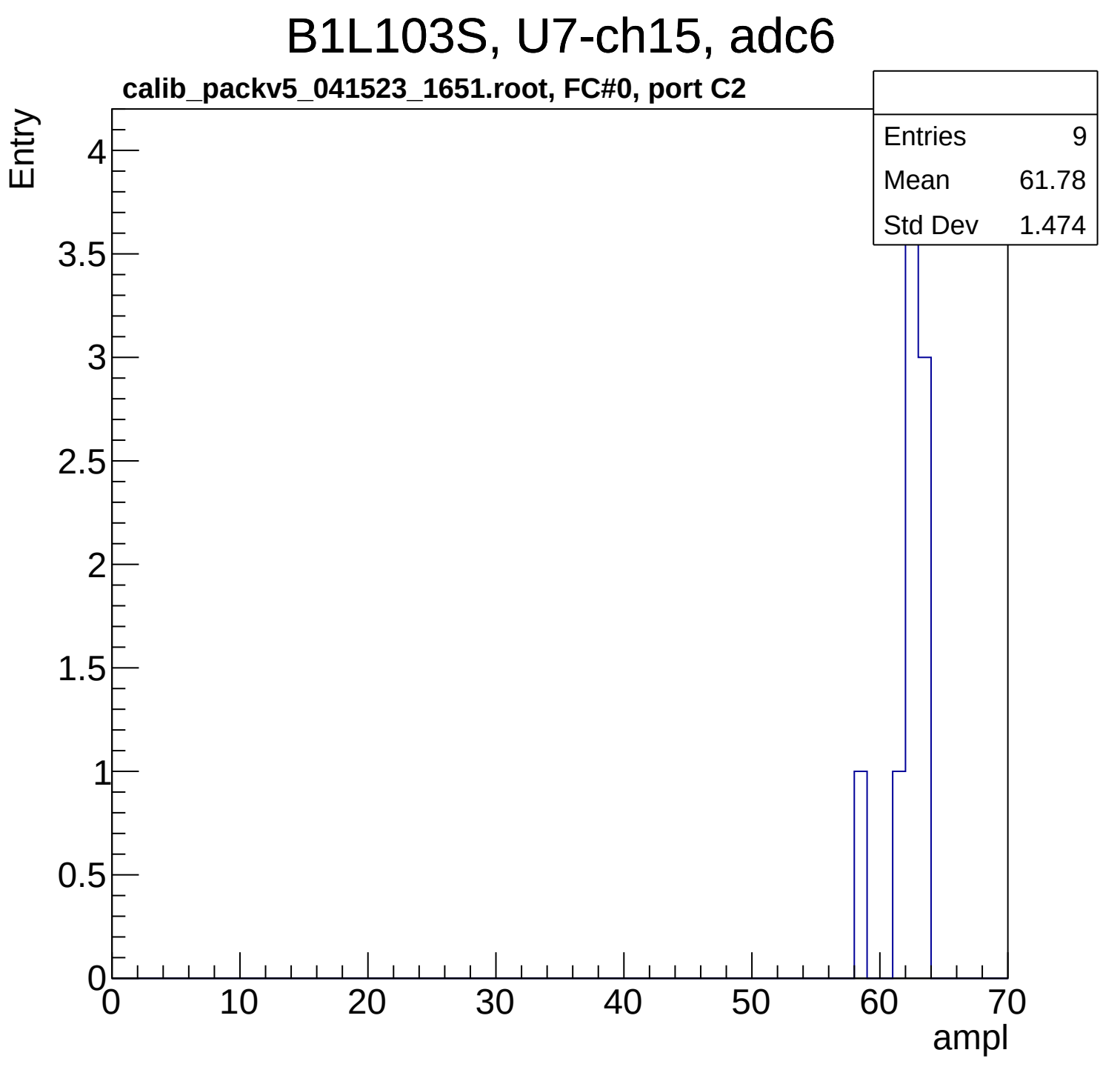
50
60
70
ampl


B1L103S, U7-ch15, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 9
Mean 61.78
Std Dev 1.474
Entry
ampl
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1.5
2
2.5
3
3.5
4
0
10
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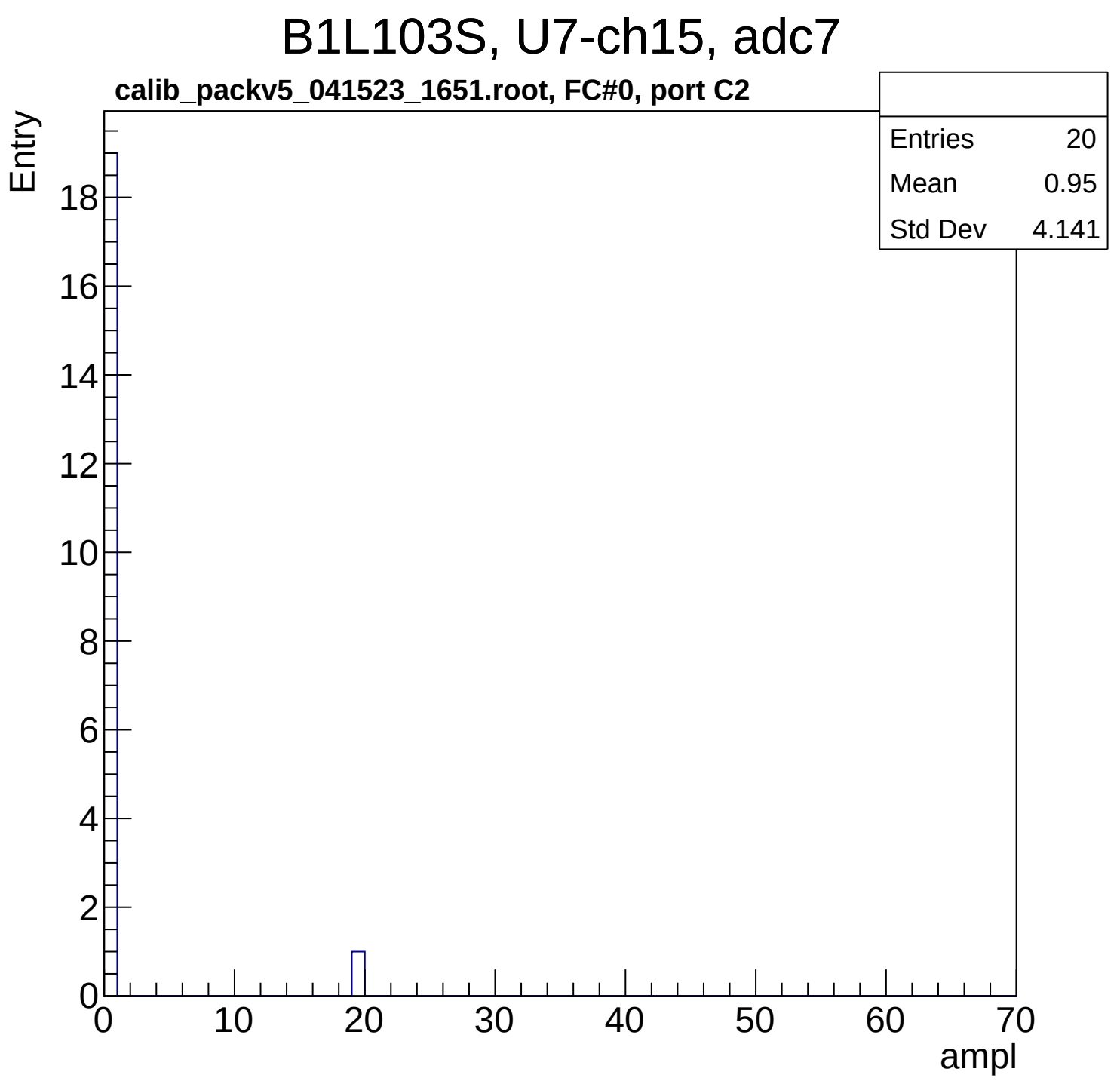
40
50
60
70


B1L103S, U7-ch15, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 0.95
Std Dev 4.141
Entry
0
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6
8
10
12
14
16
18
0
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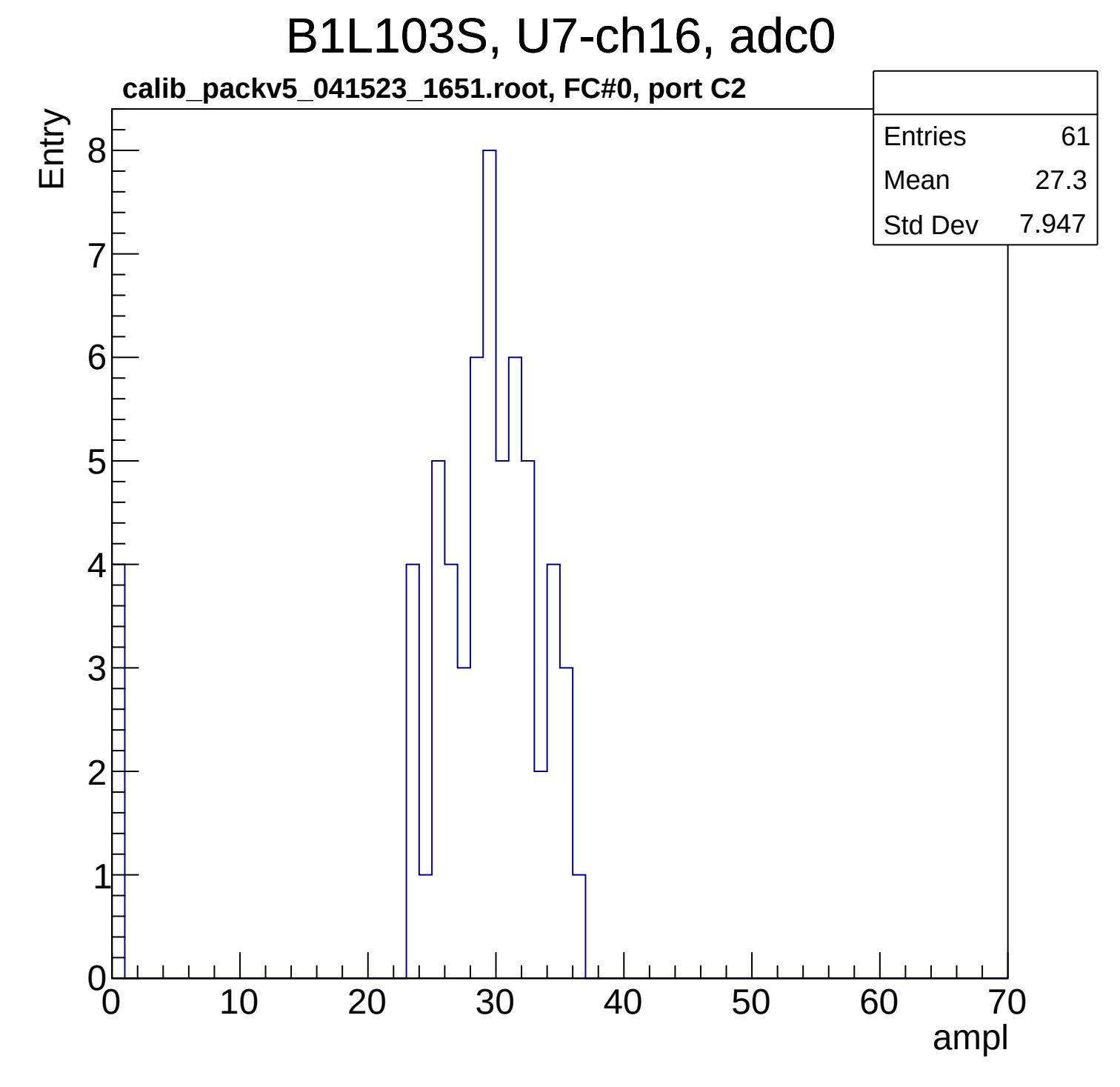
70
ampl


B1L103S, U7-ch16, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 27.3
Std Dev 7.947
Entry
ampl
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2
3
4
5
6
7
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0
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40
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60
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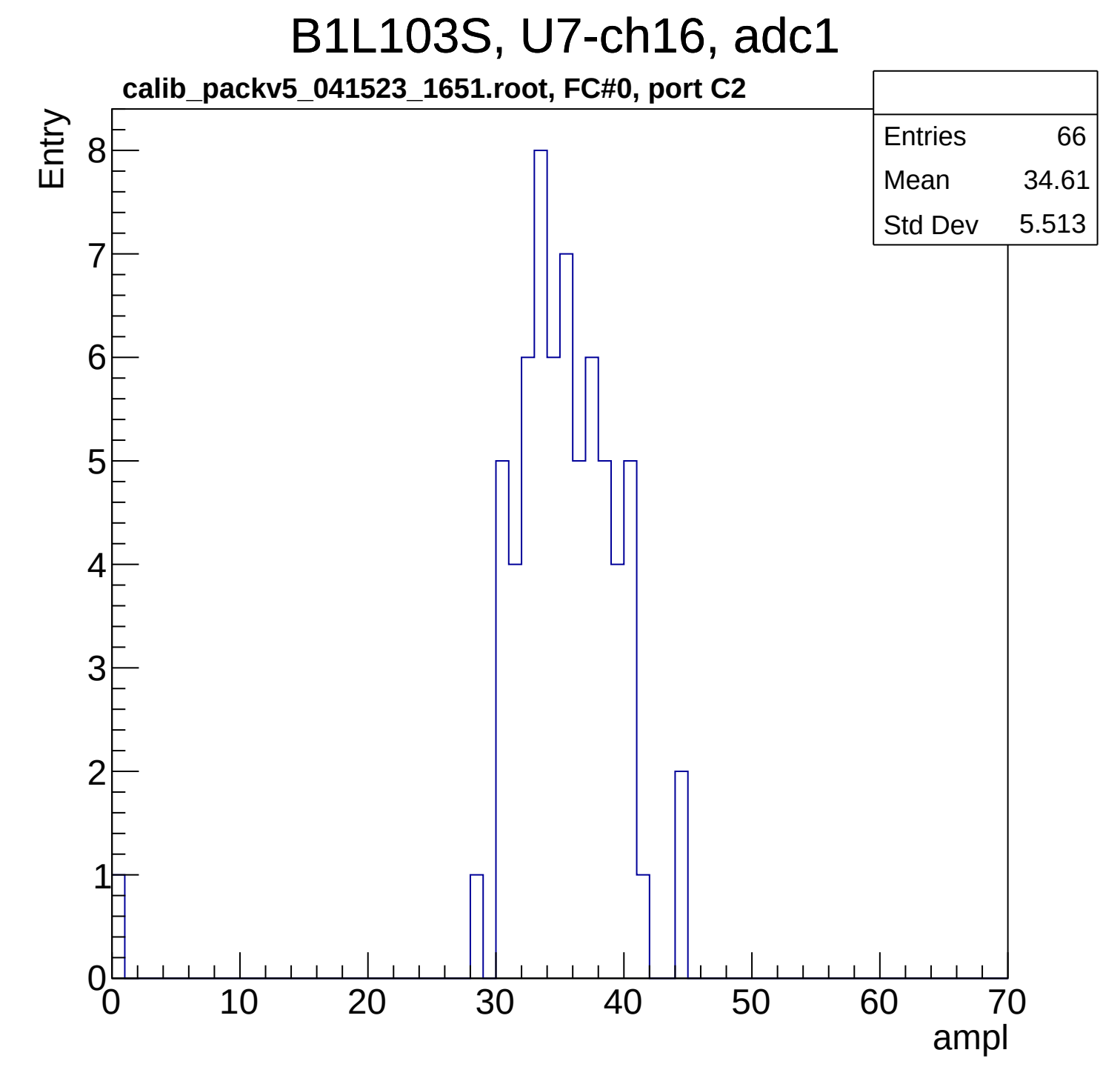
B1L103S, U7-ch16, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 34.61
Std Dev 5.513
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
30
40
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60
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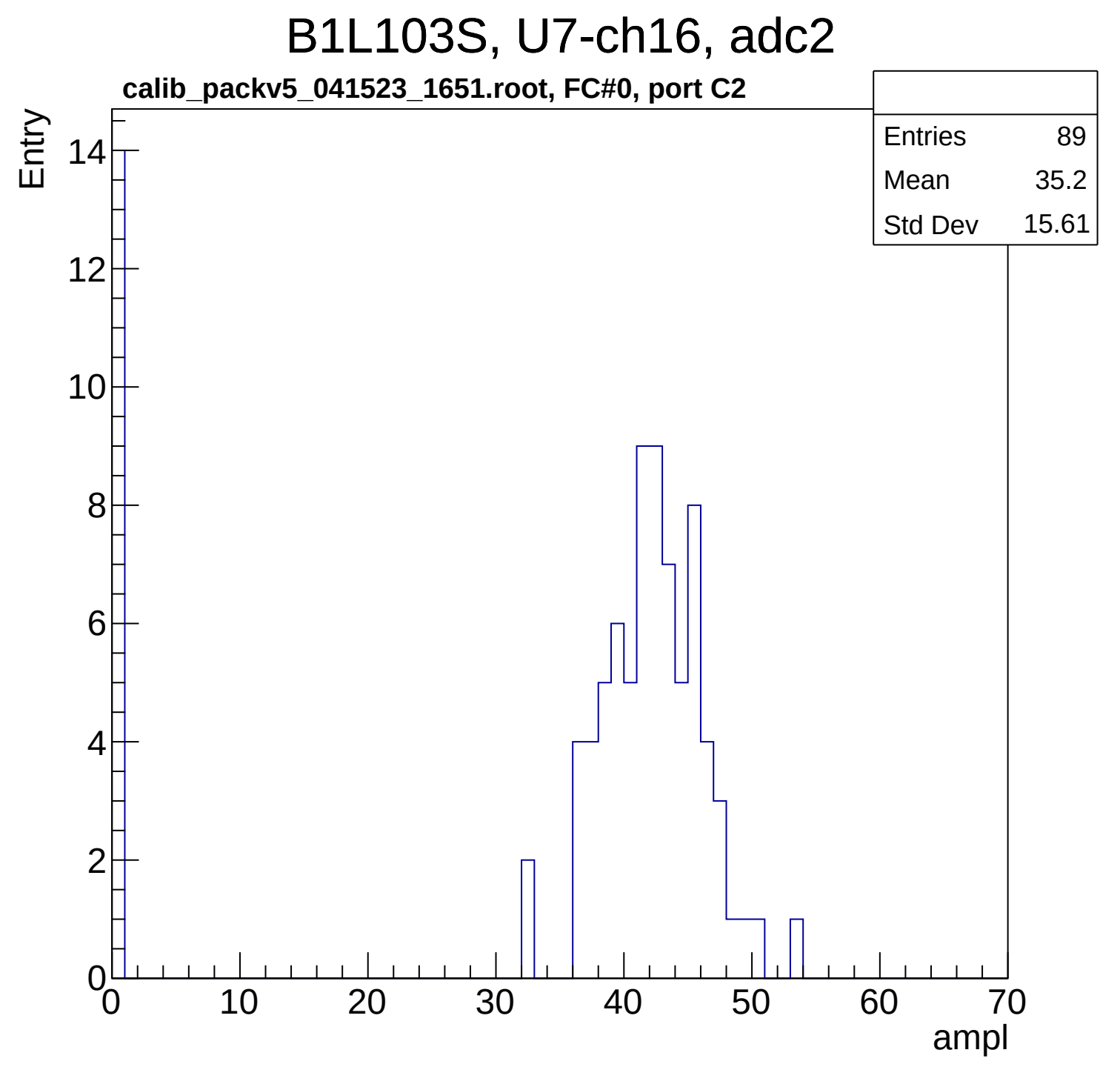
B1L103S, U7-ch16, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 89
Mean 35.2
Std Dev 15.61
Entry
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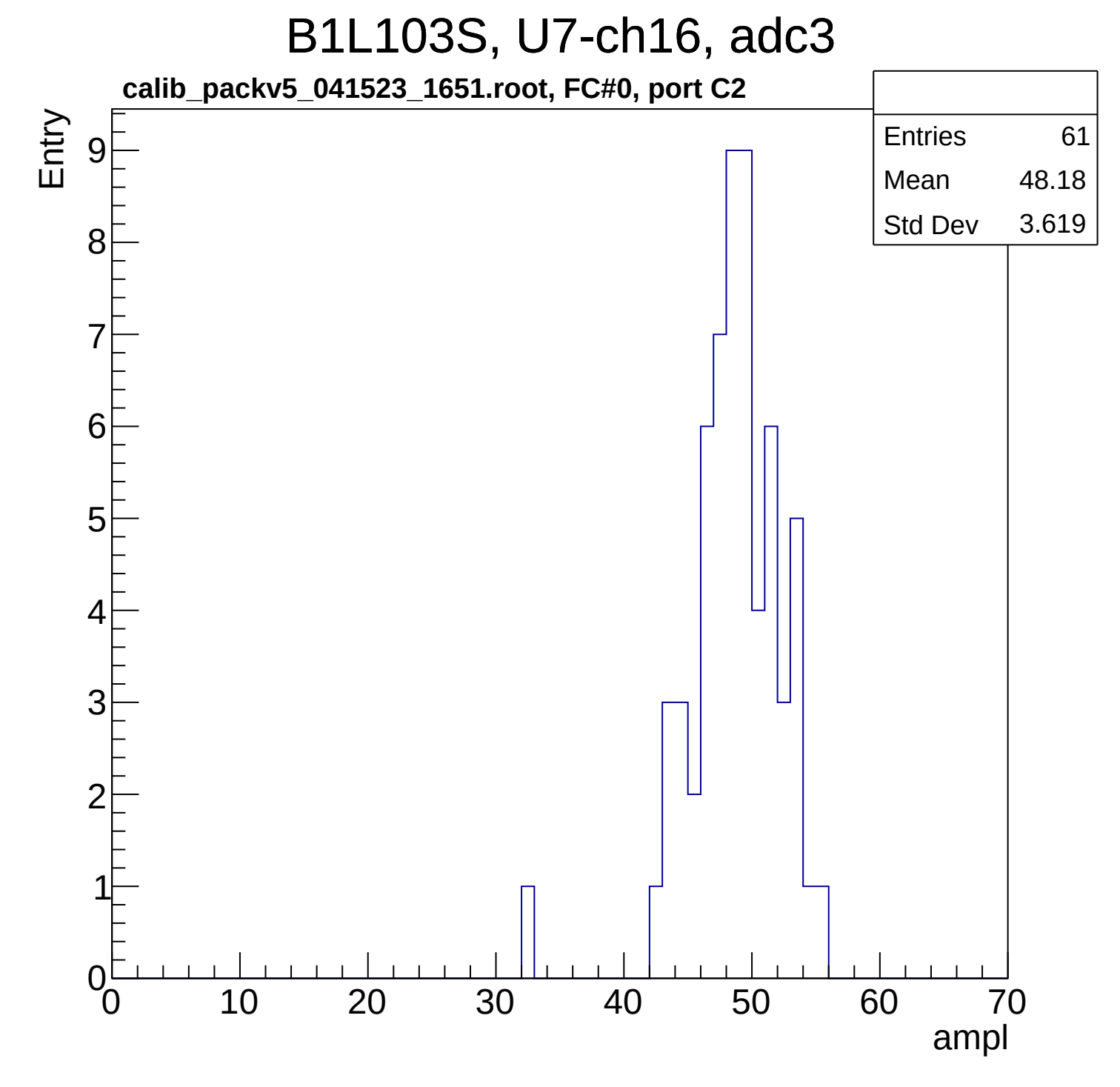
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch16, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 48.18
Std Dev 3.619
Entry
ampl
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3
4
5
6
7
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9
0
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20
30
40
50
60
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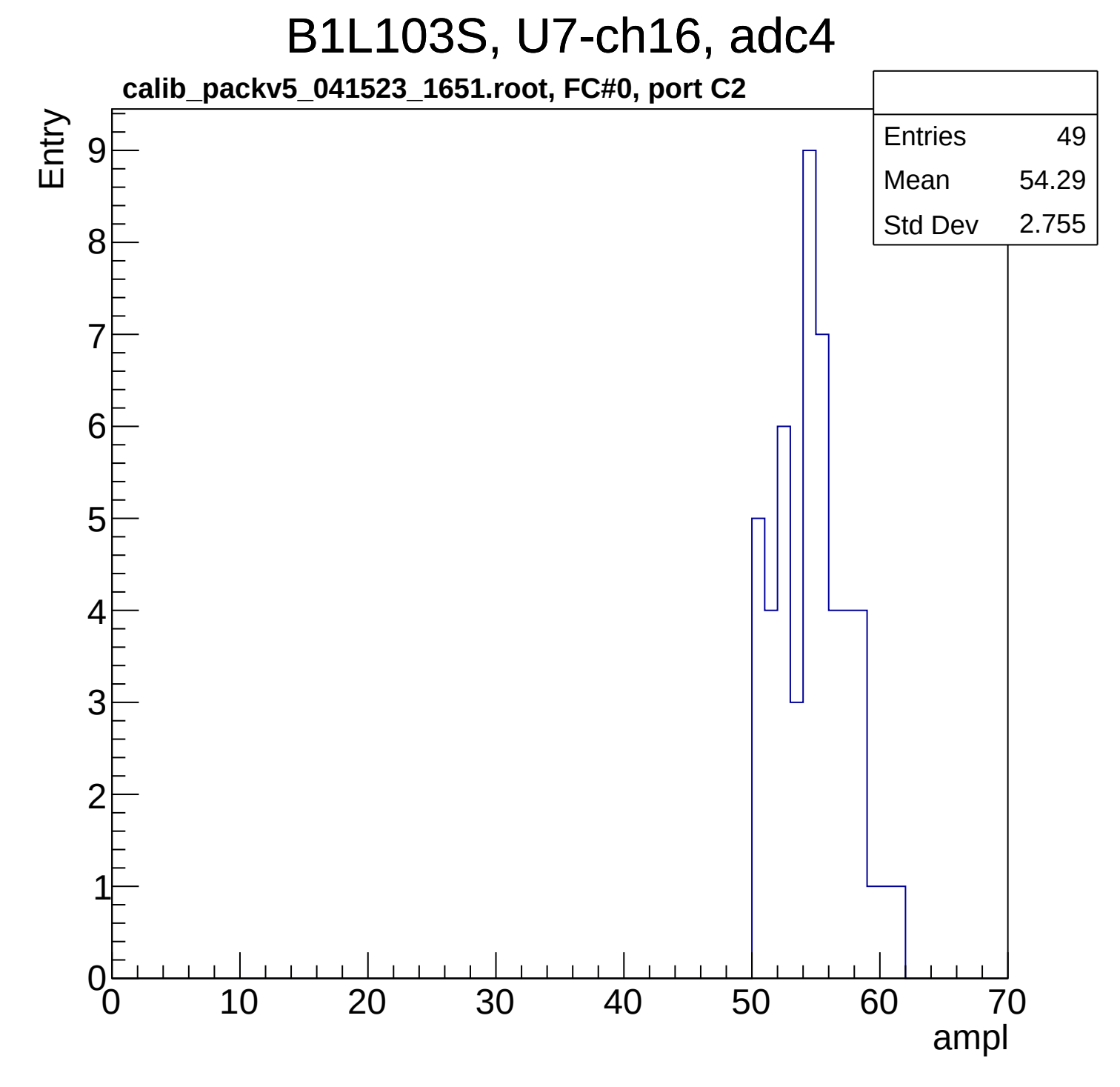
B1L103S, U7-ch16, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 54.29
Std Dev 2.755
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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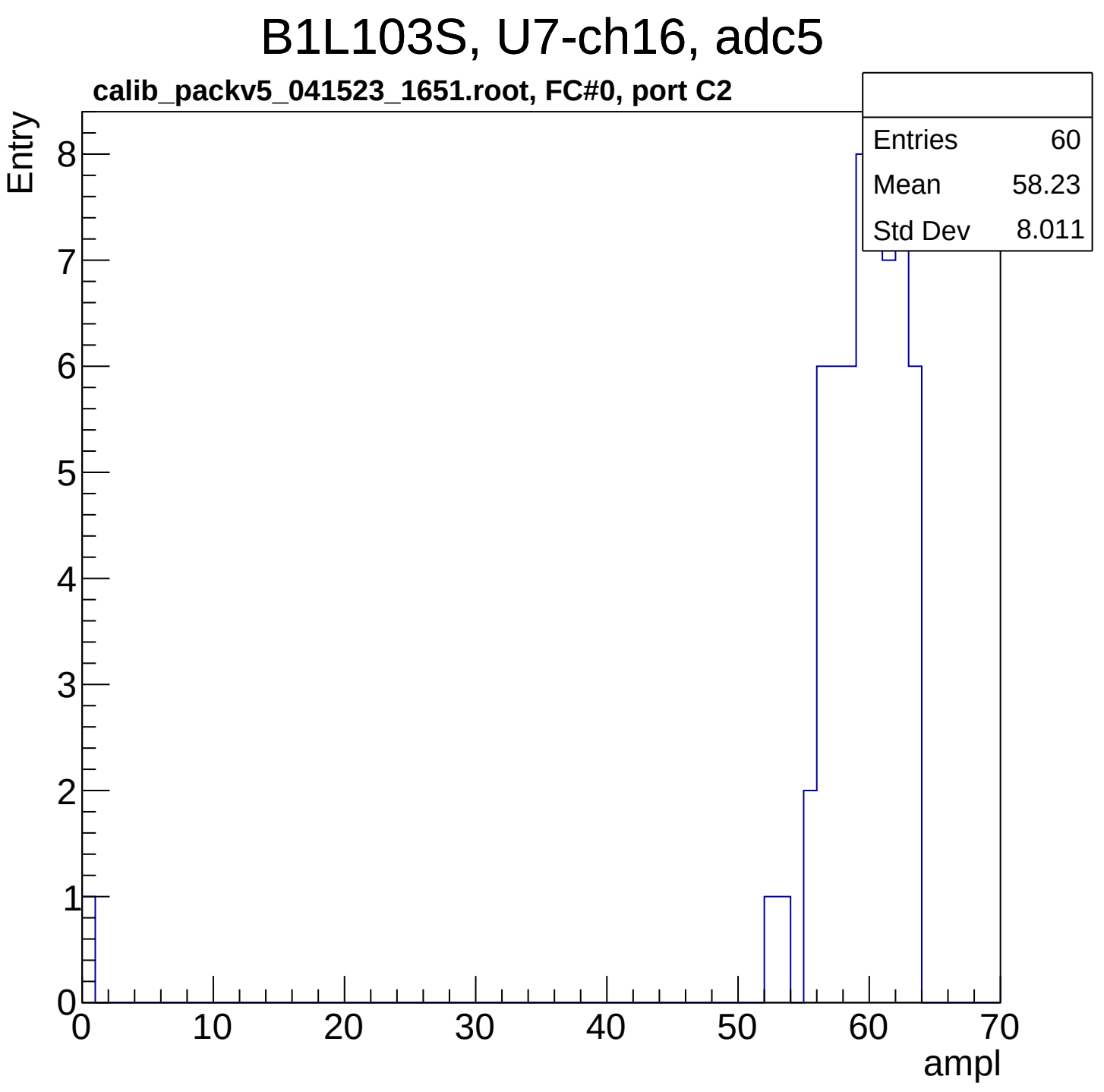
B1L103S, U7-ch16, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 58.23
Std Dev 8.011
Entry
ampl
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2
3
4
5
6
7
8
0
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40
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60
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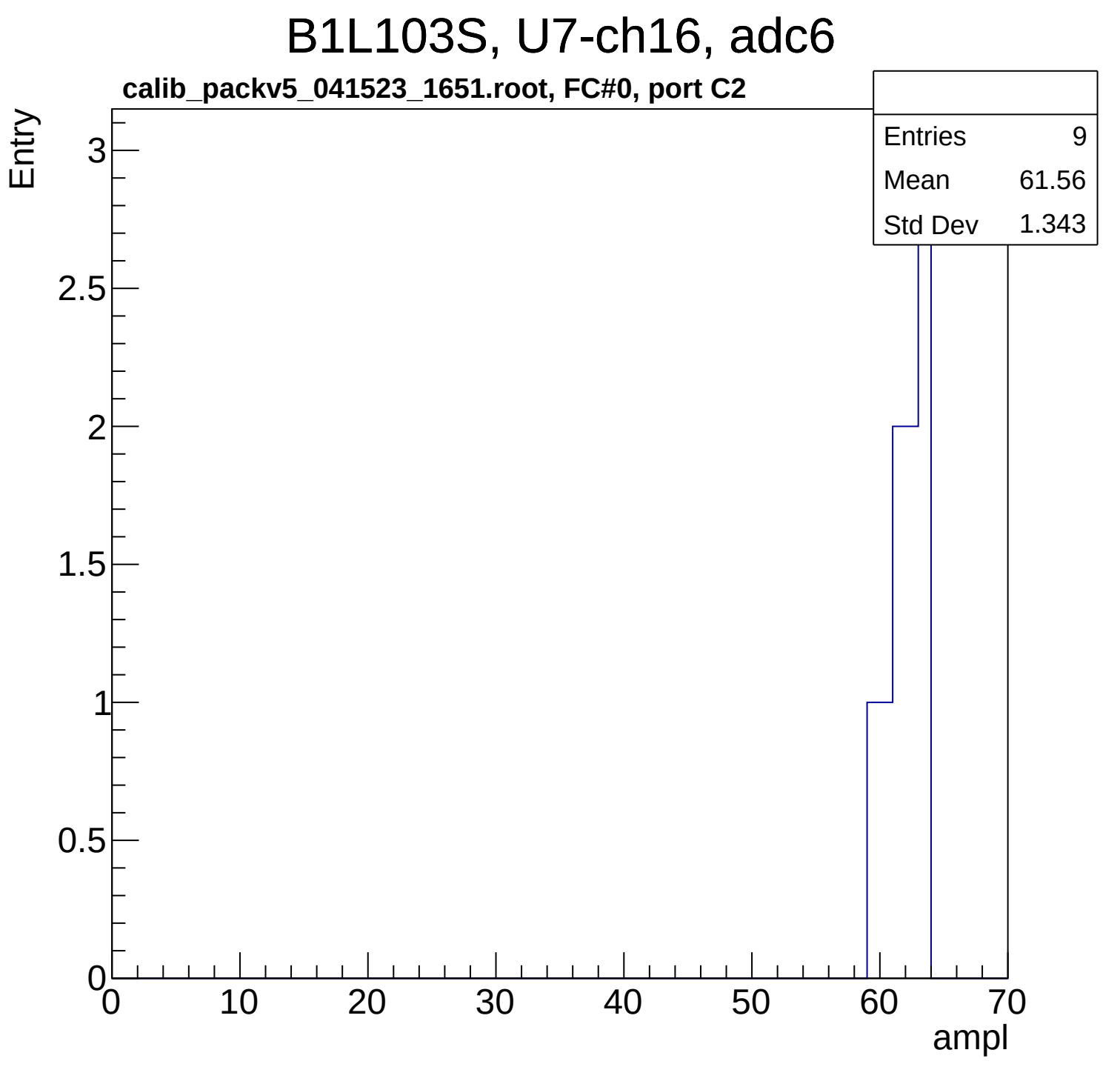
B1L103S, U7-ch16, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 9
Mean 61.56
Std Dev 1.343
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
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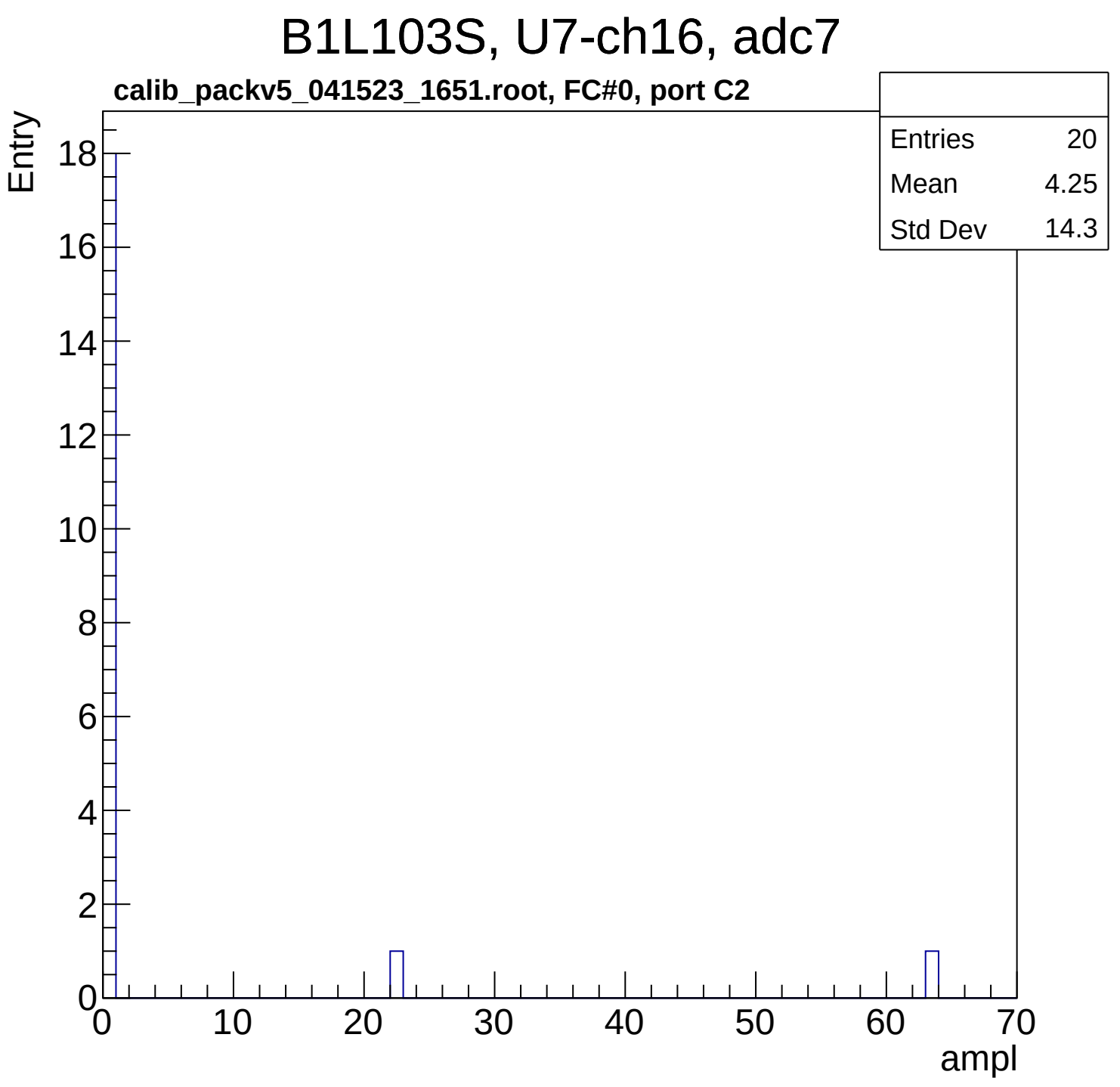
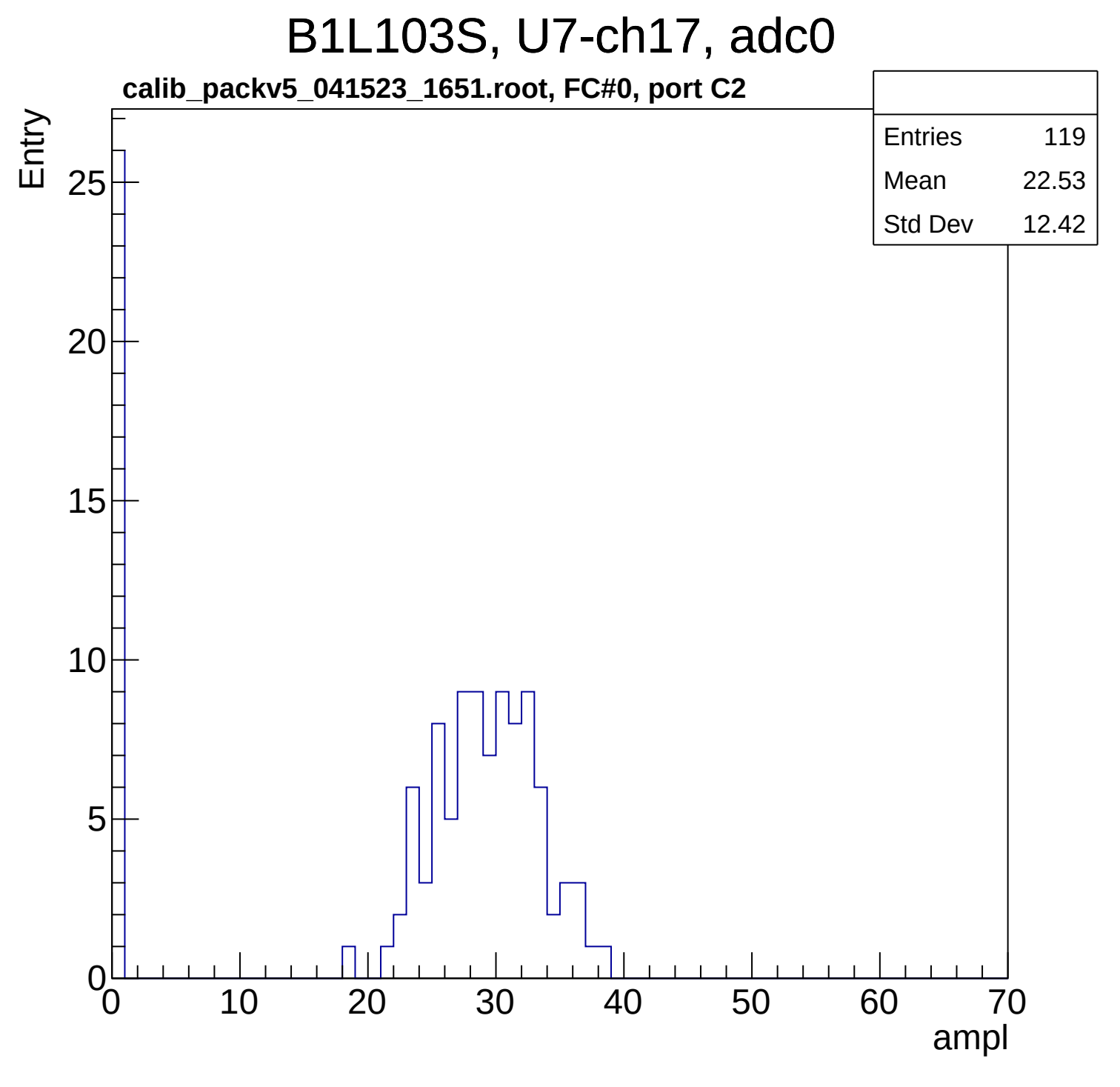
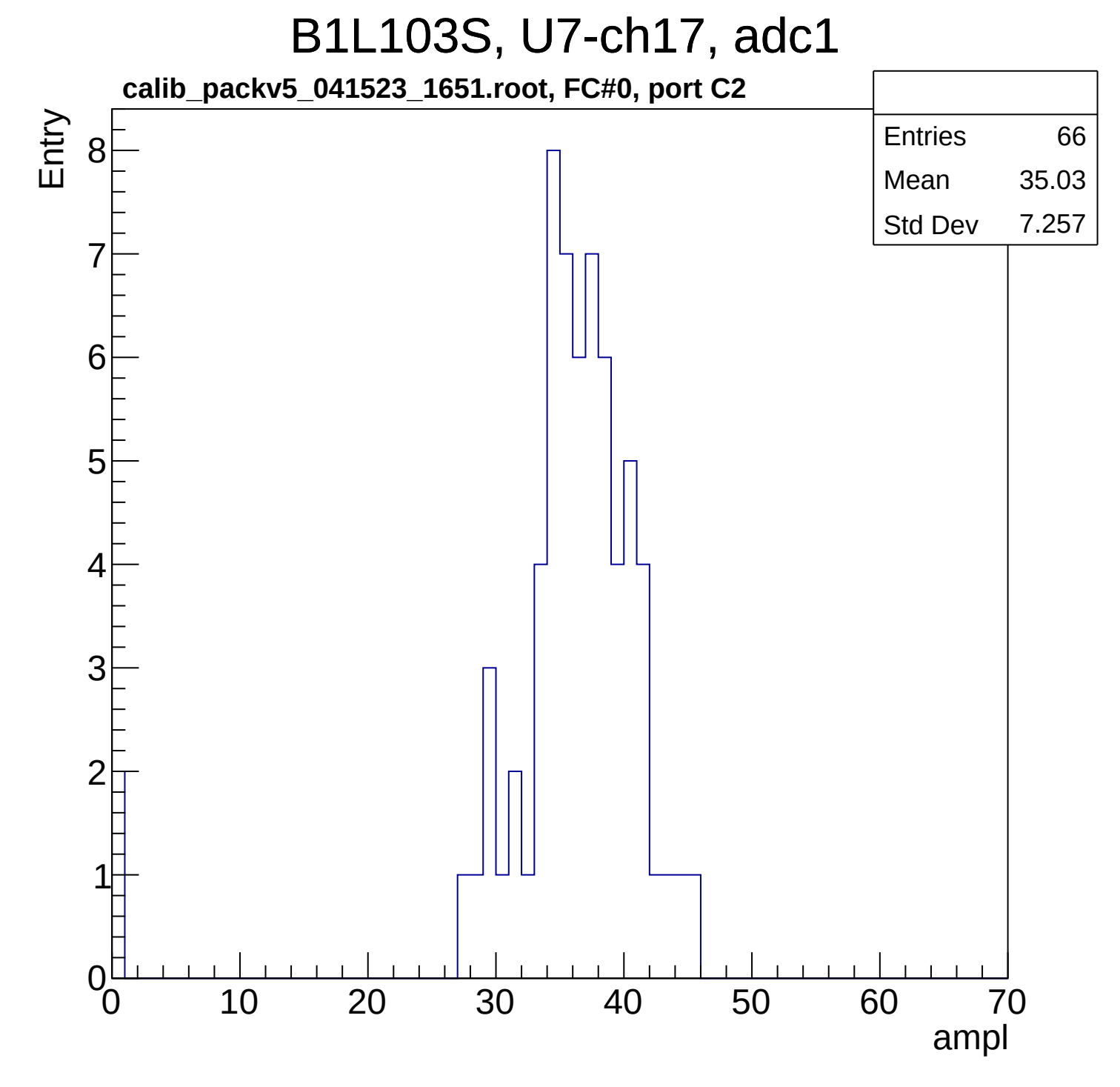

B1L103S, U7-ch16, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 4.25
Std Dev 14.3
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch17, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 119
Mean 22.53
Std Dev 12.42
Entry
0
5
10
15
20
25
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch17, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 35.03
Std Dev 7.257
Entry
ampl
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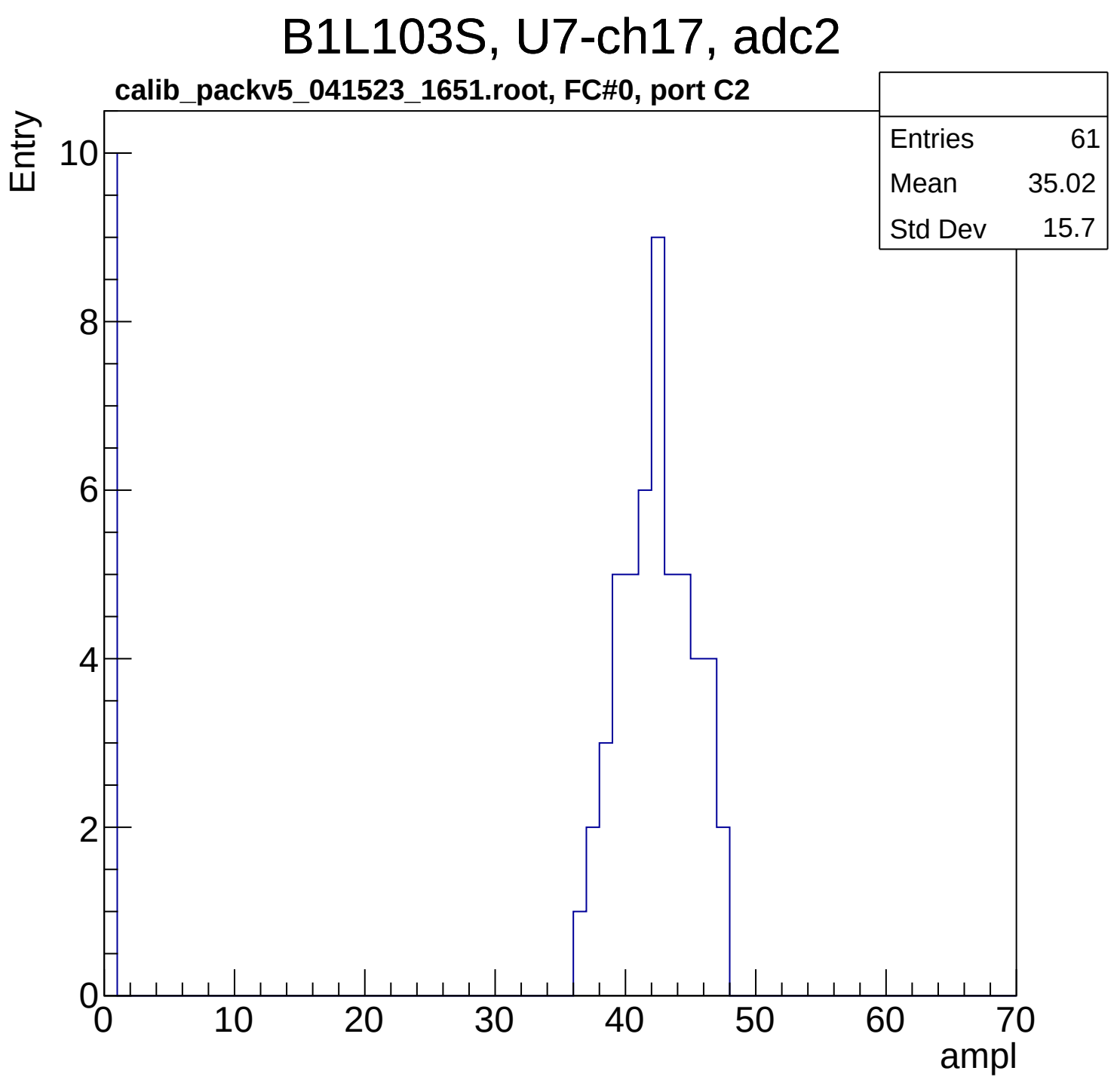
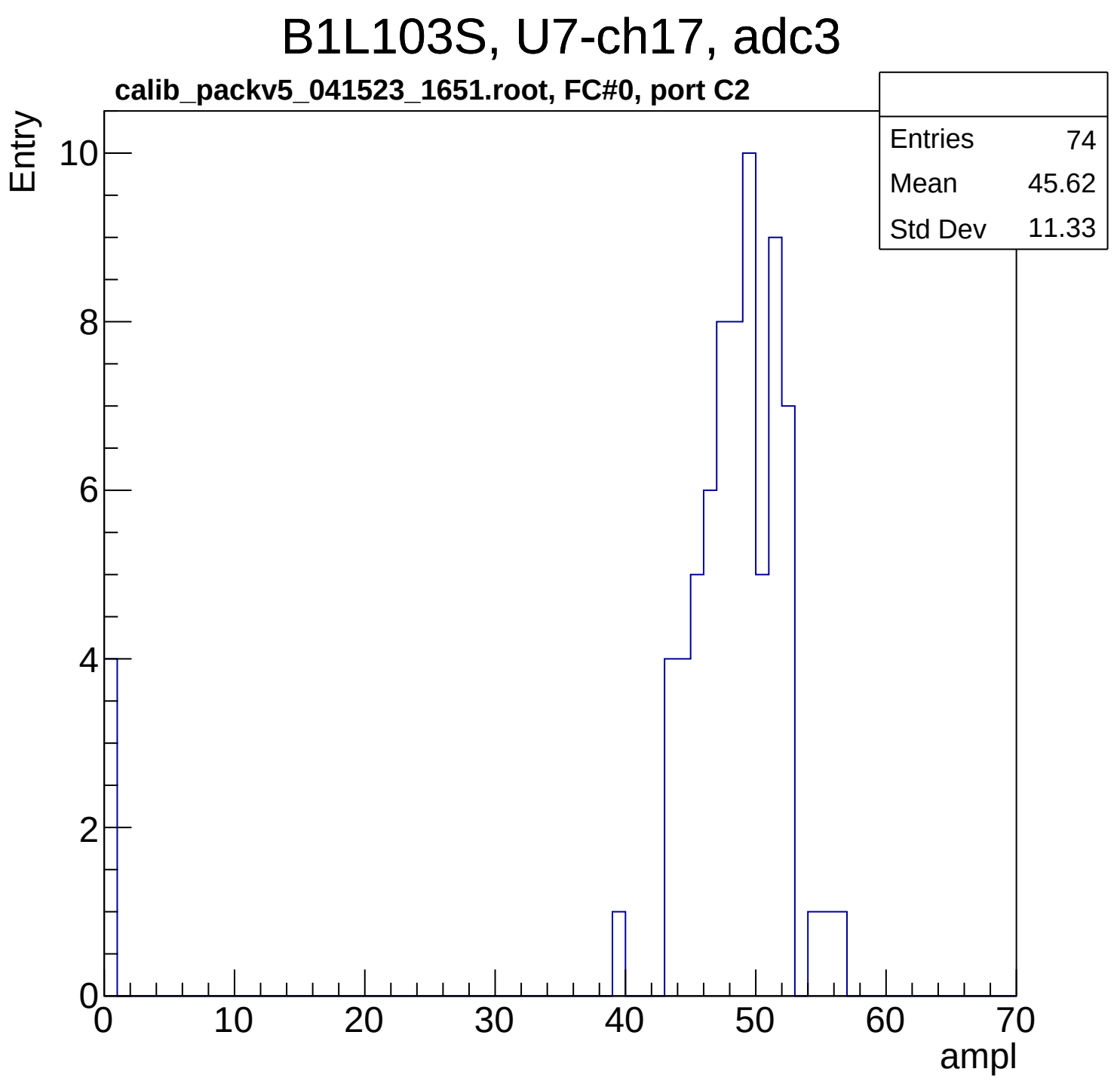
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch17, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 35.02
Std Dev 15.7
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch17, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 45.62
Std Dev 11.33
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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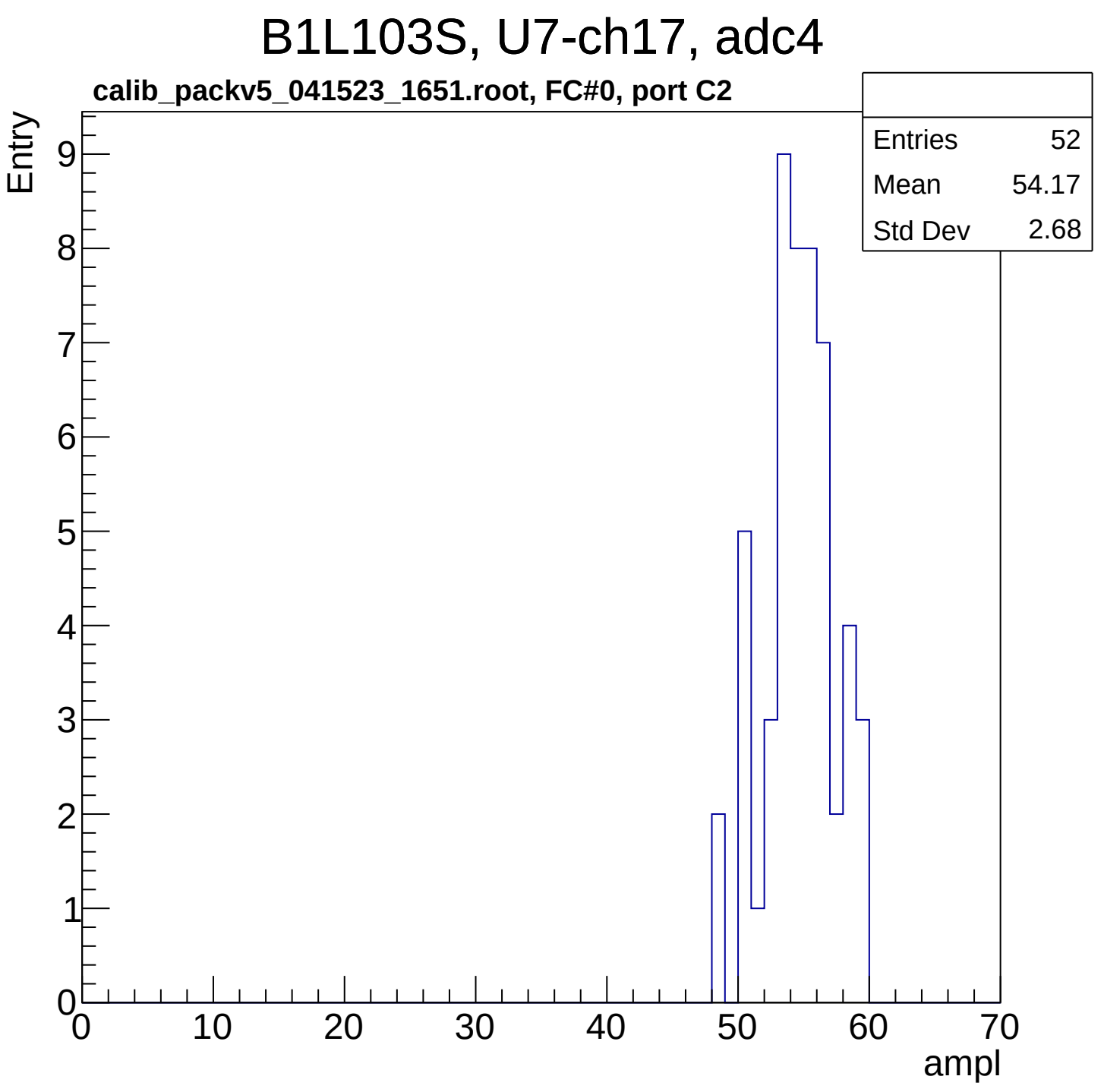
B1L103S, U7-ch17, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 54.17
Std Dev 2.68
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
50
60
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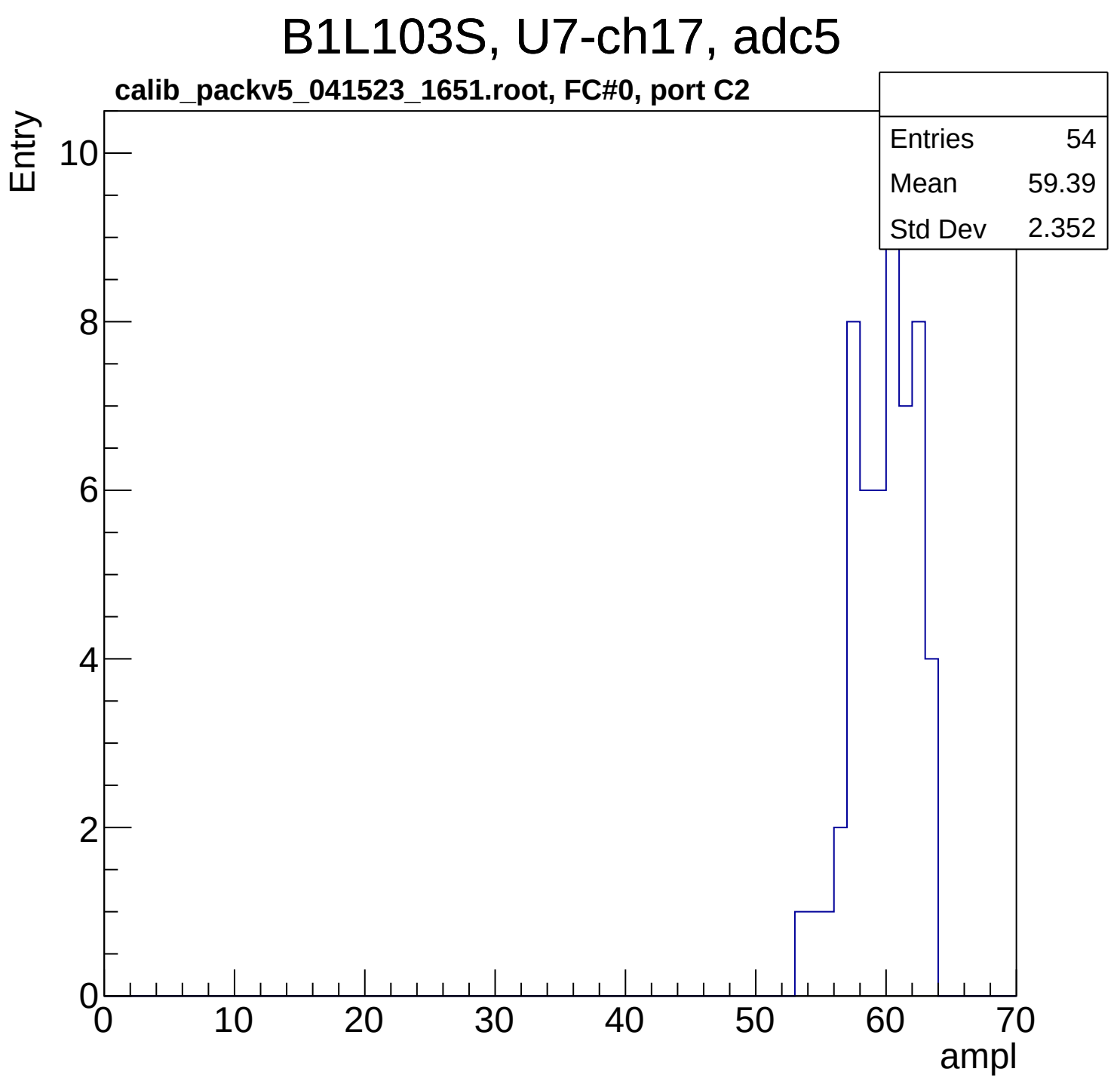
B1L103S, U7-ch17, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 59.39
Std Dev 2.352
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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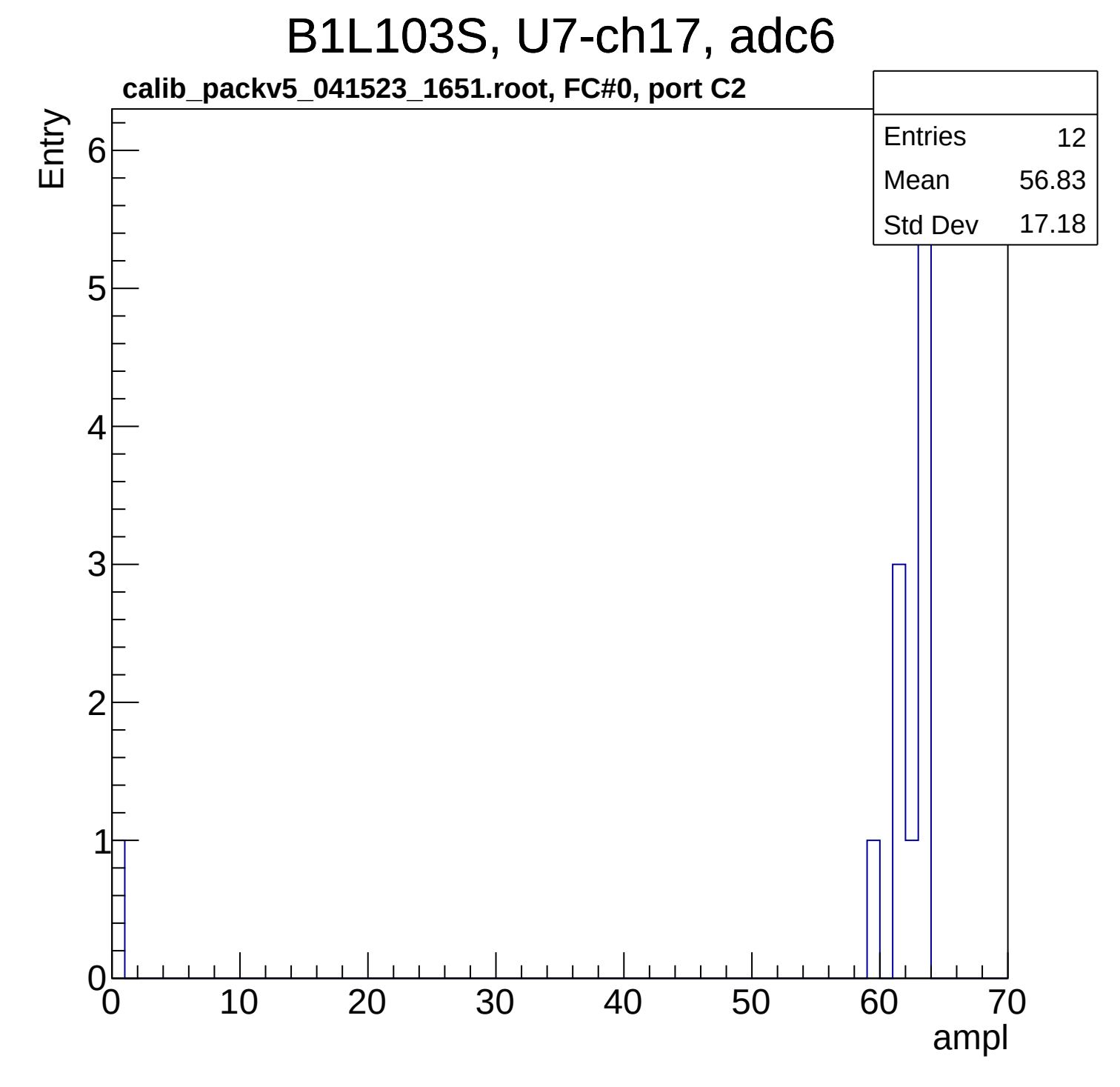
B1L103S, U7-ch17, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 56.83
Std Dev 17.18
Entry
0
1
2
3
4
5
6
0
10
20
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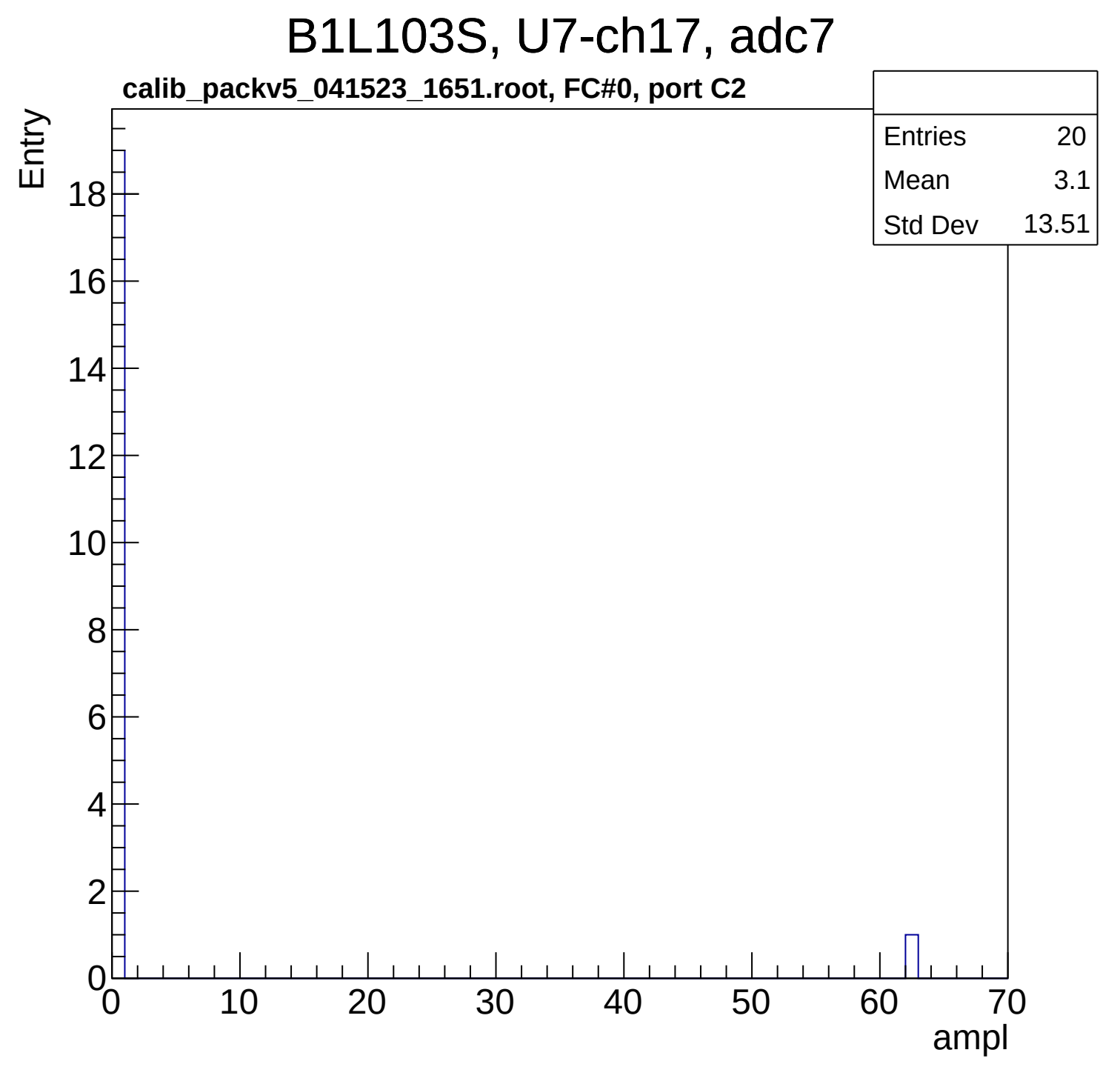
50
60
70
ampl


B1L103S, U7-ch17, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.1
Std Dev 13.51
Entry
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6
8
10
12
14
16
18
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10
20
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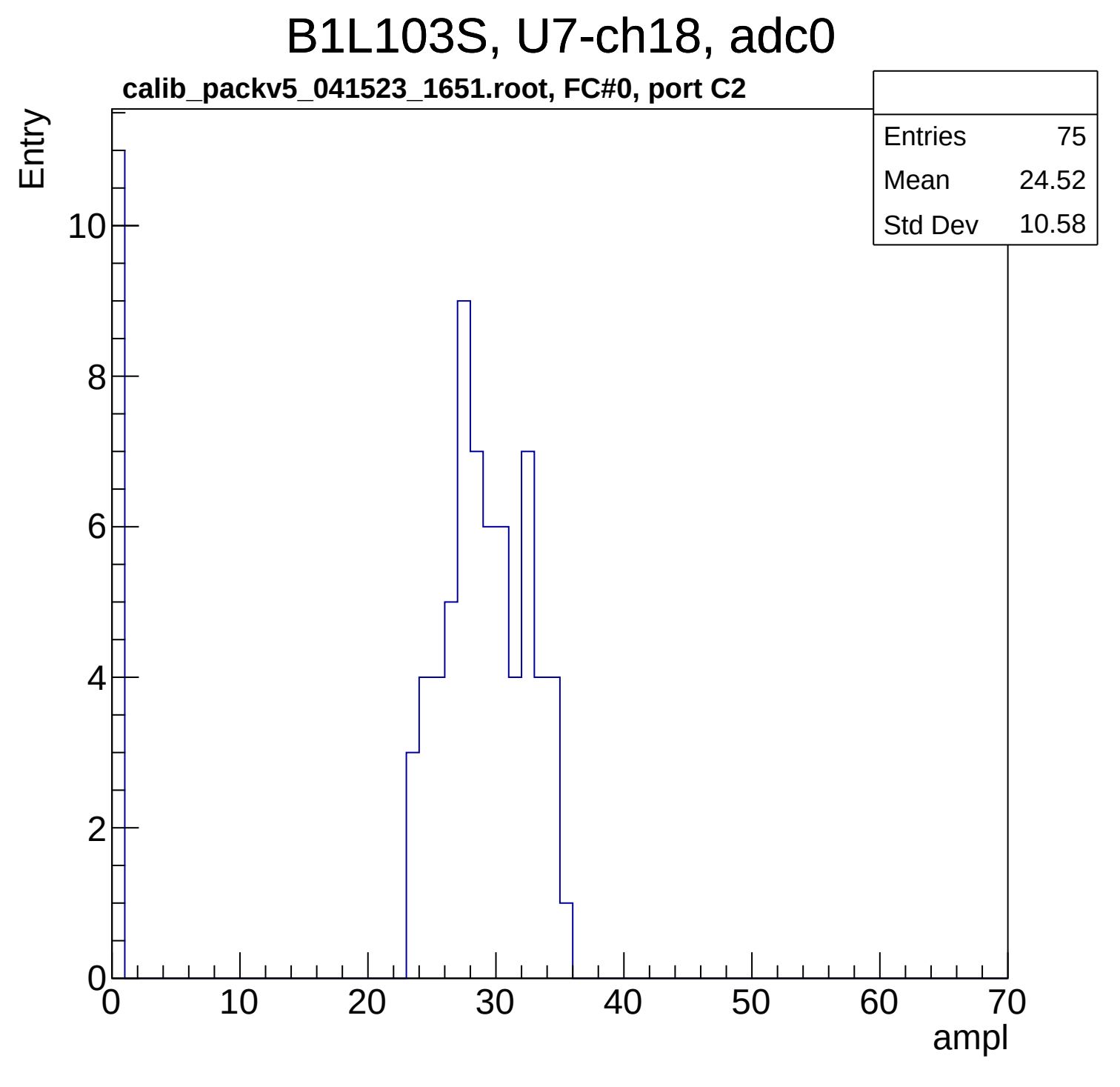
70
ampl


B1L103S, U7-ch18, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 24.52
Std Dev 10.58
Entry
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2
4
6
8
10
0
10
20
30
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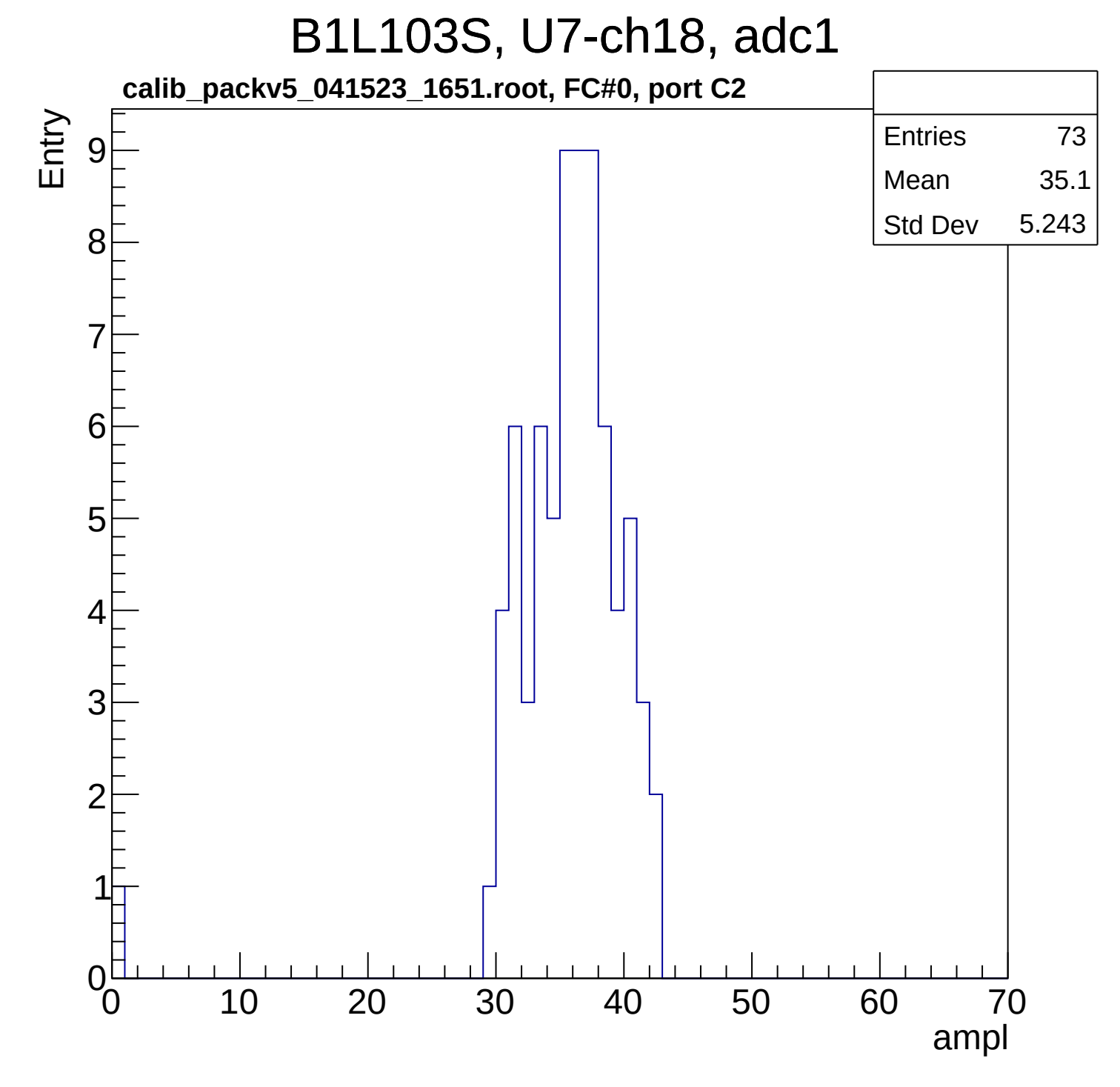
50
60
70
ampl


B1L103S, U7-ch18, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 35.1
Std Dev 5.243
Entry
ampl
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3
4
5
6
7
8
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0
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60
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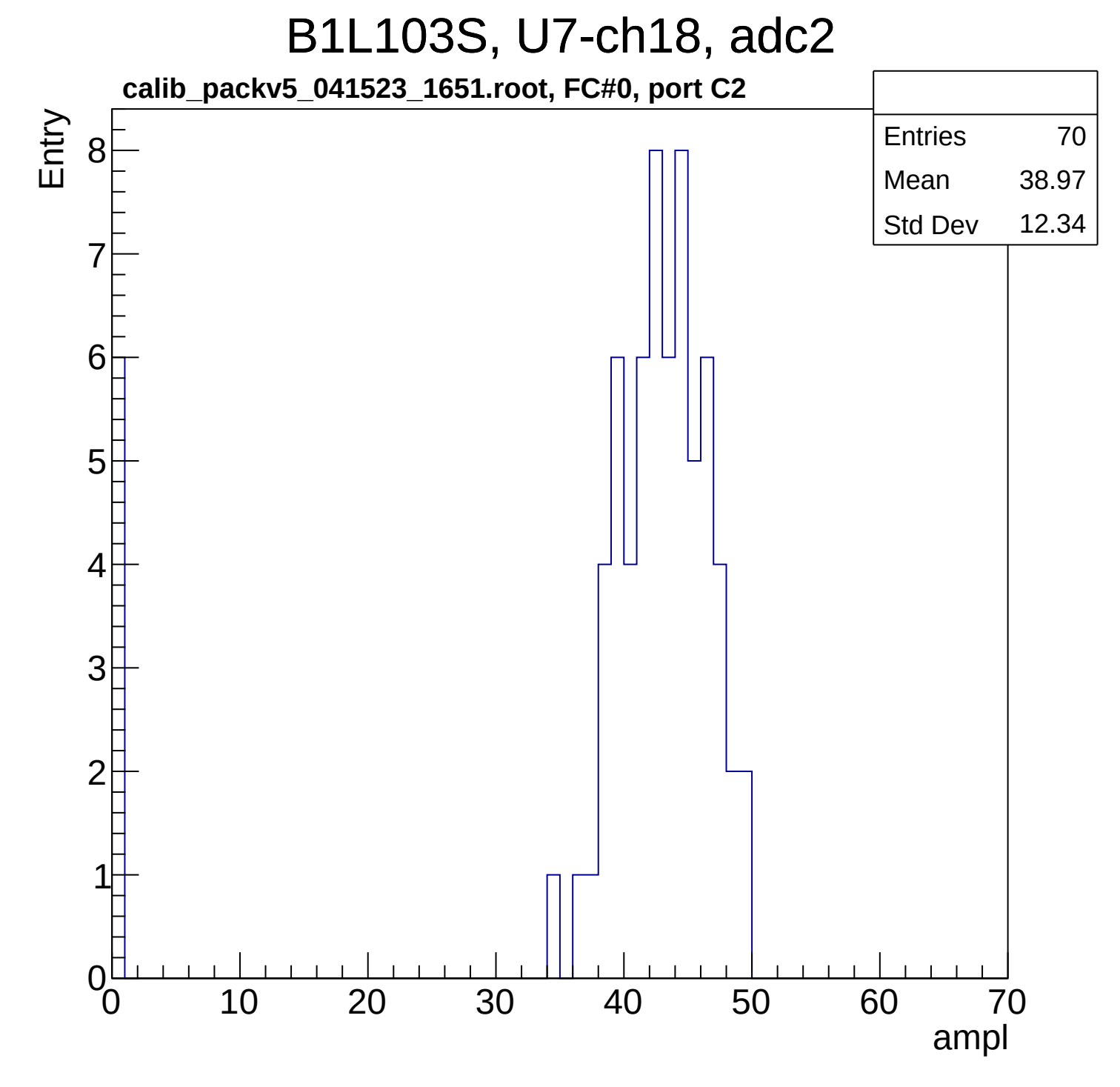
B1L103S, U7-ch18, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 38.97
Std Dev 12.34
Entry
ampl
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1
2
3
4
5
6
7
8
0
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40
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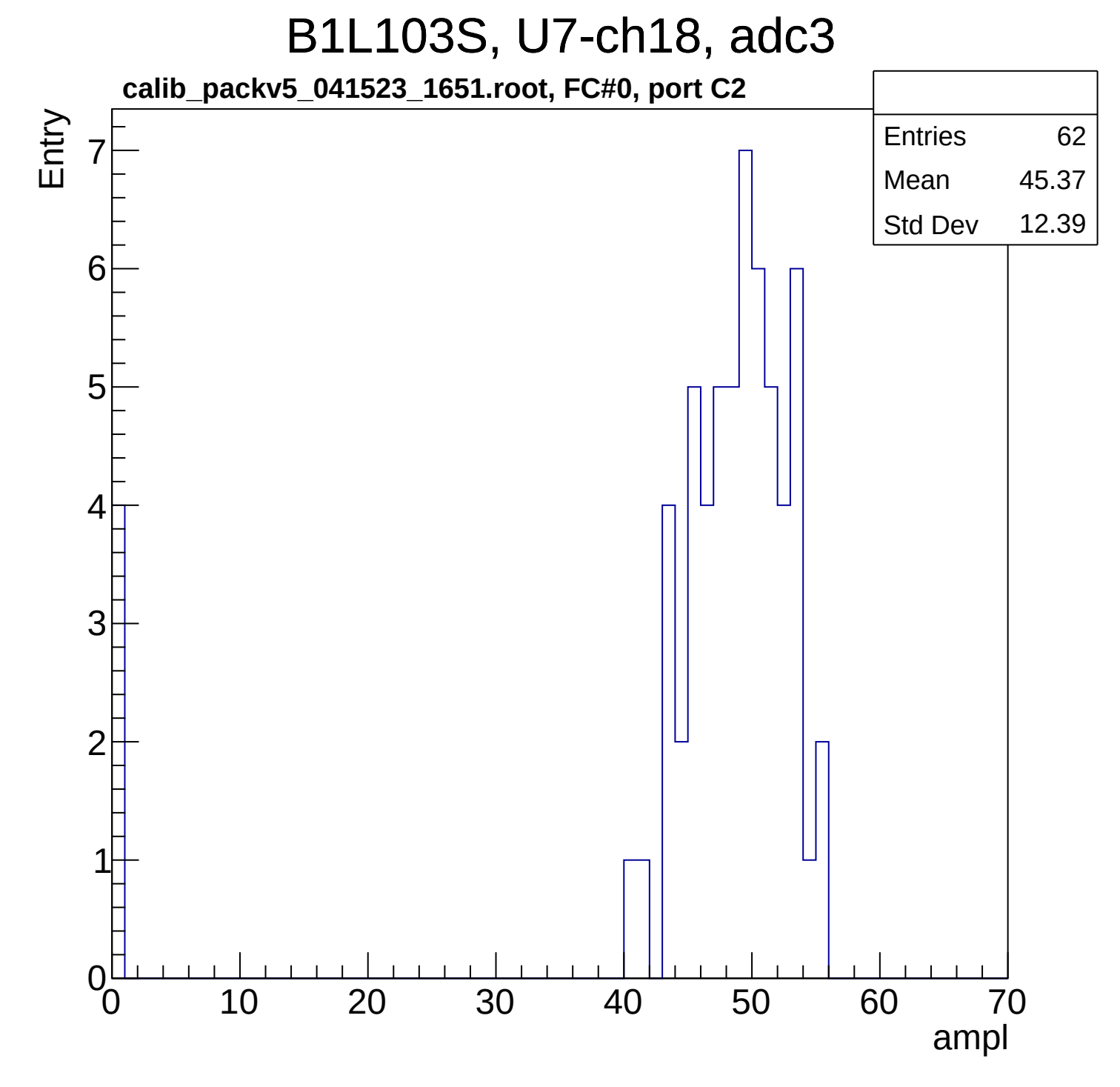
B1L103S, U7-ch18, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 45.37
Std Dev 12.39
Entry
ampl
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1
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4
5
6
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0
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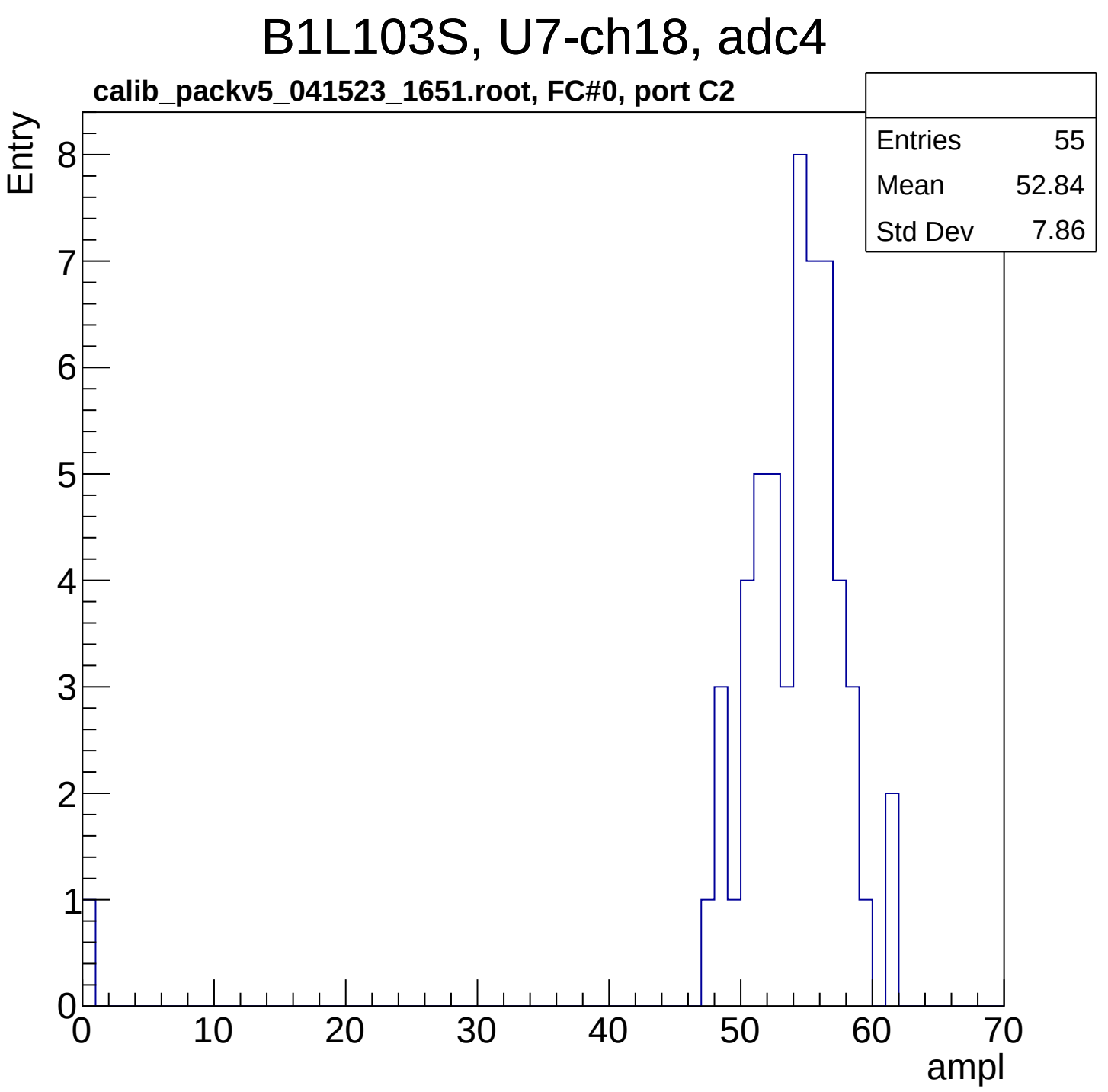
B1L103S, U7-ch18, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 52.84
Std Dev 7.86
Entry
ampl
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4
5
6
7
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0
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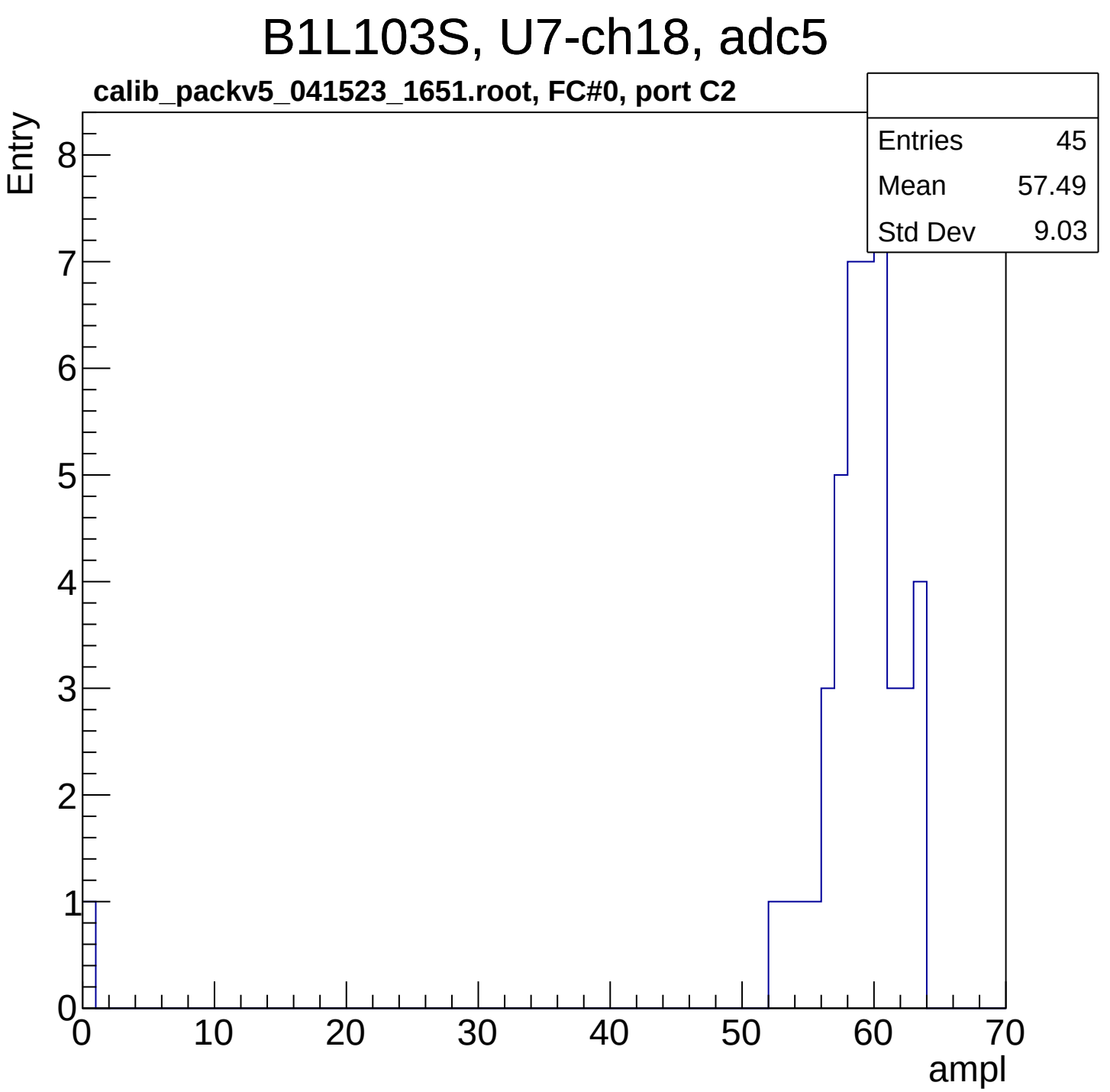
B1L103S, U7-ch18, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 57.49
Std Dev 9.03
Entry
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4
5
6
7
8
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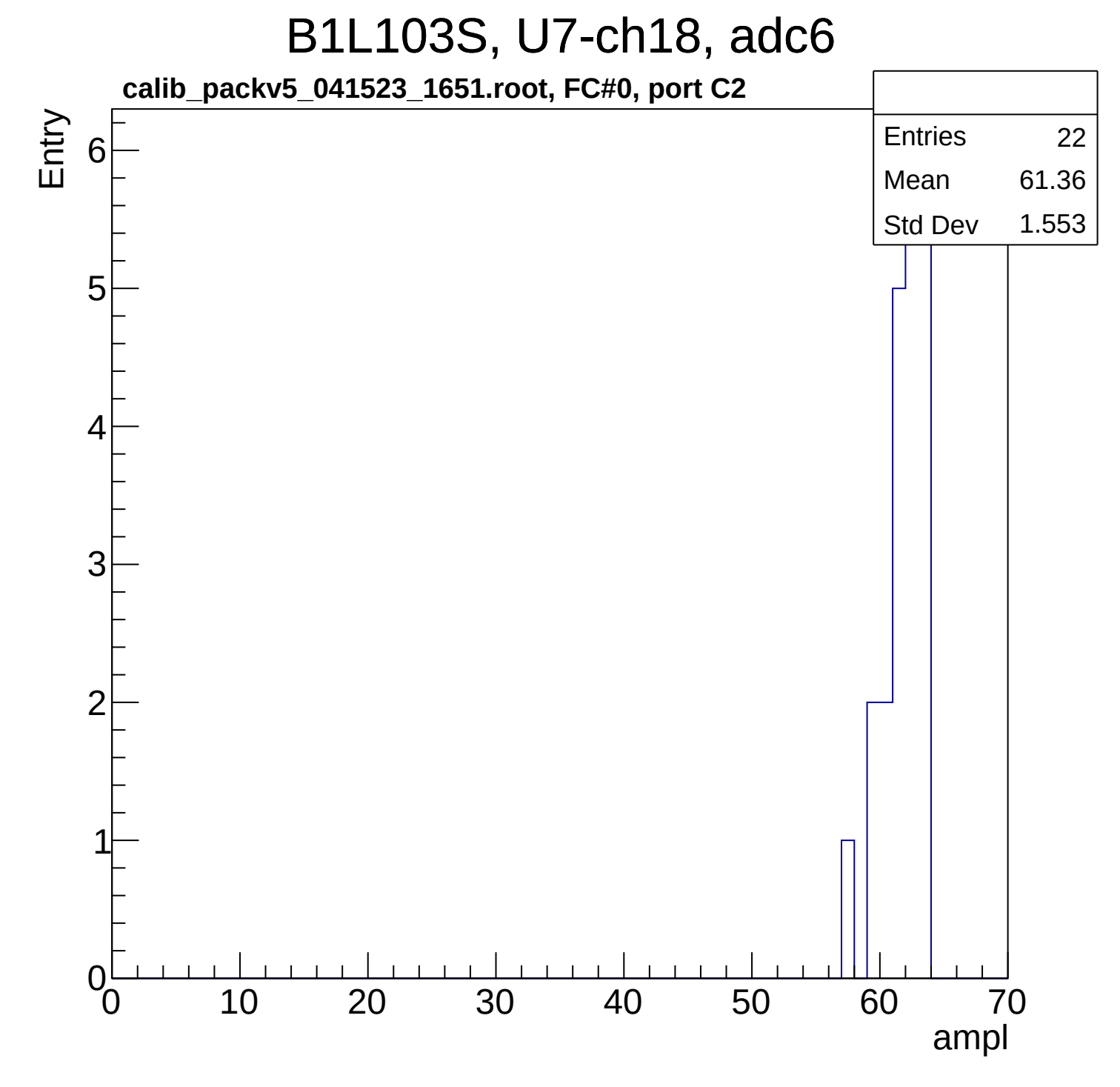
ampl


B1L103S, U7-ch18, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 61.36
Std Dev 1.553
Entry
ampl
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3
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5
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0
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60
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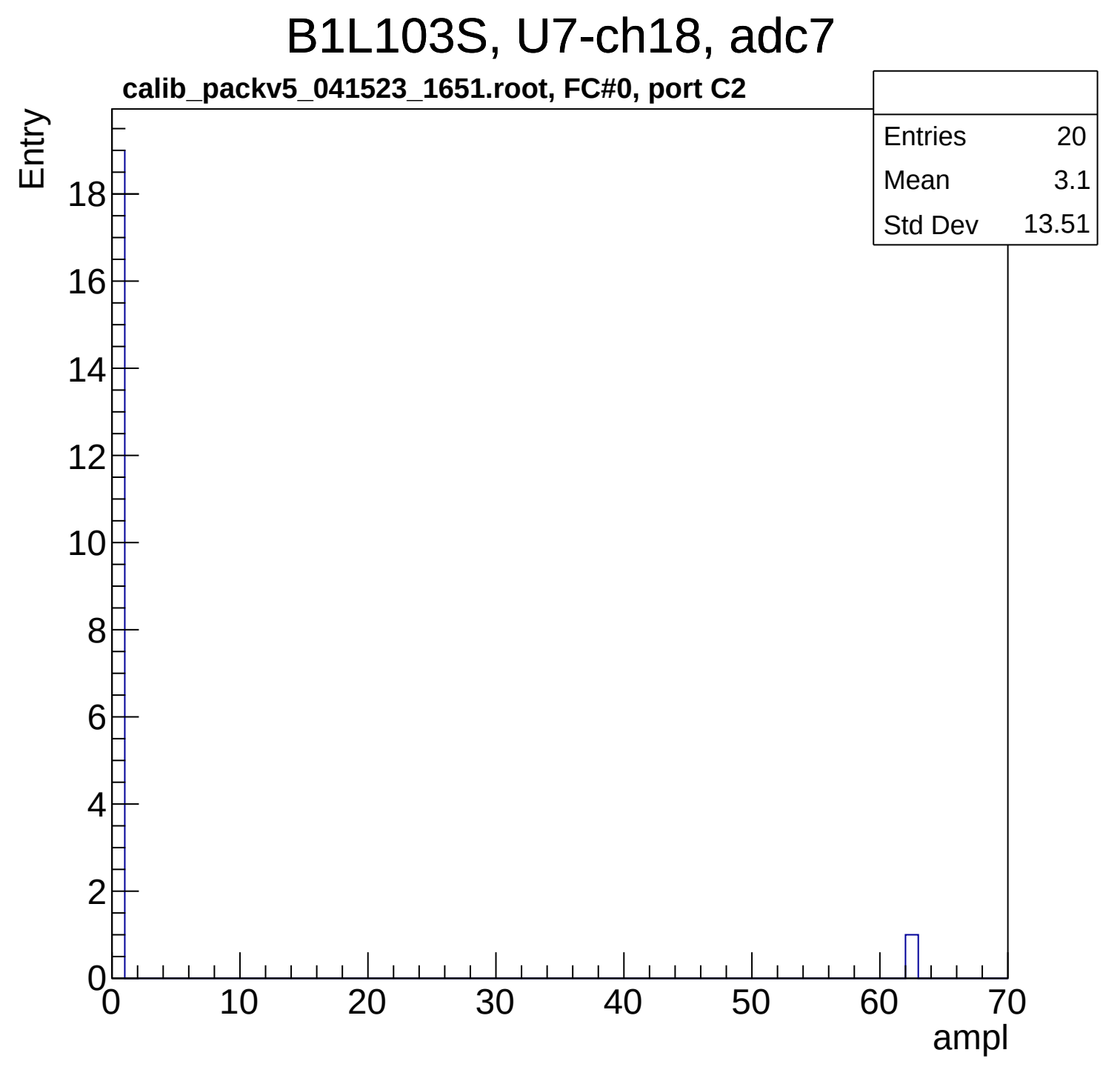
B1L103S, U7-ch18, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.1
Std Dev 13.51
Entry
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6
8
10
12
14
16
18
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10
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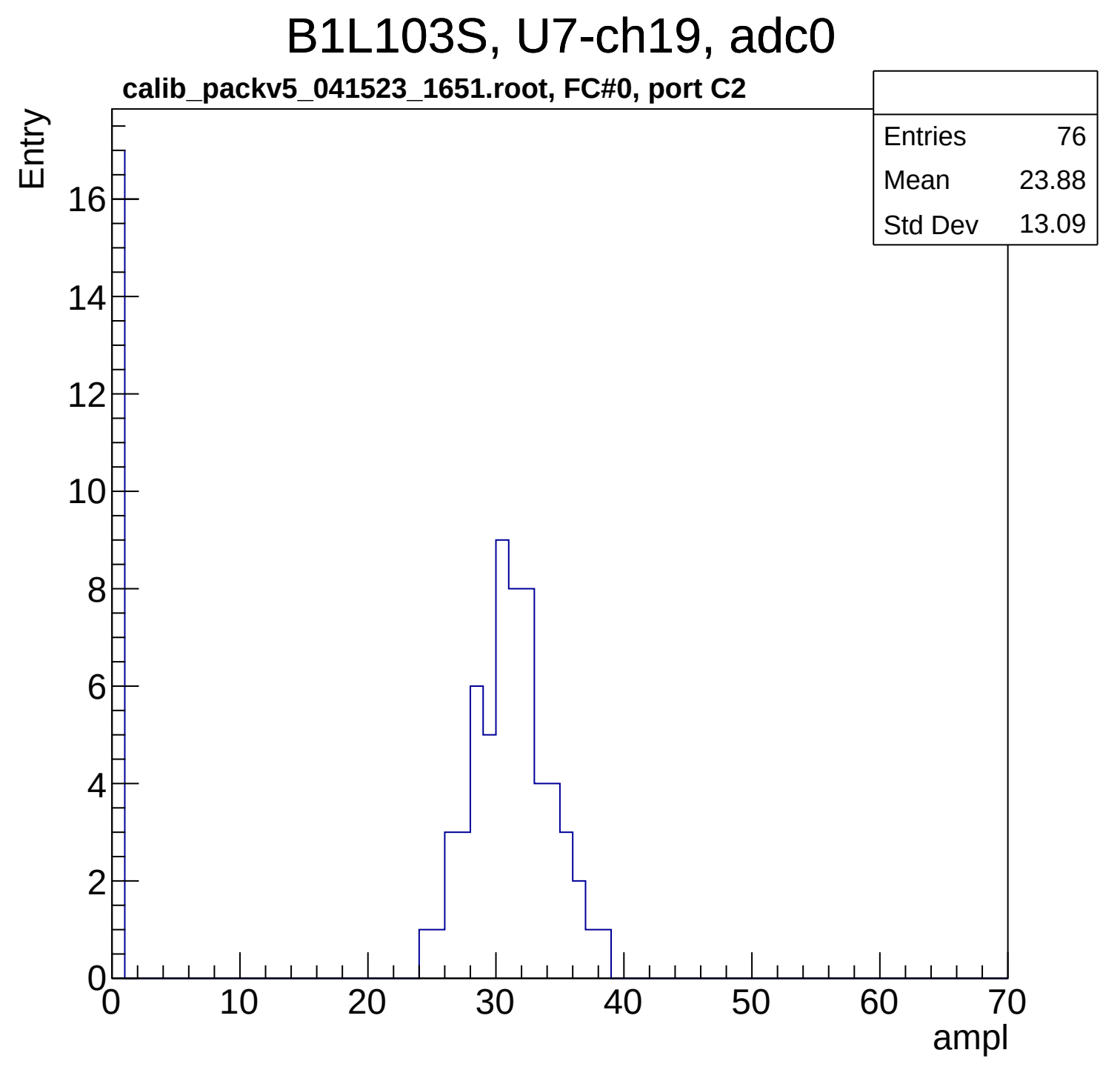
70
ampl


B1L103S, U7-ch19, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 23.88
Std Dev 13.09
Entry
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6
8
10
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14
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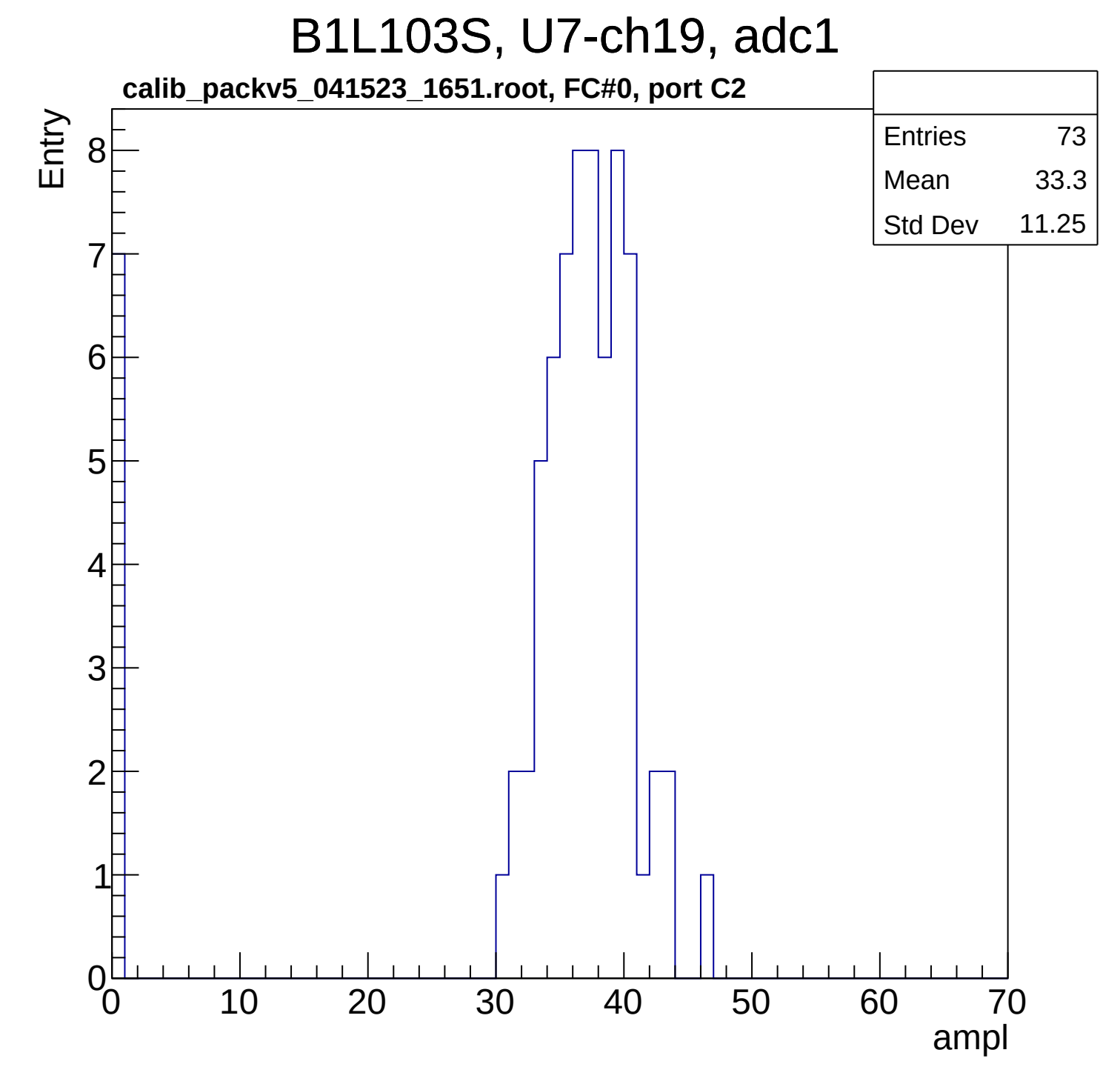
ampl


B1L103S, U7-ch19, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 33.3
Std Dev 11.25
Entry
ampl
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2
3
4
5
6
7
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0
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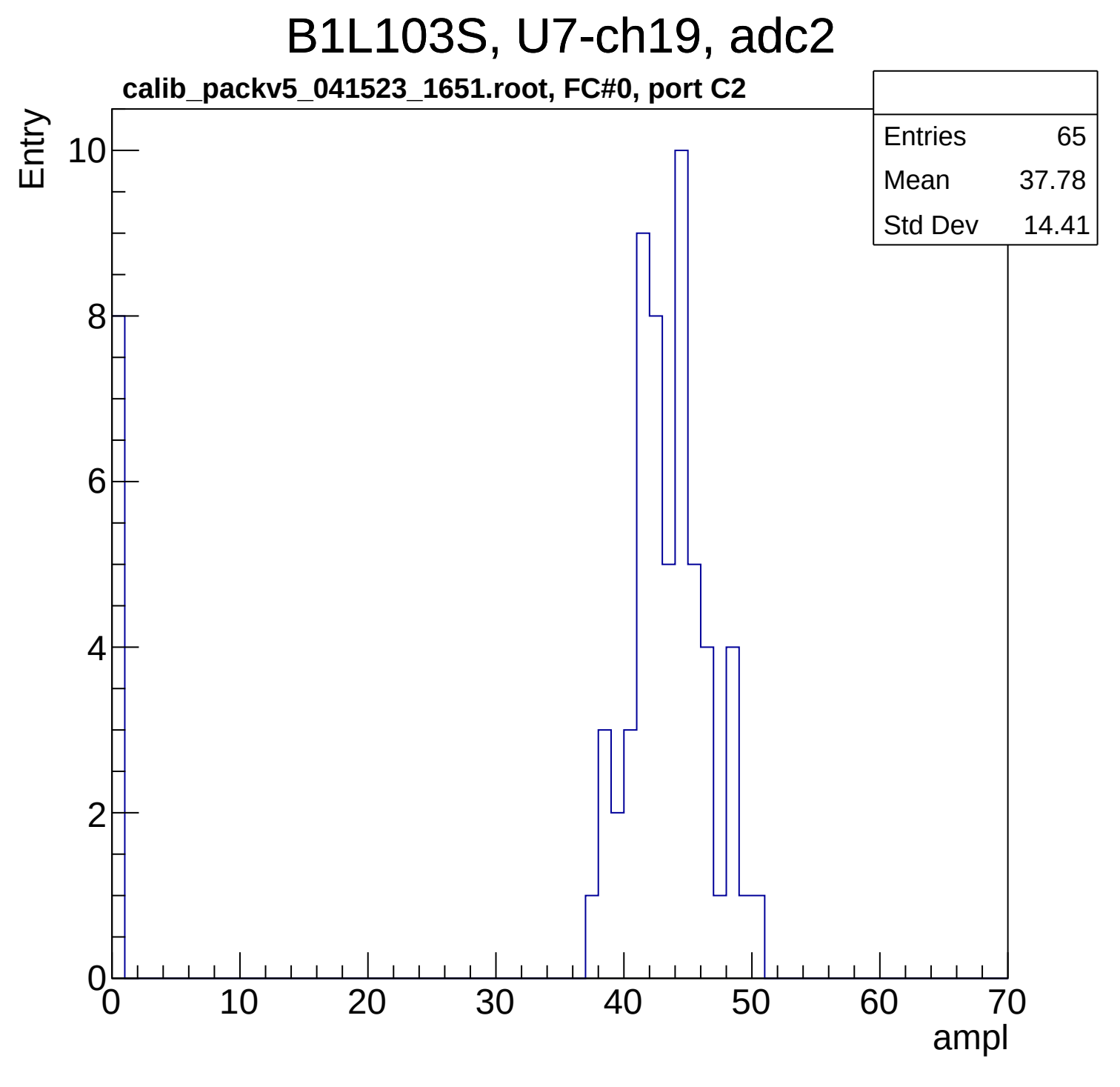
B1L103S, U7-ch19, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 37.78
Std Dev 14.41
Entry
ampl
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4
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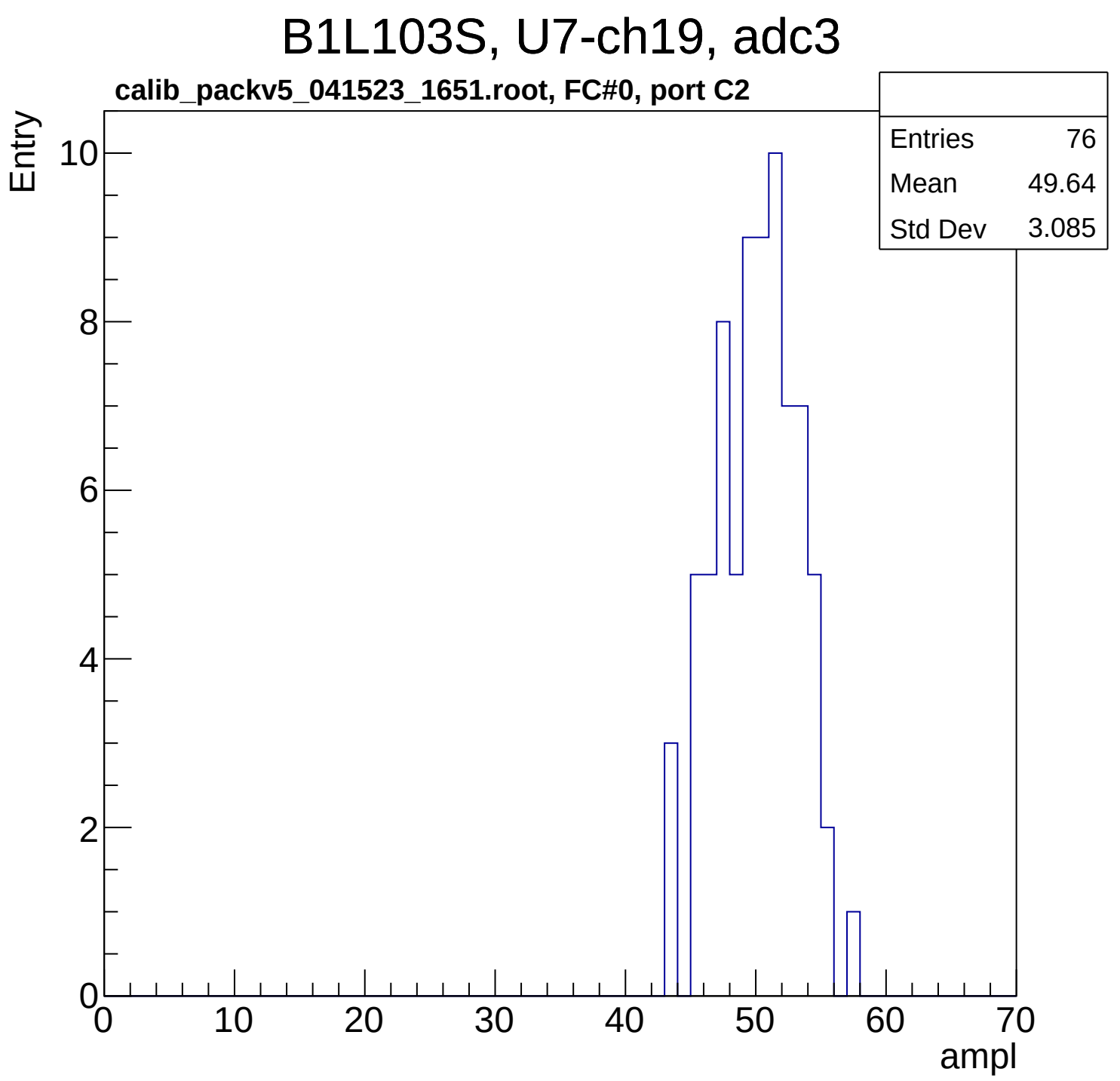
B1L103S, U7-ch19, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 49.64
Std Dev 3.085
Entry
ampl
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4
6
8
10
0
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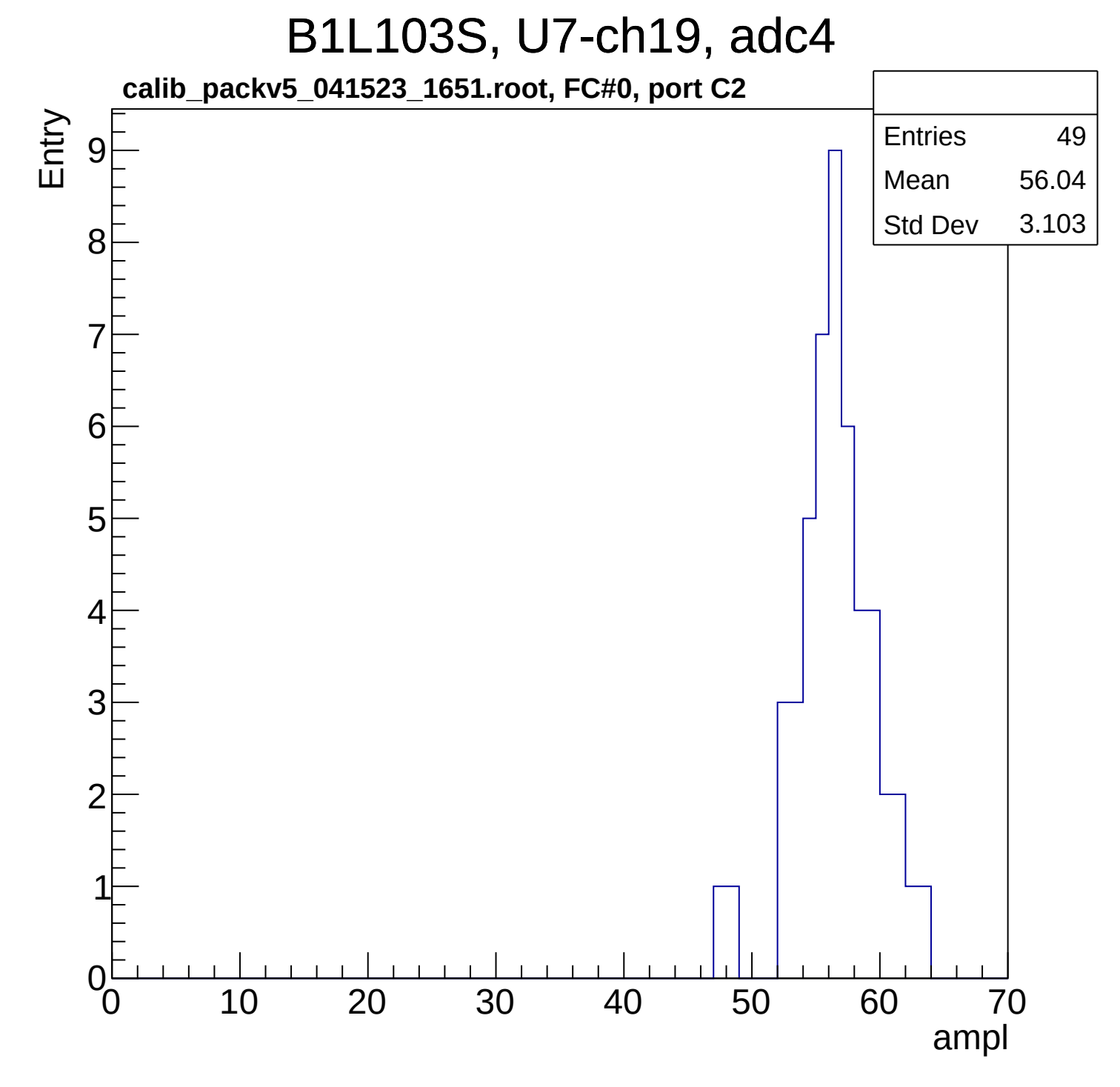
B1L103S, U7-ch19, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 56.04
Std Dev 3.103
Entry
ampl
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3
4
5
6
7
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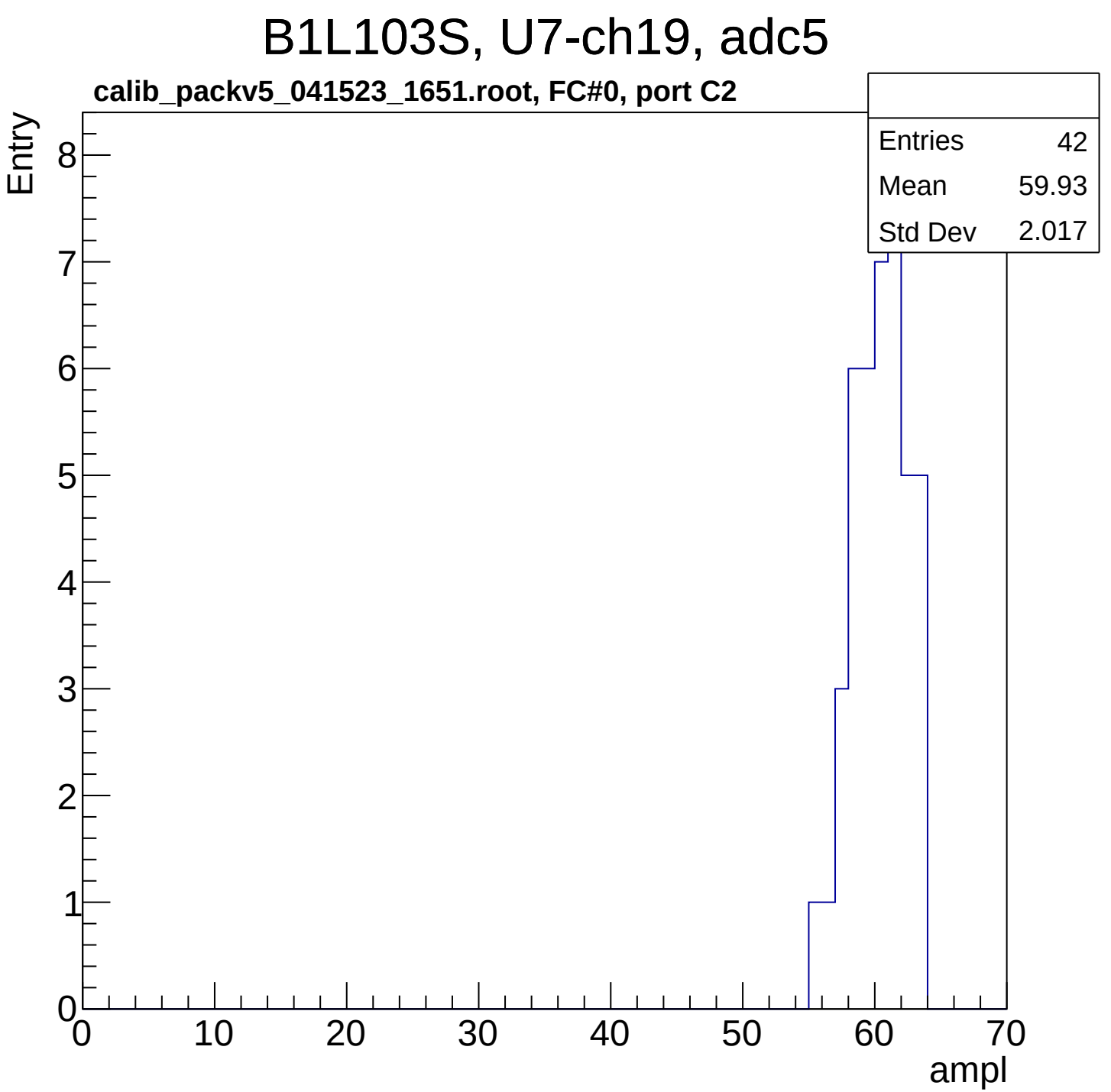
B1L103S, U7-ch19, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 42
Mean 59.93
Std Dev 2.017
Entry
ampl
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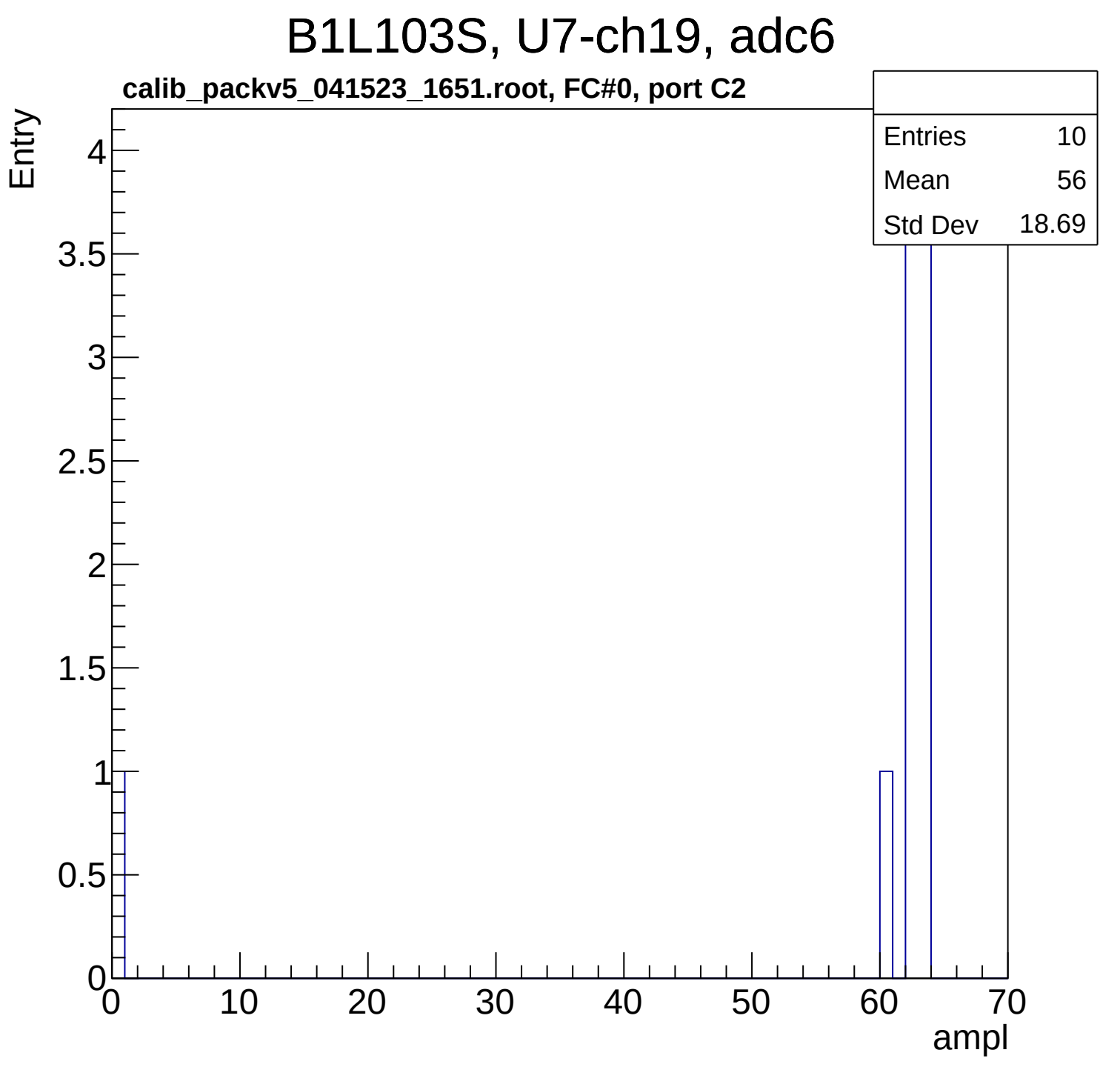
B1L103S, U7-ch19, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 56
Std Dev 18.69
Entry
ampl
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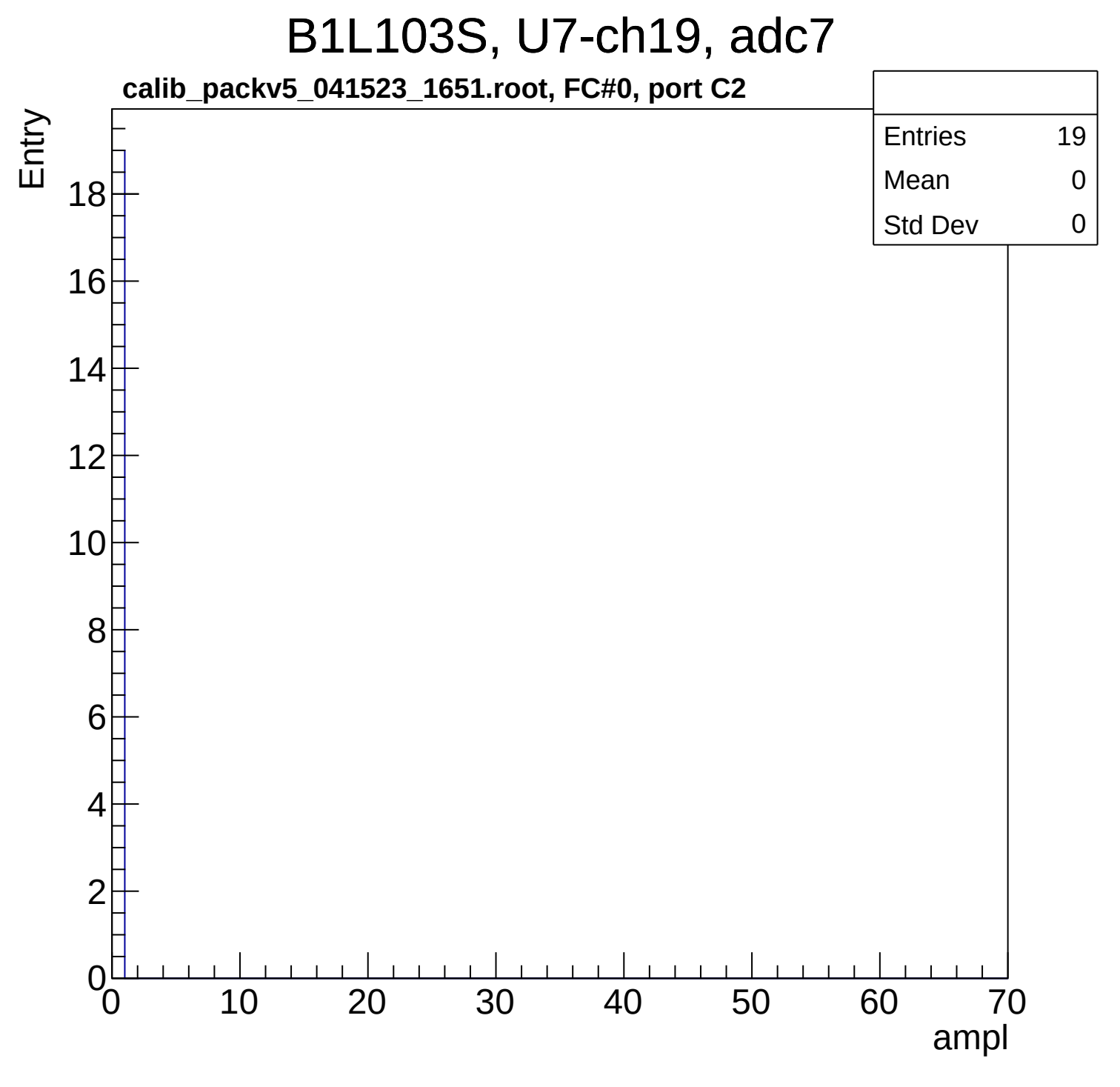
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U7-ch19, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
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30
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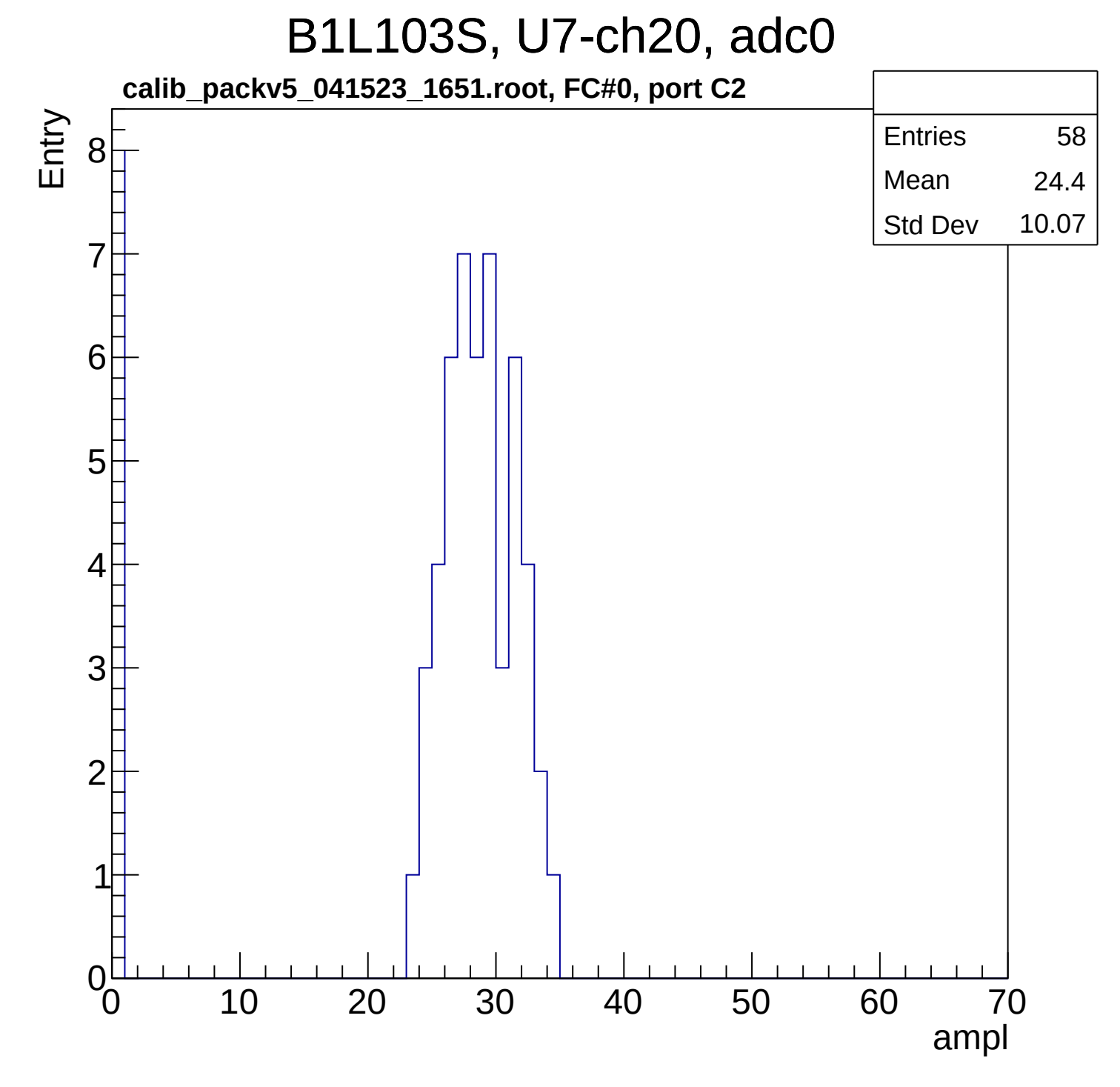
50
60
70
ampl


B1L103S, U7-ch20, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 24.4
Std Dev 10.07
Entry
ampl
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2
3
4
5
6
7
8
0
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40
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60
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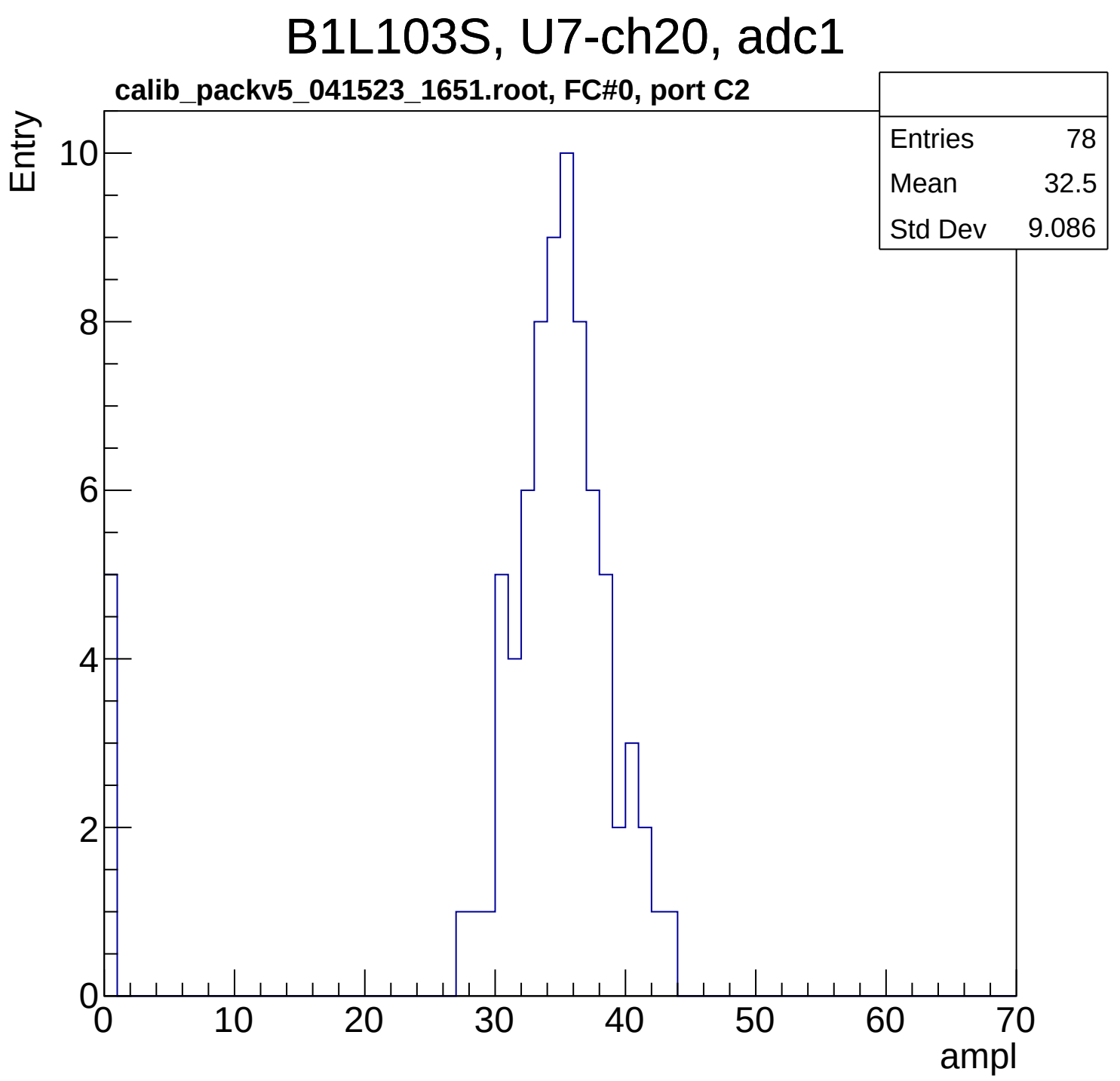
B1L103S, U7-ch20, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 32.5
Std Dev 9.086
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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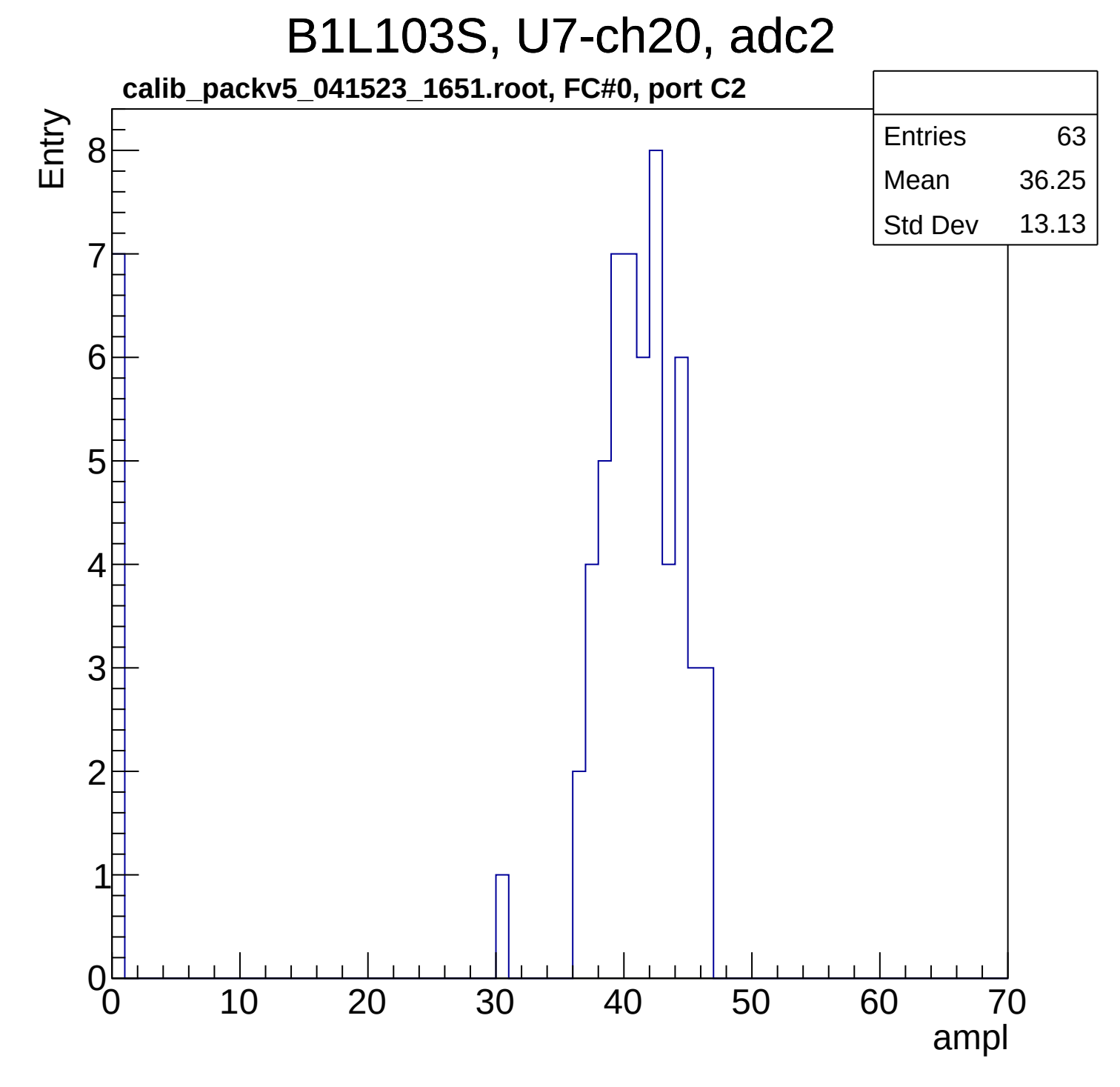
B1L103S, U7-ch20, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 36.25
Std Dev 13.13
Entry
ampl
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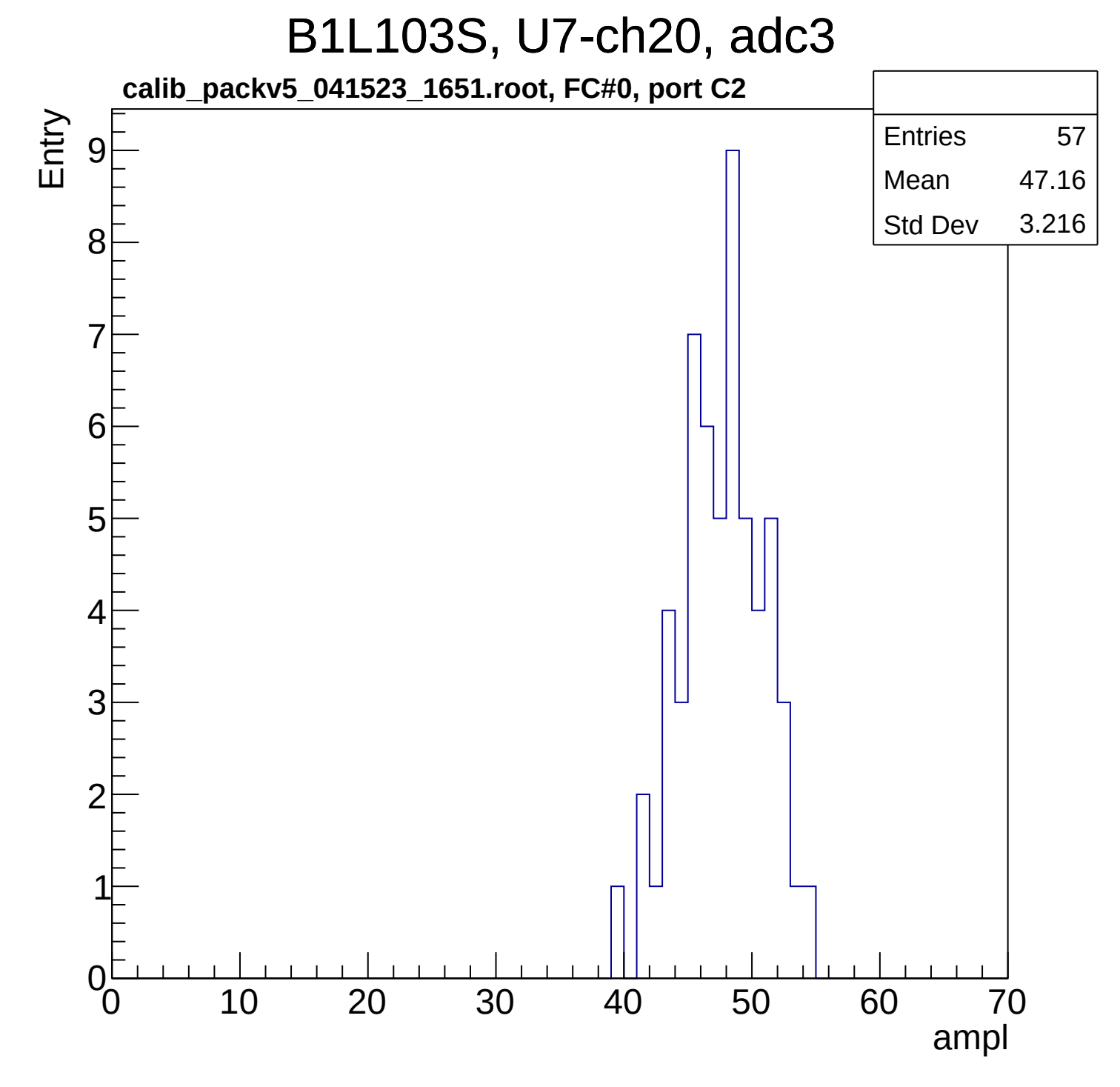
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch20, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 47.16
Std Dev 3.216
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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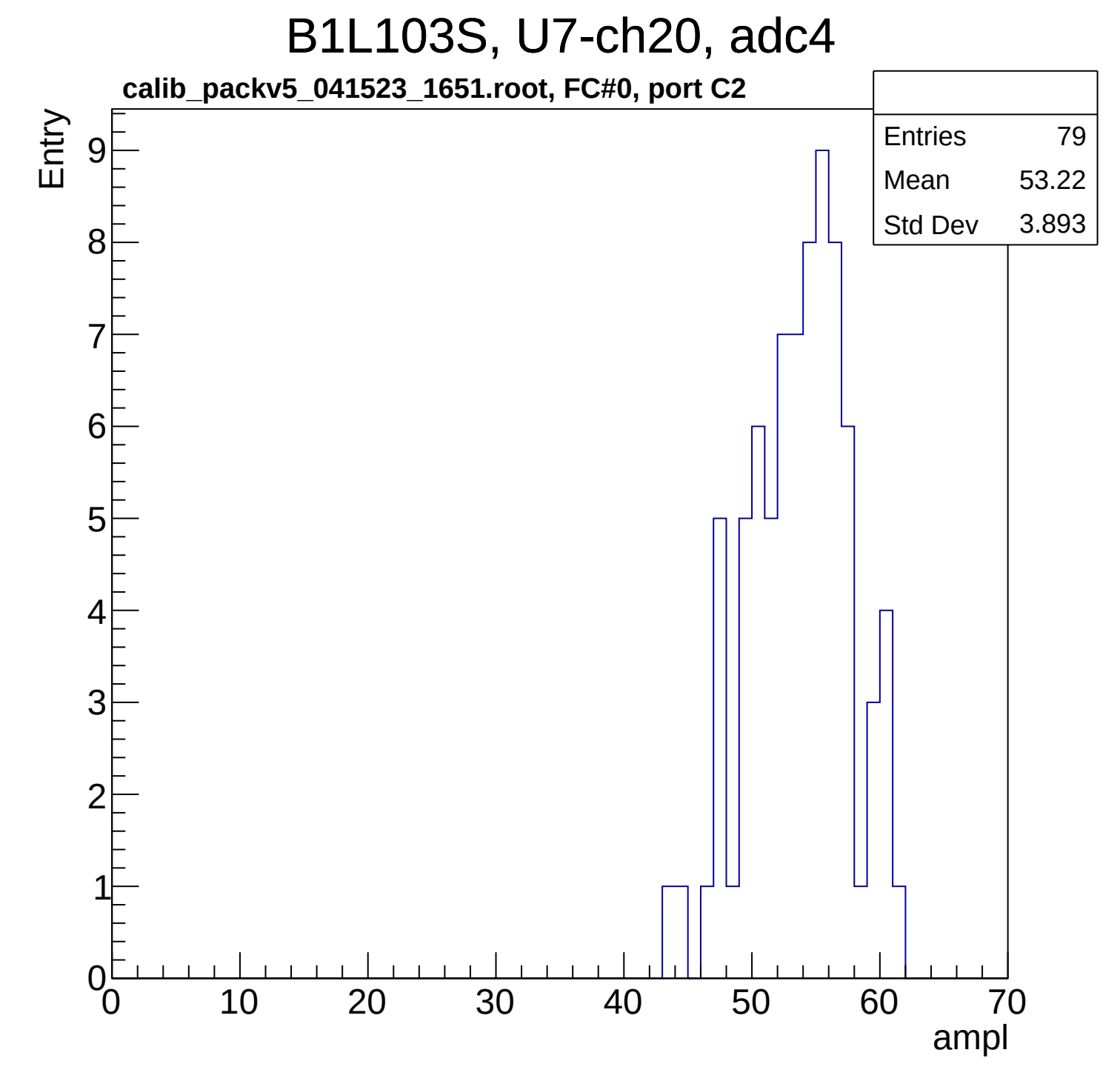
B1L103S, U7-ch20, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 53.22
Std Dev 3.893
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
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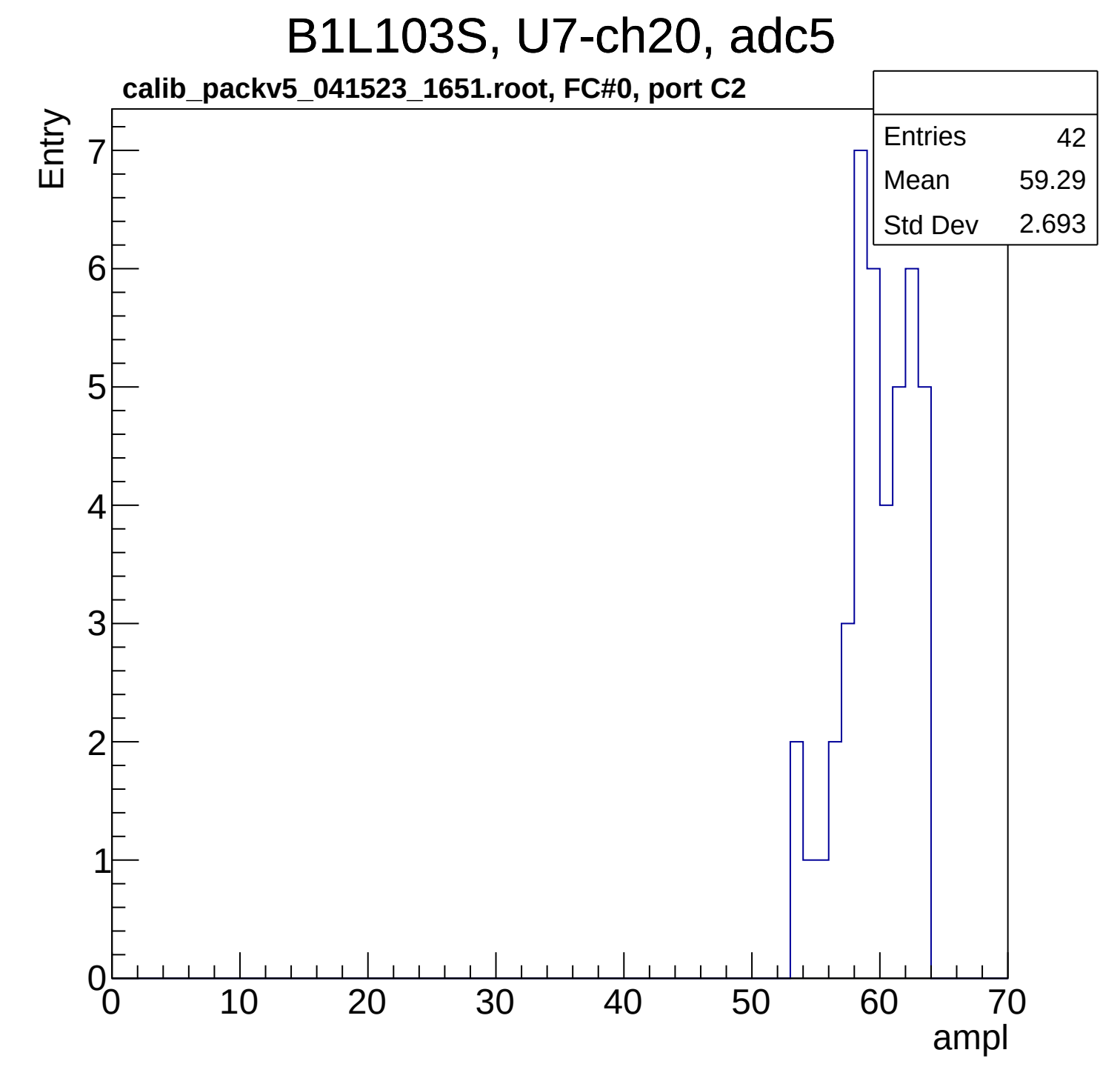
60
70


B1L103S, U7-ch20, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 42
Mean 59.29
Std Dev 2.693
Entry
ampl
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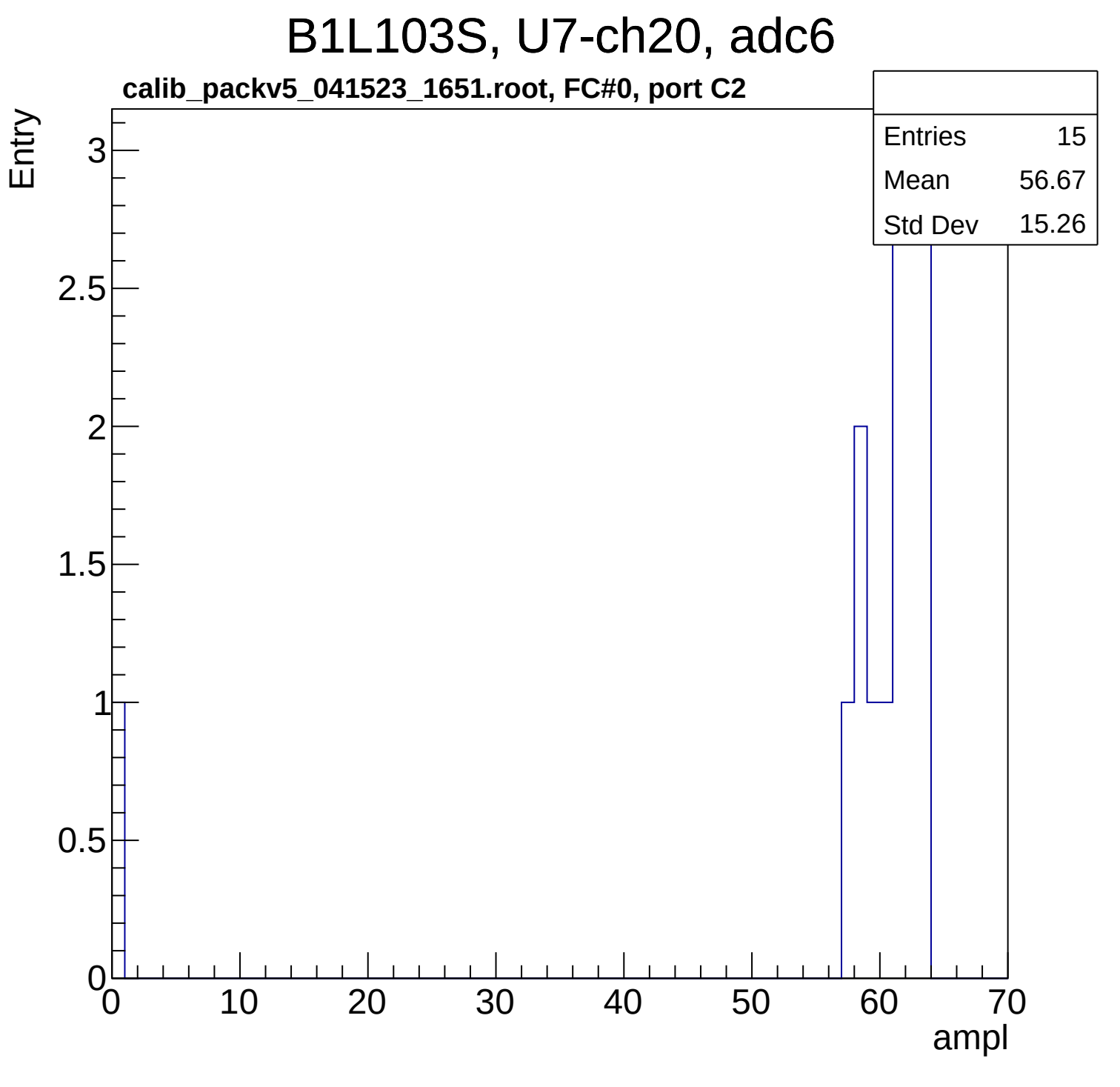
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U7-ch20, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 15
Mean 56.67
Std Dev 15.26
Entry
ampl
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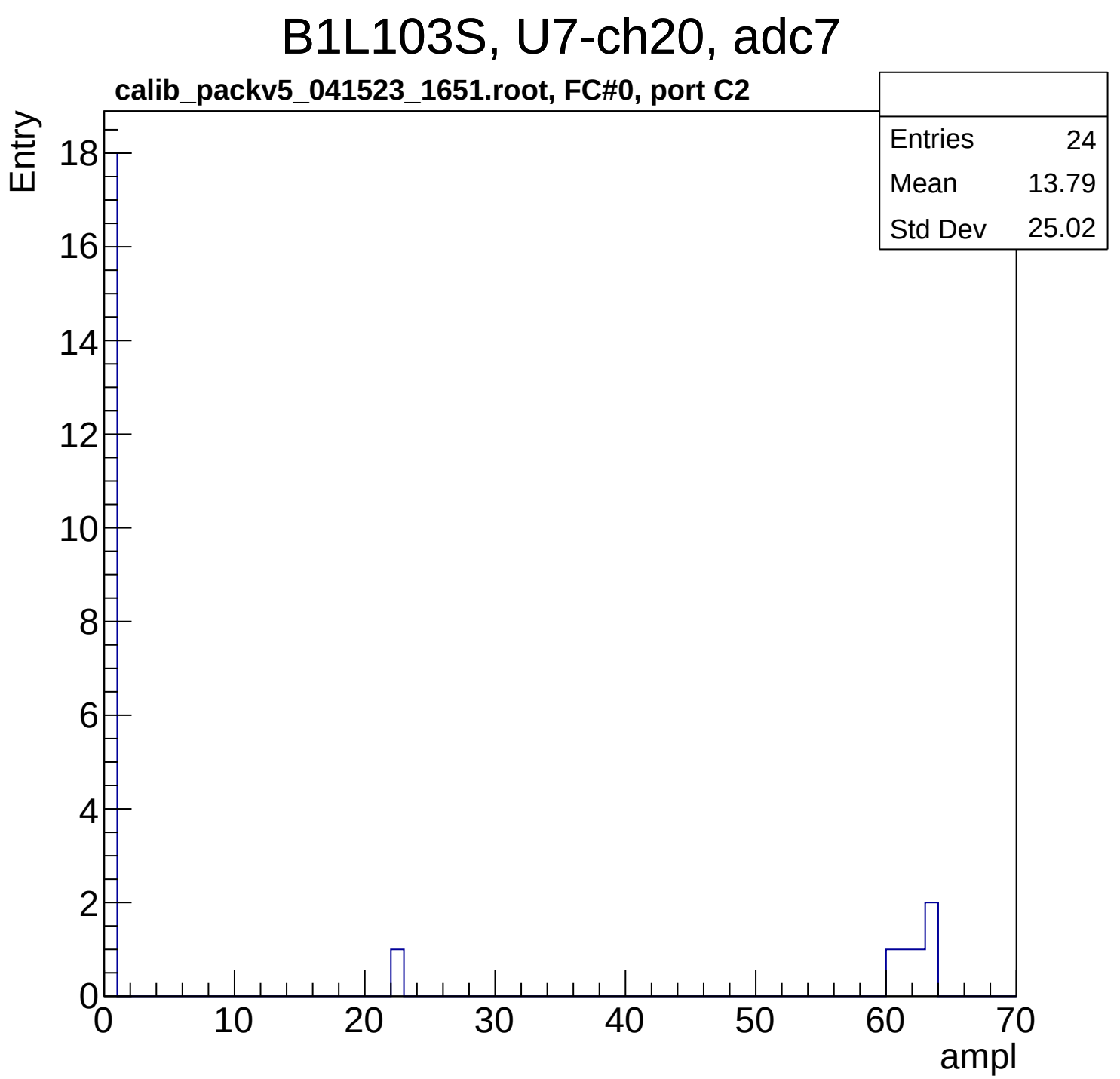
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U7-ch20, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 24
Mean 13.79
Std Dev 25.02
Entry
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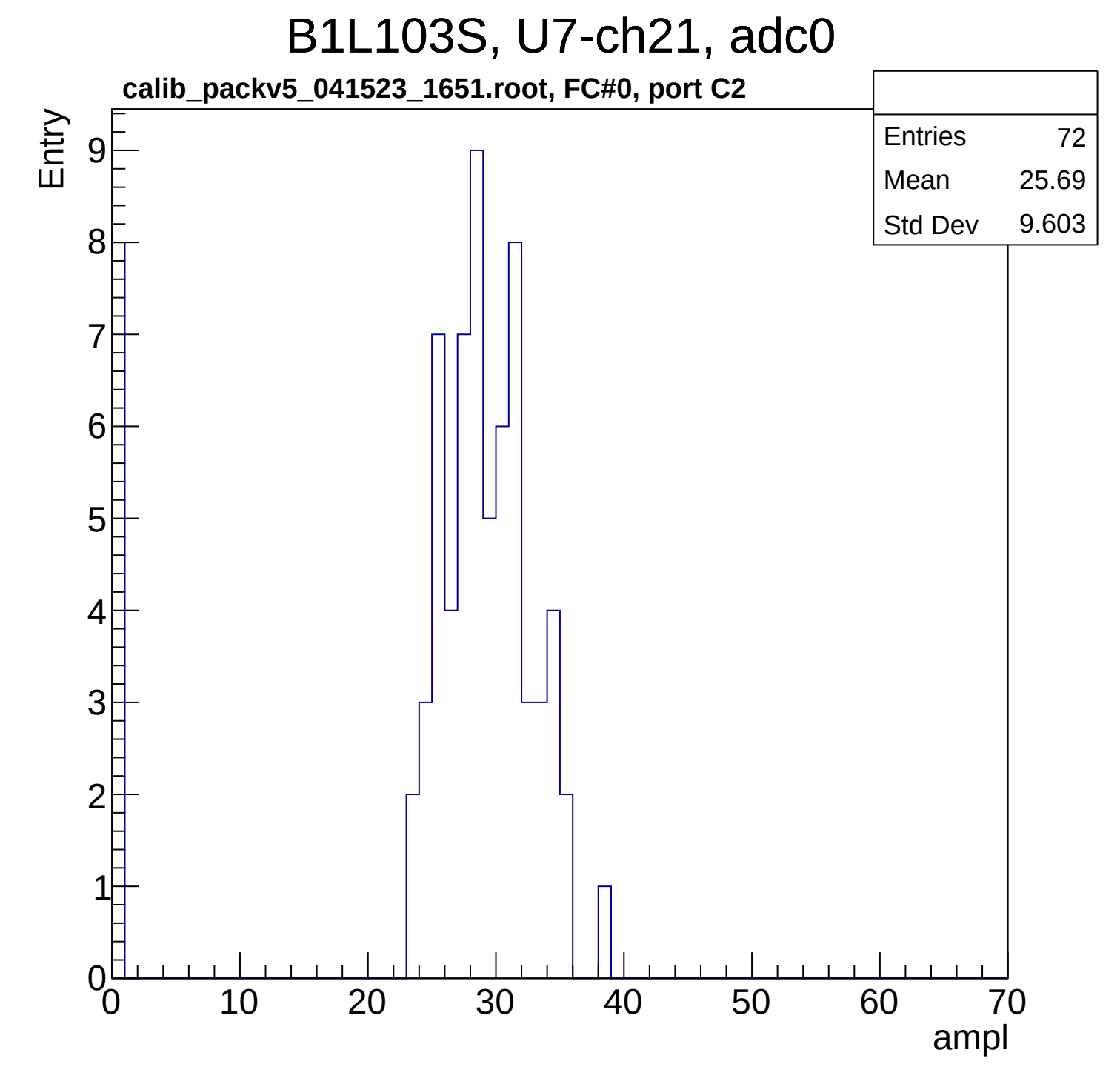
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch21, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 25.69
Std Dev 9.603
Entry
ampl
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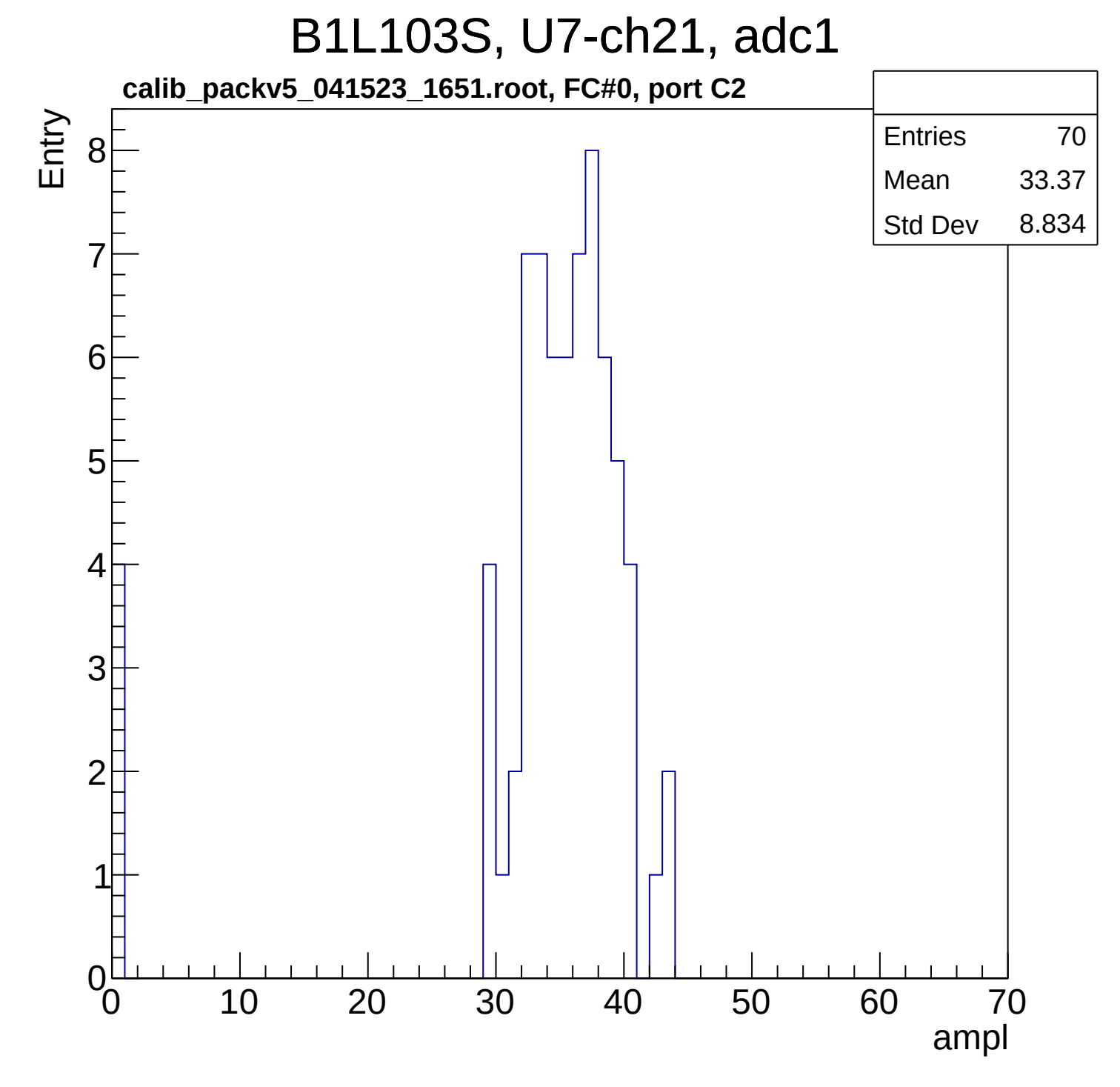
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U7-ch21, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 33.37
Std Dev 8.834
Entry
ampl
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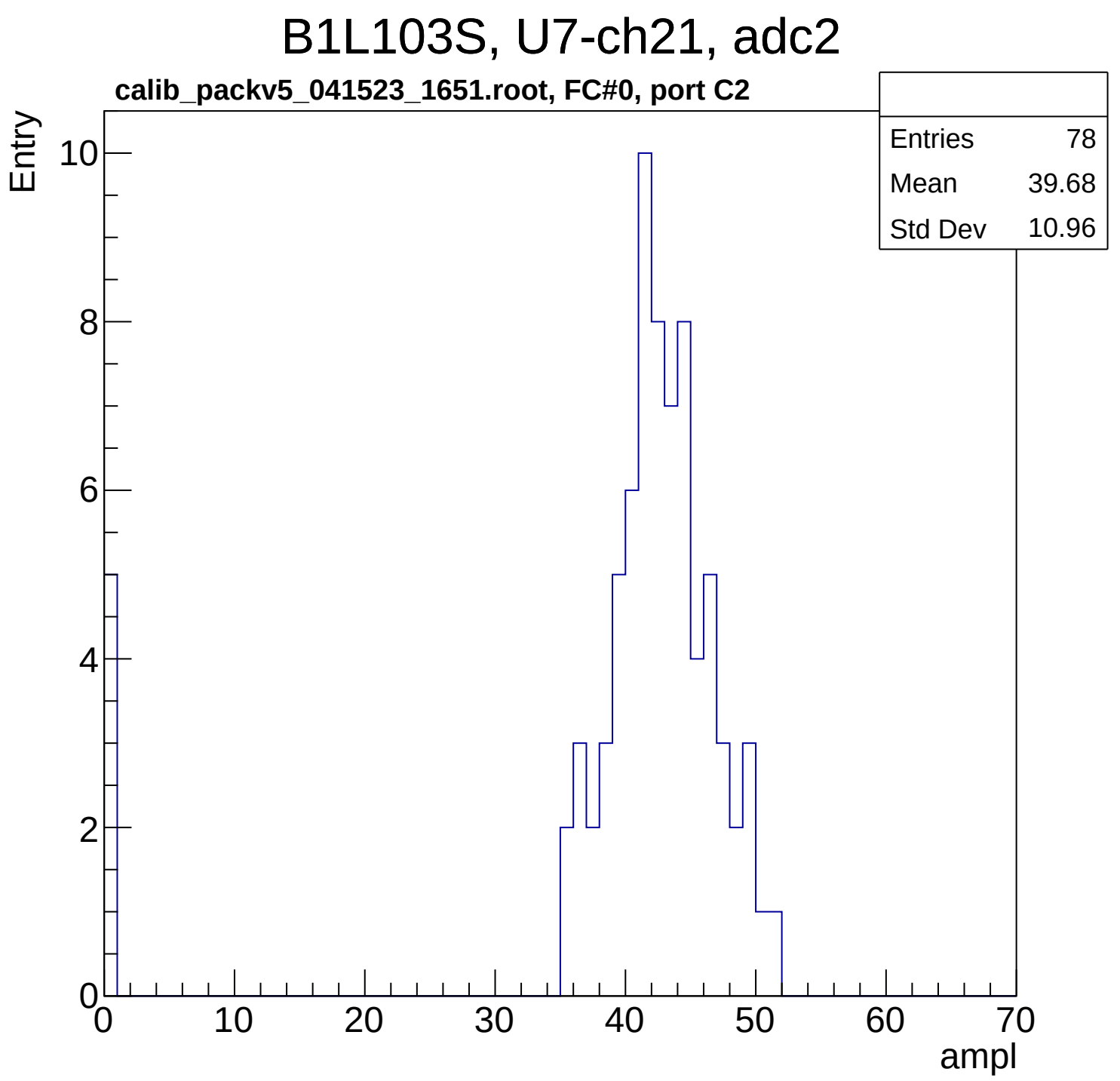
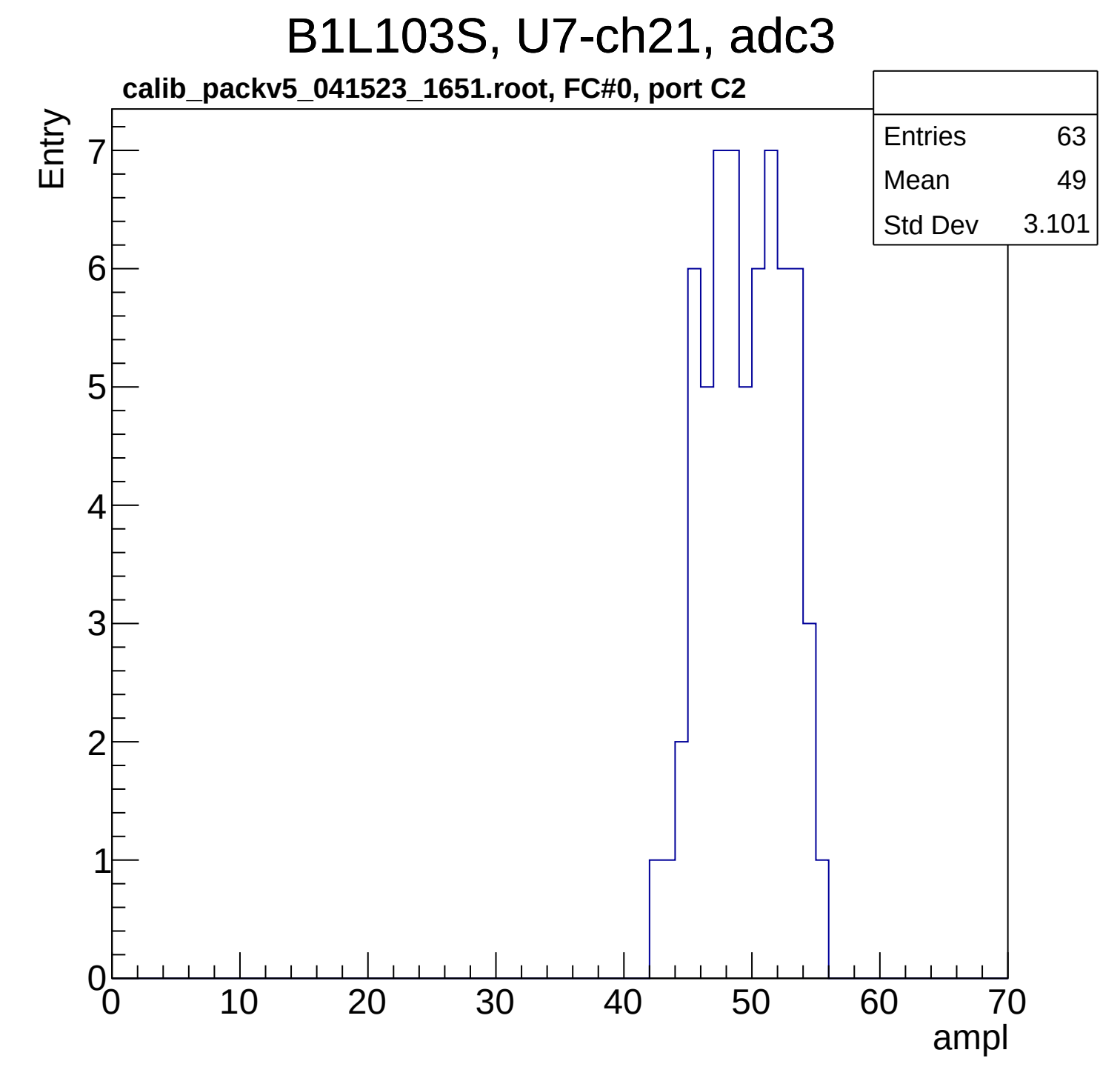
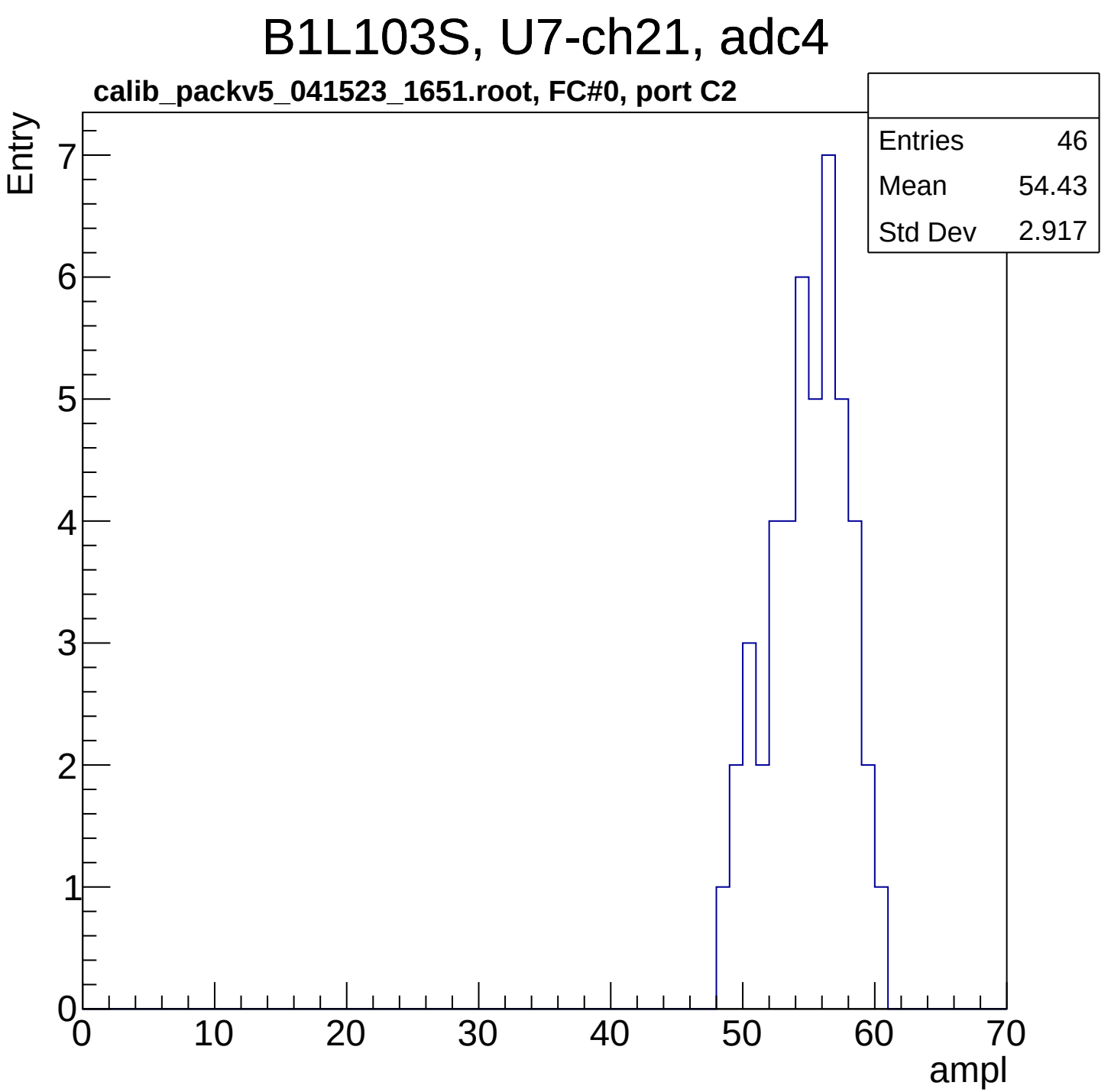
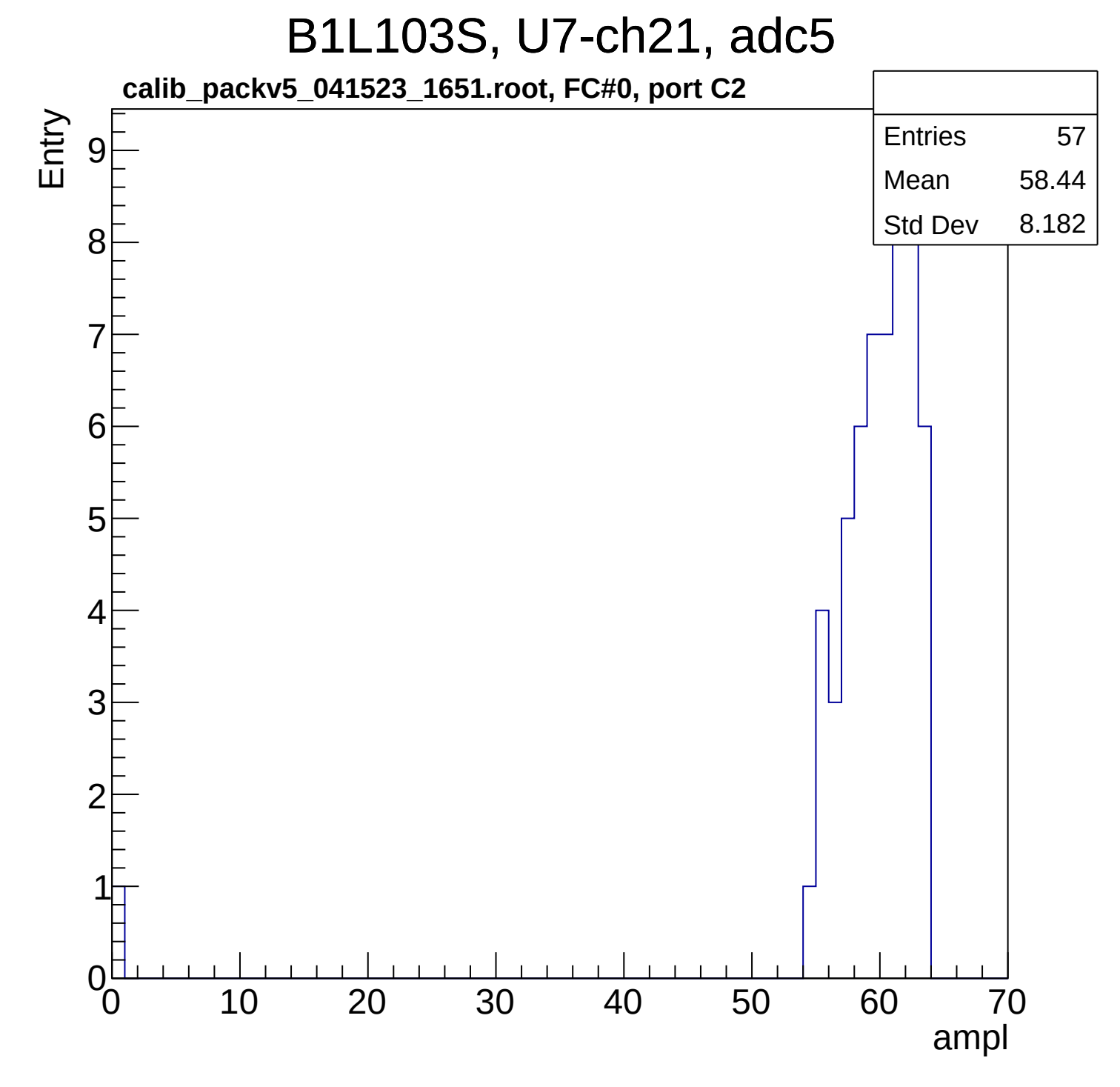
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch21, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 39.68
Std Dev 10.96
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U7-ch21, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 49
Std Dev 3.101
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U7-ch21, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 54.43
Std Dev 2.917
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U7-ch21, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 58.44
Std Dev 8.182
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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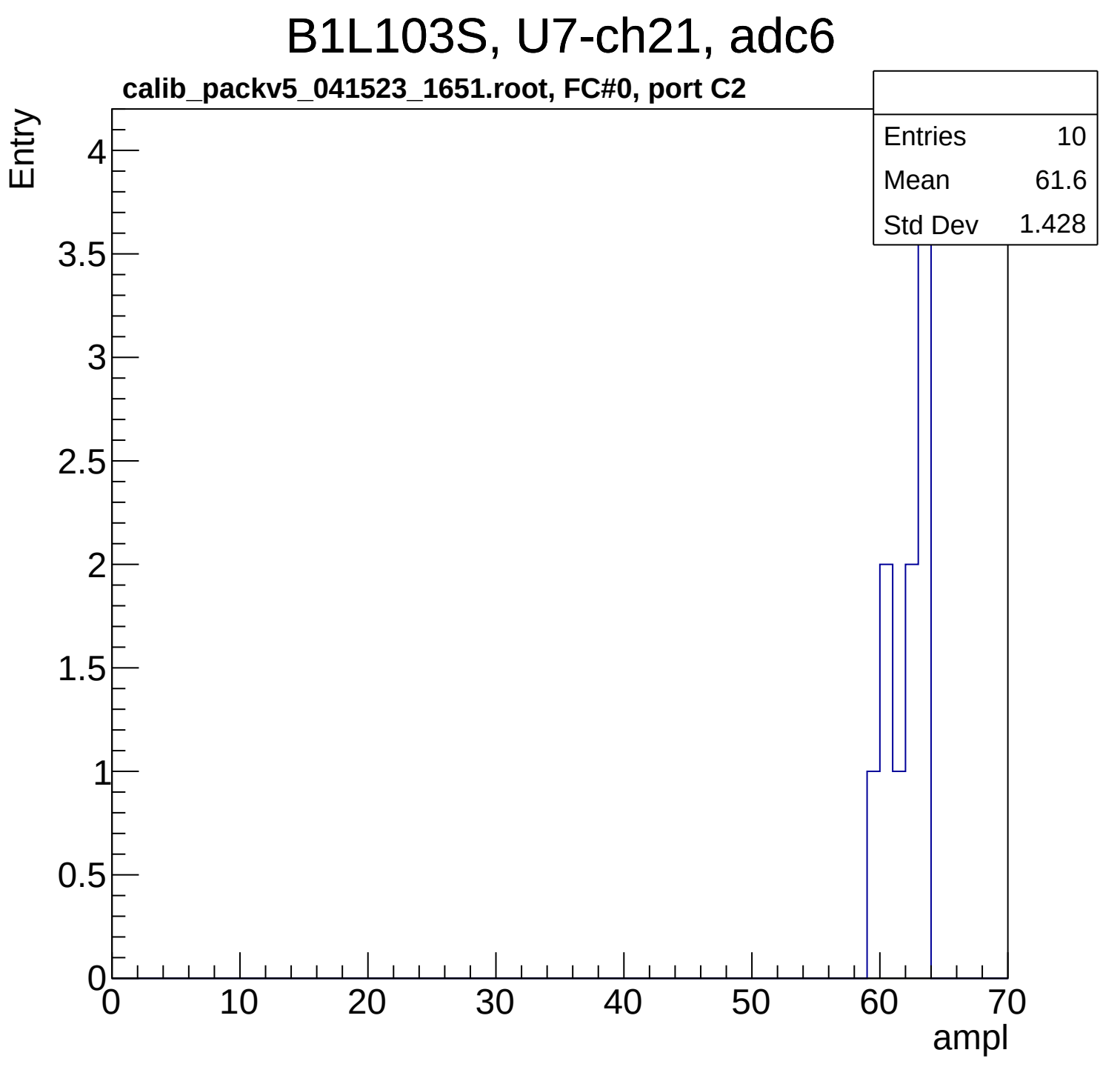
B1L103S, U7-ch21, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 61.6
Std Dev 1.428
Entry
ampl
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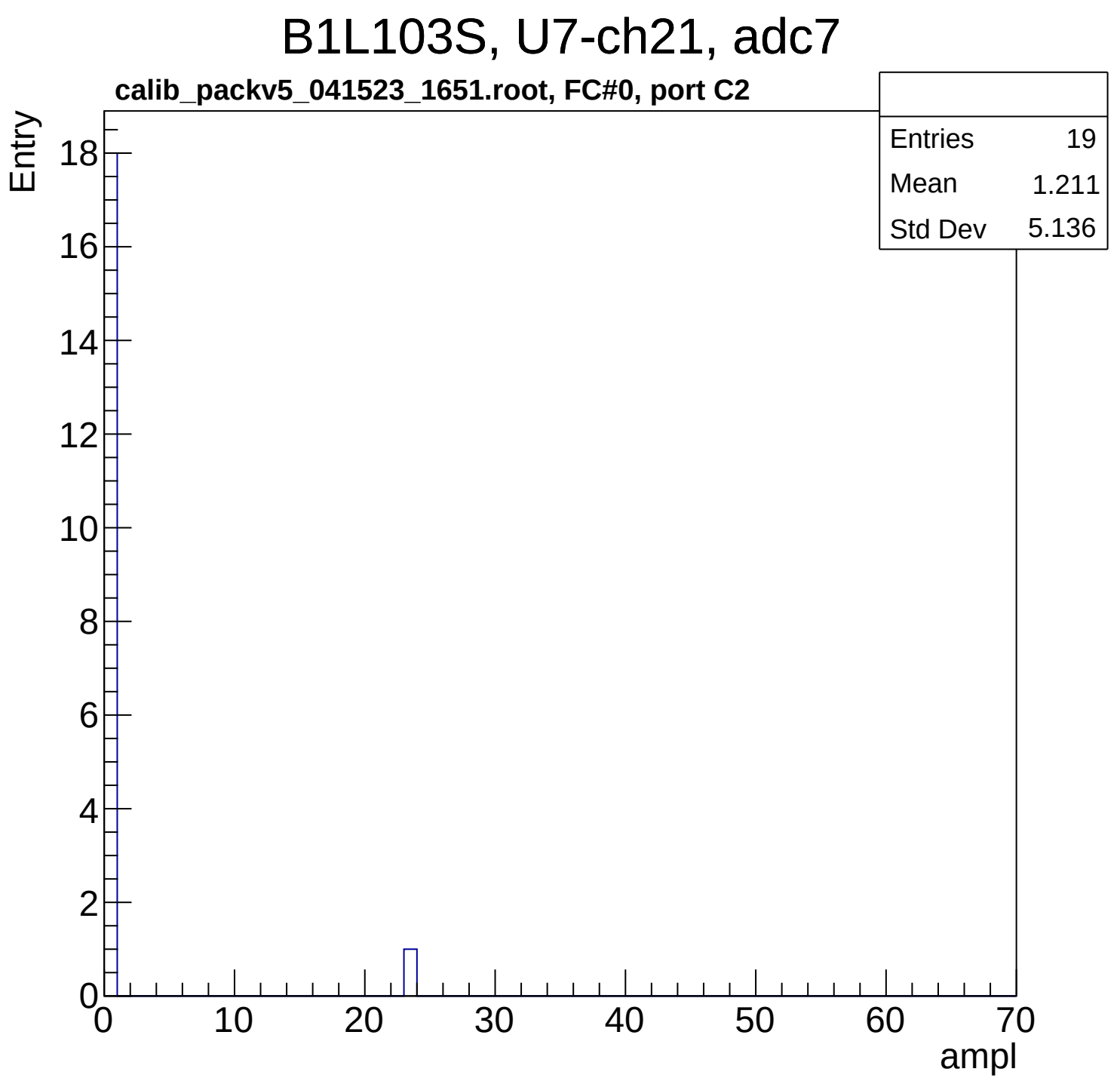
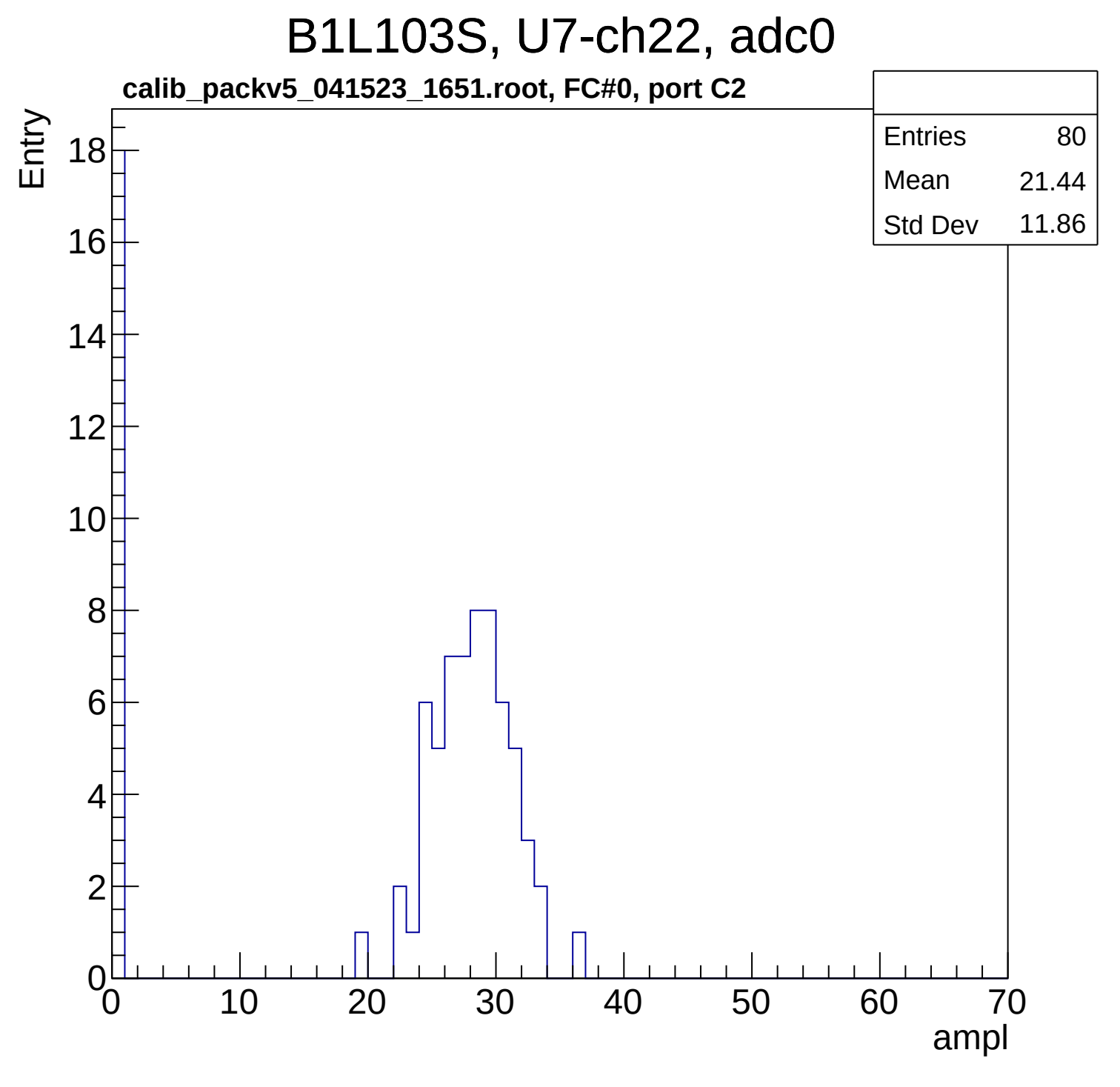
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U7-ch21, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.211
Std Dev 5.136
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch22, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 21.44
Std Dev 11.86
Entry
ampl
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6
8
10
12
14
16
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0
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20
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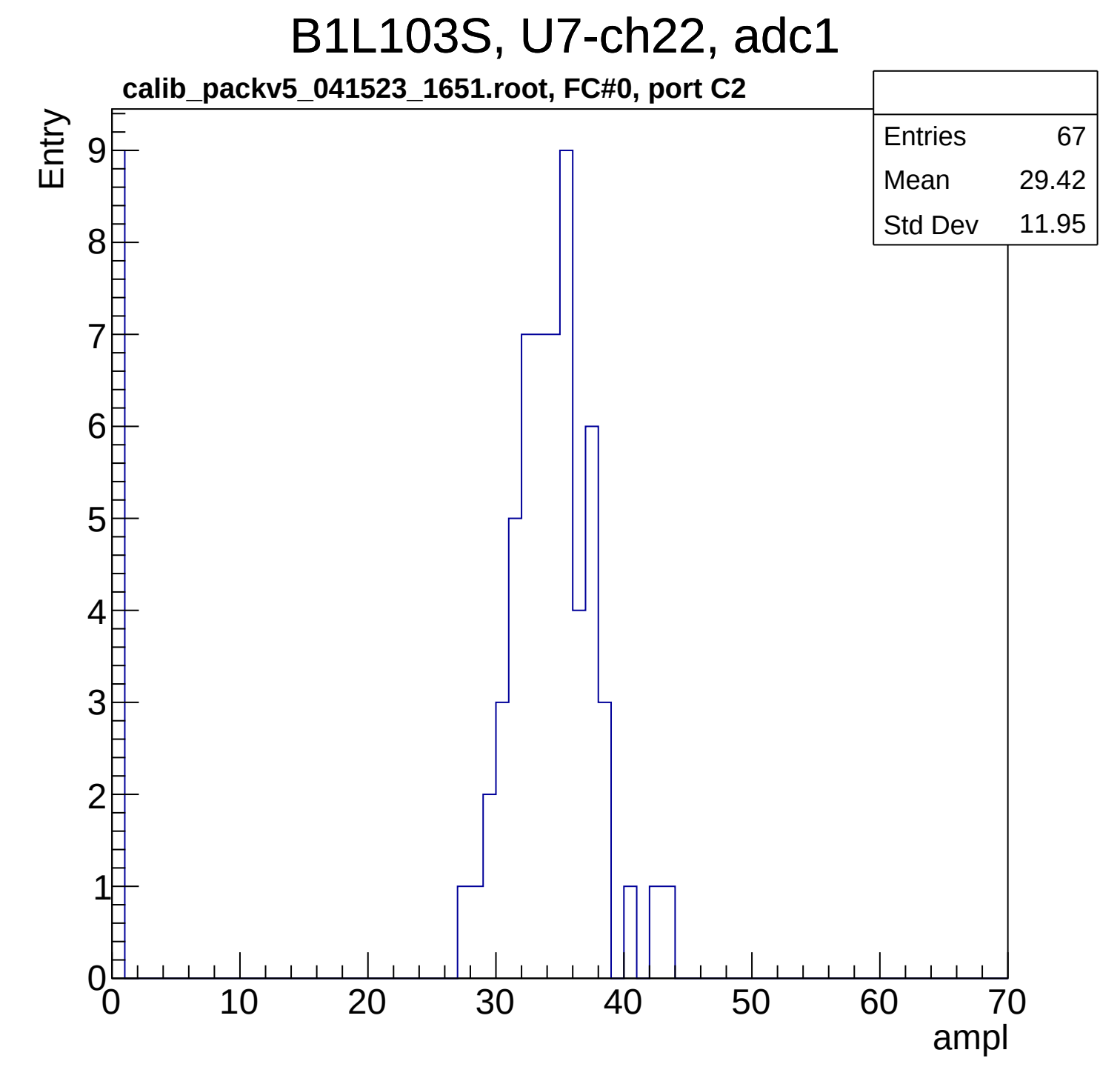
40
50
60
70


B1L103S, U7-ch22, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 29.42
Std Dev 11.95
Entry
ampl
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3
4
5
6
7
8
9
0
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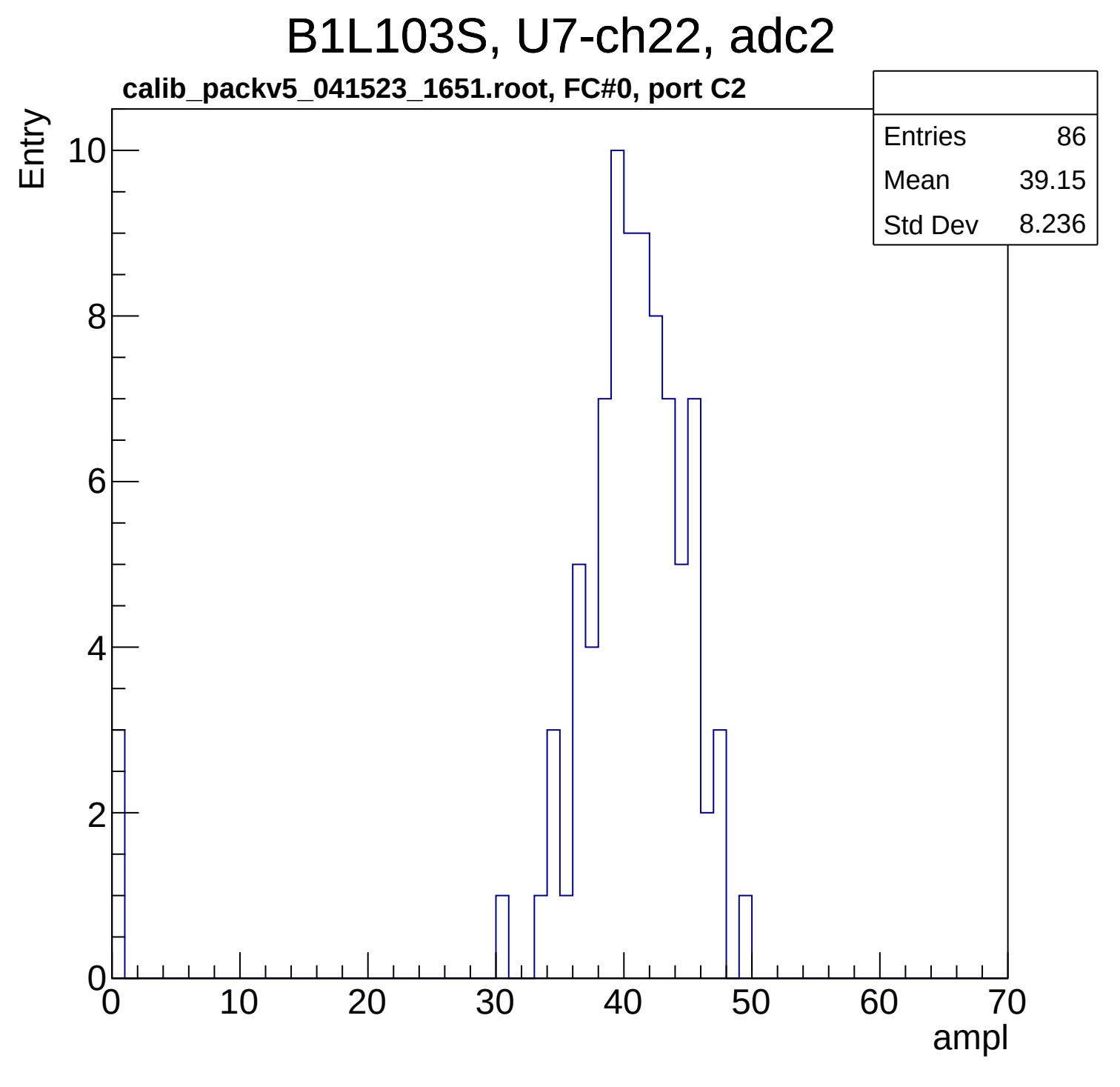
20
30
40
50
60
70


B1L103S, U7-ch22, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 39.15
Std Dev 8.236
Entry
ampl
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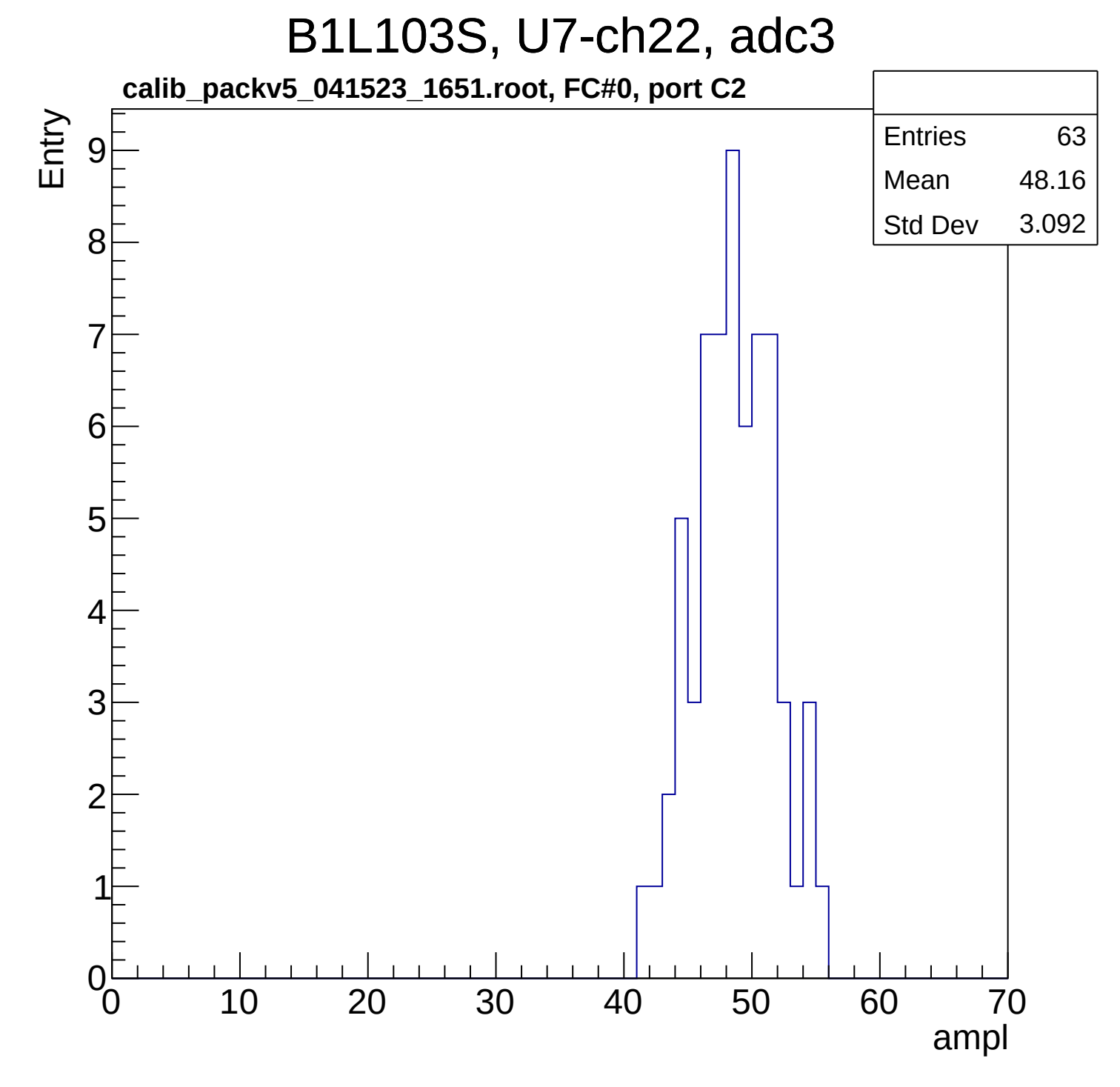
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U7-ch22, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 48.16
Std Dev 3.092
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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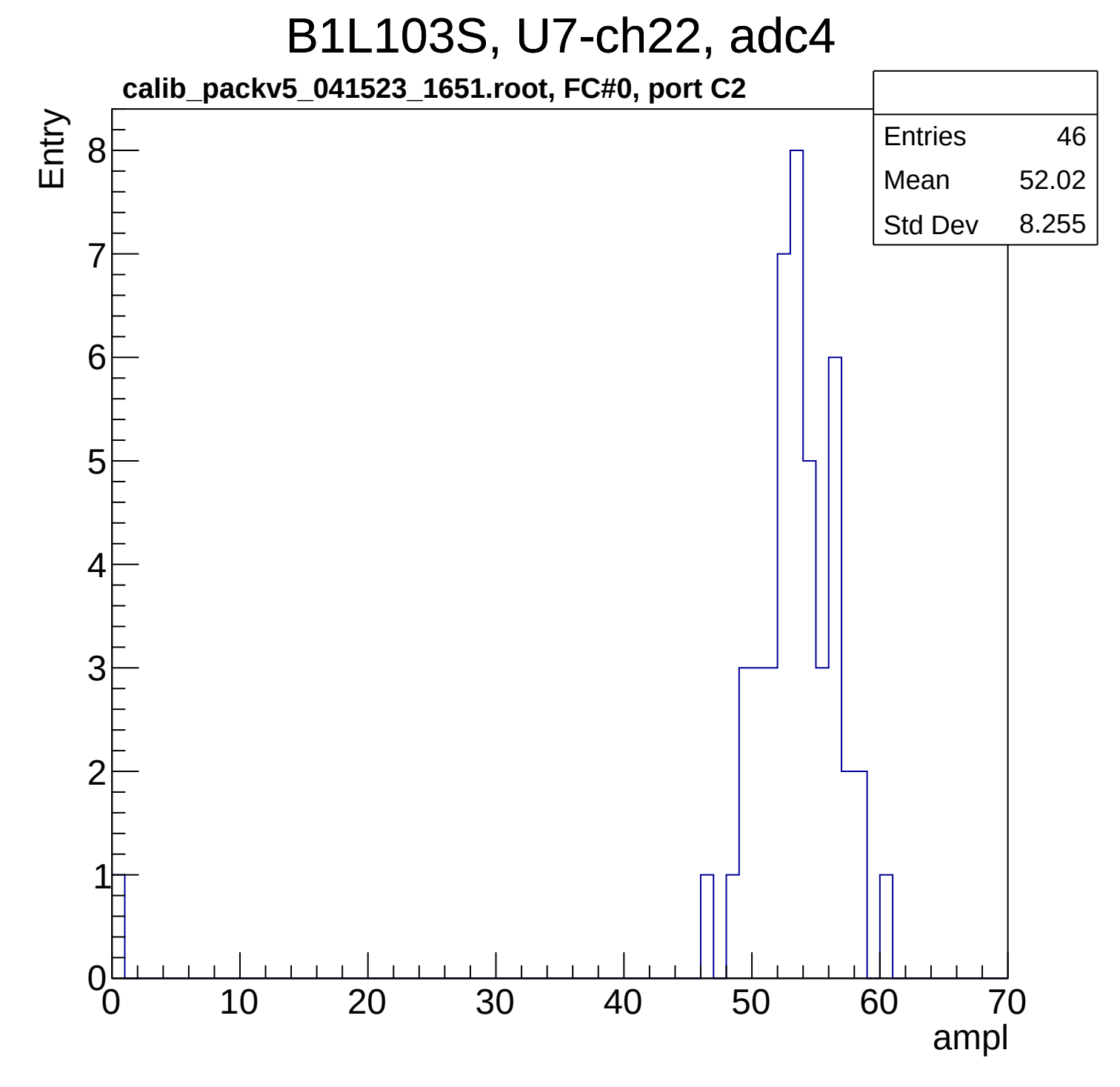
40
50
60
70


B1L103S, U7-ch22, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 52.02
Std Dev 8.255
Entry
ampl
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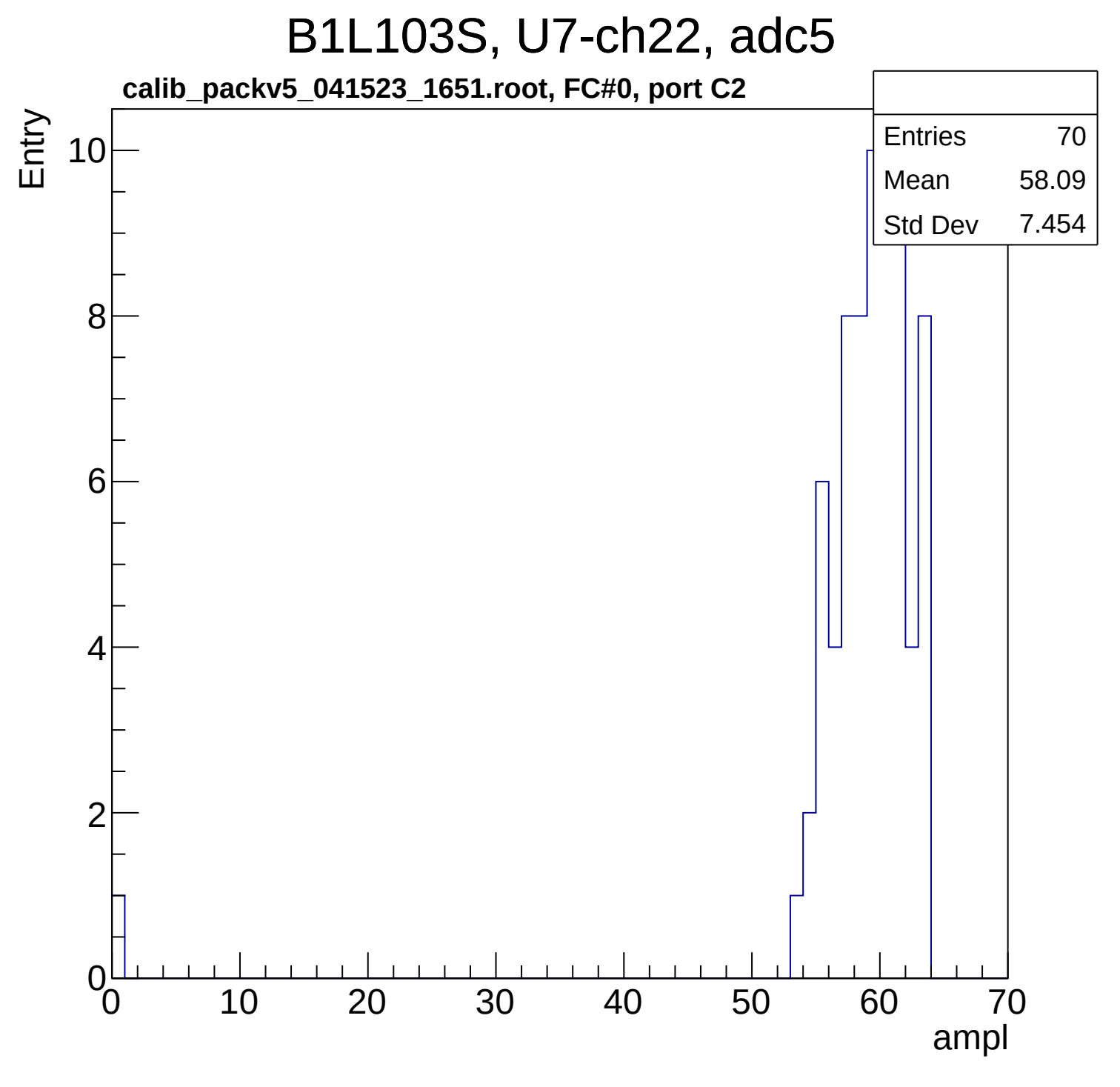
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch22, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 58.09
Std Dev 7.454
Entry
ampl
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2
4
6
8
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0
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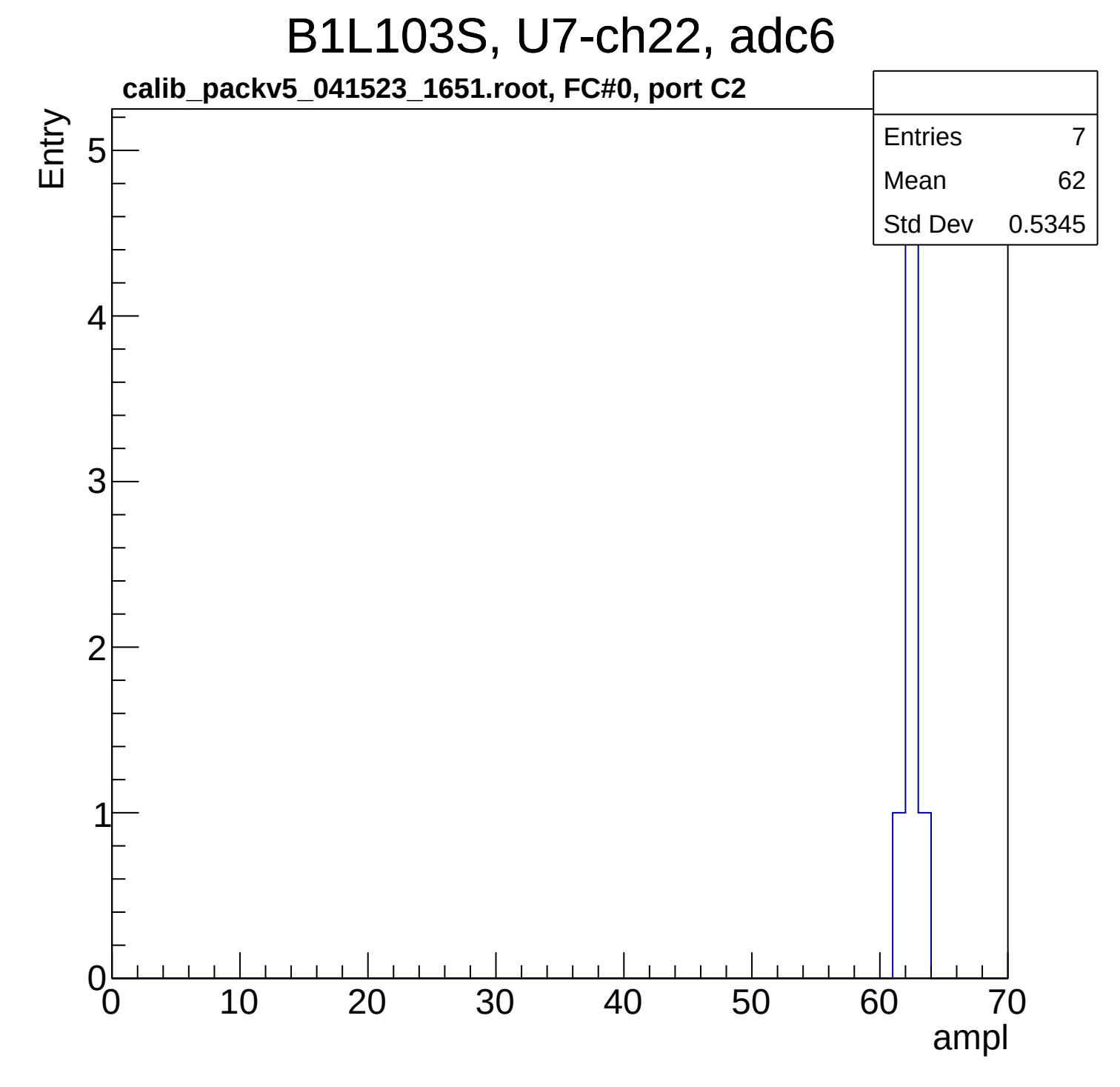
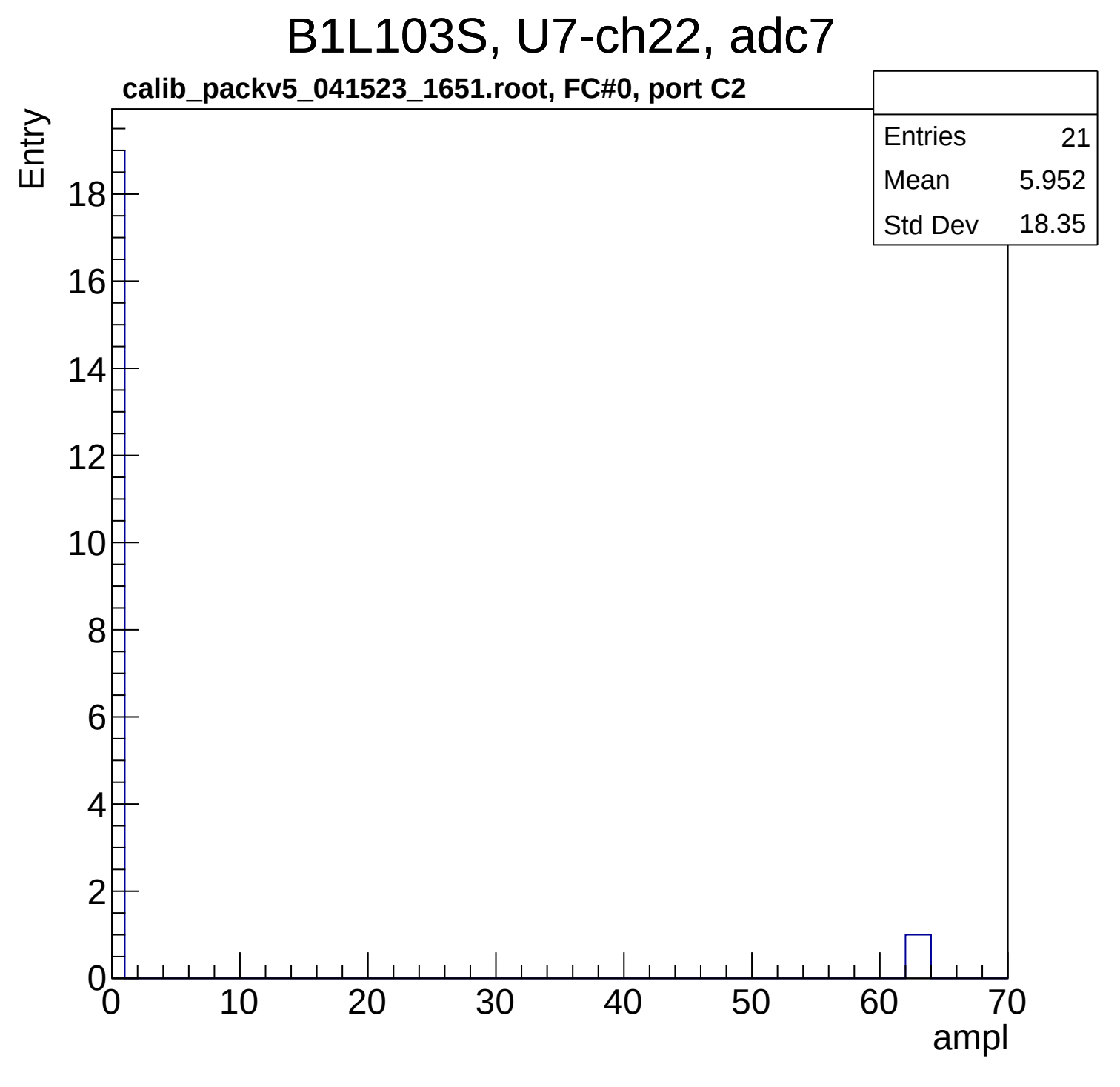
20
30
40
50
60
70


B1L103S, U7-ch22, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 62
Std Dev 0.5345
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U7-ch22, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 5.952
Std Dev 18.35
Entry
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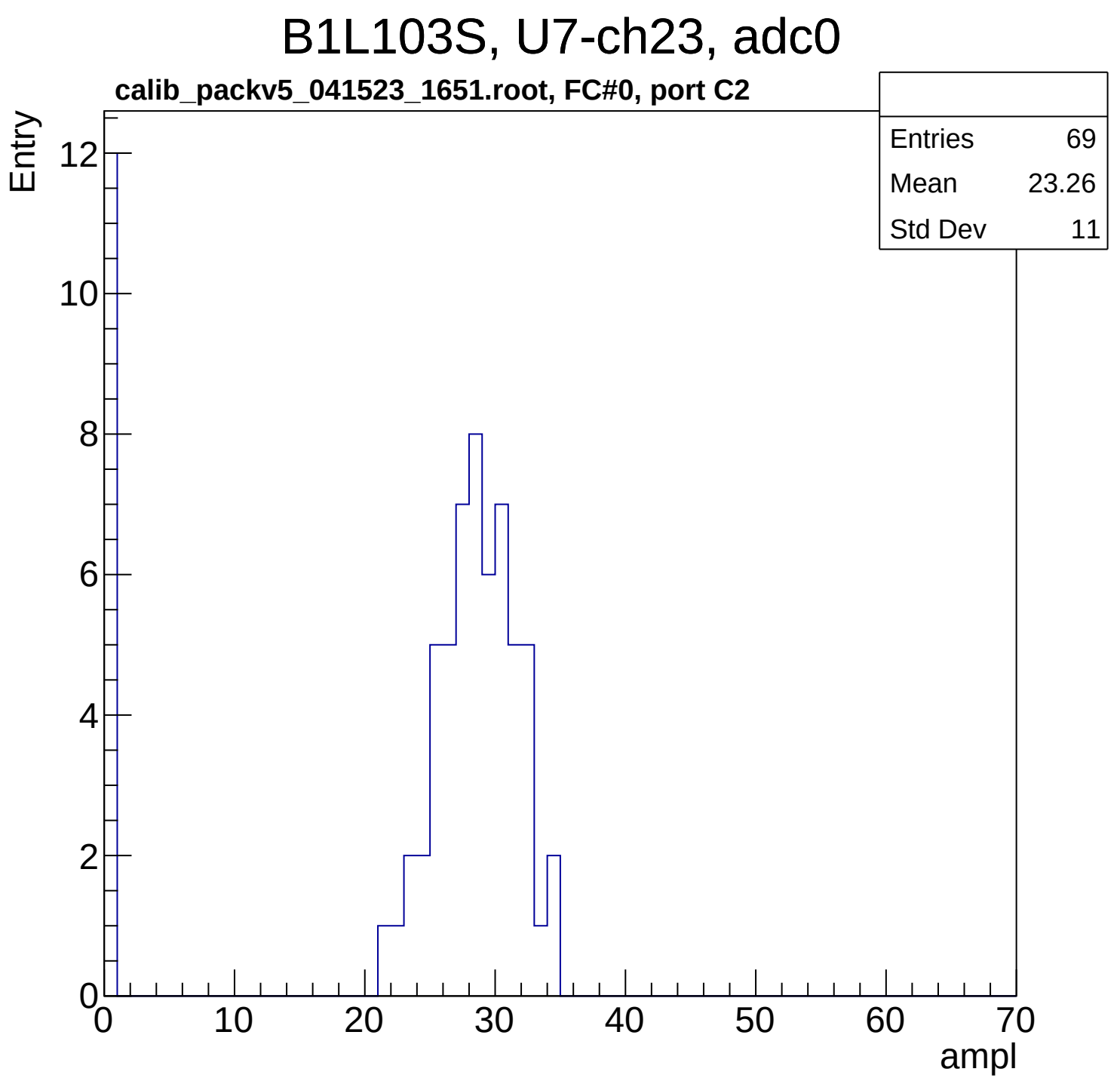
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch23, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 23.26
Std Dev 11
Entry
0
2
4
6
8
10
12
0
10
20
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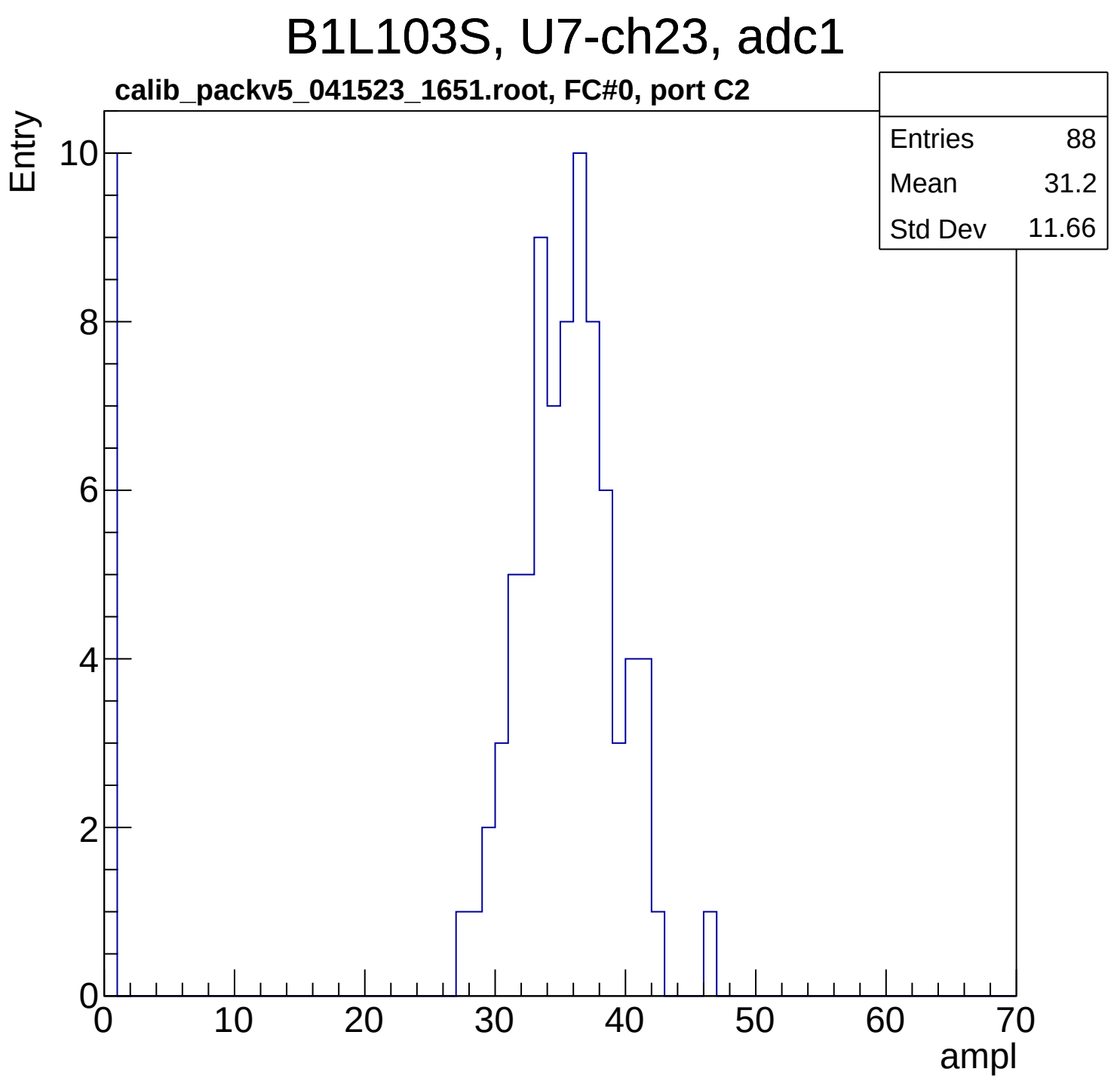
50
60
70
ampl


B1L103S, U7-ch23, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 88
Mean 31.2
Std Dev 11.66
Entry
ampl
0
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4
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10
0
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60
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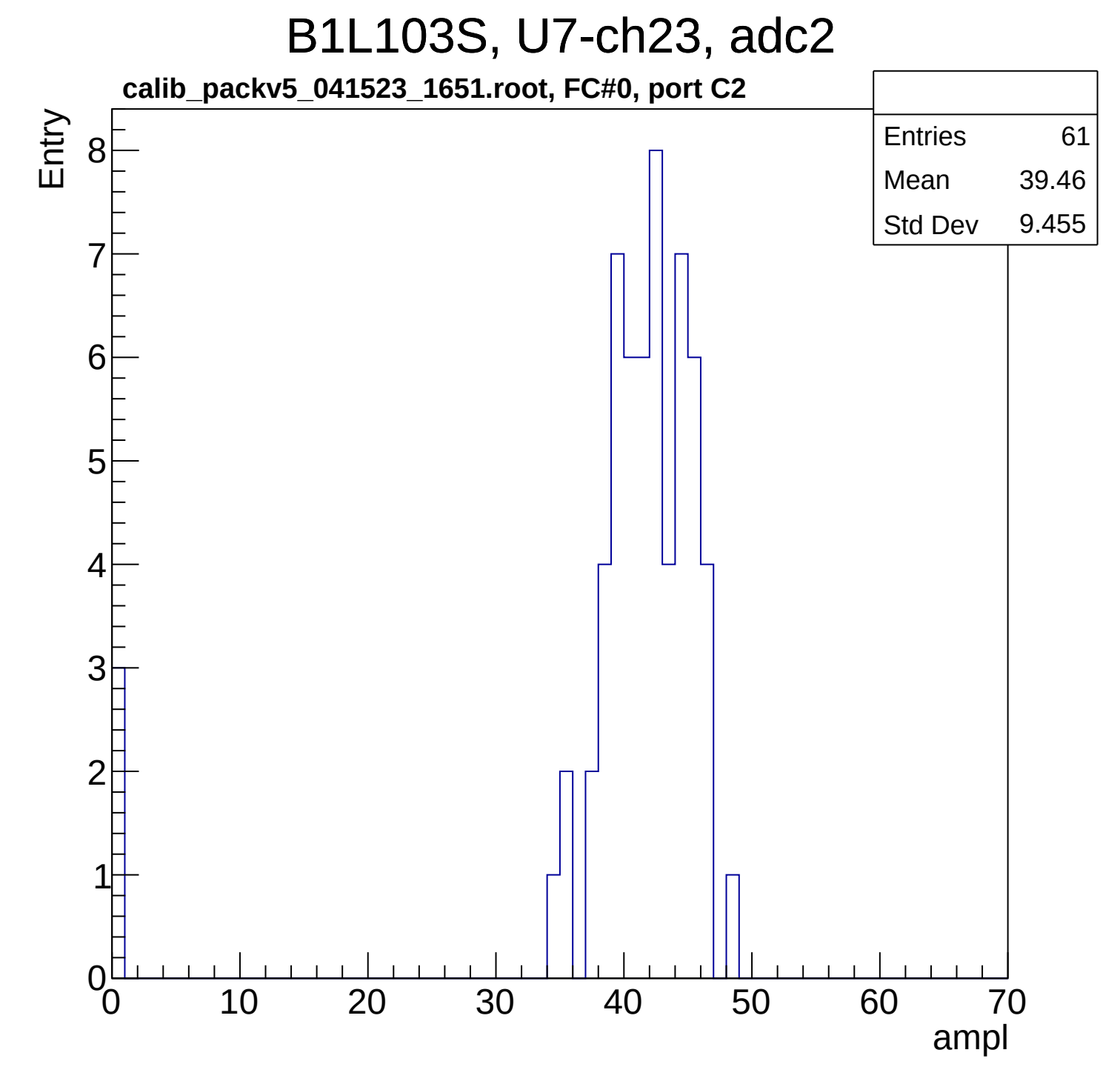
B1L103S, U7-ch23, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 39.46
Std Dev 9.455
Entry
ampl
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1
2
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5
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50
60
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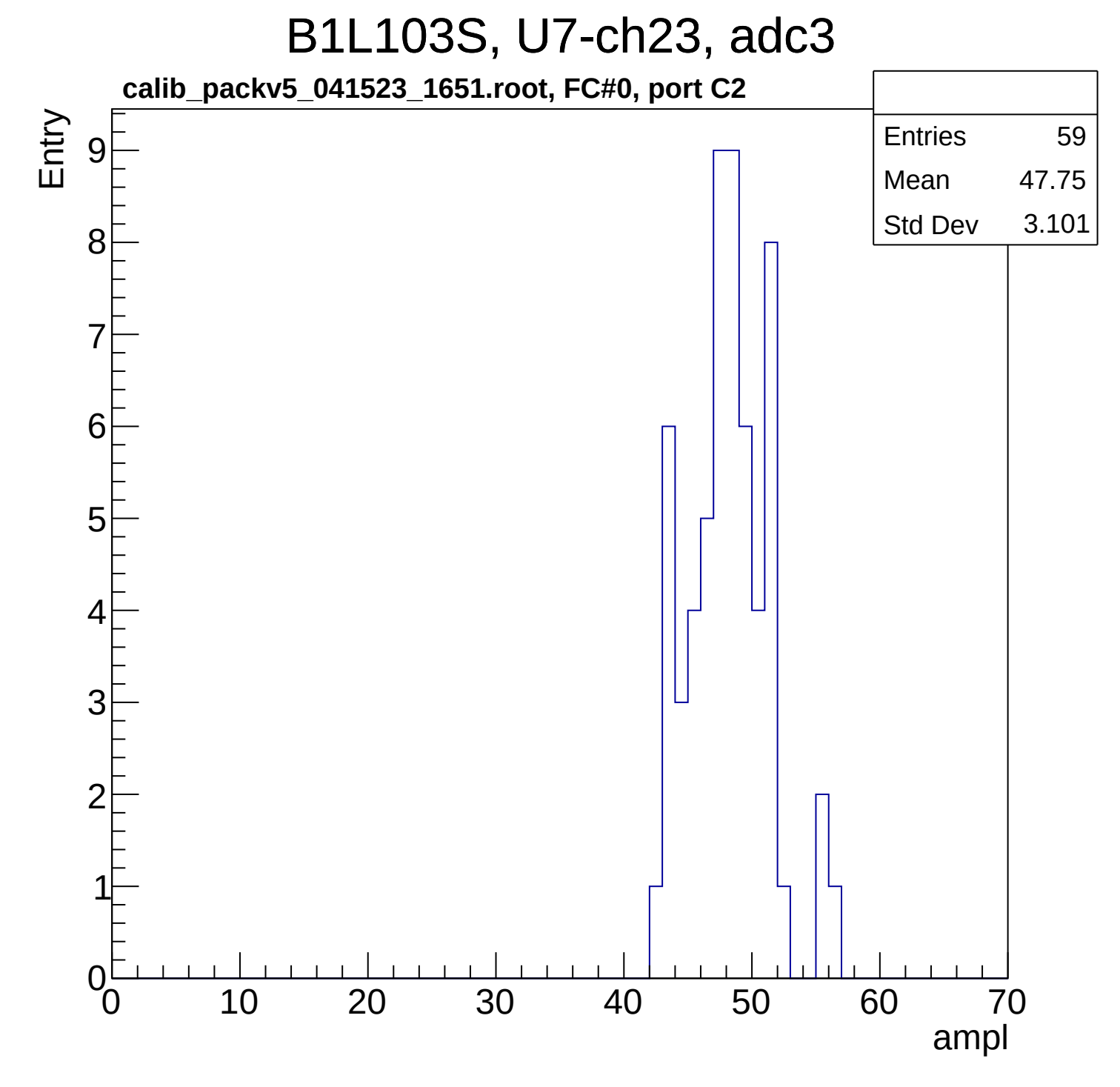
B1L103S, U7-ch23, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 47.75
Std Dev 3.101
Entry
ampl
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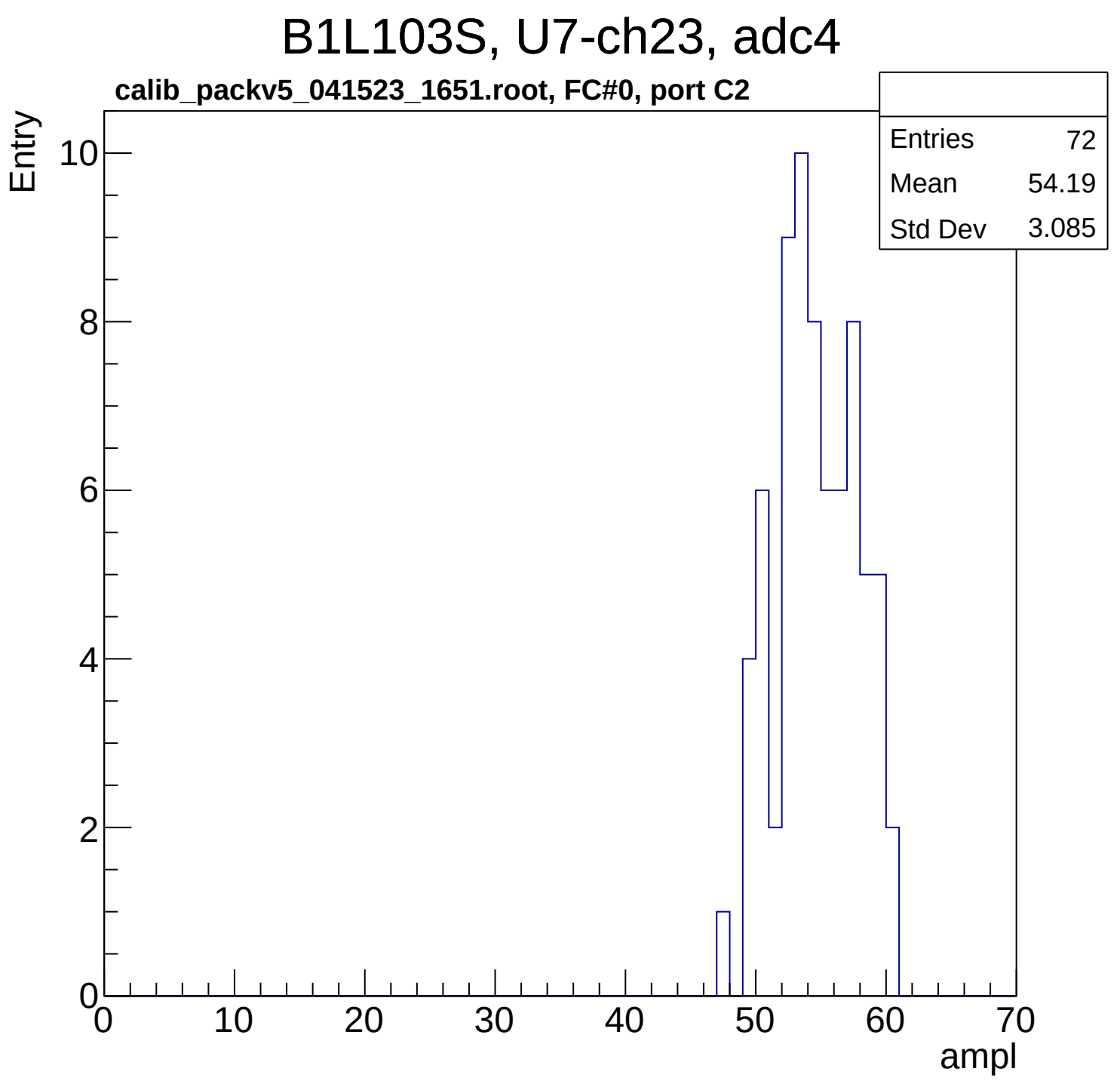
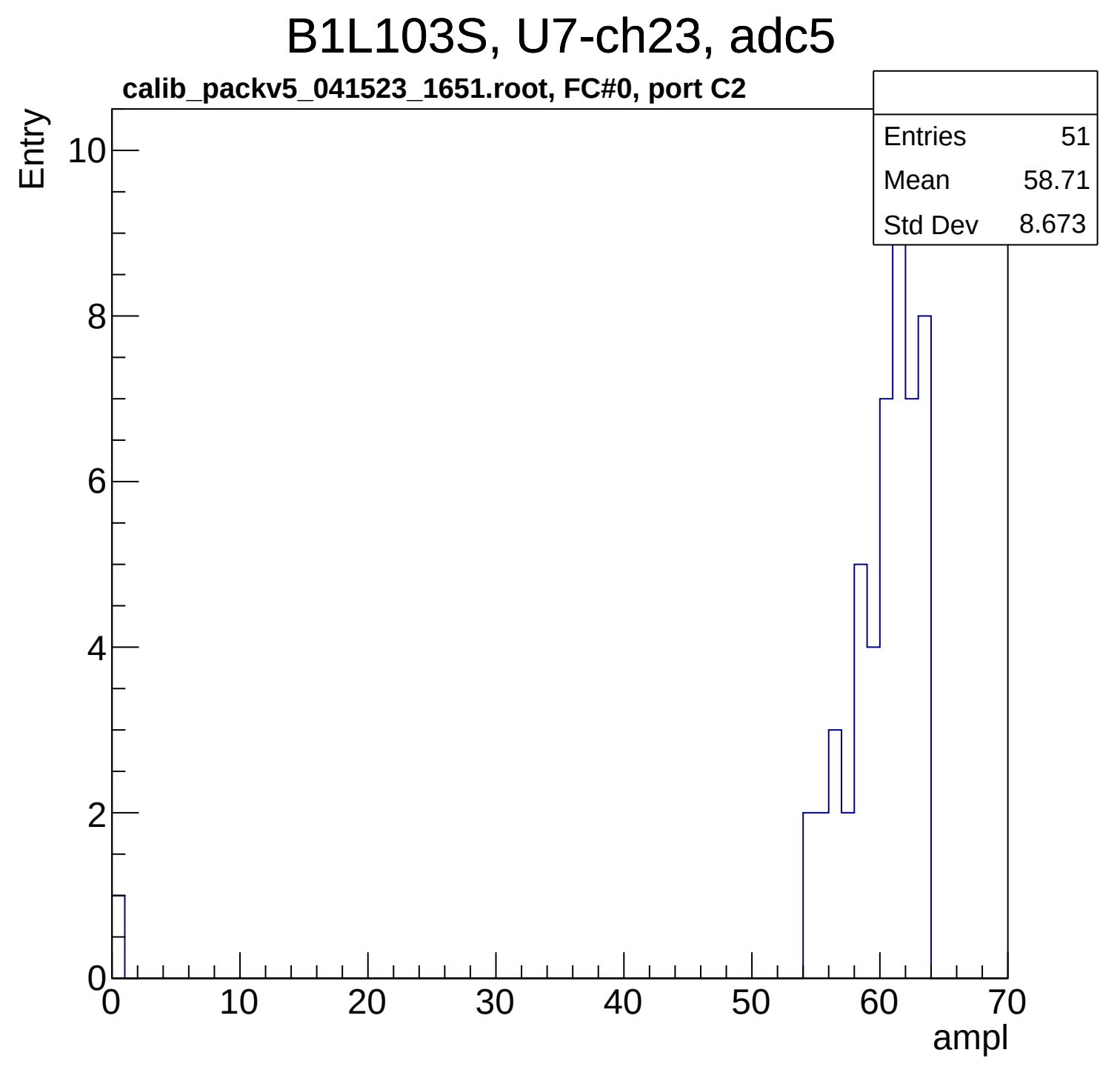
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U7-ch23, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 54.19
Std Dev 3.085
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U7-ch23, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 58.71
Std Dev 8.673
Entry
ampl
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4
6
8
10
0
10
20
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40
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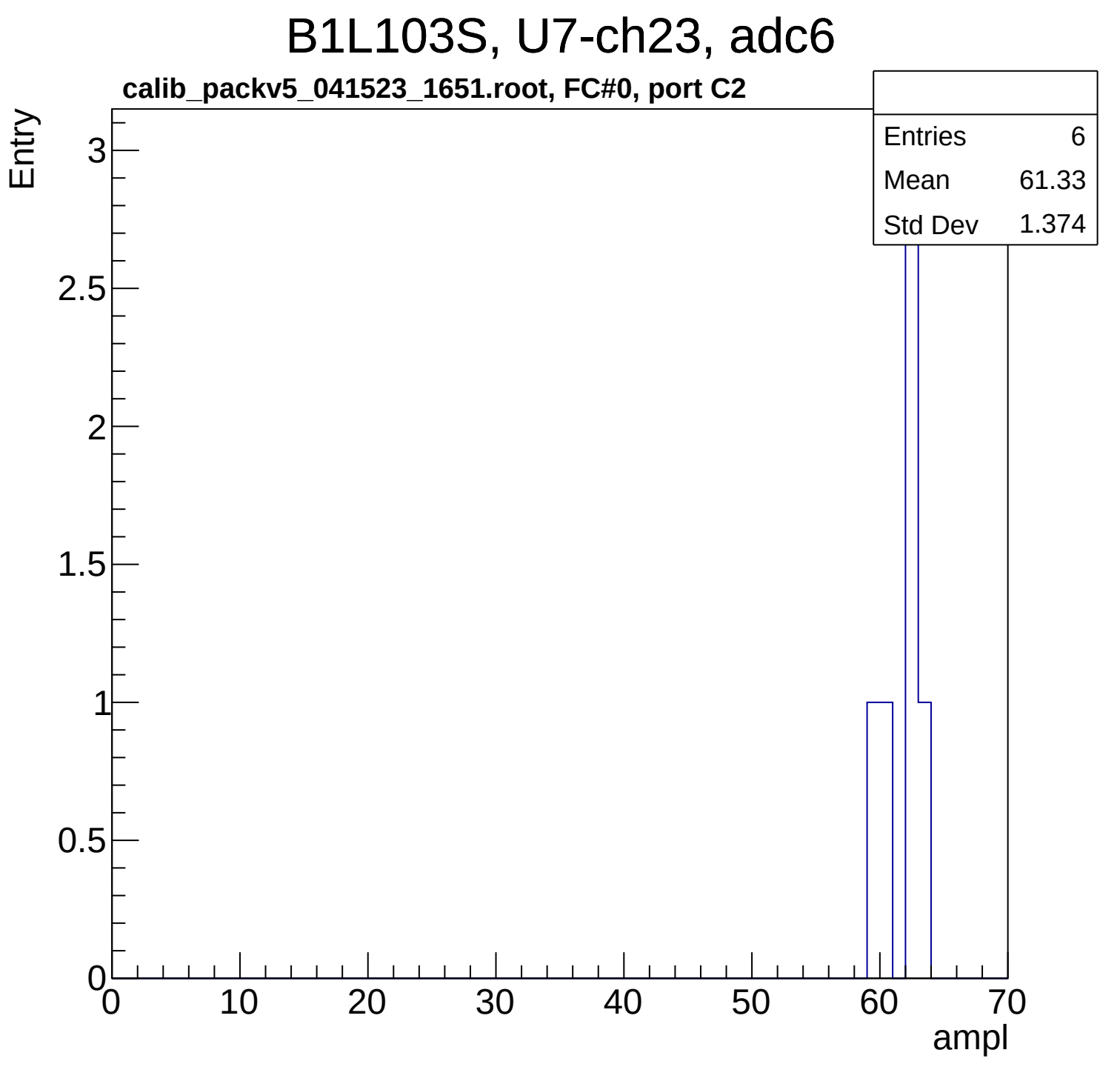
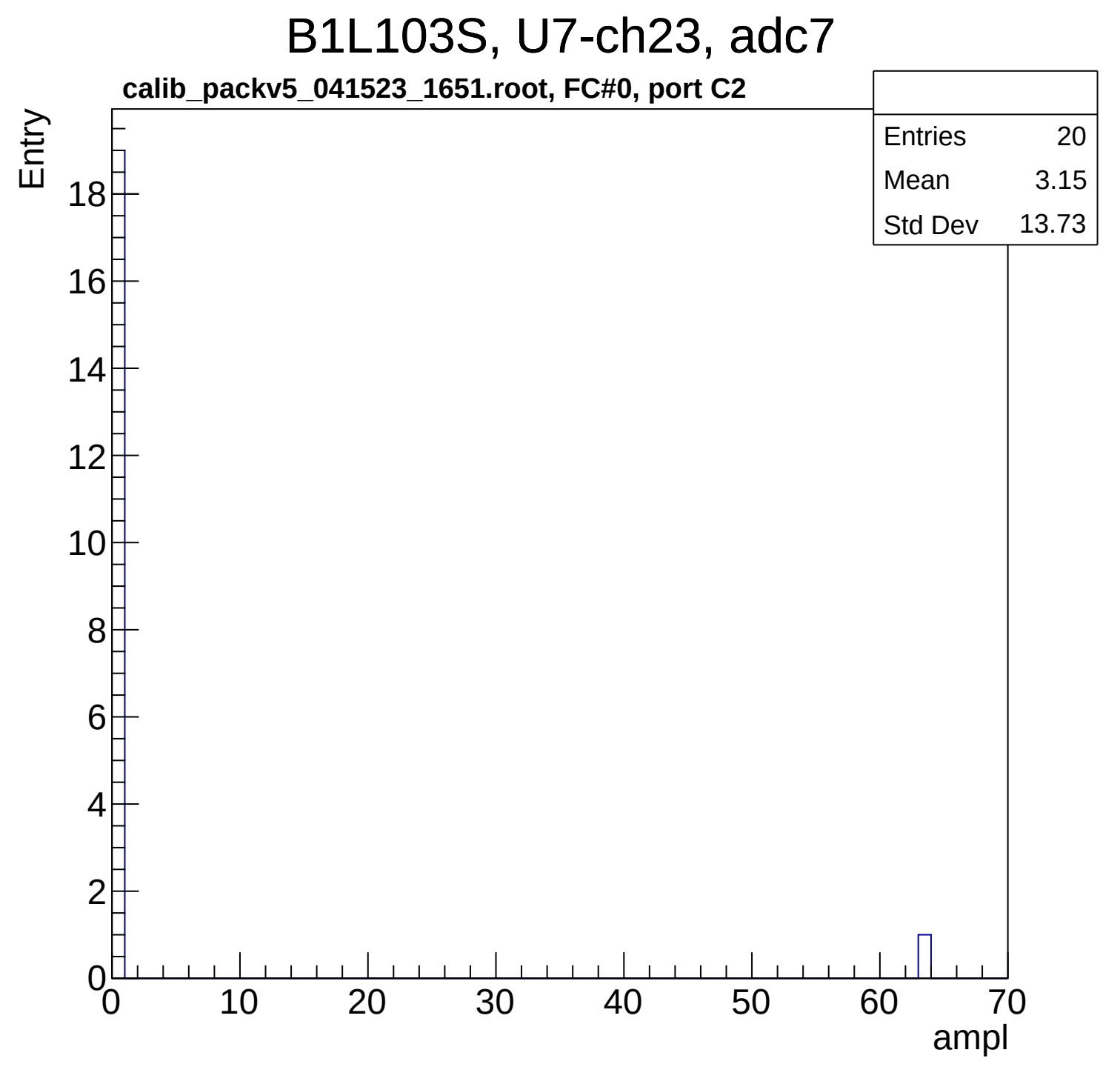
60
70


B1L103S, U7-ch23, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 61.33
Std Dev 1.374
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U7-ch23, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
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4
6
8
10
12
14
16
18
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10
20
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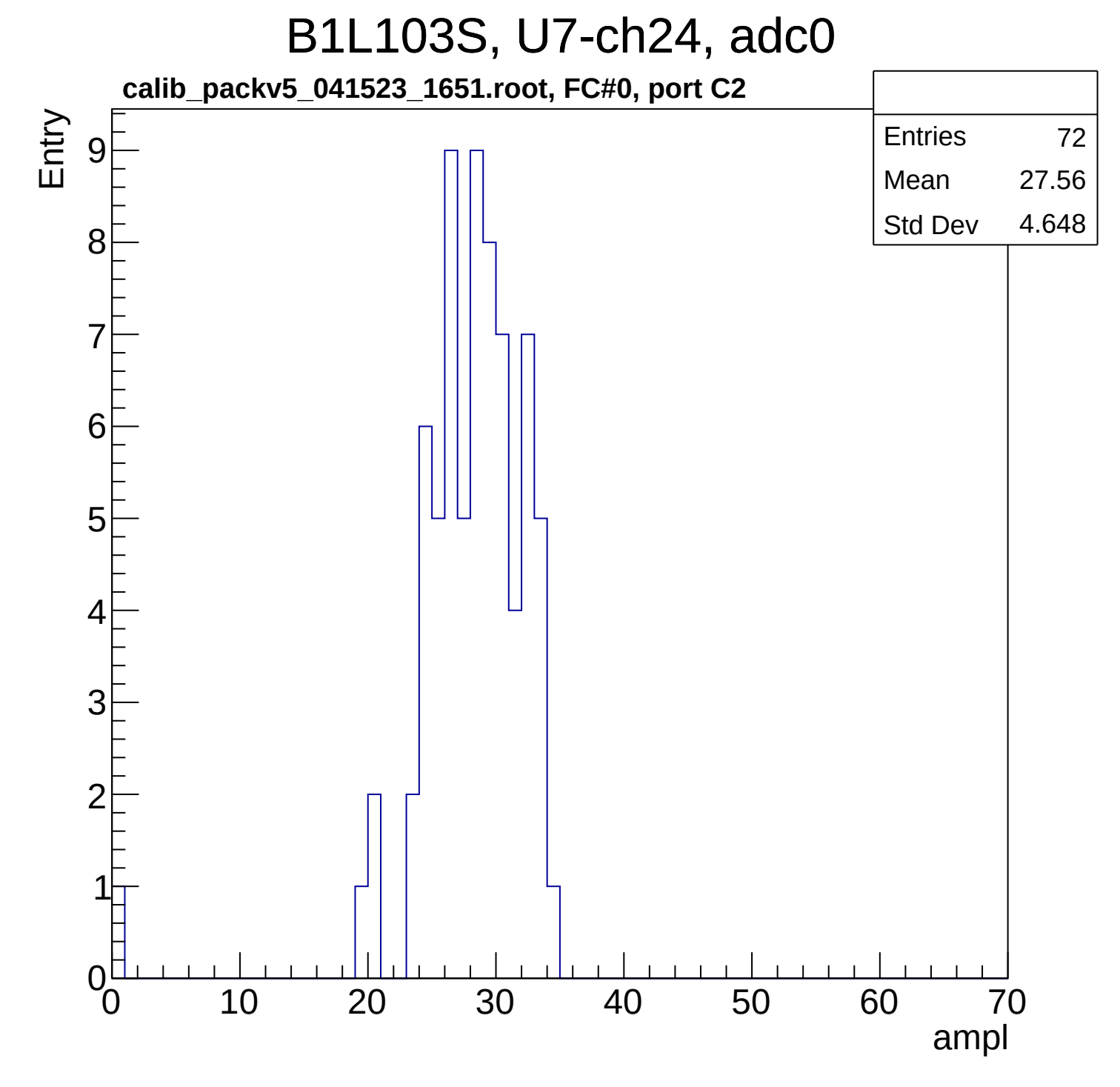
40
50
60
70
ampl


B1L103S, U7-ch24, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 27.56
Std Dev 4.648
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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40
50
60
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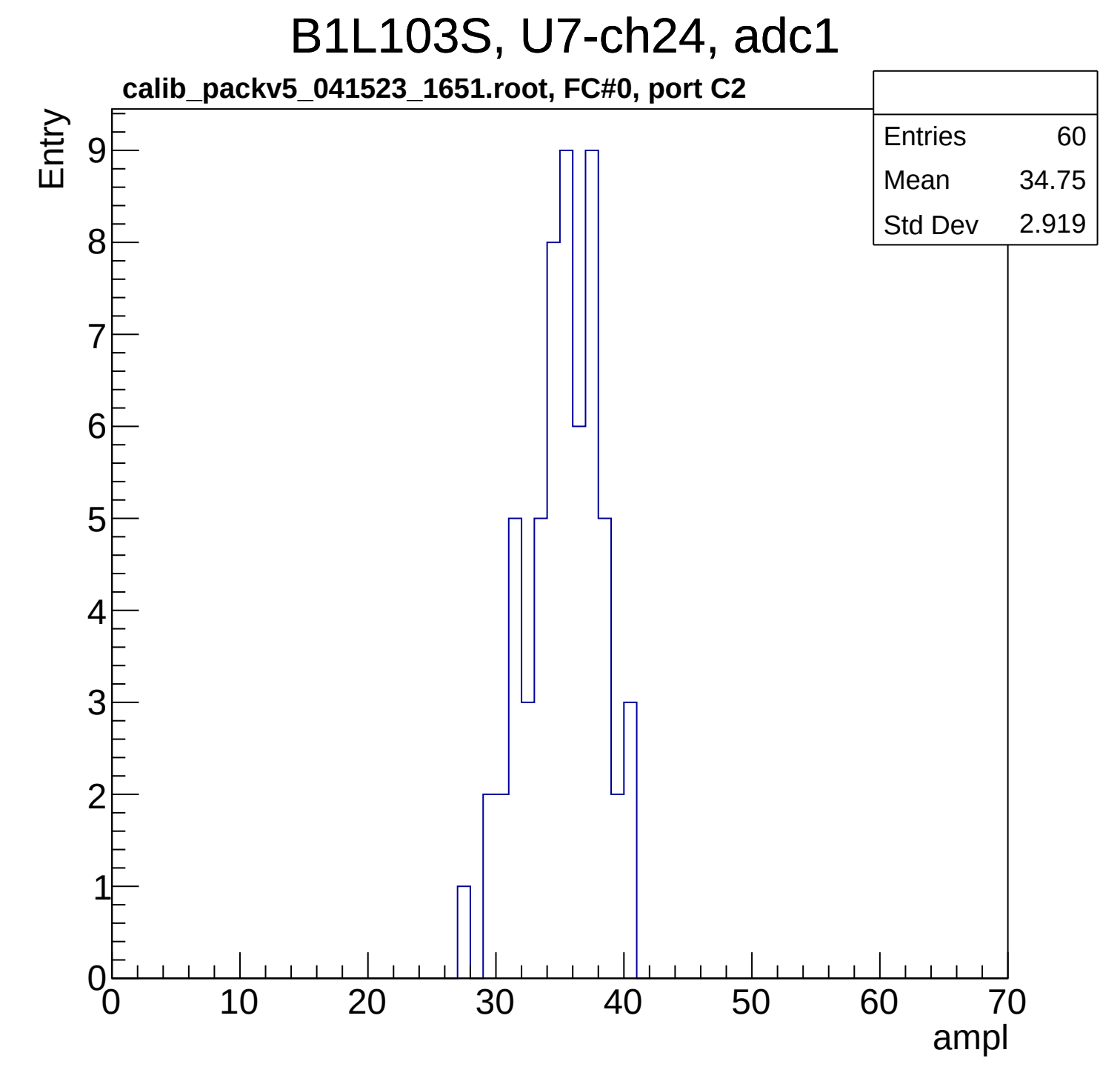
B1L103S, U7-ch24, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 34.75
Std Dev 2.919
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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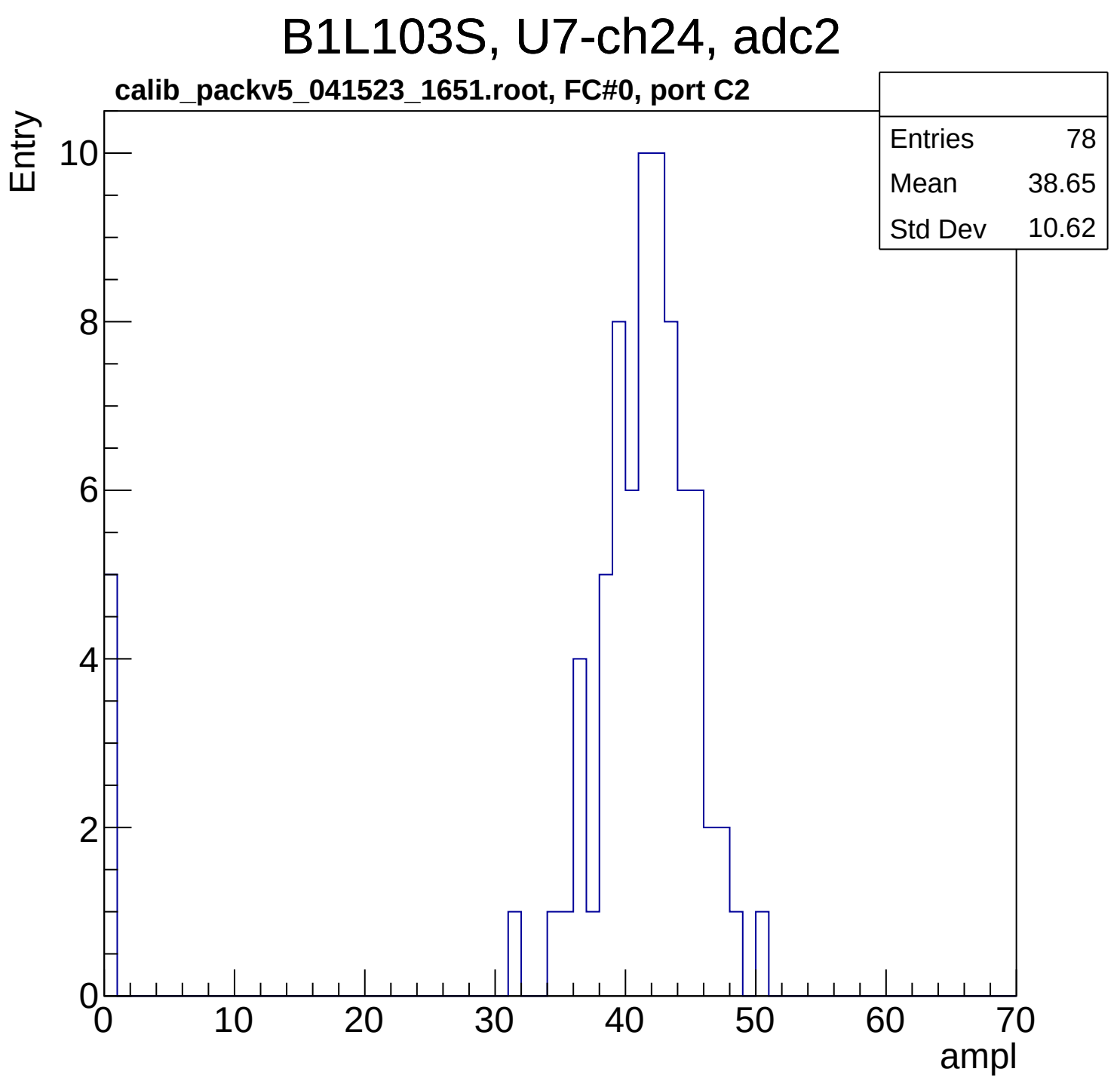
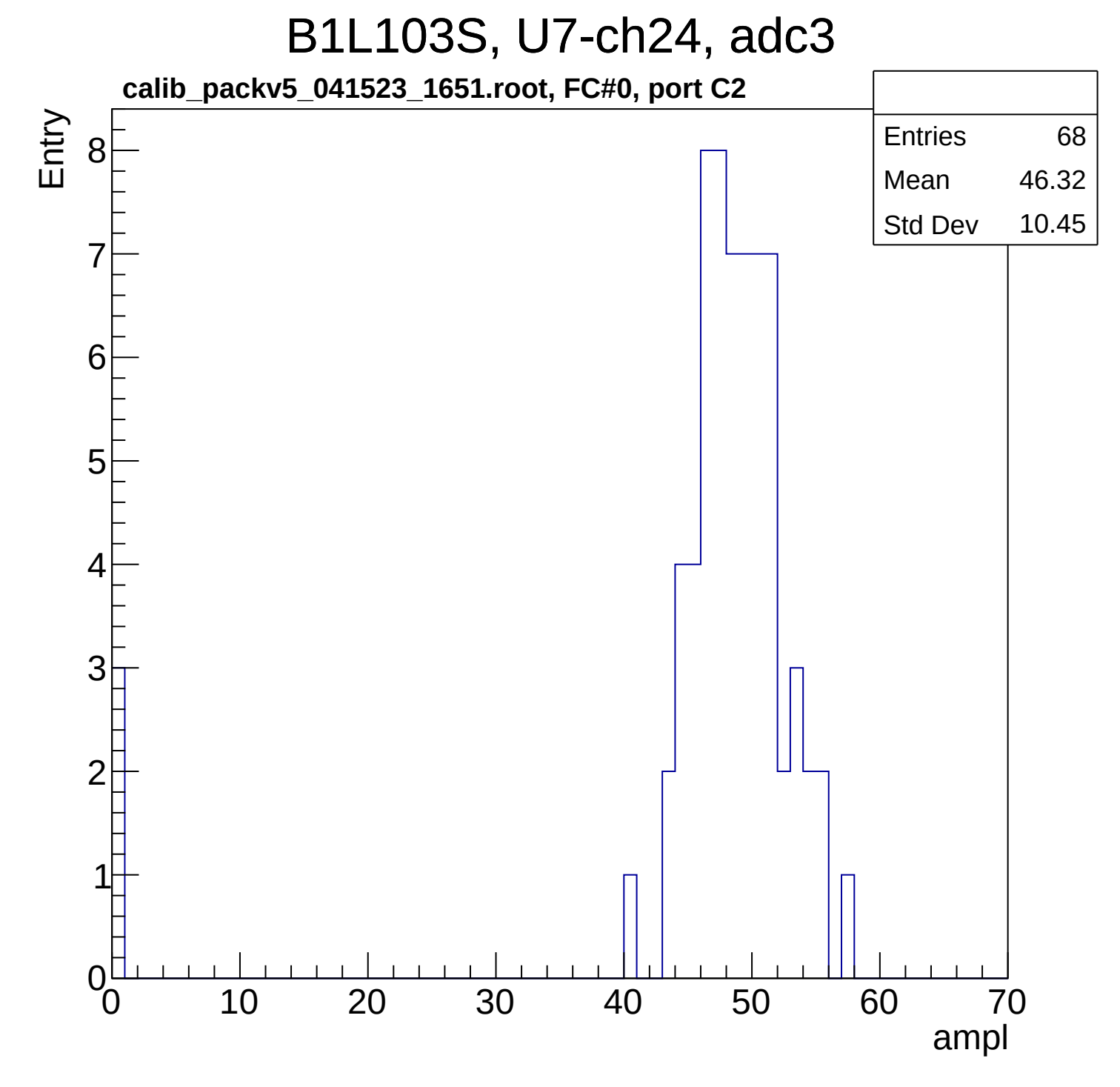

B1L103S, U7-ch24, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 38.65
Std Dev 10.62
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U7-ch24, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 46.32
Std Dev 10.45
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
30
40
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60
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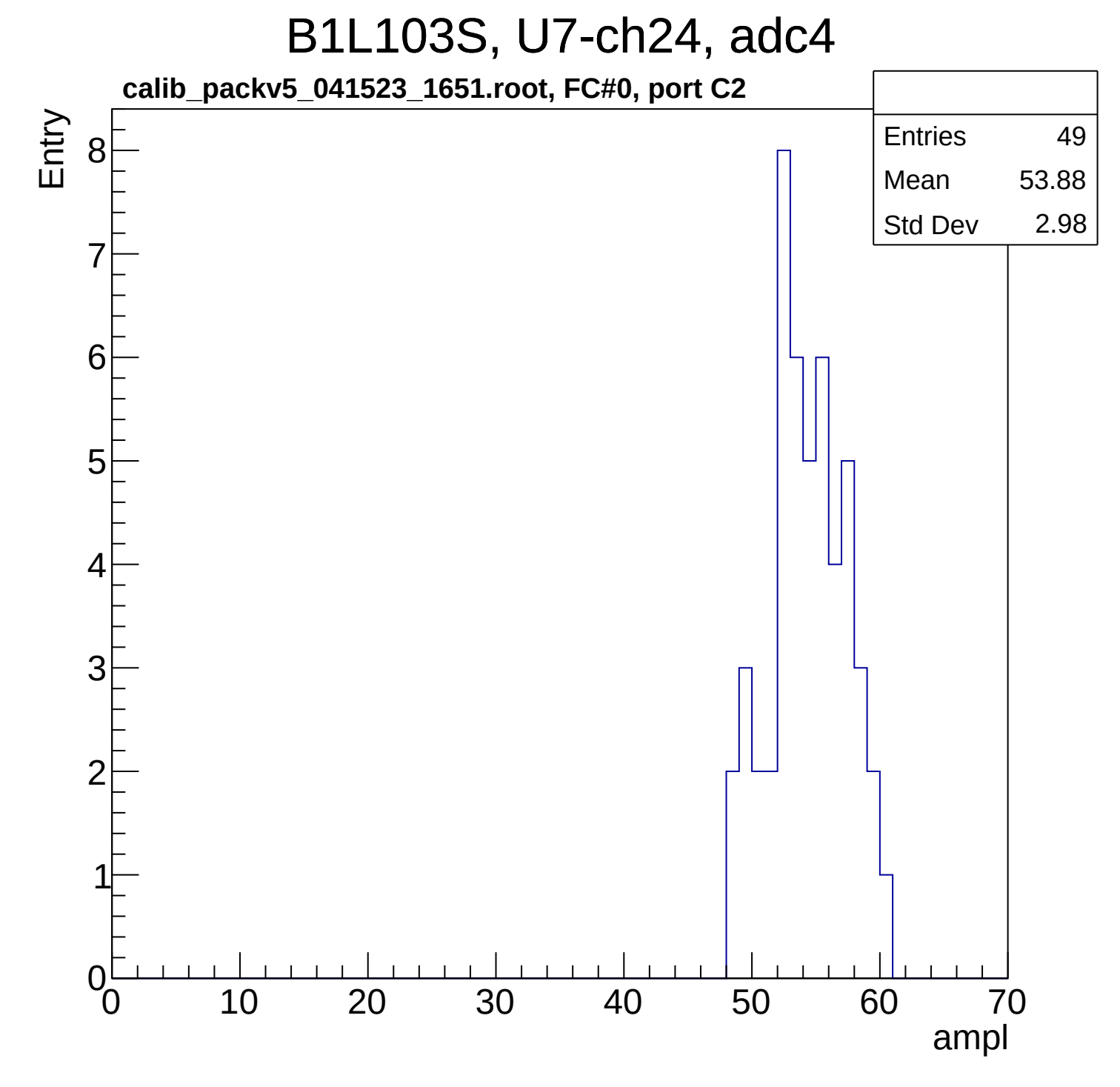
B1L103S, U7-ch24, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 53.88
Std Dev 2.98
Entry
ampl
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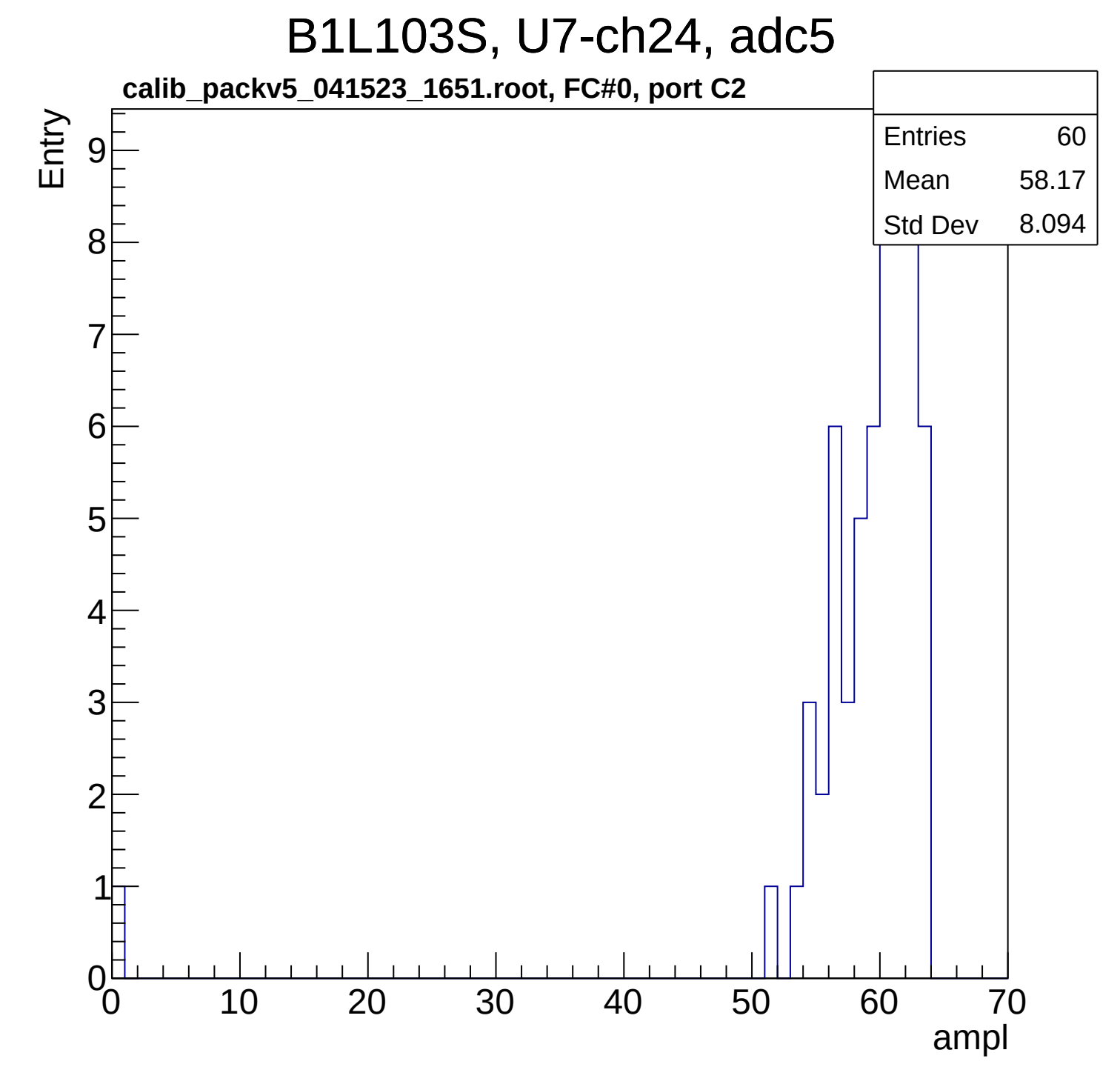
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch24, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 58.17
Std Dev 8.094
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
50
60
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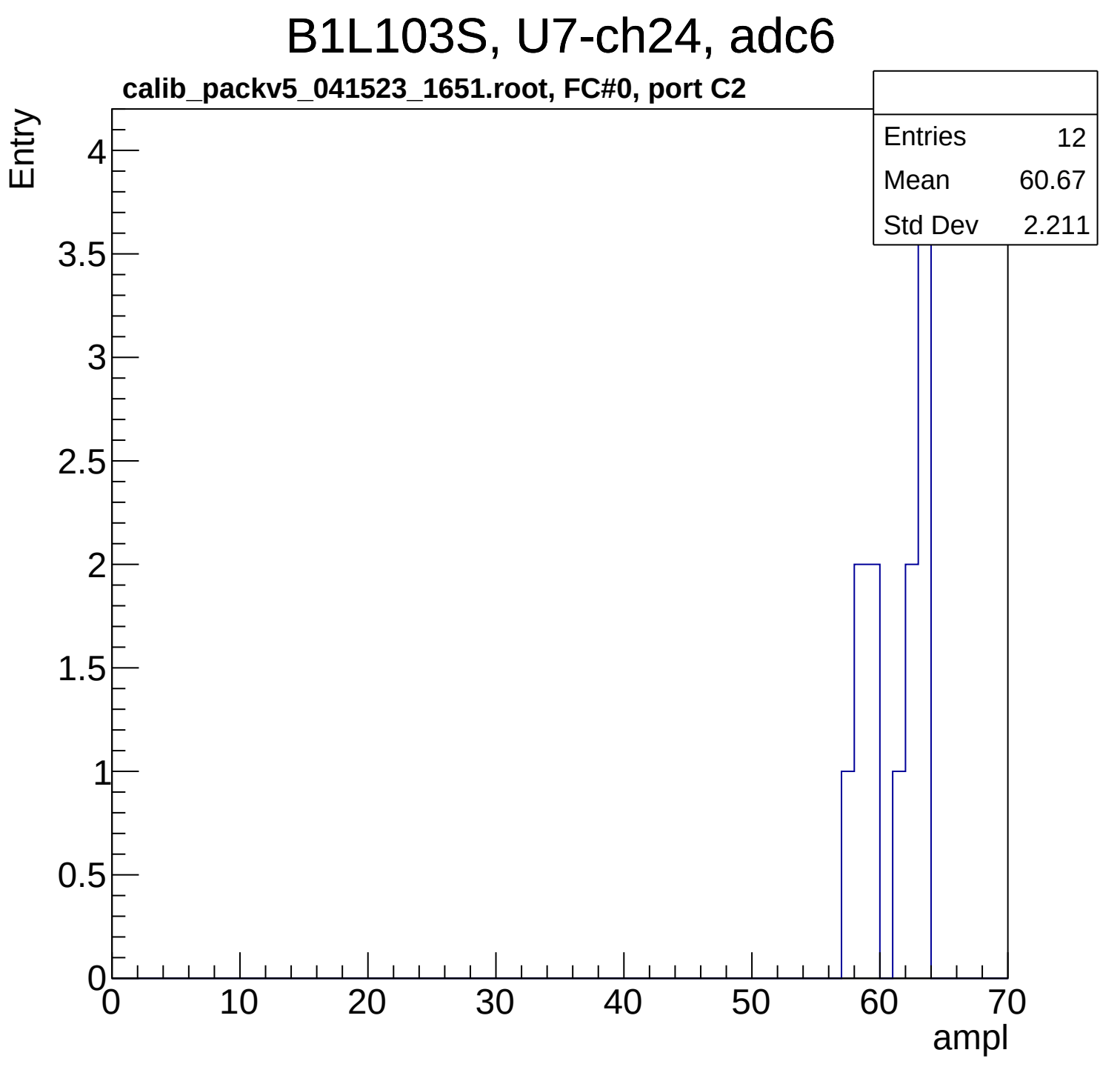
B1L103S, U7-ch24, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 60.67
Std Dev 2.211
Entry
ampl
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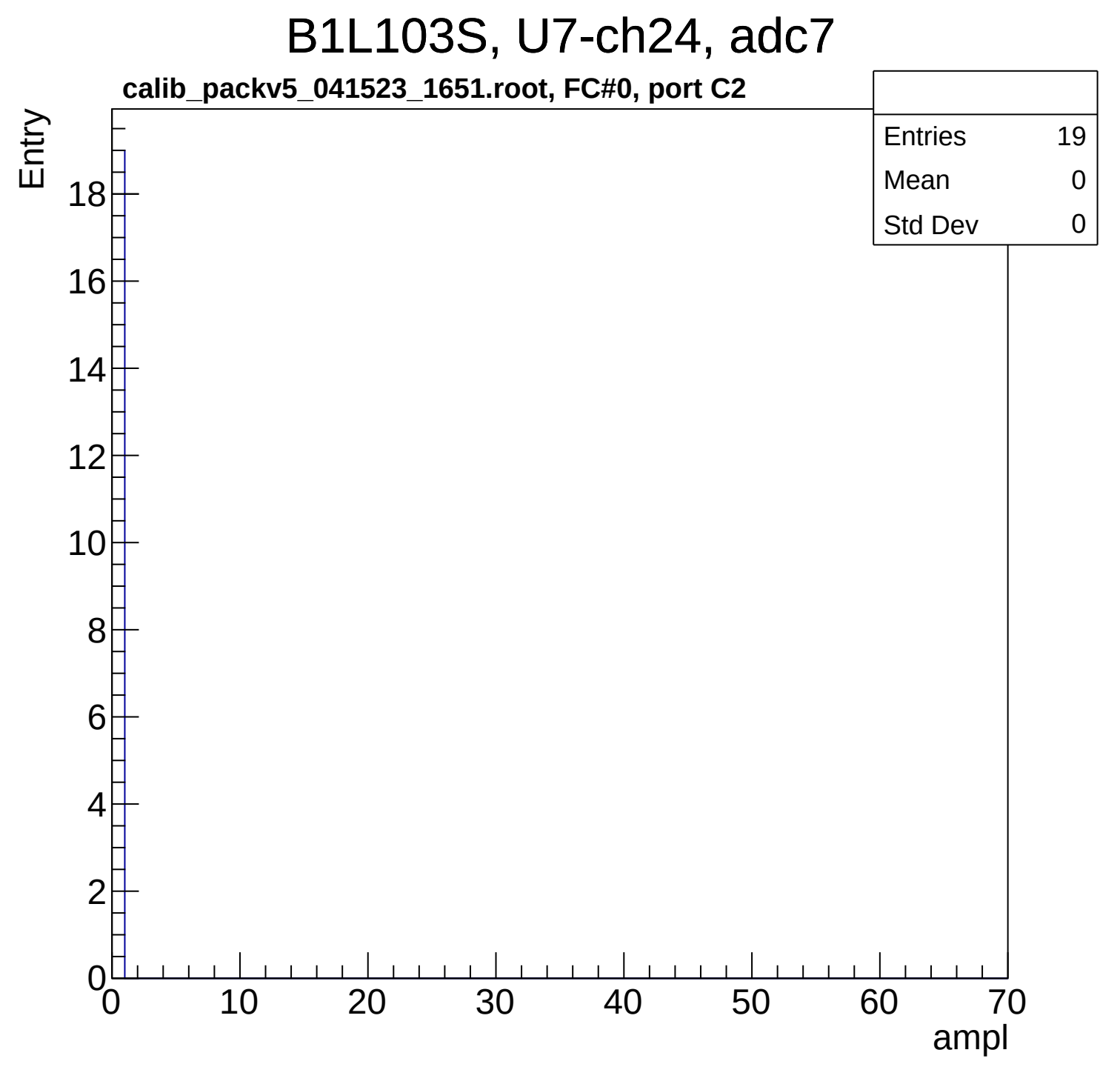
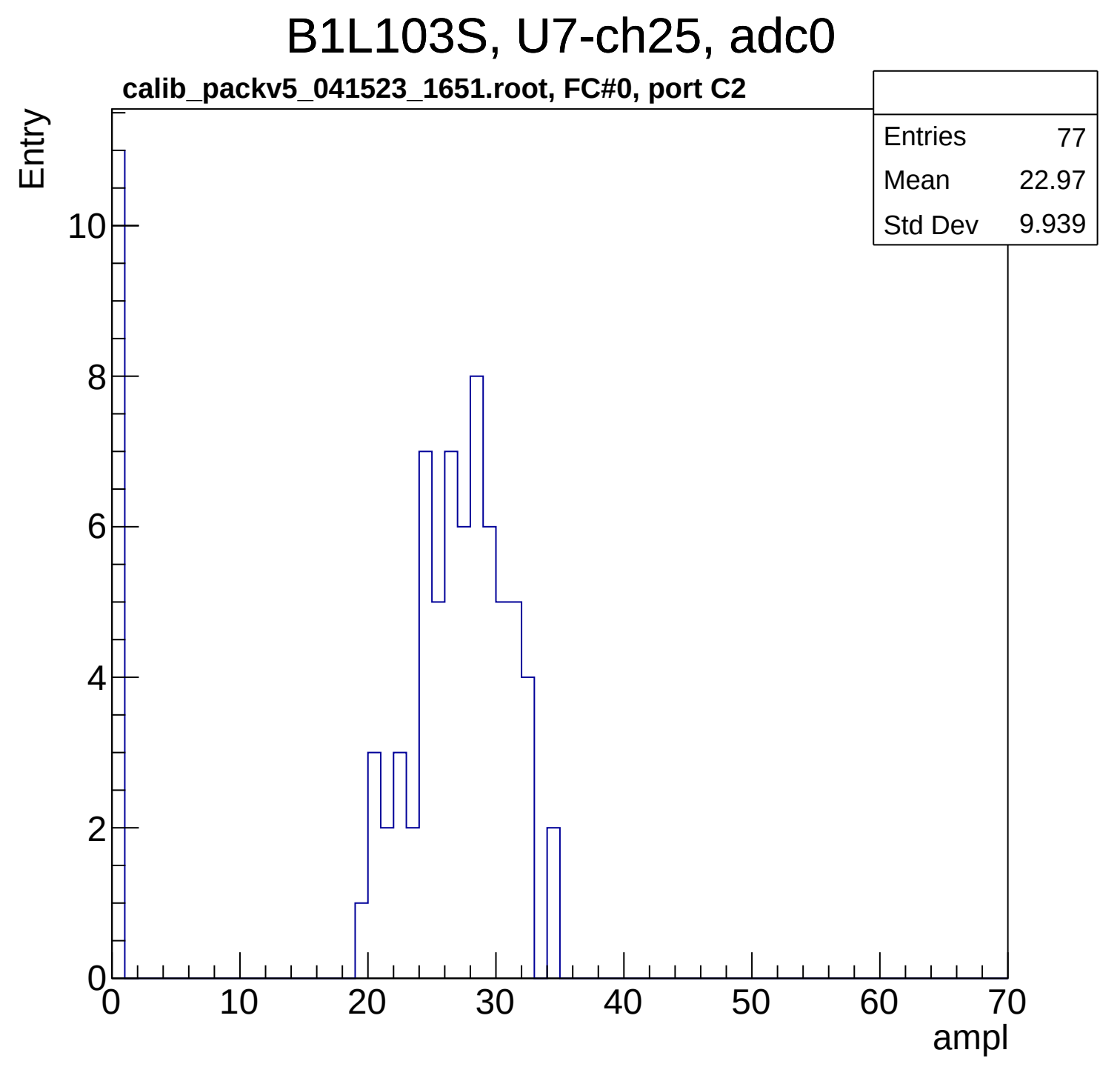
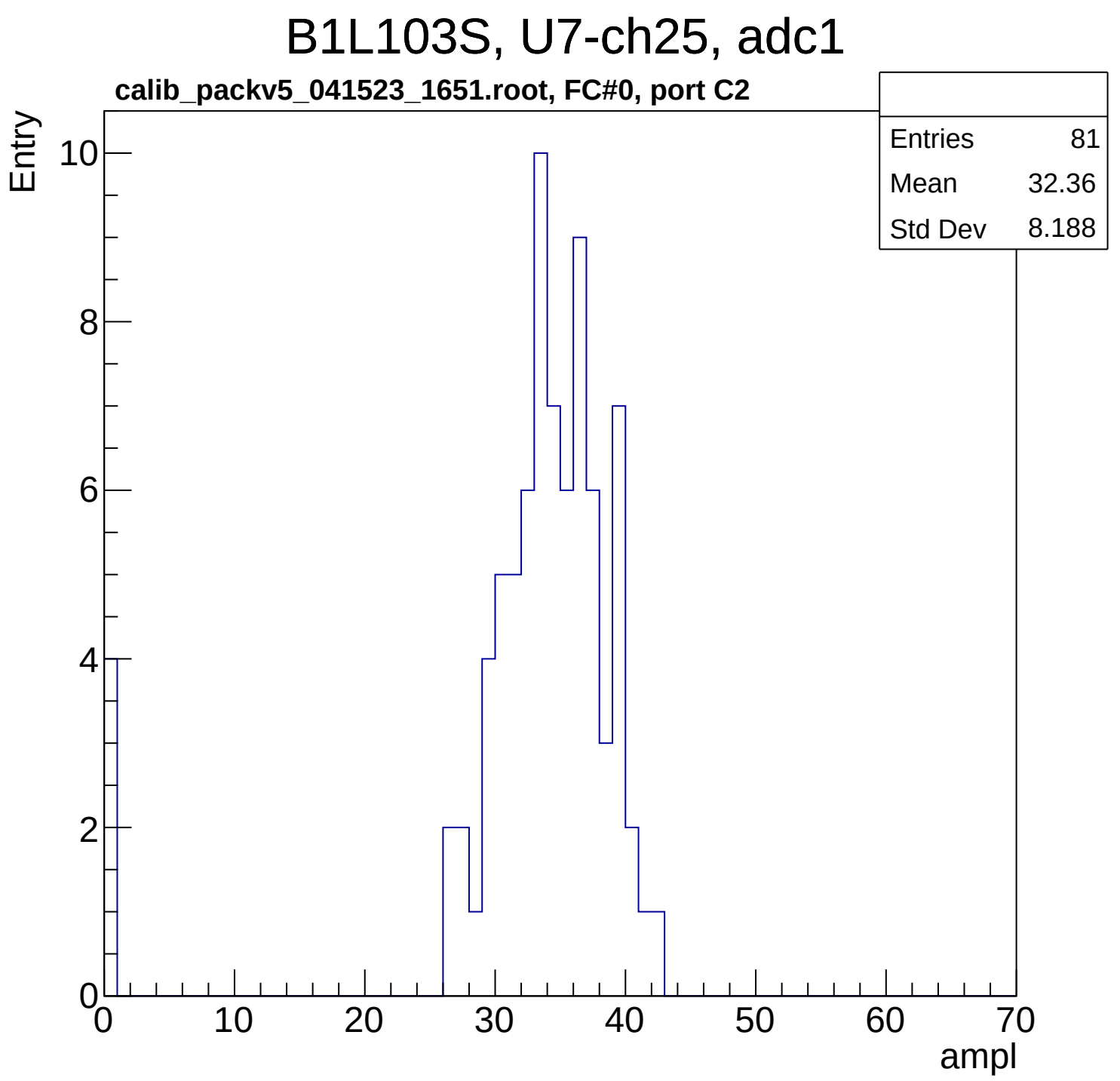
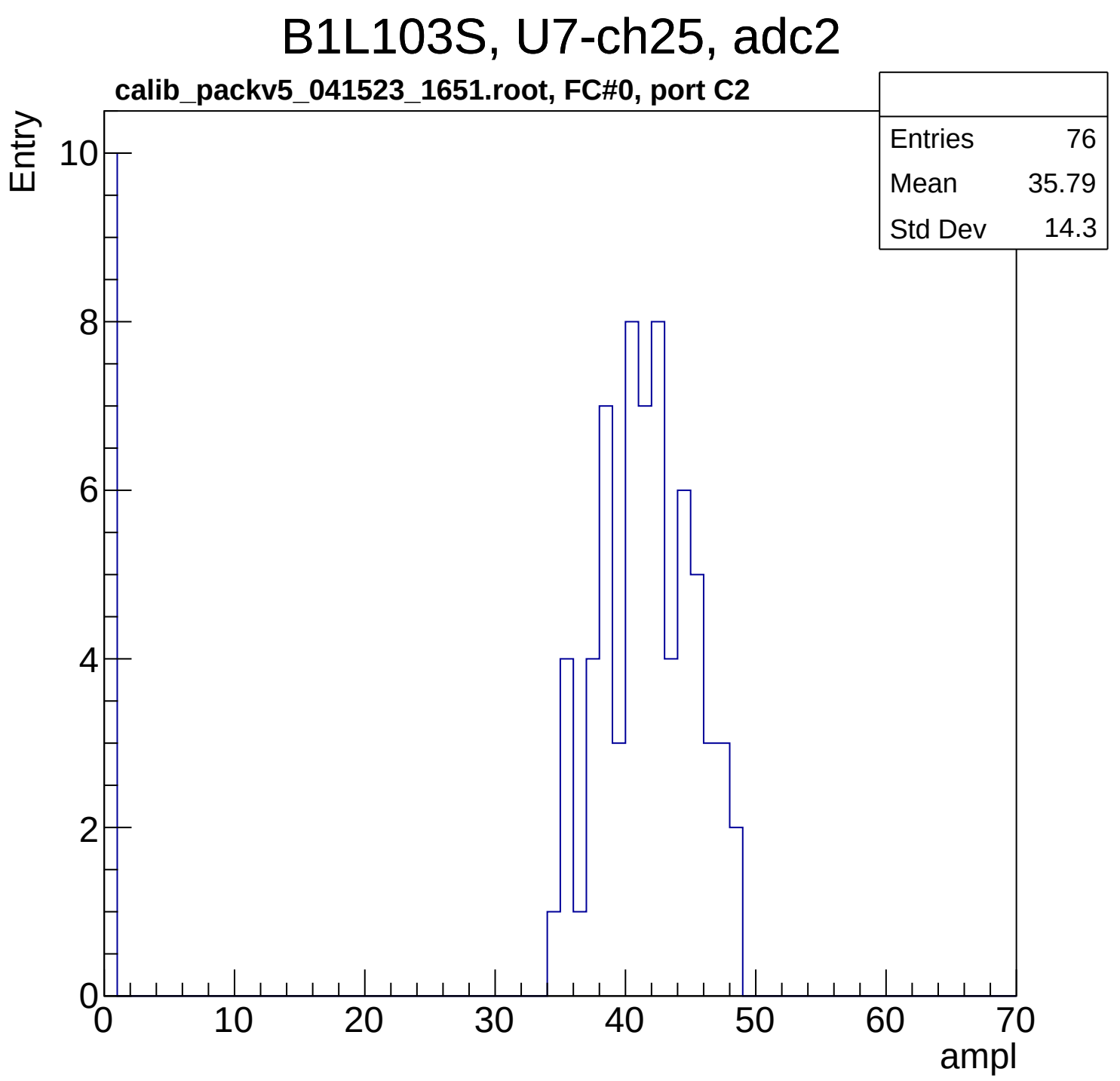
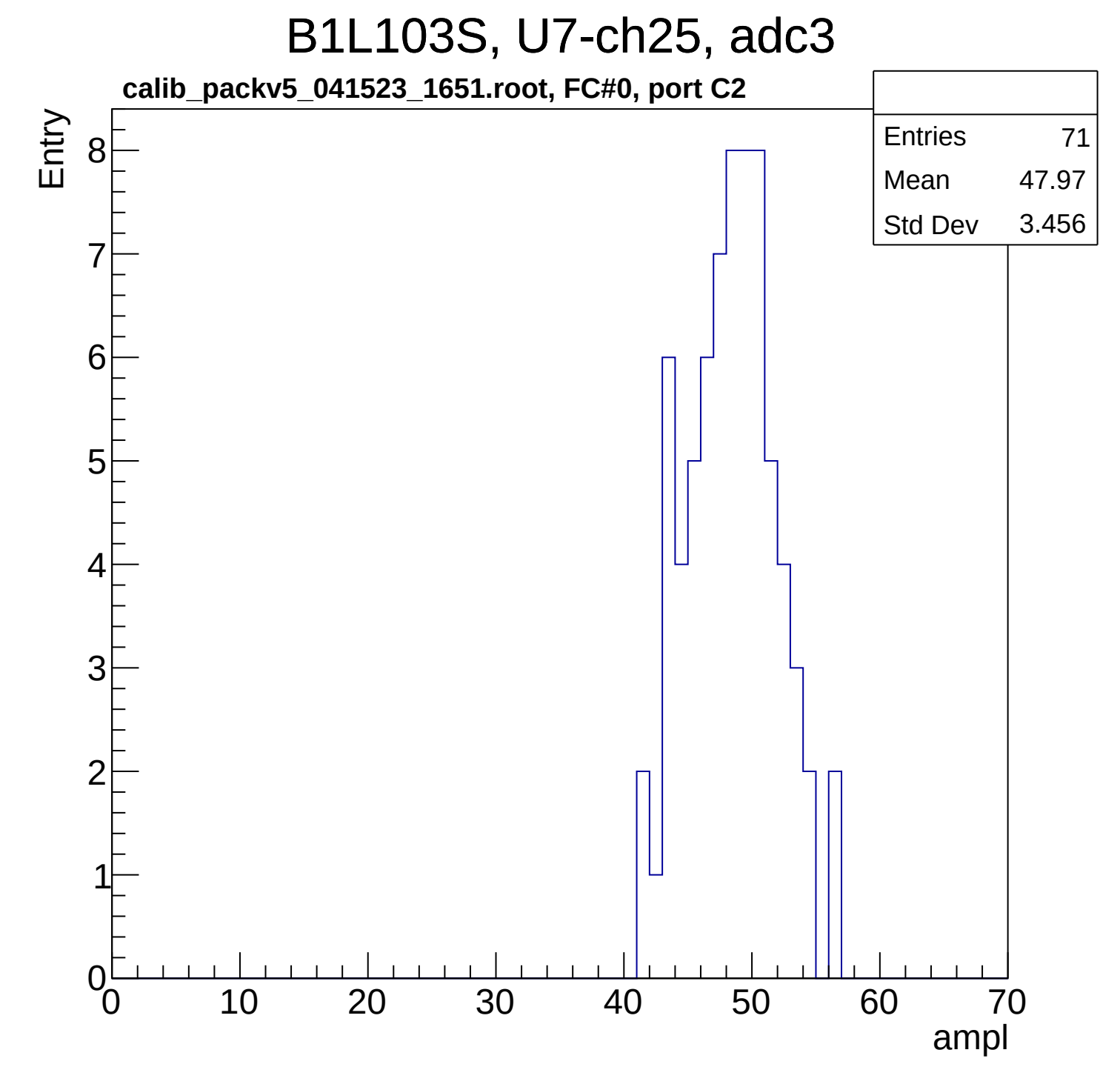
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U7-ch24, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch25, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 22.97
Std Dev 9.939
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch25, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 32.36
Std Dev 8.188
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U7-ch25, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 35.79
Std Dev 14.3
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch25, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 47.97
Std Dev 3.456
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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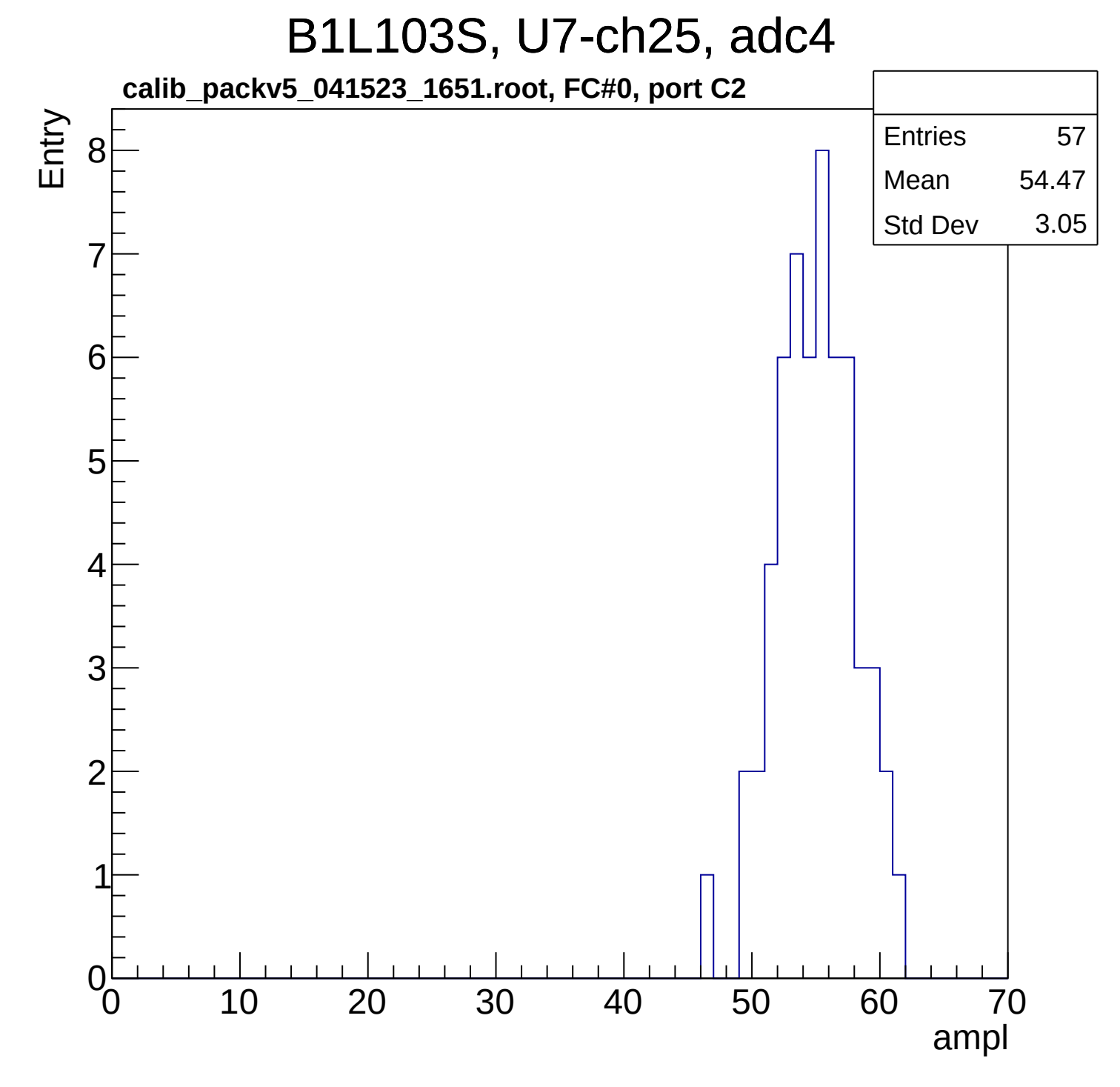
B1L103S, U7-ch25, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 54.47
Std Dev 3.05
Entry
ampl
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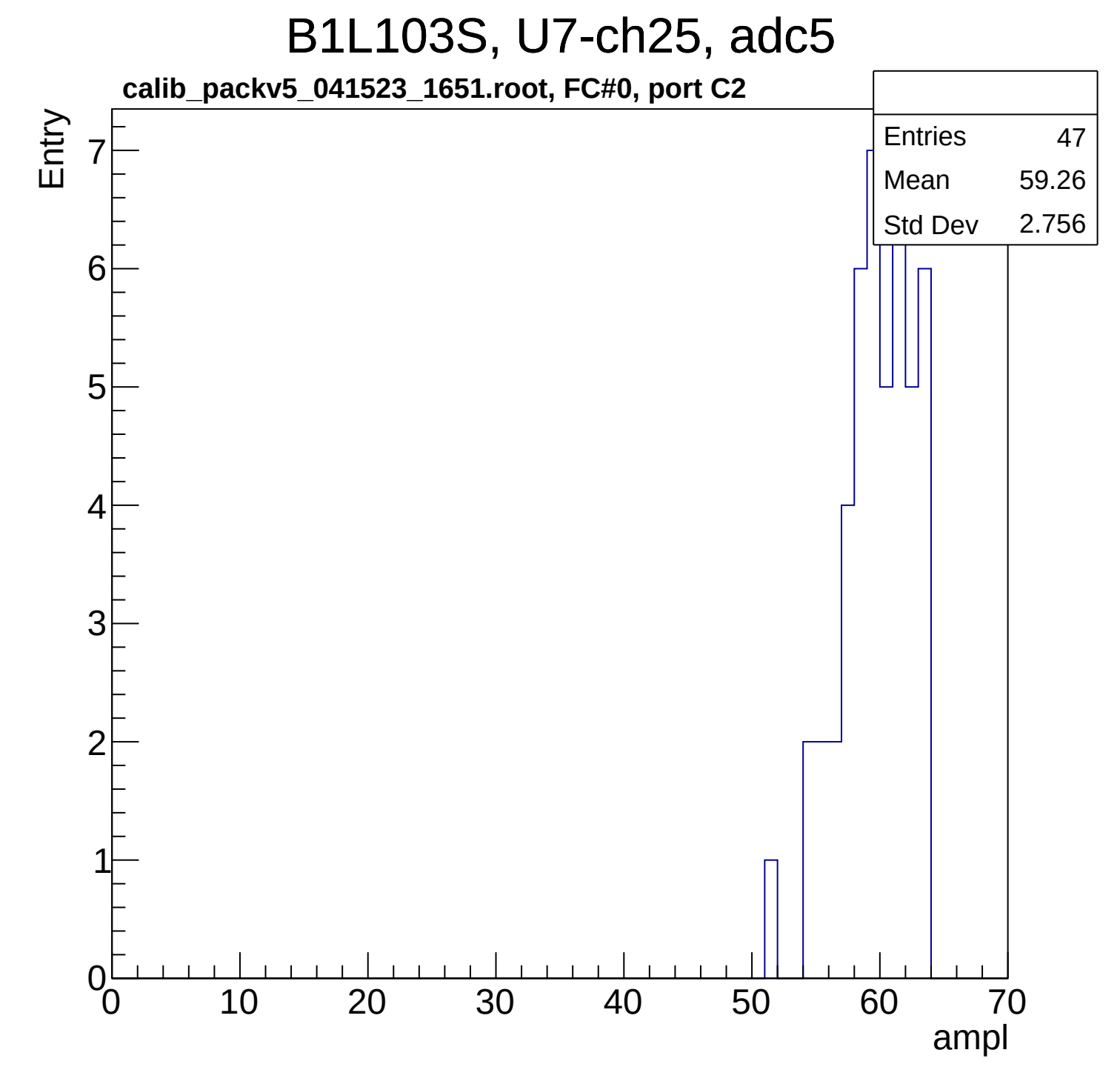
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch25, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 59.26
Std Dev 2.756
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
30
40
50
60
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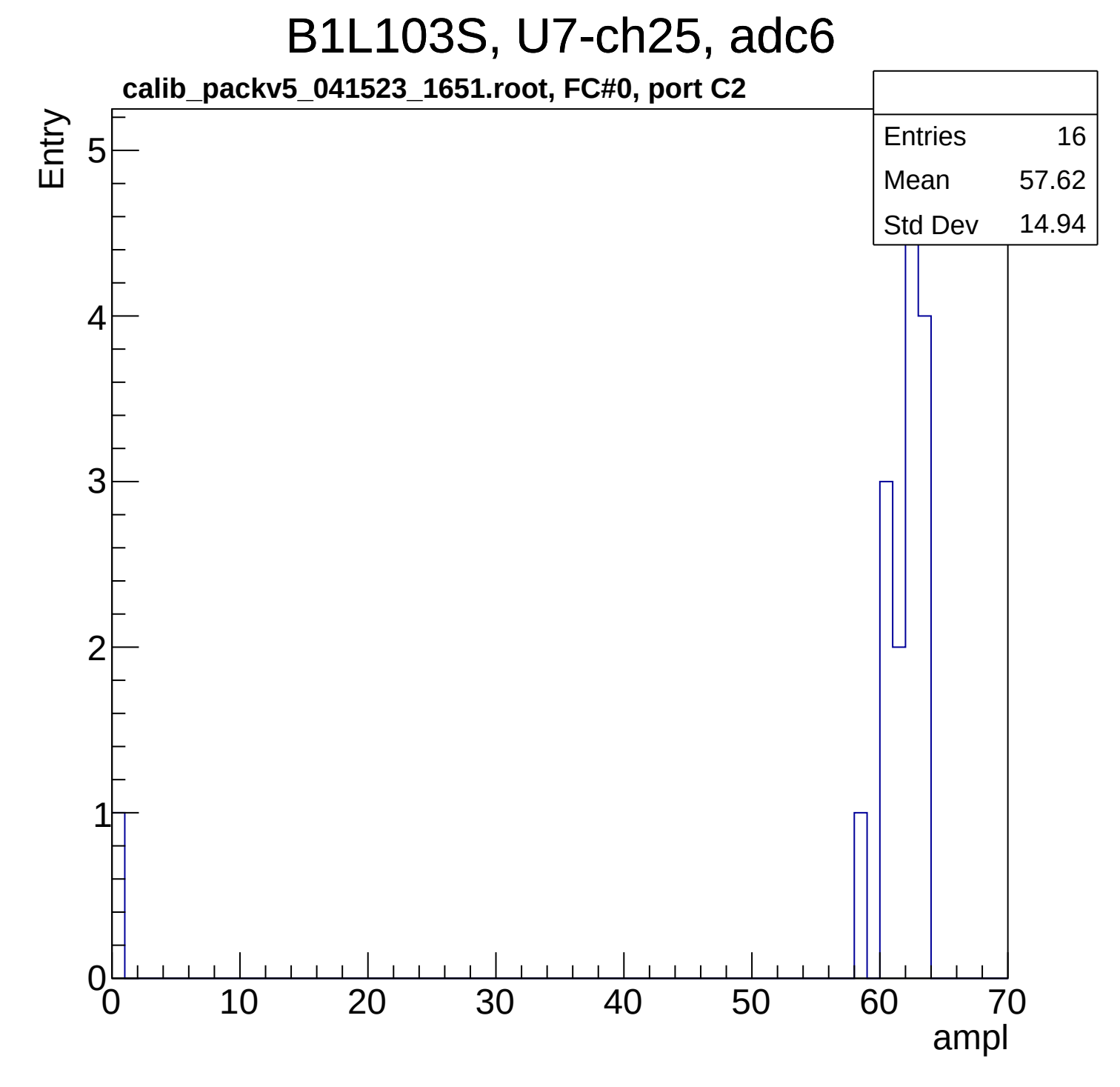
B1L103S, U7-ch25, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 16
Mean 57.62
Std Dev 14.94
Entry
ampl
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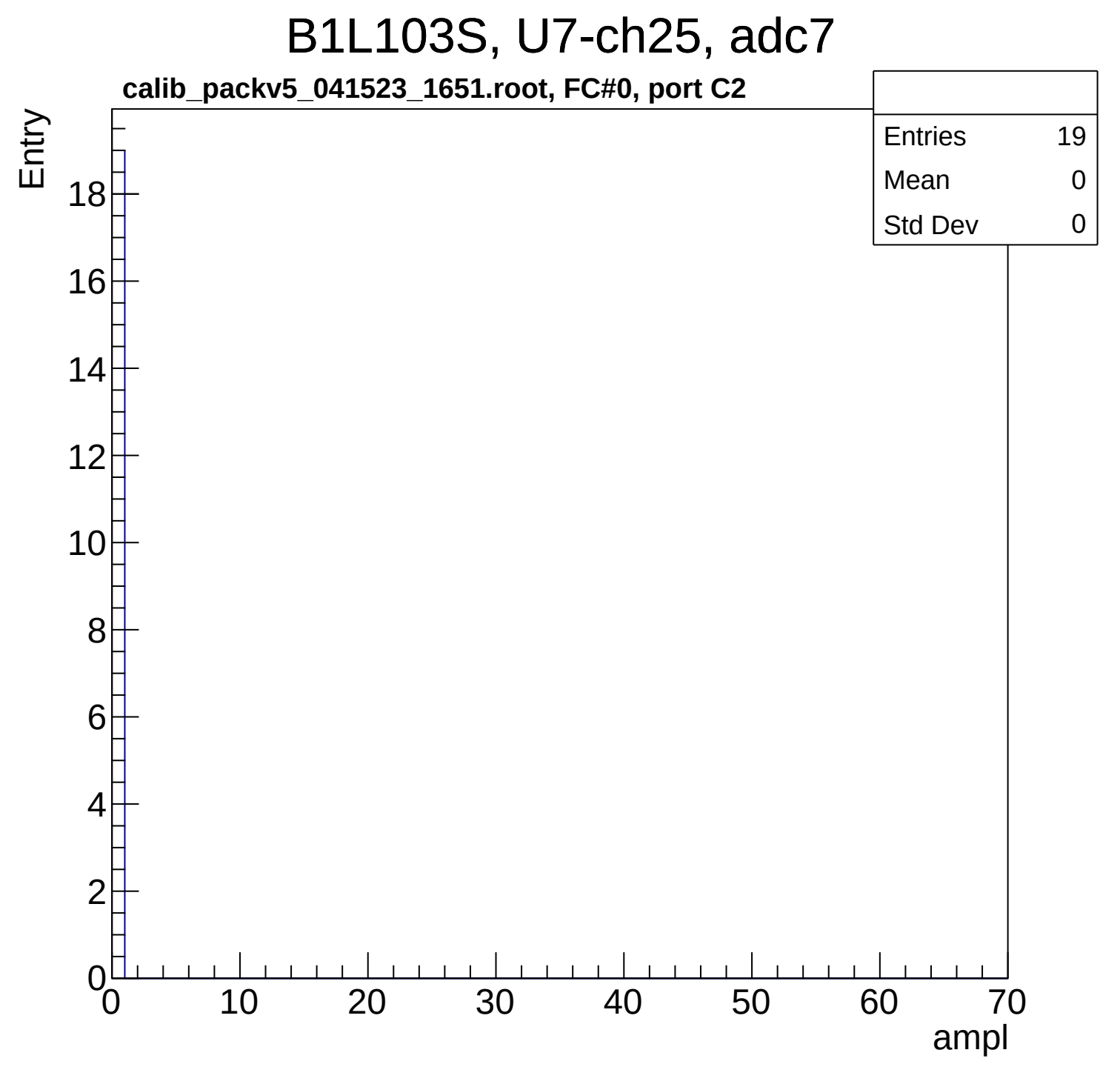
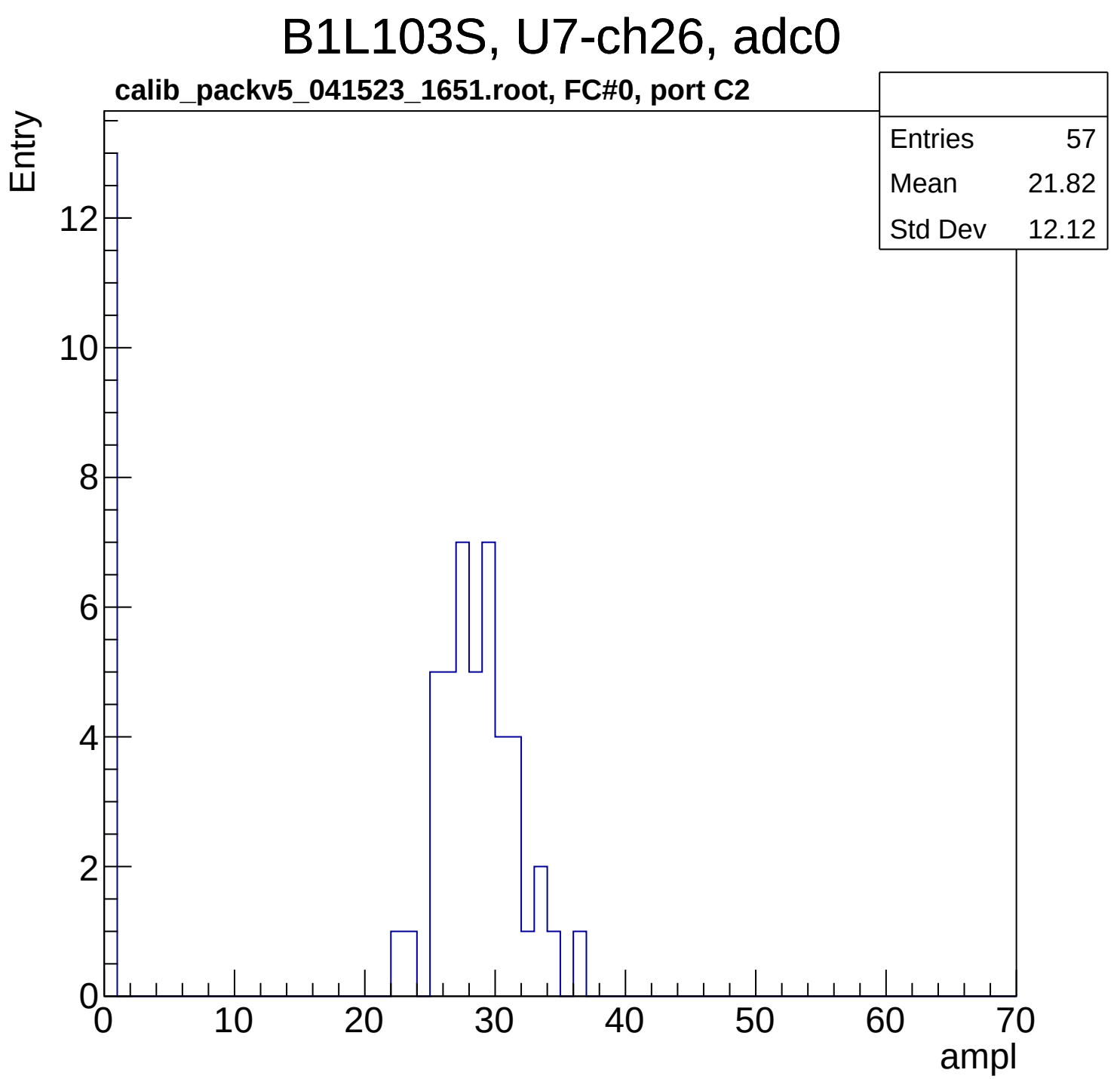
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U7-ch25, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch26, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 21.82
Std Dev 12.12
Entry
0
2
4
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8
10
12
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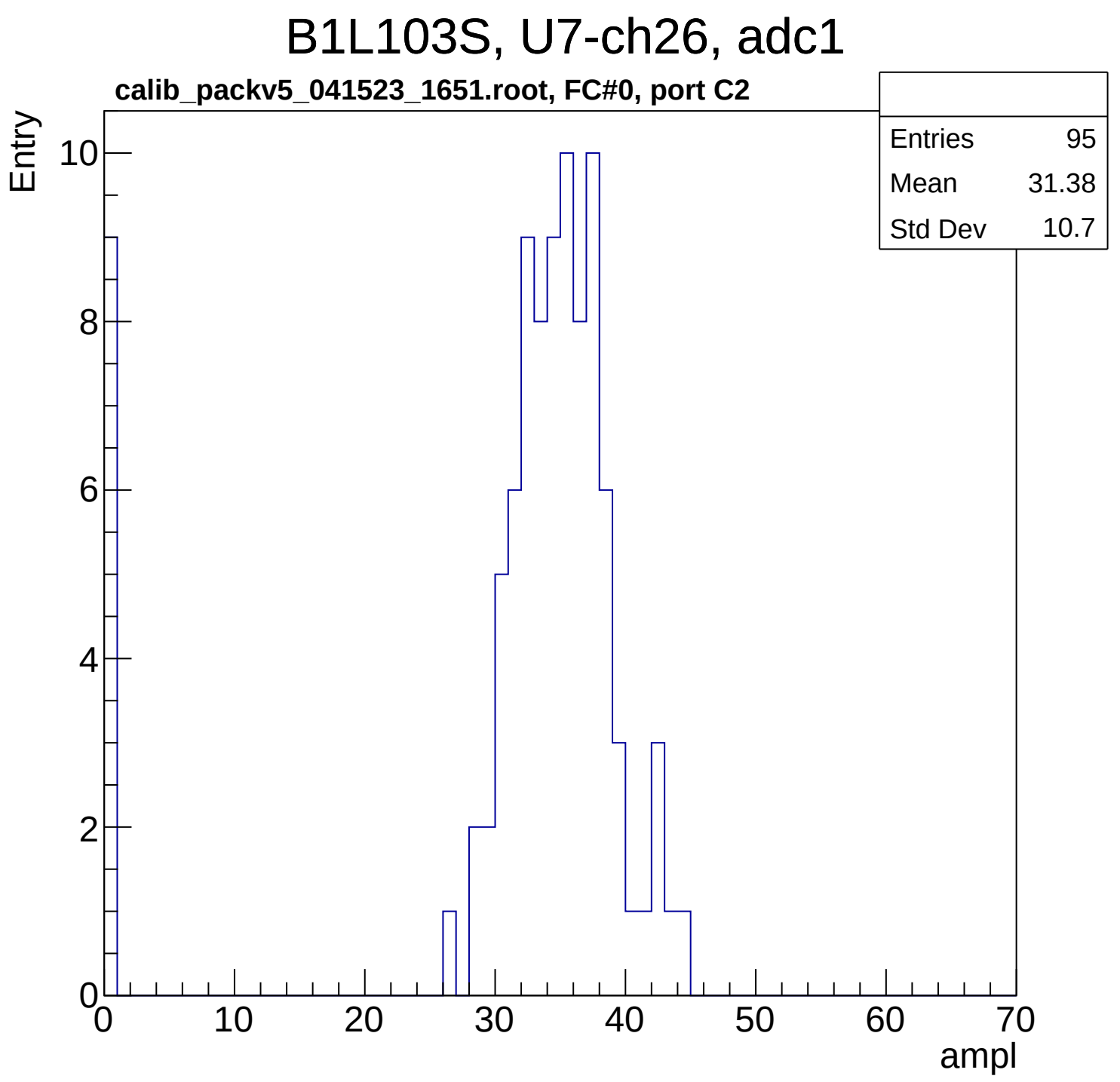
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch26, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 95
Mean 31.38
Std Dev 10.7
Entry
0
2
4
6
8
10
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10
20
30
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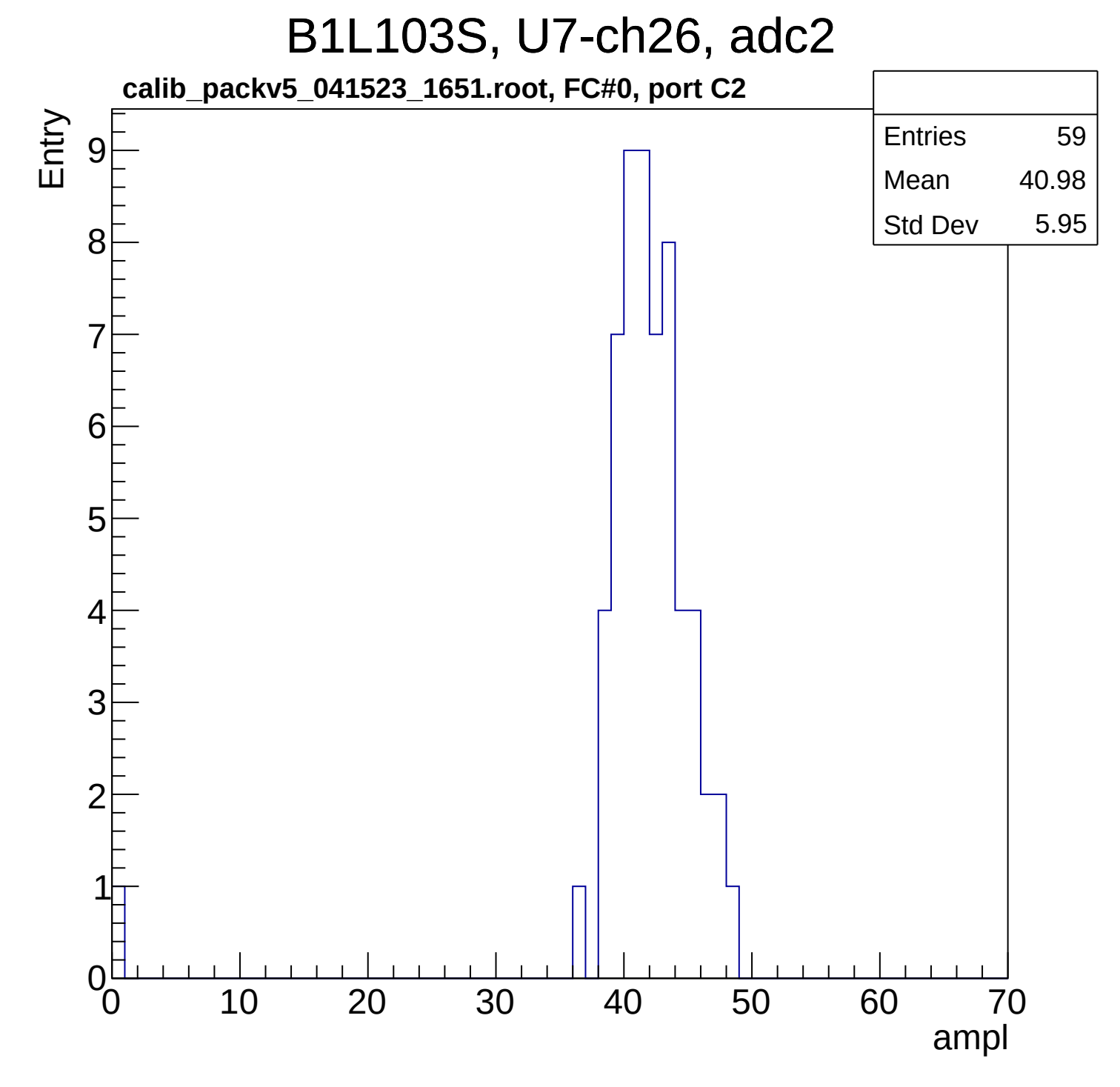
50
60
70
ampl


B1L103S, U7-ch26, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 40.98
Std Dev 5.95
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
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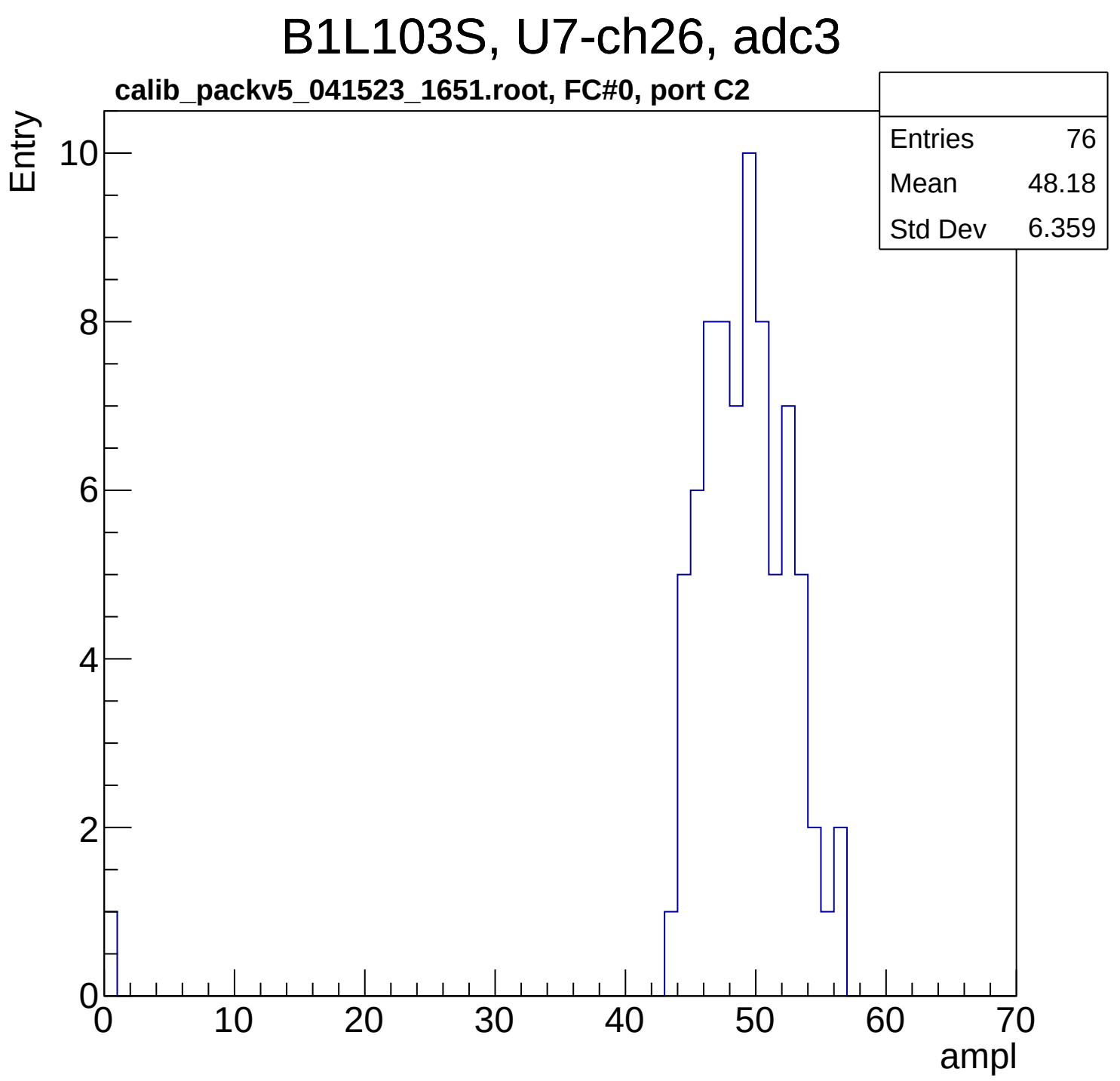
60
70


B1L103S, U7-ch26, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 48.18
Std Dev 6.359
Entry
ampl
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4
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8
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0
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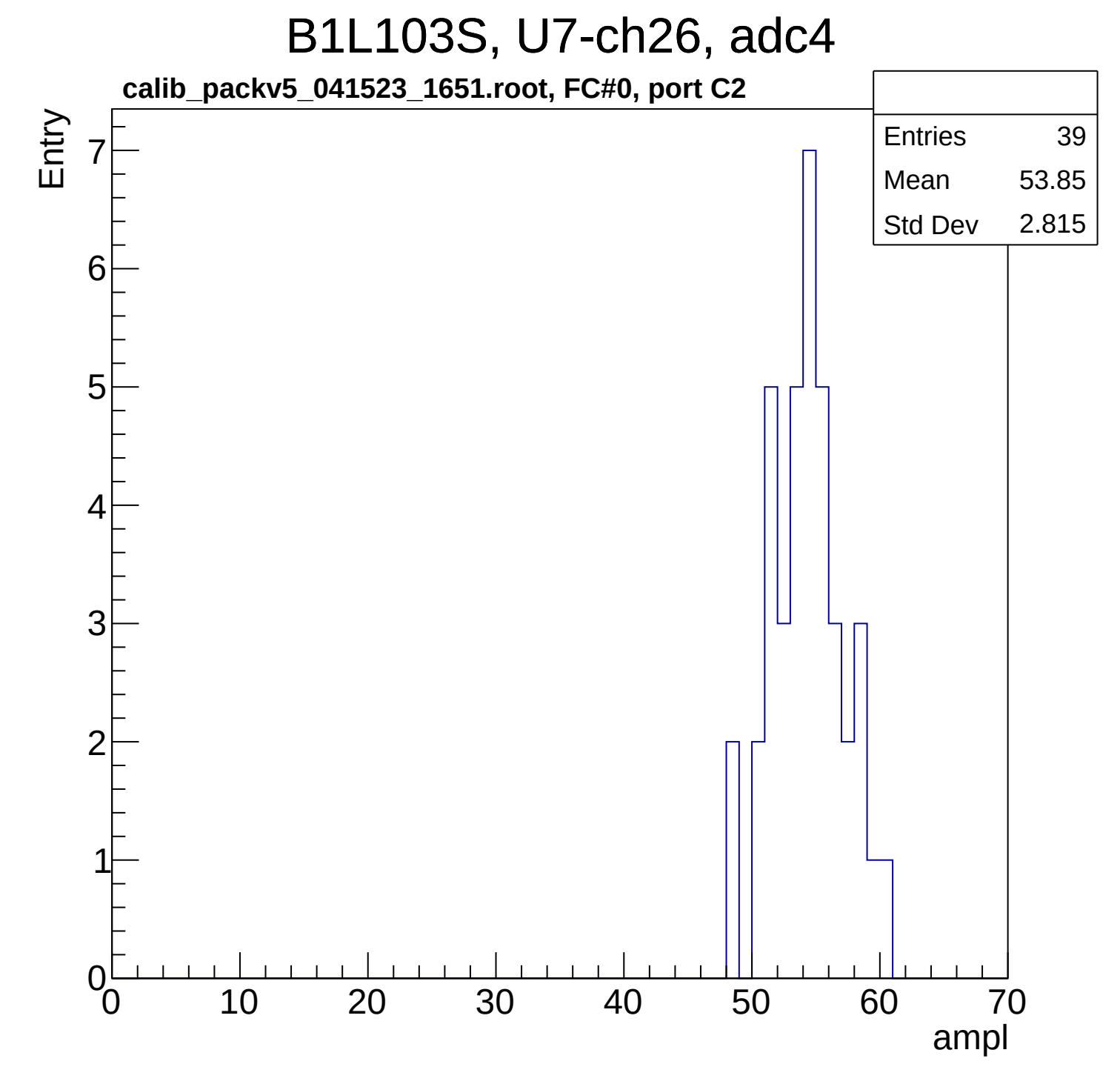
50
60
70


B1L103S, U7-ch26, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 39
Mean 53.85
Std Dev 2.815
Entry
ampl
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2
3
4
5
6
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0
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60
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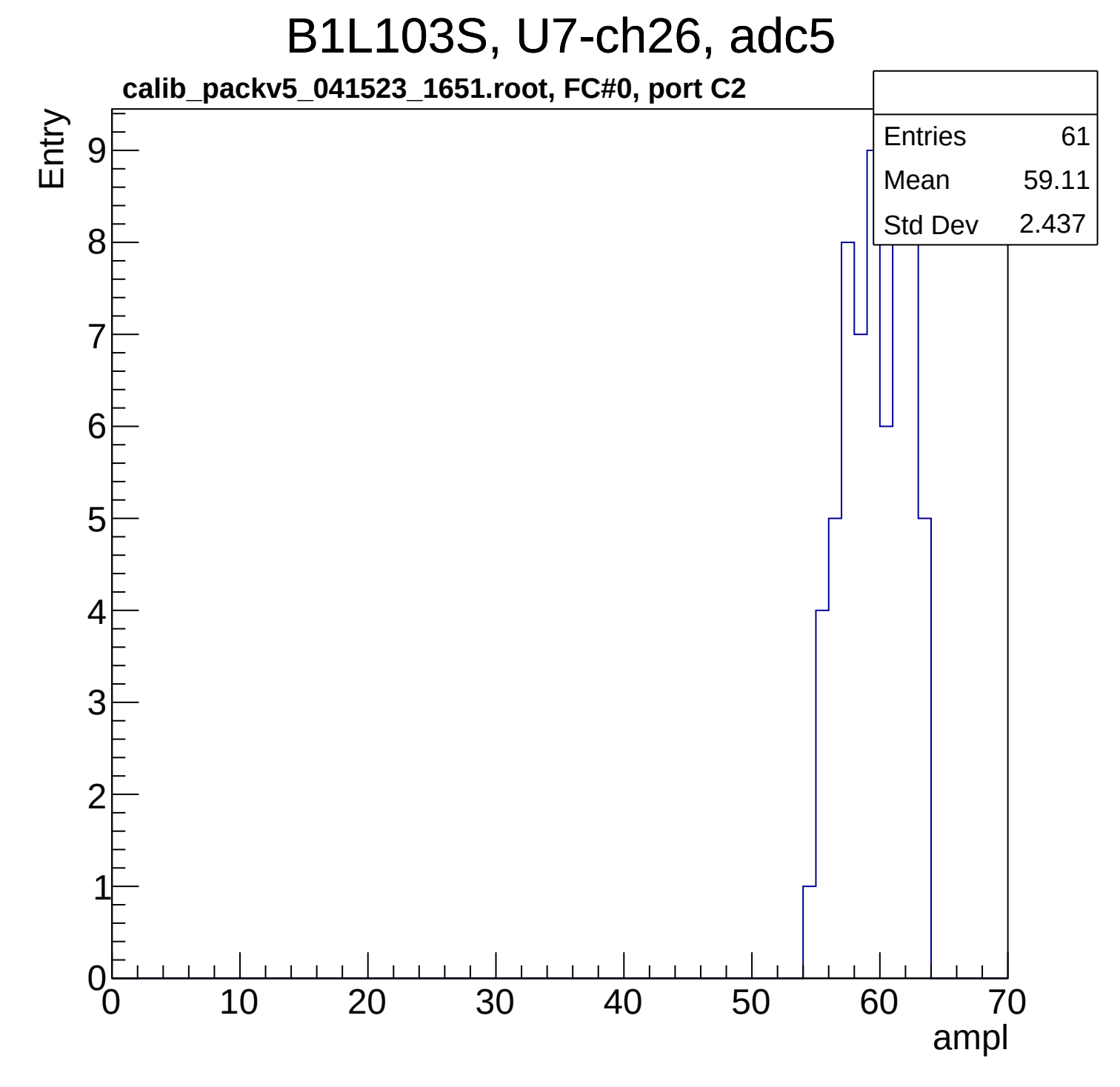
B1L103S, U7-ch26, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 59.11
Std Dev 2.437
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
30
40
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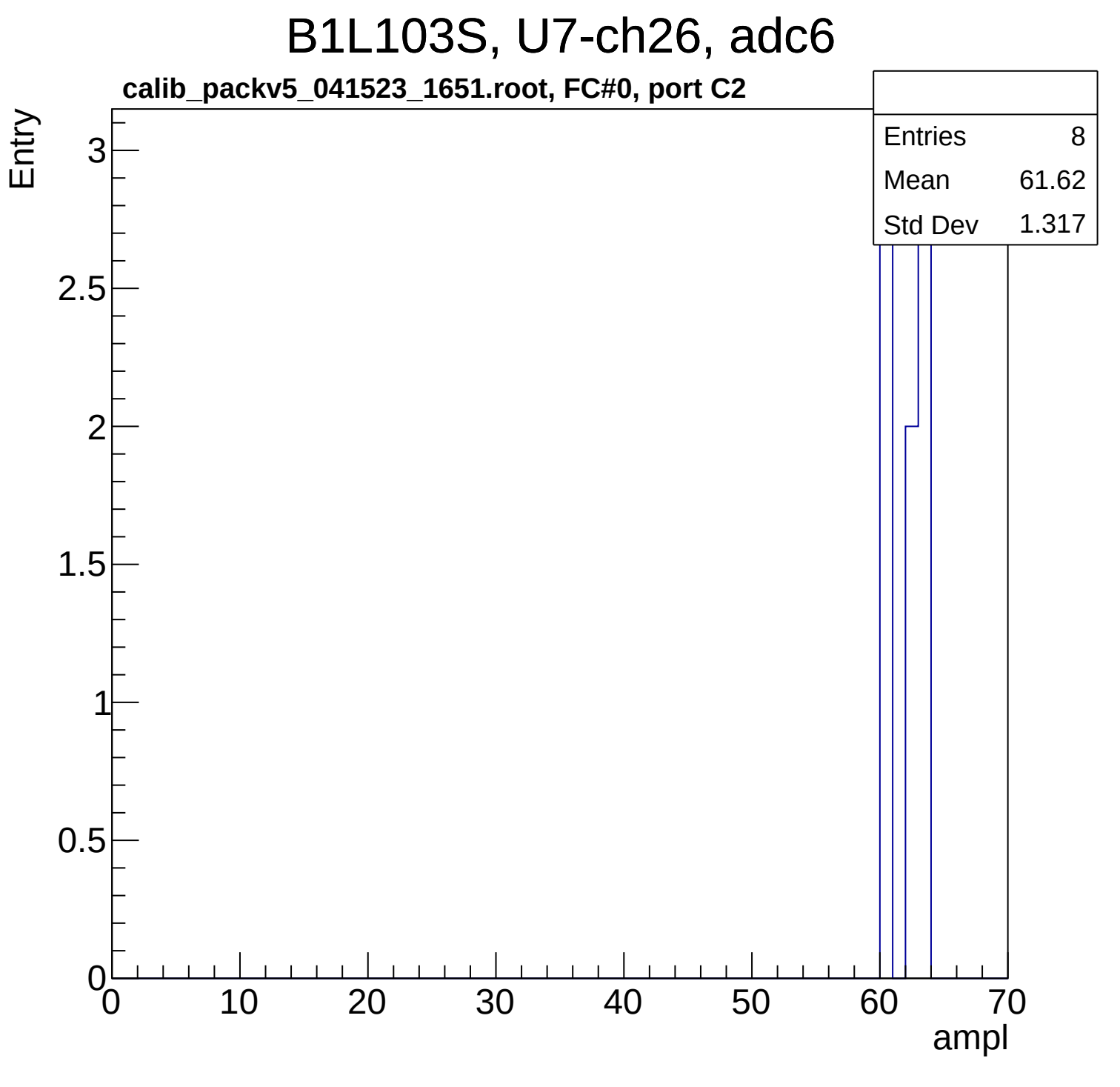
60
70


B1L103S, U7-ch26, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 61.62
Std Dev 1.317
Entry
ampl
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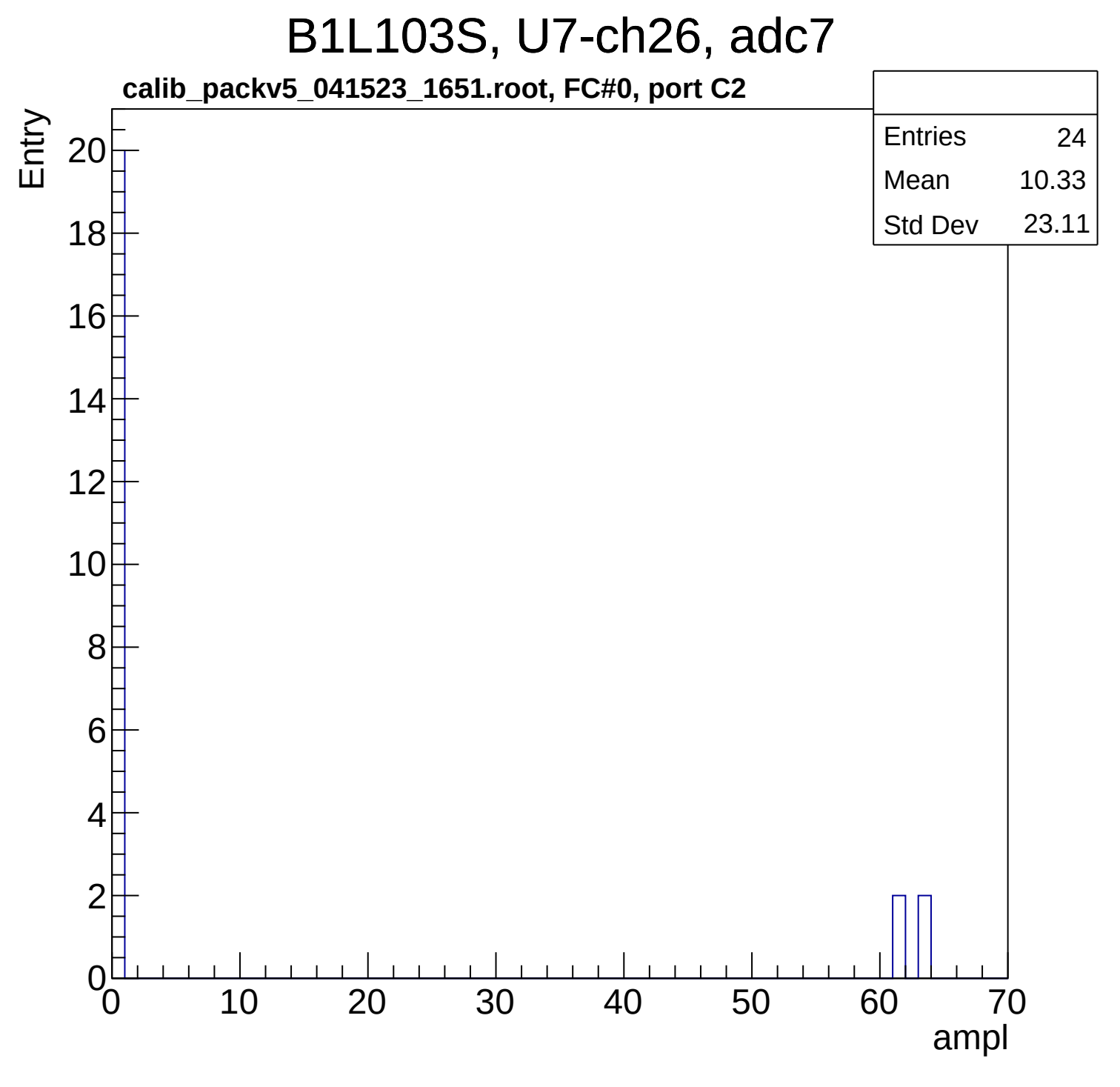
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U7-ch26, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 24
Mean 10.33
Std Dev 23.11
Entry
0
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8
10
12
14
16
18
20
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10
20
30
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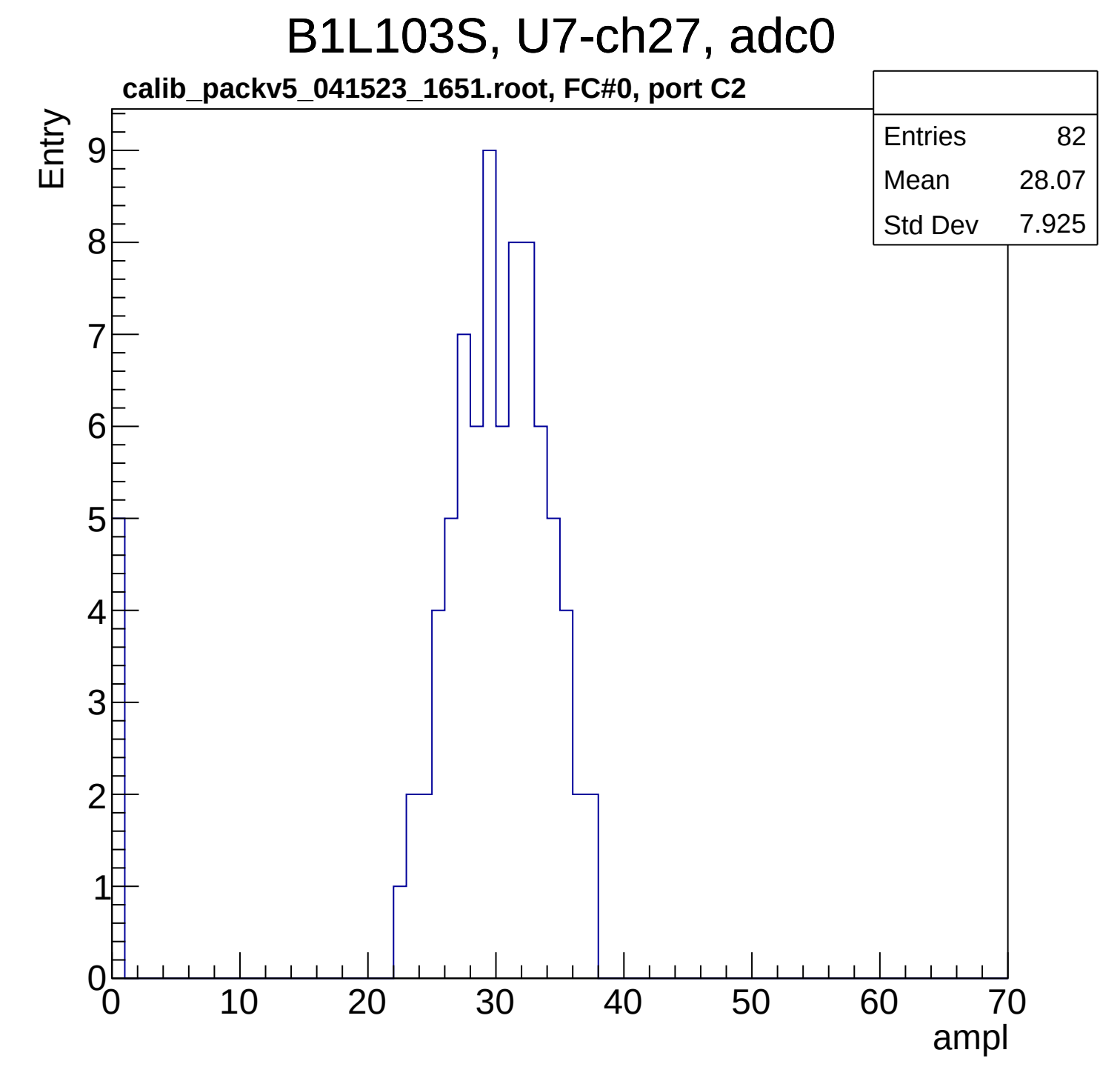
50
60
70
ampl


B1L103S, U7-ch27, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 28.07
Std Dev 7.925
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
50
60
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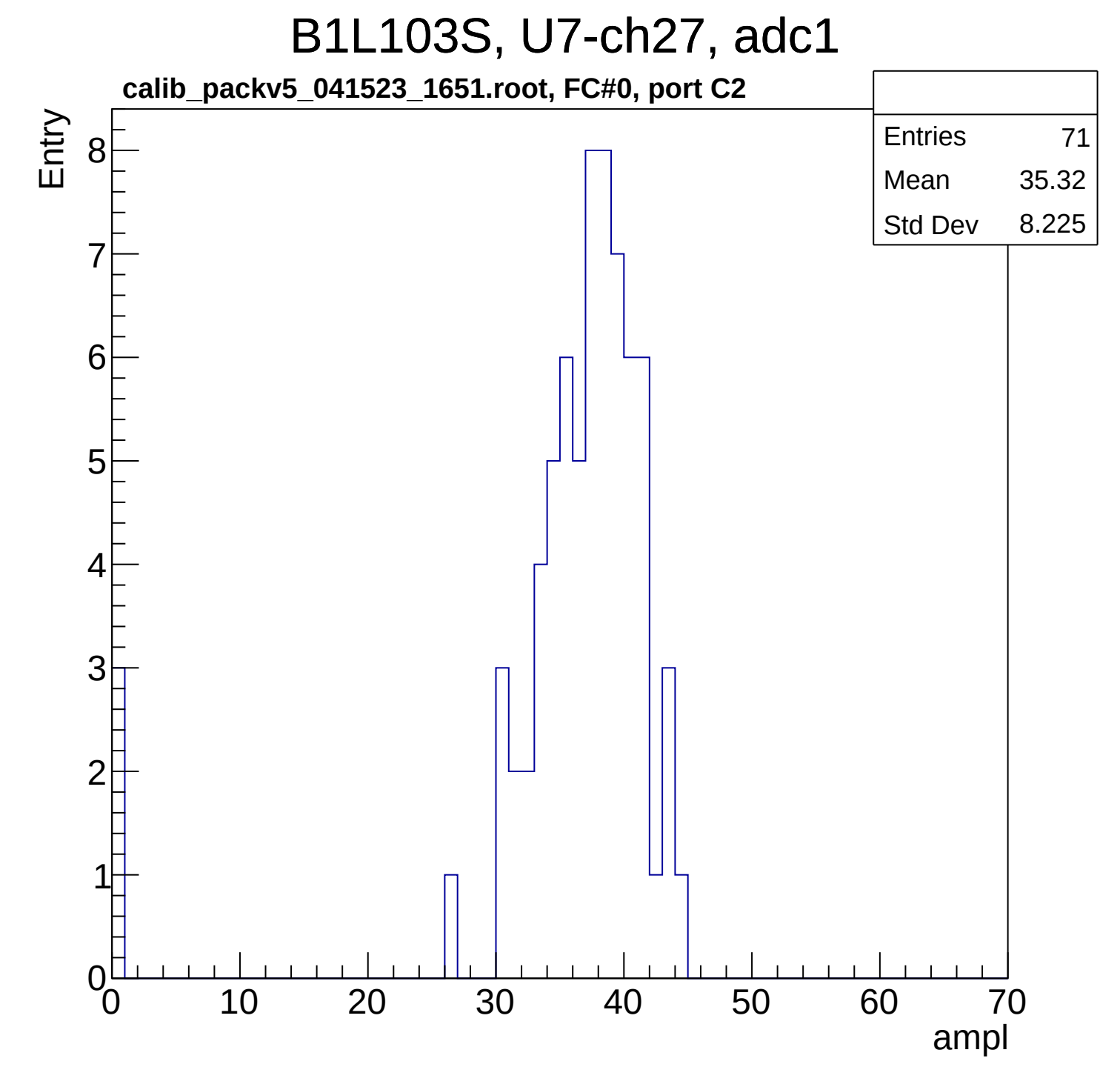
B1L103S, U7-ch27, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 35.32
Std Dev 8.225
Entry
ampl
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2
3
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5
6
7
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0
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20
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40
50
60
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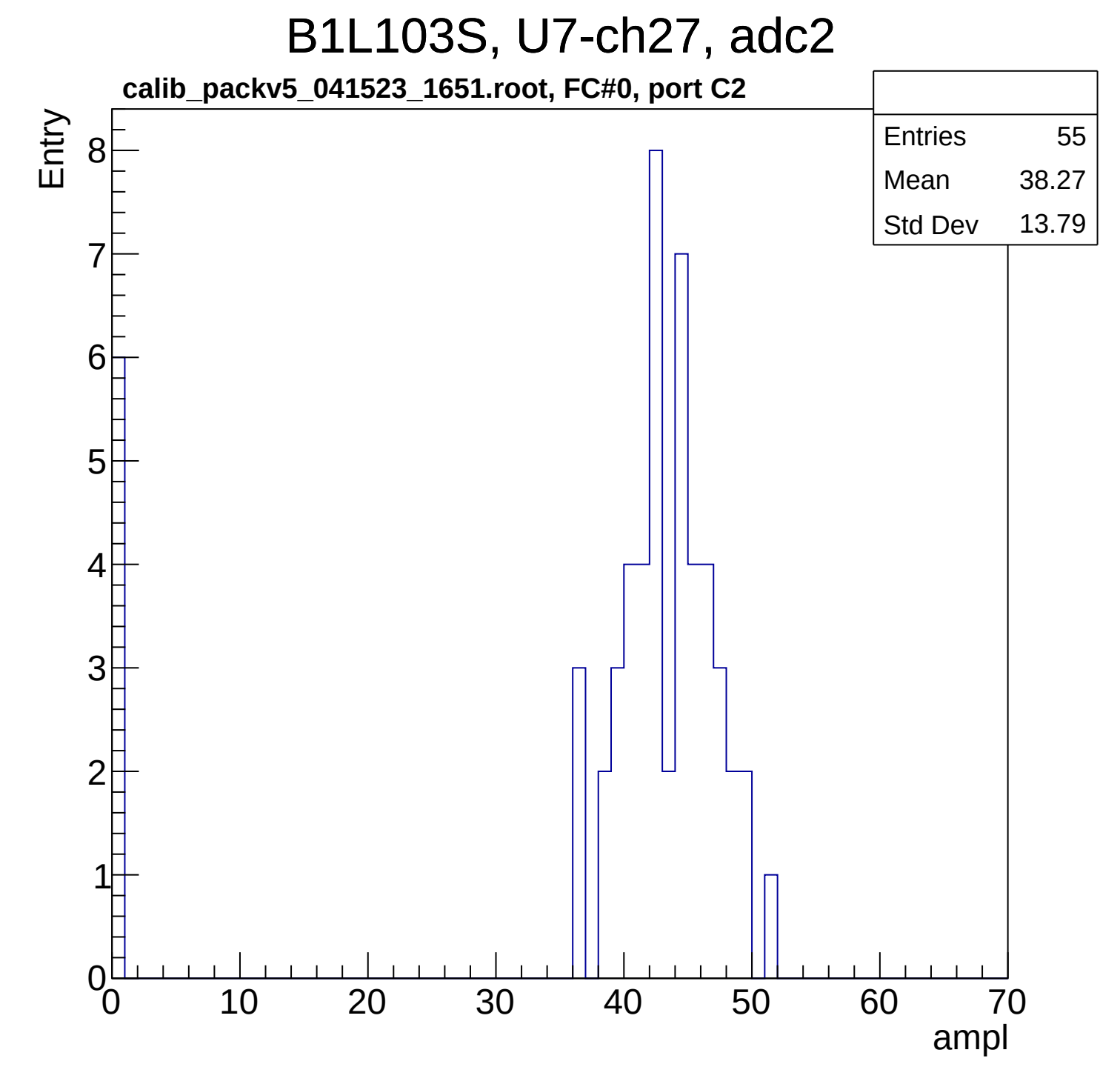
B1L103S, U7-ch27, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 38.27
Std Dev 13.79
Entry
ampl
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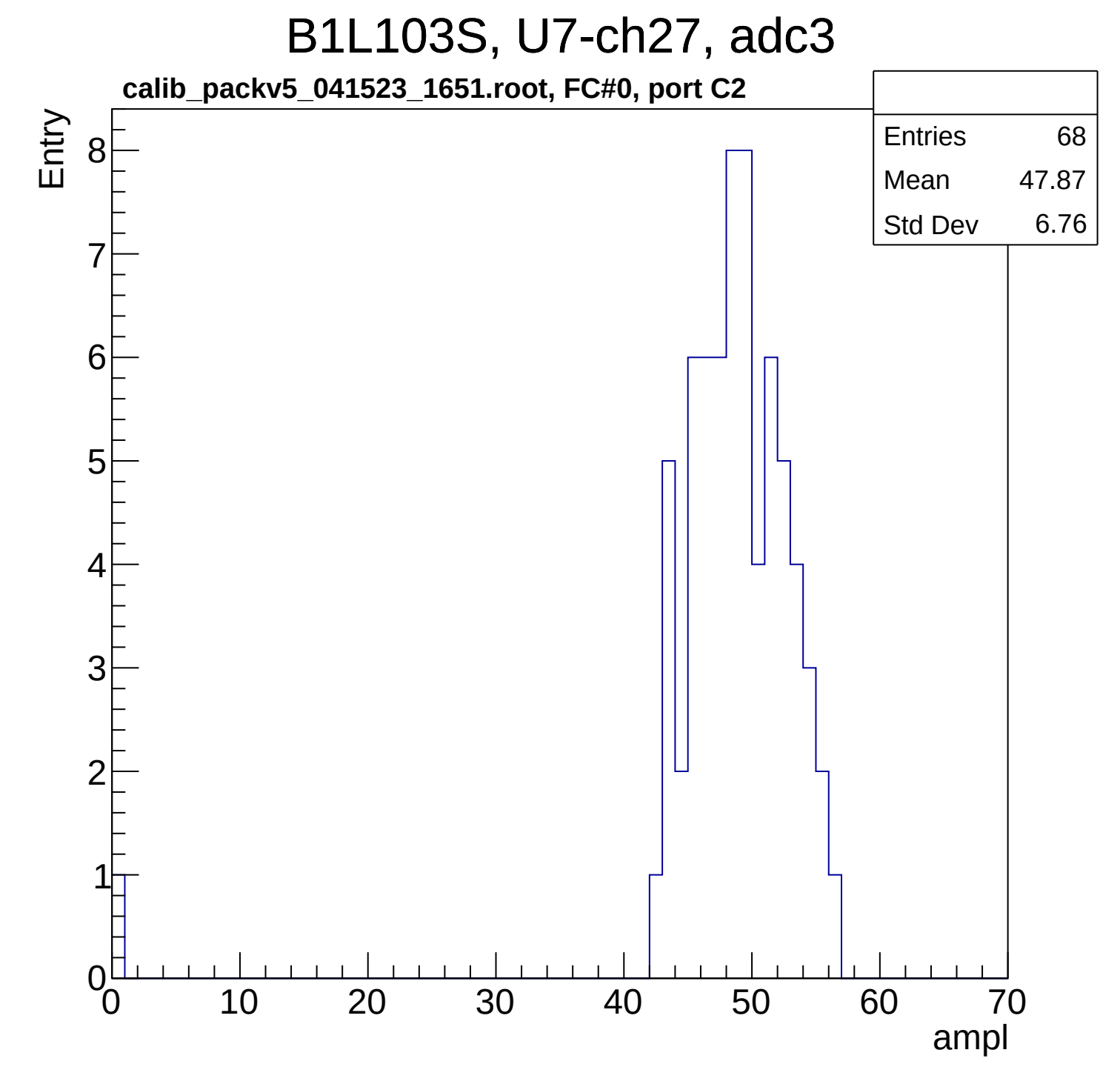
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch27, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 47.87
Std Dev 6.76
Entry
ampl
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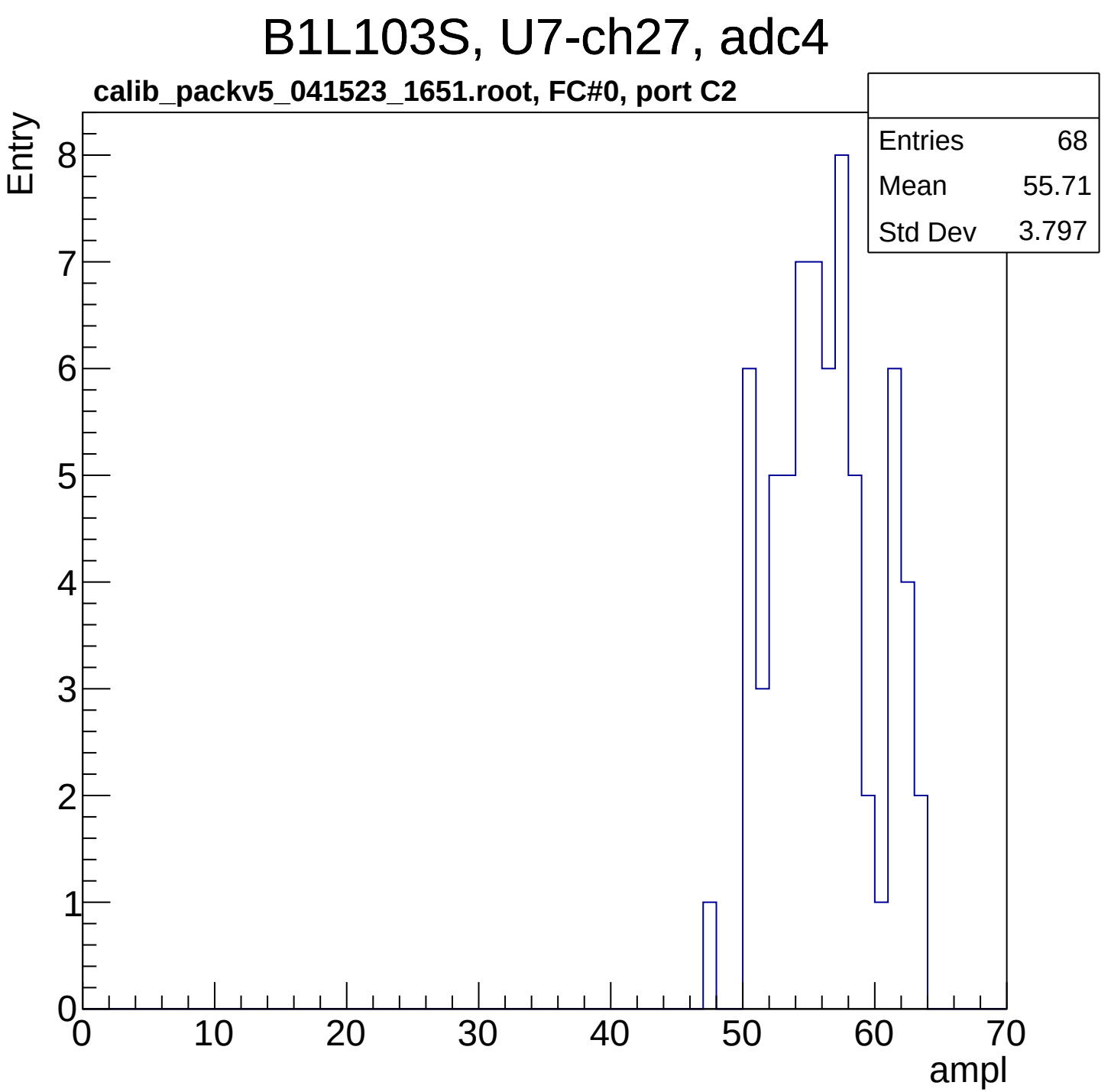
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch27, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 55.71
Std Dev 3.797
Entry
ampl
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2
3
4
5
6
7
8
0
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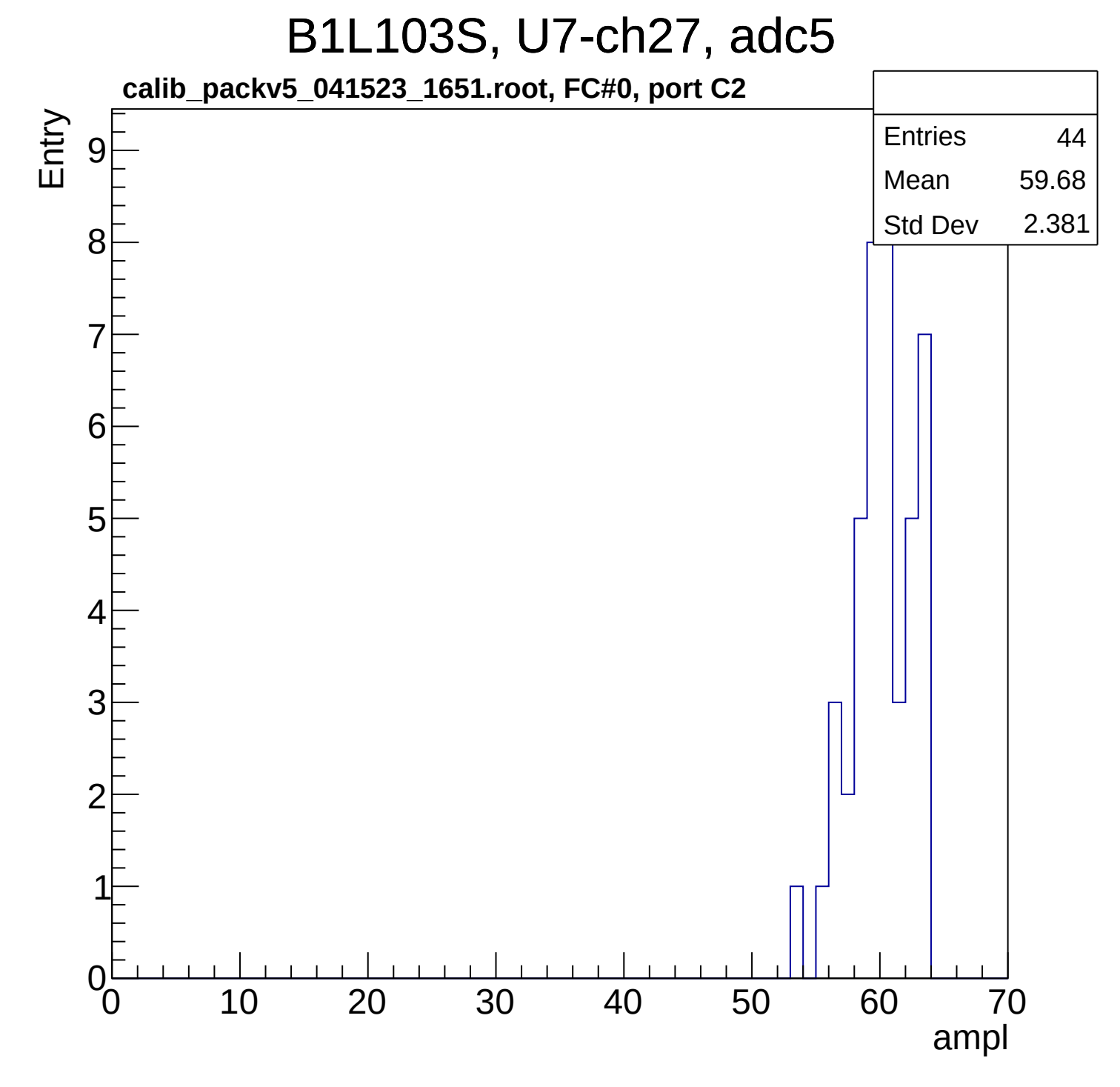
40
50
60
70


B1L103S, U7-ch27, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 59.68
Std Dev 2.381
Entry
ampl
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8
9
0
10
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40
50
60
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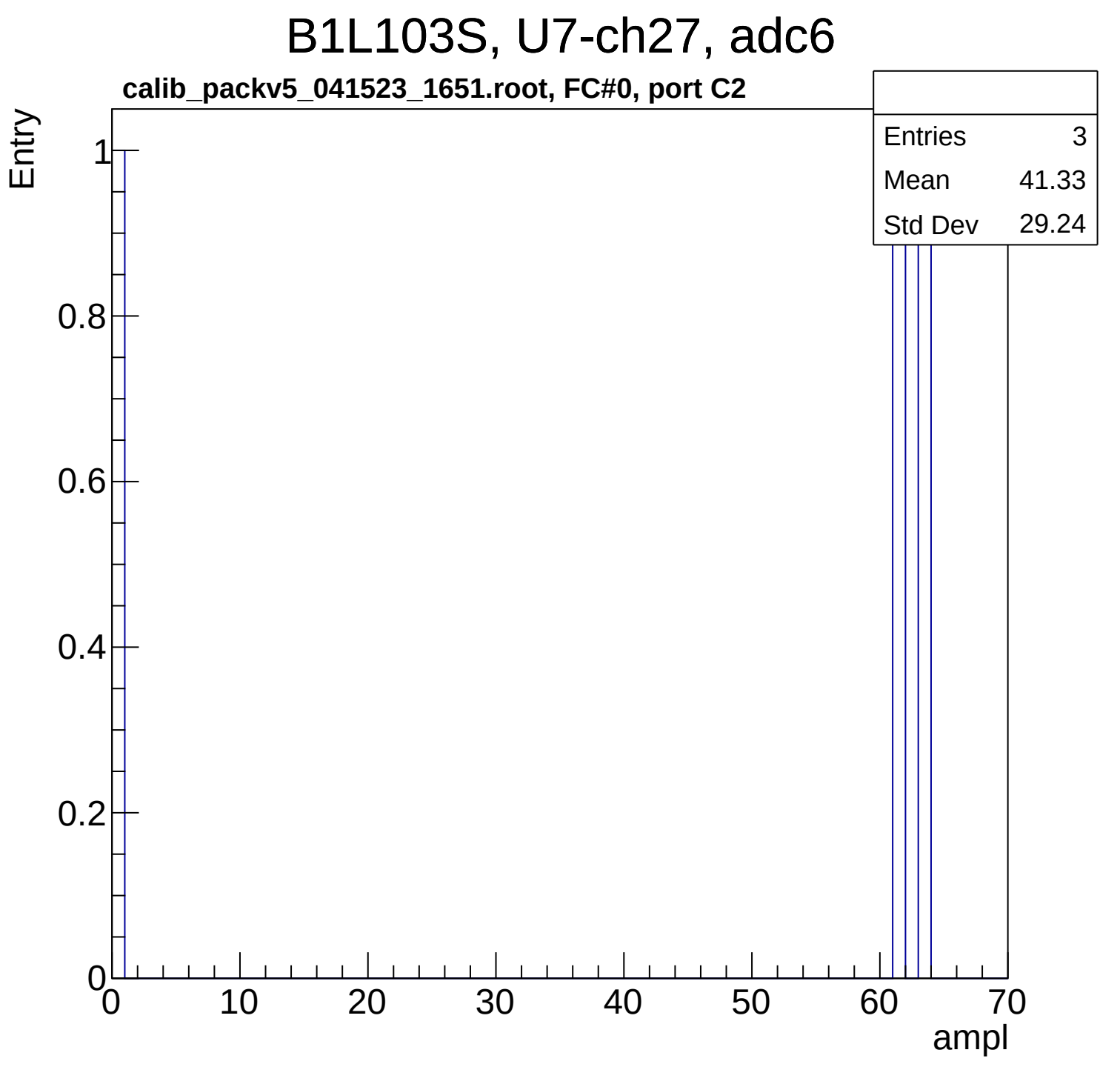
B1L103S, U7-ch27, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 3
Mean 41.33
Std Dev 29.24
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
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20
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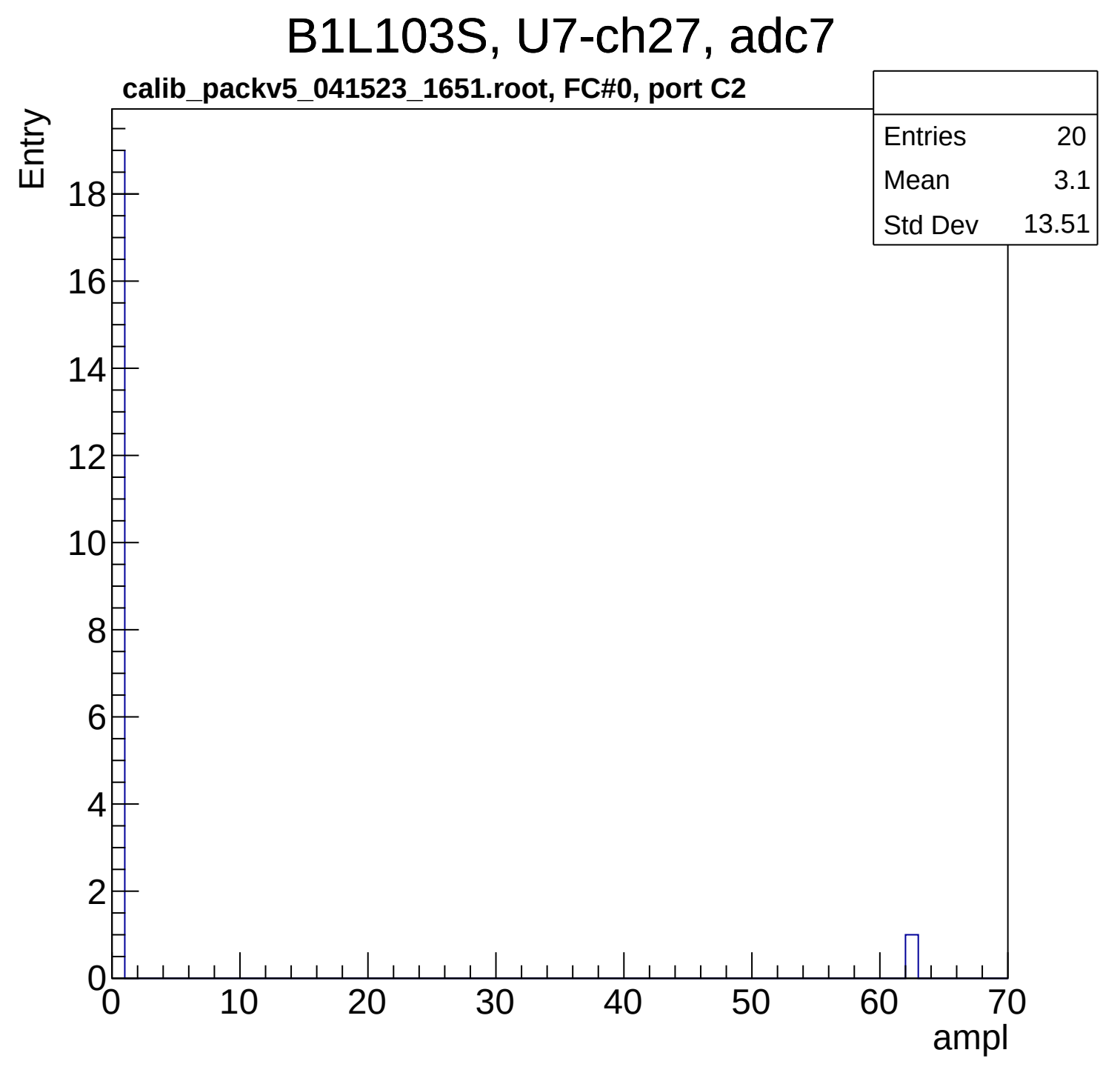
40
50
60
70


B1L103S, U7-ch27, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.1
Std Dev 13.51
Entry
0
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6
8
10
12
14
16
18
0
10
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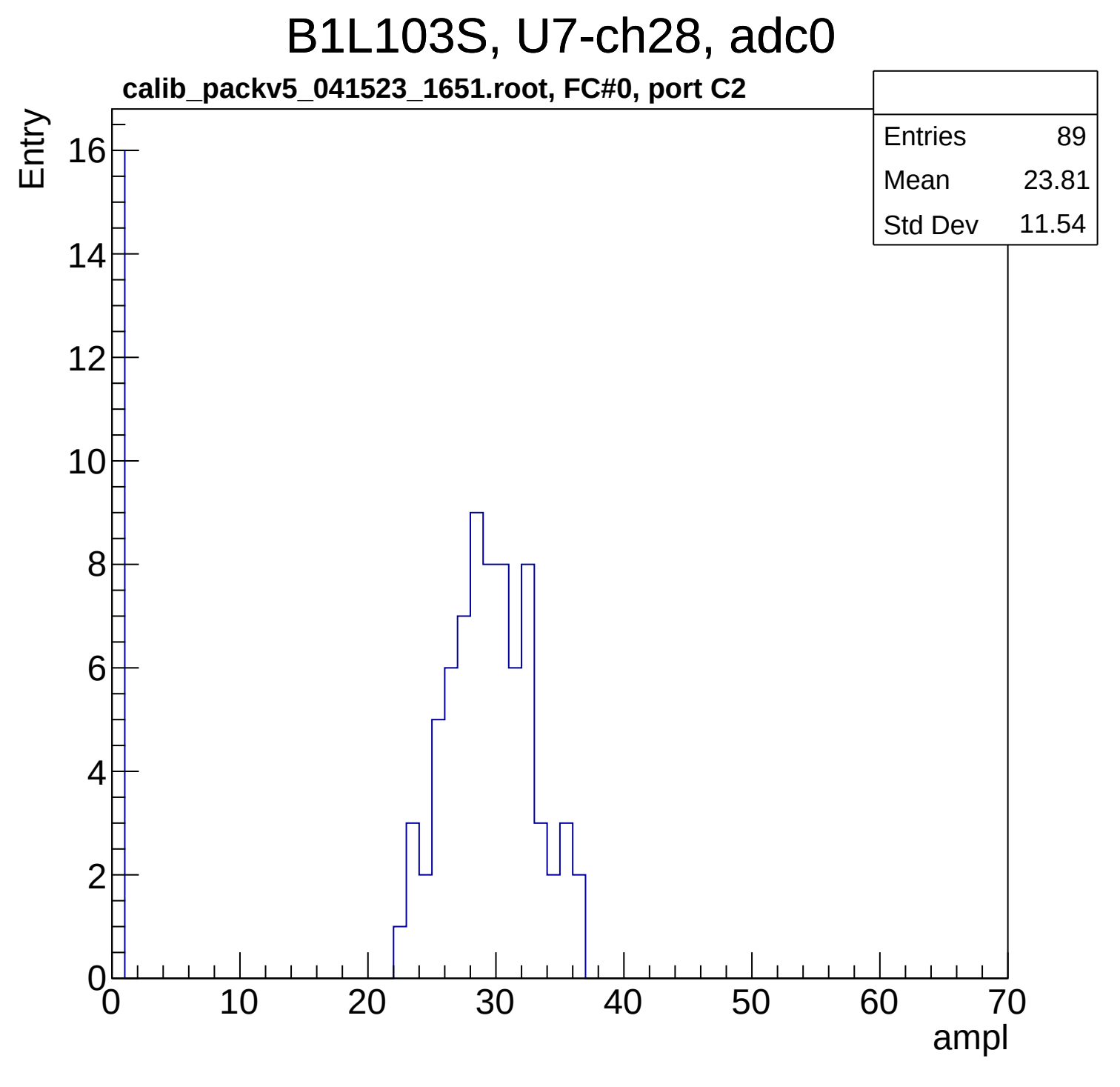
70
ampl


B1L103S, U7-ch28, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 89
Mean 23.81
Std Dev 11.54
Entry
ampl
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2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
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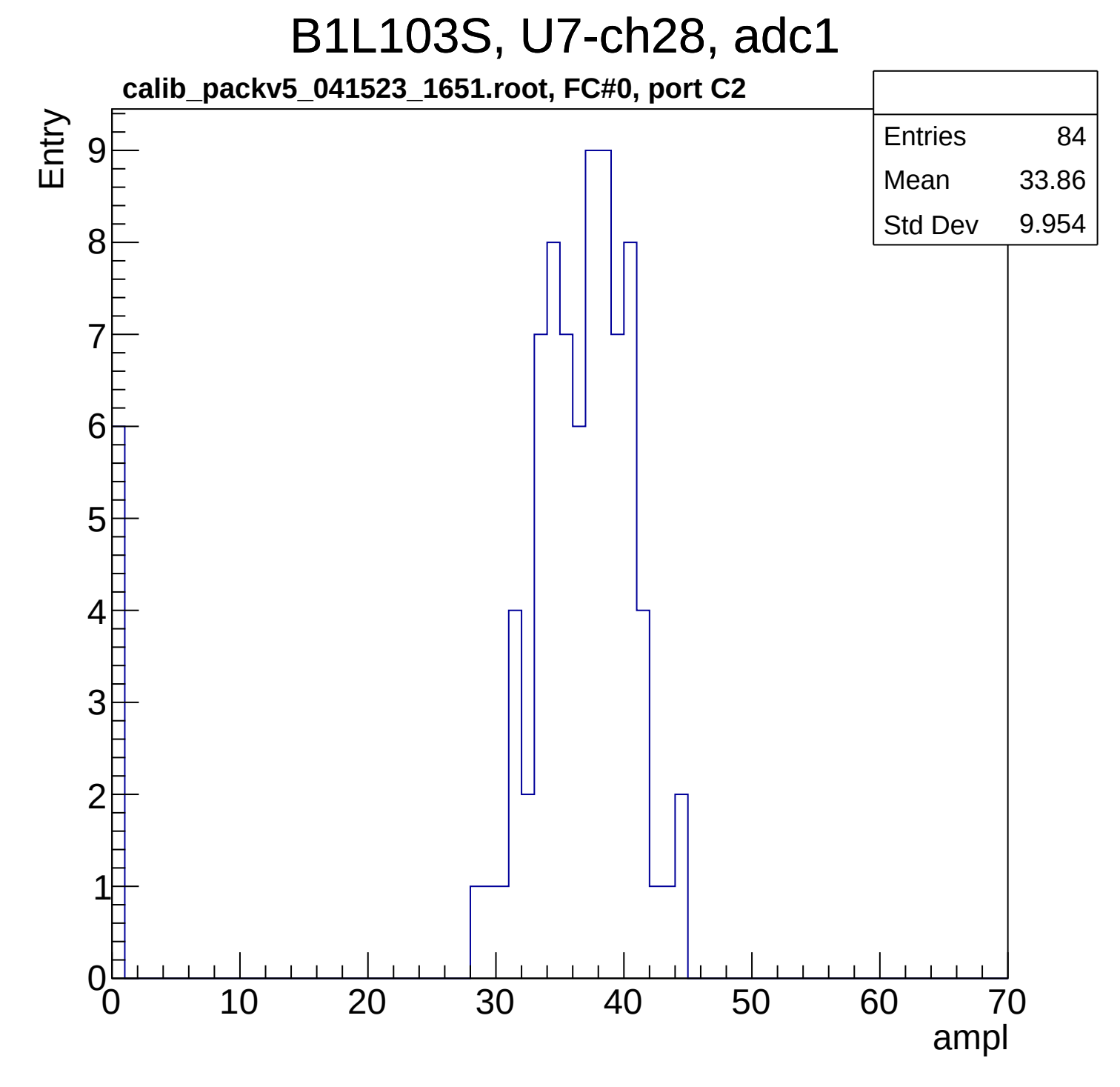
B1L103S, U7-ch28, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 33.86
Std Dev 9.954
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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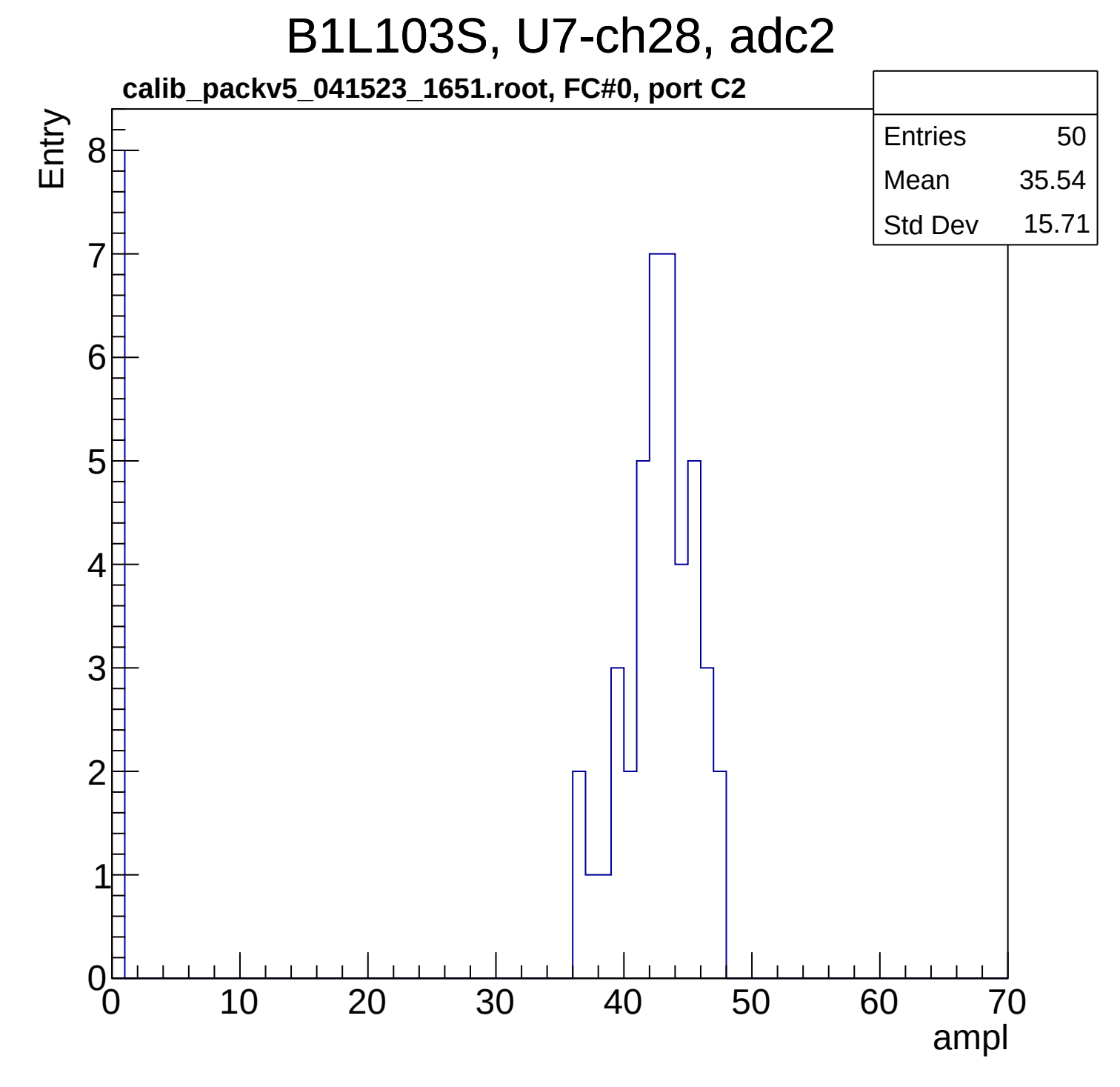
B1L103S, U7-ch28, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 35.54
Std Dev 15.71
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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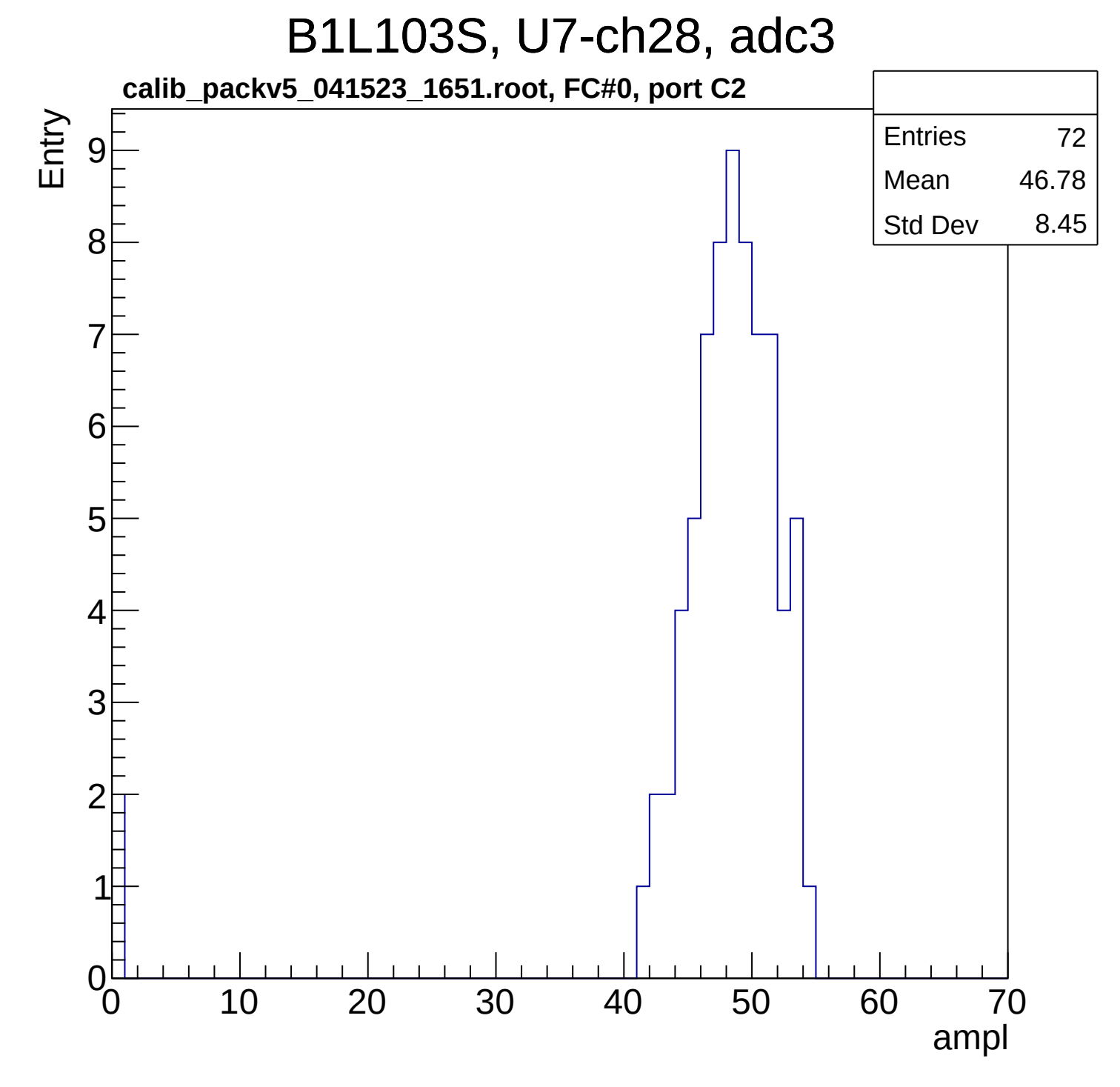
B1L103S, U7-ch28, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 46.78
Std Dev 8.45
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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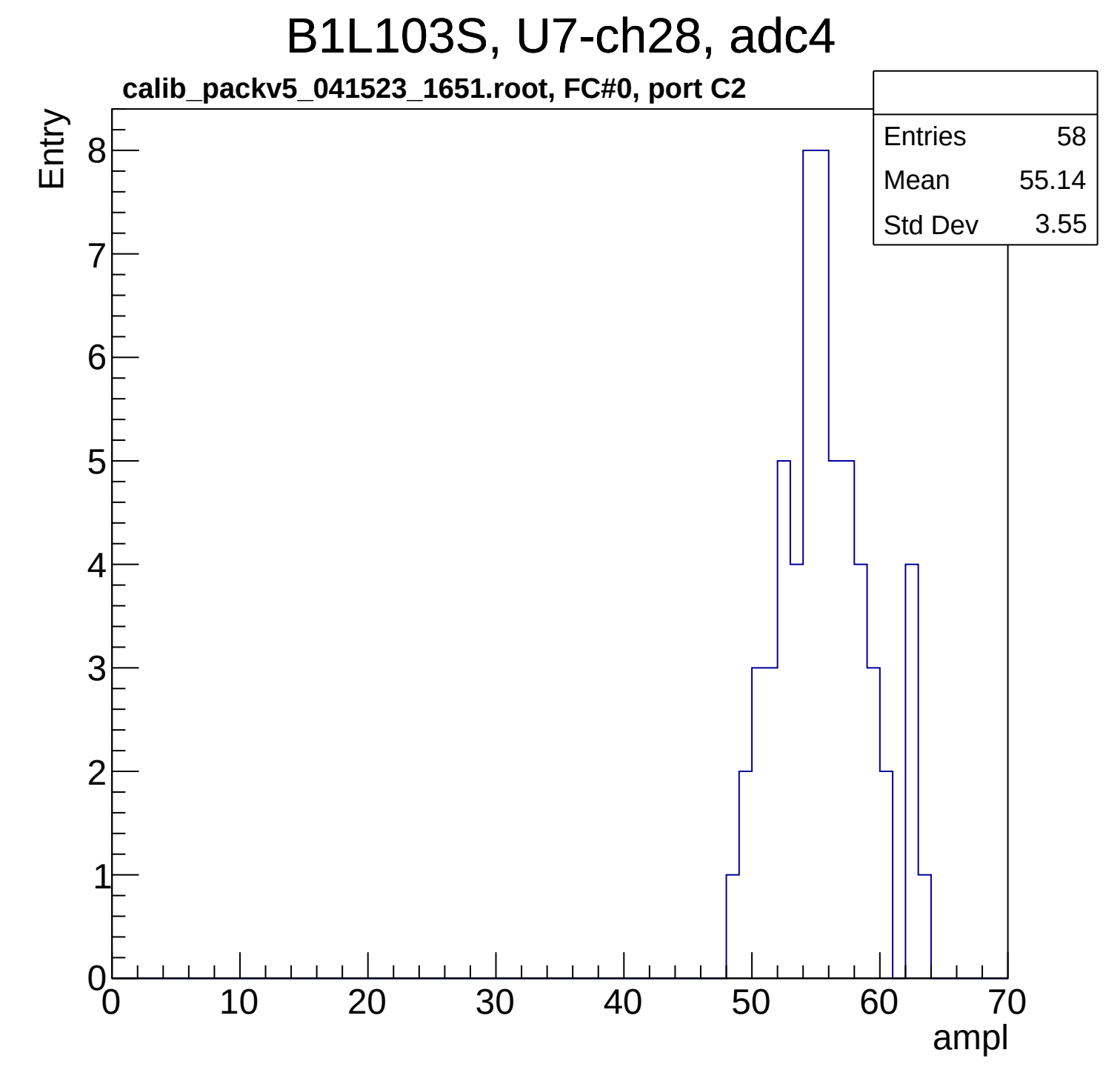
B1L103S, U7-ch28, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 55.14
Std Dev 3.55
Entry
ampl
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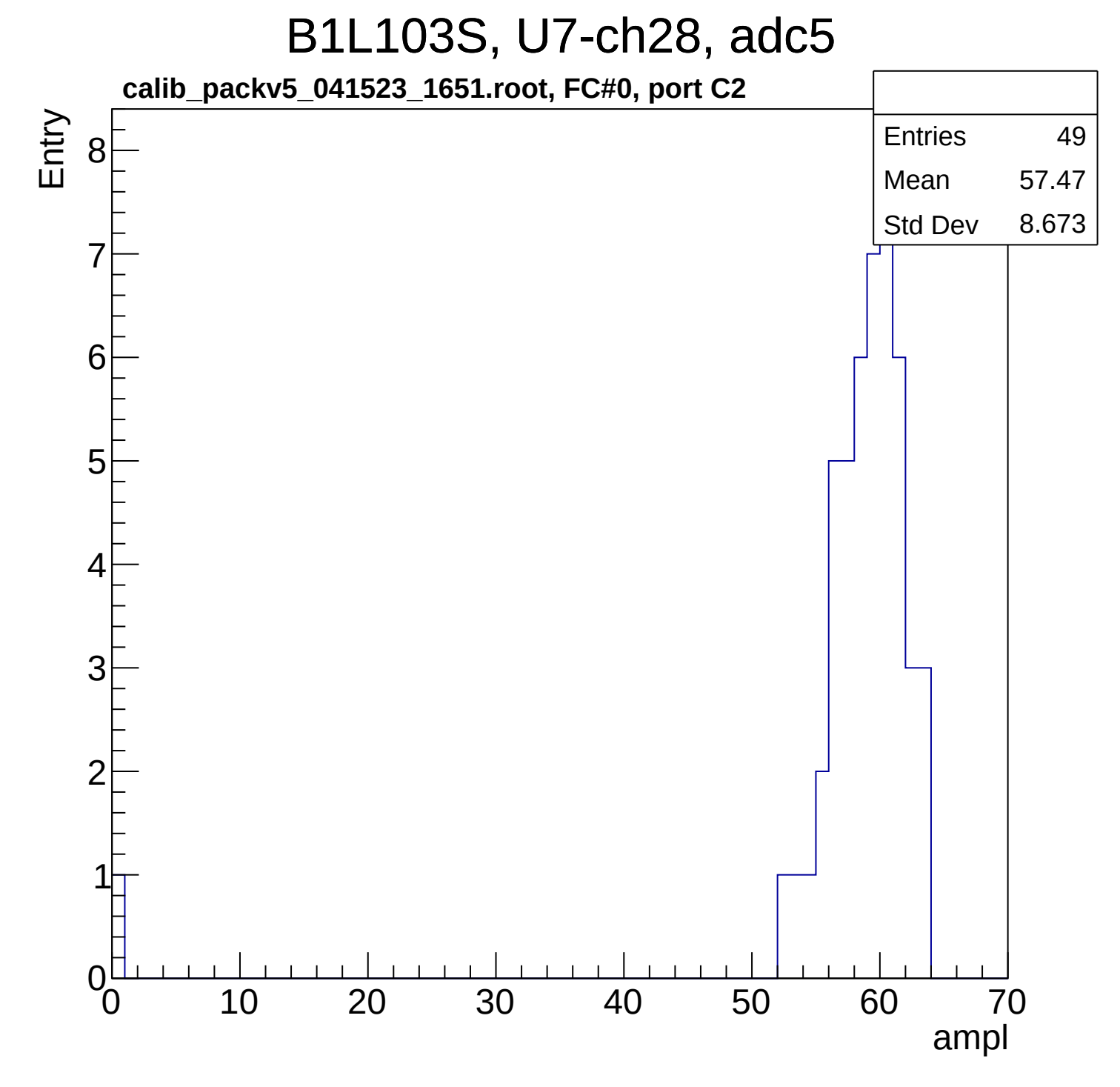
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch28, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 57.47
Std Dev 8.673
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
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60
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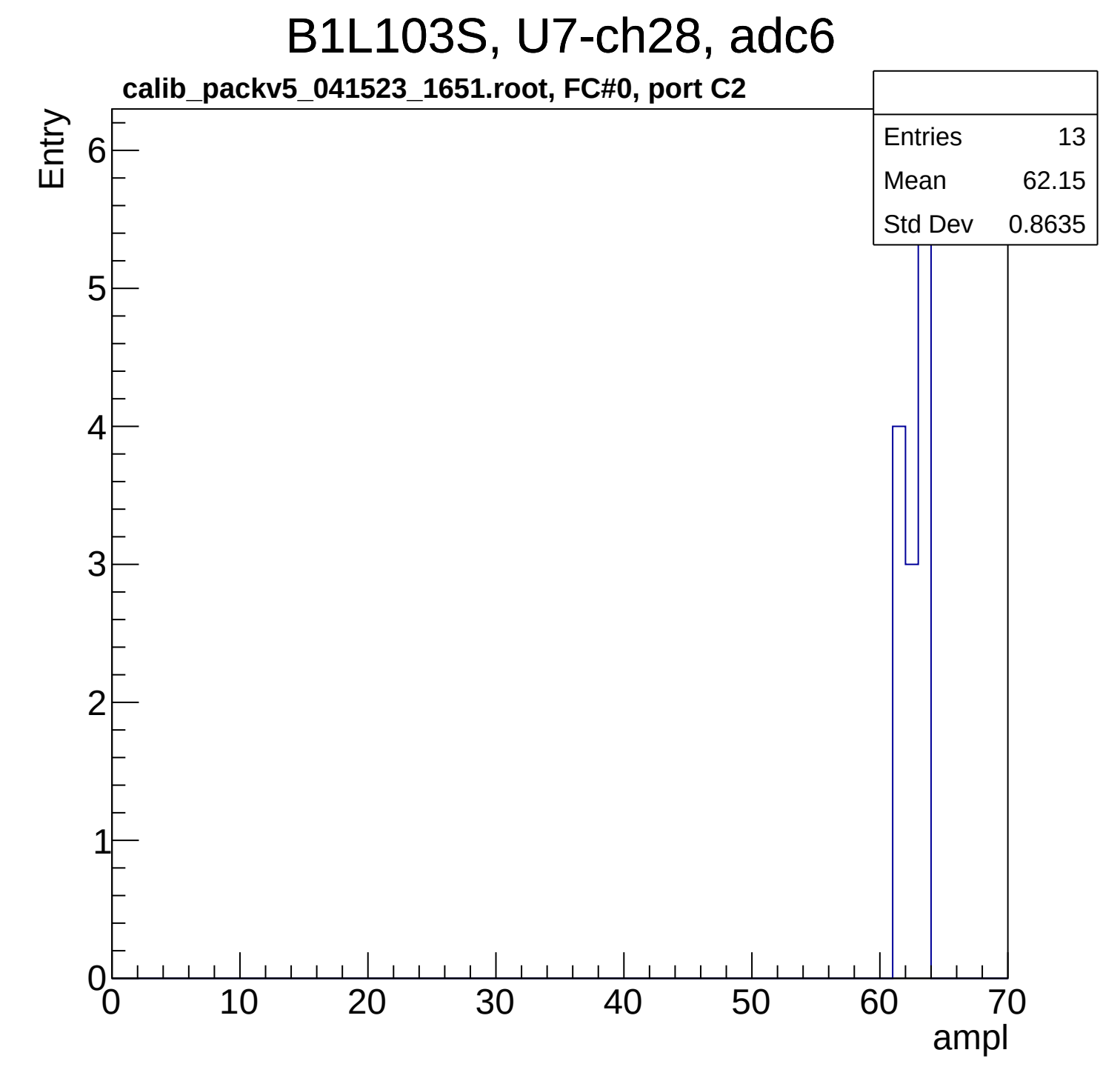
B1L103S, U7-ch28, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 13
Mean 62.15
Std Dev 0.8635
Entry
ampl
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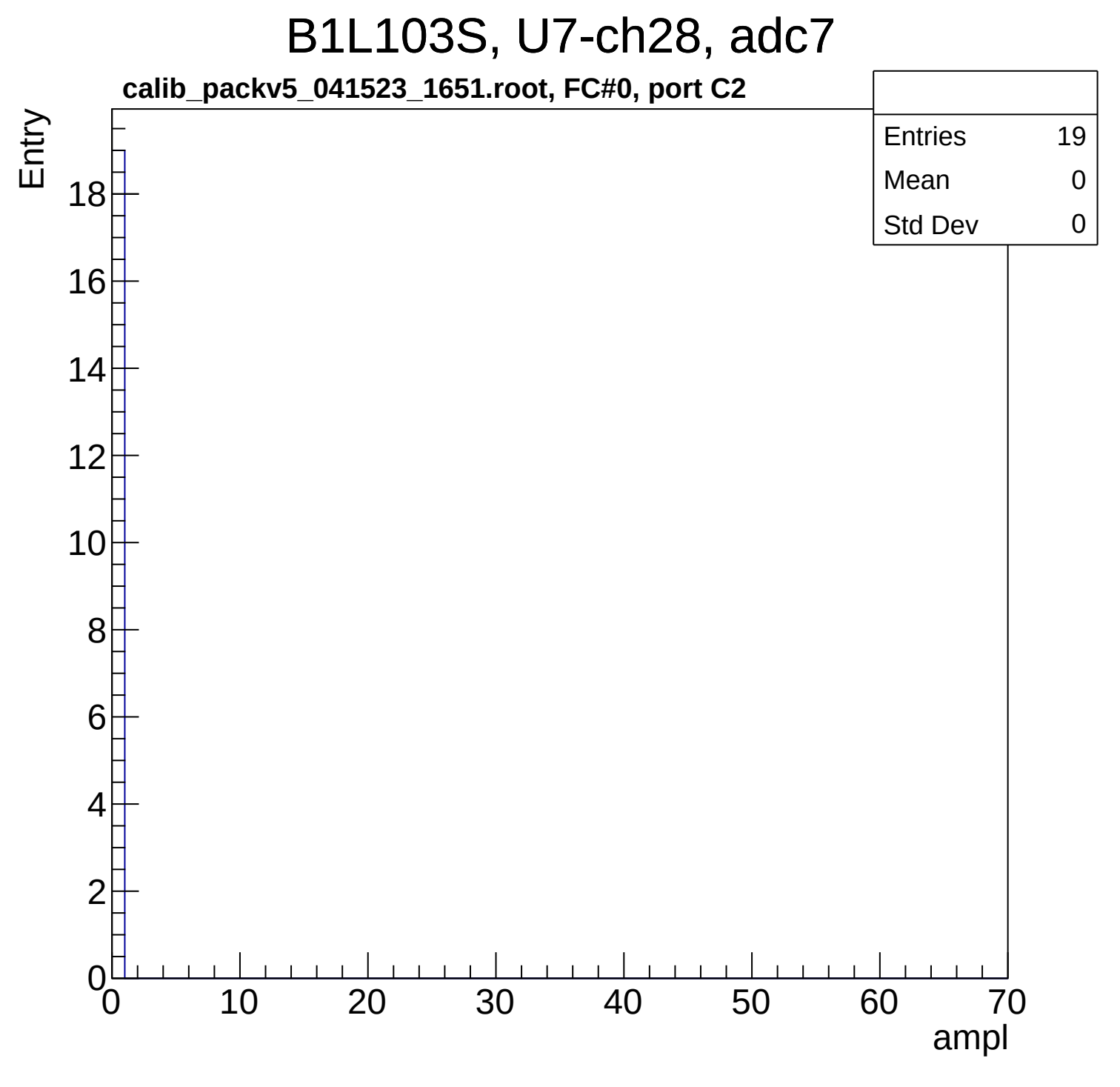
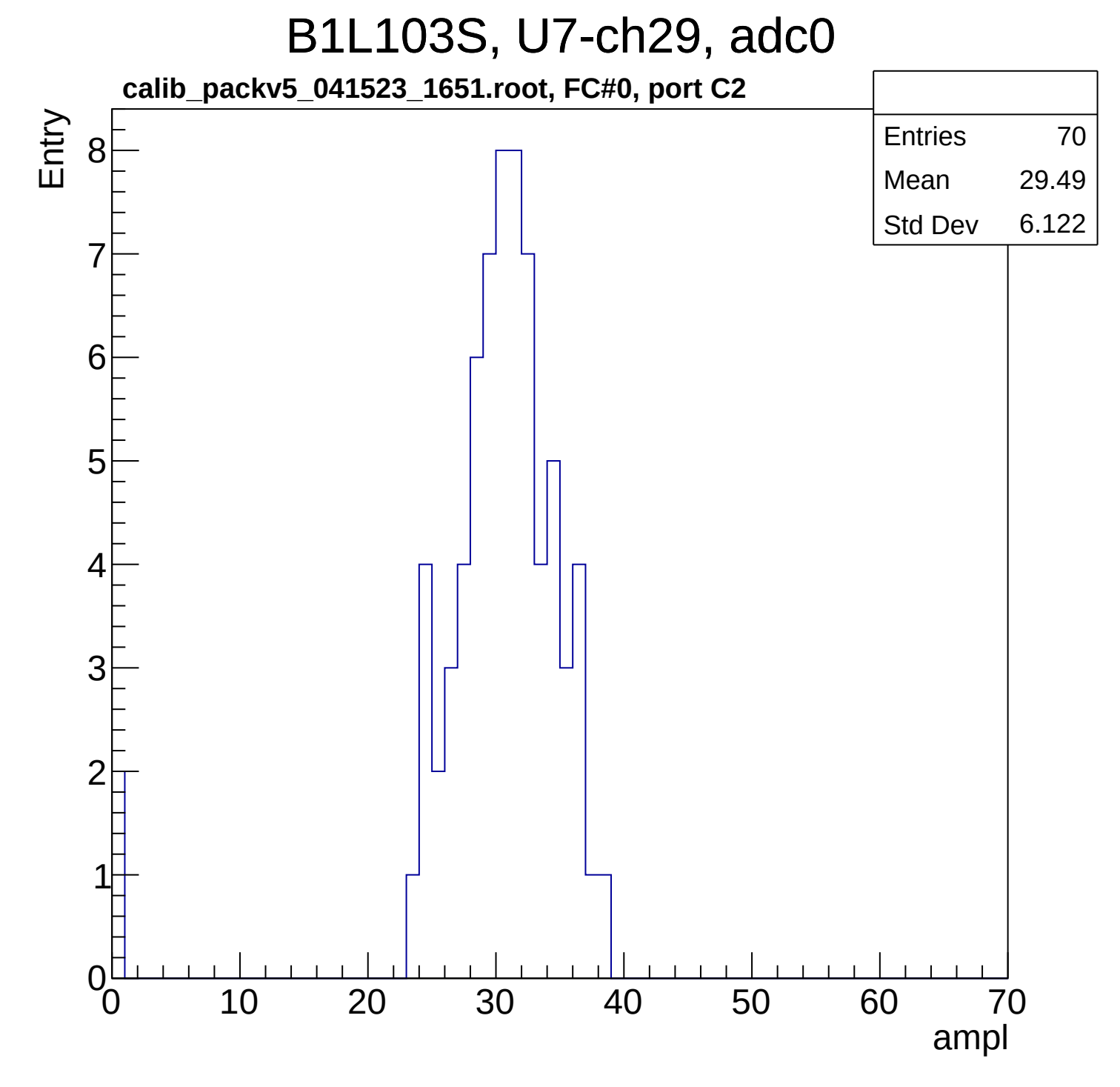
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U7-ch28, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch29, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 29.49
Std Dev 6.122
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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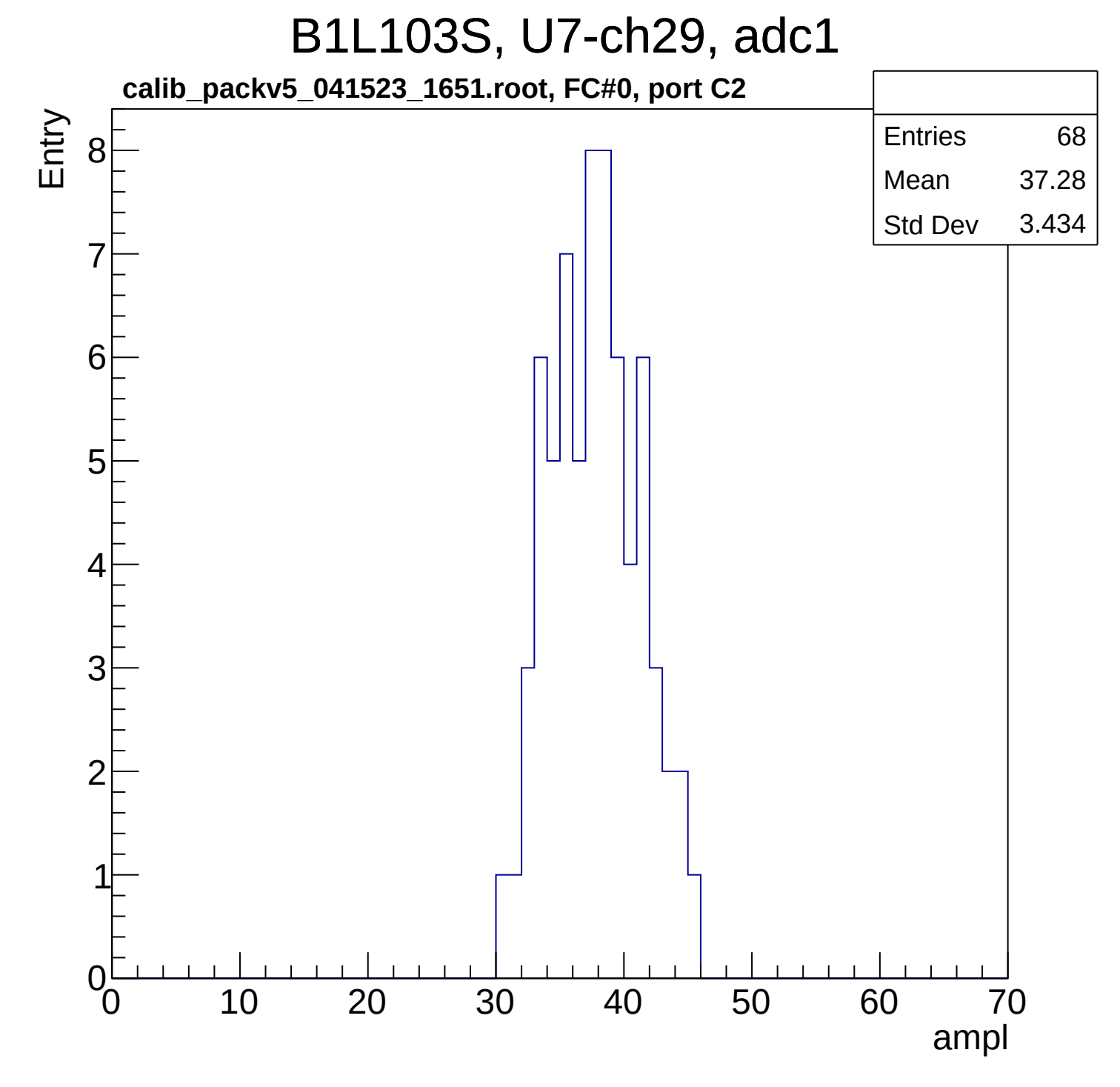
B1L103S, U7-ch29, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 37.28
Std Dev 3.434
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
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60
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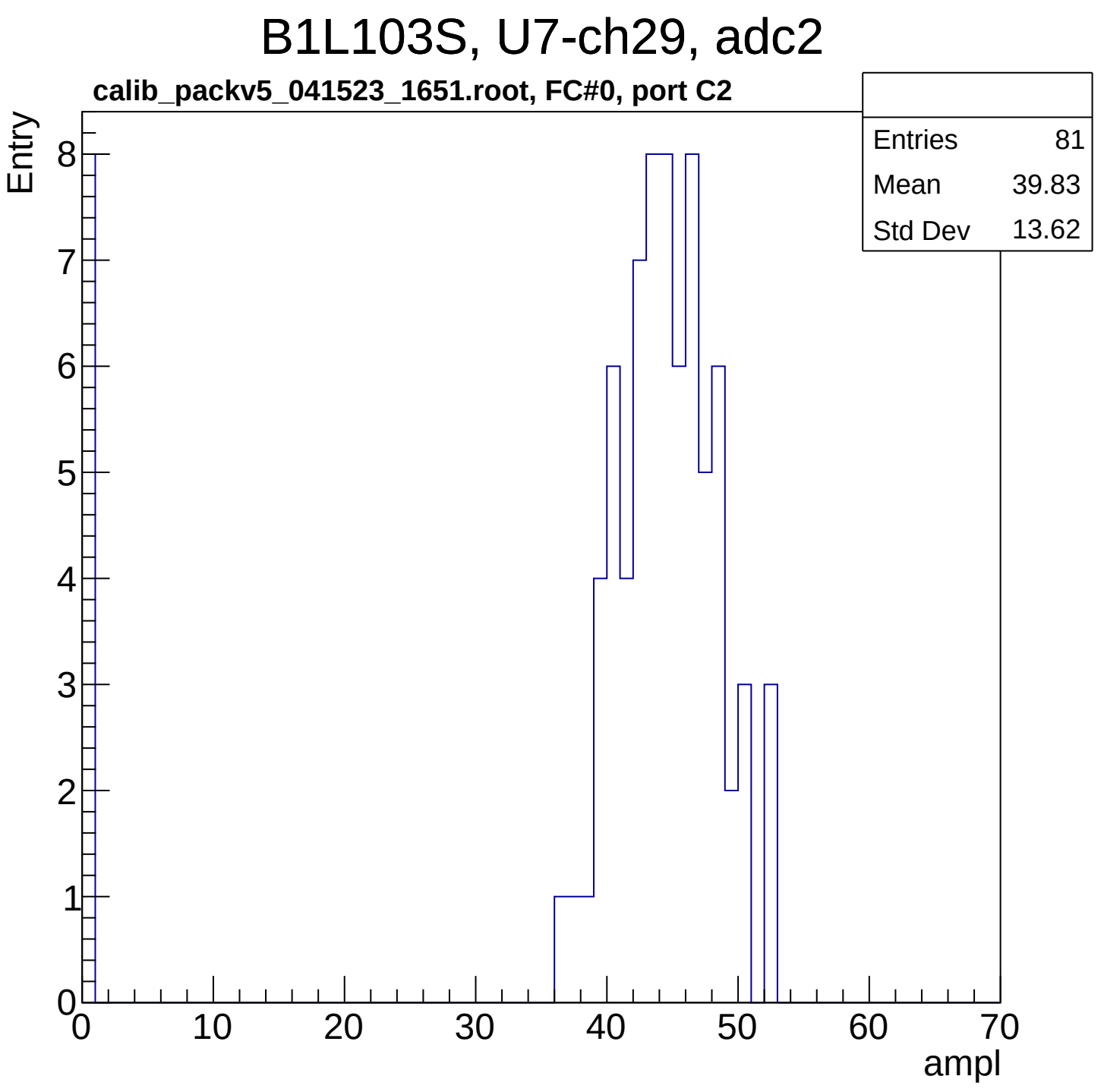
B1L103S, U7-ch29, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 39.83
Std Dev 13.62
Entry
ampl
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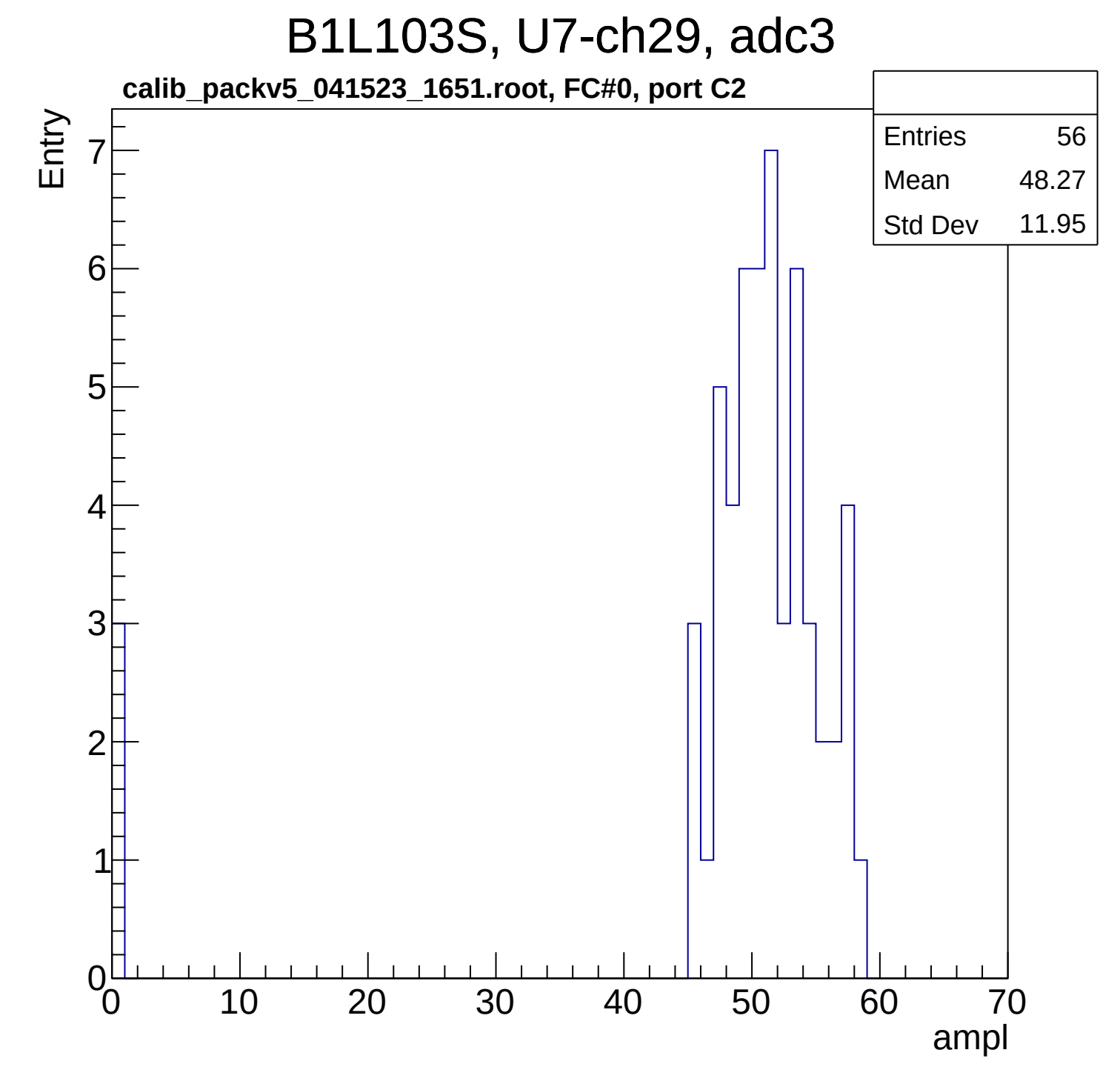
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch29, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 48.27
Std Dev 11.95
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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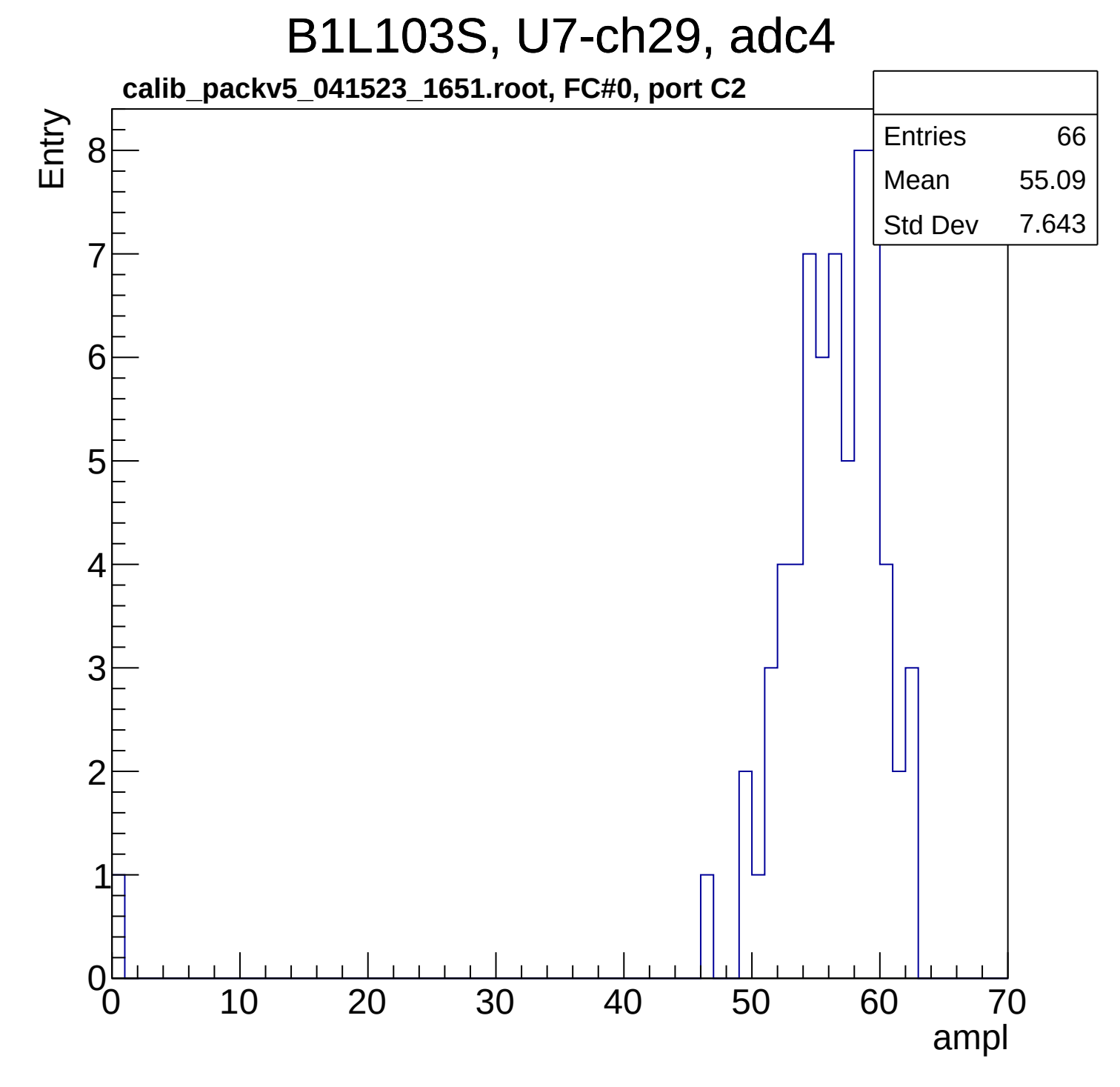
B1L103S, U7-ch29, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 55.09
Std Dev 7.643
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
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60
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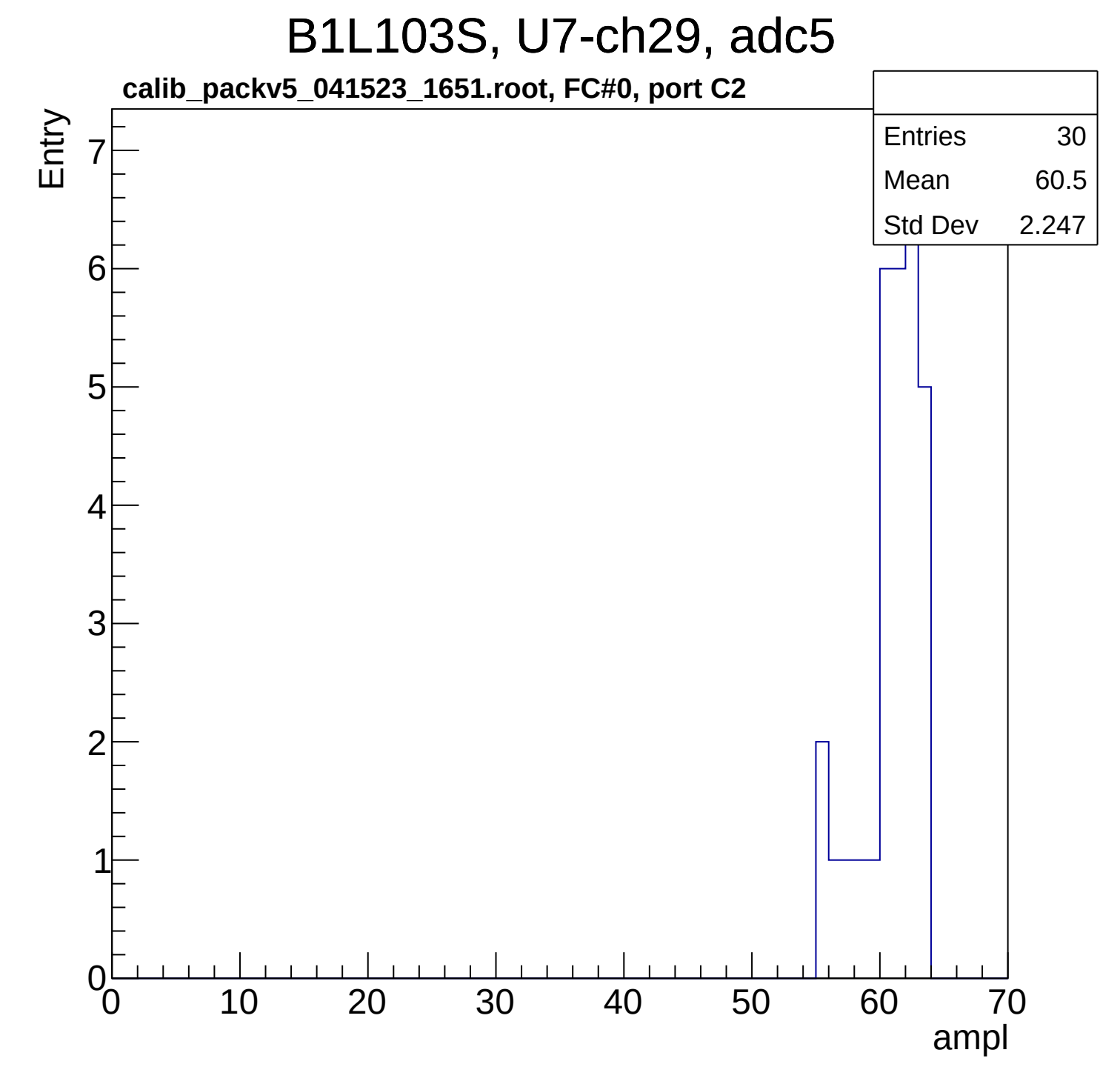
B1L103S, U7-ch29, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 30
Mean 60.5
Std Dev 2.247
Entry
ampl
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2
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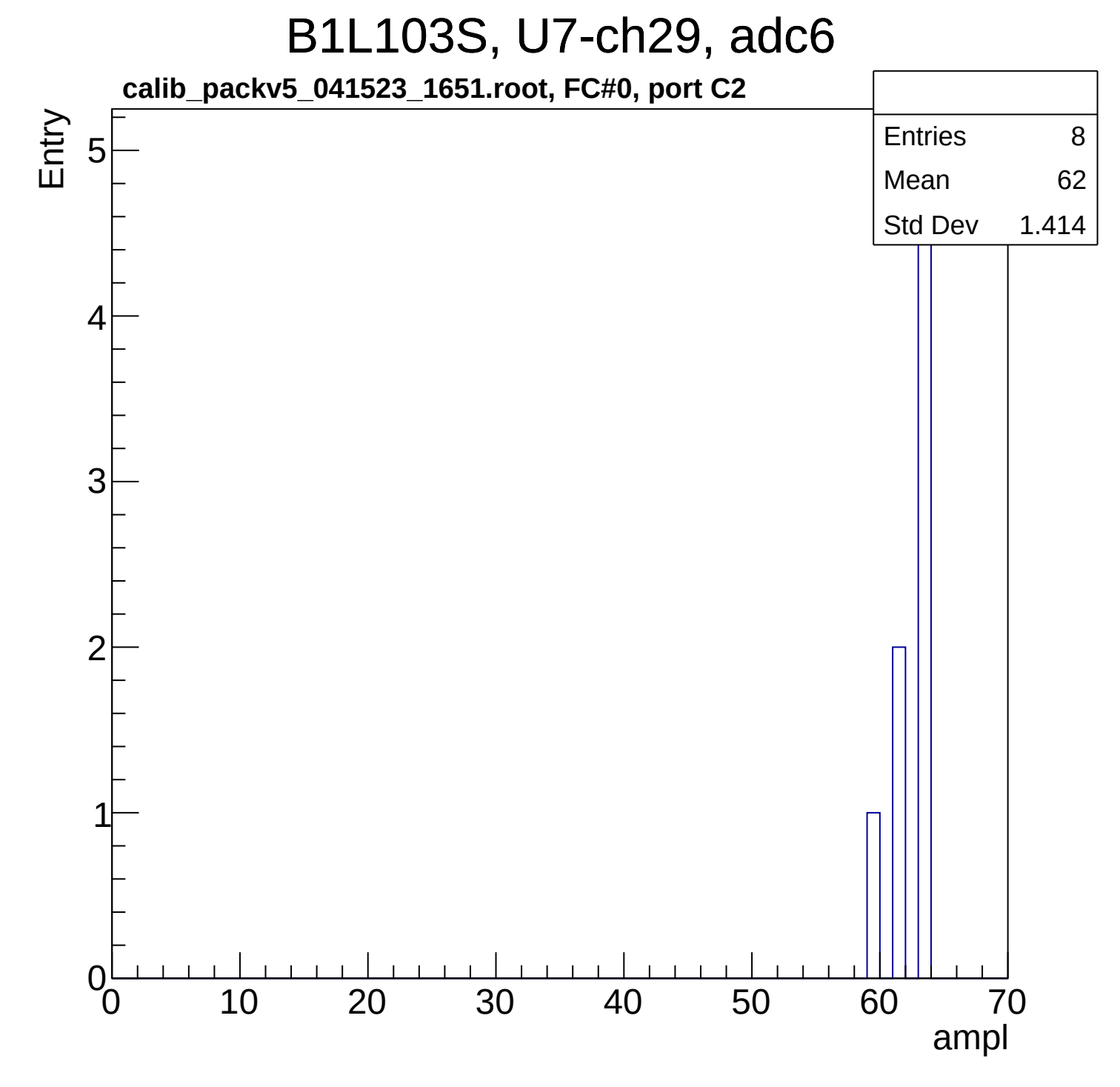
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U7-ch29, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 62
Std Dev 1.414
Entry
ampl
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1
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3
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5
0
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20
30
40
50
60
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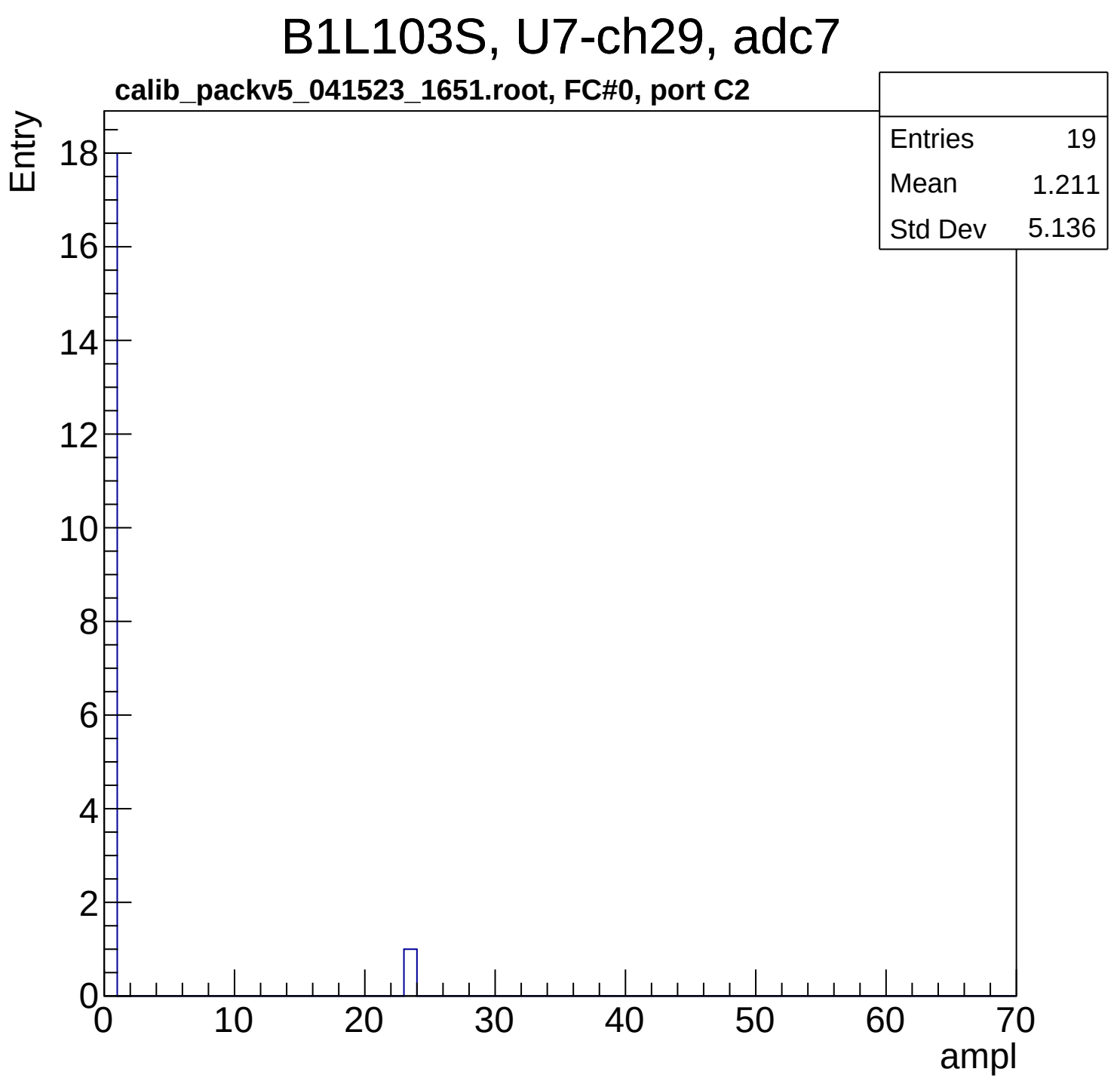
B1L103S, U7-ch29, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.211
Std Dev 5.136
Entry
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6
8
10
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14
16
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10
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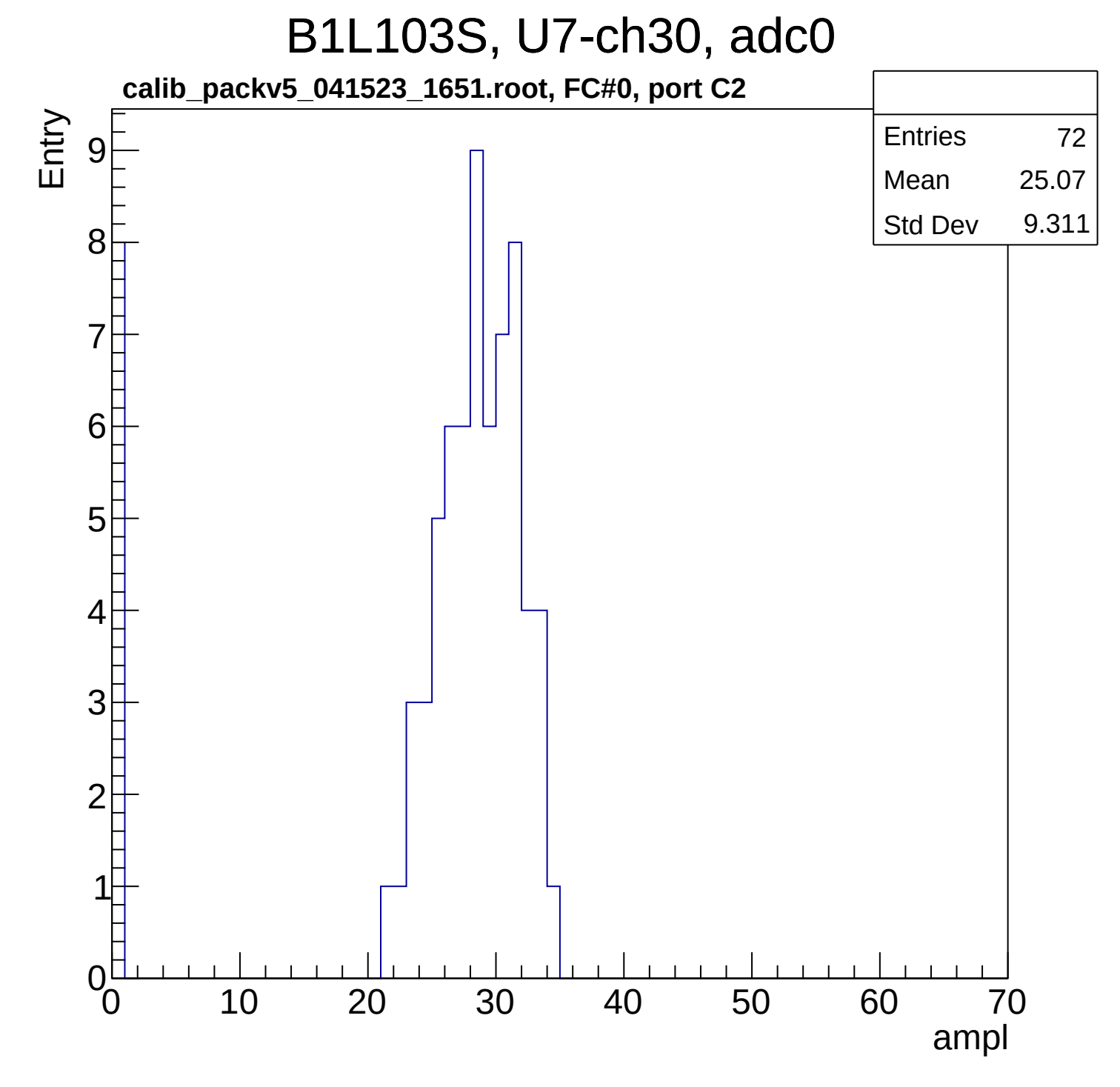
50
60
70
ampl


B1L103S, U7-ch30, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 25.07
Std Dev 9.311
Entry
ampl
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2
3
4
5
6
7
8
9
0
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40
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60
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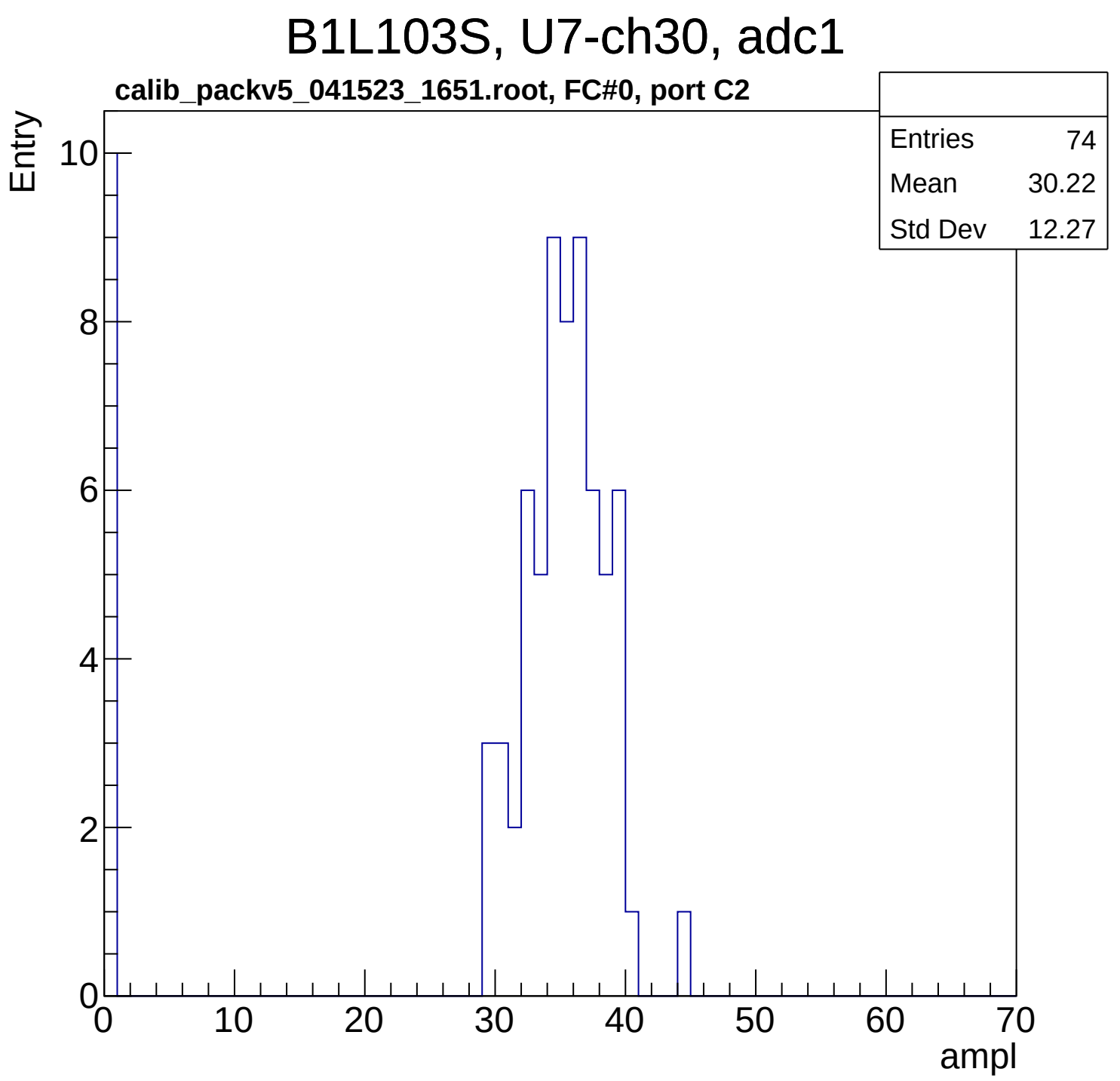
B1L103S, U7-ch30, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 30.22
Std Dev 12.27
Entry
ampl
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6
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0
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20
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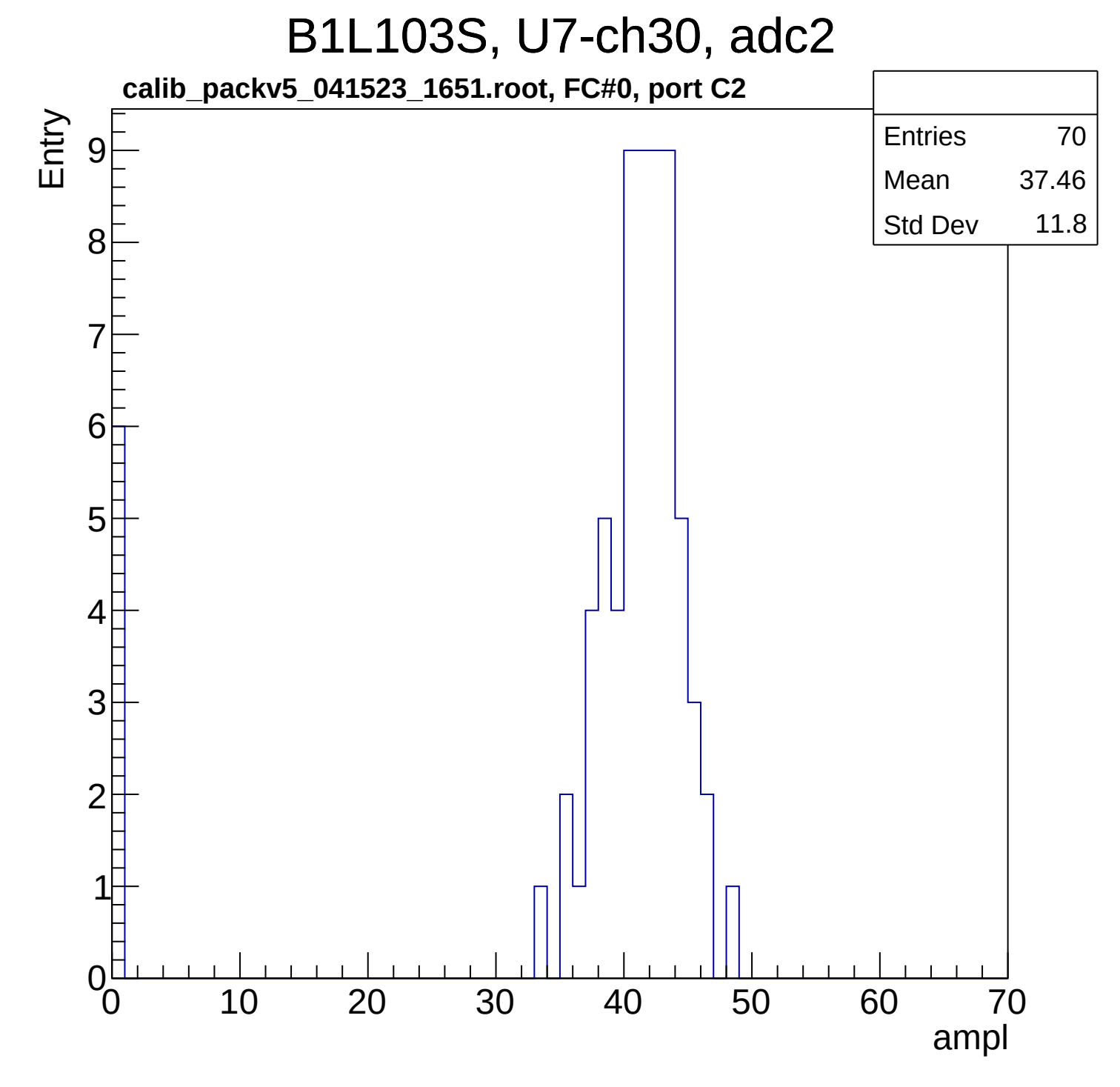
60
70


B1L103S, U7-ch30, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 37.46
Std Dev 11.8
Entry
ampl
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2
3
4
5
6
7
8
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0
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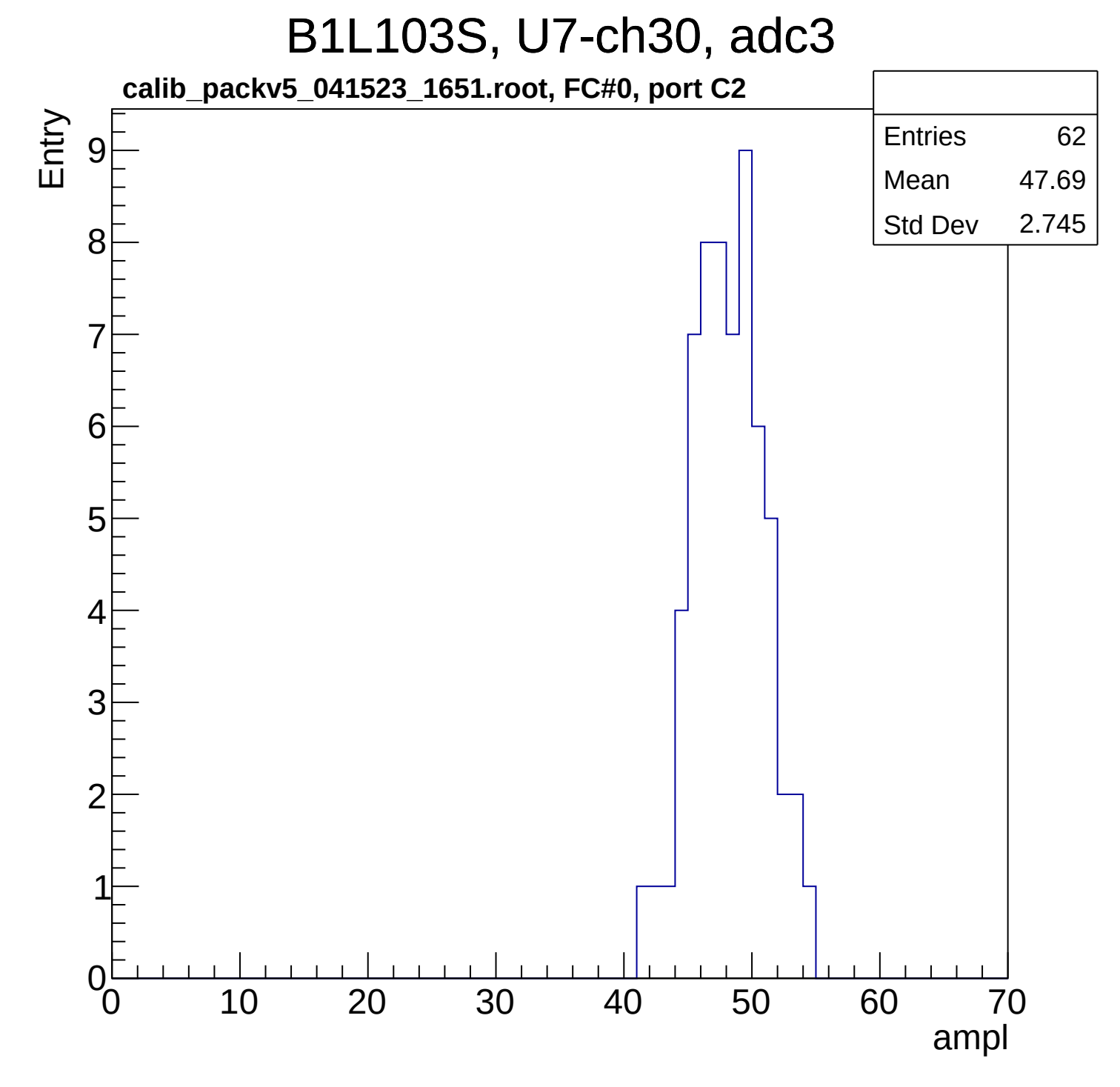
B1L103S, U7-ch30, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 47.69
Std Dev 2.745
Entry
ampl
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3
4
5
6
7
8
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0
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60
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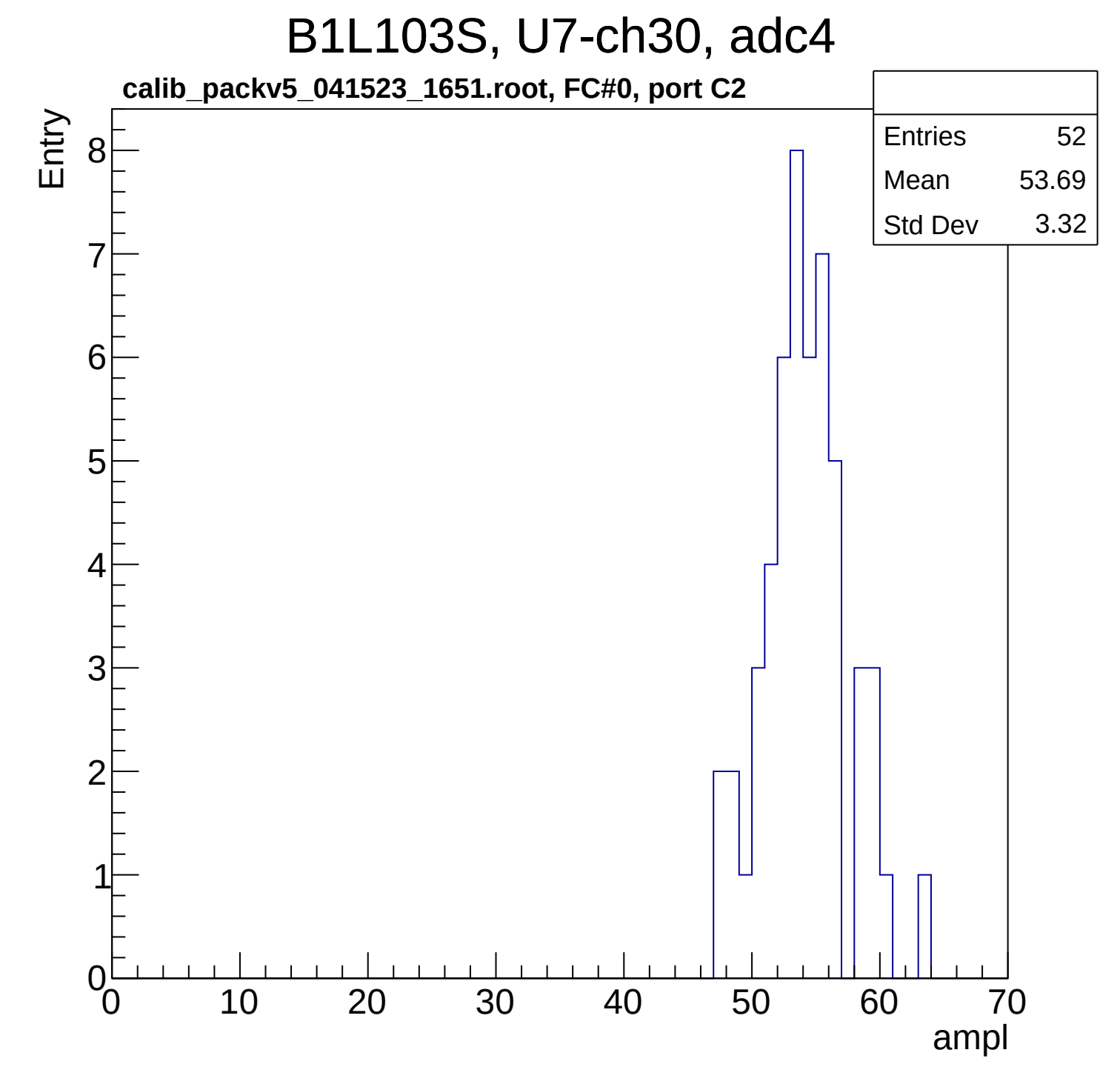
B1L103S, U7-ch30, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 53.69
Std Dev 3.32
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
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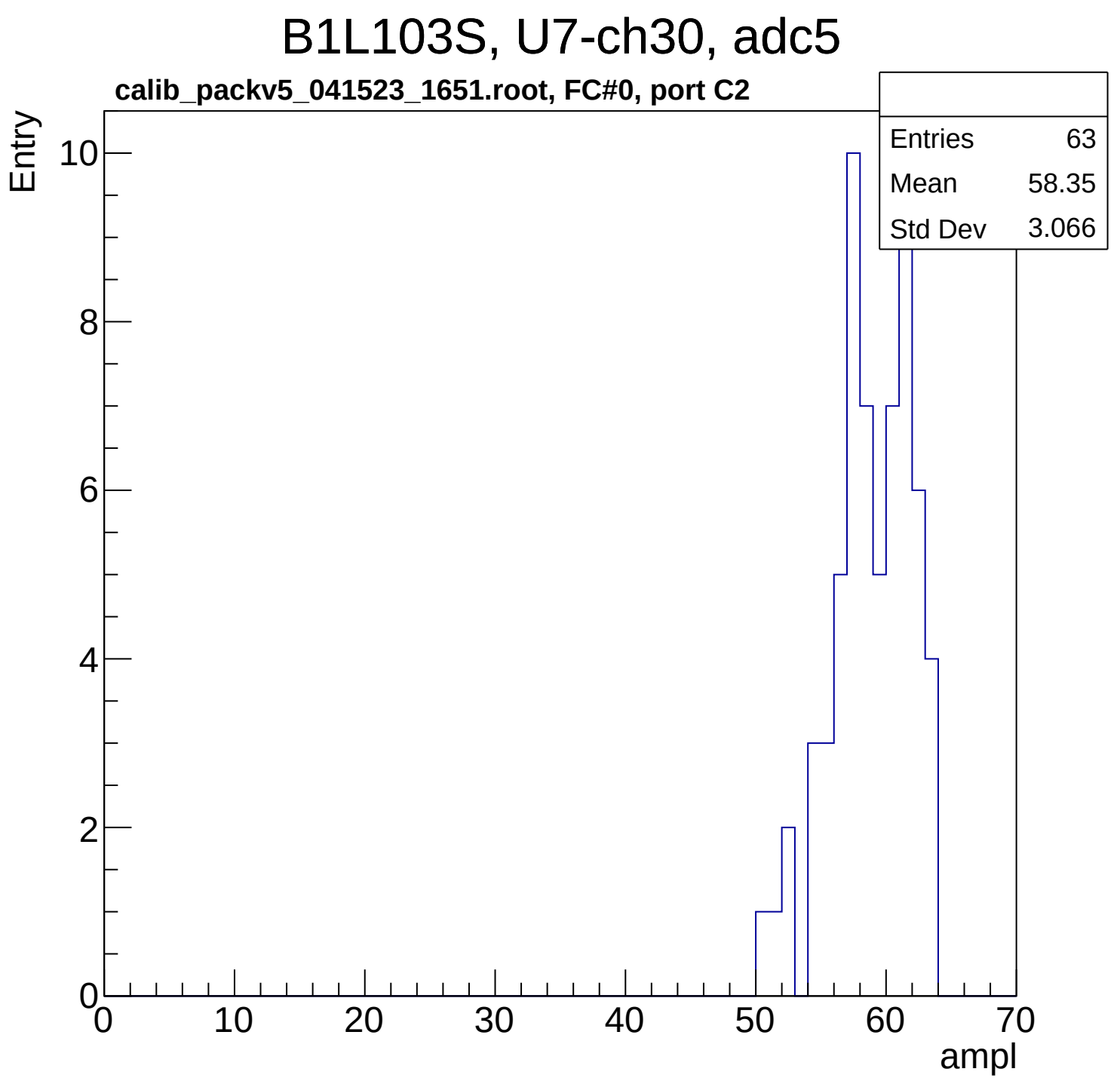
40
50
60
70


B1L103S, U7-ch30, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 58.35
Std Dev 3.066
Entry
ampl
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2
4
6
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0
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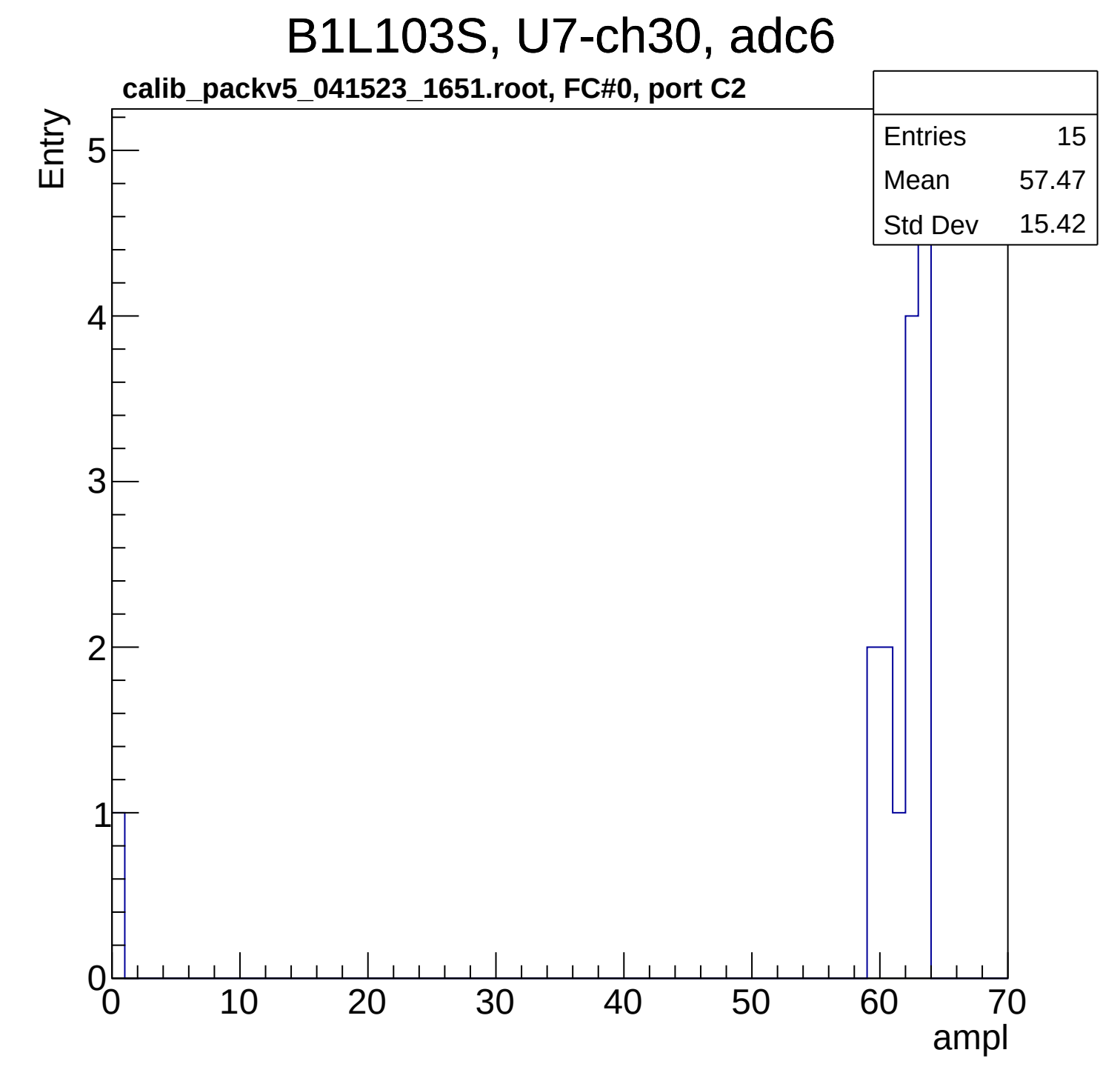
60
70


B1L103S, U7-ch30, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 15
Mean 57.47
Std Dev 15.42
Entry
ampl
0
1
2
3
4
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0
10
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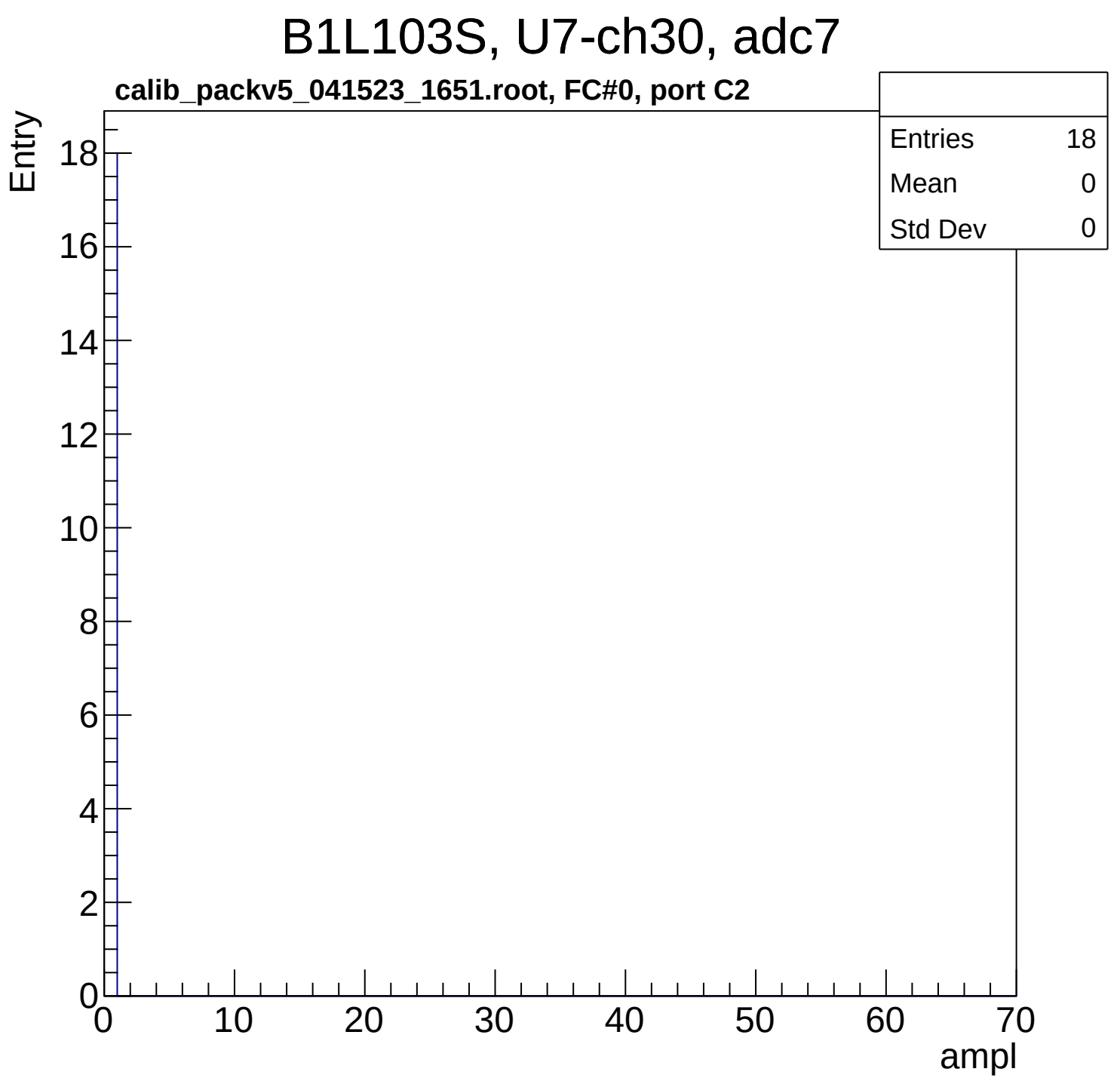
60
70


B1L103S, U7-ch30, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
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6
8
10
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14
16
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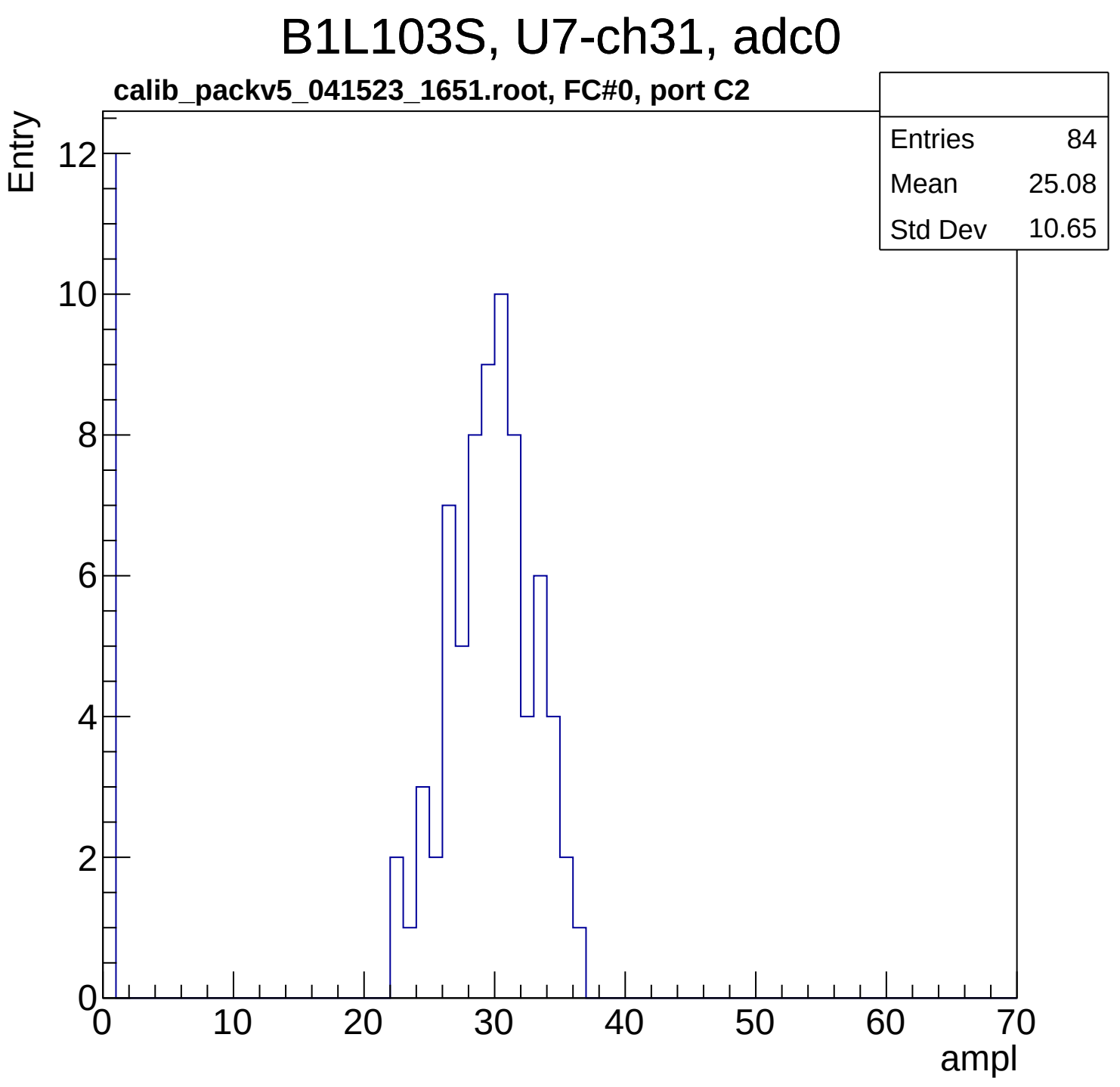
70
ampl


B1L103S, U7-ch31, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 25.08
Std Dev 10.65
Entry
0
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8
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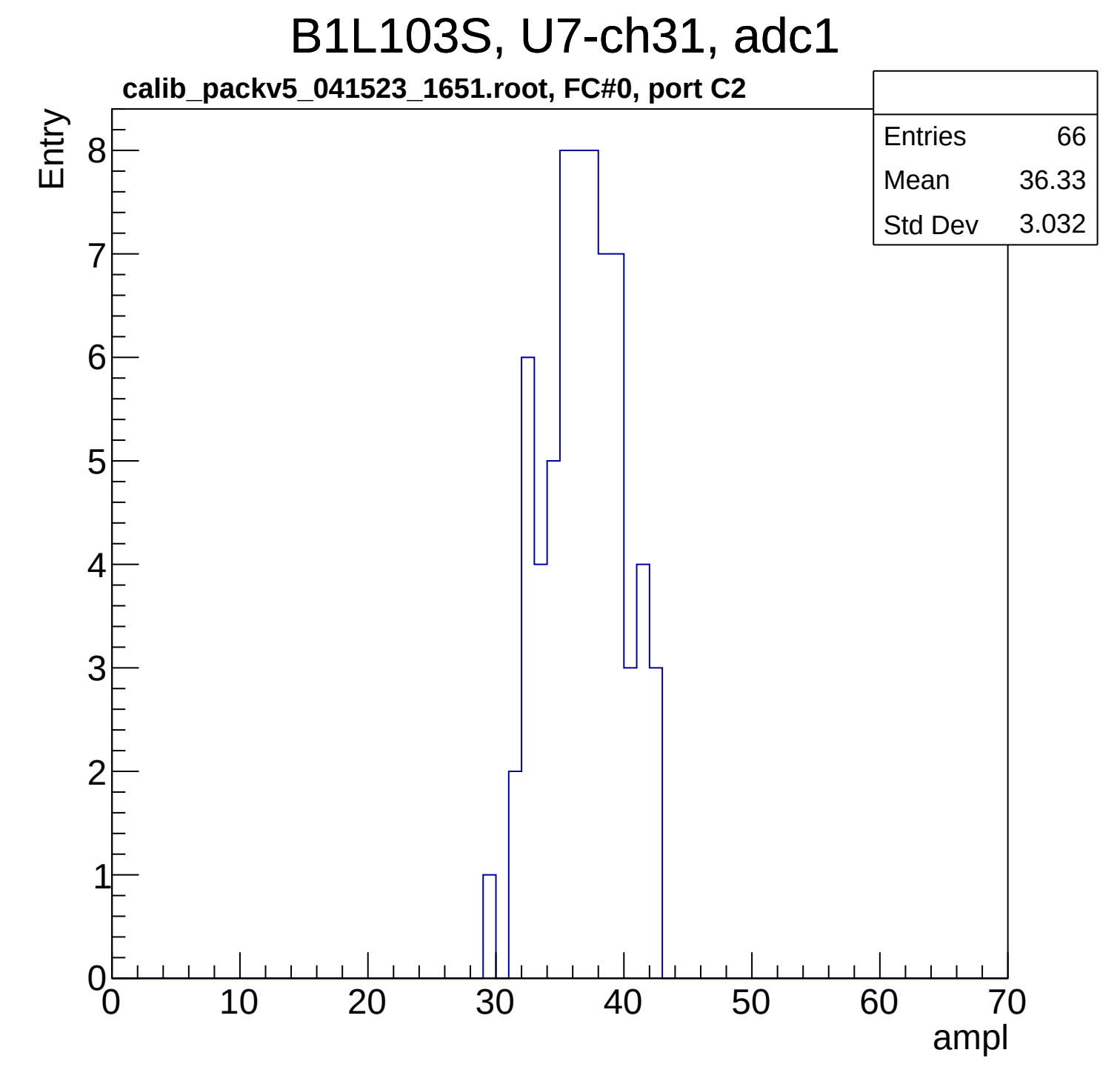
70
ampl


B1L103S, U7-ch31, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 36.33
Std Dev 3.032
Entry
ampl
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2
3
4
5
6
7
8
0
10
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60
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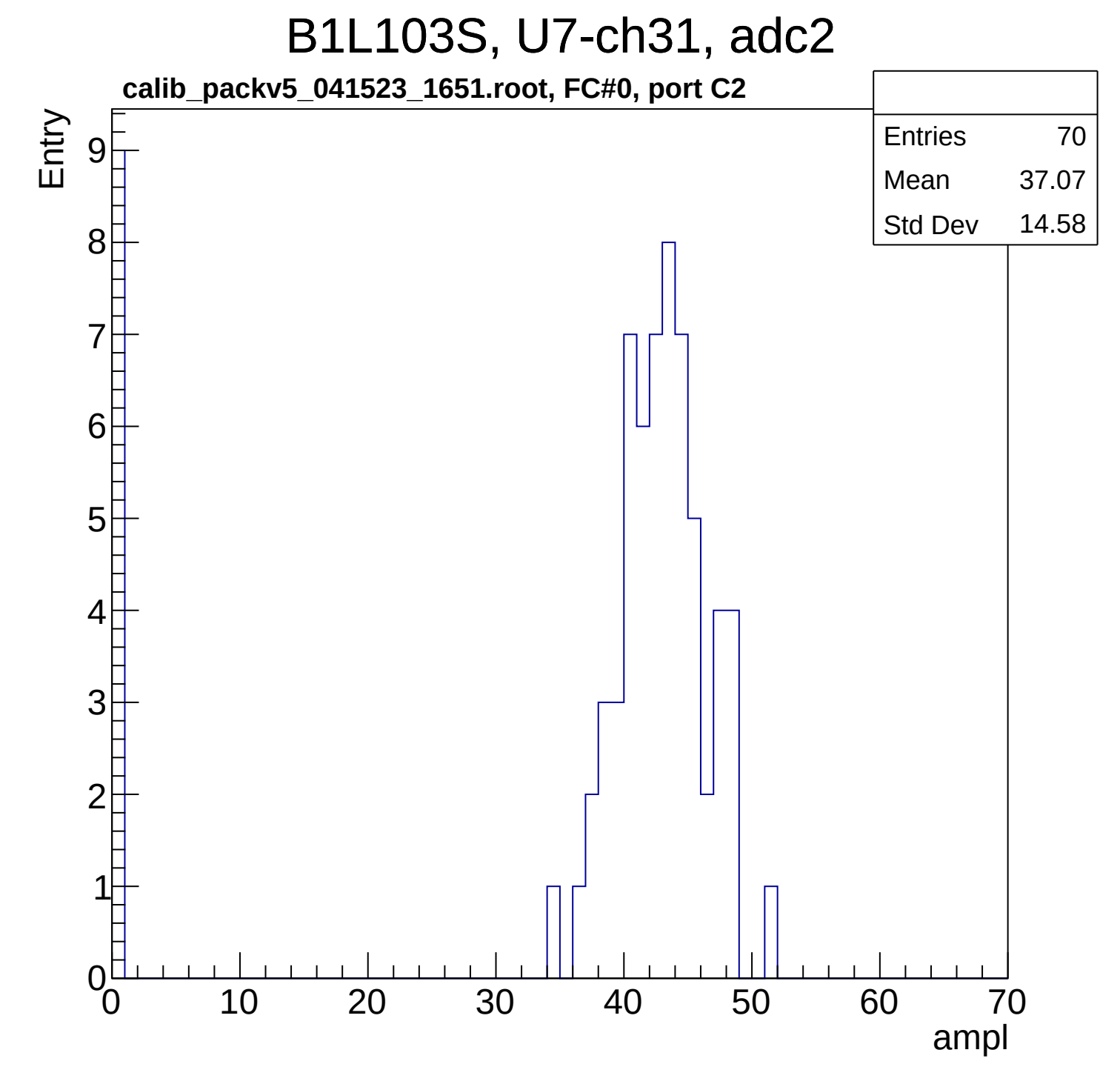
B1L103S, U7-ch31, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 37.07
Std Dev 14.58
Entry
ampl
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2
3
4
5
6
7
8
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0
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60
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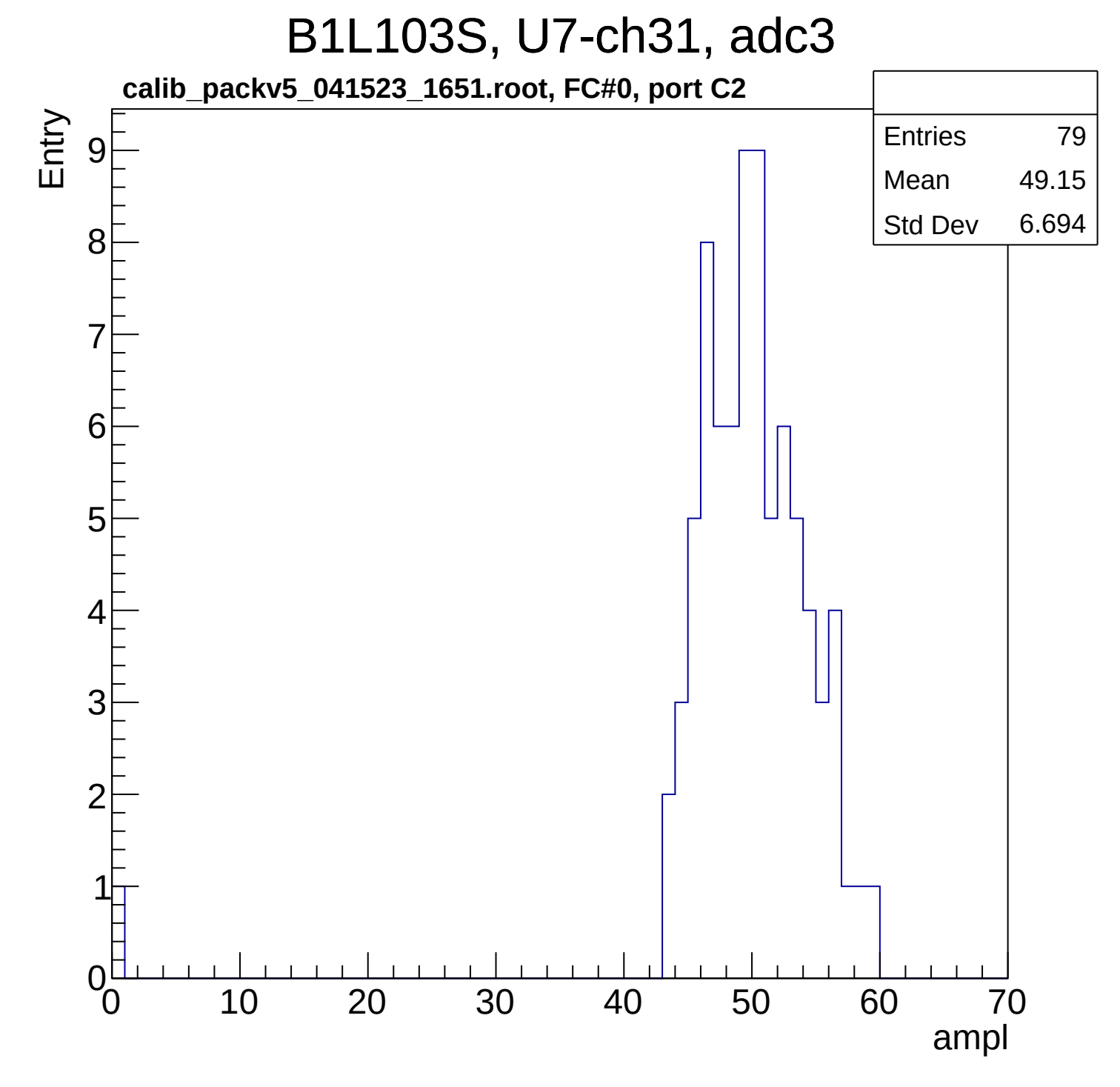
B1L103S, U7-ch31, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 49.15
Std Dev 6.694
Entry
ampl
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2
3
4
5
6
7
8
9
0
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60
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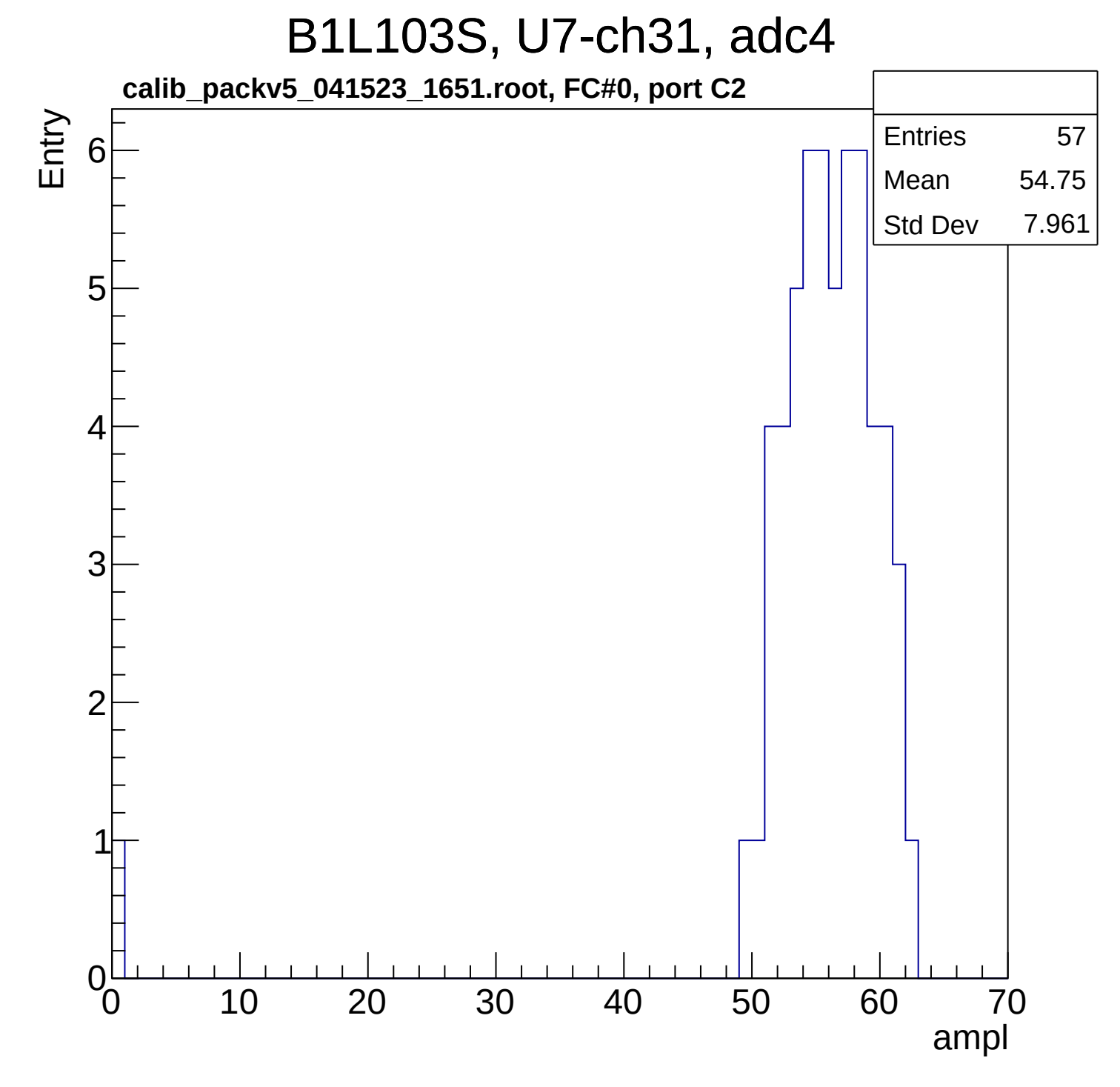
B1L103S, U7-ch31, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 54.75
Std Dev 7.961
Entry
ampl
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4
5
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60
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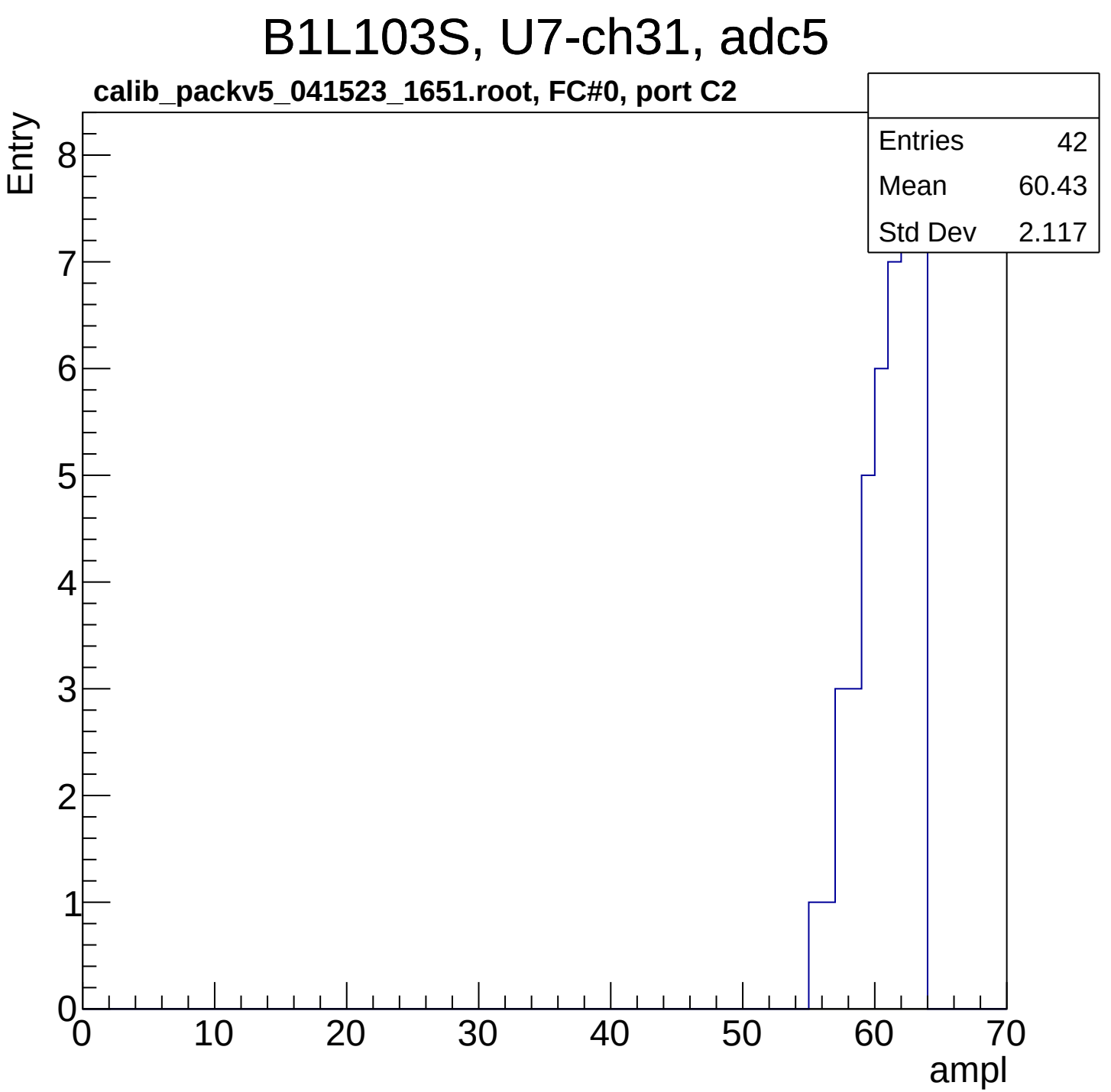
B1L103S, U7-ch31, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 42
Mean 60.43
Std Dev 2.117
Entry
ampl
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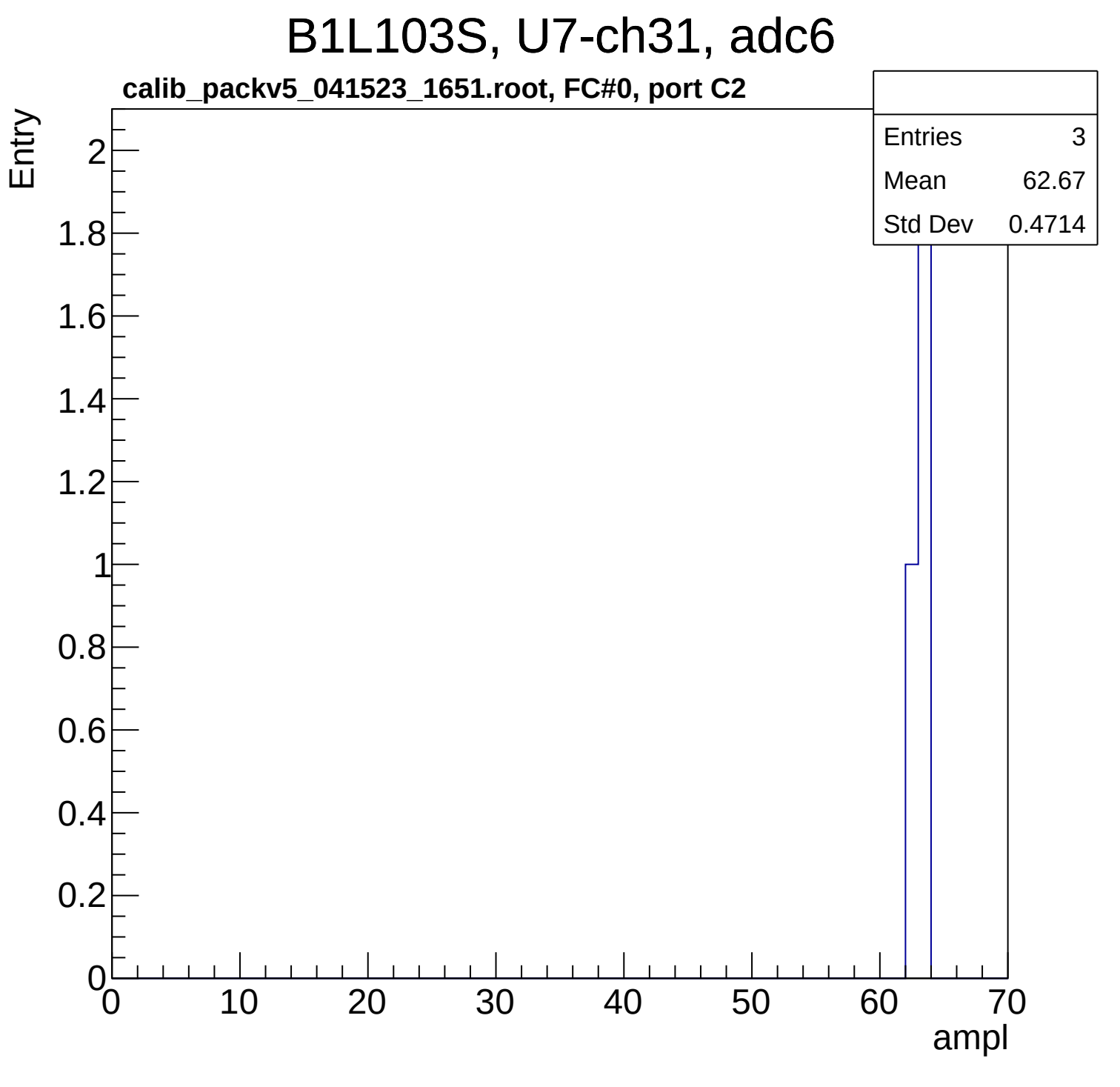
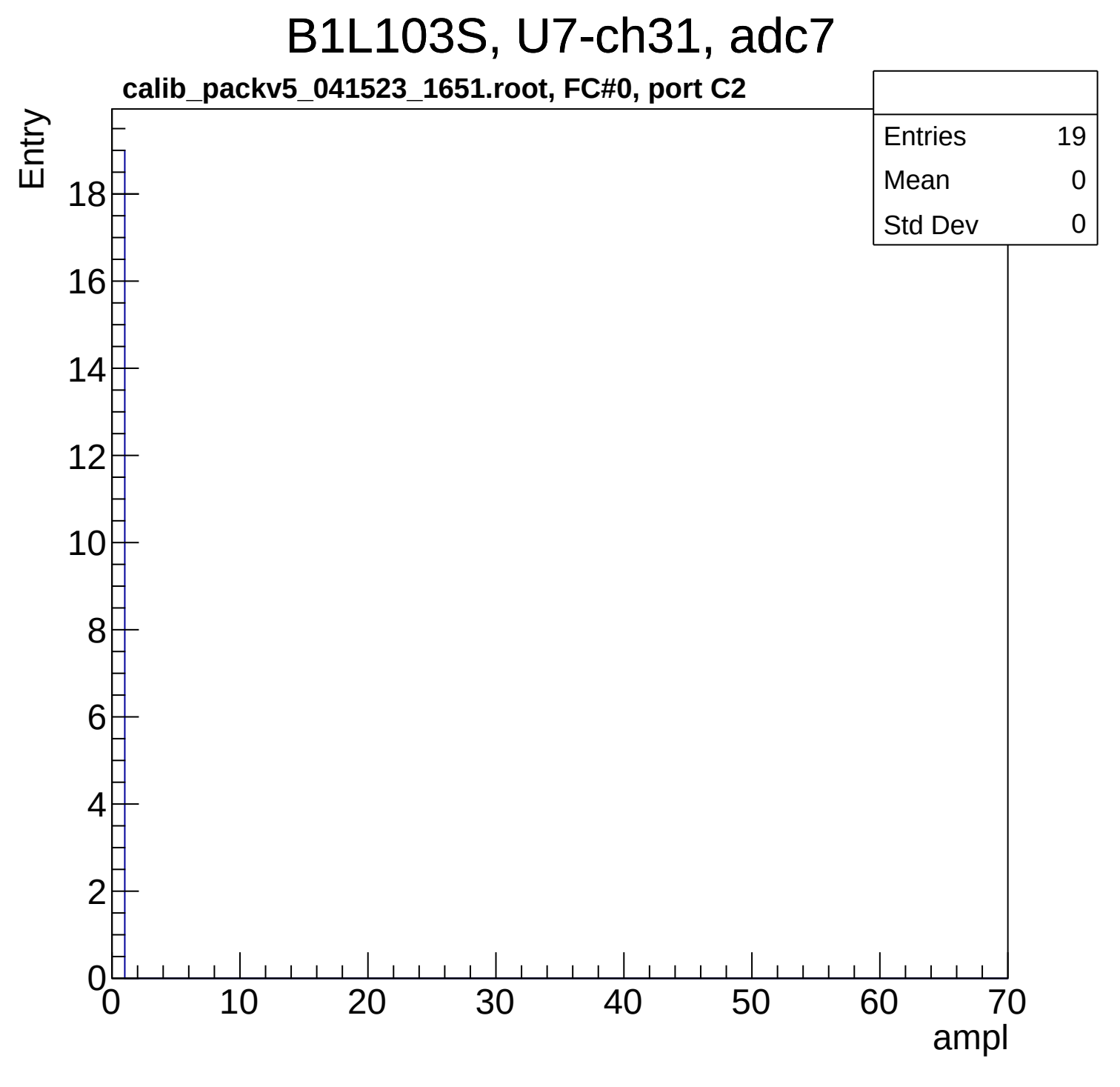
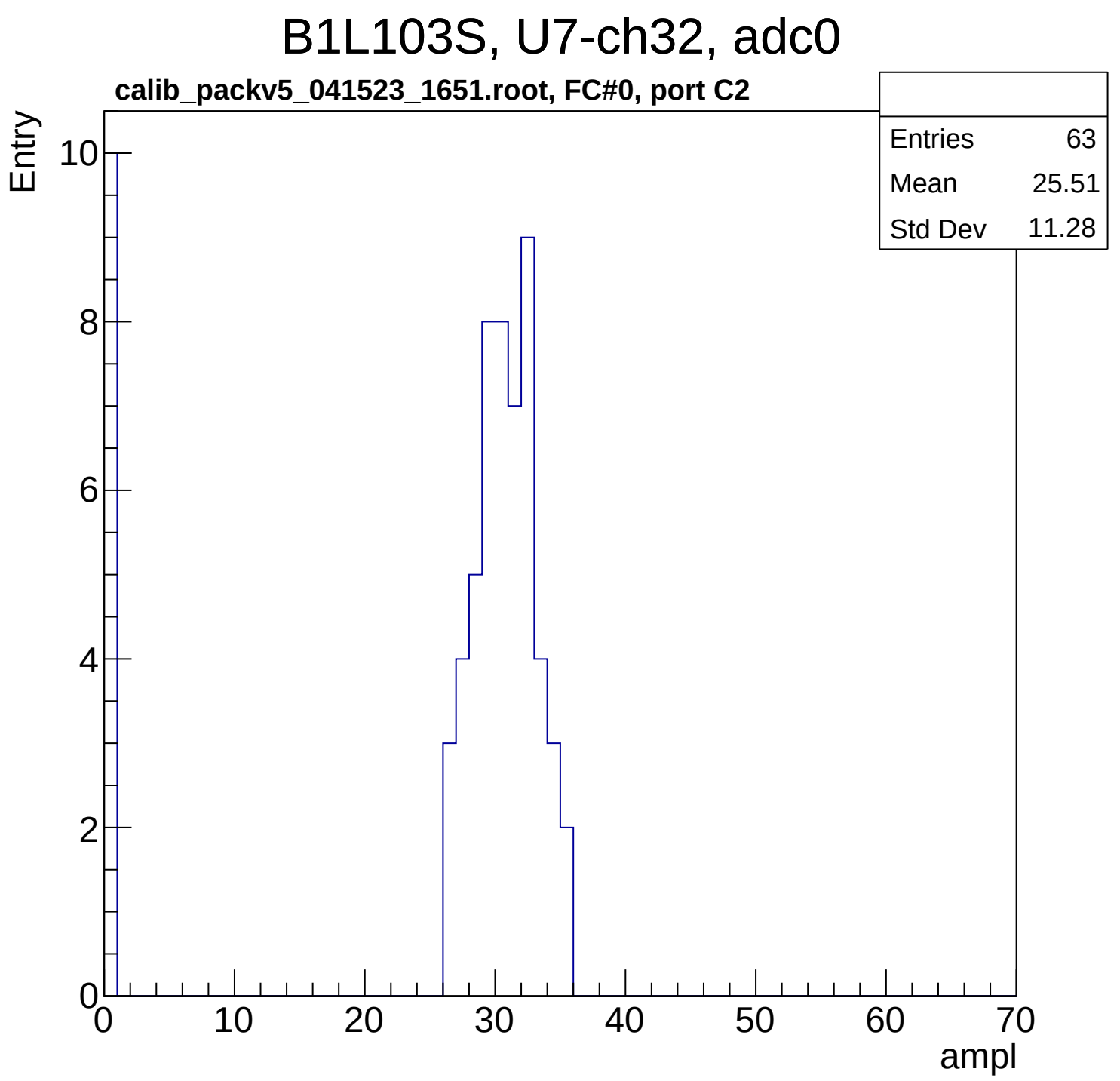
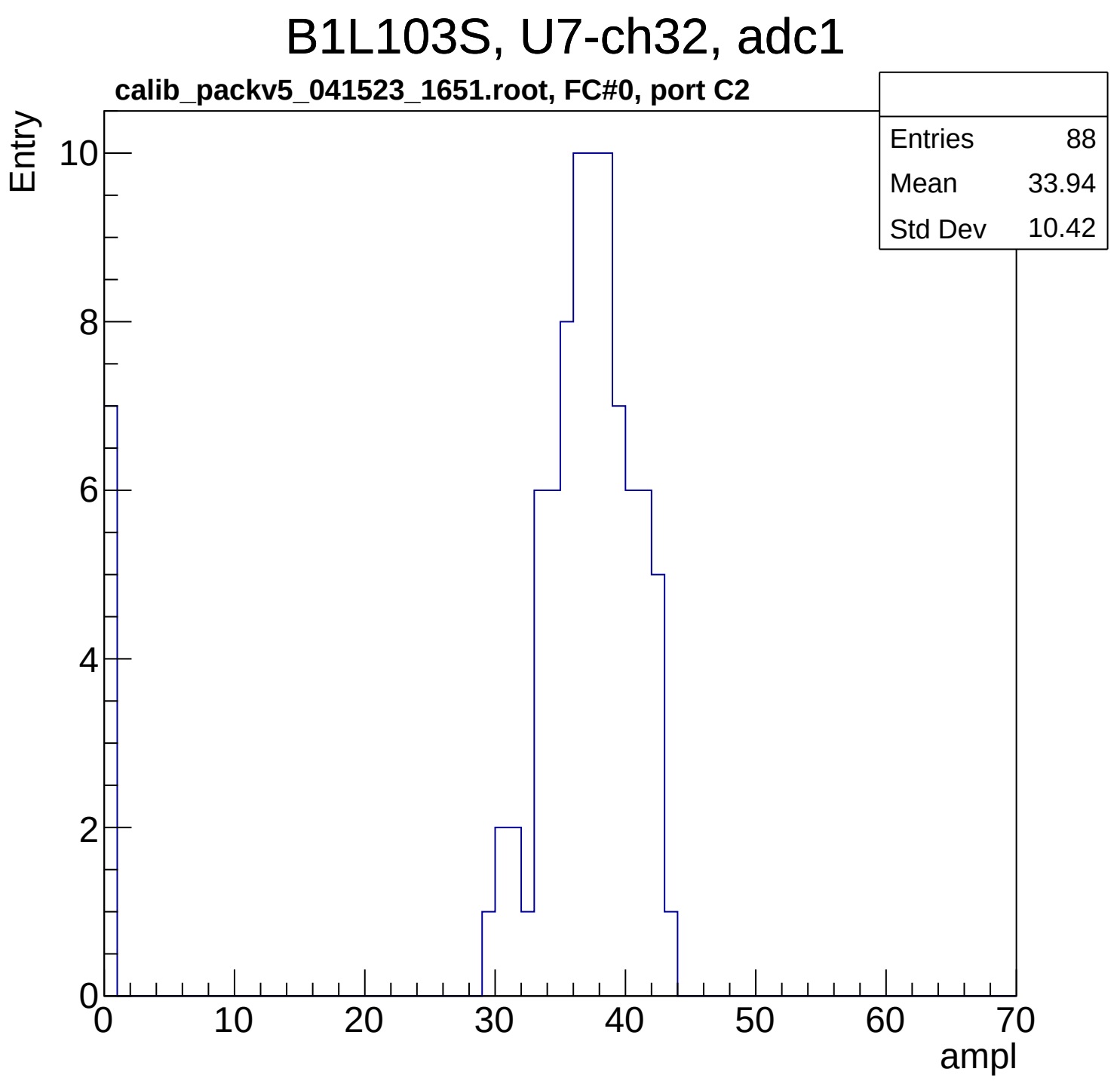
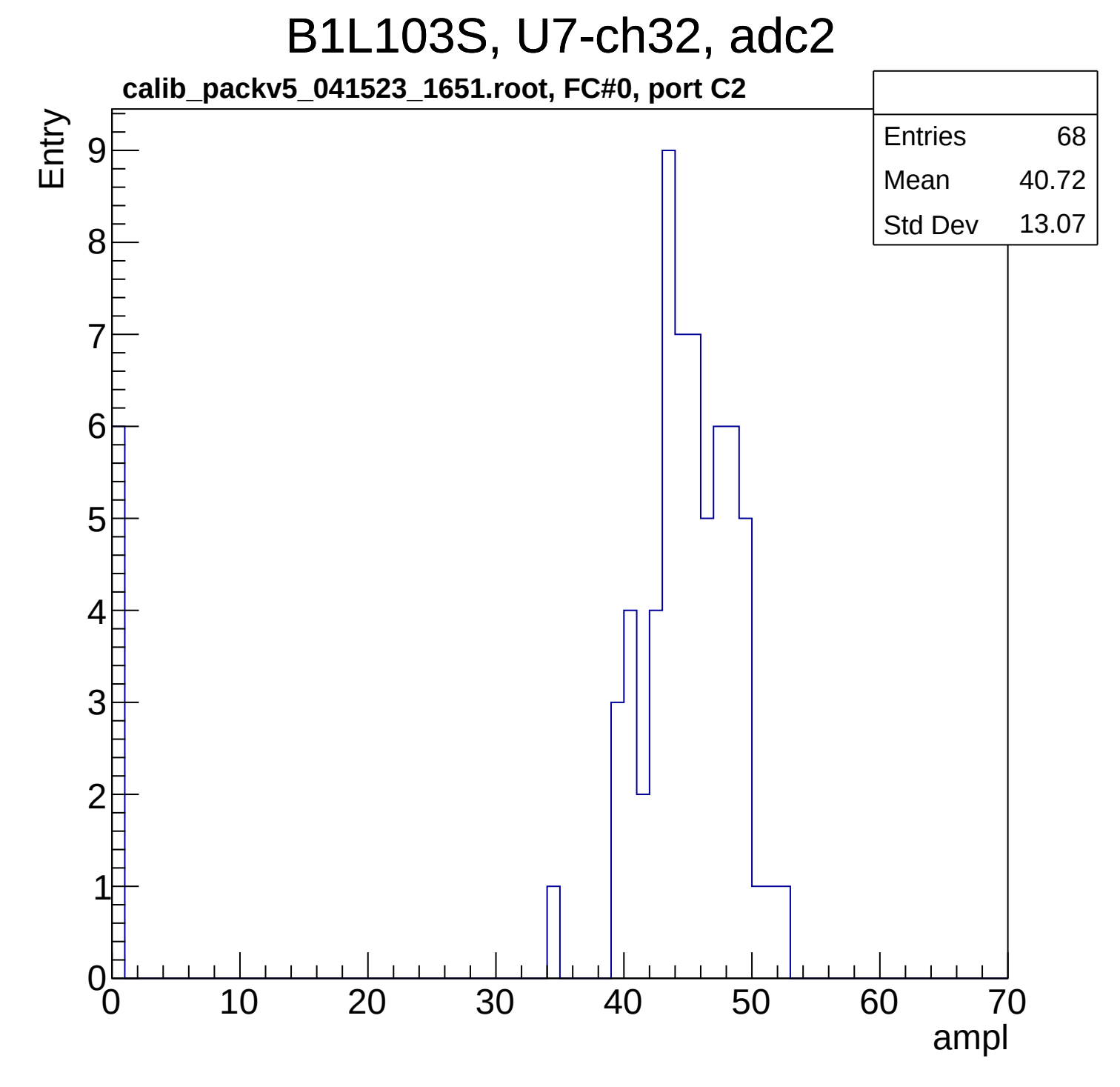
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

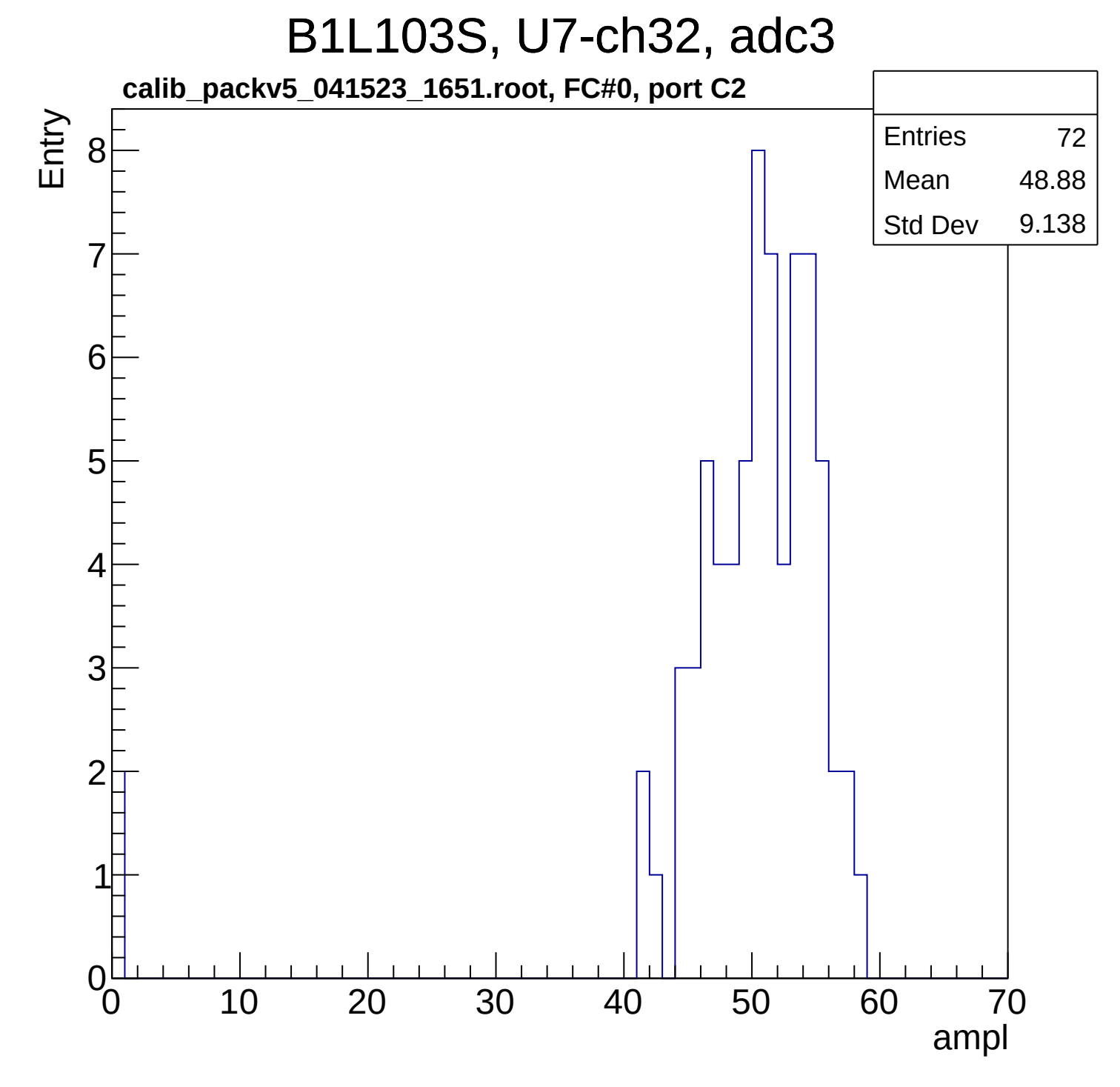

B1L103S, U7-ch31, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 3
Mean 62.67
Std Dev 0.4714
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

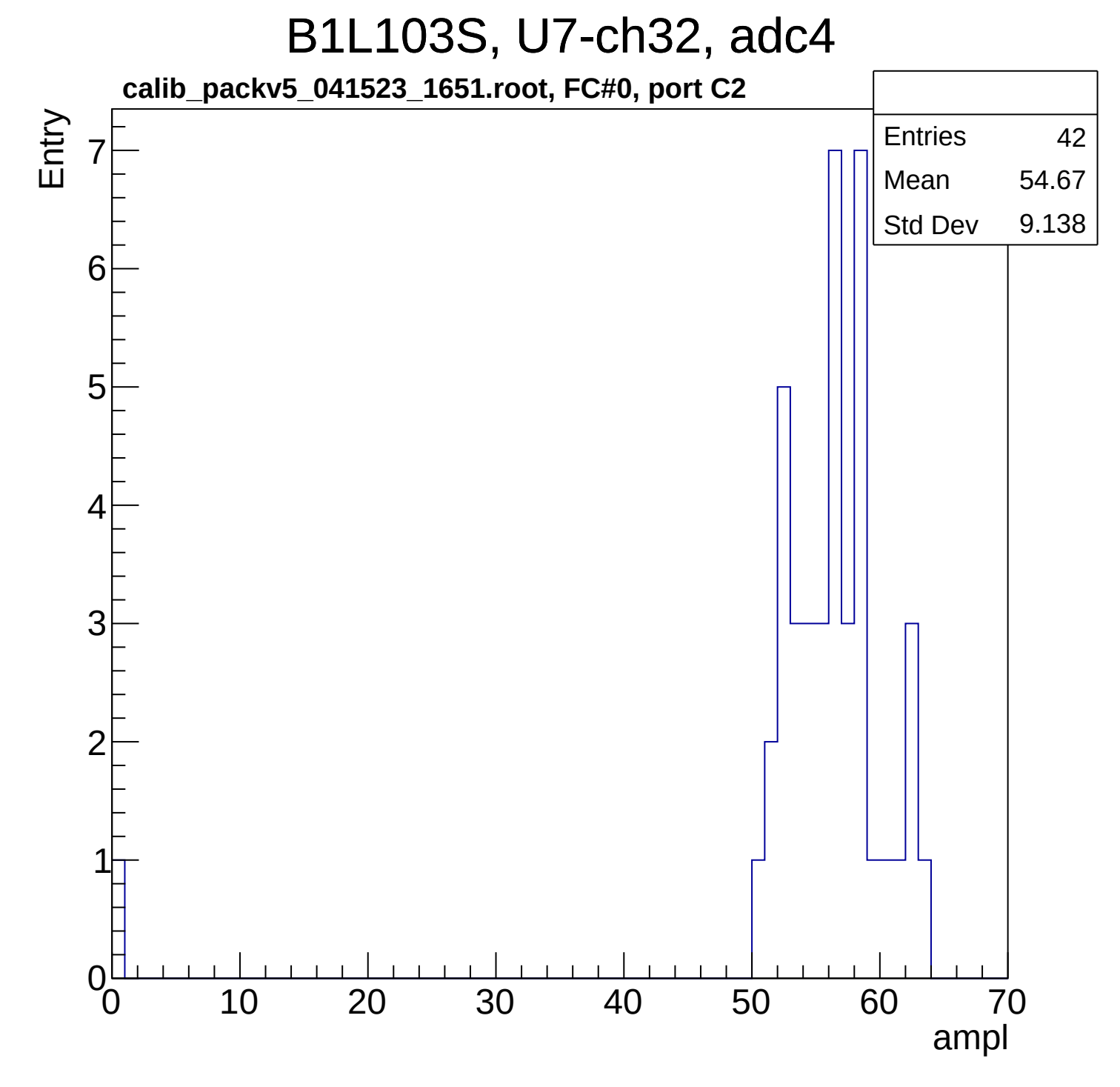

B1L103S, U7-ch31, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

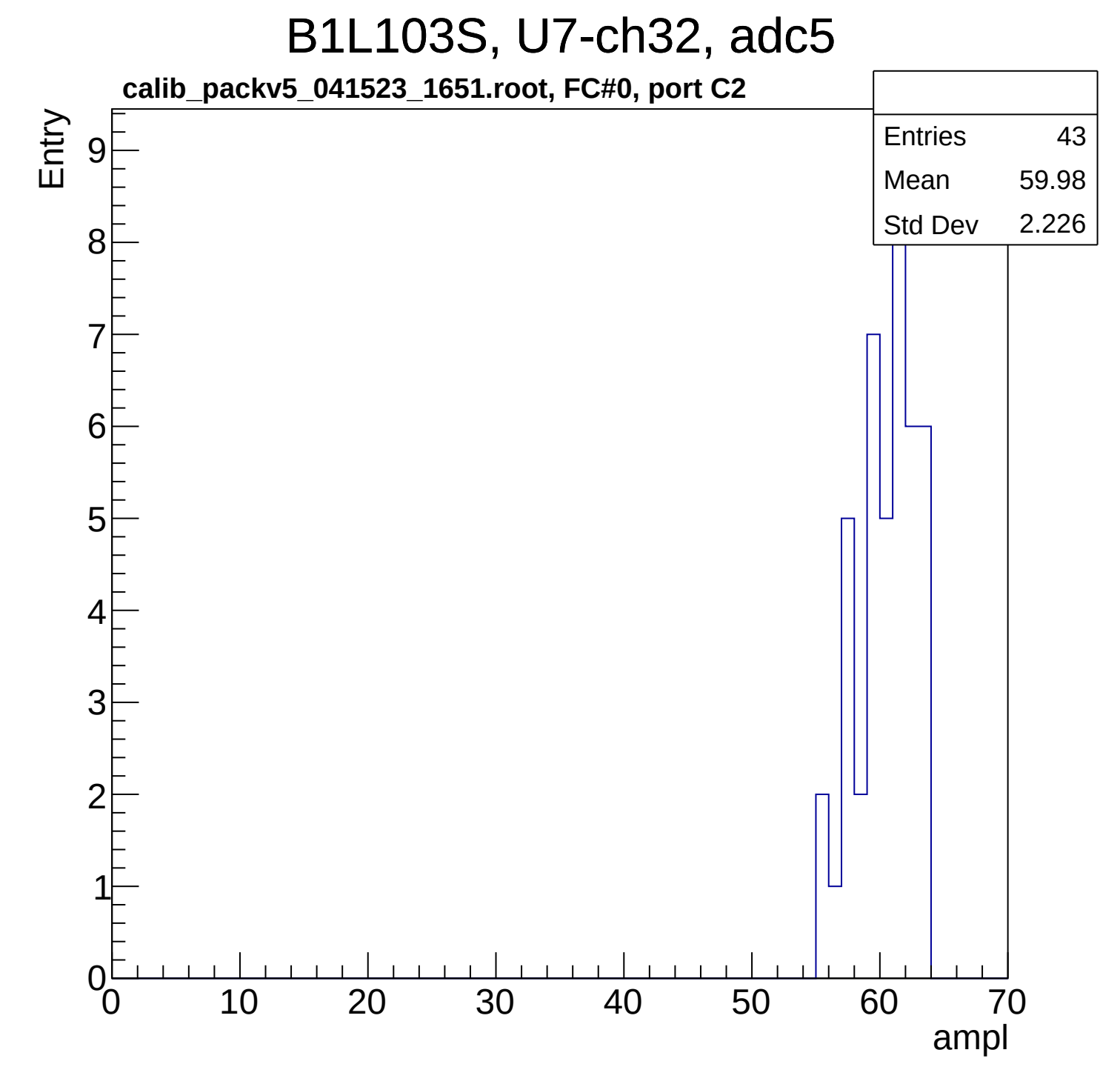

B1L103S, U7-ch32, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 25.51
Std Dev 11.28
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

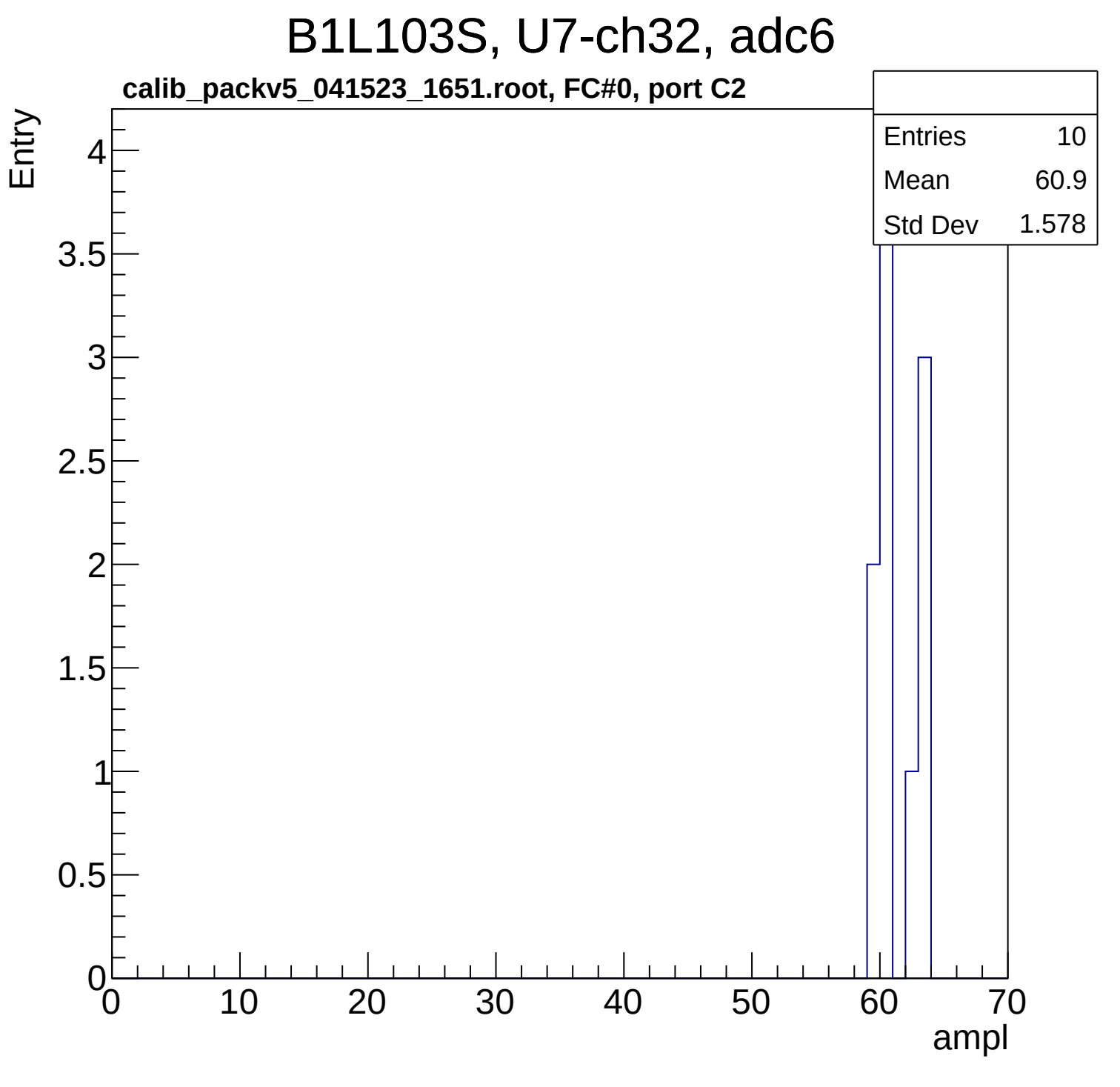

B1L103S, U7-ch32, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 88
Mean 33.94
Std Dev 10.42
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

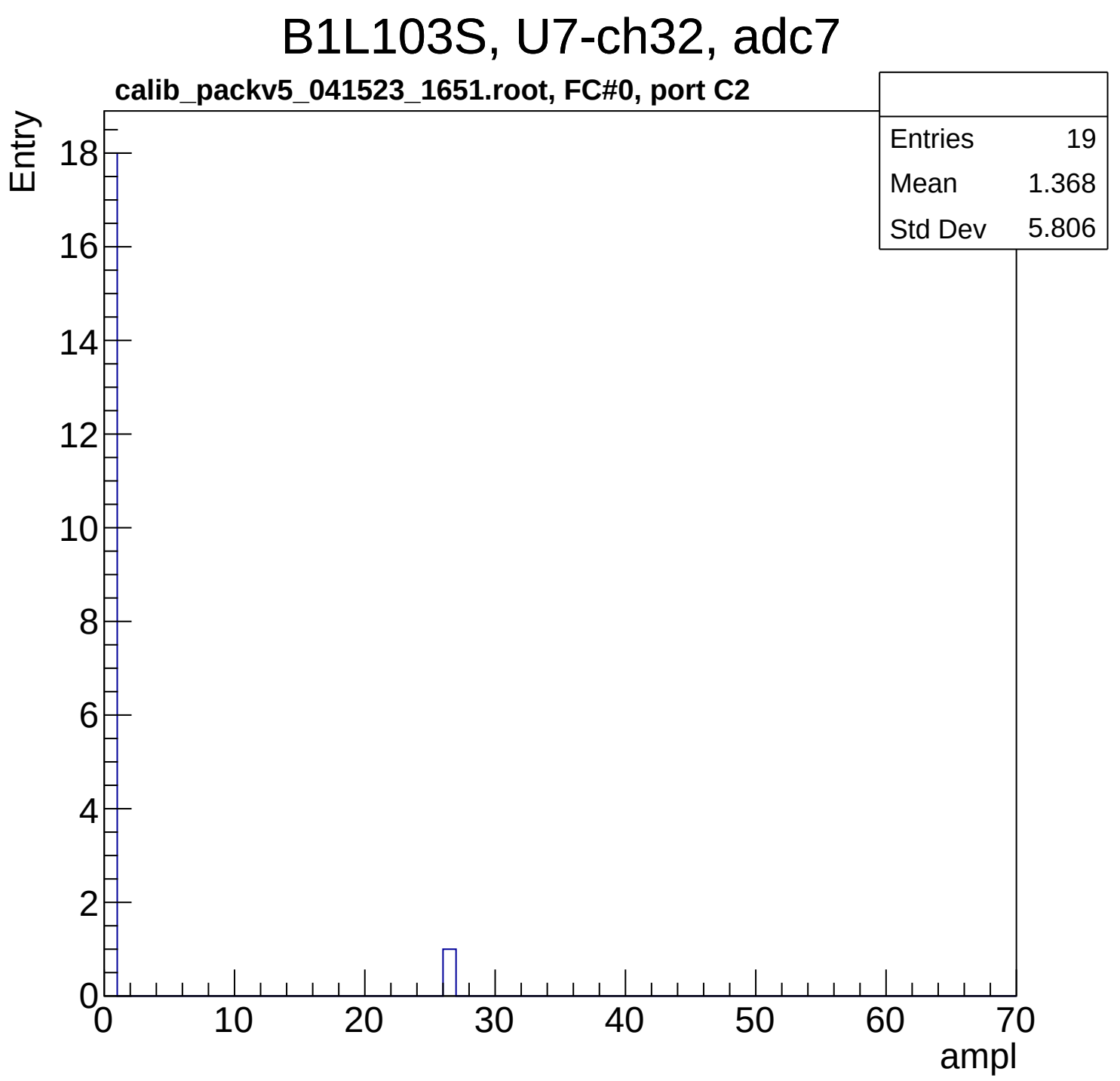

B1L103S, U7-ch32, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 40.72
Std Dev 13.07
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

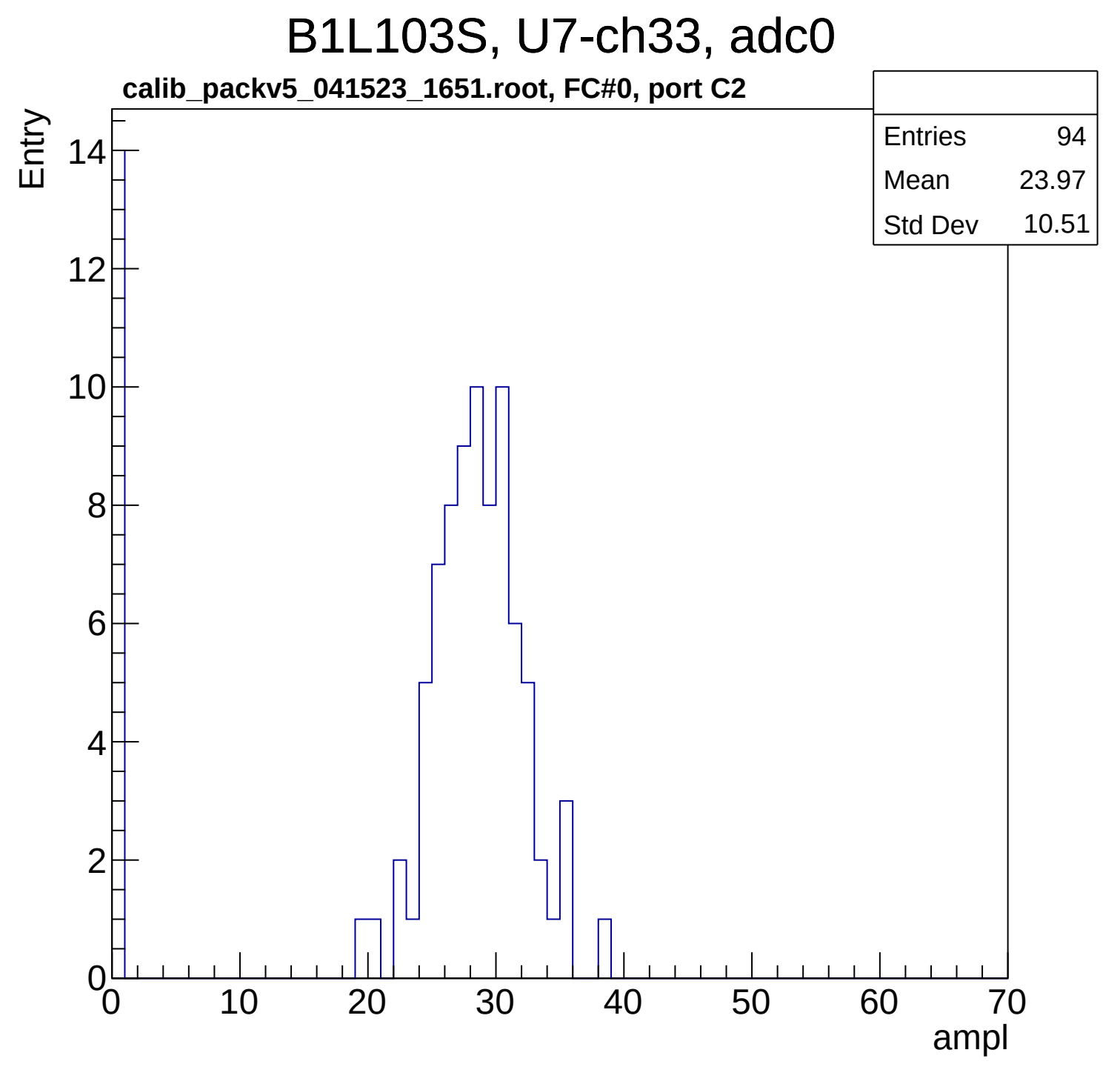

B1L103S, U7-ch32, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 48.88
Std Dev 9.138
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

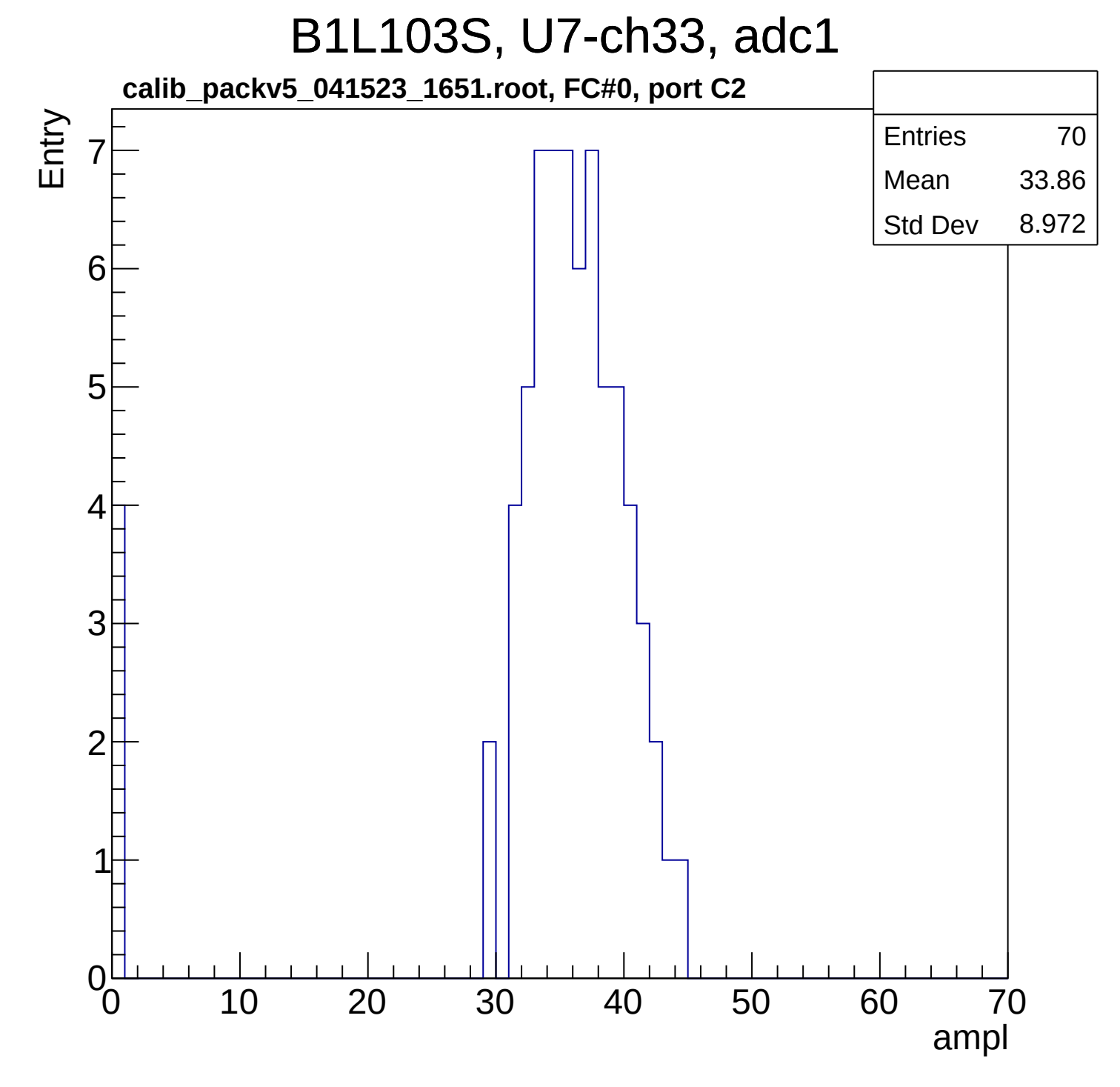

B1L103S, U7-ch32, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 42
Mean 54.67
Std Dev 9.138
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

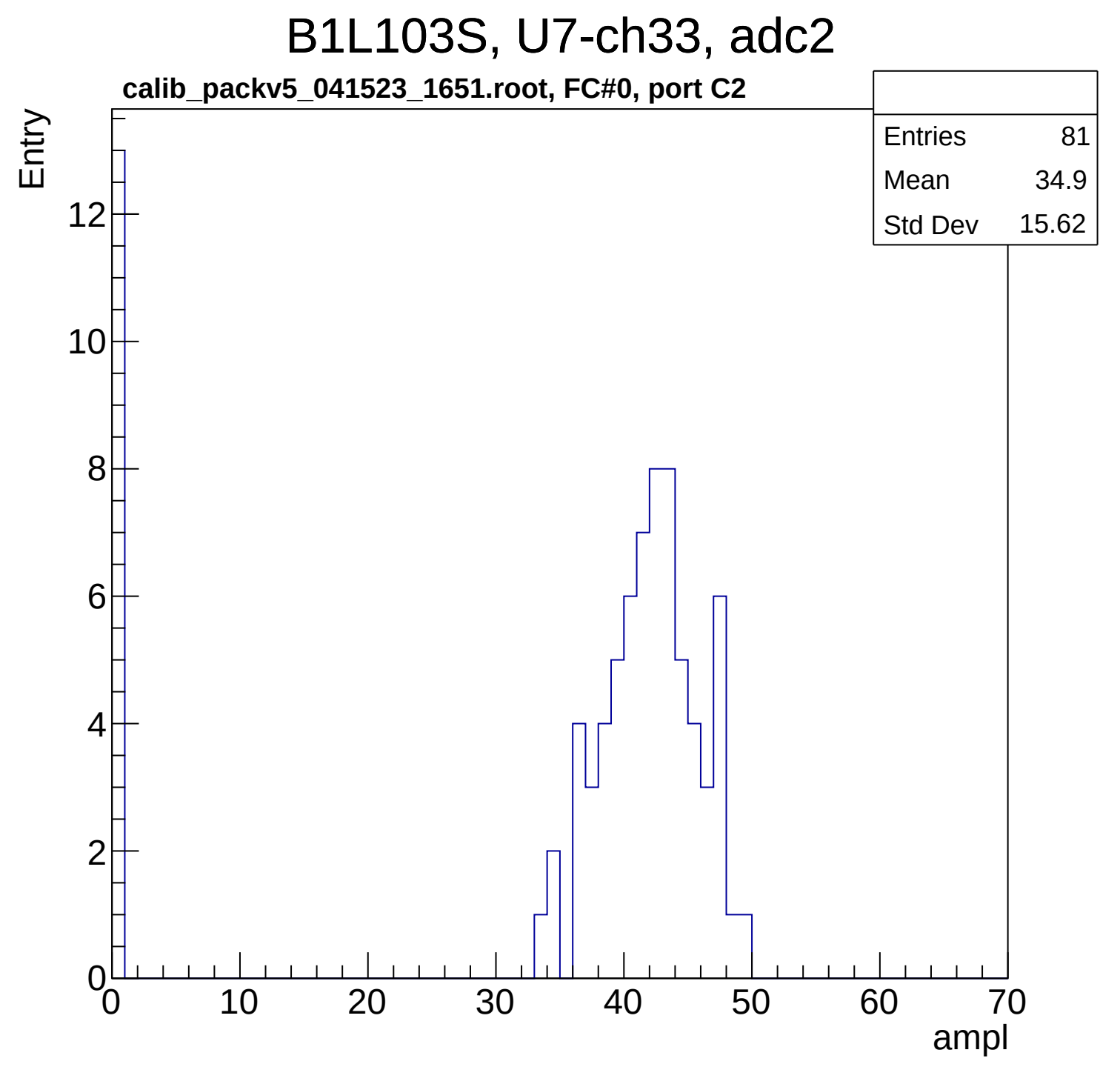

B1L103S, U7-ch32, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 43
Mean 59.98
Std Dev 2.226
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

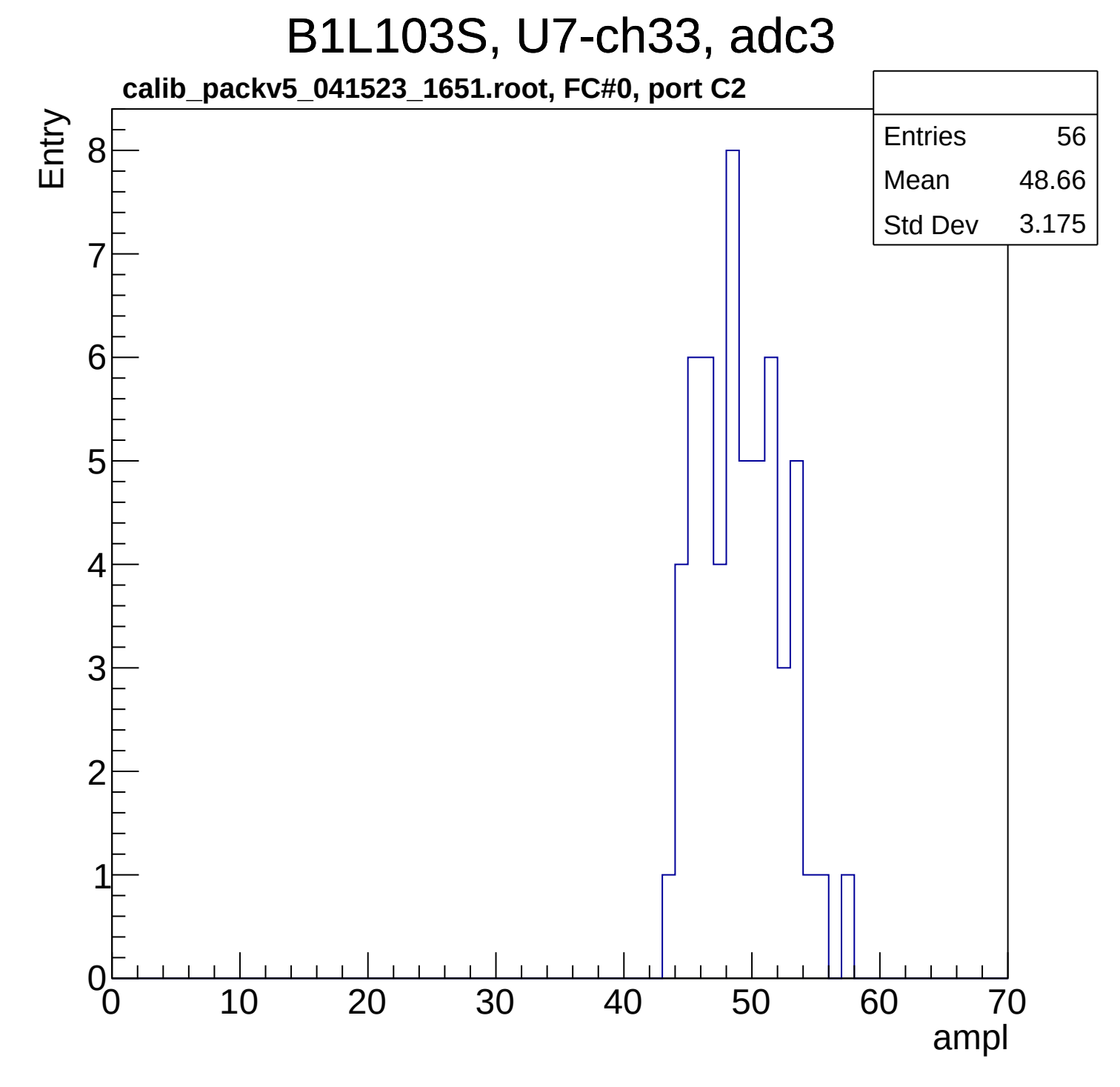

B1L103S, U7-ch32, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 60.9
Std Dev 1.578
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U7-ch32, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.368
Std Dev 5.806
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch33, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 94
Mean 23.97
Std Dev 10.51
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch33, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 33.86
Std Dev 8.972
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U7-ch33, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 34.9
Std Dev 15.62
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch33, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 48.66
Std Dev 3.175
Entry
ampl
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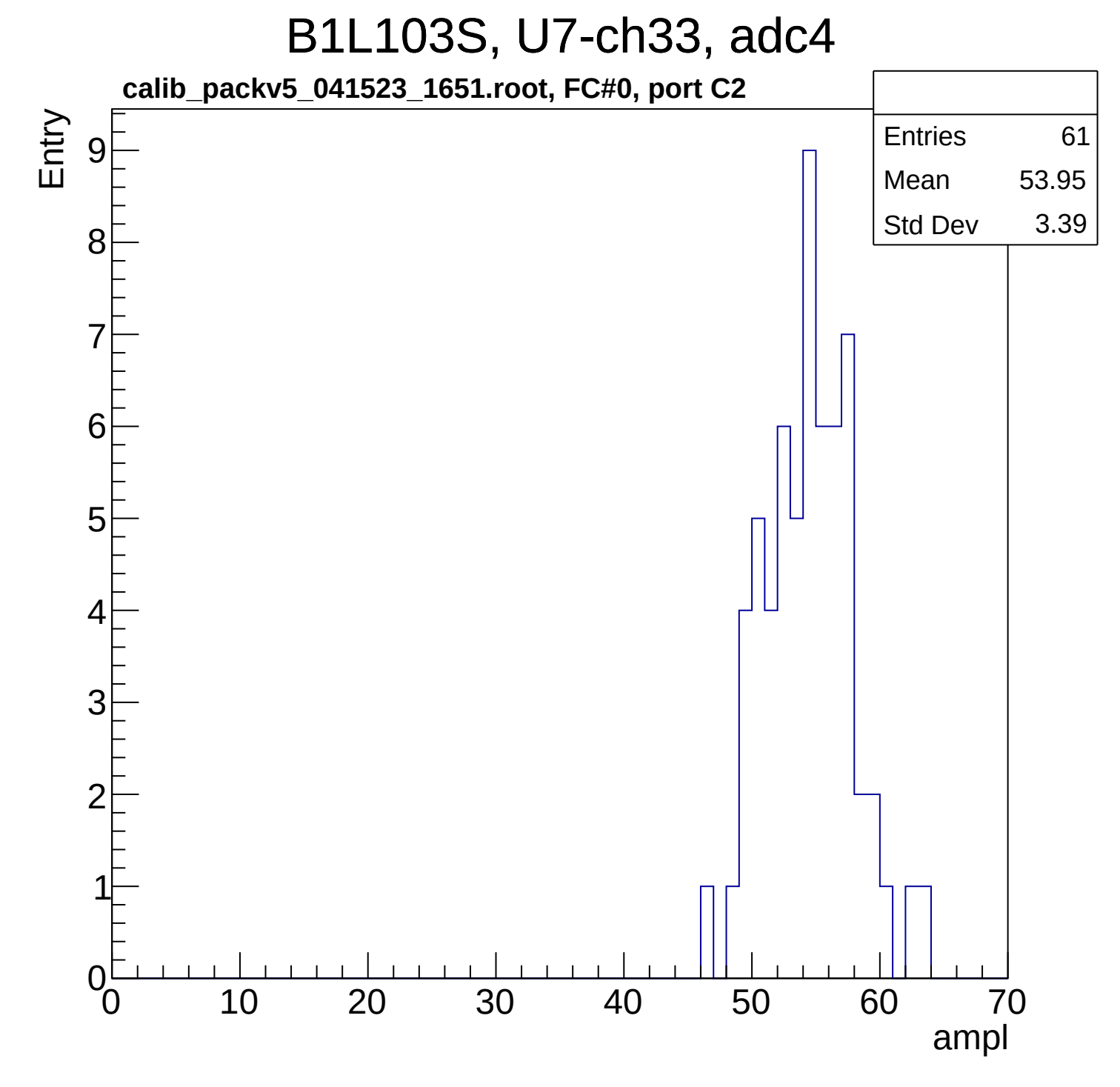
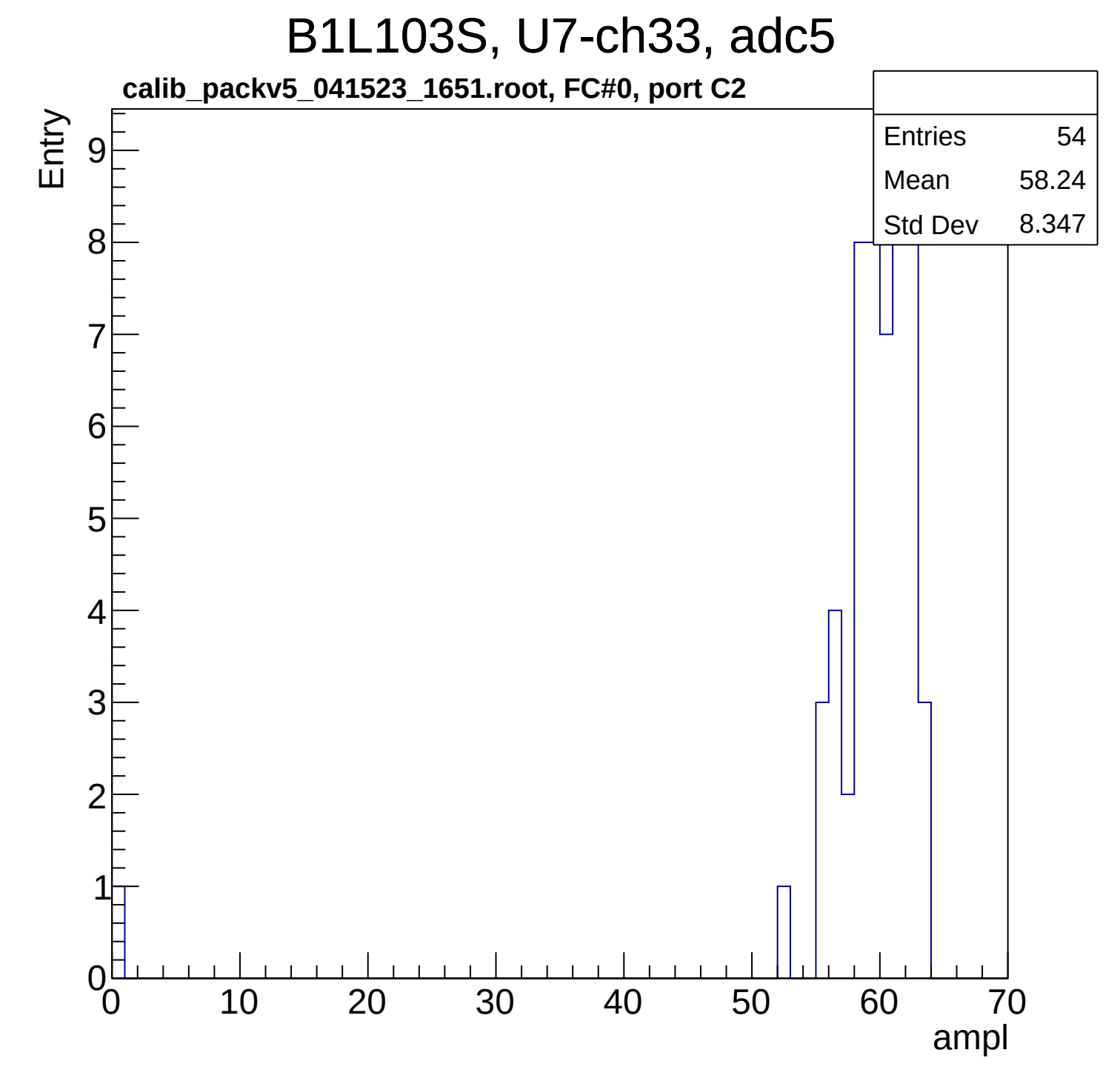
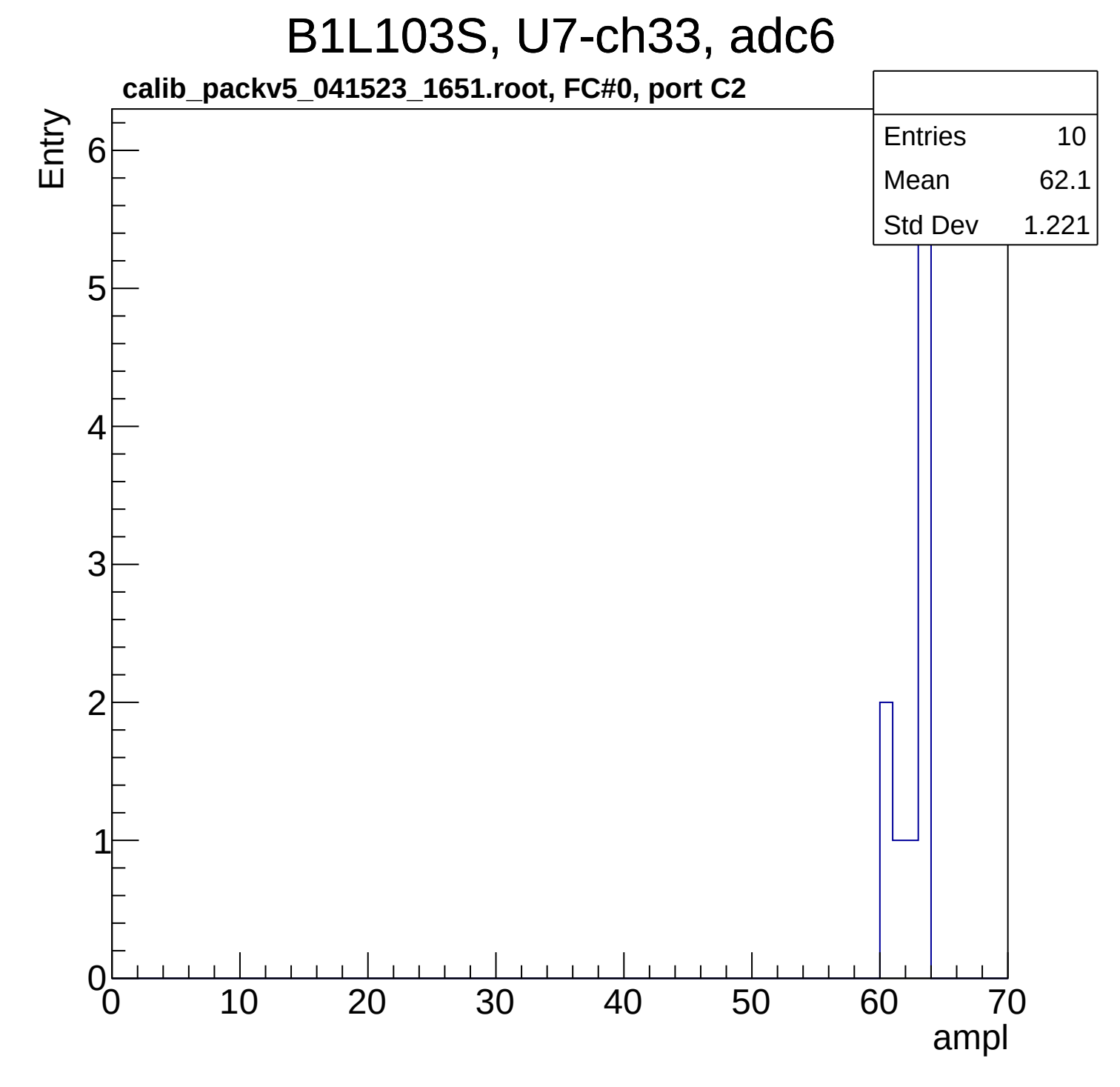
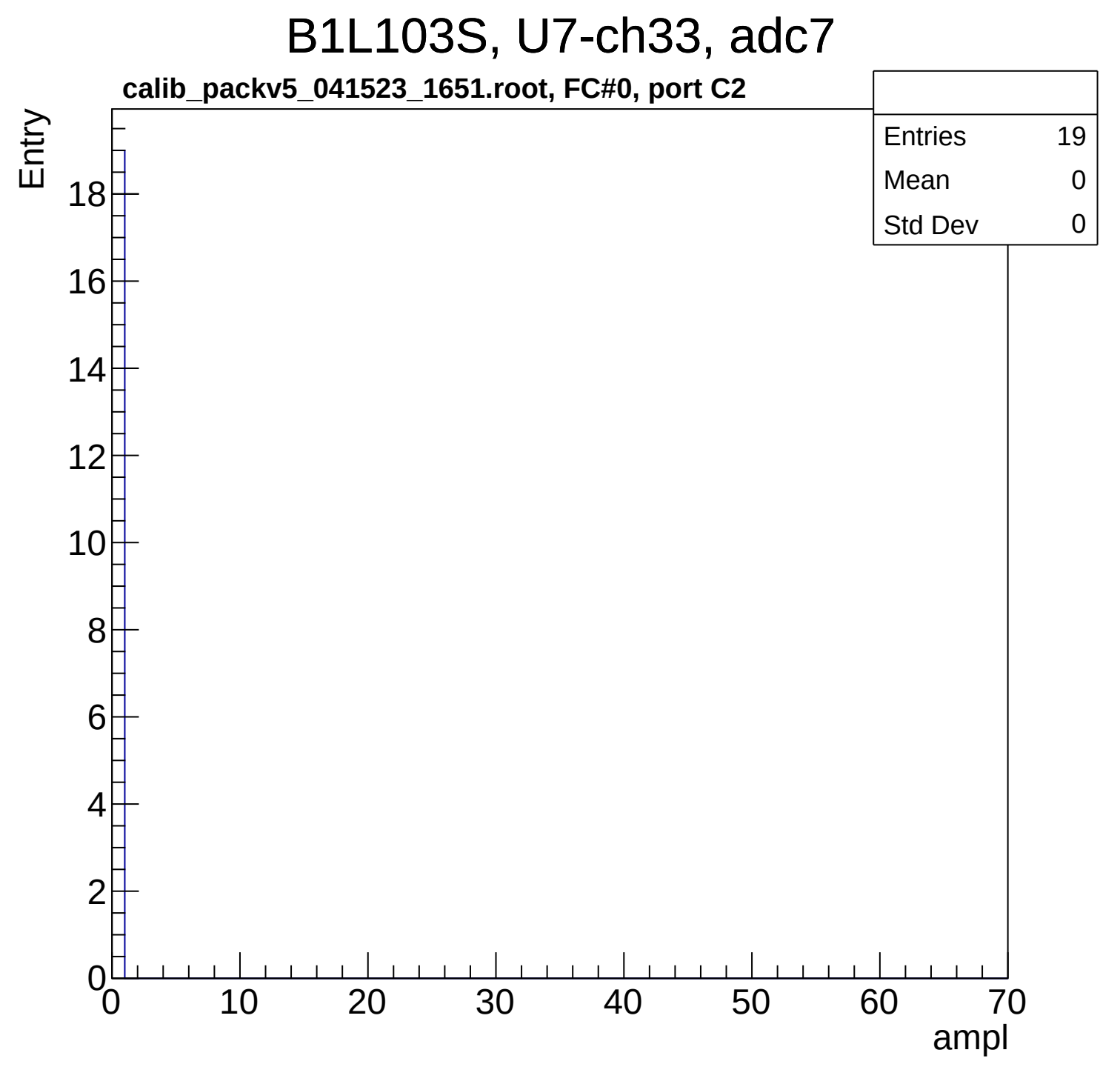
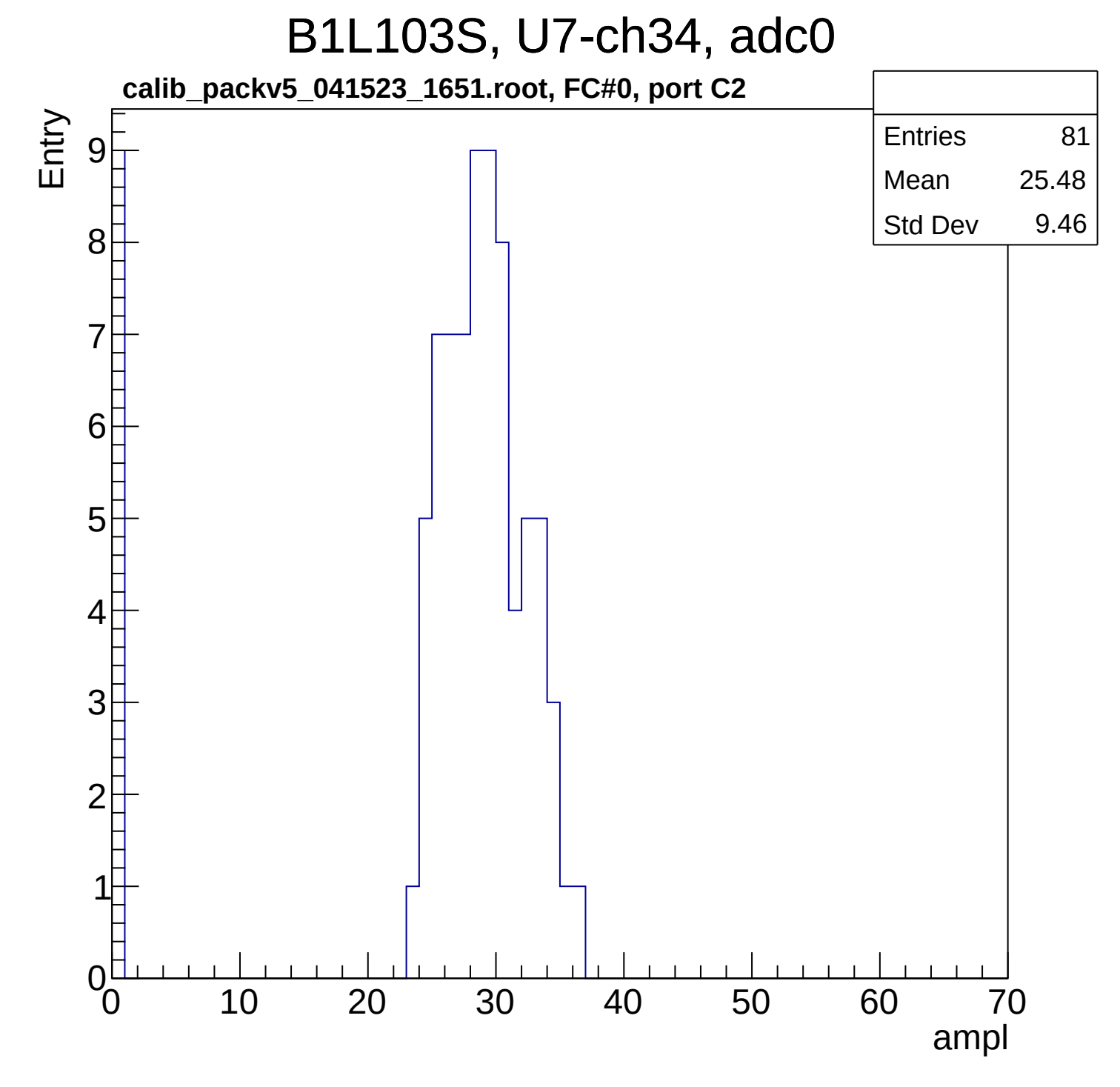
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

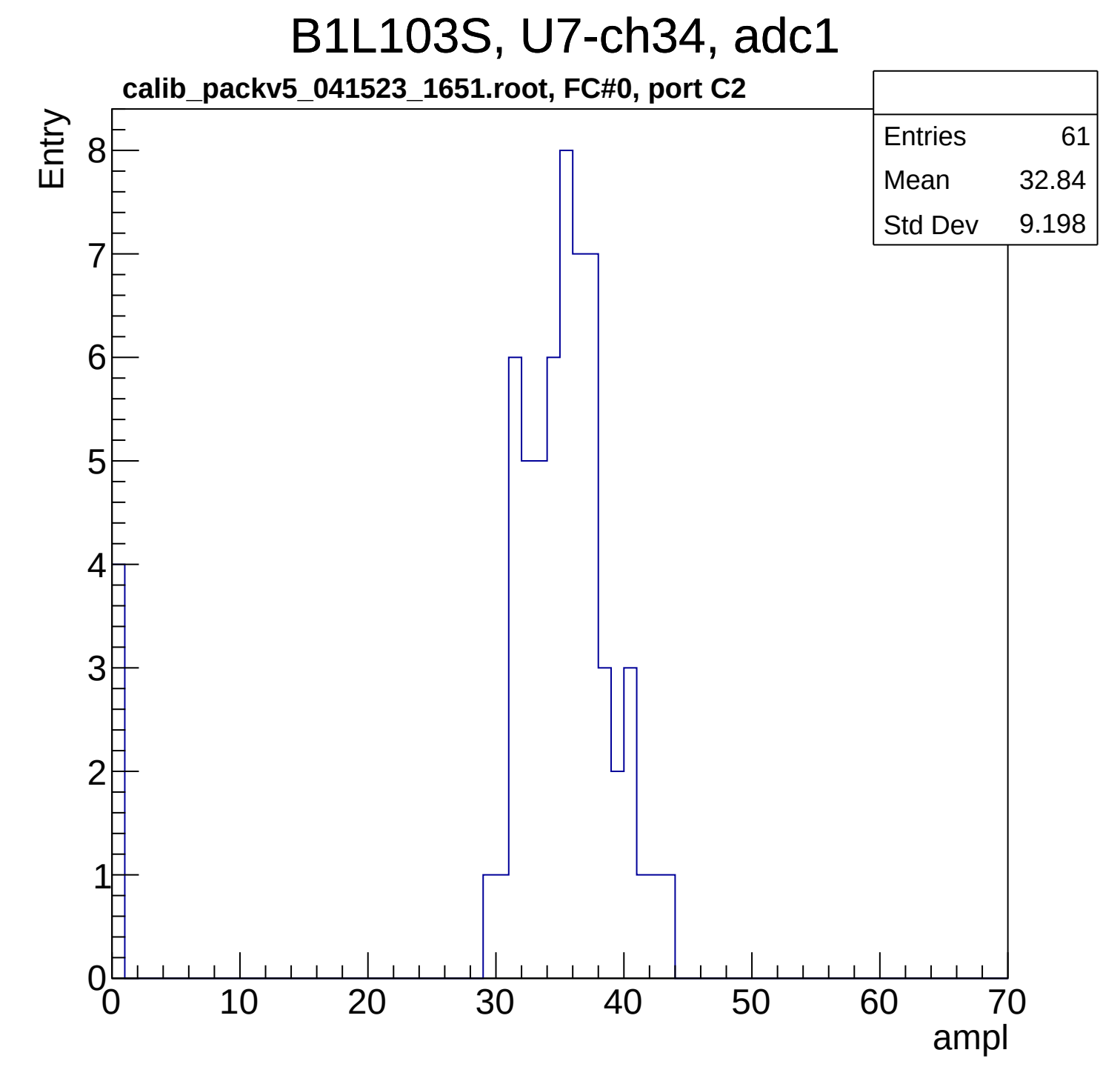

B1L103S, U7-ch33, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 53.95
Std Dev 3.39
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U7-ch33, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 58.24
Std Dev 8.347
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U7-ch33, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 62.1
Std Dev 1.221
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U7-ch33, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch34, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 25.48
Std Dev 9.46
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U7-ch34, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 32.84
Std Dev 9.198
Entry
ampl
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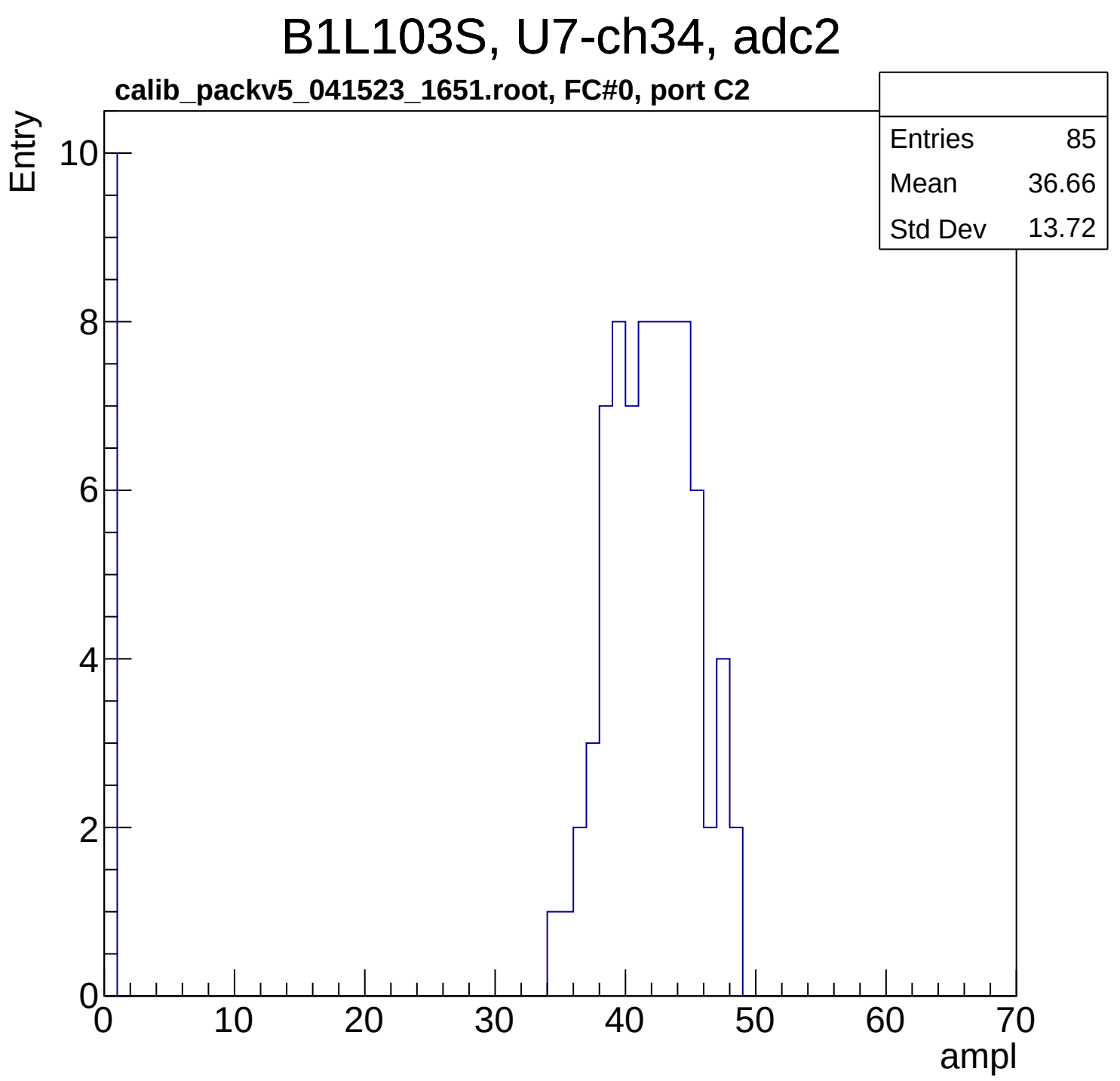
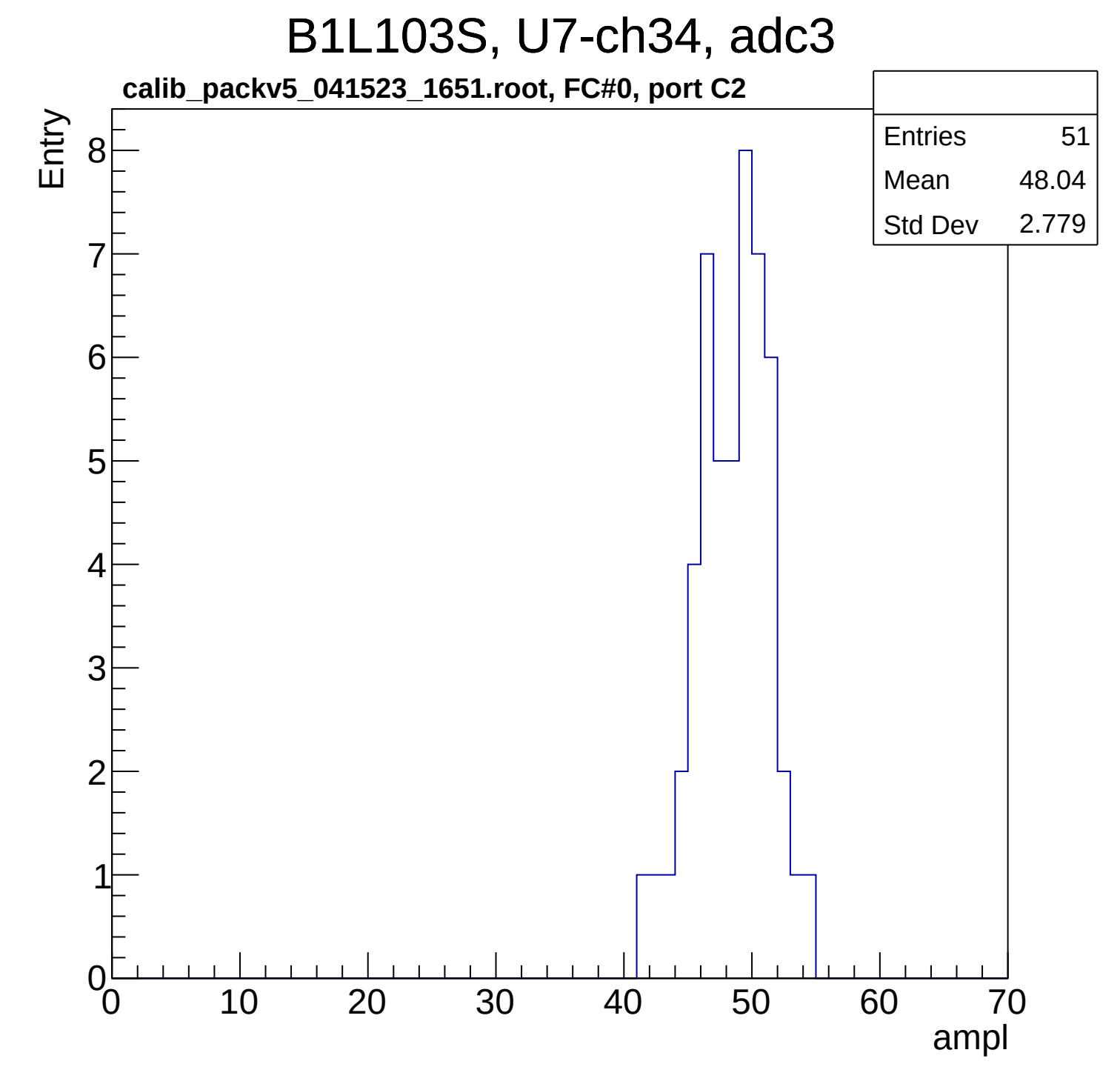
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch34, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 36.66
Std Dev 13.72
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U7-ch34, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 48.04
Std Dev 2.779
Entry
ampl
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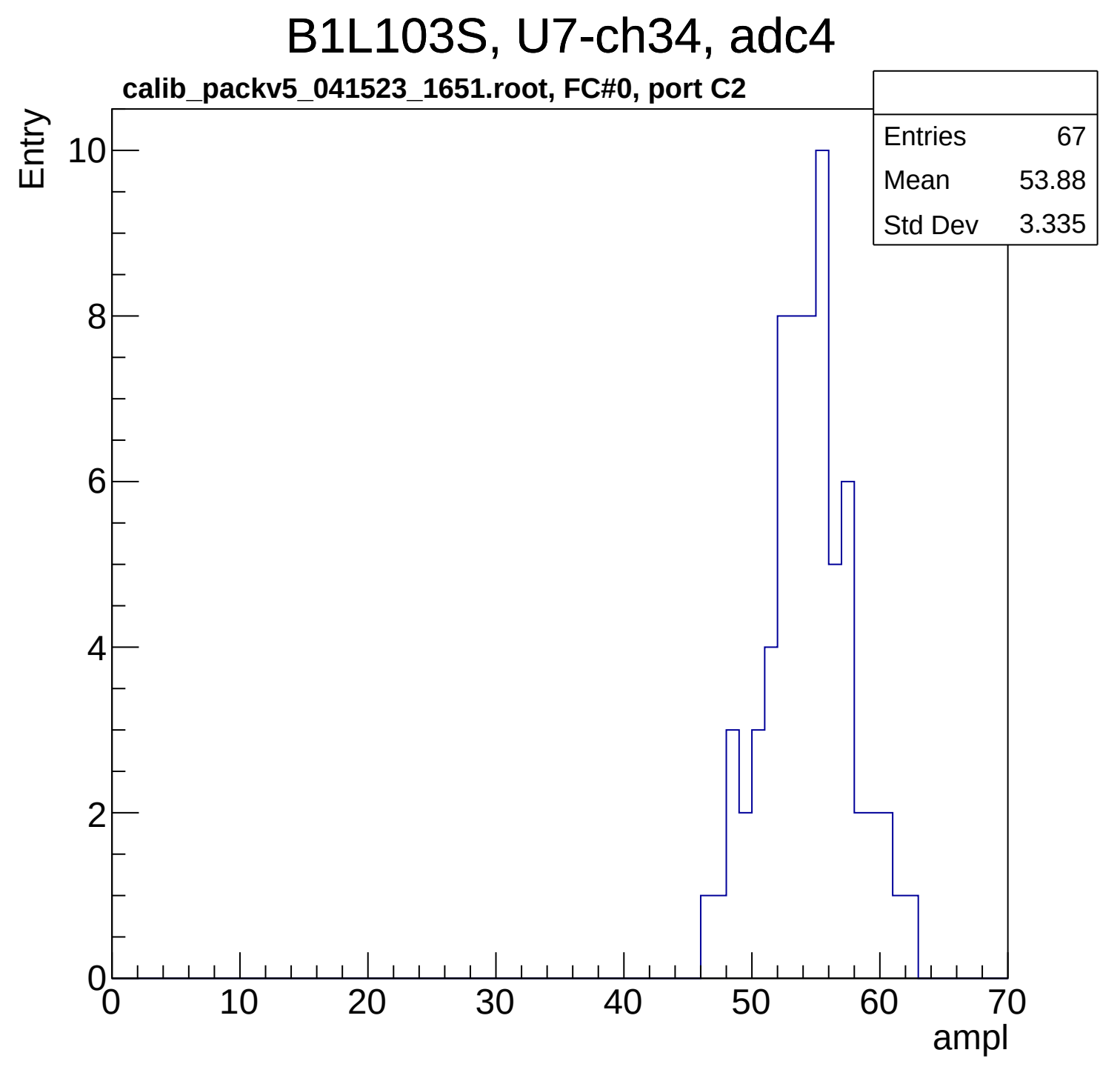
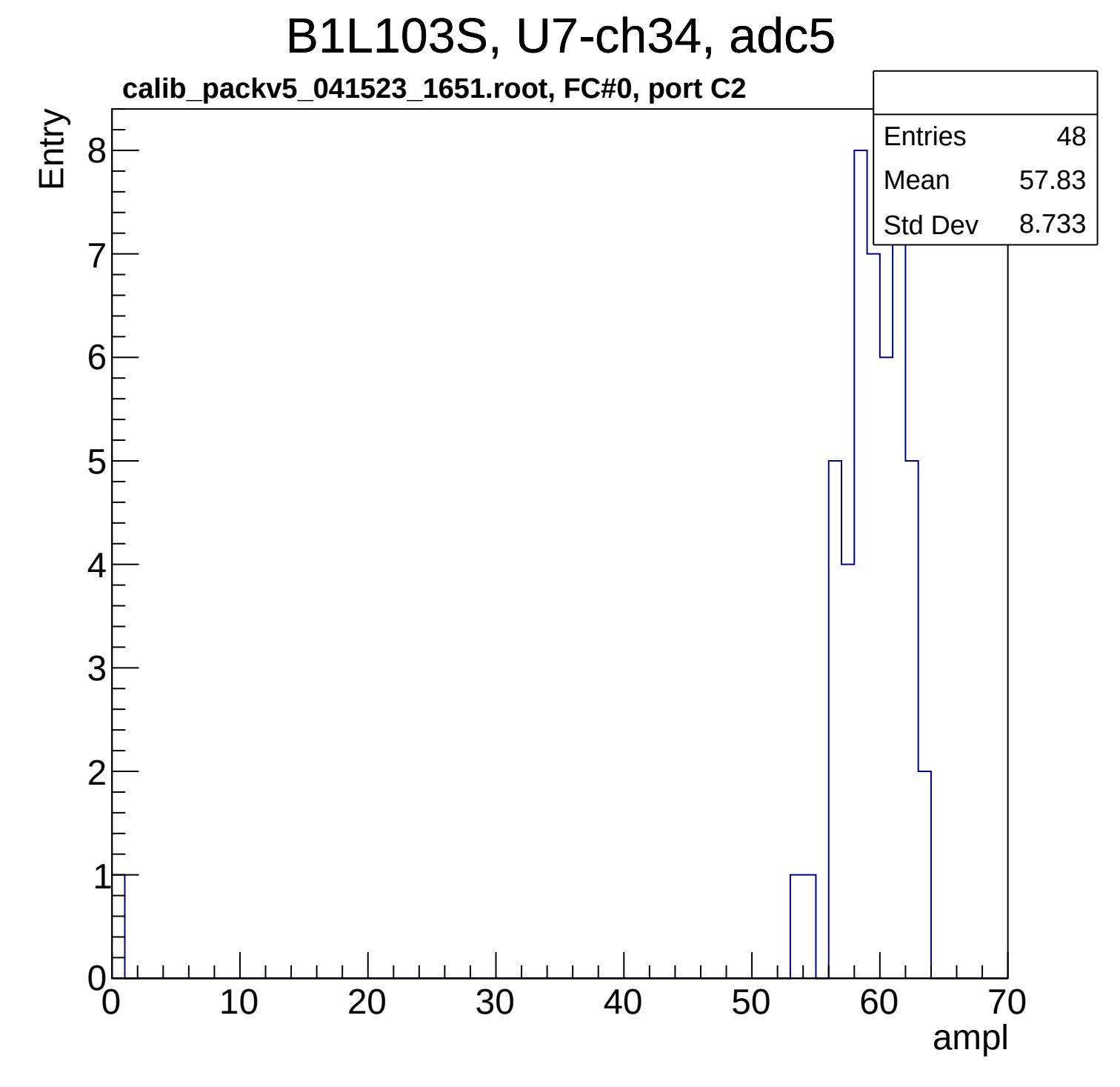
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch34, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 53.88
Std Dev 3.335
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U7-ch34, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 57.83
Std Dev 8.733
Entry
ampl
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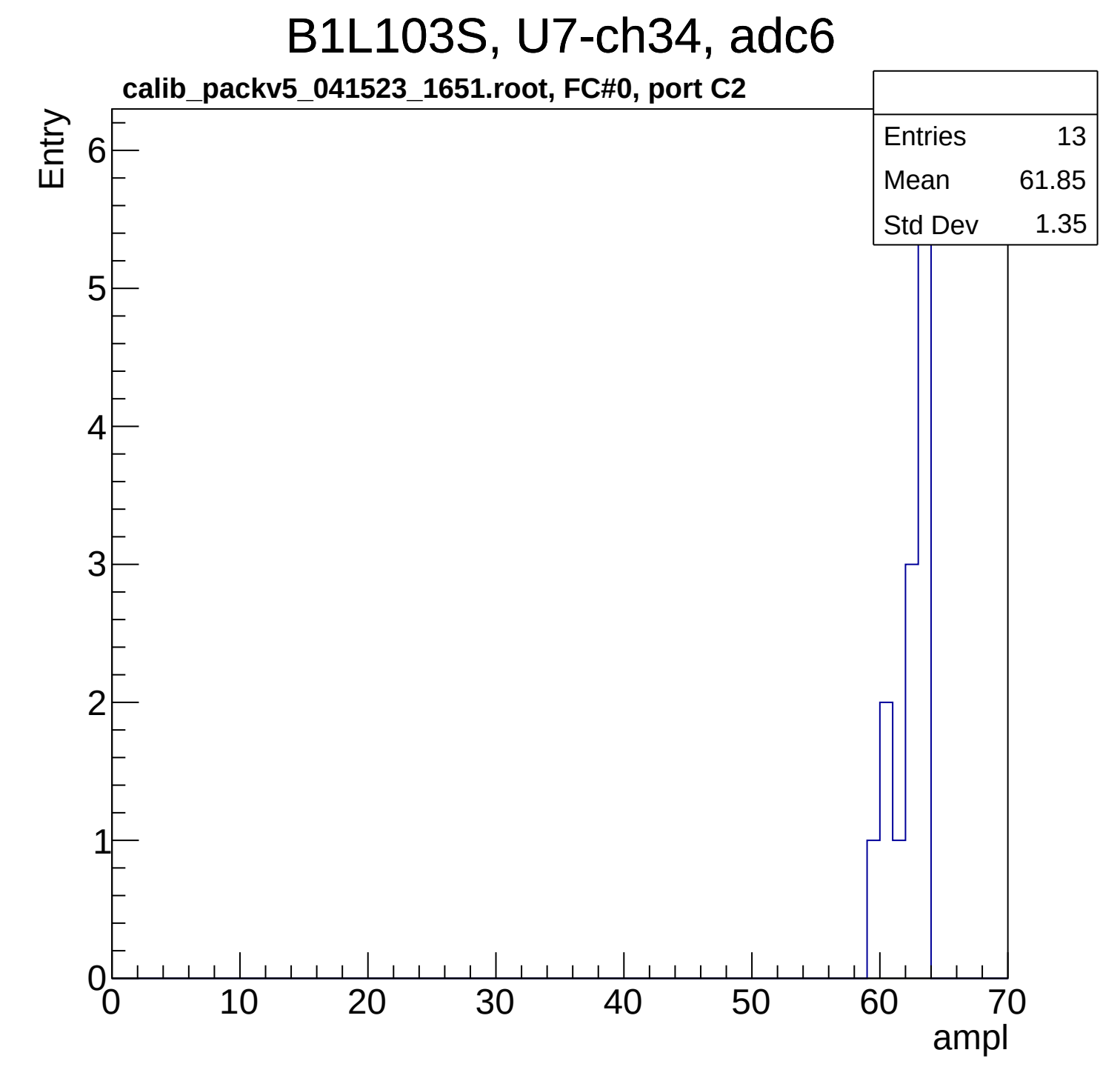
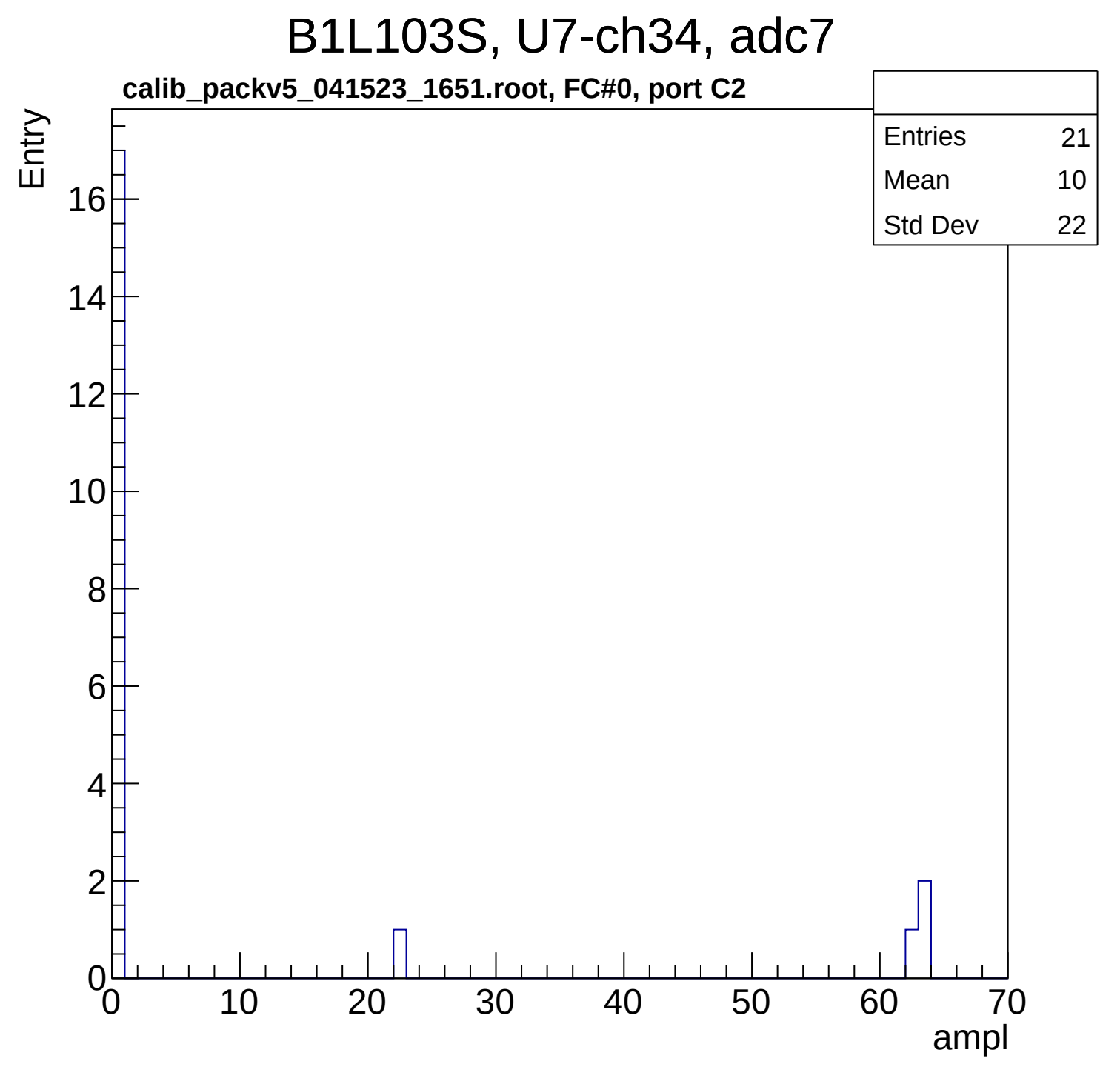
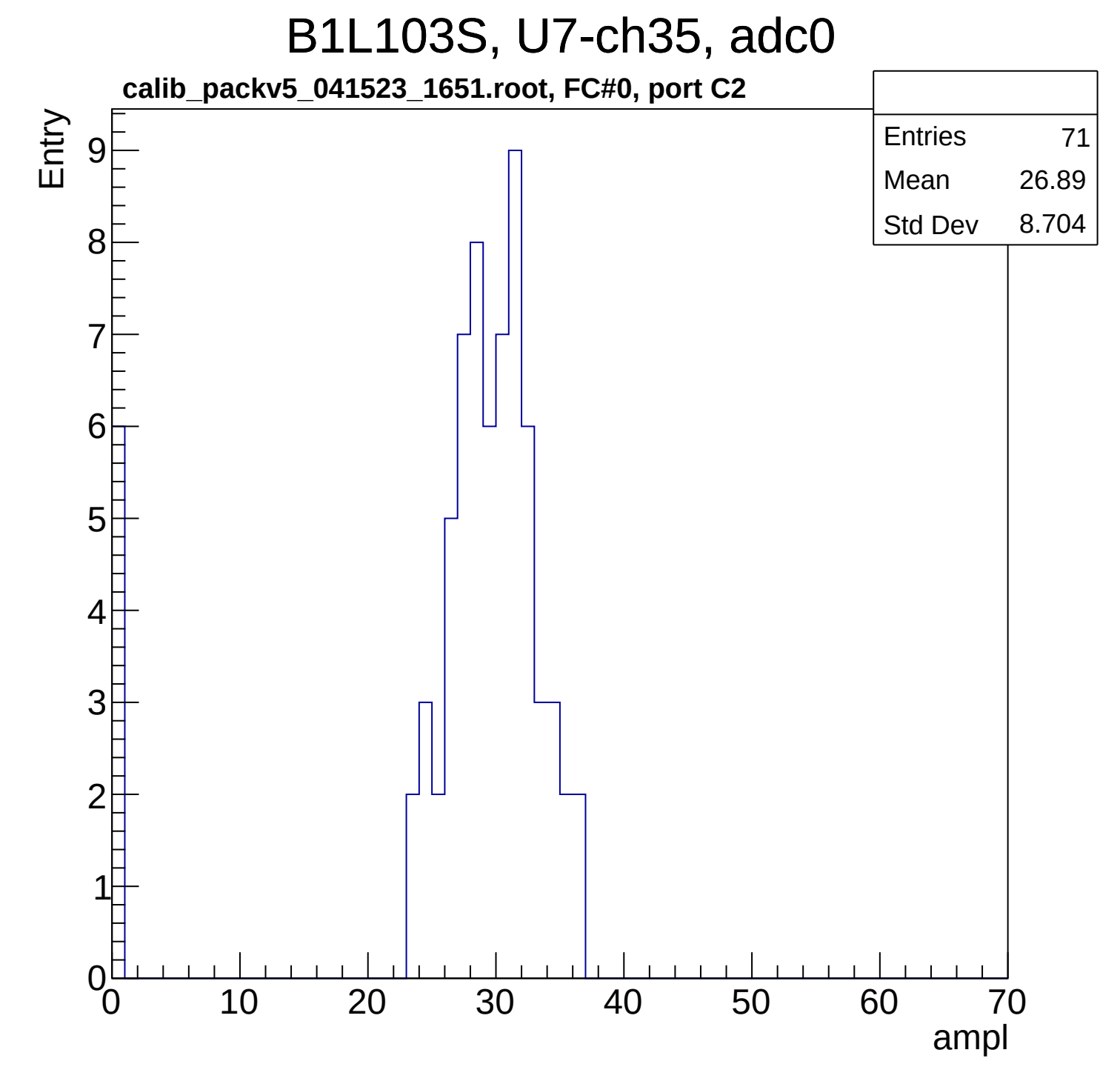
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch34, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 13
Mean 61.85
Std Dev 1.35
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U7-ch34, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 10
Std Dev 22
Entry
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch35, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 26.89
Std Dev 8.704
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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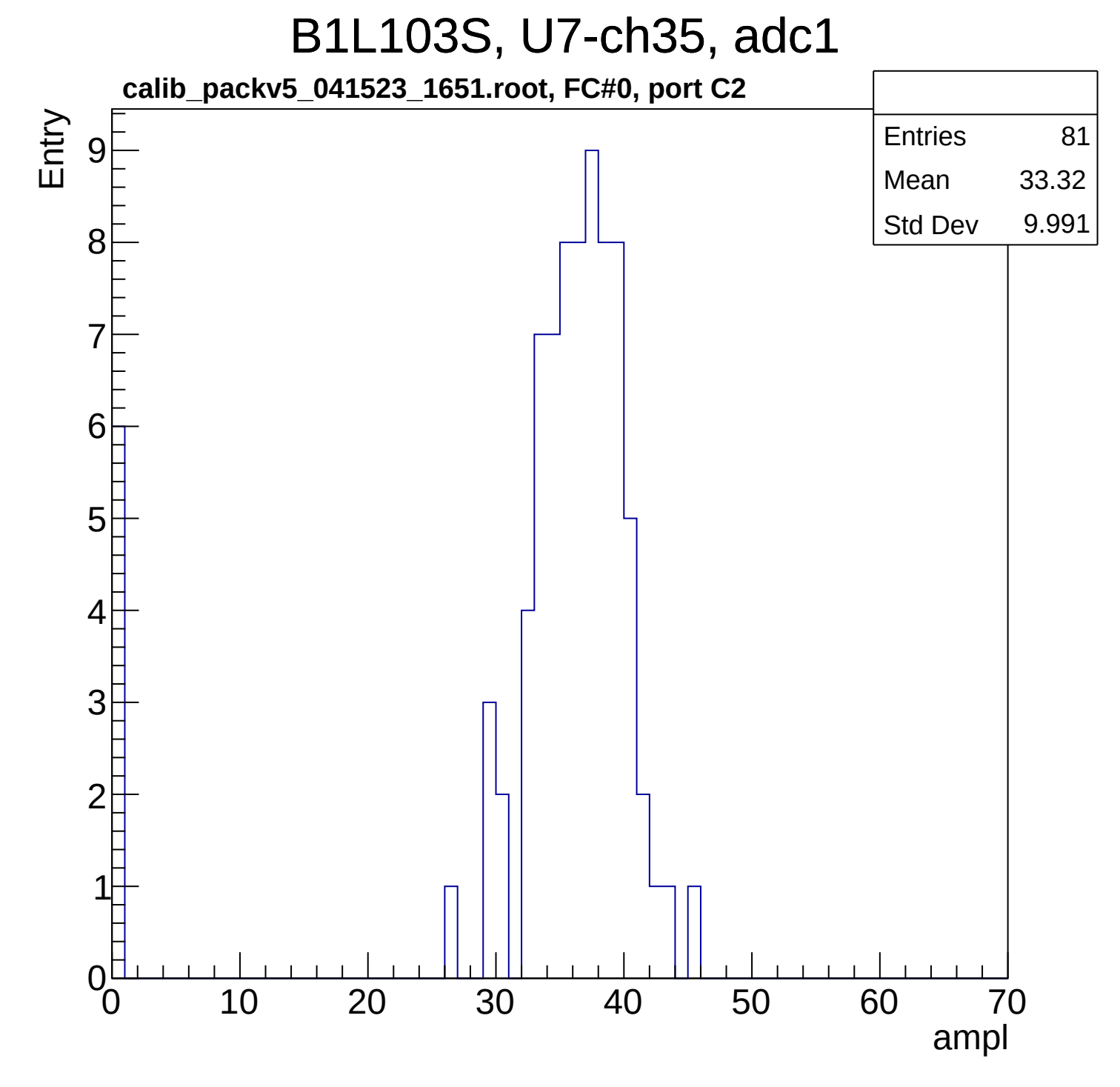
40
50
60
70


B1L103S, U7-ch35, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 33.32
Std Dev 9.991
Entry
ampl
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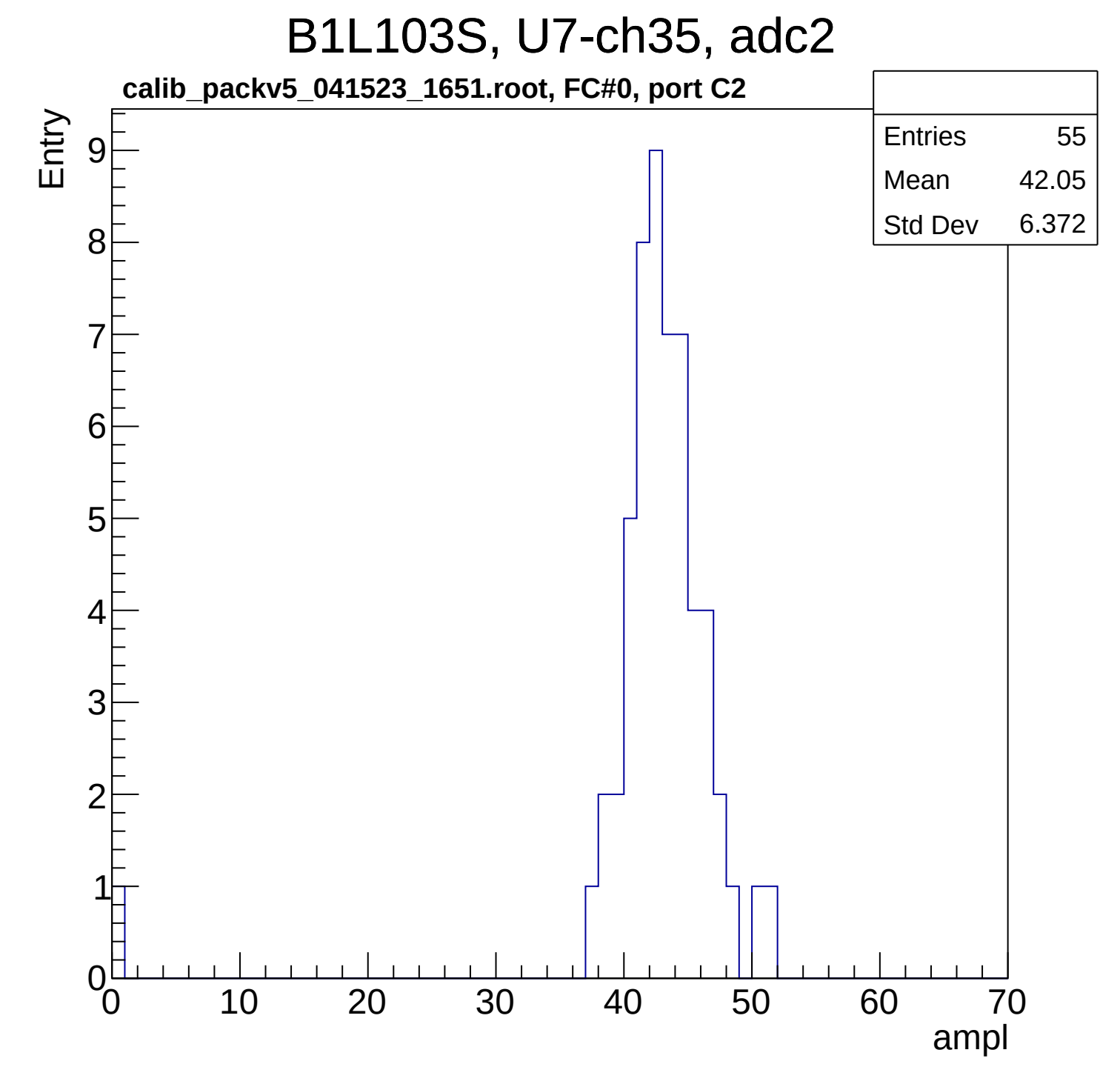
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U7-ch35, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 42.05
Std Dev 6.372
Entry
ampl
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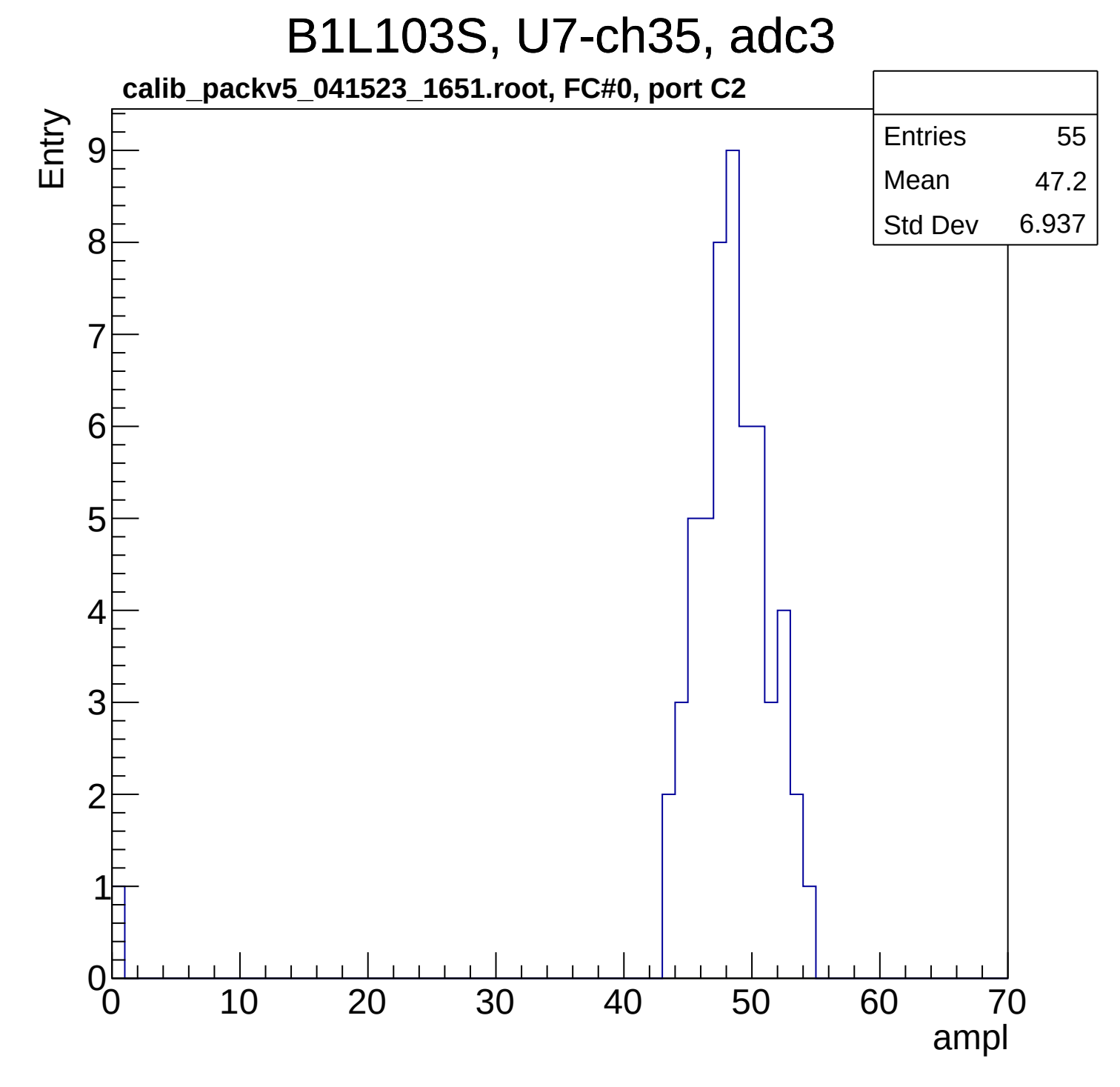
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U7-ch35, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 47.2
Std Dev 6.937
Entry
ampl
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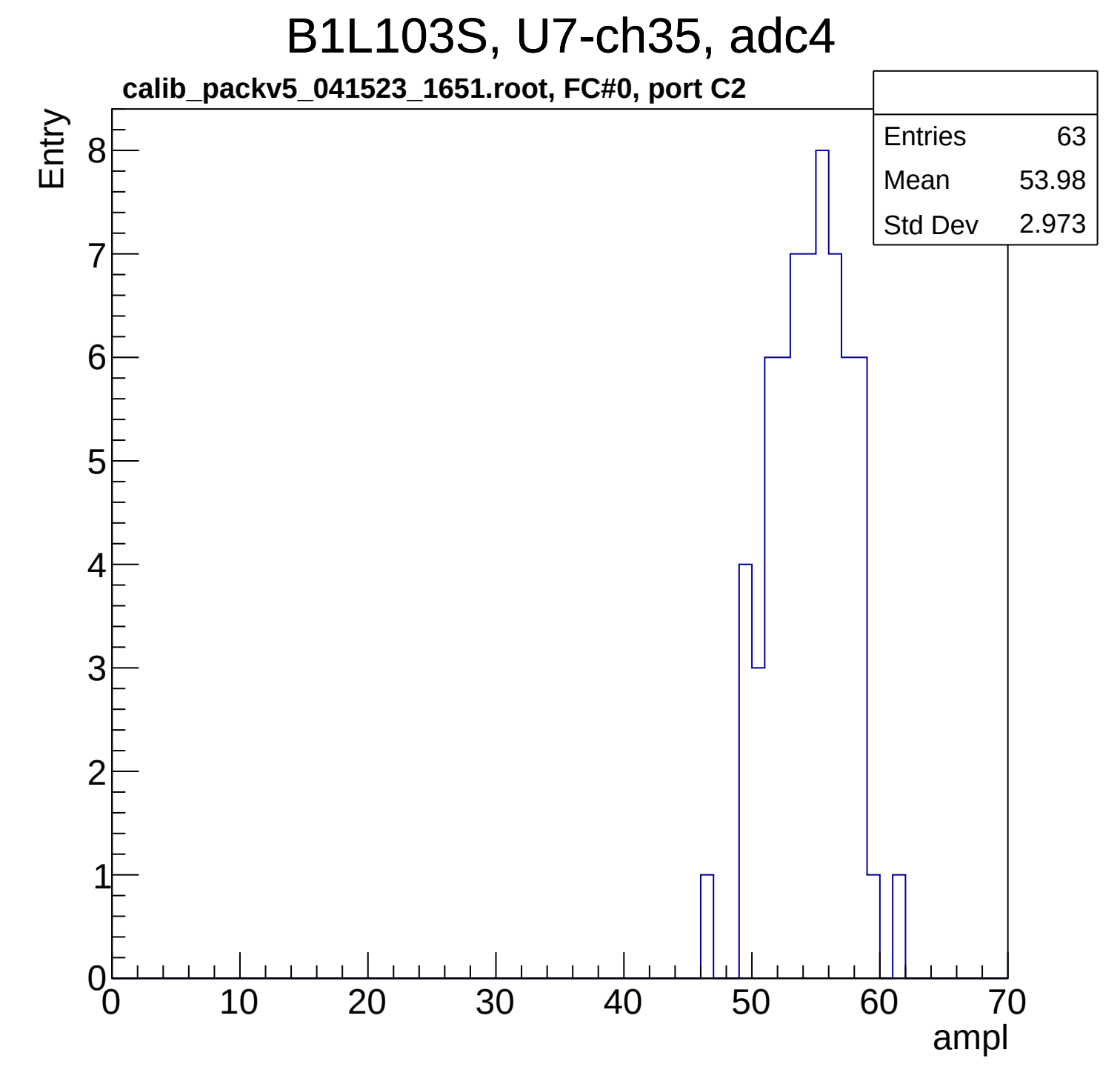
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U7-ch35, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 53.98
Std Dev 2.973
Entry
ampl
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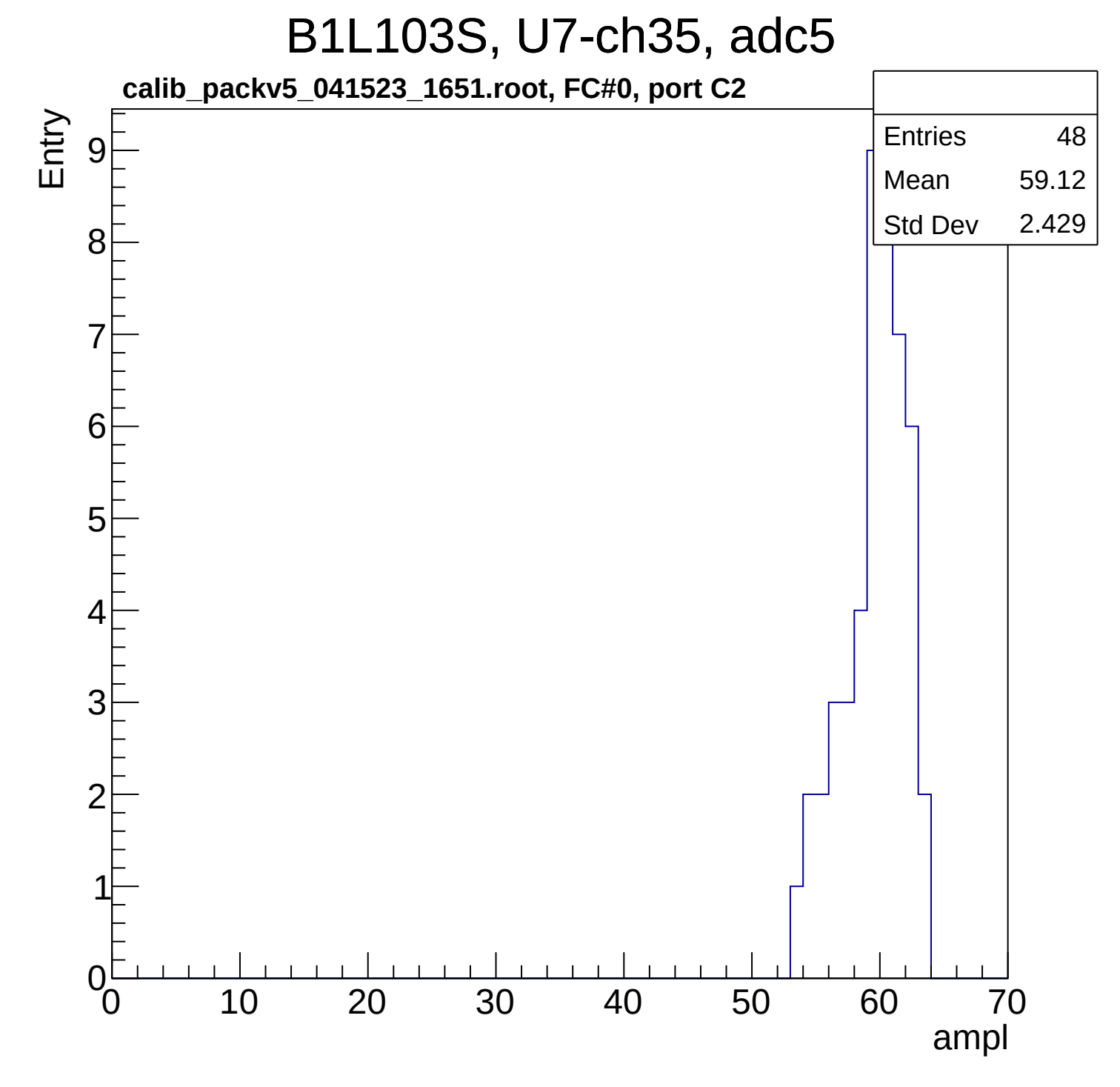
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch35, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 59.12
Std Dev 2.429
Entry
ampl
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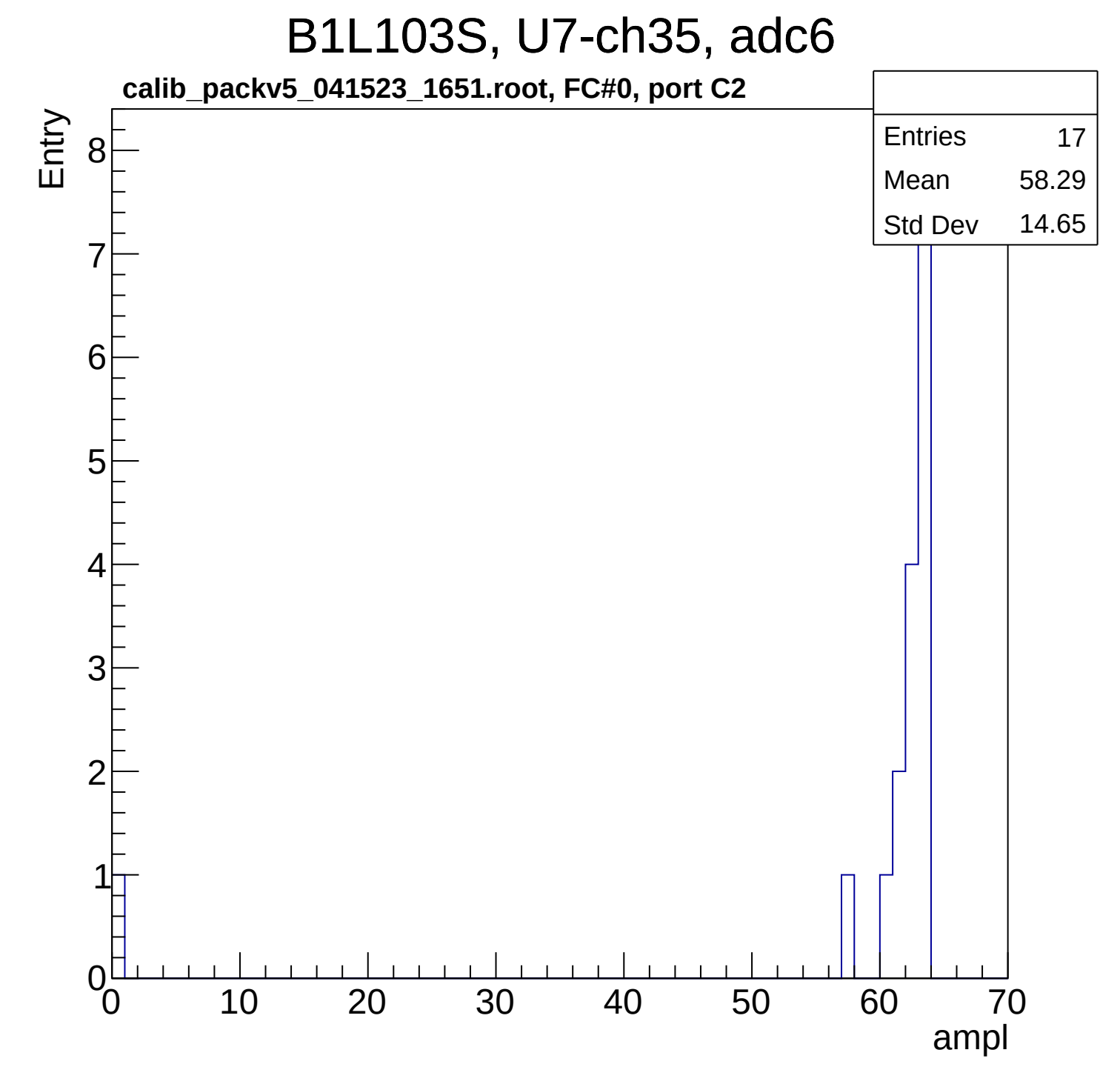
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U7-ch35, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 17
Mean 58.29
Std Dev 14.65
Entry
ampl
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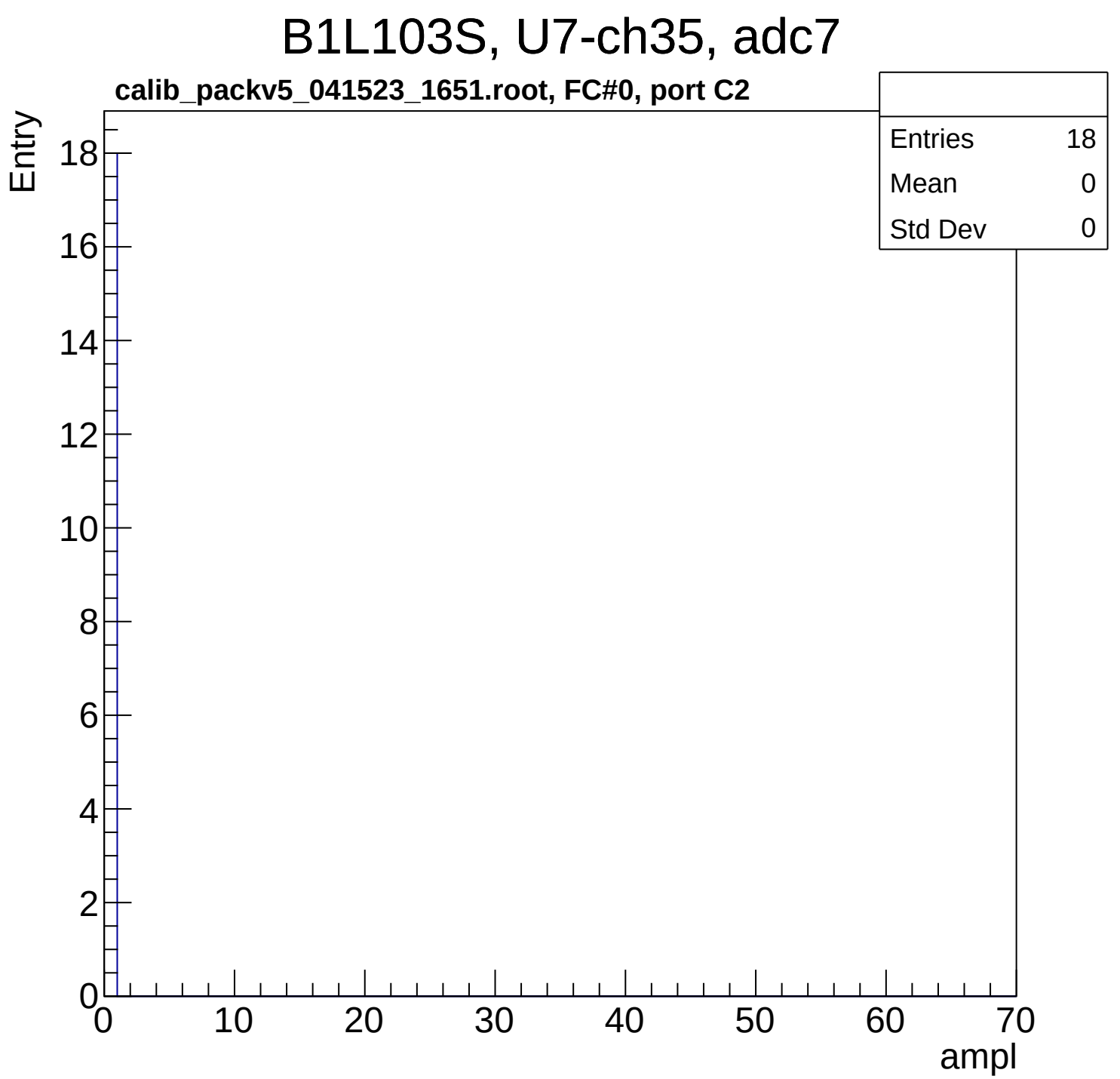
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch35, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
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30
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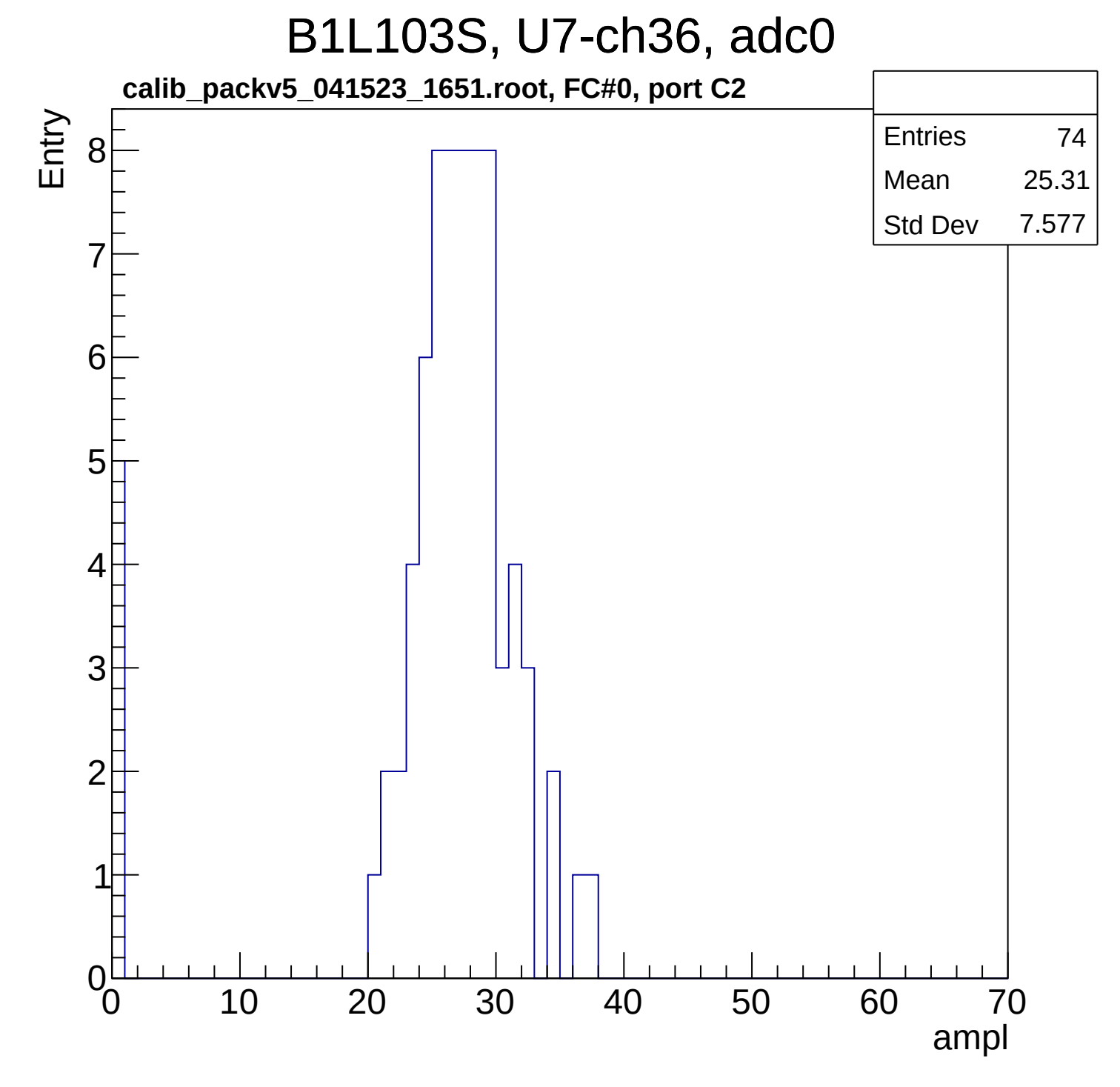
50
60
70
ampl


B1L103S, U7-ch36, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 25.31
Std Dev 7.577
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
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60
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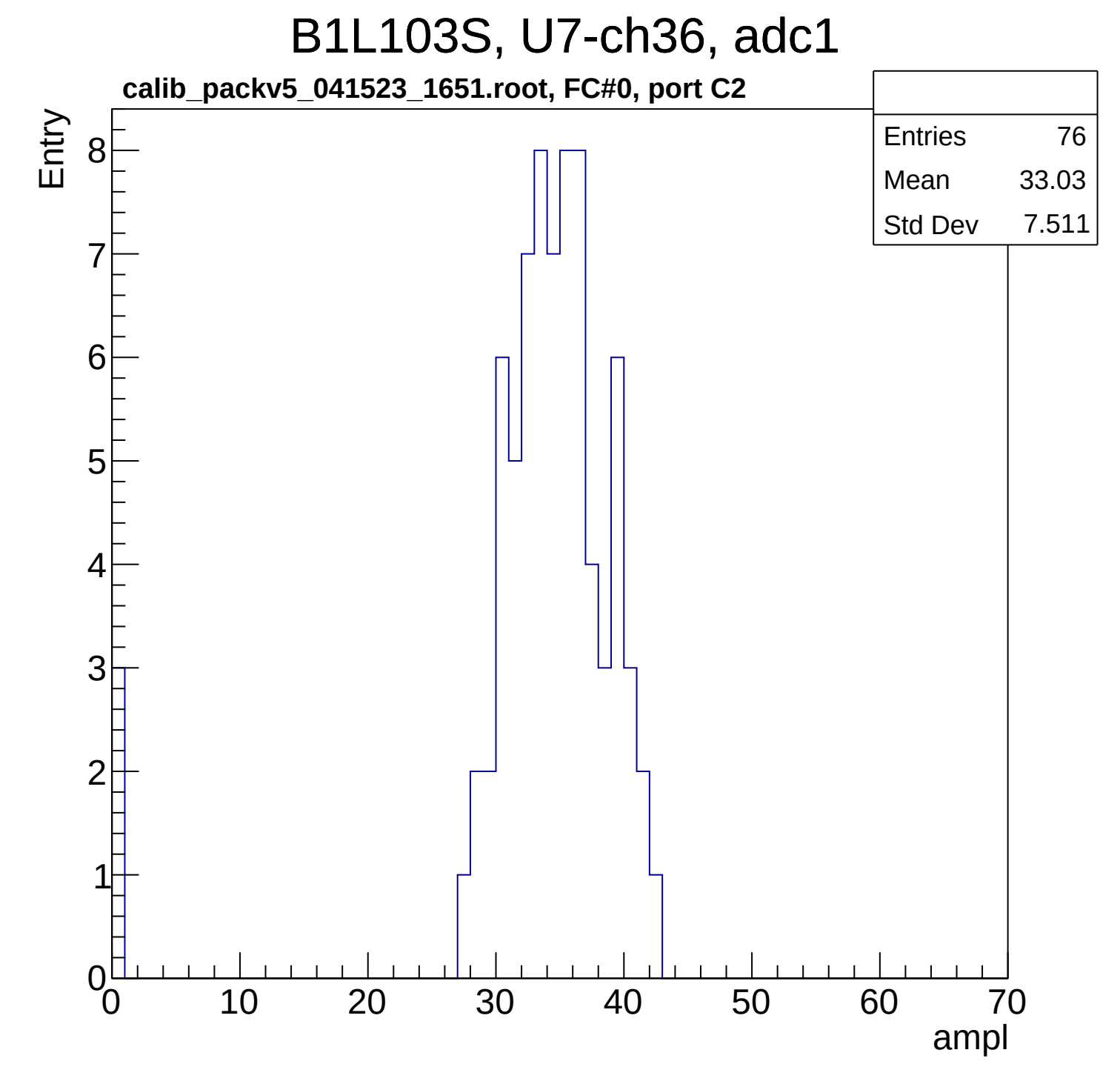
B1L103S, U7-ch36, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 33.03
Std Dev 7.511
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
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60
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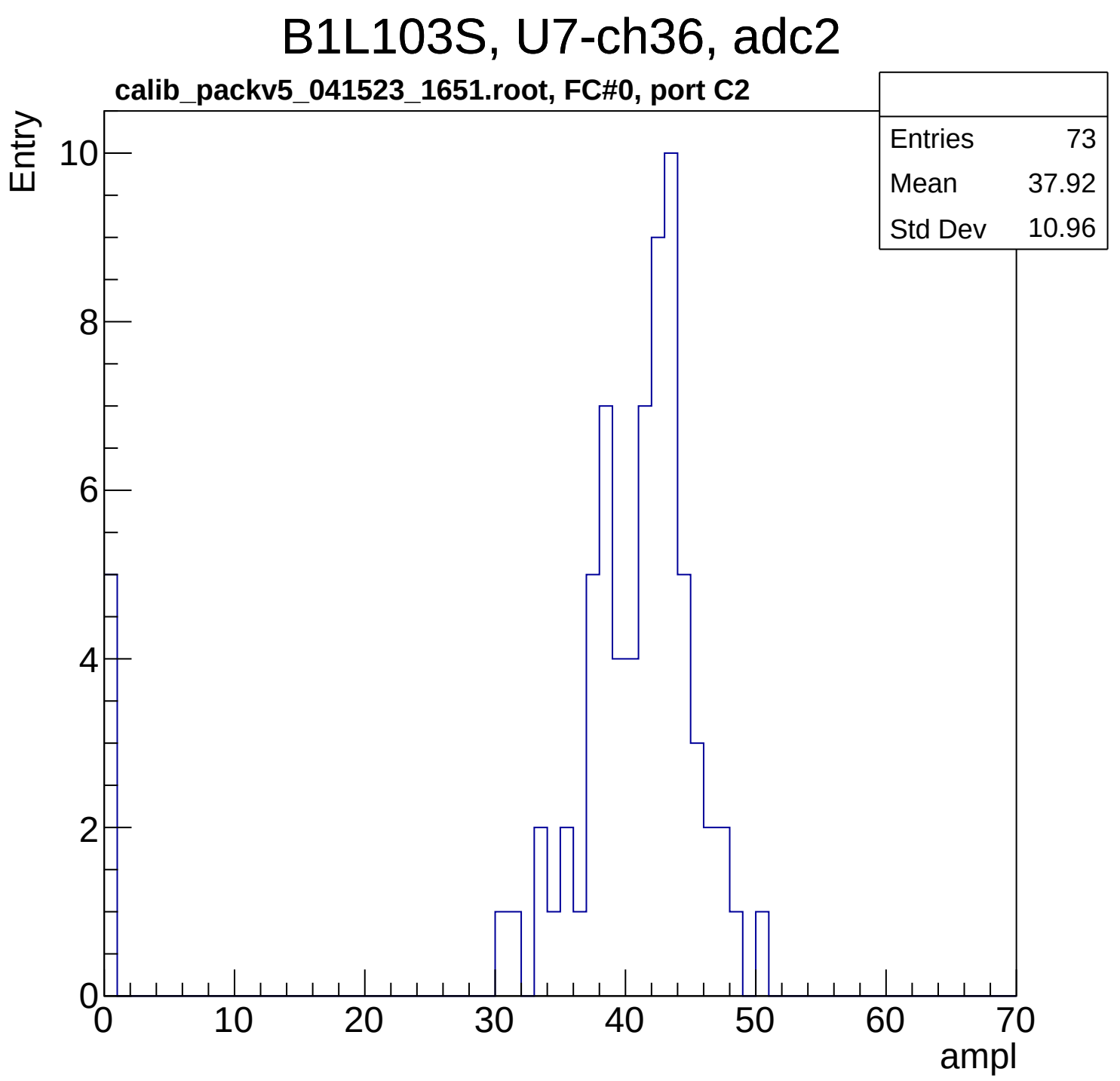
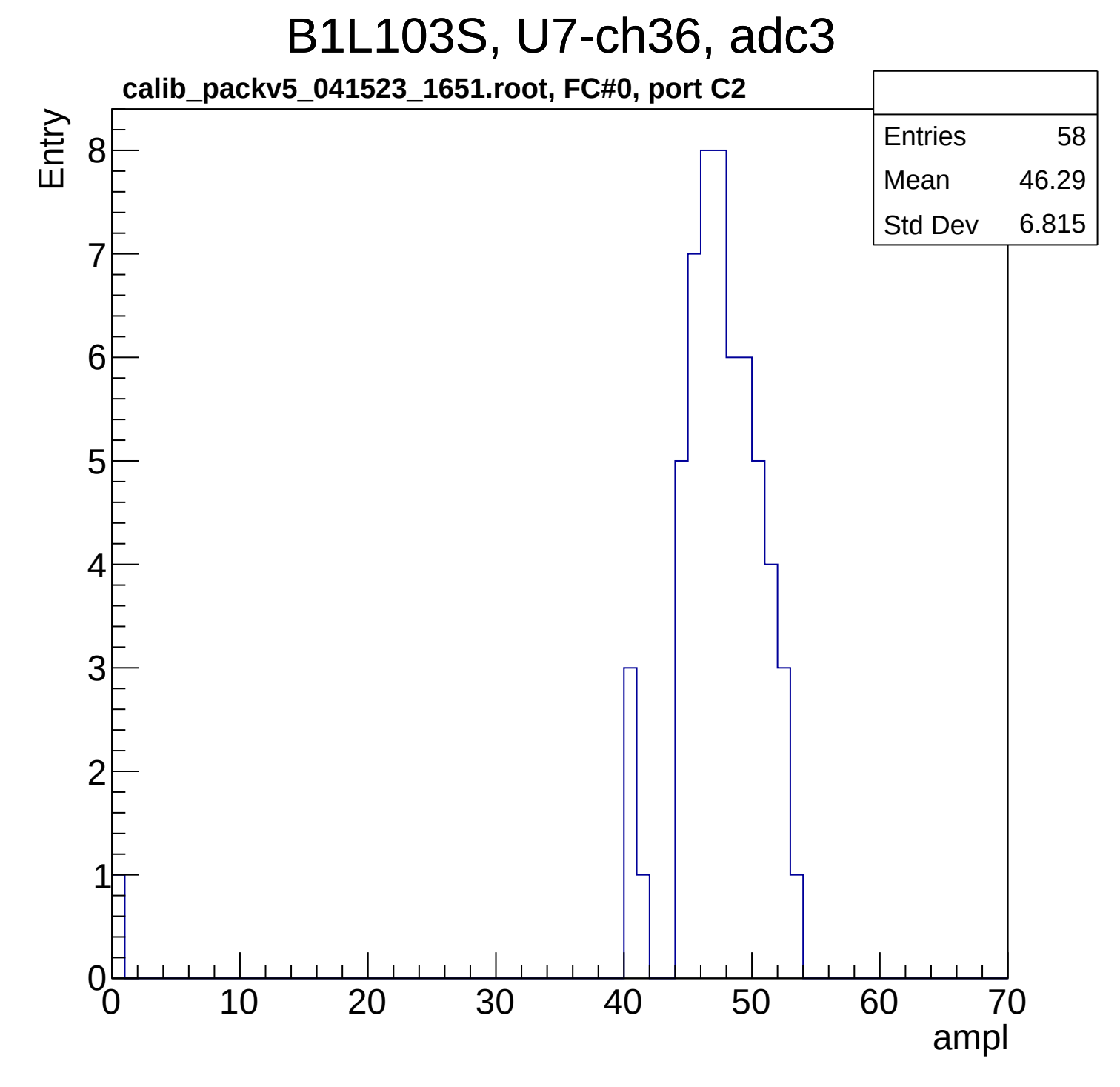

B1L103S, U7-ch36, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 37.92
Std Dev 10.96
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U7-ch36, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 46.29
Std Dev 6.815
Entry
ampl
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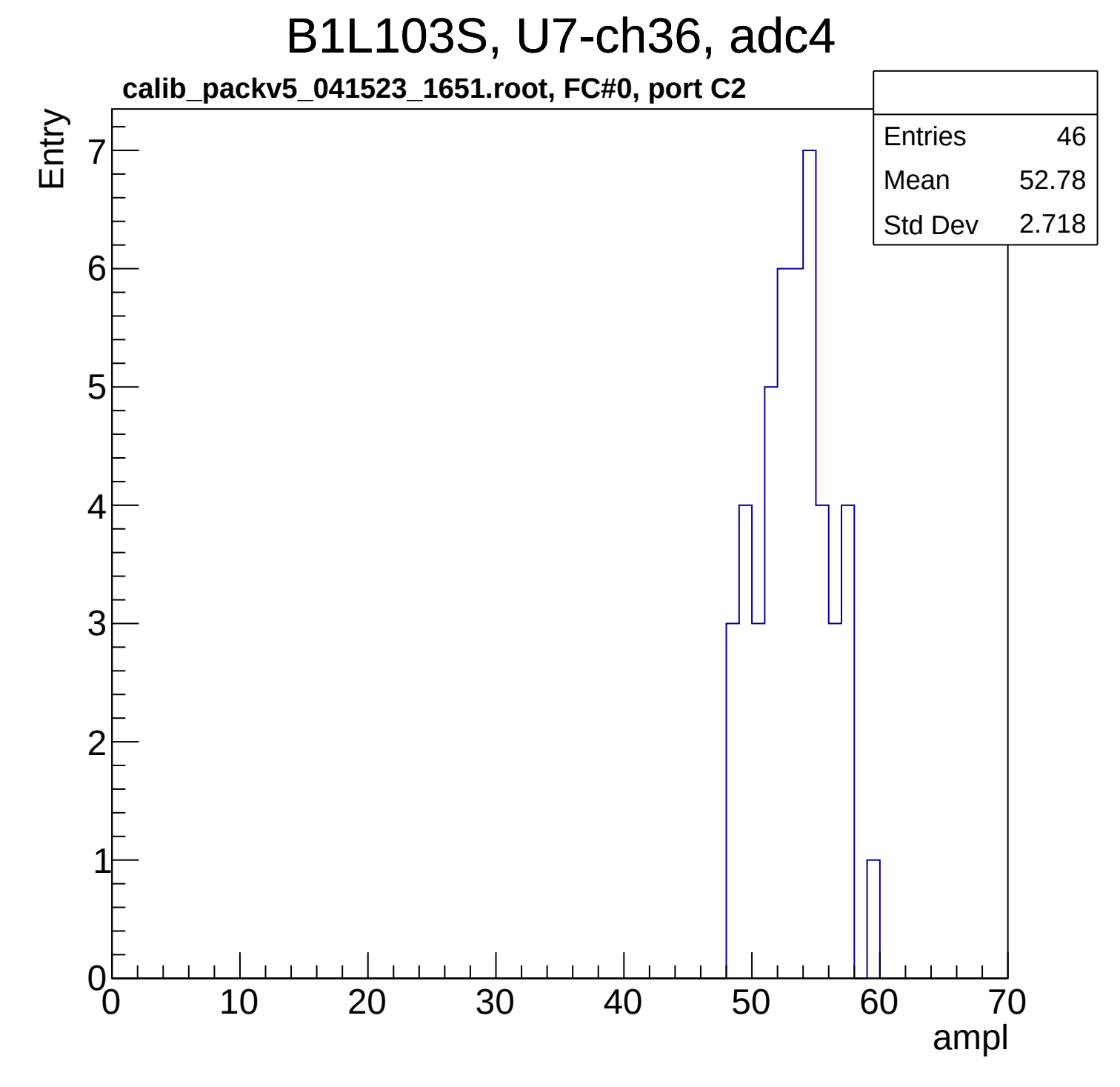
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch36, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 52.78
Std Dev 2.718
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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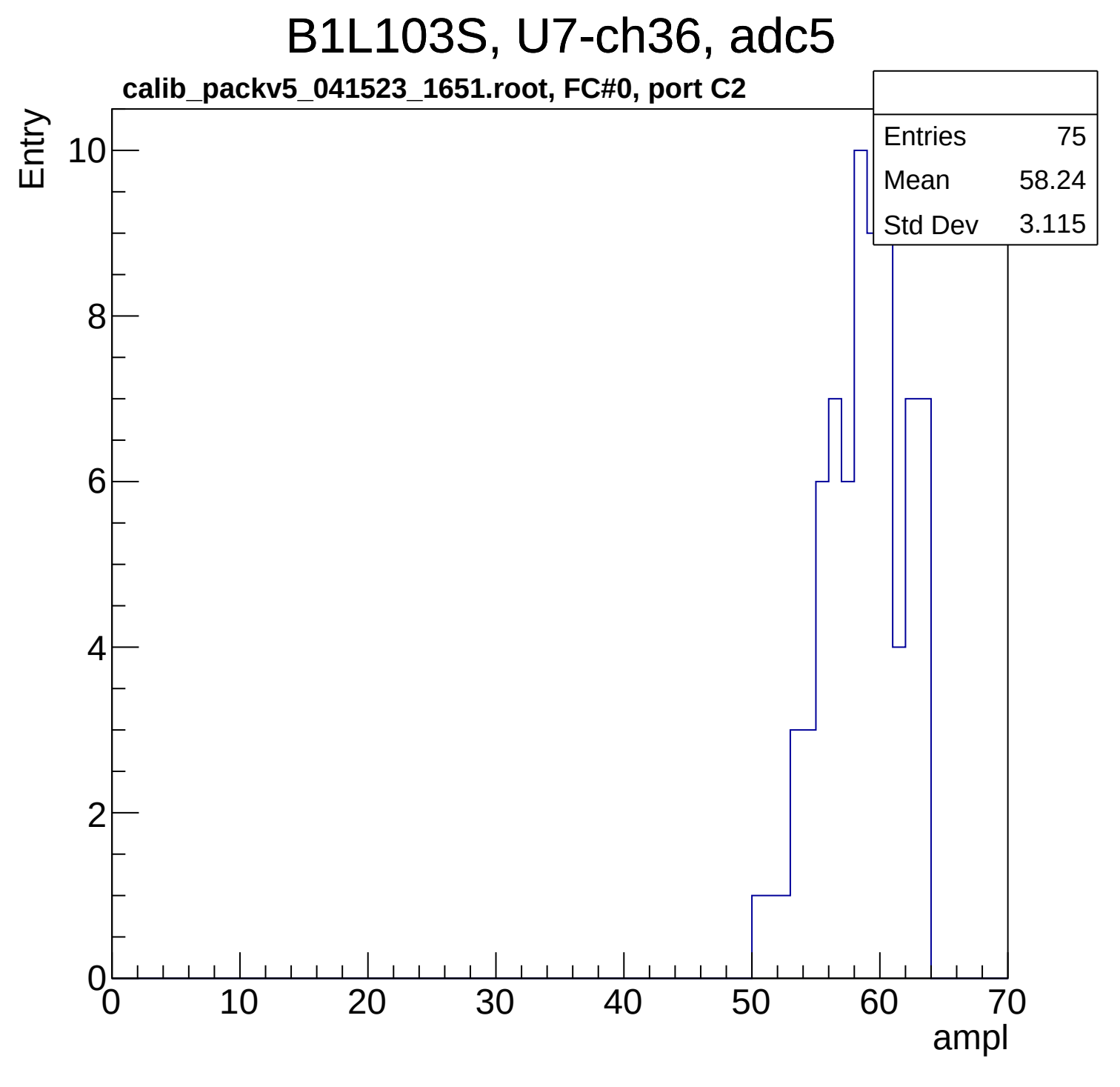
B1L103S, U7-ch36, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 58.24
Std Dev 3.115
Entry
ampl
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2
4
6
8
10
0
10
20
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40
50
60
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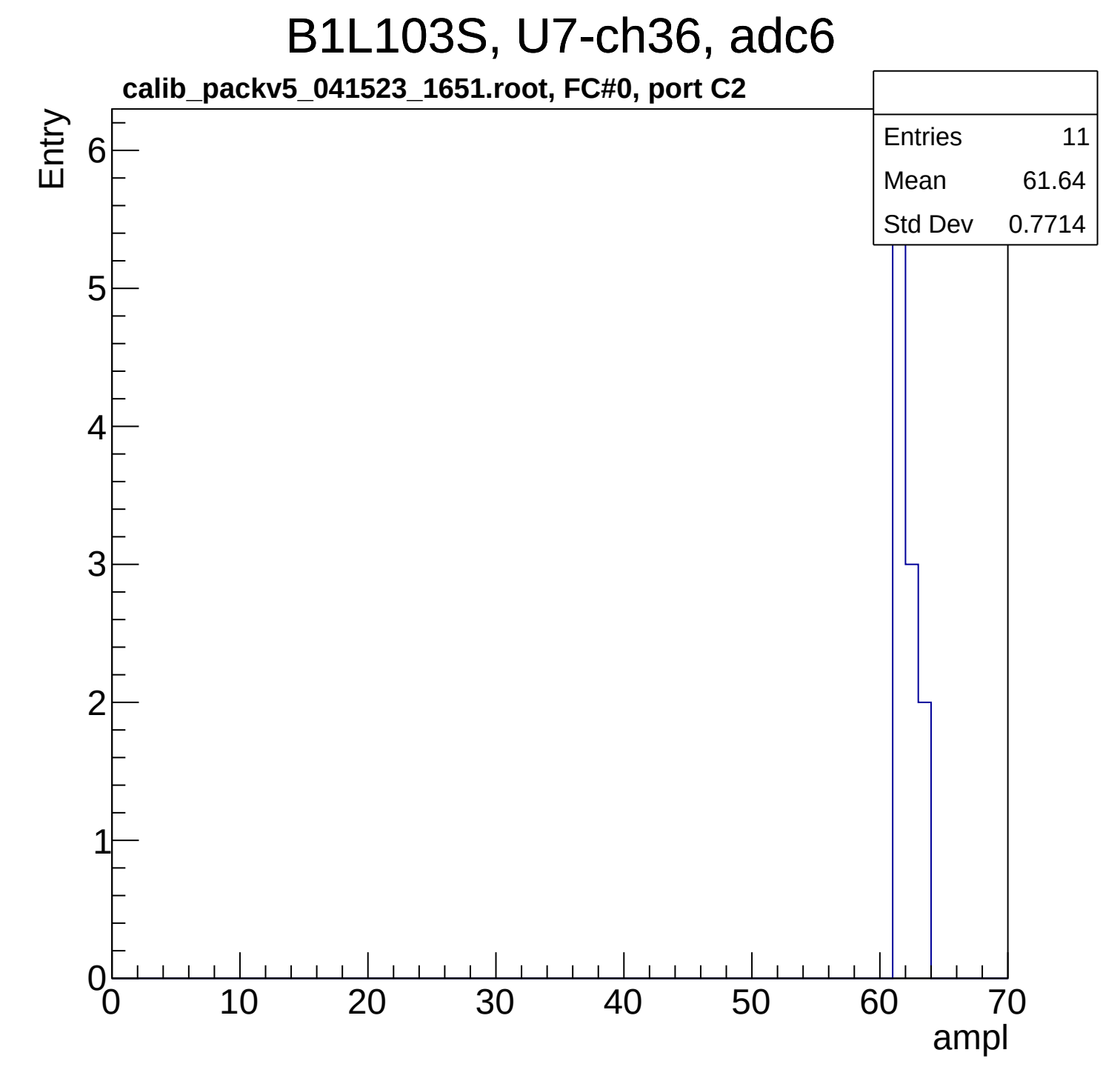
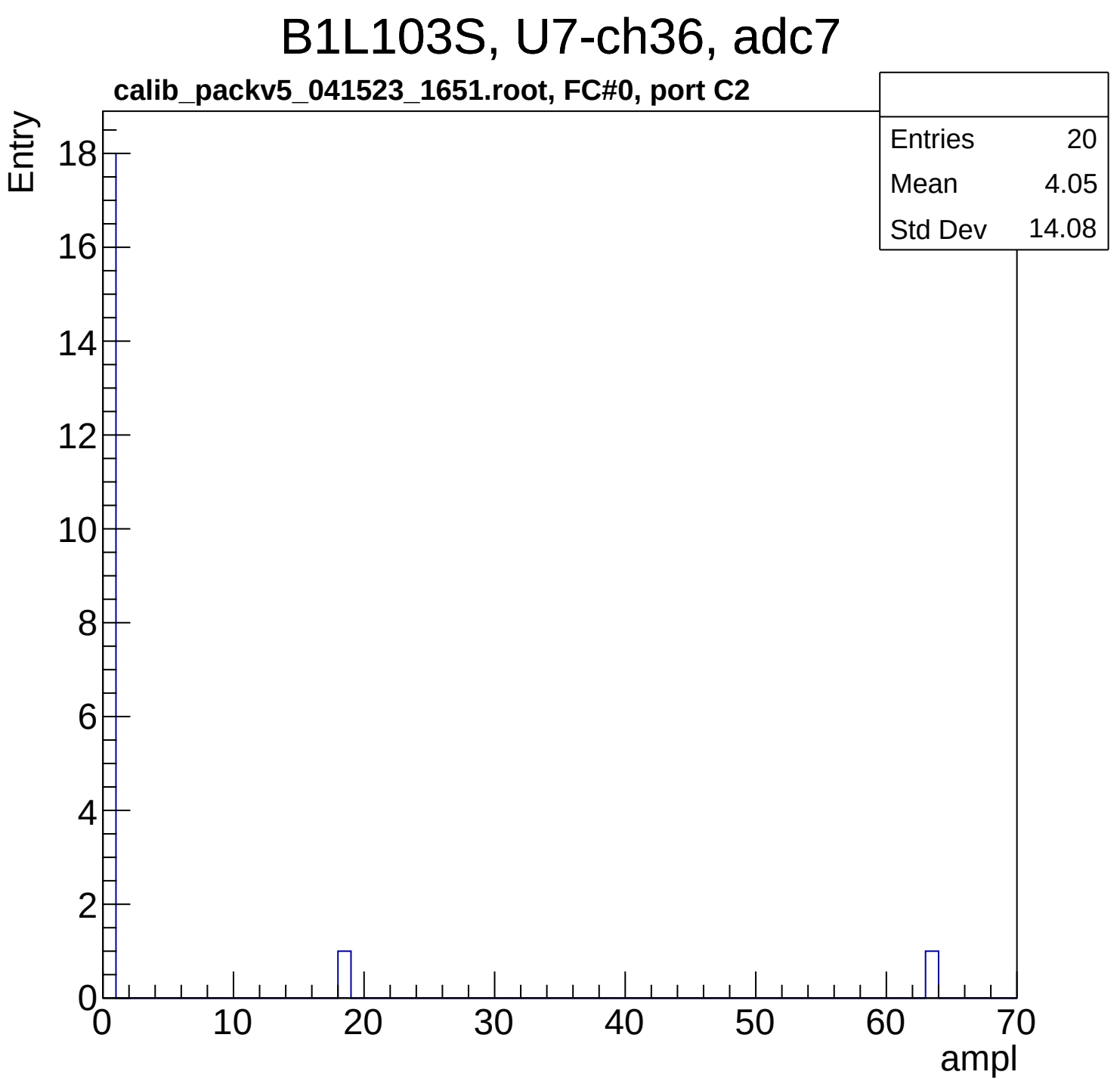

B1L103S, U7-ch36, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 61.64
Std Dev 0.7714
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U7-ch36, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 4.05
Std Dev 14.08
Entry
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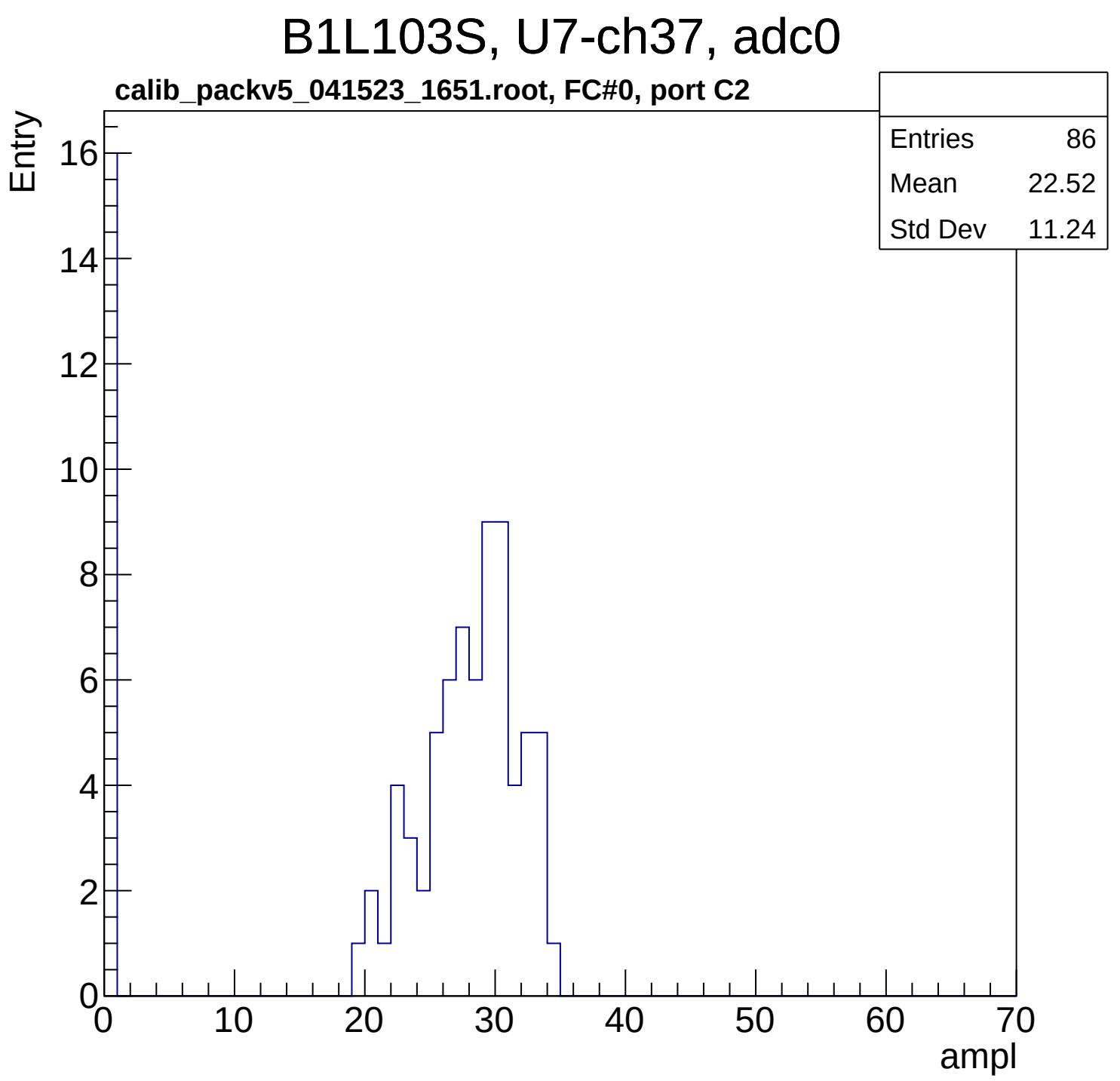
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch37, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 22.52
Std Dev 11.24
Entry
ampl
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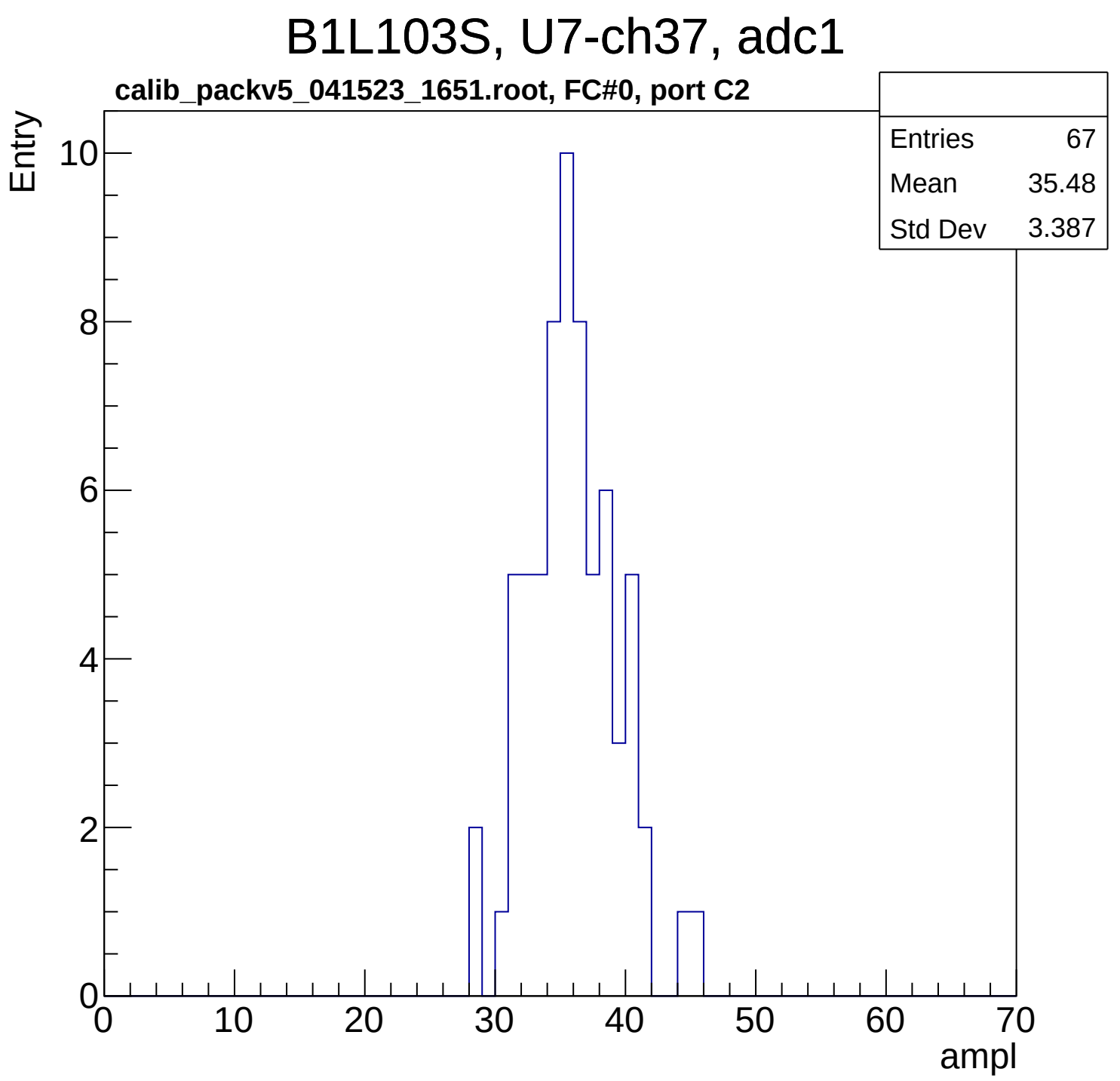
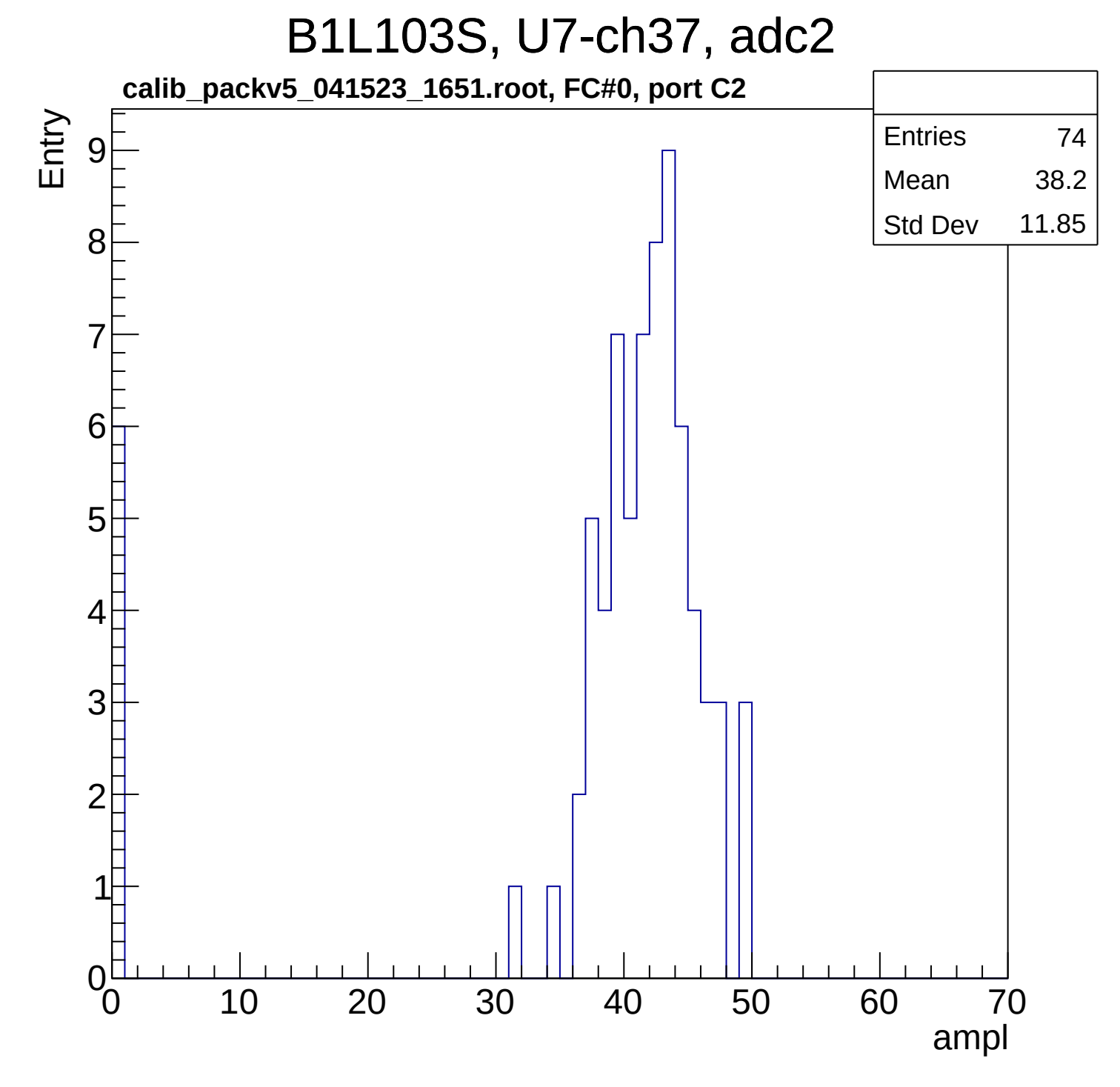
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70


B1L103S, U7-ch37, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 35.48
Std Dev 3.387
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch37, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 38.2
Std Dev 11.85
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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60
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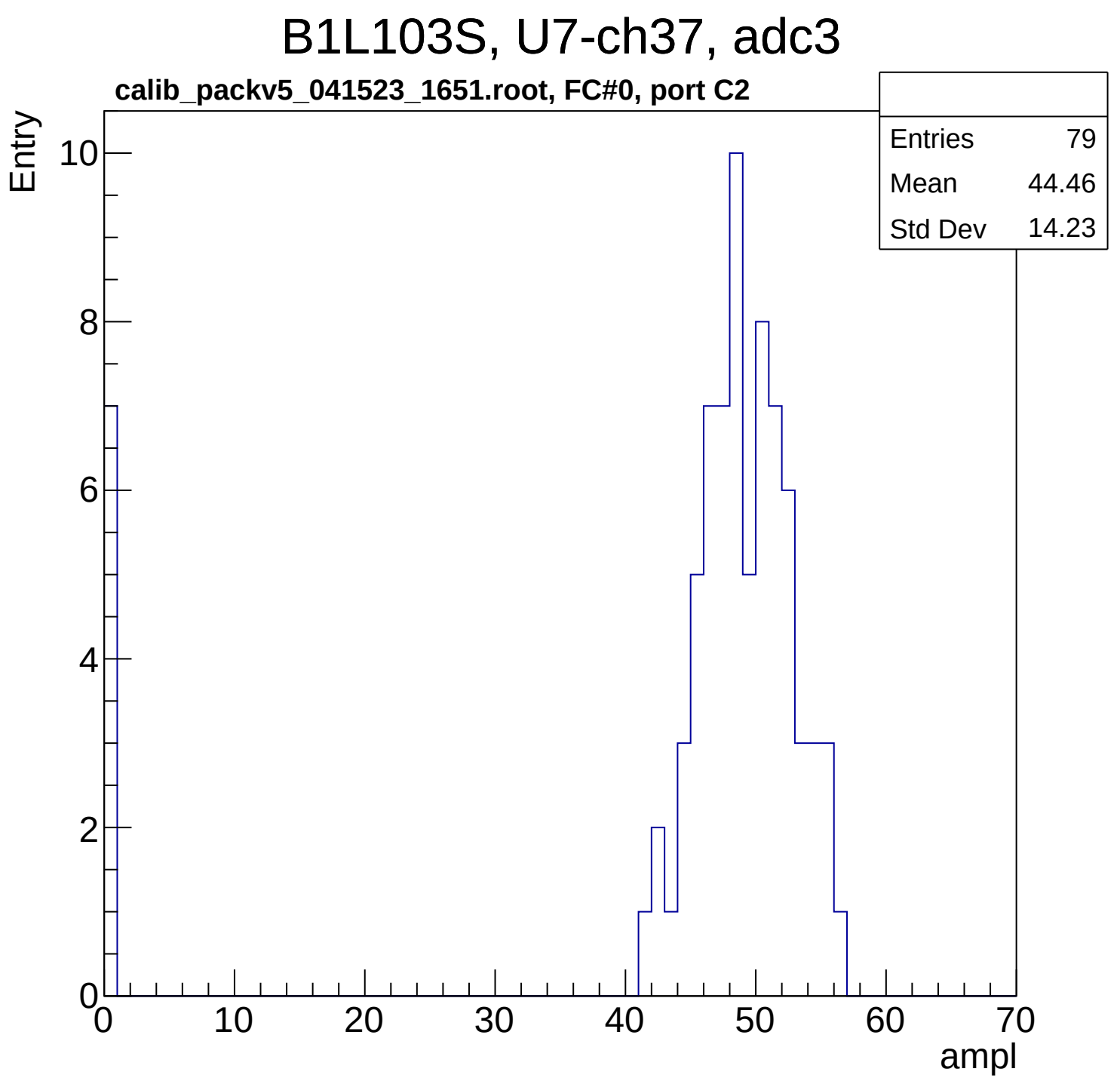
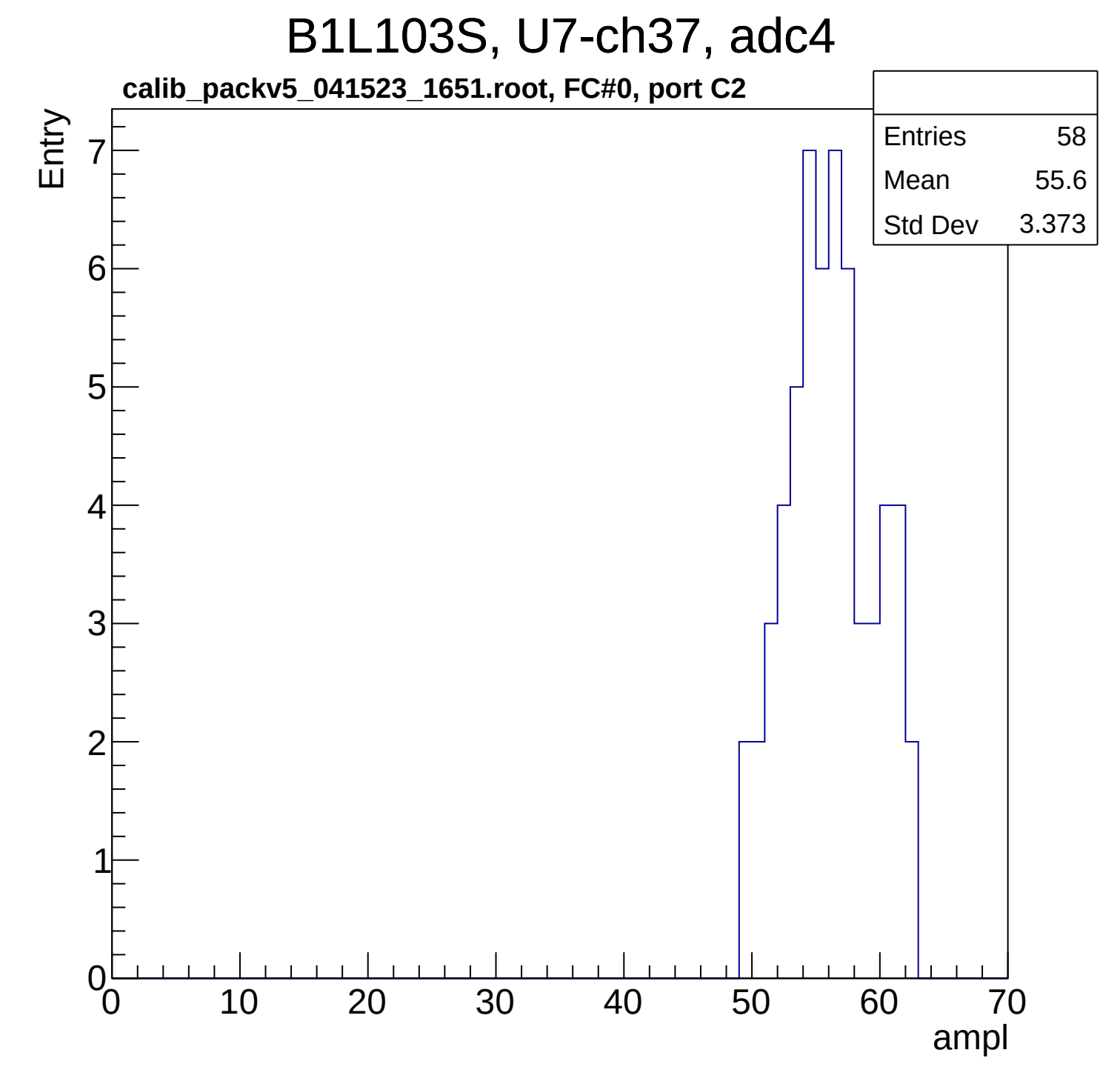

B1L103S, U7-ch37, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 44.46
Std Dev 14.23
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U7-ch37, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 55.6
Std Dev 3.373
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
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40
50
60
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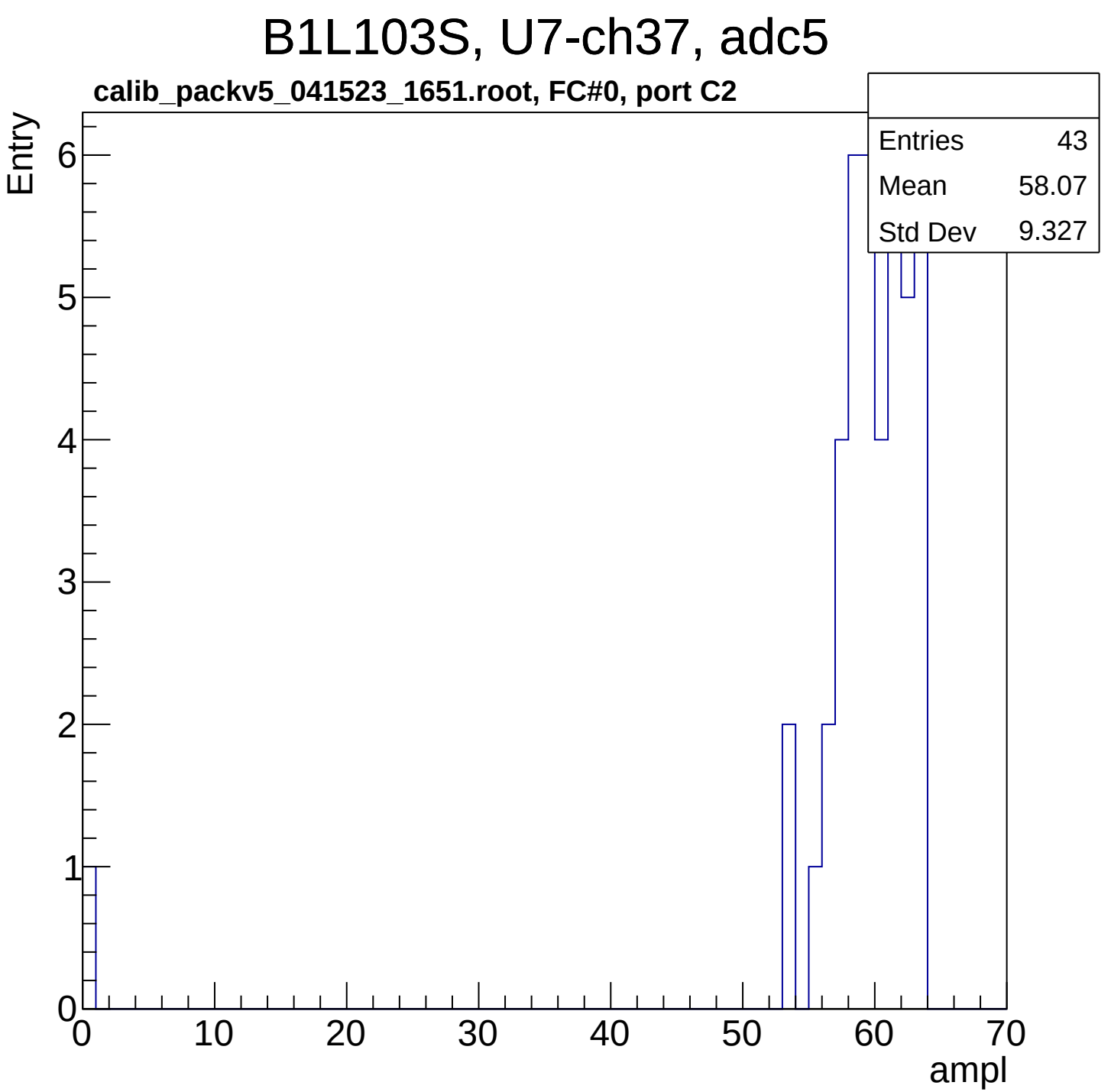
B1L103S, U7-ch37, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 43
Mean 58.07
Std Dev 9.327
Entry
ampl
0
1
2
3
4
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0
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40
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60
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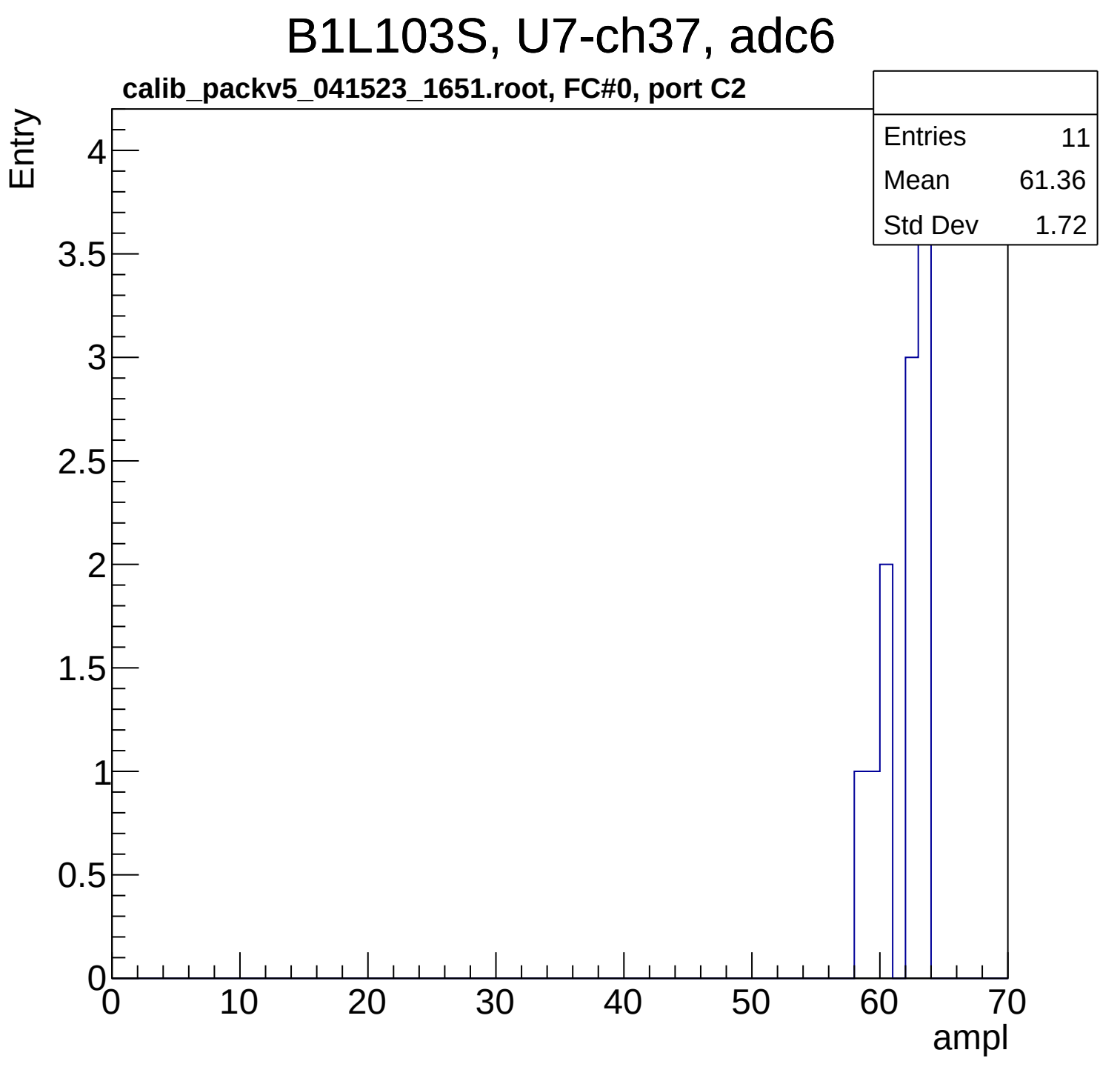
B1L103S, U7-ch37, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 61.36
Std Dev 1.72
Entry
ampl
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0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
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50
60
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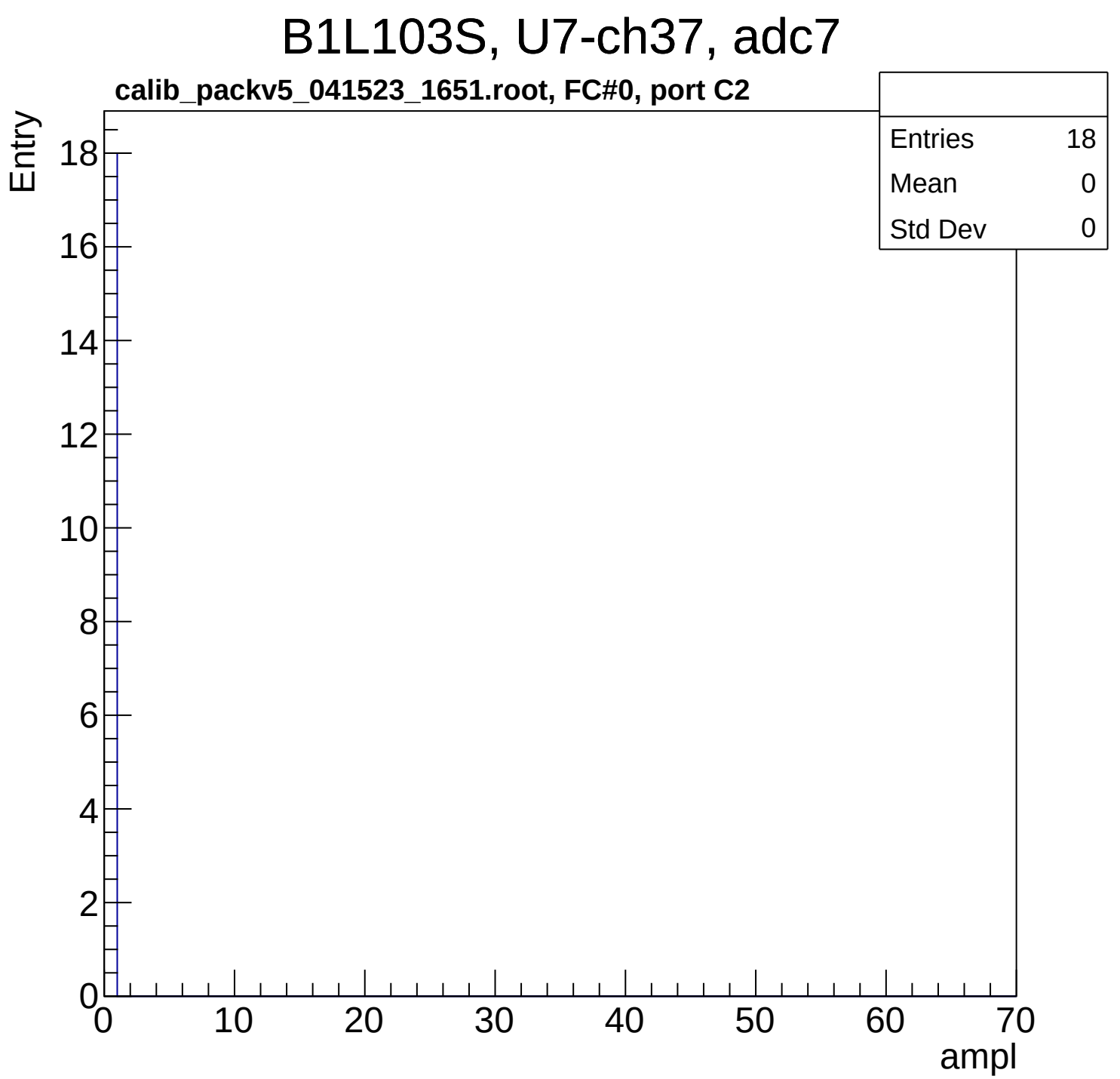
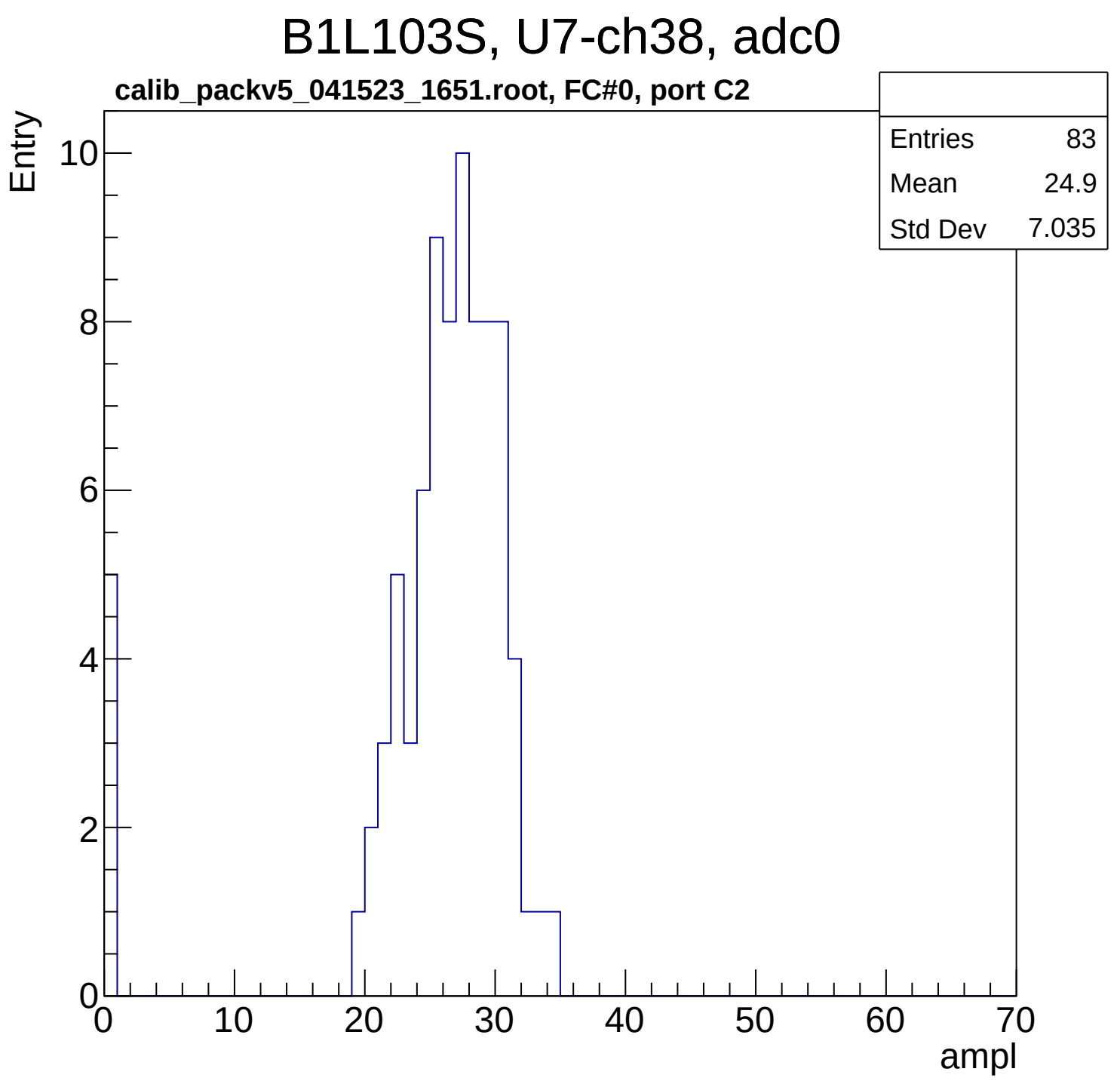

B1L103S, U7-ch37, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch38, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 24.9
Std Dev 7.035
Entry
0
2
4
6
8
10
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10
20
30
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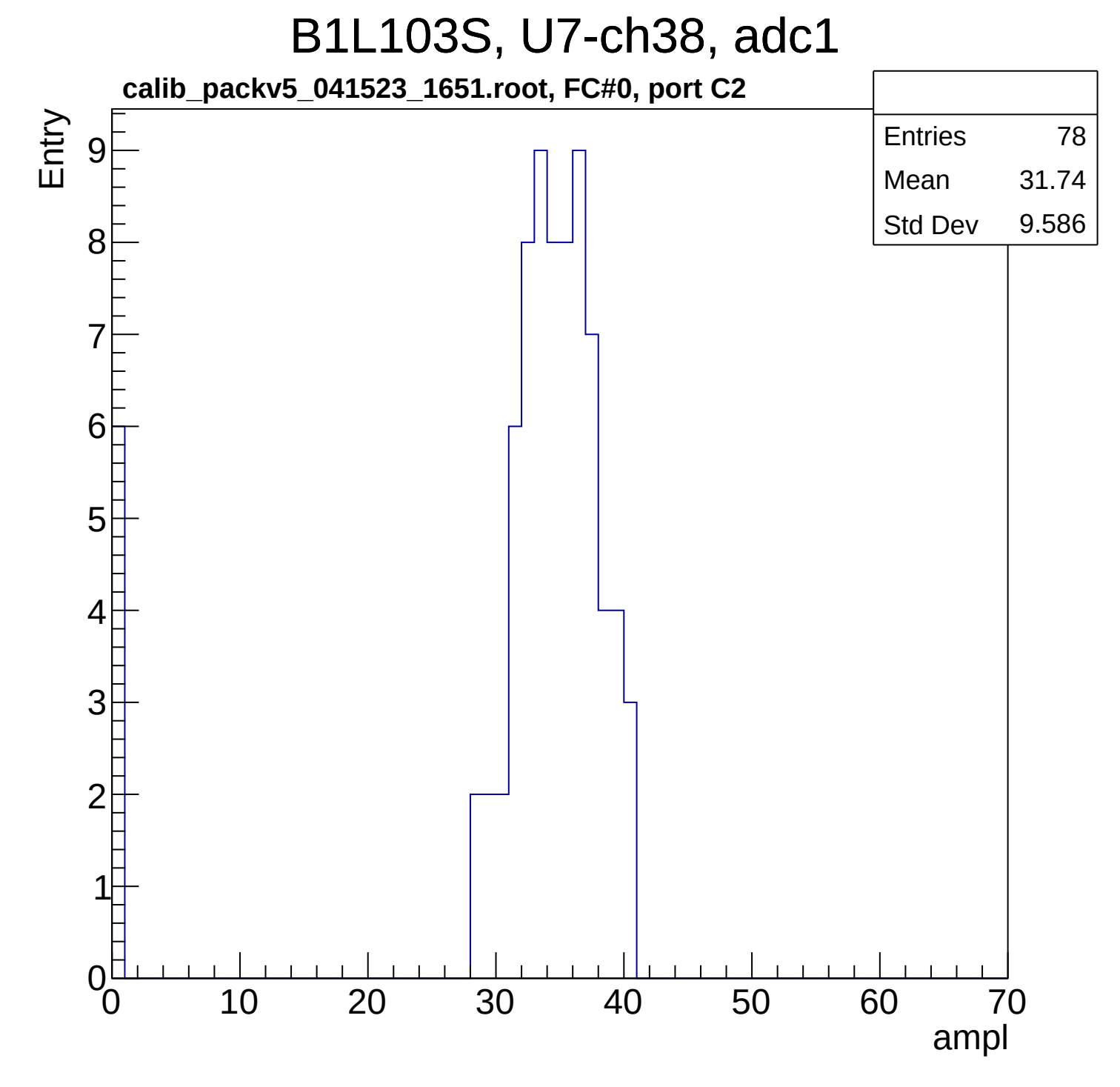
50
60
70
ampl


B1L103S, U7-ch38, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 31.74
Std Dev 9.586
Entry
ampl
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3
4
5
6
7
8
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0
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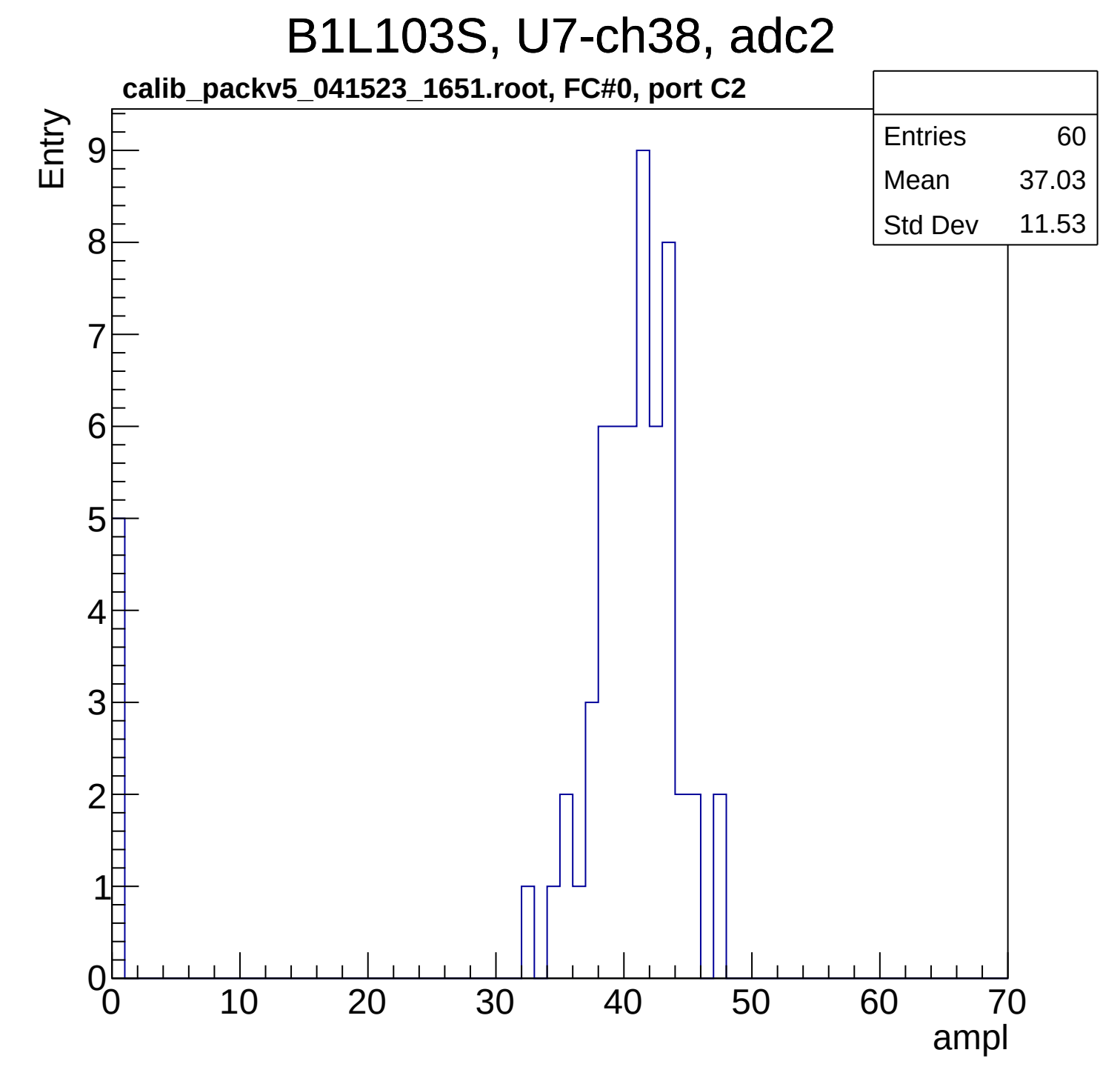
B1L103S, U7-ch38, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 37.03
Std Dev 11.53
Entry
ampl
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2
3
4
5
6
7
8
9
0
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60
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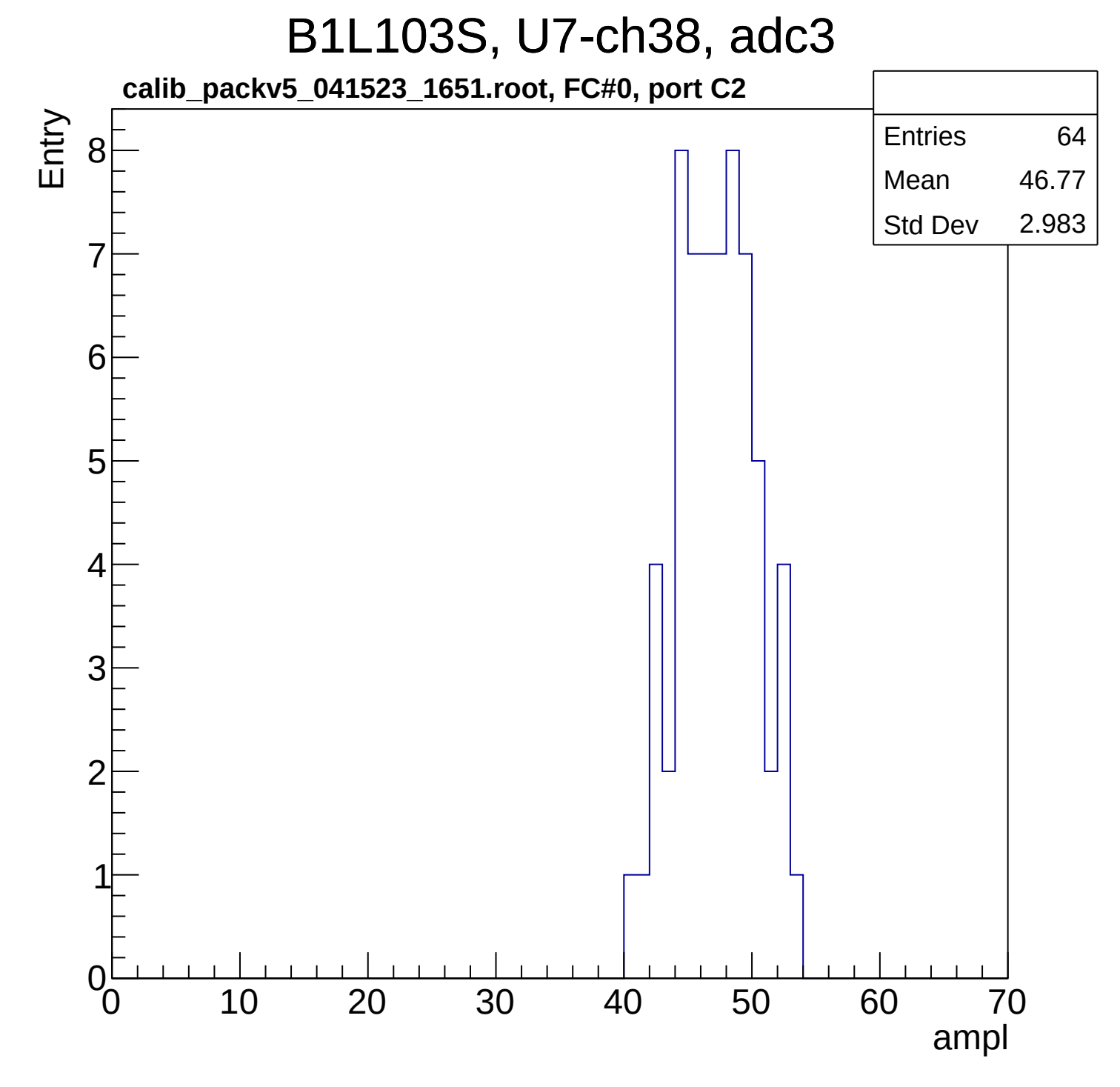
B1L103S, U7-ch38, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 46.77
Std Dev 2.983
Entry
ampl
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7
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0
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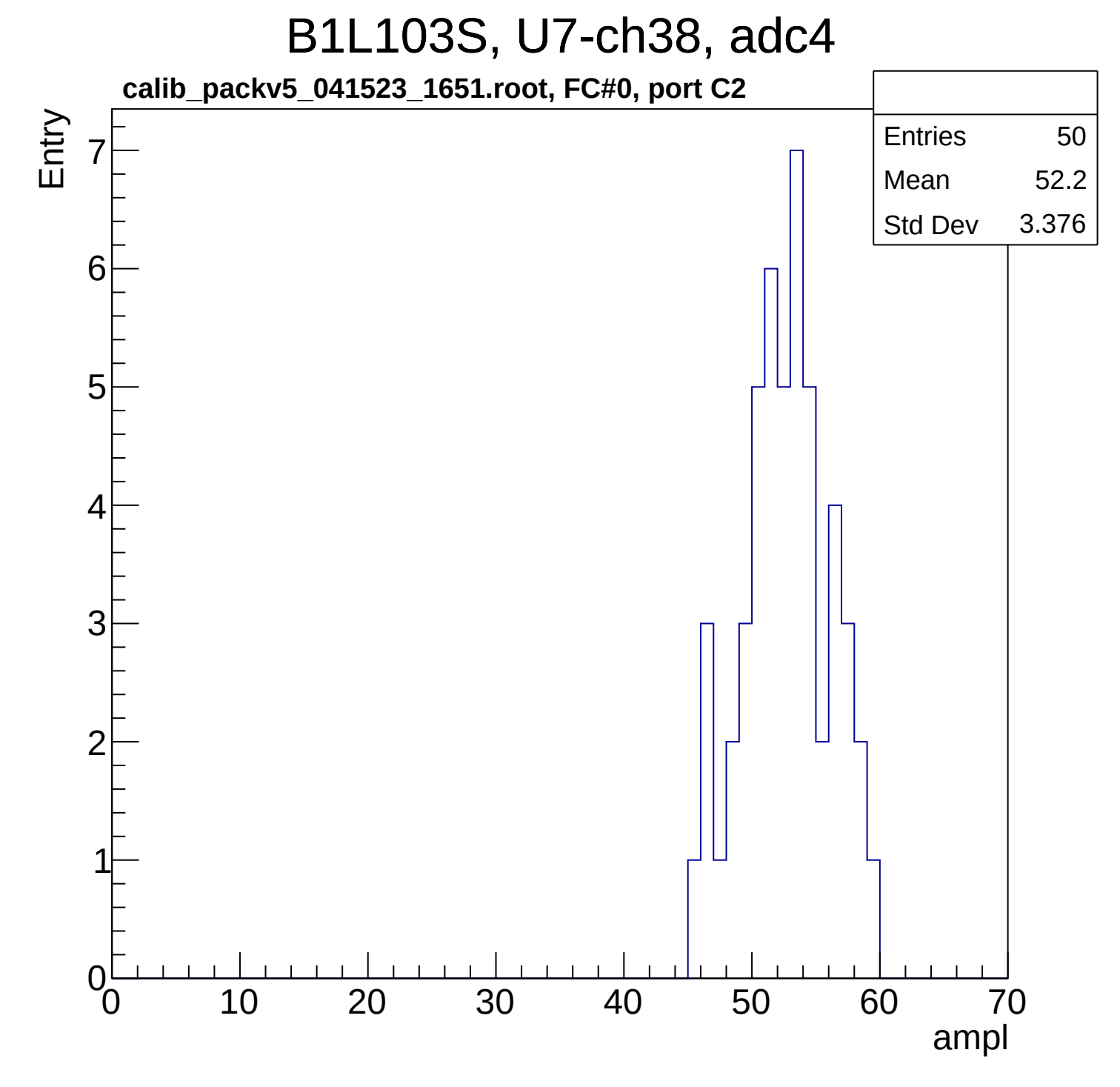
B1L103S, U7-ch38, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 52.2
Std Dev 3.376
Entry
ampl
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4
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0
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40
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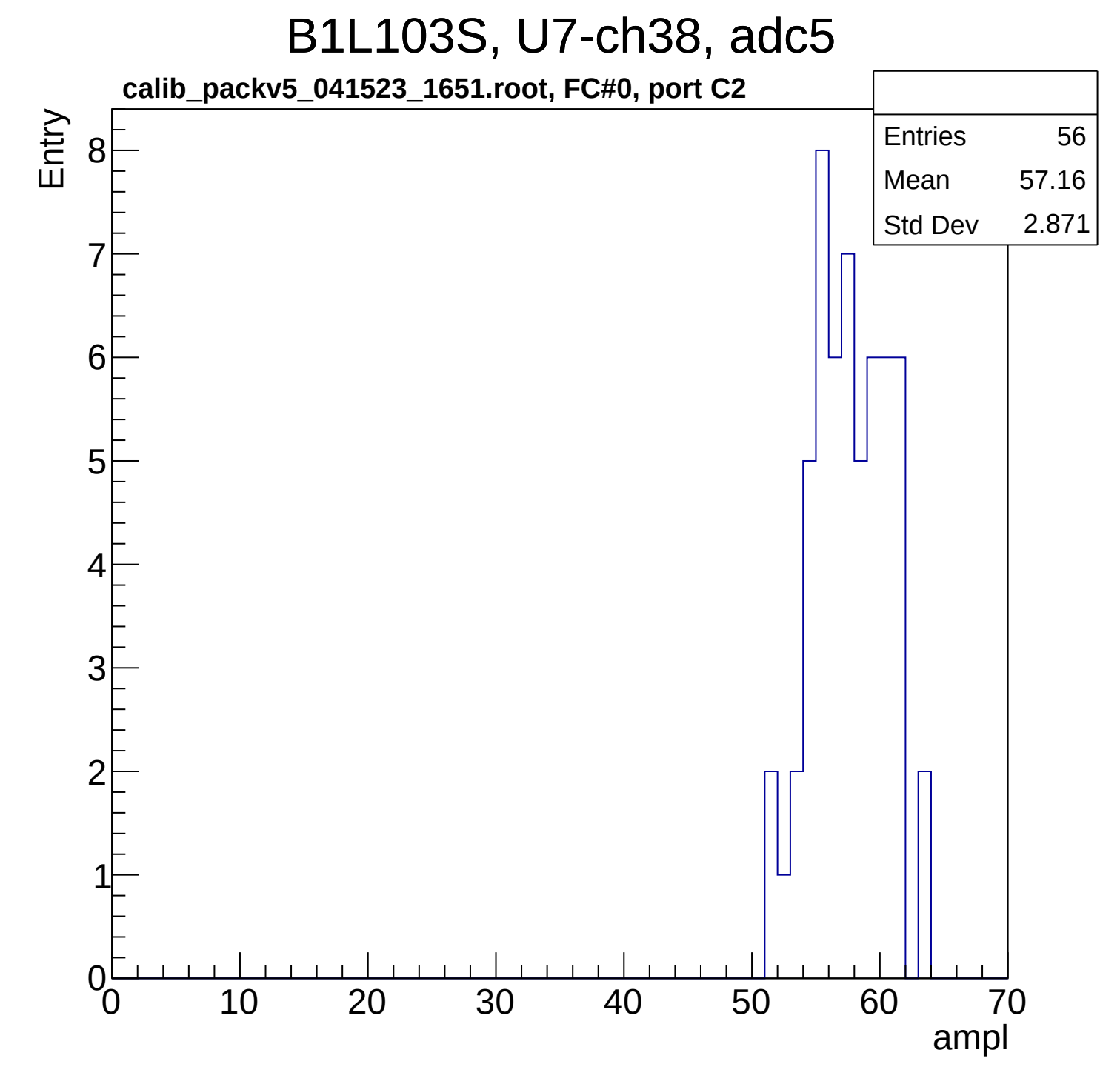
B1L103S, U7-ch38, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 57.16
Std Dev 2.871
Entry
ampl
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4
5
6
7
8
0
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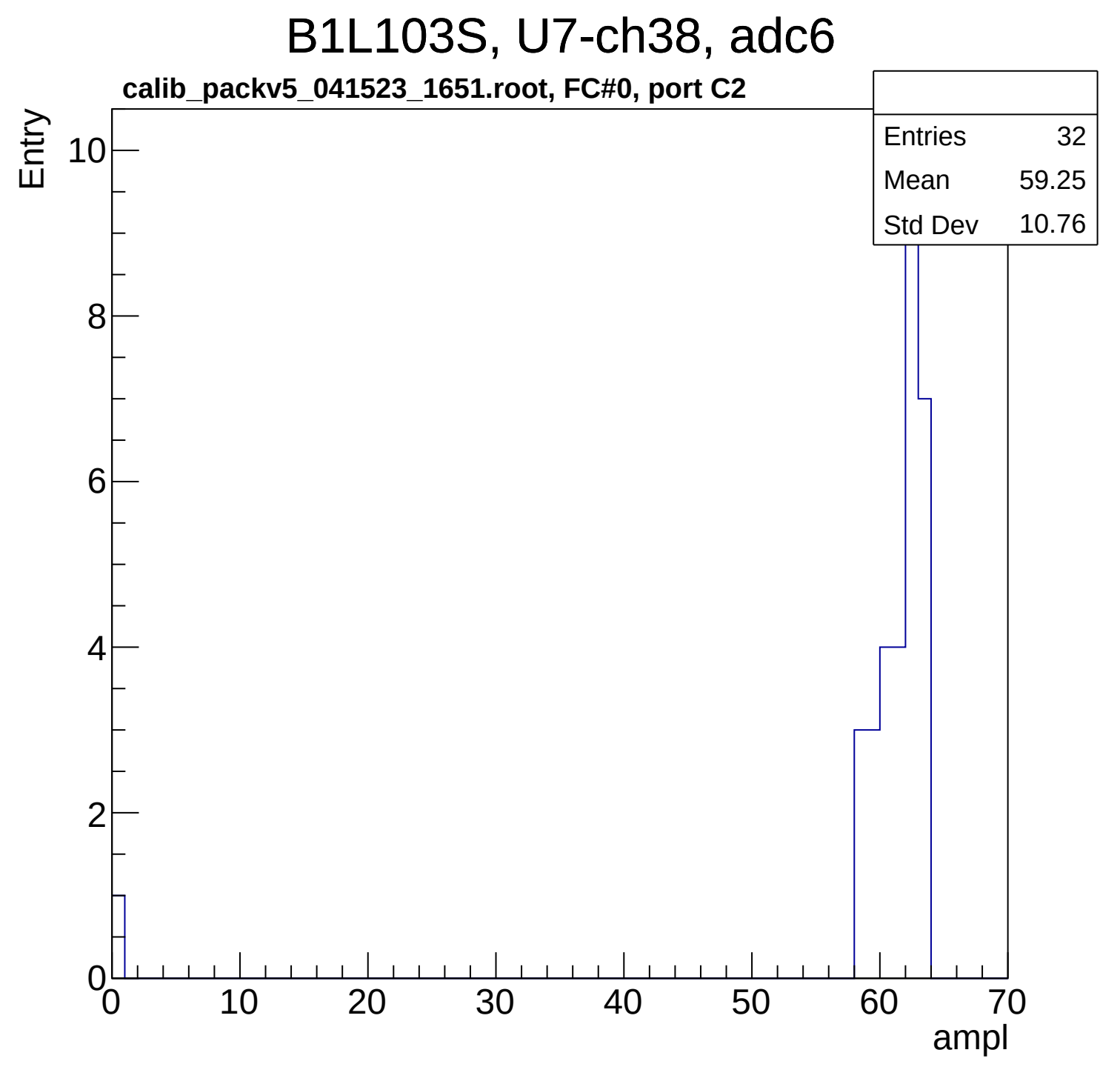
B1L103S, U7-ch38, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 32
Mean 59.25
Std Dev 10.76
Entry
ampl
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8
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0
10
20
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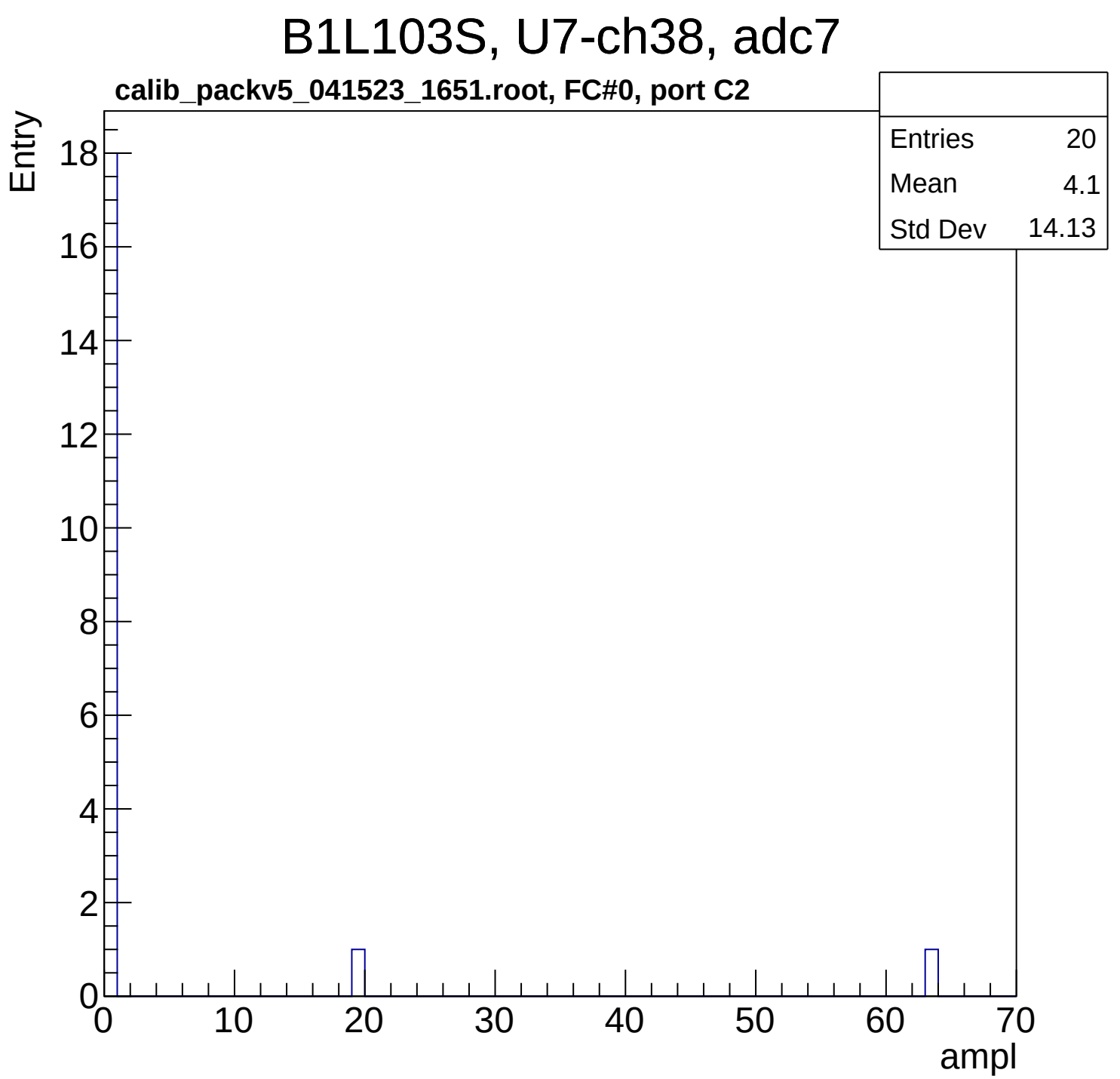
40
50
60
70


B1L103S, U7-ch38, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 4.1
Std Dev 14.13
Entry
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6
8
10
12
14
16
18
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10
20
30
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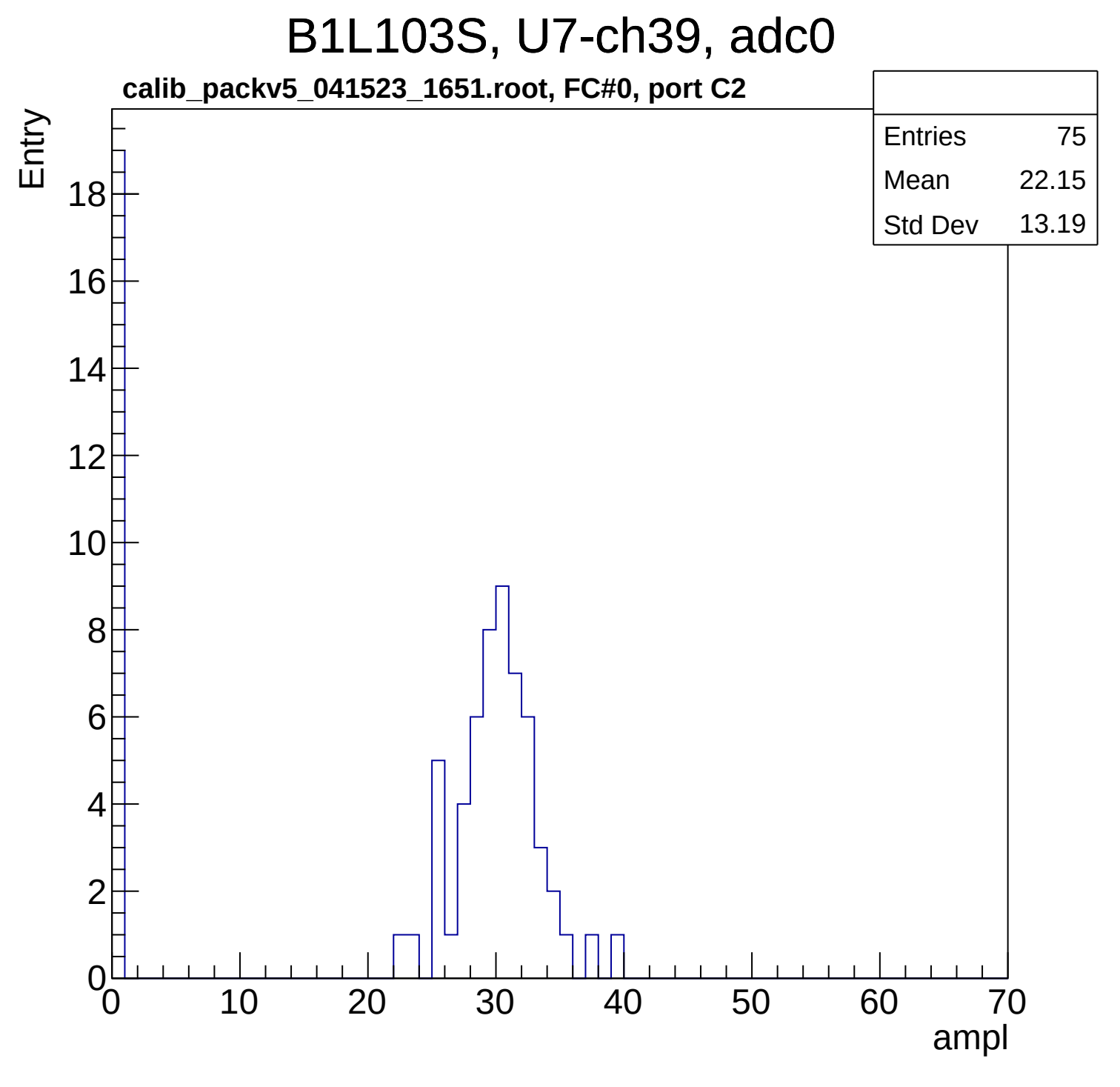
50
60
70
ampl


B1L103S, U7-ch39, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 22.15
Std Dev 13.19
Entry
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6
8
10
12
14
16
18
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10
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30
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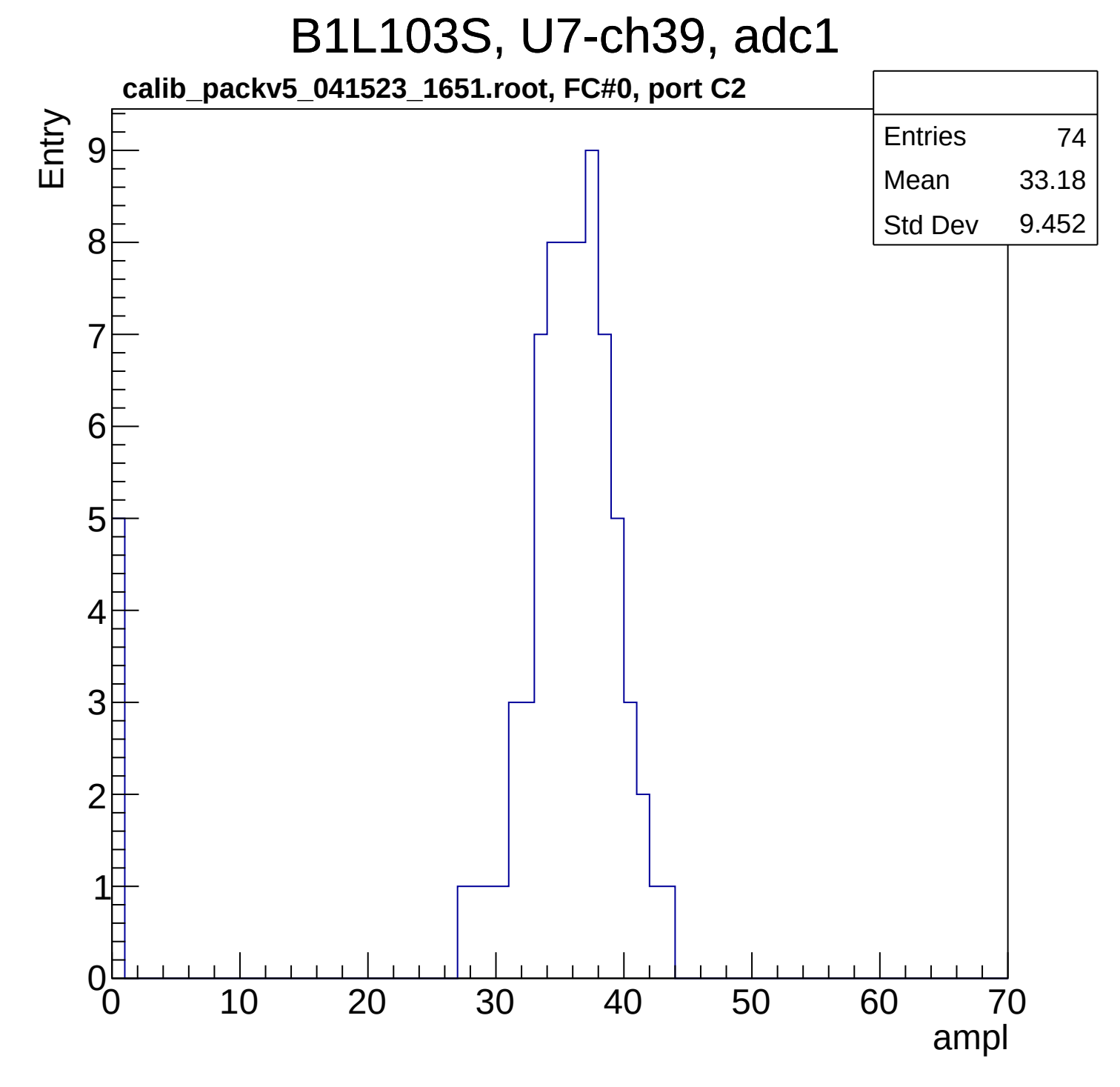
50
60
70
ampl


B1L103S, U7-ch39, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 33.18
Std Dev 9.452
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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60
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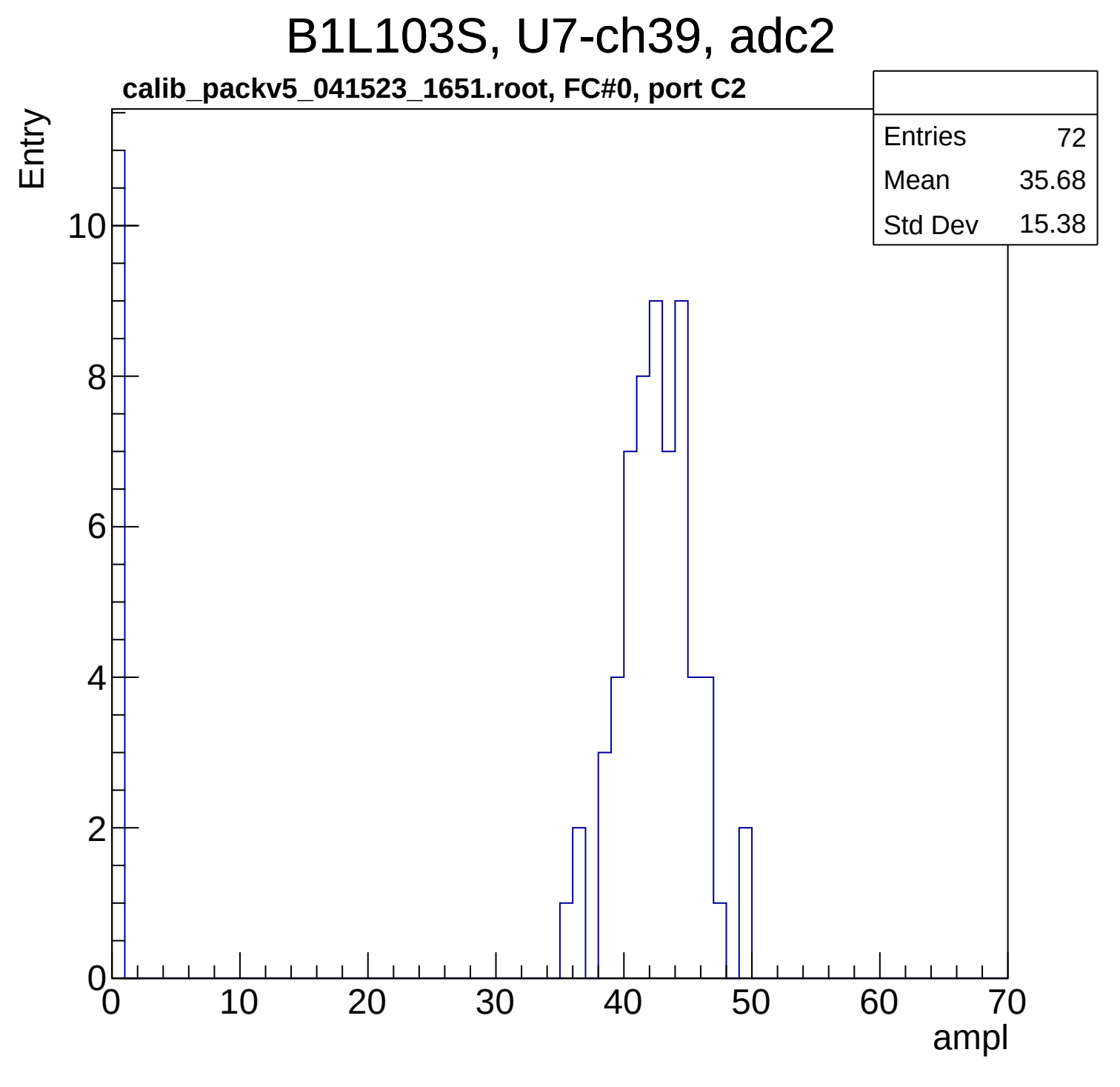
B1L103S, U7-ch39, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 35.68
Std Dev 15.38
Entry
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10
0
10
20
30
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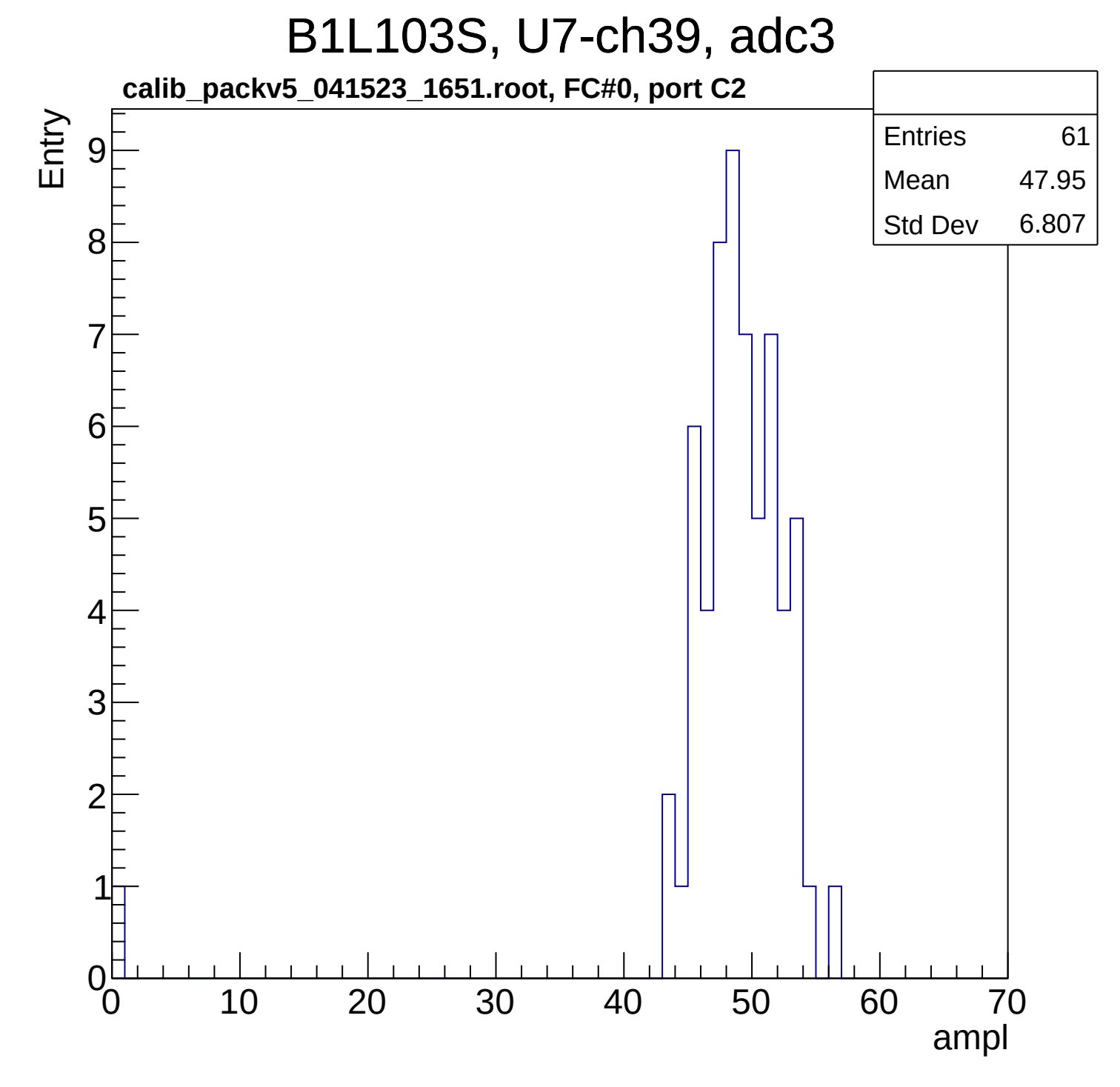
50
60
70
ampl


B1L103S, U7-ch39, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 47.95
Std Dev 6.807
Entry
ampl
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3
4
5
6
7
8
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0
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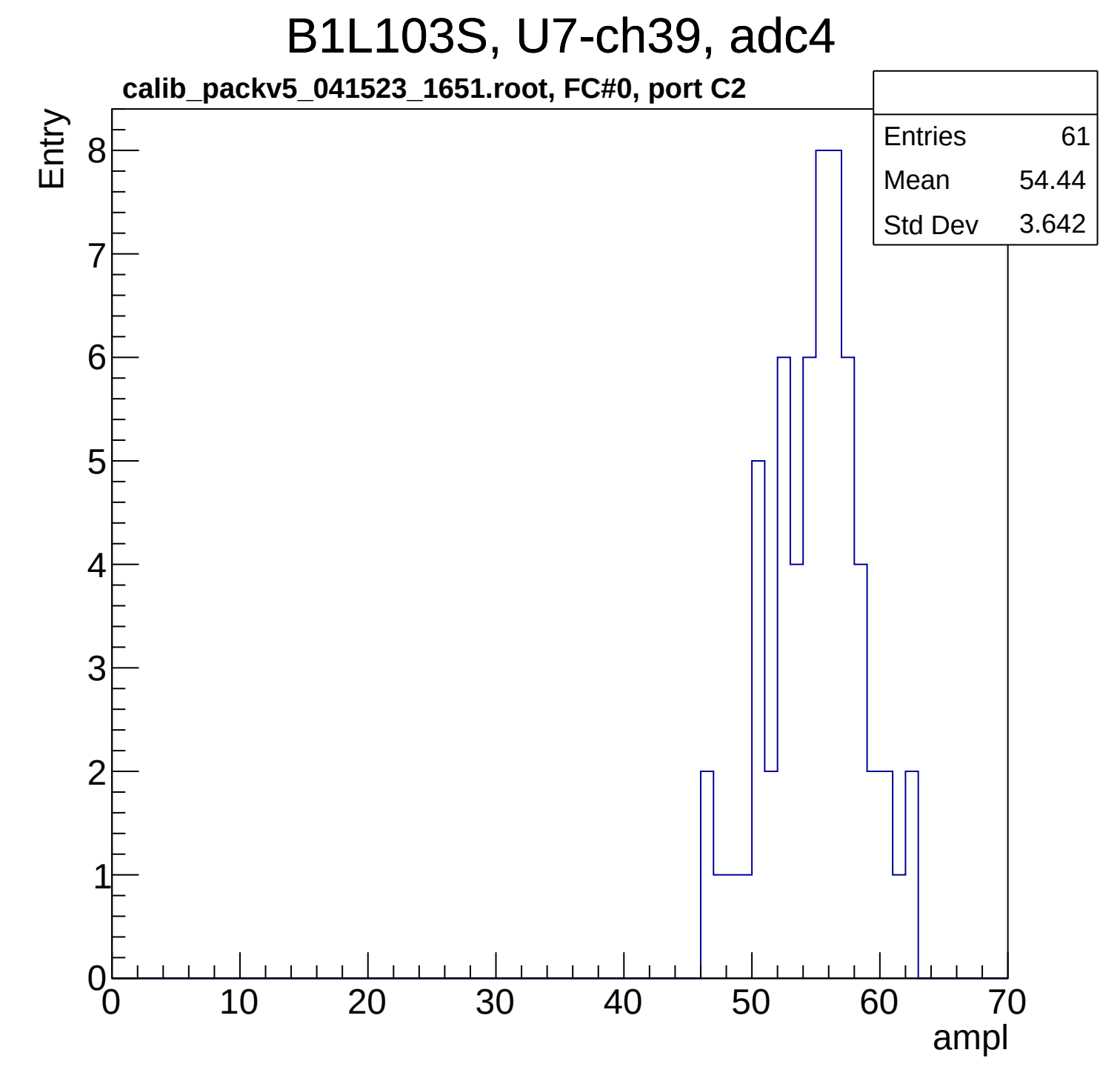
B1L103S, U7-ch39, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 54.44
Std Dev 3.642
Entry
ampl
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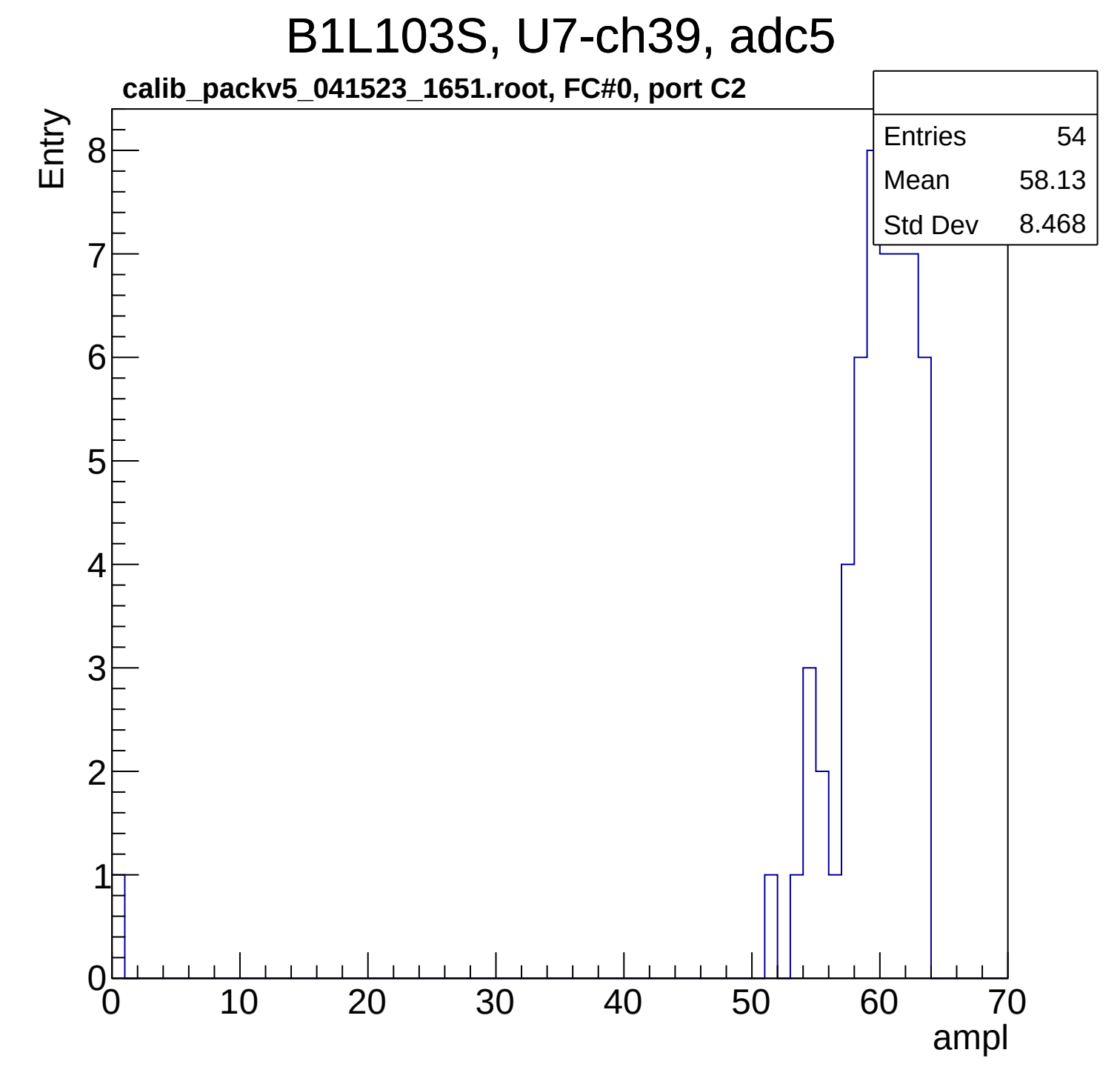
B1L103S, U7-ch39, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 58.13
Std Dev 8.468
Entry
ampl
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4
5
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7
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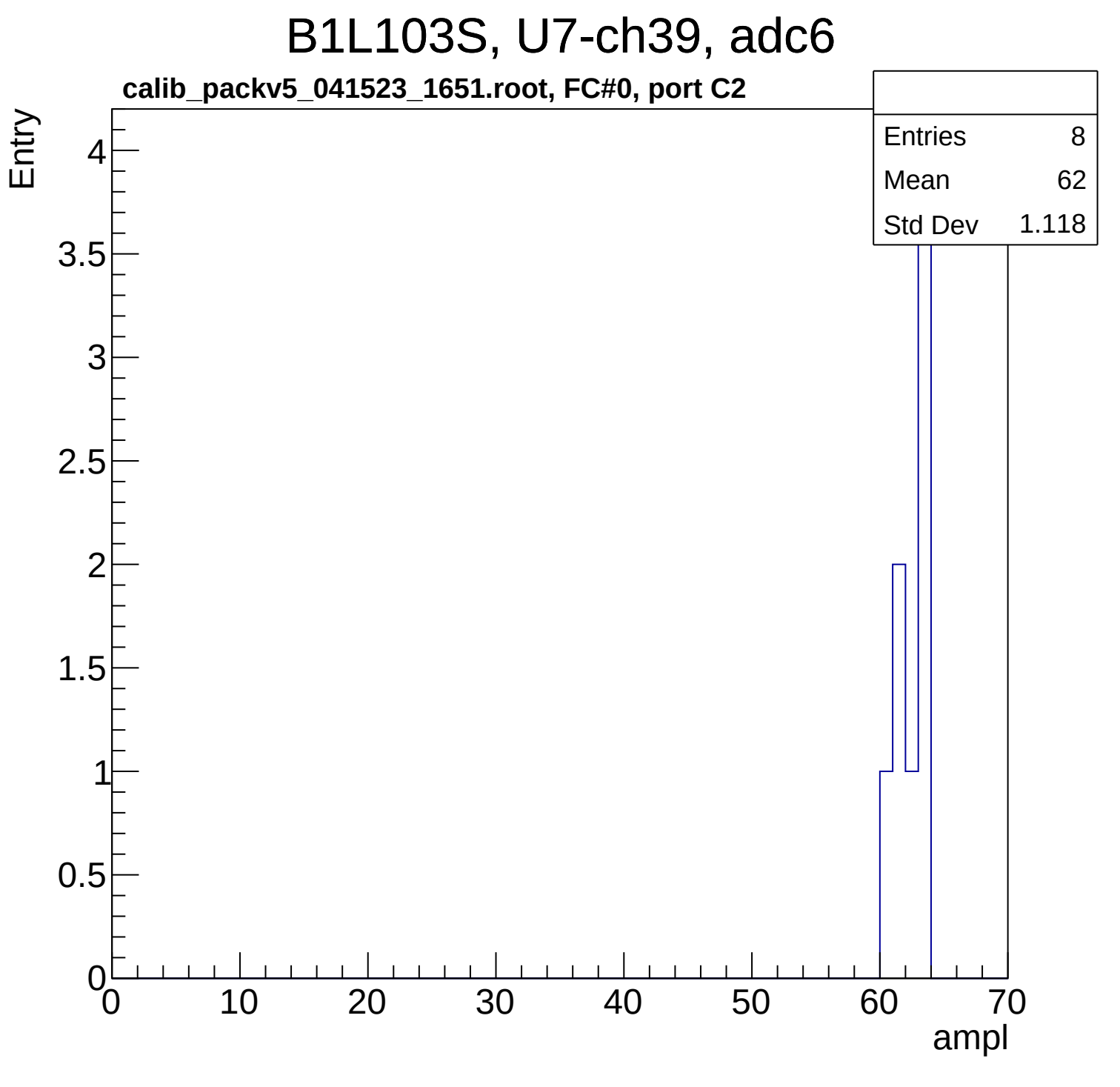
60
70


B1L103S, U7-ch39, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 62
Std Dev 1.118
Entry
ampl
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0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
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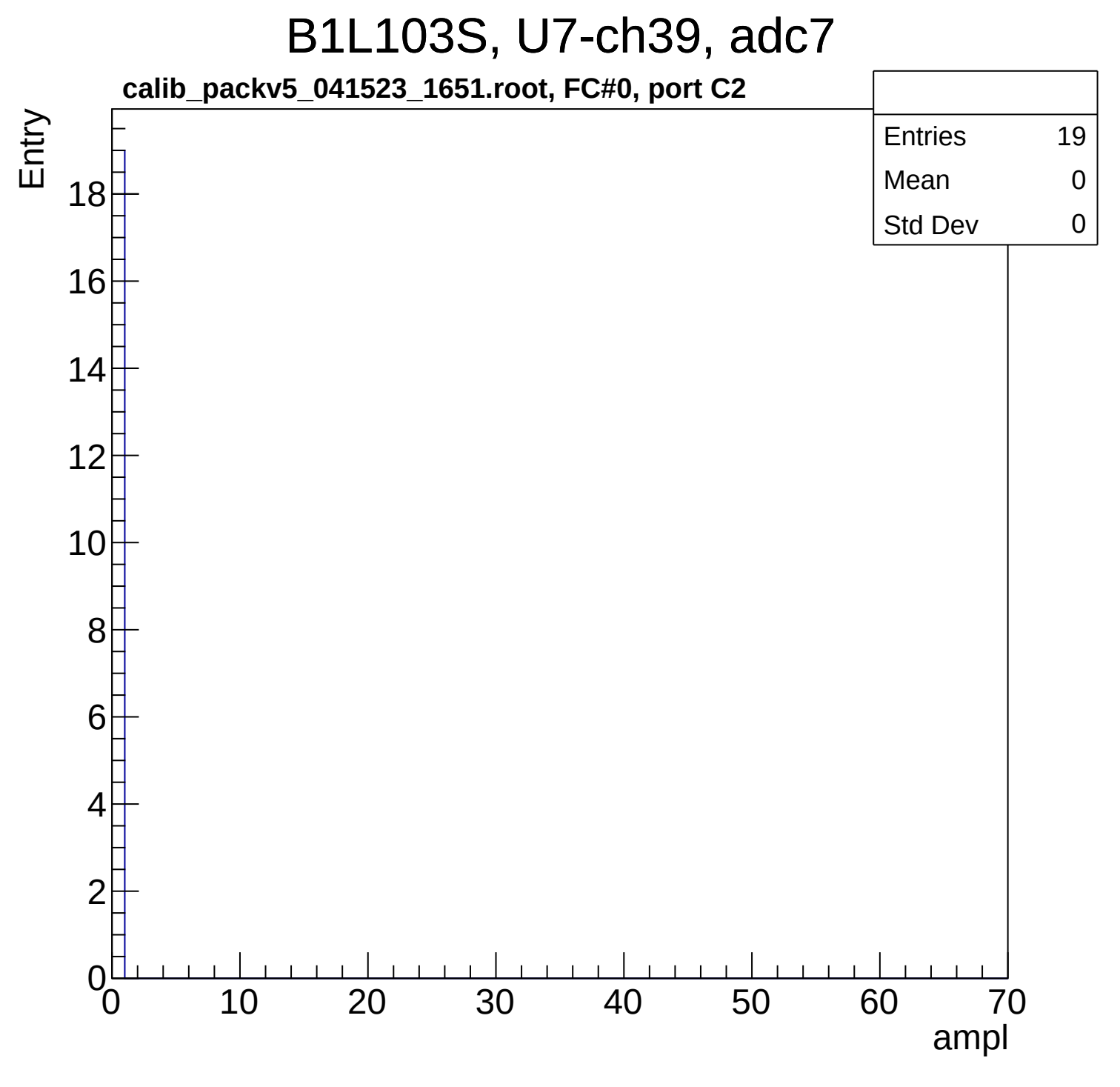
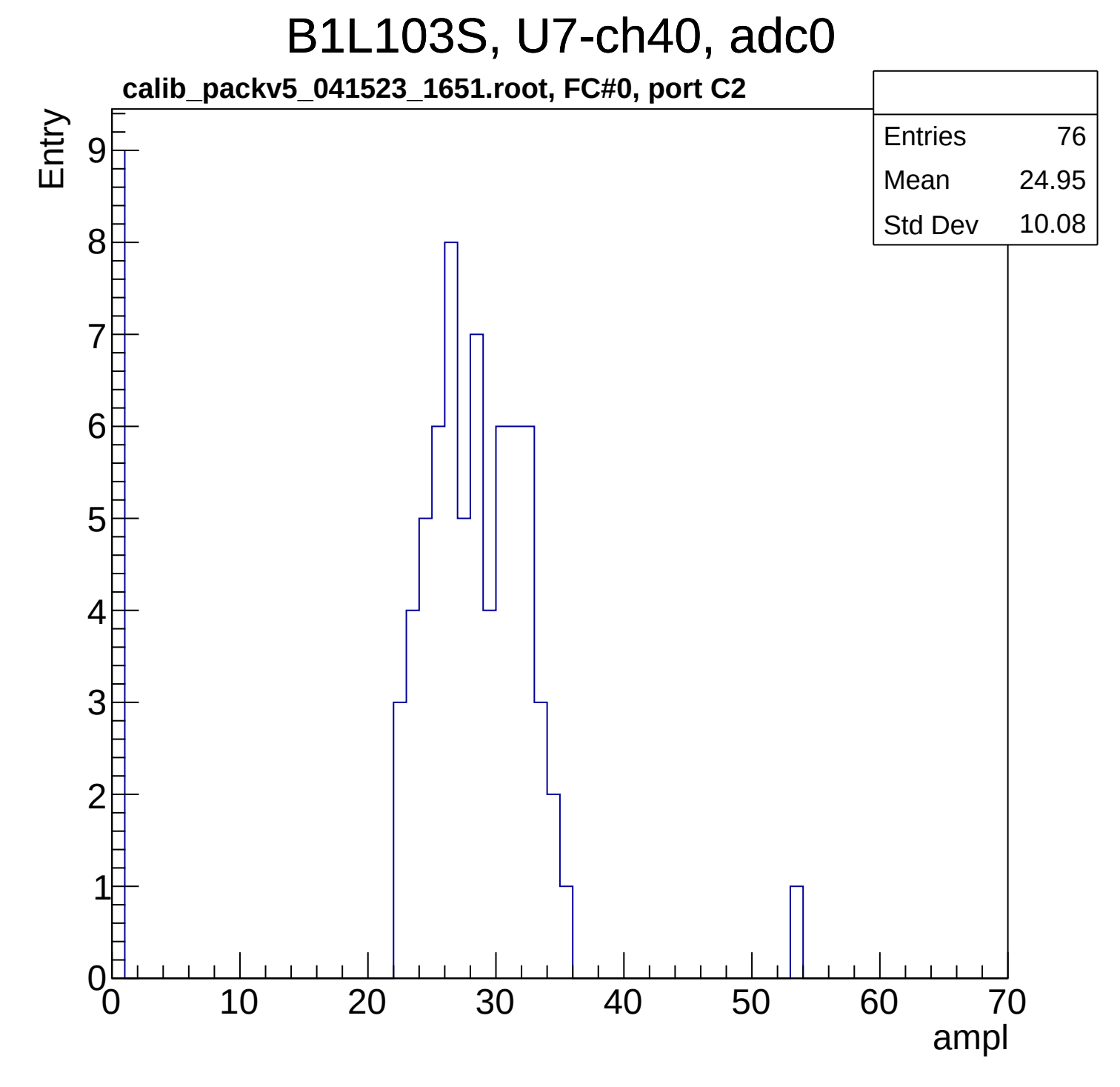

B1L103S, U7-ch39, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch40, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 24.95
Std Dev 10.08
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
30
40
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60
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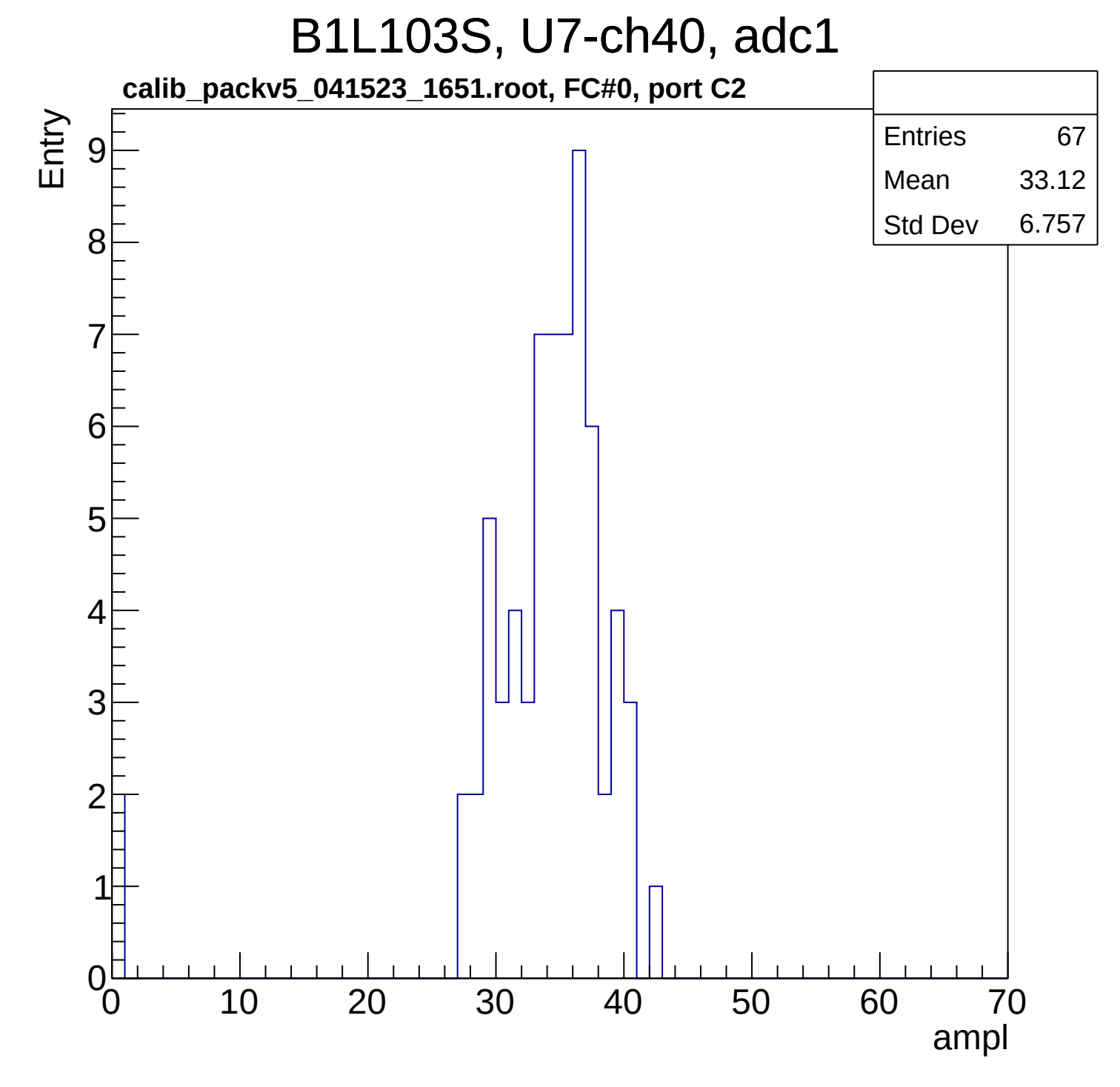
B1L103S, U7-ch40, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 33.12
Std Dev 6.757
Entry
ampl
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2
3
4
5
6
7
8
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0
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40
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60
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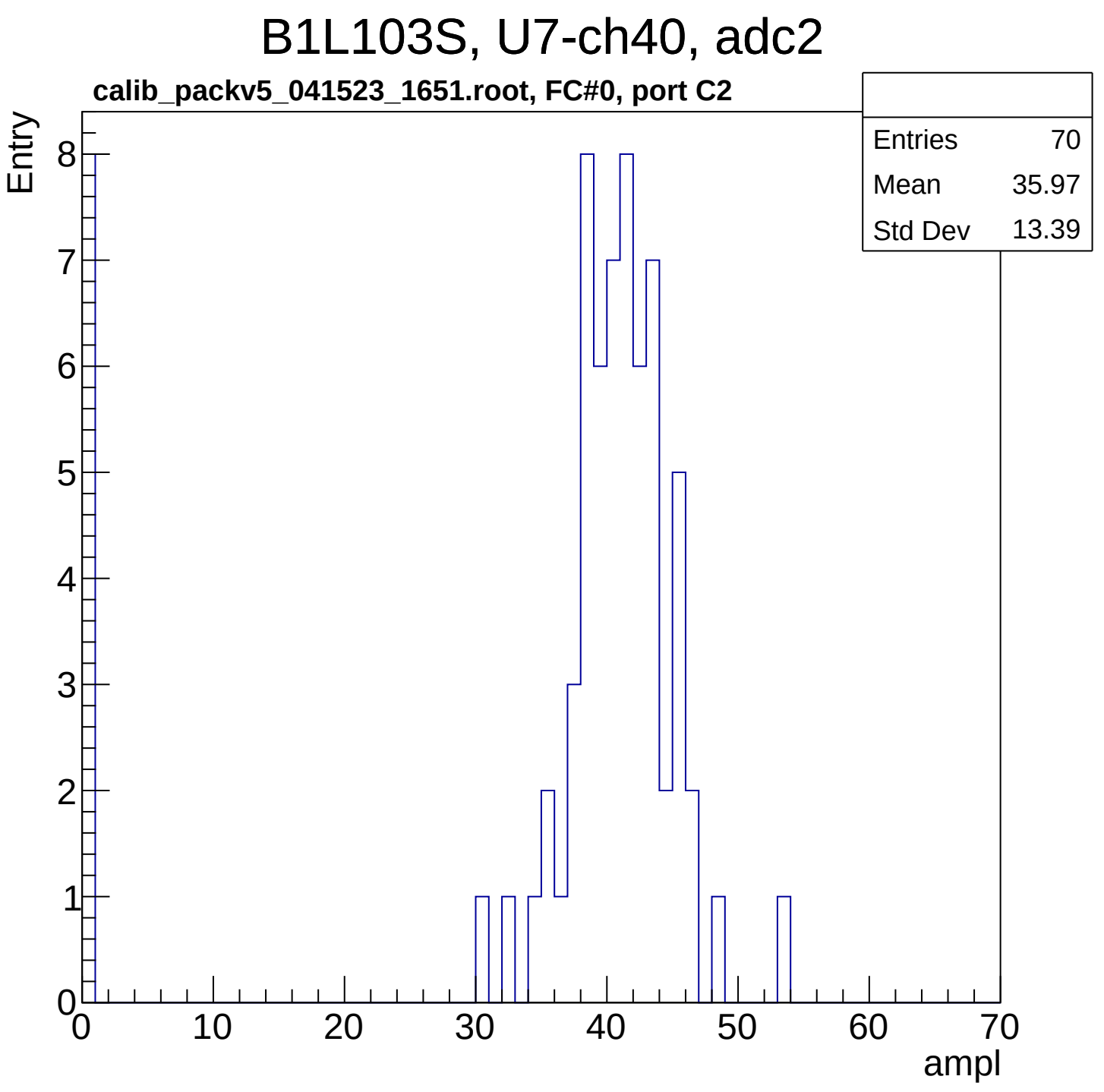
B1L103S, U7-ch40, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 35.97
Std Dev 13.39
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
30
40
50
60
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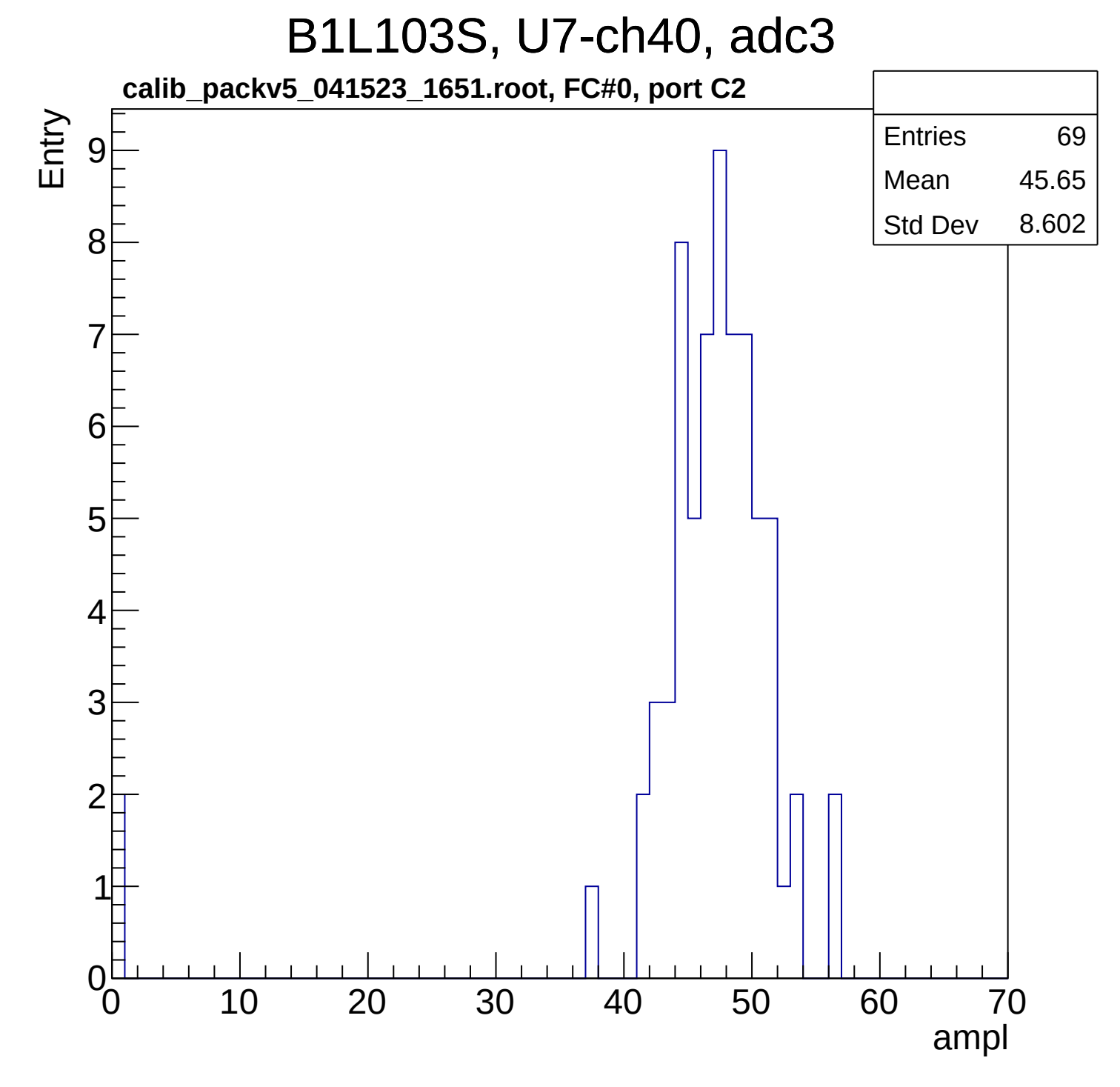
B1L103S, U7-ch40, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 45.65
Std Dev 8.602
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
30
40
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60
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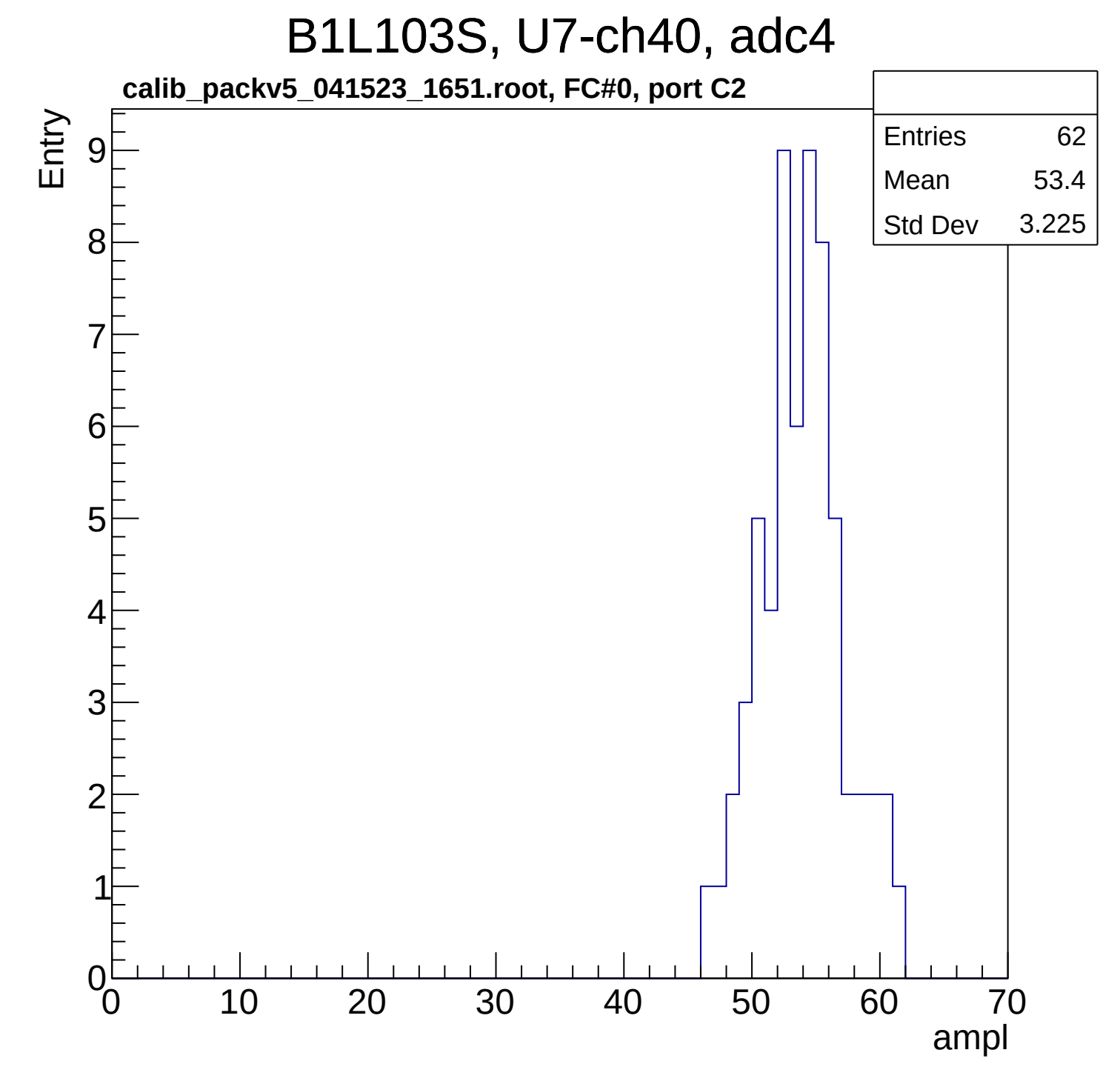
B1L103S, U7-ch40, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 53.4
Std Dev 3.225
Entry
ampl
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2
3
4
5
6
7
8
9
0
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60
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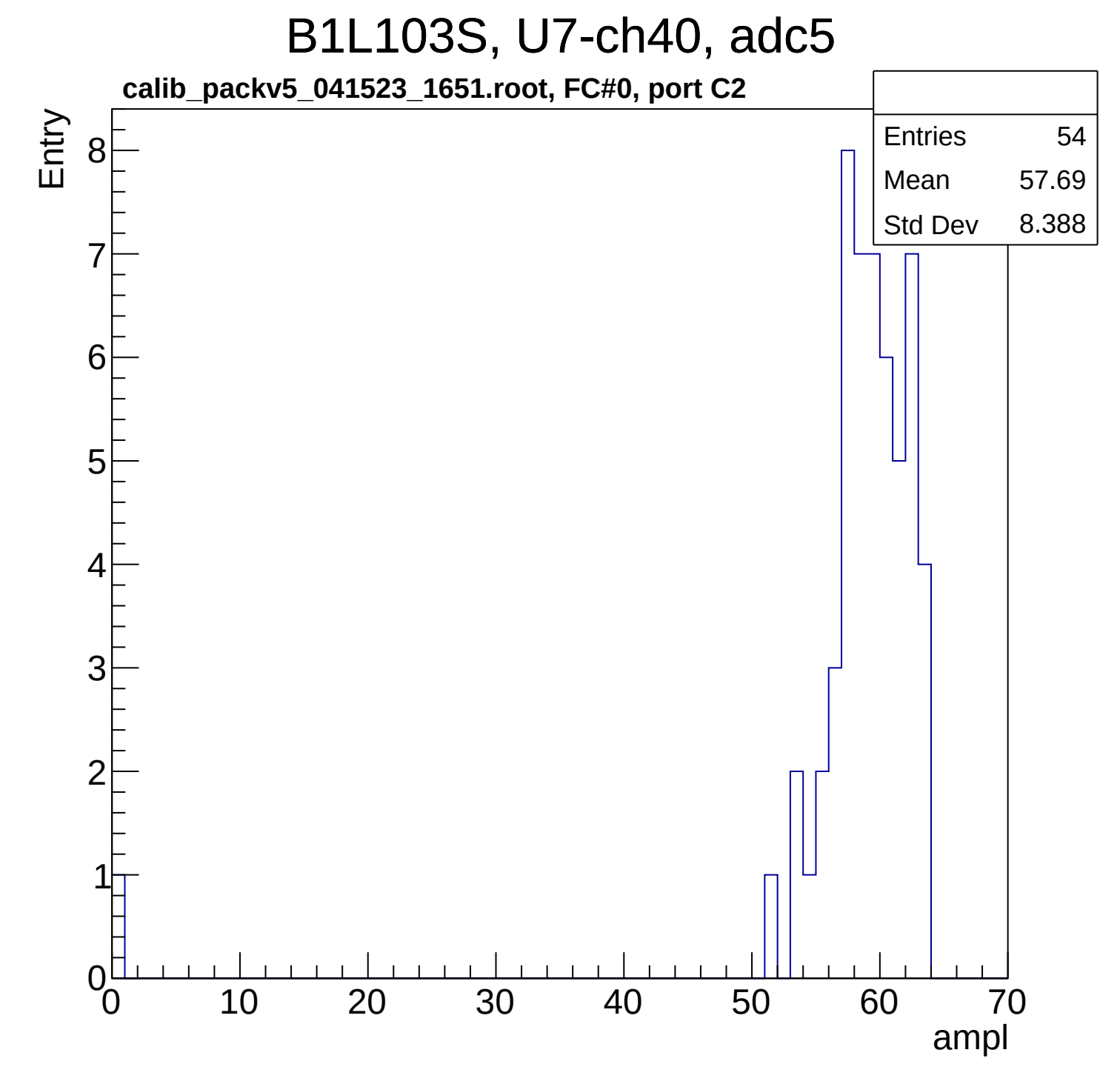
B1L103S, U7-ch40, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 57.69
Std Dev 8.388
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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40
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60
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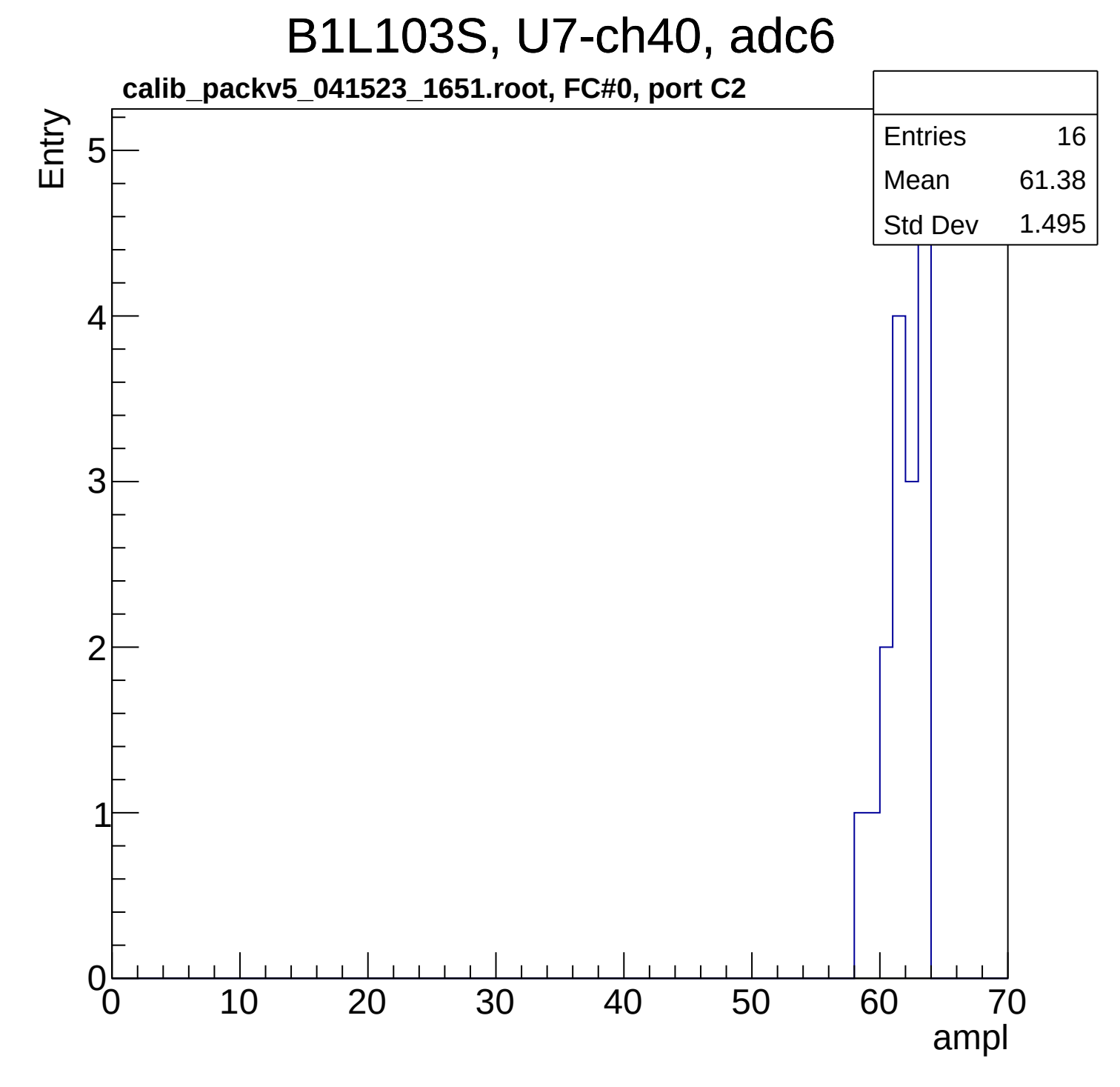
B1L103S, U7-ch40, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 16
Mean 61.38
Std Dev 1.495
Entry
ampl
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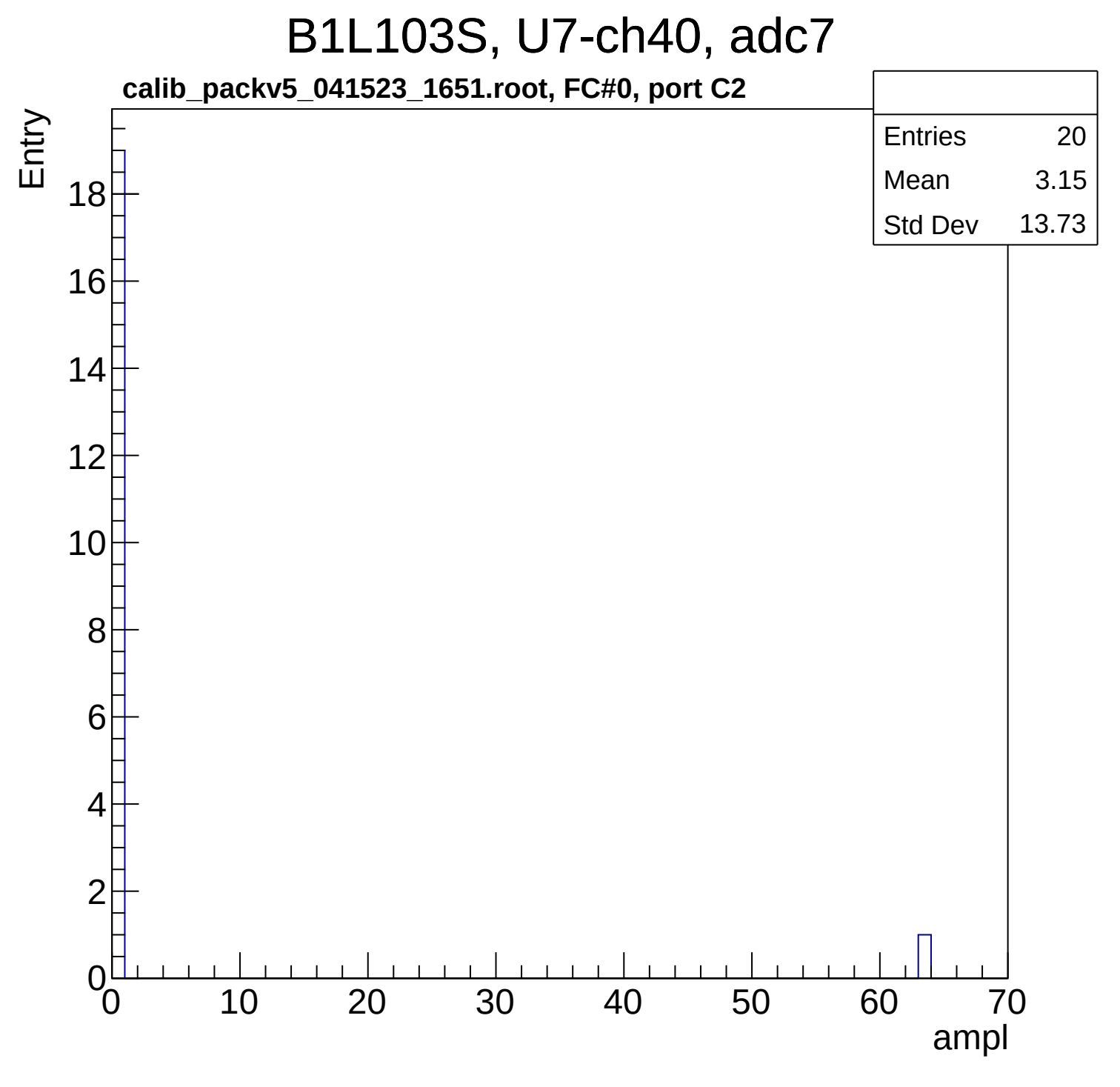
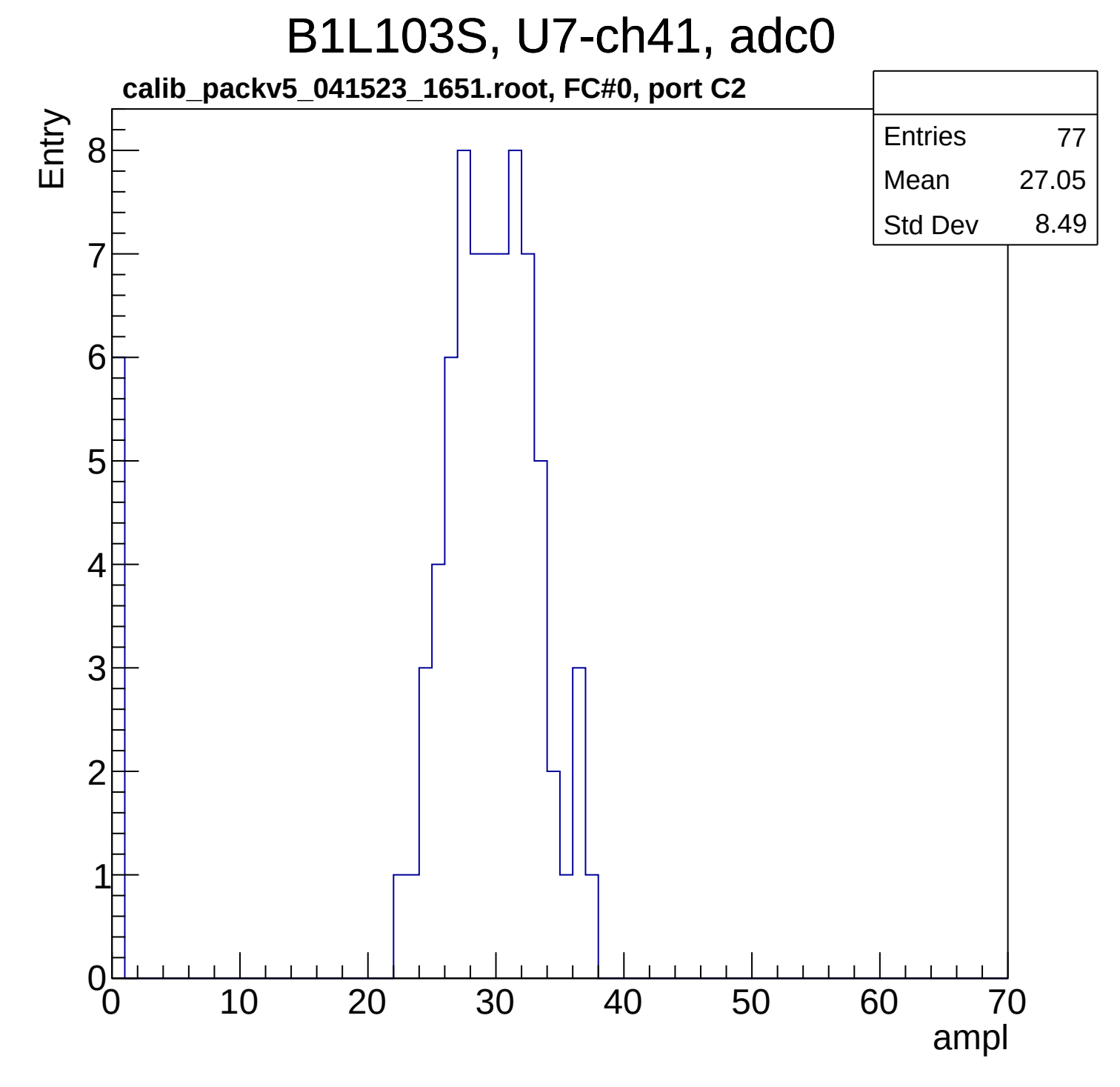
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U7-ch40, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch41, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 27.05
Std Dev 8.49
Entry
ampl
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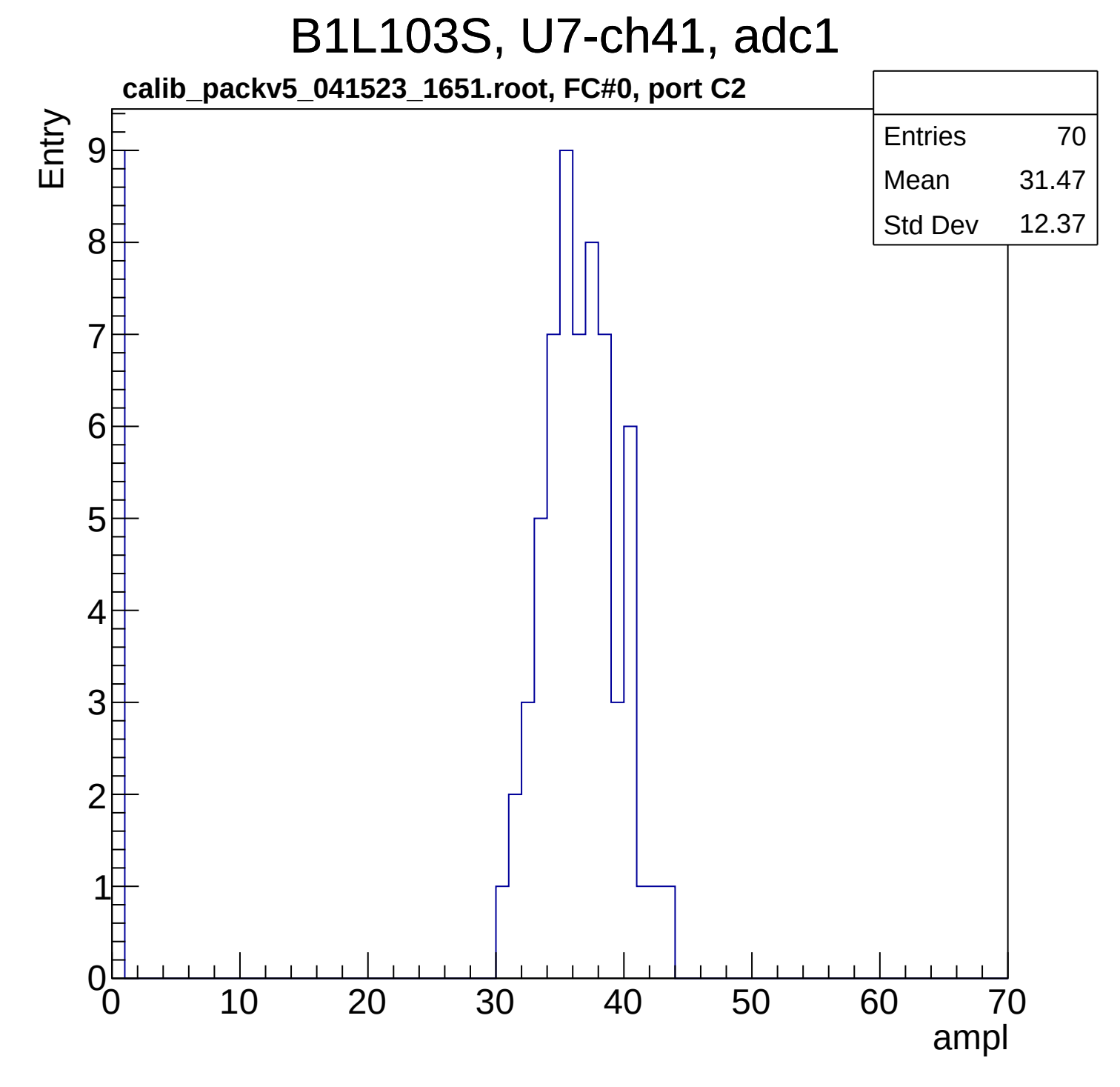
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch41, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 31.47
Std Dev 12.37
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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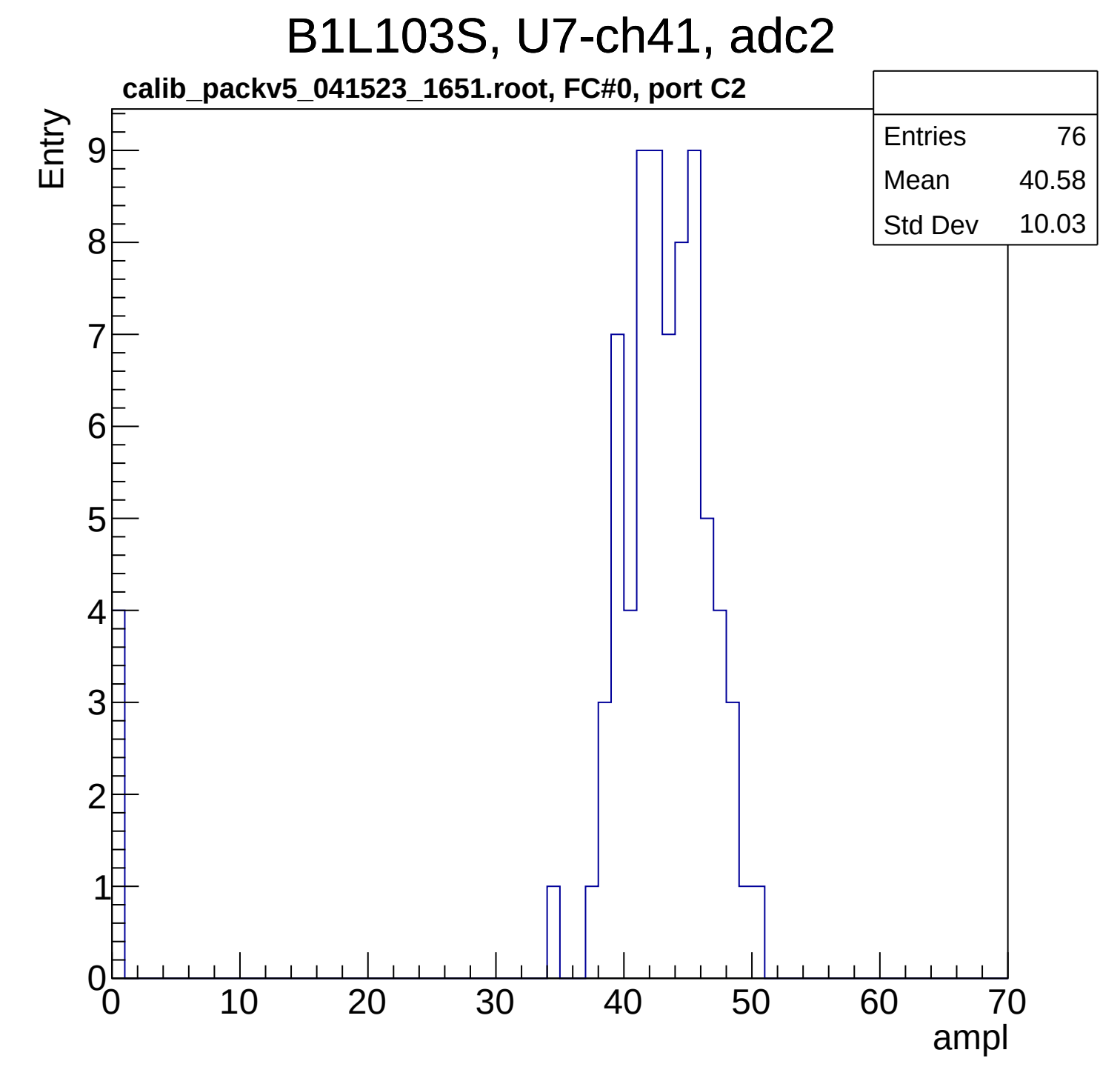
B1L103S, U7-ch41, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 40.58
Std Dev 10.03
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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40
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60
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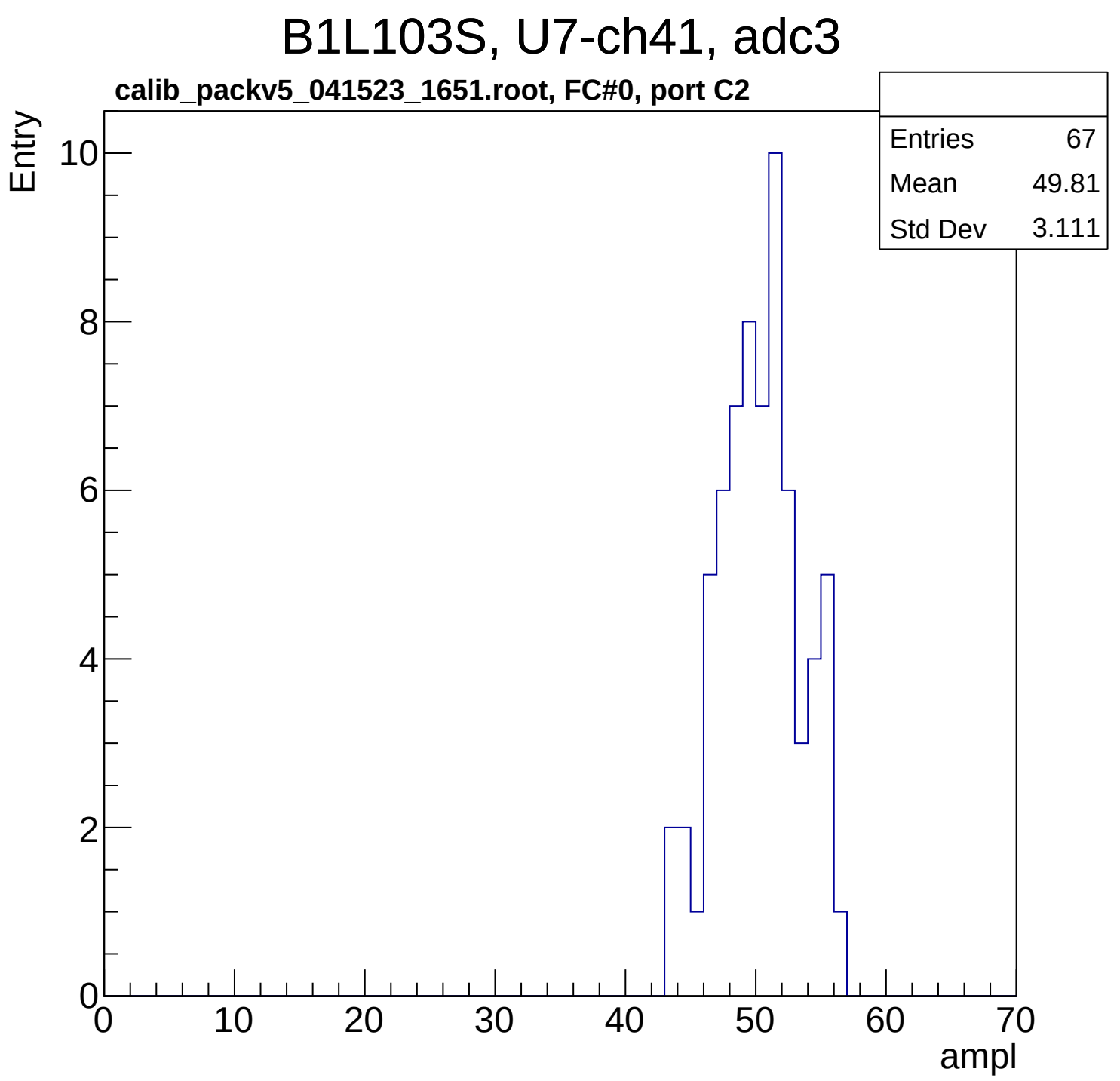
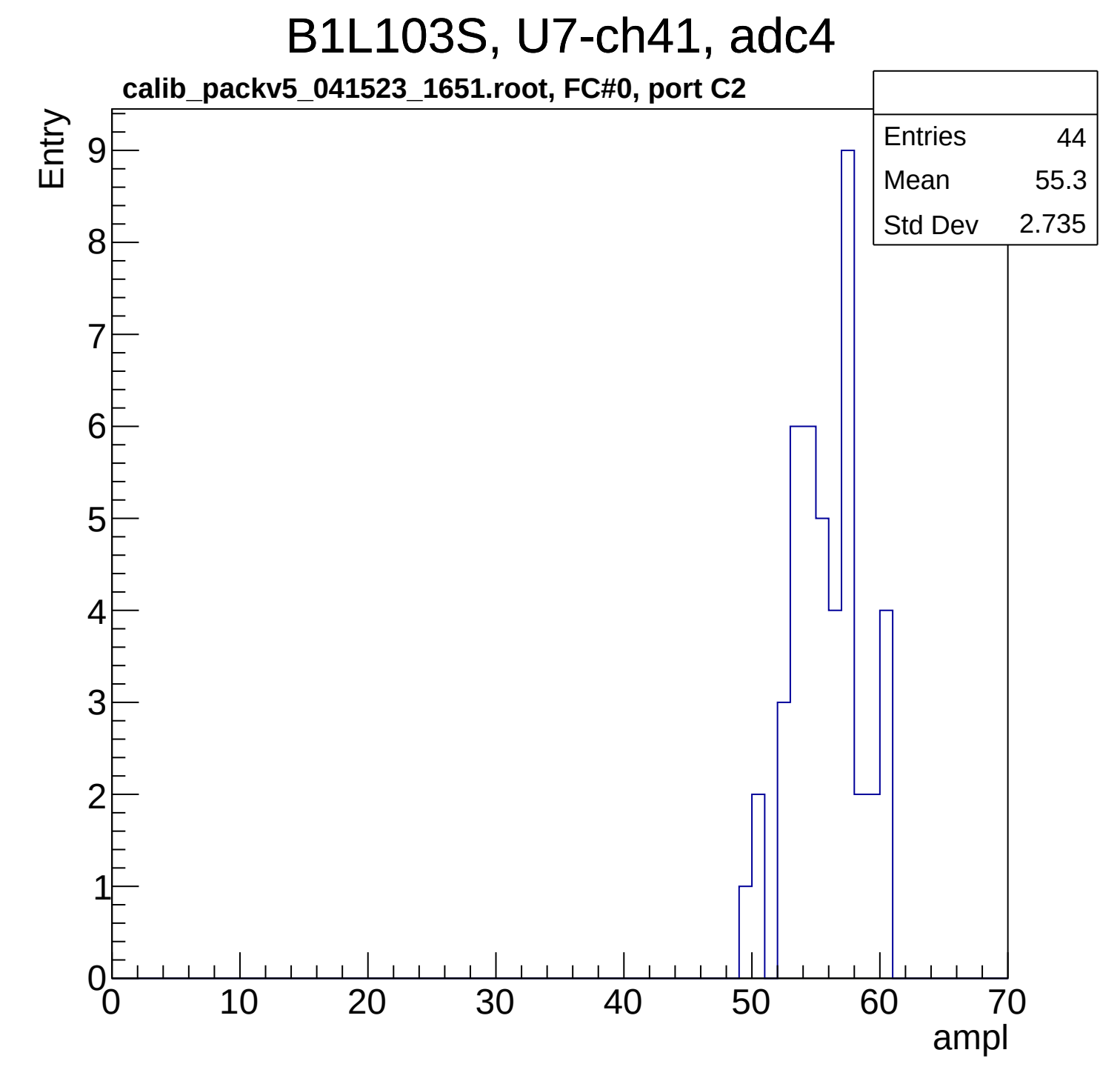

B1L103S, U7-ch41, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 49.81
Std Dev 3.111
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U7-ch41, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 55.3
Std Dev 2.735
Entry
ampl
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2
3
4
5
6
7
8
9
0
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60
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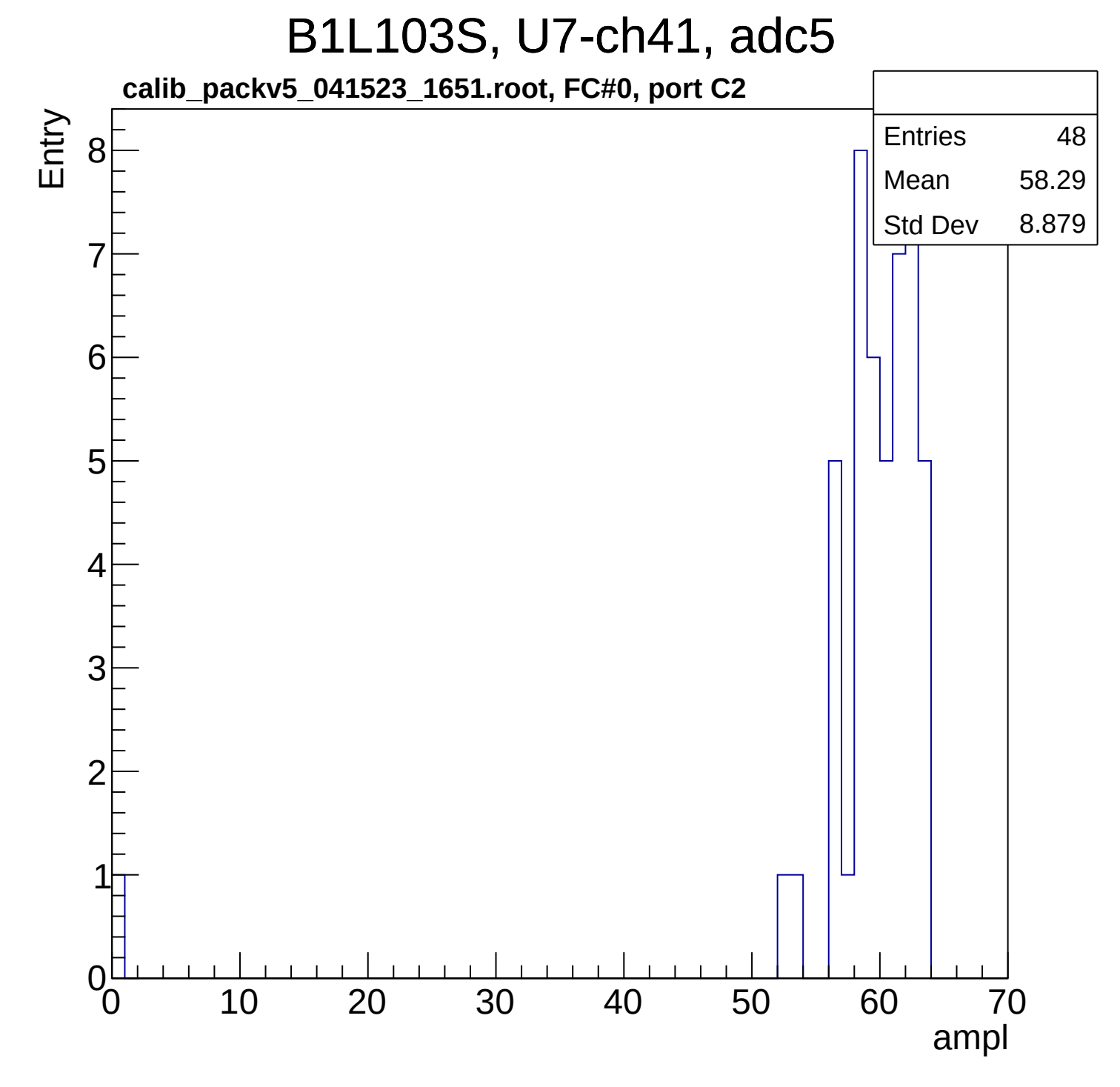
B1L103S, U7-ch41, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 58.29
Std Dev 8.879
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
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40
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60
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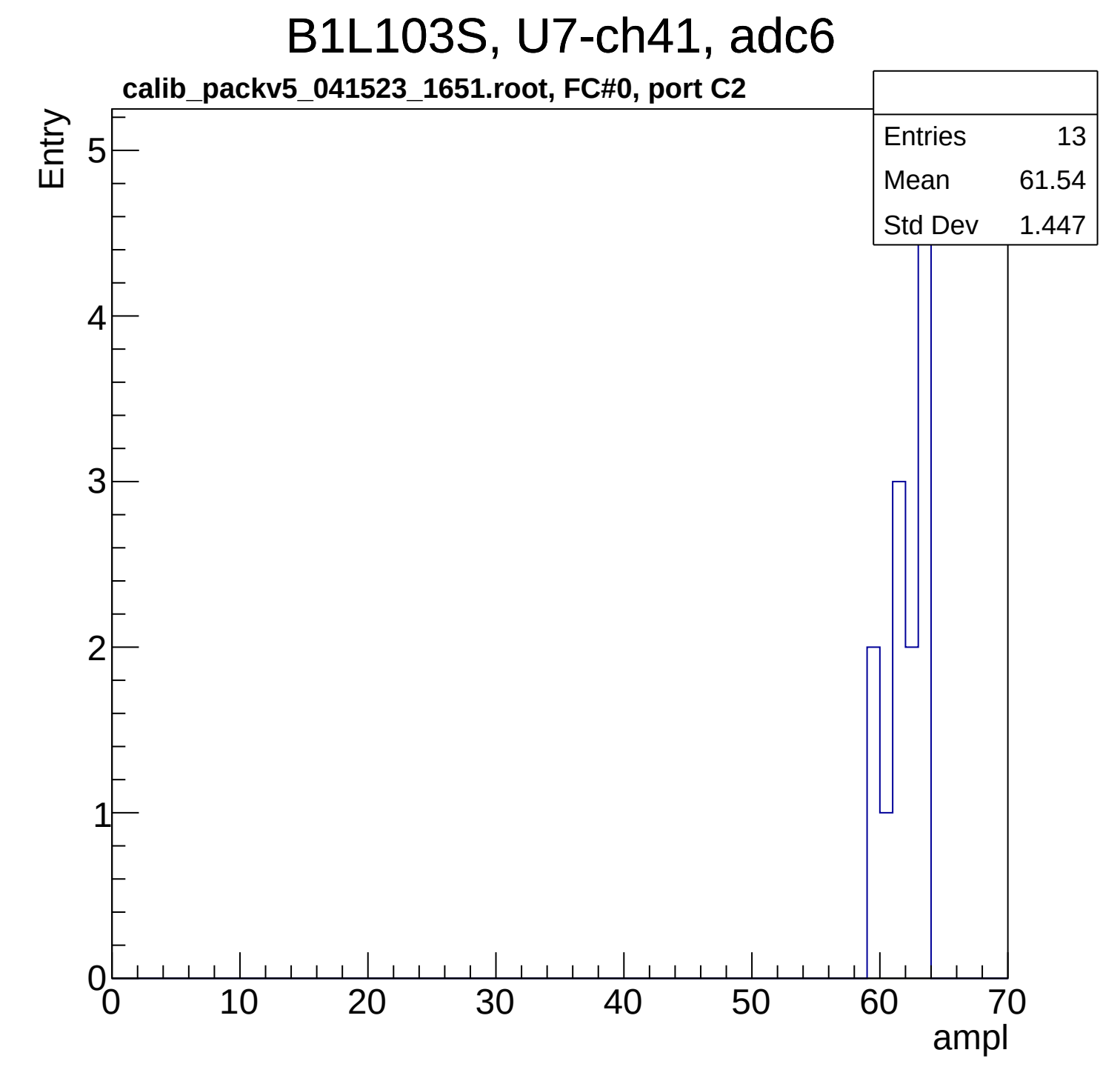
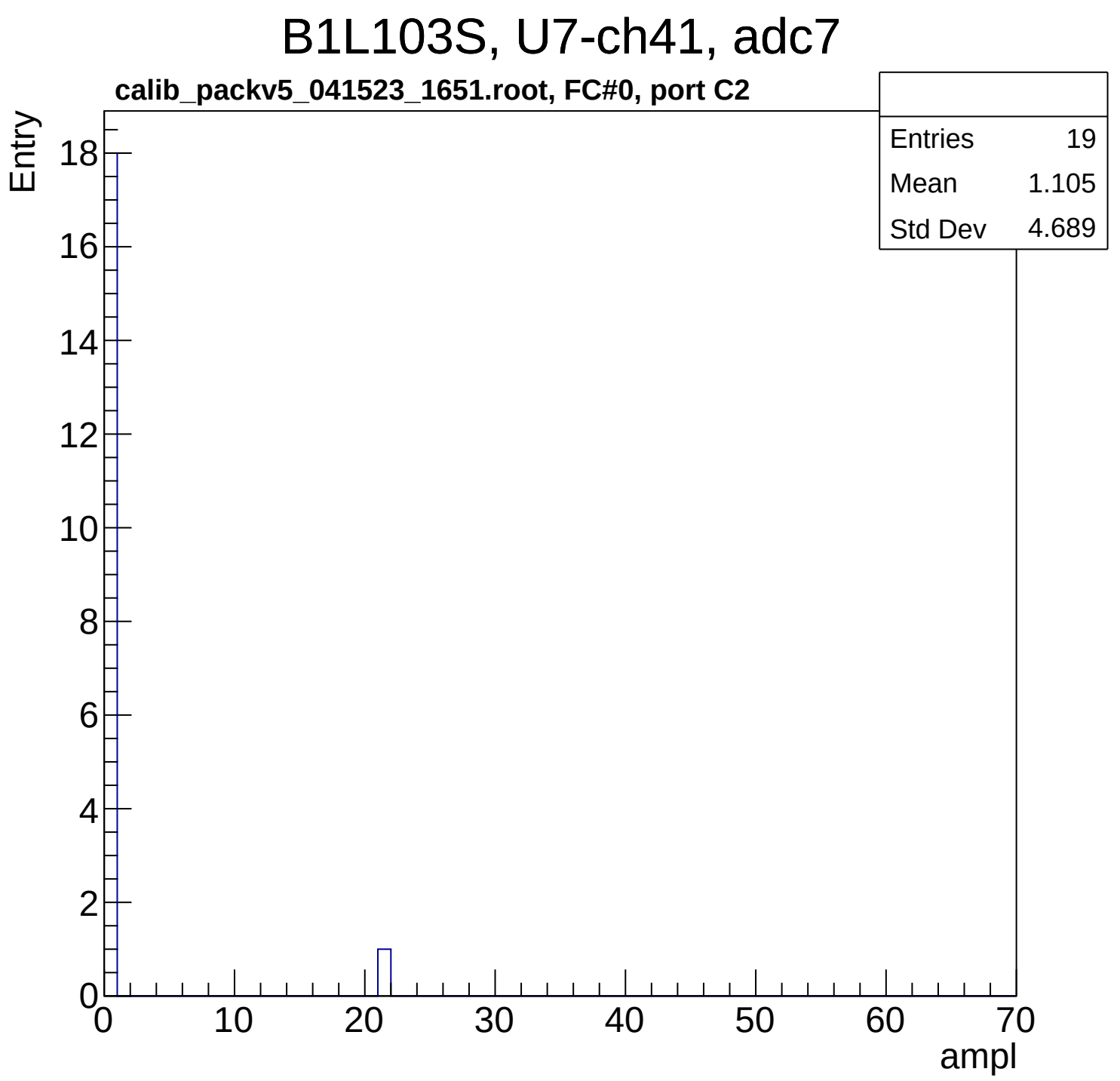

B1L103S, U7-ch41, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 13
Mean 61.54
Std Dev 1.447
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U7-ch41, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.105
Std Dev 4.689
Entry
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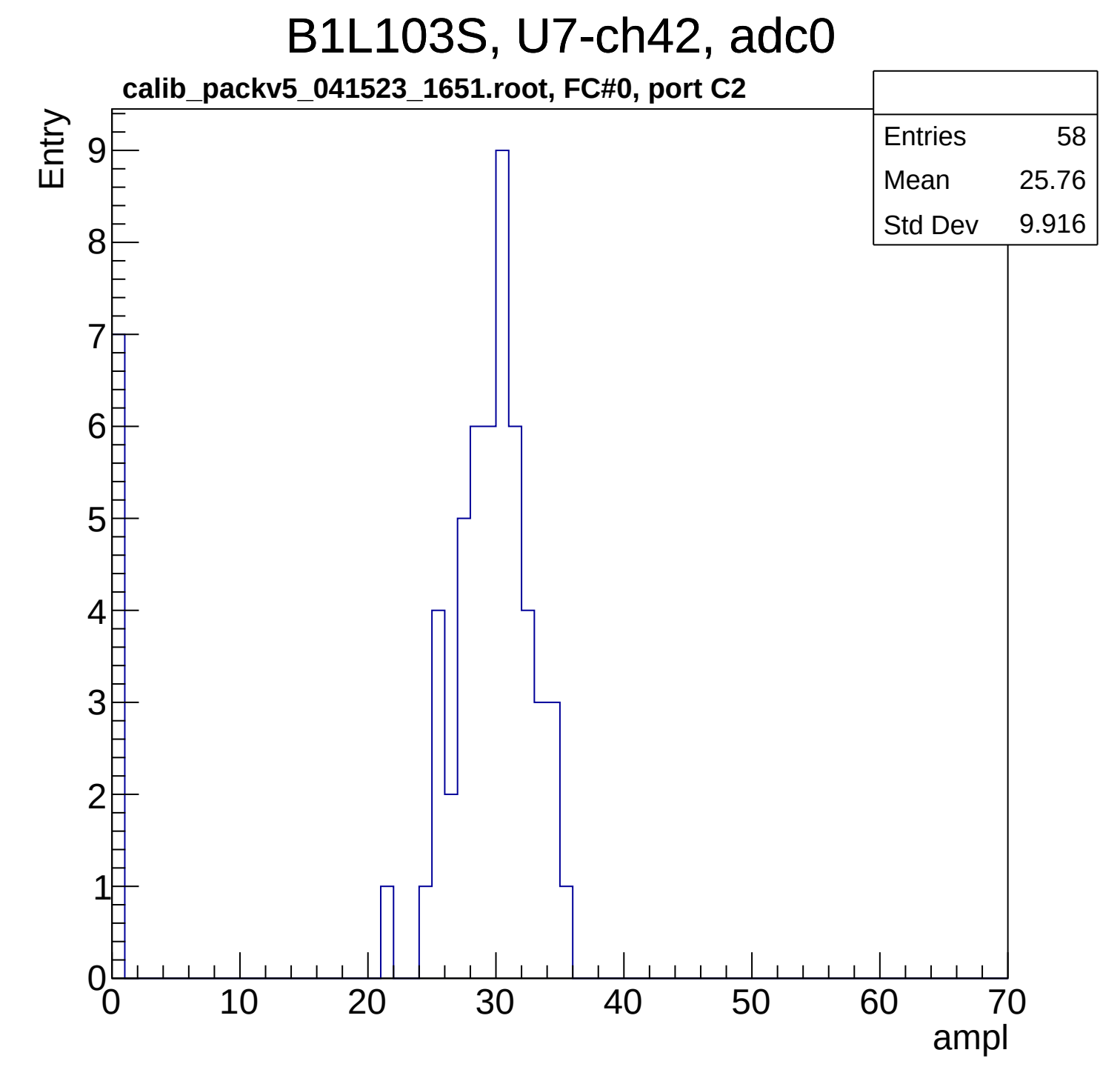
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch42, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 25.76
Std Dev 9.916
Entry
ampl
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2
3
4
5
6
7
8
9
0
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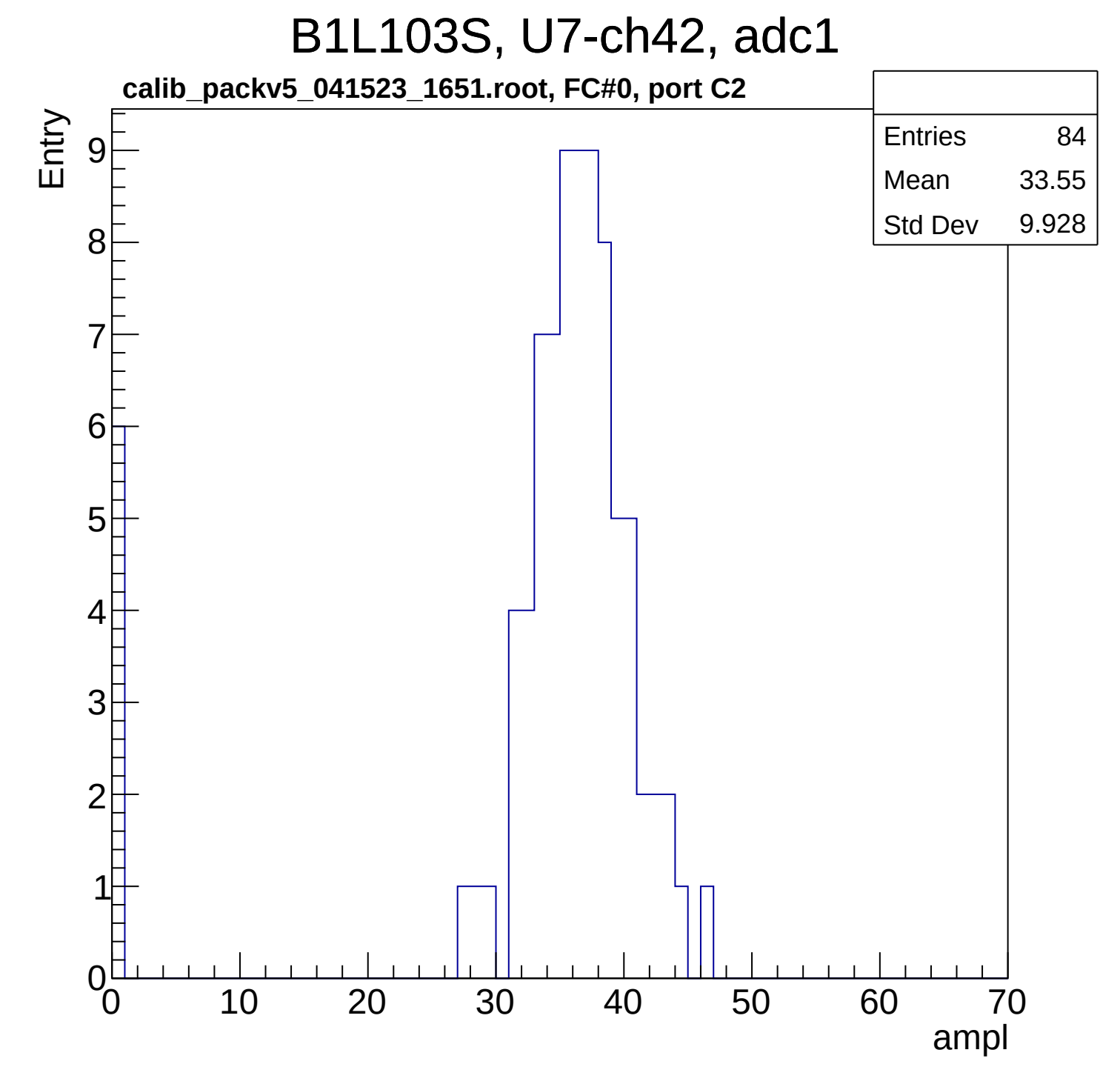
20
30
40
50
60
70


B1L103S, U7-ch42, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 33.55
Std Dev 9.928
Entry
ampl
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3
4
5
6
7
8
9
0
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60
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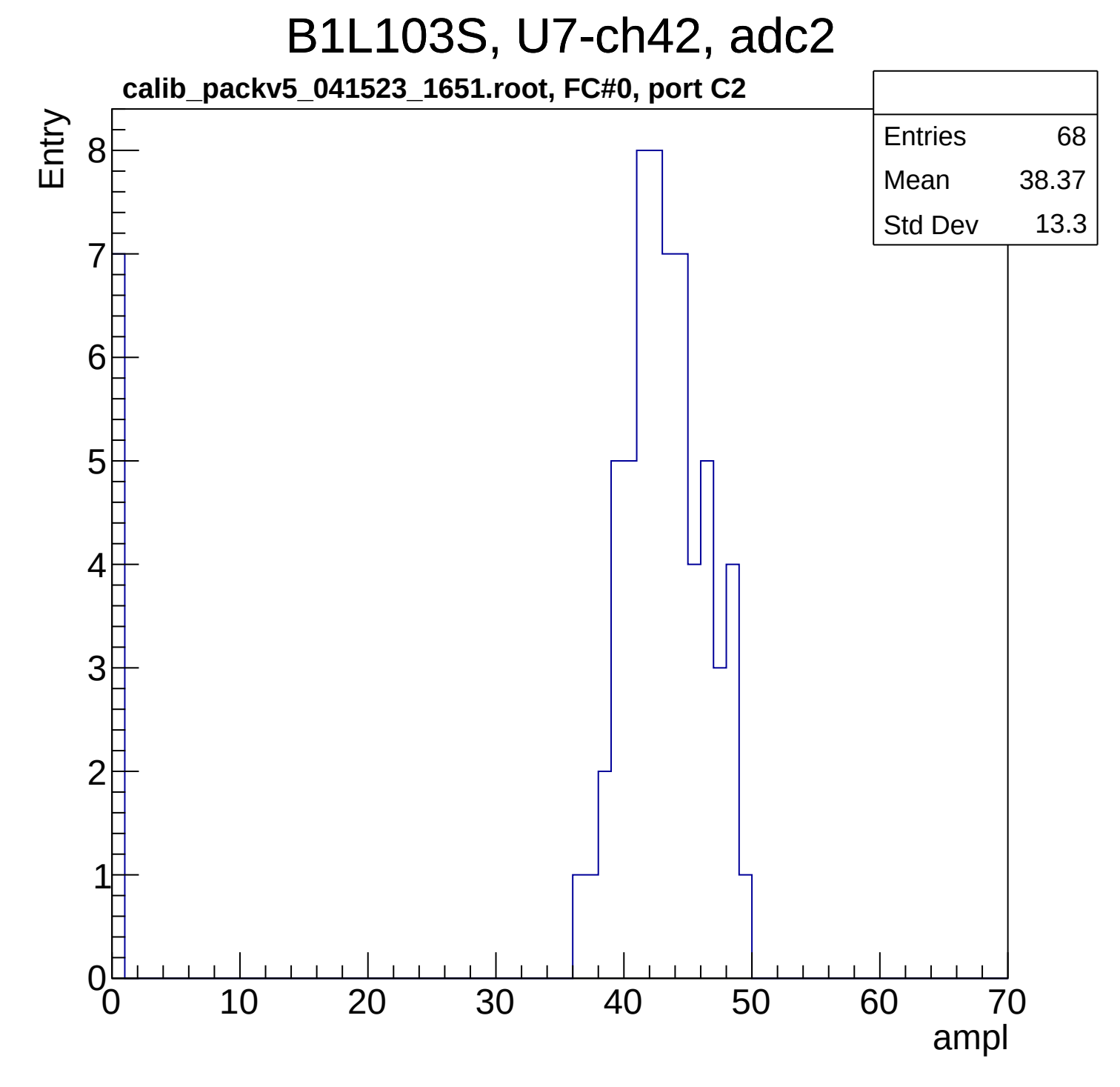
B1L103S, U7-ch42, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 38.37
Std Dev 13.3
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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40
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60
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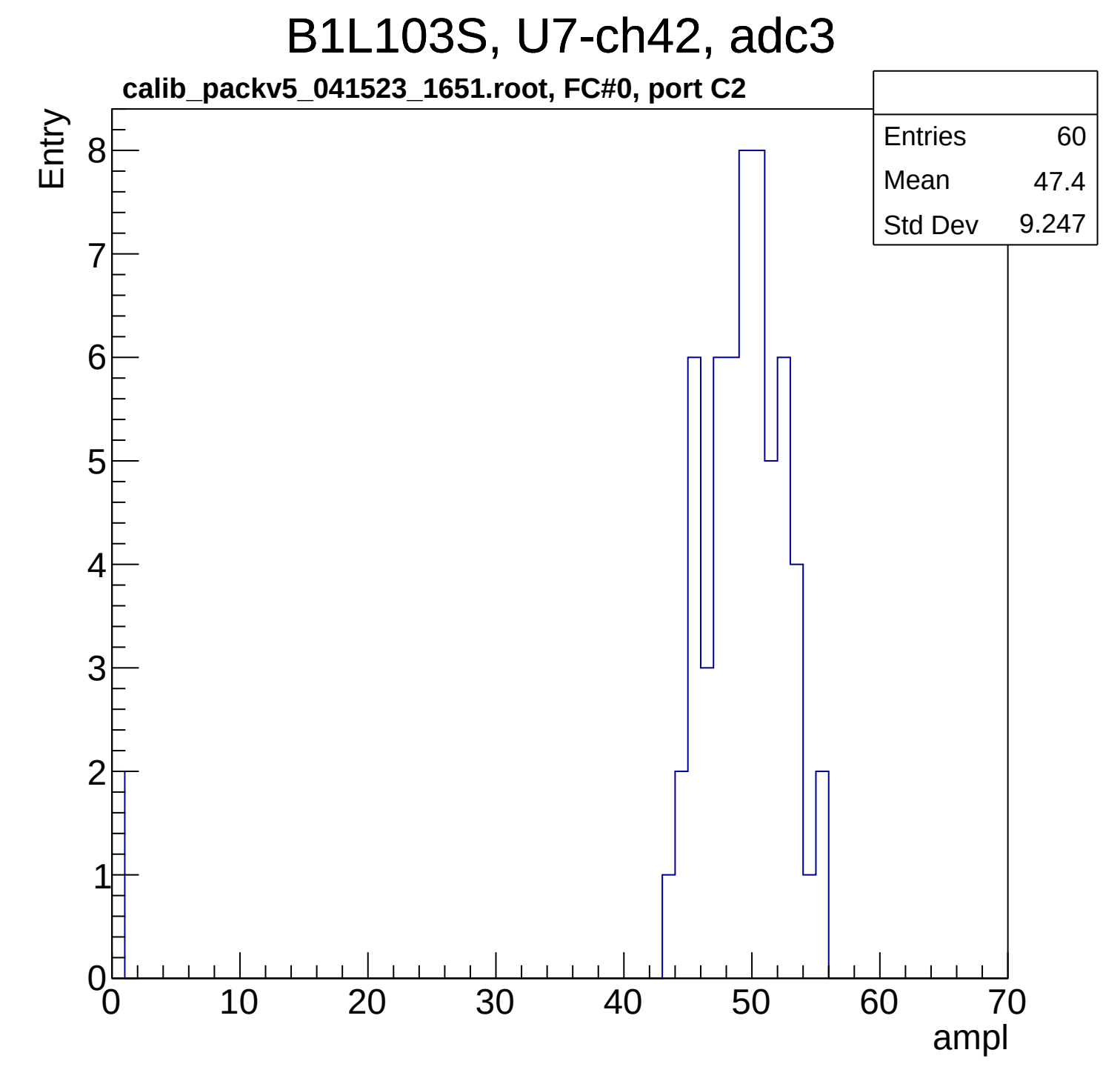
B1L103S, U7-ch42, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 47.4
Std Dev 9.247
Entry
ampl
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2
3
4
5
6
7
8
0
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20
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40
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60
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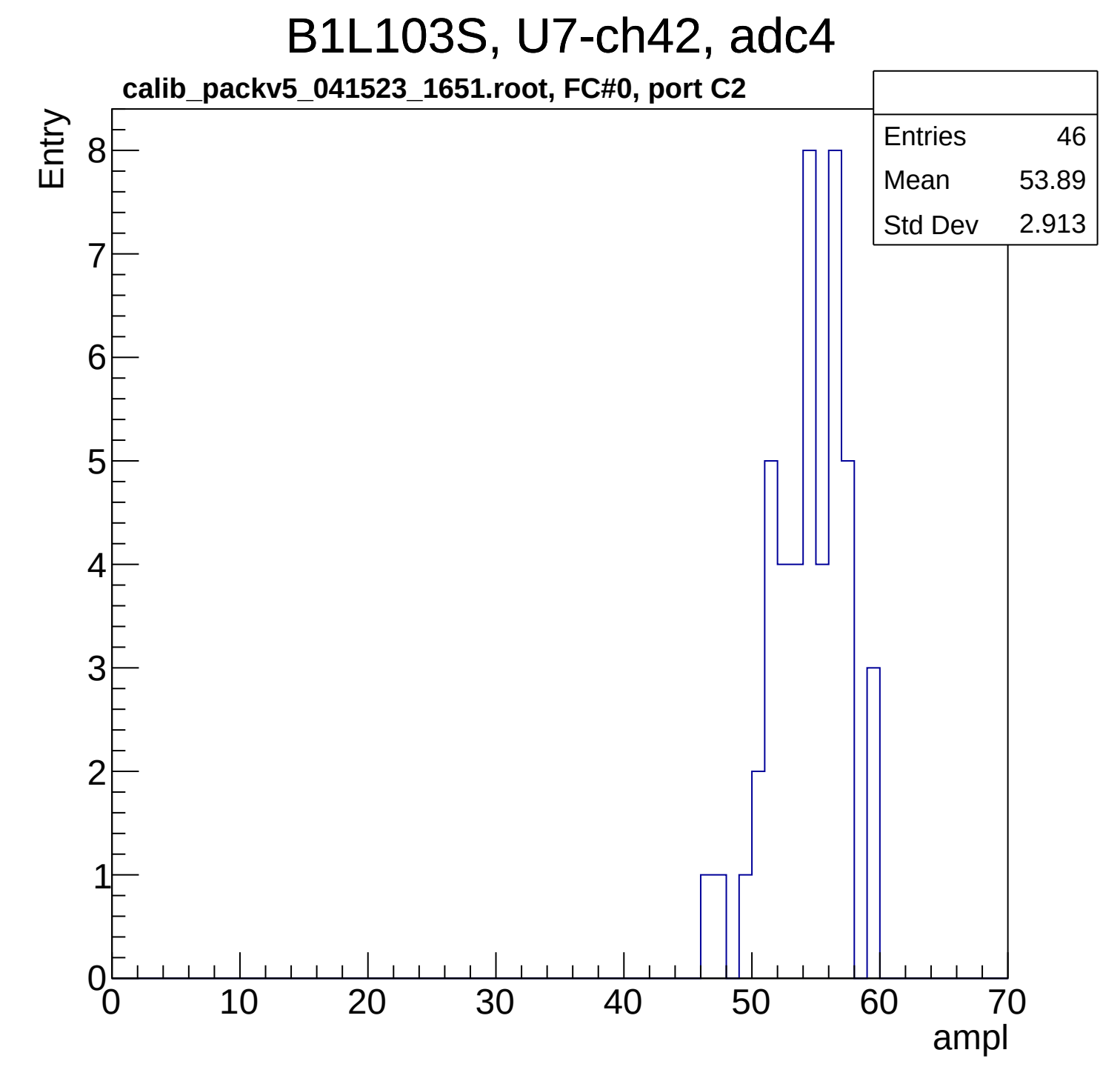
B1L103S, U7-ch42, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 53.89
Std Dev 2.913
Entry
ampl
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2
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4
5
6
7
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0
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60
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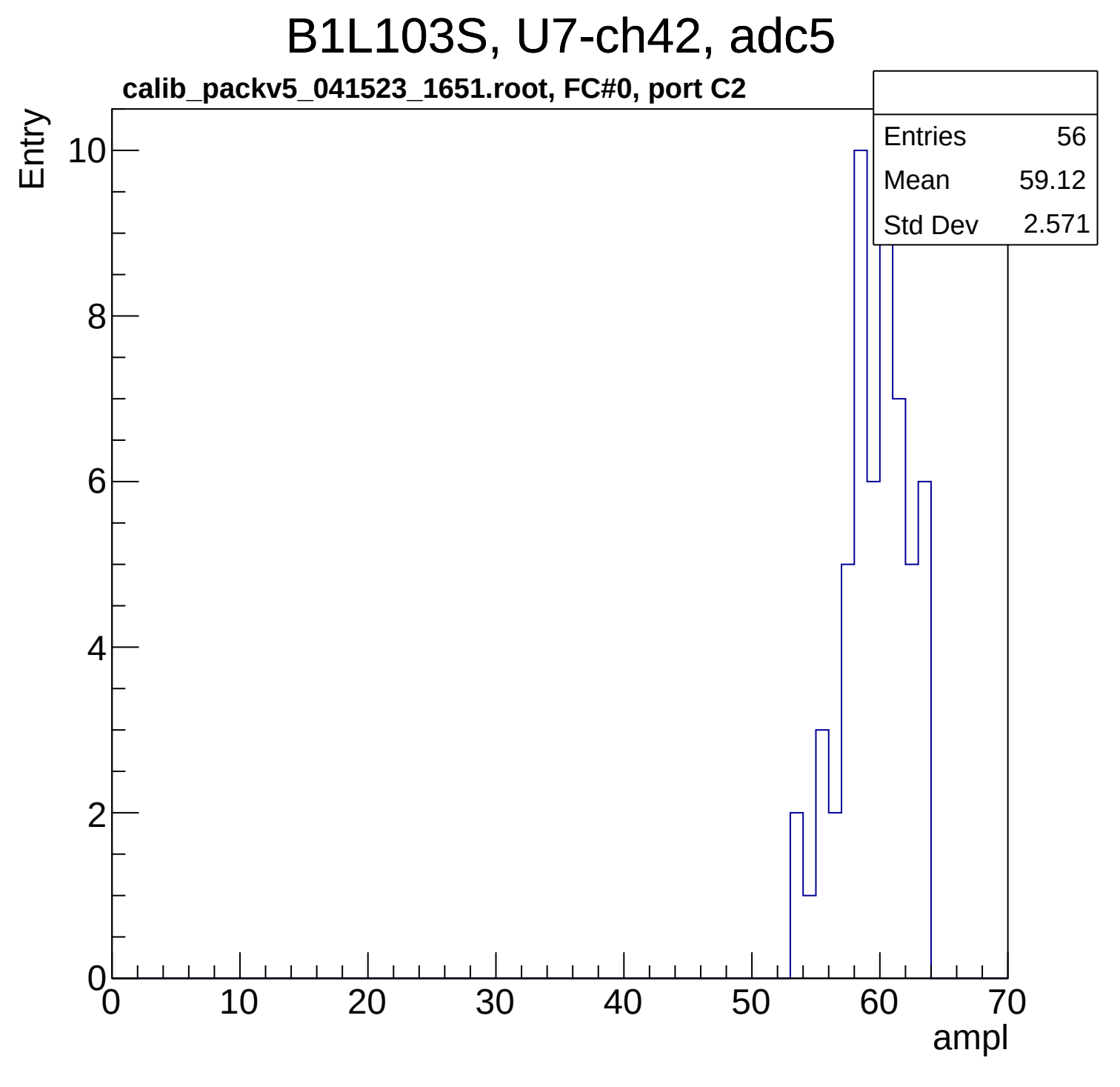
B1L103S, U7-ch42, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 59.12
Std Dev 2.571
Entry
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10
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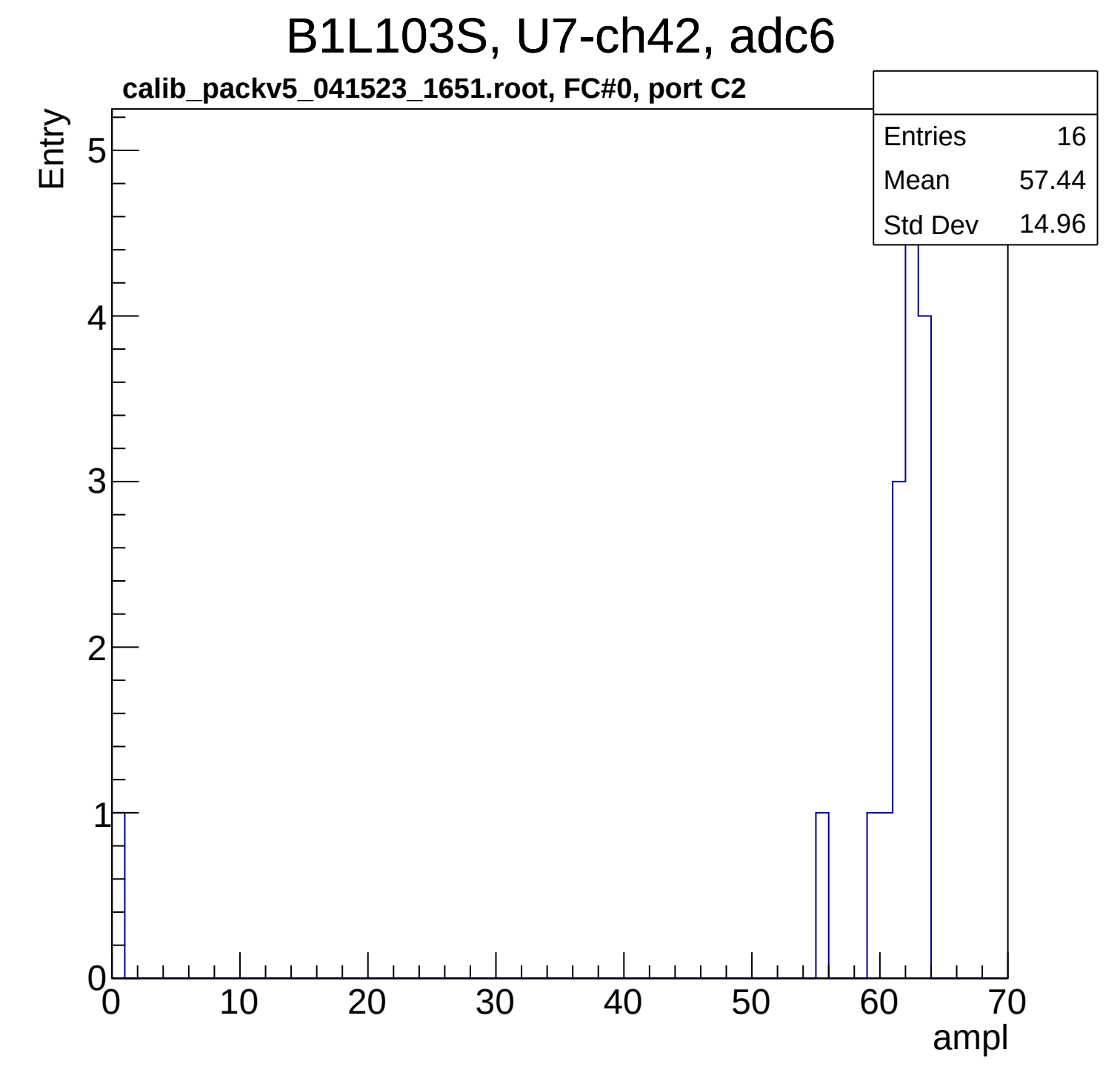
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch42, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 16
Mean 57.44
Std Dev 14.96
Entry
ampl
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4
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0
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60
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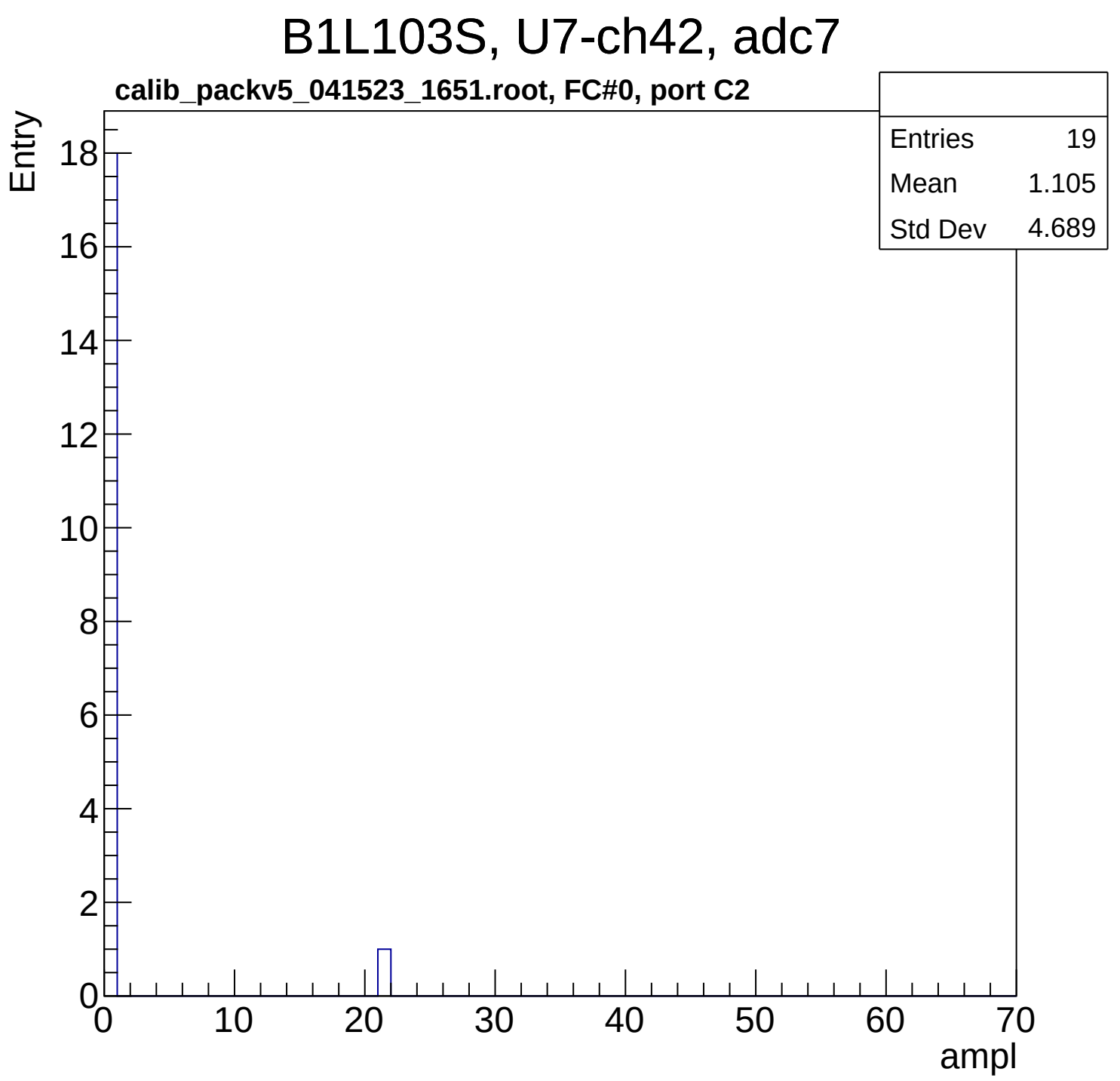
B1L103S, U7-ch42, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.105
Std Dev 4.689
Entry
0
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6
8
10
12
14
16
18
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10
20
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50
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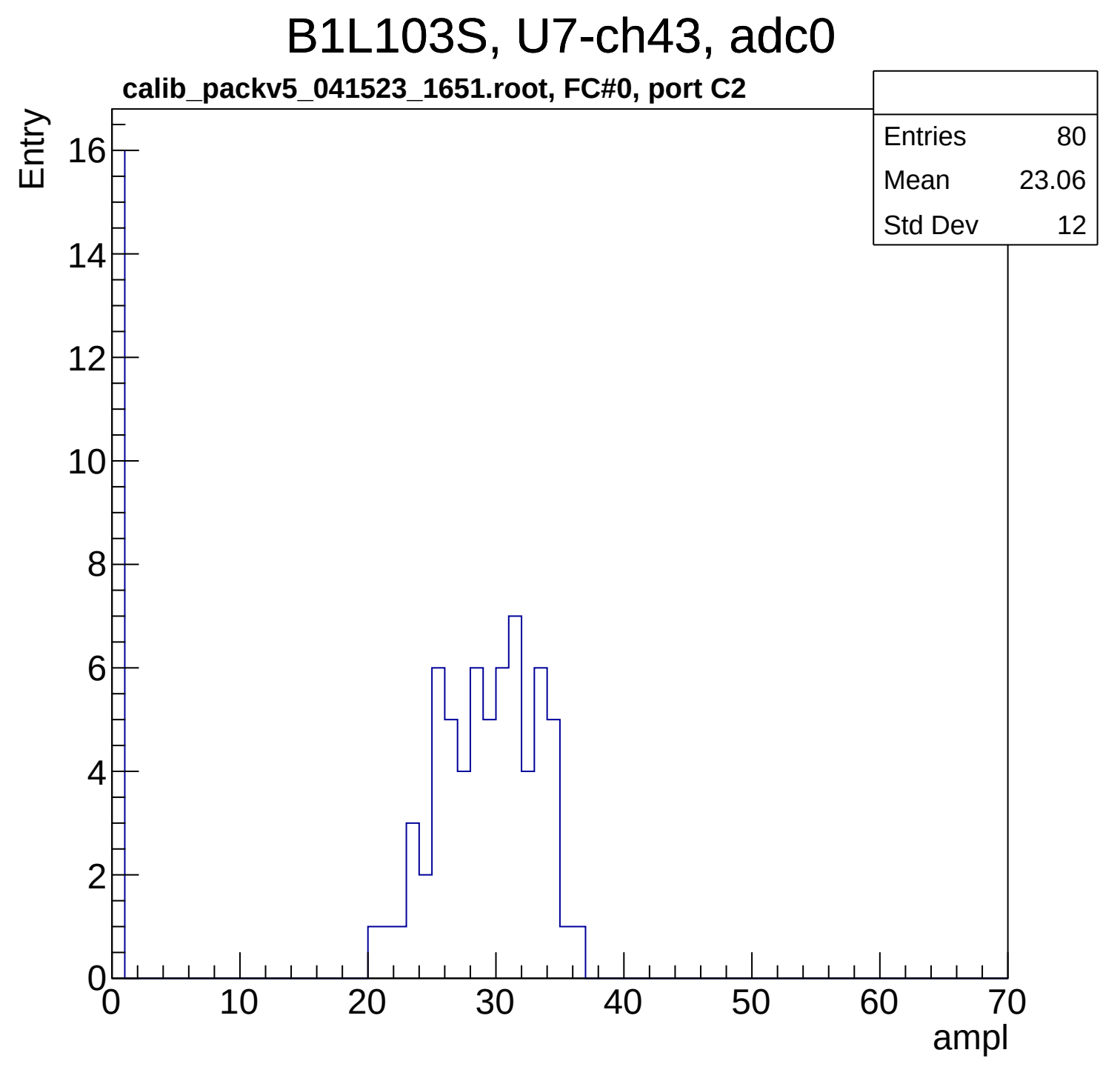
70
ampl


B1L103S, U7-ch43, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 23.06
Std Dev 12
Entry
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6
8
10
12
14
16
0
10
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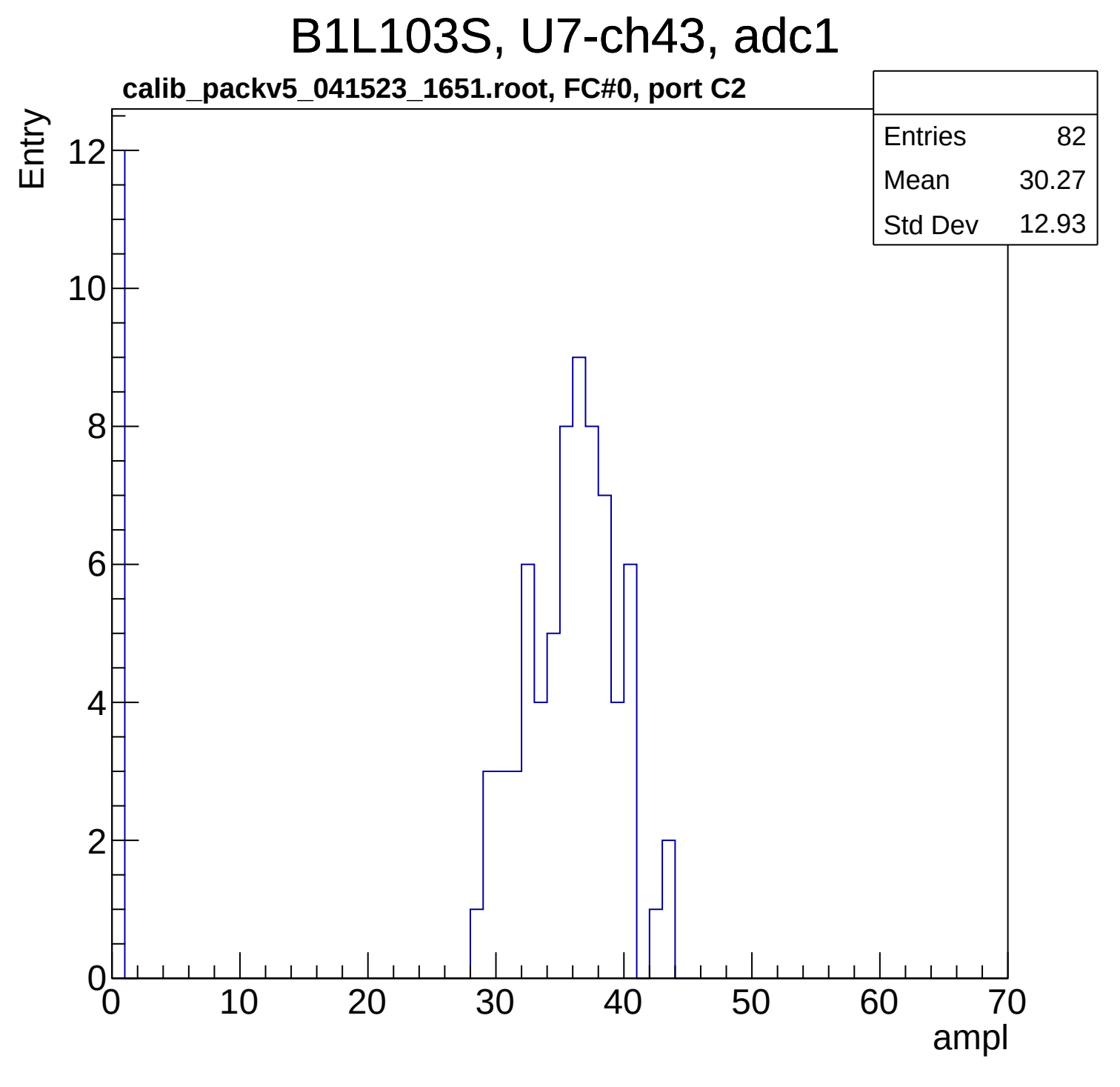
50
60
70
ampl


B1L103S, U7-ch43, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 30.27
Std Dev 12.93
Entry
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10
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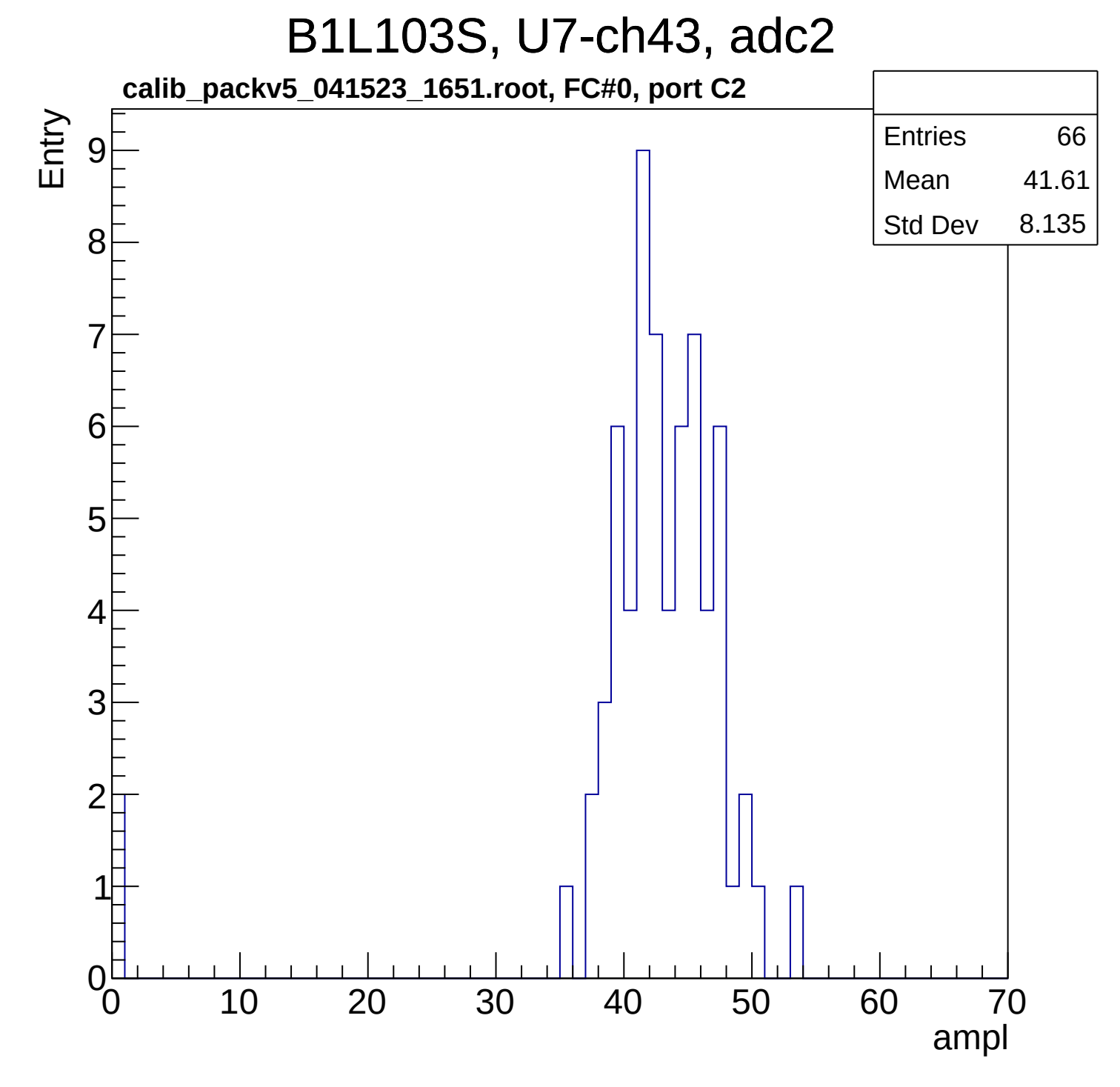
70
ampl


B1L103S, U7-ch43, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 41.61
Std Dev 8.135
Entry
ampl
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4
5
6
7
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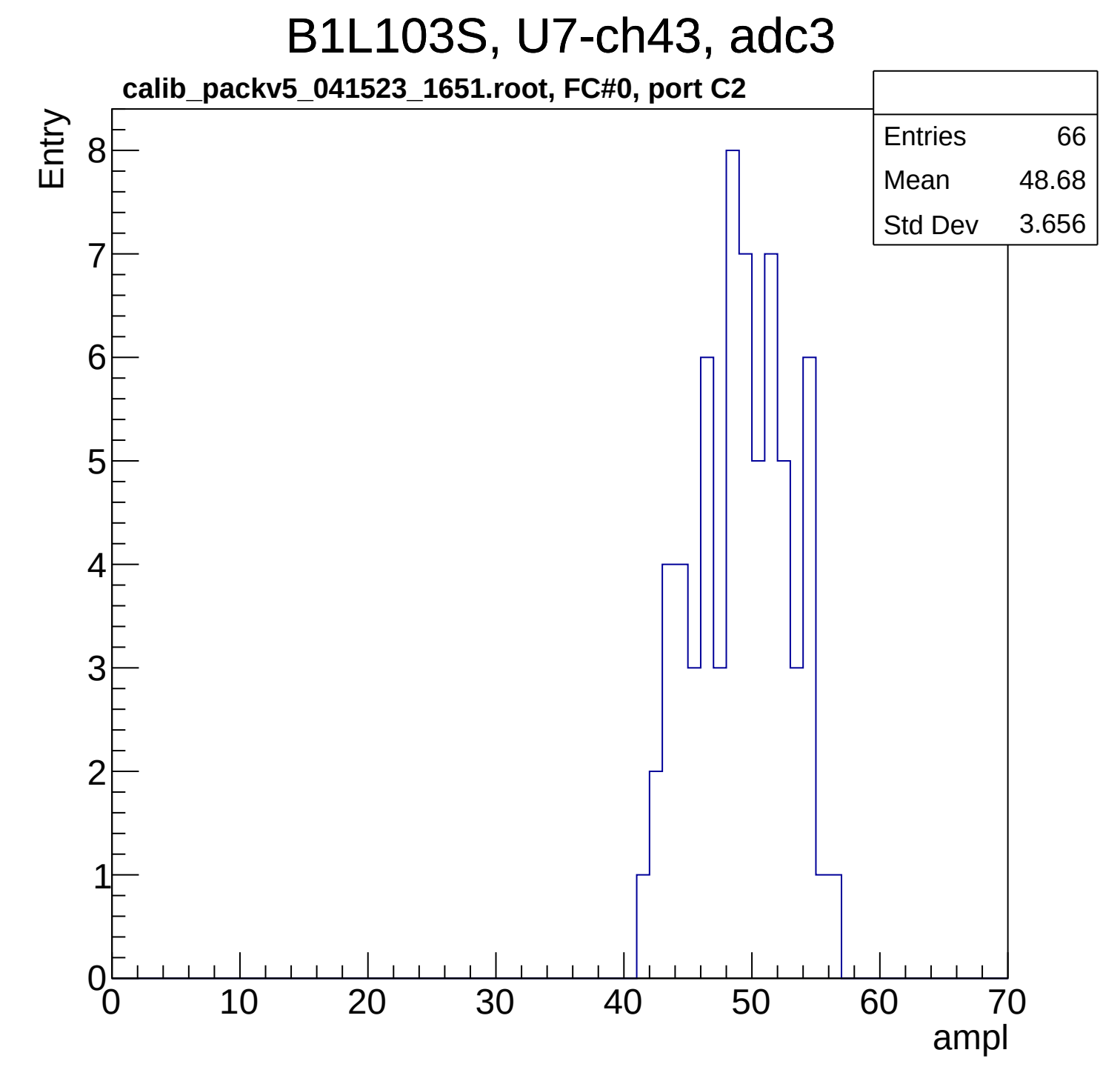
B1L103S, U7-ch43, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 48.68
Std Dev 3.656
Entry
ampl
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2
3
4
5
6
7
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0
10
20
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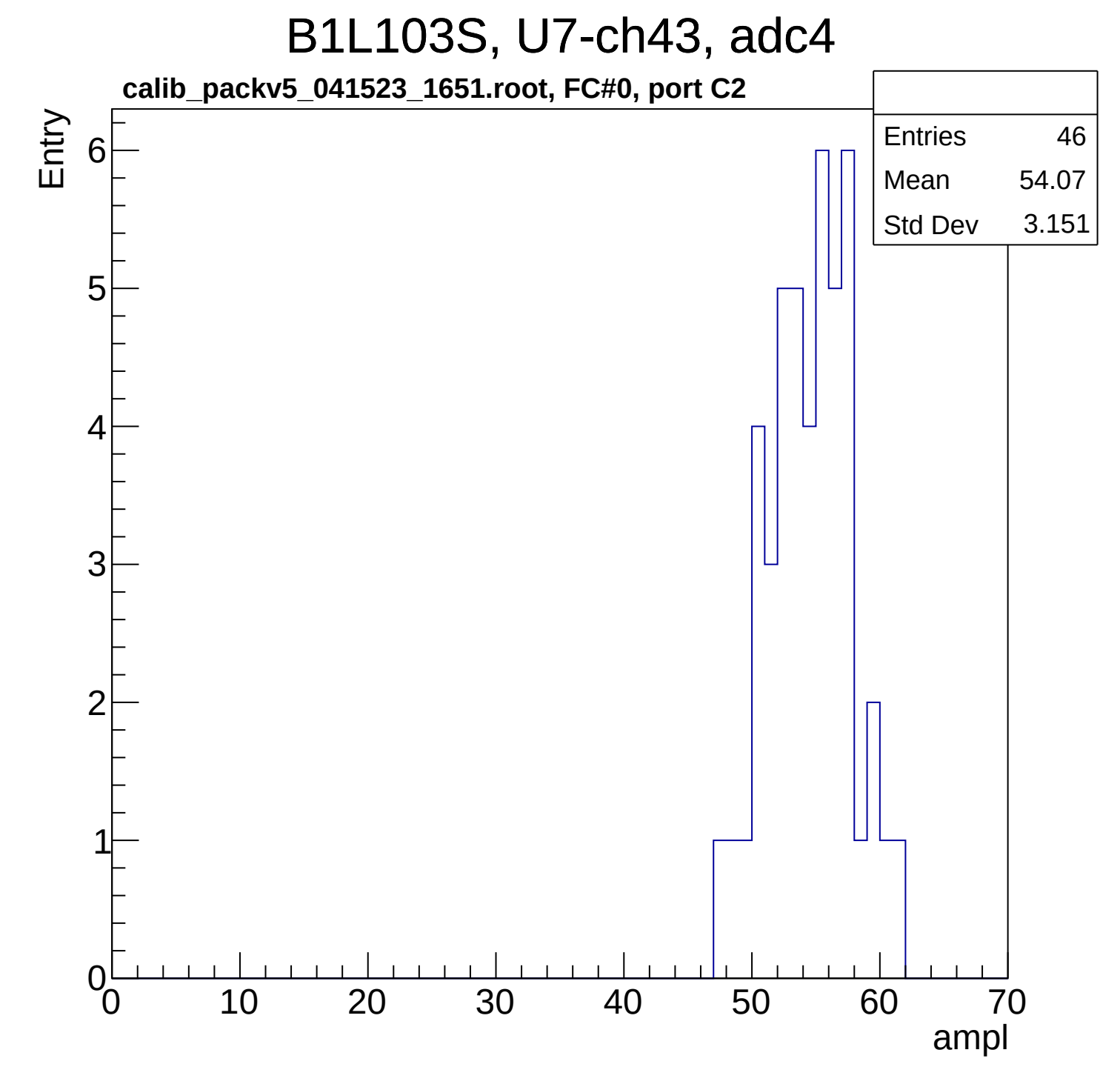
B1L103S, U7-ch43, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 54.07
Std Dev 3.151
Entry
ampl
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0
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40
50
60
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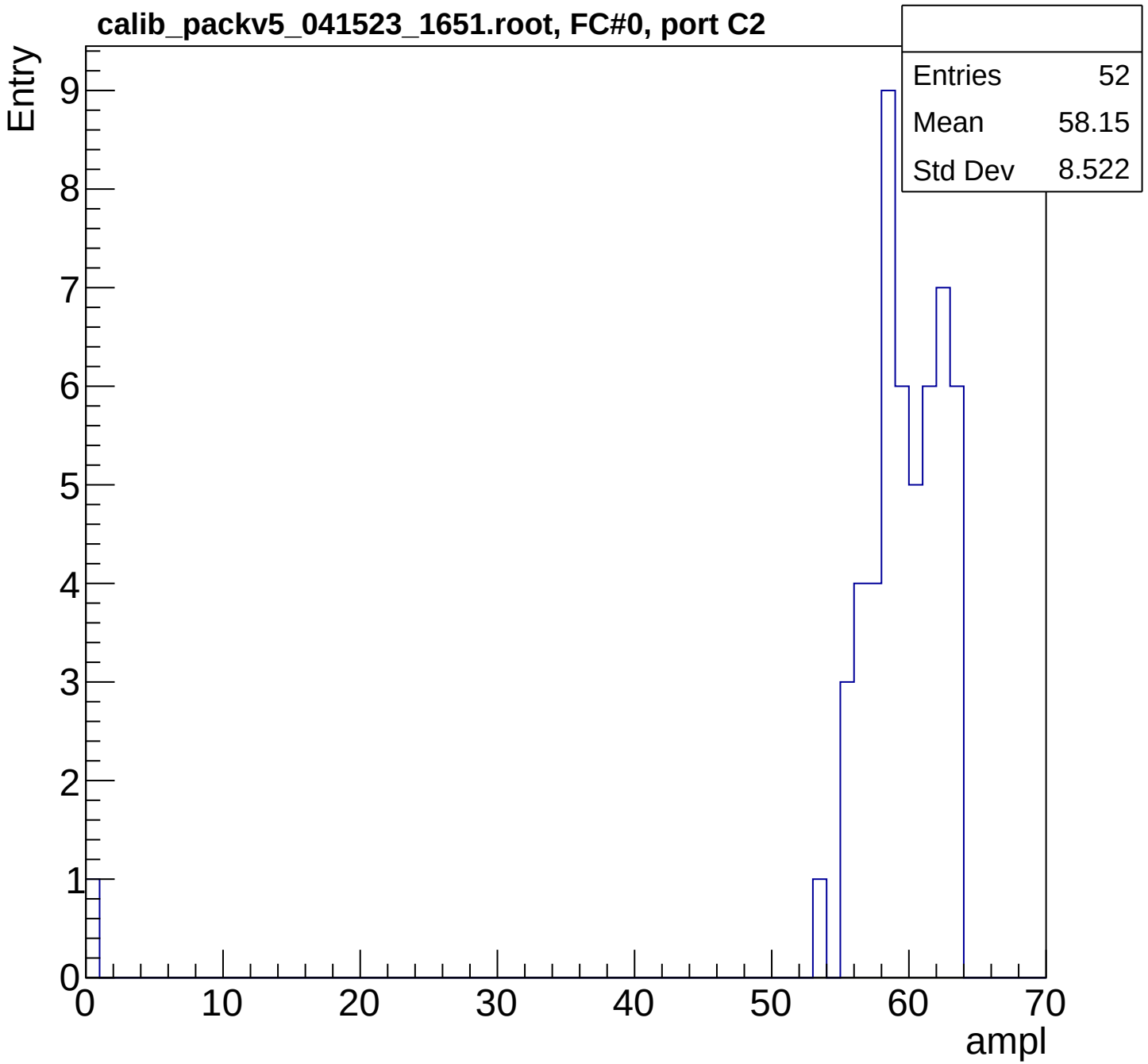
B1L103S, U7-ch43, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 58.15
Std Dev 8.522
Entry
ampl
0
1
2
3
4
5
6
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8
9
0
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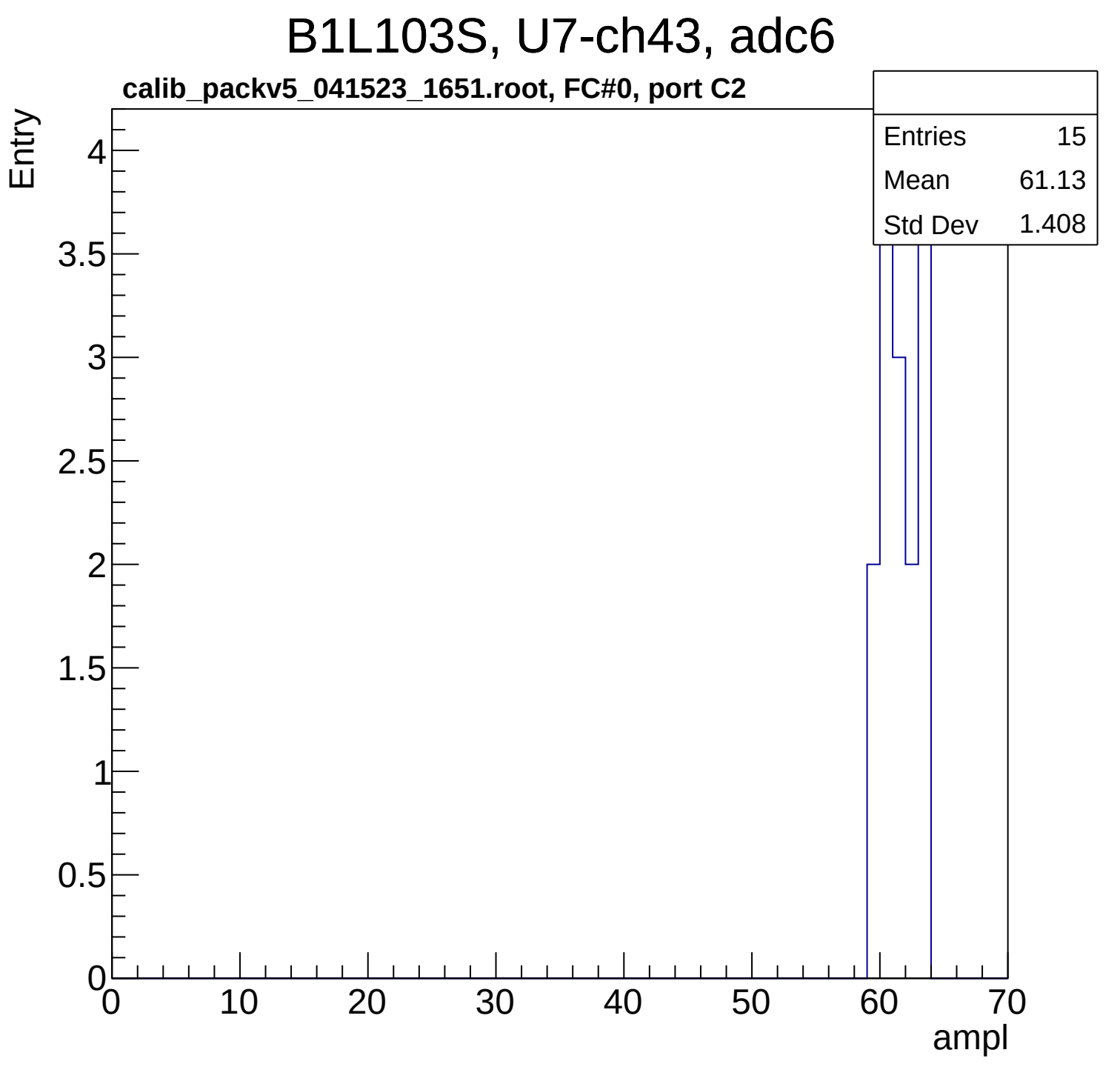
50
60
70


B1L103S, U7-ch43, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 15
Mean 61.13
Std Dev 1.408
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
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40
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60
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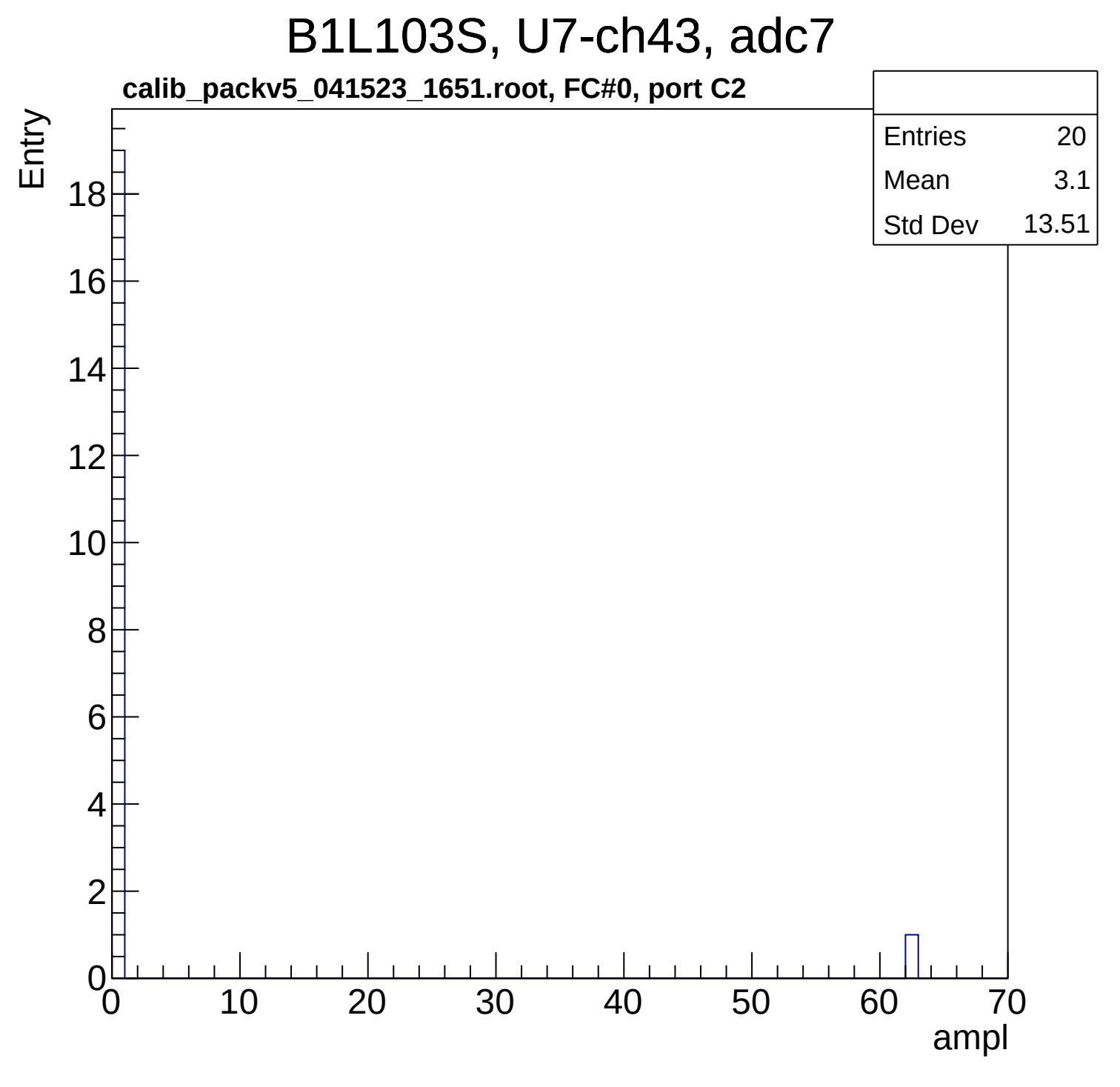
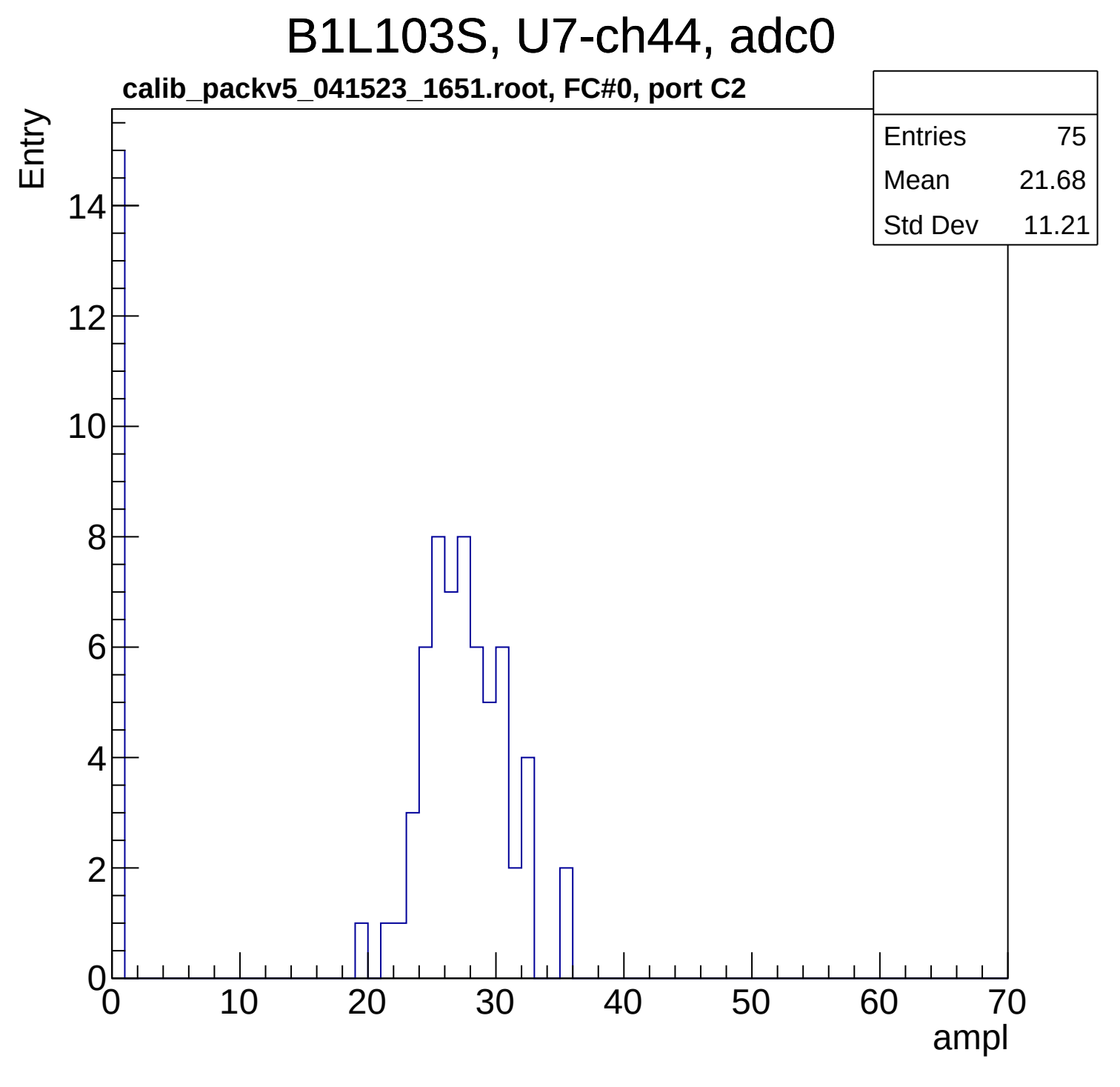

B1L103S, U7-ch43, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.1
Std Dev 13.51
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch44, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 21.68
Std Dev 11.21
Entry
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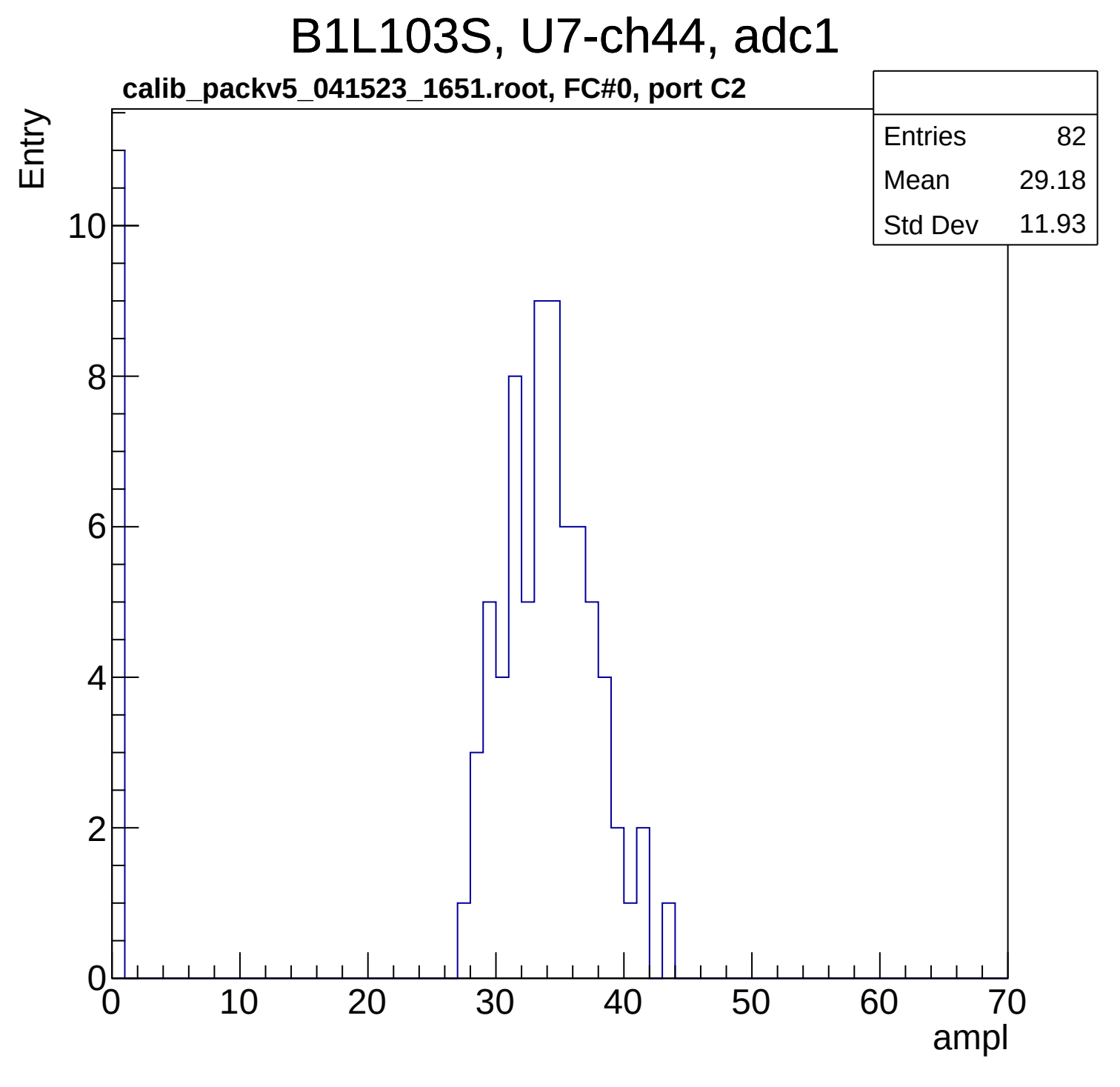
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch44, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 29.18
Std Dev 11.93
Entry
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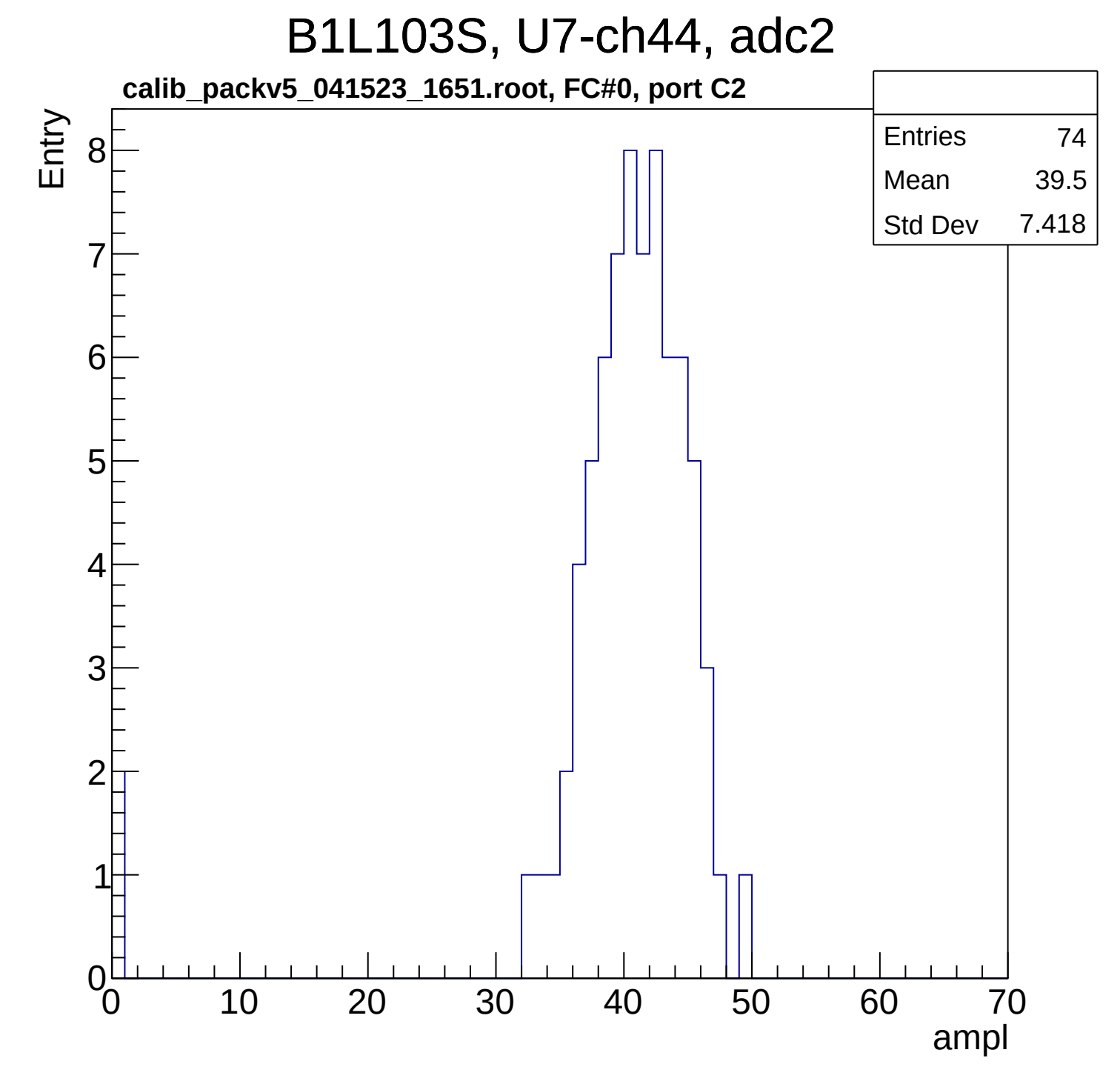
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch44, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 39.5
Std Dev 7.418
Entry
ampl
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2
3
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5
6
7
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0
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60
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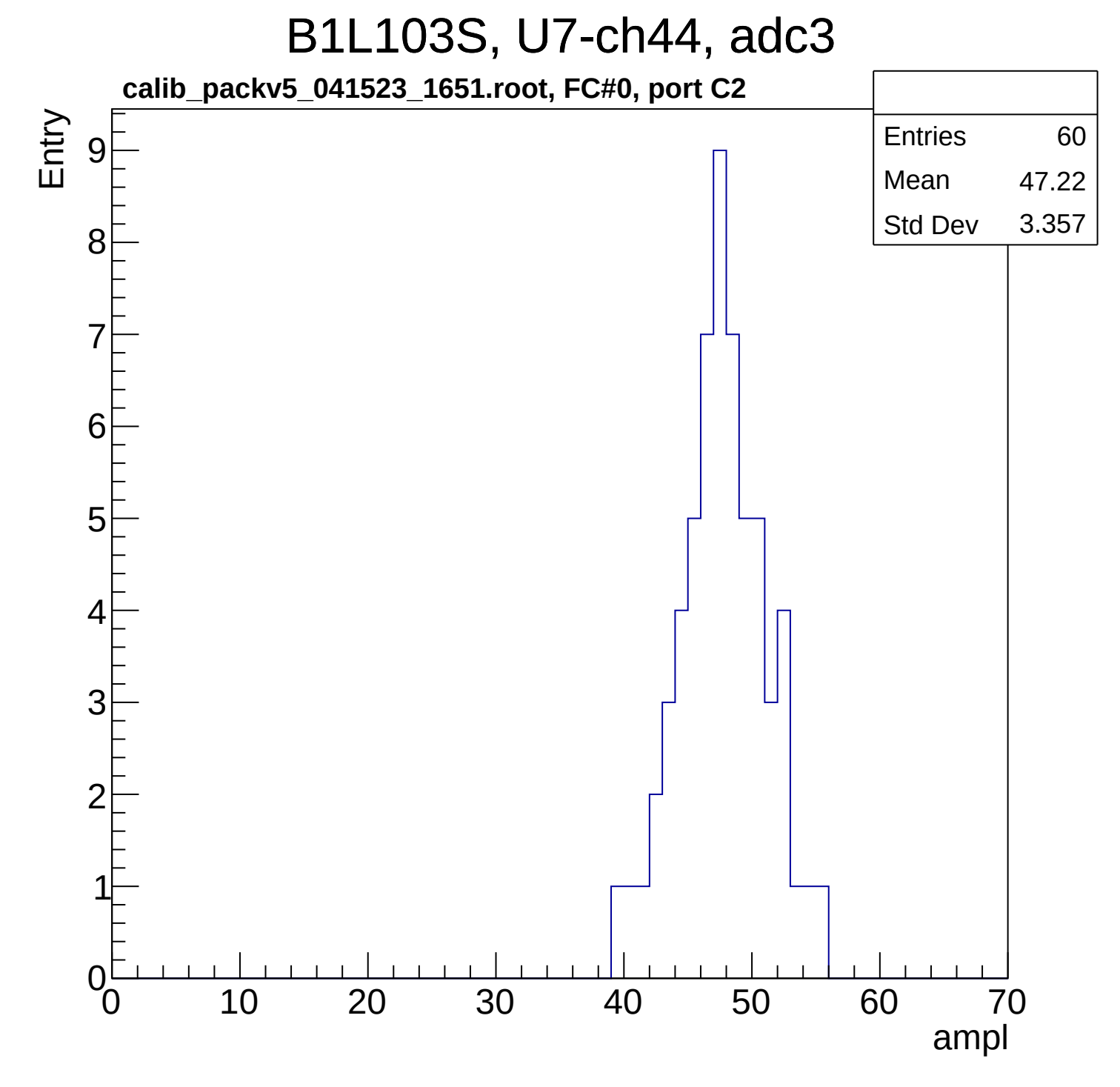
B1L103S, U7-ch44, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 47.22
Std Dev 3.357
Entry
ampl
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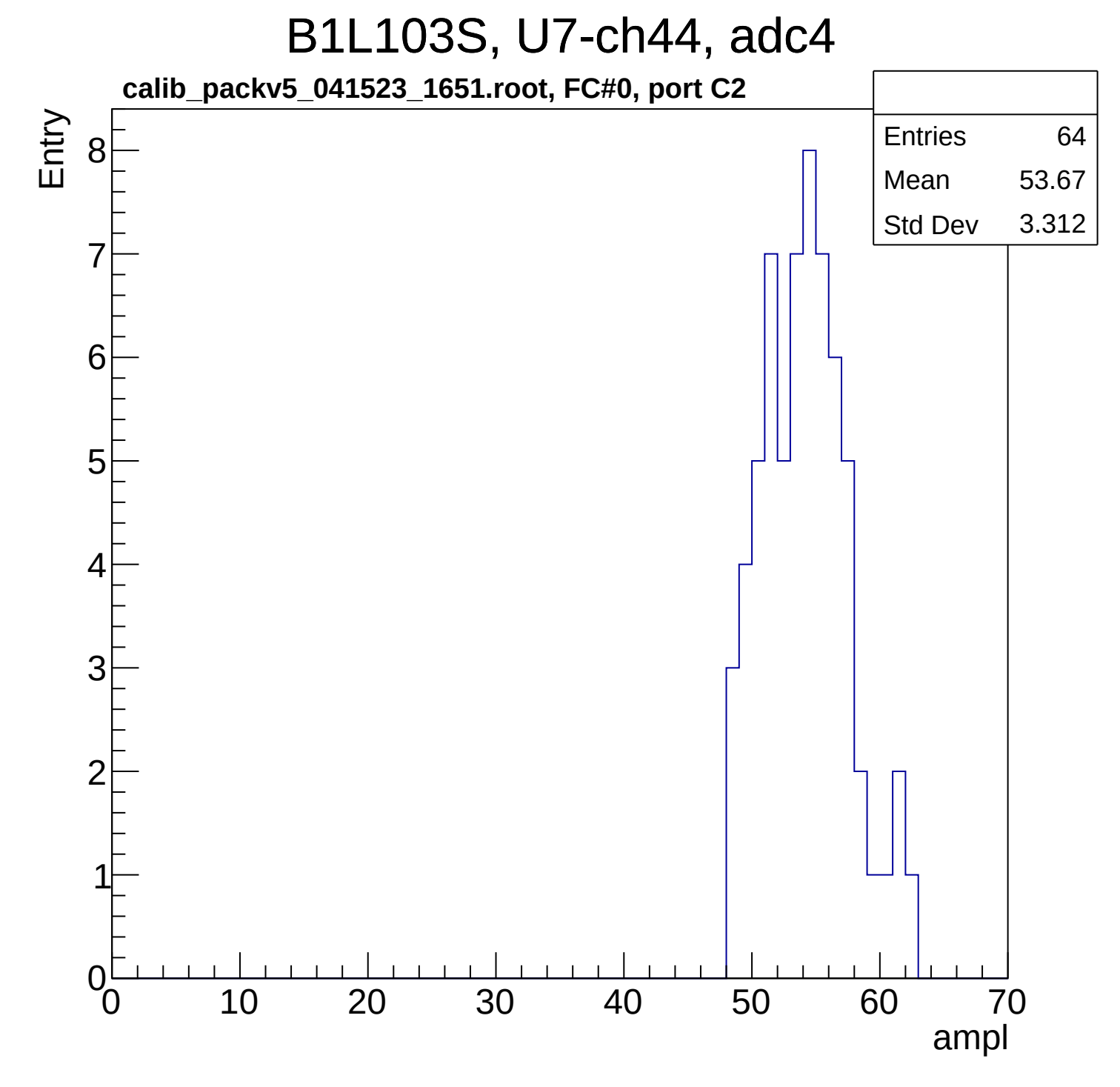
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U7-ch44, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 53.67
Std Dev 3.312
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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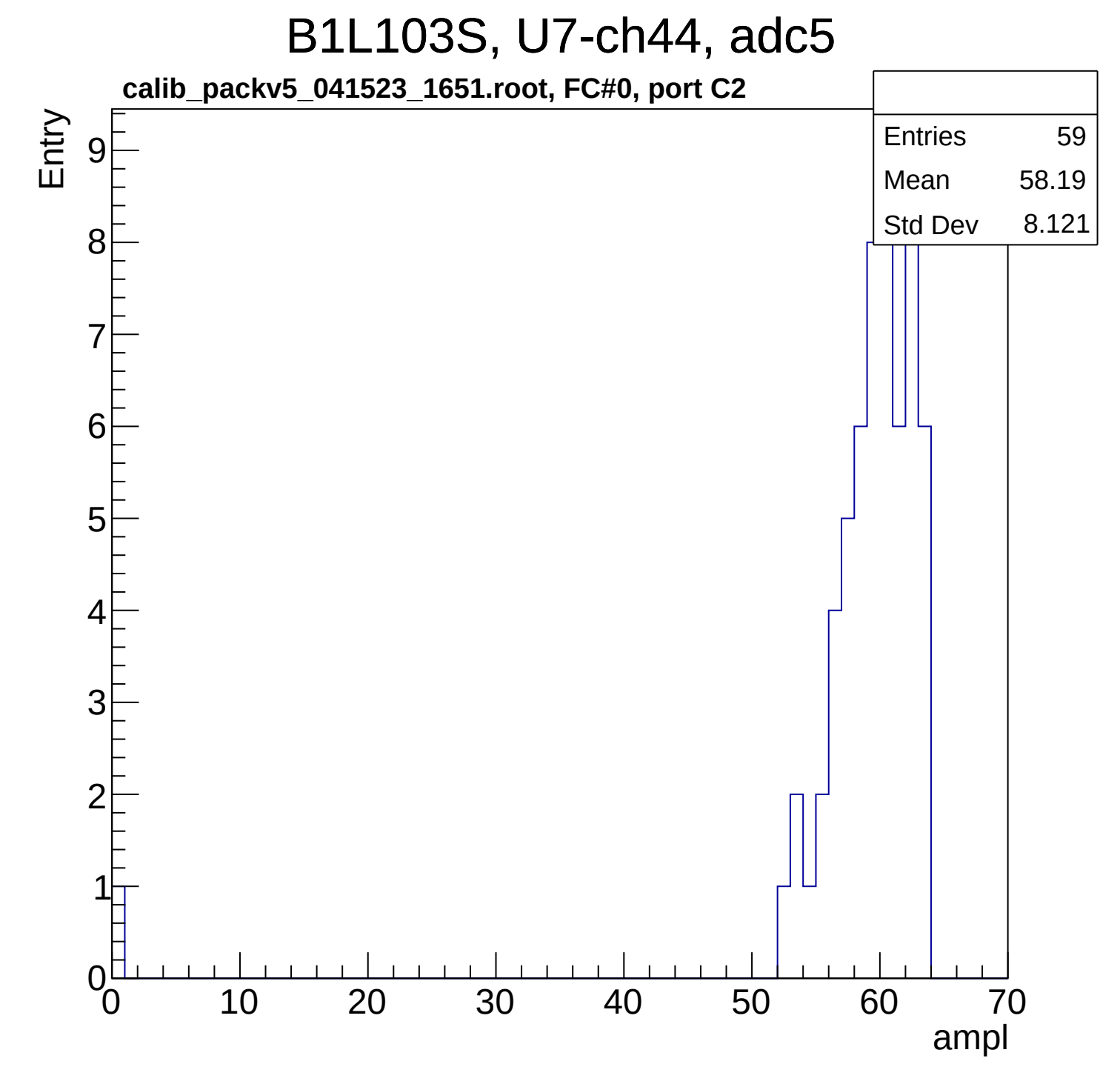
B1L103S, U7-ch44, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 58.19
Std Dev 8.121
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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60
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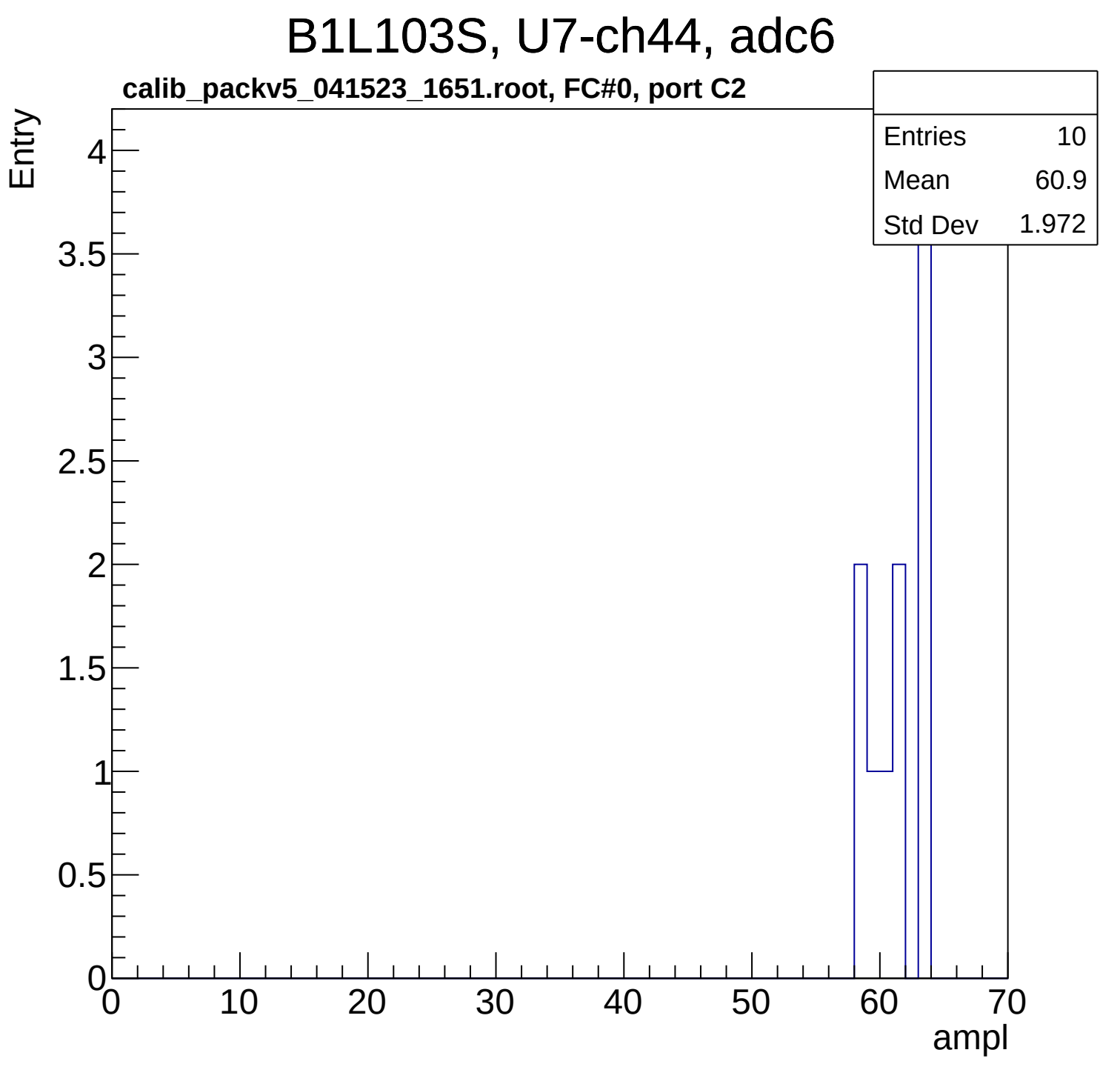
B1L103S, U7-ch44, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 60.9
Std Dev 1.972
Entry
ampl
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0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
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40
50
60
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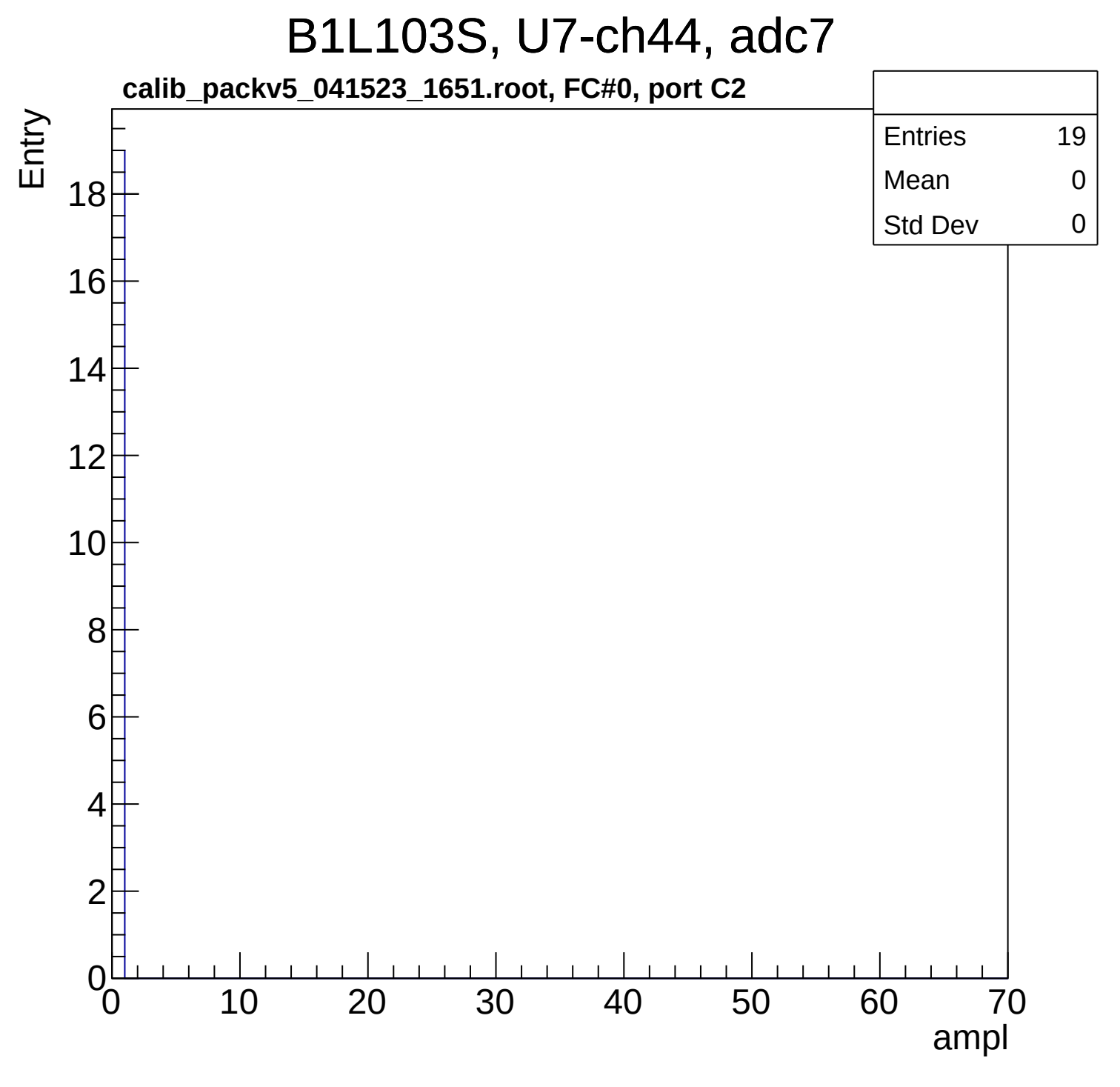
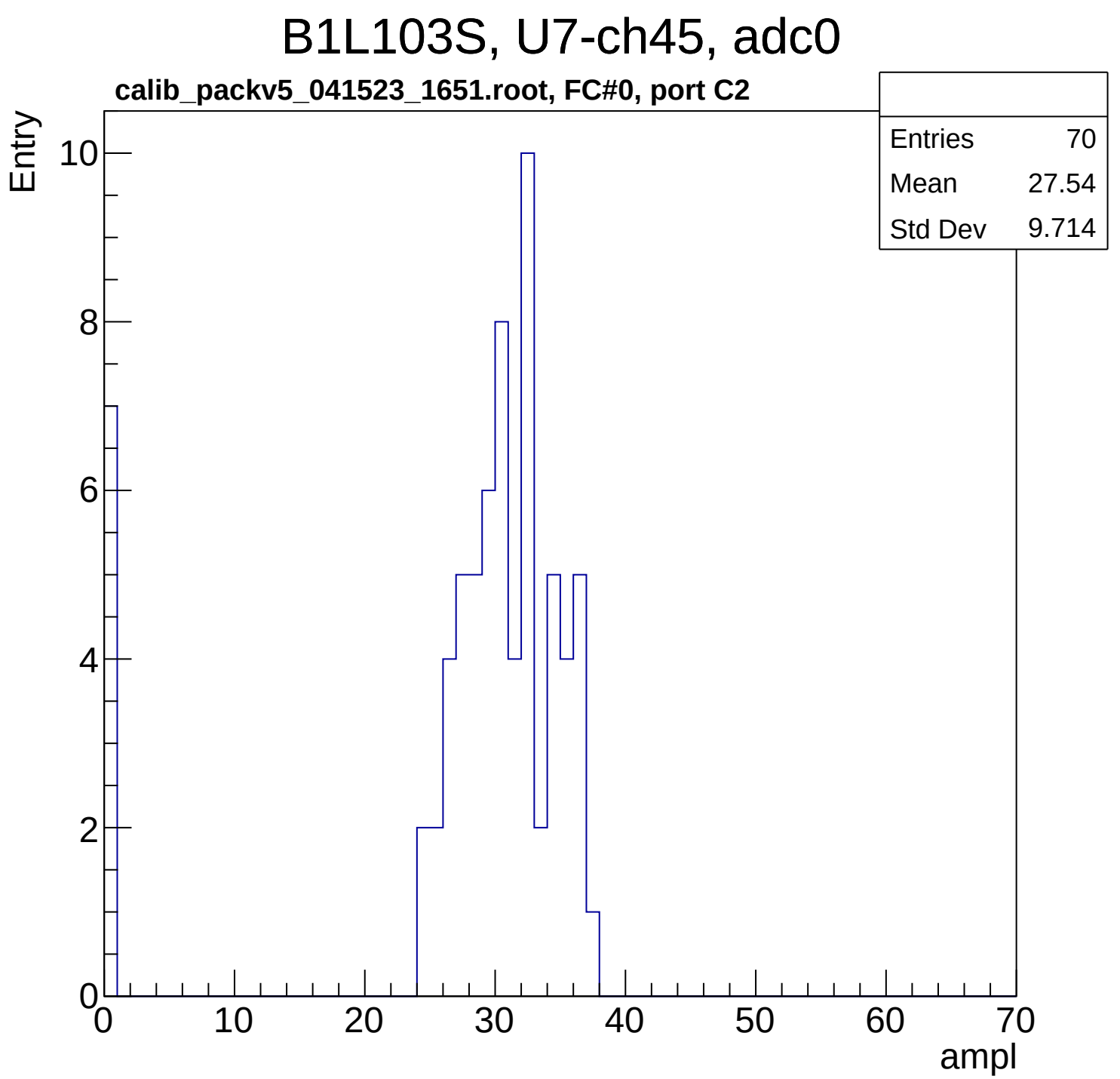

B1L103S, U7-ch44, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch45, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 27.54
Std Dev 9.714
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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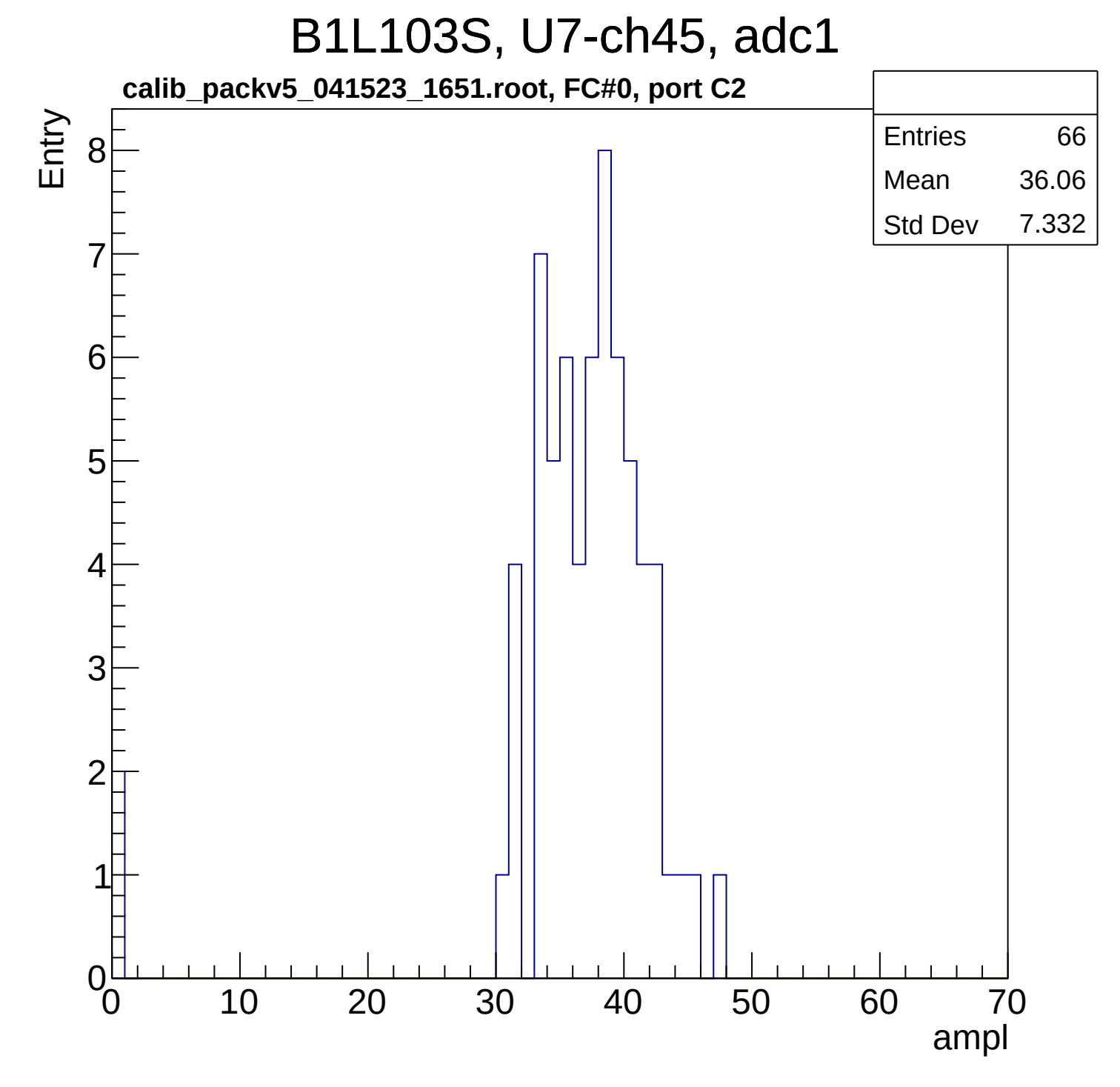
B1L103S, U7-ch45, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 36.06
Std Dev 7.332
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
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40
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60
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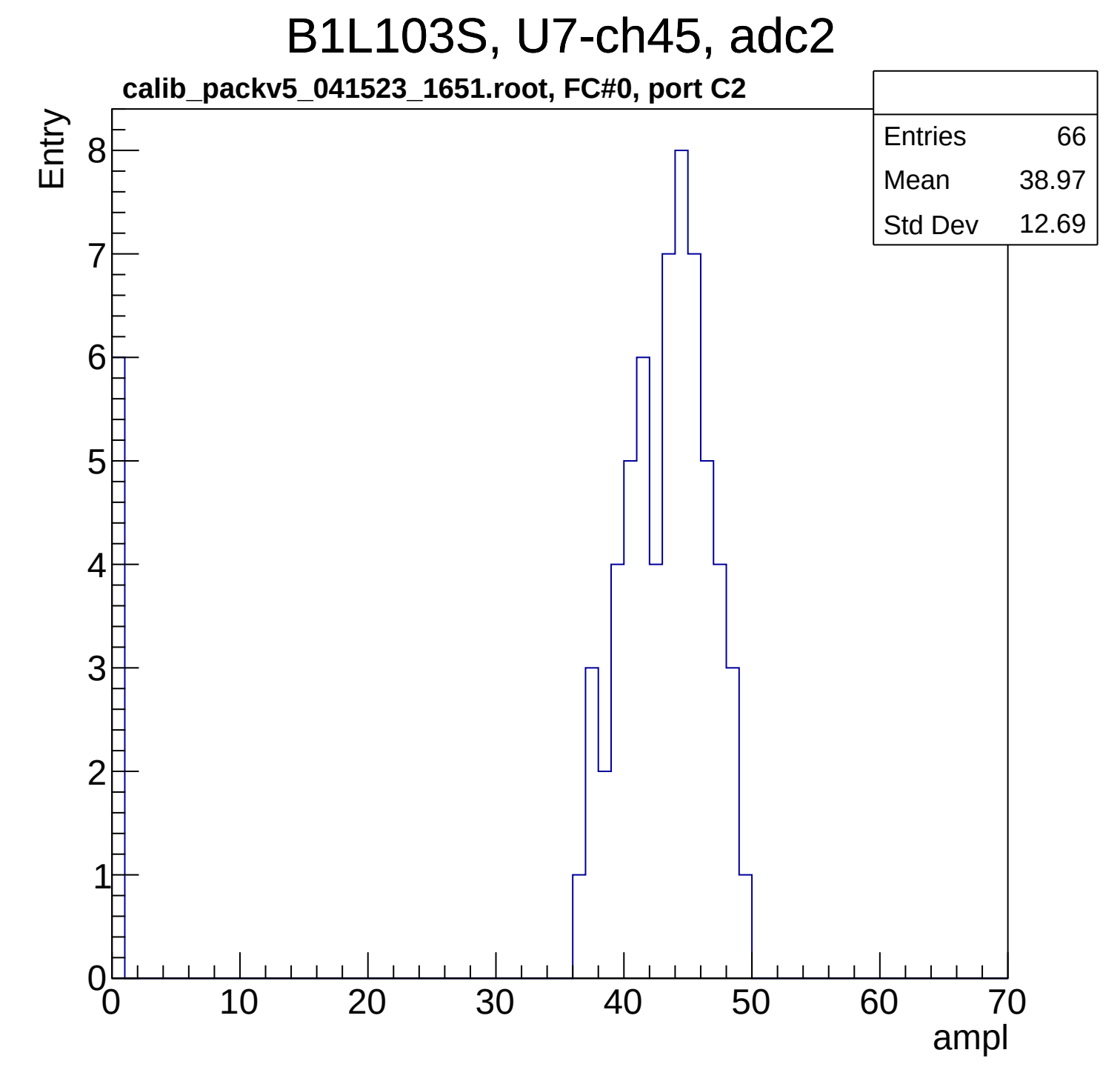
B1L103S, U7-ch45, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 38.97
Std Dev 12.69
Entry
ampl
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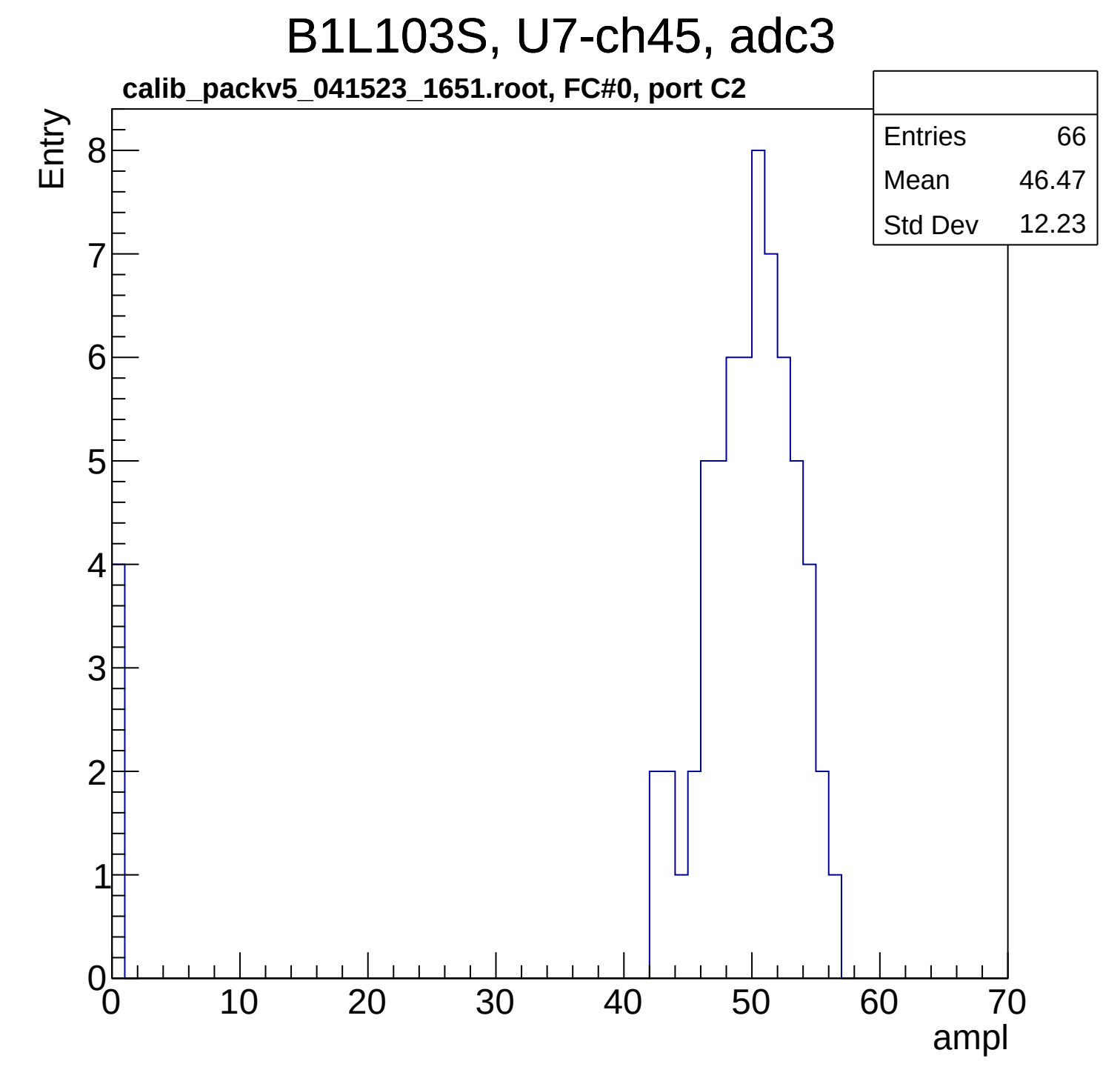
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch45, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 46.47
Std Dev 12.23
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
30
40
50
60
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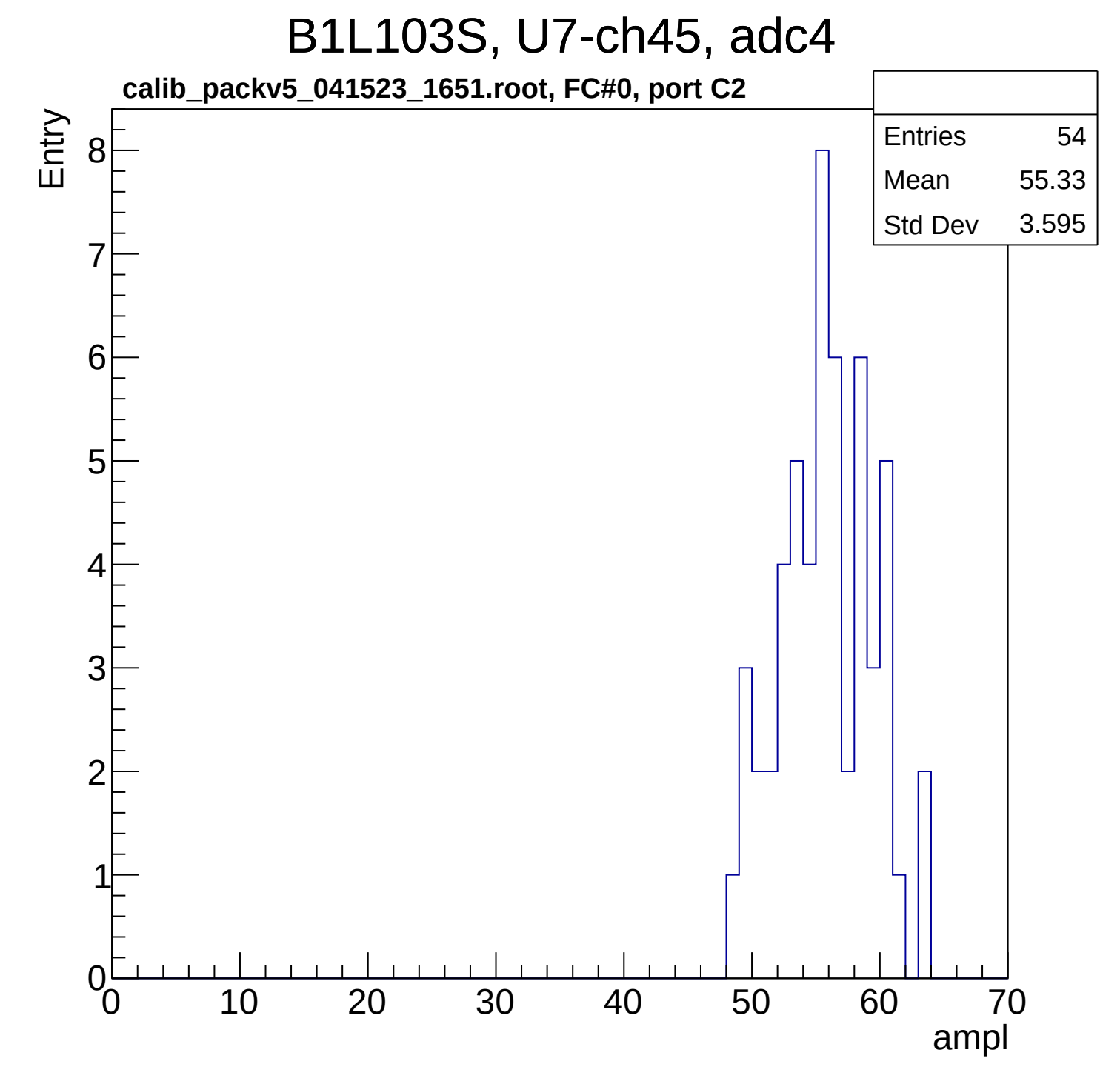
B1L103S, U7-ch45, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 55.33
Std Dev 3.595
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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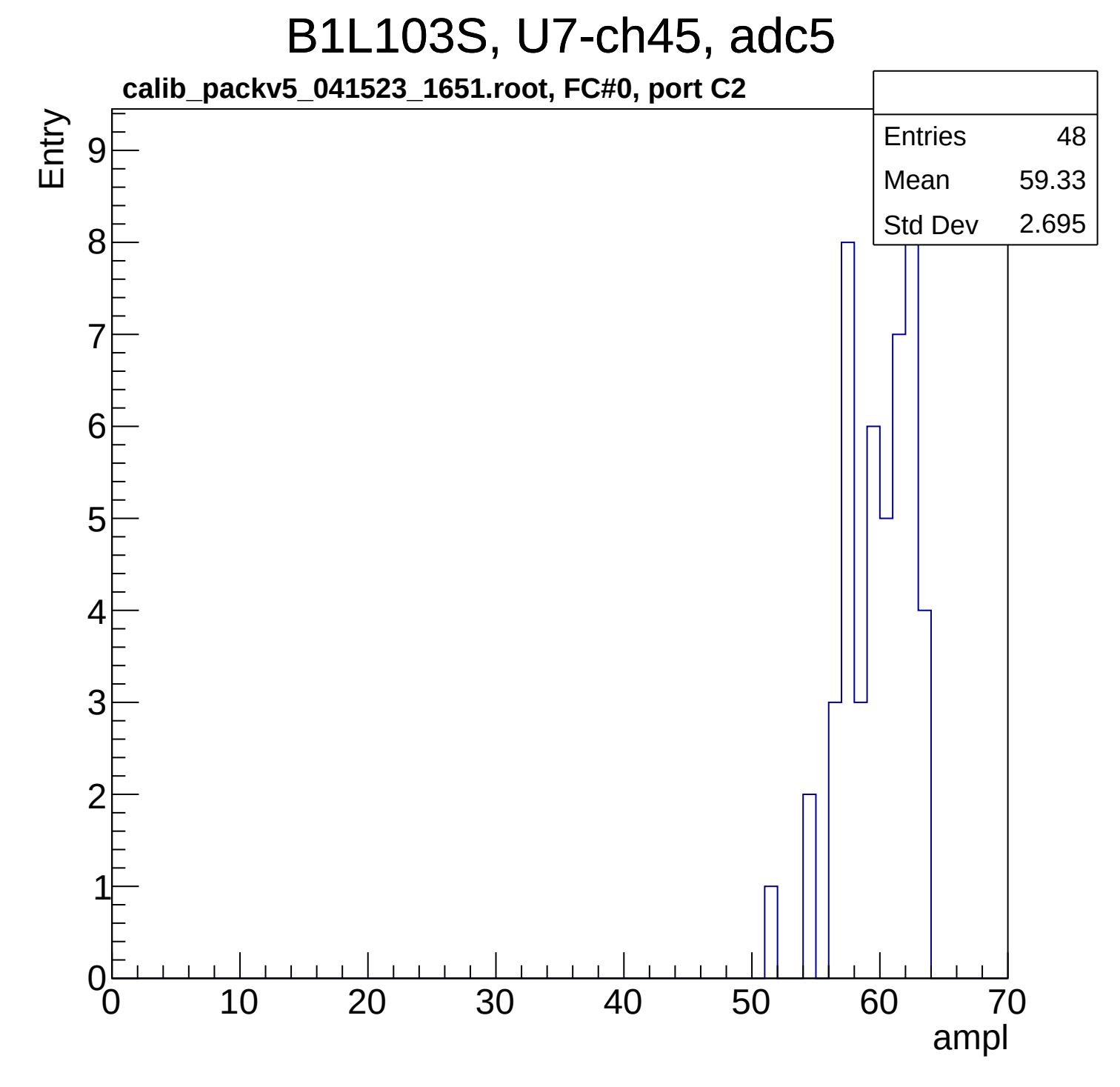
B1L103S, U7-ch45, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 59.33
Std Dev 2.695
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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60
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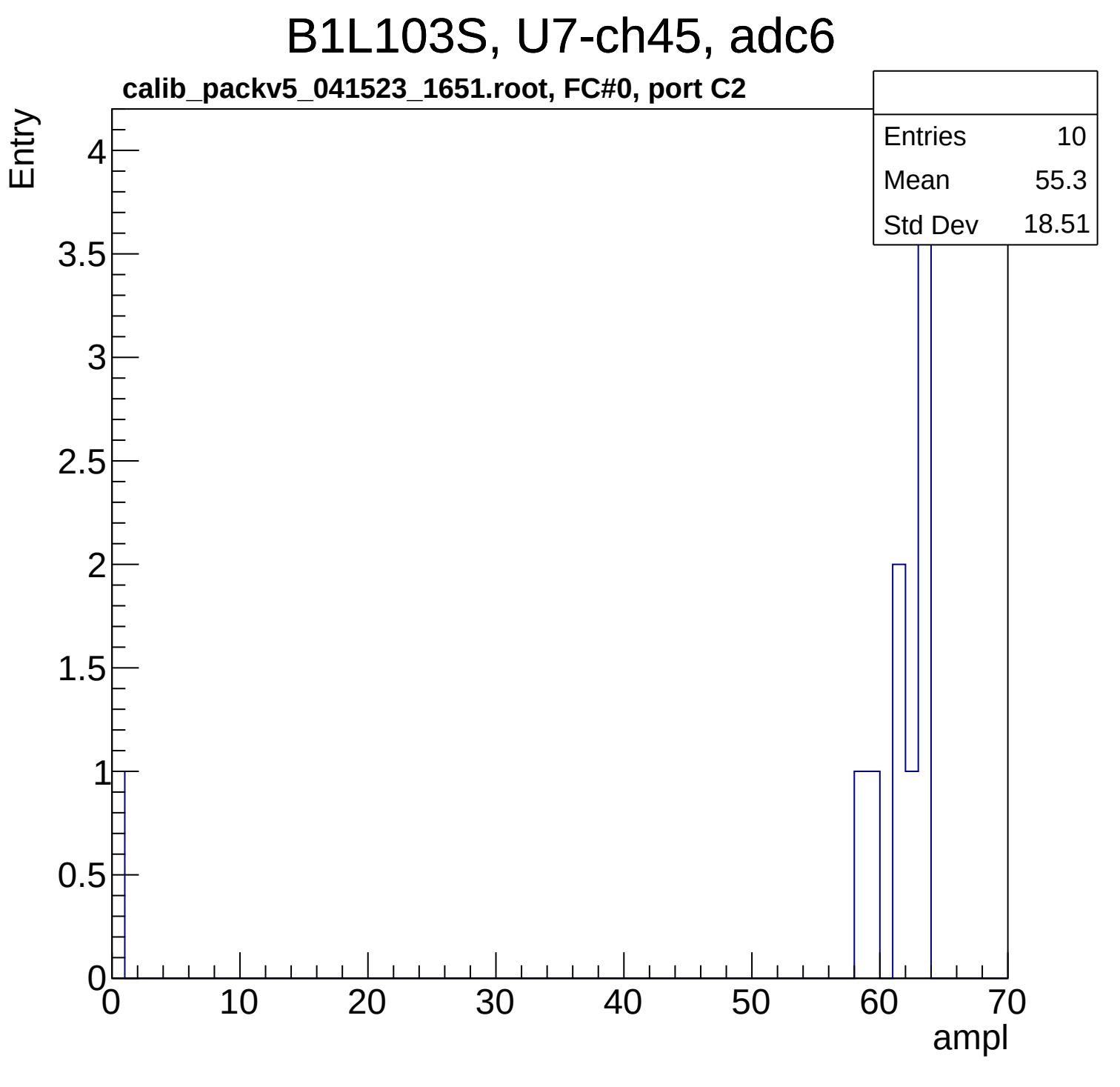
B1L103S, U7-ch45, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 55.3
Std Dev 18.51
Entry
ampl
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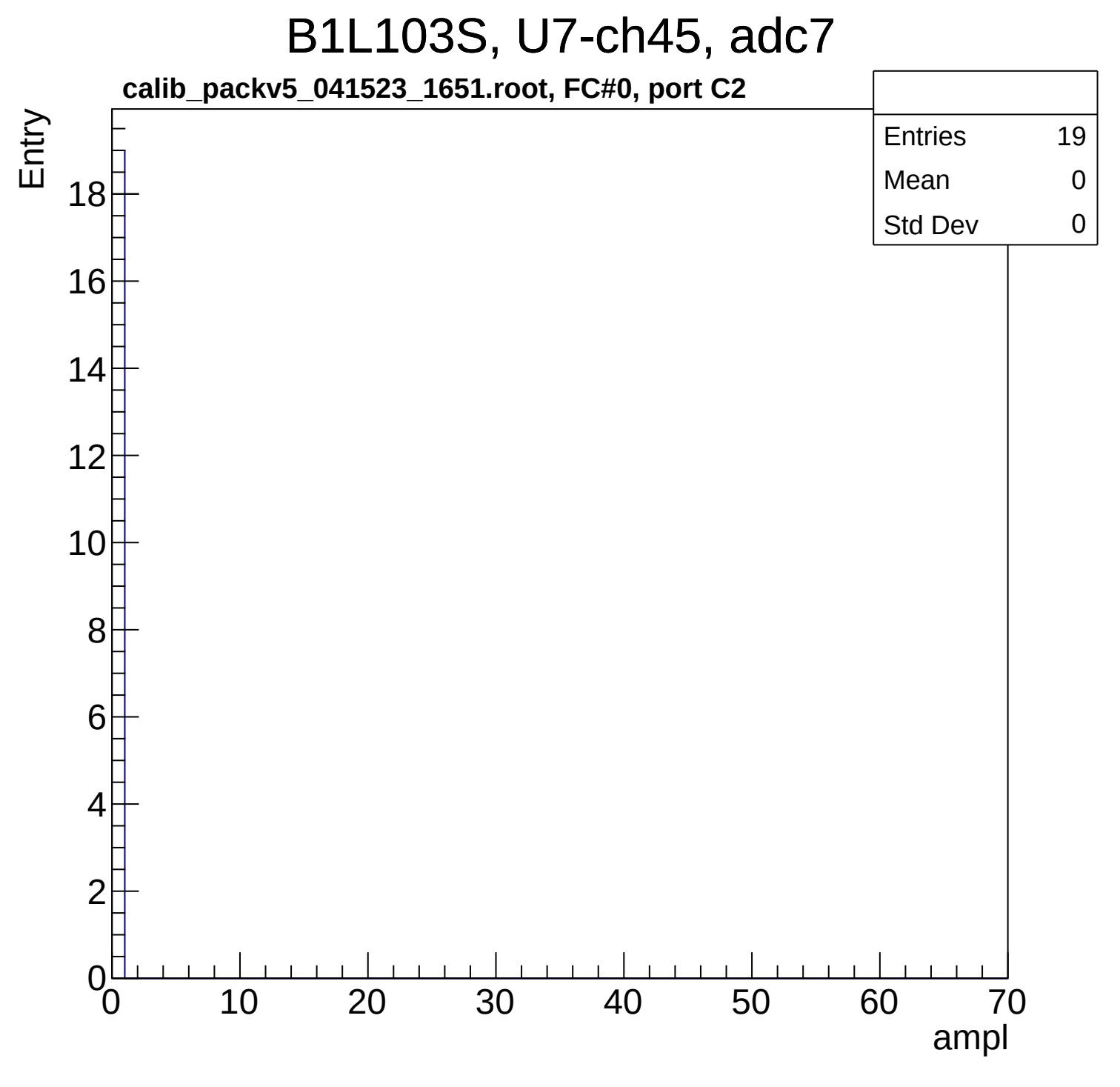
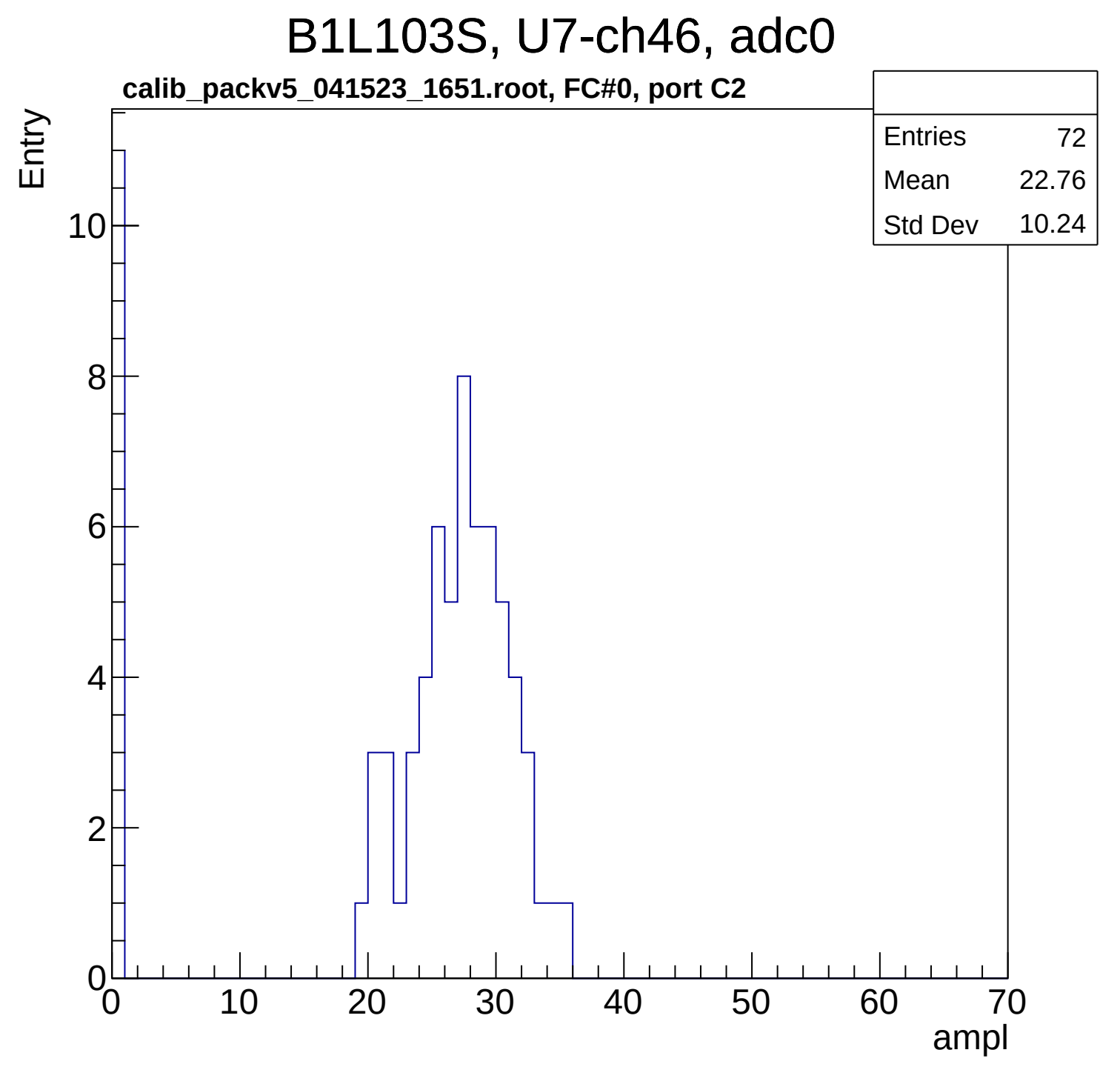
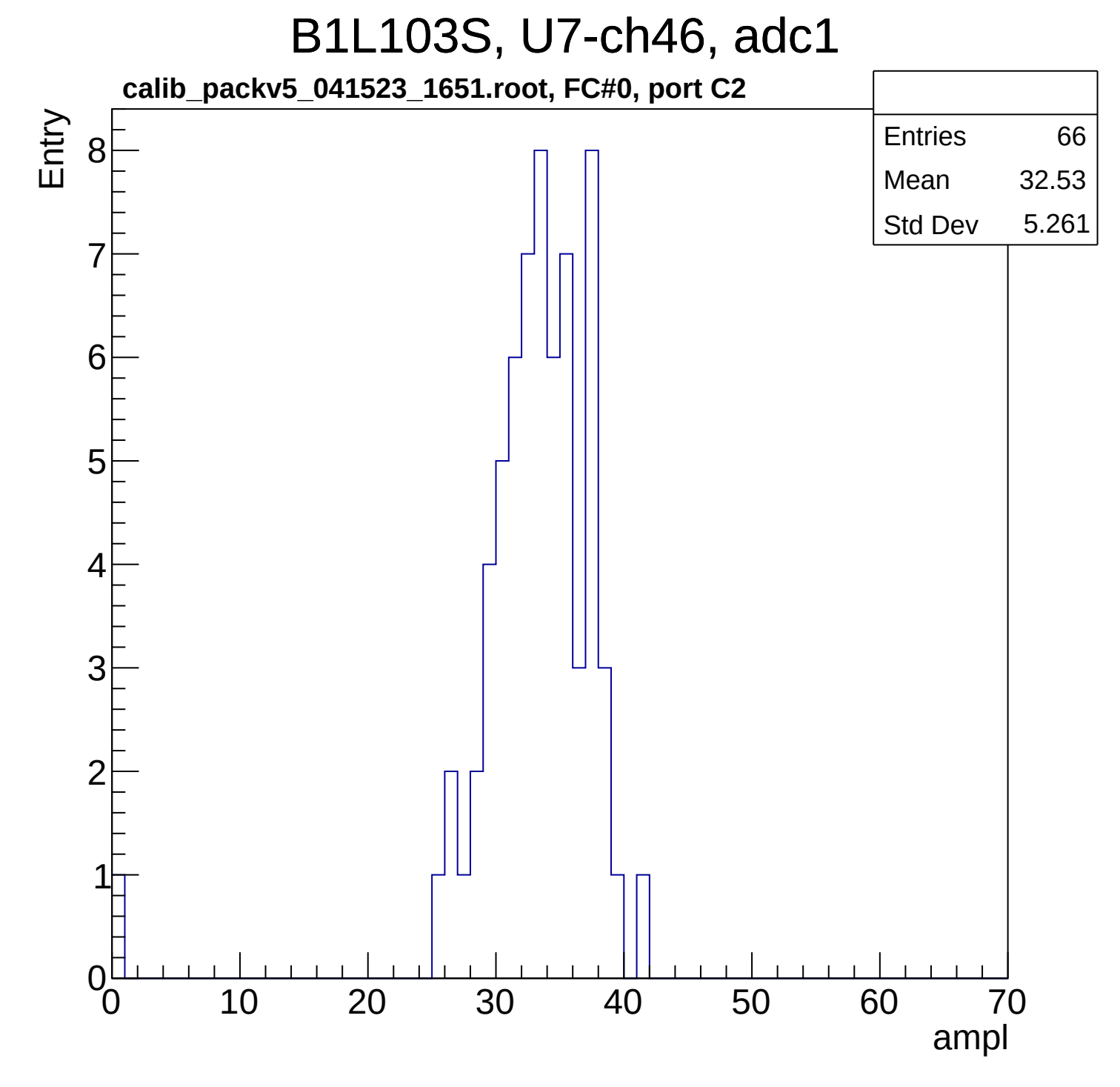
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U7-ch45, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch46, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 22.76
Std Dev 10.24
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch46, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 32.53
Std Dev 5.261
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
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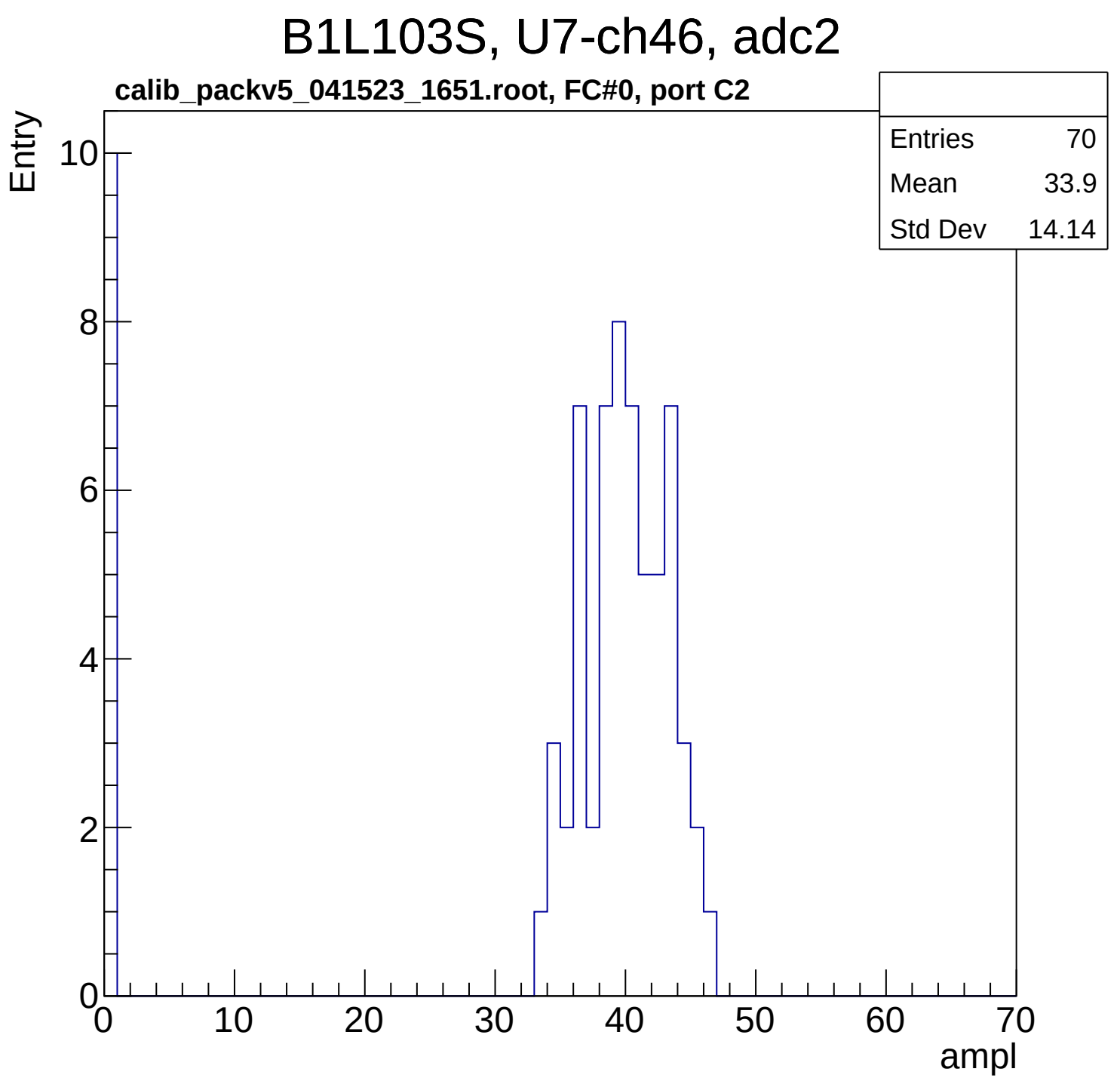
40
50
60
70


B1L103S, U7-ch46, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 33.9
Std Dev 14.14
Entry
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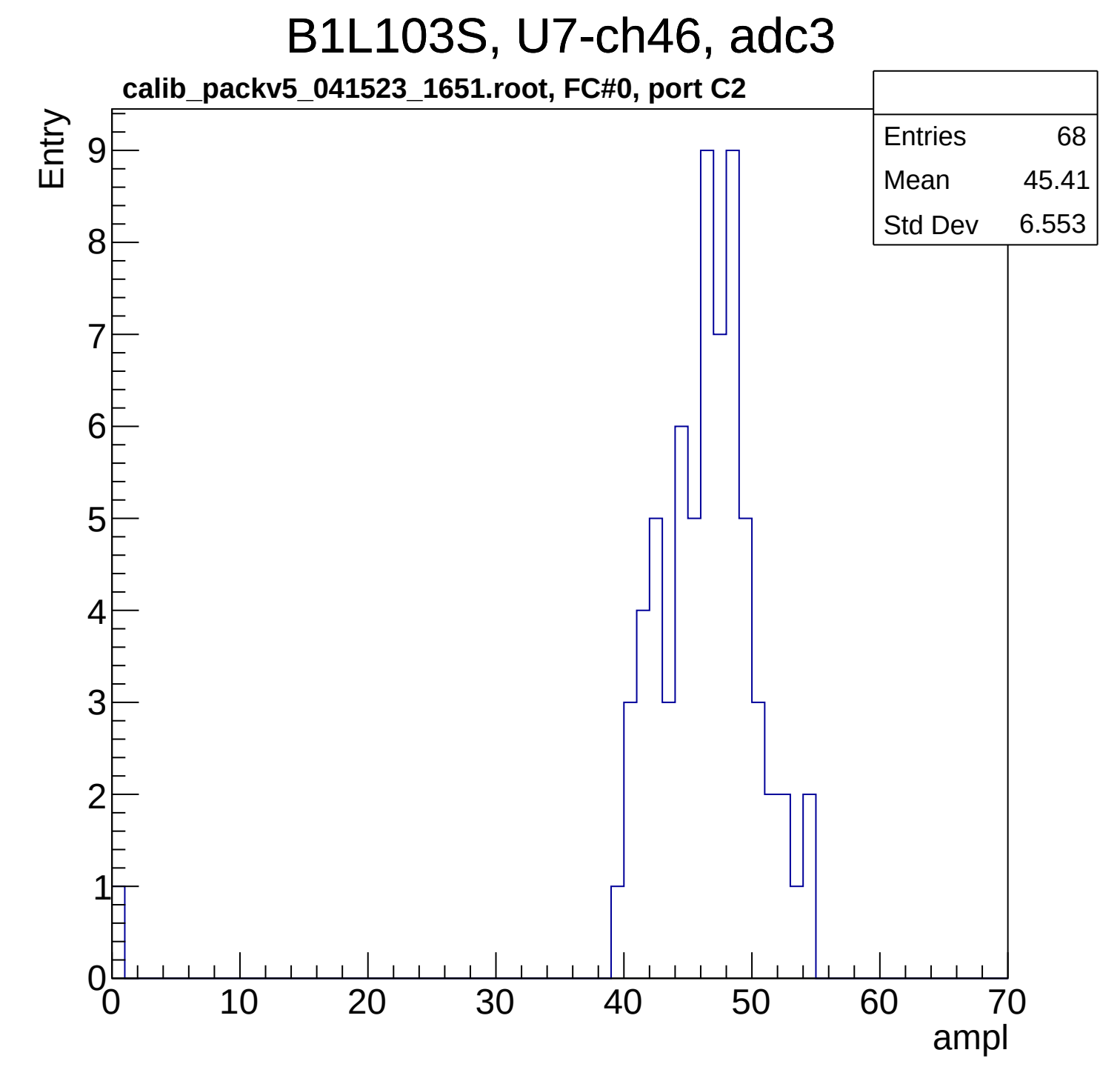
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch46, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 45.41
Std Dev 6.553
Entry
ampl
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3
4
5
6
7
8
9
0
10
20
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40
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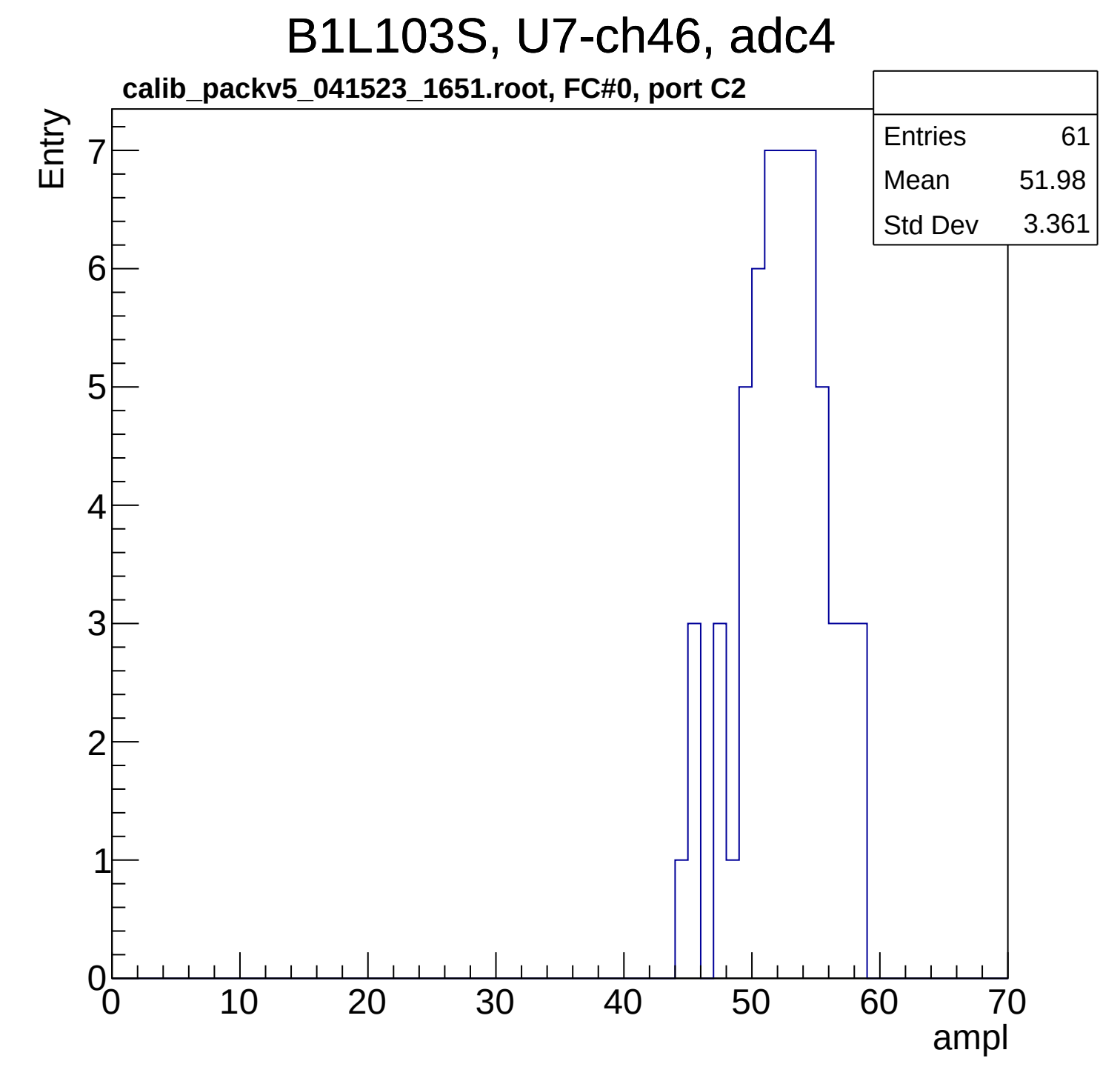
60
70


B1L103S, U7-ch46, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 51.98
Std Dev 3.361
Entry
ampl
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1
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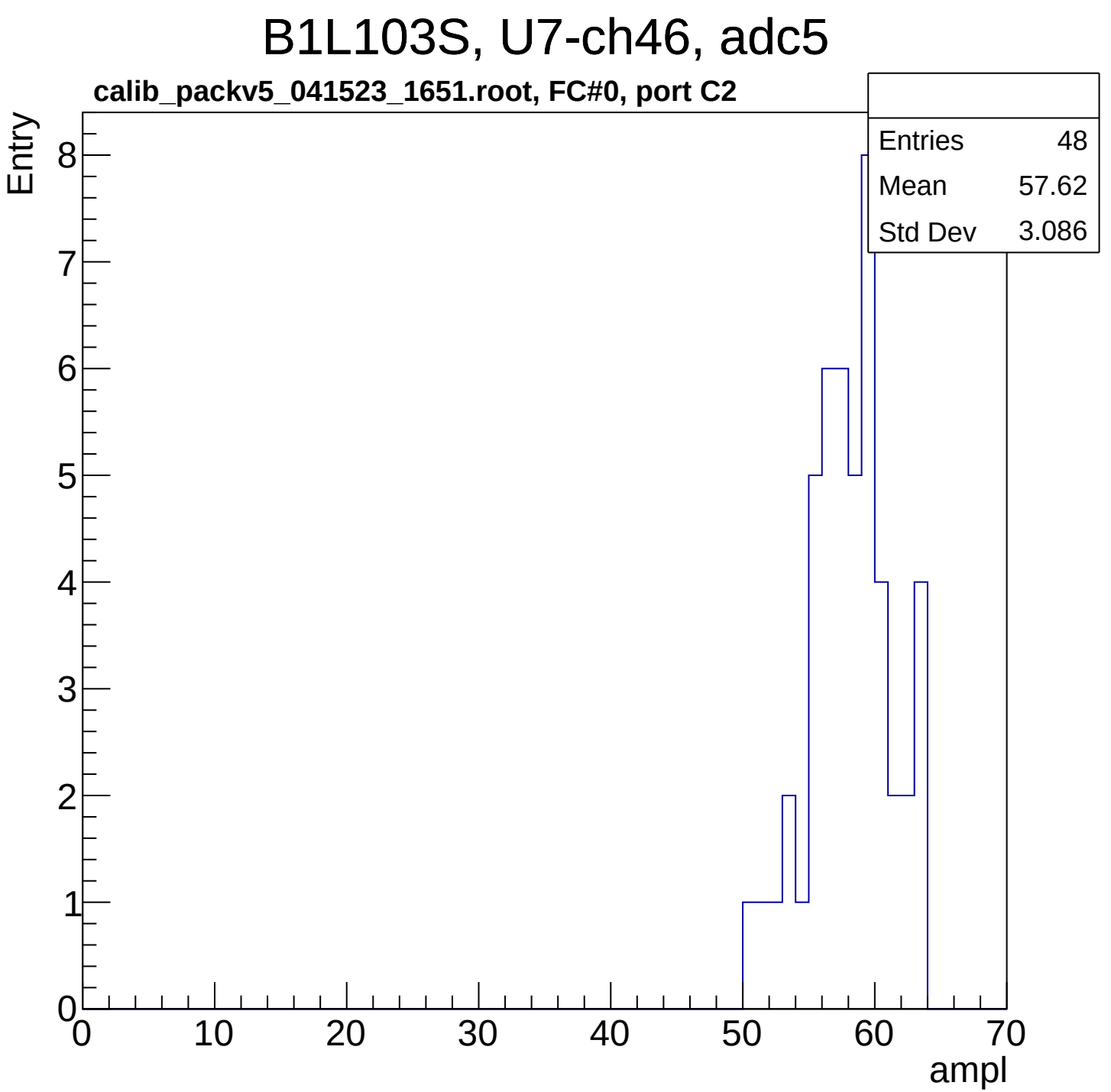
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U7-ch46, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 57.62
Std Dev 3.086
Entry
ampl
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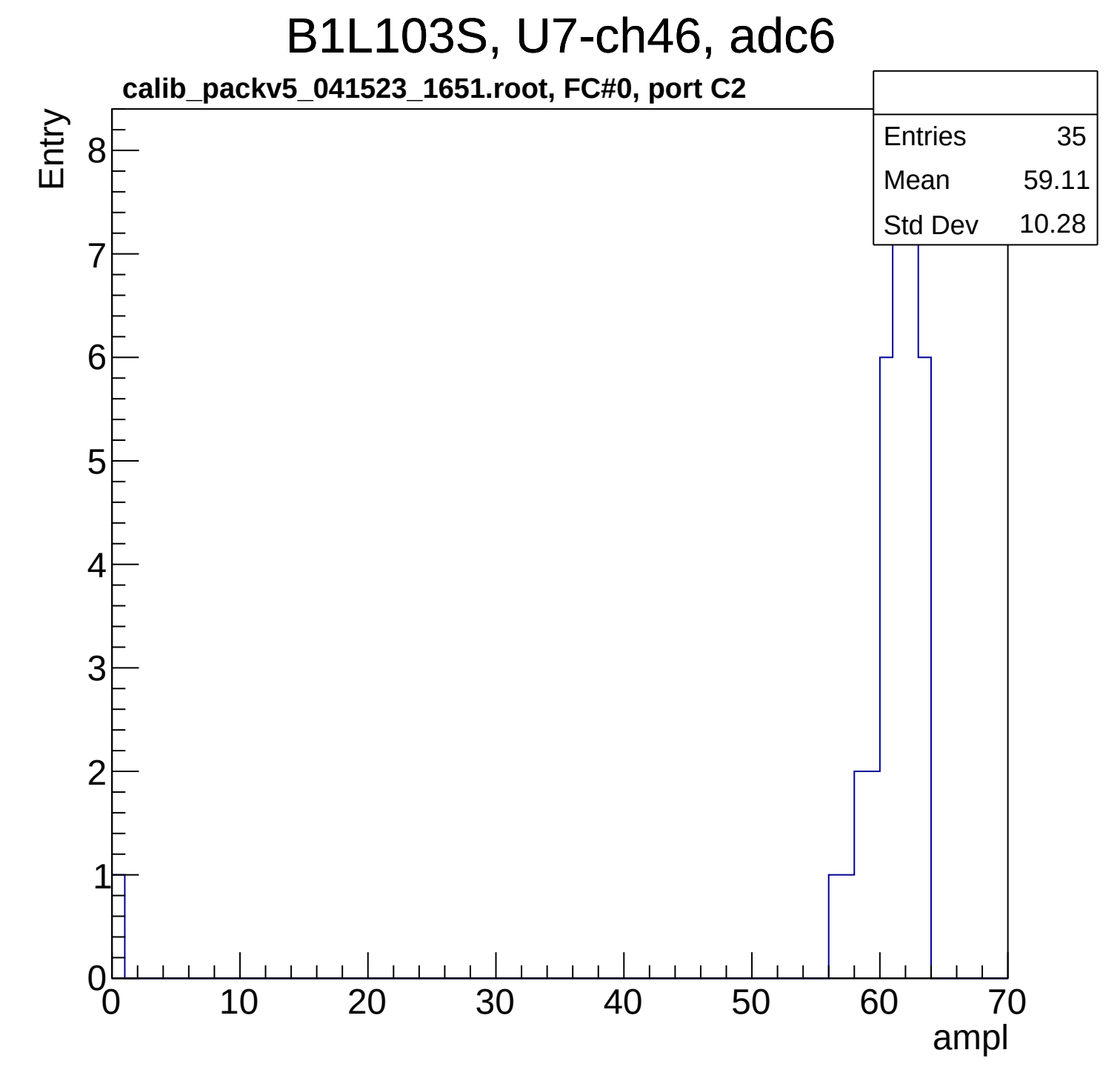
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch46, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 35
Mean 59.11
Std Dev 10.28
Entry
ampl
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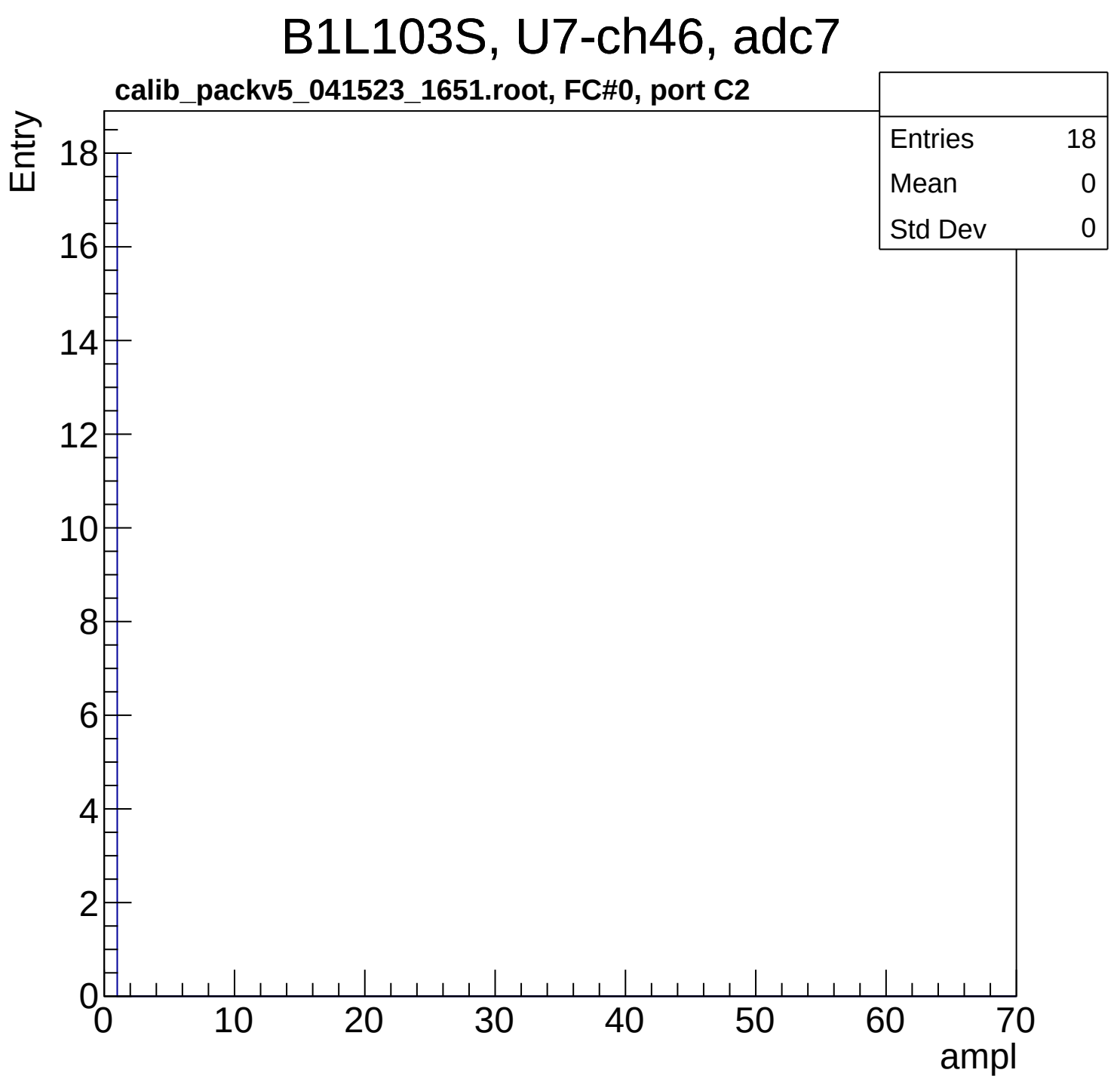
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch46, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
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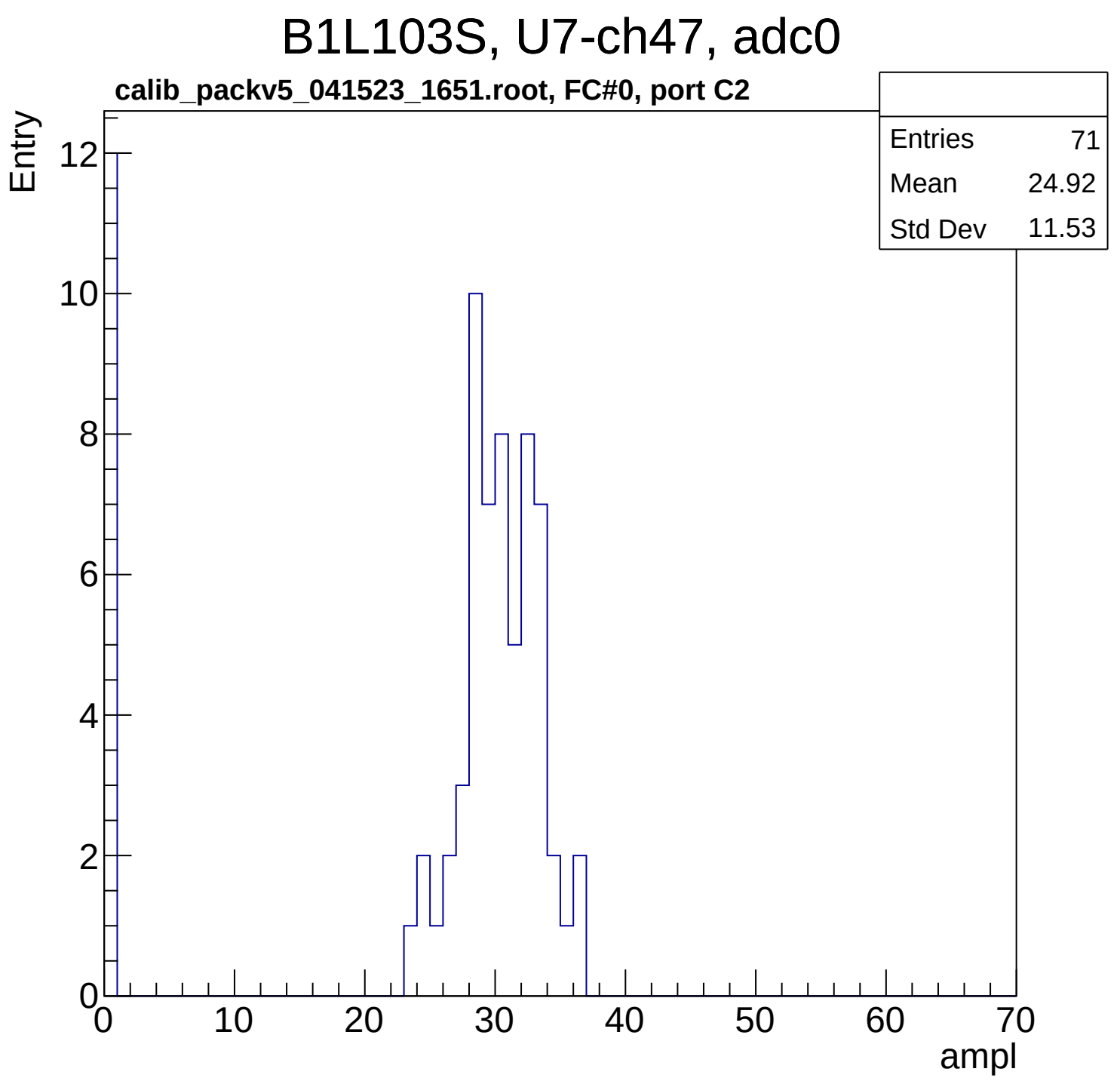
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch47, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 24.92
Std Dev 11.53
Entry
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8
10
12
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10
20
30
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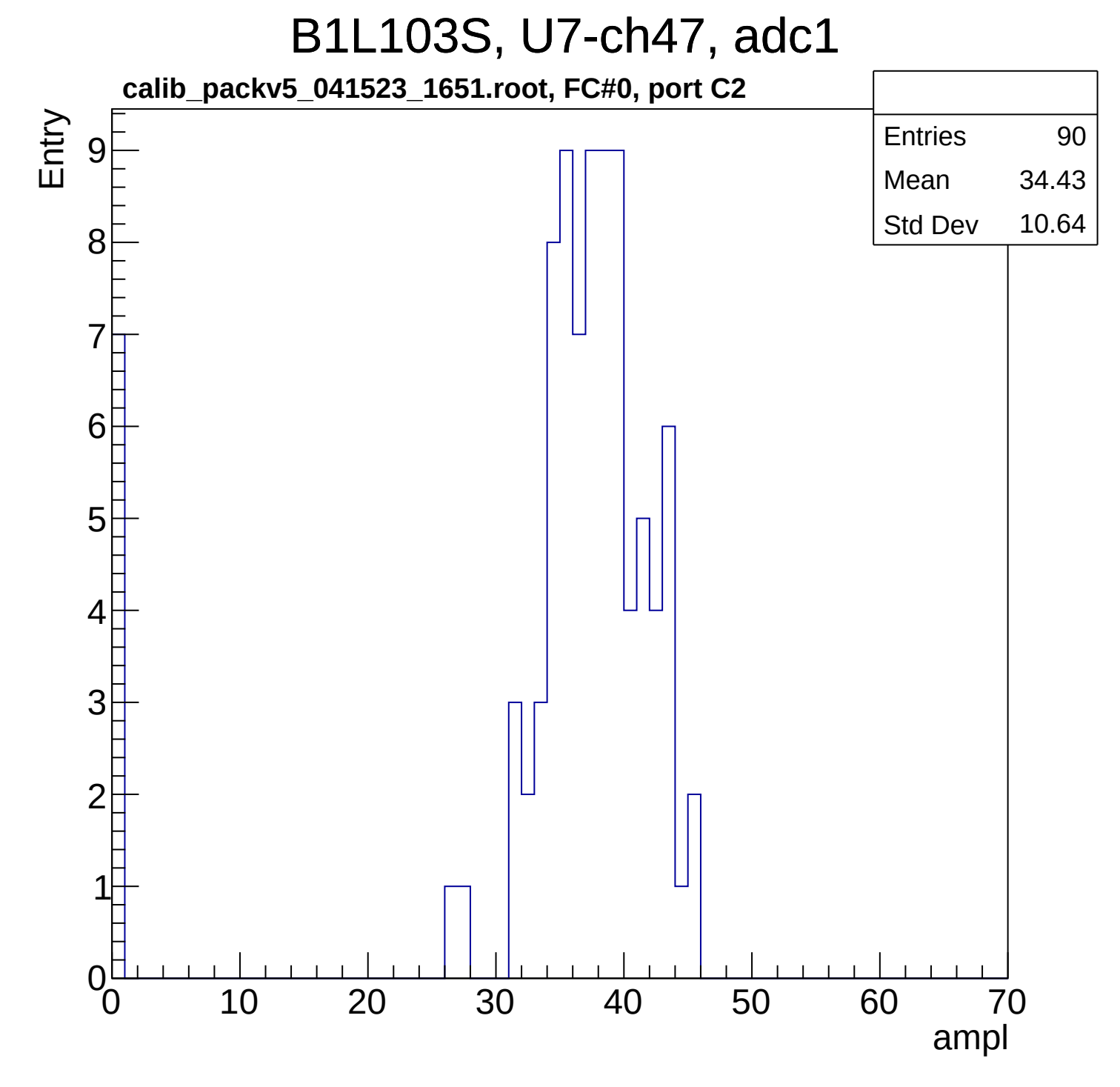
50
60
70
ampl


B1L103S, U7-ch47, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 90
Mean 34.43
Std Dev 10.64
Entry
ampl
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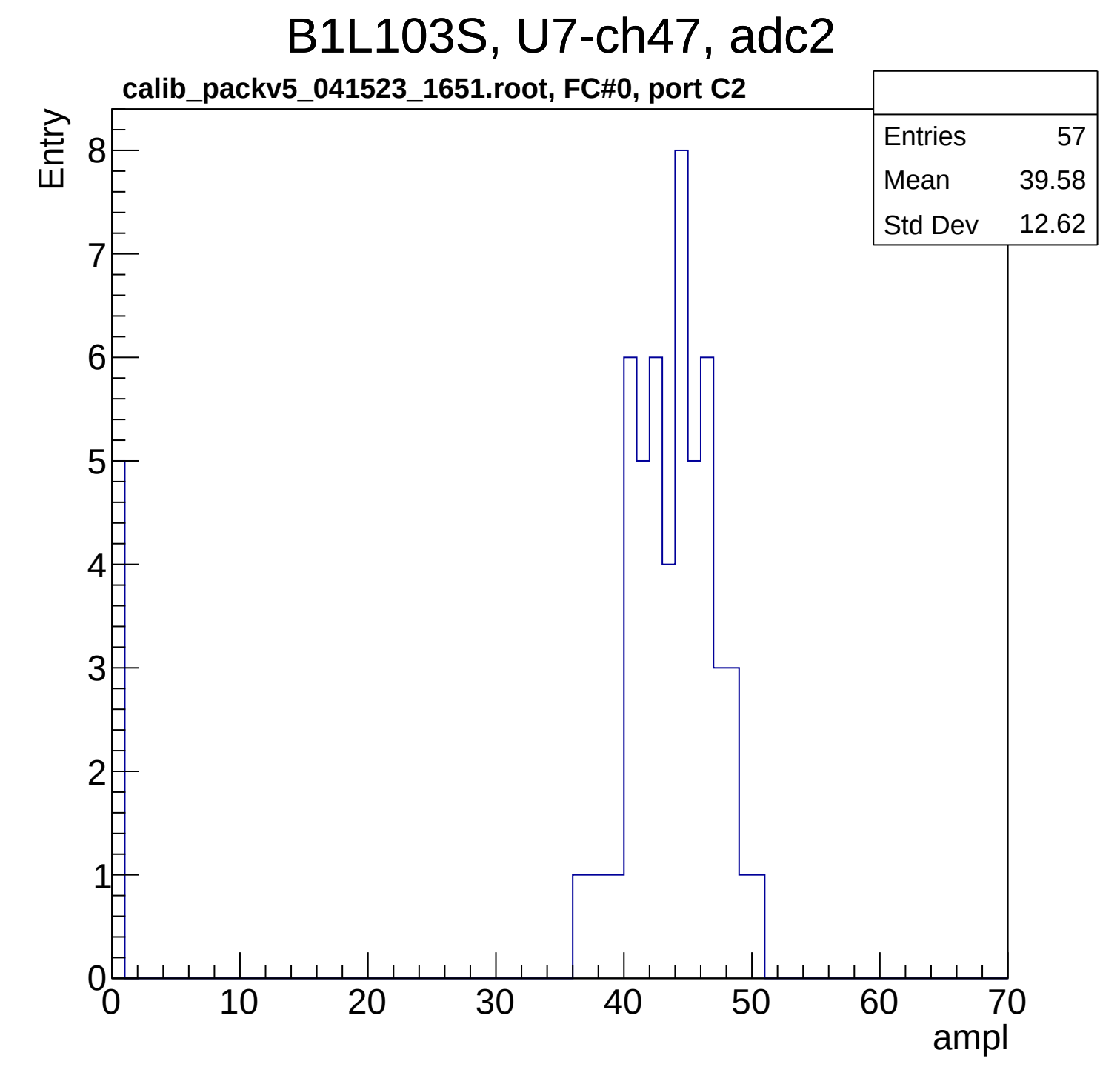
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U7-ch47, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 39.58
Std Dev 12.62
Entry
ampl
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4
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40
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60
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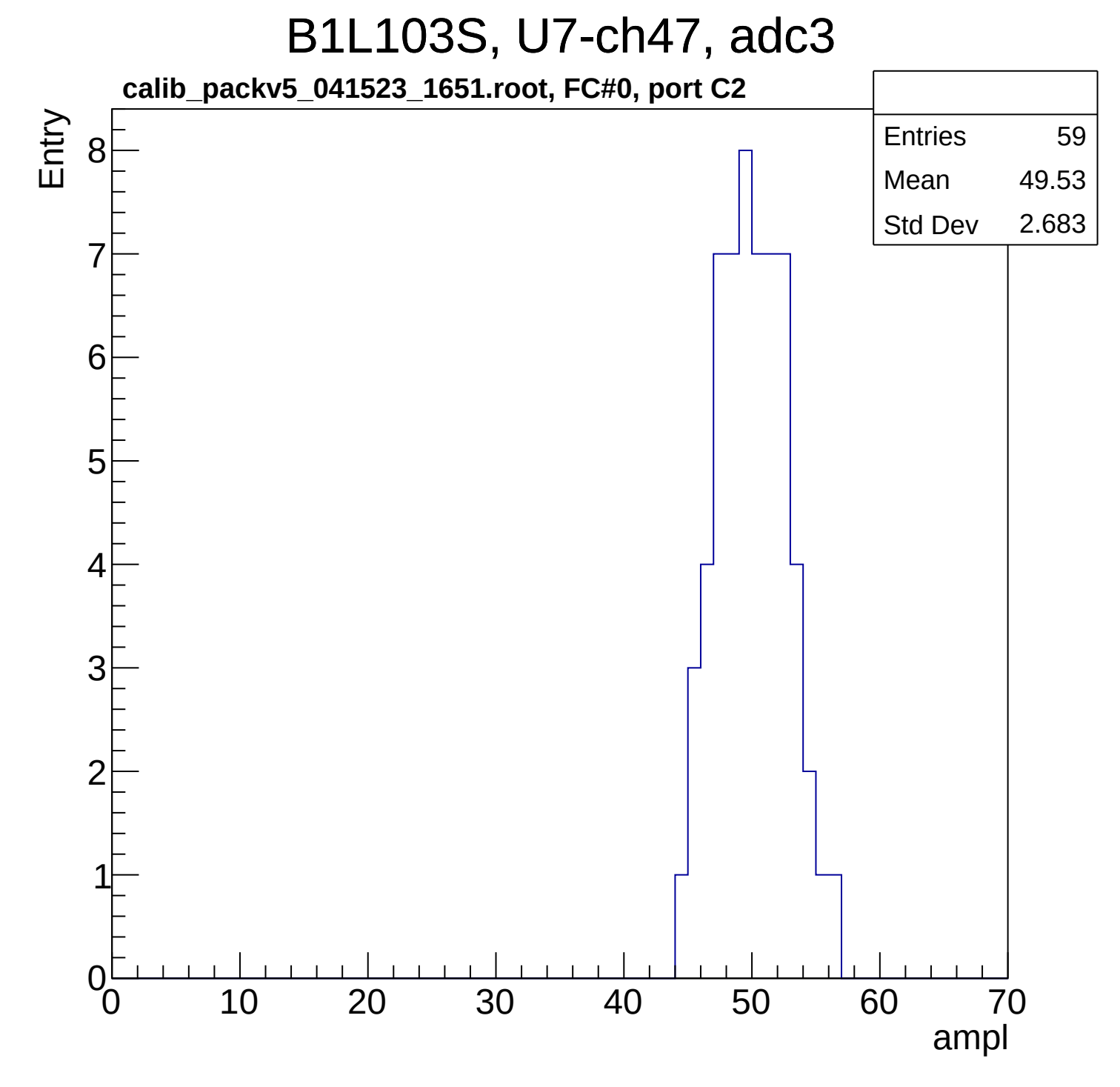
B1L103S, U7-ch47, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 49.53
Std Dev 2.683
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
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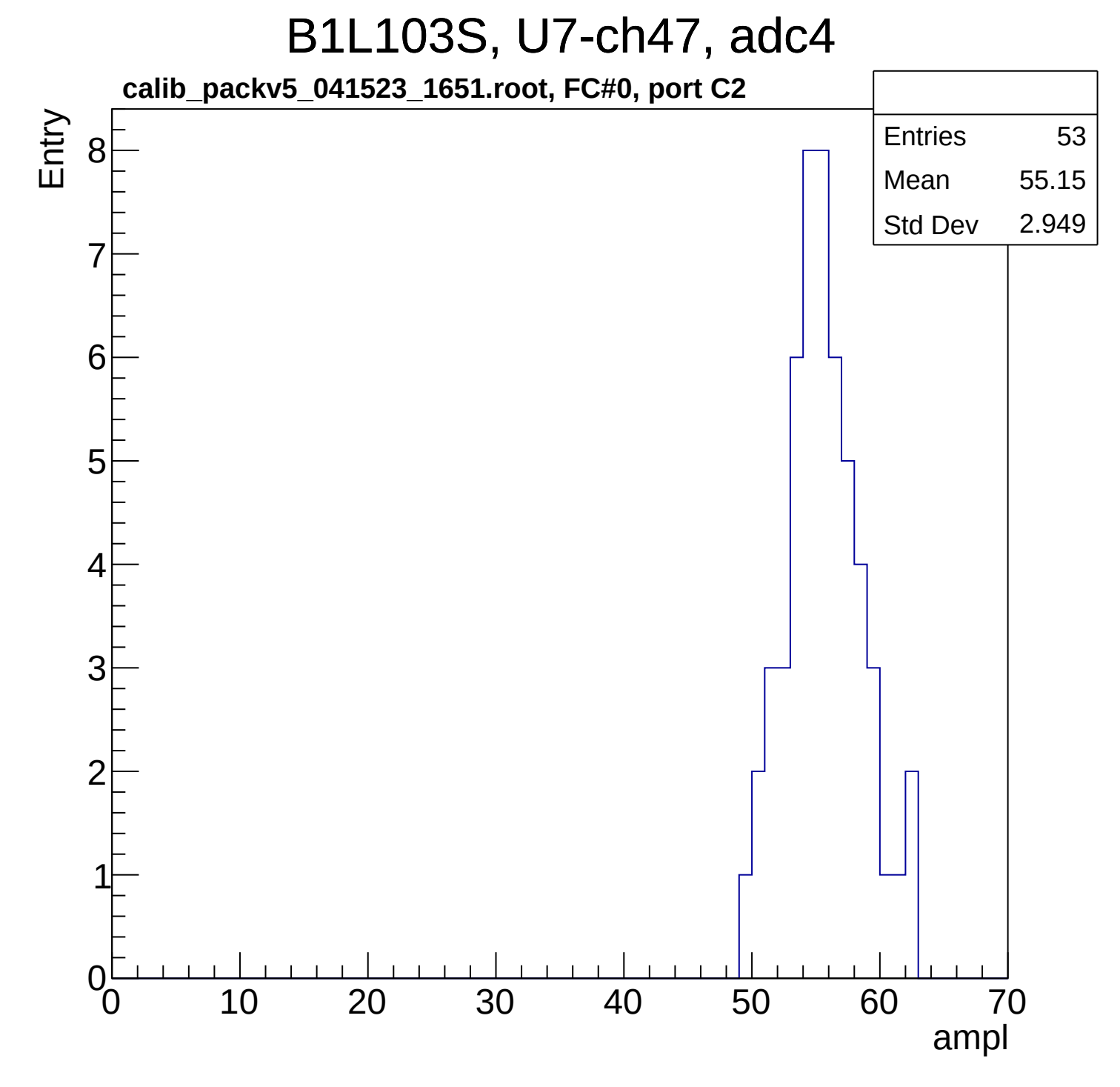
40
50
60
70


B1L103S, U7-ch47, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 55.15
Std Dev 2.949
Entry
ampl
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5
6
7
8
0
10
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40
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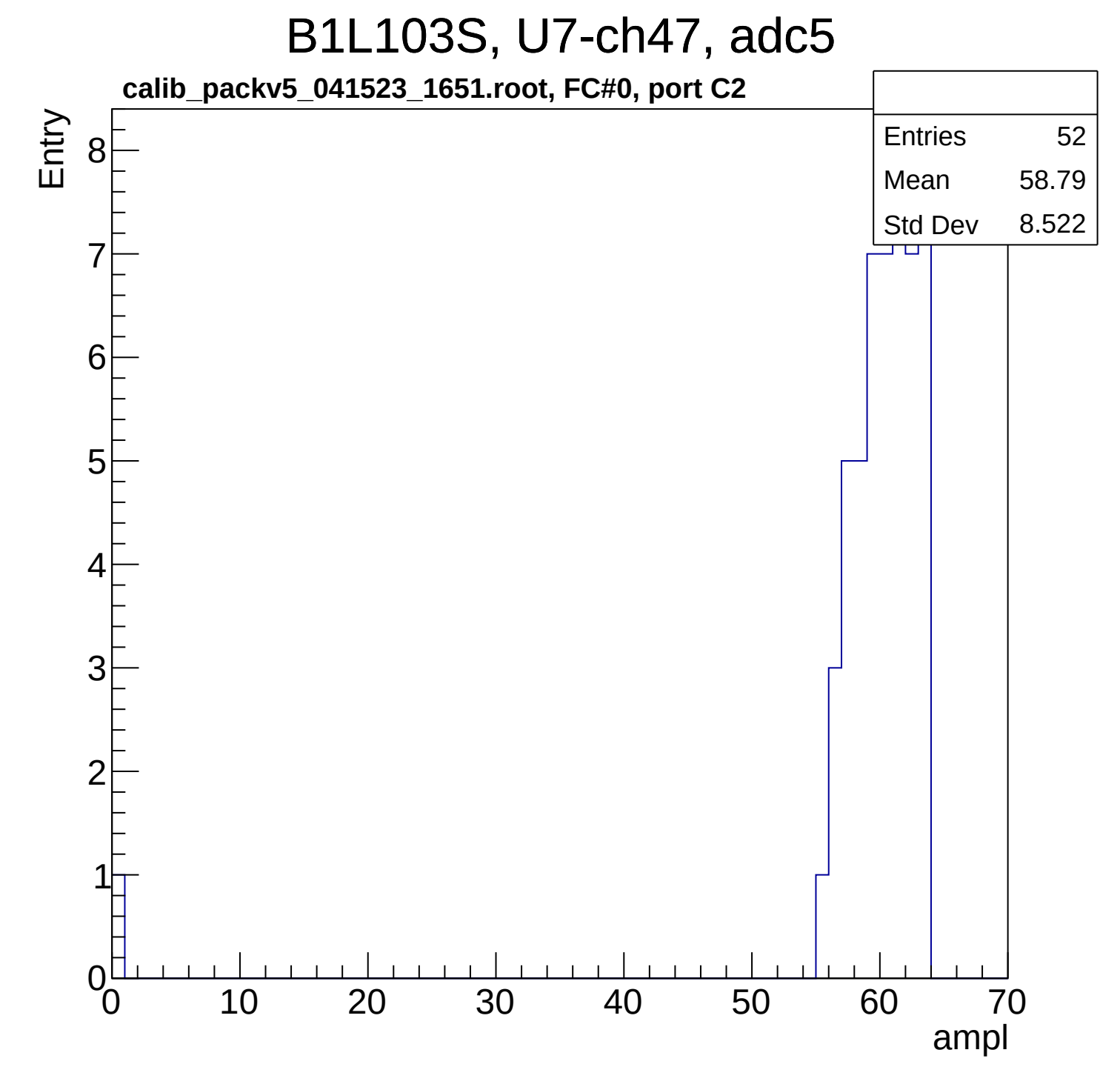
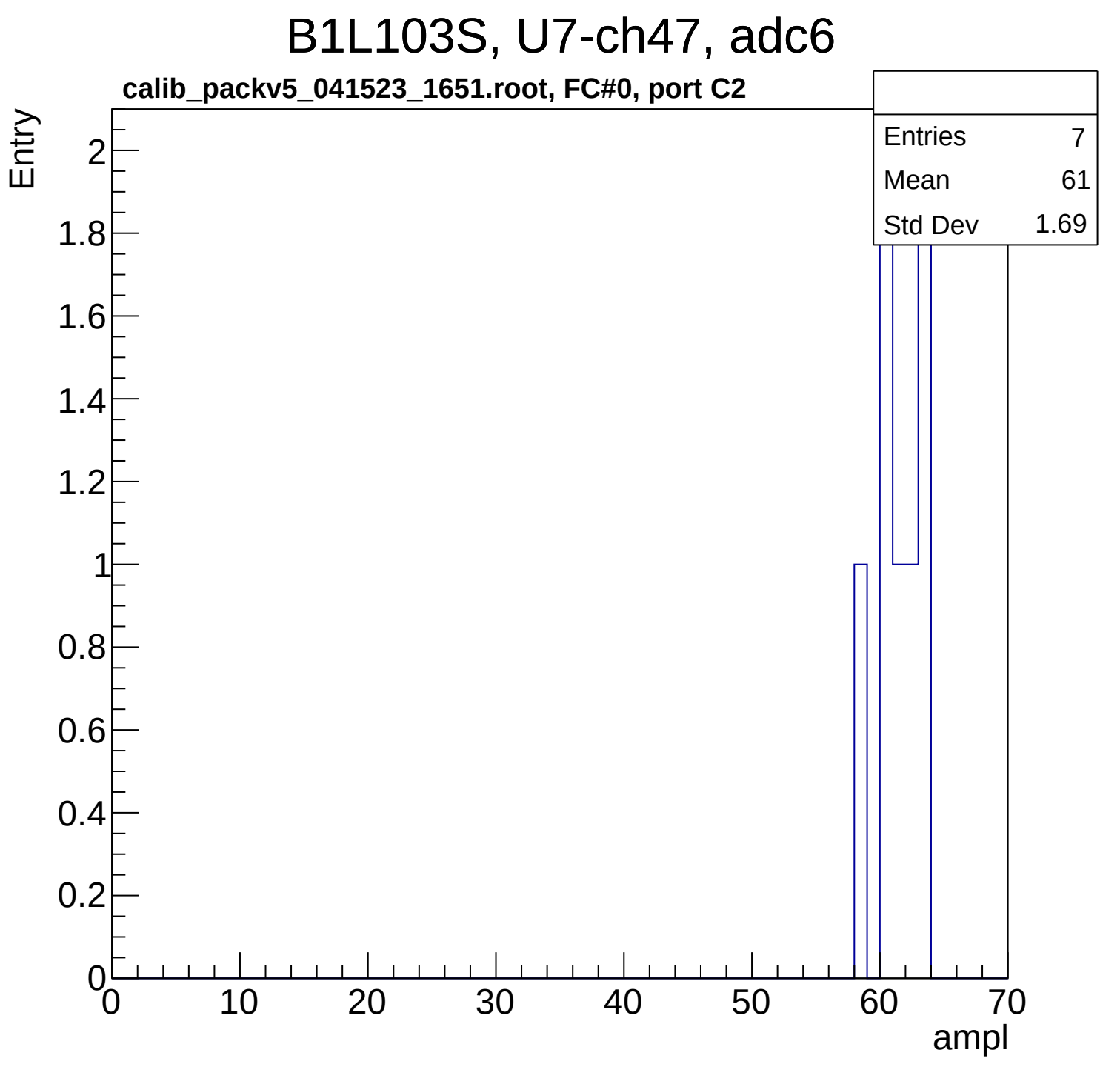

B1L103S, U7-ch47, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 58.79
Std Dev 8.522
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch47, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 61
Std Dev 1.69
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
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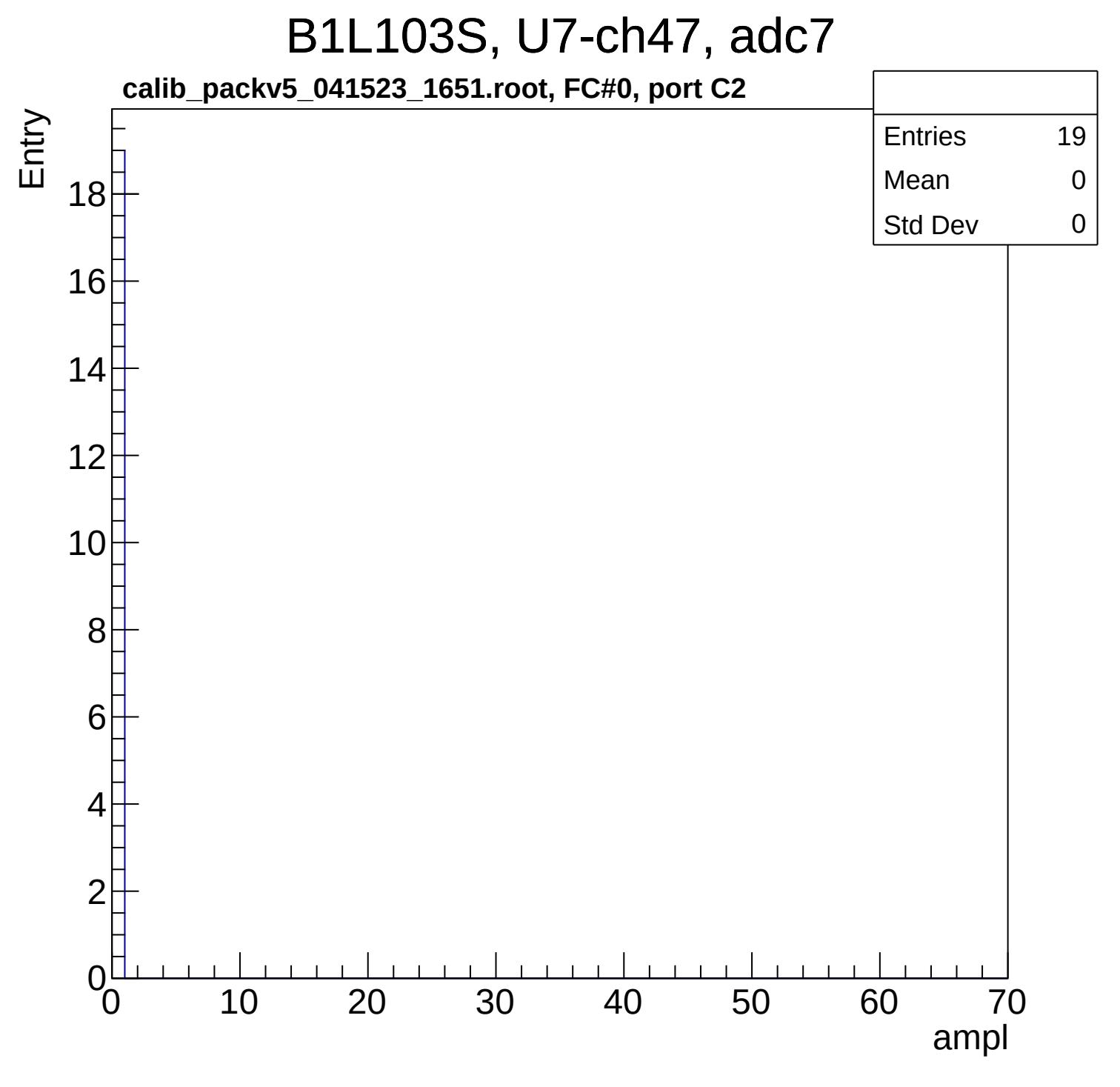
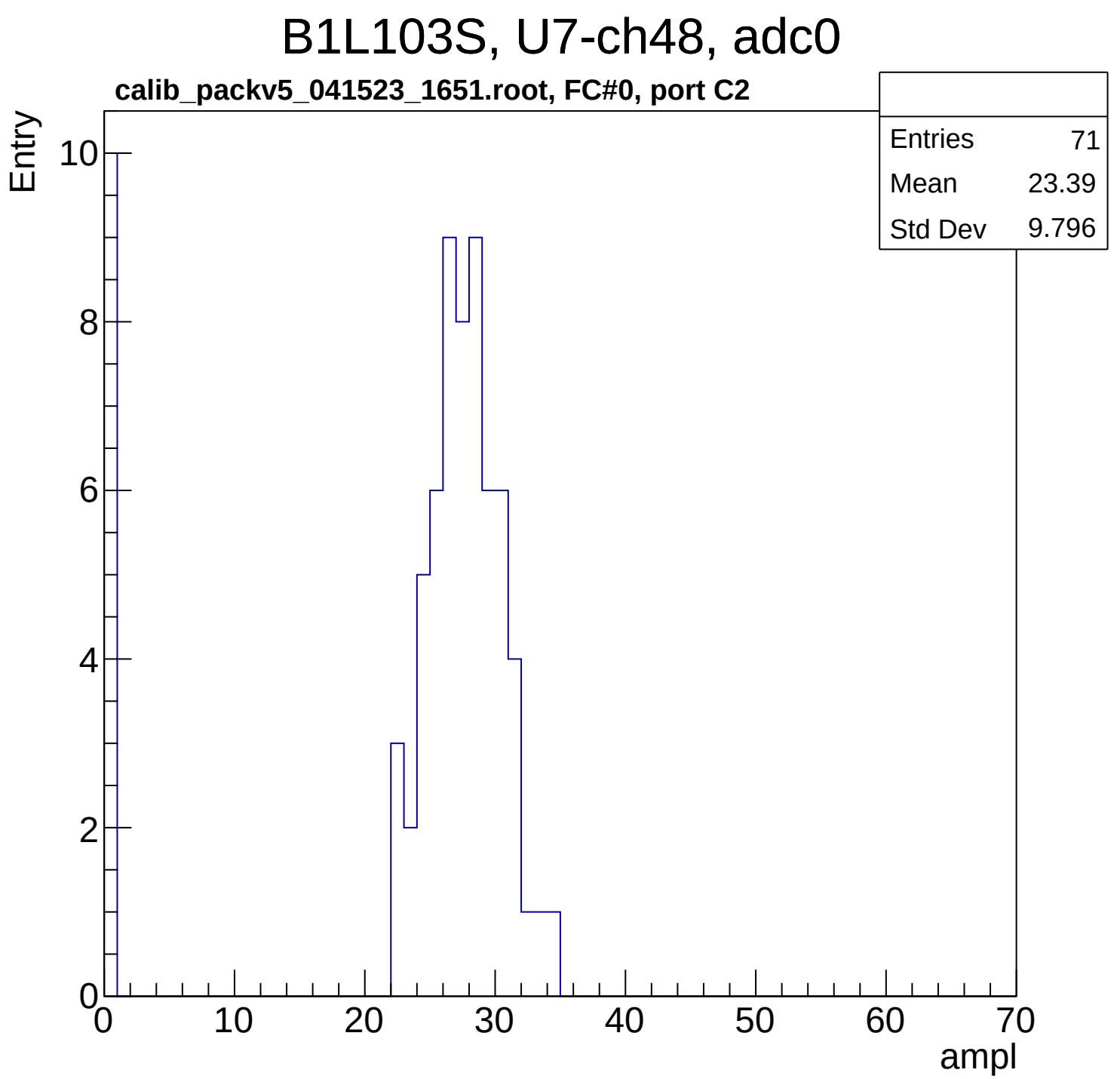
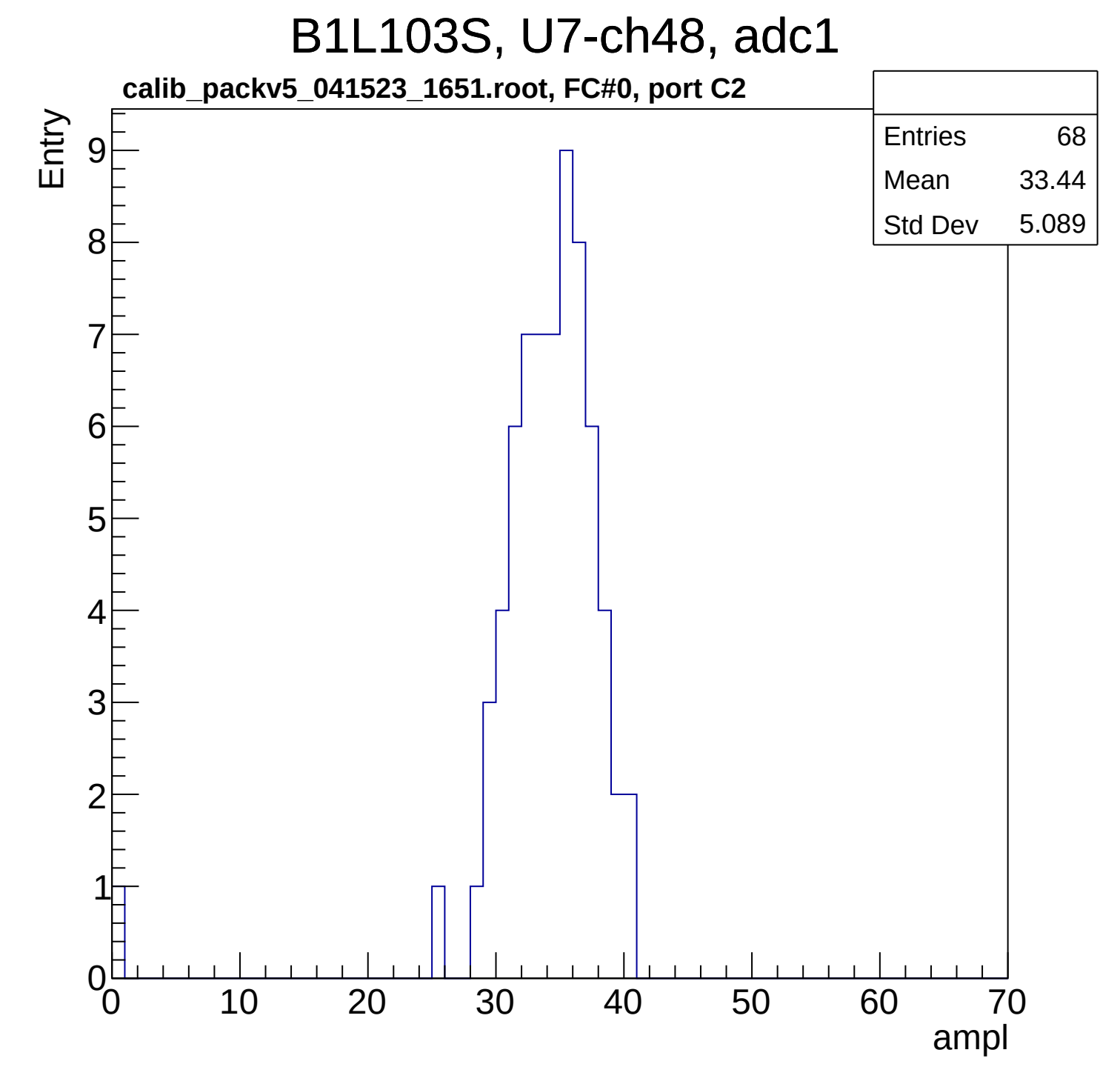
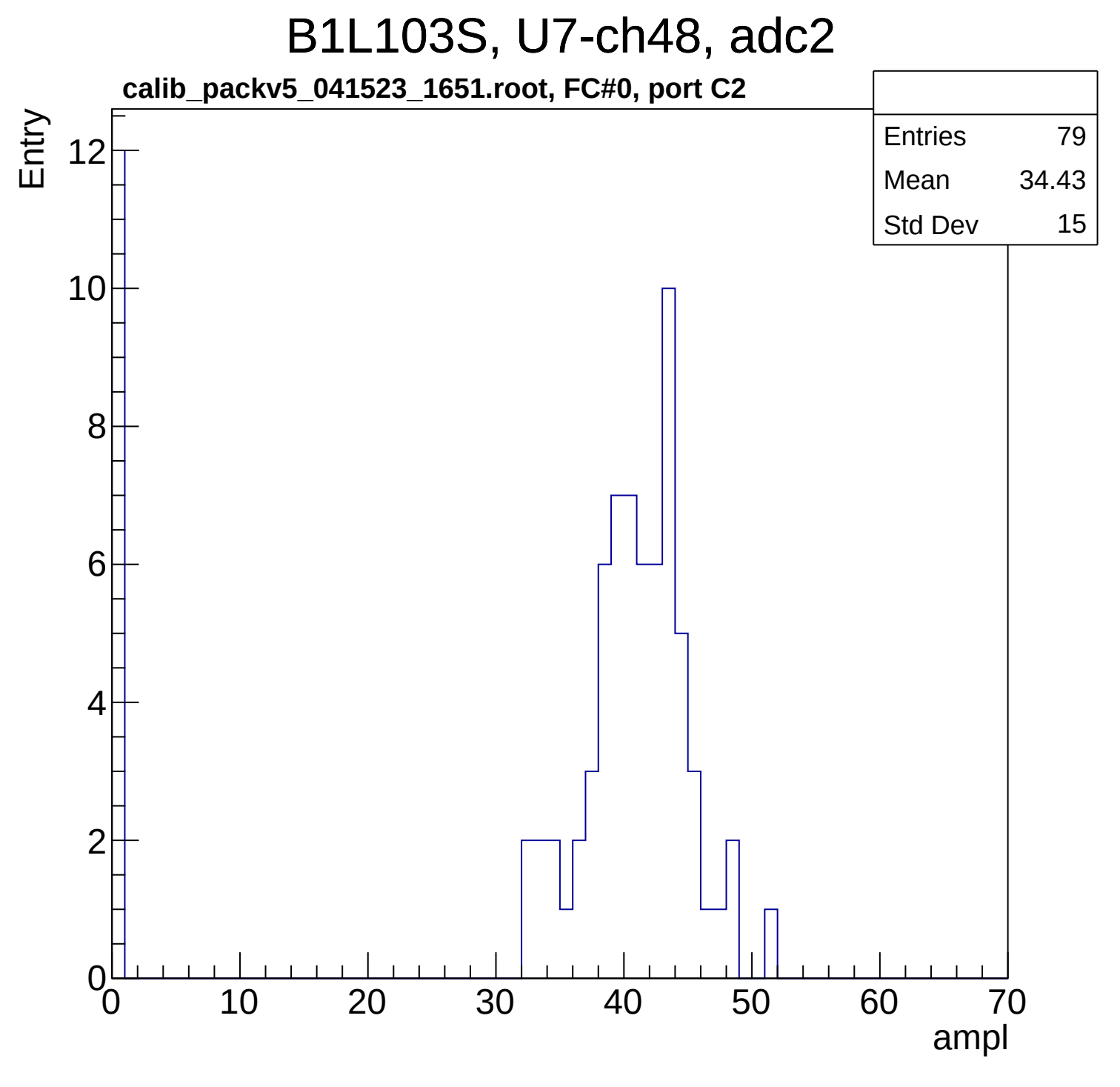
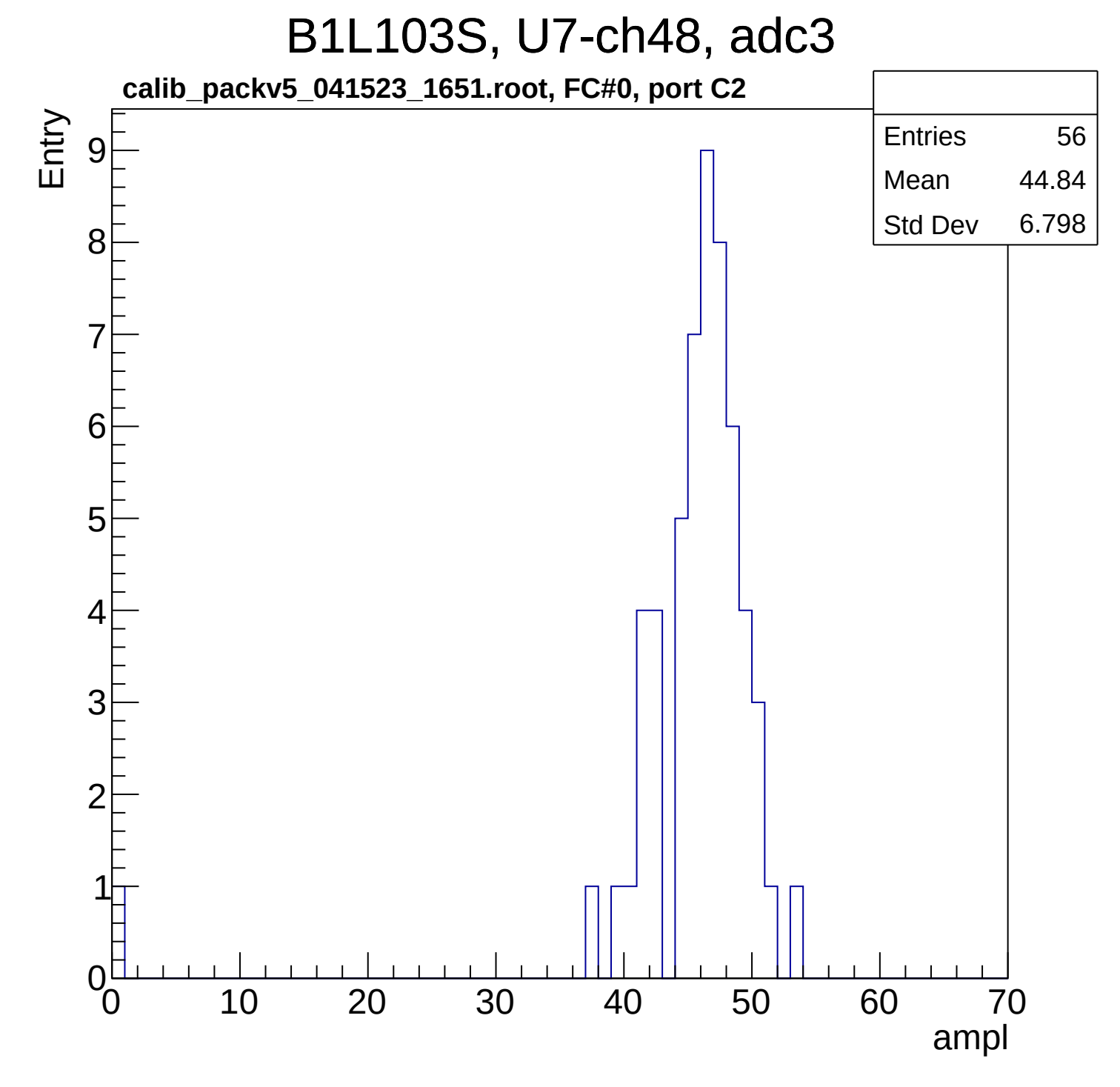
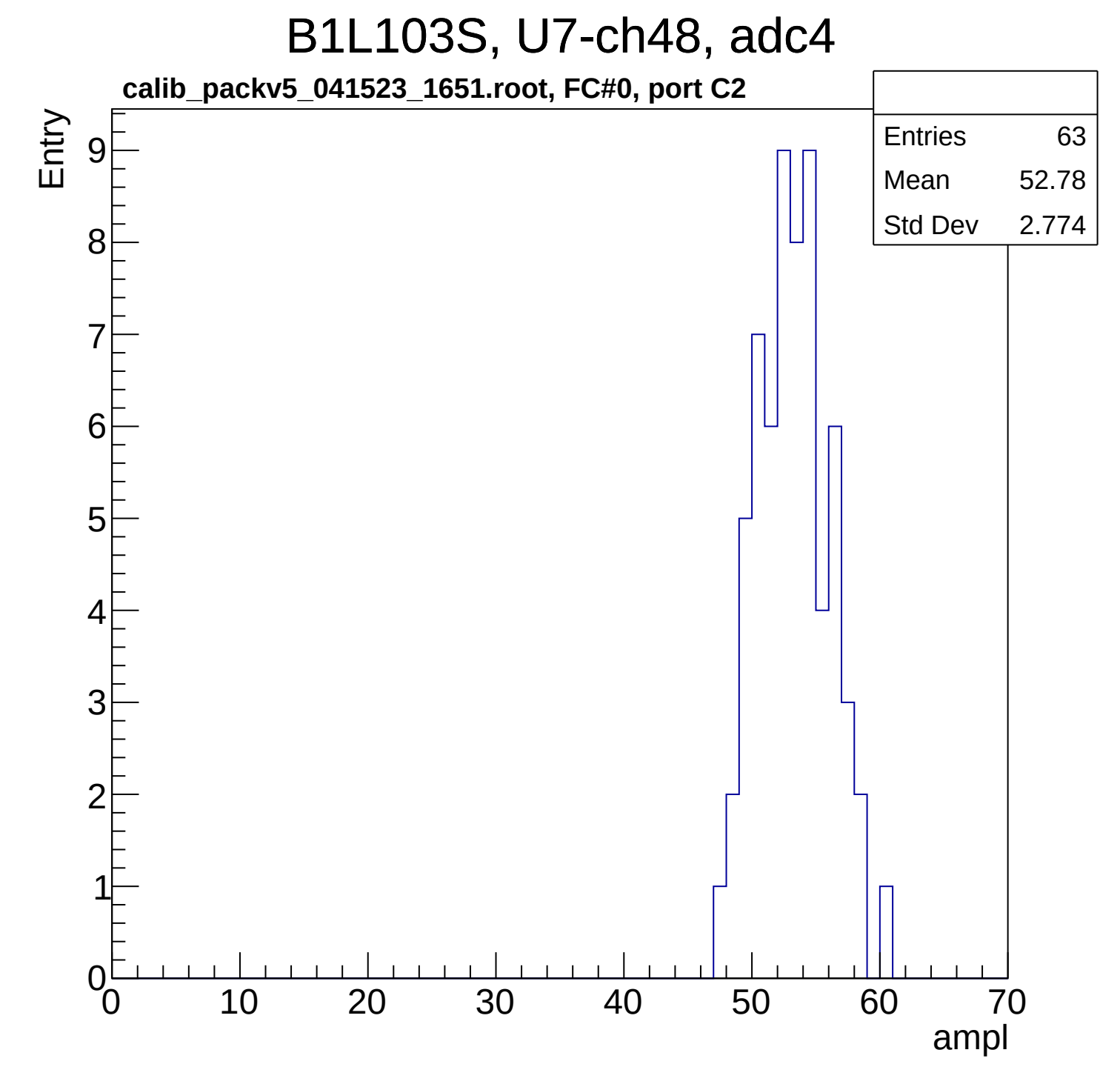

B1L103S, U7-ch47, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

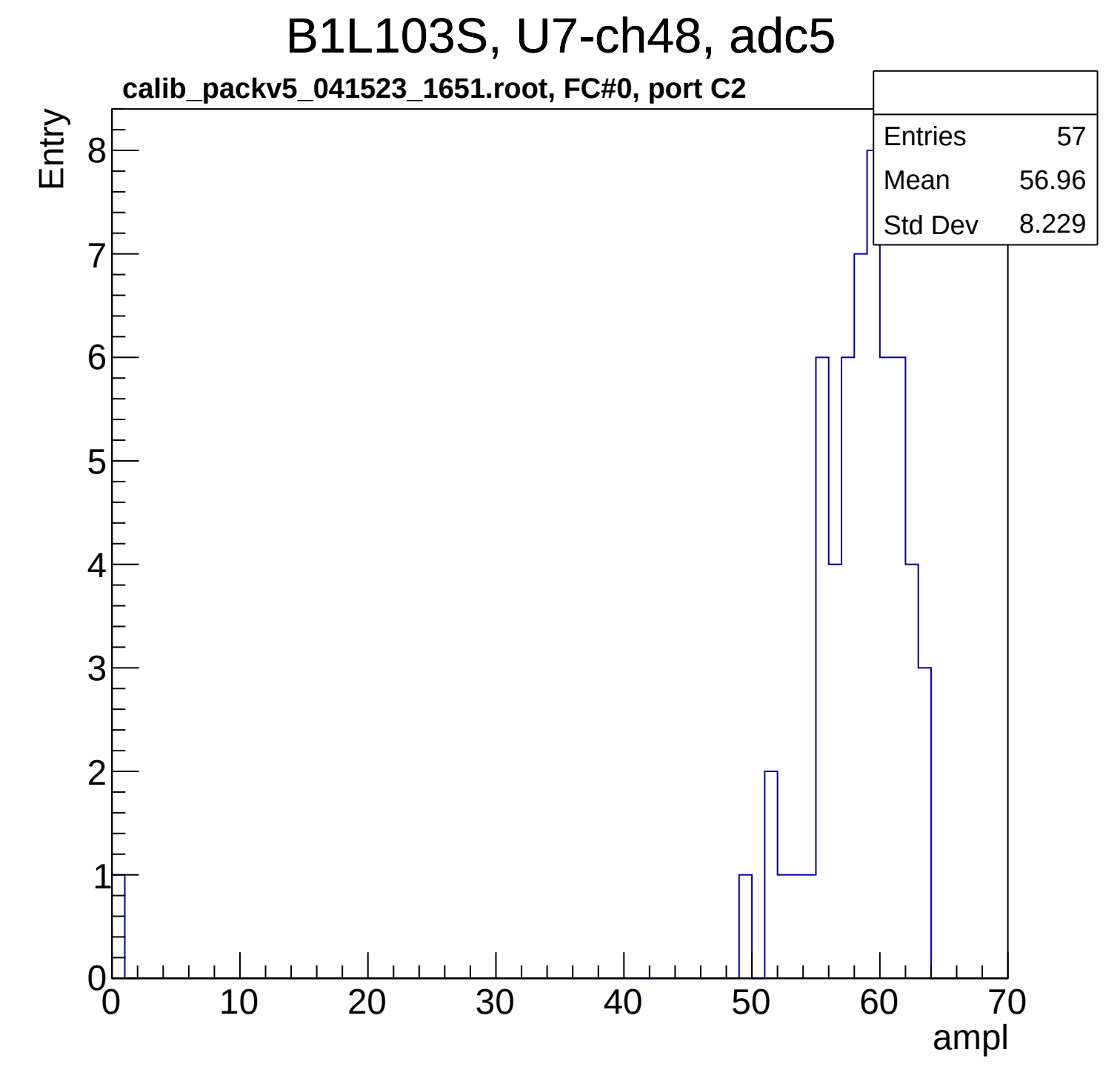

B1L103S, U7-ch48, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 23.39
Std Dev 9.796
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

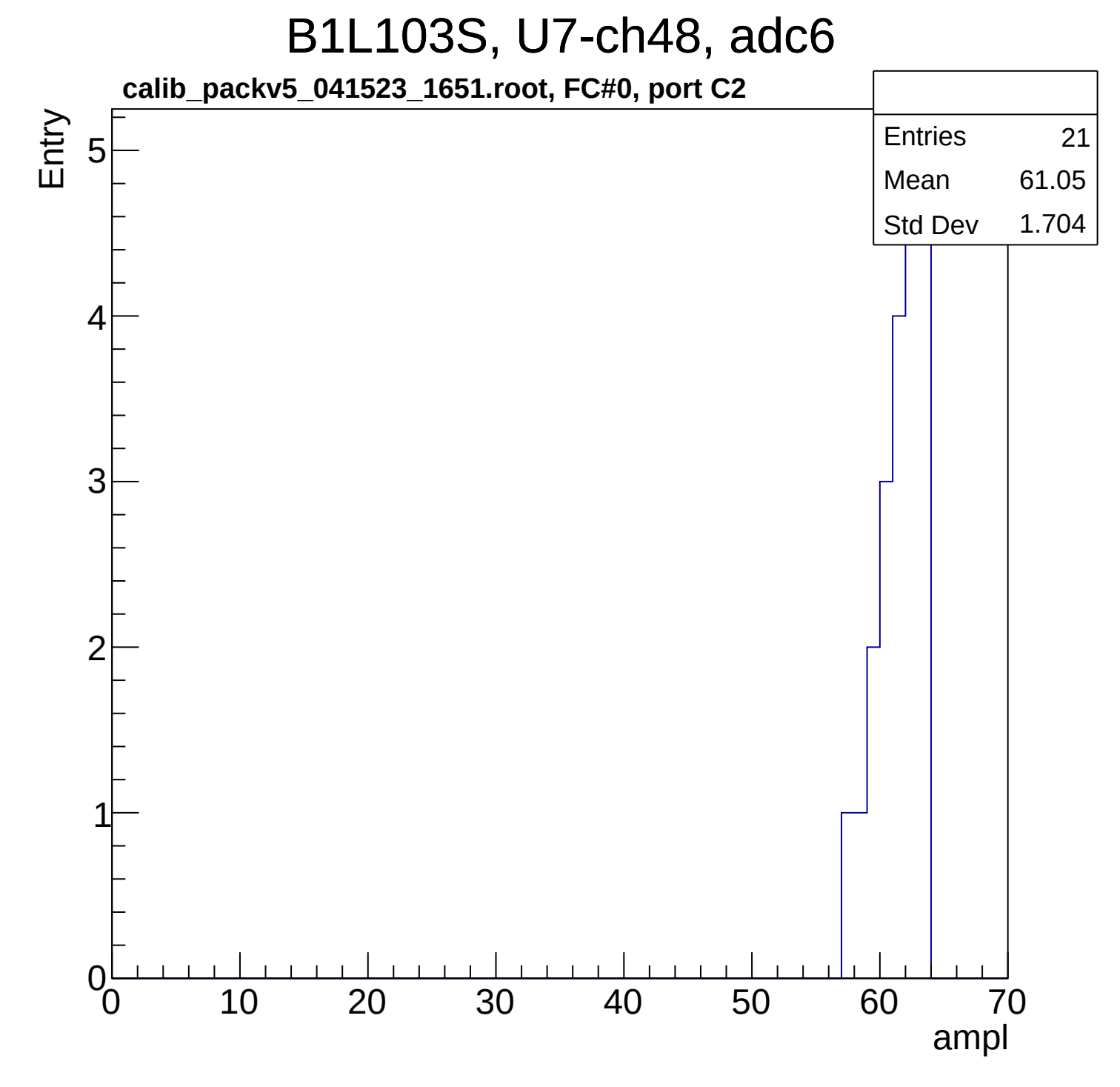

B1L103S, U7-ch48, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 33.44
Std Dev 5.089
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

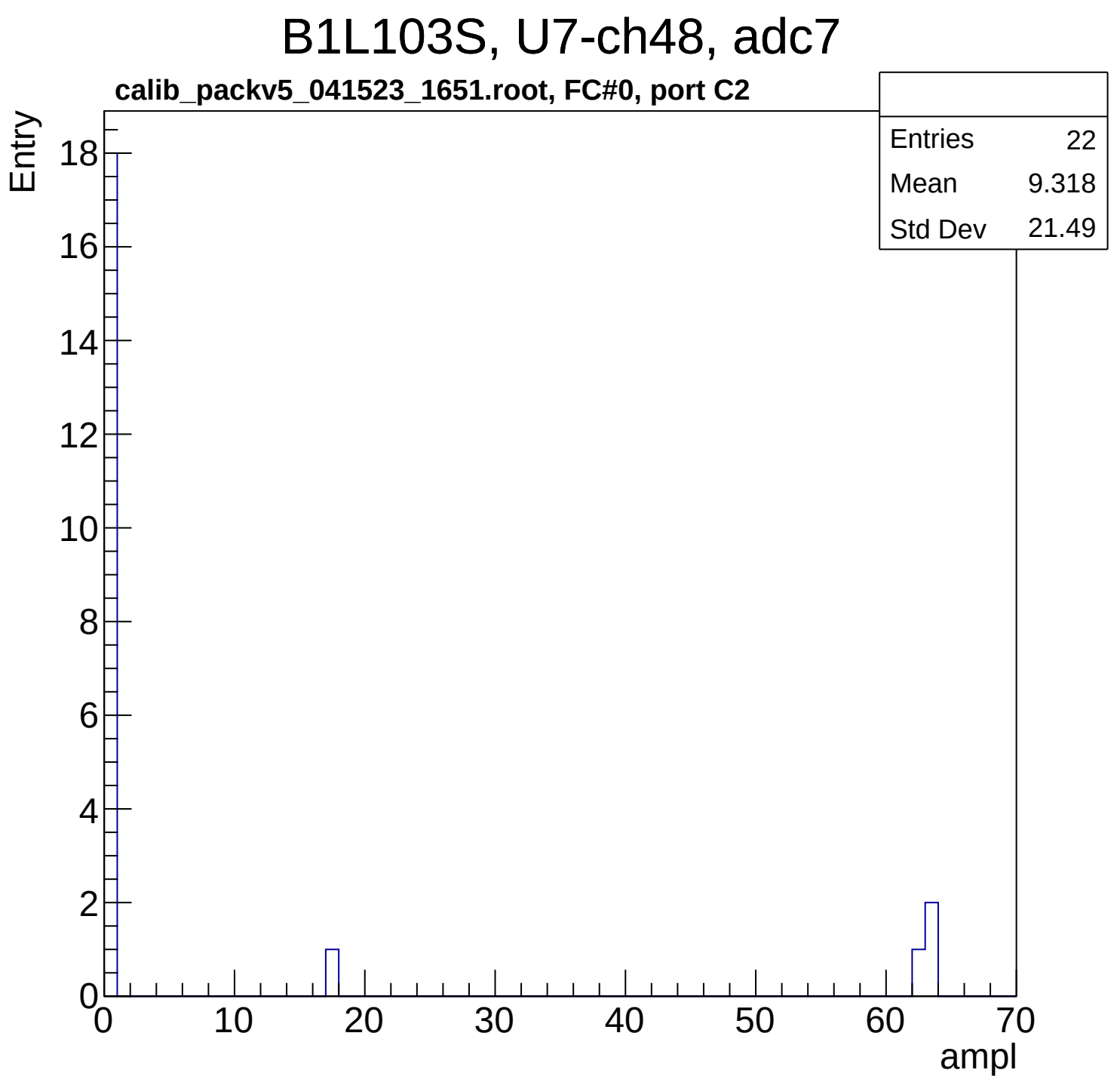

B1L103S, U7-ch48, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 34.43
Std Dev 15
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70

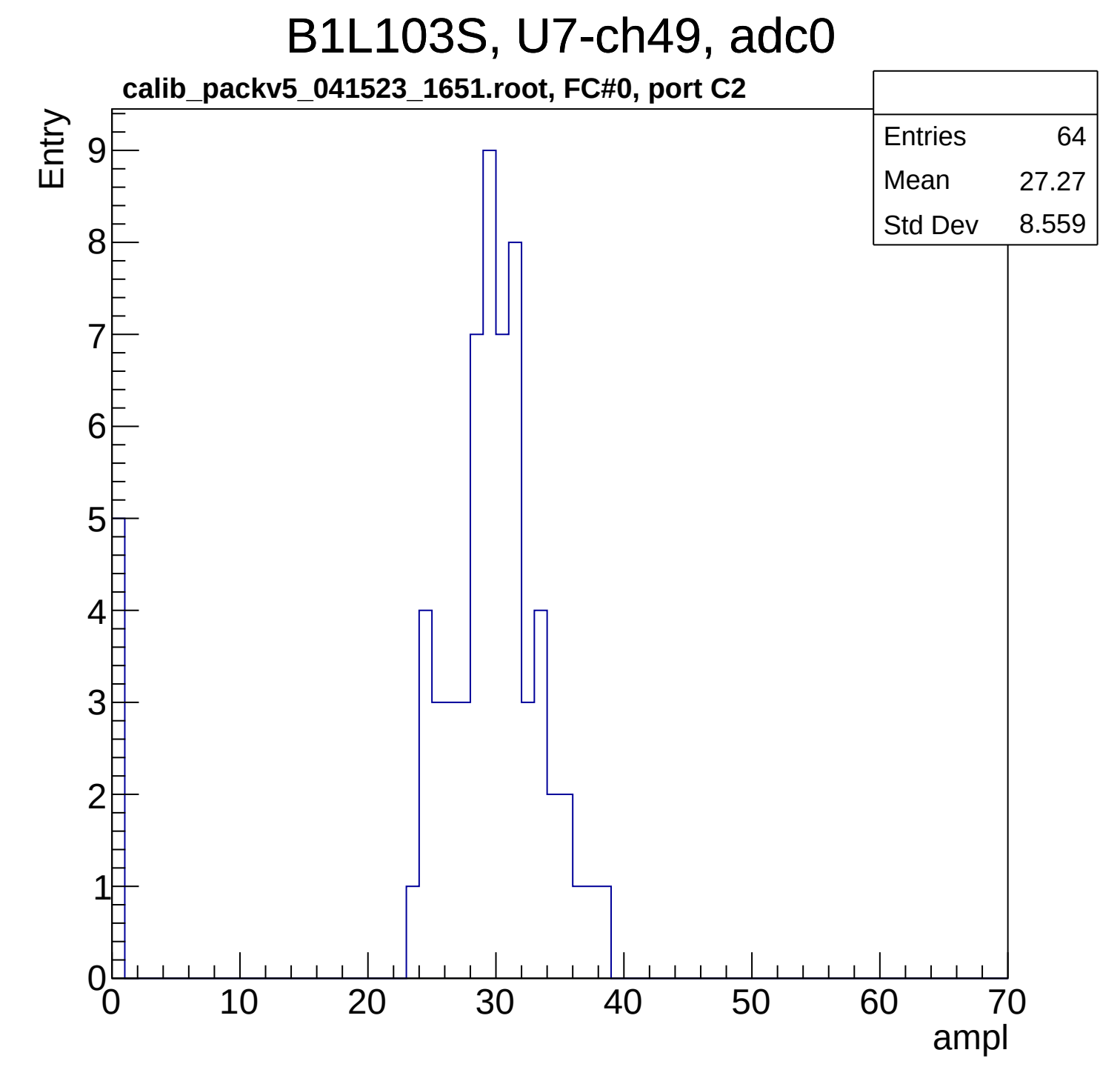

B1L103S, U7-ch48, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 44.84
Std Dev 6.798
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

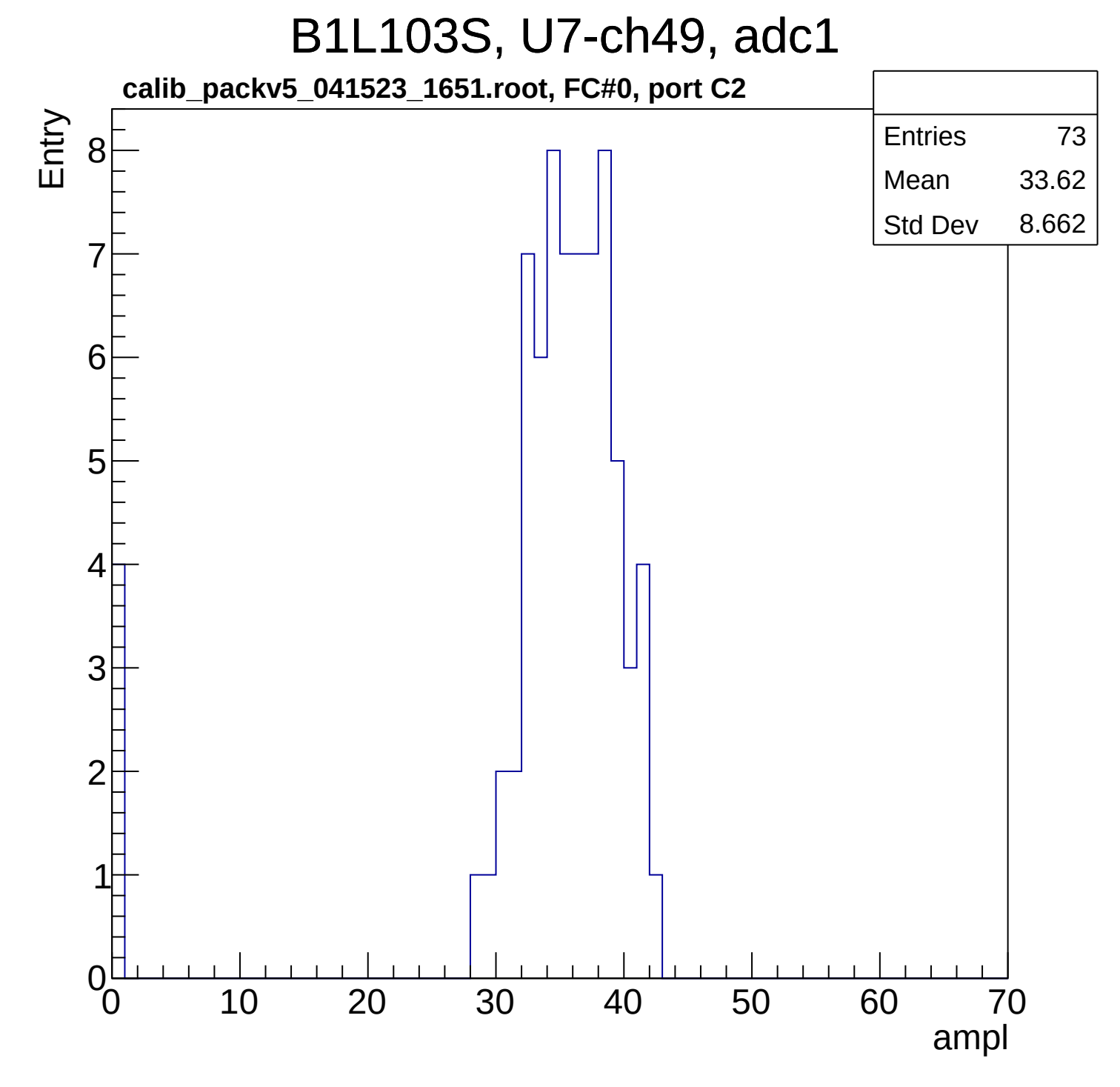

B1L103S, U7-ch48, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 52.78
Std Dev 2.774
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

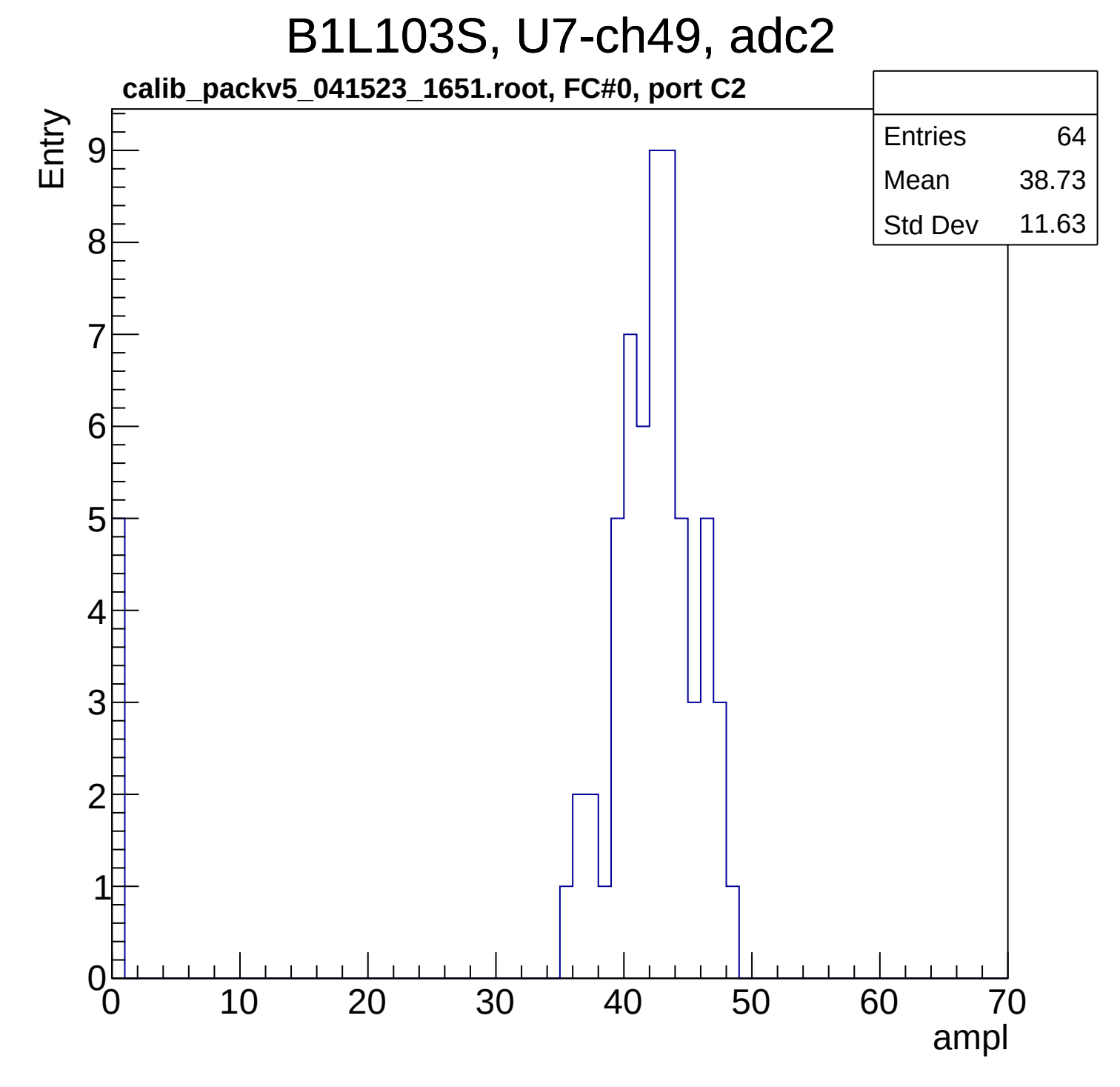

B1L103S, U7-ch48, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 56.96
Std Dev 8.229
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

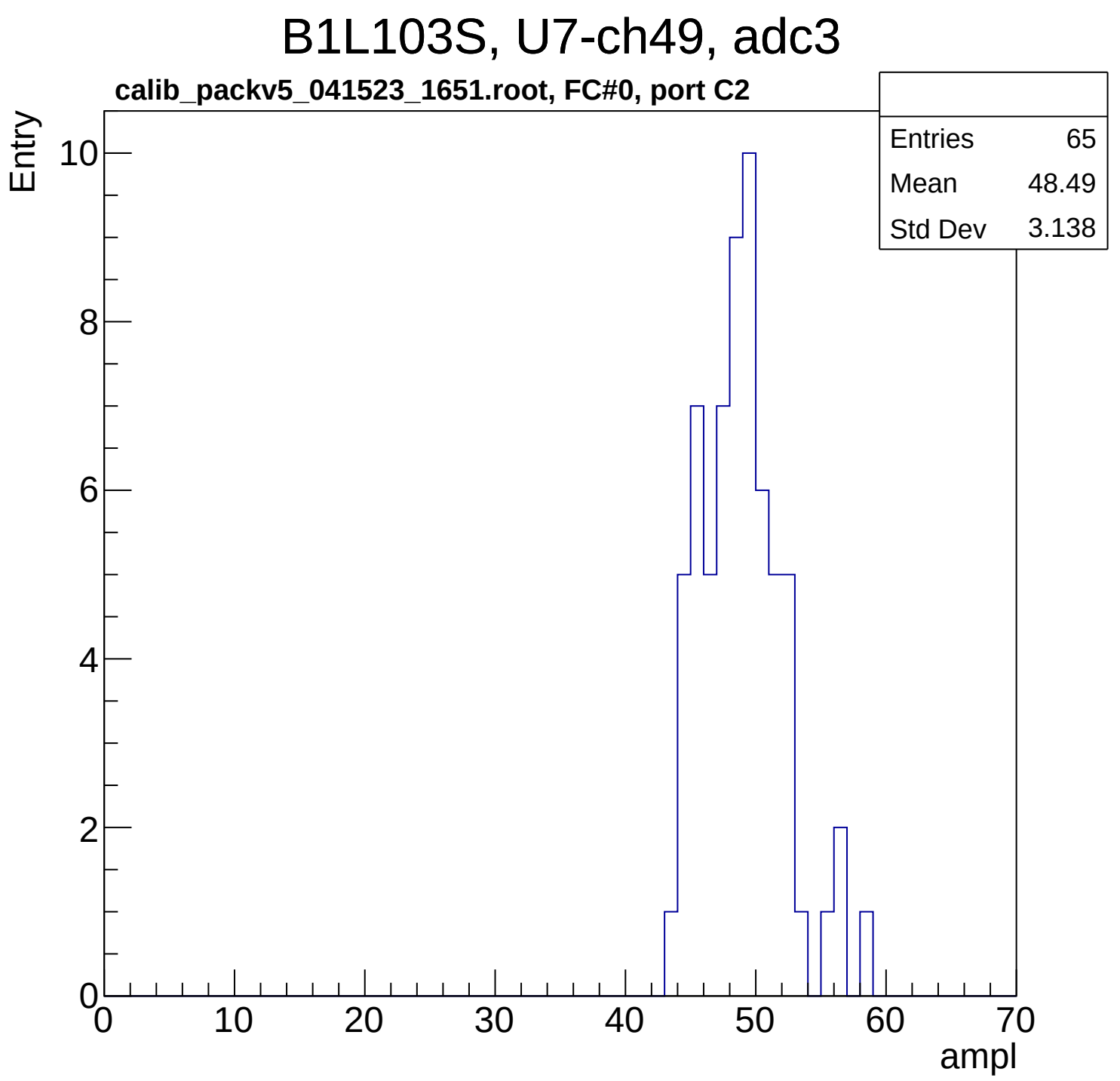

B1L103S, U7-ch48, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 61.05
Std Dev 1.704
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

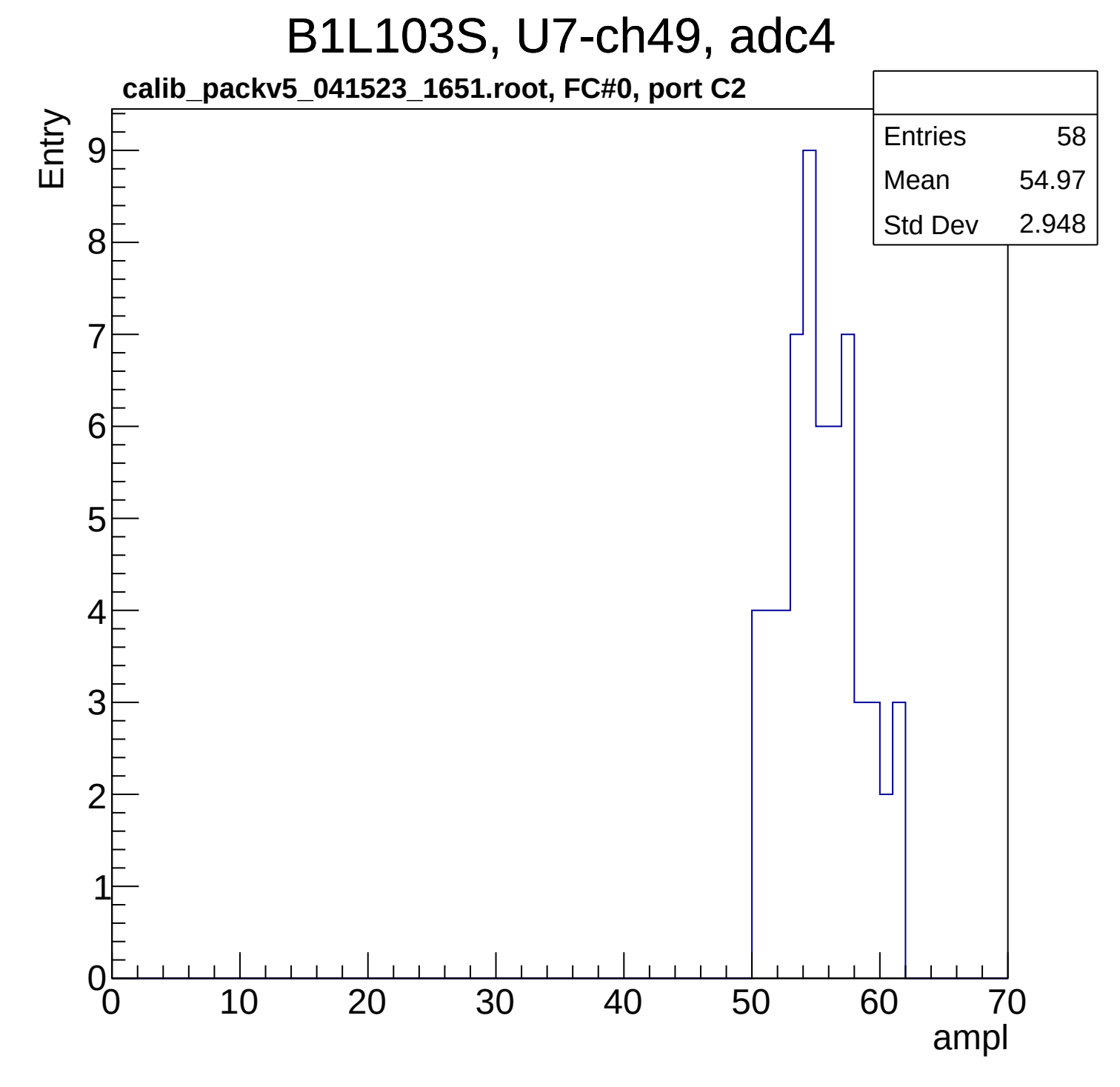

B1L103S, U7-ch48, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 9.318
Std Dev 21.49
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

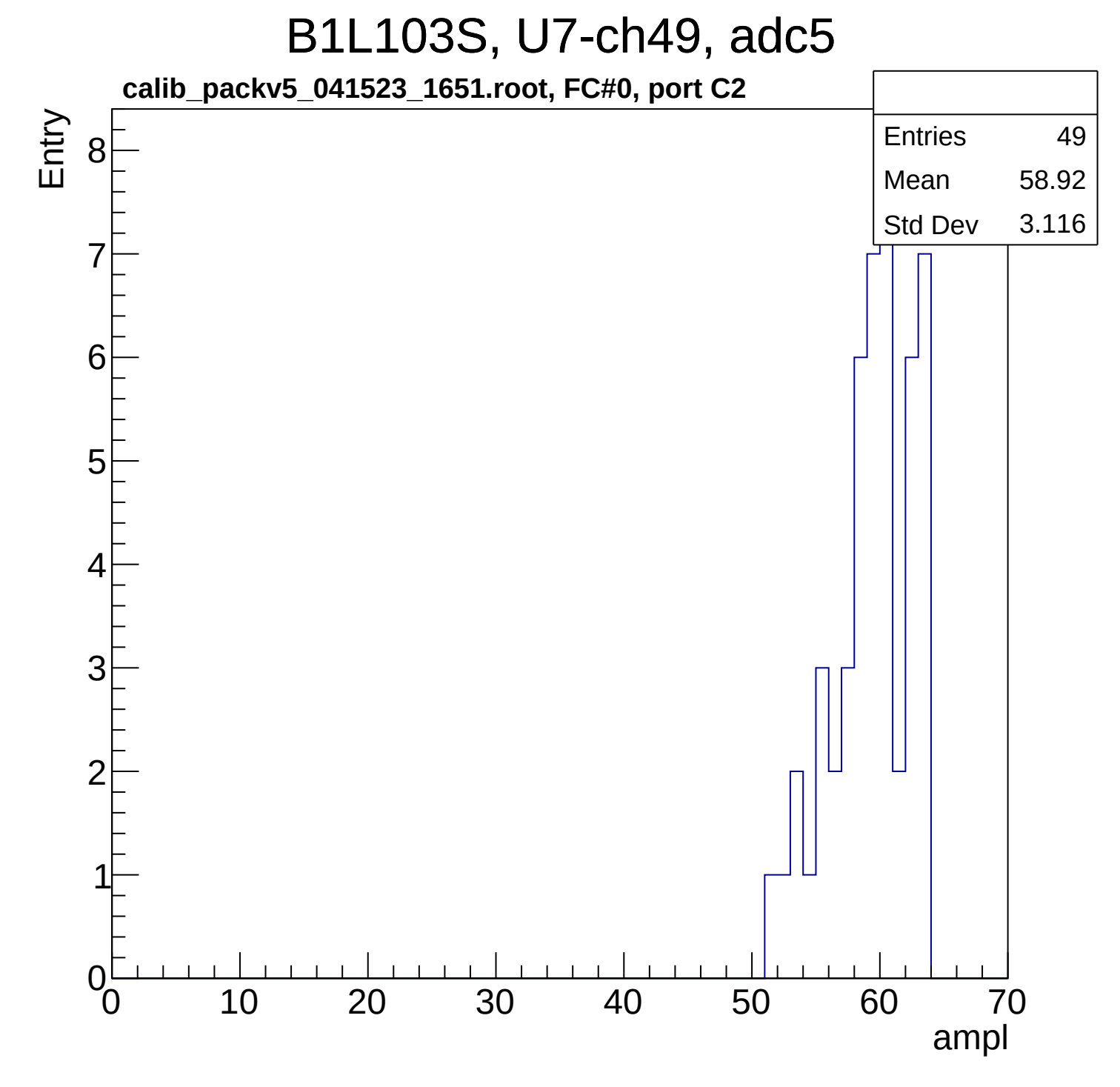

B1L103S, U7-ch49, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 27.27
Std Dev 8.559
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

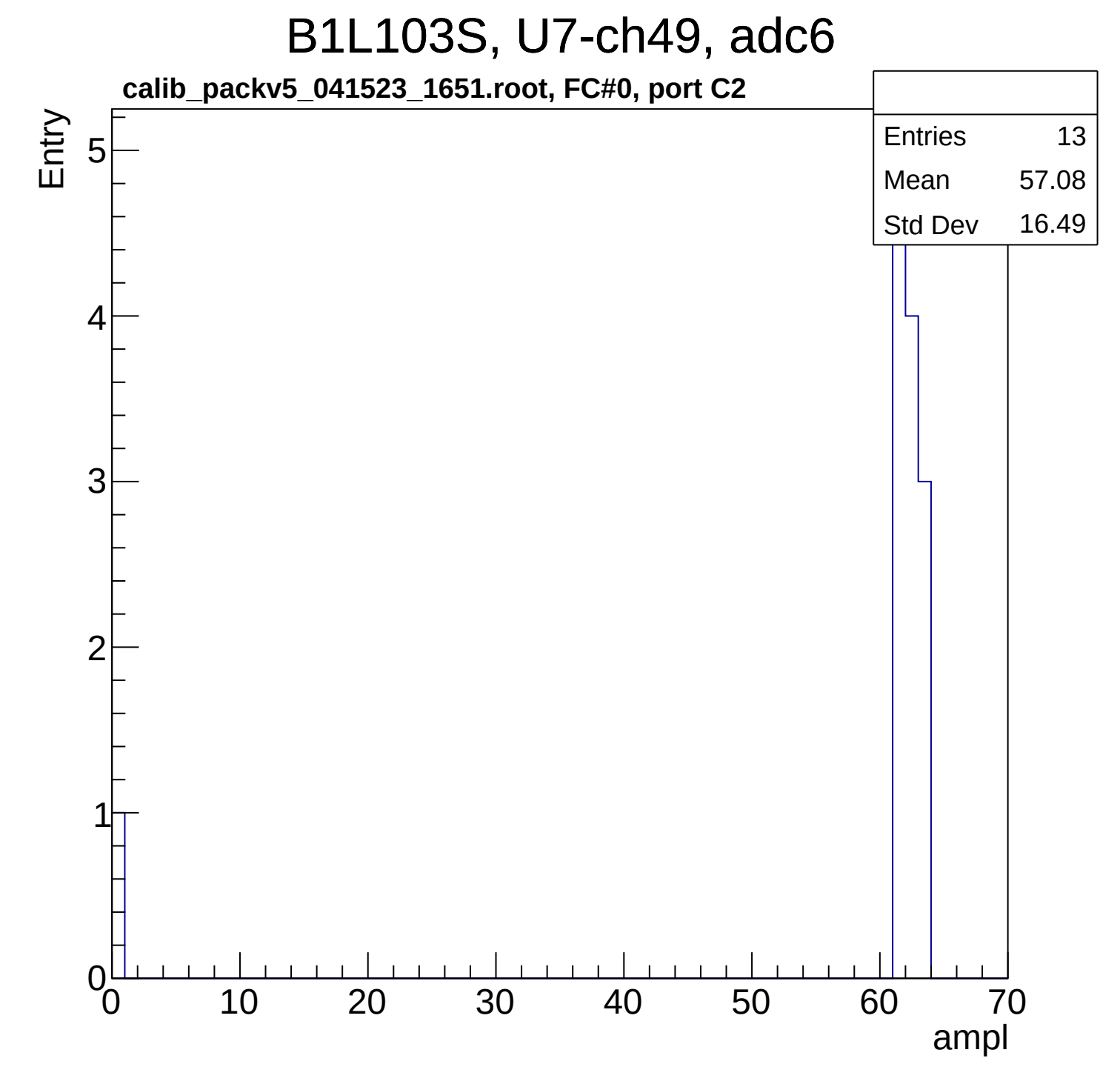

B1L103S, U7-ch49, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 33.62
Std Dev 8.662
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

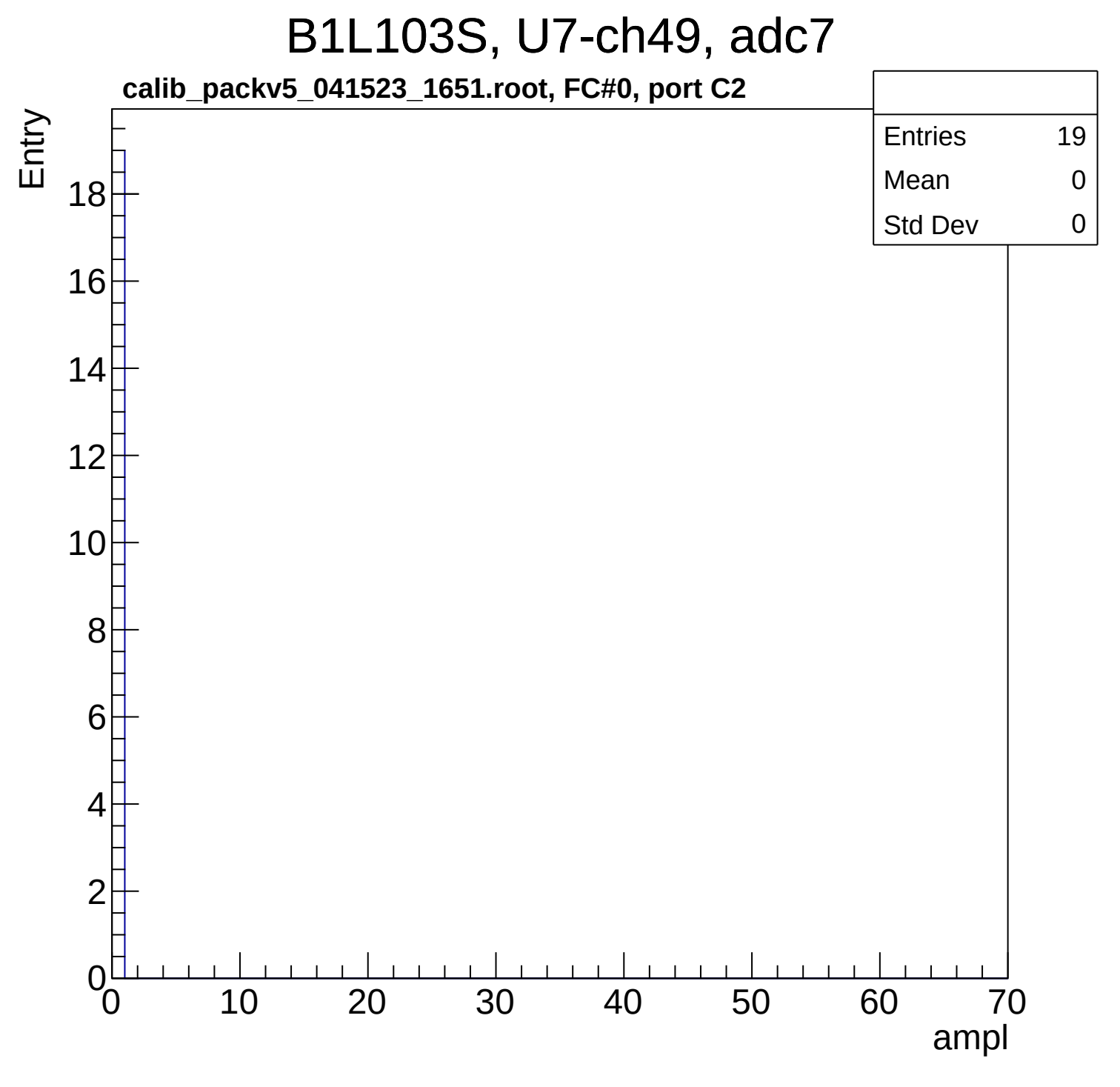

B1L103S, U7-ch49, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 38.73
Std Dev 11.63
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

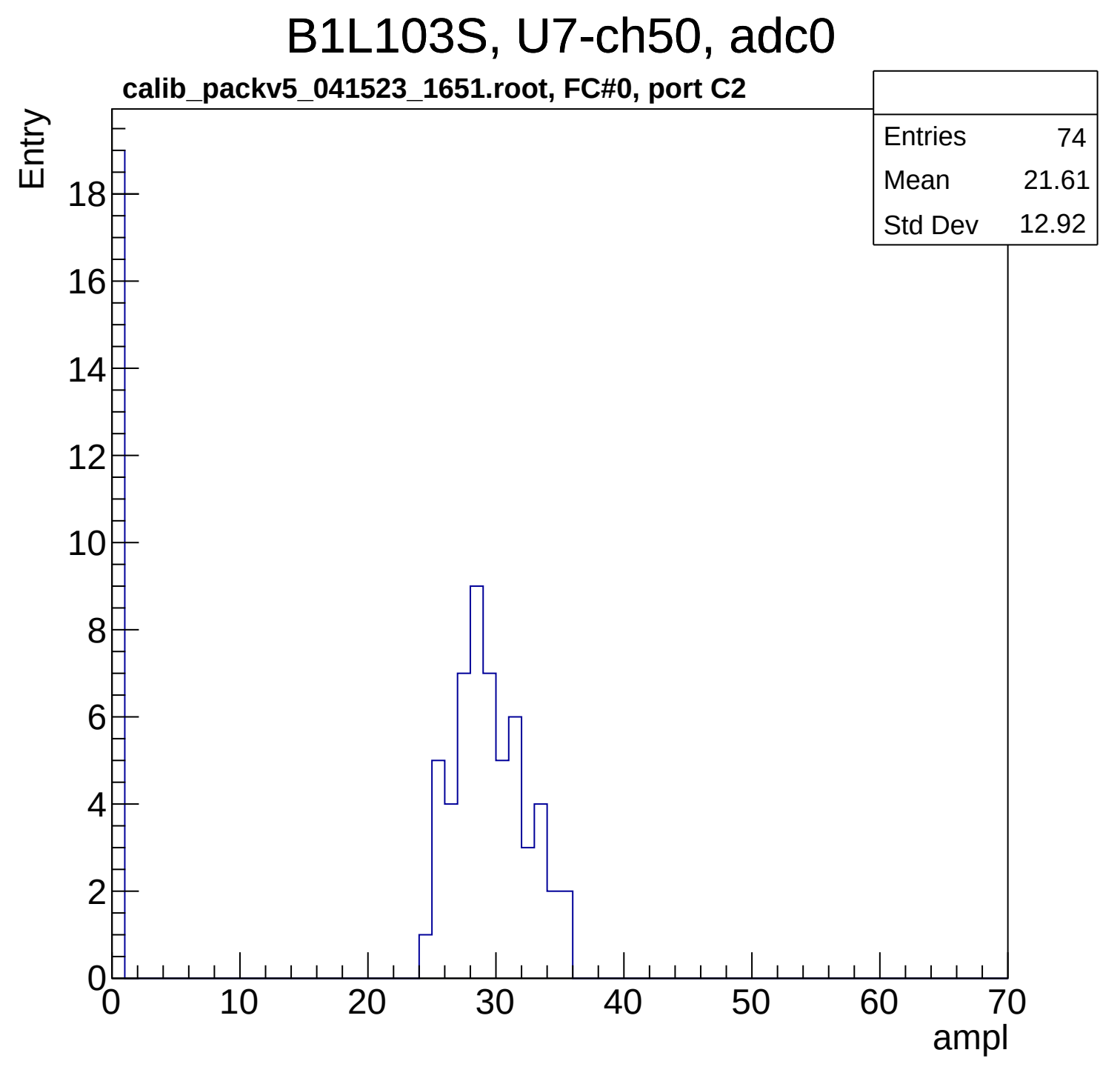

B1L103S, U7-ch49, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 48.49
Std Dev 3.138
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

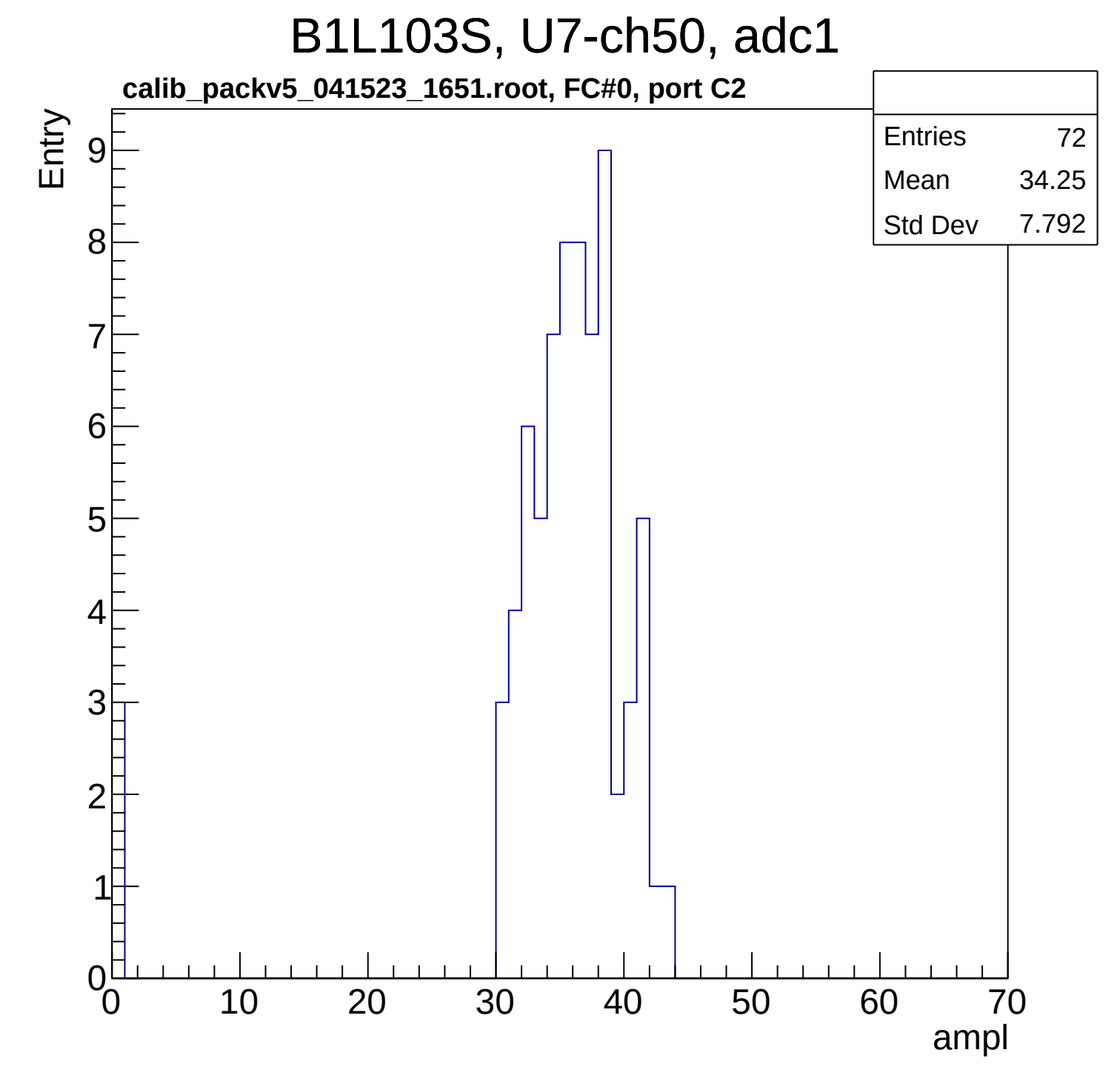

B1L103S, U7-ch49, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 54.97
Std Dev 2.948
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

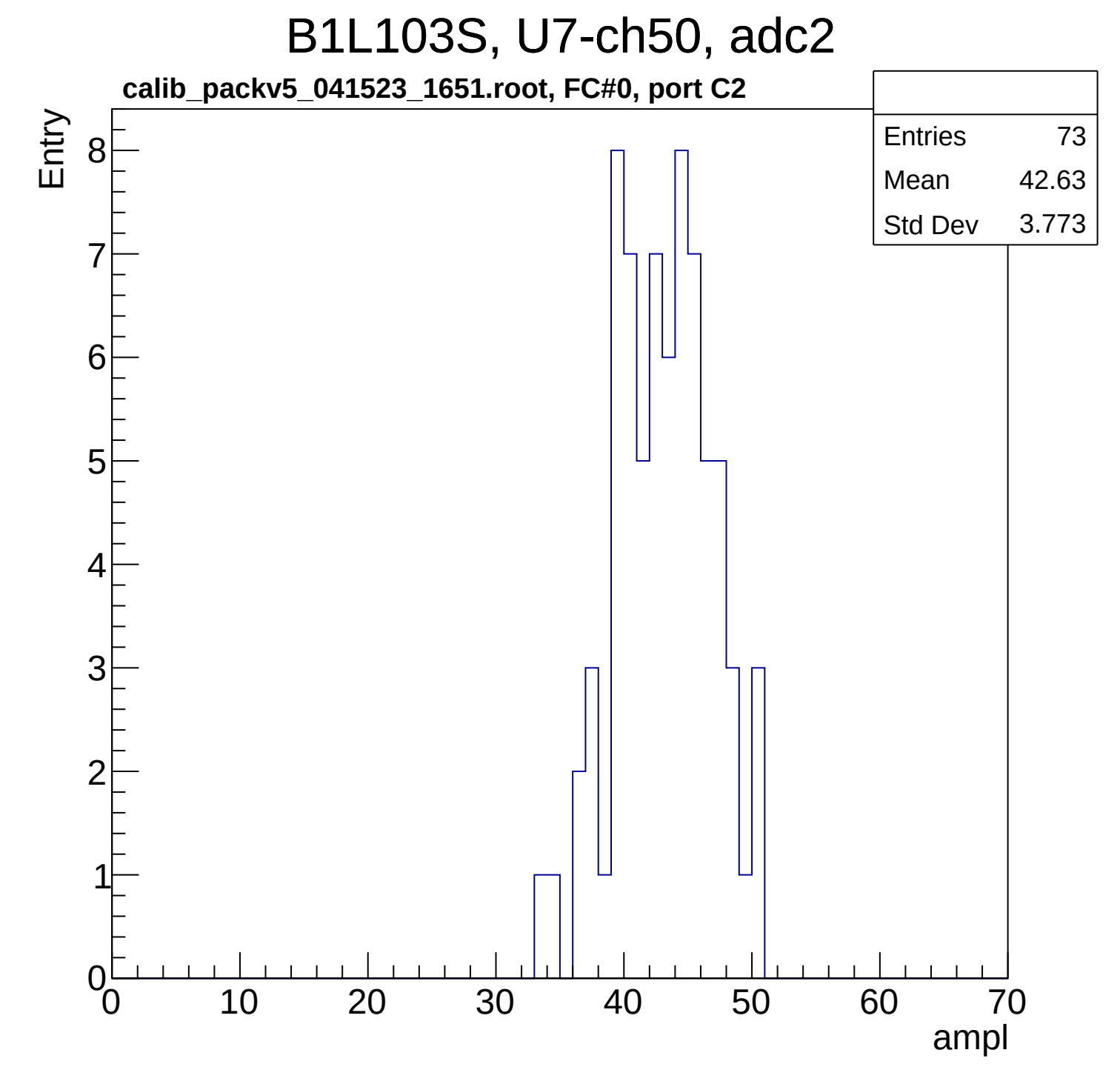

B1L103S, U7-ch49, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 58.92
Std Dev 3.116
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch49, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 13
Mean 57.08
Std Dev 16.49
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U7-ch49, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch50, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 21.61
Std Dev 12.92
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch50, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 34.25
Std Dev 7.792
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U7-ch50, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 42.63
Std Dev 3.773
Entry
ampl
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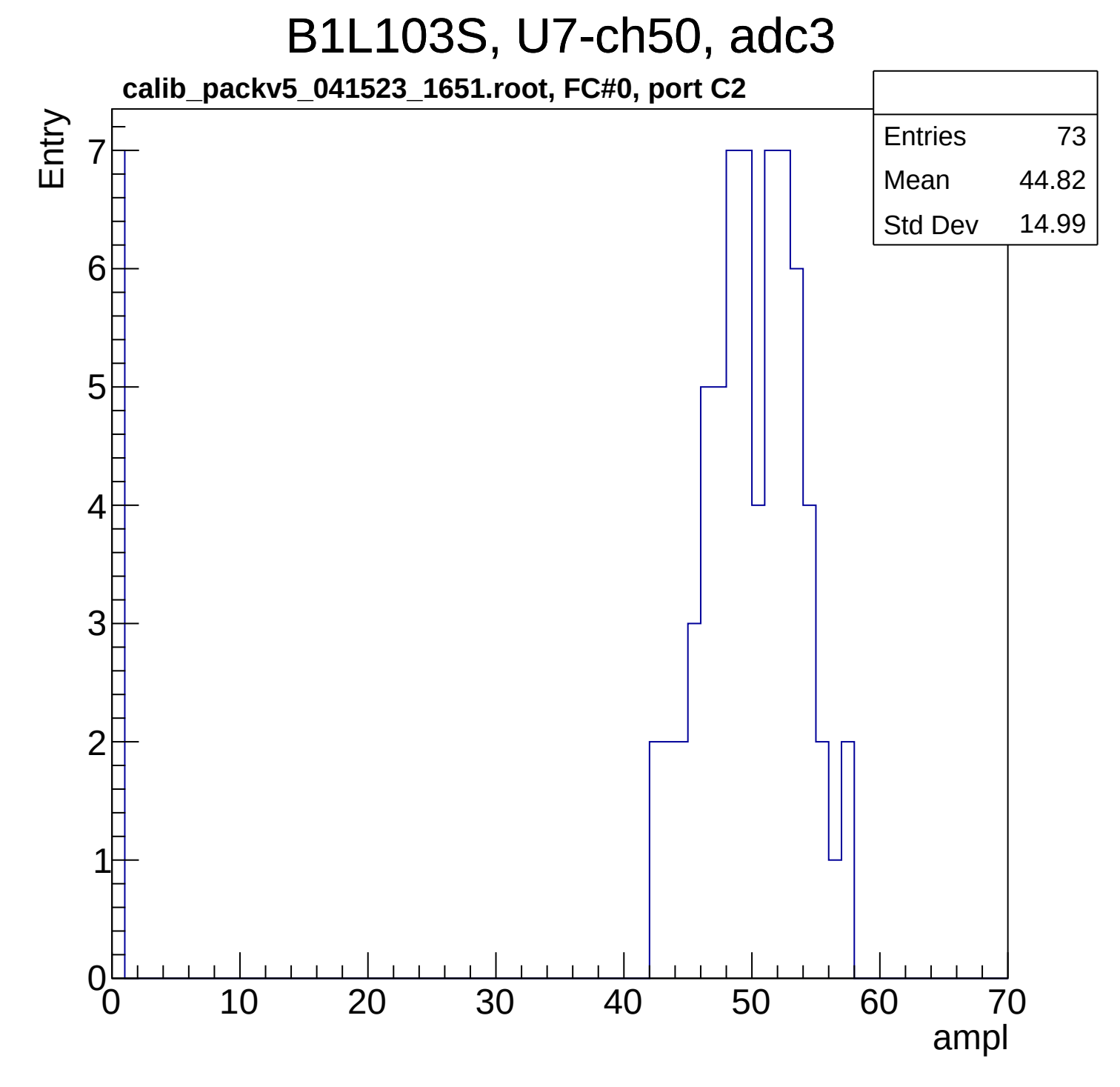
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch50, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 44.82
Std Dev 14.99
Entry
ampl
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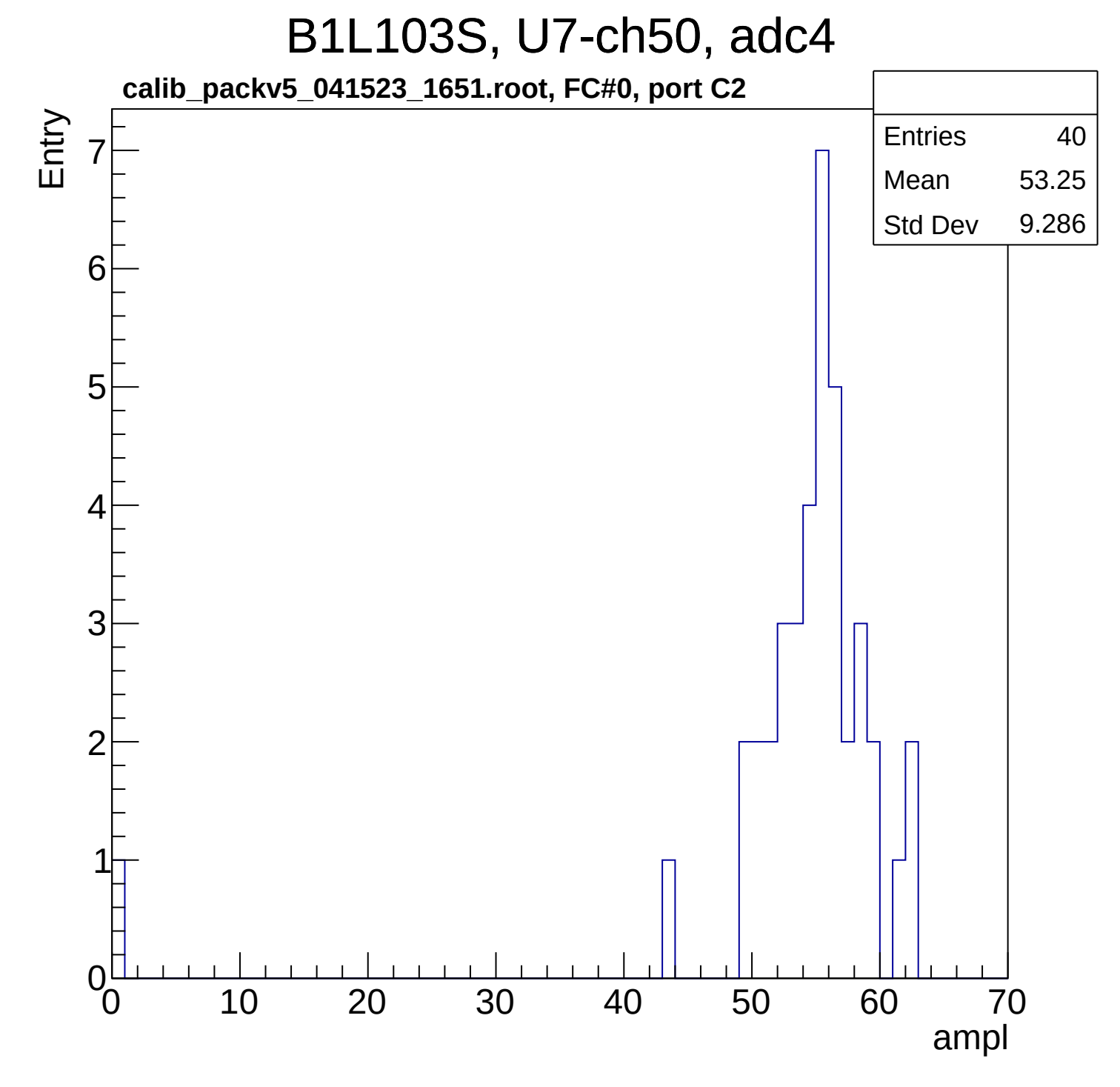
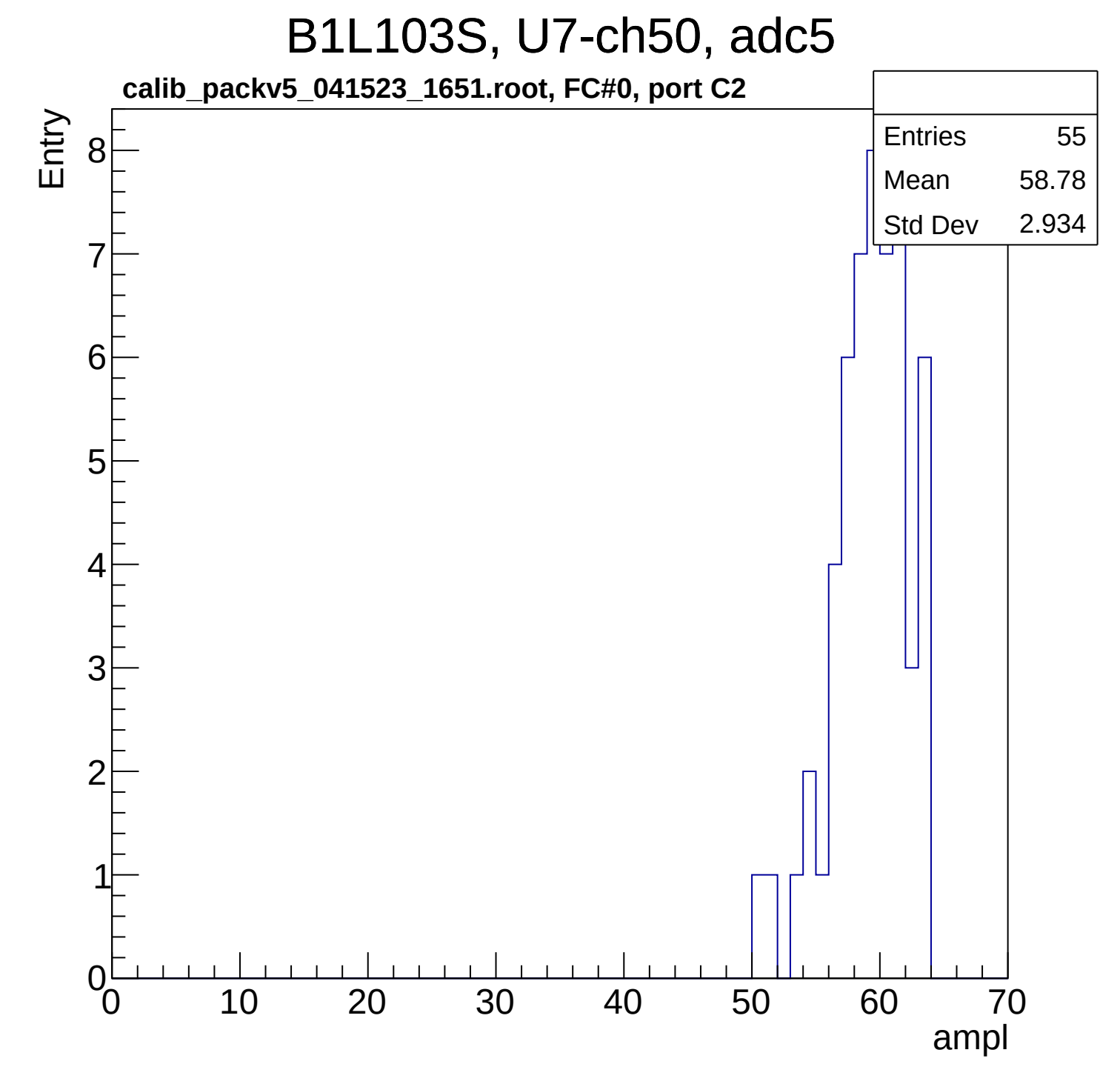
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U7-ch50, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 40
Mean 53.25
Std Dev 9.286
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U7-ch50, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 58.78
Std Dev 2.934
Entry
ampl
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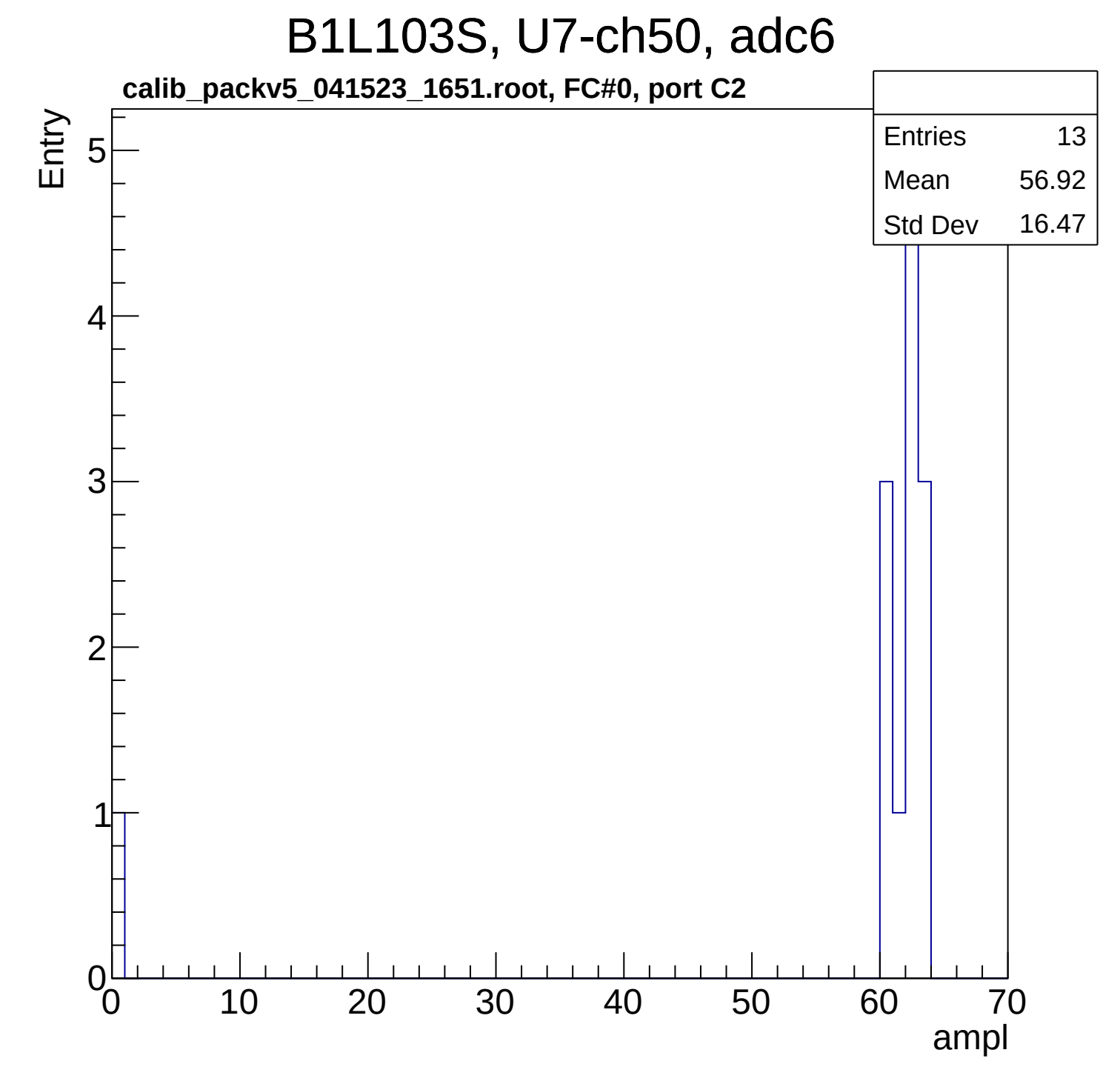
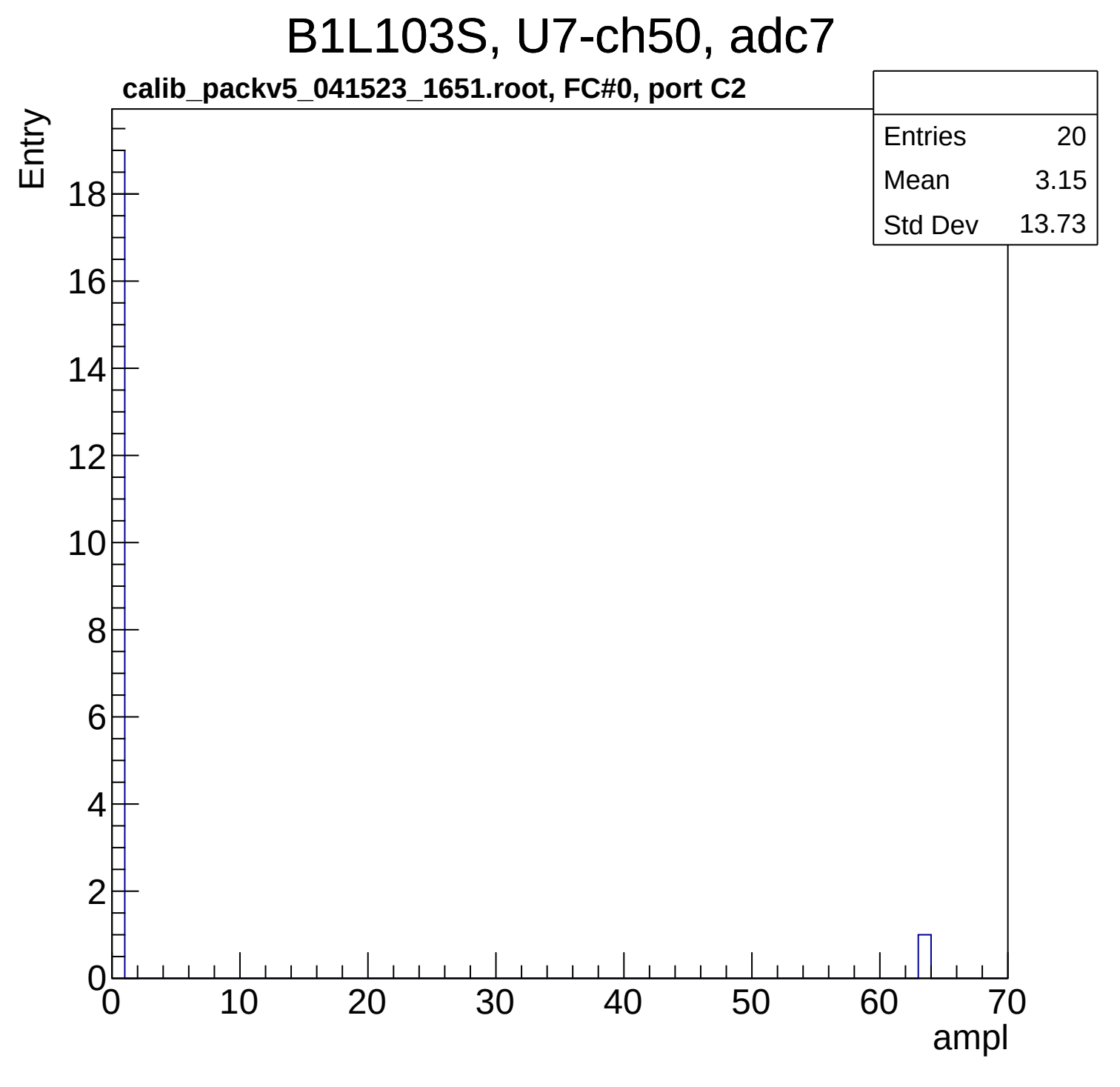
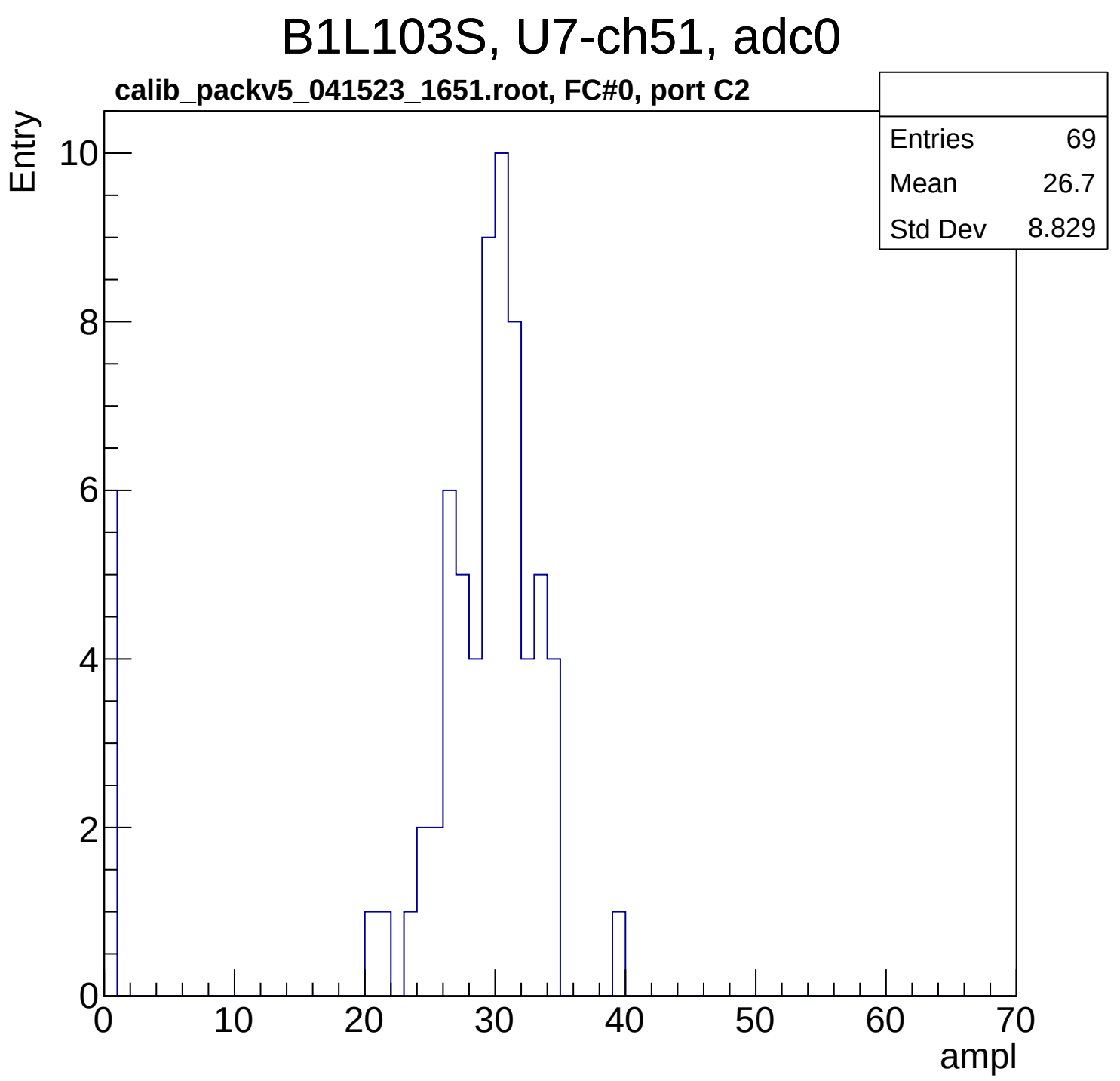
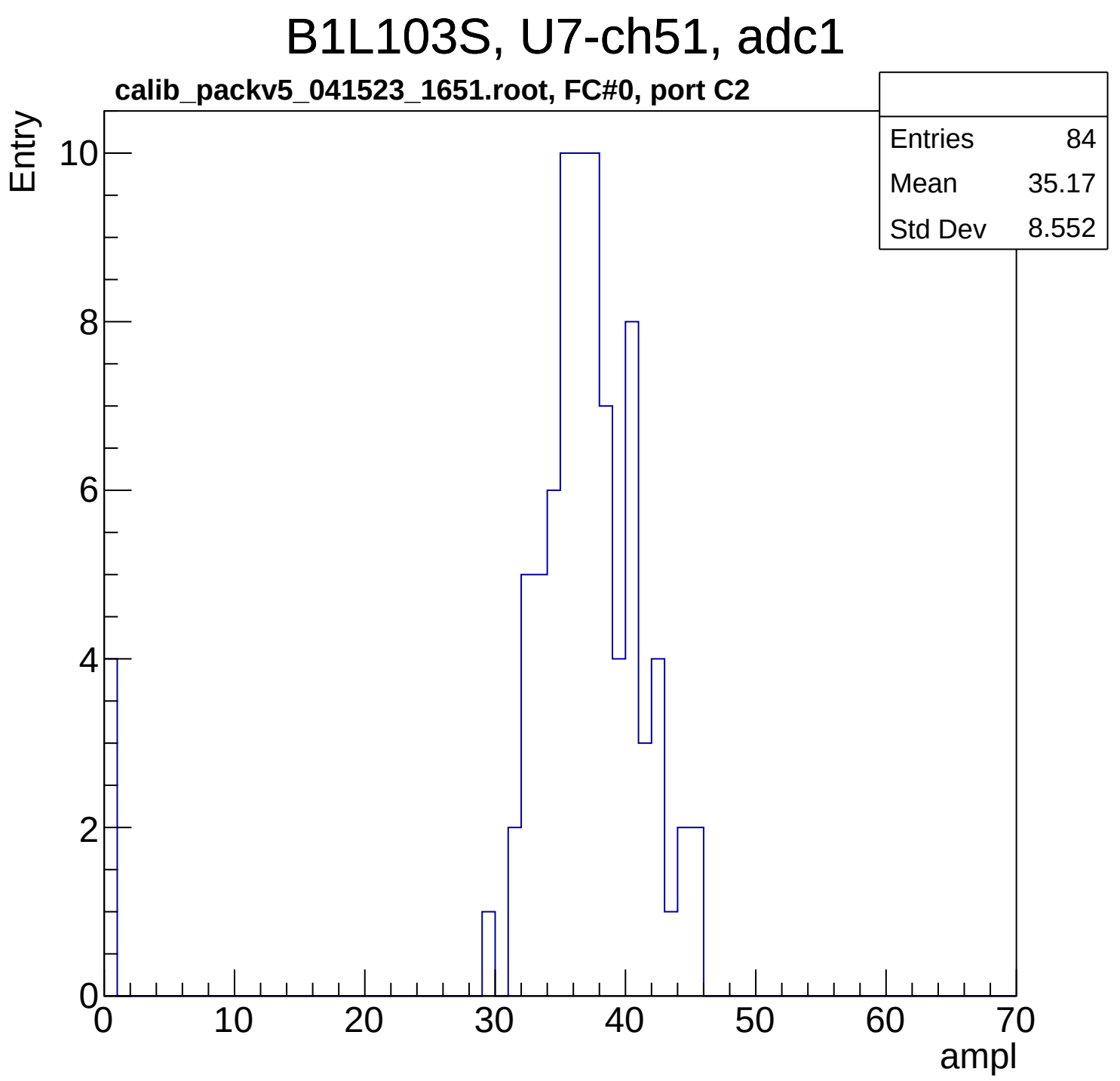
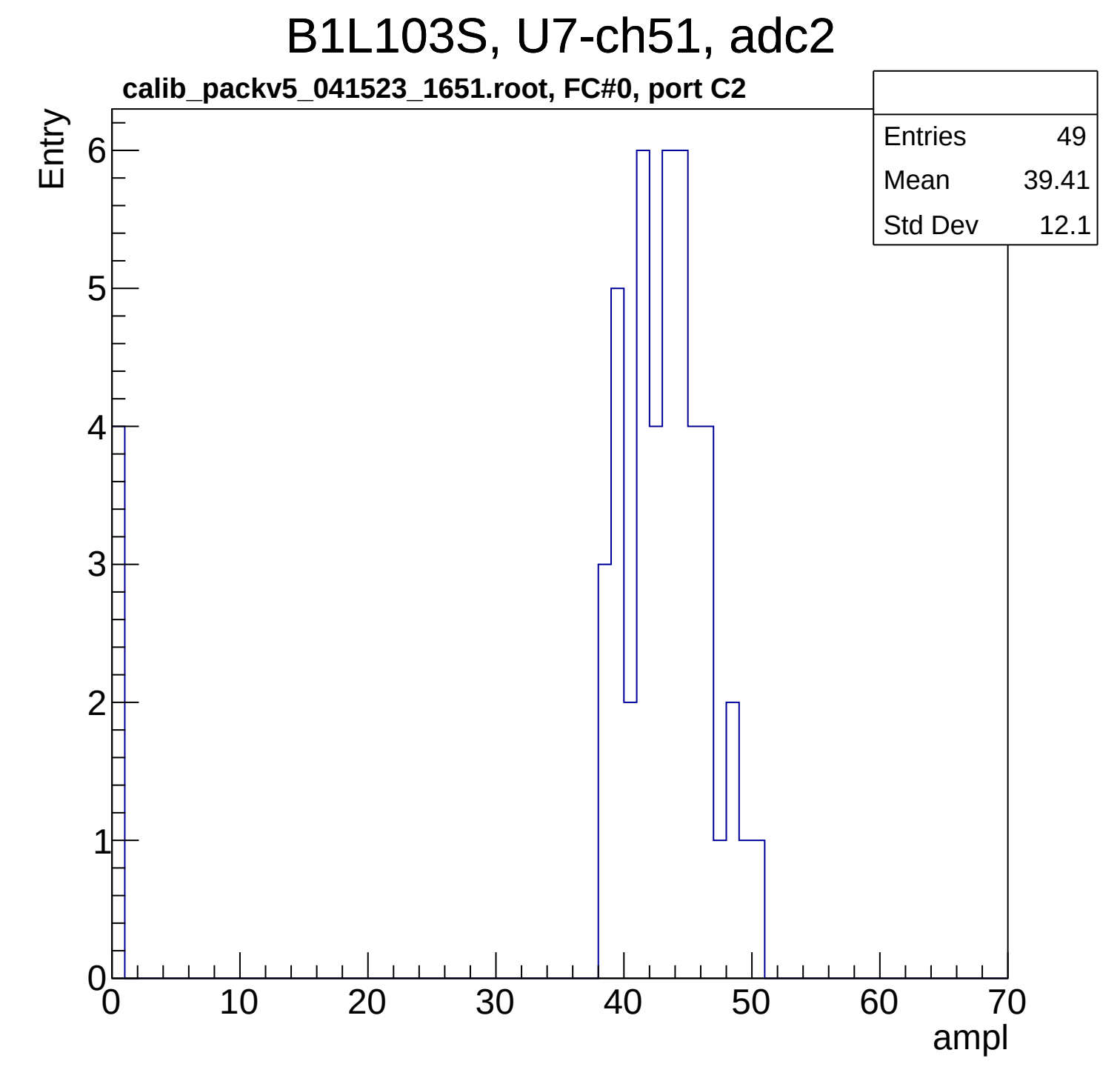
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

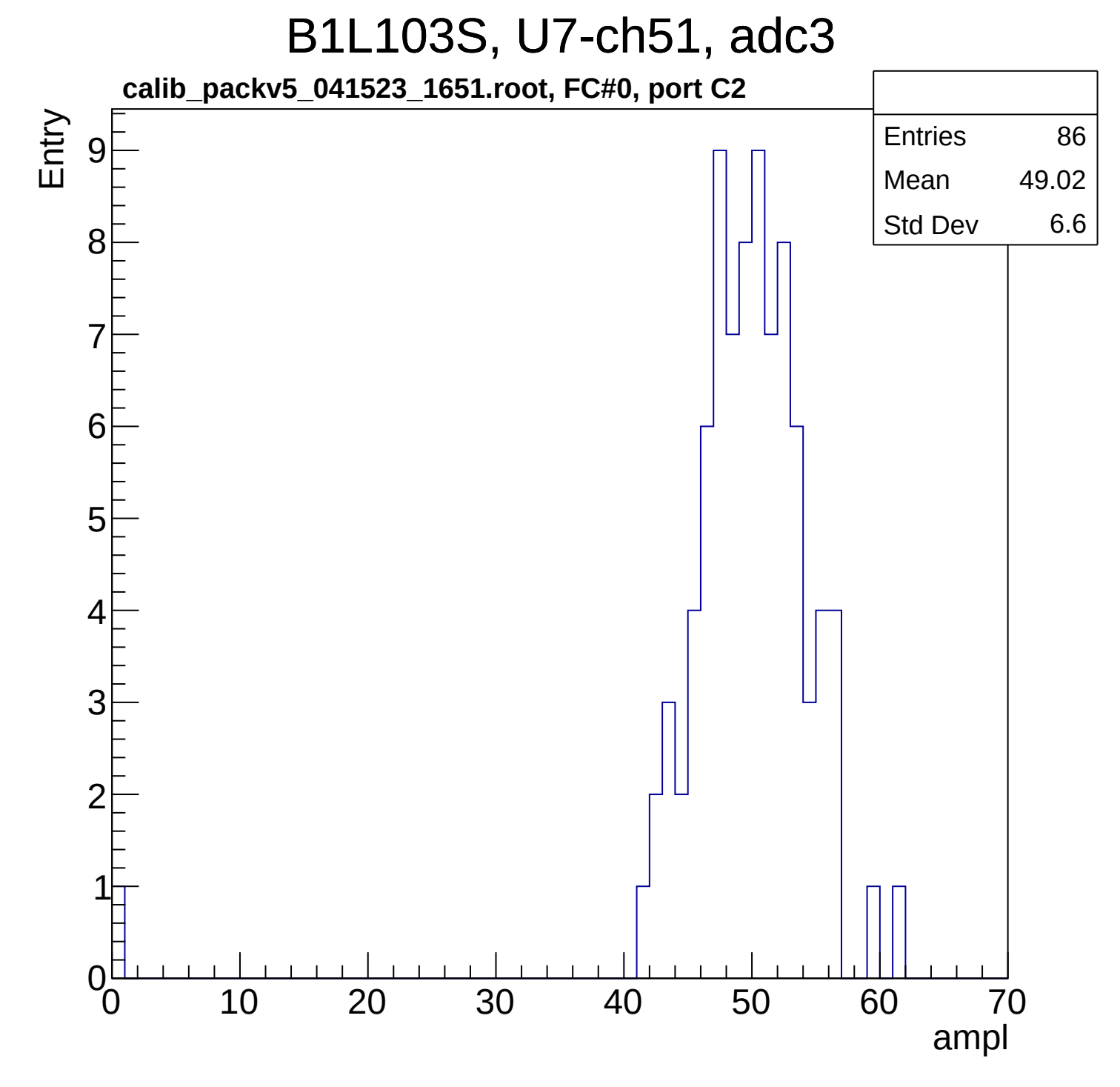

B1L103S, U7-ch50, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 13
Mean 56.92
Std Dev 16.47
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U7-ch50, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch51, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 26.7
Std Dev 8.829
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U7-ch51, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 35.17
Std Dev 8.552
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U7-ch51, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 39.41
Std Dev 12.1
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch51, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 49.02
Std Dev 6.6
Entry
ampl
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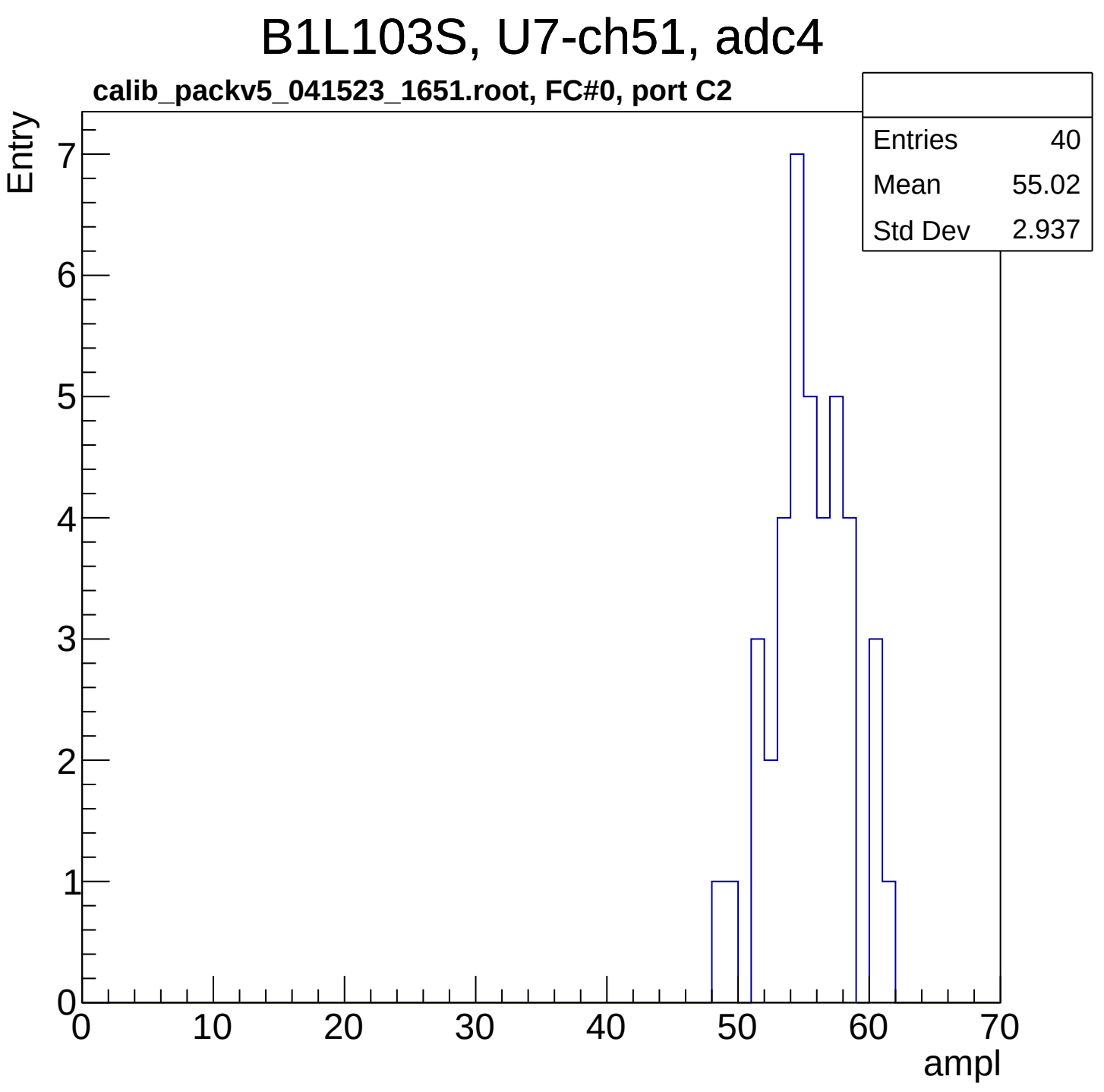
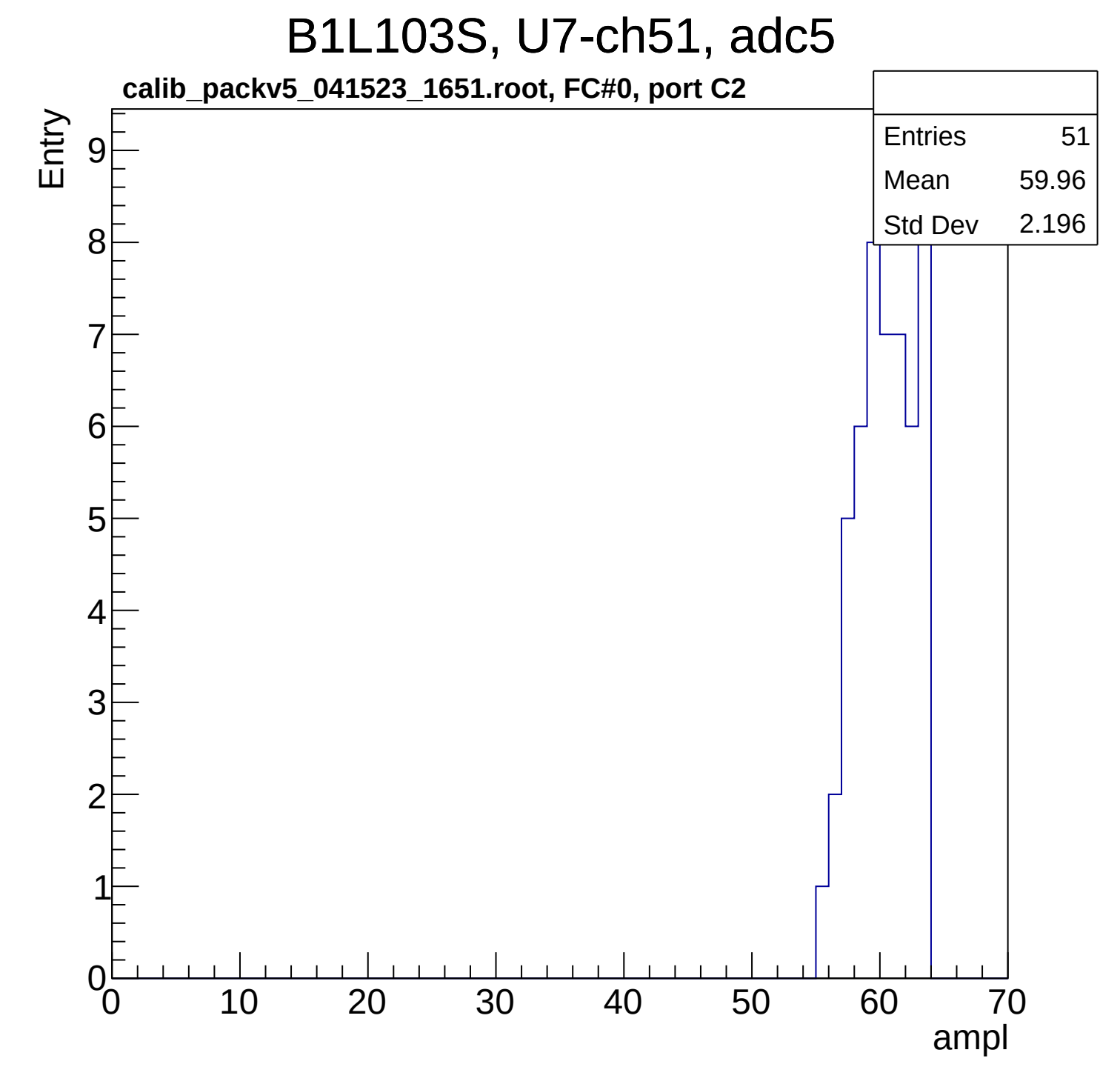
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U7-ch51, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 40
Mean 55.02
Std Dev 2.937
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U7-ch51, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 59.96
Std Dev 2.196
Entry
ampl
0
1
2
3
4
5
6
7
8
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0
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60
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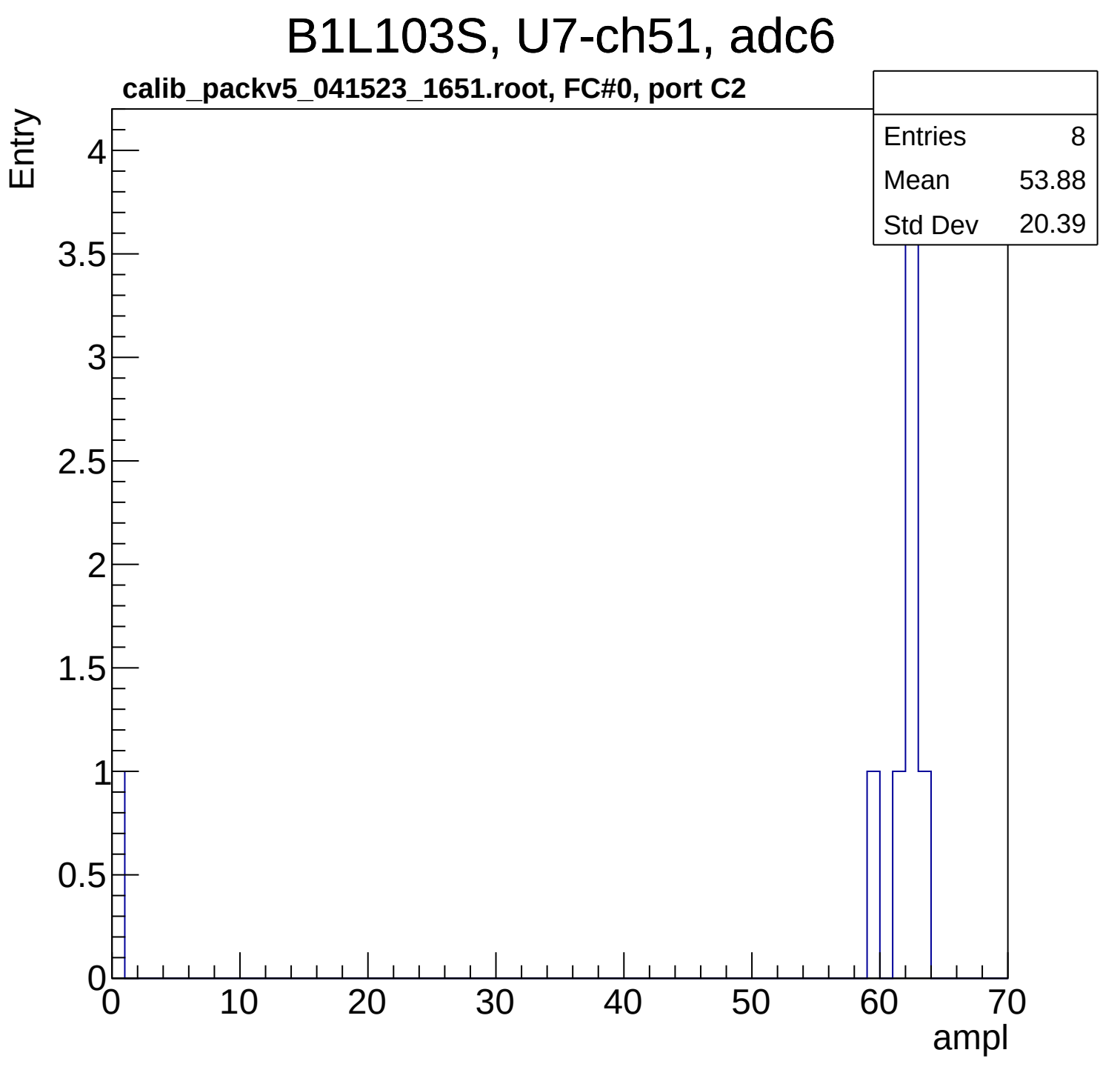
B1L103S, U7-ch51, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 53.88
Std Dev 20.39
Entry
ampl
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0.5
1
1.5
2
2.5
3
3.5
4
0
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20
30
40
50
60
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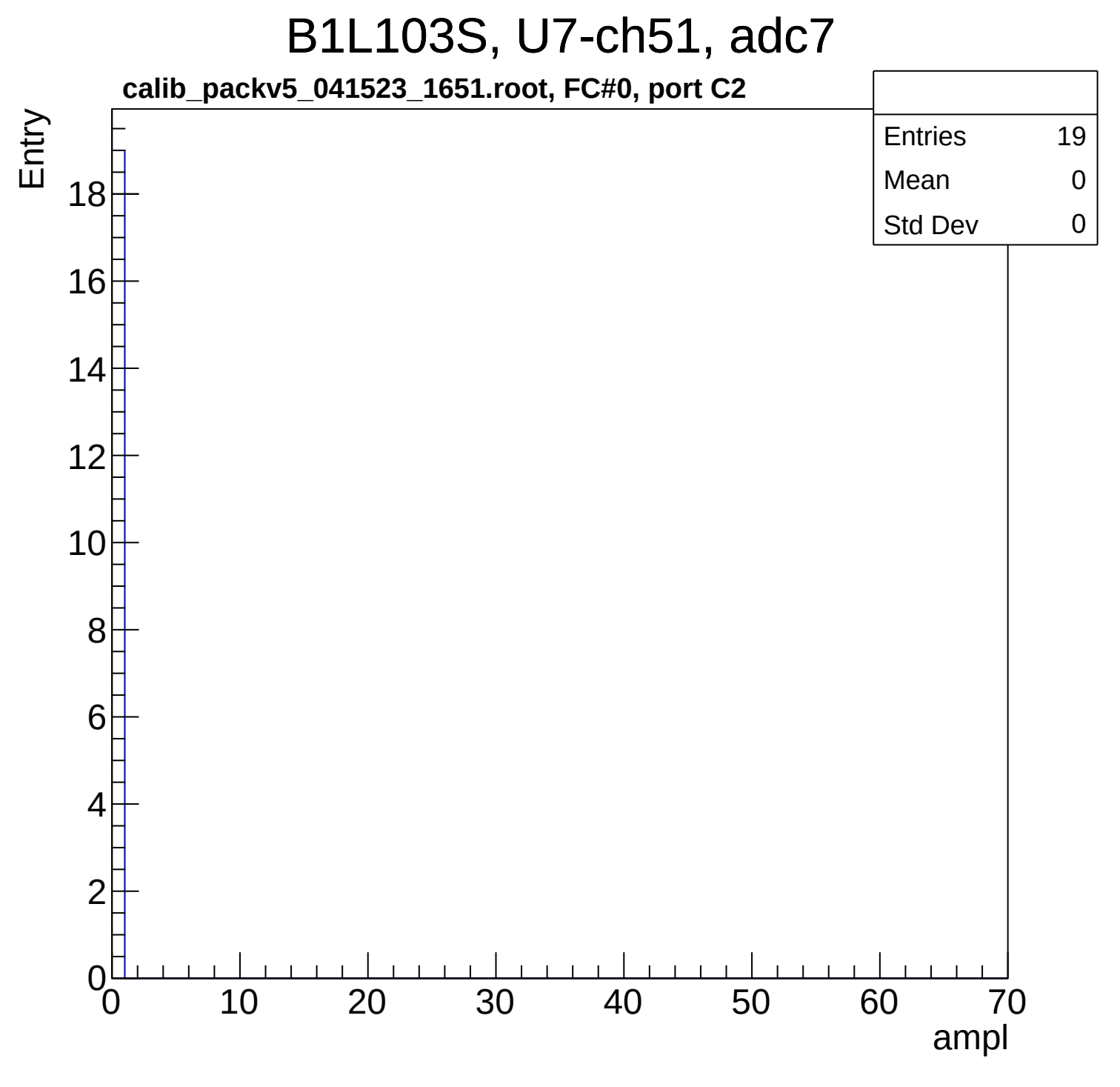
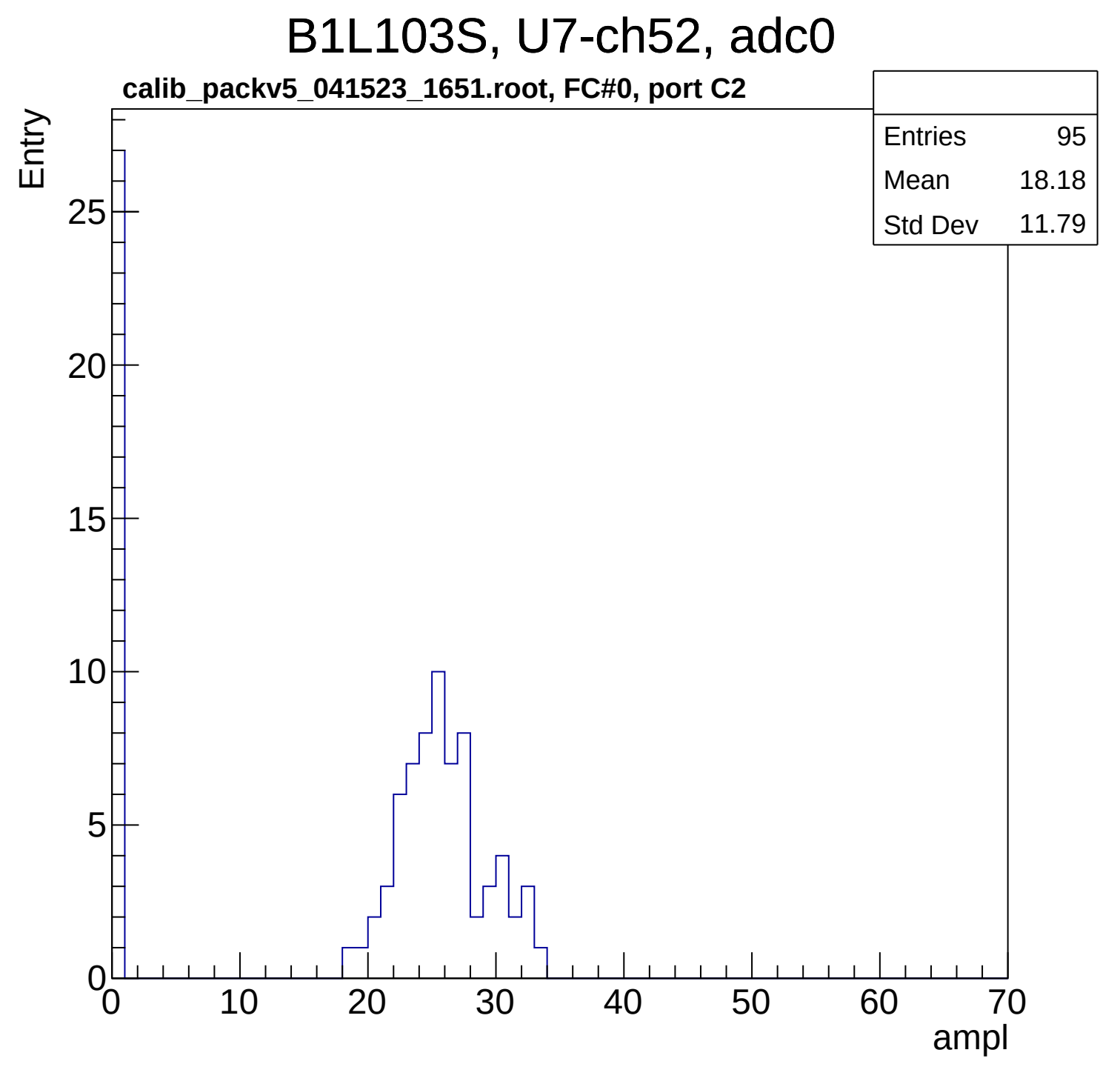
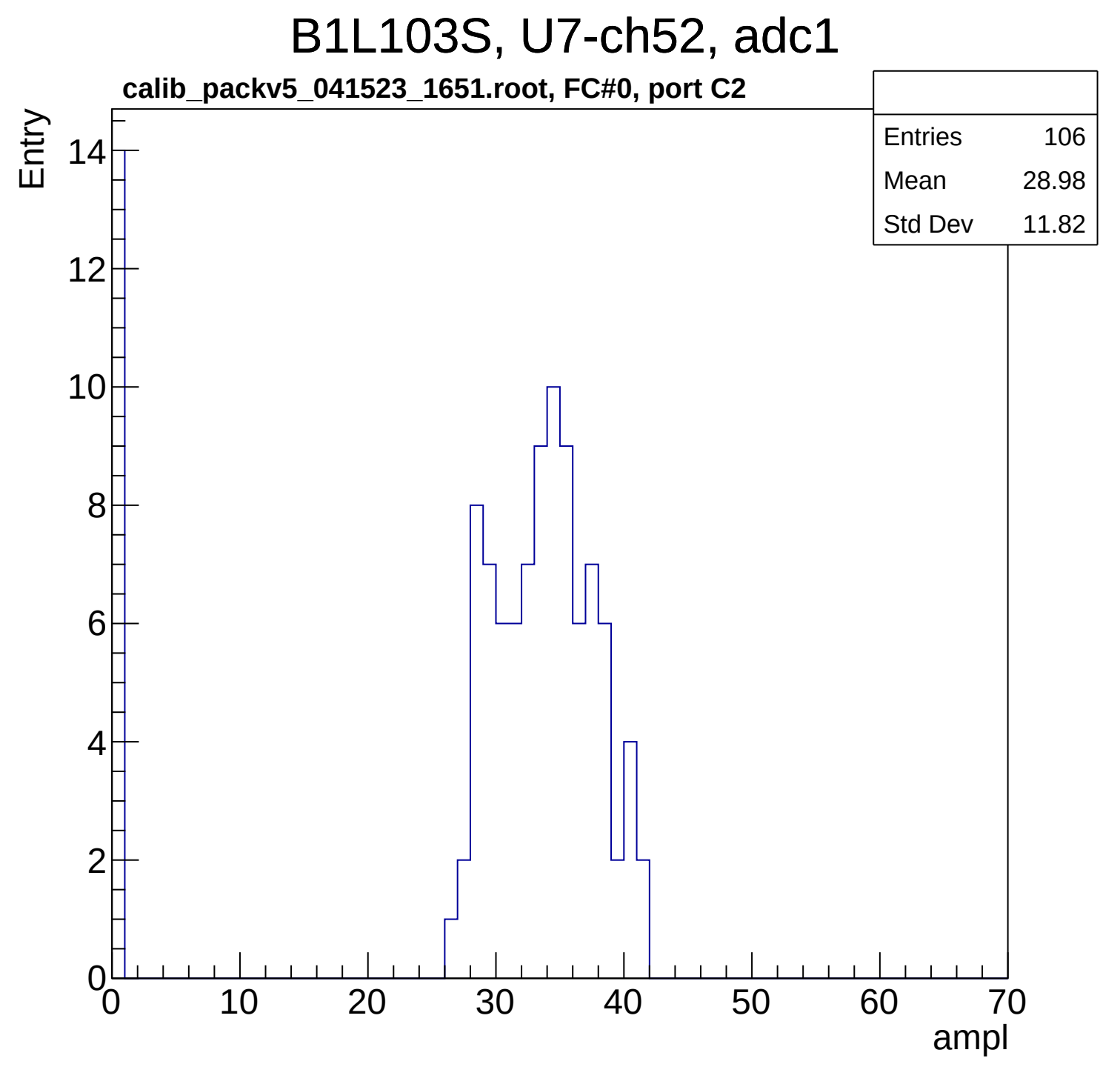

B1L103S, U7-ch51, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch52, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 95
Mean 18.18
Std Dev 11.79
Entry
0
5
10
15
20
25
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch52, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 106
Mean 28.98
Std Dev 11.82
Entry
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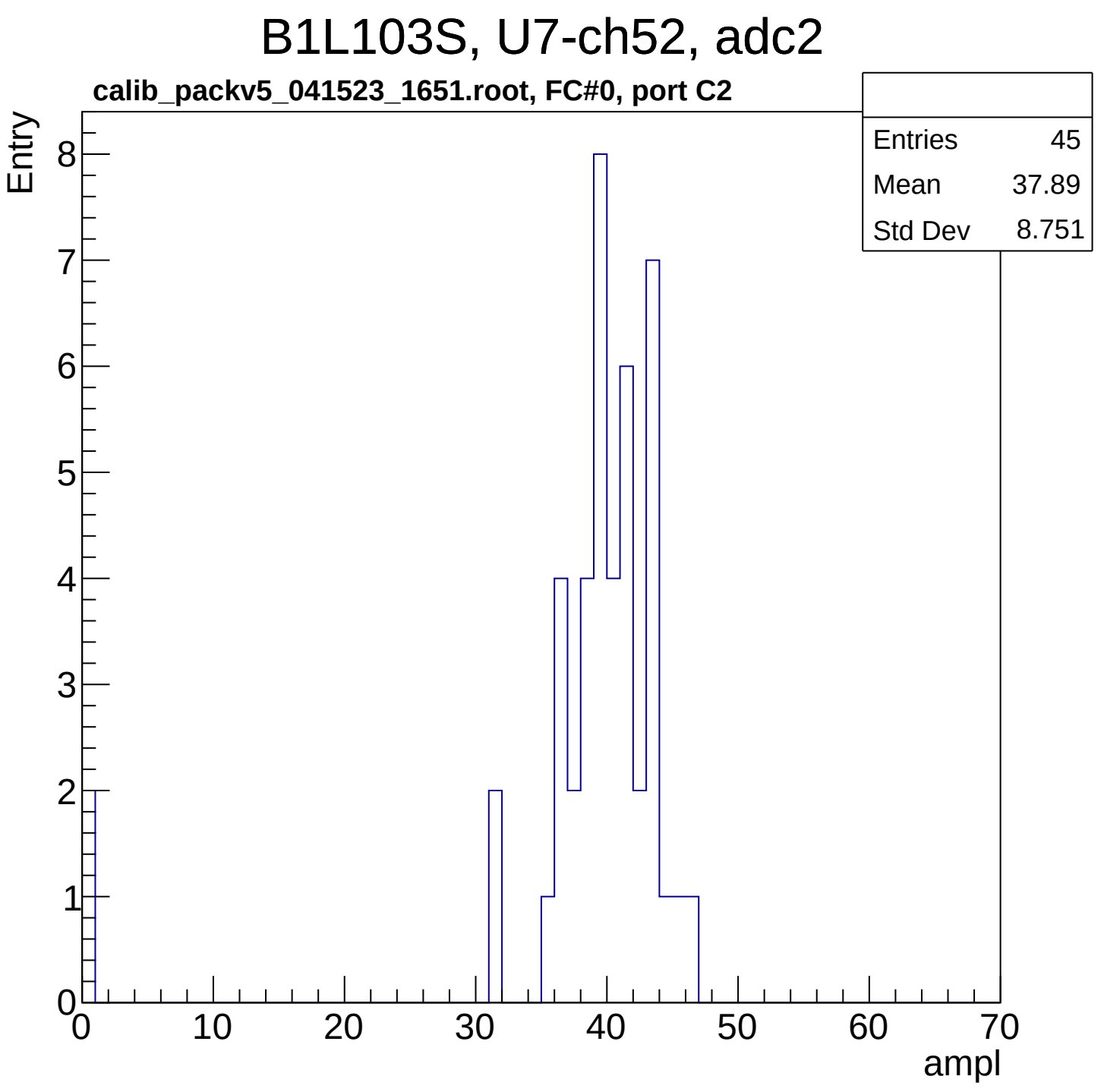
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch52, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 37.89
Std Dev 8.751
Entry
ampl
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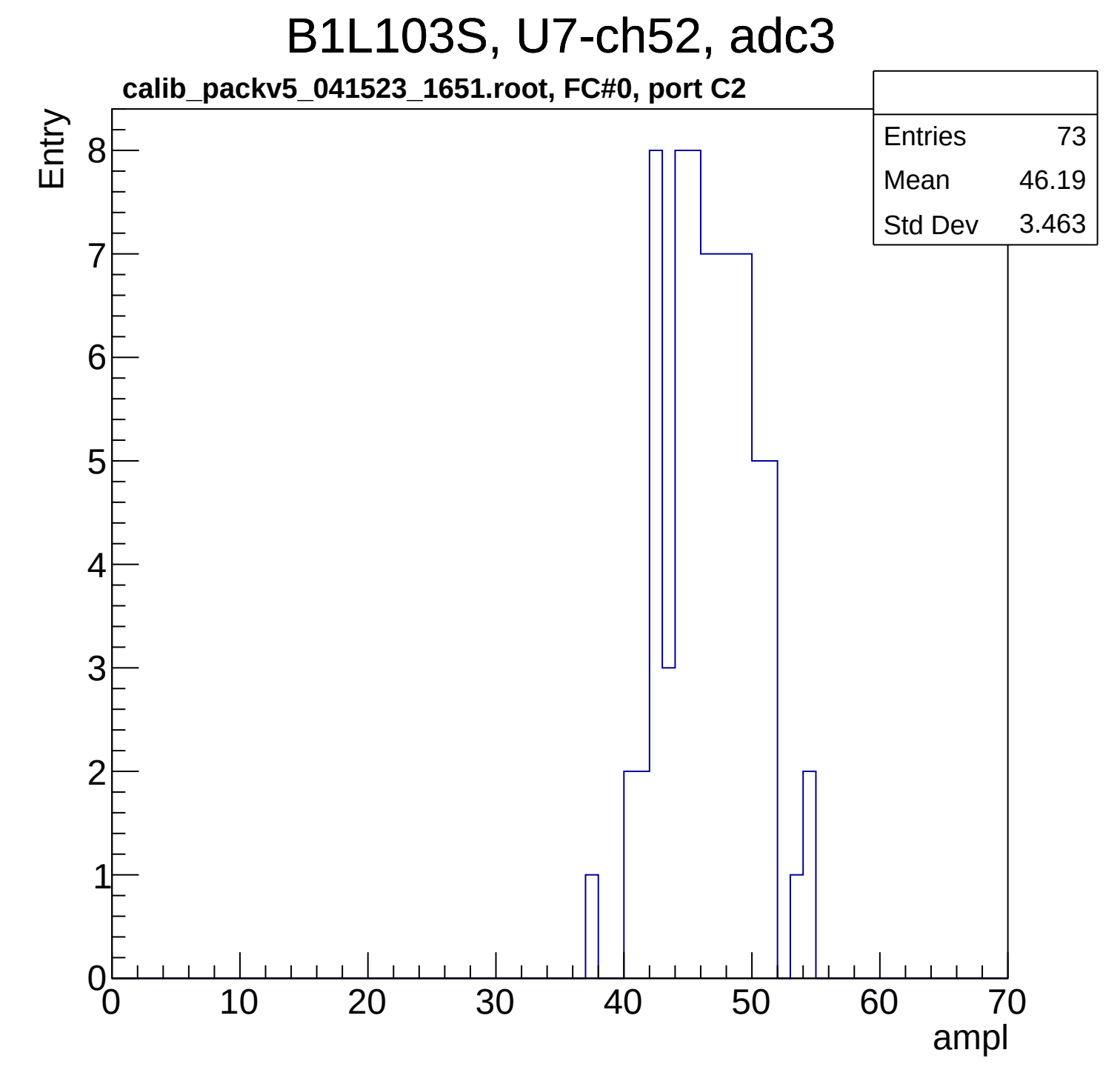
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch52, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 46.19
Std Dev 3.463
Entry
ampl
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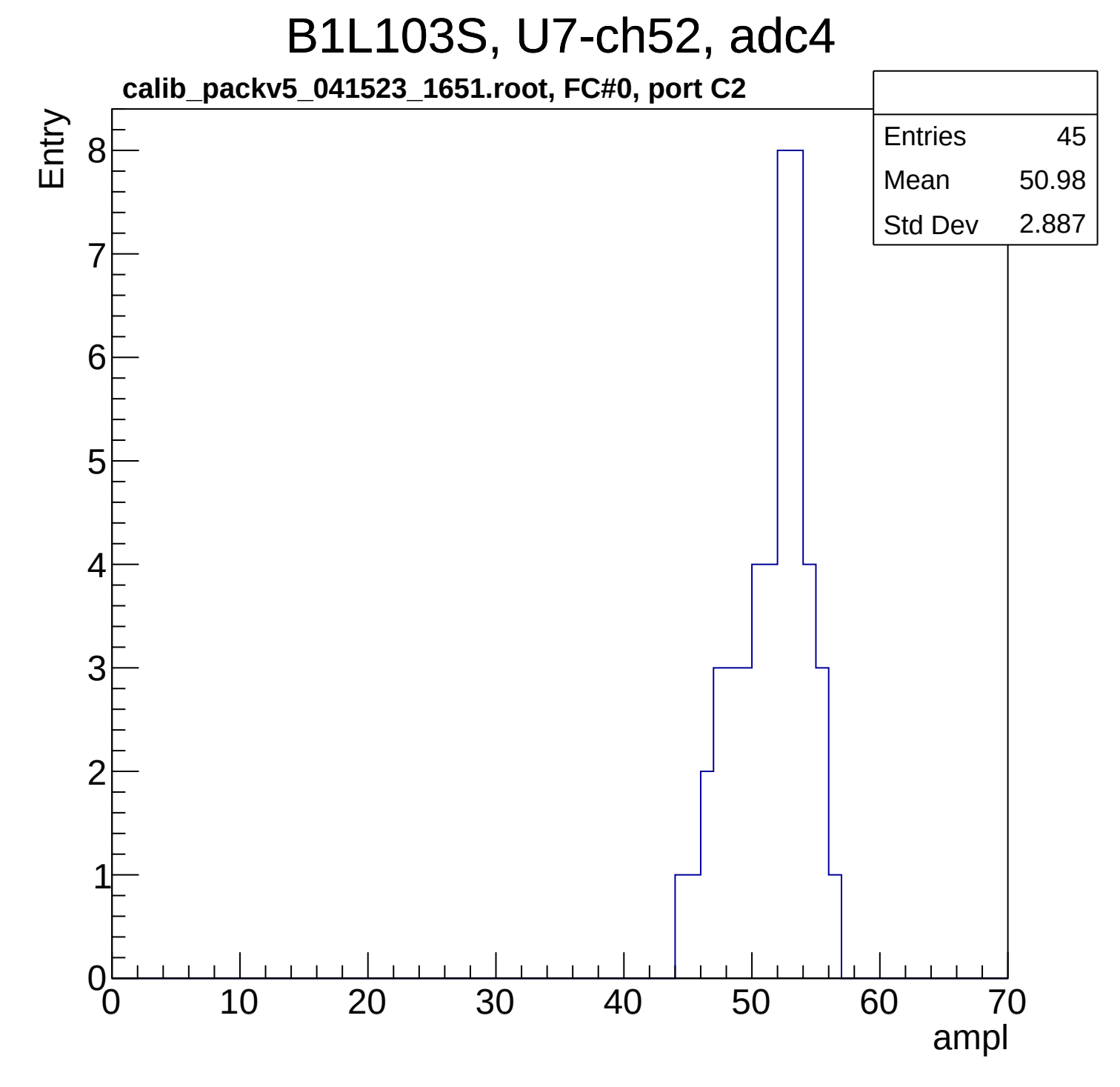
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch52, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 50.98
Std Dev 2.887
Entry
ampl
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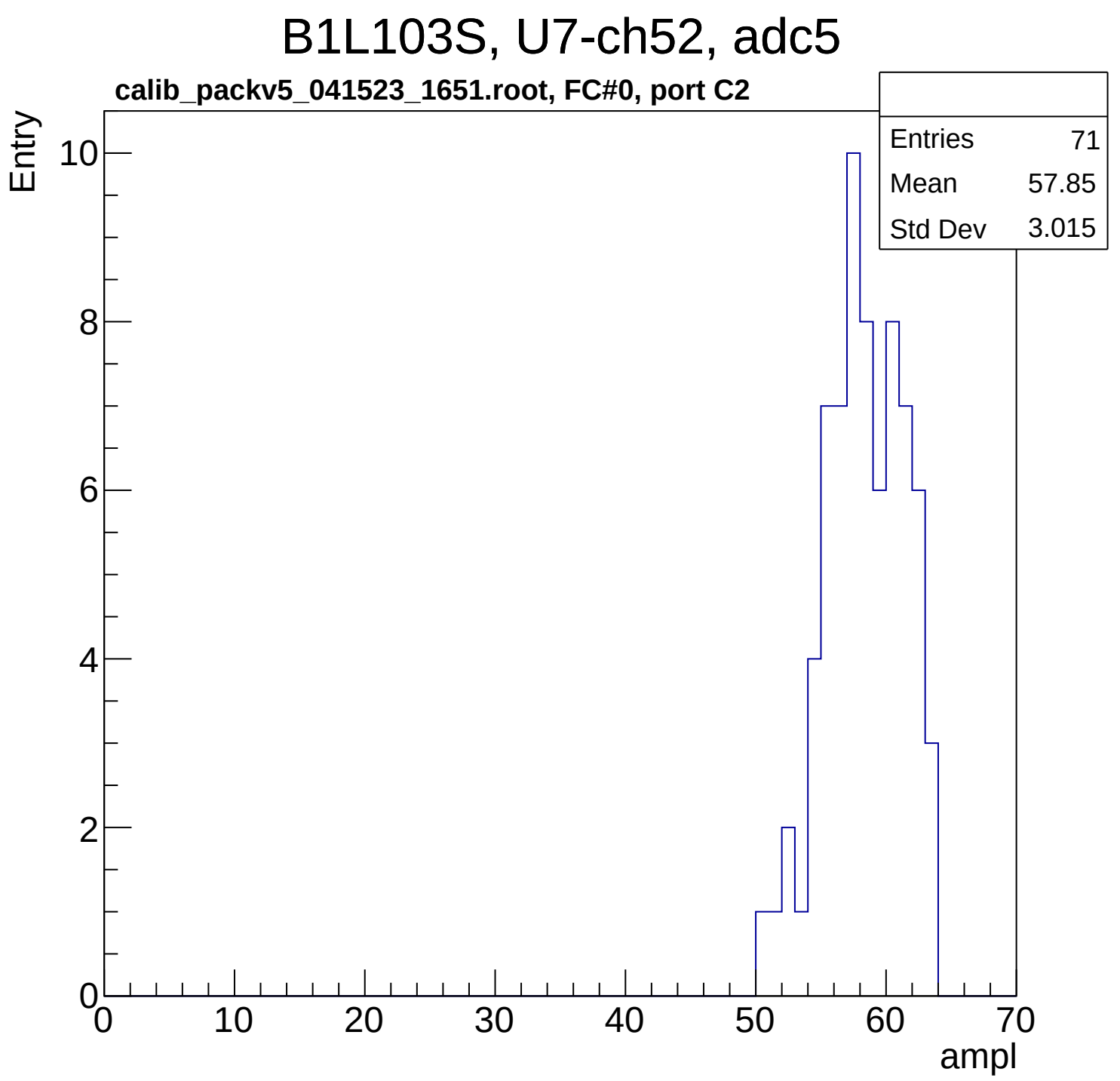
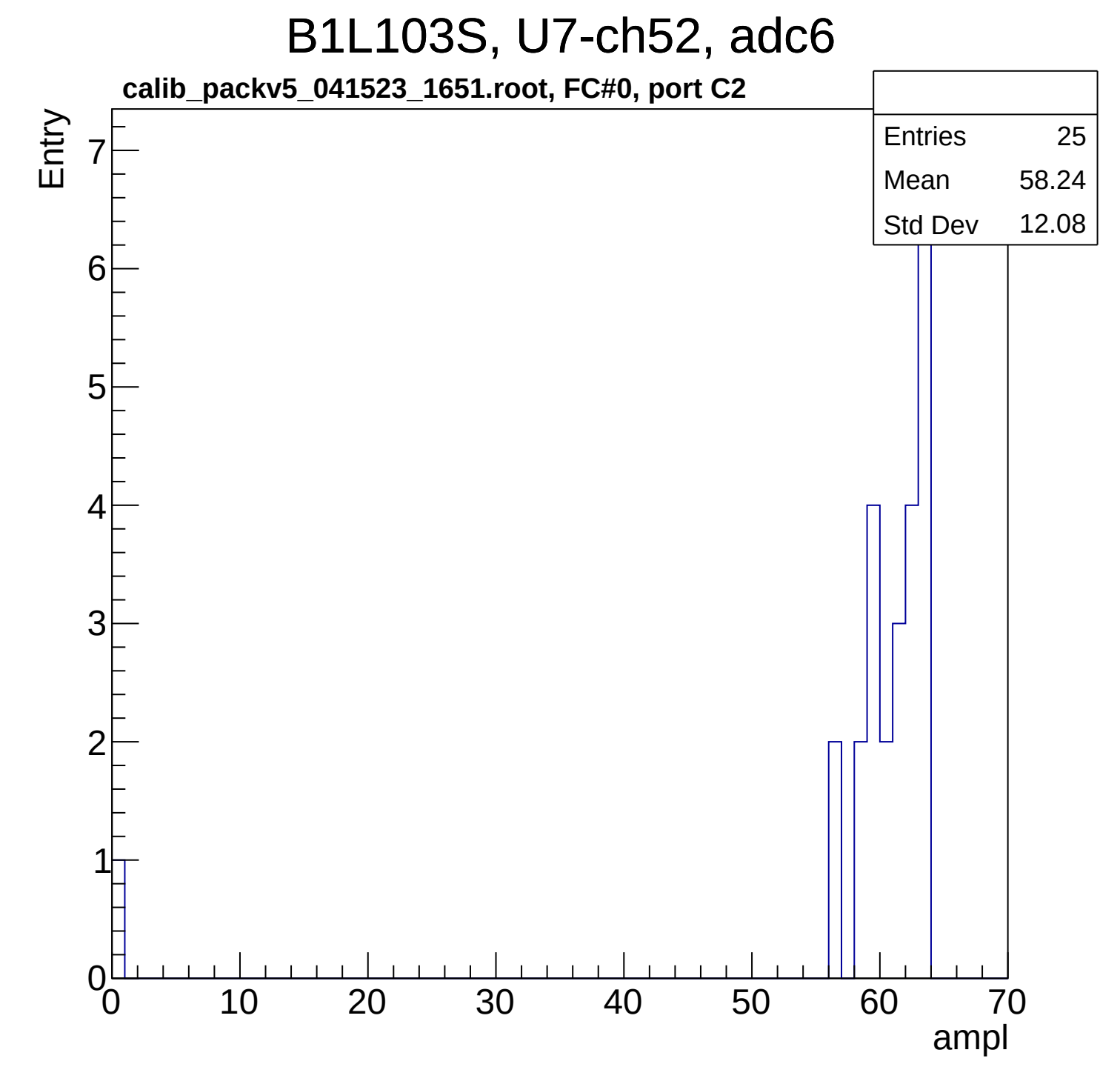
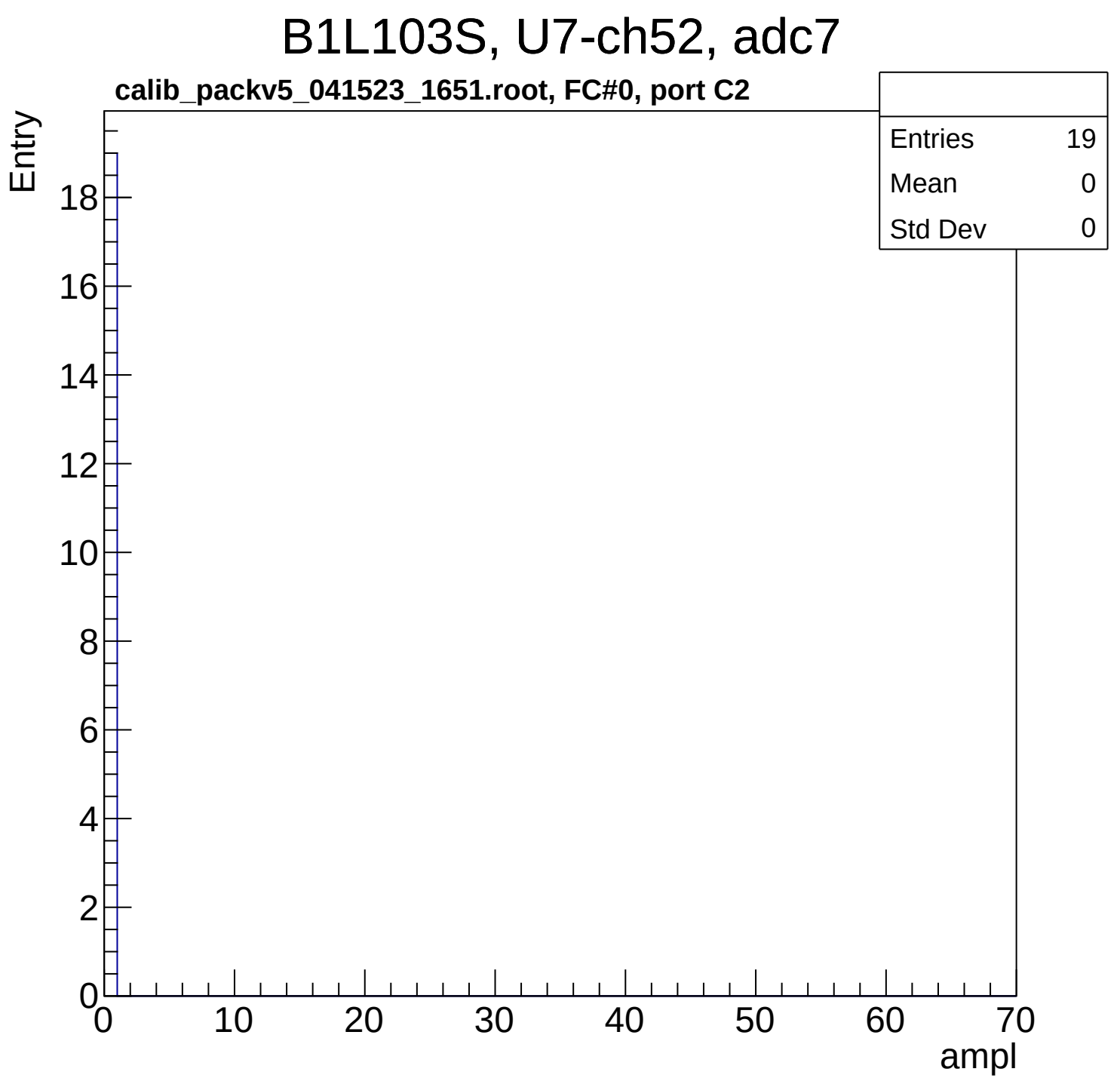
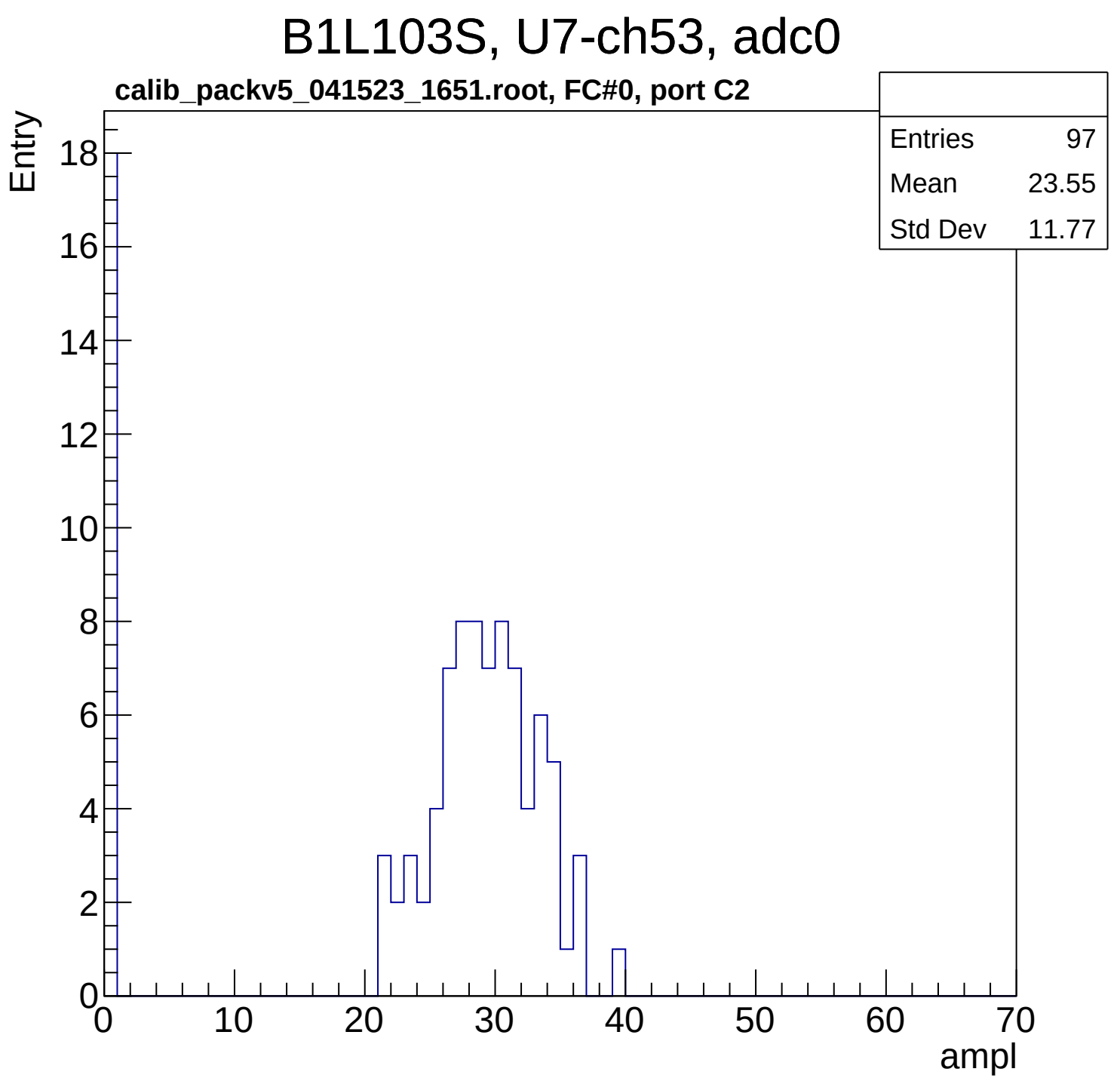
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch52, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 57.85
Std Dev 3.015
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch52, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 25
Mean 58.24
Std Dev 12.08
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U7-ch52, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch53, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 97
Mean 23.55
Std Dev 11.77
Entry
0
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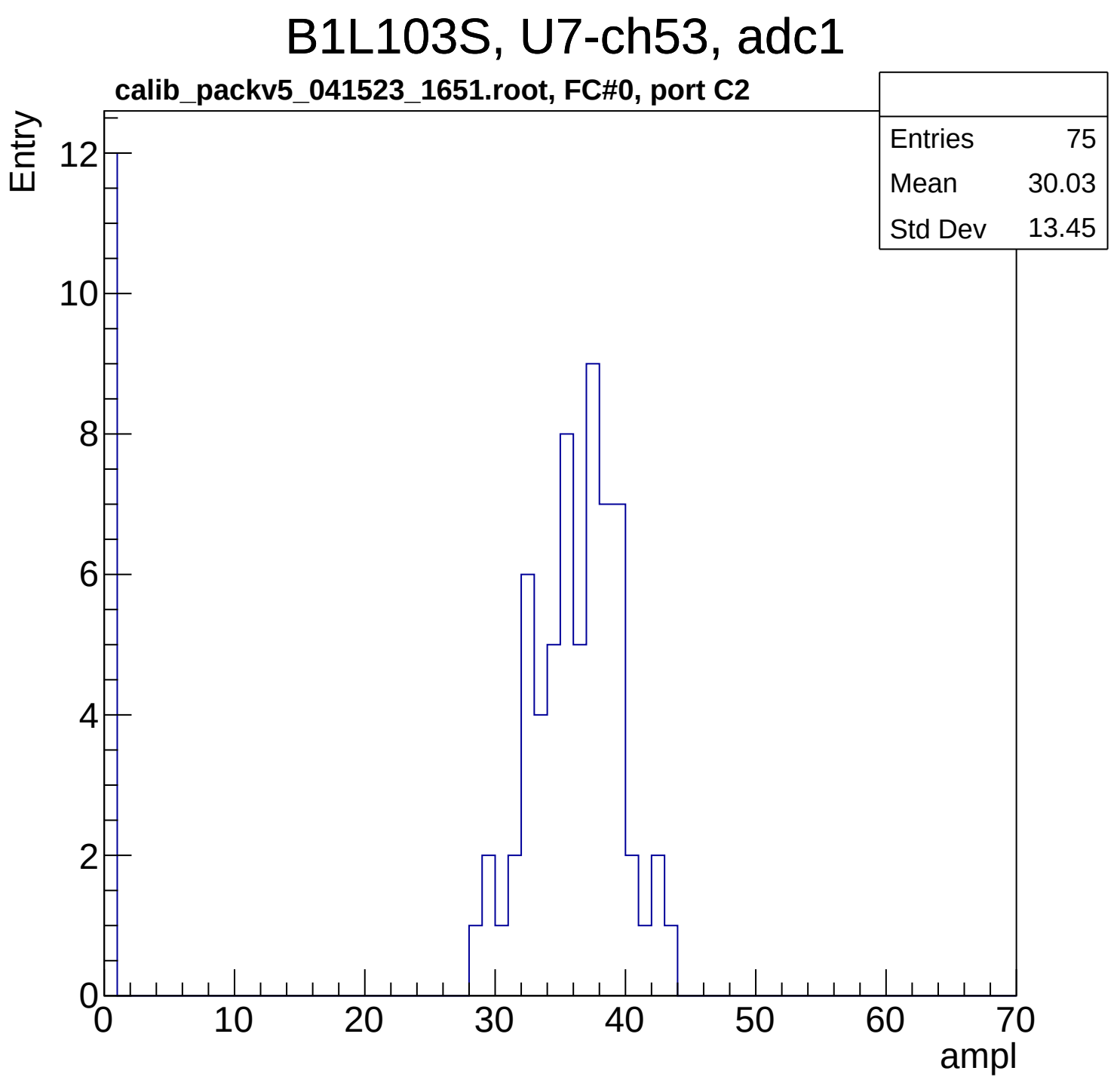
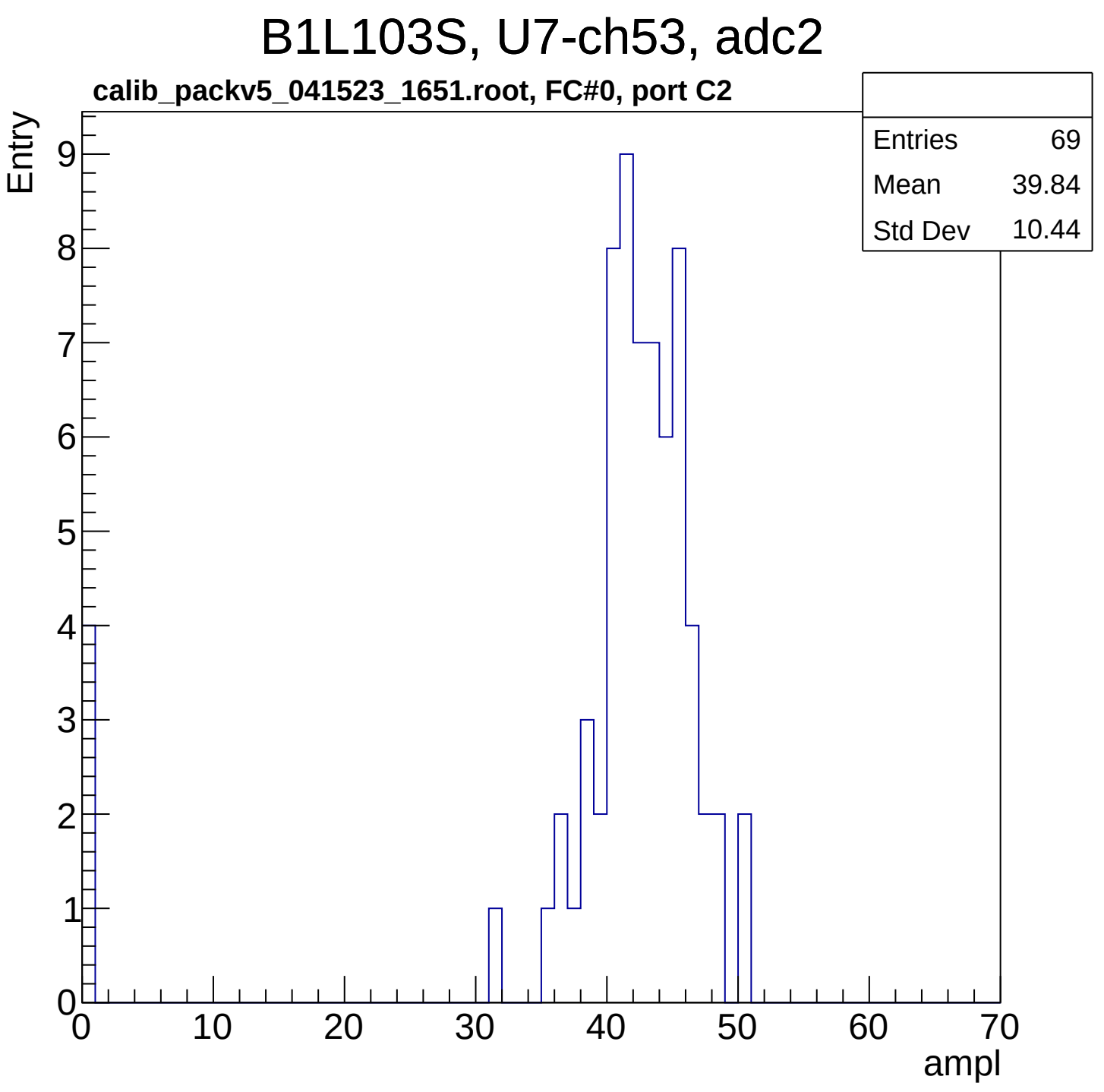
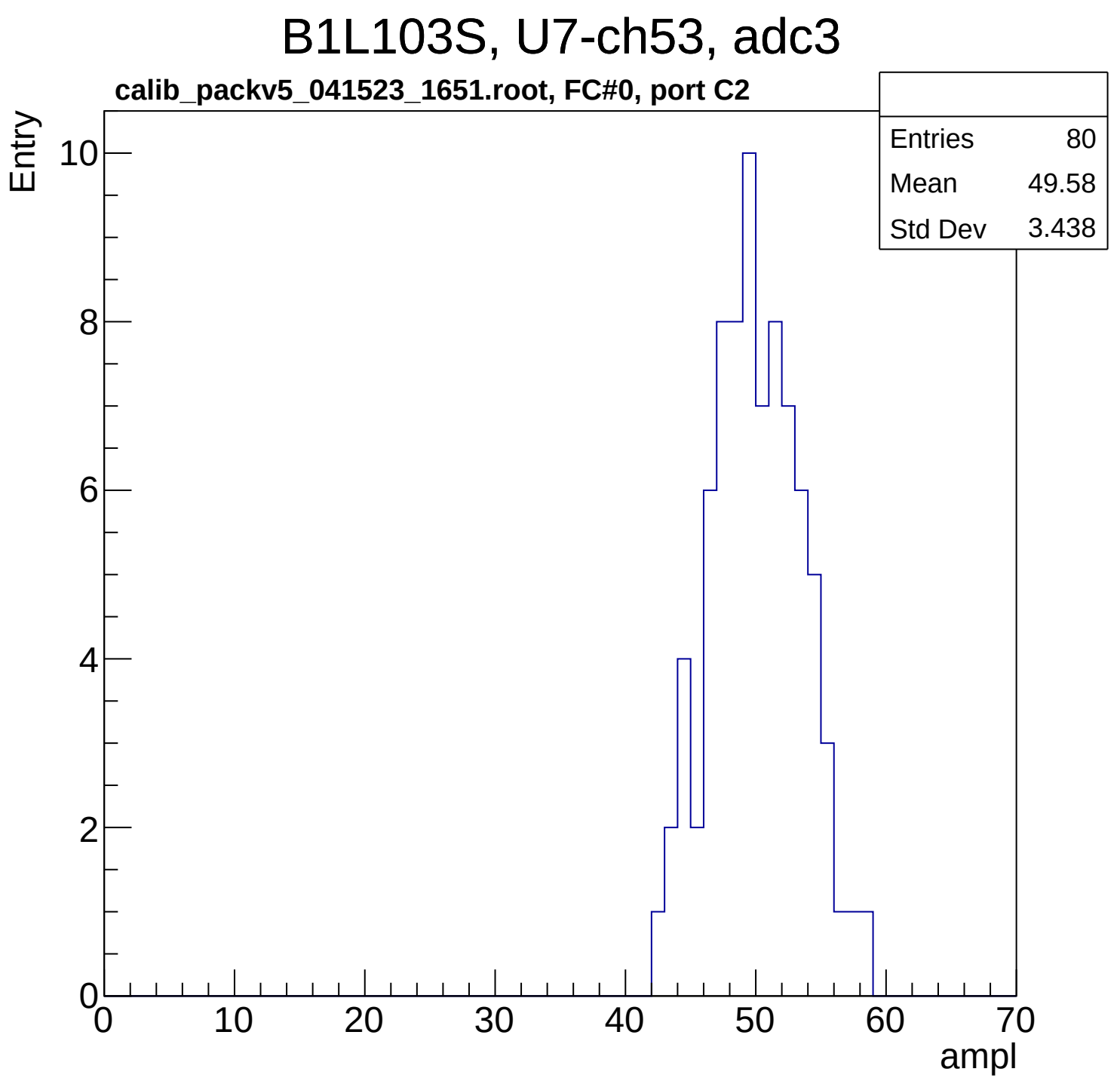
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch53, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 30.03
Std Dev 13.45
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch53, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 39.84
Std Dev 10.44
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U7-ch53, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 49.58
Std Dev 3.438
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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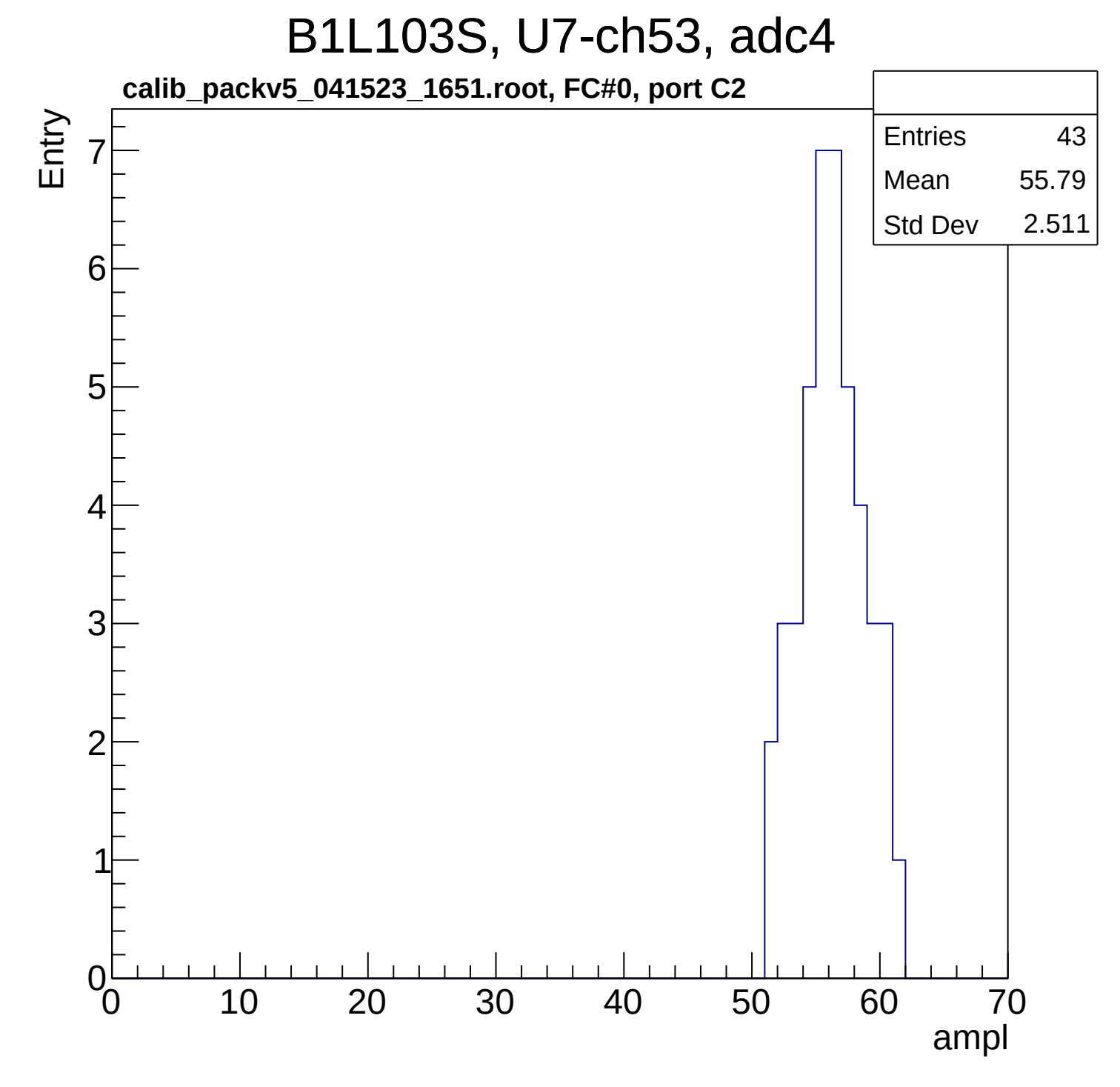
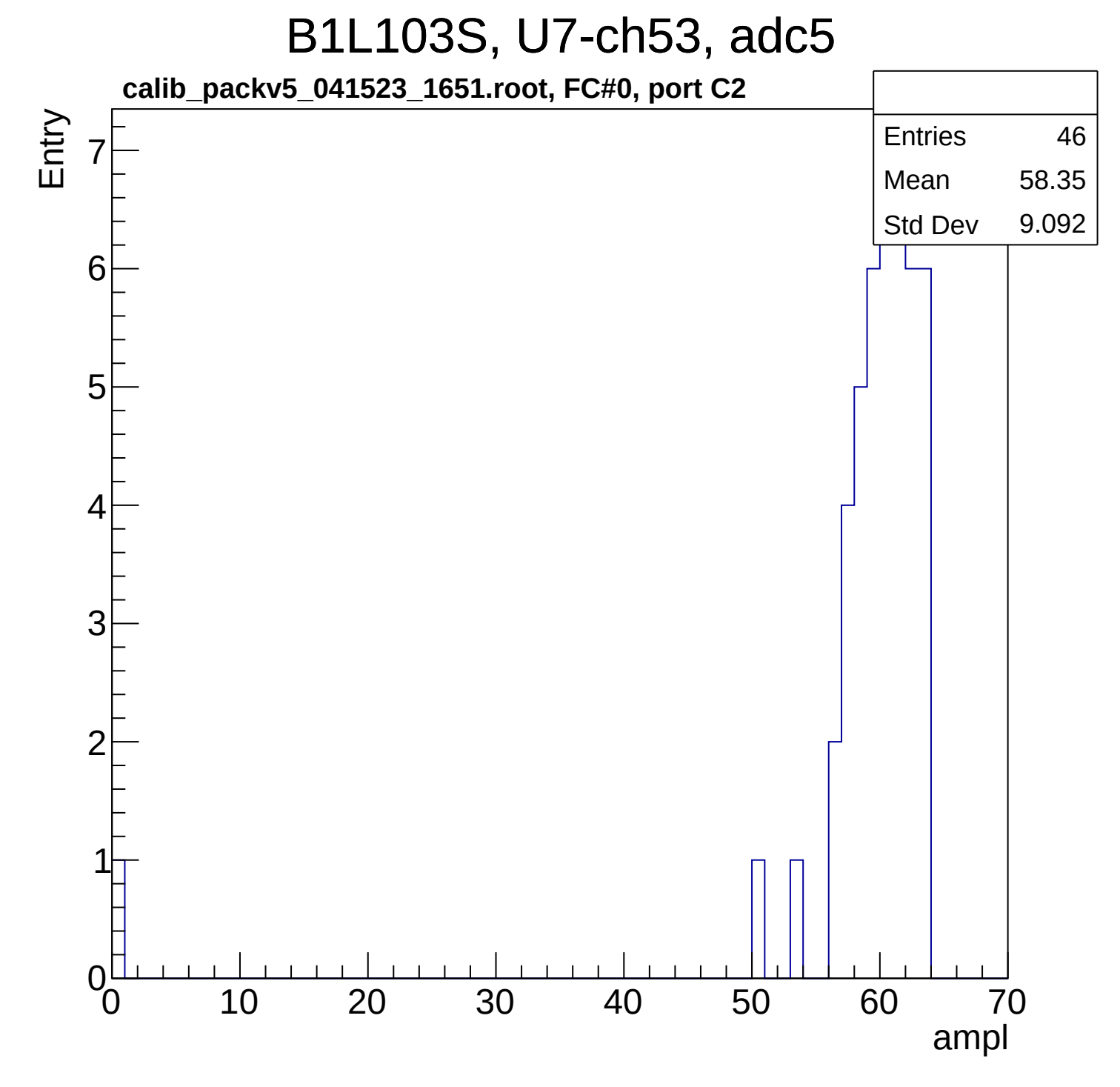

B1L103S, U7-ch53, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 43
Mean 55.79
Std Dev 2.511
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U7-ch53, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 58.35
Std Dev 9.092
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
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40
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60
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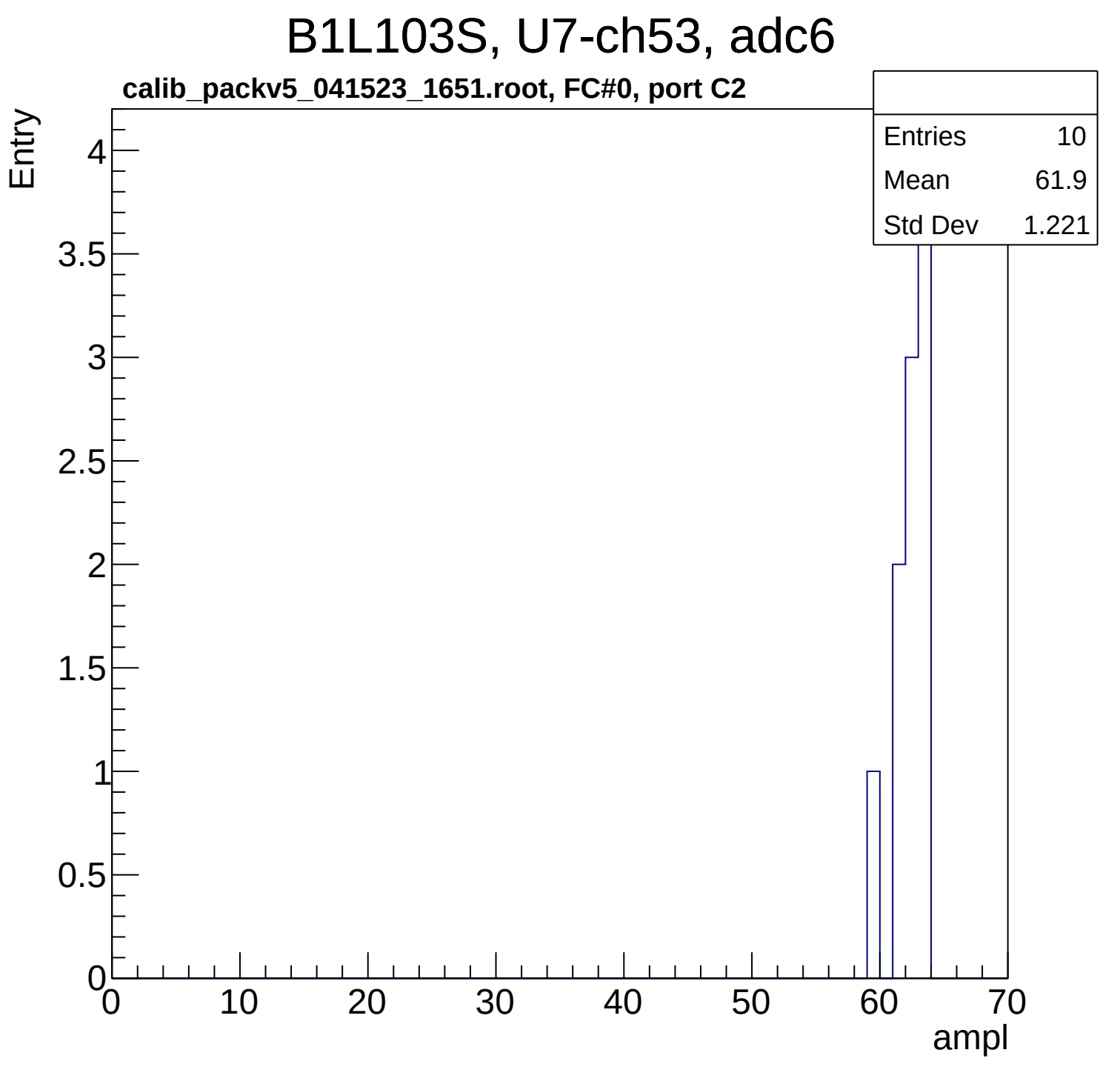
B1L103S, U7-ch53, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 61.9
Std Dev 1.221
Entry
ampl
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0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
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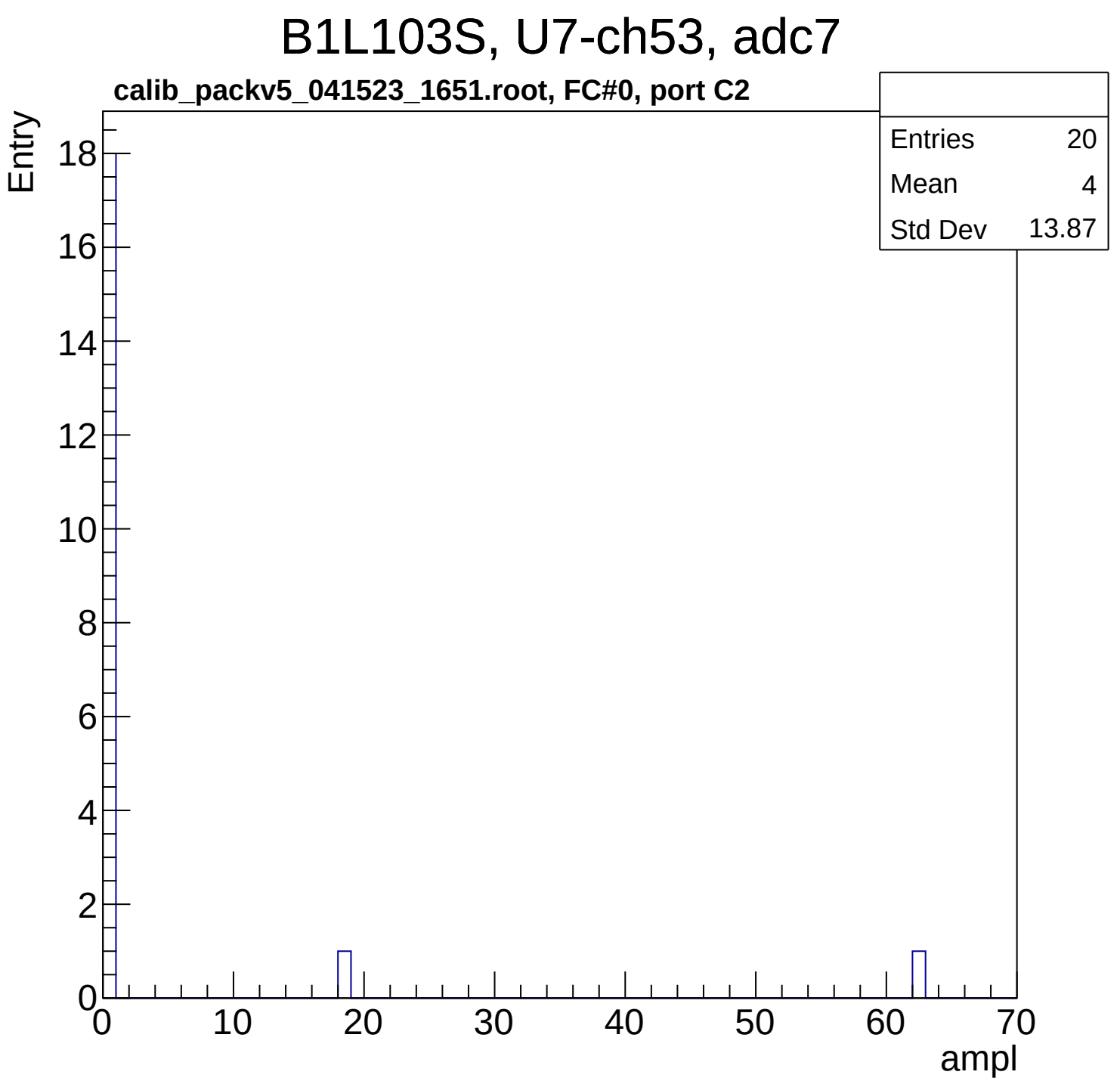
40
50
60
70


B1L103S, U7-ch53, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 4
Std Dev 13.87
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
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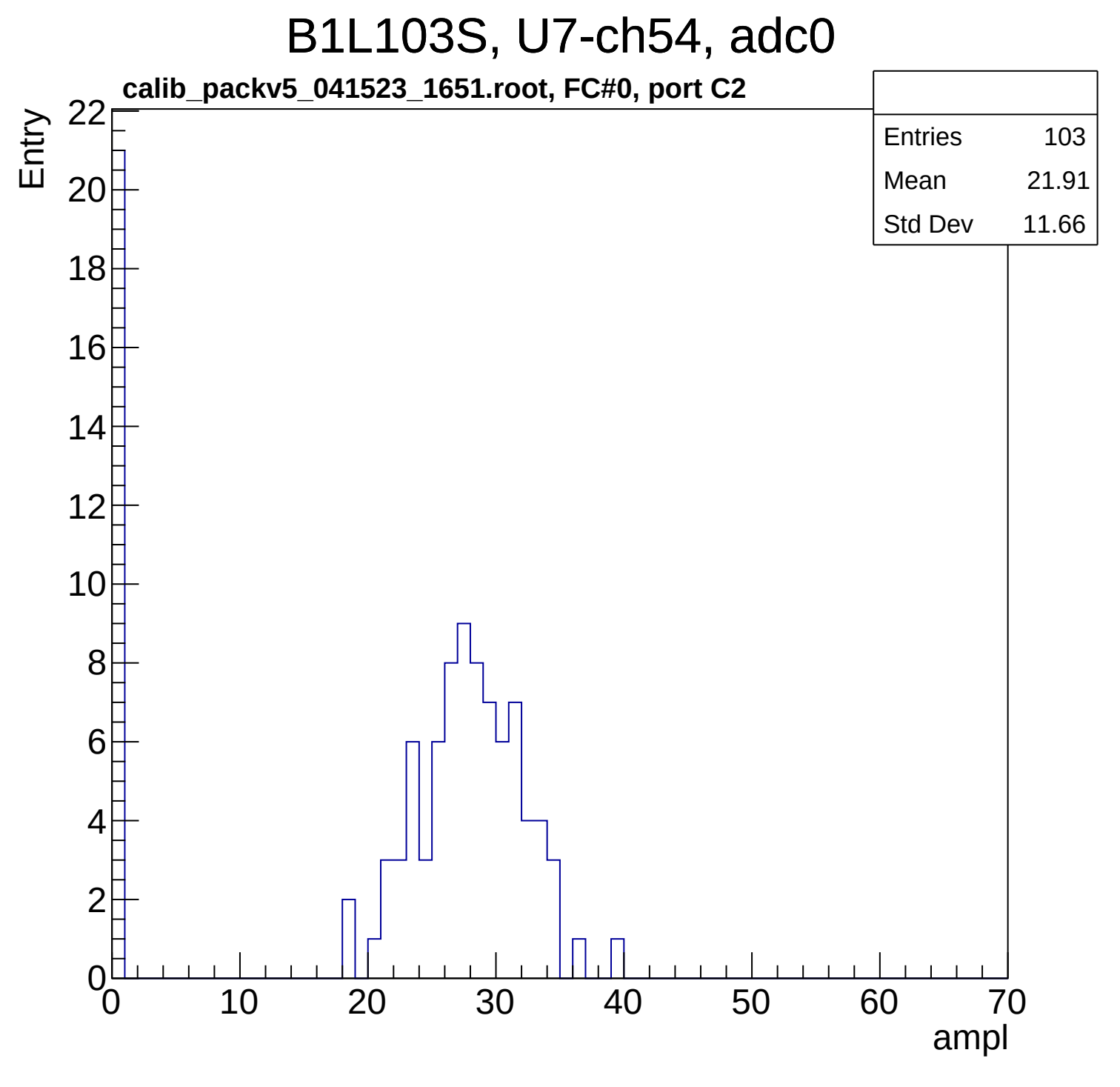
50
60
70
ampl


B1L103S, U7-ch54, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 103
Mean 21.91
Std Dev 11.66
Entry
ampl
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4
6
8
10
12
14
16
18
20
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0
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60
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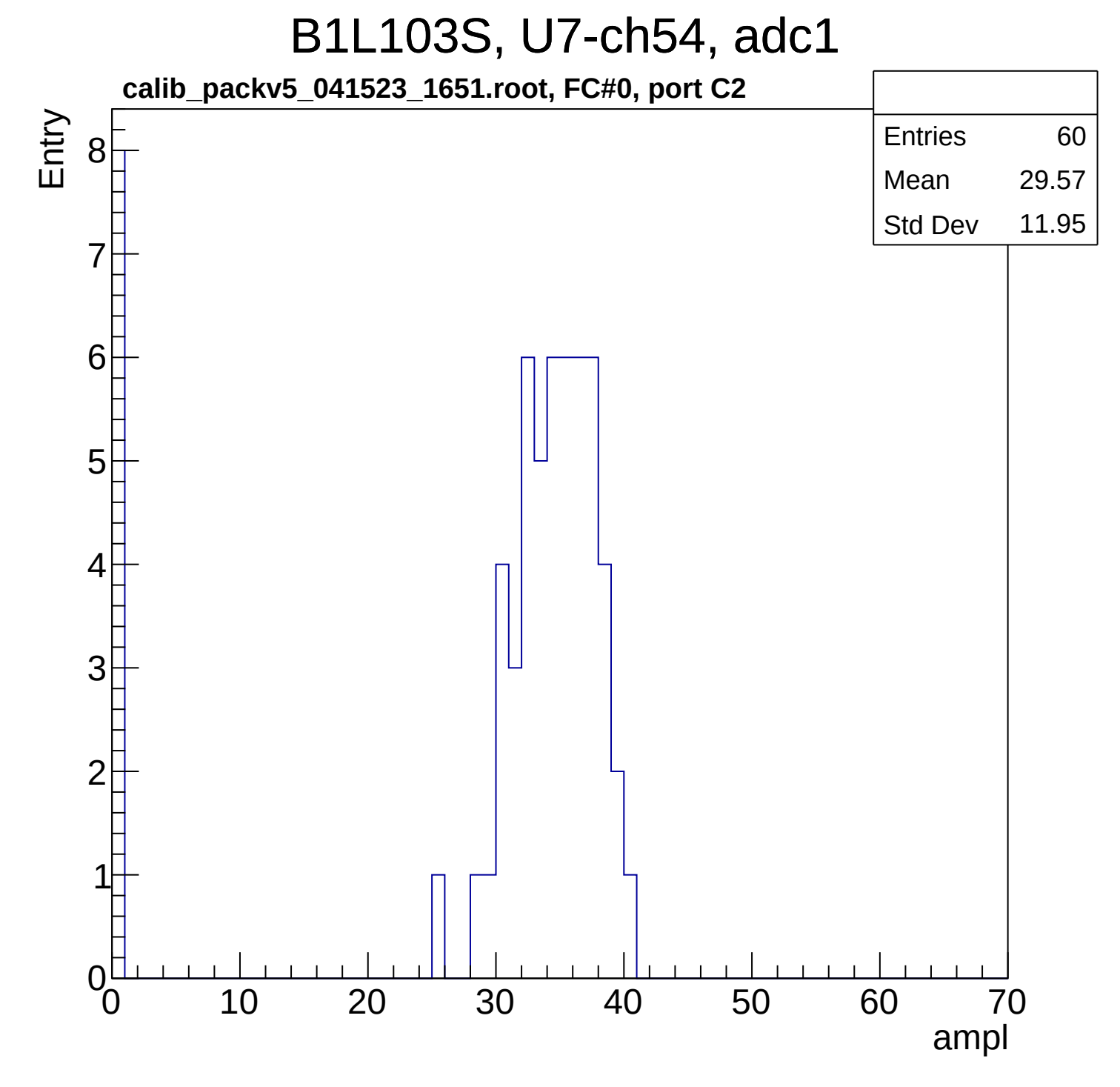
B1L103S, U7-ch54, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 29.57
Std Dev 11.95
Entry
ampl
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2
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4
5
6
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60
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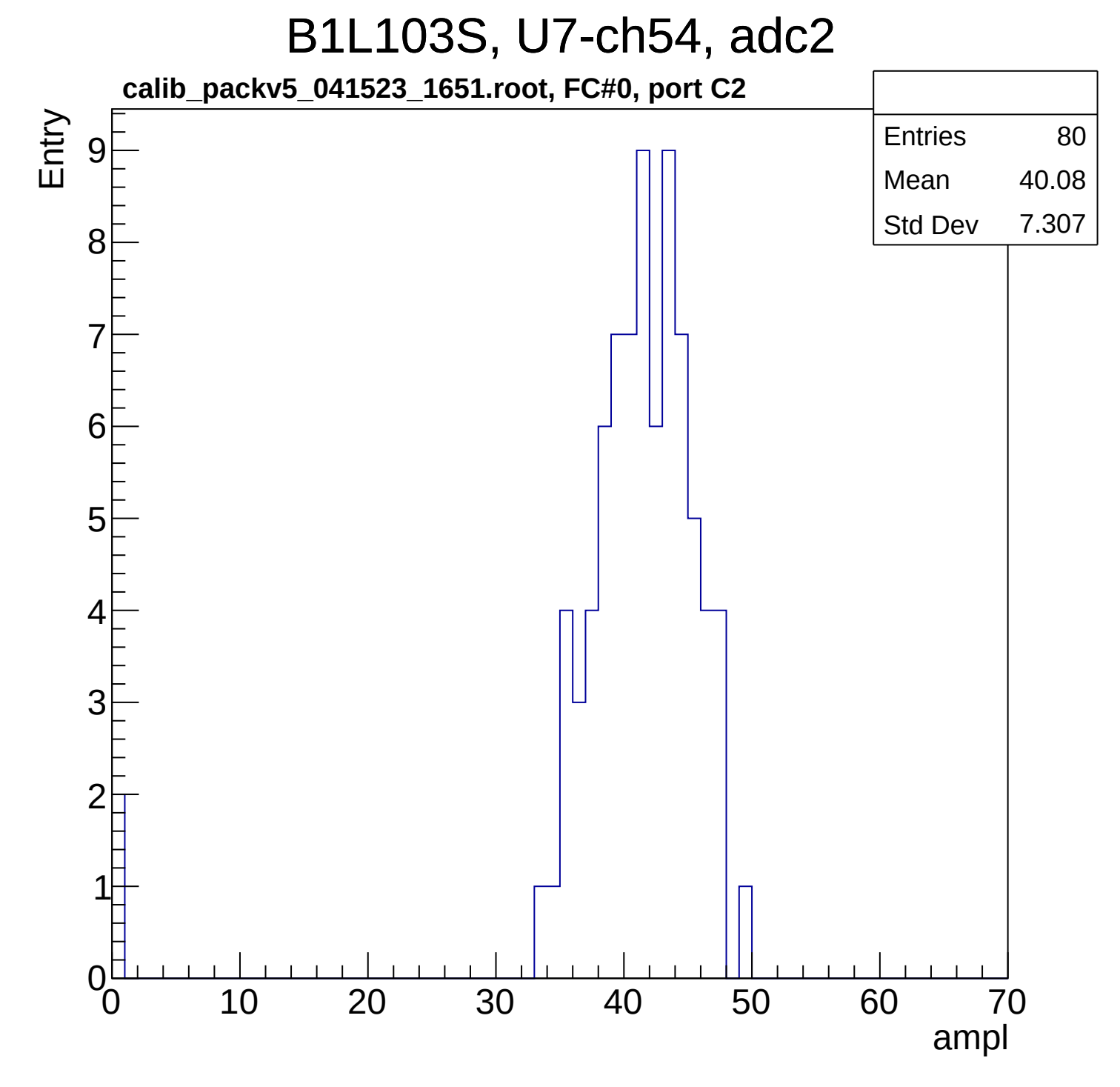
B1L103S, U7-ch54, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 40.08
Std Dev 7.307
Entry
ampl
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2
3
4
5
6
7
8
9
0
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40
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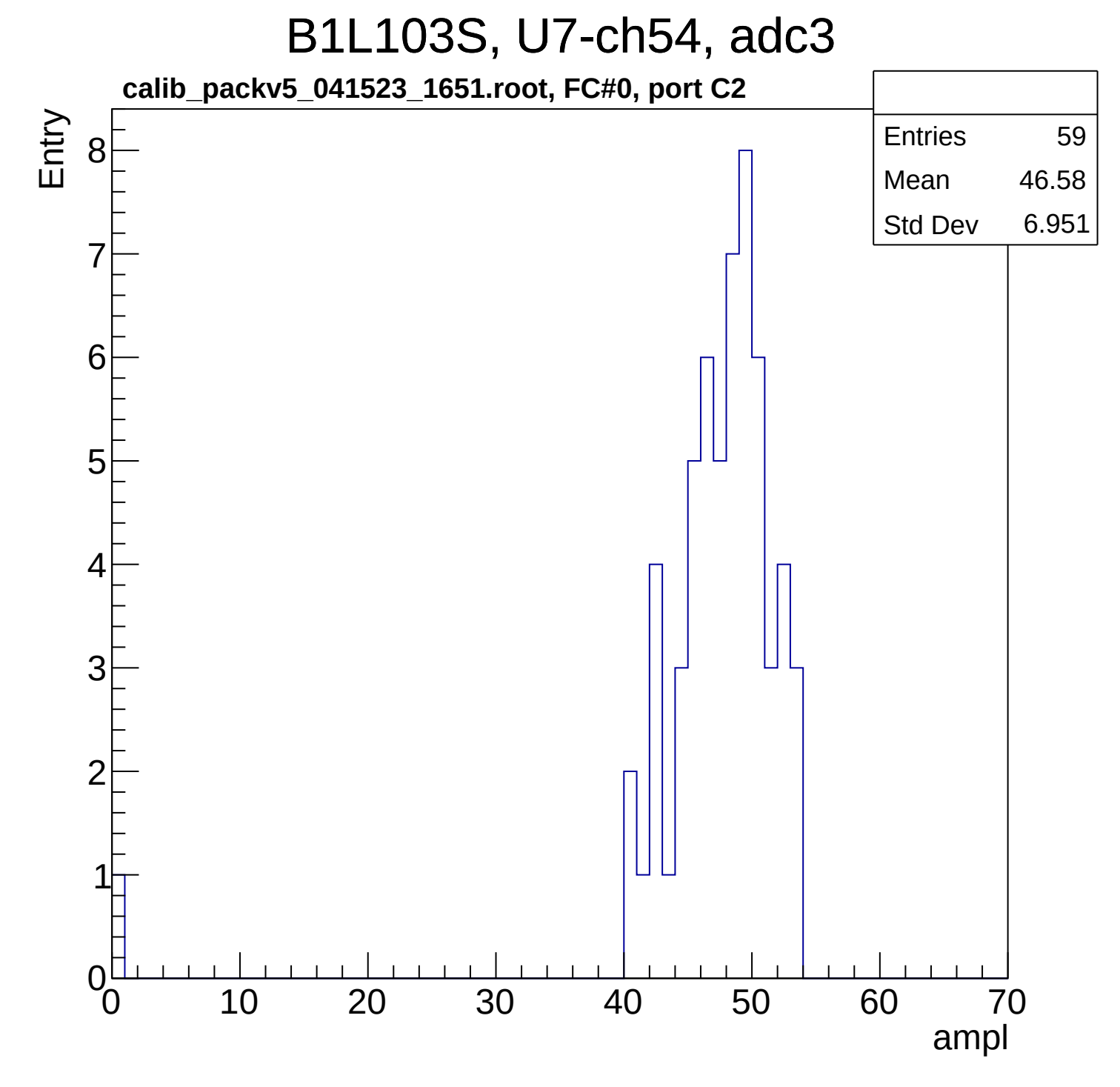
60
70


B1L103S, U7-ch54, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 46.58
Std Dev 6.951
Entry
ampl
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1
2
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4
5
6
7
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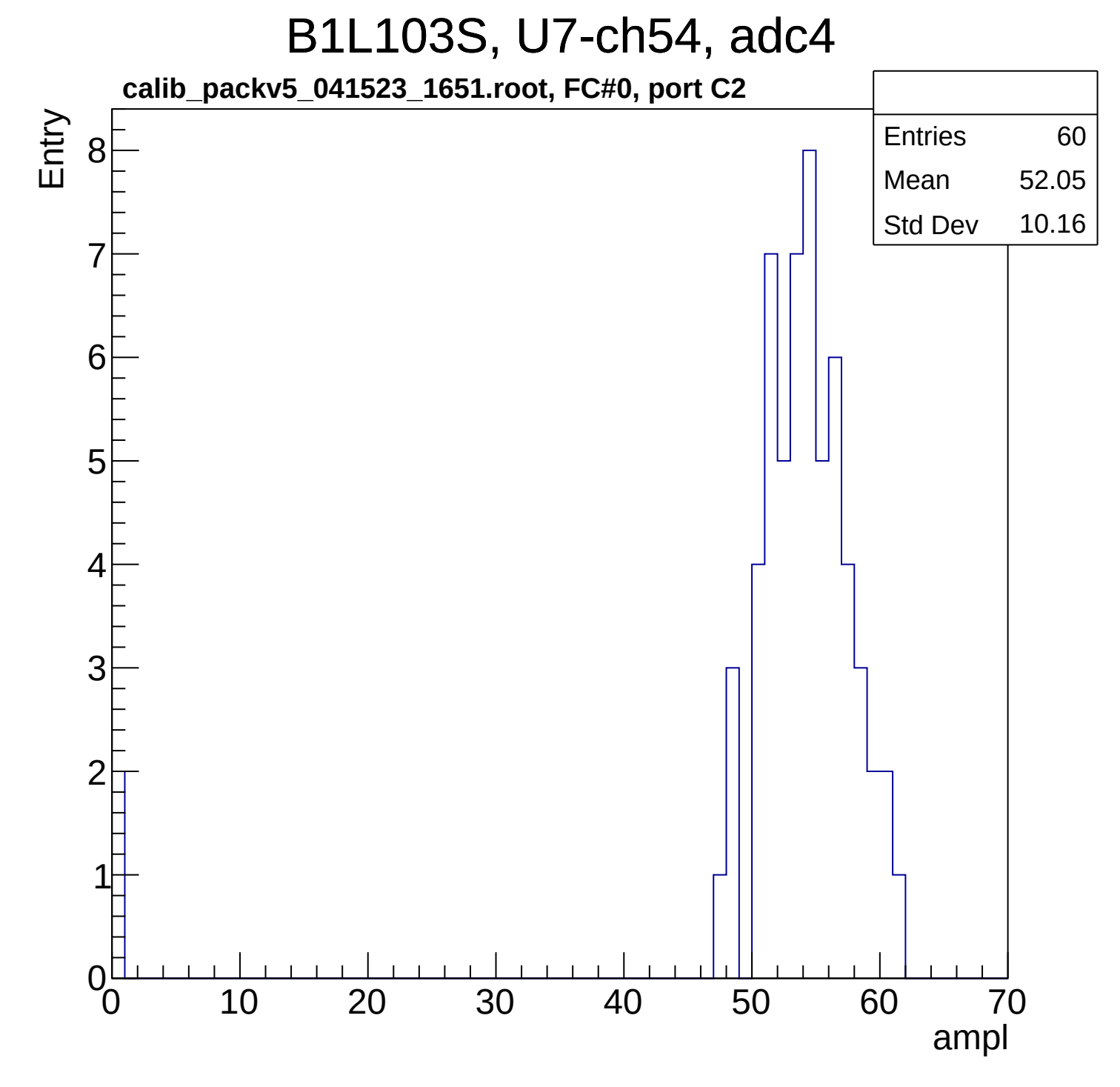
0
10
20
30
40
50
60
70


B1L103S, U7-ch54, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 52.05
Std Dev 10.16
Entry
ampl
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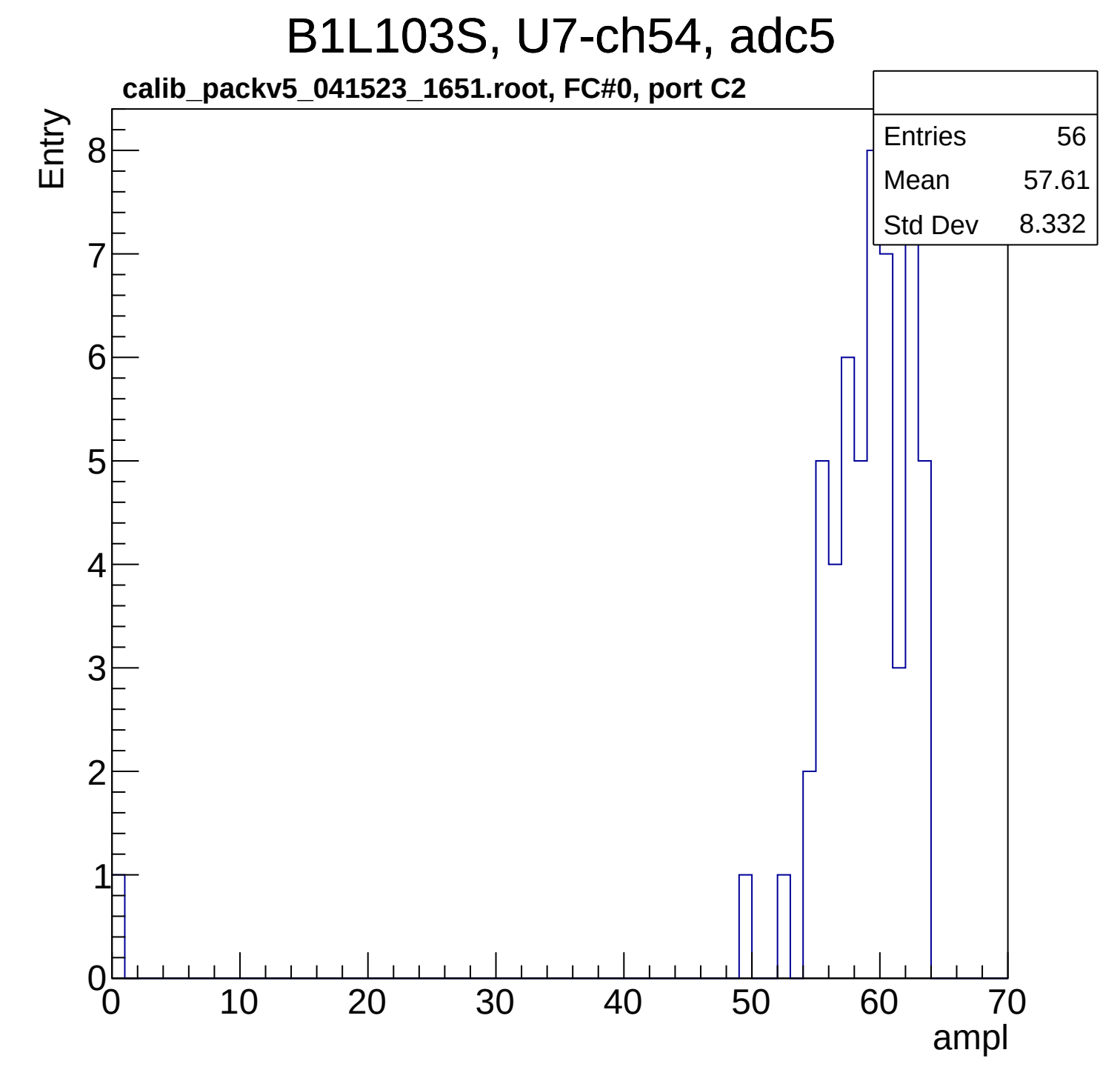
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch54, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 57.61
Std Dev 8.332
Entry
ampl
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2
3
4
5
6
7
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0
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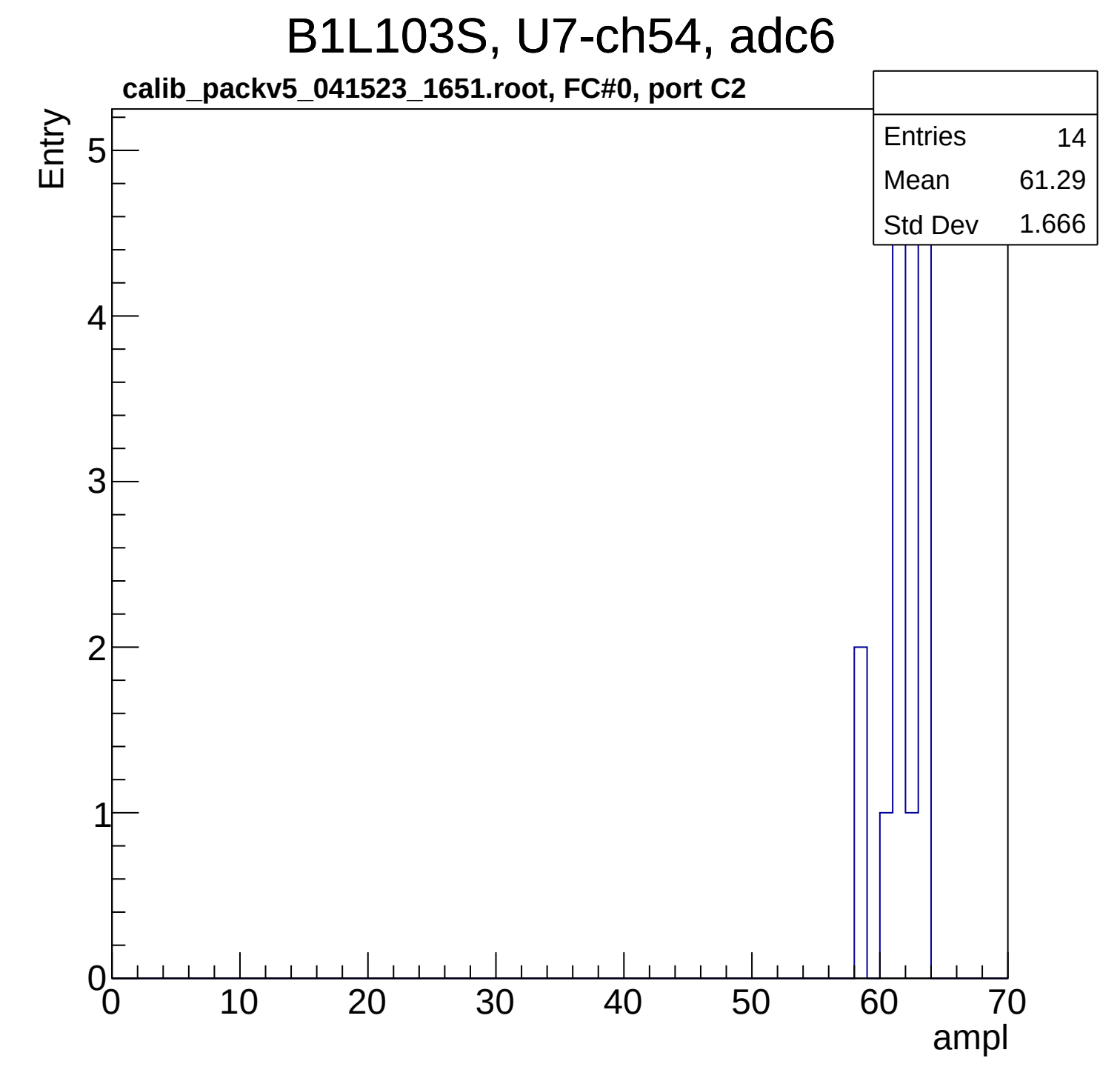
60
70


B1L103S, U7-ch54, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 14
Mean 61.29
Std Dev 1.666
Entry
ampl
0
1
2
3
4
5
0
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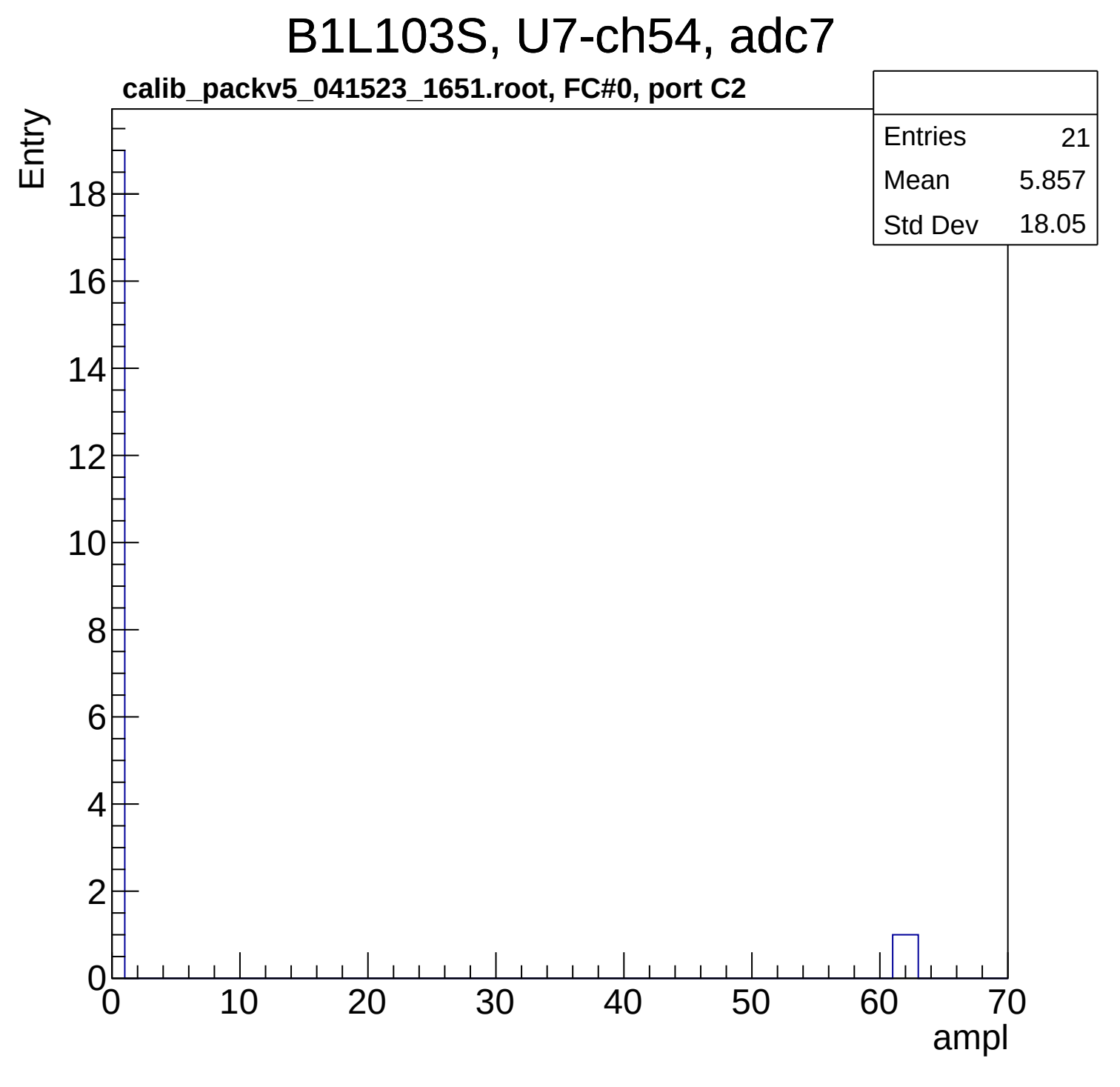
20
30
40
50
60
70


B1L103S, U7-ch54, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 5.857
Std Dev 18.05
Entry
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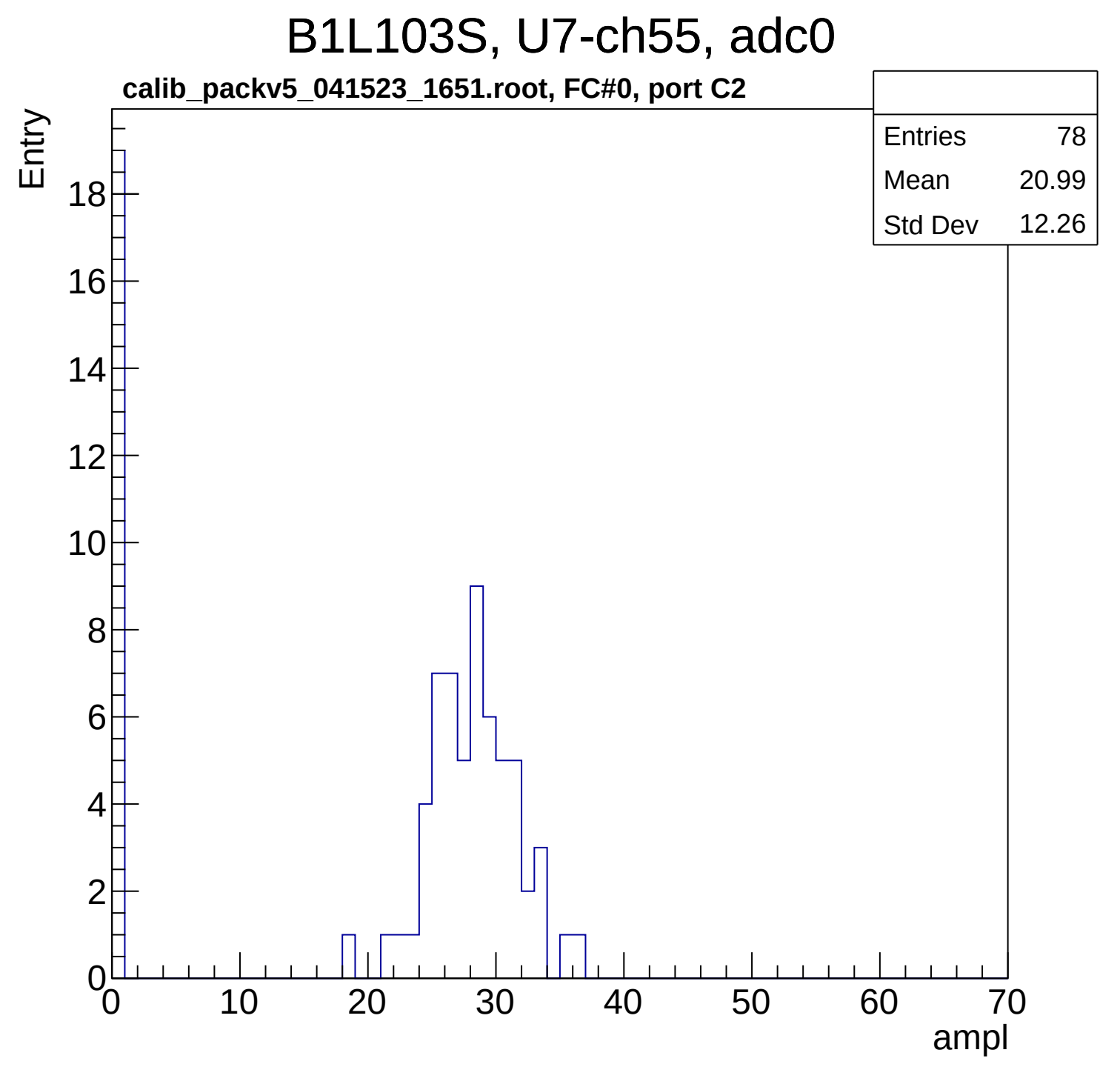
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch55, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 20.99
Std Dev 12.26
Entry
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6
8
10
12
14
16
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10
20
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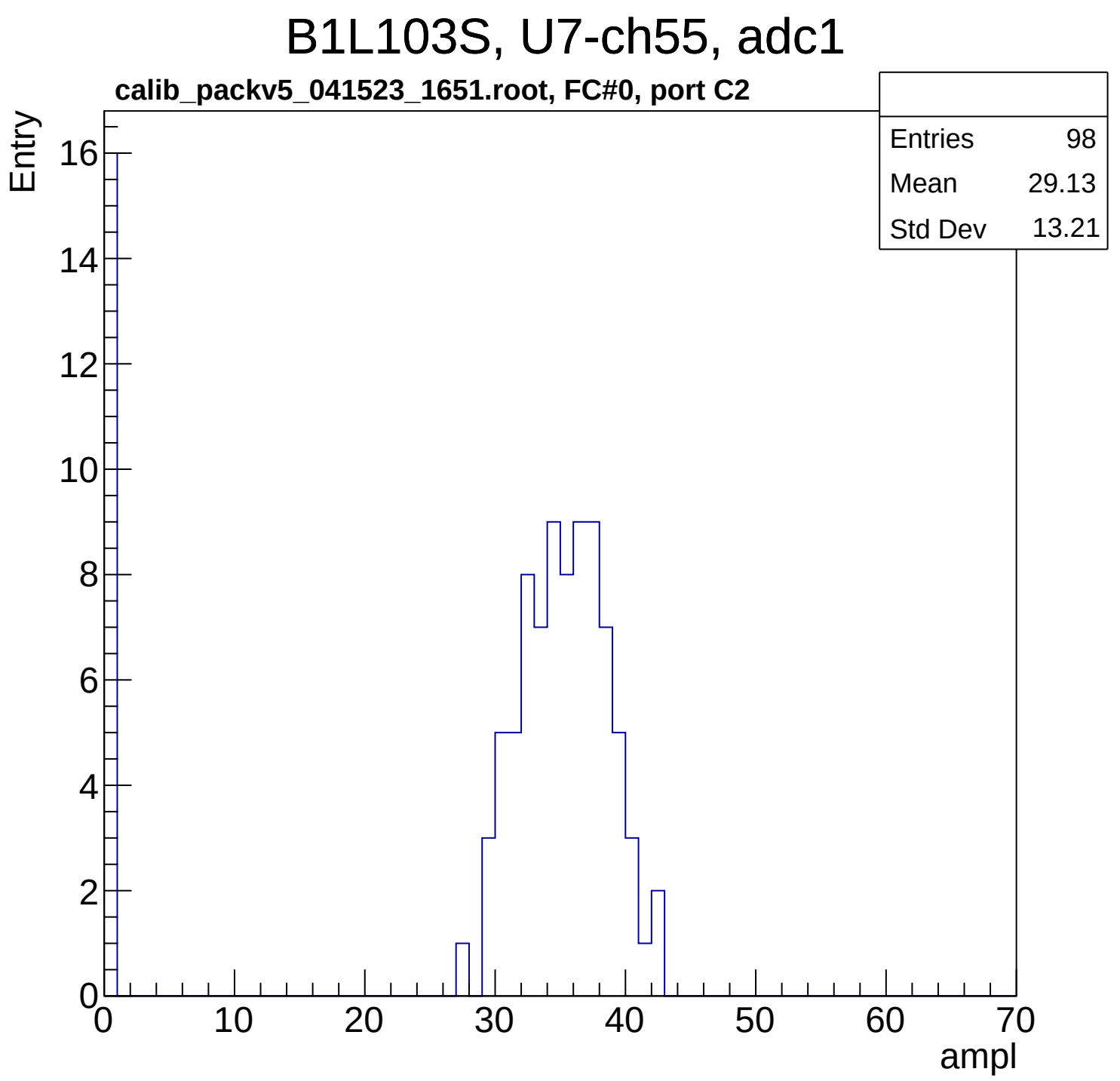
40
50
60
70
ampl


B1L103S, U7-ch55, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 98
Mean 29.13
Std Dev 13.21
Entry
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16
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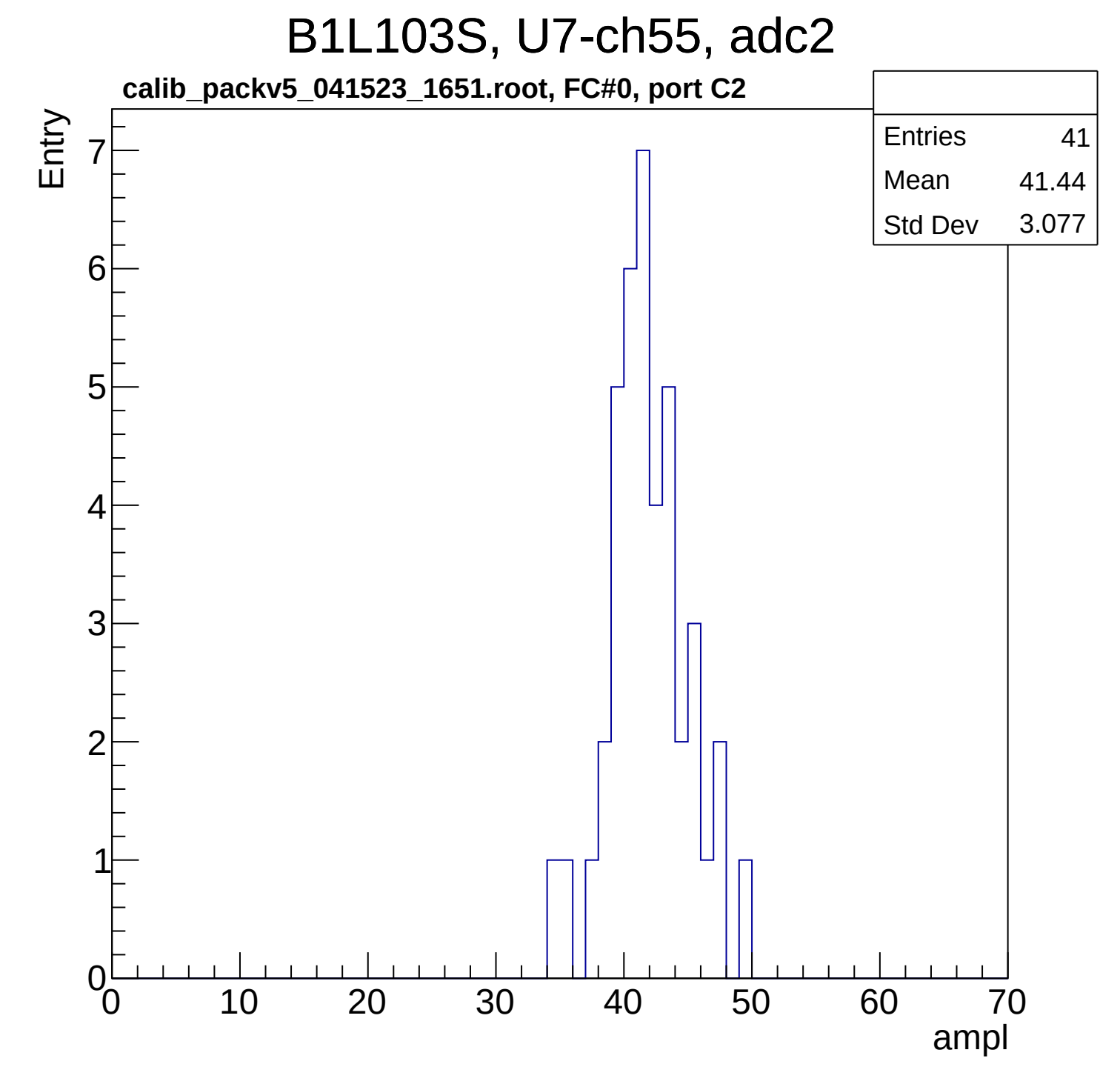
50
60
70
ampl


B1L103S, U7-ch55, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 41
Mean 41.44
Std Dev 3.077
Entry
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0
10
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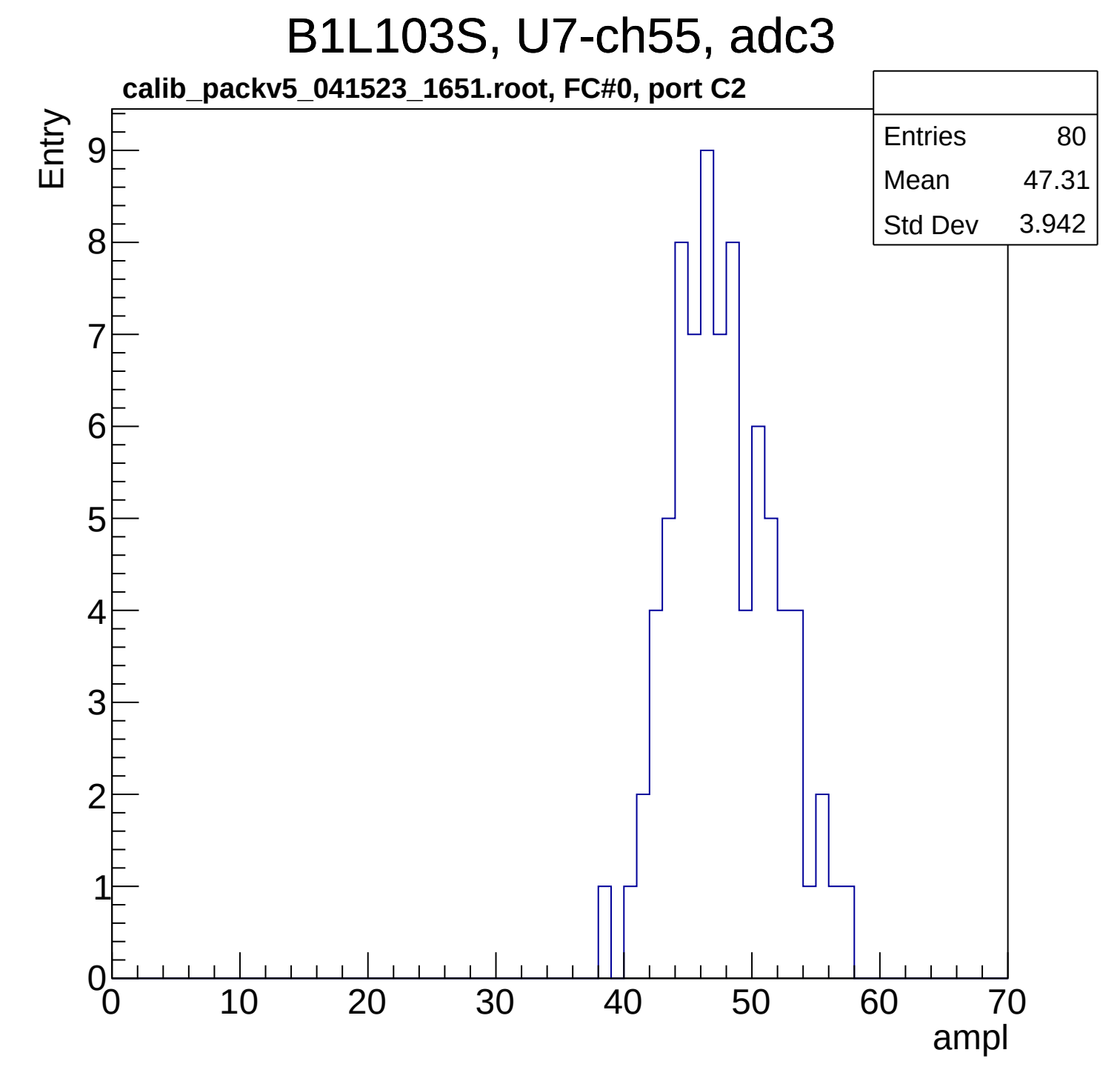
50
60
70
ampl


B1L103S, U7-ch55, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 47.31
Std Dev 3.942
Entry
ampl
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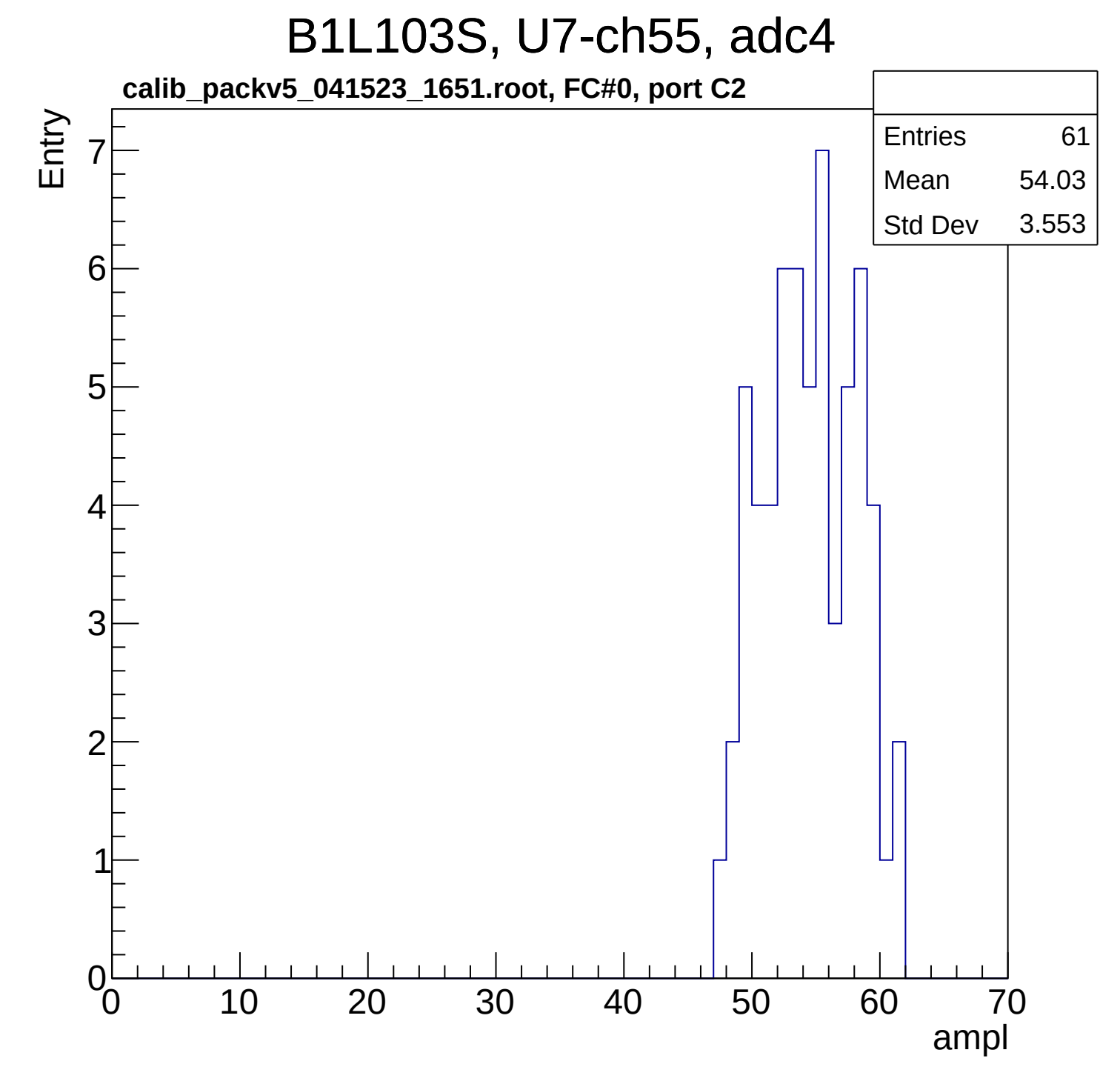
60
70


B1L103S, U7-ch55, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 54.03
Std Dev 3.553
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
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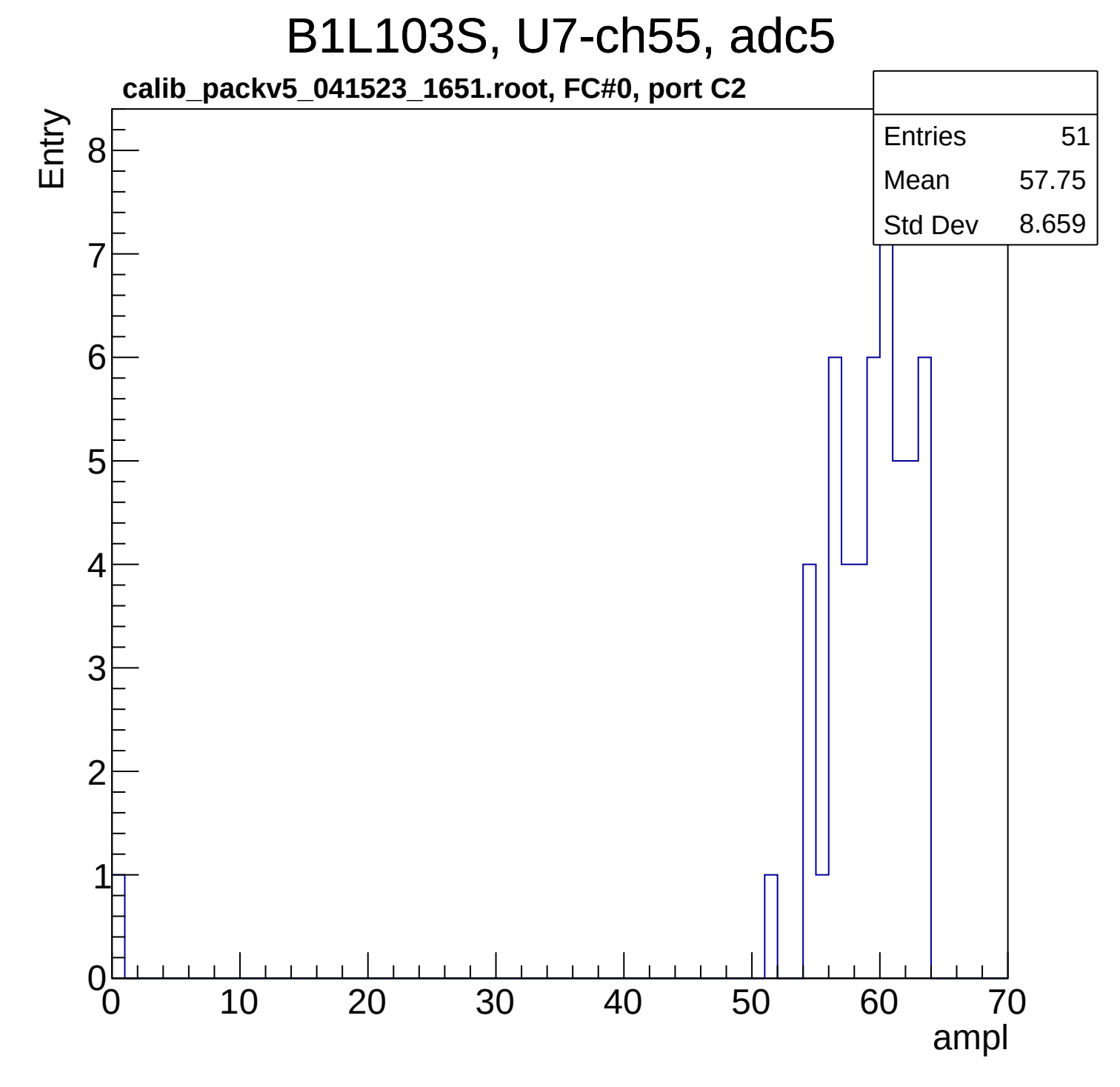
B1L103S, U7-ch55, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 57.75
Std Dev 8.659
Entry
ampl
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2
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0
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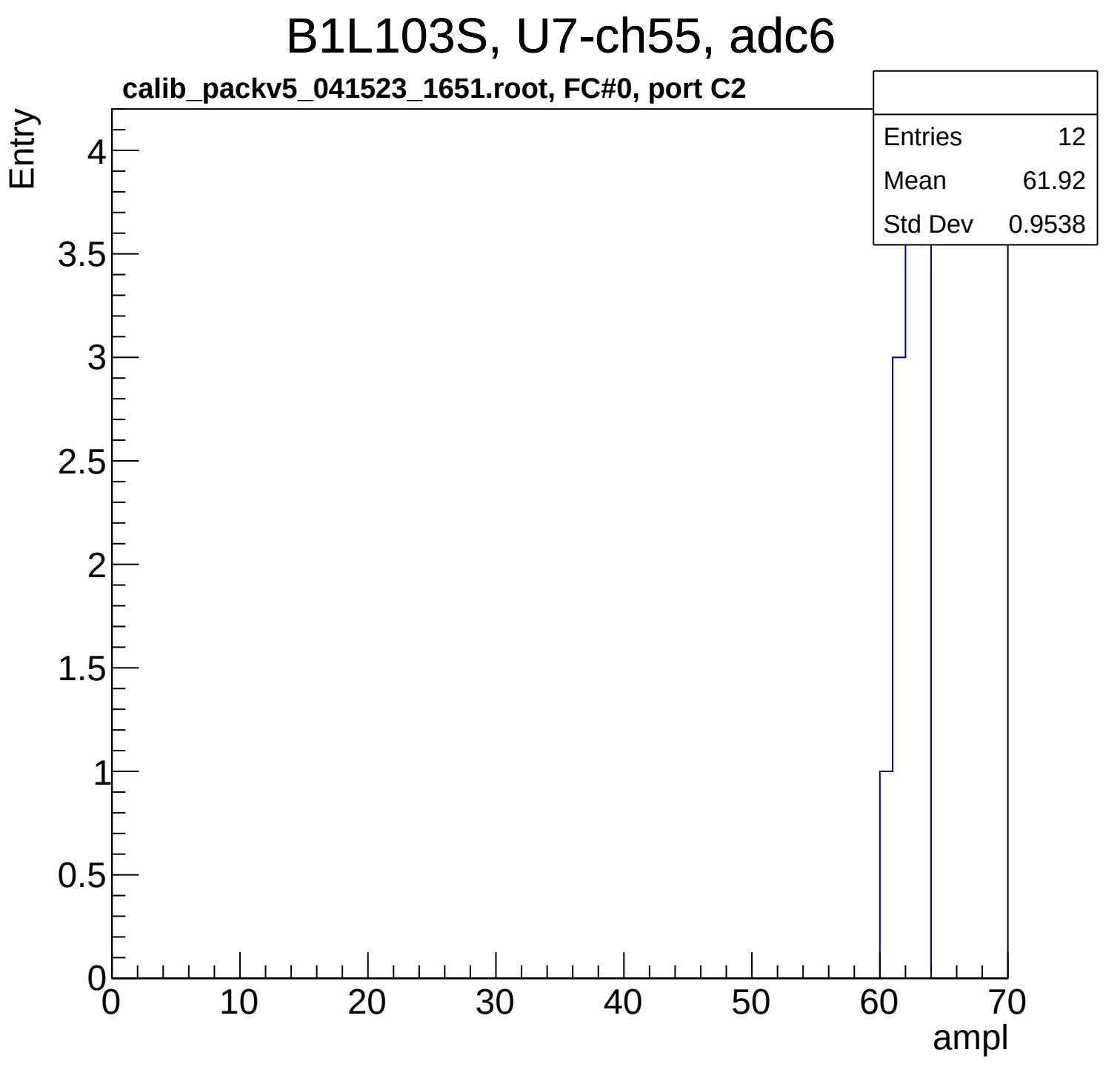
B1L103S, U7-ch55, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 61.92
Std Dev 0.9538
Entry
ampl
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1.5
2
2.5
3
3.5
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0
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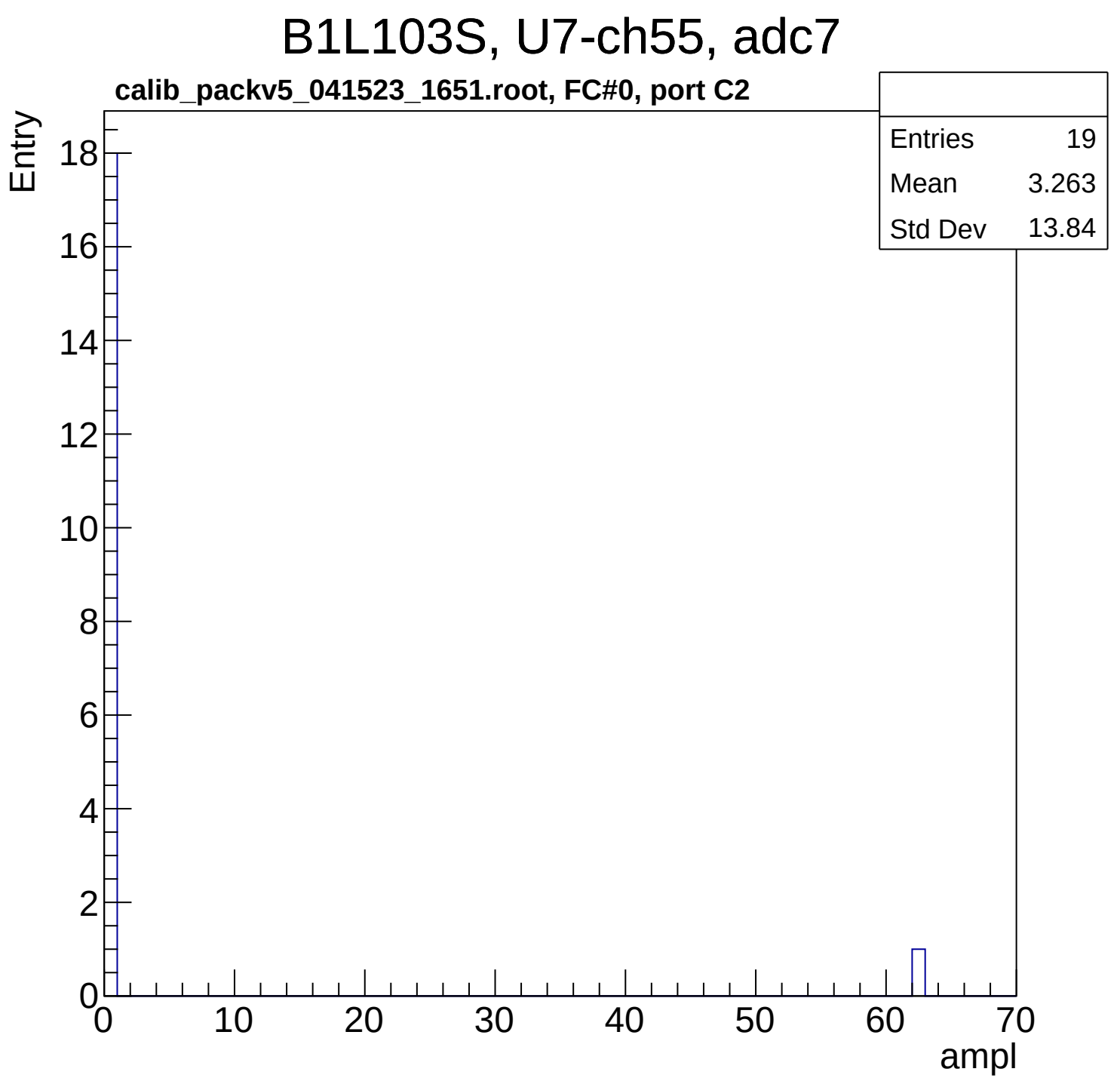
B1L103S, U7-ch55, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 3.263
Std Dev 13.84
Entry
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10
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14
16
18
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10
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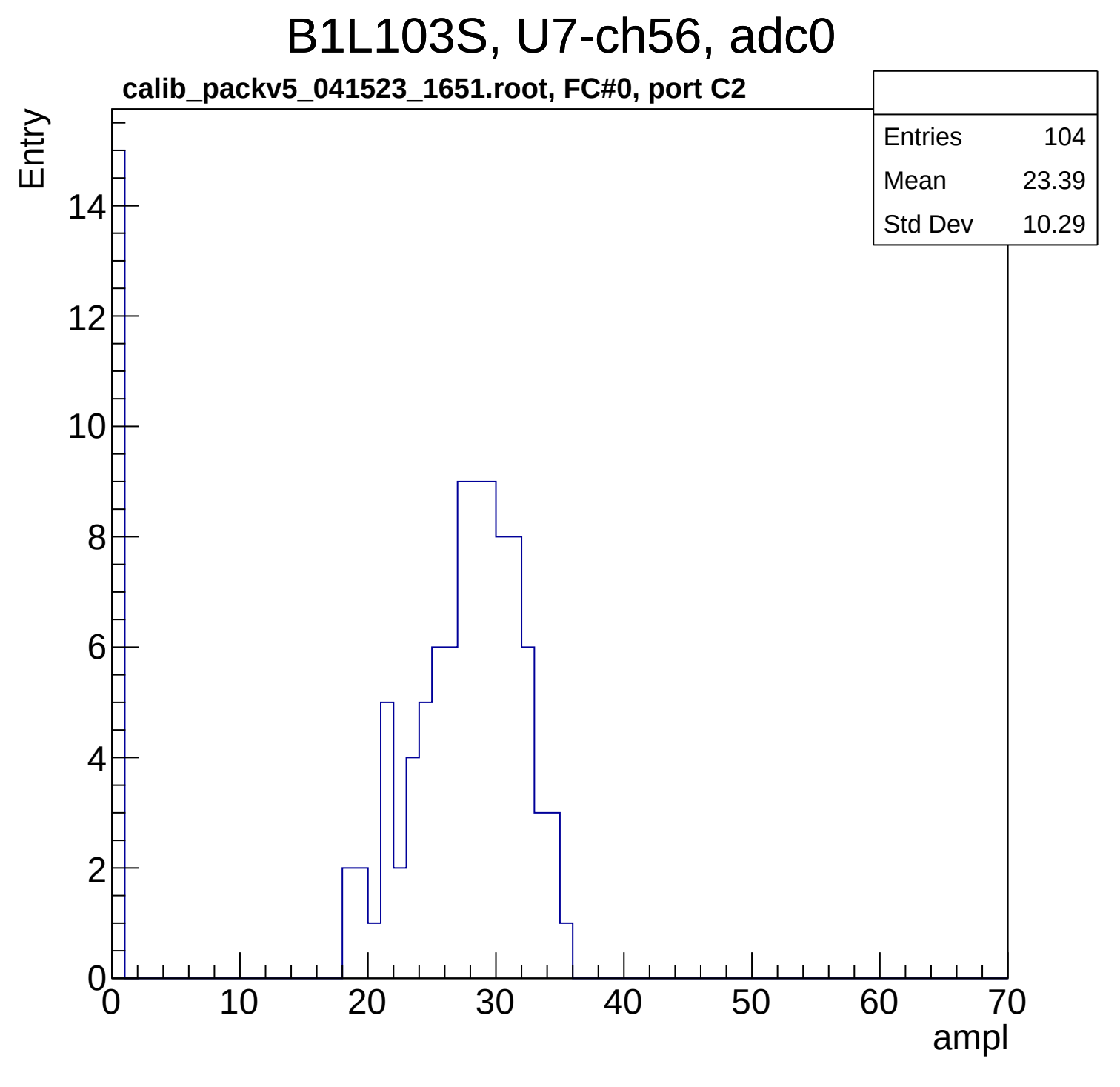
60
70
ampl


B1L103S, U7-ch56, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 104
Mean 23.39
Std Dev 10.29
Entry
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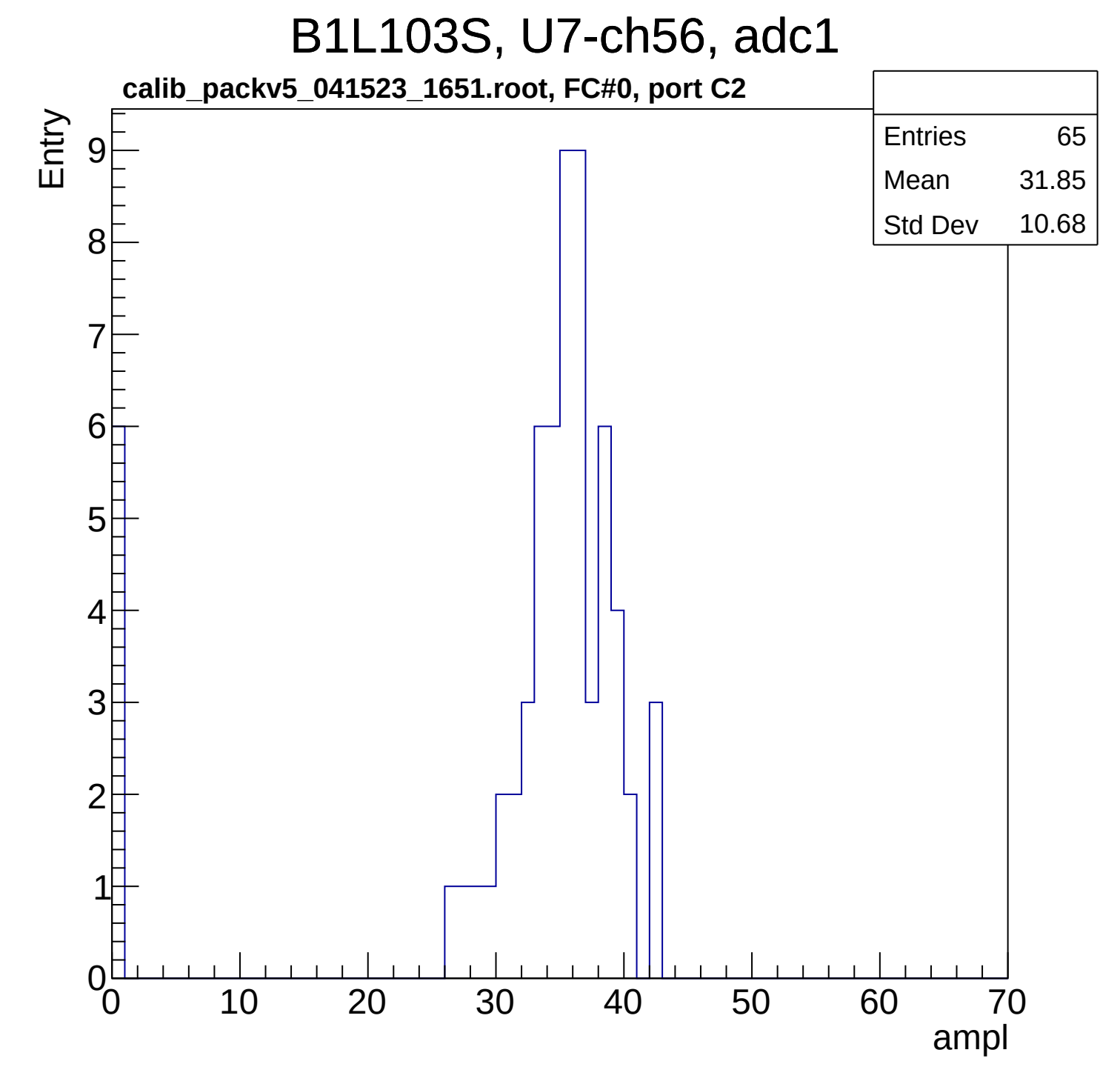
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch56, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 31.85
Std Dev 10.68
Entry
ampl
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2
3
4
5
6
7
8
9
0
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40
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60
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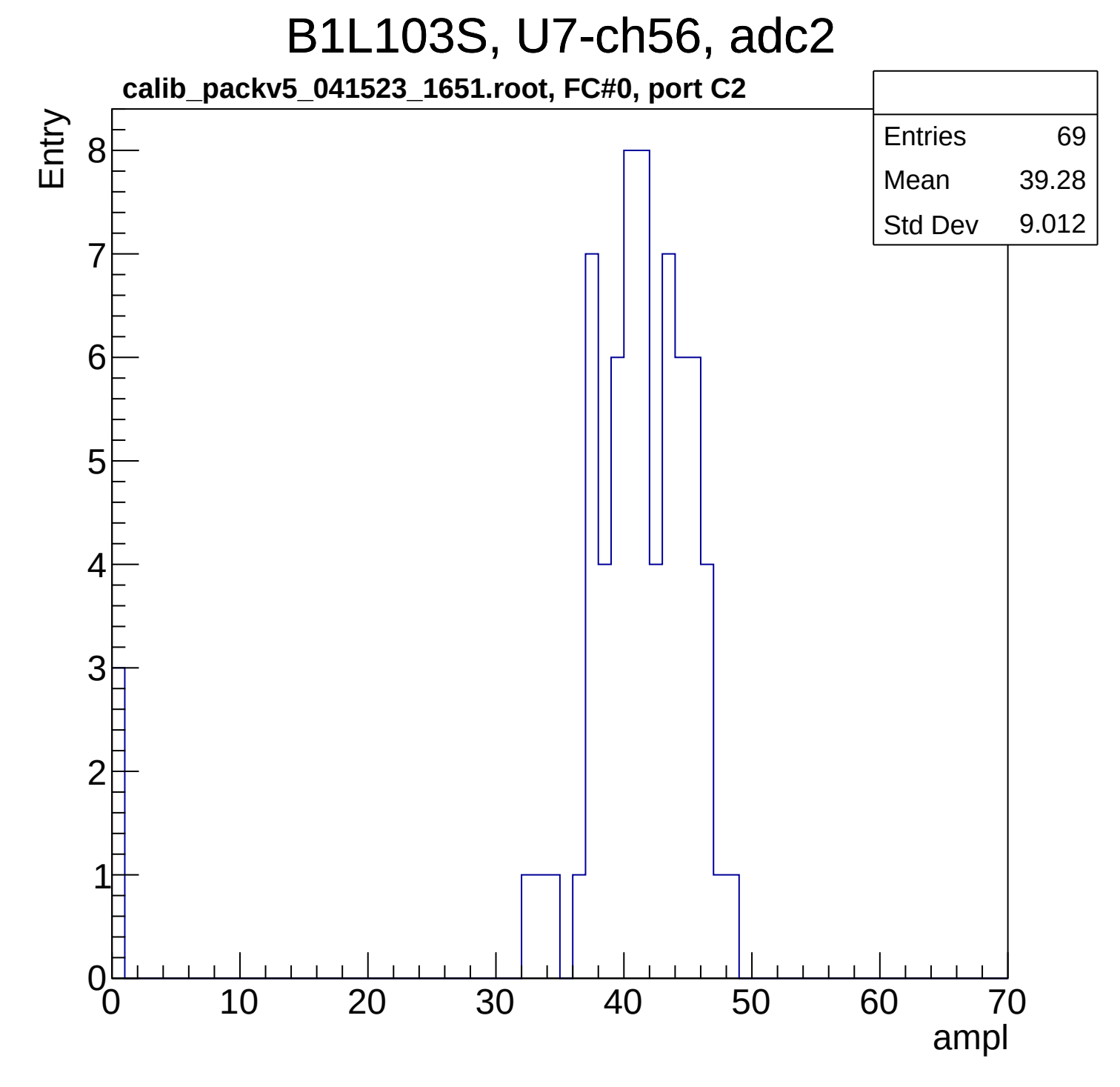
B1L103S, U7-ch56, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 39.28
Std Dev 9.012
Entry
ampl
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2
3
4
5
6
7
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0
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40
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60
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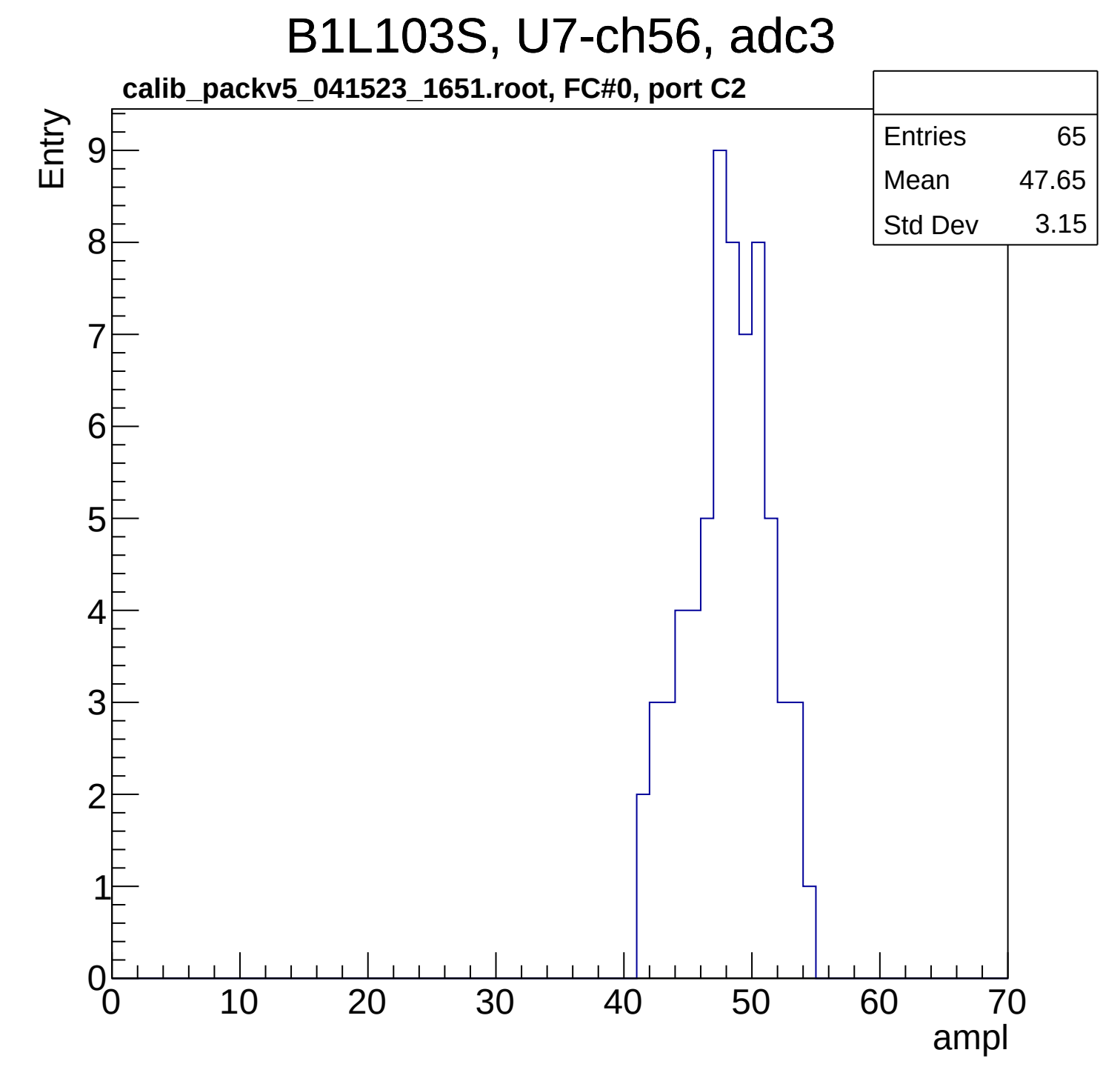
B1L103S, U7-ch56, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 47.65
Std Dev 3.15
Entry
ampl
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4
5
6
7
8
9
0
10
20
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40
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60
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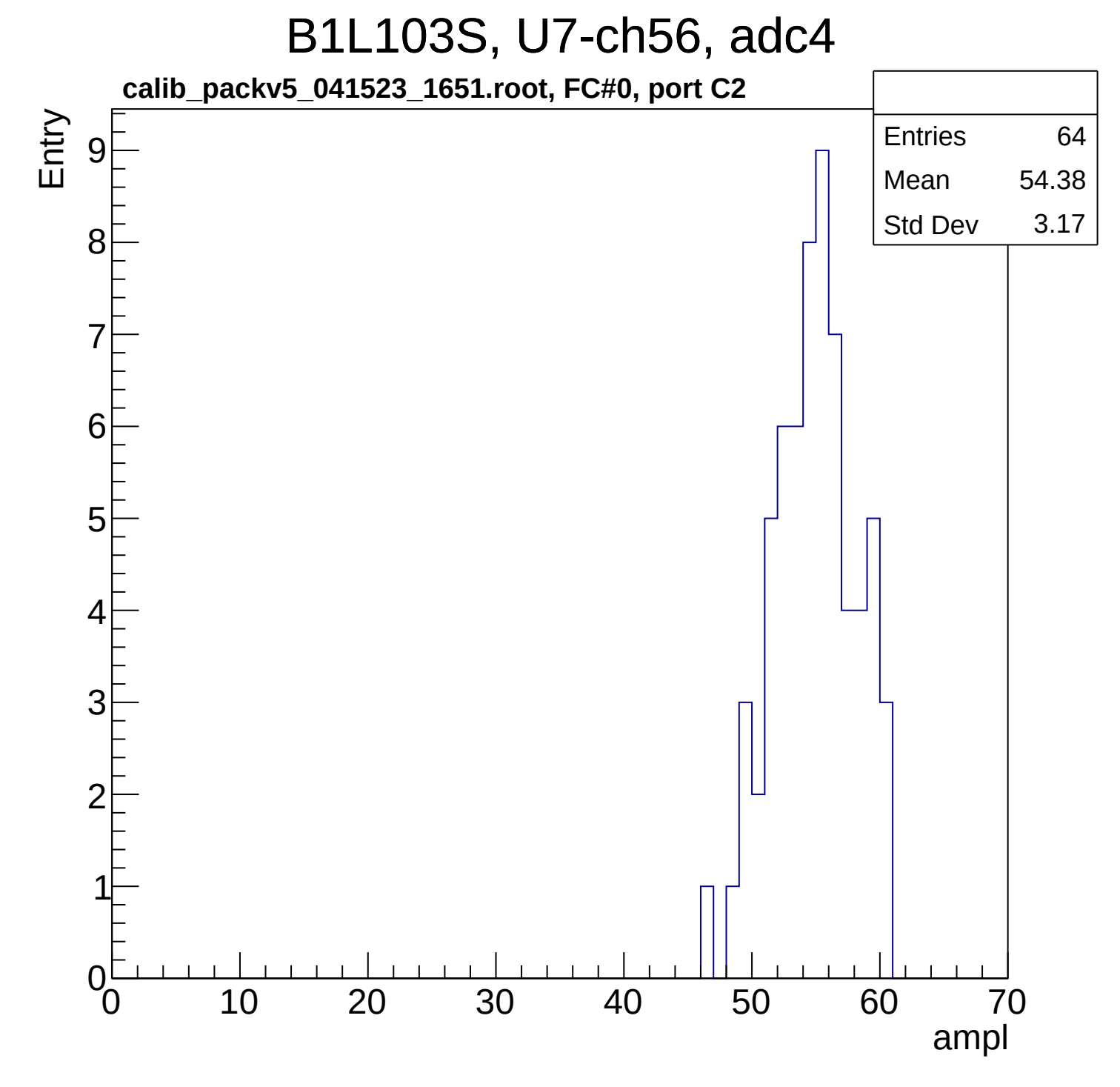
B1L103S, U7-ch56, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 54.38
Std Dev 3.17
Entry
ampl
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20
30
40
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2
3
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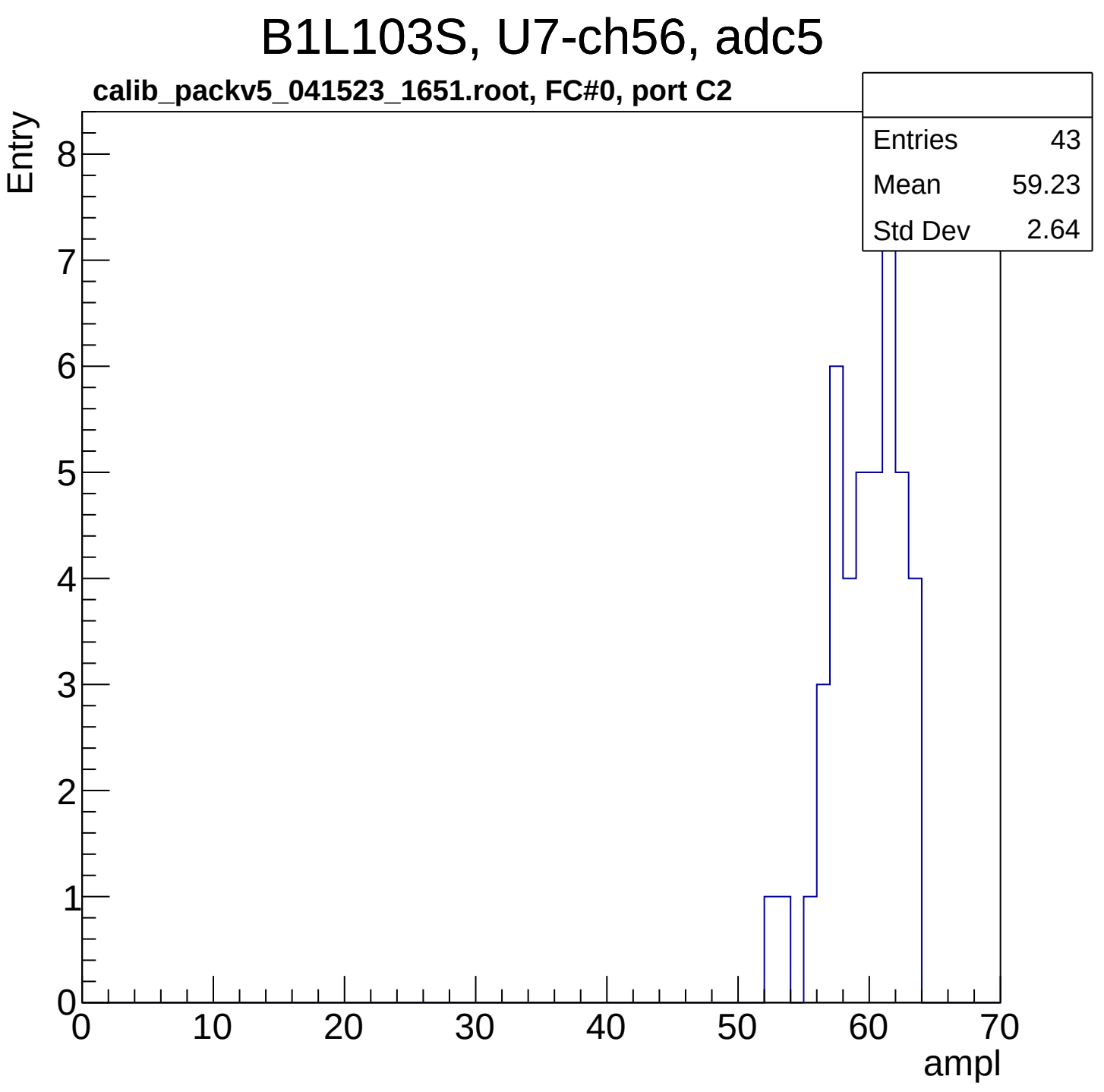
6
7
8
9


B1L103S, U7-ch56, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 43
Mean 59.23
Std Dev 2.64
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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40
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60
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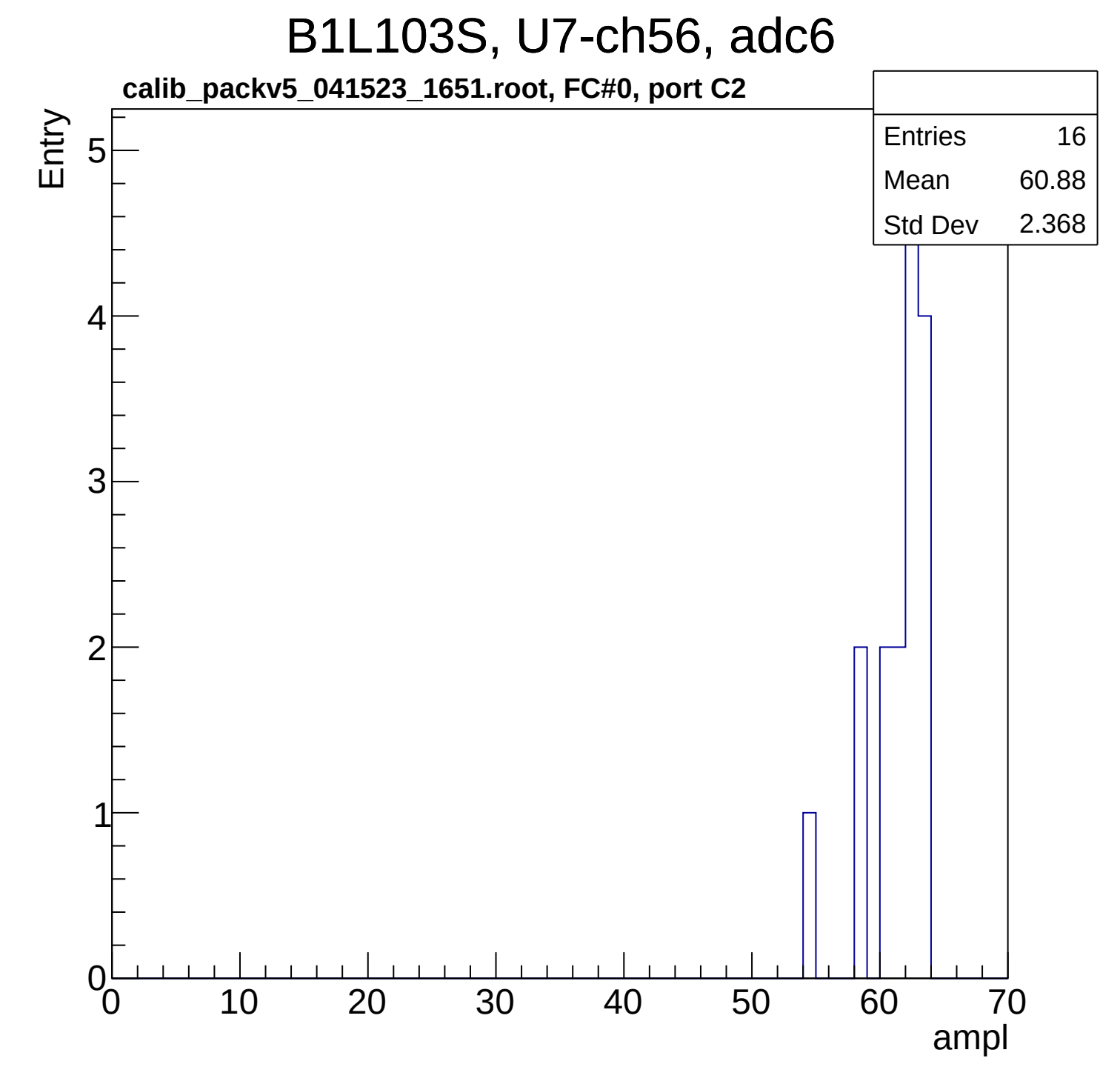
B1L103S, U7-ch56, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 16
Mean 60.88
Std Dev 2.368
Entry
ampl
0
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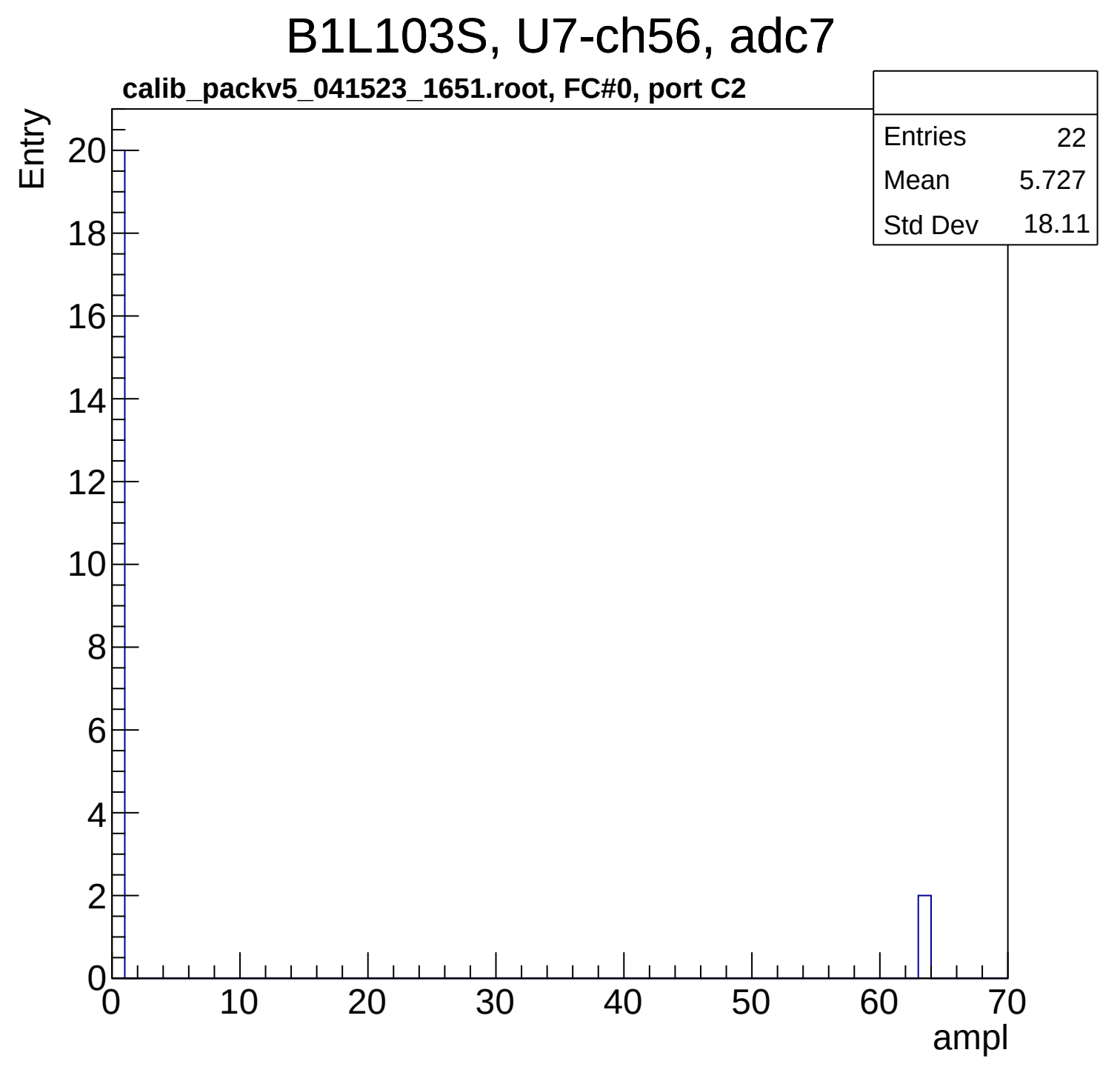
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U7-ch56, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 5.727
Std Dev 18.11
Entry
ampl
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6
8
10
12
14
16
18
20
0
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20
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40
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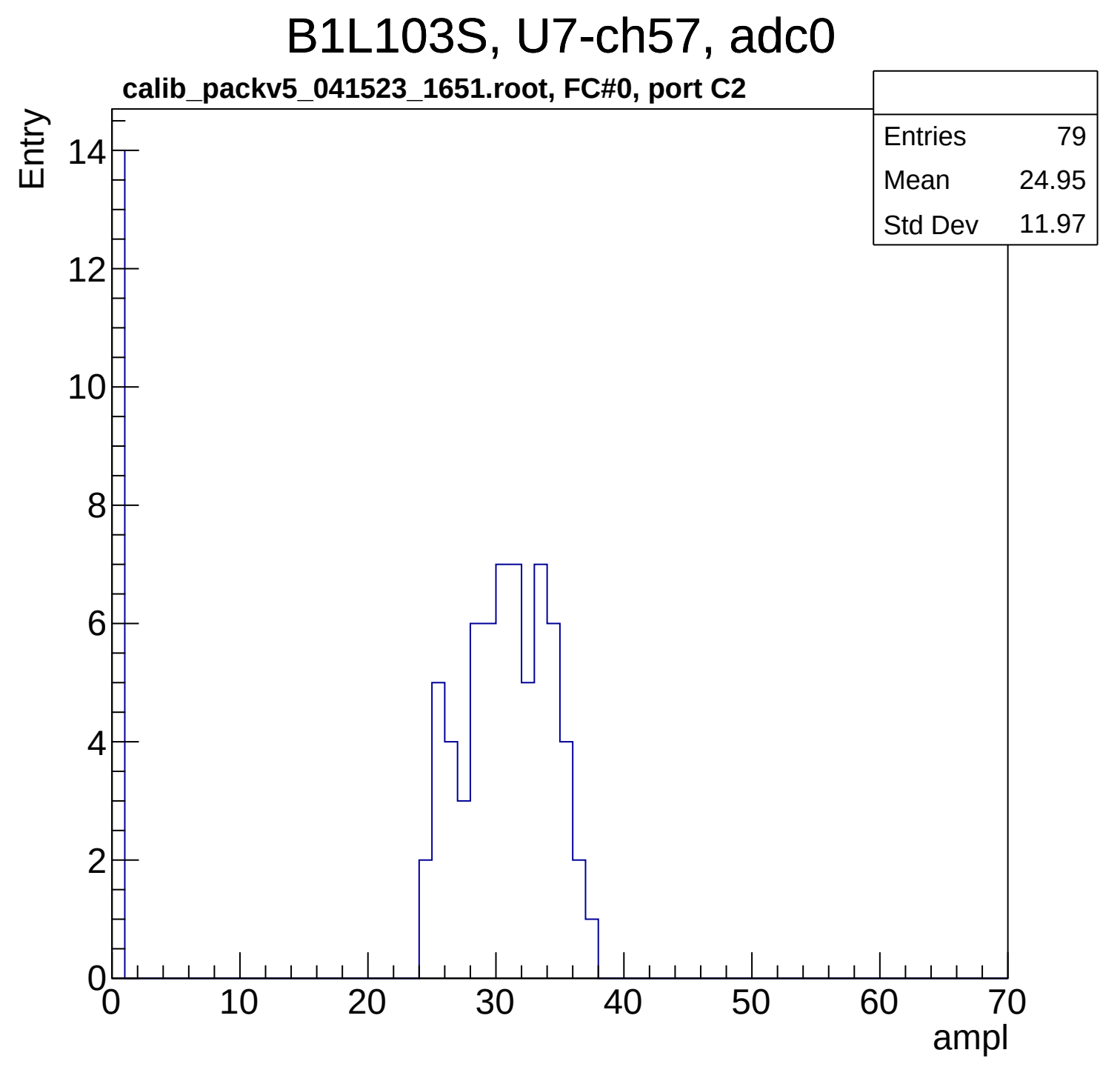
B1L103S, U7-ch57, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 24.95
Std Dev 11.97
Entry
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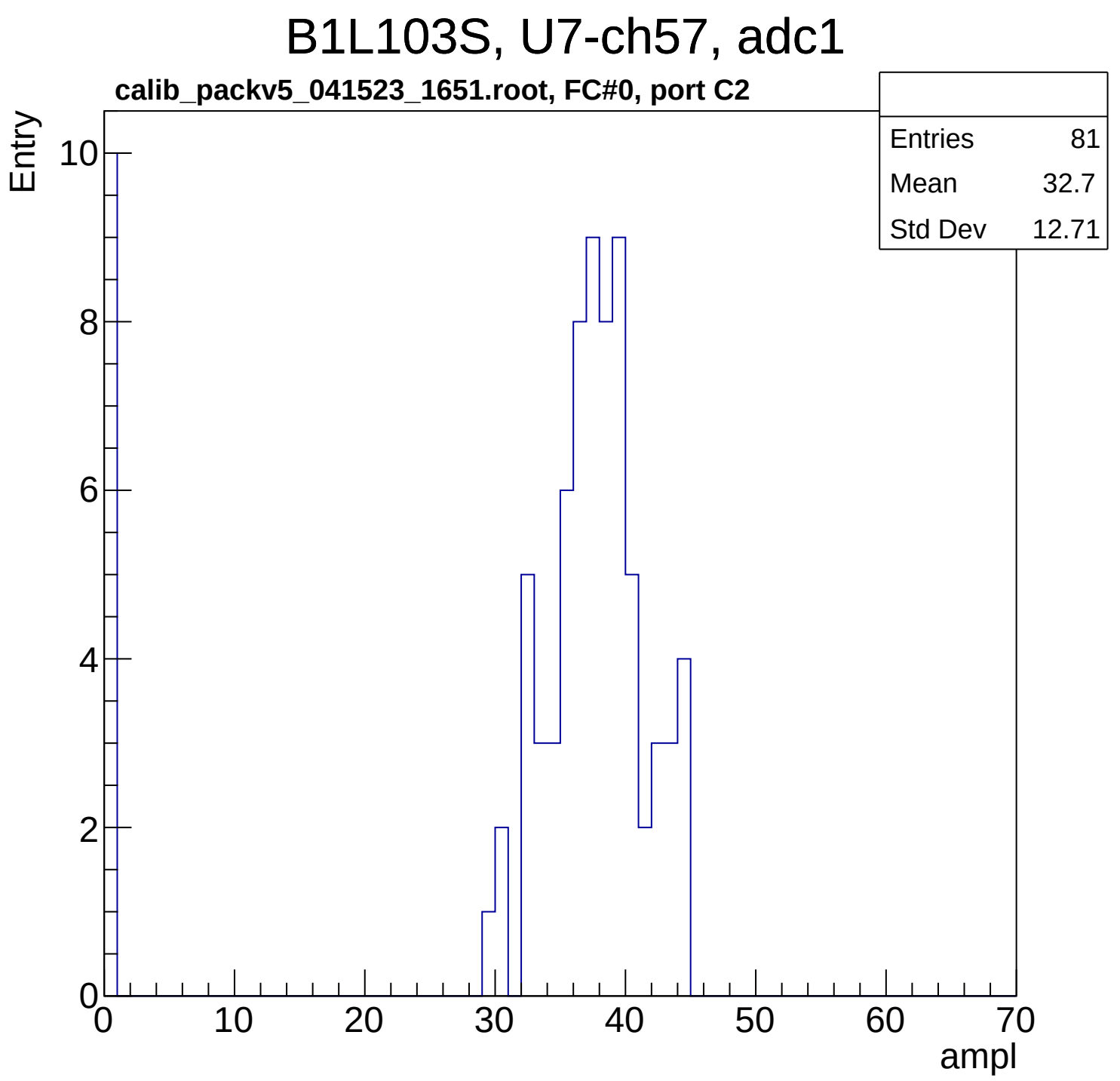
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch57, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 32.7
Std Dev 12.71
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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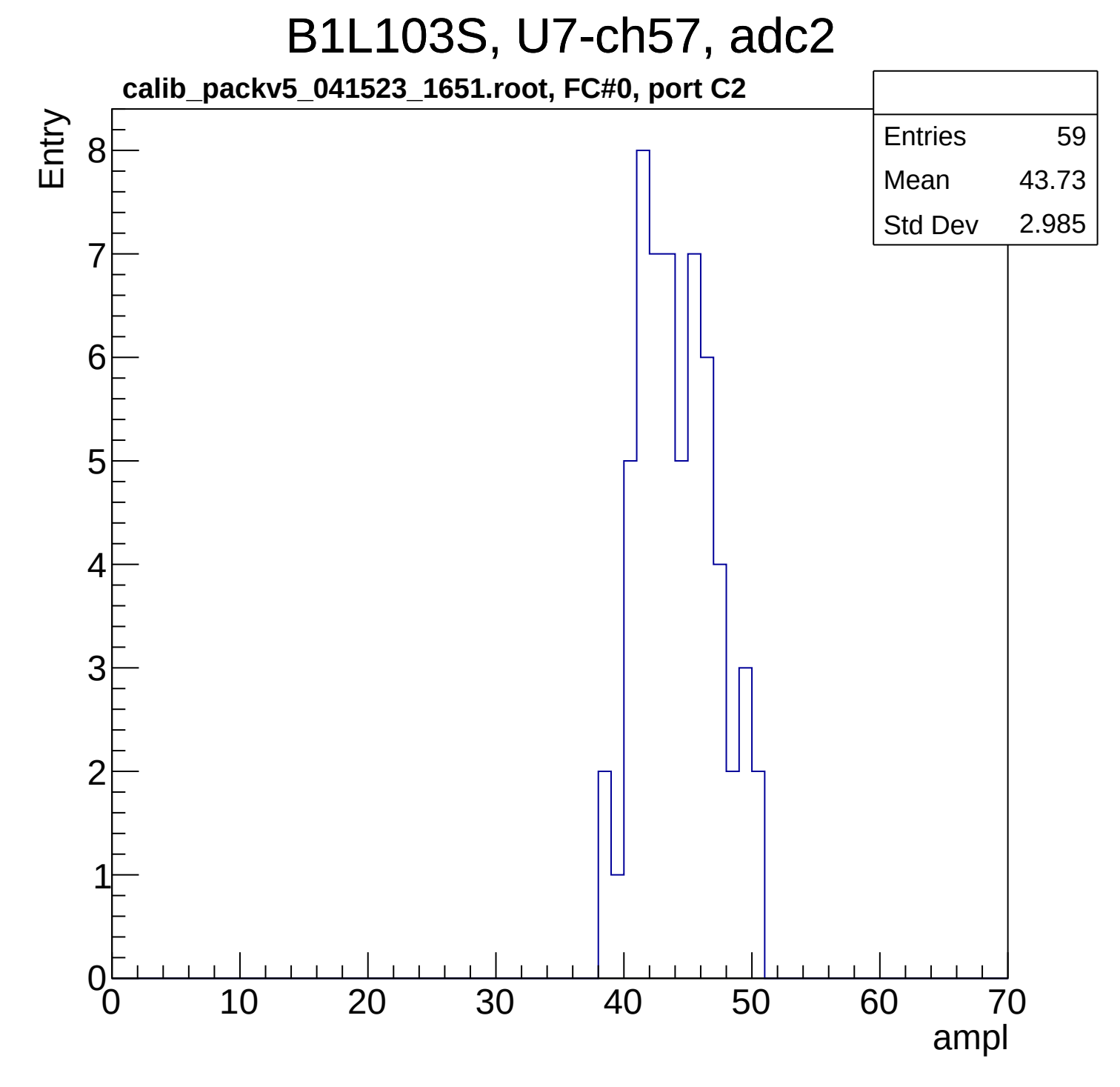
B1L103S, U7-ch57, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 43.73
Std Dev 2.985
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
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60
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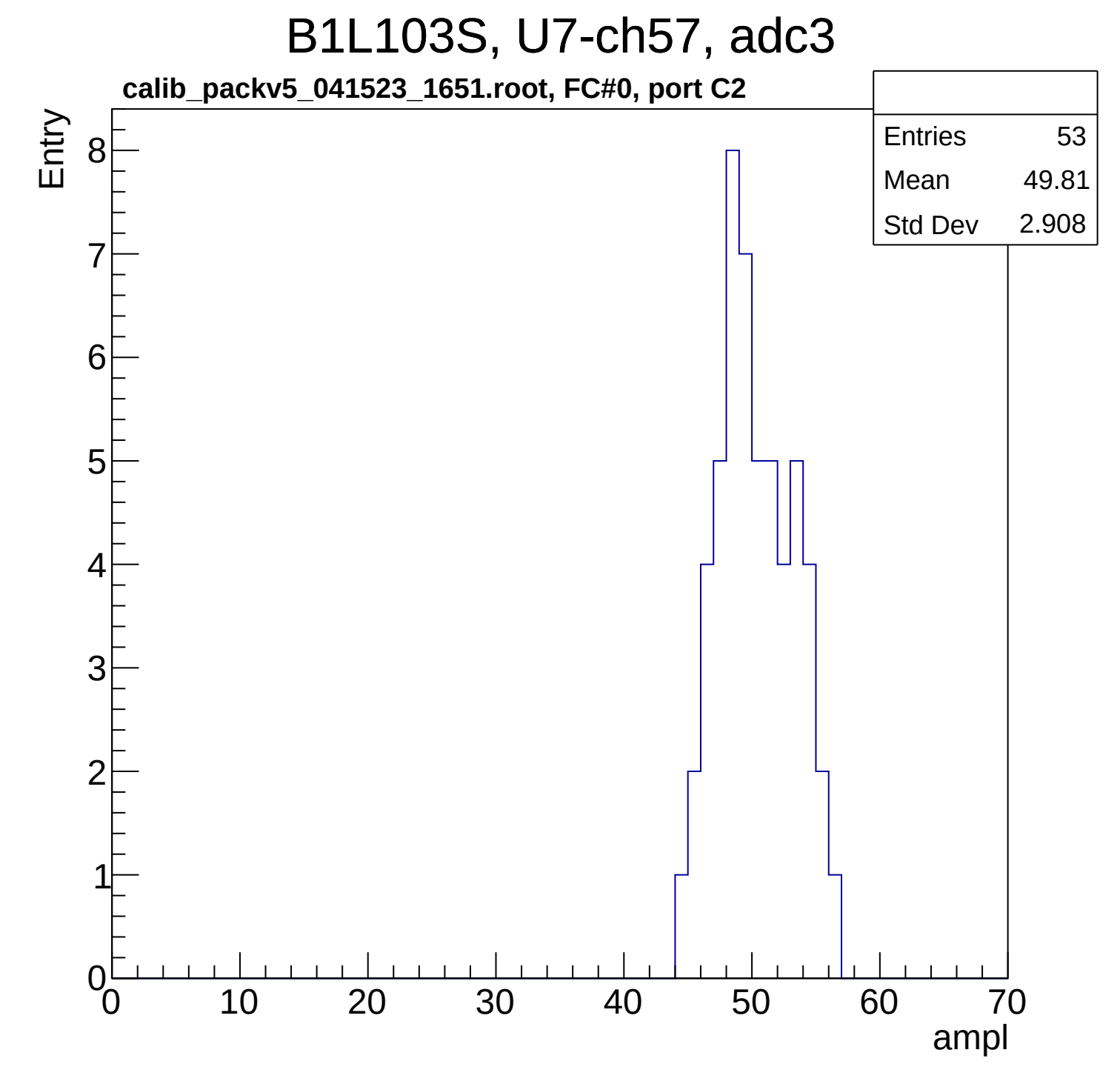
B1L103S, U7-ch57, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 49.81
Std Dev 2.908
Entry
ampl
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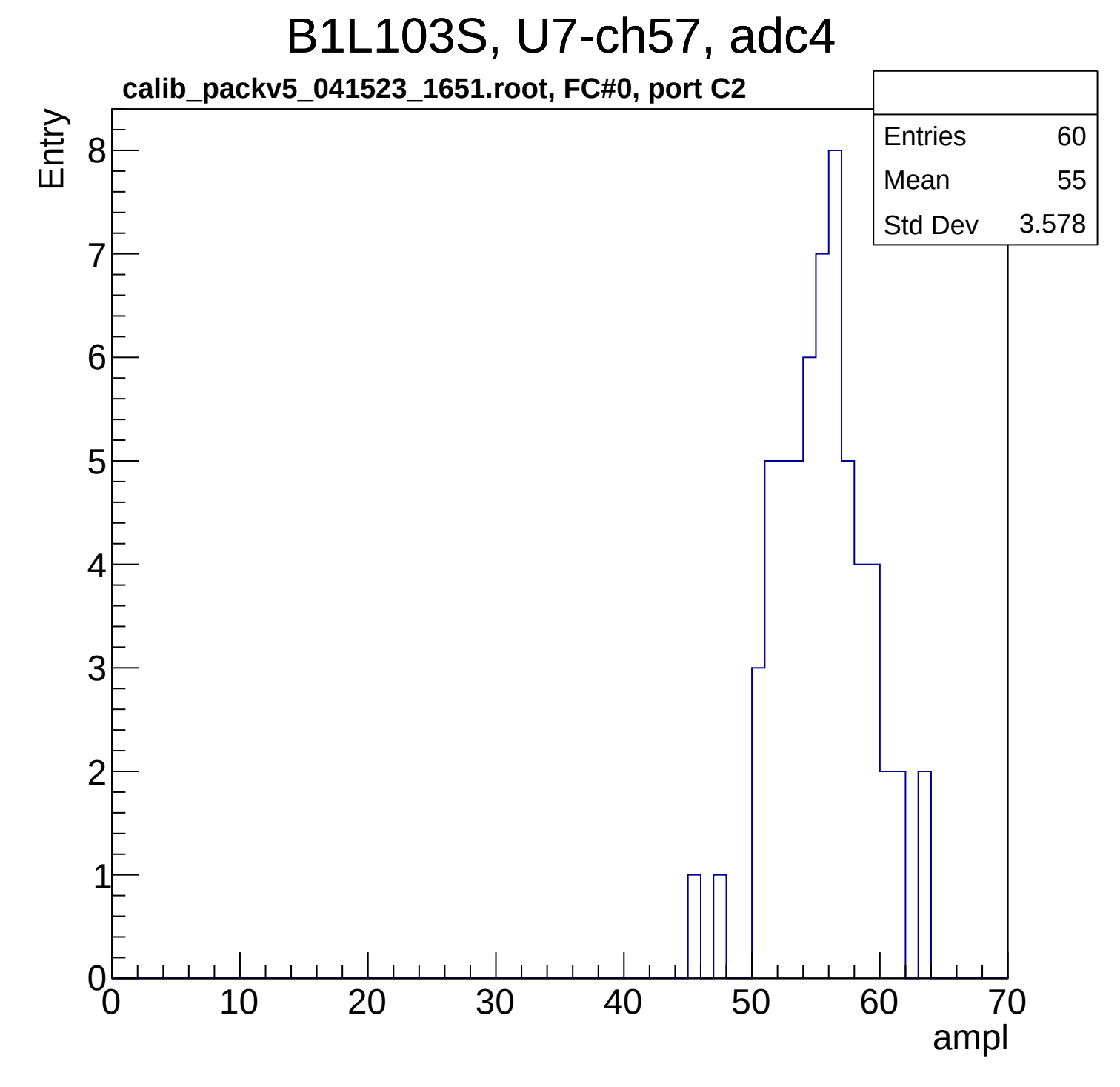
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch57, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 55
Std Dev 3.578
Entry
ampl
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3
4
5
6
7
8
0
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20
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40
50
60
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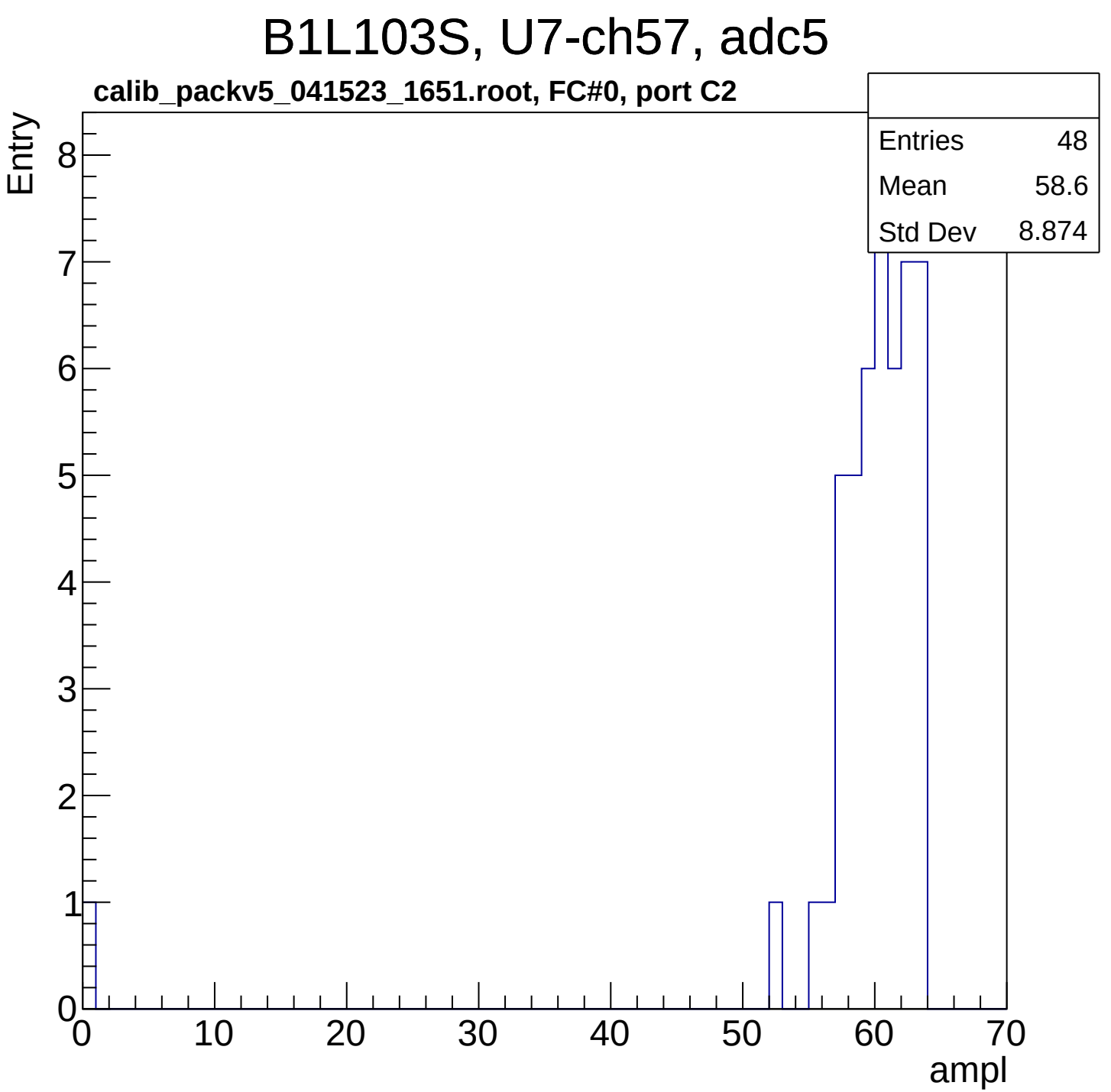
B1L103S, U7-ch57, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 58.6
Std Dev 8.874
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
30
40
50
60
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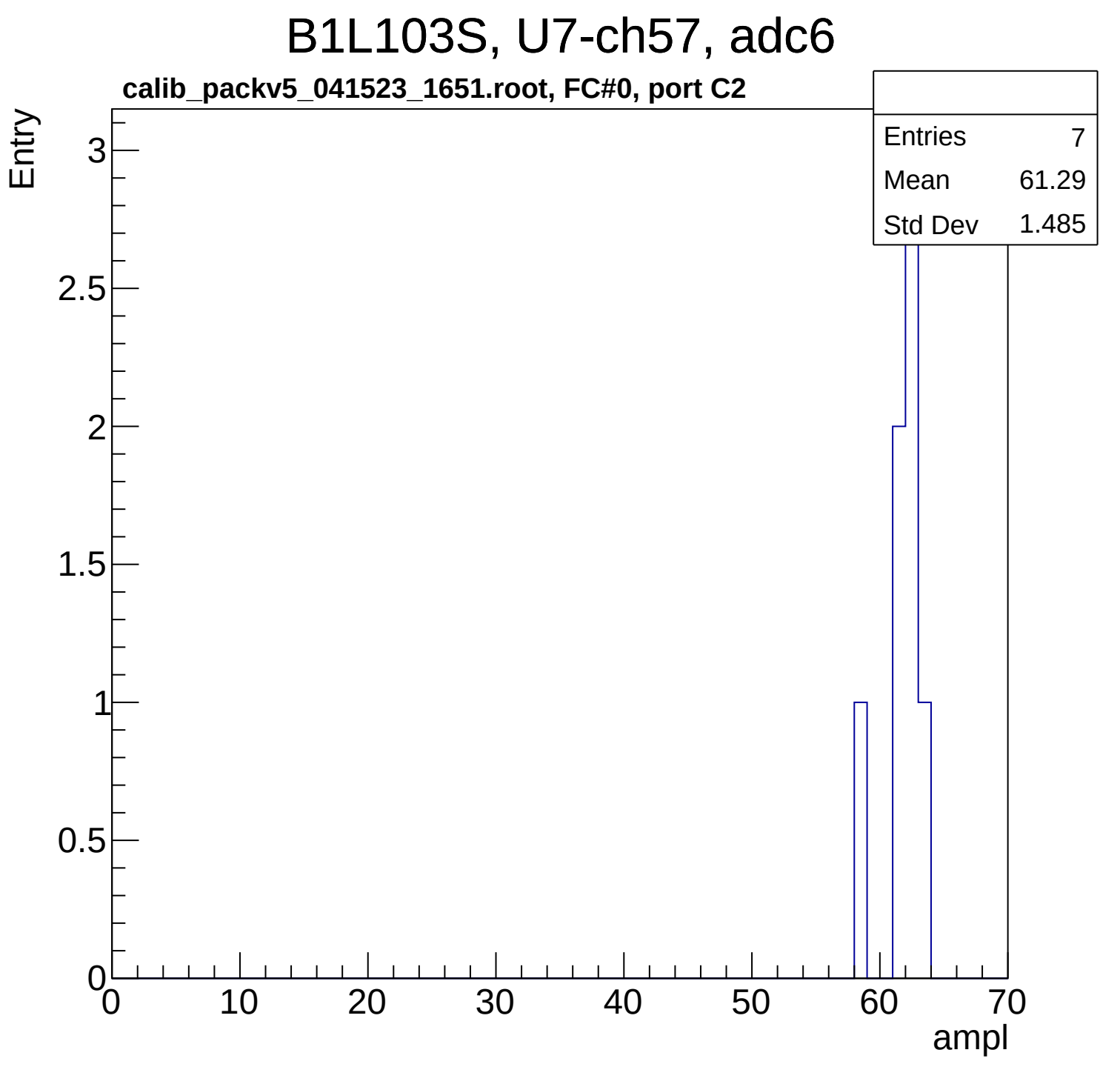
B1L103S, U7-ch57, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 61.29
Std Dev 1.485
Entry
ampl
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1
1.5
2
2.5
3
0
10
20
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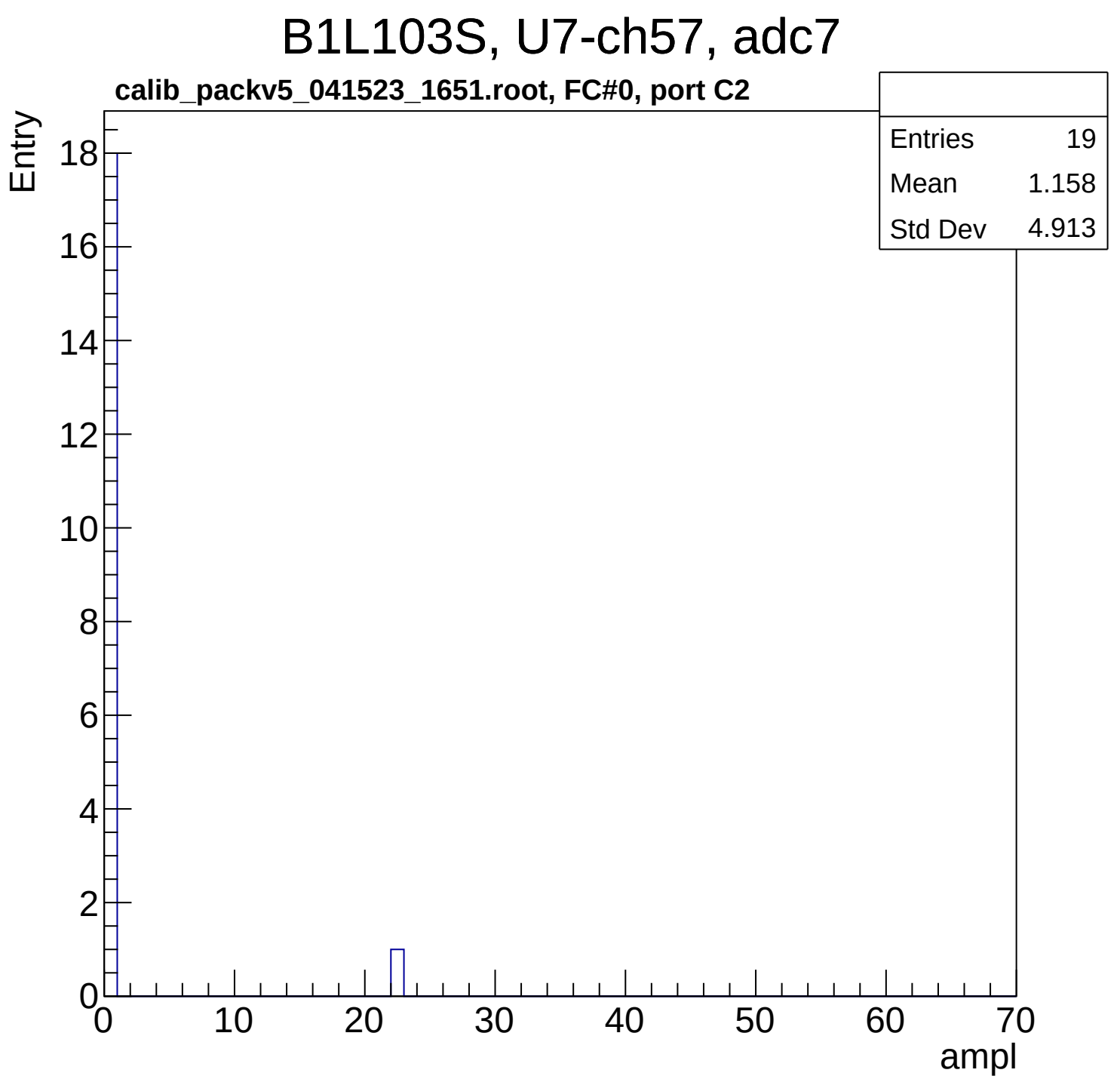
40
50
60
70


B1L103S, U7-ch57, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.158
Std Dev 4.913
Entry
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6
8
10
12
14
16
18
0
10
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30
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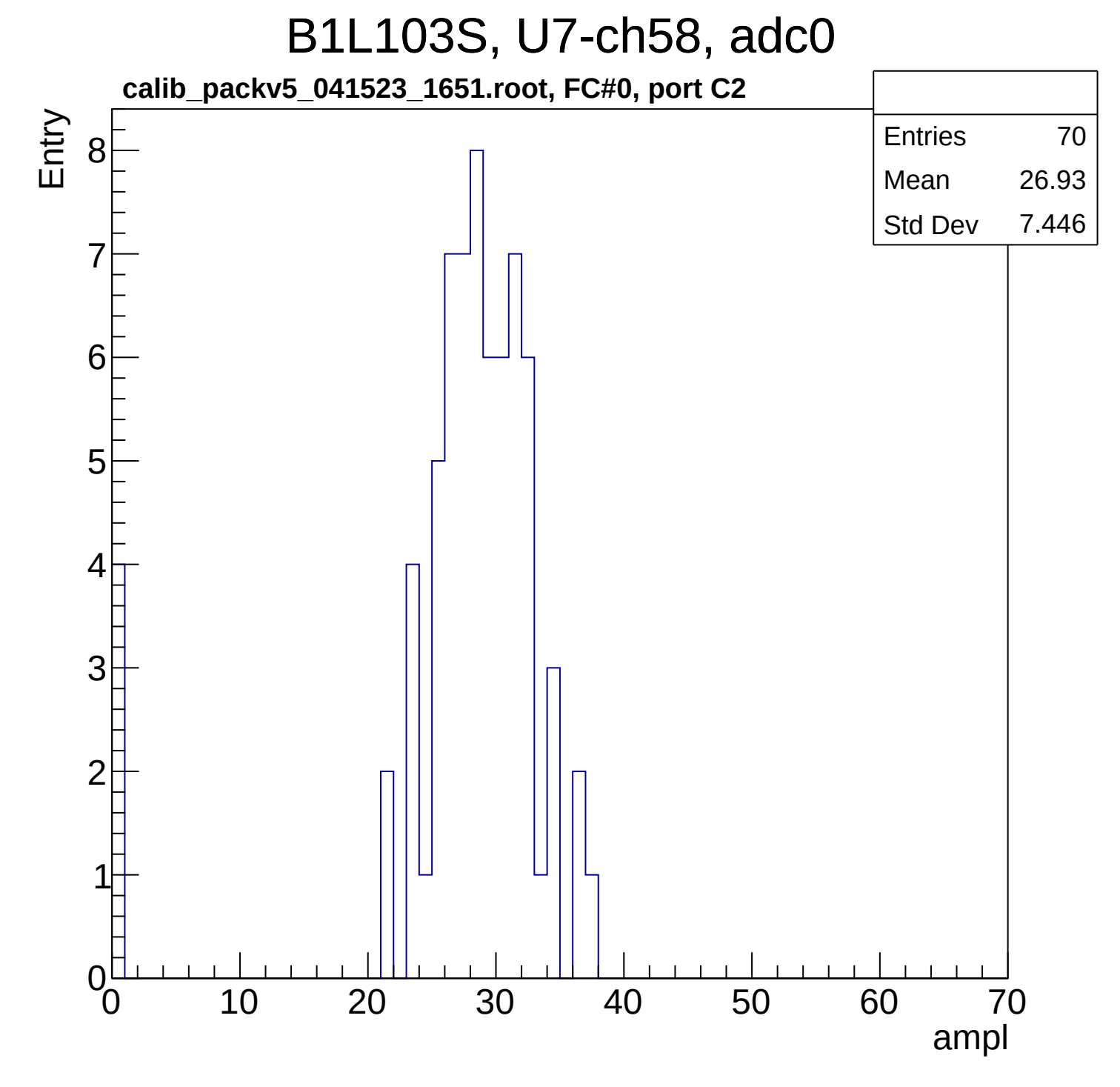
50
60
70
ampl


B1L103S, U7-ch58, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 26.93
Std Dev 7.446
Entry
ampl
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3
4
5
6
7
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0
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20
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40
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60
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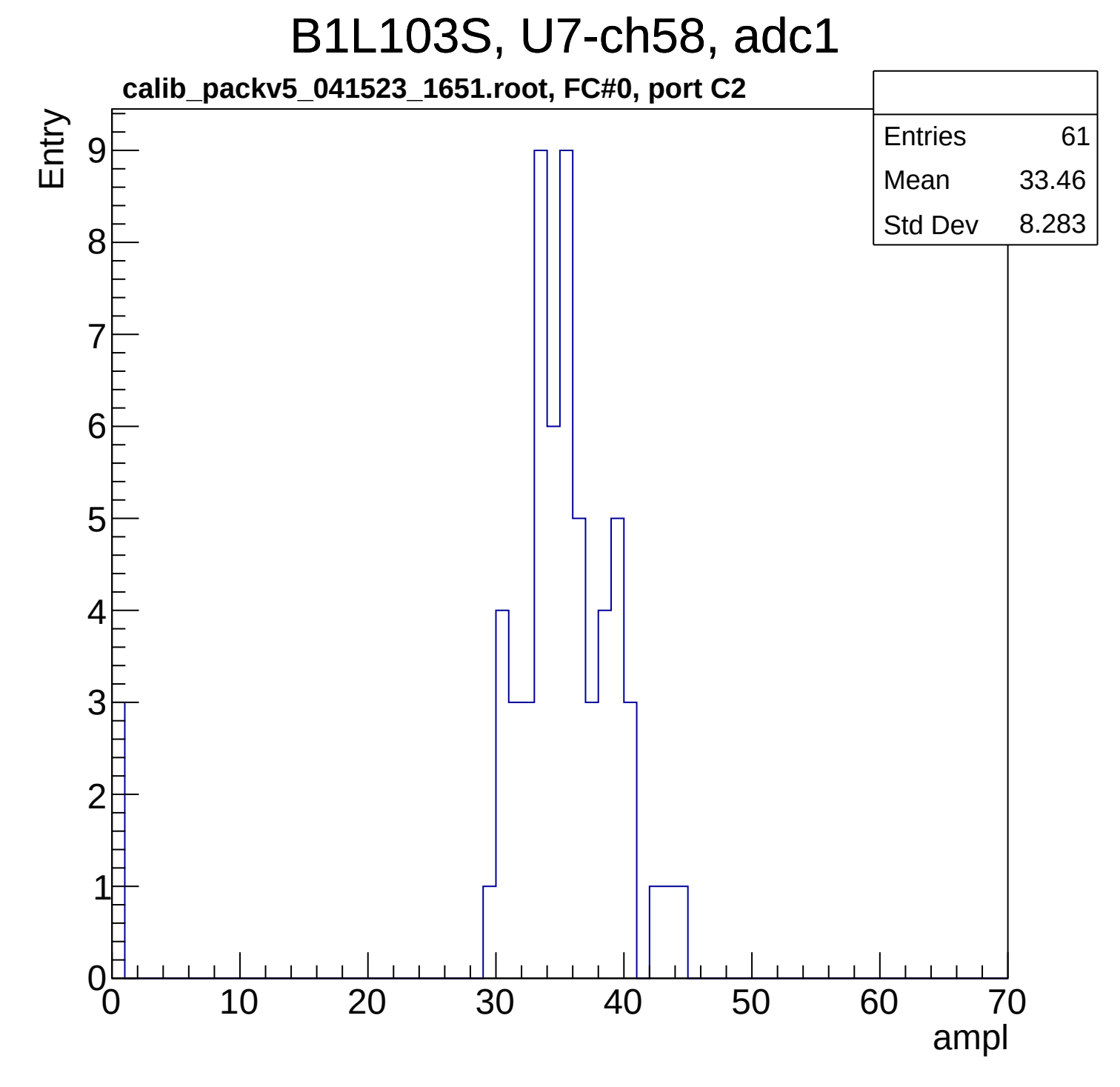
B1L103S, U7-ch58, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 33.46
Std Dev 8.283
Entry
ampl
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6
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9
0
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20
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60
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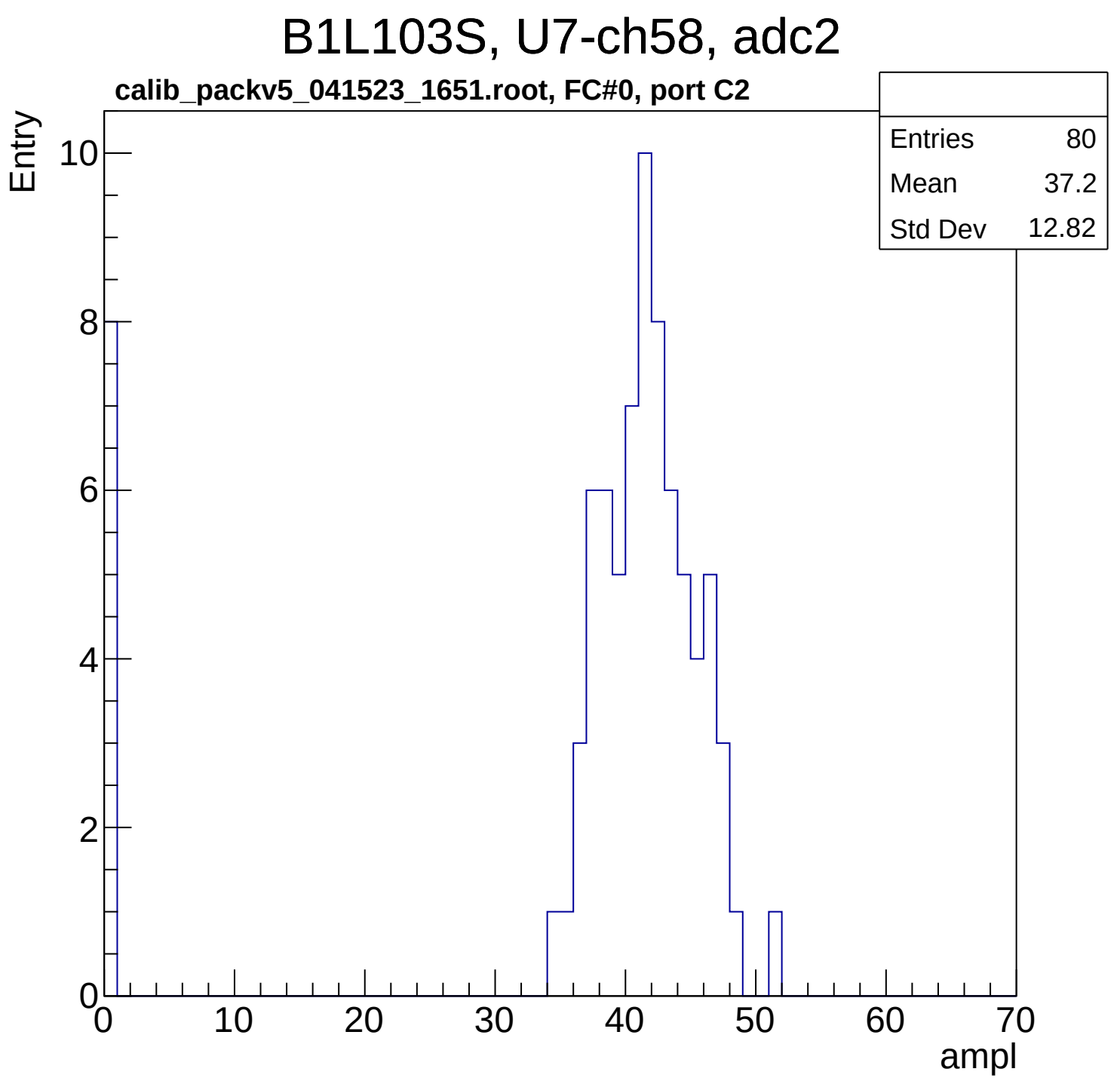
B1L103S, U7-ch58, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 37.2
Std Dev 12.82
Entry
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10
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30
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50
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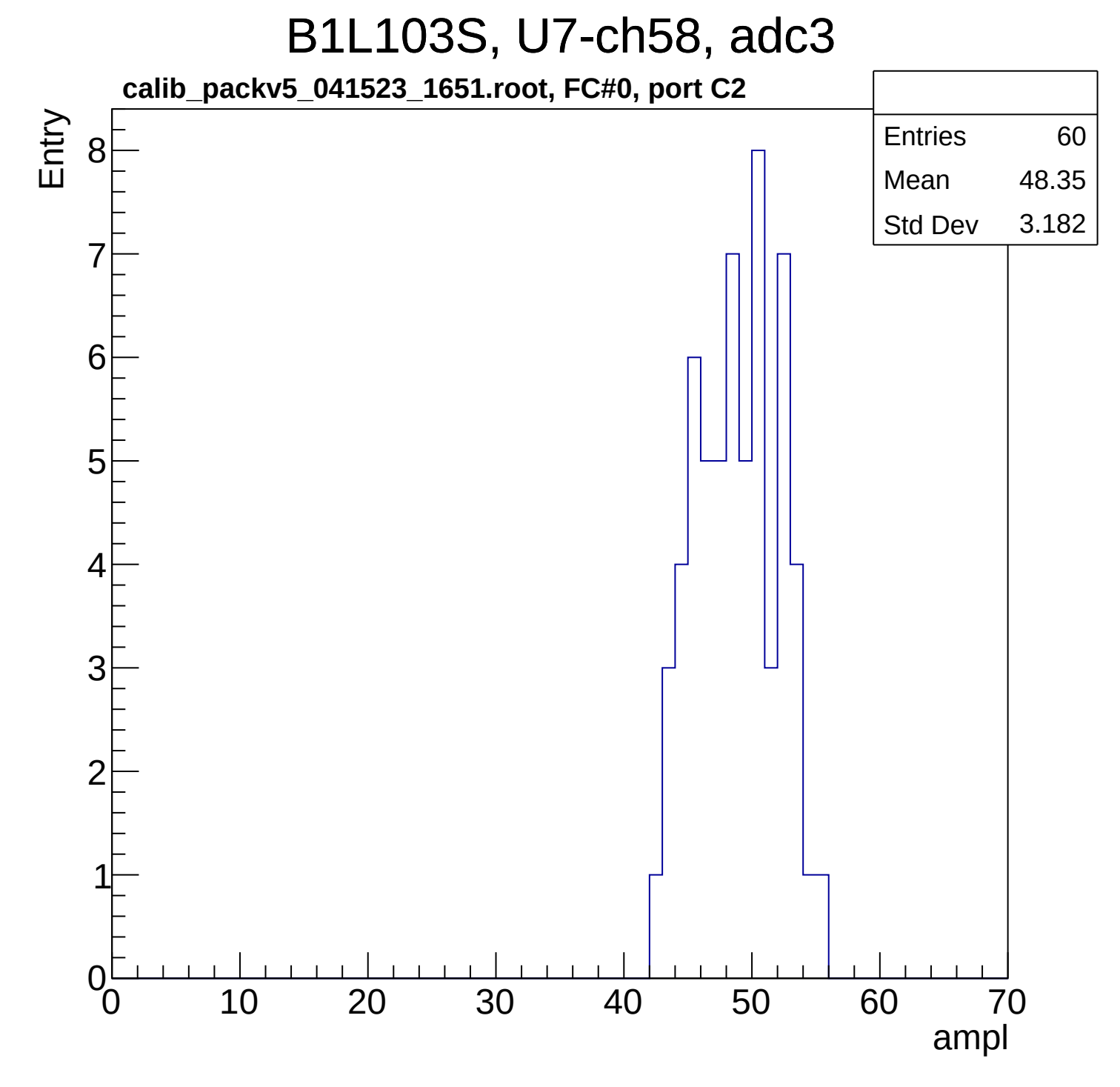
70
ampl


B1L103S, U7-ch58, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 48.35
Std Dev 3.182
Entry
ampl
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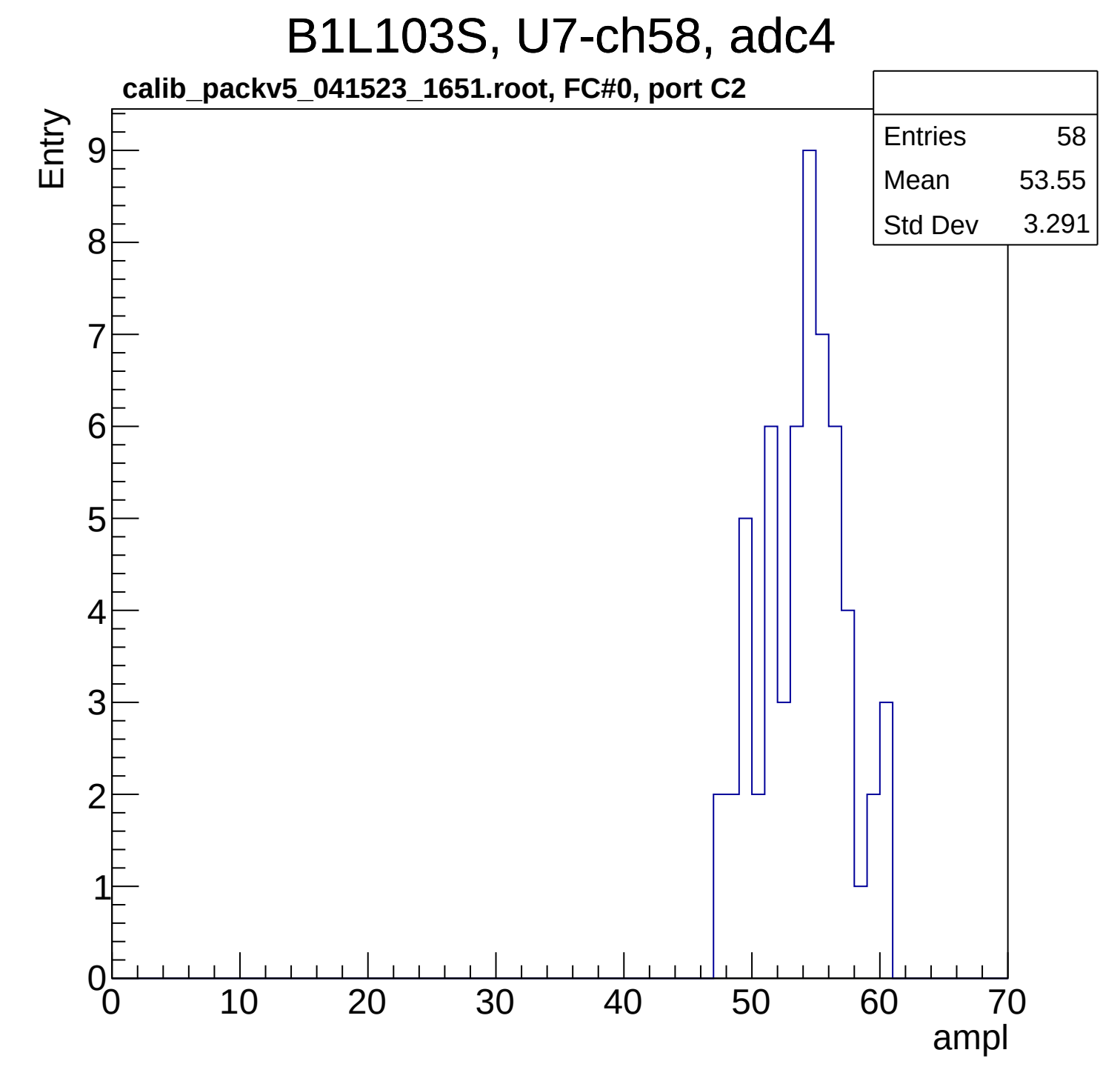
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch58, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 53.55
Std Dev 3.291
Entry
ampl
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3
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5
6
7
8
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0
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60
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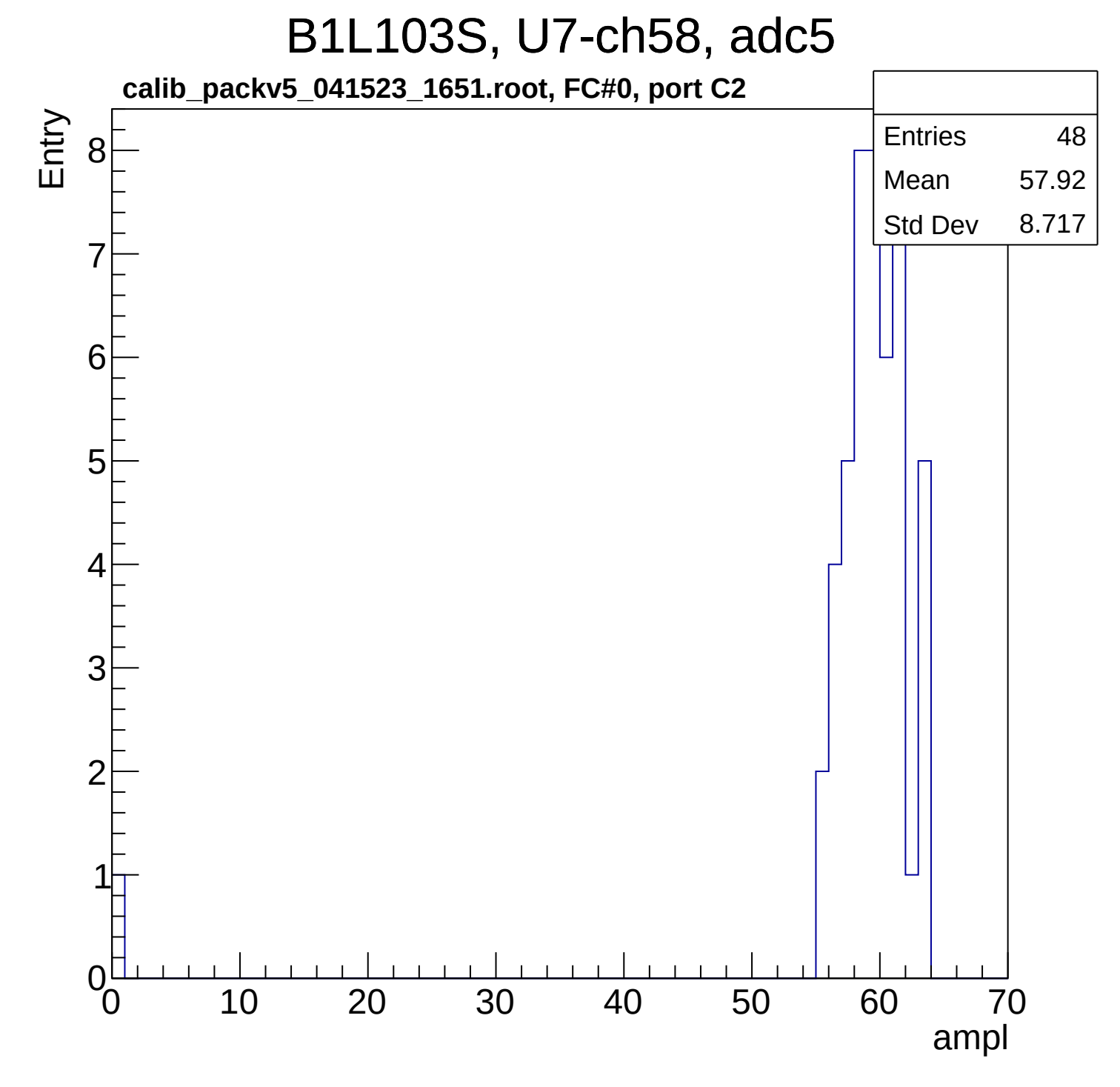
B1L103S, U7-ch58, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 57.92
Std Dev 8.717
Entry
ampl
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2
3
4
5
6
7
8
0
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60
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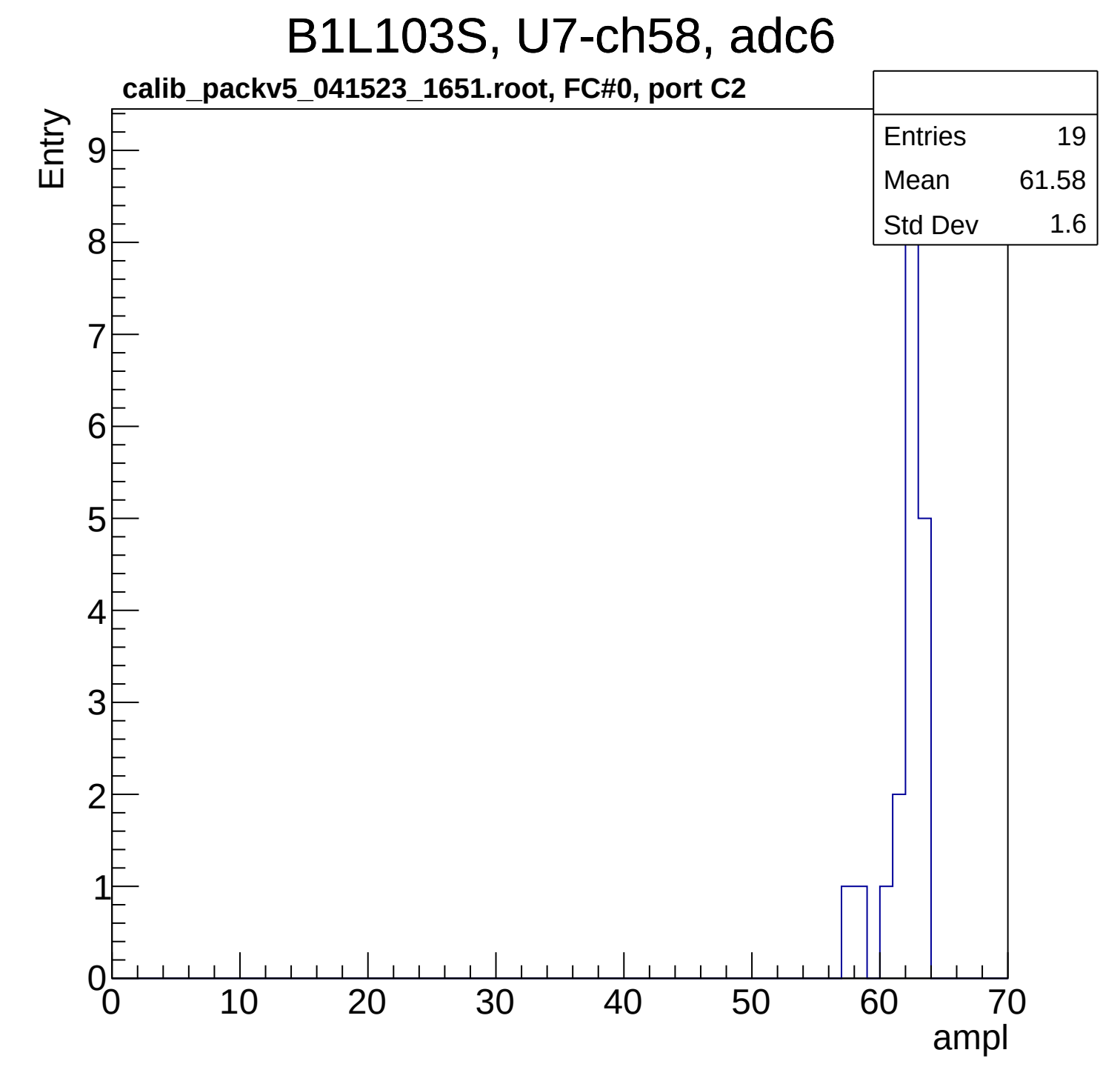
B1L103S, U7-ch58, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 61.58
Std Dev 1.6
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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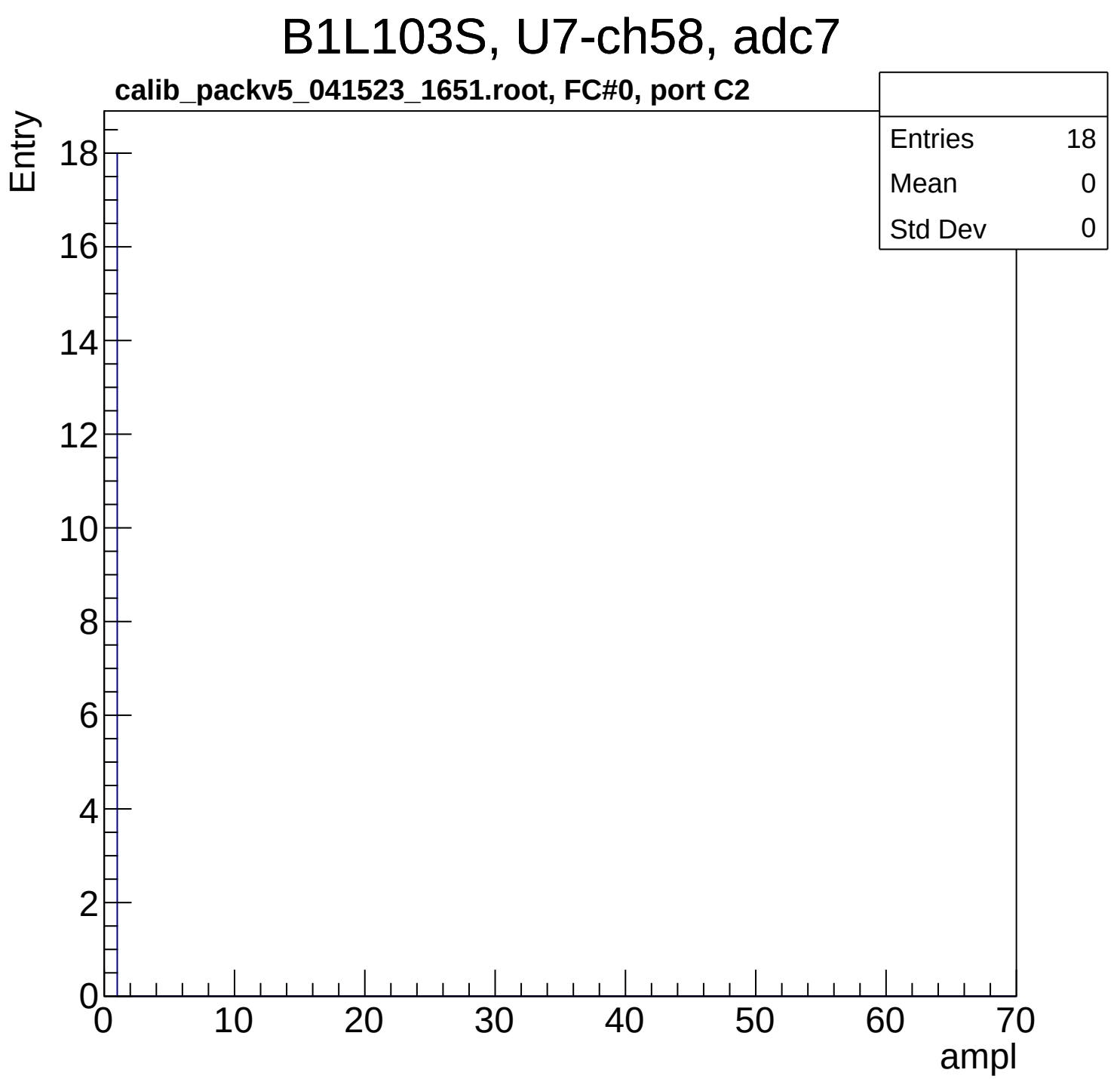
60
70


B1L103S, U7-ch58, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
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8
10
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14
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0
10
20
30
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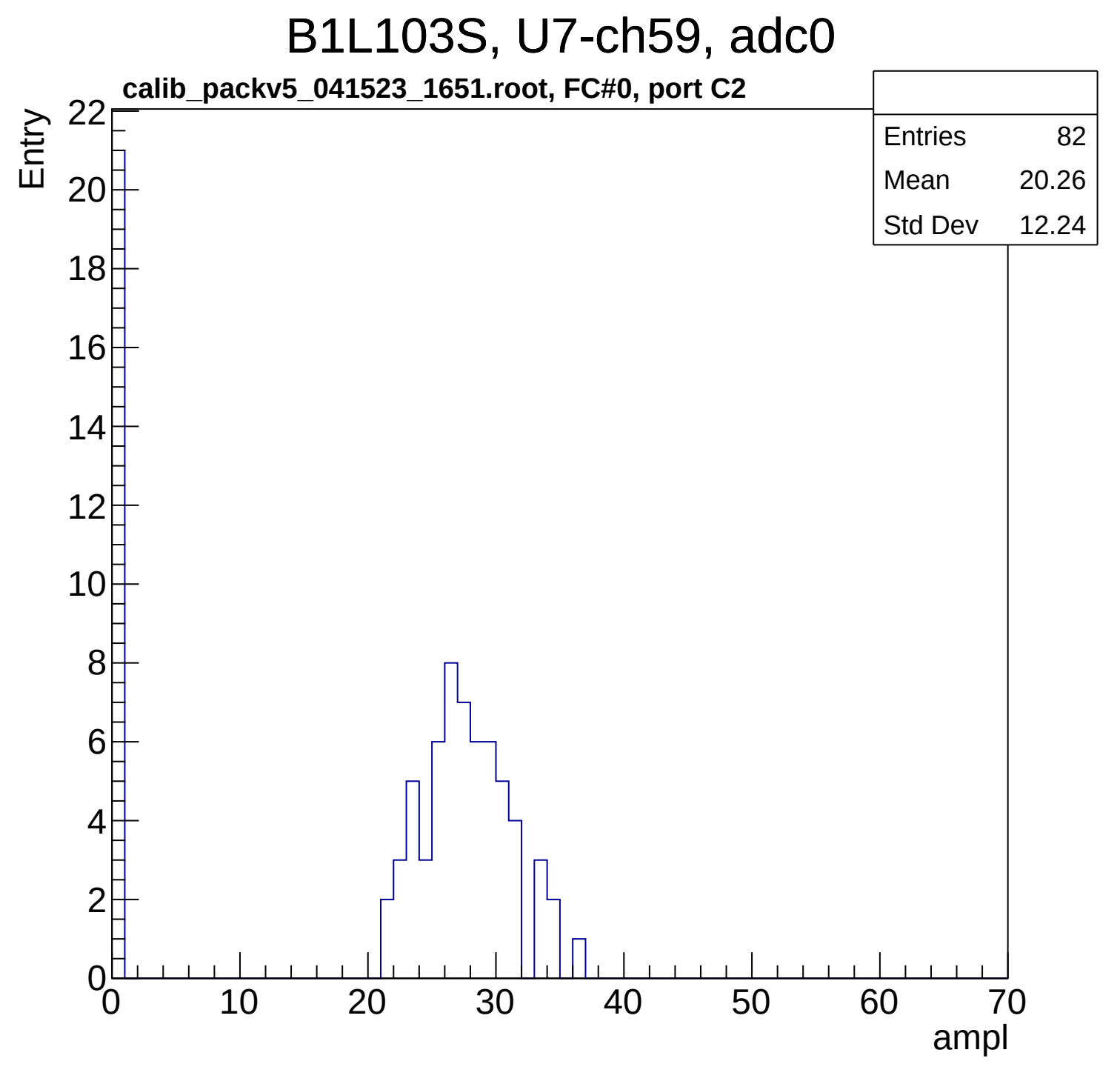
50
60
70
ampl


B1L103S, U7-ch59, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 20.26
Std Dev 12.24
Entry
ampl
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8
10
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14
16
18
20
22
0
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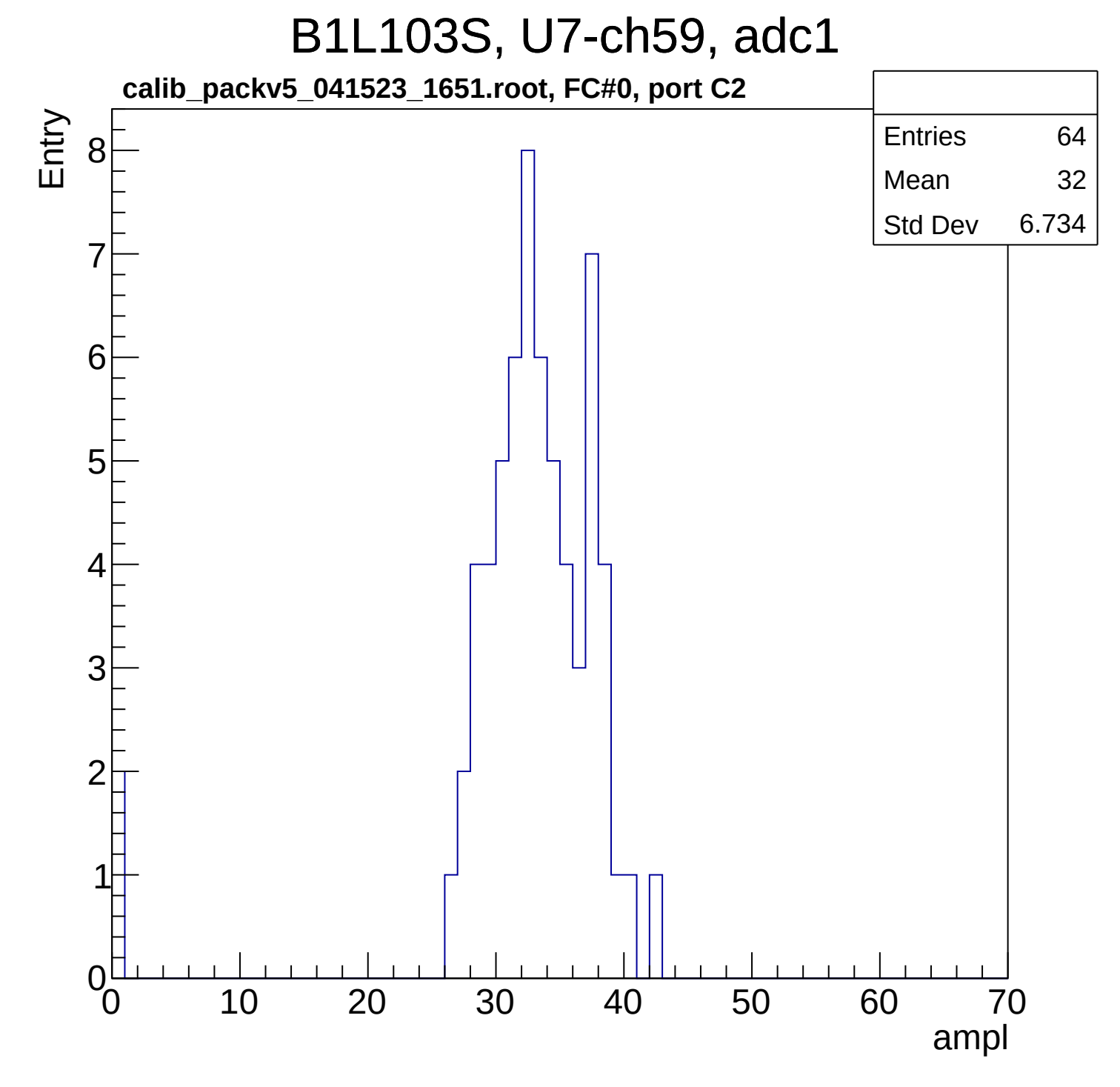
B1L103S, U7-ch59, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 32
Std Dev 6.734
Entry
ampl
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1
2
3
4
5
6
7
8
0
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40
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60
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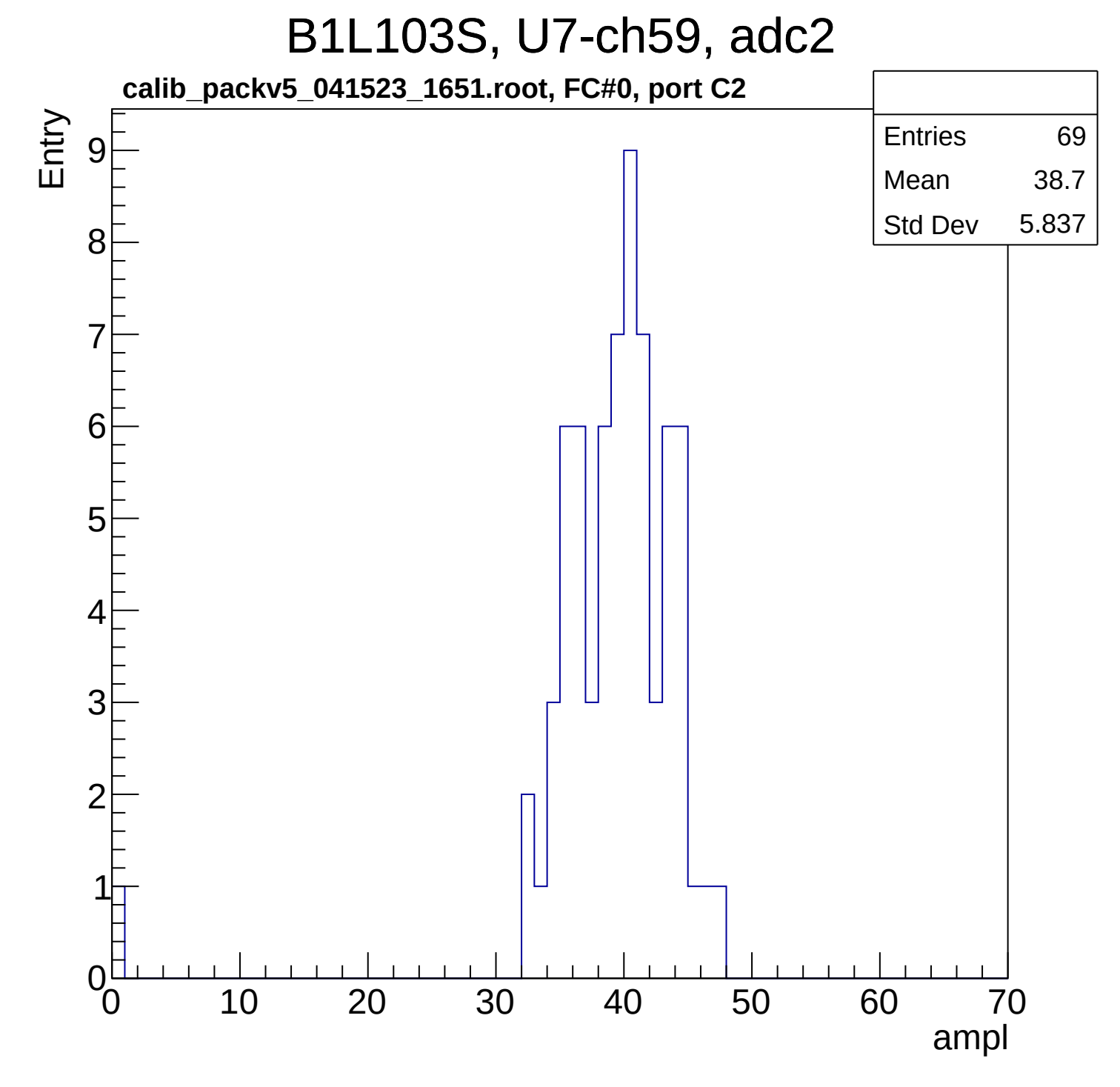
B1L103S, U7-ch59, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 38.7
Std Dev 5.837
Entry
ampl
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3
4
5
6
7
8
9
0
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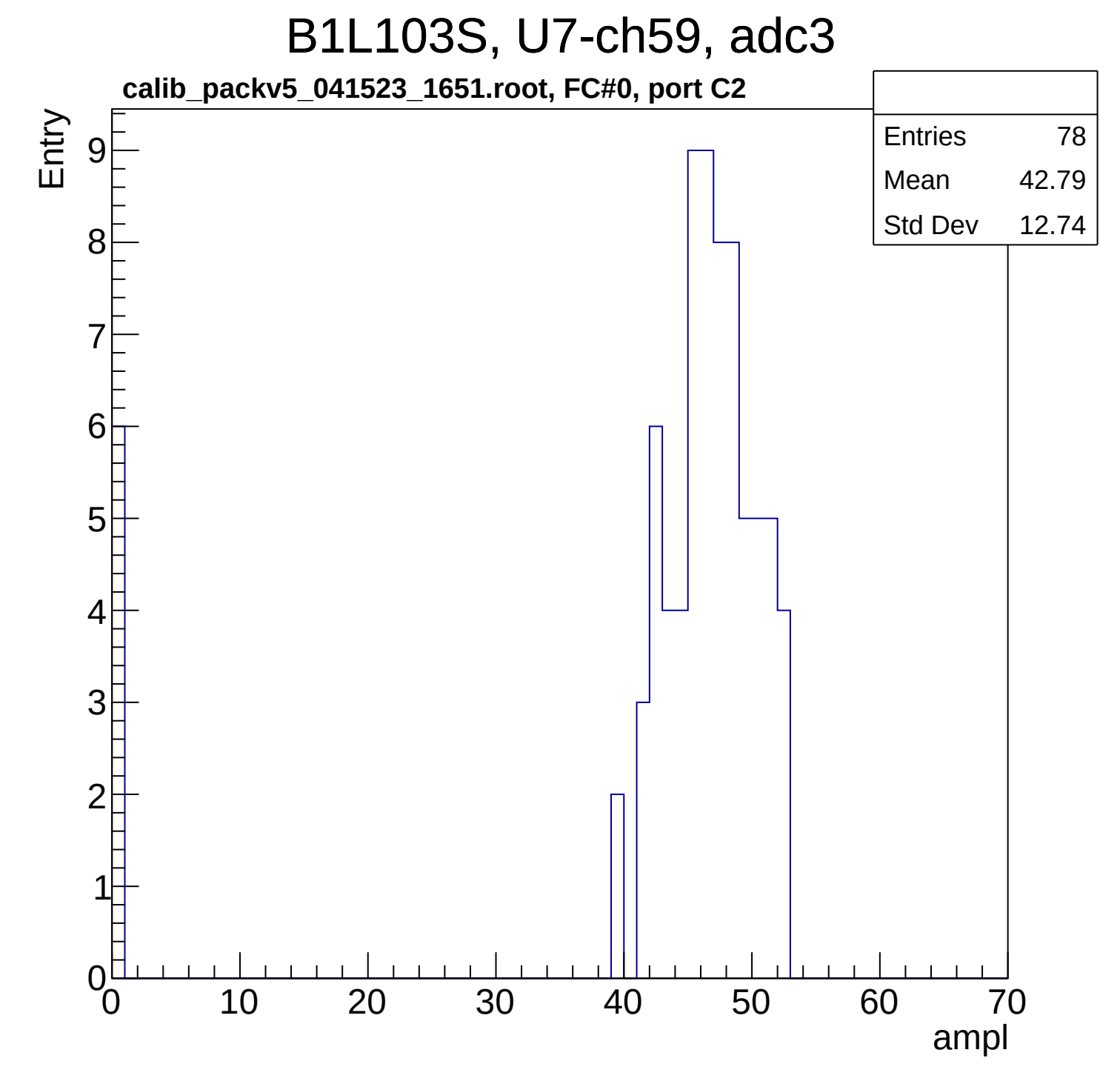
B1L103S, U7-ch59, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 42.79
Std Dev 12.74
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
50
60
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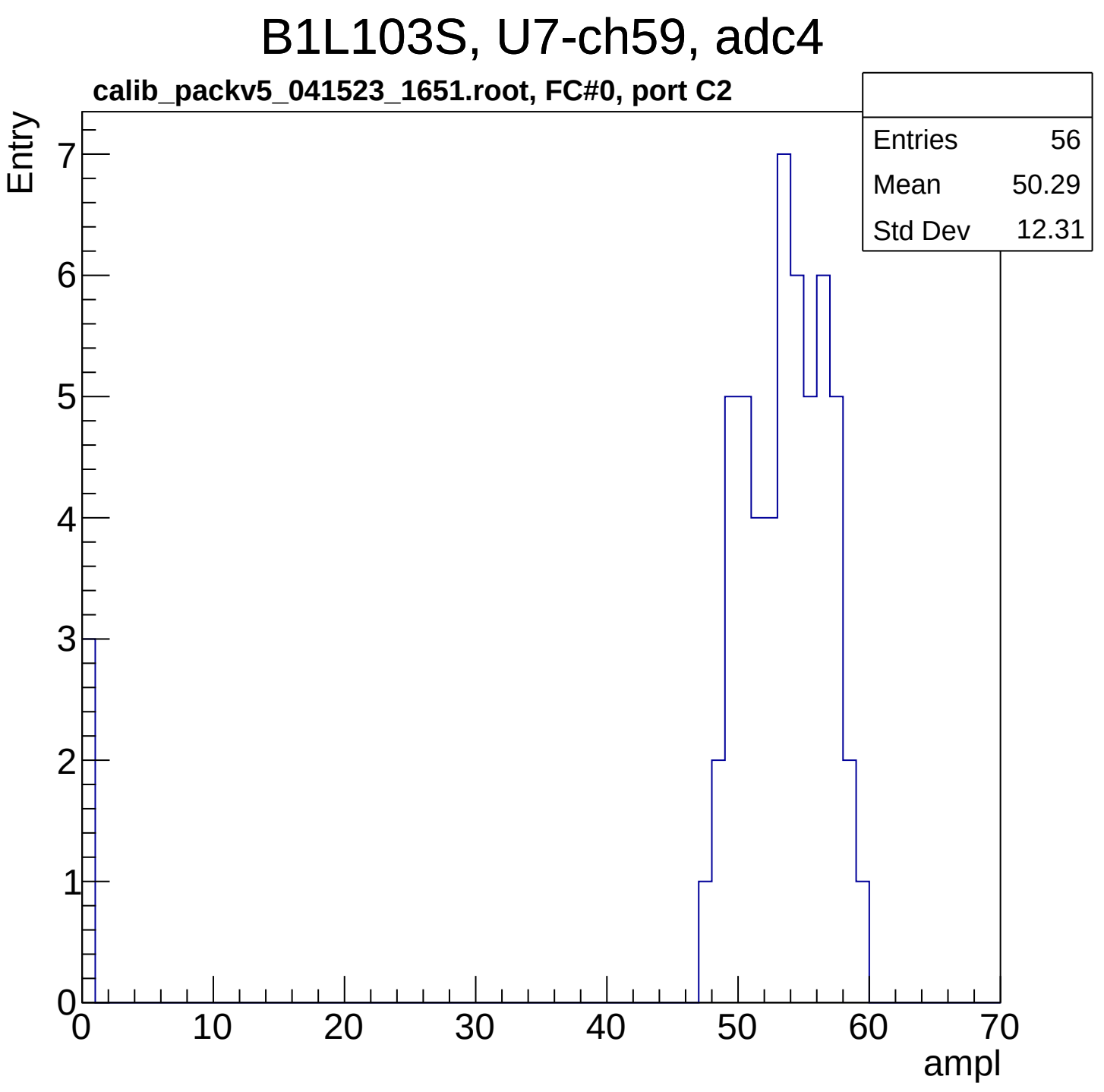
B1L103S, U7-ch59, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 50.29
Std Dev 12.31
Entry
ampl
0
1
2
3
4
5
6
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0
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60
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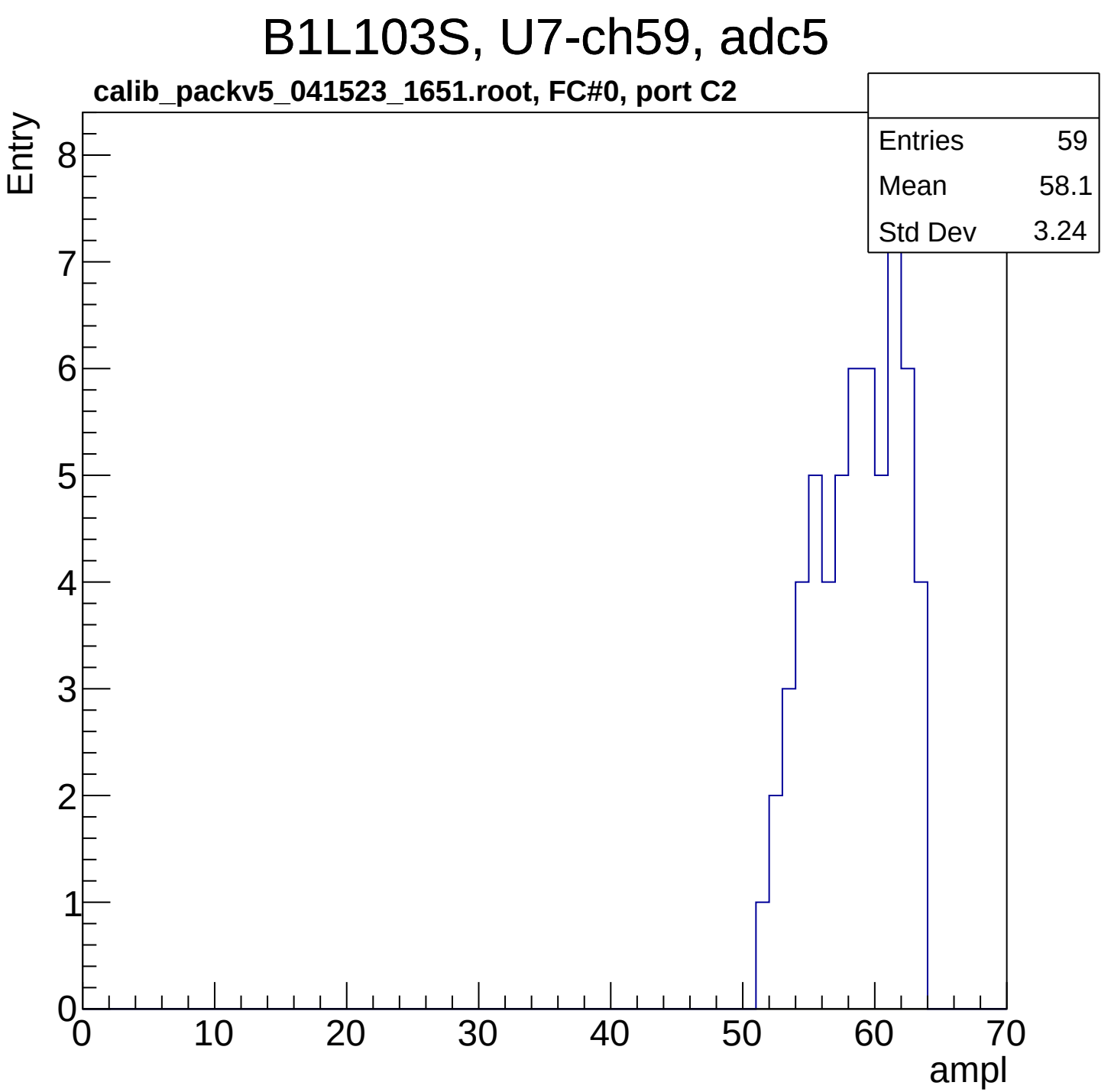
B1L103S, U7-ch59, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 58.1
Std Dev 3.24
Entry
ampl
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7
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0
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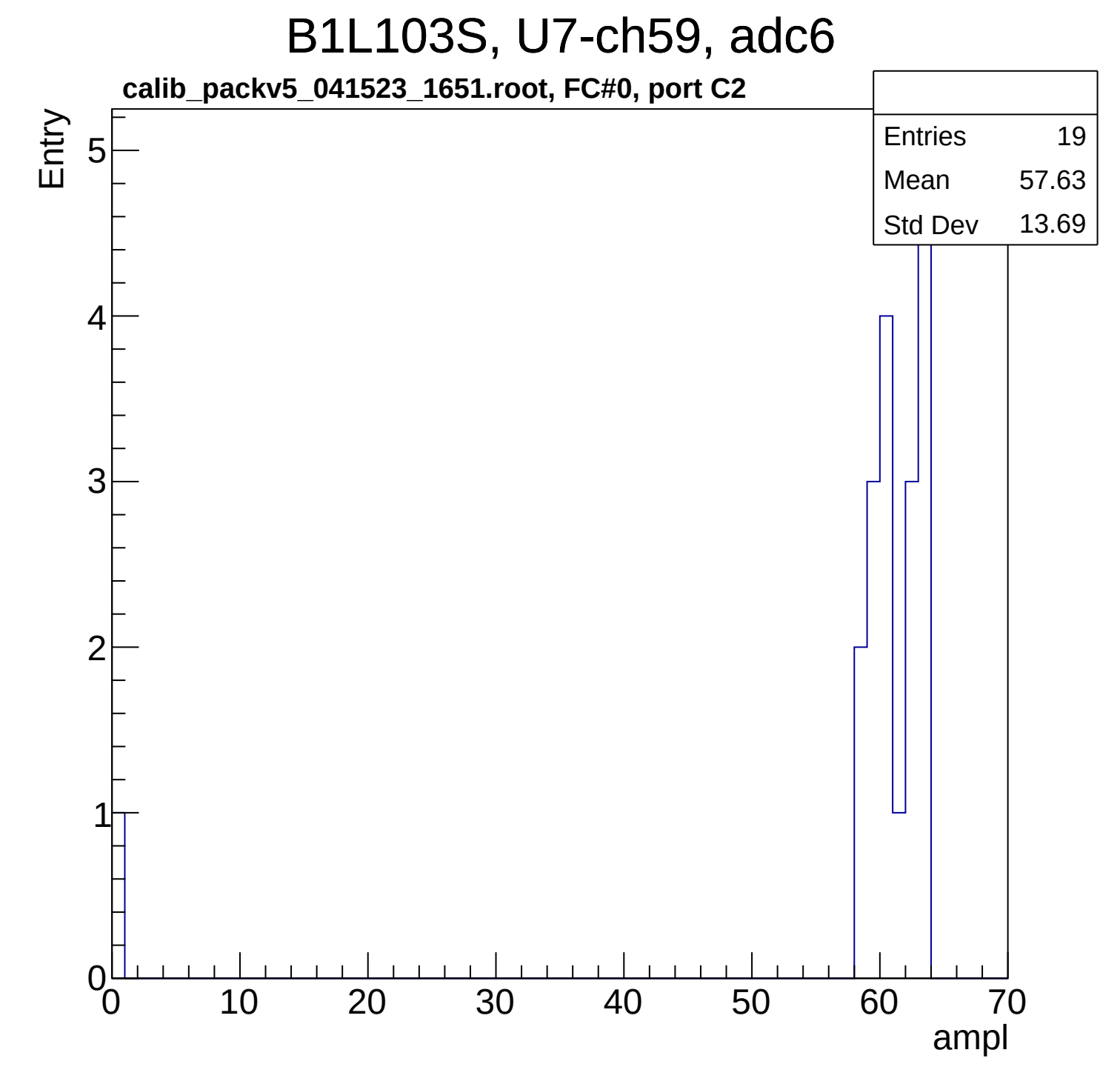
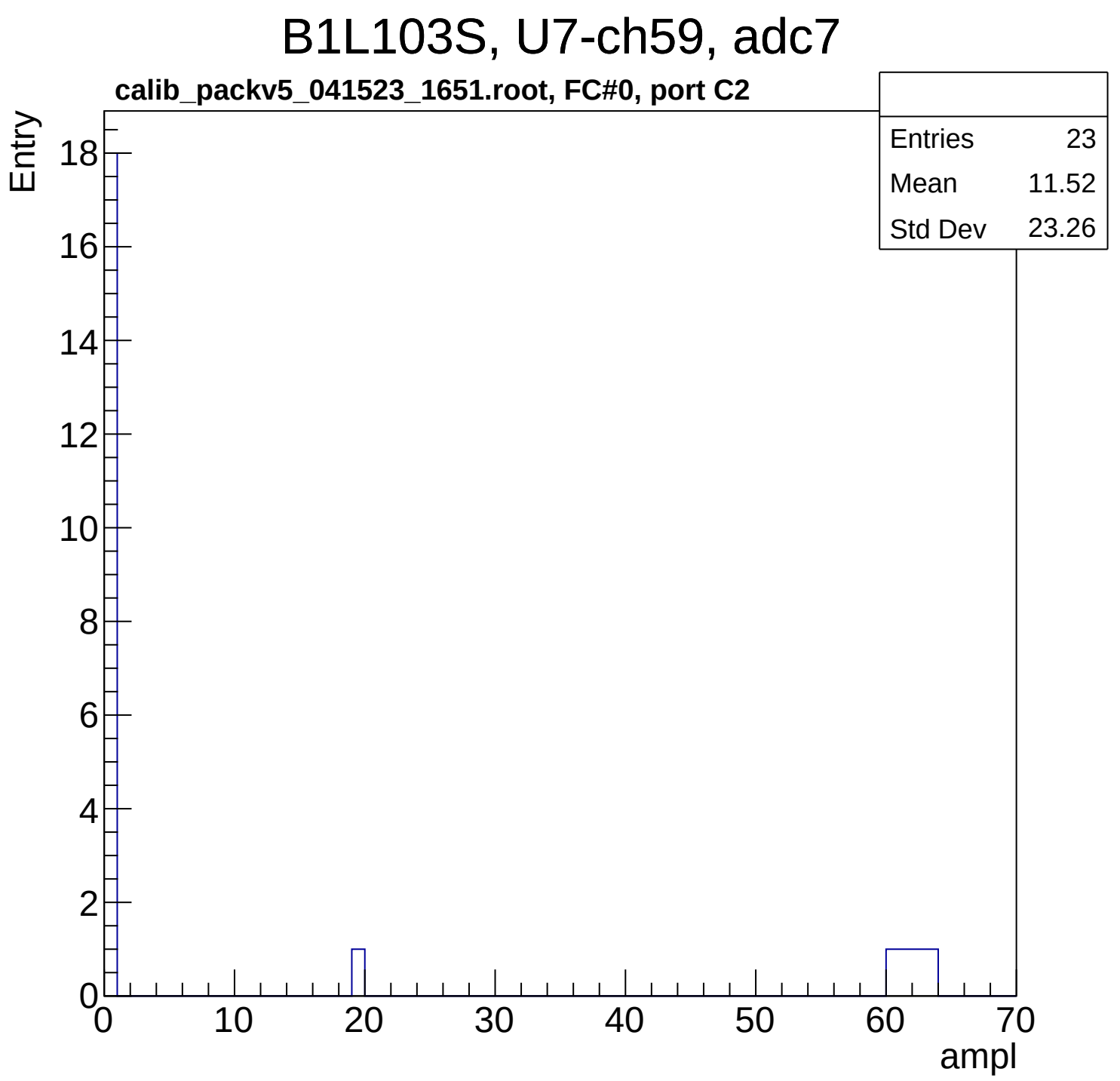
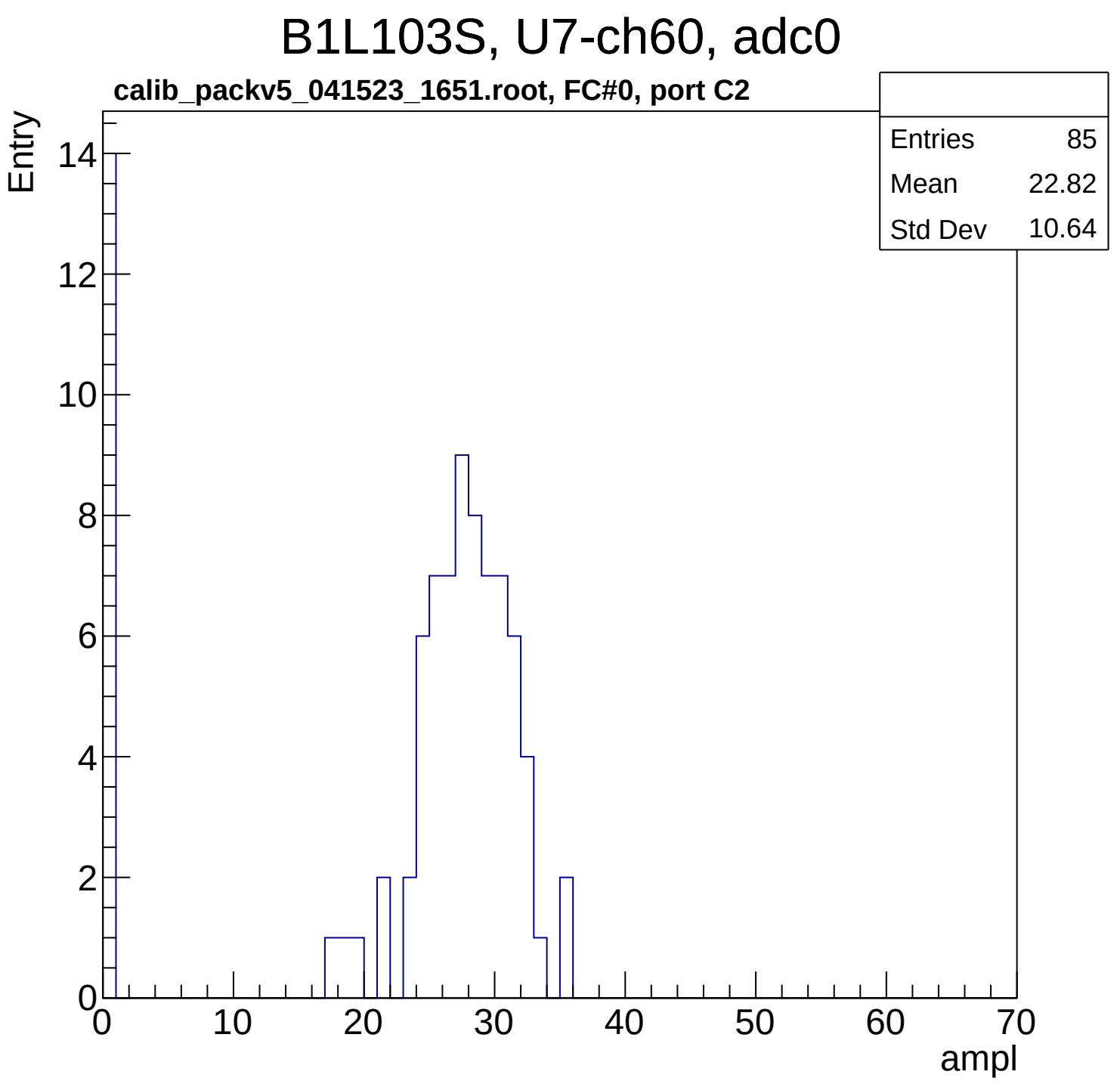

B1L103S, U7-ch59, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 57.63
Std Dev 13.69
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch59, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 23
Mean 11.52
Std Dev 23.26
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch60, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 22.82
Std Dev 10.64
Entry
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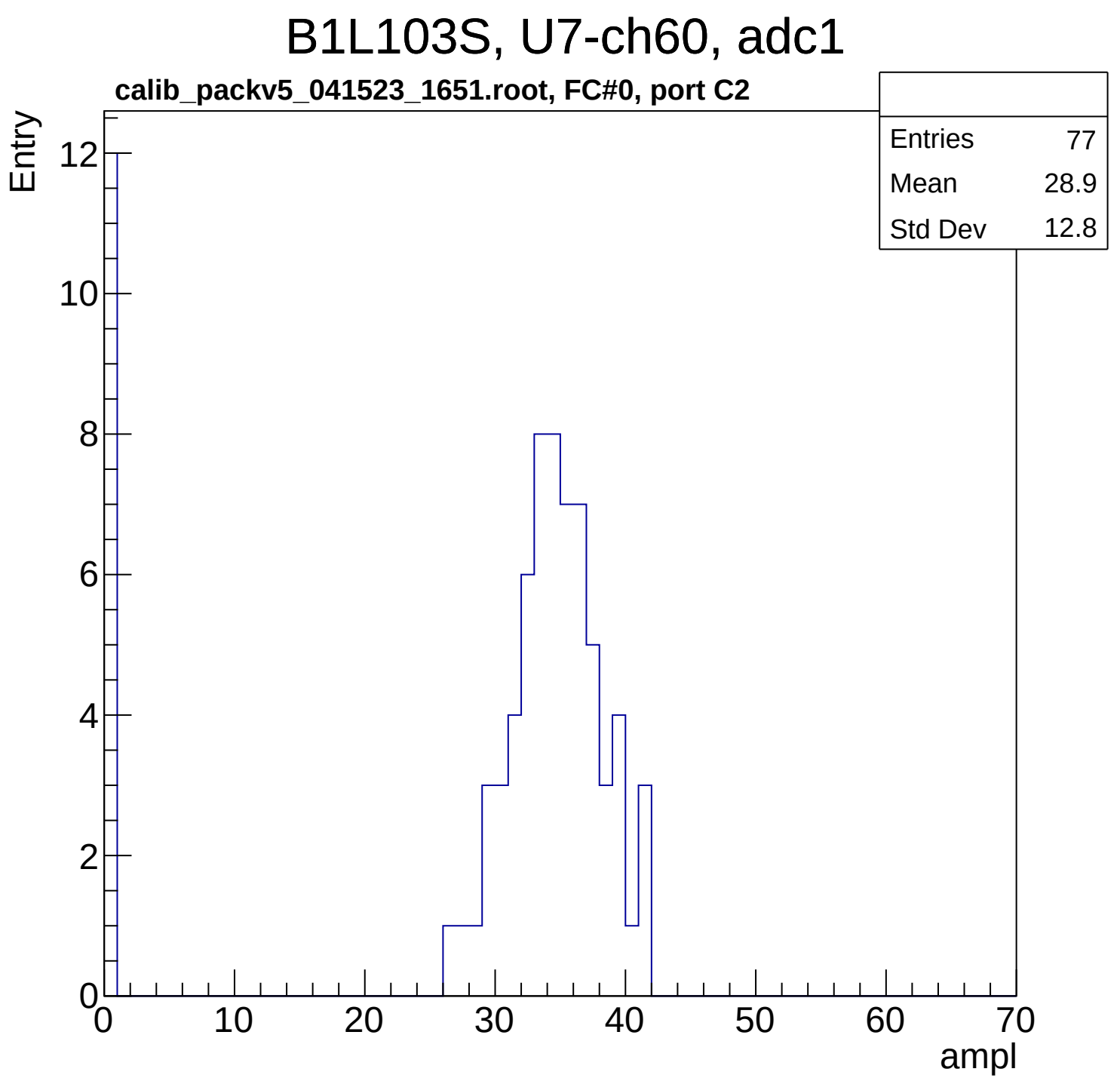
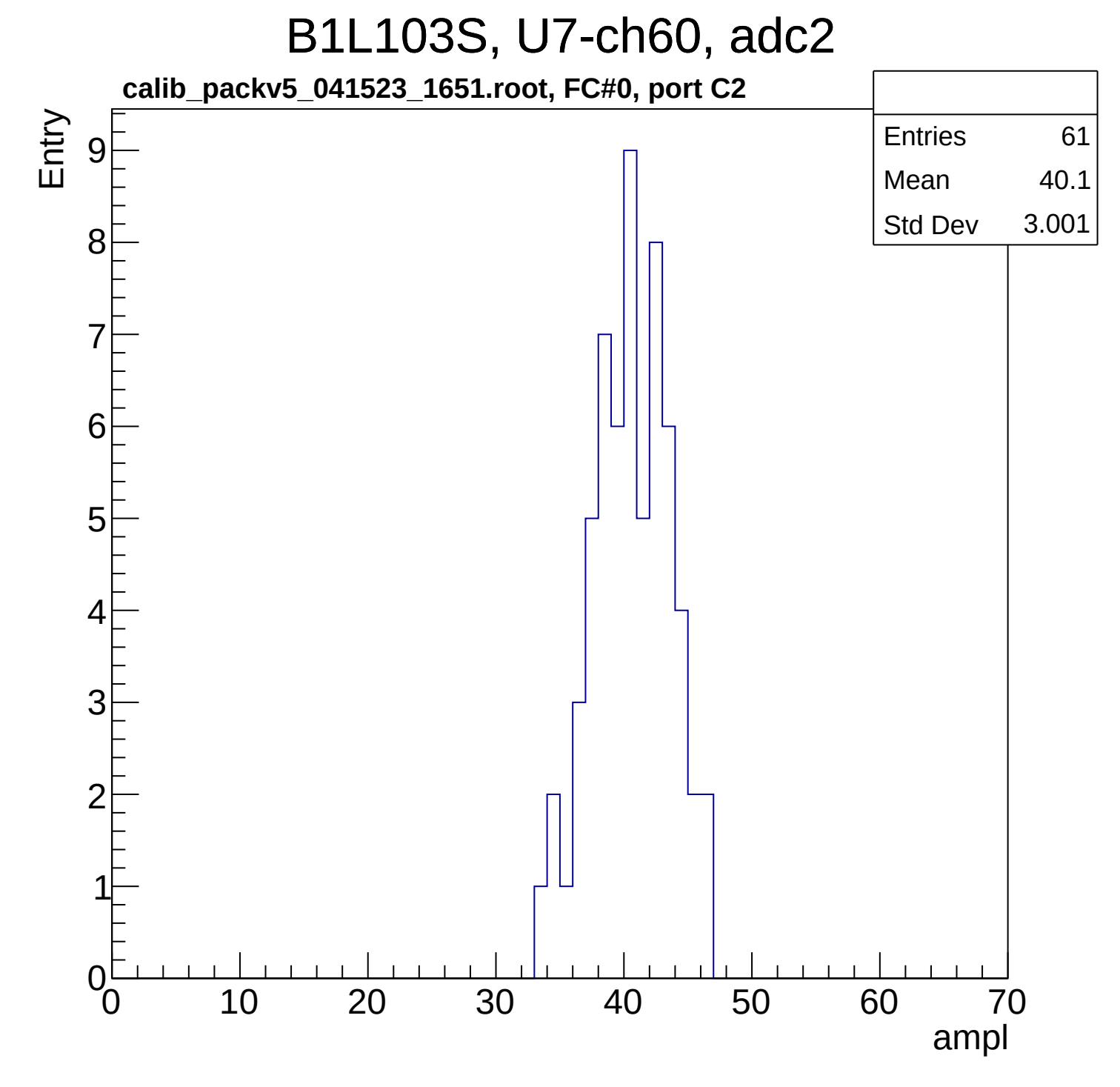
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch60, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 28.9
Std Dev 12.8
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch60, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 40.1
Std Dev 3.001
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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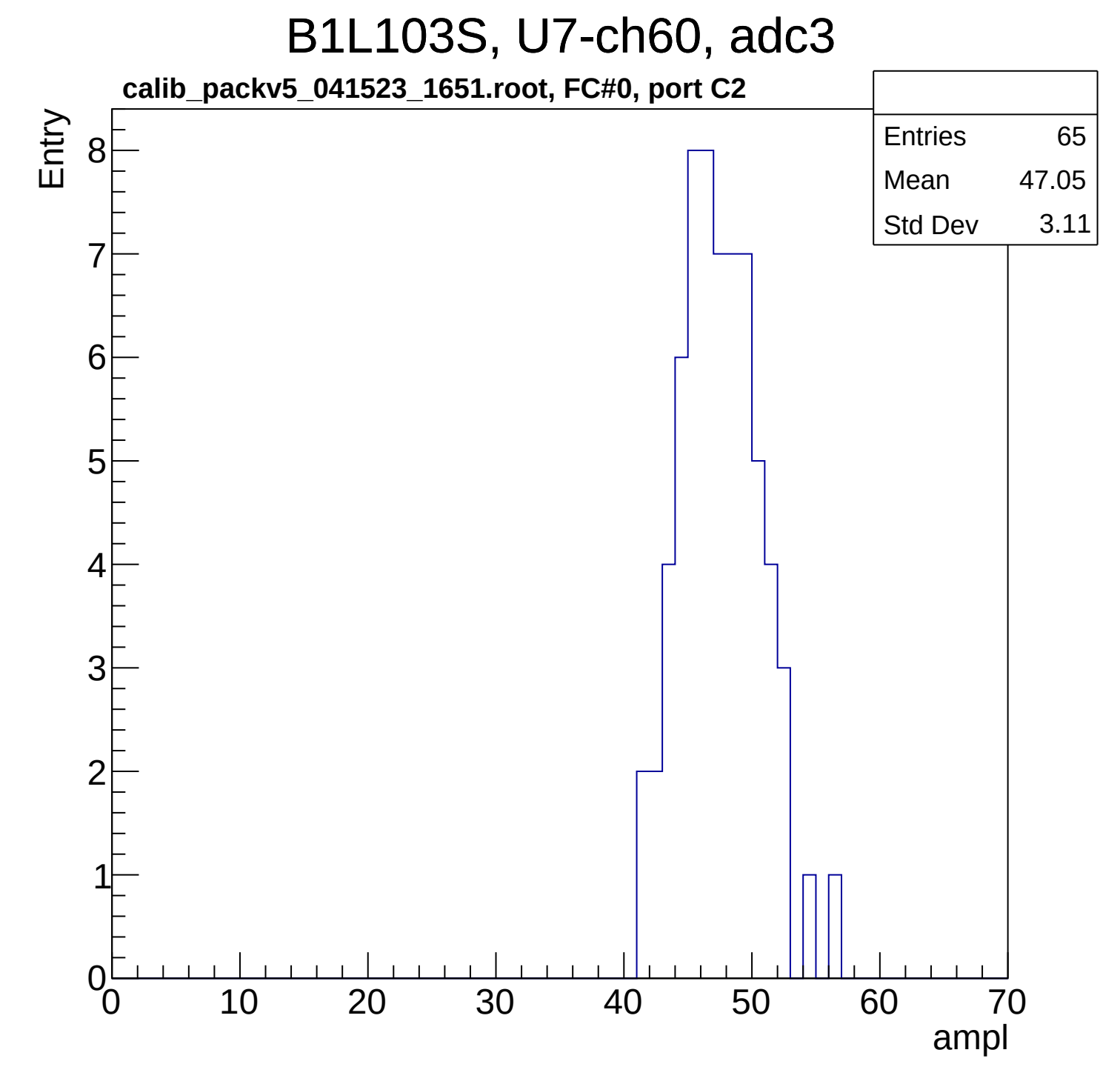
B1L103S, U7-ch60, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 47.05
Std Dev 3.11
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
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40
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60
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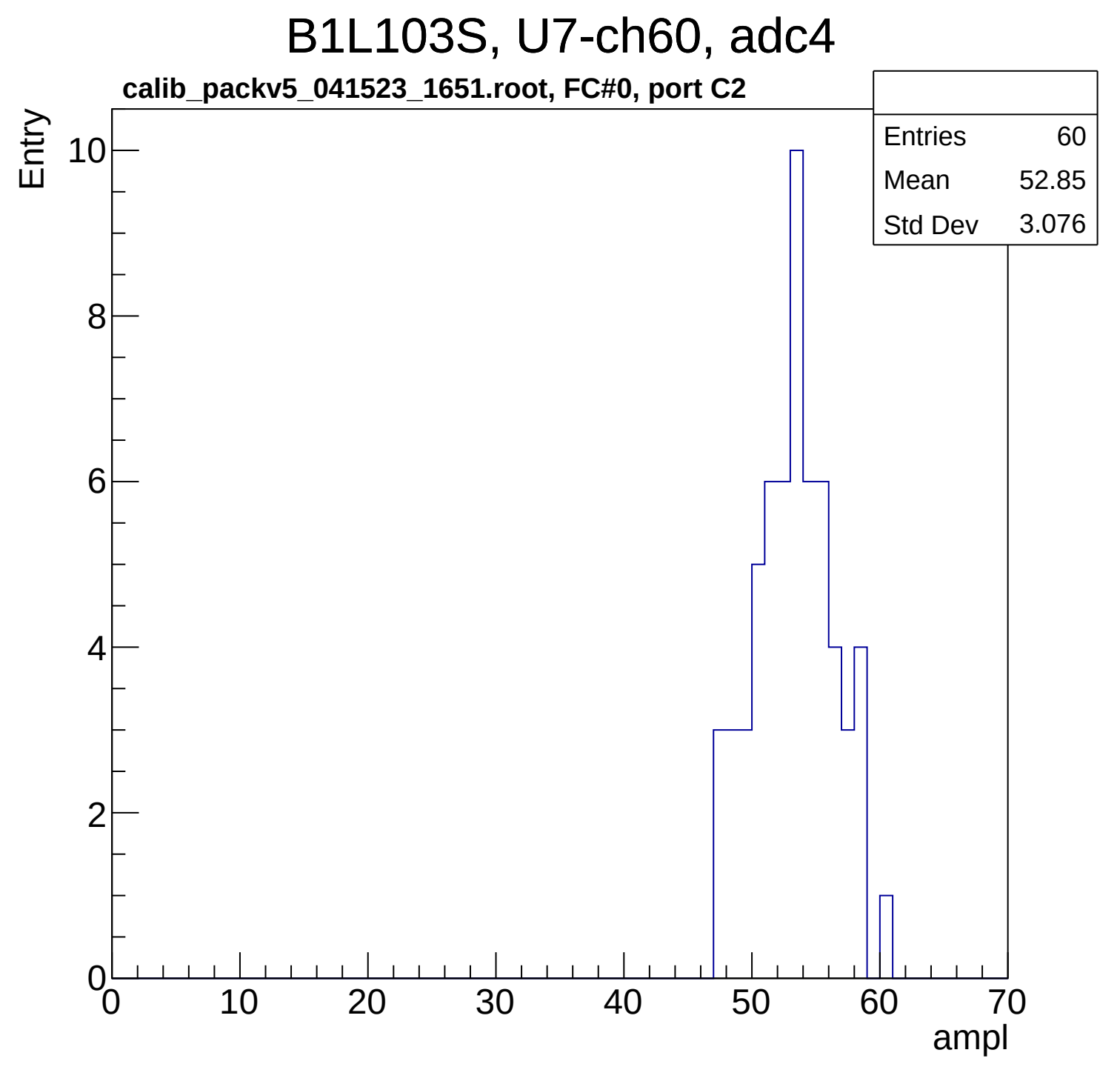
B1L103S, U7-ch60, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 52.85
Std Dev 3.076
Entry
ampl
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4
6
8
10
0
10
20
30
40
50
60
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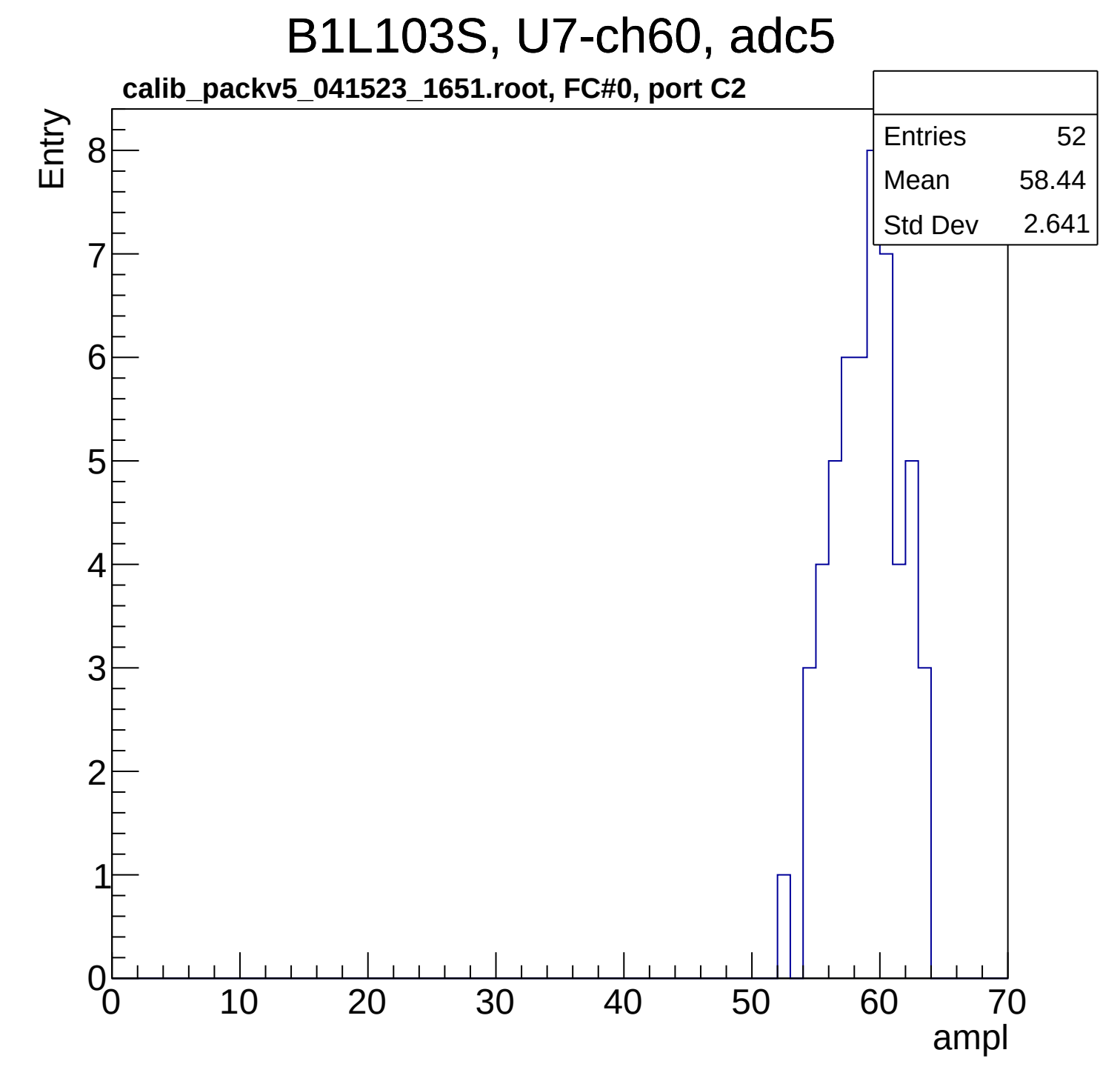
B1L103S, U7-ch60, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 58.44
Std Dev 2.641
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
30
40
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60
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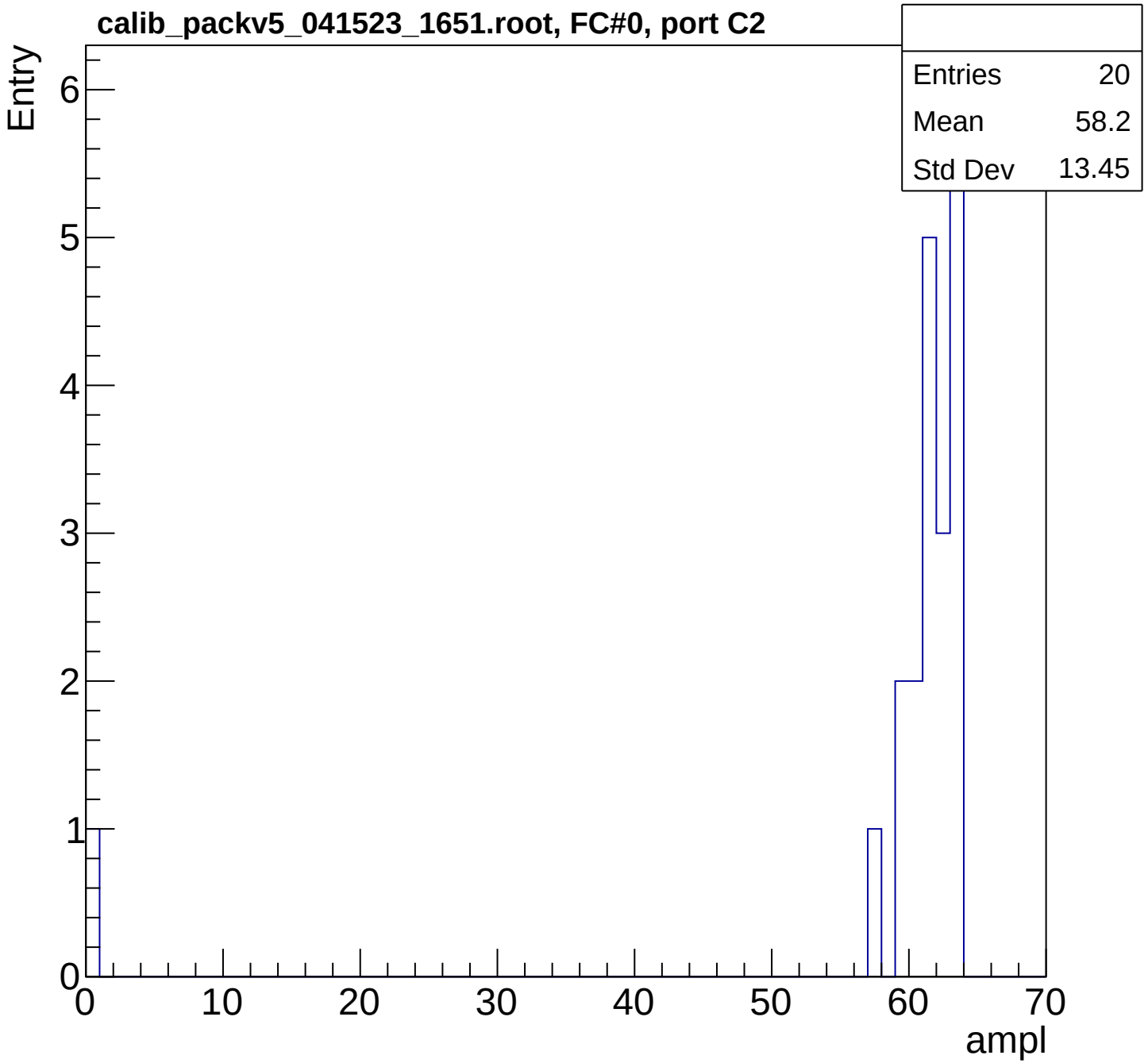
B1L103S, U7-ch60, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 58.2
Std Dev 13.45
Entry
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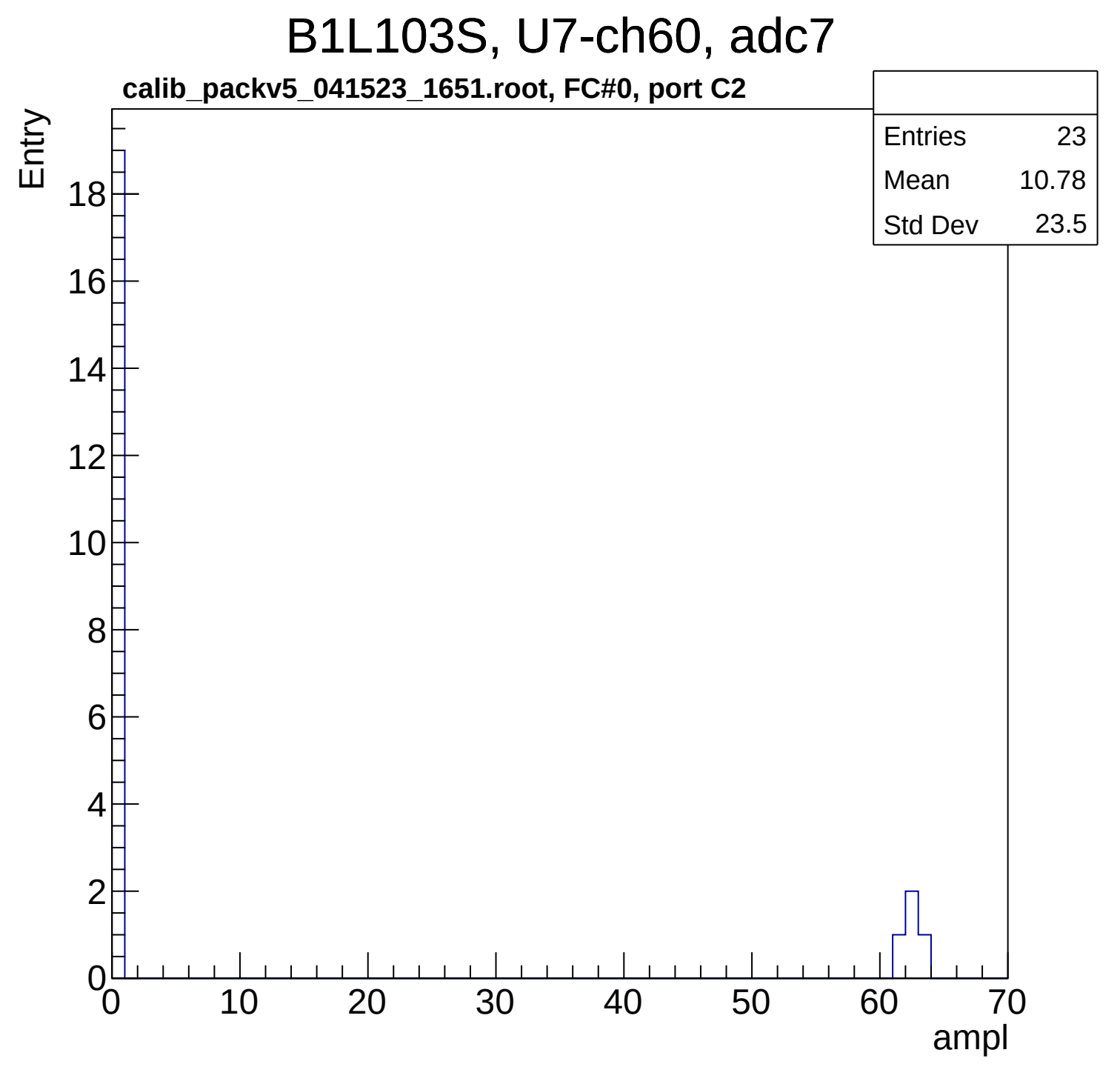
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch60, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 23
Mean 10.78
Std Dev 23.5
Entry
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6
8
10
12
14
16
18
0
10
20
30
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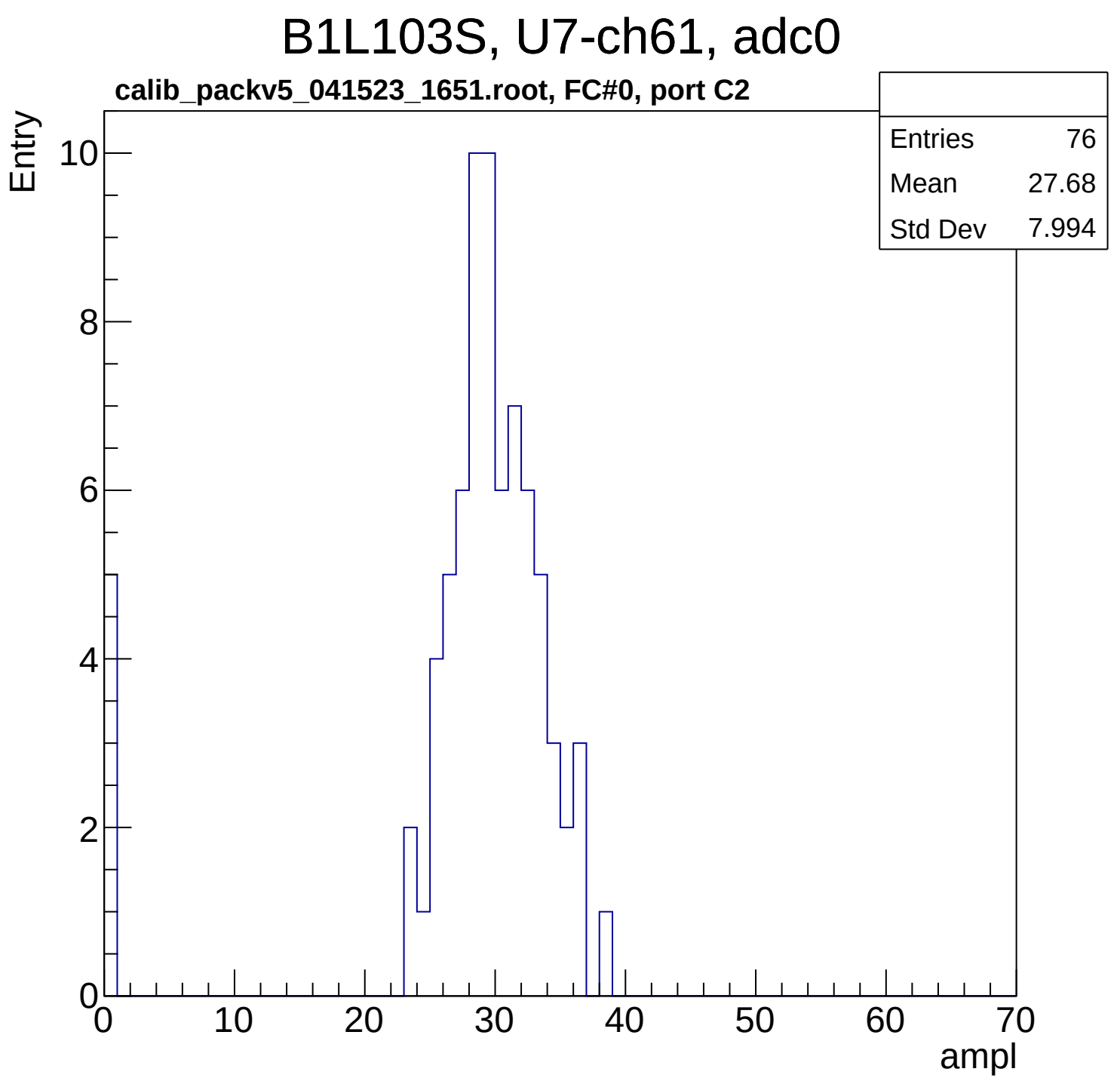
50
60
70
ampl


B1L103S, U7-ch61, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 27.68
Std Dev 7.994
Entry
ampl
0
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4
6
8
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0
10
20
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40
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60
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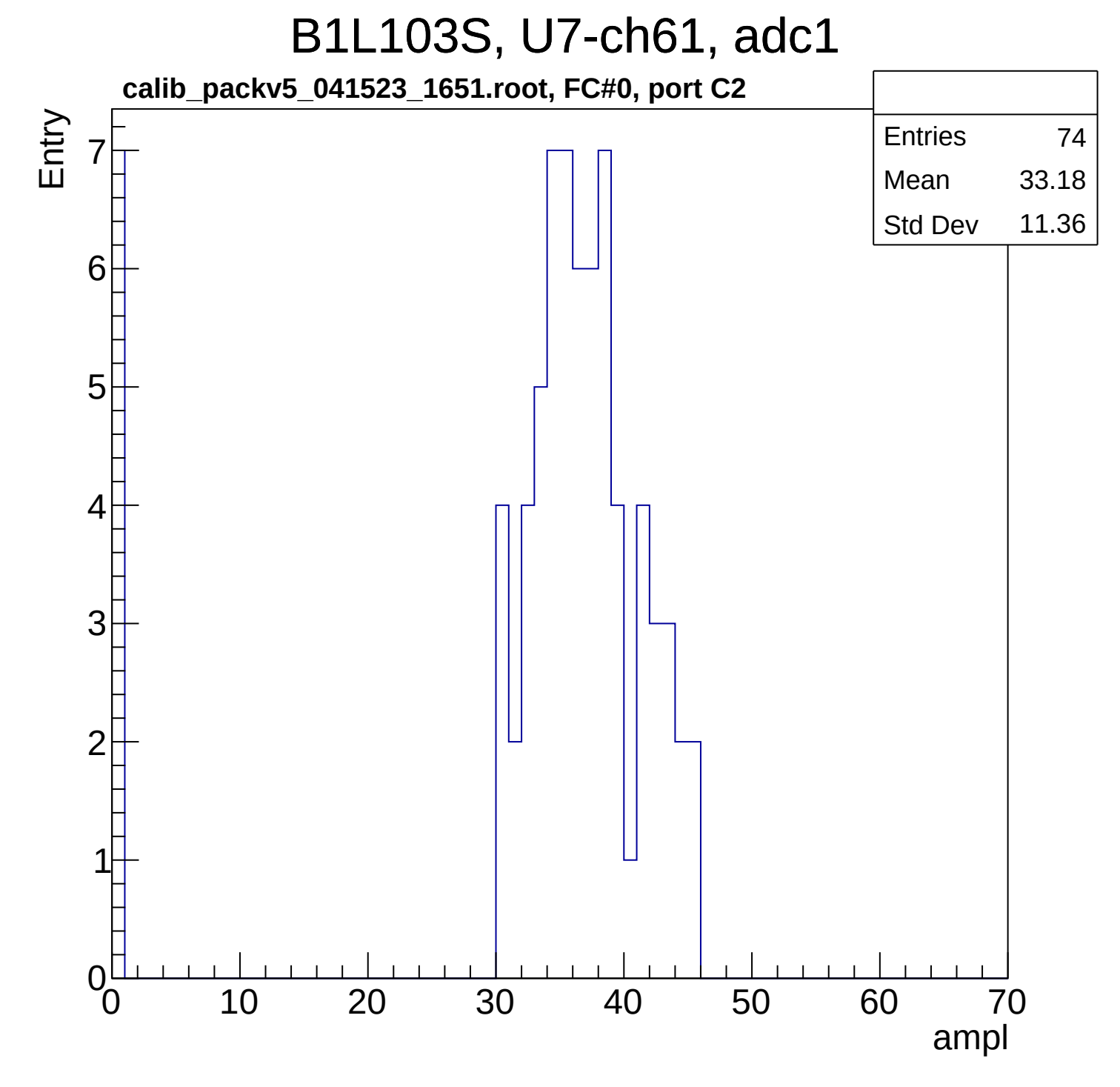
B1L103S, U7-ch61, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 33.18
Std Dev 11.36
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
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40
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60
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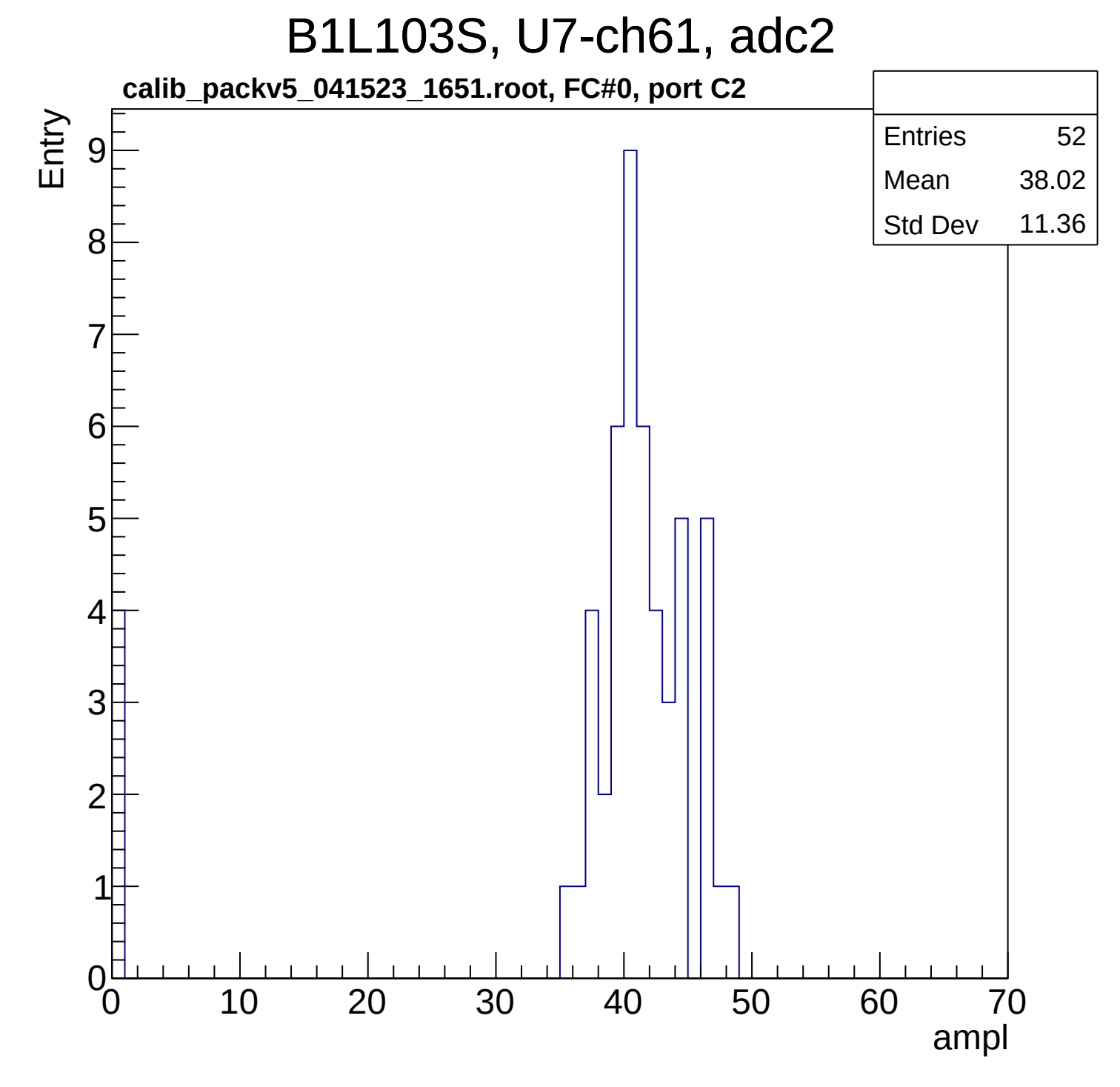
B1L103S, U7-ch61, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 38.02
Std Dev 11.36
Entry
ampl
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2
3
4
5
6
7
8
9
0
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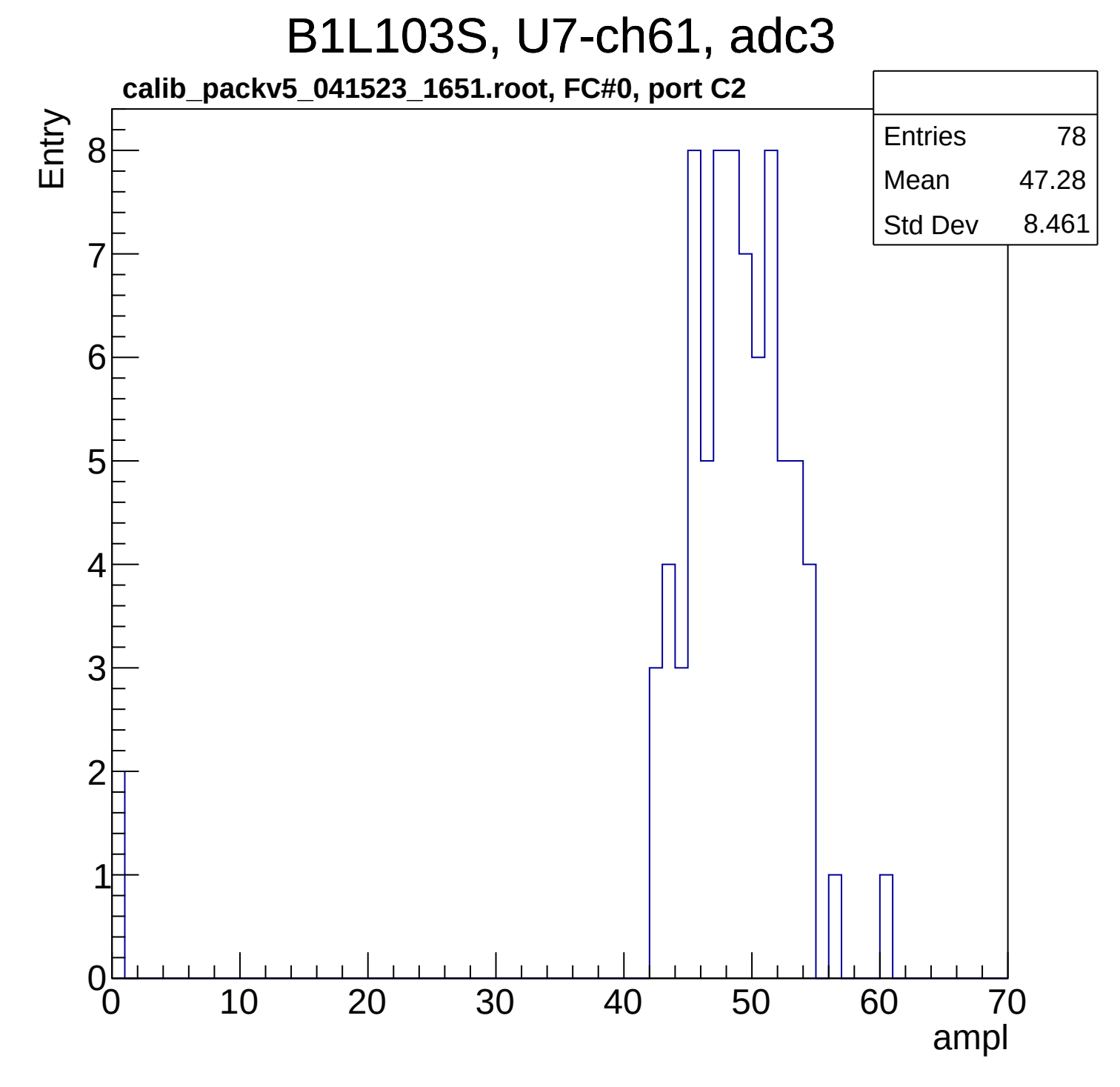
B1L103S, U7-ch61, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 47.28
Std Dev 8.461
Entry
ampl
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2
3
4
5
6
7
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0
10
20
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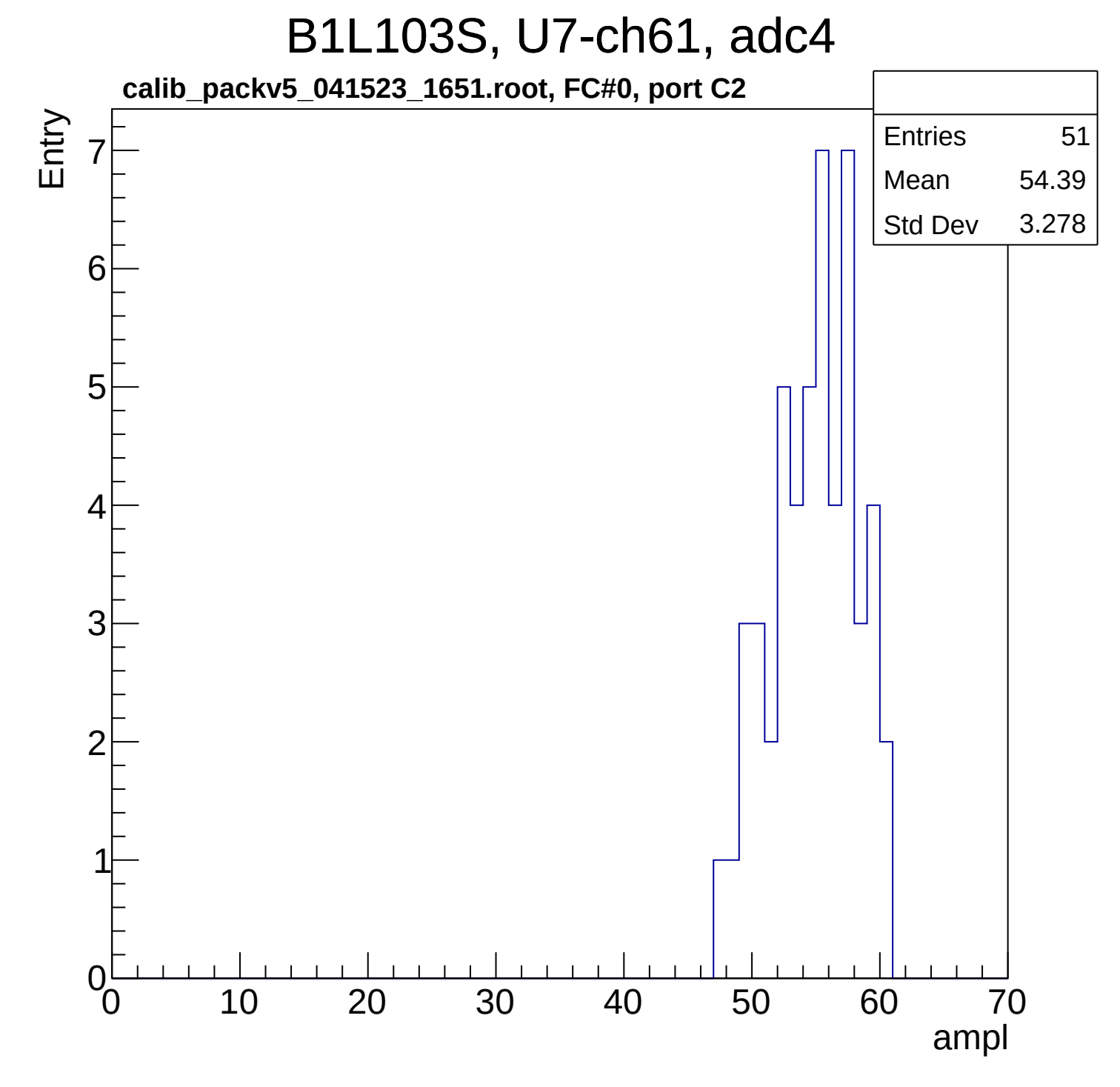
B1L103S, U7-ch61, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 54.39
Std Dev 3.278
Entry
ampl
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3
4
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6
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0
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60
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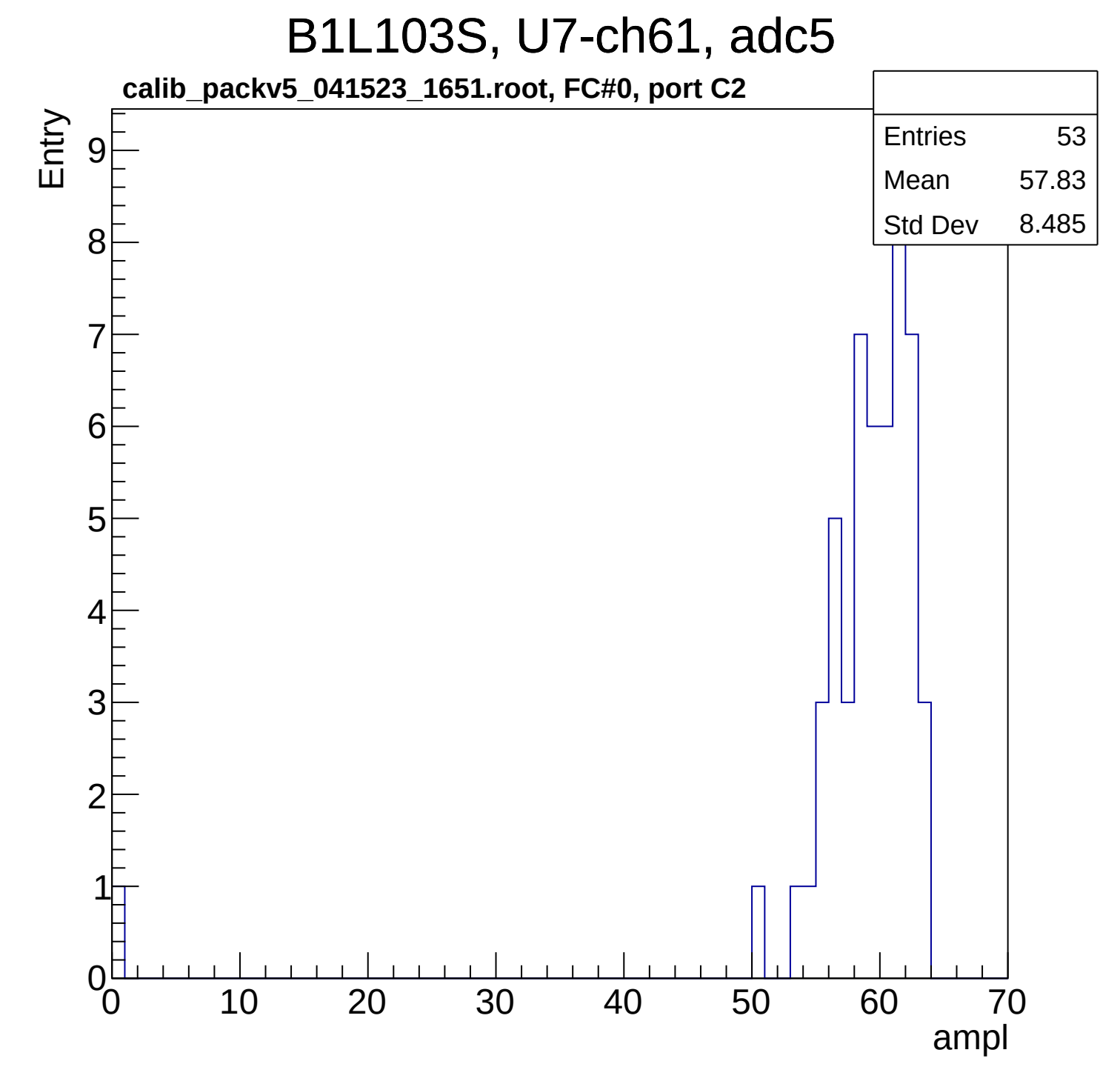
B1L103S, U7-ch61, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 57.83
Std Dev 8.485
Entry
ampl
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3
4
5
6
7
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0
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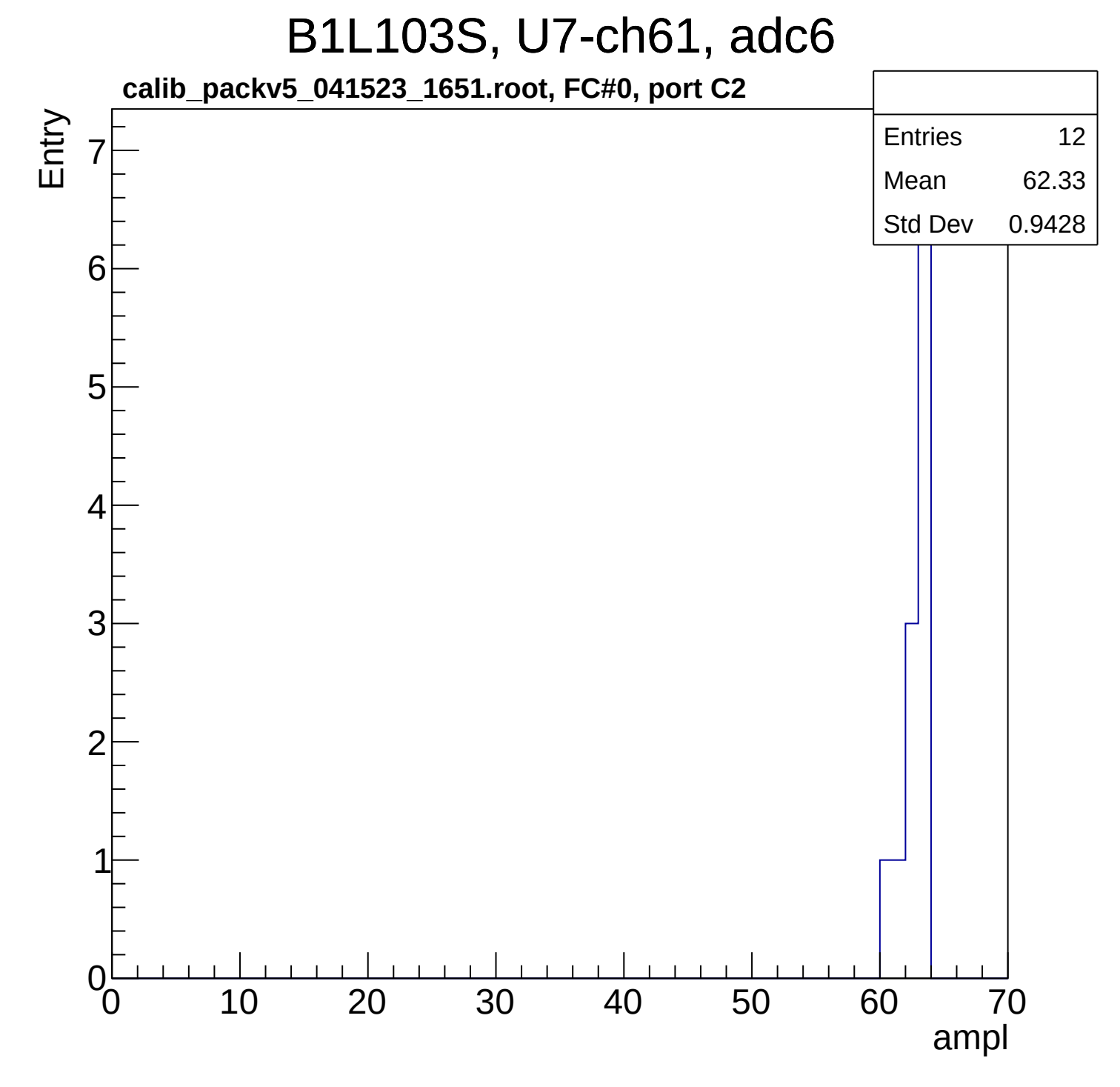
B1L103S, U7-ch61, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 62.33
Std Dev 0.9428
Entry
ampl
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4
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6
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0
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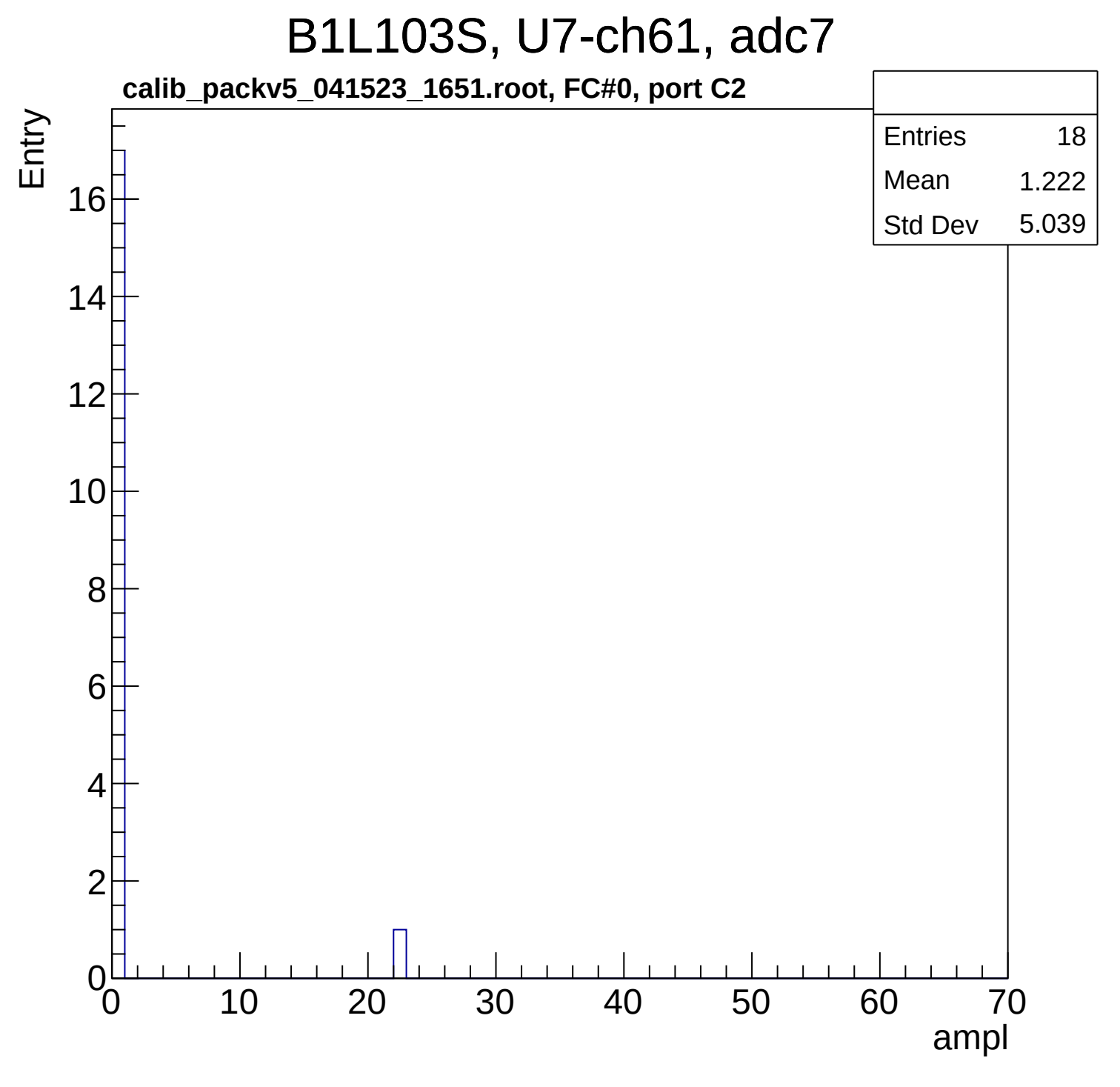
B1L103S, U7-ch61, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 1.222
Std Dev 5.039
Entry
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6
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10
12
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16
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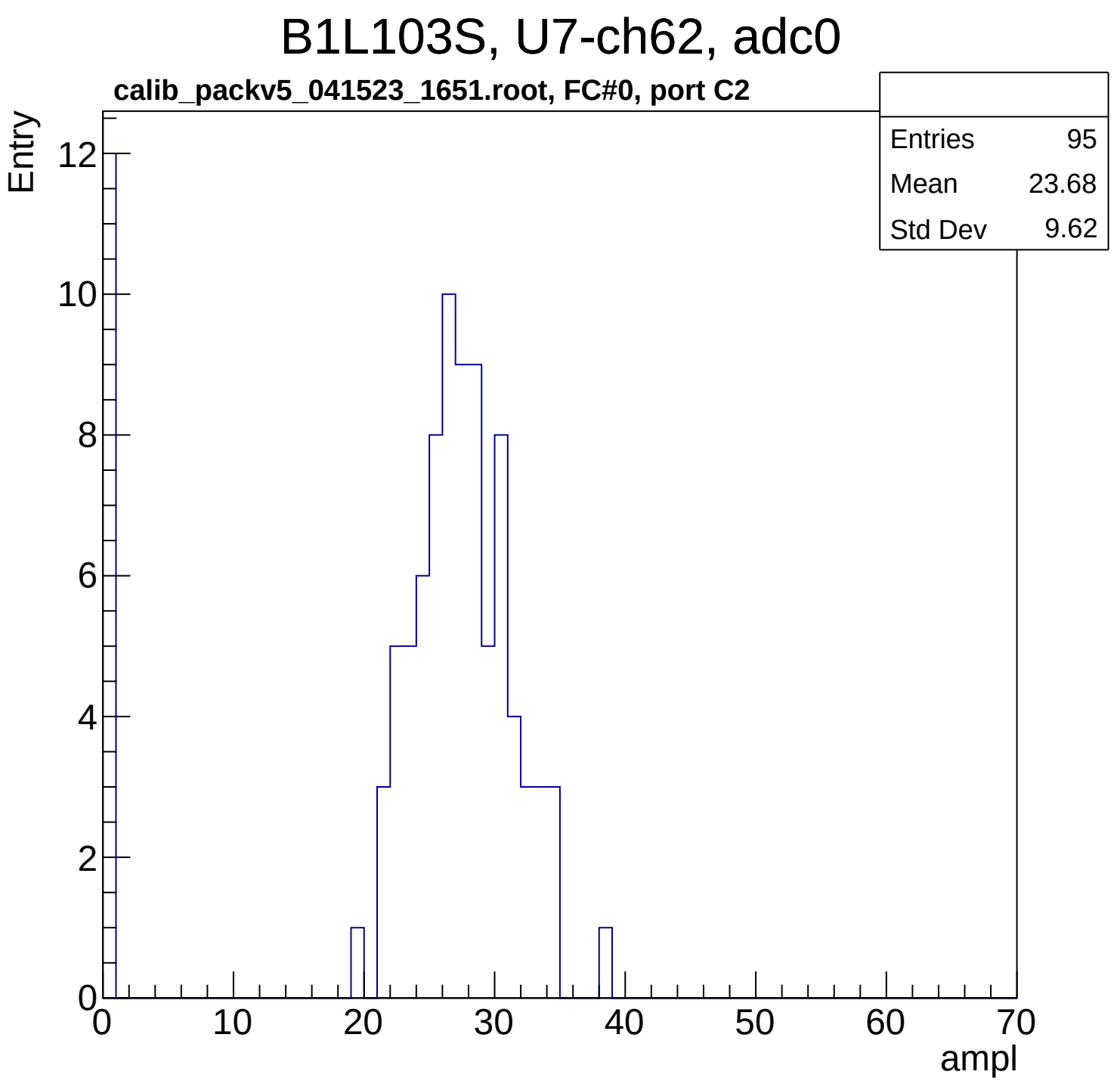
70
ampl


B1L103S, U7-ch62, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 95
Mean 23.68
Std Dev 9.62
Entry
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10
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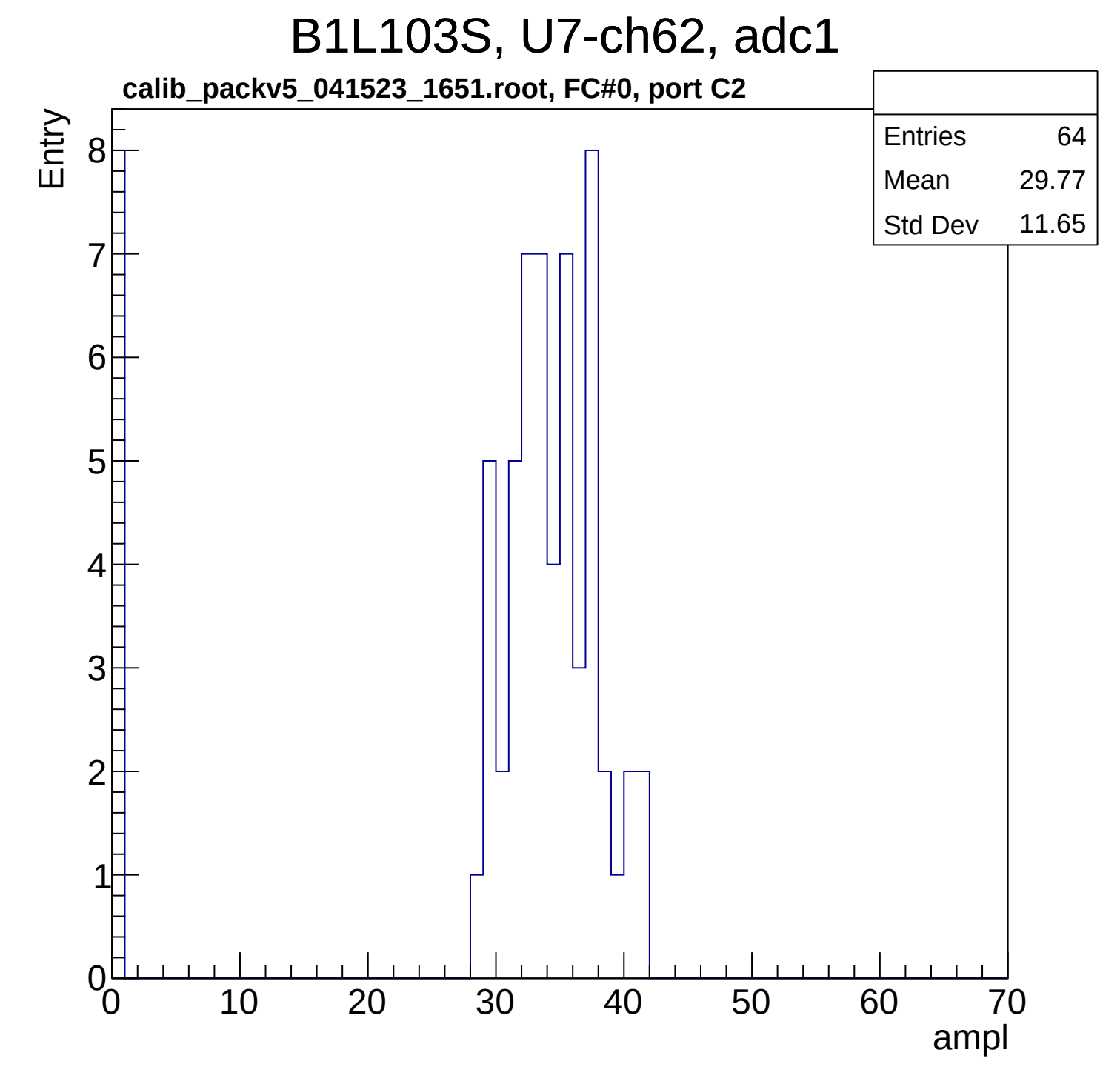
70
ampl


B1L103S, U7-ch62, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 29.77
Std Dev 11.65
Entry
ampl
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2
3
4
5
6
7
8
0
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60
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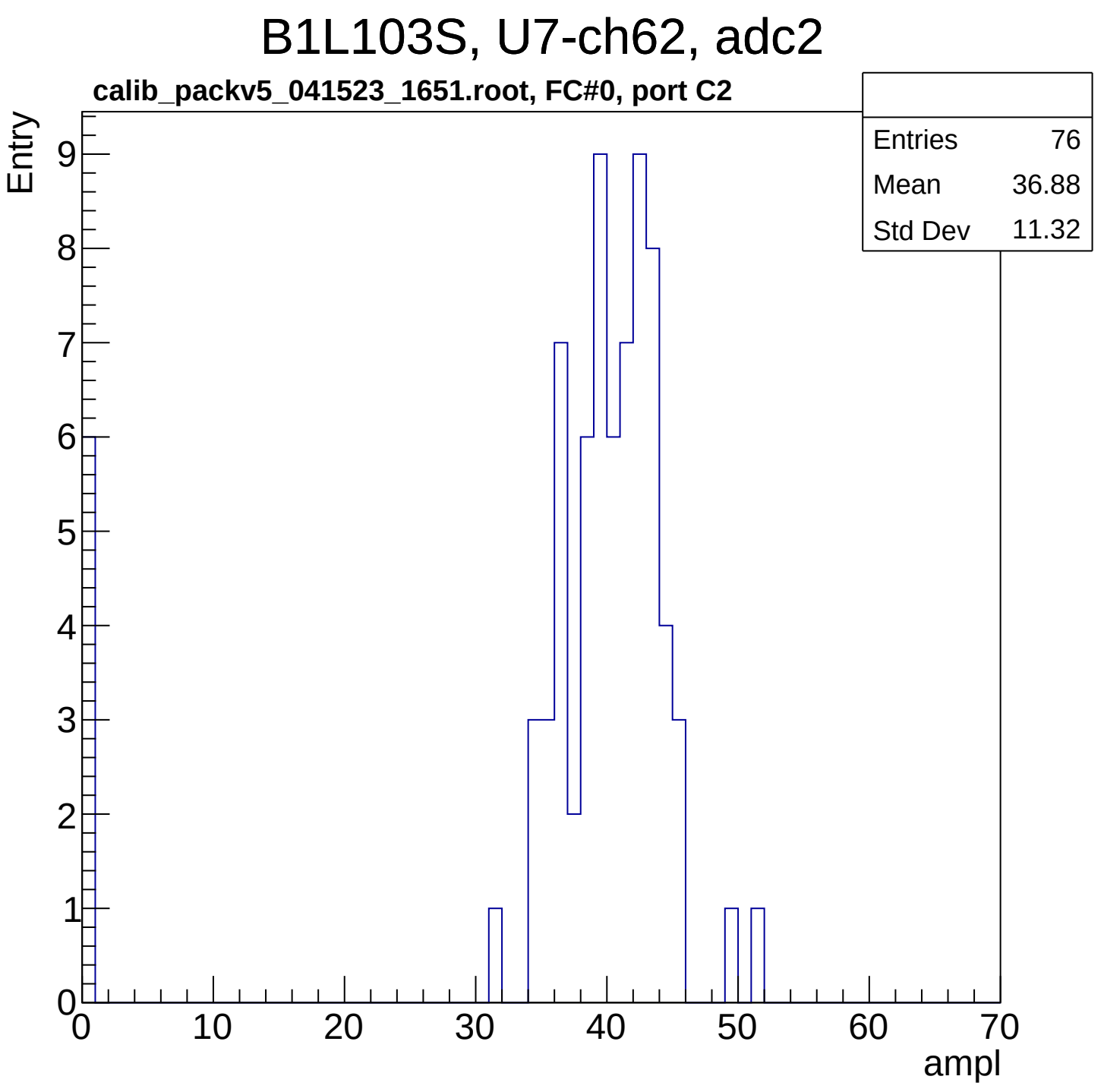
B1L103S, U7-ch62, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 36.88
Std Dev 11.32
Entry
ampl
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2
3
4
5
6
7
8
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0
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60
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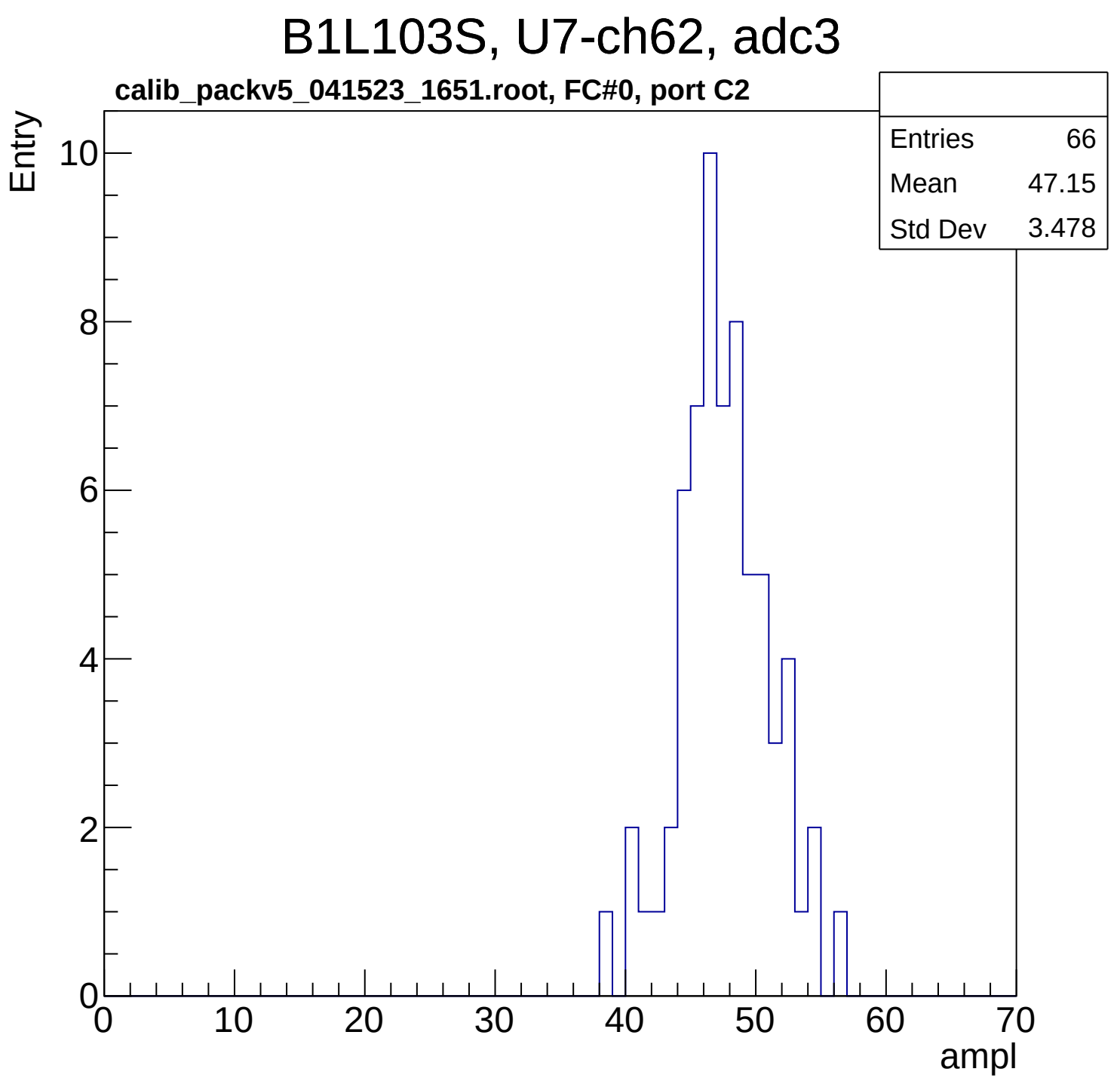
B1L103S, U7-ch62, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 47.15
Std Dev 3.478
Entry
ampl
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8
10
0
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20
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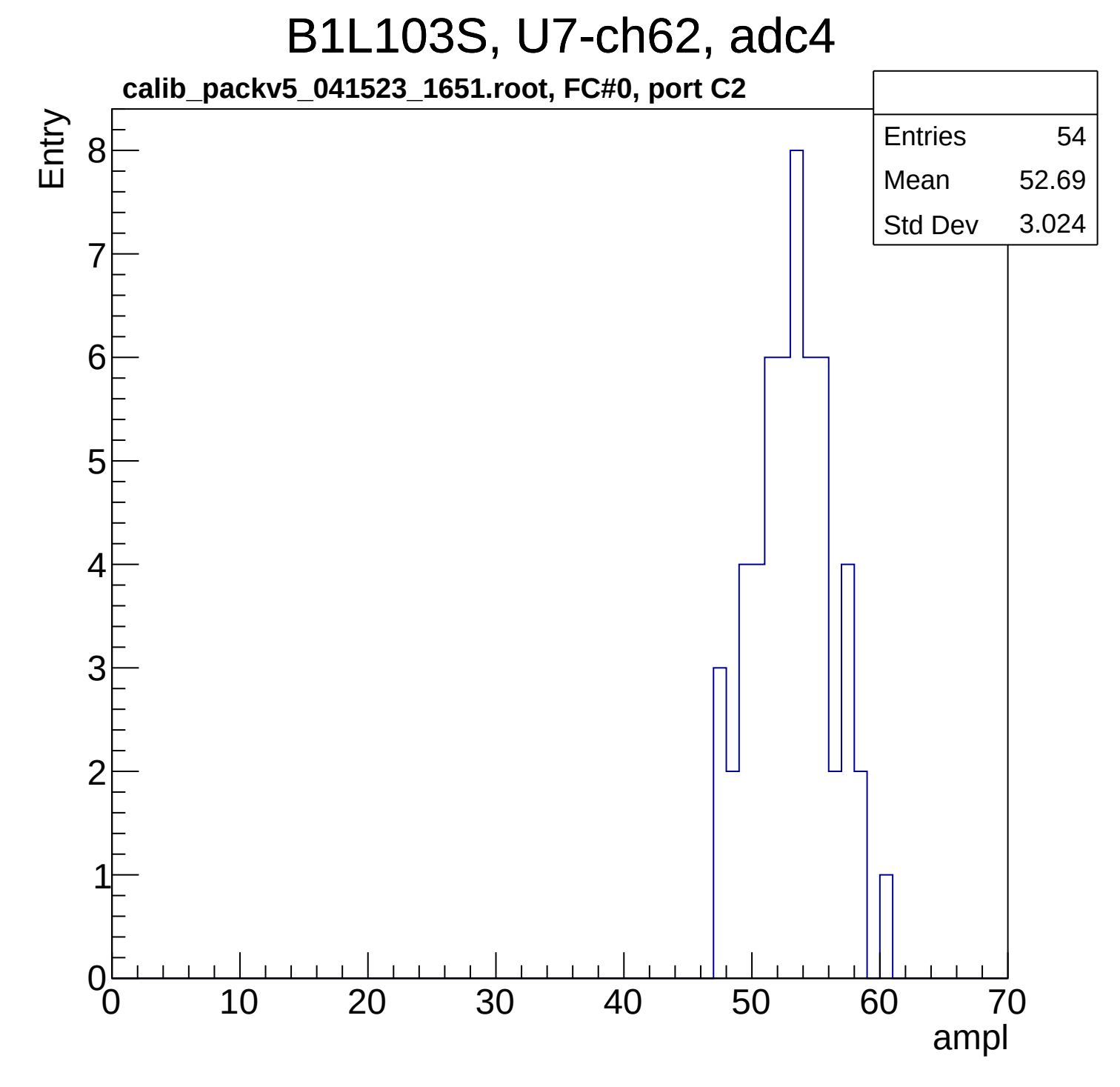
60
70


B1L103S, U7-ch62, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 52.69
Std Dev 3.024
Entry
ampl
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2
3
4
5
6
7
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0
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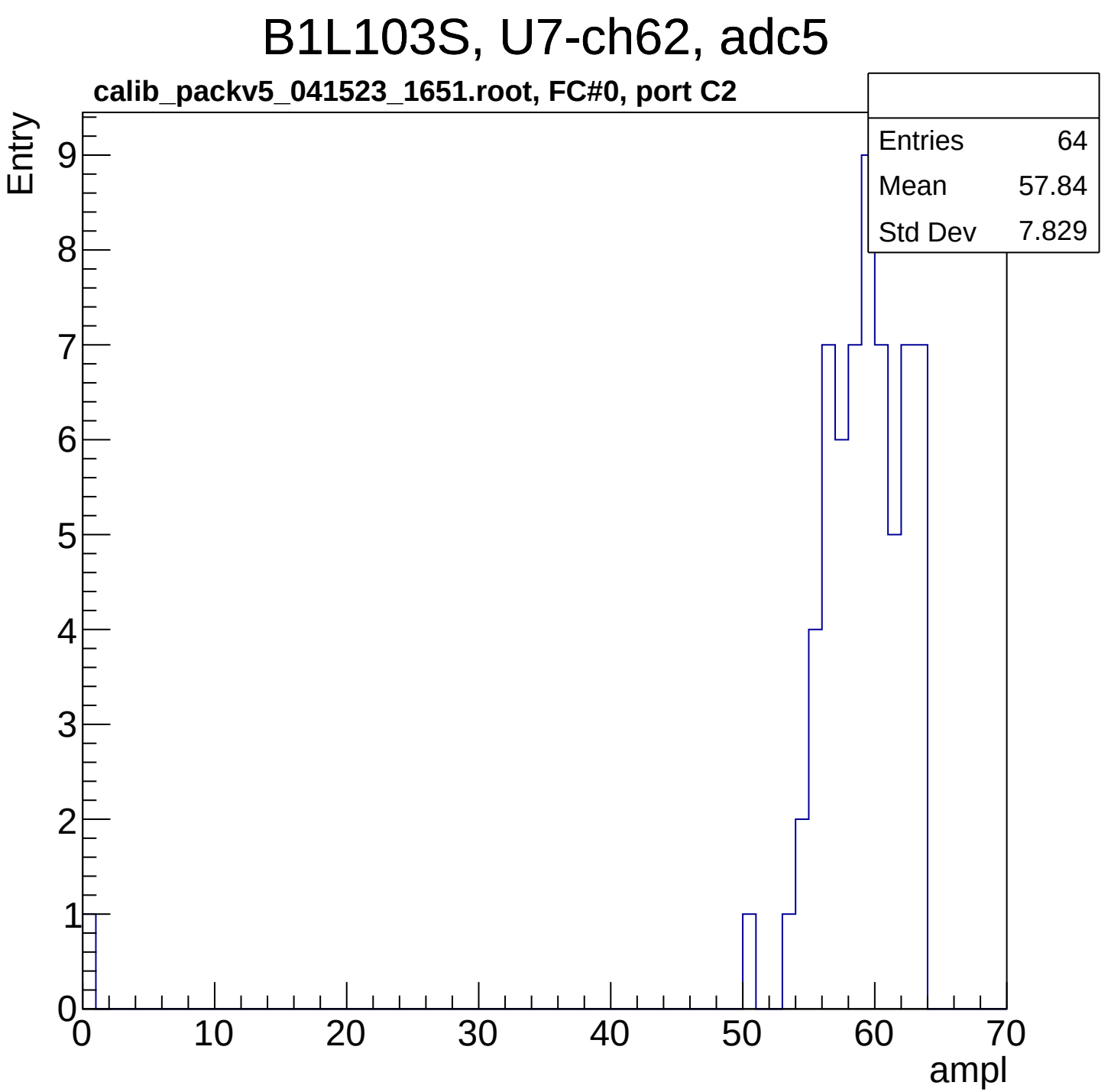
B1L103S, U7-ch62, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 57.84
Std Dev 7.829
Entry
ampl
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4
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6
7
8
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0
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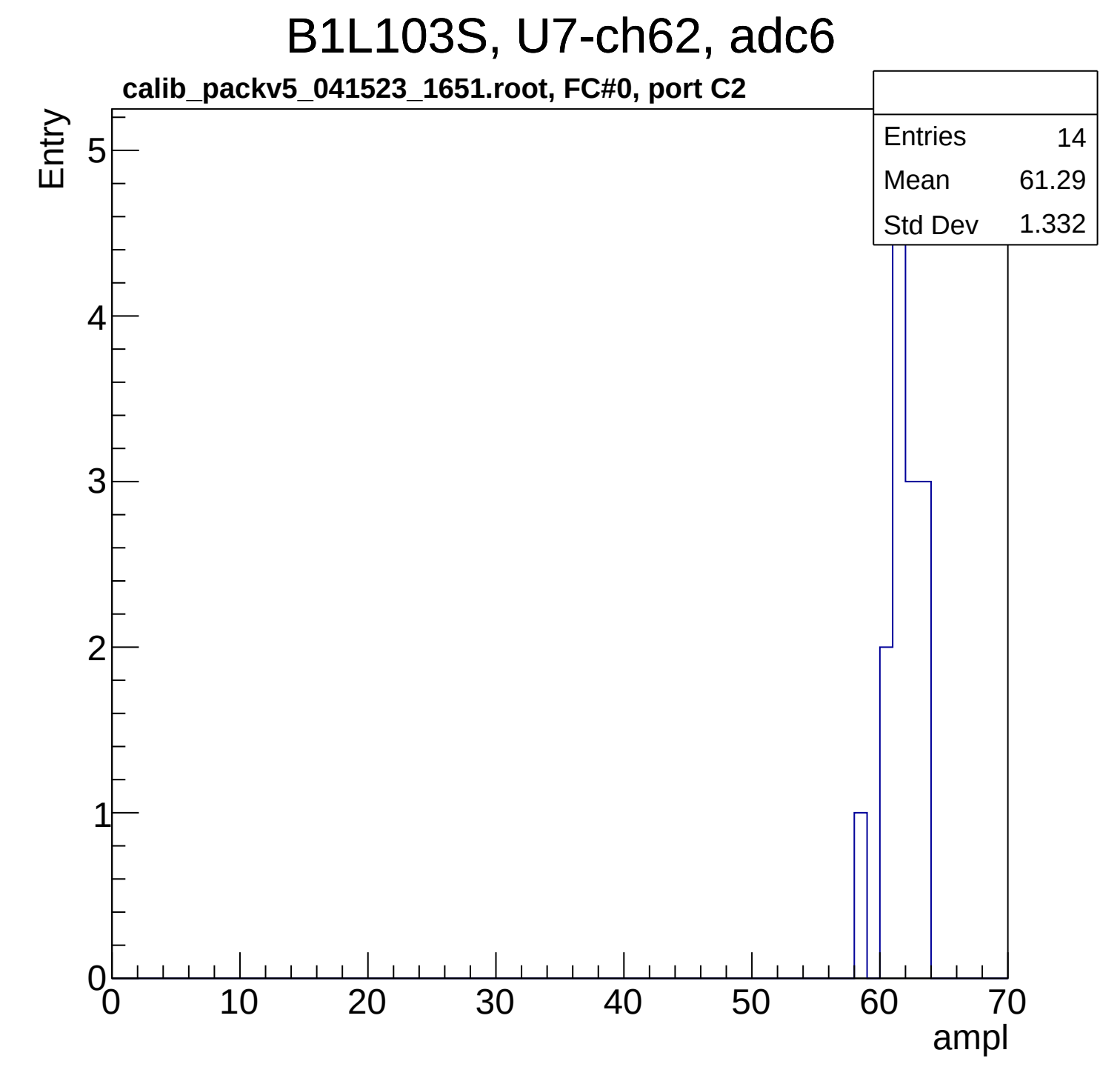
B1L103S, U7-ch62, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 14
Mean 61.29
Std Dev 1.332
Entry
ampl
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2
3
4
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0
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40
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60
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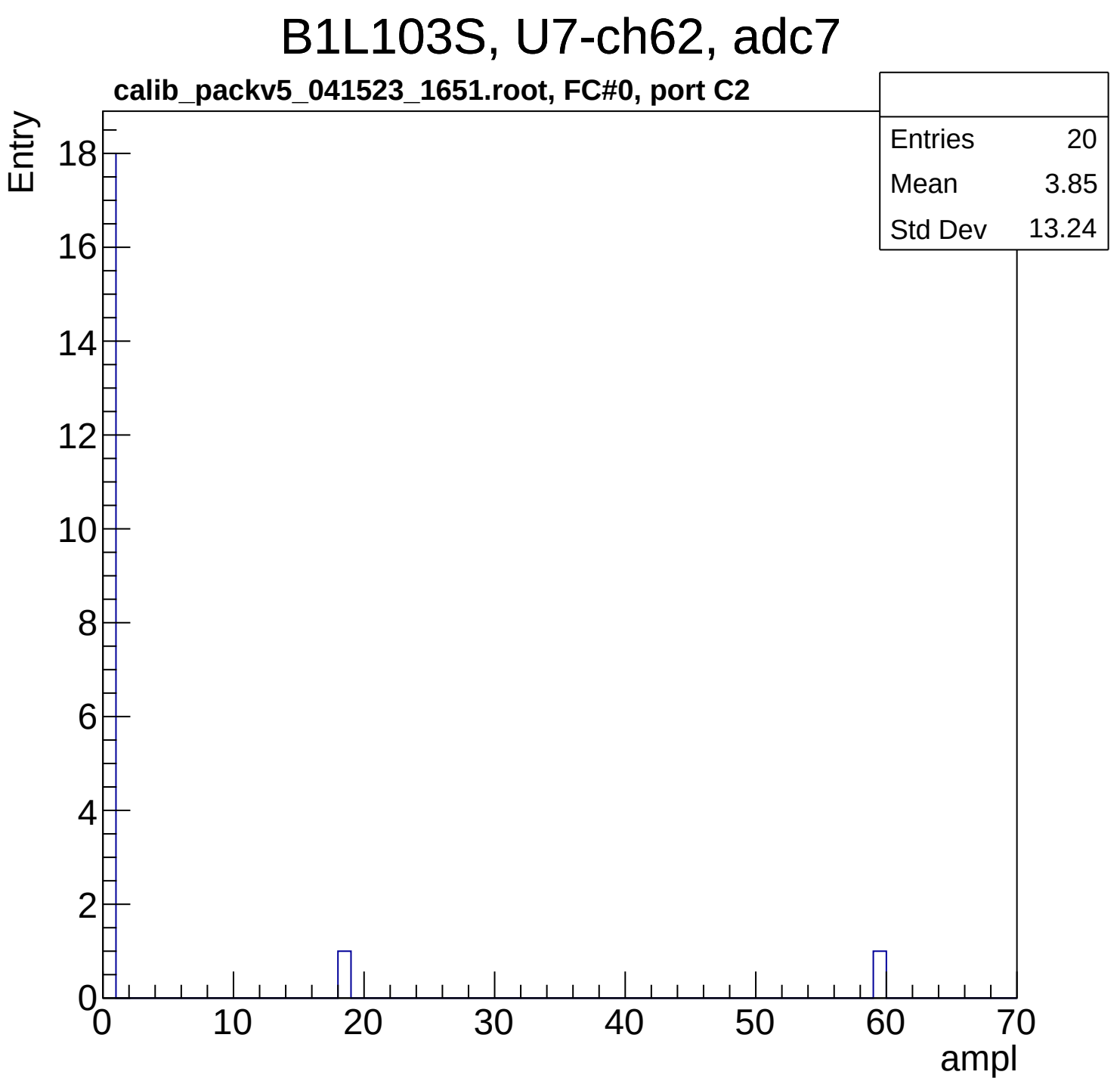
B1L103S, U7-ch62, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.85
Std Dev 13.24
Entry
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6
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10
12
14
16
18
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10
20
30
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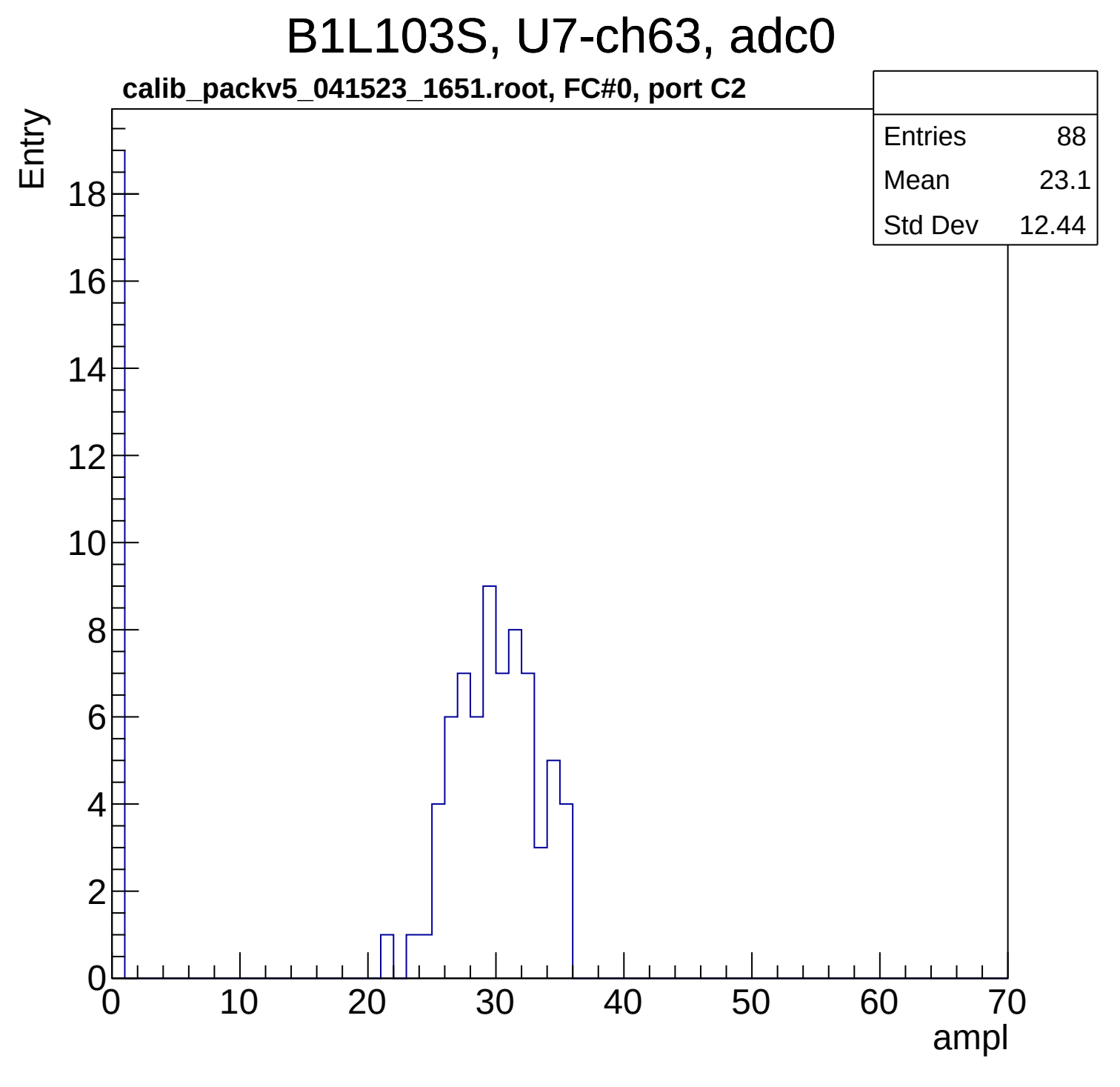
50
60
70
ampl


B1L103S, U7-ch63, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 88
Mean 23.1
Std Dev 12.44
Entry
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8
10
12
14
16
18
0
10
20
30
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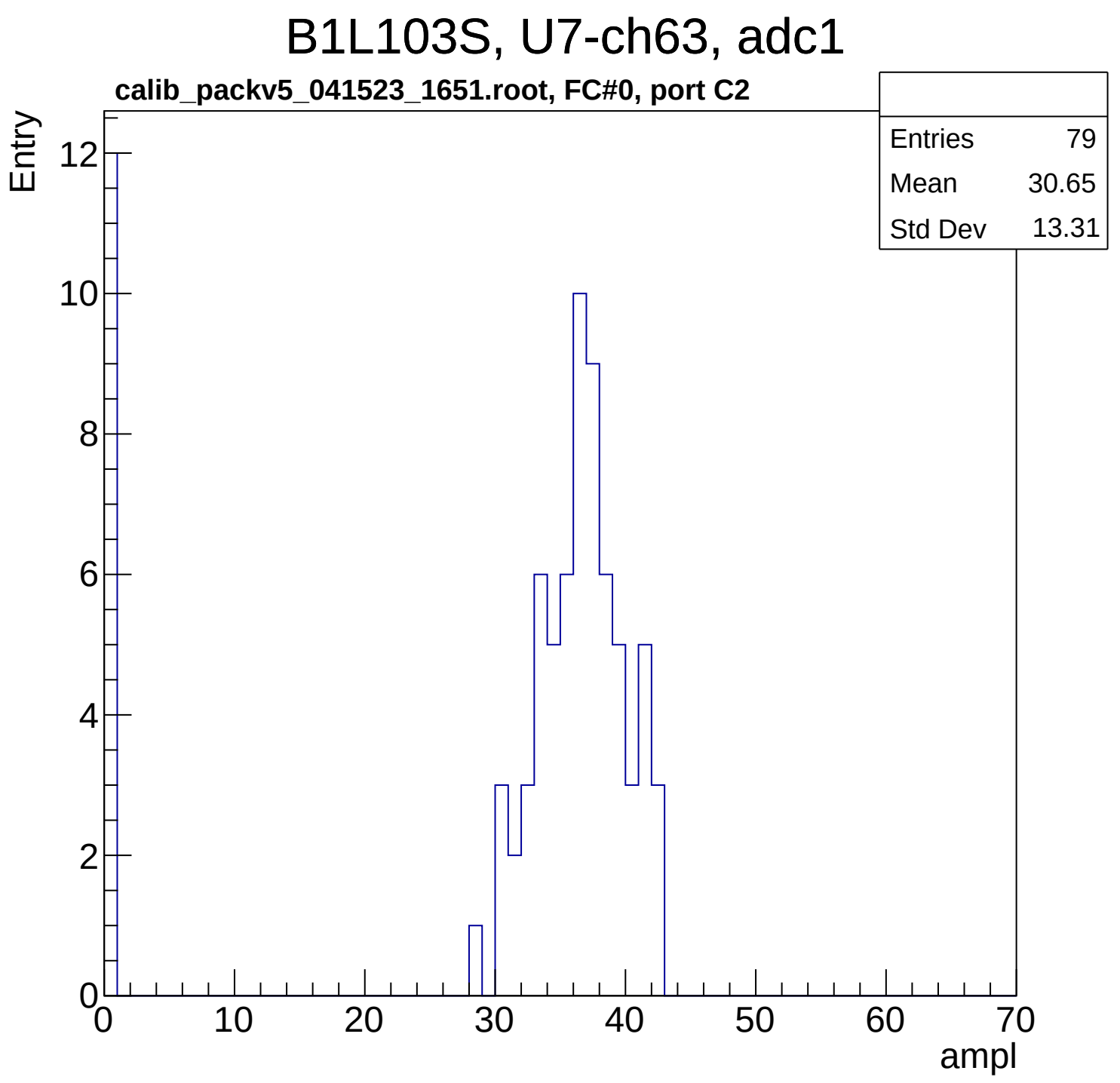
50
60
70
ampl


B1L103S, U7-ch63, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 30.65
Std Dev 13.31
Entry
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8
10
12
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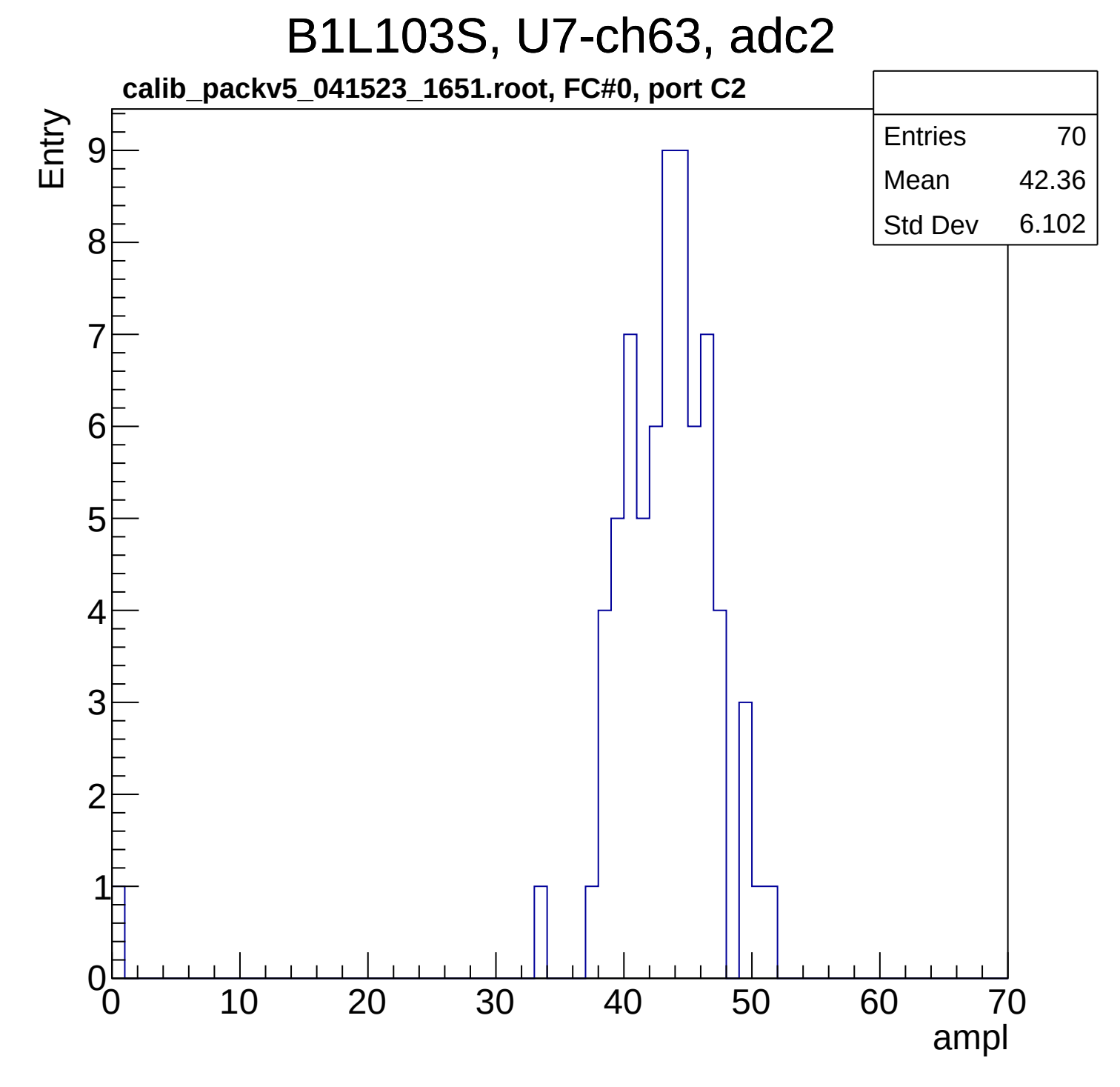
70
ampl


B1L103S, U7-ch63, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 42.36
Std Dev 6.102
Entry
ampl
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3
4
5
6
7
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60
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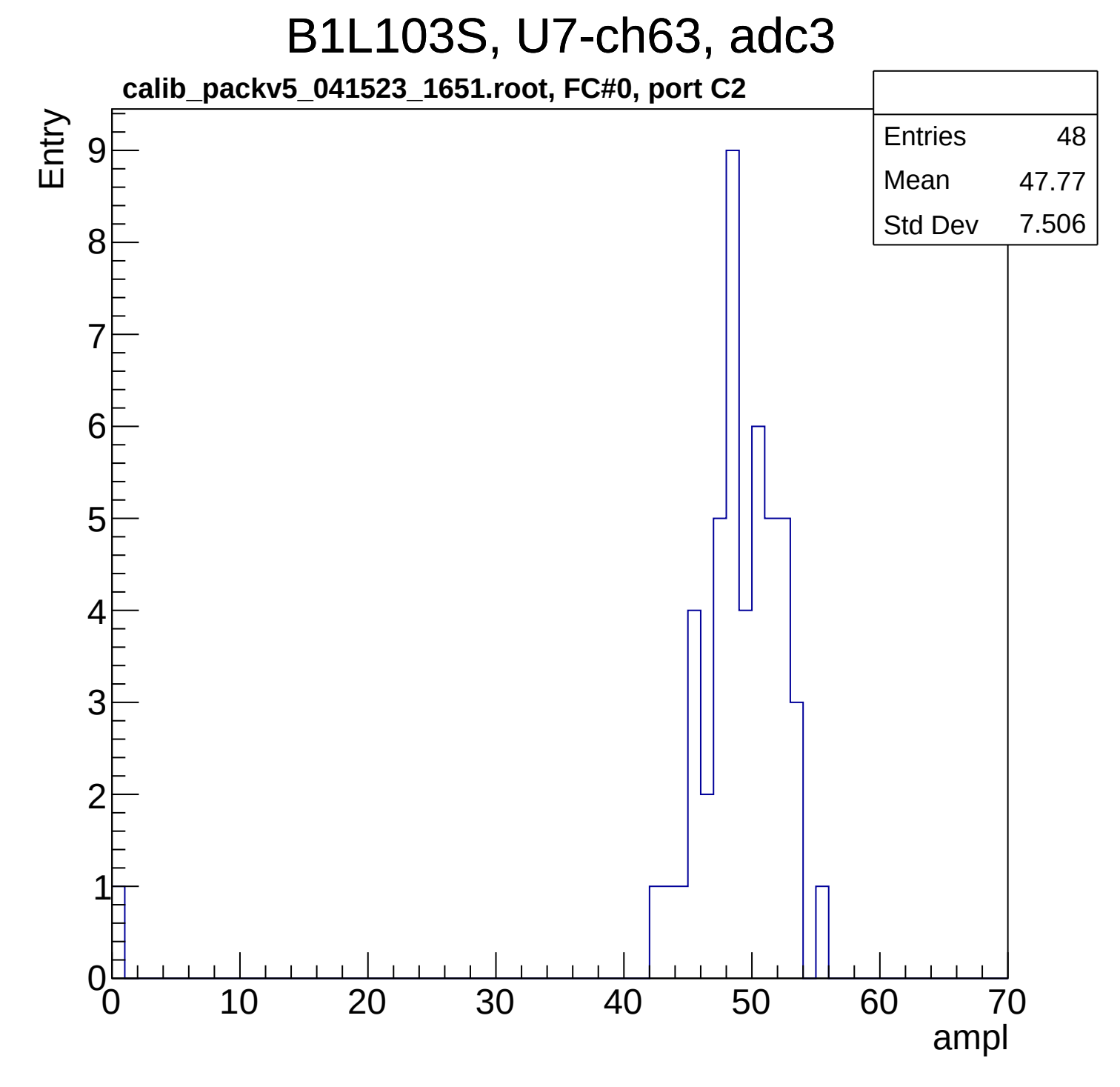
B1L103S, U7-ch63, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 47.77
Std Dev 7.506
Entry
ampl
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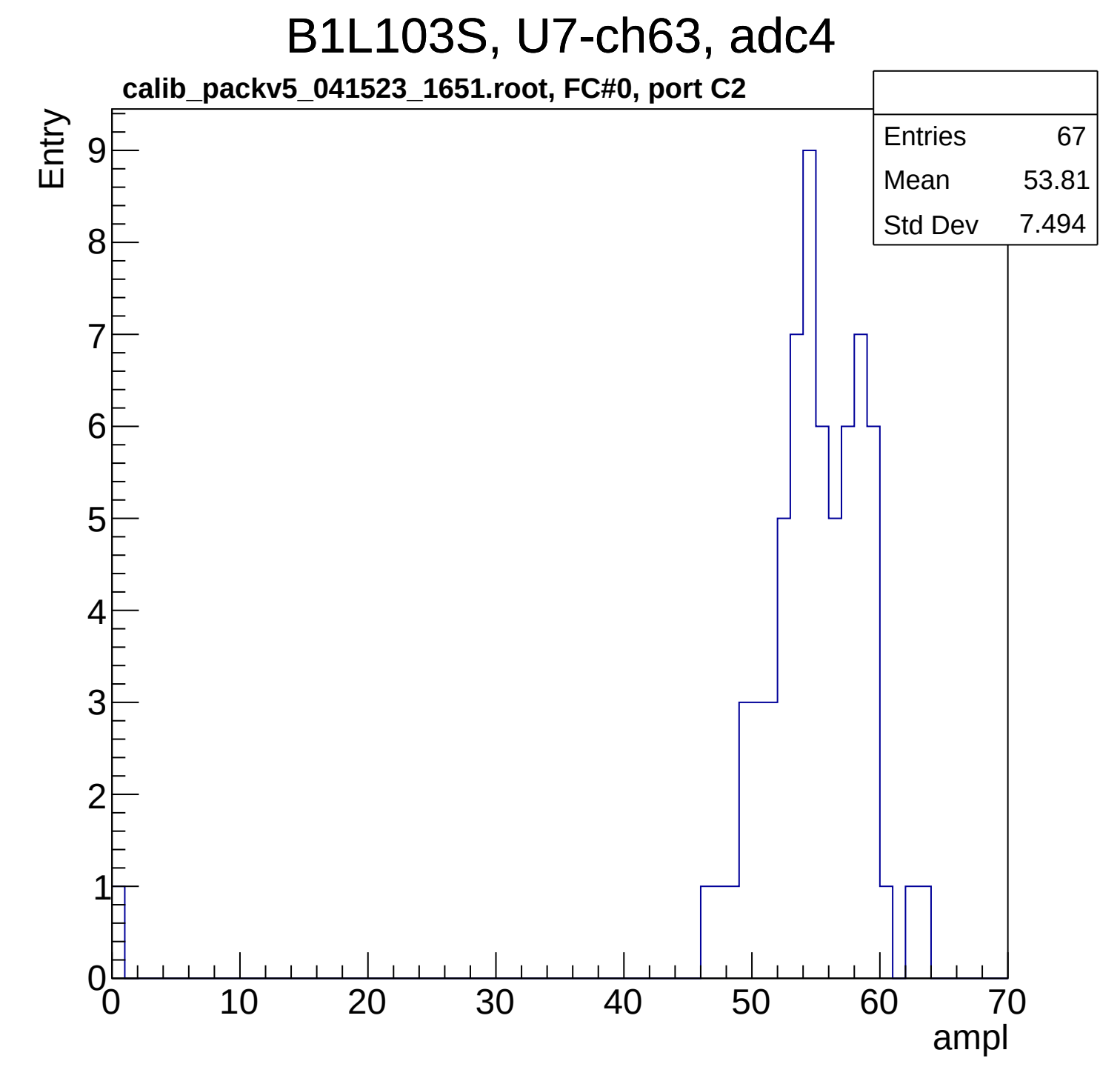
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U7-ch63, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 53.81
Std Dev 7.494
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
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60
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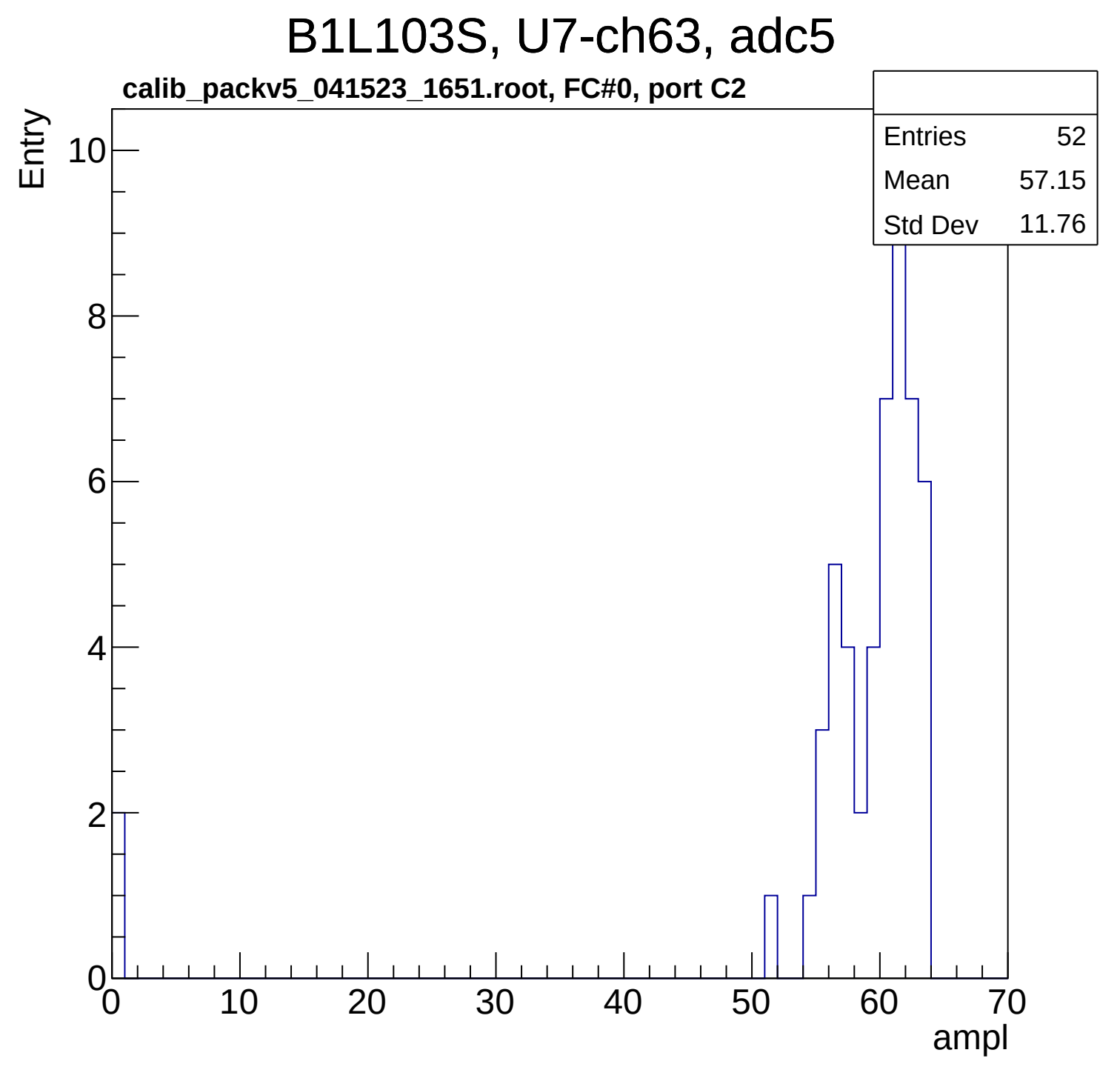
B1L103S, U7-ch63, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 57.15
Std Dev 11.76
Entry
0
2
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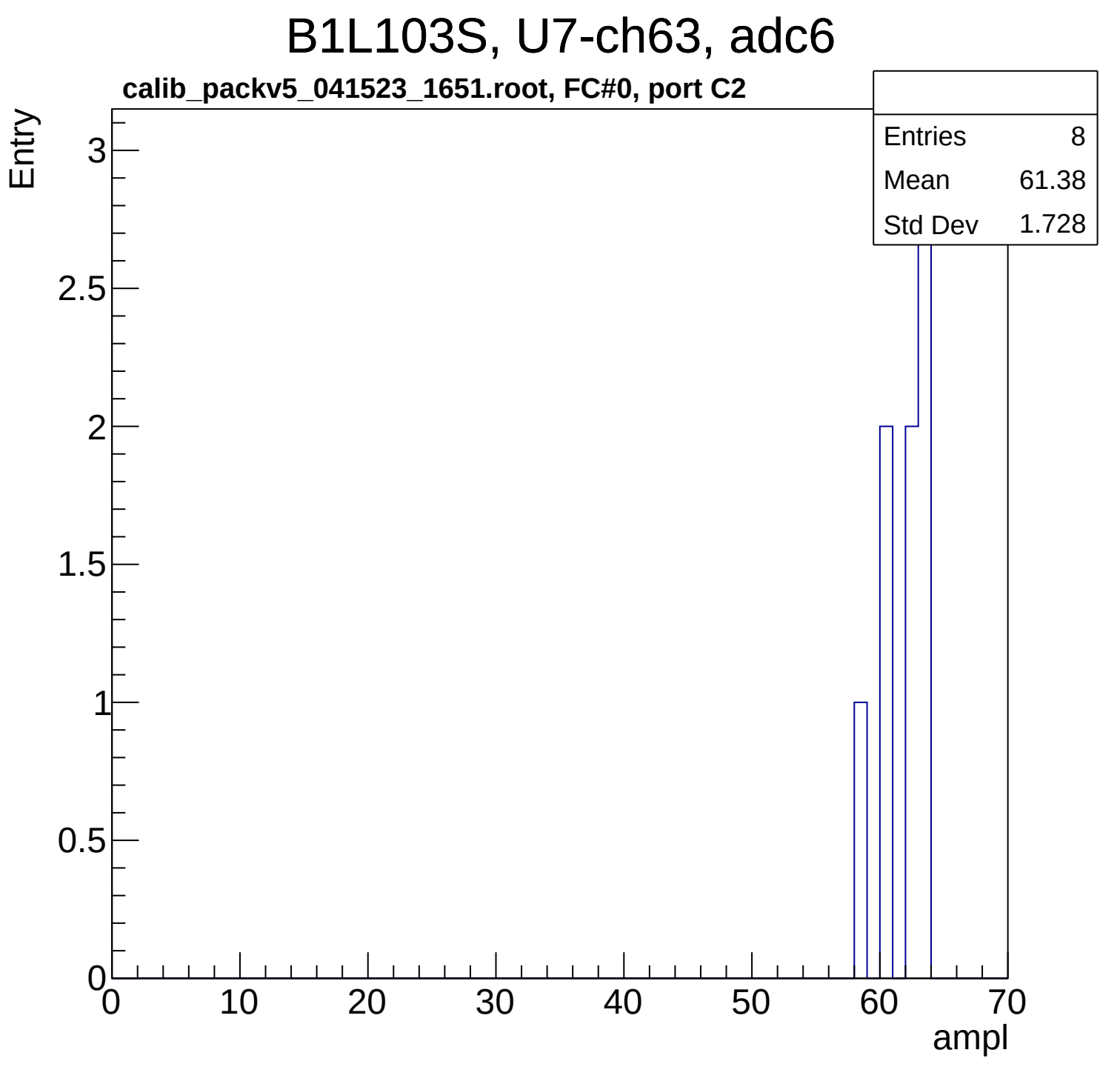
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch63, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 61.38
Std Dev 1.728
Entry
ampl
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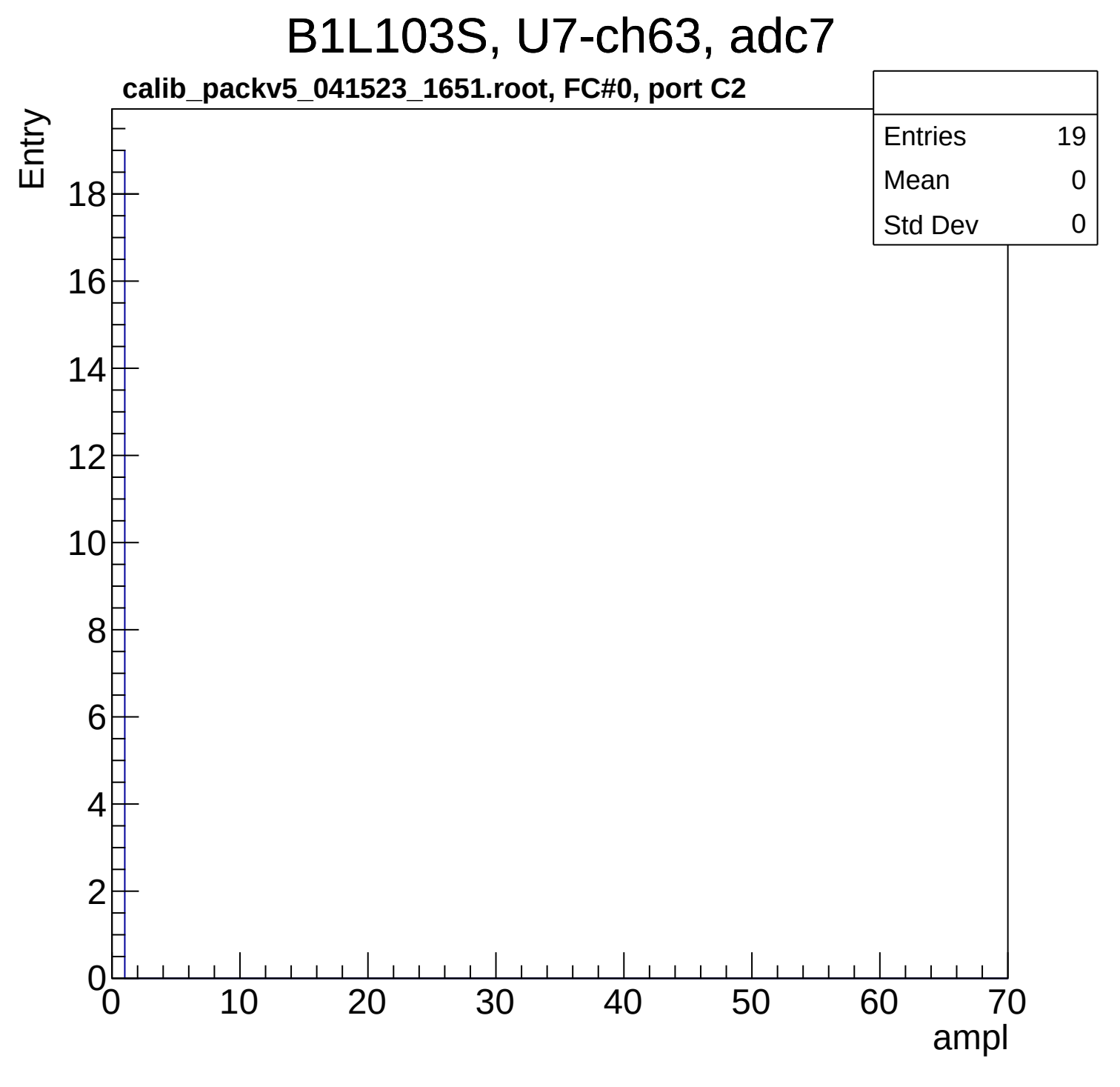
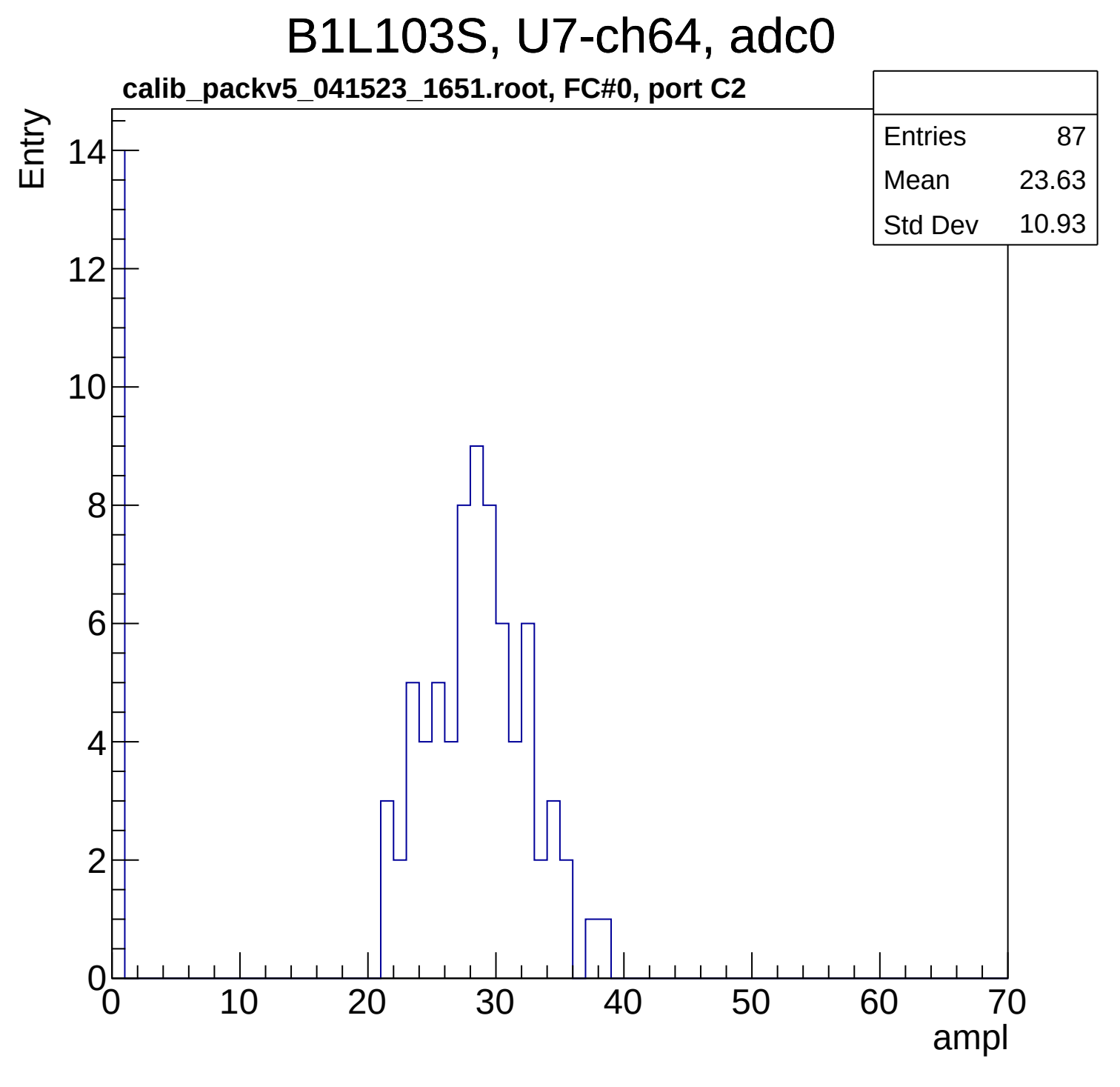
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U7-ch63, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch64, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 87
Mean 23.63
Std Dev 10.93
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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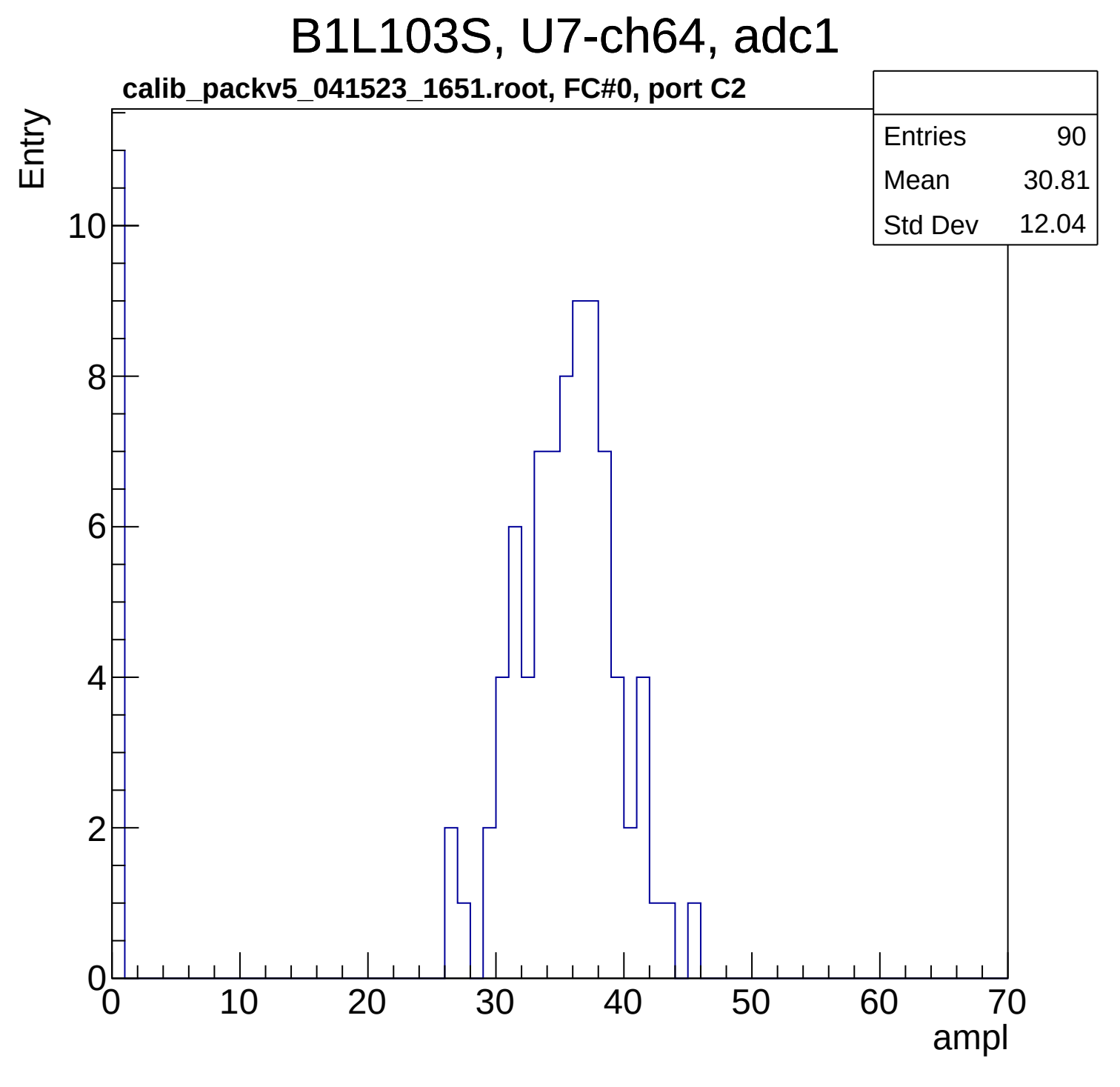
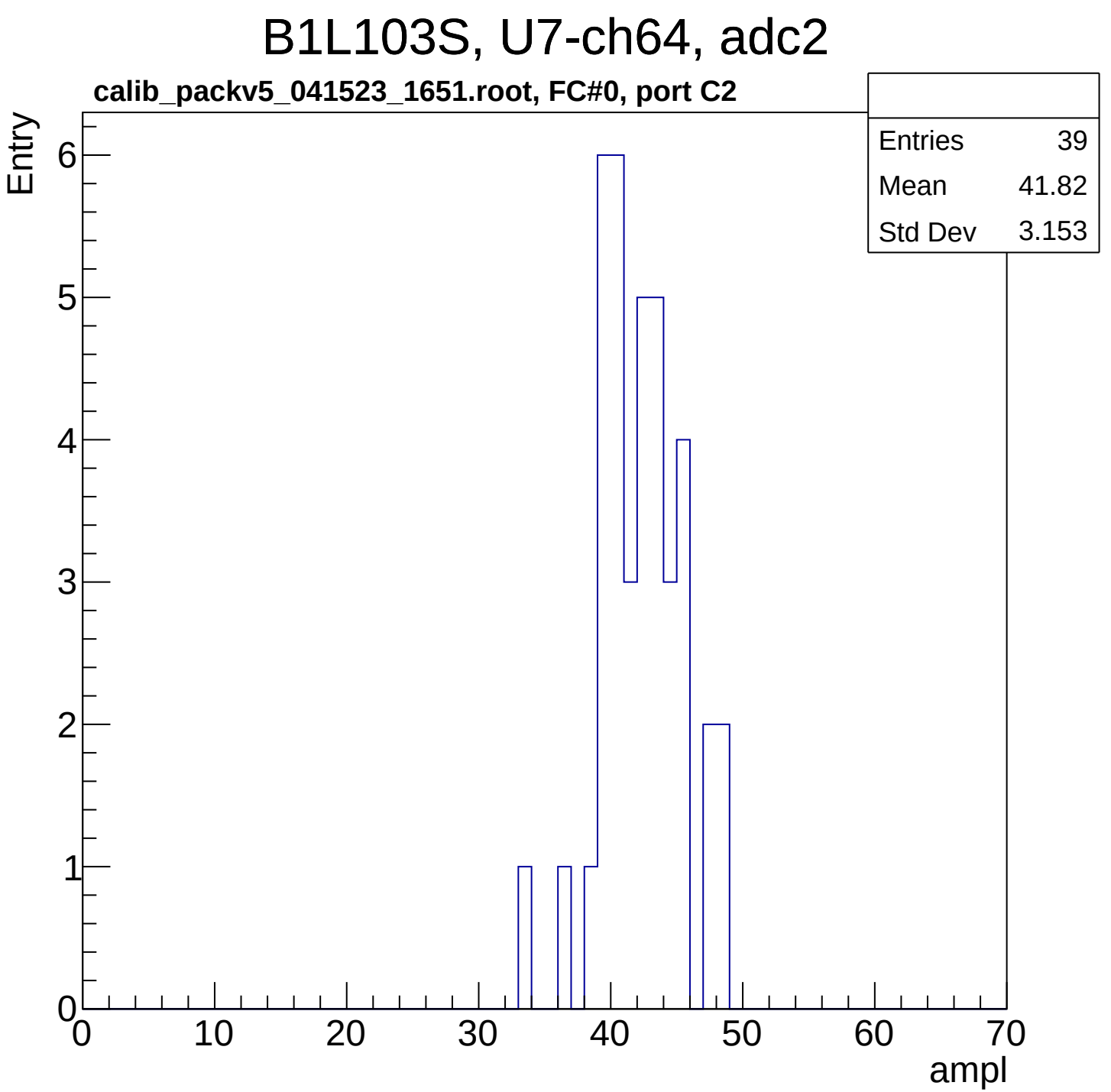
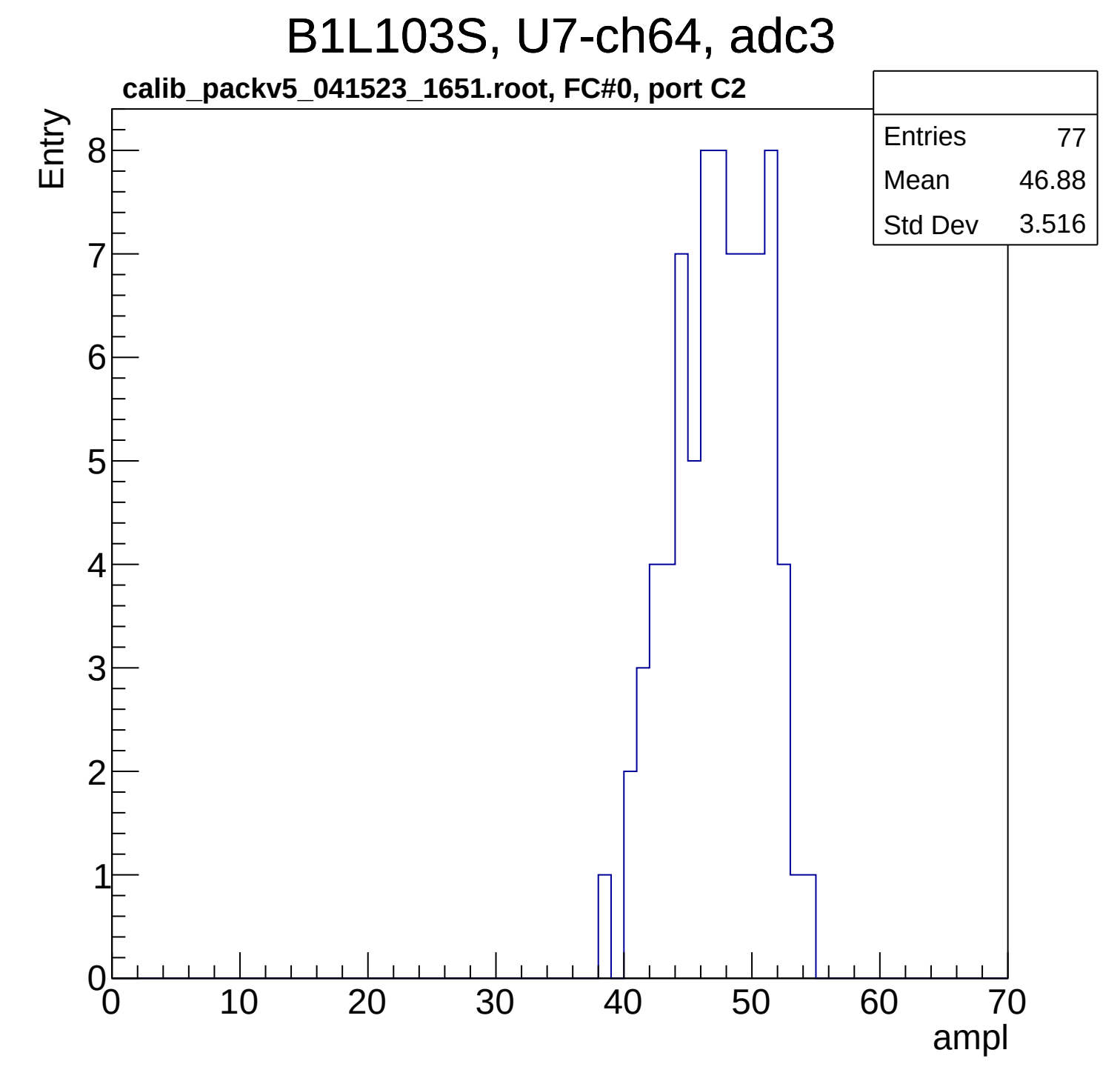

B1L103S, U7-ch64, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 90
Mean 30.81
Std Dev 12.04
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch64, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 39
Mean 41.82
Std Dev 3.153
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U7-ch64, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 46.88
Std Dev 3.516
Entry
ampl
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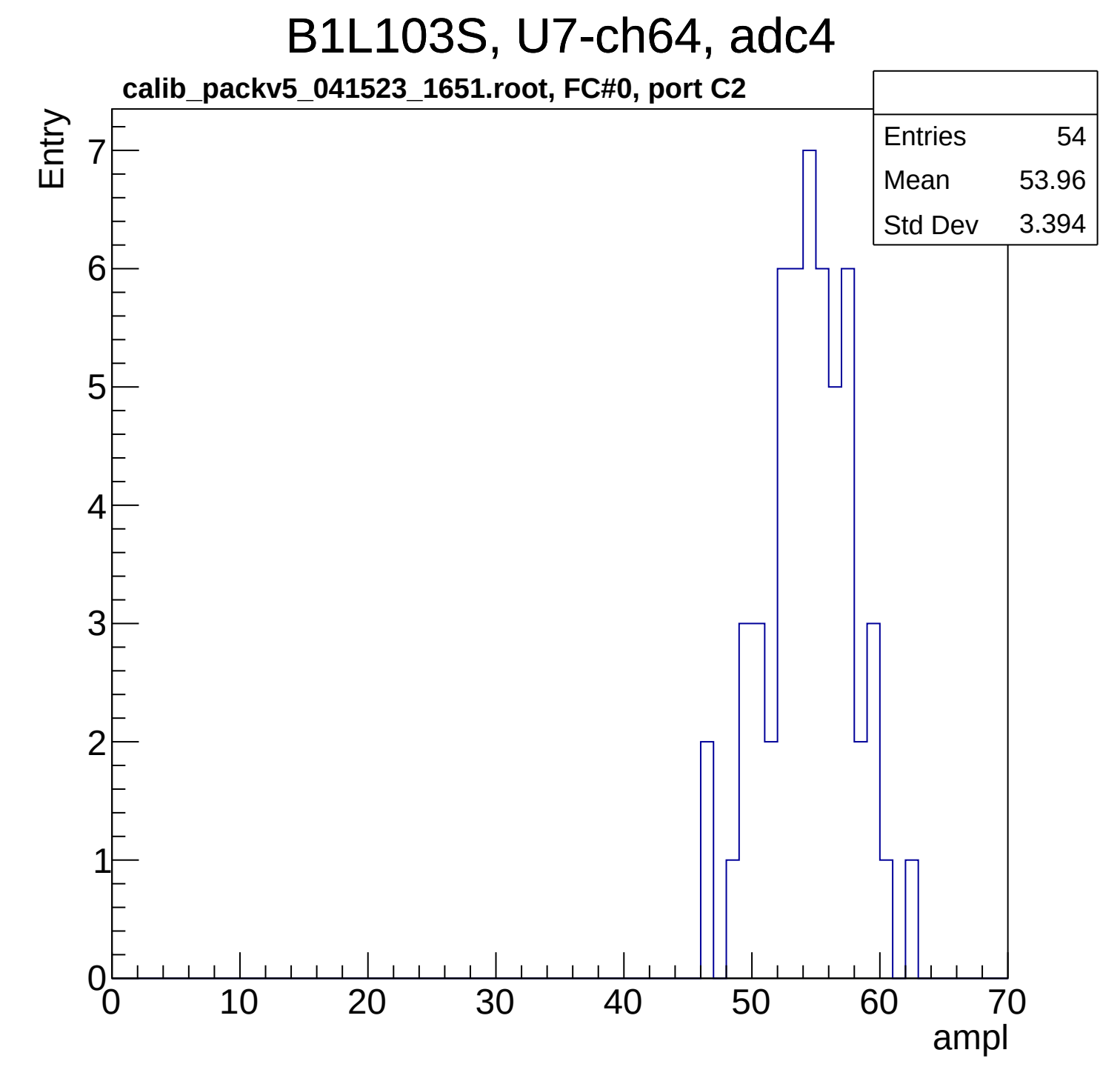
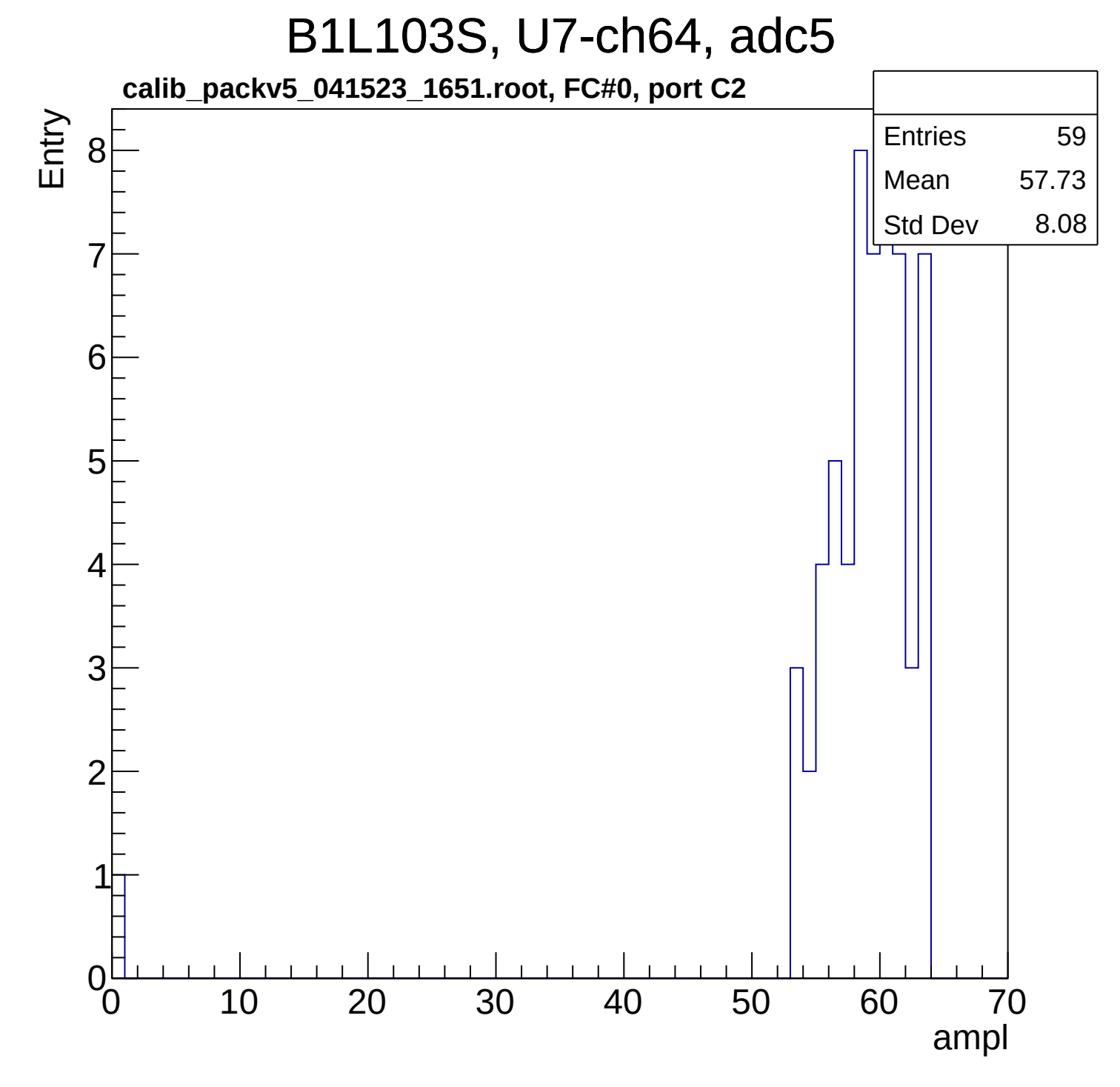
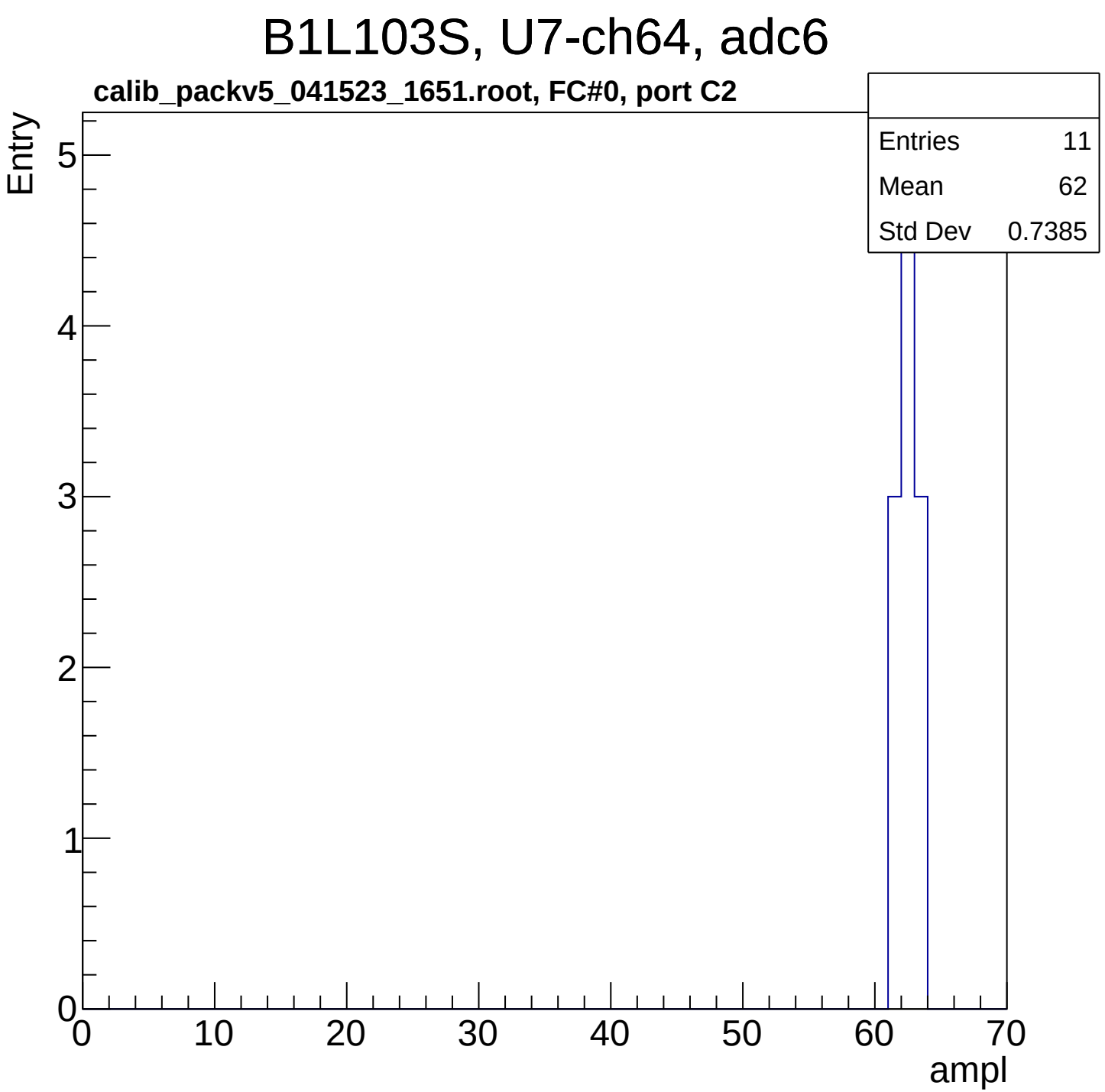
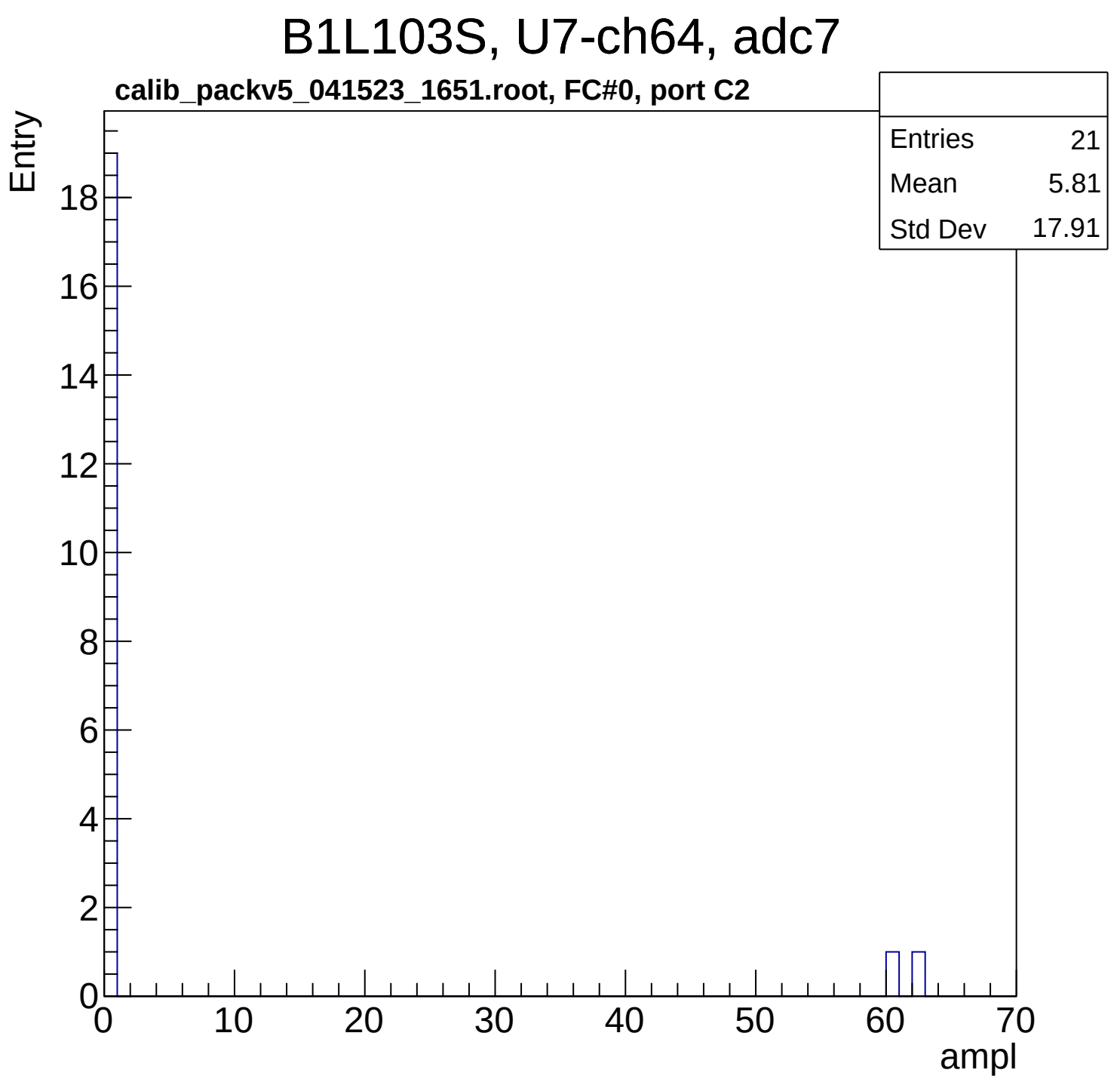
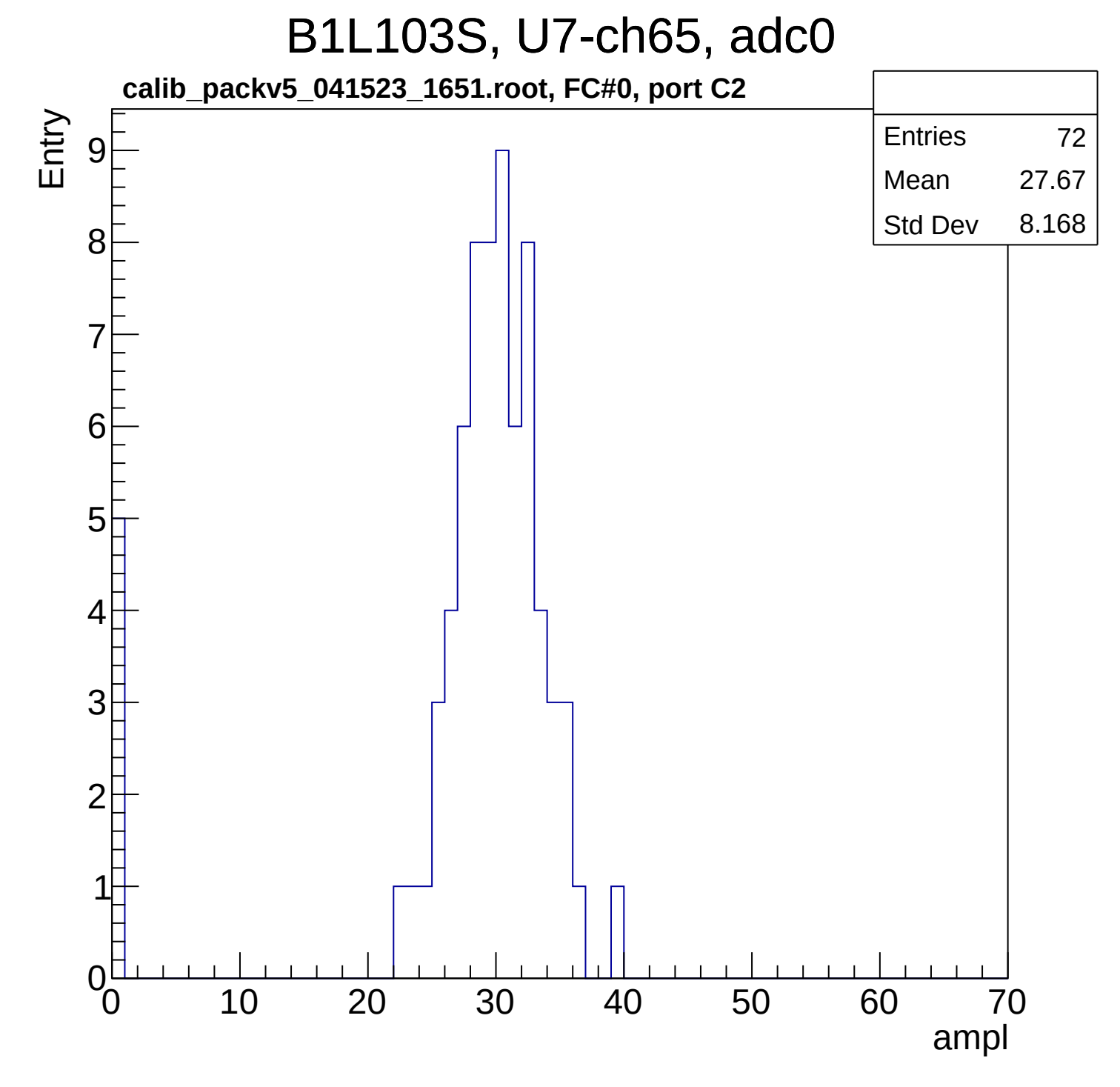
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch64, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 53.96
Std Dev 3.394
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U7-ch64, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 57.73
Std Dev 8.08
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch64, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 62
Std Dev 0.7385
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch64, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 5.81
Std Dev 17.91
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch65, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 27.67
Std Dev 8.168
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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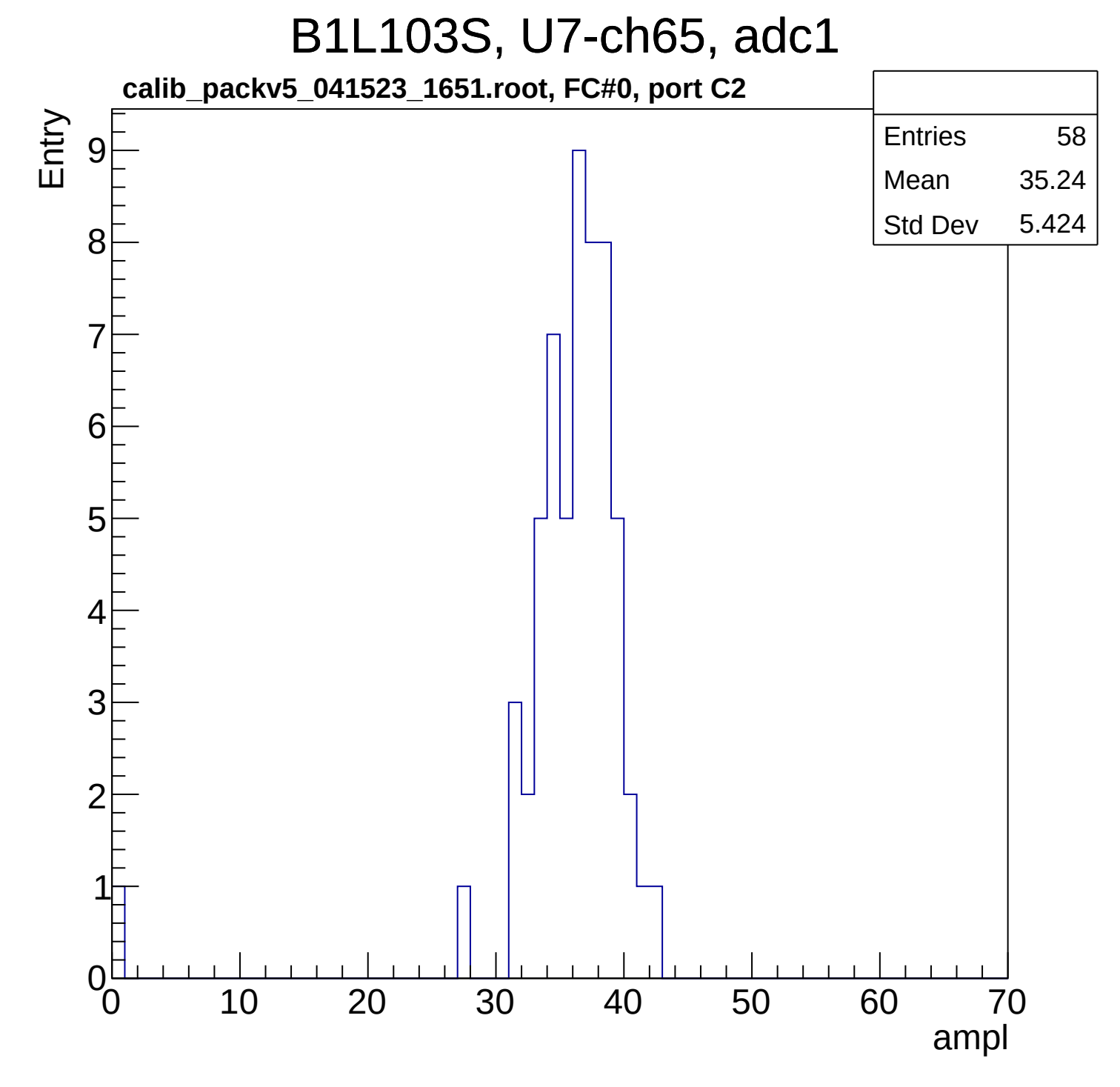
B1L103S, U7-ch65, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 35.24
Std Dev 5.424
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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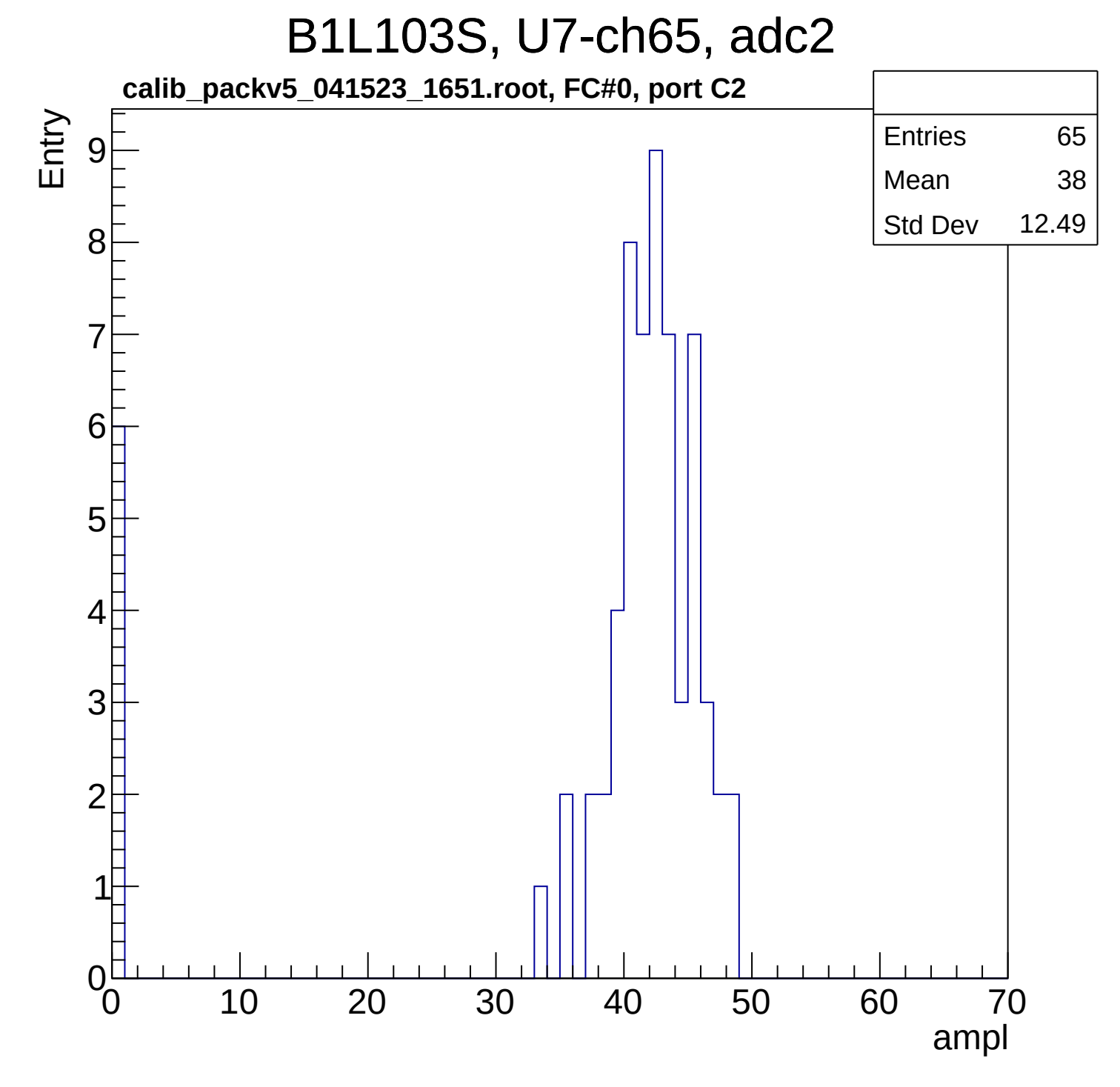
B1L103S, U7-ch65, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 38
Std Dev 12.49
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
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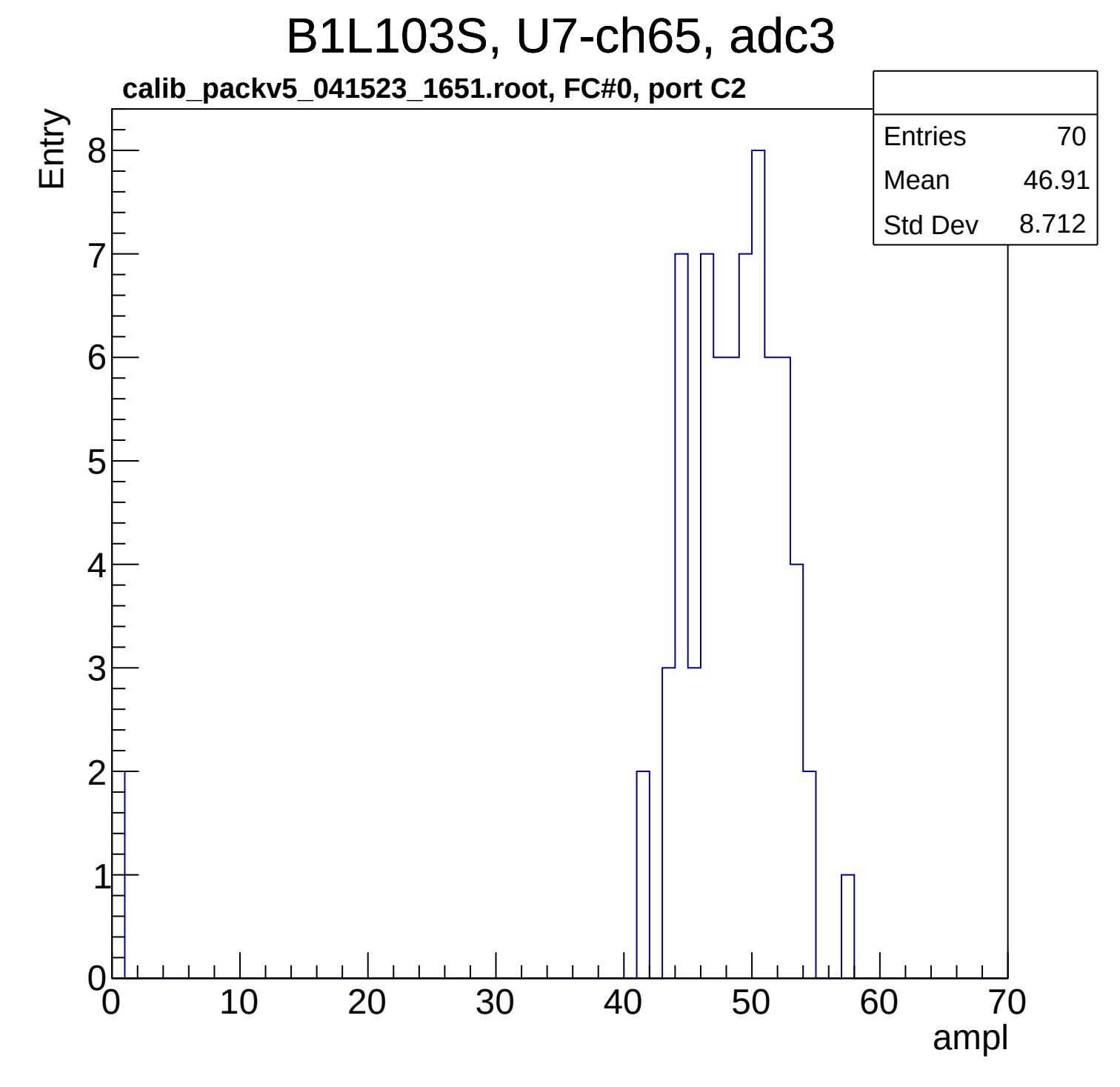
60
70


B1L103S, U7-ch65, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 46.91
Std Dev 8.712
Entry
ampl
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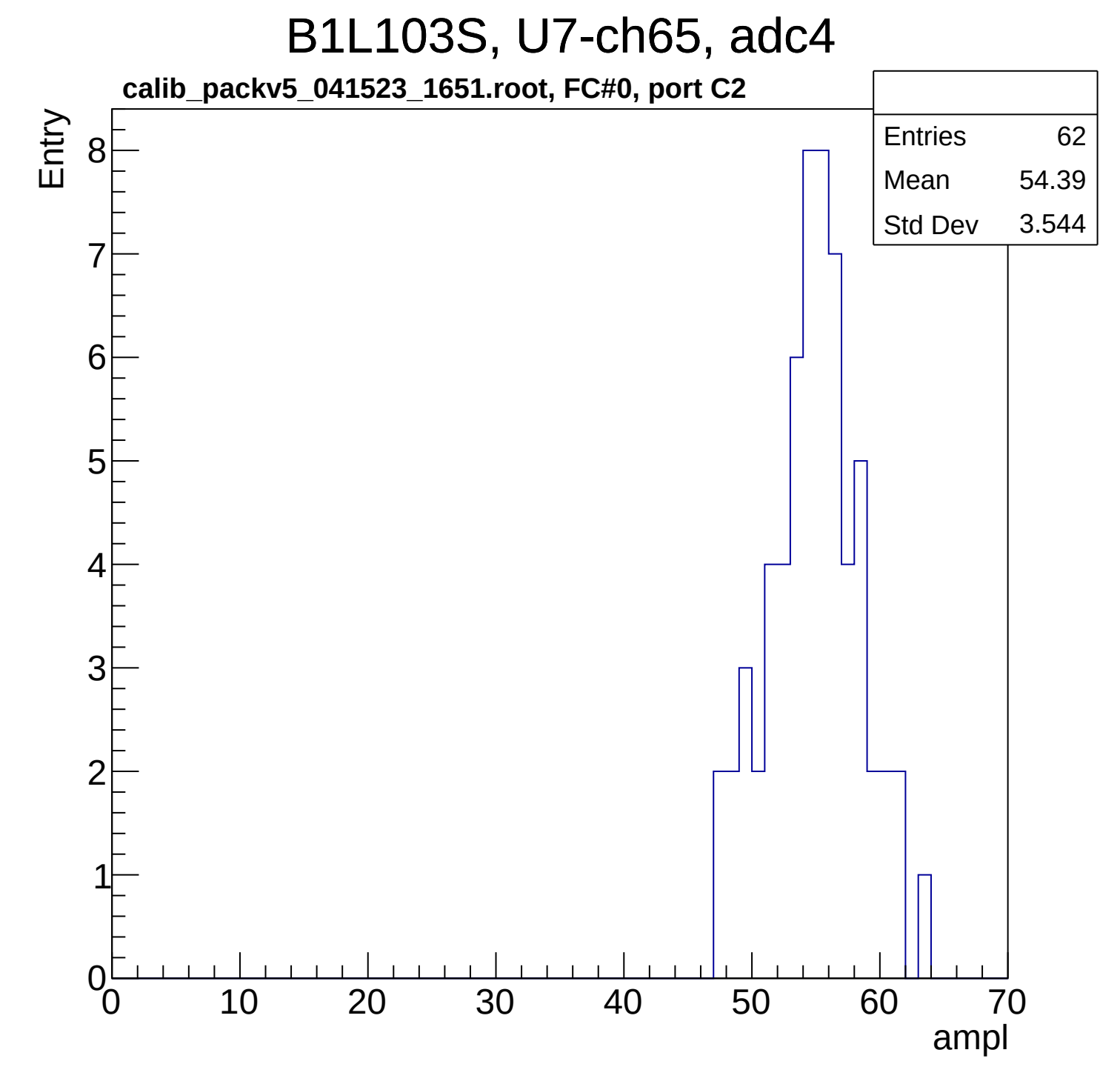
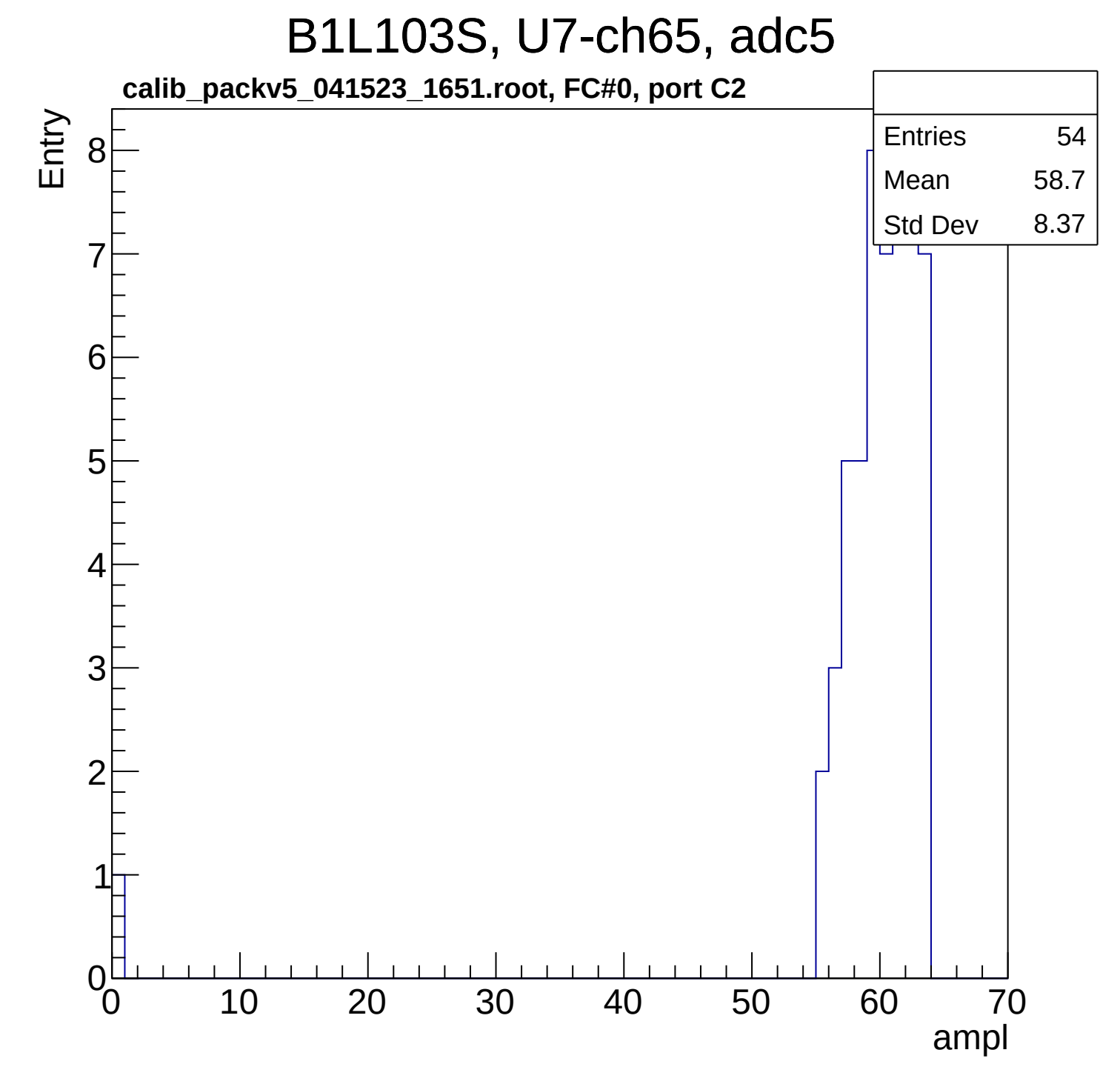
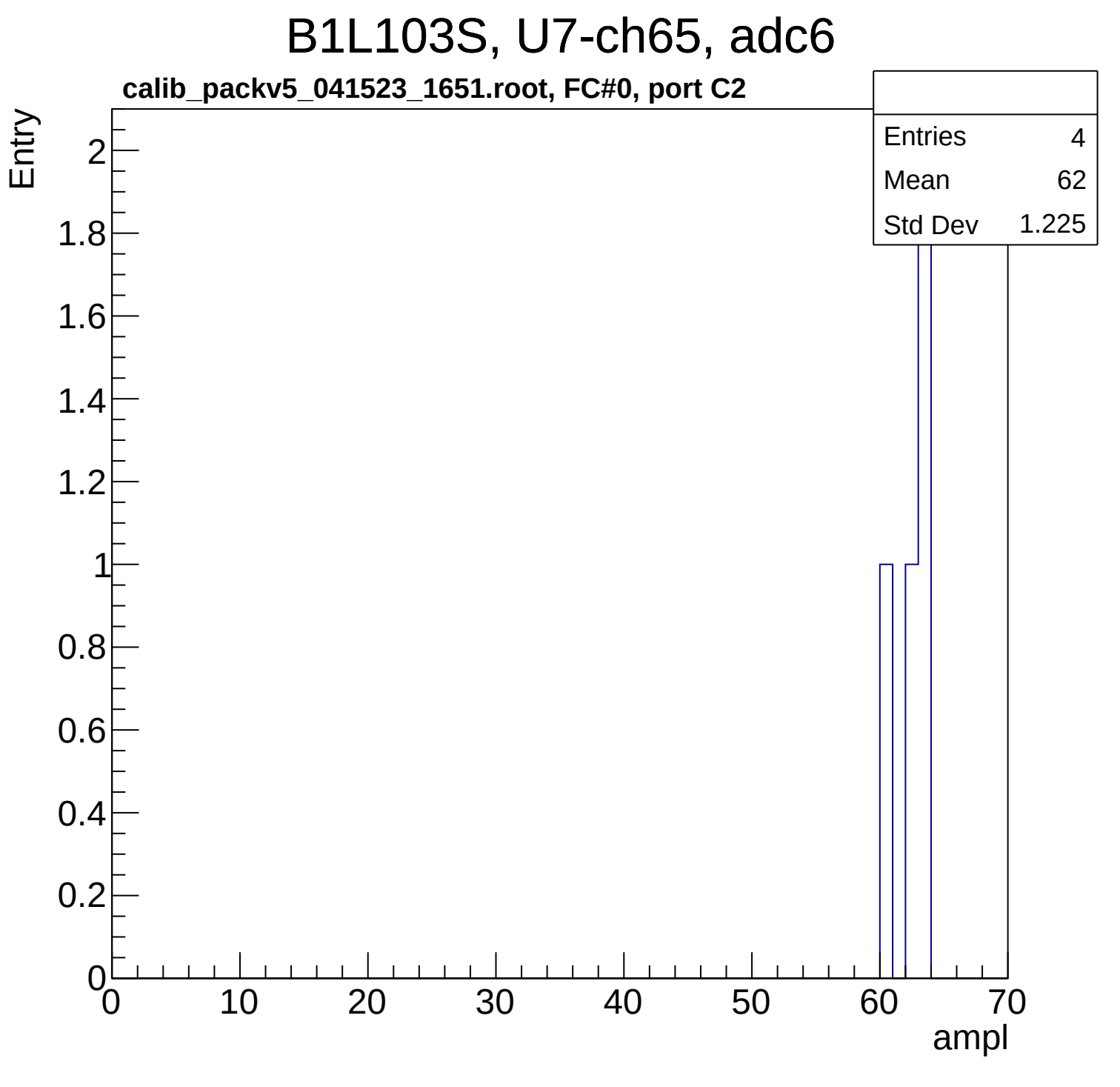
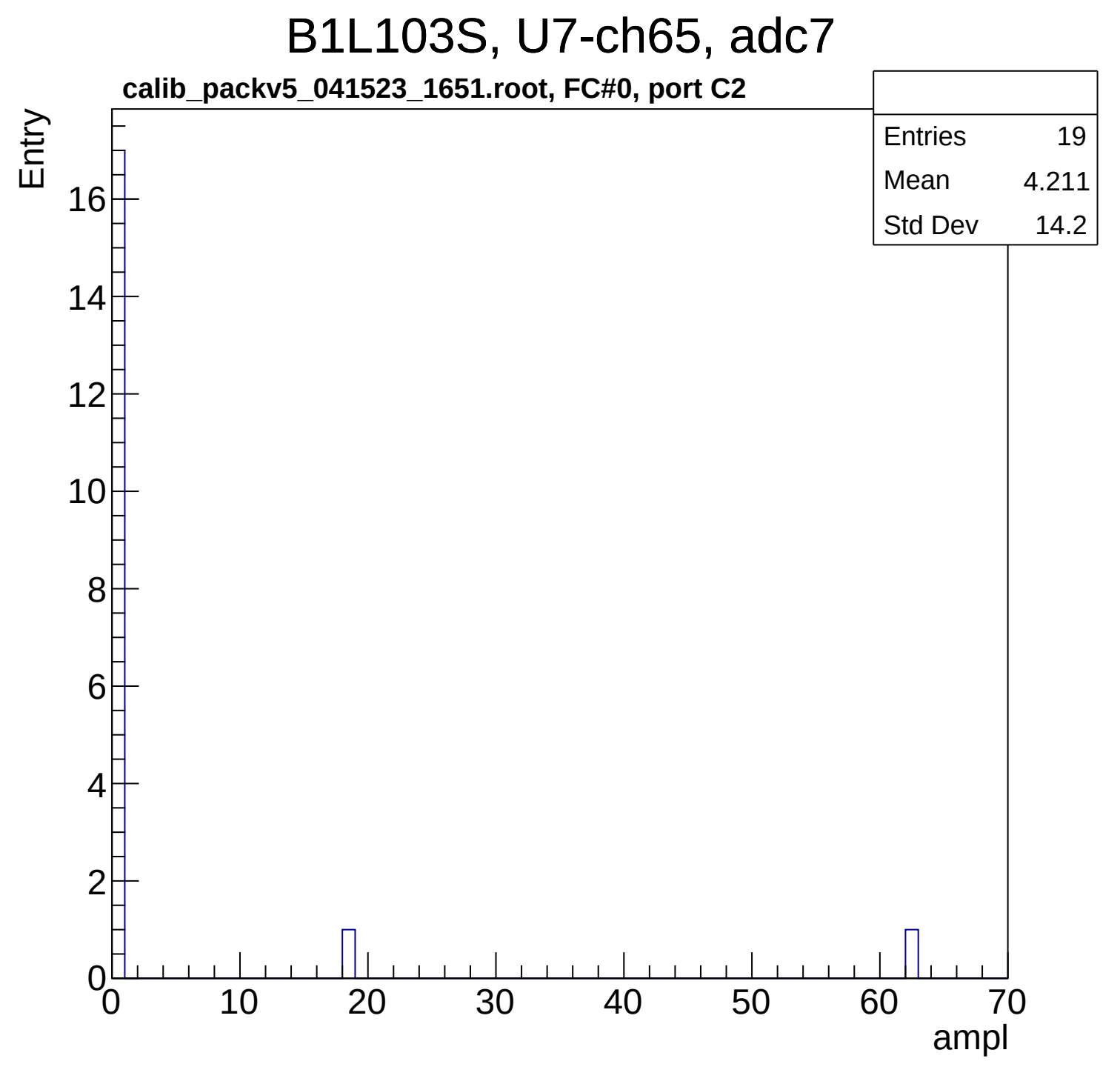
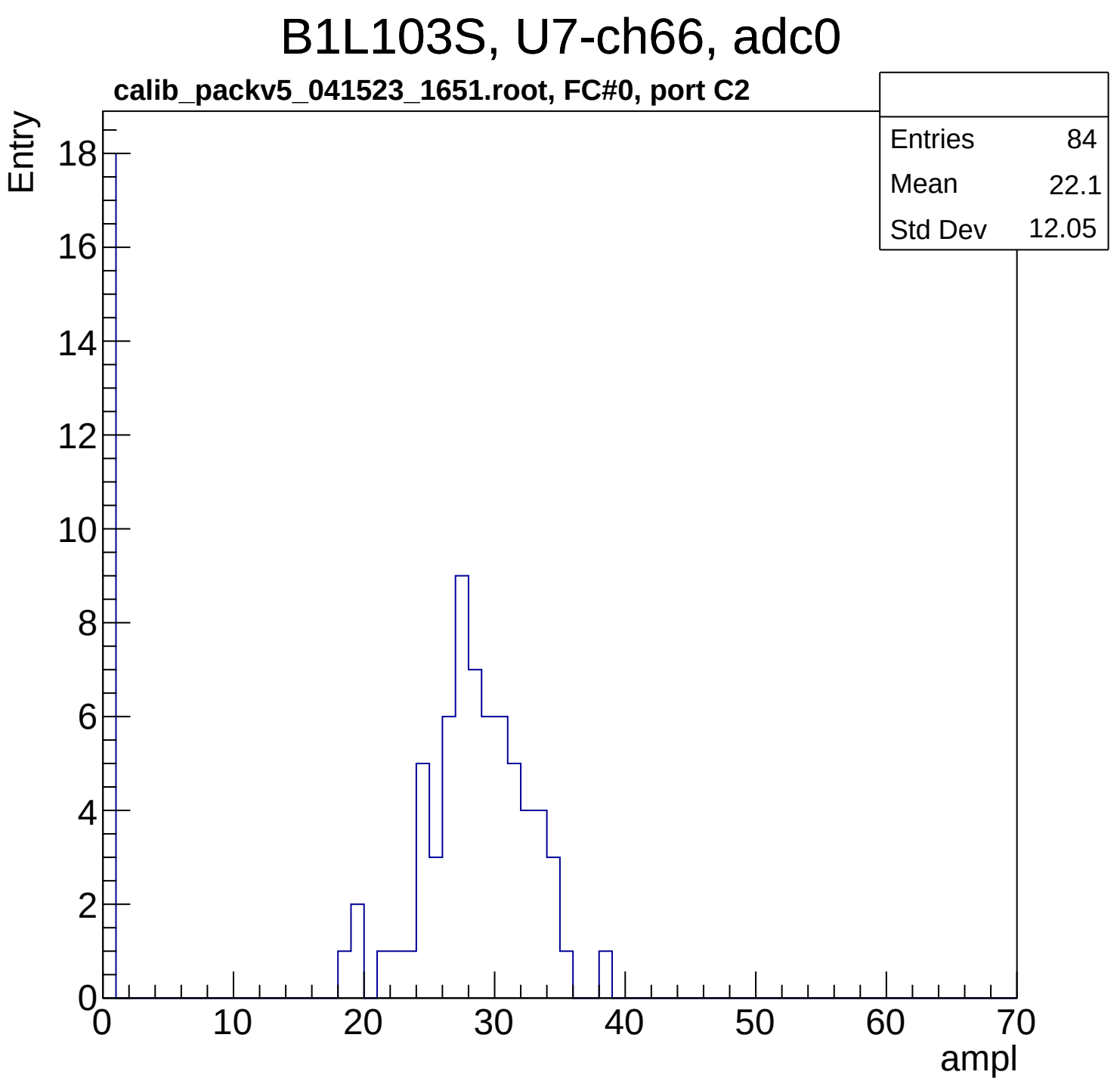
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch65, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 54.39
Std Dev 3.544
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch65, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 58.7
Std Dev 8.37
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch65, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 4
Mean 62
Std Dev 1.225
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U7-ch65, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 4.211
Std Dev 14.2
Entry
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch66, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 22.1
Std Dev 12.05
Entry
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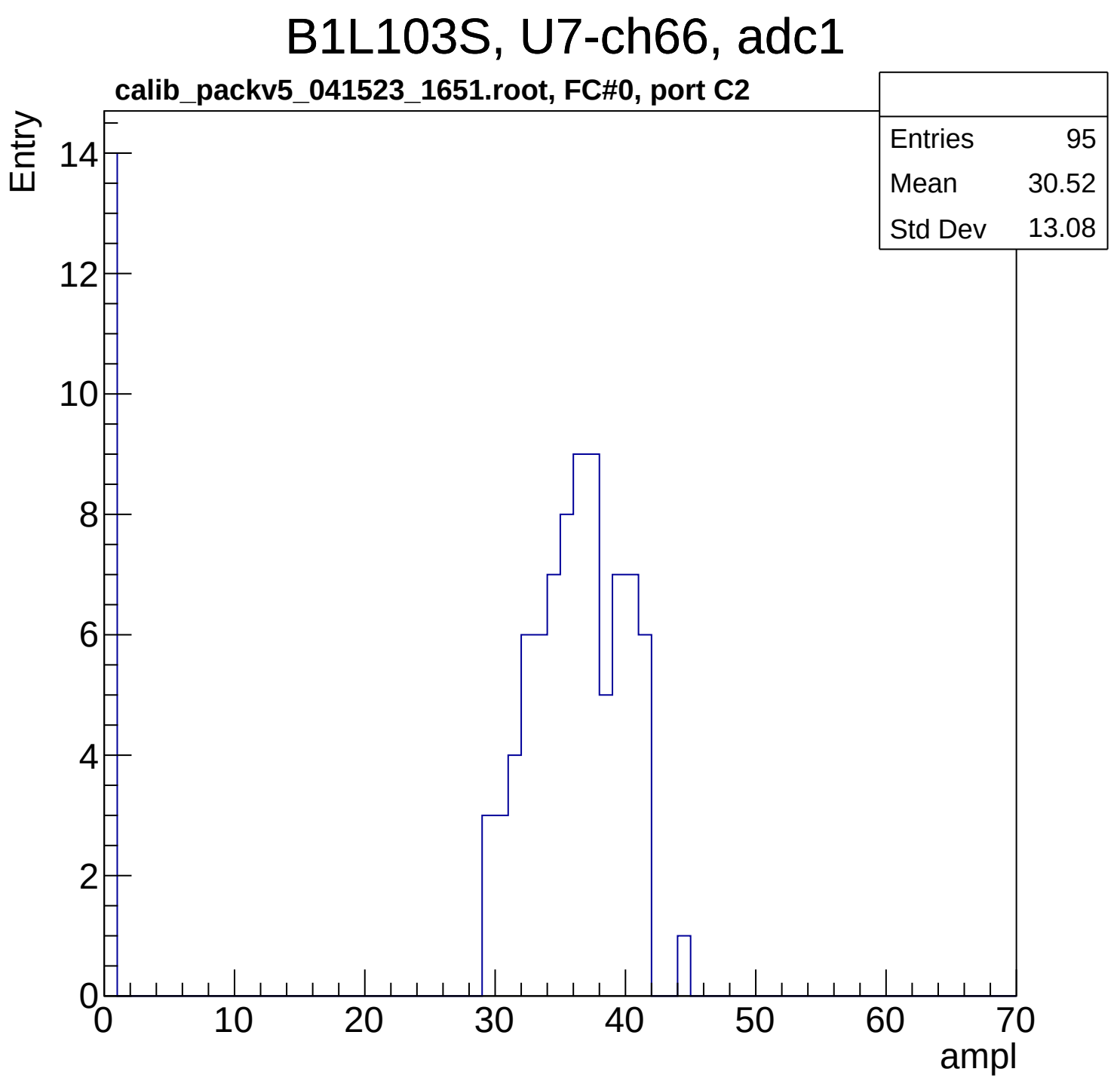
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch66, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 95
Mean 30.52
Std Dev 13.08
Entry
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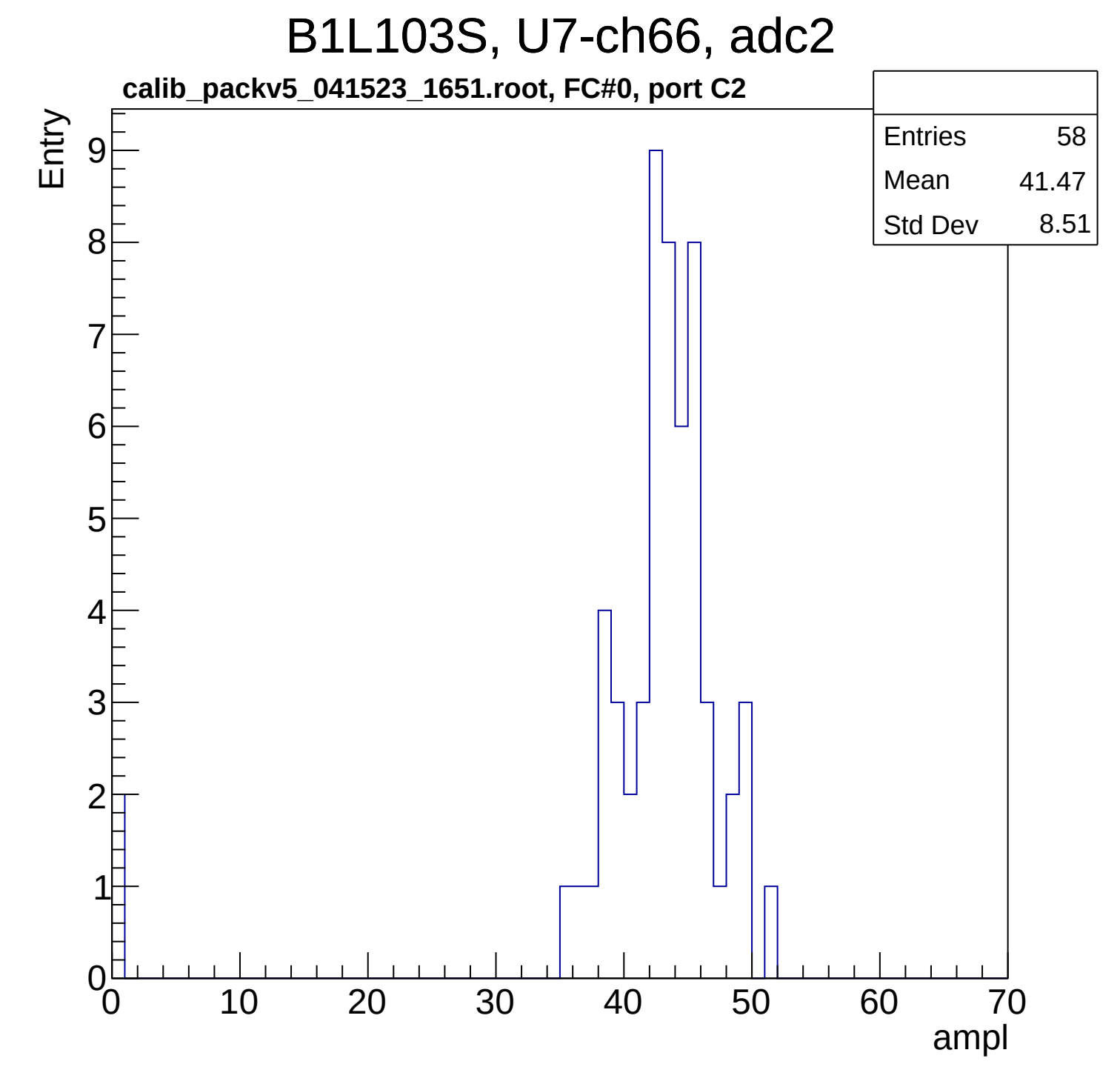
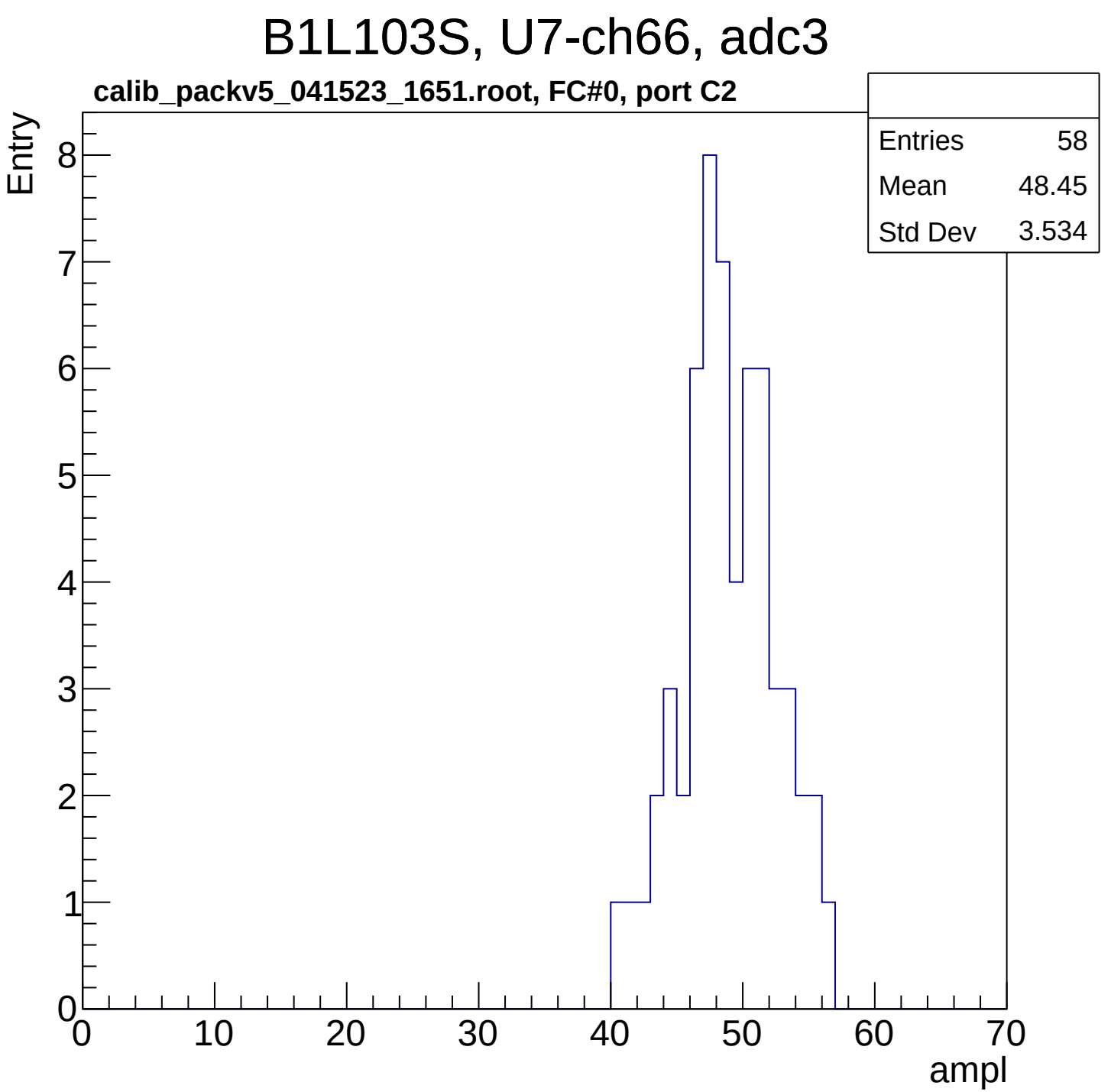
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch66, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 41.47
Std Dev 8.51
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U7-ch66, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 48.45
Std Dev 3.534
Entry
ampl
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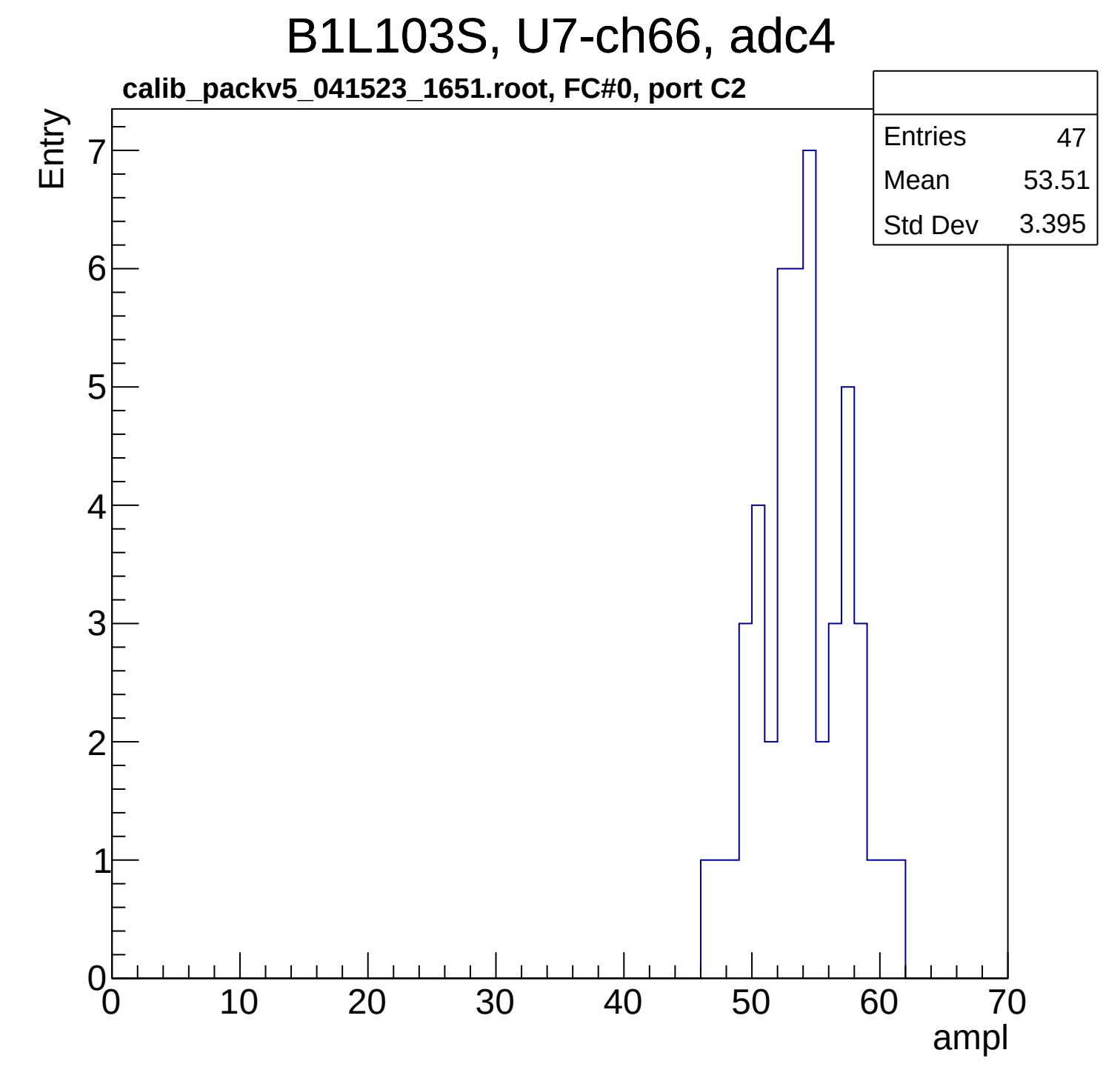
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch66, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 53.51
Std Dev 3.395
Entry
ampl
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2
3
4
5
6
7
0
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20
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60
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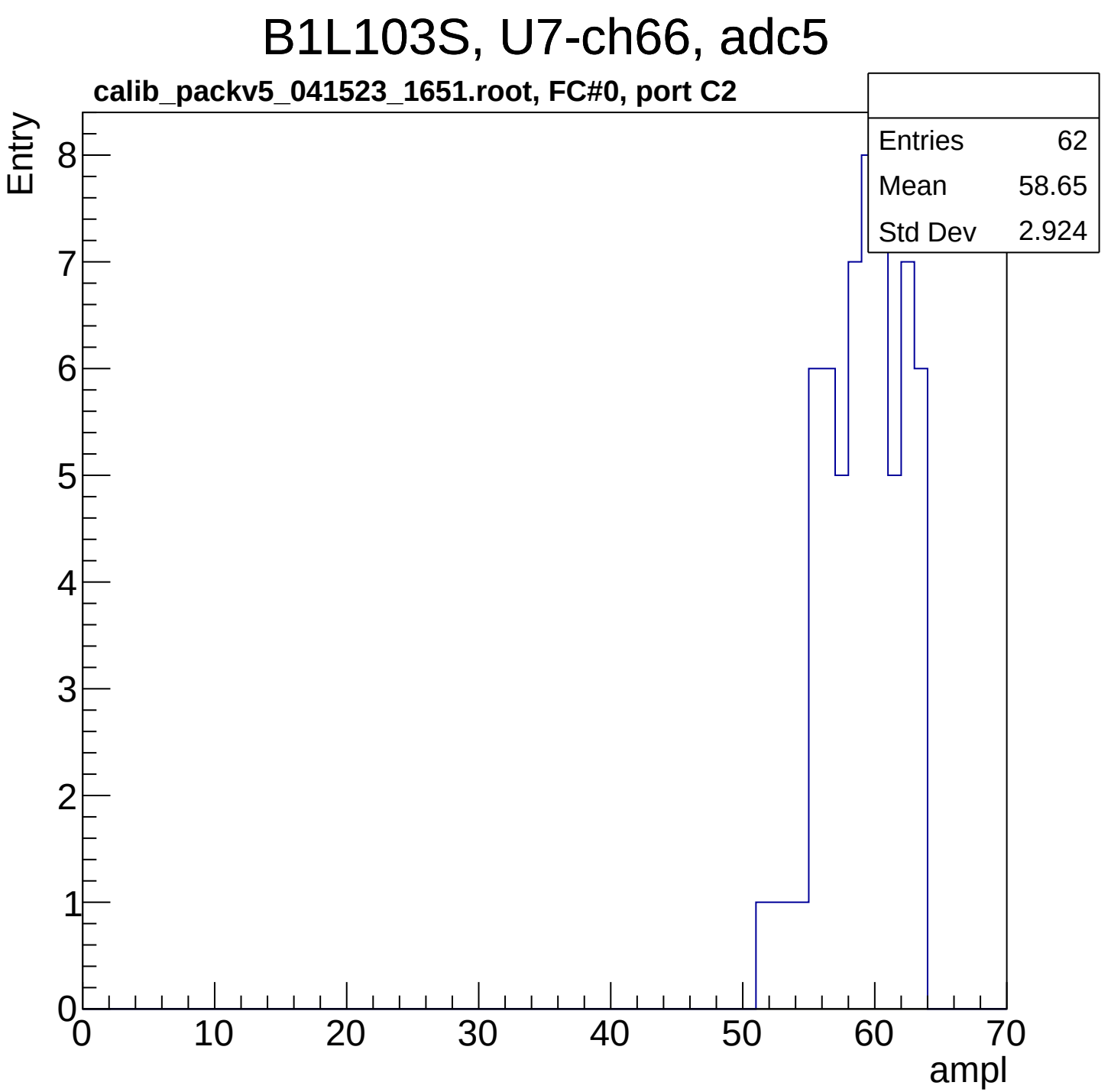
B1L103S, U7-ch66, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 58.65
Std Dev 2.924
Entry
ampl
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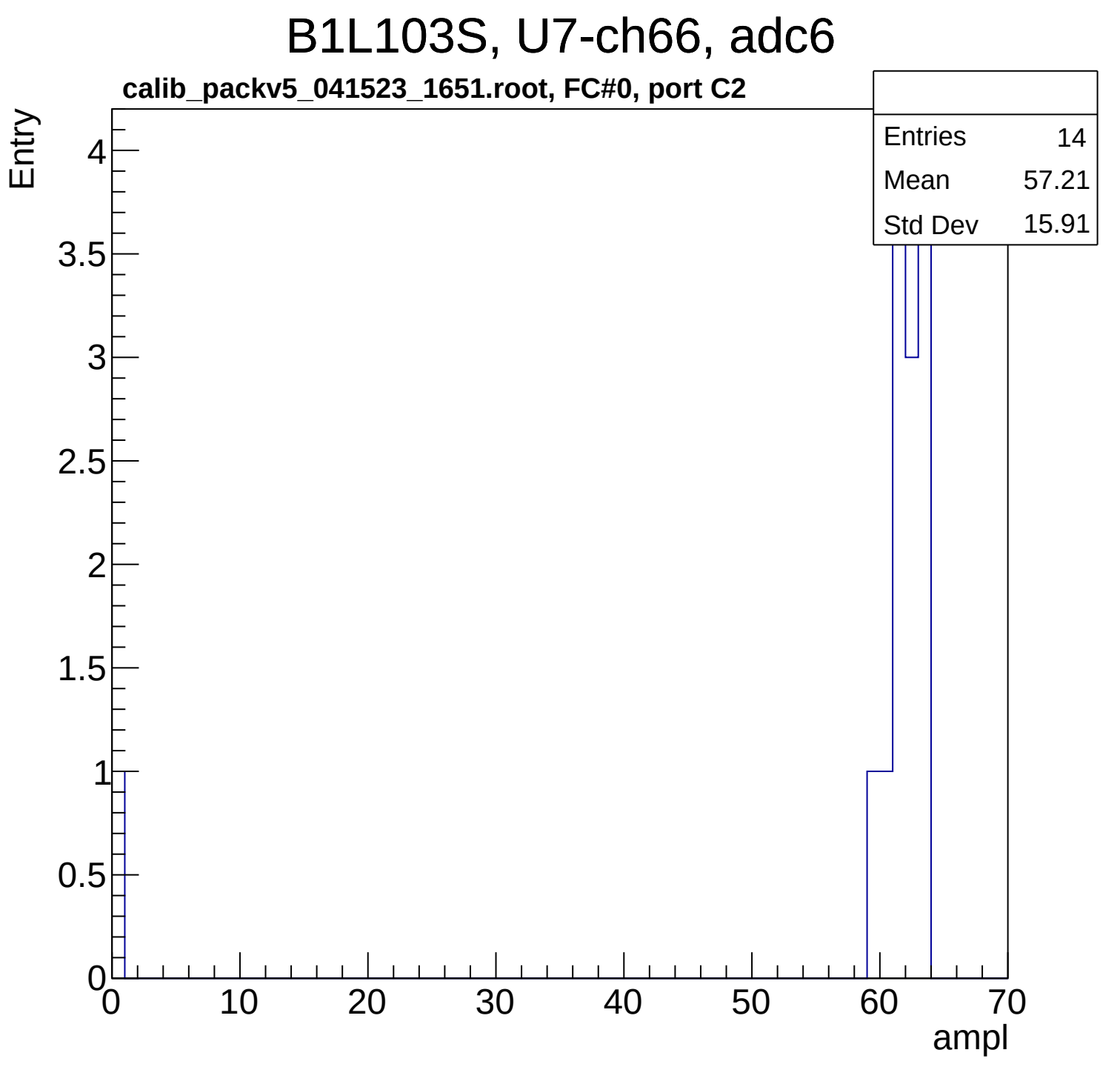
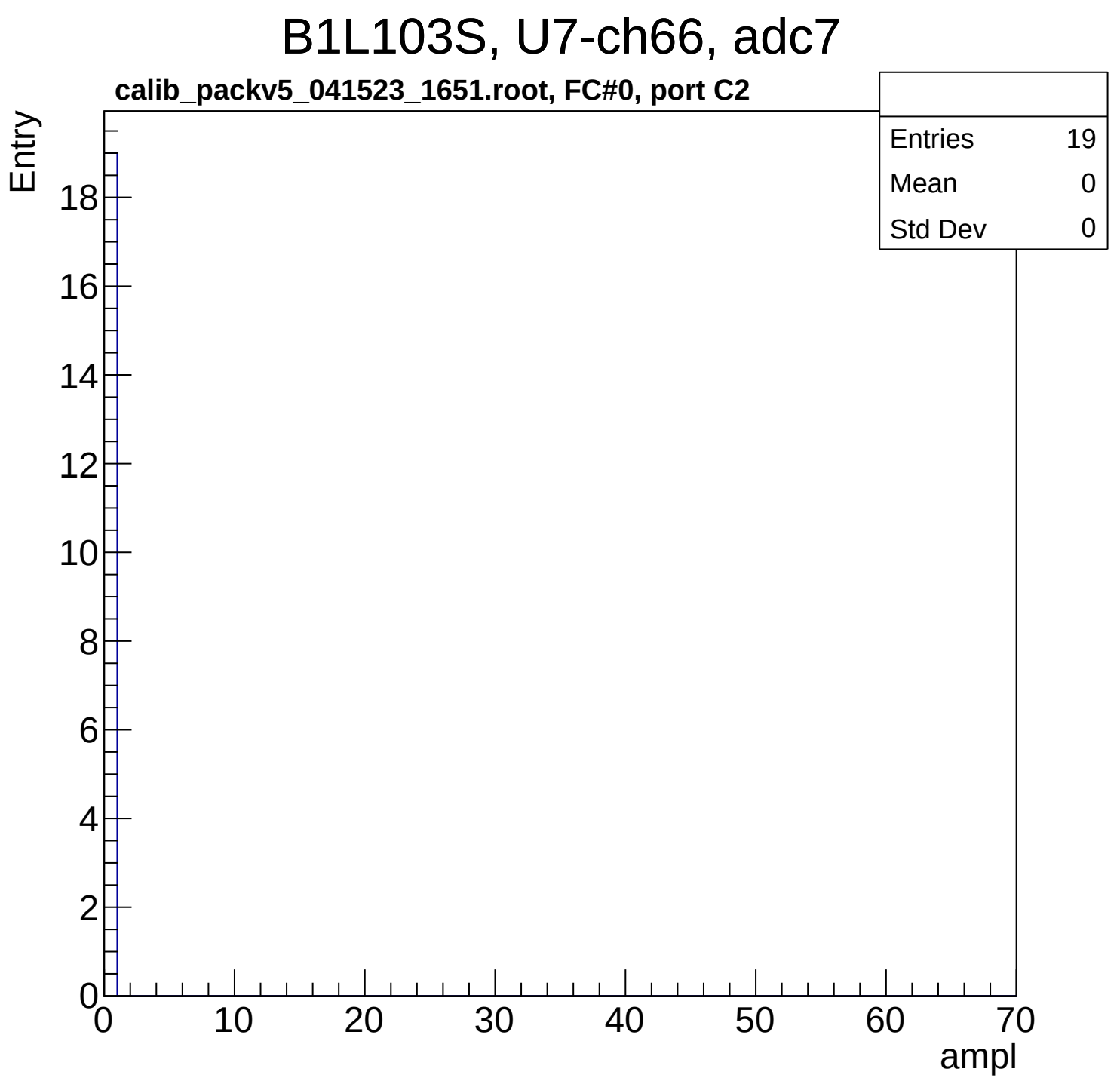
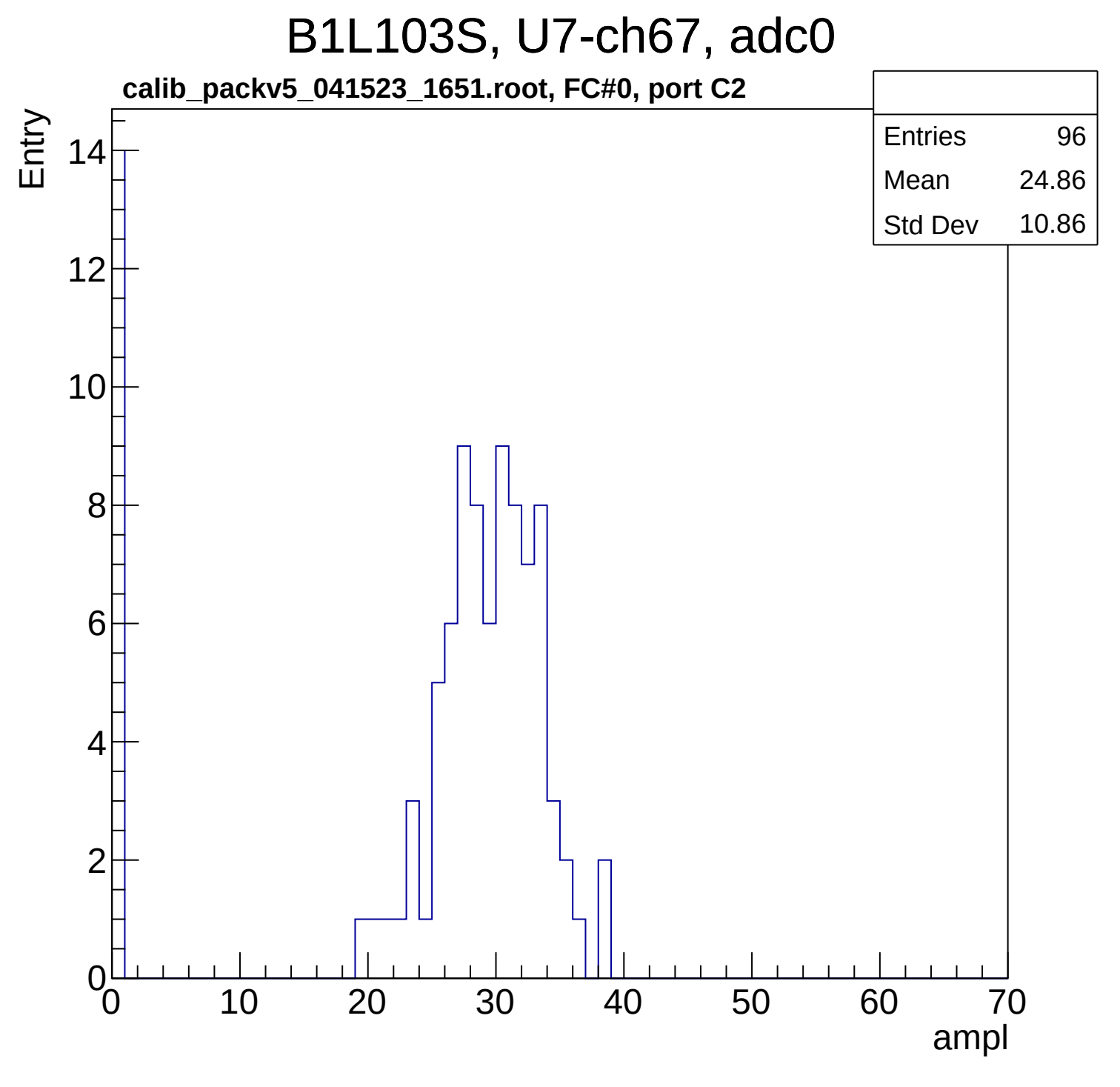
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch66, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 14
Mean 57.21
Std Dev 15.91
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U7-ch66, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch67, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 96
Mean 24.86
Std Dev 10.86
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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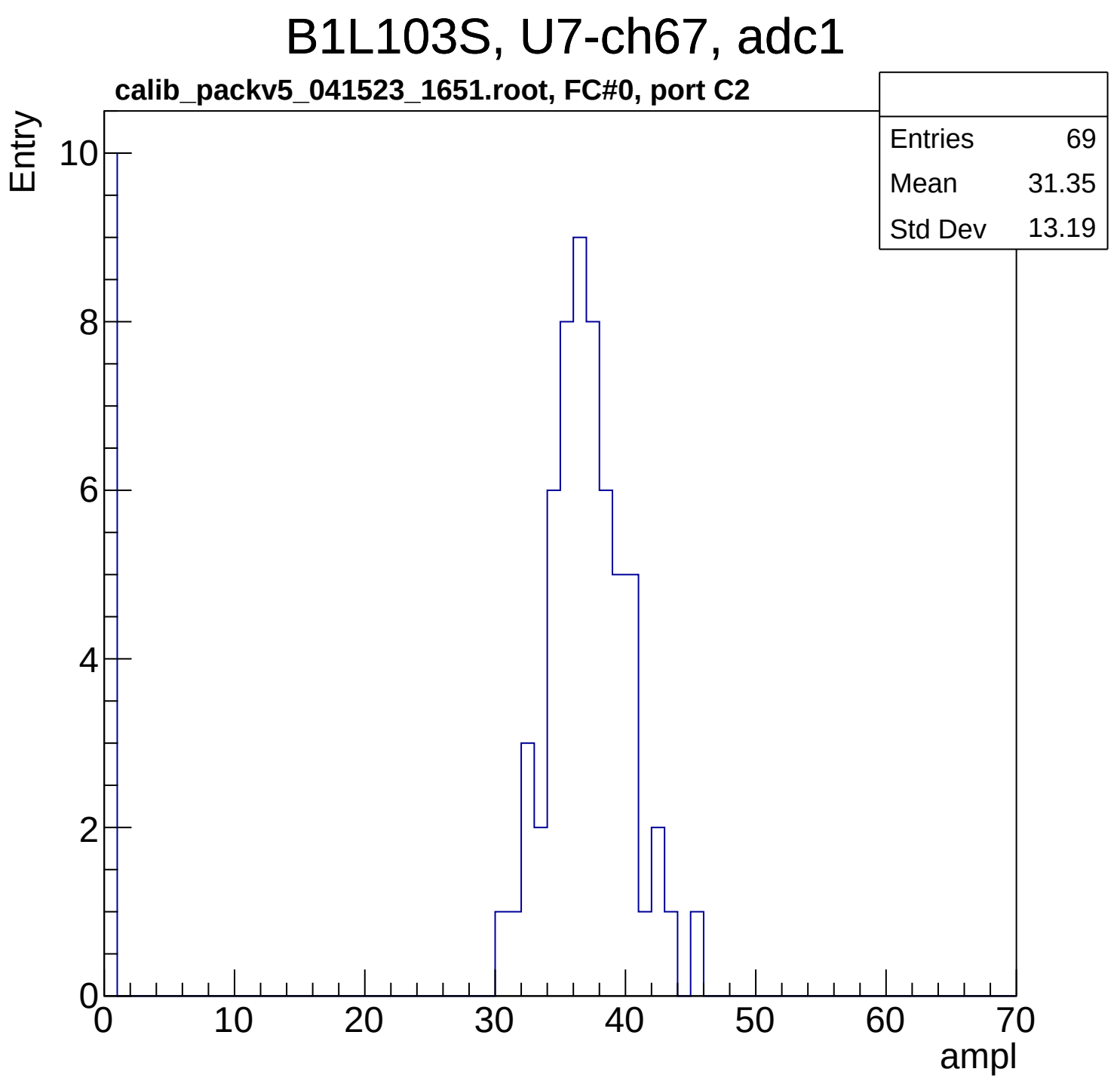
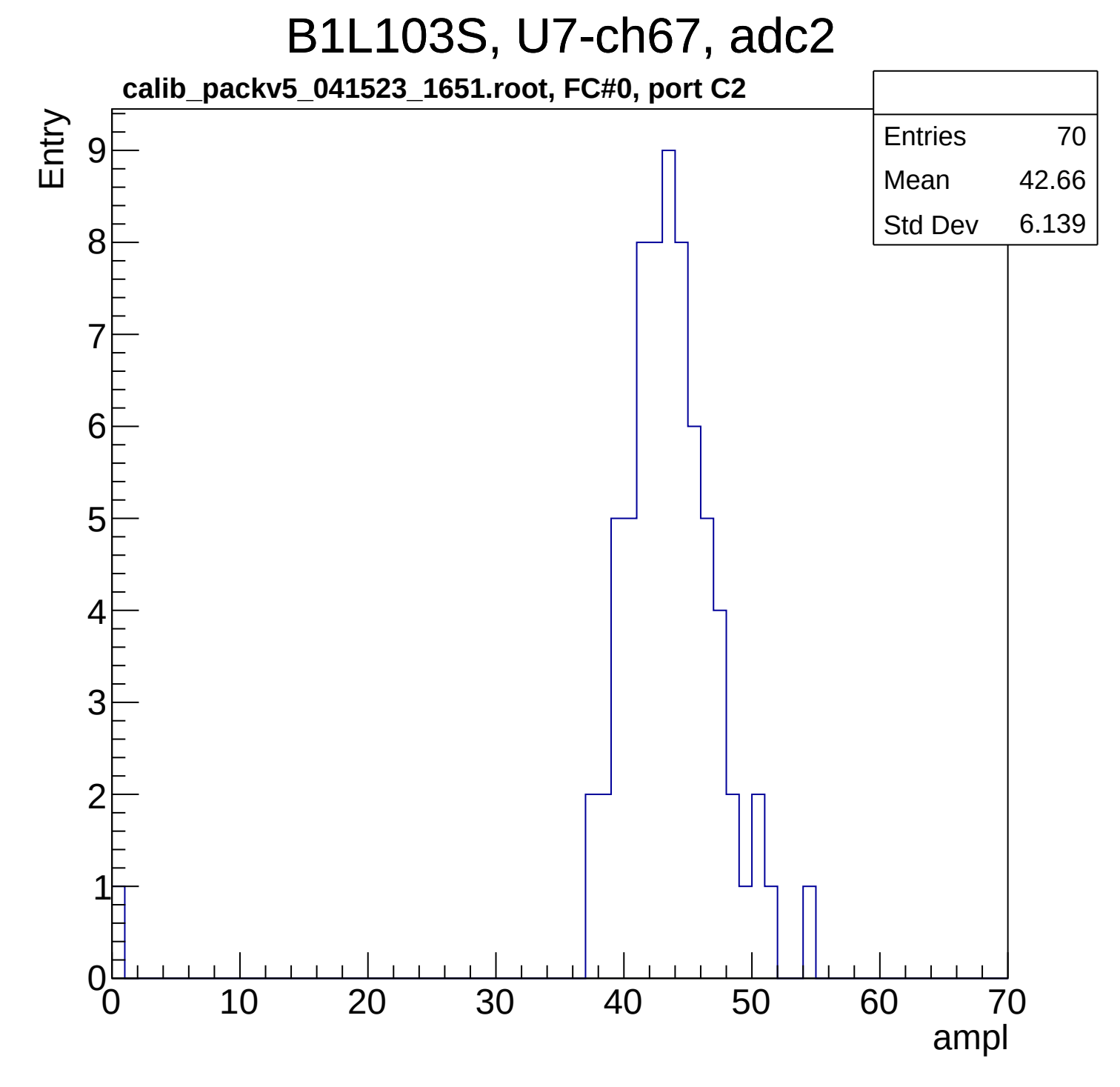

B1L103S, U7-ch67, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 31.35
Std Dev 13.19
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch67, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 42.66
Std Dev 6.139
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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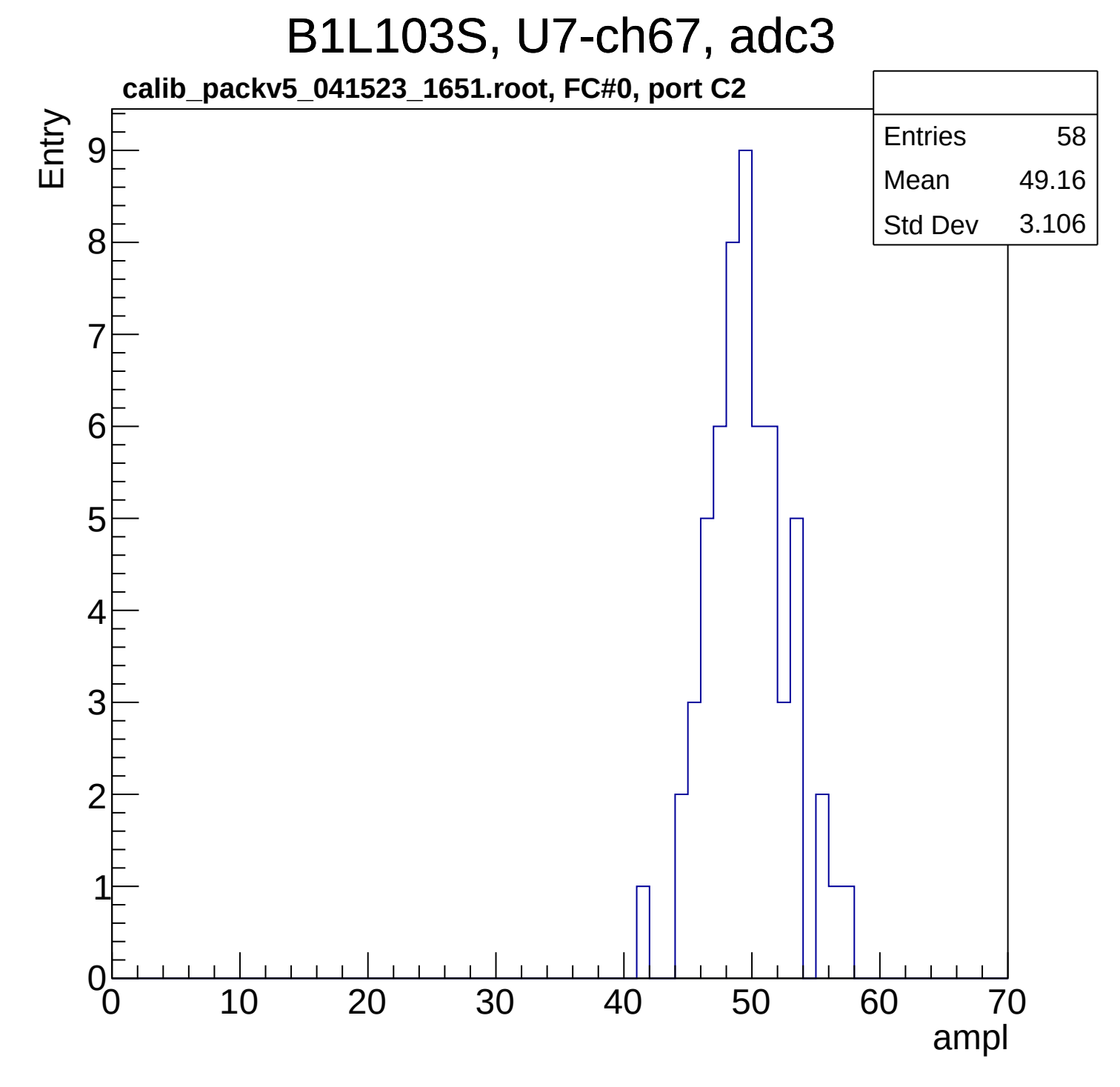
40
50
60
70


B1L103S, U7-ch67, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 49.16
Std Dev 3.106
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
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60
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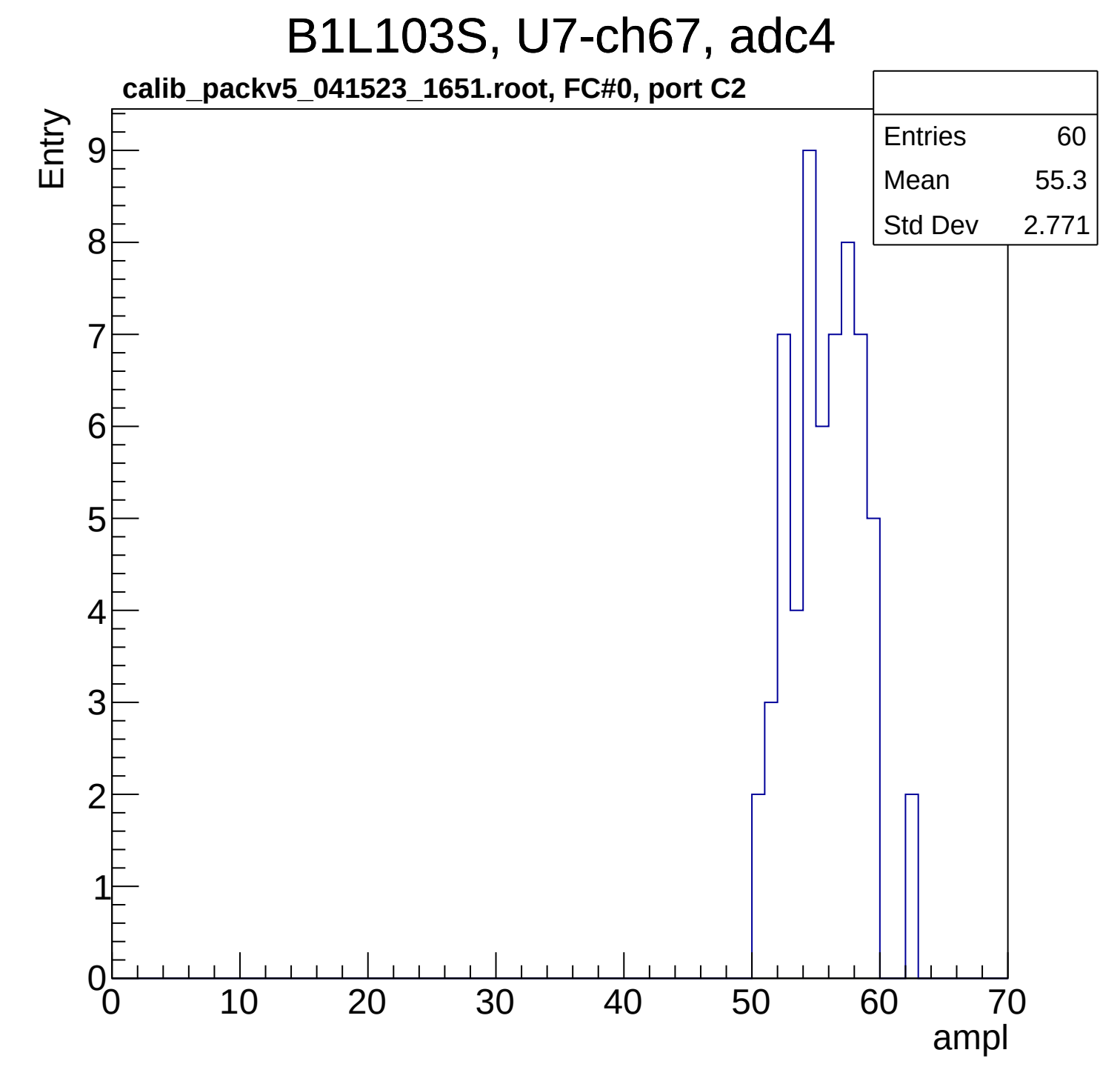
B1L103S, U7-ch67, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 55.3
Std Dev 2.771
Entry
ampl
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2
3
4
5
6
7
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0
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60
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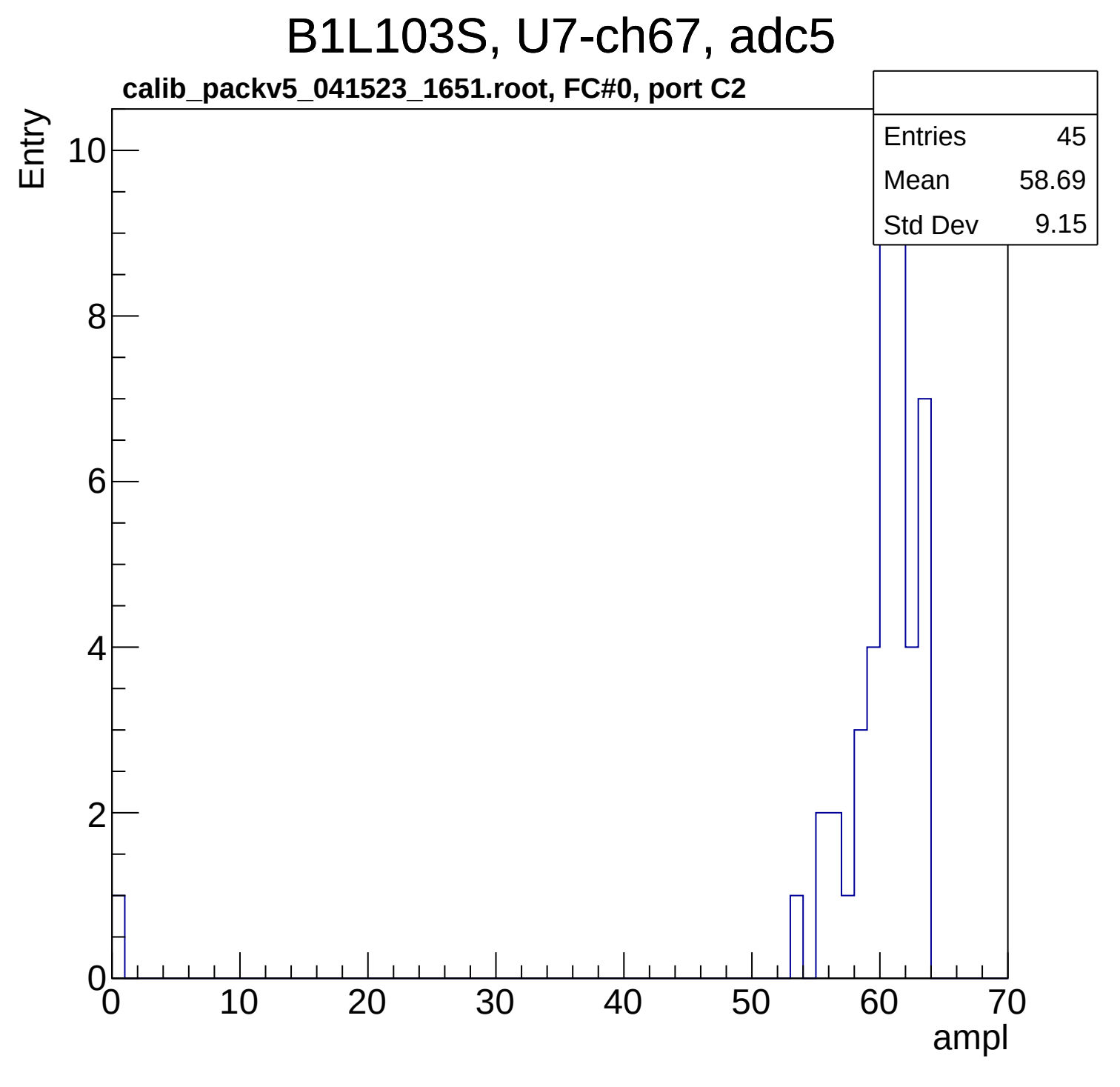
B1L103S, U7-ch67, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 58.69
Std Dev 9.15
Entry
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8
10
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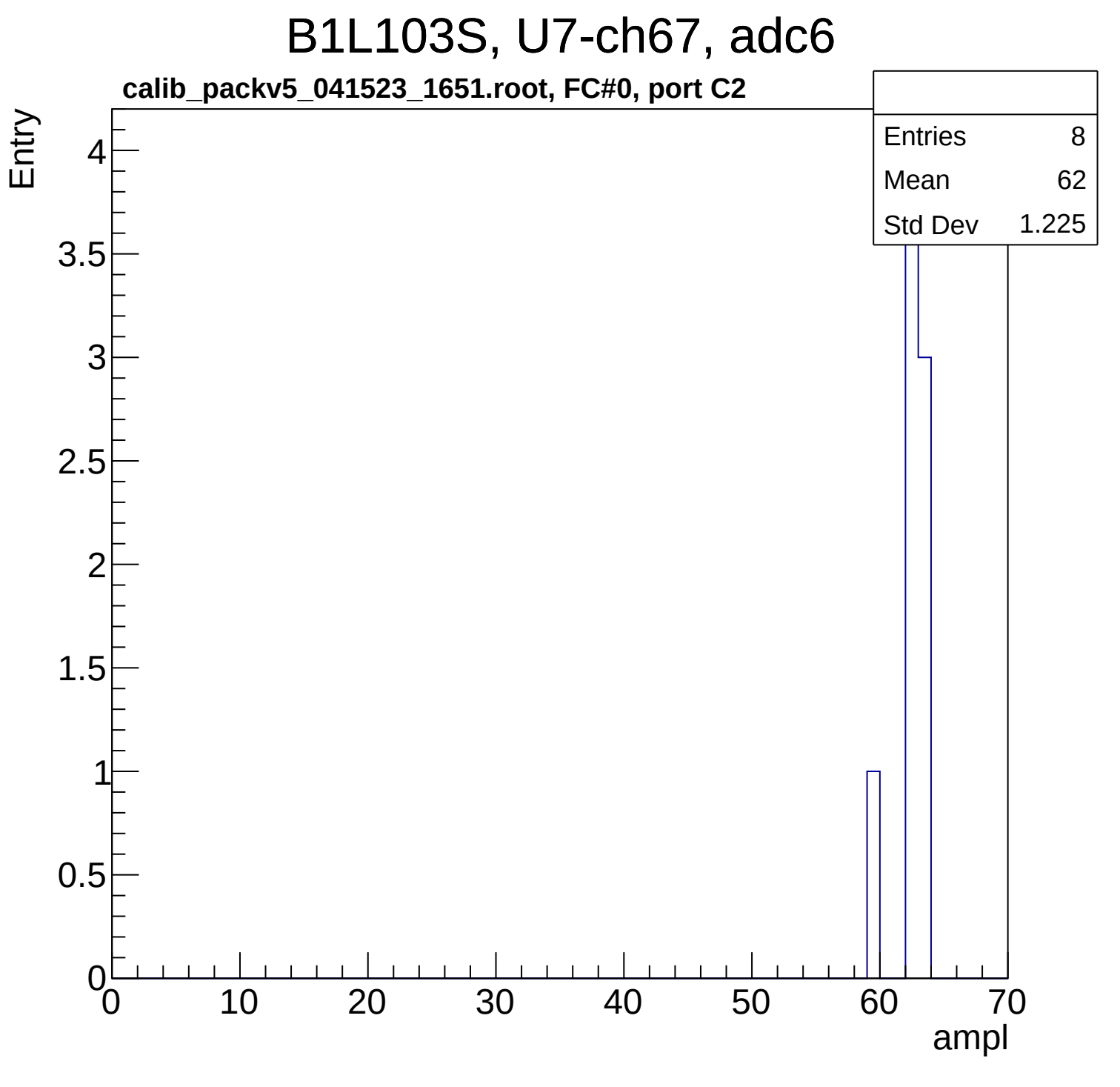
50
60
70
ampl


B1L103S, U7-ch67, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 62
Std Dev 1.225
Entry
ampl
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1.5
2
2.5
3
3.5
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0
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40
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60
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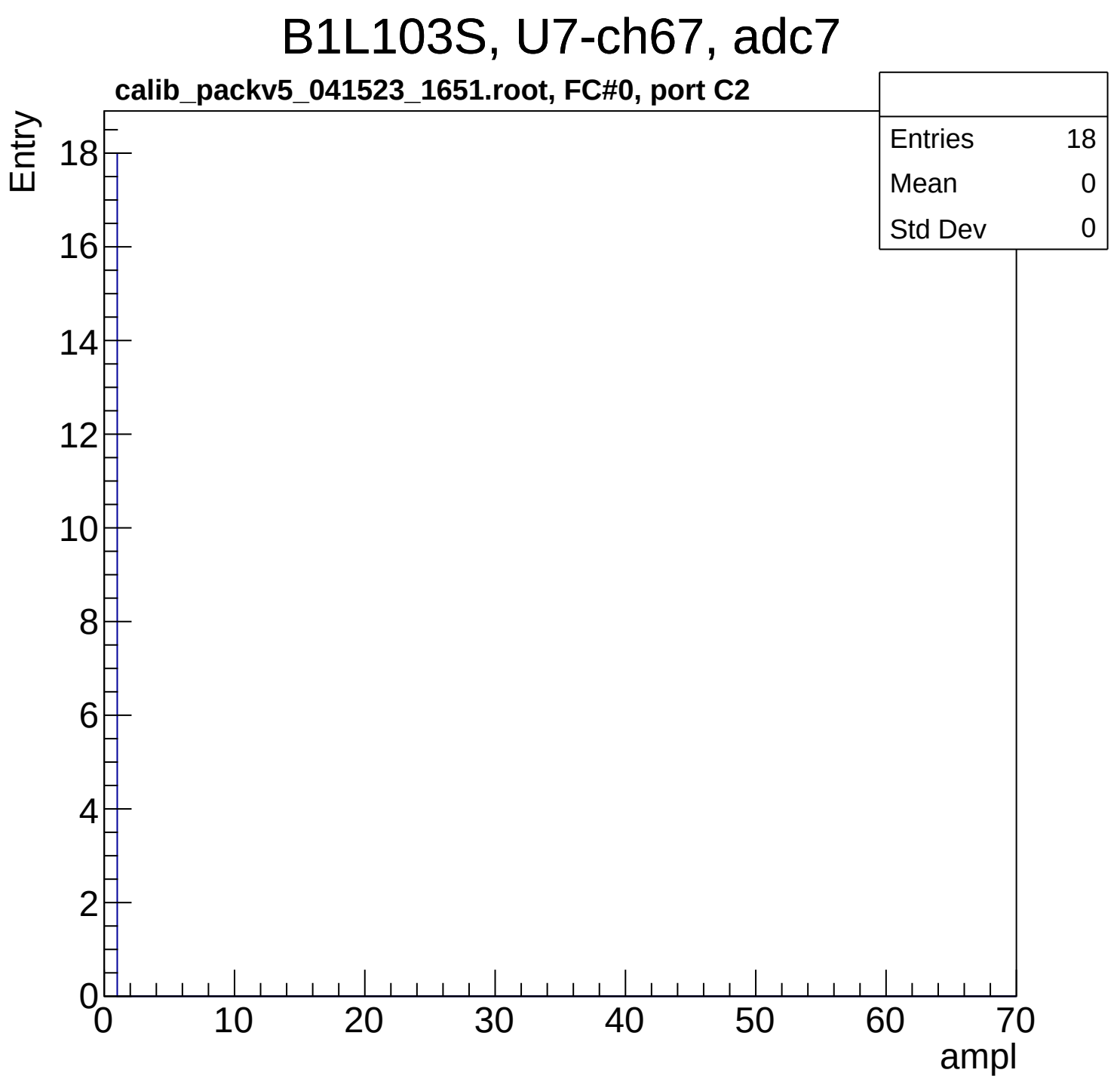
B1L103S, U7-ch67, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
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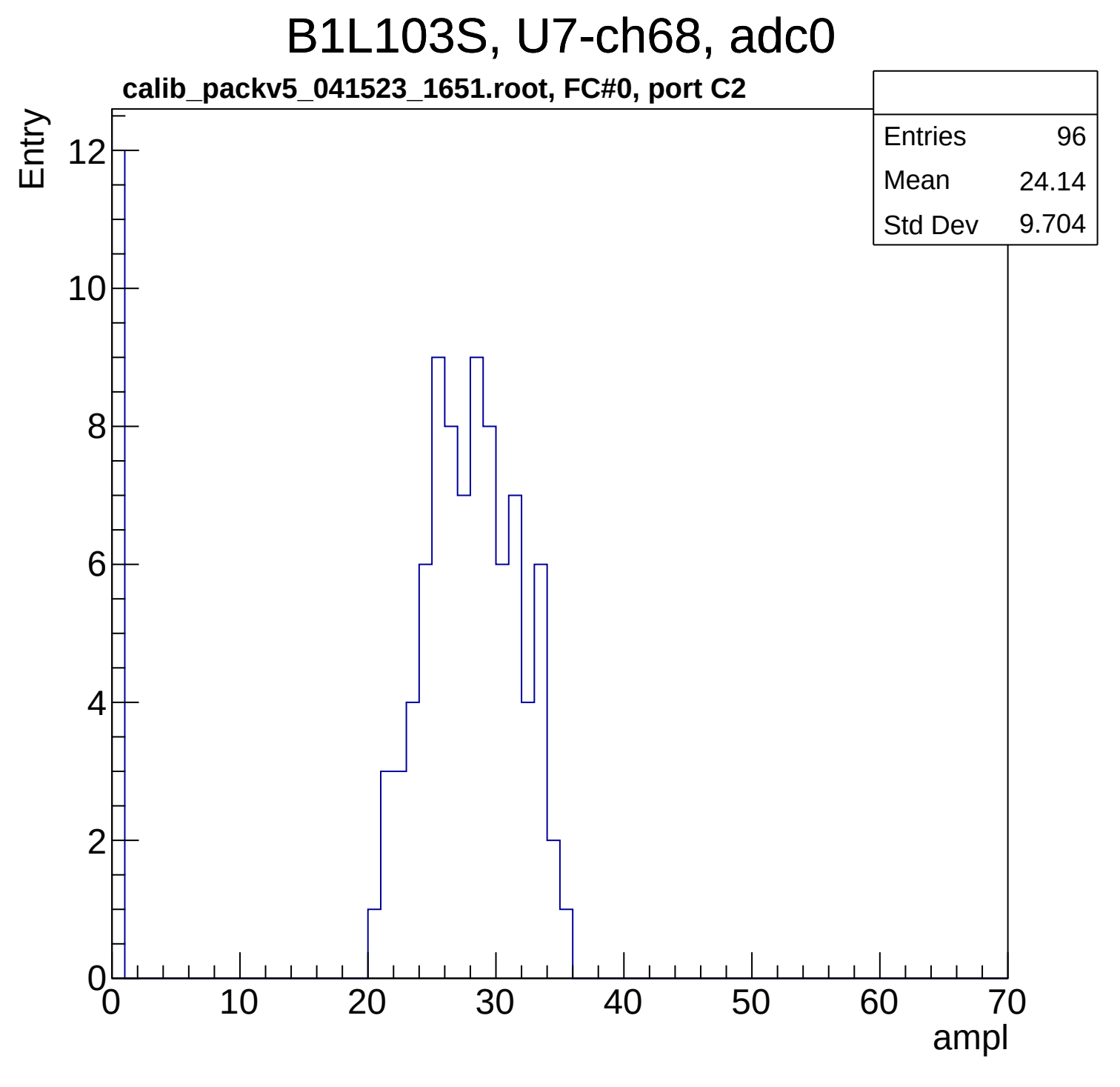
50
60
70
ampl


B1L103S, U7-ch68, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 96
Mean 24.14
Std Dev 9.704
Entry
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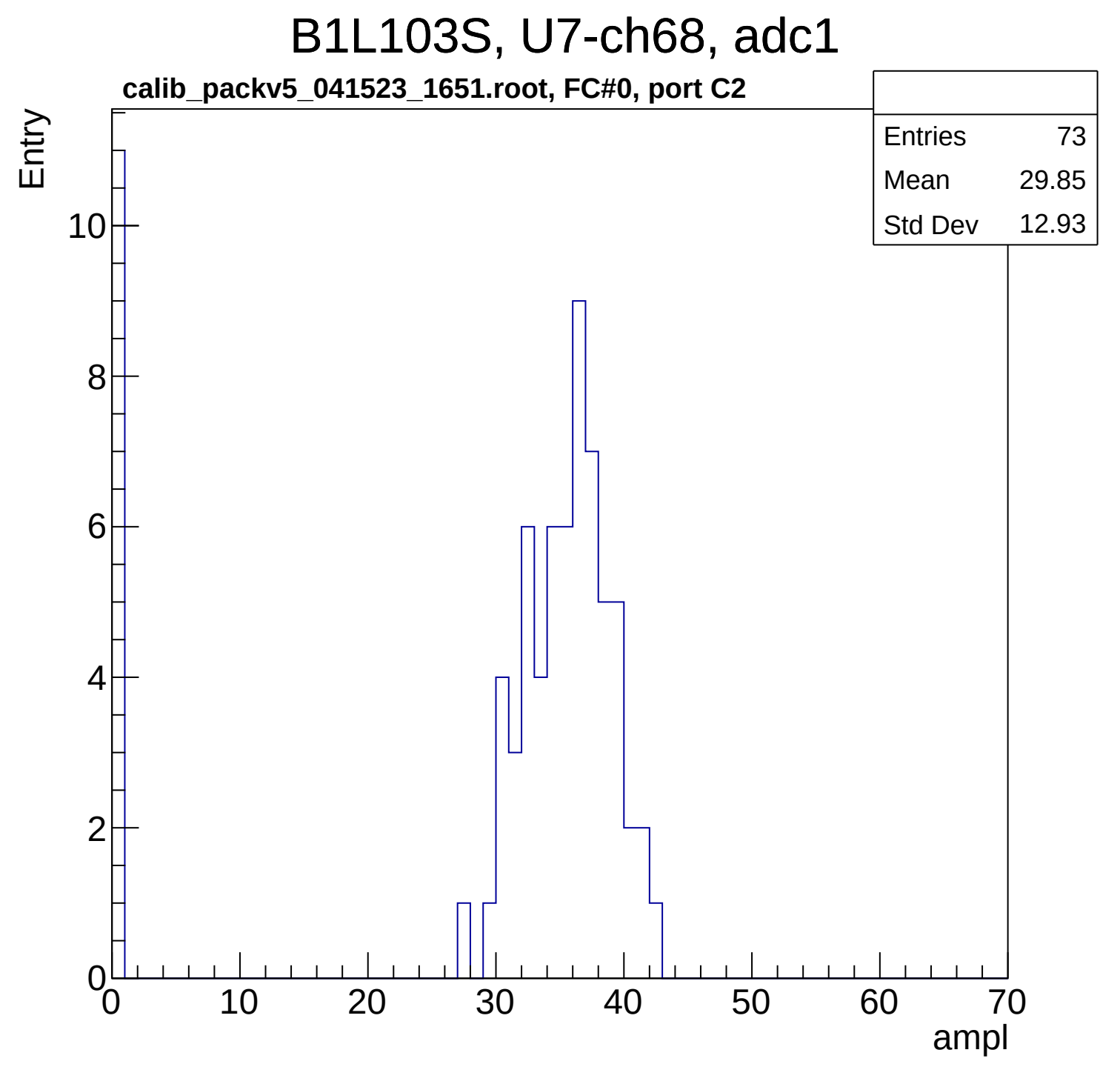
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch68, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 29.85
Std Dev 12.93
Entry
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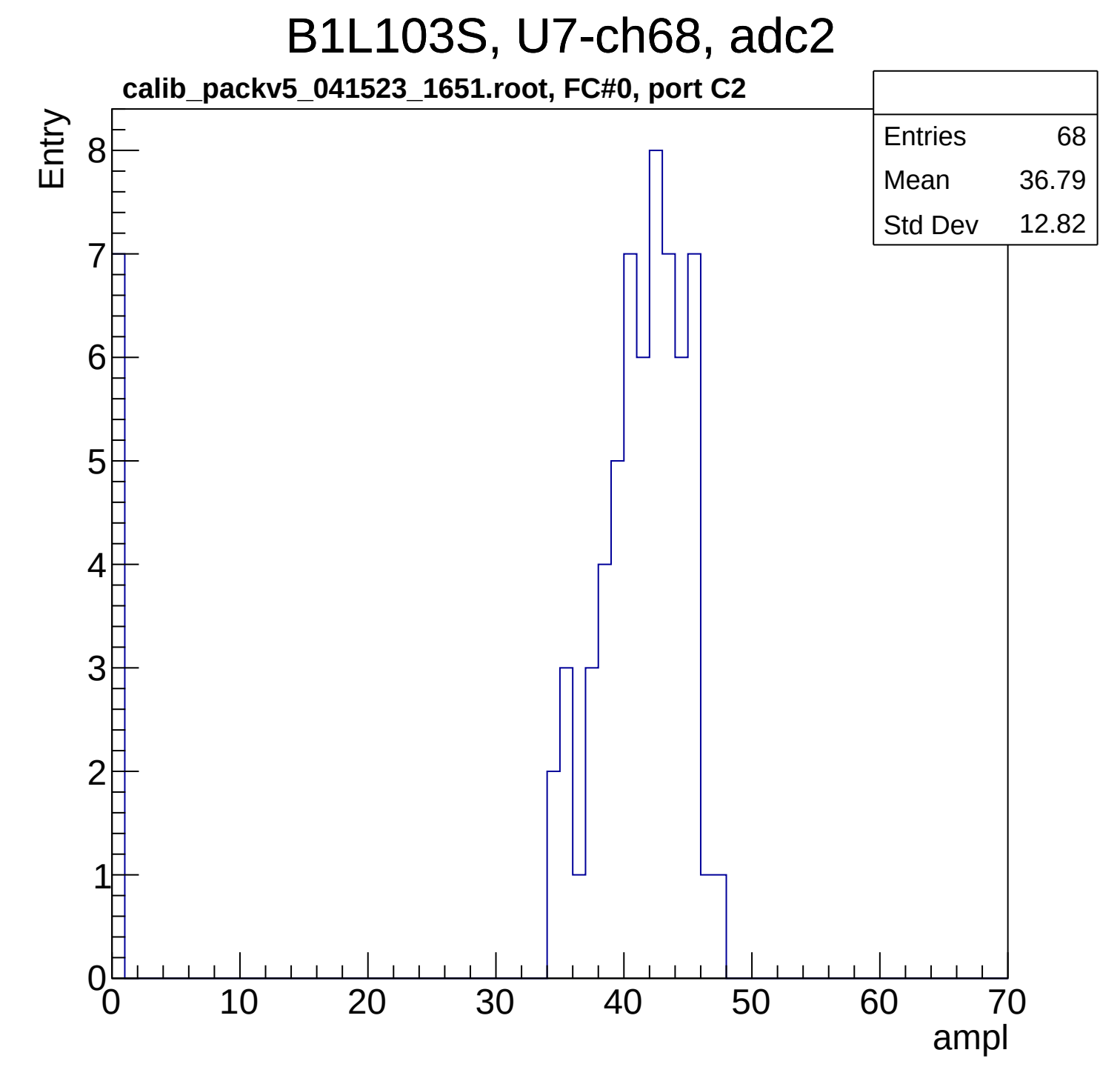
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch68, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 36.79
Std Dev 12.82
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
30
40
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60
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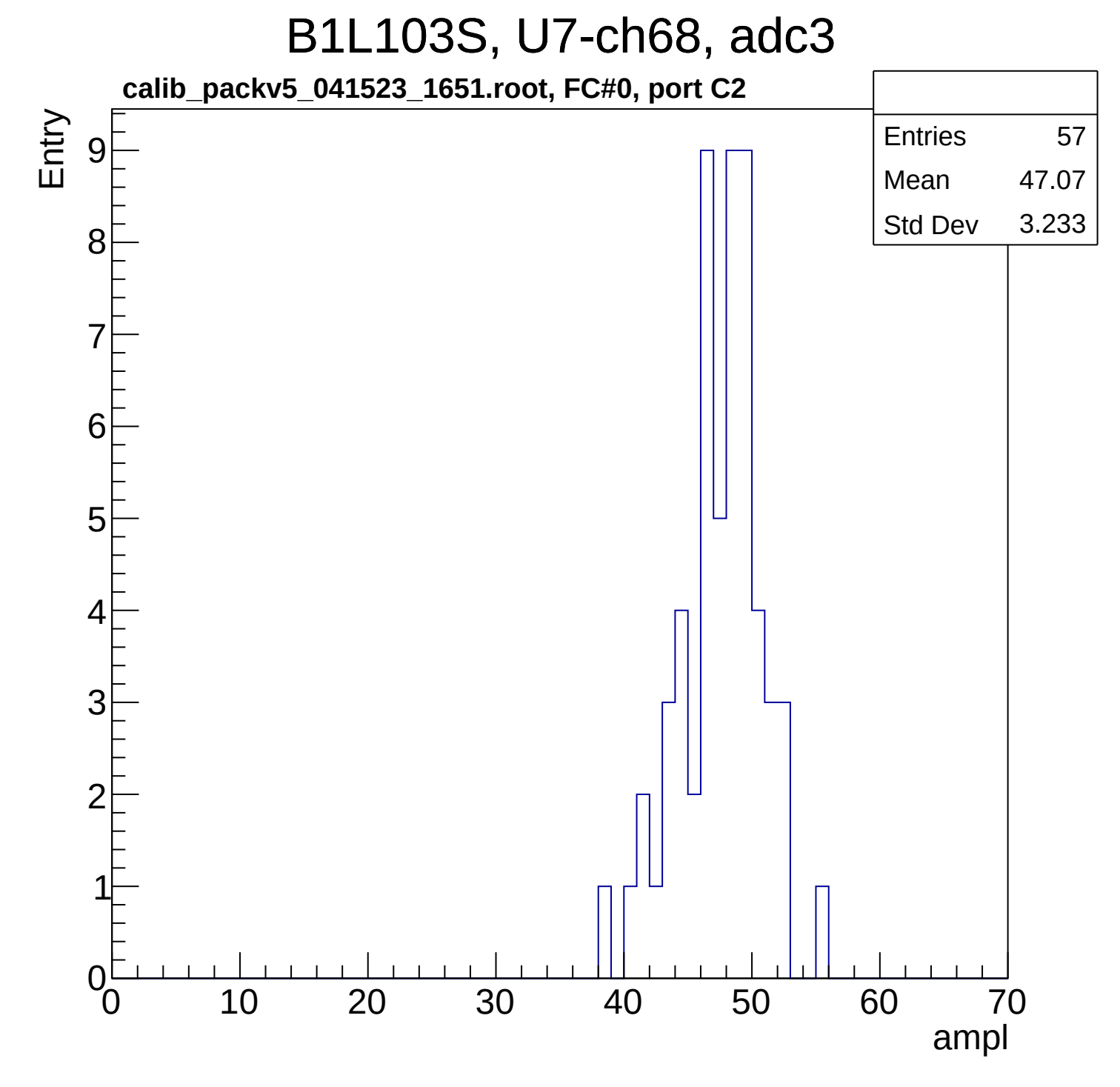
B1L103S, U7-ch68, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 47.07
Std Dev 3.233
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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40
50
60
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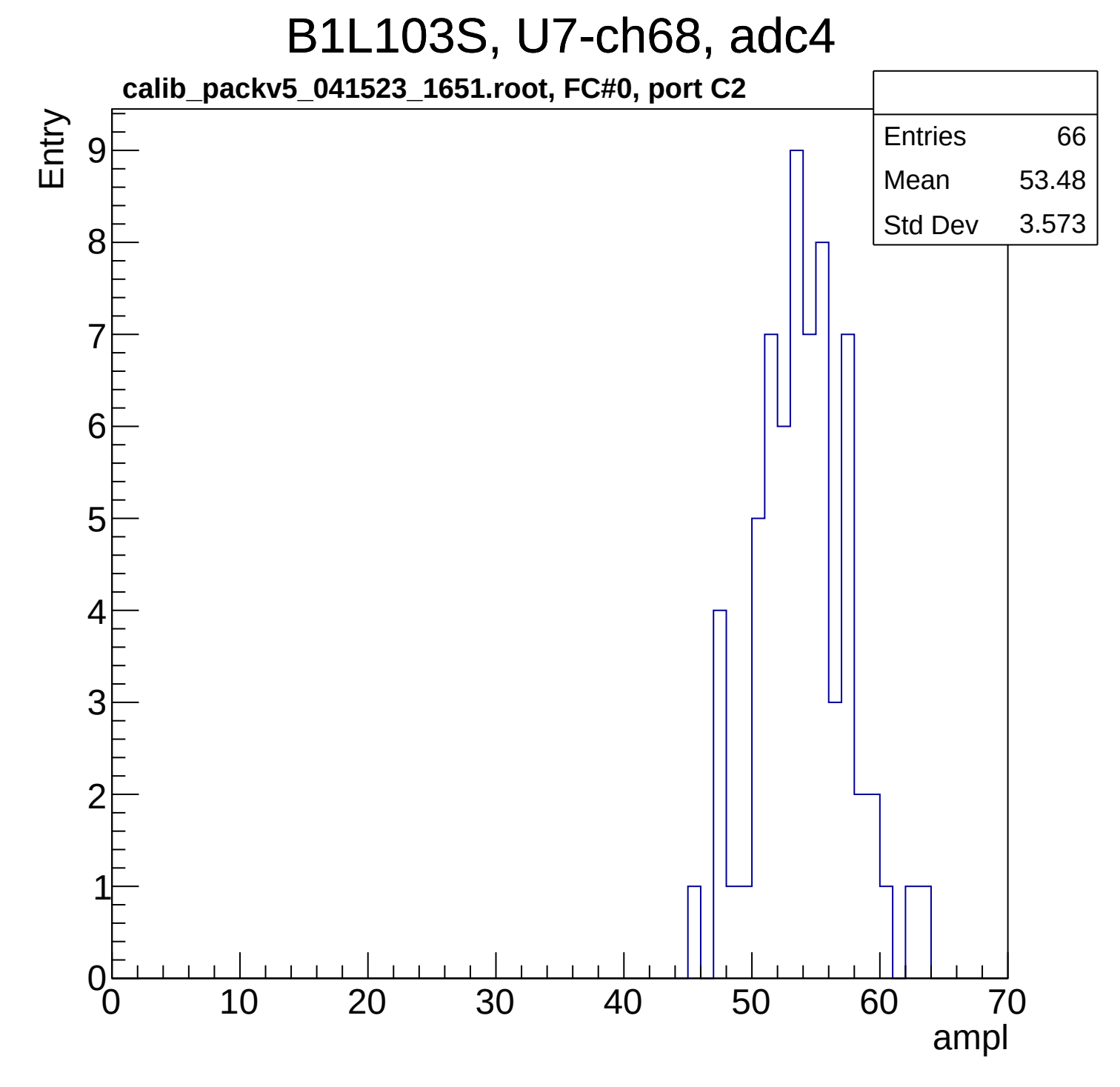
B1L103S, U7-ch68, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 53.48
Std Dev 3.573
Entry
ampl
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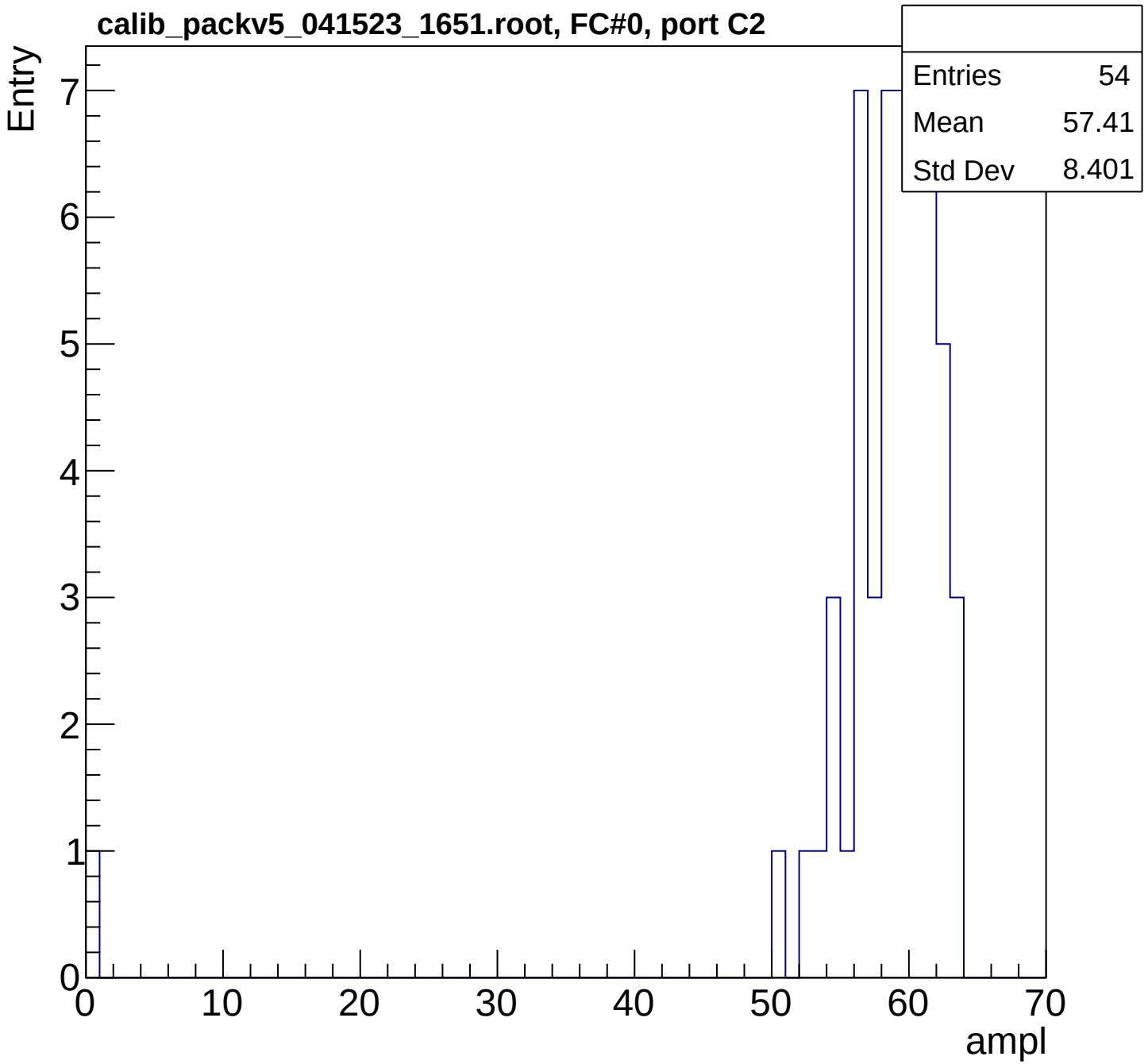
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U7-ch68, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 57.41
Std Dev 8.401
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
30
40
50
60
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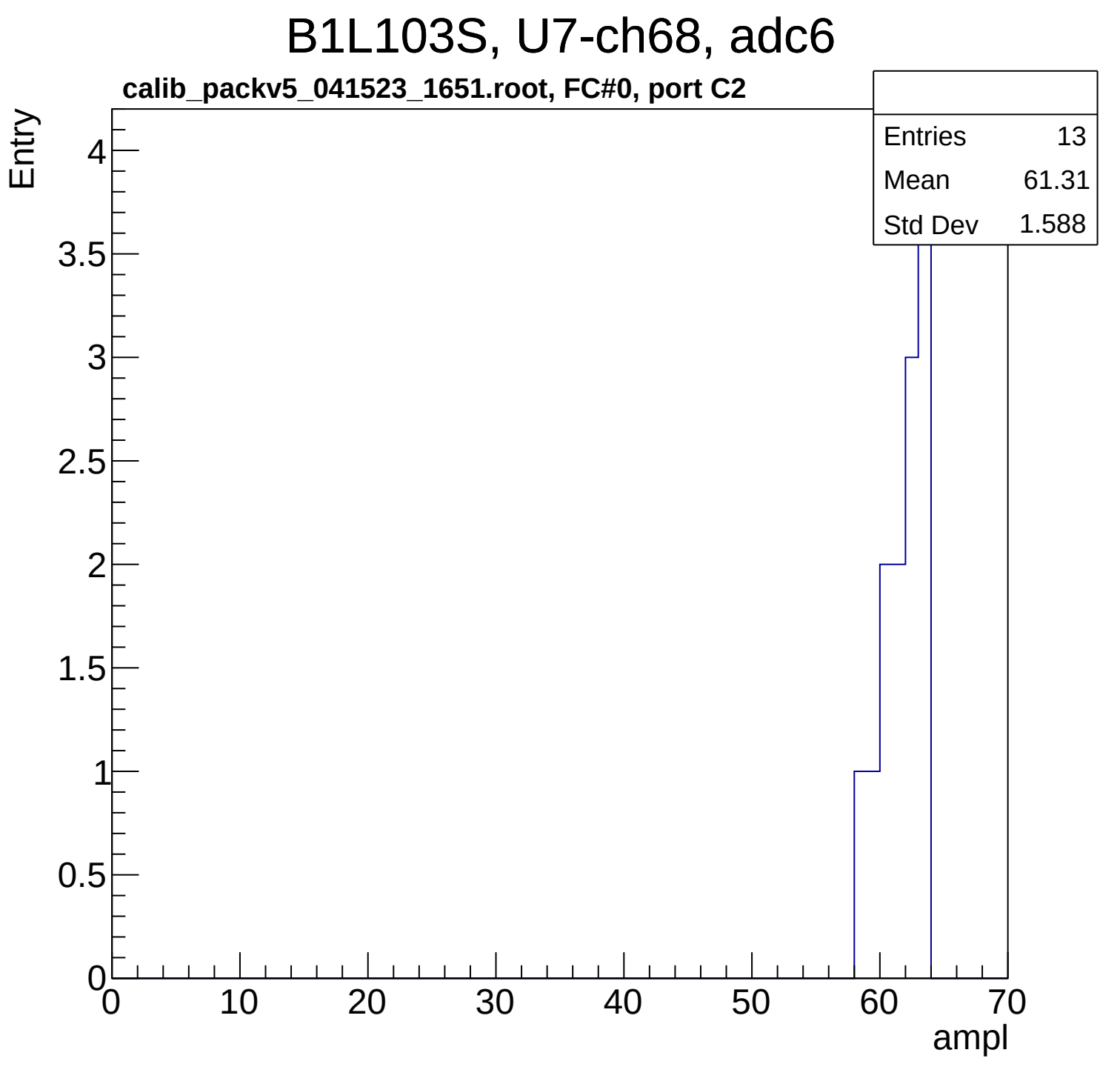
B1L103S, U7-ch68, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 13
Mean 61.31
Std Dev 1.588
Entry
ampl
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0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
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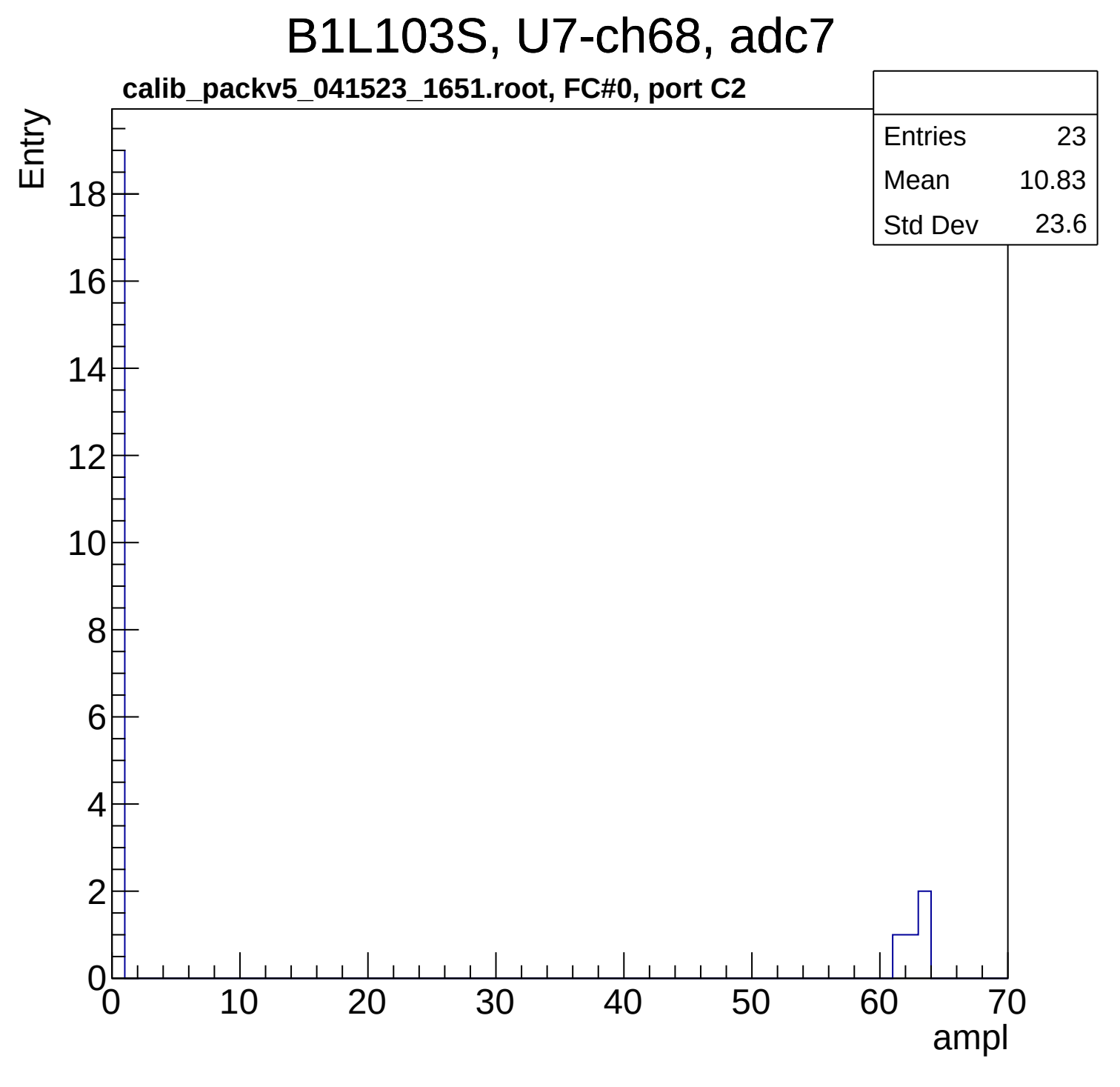
B1L103S, U7-ch68, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 23
Mean 10.83
Std Dev 23.6
Entry
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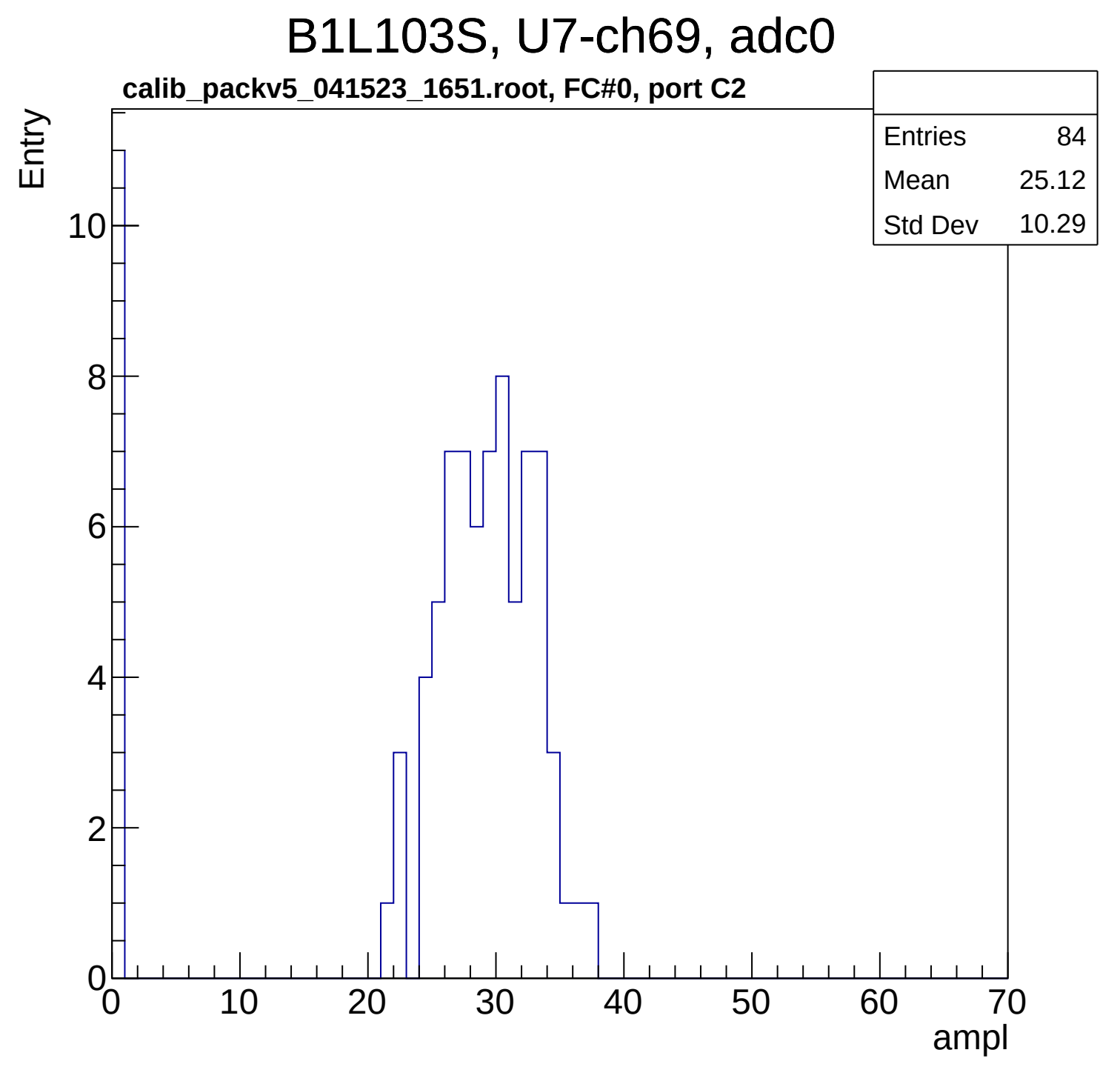
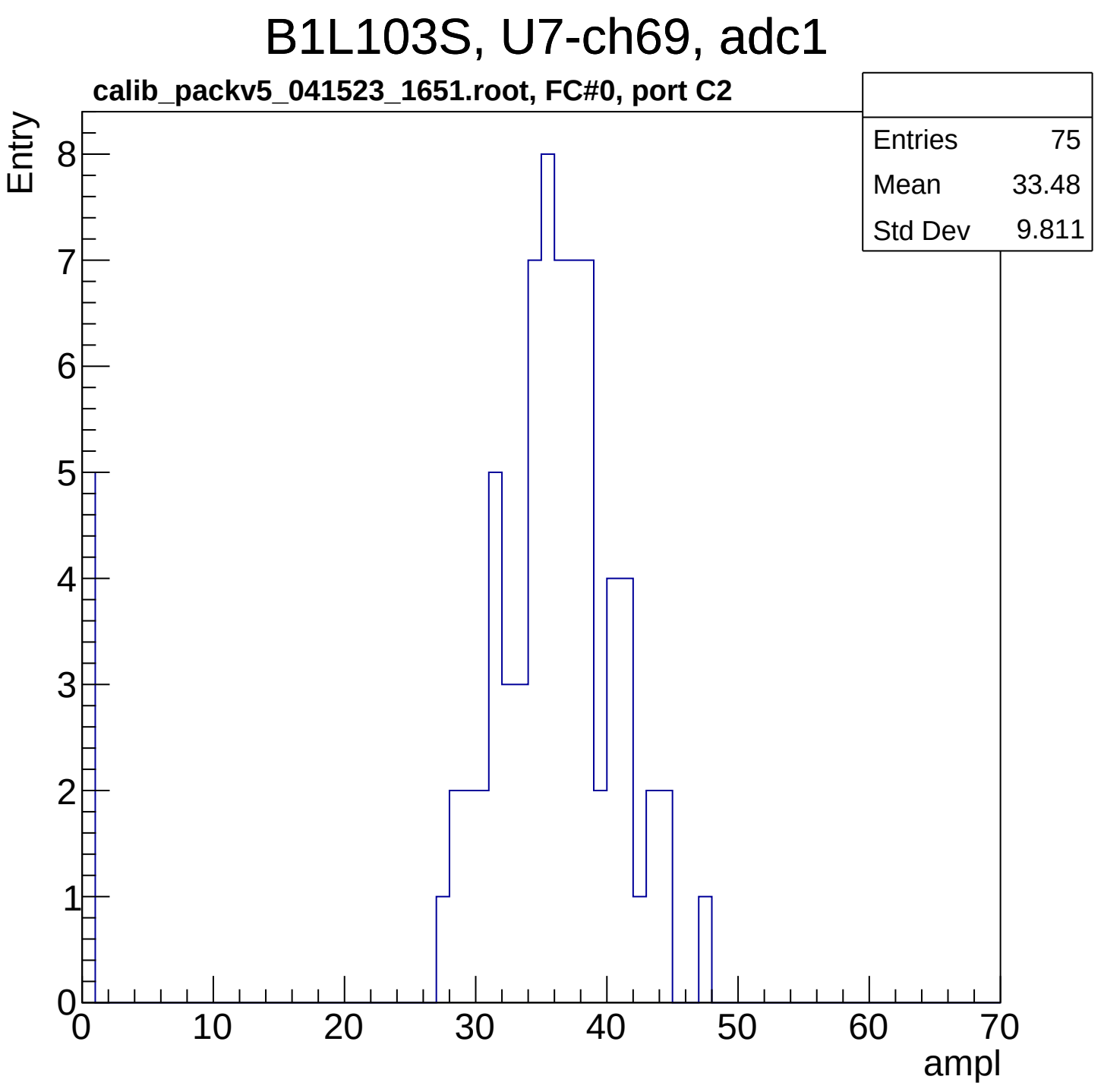
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch69, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 25.12
Std Dev 10.29
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch69, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 33.48
Std Dev 9.811
Entry
ampl
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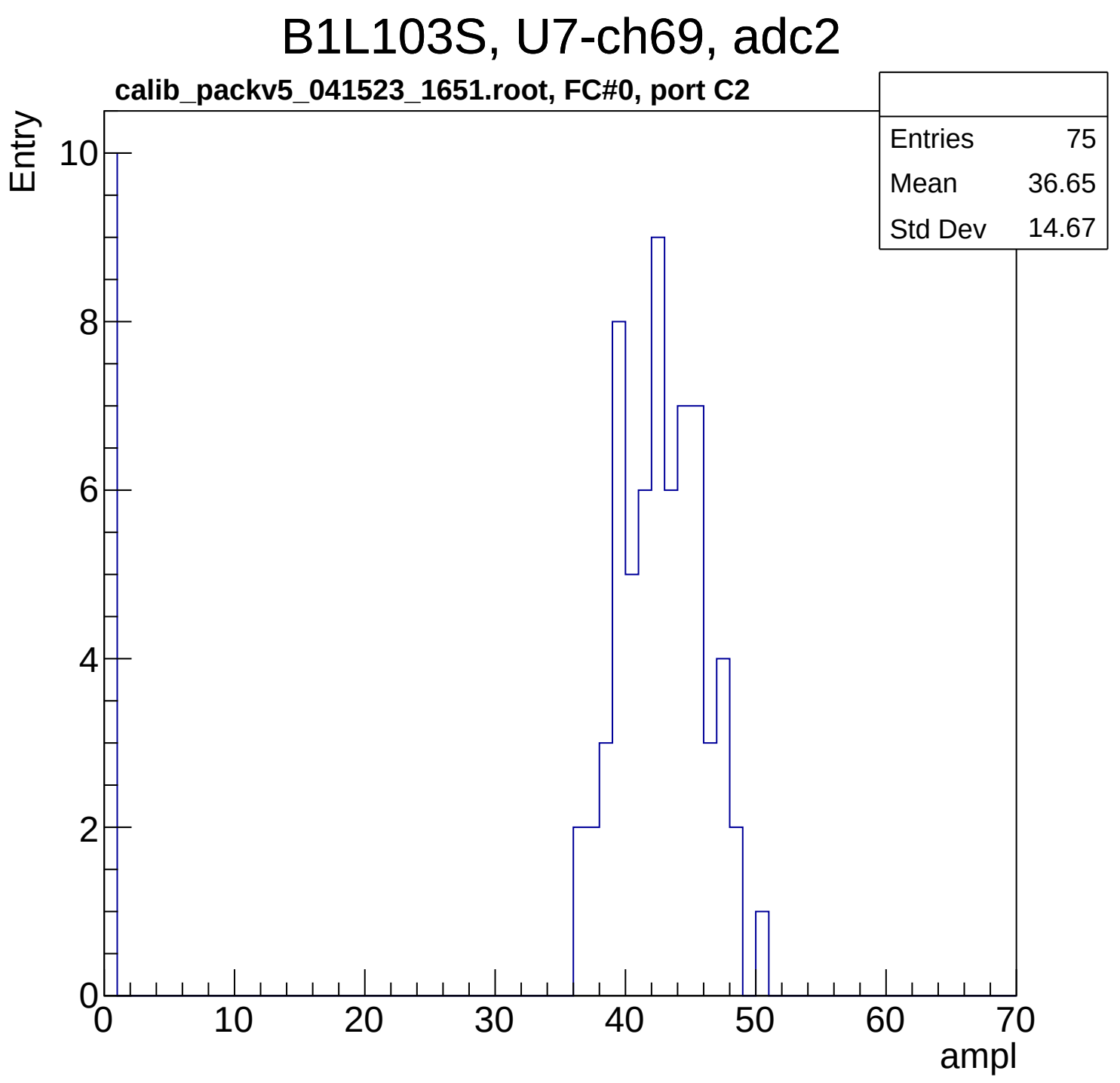
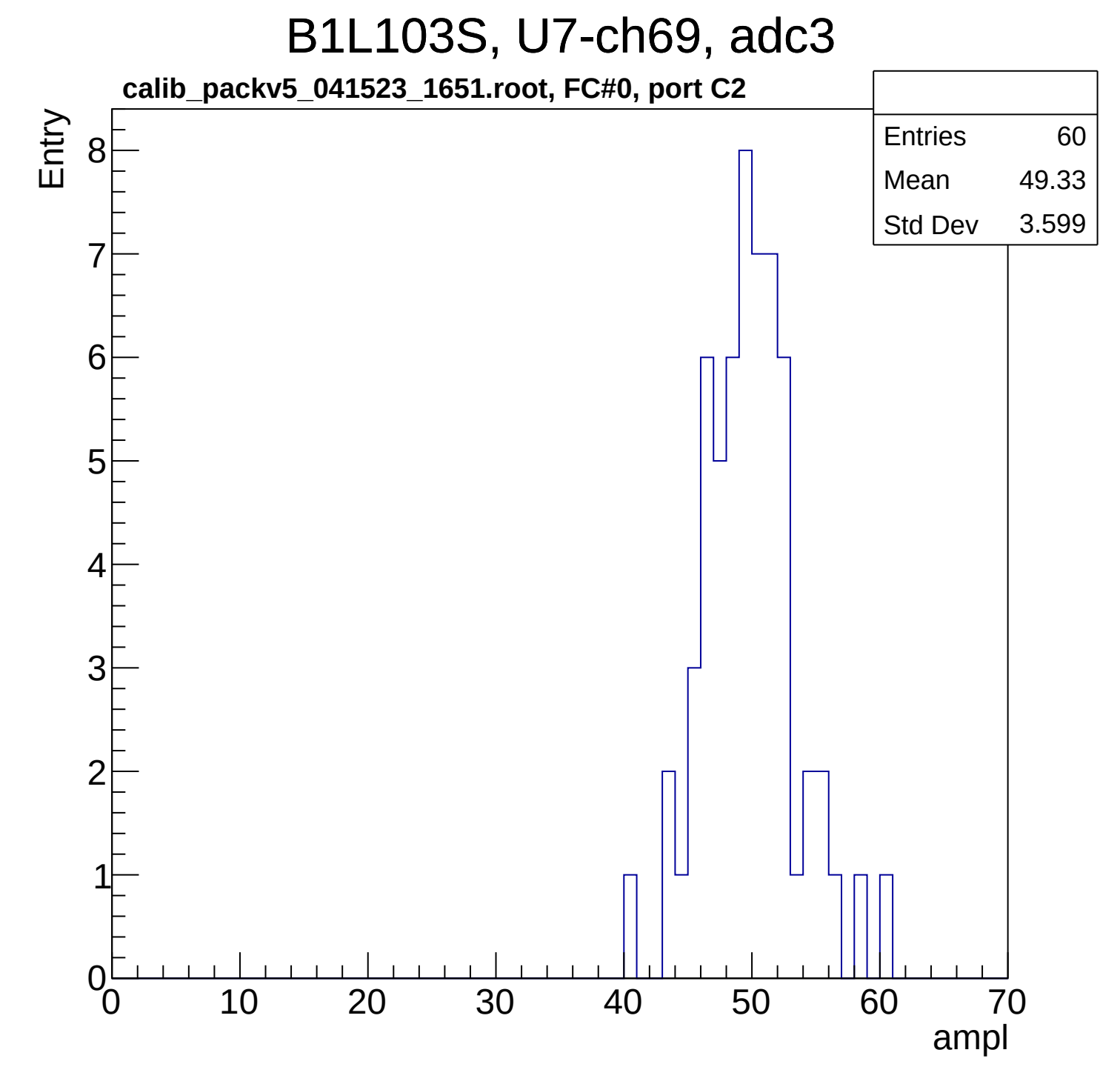
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch69, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 36.65
Std Dev 14.67
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch69, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 49.33
Std Dev 3.599
Entry
ampl
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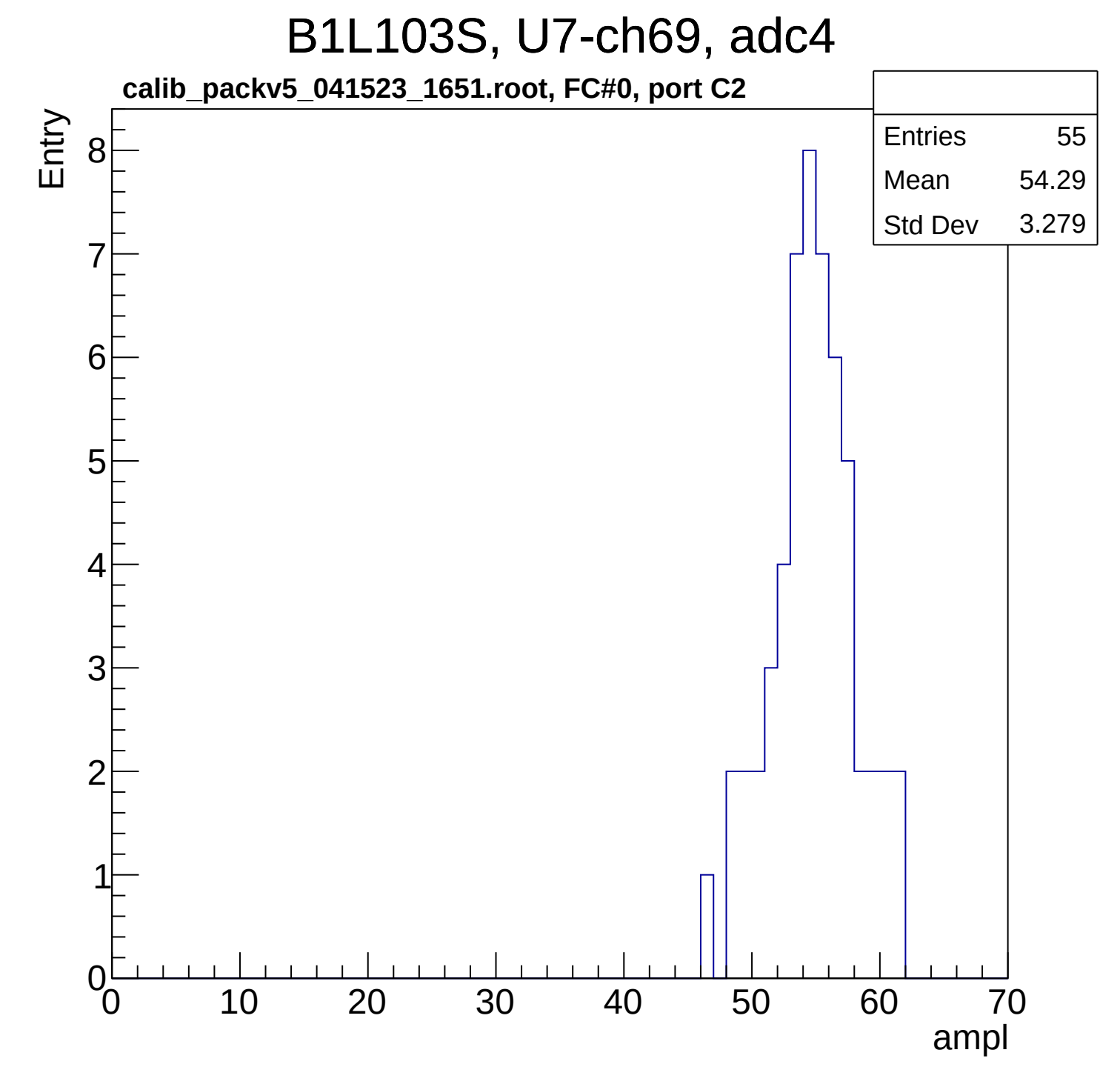
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch69, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 54.29
Std Dev 3.279
Entry
ampl
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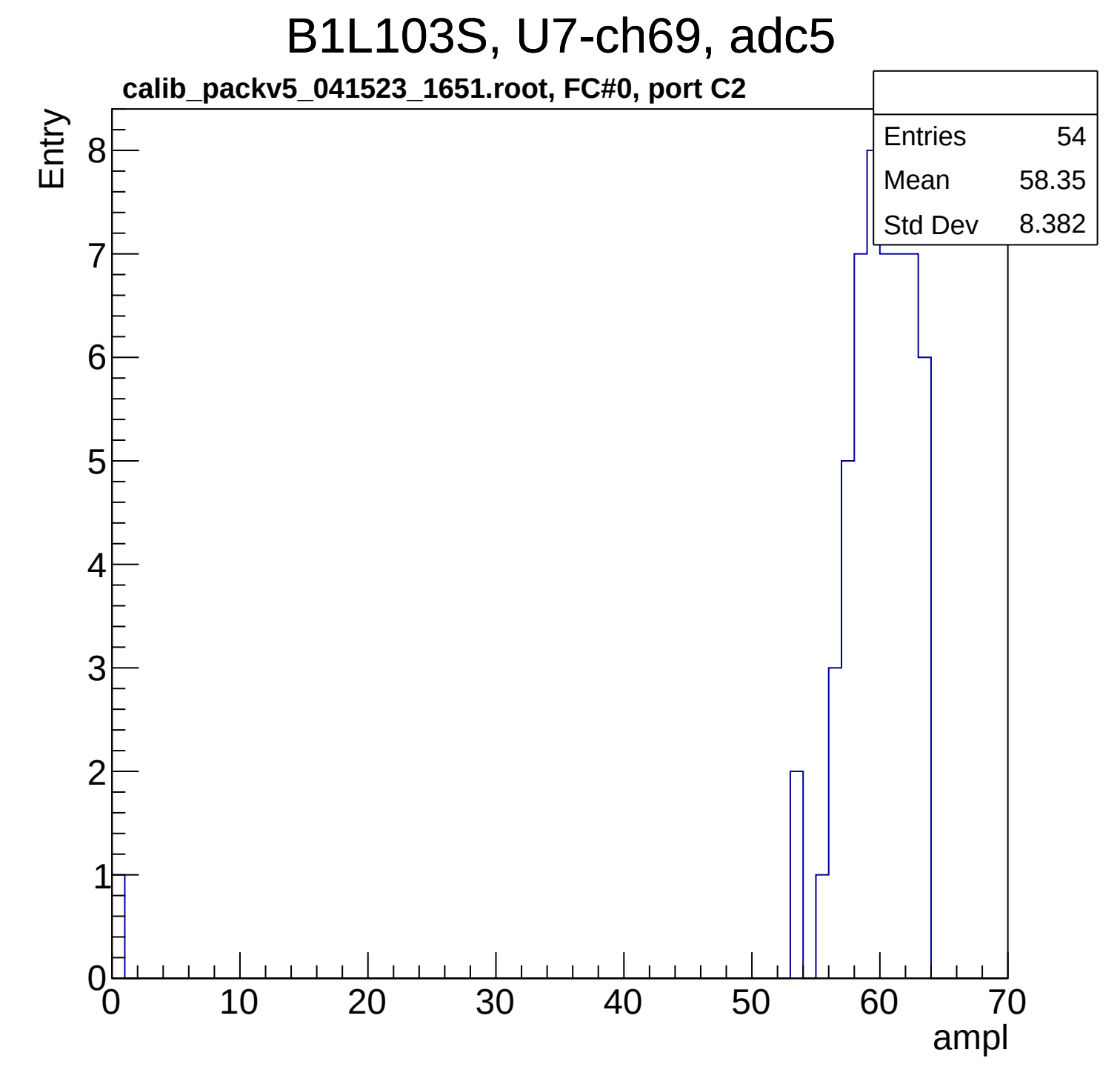
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch69, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 58.35
Std Dev 8.382
Entry
ampl
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2
3
4
5
6
7
8
0
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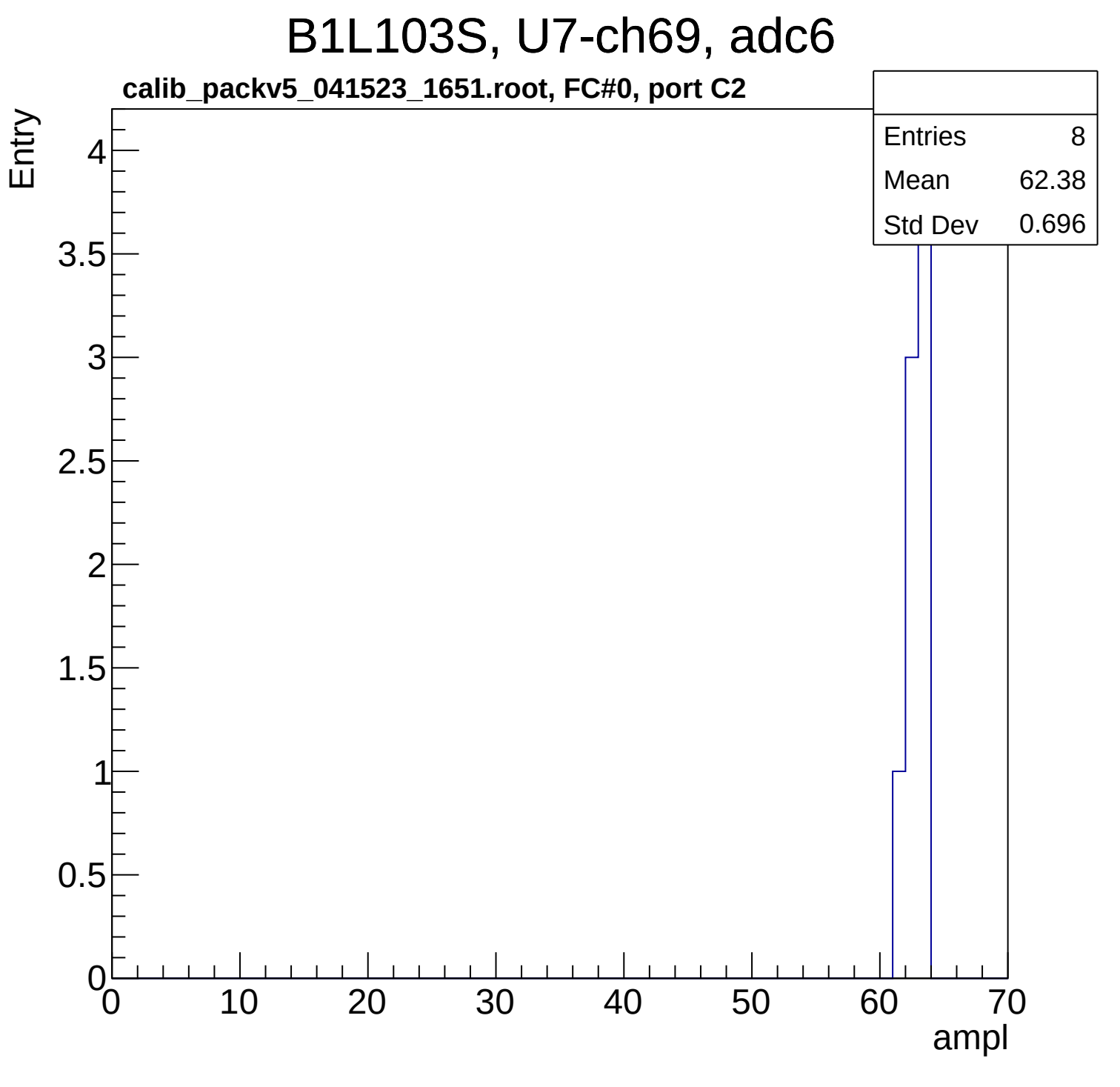
40
50
60
70


B1L103S, U7-ch69, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 62.38
Std Dev 0.696
Entry
ampl
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1.5
2
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3
3.5
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0
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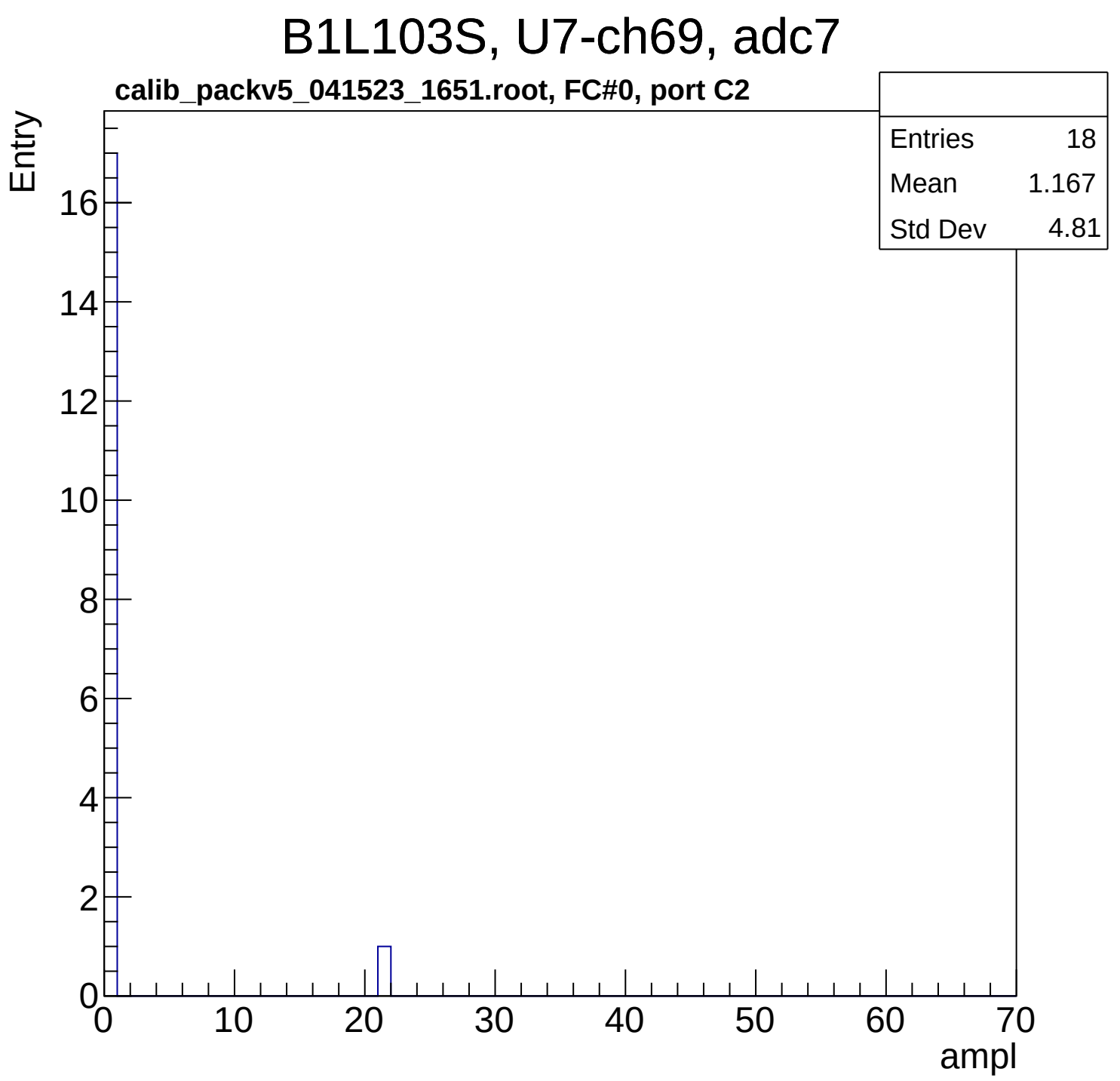
50
60
70


B1L103S, U7-ch69, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 1.167
Std Dev 4.81
Entry
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4
6
8
10
12
14
16
0
10
20
30
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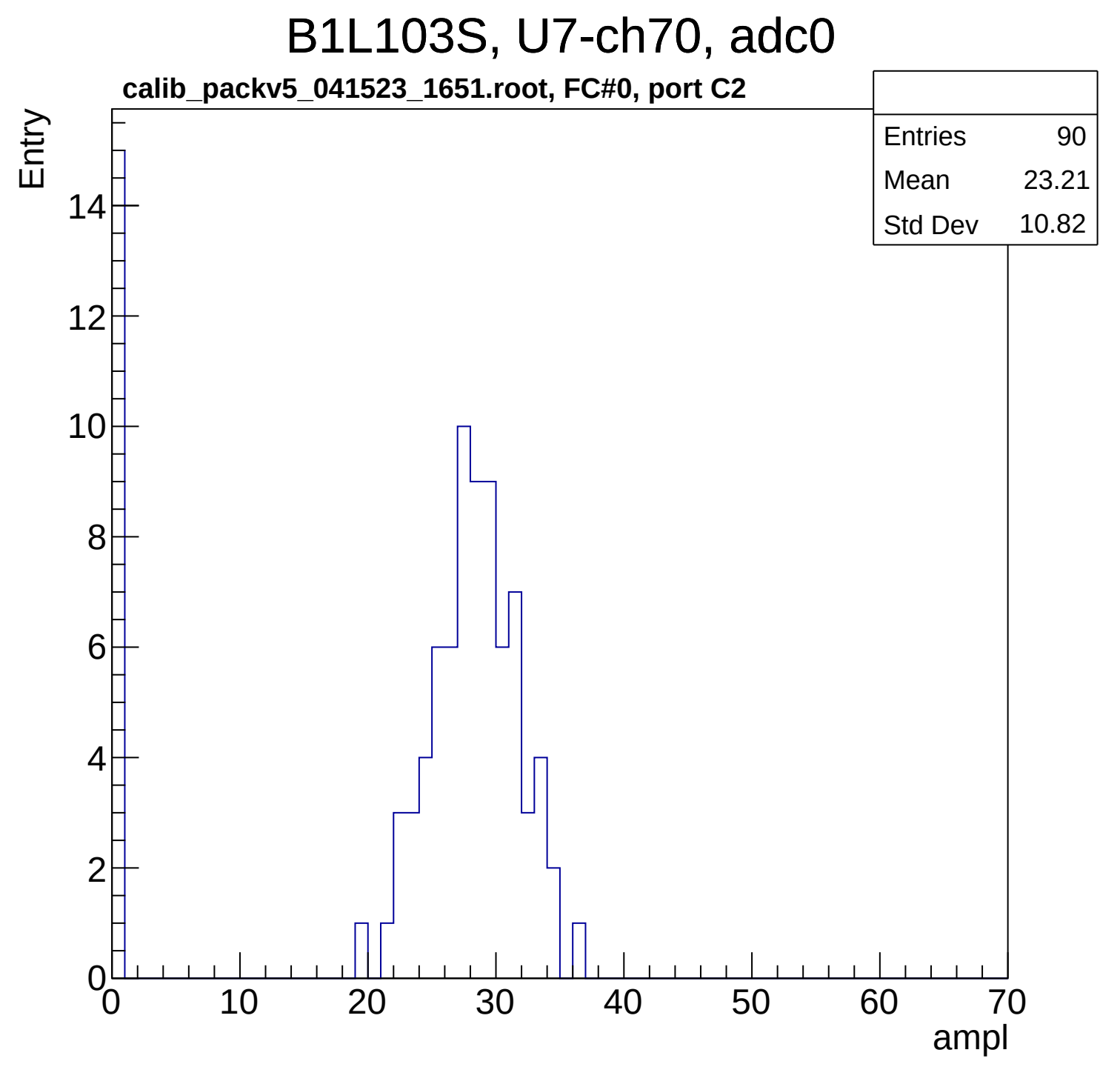
50
60
70
ampl


B1L103S, U7-ch70, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 90
Mean 23.21
Std Dev 10.82
Entry
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4
6
8
10
12
14
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10
20
30
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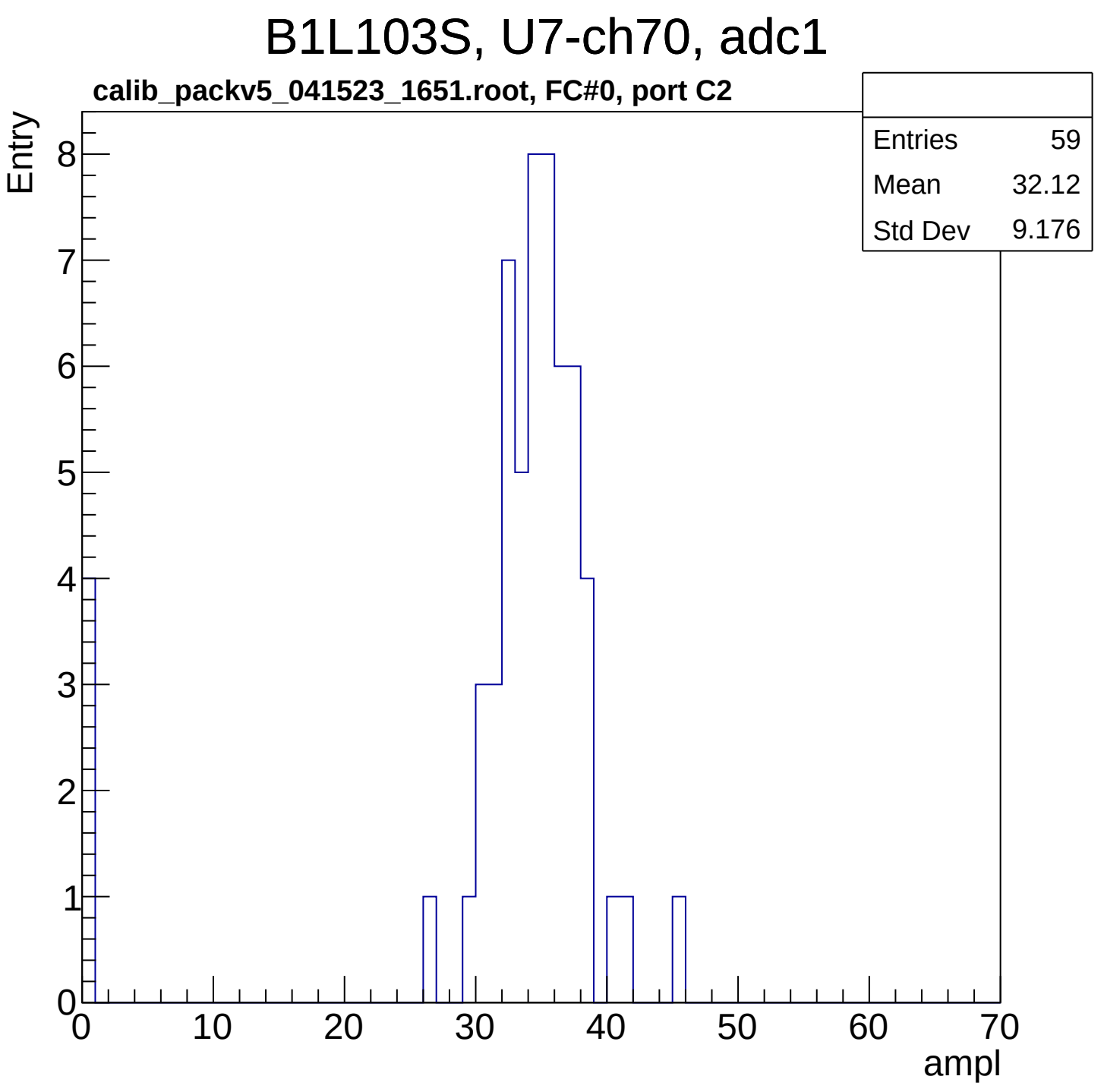
50
60
70
ampl


B1L103S, U7-ch70, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 32.12
Std Dev 9.176
Entry
ampl
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2
3
4
5
6
7
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0
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20
30
40
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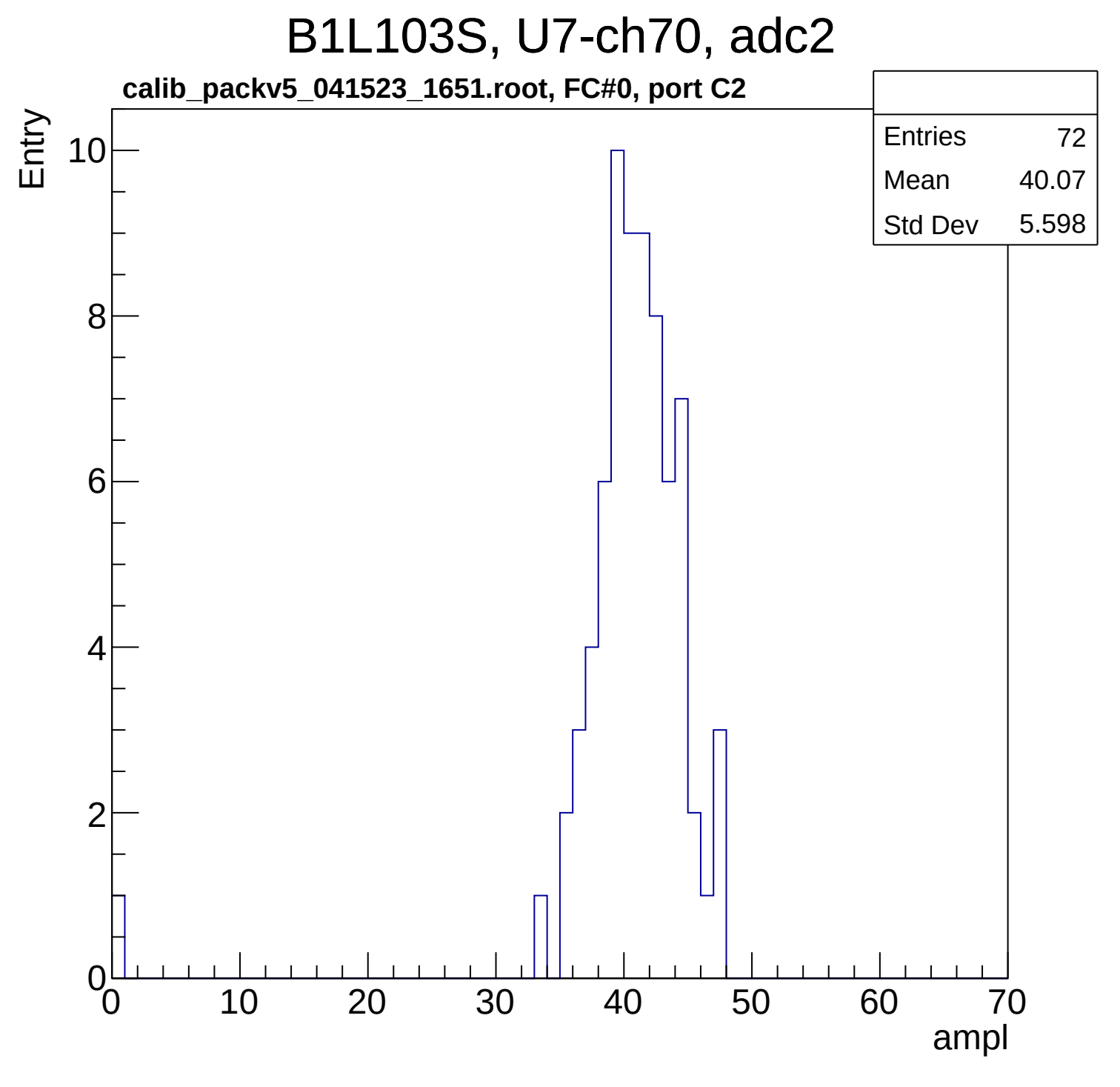
60
70


B1L103S, U7-ch70, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 40.07
Std Dev 5.598
Entry
ampl
0
2
4
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8
10
0
10
20
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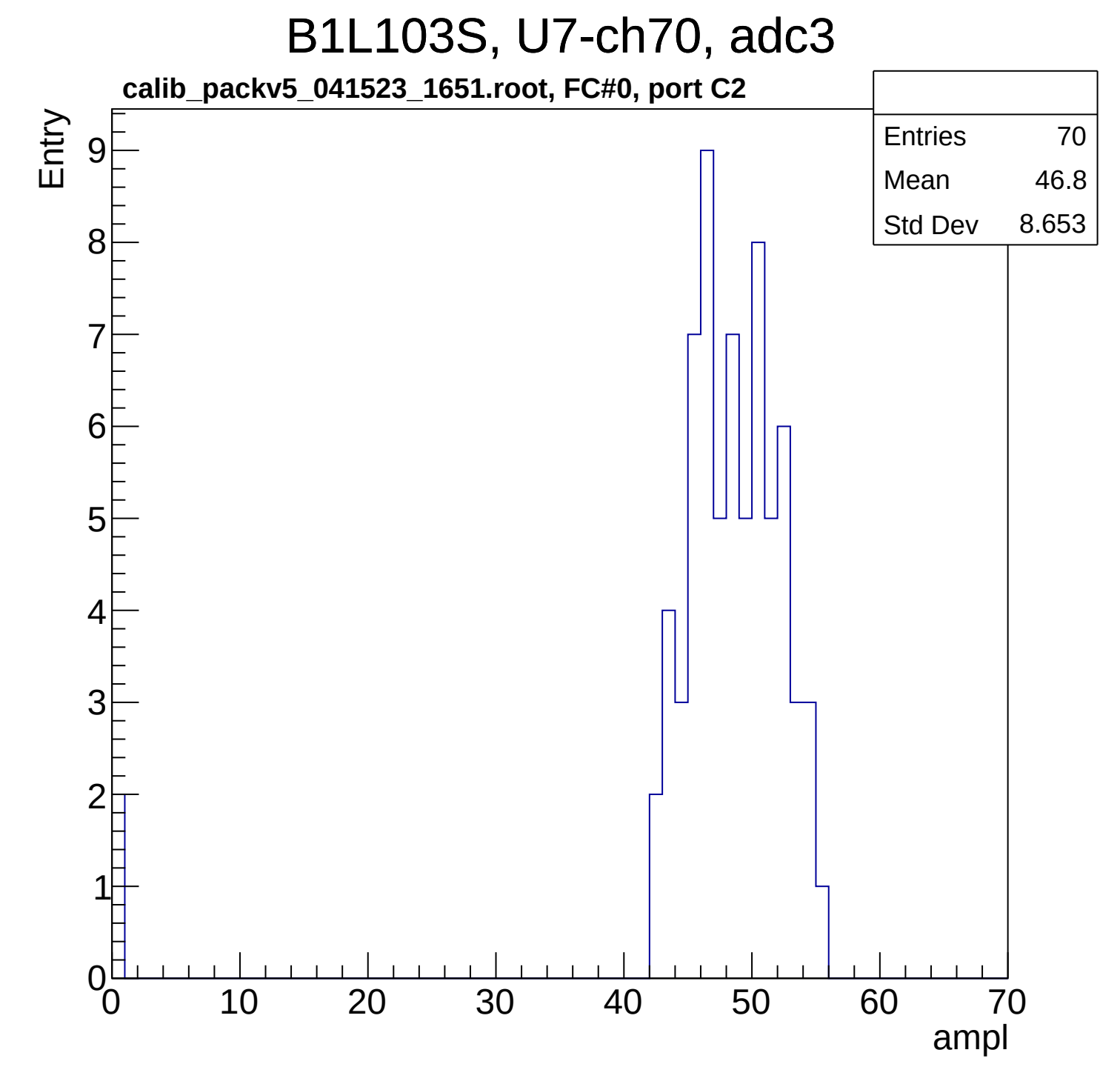
40
50
60
70


B1L103S, U7-ch70, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 46.8
Std Dev 8.653
Entry
ampl
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3
4
5
6
7
8
9
0
10
20
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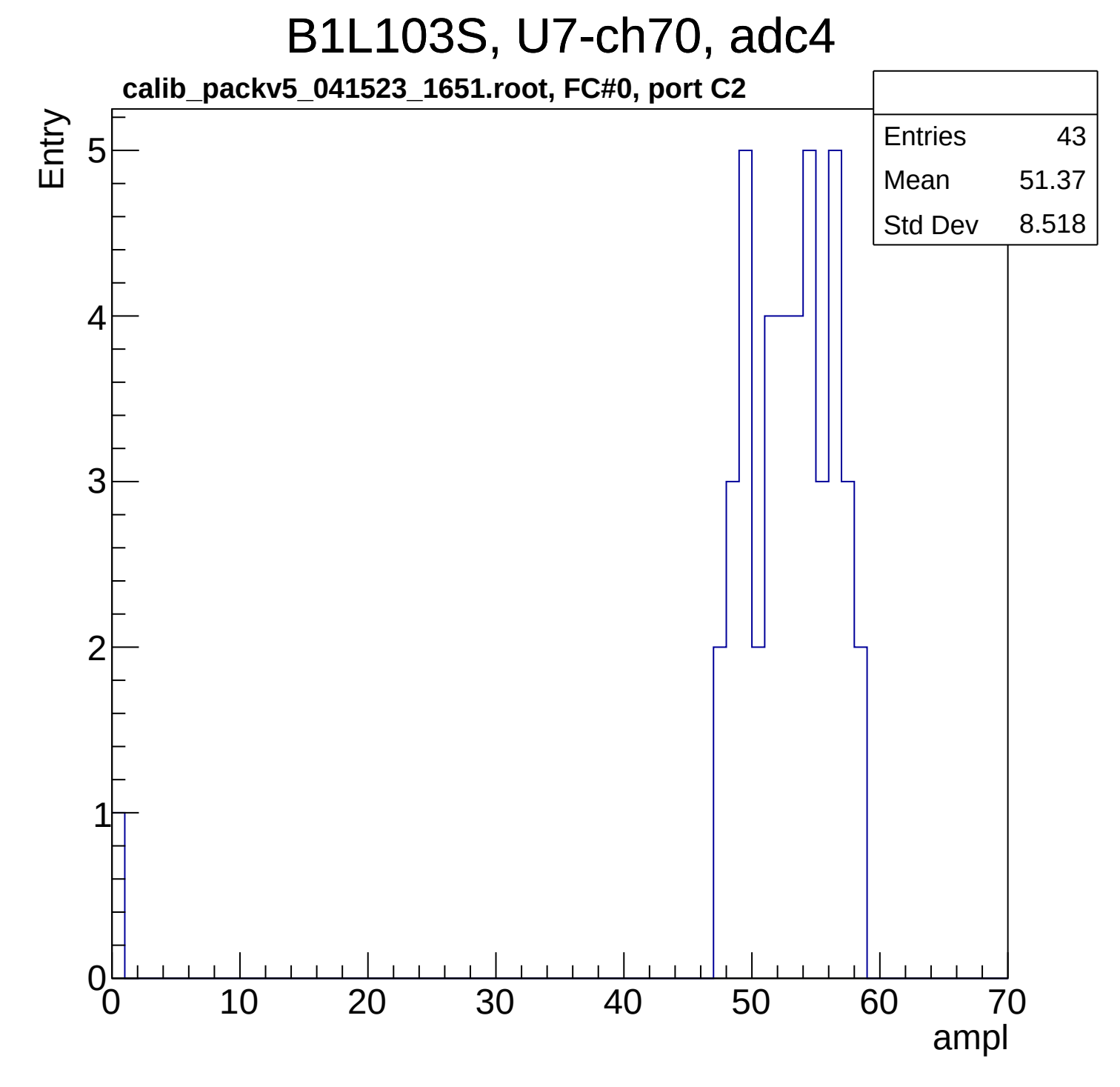
40
50
60
70


B1L103S, U7-ch70, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 43
Mean 51.37
Std Dev 8.518
Entry
ampl
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2
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4
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0
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20
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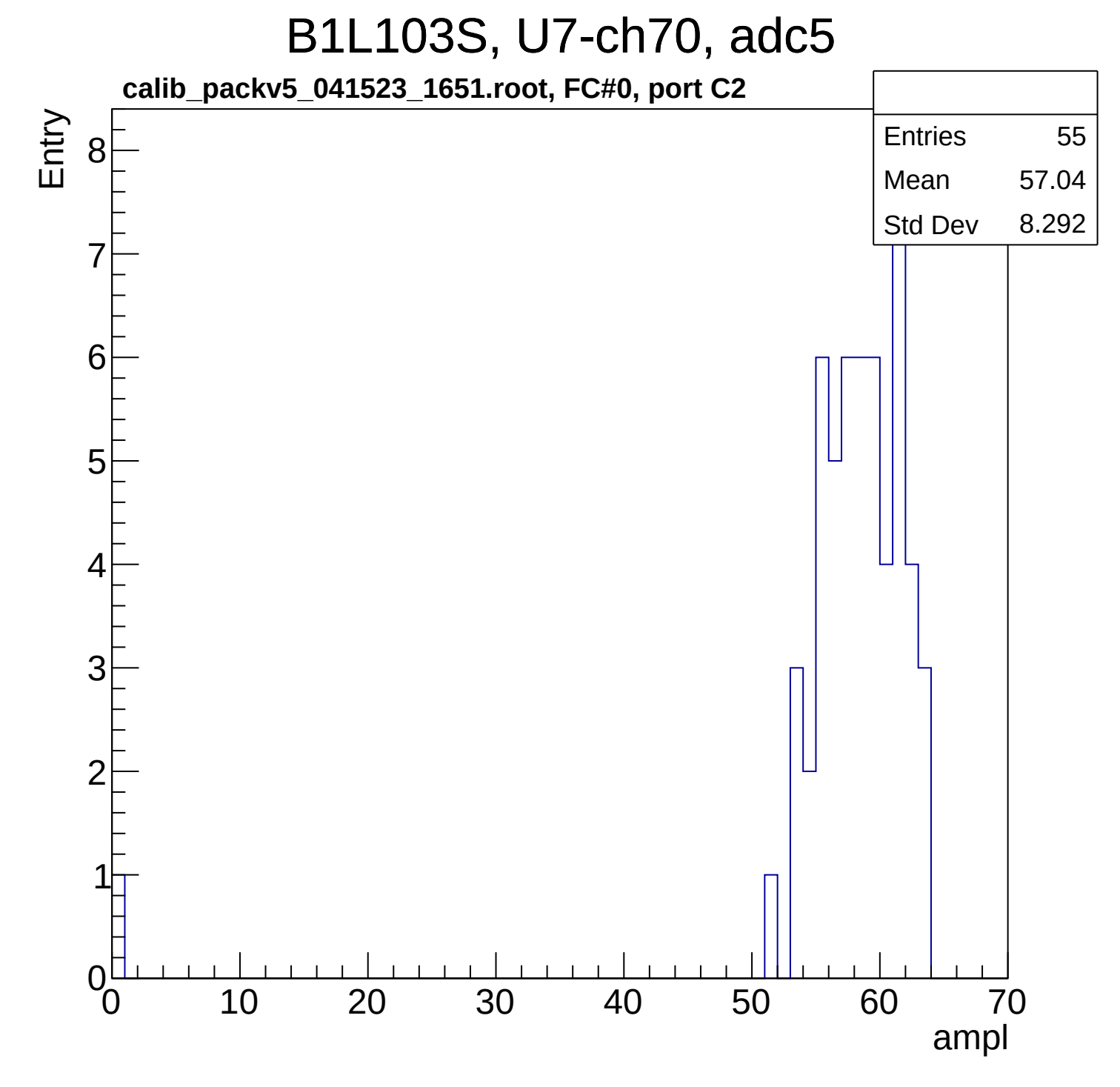
40
50
60
70


B1L103S, U7-ch70, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 57.04
Std Dev 8.292
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
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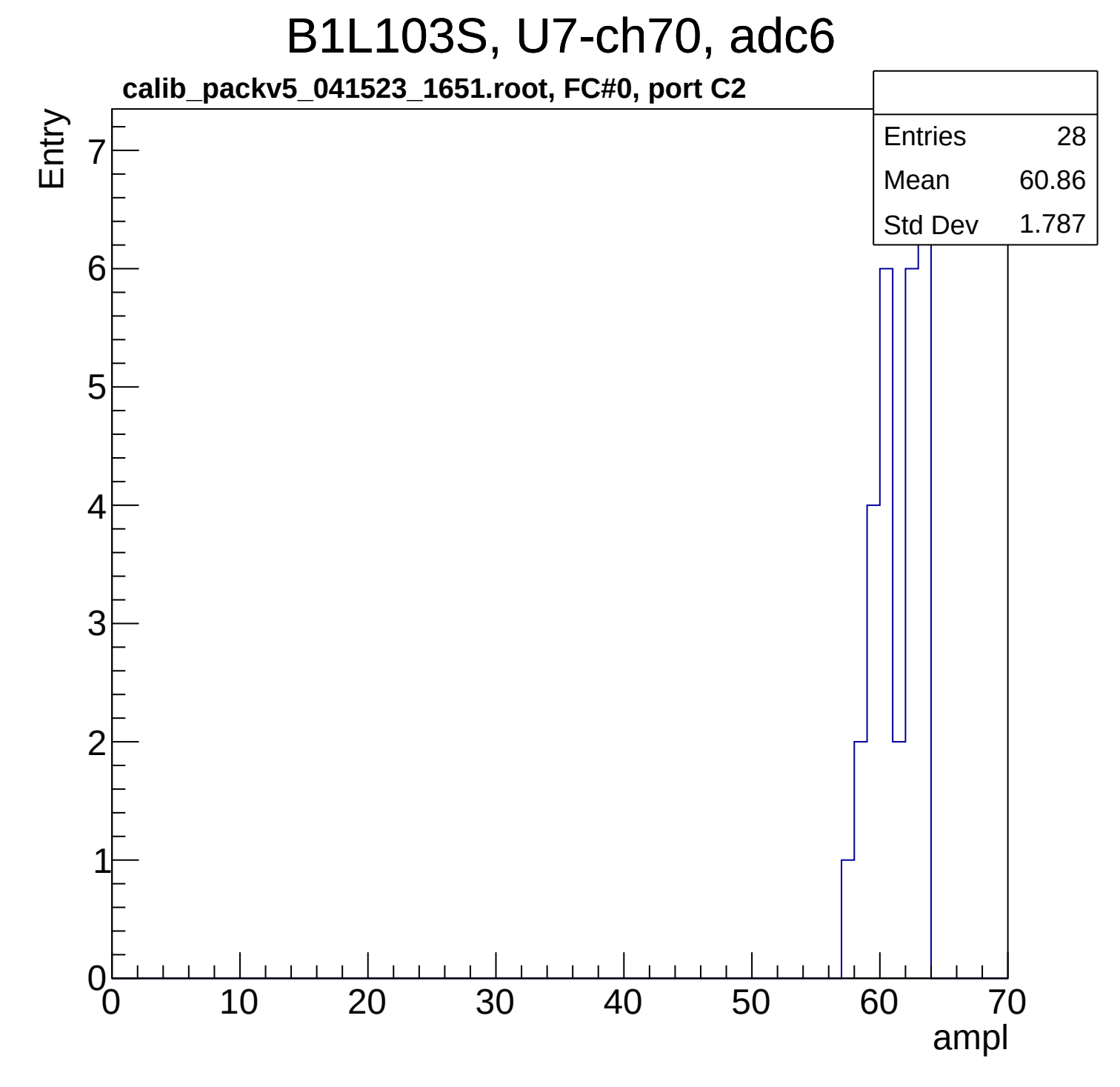
50
60
70


B1L103S, U7-ch70, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 28
Mean 60.86
Std Dev 1.787
Entry
ampl
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4
5
6
7
0
10
20
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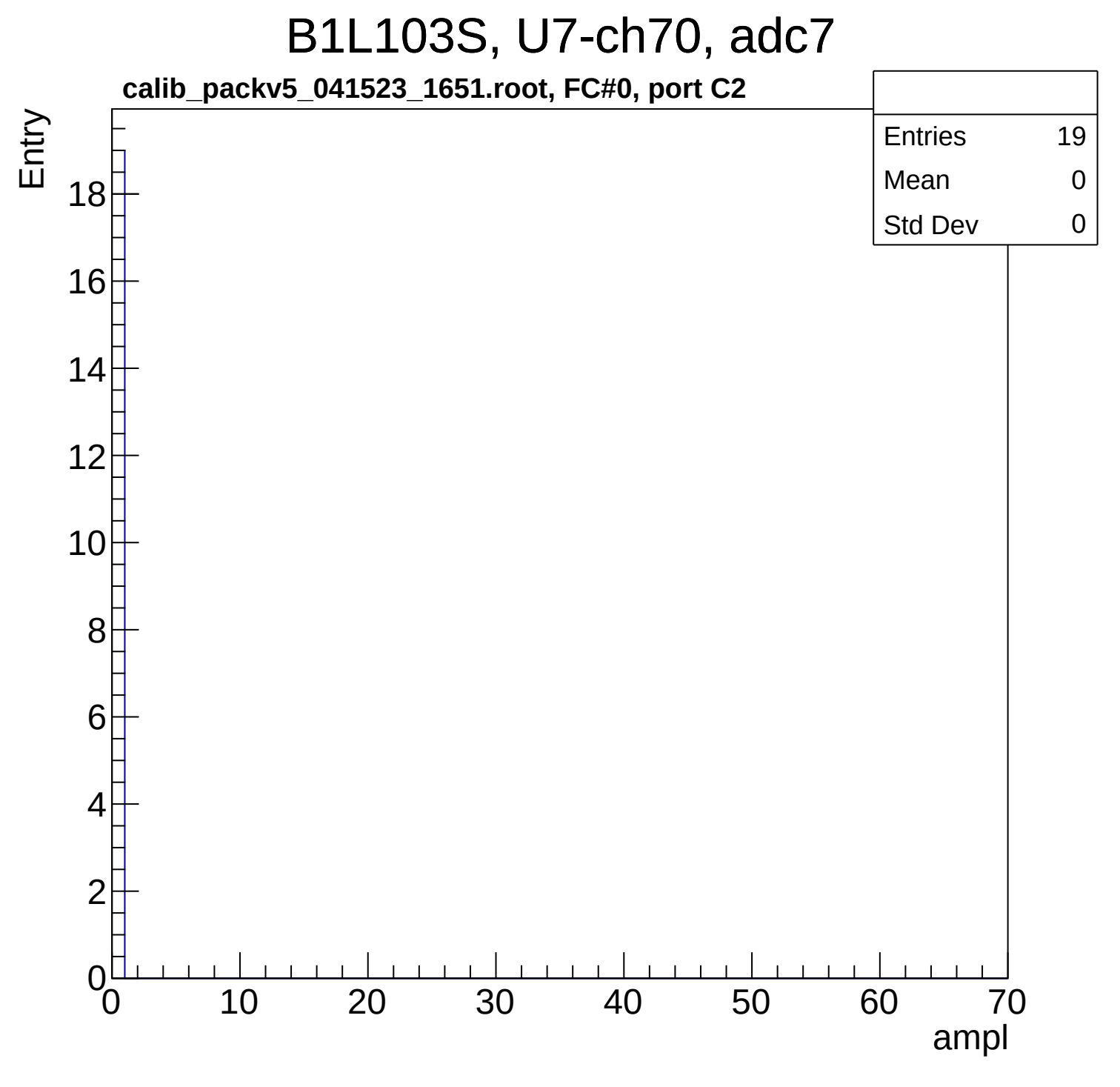
40
50
60
70


B1L103S, U7-ch70, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
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6
8
10
12
14
16
18
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10
20
30
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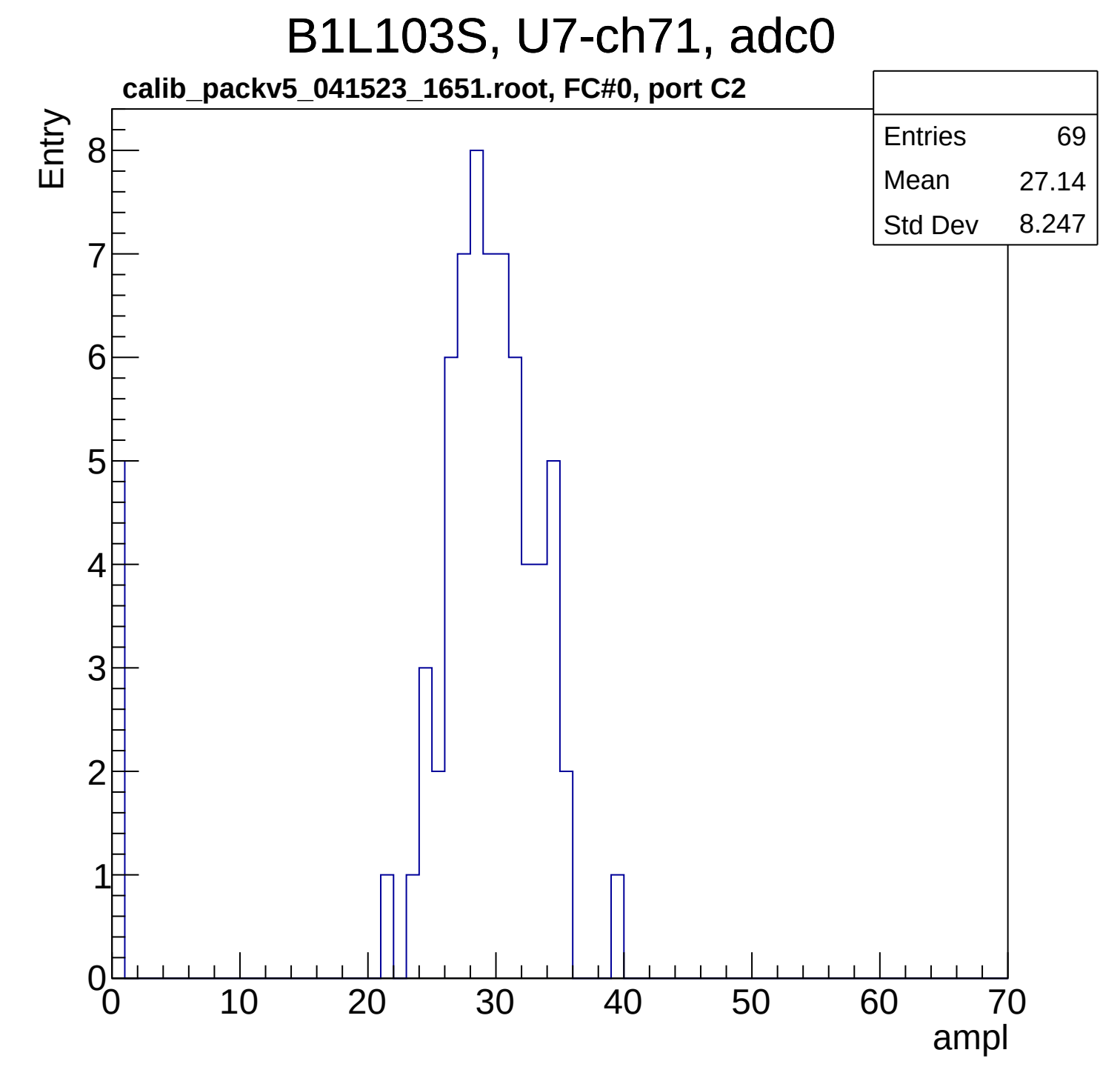
50
60
70
ampl


B1L103S, U7-ch71, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 27.14
Std Dev 8.247
Entry
ampl
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2
3
4
5
6
7
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0
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20
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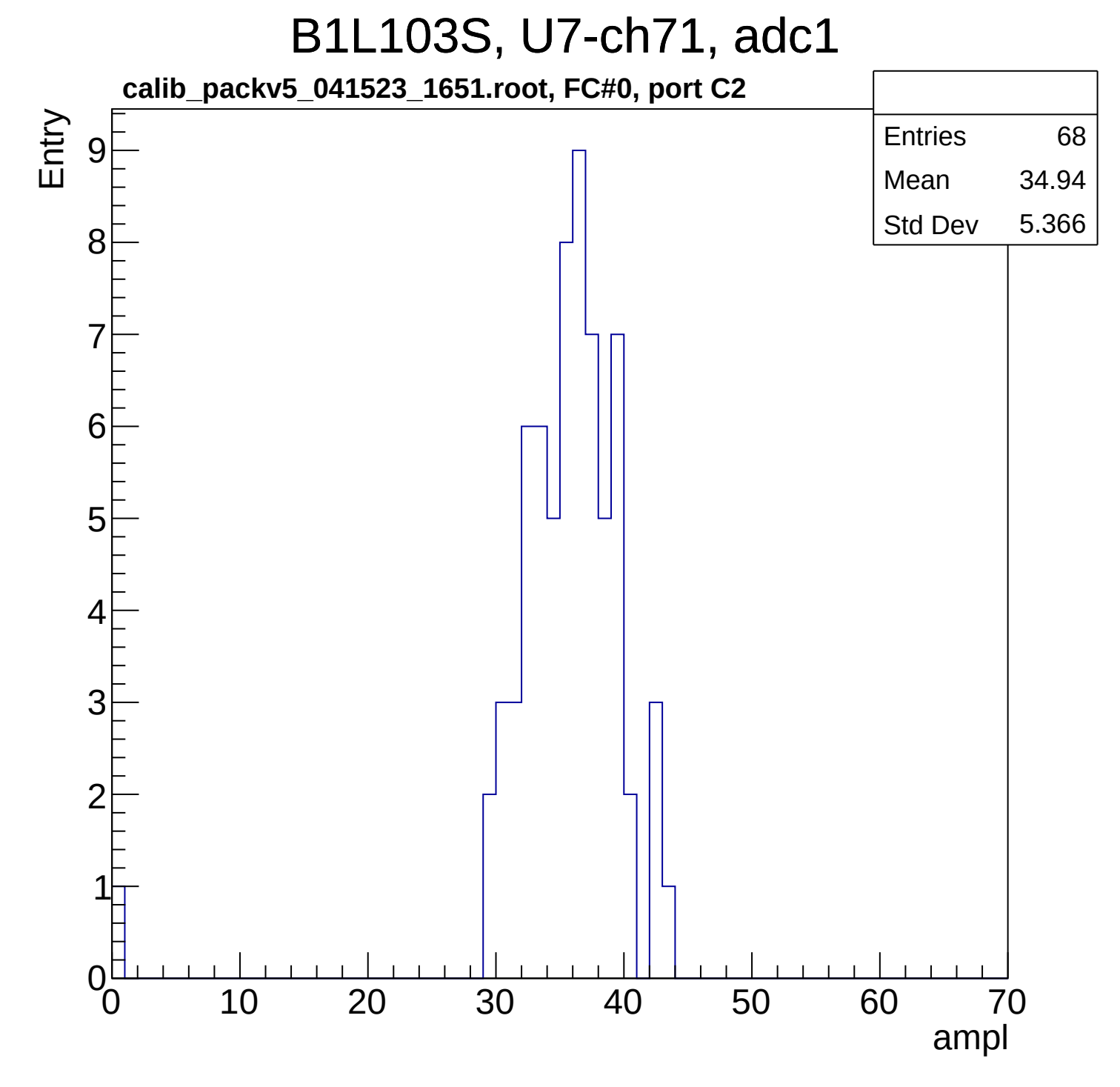
40
50
60
70


B1L103S, U7-ch71, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 34.94
Std Dev 5.366
Entry
ampl
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3
4
5
6
7
8
9
0
10
20
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40
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60
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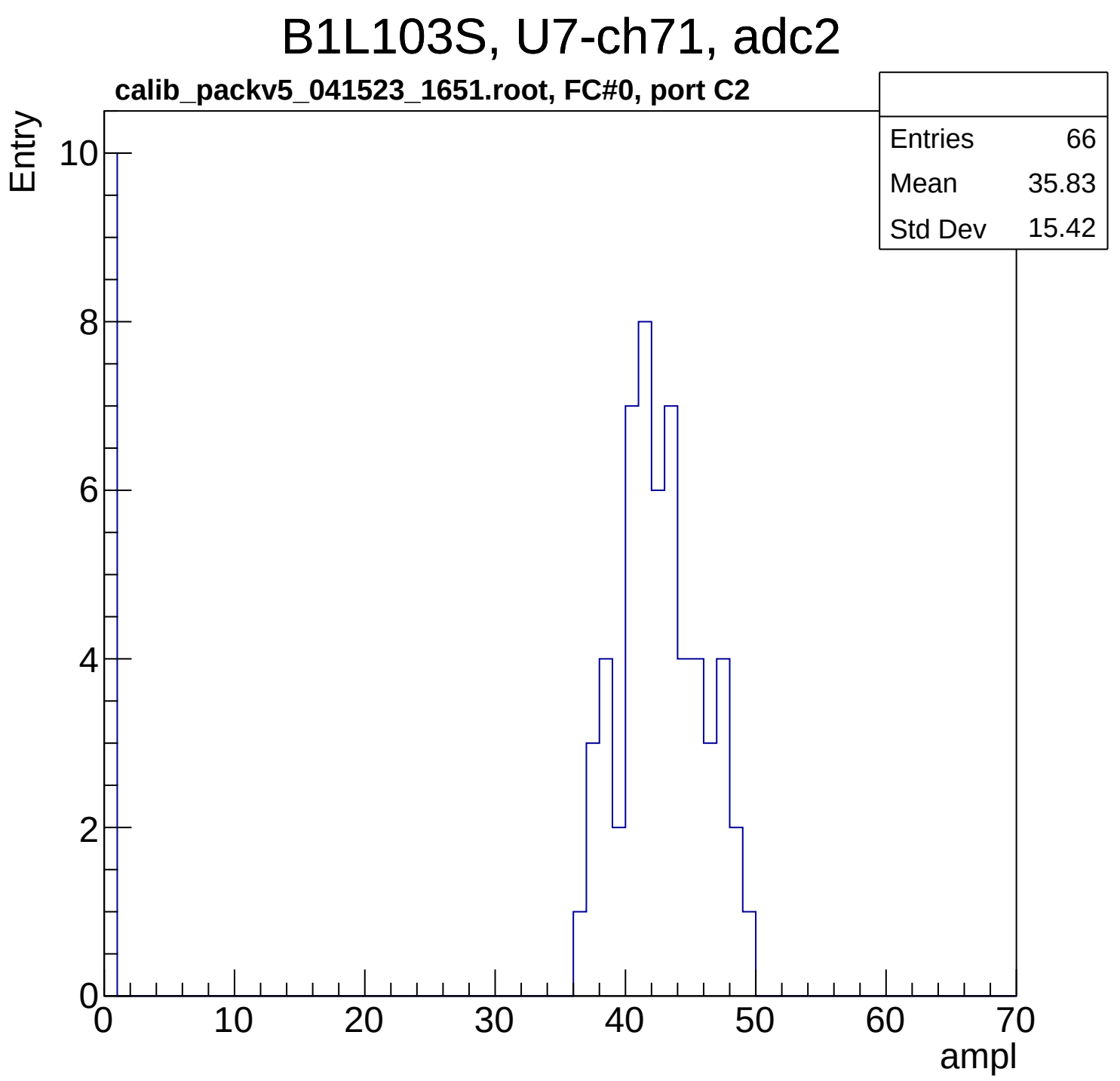
B1L103S, U7-ch71, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 35.83
Std Dev 15.42
Entry
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6
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10
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10
20
30
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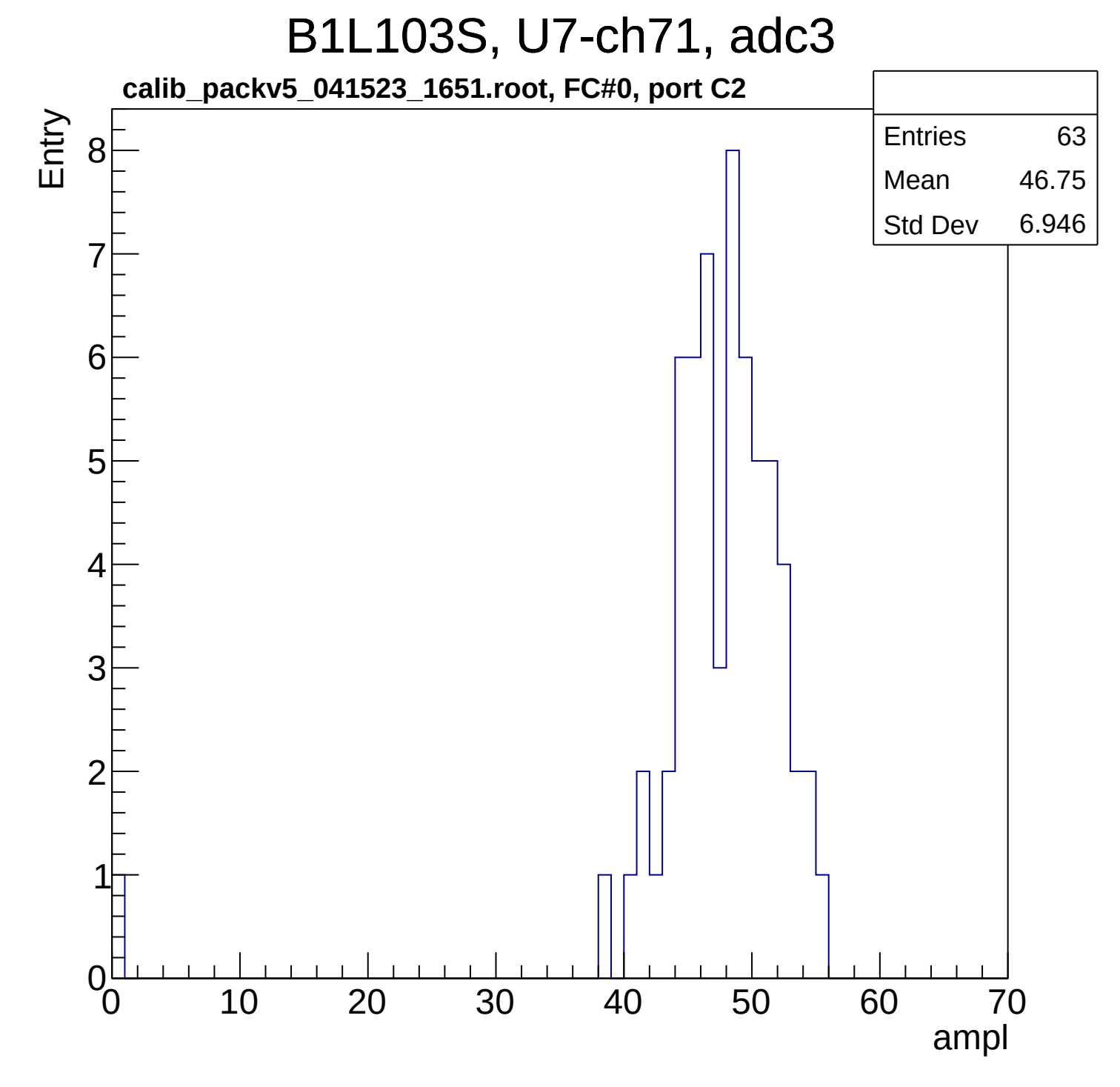
50
60
70
ampl


B1L103S, U7-ch71, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 46.75
Std Dev 6.946
Entry
ampl
0
1
2
3
4
5
6
7
8
0
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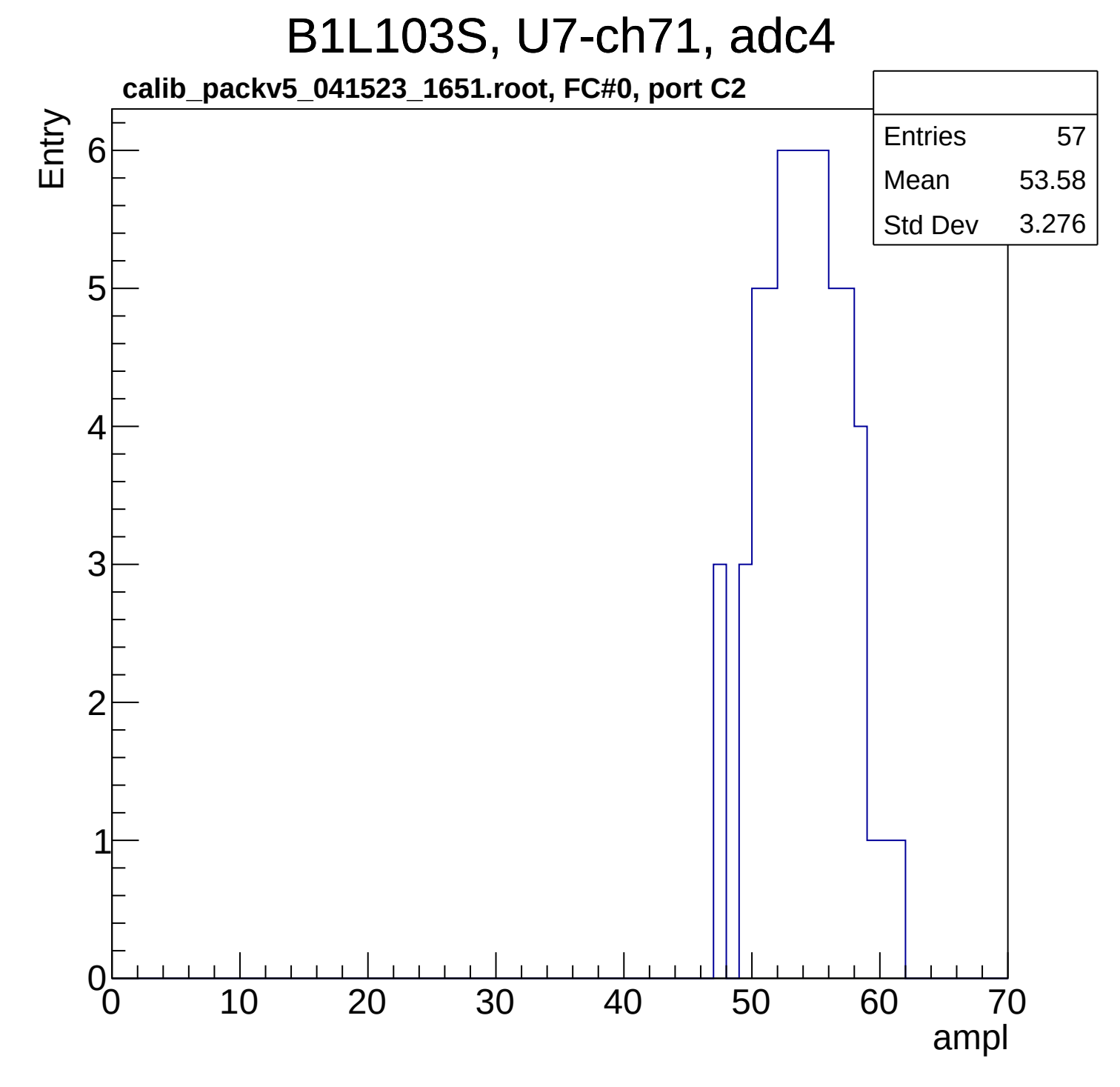
40
50
60
70


B1L103S, U7-ch71, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 53.58
Std Dev 3.276
Entry
ampl
0
1
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3
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5
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0
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60
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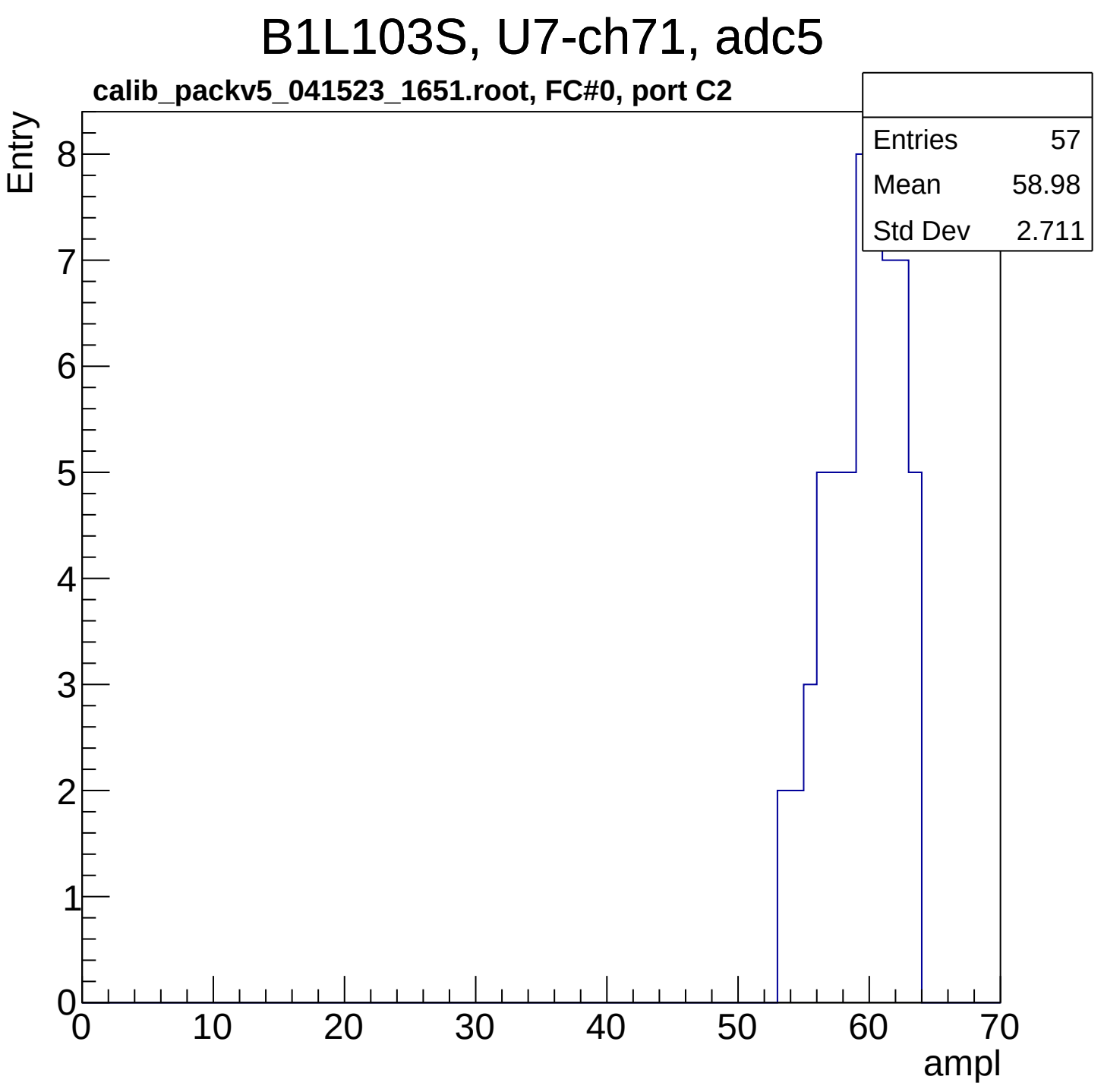
B1L103S, U7-ch71, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 58.98
Std Dev 2.711
Entry
ampl
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2
3
4
5
6
7
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0
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40
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60
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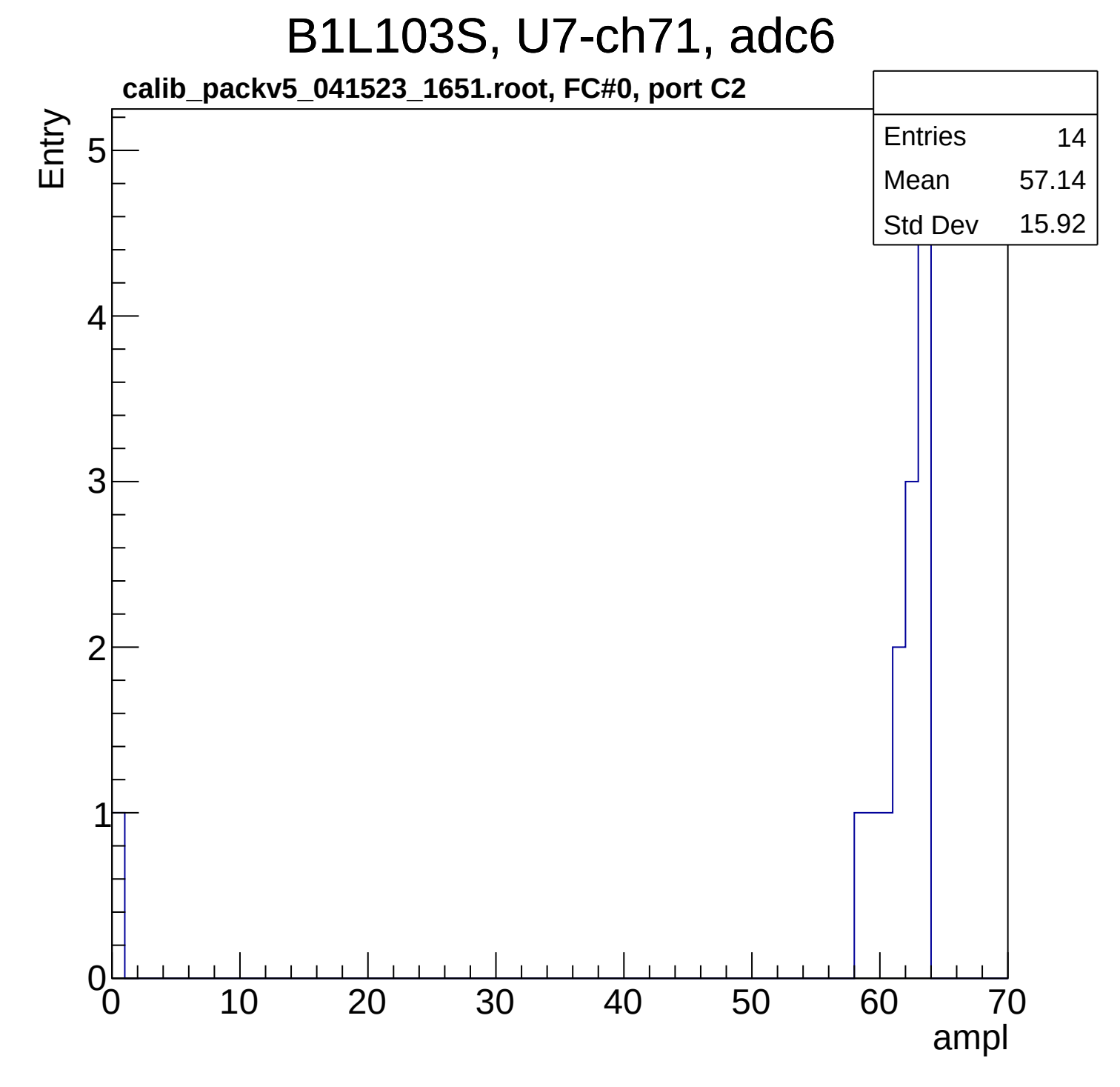
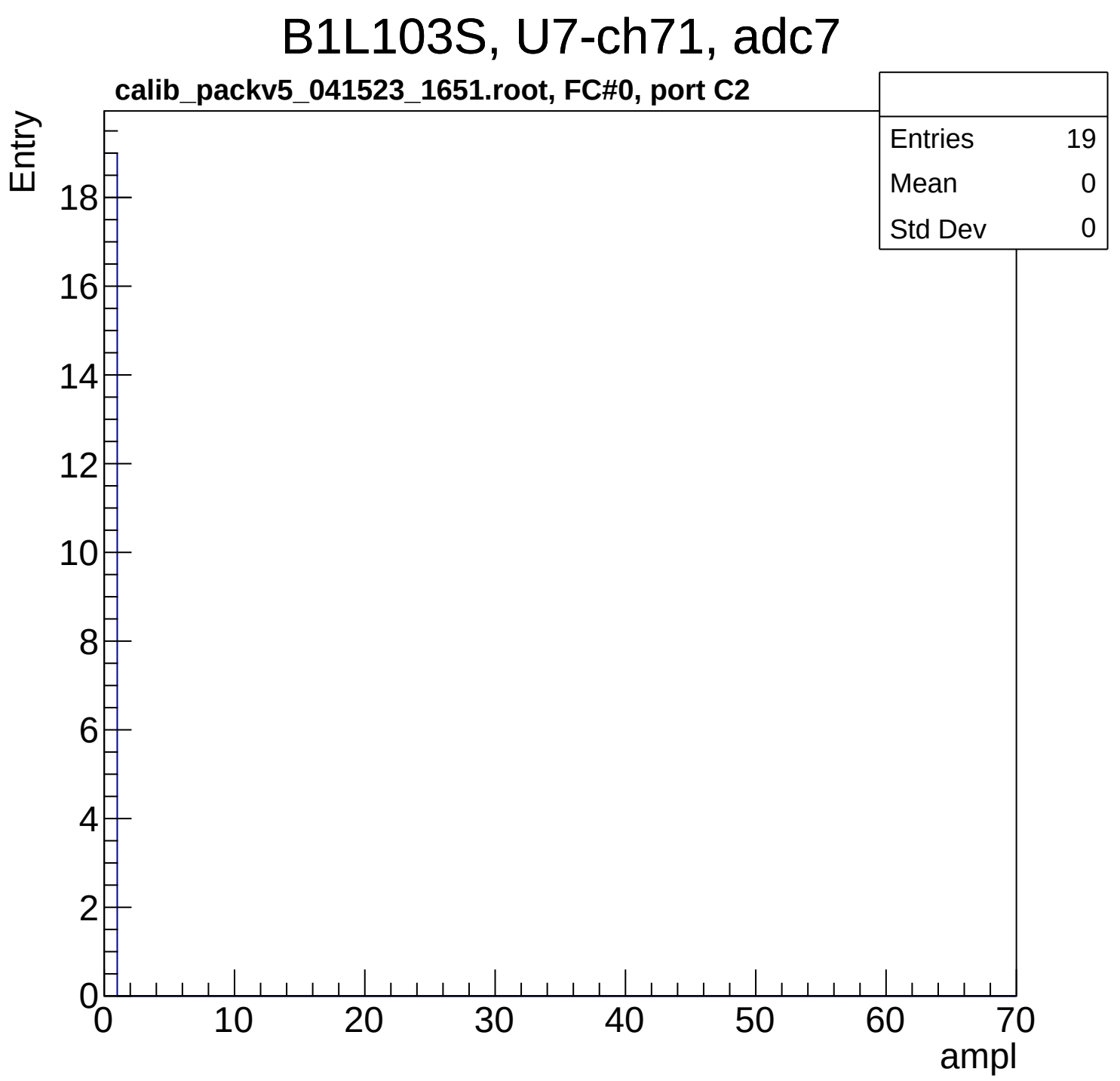
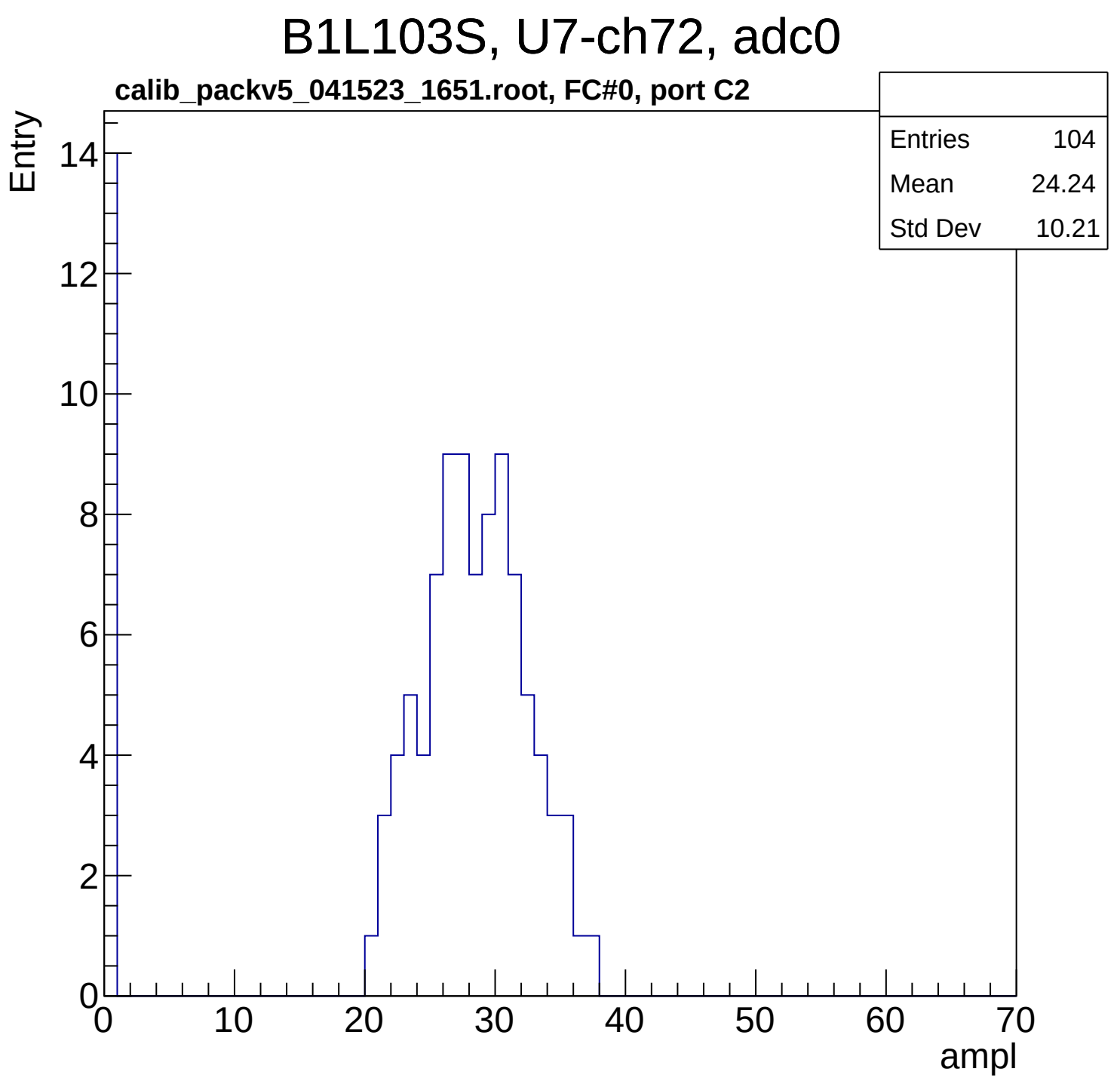

B1L103S, U7-ch71, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 14
Mean 57.14
Std Dev 15.92
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch71, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch72, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 104
Mean 24.24
Std Dev 10.21
Entry
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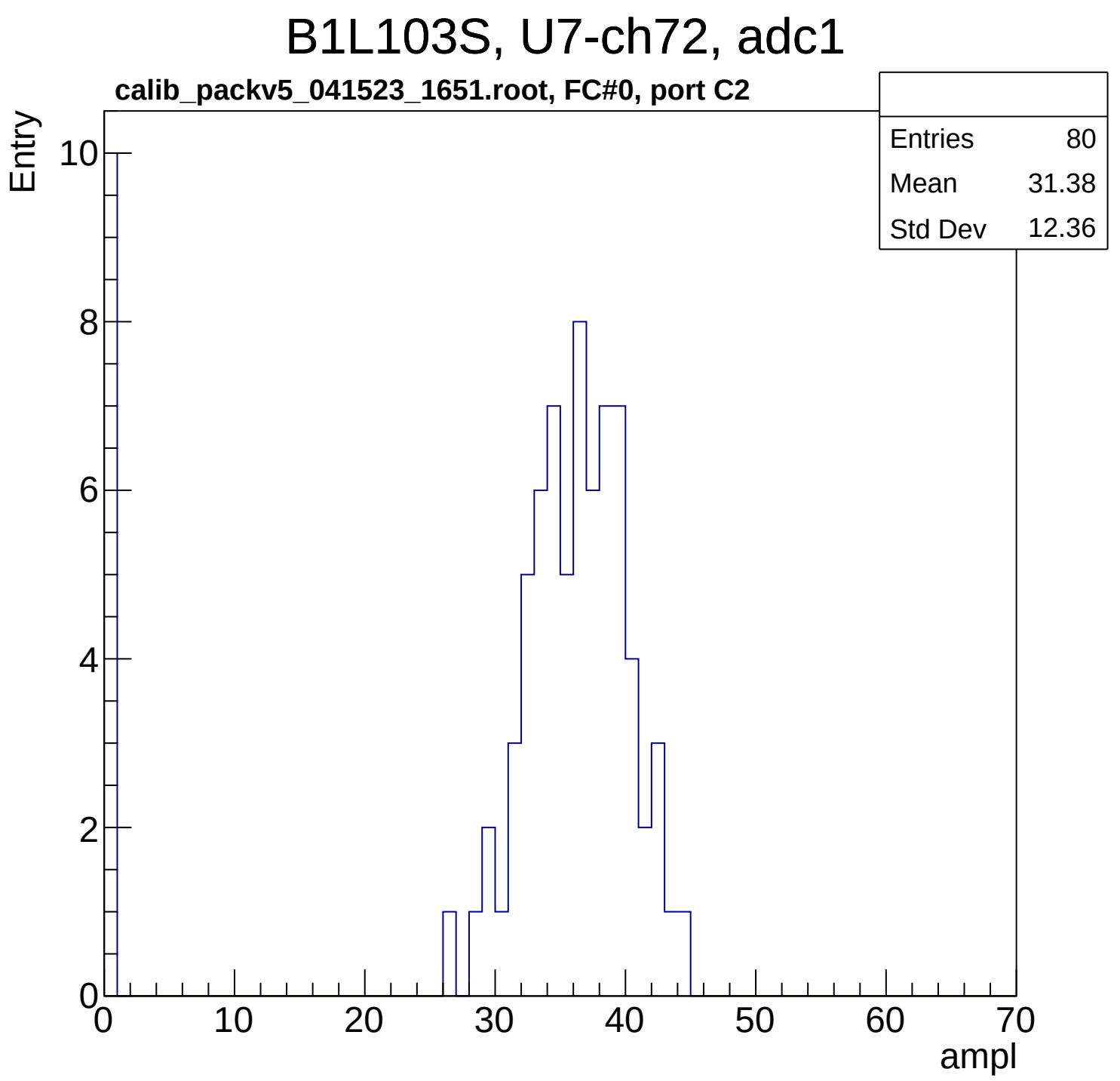
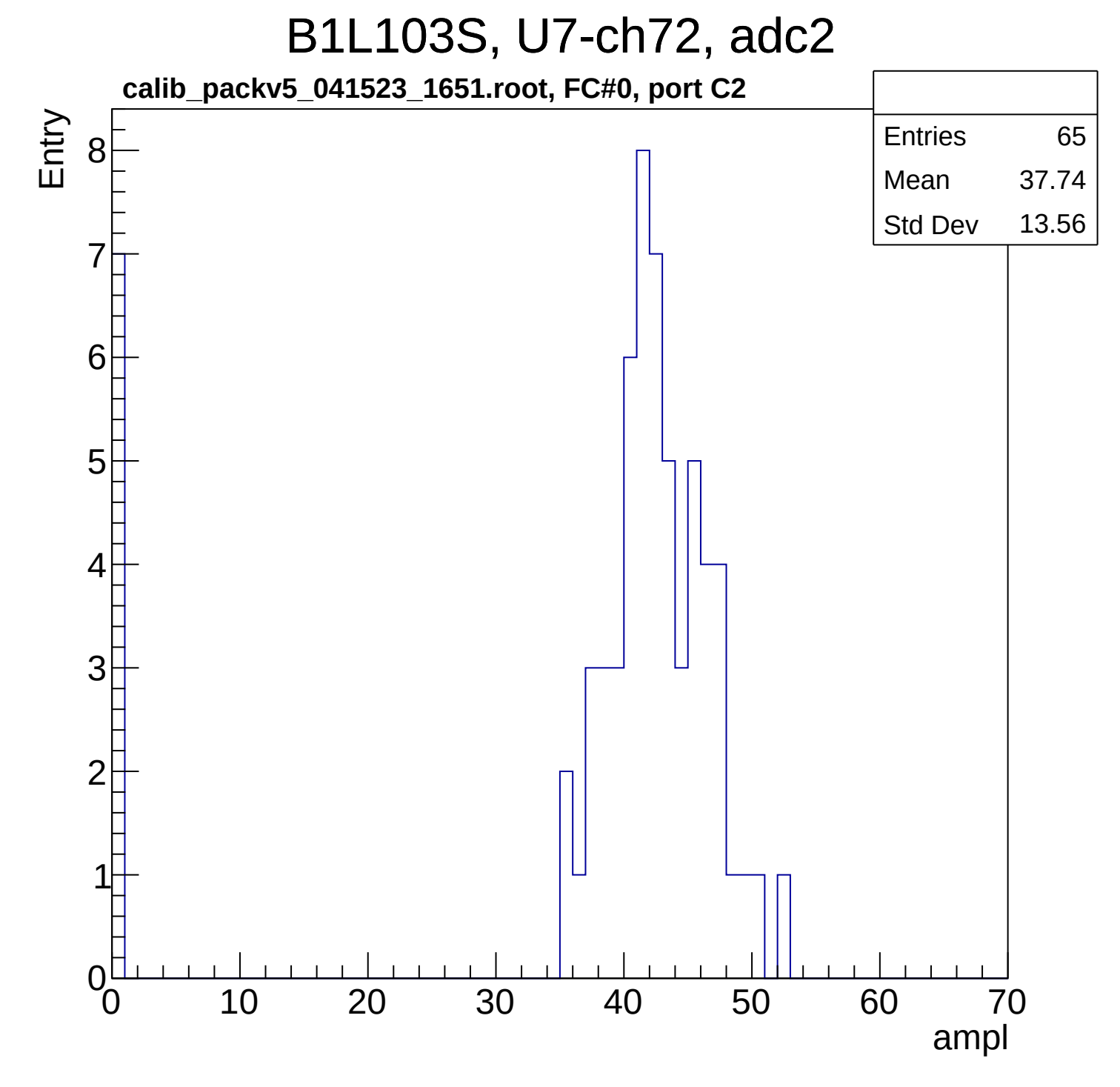
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch72, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 31.38
Std Dev 12.36
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U7-ch72, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 37.74
Std Dev 13.56
Entry
ampl
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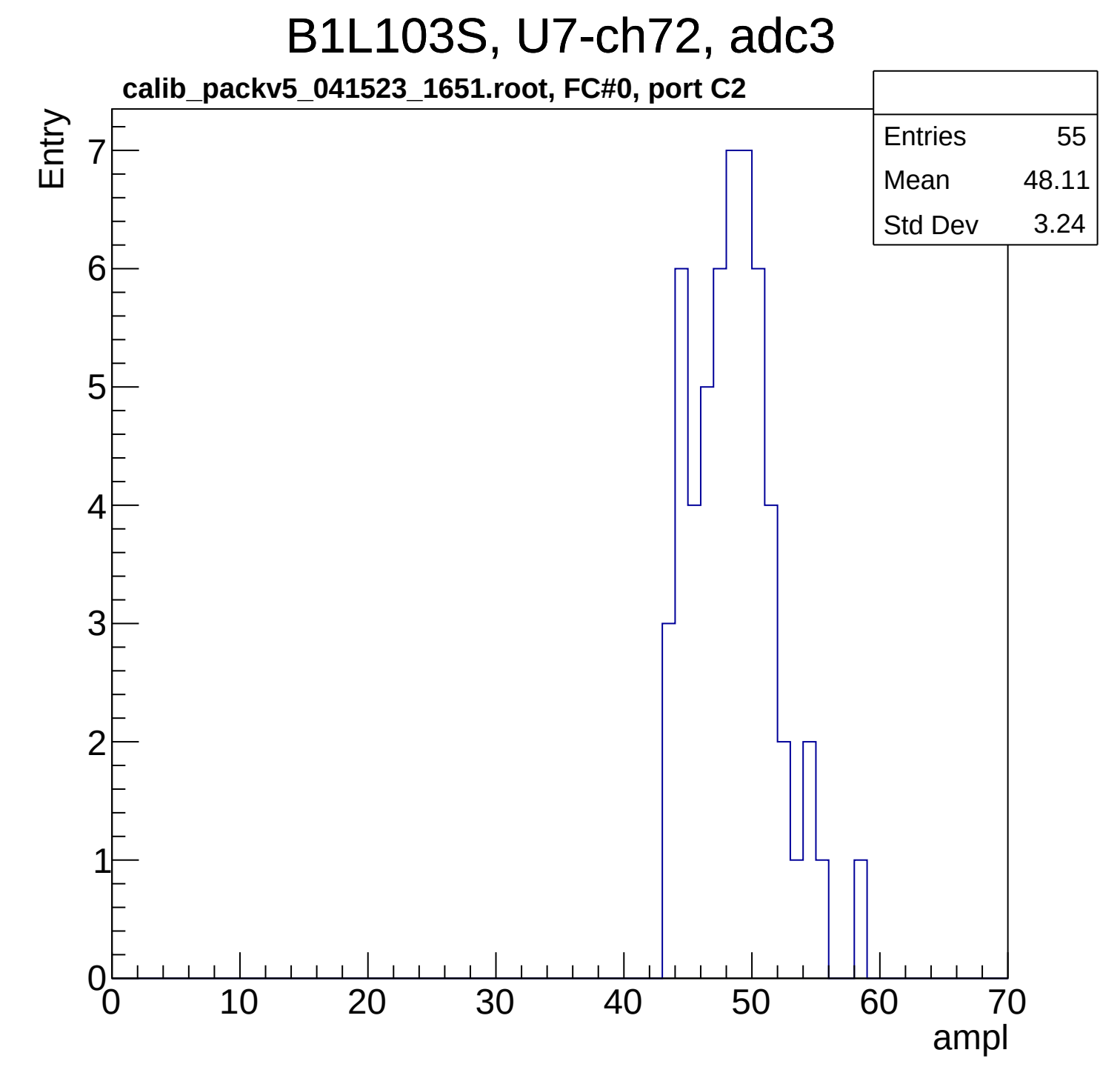
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch72, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 48.11
Std Dev 3.24
Entry
ampl
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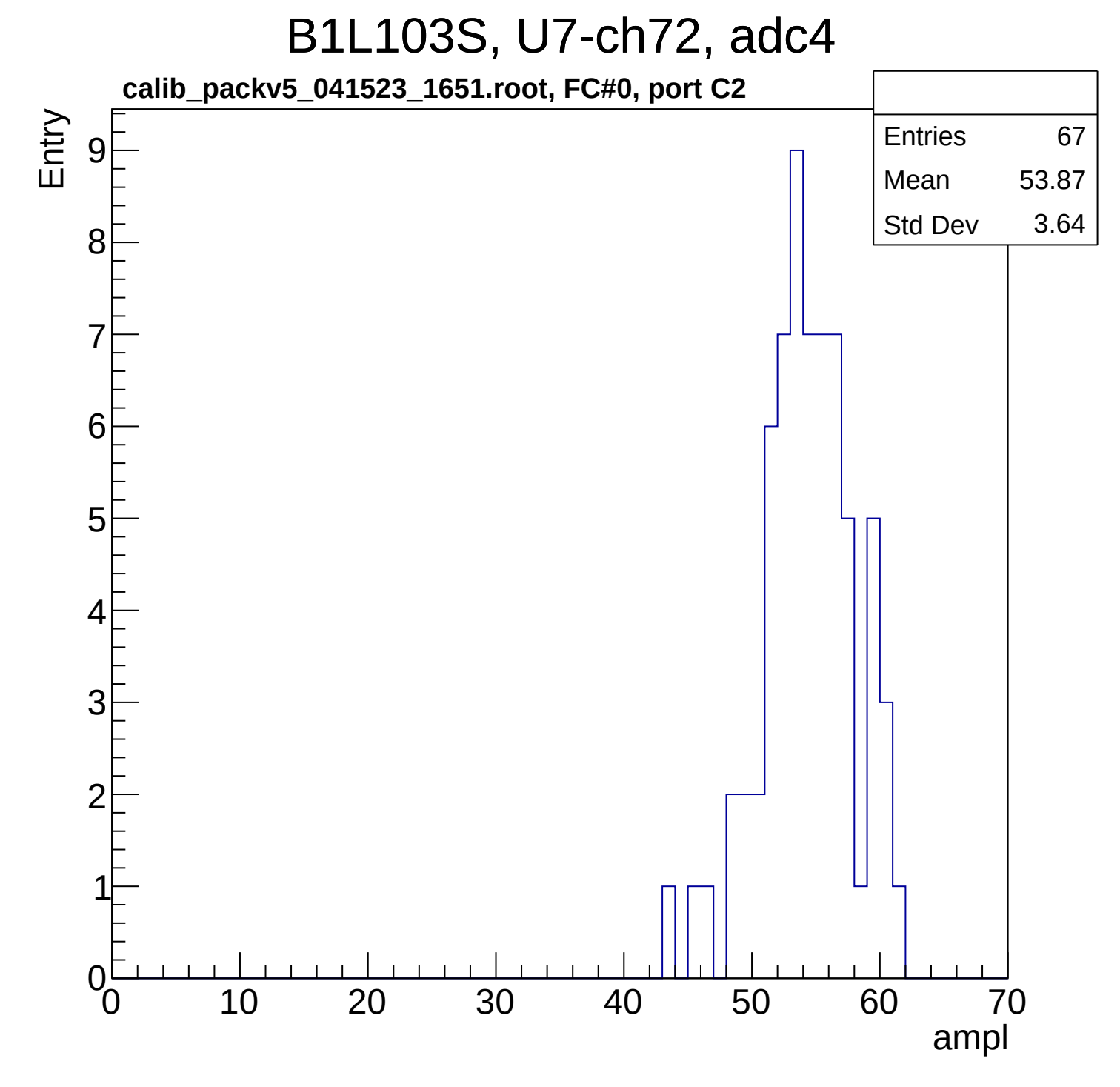
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U7-ch72, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 53.87
Std Dev 3.64
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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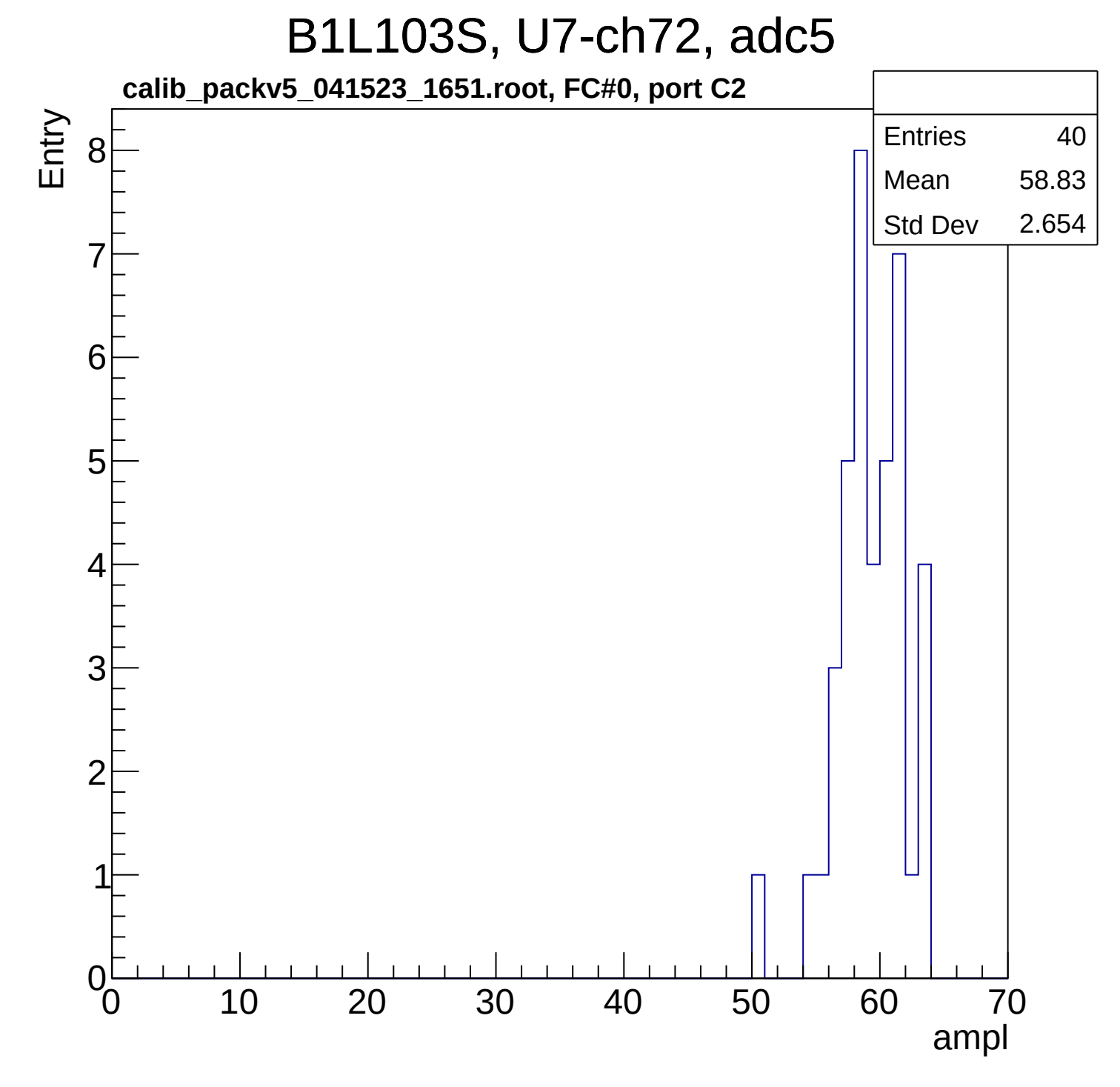
B1L103S, U7-ch72, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 40
Mean 58.83
Std Dev 2.654
Entry
ampl
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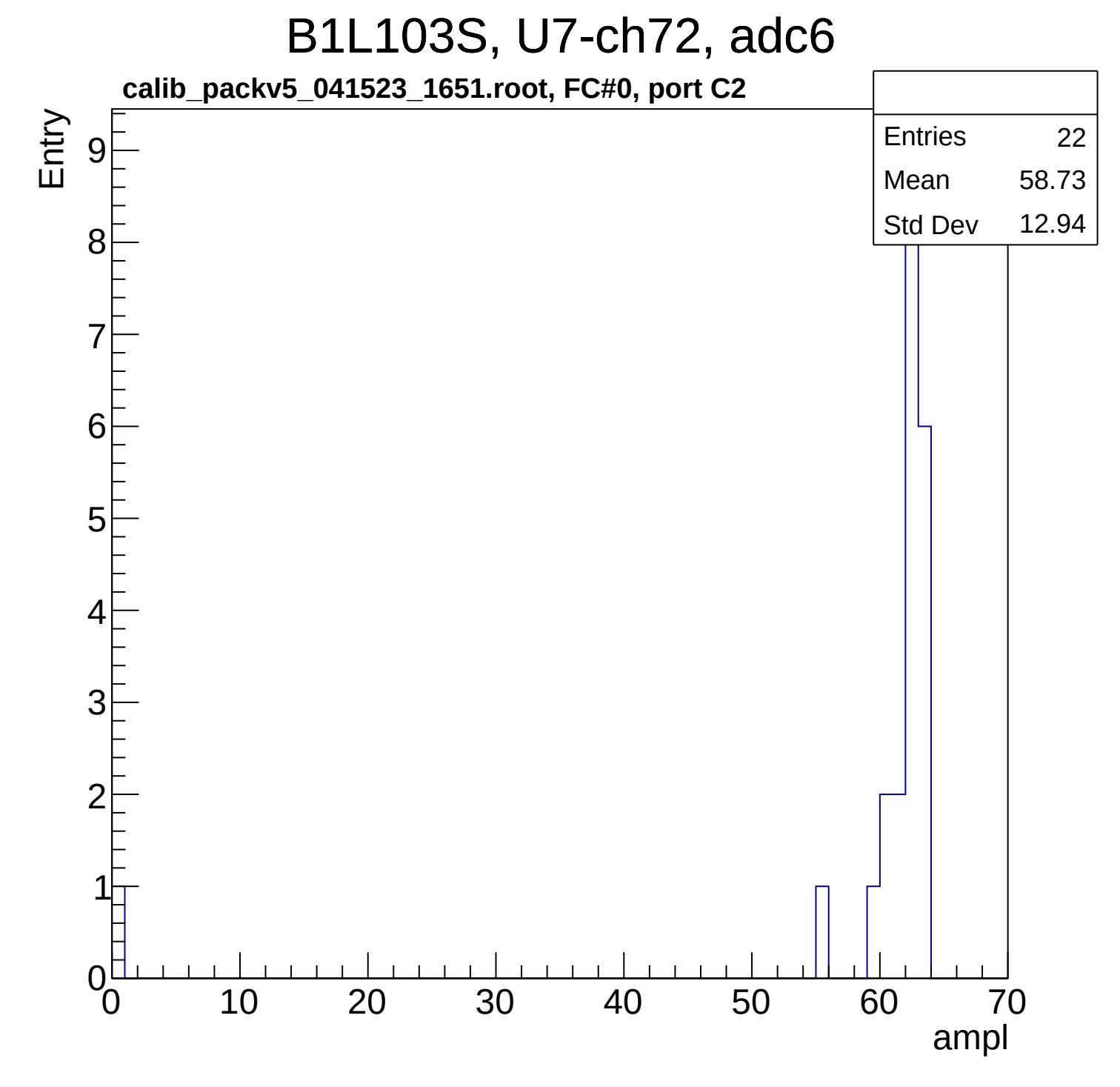
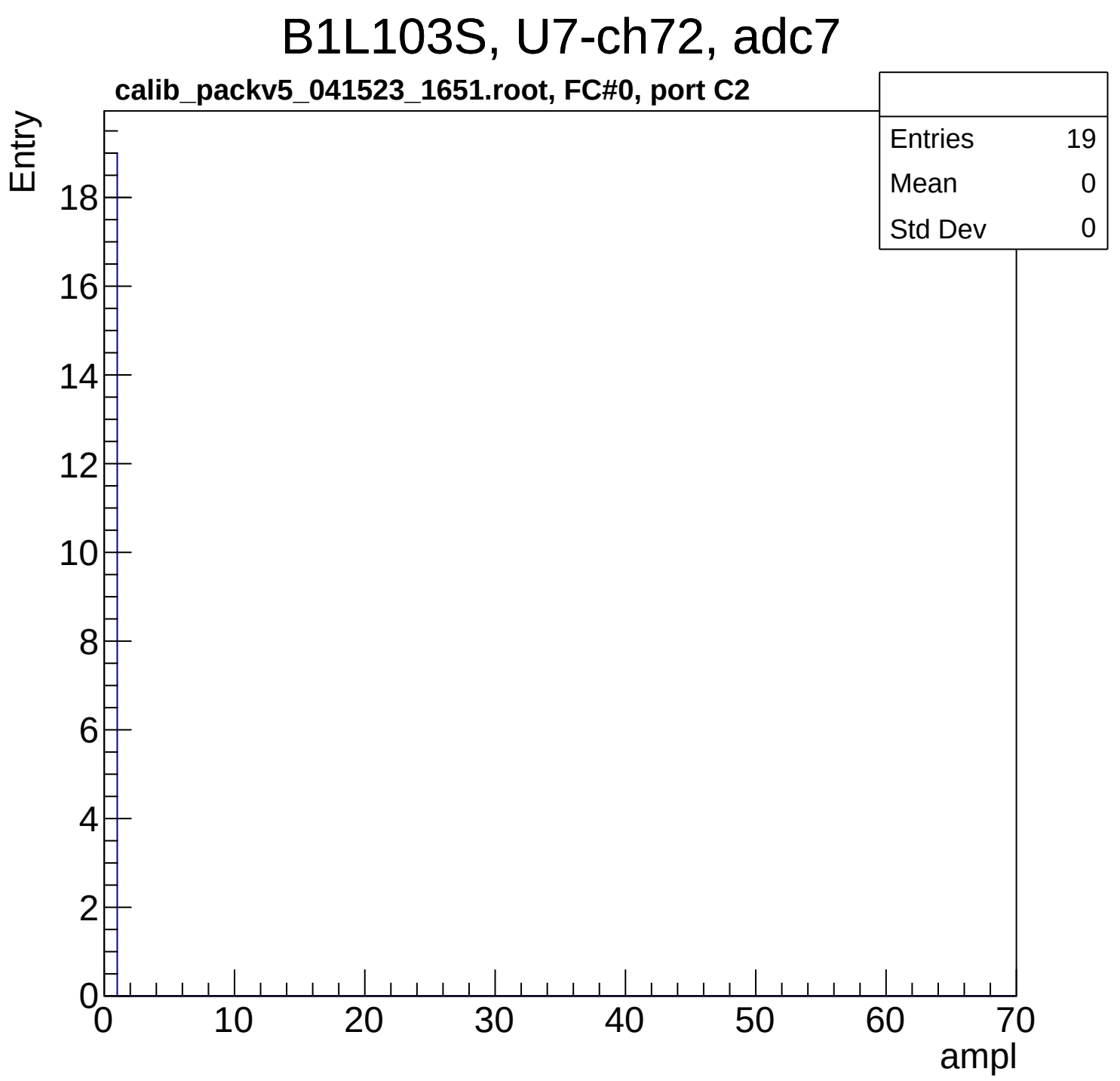
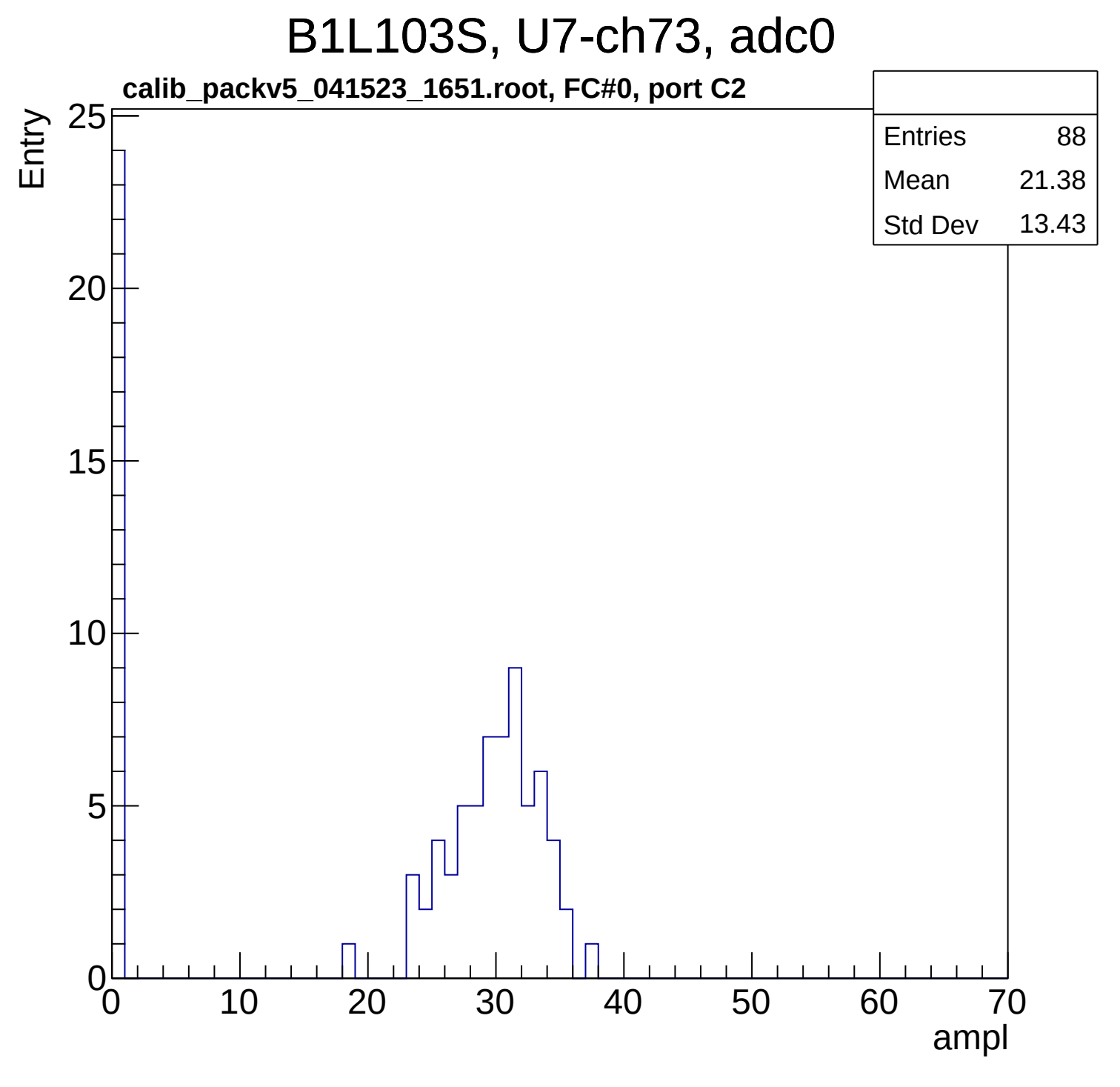
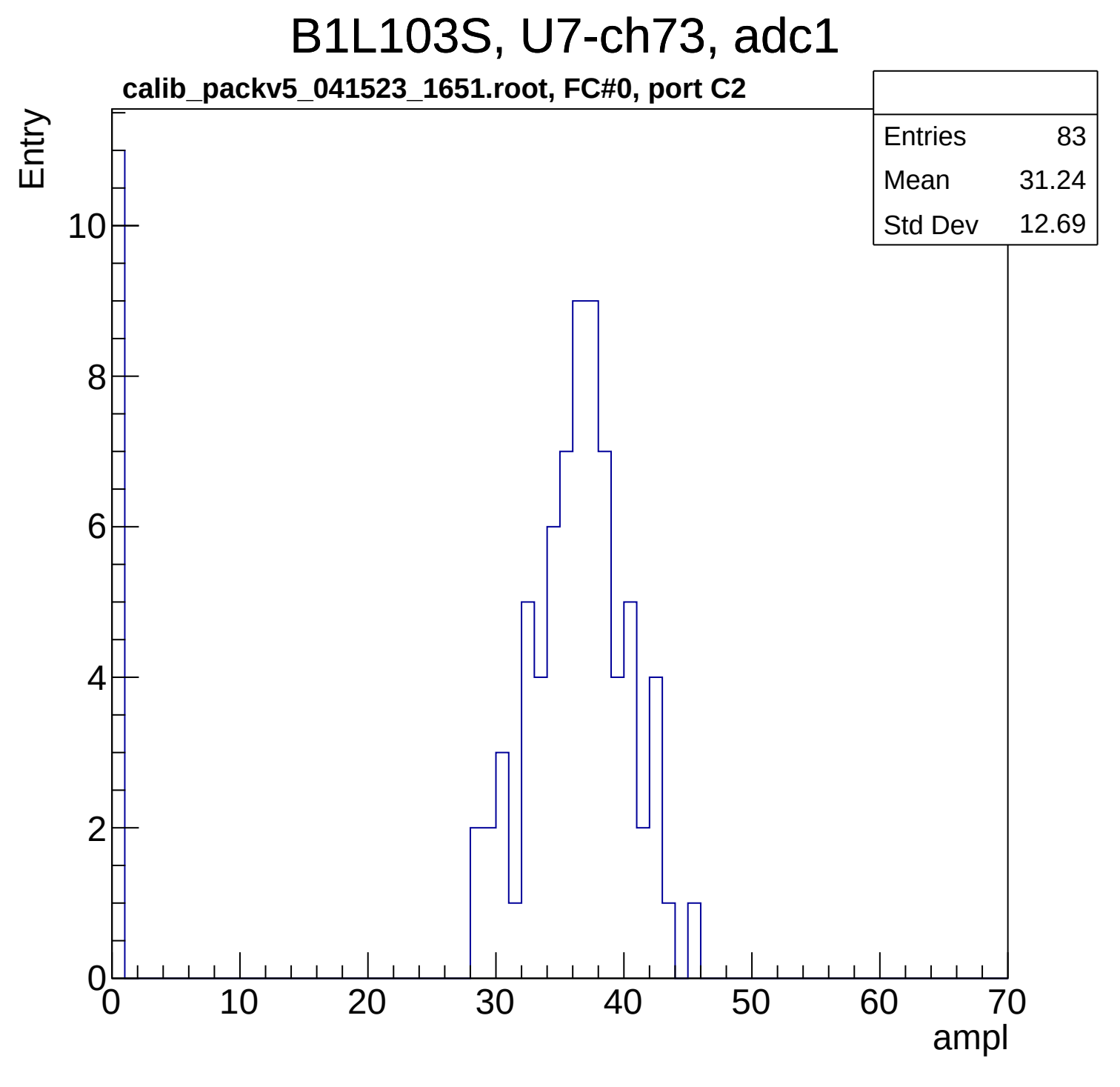
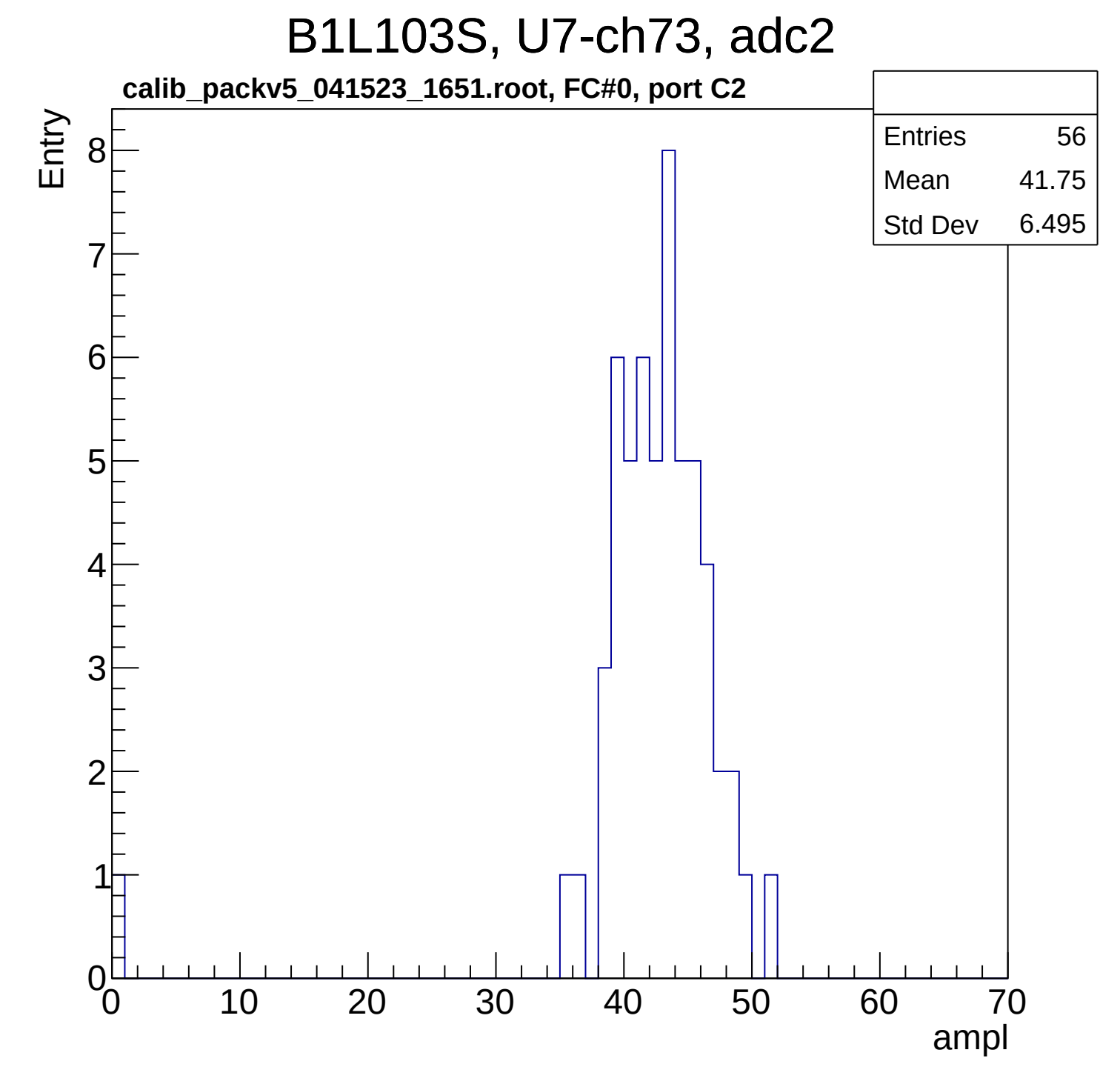
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch72, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 58.73
Std Dev 12.94
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U7-ch72, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch73, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 88
Mean 21.38
Std Dev 13.43
Entry
ampl
0
5
10
15
20
25
0
10
20
30
40
50
60
70


B1L103S, U7-ch73, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 31.24
Std Dev 12.69
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch73, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 41.75
Std Dev 6.495
Entry
ampl
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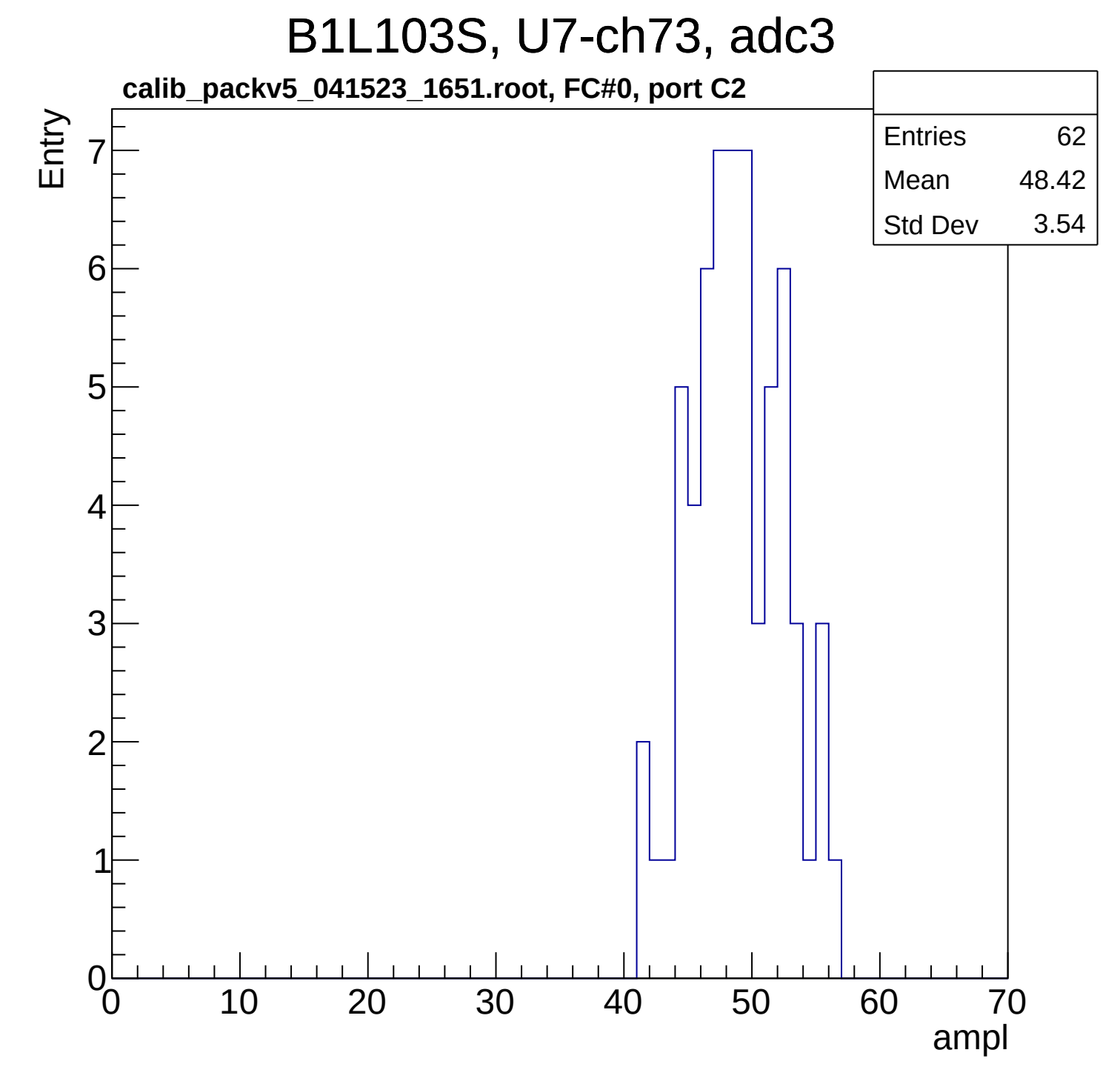
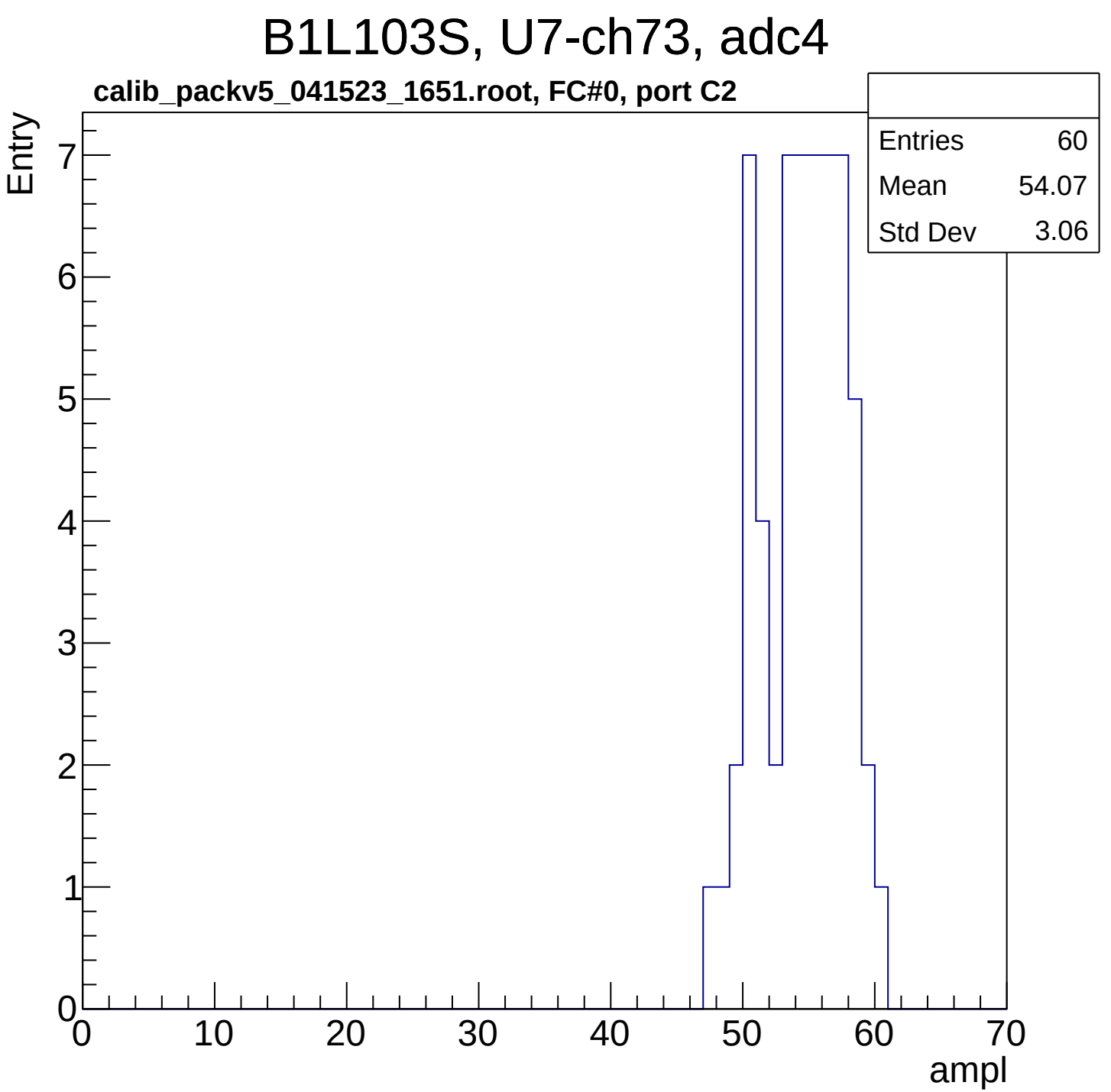
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch73, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 48.42
Std Dev 3.54
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U7-ch73, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 54.07
Std Dev 3.06
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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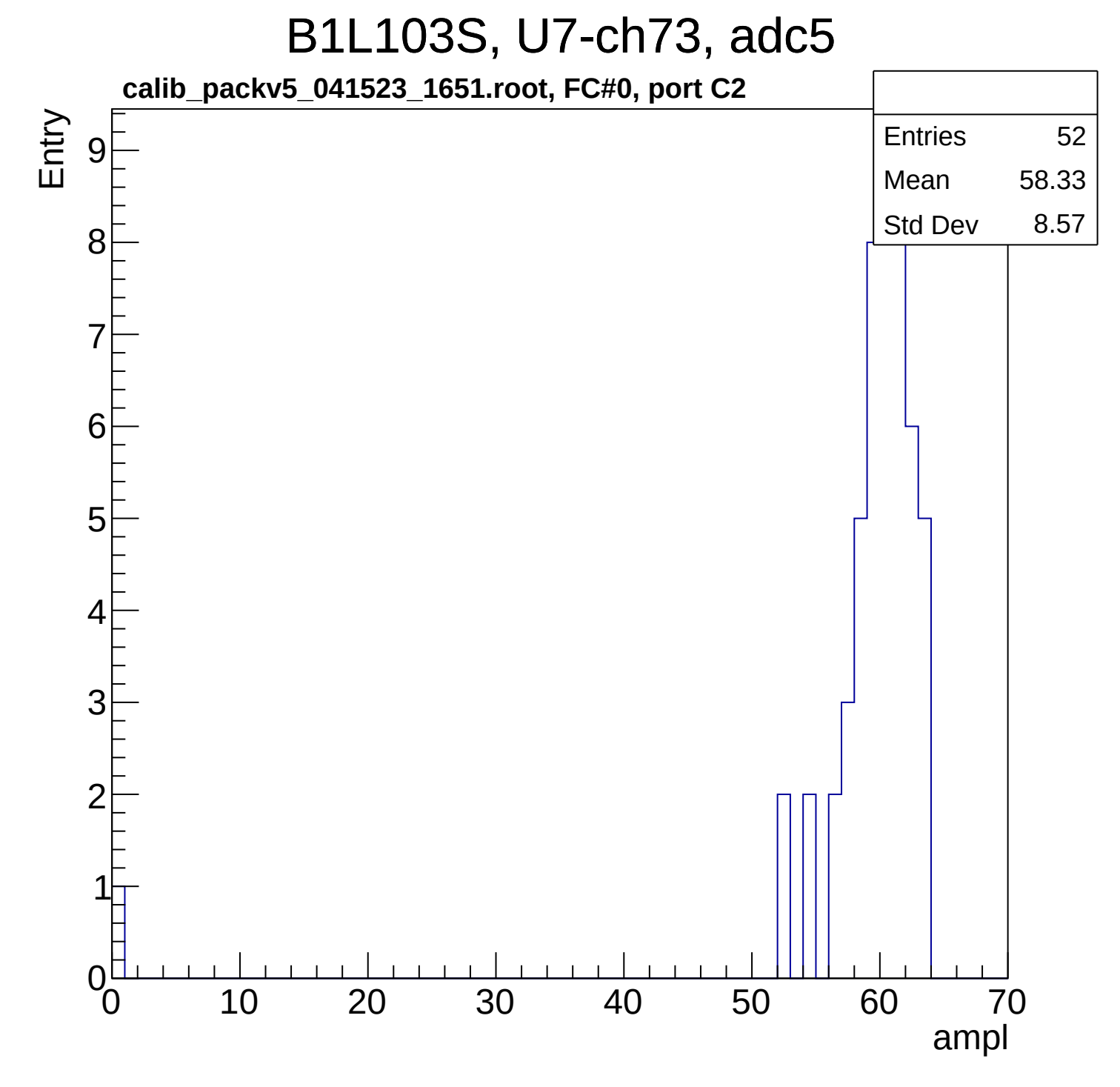
B1L103S, U7-ch73, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 58.33
Std Dev 8.57
Entry
ampl
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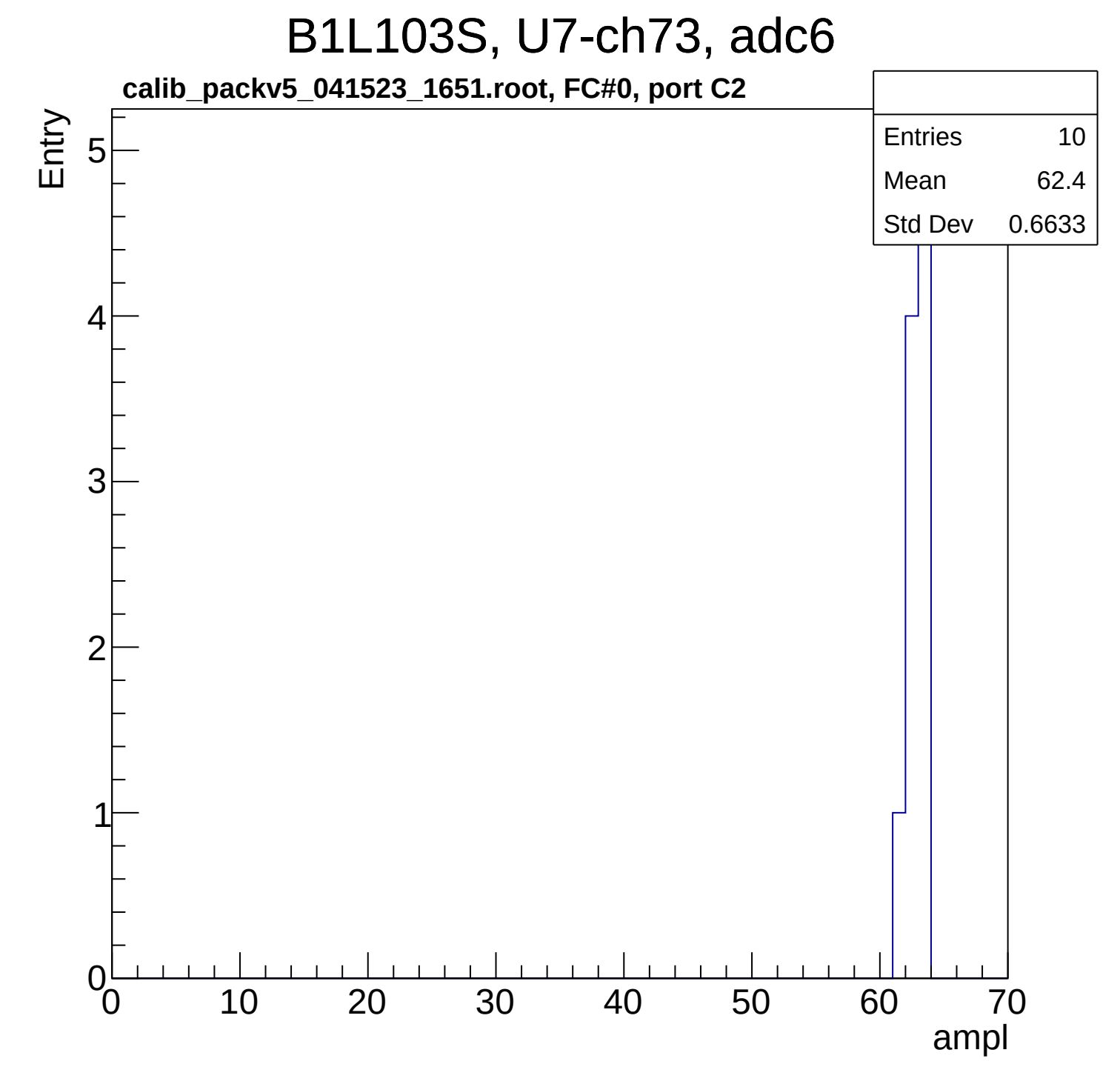
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U7-ch73, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 62.4
Std Dev 0.6633
Entry
0
1
2
3
4
5
0
10
20
30
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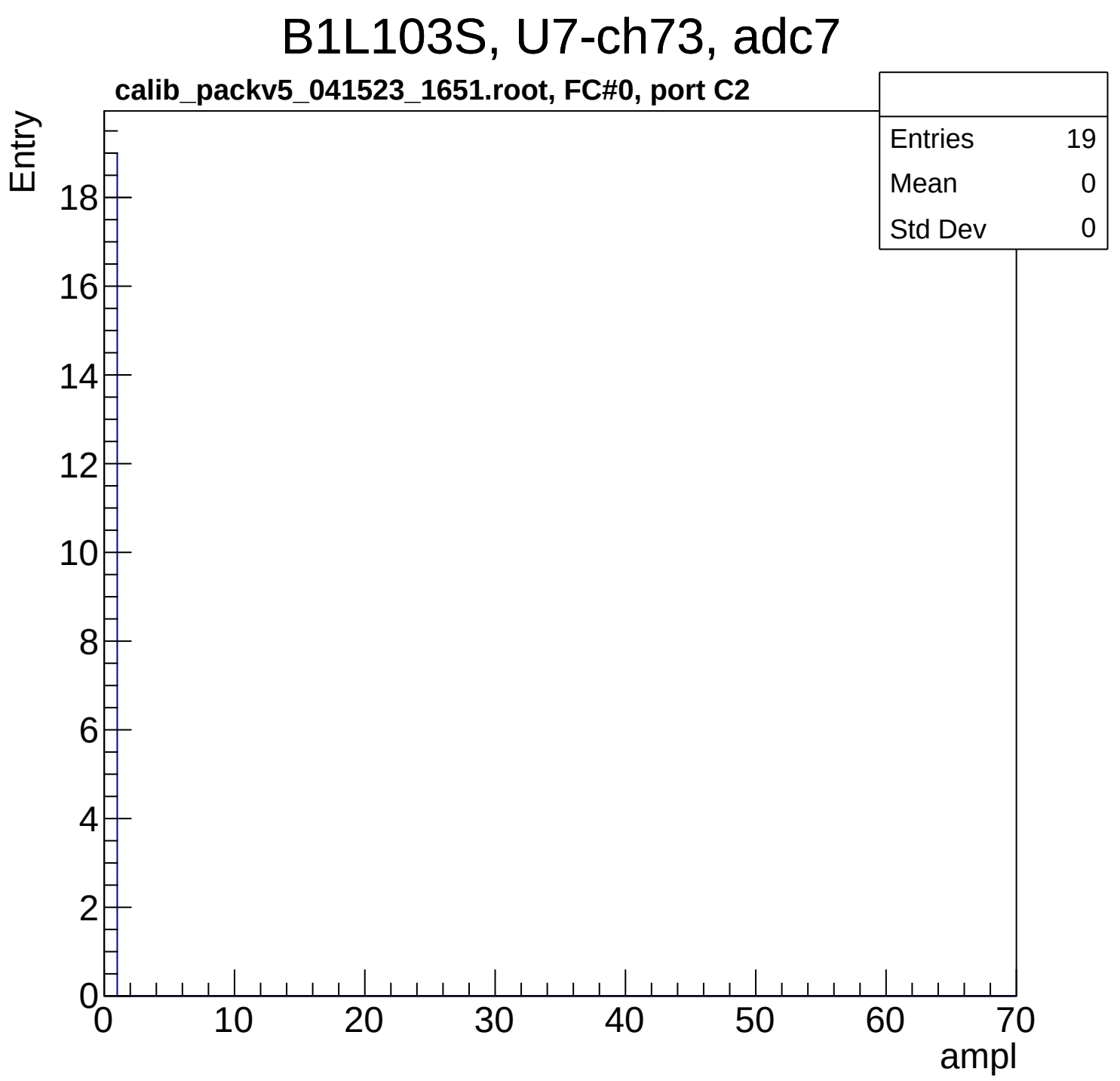
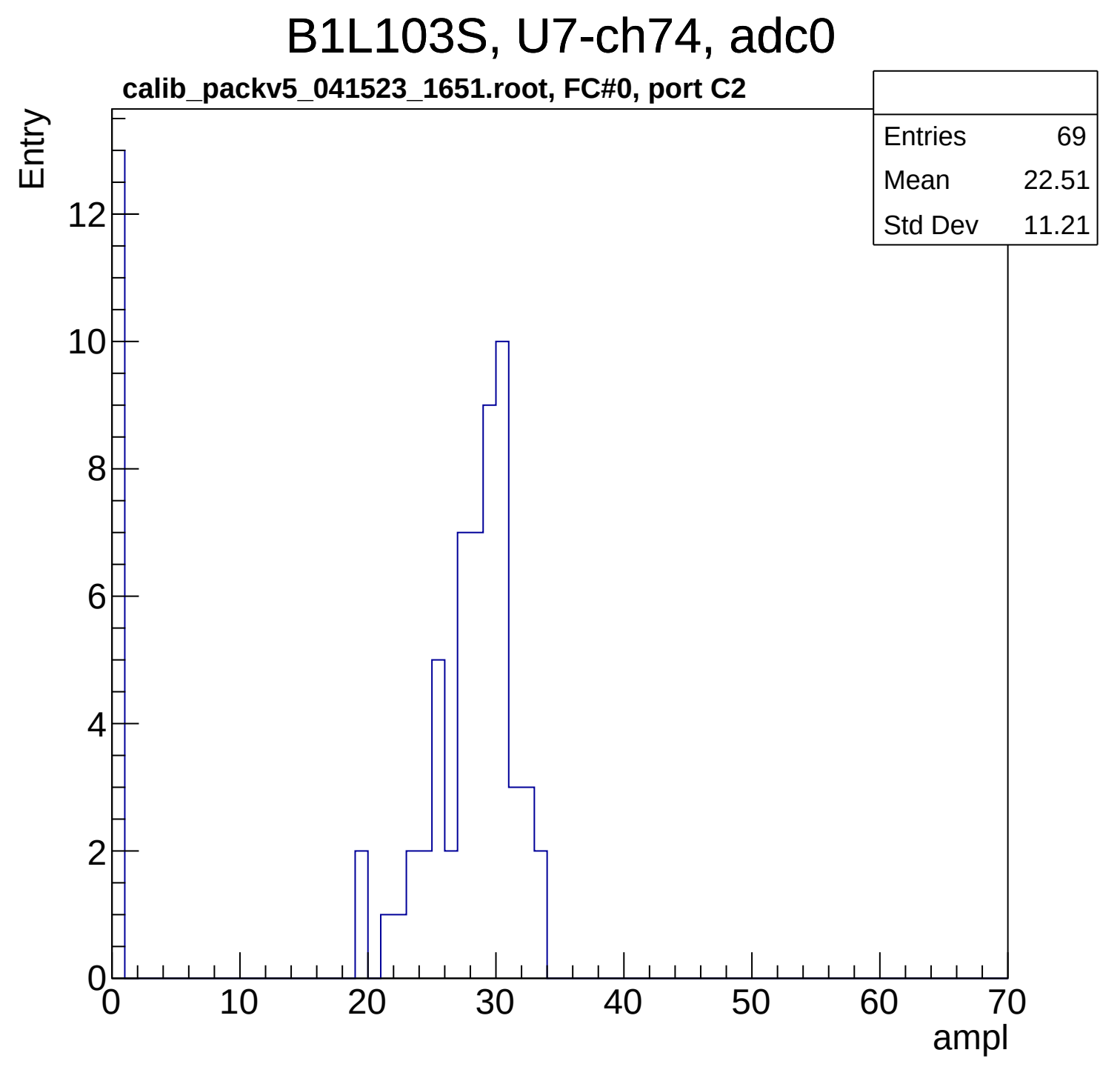
50
60
70
ampl


B1L103S, U7-ch73, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch74, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 22.51
Std Dev 11.21
Entry
0
2
4
6
8
10
12
0
10
20
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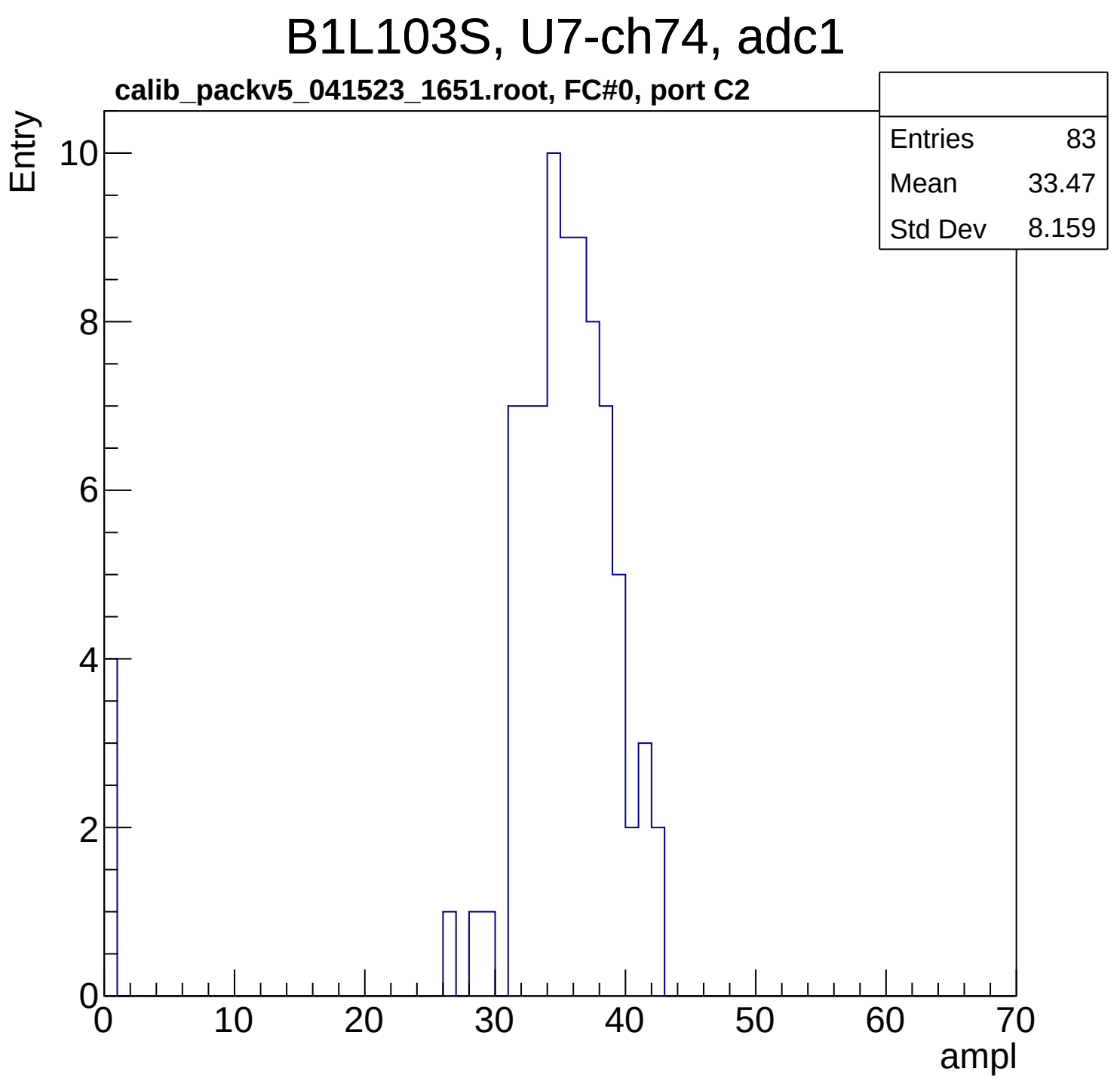
50
60
70
ampl


B1L103S, U7-ch74, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 33.47
Std Dev 8.159
Entry
0
2
4
6
8
10
0
10
20
30
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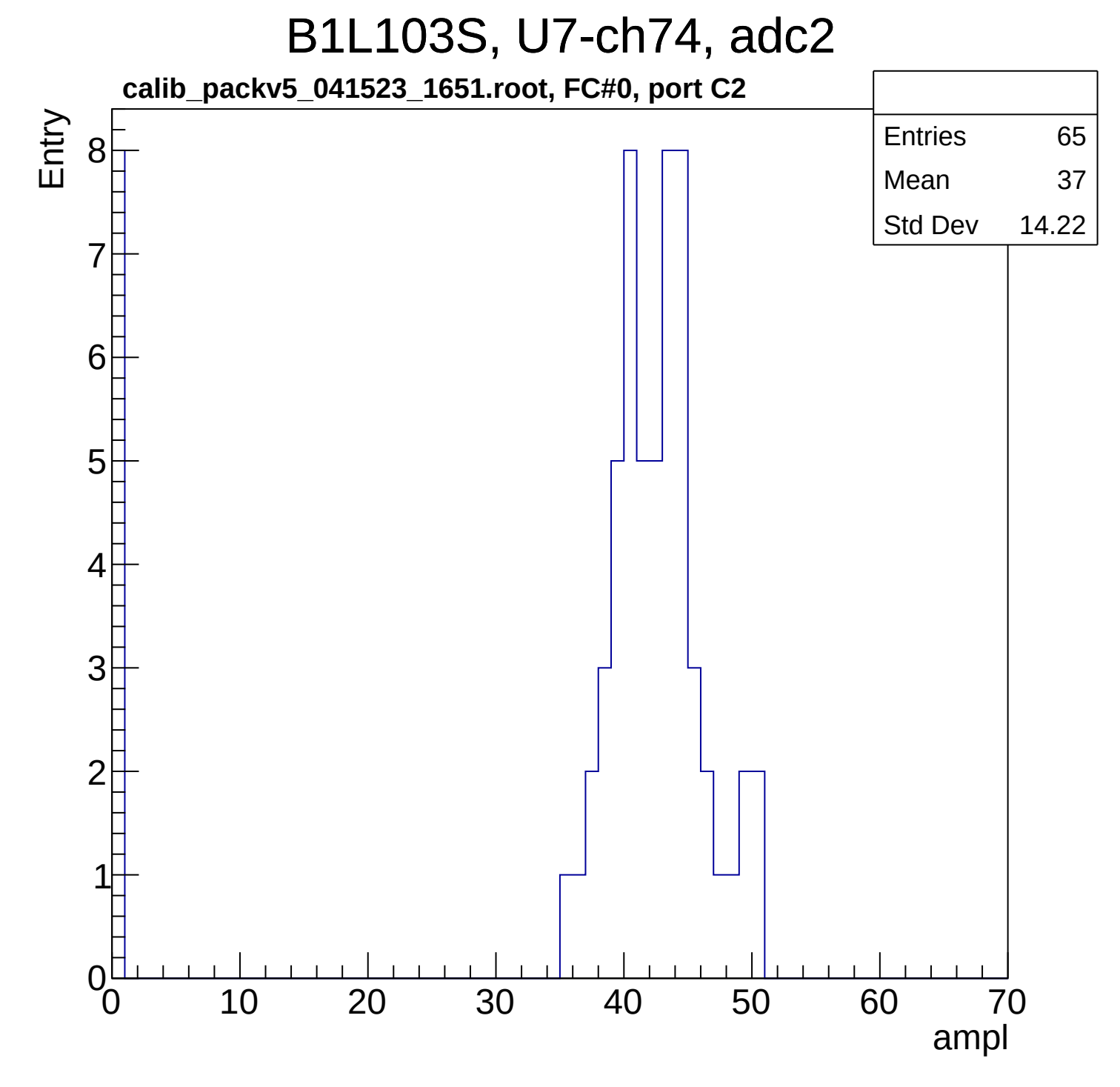
50
60
70
ampl


B1L103S, U7-ch74, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 37
Std Dev 14.22
Entry
ampl
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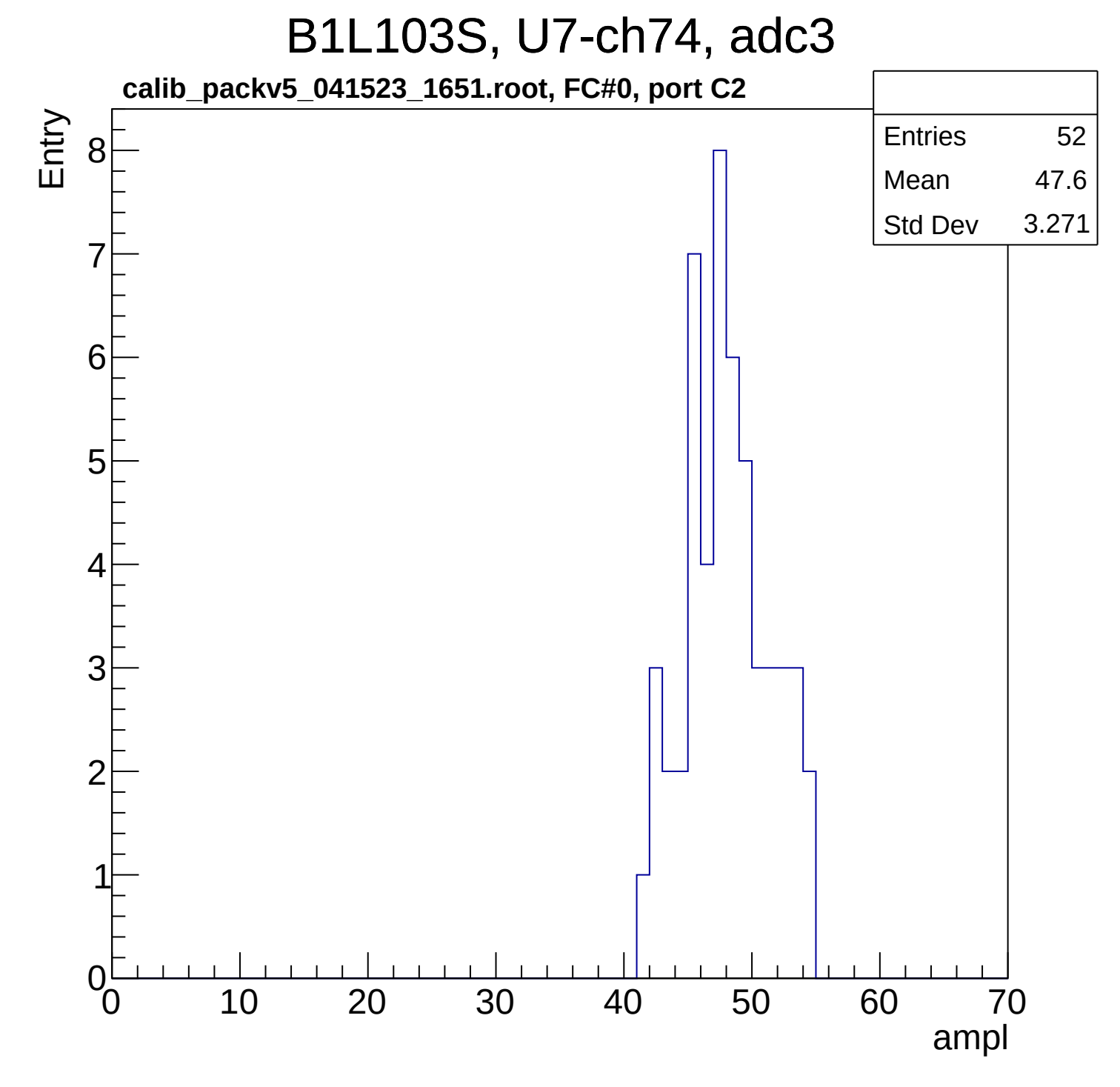
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch74, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 47.6
Std Dev 3.271
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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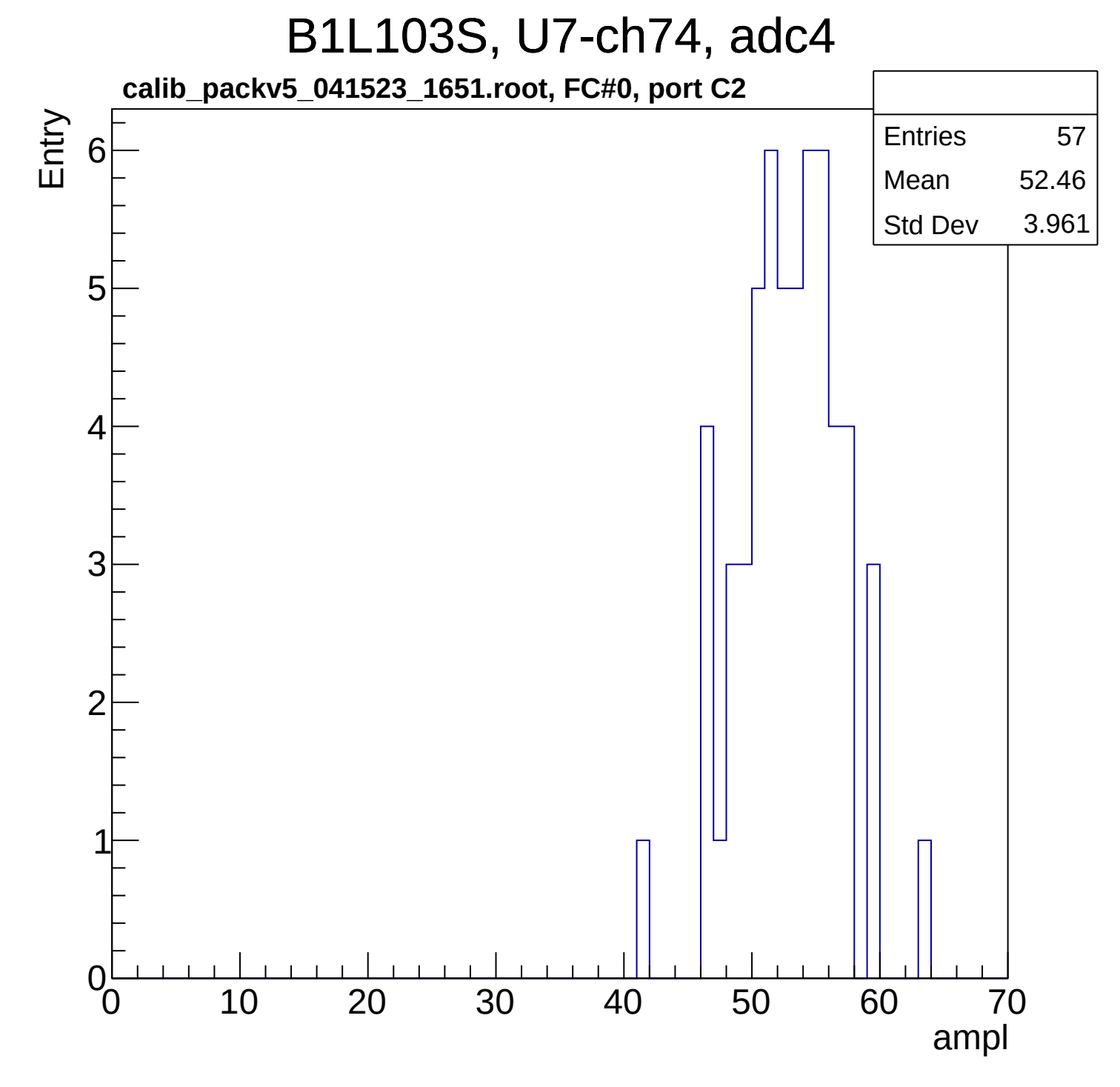
B1L103S, U7-ch74, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 52.46
Std Dev 3.961
Entry
ampl
0
1
2
3
4
5
6
0
10
20
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40
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60
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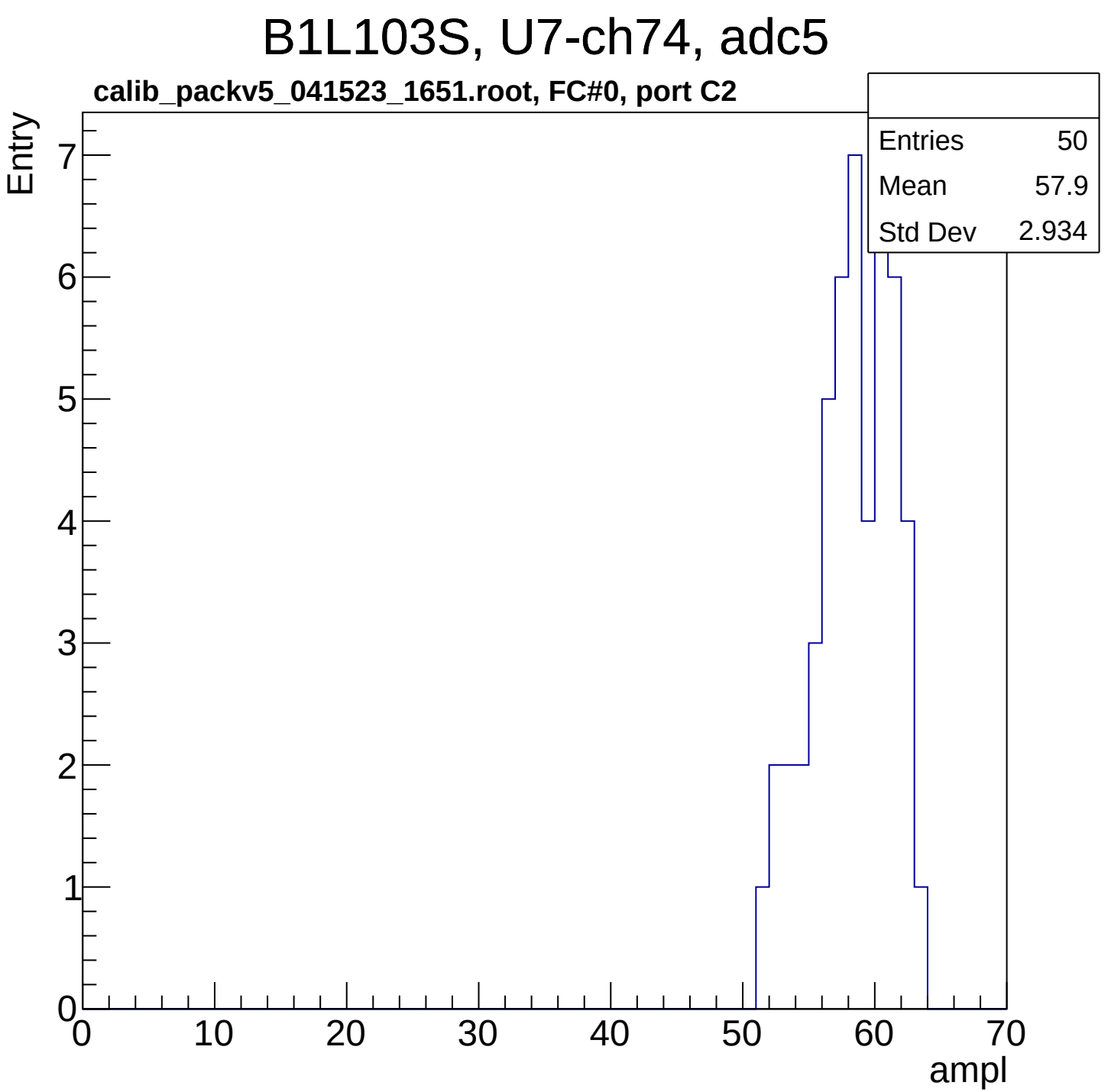
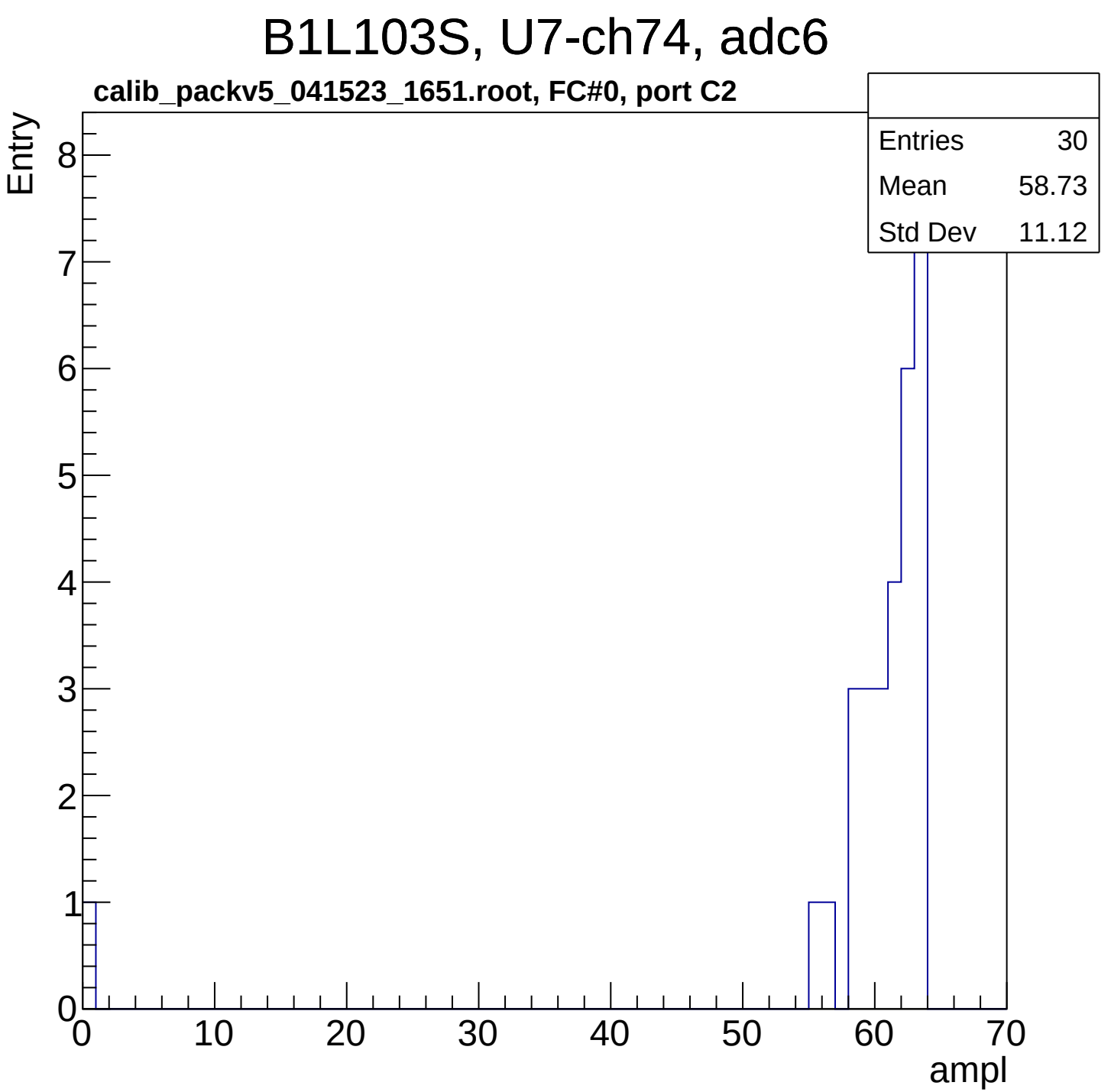

B1L103S, U7-ch74, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 57.9
Std Dev 2.934
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U7-ch74, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 30
Mean 58.73
Std Dev 11.12
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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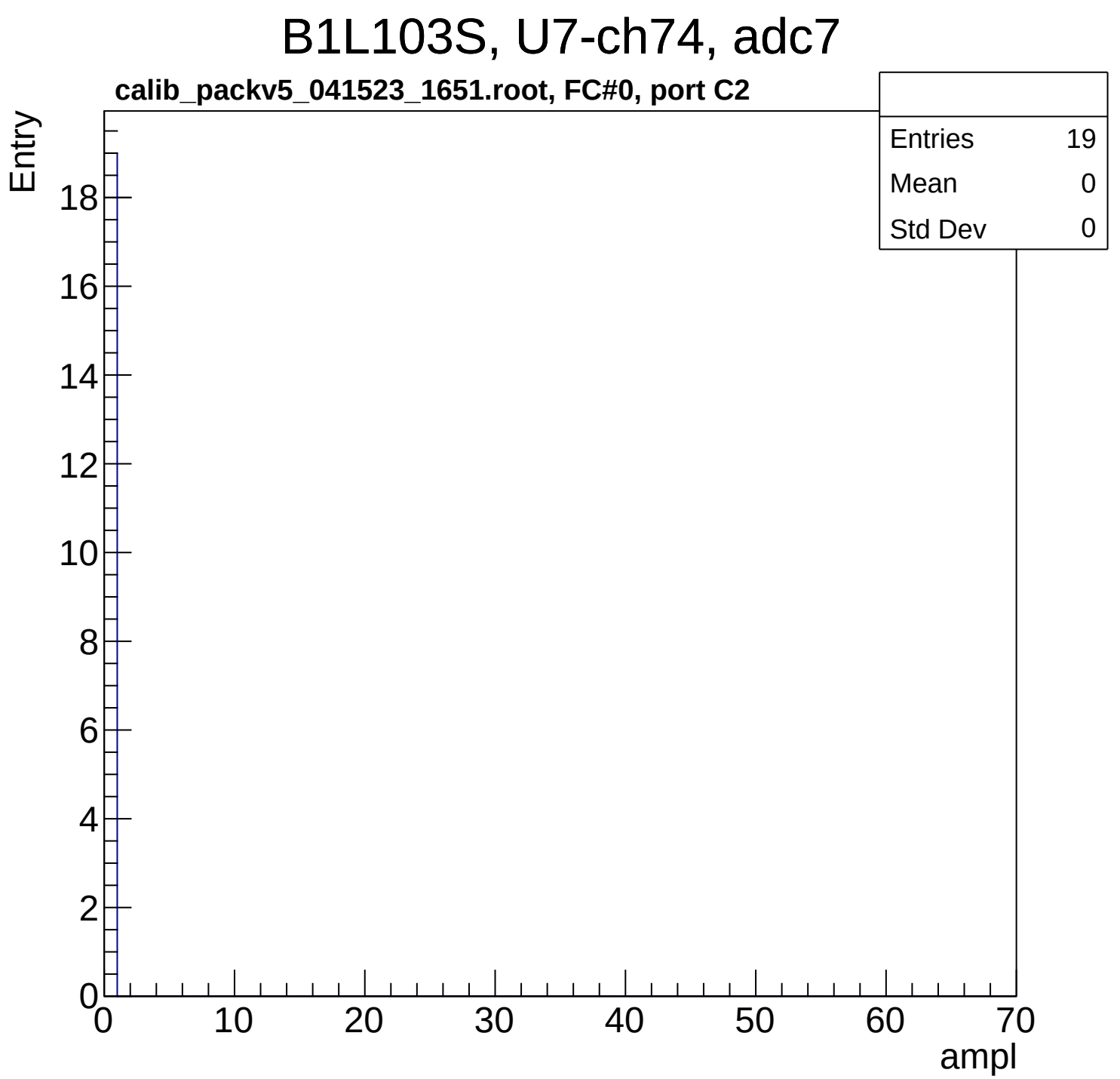
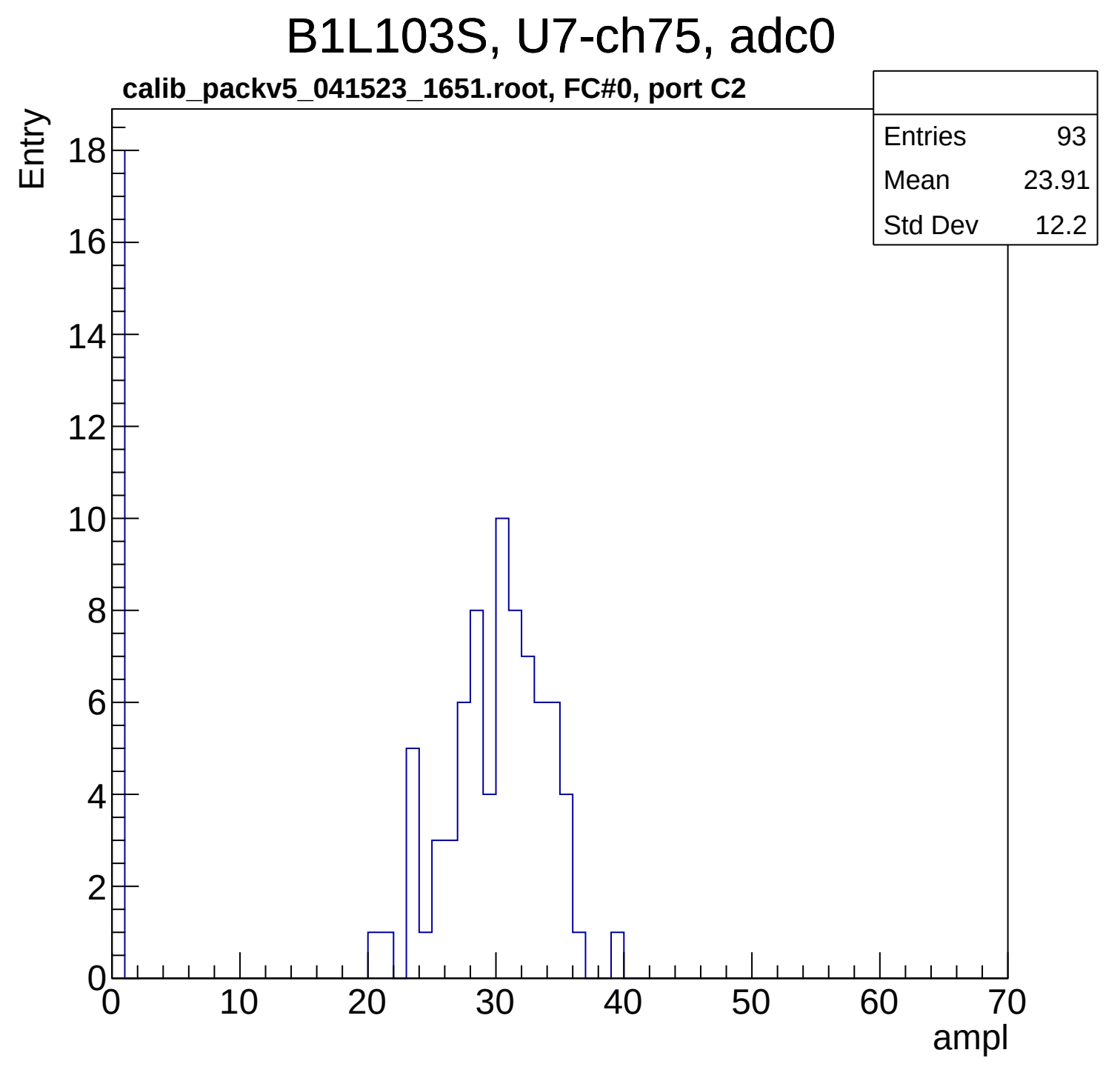
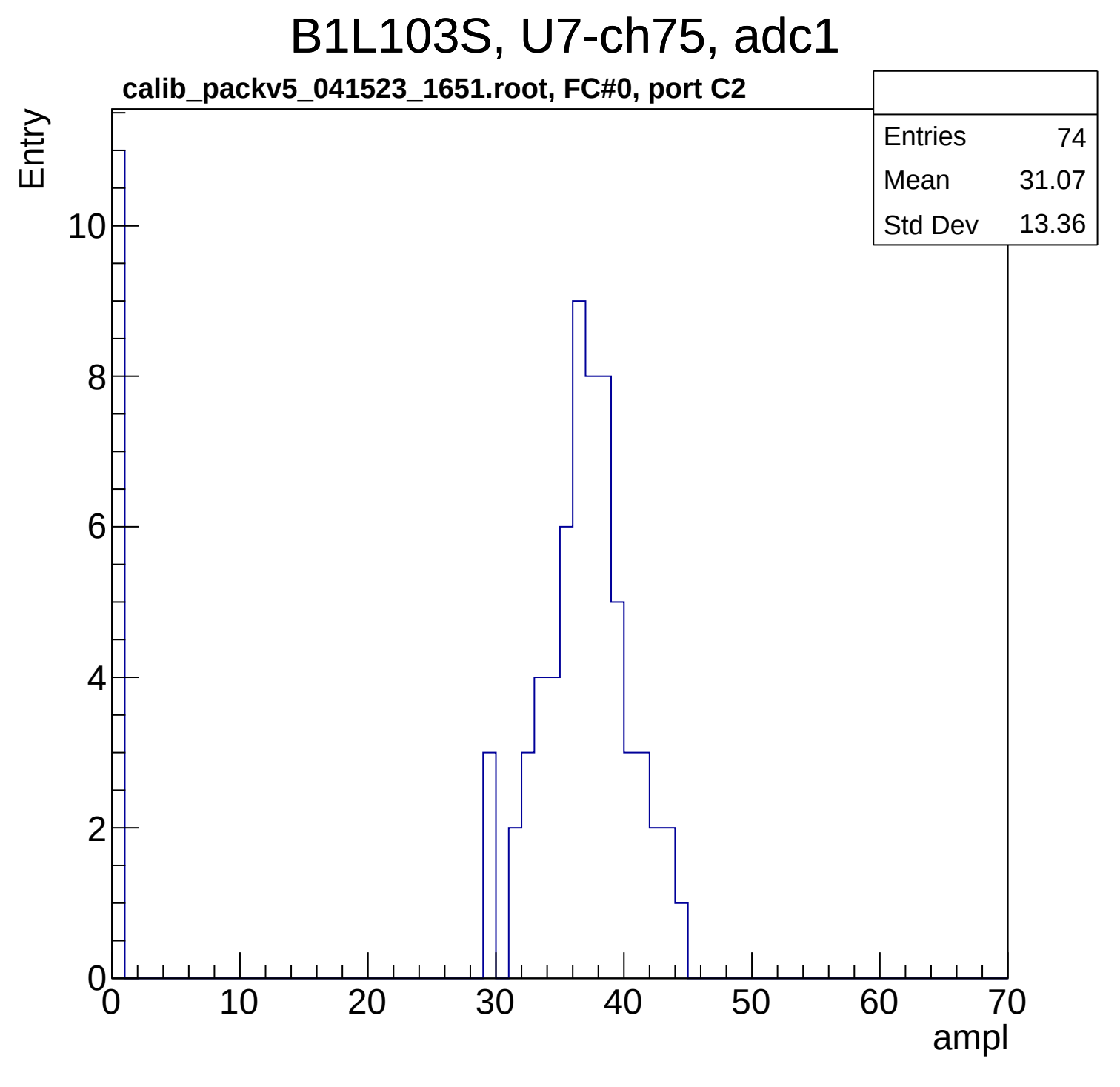
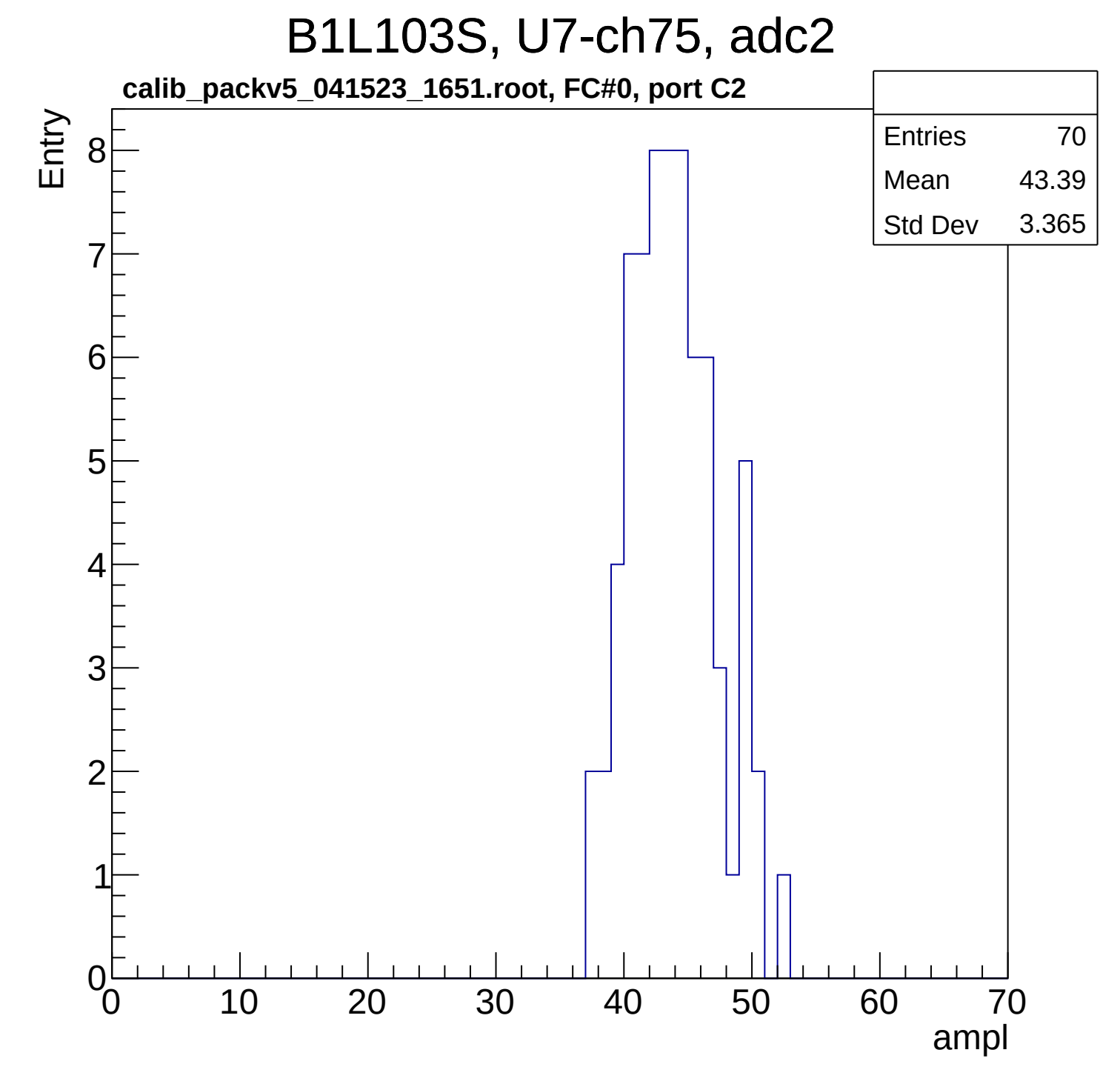

B1L103S, U7-ch74, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch75, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 93
Mean 23.91
Std Dev 12.2
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70


B1L103S, U7-ch75, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 31.07
Std Dev 13.36
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch75, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 43.39
Std Dev 3.365
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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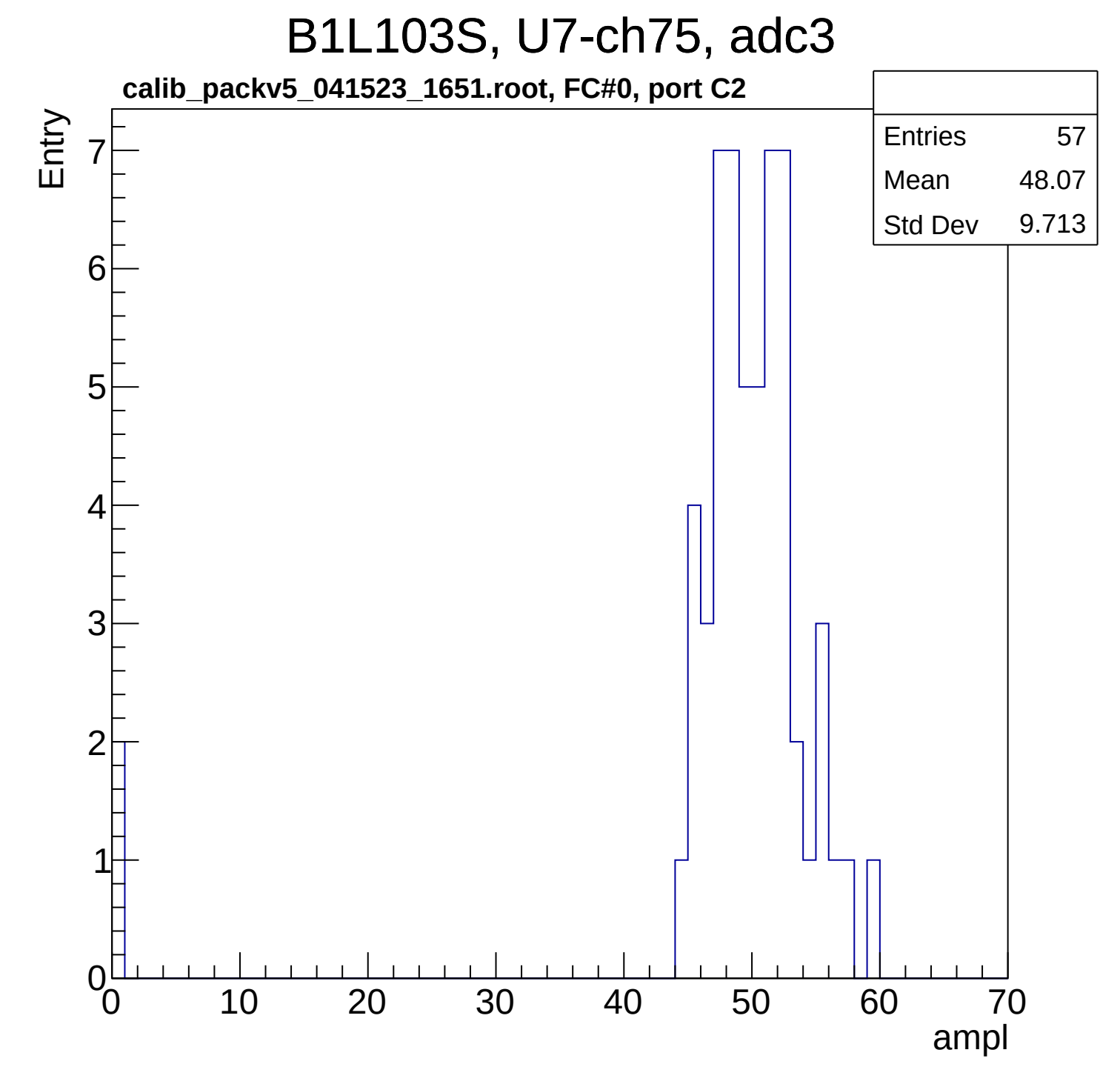
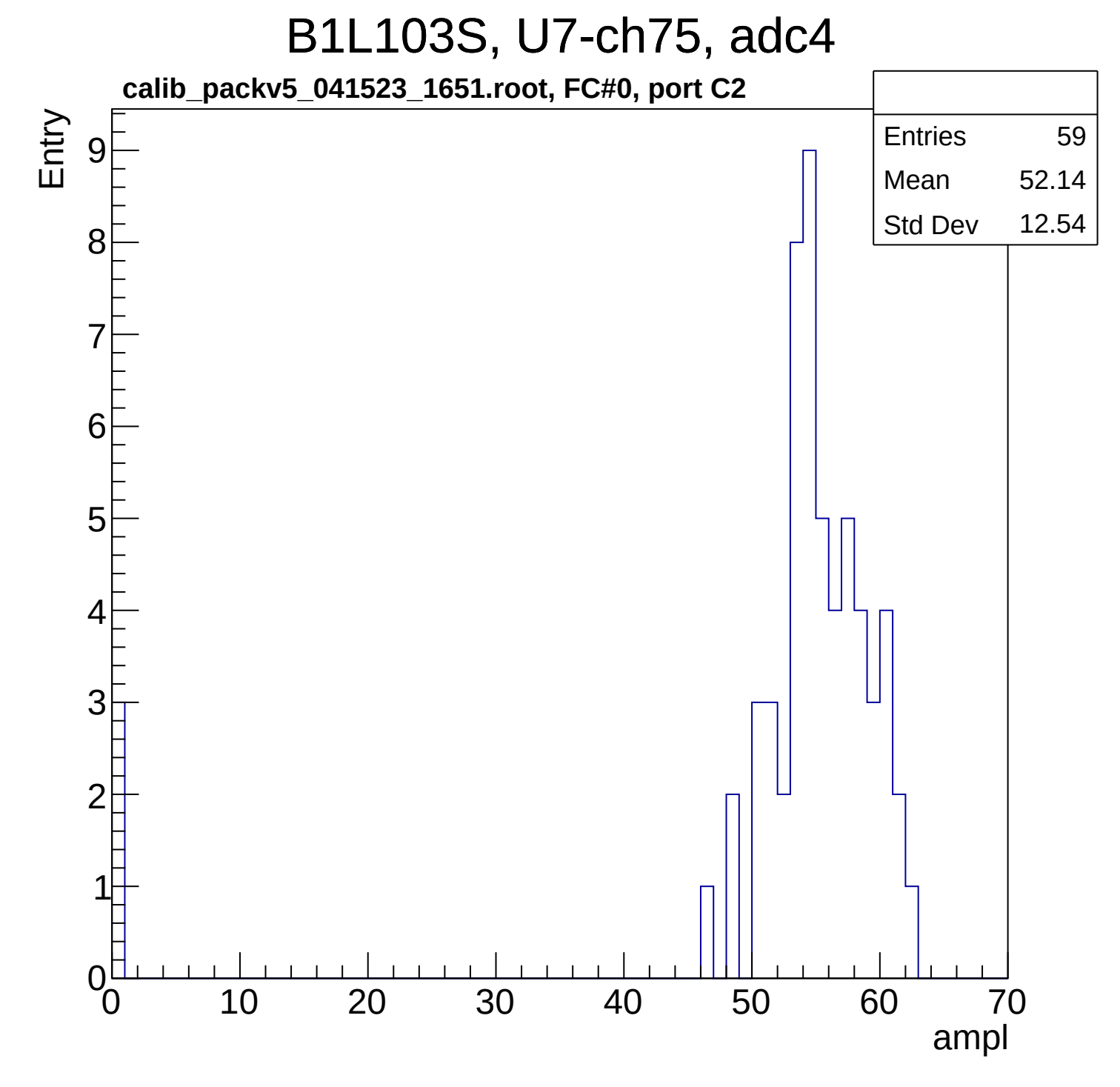
40
50
60
70


B1L103S, U7-ch75, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 48.07
Std Dev 9.713
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U7-ch75, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 52.14
Std Dev 12.54
Entry
ampl
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2
3
4
5
6
7
8
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0
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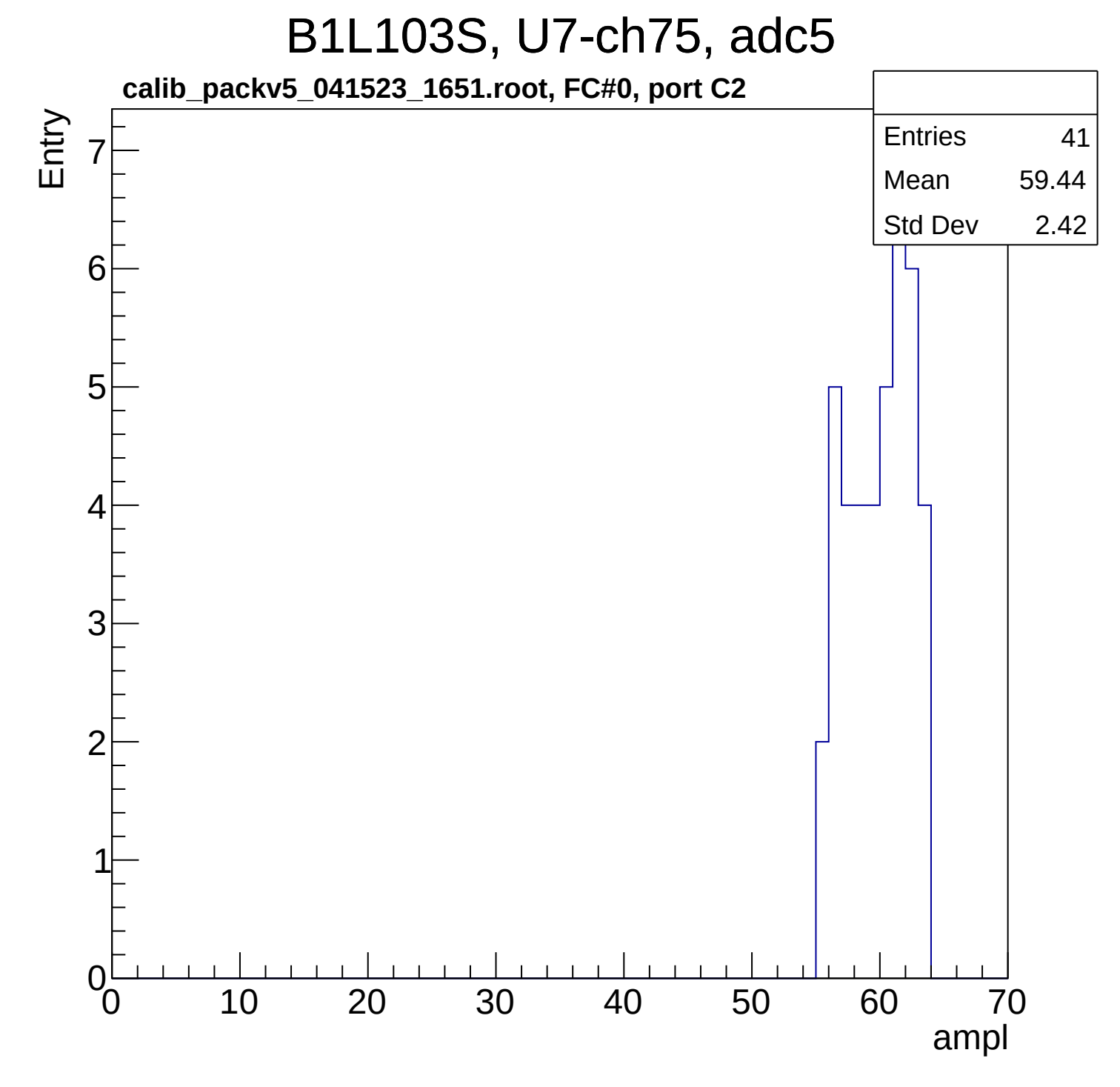
B1L103S, U7-ch75, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 41
Mean 59.44
Std Dev 2.42
Entry
ampl
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2
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4
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6
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0
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60
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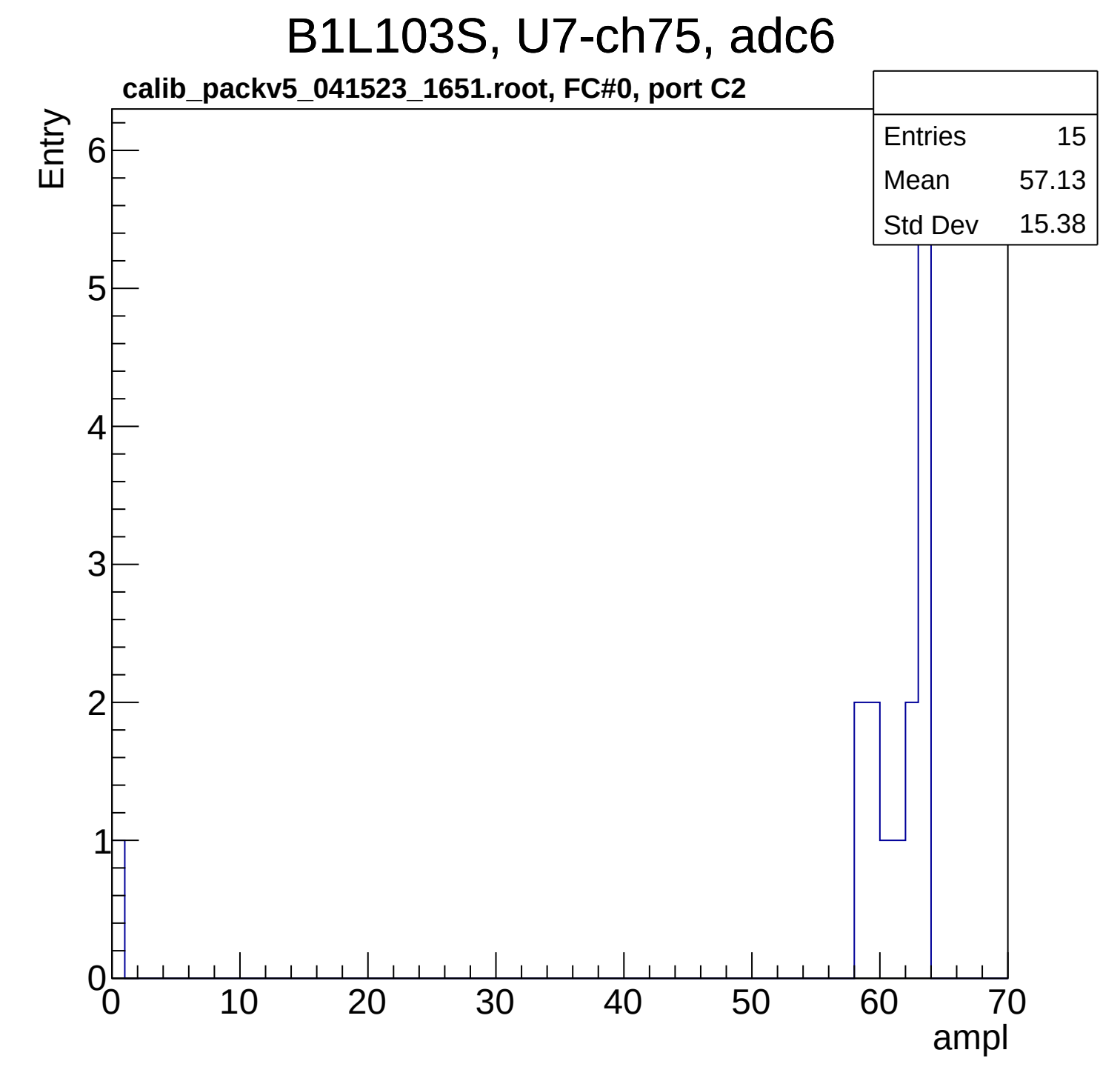
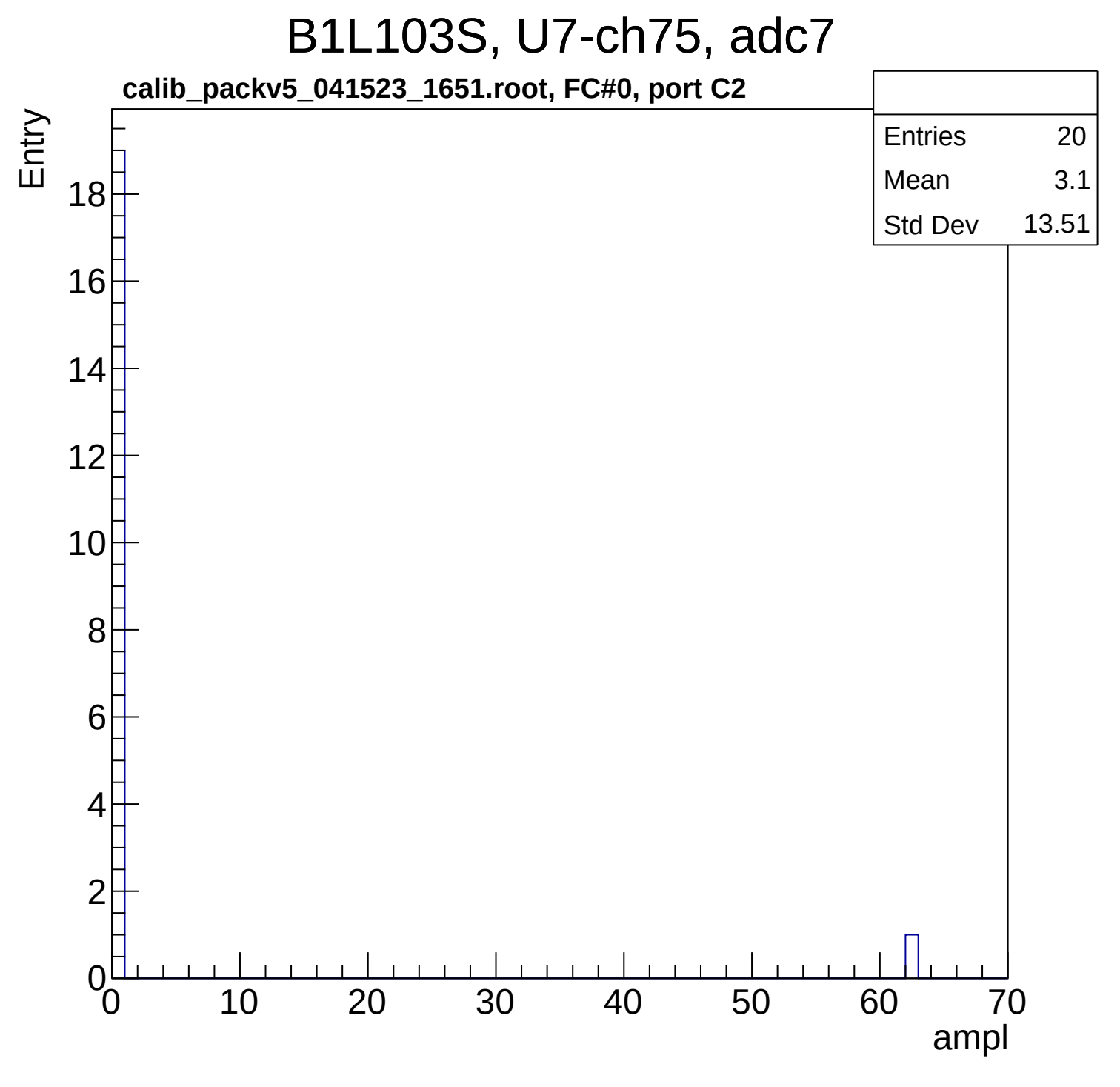
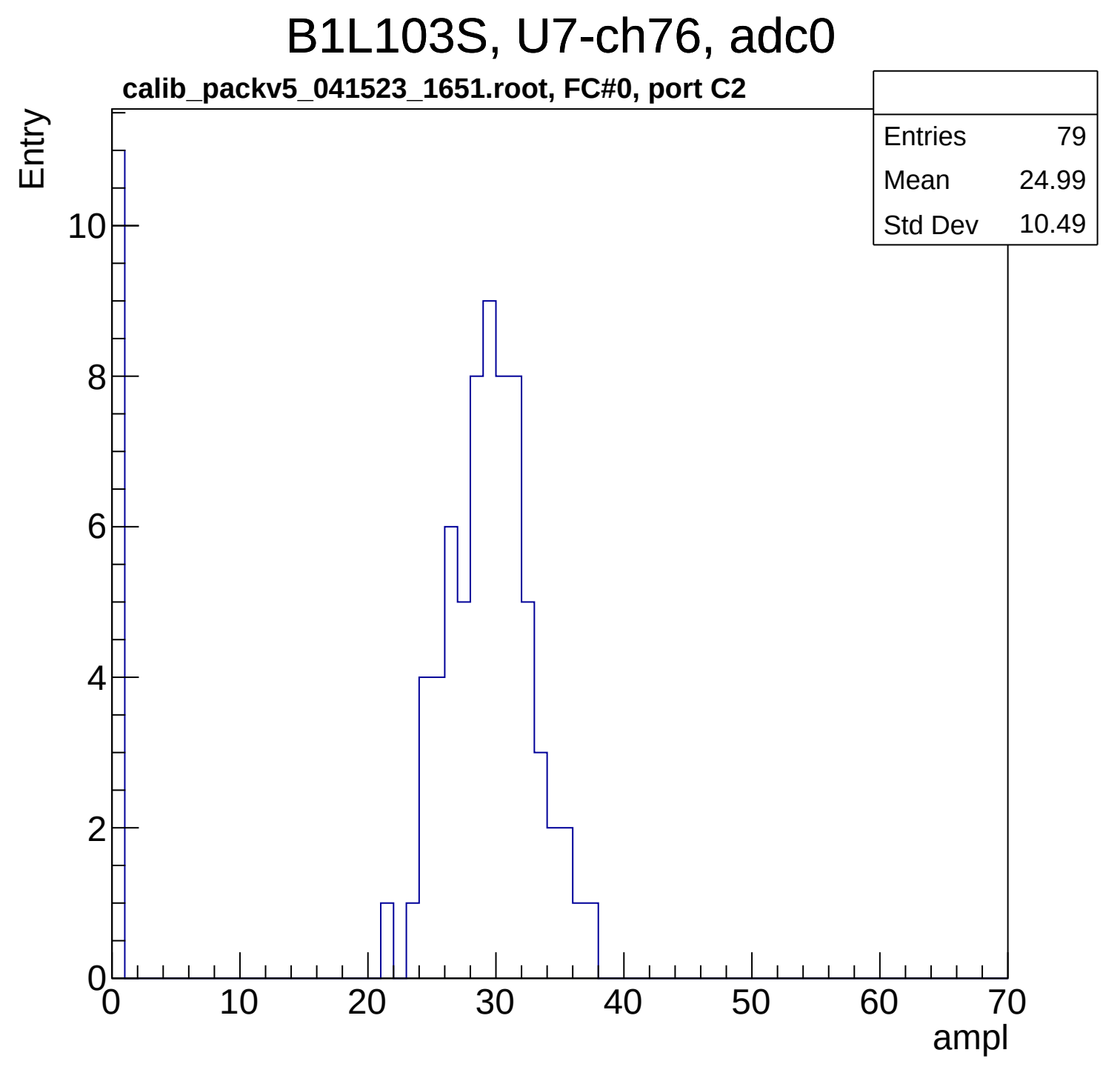
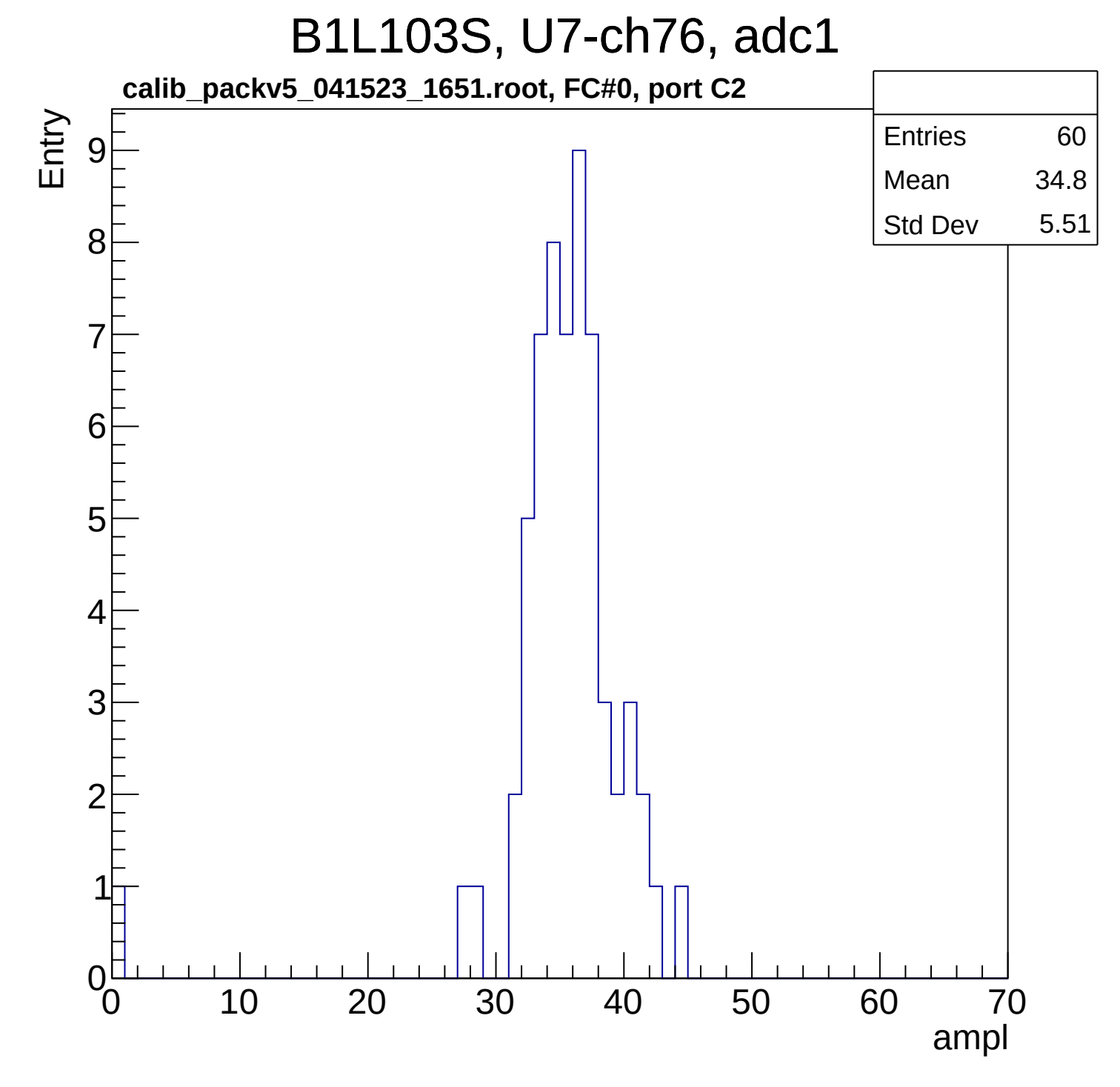

B1L103S, U7-ch75, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 15
Mean 57.13
Std Dev 15.38
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch75, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.1
Std Dev 13.51
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch76, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 24.99
Std Dev 10.49
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch76, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 34.8
Std Dev 5.51
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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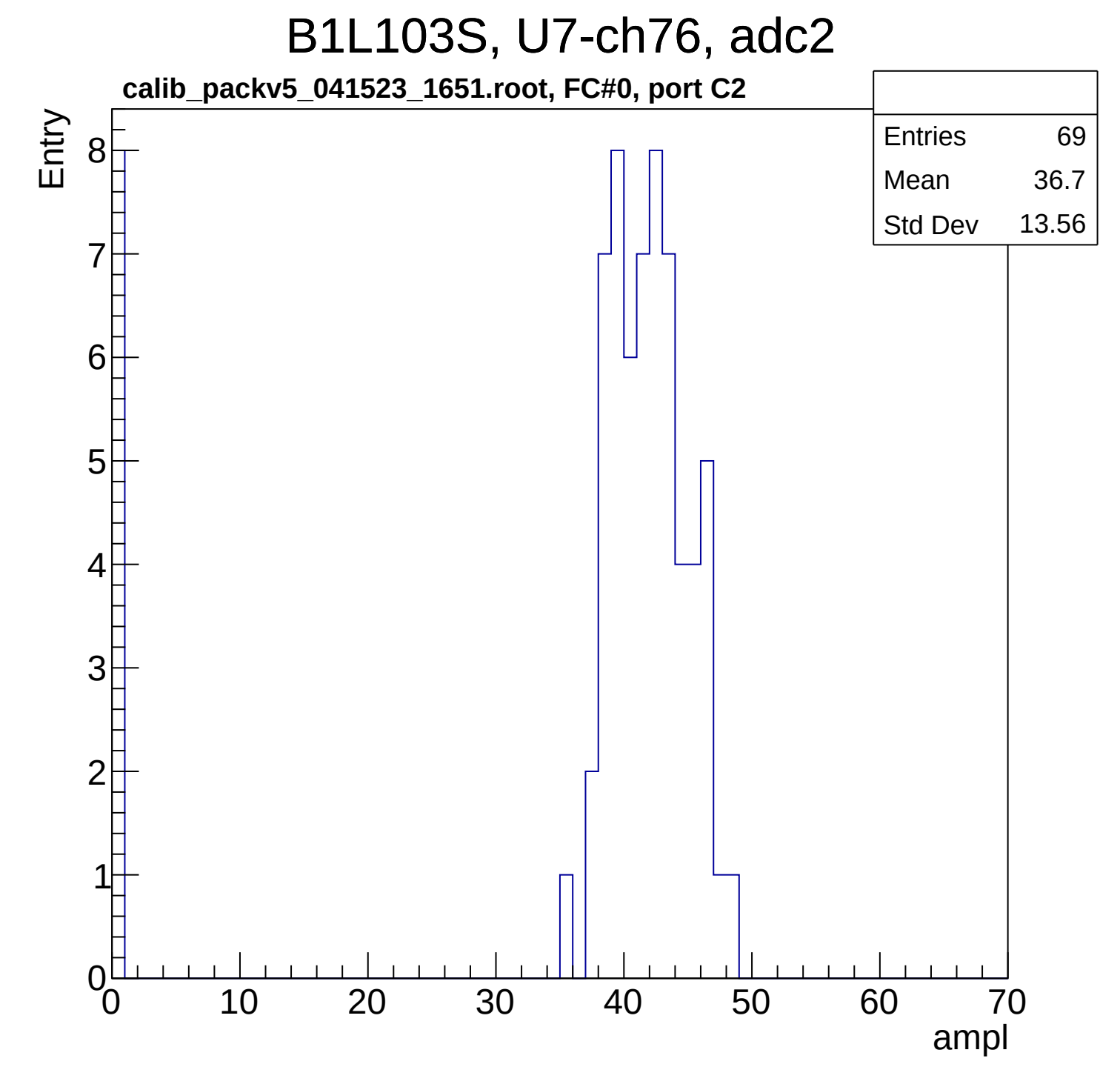
40
50
60
70


B1L103S, U7-ch76, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 36.7
Std Dev 13.56
Entry
ampl
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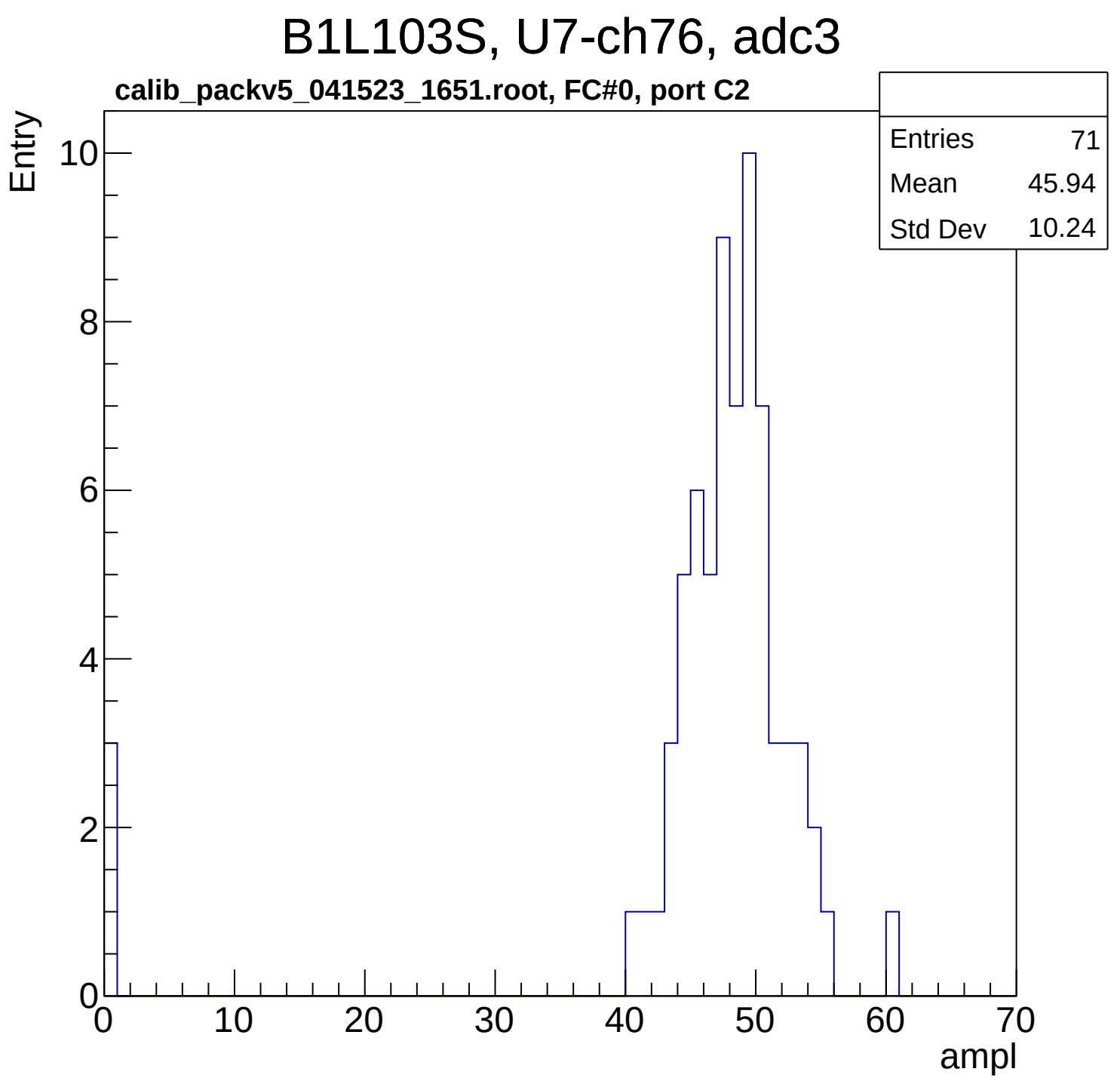
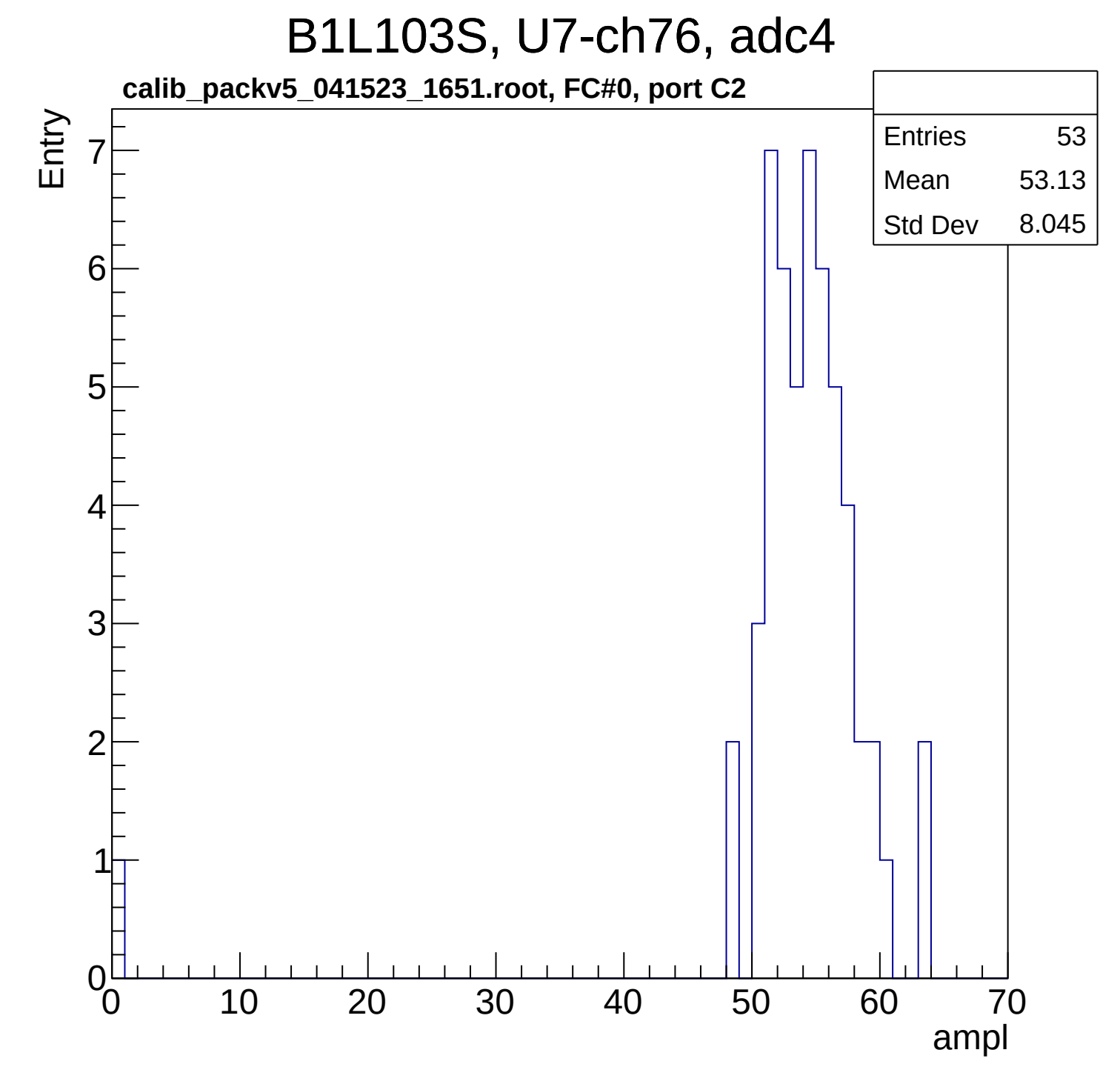
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch76, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 45.94
Std Dev 10.24
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch76, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 53.13
Std Dev 8.045
Entry
ampl
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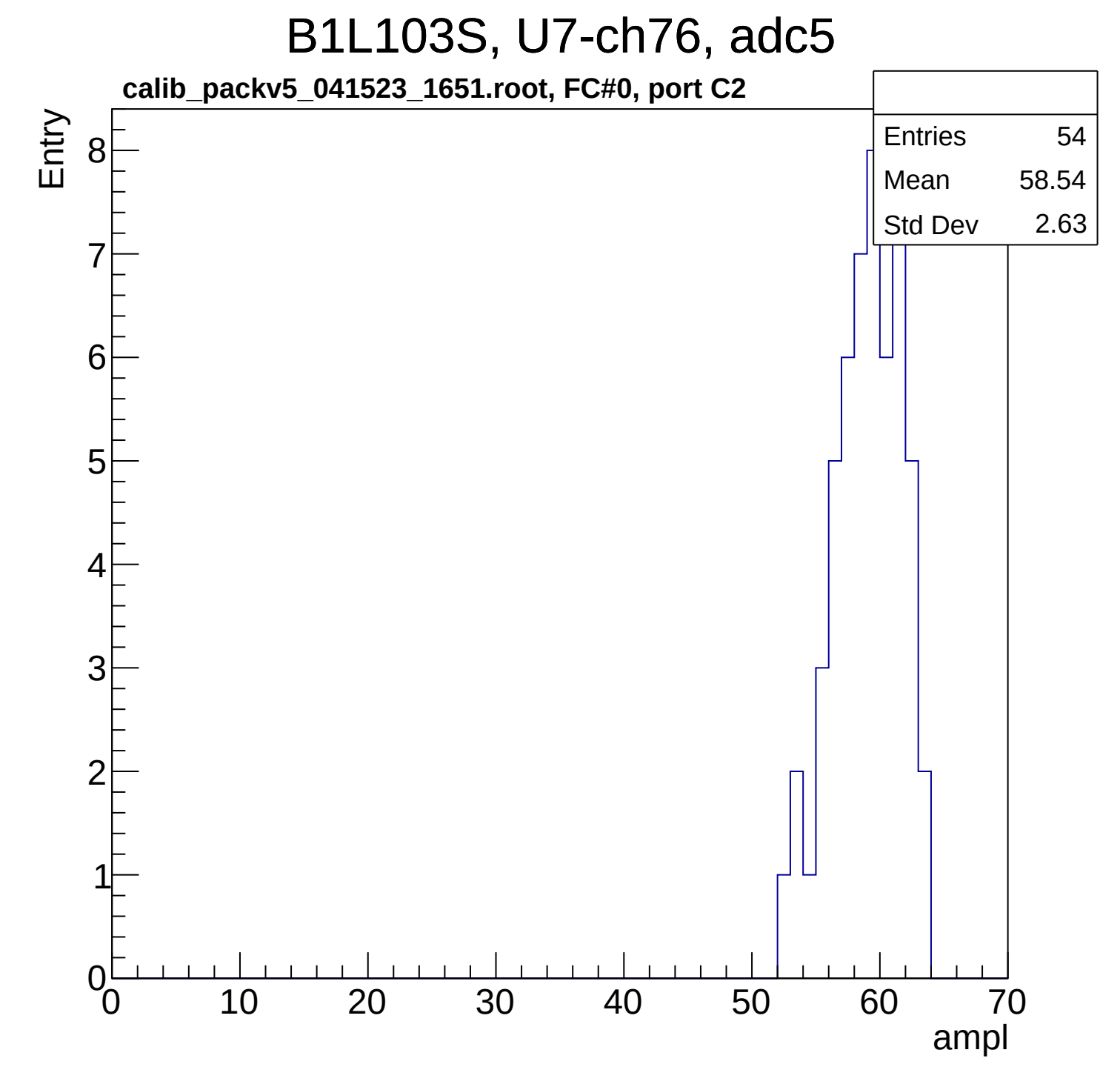
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U7-ch76, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 58.54
Std Dev 2.63
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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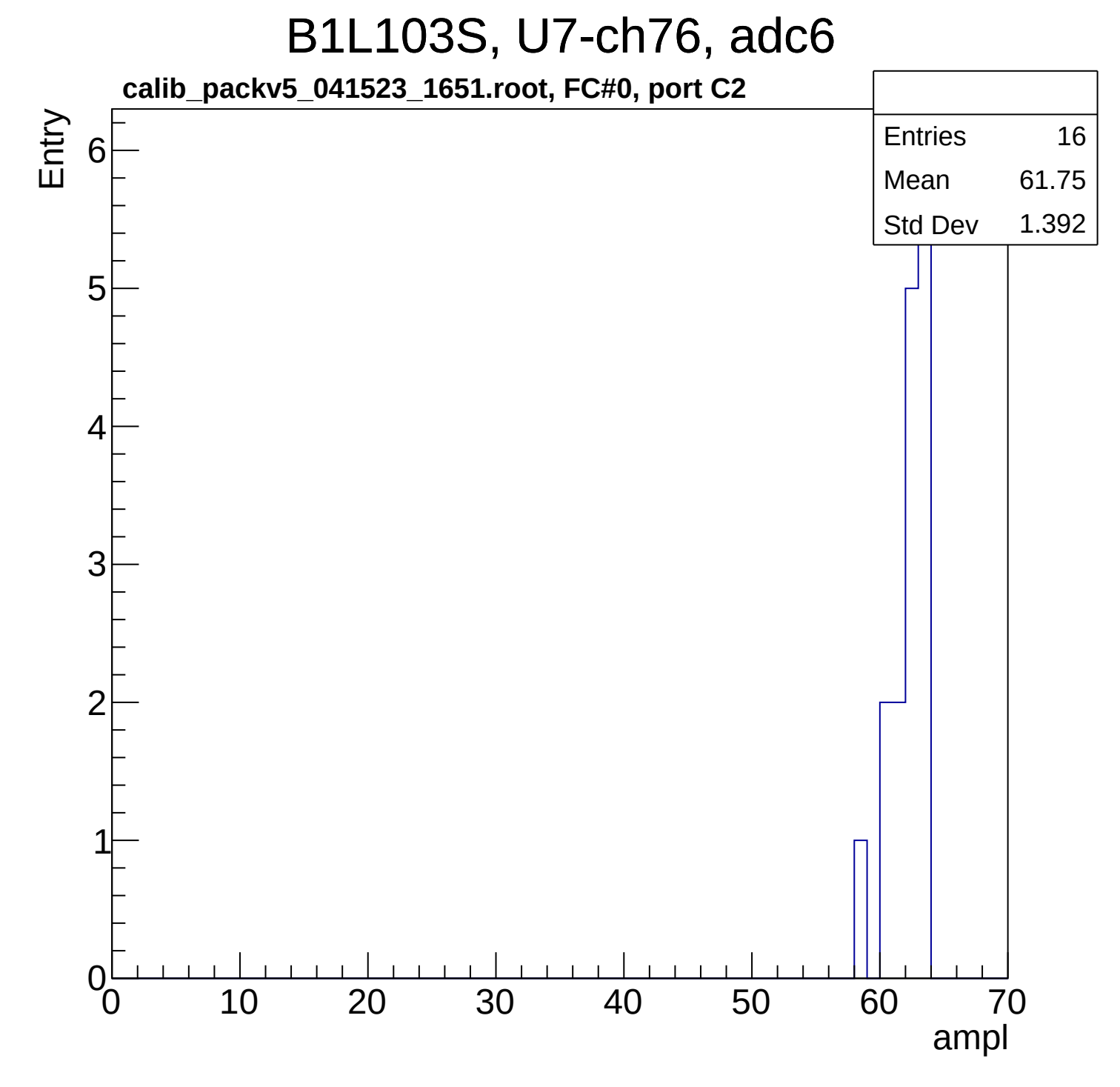
B1L103S, U7-ch76, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 16
Mean 61.75
Std Dev 1.392
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
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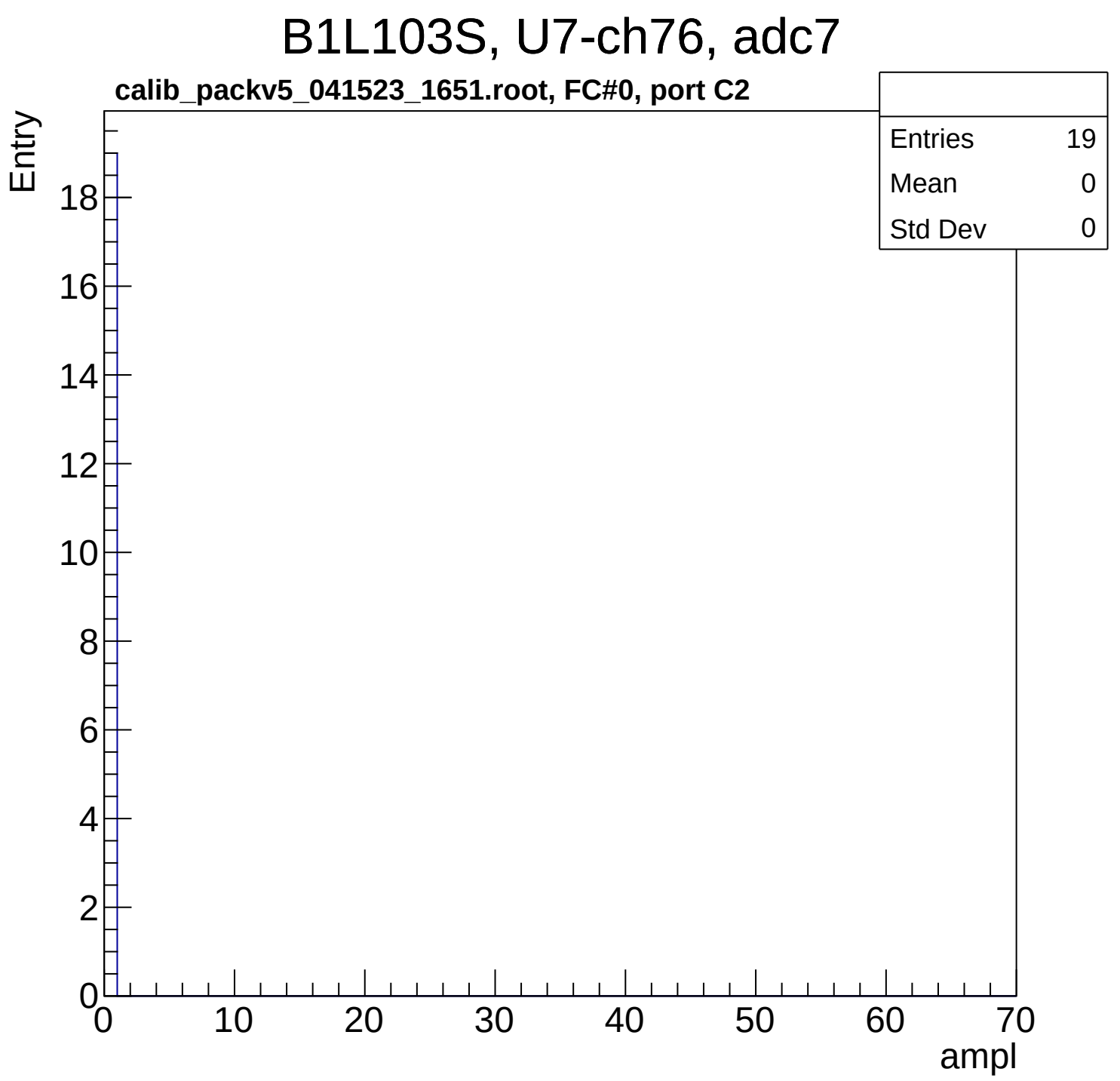
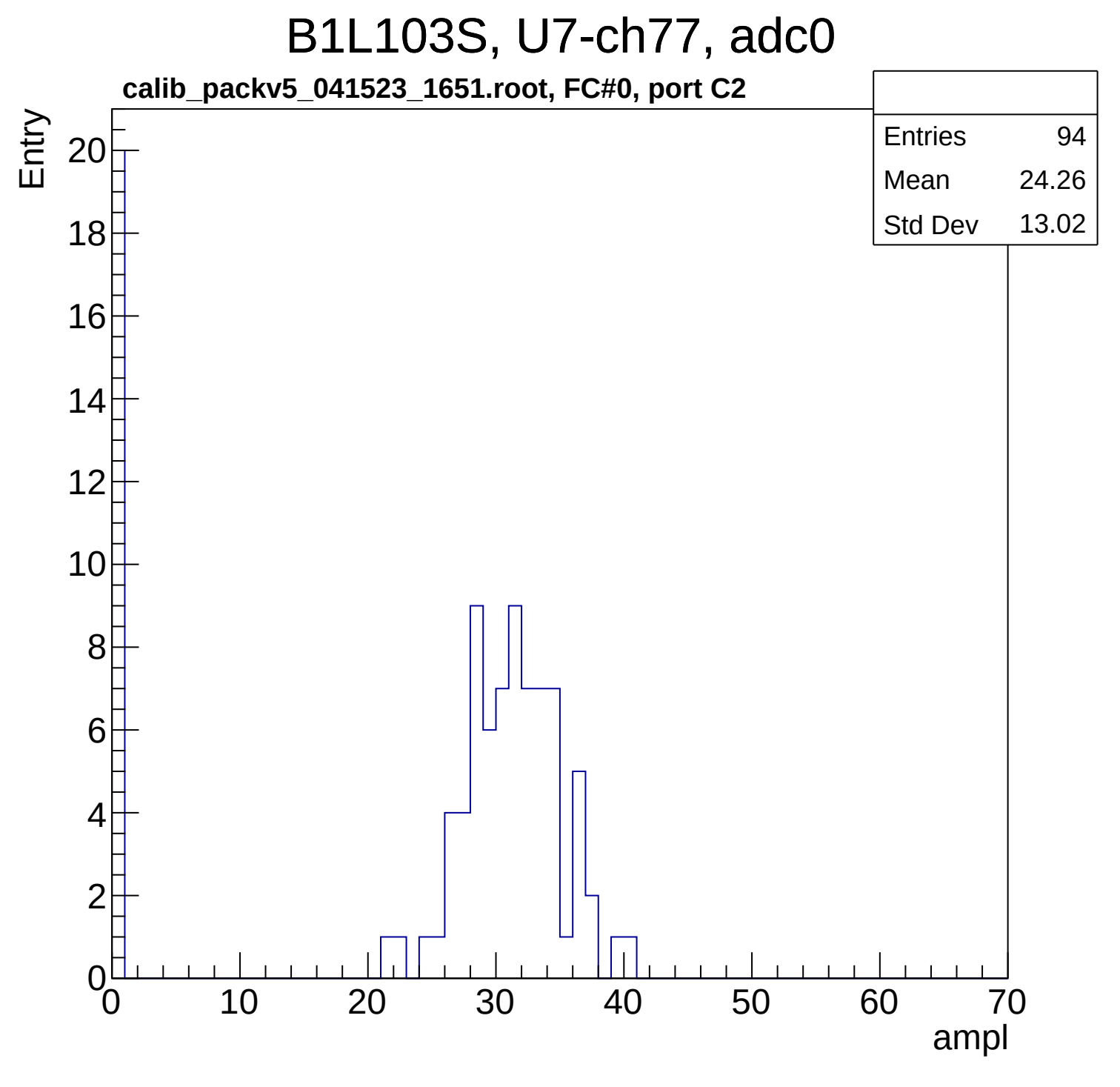

B1L103S, U7-ch76, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch77, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 94
Mean 24.26
Std Dev 13.02
Entry
0
2
4
6
8
10
12
14
16
18
20
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10
20
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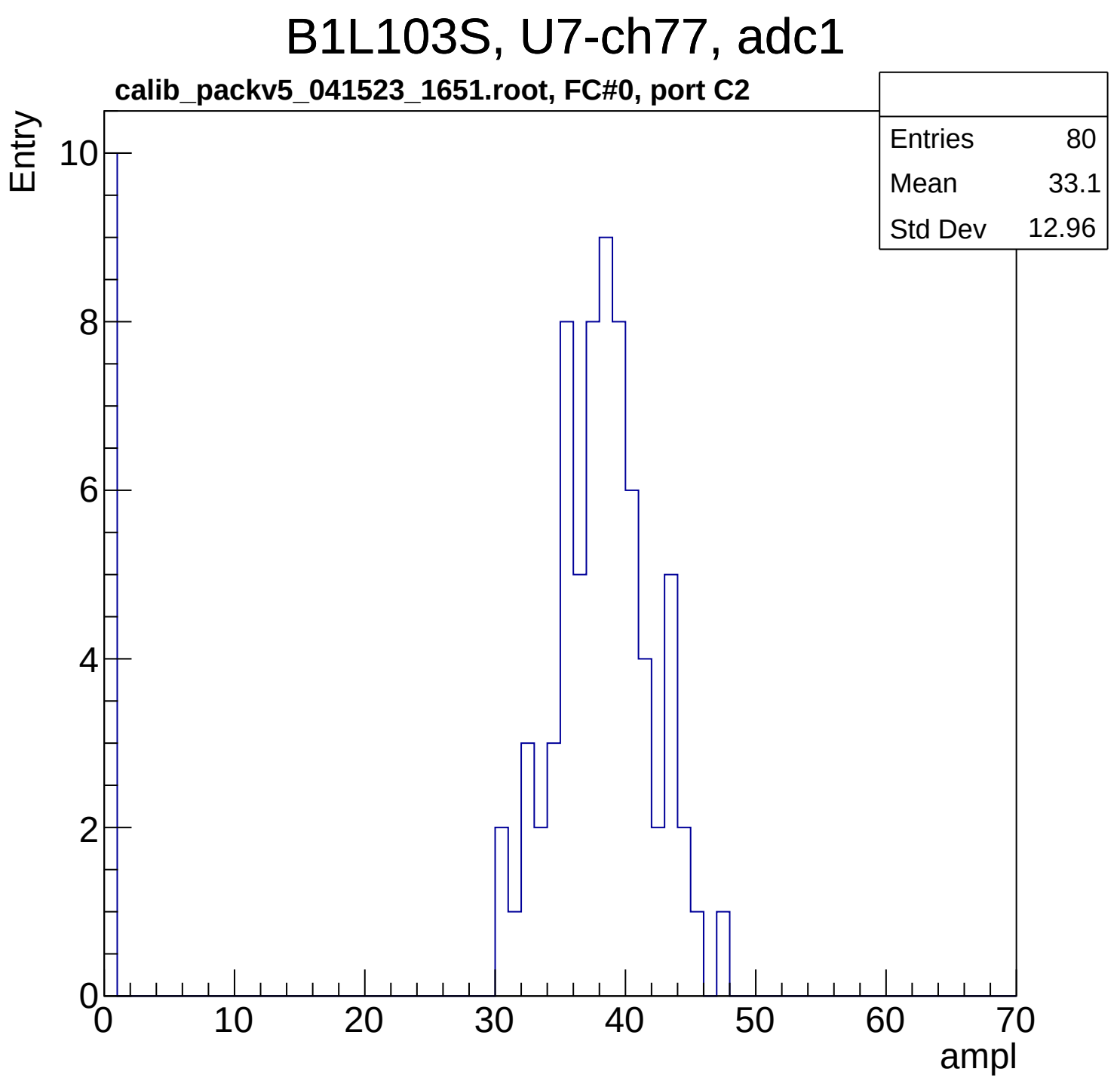
50
60
70
ampl


B1L103S, U7-ch77, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 33.1
Std Dev 12.96
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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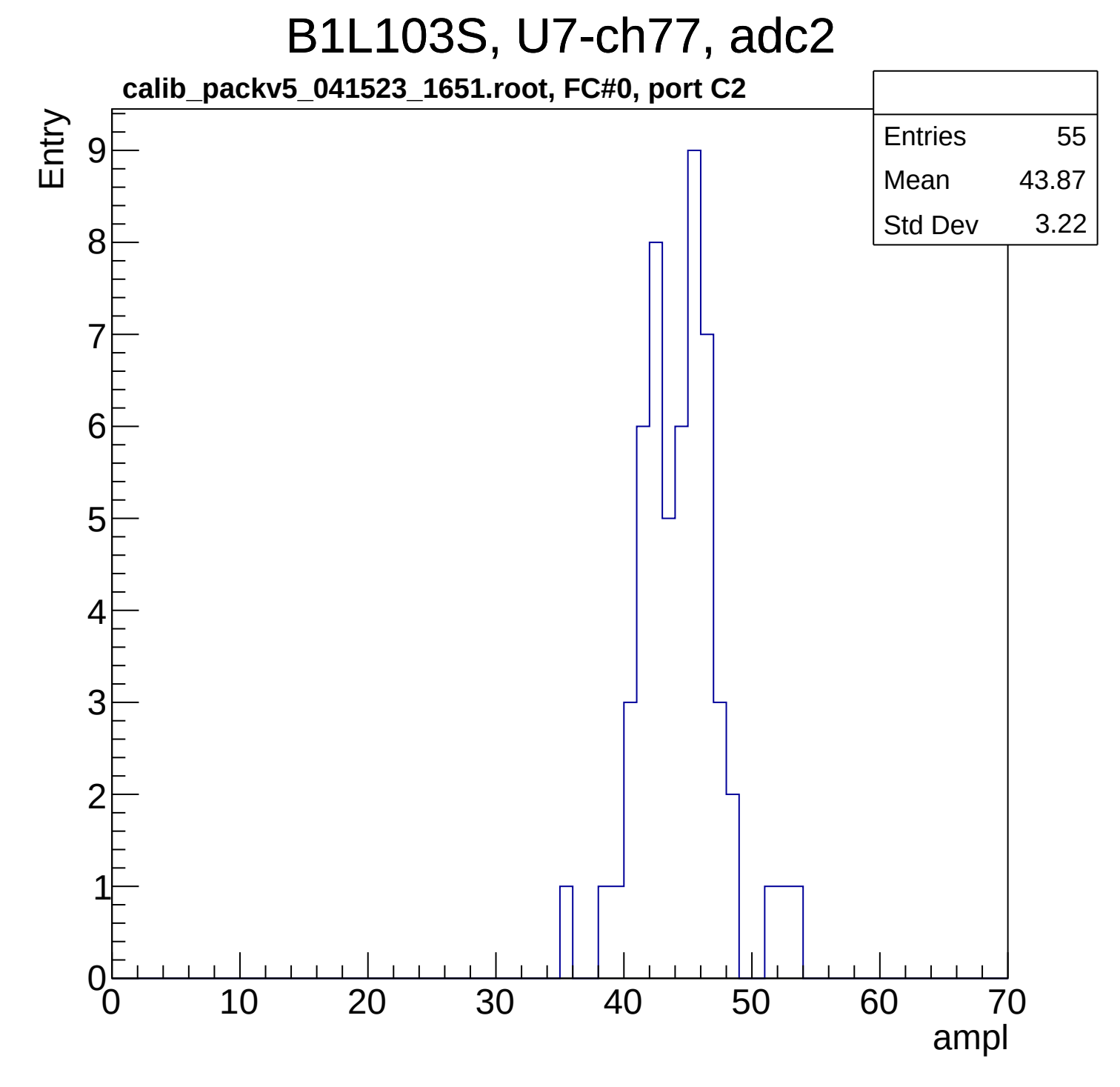
B1L103S, U7-ch77, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 43.87
Std Dev 3.22
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
50
60
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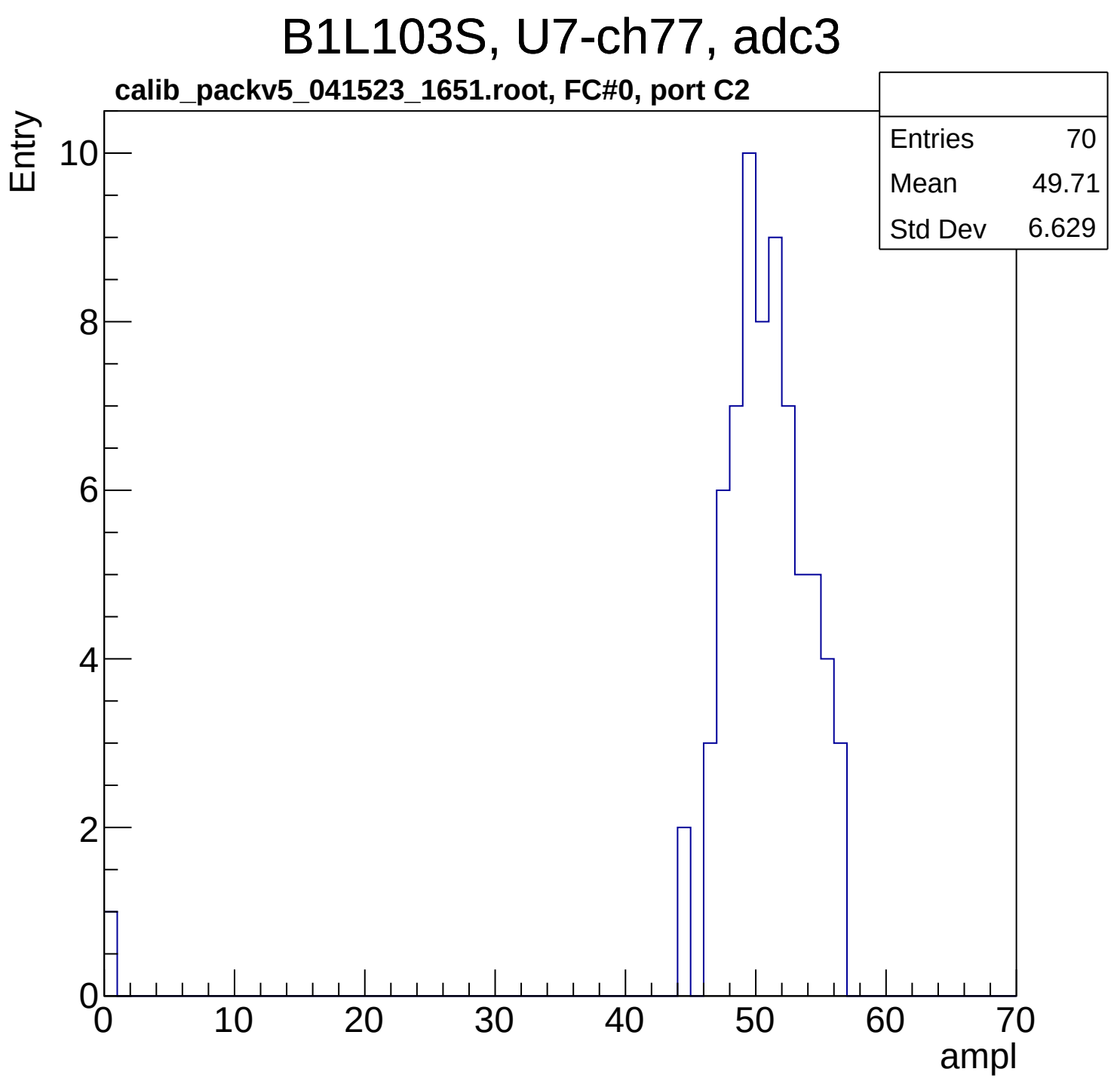
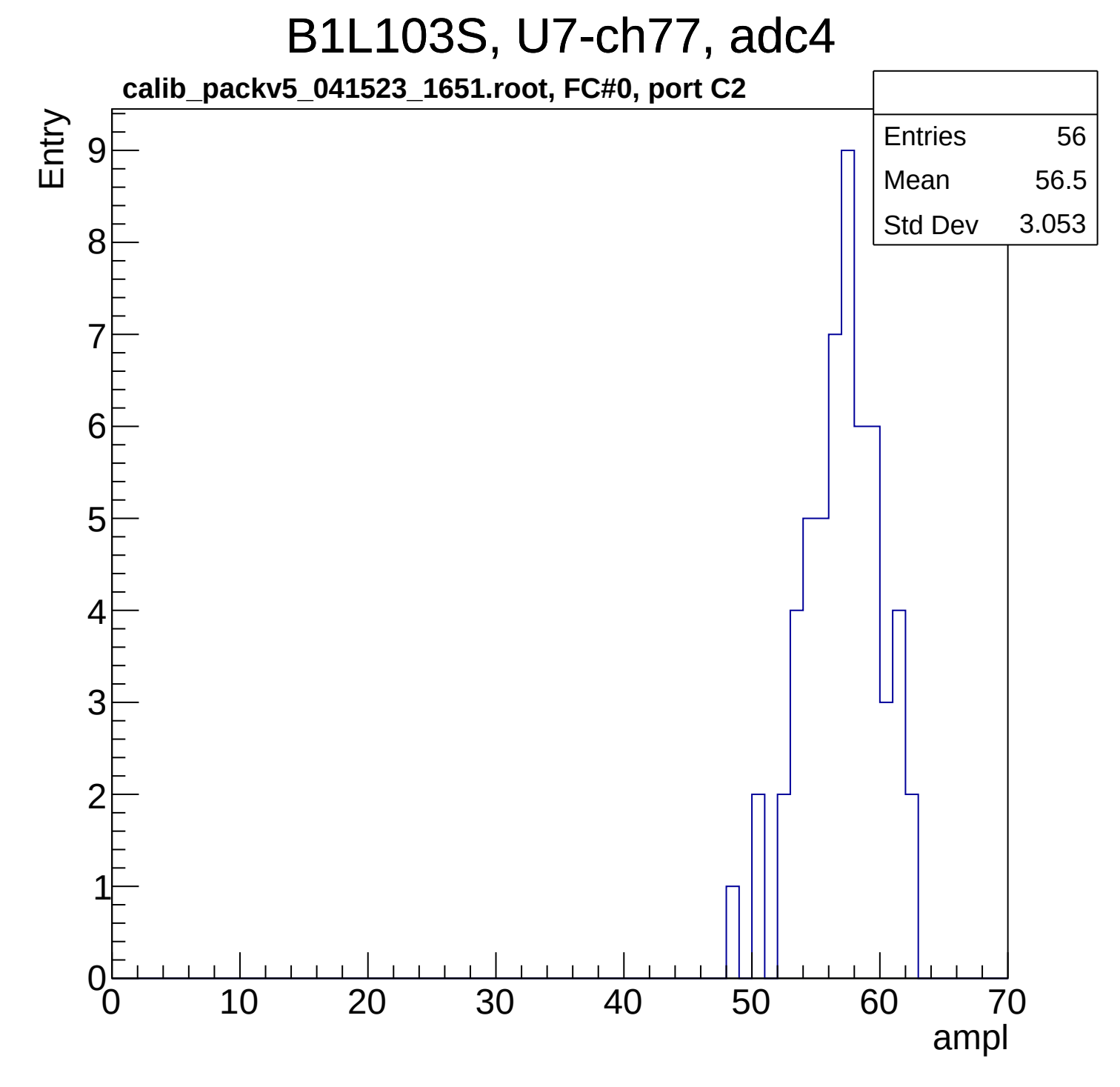

B1L103S, U7-ch77, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 49.71
Std Dev 6.629
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch77, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 56.5
Std Dev 3.053
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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50
60
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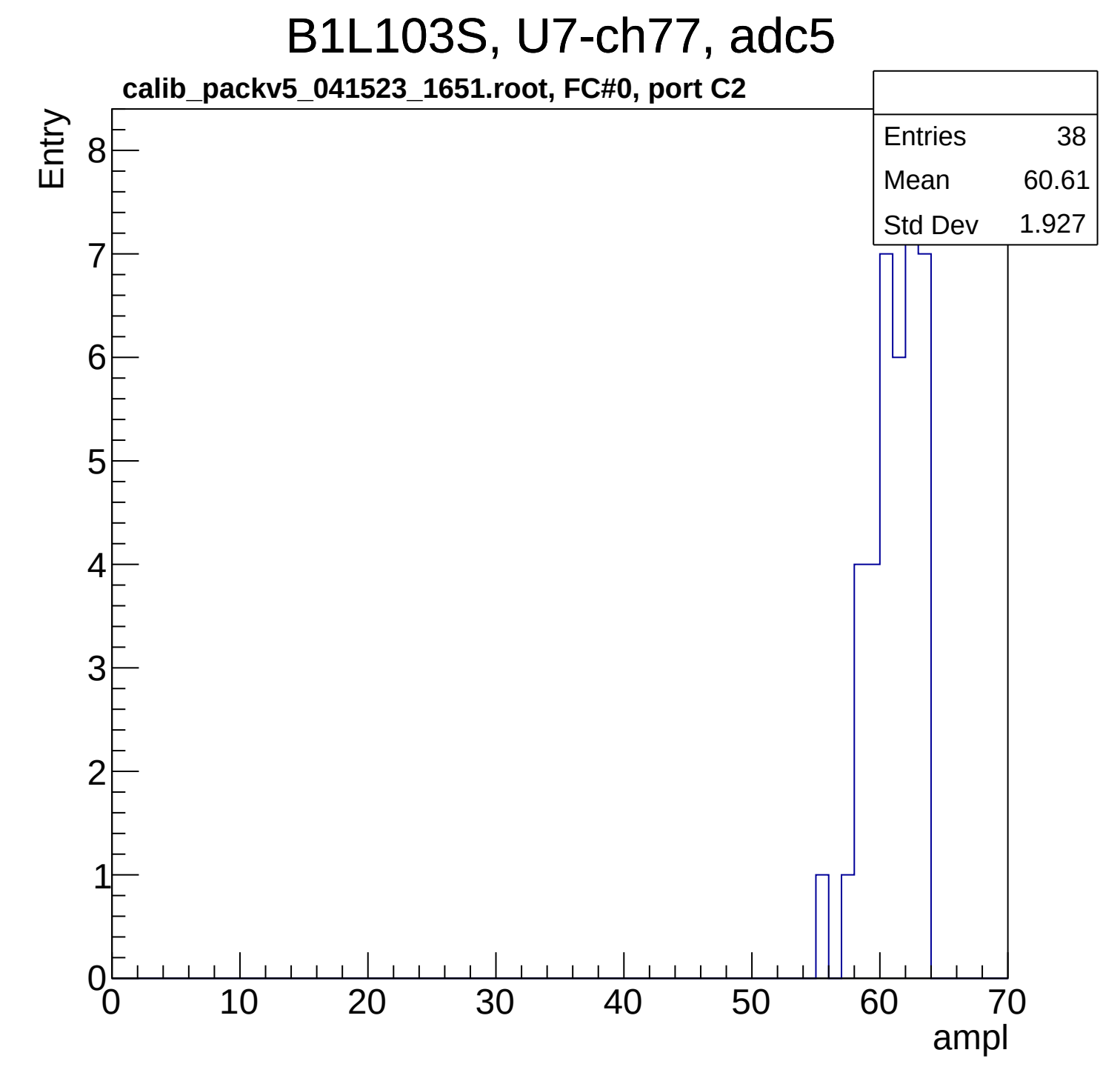
B1L103S, U7-ch77, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 38
Mean 60.61
Std Dev 1.927
Entry
ampl
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1
2
3
4
5
6
7
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0
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40
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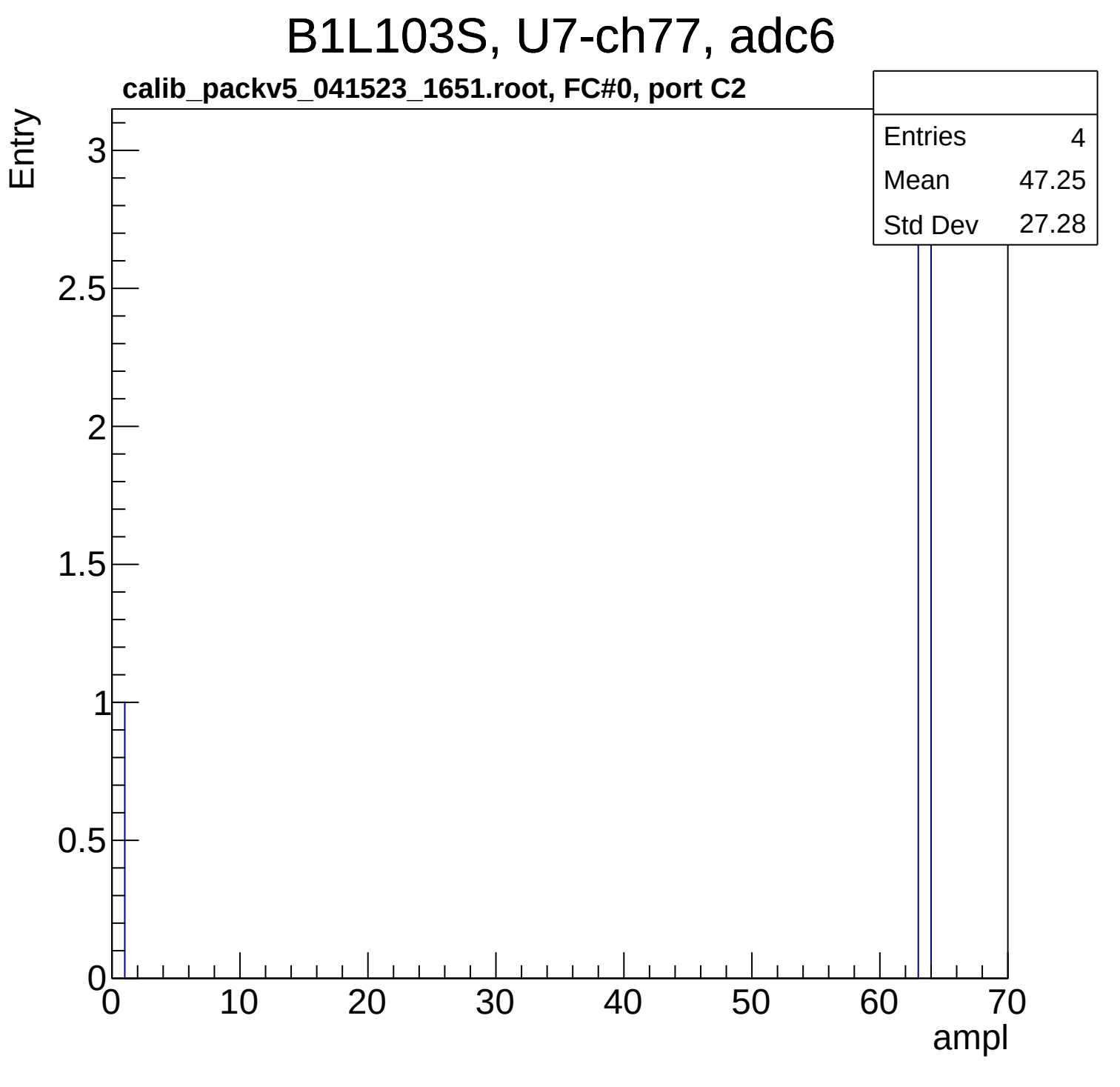
60
70


B1L103S, U7-ch77, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 4
Mean 47.25
Std Dev 27.28
Entry
ampl
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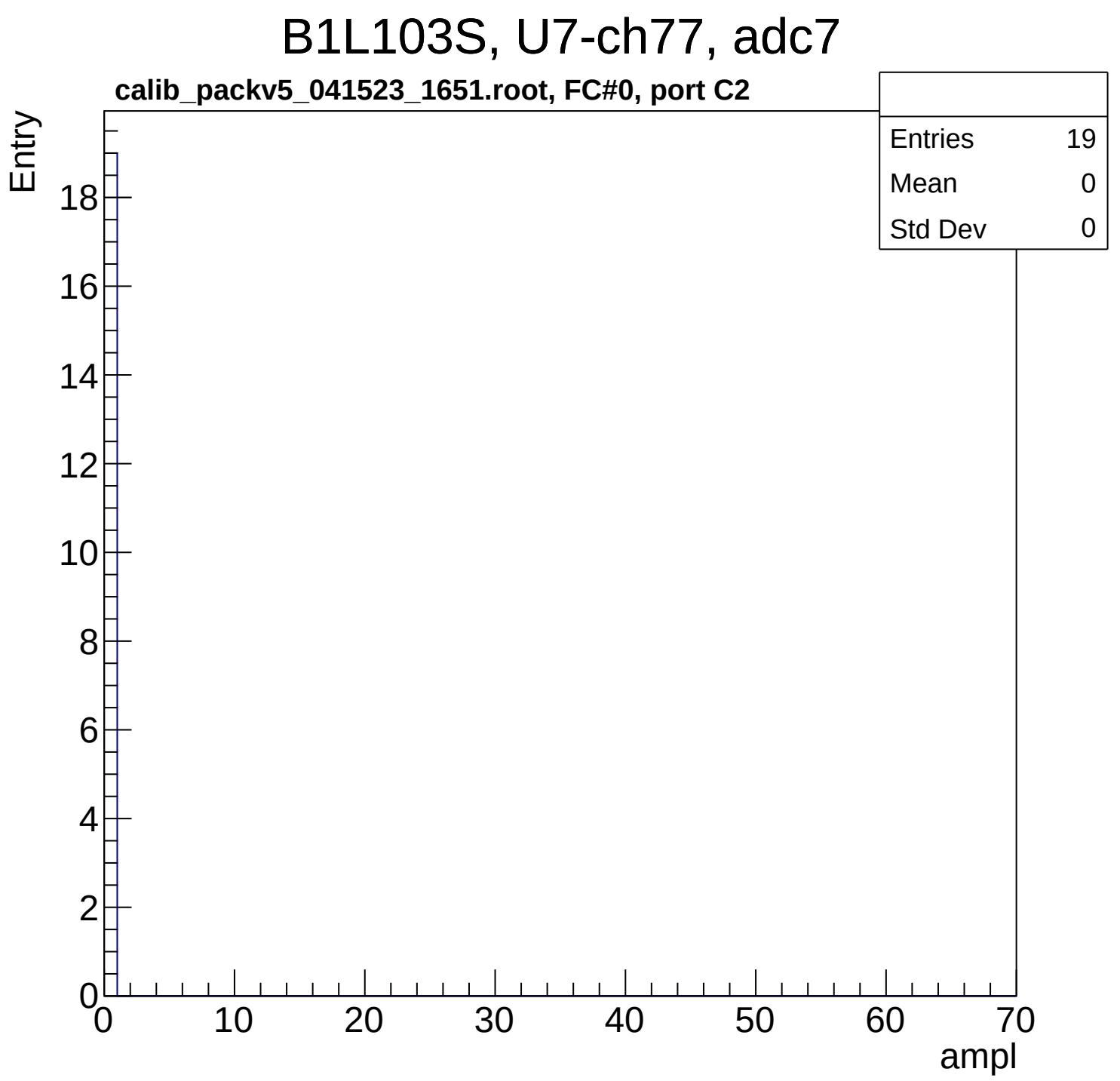
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U7-ch77, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
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10
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30
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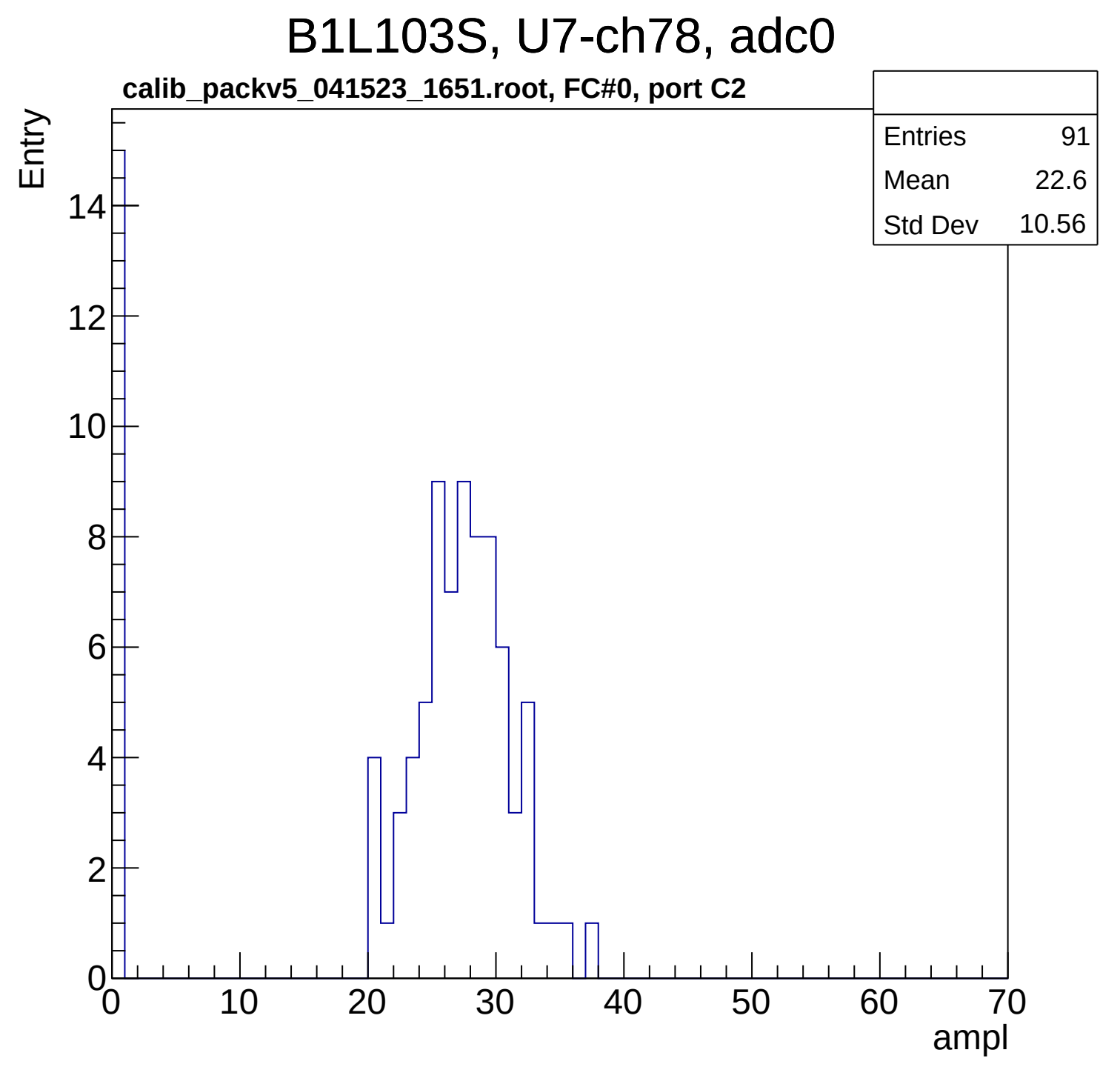
50
60
70
ampl


B1L103S, U7-ch78, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 91
Mean 22.6
Std Dev 10.56
Entry
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6
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10
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10
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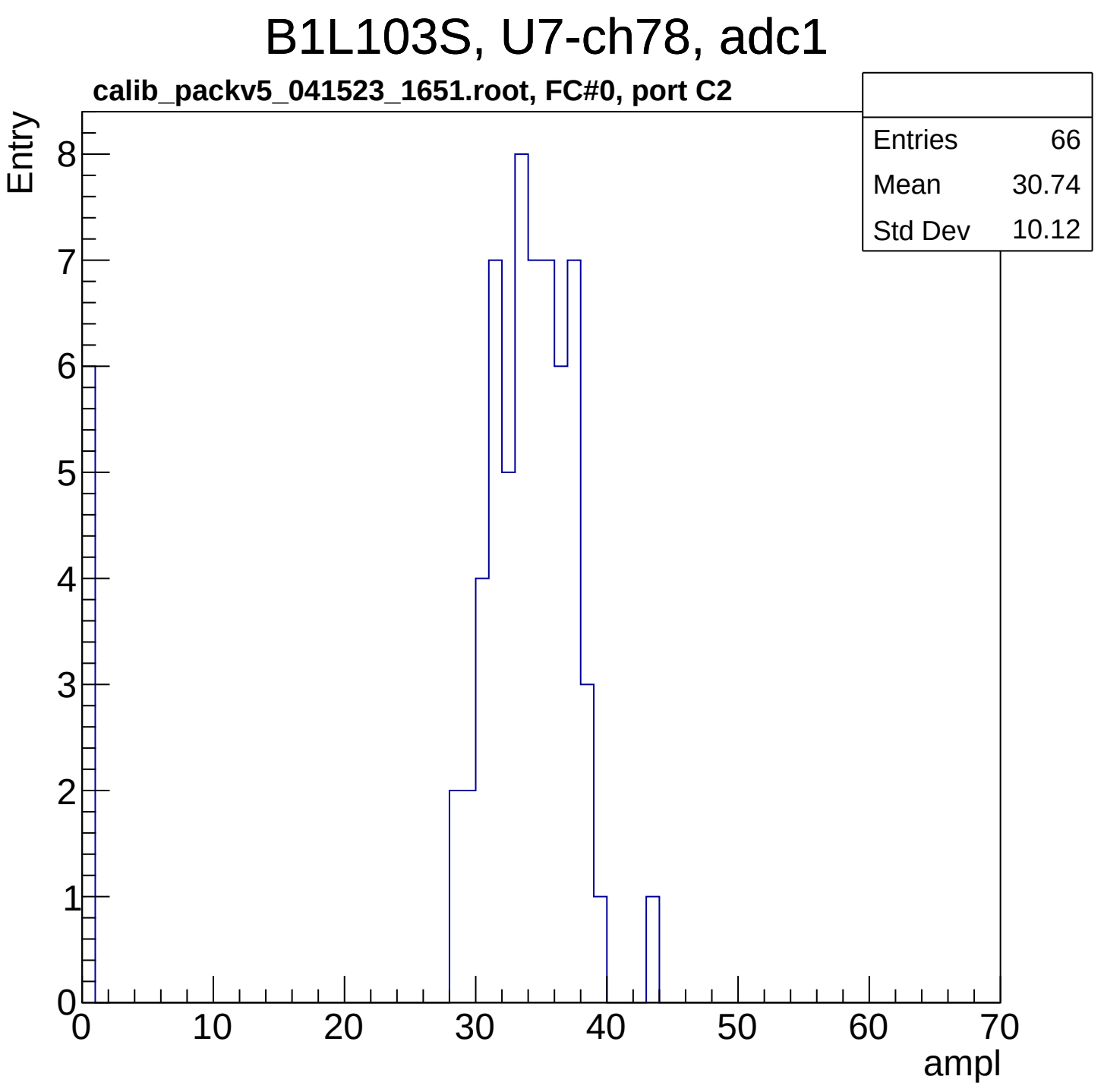
70
ampl


B1L103S, U7-ch78, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 30.74
Std Dev 10.12
Entry
ampl
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2
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4
5
6
7
8
0
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20
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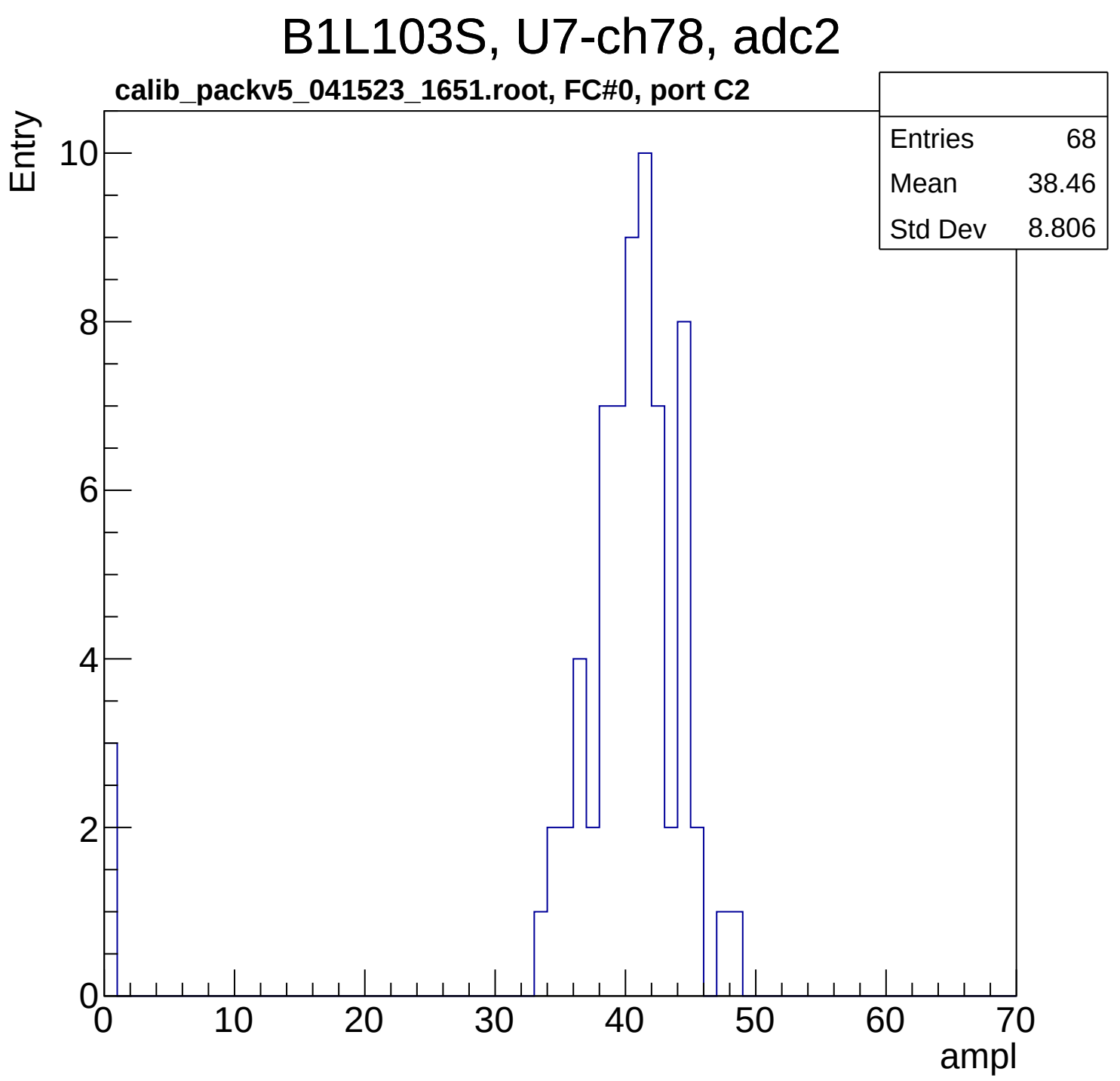
40
50
60
70


B1L103S, U7-ch78, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 38.46
Std Dev 8.806
Entry
ampl
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2
4
6
8
10
0
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20
30
40
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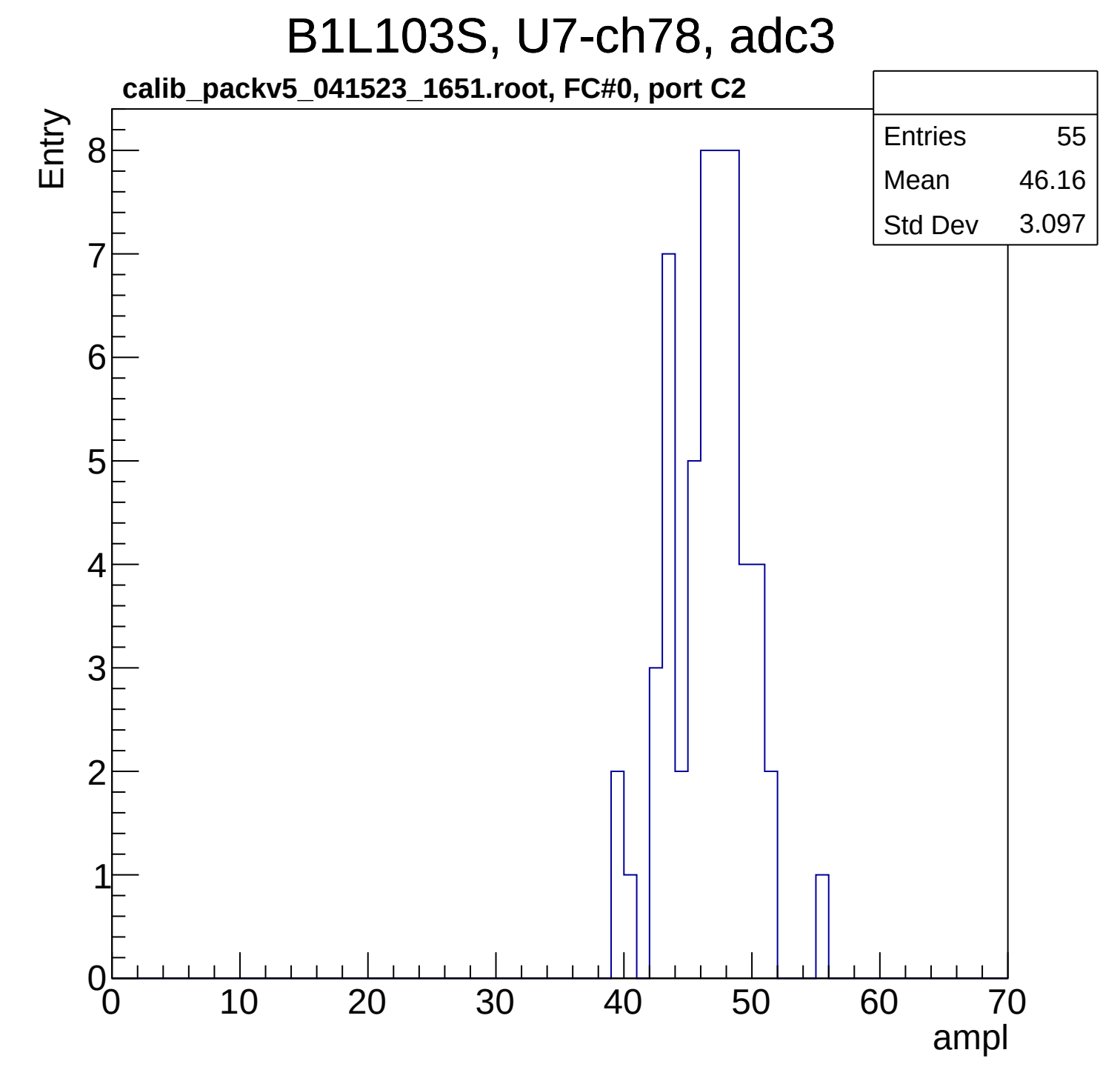
60
70


B1L103S, U7-ch78, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 46.16
Std Dev 3.097
Entry
ampl
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2
3
4
5
6
7
8
0
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20
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60
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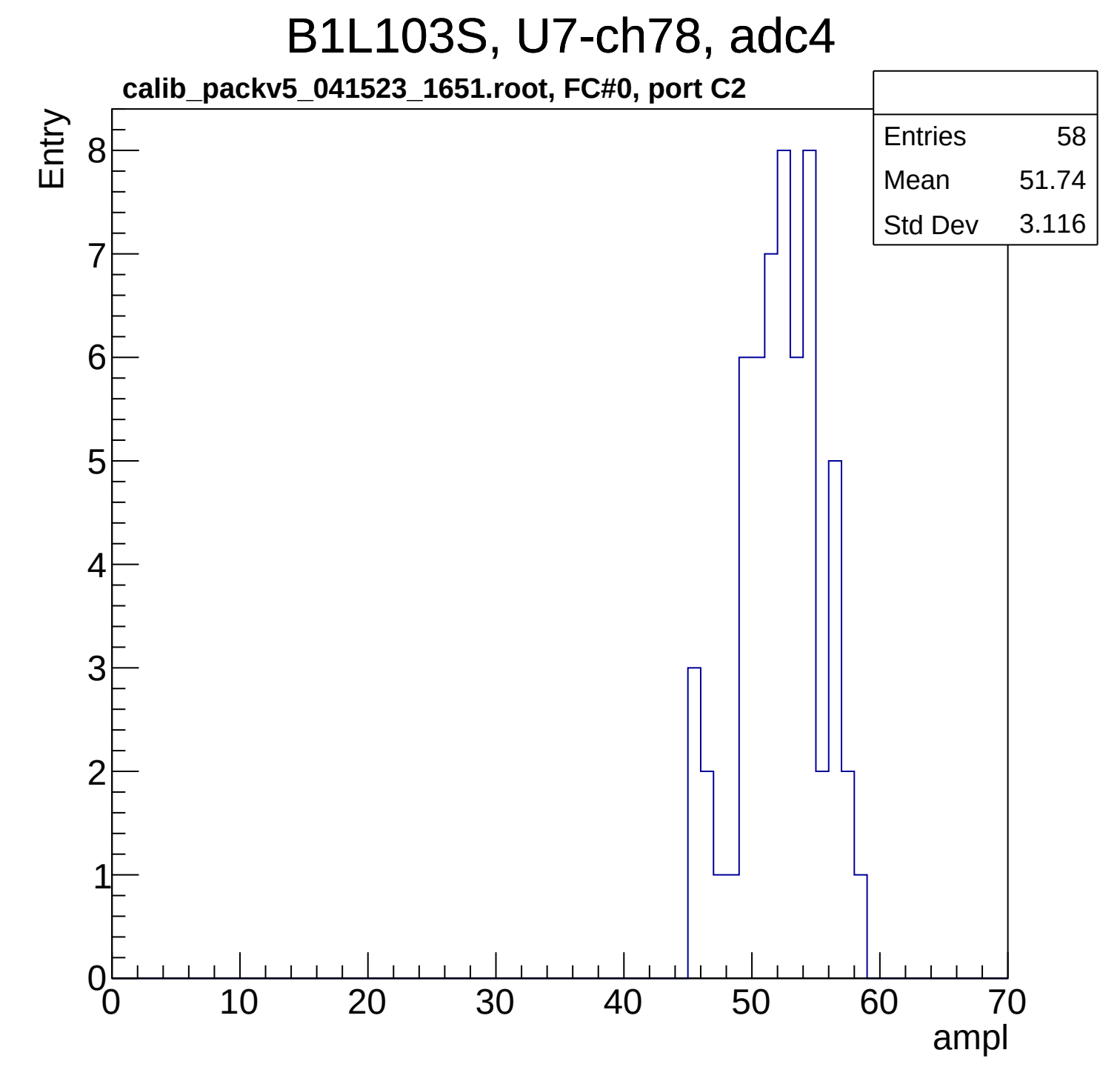
B1L103S, U7-ch78, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 51.74
Std Dev 3.116
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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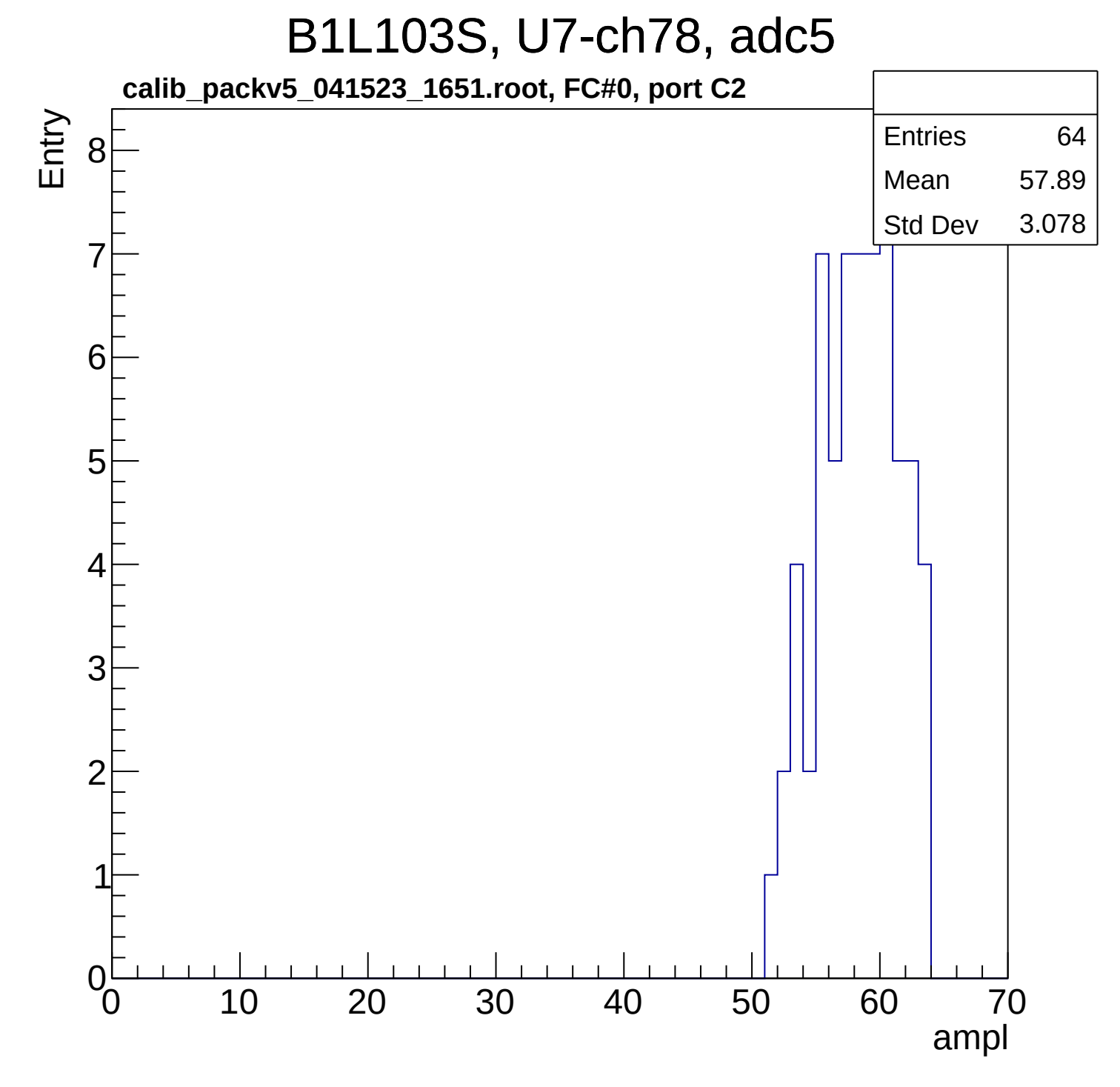
40
50
60
70


B1L103S, U7-ch78, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 57.89
Std Dev 3.078
Entry
ampl
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2
3
4
5
6
7
8
0
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20
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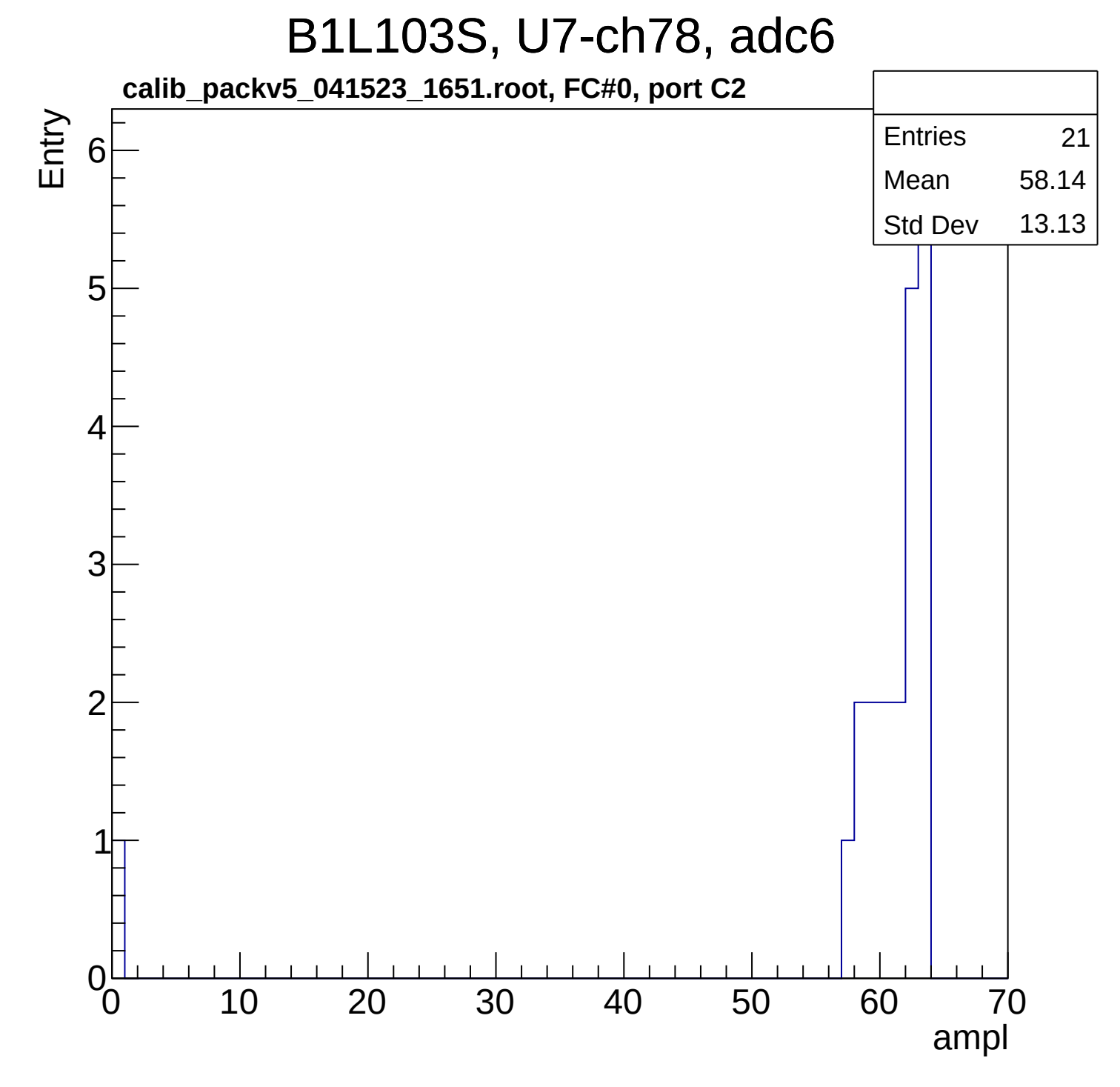
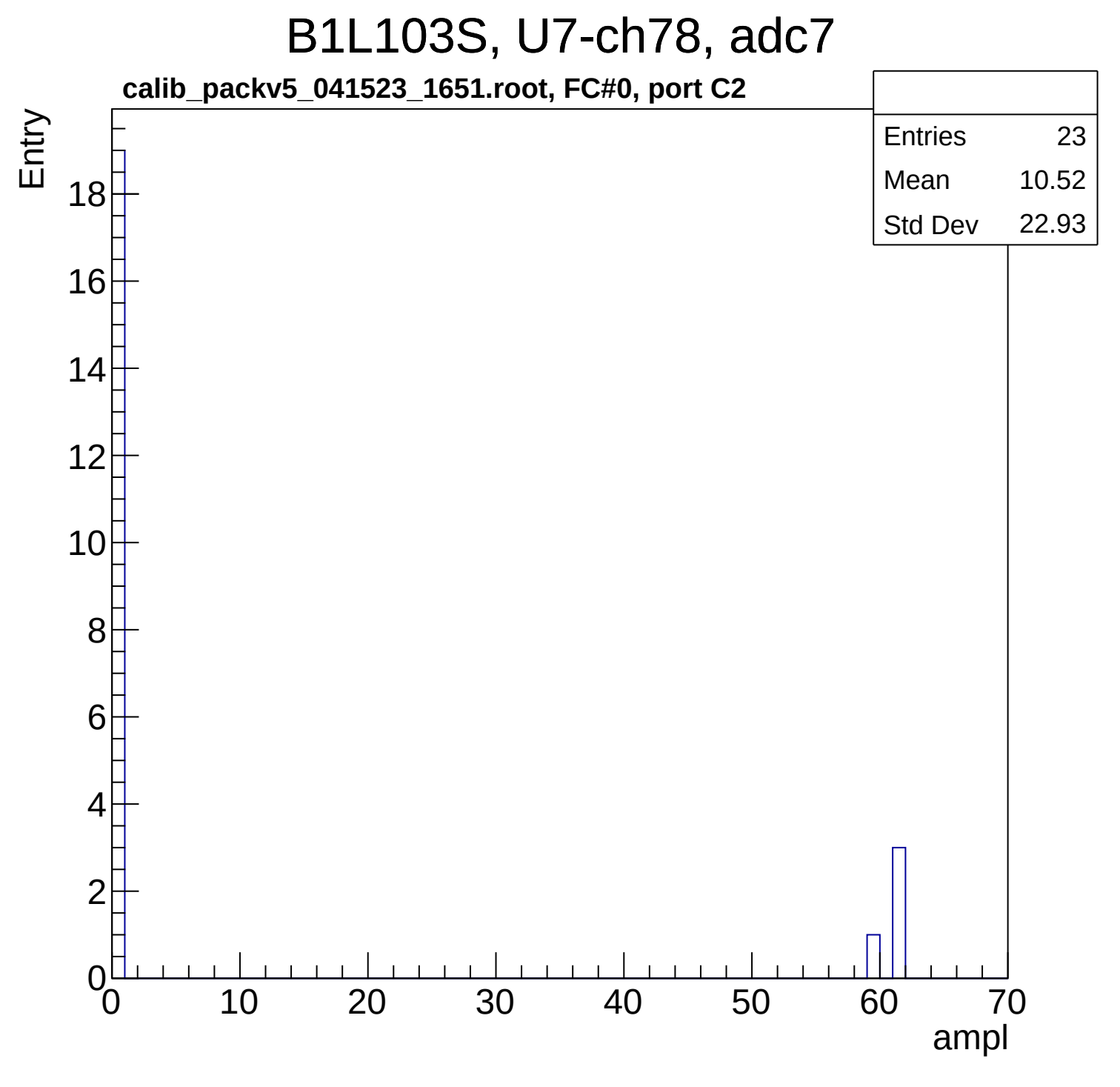
60
70


B1L103S, U7-ch78, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 58.14
Std Dev 13.13
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch78, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 23
Mean 10.52
Std Dev 22.93
Entry
0
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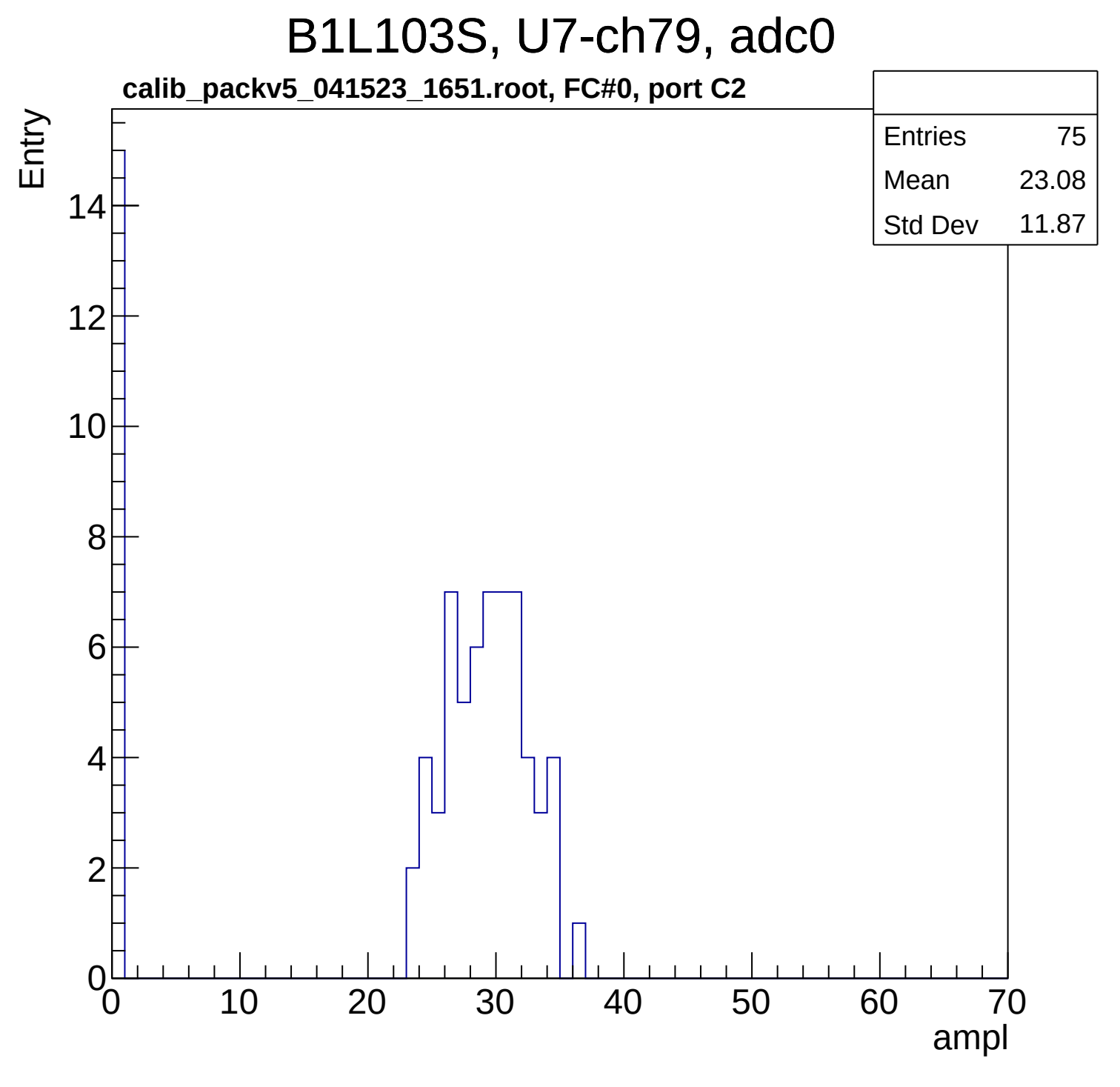
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch79, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 23.08
Std Dev 11.87
Entry
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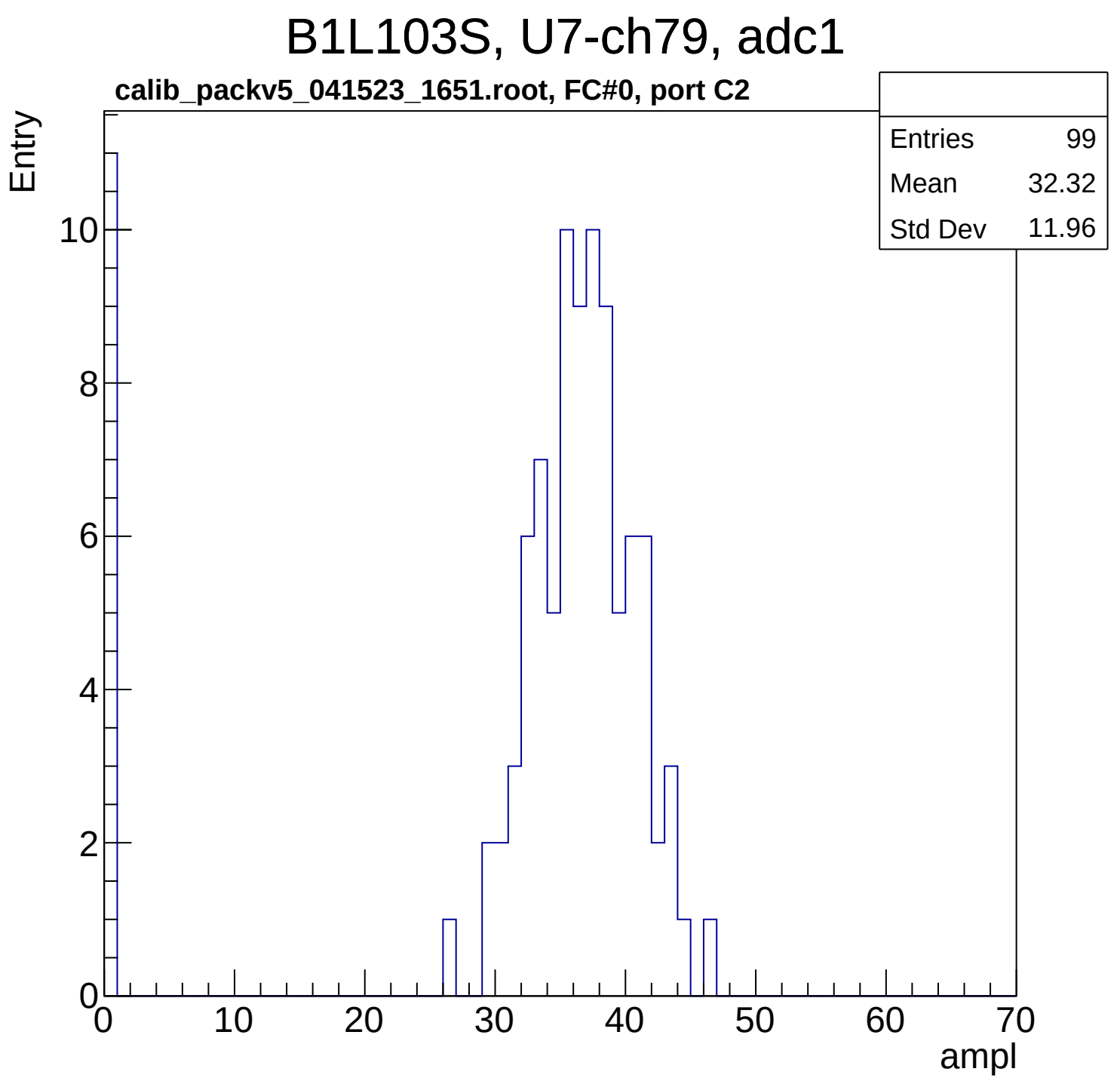
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch79, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 99
Mean 32.32
Std Dev 11.96
Entry
0
2
4
6
8
10
0
10
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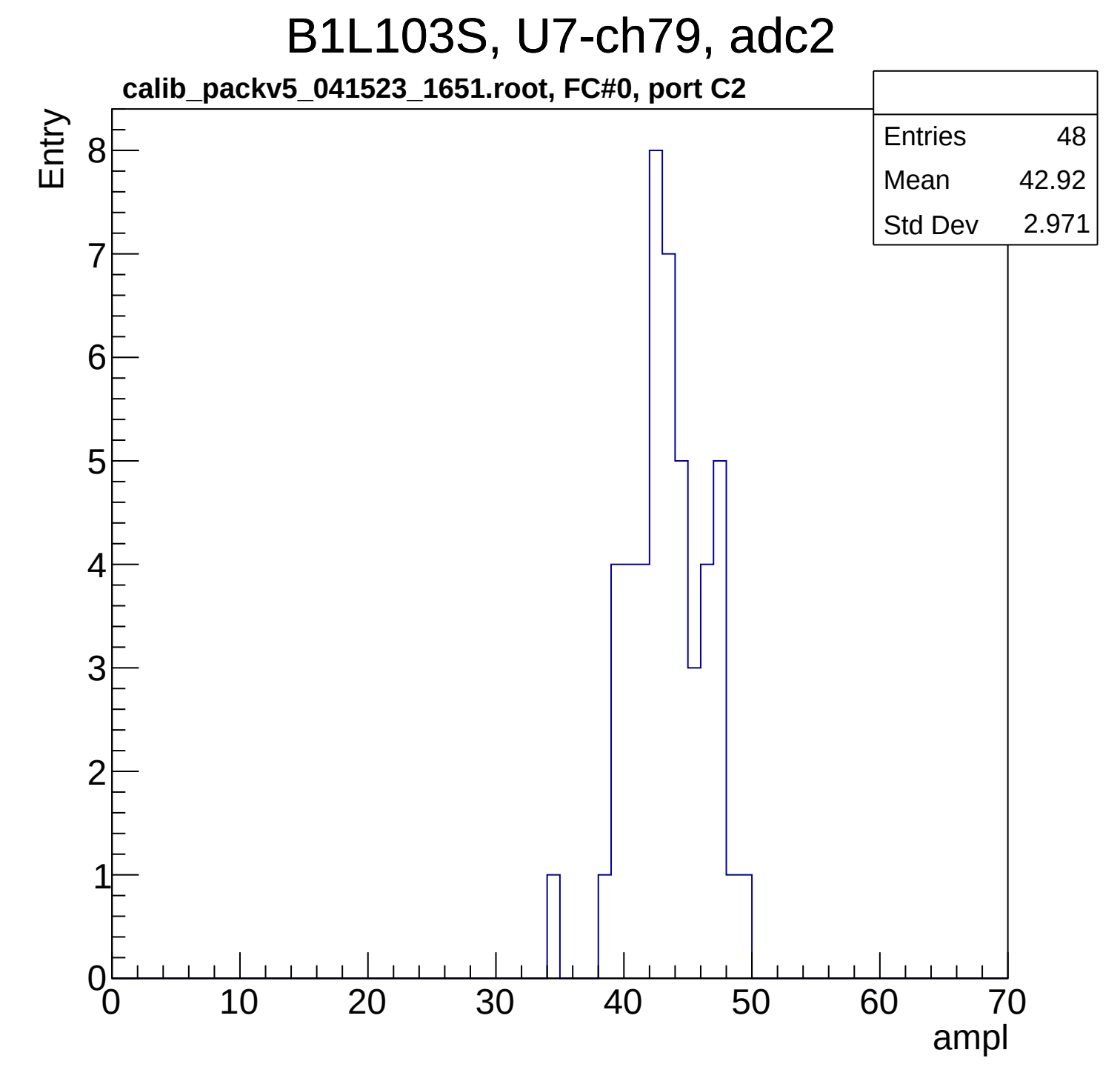
50
60
70
ampl


B1L103S, U7-ch79, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 42.92
Std Dev 2.971
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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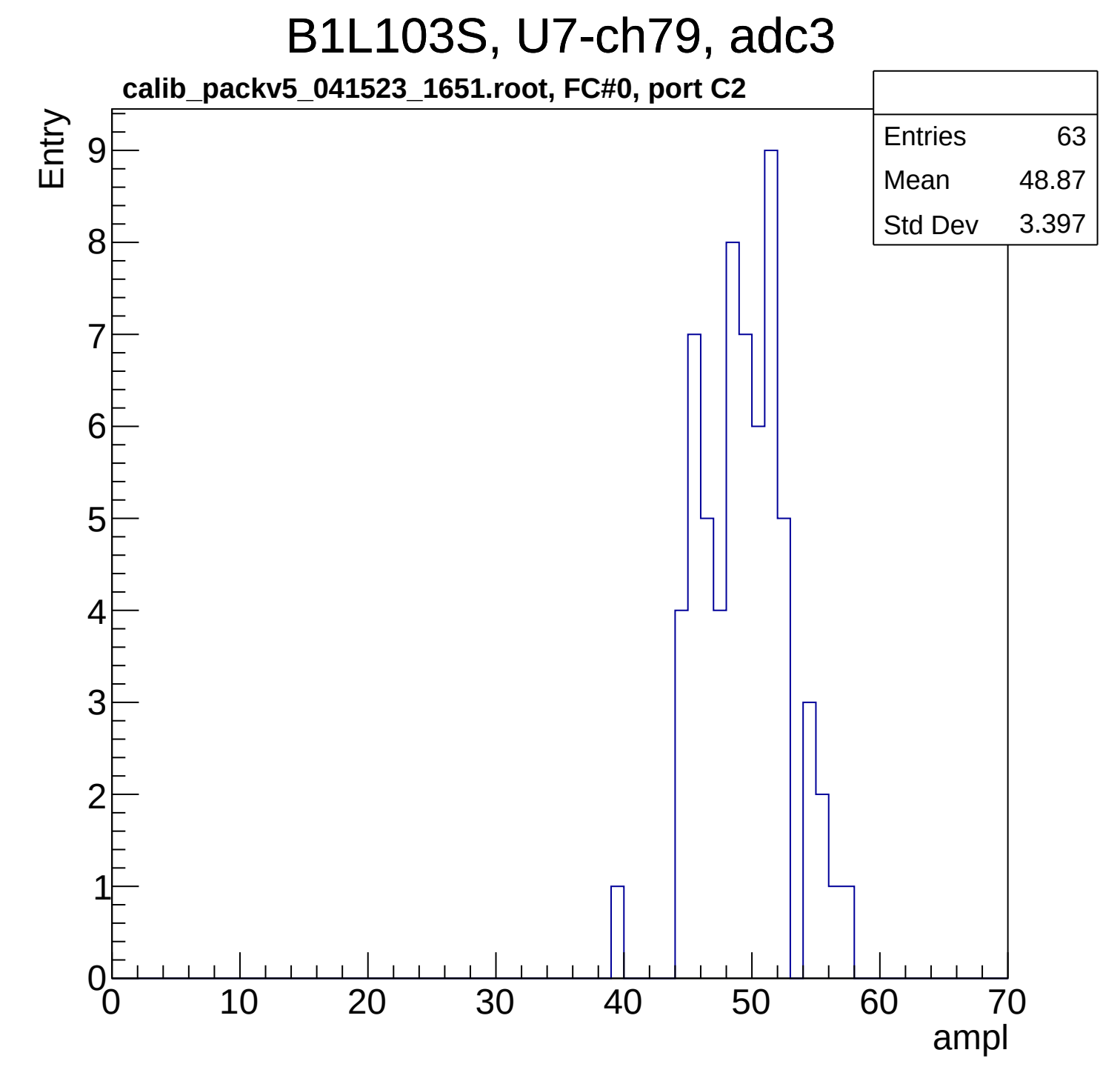
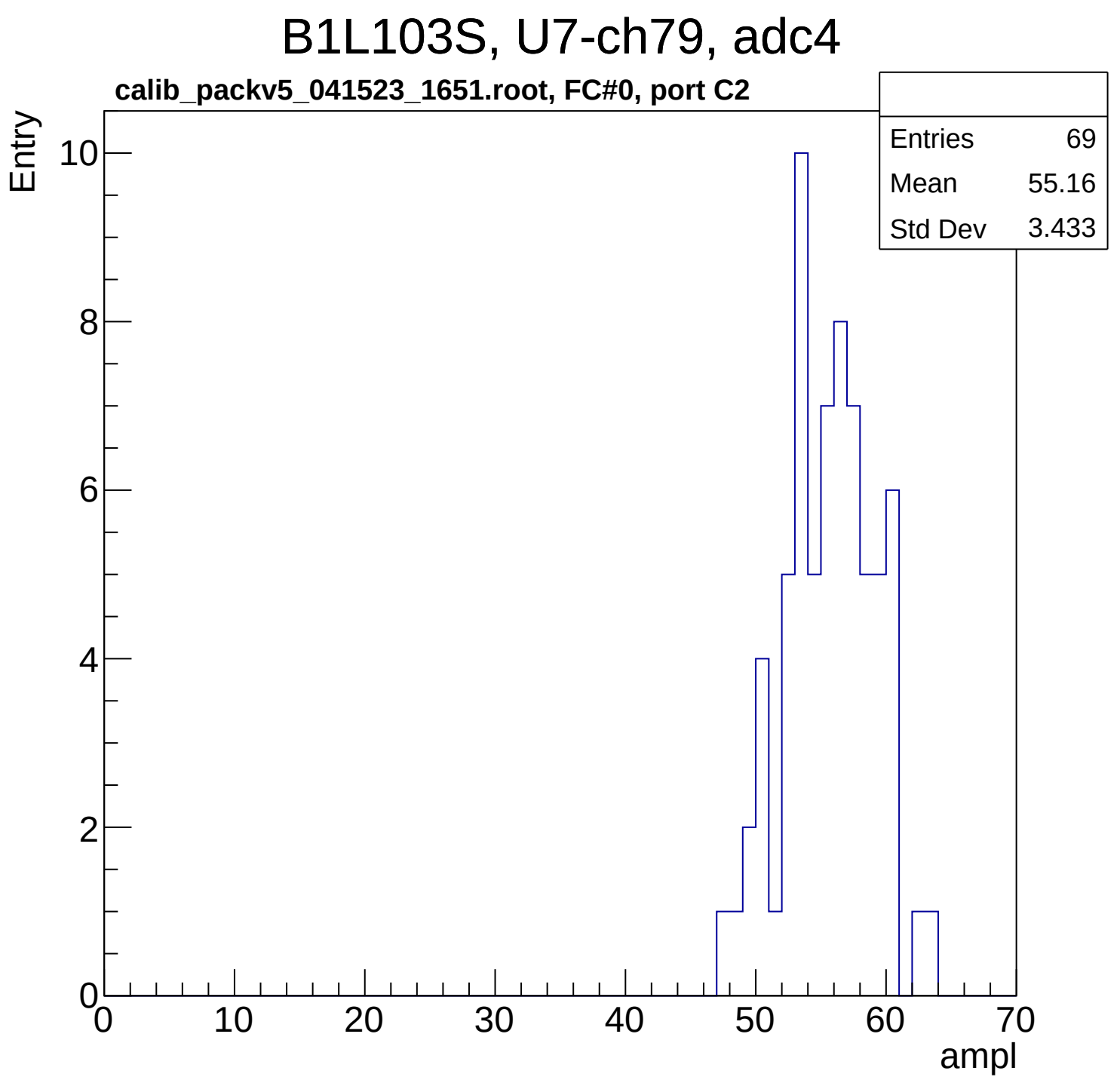
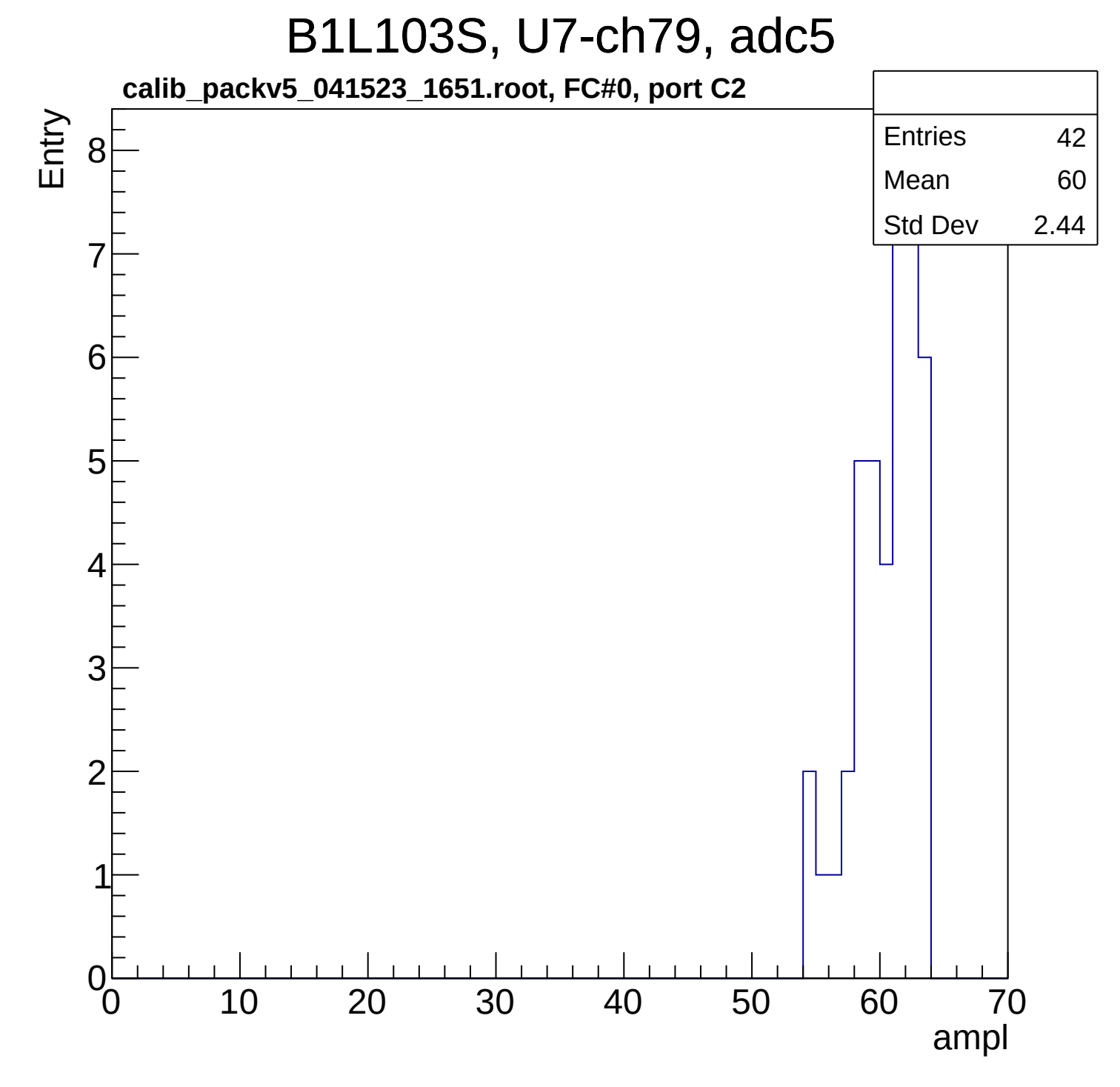

B1L103S, U7-ch79, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 48.87
Std Dev 3.397
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U7-ch79, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 55.16
Std Dev 3.433
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch79, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 42
Mean 60
Std Dev 2.44
Entry
ampl
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5
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0
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20
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40
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60
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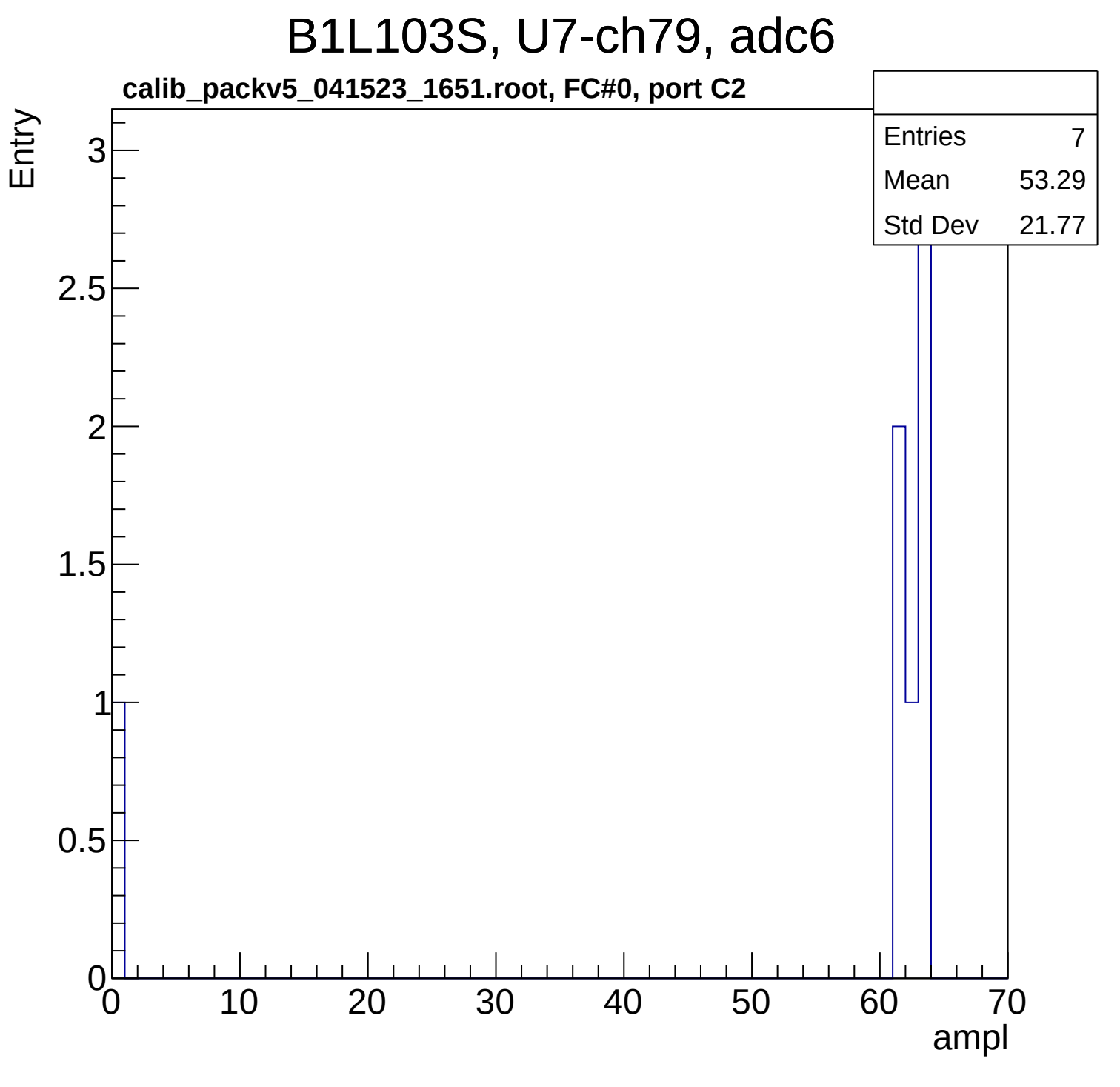
B1L103S, U7-ch79, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 53.29
Std Dev 21.77
Entry
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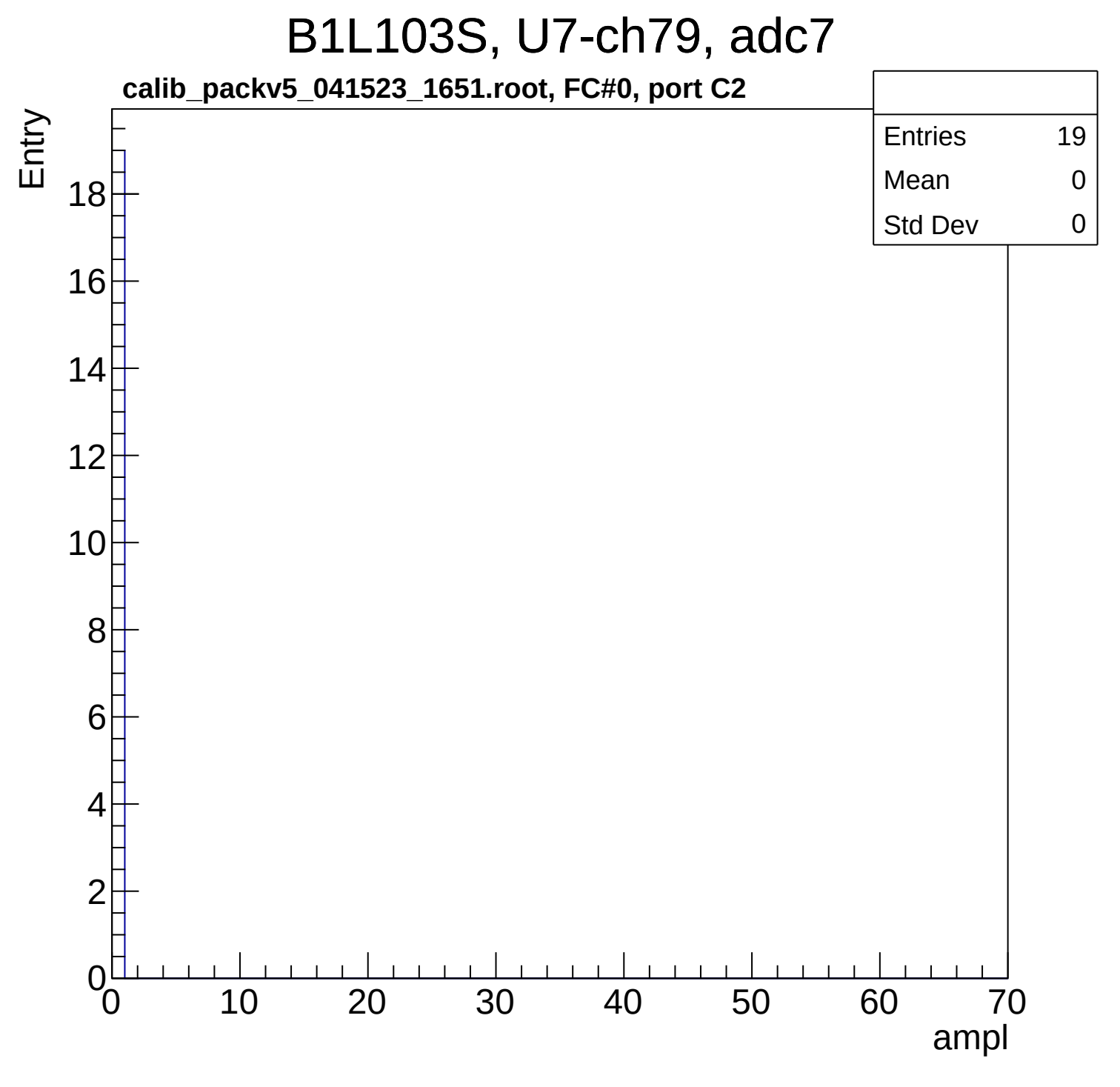
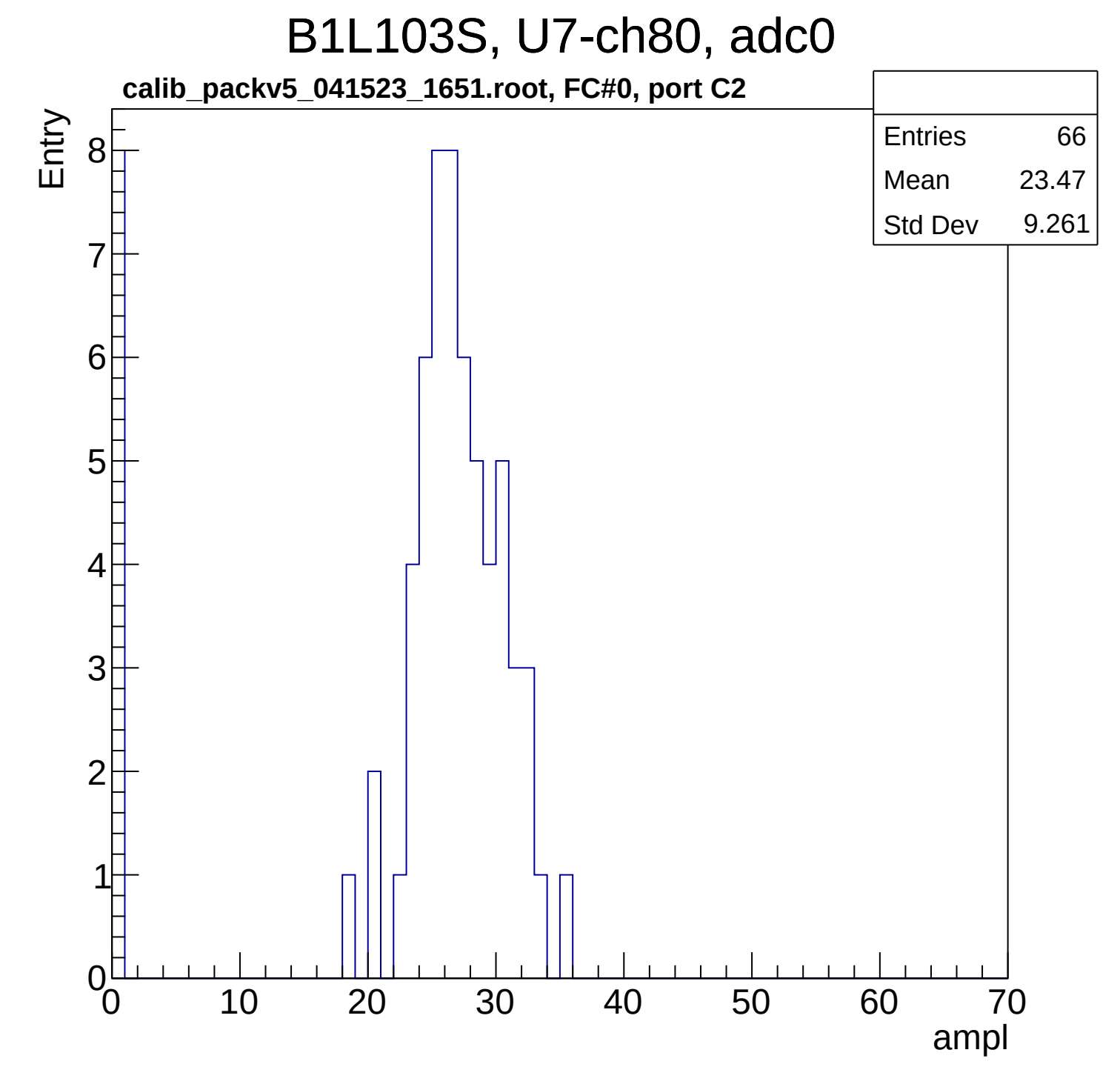
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch79, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch80, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 23.47
Std Dev 9.261
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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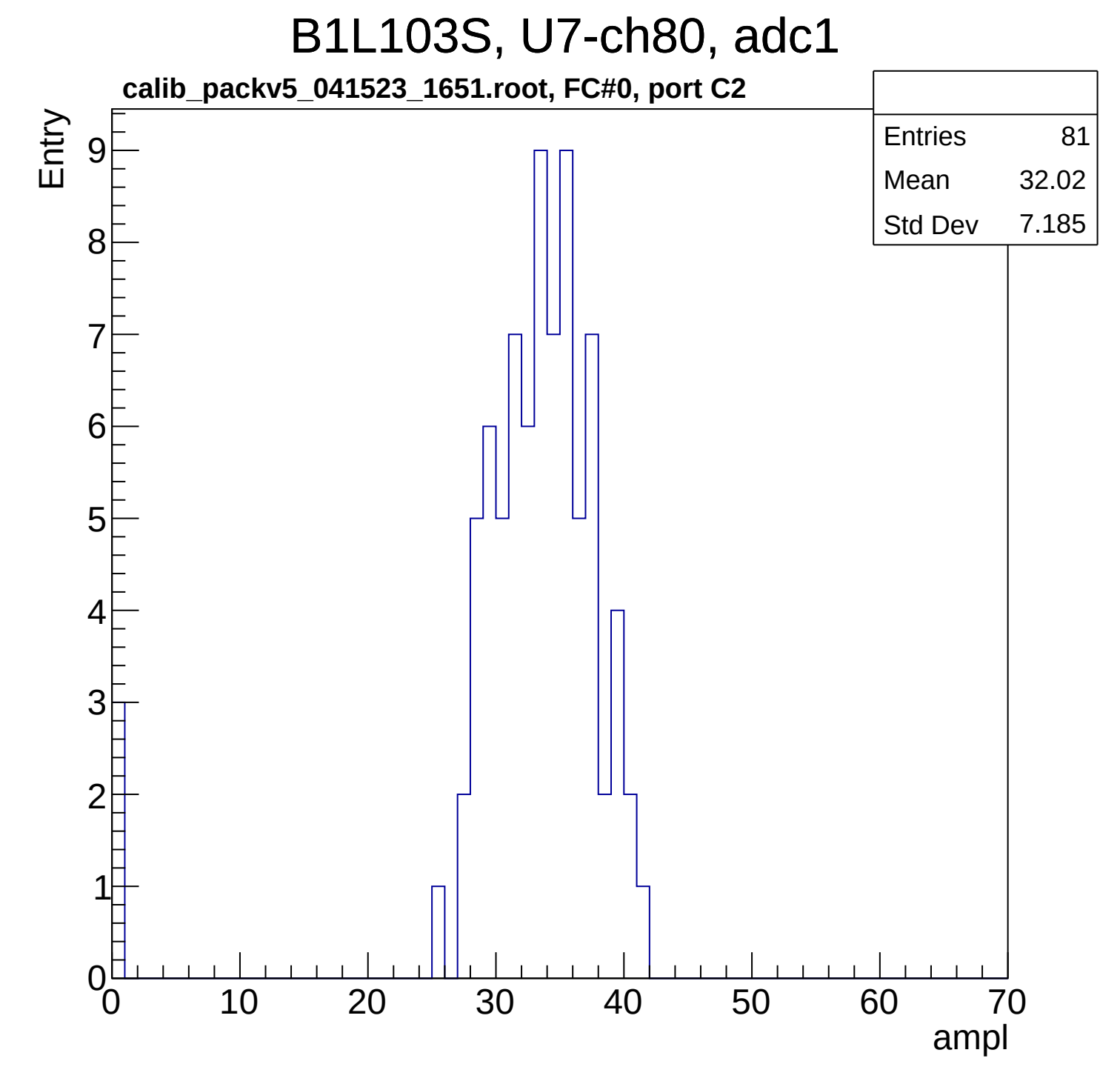
B1L103S, U7-ch80, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 32.02
Std Dev 7.185
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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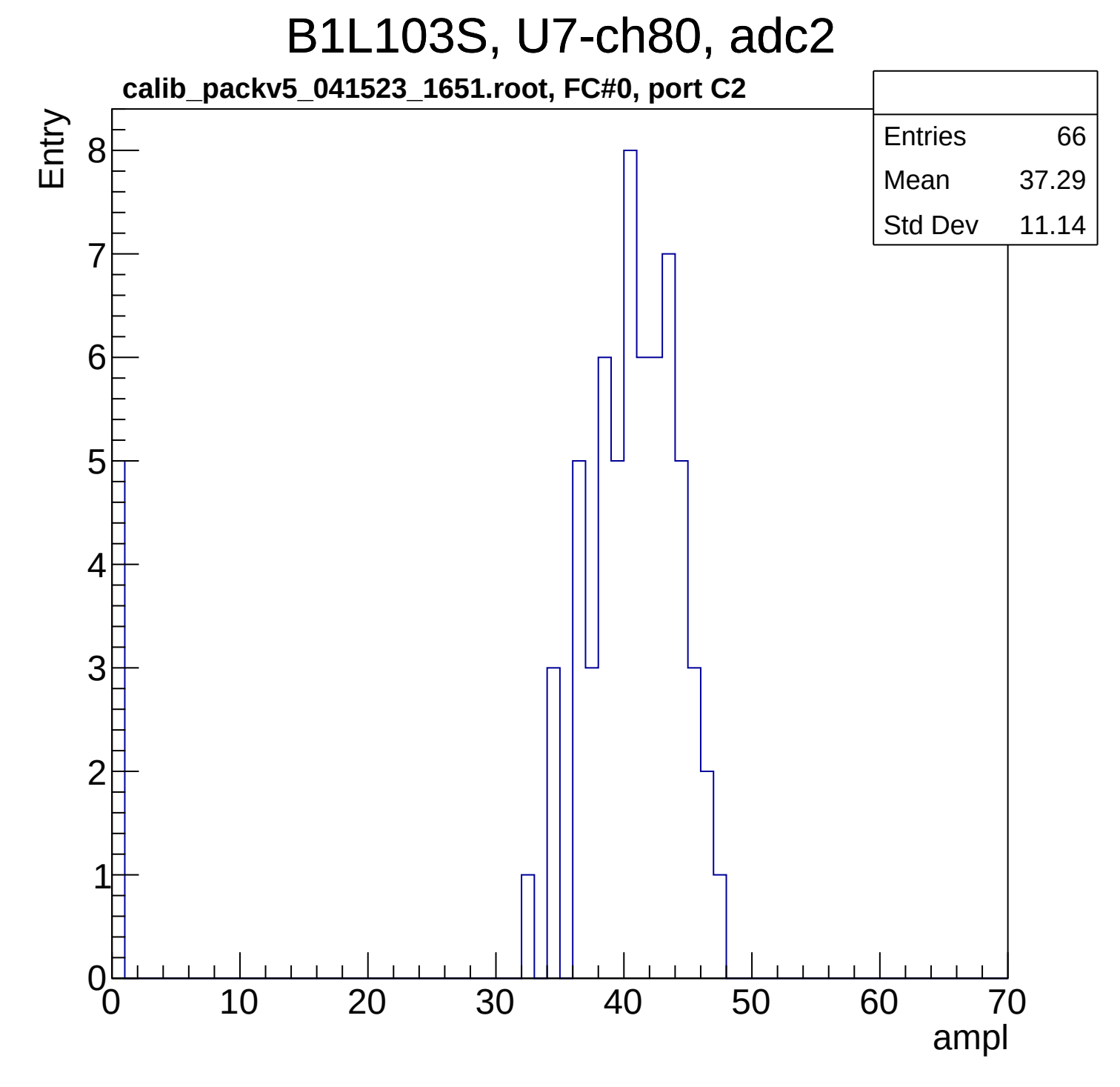
B1L103S, U7-ch80, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 37.29
Std Dev 11.14
Entry
ampl
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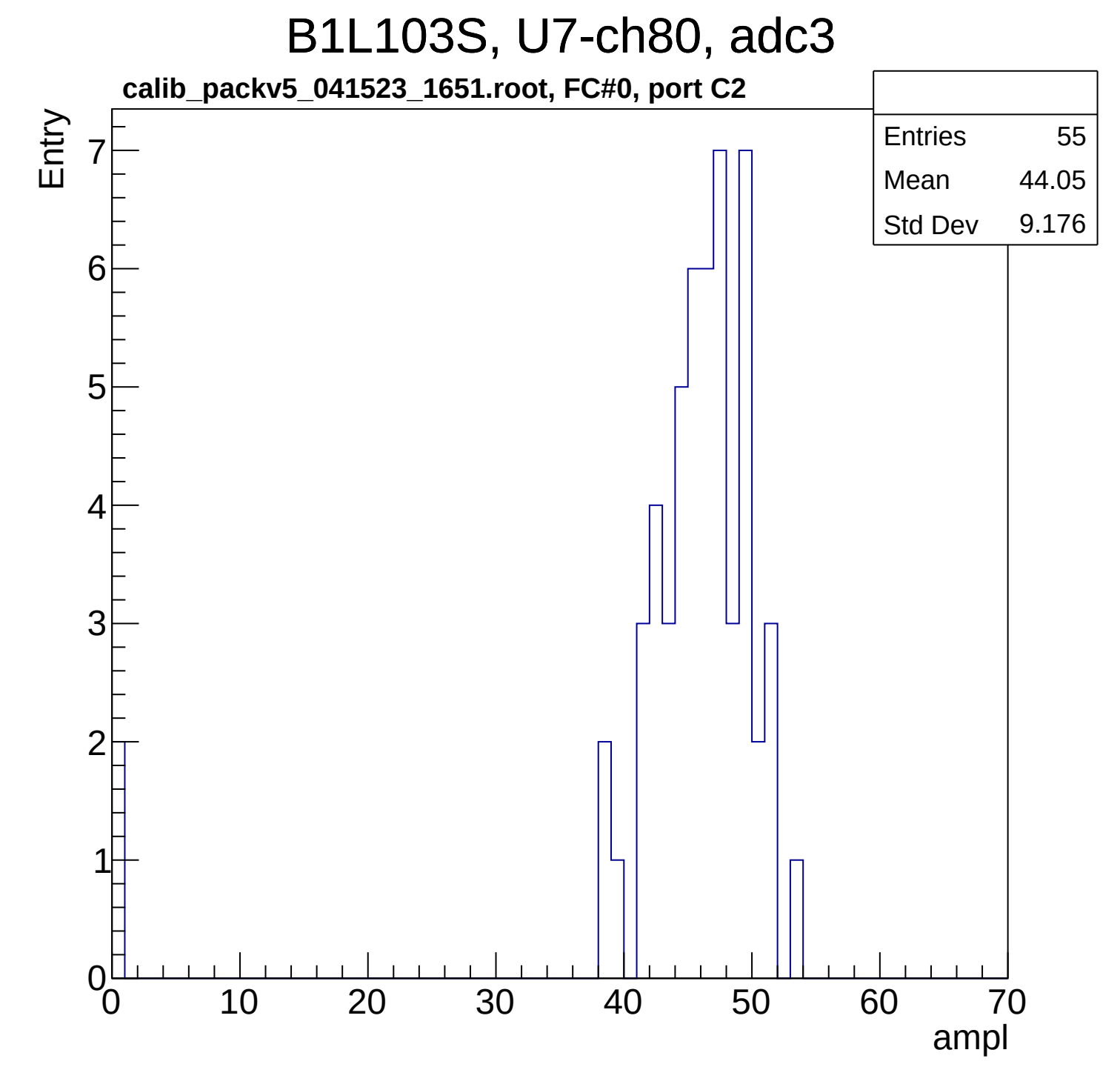
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch80, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 44.05
Std Dev 9.176
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
30
40
50
60
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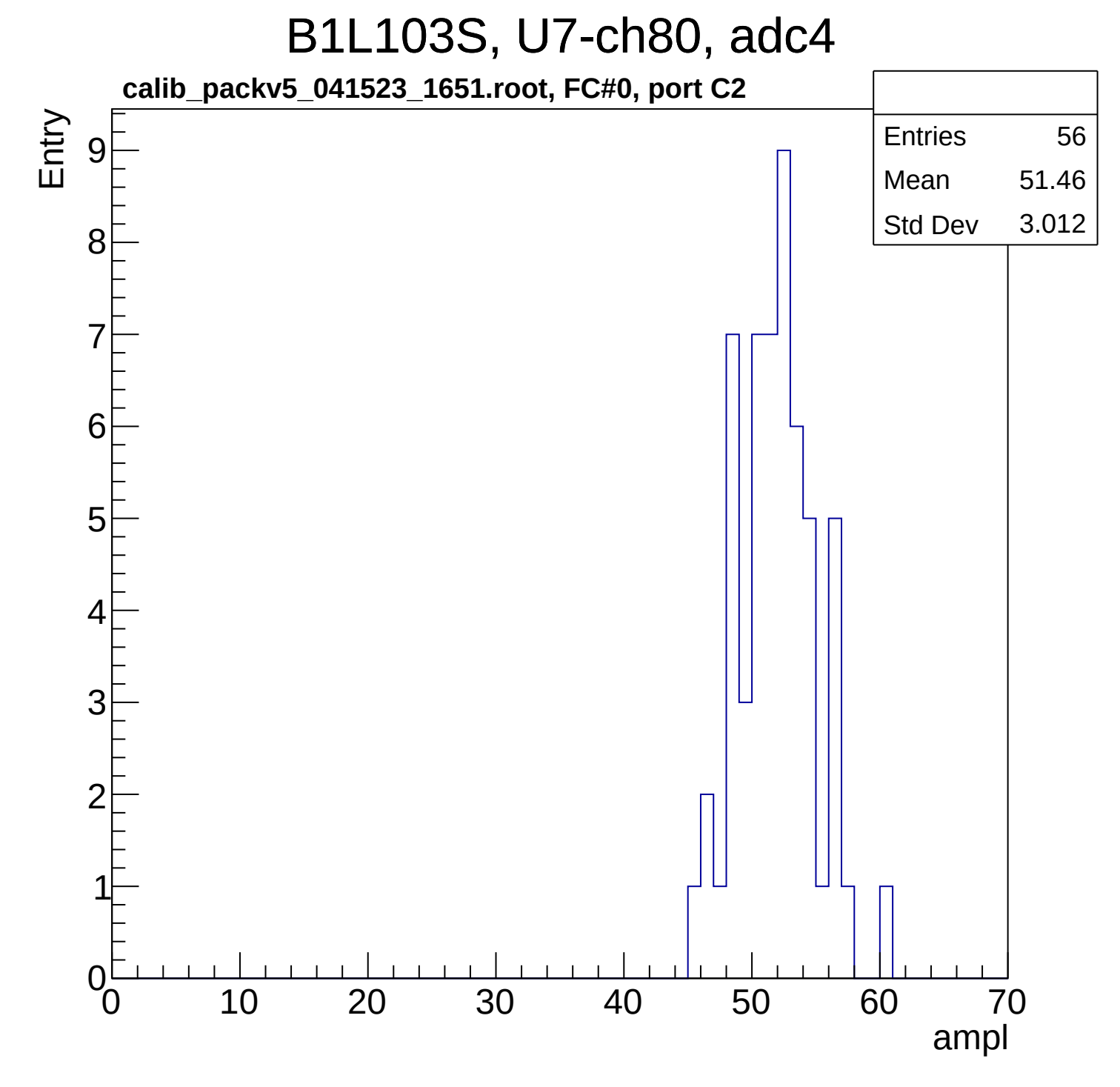
B1L103S, U7-ch80, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 51.46
Std Dev 3.012
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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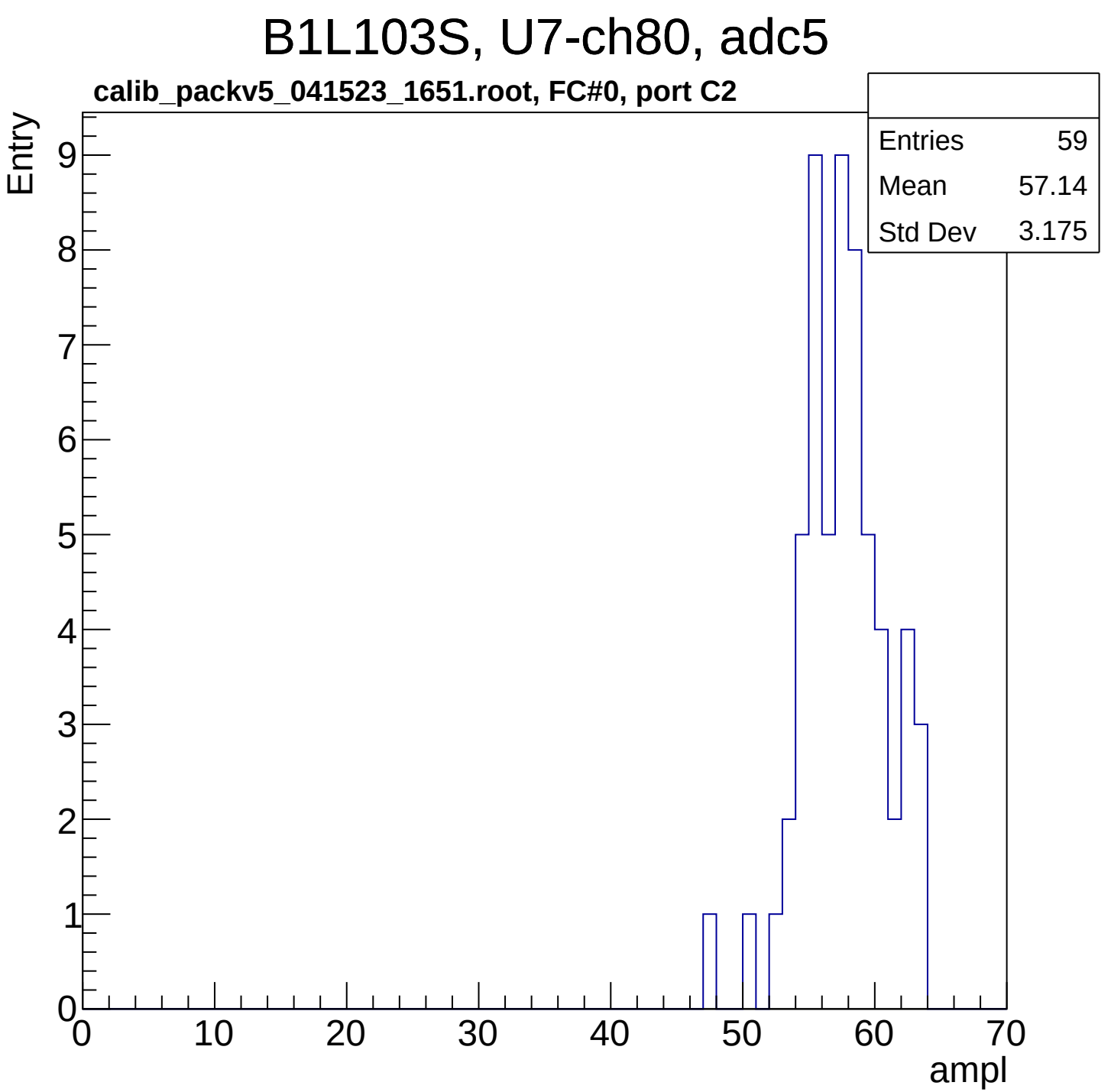
B1L103S, U7-ch80, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 57.14
Std Dev 3.175
Entry
ampl
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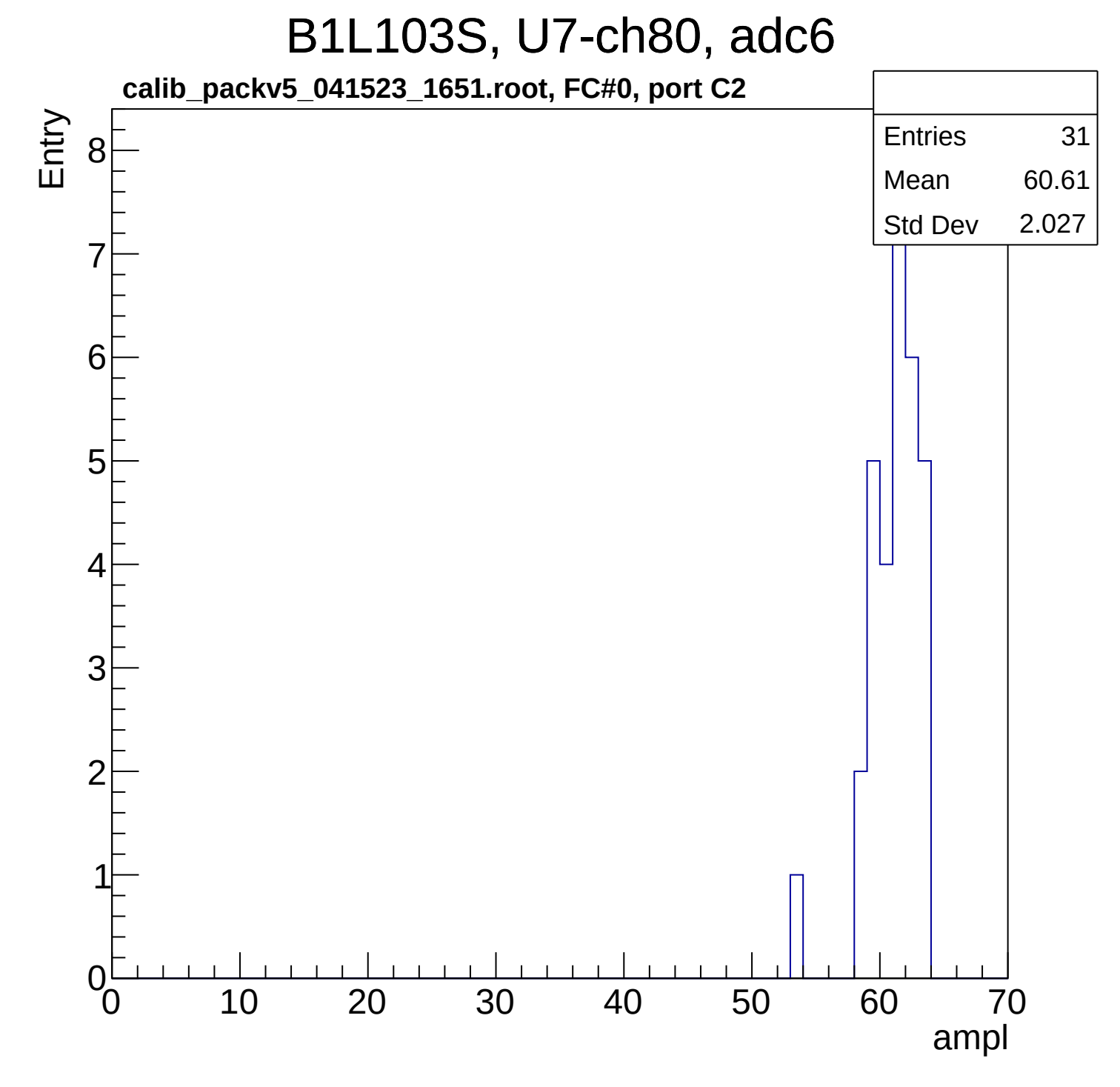
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U7-ch80, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 31
Mean 60.61
Std Dev 2.027
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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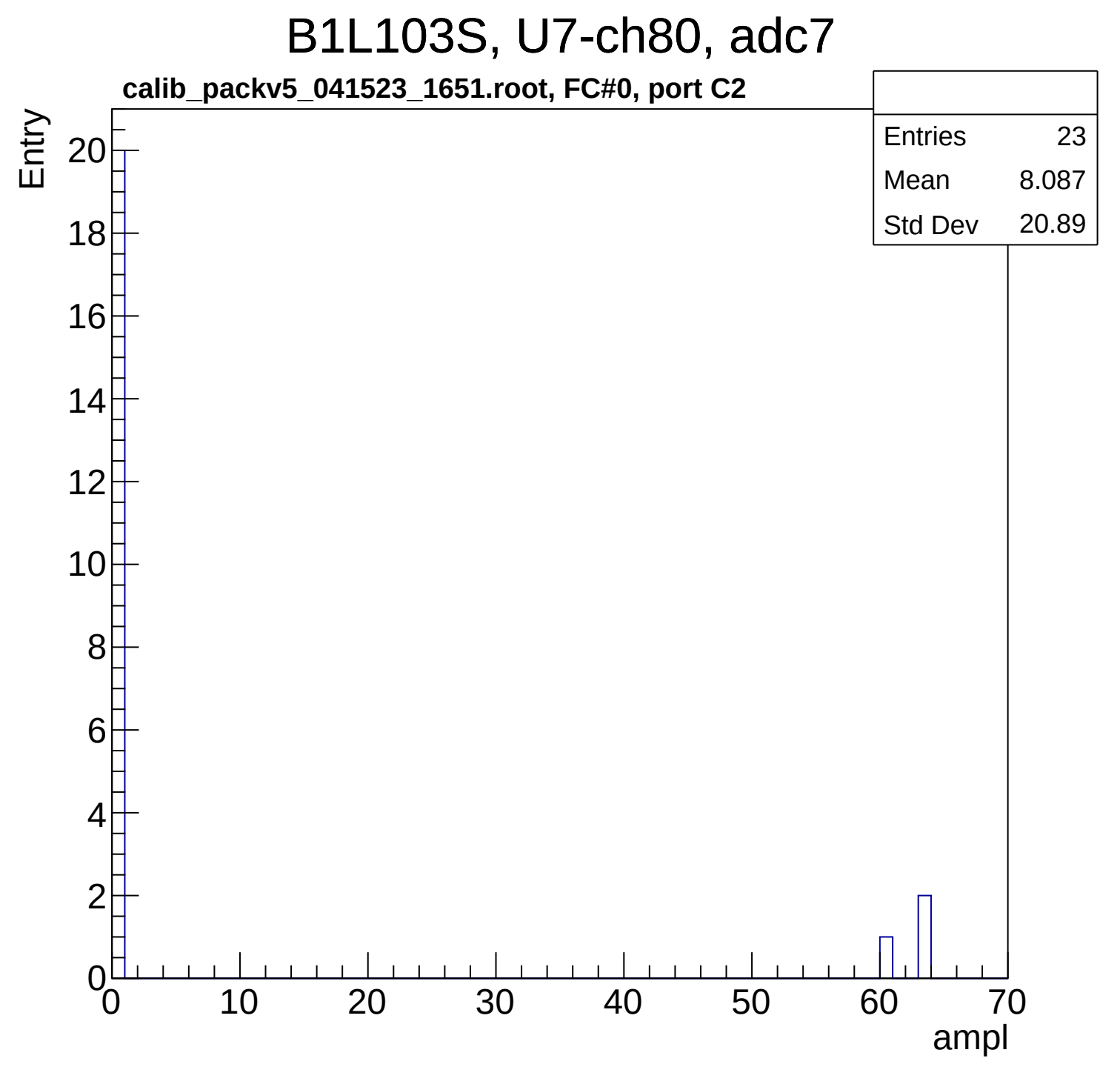
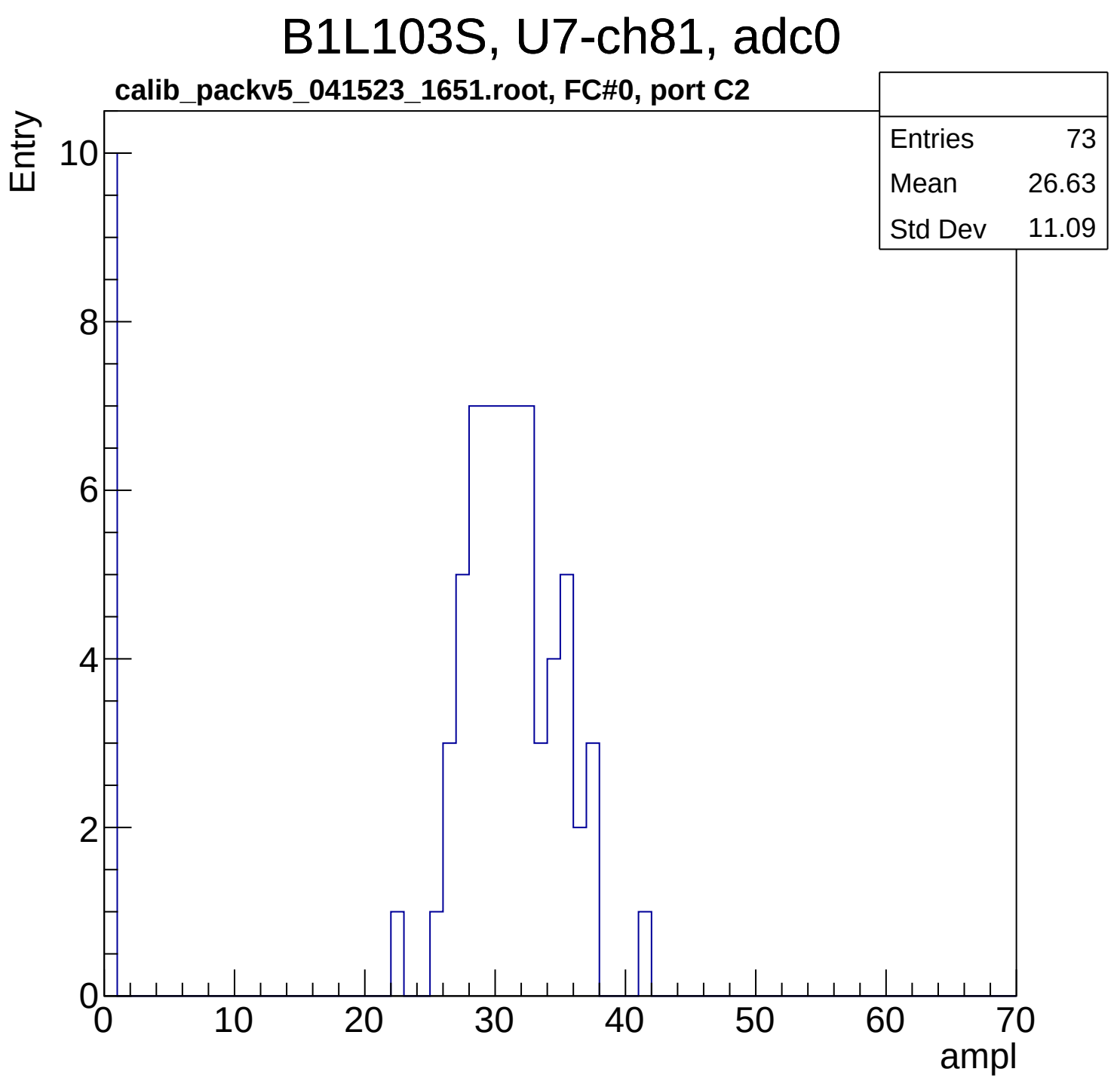
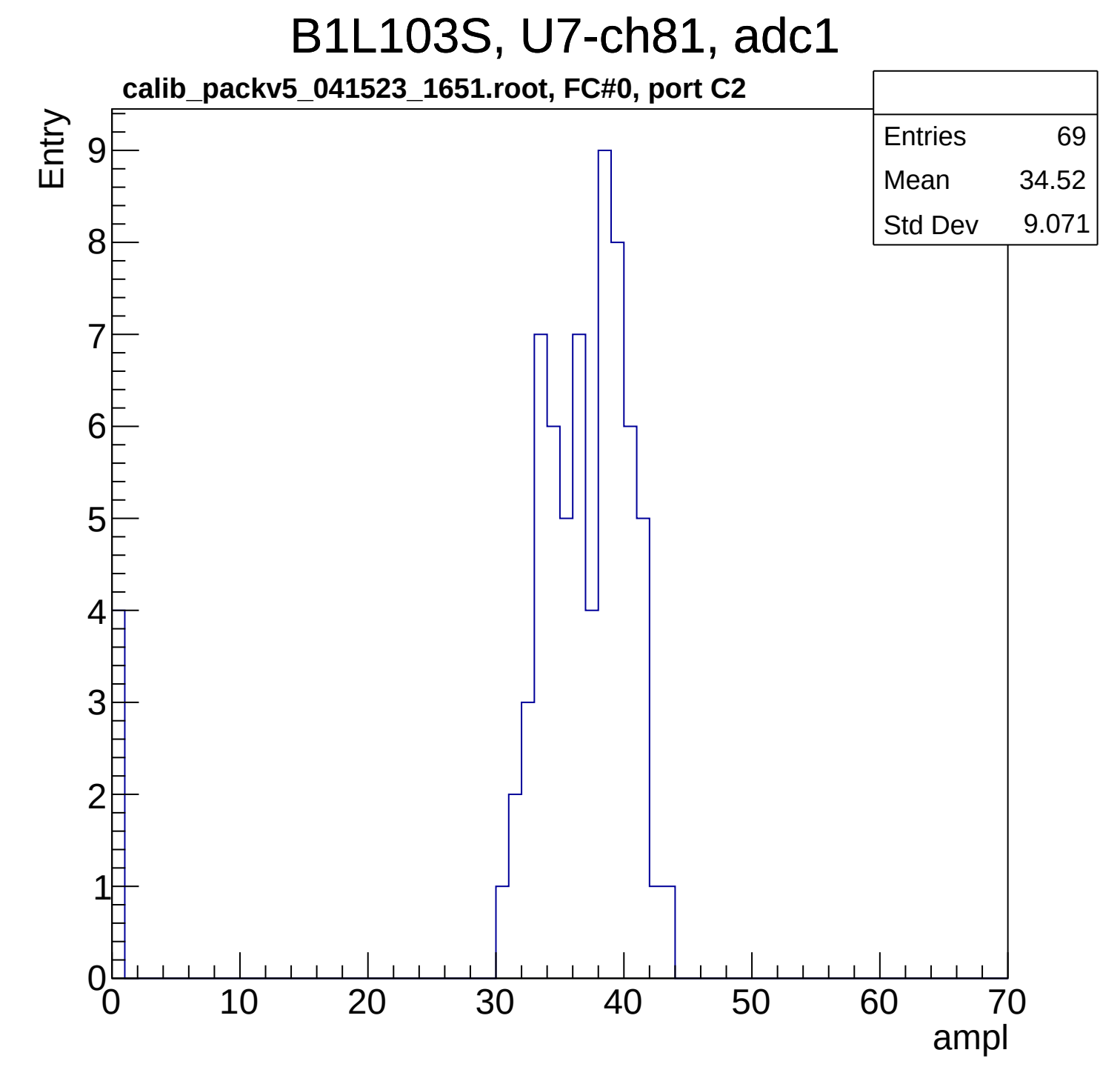

B1L103S, U7-ch80, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 23
Mean 8.087
Std Dev 20.89
Entry
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch81, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 26.63
Std Dev 11.09
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch81, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 34.52
Std Dev 9.071
Entry
ampl
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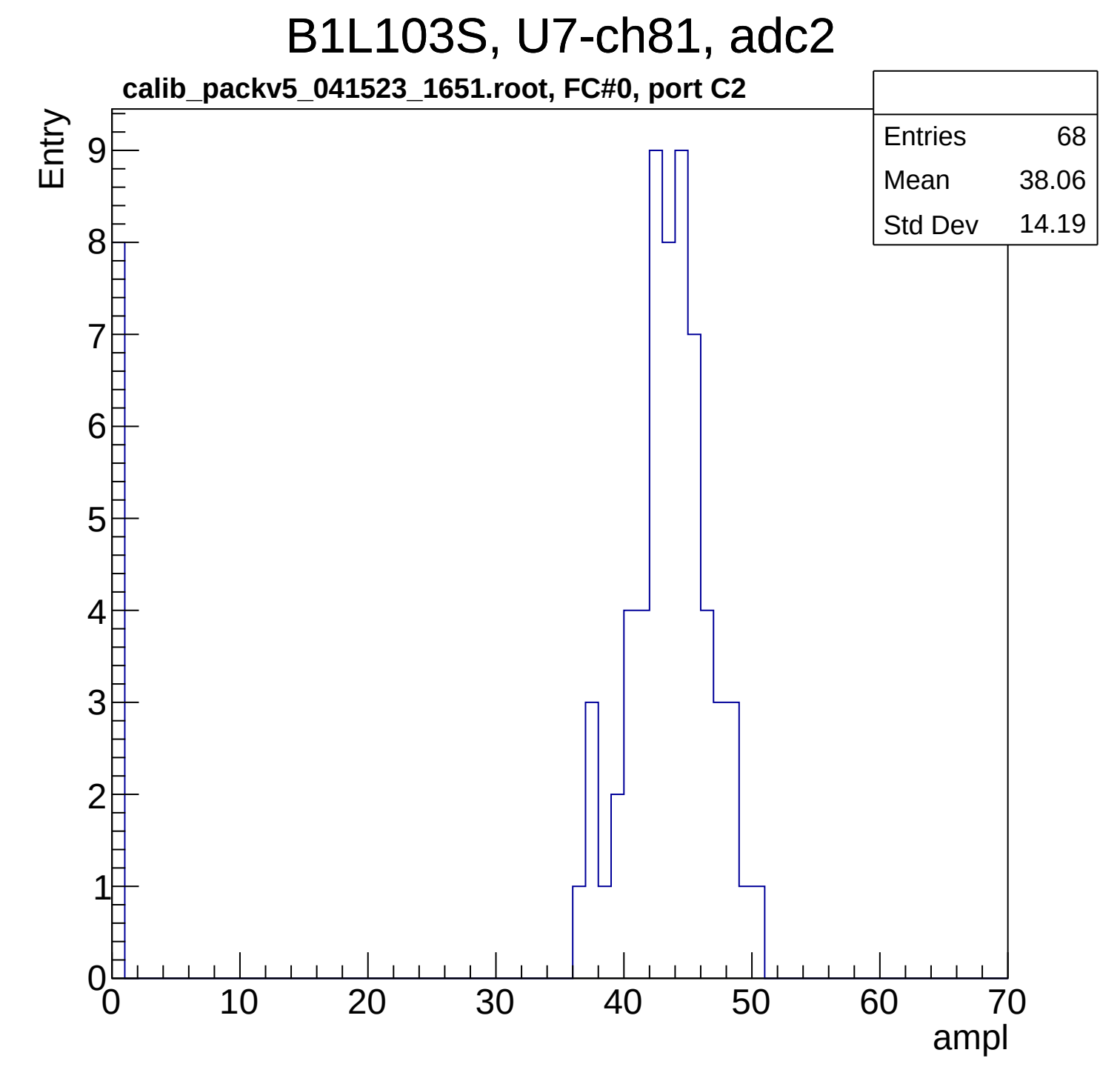
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U7-ch81, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 38.06
Std Dev 14.19
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
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40
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60
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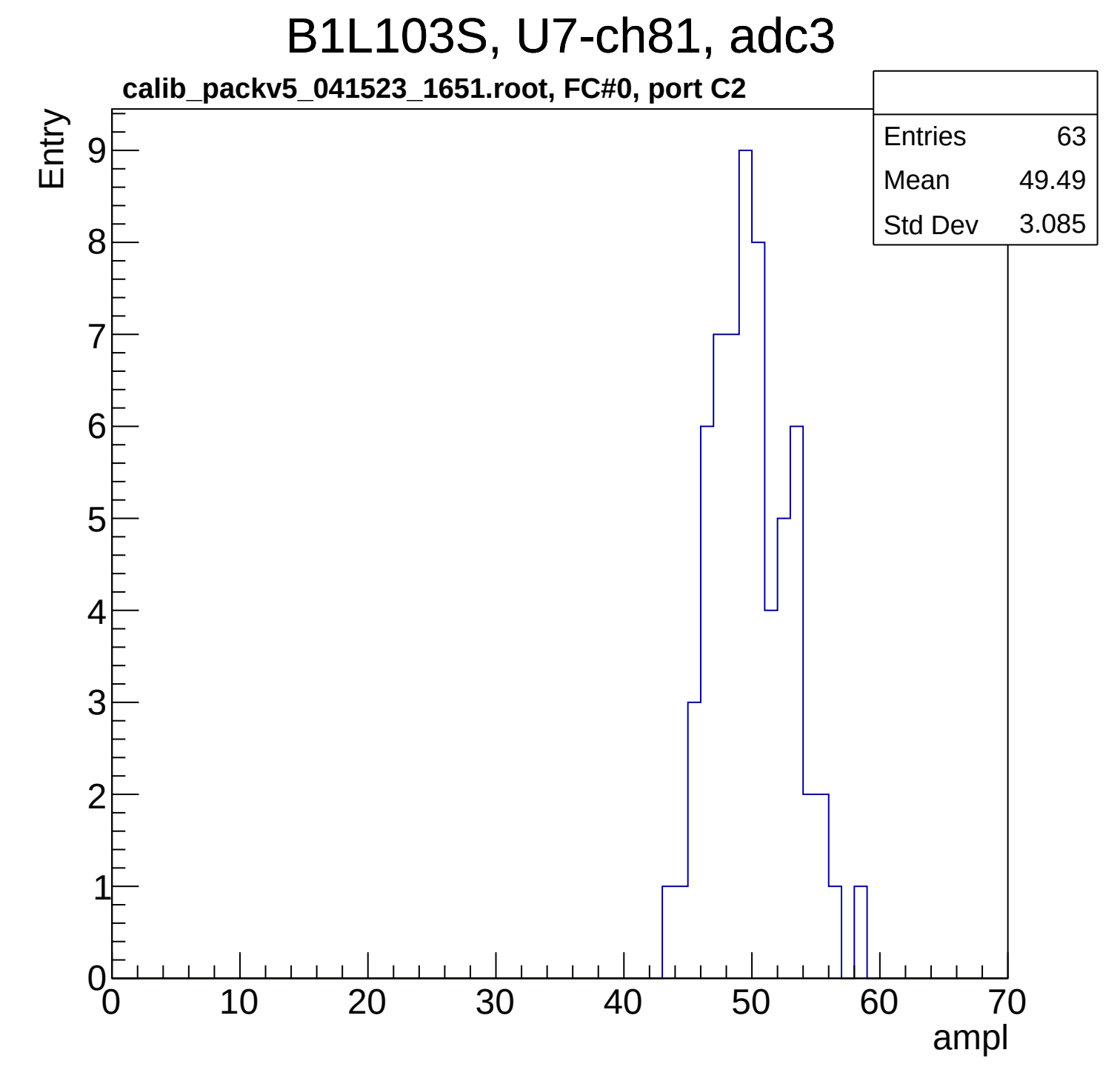
B1L103S, U7-ch81, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 49.49
Std Dev 3.085
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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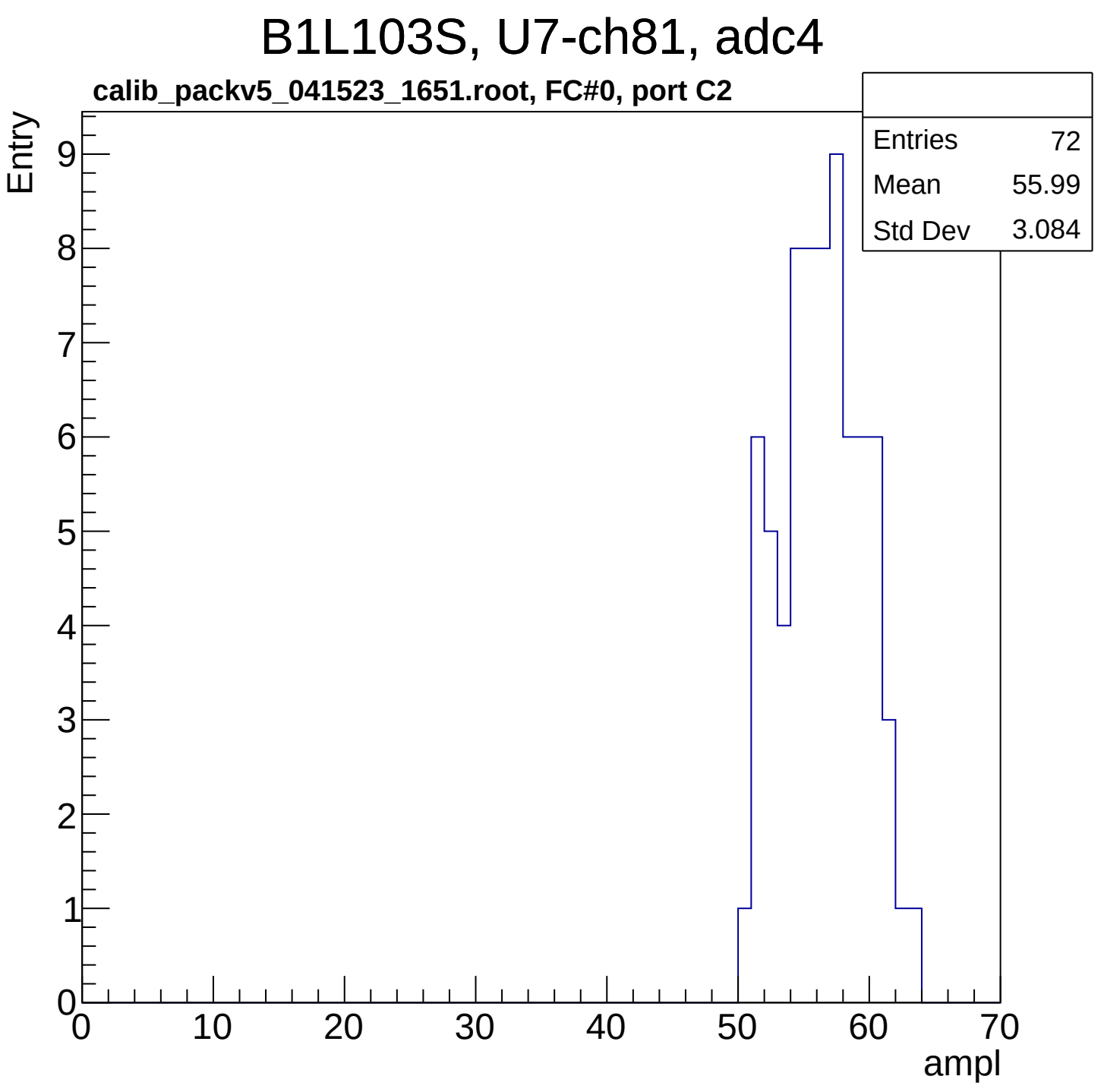
40
50
60
70


B1L103S, U7-ch81, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 55.99
Std Dev 3.084
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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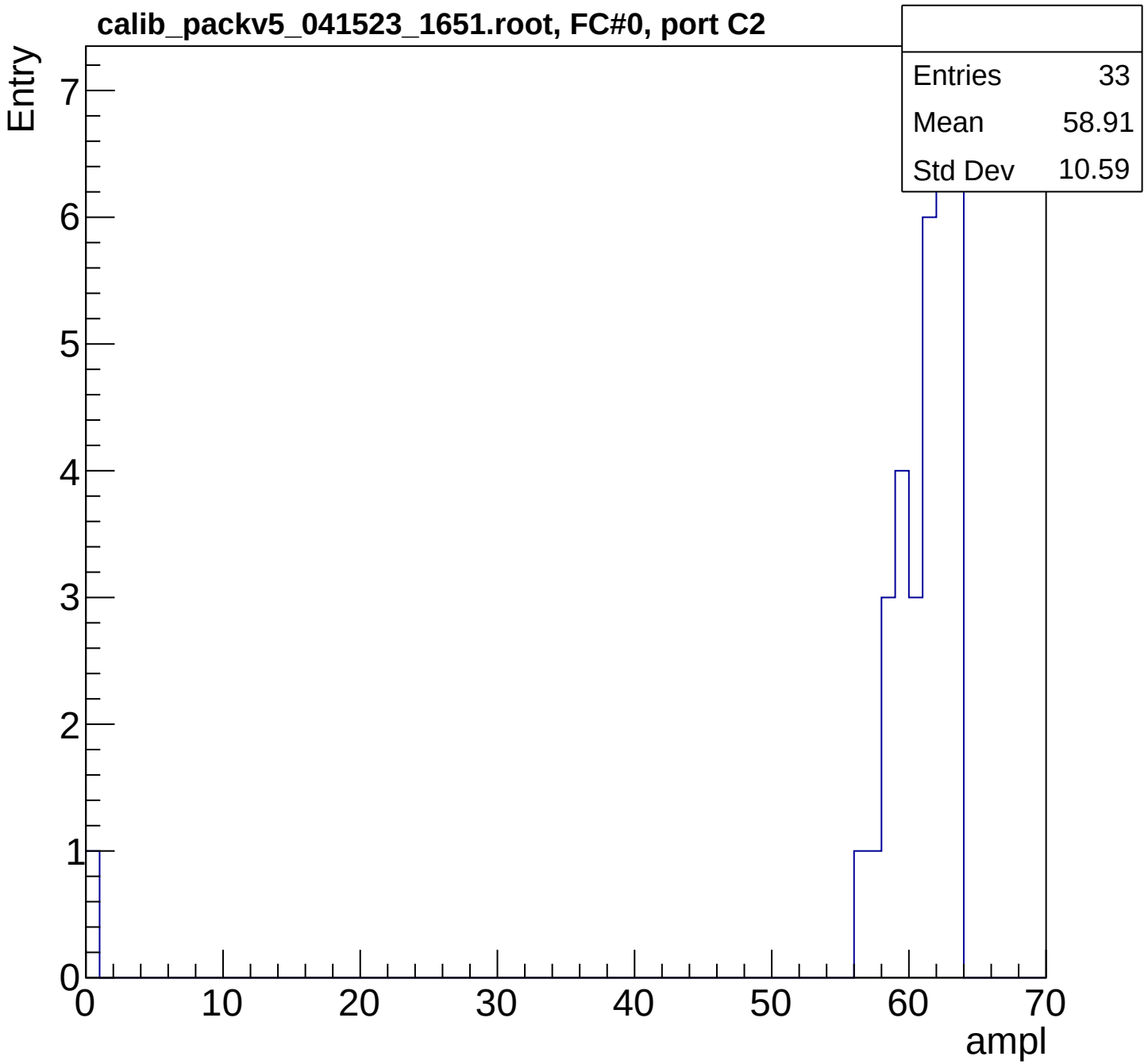
60
70


B1L103S, U7-ch81, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 33
Mean 58.91
Std Dev 10.59
Entry
ampl
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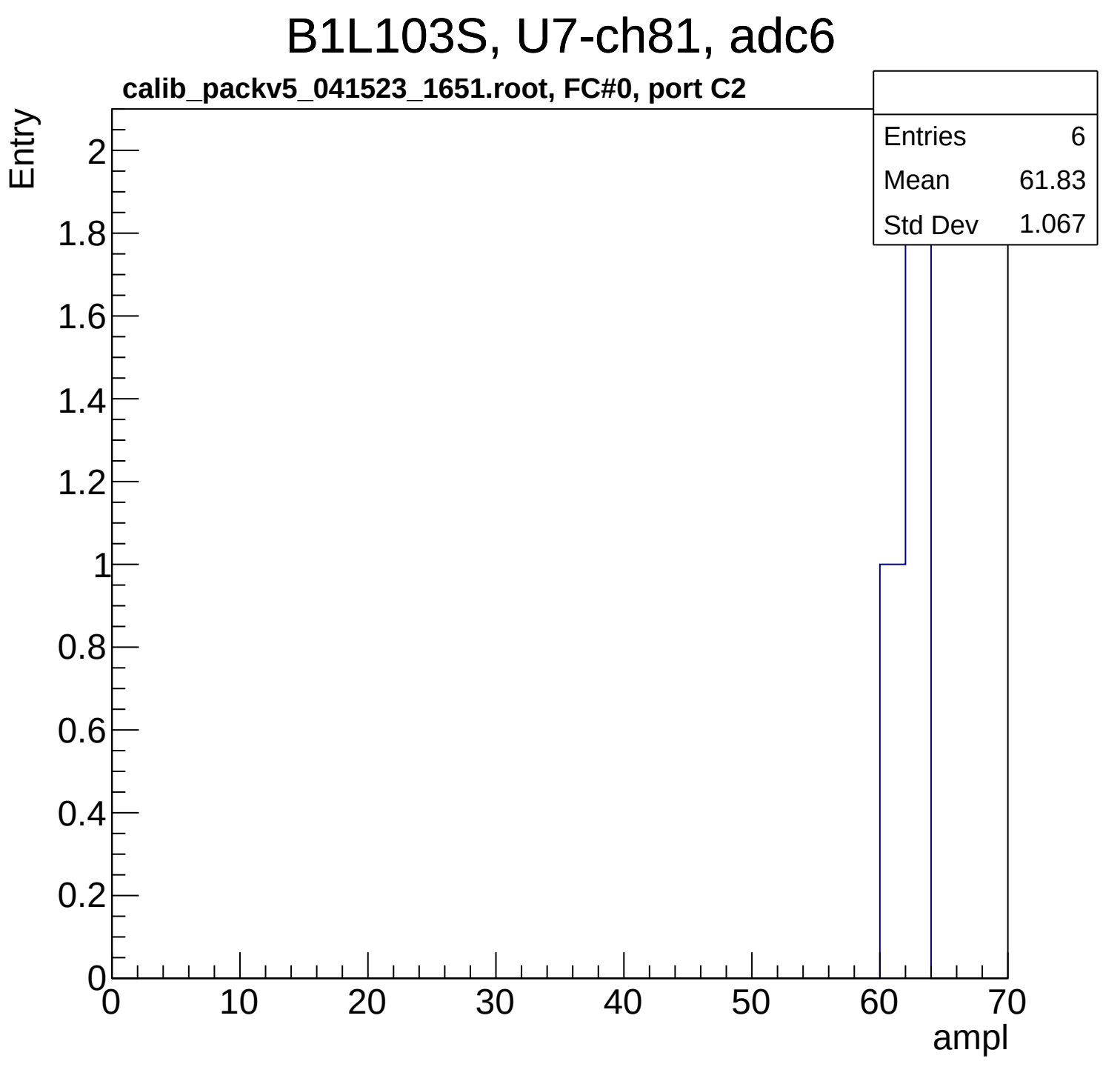
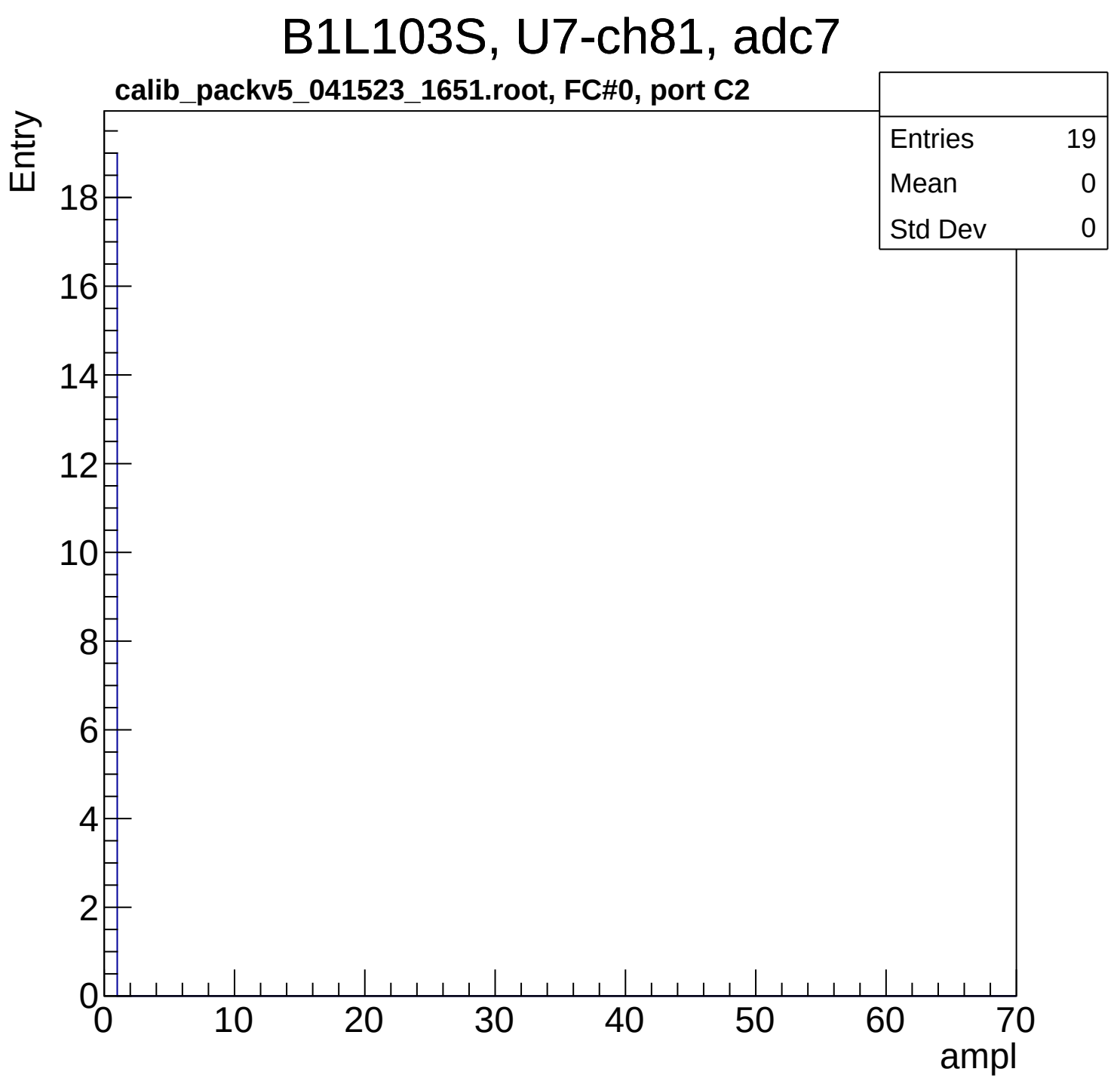
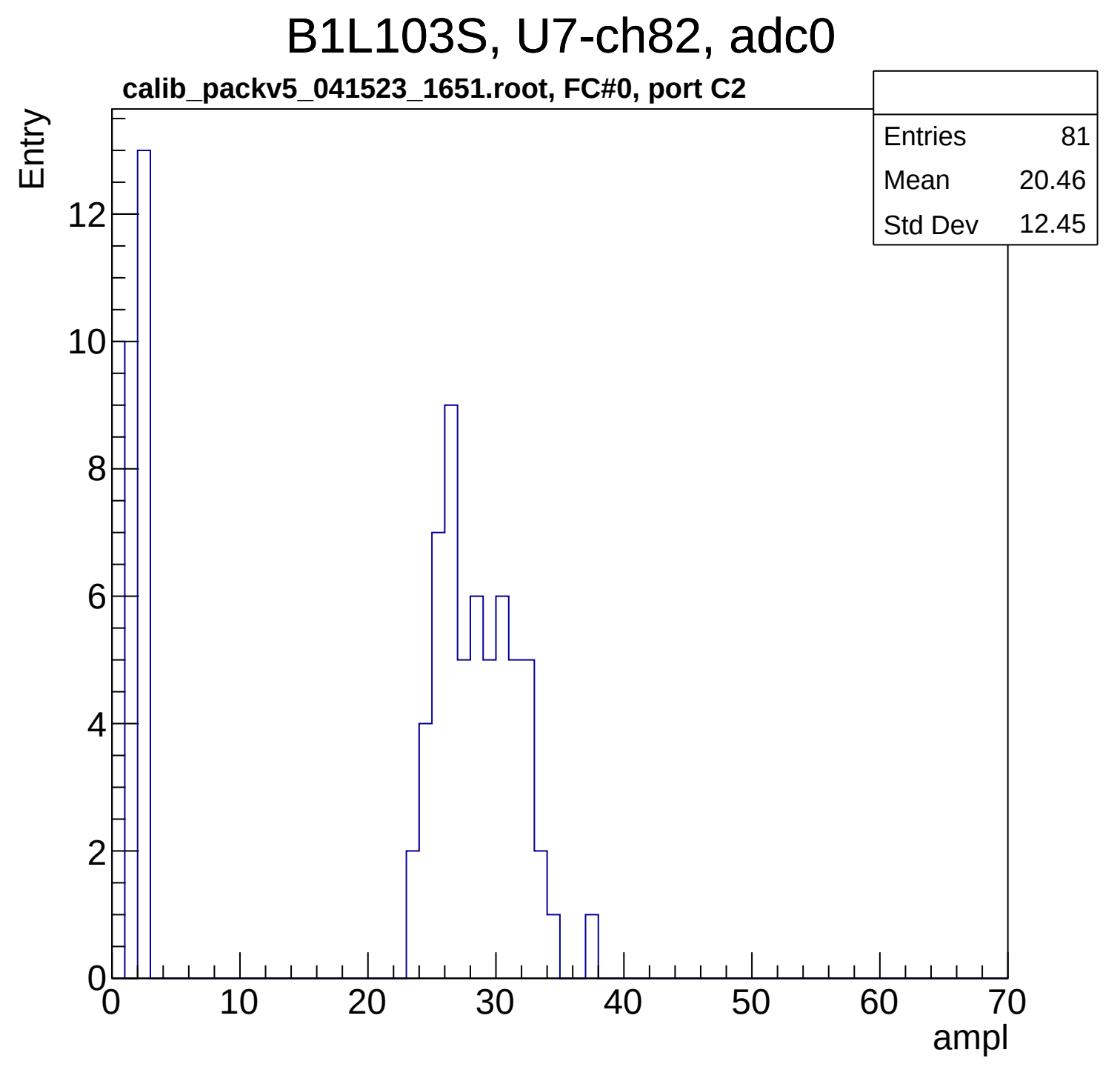
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U7-ch81, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 61.83
Std Dev 1.067
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U7-ch81, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch82, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 20.46
Std Dev 12.45
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
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60
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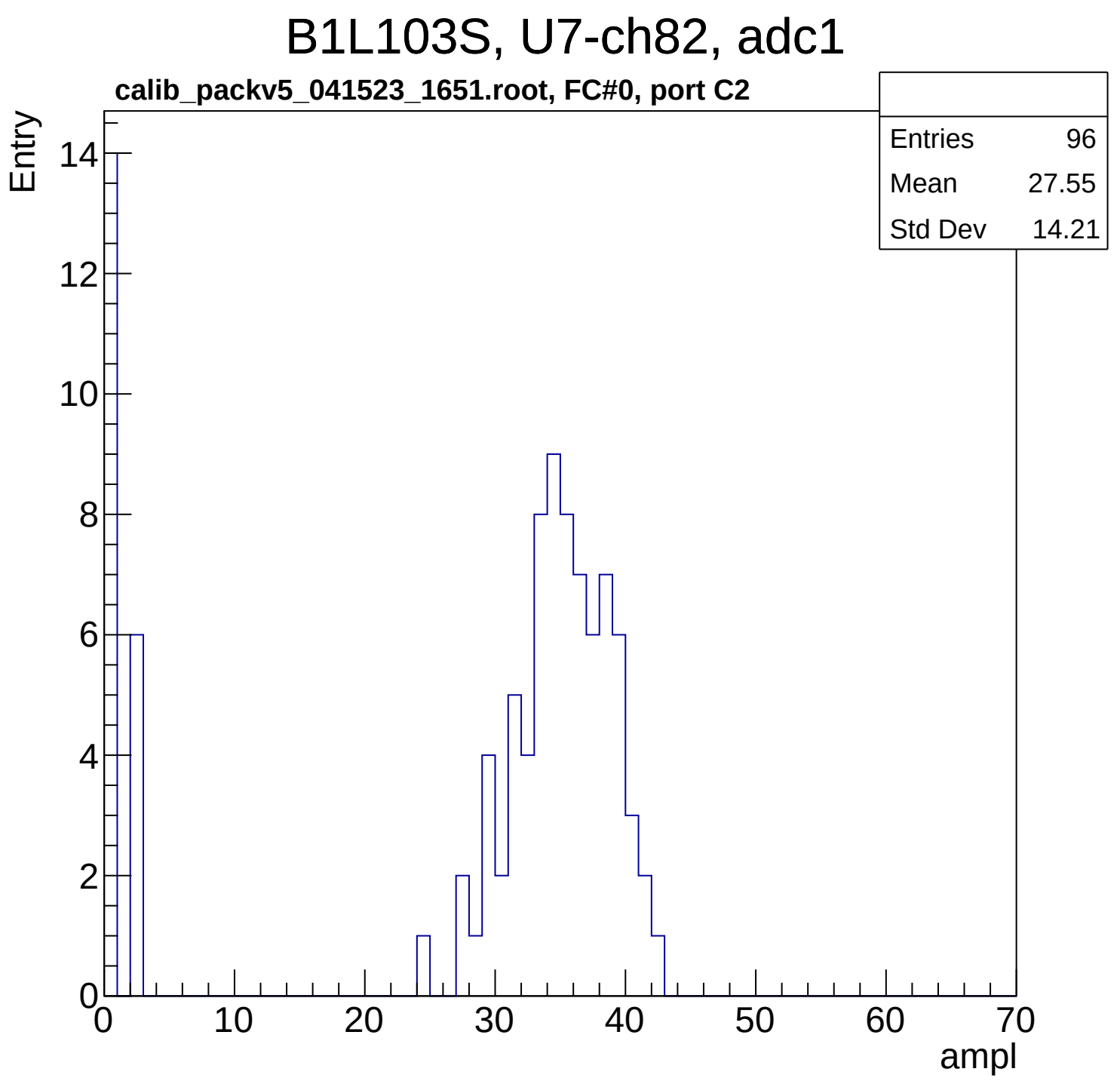
B1L103S, U7-ch82, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 96
Mean 27.55
Std Dev 14.21
Entry
ampl
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2
4
6
8
10
12
14
0
10
20
30
40
50
60
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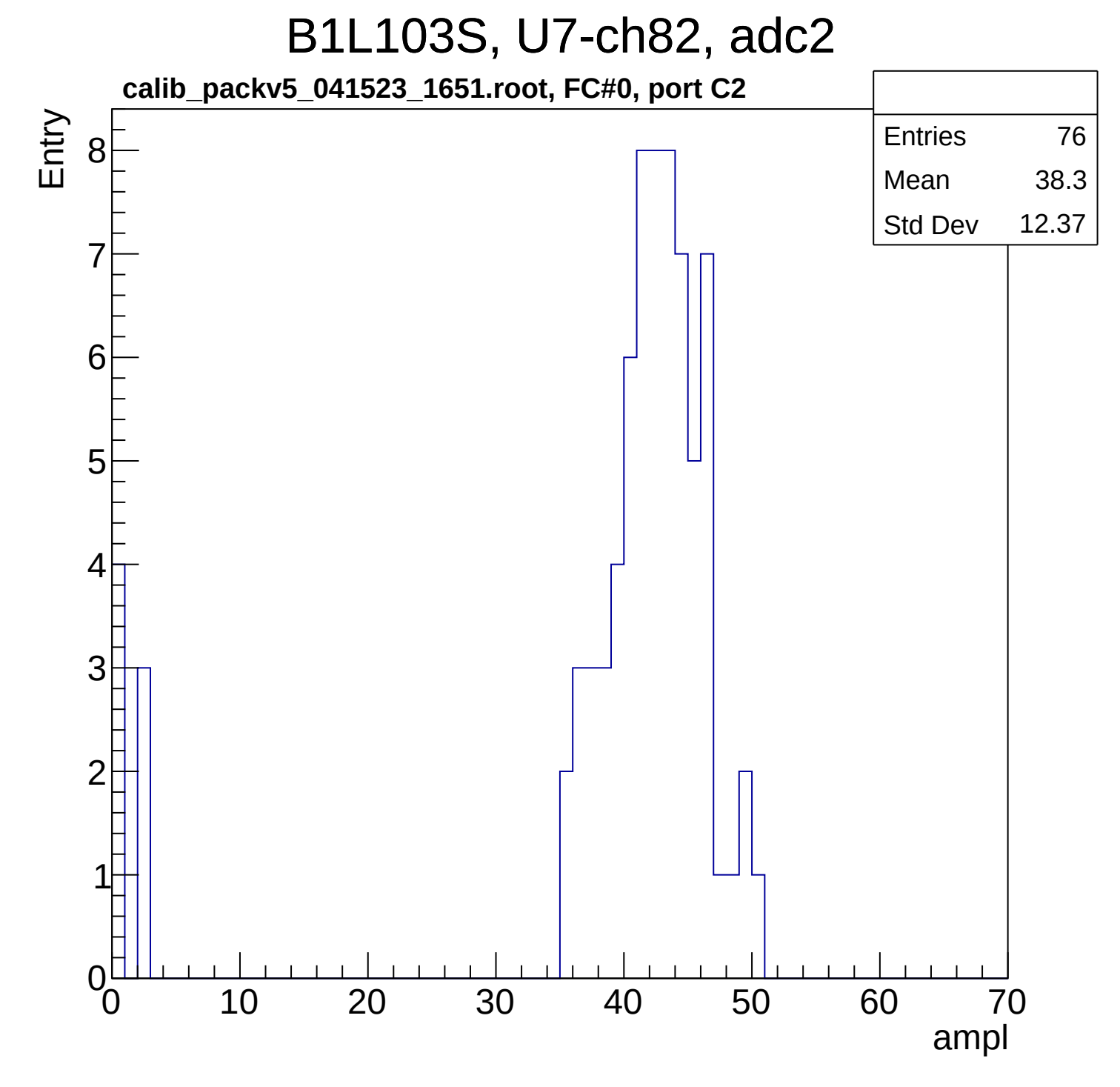
B1L103S, U7-ch82, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 38.3
Std Dev 12.37
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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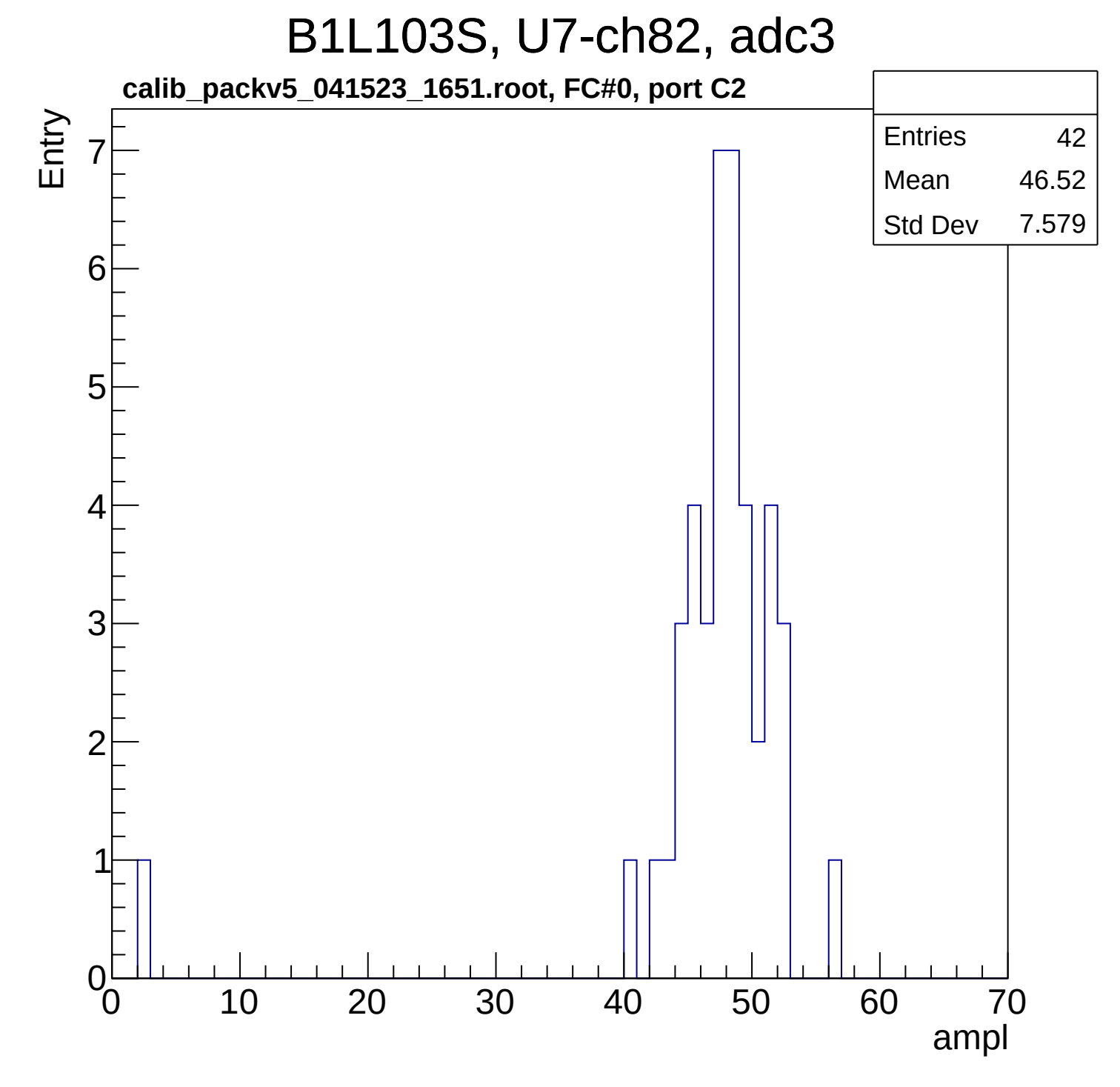
B1L103S, U7-ch82, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 42
Mean 46.52
Std Dev 7.579
Entry
ampl
0
1
2
3
4
5
6
7
0
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20
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40
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60
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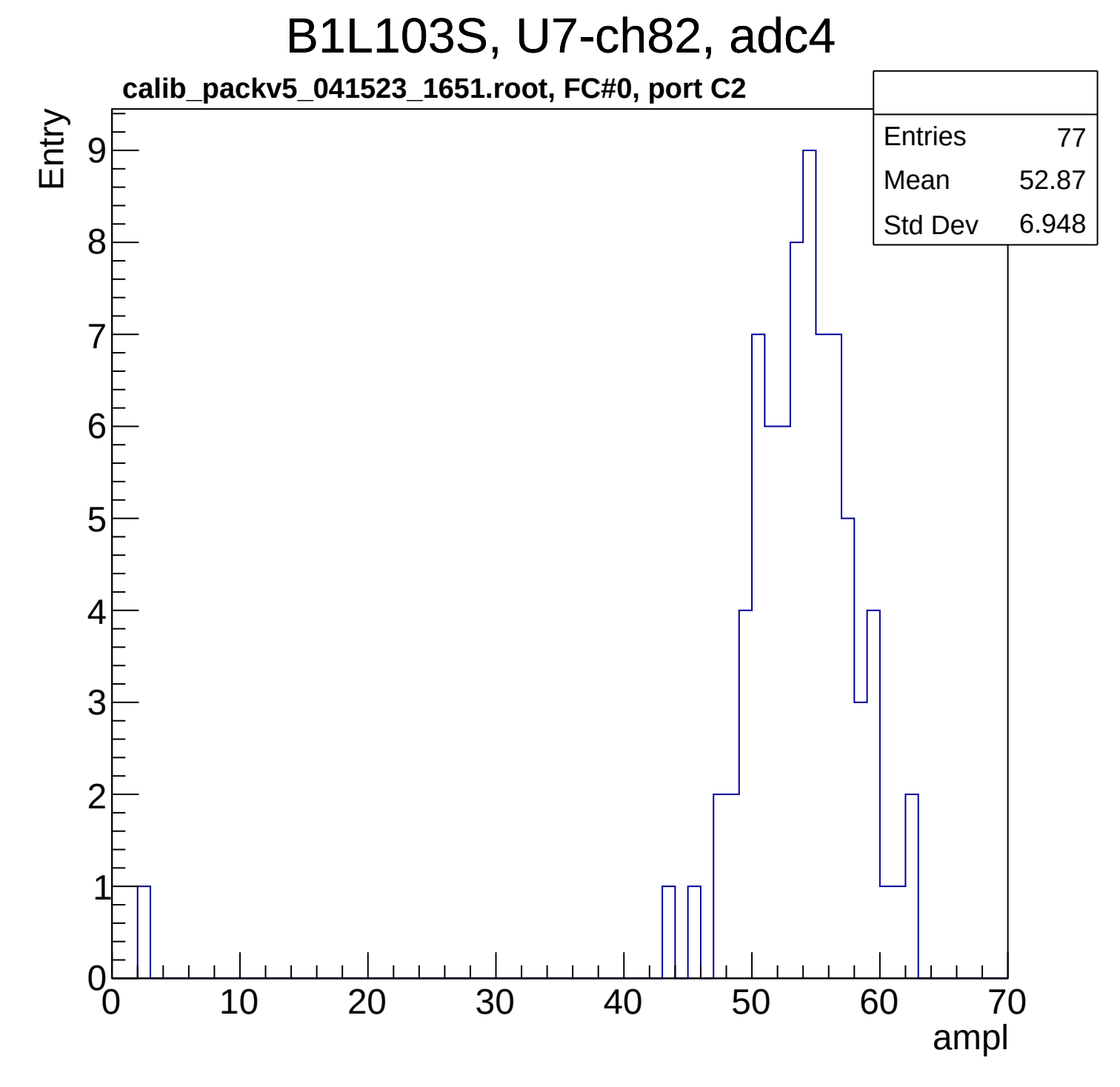
B1L103S, U7-ch82, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 52.87
Std Dev 6.948
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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60
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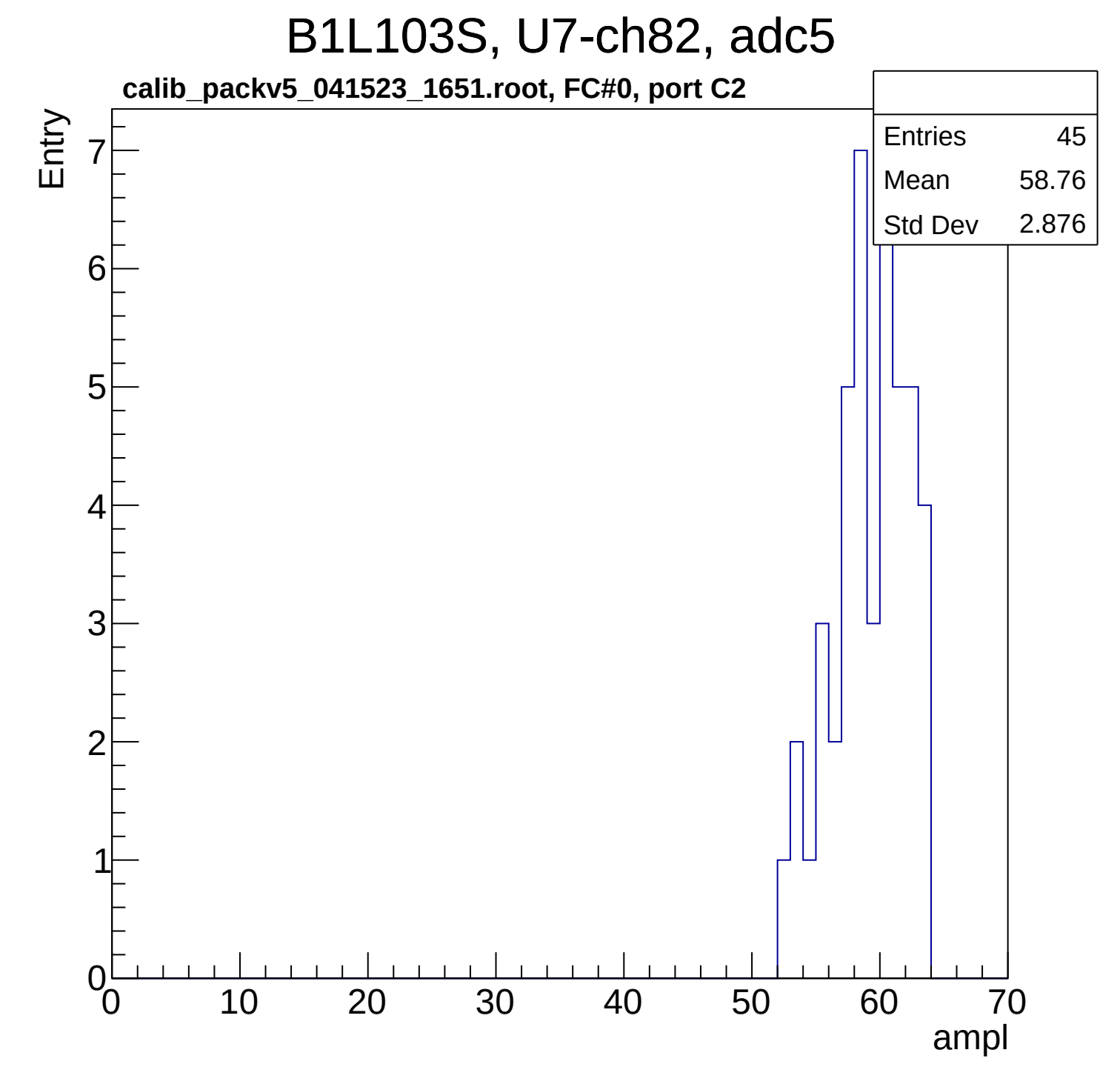
B1L103S, U7-ch82, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 58.76
Std Dev 2.876
Entry
ampl
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1
2
3
4
5
6
7
0
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20
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40
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60
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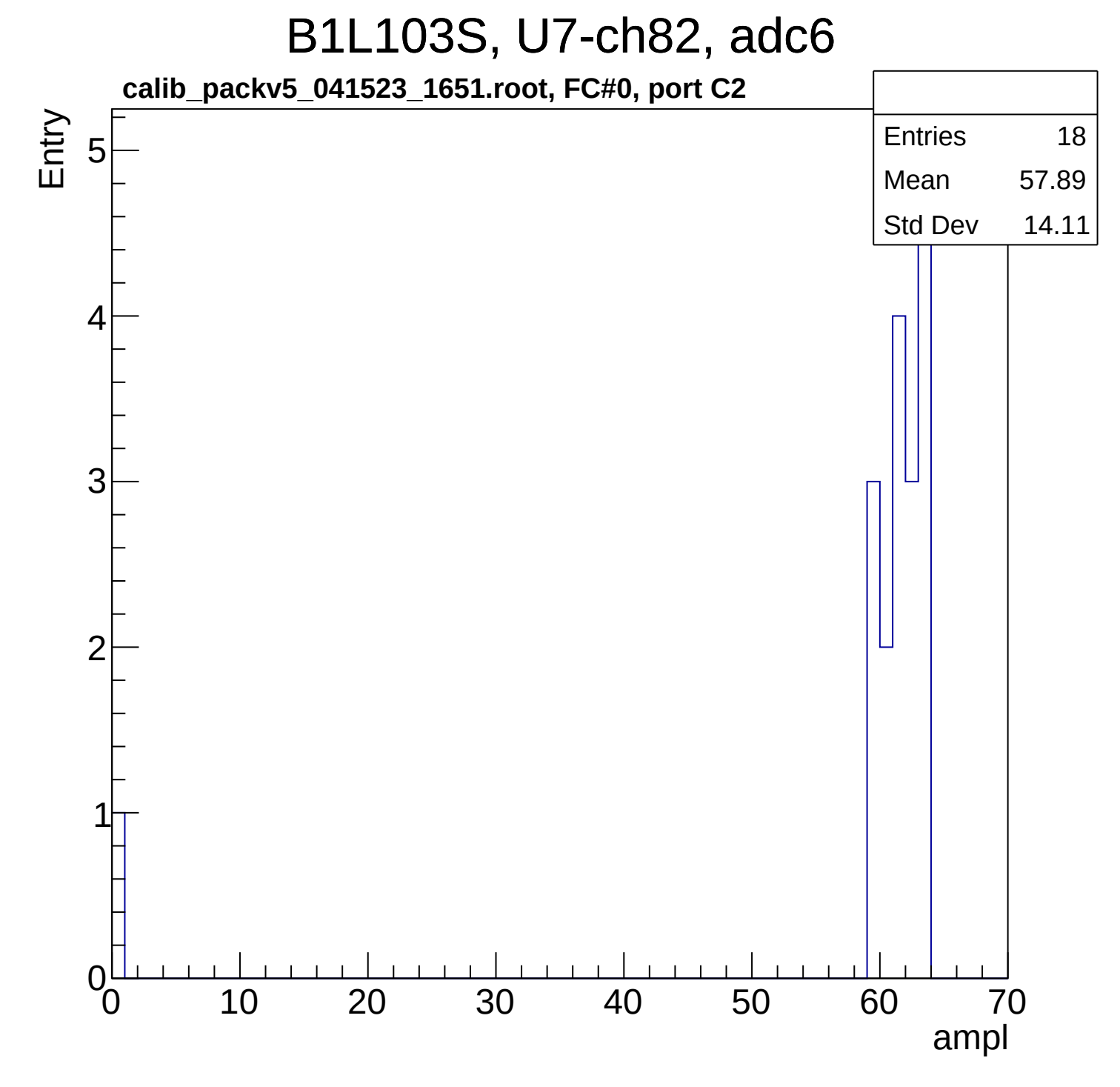
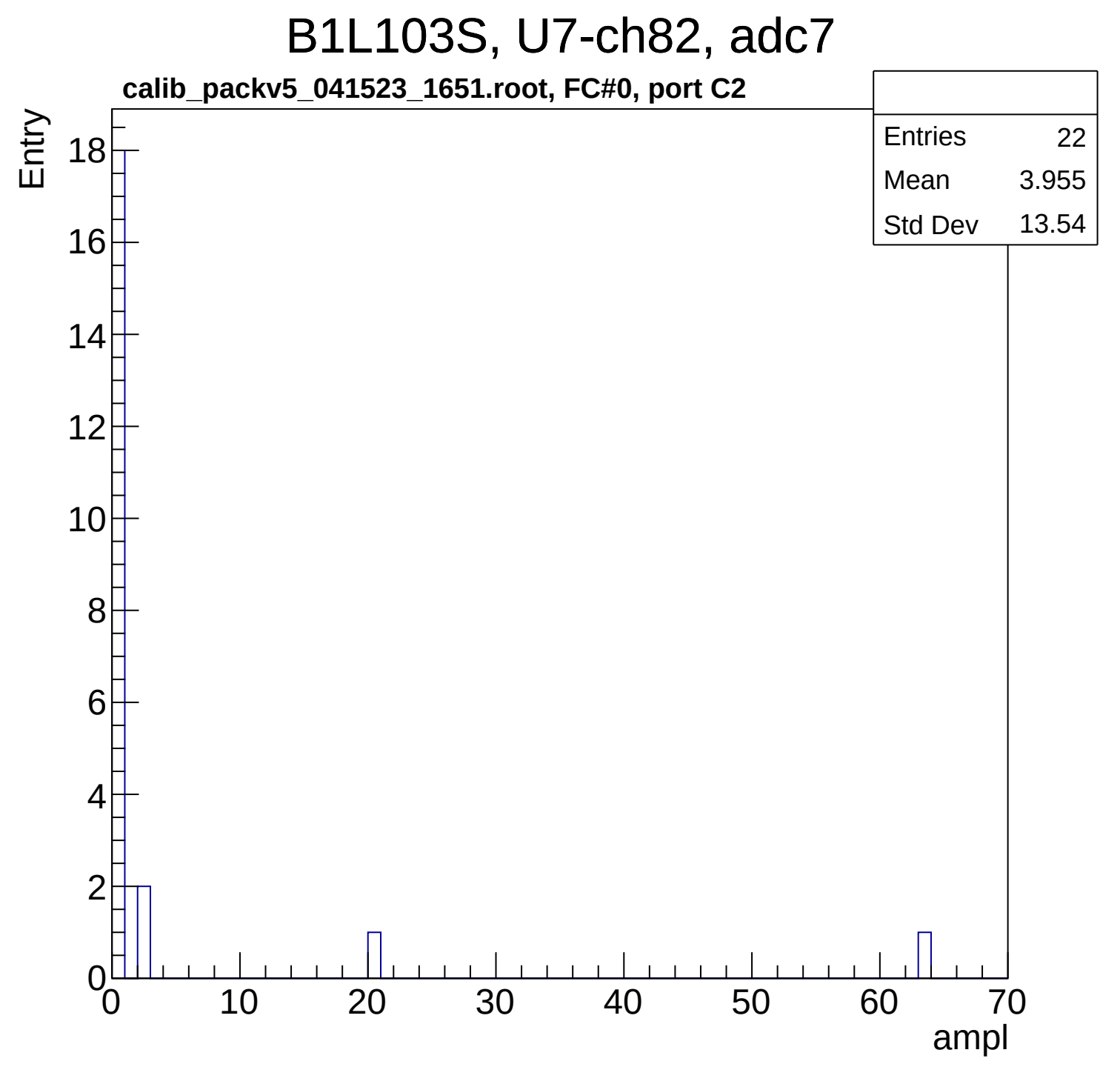

B1L103S, U7-ch82, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 57.89
Std Dev 14.11
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U7-ch82, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 3.955
Std Dev 13.54
Entry
ampl
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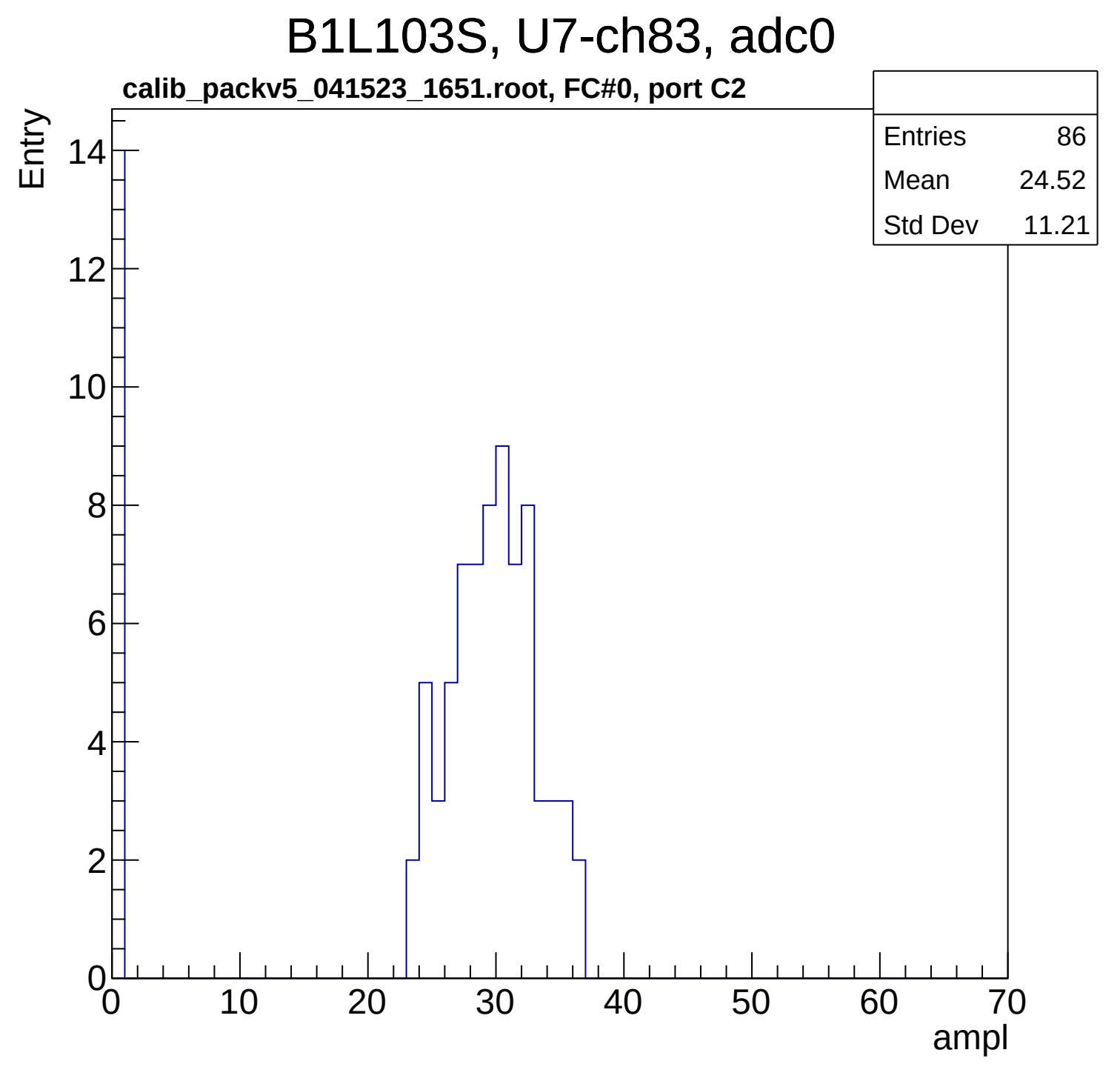
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70


B1L103S, U7-ch83, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 24.52
Std Dev 11.21
Entry
ampl
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2
4
6
8
10
12
14
0
10
20
30
40
50
60
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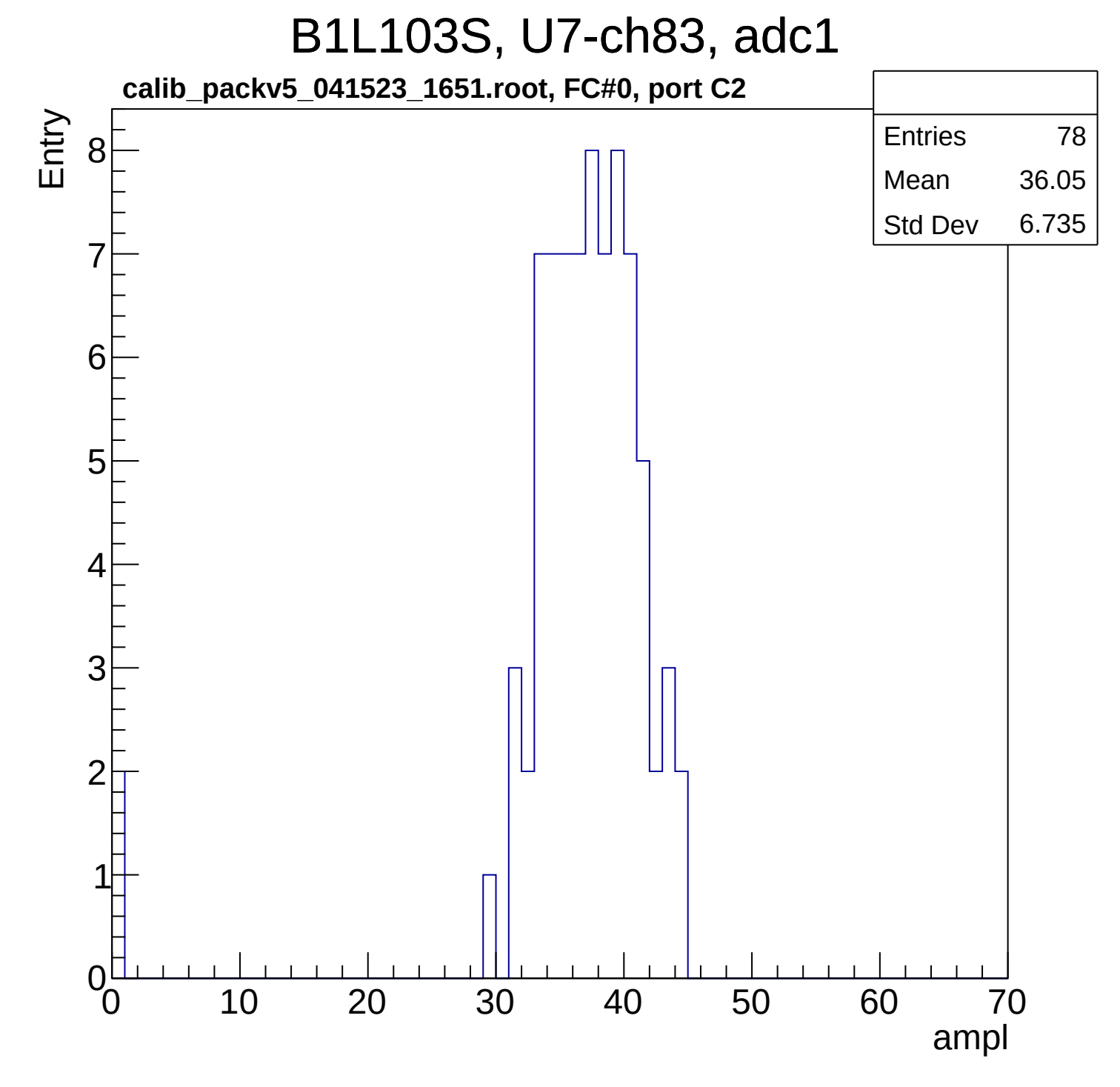
B1L103S, U7-ch83, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 36.05
Std Dev 6.735
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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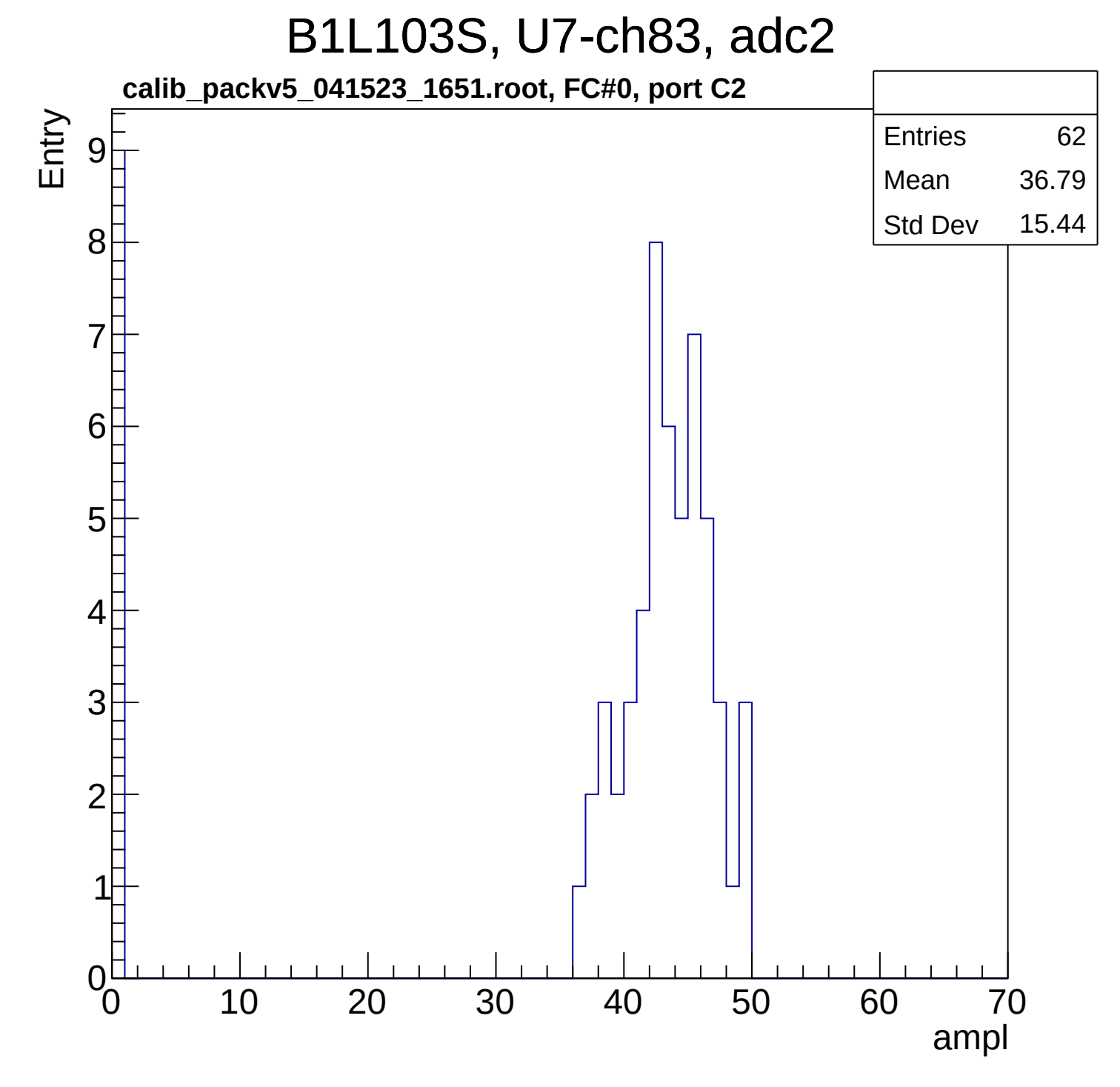
B1L103S, U7-ch83, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 36.79
Std Dev 15.44
Entry
ampl
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2
3
4
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6
7
8
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0
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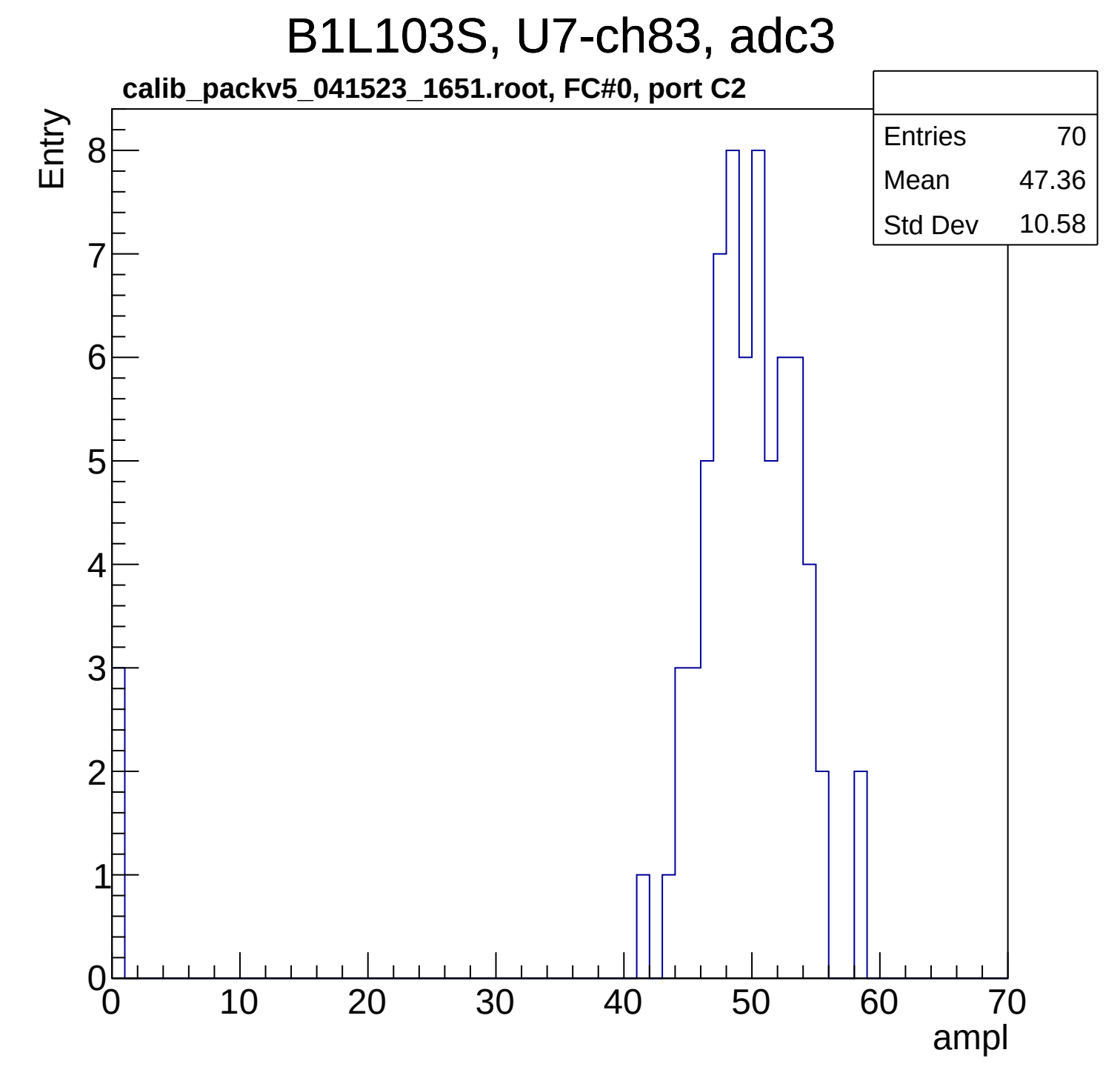
B1L103S, U7-ch83, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 47.36
Std Dev 10.58
Entry
ampl
0
1
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3
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5
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0
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60
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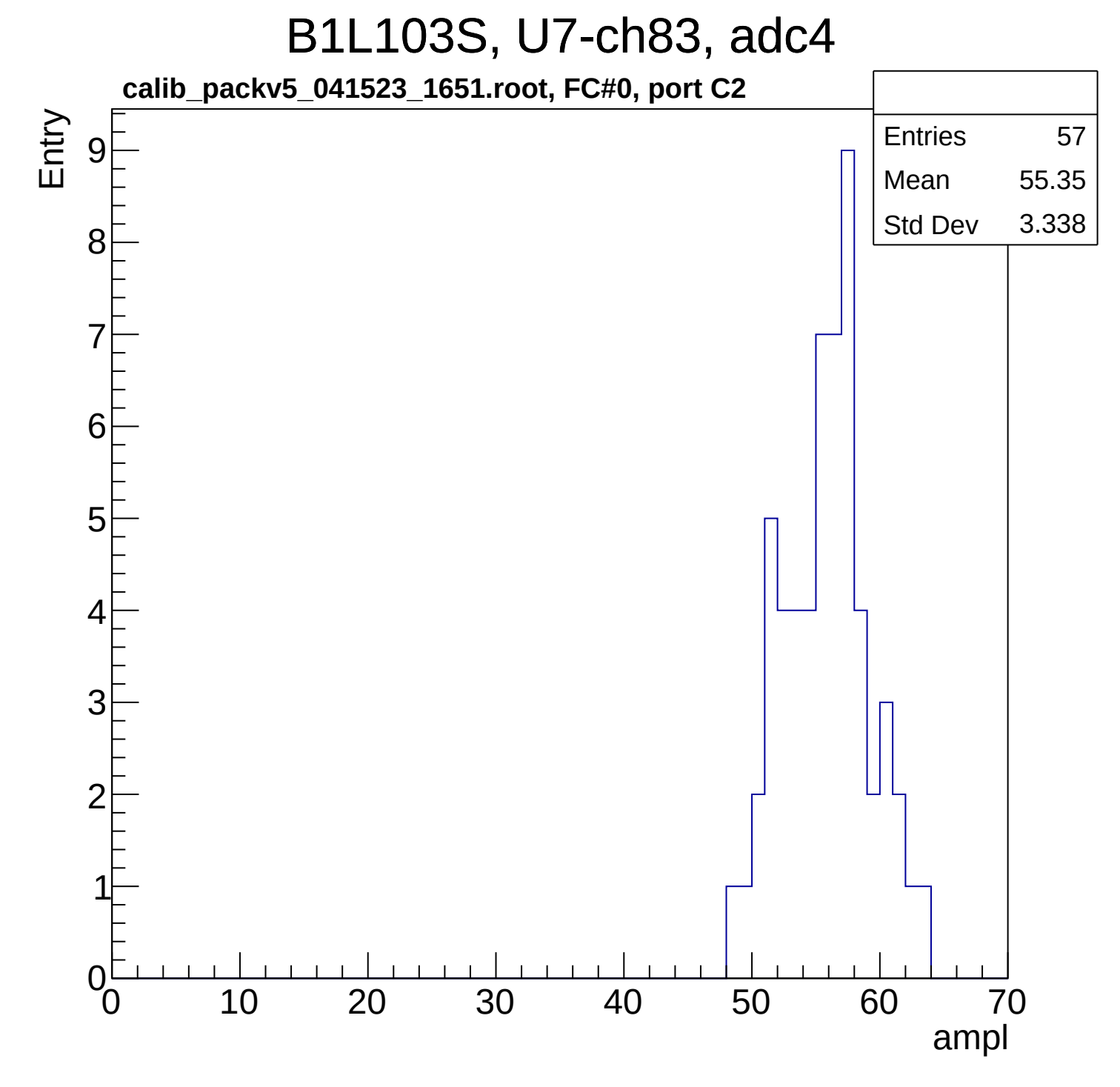
B1L103S, U7-ch83, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 55.35
Std Dev 3.338
Entry
ampl
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4
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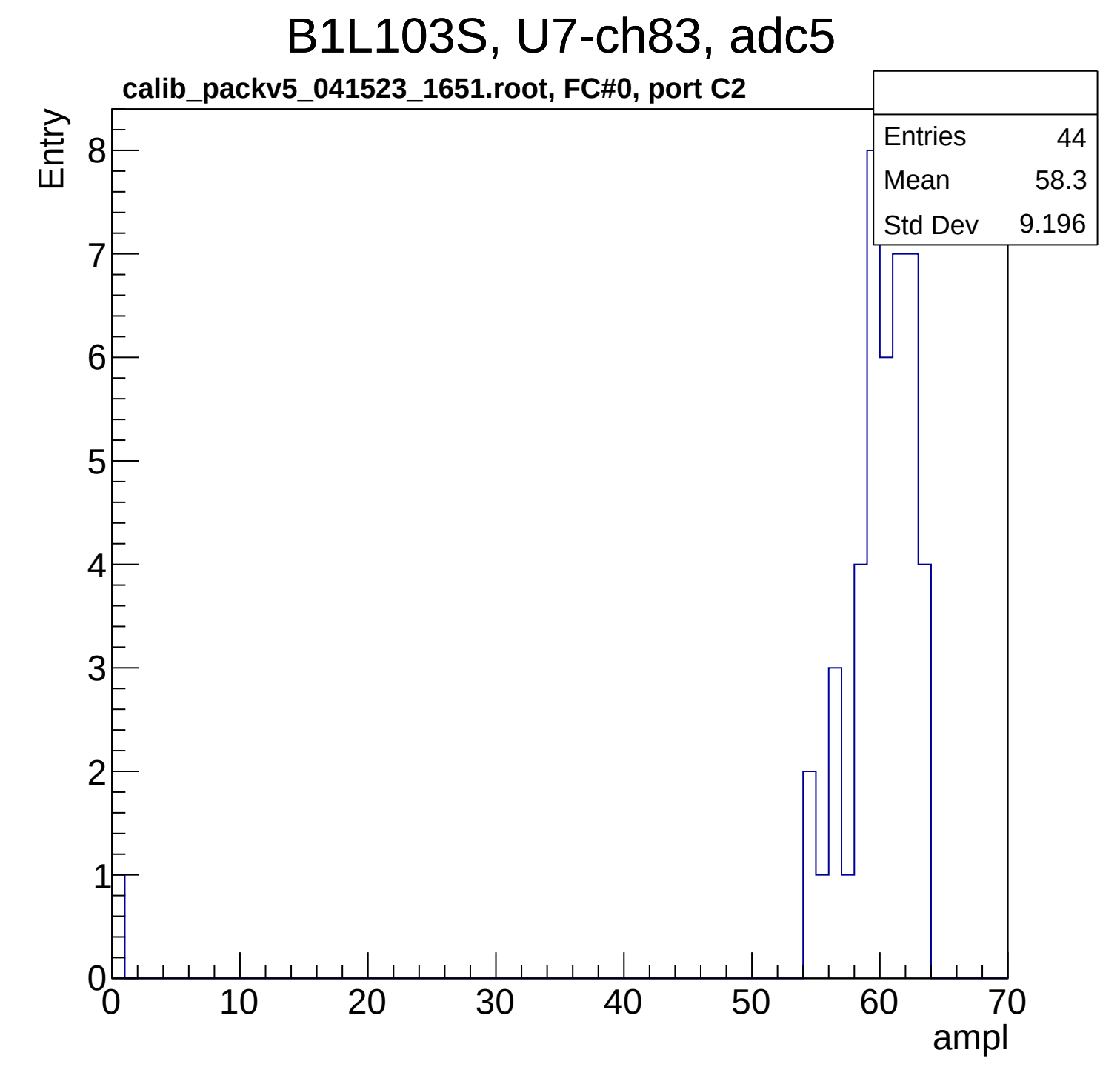
B1L103S, U7-ch83, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 58.3
Std Dev 9.196
Entry
ampl
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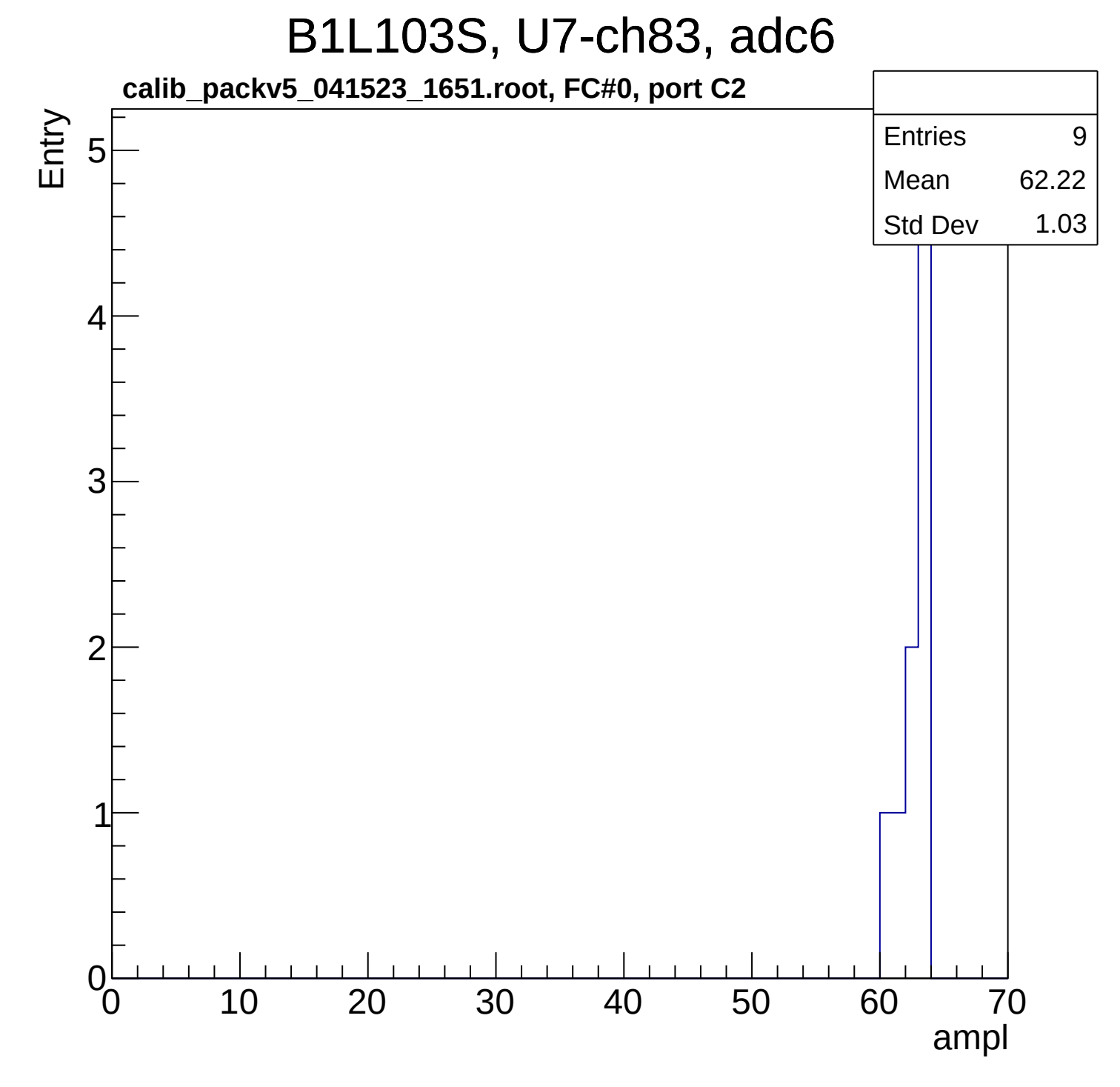
B1L103S, U7-ch83, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 9
Mean 62.22
Std Dev 1.03
Entry
0
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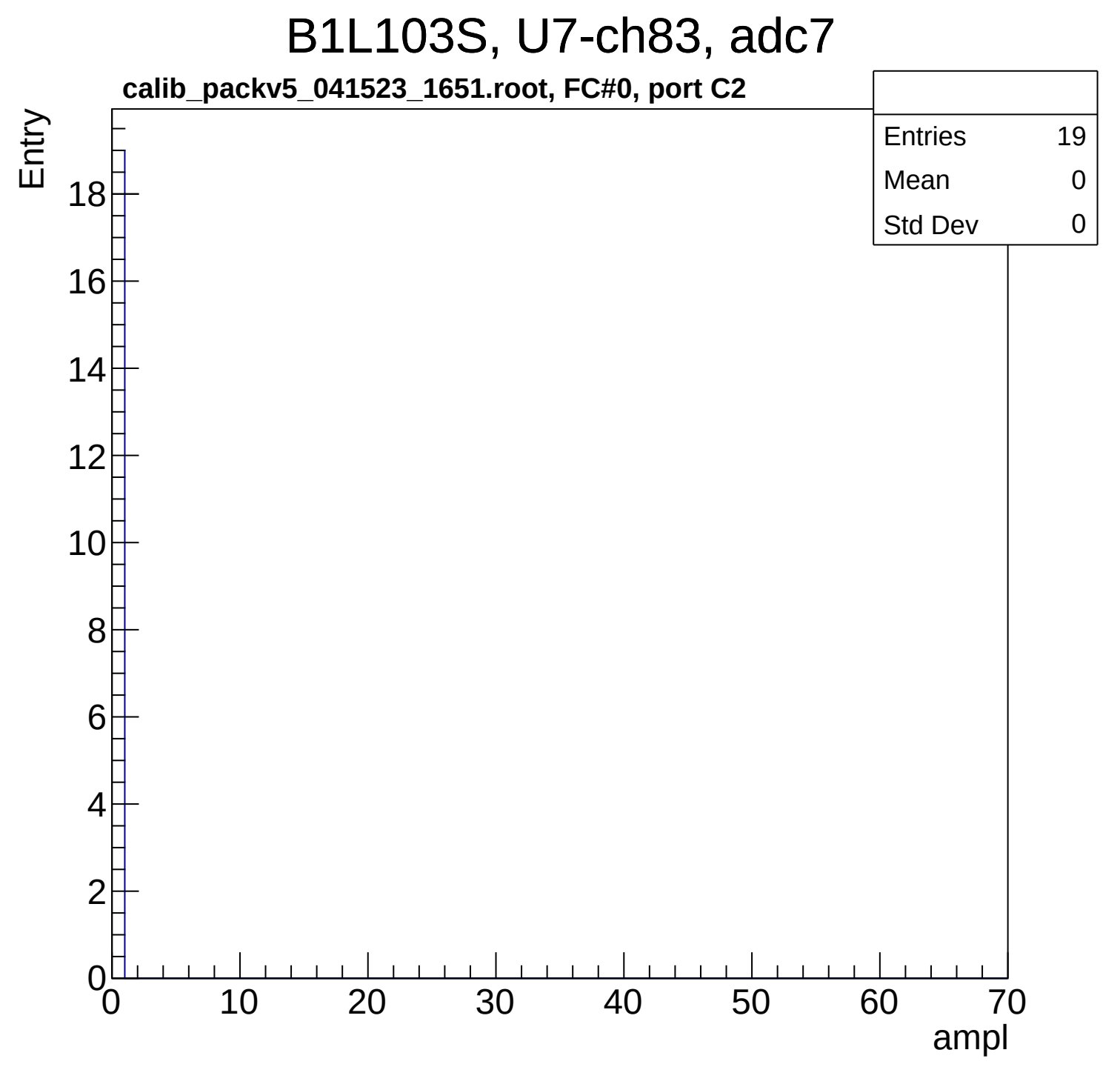
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch83, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
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6
8
10
12
14
16
18
0
10
20
30
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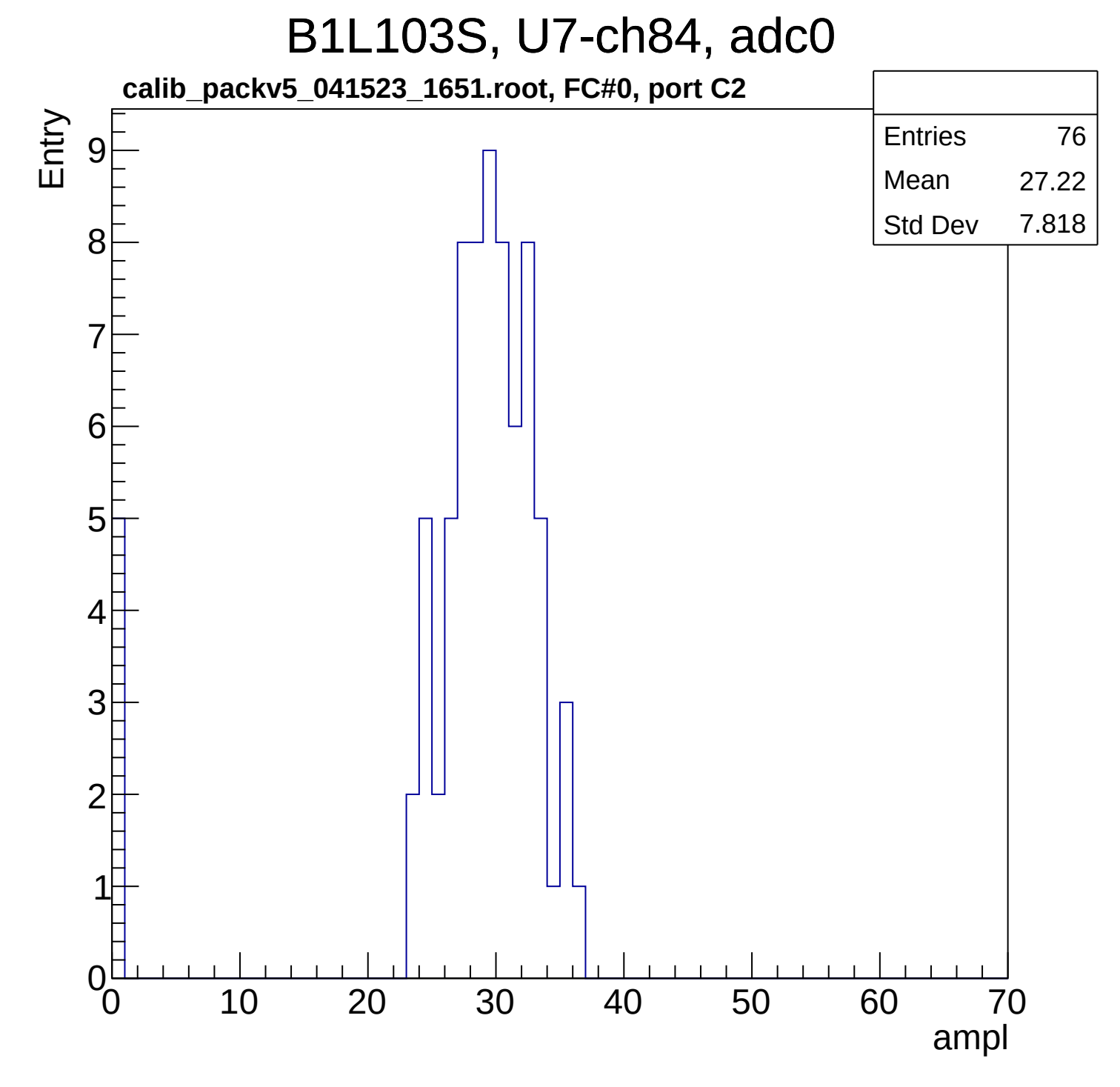
50
60
70
ampl


B1L103S, U7-ch84, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 27.22
Std Dev 7.818
Entry
ampl
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6
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60
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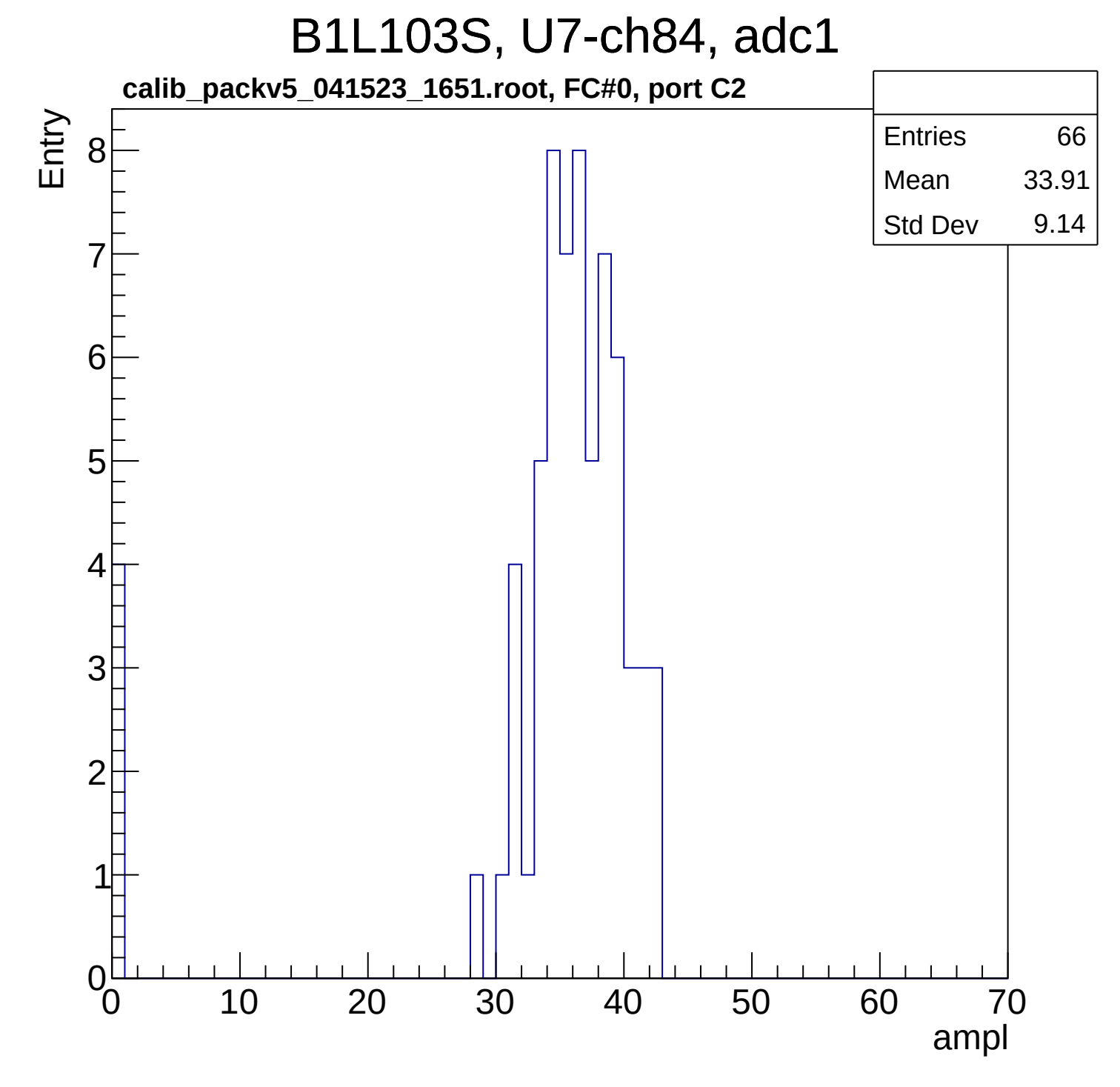
B1L103S, U7-ch84, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 33.91
Std Dev 9.14
Entry
ampl
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0
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60
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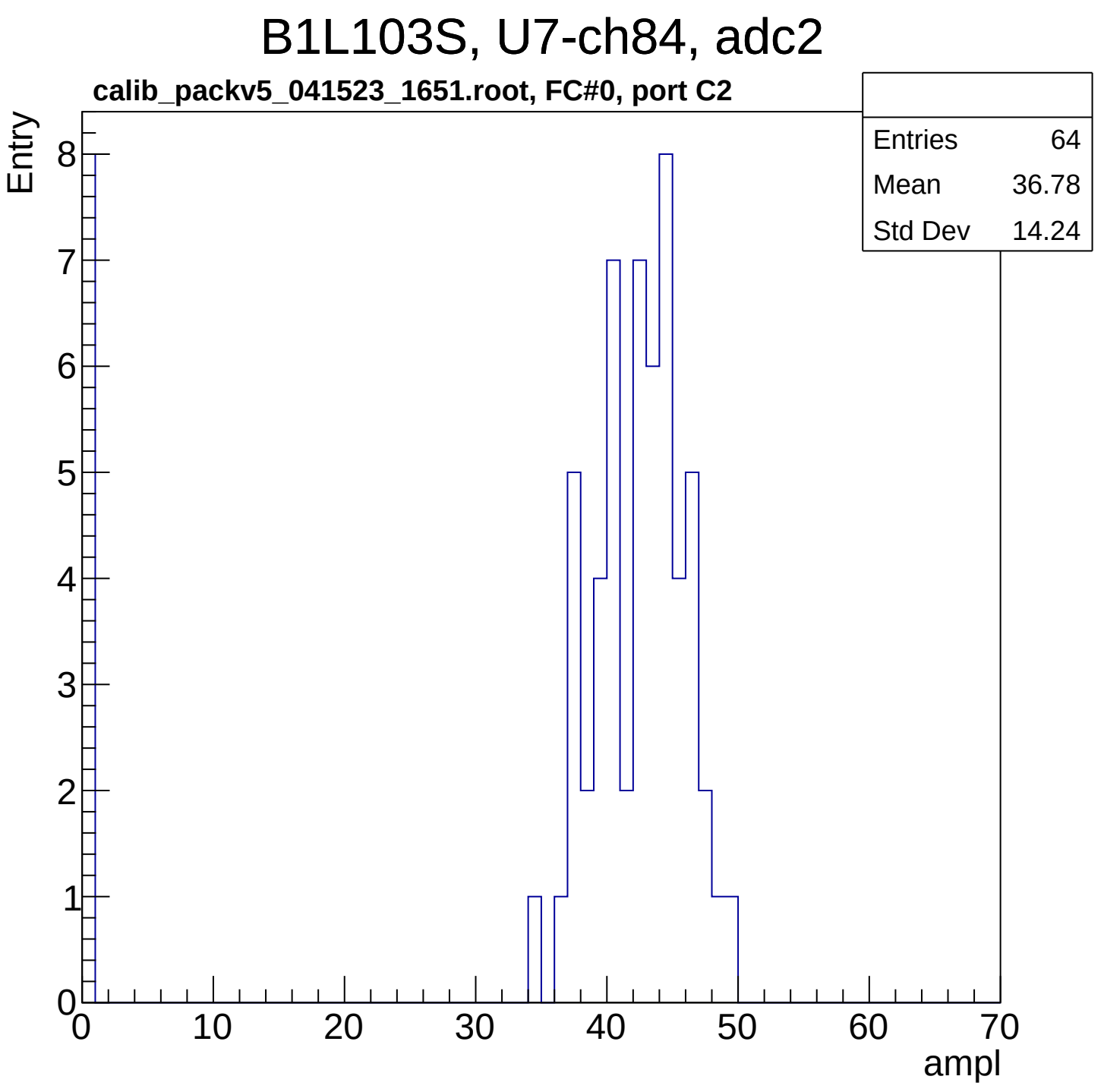
B1L103S, U7-ch84, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 36.78
Std Dev 14.24
Entry
ampl
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2
3
4
5
6
7
8
0
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60
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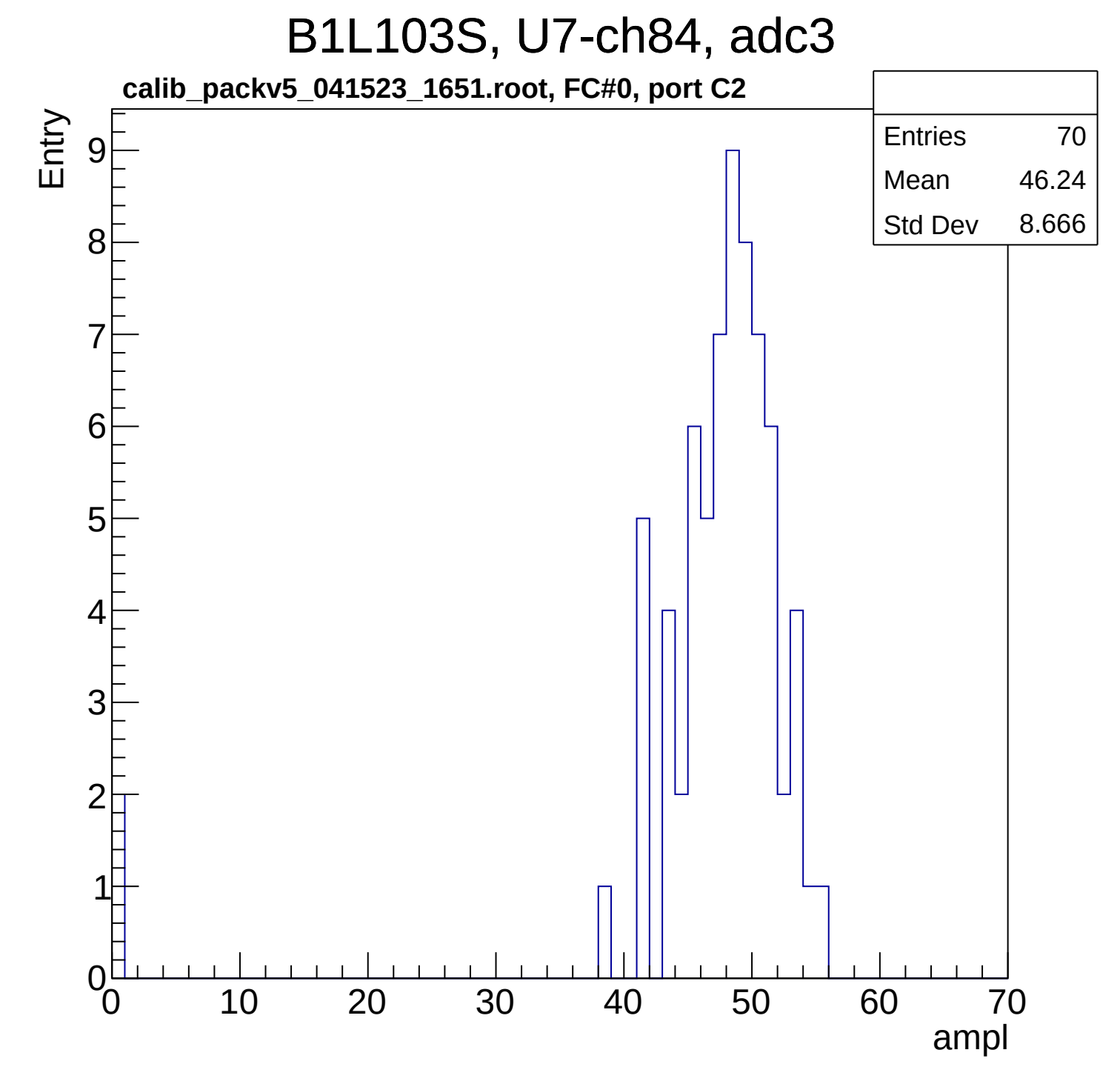
B1L103S, U7-ch84, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 46.24
Std Dev 8.666
Entry
ampl
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3
4
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6
7
8
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0
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60
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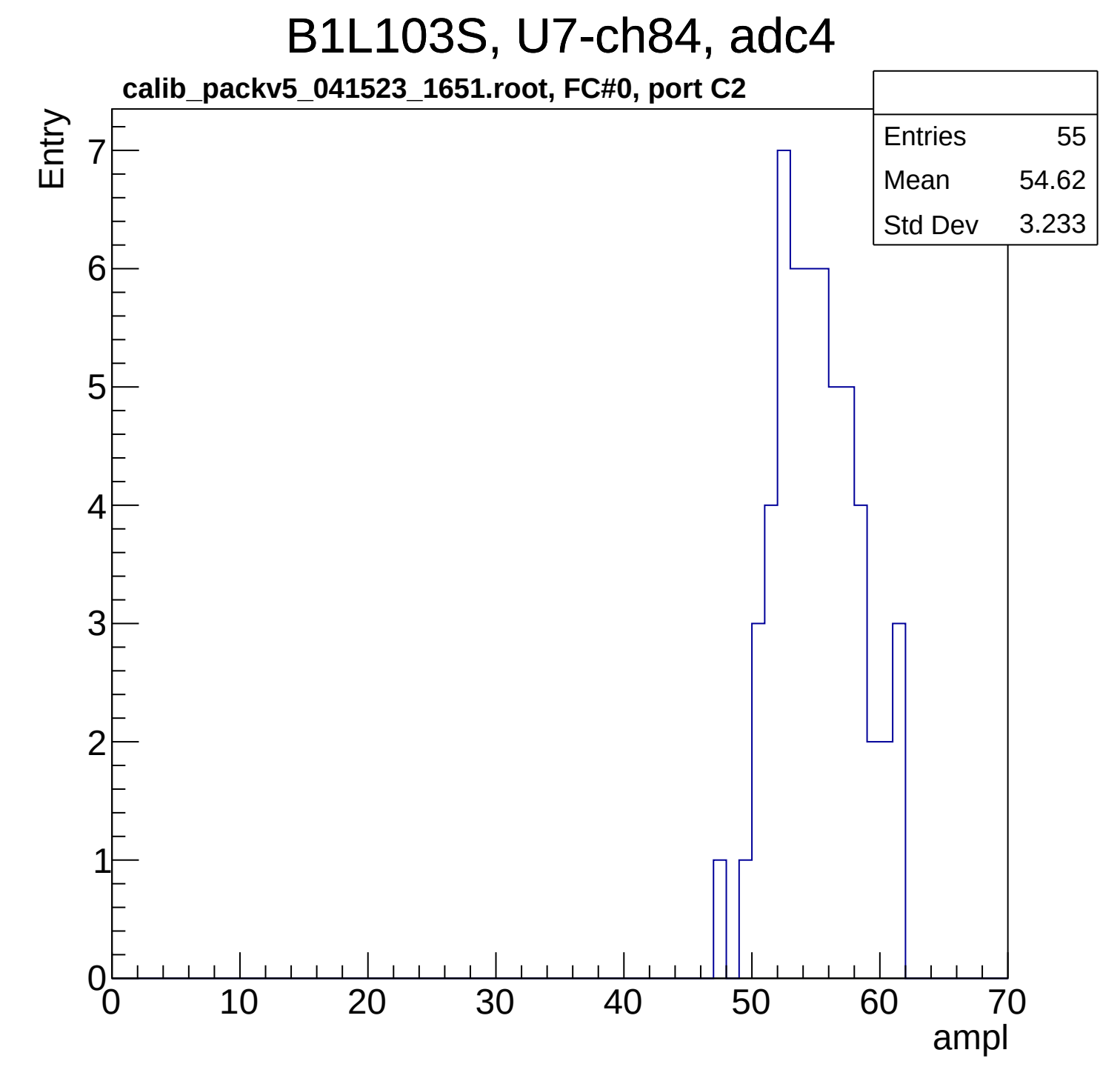
B1L103S, U7-ch84, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 54.62
Std Dev 3.233
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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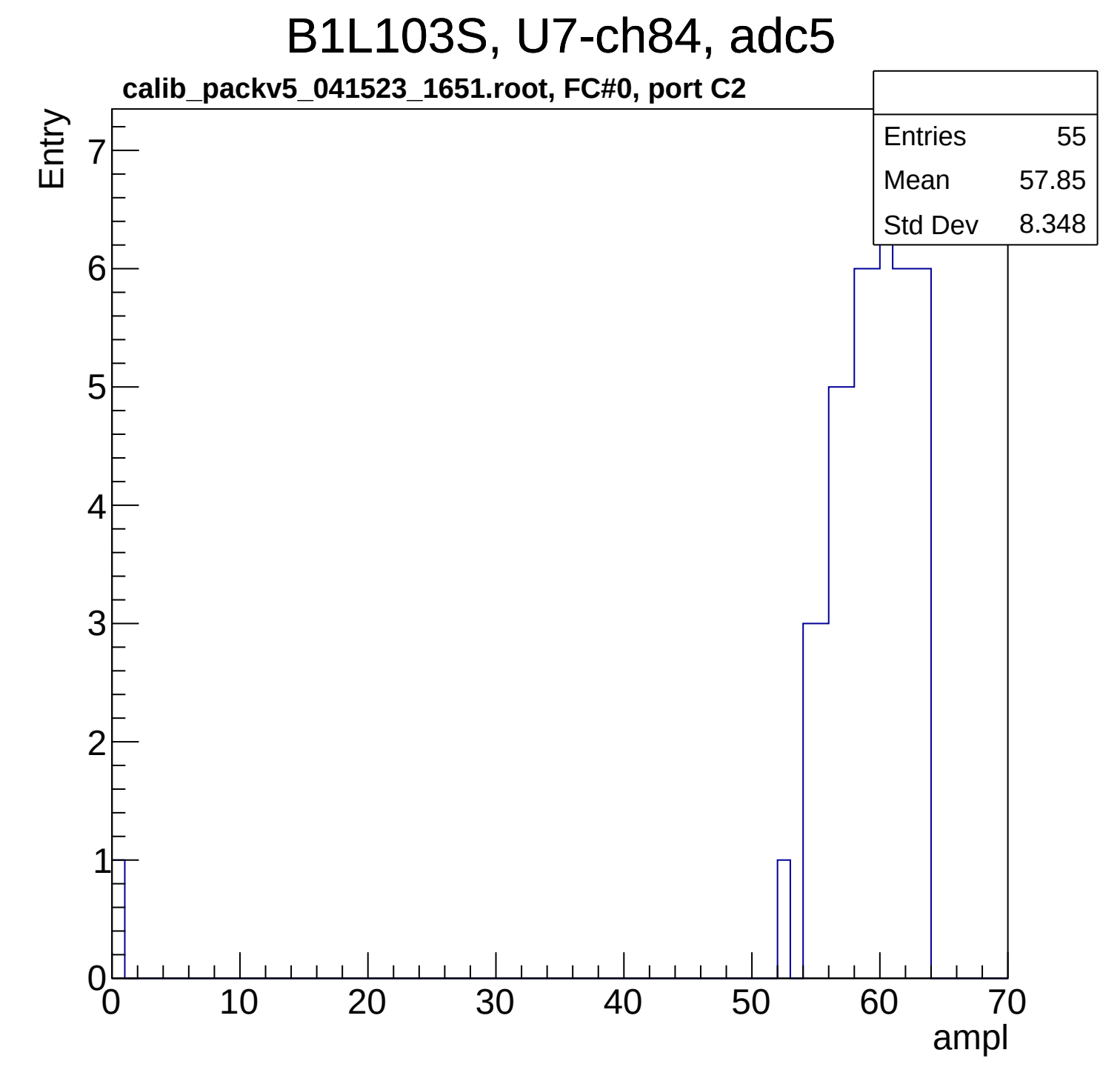
B1L103S, U7-ch84, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 57.85
Std Dev 8.348
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
30
40
50
60
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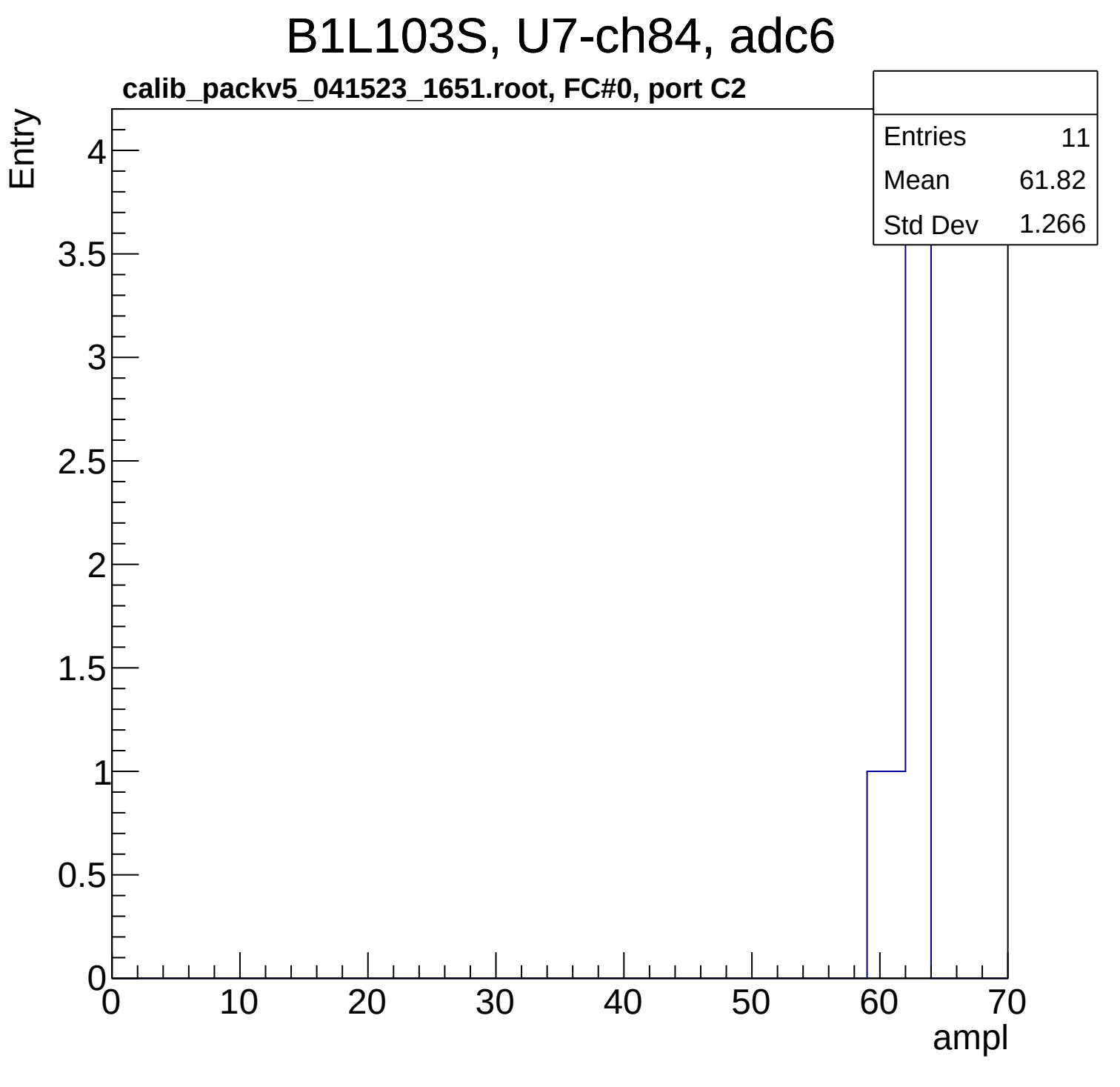
B1L103S, U7-ch84, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 61.82
Std Dev 1.266
Entry
ampl
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0.5
1
1.5
2
2.5
3
3.5
4
0
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20
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60
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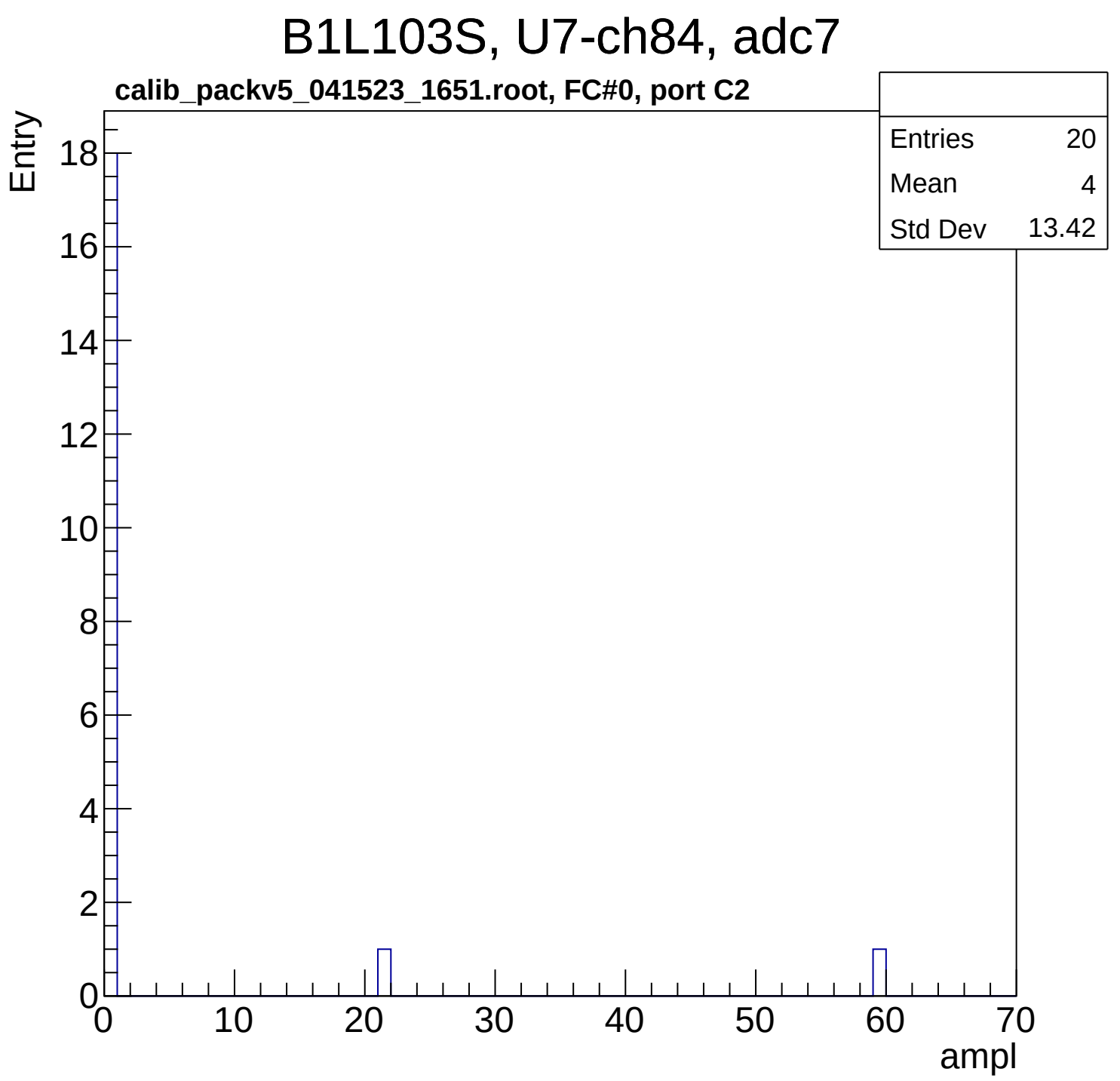
B1L103S, U7-ch84, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 4
Std Dev 13.42
Entry
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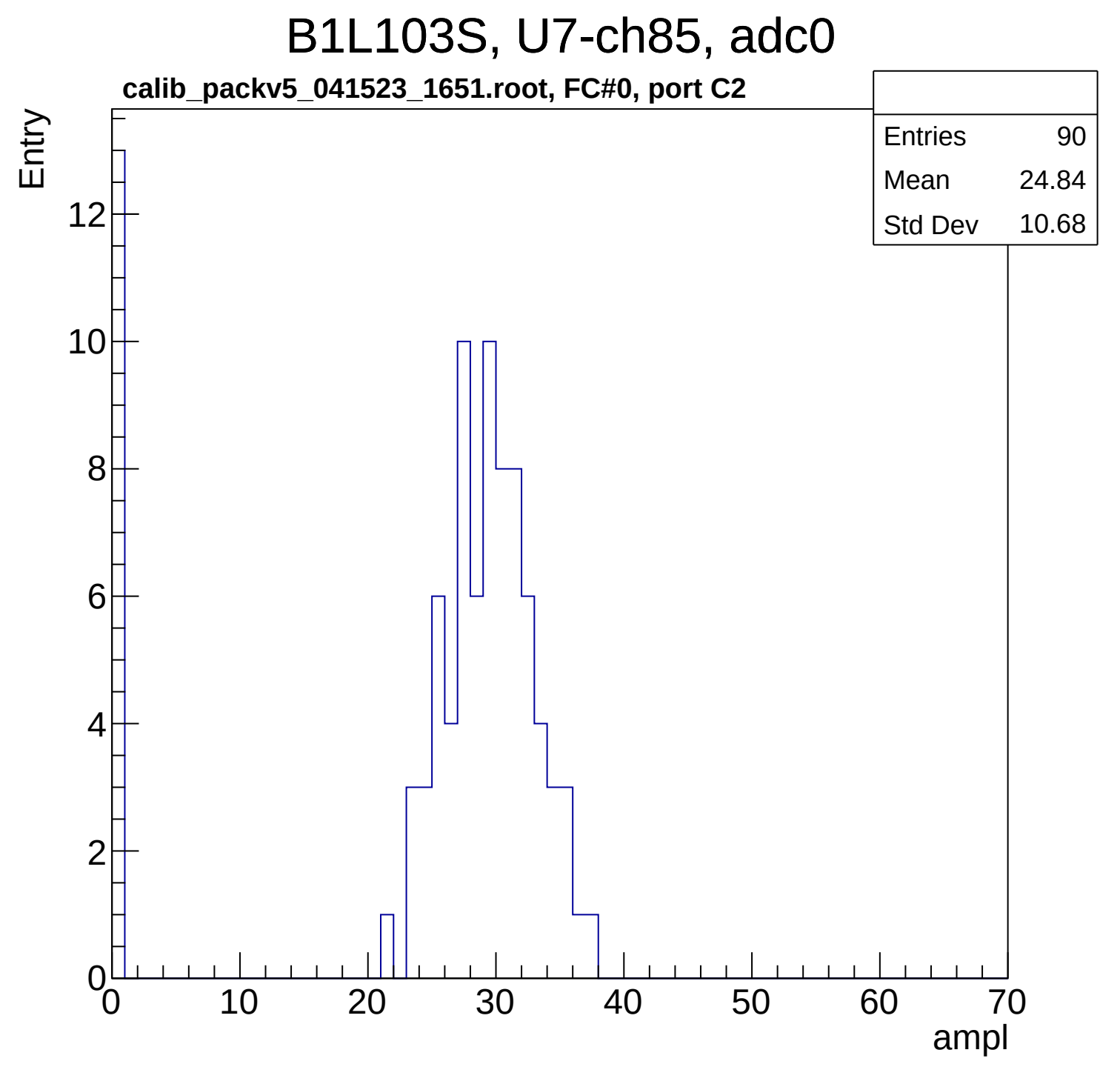
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch85, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 90
Mean 24.84
Std Dev 10.68
Entry
0
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4
6
8
10
12
0
10
20
30
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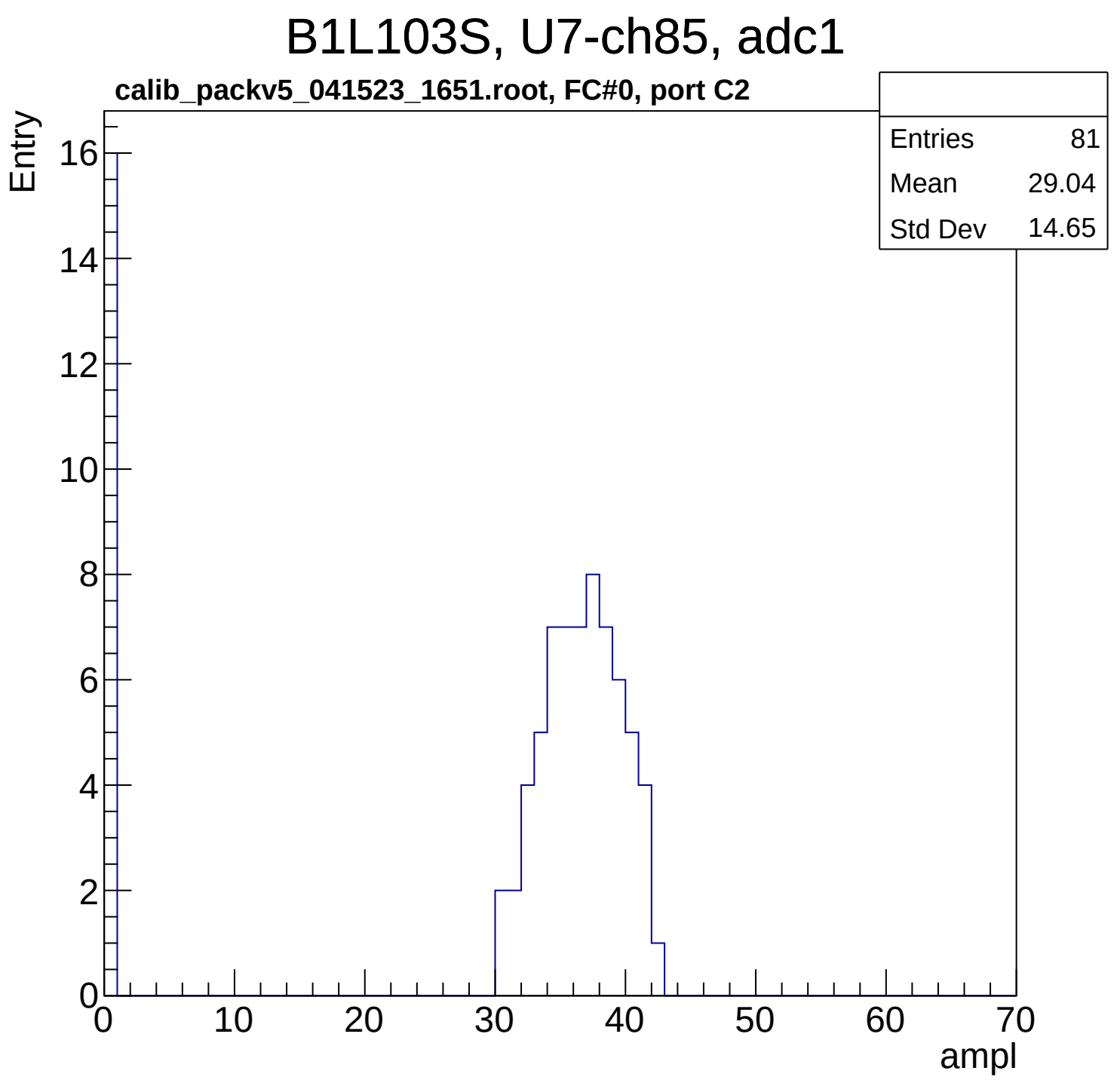
50
60
70
ampl


B1L103S, U7-ch85, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 29.04
Std Dev 14.65
Entry
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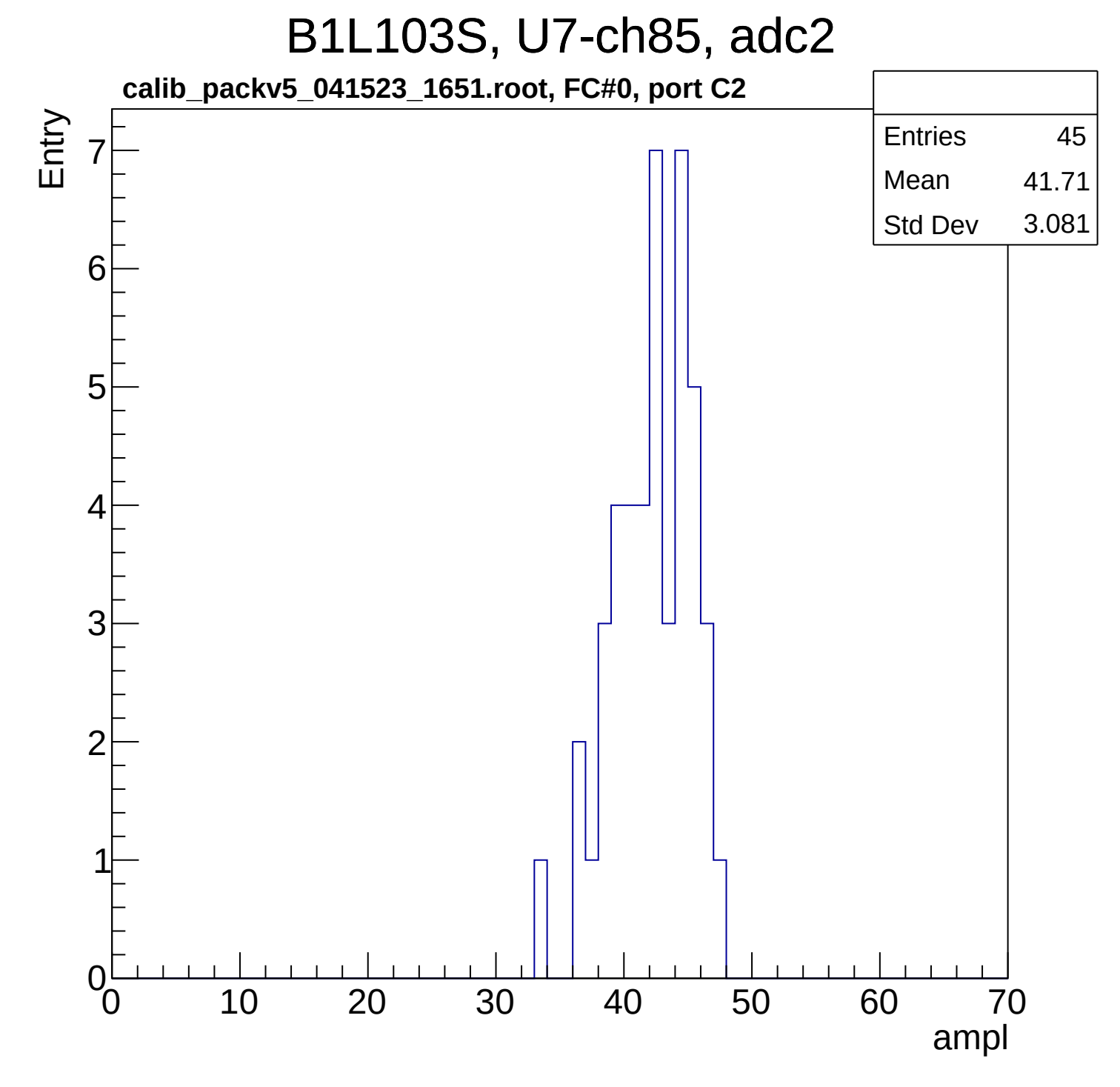
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch85, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 41.71
Std Dev 3.081
Entry
ampl
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2
3
4
5
6
7
0
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20
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40
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60
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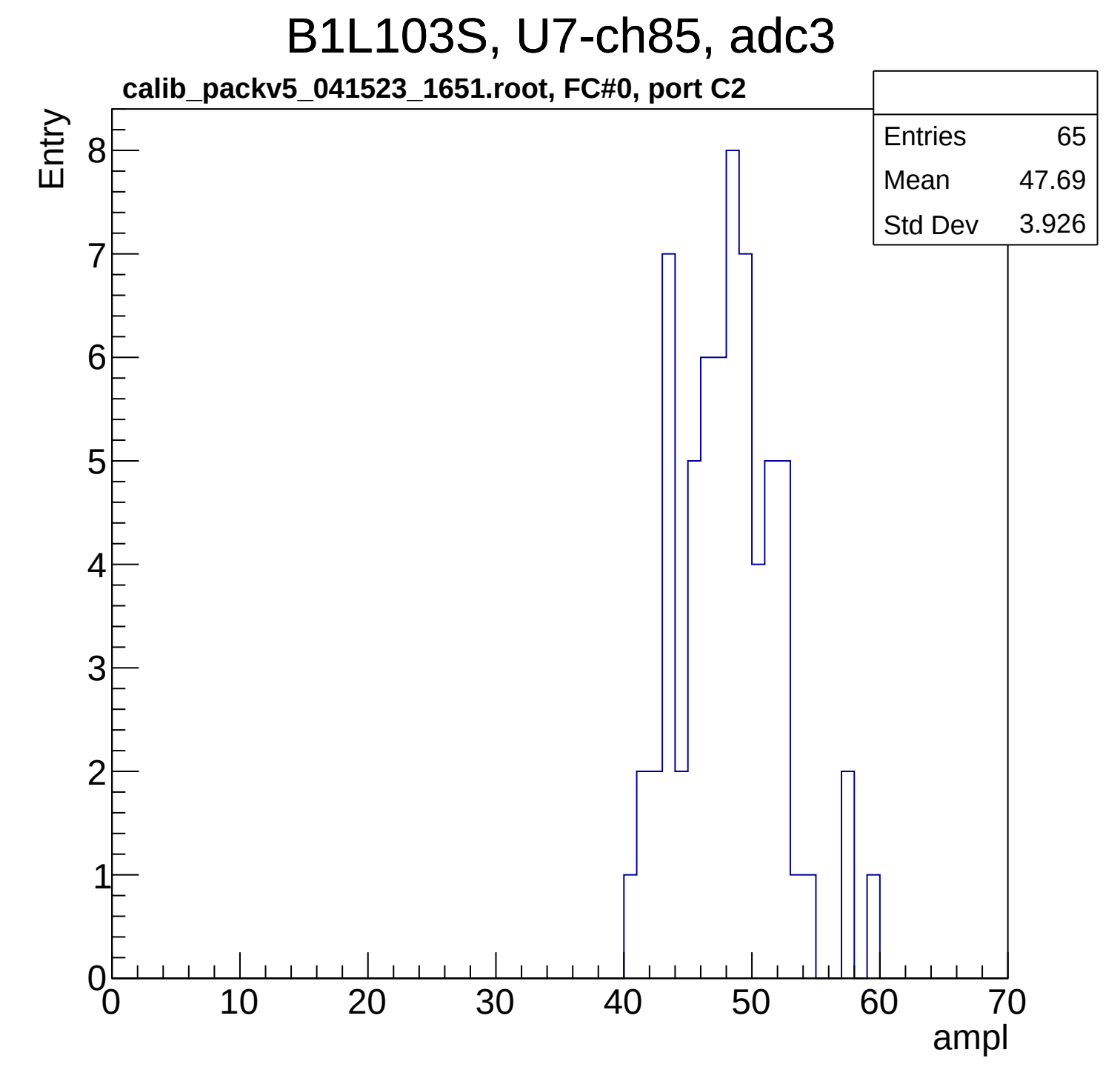
B1L103S, U7-ch85, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 47.69
Std Dev 3.926
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
30
40
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60
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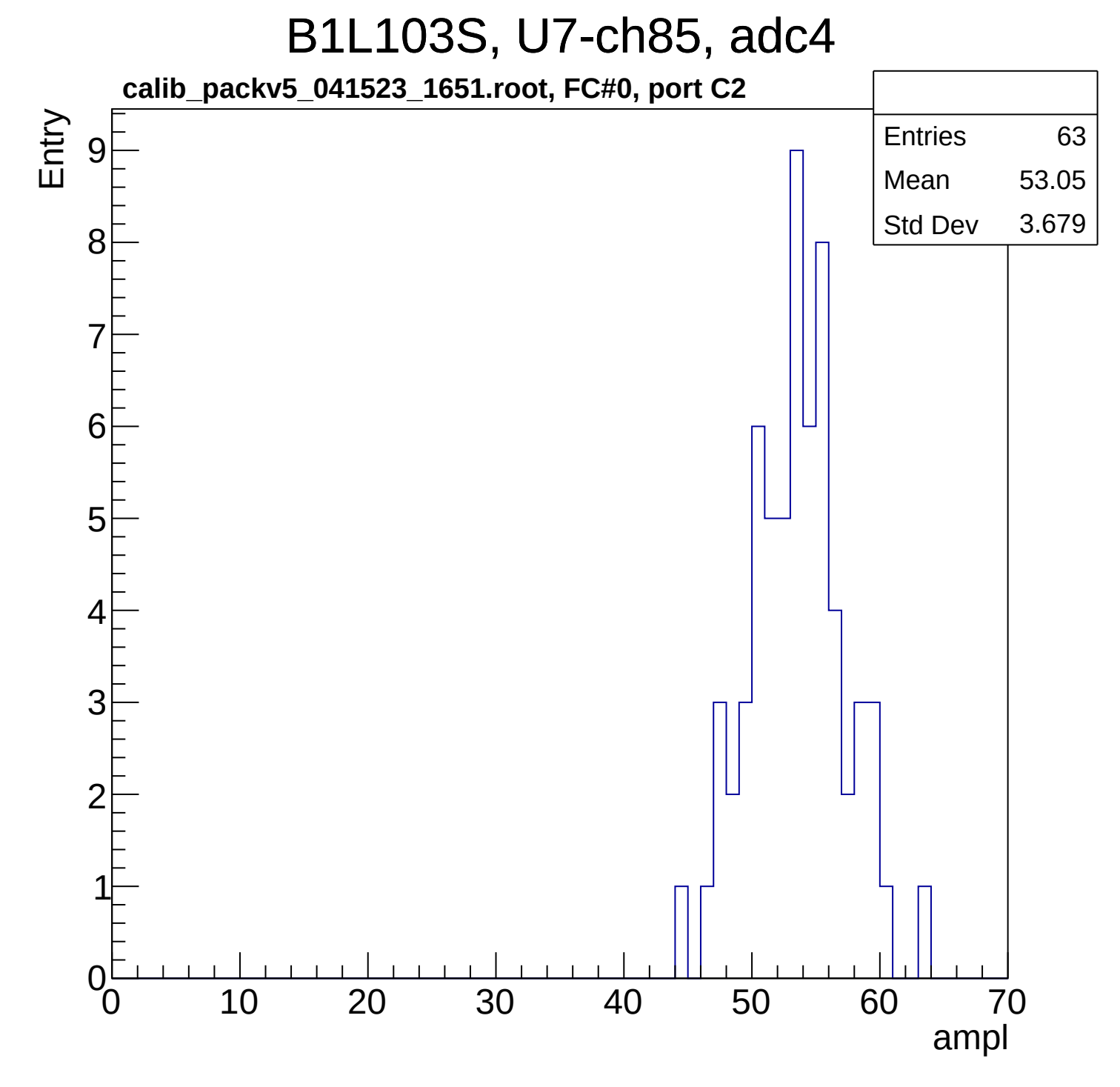
B1L103S, U7-ch85, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 53.05
Std Dev 3.679
Entry
ampl
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3
4
5
6
7
8
9
0
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20
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40
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60
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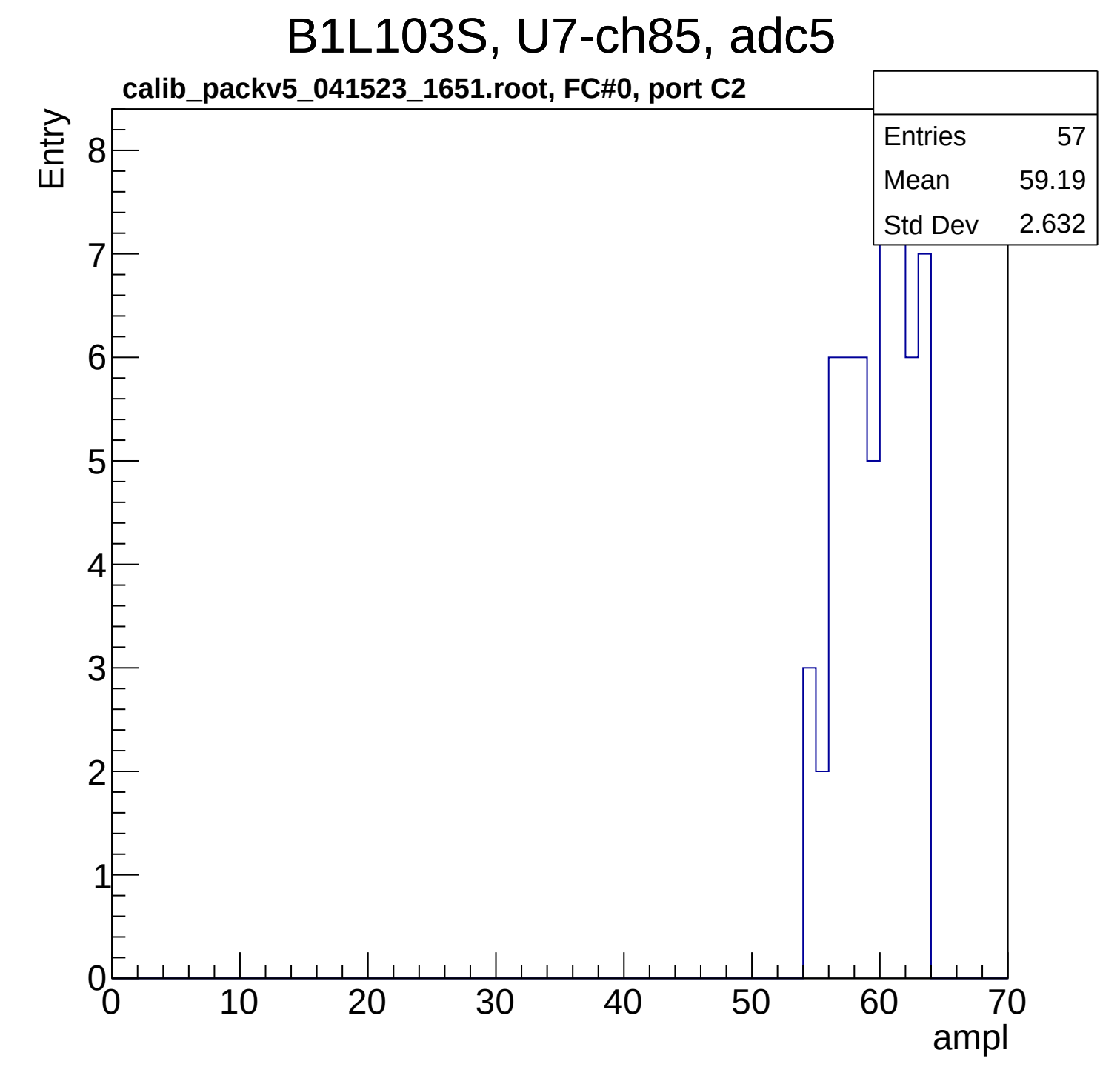
B1L103S, U7-ch85, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 59.19
Std Dev 2.632
Entry
ampl
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3
4
5
6
7
8
0
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20
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40
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60
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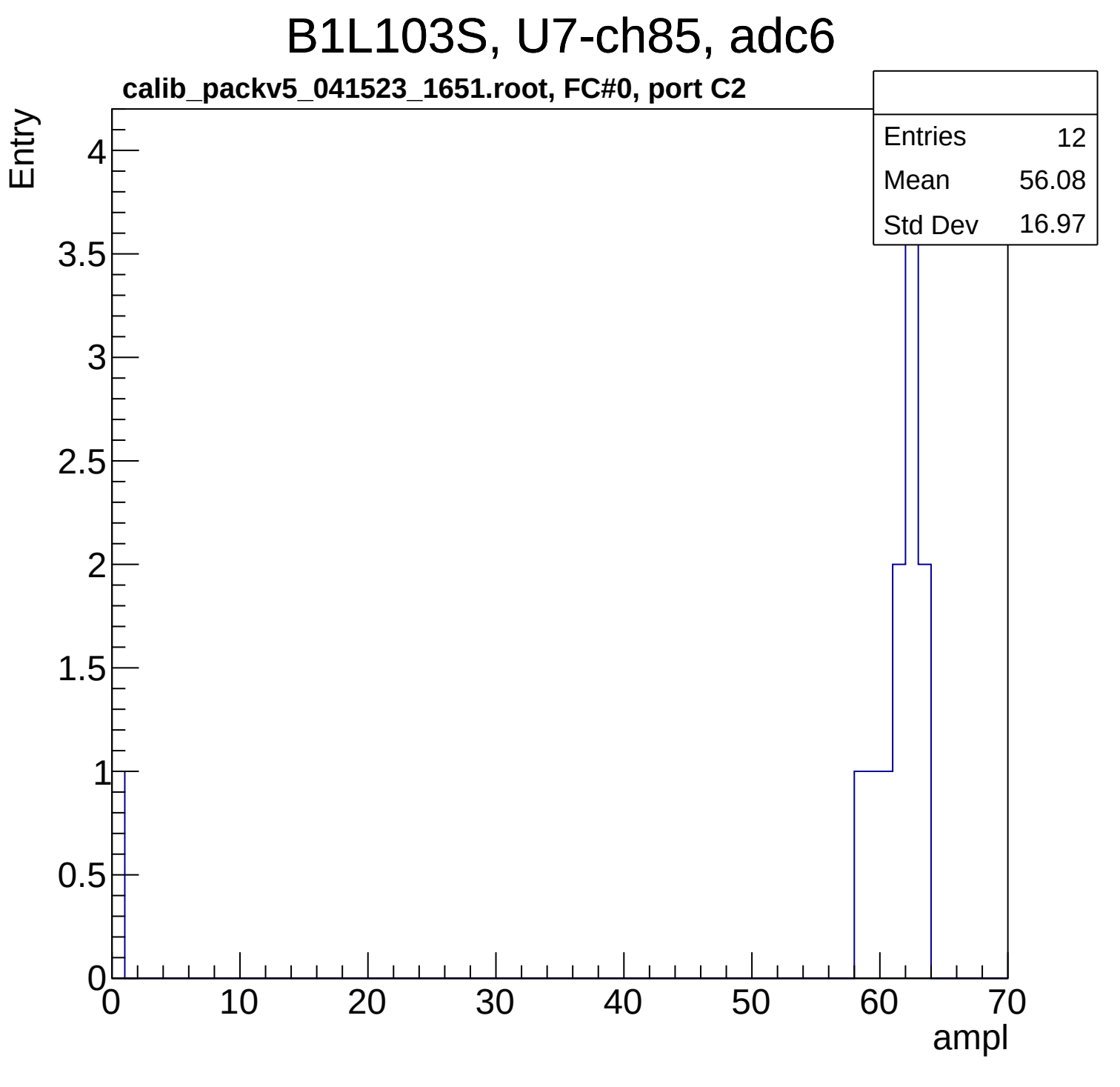
B1L103S, U7-ch85, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 56.08
Std Dev 16.97
Entry
ampl
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1.5
2
2.5
3
3.5
4
0
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20
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60
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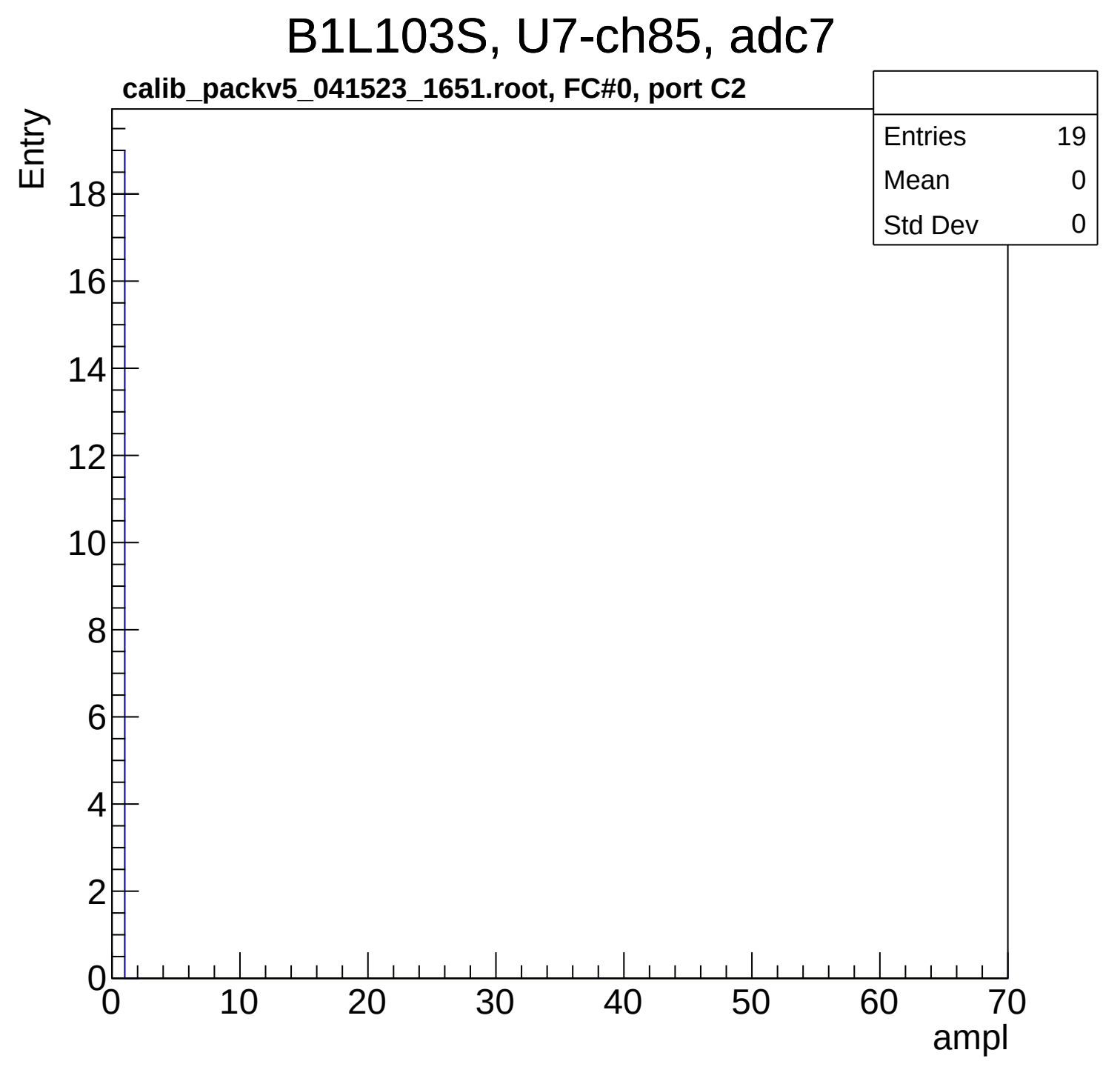
B1L103S, U7-ch85, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
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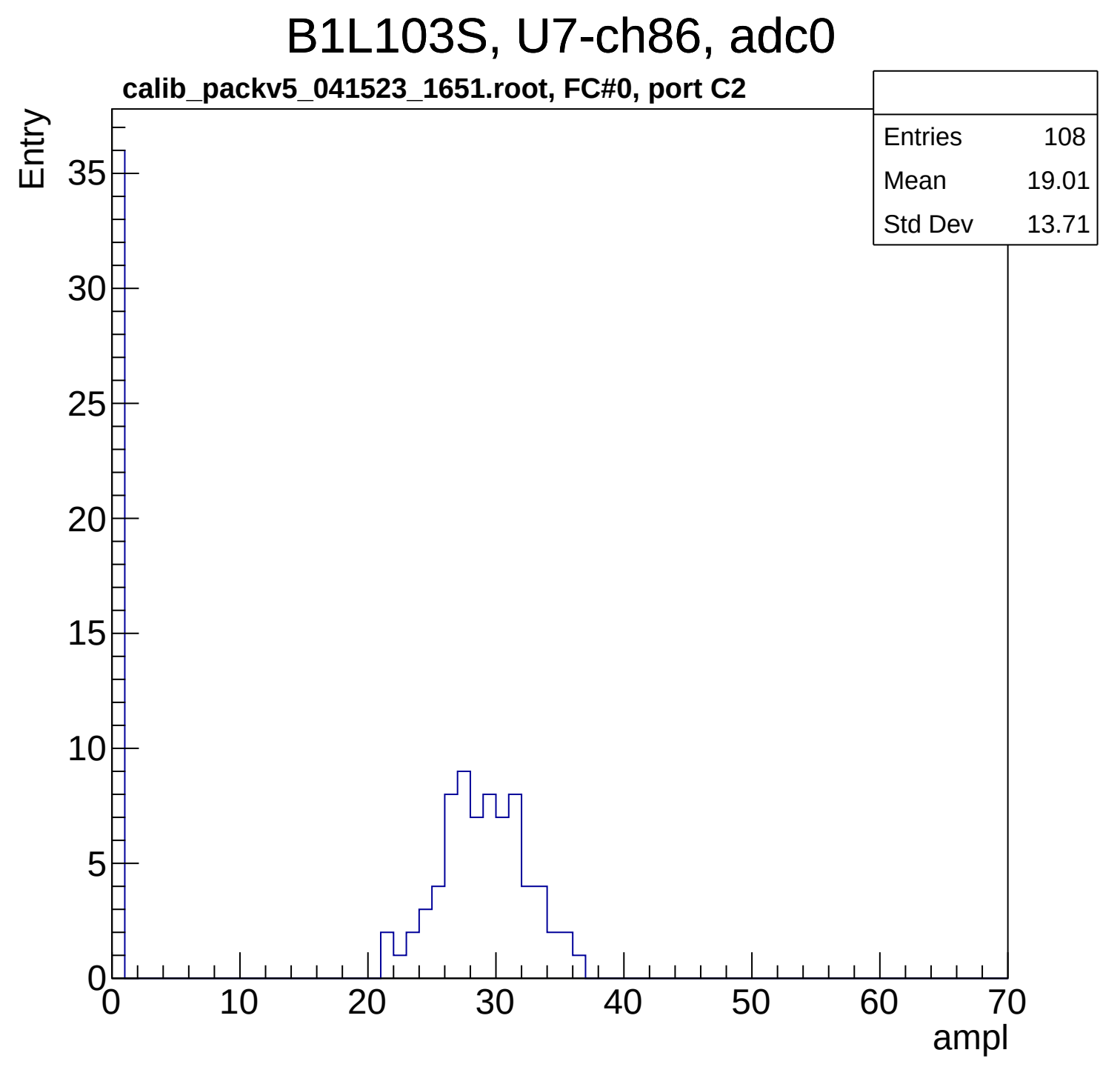
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch86, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 108
Mean 19.01
Std Dev 13.71
Entry
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15
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35
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10
20
30
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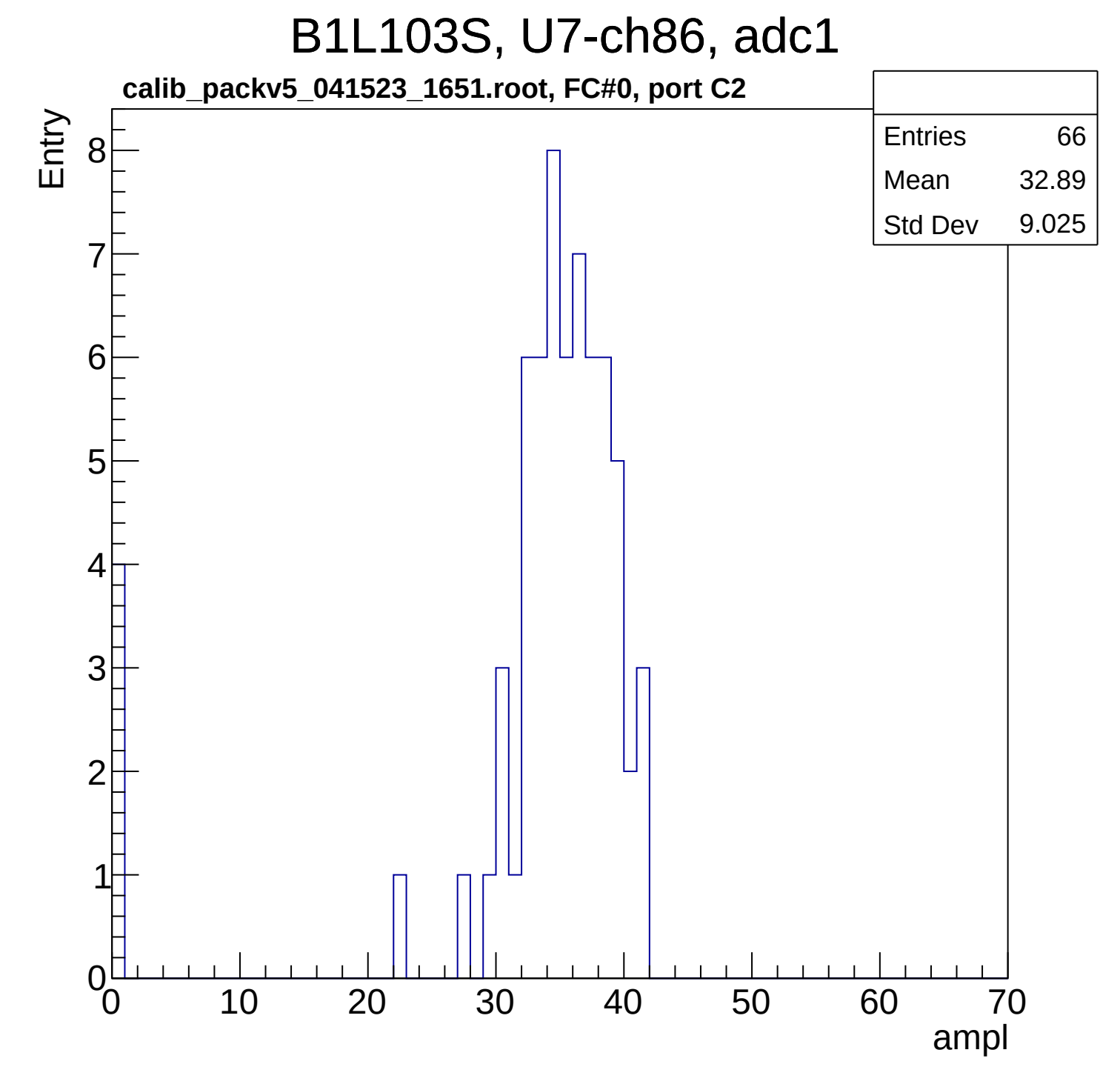
50
60
70
ampl


B1L103S, U7-ch86, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 32.89
Std Dev 9.025
Entry
ampl
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2
3
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5
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7
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0
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40
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60
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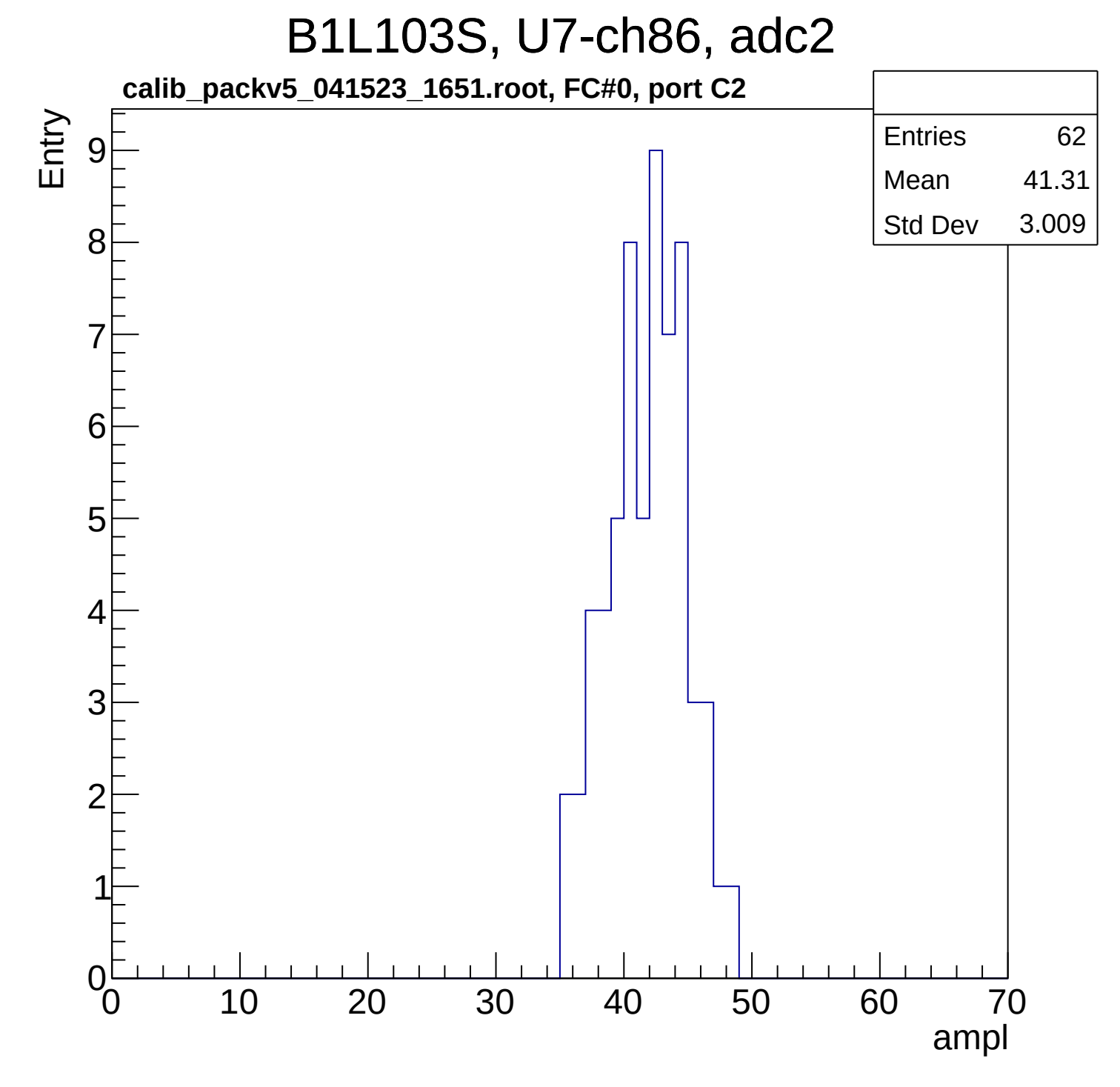
B1L103S, U7-ch86, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 41.31
Std Dev 3.009
Entry
ampl
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8
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0
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60
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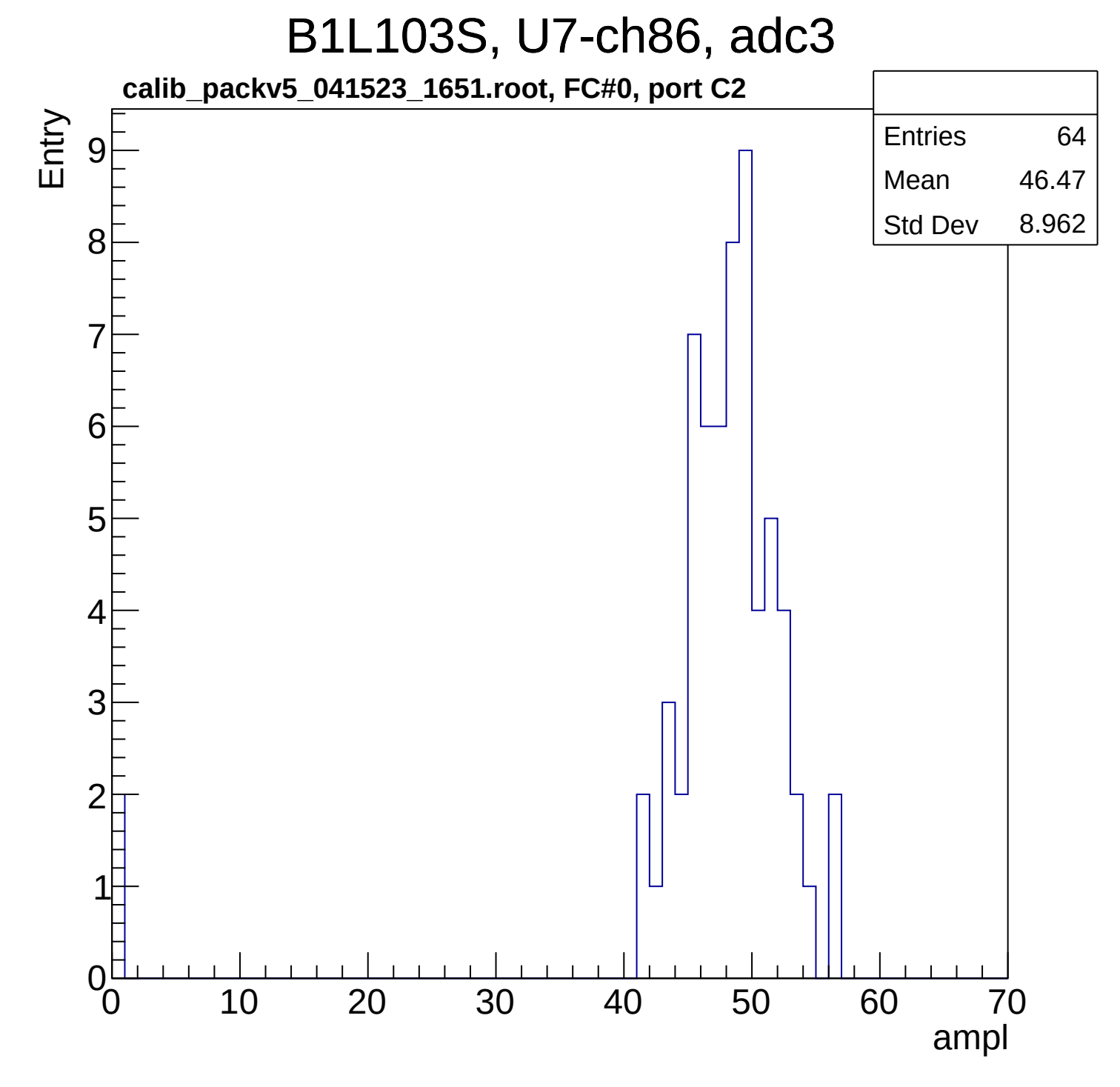
B1L103S, U7-ch86, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 46.47
Std Dev 8.962
Entry
ampl
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4
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6
7
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0
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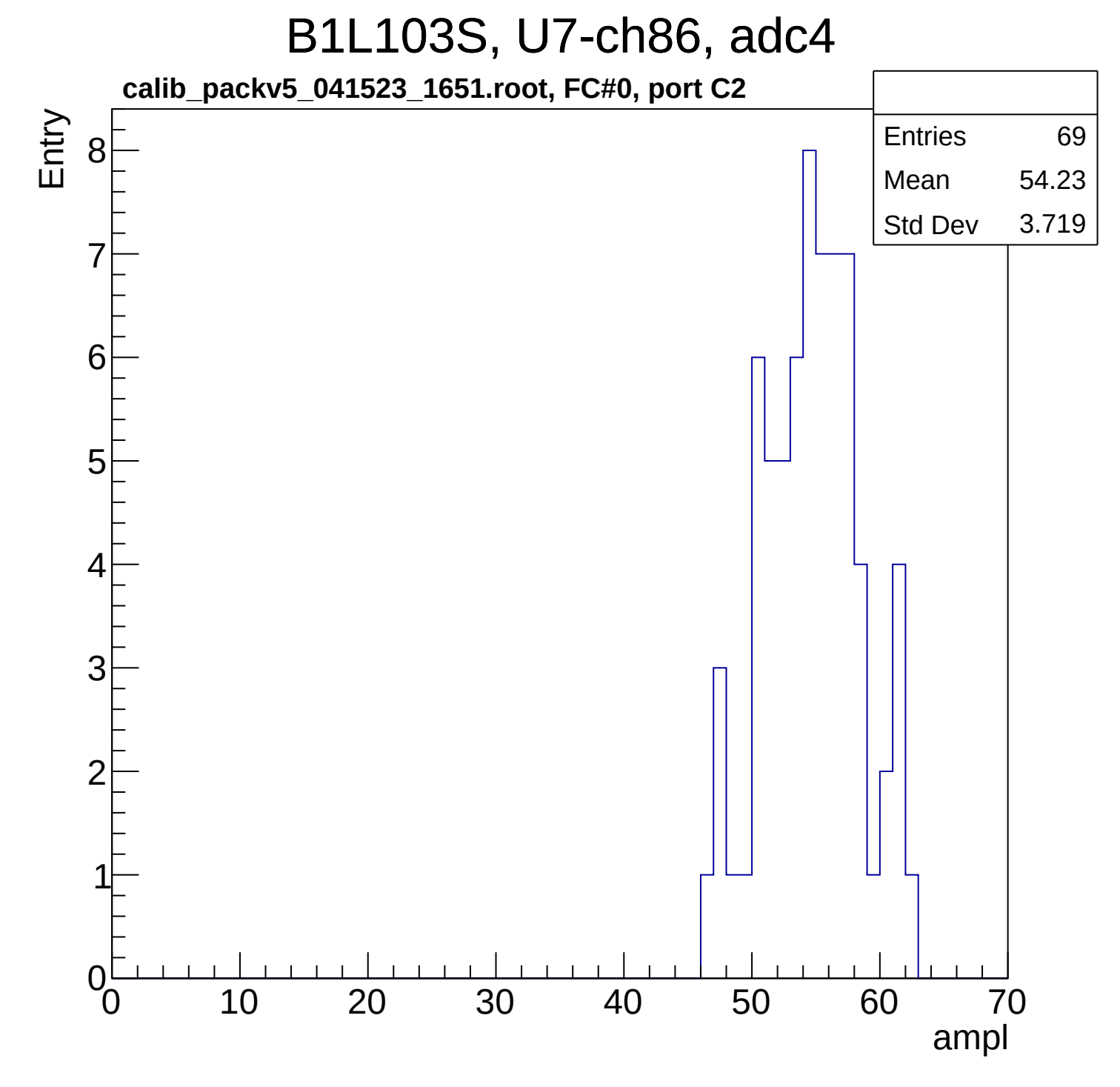
B1L103S, U7-ch86, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 54.23
Std Dev 3.719
Entry
ampl
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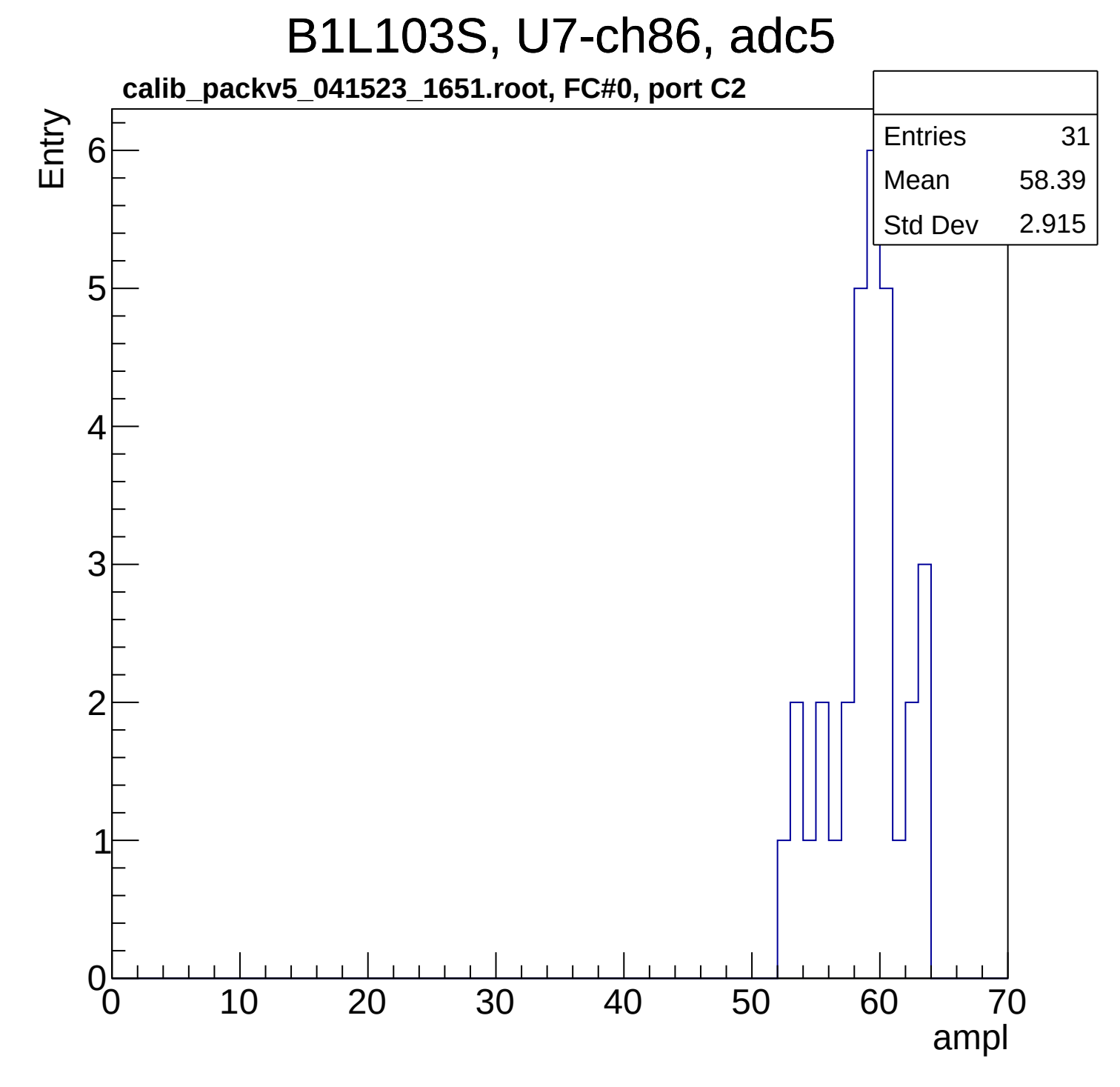
B1L103S, U7-ch86, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 31
Mean 58.39
Std Dev 2.915
Entry
ampl
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1
2
3
4
5
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0
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20
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40
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60
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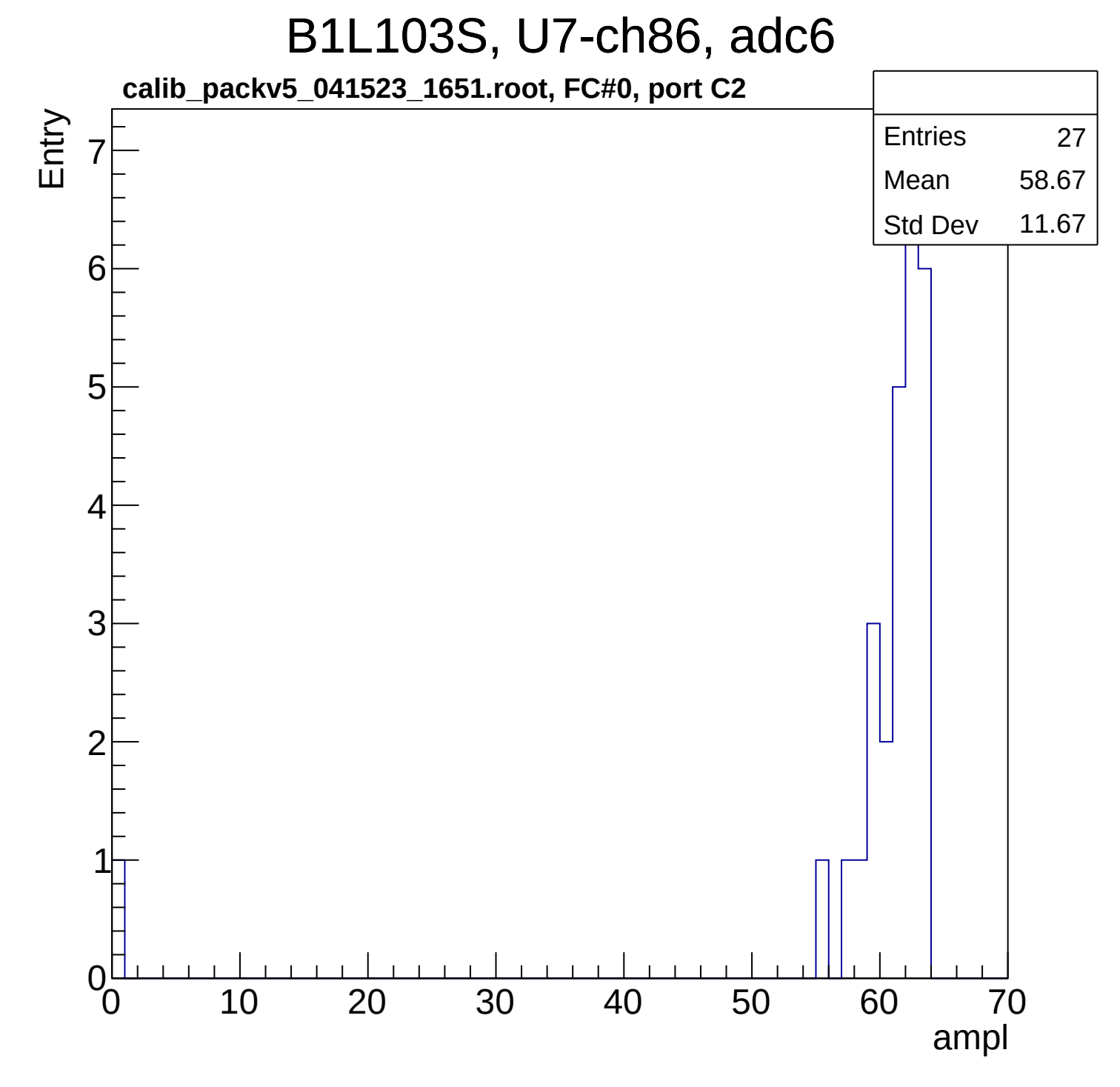
B1L103S, U7-ch86, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 27
Mean 58.67
Std Dev 11.67
Entry
ampl
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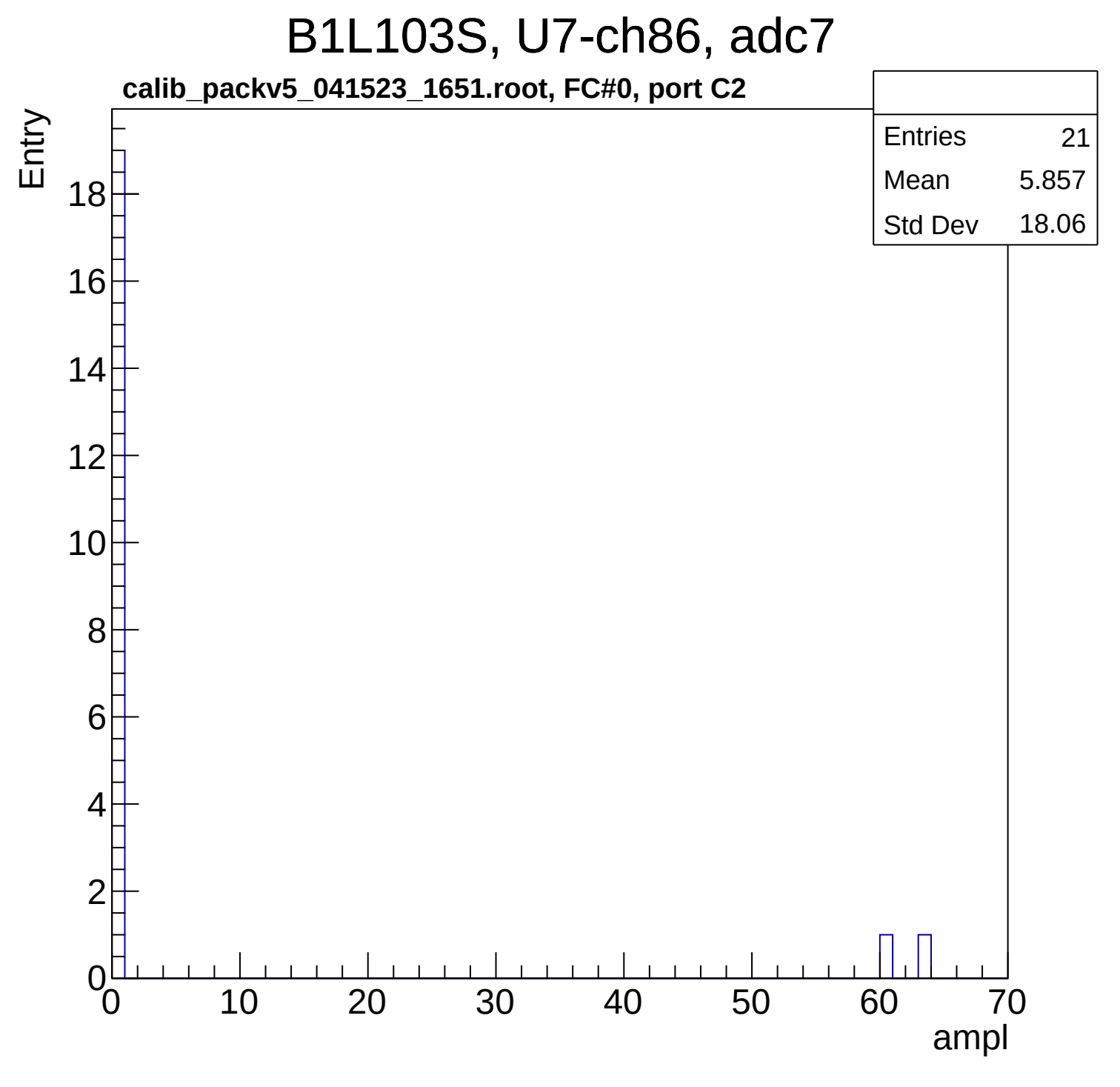
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U7-ch86, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 5.857
Std Dev 18.06
Entry
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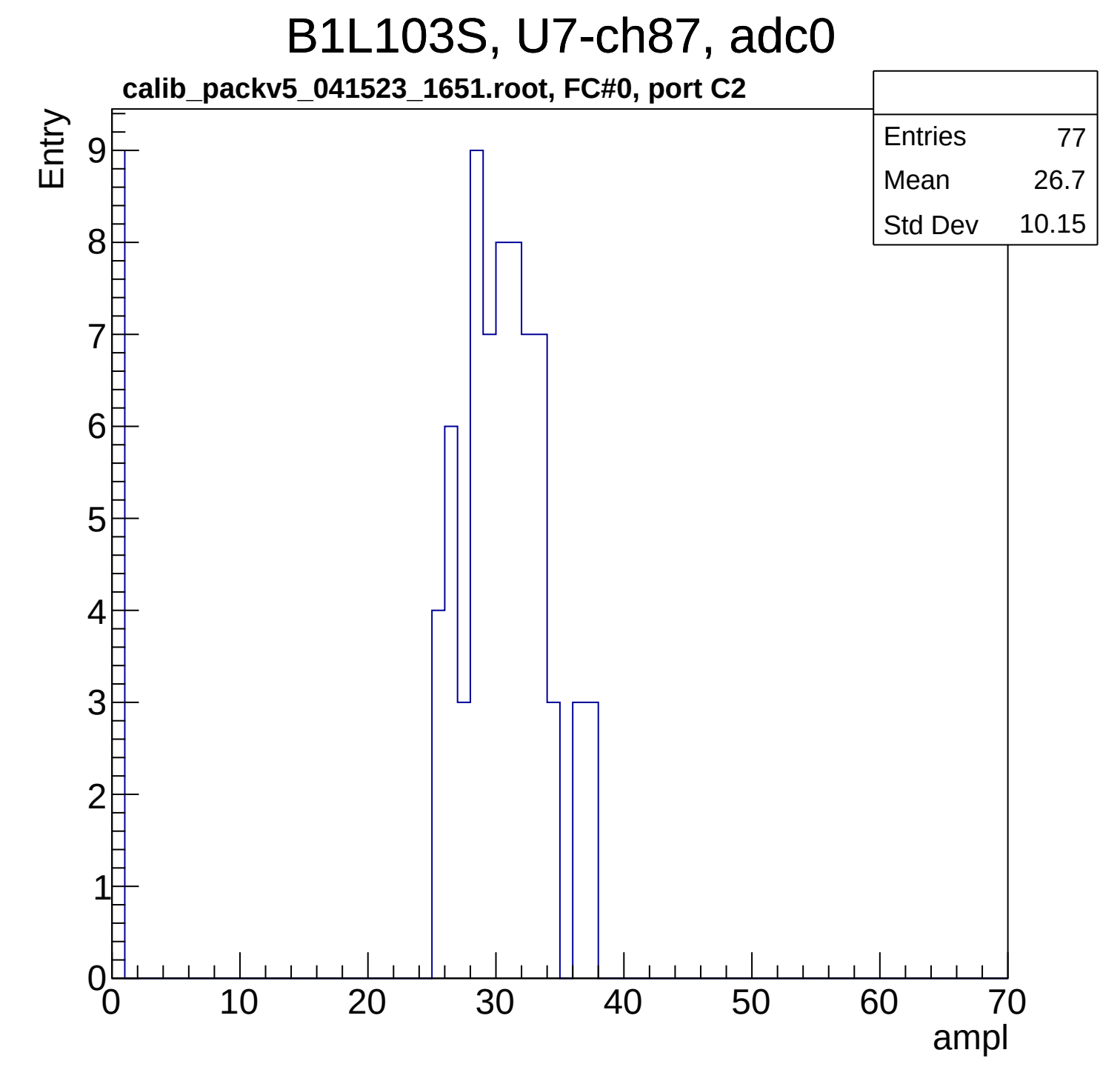
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch87, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 26.7
Std Dev 10.15
Entry
ampl
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5
6
7
8
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0
10
20
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40
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60
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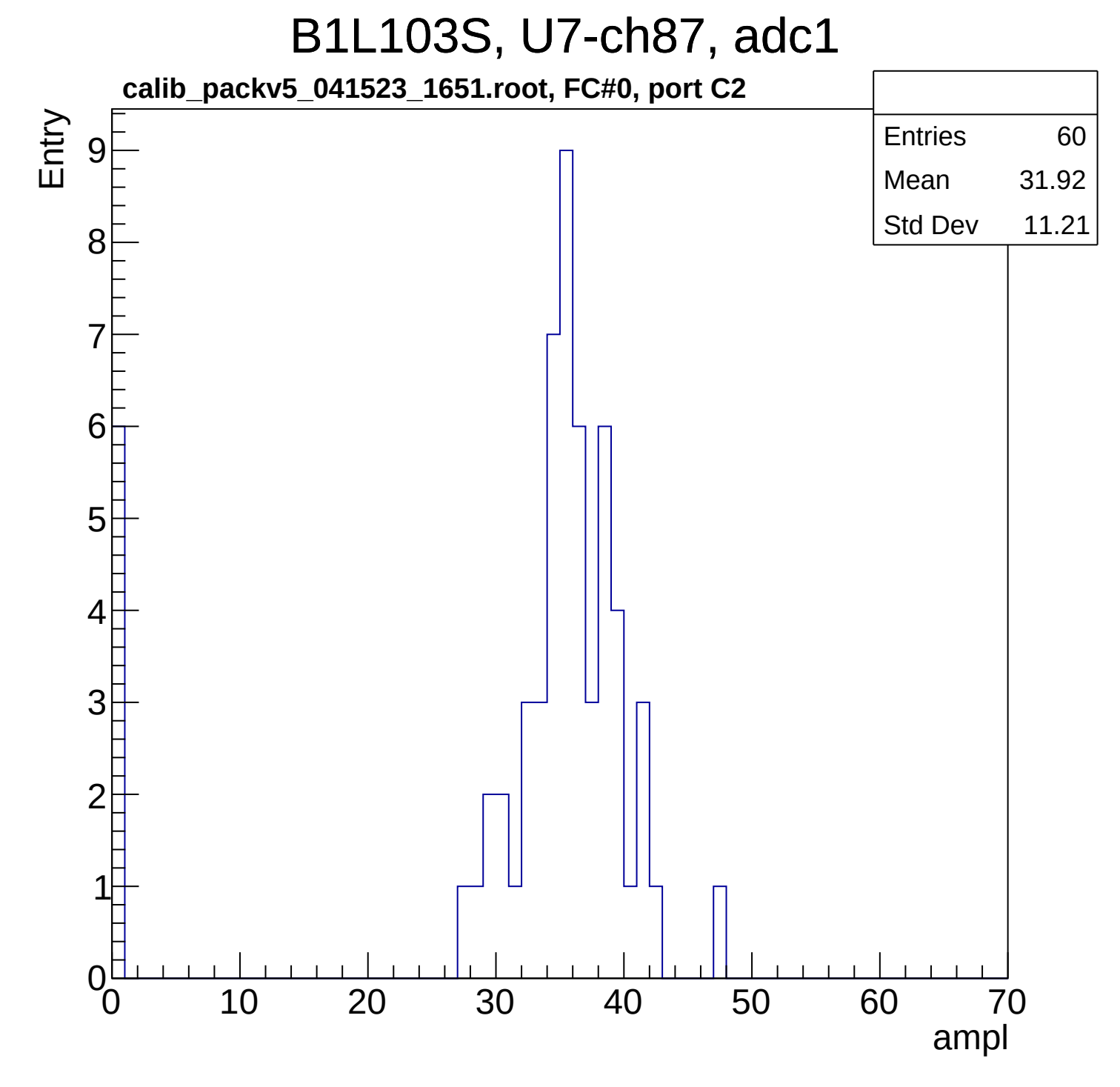
B1L103S, U7-ch87, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 31.92
Std Dev 11.21
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
50
60
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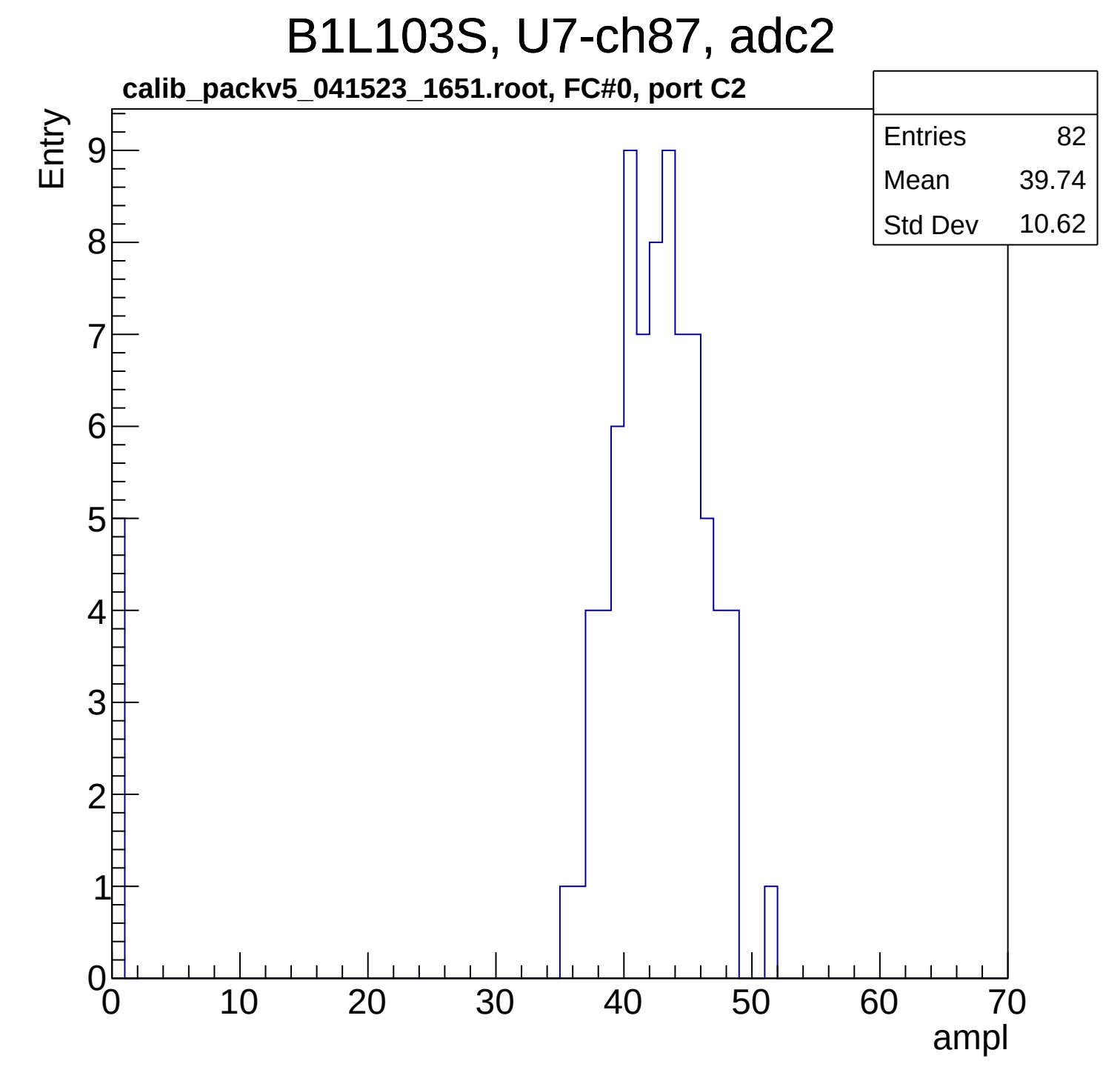
B1L103S, U7-ch87, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 39.74
Std Dev 10.62
Entry
ampl
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2
3
4
5
6
7
8
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0
10
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40
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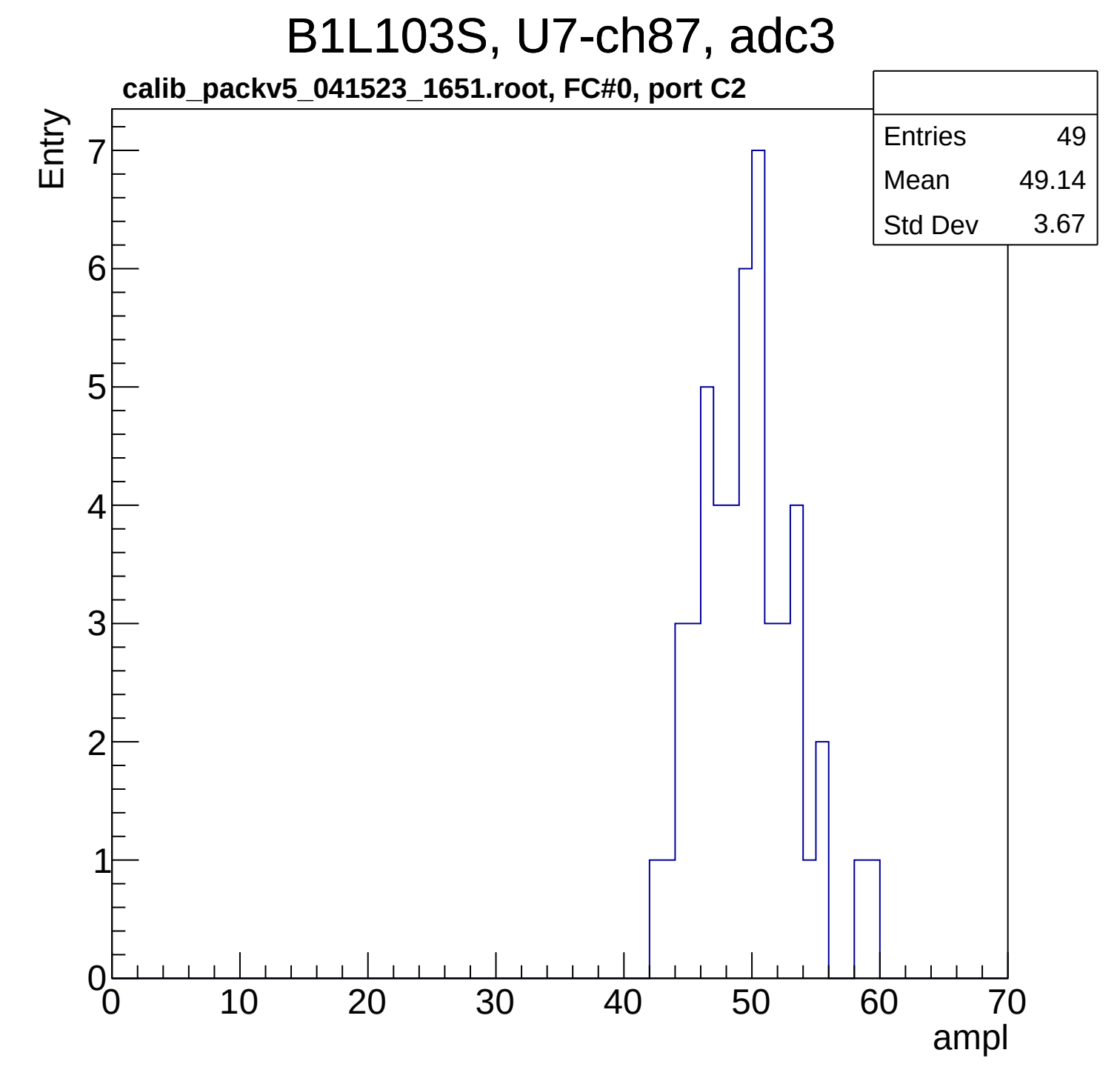
60
70


B1L103S, U7-ch87, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 49.14
Std Dev 3.67
Entry
ampl
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1
2
3
4
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6
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0
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40
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60
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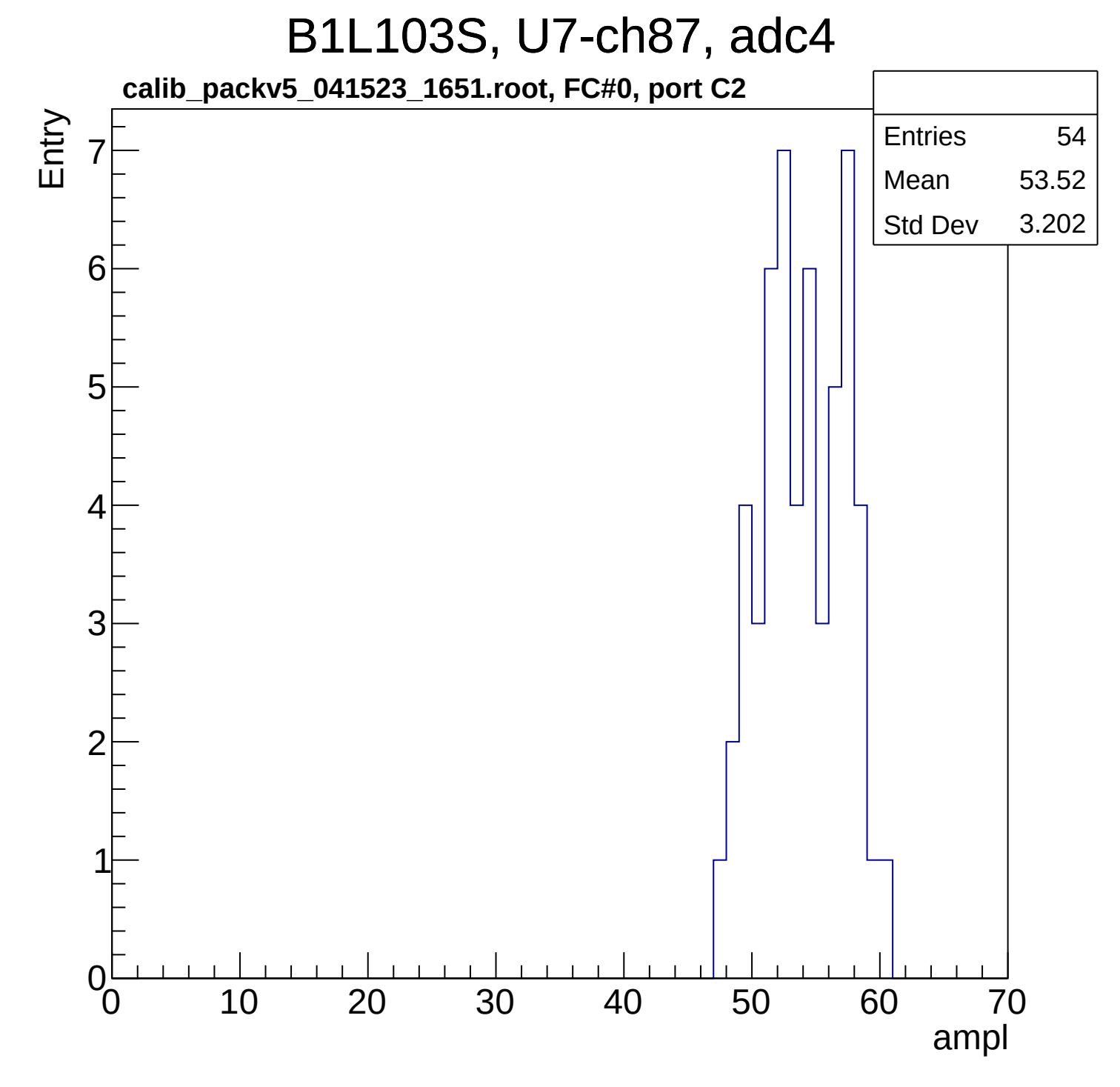
B1L103S, U7-ch87, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 53.52
Std Dev 3.202
Entry
ampl
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2
3
4
5
6
7
0
10
20
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40
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60
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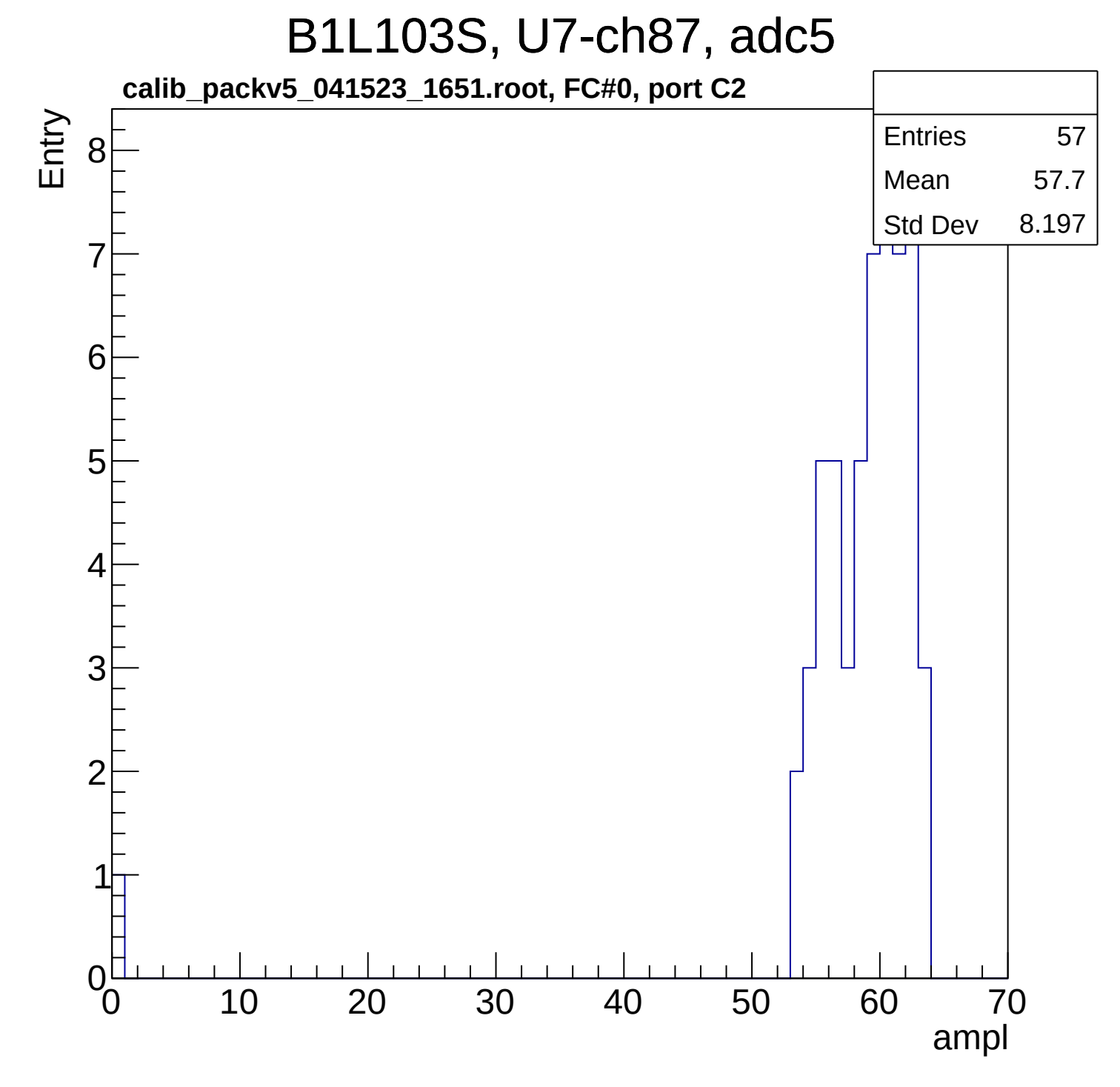
B1L103S, U7-ch87, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 57.7
Std Dev 8.197
Entry
ampl
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3
4
5
6
7
8
0
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20
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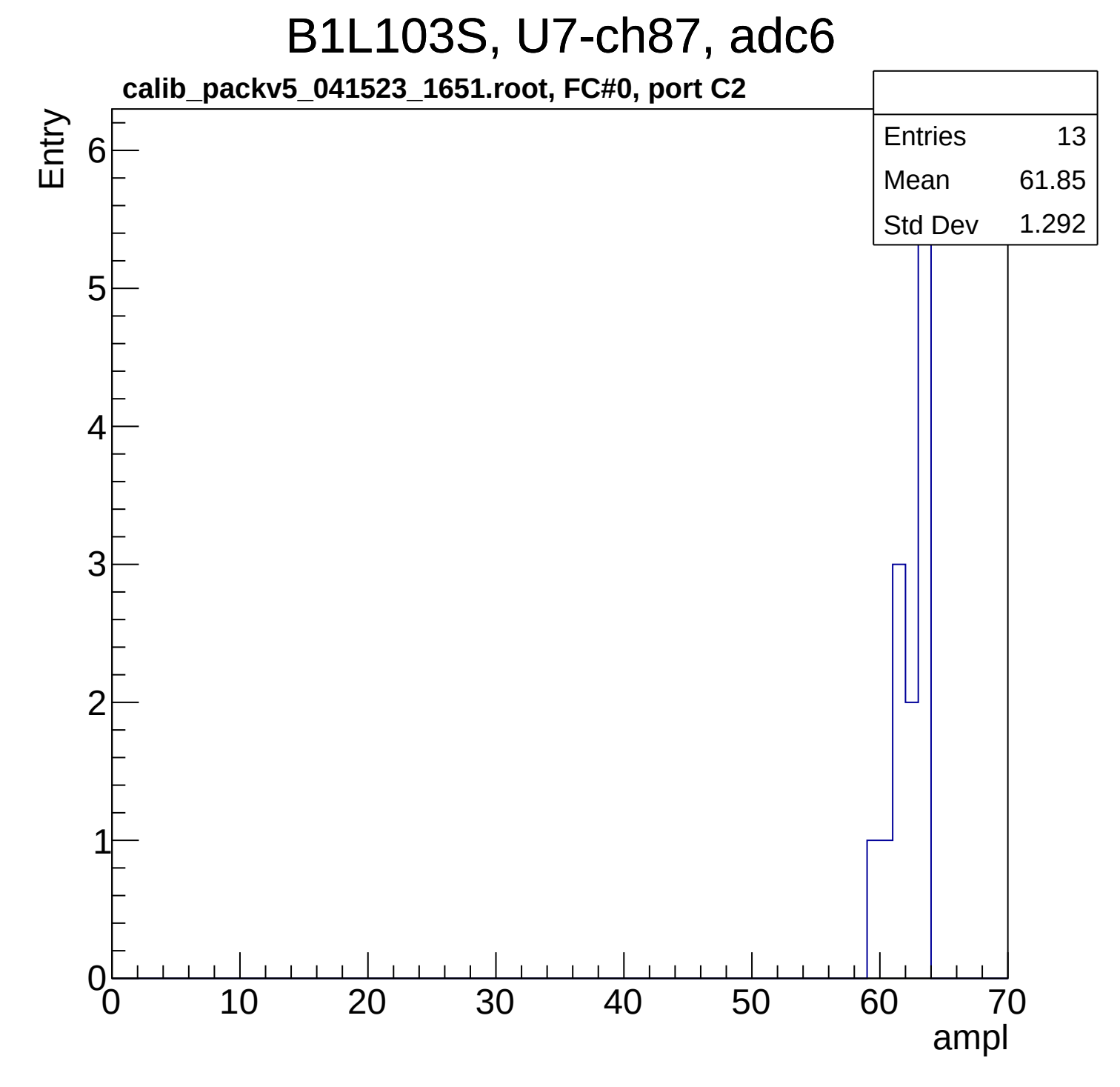
B1L103S, U7-ch87, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 13
Mean 61.85
Std Dev 1.292
Entry
ampl
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1
2
3
4
5
6
0
10
20
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40
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60
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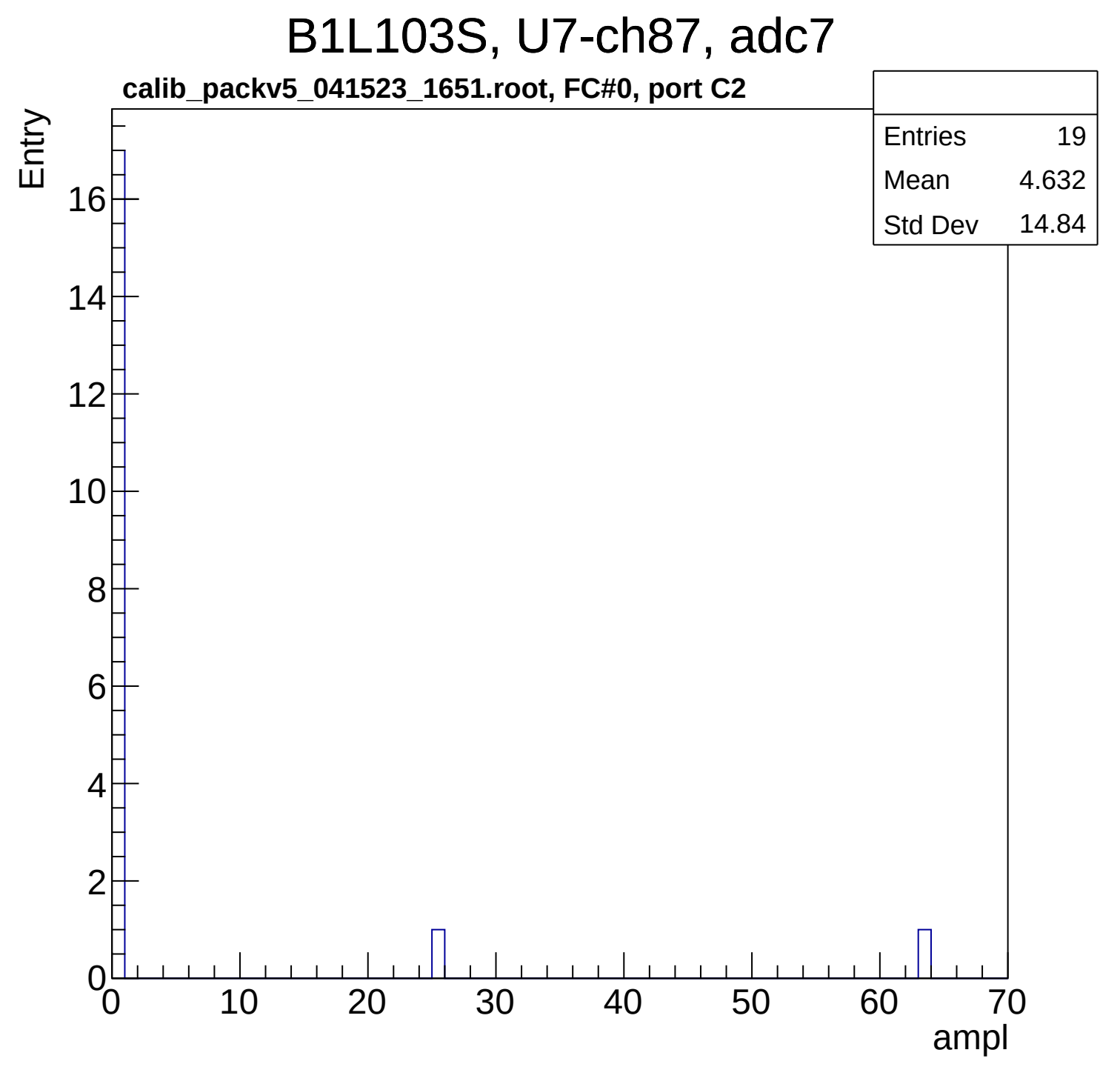
B1L103S, U7-ch87, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 4.632
Std Dev 14.84
Entry
ampl
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4
6
8
10
12
14
16
0
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20
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40
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60
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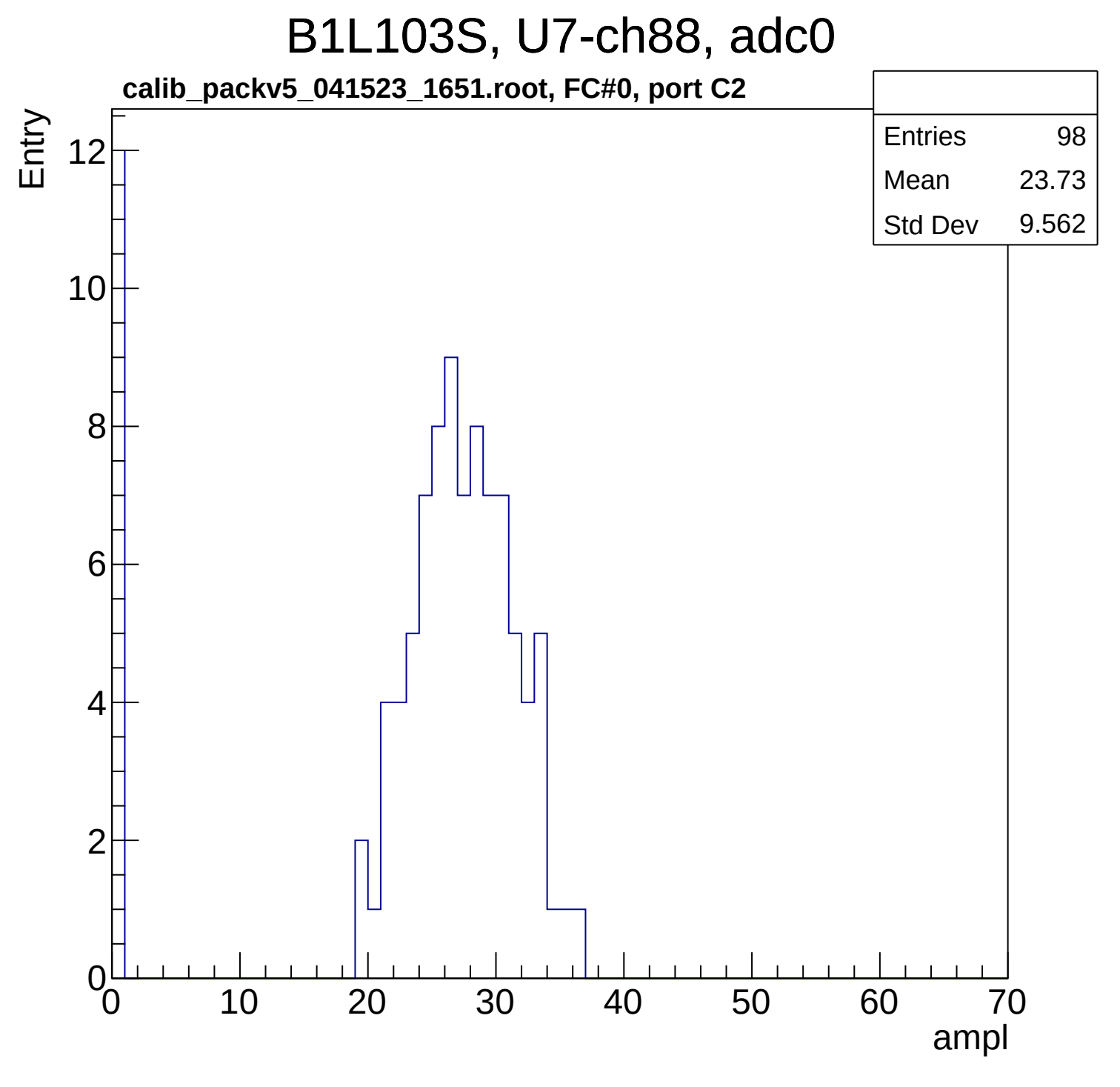
B1L103S, U7-ch88, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 98
Mean 23.73
Std Dev 9.562
Entry
0
2
4
6
8
10
12
0
10
20
30
40
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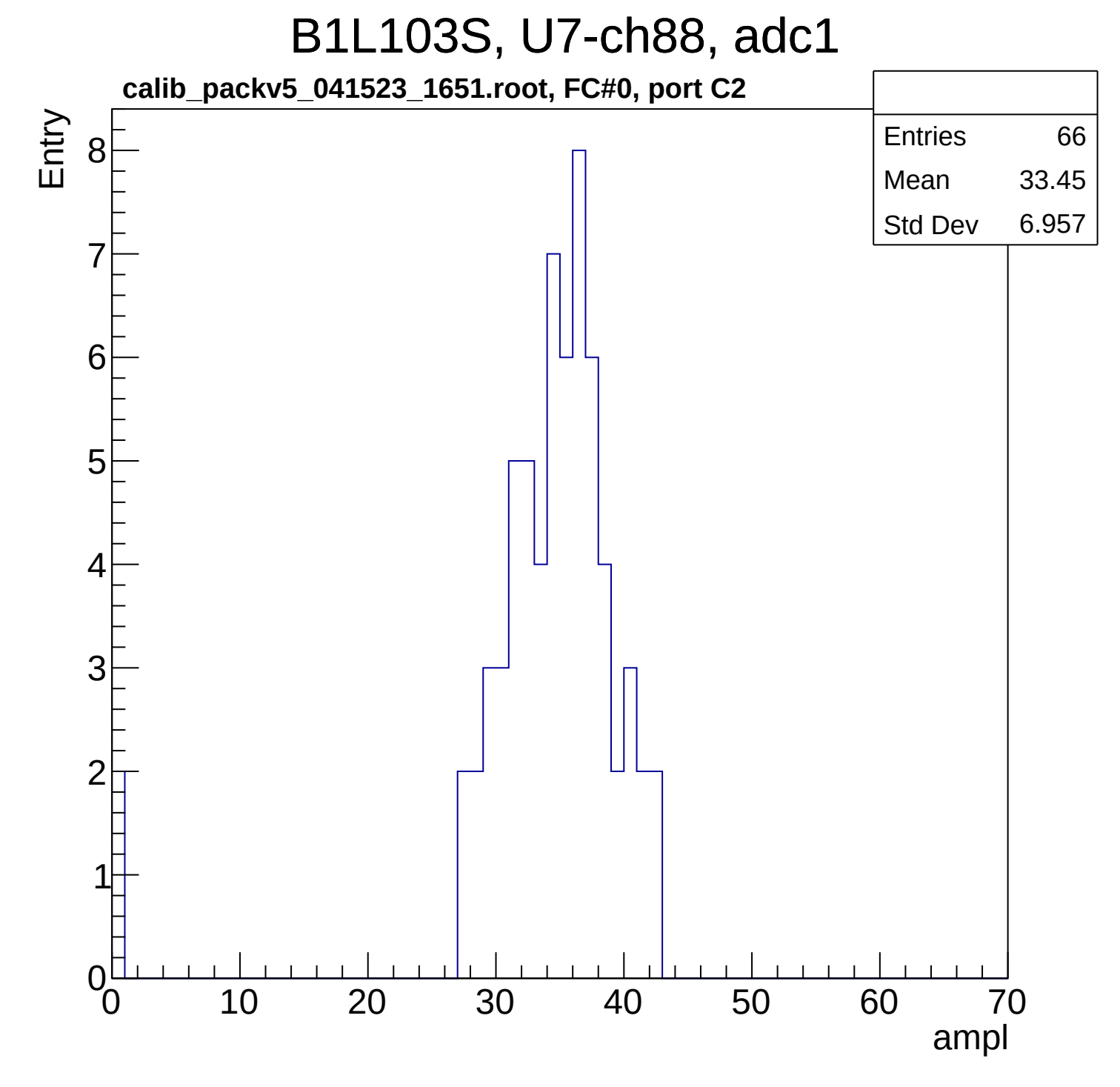
60
70
ampl


B1L103S, U7-ch88, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 33.45
Std Dev 6.957
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
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40
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60
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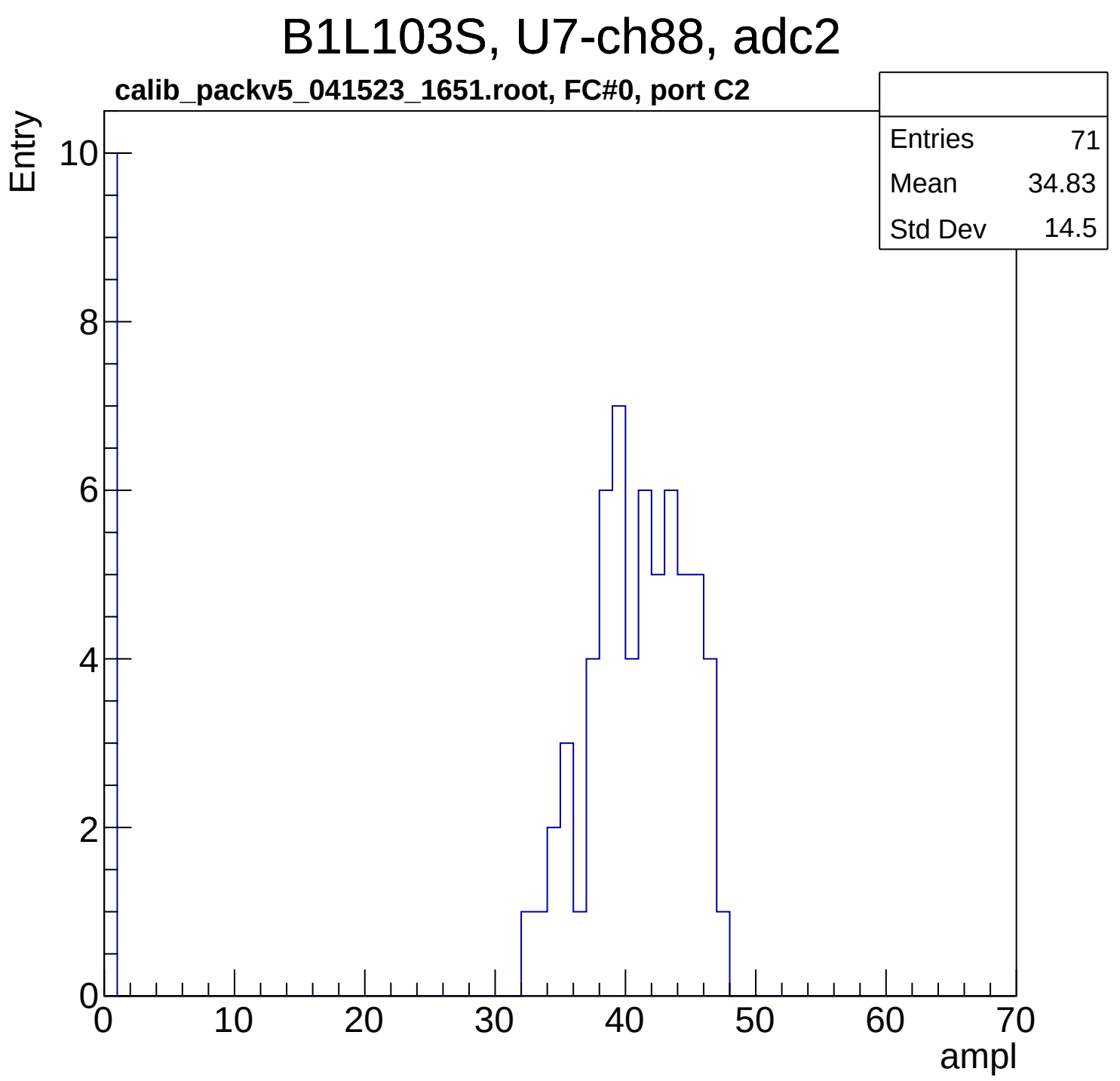
B1L103S, U7-ch88, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 34.83
Std Dev 14.5
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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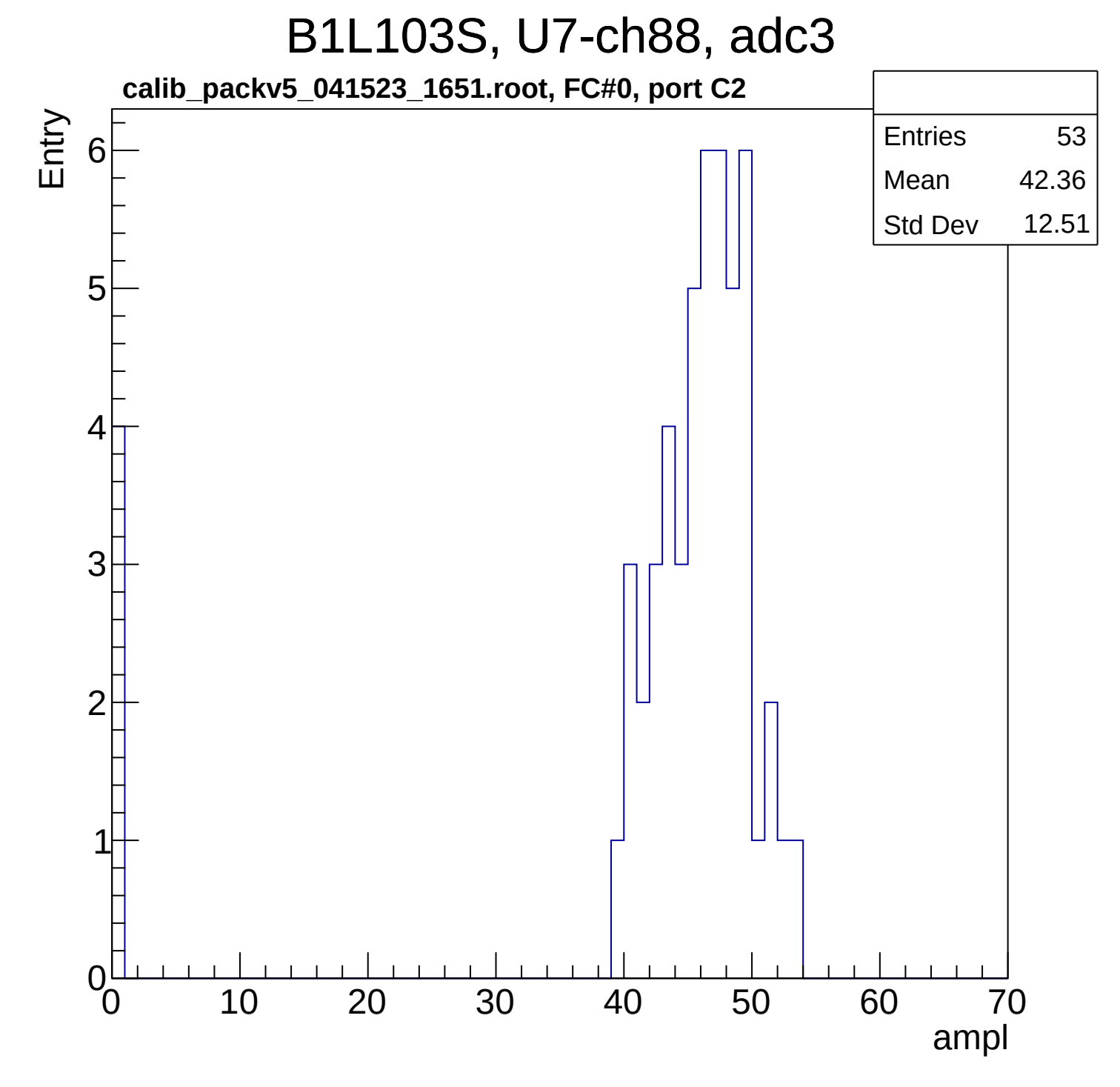
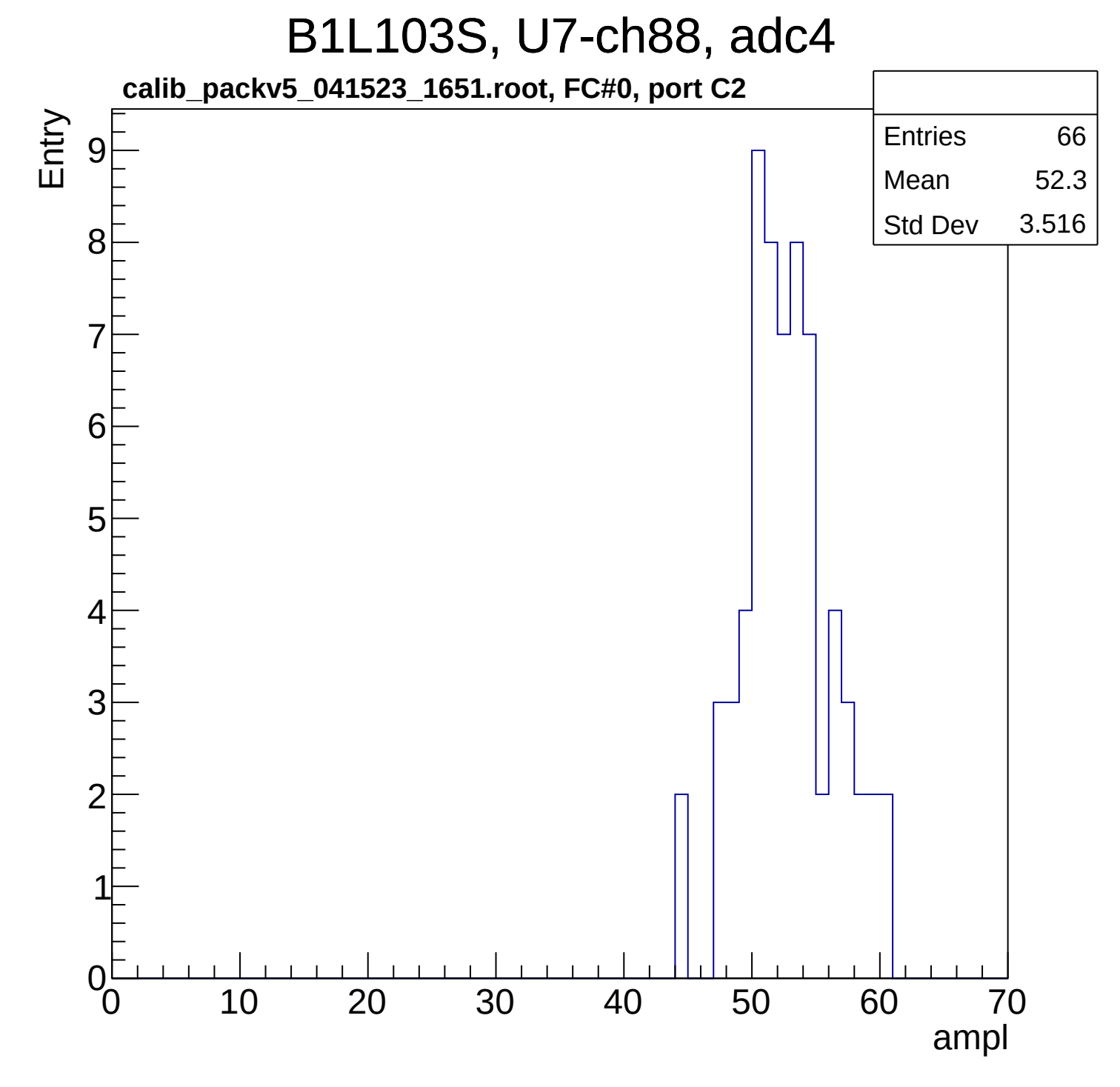

B1L103S, U7-ch88, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 42.36
Std Dev 12.51
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch88, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 52.3
Std Dev 3.516
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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60
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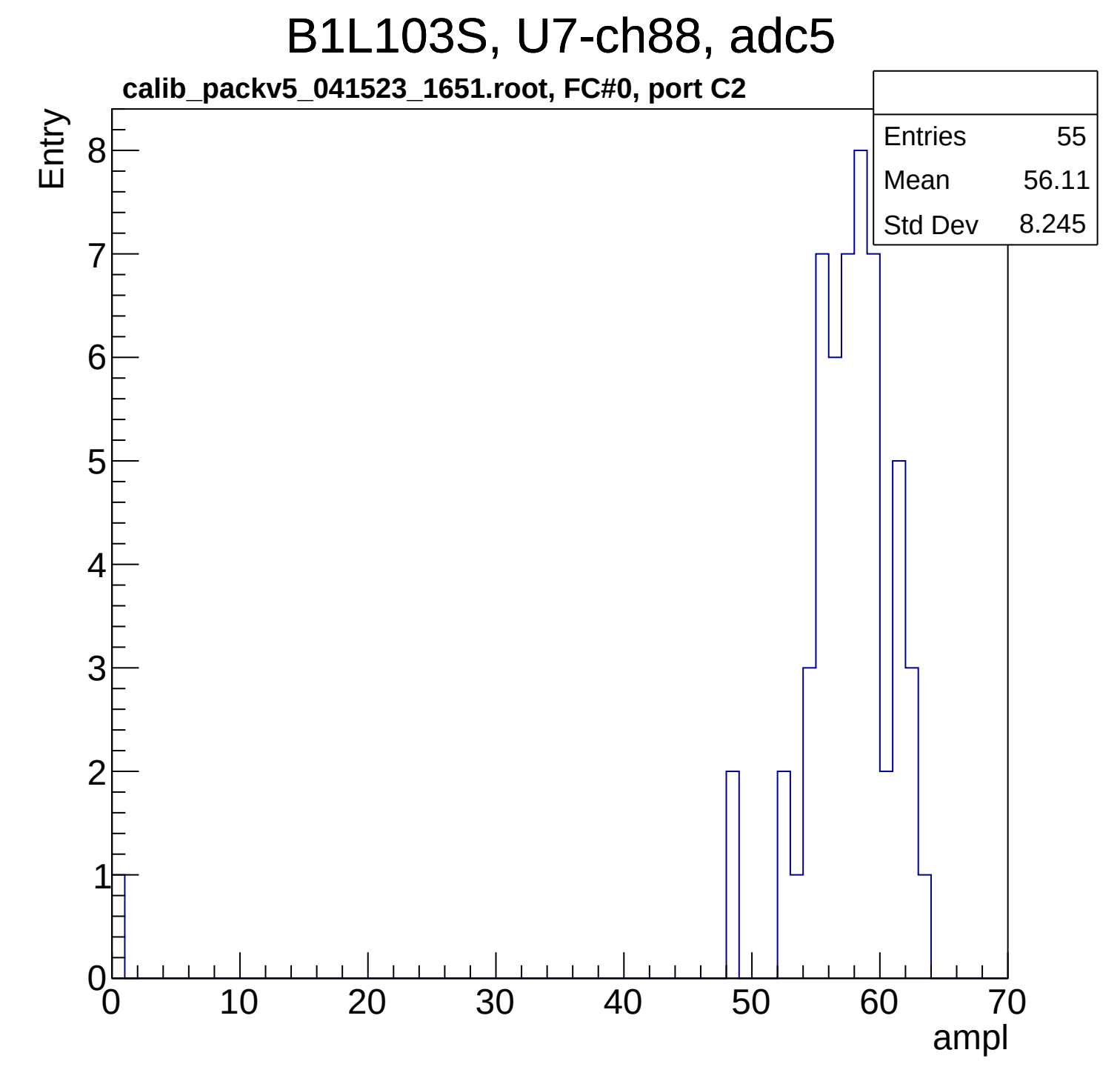
B1L103S, U7-ch88, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 56.11
Std Dev 8.245
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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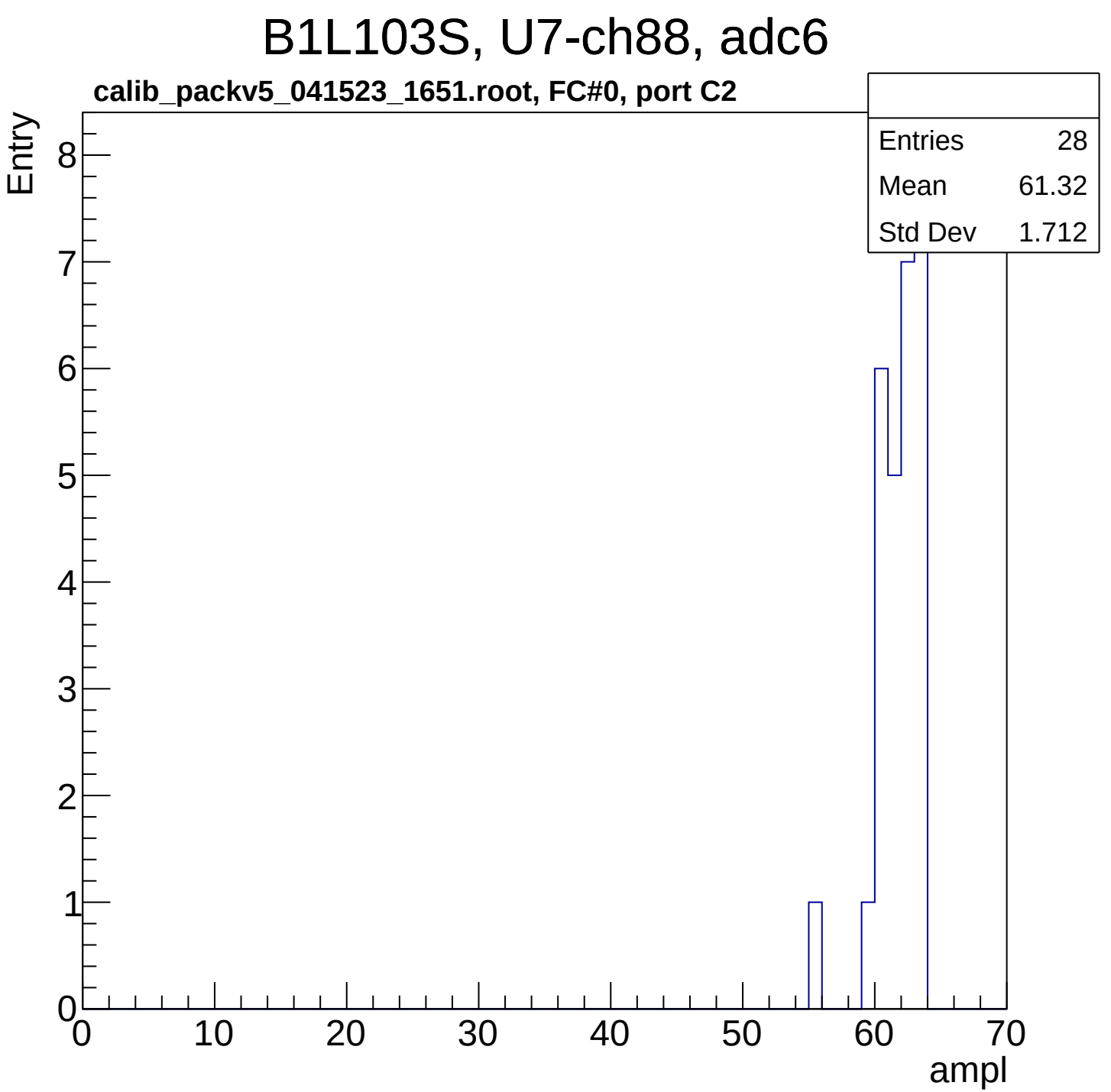
B1L103S, U7-ch88, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 28
Mean 61.32
Std Dev 1.712
Entry
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2
3
4
5
6
7
8
0
10
20
30
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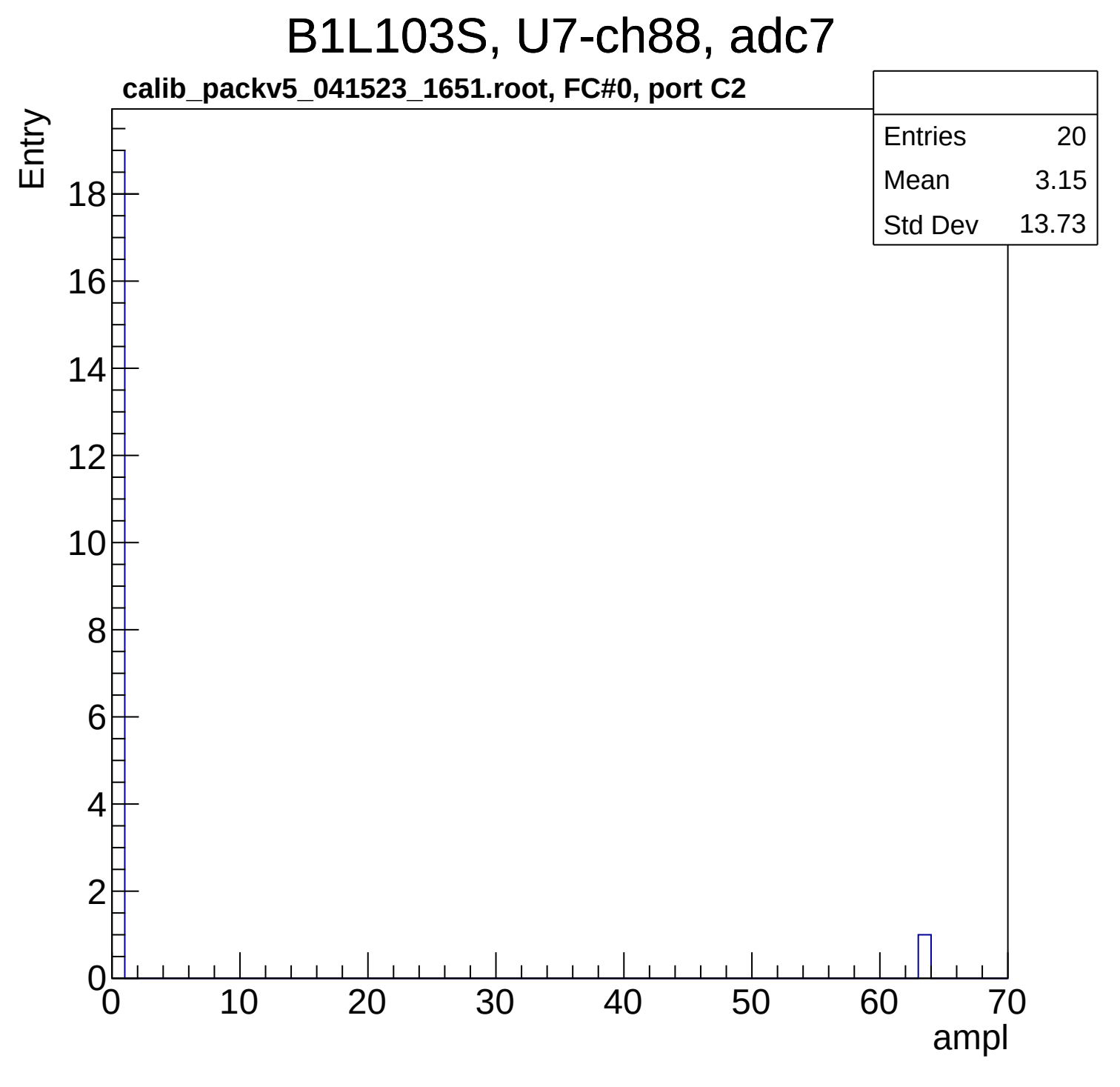
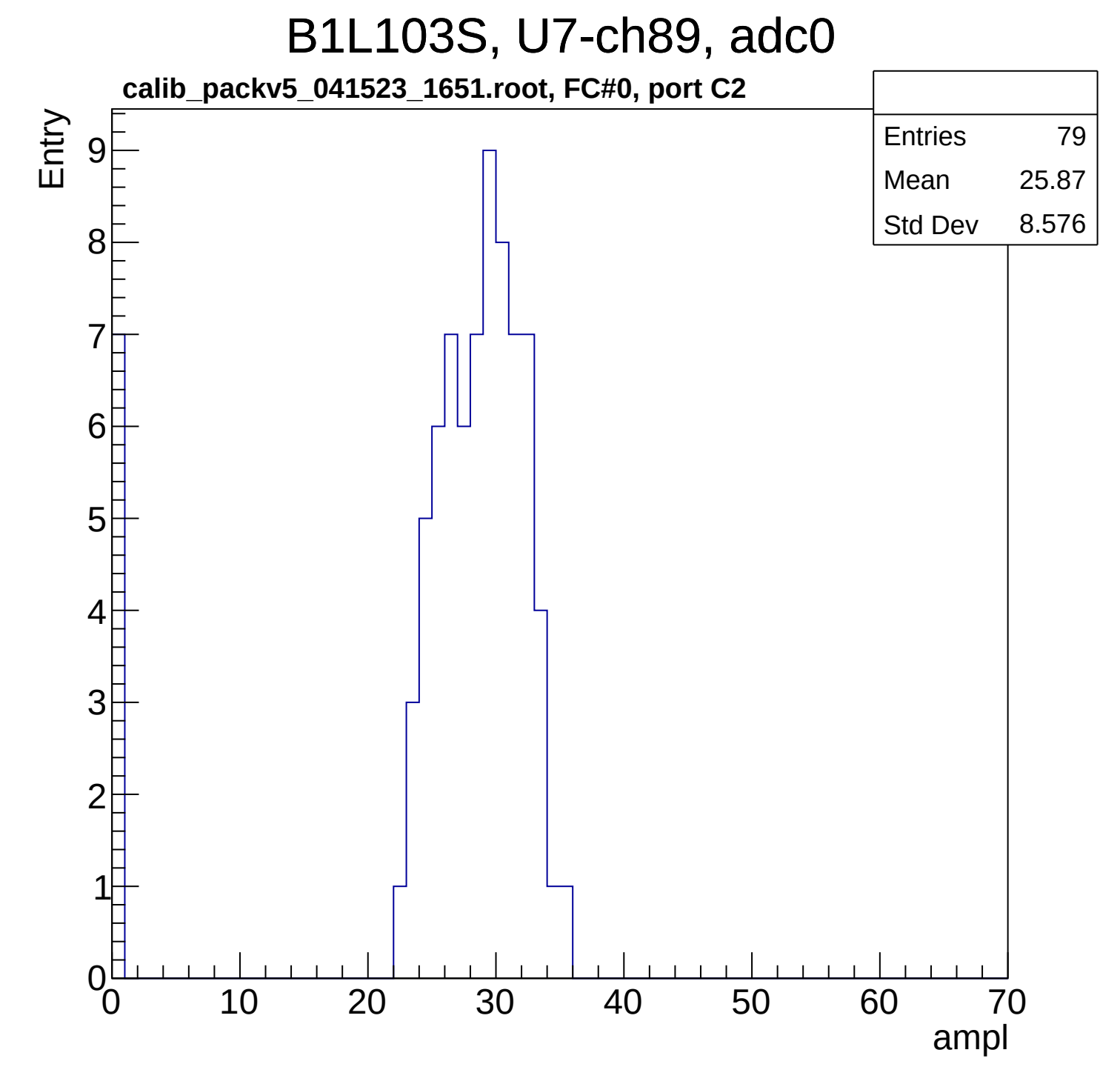
50
60
70
ampl


B1L103S, U7-ch88, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch89, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 25.87
Std Dev 8.576
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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60
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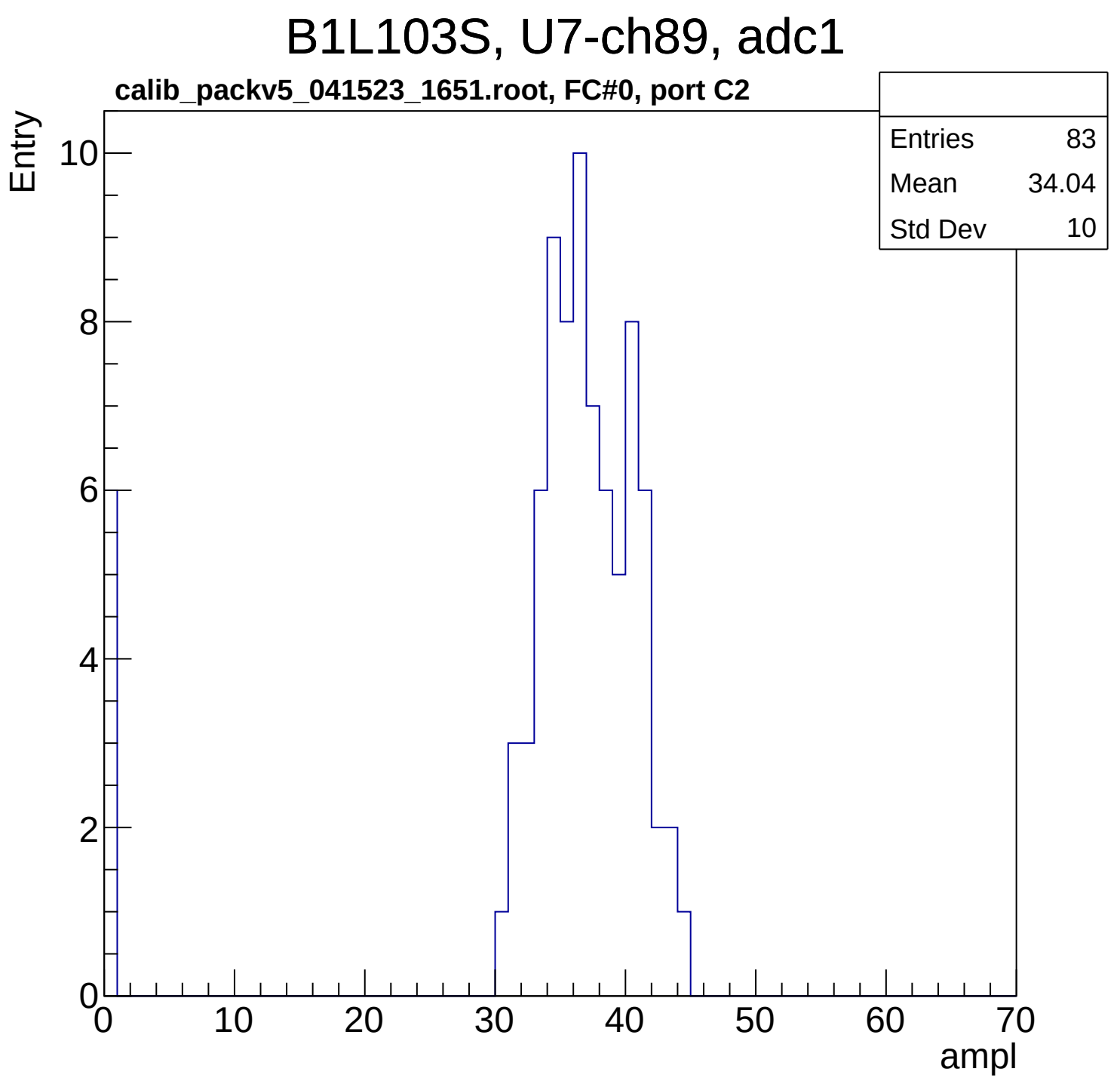
B1L103S, U7-ch89, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 34.04
Std Dev 10
Entry
ampl
0
2
4
6
8
10
0
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30
40
50
60
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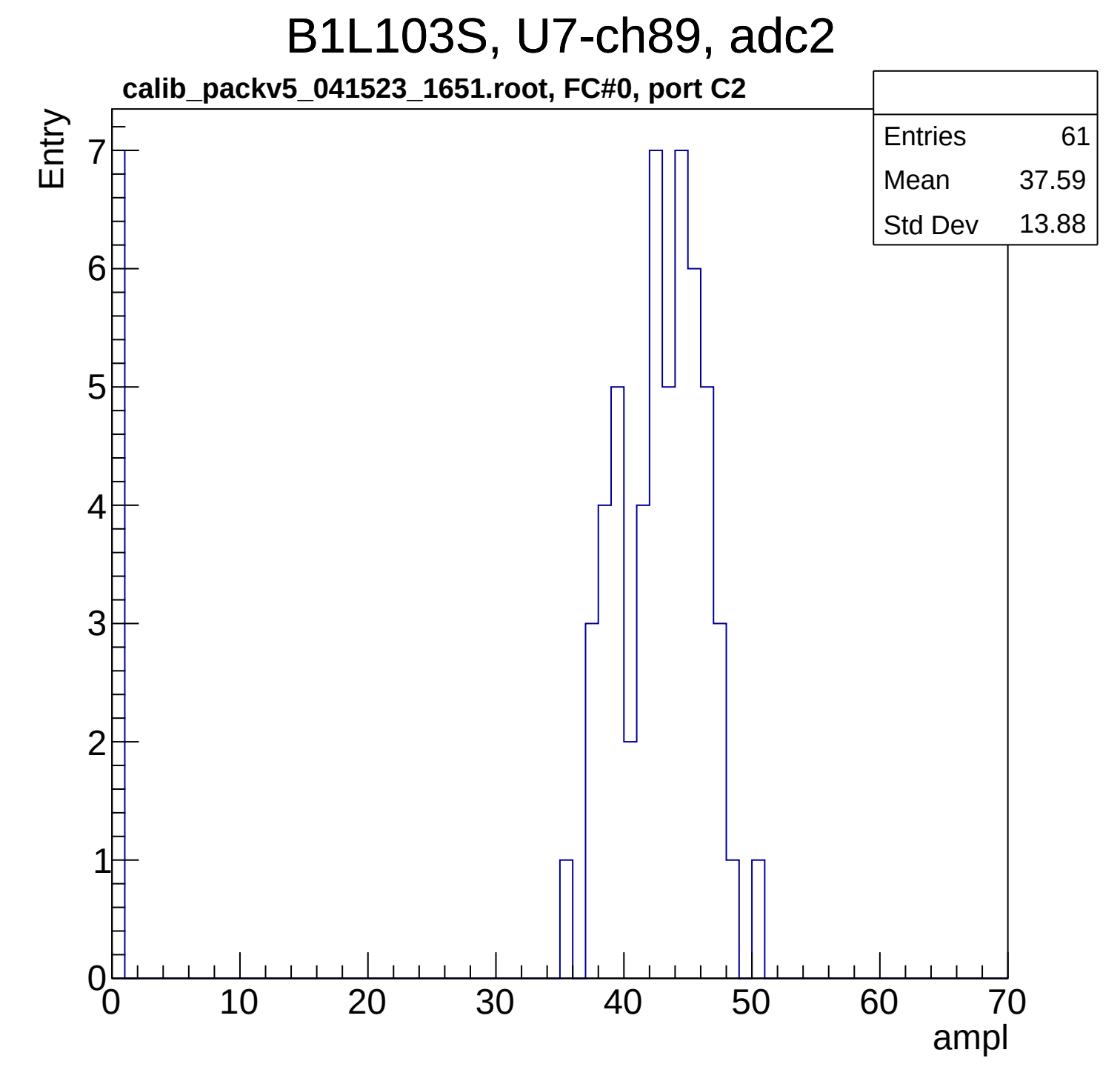
B1L103S, U7-ch89, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 37.59
Std Dev 13.88
Entry
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1
2
3
4
5
6
7
0
10
20
30
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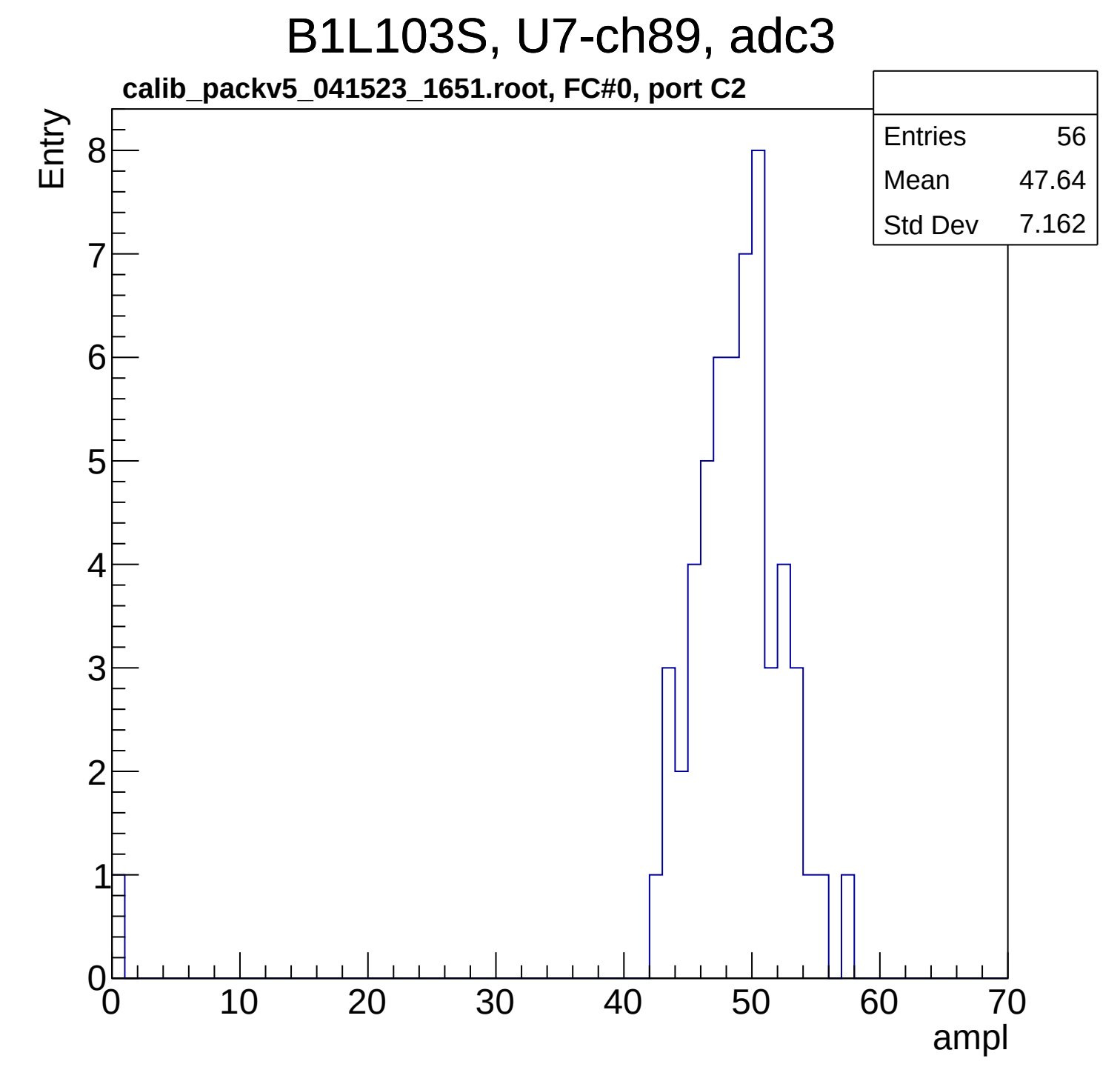
50
60
70
ampl


B1L103S, U7-ch89, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 47.64
Std Dev 7.162
Entry
ampl
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2
3
4
5
6
7
8
0
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40
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60
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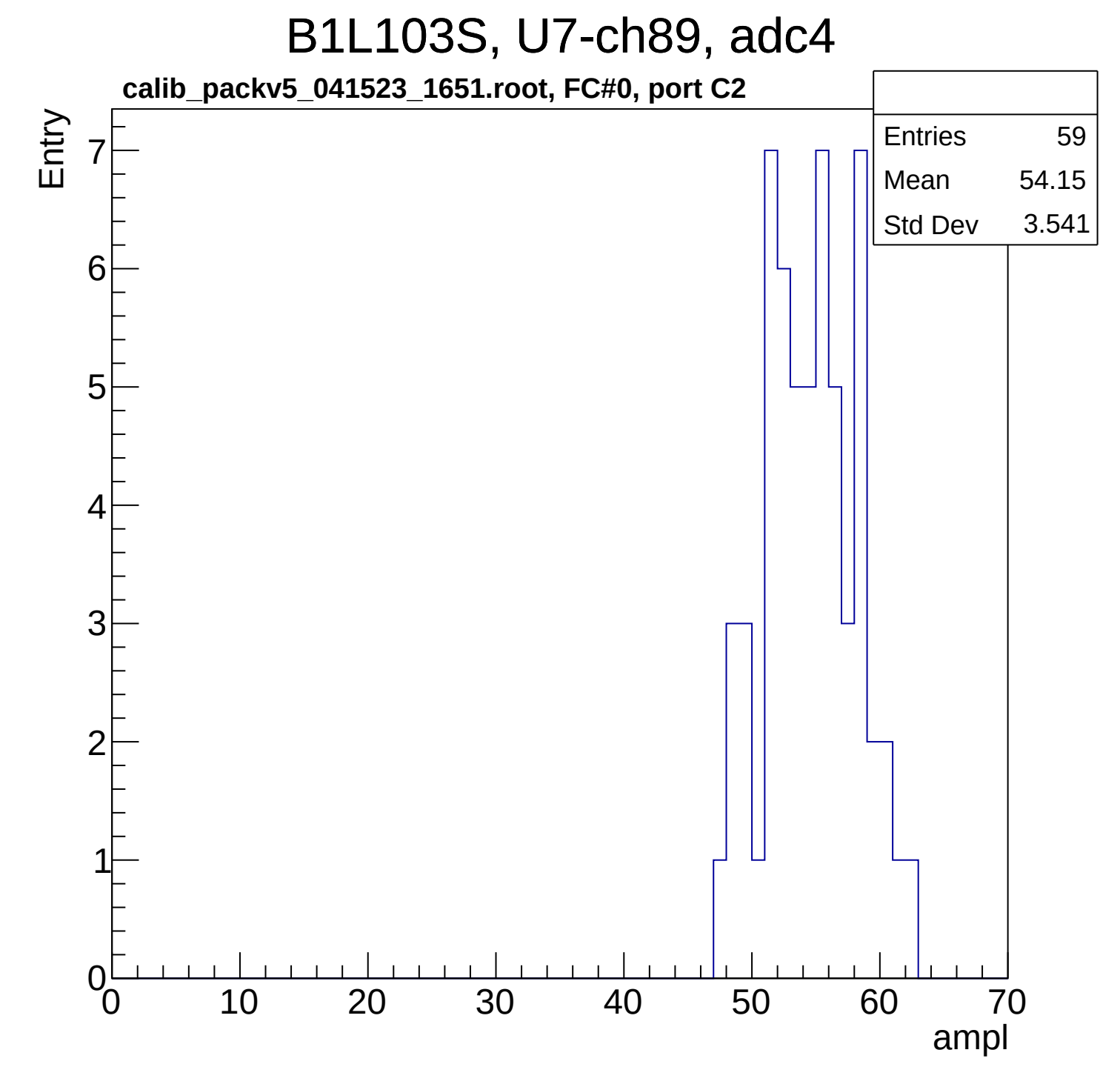
B1L103S, U7-ch89, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 54.15
Std Dev 3.541
Entry
ampl
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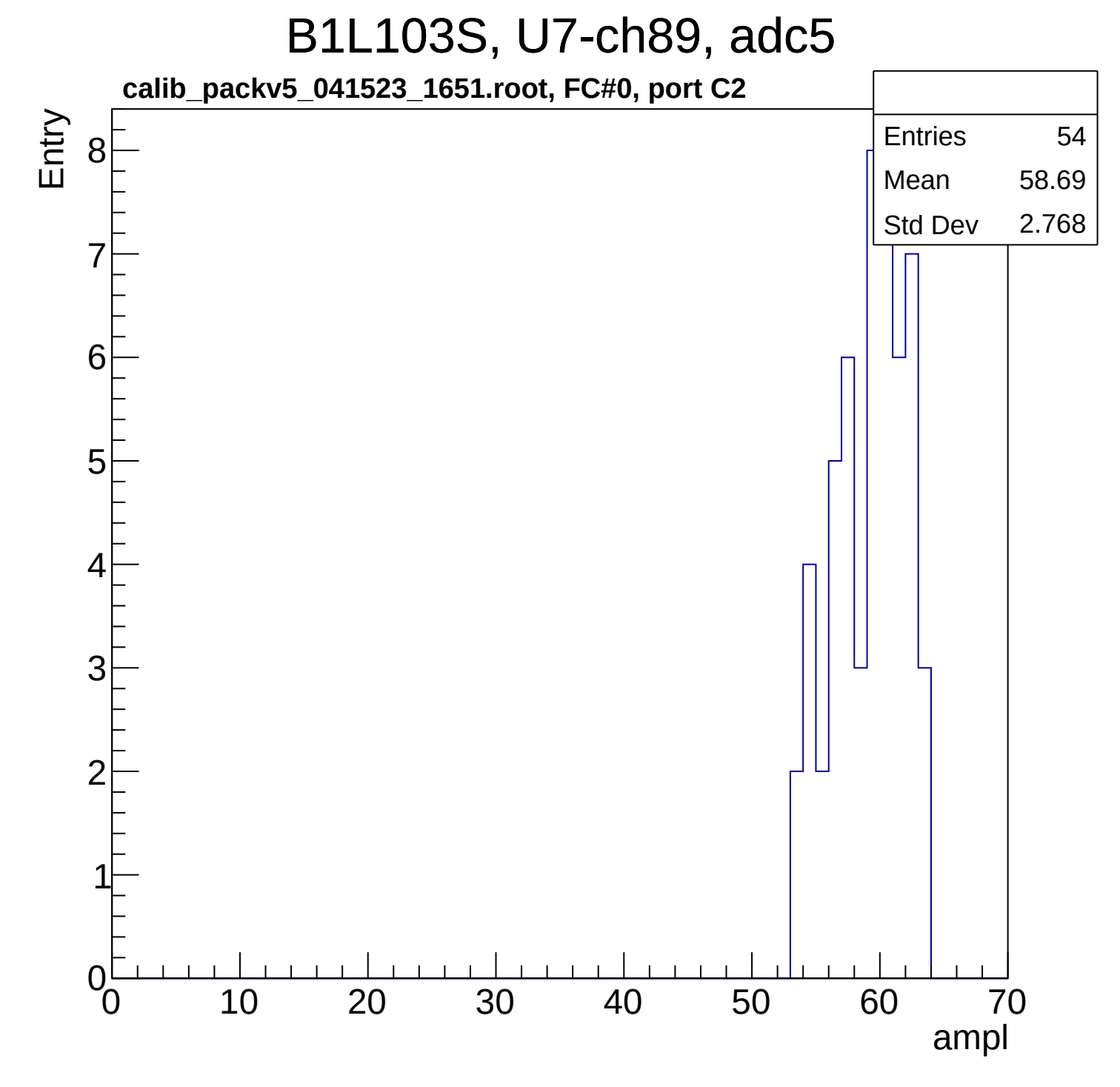
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U7-ch89, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 58.69
Std Dev 2.768
Entry
ampl
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1
2
3
4
5
6
7
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0
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20
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40
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60
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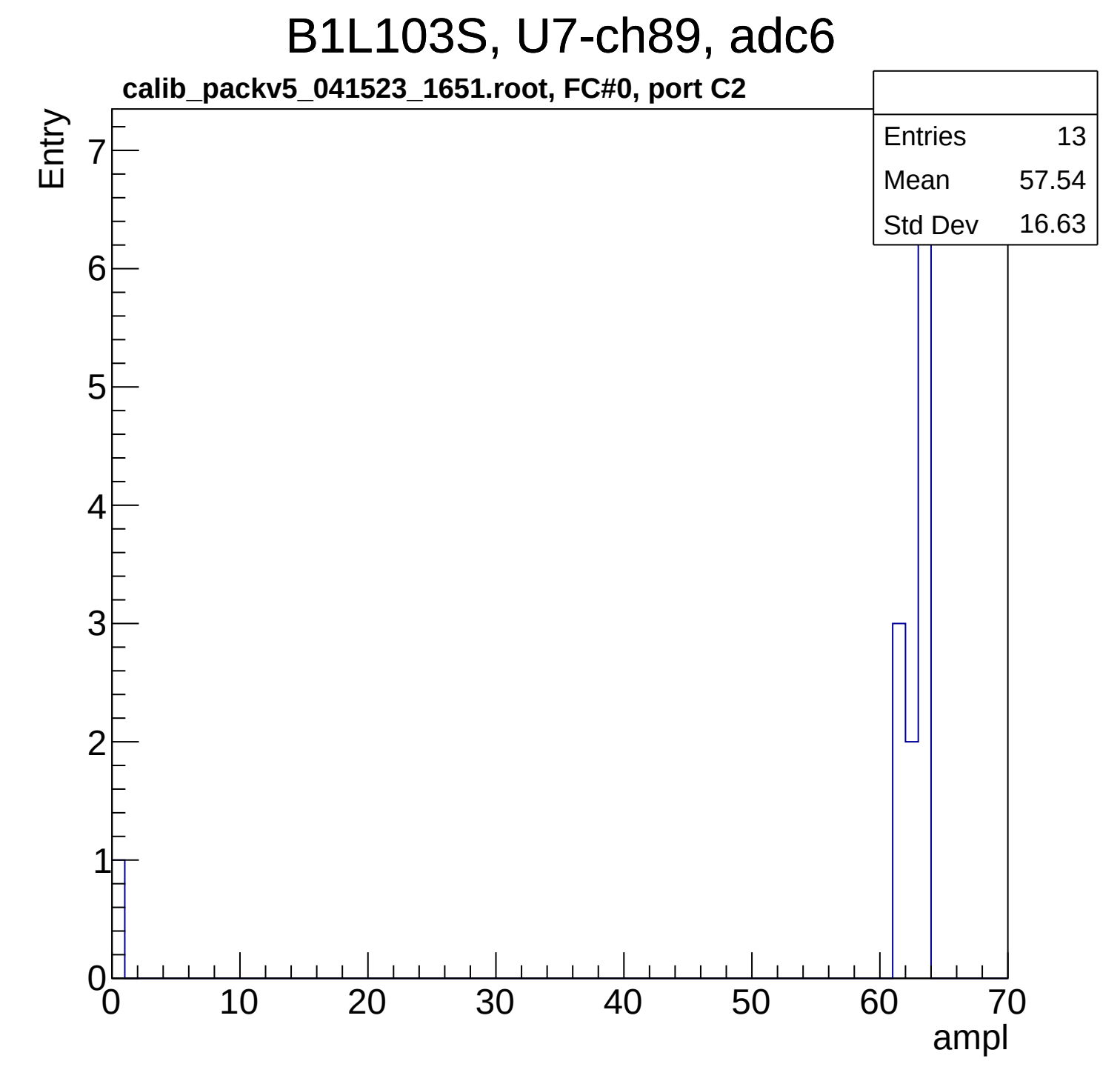
B1L103S, U7-ch89, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 13
Mean 57.54
Std Dev 16.63
Entry
ampl
0
1
2
3
4
5
6
7
0
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20
30
40
50
60
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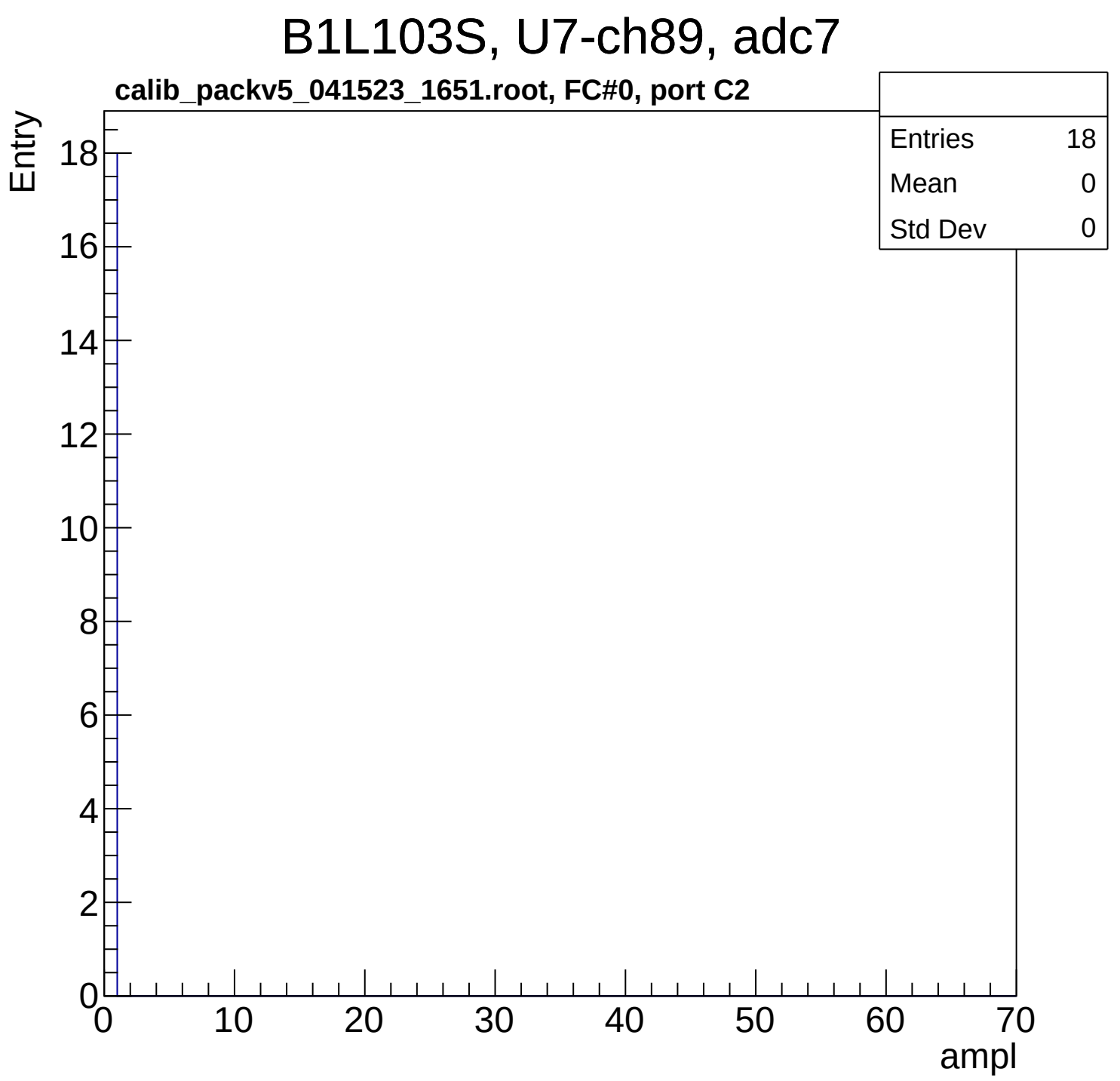
B1L103S, U7-ch89, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
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6
8
10
12
14
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10
20
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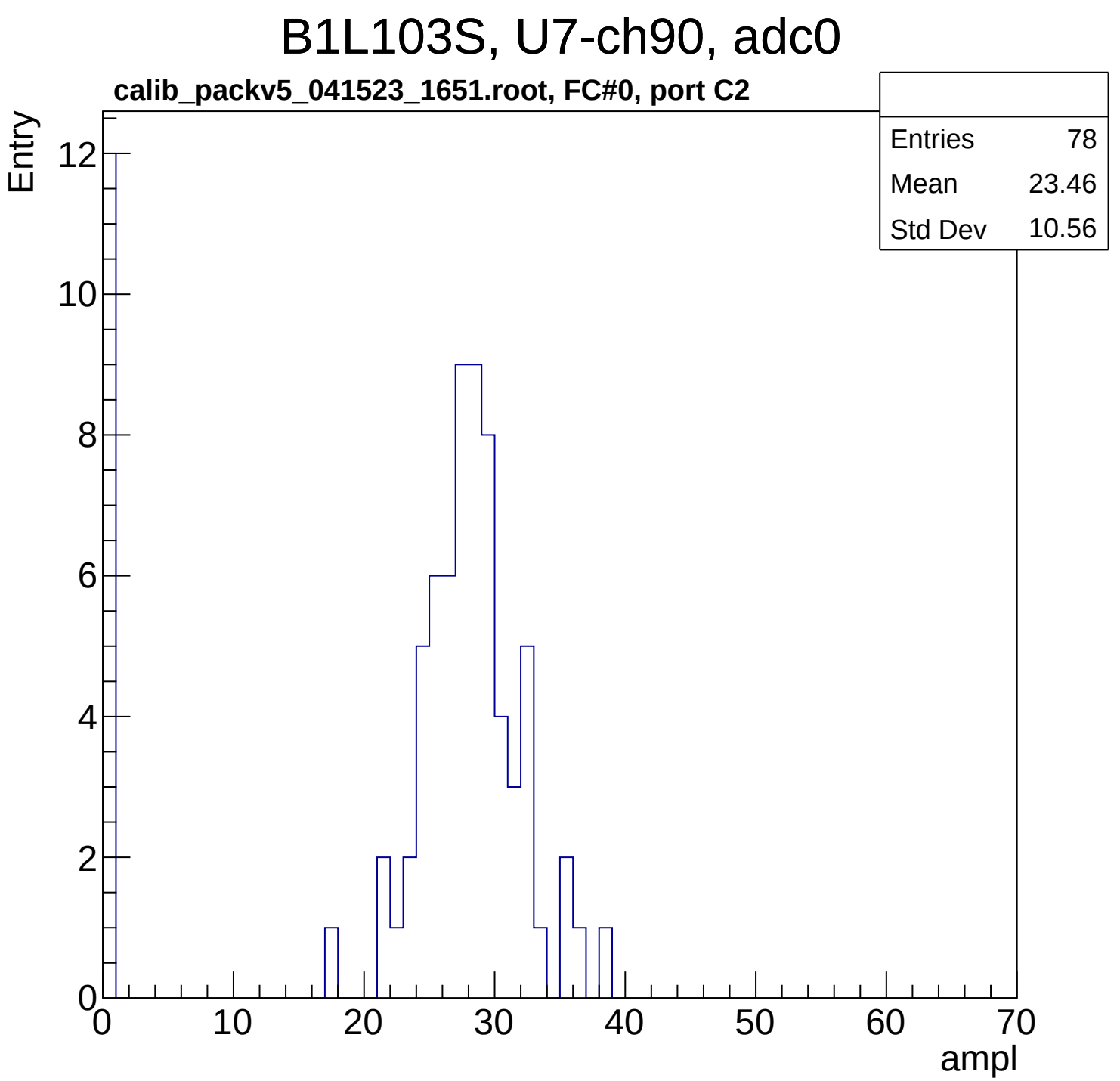
50
60
70
ampl


B1L103S, U7-ch90, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 23.46
Std Dev 10.56
Entry
0
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6
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12
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10
20
30
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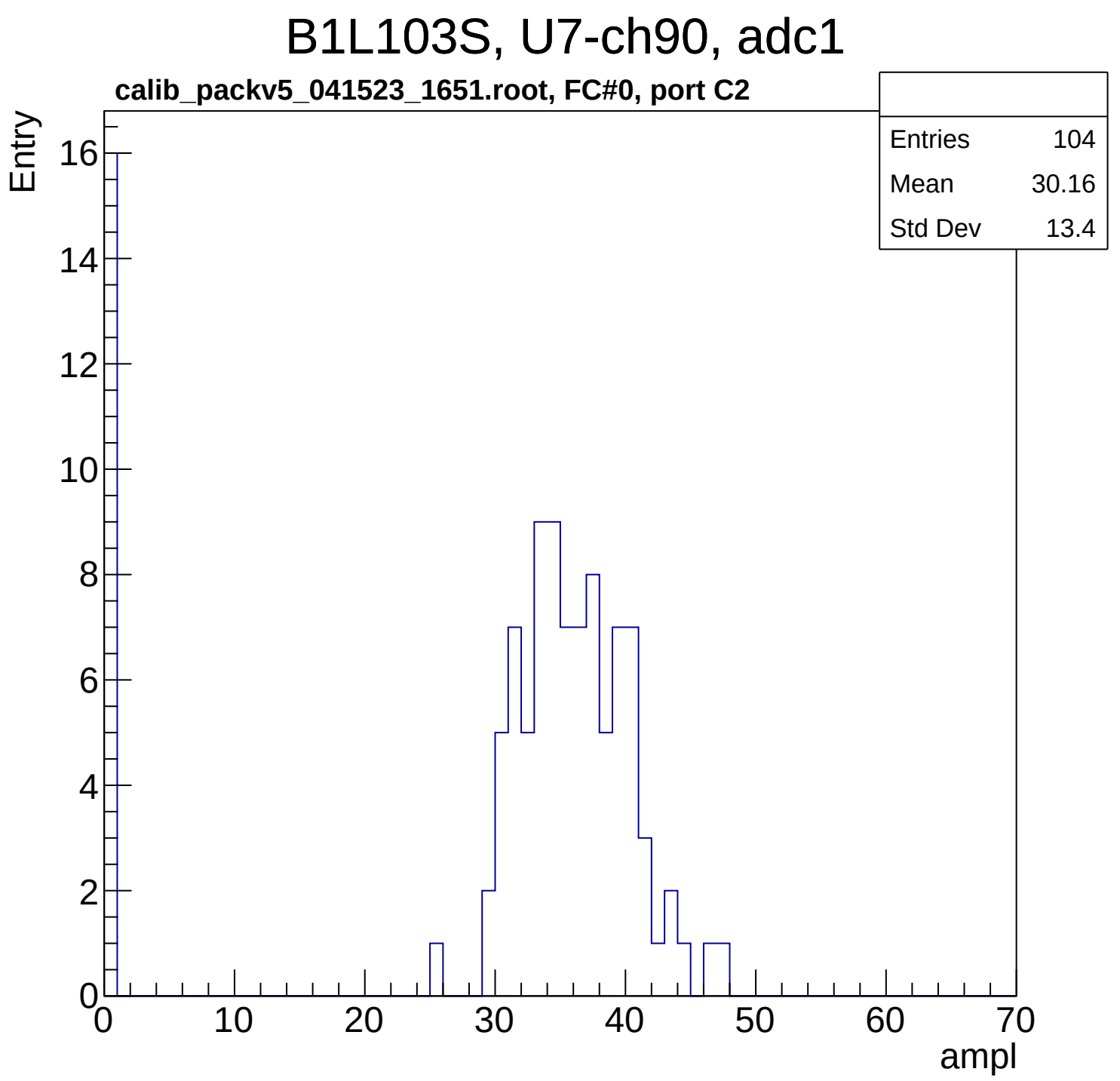
60
70
ampl


B1L103S, U7-ch90, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 104
Mean 30.16
Std Dev 13.4
Entry
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8
10
12
14
16
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20
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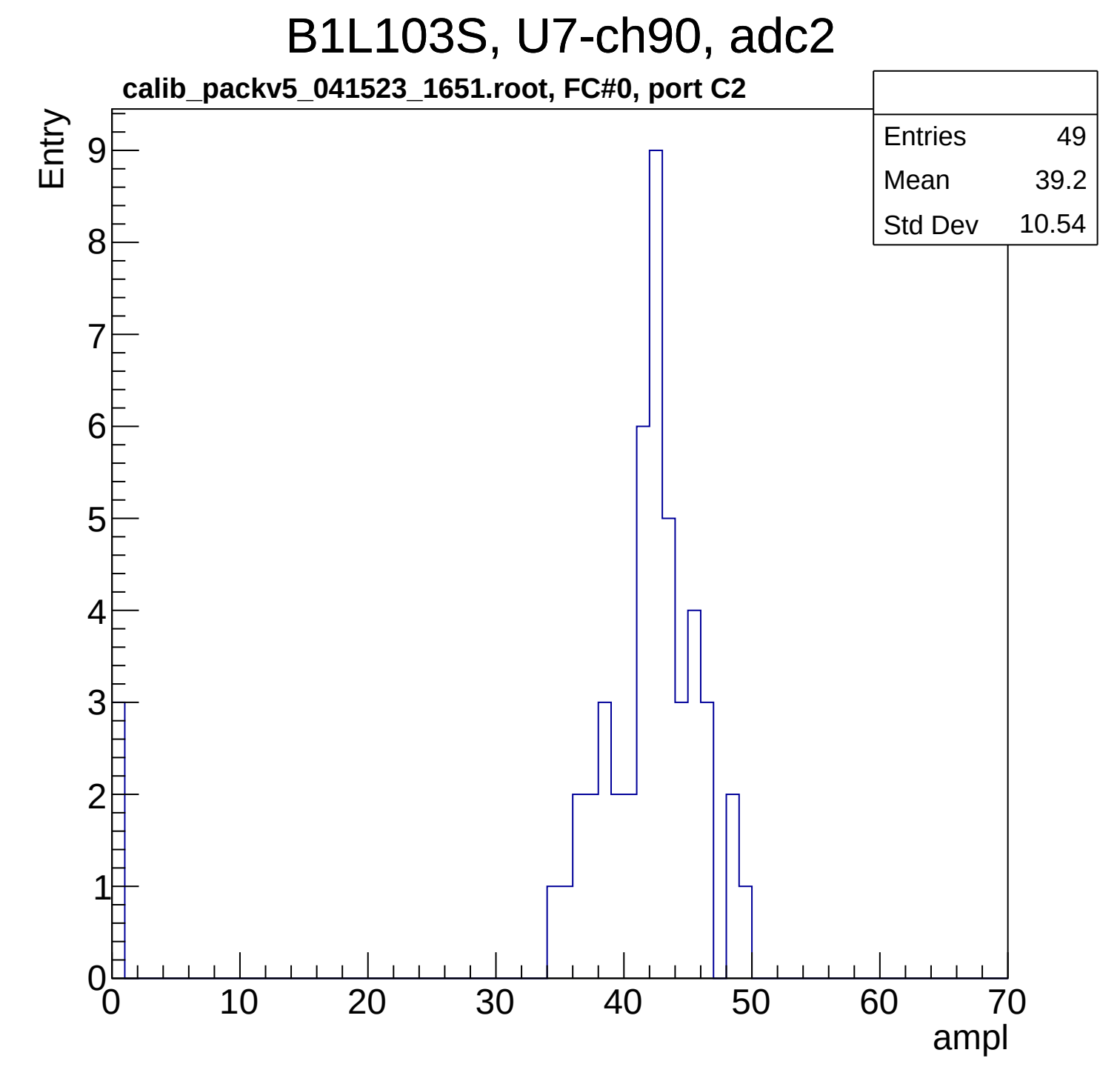
50
60
70
ampl


B1L103S, U7-ch90, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 39.2
Std Dev 10.54
Entry
ampl
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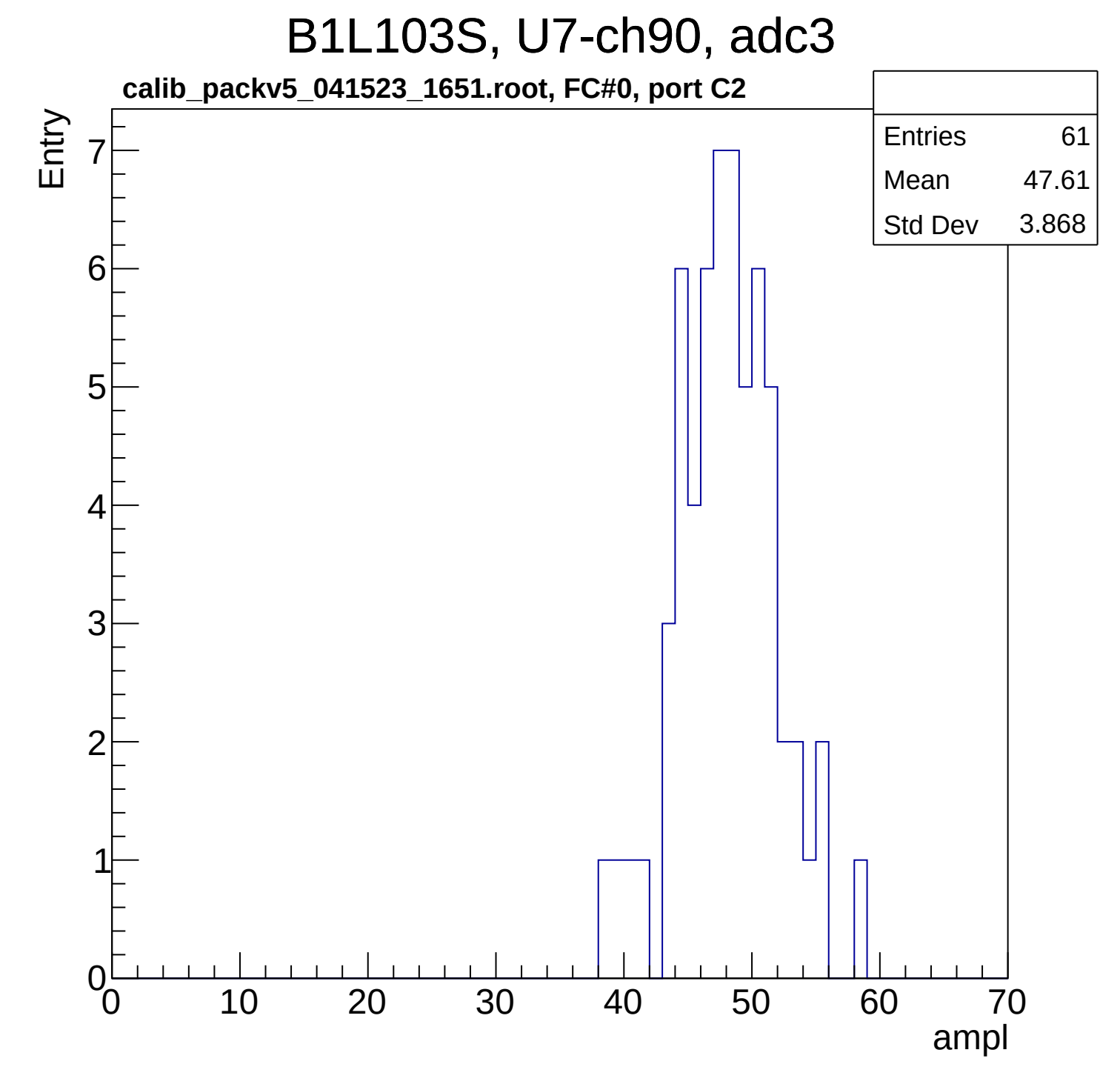
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U7-ch90, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 47.61
Std Dev 3.868
Entry
ampl
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4
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0
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20
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60
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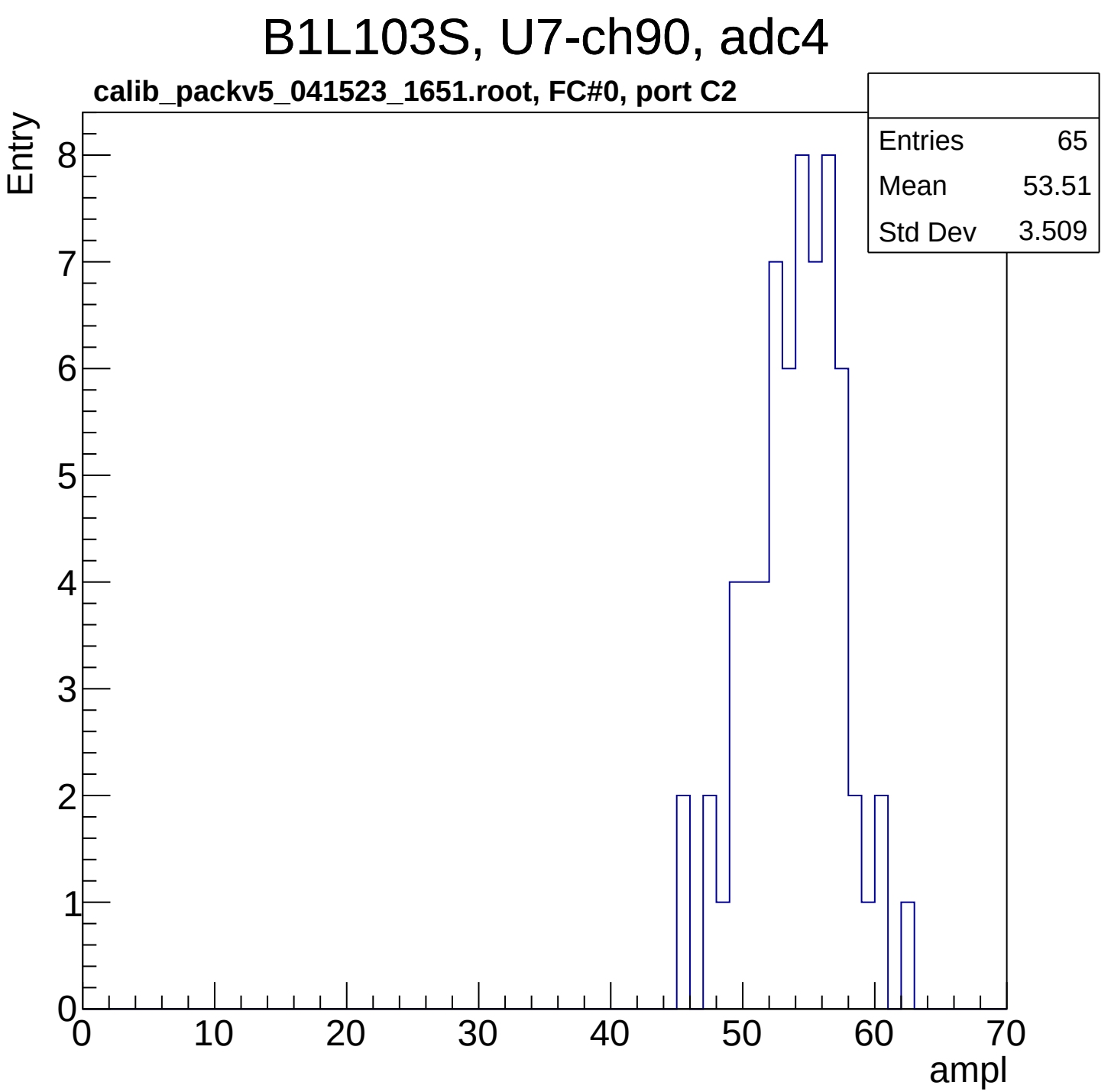
B1L103S, U7-ch90, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 53.51
Std Dev 3.509
Entry
ampl
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1
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3
4
5
6
7
8
0
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40
50
60
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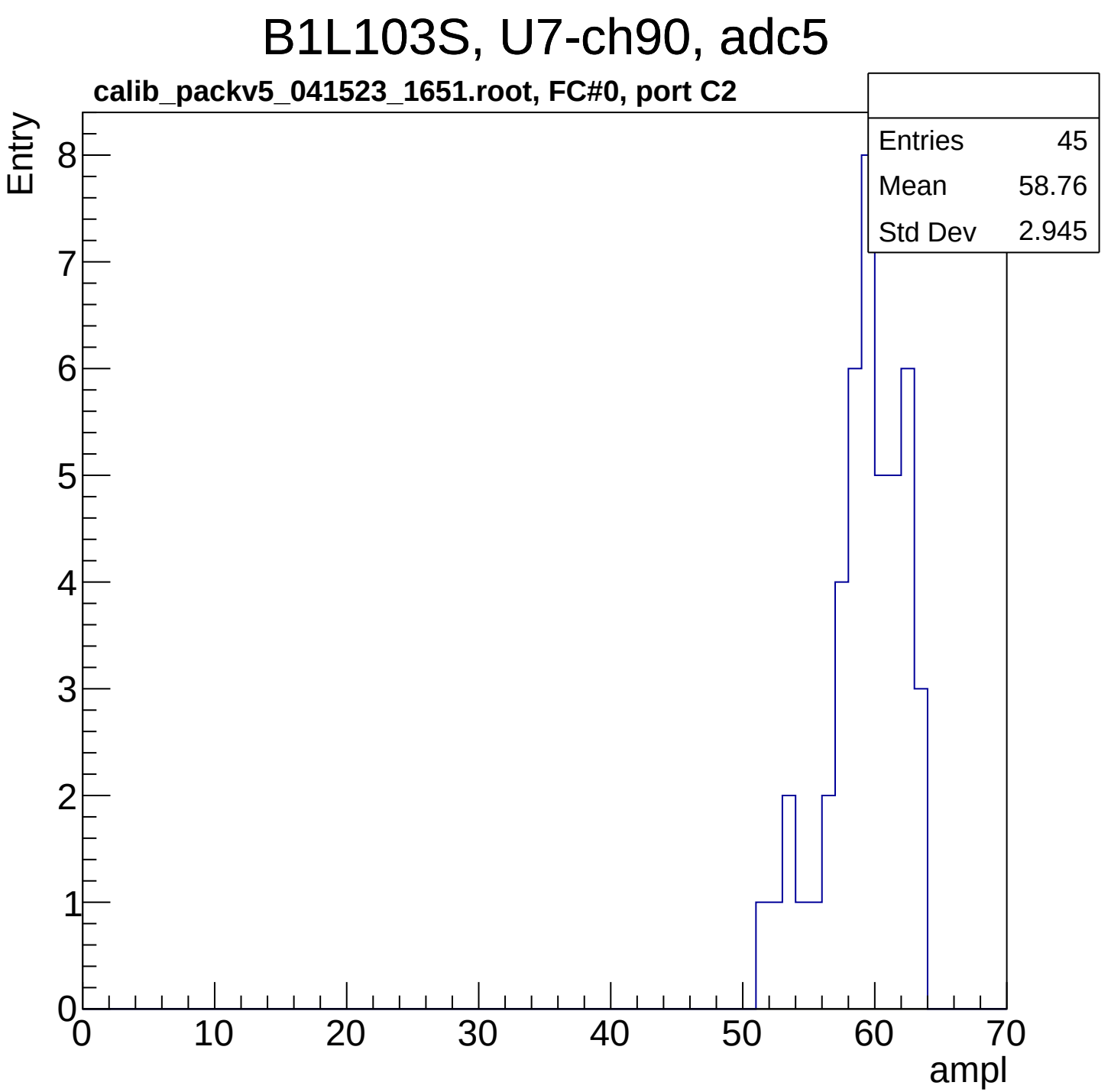
B1L103S, U7-ch90, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 58.76
Std Dev 2.945
Entry
ampl
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2
3
4
5
6
7
8
0
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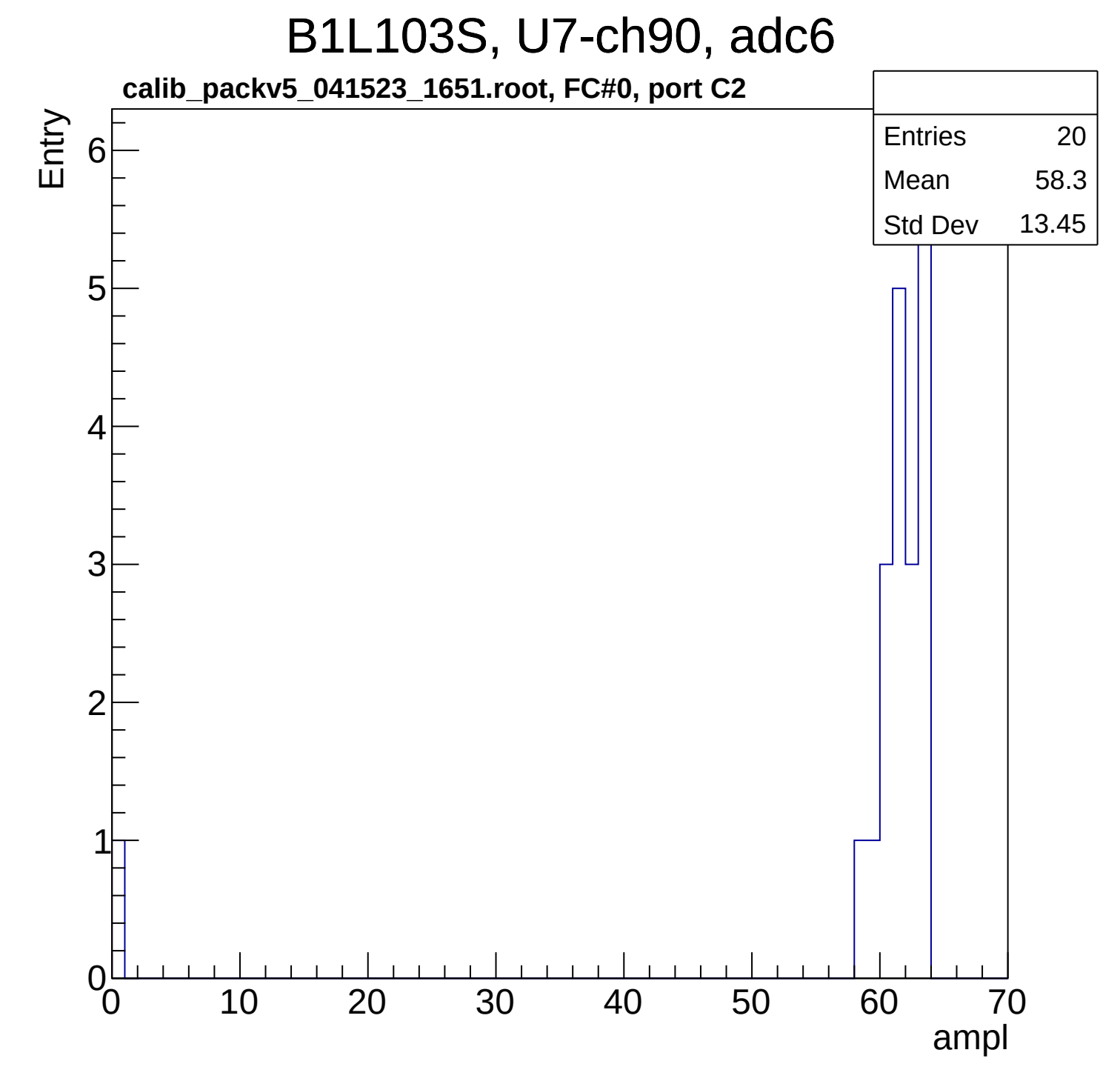
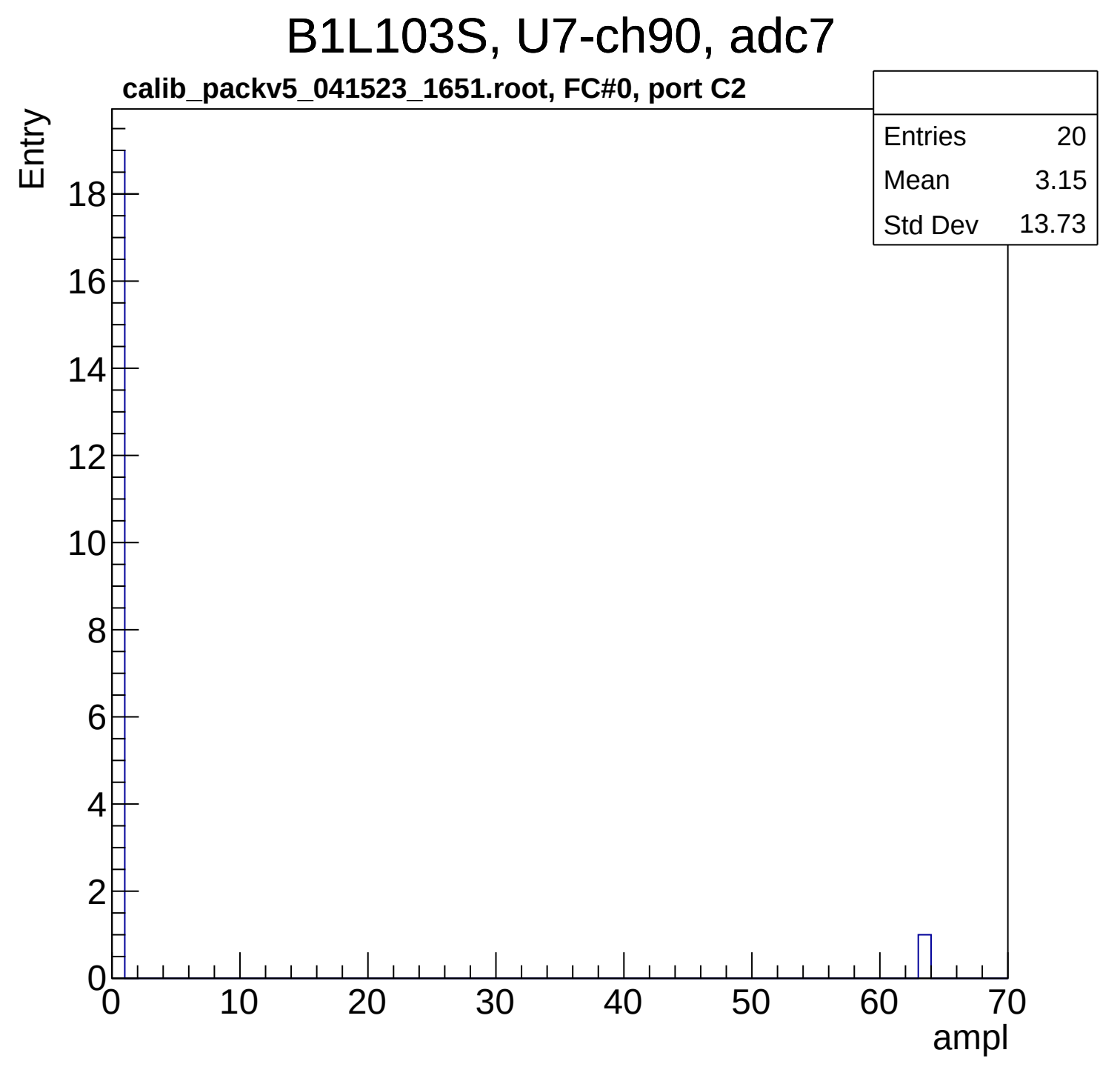

B1L103S, U7-ch90, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 58.3
Std Dev 13.45
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch90, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
0
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4
6
8
10
12
14
16
18
0
10
20
30
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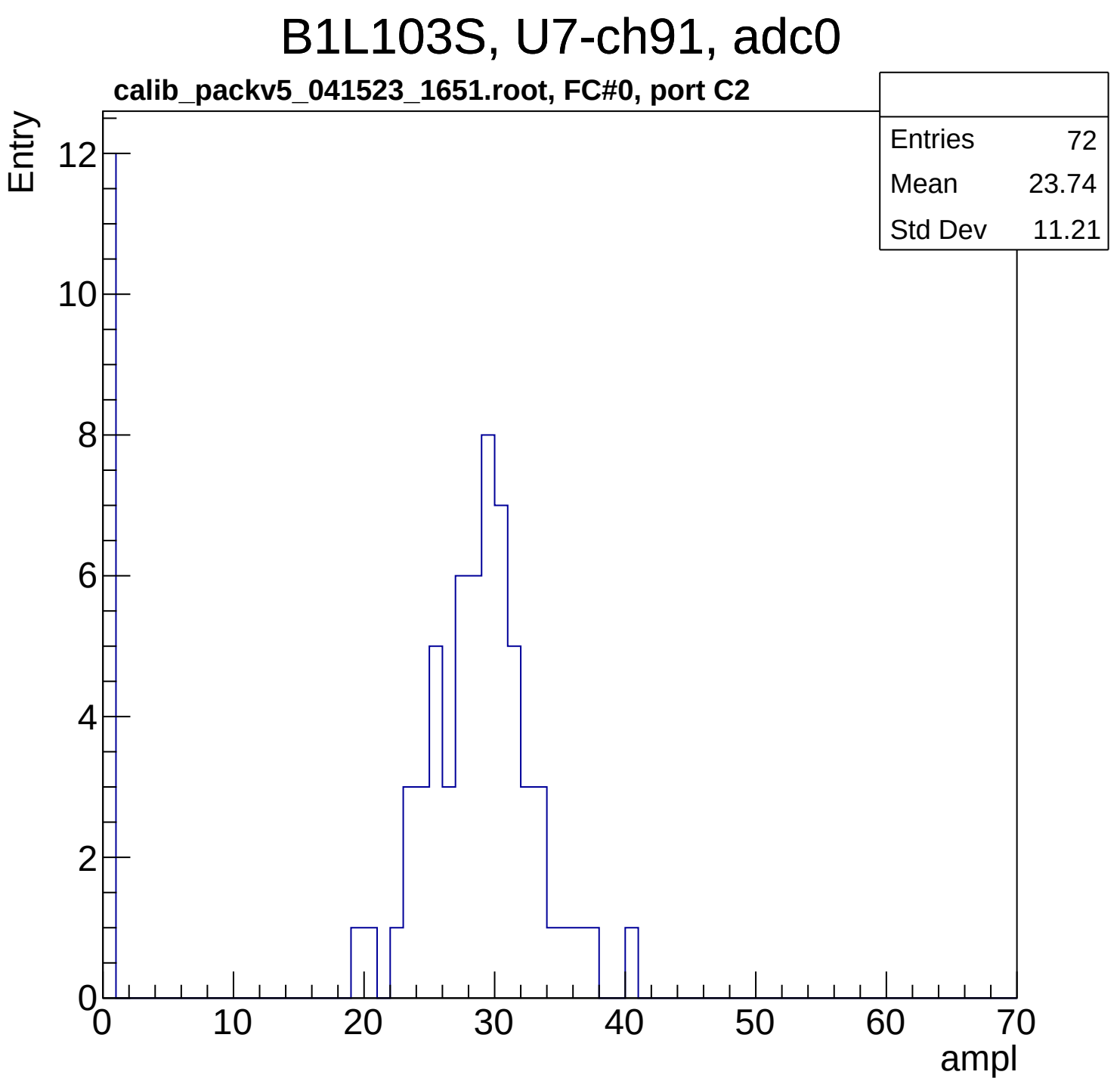
50
60
70
ampl


B1L103S, U7-ch91, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 23.74
Std Dev 11.21
Entry
0
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4
6
8
10
12
0
10
20
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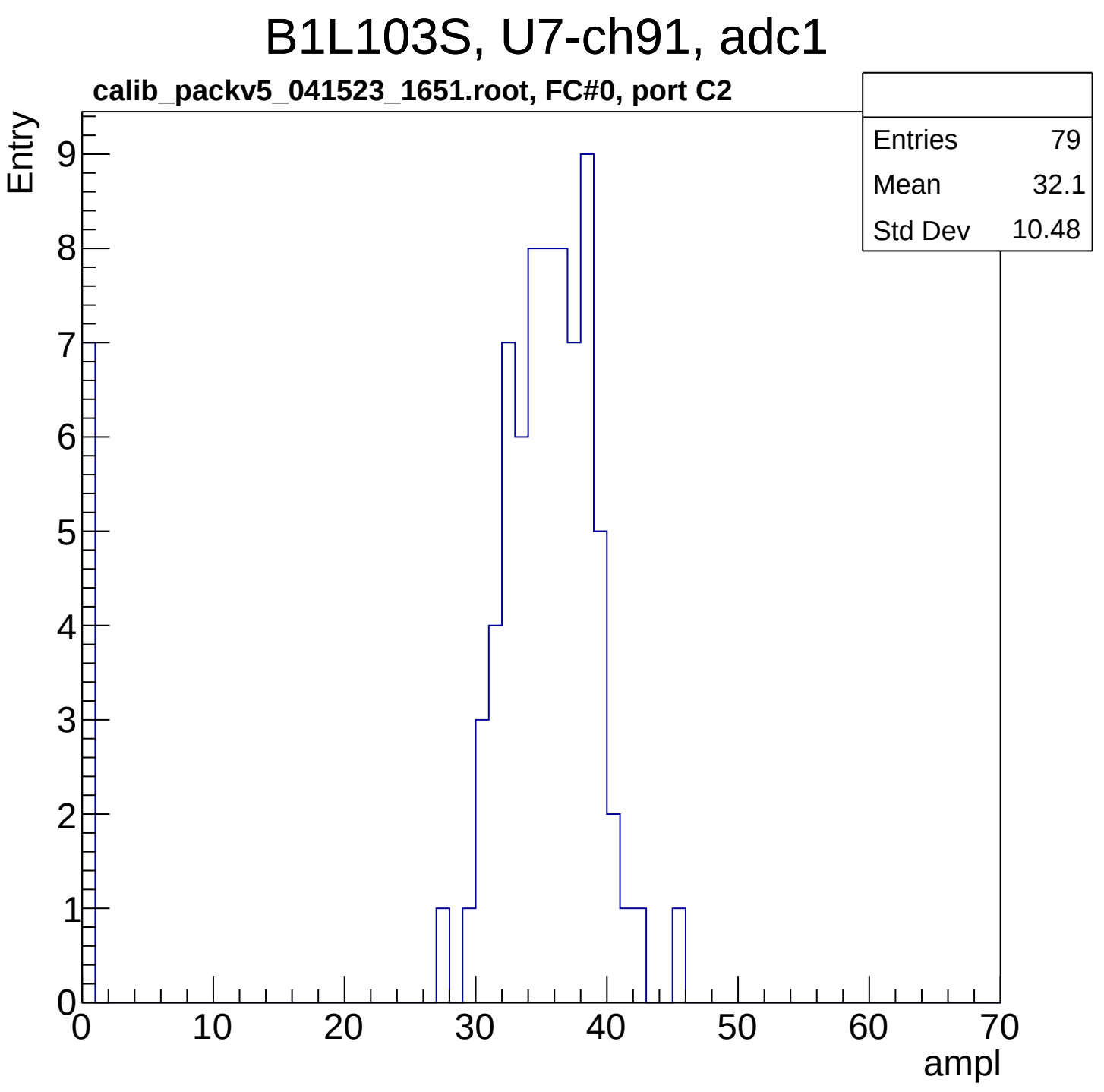
50
60
70
ampl


B1L103S, U7-ch91, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 32.1
Std Dev 10.48
Entry
ampl
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2
3
4
5
6
7
8
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0
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40
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60
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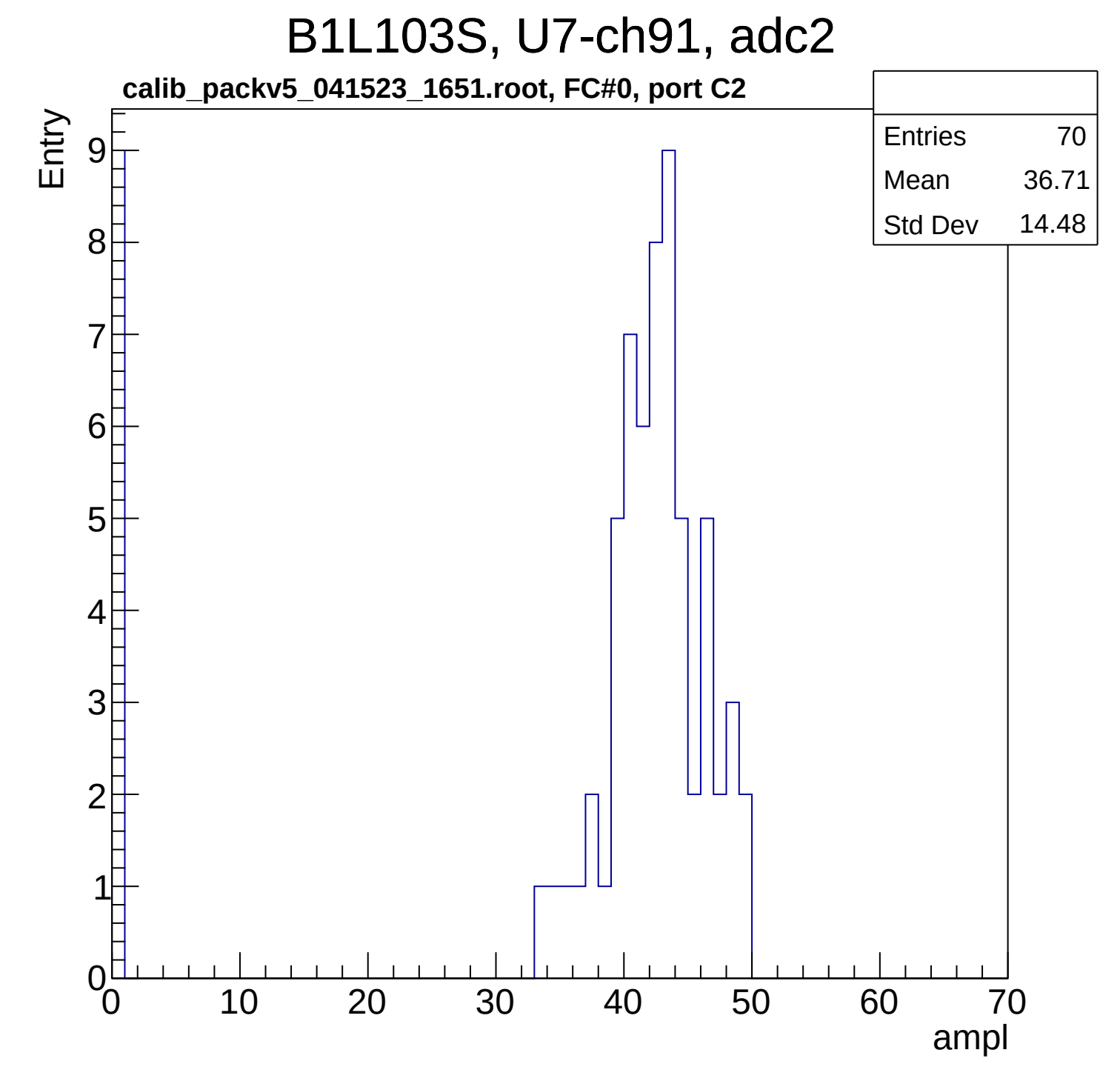
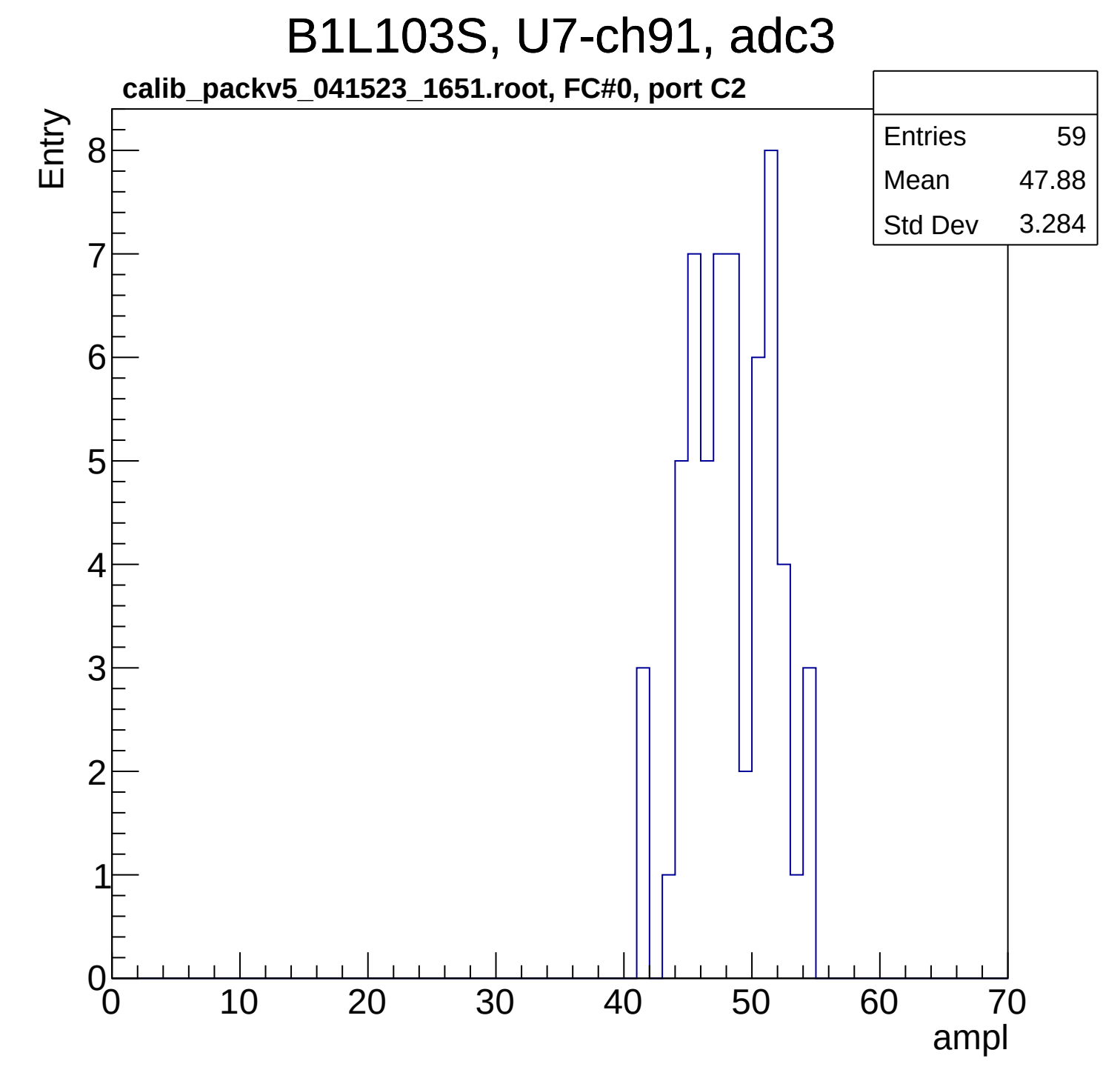

B1L103S, U7-ch91, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 36.71
Std Dev 14.48
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U7-ch91, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 47.88
Std Dev 3.284
Entry
ampl
0
1
2
3
4
5
6
7
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0
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40
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60
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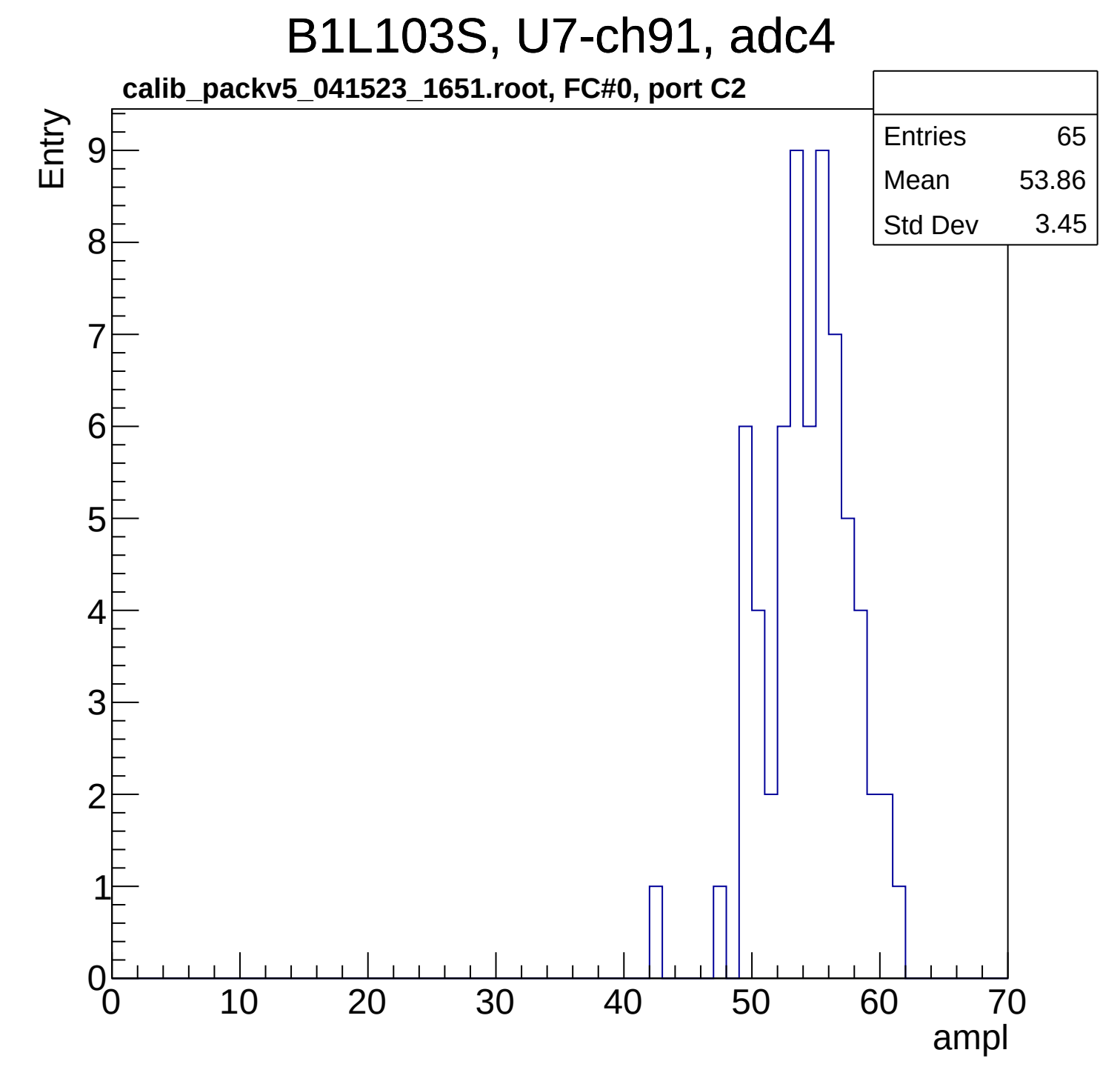
B1L103S, U7-ch91, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 53.86
Std Dev 3.45
Entry
ampl
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2
3
4
5
6
7
8
9
0
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60
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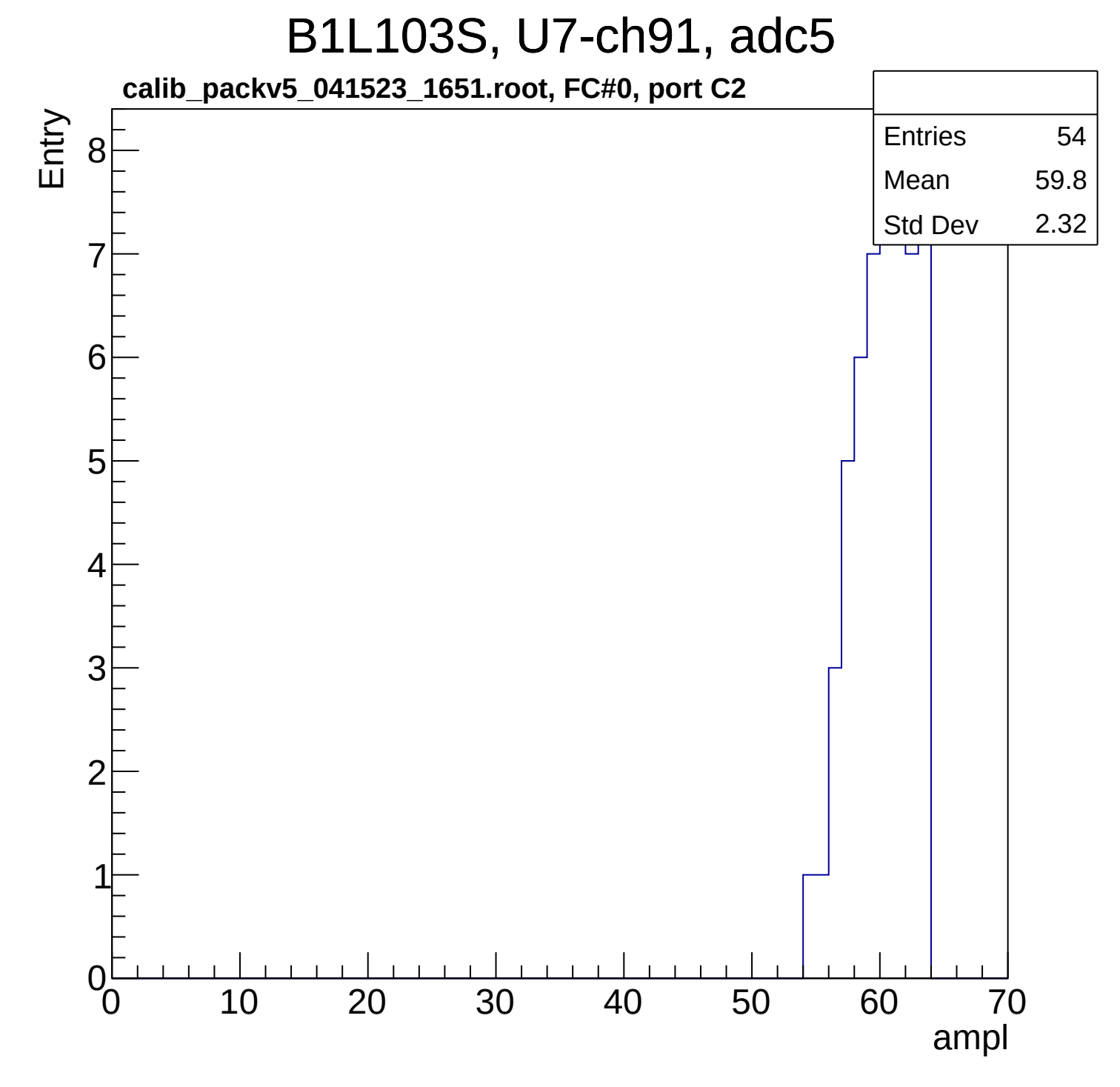
B1L103S, U7-ch91, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 59.8
Std Dev 2.32
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
30
40
50
60
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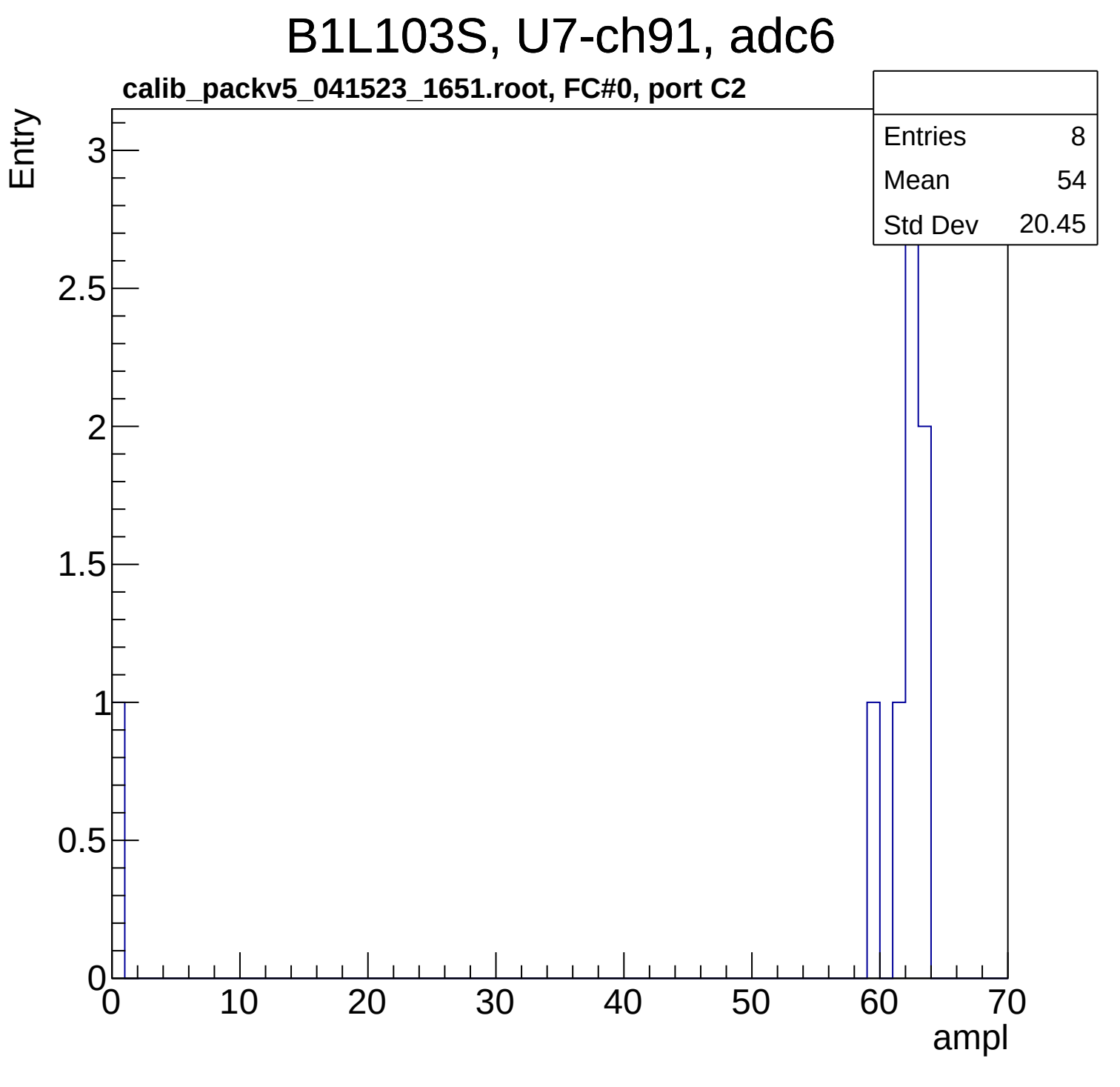
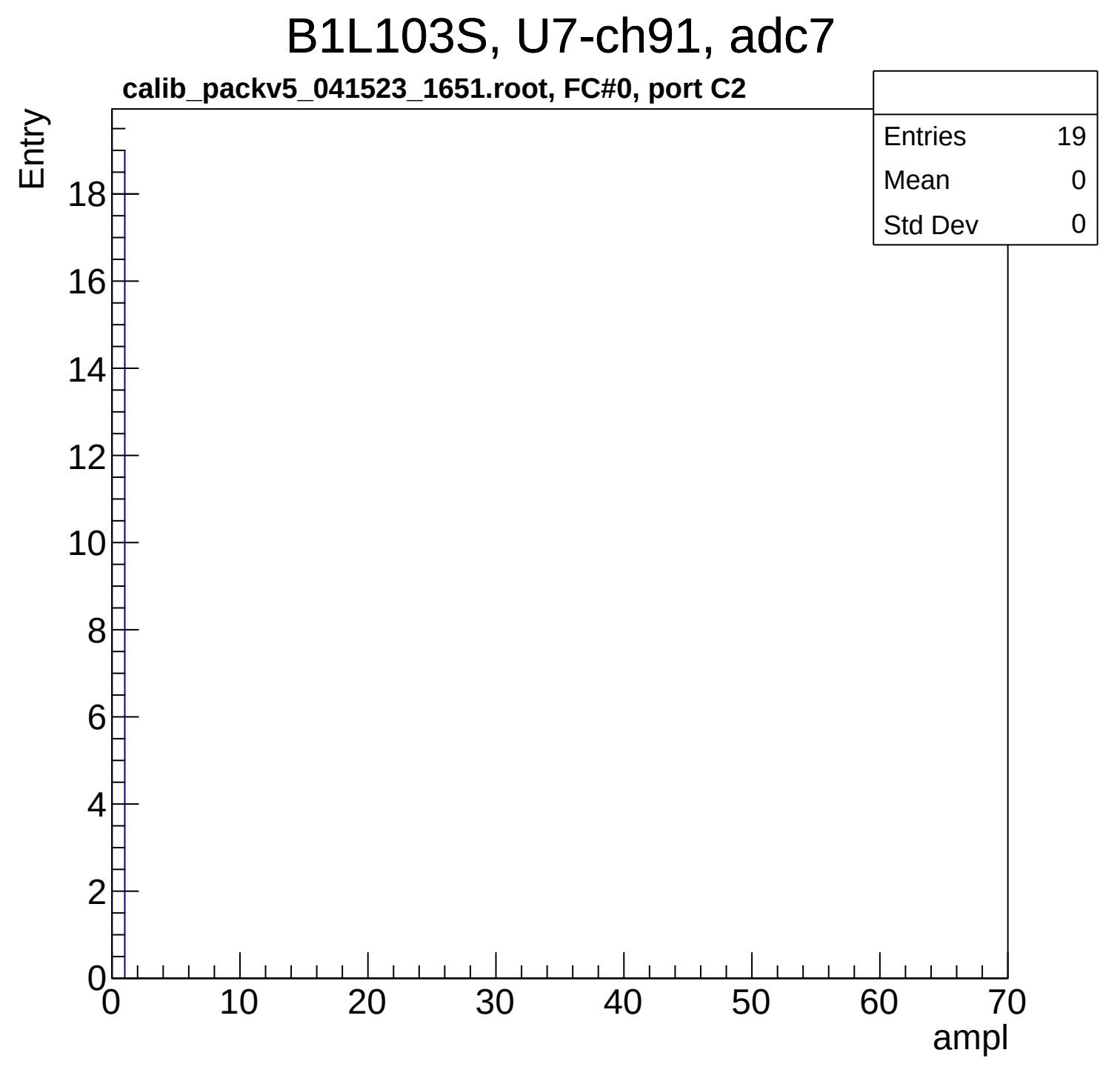
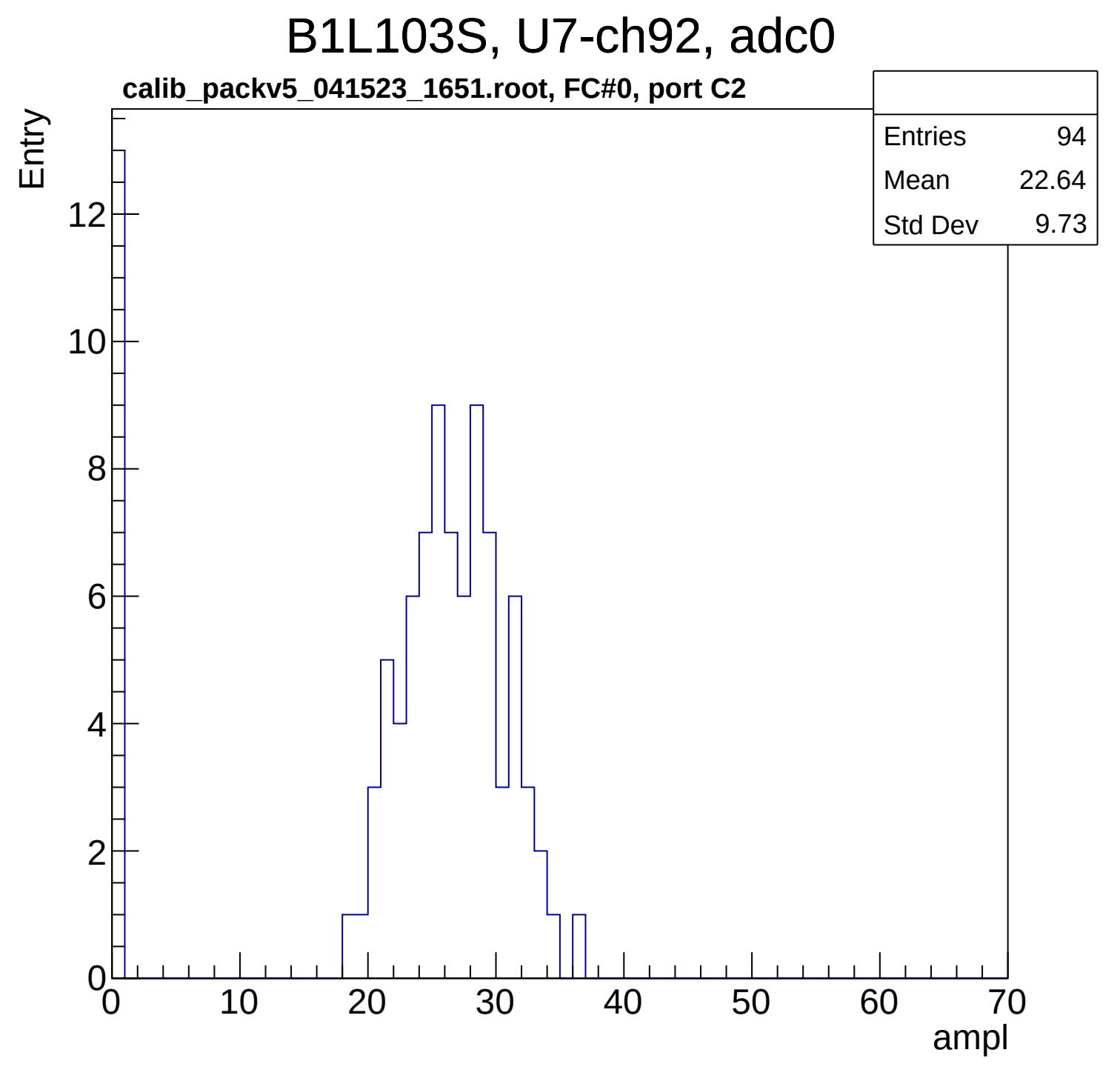
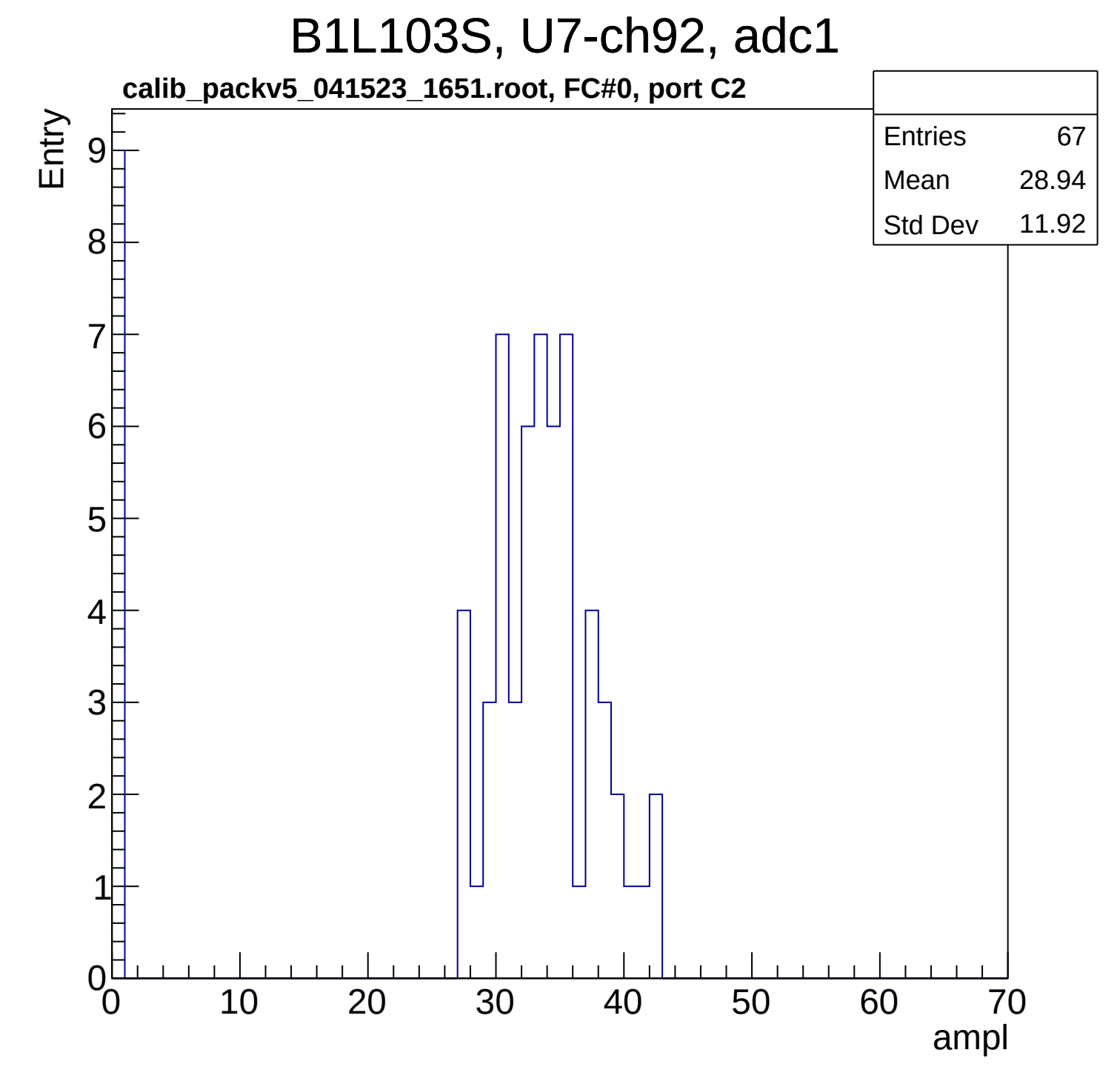
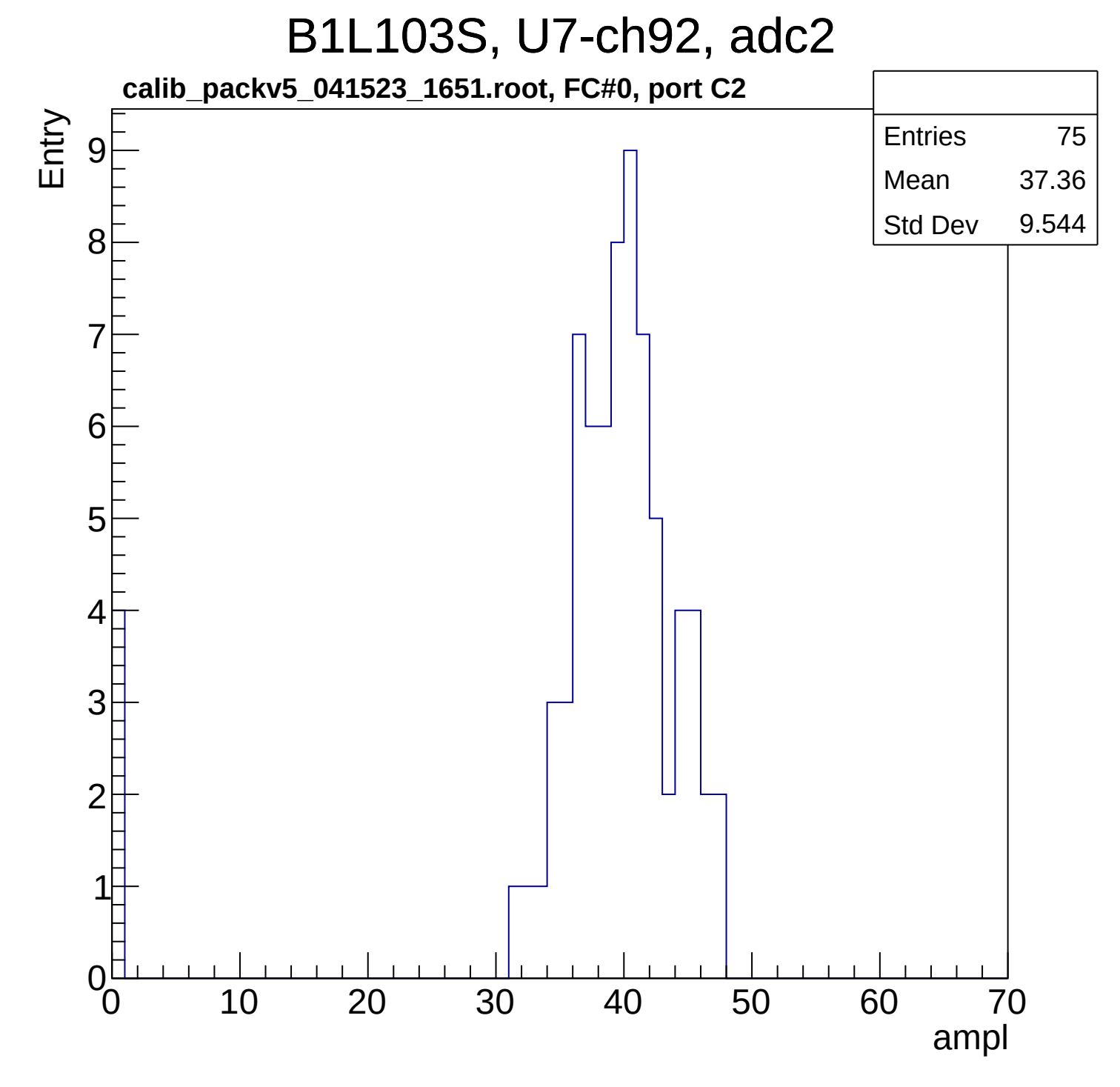

B1L103S, U7-ch91, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 54
Std Dev 20.45
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U7-ch91, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch92, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 94
Mean 22.64
Std Dev 9.73
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70


B1L103S, U7-ch92, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 28.94
Std Dev 11.92
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U7-ch92, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 37.36
Std Dev 9.544
Entry
ampl
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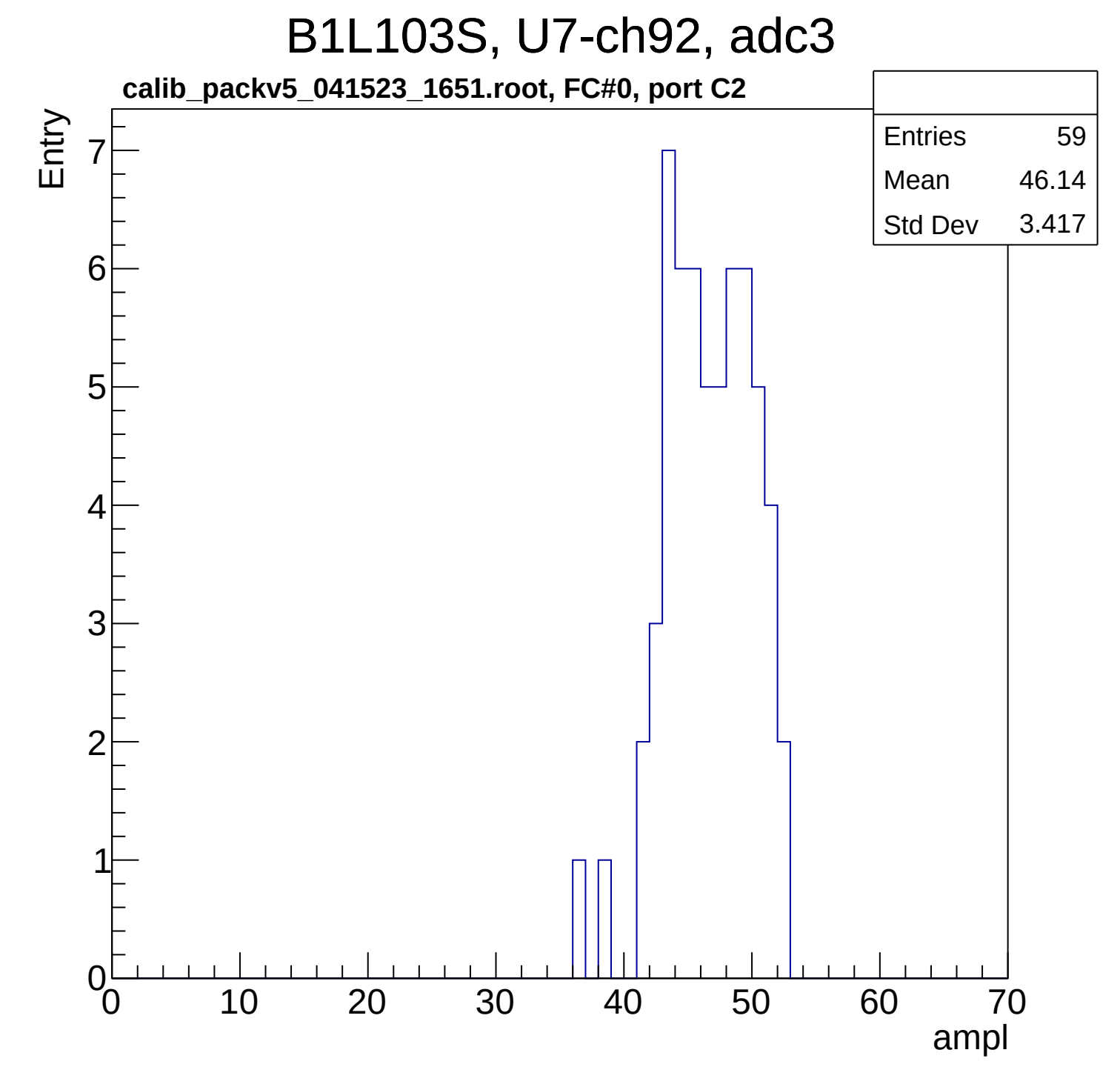
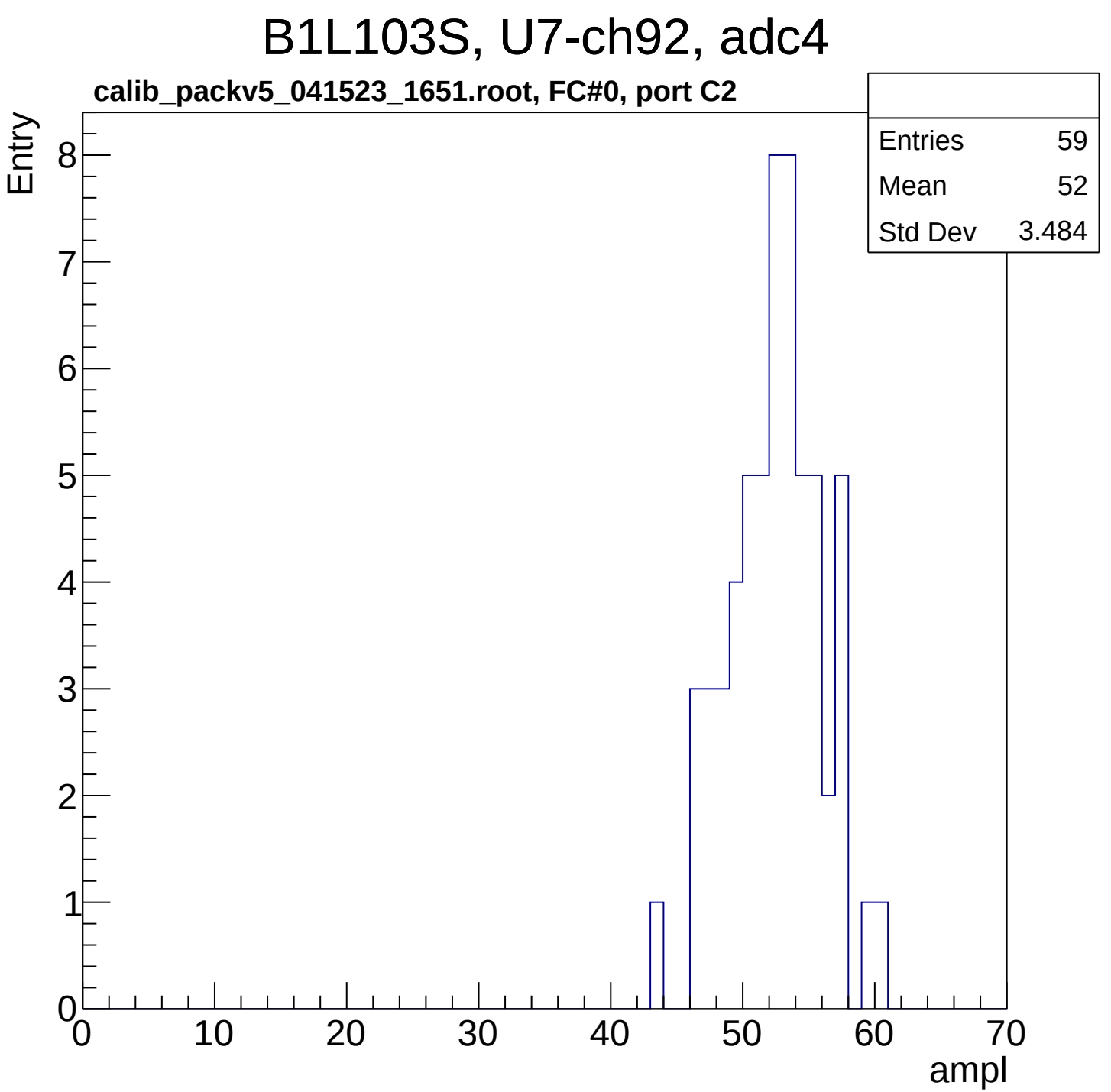
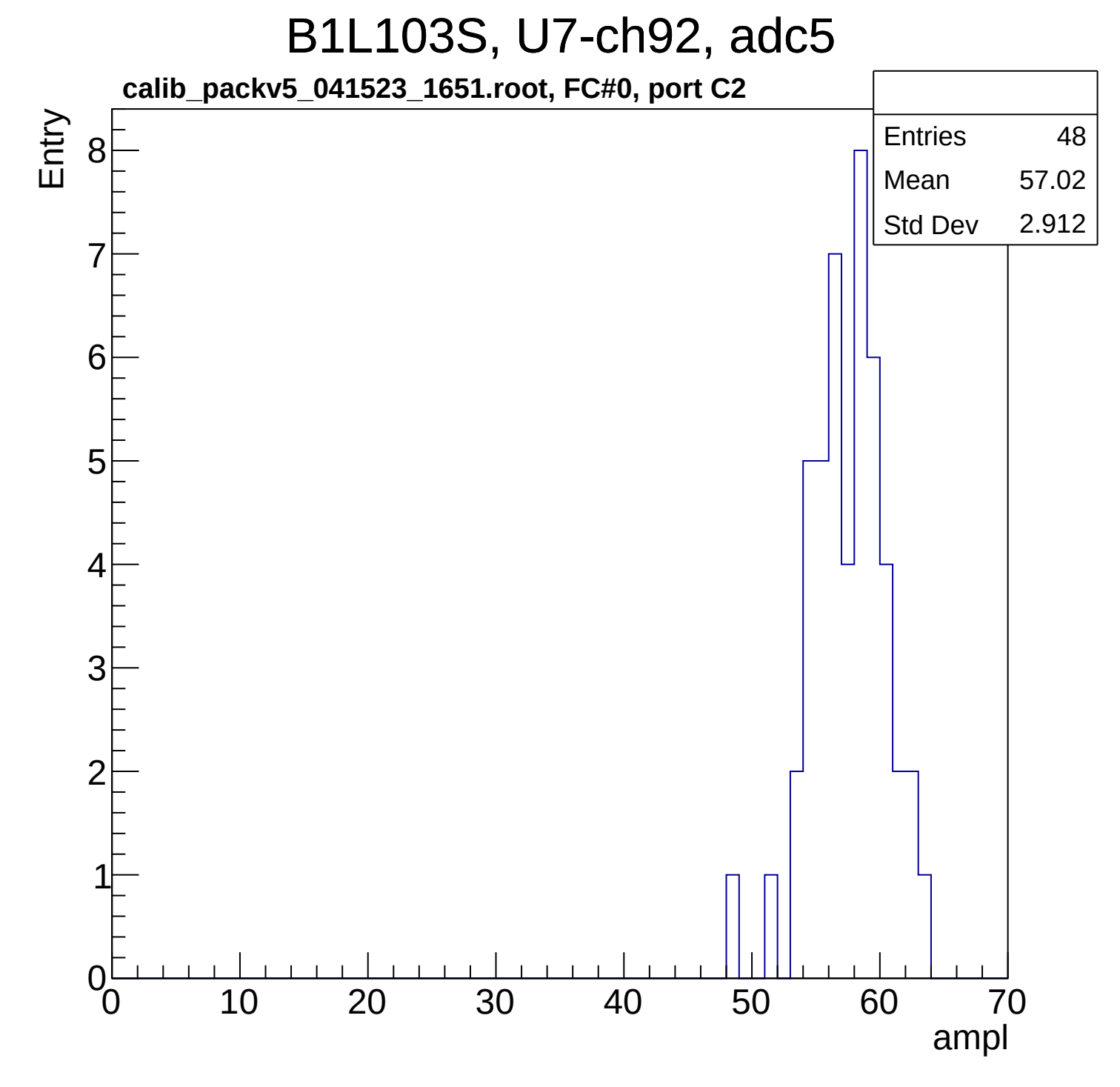
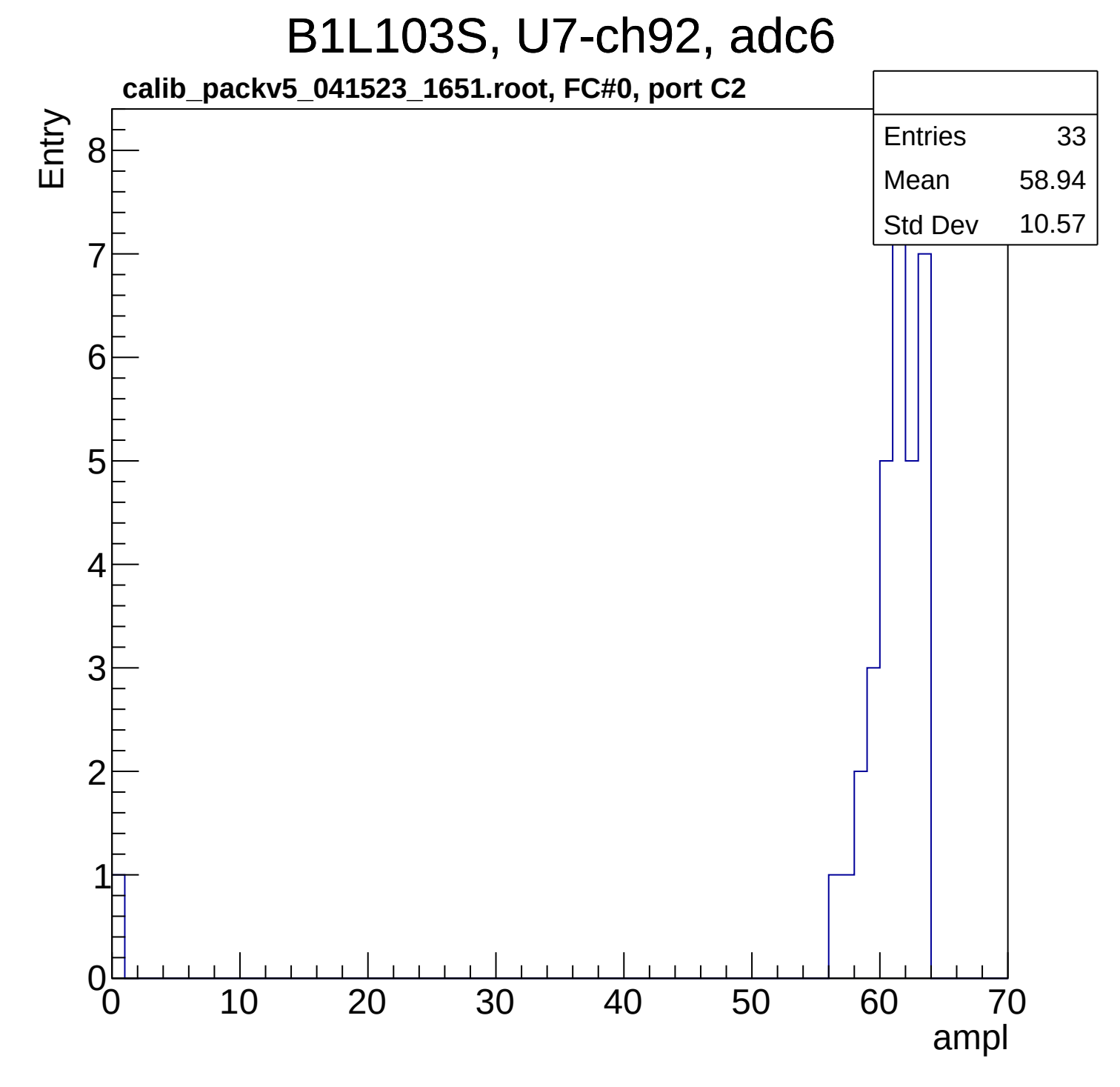
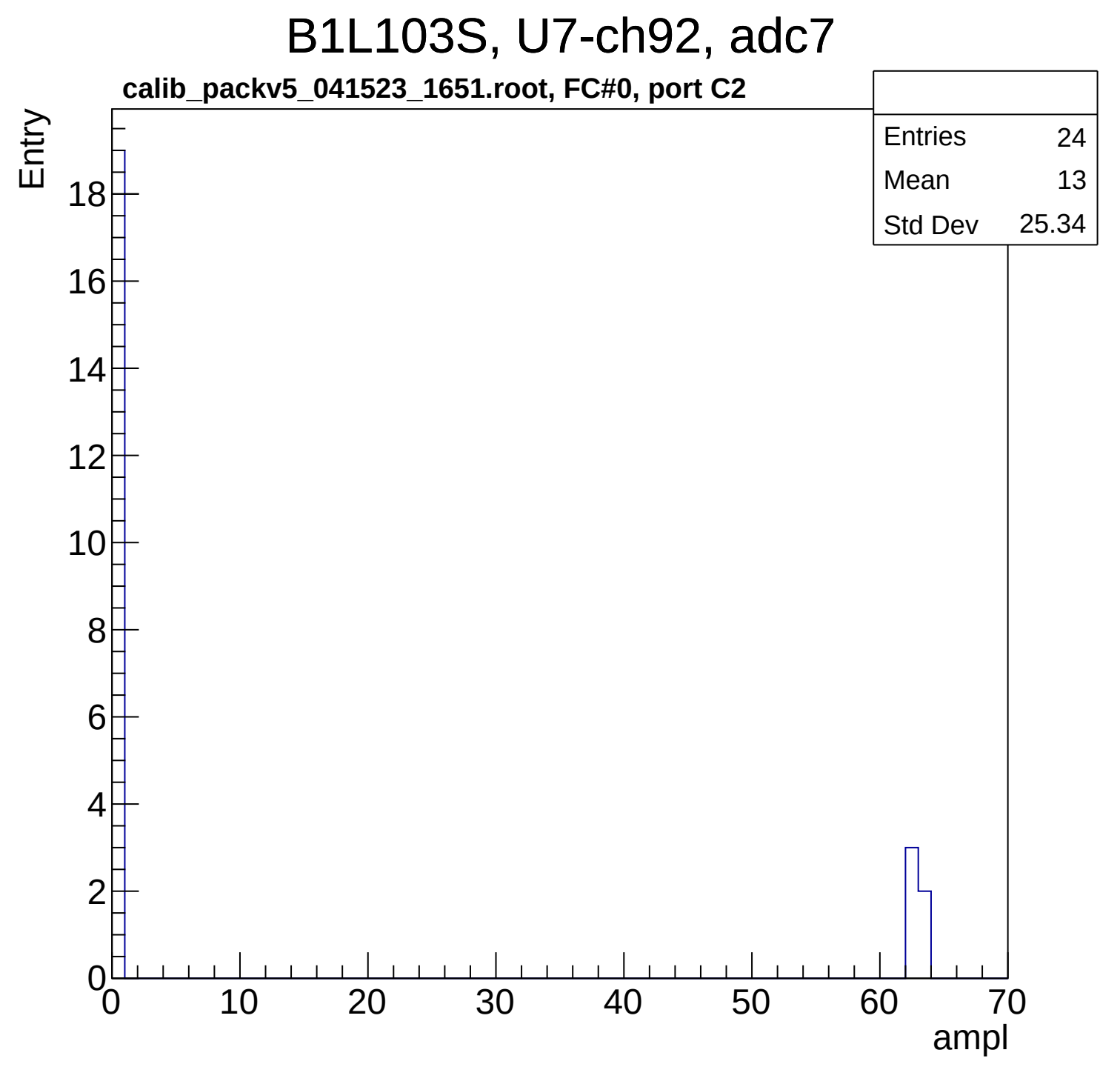
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

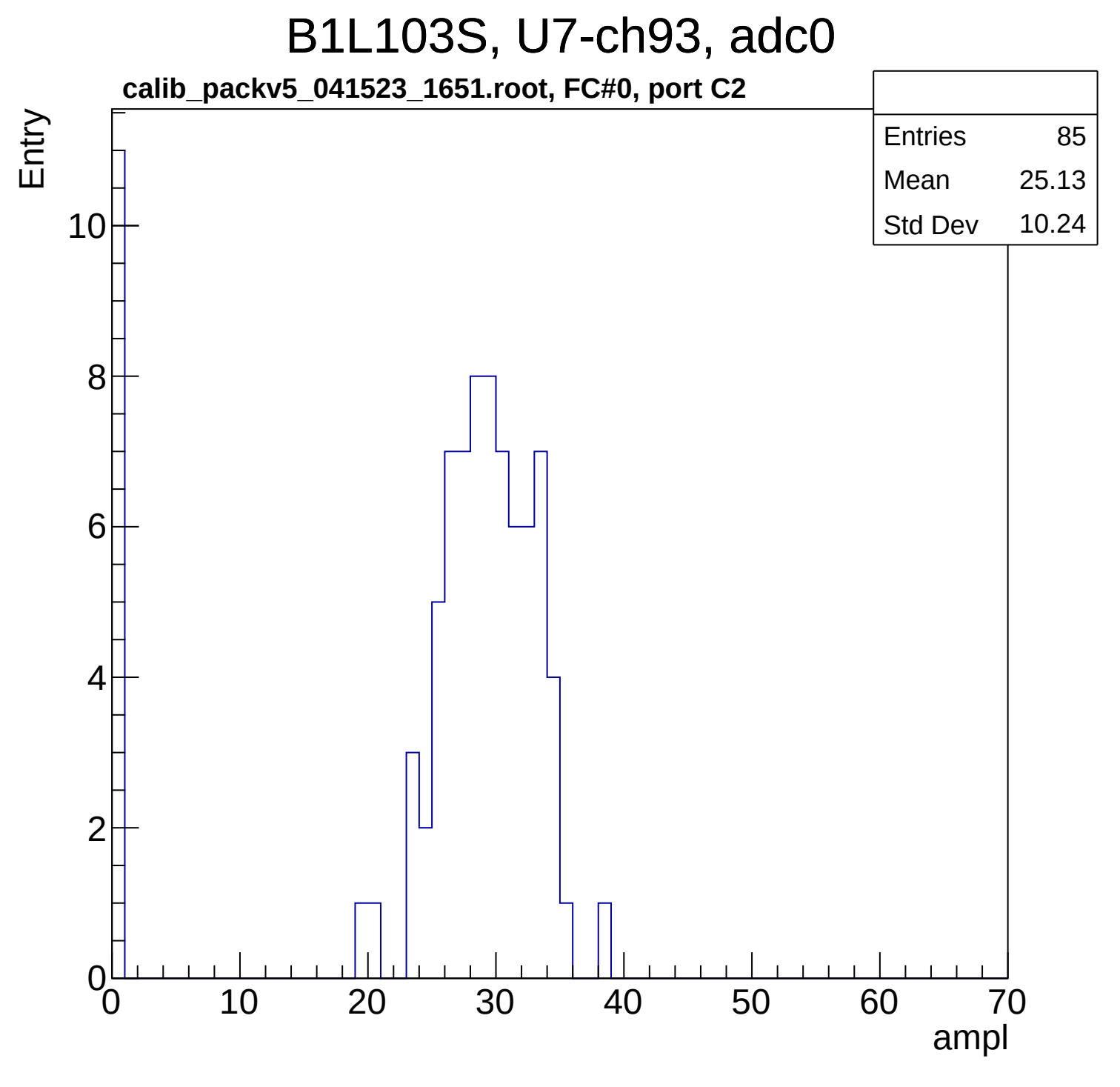

B1L103S, U7-ch92, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 46.14
Std Dev 3.417
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

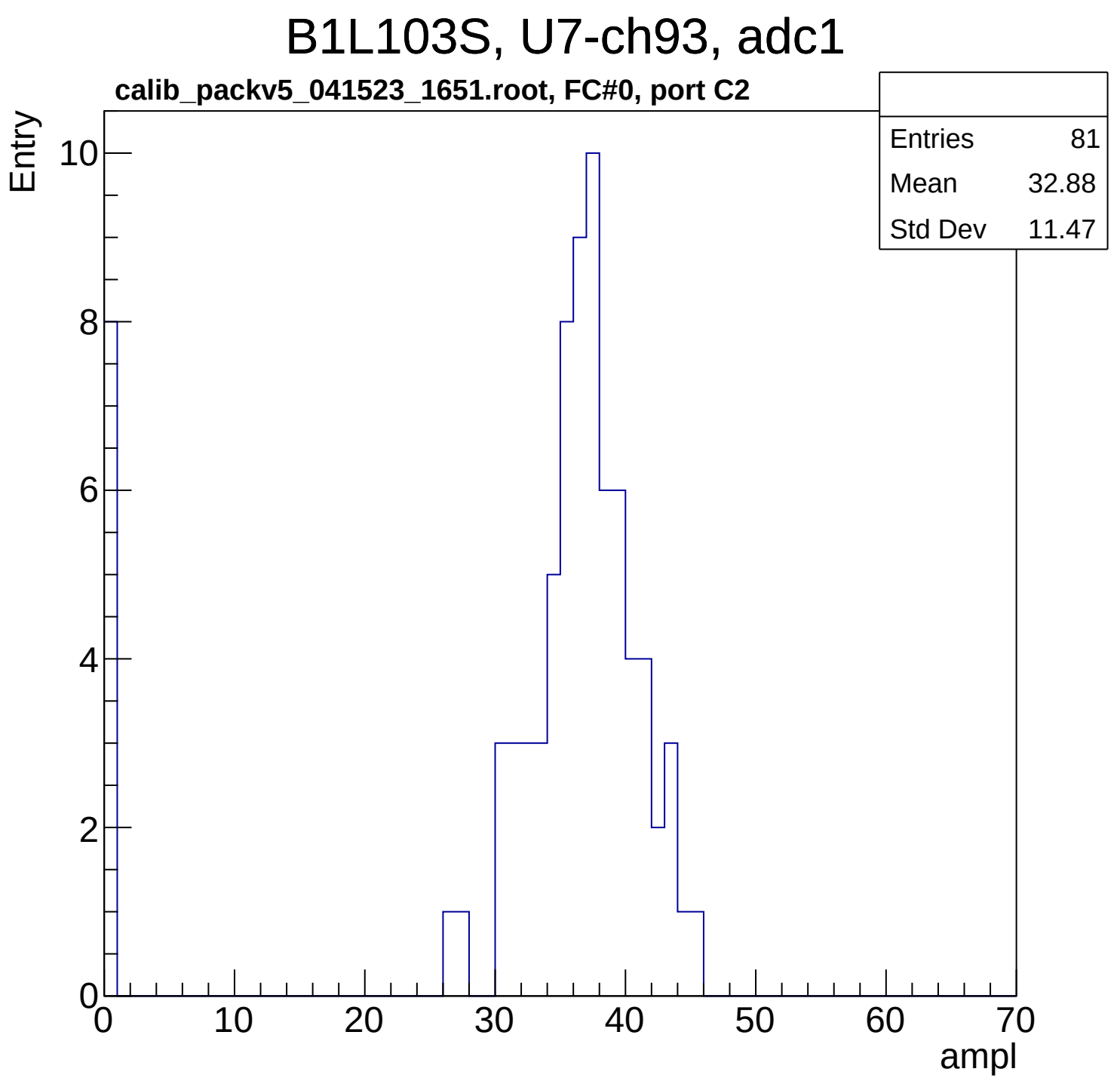

B1L103S, U7-ch92, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 52
Std Dev 3.484
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

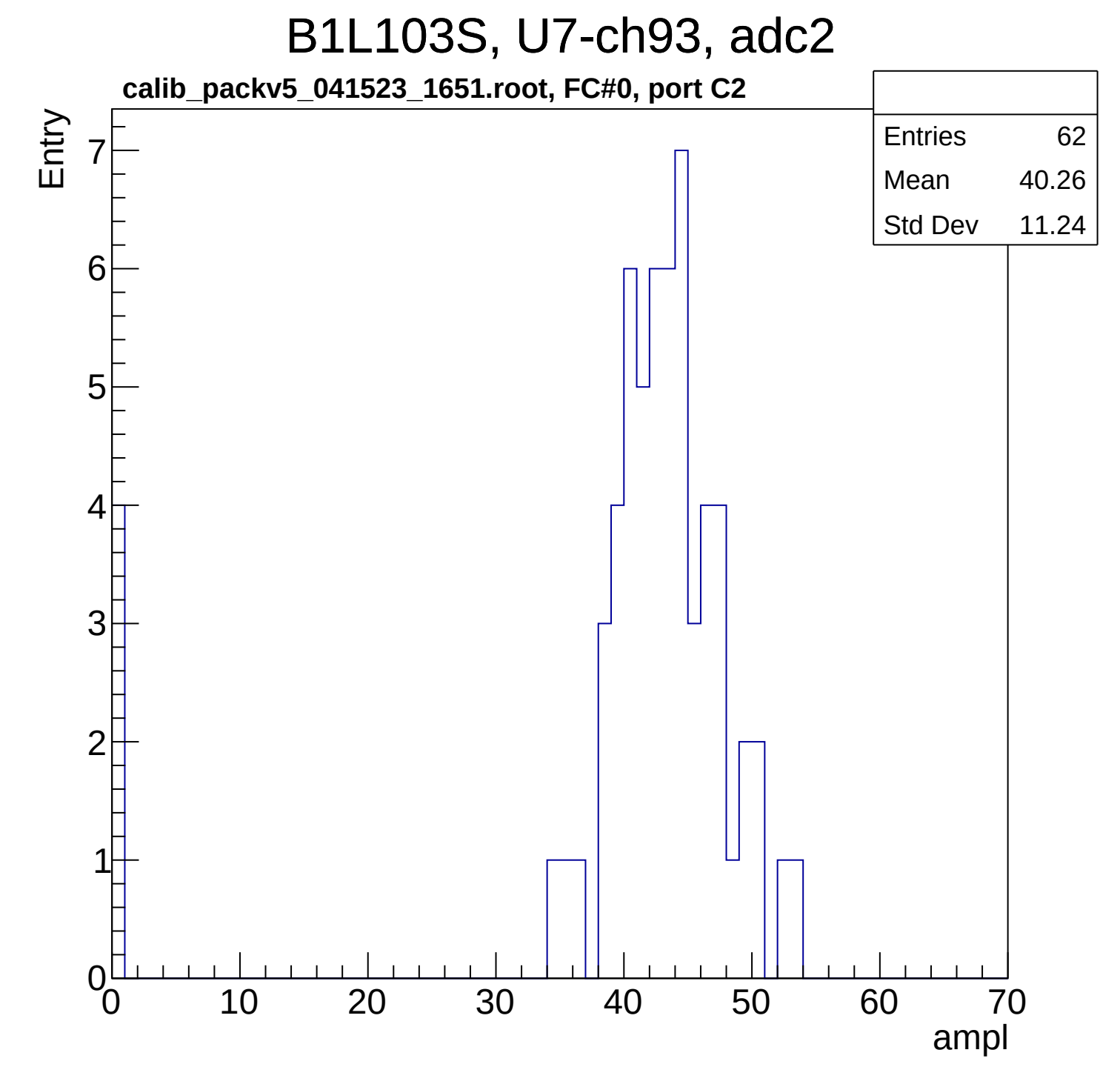

B1L103S, U7-ch92, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 57.02
Std Dev 2.912
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch92, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 33
Mean 58.94
Std Dev 10.57
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch92, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 24
Mean 13
Std Dev 25.34
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch93, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 25.13
Std Dev 10.24
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch93, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 32.88
Std Dev 11.47
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch93, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 40.26
Std Dev 11.24
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
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40
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60
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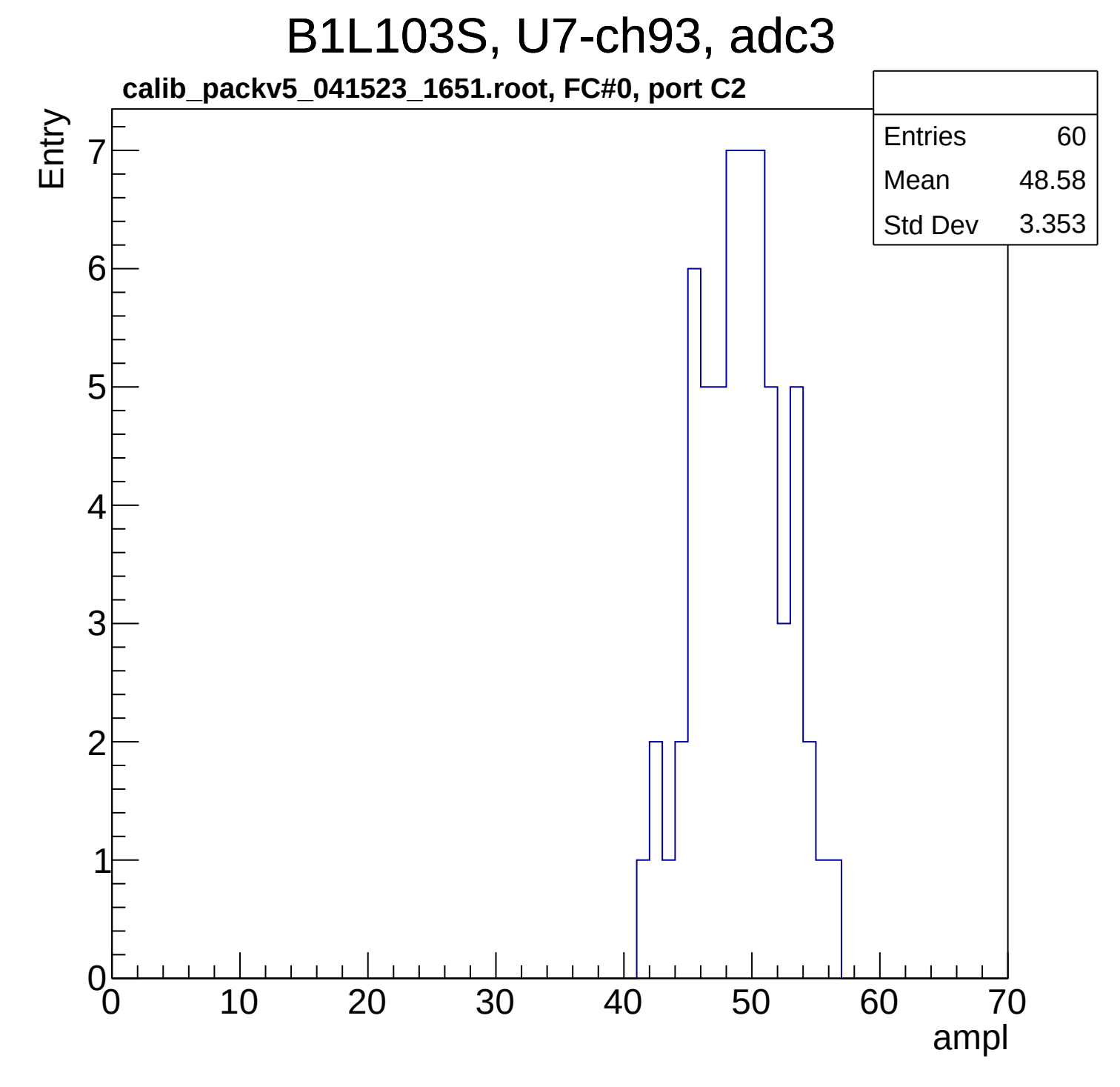
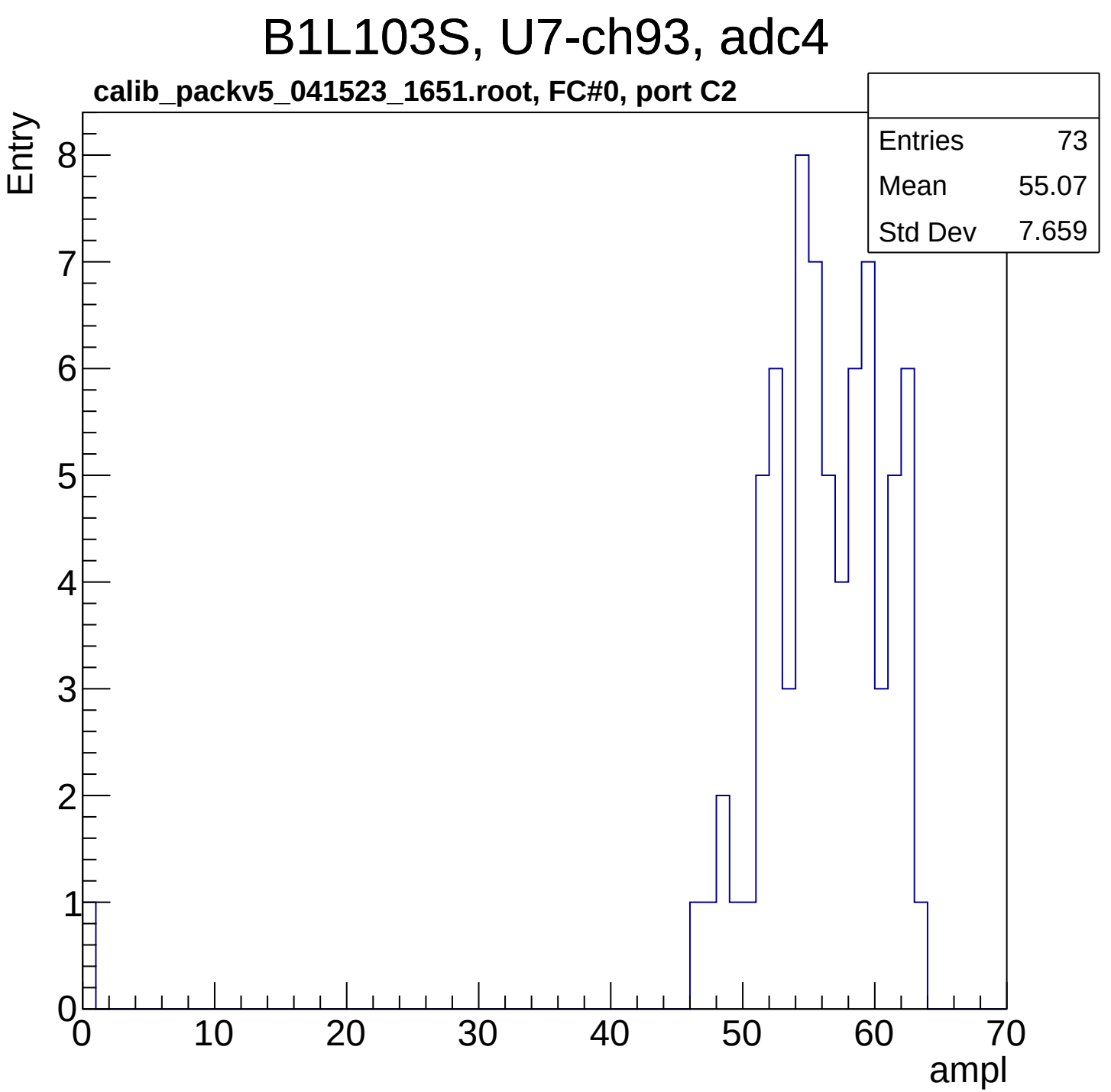

B1L103S, U7-ch93, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 48.58
Std Dev 3.353
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U7-ch93, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 55.07
Std Dev 7.659
Entry
ampl
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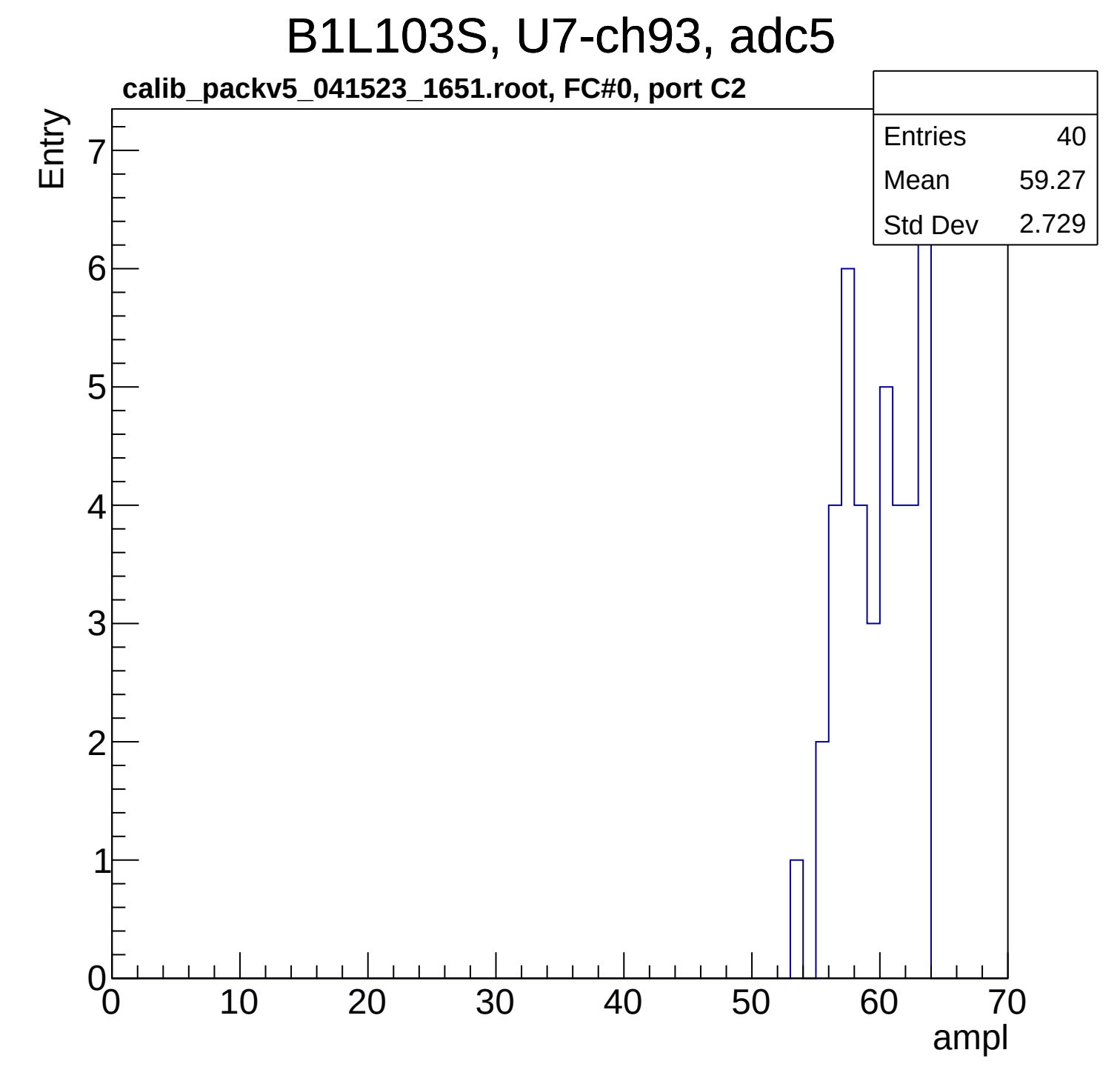
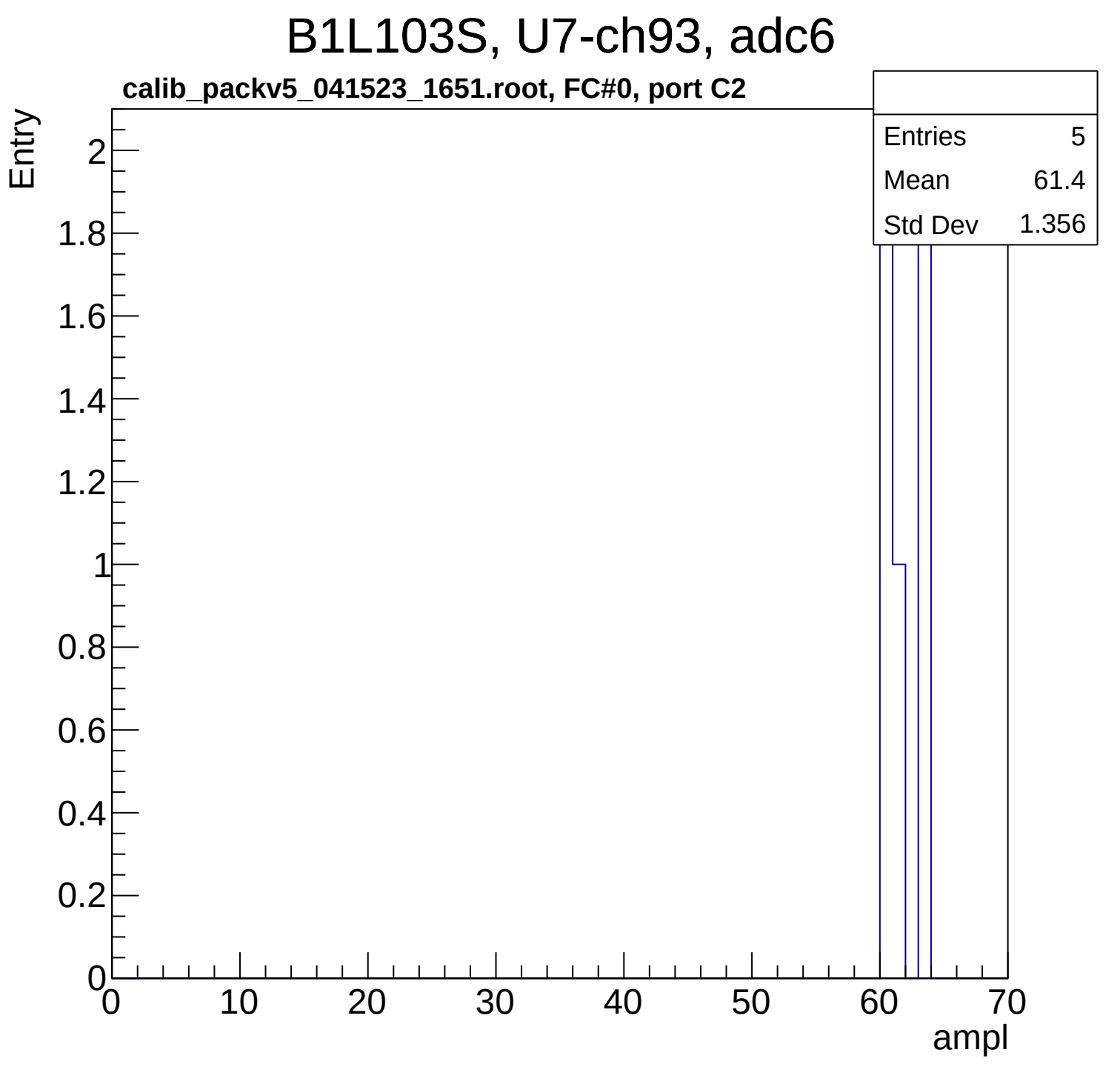
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch93, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 40
Mean 59.27
Std Dev 2.729
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U7-ch93, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 5
Mean 61.4
Std Dev 1.356
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
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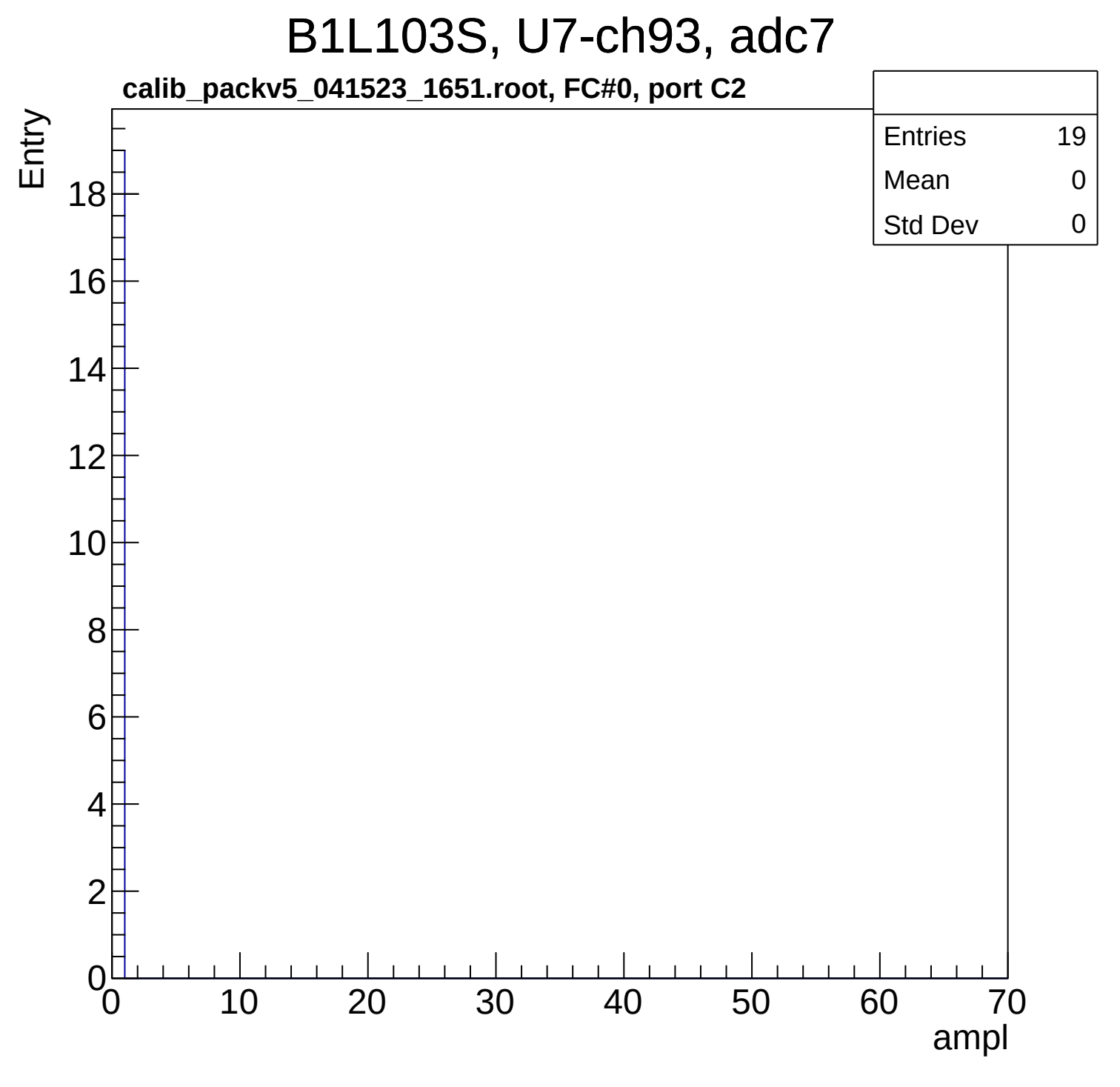
40
50
60
70


B1L103S, U7-ch93, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
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10
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30
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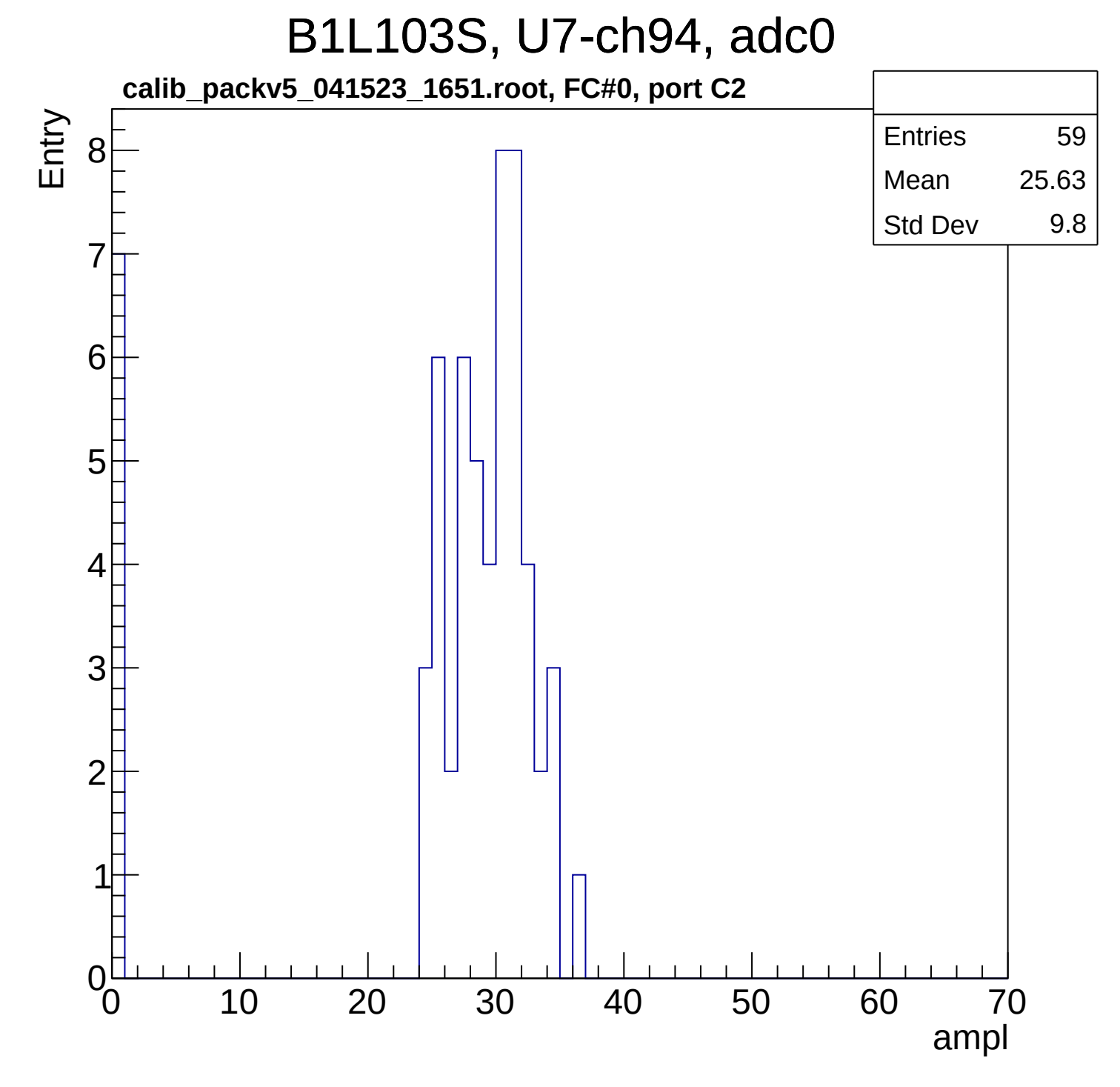
50
60
70
ampl


B1L103S, U7-ch94, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 25.63
Std Dev 9.8
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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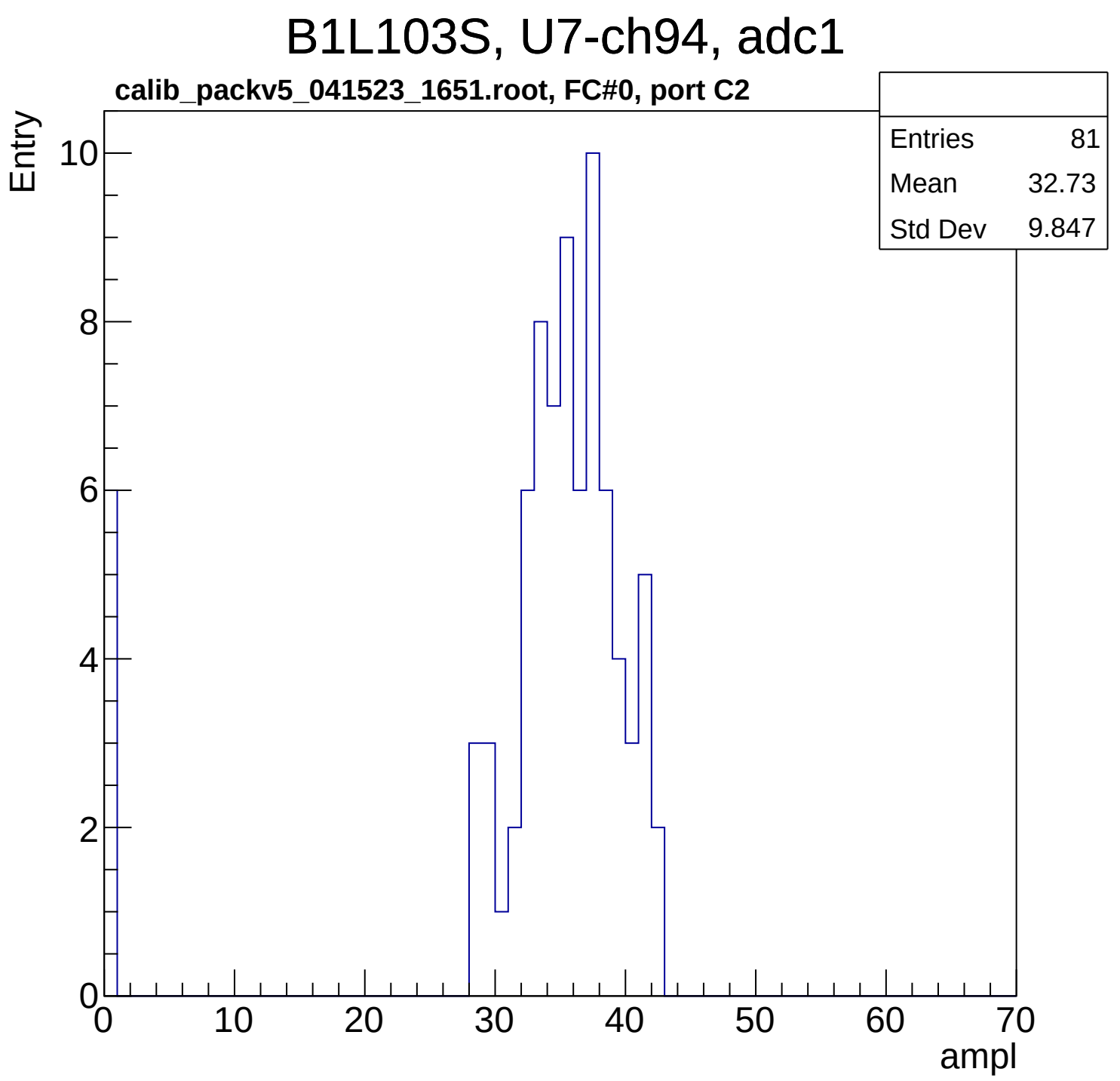
40
50
60
70


B1L103S, U7-ch94, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 32.73
Std Dev 9.847
Entry
ampl
0
2
4
6
8
10
0
10
20
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40
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60
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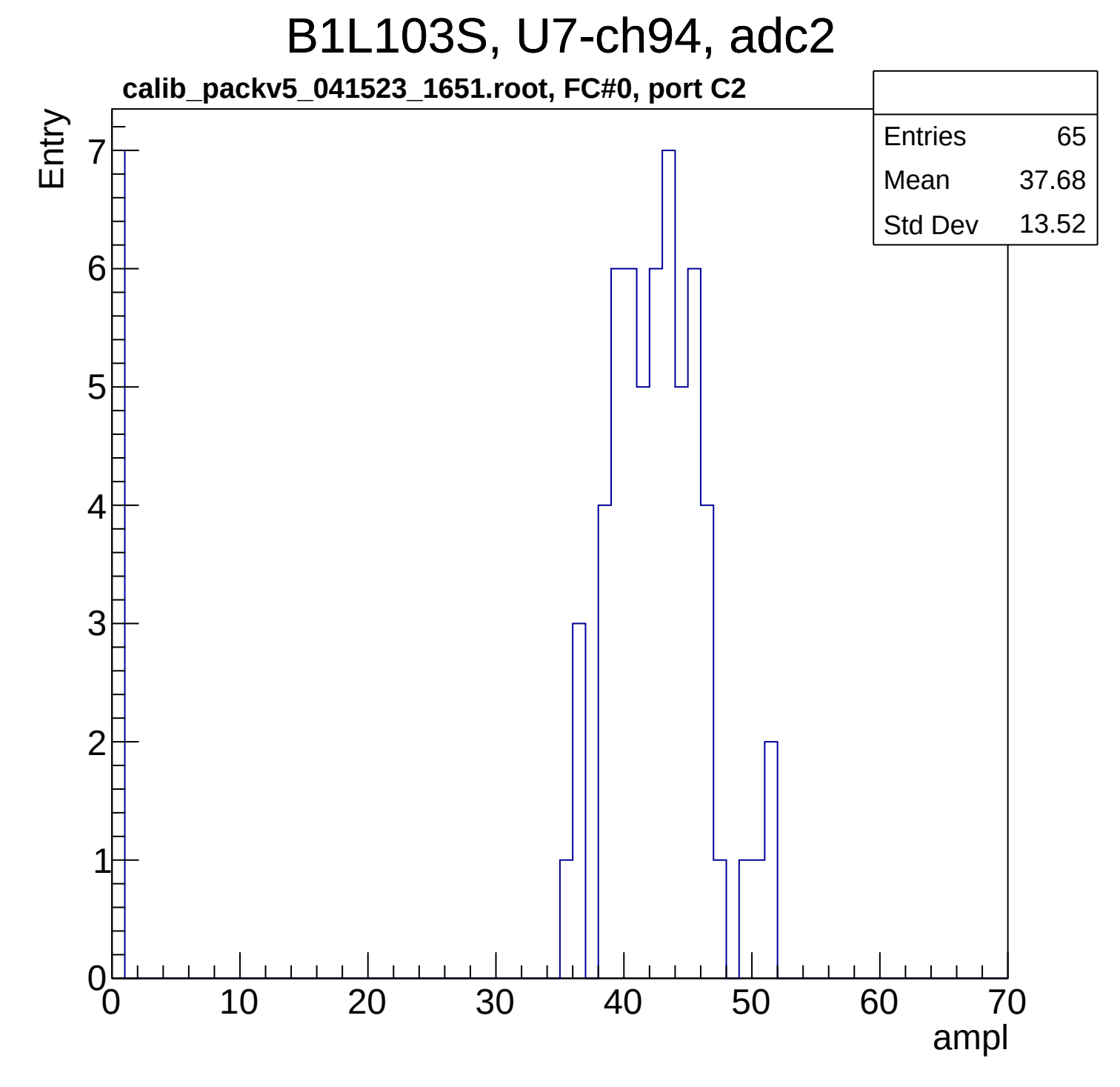
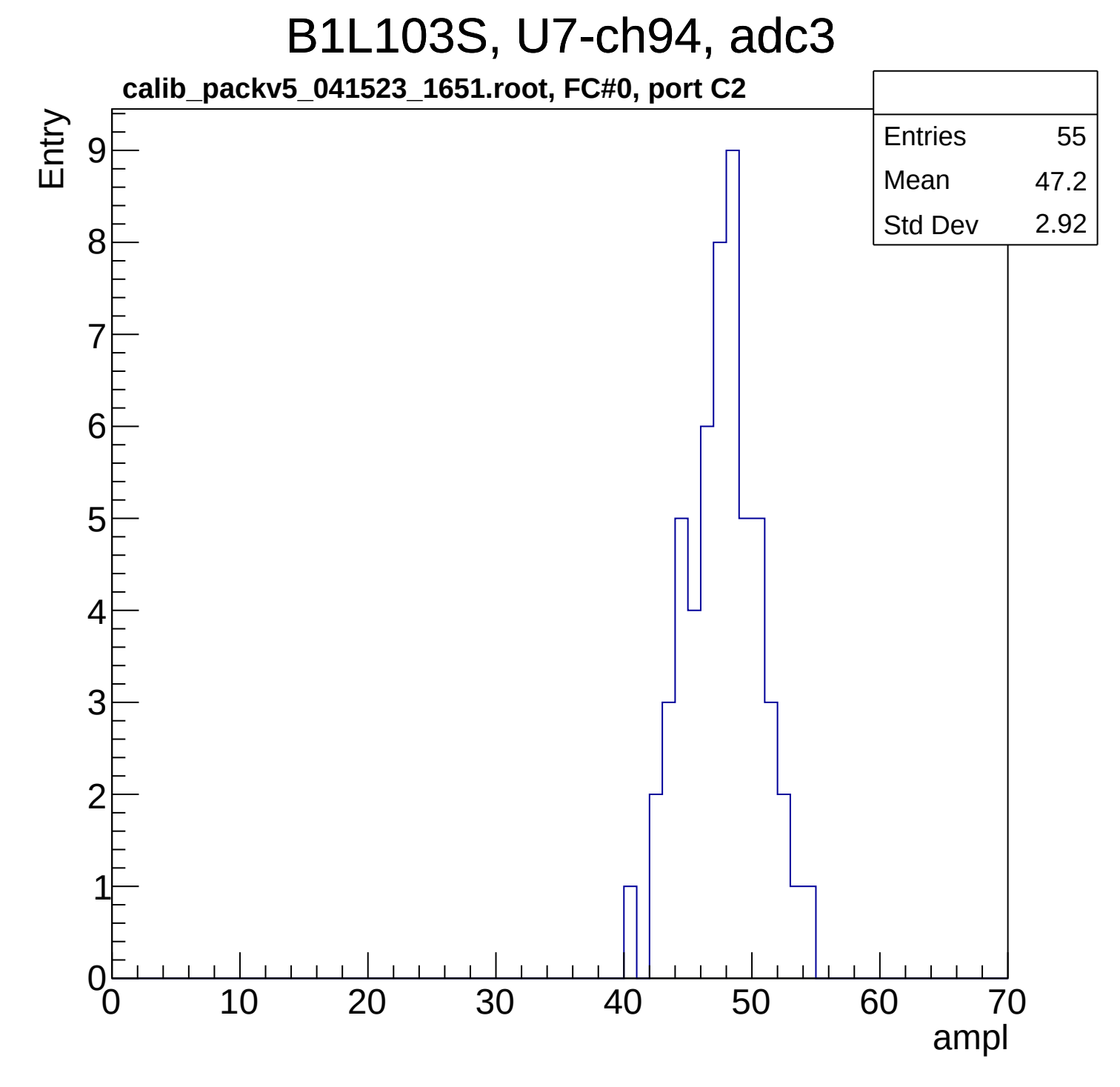

B1L103S, U7-ch94, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 37.68
Std Dev 13.52
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U7-ch94, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 47.2
Std Dev 2.92
Entry
ampl
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2
3
4
5
6
7
8
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0
10
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40
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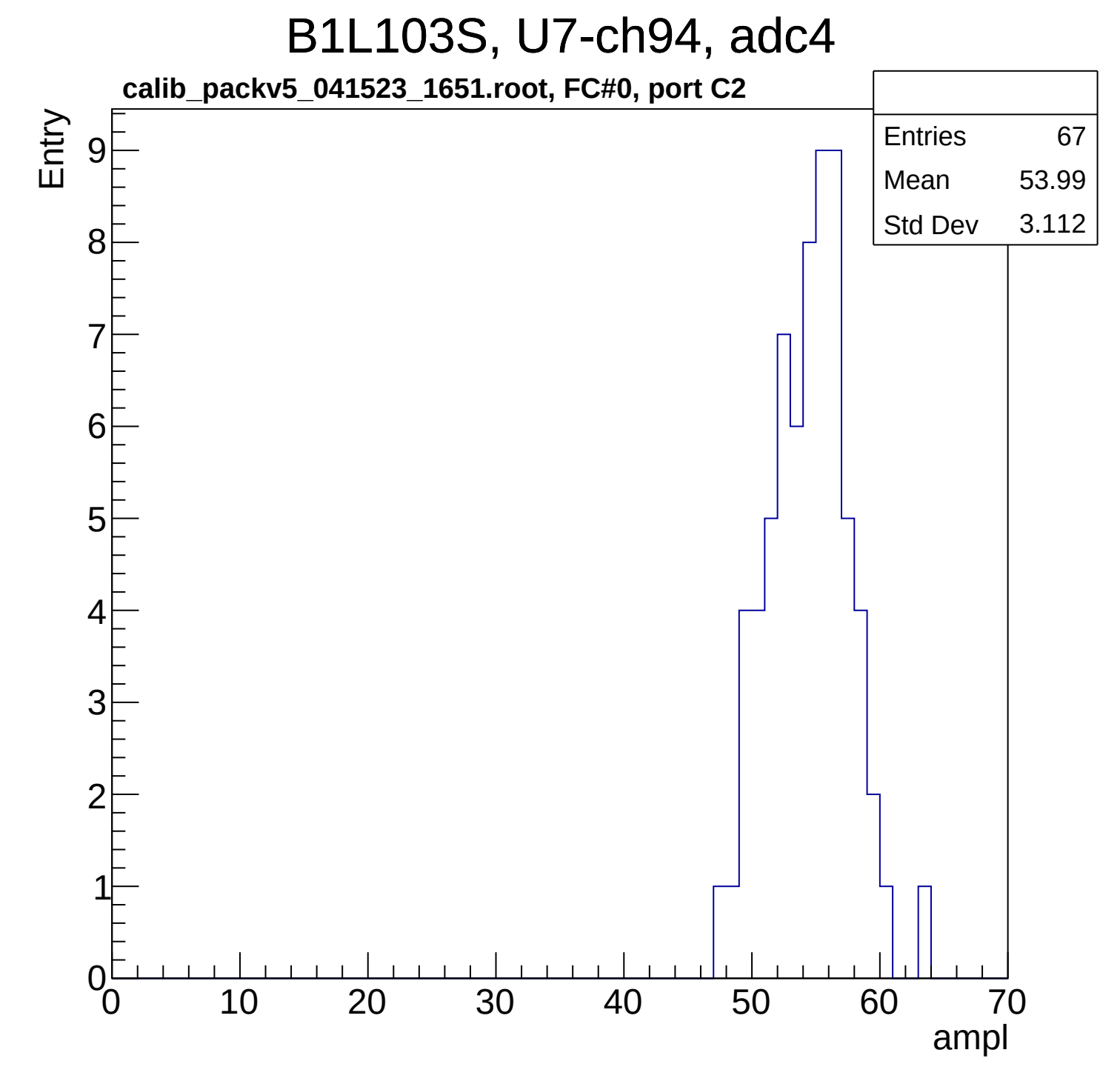
60
70


B1L103S, U7-ch94, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 53.99
Std Dev 3.112
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
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60
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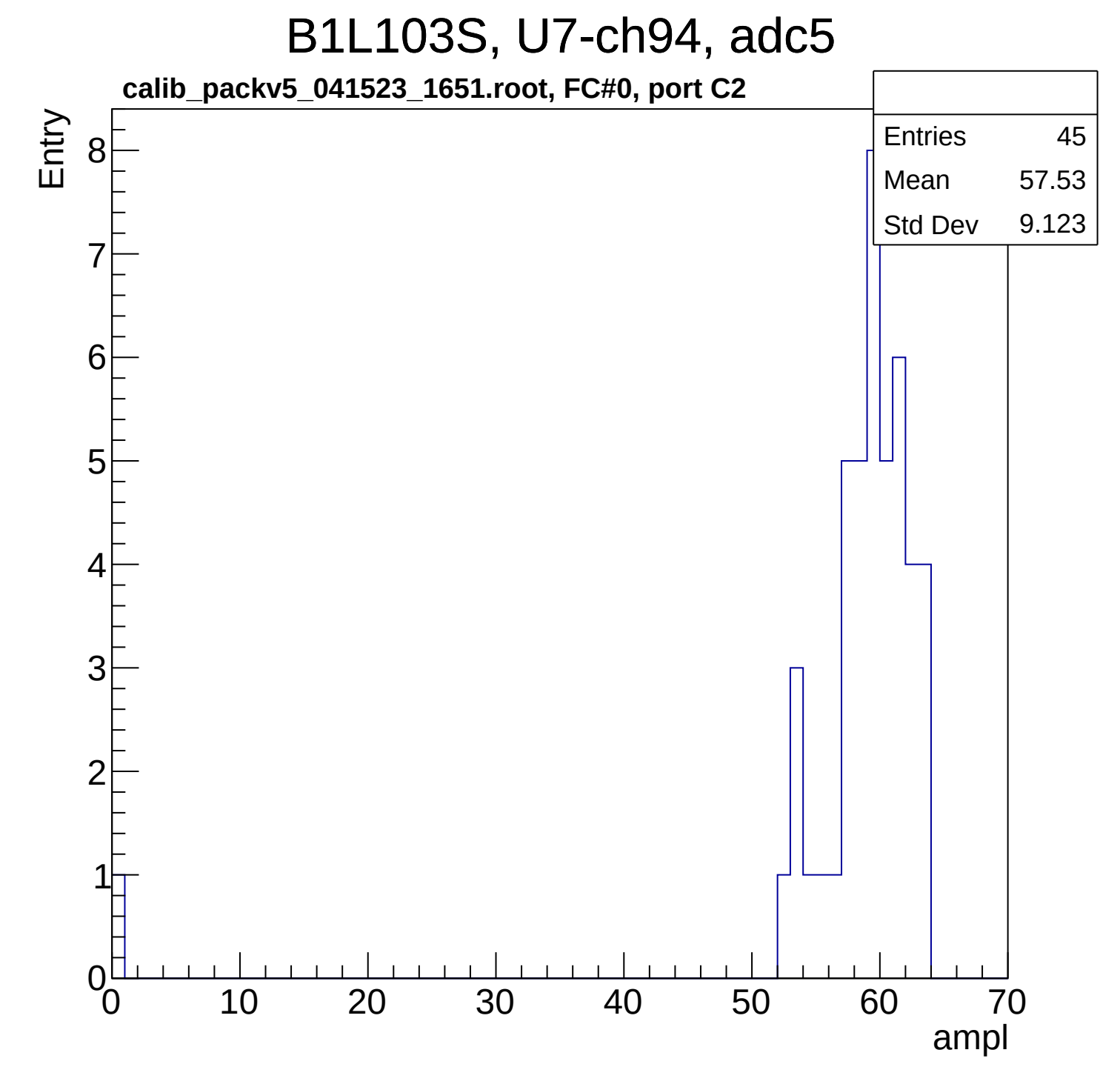
B1L103S, U7-ch94, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 57.53
Std Dev 9.123
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
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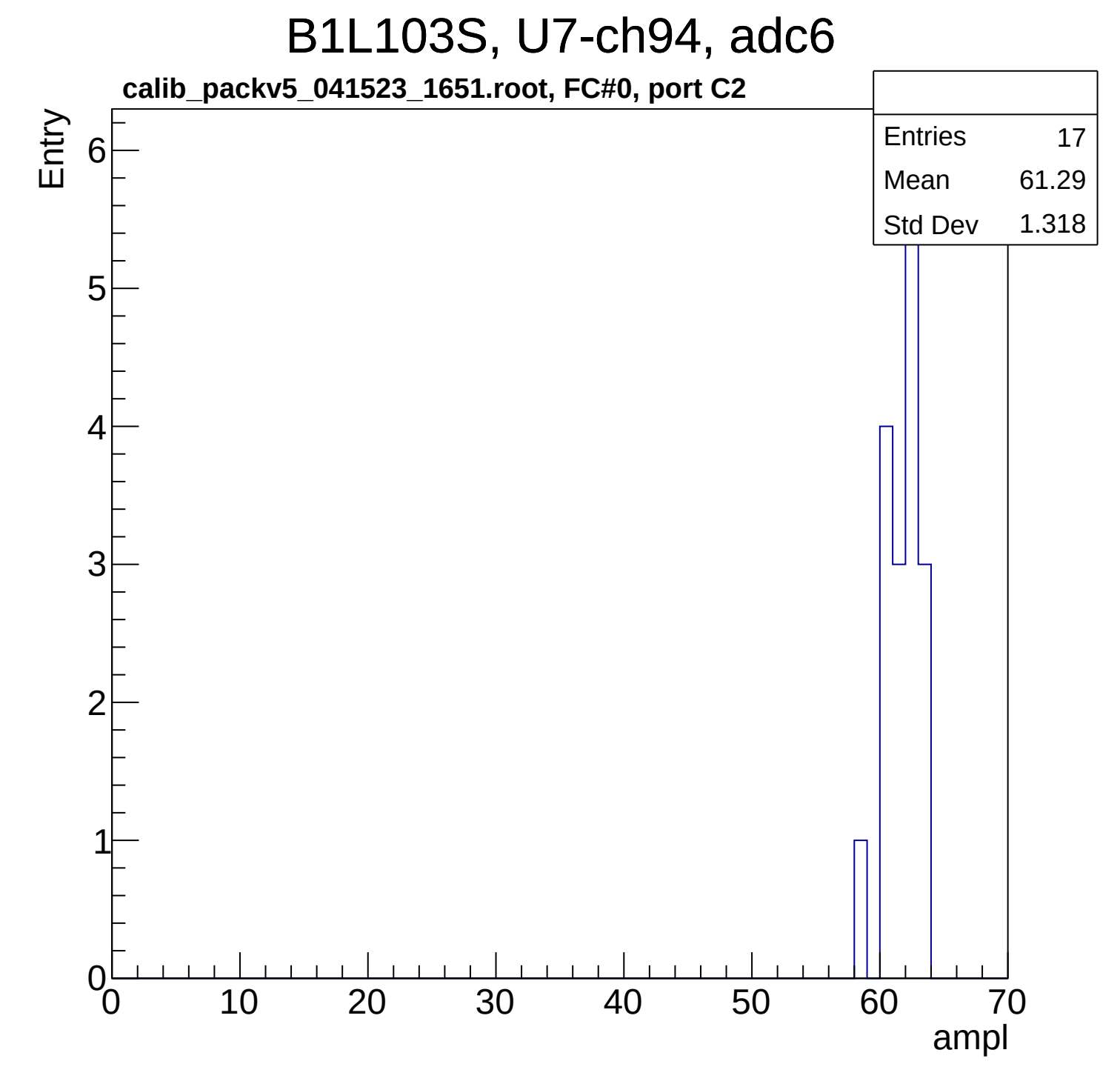
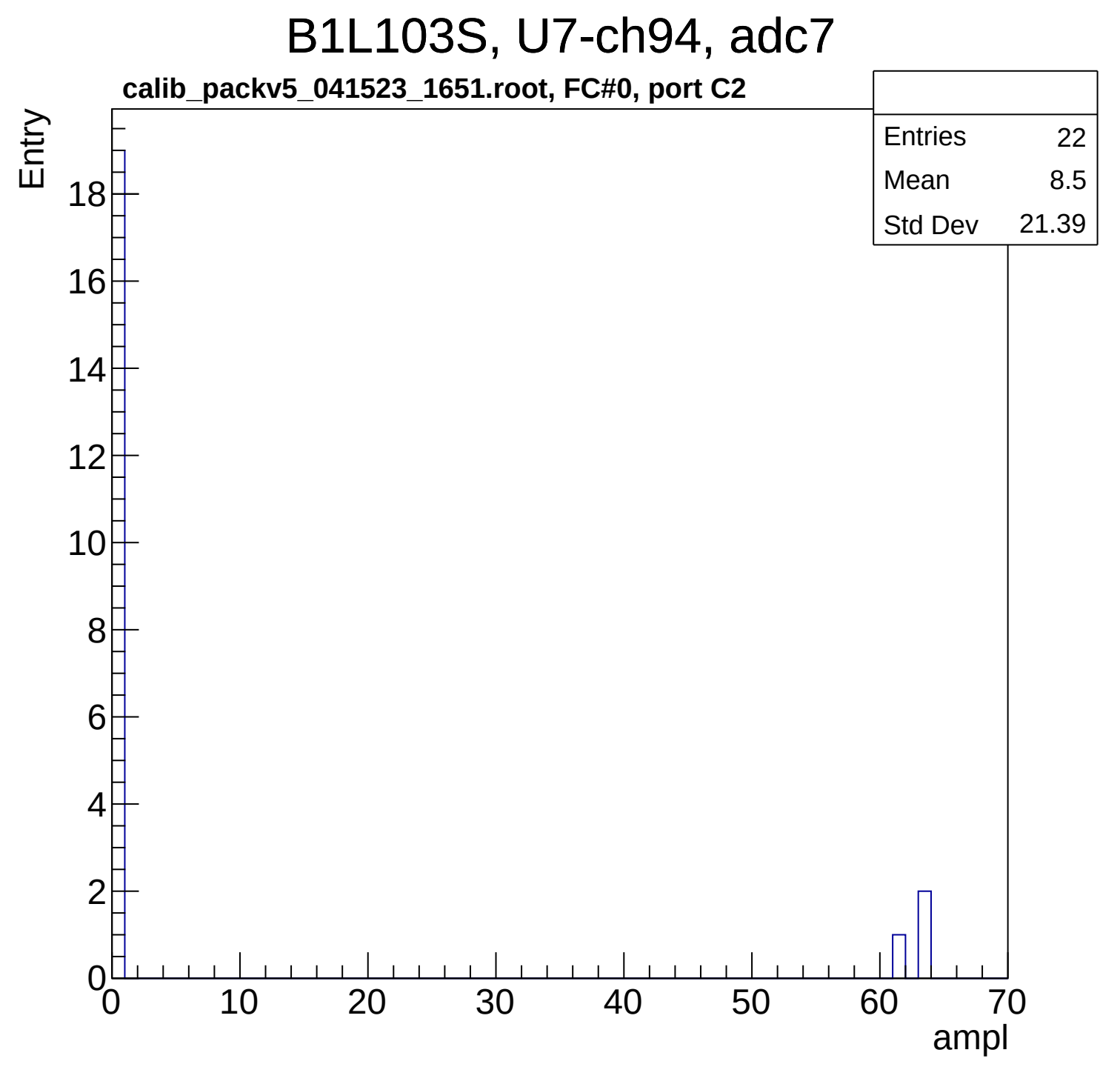
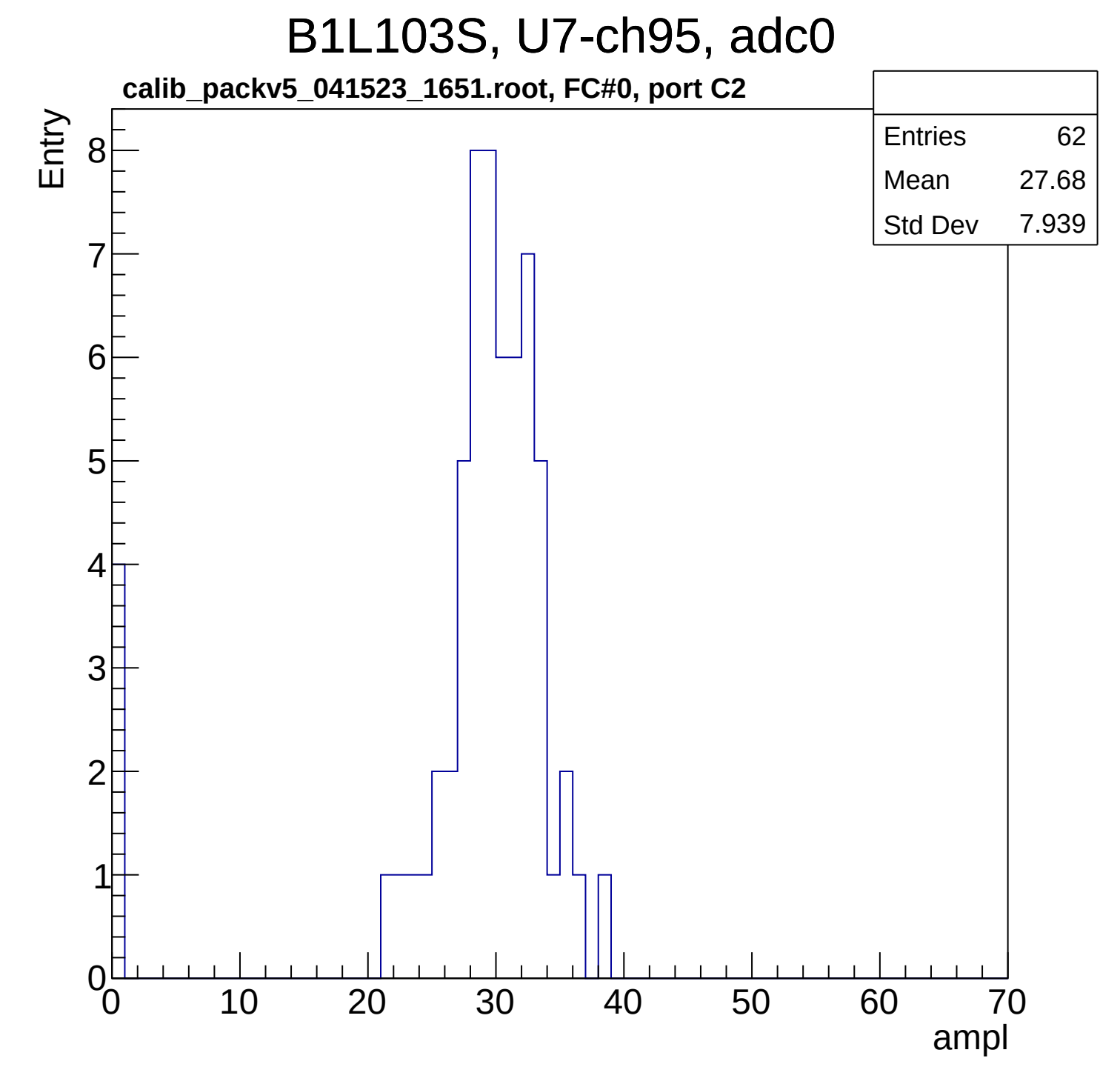
50
60
70


B1L103S, U7-ch94, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 17
Mean 61.29
Std Dev 1.318
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U7-ch94, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 8.5
Std Dev 21.39
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch95, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 27.68
Std Dev 7.939
Entry
ampl
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1
2
3
4
5
6
7
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0
10
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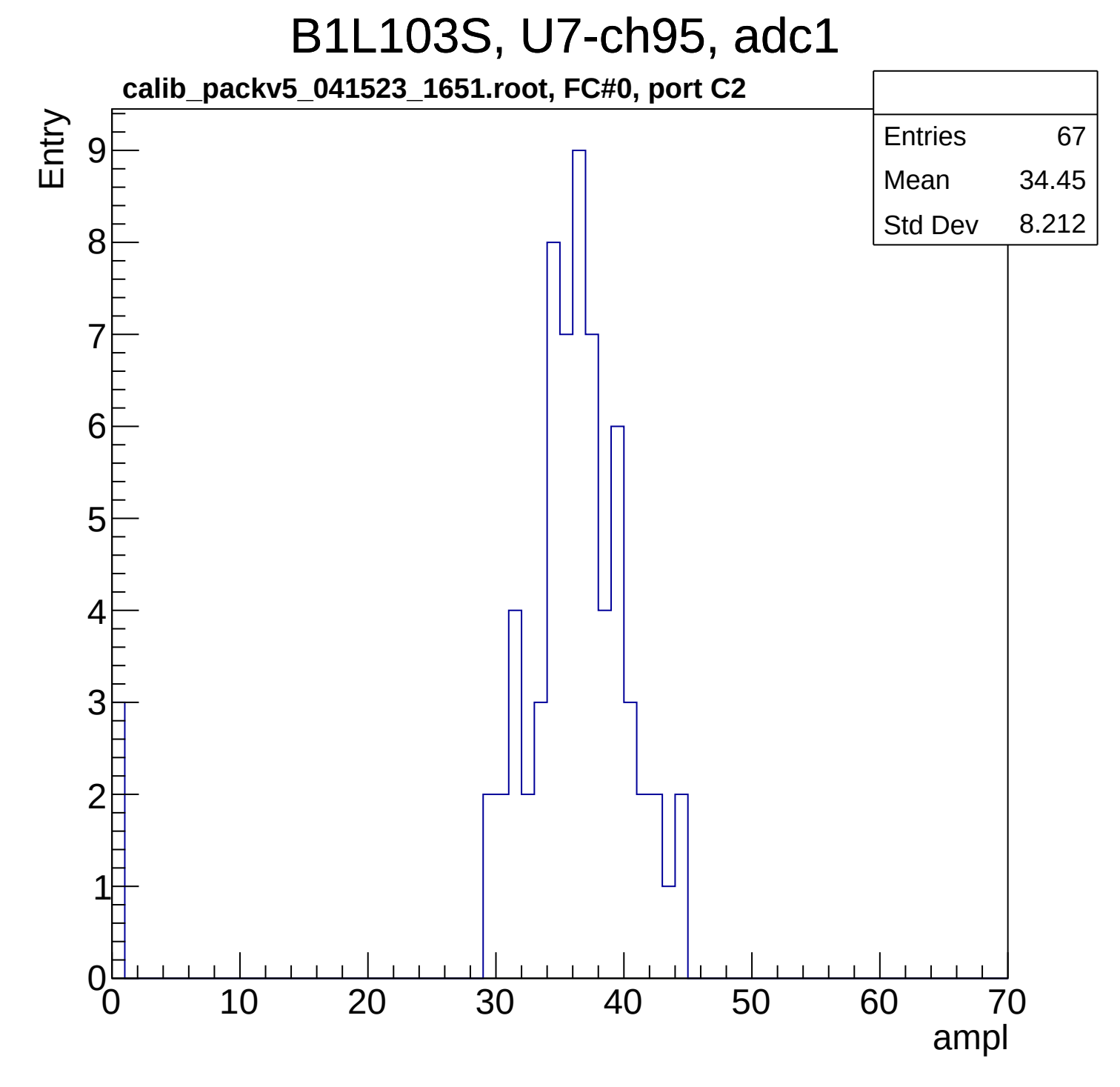
B1L103S, U7-ch95, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 34.45
Std Dev 8.212
Entry
ampl
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2
3
4
5
6
7
8
9
0
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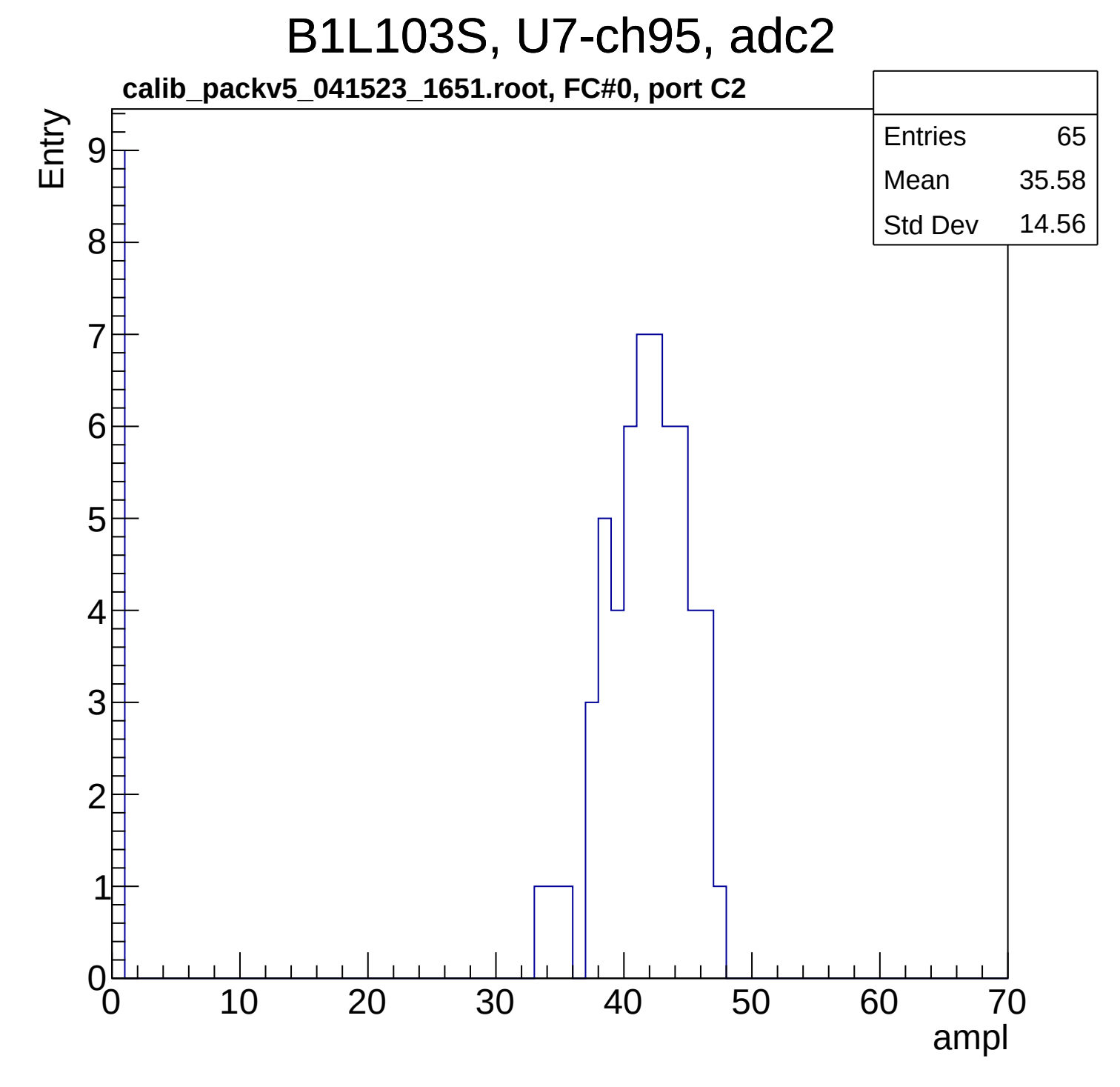
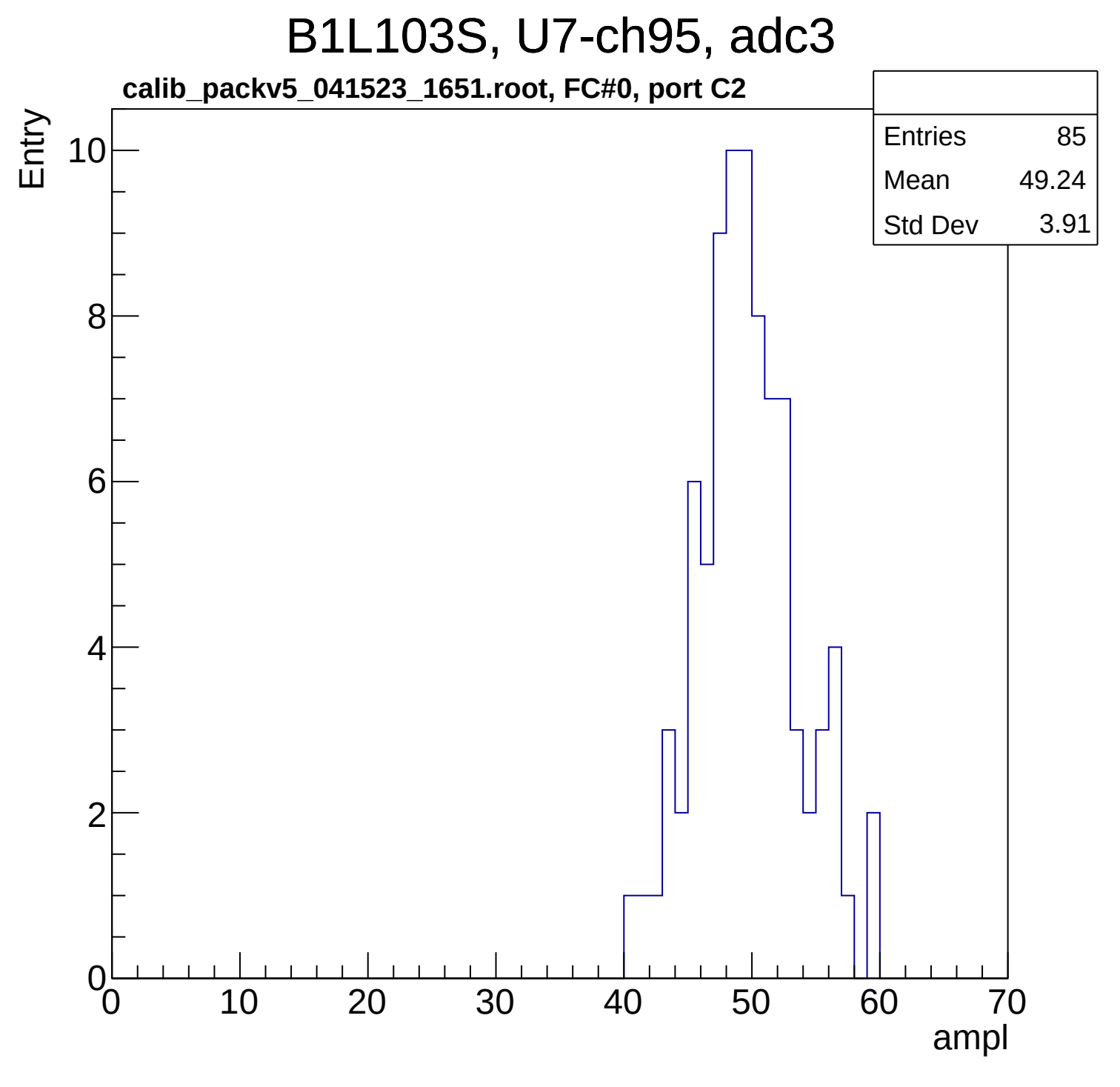
70


B1L103S, U7-ch95, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 35.58
Std Dev 14.56
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U7-ch95, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 49.24
Std Dev 3.91
Entry
ampl
0
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4
6
8
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0
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40
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60
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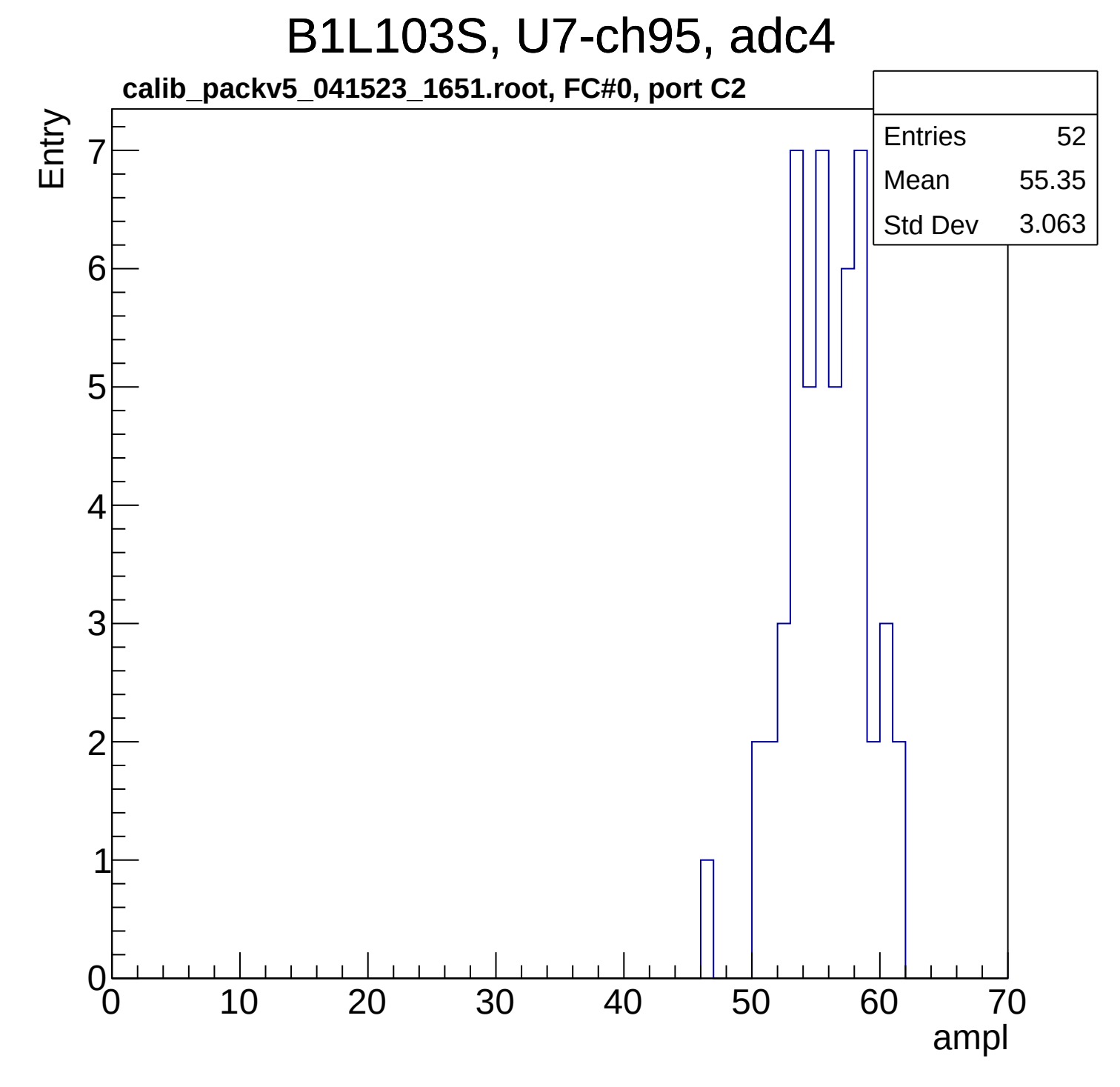
B1L103S, U7-ch95, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 55.35
Std Dev 3.063
Entry
ampl
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2
3
4
5
6
7
0
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20
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40
50
60
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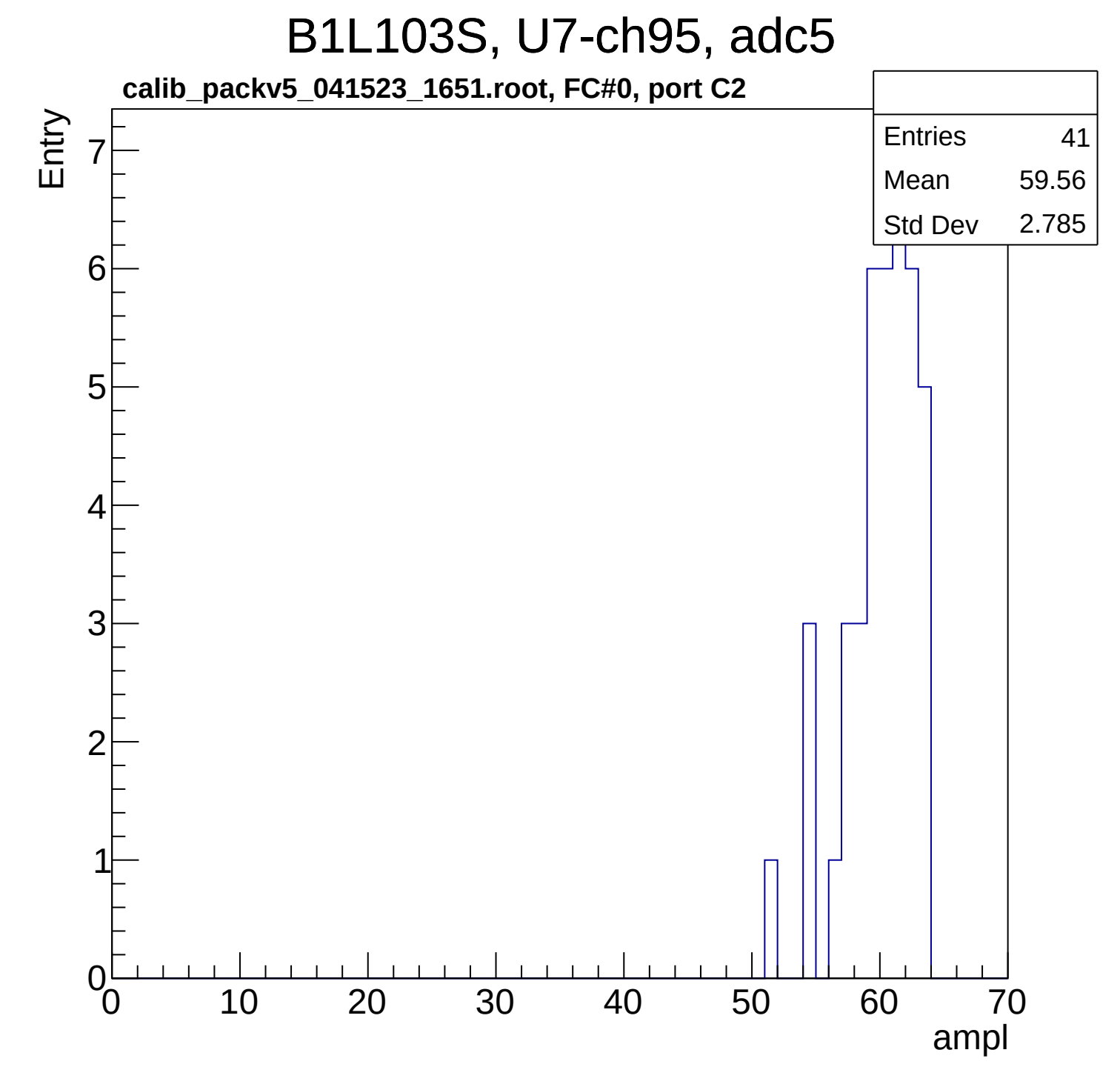
B1L103S, U7-ch95, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 41
Mean 59.56
Std Dev 2.785
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ampl
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4
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0
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20
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40
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60
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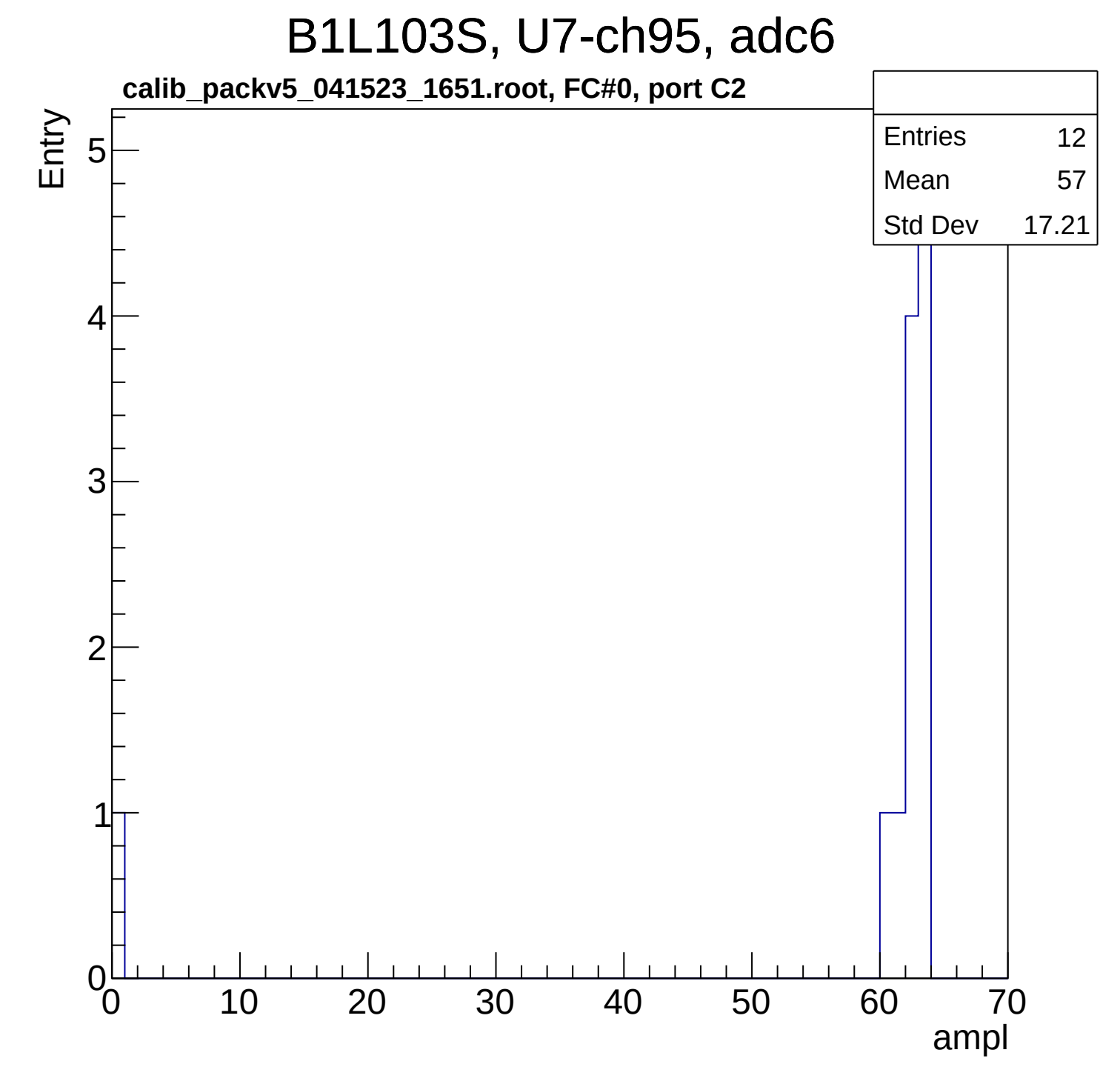
B1L103S, U7-ch95, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 57
Std Dev 17.21
Entry
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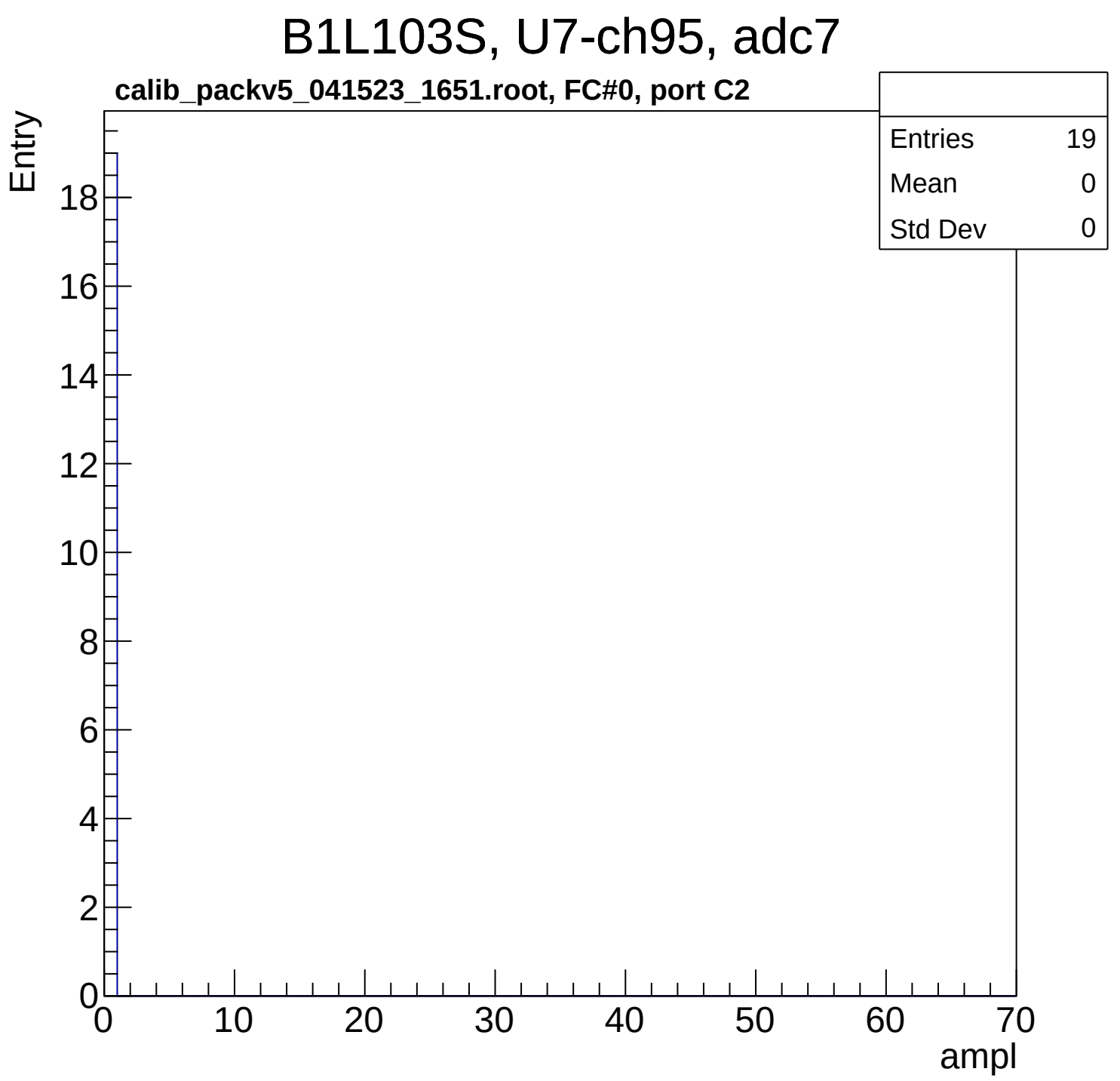
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch95, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
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2
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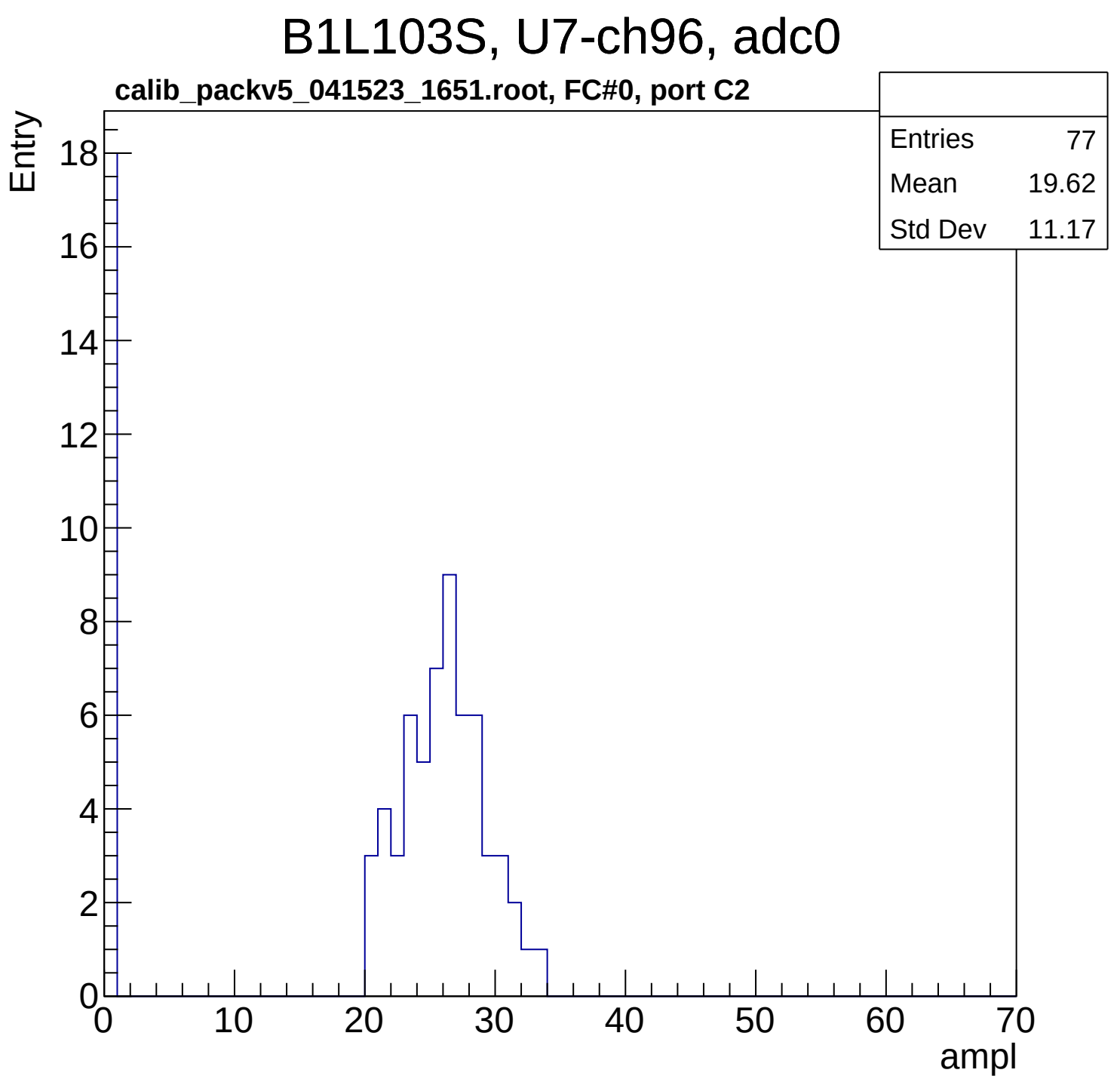
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch96, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 19.62
Std Dev 11.17
Entry
0
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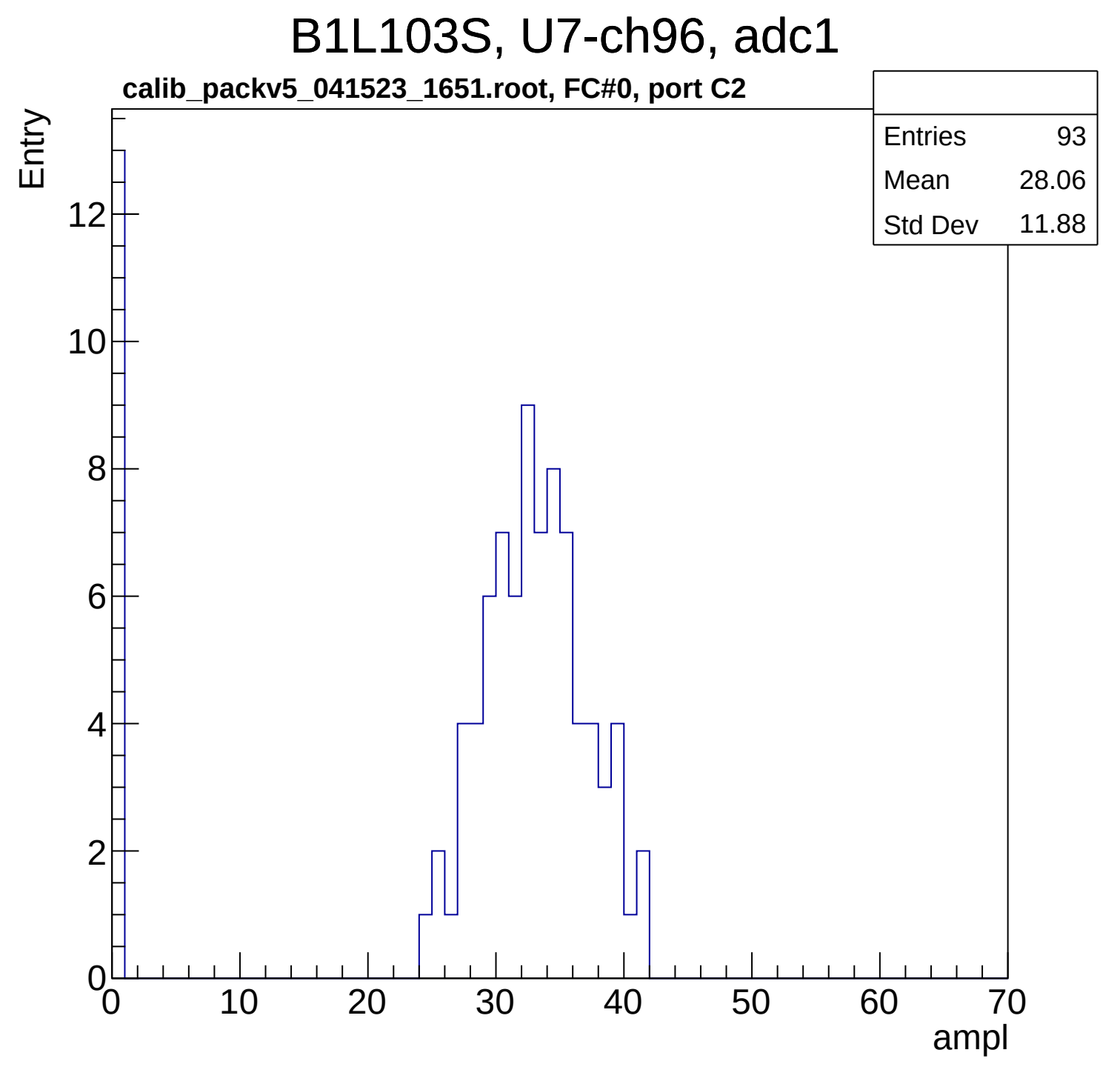
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch96, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 93
Mean 28.06
Std Dev 11.88
Entry
ampl
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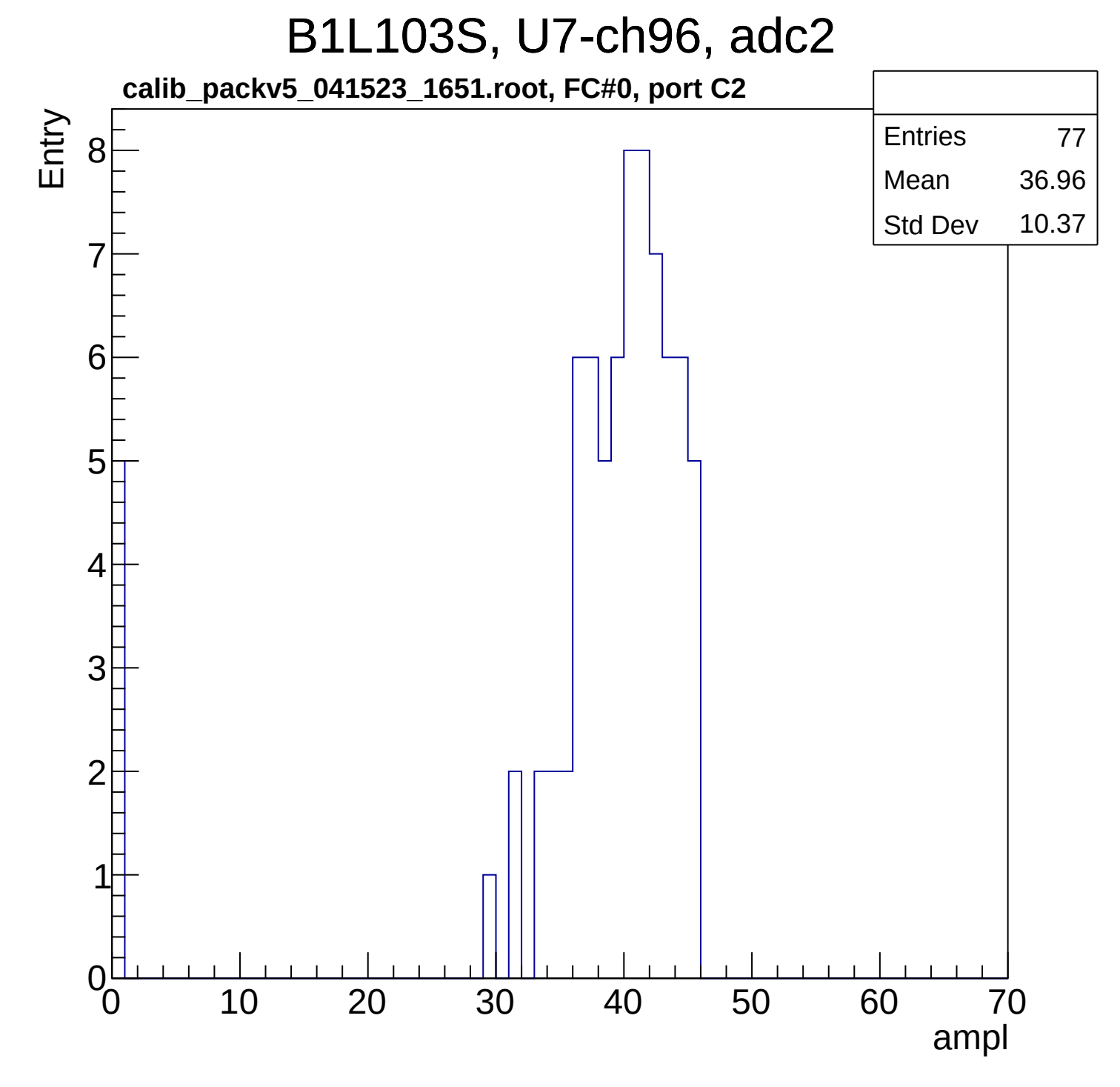
2
4
6
8
10
12
0
10
20
30
40
50
60
70


B1L103S, U7-ch96, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 36.96
Std Dev 10.37
Entry
ampl
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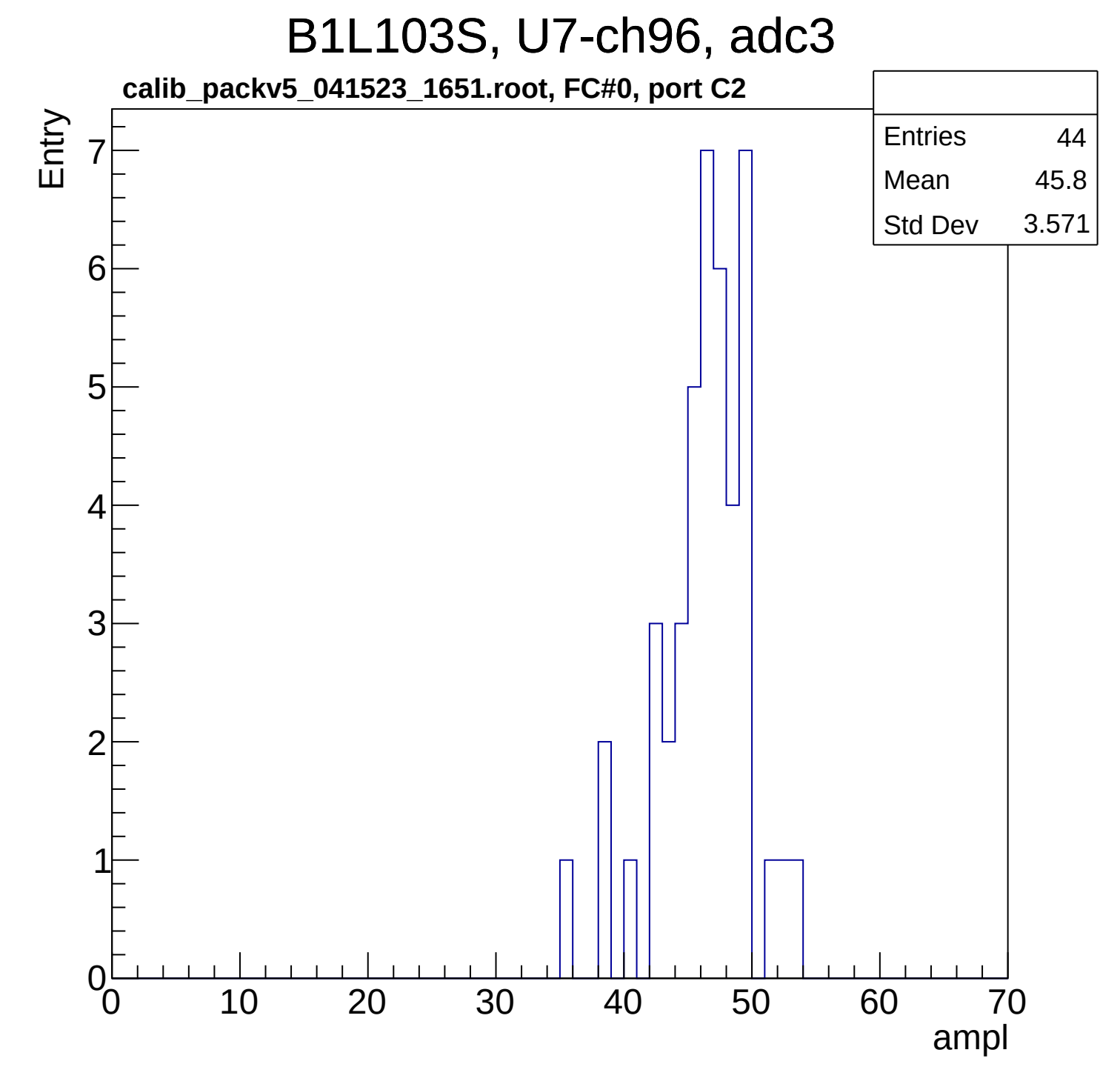
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch96, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 45.8
Std Dev 3.571
Entry
ampl
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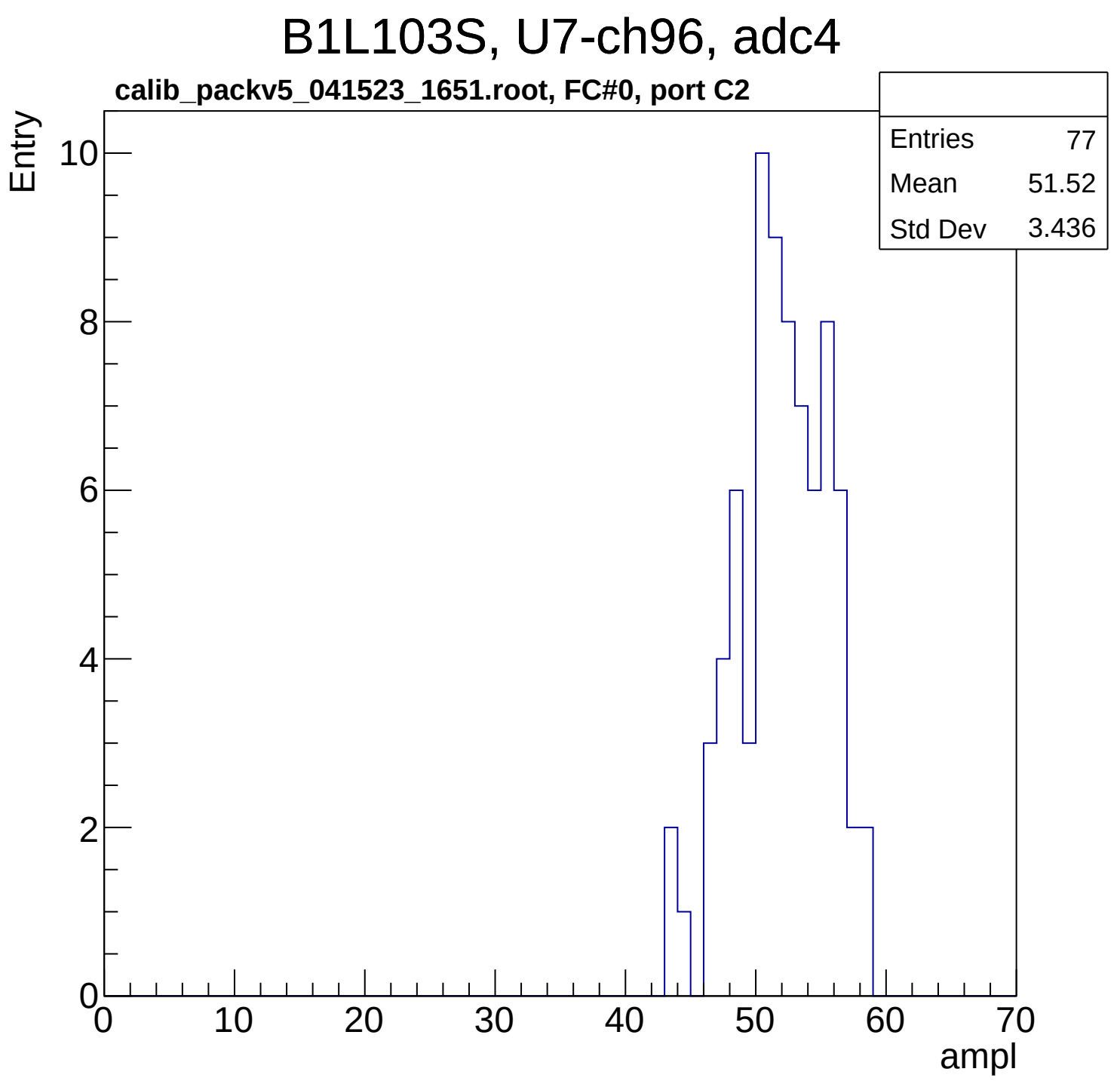
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U7-ch96, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 51.52
Std Dev 3.436
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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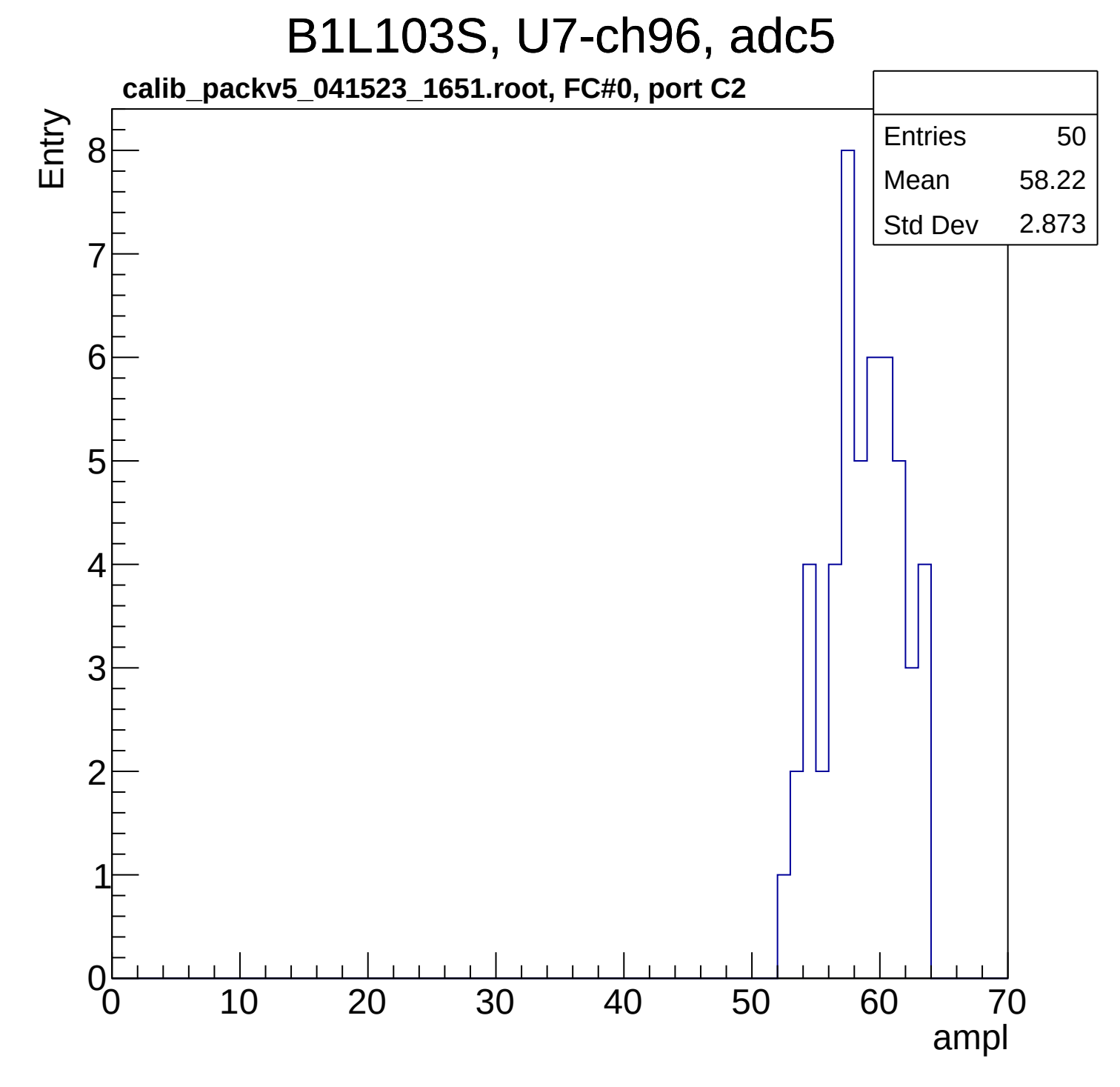
B1L103S, U7-ch96, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 58.22
Std Dev 2.873
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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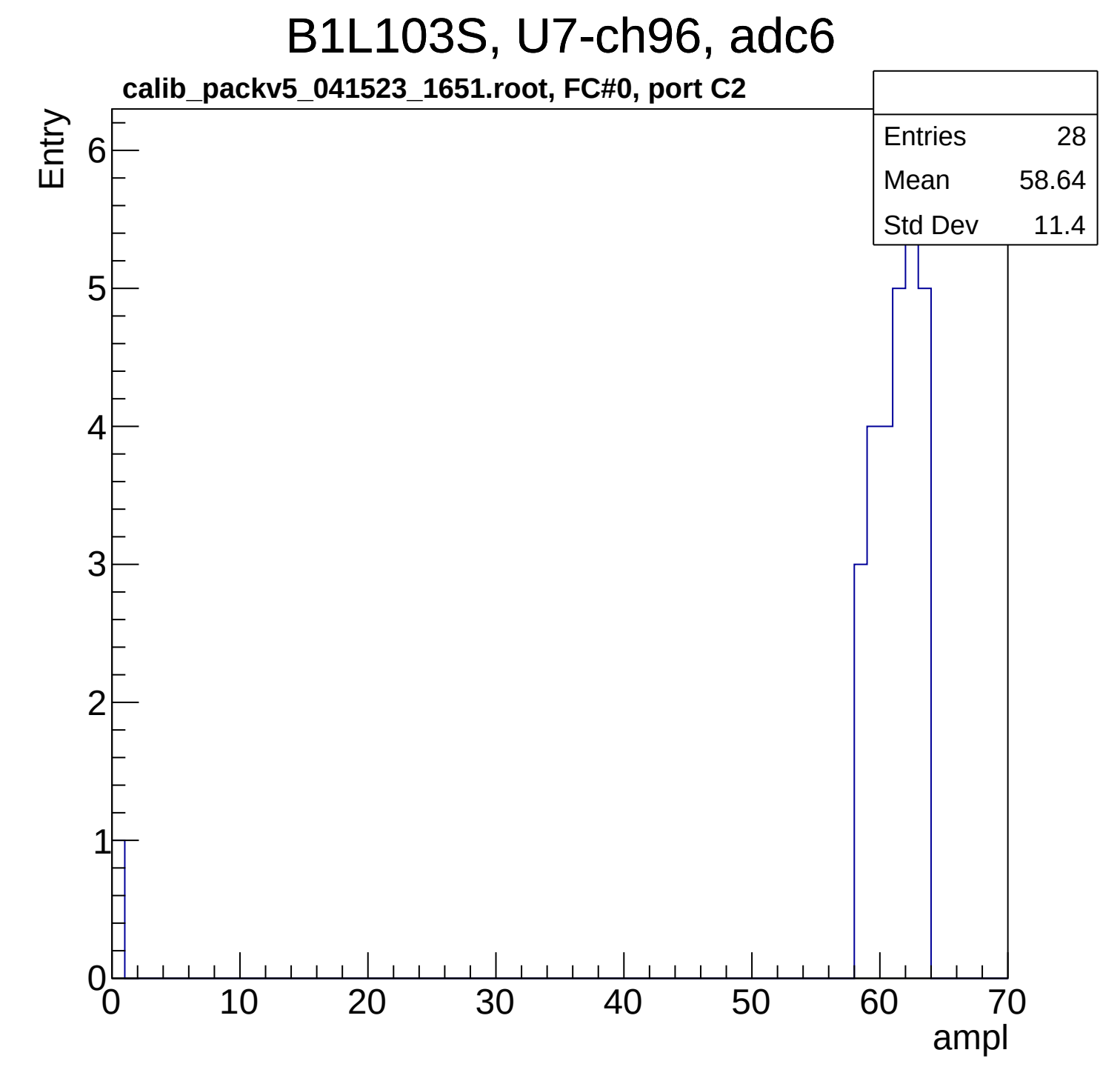
B1L103S, U7-ch96, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 28
Mean 58.64
Std Dev 11.4
Entry
0
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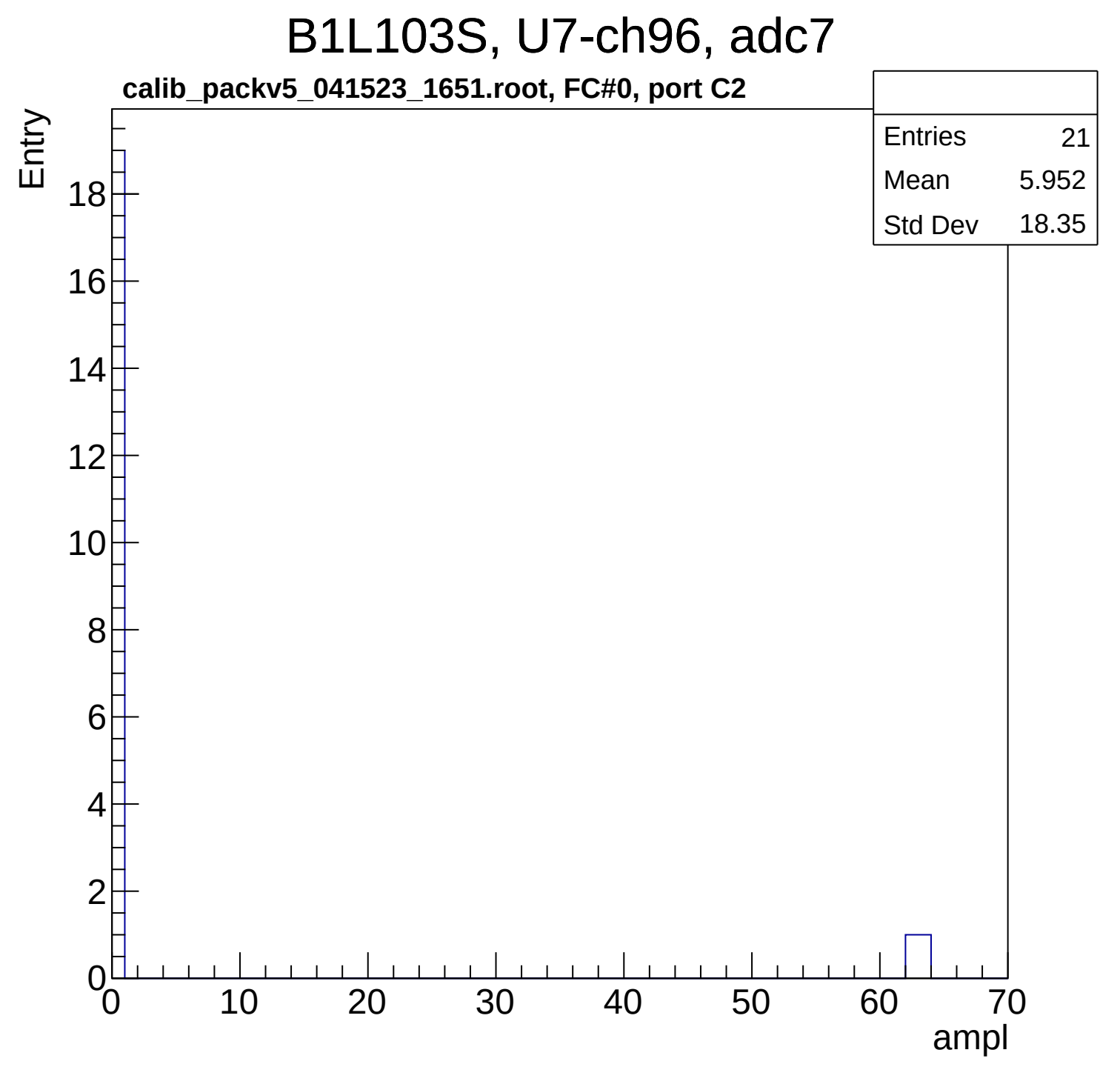
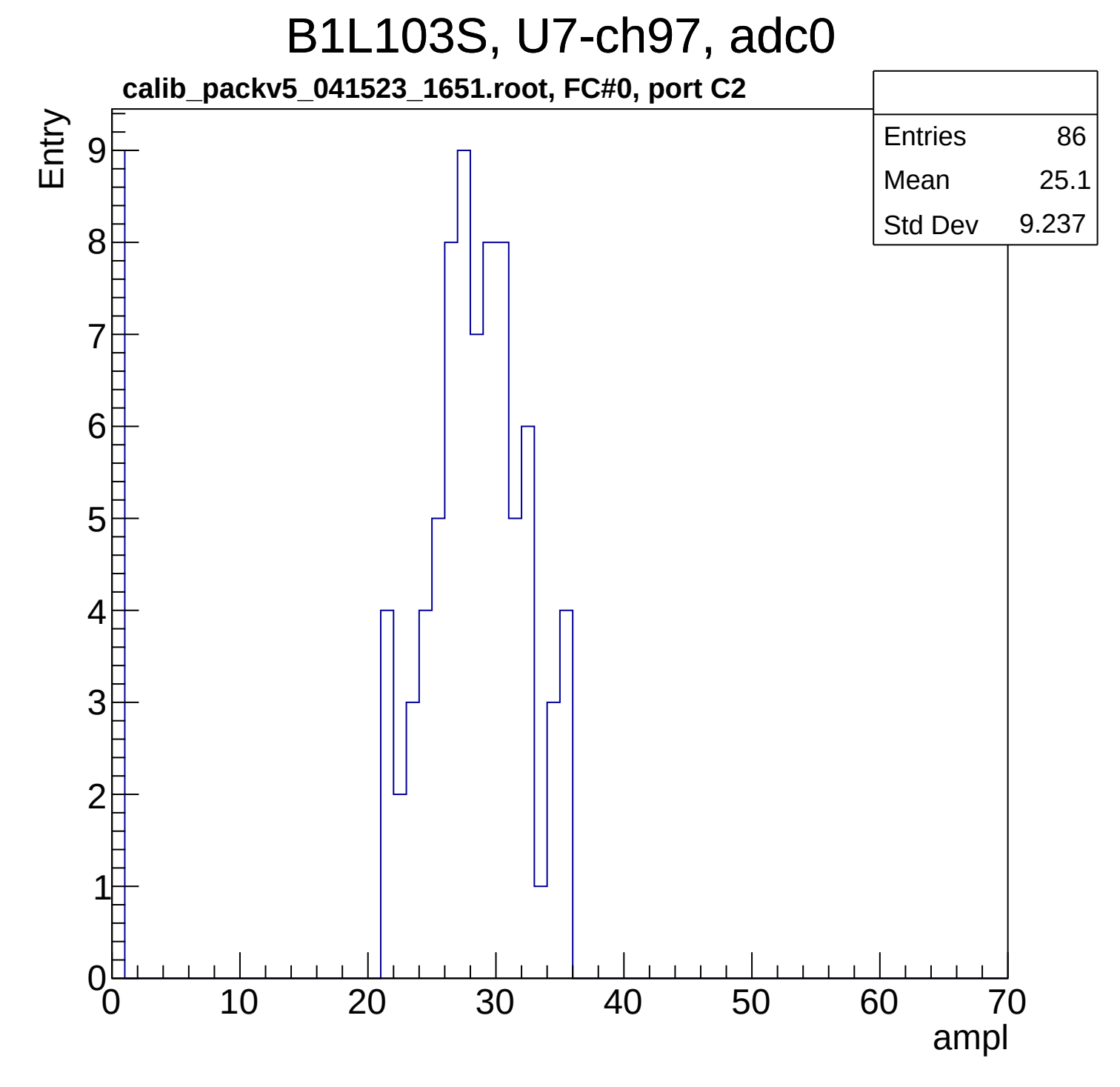
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch96, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 5.952
Std Dev 18.35
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch97, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 25.1
Std Dev 9.237
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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60
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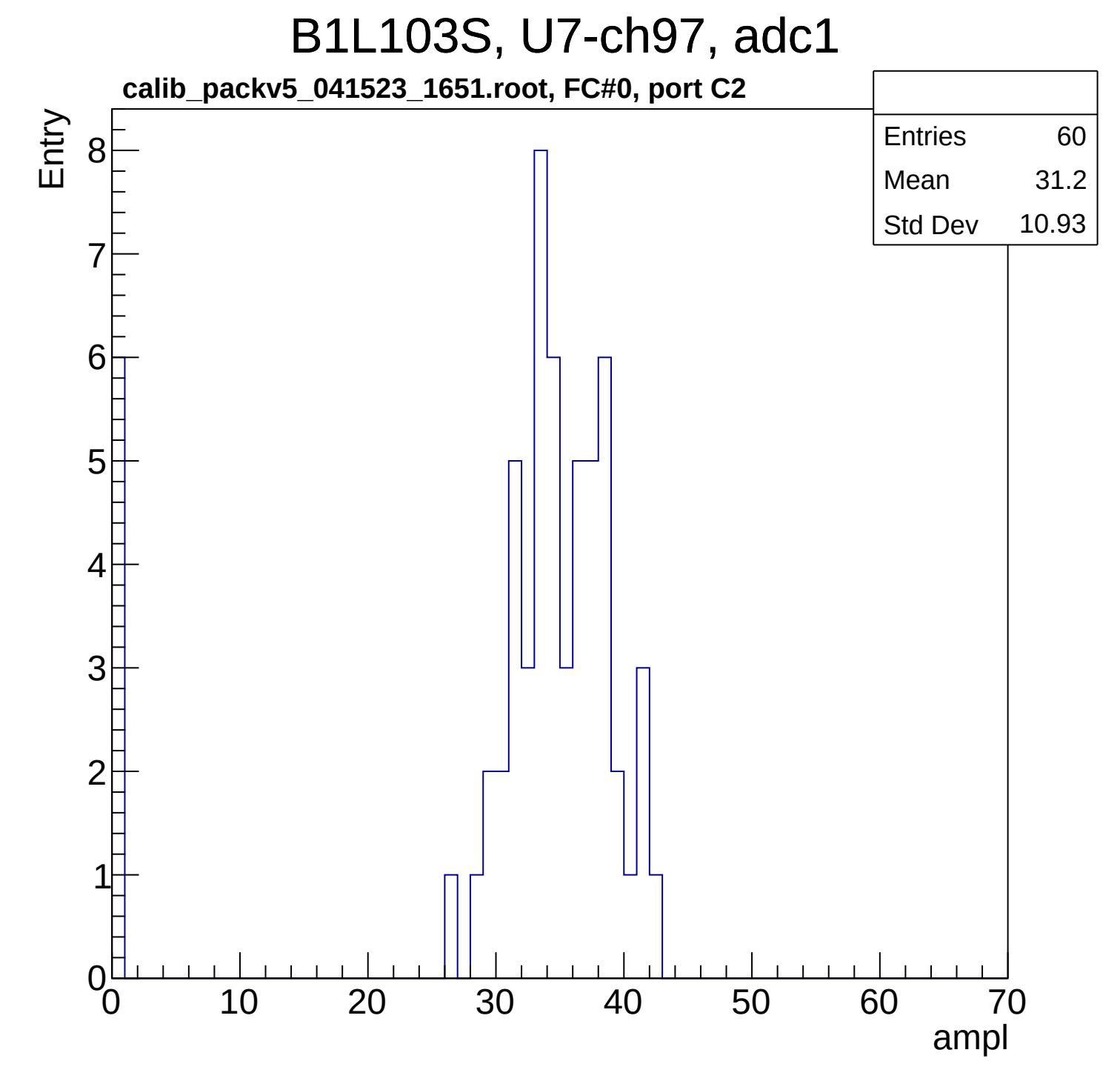
B1L103S, U7-ch97, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 31.2
Std Dev 10.93
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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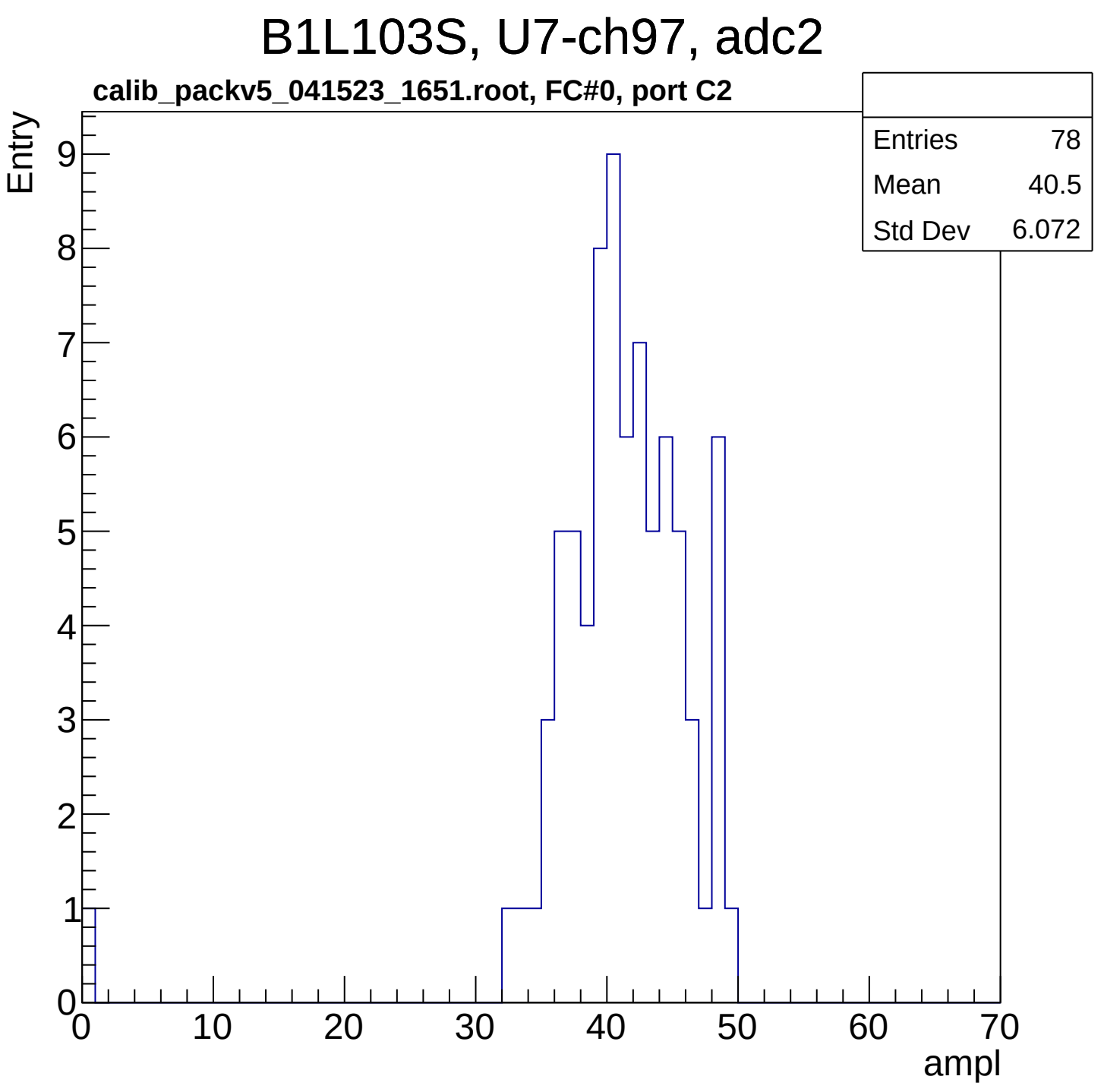
B1L103S, U7-ch97, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 40.5
Std Dev 6.072
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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40
50
60
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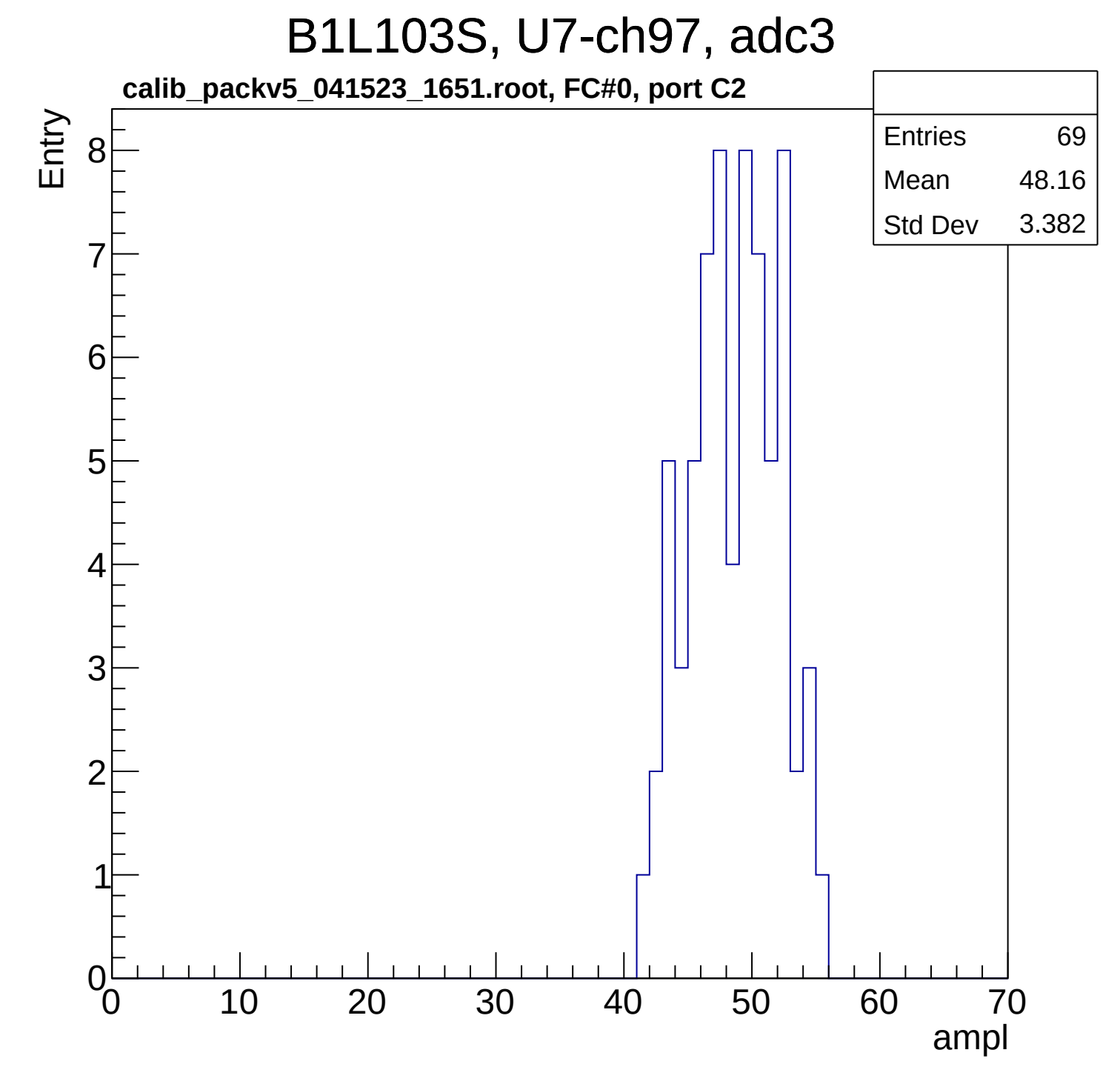
B1L103S, U7-ch97, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 48.16
Std Dev 3.382
Entry
ampl
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2
3
4
5
6
7
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0
10
20
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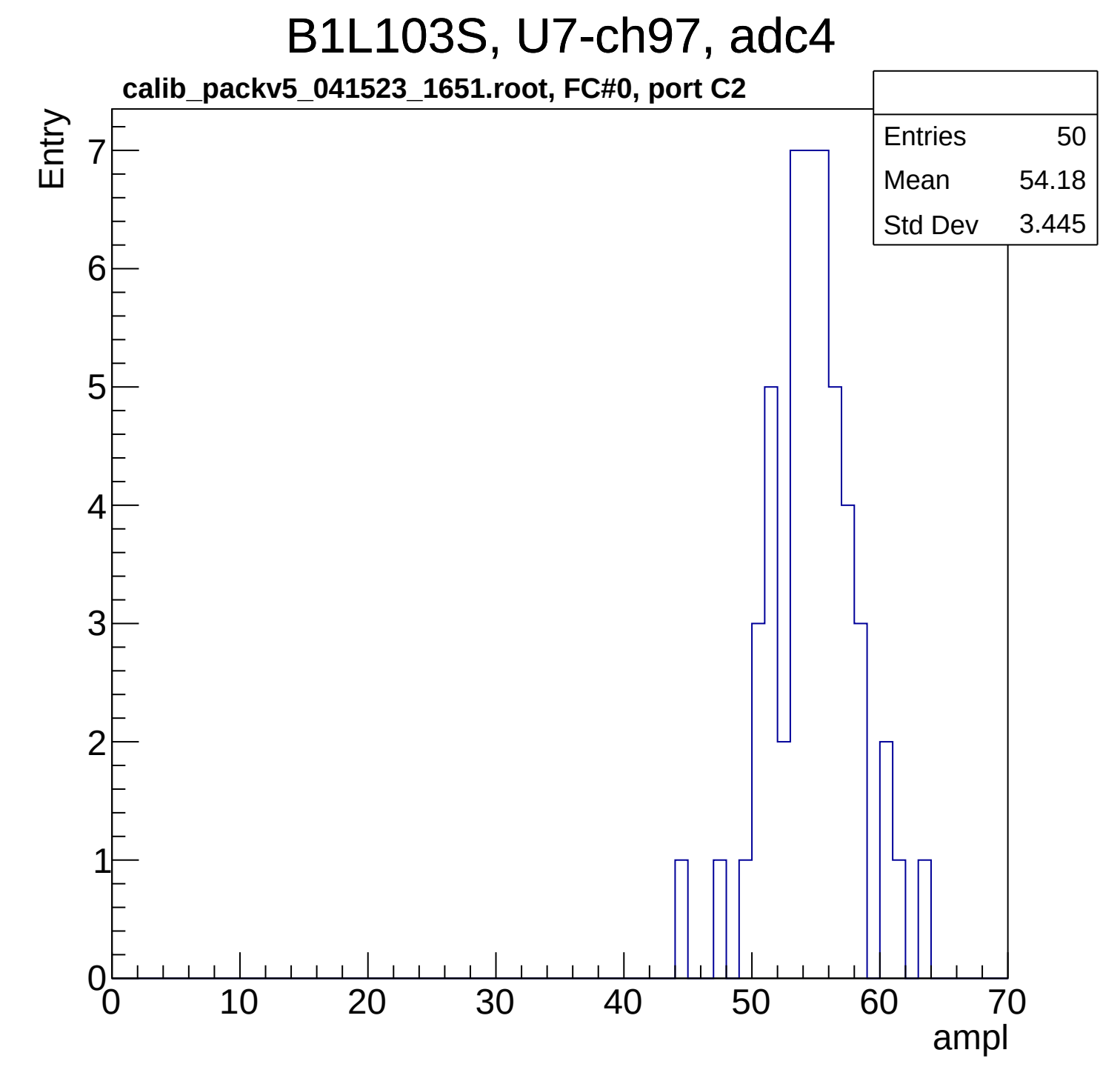
40
50
60
70


B1L103S, U7-ch97, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 54.18
Std Dev 3.445
Entry
ampl
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1
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3
4
5
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0
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20
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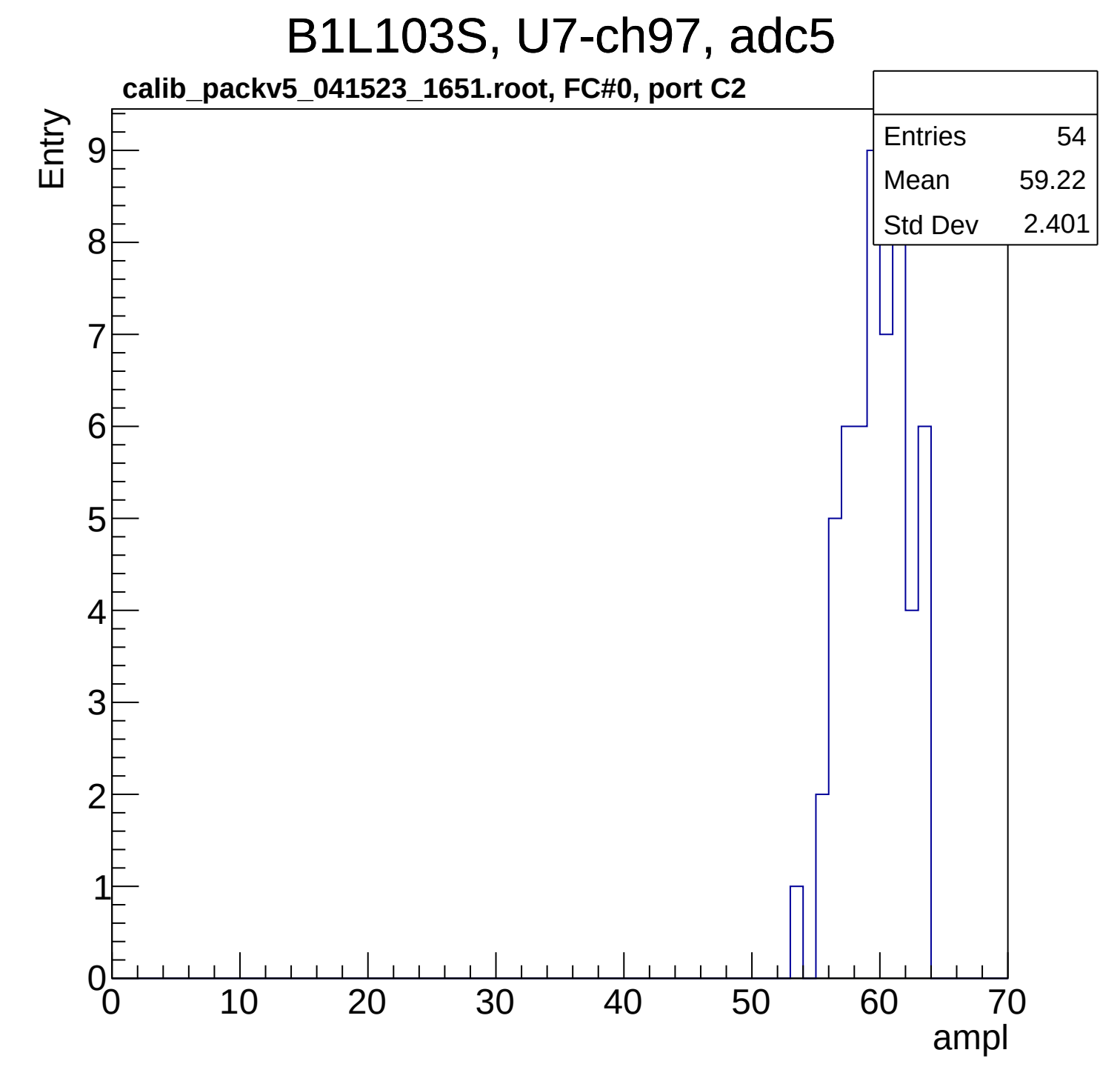
40
50
60
70


B1L103S, U7-ch97, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 59.22
Std Dev 2.401
Entry
ampl
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2
3
4
5
6
7
8
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0
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20
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50
60
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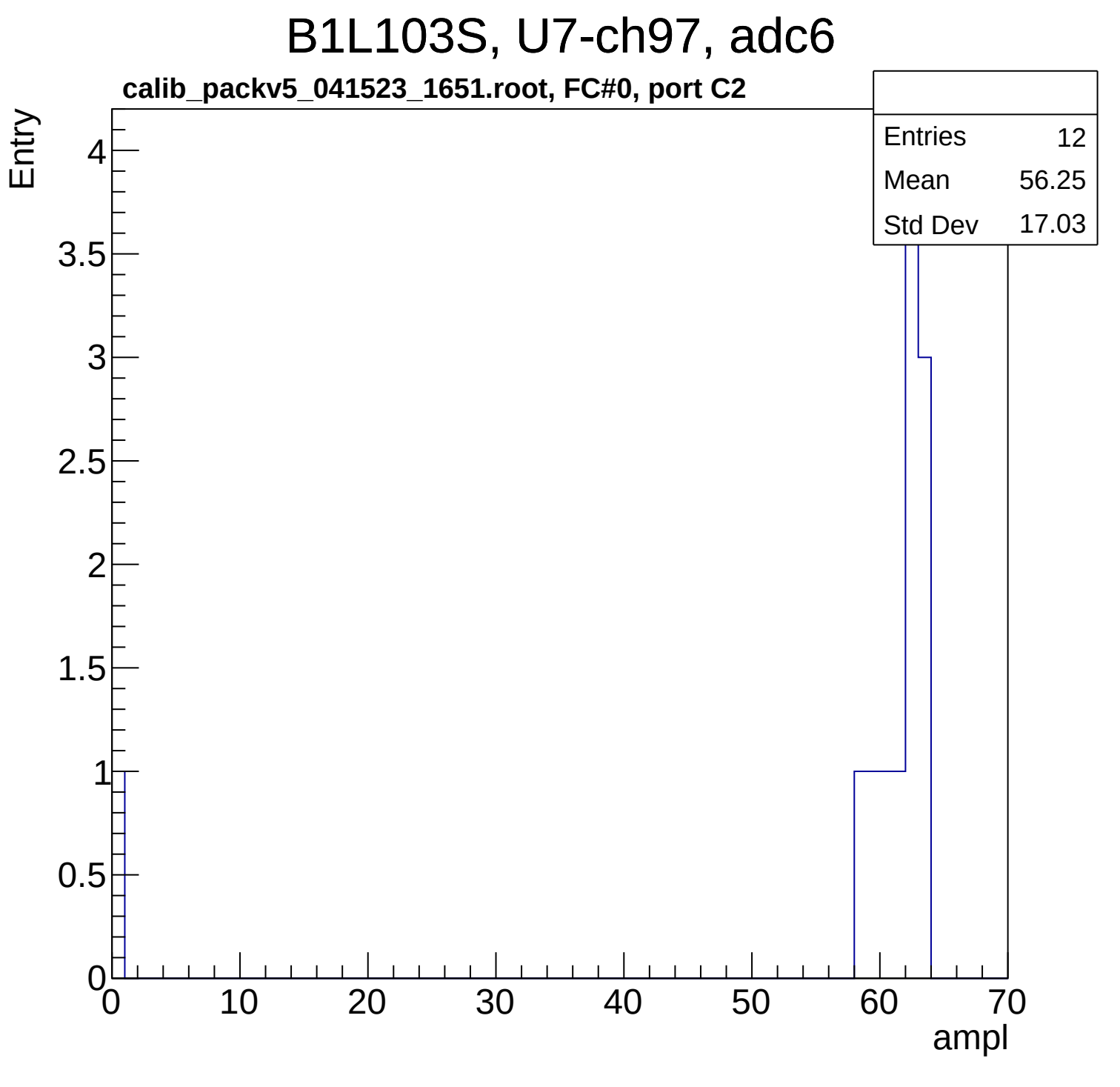
B1L103S, U7-ch97, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 56.25
Std Dev 17.03
Entry
ampl
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1.5
2
2.5
3
3.5
4
0
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60
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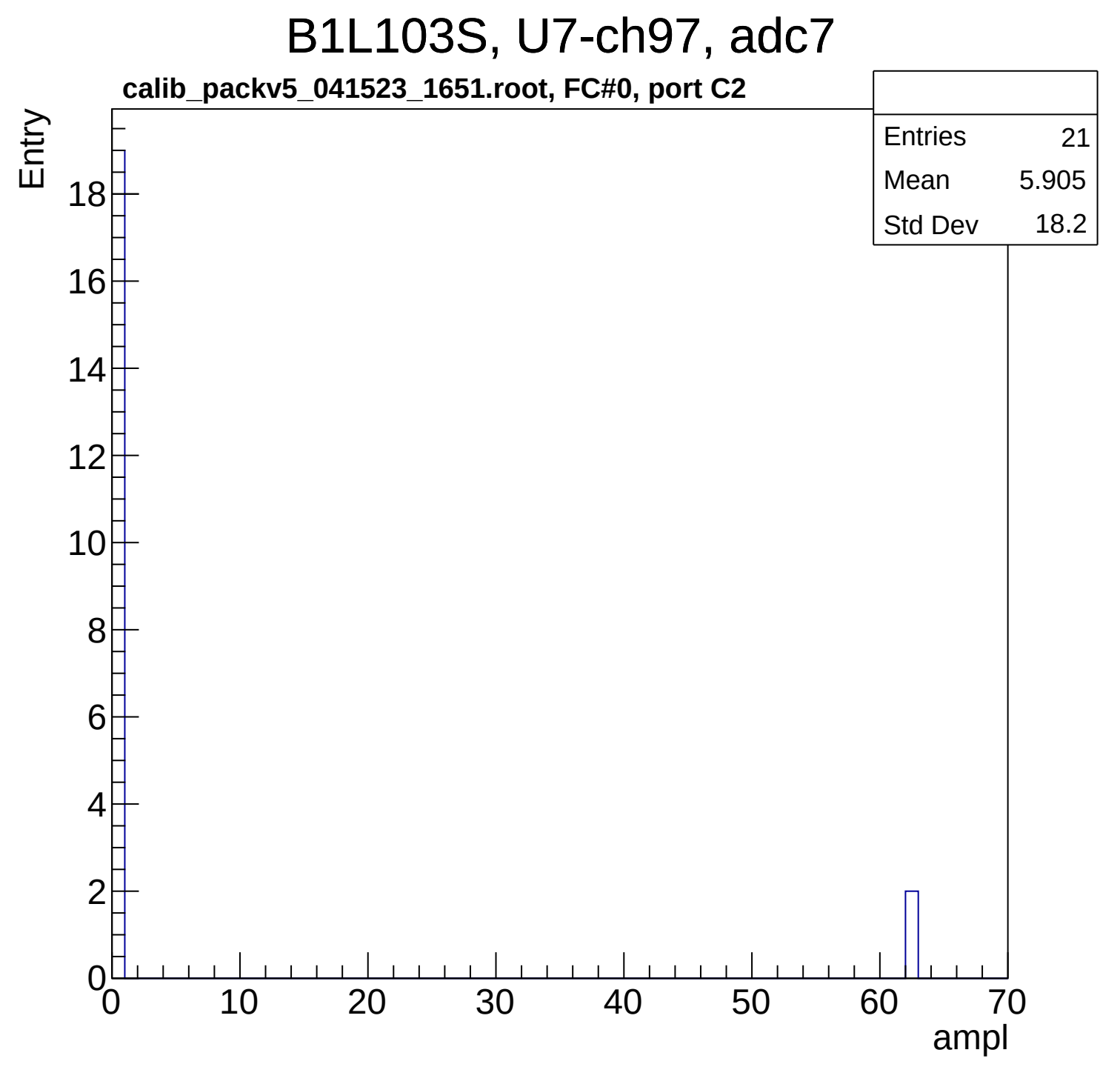
B1L103S, U7-ch97, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 5.905
Std Dev 18.2
Entry
0
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6
8
10
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14
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50
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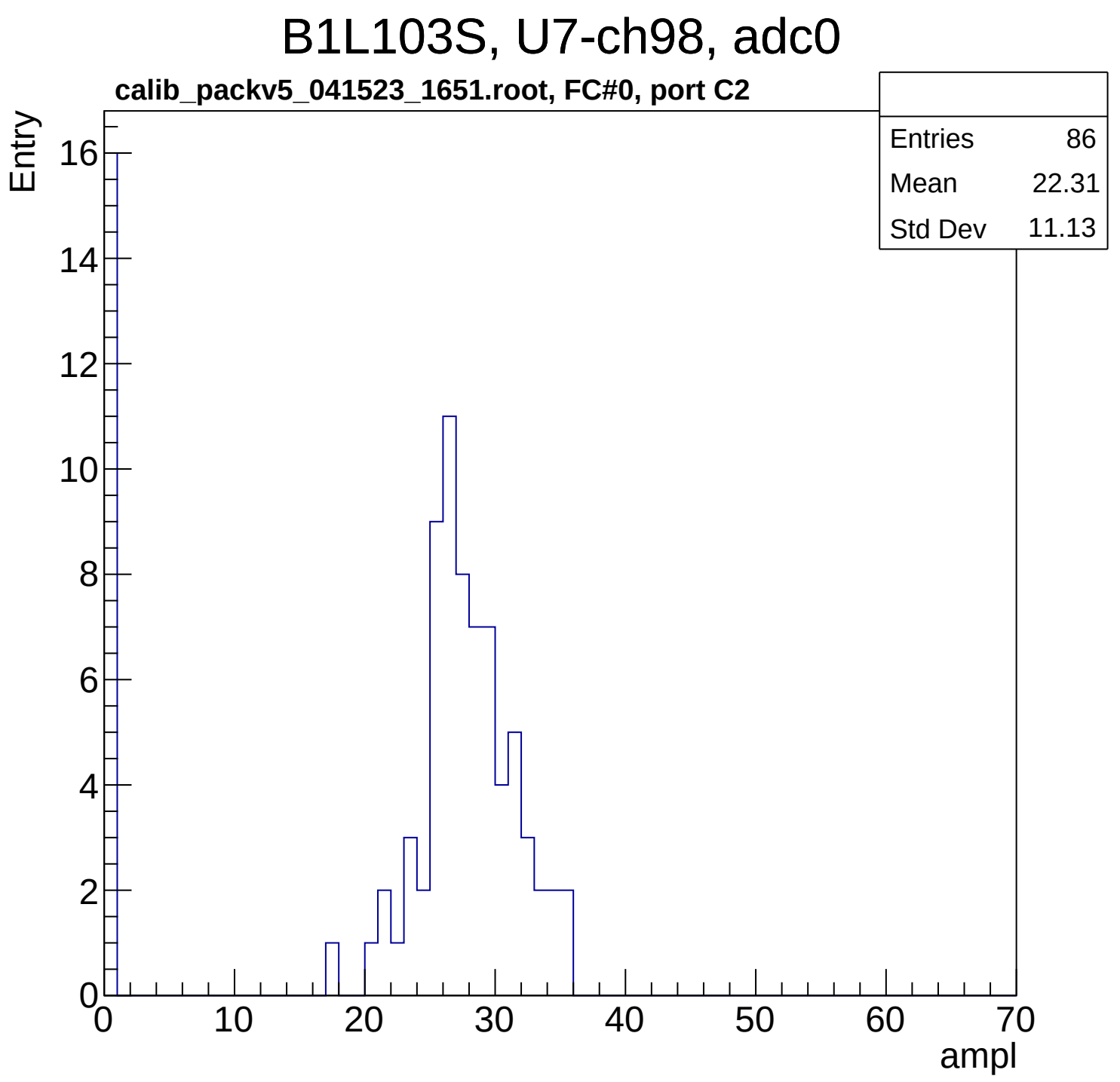
70
ampl


B1L103S, U7-ch98, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 22.31
Std Dev 11.13
Entry
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4
6
8
10
12
14
16
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10
20
30
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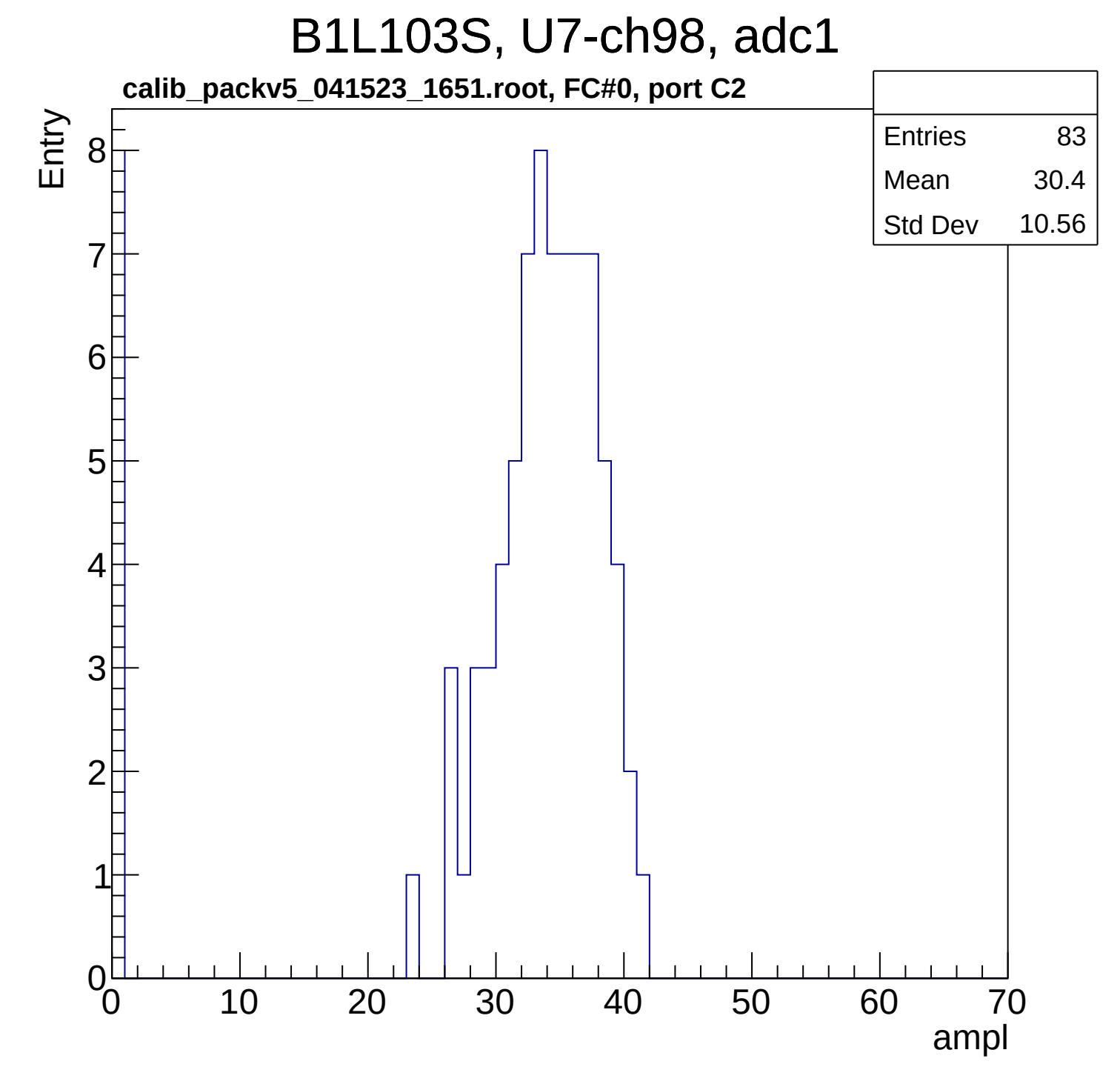
50
60
70
ampl


B1L103S, U7-ch98, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 30.4
Std Dev 10.56
Entry
ampl
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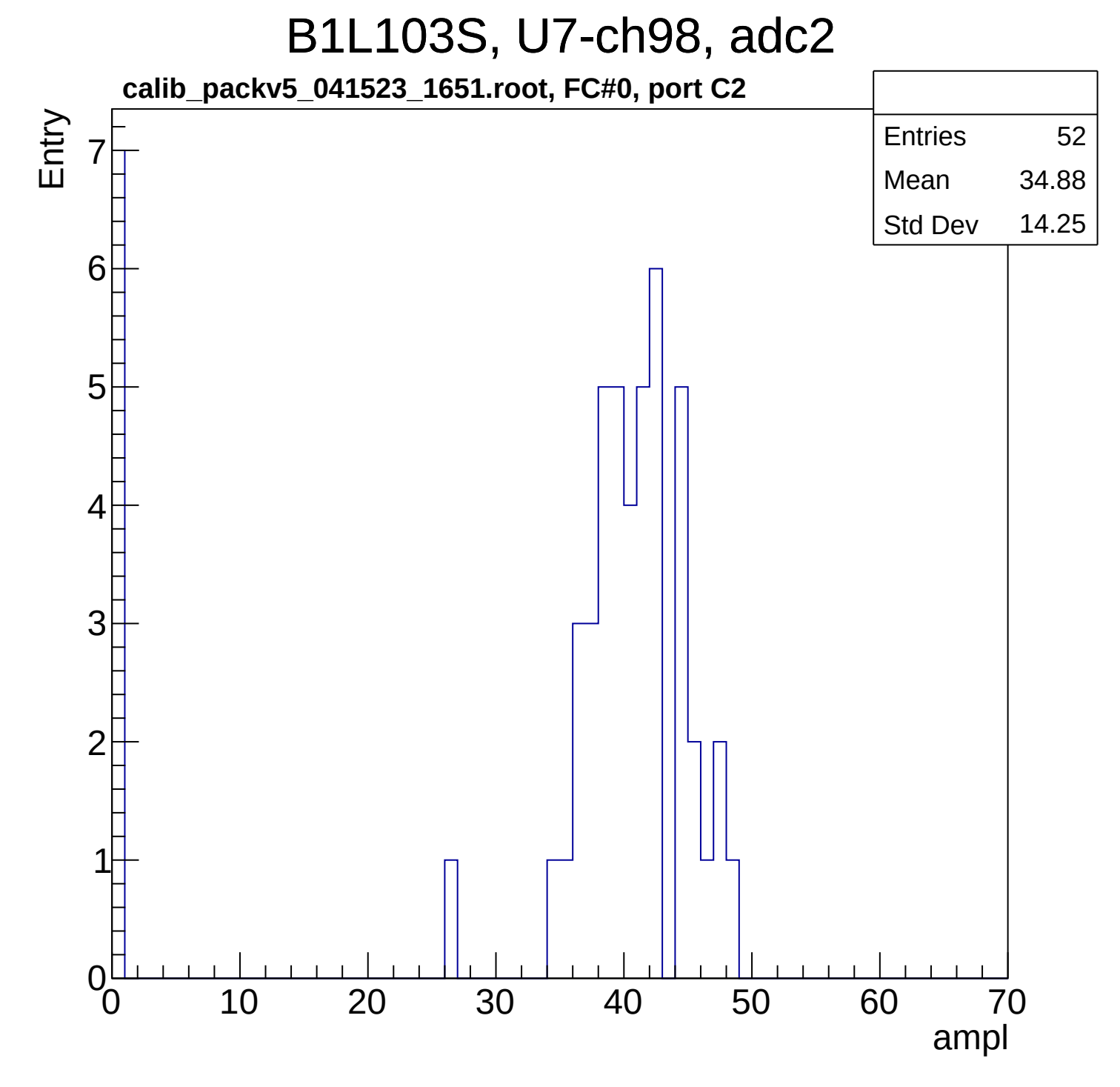
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch98, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 34.88
Std Dev 14.25
Entry
ampl
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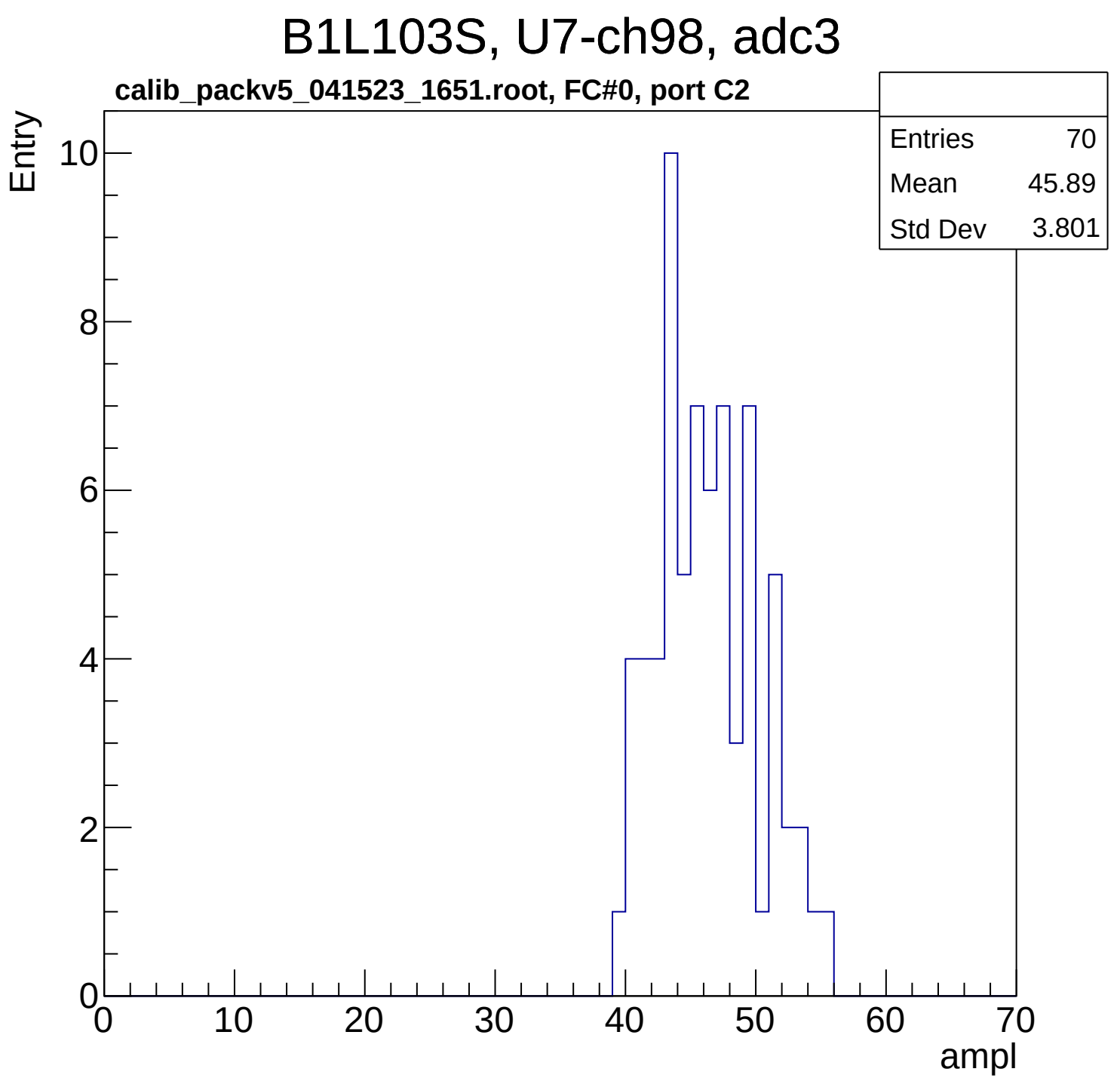
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U7-ch98, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 45.89
Std Dev 3.801
Entry
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10
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10
20
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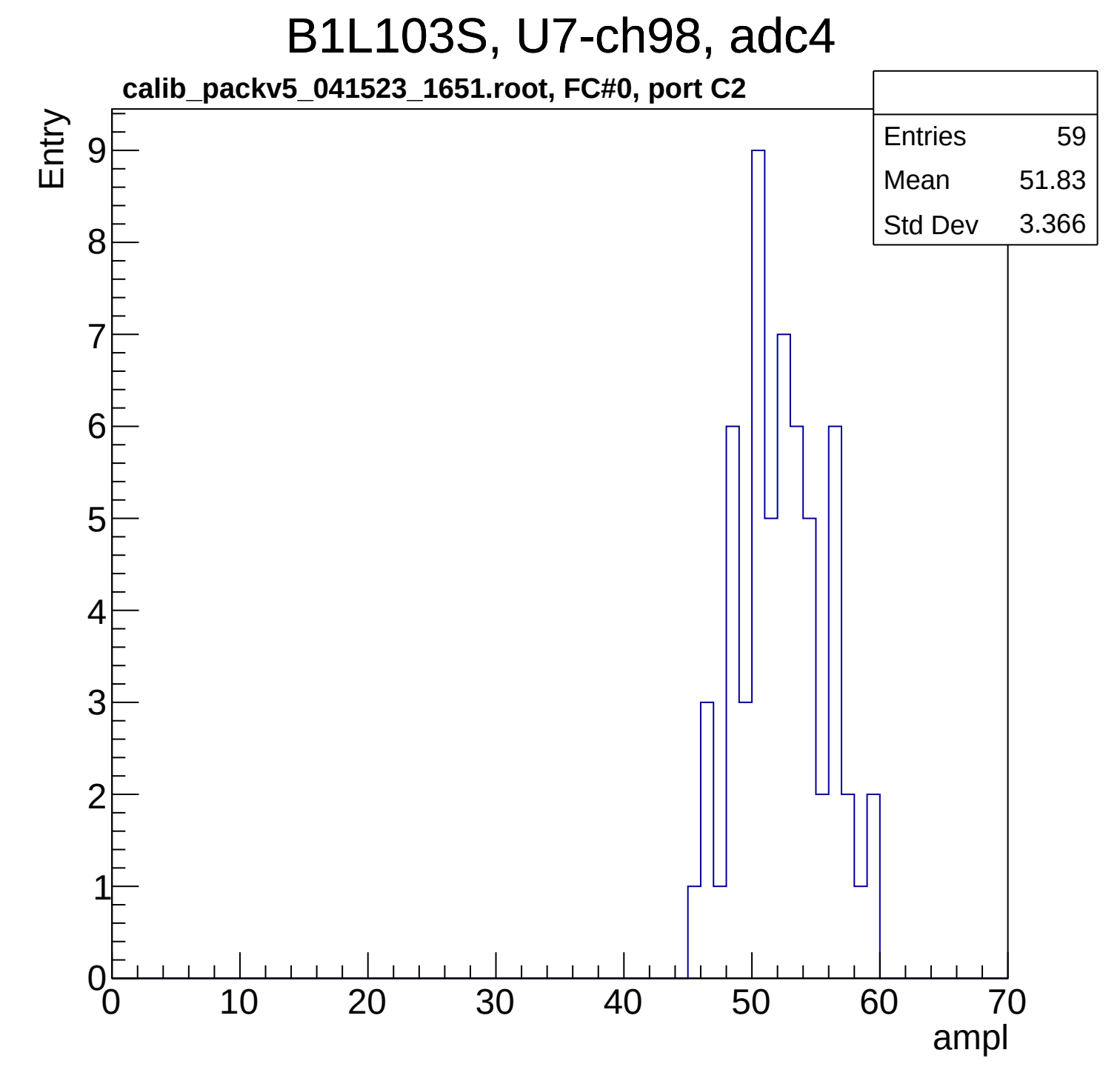
50
60
70
ampl


B1L103S, U7-ch98, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 51.83
Std Dev 3.366
Entry
ampl
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5
6
7
8
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0
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60
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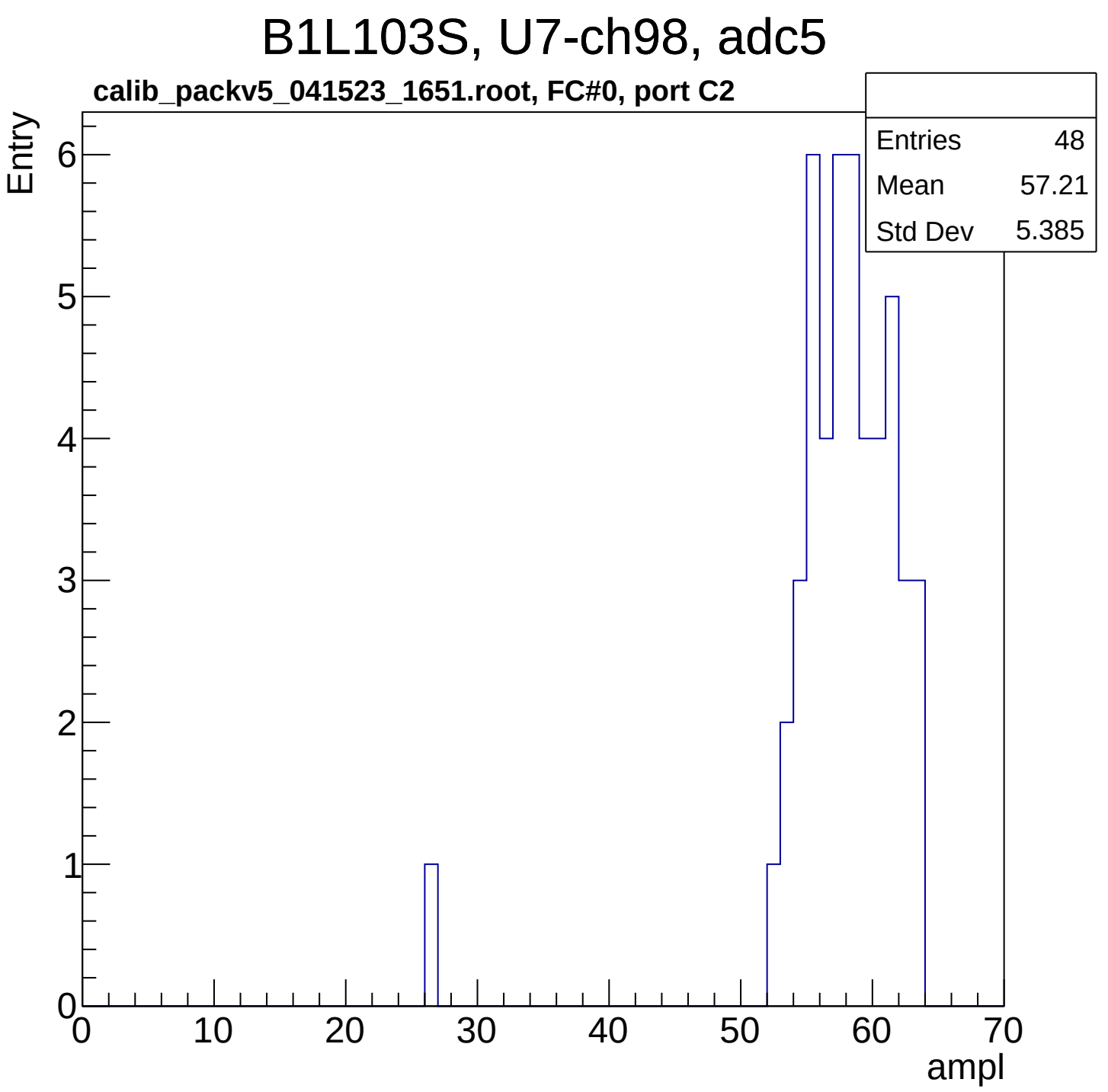
B1L103S, U7-ch98, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 57.21
Std Dev 5.385
Entry
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6
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20
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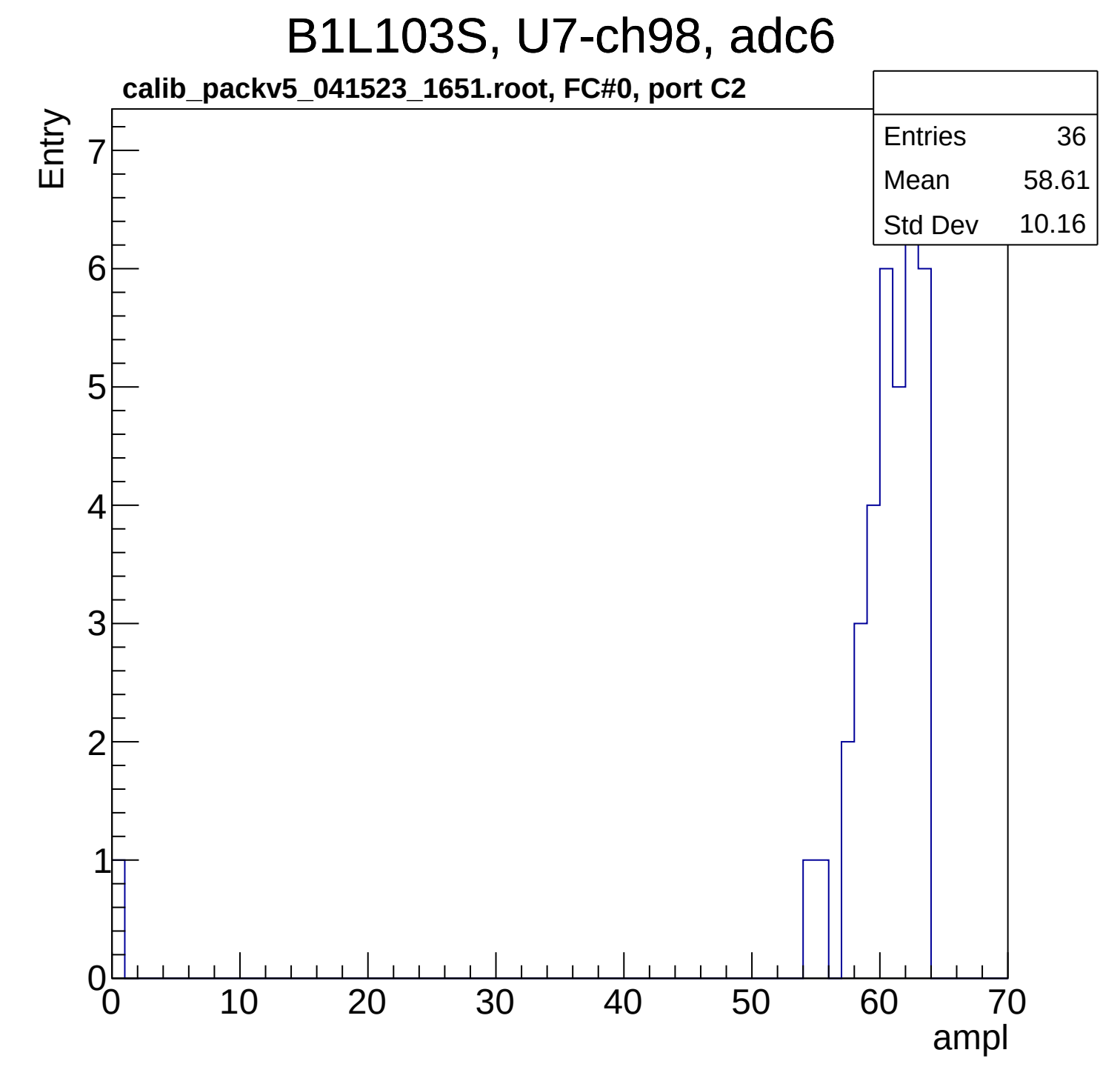
50
60
70
ampl


B1L103S, U7-ch98, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 36
Mean 58.61
Std Dev 10.16
Entry
ampl
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4
5
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7
0
10
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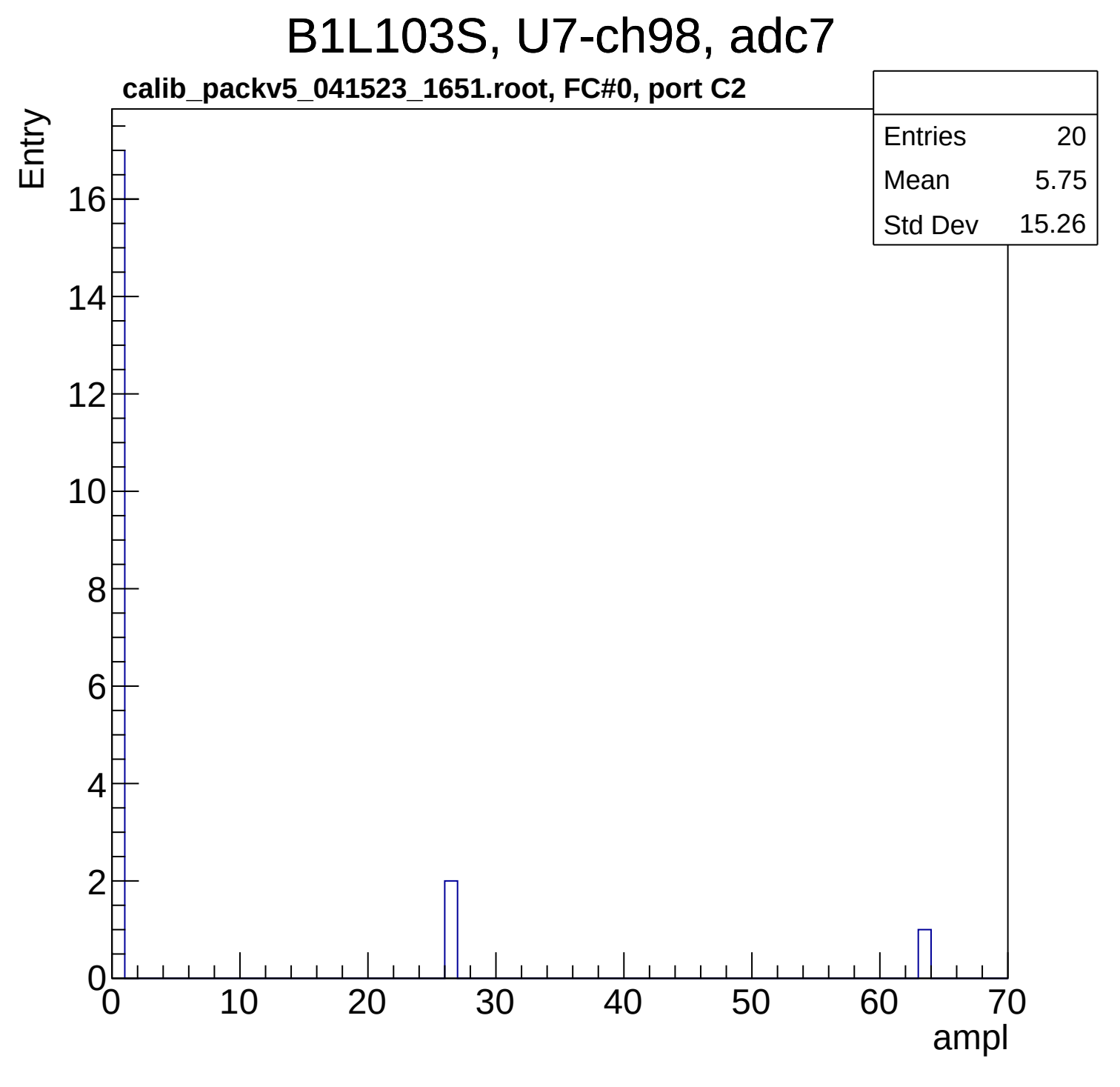
40
50
60
70


B1L103S, U7-ch98, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 5.75
Std Dev 15.26
Entry
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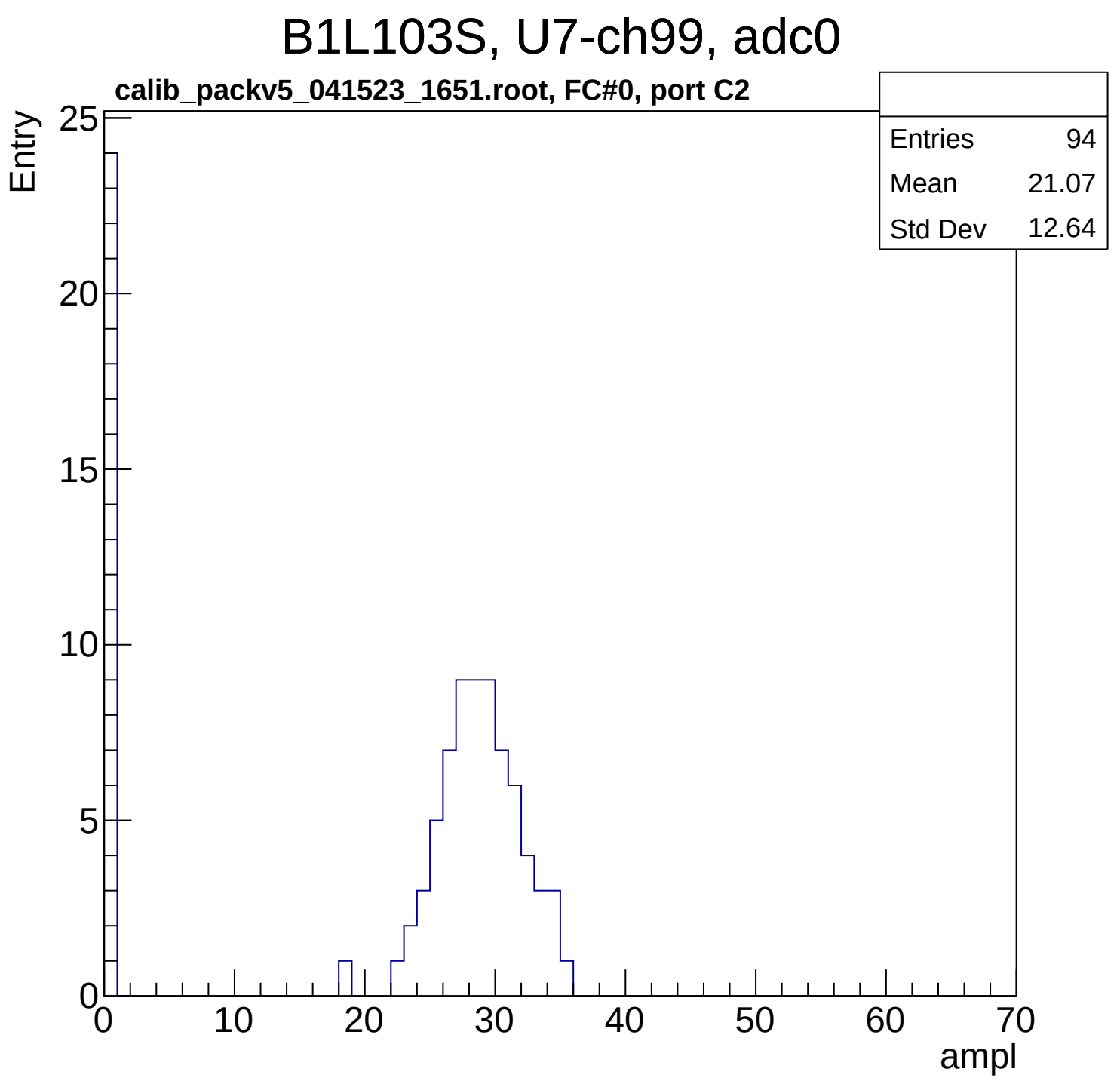
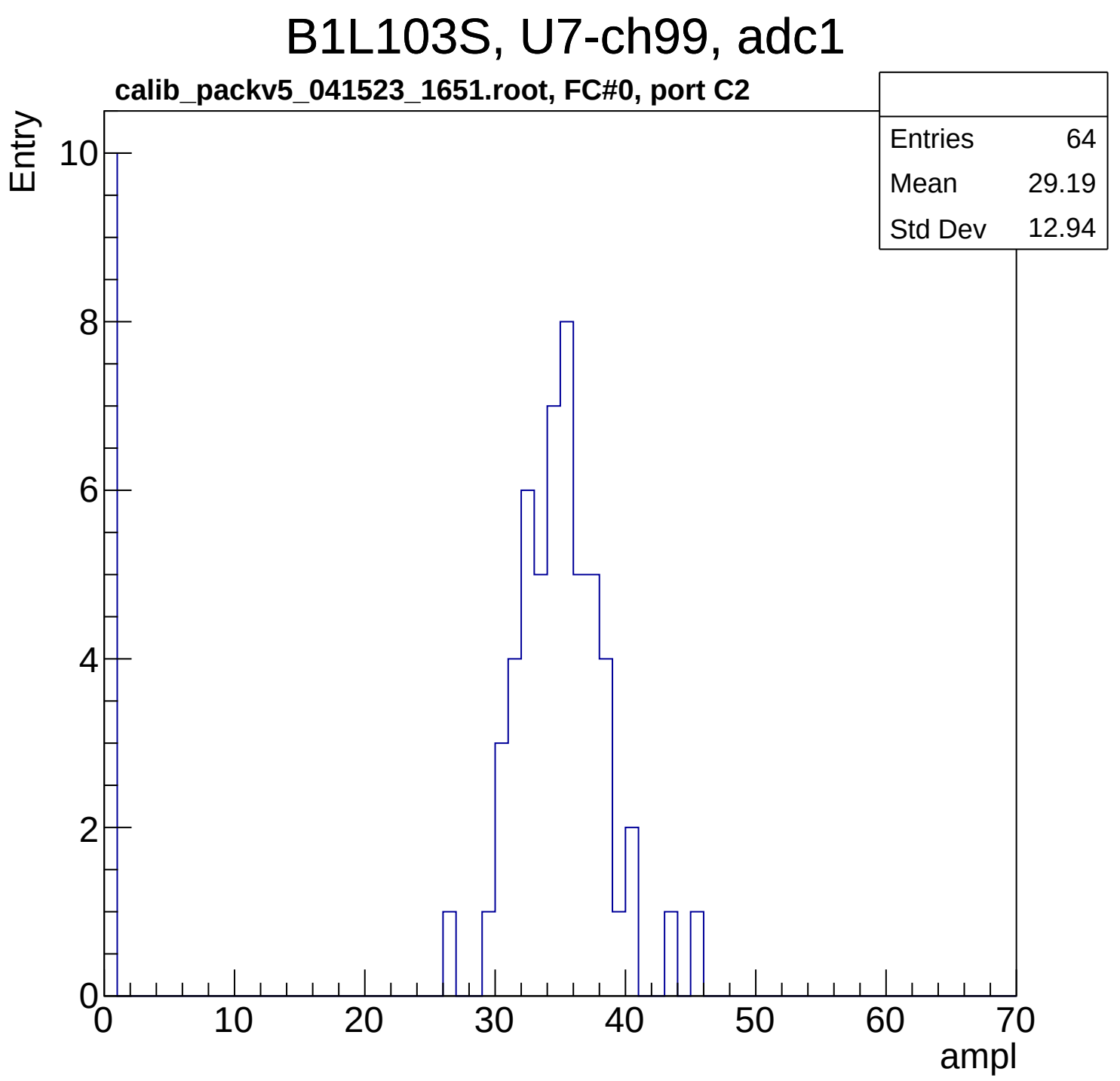
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch99, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 94
Mean 21.07
Std Dev 12.64
Entry
0
5
10
15
20
25
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch99, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 29.19
Std Dev 12.94
Entry
ampl
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0
10
20
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40
50
60
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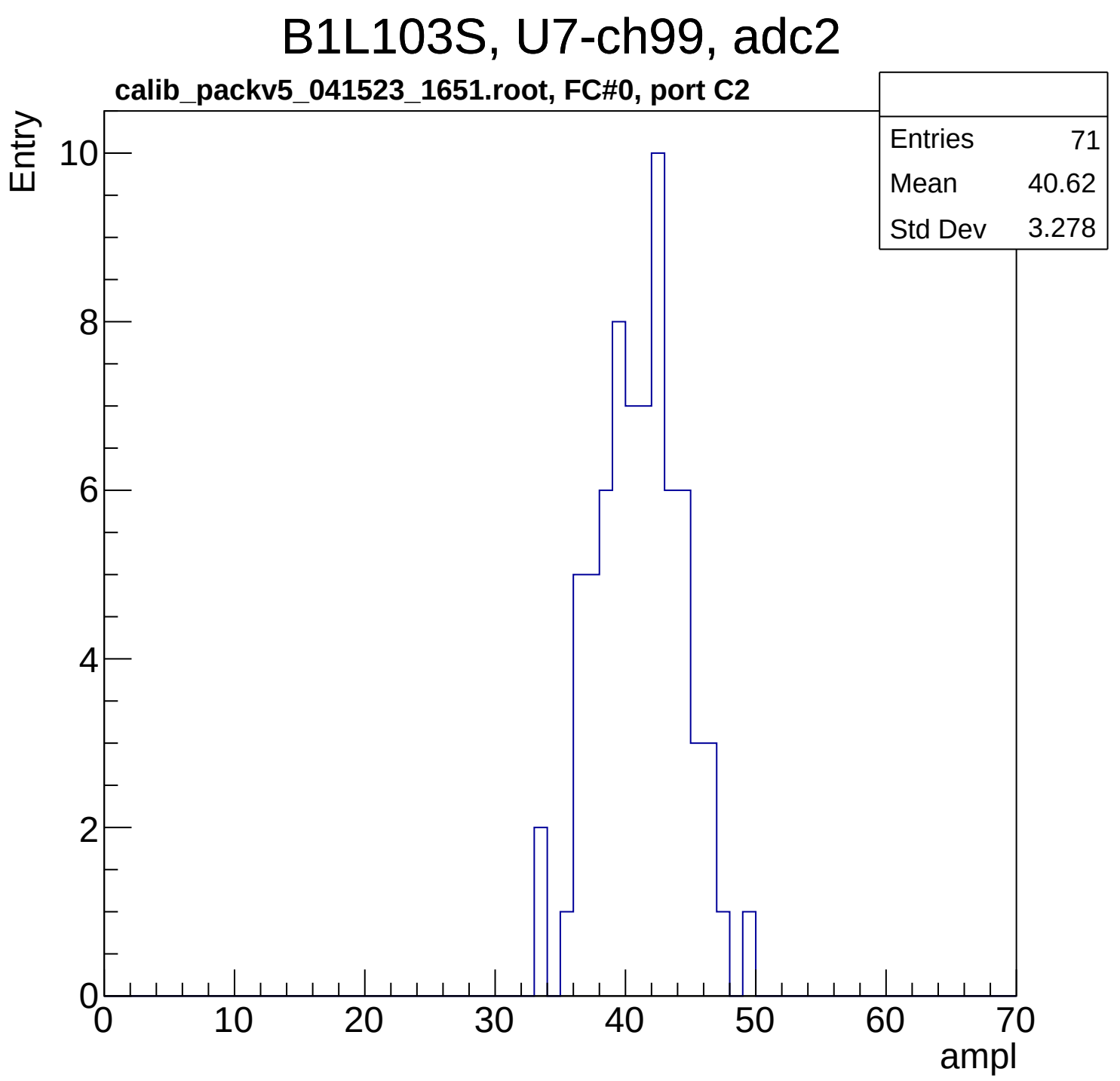
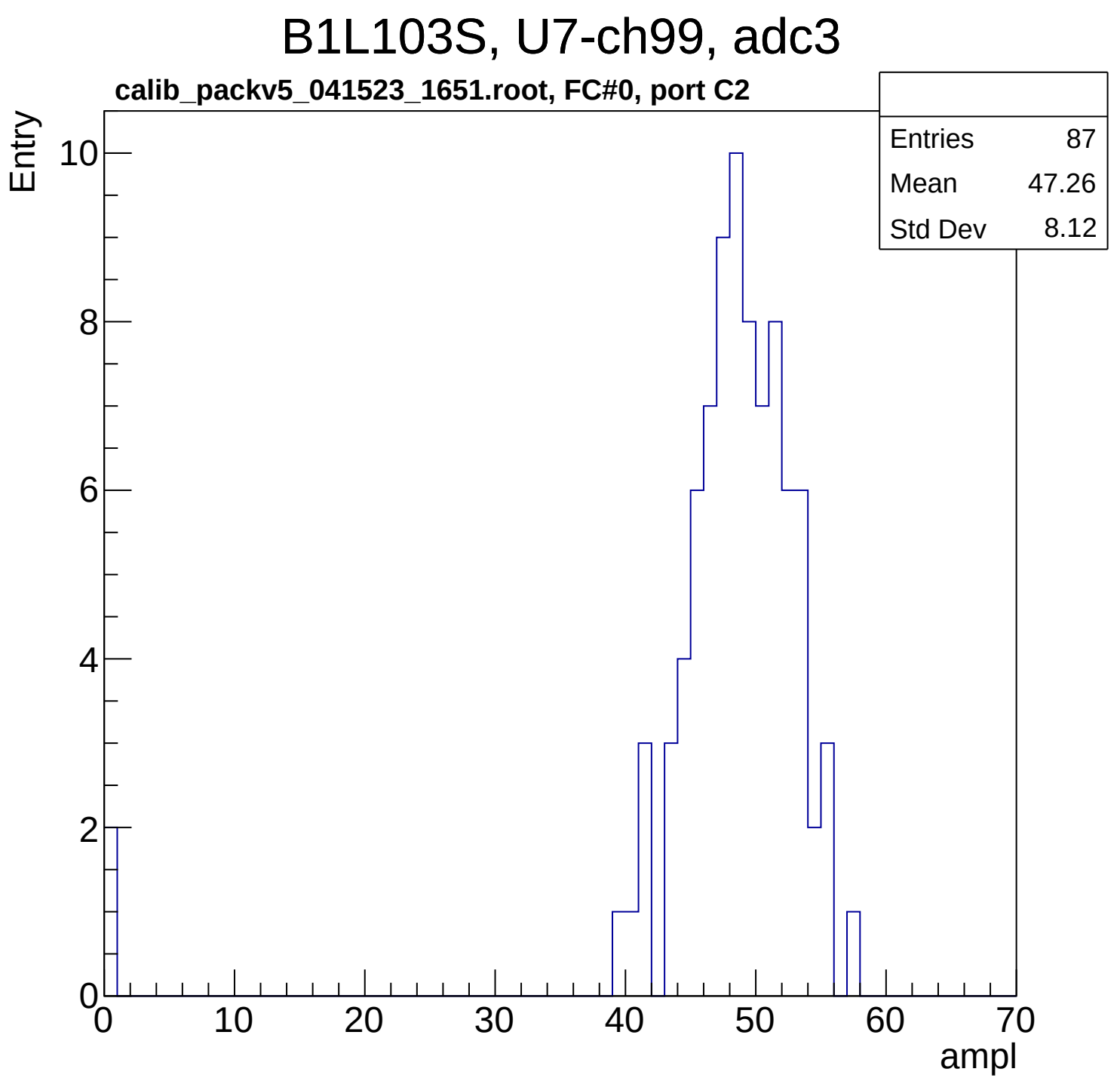

B1L103S, U7-ch99, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 40.62
Std Dev 3.278
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch99, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 87
Mean 47.26
Std Dev 8.12
Entry
0
2
4
6
8
10
0
10
20
30
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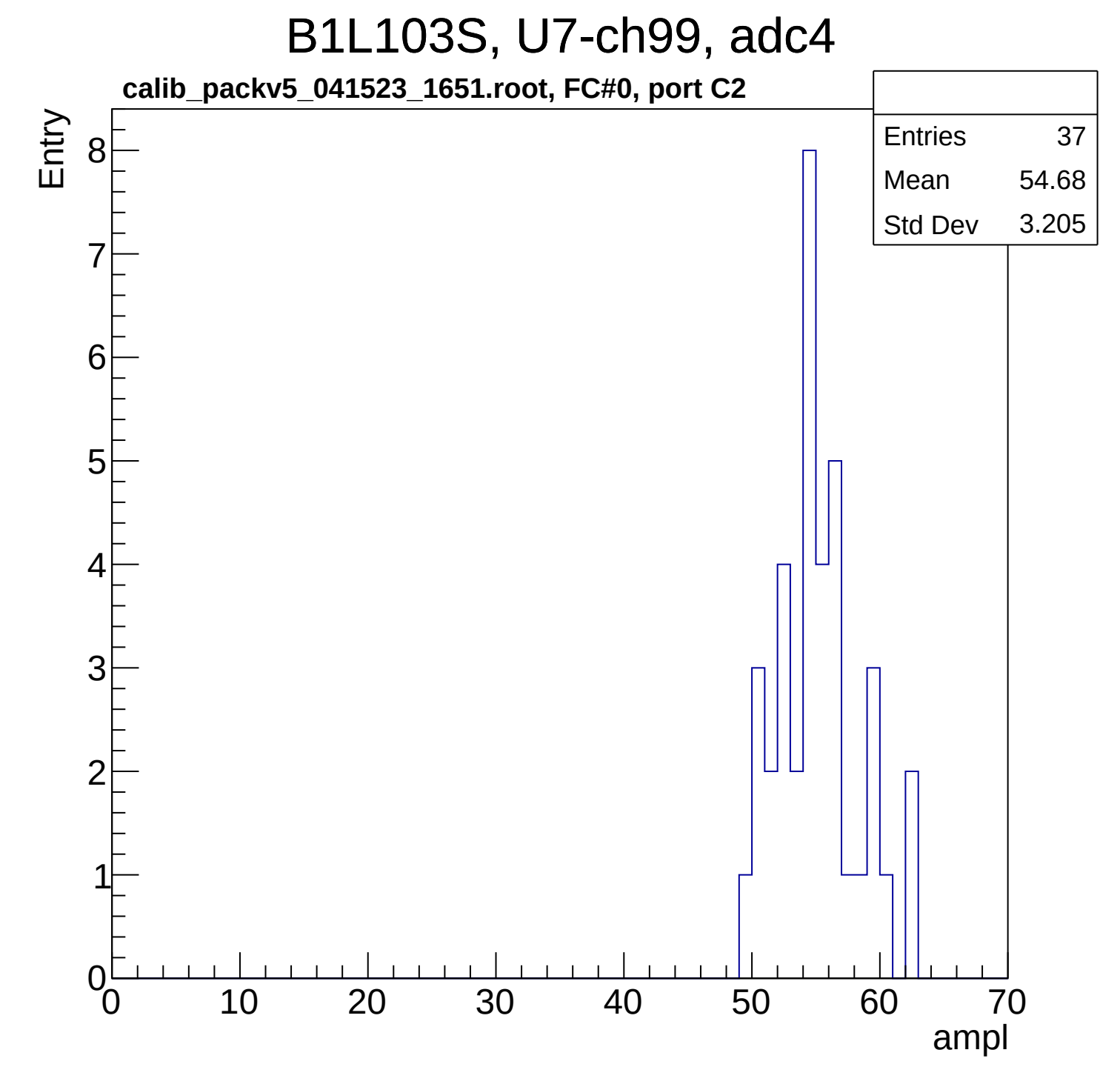
50
60
70
ampl


B1L103S, U7-ch99, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 37
Mean 54.68
Std Dev 3.205
Entry
ampl
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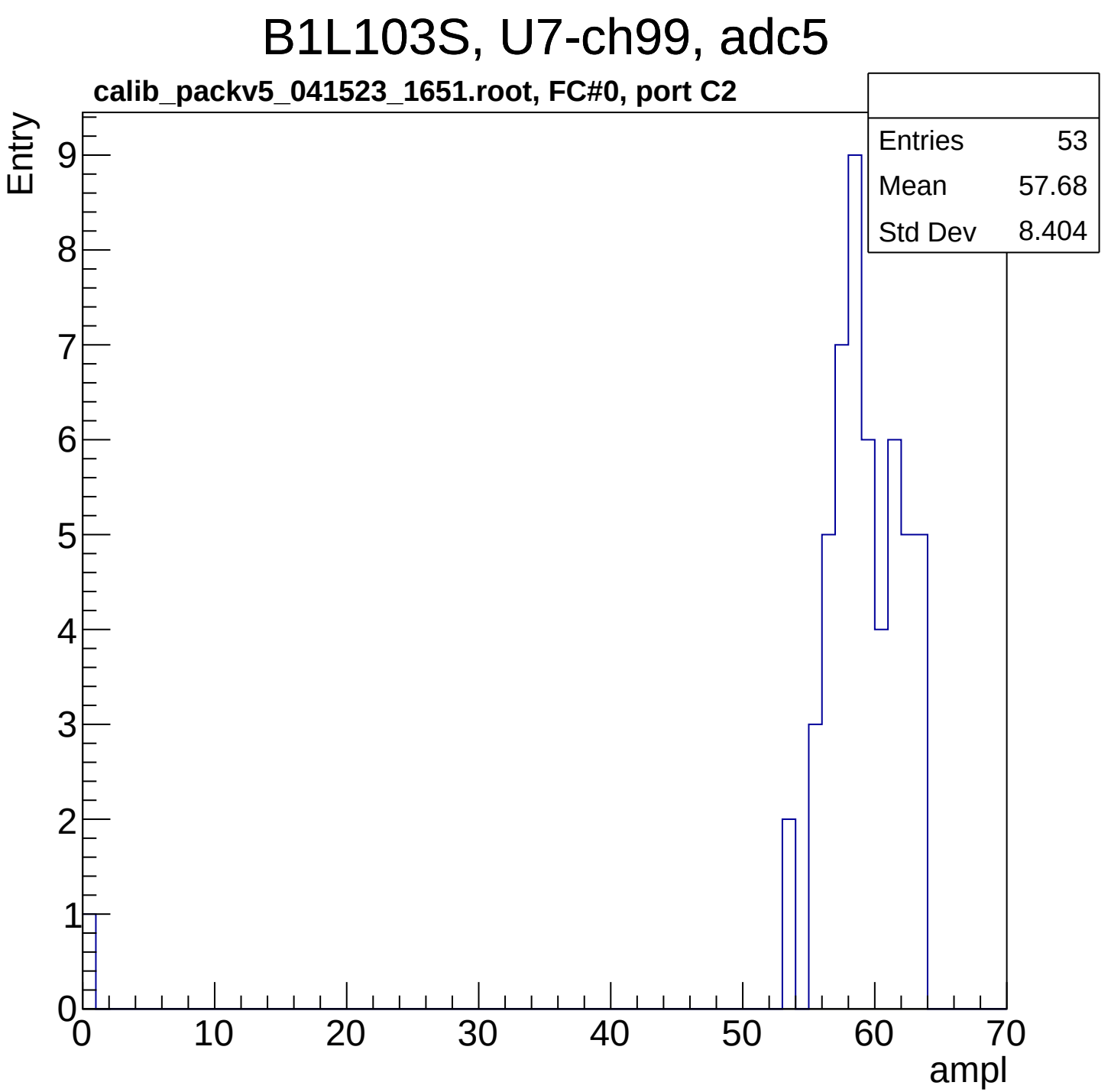
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch99, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 57.68
Std Dev 8.404
Entry
ampl
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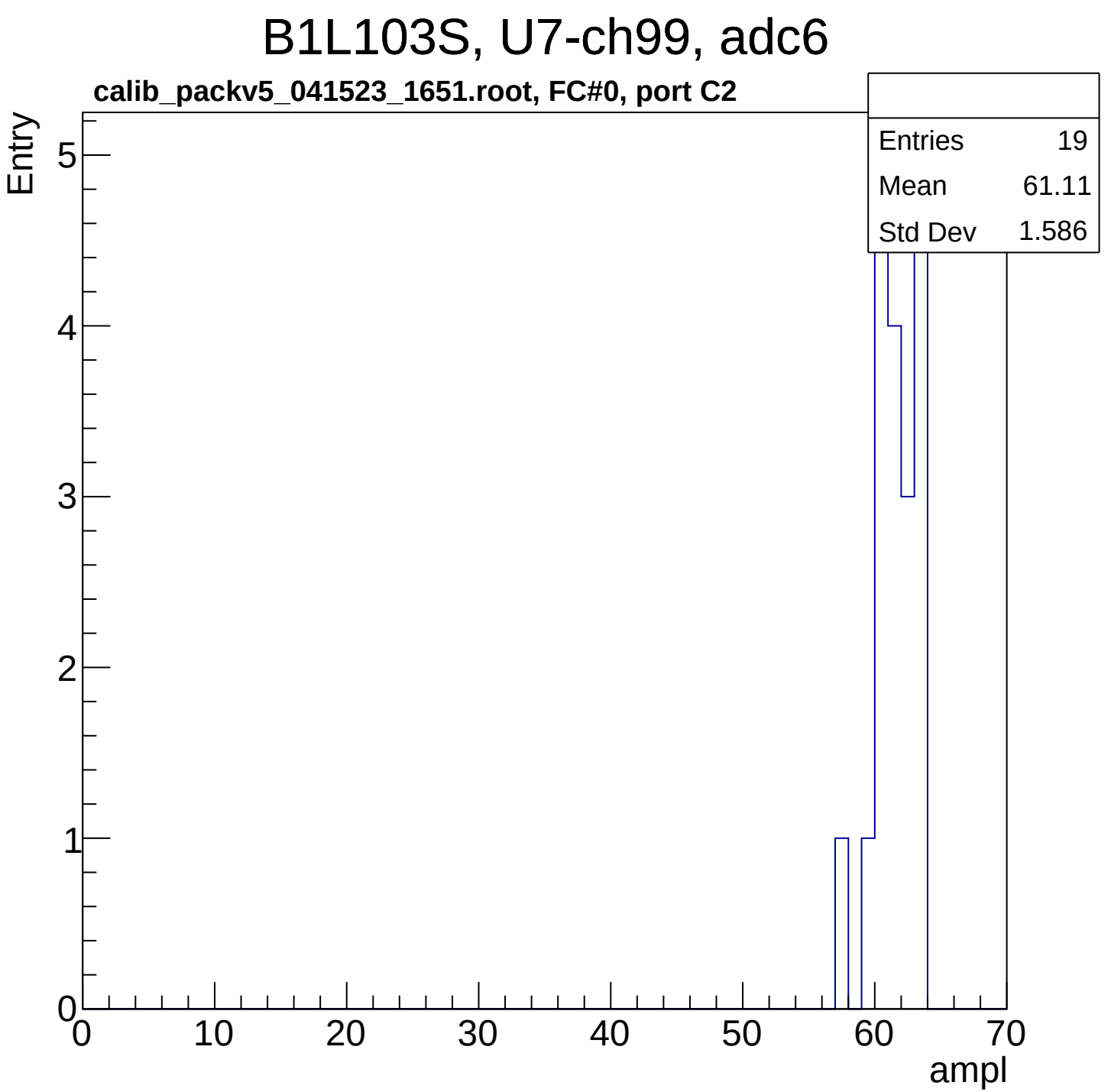
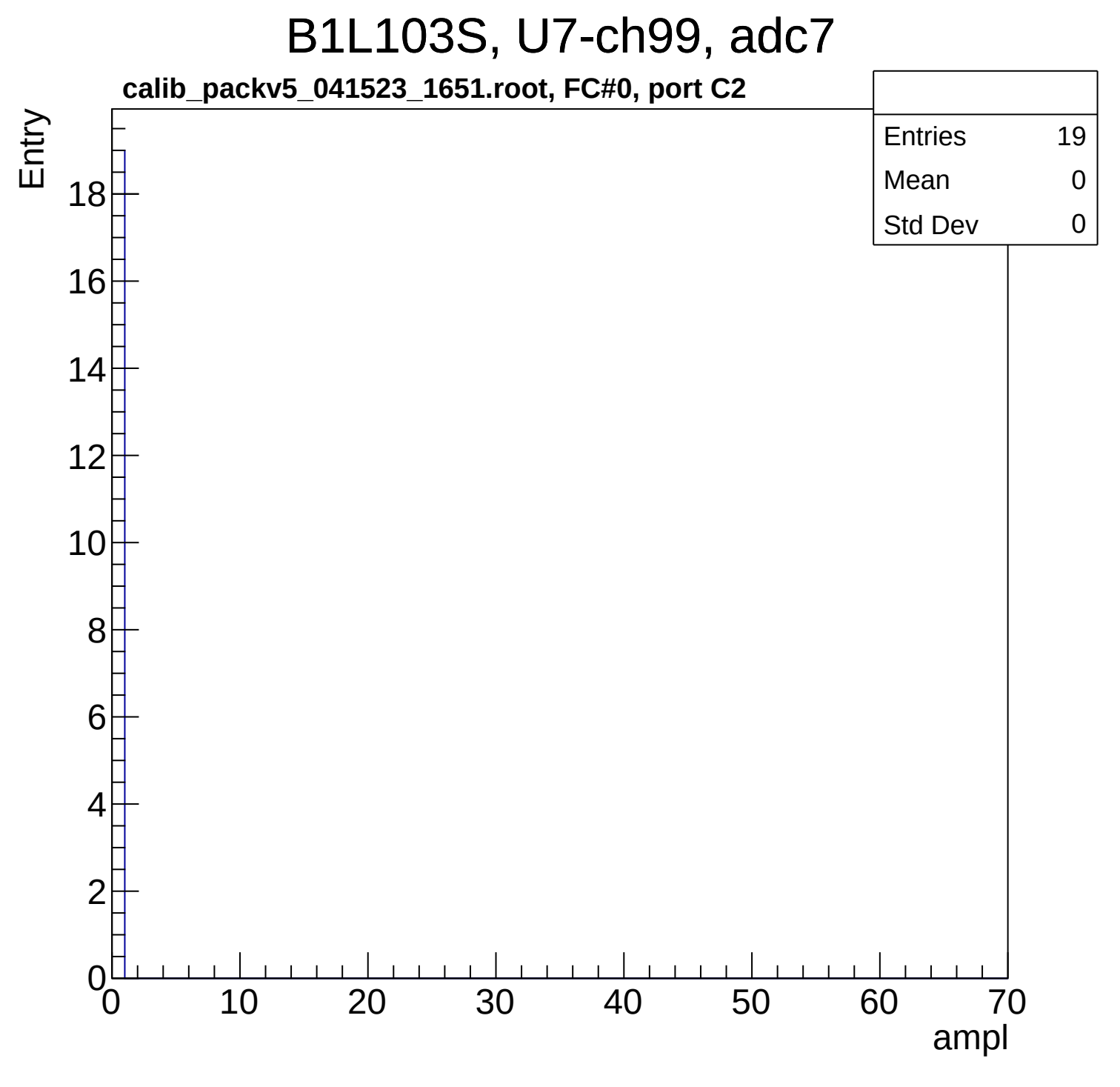
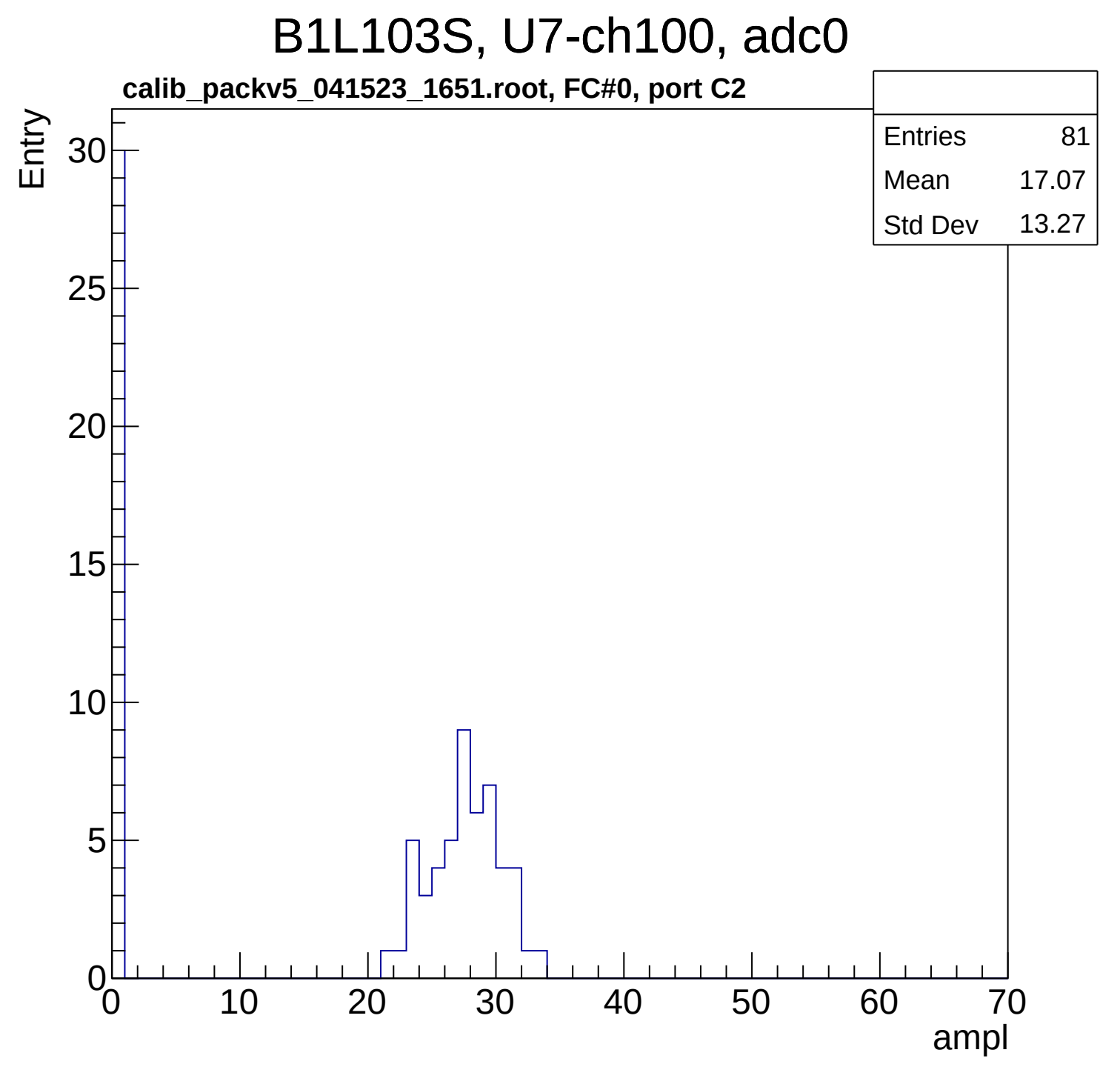
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U7-ch99, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 61.11
Std Dev 1.586
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch99, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch100, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 17.07
Std Dev 13.27
Entry
ampl
0
5
10
15
20
25
30
0
10
20
30
40
50
60
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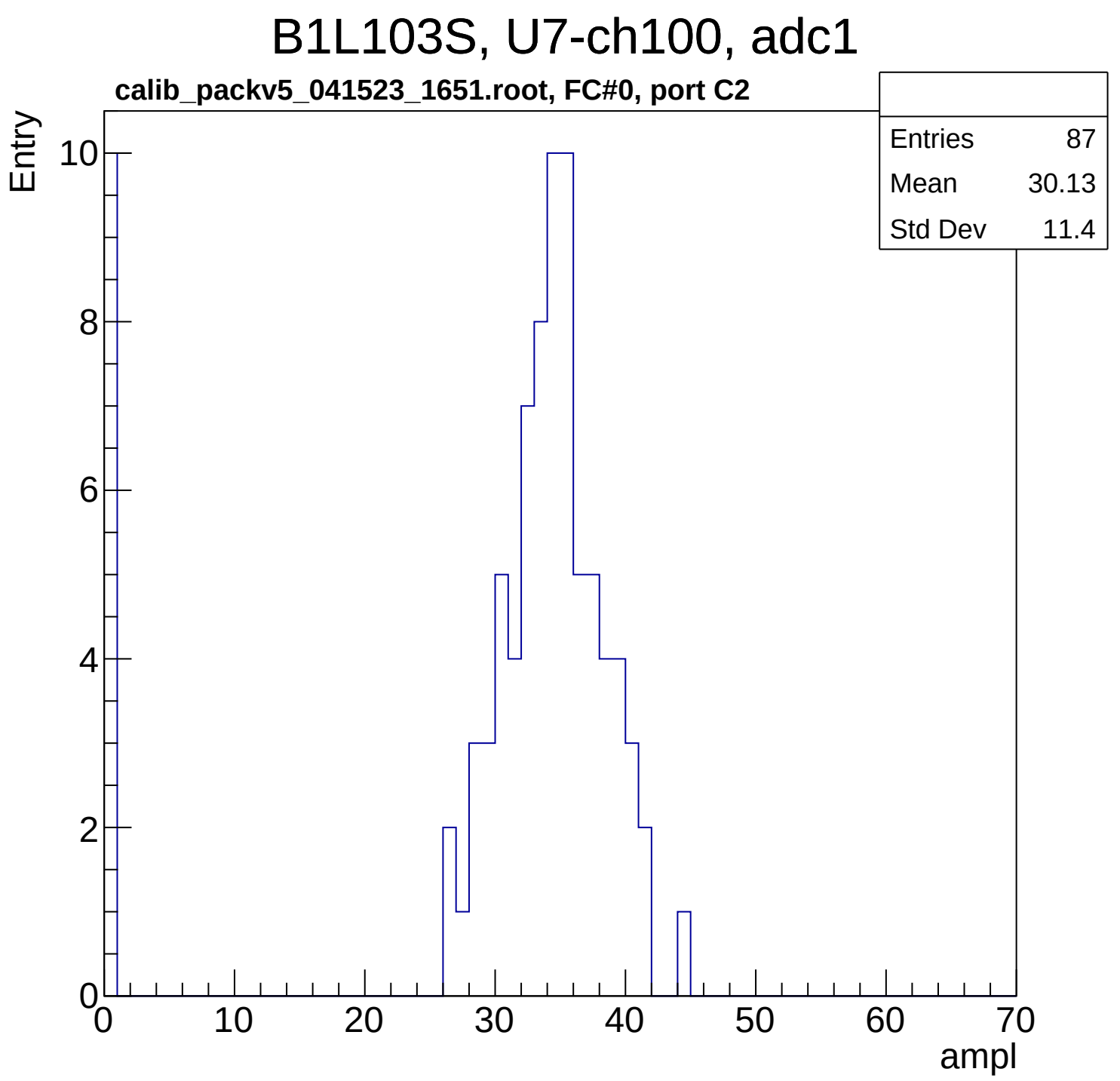
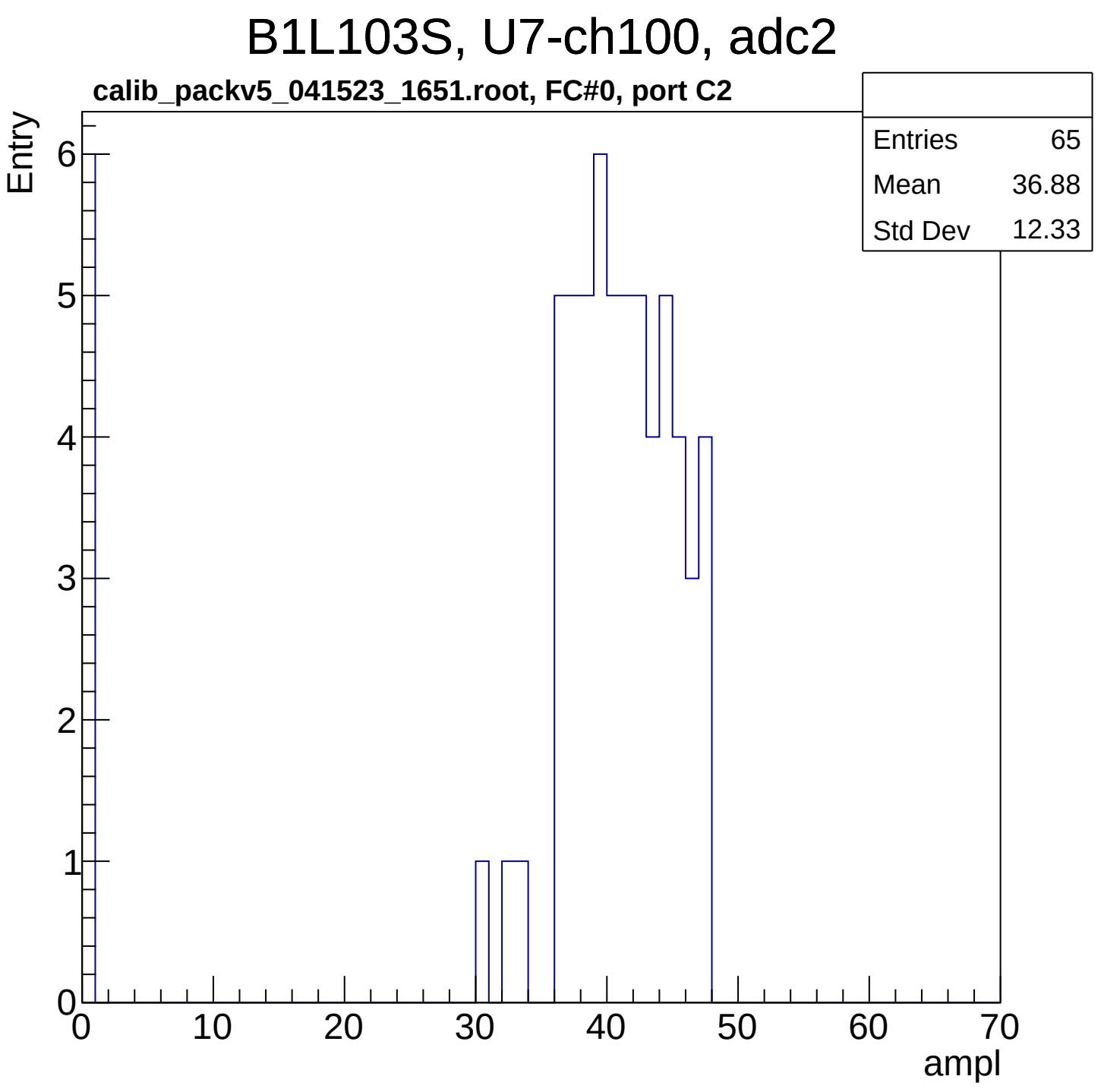
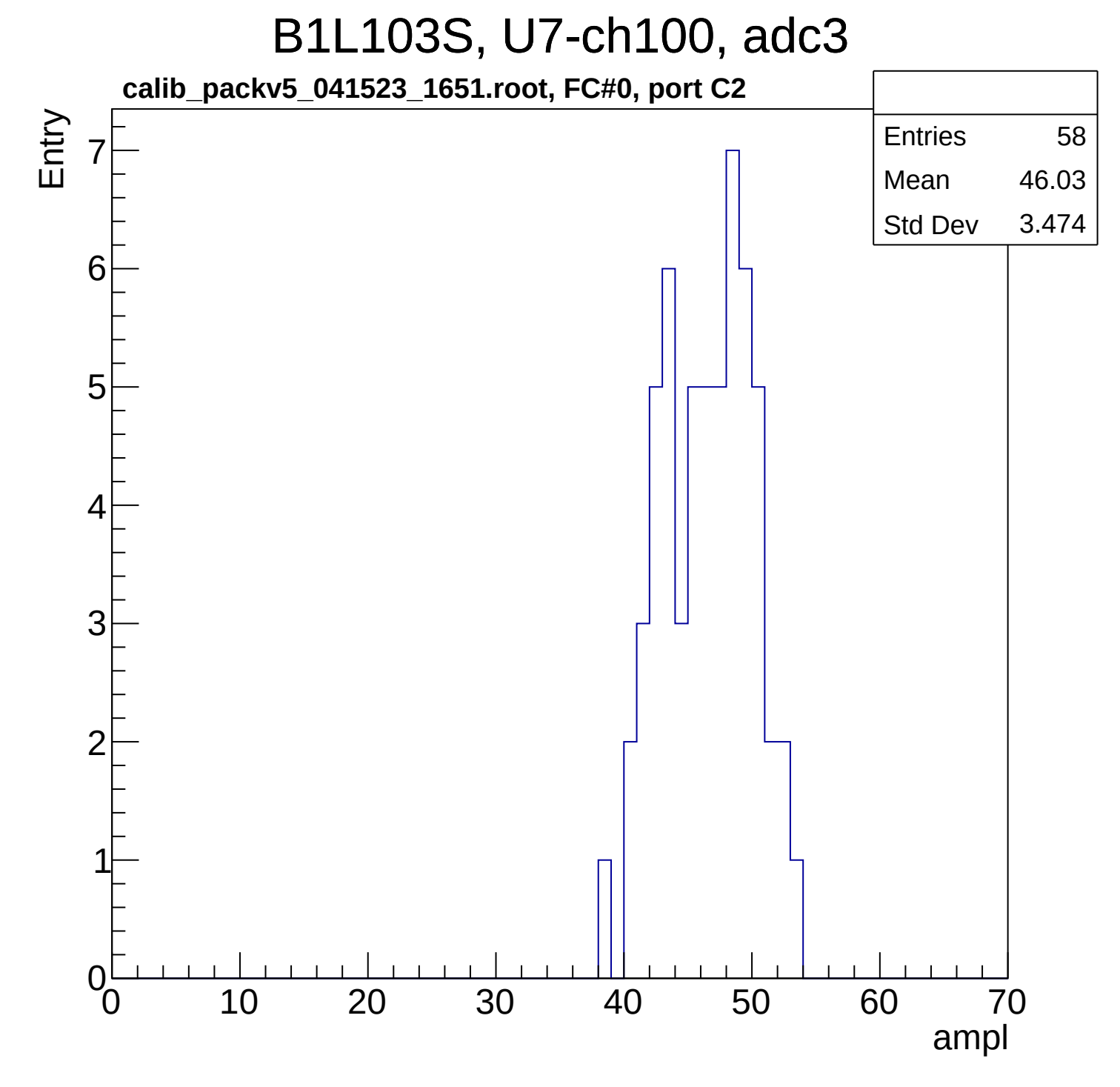

B1L103S, U7-ch100, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 87
Mean 30.13
Std Dev 11.4
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U7-ch100, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 36.88
Std Dev 12.33
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U7-ch100, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 46.03
Std Dev 3.474
Entry
ampl
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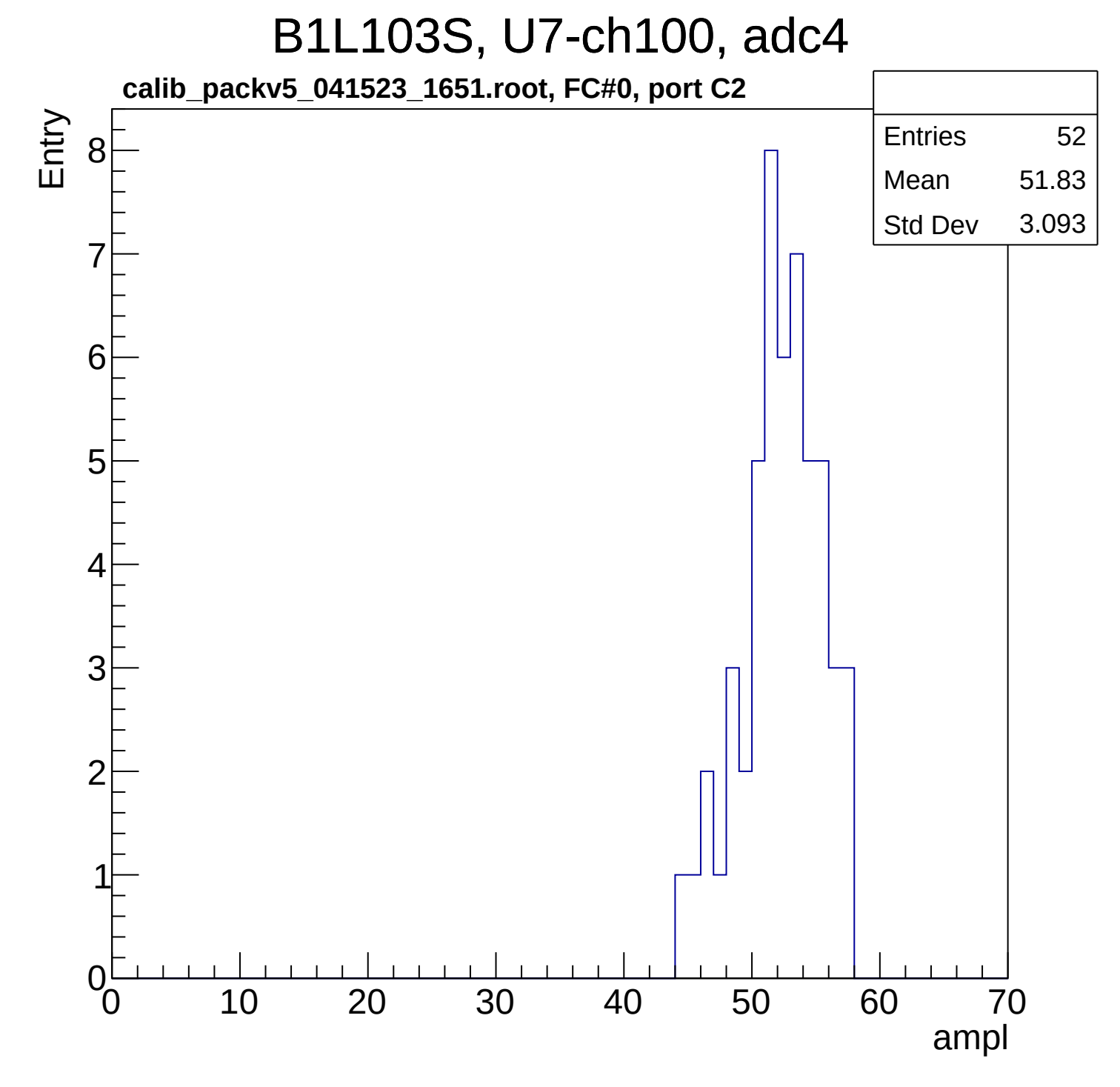
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U7-ch100, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 51.83
Std Dev 3.093
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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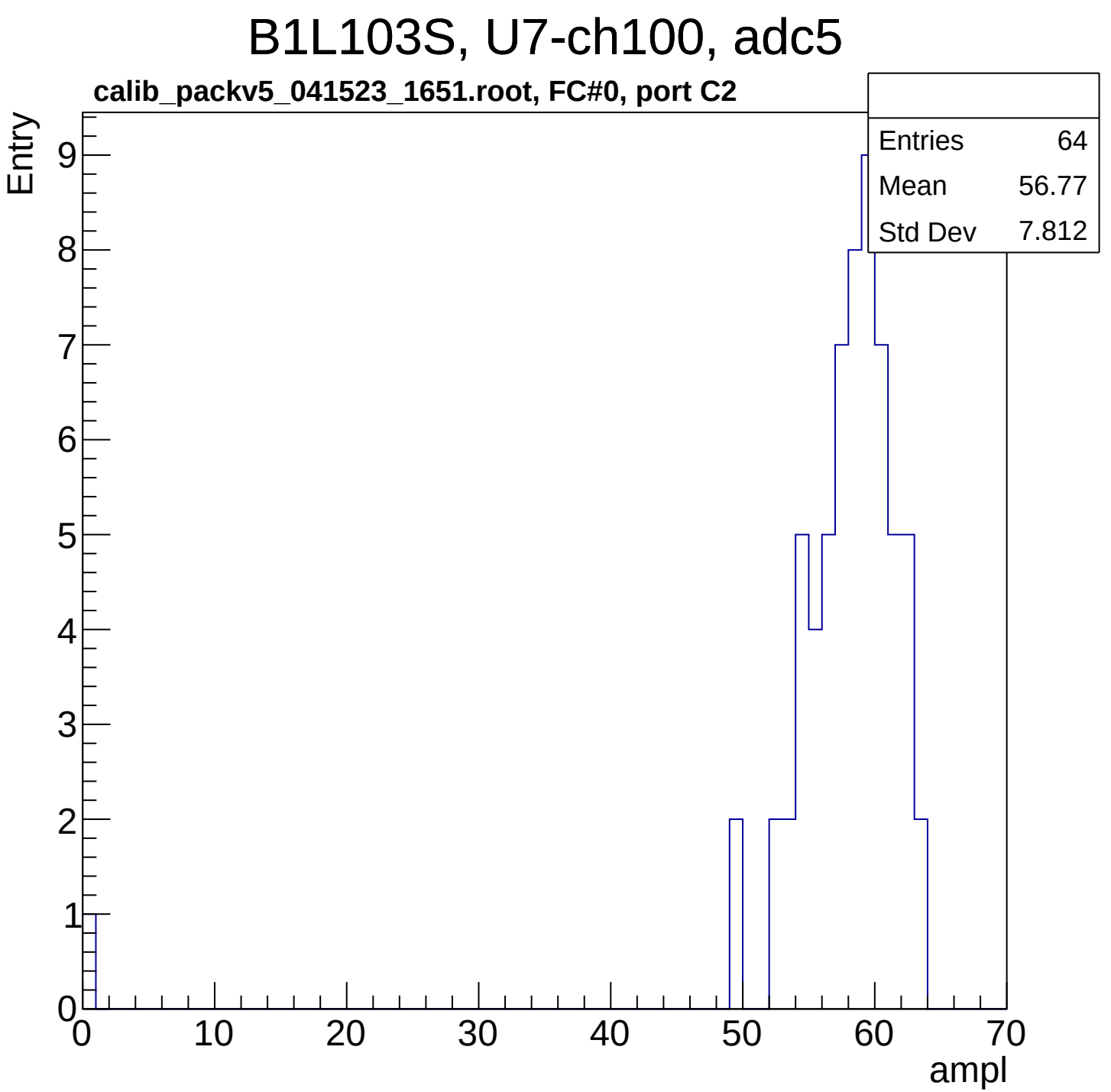
B1L103S, U7-ch100, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 56.77
Std Dev 7.812
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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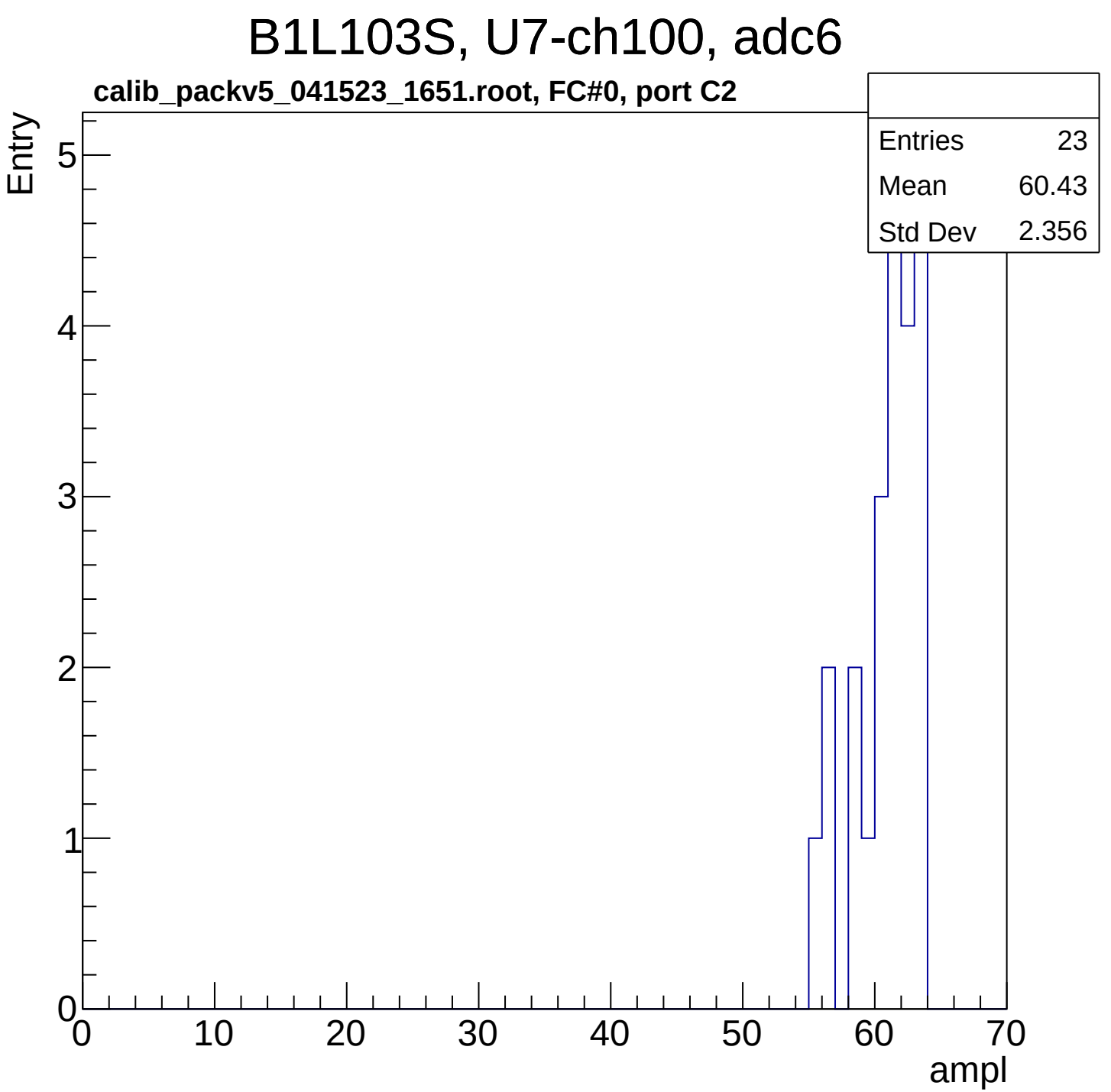
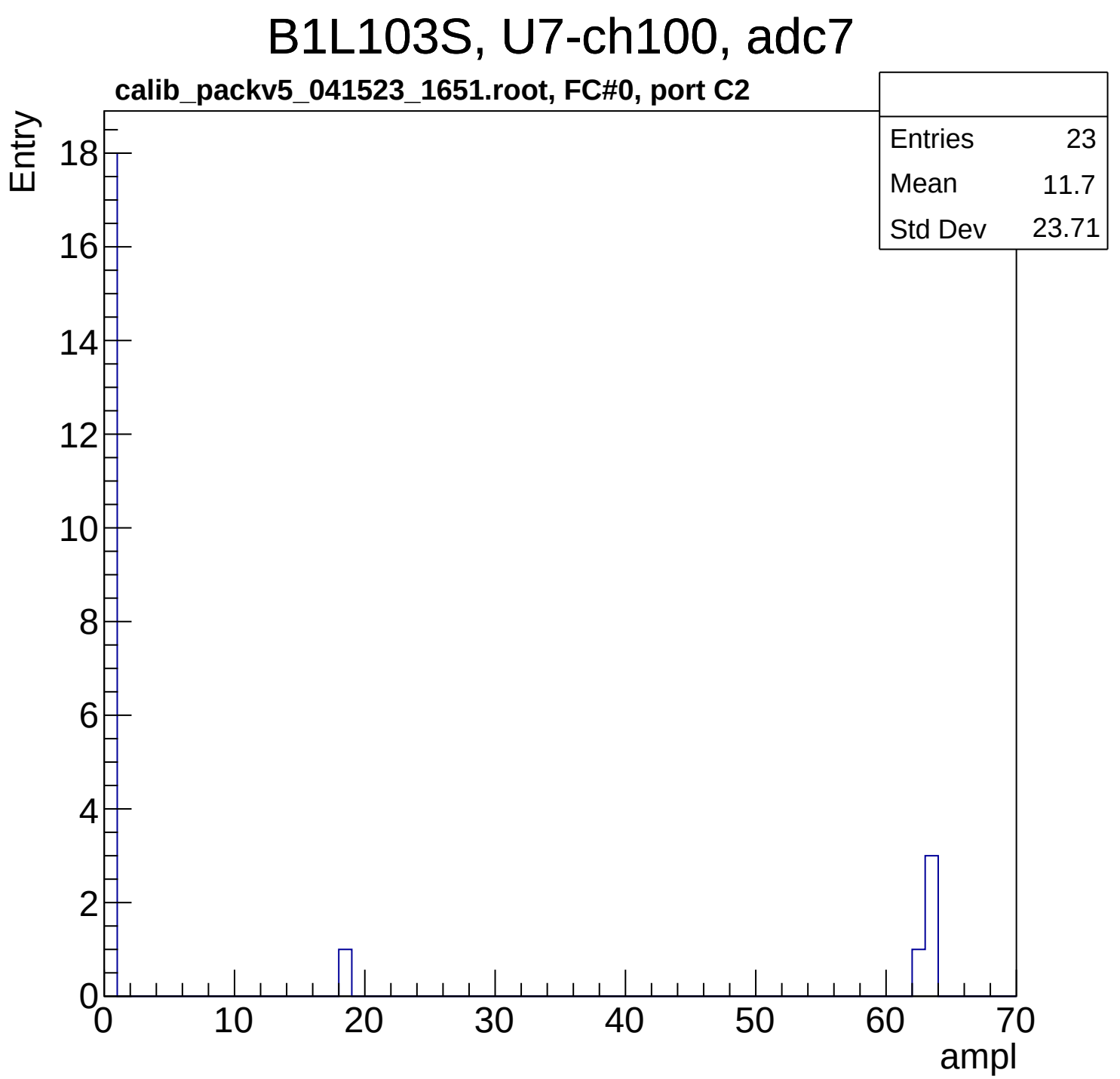
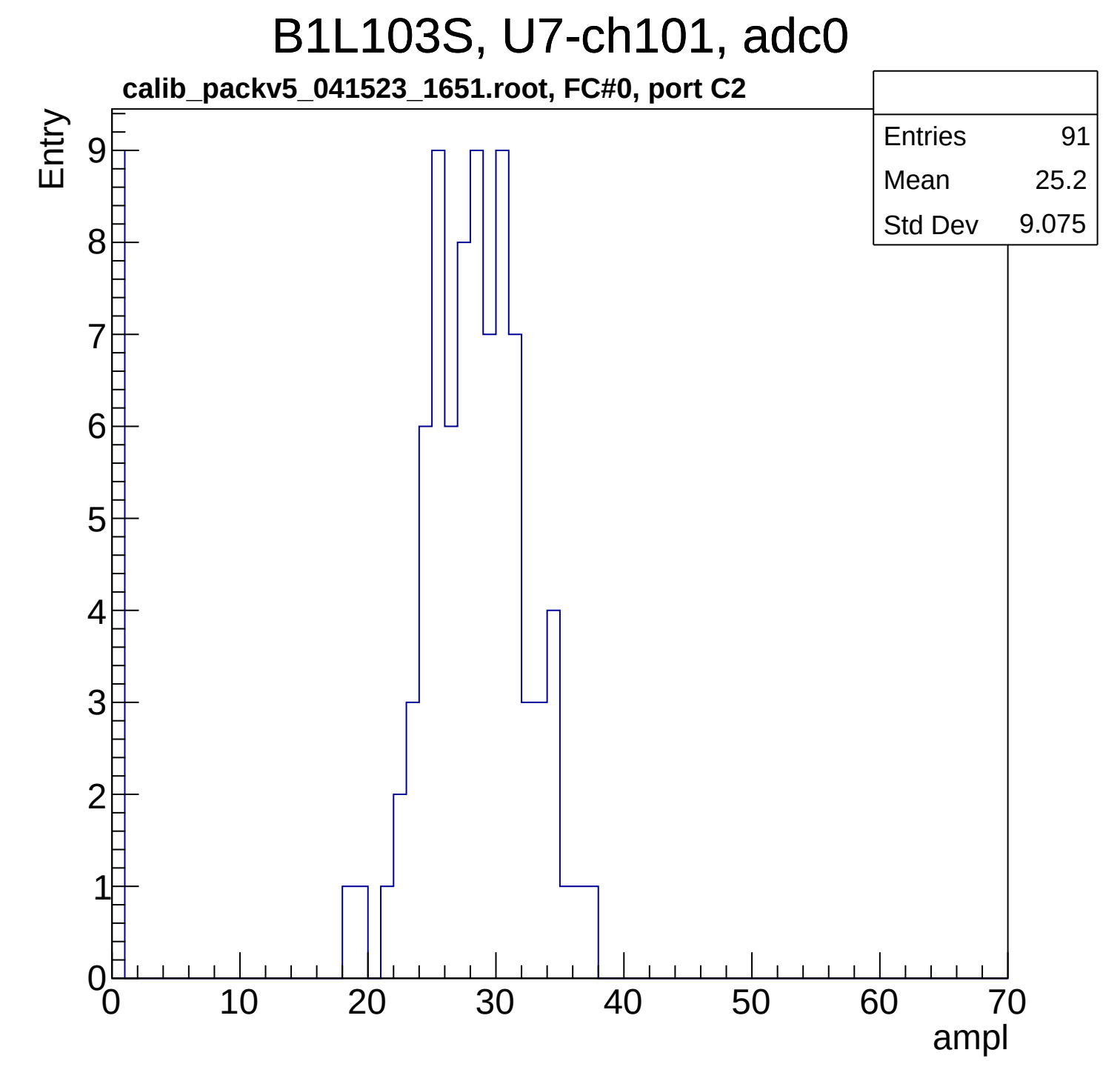
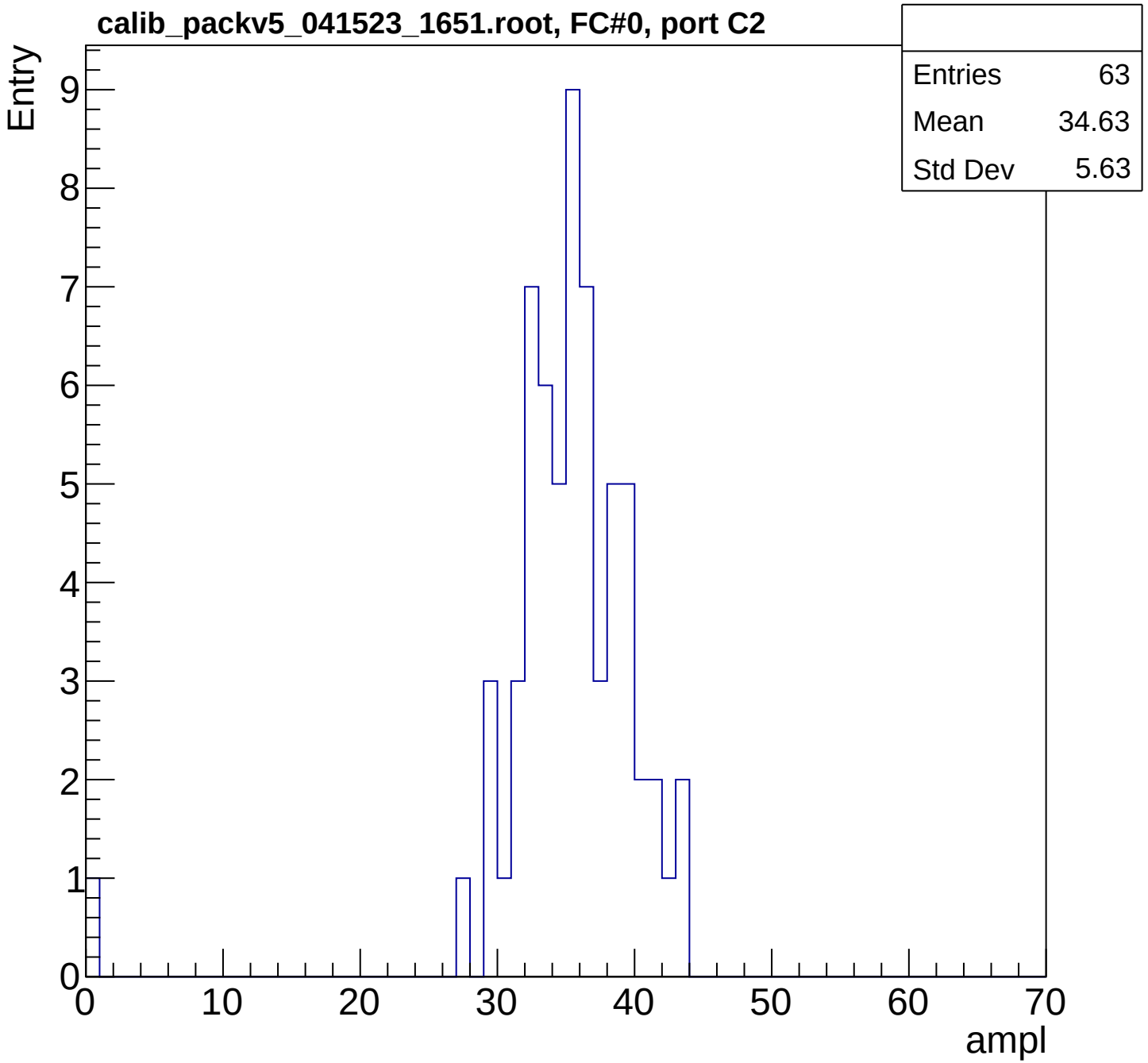
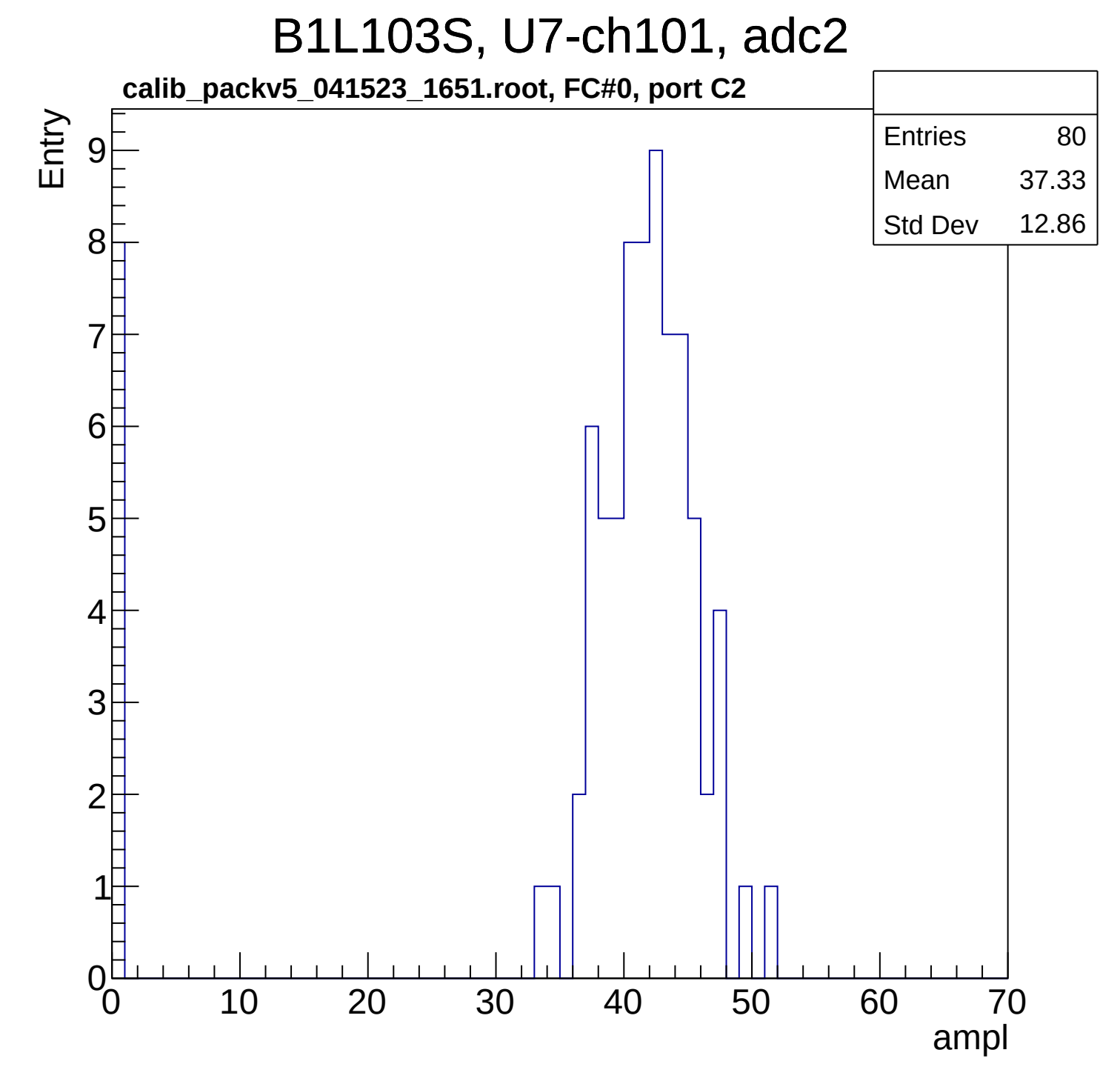
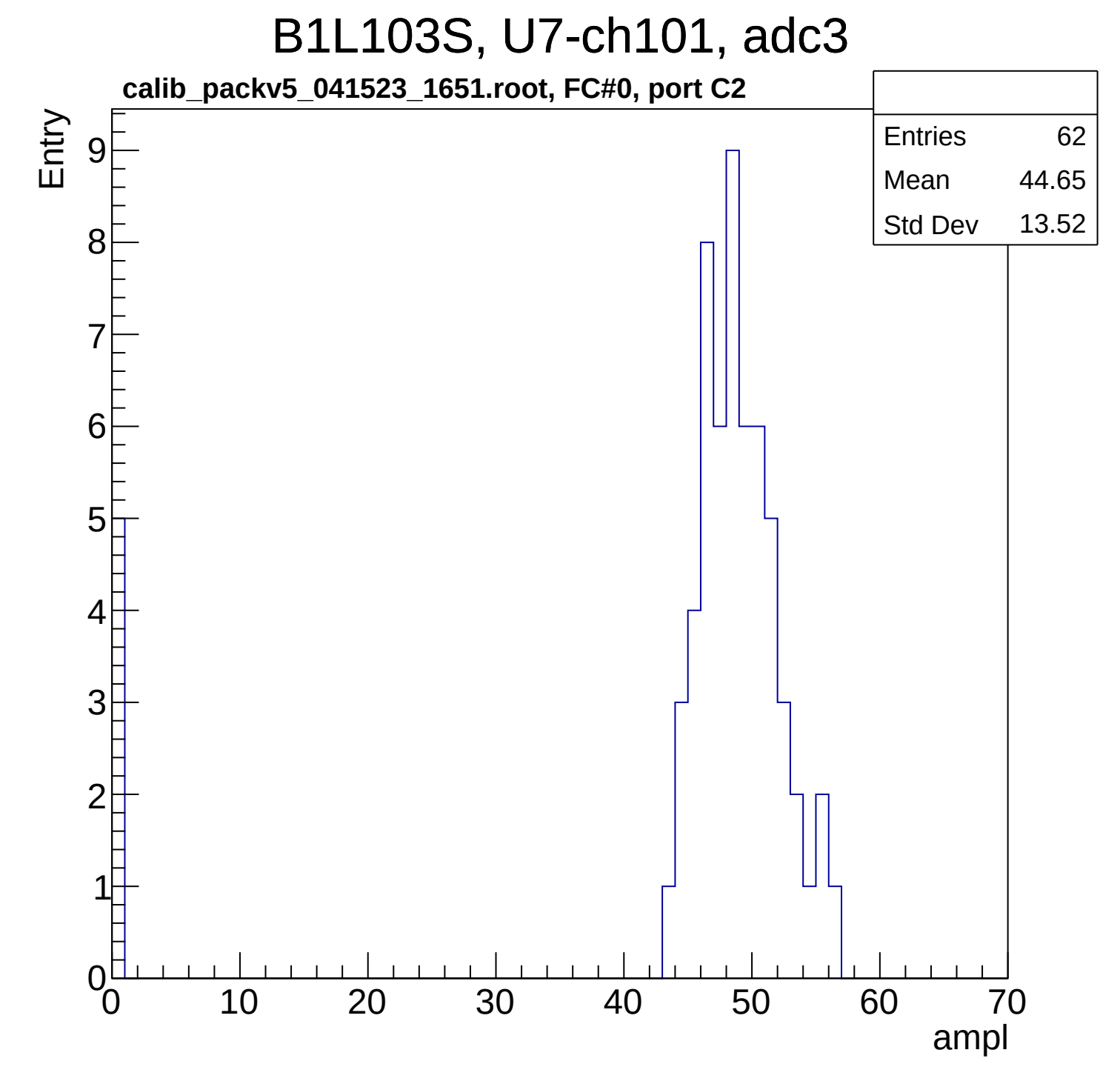

B1L103S, U7-ch100, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 23
Mean 60.43
Std Dev 2.356
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U7-ch100, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 23
Mean 11.7
Std Dev 23.71
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch101, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 91
Mean 25.2
Std Dev 9.075
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U7-ch101, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 34.63
Std Dev 5.63
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U7-ch101, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 37.33
Std Dev 12.86
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U7-ch101, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 44.65
Std Dev 13.52
Entry
ampl
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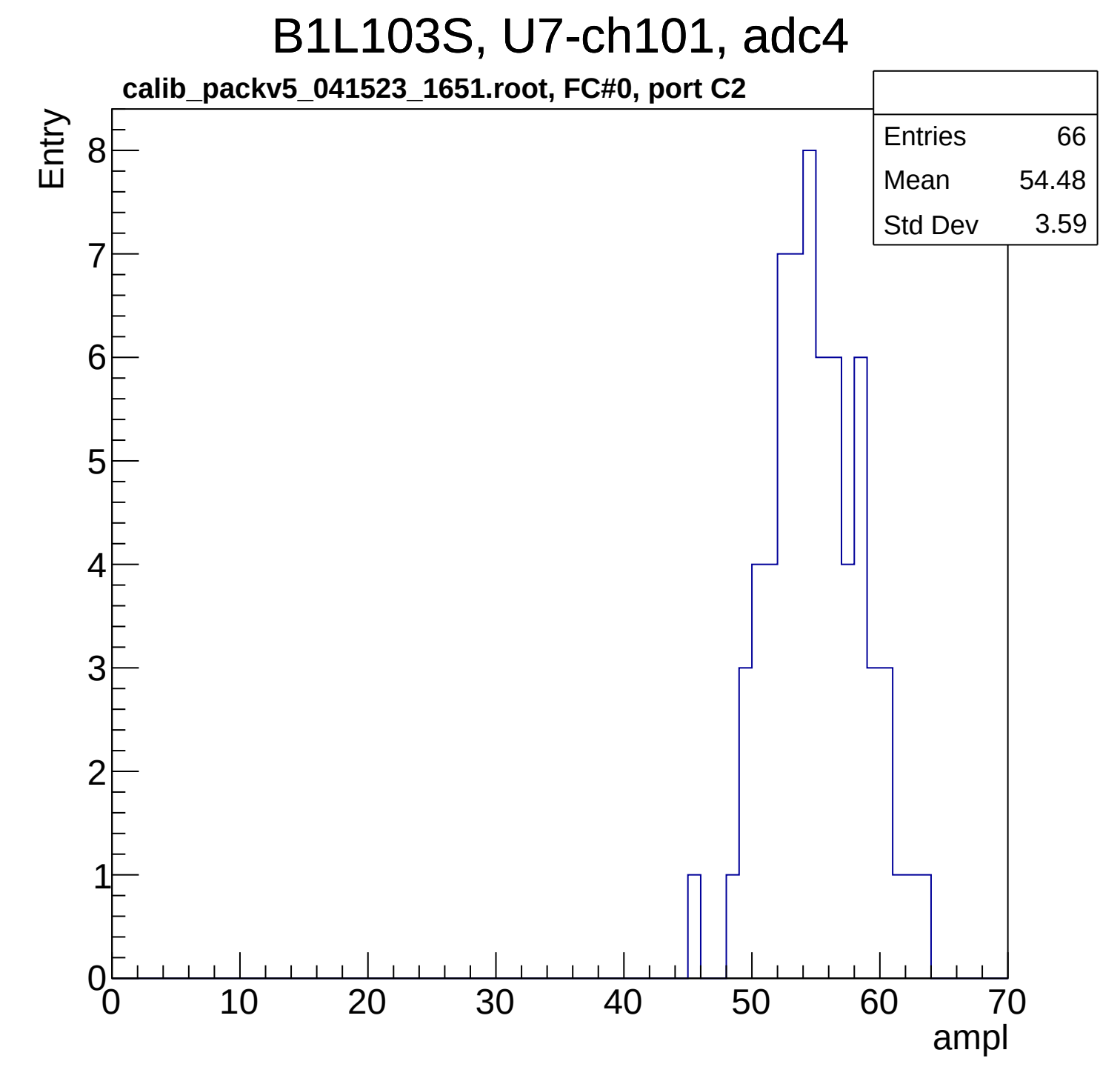
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U7-ch101, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 54.48
Std Dev 3.59
Entry
ampl
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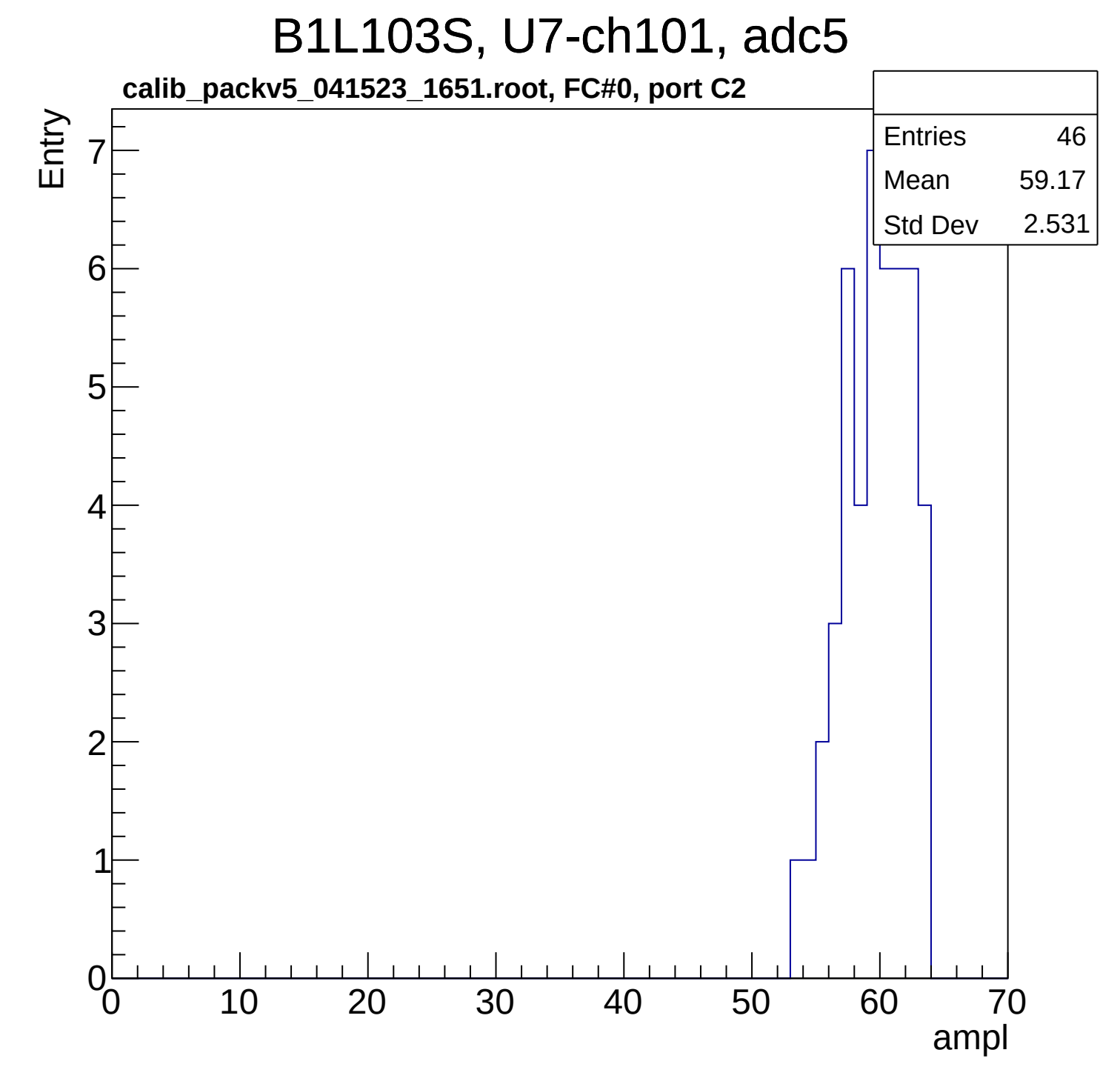
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch101, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 59.17
Std Dev 2.531
Entry
ampl
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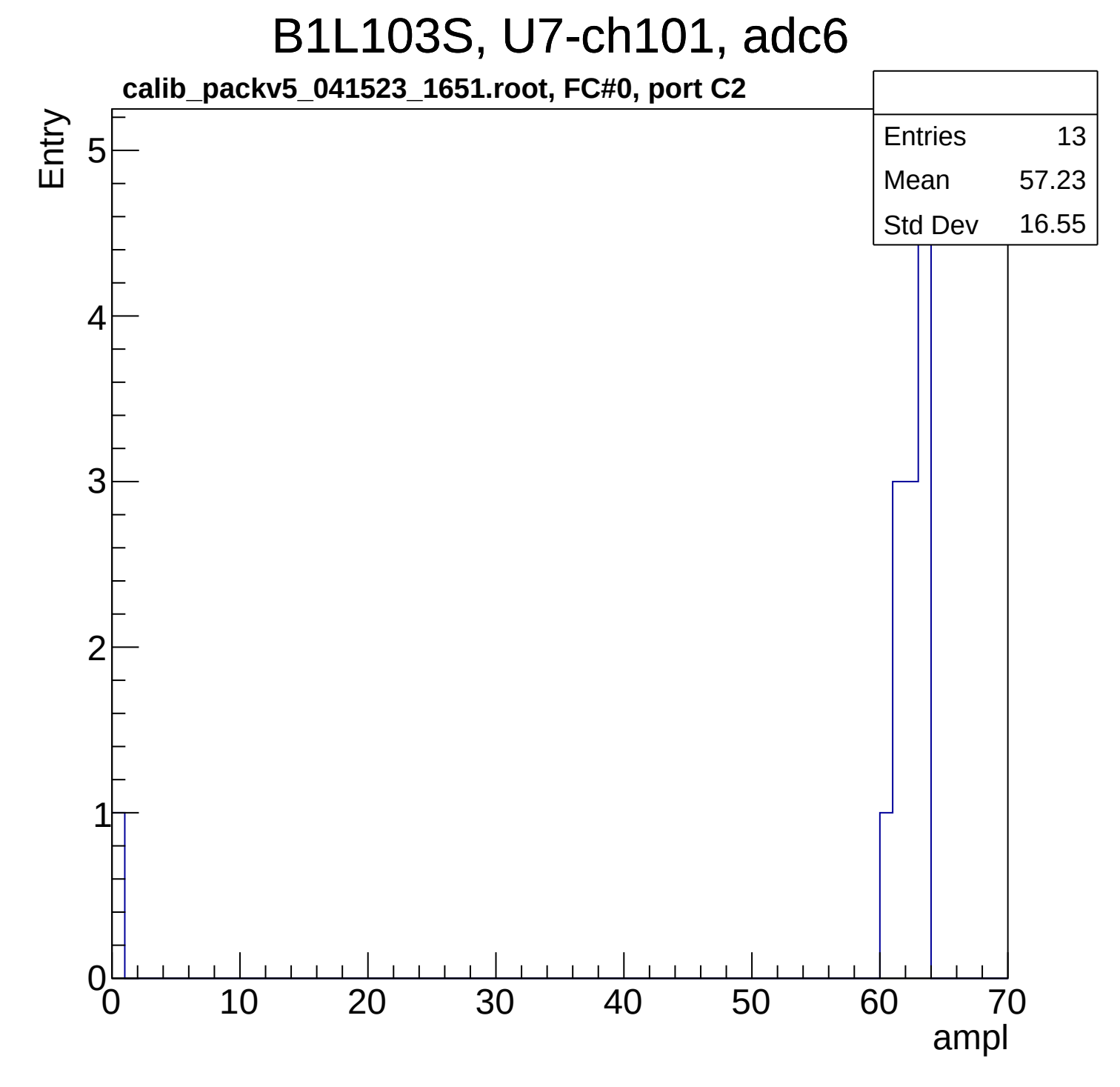
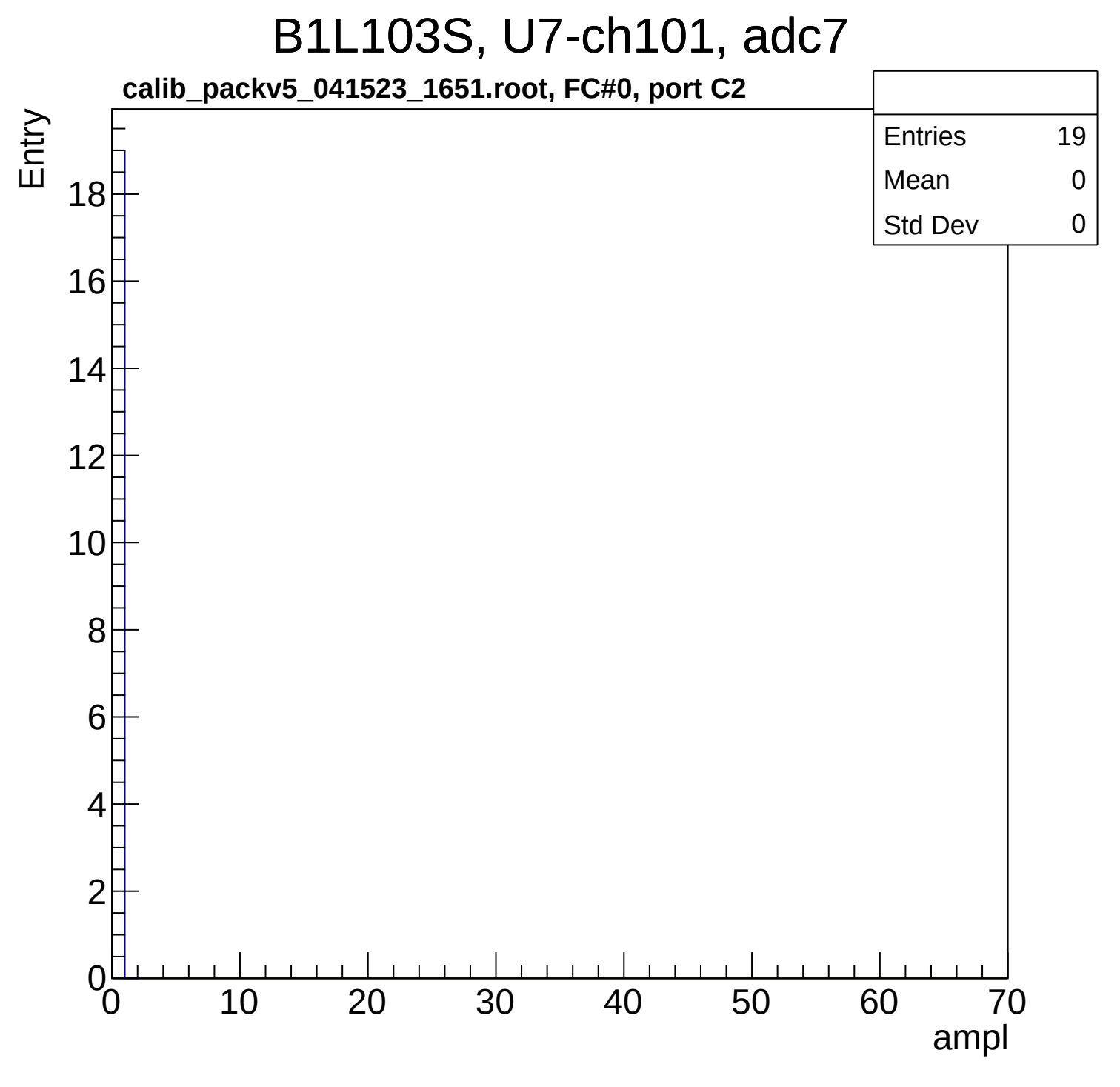
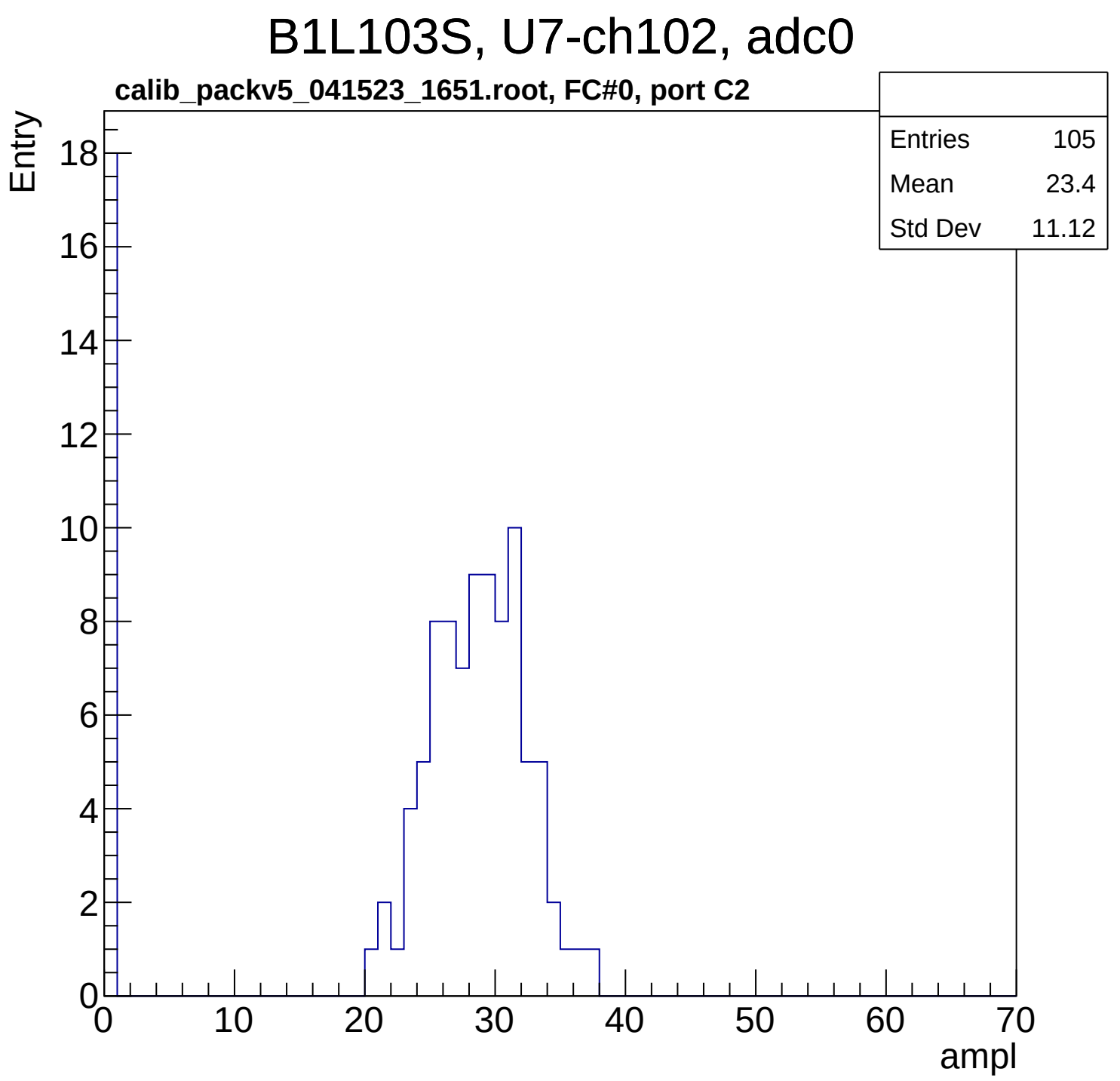
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U7-ch101, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 13
Mean 57.23
Std Dev 16.55
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch101, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch102, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 105
Mean 23.4
Std Dev 11.12
Entry
0
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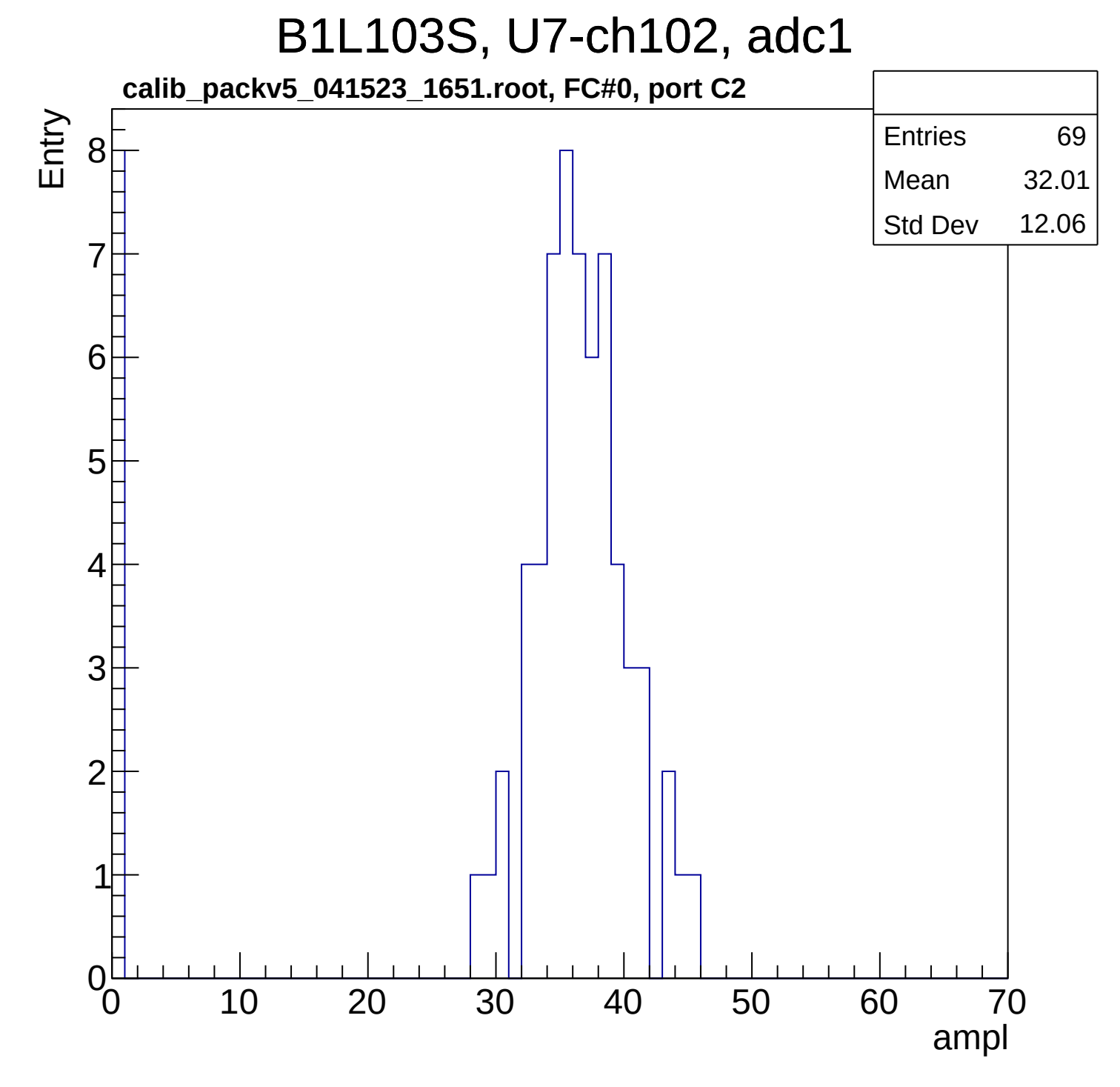
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch102, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 32.01
Std Dev 12.06
Entry
ampl
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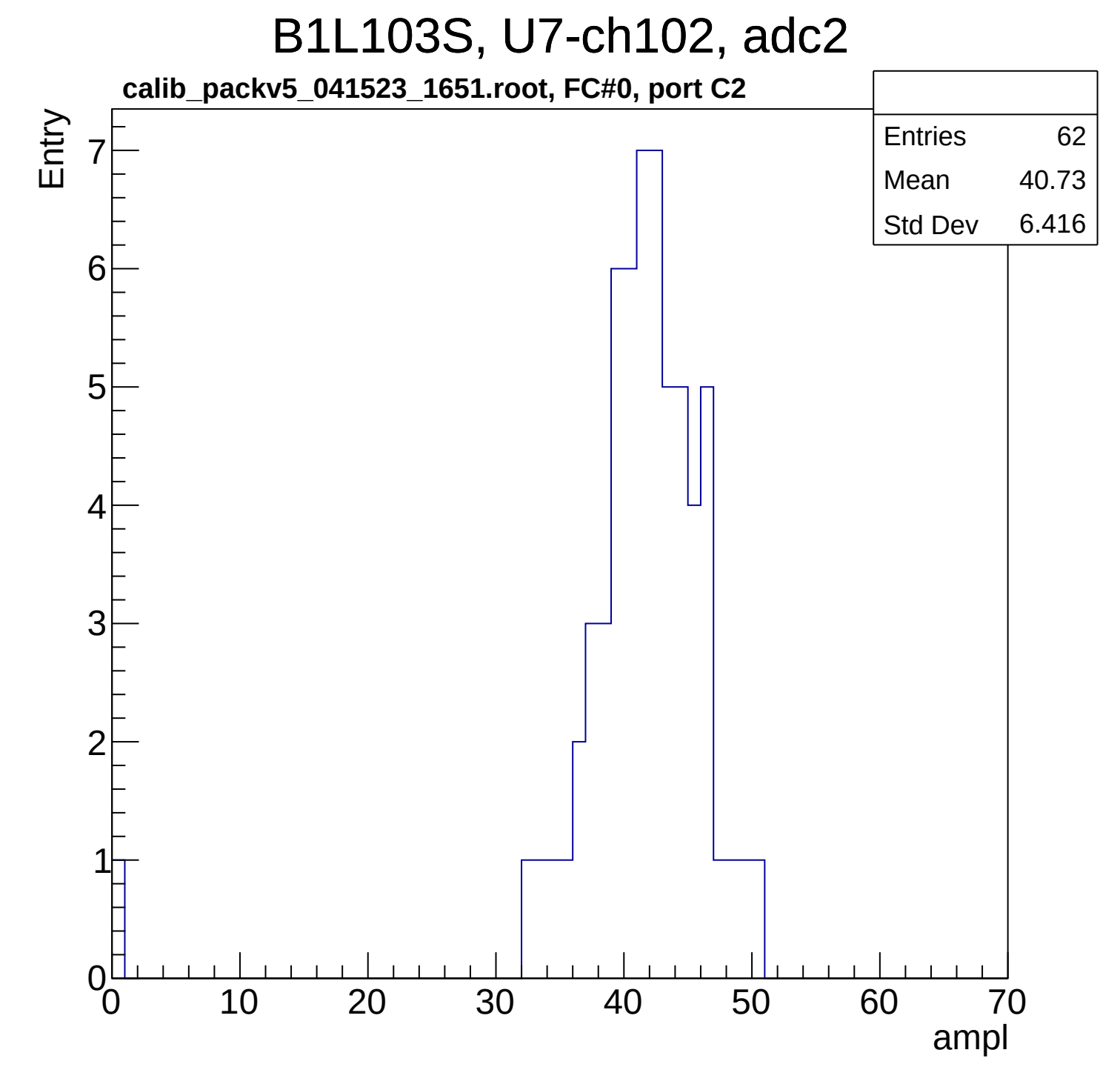
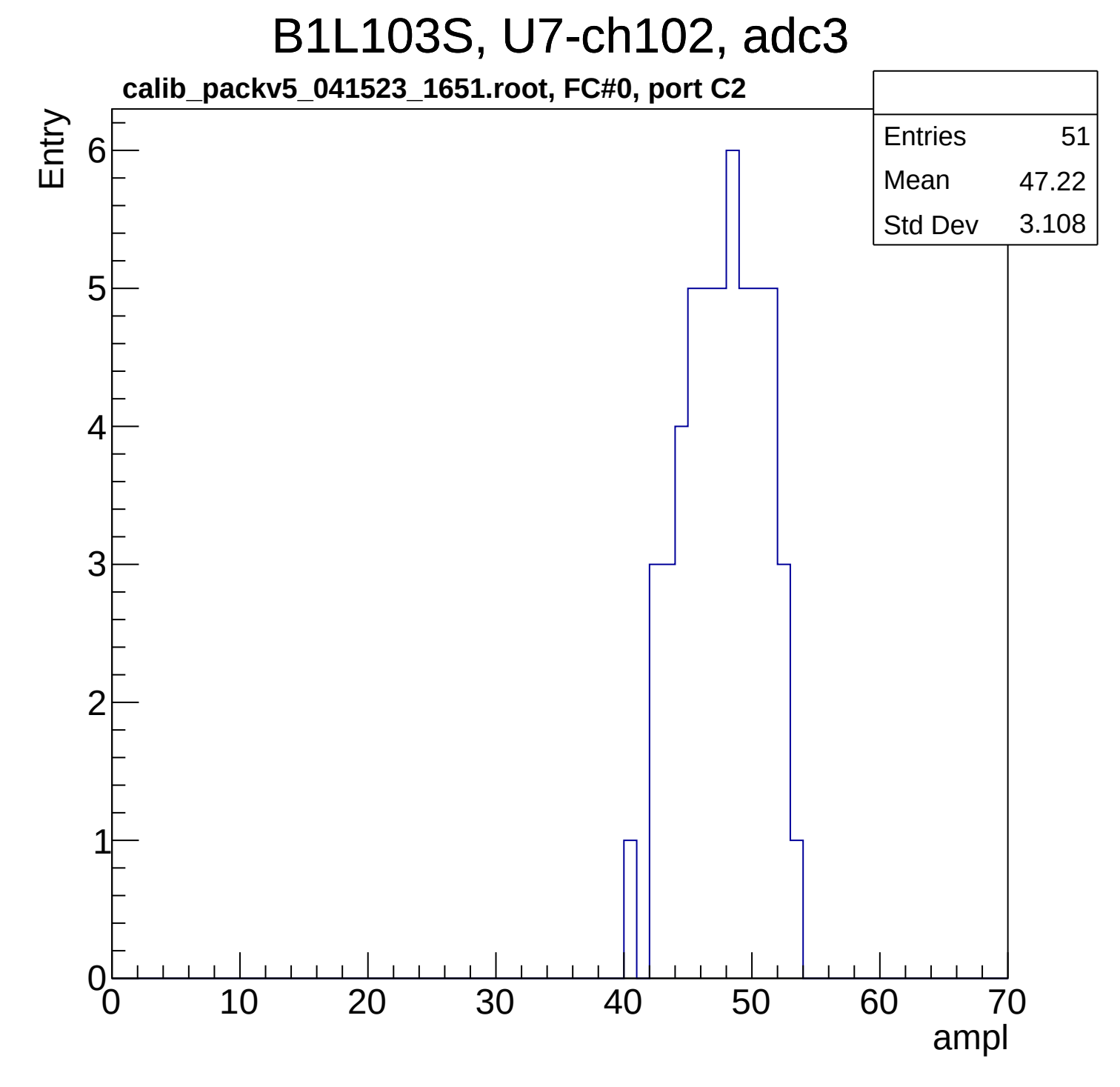
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch102, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 40.73
Std Dev 6.416
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U7-ch102, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 47.22
Std Dev 3.108
Entry
0
1
2
3
4
5
6
0
10
20
30
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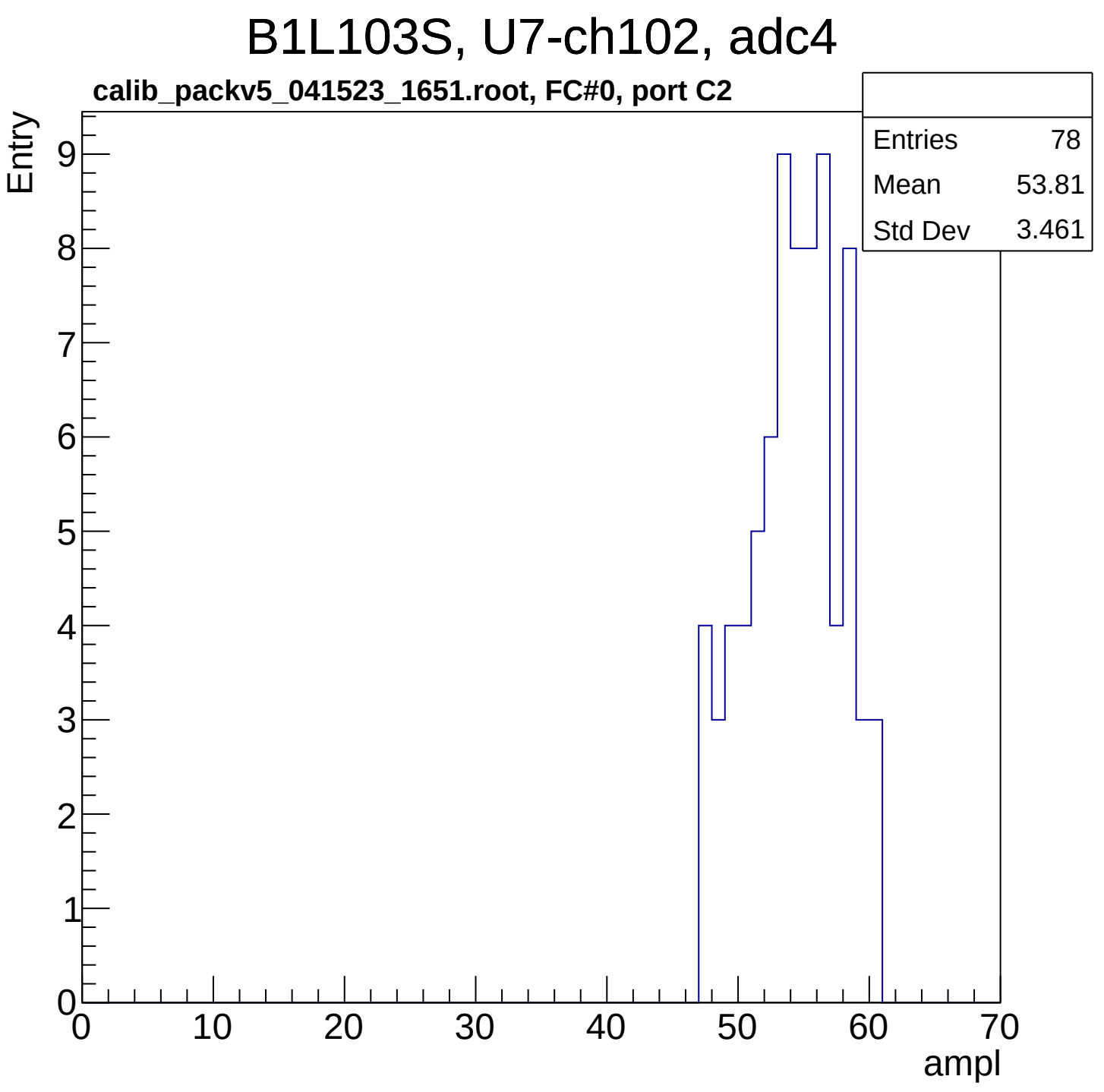
50
60
70
ampl


B1L103S, U7-ch102, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 53.81
Std Dev 3.461
Entry
ampl
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4
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6
7
8
9
0
10
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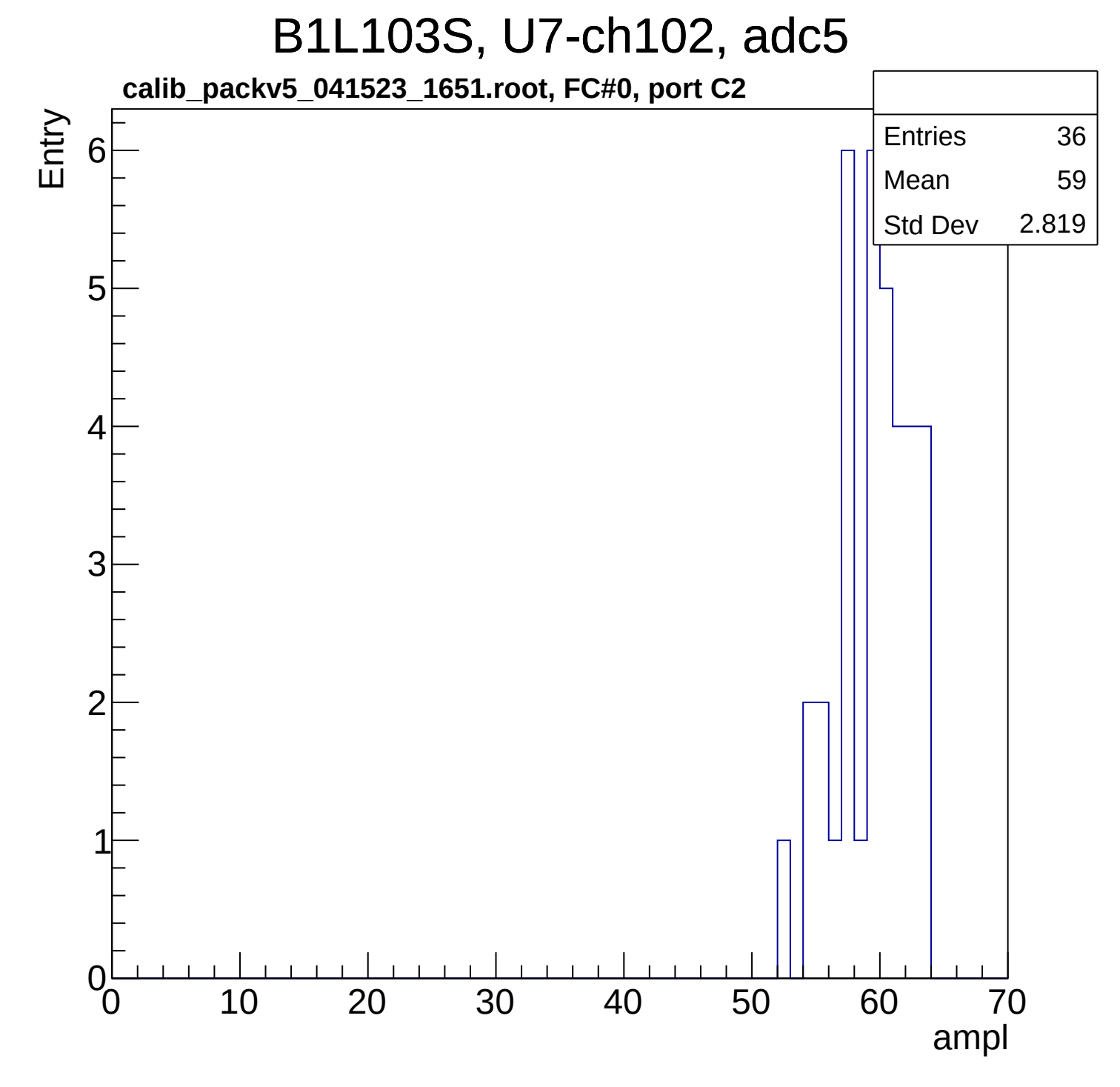
40
50
60
70


B1L103S, U7-ch102, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 36
Mean 59
Std Dev 2.819
Entry
0
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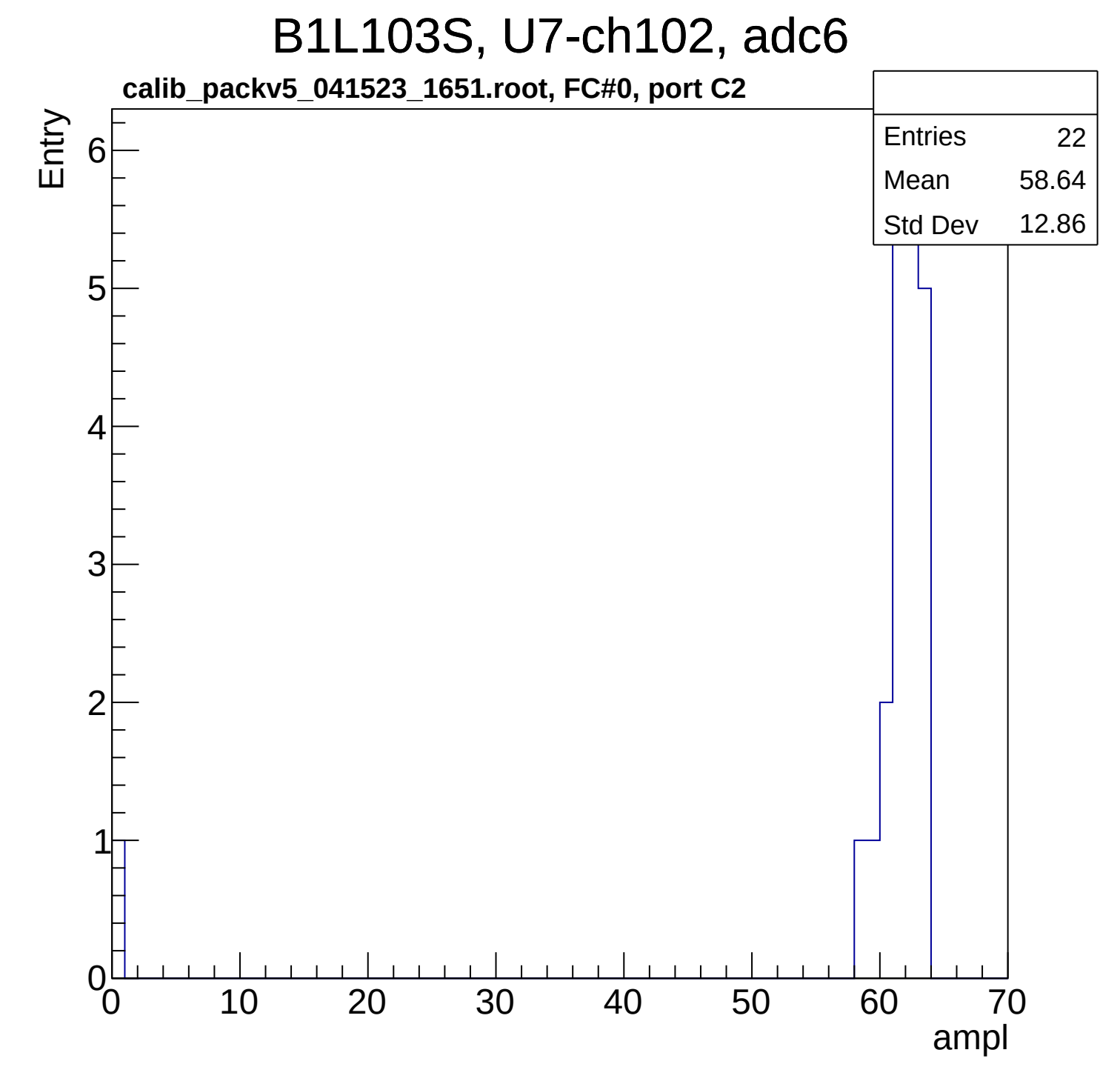
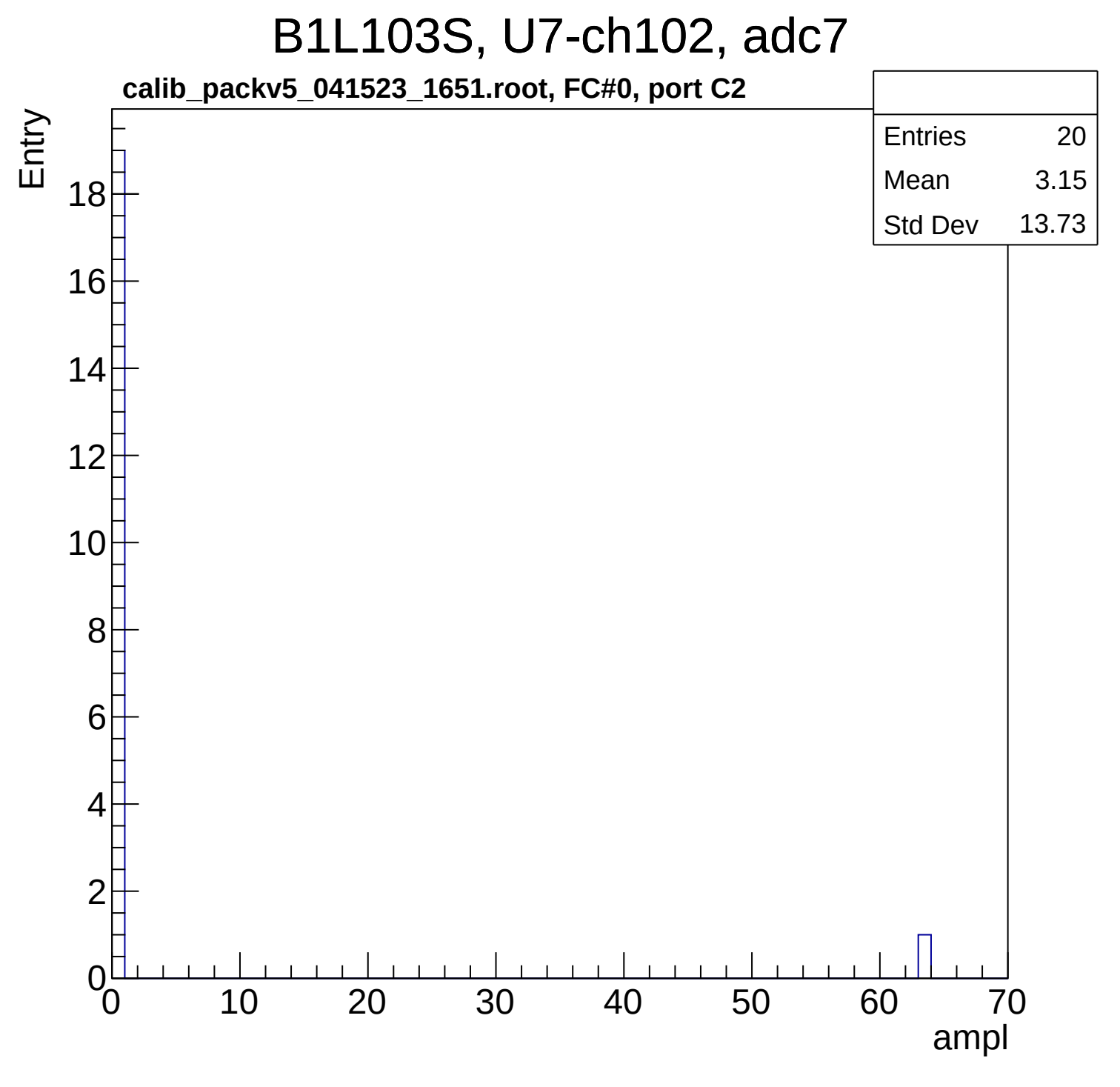
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch102, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 58.64
Std Dev 12.86
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U7-ch102, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
0
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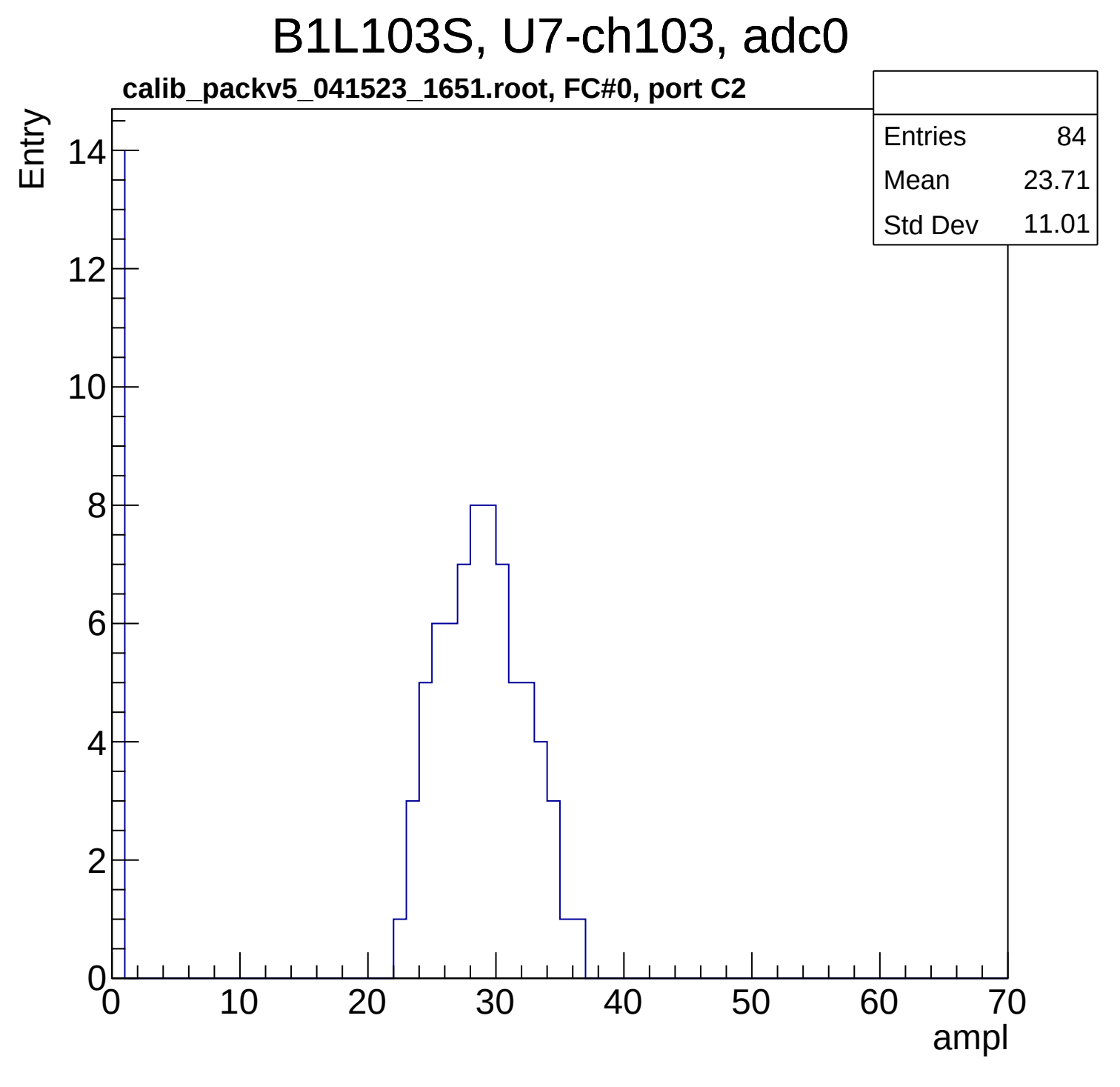
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch103, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 23.71
Std Dev 11.01
Entry
ampl
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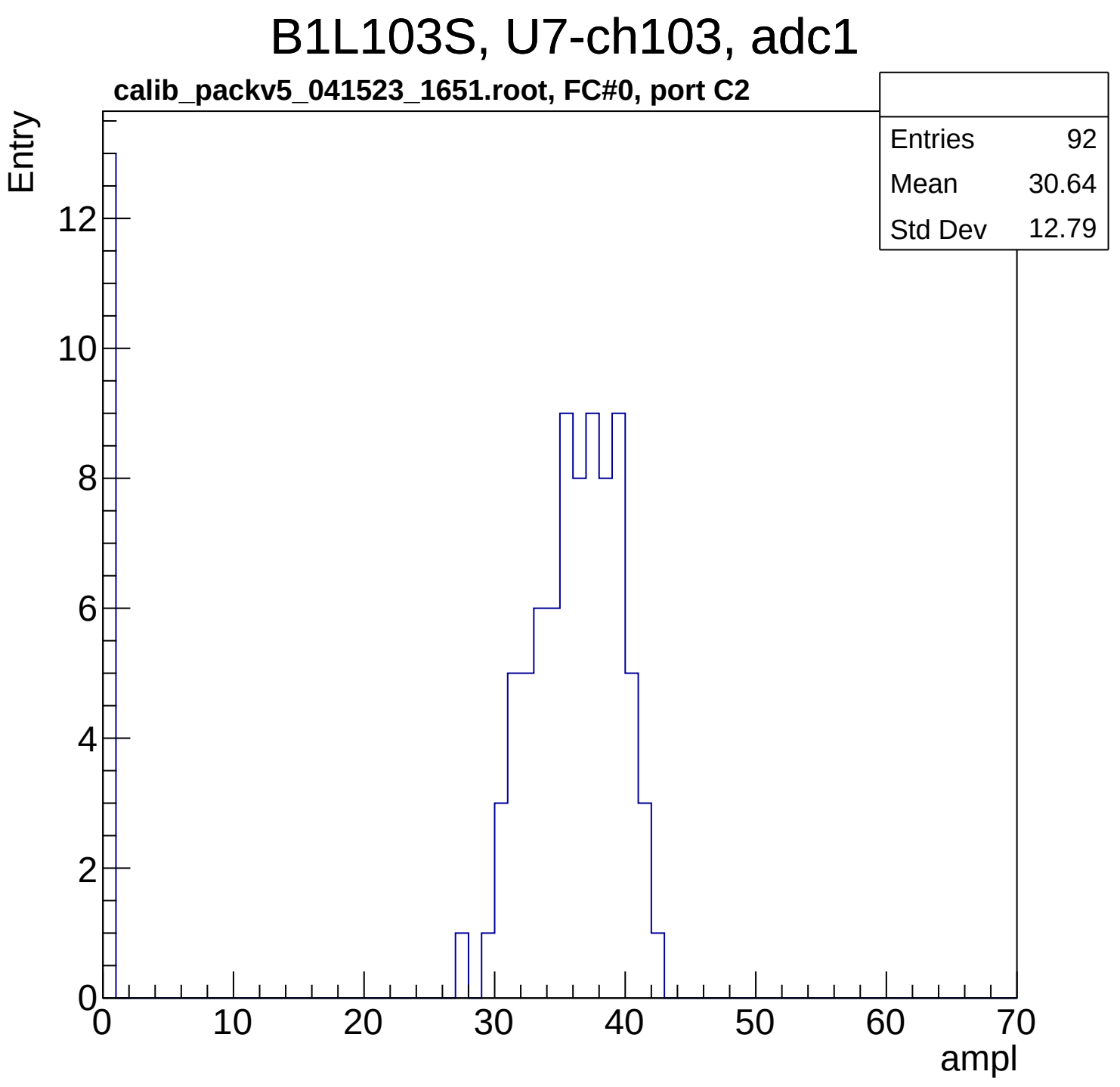
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L103S, U7-ch103, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 92
Mean 30.64
Std Dev 12.79
Entry
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4
6
8
10
12
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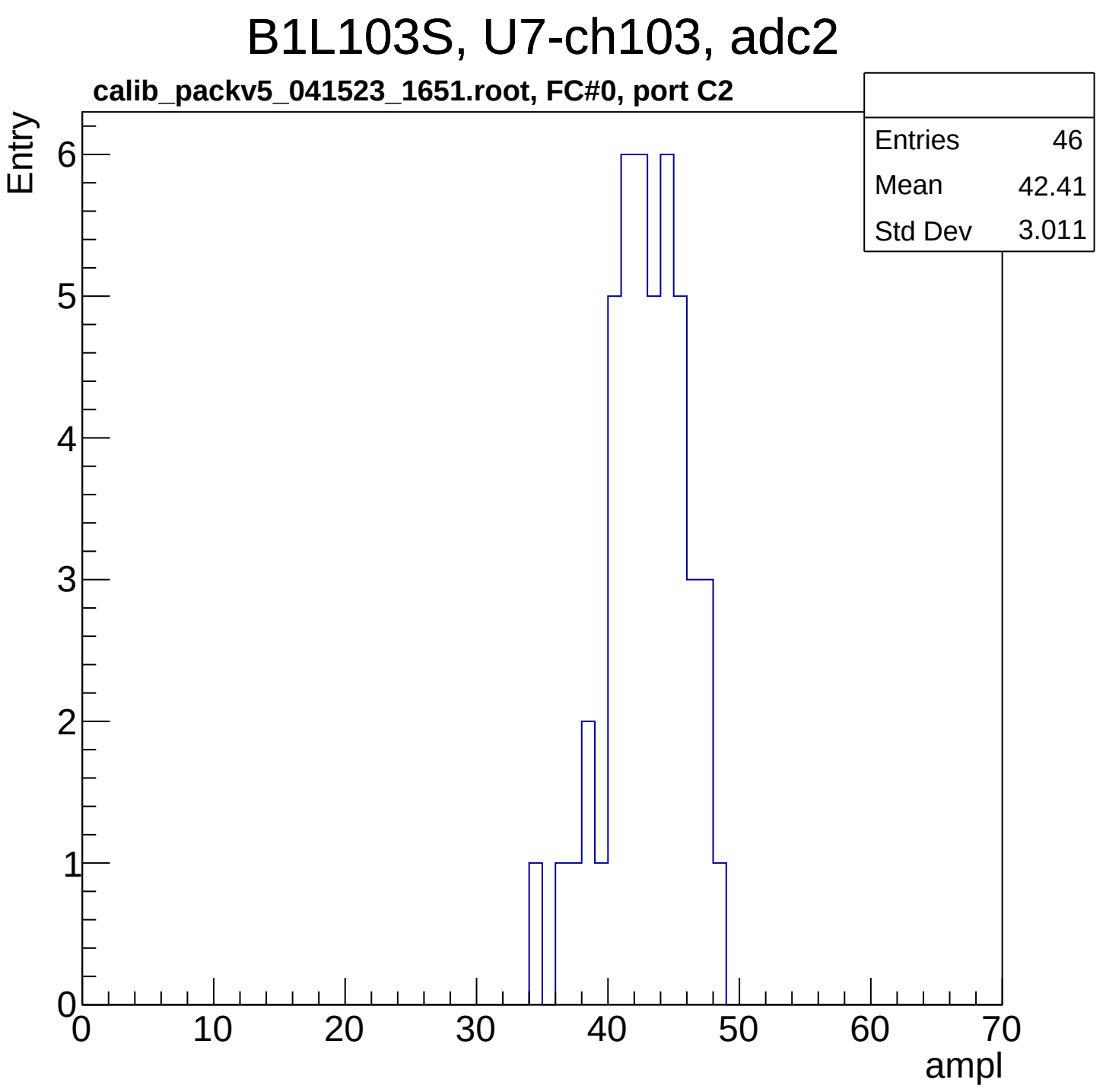
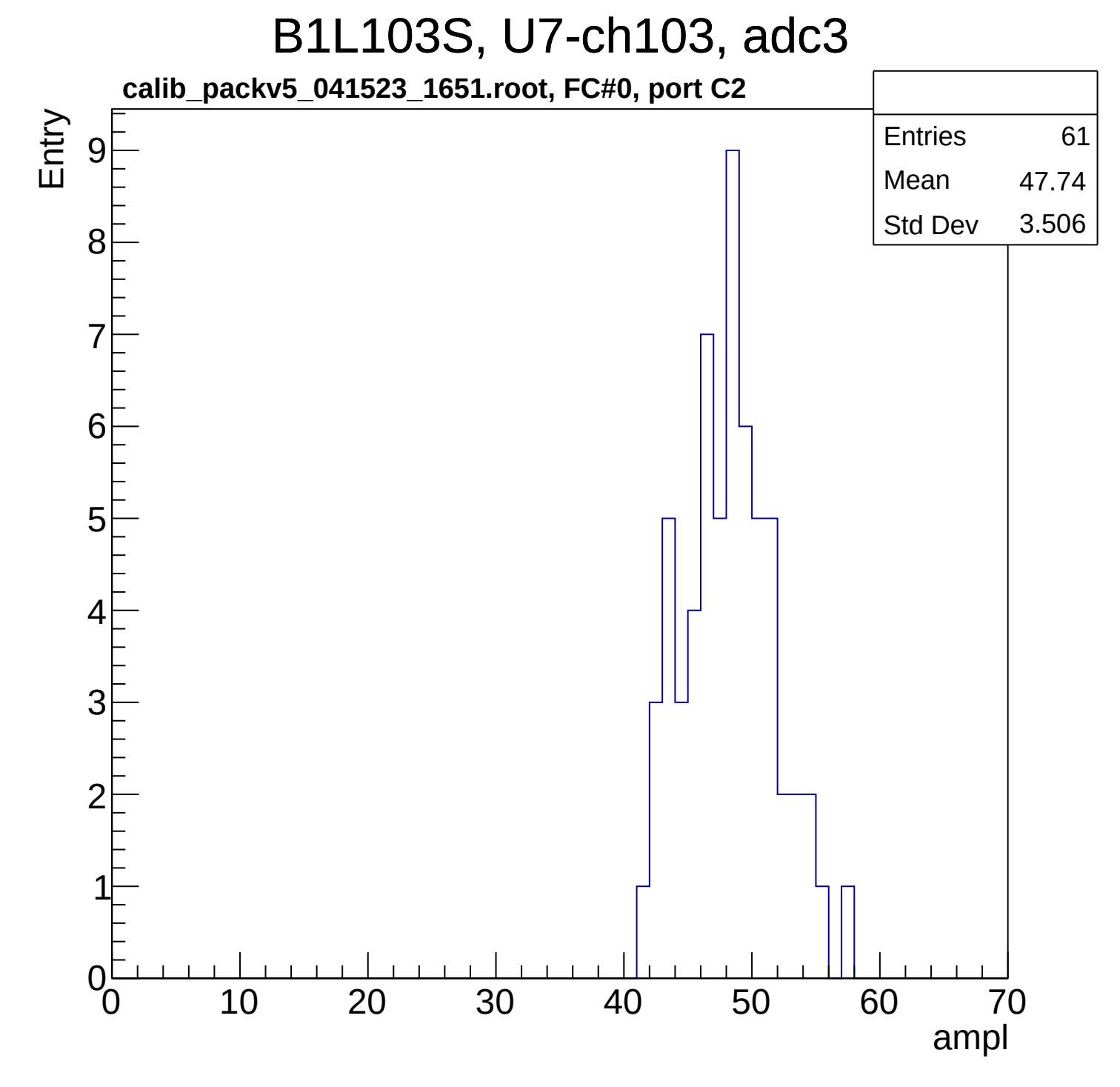
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch103, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 42.41
Std Dev 3.011
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch103, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 47.74
Std Dev 3.506
Entry
ampl
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3
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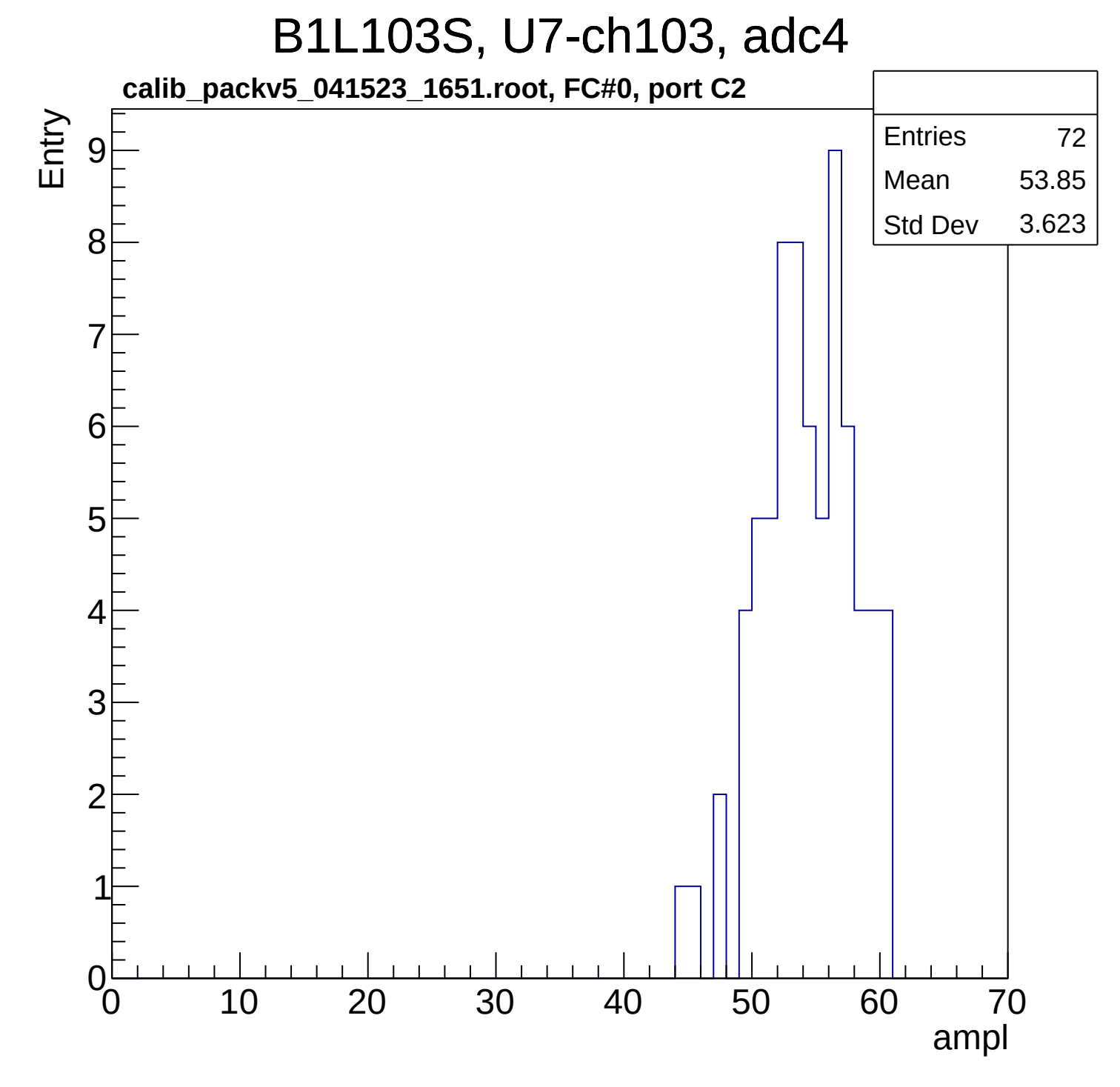
B1L103S, U7-ch103, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 53.85
Std Dev 3.623
Entry
ampl
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3
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6
7
8
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0
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60
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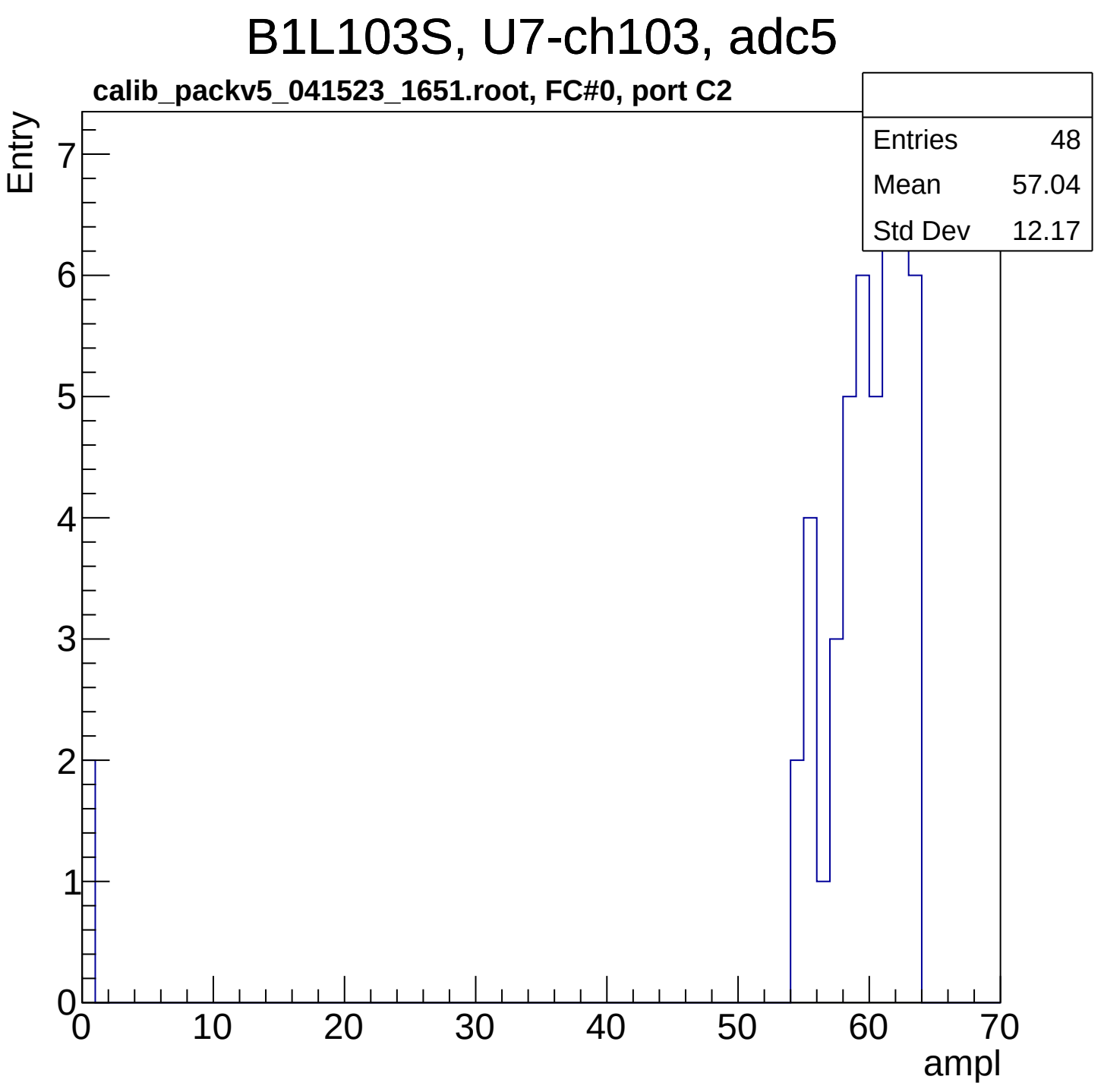
B1L103S, U7-ch103, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 57.04
Std Dev 12.17
Entry
ampl
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6
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0
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60
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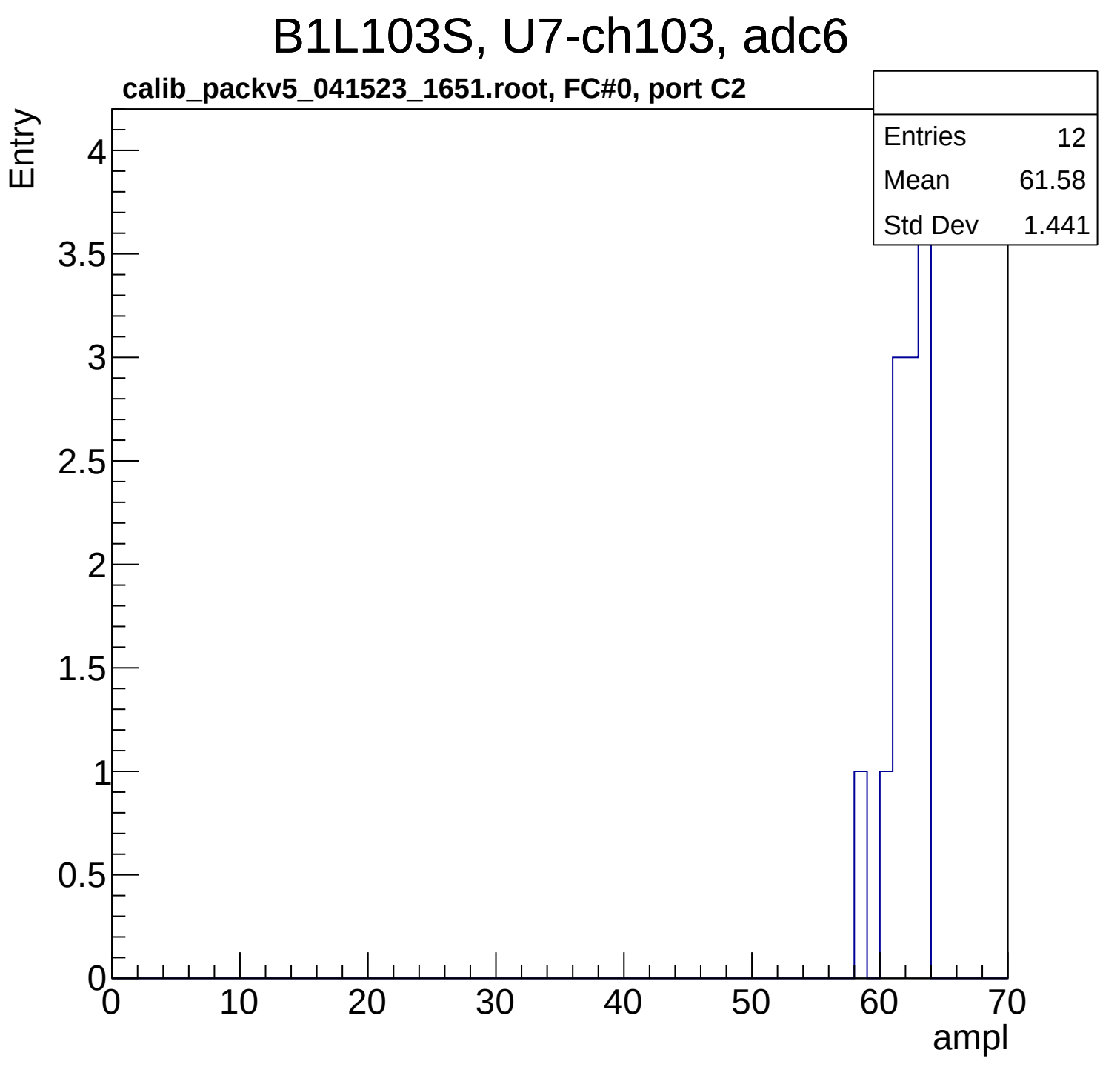
B1L103S, U7-ch103, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 61.58
Std Dev 1.441
Entry
ampl
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1.5
2
2.5
3
3.5
4
0
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40
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60
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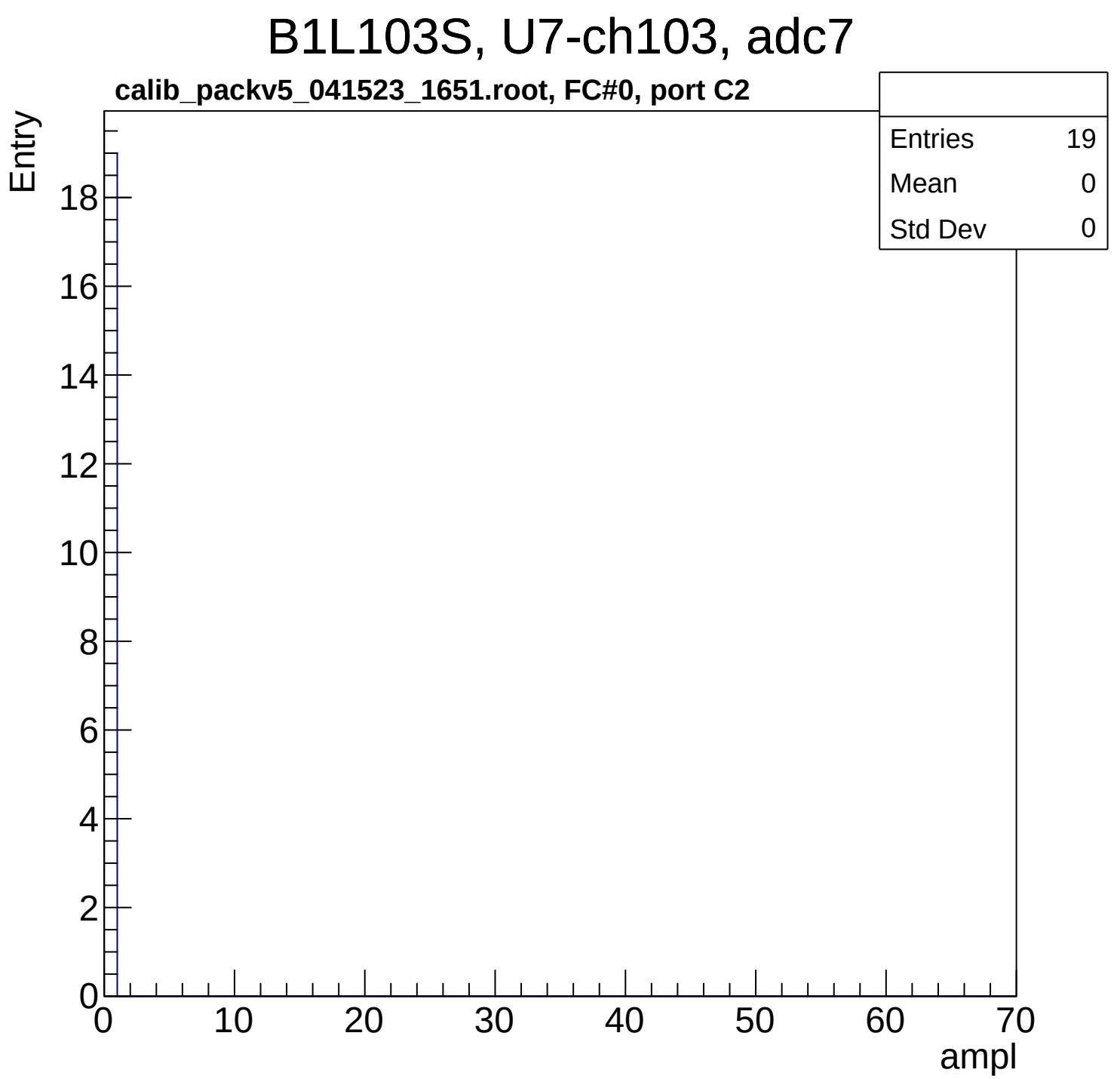
B1L103S, U7-ch103, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
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6
8
10
12
14
16
18
0
10
20
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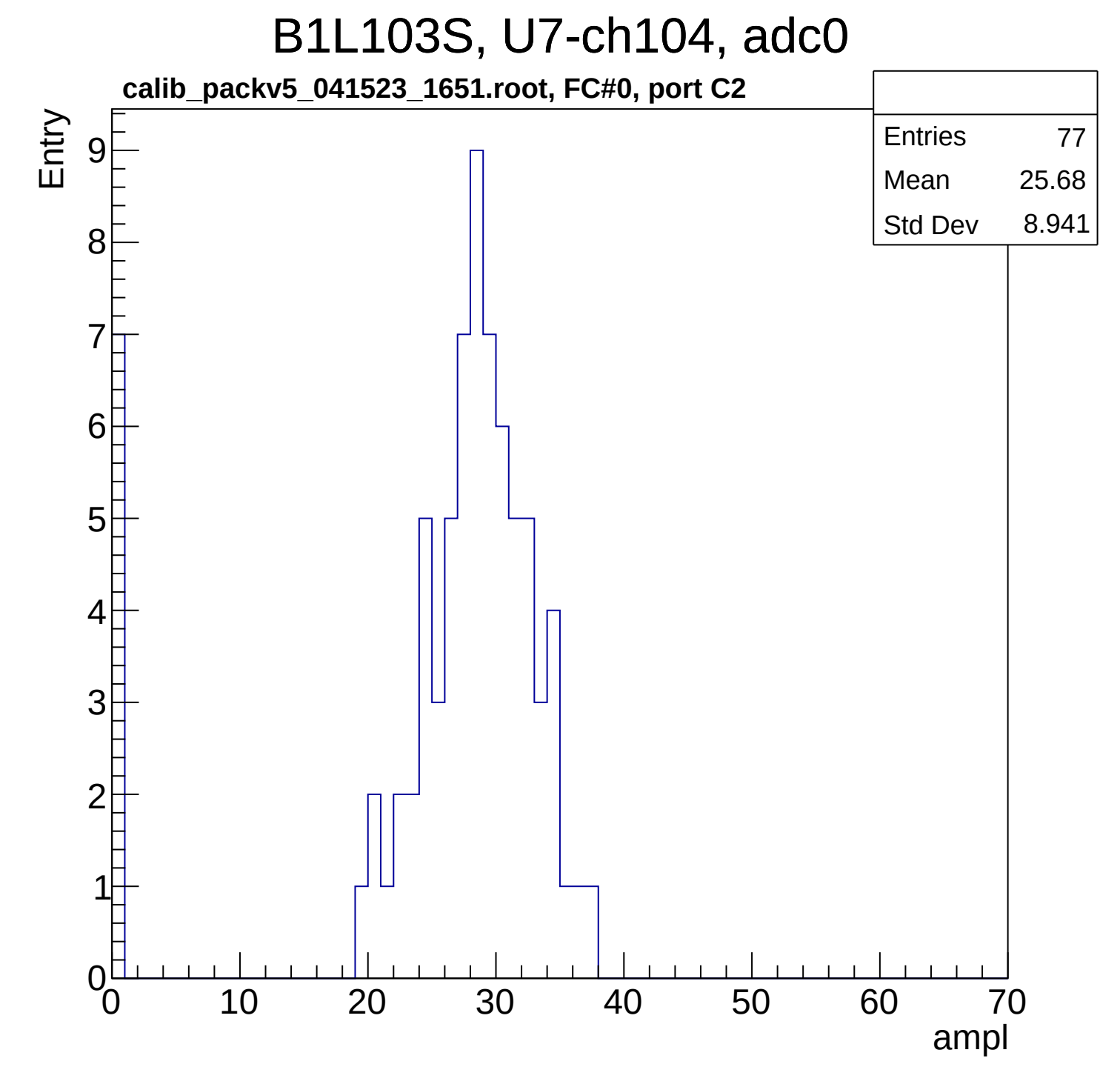
50
60
70
ampl


B1L103S, U7-ch104, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 25.68
Std Dev 8.941
Entry
ampl
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3
4
5
6
7
8
9
0
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40
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60
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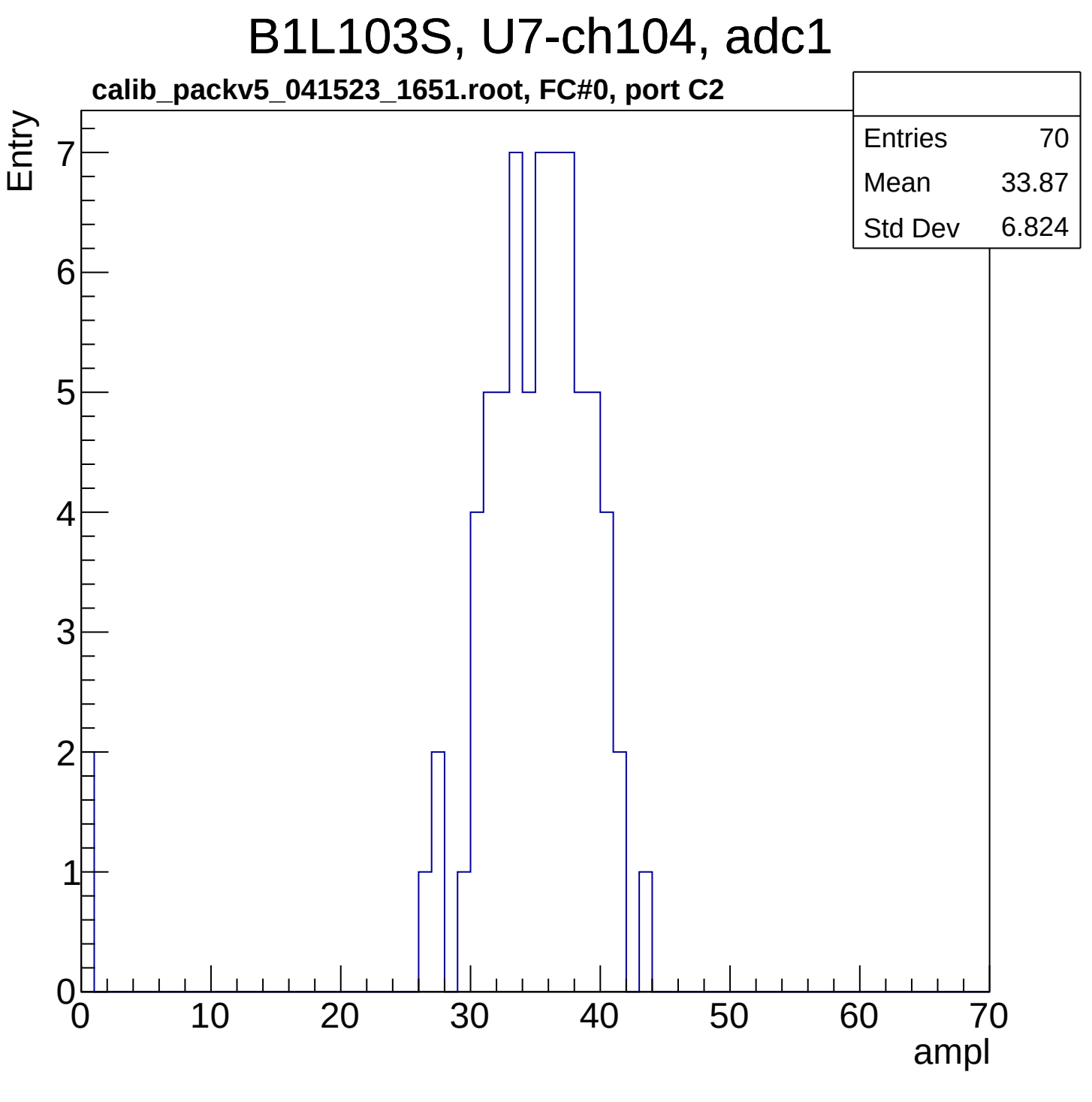
B1L103S, U7-ch104, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 33.87
Std Dev 6.824
Entry
ampl
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2
3
4
5
6
7
0
10
20
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40
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60
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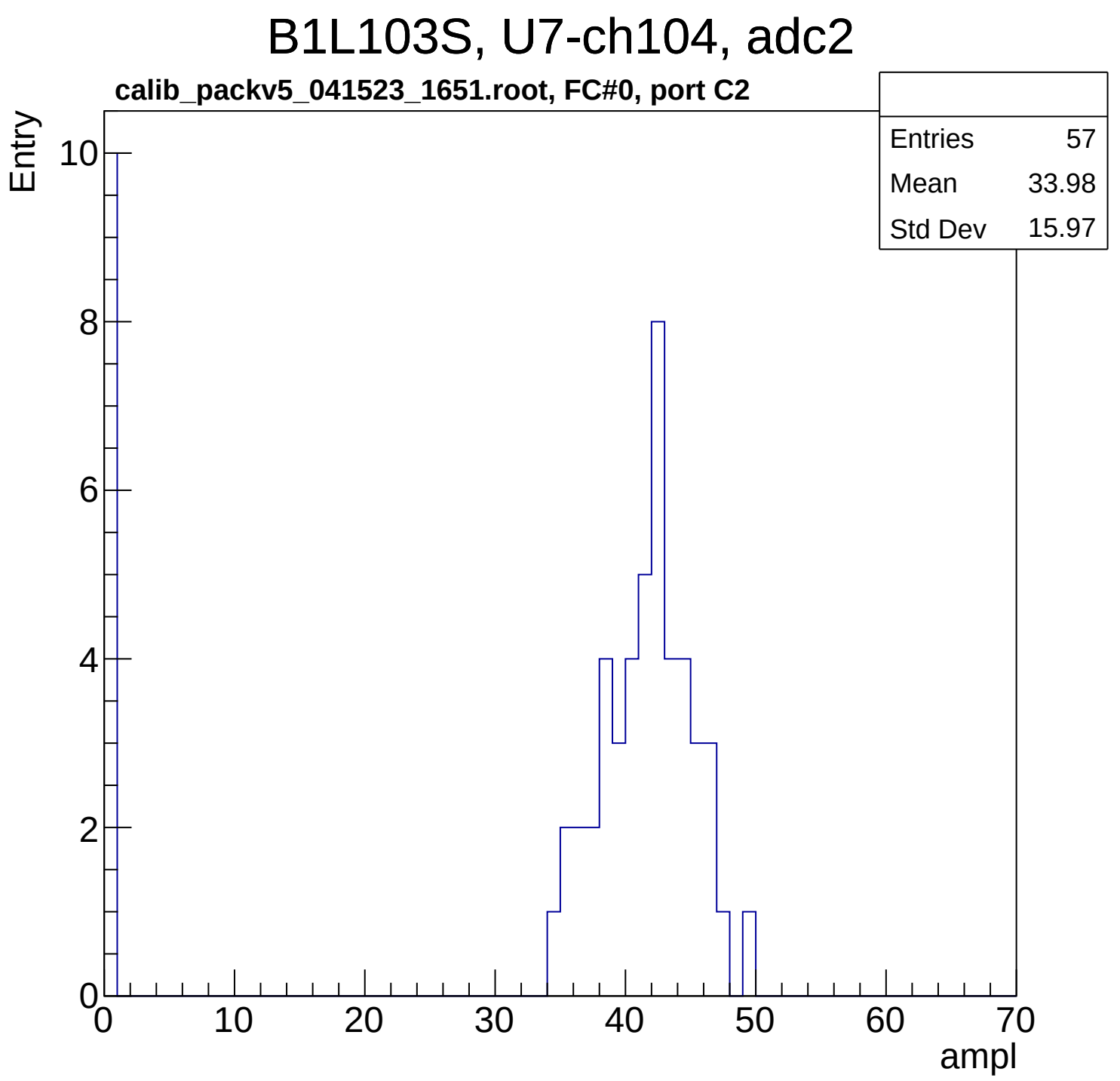
B1L103S, U7-ch104, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 33.98
Std Dev 15.97
Entry
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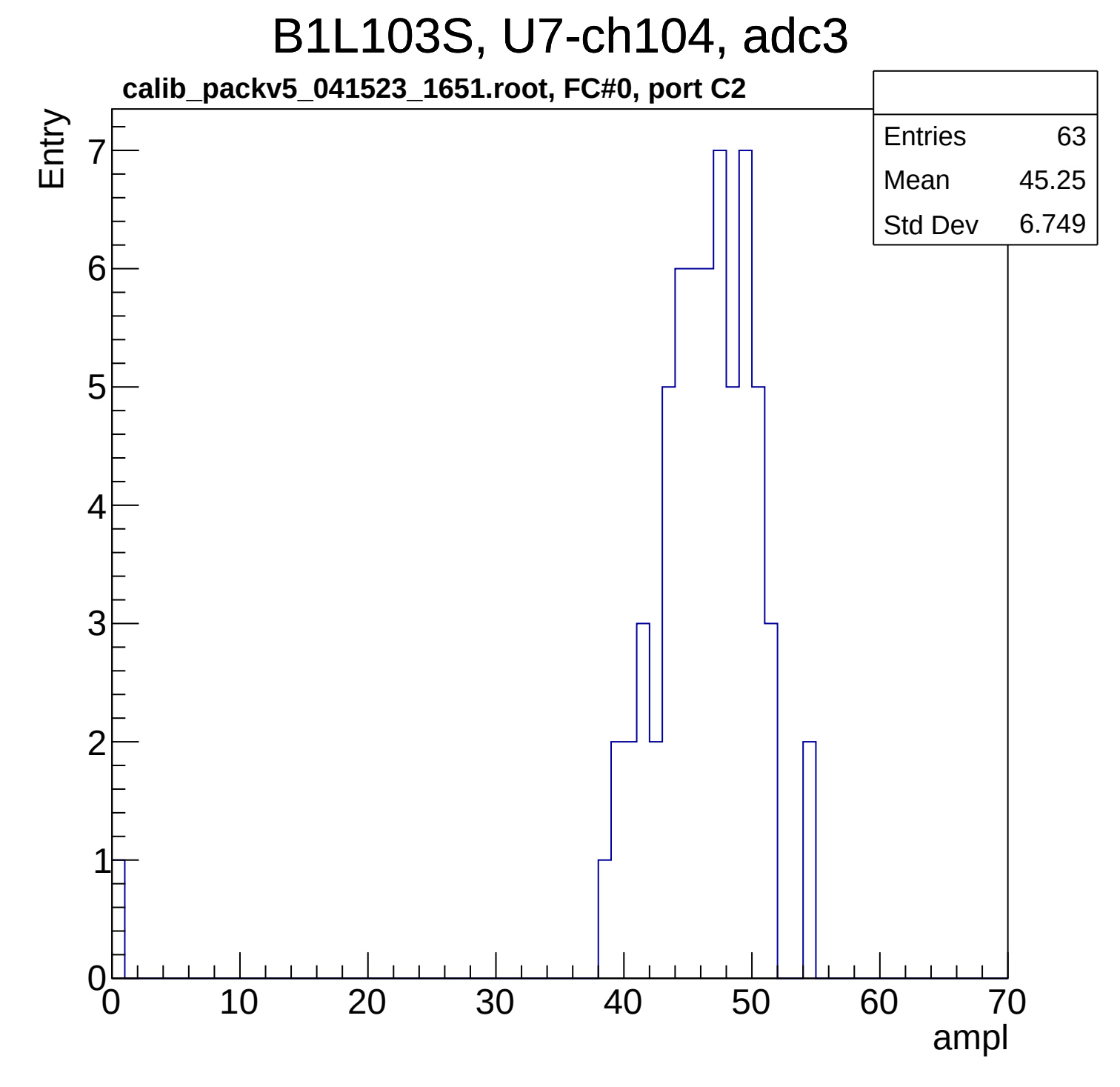
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch104, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 45.25
Std Dev 6.749
Entry
ampl
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3
4
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0
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20
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40
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60
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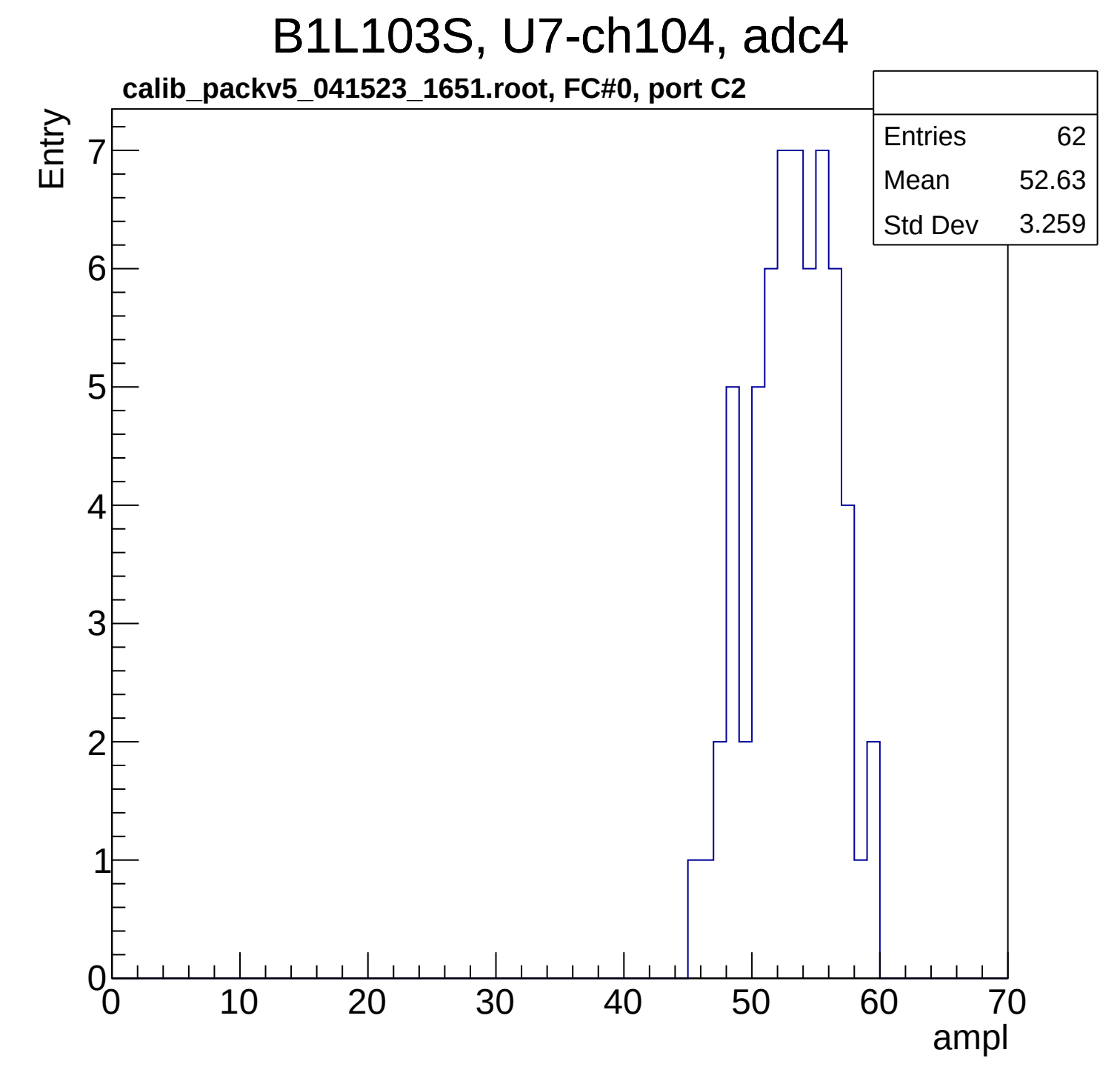
B1L103S, U7-ch104, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 52.63
Std Dev 3.259
Entry
ampl
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3
4
5
6
7
0
10
20
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40
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60
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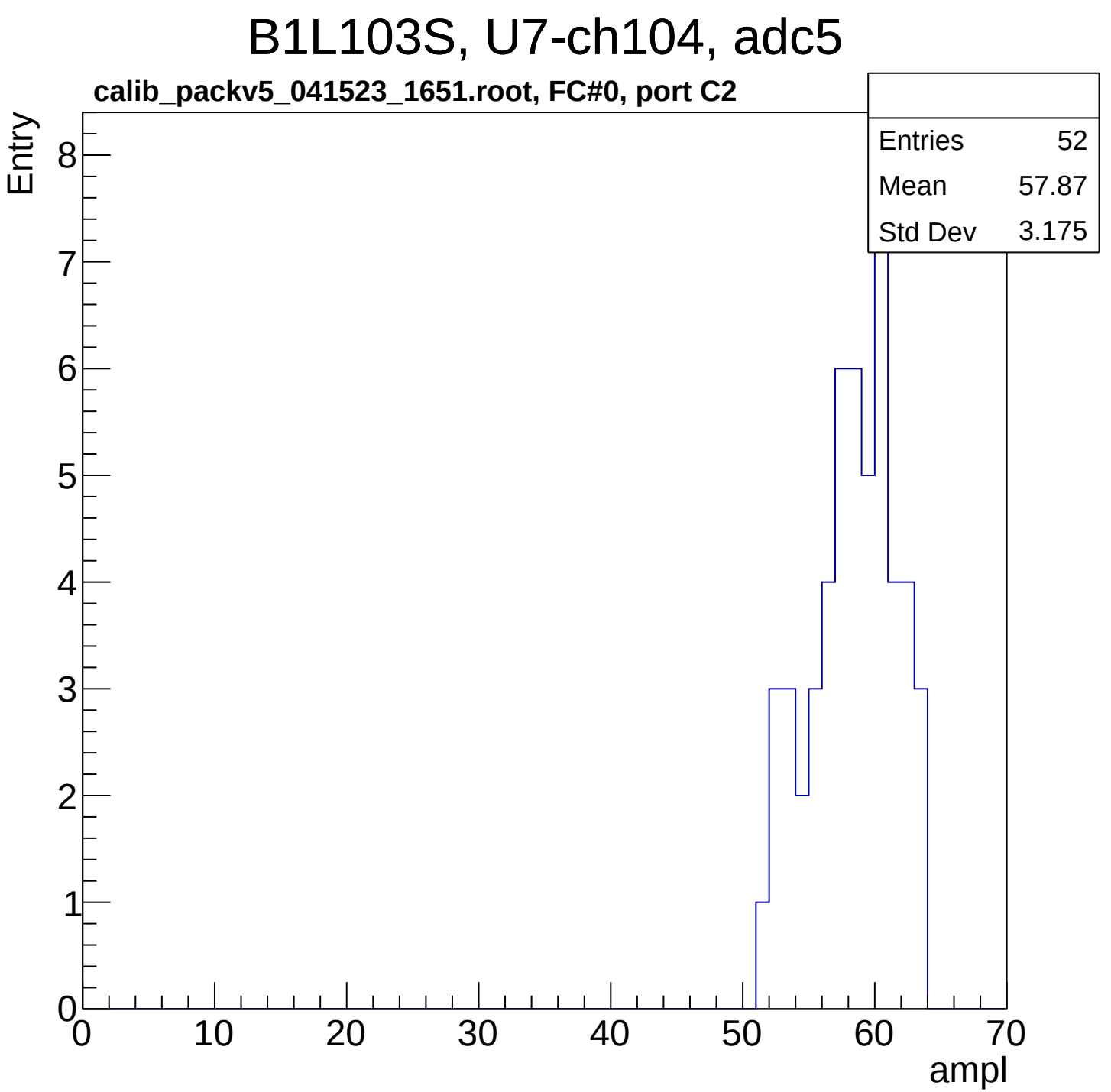
B1L103S, U7-ch104, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 57.87
Std Dev 3.175
Entry
ampl
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2
3
4
5
6
7
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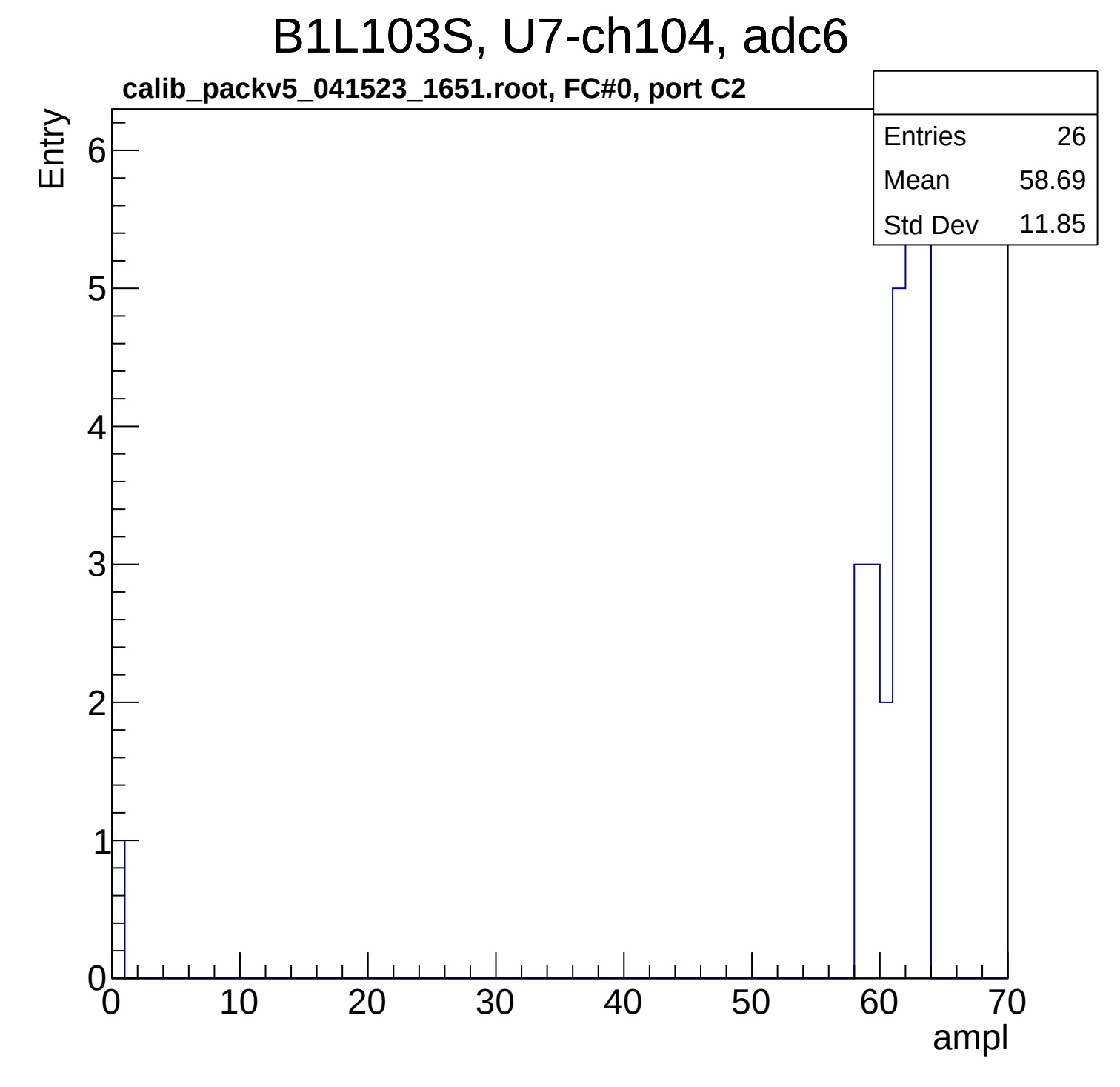
B1L103S, U7-ch104, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 26
Mean 58.69
Std Dev 11.85
Entry
ampl
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3
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0
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20
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40
50
60
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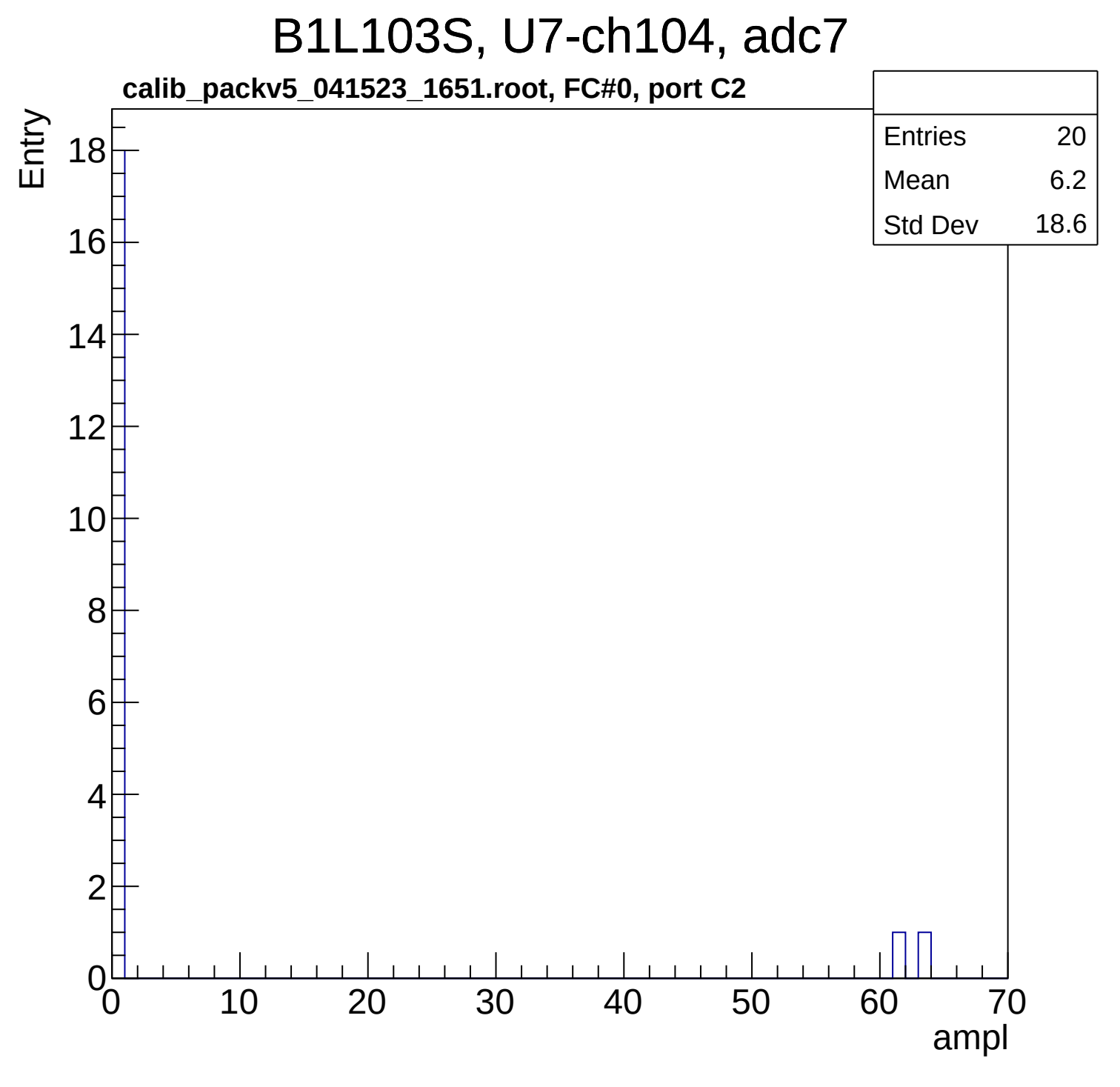
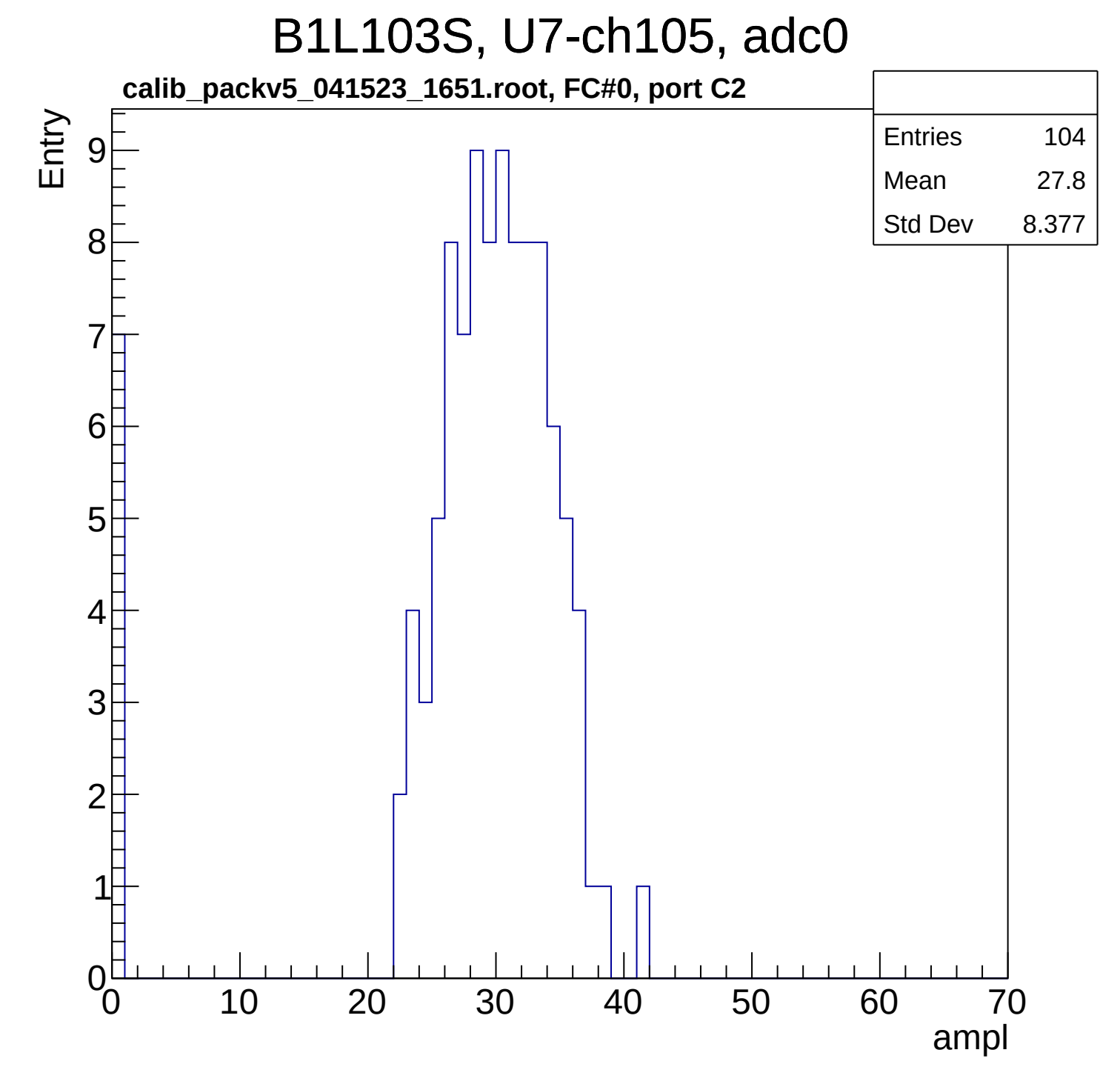

B1L103S, U7-ch104, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 6.2
Std Dev 18.6
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch105, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 104
Mean 27.8
Std Dev 8.377
Entry
ampl
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3
4
5
6
7
8
9
0
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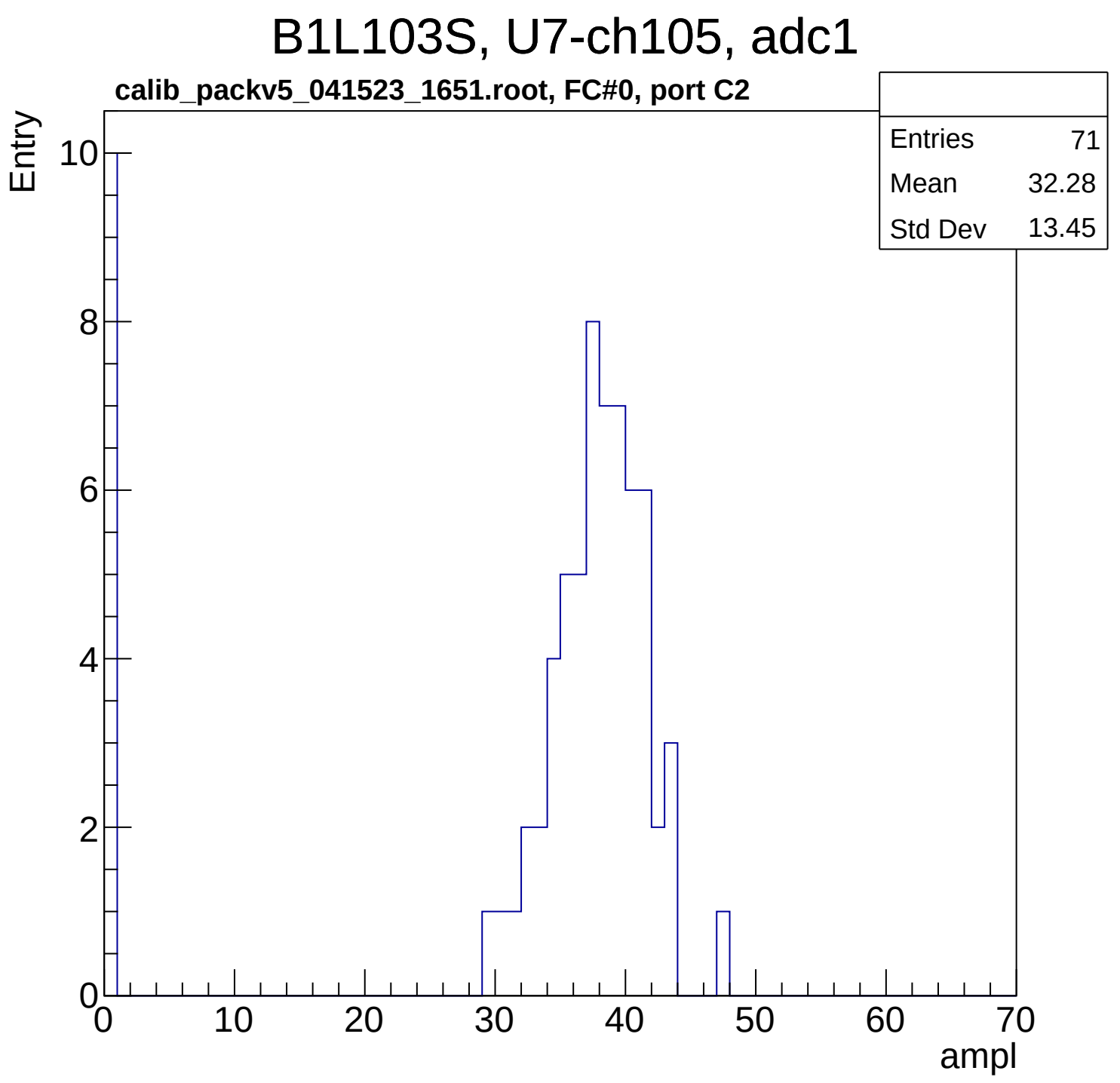
B1L103S, U7-ch105, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 32.28
Std Dev 13.45
Entry
ampl
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4
6
8
10
0
10
20
30
40
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60
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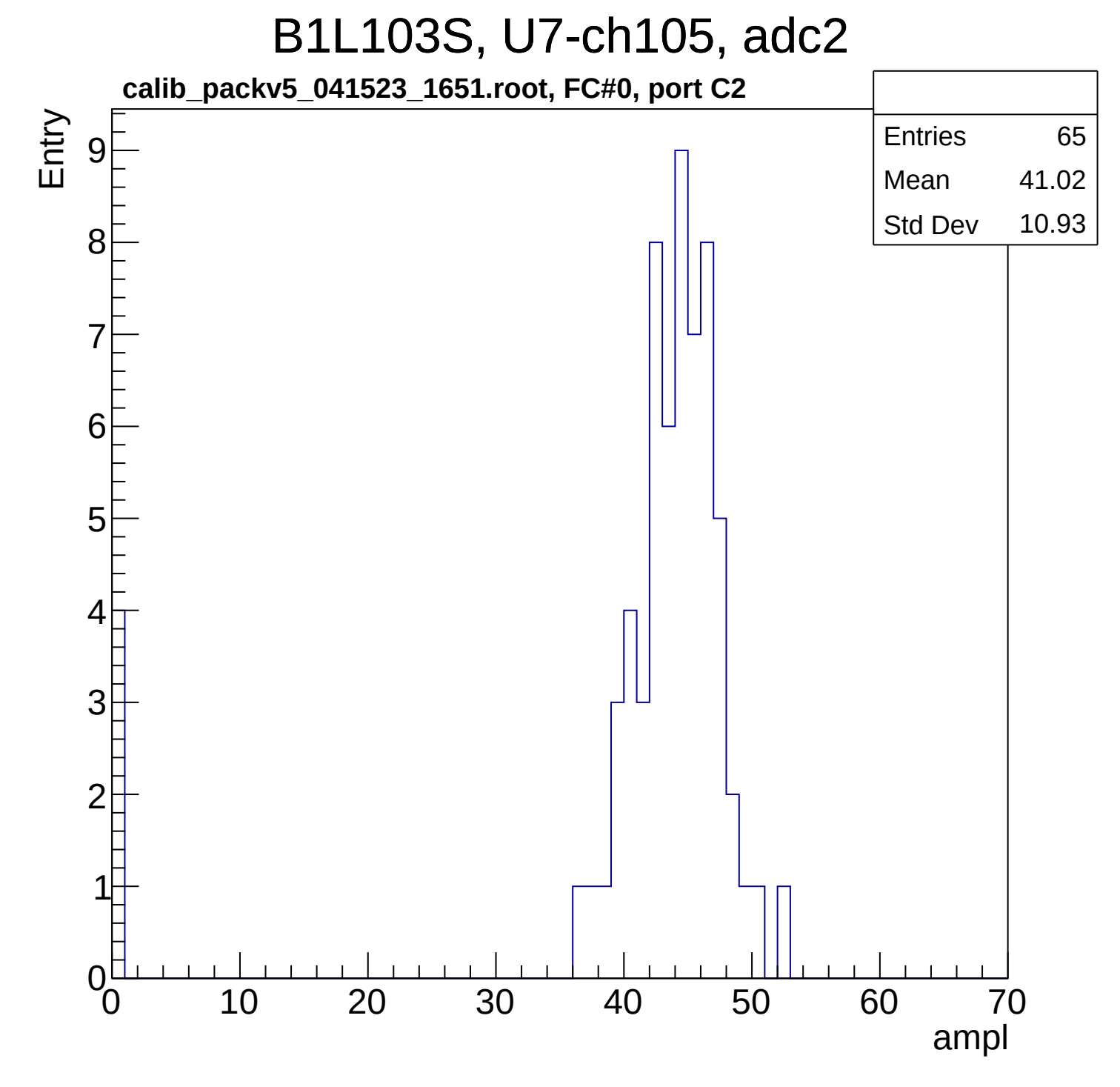
B1L103S, U7-ch105, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 41.02
Std Dev 10.93
Entry
ampl
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4
5
6
7
8
9
0
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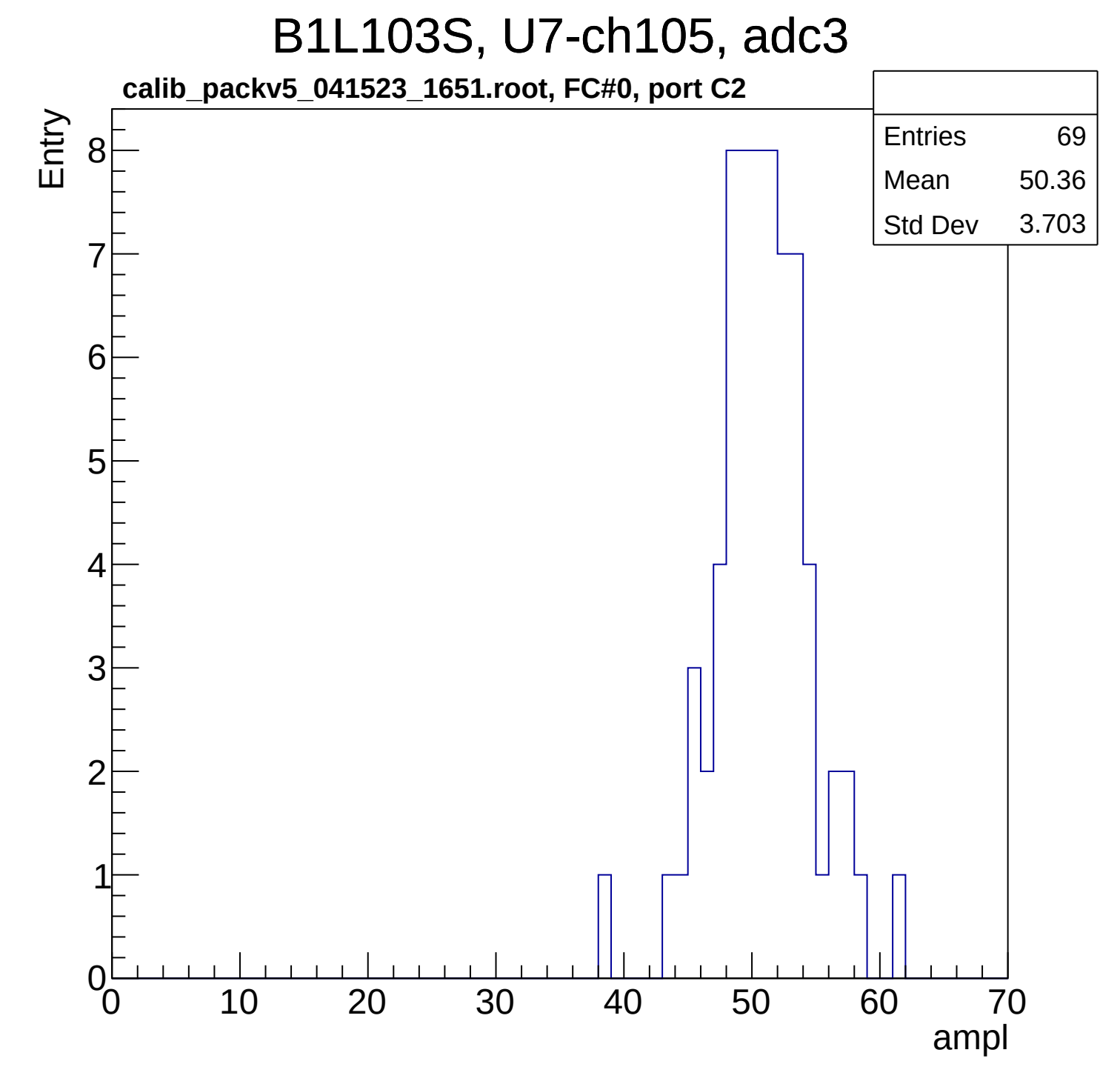
B1L103S, U7-ch105, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 50.36
Std Dev 3.703
Entry
ampl
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4
5
6
7
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0
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40
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60
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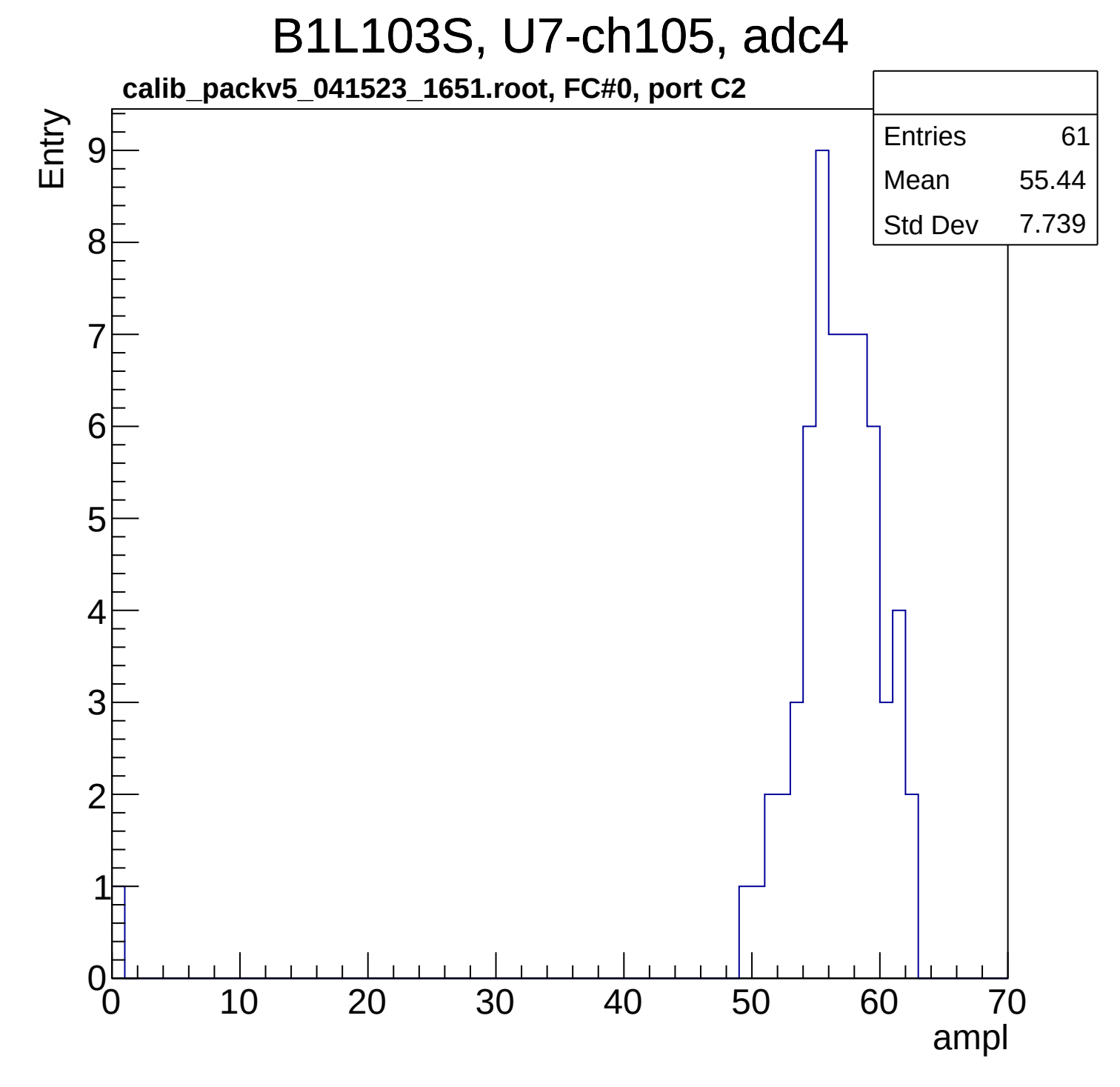
B1L103S, U7-ch105, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 55.44
Std Dev 7.739
Entry
ampl
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3
4
5
6
7
8
9
0
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20
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40
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60
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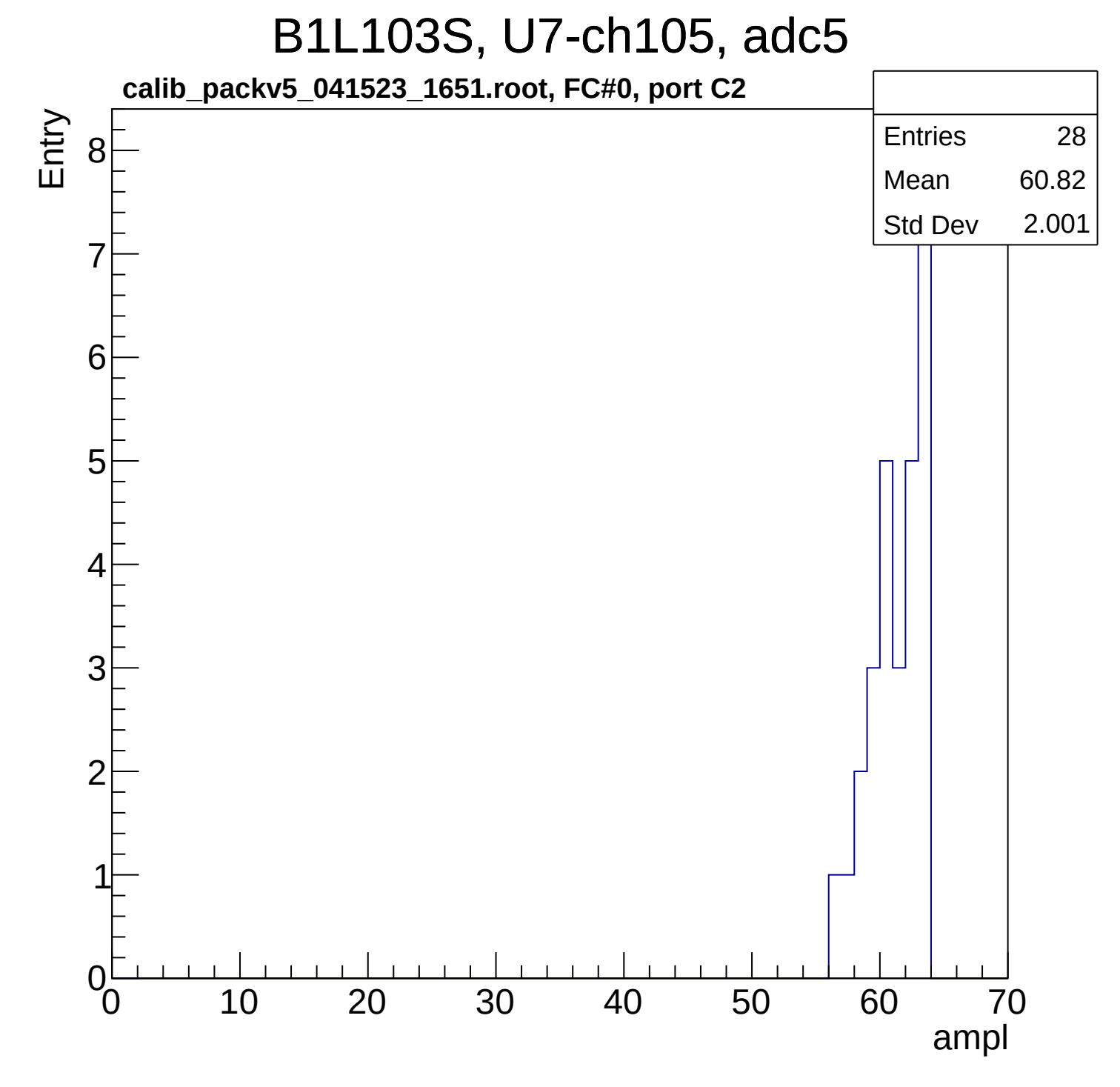
B1L103S, U7-ch105, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 28
Mean 60.82
Std Dev 2.001
Entry
ampl
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2
3
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5
6
7
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0
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20
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40
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60
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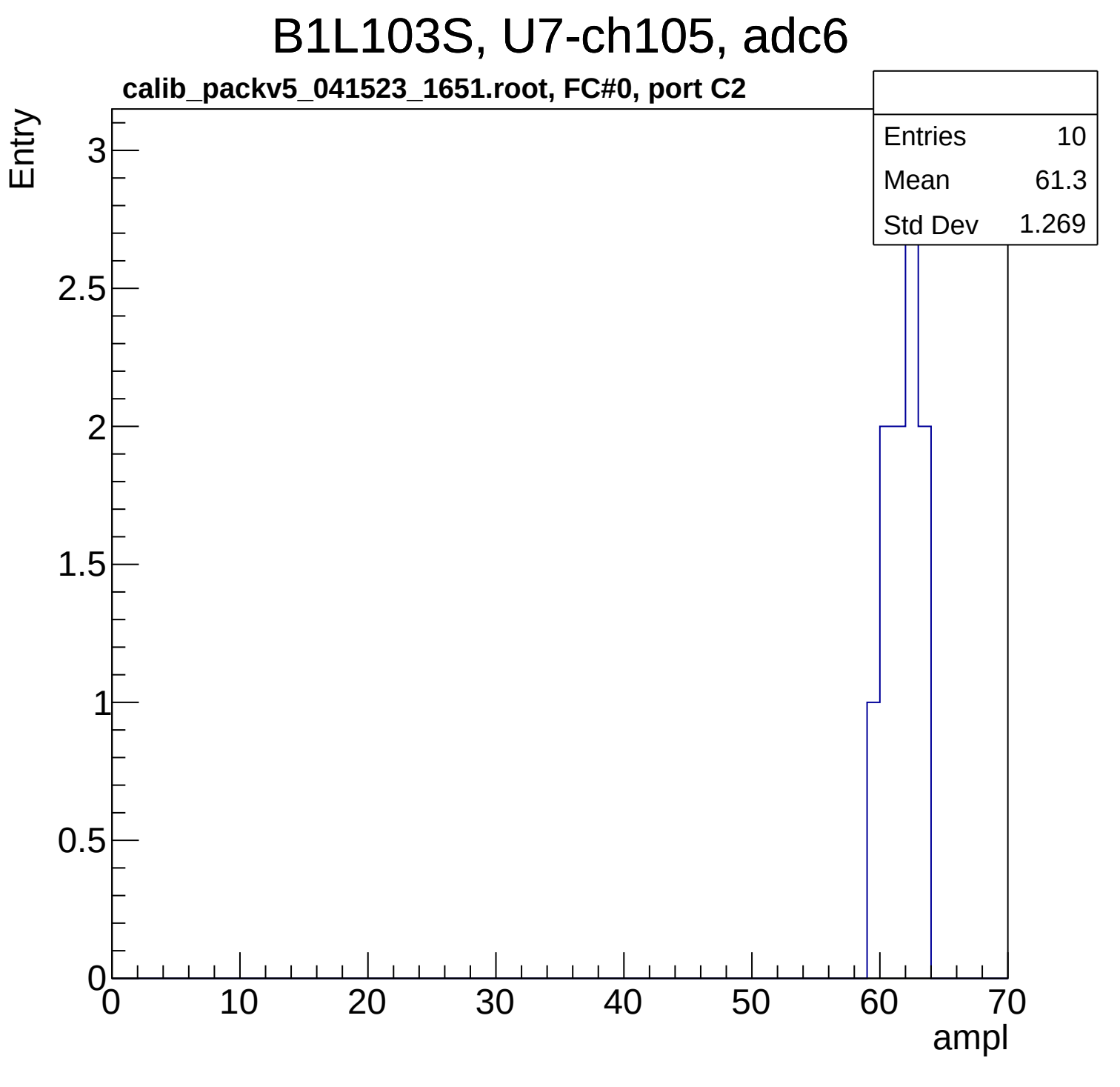
B1L103S, U7-ch105, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 61.3
Std Dev 1.269
Entry
ampl
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1.5
2
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0
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20
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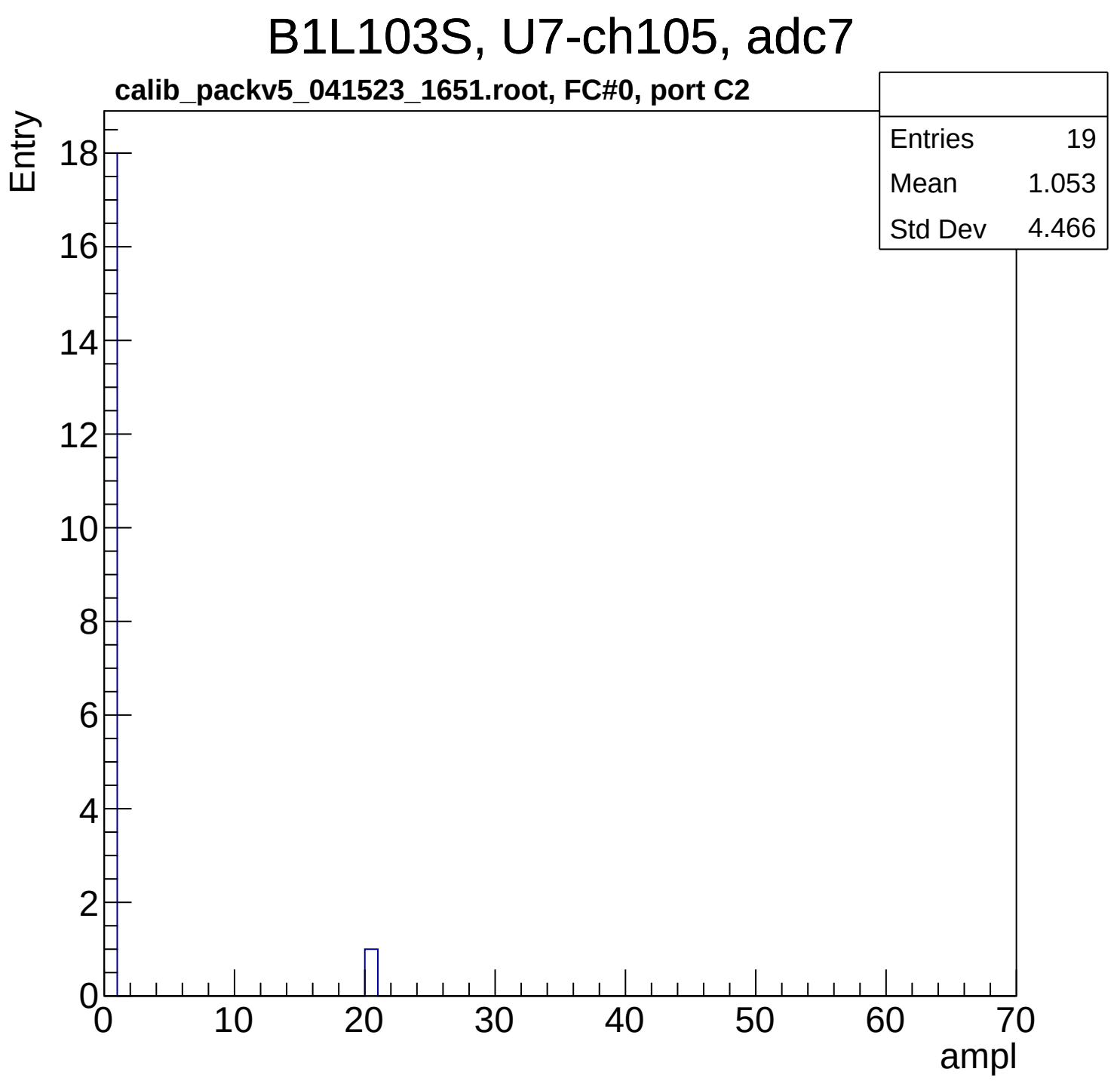
B1L103S, U7-ch105, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.053
Std Dev 4.466
Entry
ampl
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6
8
10
12
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16
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0
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60
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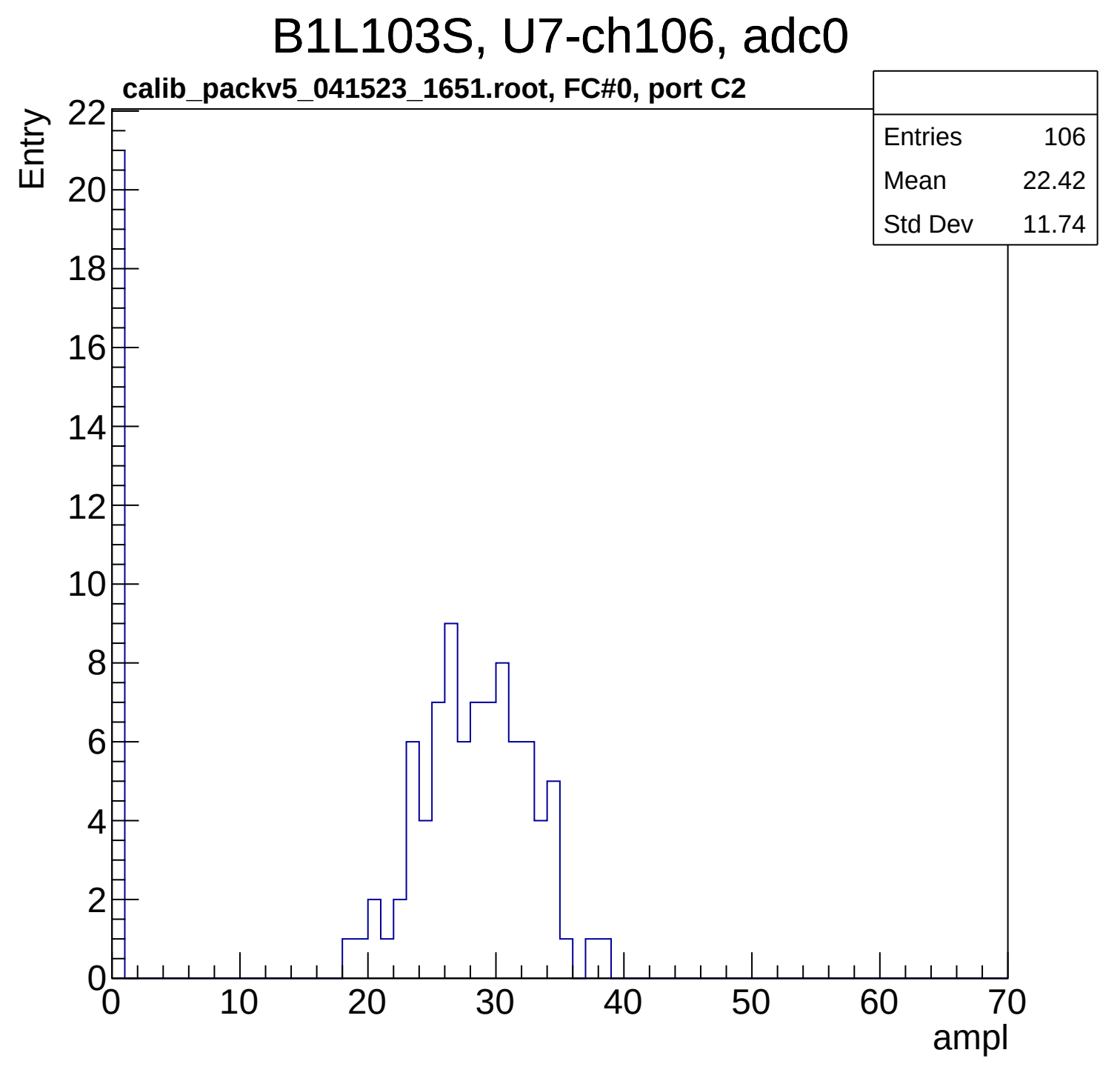
B1L103S, U7-ch106, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 106
Mean 22.42
Std Dev 11.74
Entry
ampl
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8
10
12
14
16
18
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0
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60
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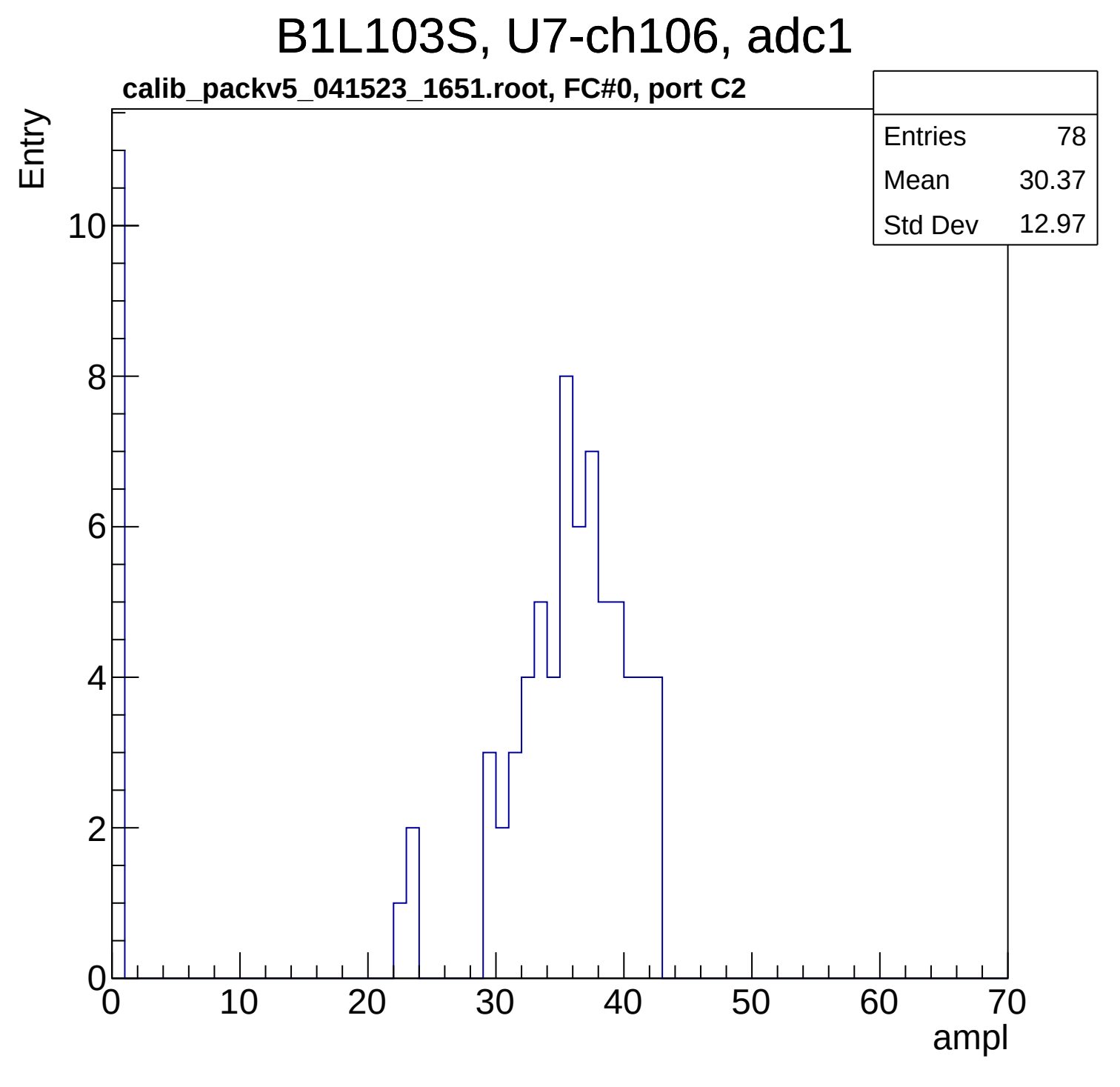
B1L103S, U7-ch106, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 30.37
Std Dev 12.97
Entry
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4
6
8
10
0
10
20
30
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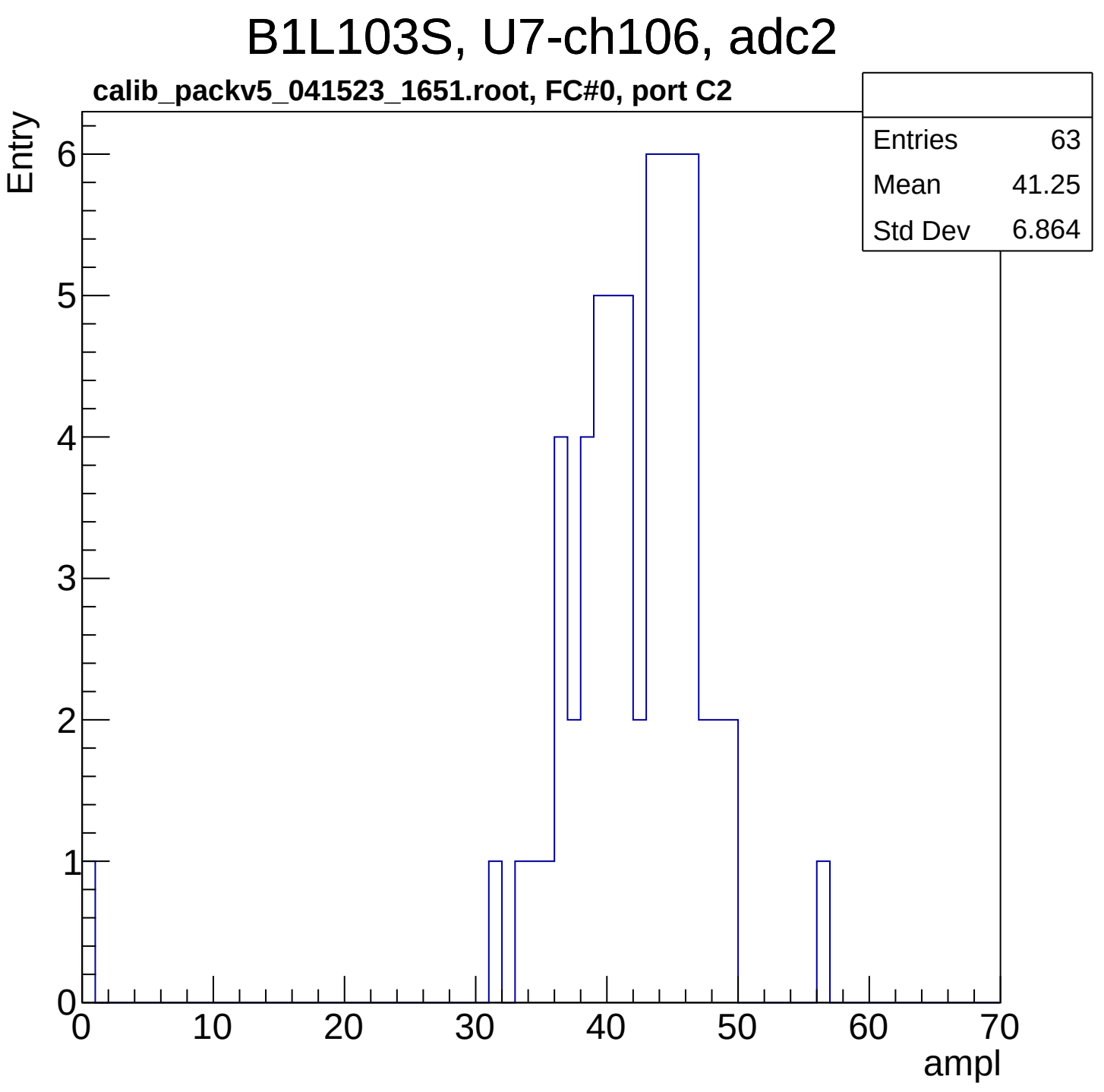
50
60
70
ampl


B1L103S, U7-ch106, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 41.25
Std Dev 6.864
Entry
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4
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6
0
10
20
30
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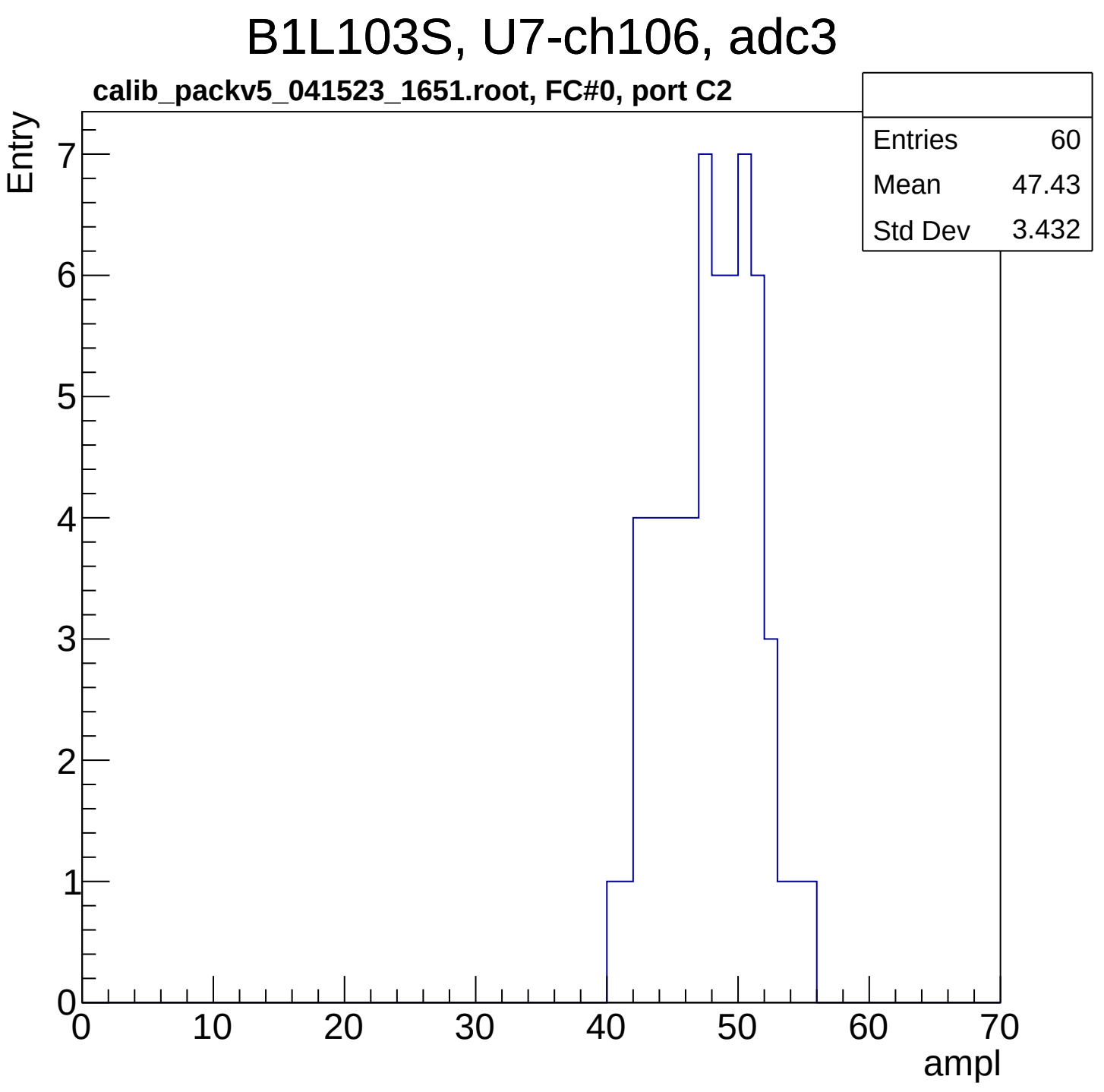
50
60
70
ampl


B1L103S, U7-ch106, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 47.43
Std Dev 3.432
Entry
ampl
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4
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0
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60
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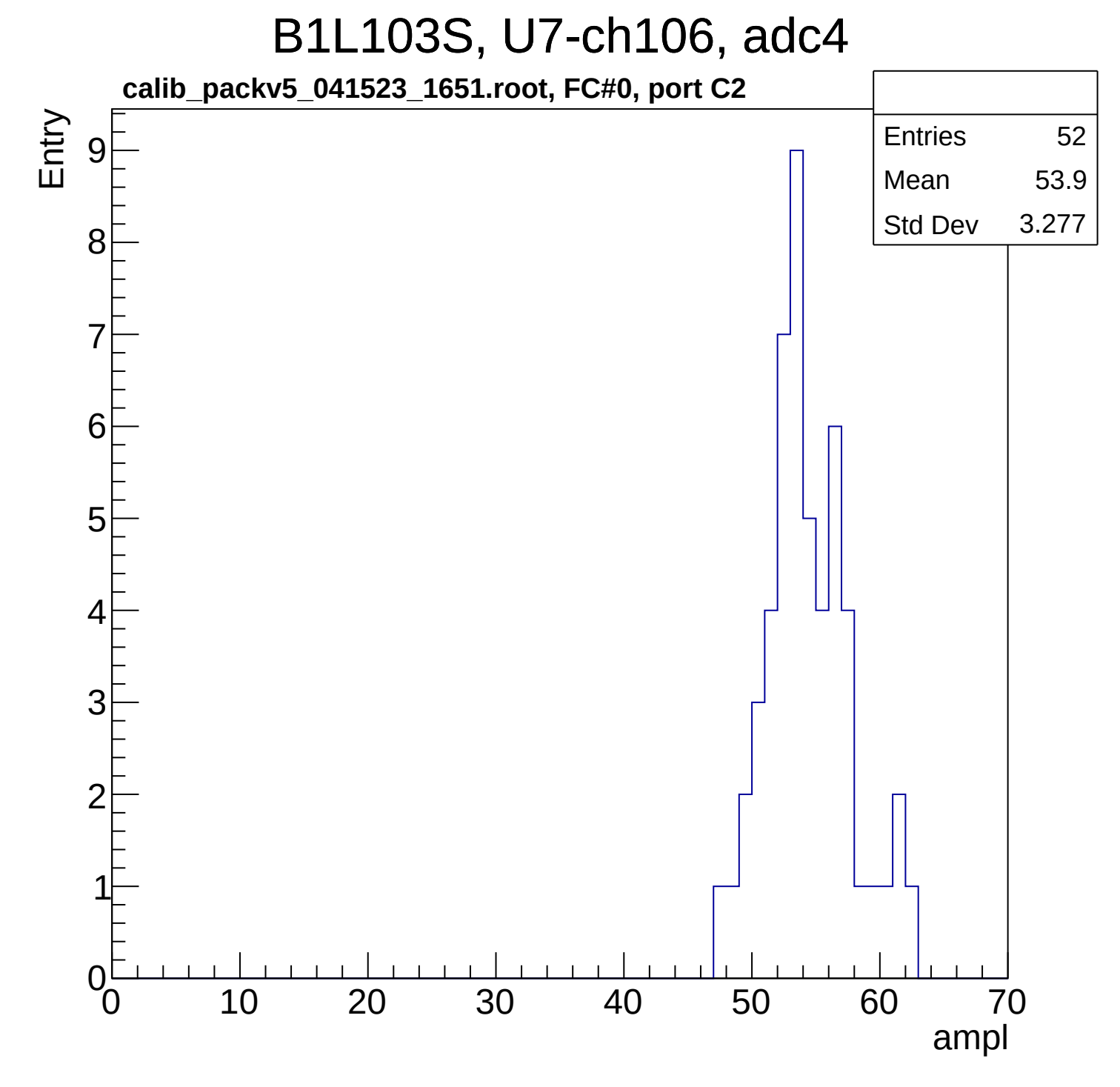
B1L103S, U7-ch106, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 53.9
Std Dev 3.277
Entry
ampl
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6
7
8
9
0
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60
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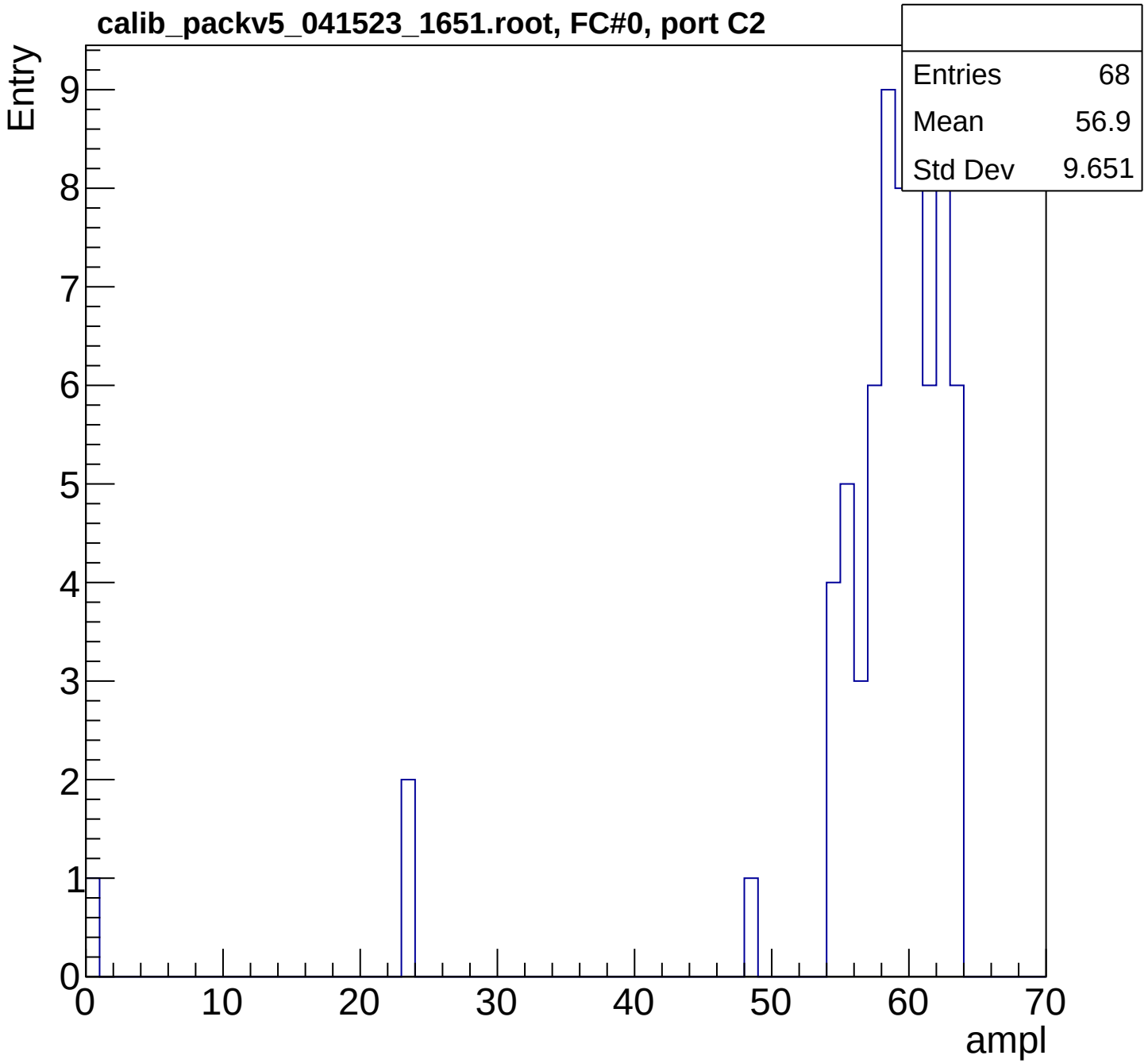
B1L103S, U7-ch106, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 56.9
Std Dev 9.651
Entry
ampl
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5
6
7
8
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0
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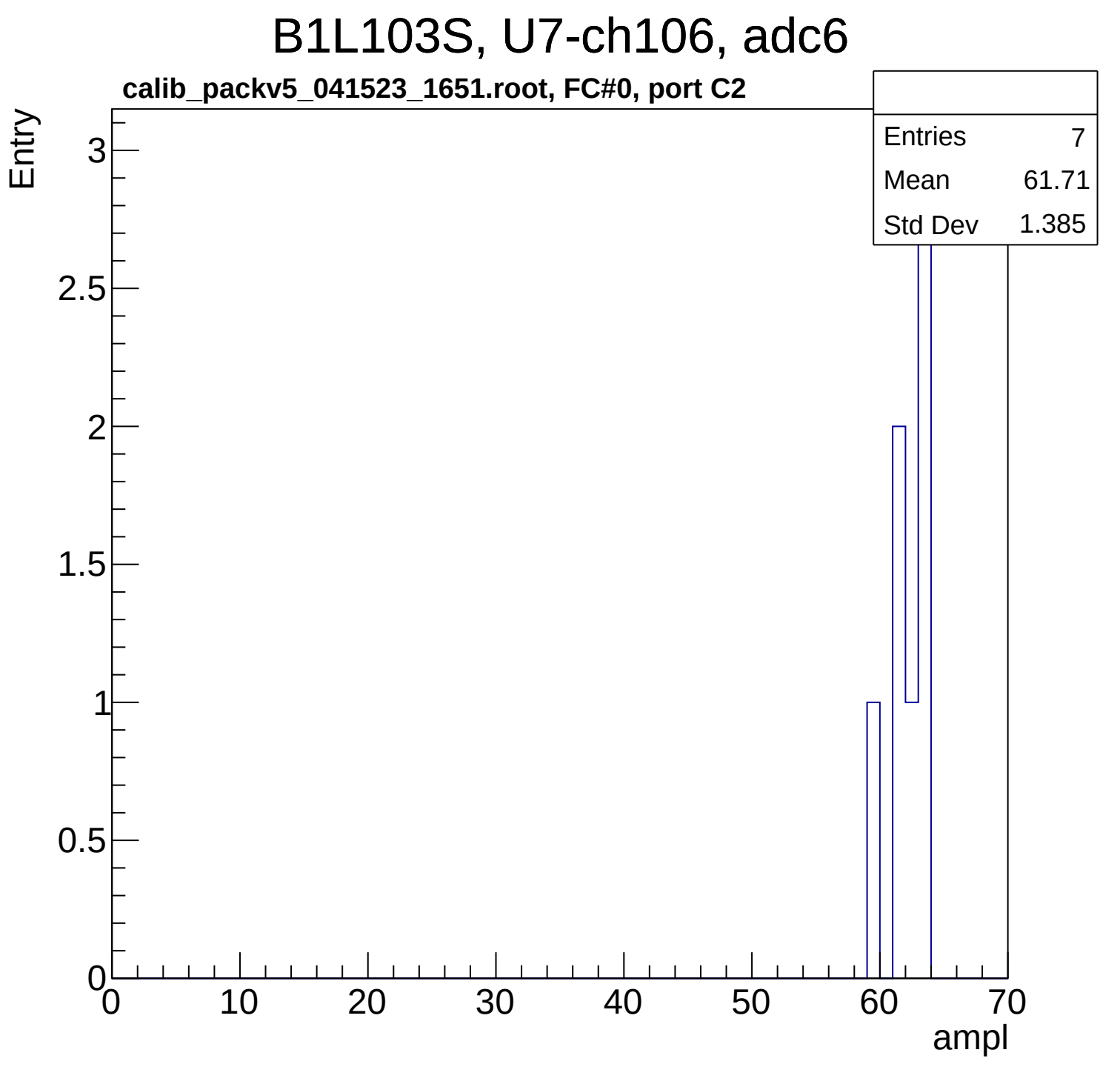
B1L103S, U7-ch106, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 61.71
Std Dev 1.385
Entry
ampl
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0.5
1
1.5
2
2.5
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0
10
20
30
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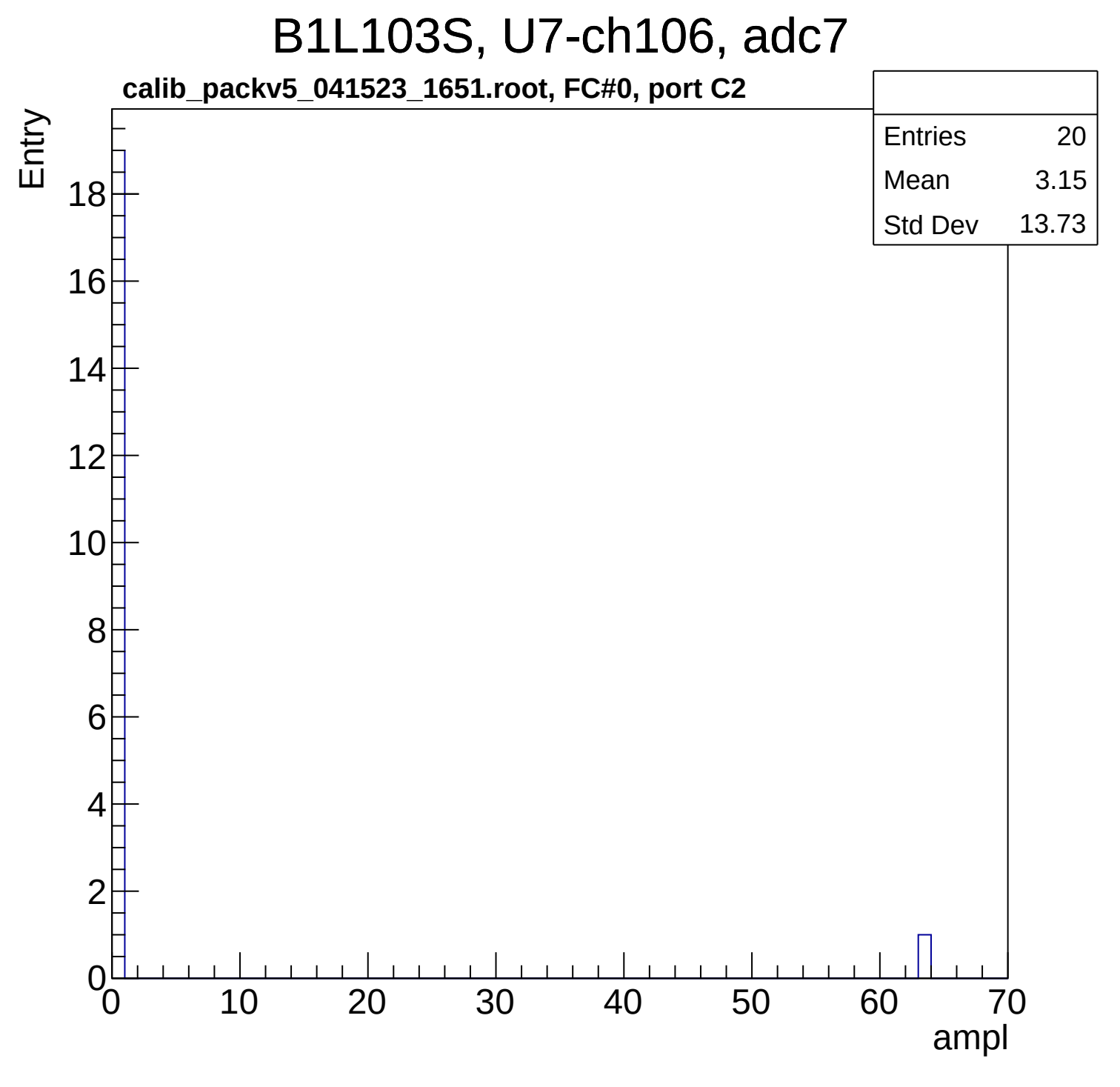
60
70


B1L103S, U7-ch106, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
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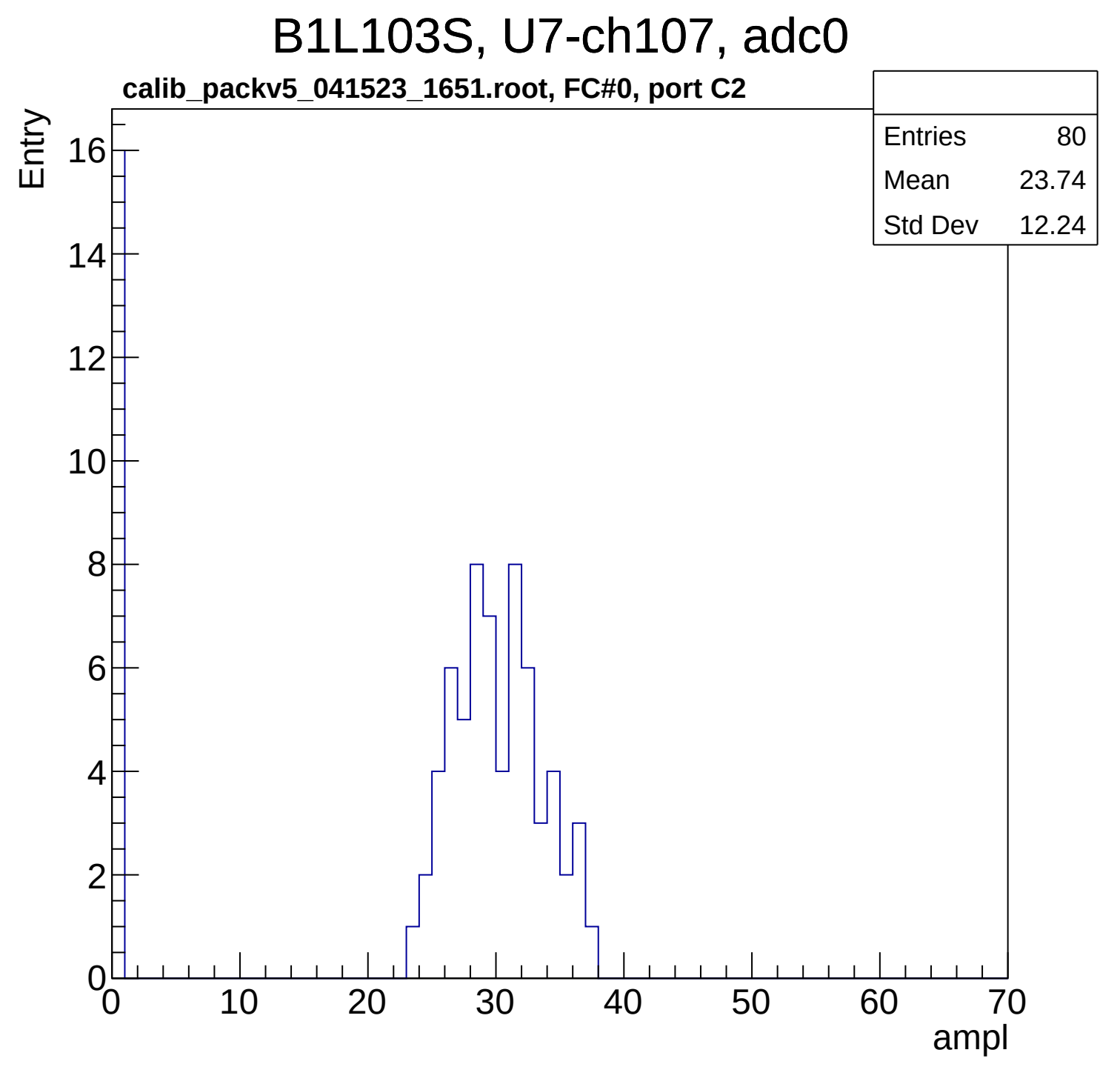
70
ampl


B1L103S, U7-ch107, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 23.74
Std Dev 12.24
Entry
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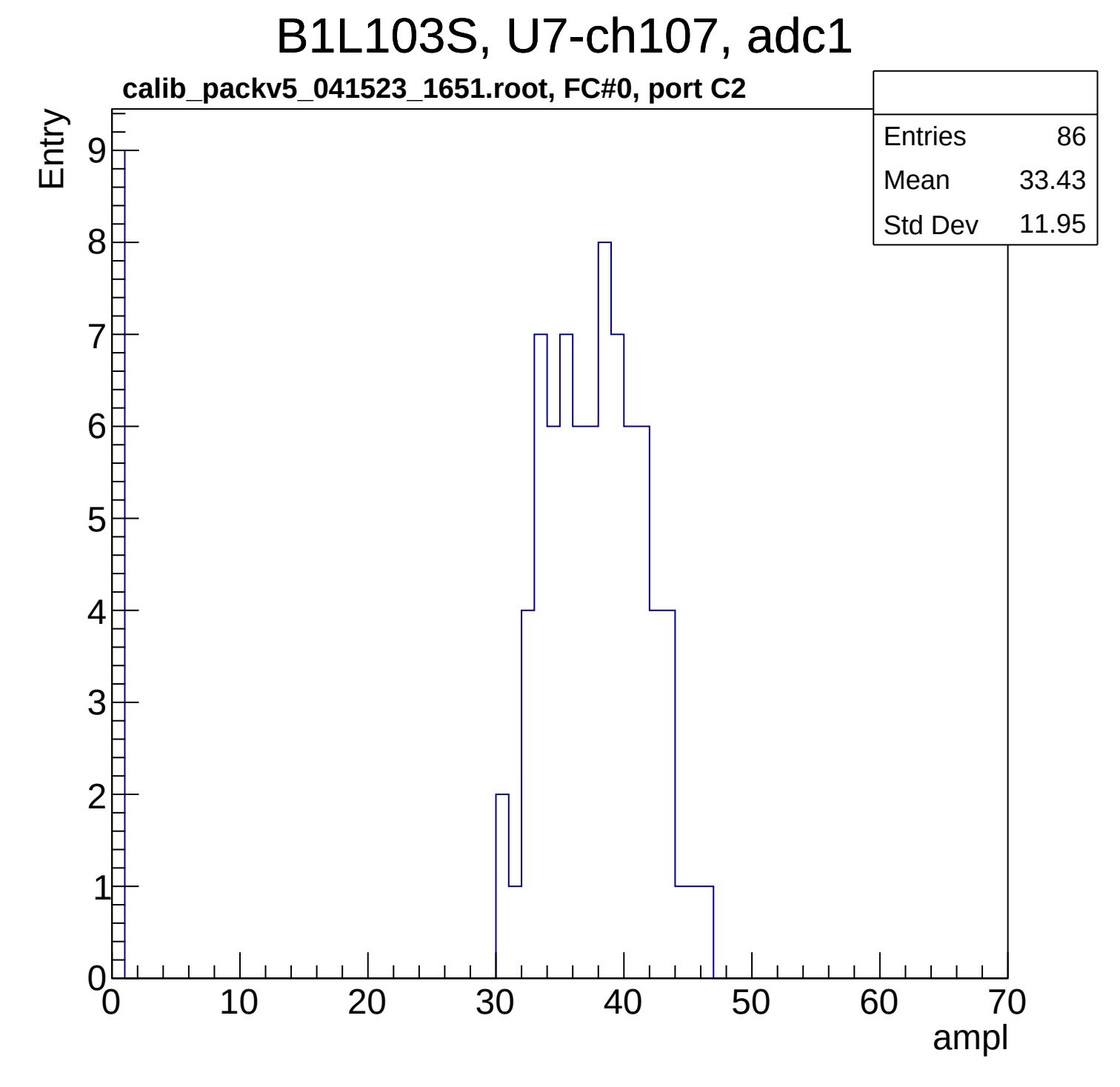
70
ampl


B1L103S, U7-ch107, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 33.43
Std Dev 11.95
Entry
ampl
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0
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40
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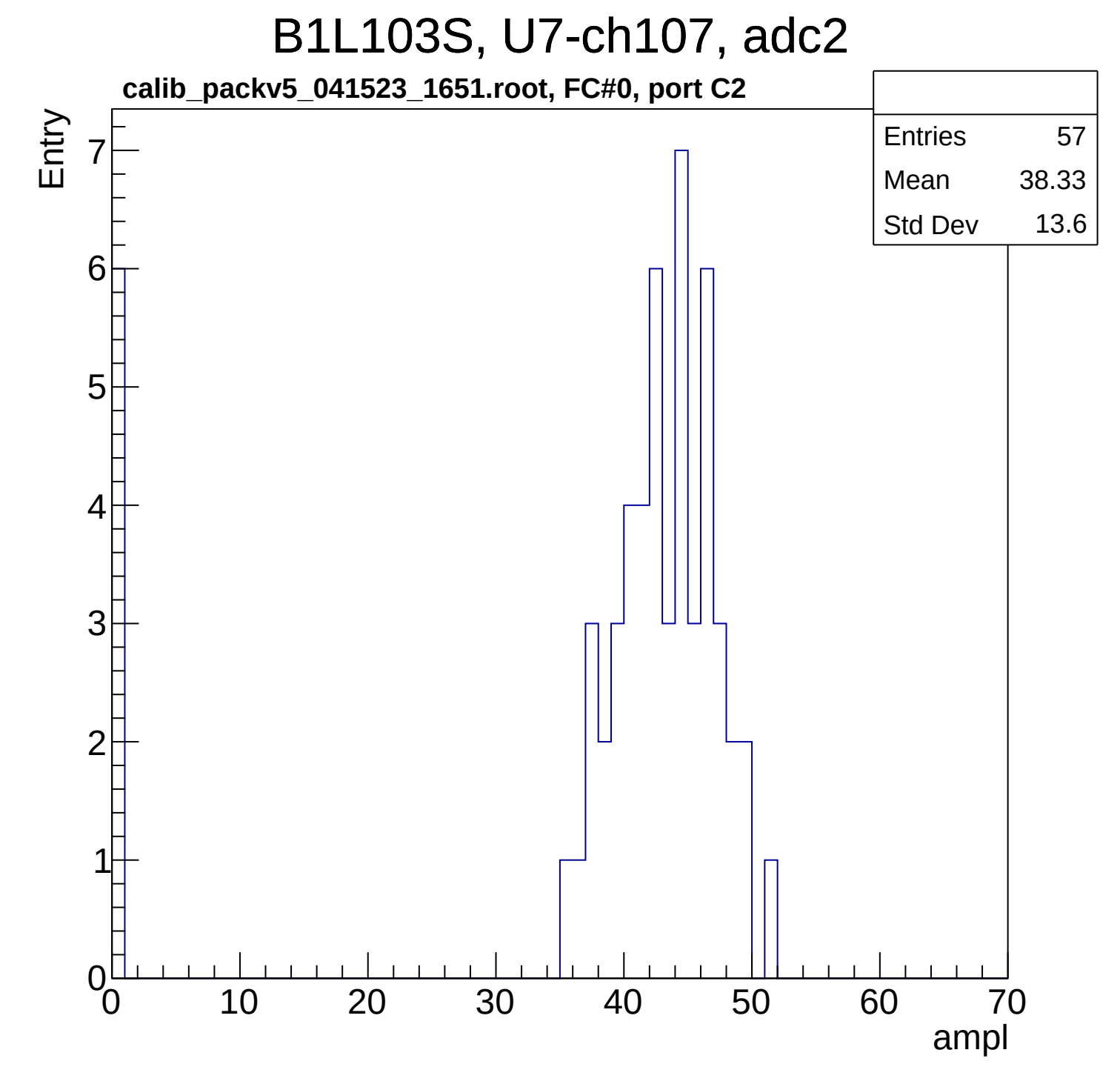
B1L103S, U7-ch107, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 38.33
Std Dev 13.6
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
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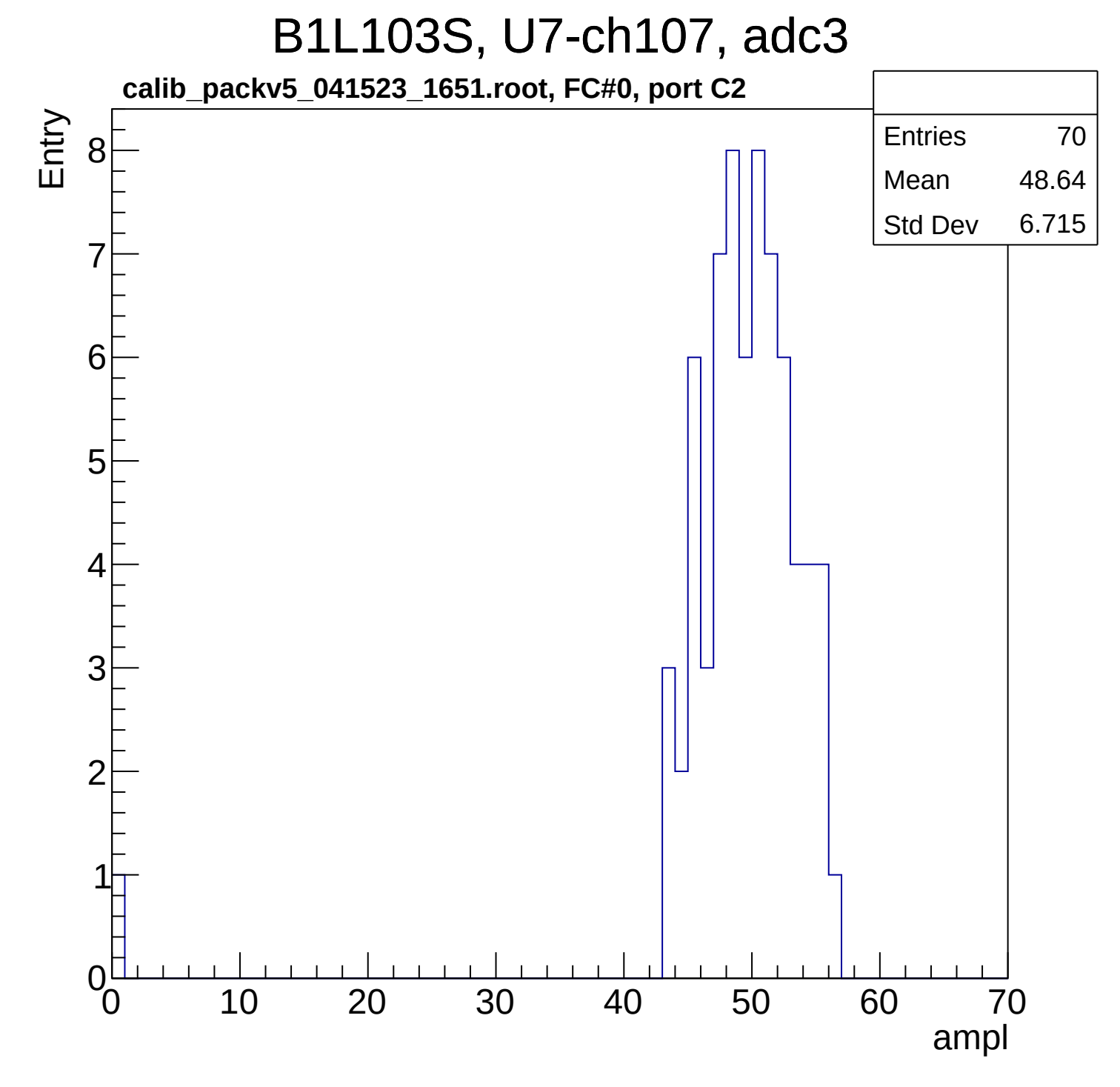
40
50
60
70


B1L103S, U7-ch107, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 48.64
Std Dev 6.715
Entry
ampl
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3
4
5
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7
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0
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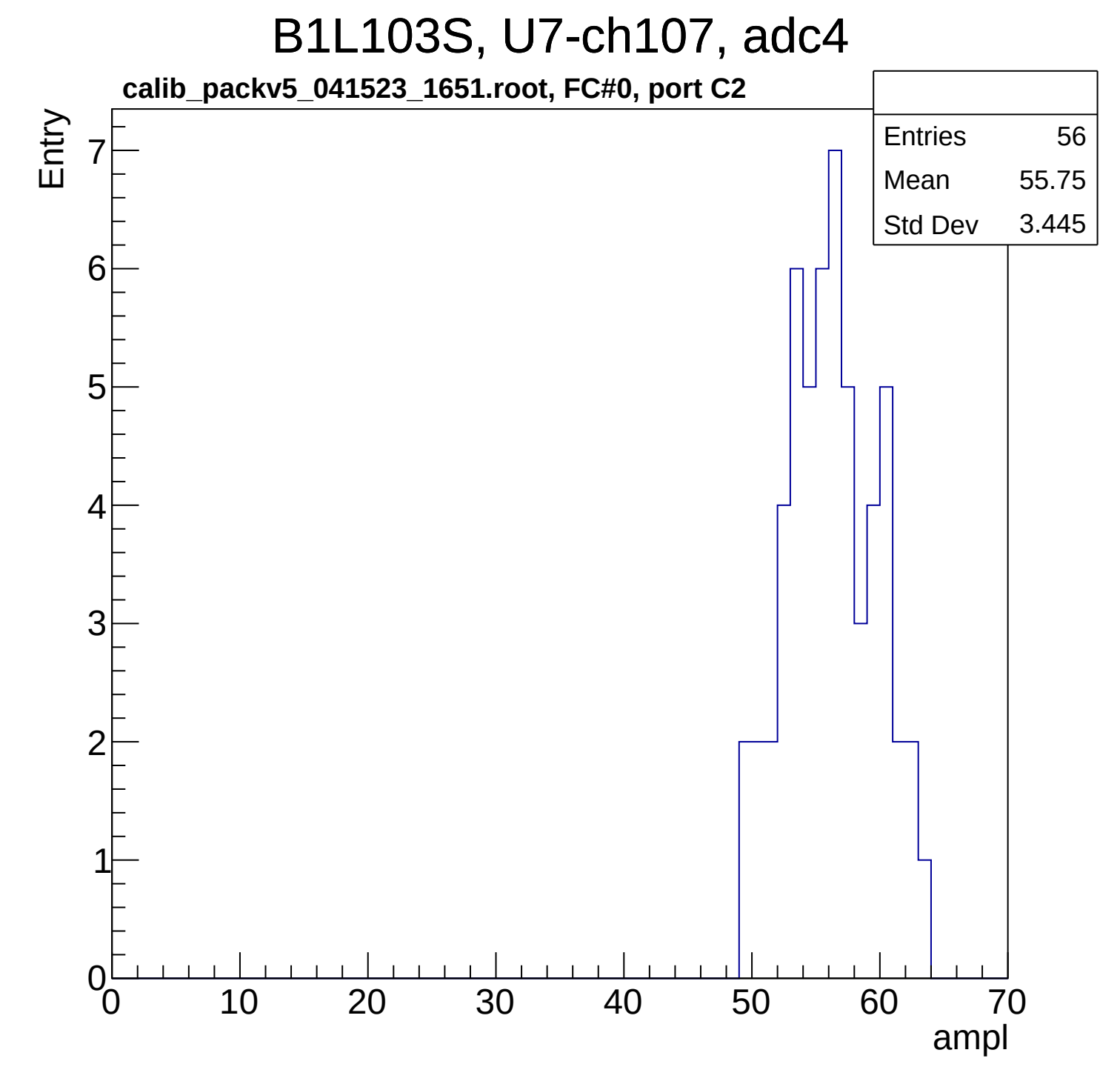
B1L103S, U7-ch107, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 55.75
Std Dev 3.445
Entry
ampl
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0
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20
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40
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60
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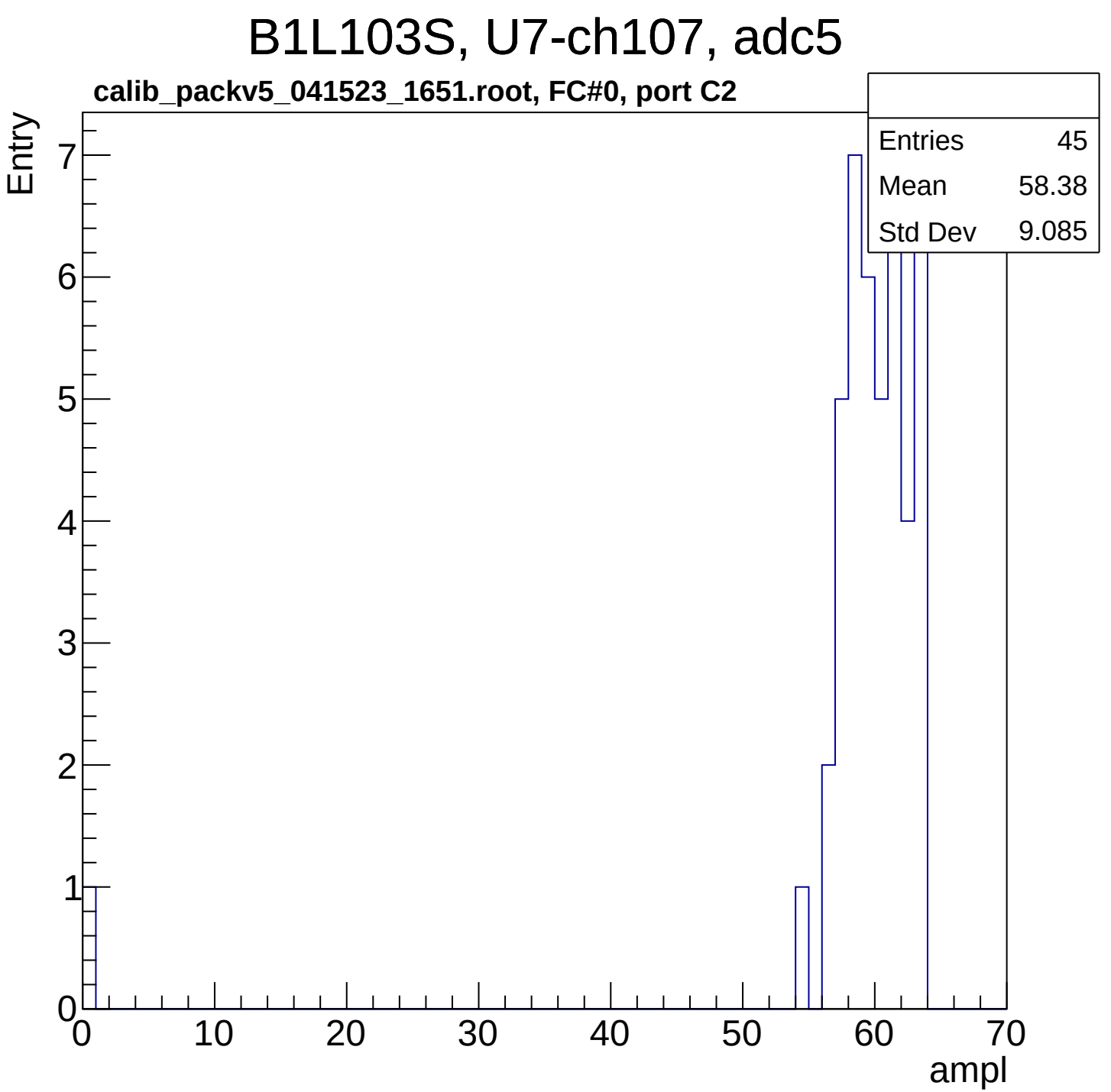
B1L103S, U7-ch107, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 58.38
Std Dev 9.085
Entry
ampl
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1
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3
4
5
6
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0
10
20
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40
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60
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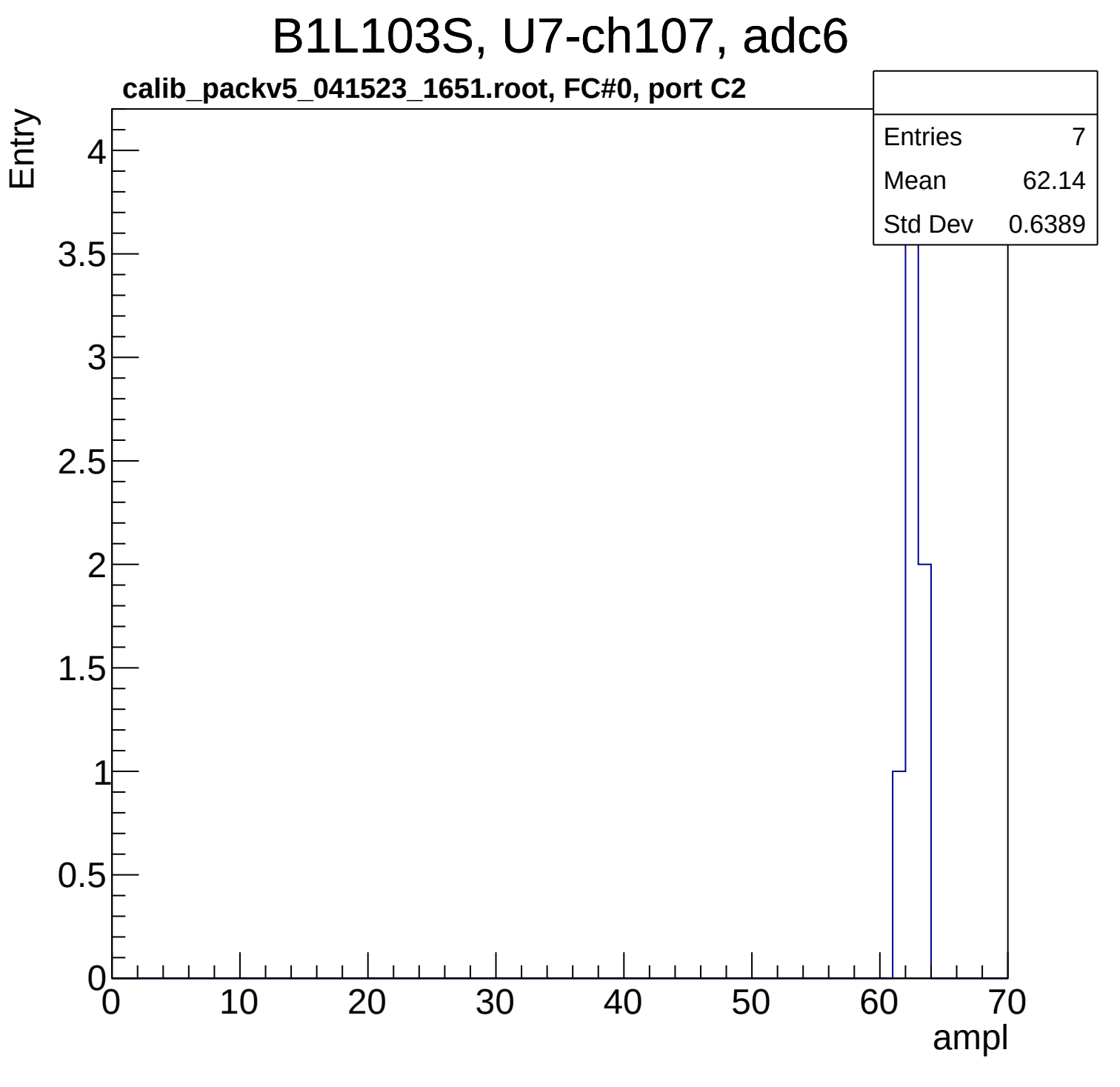
B1L103S, U7-ch107, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 62.14
Std Dev 0.6389
Entry
ampl
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0.5
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1.5
2
2.5
3
3.5
4
0
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20
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40
50
60
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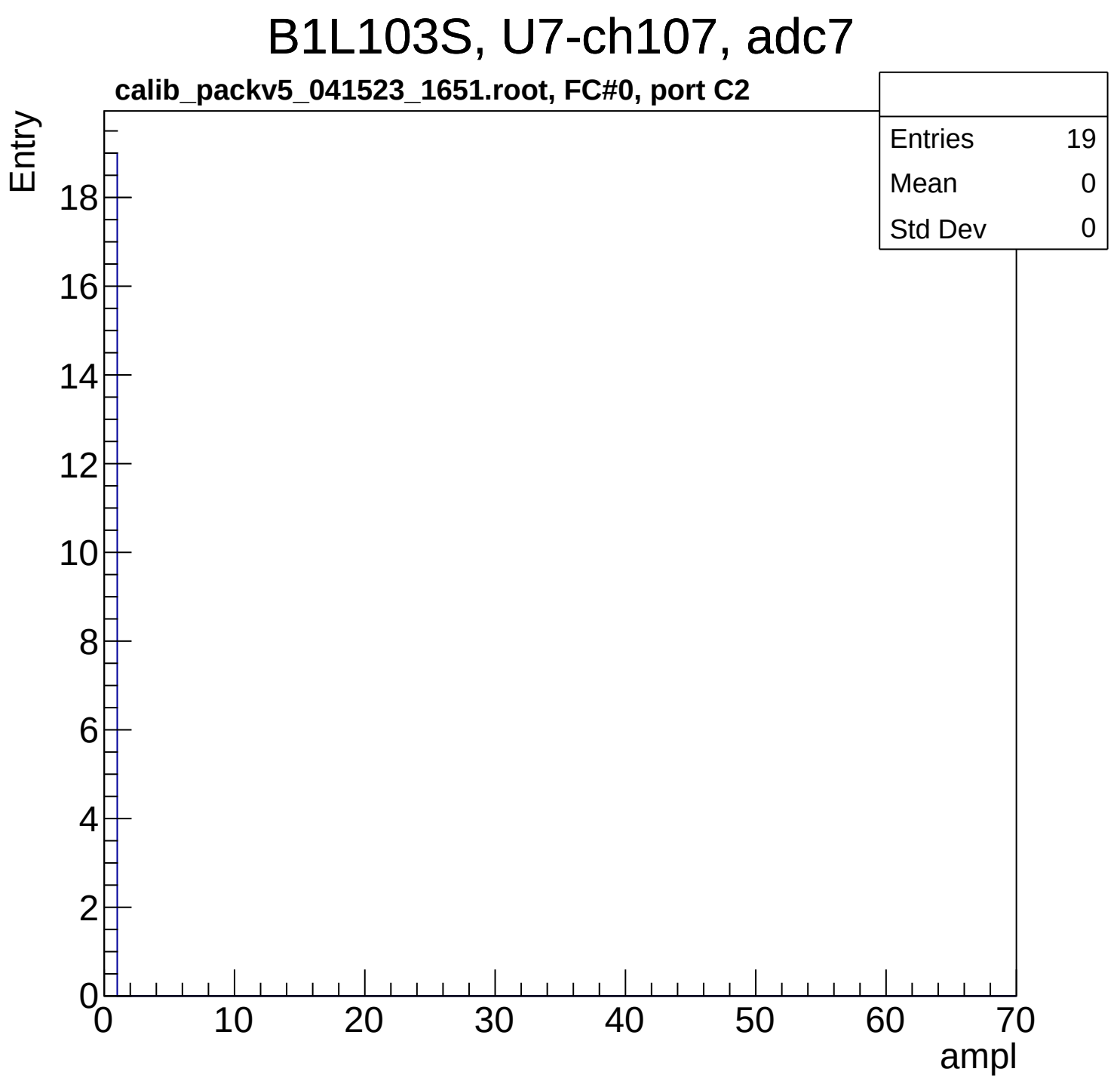
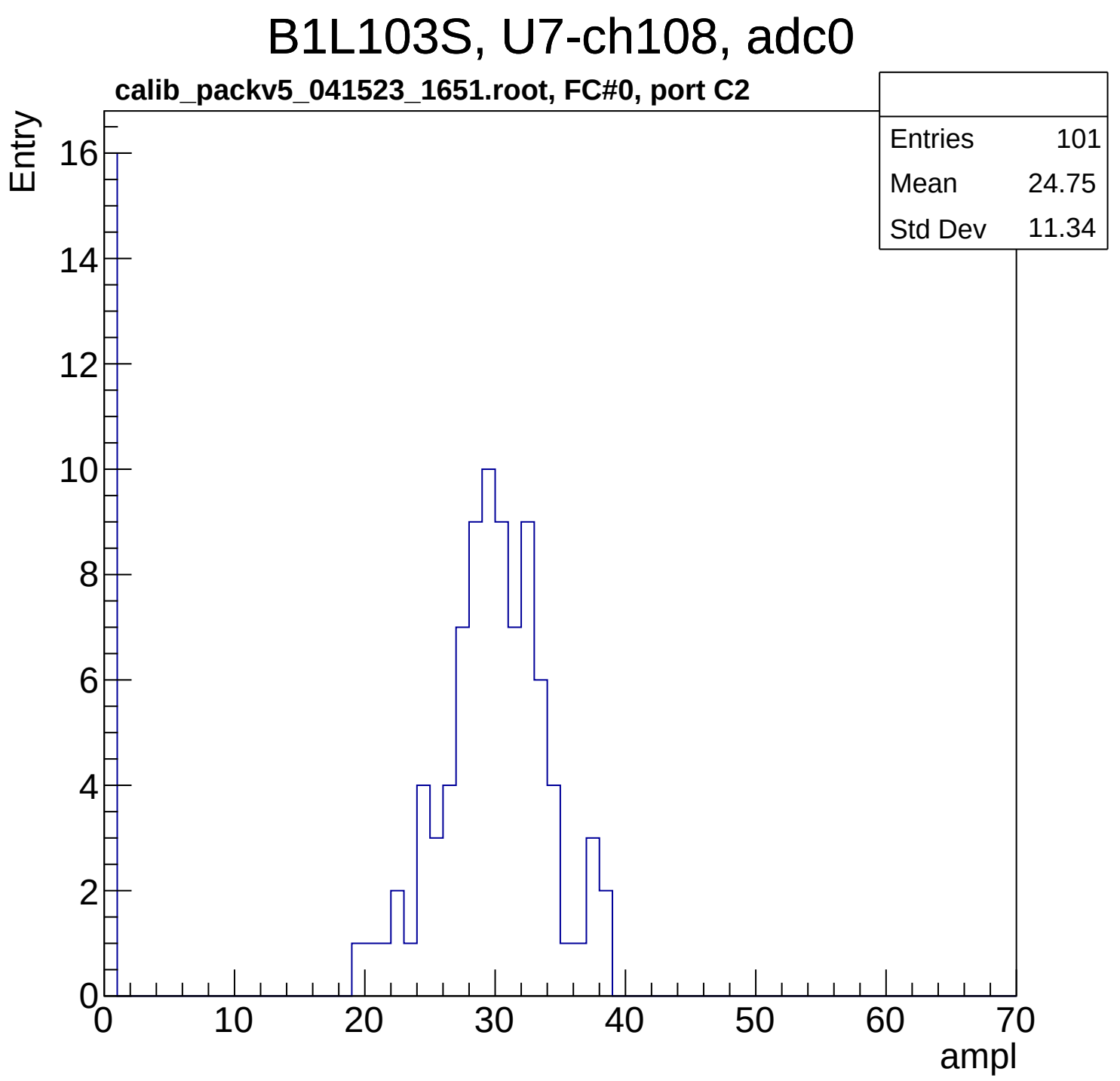

B1L103S, U7-ch107, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch108, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 101
Mean 24.75
Std Dev 11.34
Entry
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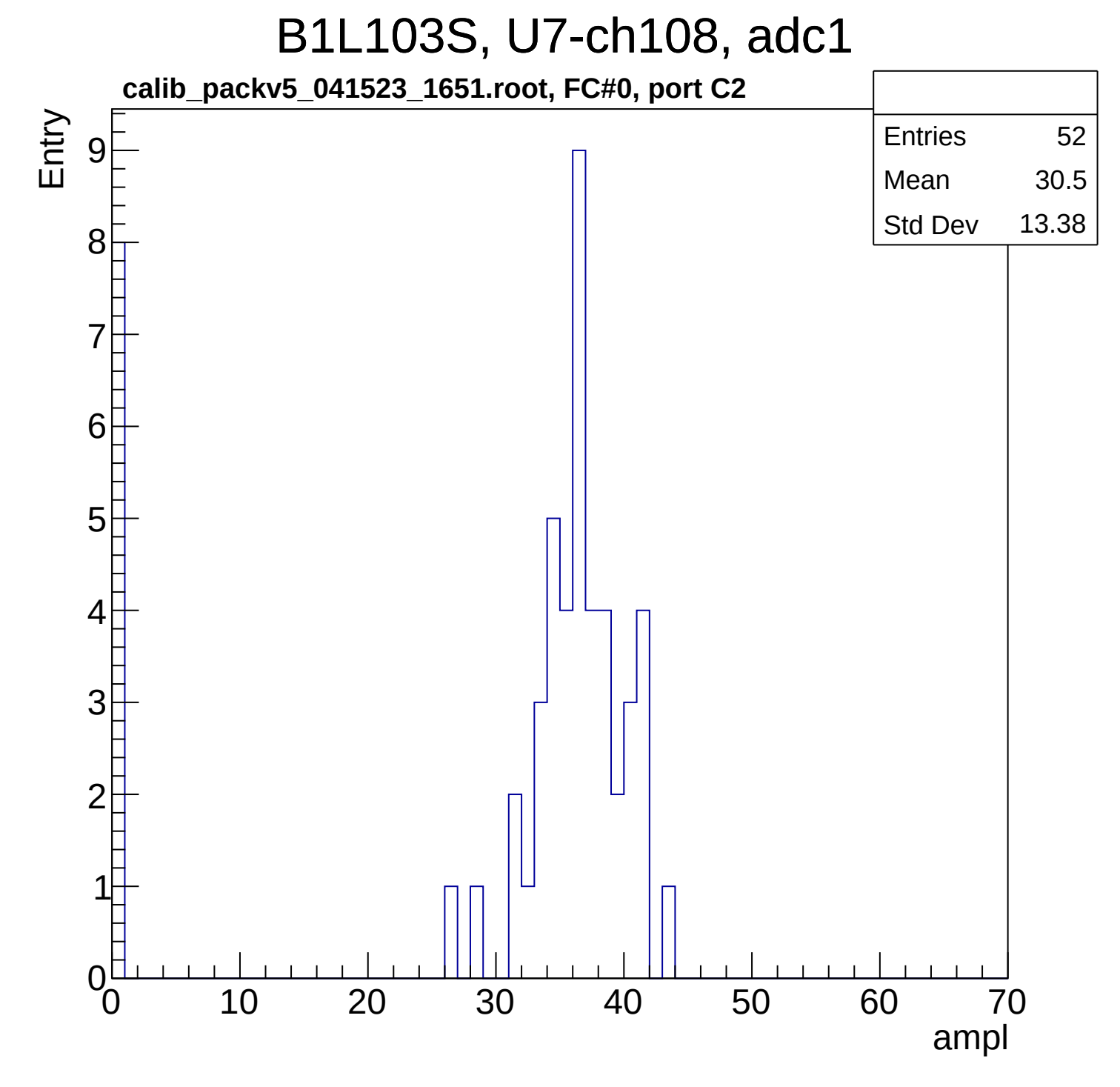
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch108, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 30.5
Std Dev 13.38
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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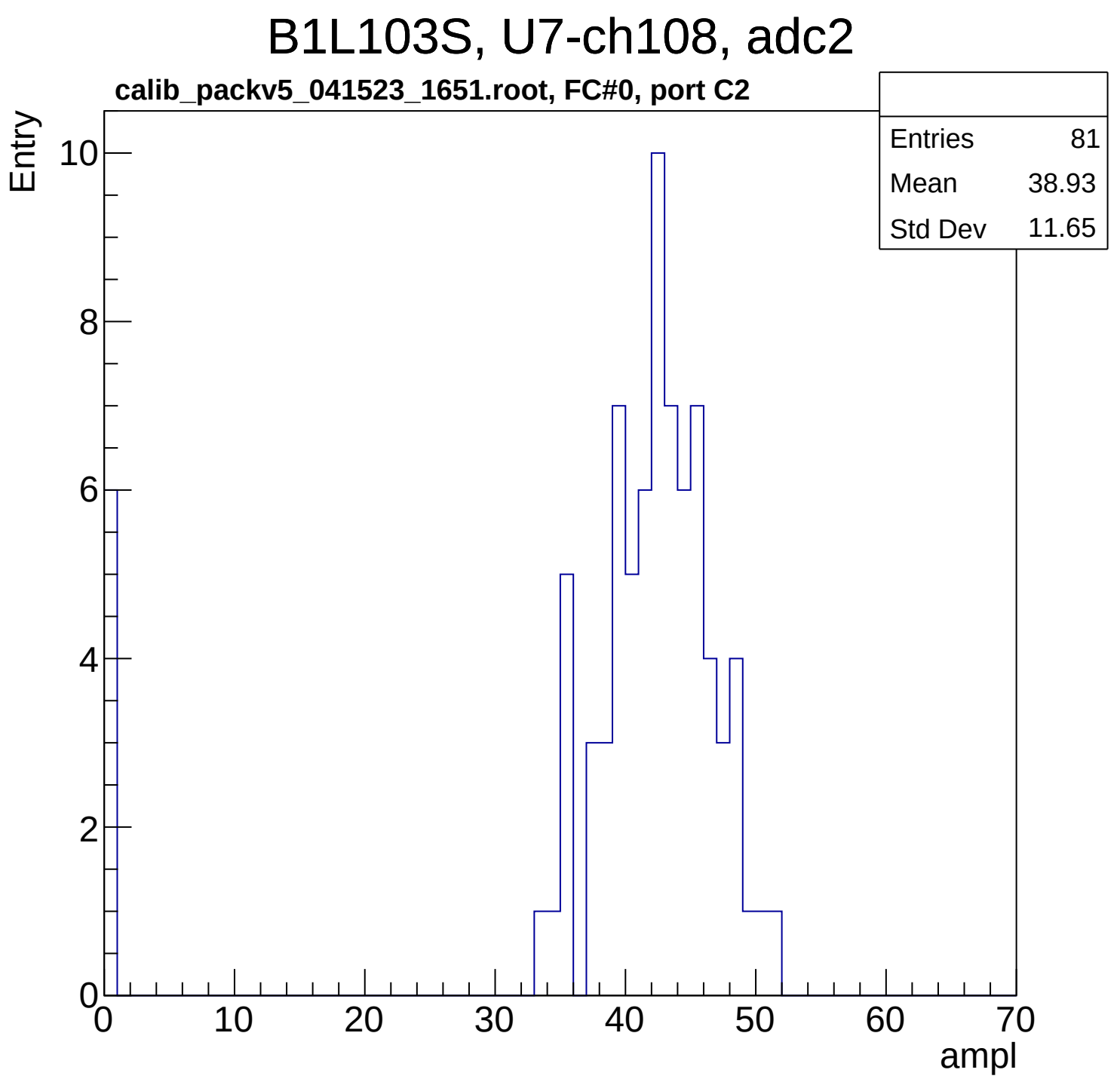
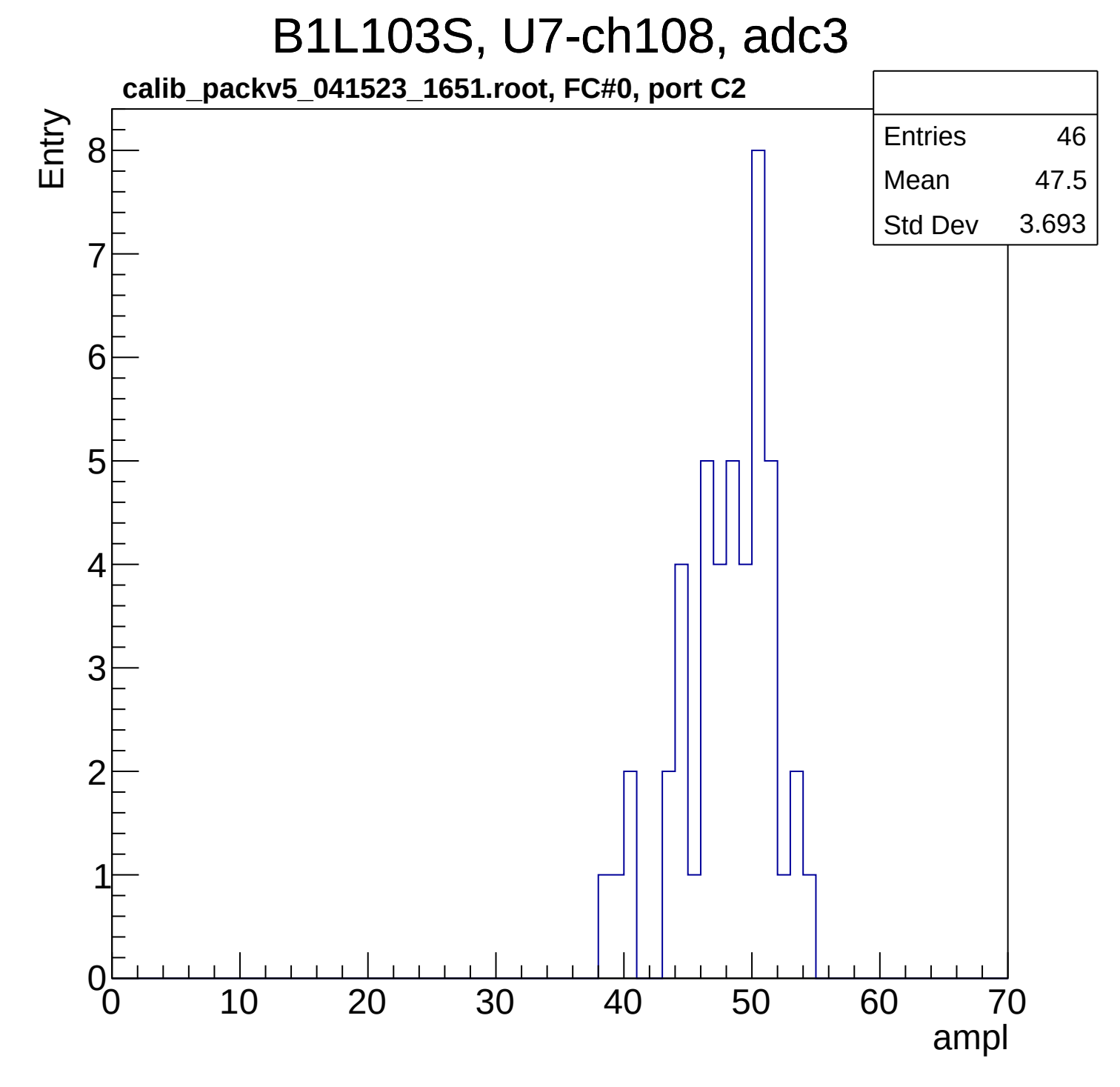

B1L103S, U7-ch108, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 38.93
Std Dev 11.65
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U7-ch108, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 47.5
Std Dev 3.693
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
30
40
50
60
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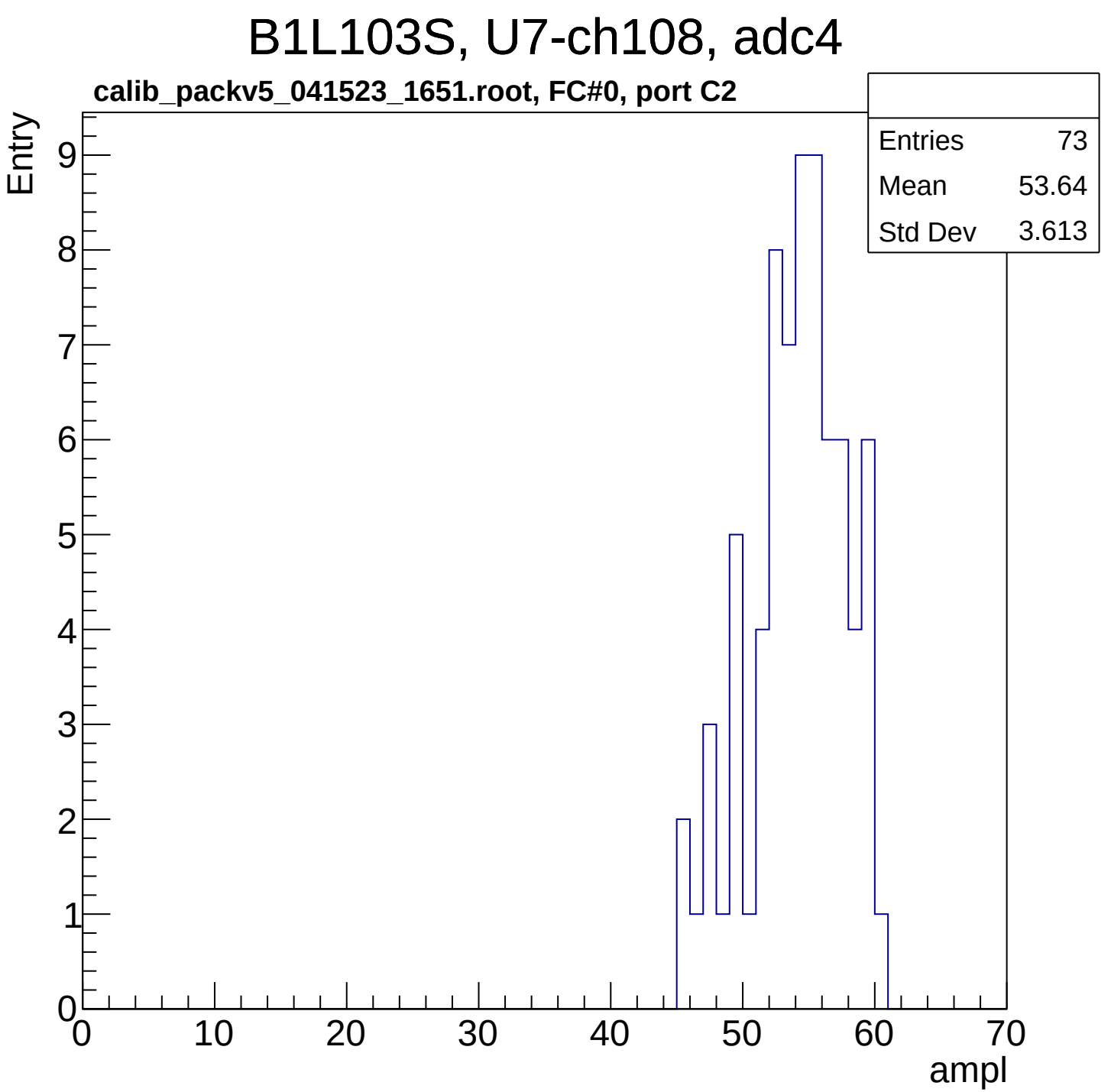
B1L103S, U7-ch108, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 53.64
Std Dev 3.613
Entry
ampl
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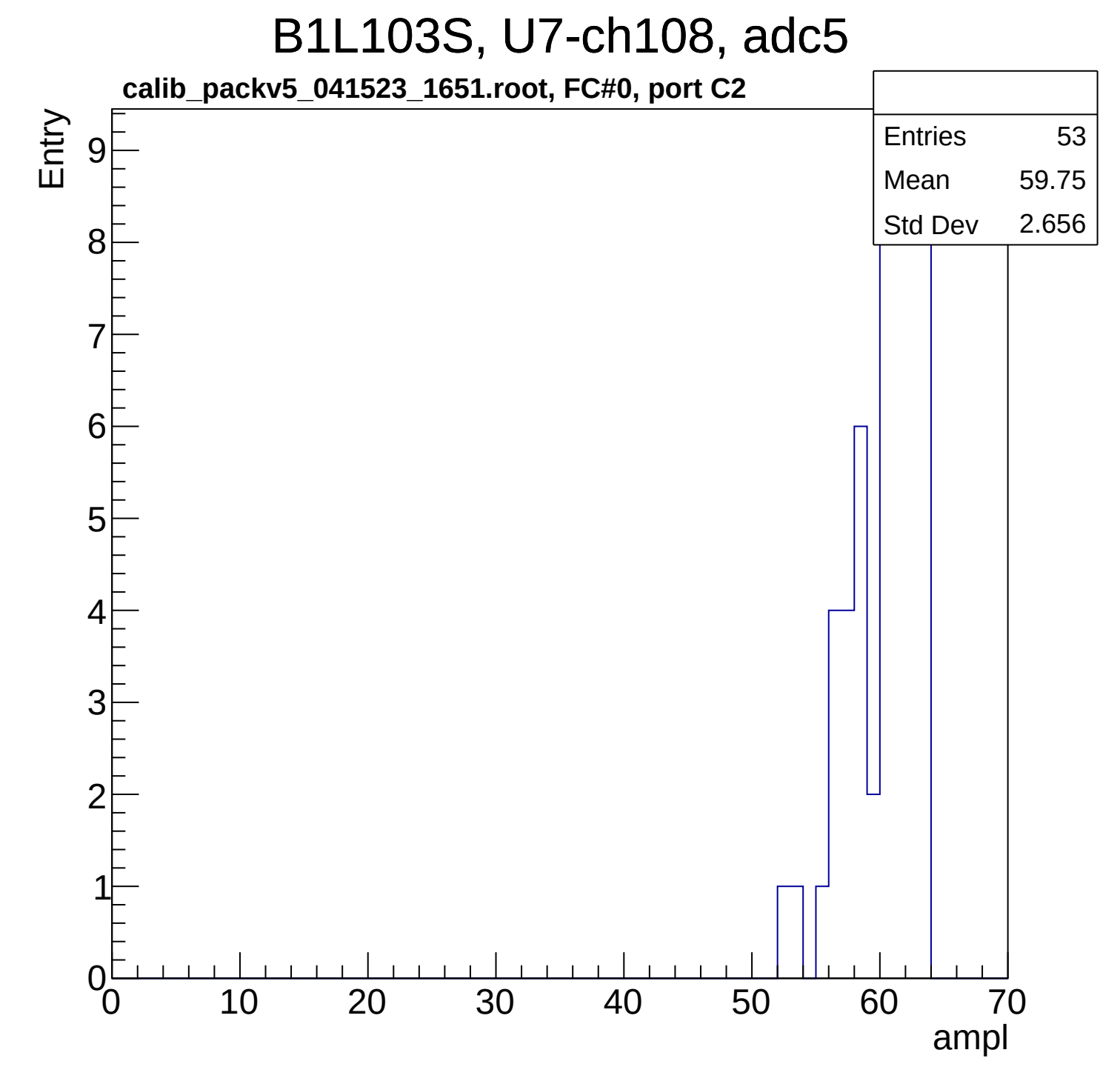
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U7-ch108, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 59.75
Std Dev 2.656
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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40
50
60
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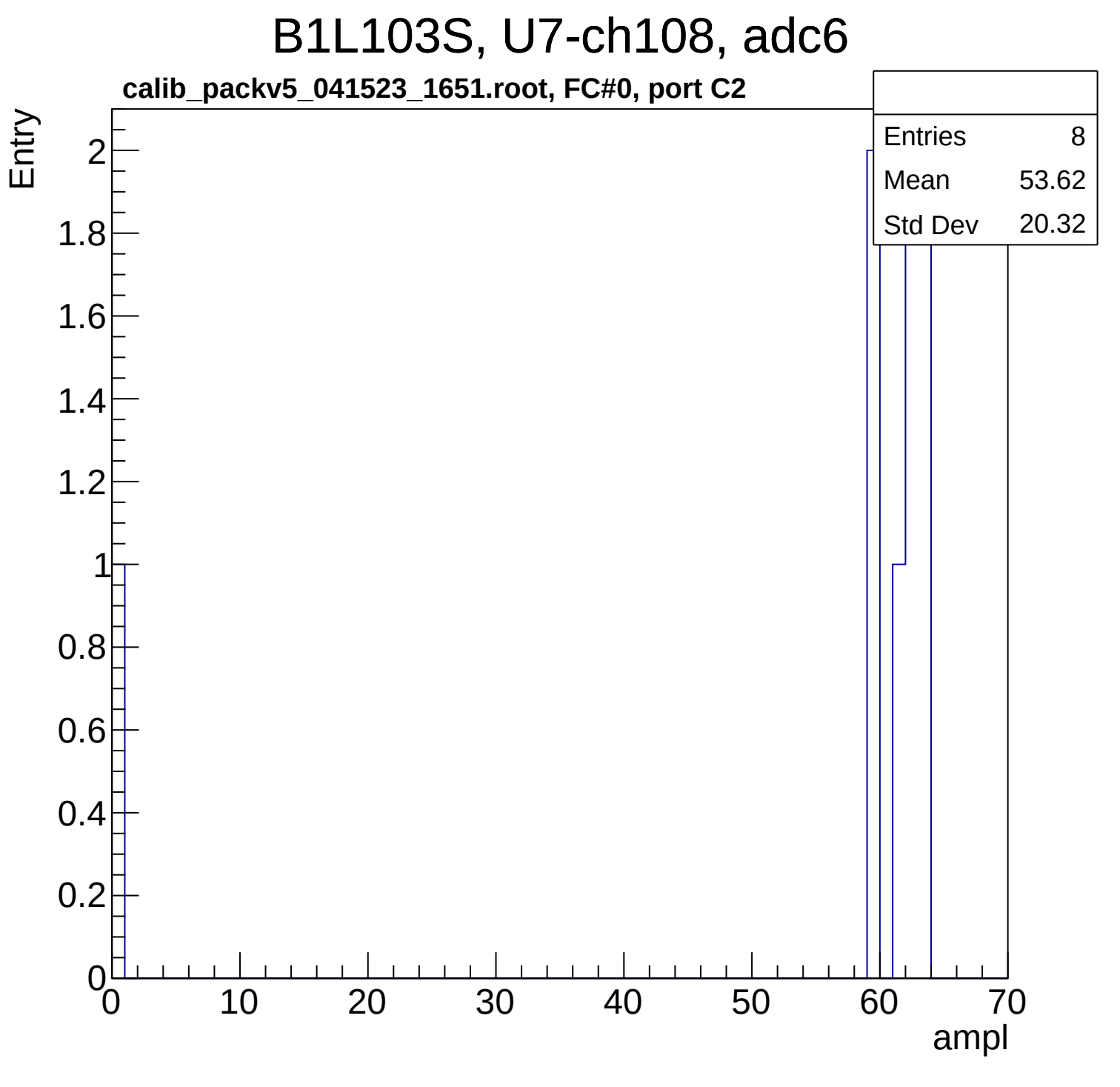
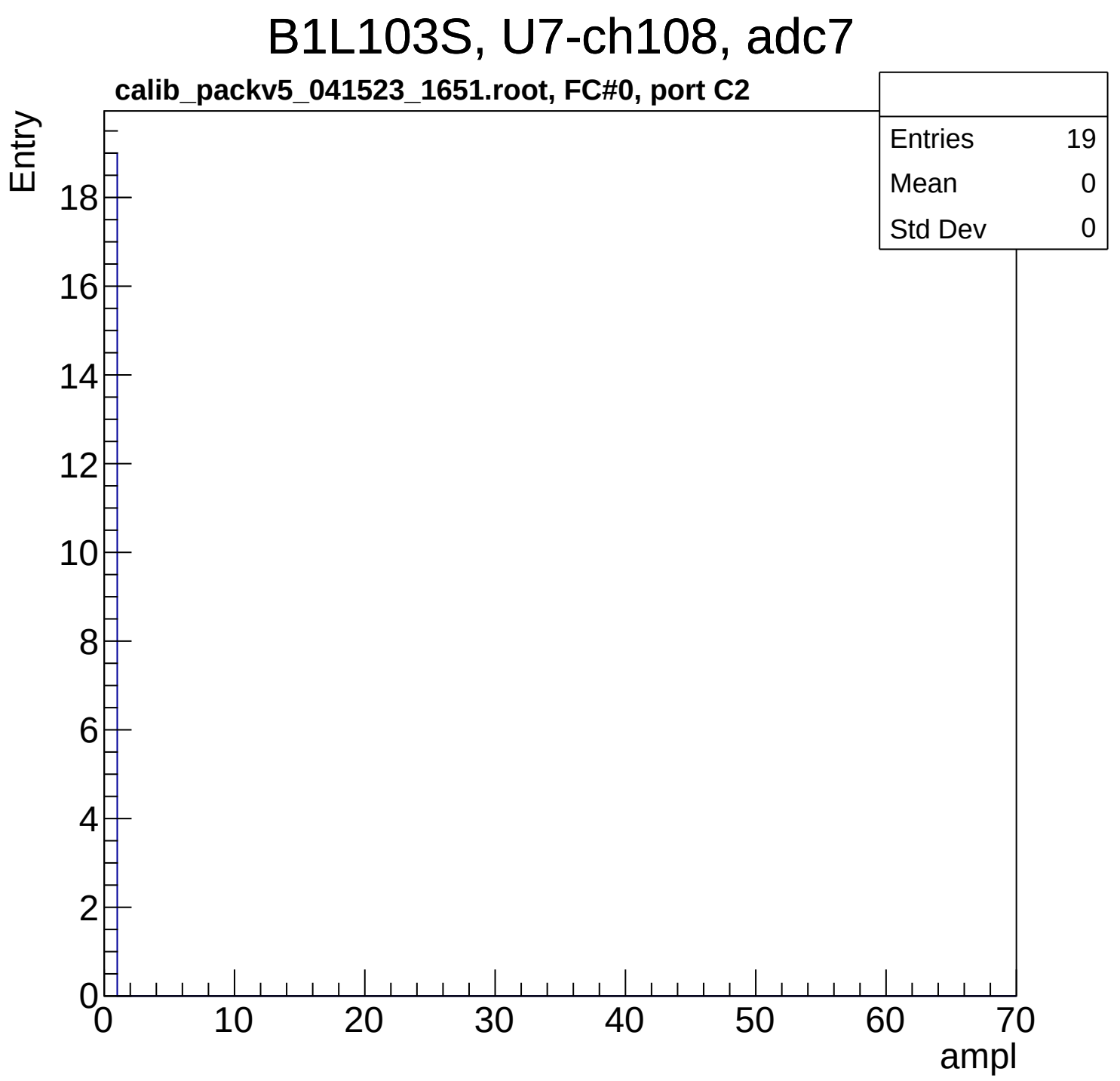
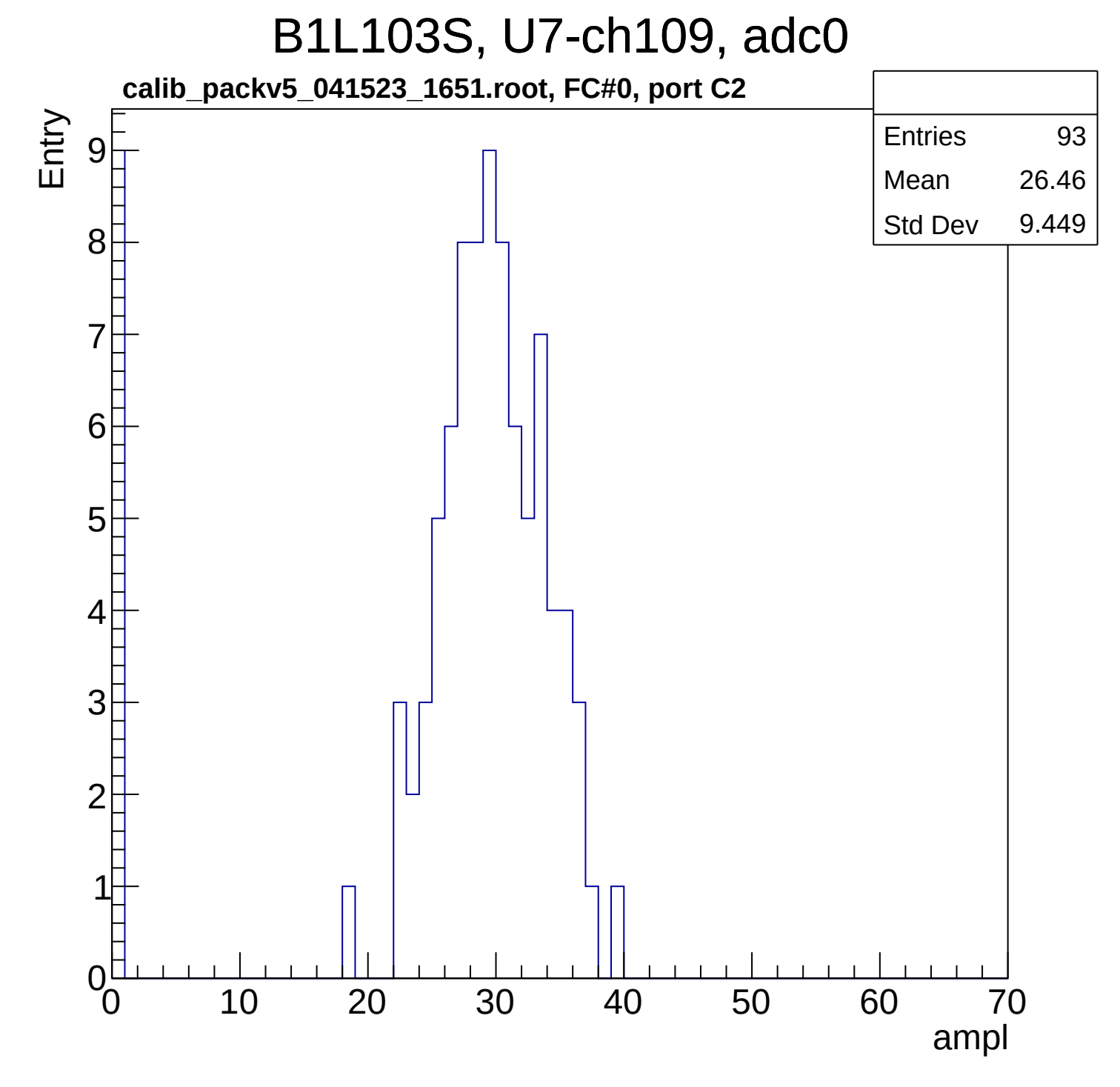

B1L103S, U7-ch108, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 53.62
Std Dev 20.32
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U7-ch108, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch109, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 93
Mean 26.46
Std Dev 9.449
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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60
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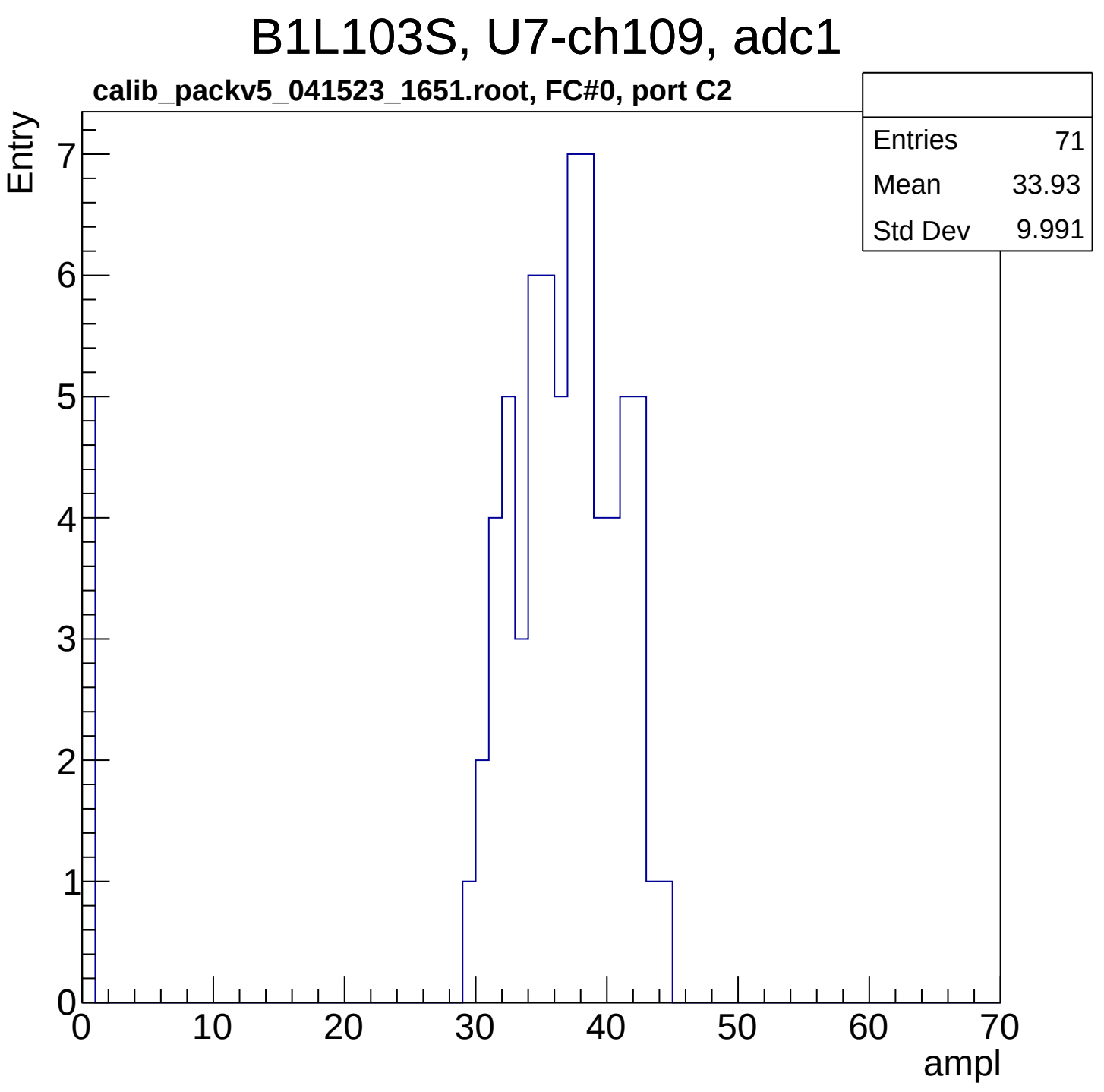
B1L103S, U7-ch109, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 33.93
Std Dev 9.991
Entry
ampl
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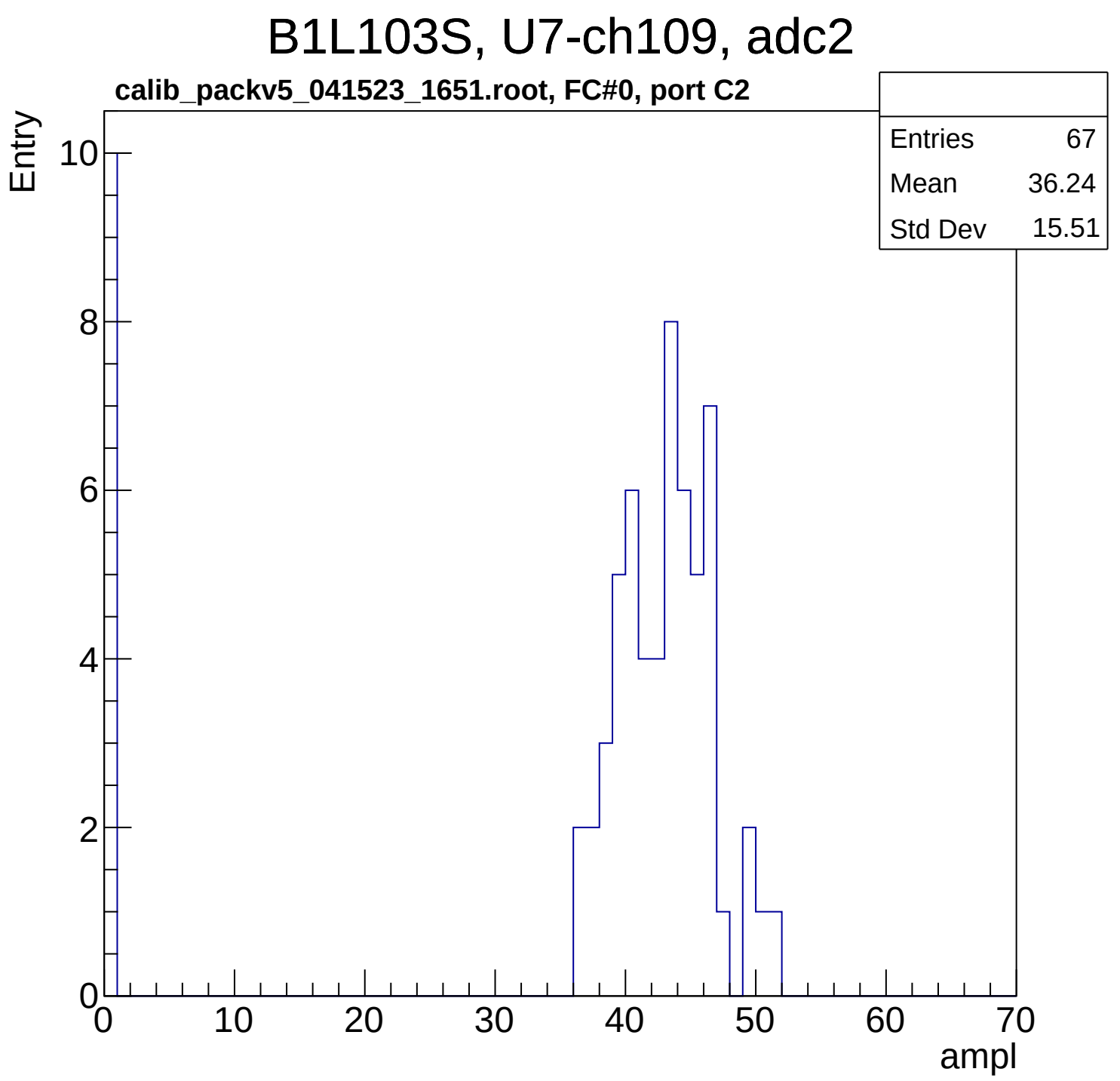
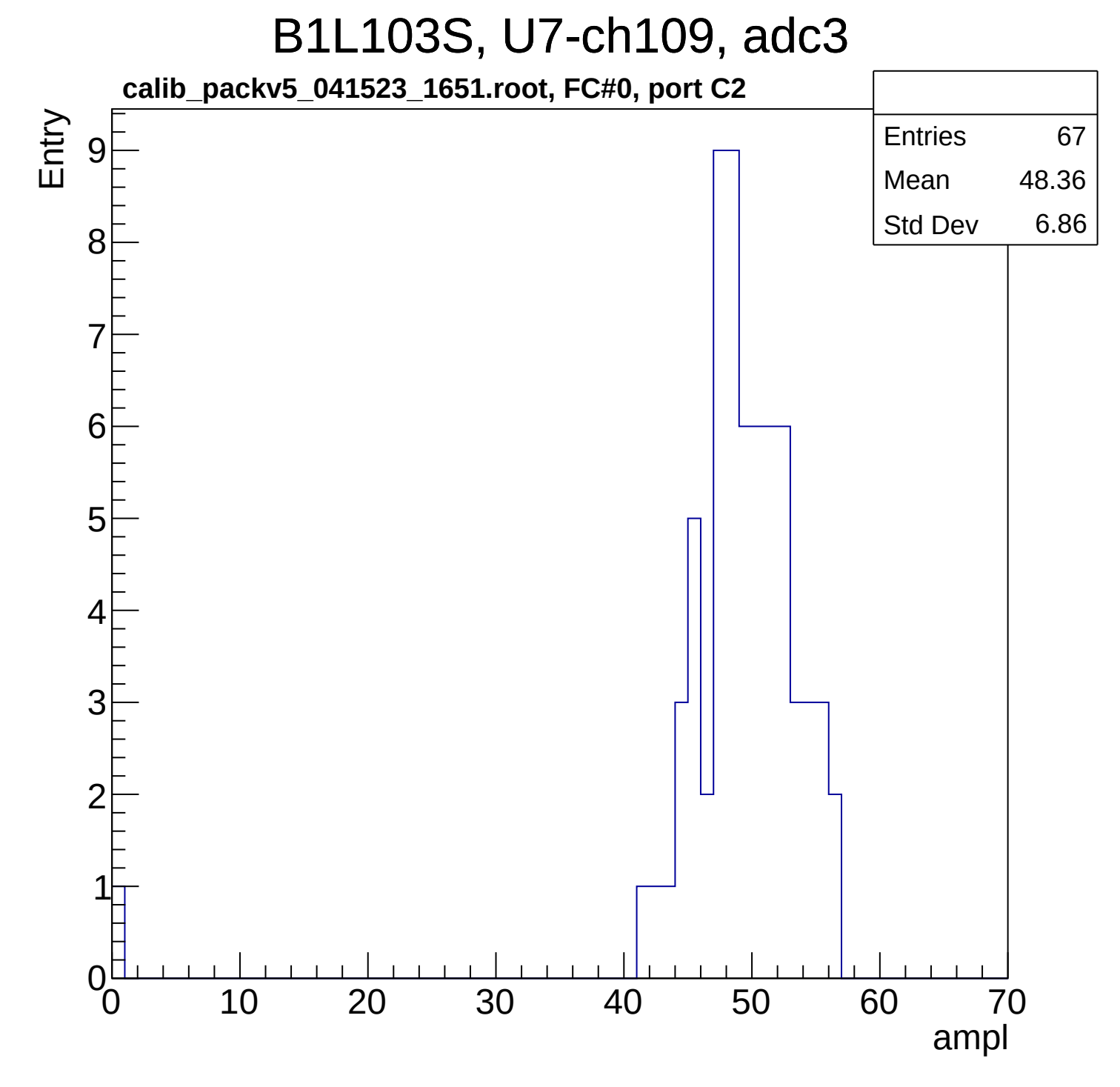
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U7-ch109, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 36.24
Std Dev 15.51
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch109, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 48.36
Std Dev 6.86
Entry
ampl
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3
4
5
6
7
8
9
0
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60
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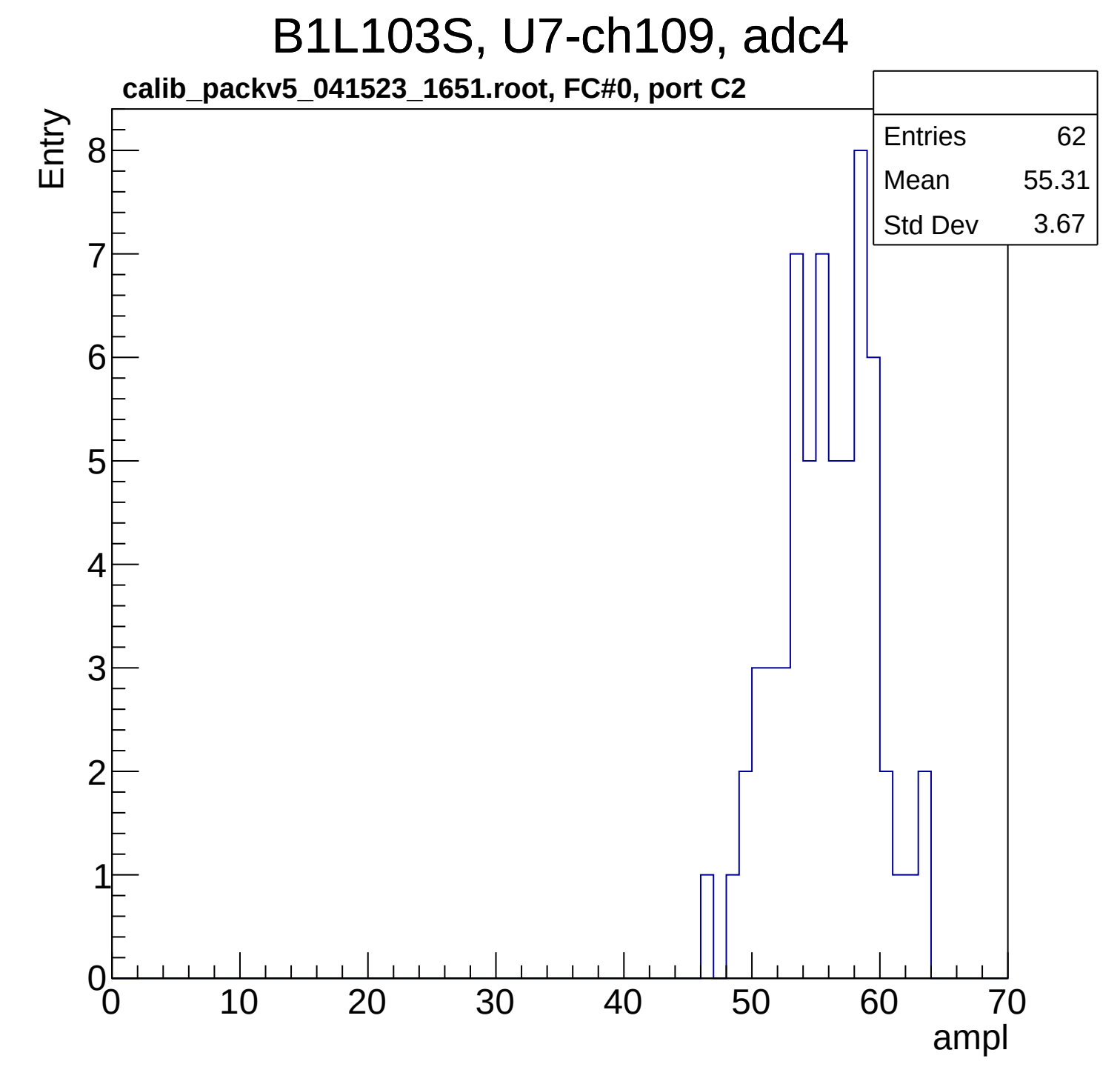
B1L103S, U7-ch109, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 55.31
Std Dev 3.67
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
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40
50
60
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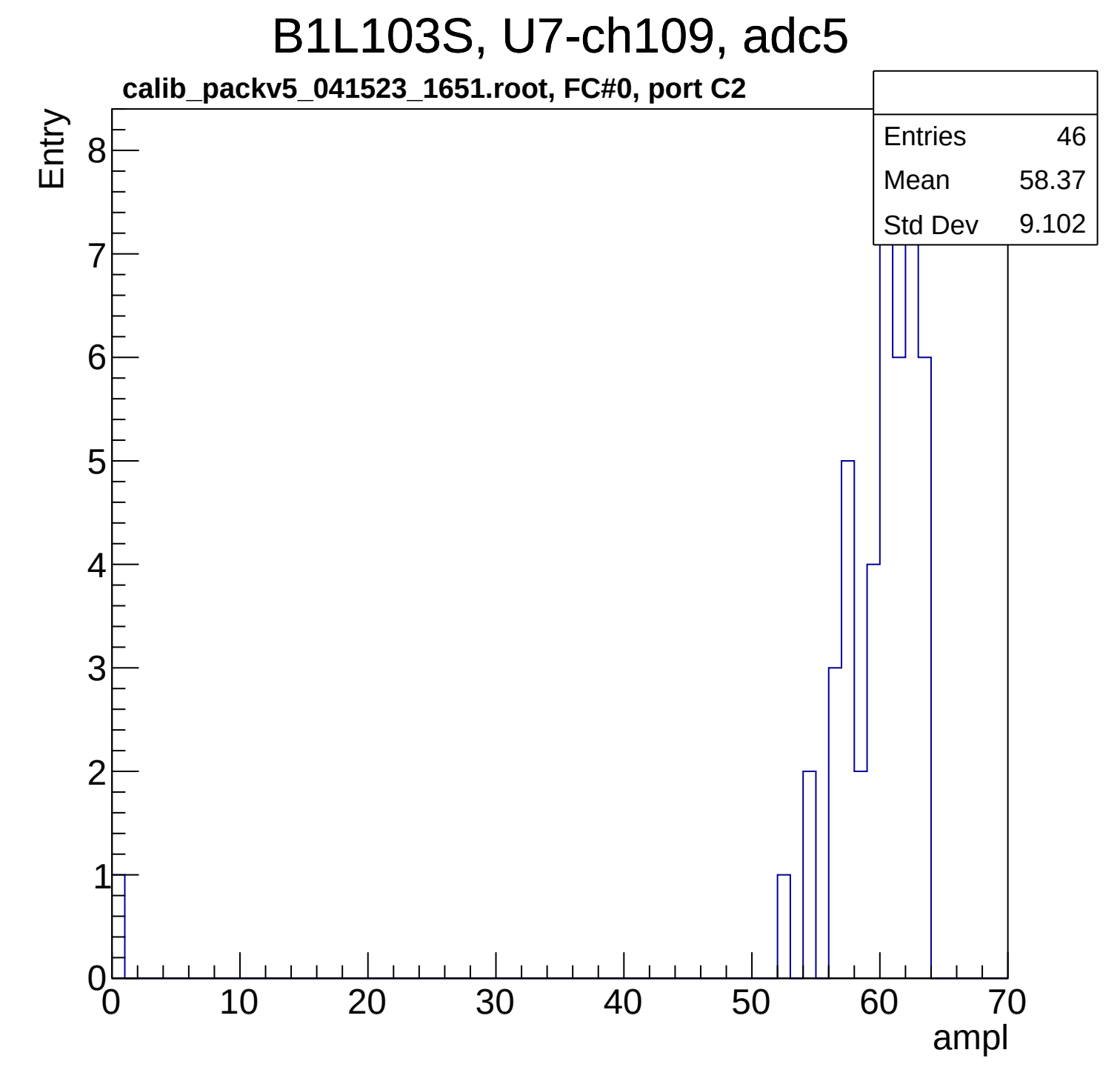
B1L103S, U7-ch109, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 58.37
Std Dev 9.102
Entry
ampl
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2
3
4
5
6
7
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0
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60
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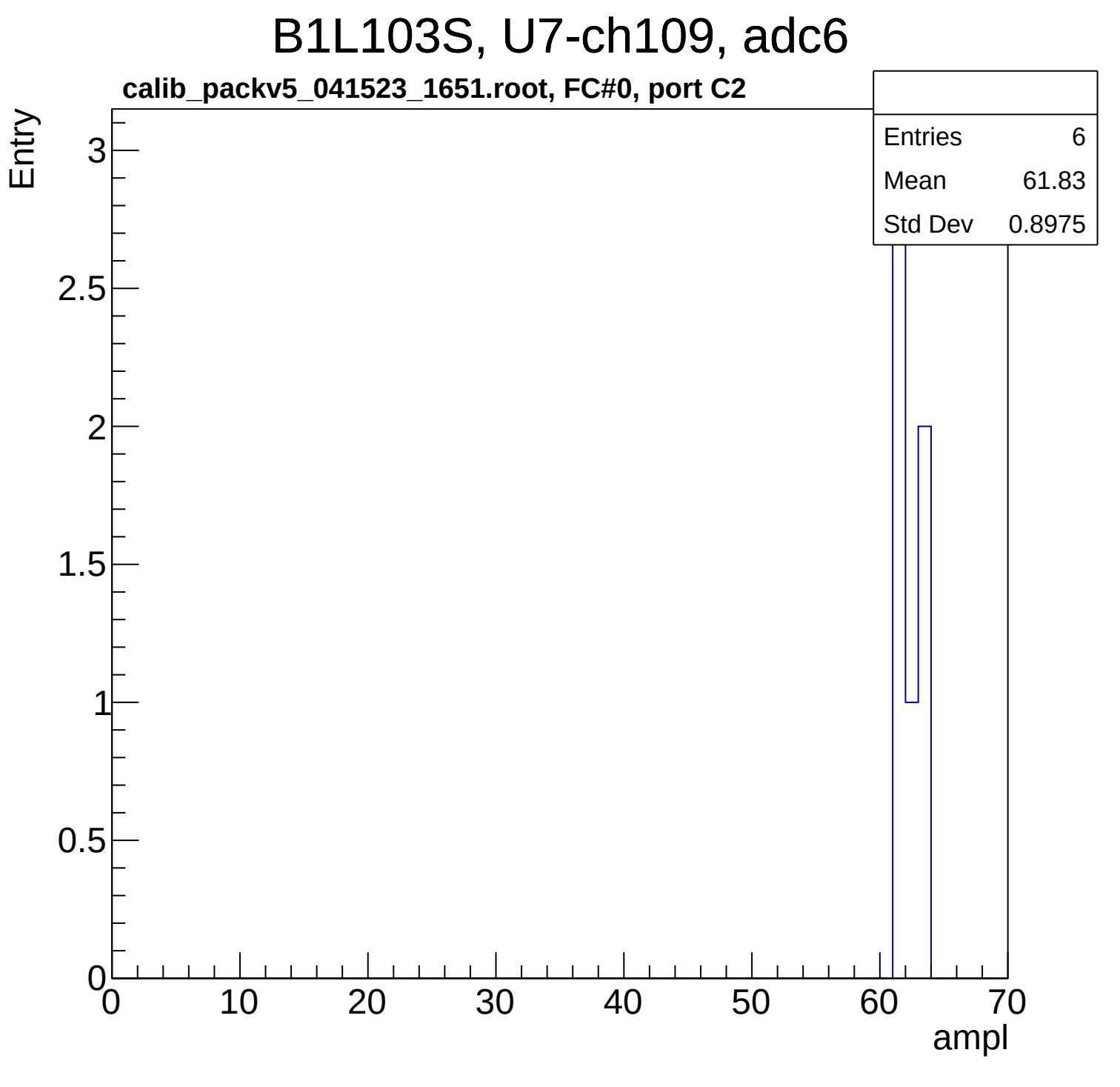
B1L103S, U7-ch109, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 61.83
Std Dev 0.8975
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
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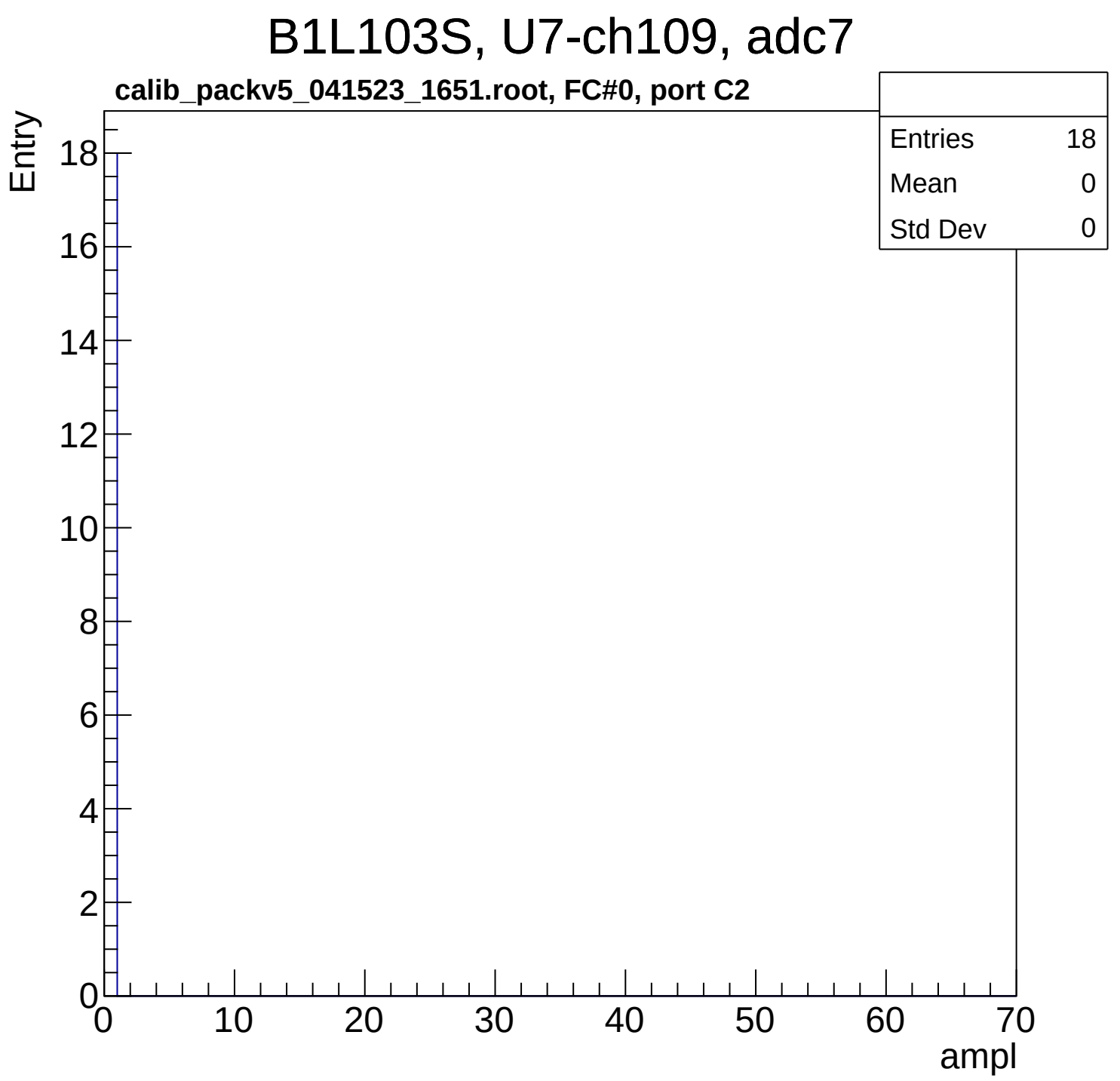
B1L103S, U7-ch109, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
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6
8
10
12
14
16
18
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10
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30
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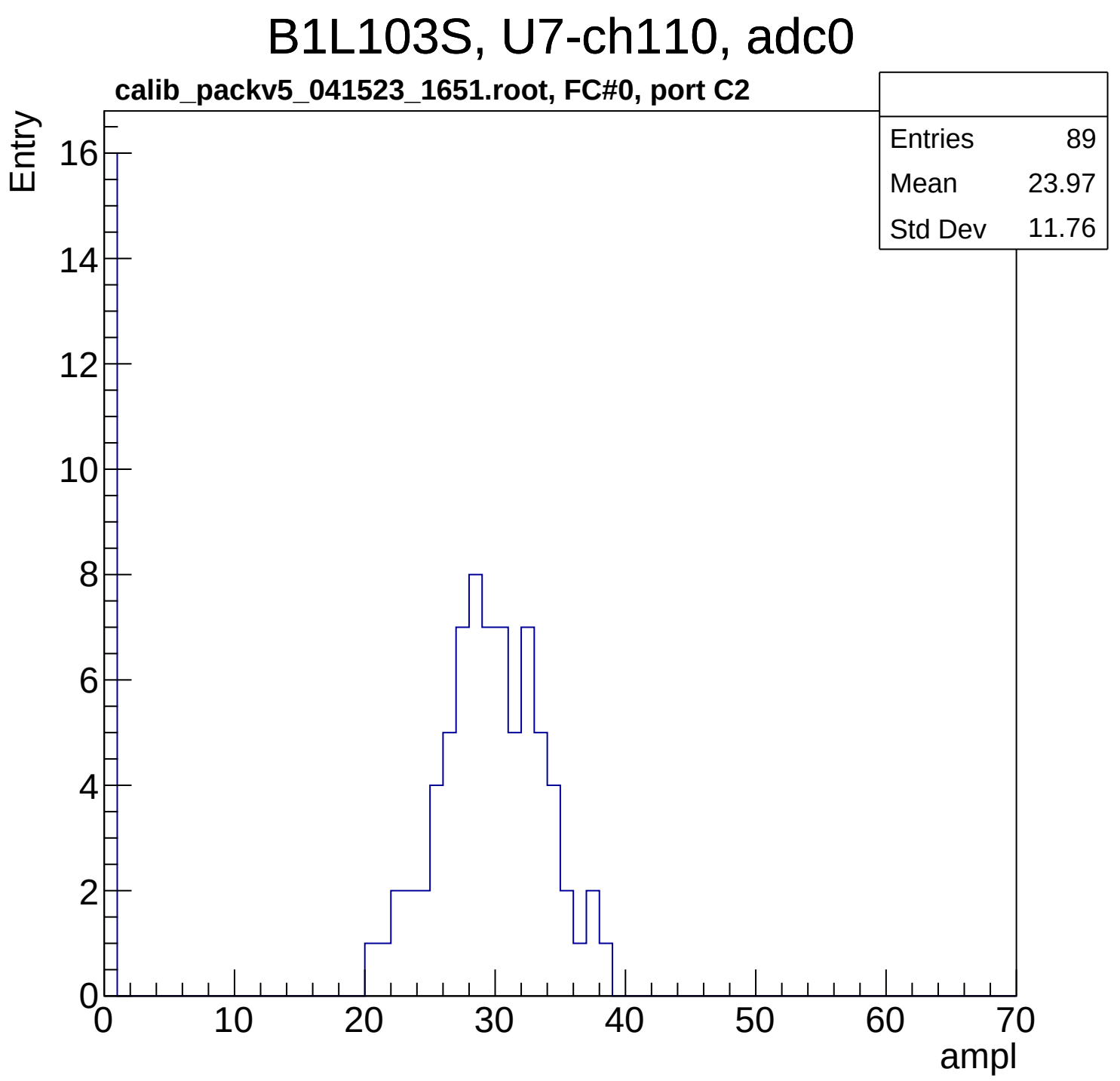
50
60
70
ampl


B1L103S, U7-ch110, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 89
Mean 23.97
Std Dev 11.76
Entry
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6
8
10
12
14
16
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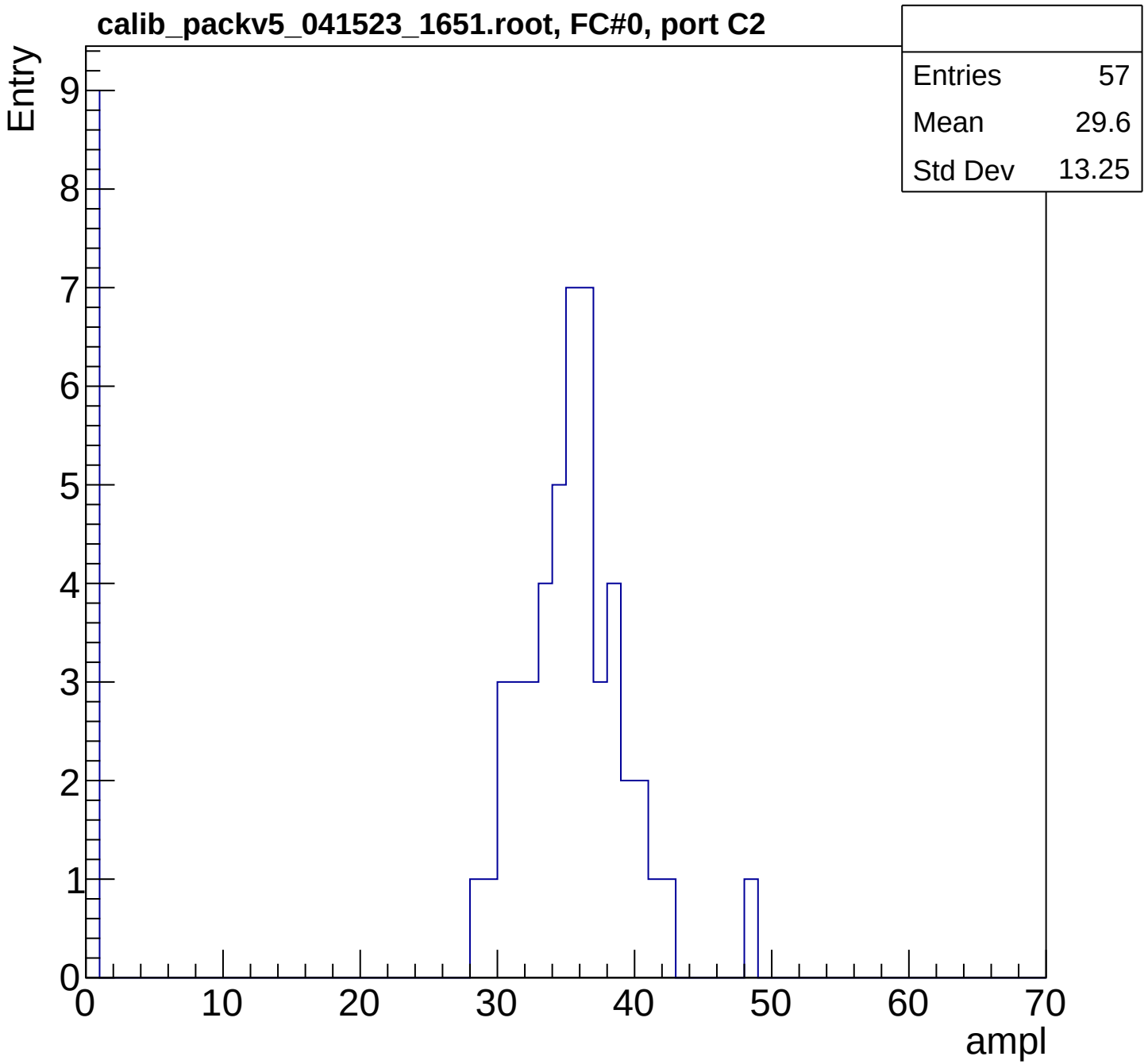
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch110, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 29.6
Std Dev 13.25
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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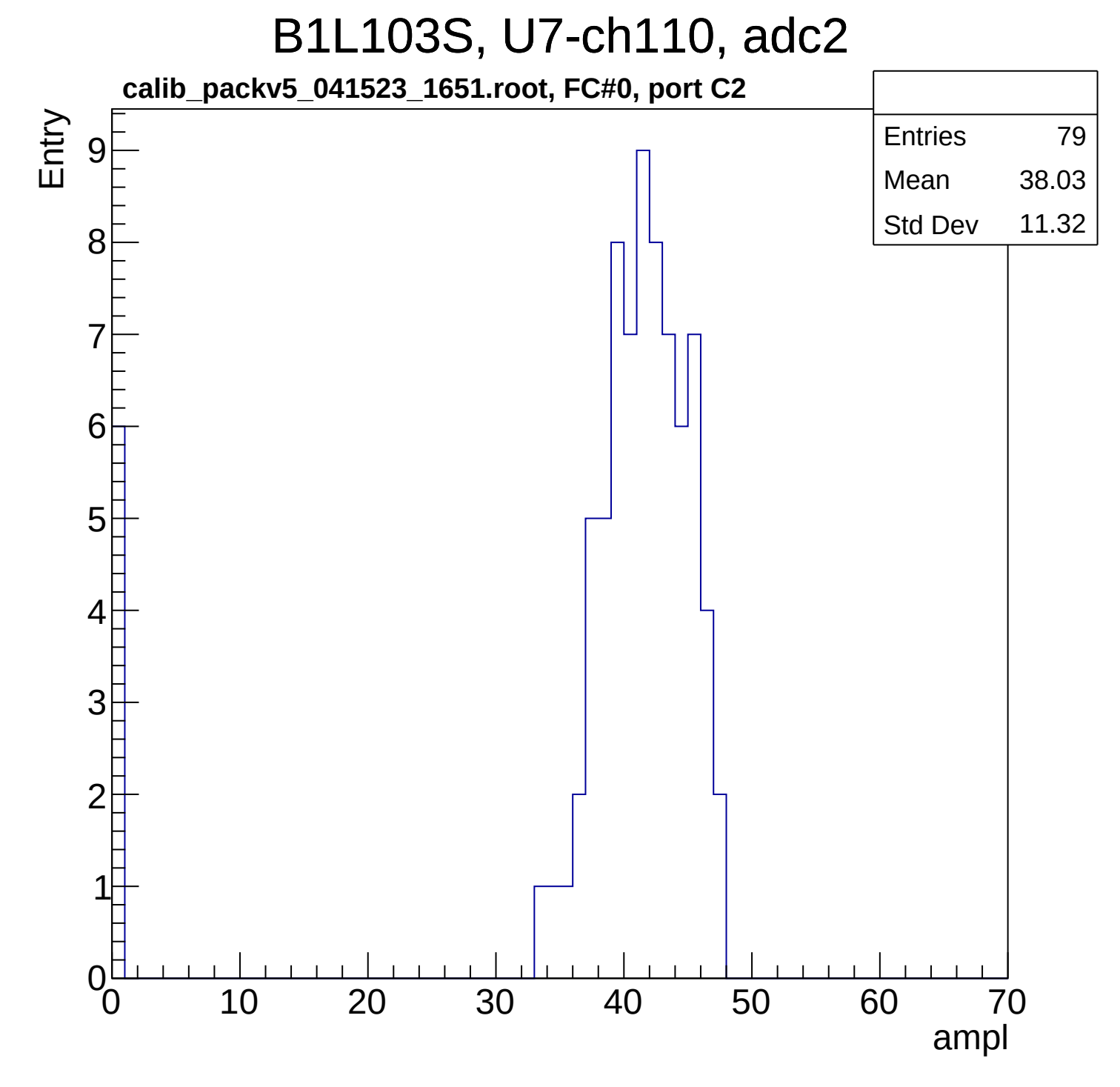
B1L103S, U7-ch110, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 38.03
Std Dev 11.32
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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60
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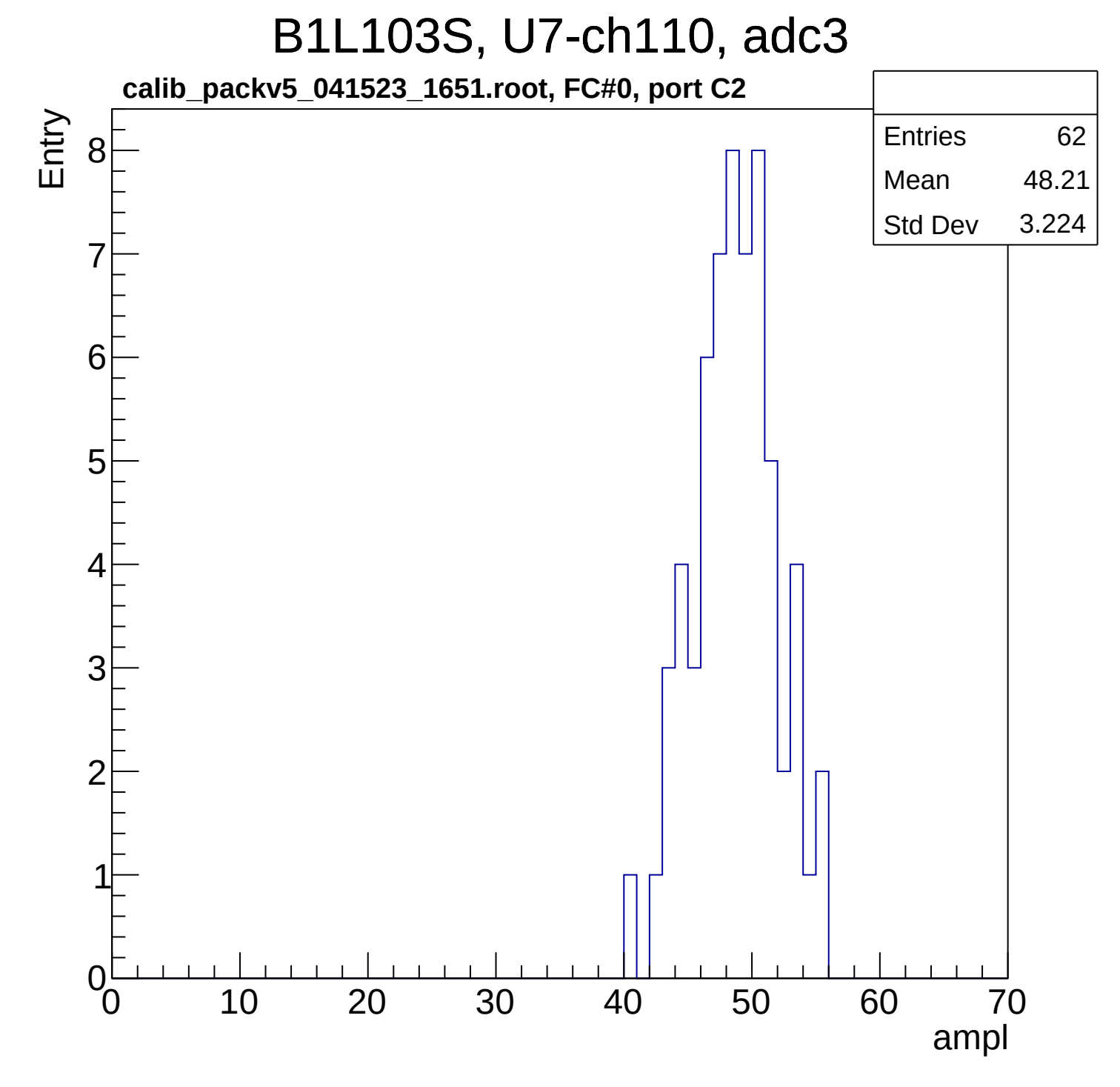
B1L103S, U7-ch110, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 48.21
Std Dev 3.224
Entry
ampl
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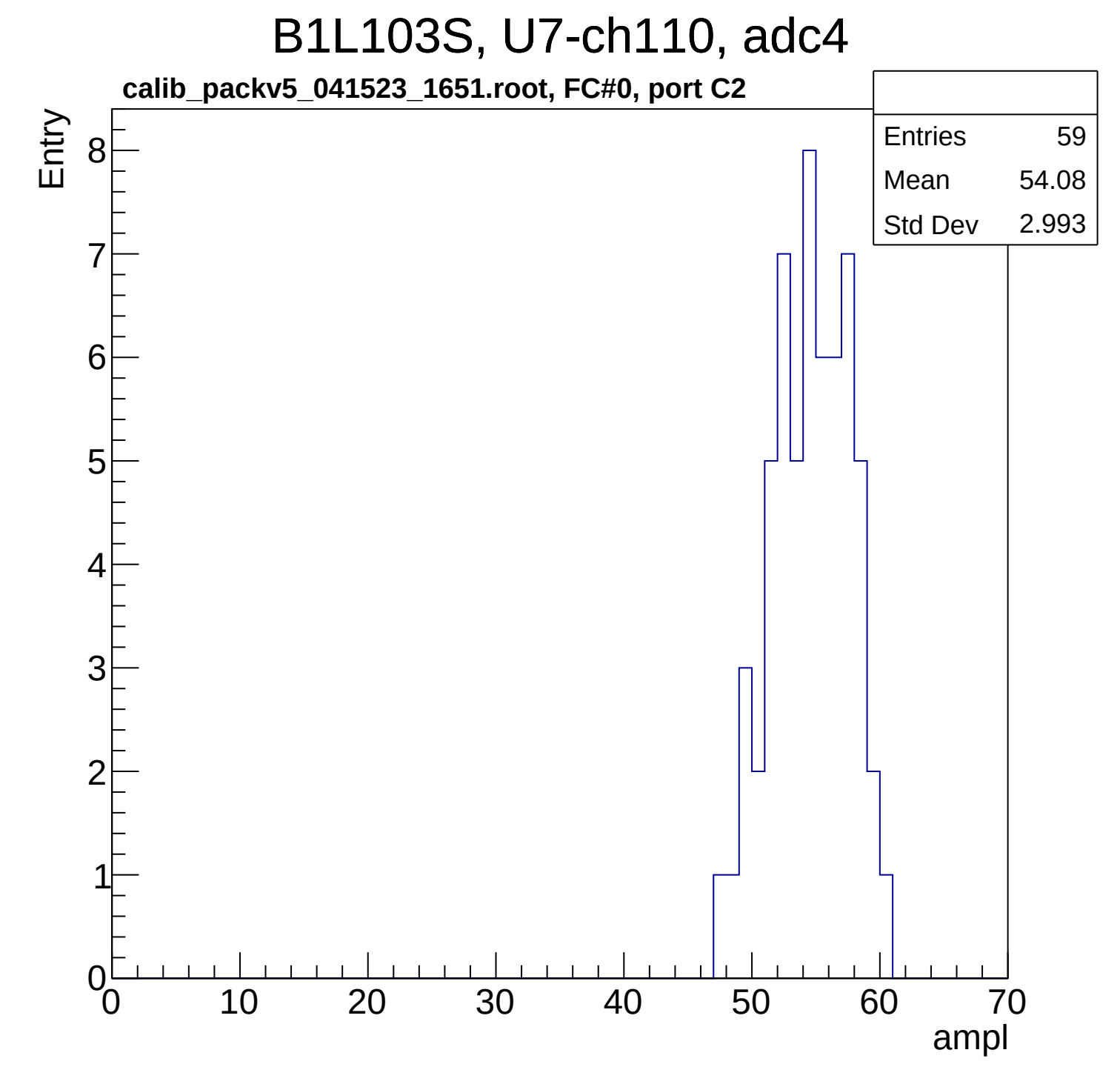
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch110, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 54.08
Std Dev 2.993
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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40
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60
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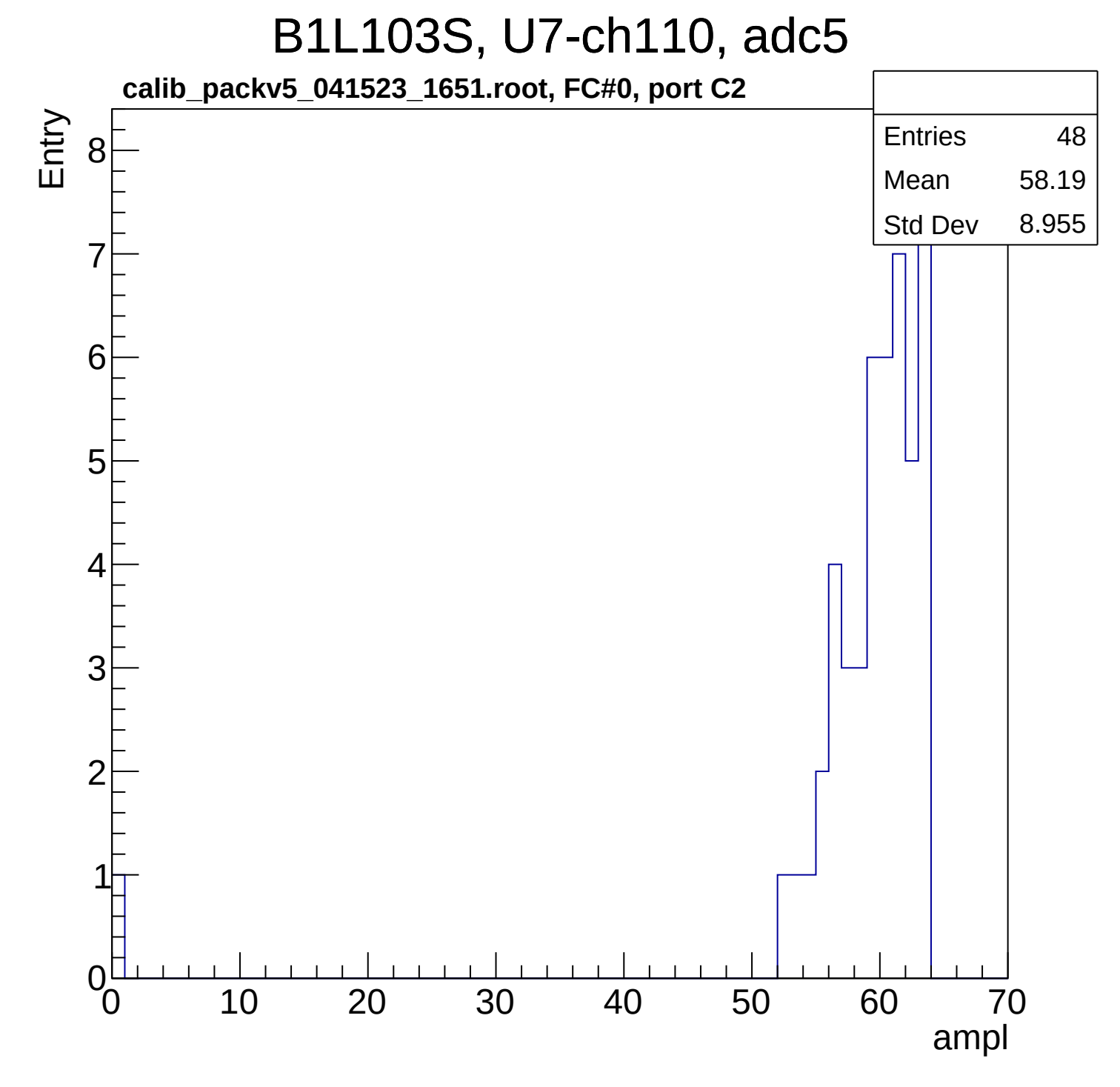
B1L103S, U7-ch110, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 58.19
Std Dev 8.955
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
30
40
50
60
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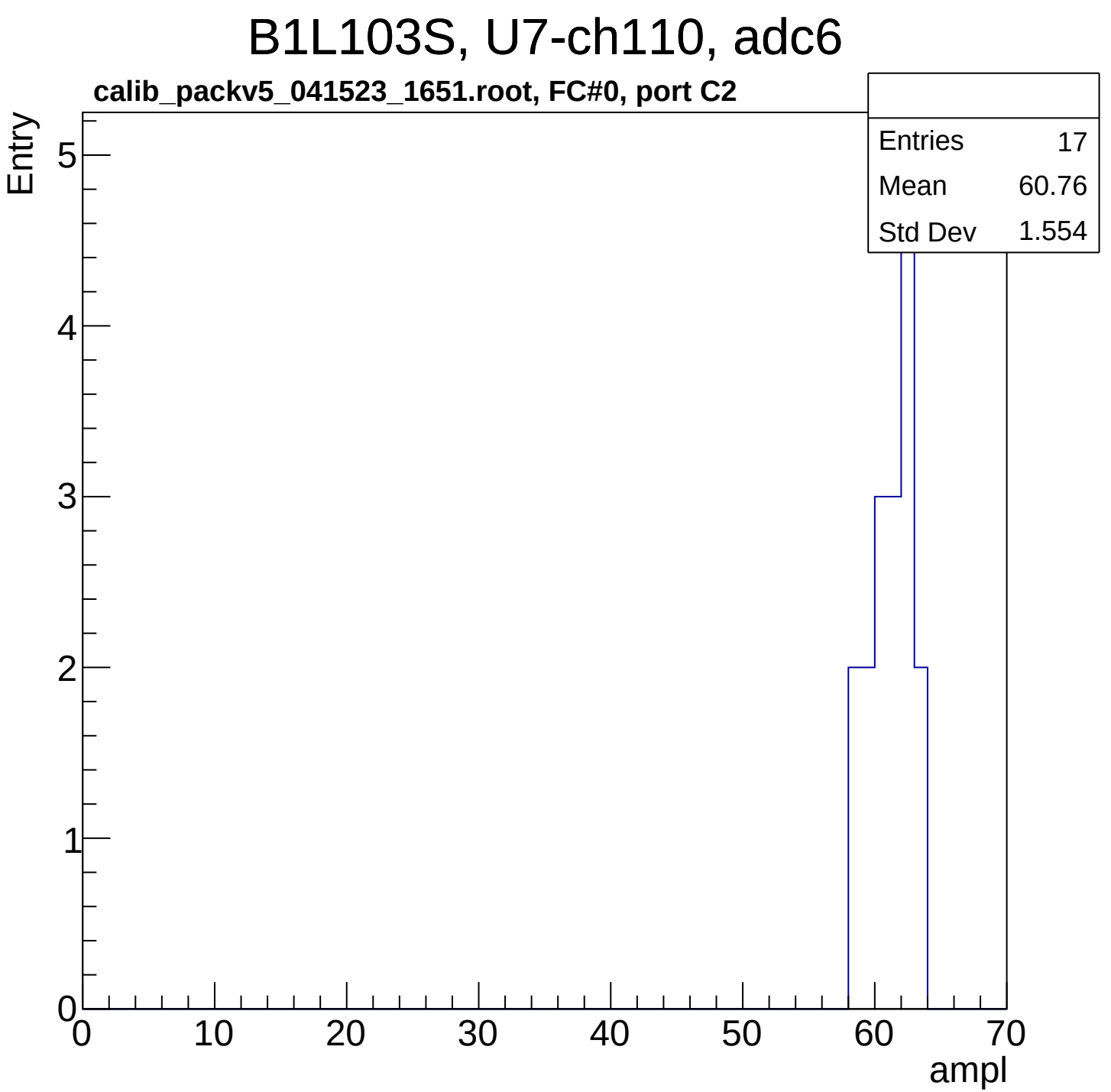
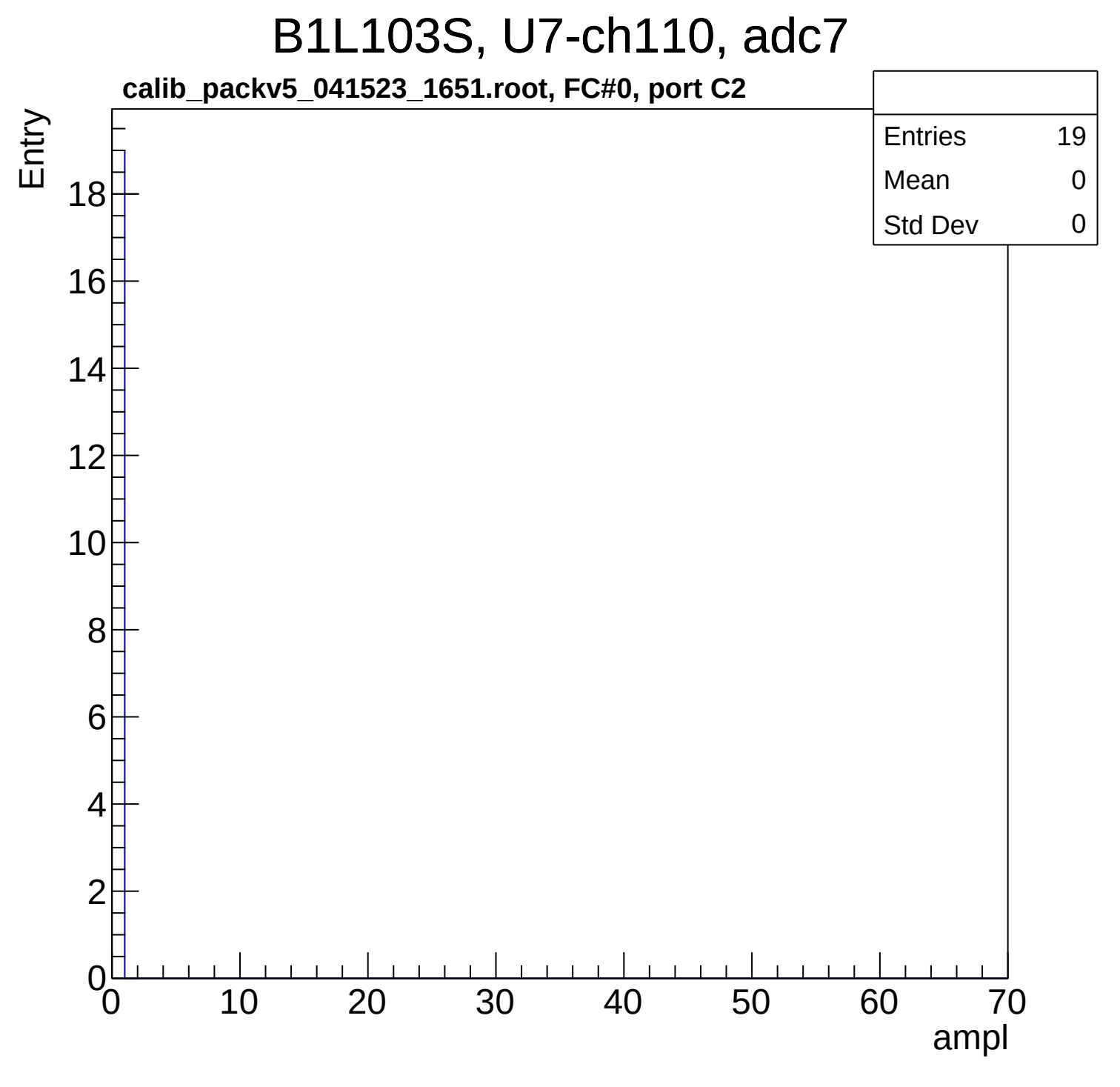

B1L103S, U7-ch110, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 17
Mean 60.76
Std Dev 1.554
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch110, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
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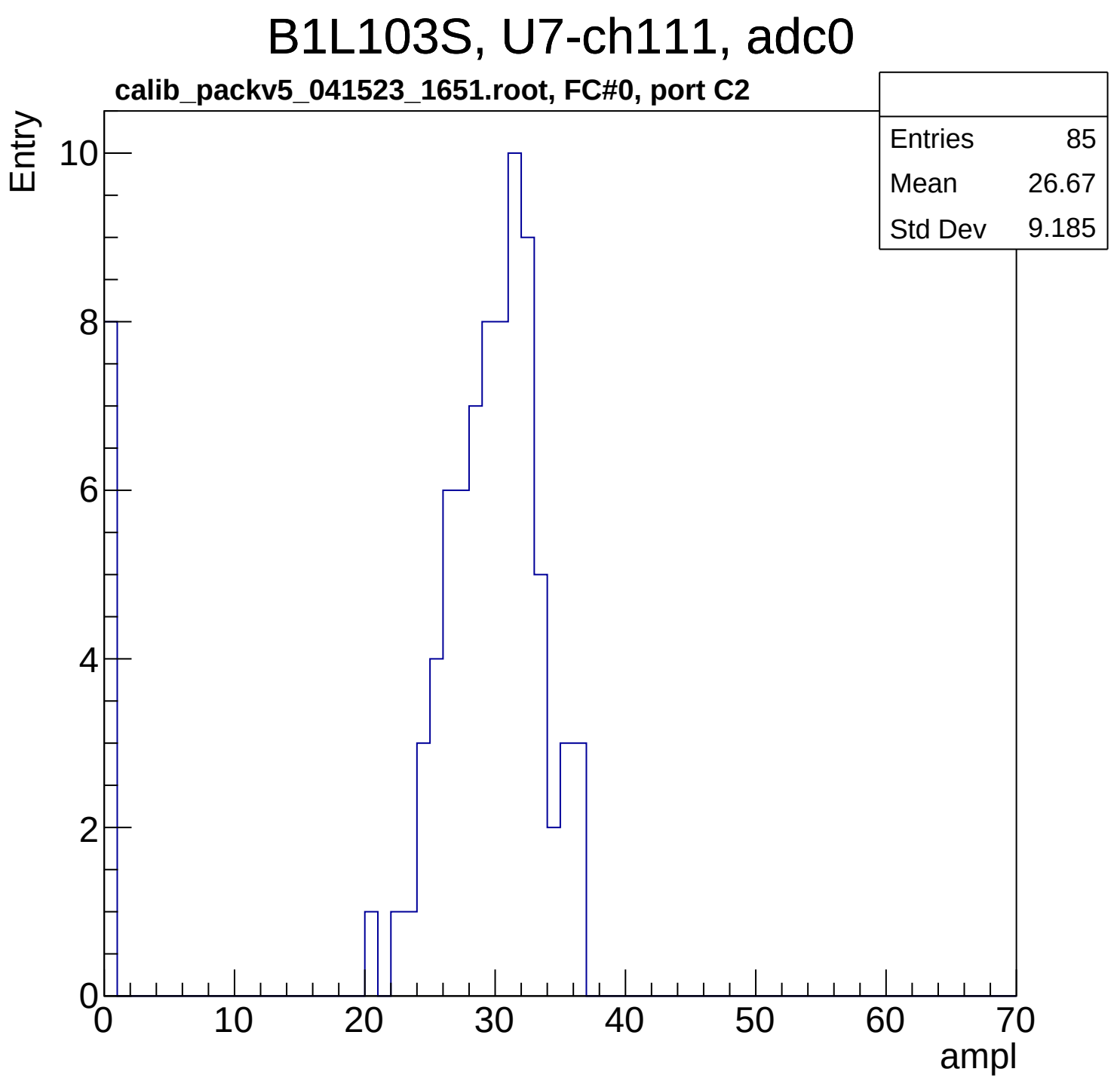
50
60
70
ampl


B1L103S, U7-ch111, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 26.67
Std Dev 9.185
Entry
ampl
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6
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0
10
20
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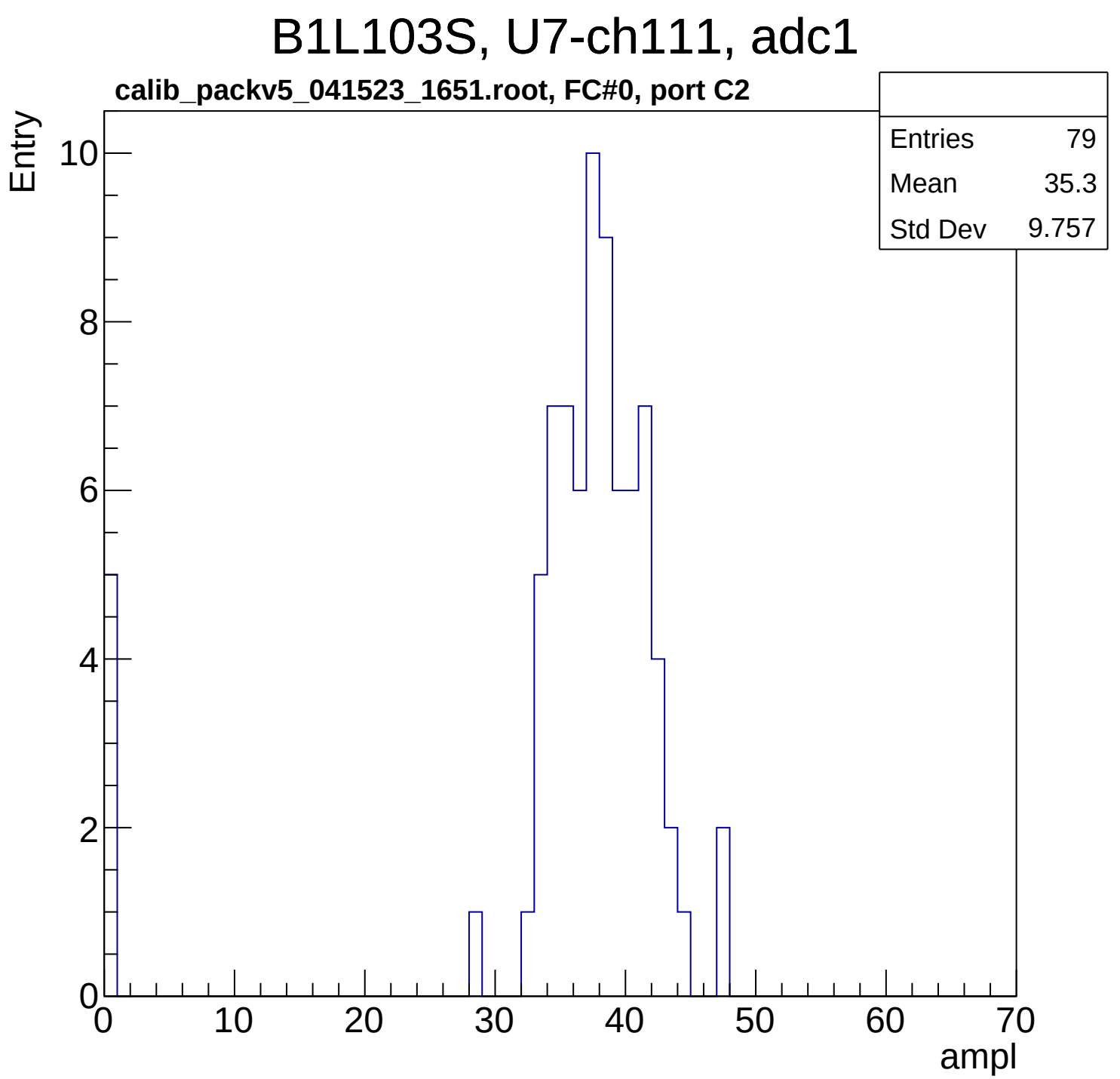
40
50
60
70


B1L103S, U7-ch111, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 35.3
Std Dev 9.757
Entry
ampl
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4
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0
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40
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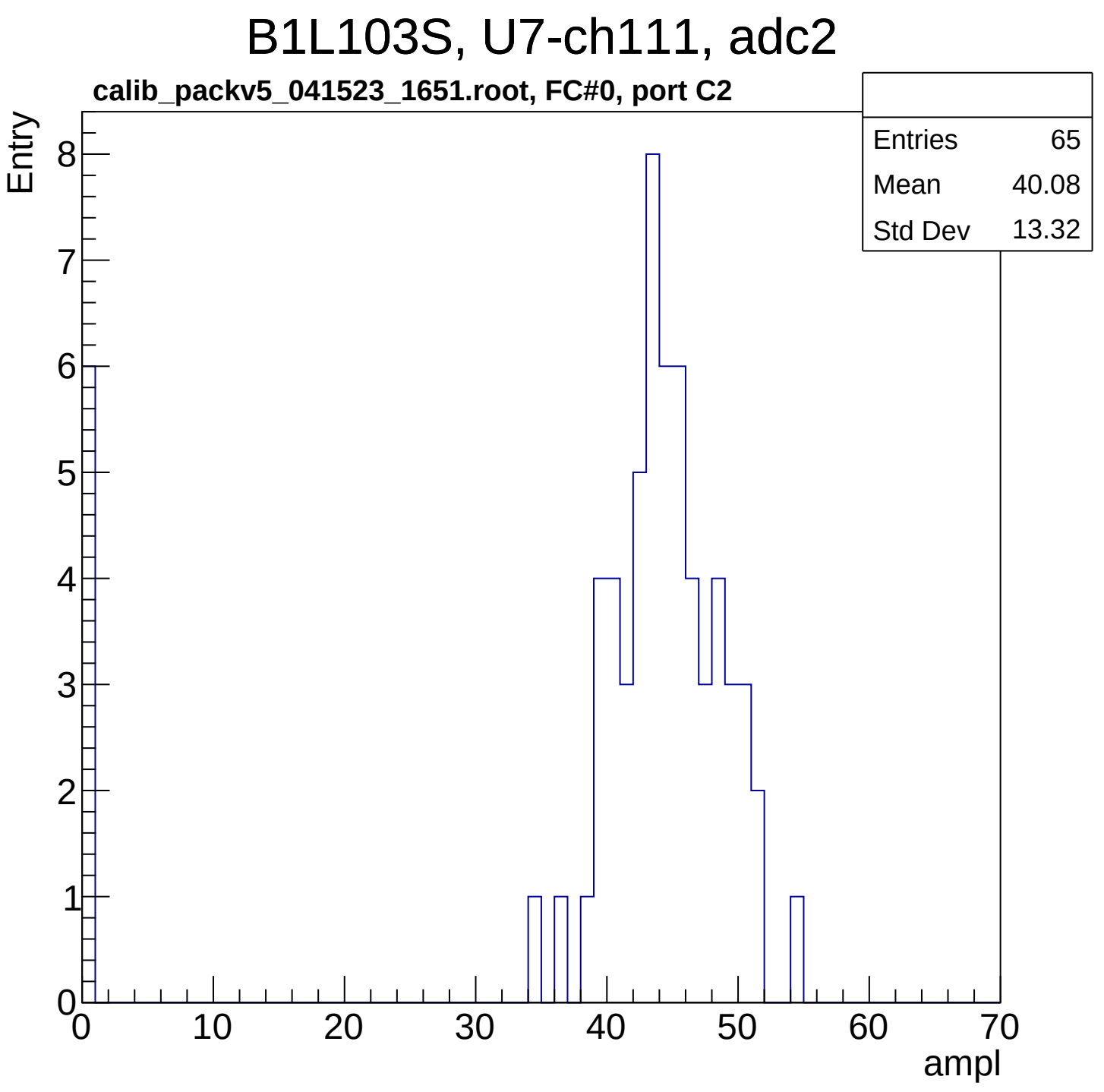
60
70


B1L103S, U7-ch111, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 40.08
Std Dev 13.32
Entry
ampl
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1
2
3
4
5
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7
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0
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40
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60
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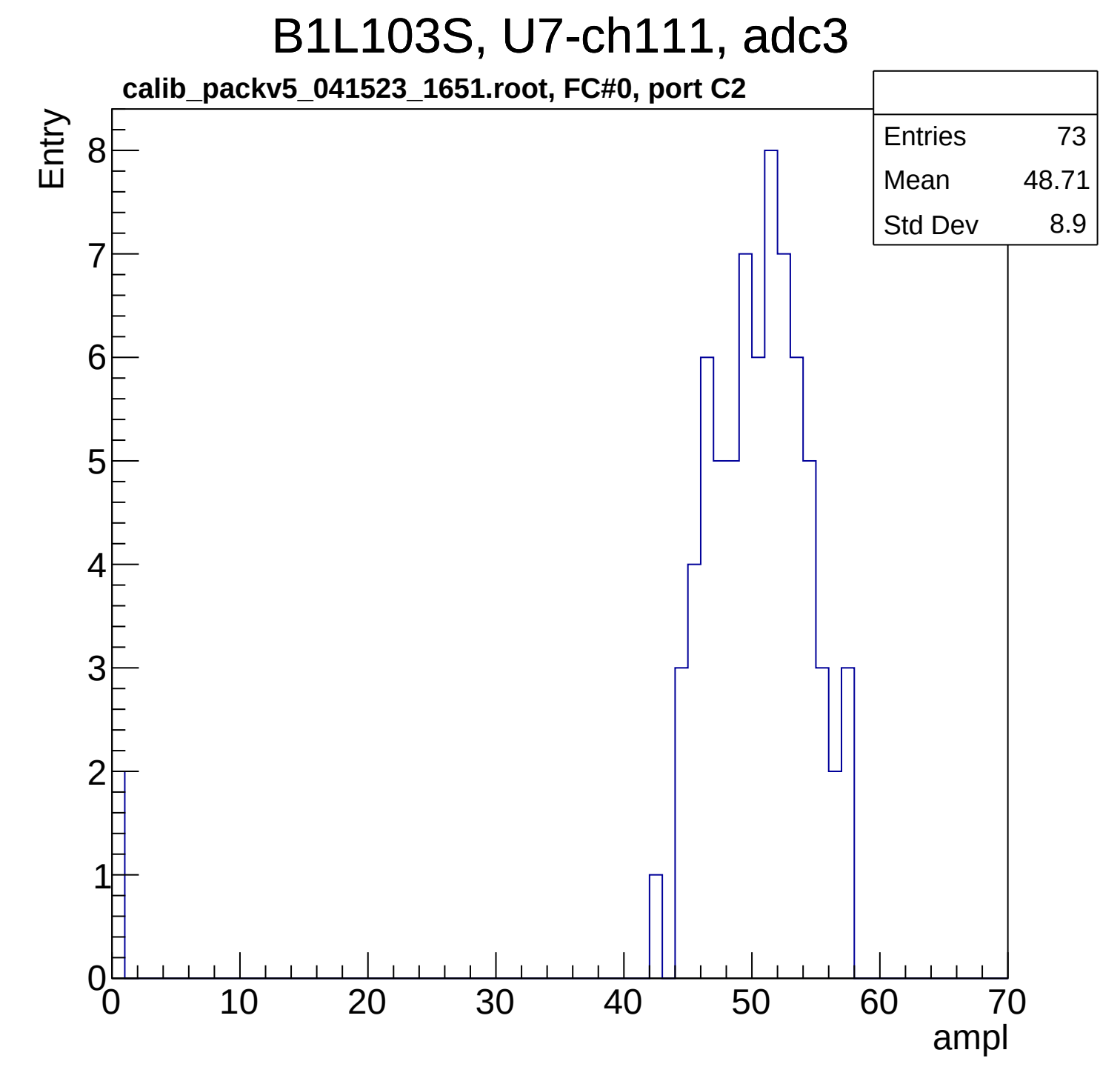
B1L103S, U7-ch111, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 48.71
Std Dev 8.9
Entry
ampl
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1
2
3
4
5
6
7
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0
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20
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40
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60
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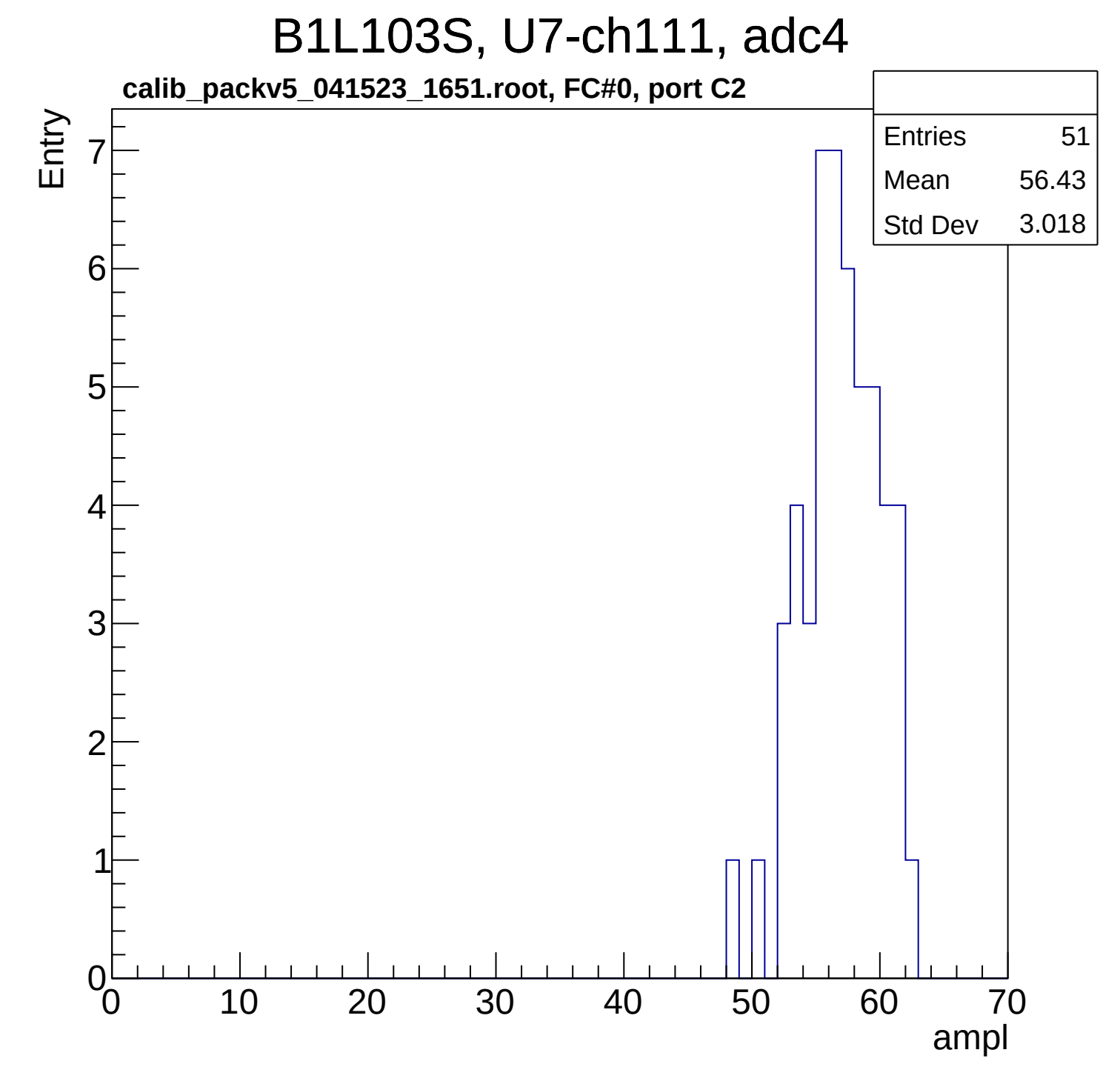
B1L103S, U7-ch111, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 56.43
Std Dev 3.018
Entry
ampl
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1
2
3
4
5
6
7
0
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20
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40
50
60
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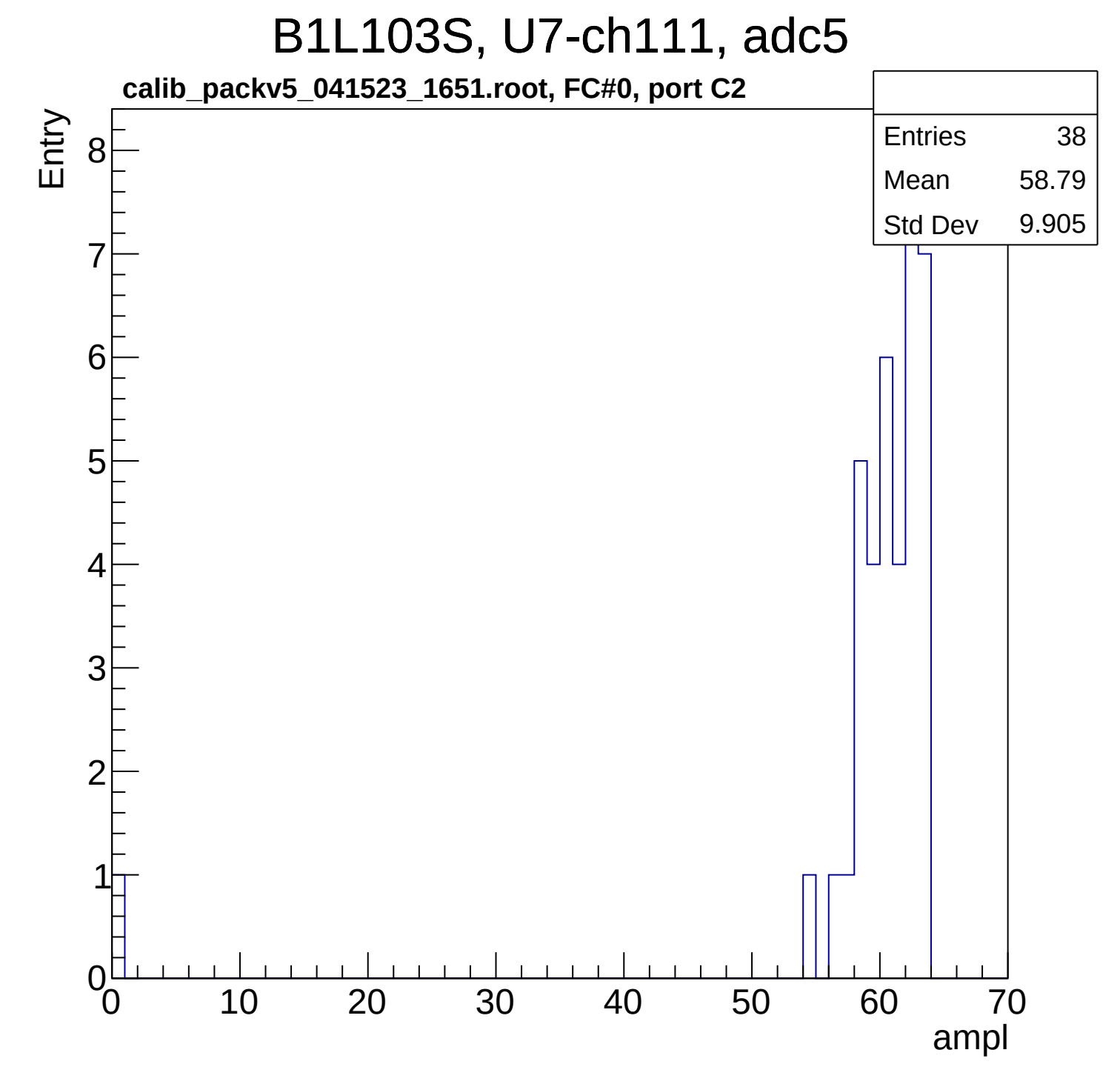
B1L103S, U7-ch111, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 38
Mean 58.79
Std Dev 9.905
Entry
ampl
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2
3
4
5
6
7
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0
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40
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60
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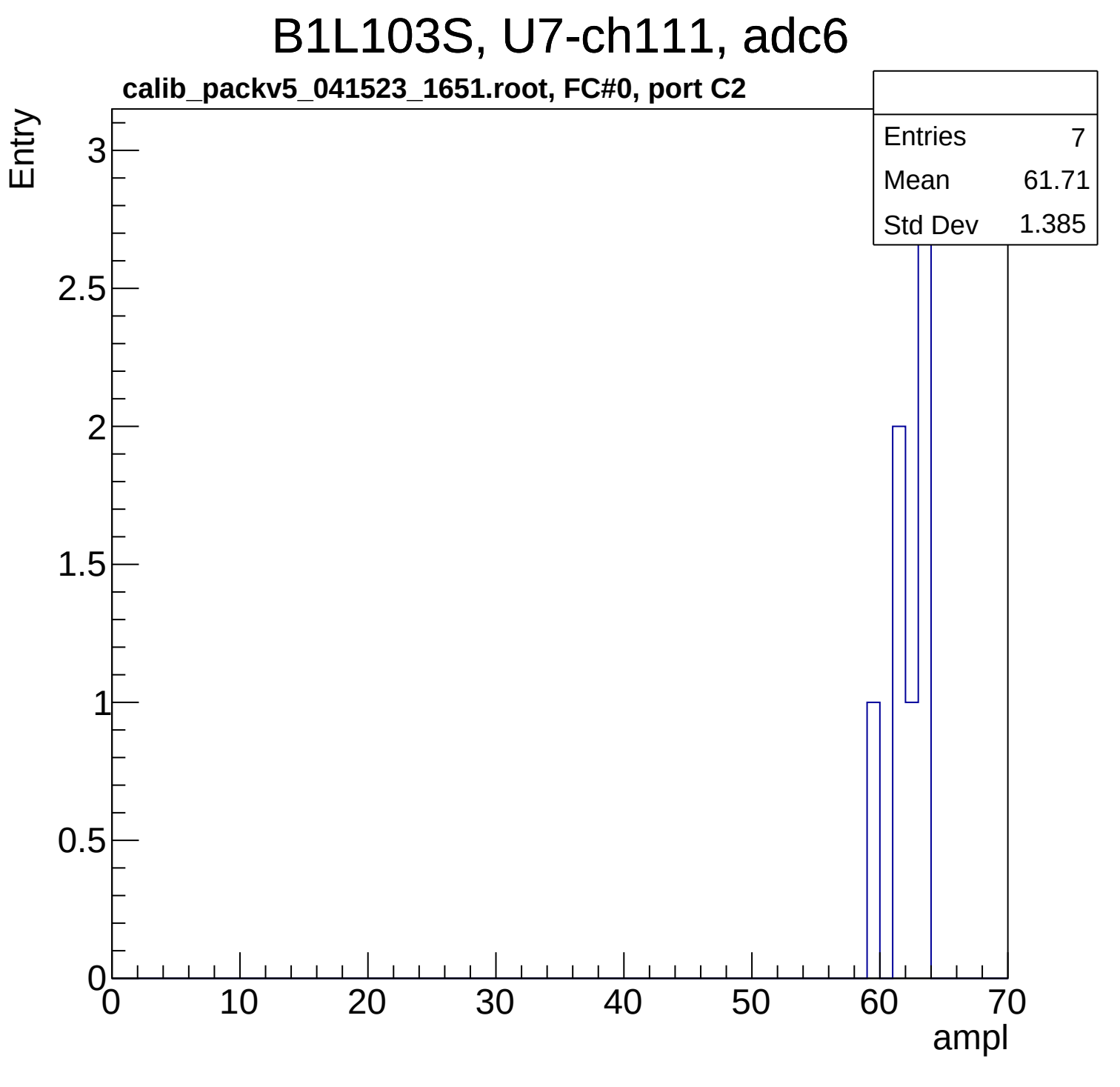
B1L103S, U7-ch111, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 61.71
Std Dev 1.385
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
10
20
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40
50
60
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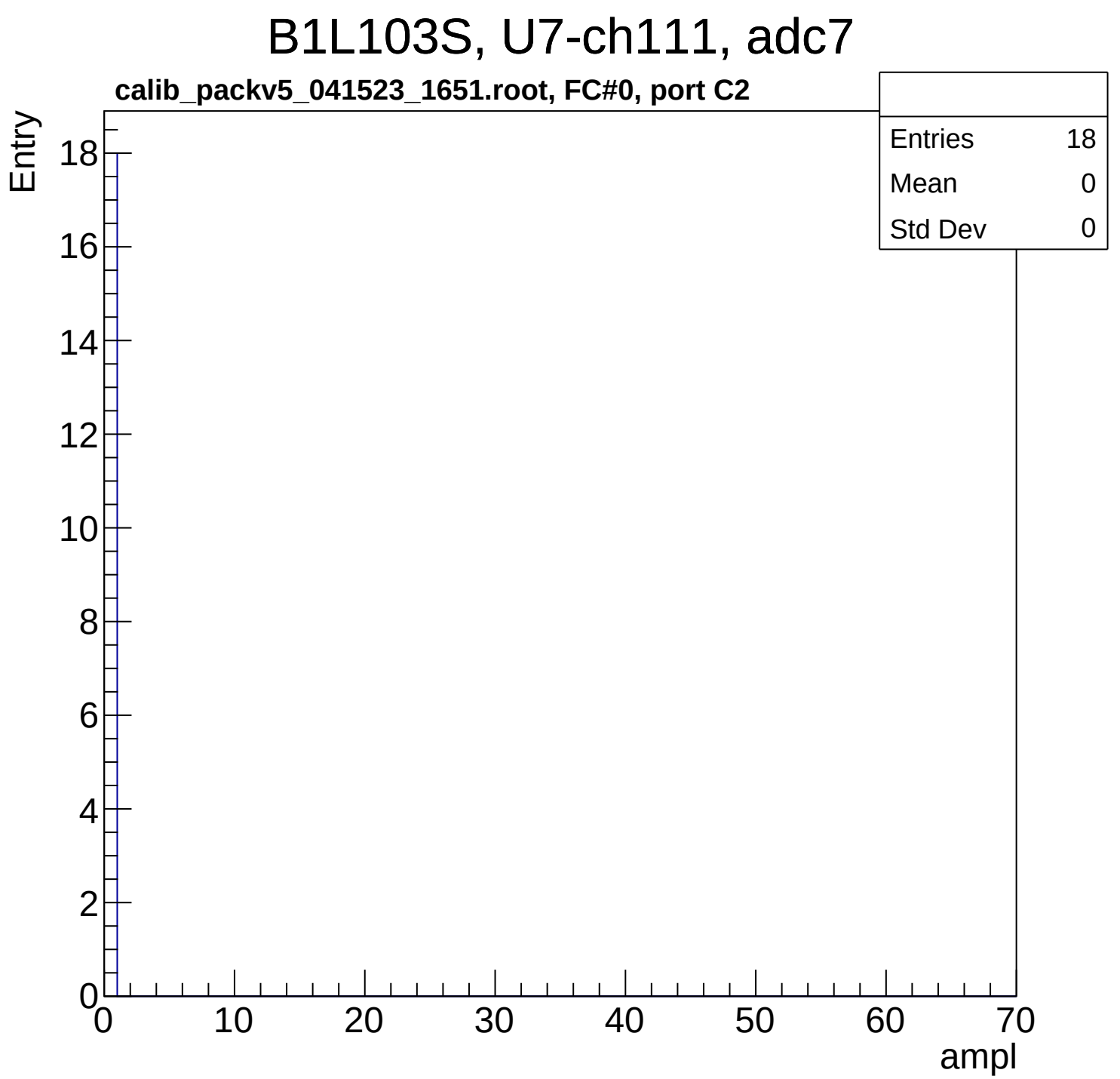
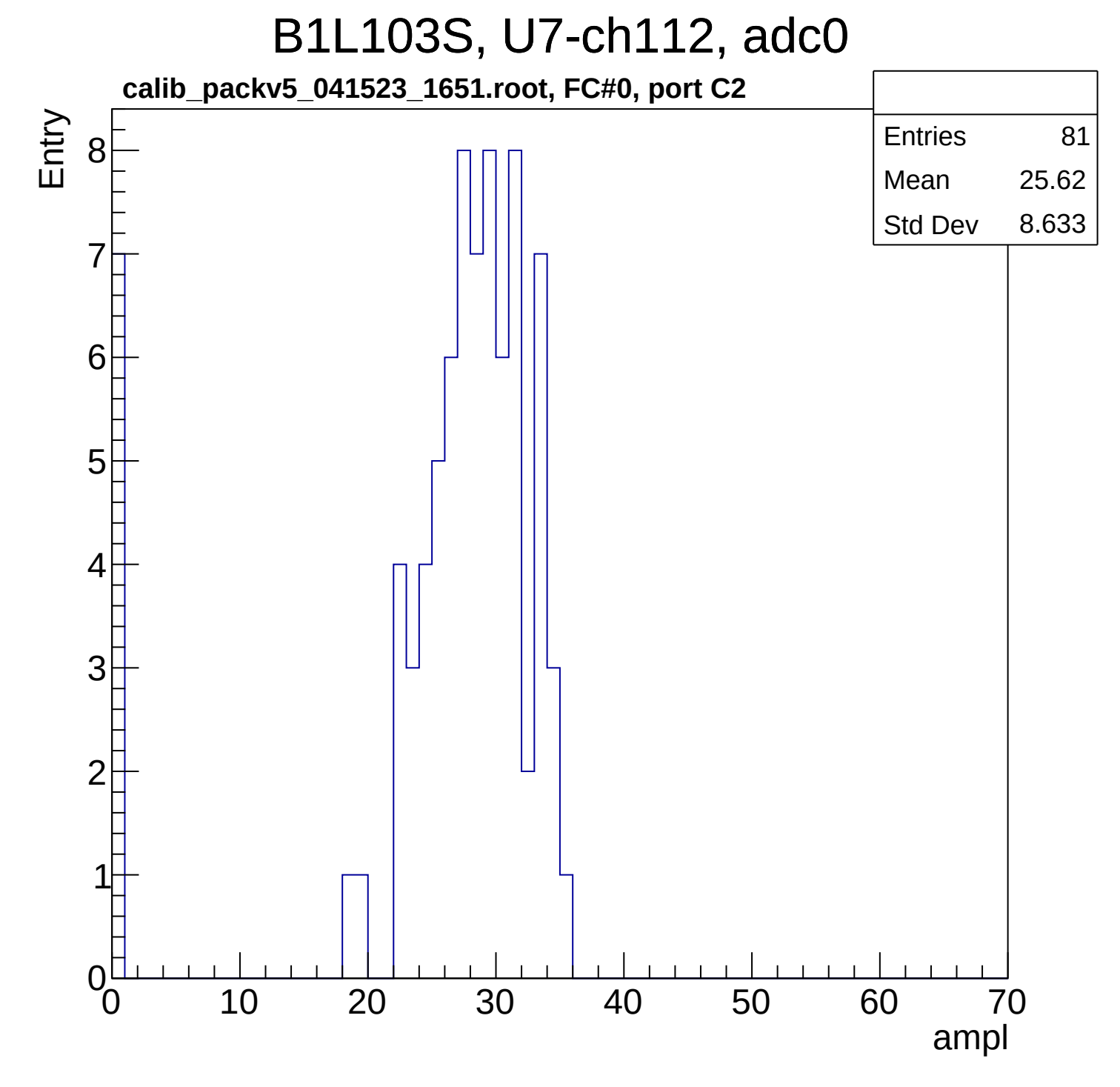

B1L103S, U7-ch111, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch112, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 25.62
Std Dev 8.633
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
30
40
50
60
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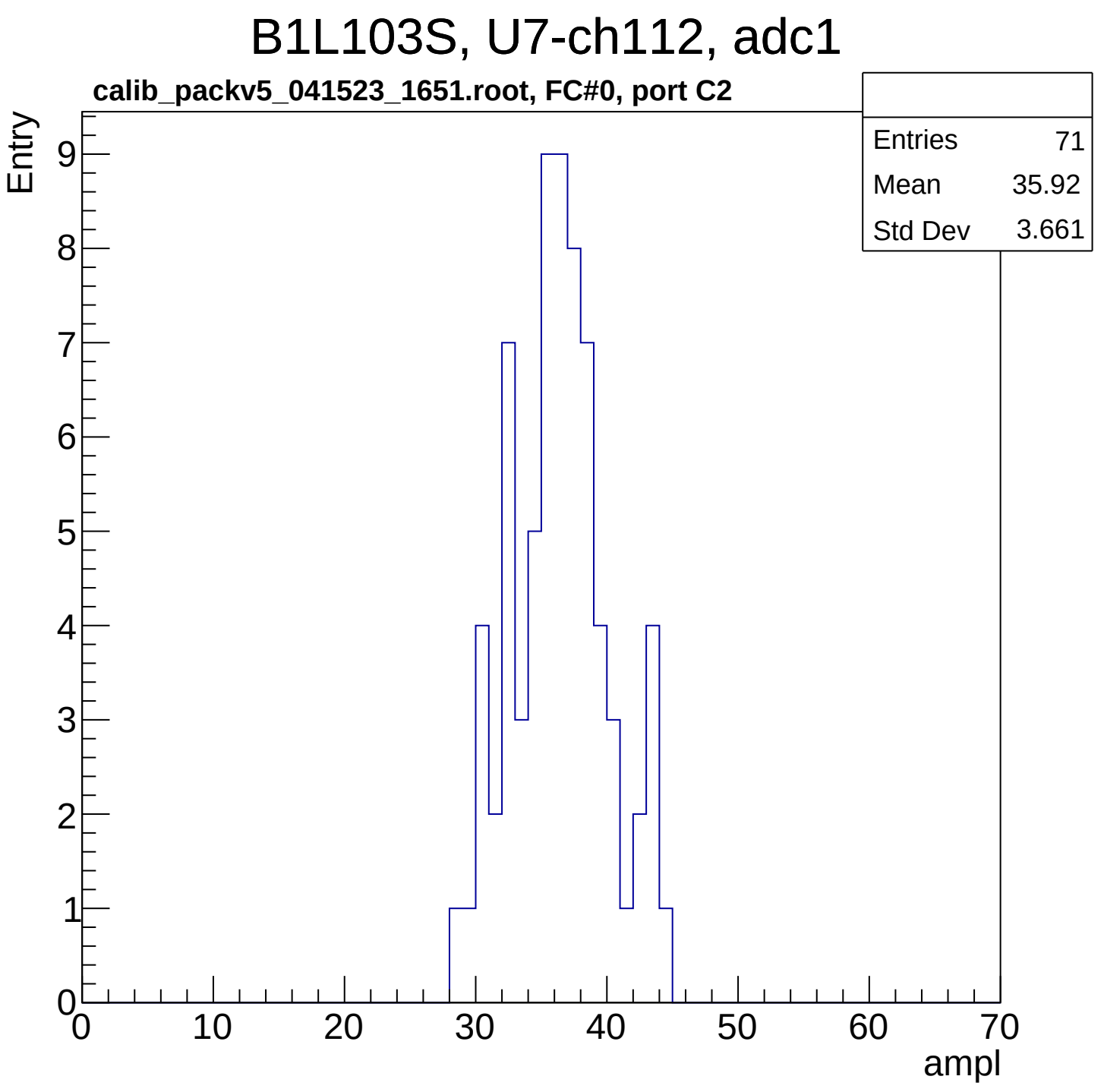
B1L103S, U7-ch112, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 35.92
Std Dev 3.661
Entry
ampl
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3
4
5
6
7
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9
0
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60
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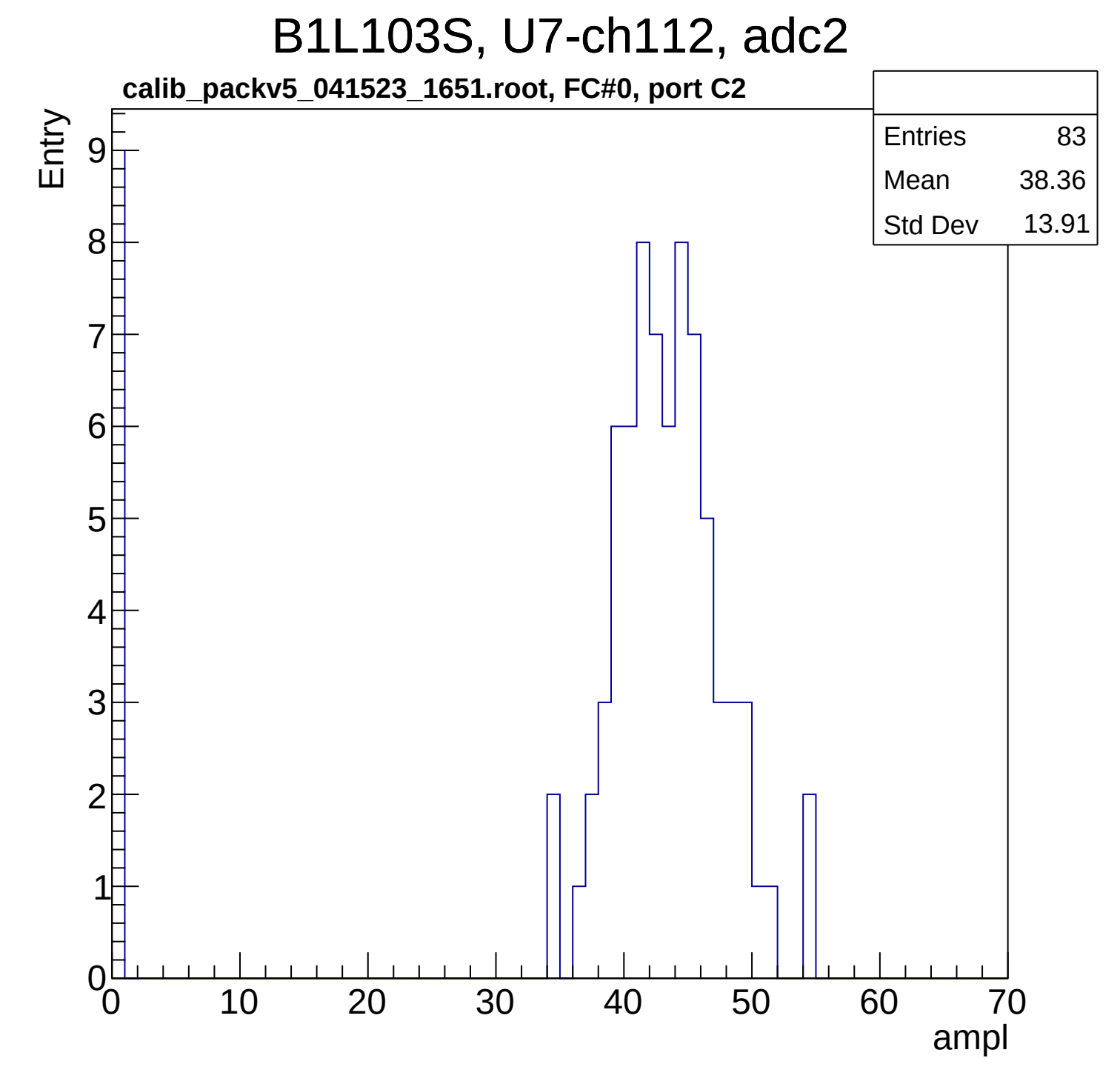
B1L103S, U7-ch112, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 38.36
Std Dev 13.91
Entry
ampl
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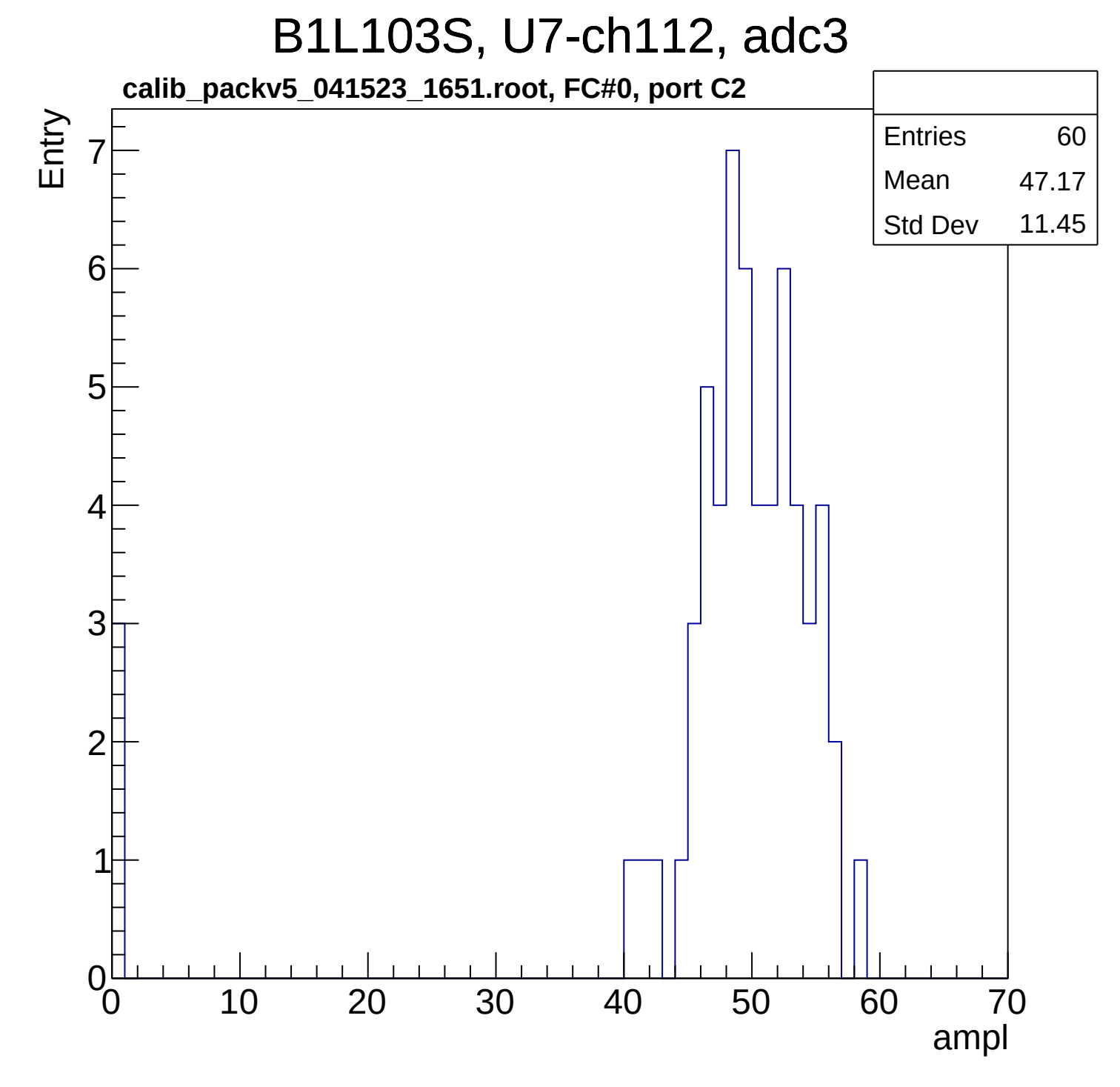
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U7-ch112, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 47.17
Std Dev 11.45
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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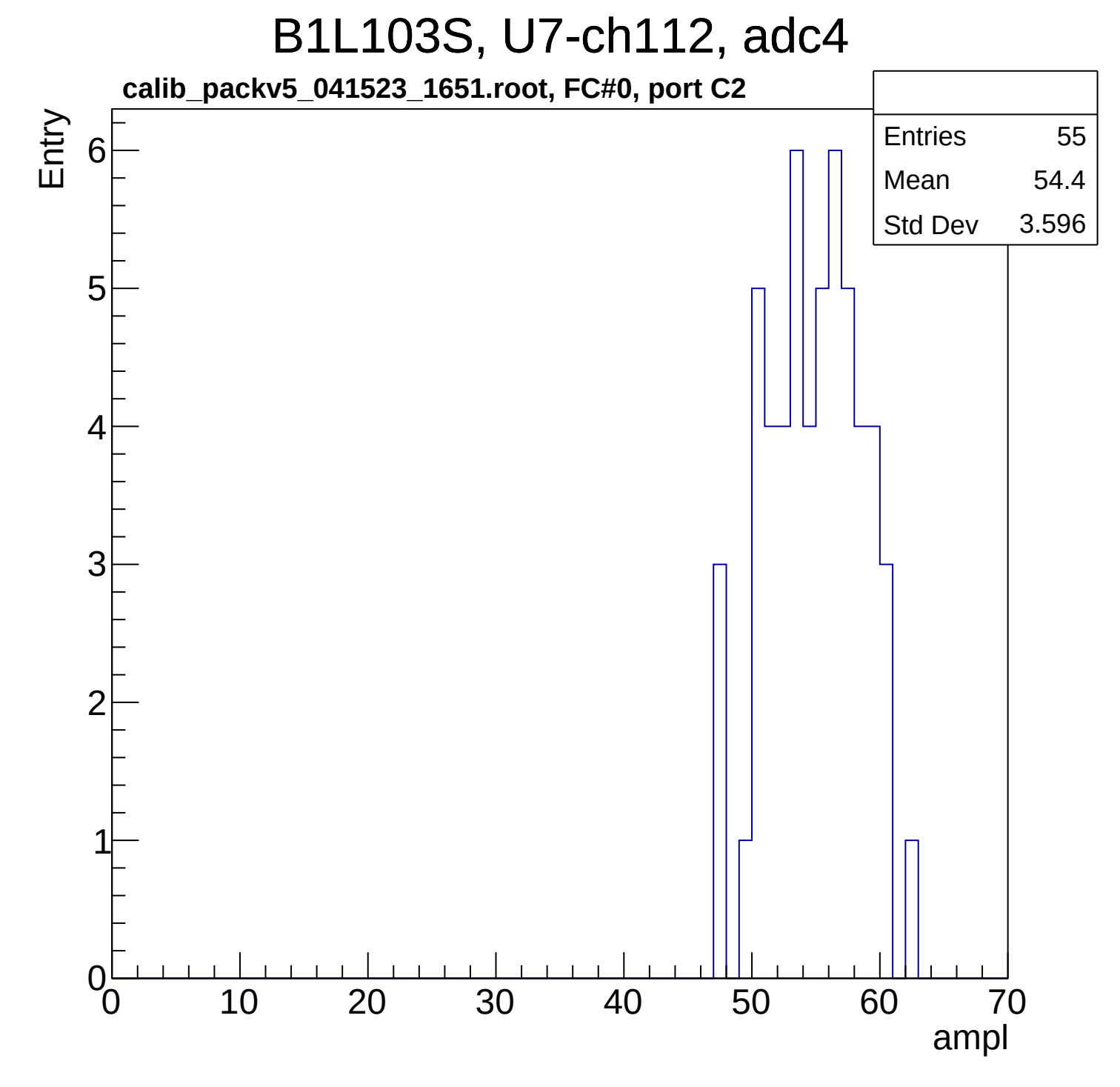
B1L103S, U7-ch112, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 54.4
Std Dev 3.596
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
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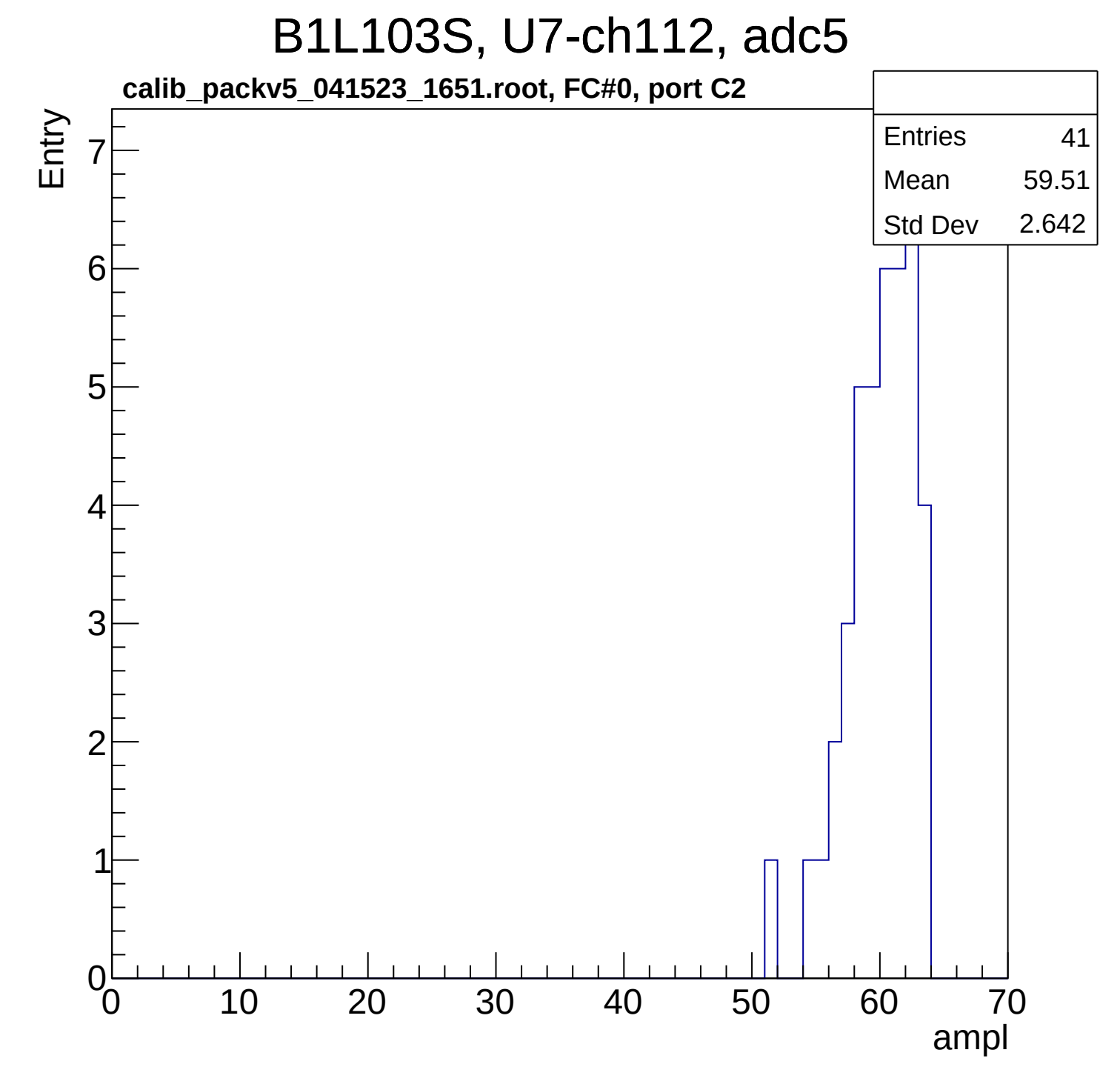
B1L103S, U7-ch112, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 41
Mean 59.51
Std Dev 2.642
Entry
ampl
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1
2
3
4
5
6
7
0
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40
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60
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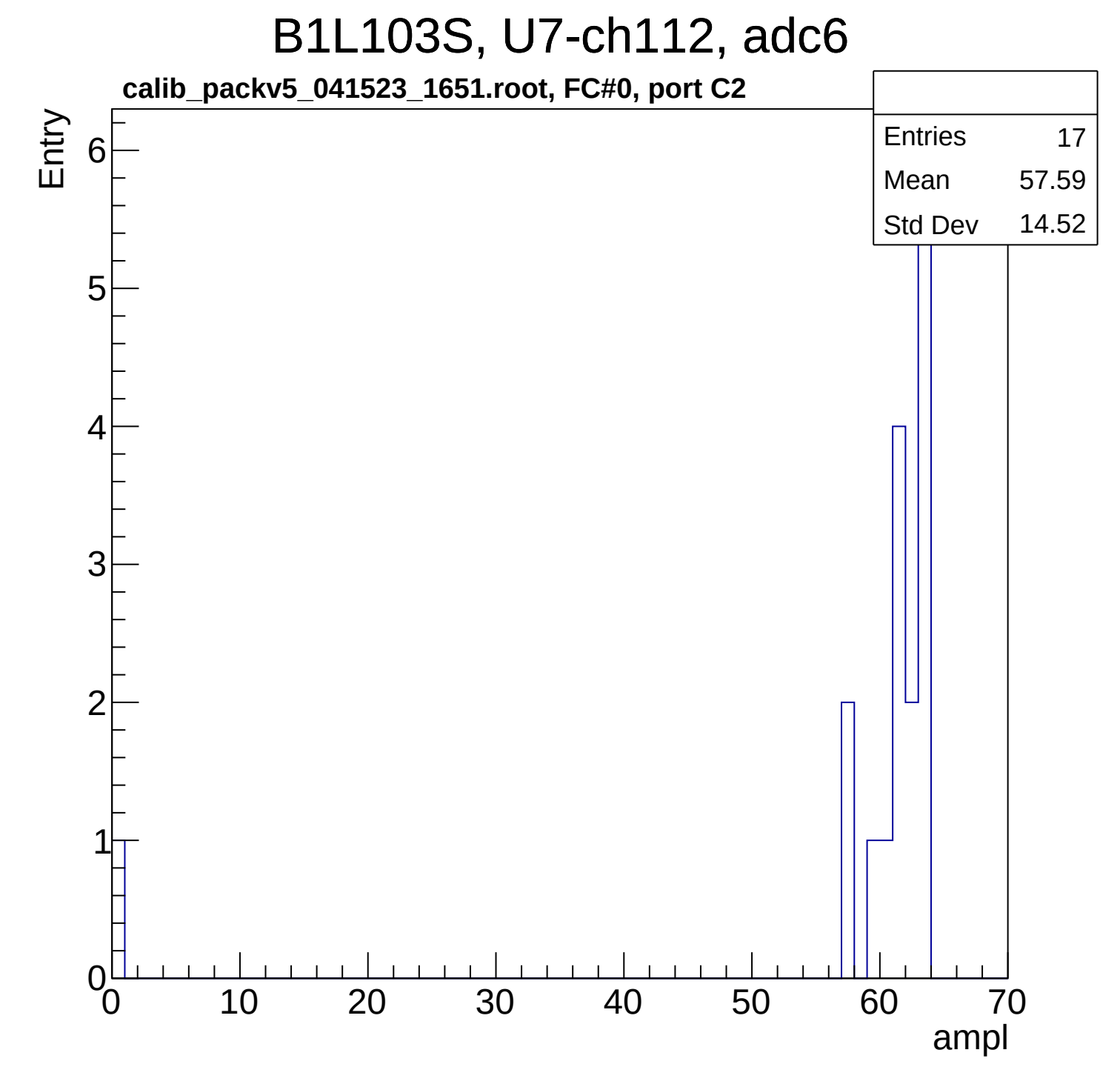
B1L103S, U7-ch112, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 17
Mean 57.59
Std Dev 14.52
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
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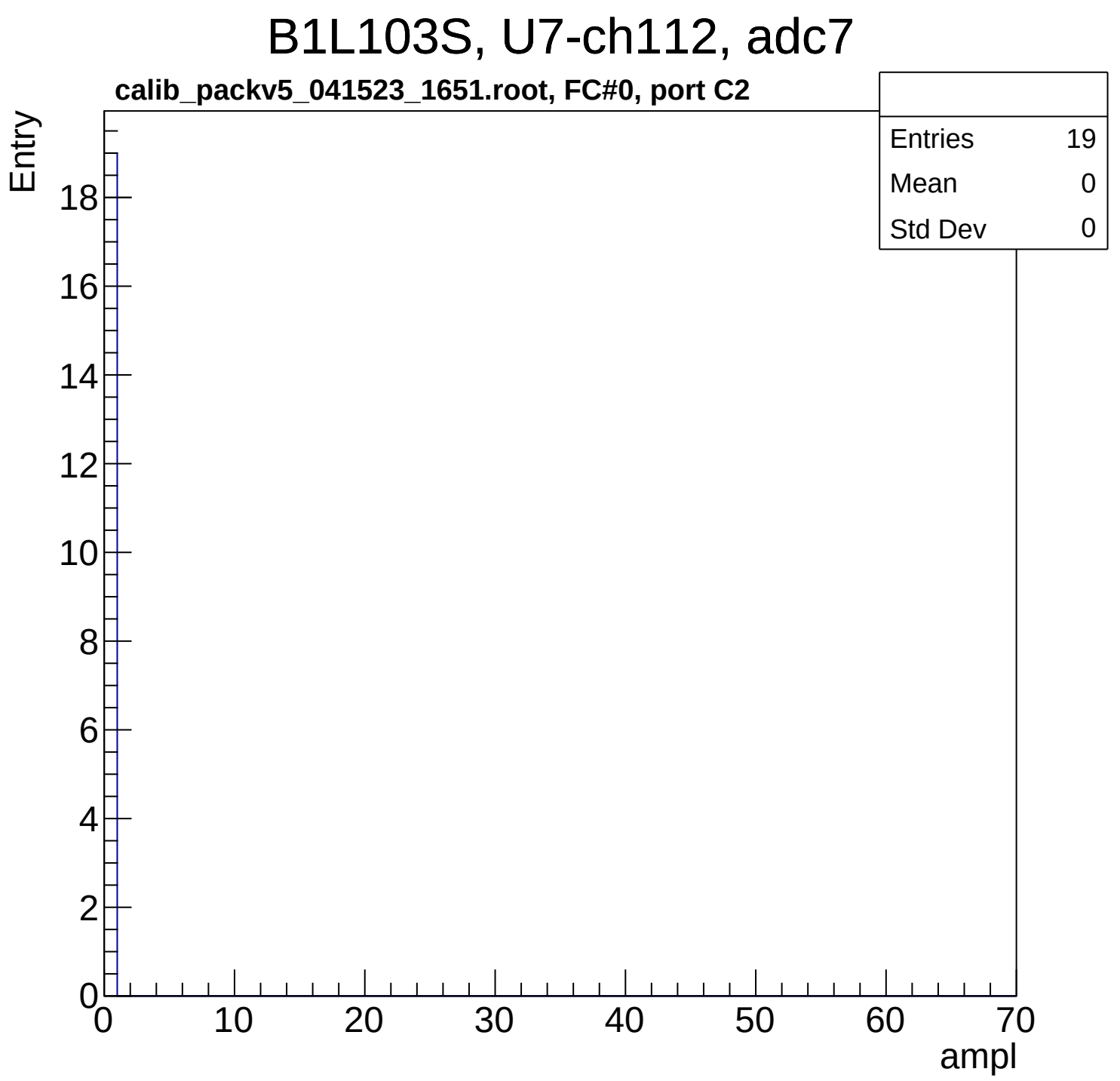
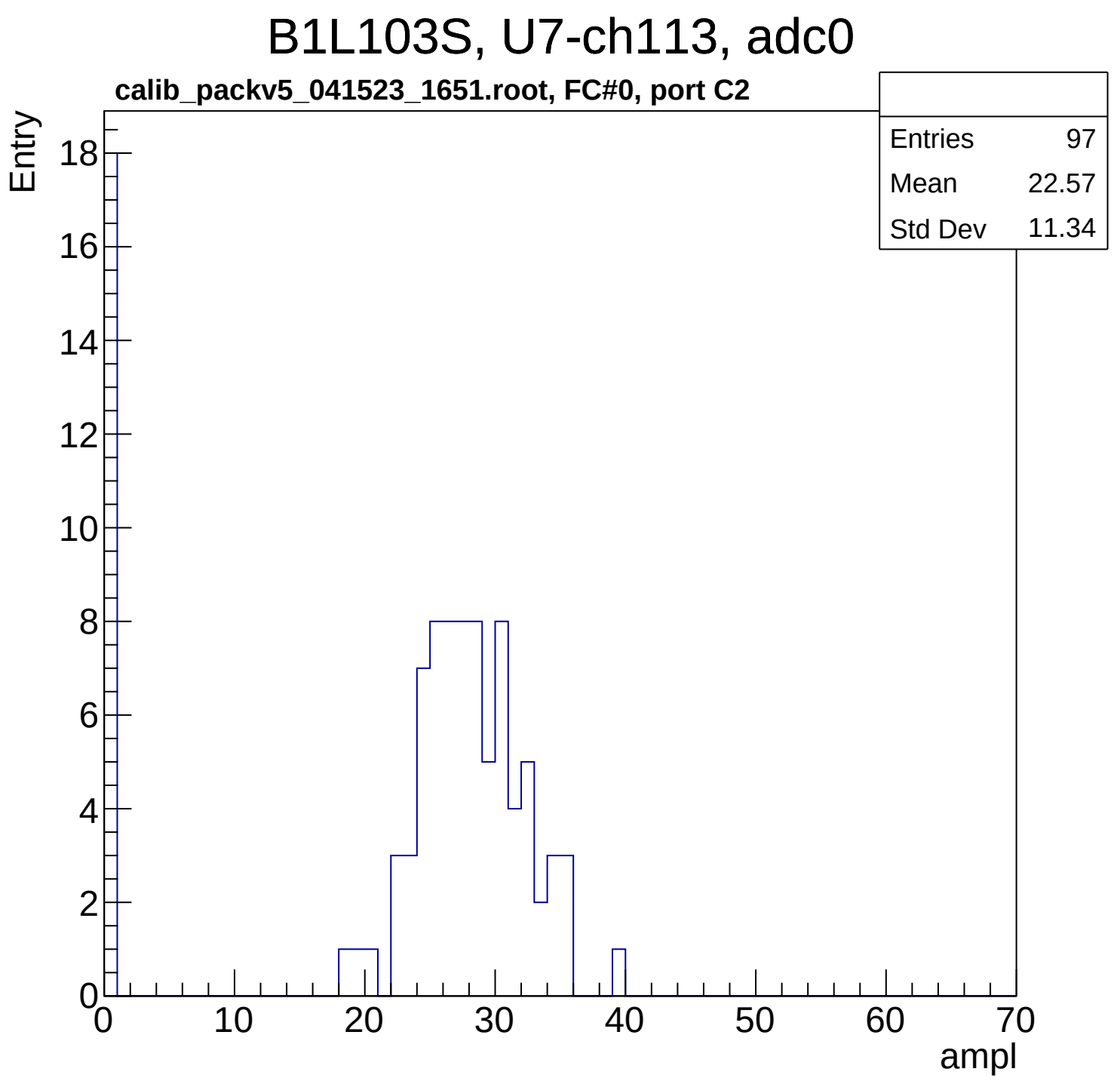
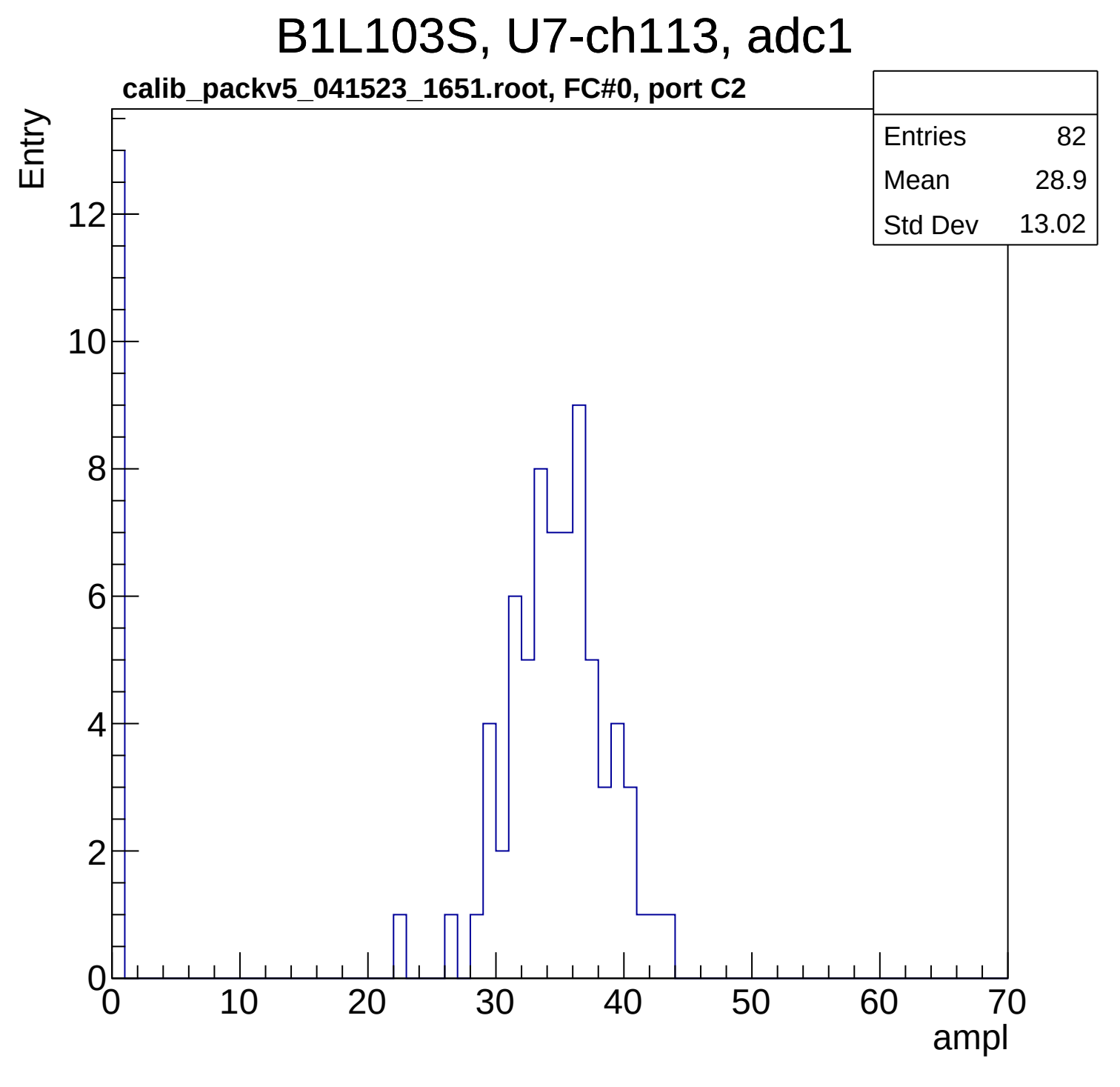
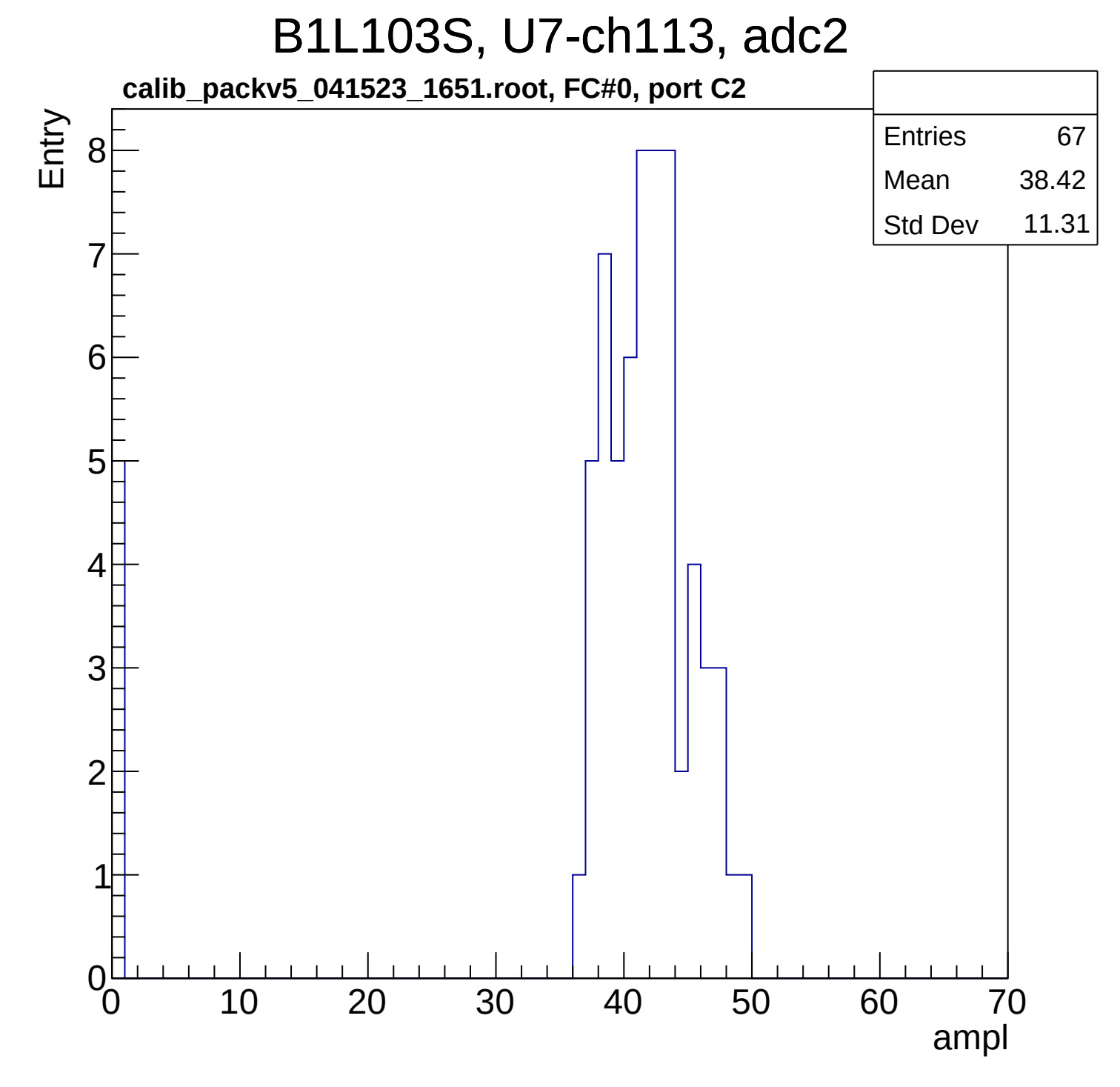

B1L103S, U7-ch112, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch113, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 97
Mean 22.57
Std Dev 11.34
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch113, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 28.9
Std Dev 13.02
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch113, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 38.42
Std Dev 11.31
Entry
ampl
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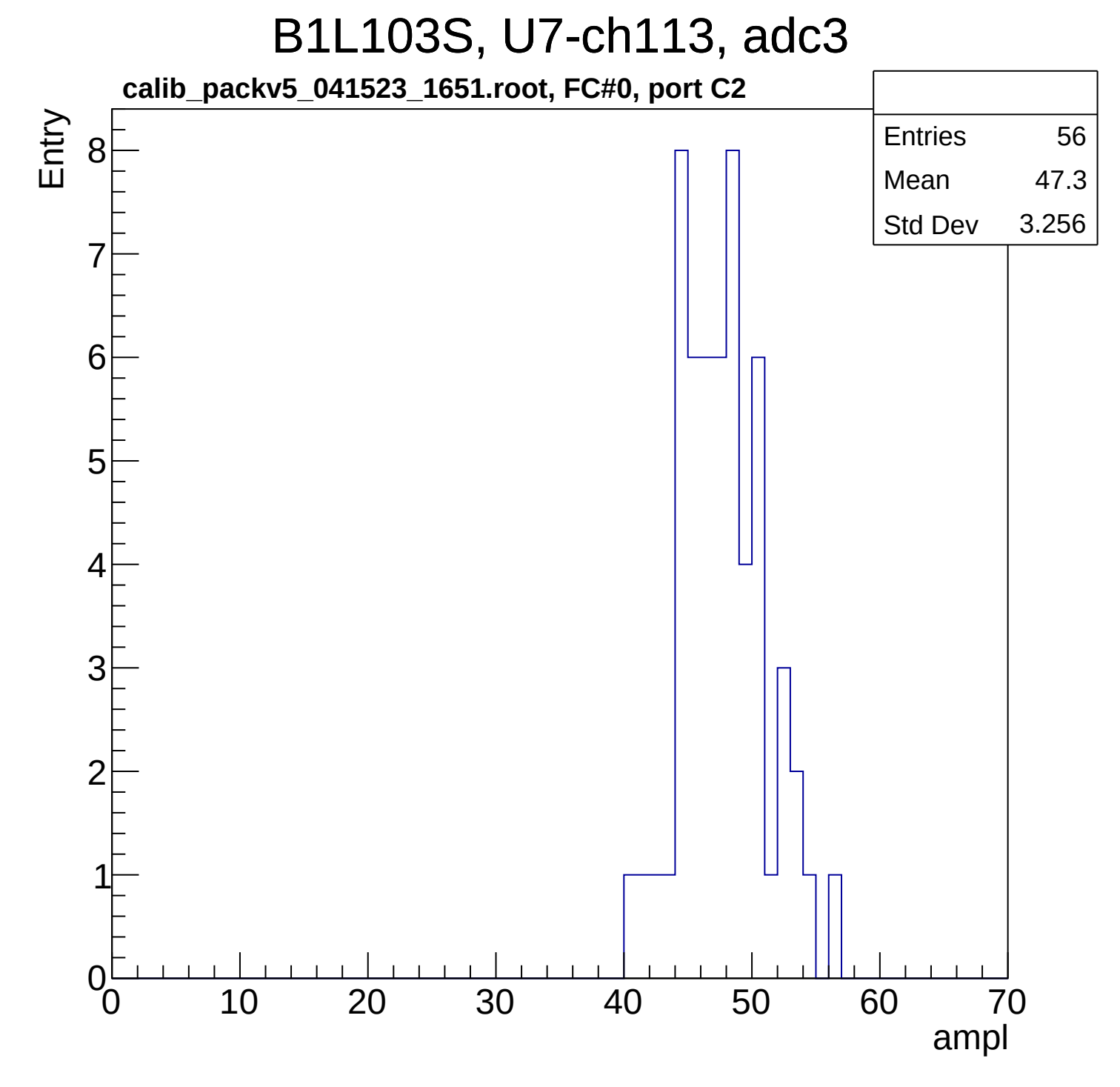
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch113, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 47.3
Std Dev 3.256
Entry
ampl
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1
2
3
4
5
6
7
8
0
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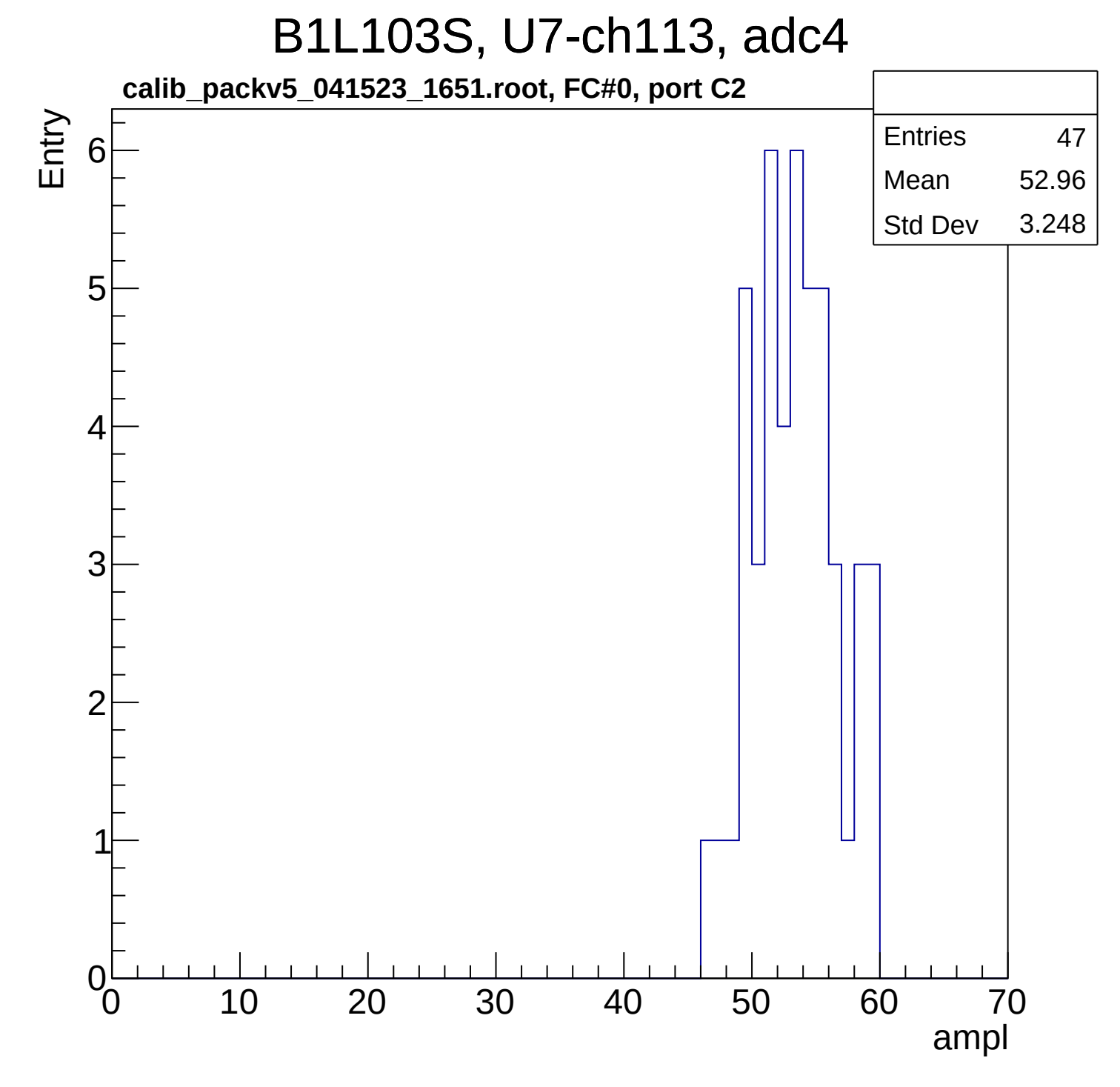
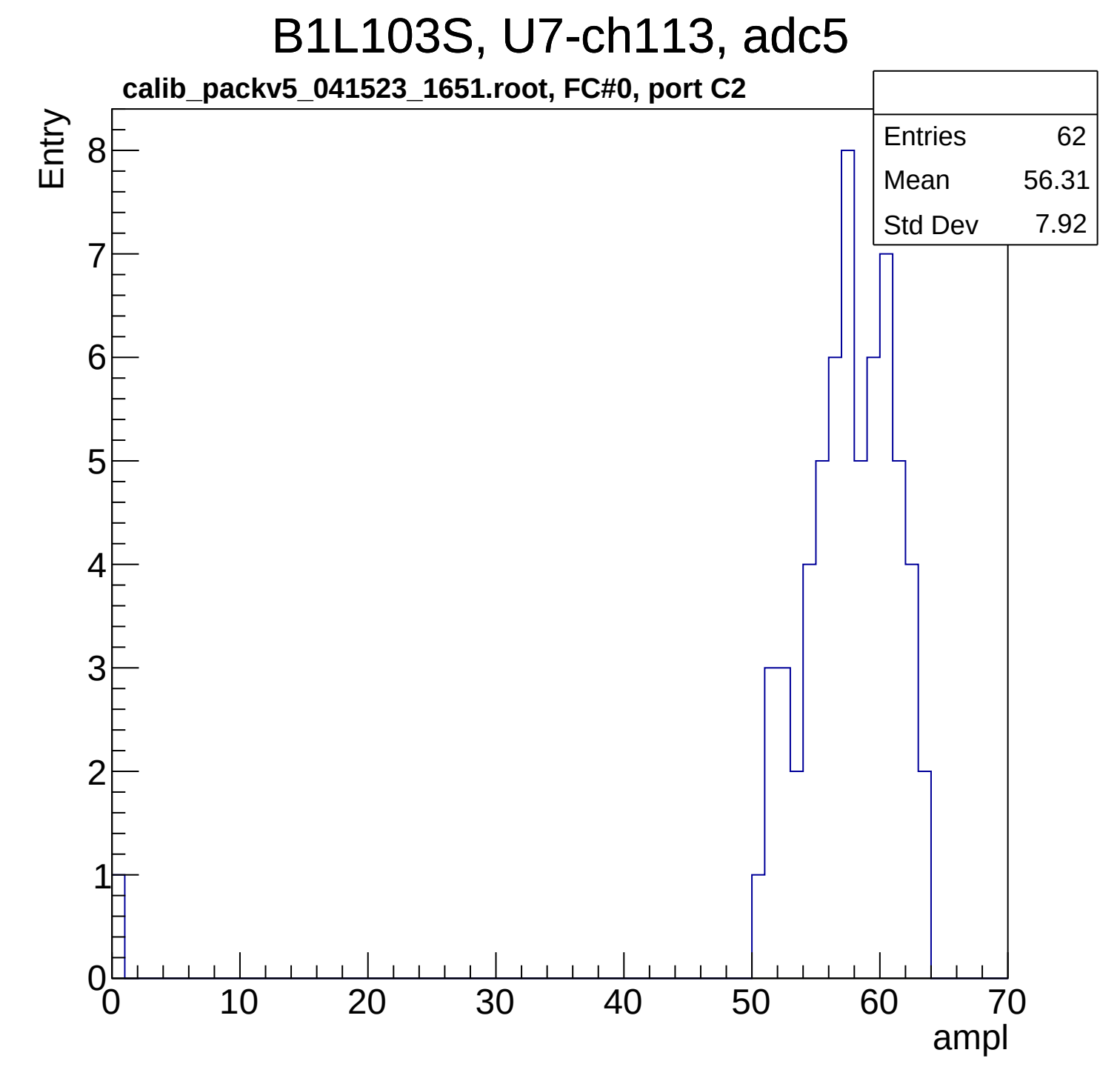
20
30
40
50
60
70


B1L103S, U7-ch113, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 52.96
Std Dev 3.248
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U7-ch113, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 56.31
Std Dev 7.92
Entry
ampl
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2
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4
5
6
7
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0
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60
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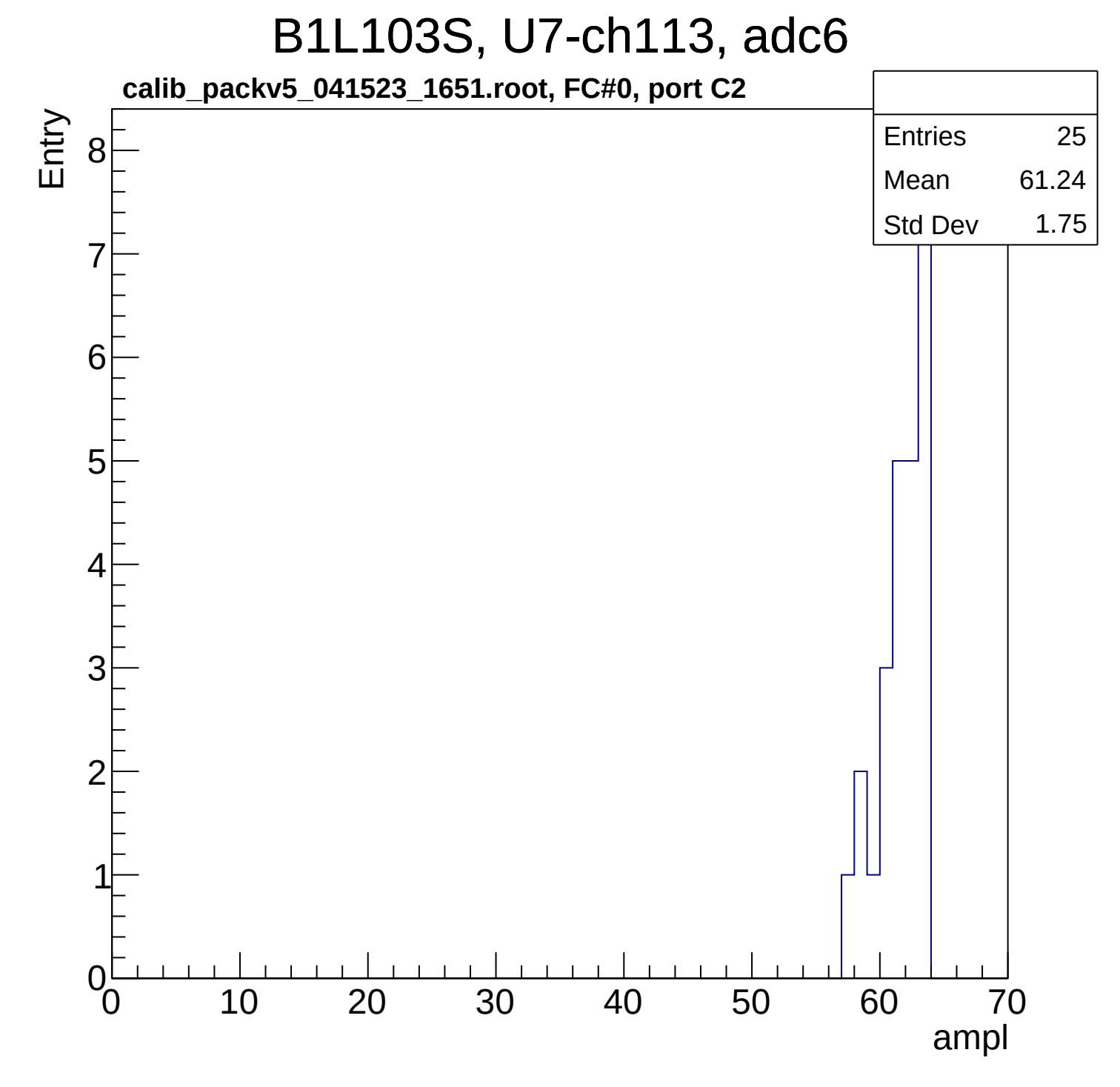
B1L103S, U7-ch113, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 25
Mean 61.24
Std Dev 1.75
Entry
ampl
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1
2
3
4
5
6
7
8
0
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60
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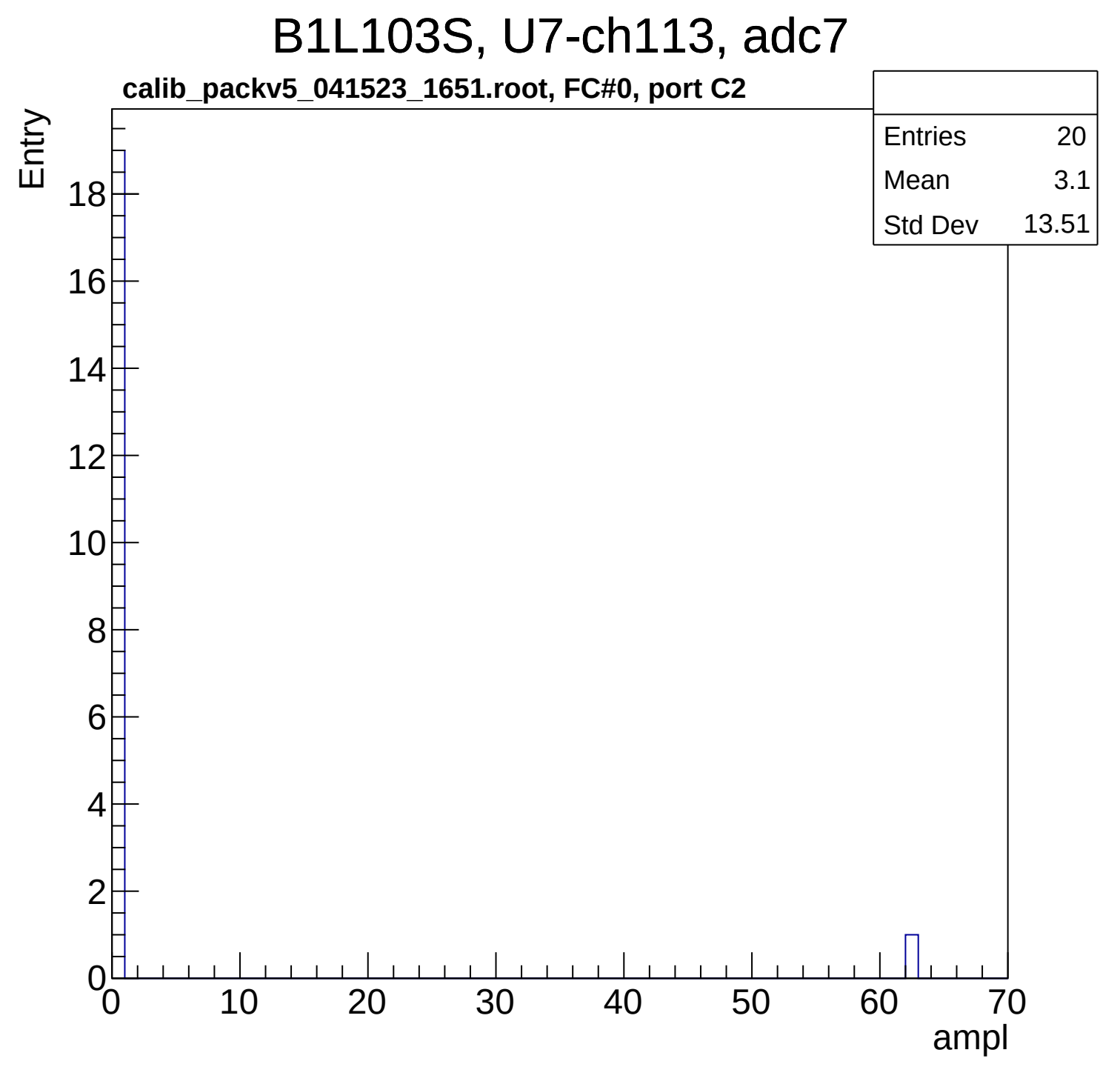
B1L103S, U7-ch113, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.1
Std Dev 13.51
Entry
0
2
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6
8
10
12
14
16
18
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10
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30
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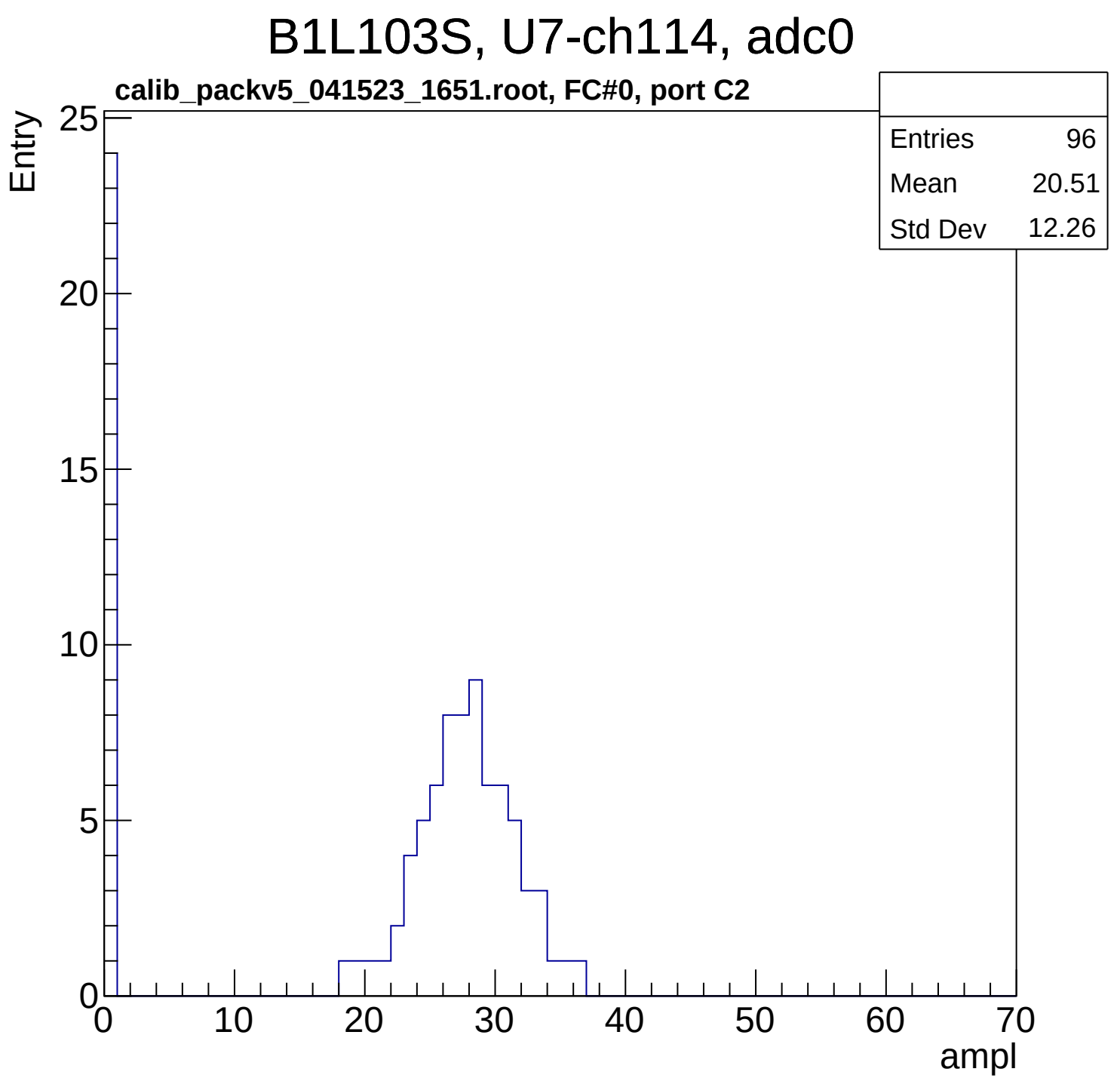
50
60
70
ampl


B1L103S, U7-ch114, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 96
Mean 20.51
Std Dev 12.26
Entry
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5
10
15
20
25
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10
20
30
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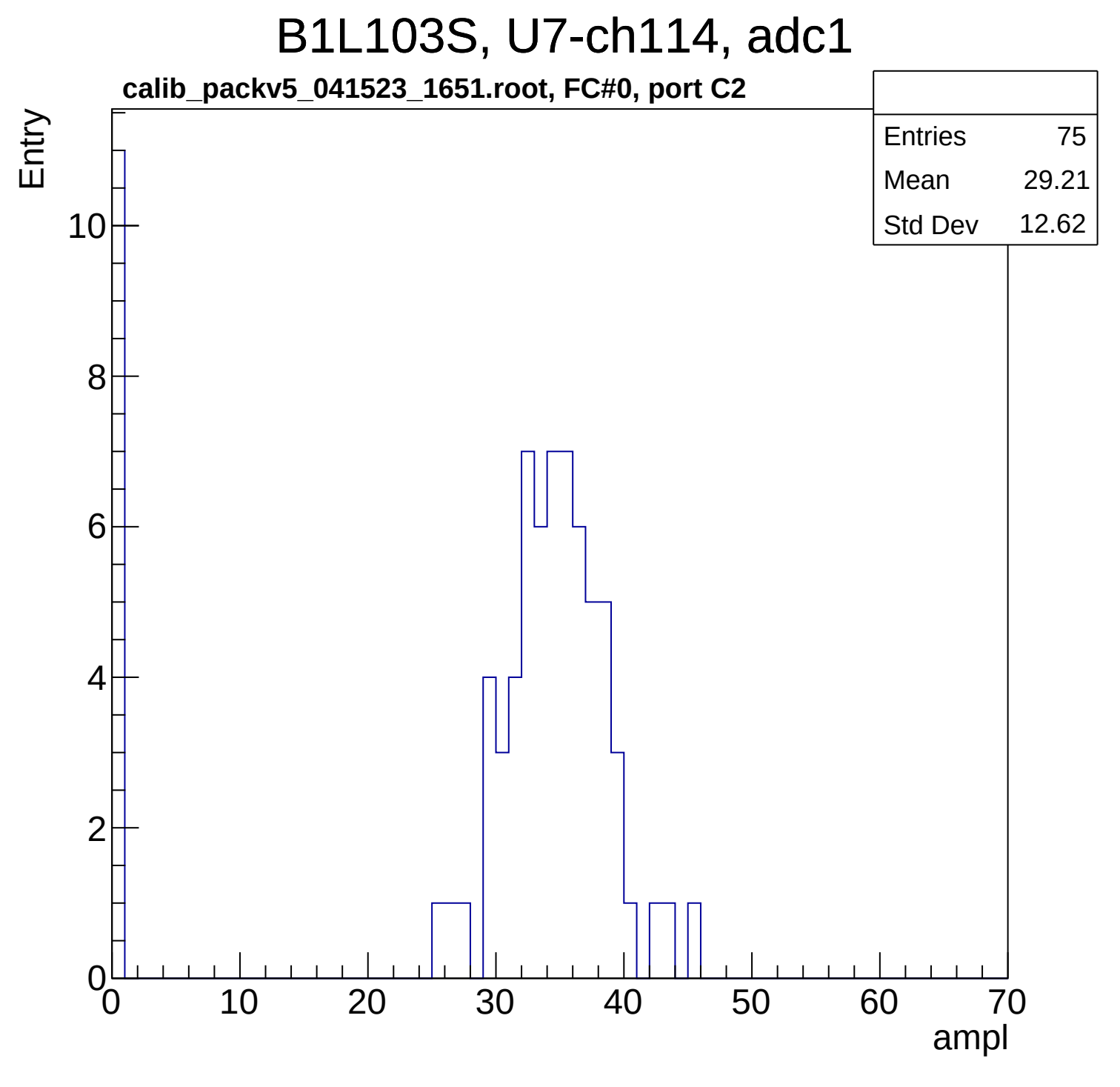
50
60
70
ampl


B1L103S, U7-ch114, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 29.21
Std Dev 12.62
Entry
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2
4
6
8
10
0
10
20
30
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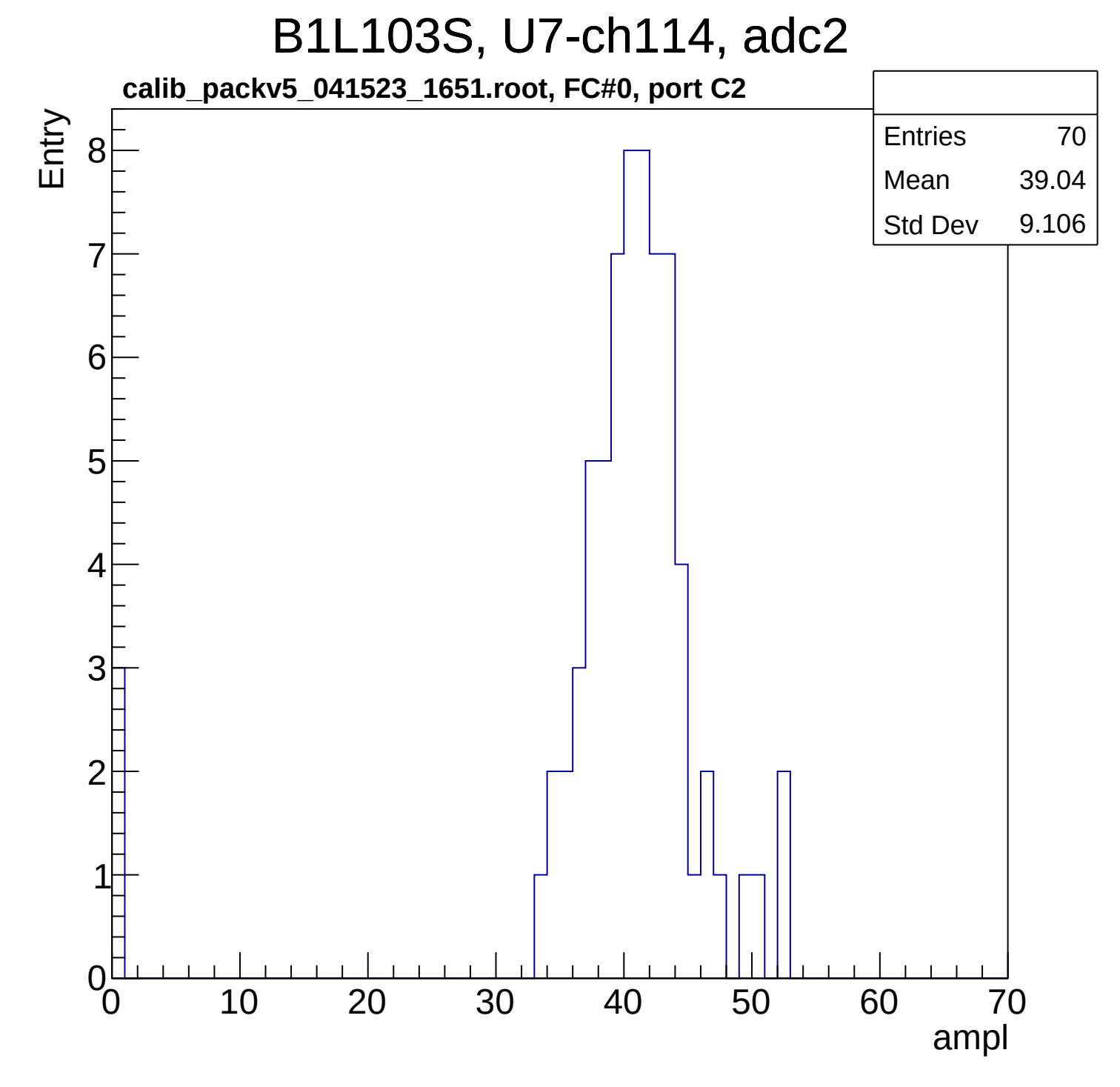
50
60
70
ampl


B1L103S, U7-ch114, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 39.04
Std Dev 9.106
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
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40
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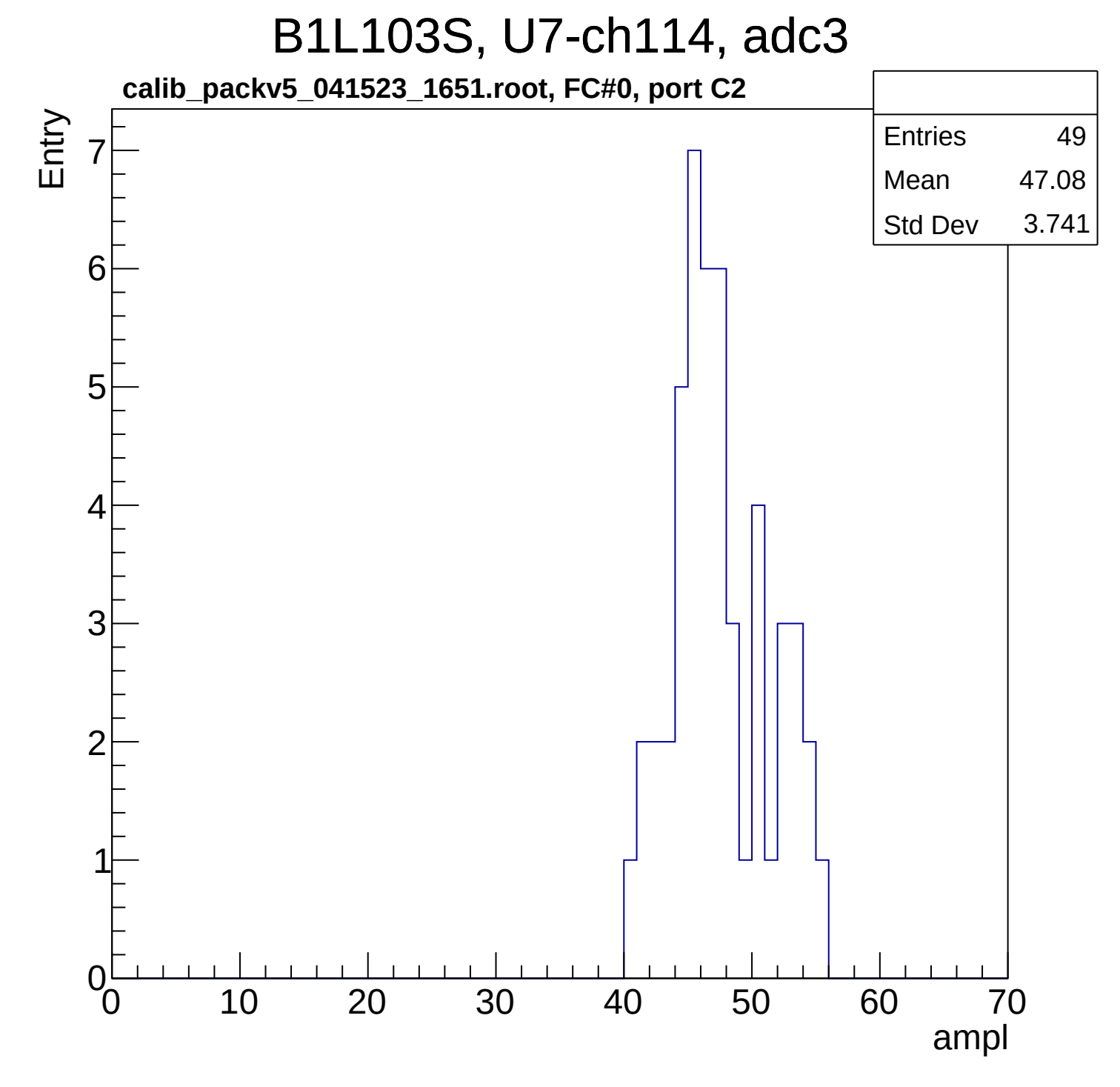
60
70


B1L103S, U7-ch114, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 47.08
Std Dev 3.741
Entry
ampl
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2
3
4
5
6
7
0
10
20
30
40
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60
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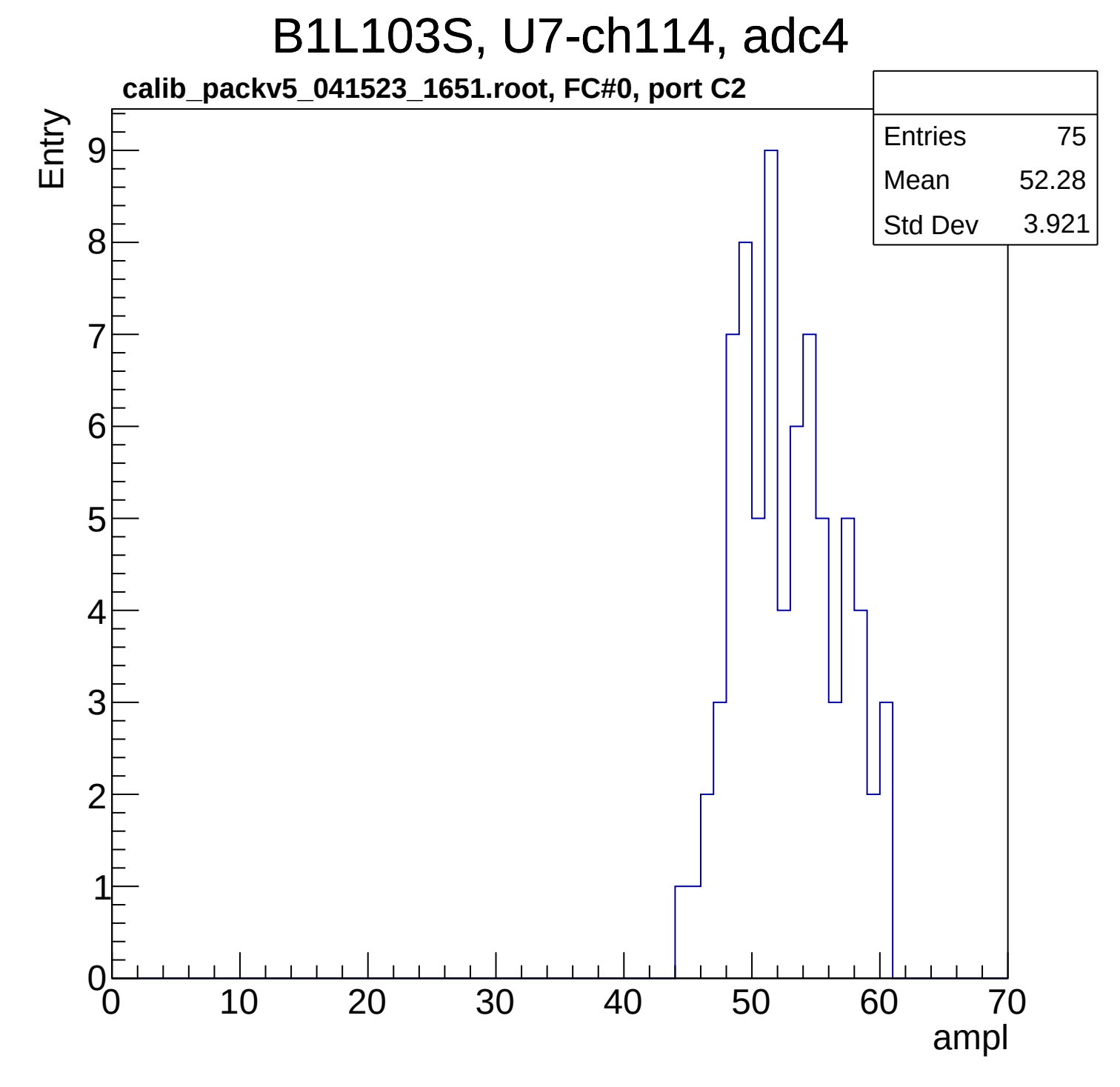
B1L103S, U7-ch114, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 52.28
Std Dev 3.921
Entry
ampl
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3
4
5
6
7
8
9
0
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60
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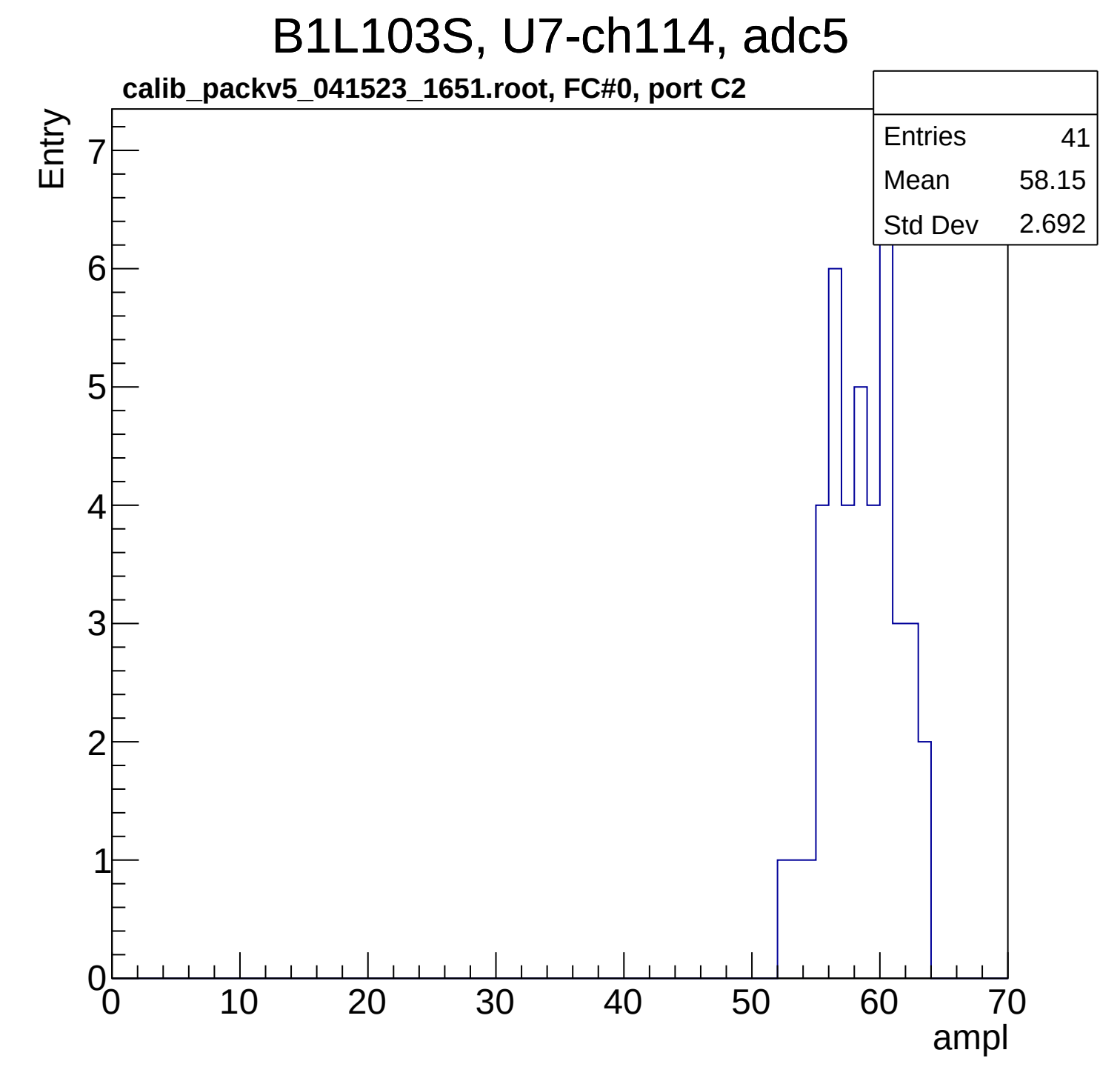
B1L103S, U7-ch114, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 41
Mean 58.15
Std Dev 2.692
Entry
ampl
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1
2
3
4
5
6
7
0
10
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60
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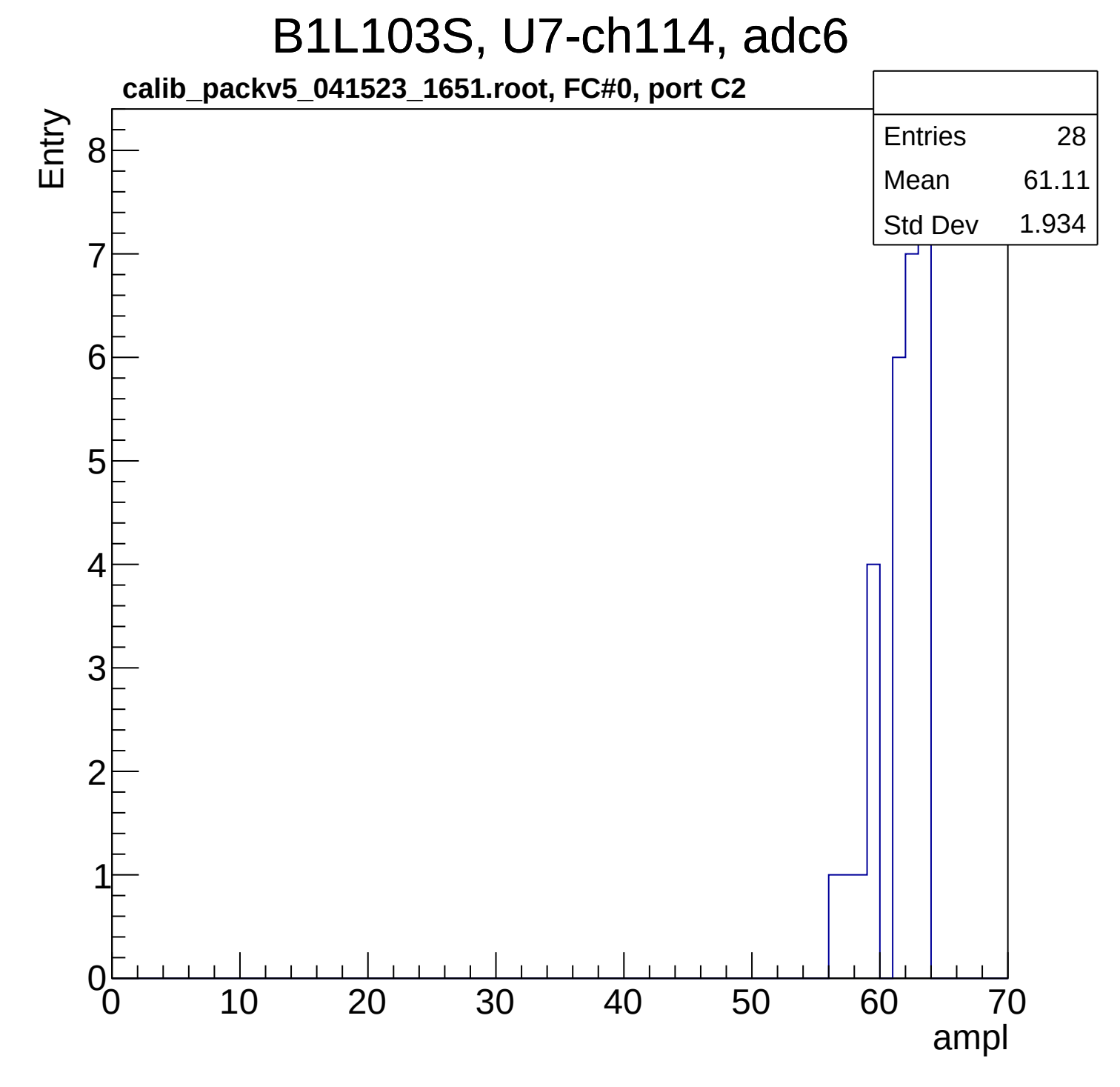
B1L103S, U7-ch114, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 28
Mean 61.11
Std Dev 1.934
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
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60
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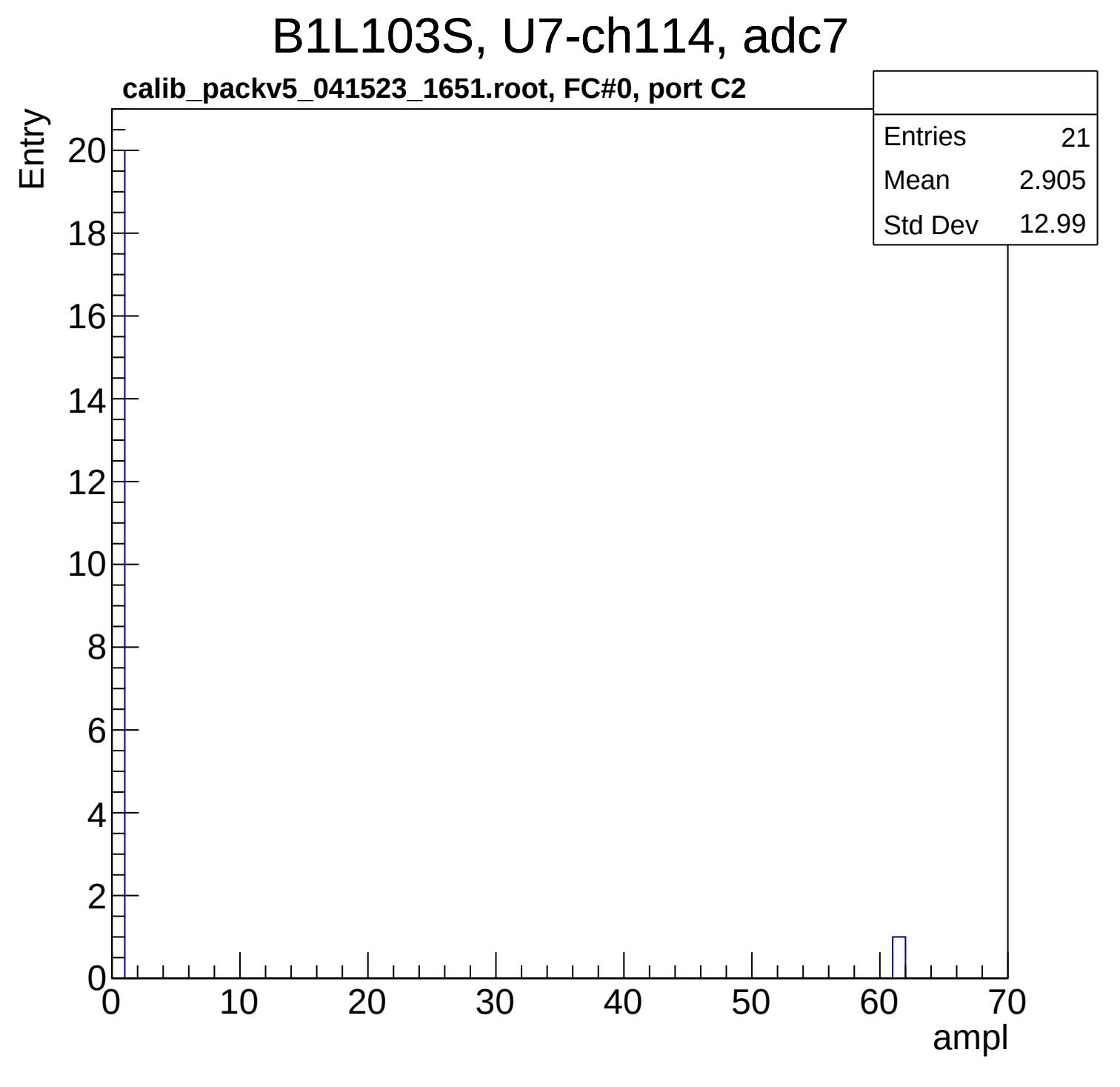
B1L103S, U7-ch114, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 2.905
Std Dev 12.99
Entry
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8
10
12
14
16
18
20
0
10
20
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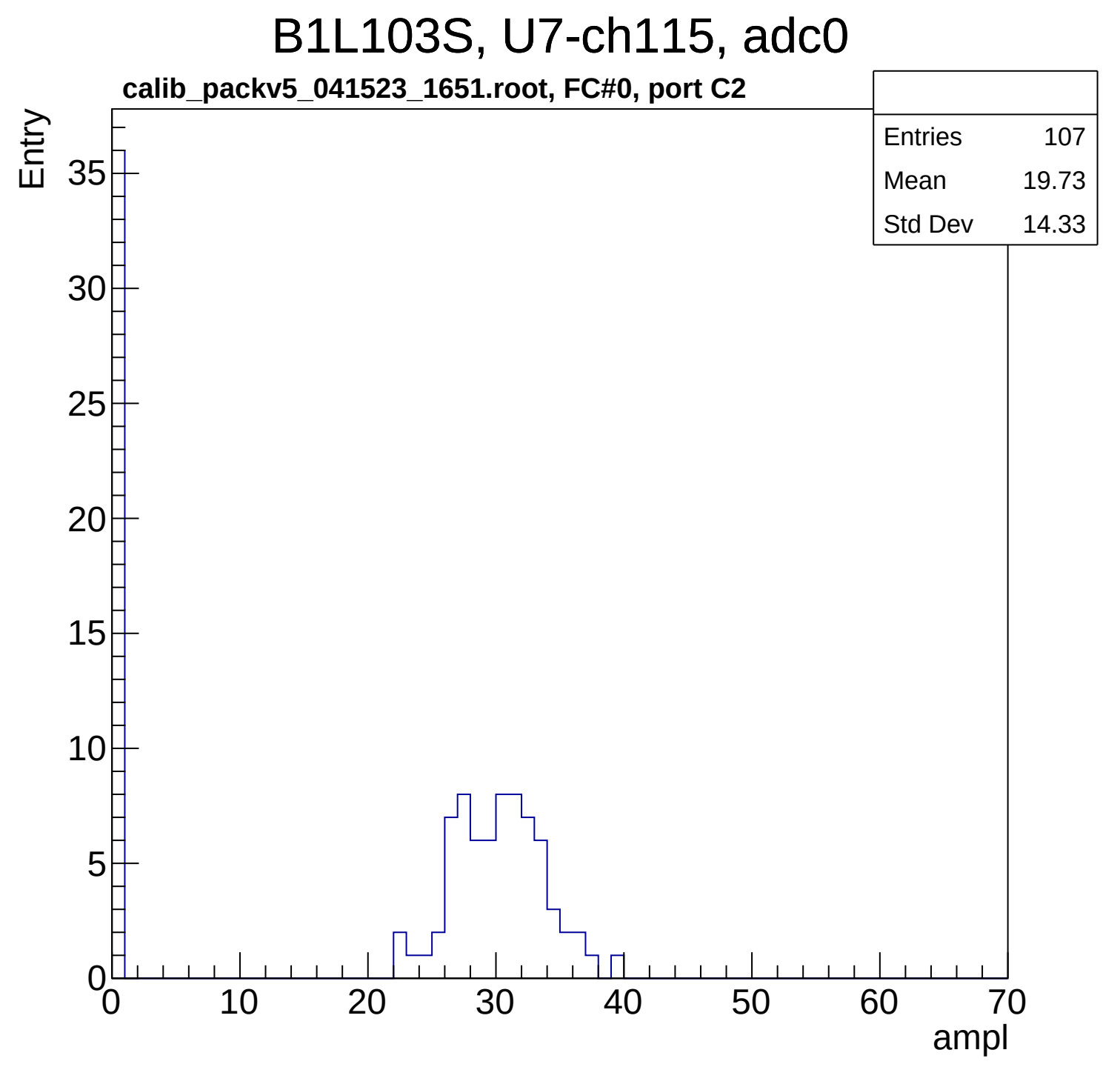
50
60
70
ampl


B1L103S, U7-ch115, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 107
Mean 19.73
Std Dev 14.33
Entry
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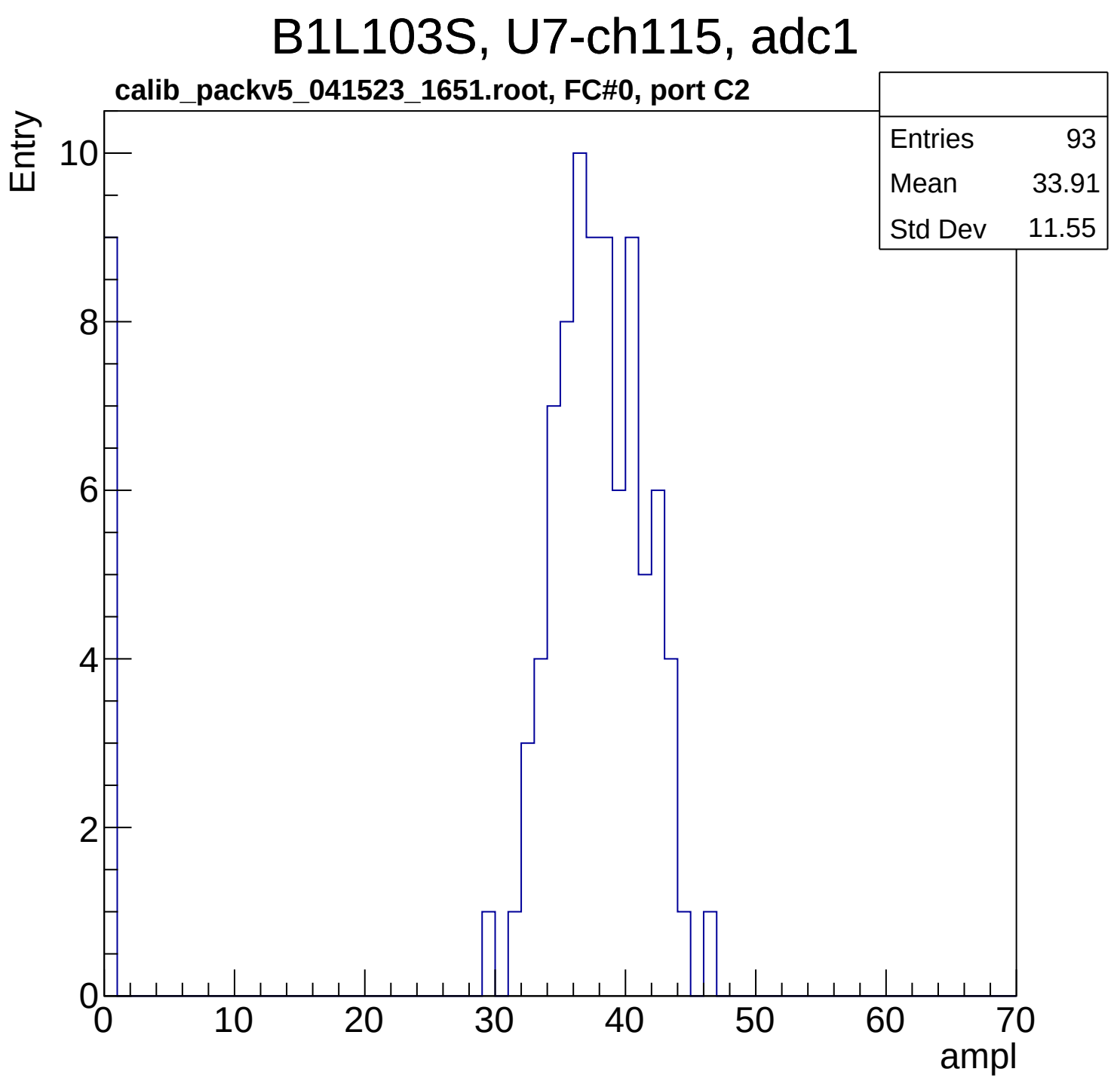
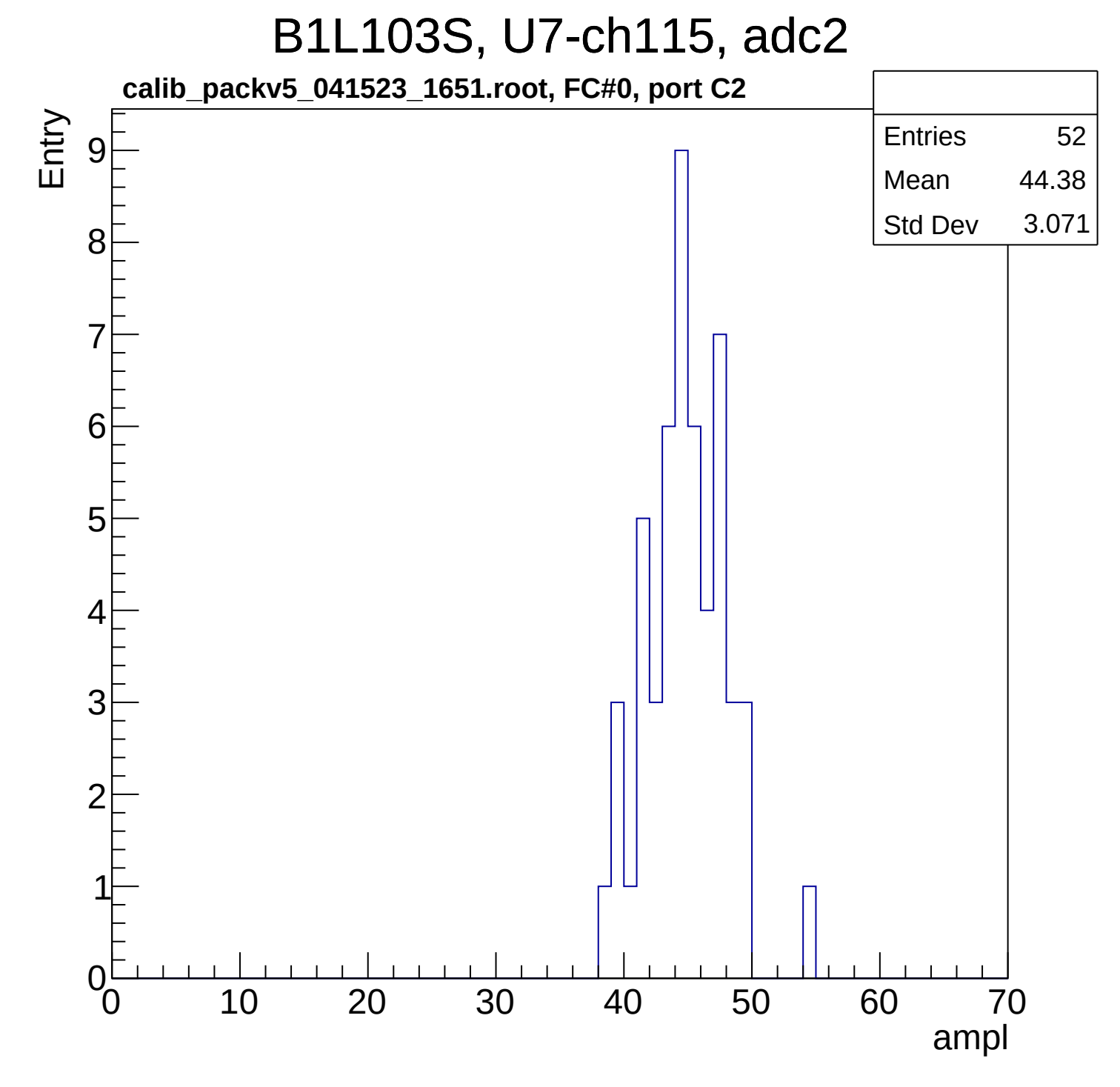
10
15
20
25
30
35
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch115, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 93
Mean 33.91
Std Dev 11.55
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U7-ch115, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 44.38
Std Dev 3.071
Entry
ampl
0
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2
3
4
5
6
7
8
9
0
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20
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40
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60
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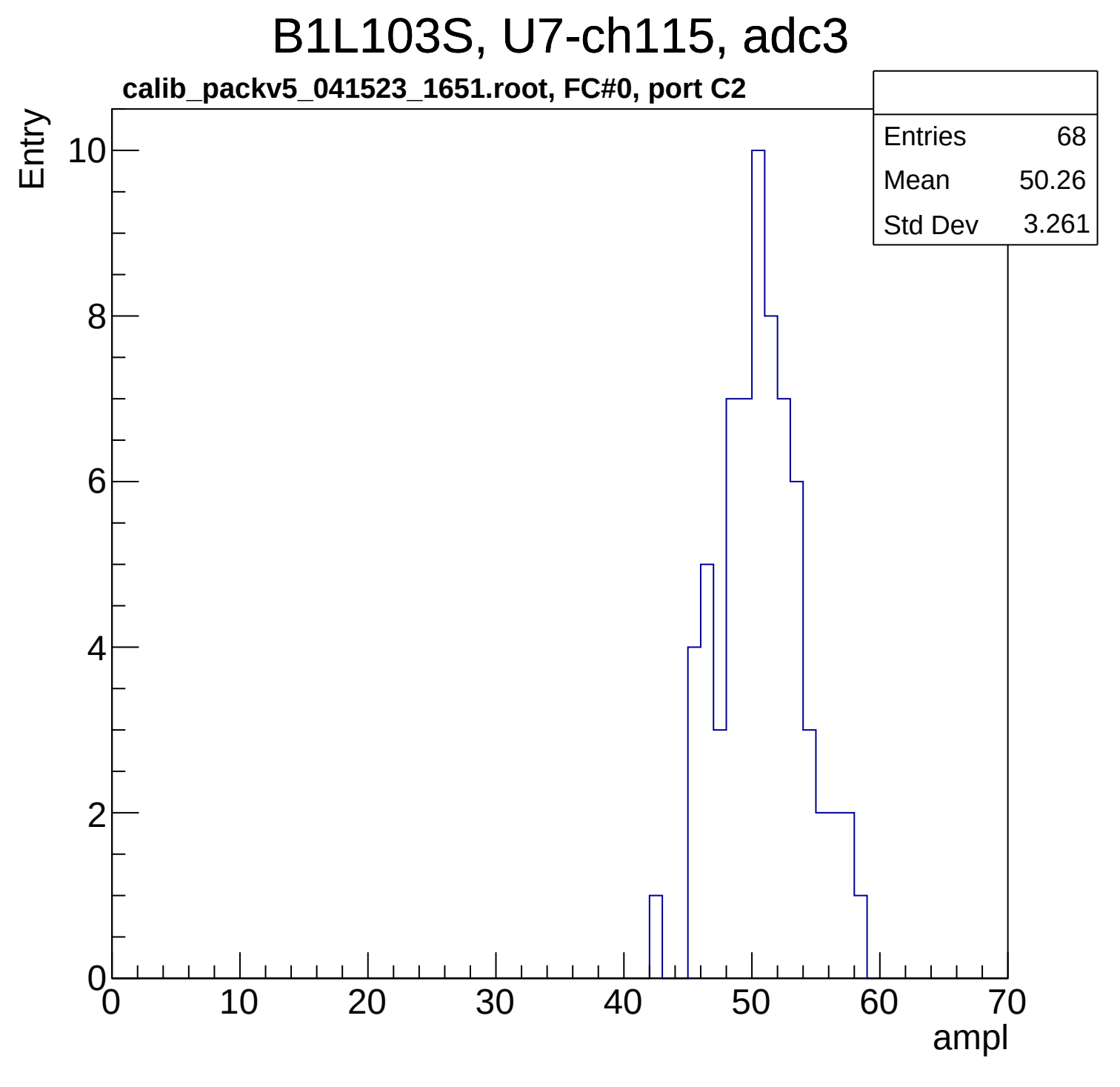
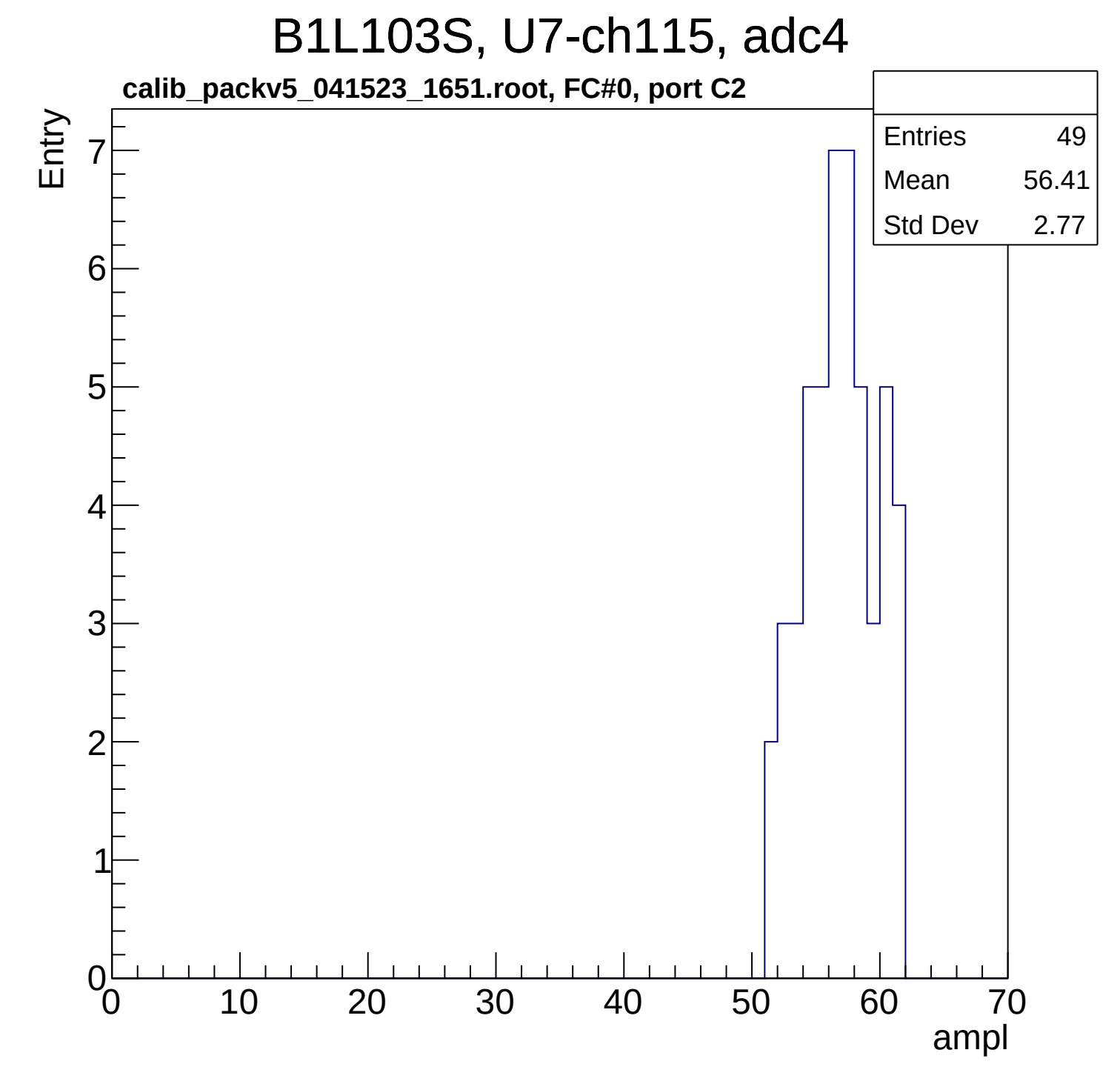
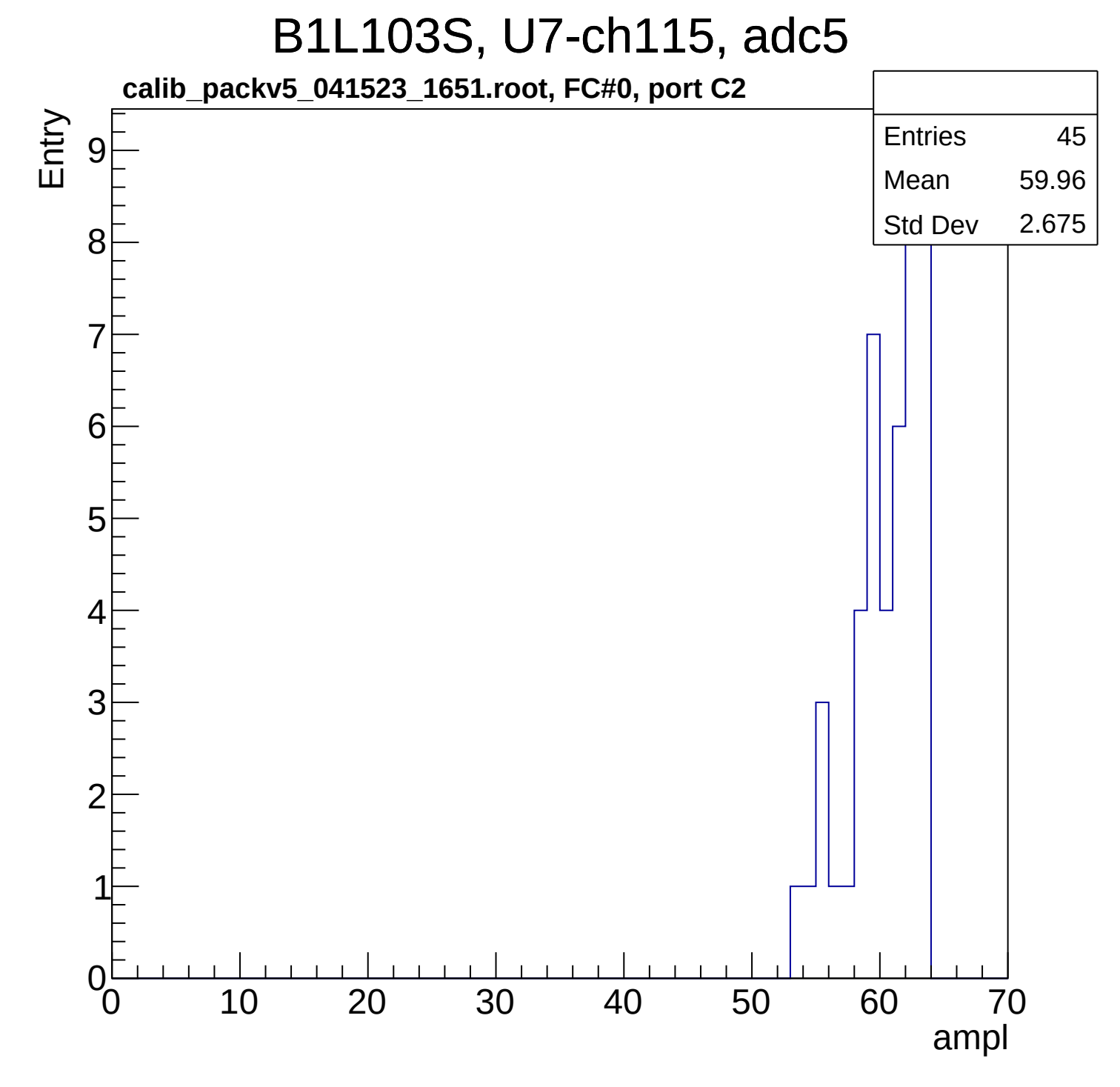

B1L103S, U7-ch115, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 50.26
Std Dev 3.261
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U7-ch115, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 56.41
Std Dev 2.77
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U7-ch115, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 59.96
Std Dev 2.675
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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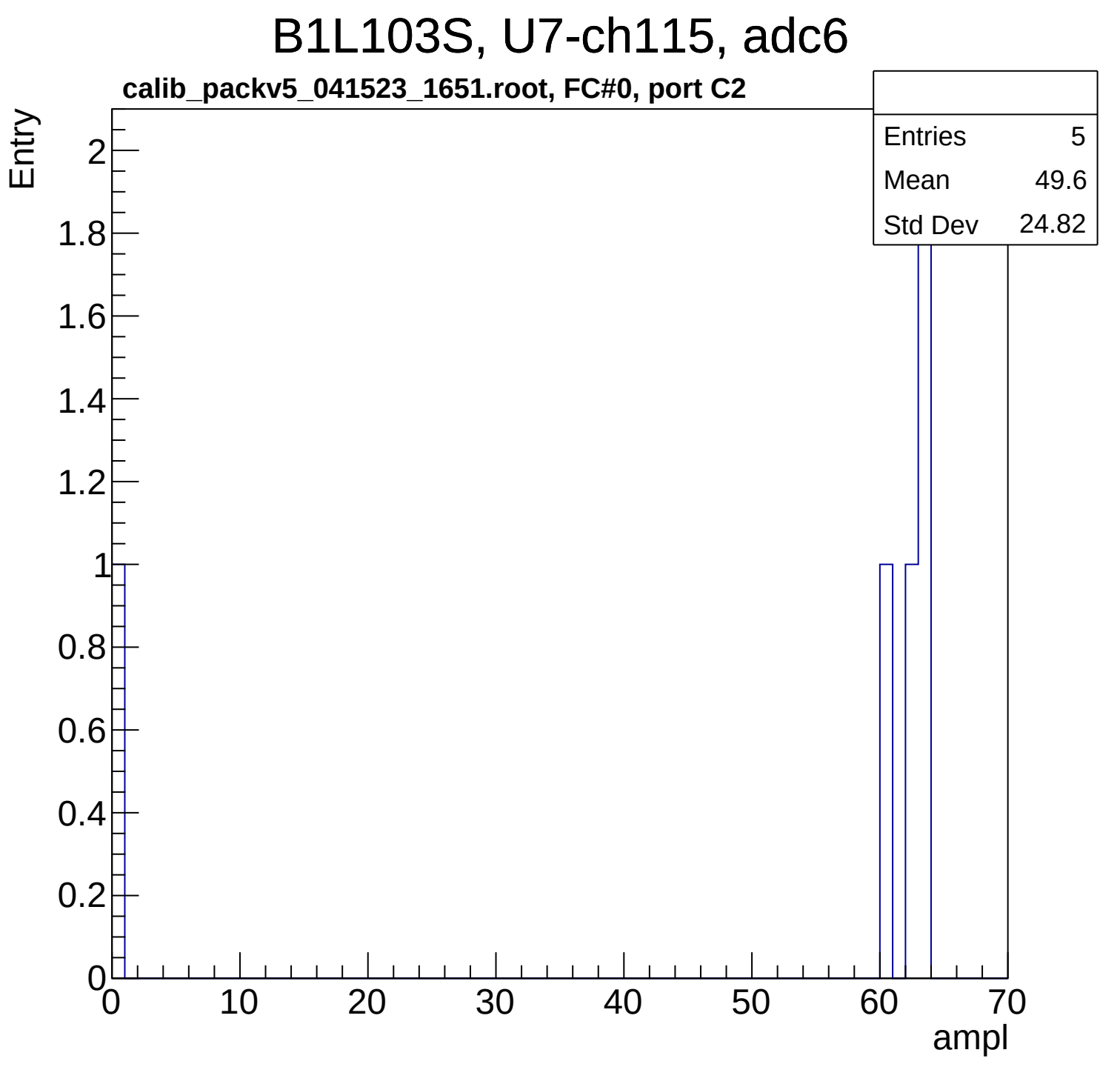
B1L103S, U7-ch115, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 5
Mean 49.6
Std Dev 24.82
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
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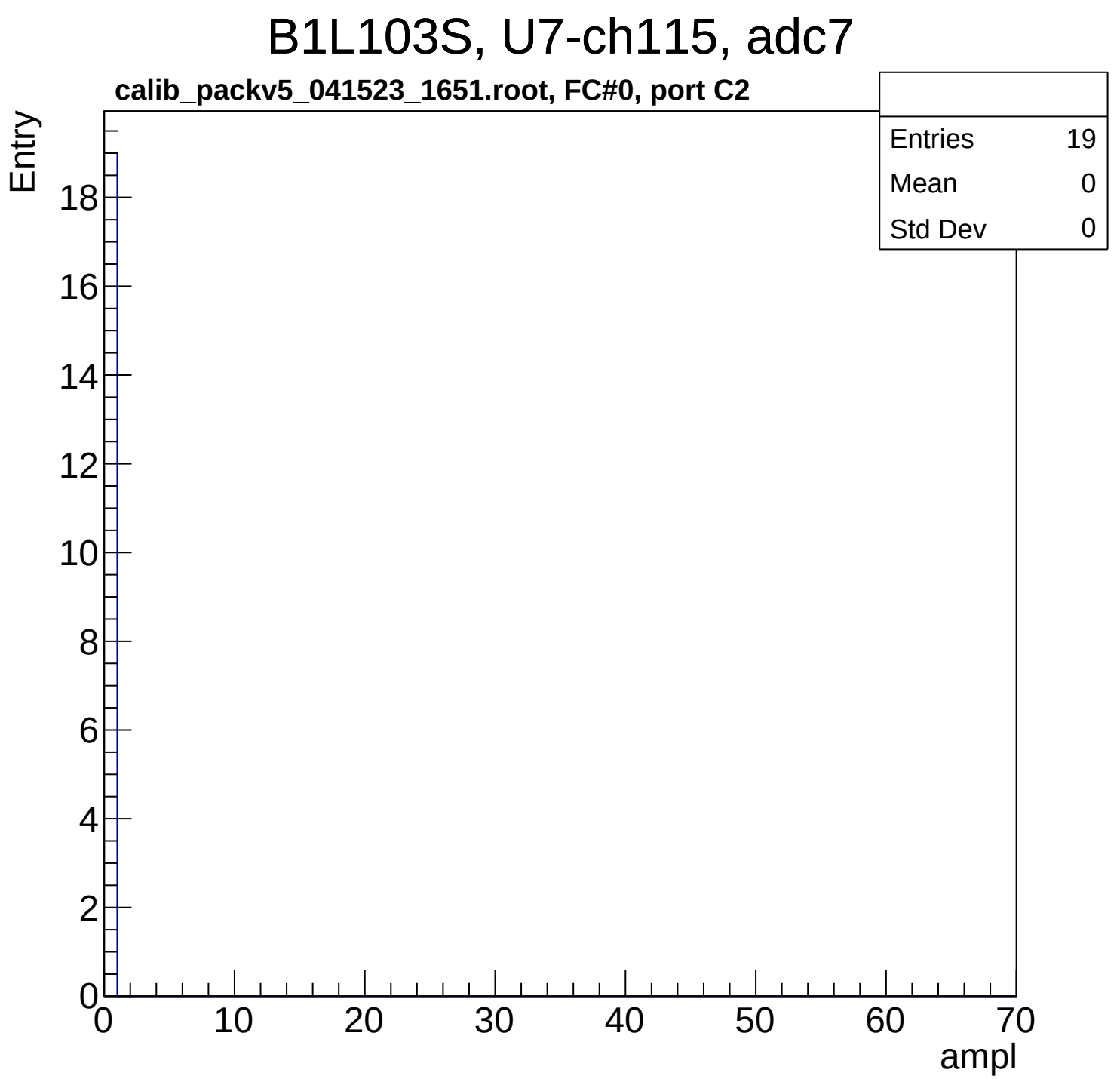
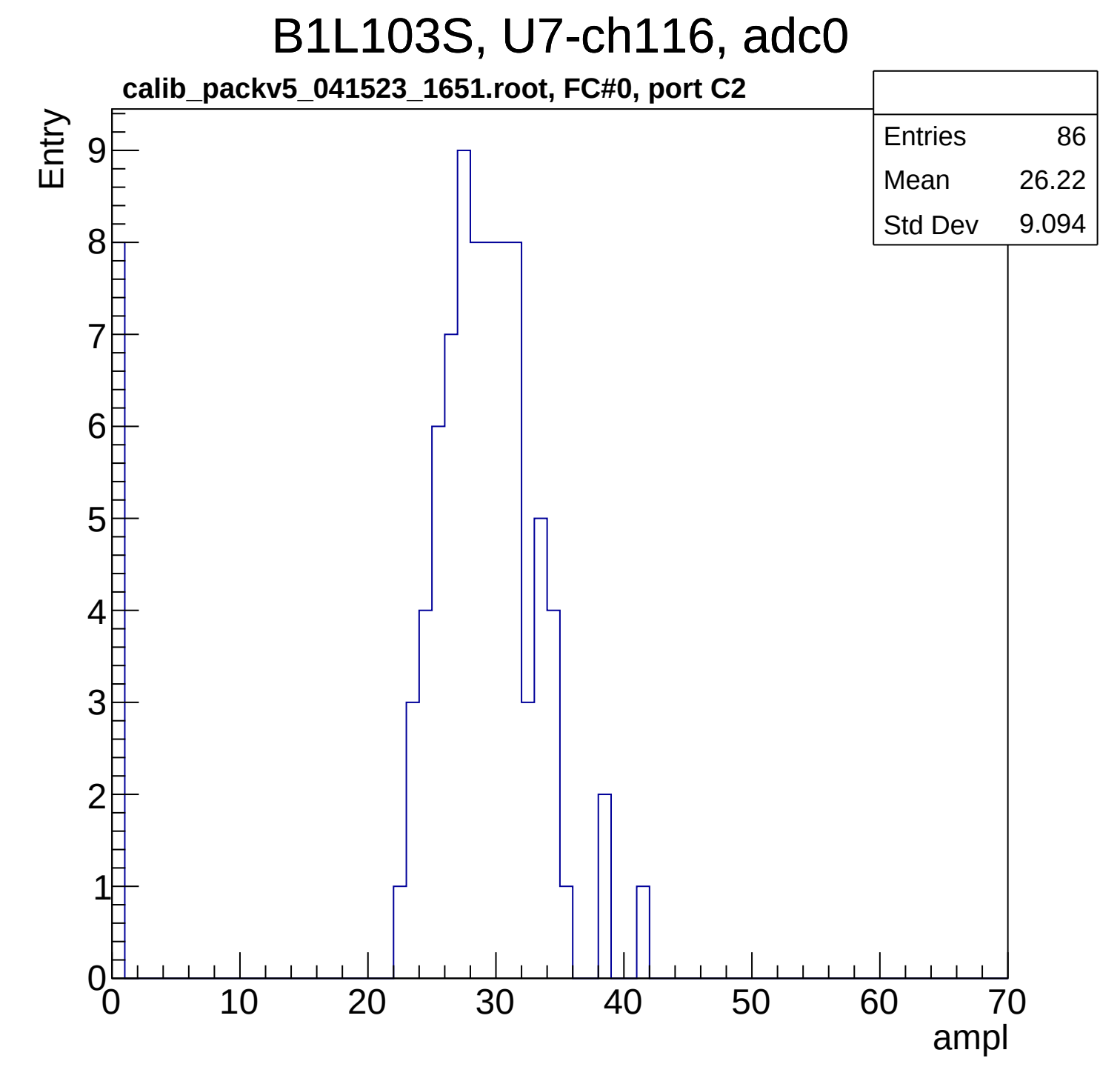

B1L103S, U7-ch115, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch116, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 26.22
Std Dev 9.094
Entry
ampl
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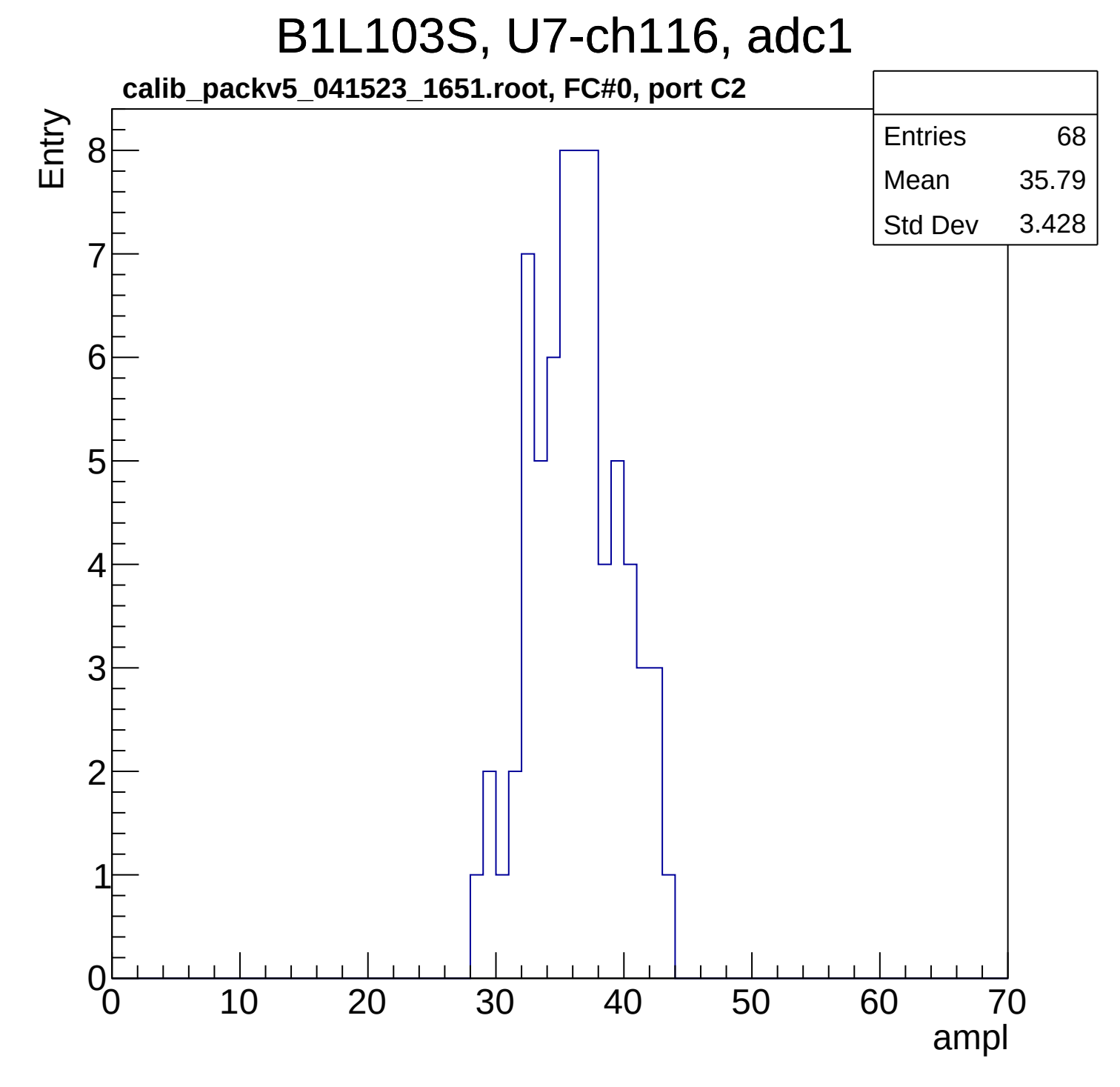
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U7-ch116, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 35.79
Std Dev 3.428
Entry
ampl
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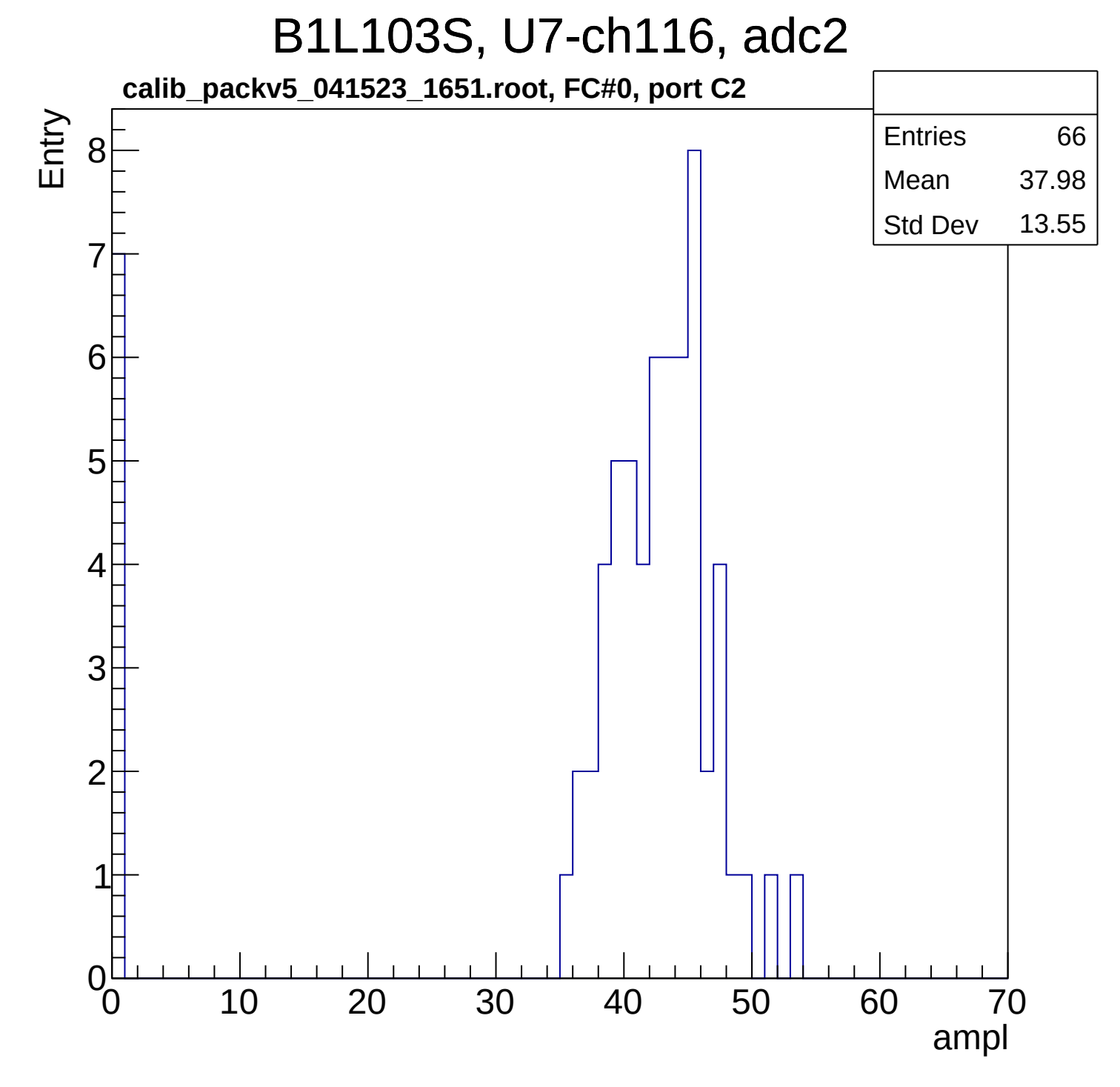
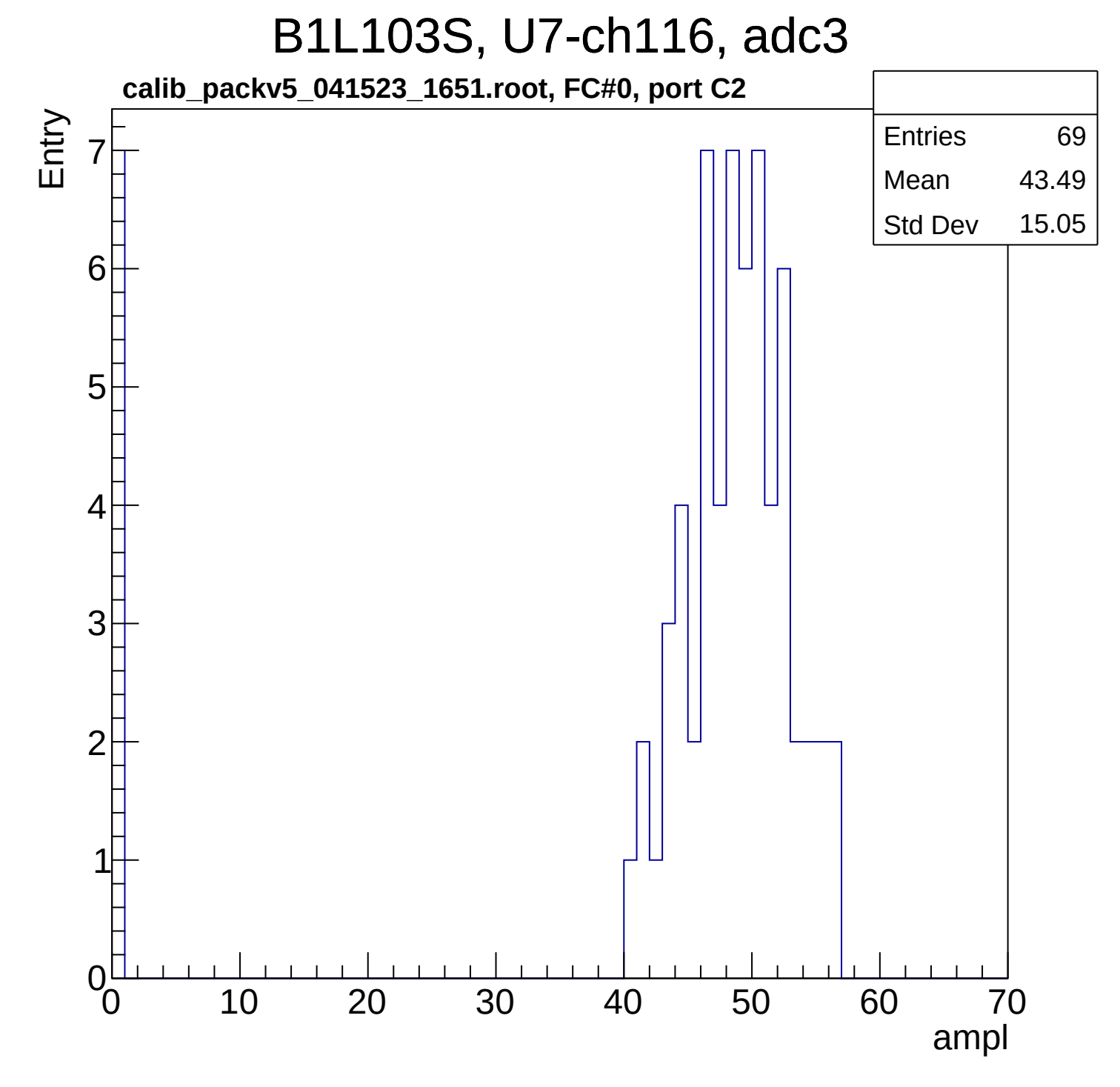
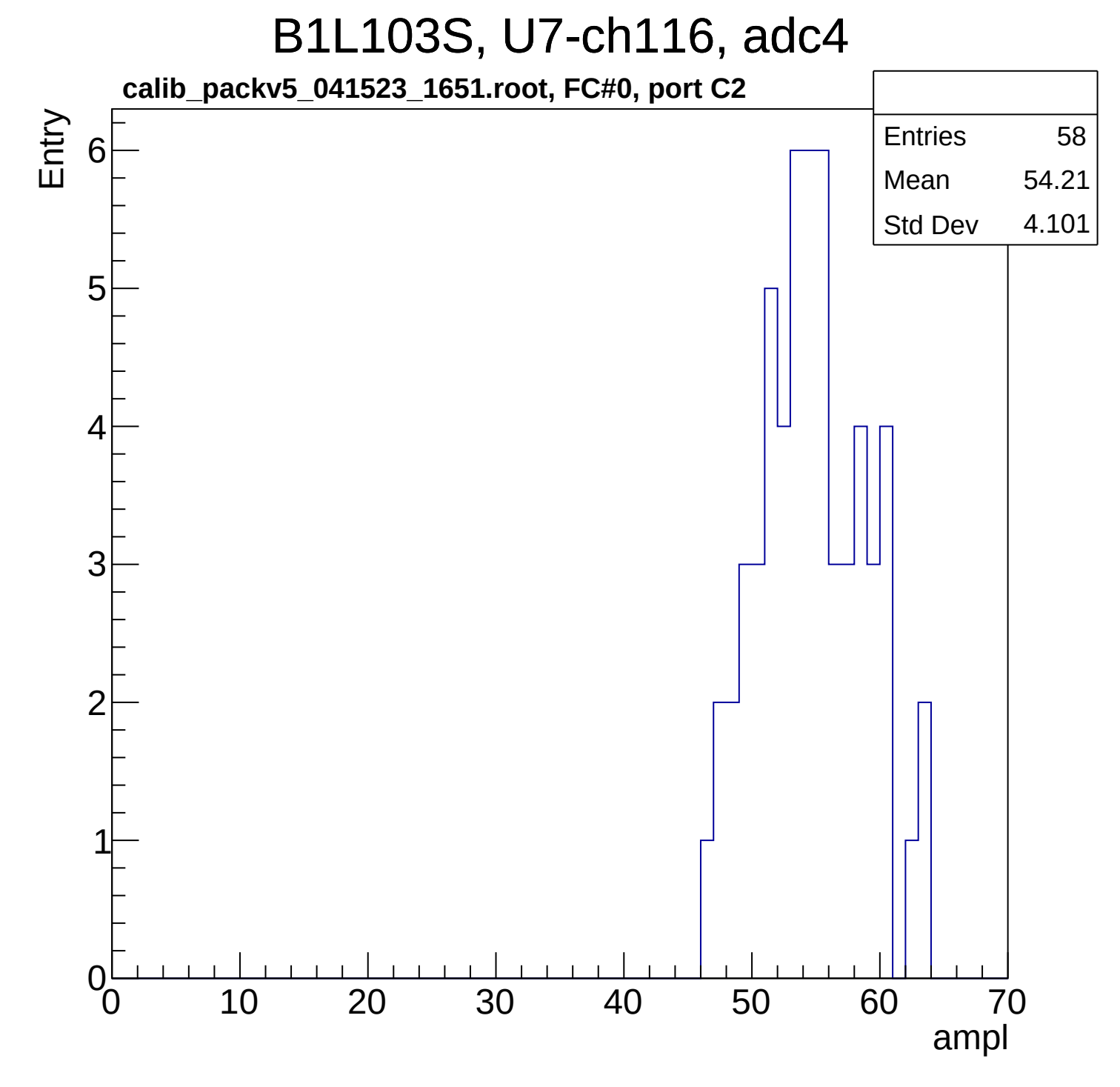
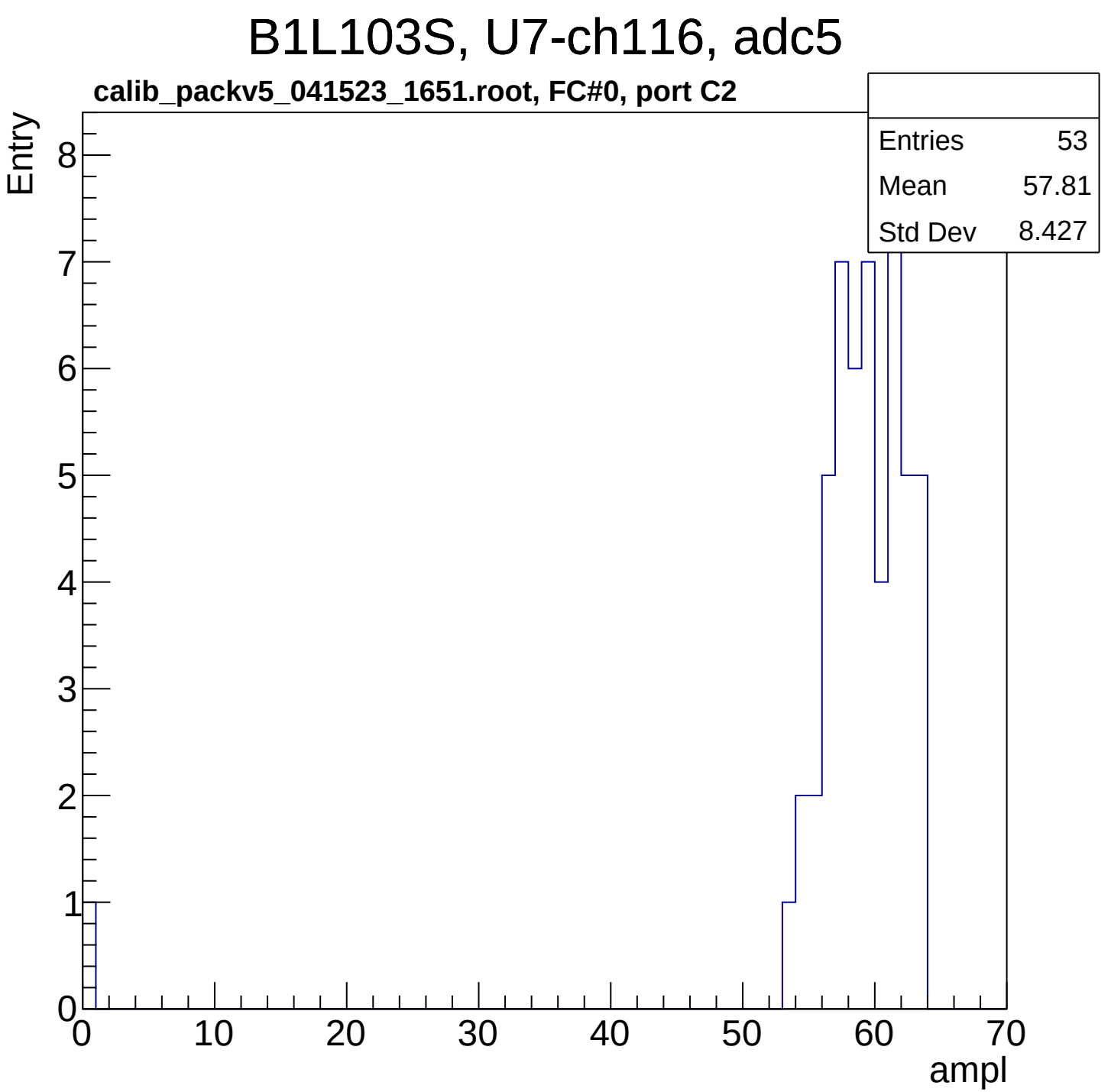
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch116, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 37.98
Std Dev 13.55
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch116, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 43.49
Std Dev 15.05
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U7-ch116, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 54.21
Std Dev 4.101
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U7-ch116, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 57.81
Std Dev 8.427
Entry
ampl
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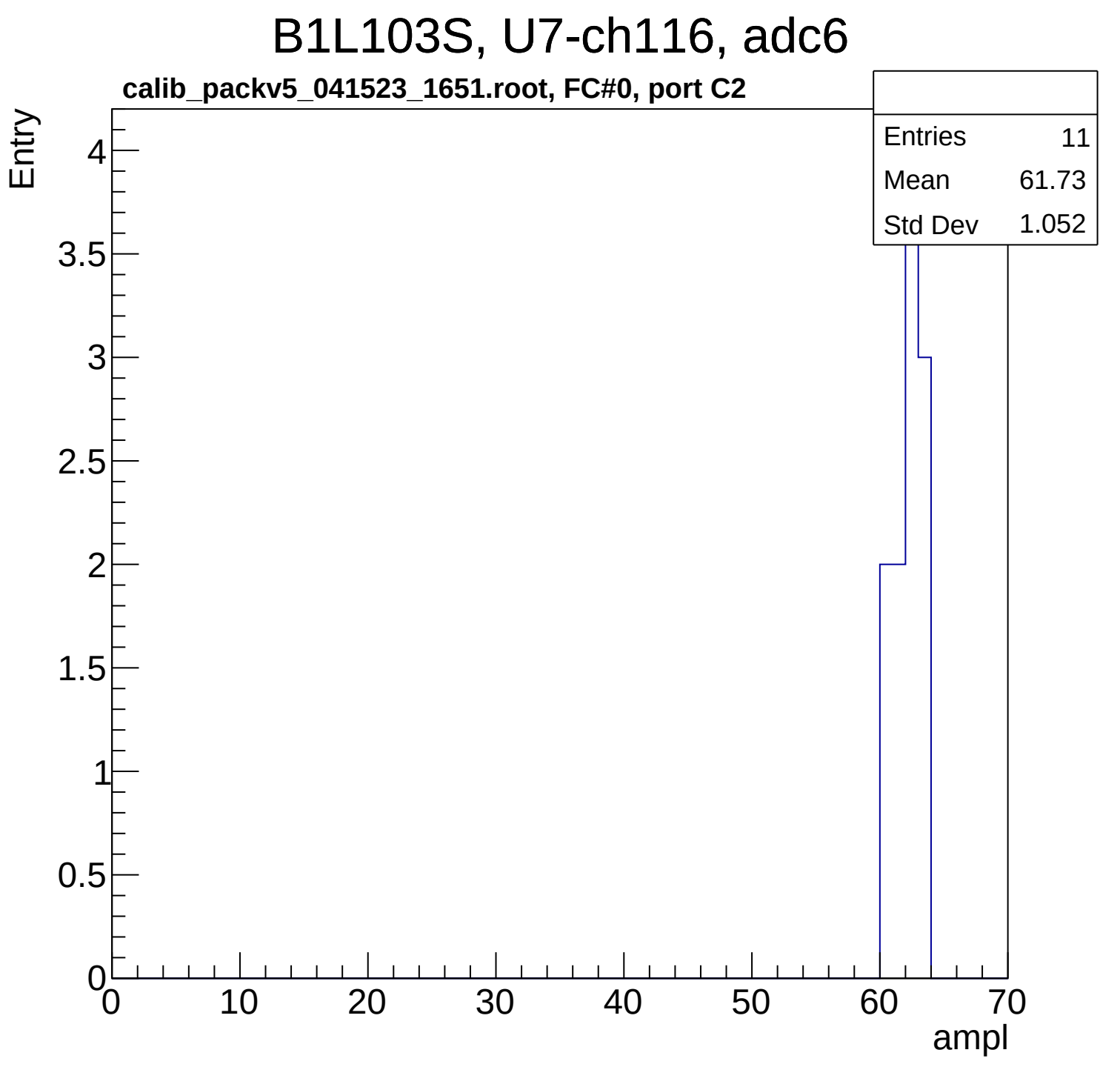
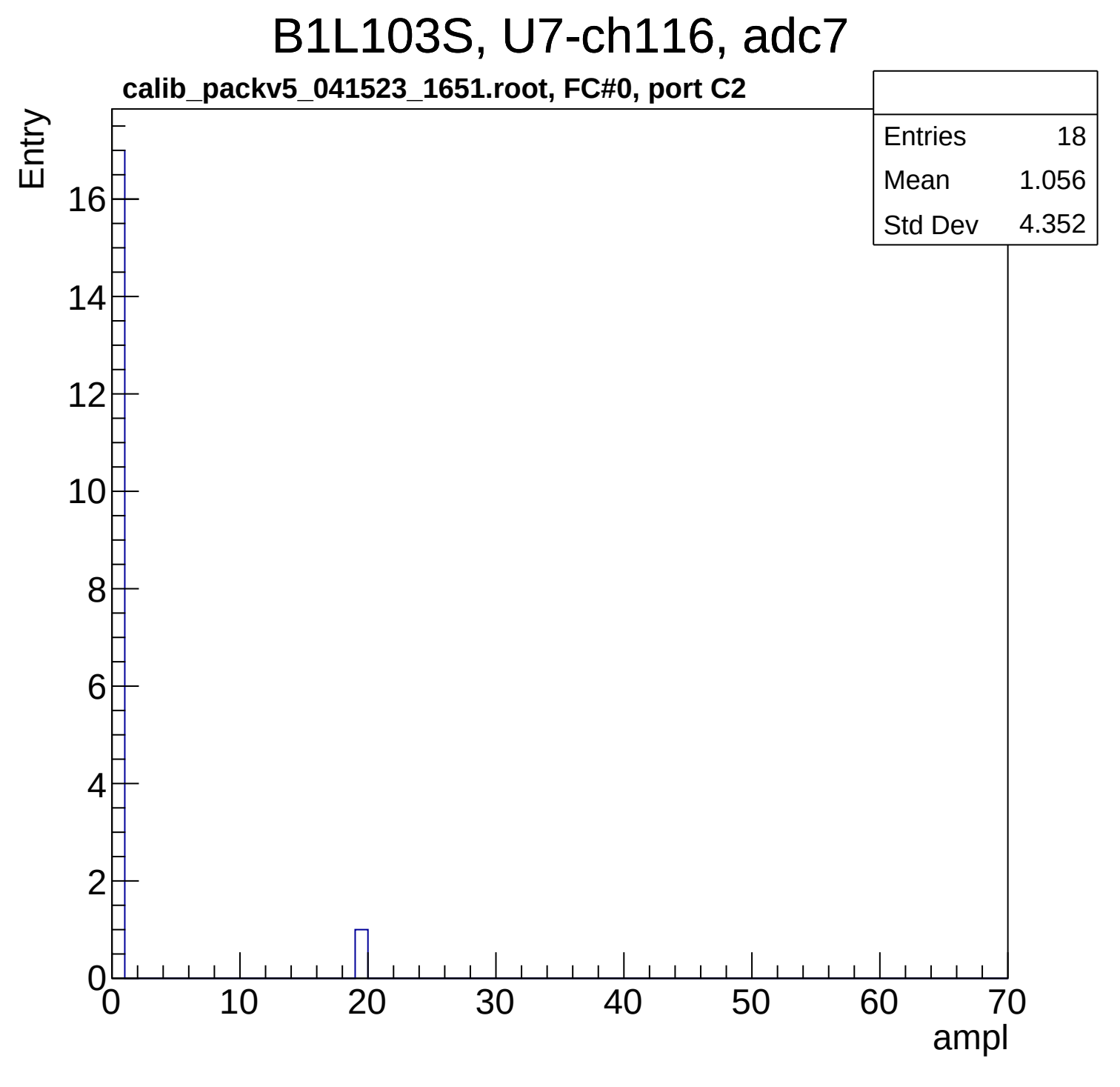
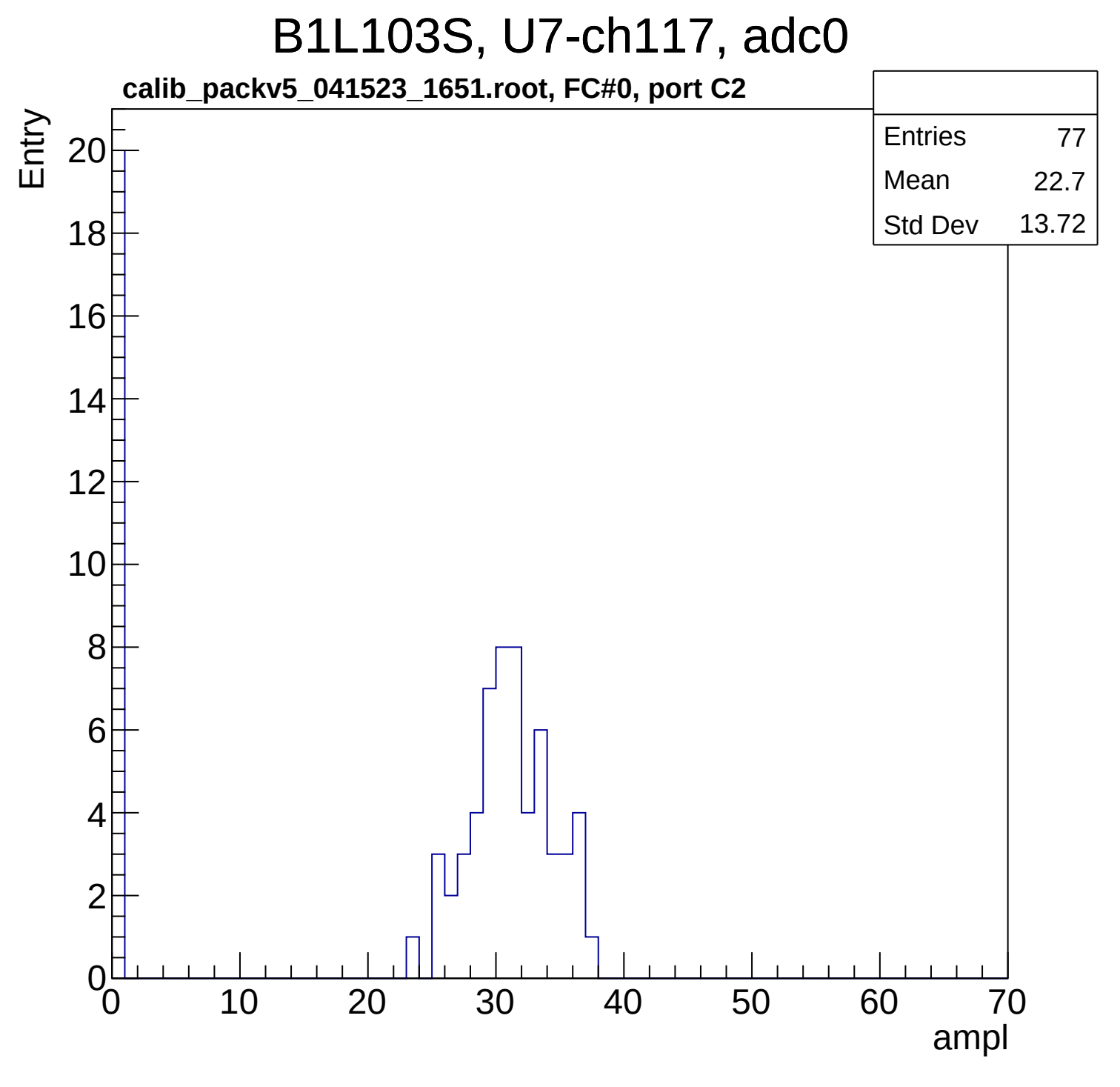
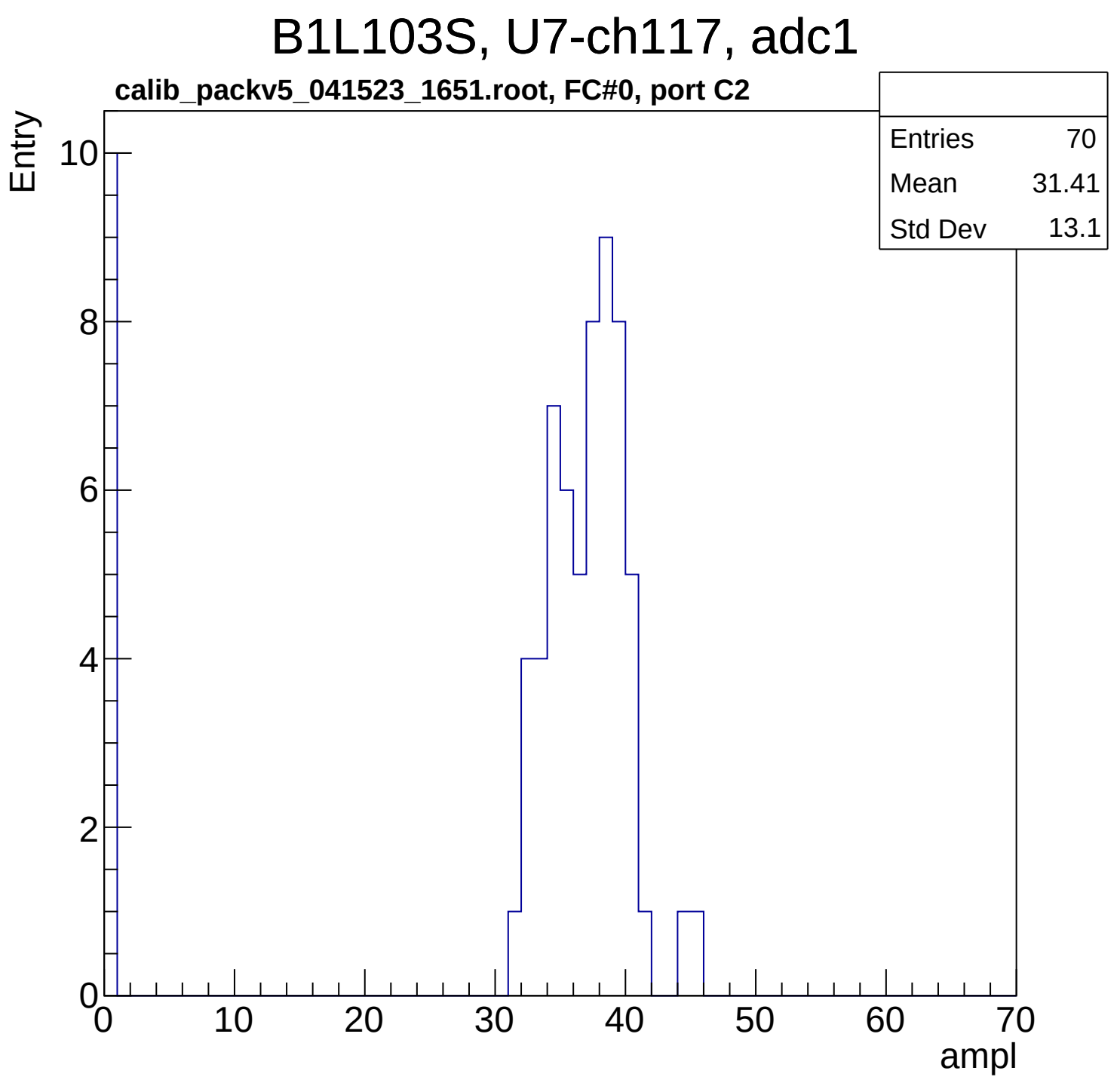
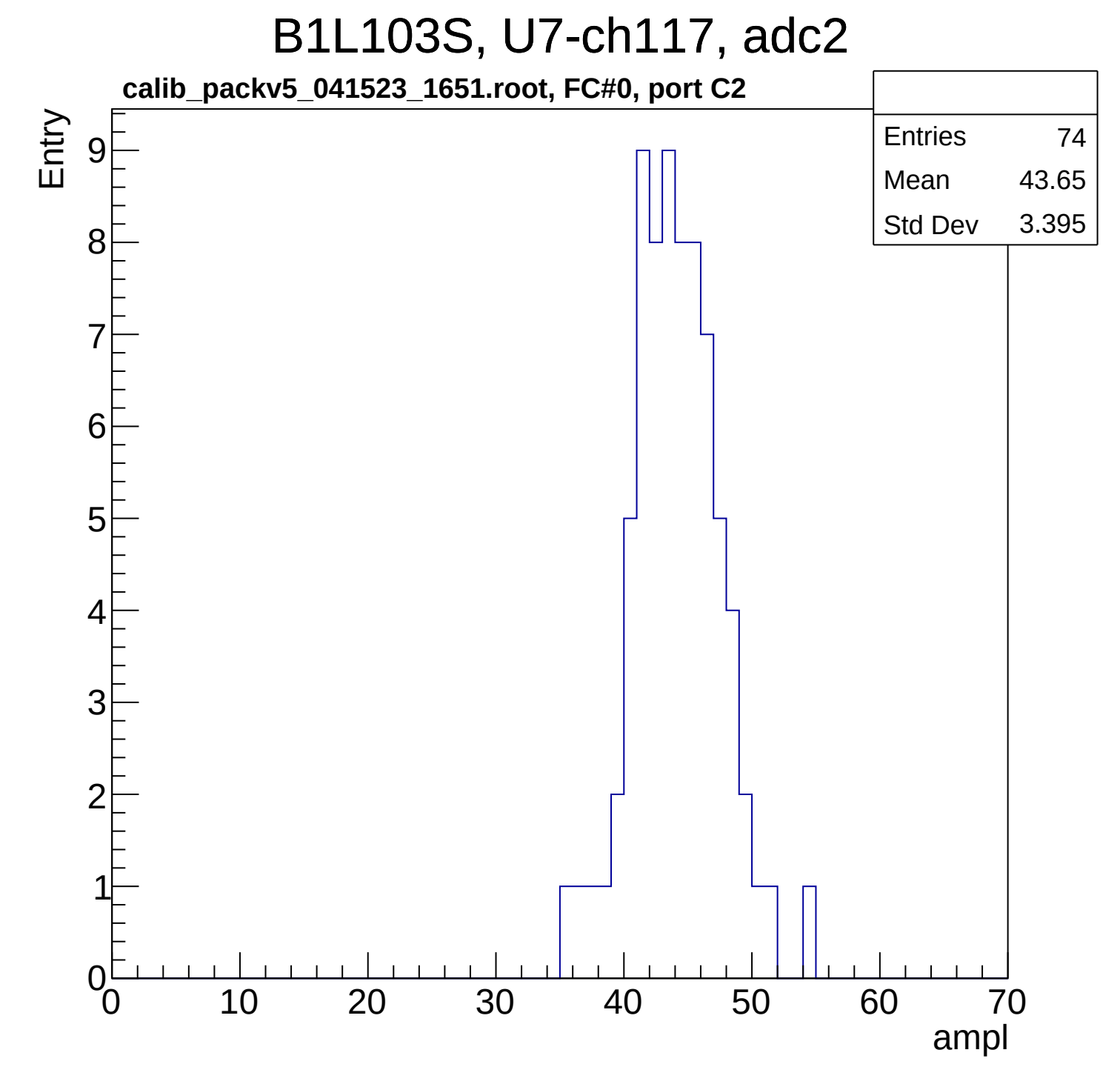
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch116, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 61.73
Std Dev 1.052
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U7-ch116, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 1.056
Std Dev 4.352
Entry
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch117, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 22.7
Std Dev 13.72
Entry
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch117, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 31.41
Std Dev 13.1
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch117, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 43.65
Std Dev 3.395
Entry
ampl
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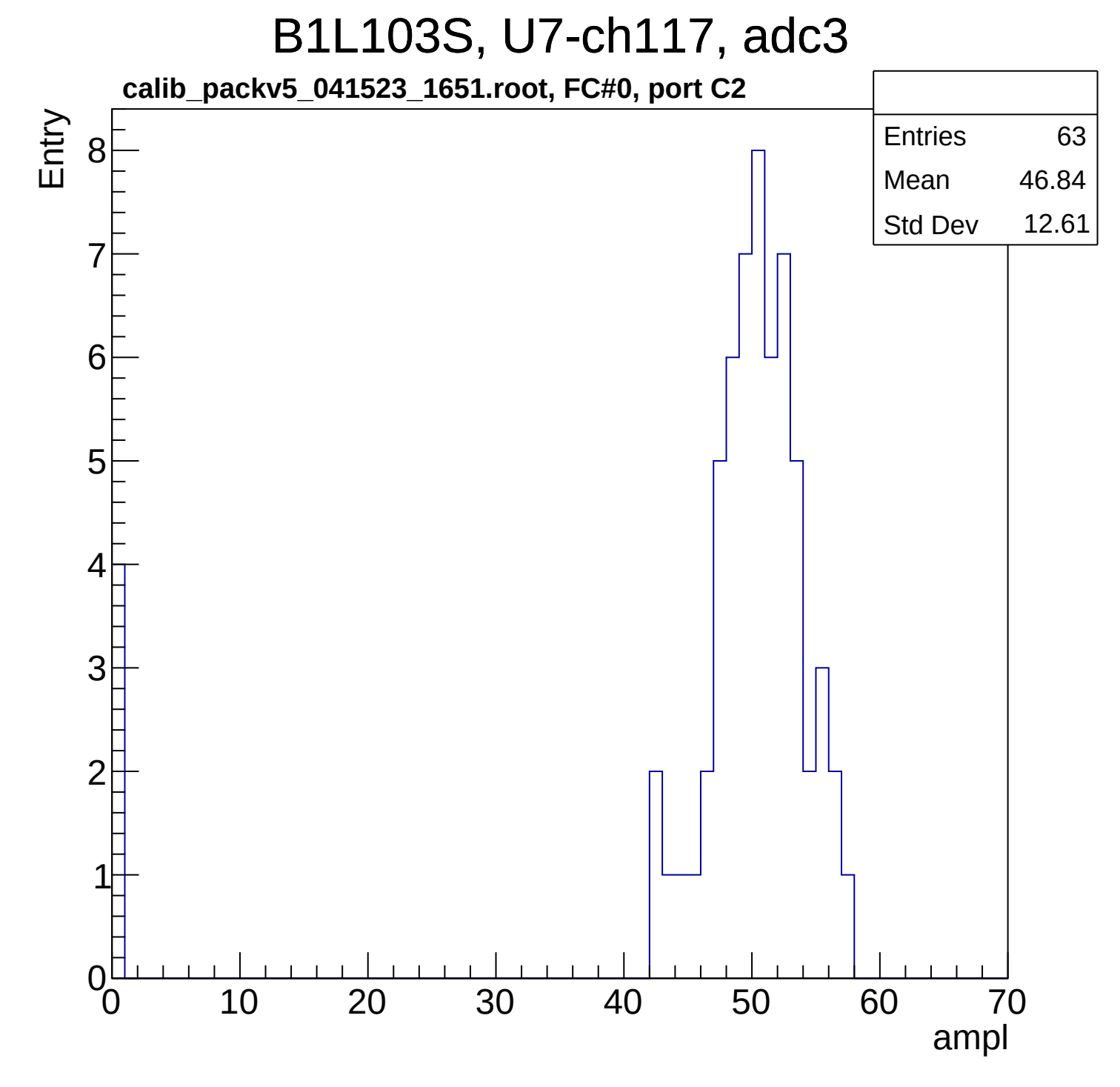
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U7-ch117, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 46.84
Std Dev 12.61
Entry
ampl
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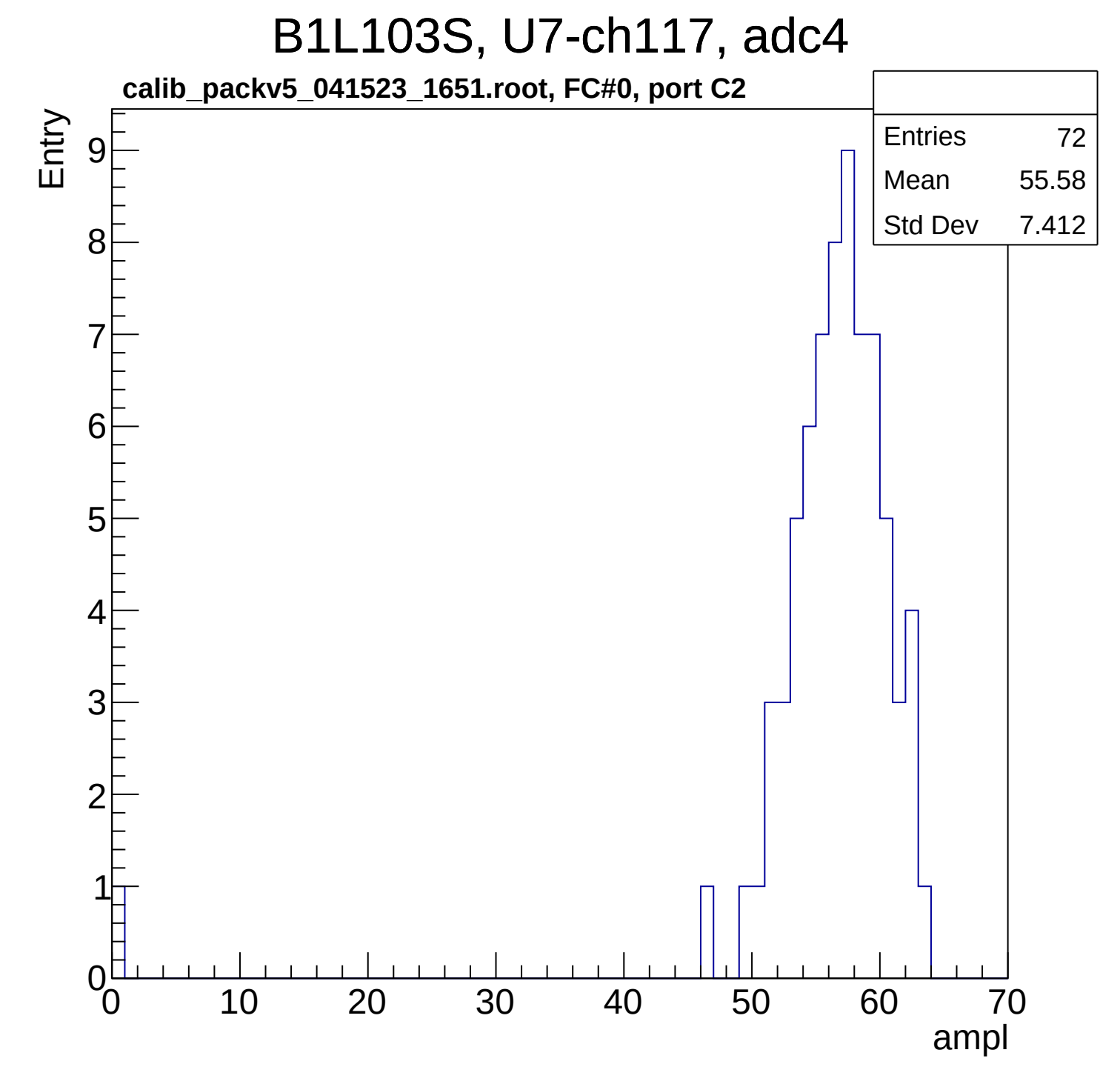
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch117, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 55.58
Std Dev 7.412
Entry
ampl
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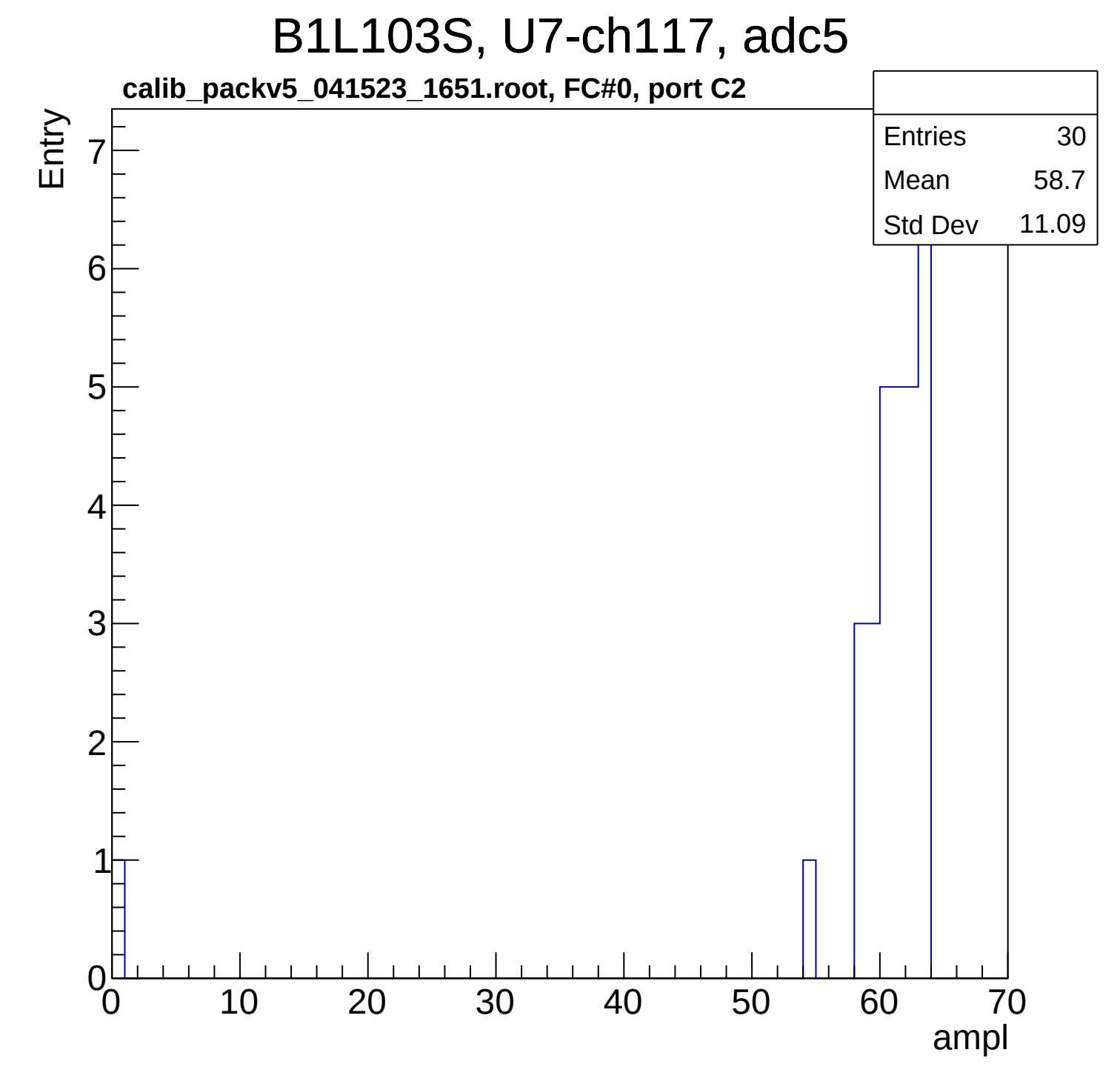
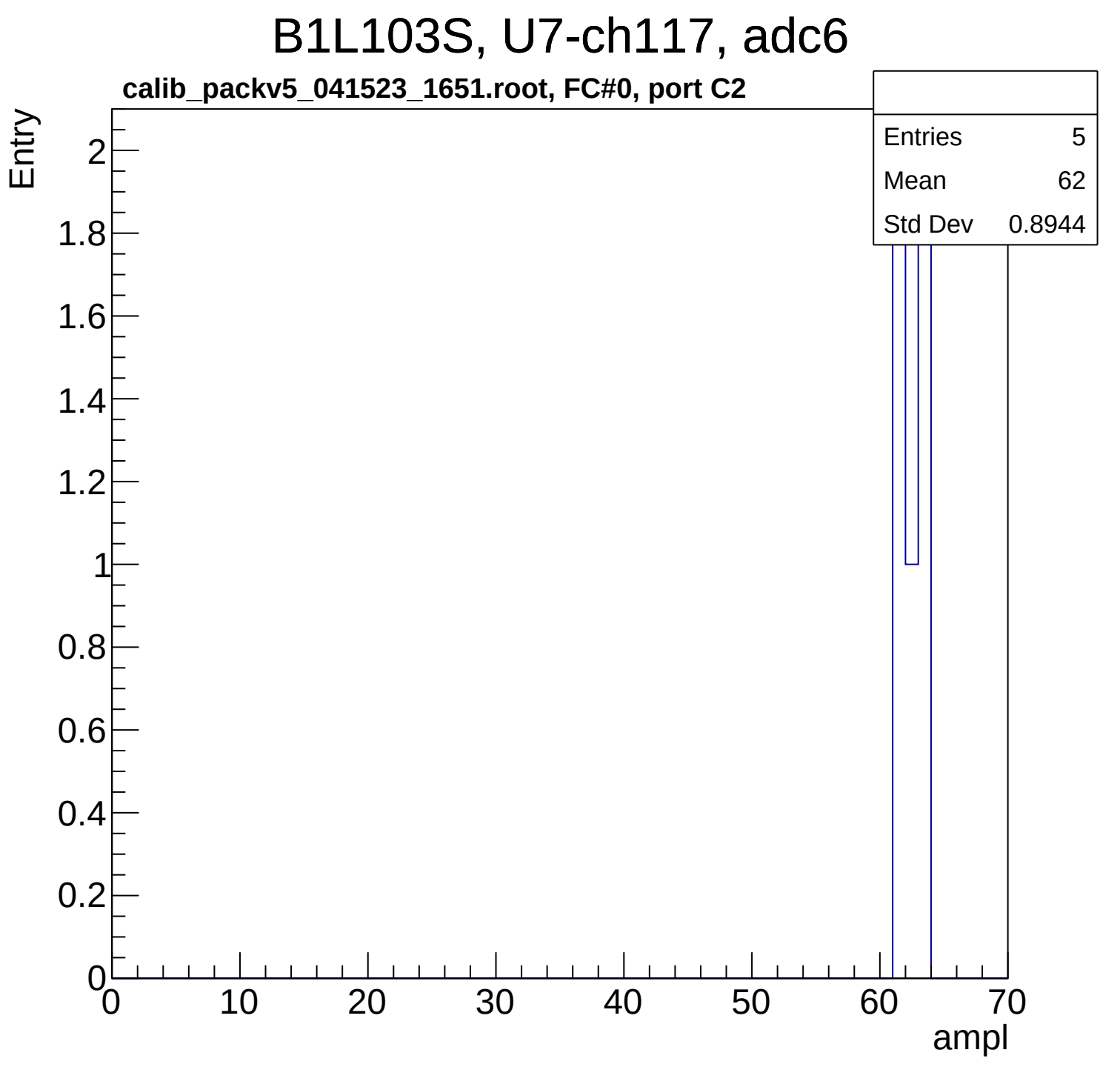
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U7-ch117, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 30
Mean 58.7
Std Dev 11.09
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U7-ch117, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 5
Mean 62
Std Dev 0.8944
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
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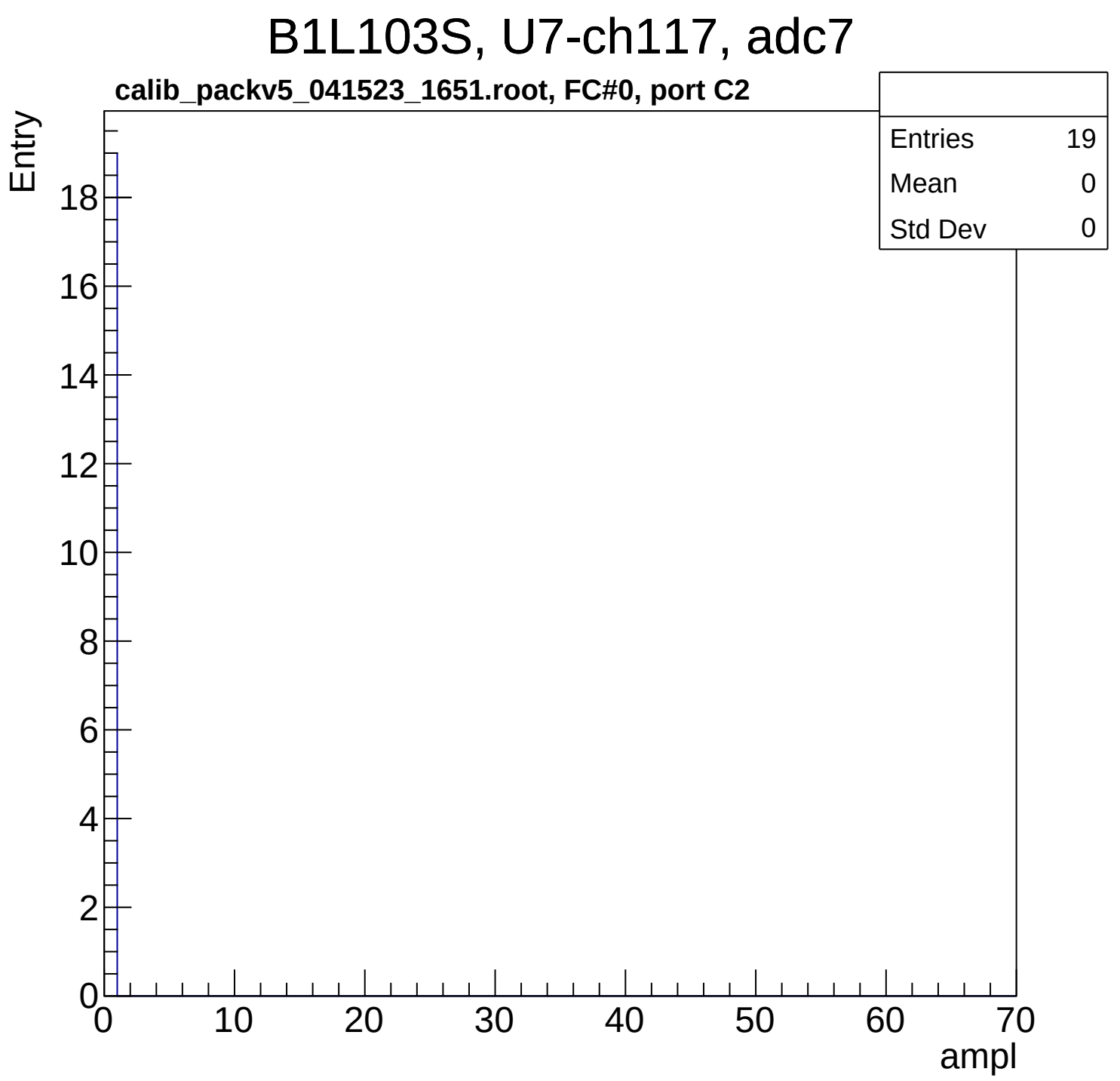
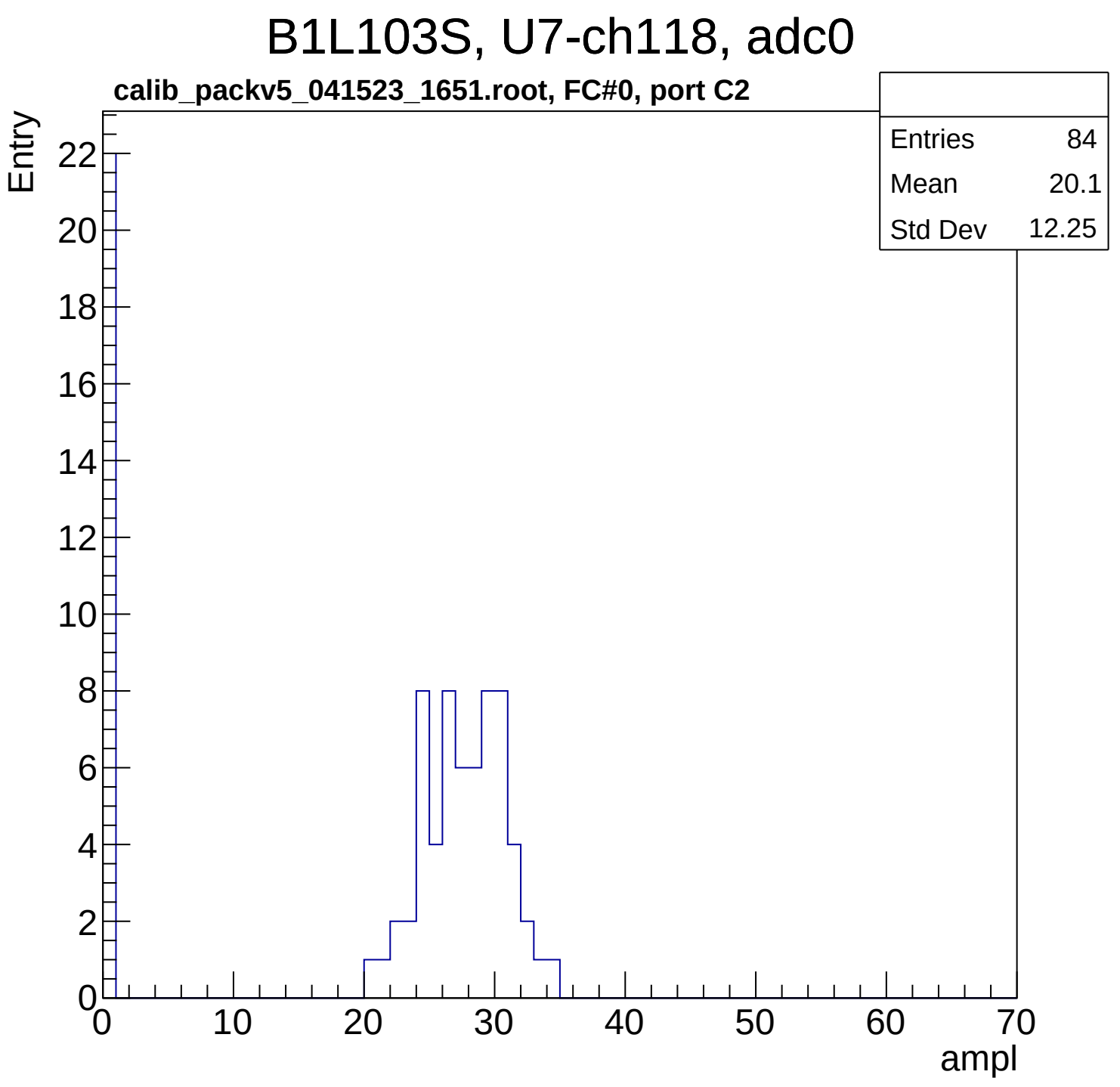
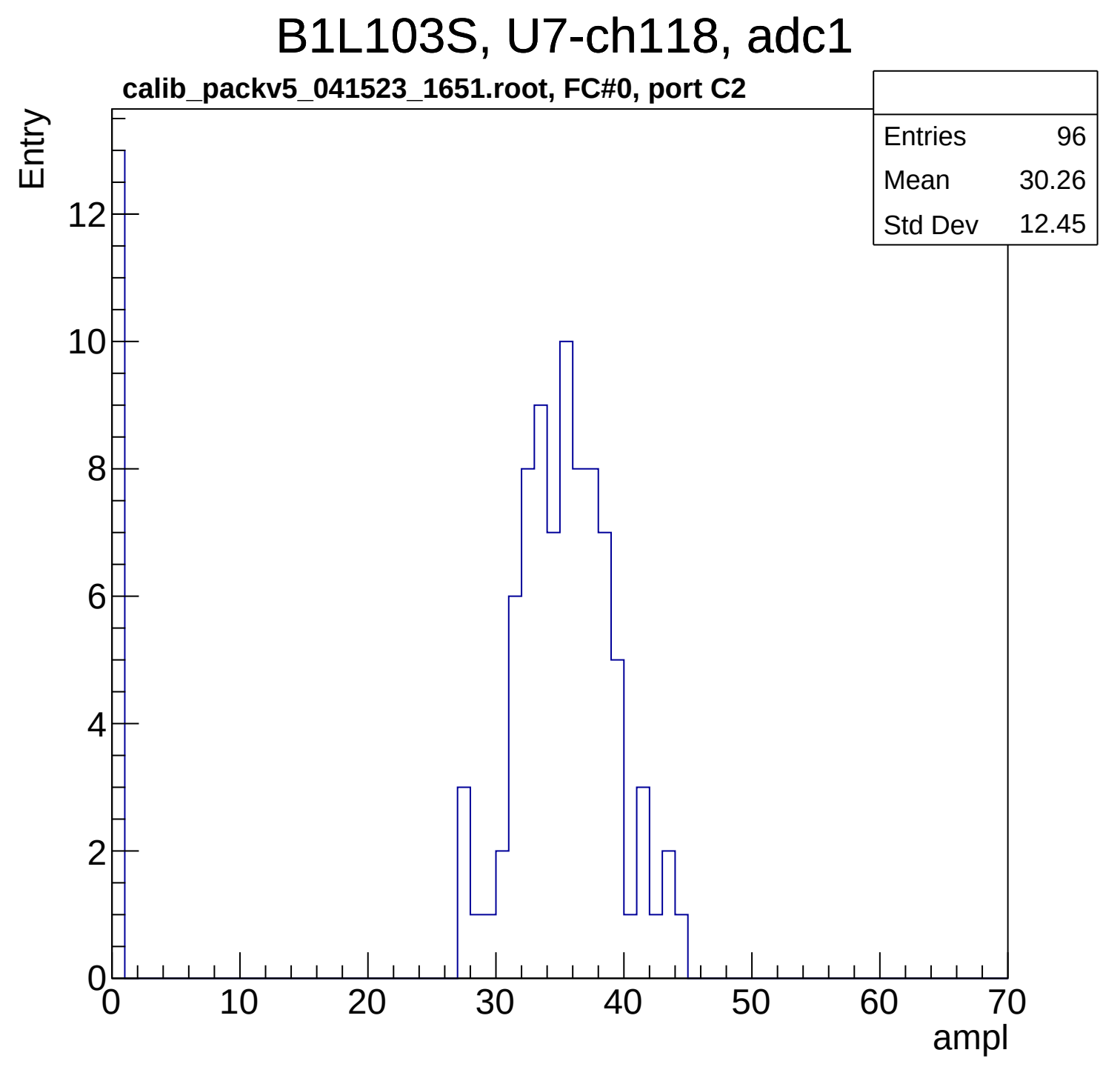
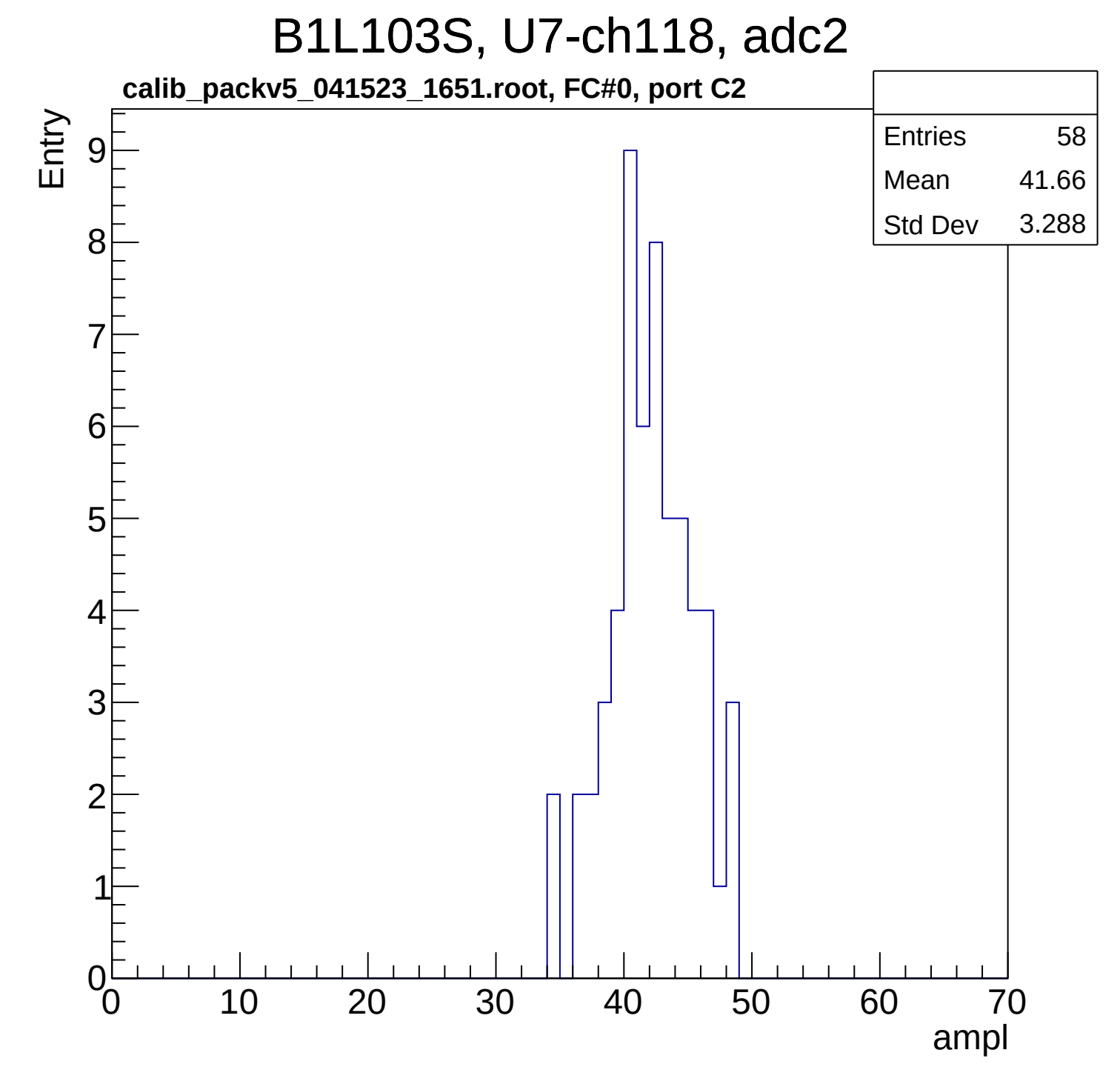

B1L103S, U7-ch117, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch118, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 20.1
Std Dev 12.25
Entry
0
2
4
6
8
10
12
14
16
18
20
22
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch118, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 96
Mean 30.26
Std Dev 12.45
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70


B1L103S, U7-ch118, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 41.66
Std Dev 3.288
Entry
ampl
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2
3
4
5
6
7
8
9
0
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40
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60
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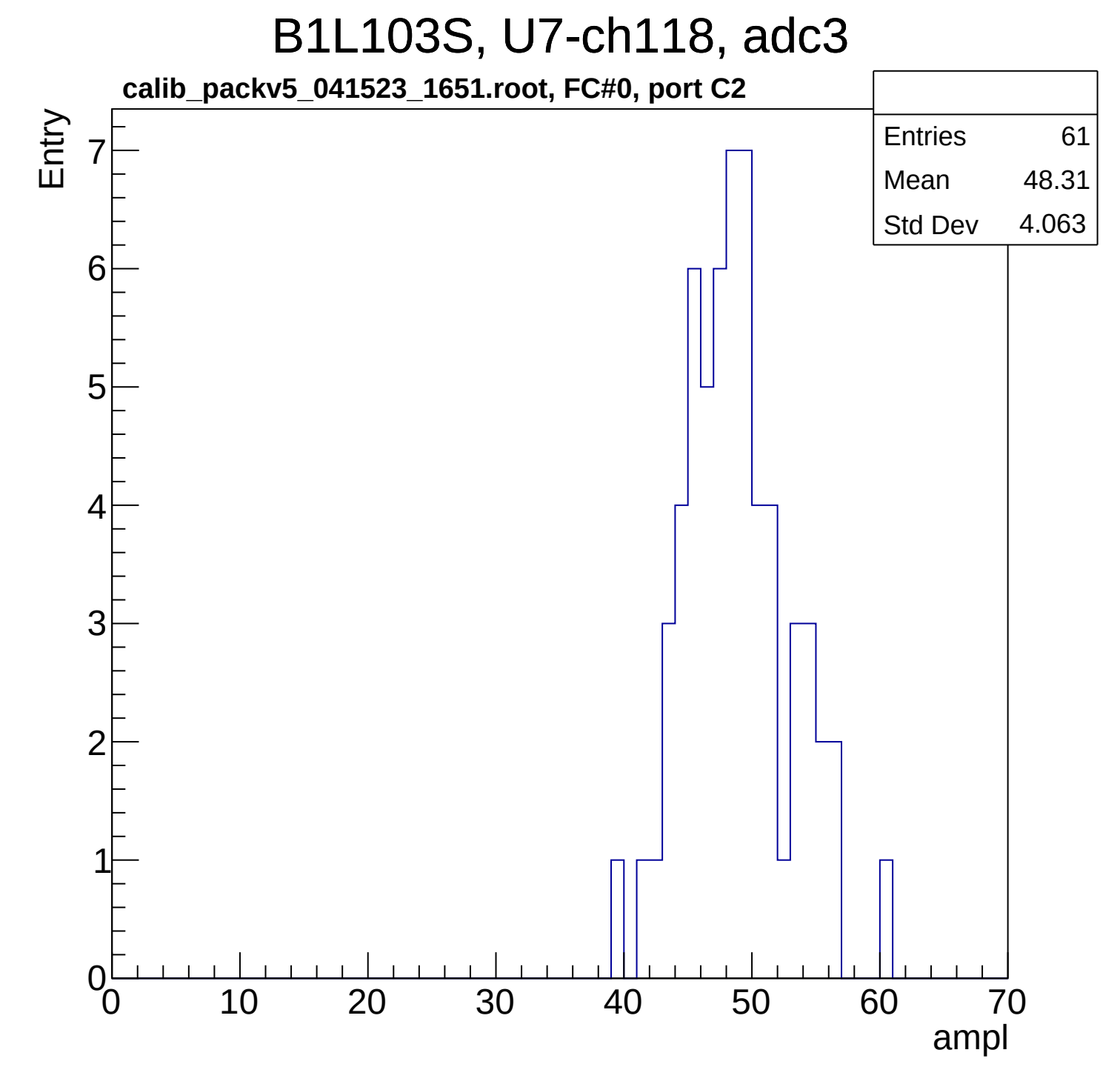
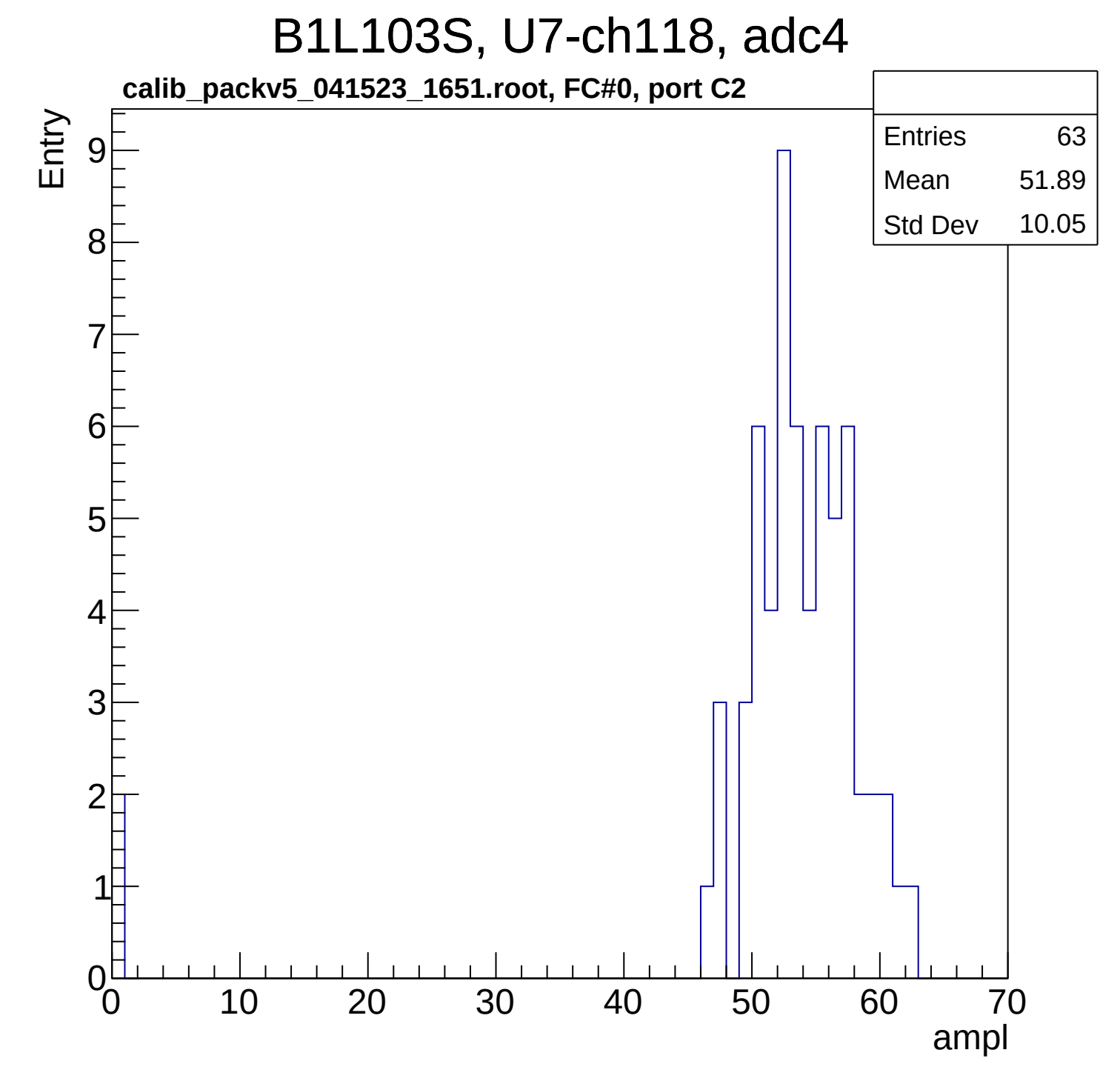

B1L103S, U7-ch118, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 48.31
Std Dev 4.063
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U7-ch118, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 51.89
Std Dev 10.05
Entry
ampl
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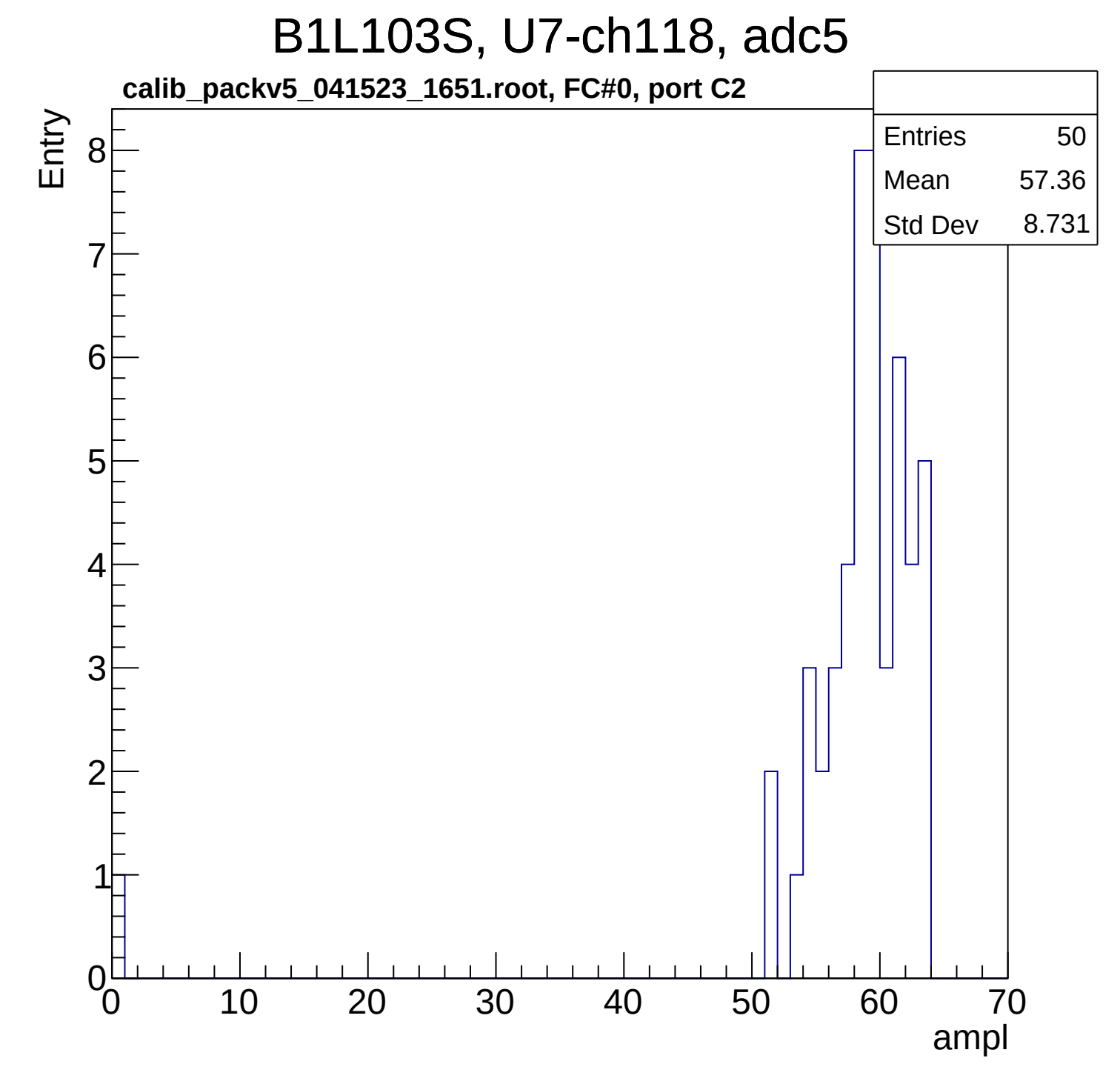
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U7-ch118, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 57.36
Std Dev 8.731
Entry
ampl
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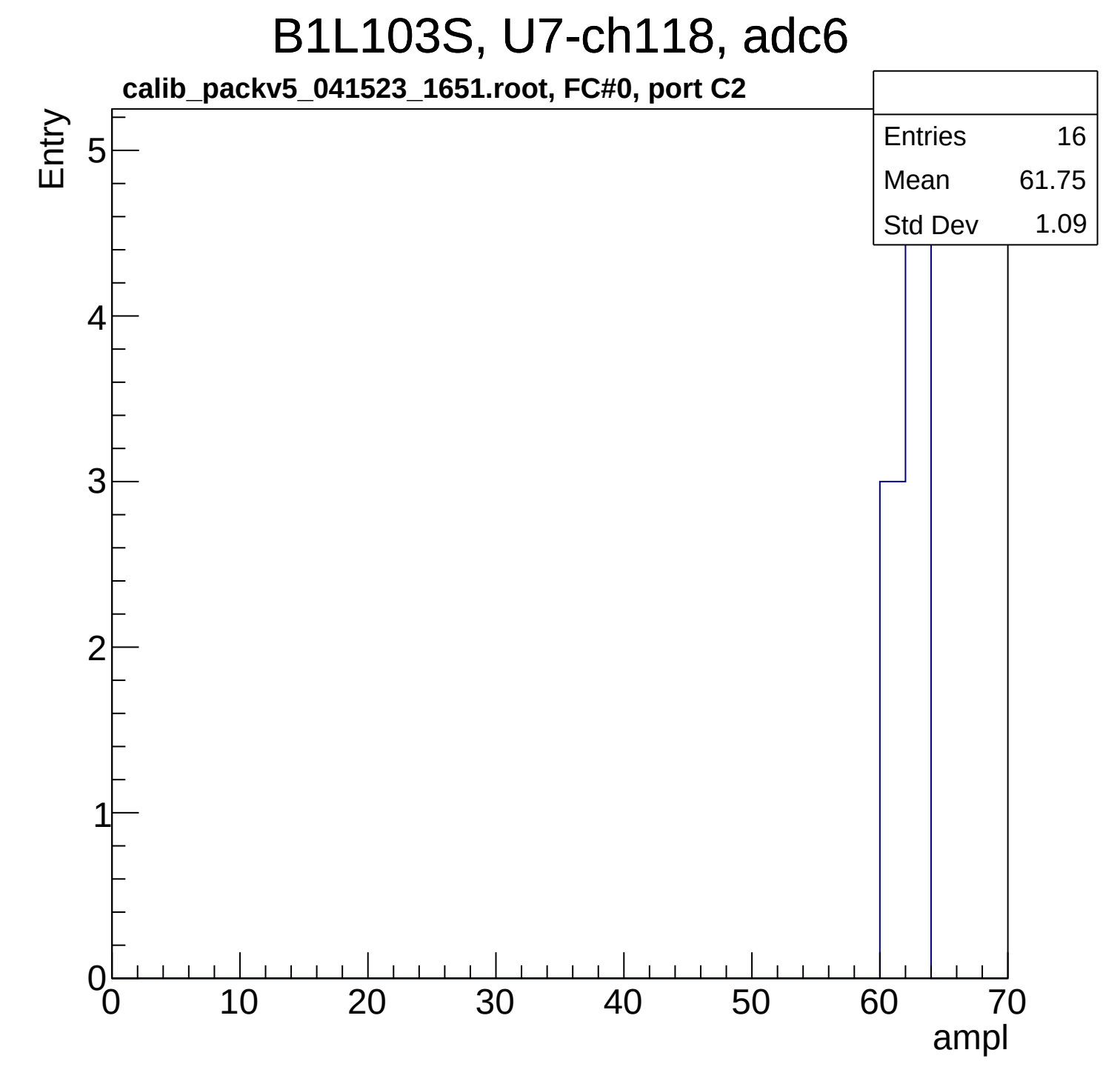
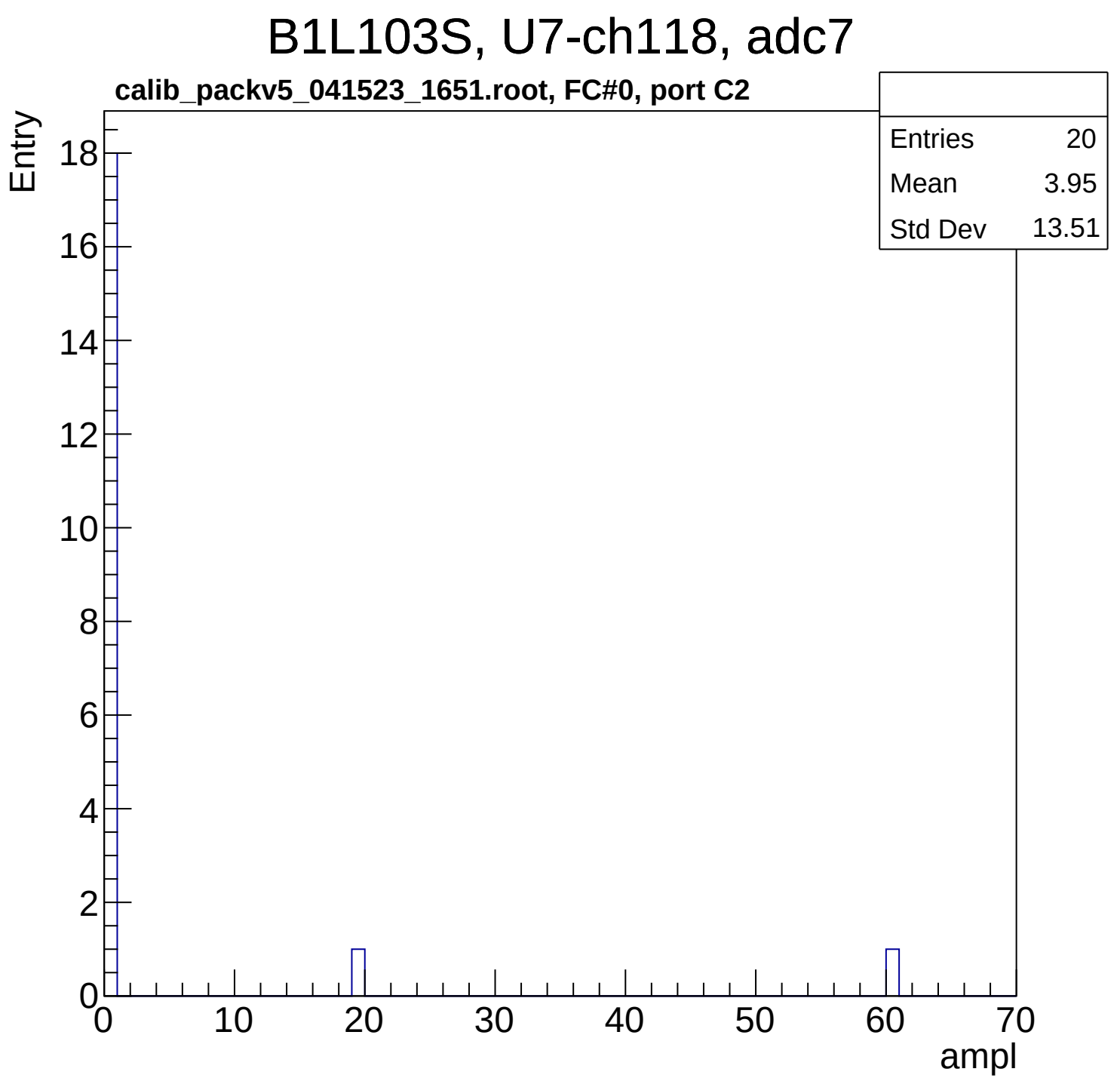
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch118, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 16
Mean 61.75
Std Dev 1.09
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch118, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.95
Std Dev 13.51
Entry
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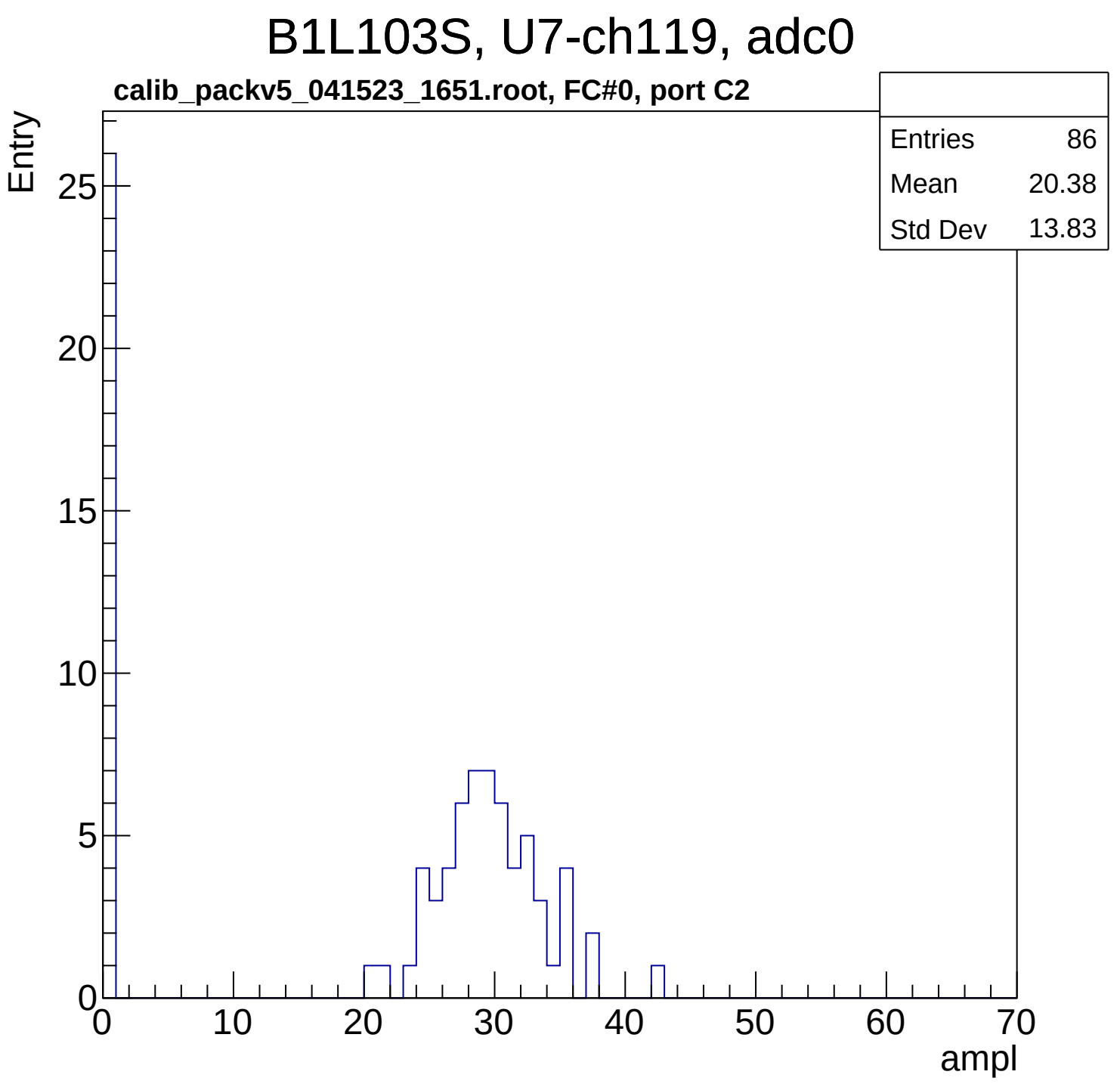
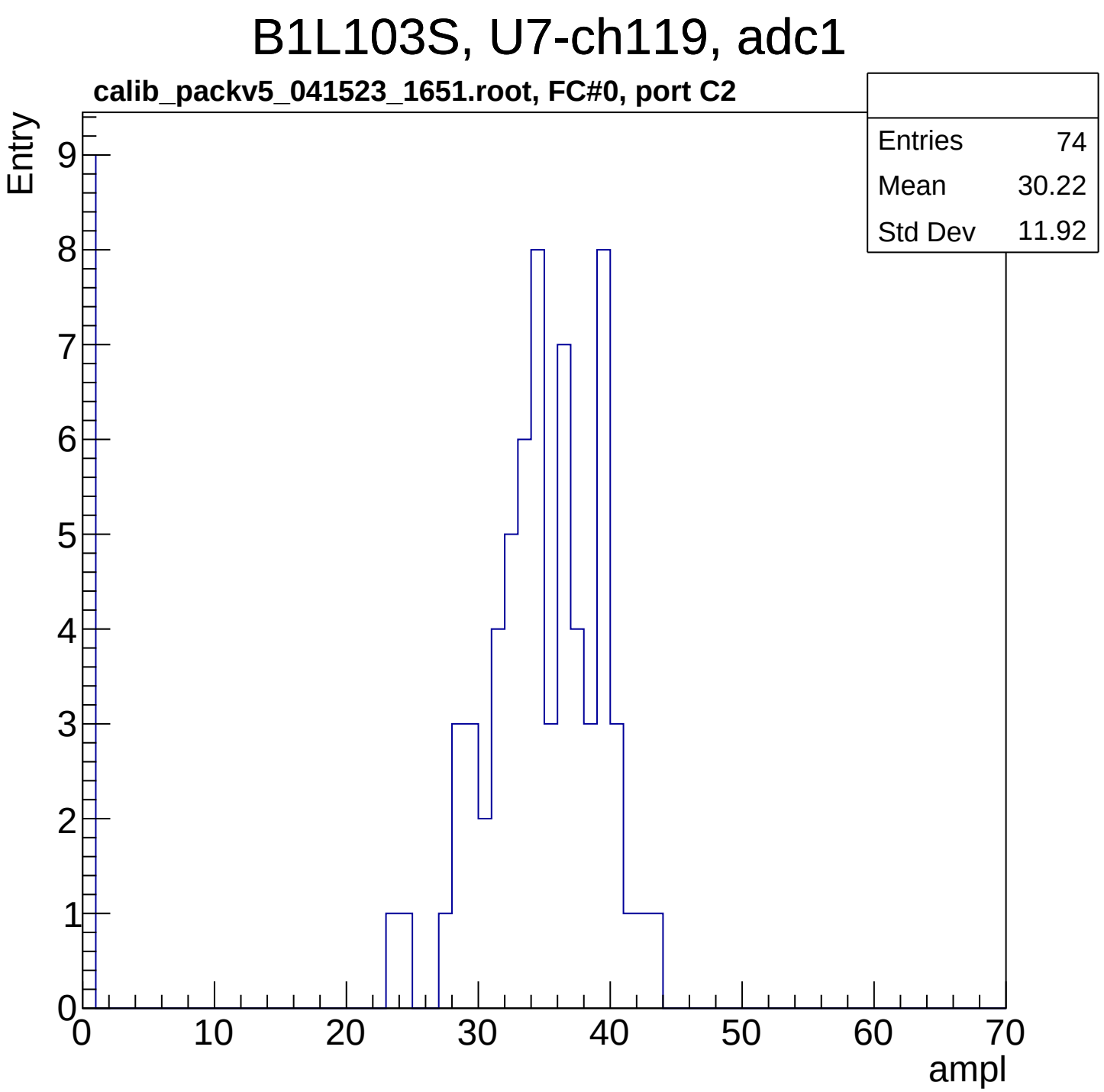
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch119, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 20.38
Std Dev 13.83
Entry
0
5
10
15
20
25
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch119, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 30.22
Std Dev 11.92
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
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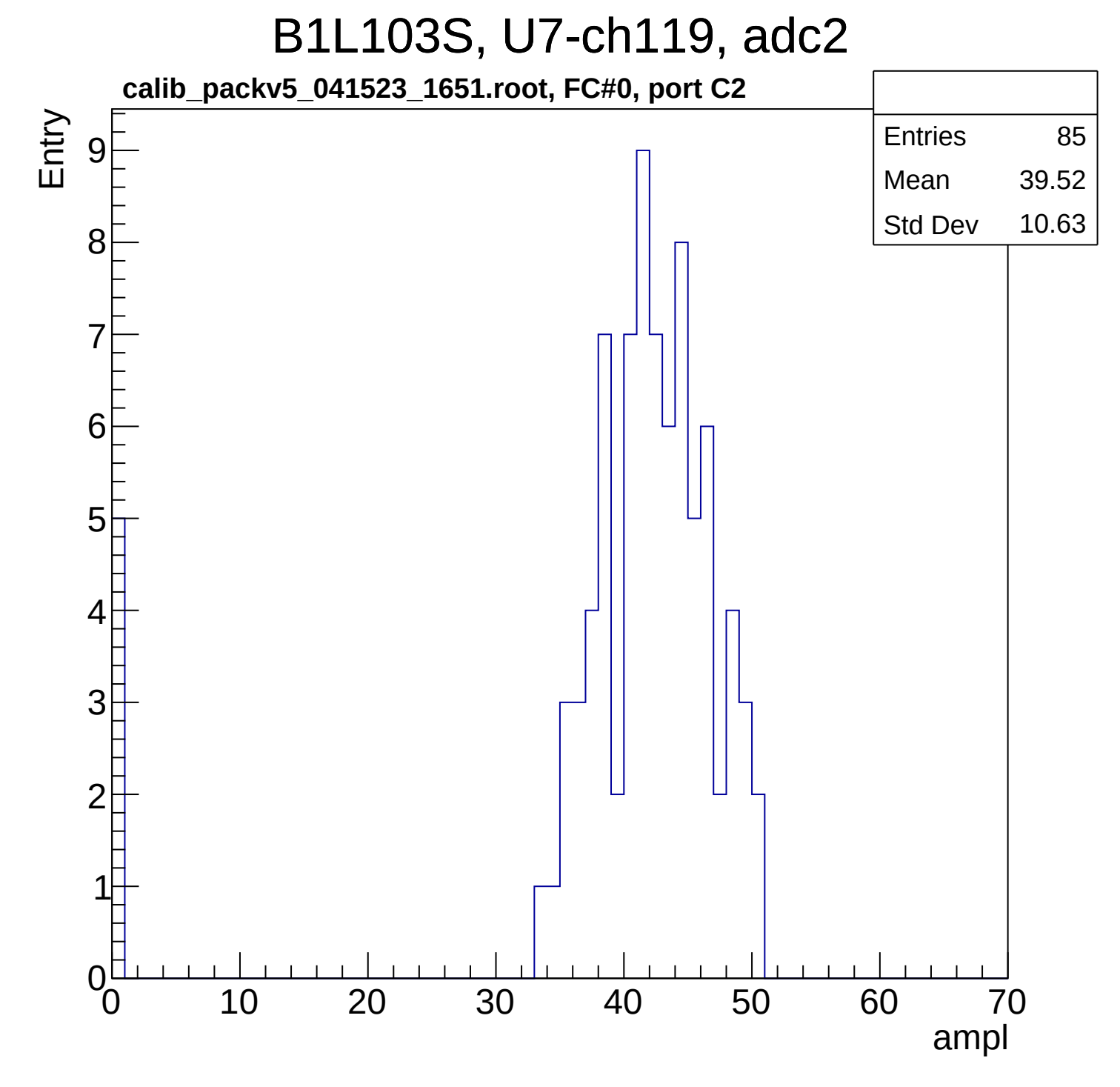
40
50
60
70


B1L103S, U7-ch119, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 39.52
Std Dev 10.63
Entry
ampl
0
1
2
3
4
5
6
7
8
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0
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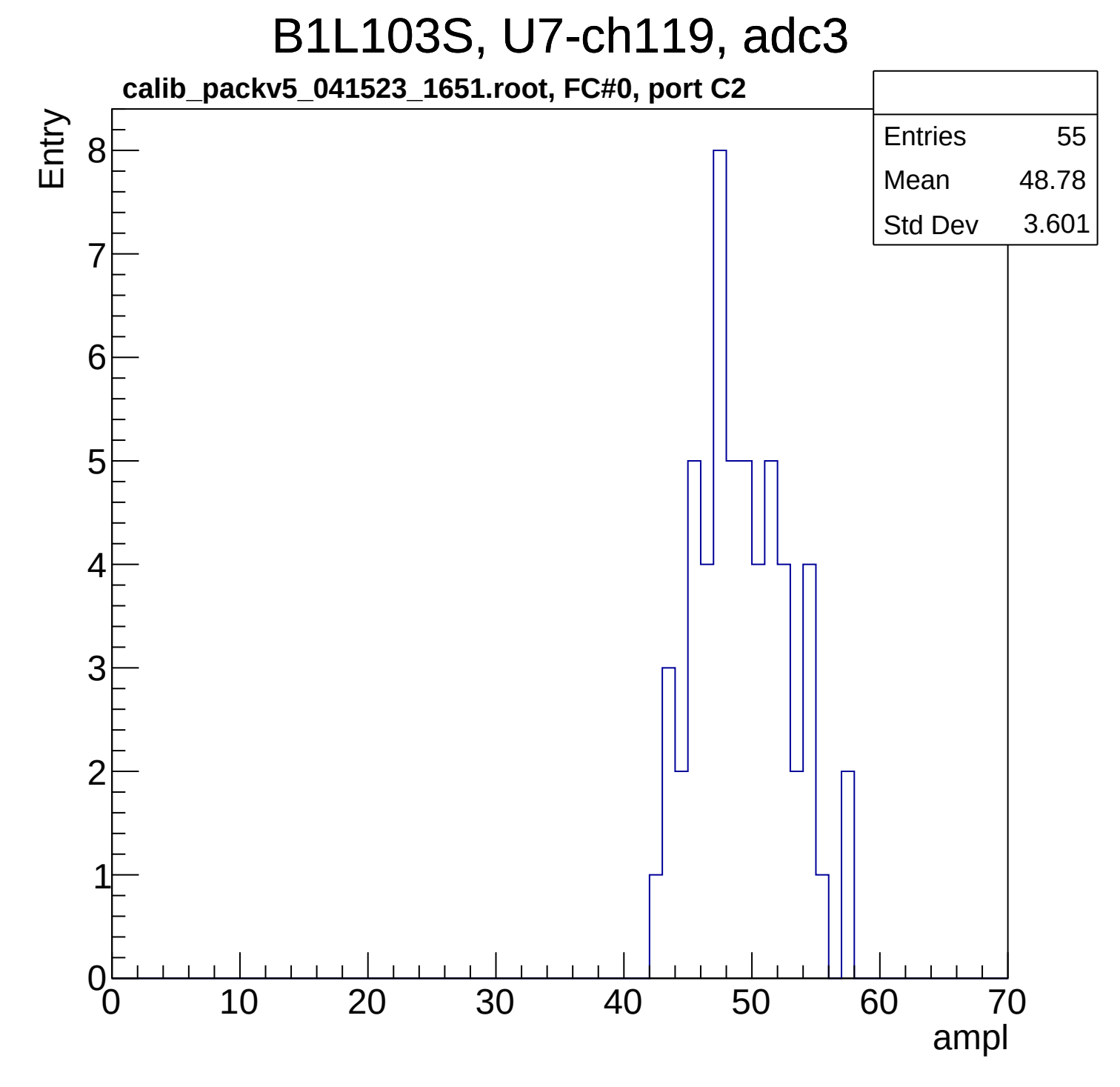
B1L103S, U7-ch119, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 48.78
Std Dev 3.601
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
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60
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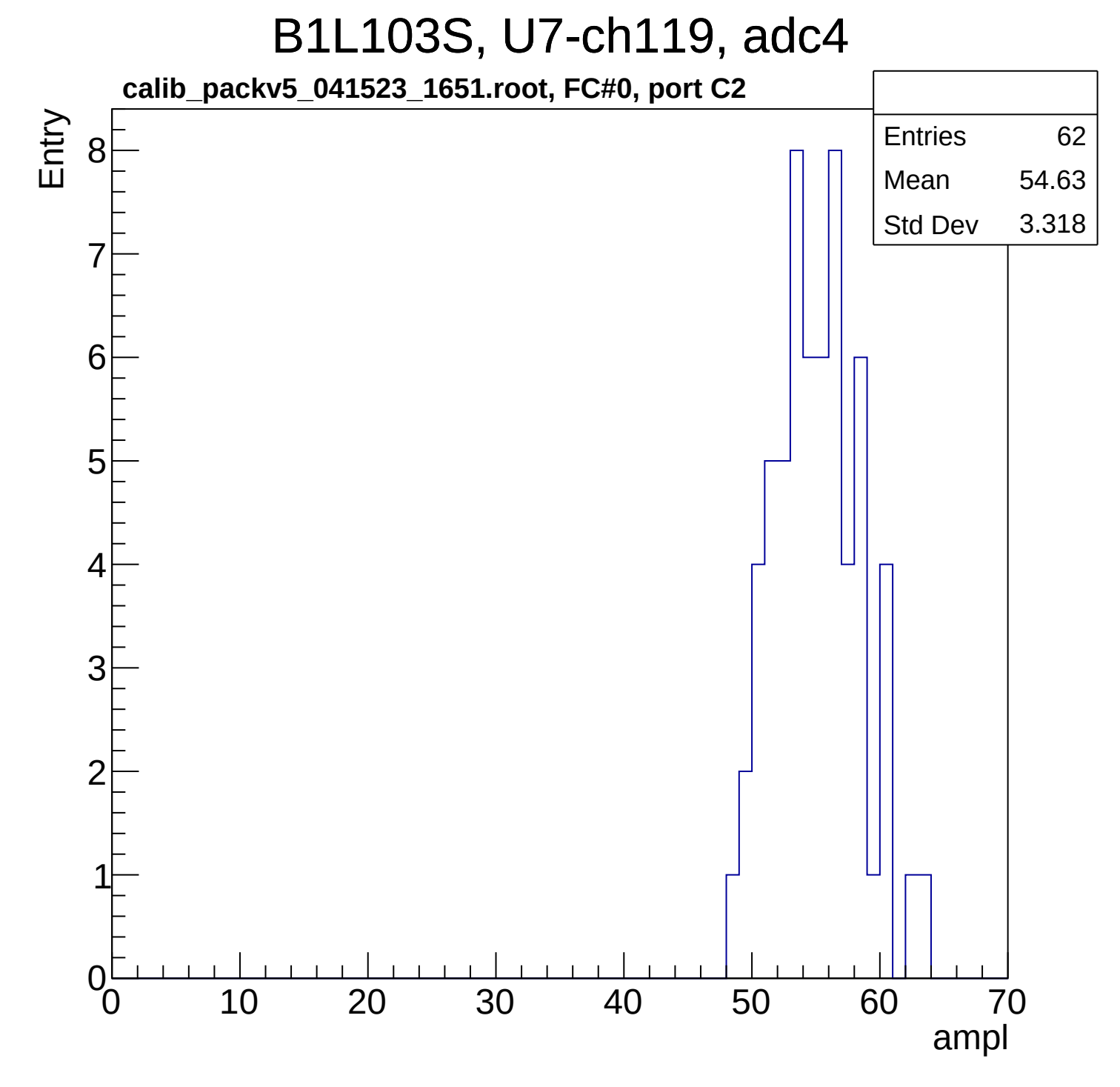
B1L103S, U7-ch119, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 54.63
Std Dev 3.318
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
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40
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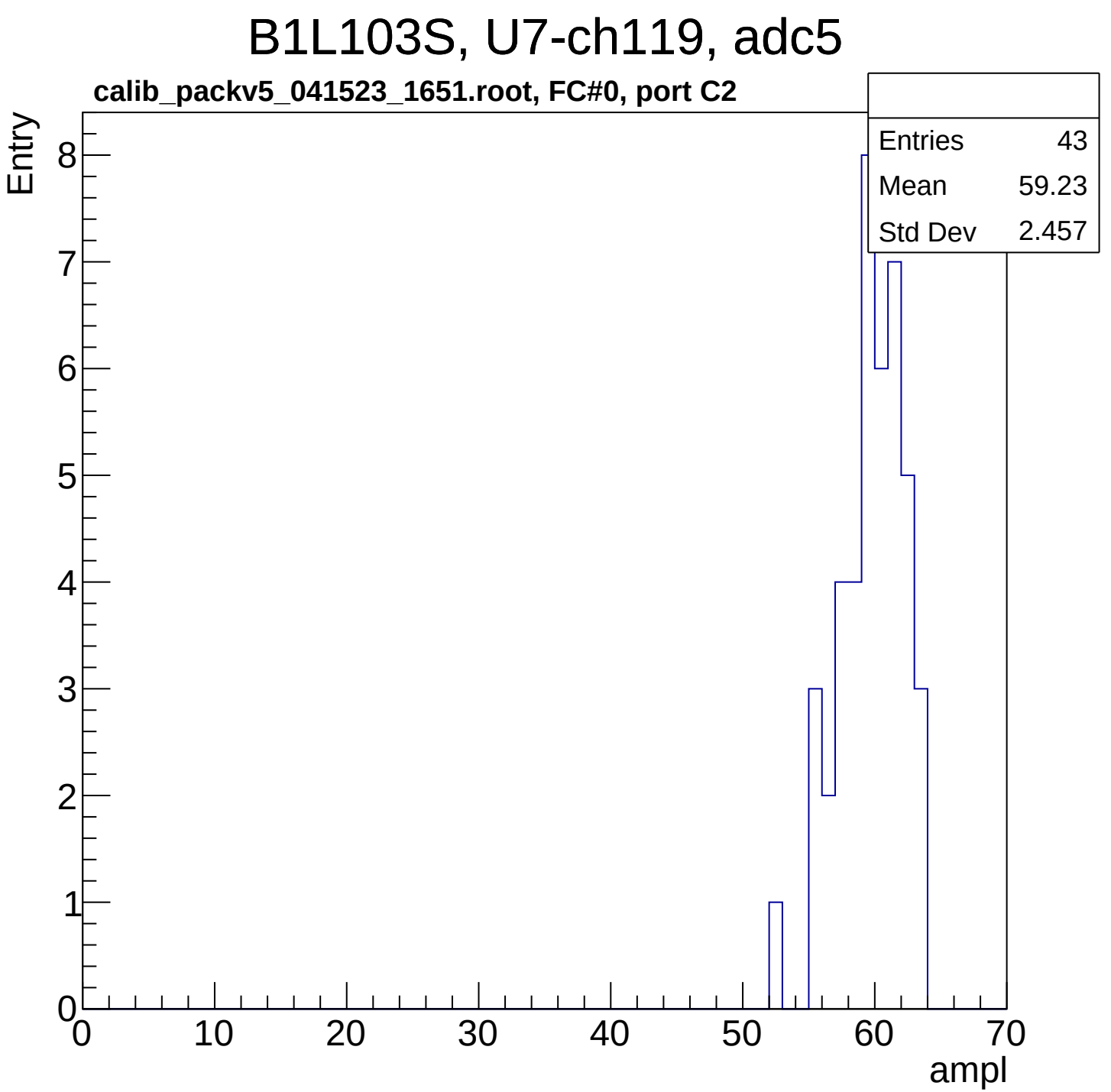
60
70


B1L103S, U7-ch119, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 43
Mean 59.23
Std Dev 2.457
Entry
ampl
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1
2
3
4
5
6
7
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0
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20
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40
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60
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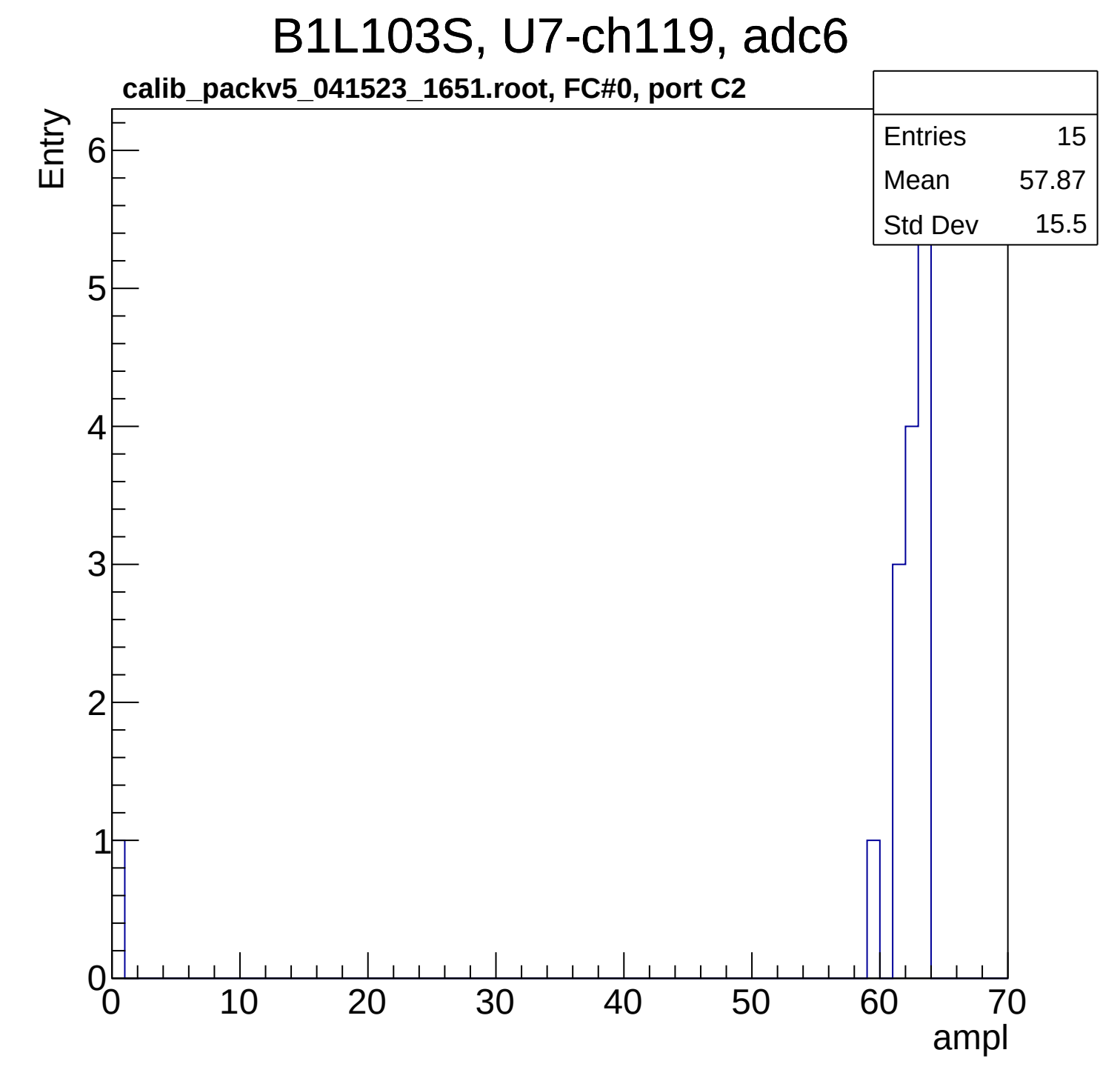
B1L103S, U7-ch119, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 15
Mean 57.87
Std Dev 15.5
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
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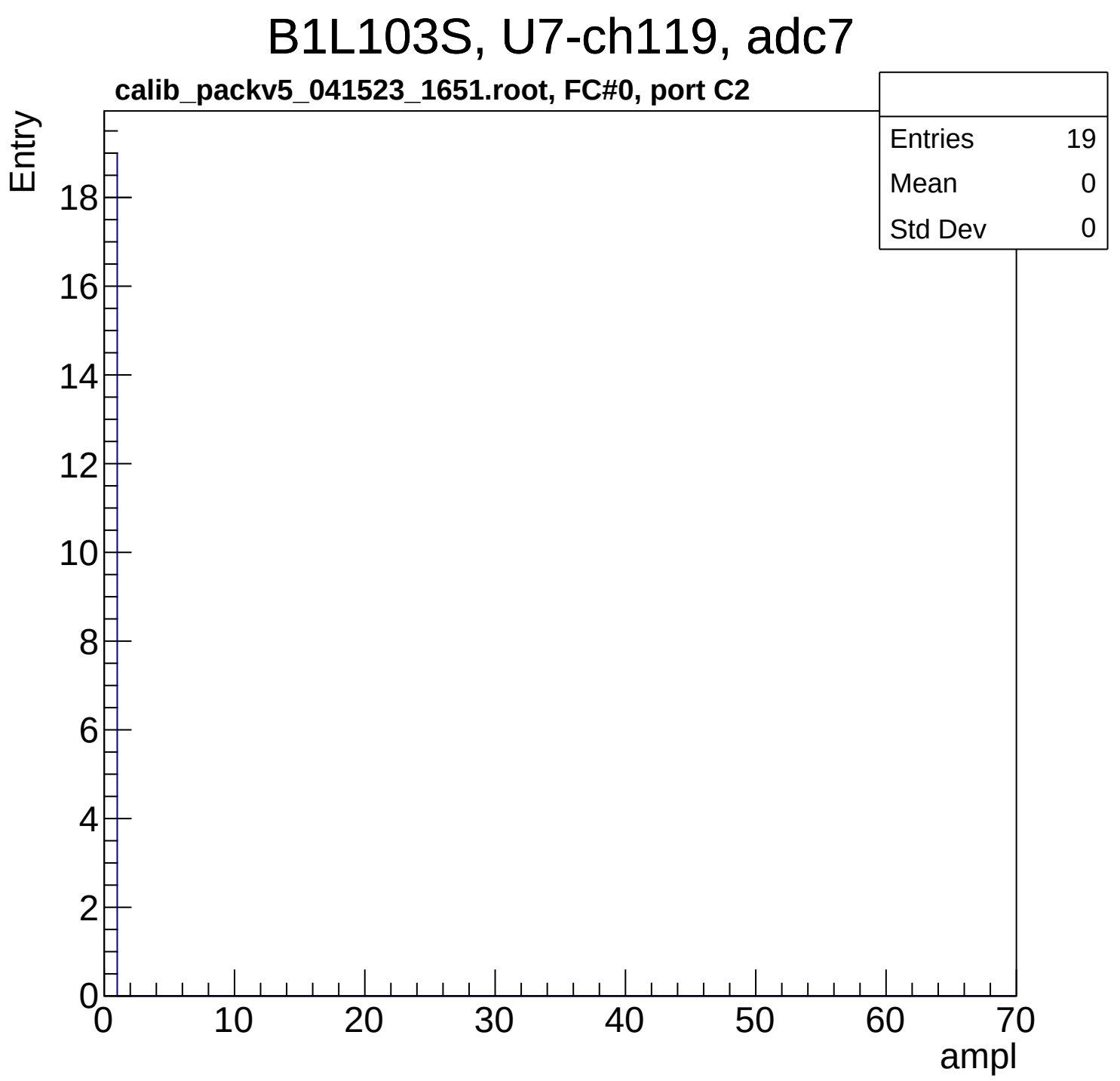
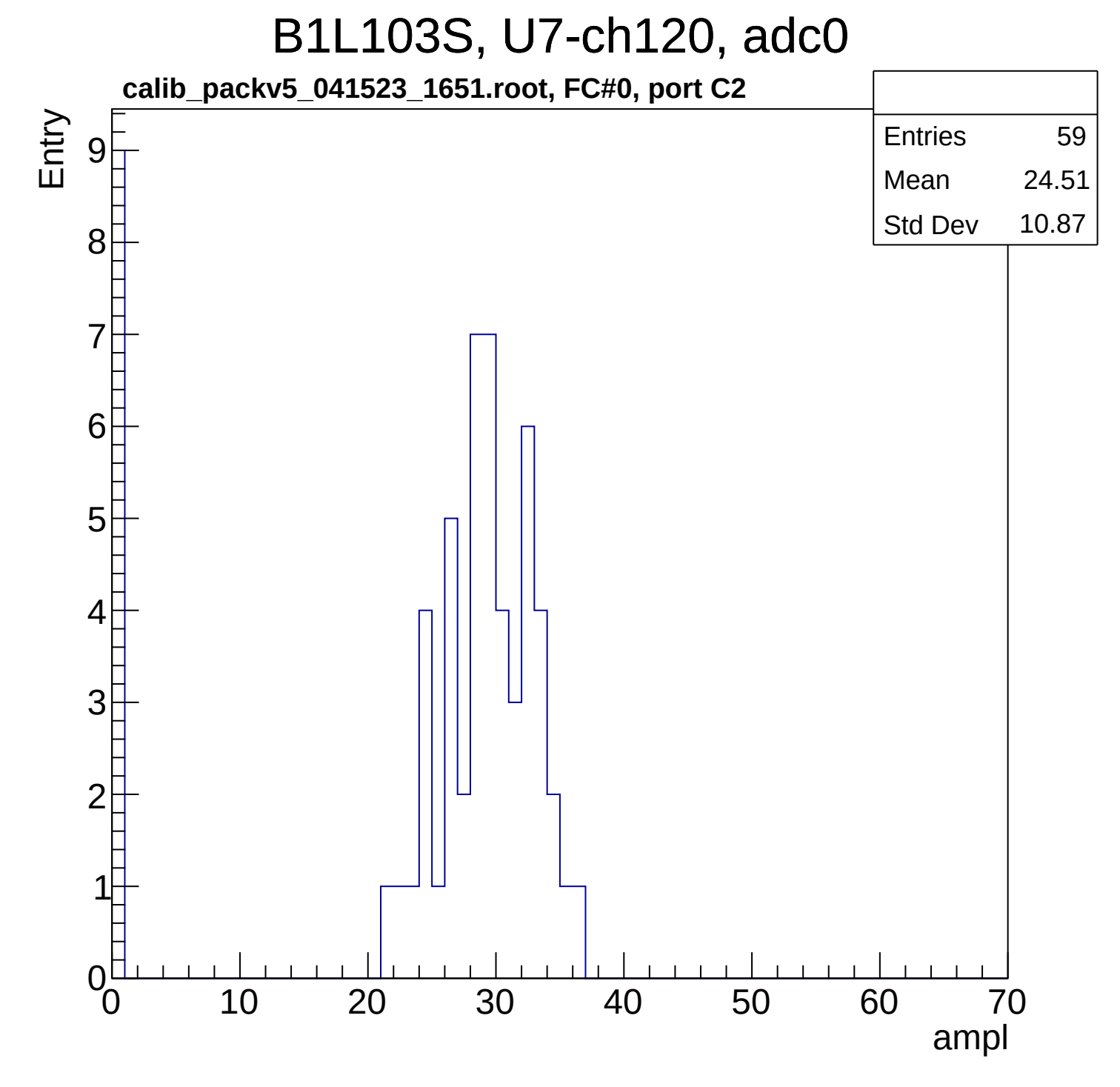

B1L103S, U7-ch119, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch120, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 24.51
Std Dev 10.87
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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30
40
50
60
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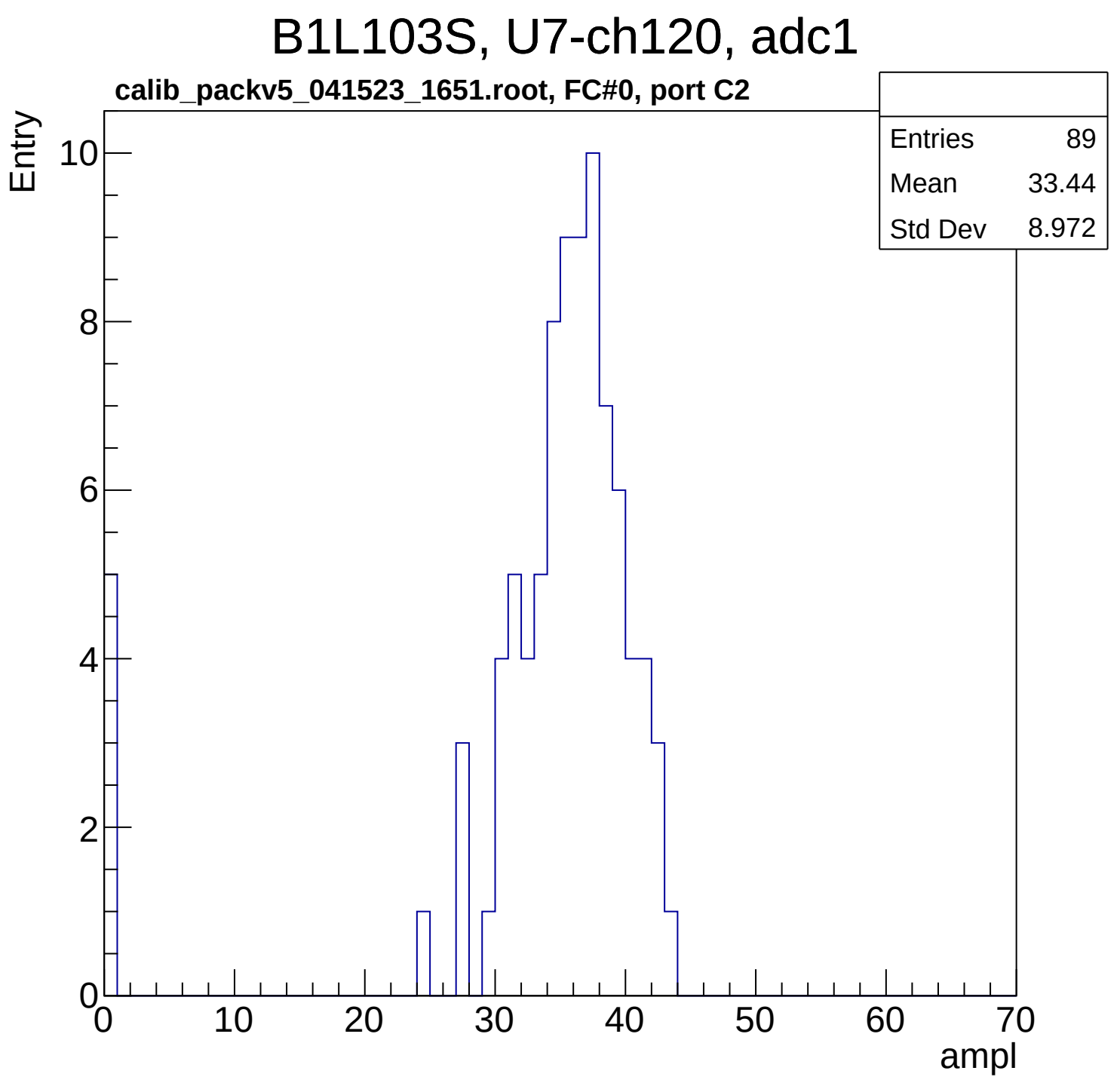
B1L103S, U7-ch120, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 89
Mean 33.44
Std Dev 8.972
Entry
ampl
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2
4
6
8
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0
10
20
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40
50
60
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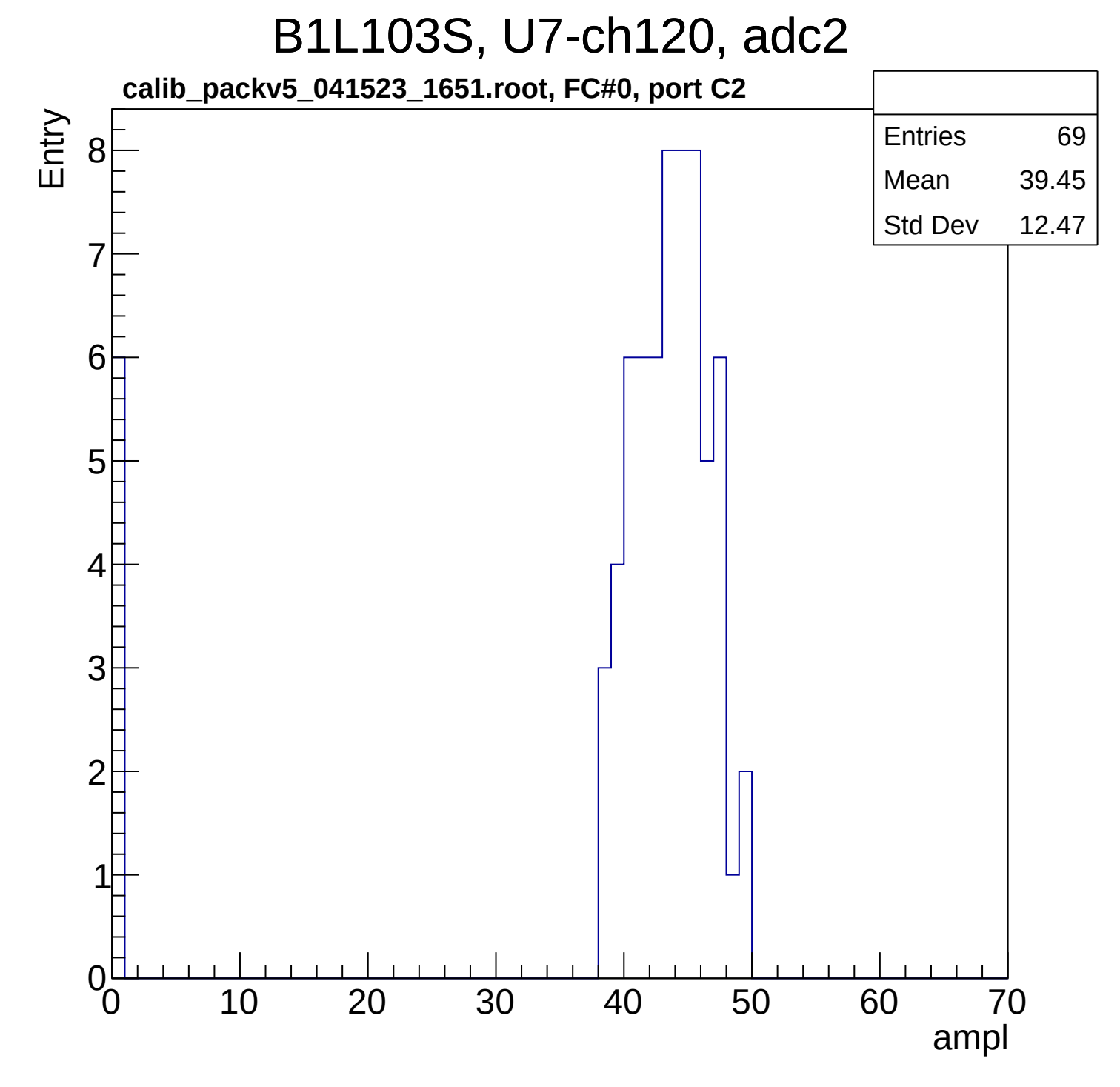
B1L103S, U7-ch120, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 39.45
Std Dev 12.47
Entry
ampl
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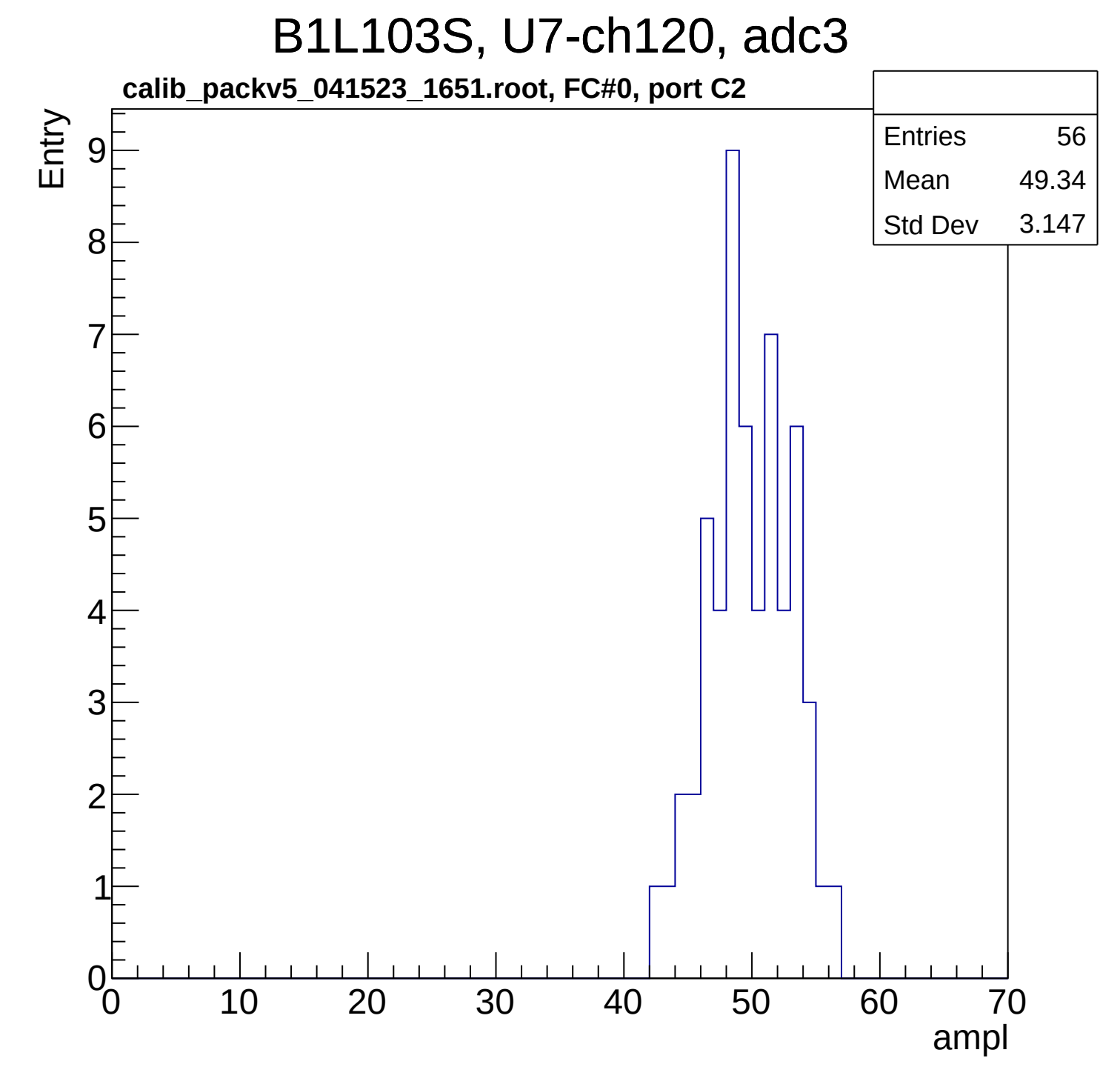
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch120, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 49.34
Std Dev 3.147
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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30
40
50
60
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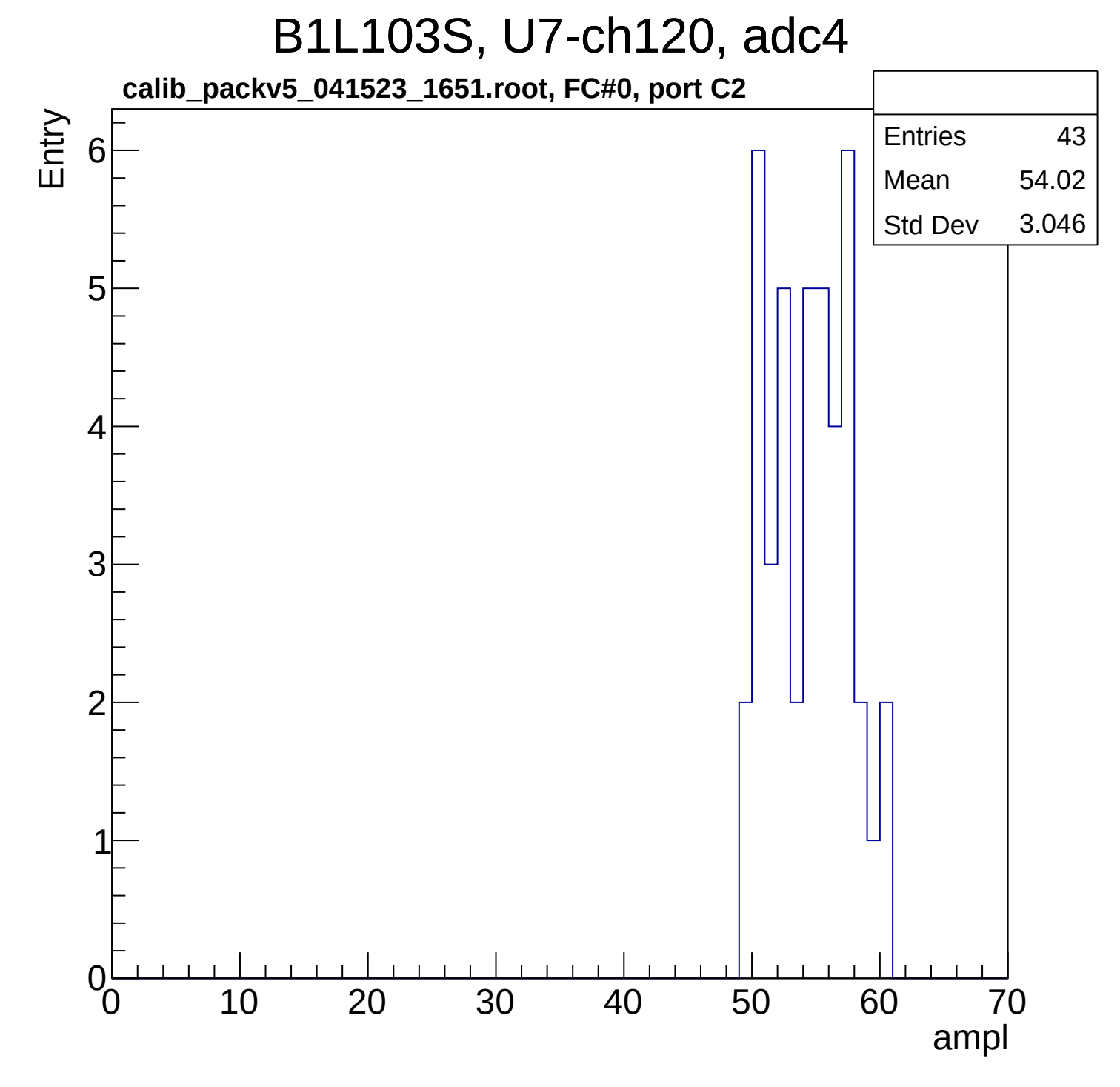
B1L103S, U7-ch120, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 43
Mean 54.02
Std Dev 3.046
Entry
ampl
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1
2
3
4
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0
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60
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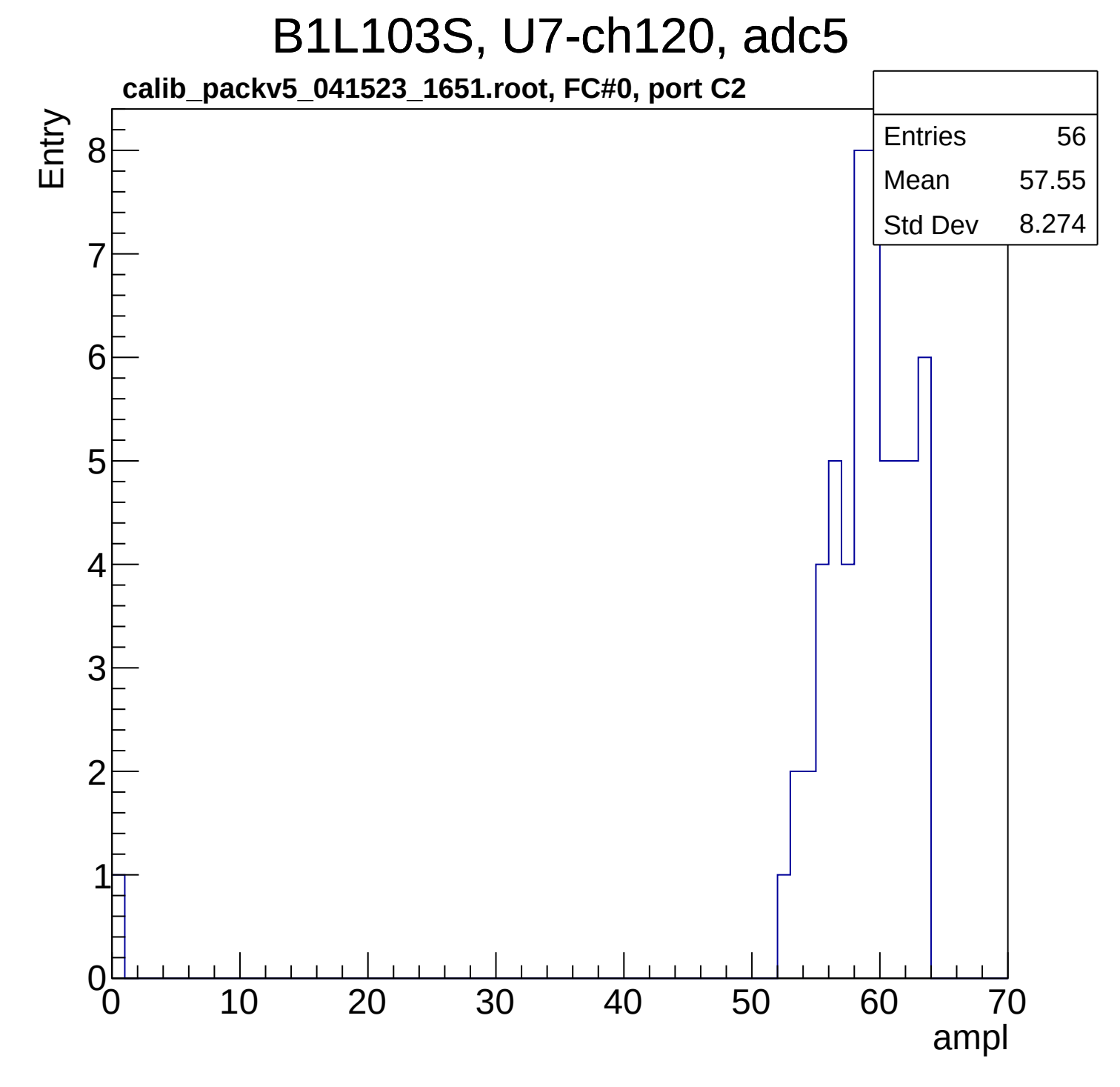
B1L103S, U7-ch120, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 57.55
Std Dev 8.274
Entry
ampl
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2
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4
5
6
7
8
0
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40
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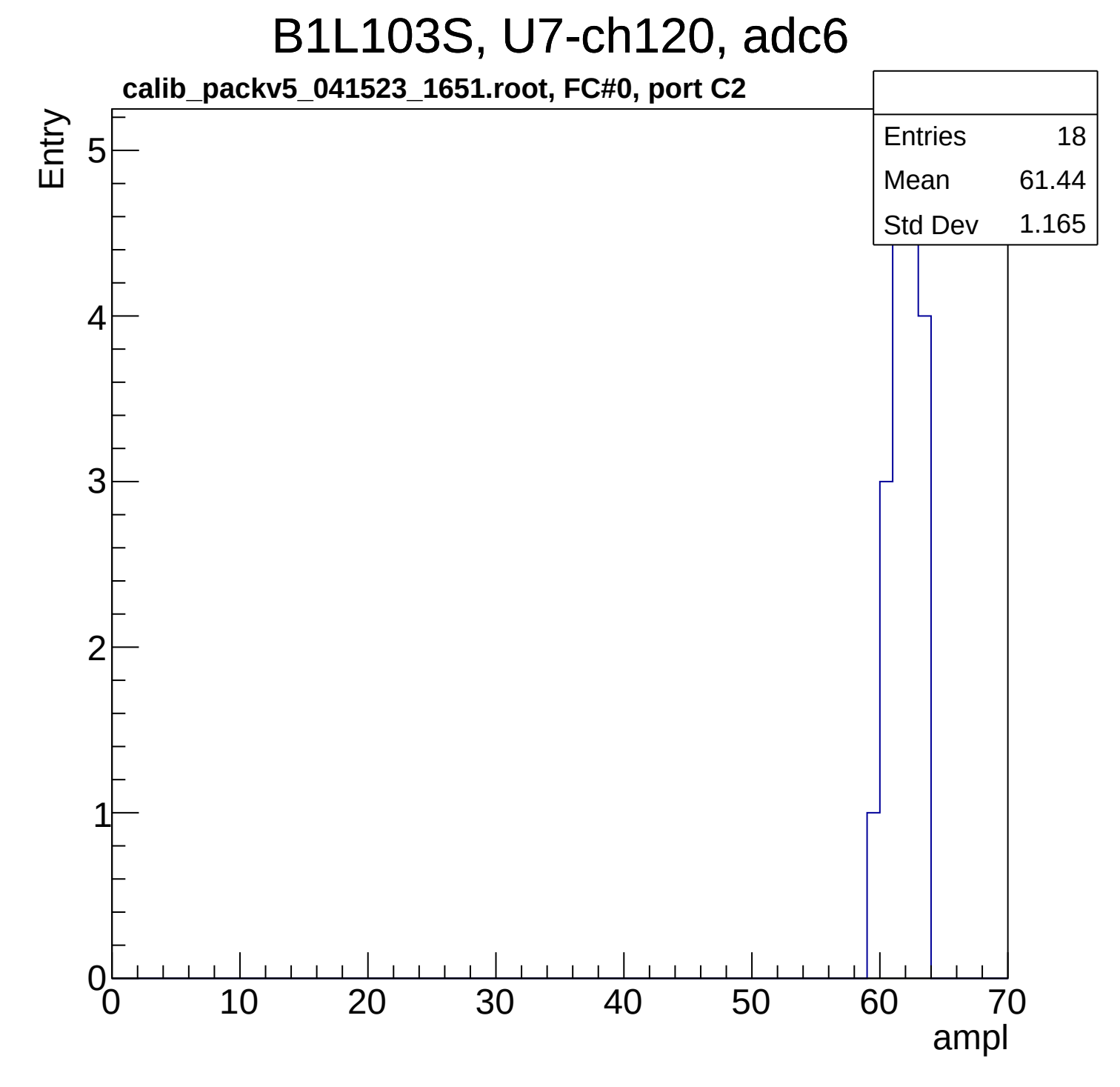
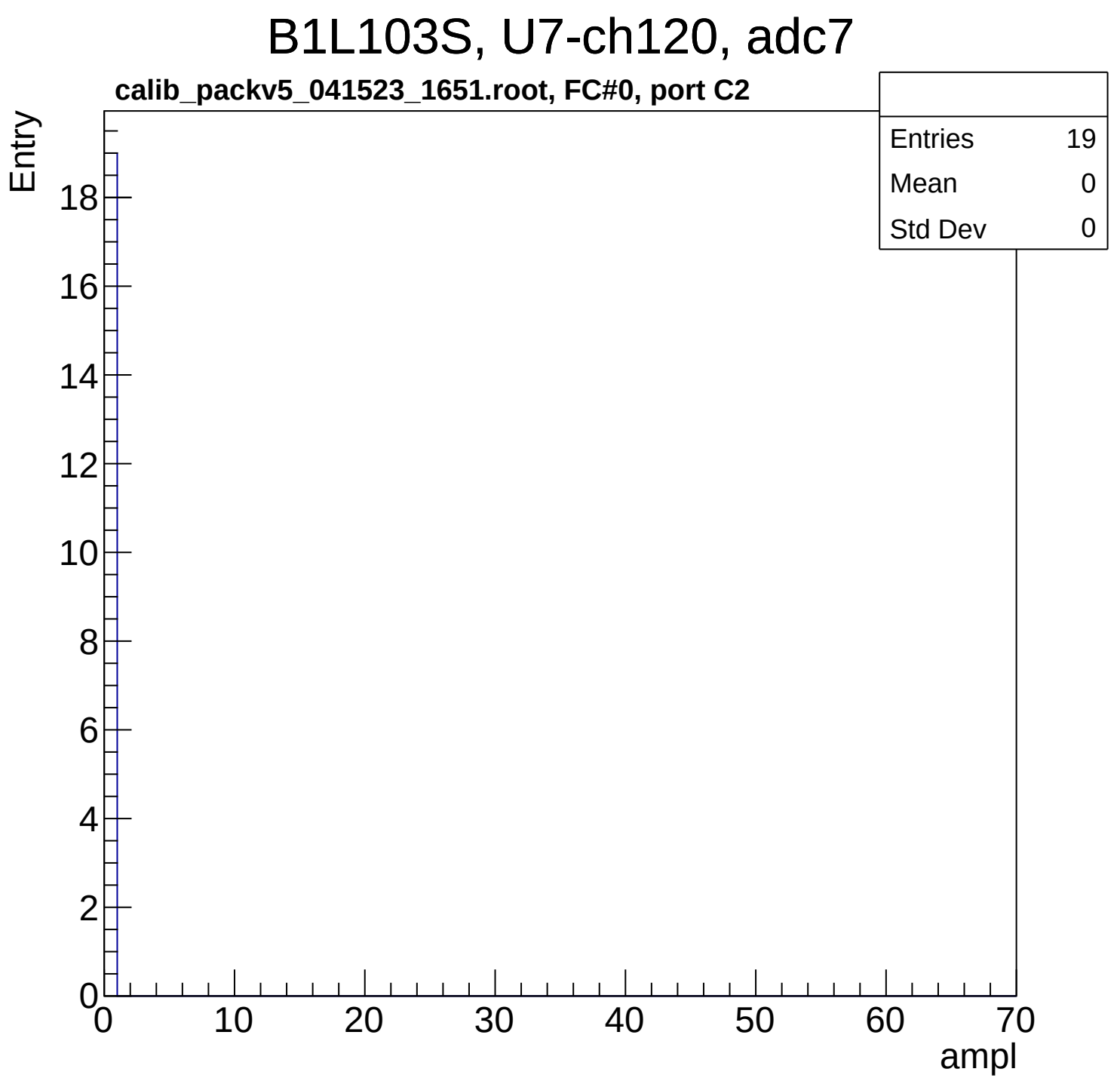
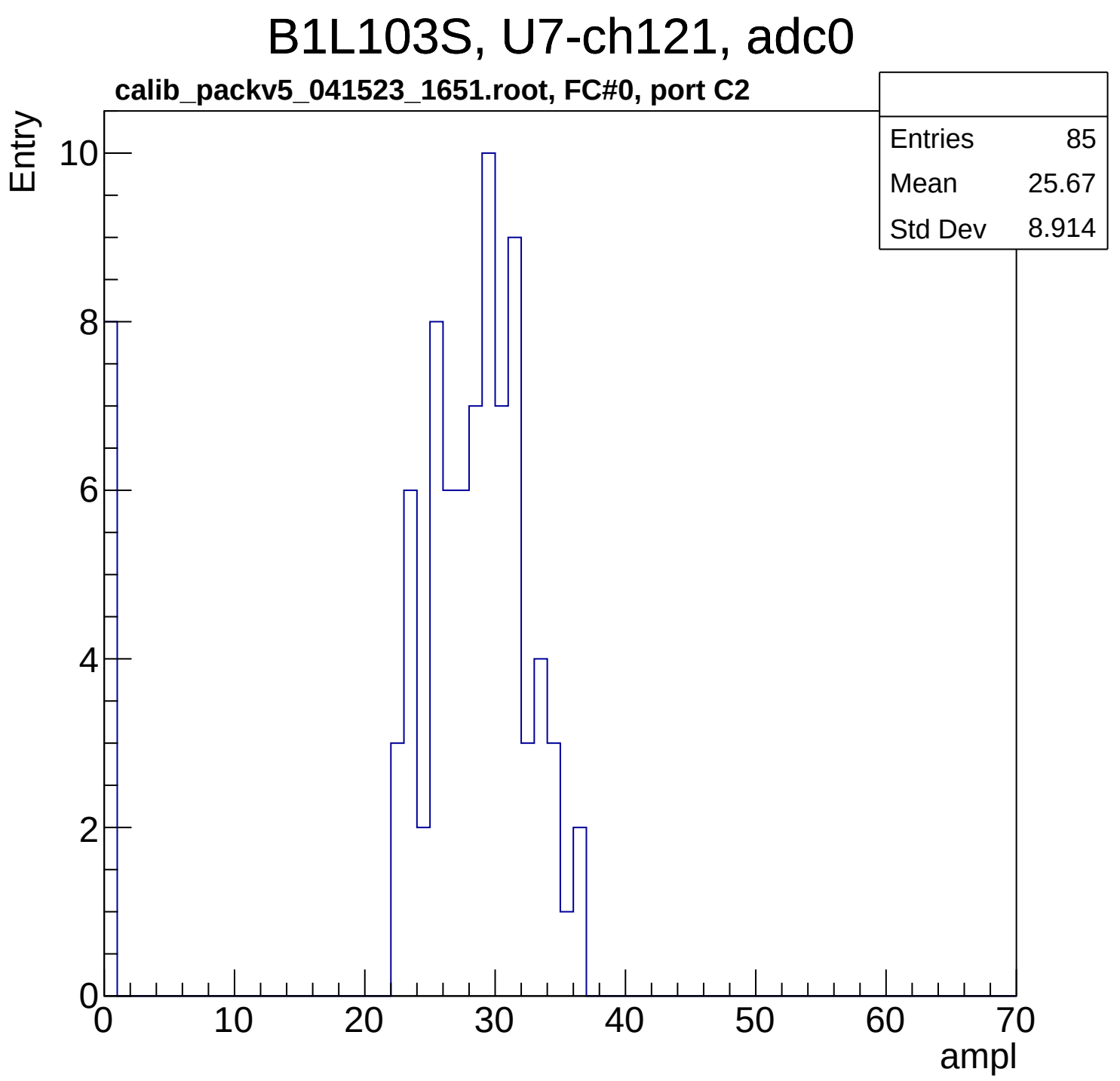

B1L103S, U7-ch120, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 61.44
Std Dev 1.165
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U7-ch120, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch121, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 25.67
Std Dev 8.914
Entry
0
2
4
6
8
10
0
10
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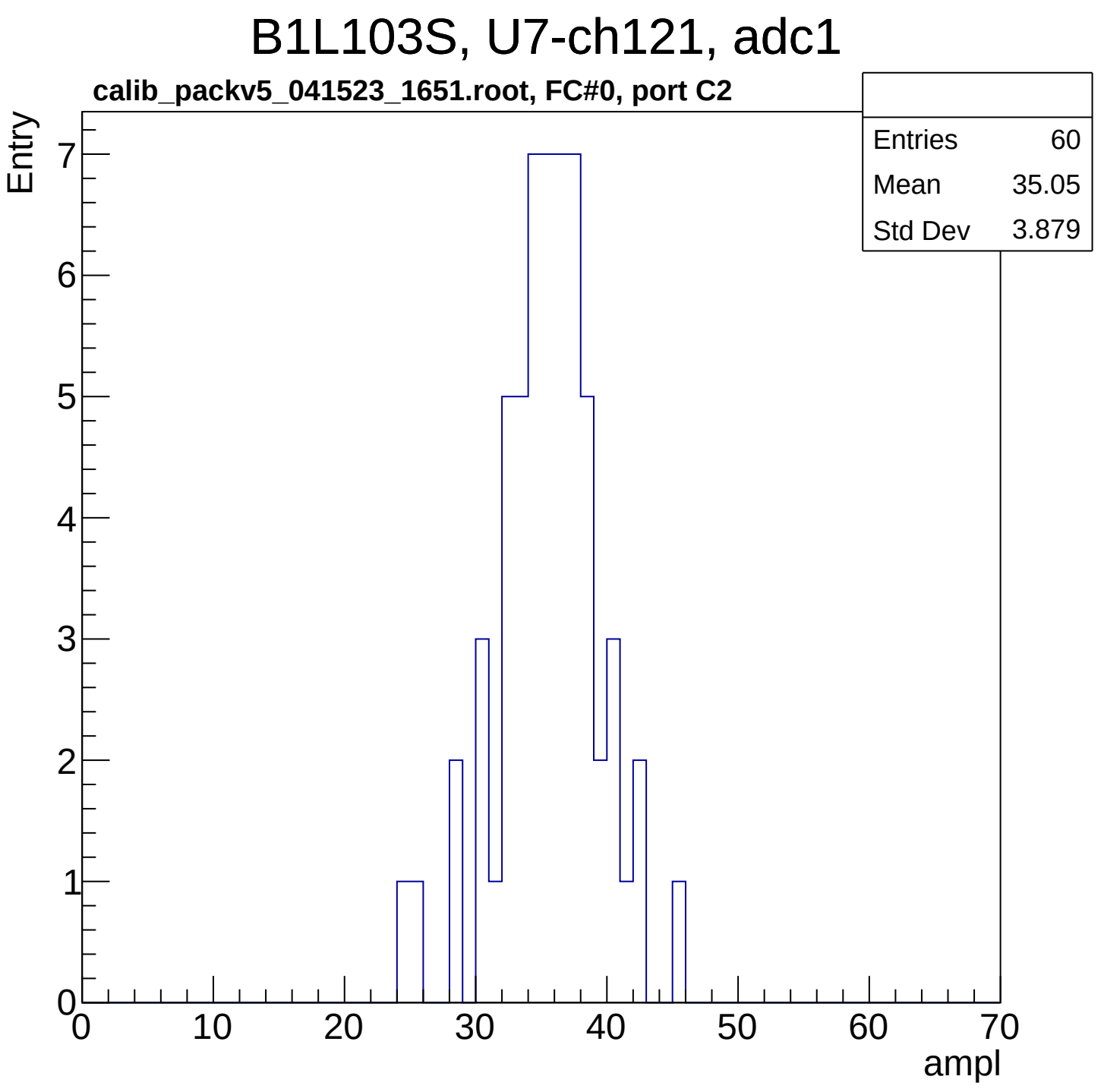
50
60
70
ampl


B1L103S, U7-ch121, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 35.05
Std Dev 3.879
Entry
ampl
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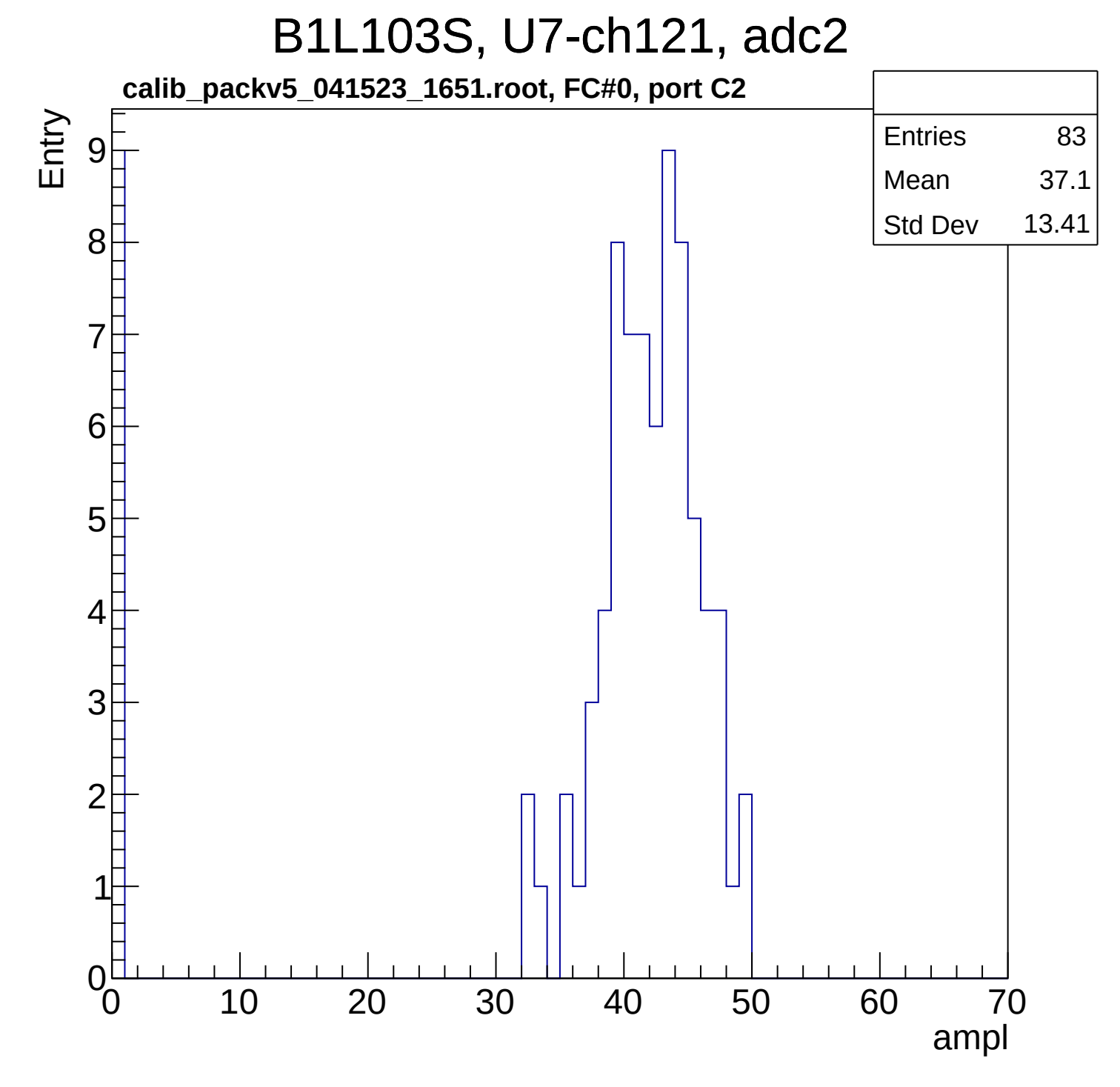
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U7-ch121, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 37.1
Std Dev 13.41
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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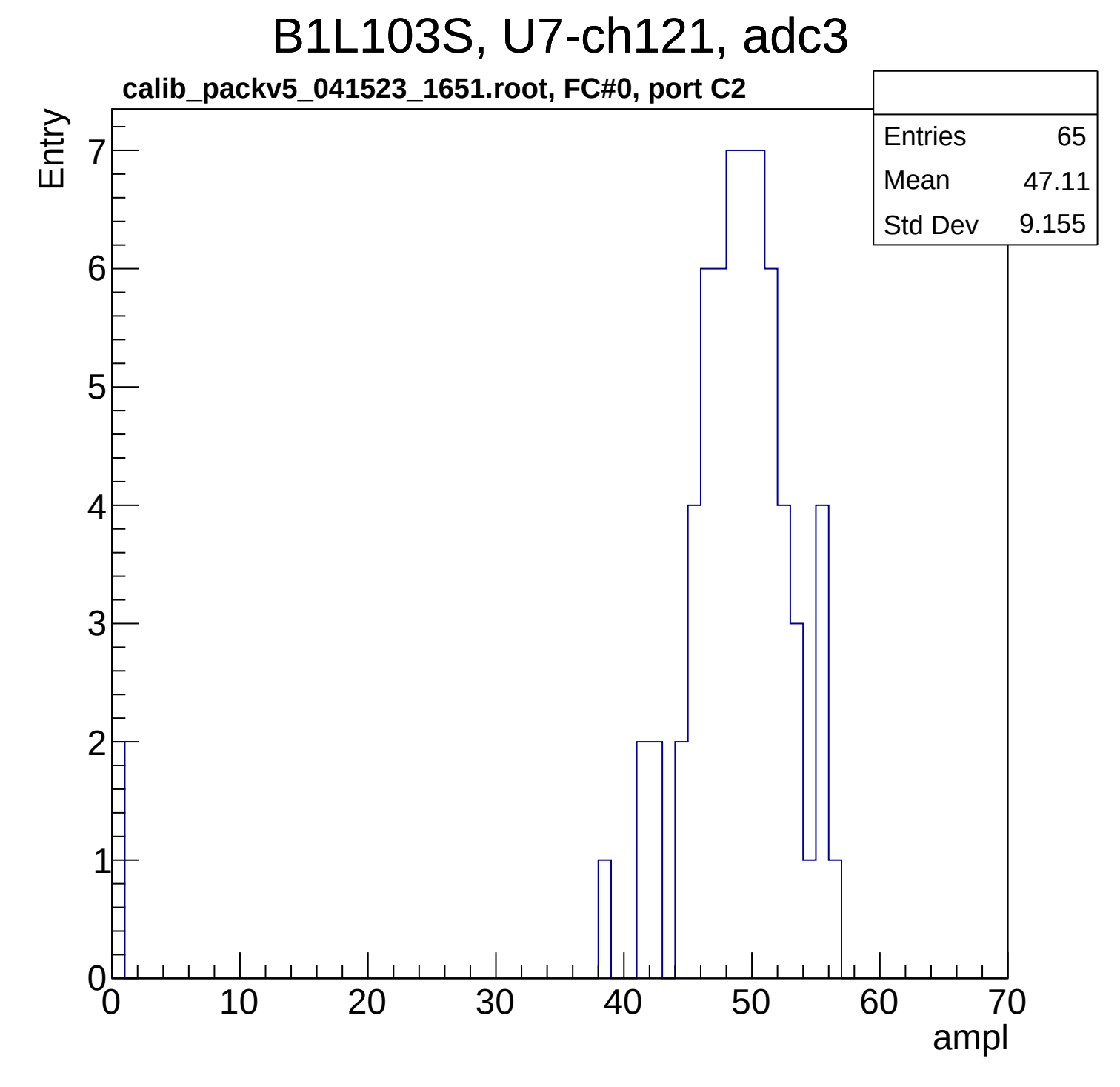
40
50
60
70


B1L103S, U7-ch121, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 47.11
Std Dev 9.155
Entry
ampl
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1
2
3
4
5
6
7
0
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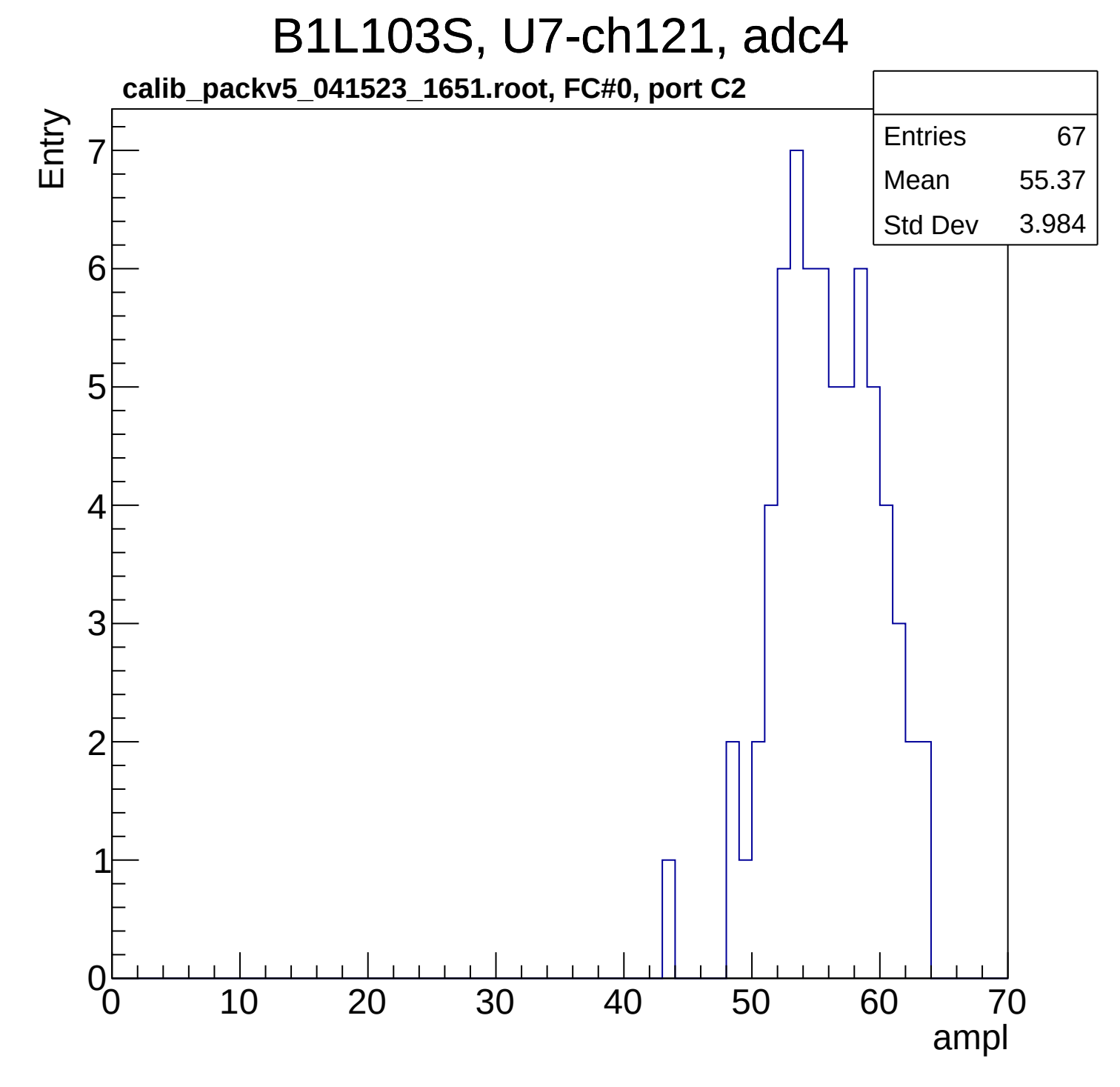
40
50
60
70


B1L103S, U7-ch121, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 55.37
Std Dev 3.984
Entry
ampl
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1
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3
4
5
6
7
0
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20
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40
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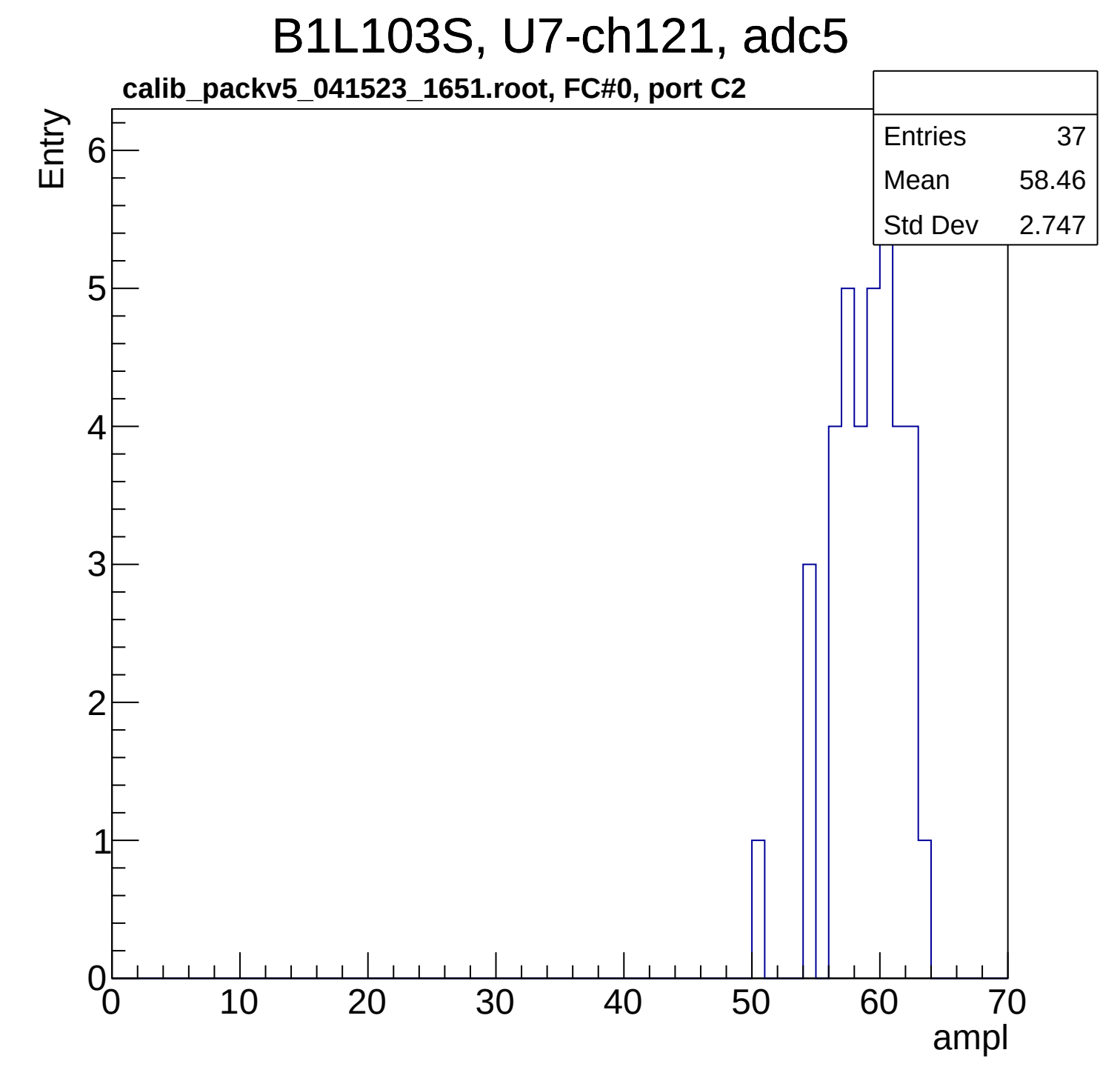
60
70


B1L103S, U7-ch121, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 37
Mean 58.46
Std Dev 2.747
Entry
ampl
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1
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0
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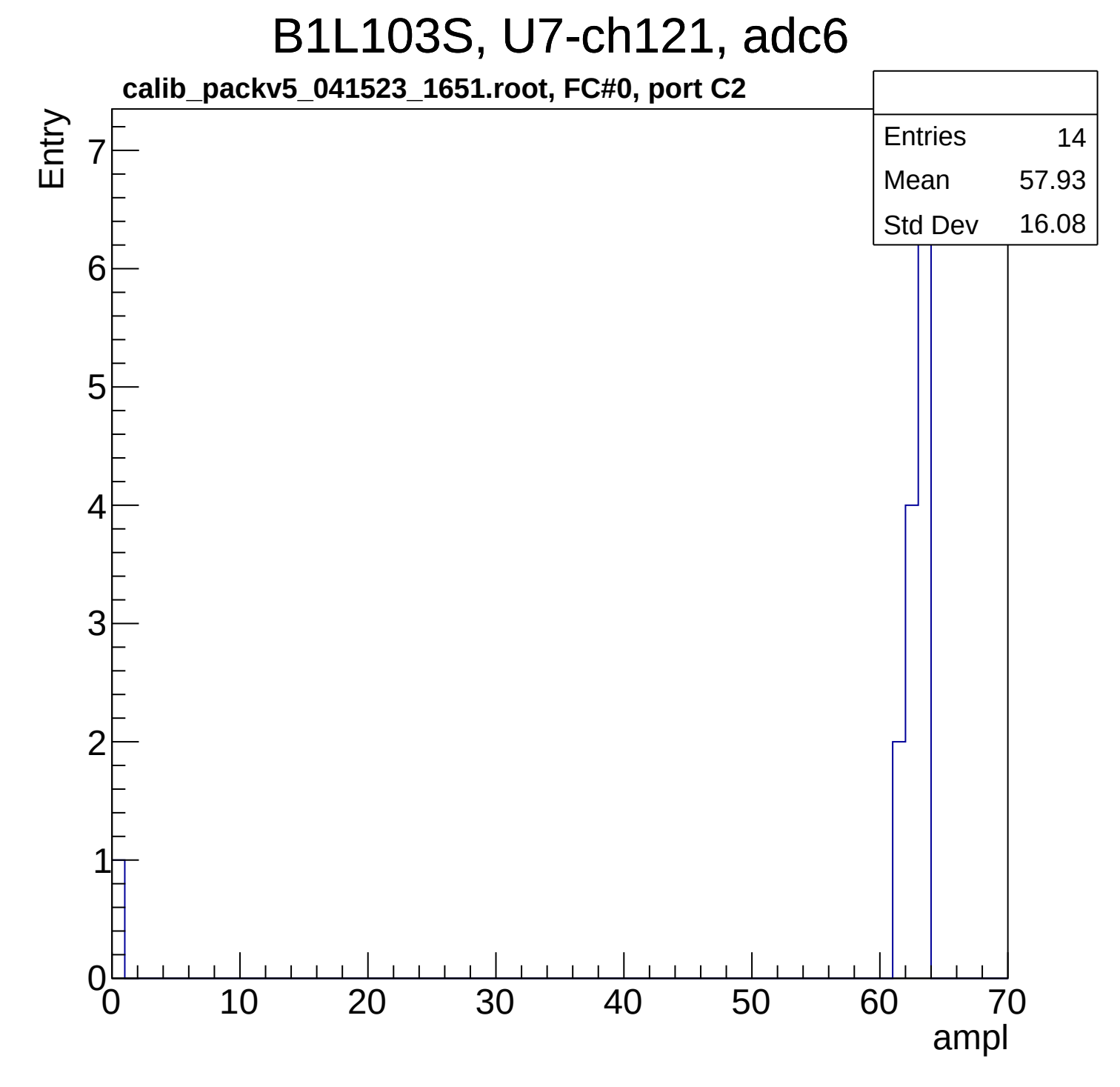
B1L103S, U7-ch121, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 14
Mean 57.93
Std Dev 16.08
Entry
ampl
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2
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4
5
6
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0
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40
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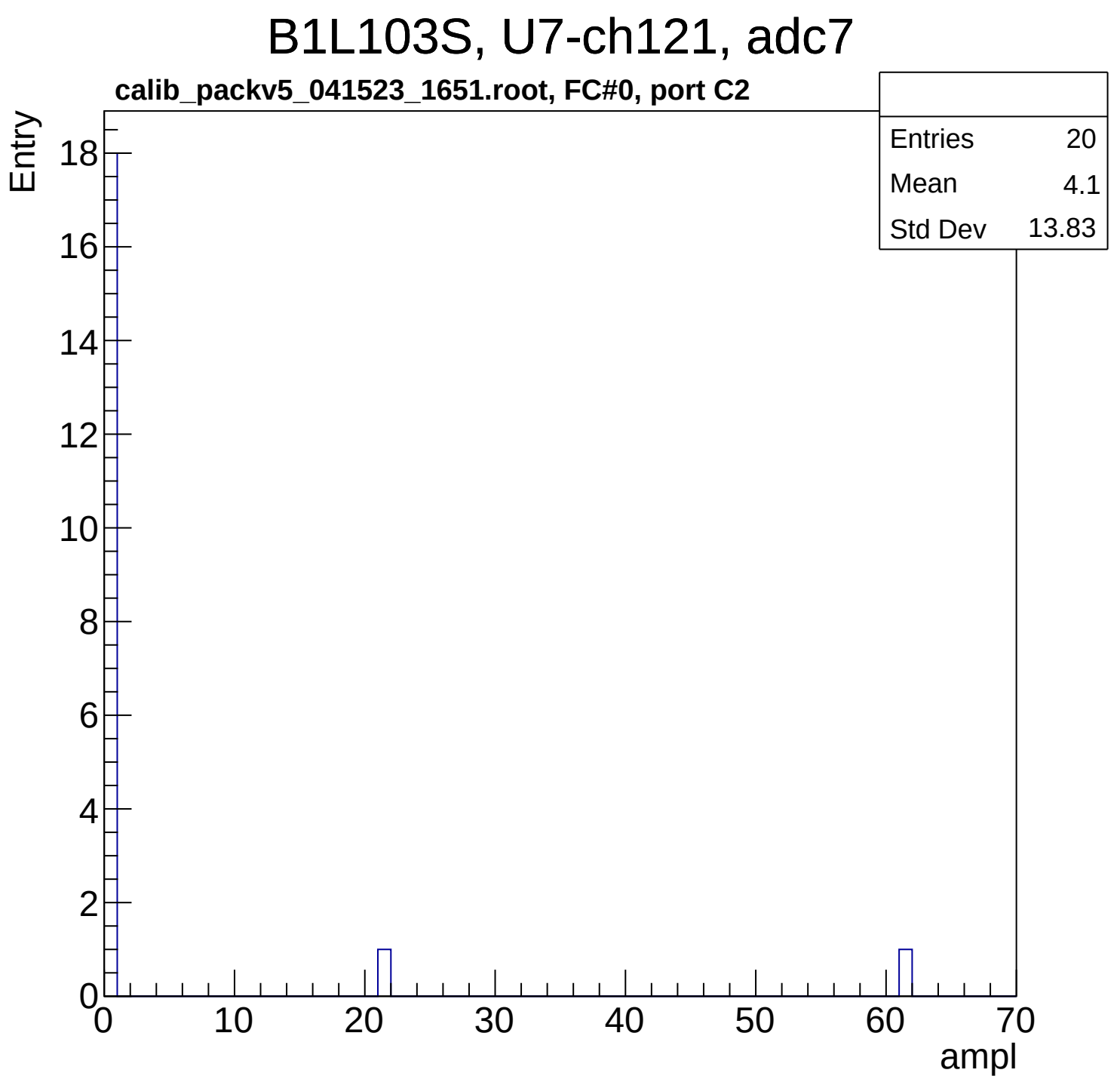
B1L103S, U7-ch121, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 4.1
Std Dev 13.83
Entry
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6
8
10
12
14
16
18
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10
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30
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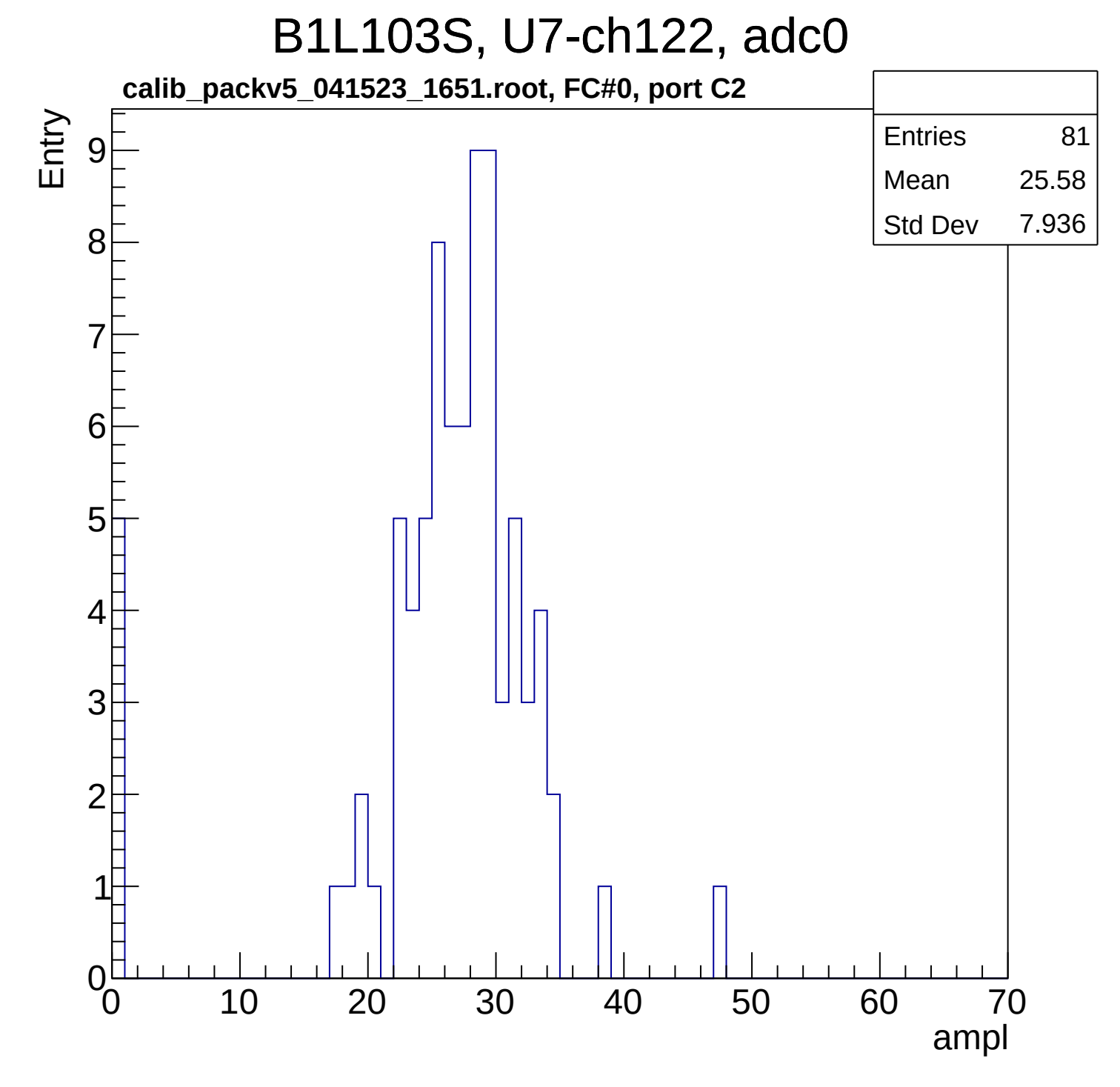
70
ampl


B1L103S, U7-ch122, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 25.58
Std Dev 7.936
Entry
ampl
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2
3
4
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6
7
8
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0
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60
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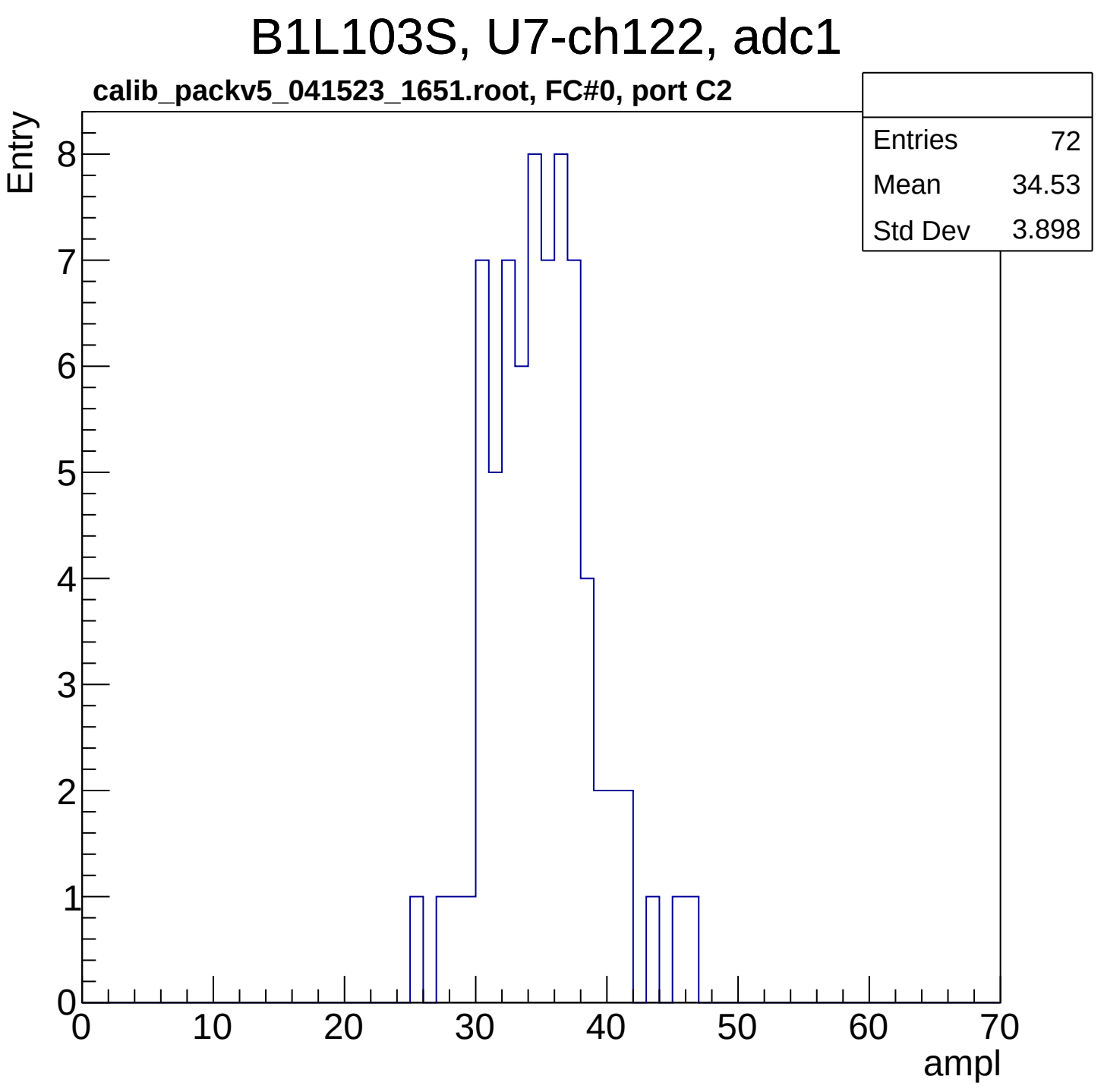
B1L103S, U7-ch122, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 34.53
Std Dev 3.898
Entry
ampl
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2
3
4
5
6
7
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0
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20
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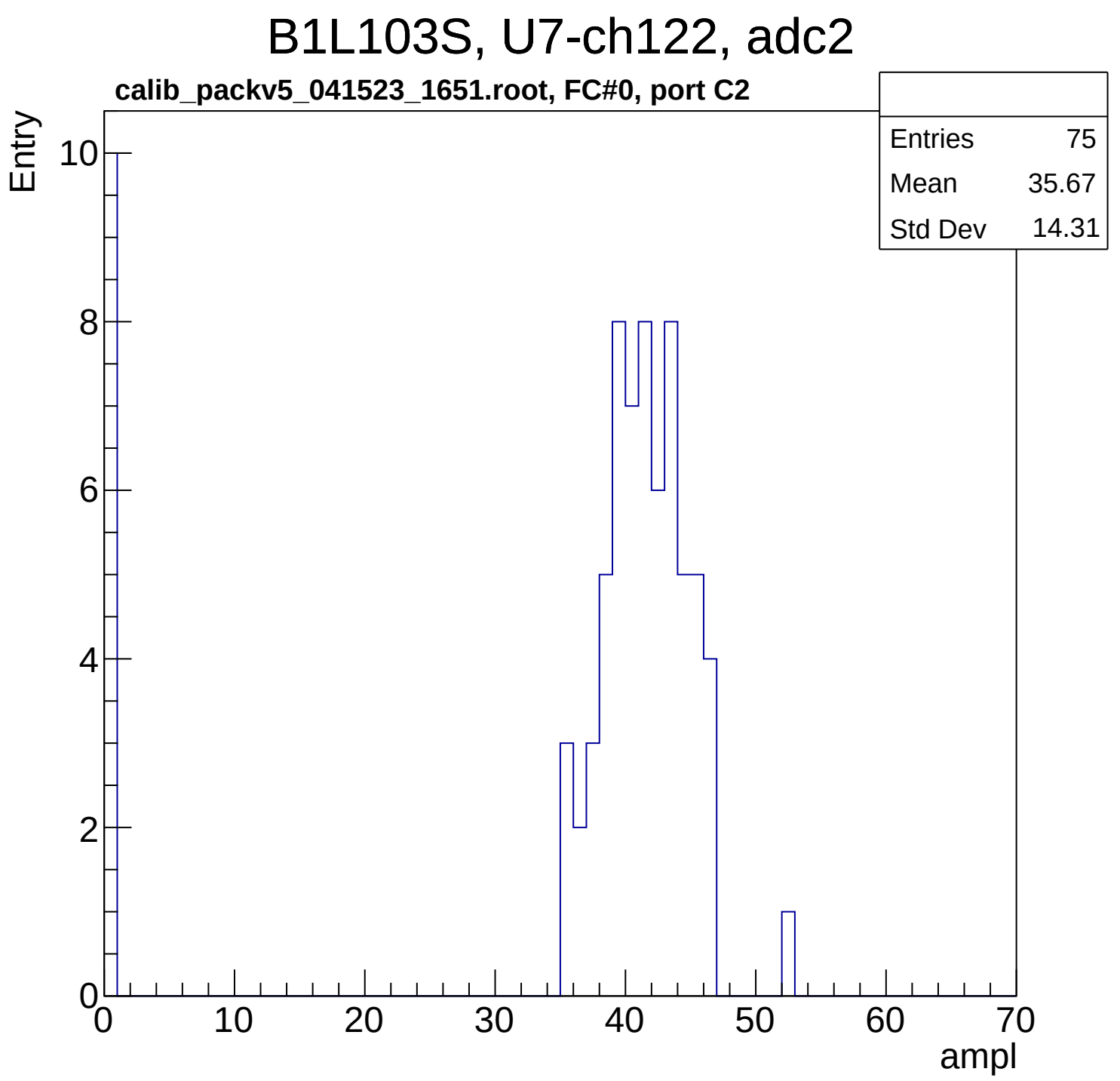
40
50
60
70


B1L103S, U7-ch122, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 35.67
Std Dev 14.31
Entry
0
2
4
6
8
10
0
10
20
30
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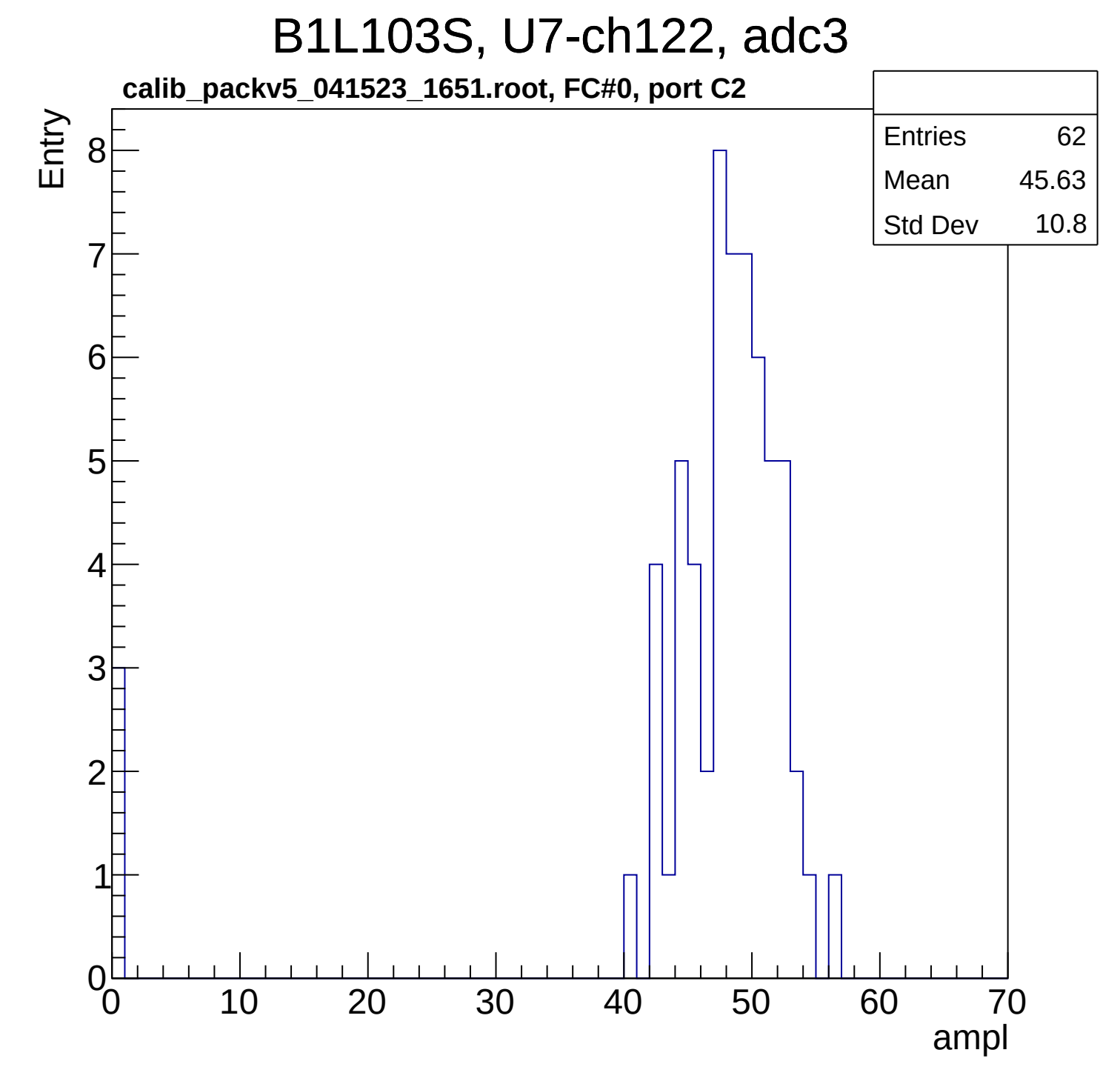
50
60
70
ampl


B1L103S, U7-ch122, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 45.63
Std Dev 10.8
Entry
ampl
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1
2
3
4
5
6
7
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0
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60
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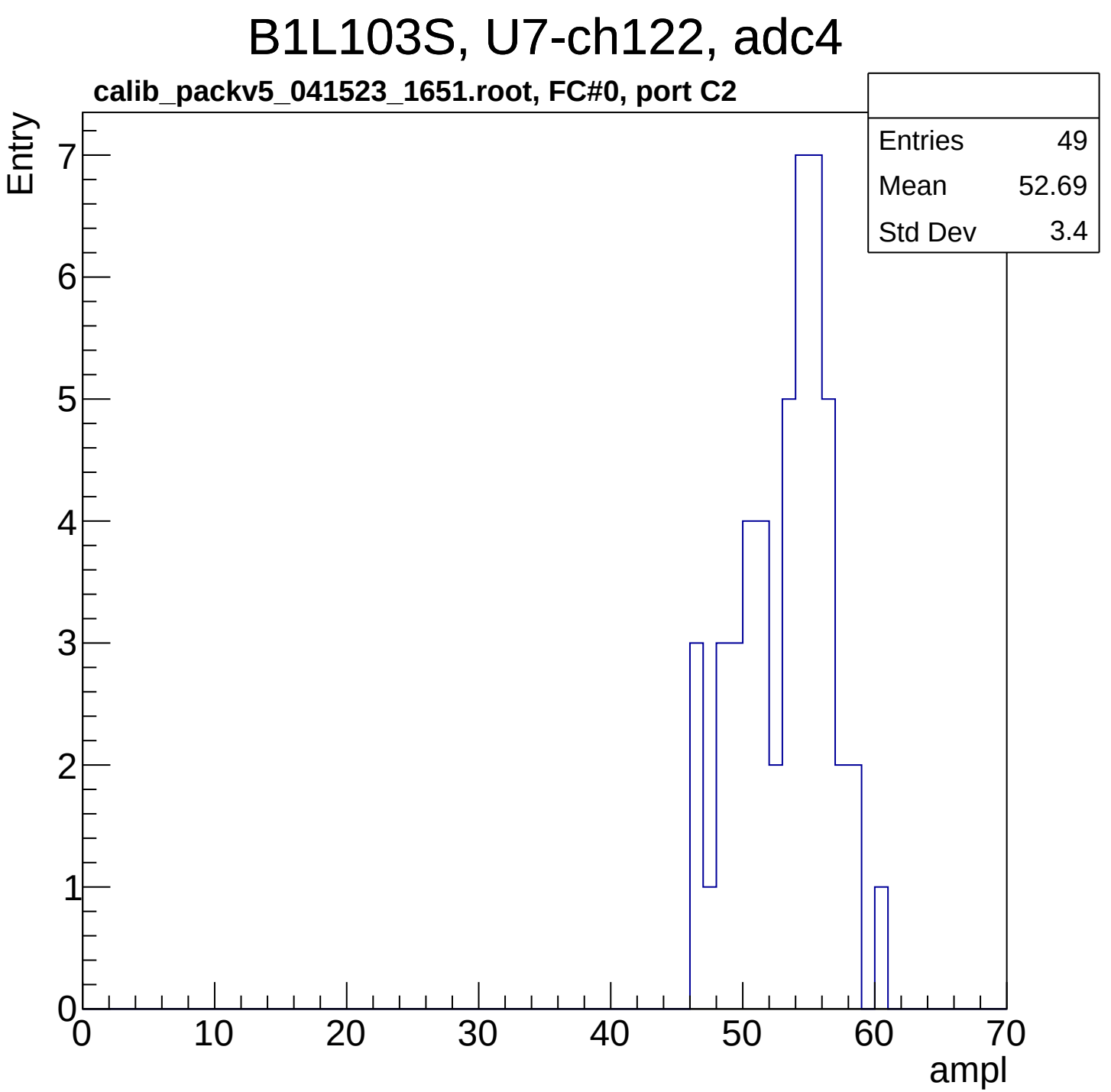
B1L103S, U7-ch122, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 52.69
Std Dev 3.4
Entry
ampl
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2
3
4
5
6
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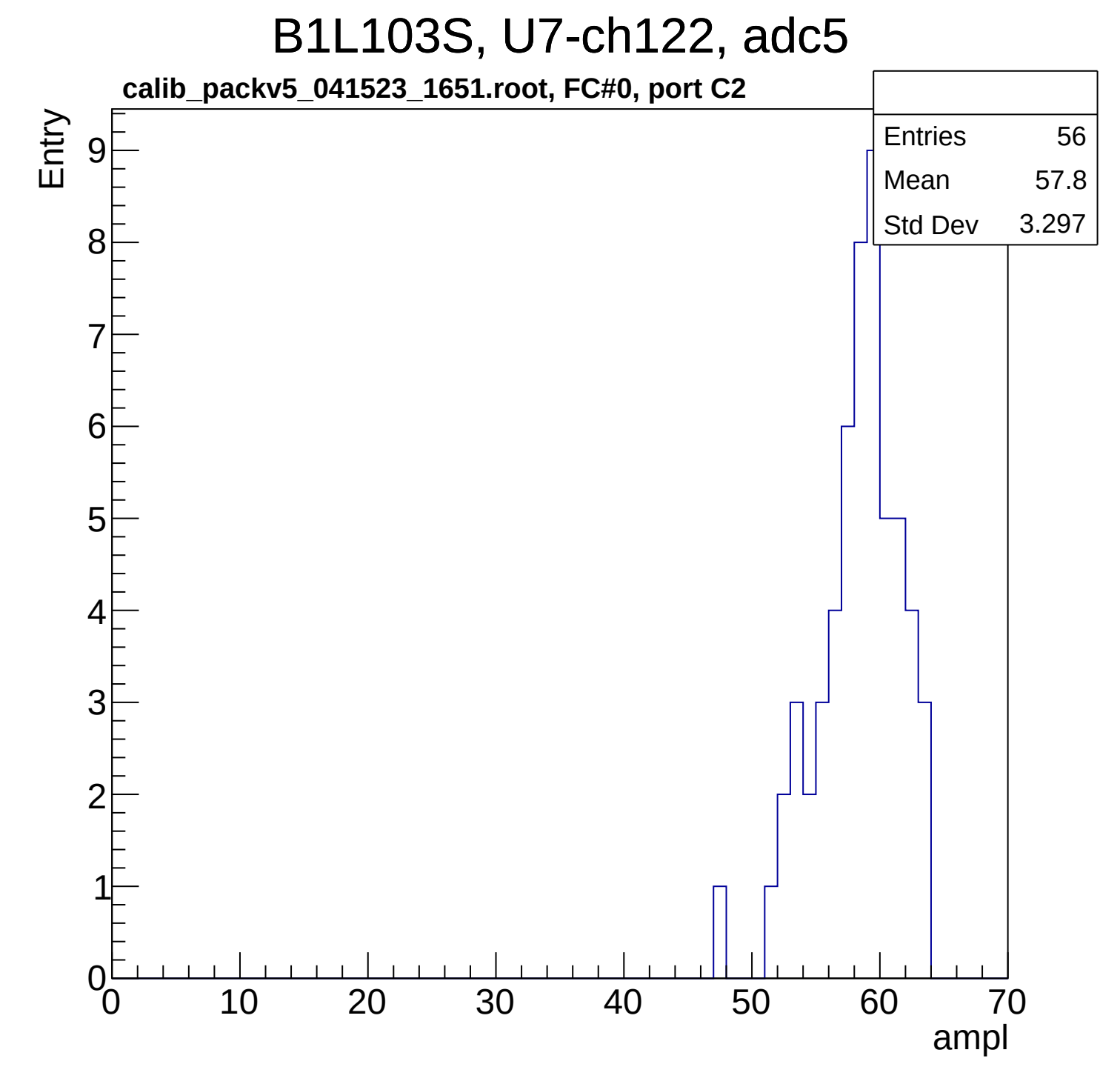
B1L103S, U7-ch122, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 57.8
Std Dev 3.297
Entry
ampl
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3
4
5
6
7
8
9
0
10
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40
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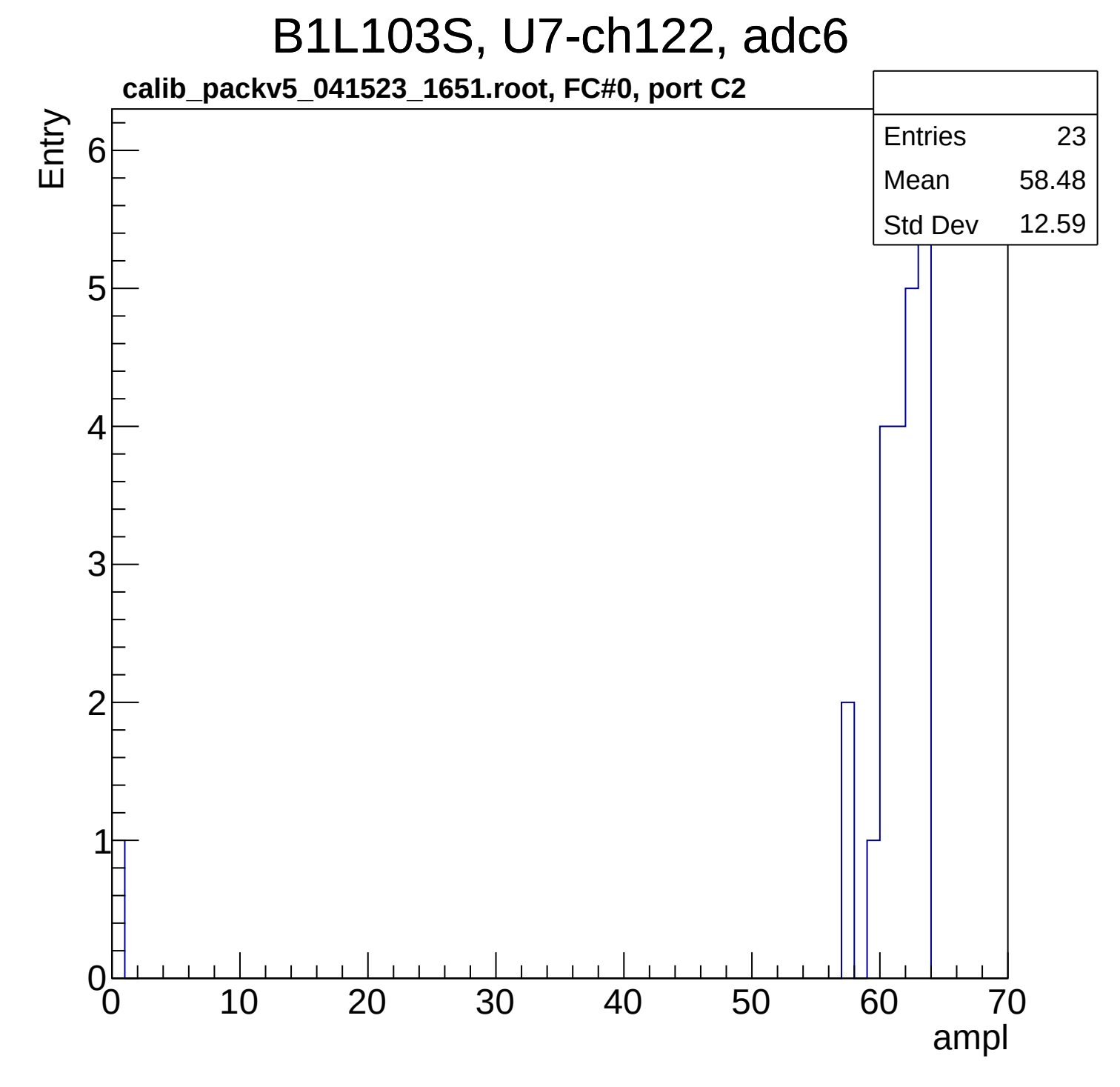
B1L103S, U7-ch122, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 23
Mean 58.48
Std Dev 12.59
Entry
ampl
0
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4
5
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0
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60
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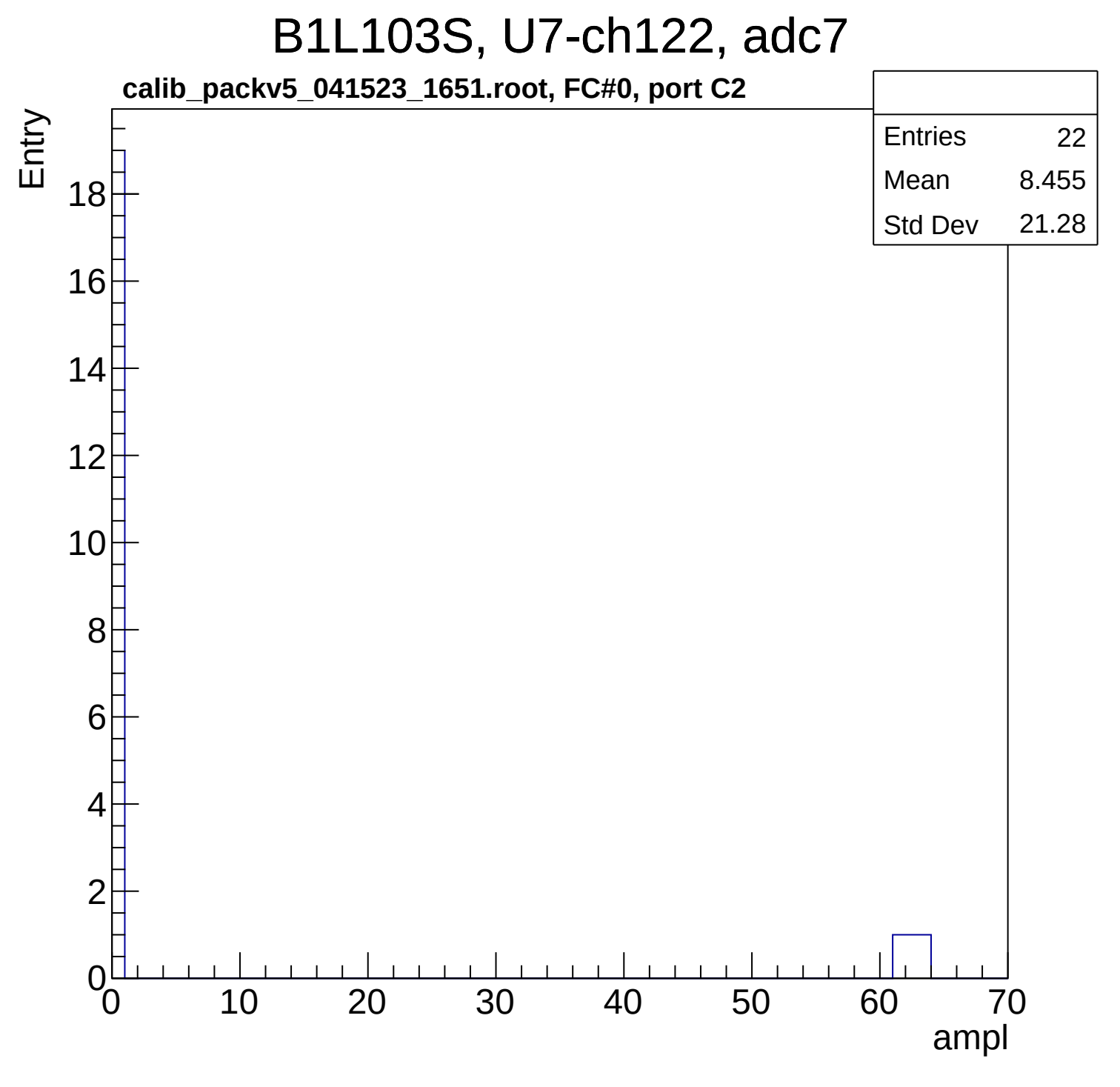
B1L103S, U7-ch122, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 8.455
Std Dev 21.28
Entry
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6
8
10
12
14
16
18
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10
20
30
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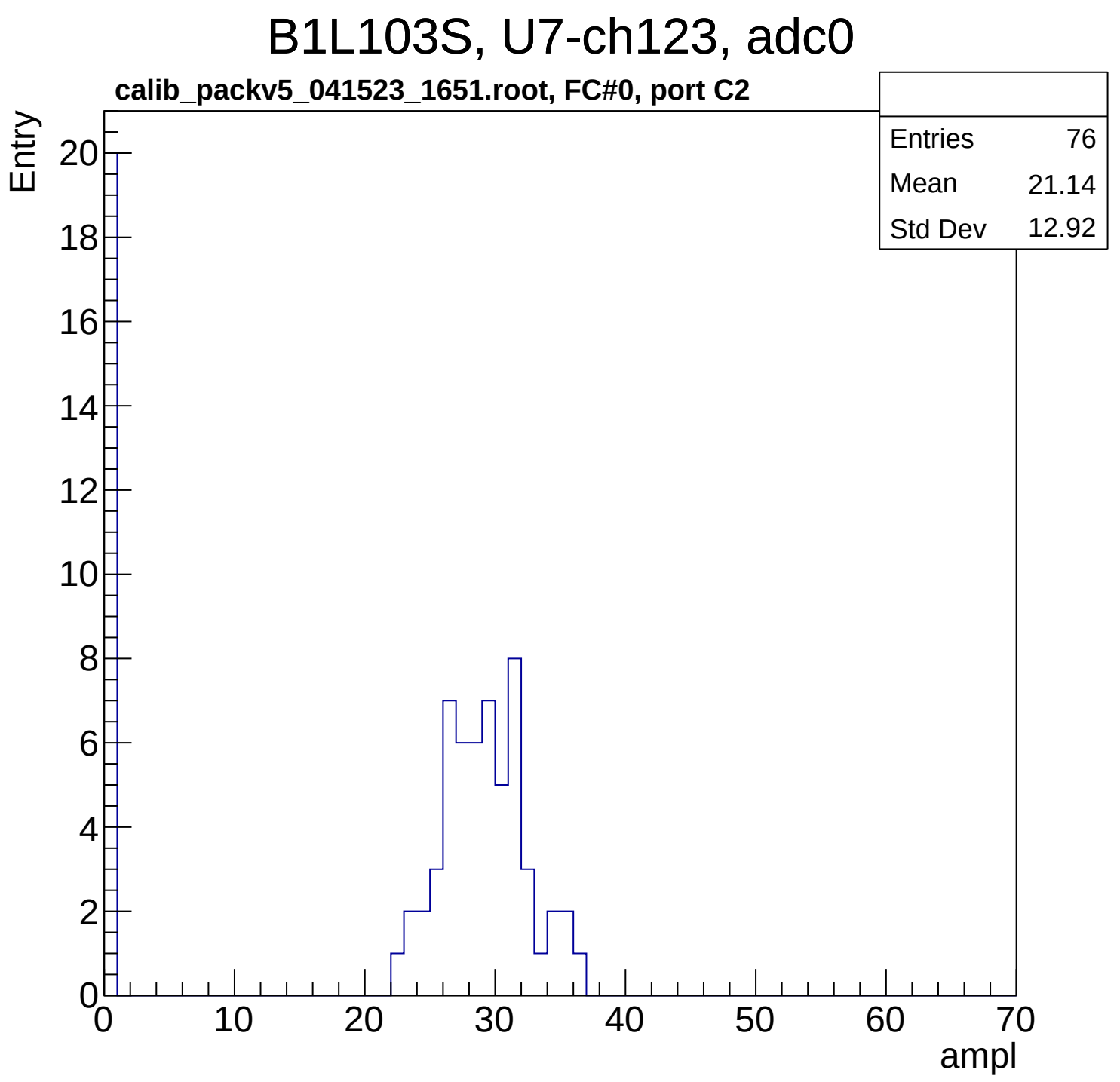
50
60
70
ampl


B1L103S, U7-ch123, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 21.14
Std Dev 12.92
Entry
ampl
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6
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10
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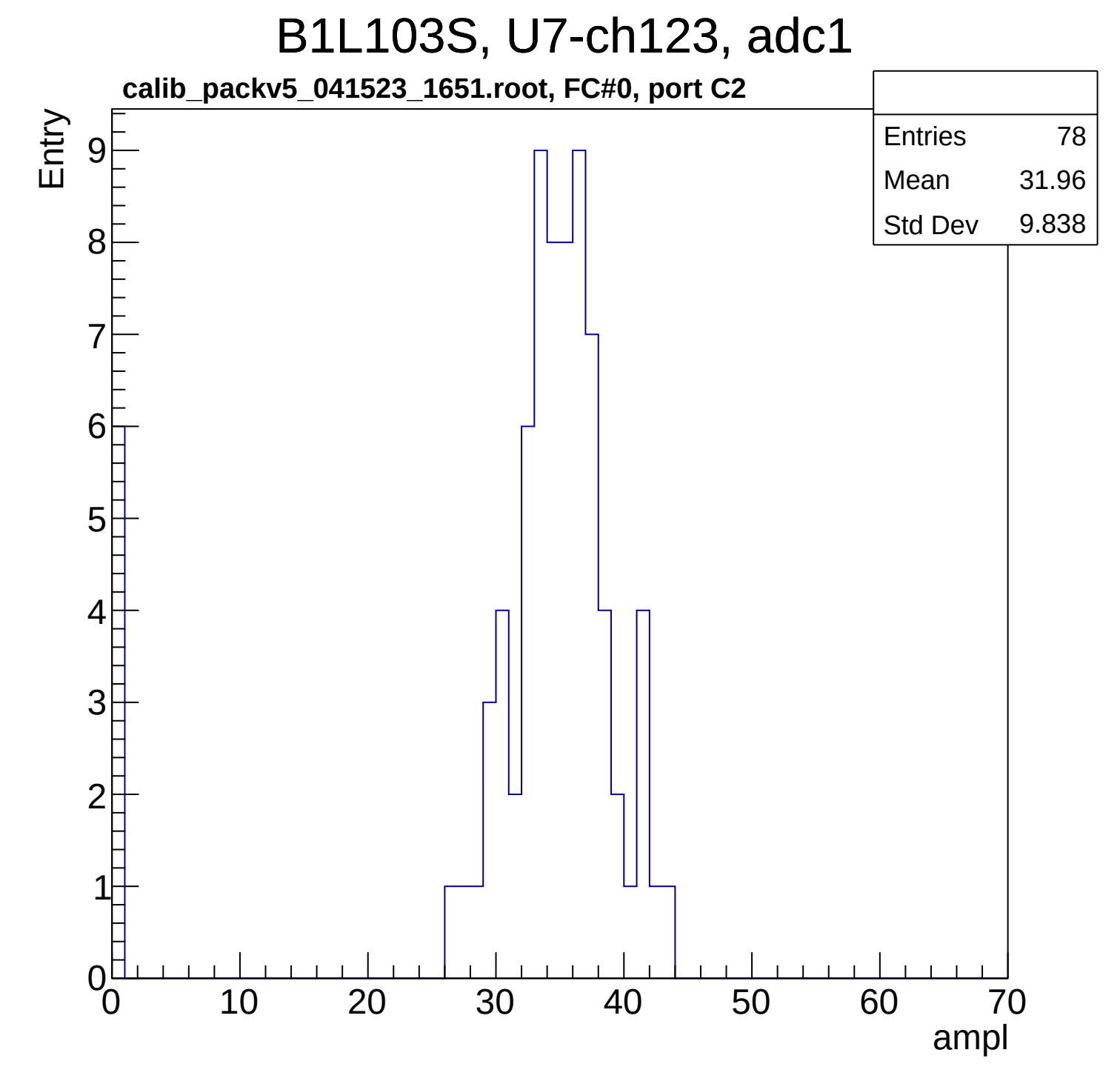
B1L103S, U7-ch123, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 31.96
Std Dev 9.838
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
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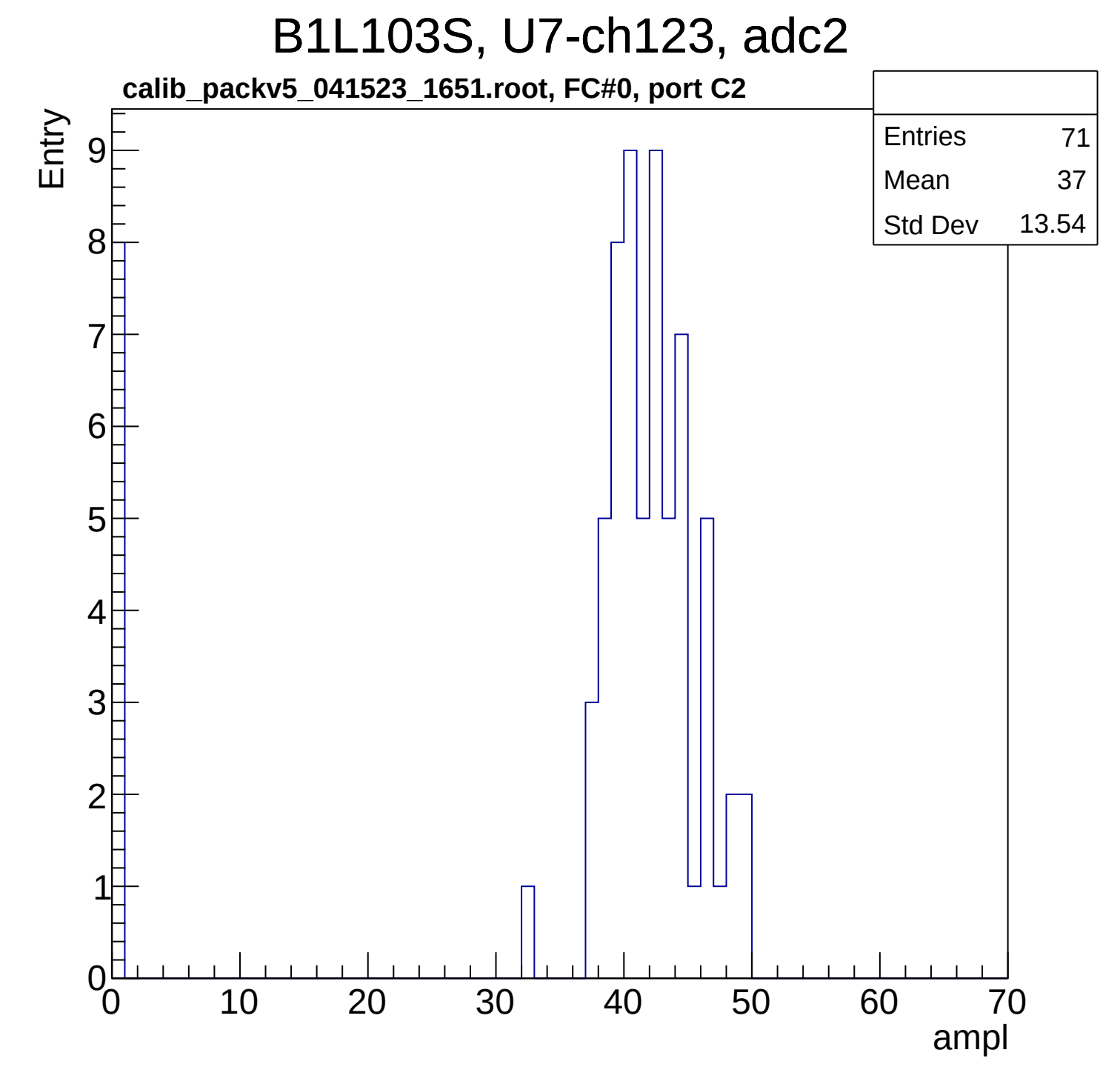
40
50
60
70


B1L103S, U7-ch123, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 37
Std Dev 13.54
Entry
ampl
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6
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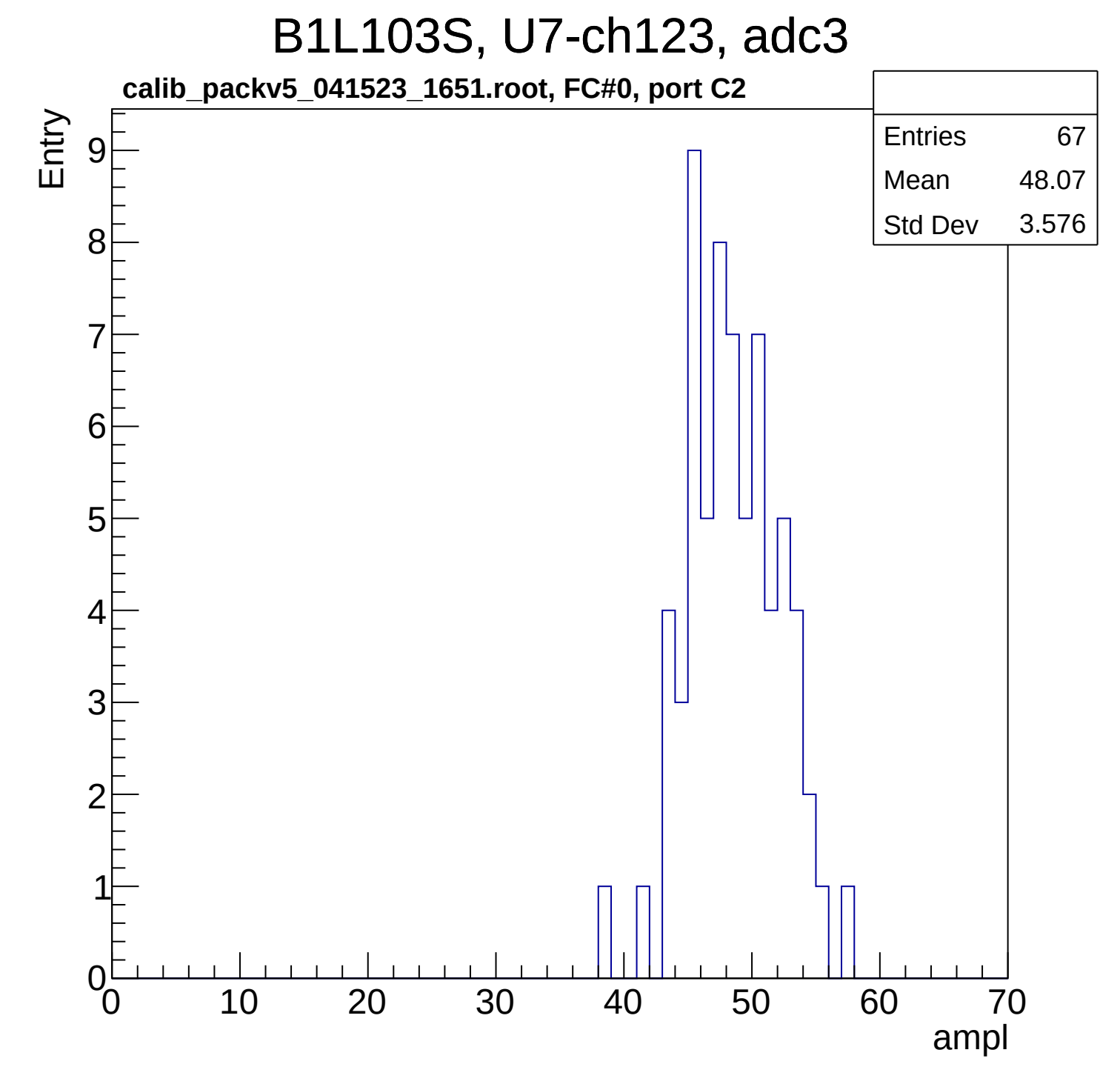
B1L103S, U7-ch123, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 48.07
Std Dev 3.576
Entry
ampl
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4
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6
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0
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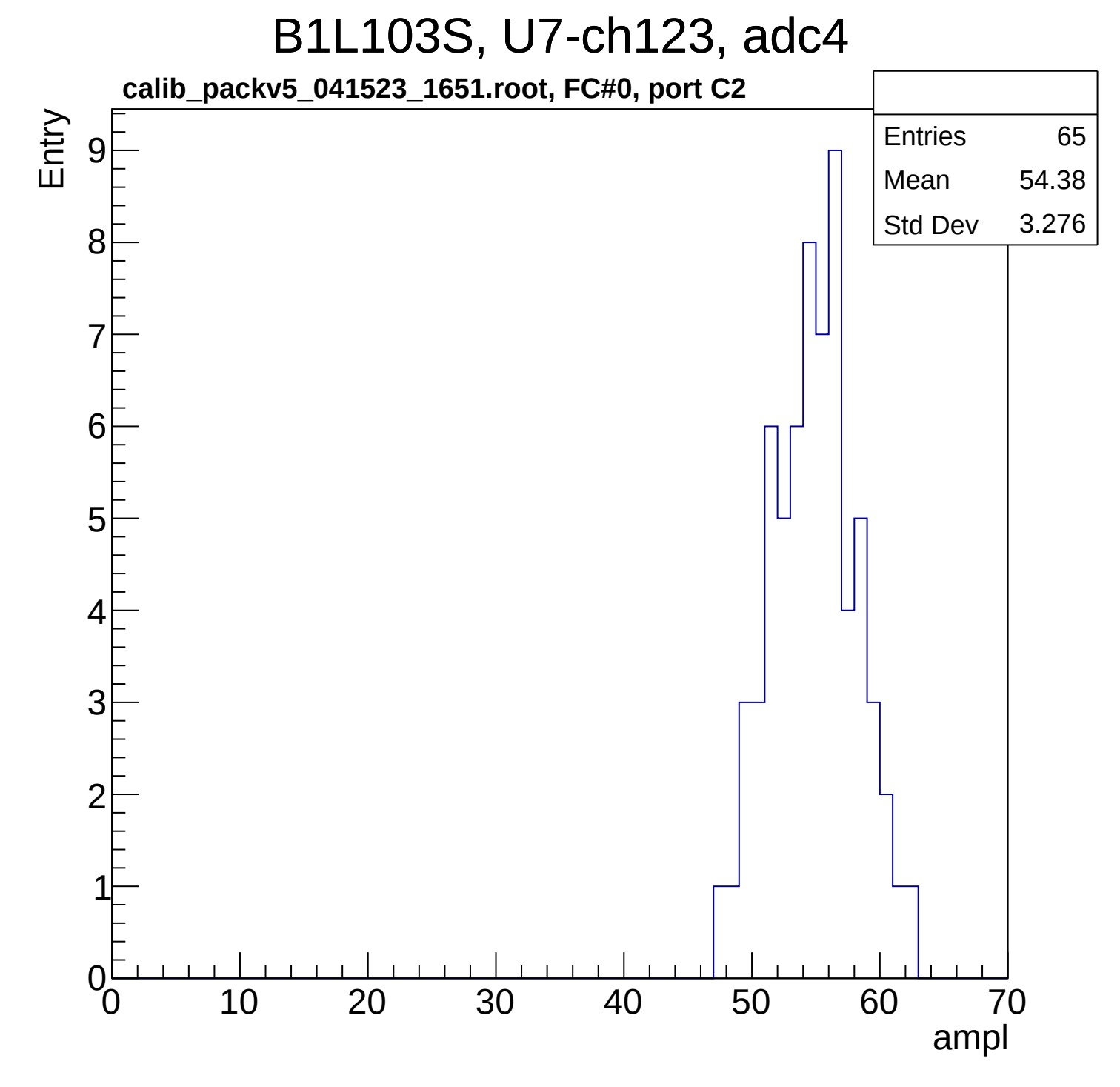
B1L103S, U7-ch123, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 54.38
Std Dev 3.276
Entry
ampl
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2
3
4
5
6
7
8
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0
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40
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60
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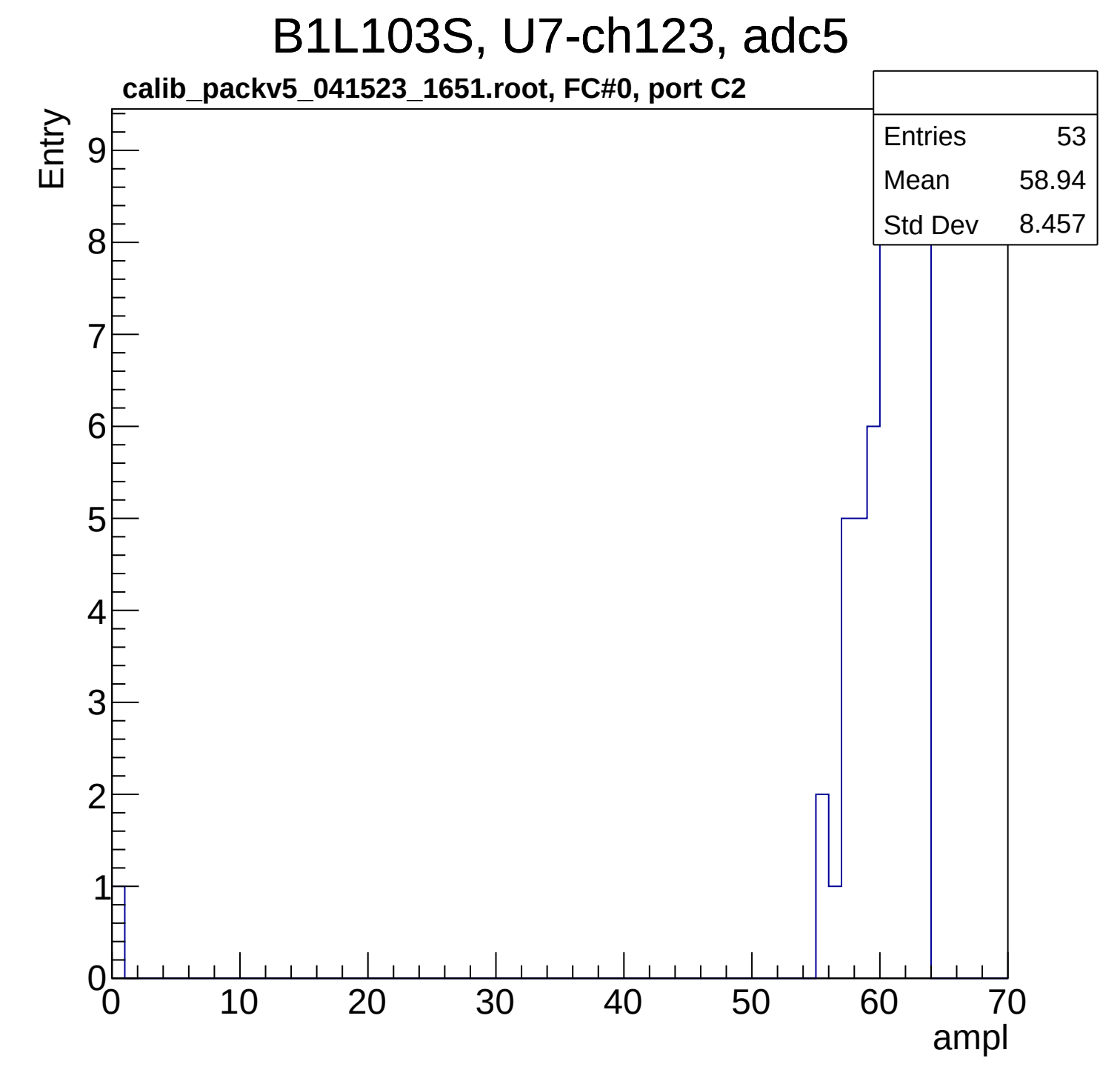
B1L103S, U7-ch123, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 58.94
Std Dev 8.457
Entry
ampl
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6
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0
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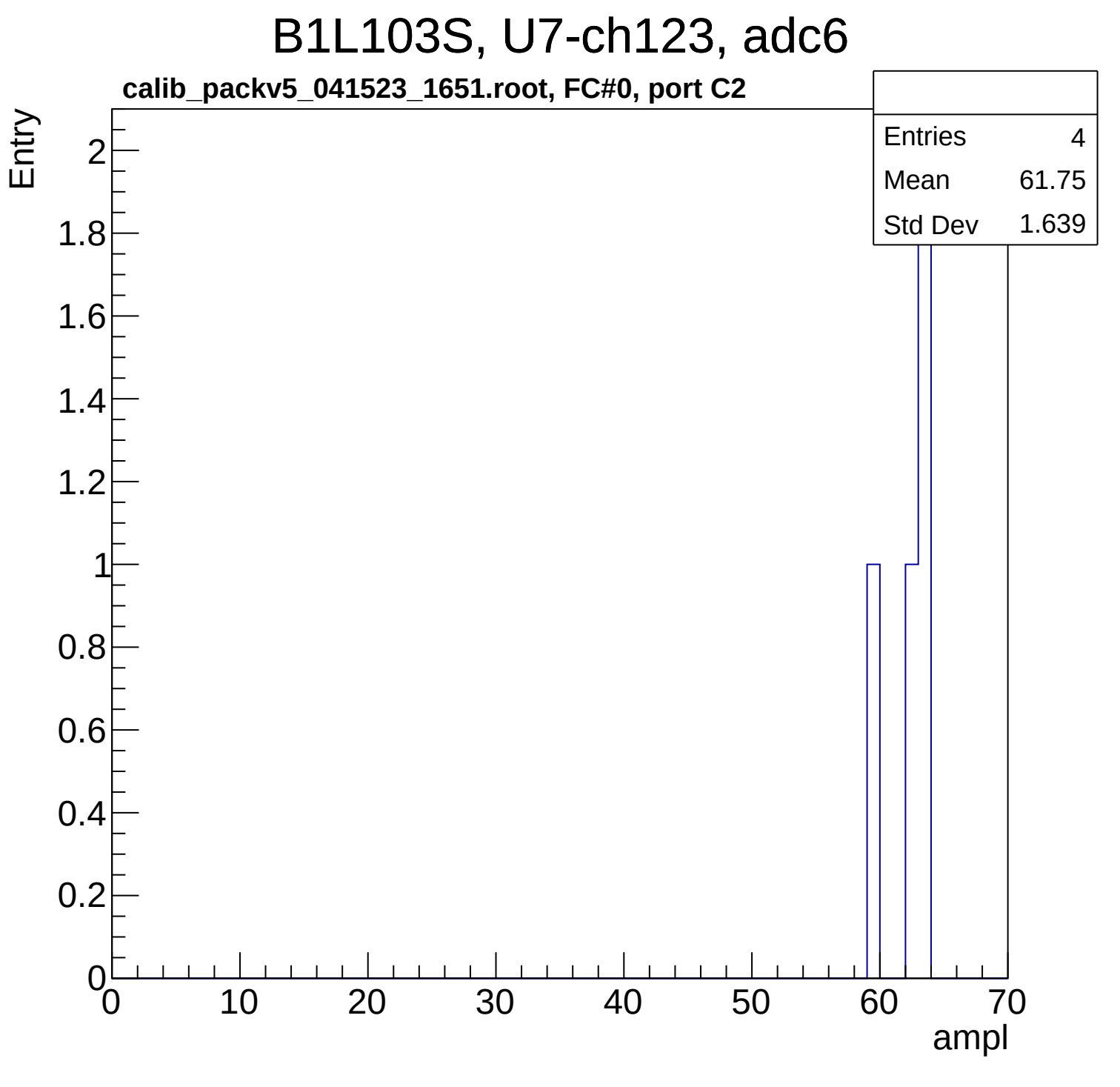
B1L103S, U7-ch123, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 4
Mean 61.75
Std Dev 1.639
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
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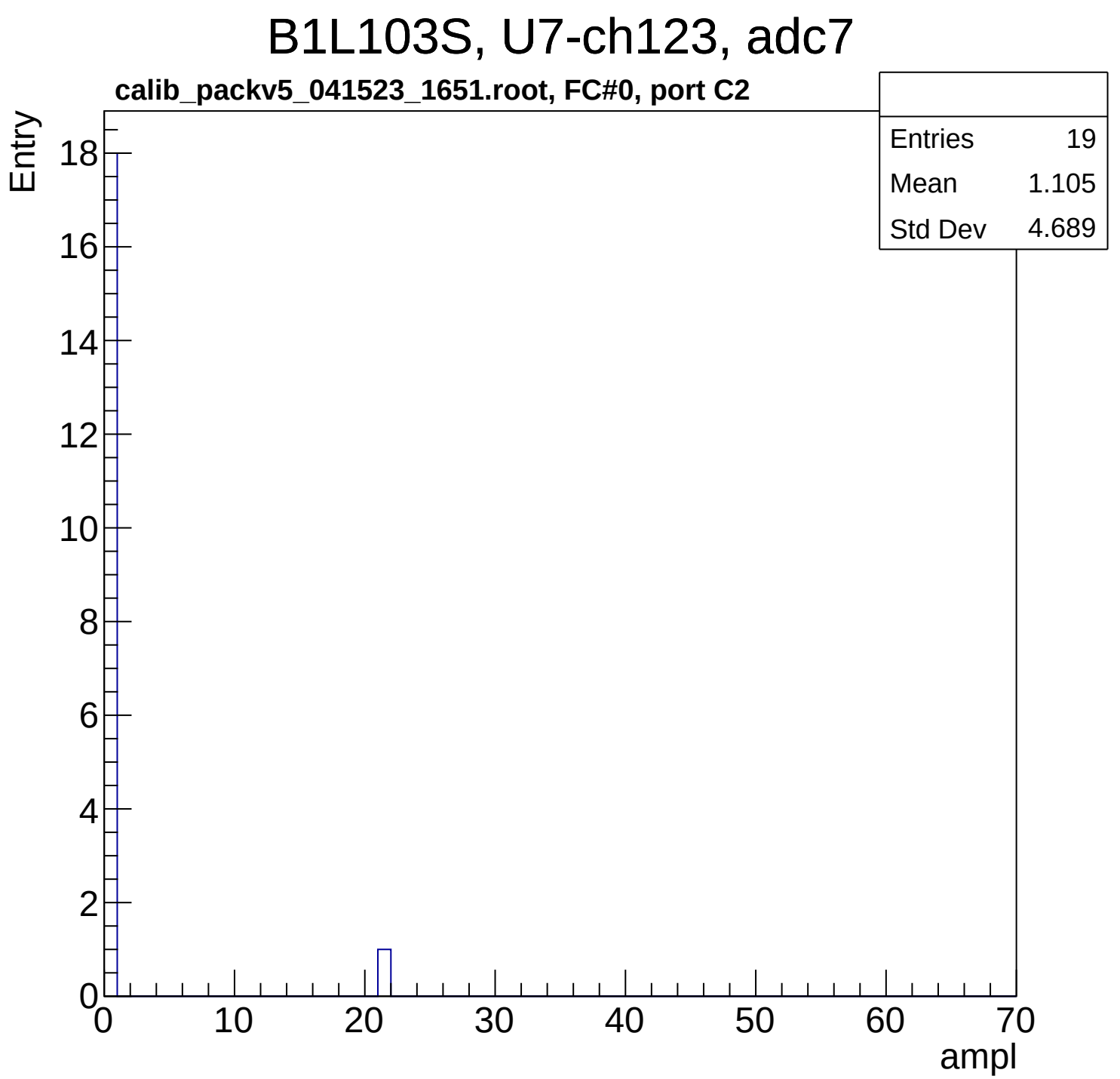
B1L103S, U7-ch123, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.105
Std Dev 4.689
Entry
0
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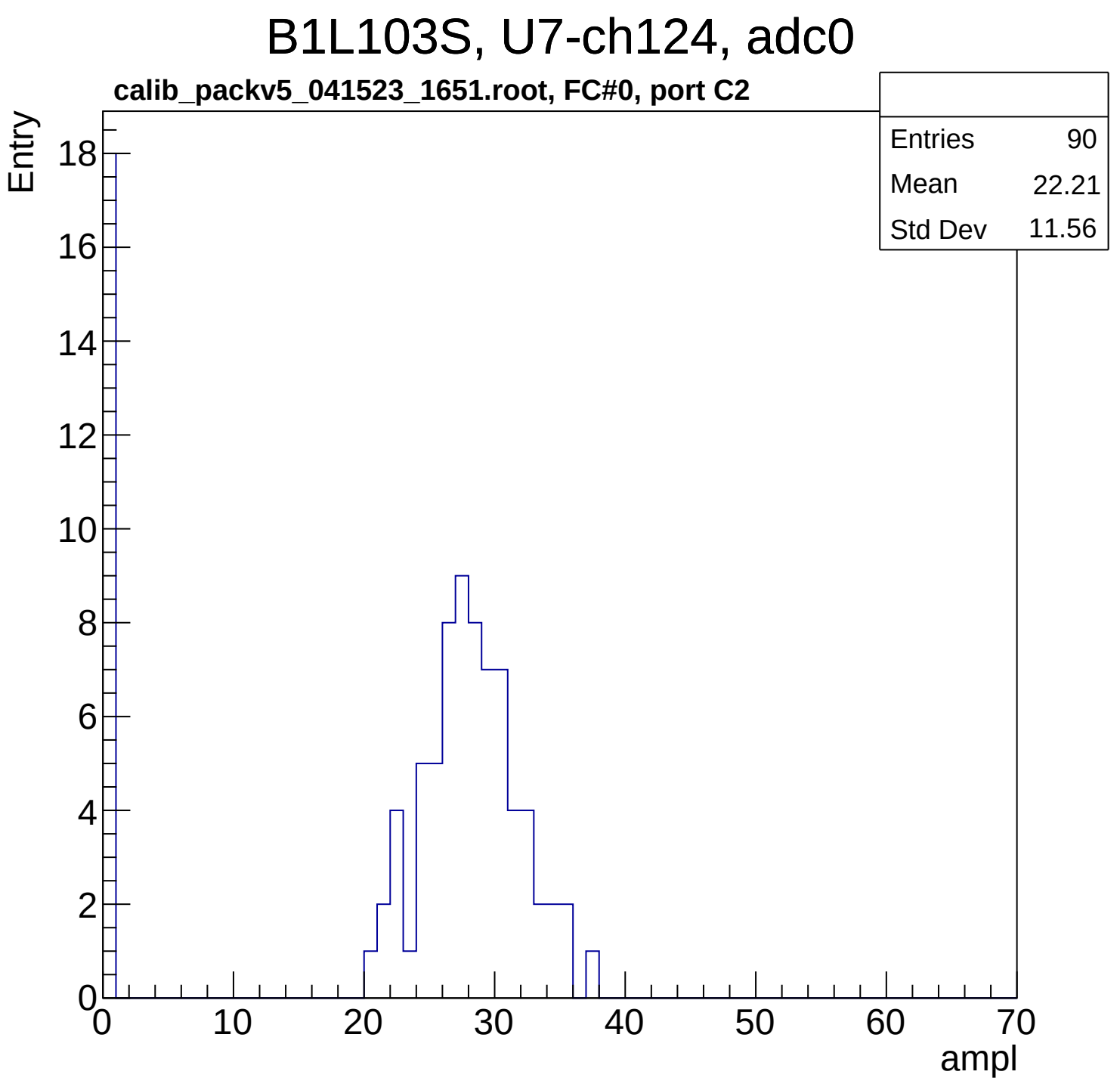
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch124, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 90
Mean 22.21
Std Dev 11.56
Entry
ampl
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4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
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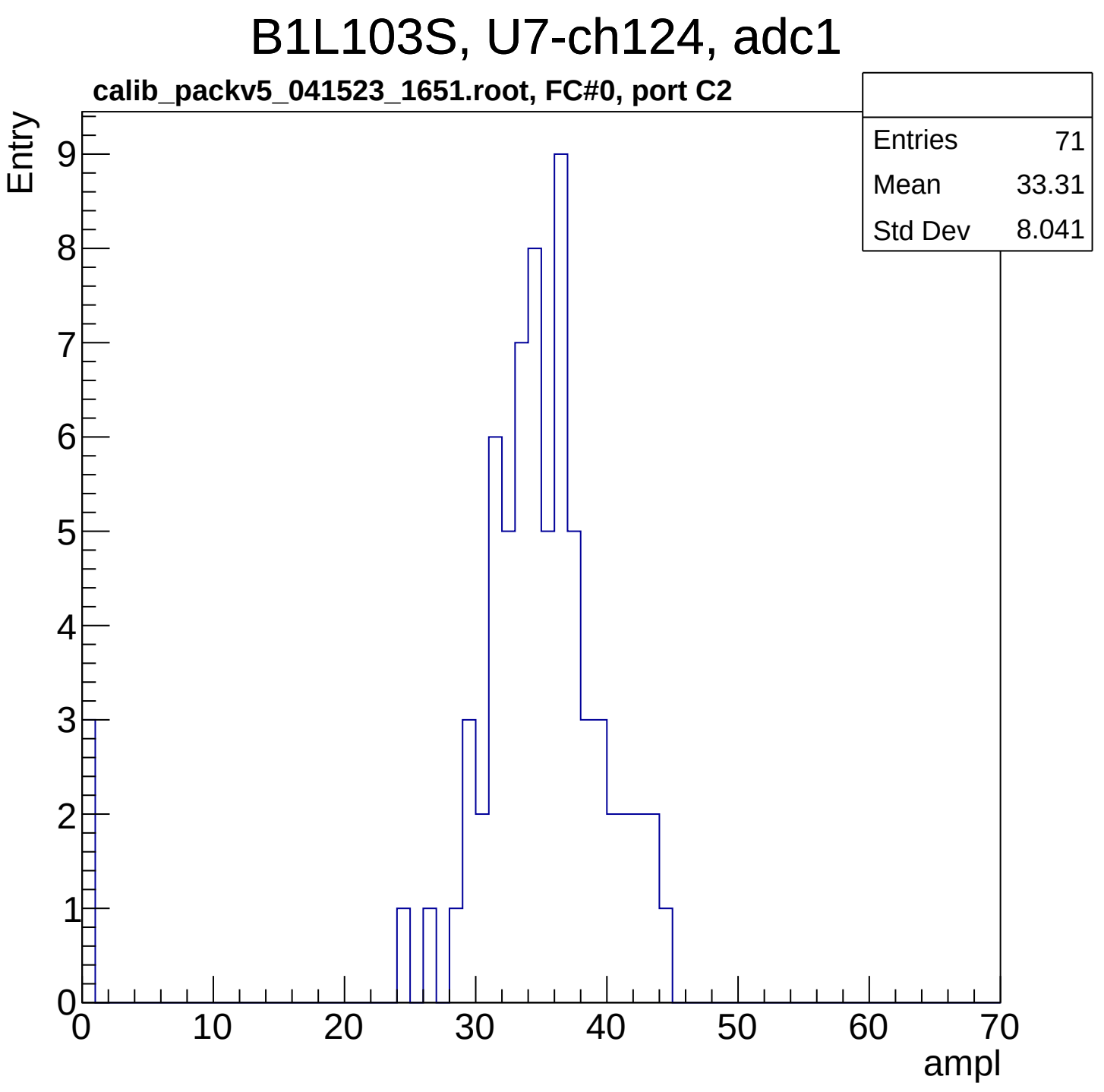
B1L103S, U7-ch124, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 33.31
Std Dev 8.041
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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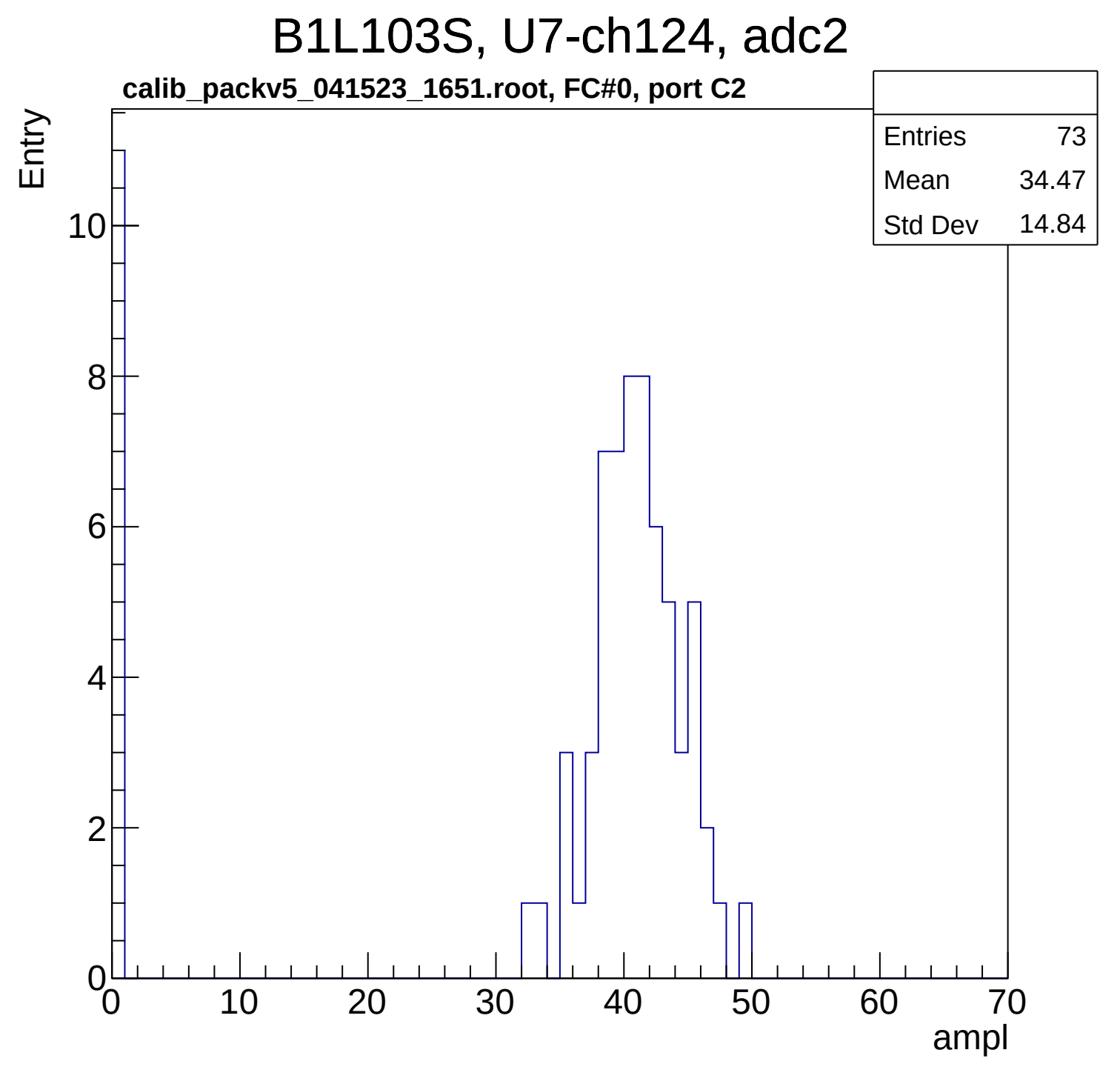
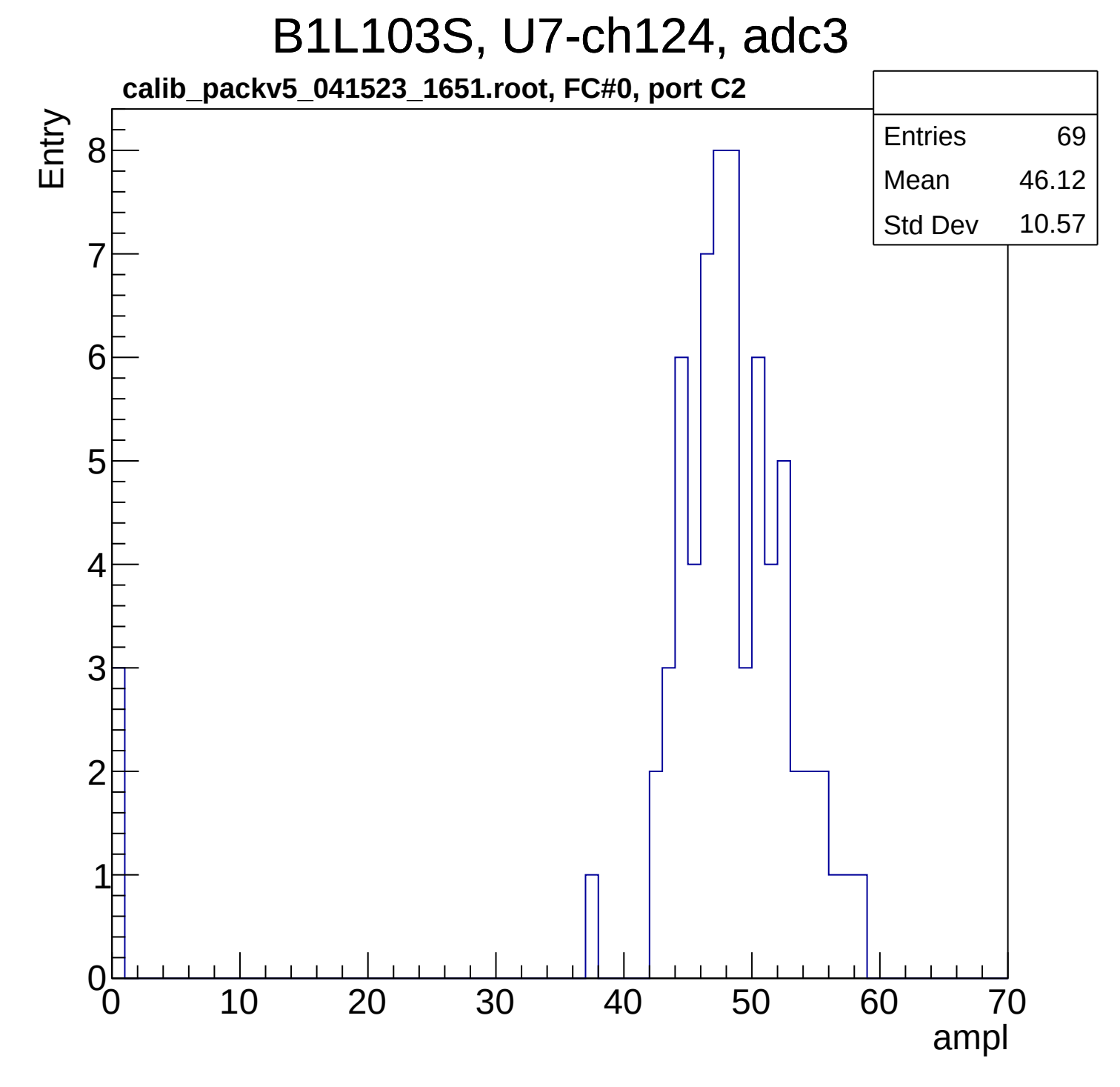
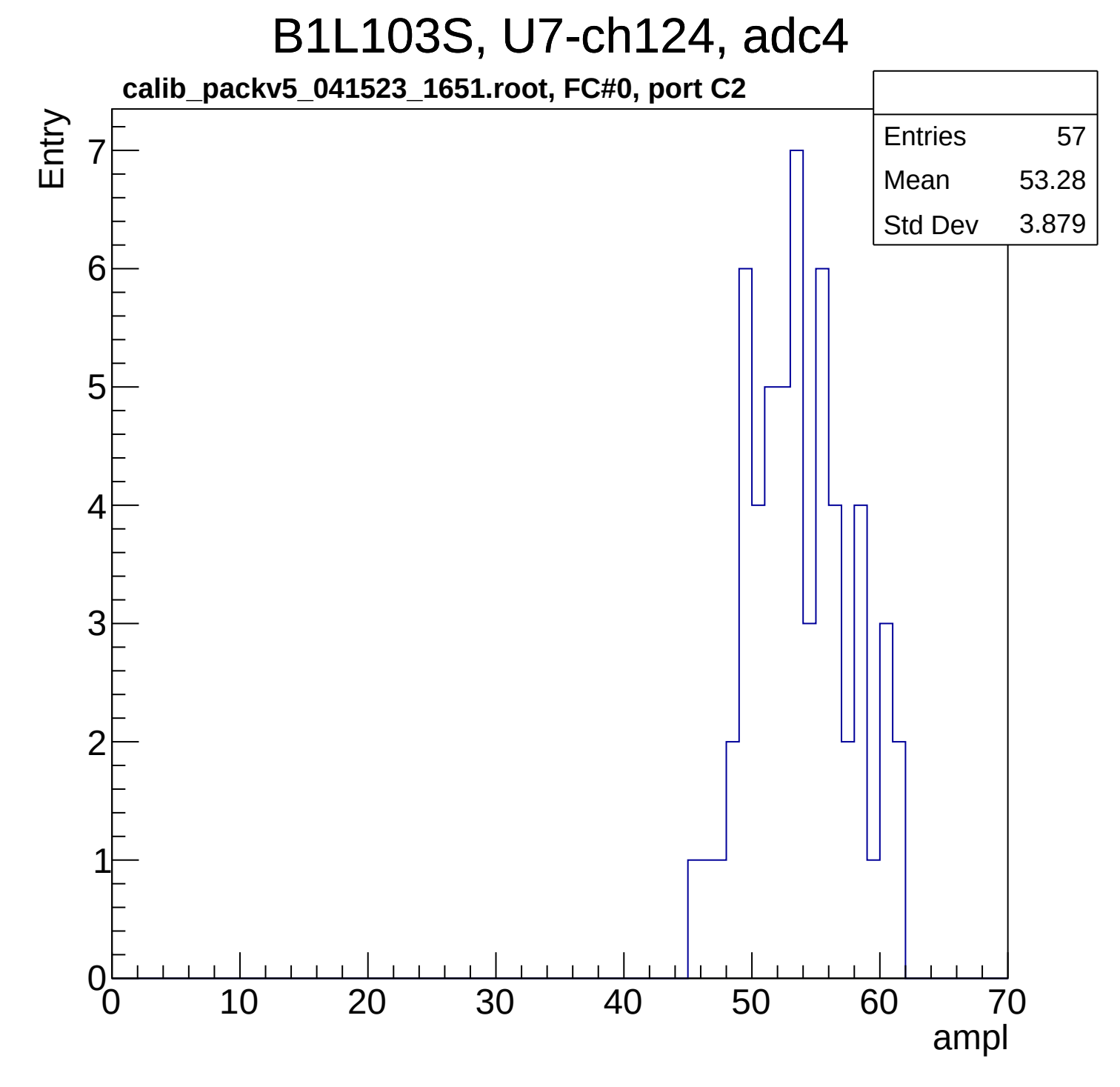

B1L103S, U7-ch124, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 34.47
Std Dev 14.84
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch124, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 46.12
Std Dev 10.57
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch124, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 53.28
Std Dev 3.879
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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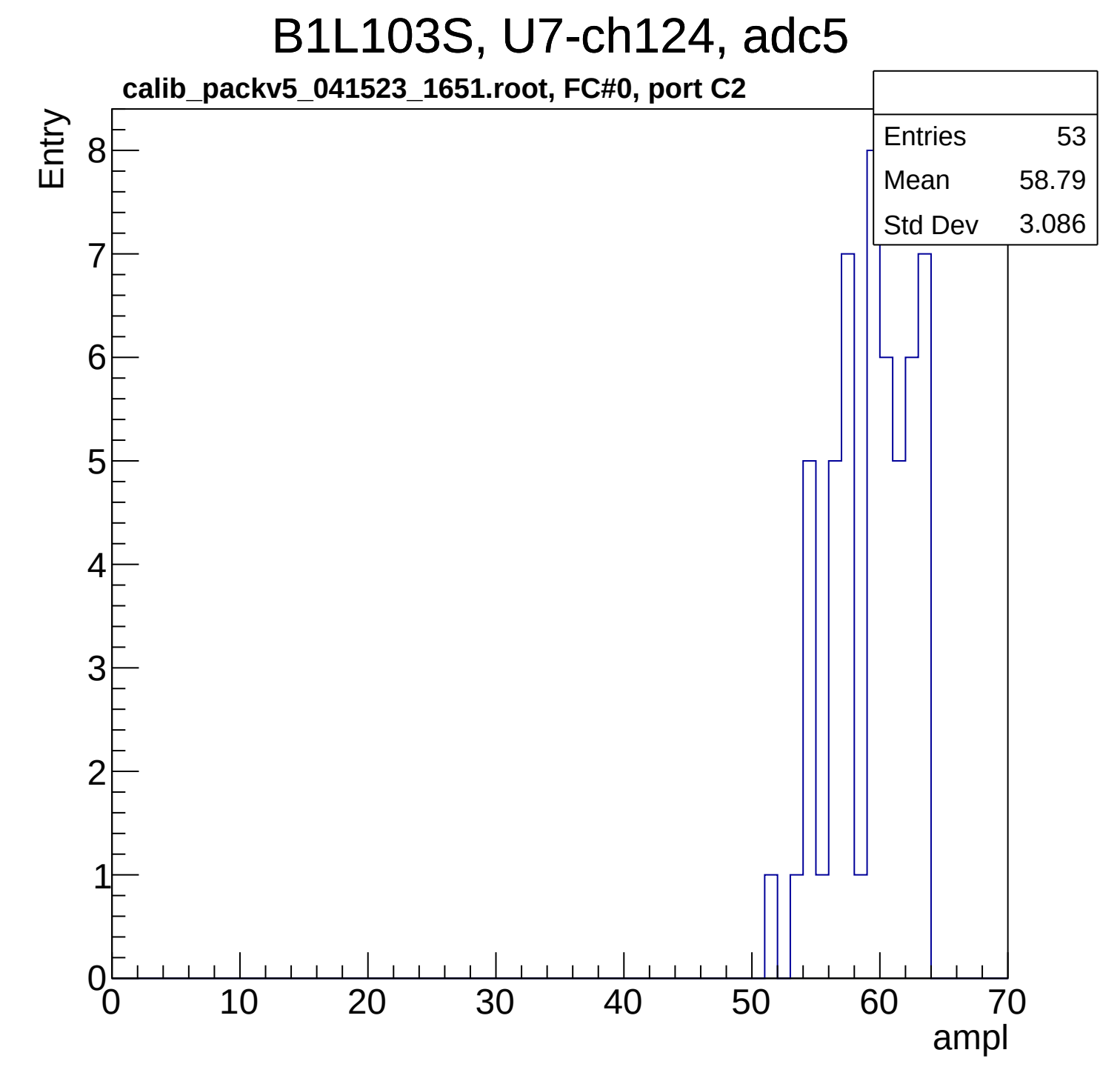
B1L103S, U7-ch124, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 58.79
Std Dev 3.086
Entry
ampl
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1
2
3
4
5
6
7
8
0
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60
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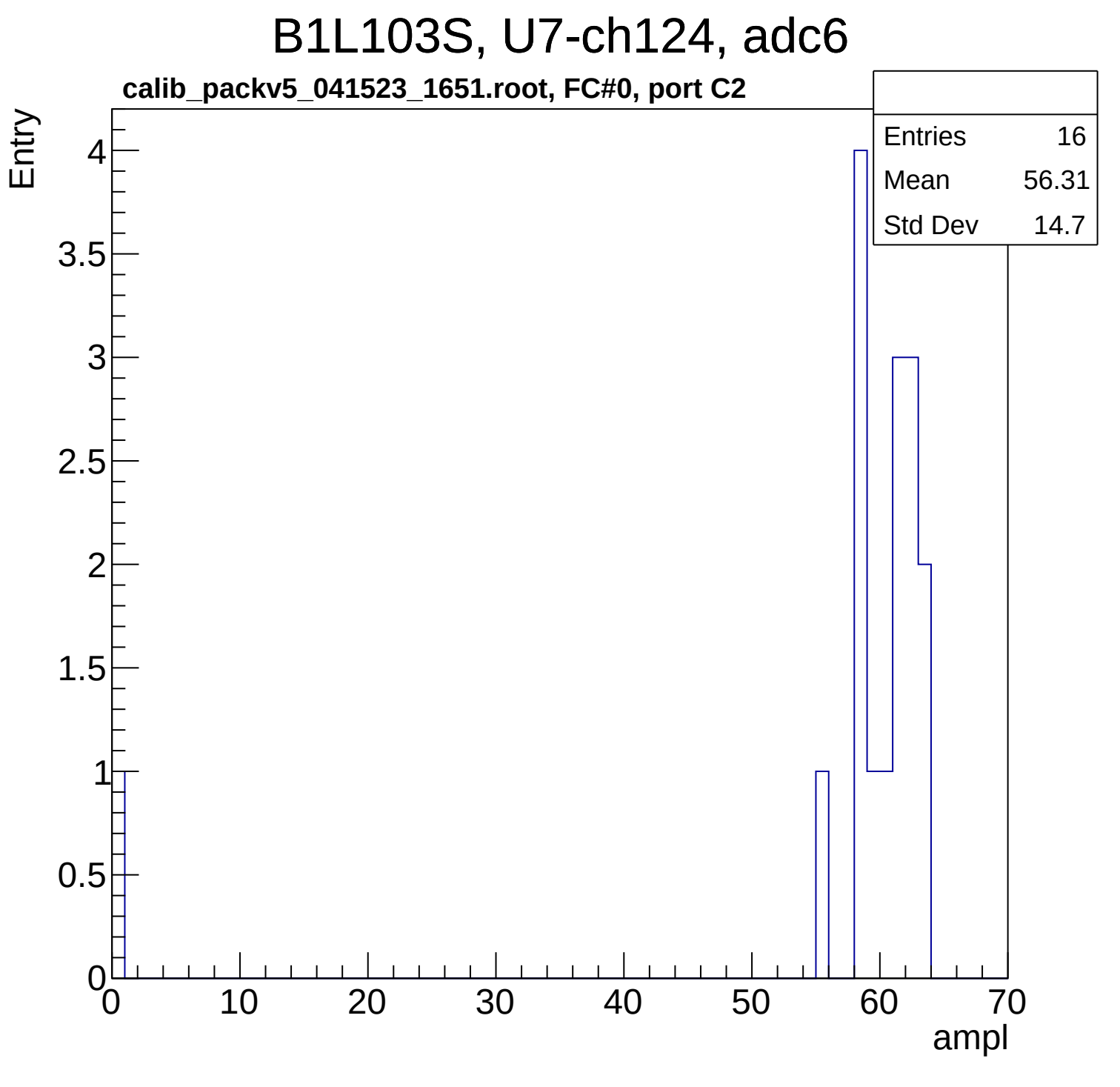
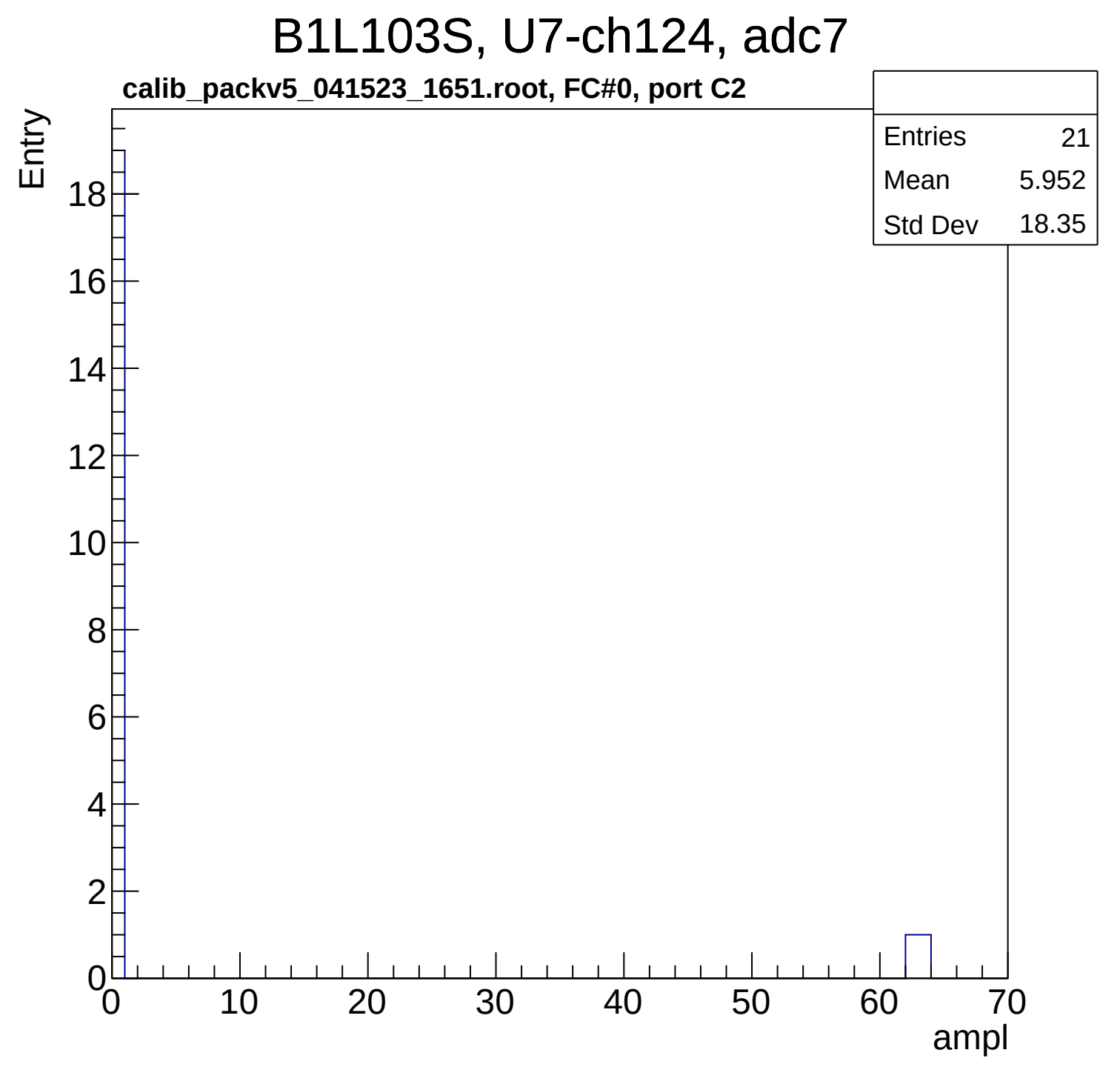

B1L103S, U7-ch124, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 16
Mean 56.31
Std Dev 14.7
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U7-ch124, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 5.952
Std Dev 18.35
Entry
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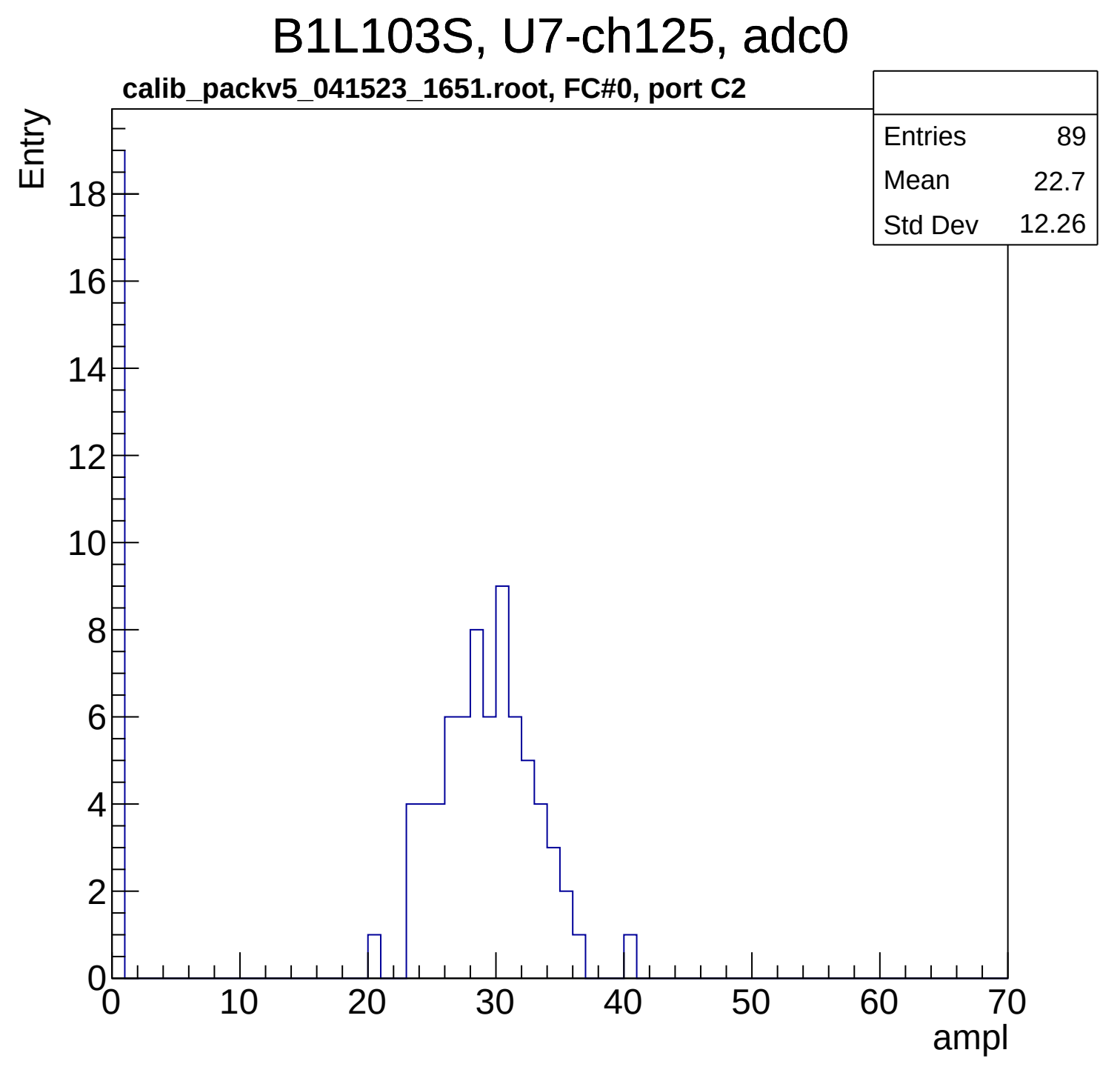
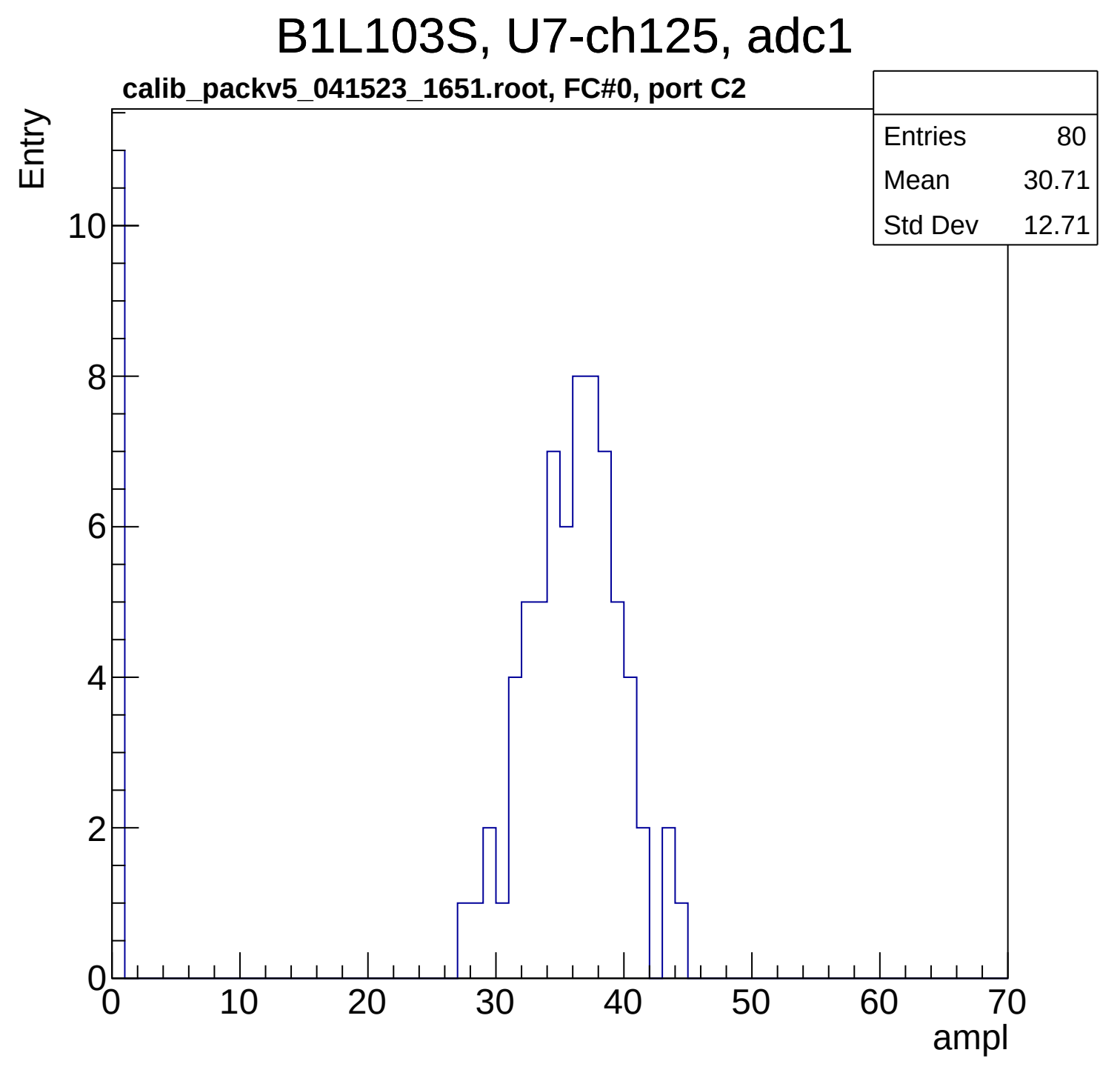
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch125, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 89
Mean 22.7
Std Dev 12.26
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch125, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 30.71
Std Dev 12.71
Entry
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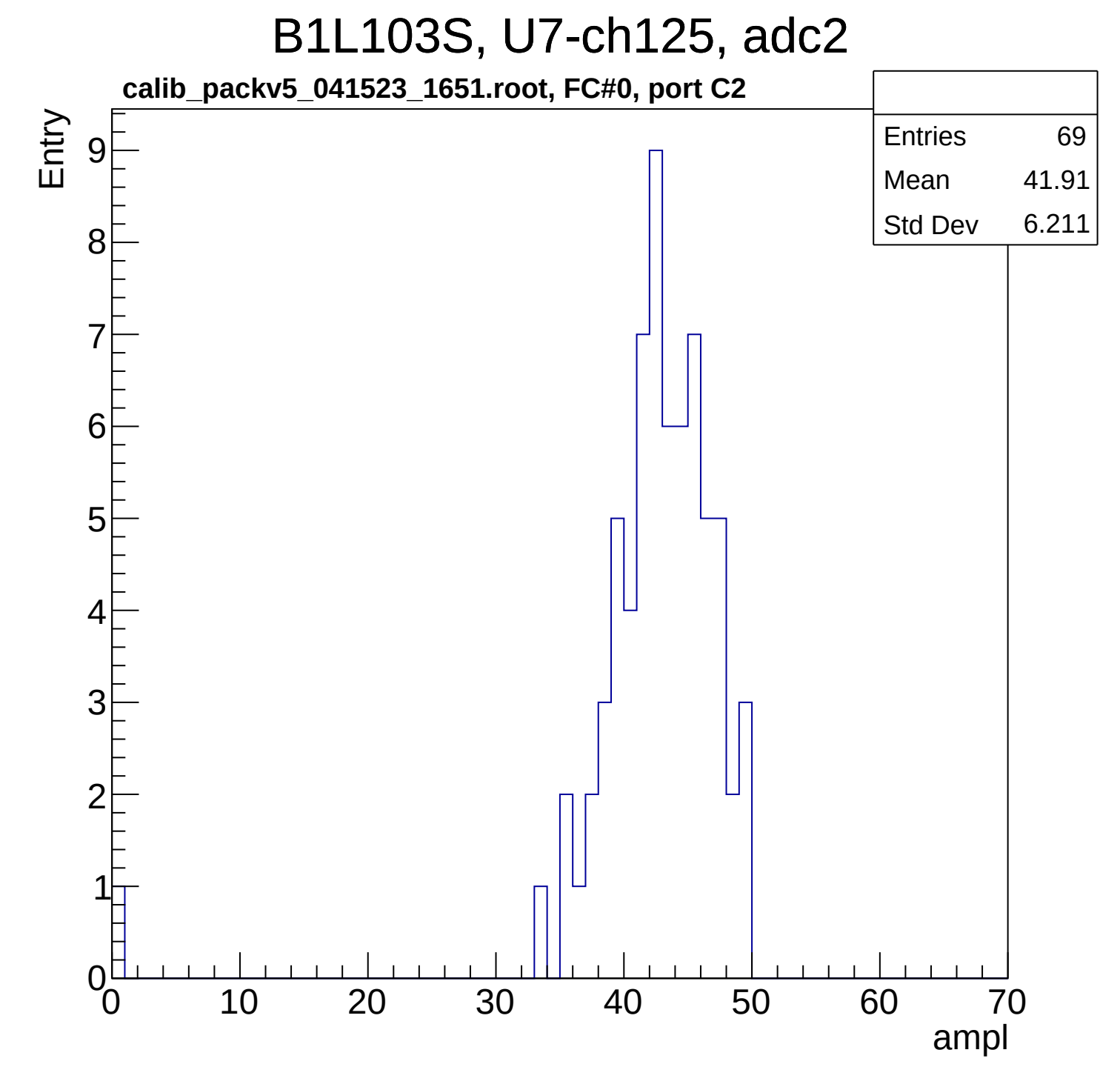
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch125, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 41.91
Std Dev 6.211
Entry
ampl
0
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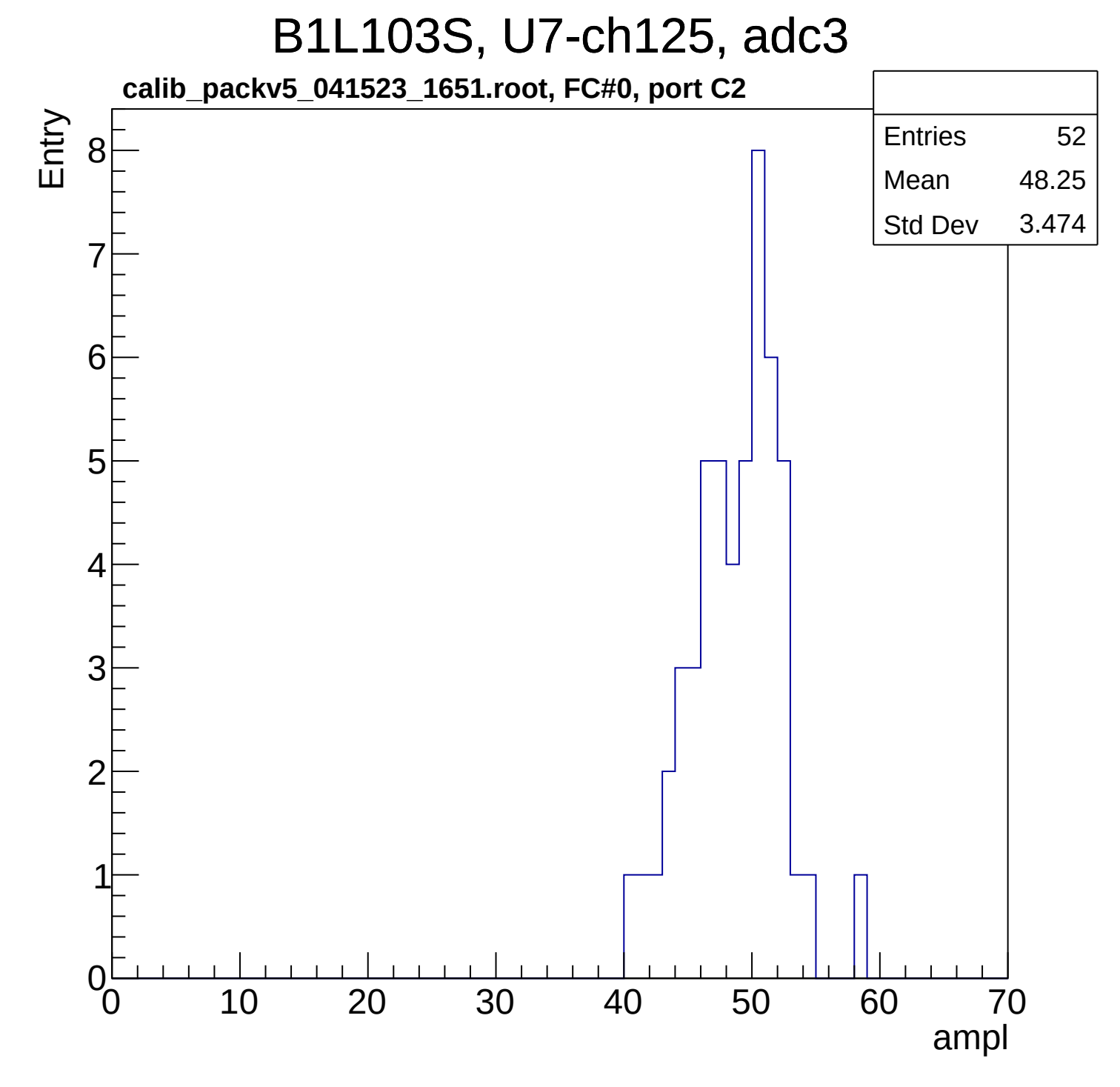
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U7-ch125, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 48.25
Std Dev 3.474
Entry
ampl
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2
3
4
5
6
7
8
0
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20
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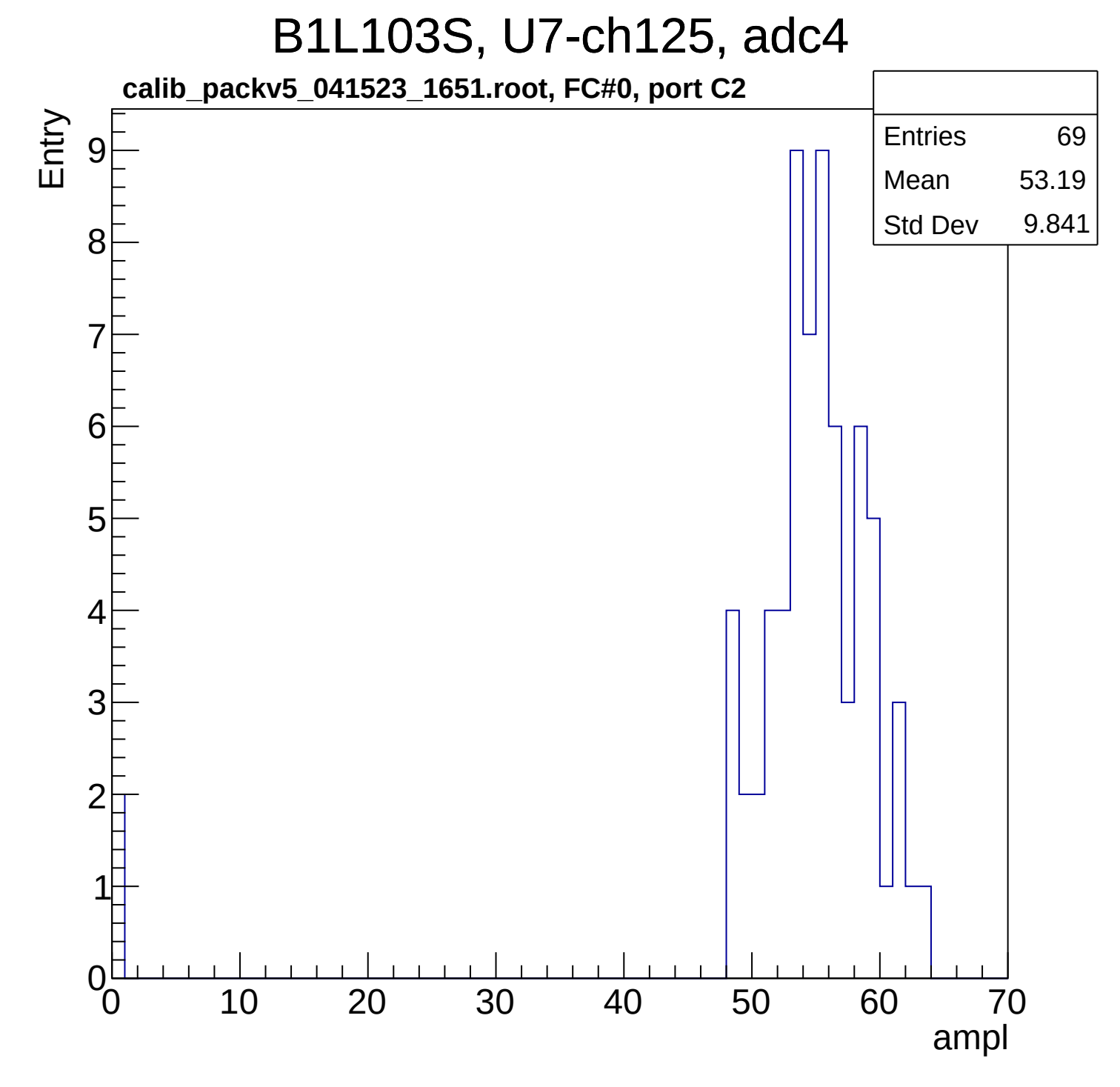
40
50
60
70


B1L103S, U7-ch125, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 53.19
Std Dev 9.841
Entry
ampl
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3
4
5
6
7
8
9
0
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20
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40
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60
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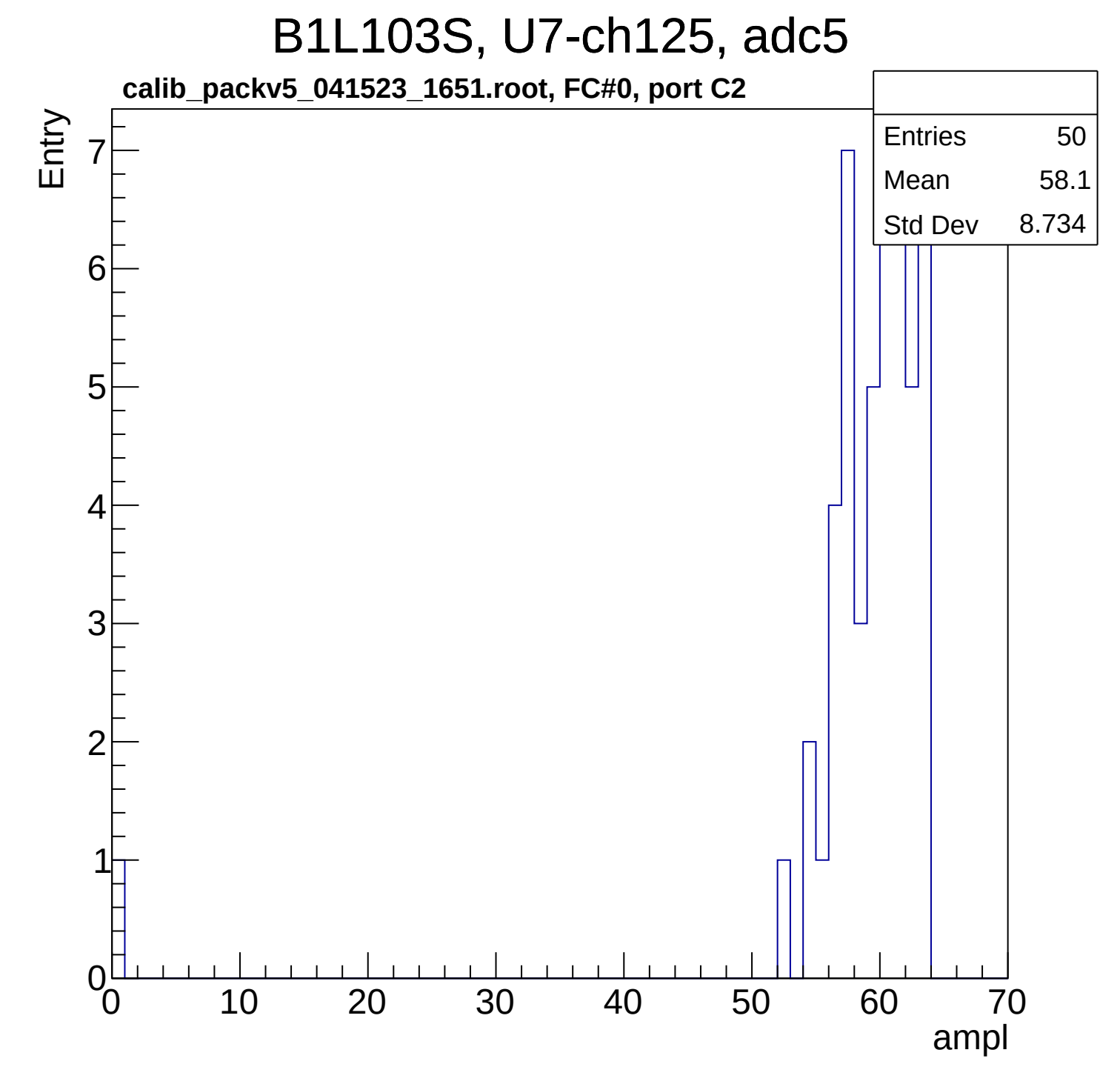
B1L103S, U7-ch125, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 58.1
Std Dev 8.734
Entry
ampl
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1
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3
4
5
6
7
0
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60
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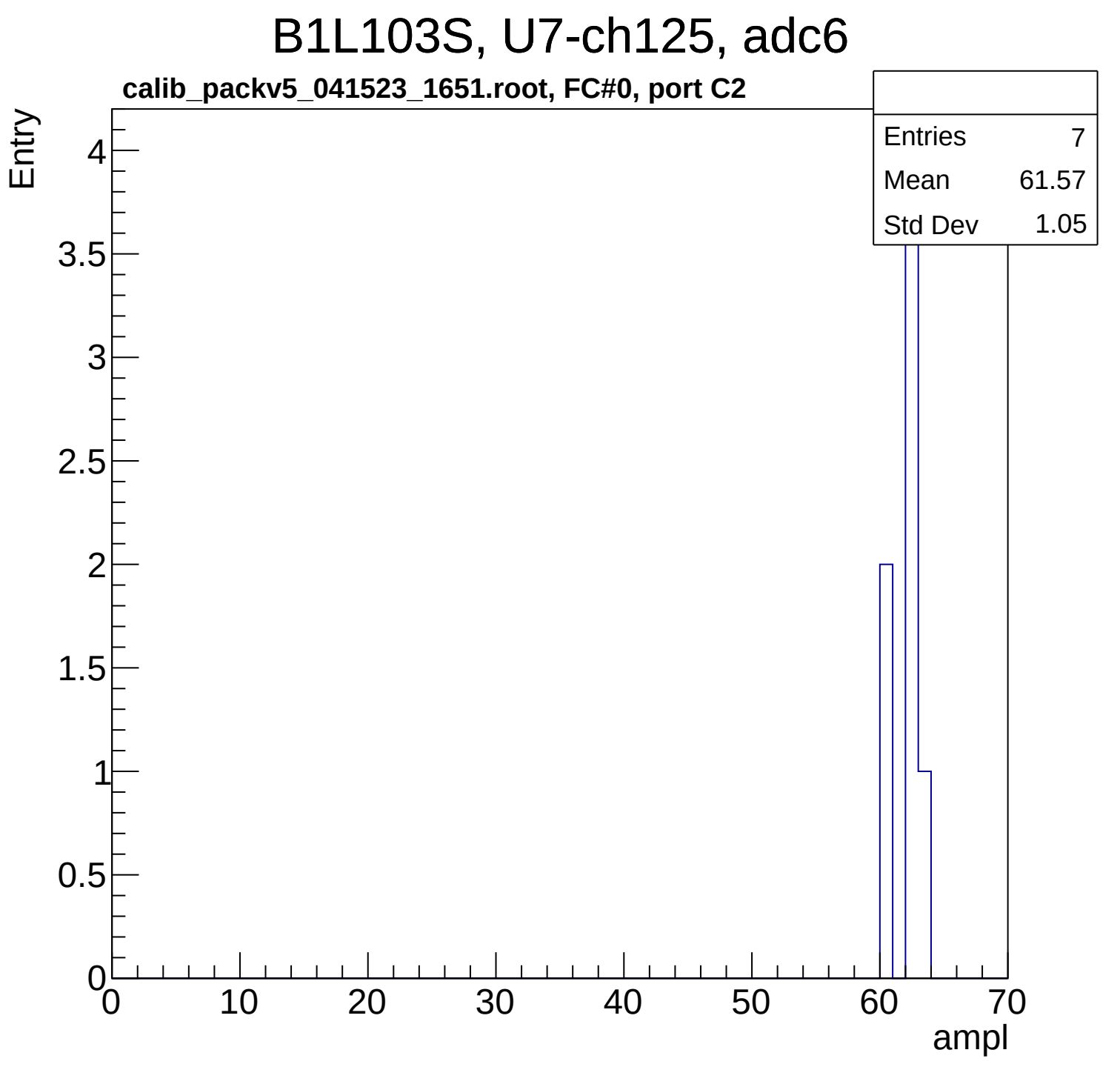
B1L103S, U7-ch125, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 61.57
Std Dev 1.05
Entry
ampl
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0.5
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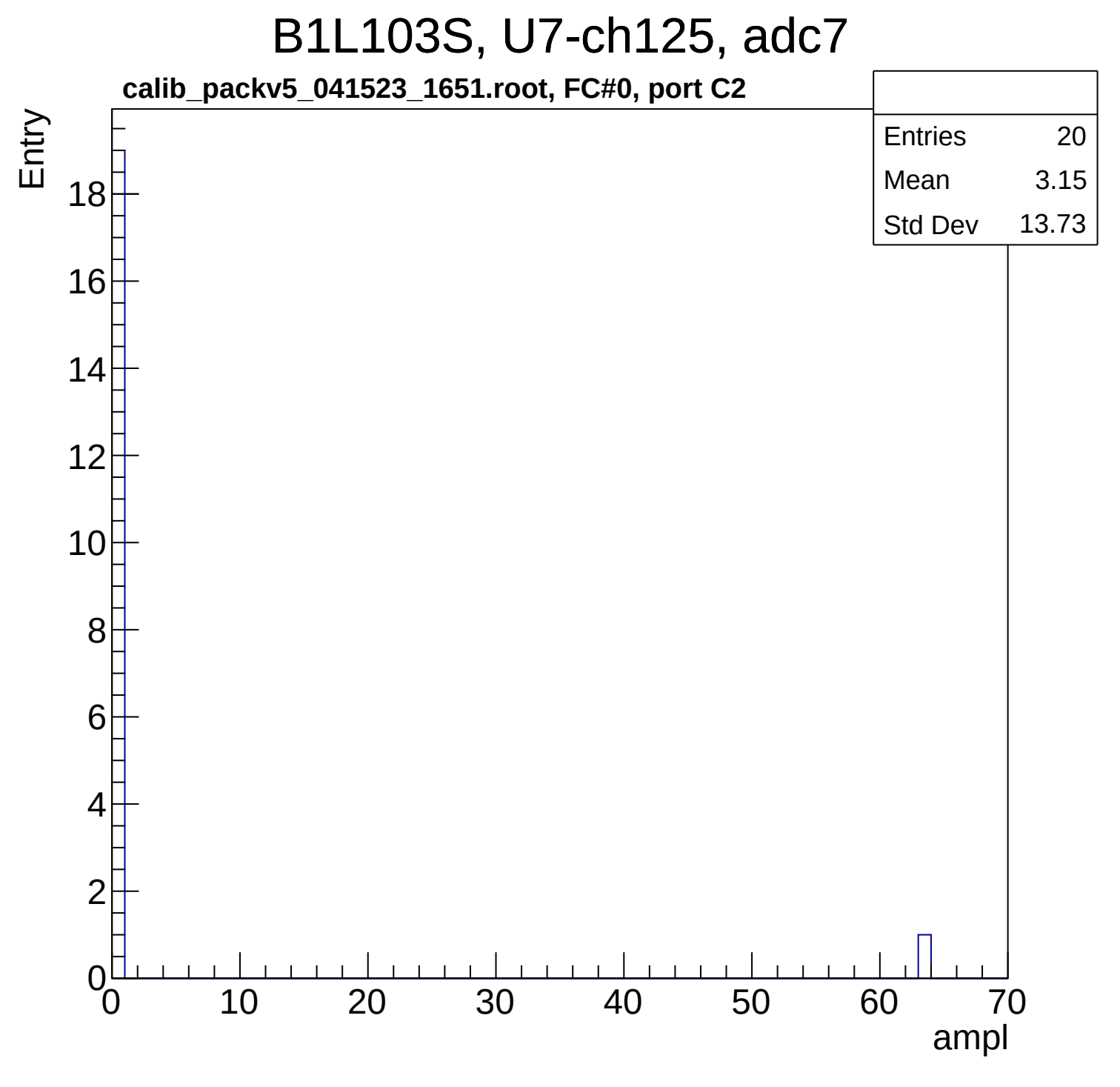
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U7-ch125, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
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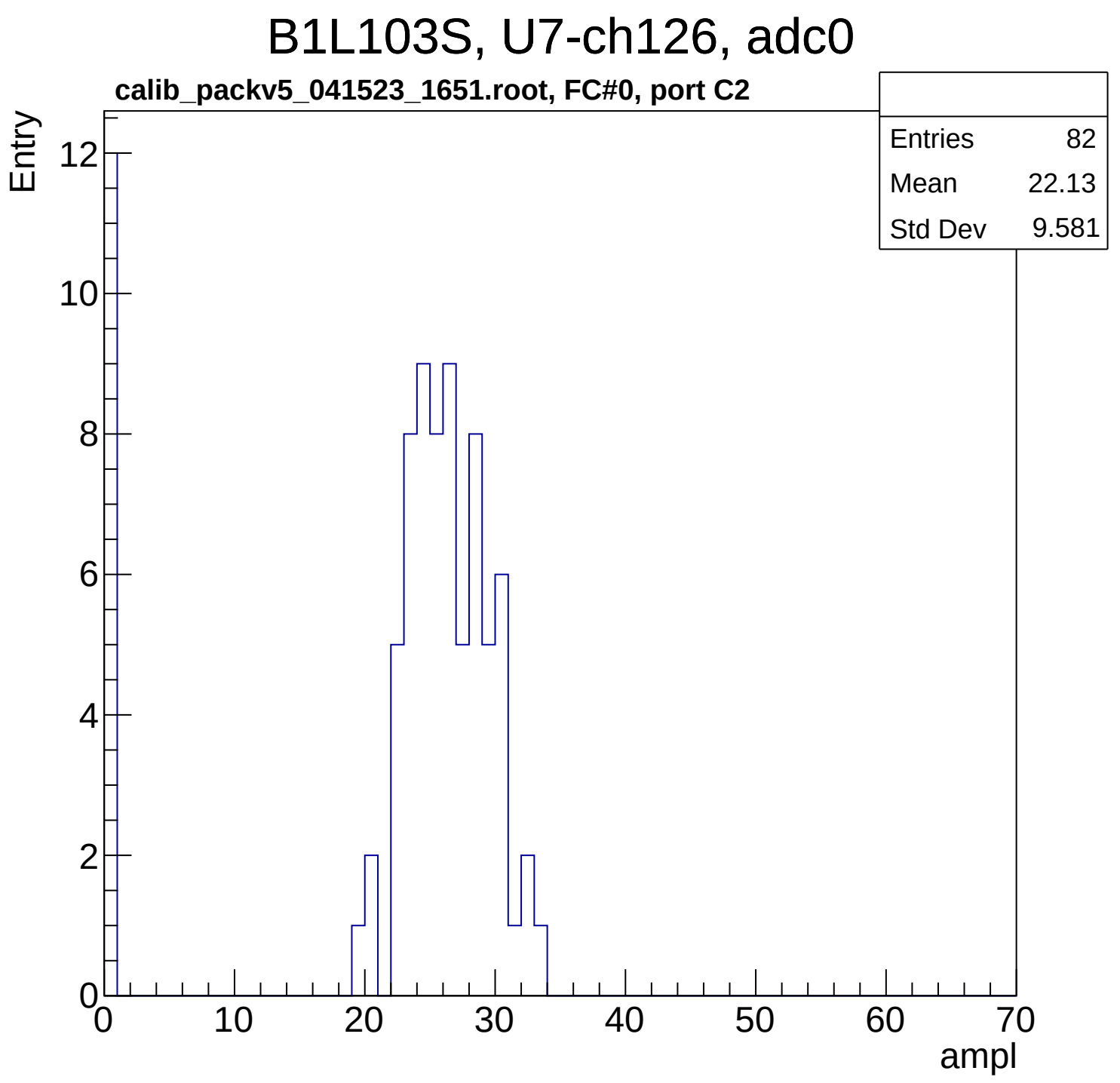
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch126, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 22.13
Std Dev 9.581
Entry
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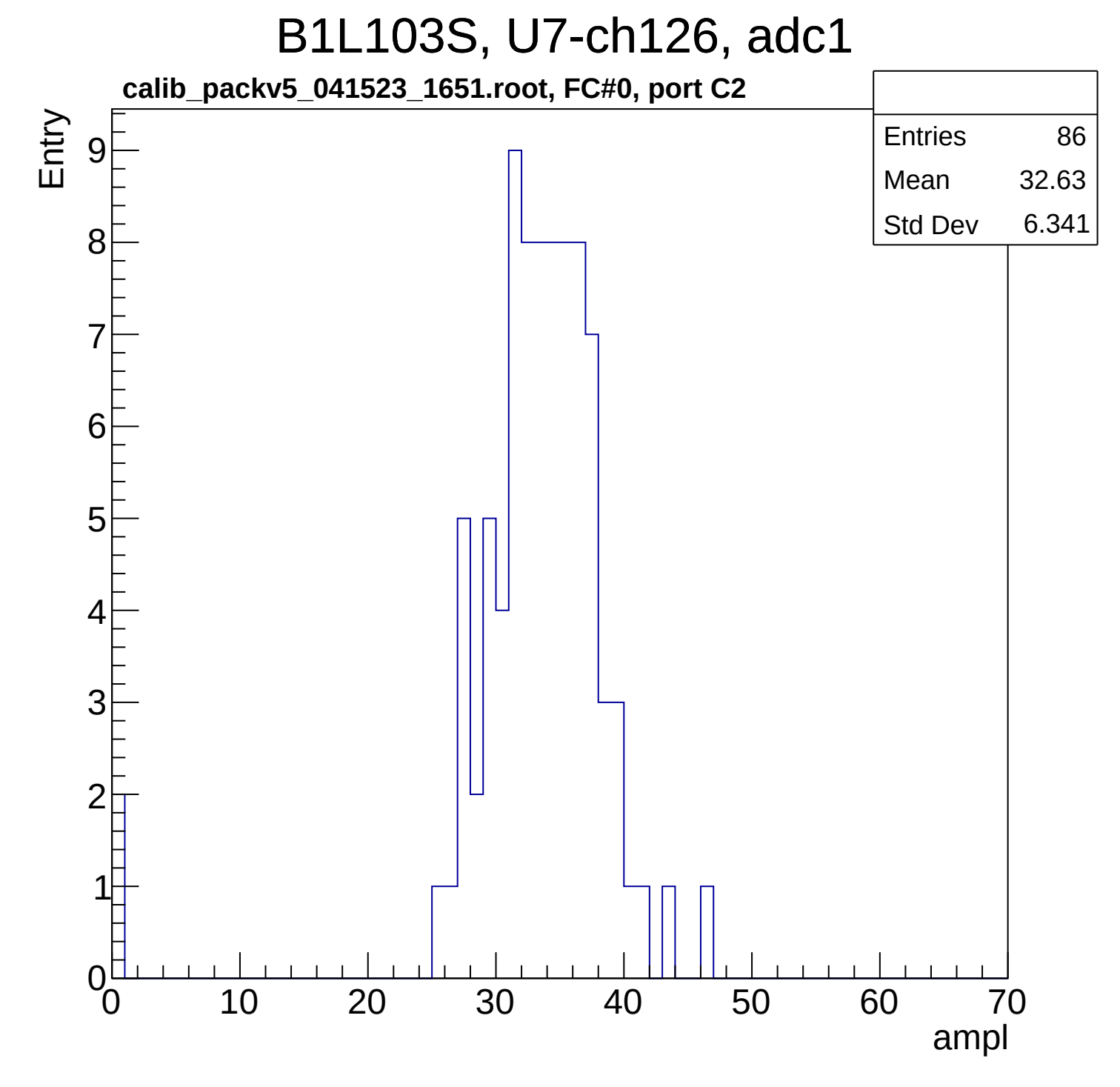
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch126, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 32.63
Std Dev 6.341
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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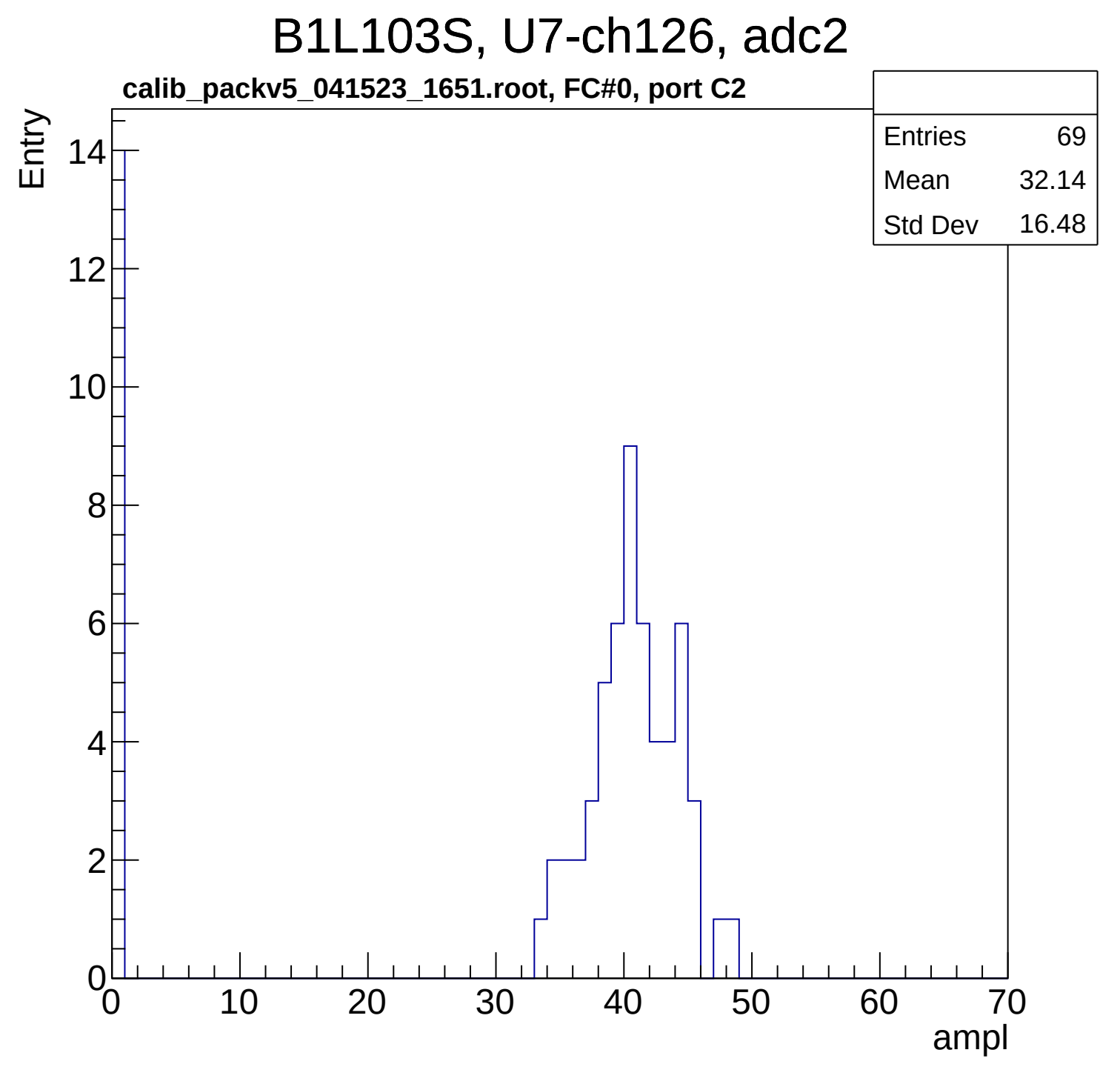
40
50
60
70


B1L103S, U7-ch126, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 32.14
Std Dev 16.48
Entry
ampl
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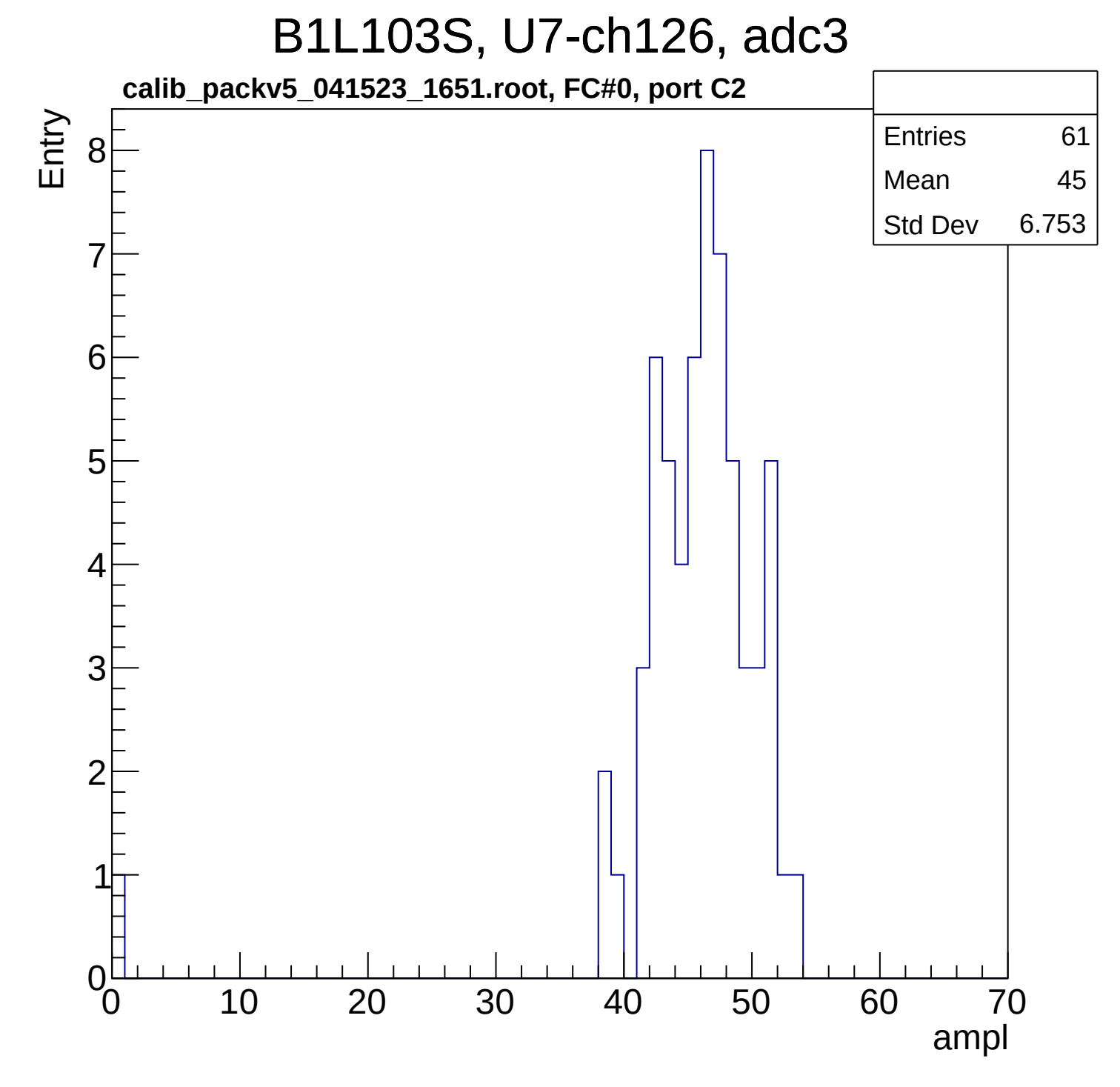
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L103S, U7-ch126, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 45
Std Dev 6.753
Entry
ampl
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2
3
4
5
6
7
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0
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20
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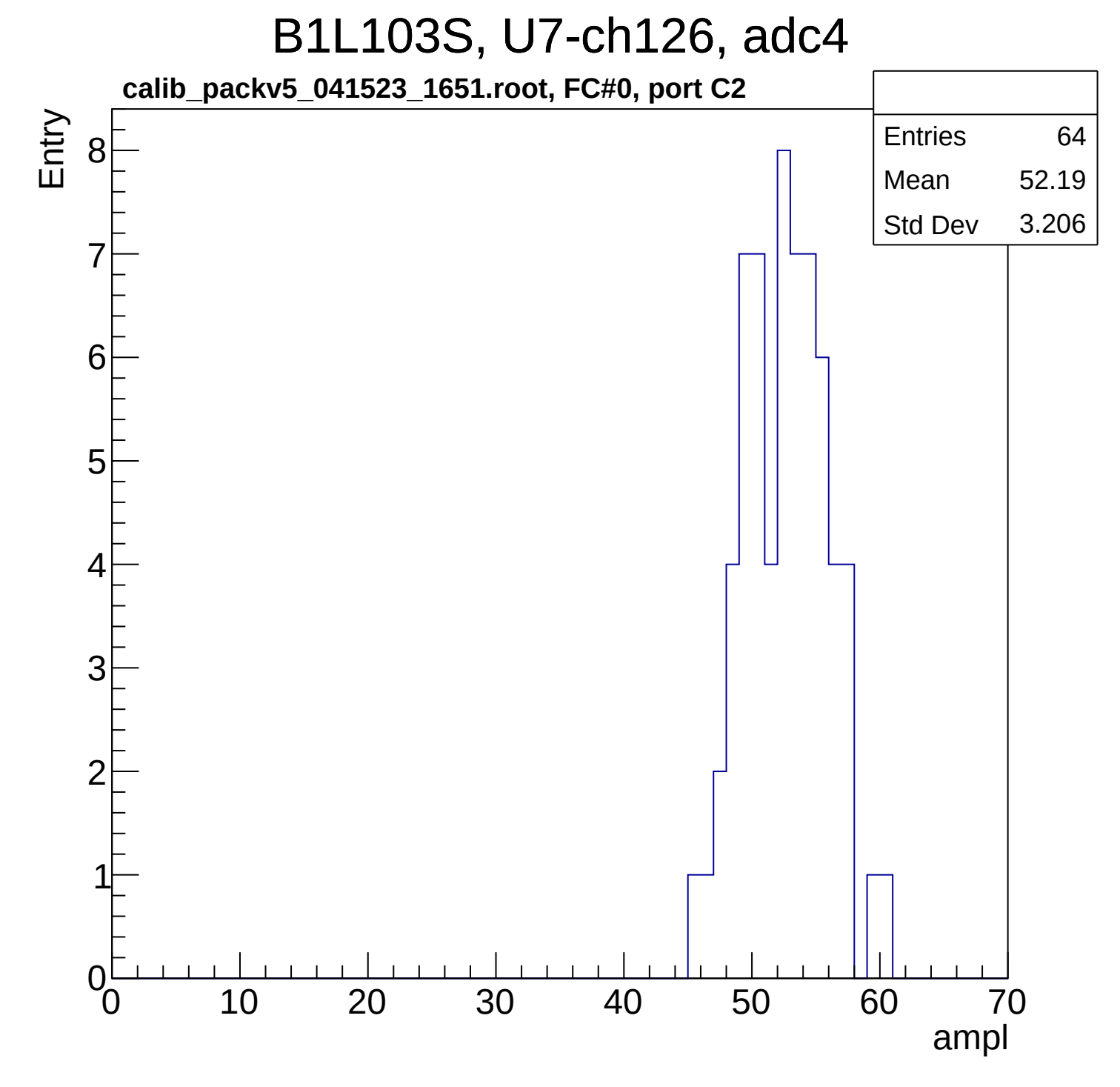
60
70


B1L103S, U7-ch126, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 52.19
Std Dev 3.206
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
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40
50
60
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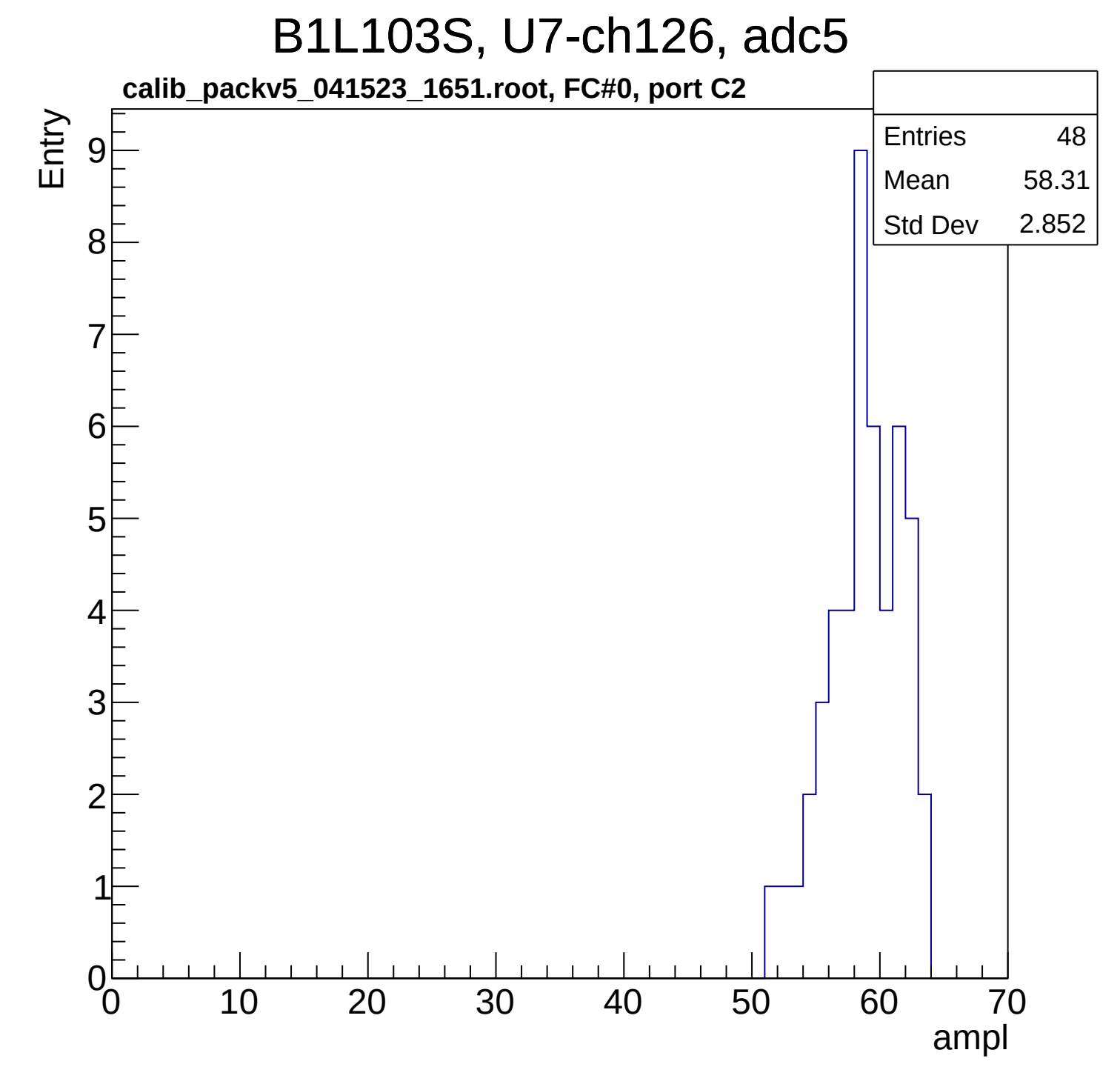
B1L103S, U7-ch126, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 58.31
Std Dev 2.852
Entry
ampl
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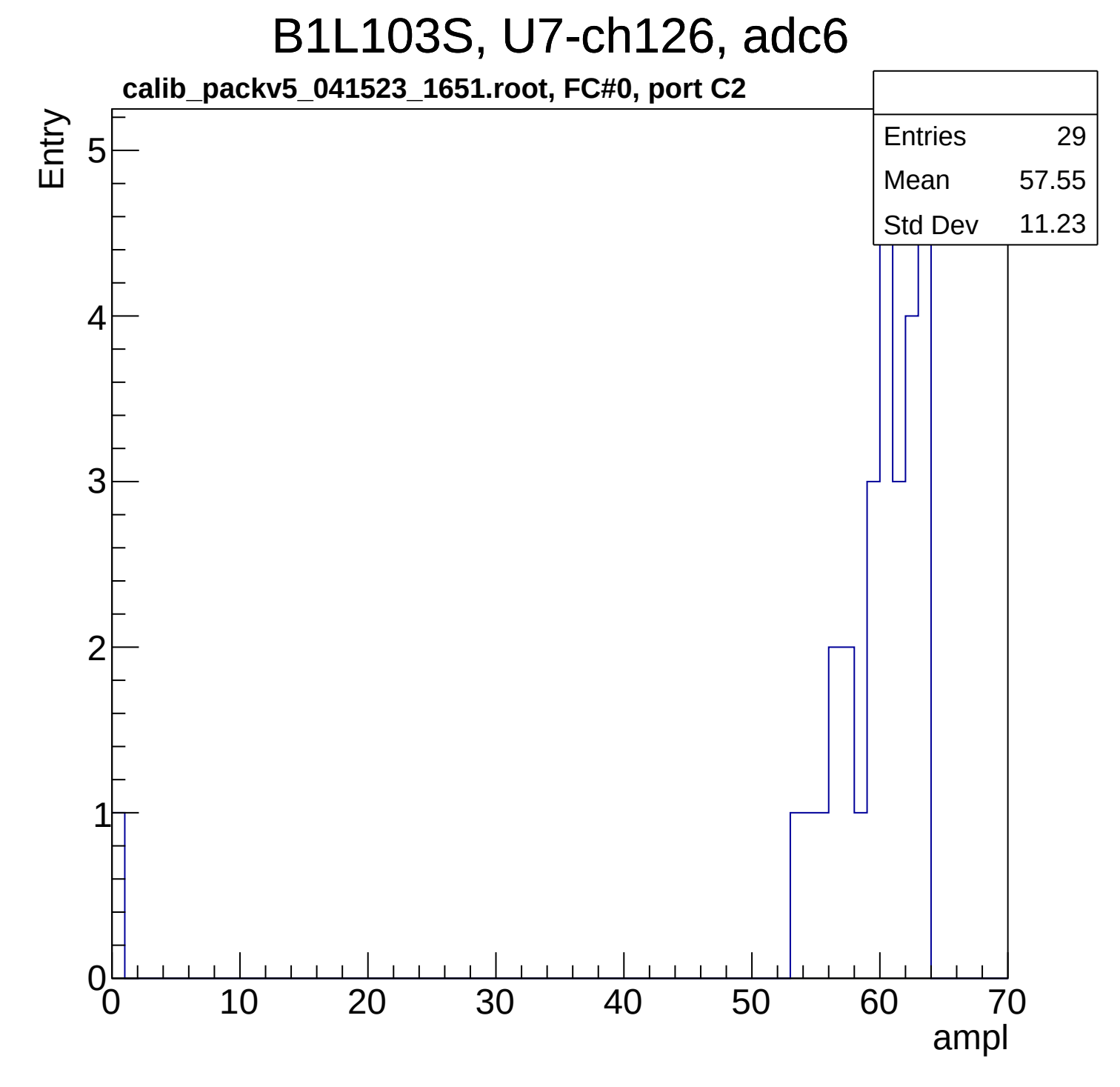
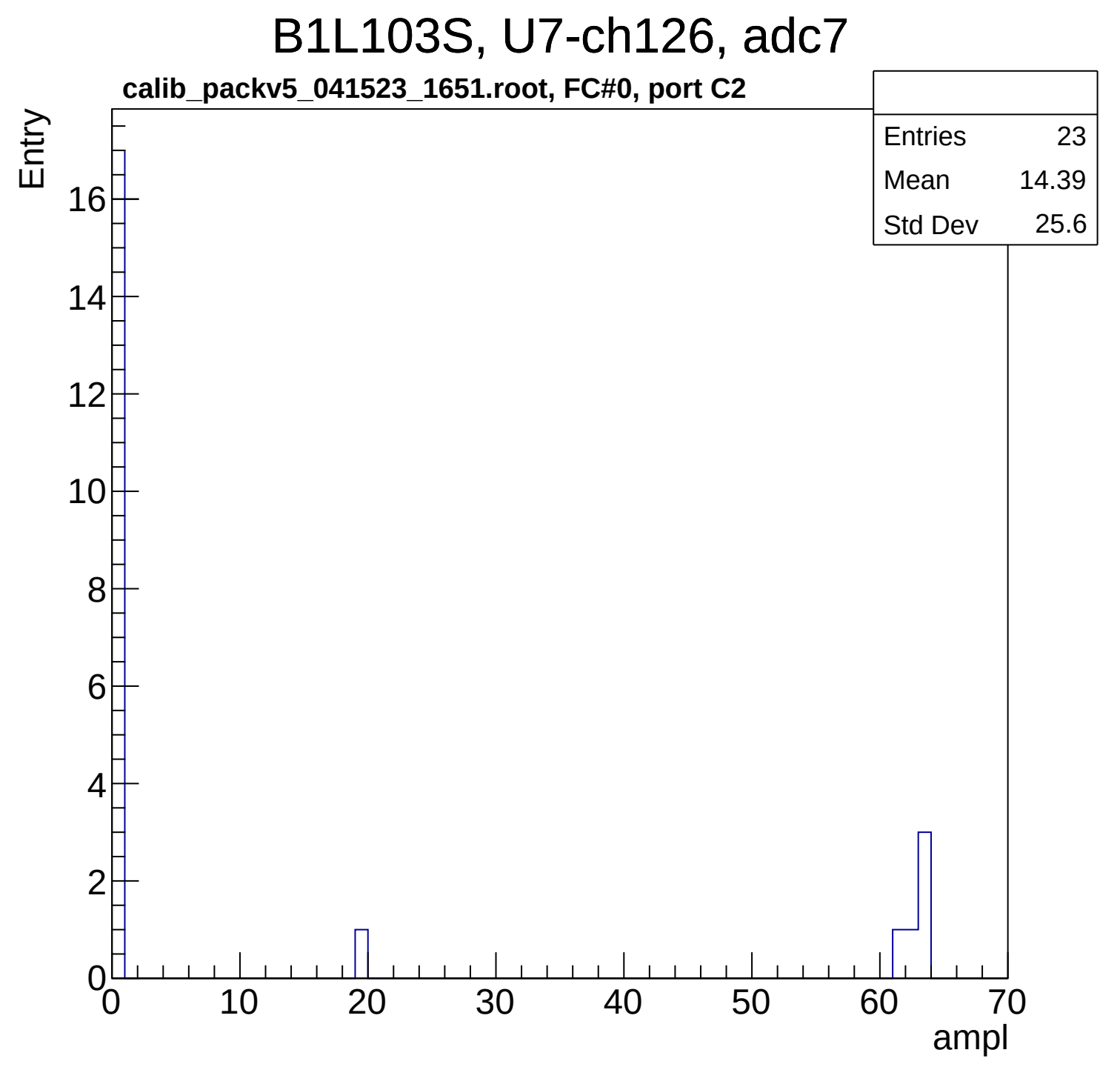
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U7-ch126, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 29
Mean 57.55
Std Dev 11.23
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U7-ch126, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 23
Mean 14.39
Std Dev 25.6
Entry
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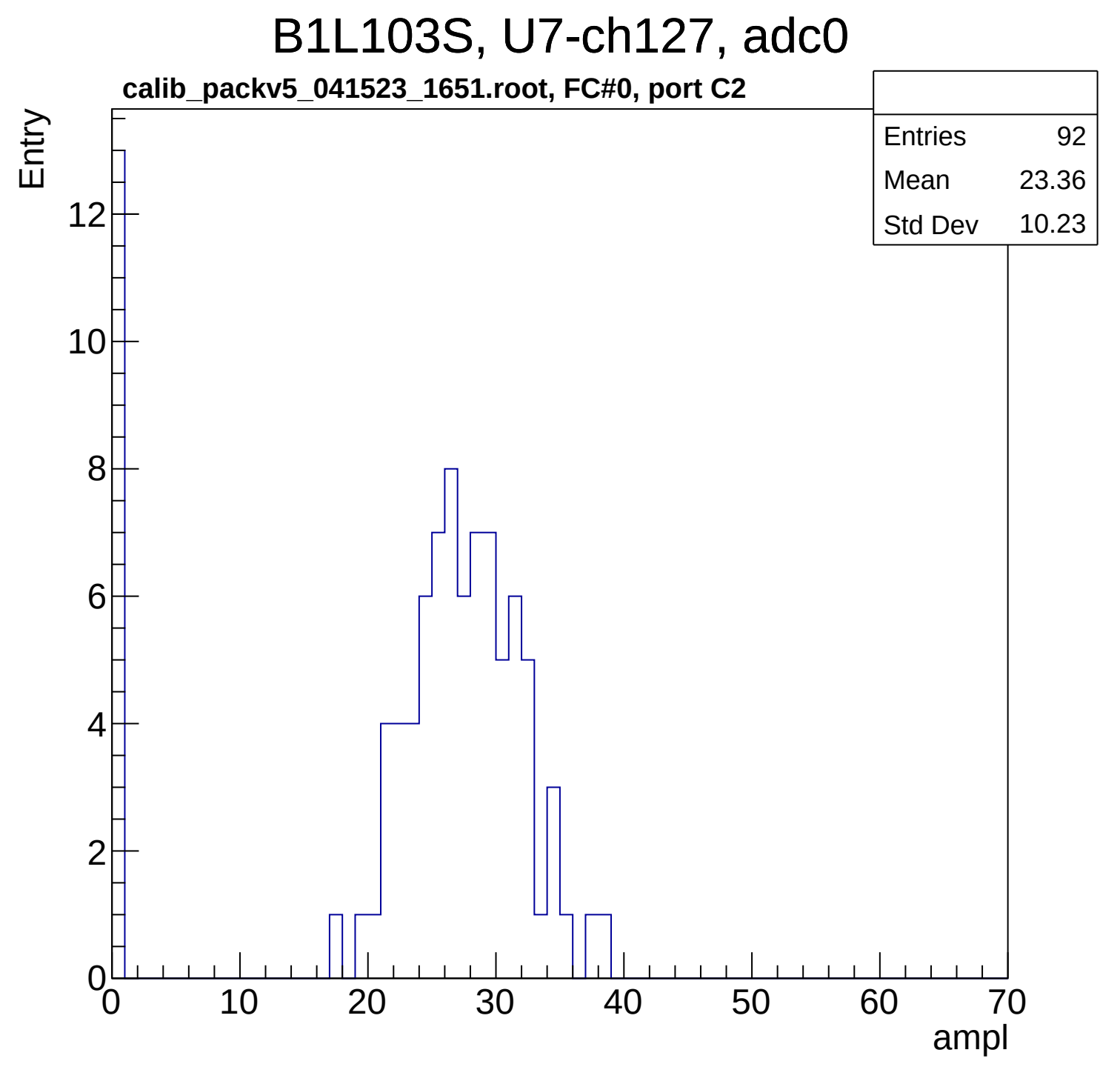
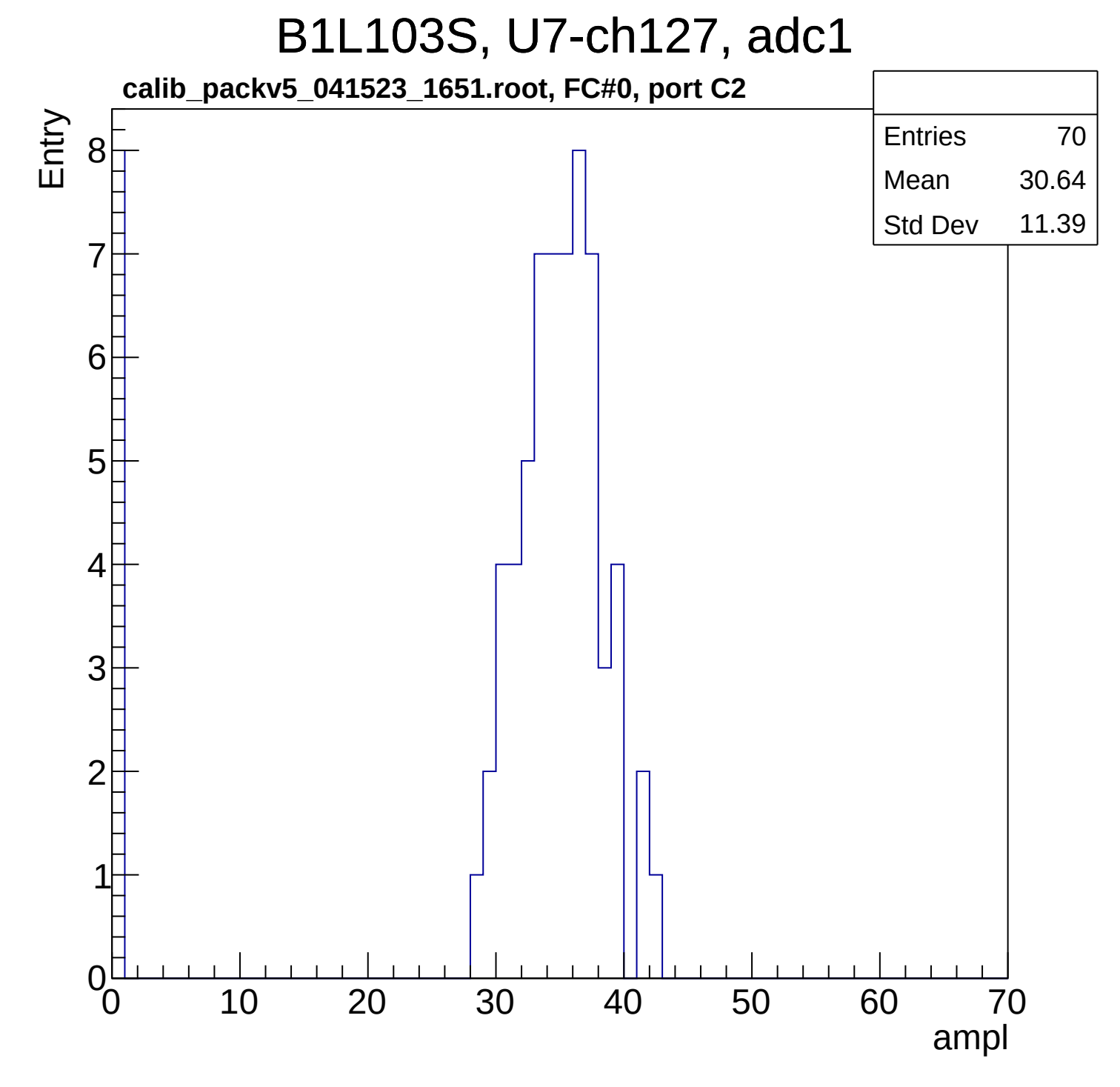
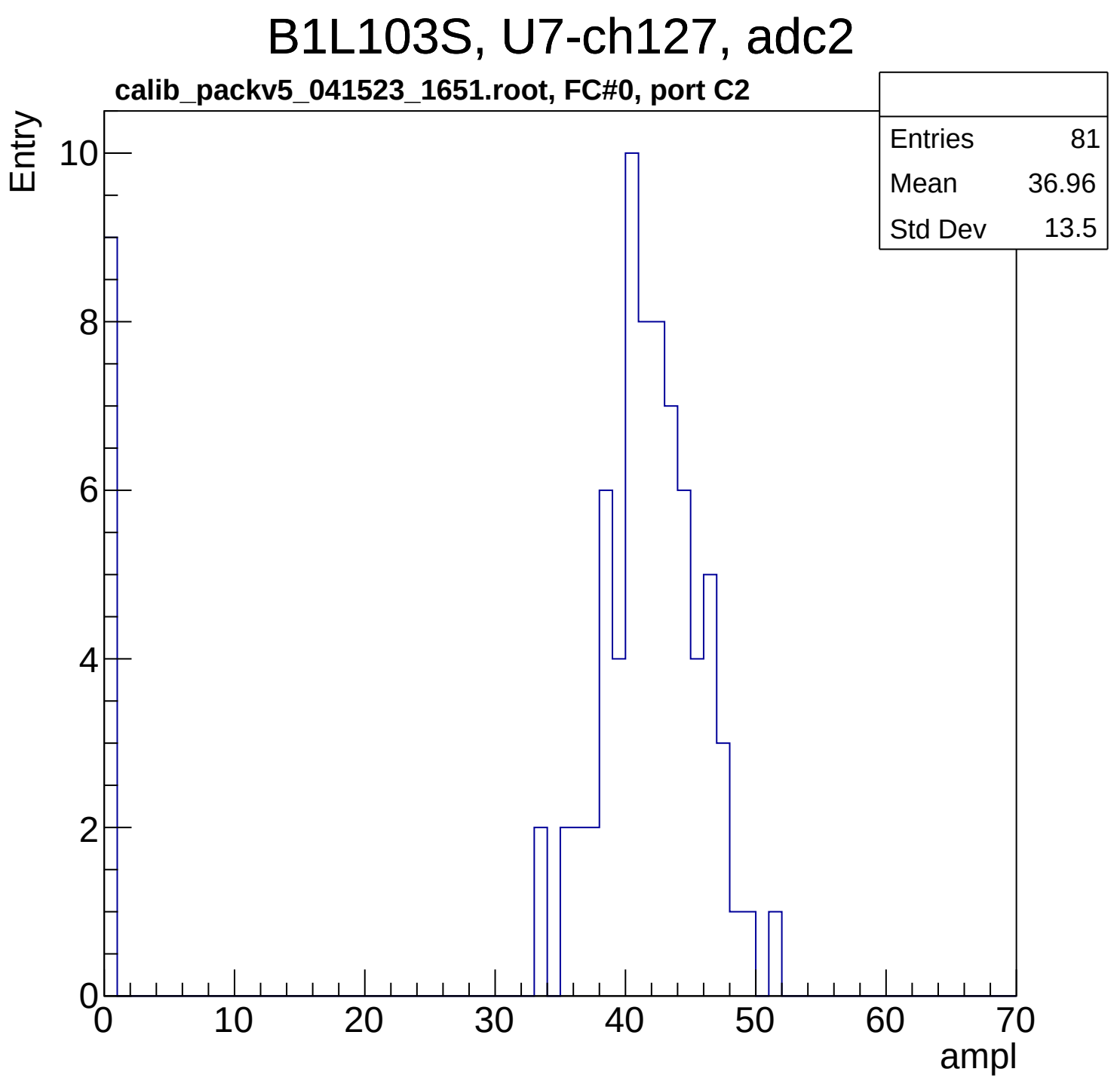
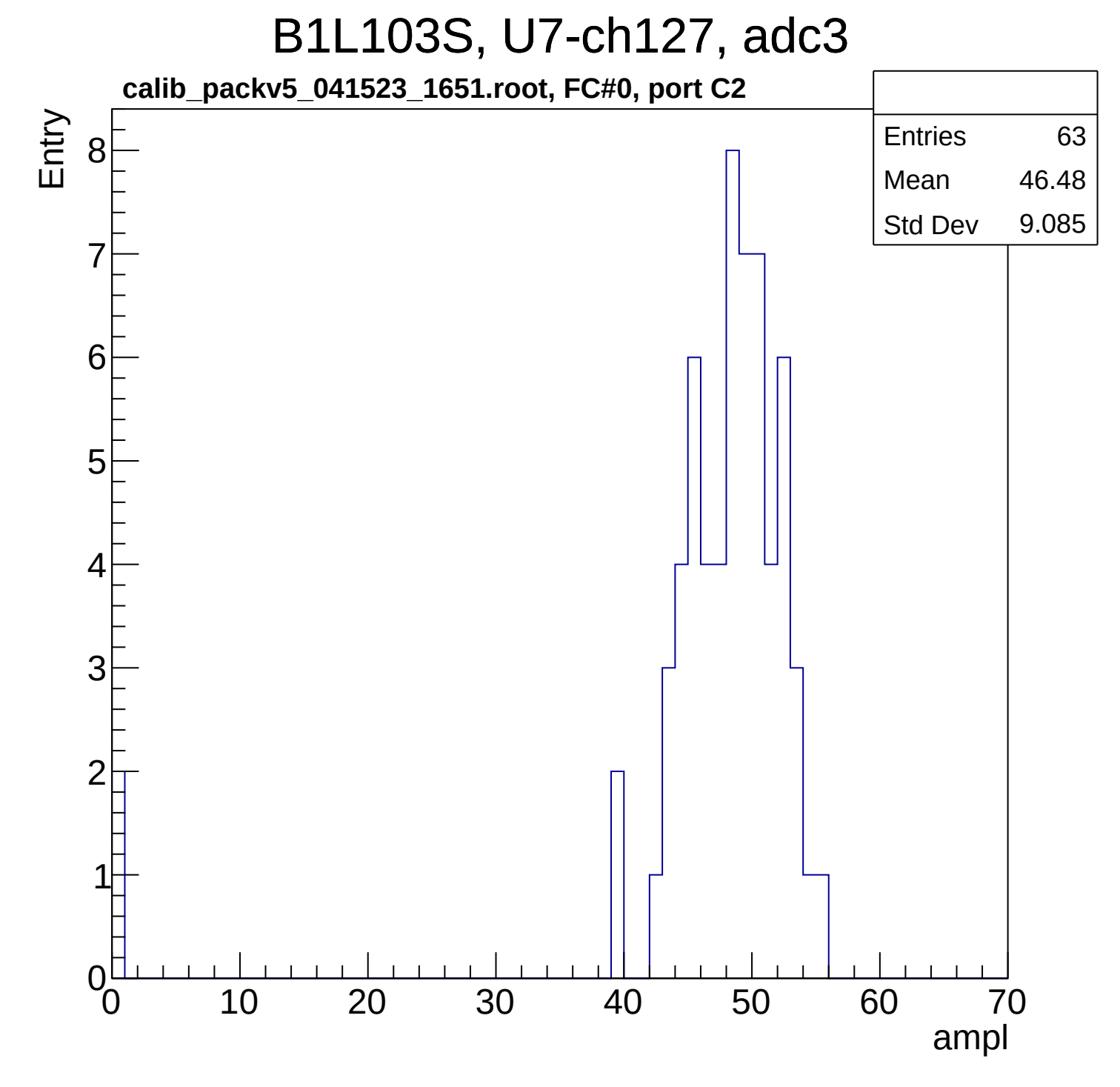
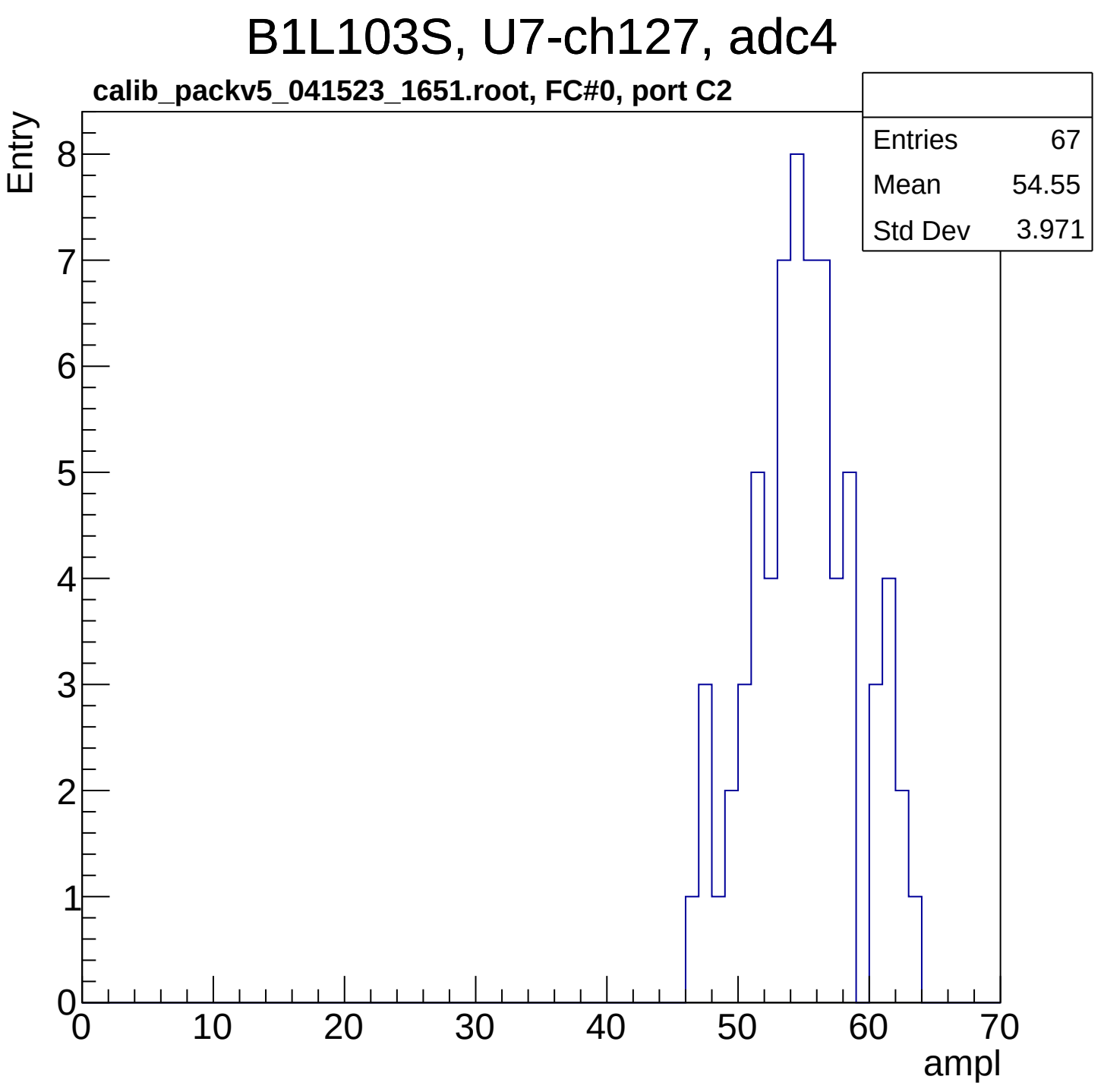
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl

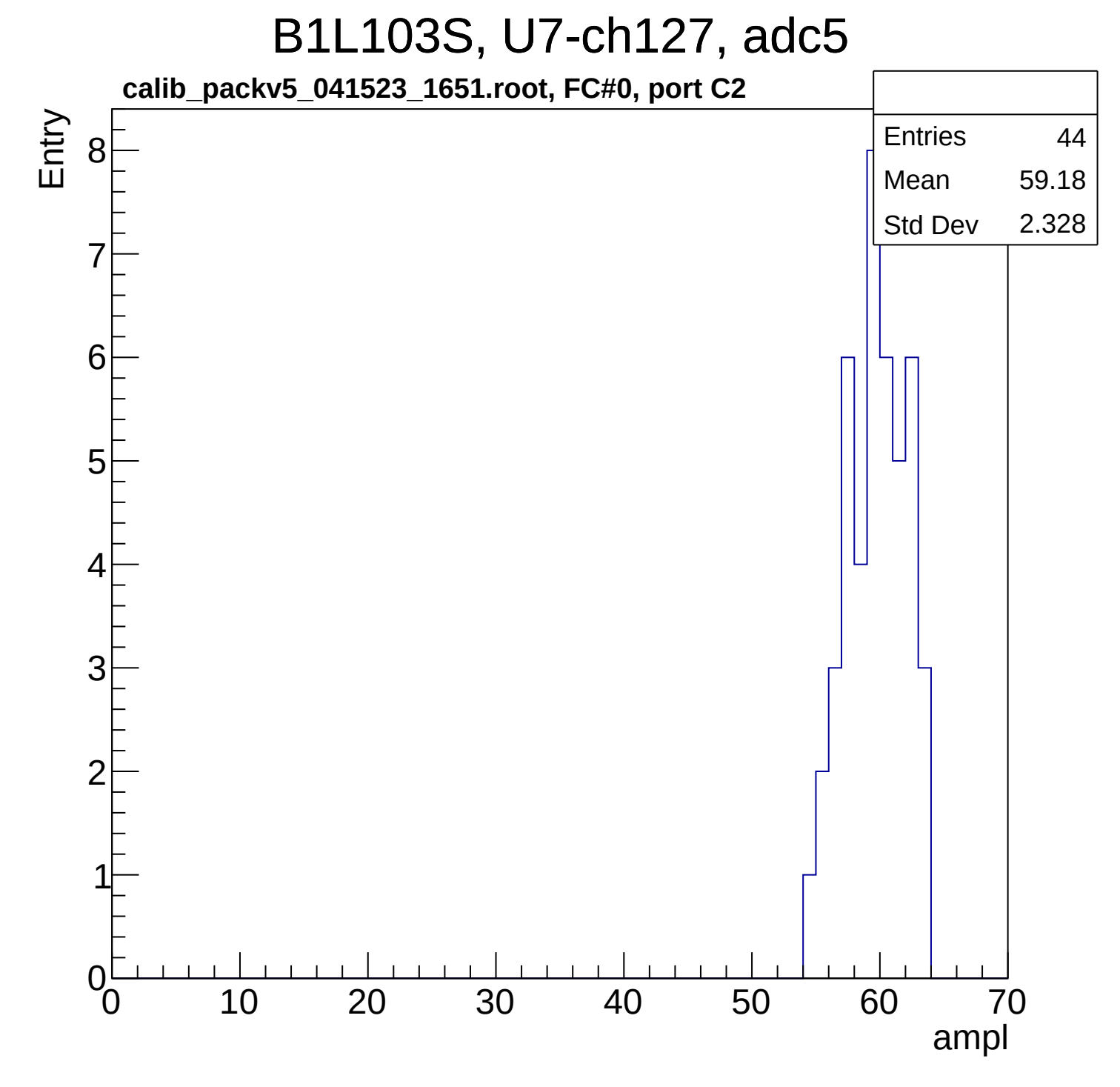

B1L103S, U7-ch127, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 92
Mean 23.36
Std Dev 10.23
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl

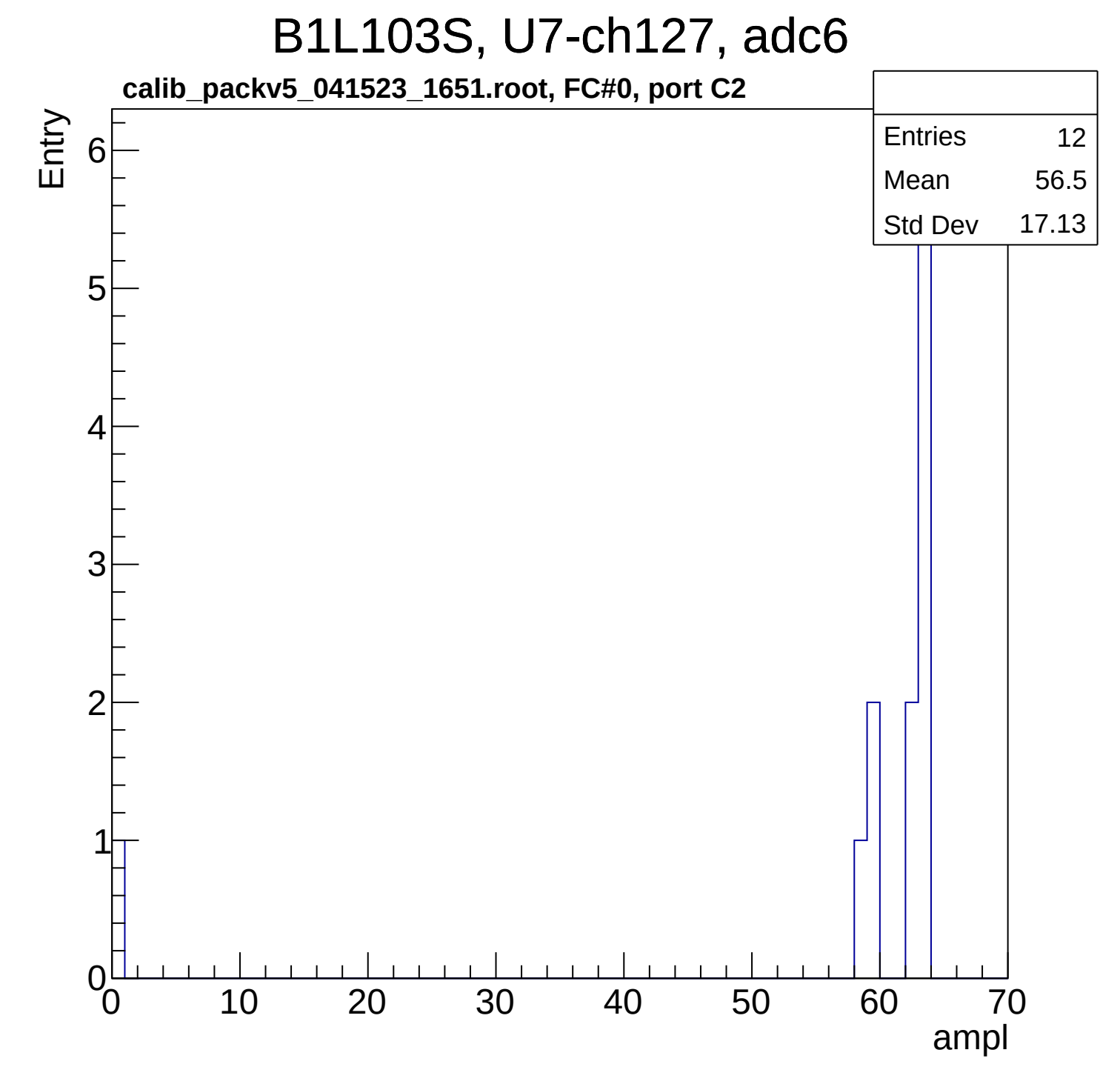

B1L103S, U7-ch127, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 30.64
Std Dev 11.39
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

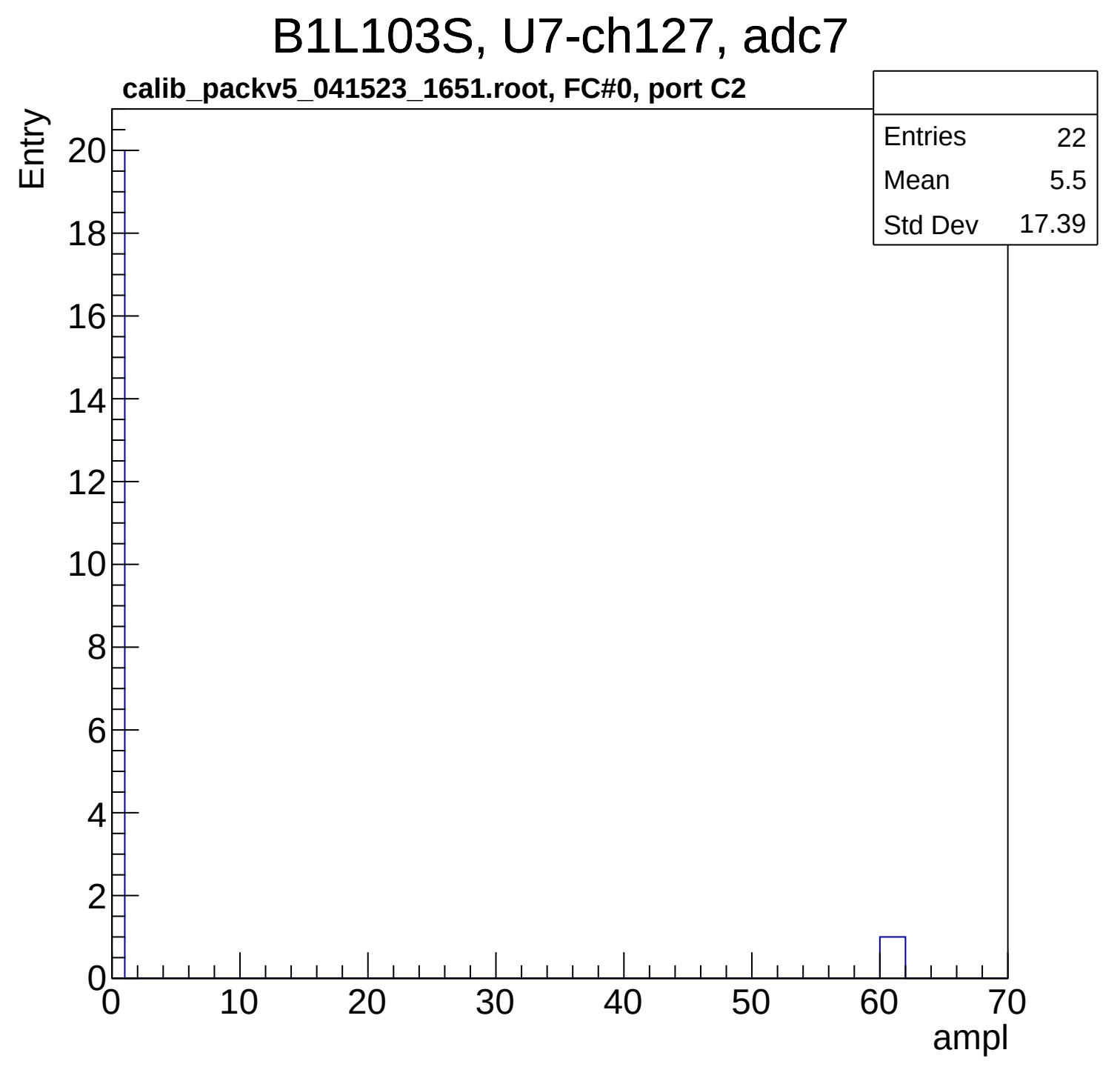

B1L103S, U7-ch127, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 36.96
Std Dev 13.5
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

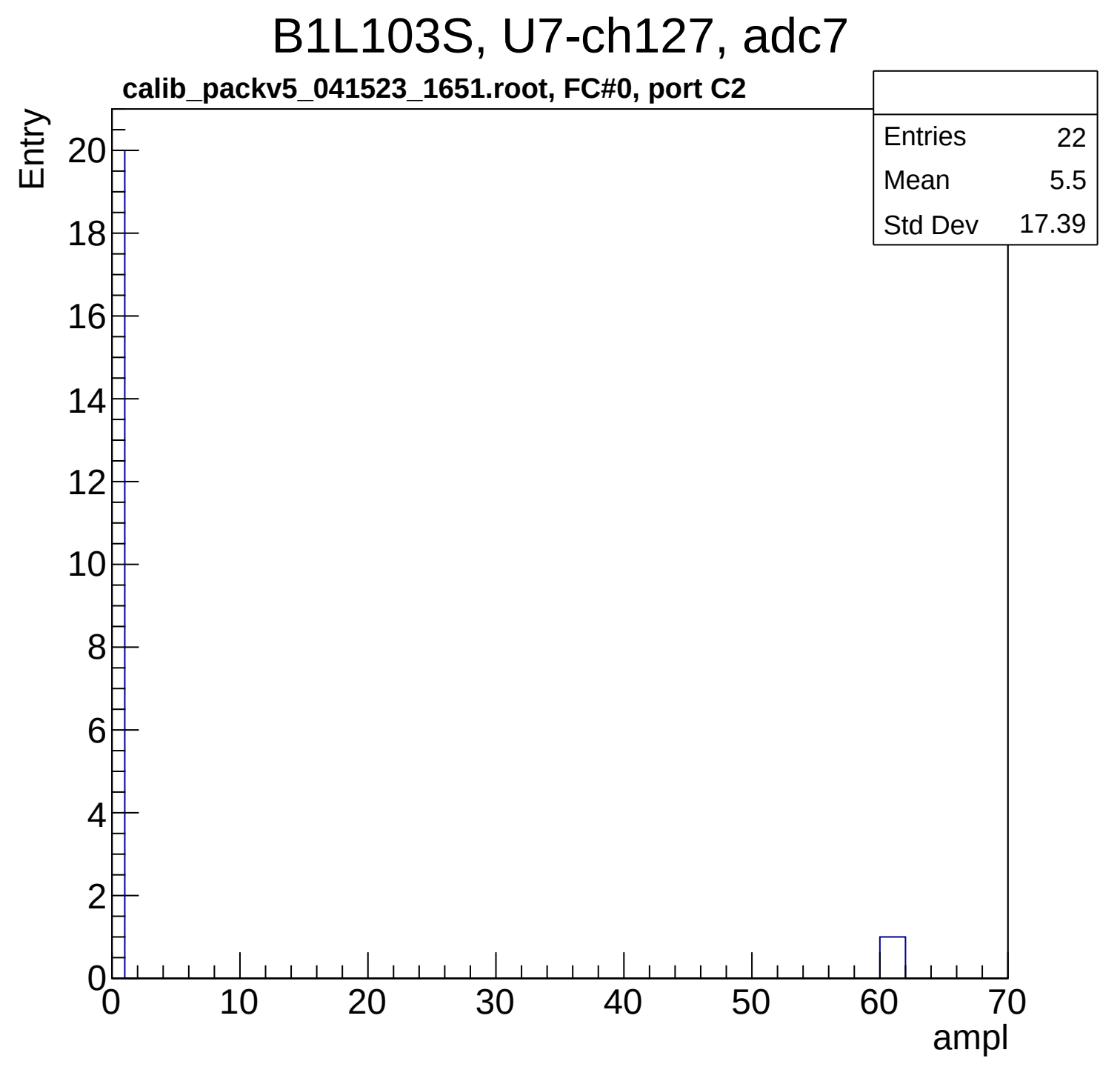

B1L103S, U7-ch127, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 46.48
Std Dev 9.085
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch127, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 54.55
Std Dev 3.971
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch127, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 59.18
Std Dev 2.328
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U7-ch127, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 56.5
Std Dev 17.13
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U7-ch127, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 5.5
Std Dev 17.39
Entry
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70
ampl


B1L103S, U7-ch127, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 5.5
Std Dev 17.39
Entry
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70
ampl