



# B1L003S, U18-ch0, adc0

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch0, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch0, adc2

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U18-ch0, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch0, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch0, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch0, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0



# B1L003S, U18-ch0, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch1, adc0

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U18-ch1, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U18-ch1, adc2

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch1, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch1, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch1, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U18-ch1, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0



# B1L003S, U18-ch1, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch2, adc0

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U18-ch2, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U18-ch2, adc2

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U18-ch2, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch2, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch2, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch2, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0



# B1L003S, U18-ch2, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch3, adc0

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch3, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U18-ch3, adc2

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch3, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch3, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch3, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch3, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0



# B1L003S, U18-ch3, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch4, adc0

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U18-ch4, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch4, adc2

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U18-ch4, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch4, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch4, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch4, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0



# B1L003S, U18-ch4, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch5, adc0

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U18-ch5, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U18-ch5, adc2

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U18-ch5, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch5, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch5, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch5, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0



# B1L003S, U18-ch5, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch6, adc0

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U18-ch6, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U18-ch6, adc2

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U18-ch6, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch6, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch6, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch6, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0



# B1L003S, U18-ch6, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch7, adc0

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U18-ch7, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch7, adc2

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U18-ch7, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch7, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch7, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch7, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0



# B1L003S, U18-ch7, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch8, adc0

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U18-ch8, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch8, adc2

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U18-ch8, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch8, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch8, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch8, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0



# B1L003S, U18-ch8, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch9, adc0

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch9, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch9, adc2

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U18-ch9, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

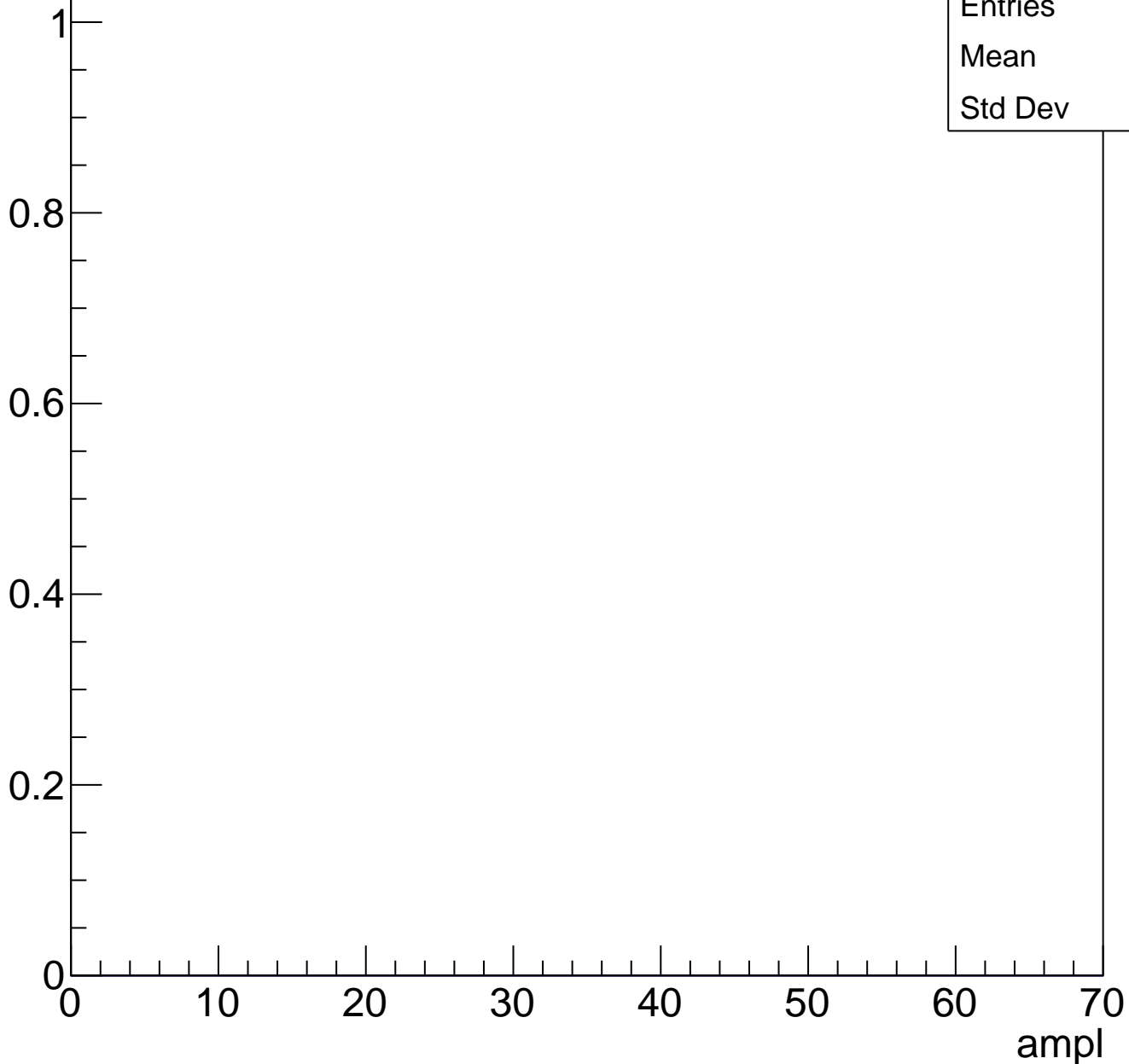


Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch9, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch9, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

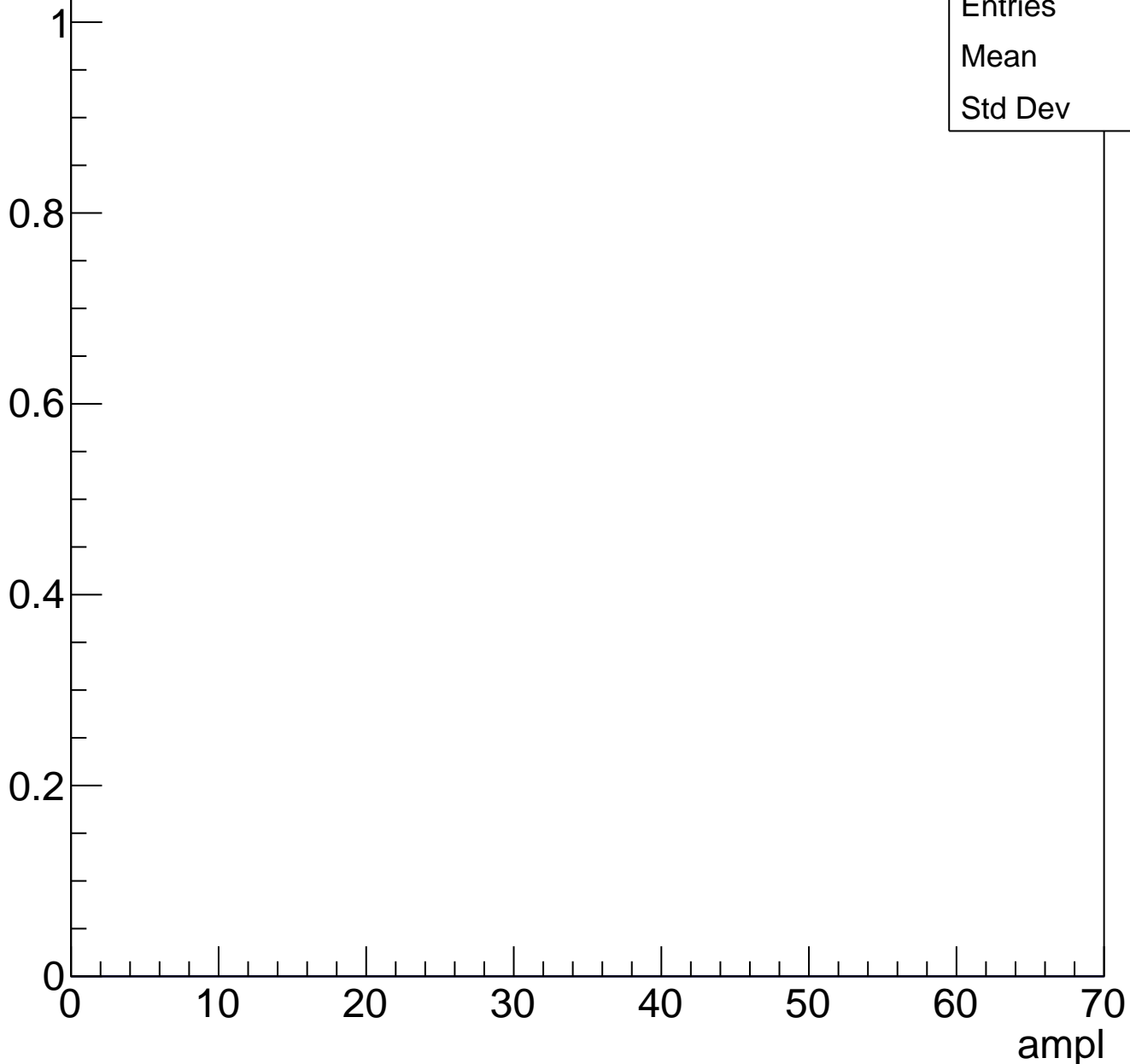


Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch9, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0



# B1L003S, U18-ch9, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch10, adc0

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U18-ch10, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U18-ch10, adc2

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch10, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch10, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch10, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch10, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0



# B1L003S, U18-ch10, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch11, adc0

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U18-ch11, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U18-ch11, adc2

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U18-ch11, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch11, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch11, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch11, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0



# B1L003S, U18-ch11, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch12, adc0

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U18-ch12, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch12, adc2

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U18-ch12, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch12, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch12, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U18-ch12, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U18-ch12, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch13, adc0

calib\_packv5\_042523\_0143.root, FC#13, port D2

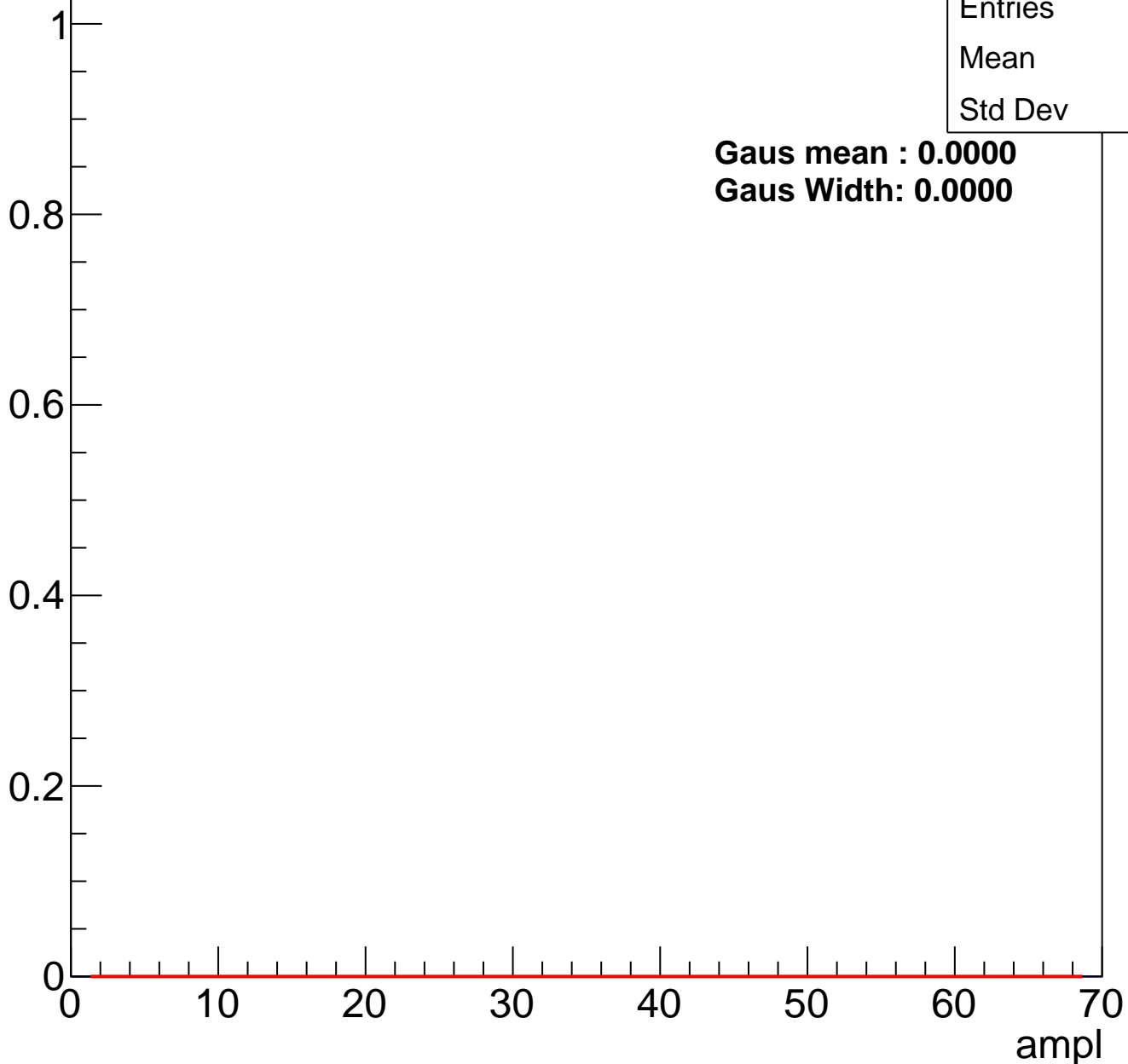
Entry



# B1L003S, U18-ch13, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U18-ch13, adc2

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U18-ch13, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch13, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch13, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch13, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

1

0.8

0.6

0.4

0.2

0

0

10

20

30

40

50

60

70

ampl

Entries

0

Mean

0

Std Dev

0



# B1L003S, U18-ch13, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch14, adc0

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U18-ch14, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

**Gaus mean : 0.0000**

**Gaus Width: 0.0000**

# B1L003S, U18-ch14, adc2

calib\_packv5\_042523\_0143.root, FC#13, port D2

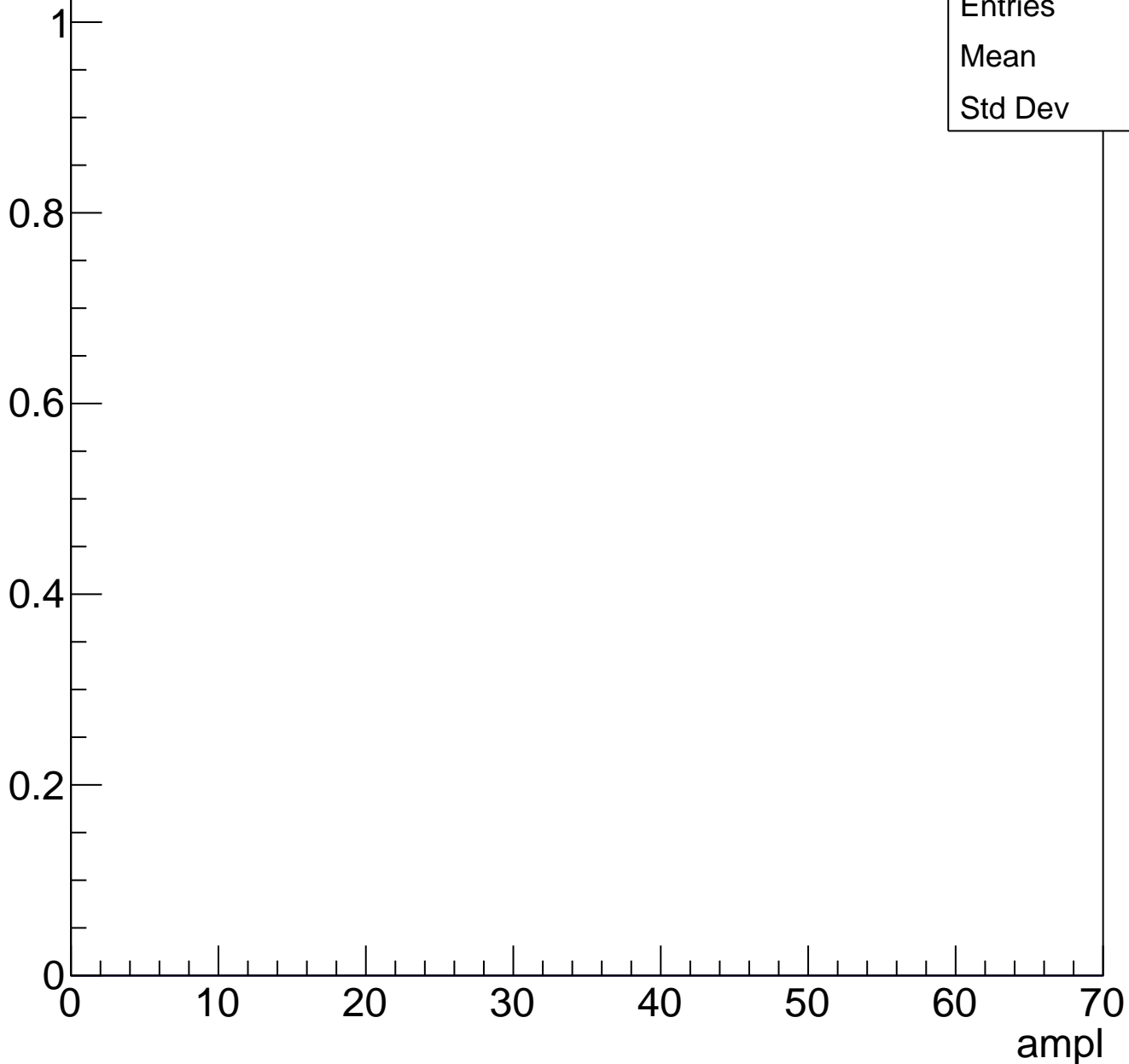
Entry



# B1L003S, U18-ch14, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch14, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch14, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch14, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0



# B1L003S, U18-ch14, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch15, adc0

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U18-ch15, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U18-ch15, adc2

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch15, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch15, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch15, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch15, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

1

0.8

0.6

0.4

0.2

0

0

10

20

30

40

50

60

70

ampl

Entries

0

Mean

0

Std Dev

0



# B1L003S, U18-ch15, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch16, adc0

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U18-ch16, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch16, adc2

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U18-ch16, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch16, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

1

0.8

0.6

0.4

0.2

0

0

10

20

30

40

50

60

70

ampl

Entries

0

Mean

0

Std Dev

0

# B1L003S, U18-ch16, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U18-ch16, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0



# B1L003S, U18-ch16, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch17, adc0

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U18-ch17, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U18-ch17, adc2

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U18-ch17, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch17, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch17, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch17, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0



# B1L003S, U18-ch17, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch18, adc0

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch18, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U18-ch18, adc2

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U18-ch18, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch18, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch18, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch18, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0



# B1L003S, U18-ch18, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch19, adc0

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U18-ch19, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U18-ch19, adc2

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U18-ch19, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch19, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch19, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch19, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0



# B1L003S, U18-ch19, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch20, adc0

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch20, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U18-ch20, adc2

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U18-ch20, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch20, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch20, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch20, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0



# B1L003S, U18-ch20, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch21, adc0

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U18-ch21, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U18-ch21, adc2

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



**Gaus mean : 0.0000**

**Gaus Width: 0.0000**

Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch21, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U18-ch21, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch21, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch21, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0



# B1L003S, U18-ch21, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch22, adc0

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U18-ch22, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch22, adc2

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U18-ch22, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch22, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch22, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch22, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0



# B1L003S, U18-ch22, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch23, adc0

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch23, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U18-ch23, adc2

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch23, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch23, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch23, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch23, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



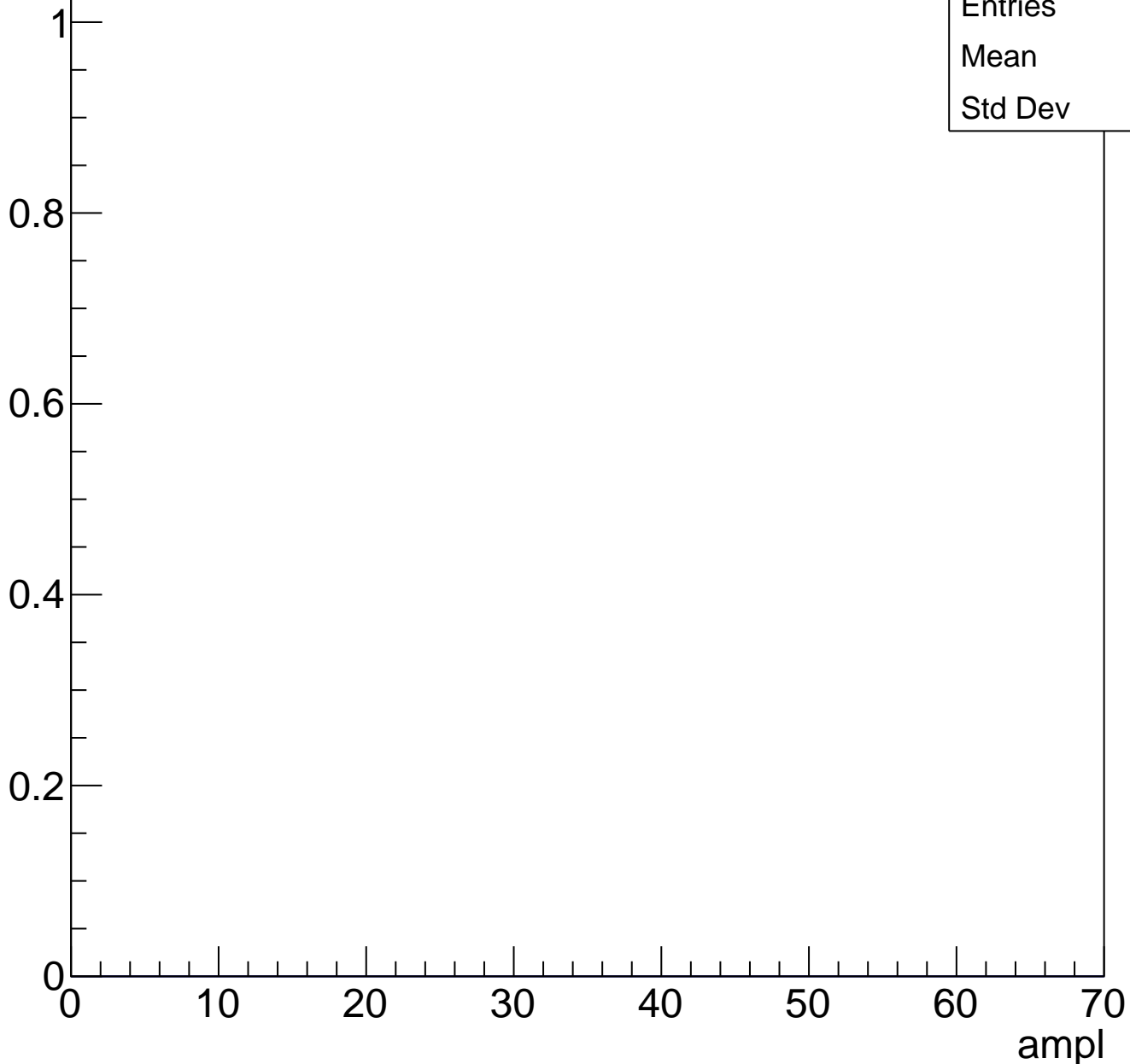
Entries	0
Mean	0
Std Dev	0



# B1L003S, U18-ch23, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch24, adc0

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U18-ch24, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U18-ch24, adc2

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U18-ch24, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch24, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch24, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch24, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0



# B1L003S, U18-ch24, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch25, adc0

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U18-ch25, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch25, adc2

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U18-ch25, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch25, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch25, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch25, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0



# B1L003S, U18-ch25, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch26, adc0

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U18-ch26, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U18-ch26, adc2

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U18-ch26, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch26, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch26, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U18-ch26, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0



# B1L003S, U18-ch26, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch27, adc0

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch27, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U18-ch27, adc2

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U18-ch27, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch27, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch27, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch27, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0



# B1L003S, U18-ch27, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch28, adc0

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch28, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch28, adc2

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch28, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch28, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch28, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch28, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0



# B1L003S, U18-ch28, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U18-ch29, adc0

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U18-ch29, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U18-ch29, adc2

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U18-ch29, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch29, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch29, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch29, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0



# B1L003S, U18-ch29, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch30, adc0

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch30, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch30, adc2

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U18-ch30, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch30, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch30, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch30, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0



# B1L003S, U18-ch30, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch31, adc0

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U18-ch31, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U18-ch31, adc2

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U18-ch31, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch31, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

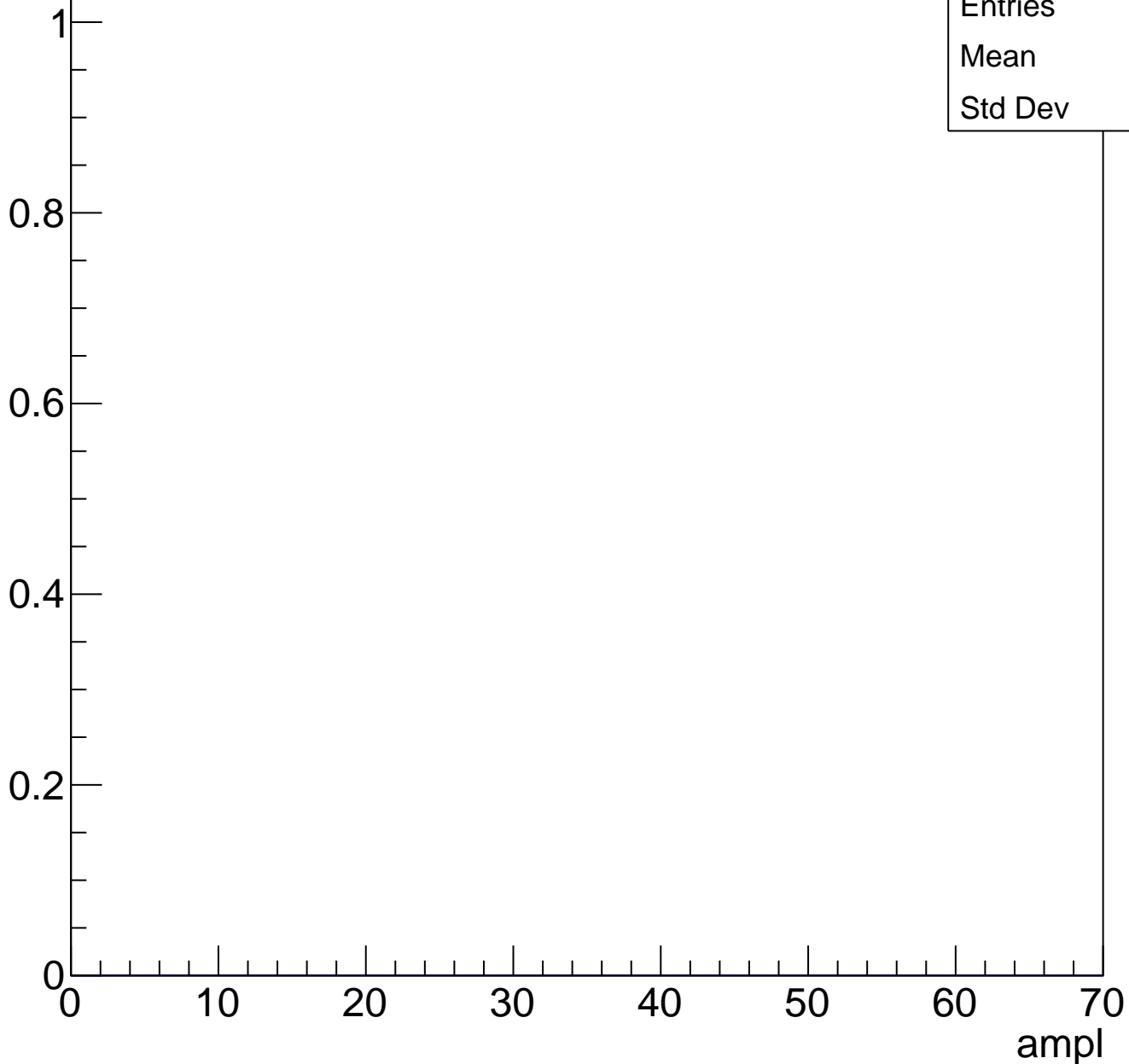


Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch31, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch31, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0



# B1L003S, U18-ch31, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch32, adc0

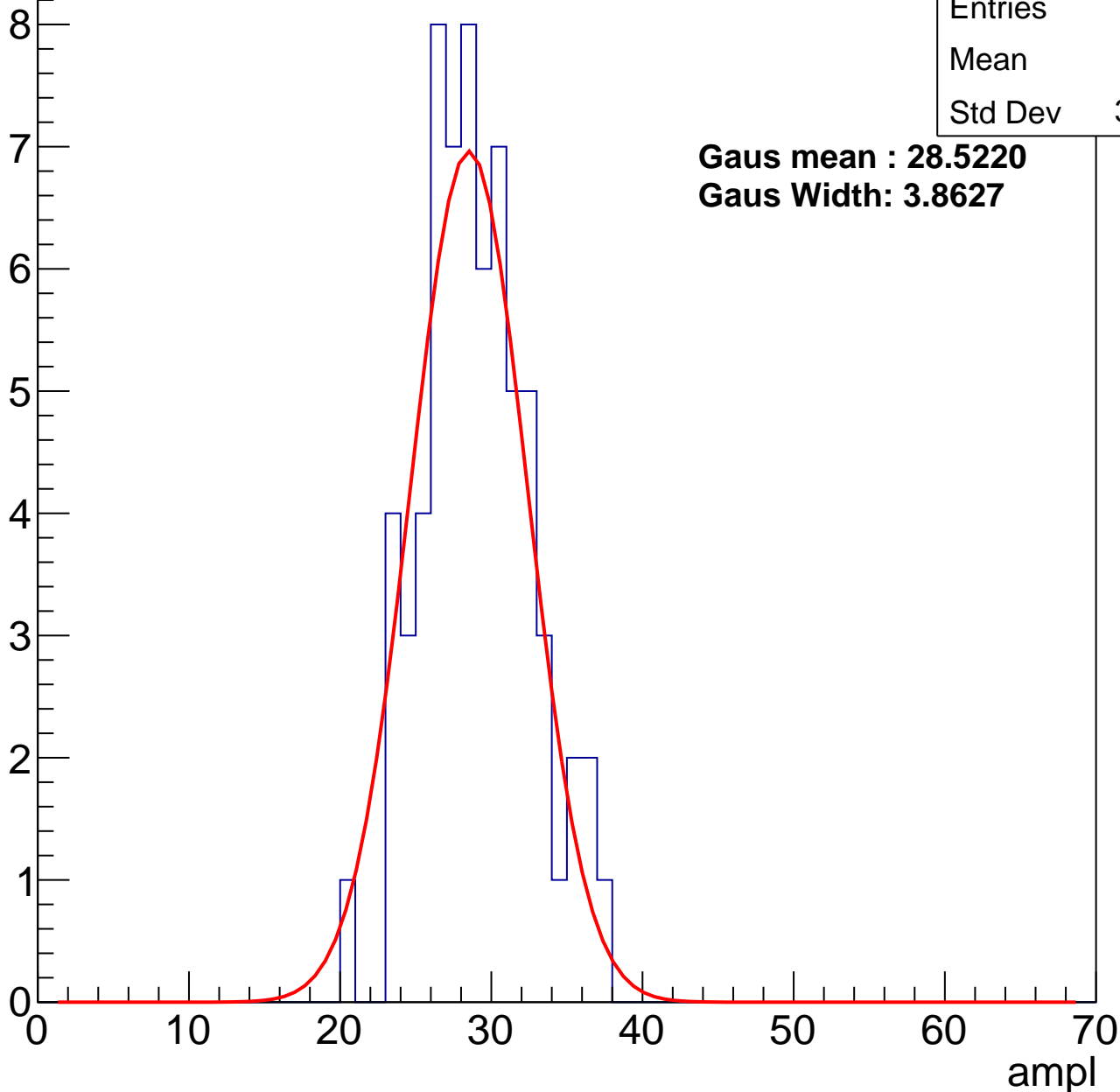
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	67
Mean	28.6
Std Dev	3.541

**Gaus mean : 28.5220**

**Gaus Width: 3.8627**



# B1L003S, U18-ch32, adc1

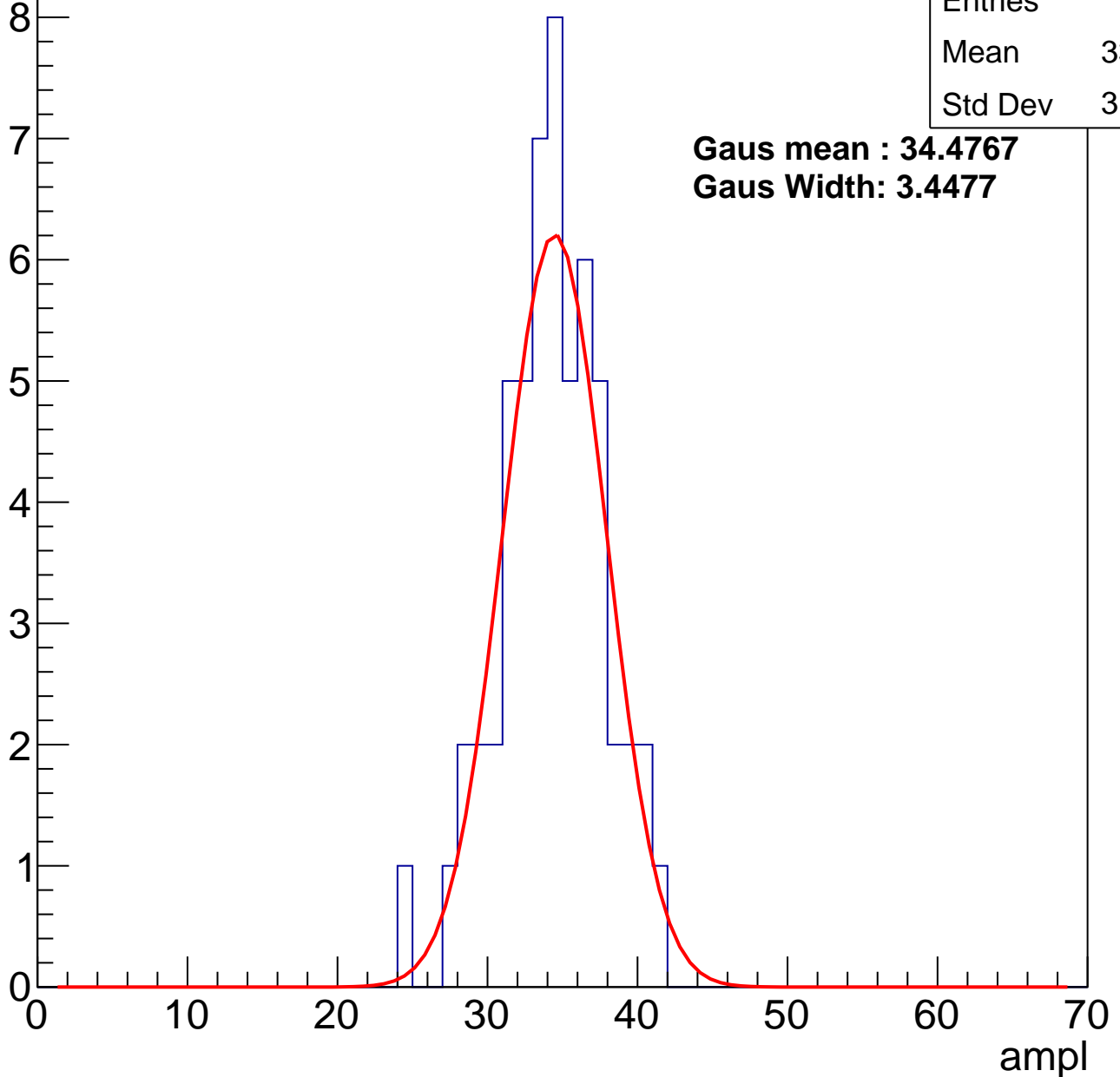
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	56
Mean	33.82
Std Dev	3.407

**Gaus mean : 34.4767**

**Gaus Width: 3.4477**



# B1L003S, U18-ch32, adc2

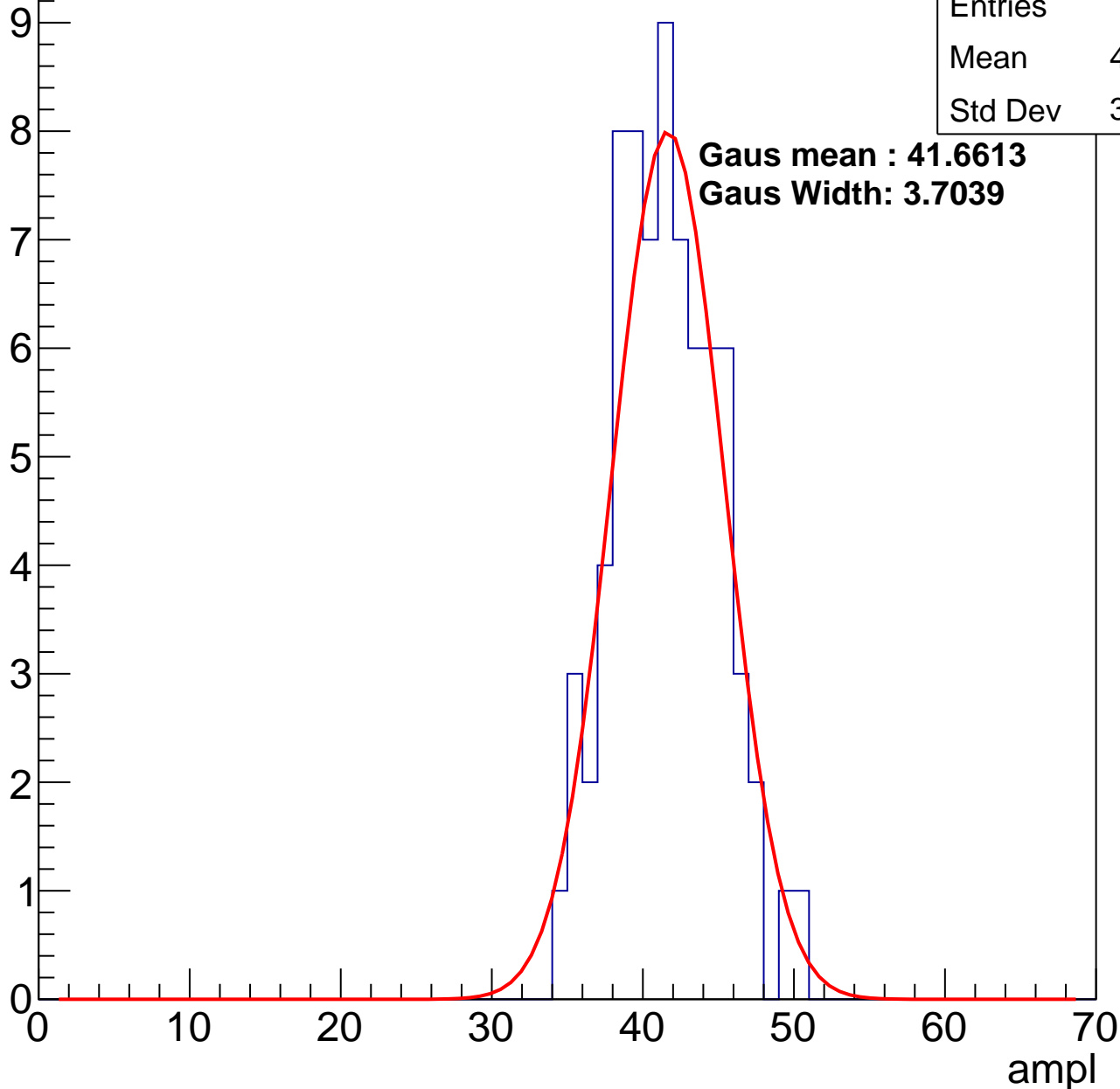
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	74
Mean	41.09
Std Dev	3.398

**Gaus mean : 41.6613**

**Gaus Width: 3.7039**

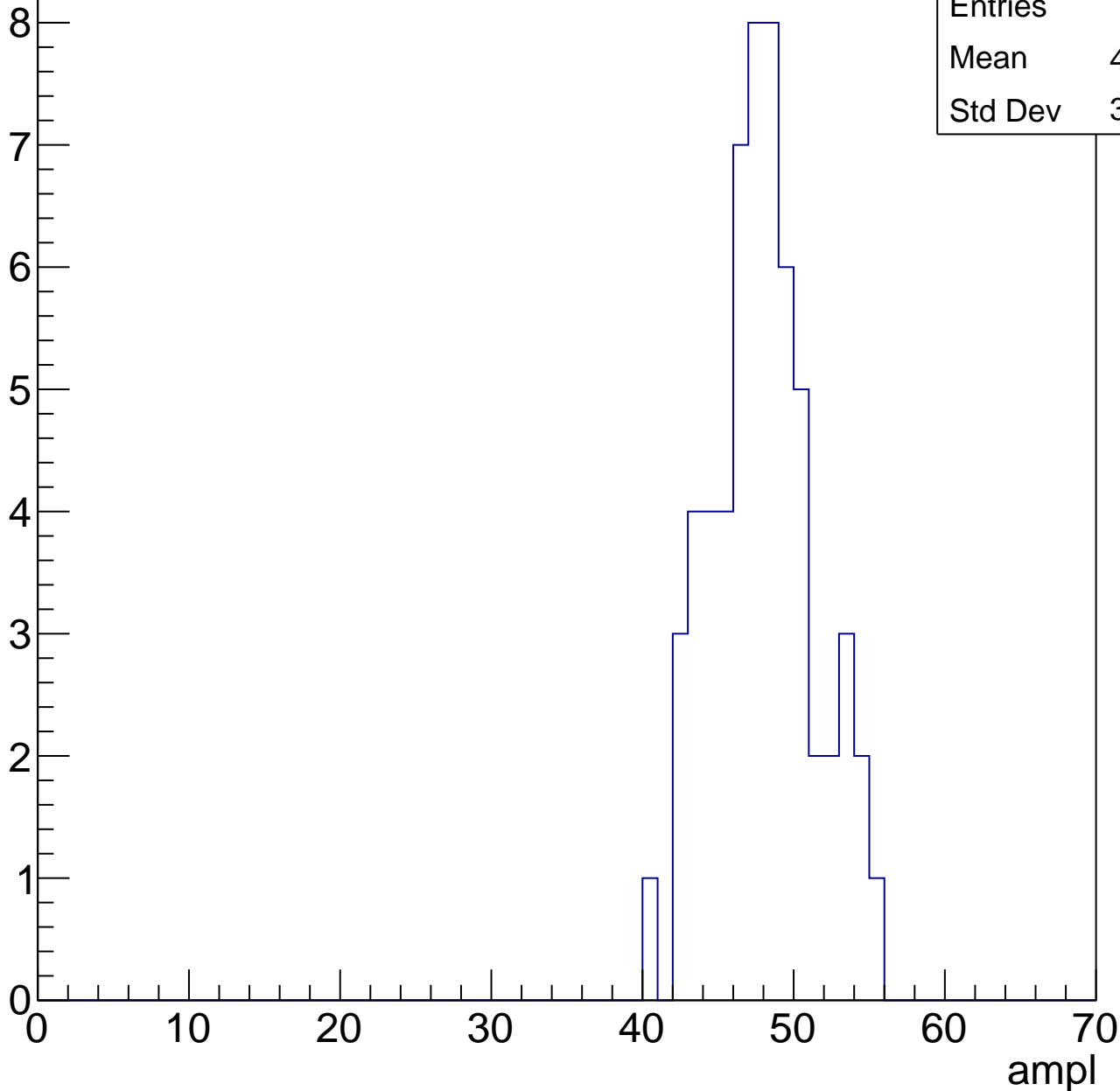


# B1L003S, U18-ch32, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	60
Mean	47.47
Std Dev	3.324

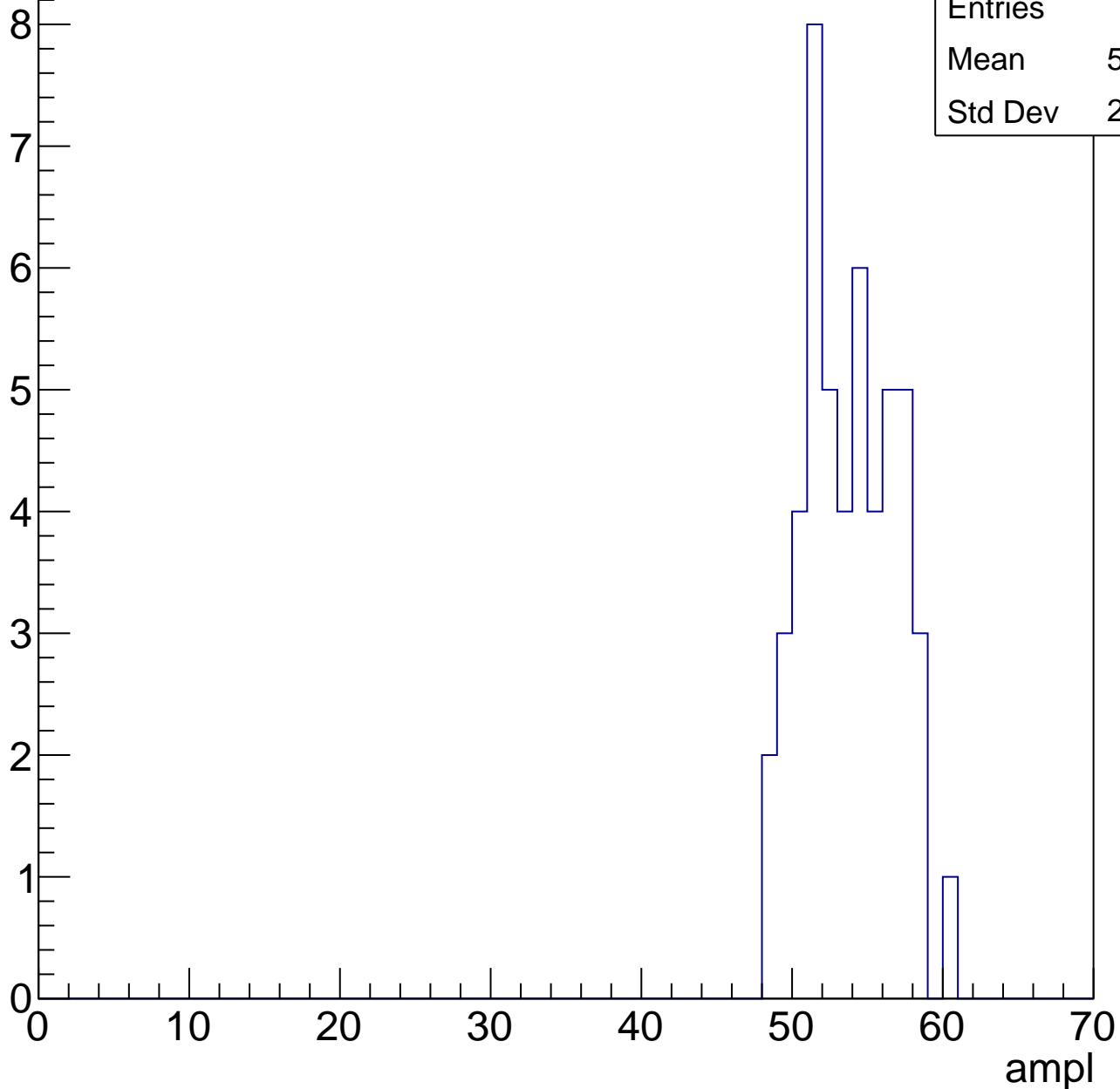


# B1L003S, U18-ch32, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

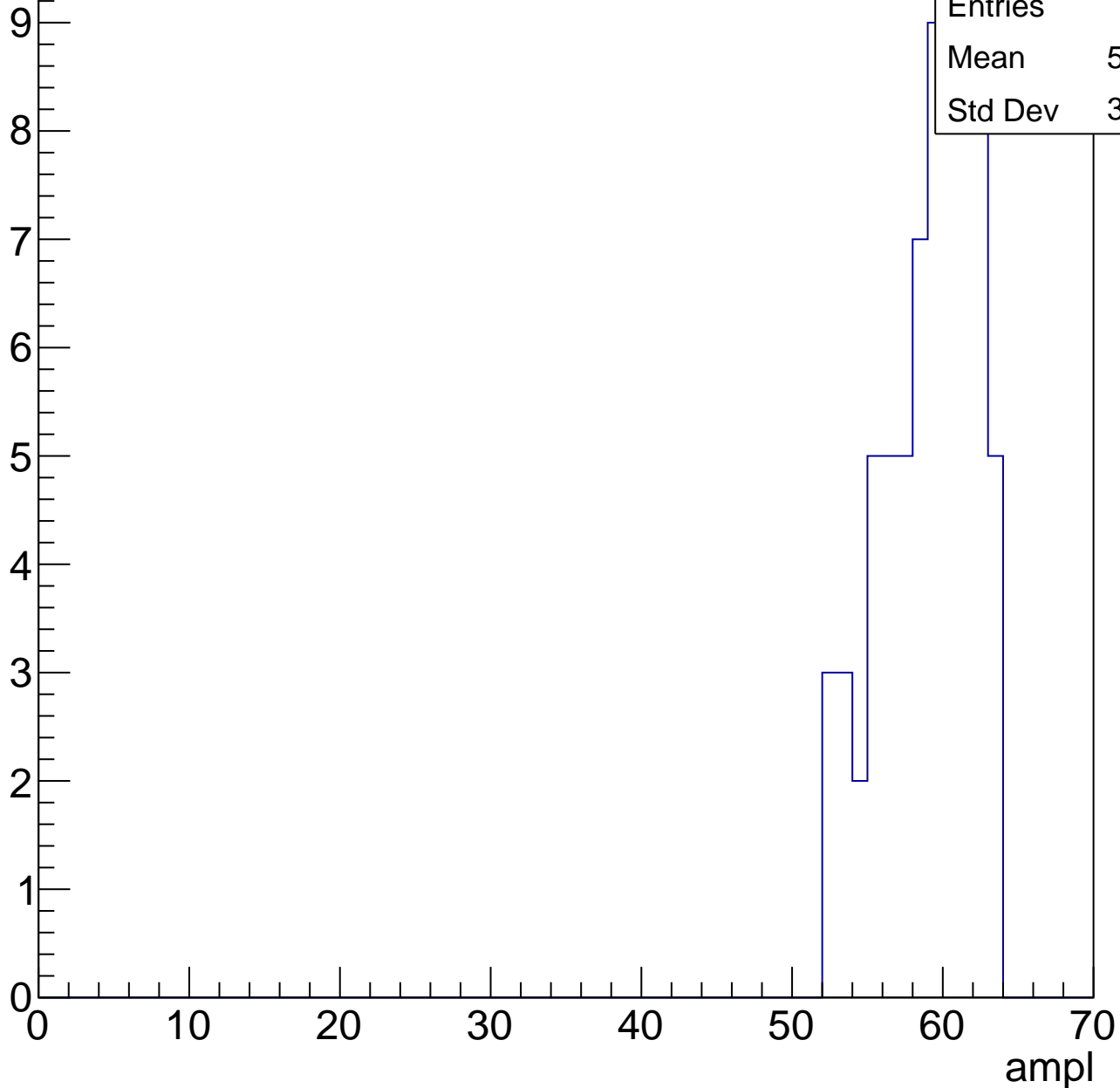
Entries	50
Mean	53.32
Std Dev	2.956



# B1L003S, U18-ch32, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

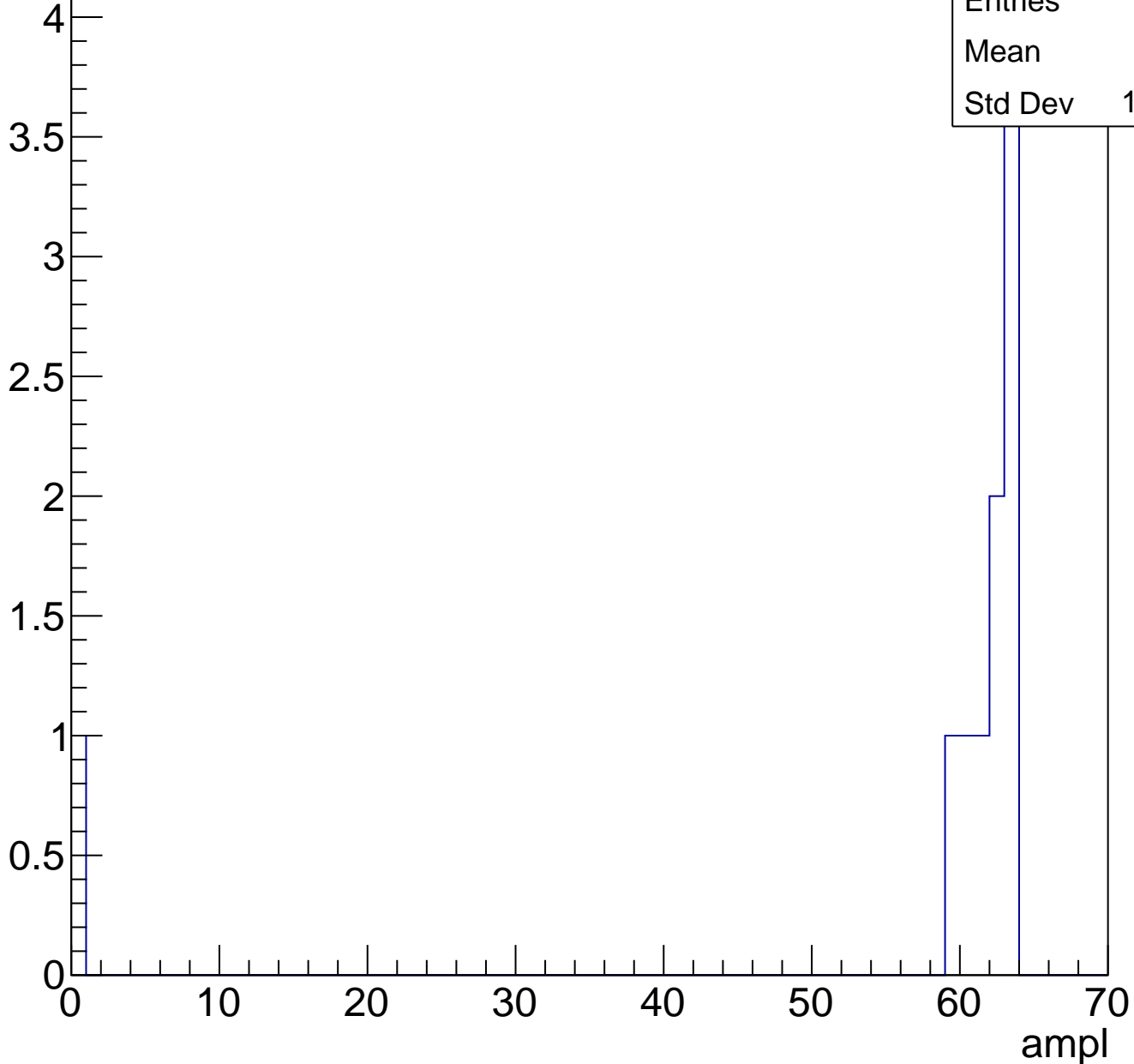
Entry



# B1L003S, U18-ch32, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U18-ch32, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	1
Mean	63
Std Dev	0

# B1L003S, U18-ch33, adc0

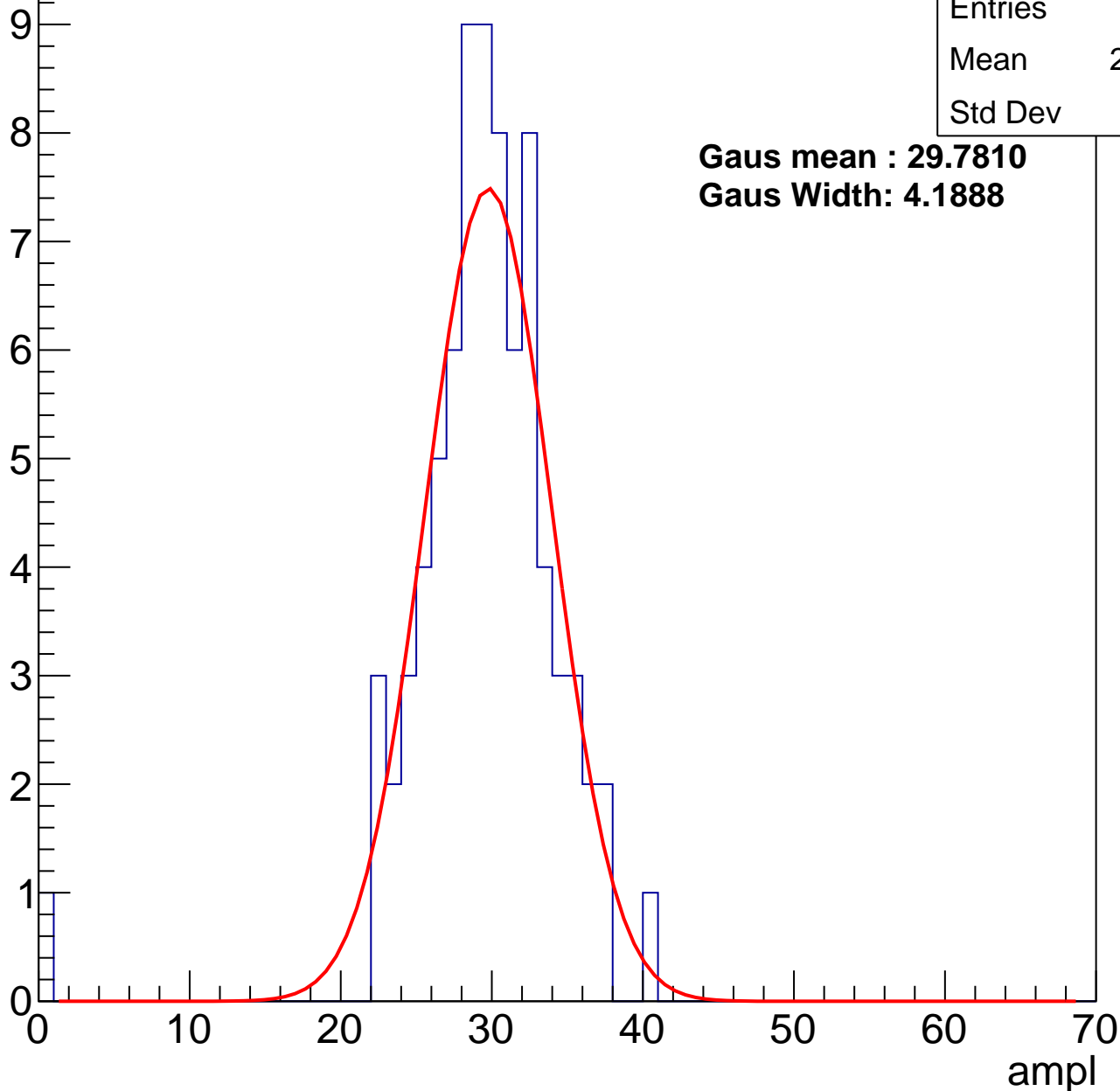
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	79
Mean	29.06
Std Dev	5

**Gaus mean : 29.7810**

**Gaus Width: 4.1888**



# B1L003S, U18-ch33, adc1

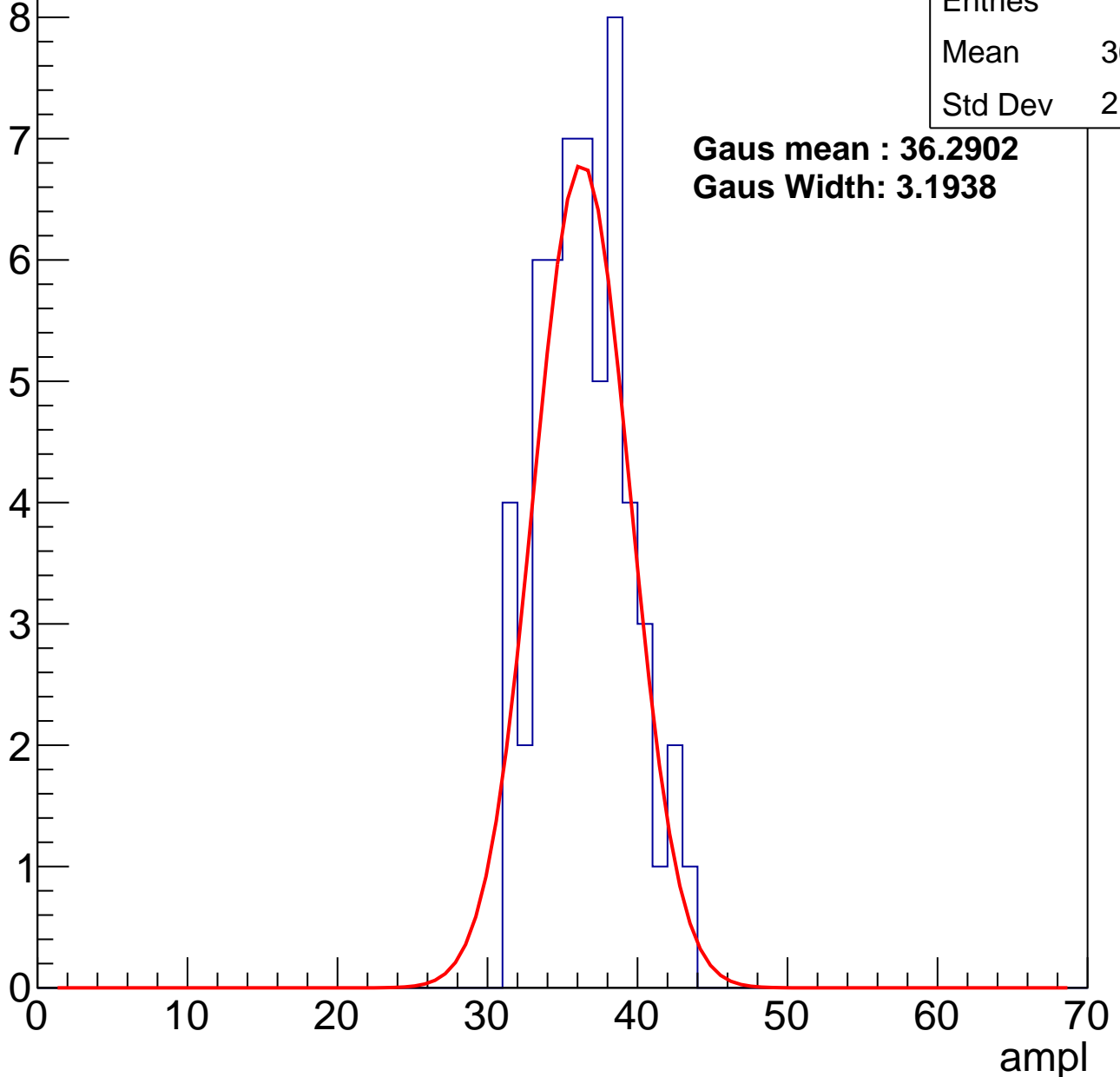
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	56
Mean	36.07
Std Dev	2.939

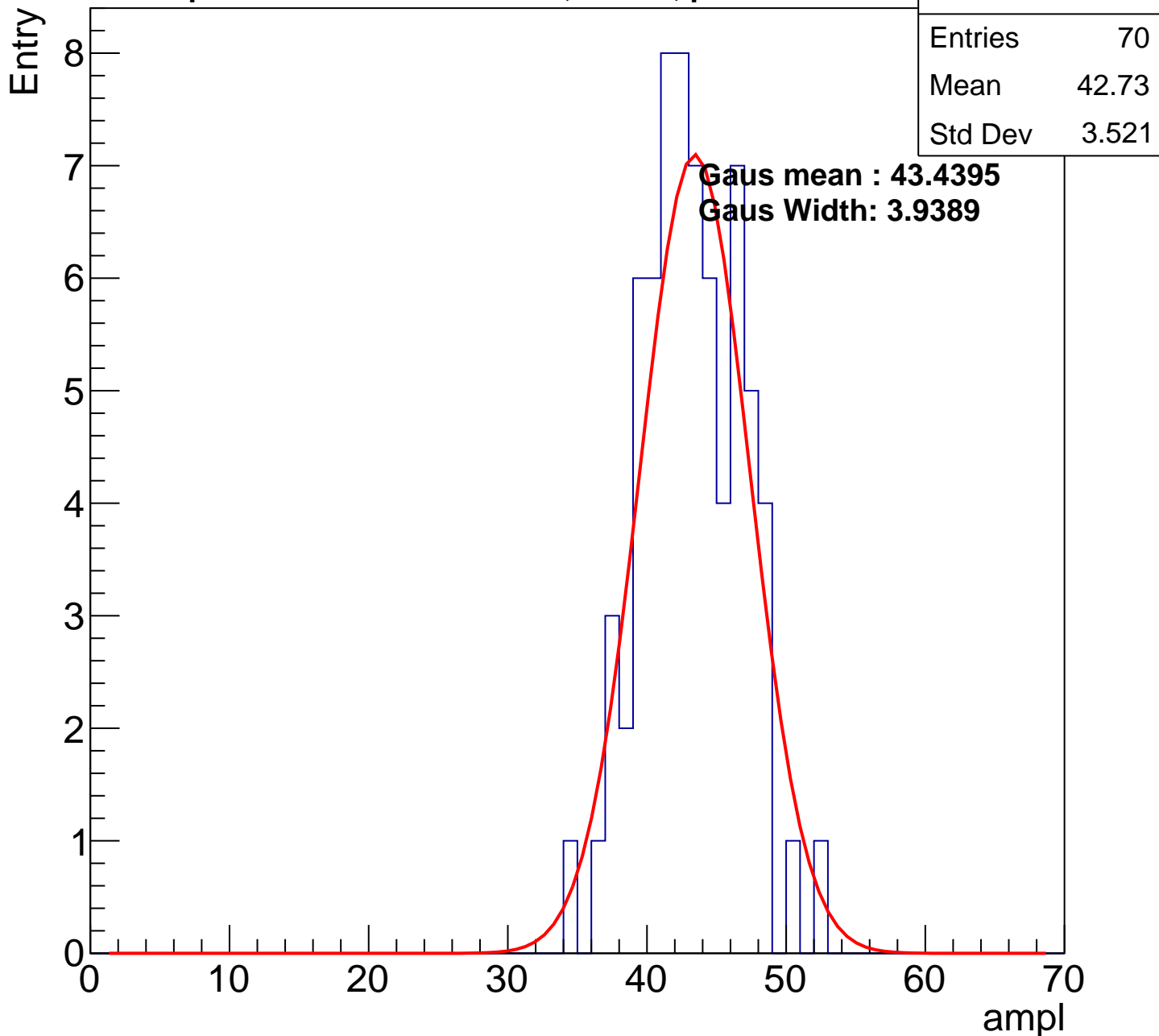
**Gaus mean : 36.2902**

**Gaus Width: 3.1938**



# B1L003S, U18-ch33, adc2

calib\_packv5\_042523\_0143.root, FC#13, port D2

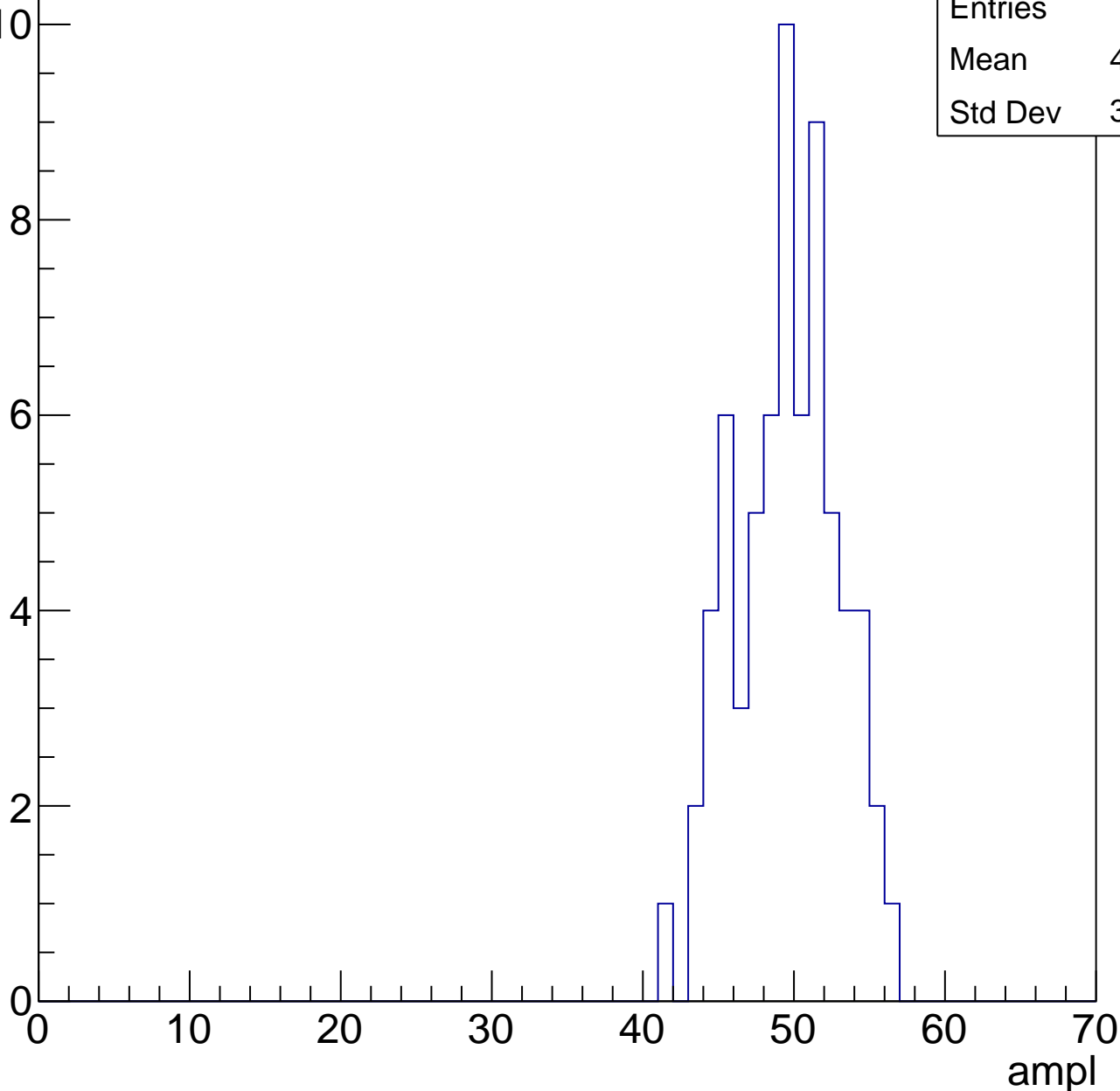


# B1L003S, U18-ch33, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	68
Mean	49.07
Std Dev	3.336

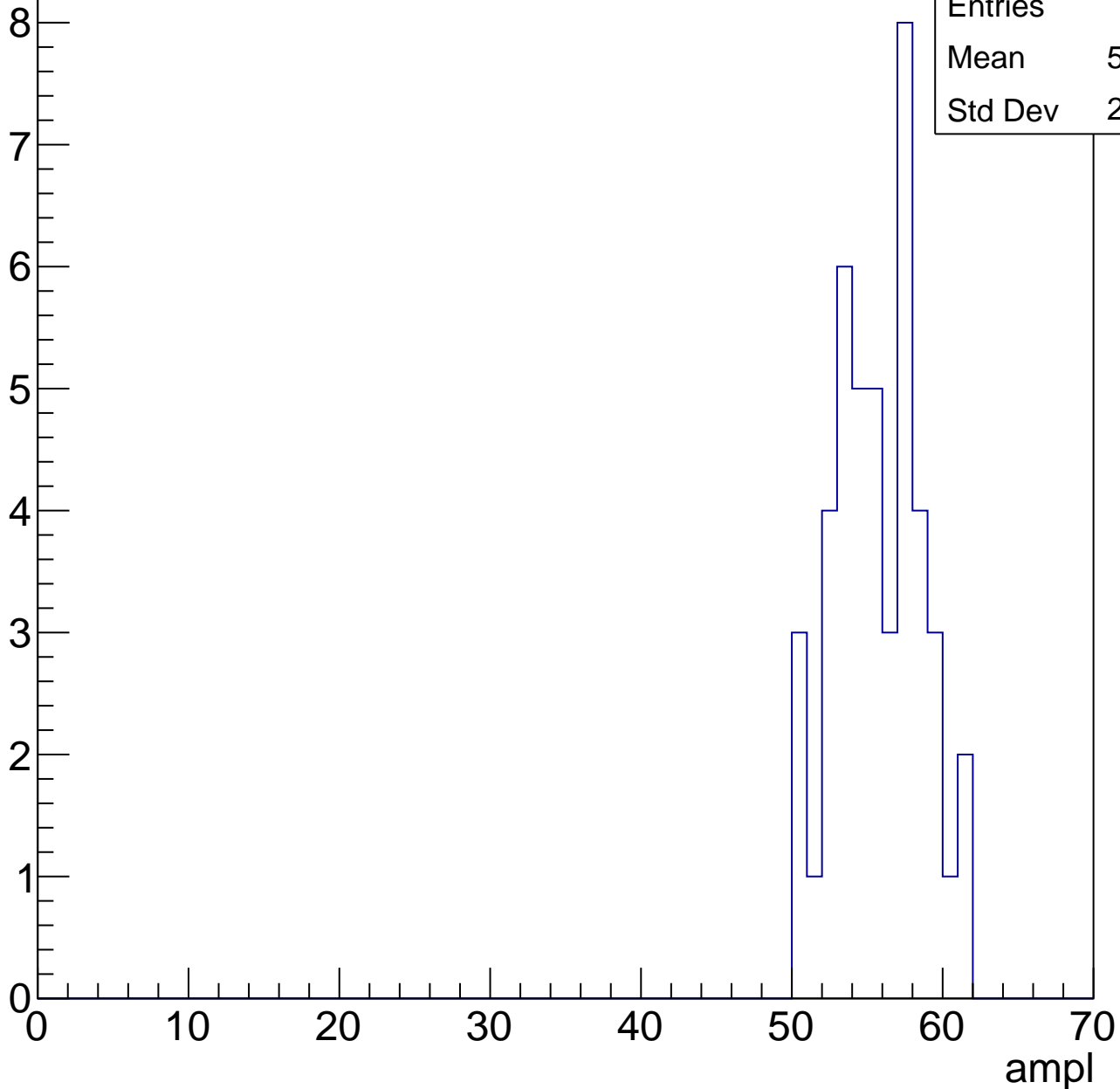


# B1L003S, U18-ch33, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	45
Mean	55.27
Std Dev	2.863



# B1L003S, U18-ch33, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

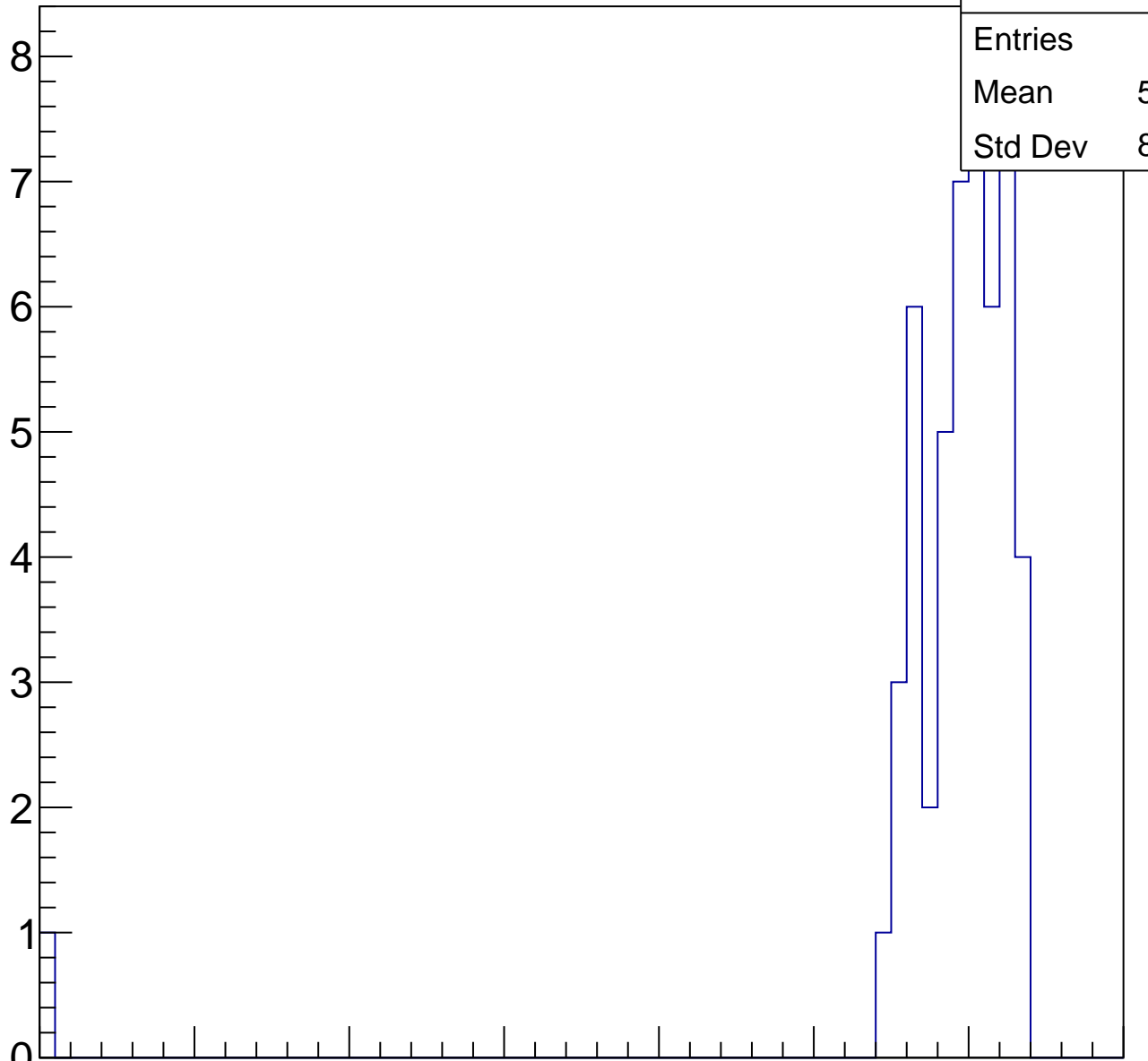
Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	51
Mean	58.16
Std Dev	8.578

ampl

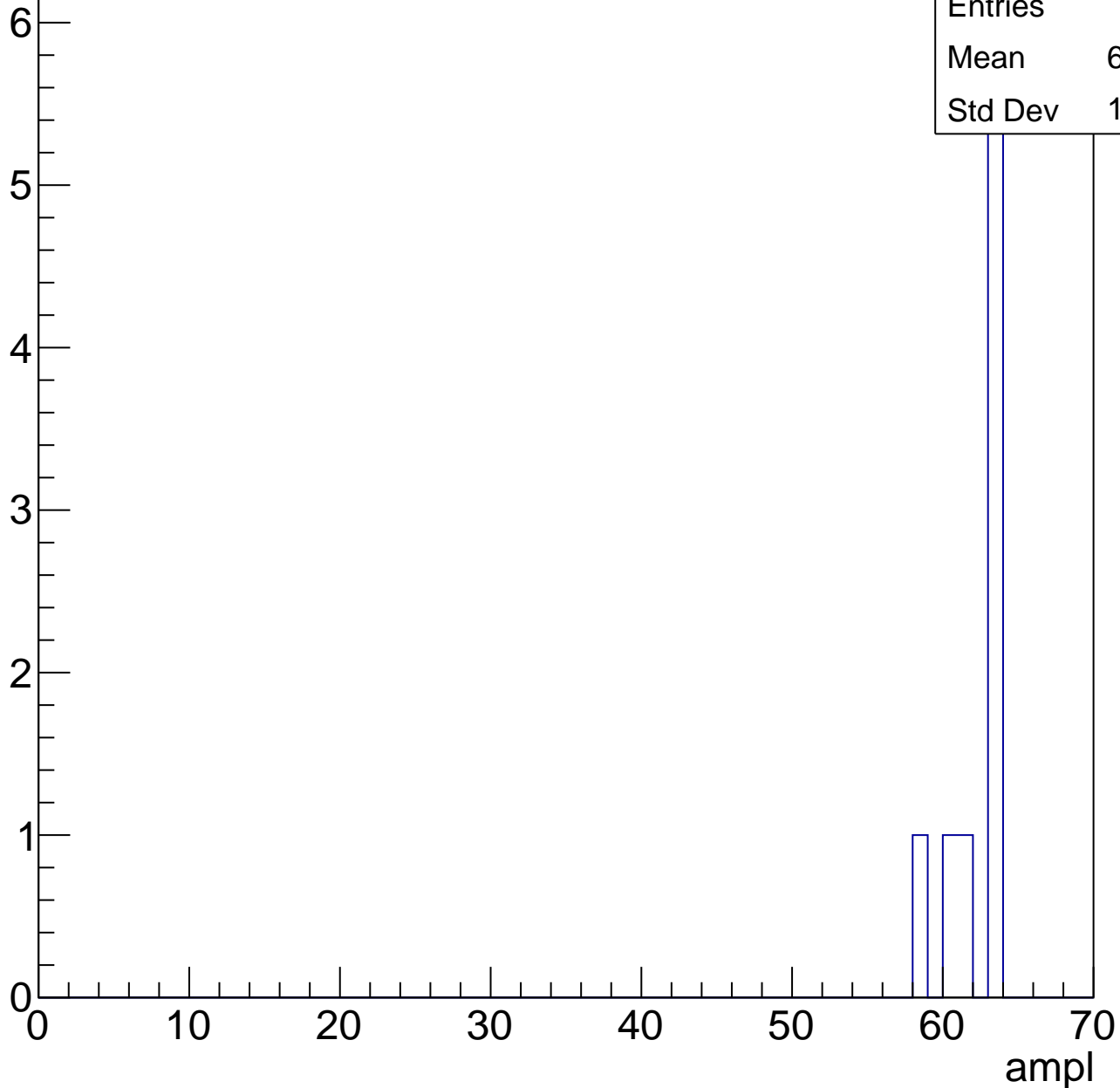
0 10 20 30 40 50 60 70



# B1L003S, U18-ch33, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

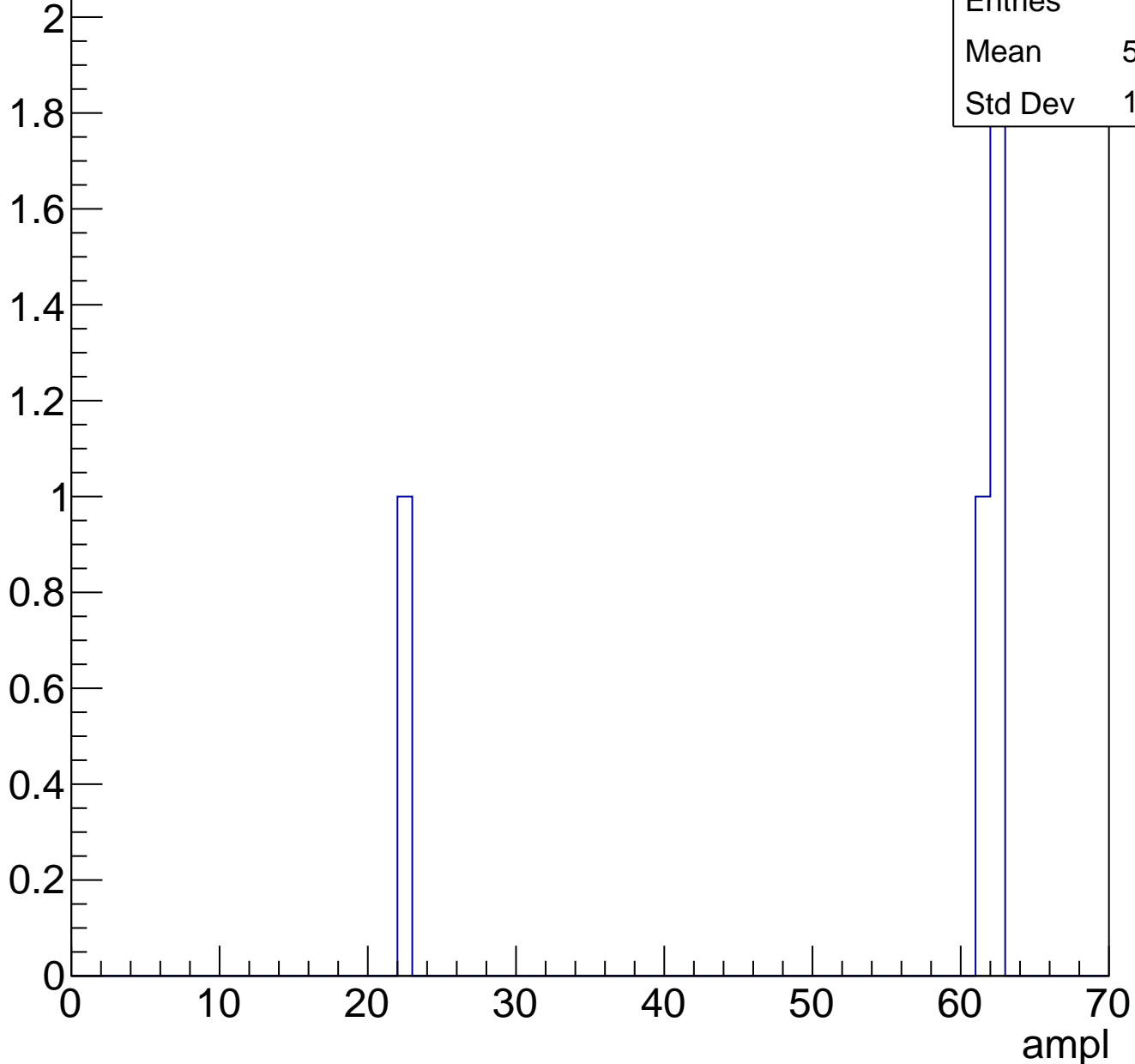




# B1L003S, U18-ch33, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	4
Mean	51.75
Std Dev	17.18

# B1L003S, U18-ch34, adc0

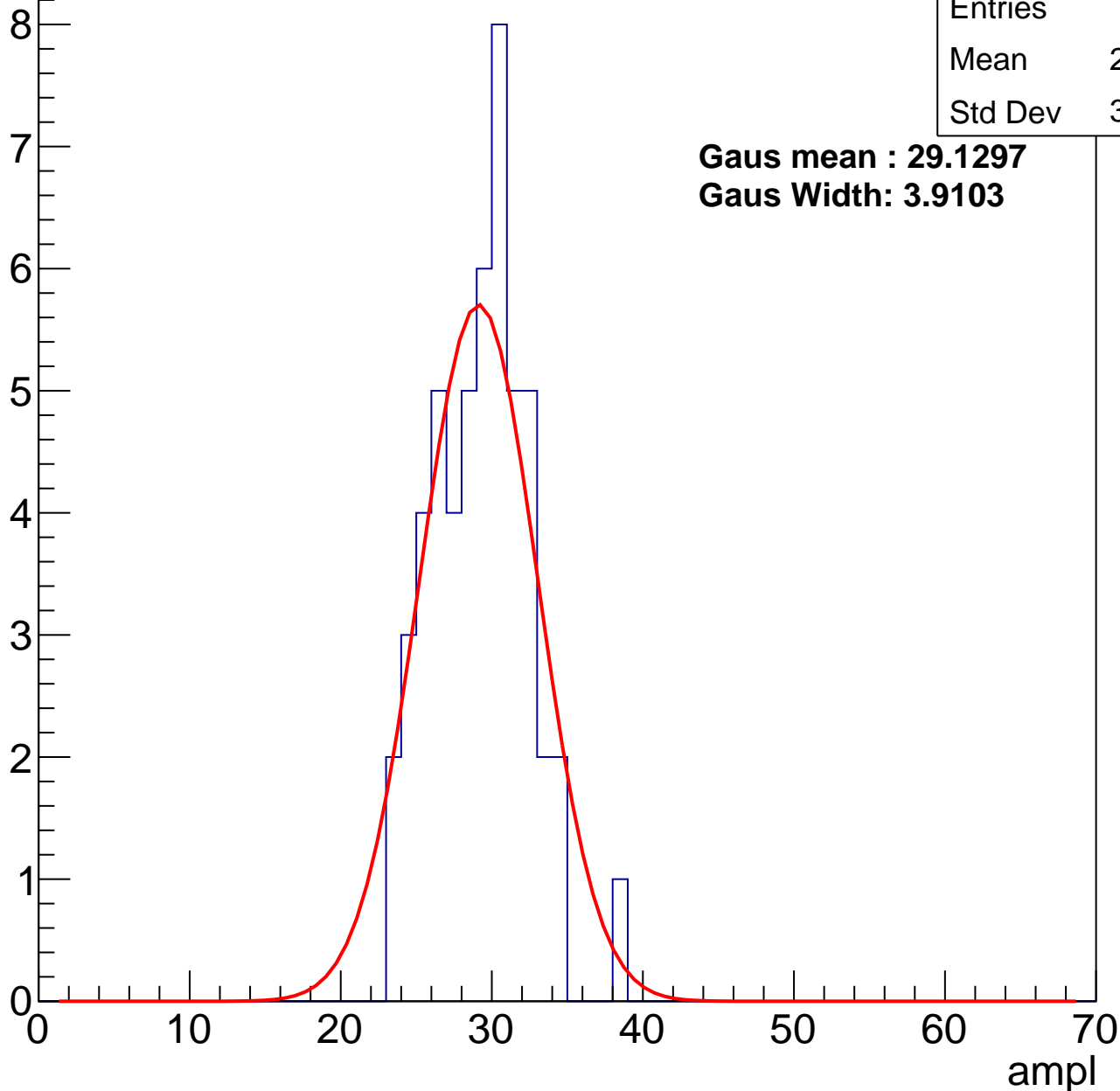
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	52
Mean	28.79
Std Dev	3.134

**Gaus mean : 29.1297**

**Gaus Width: 3.9103**



# B1L003S, U18-ch34, adc1

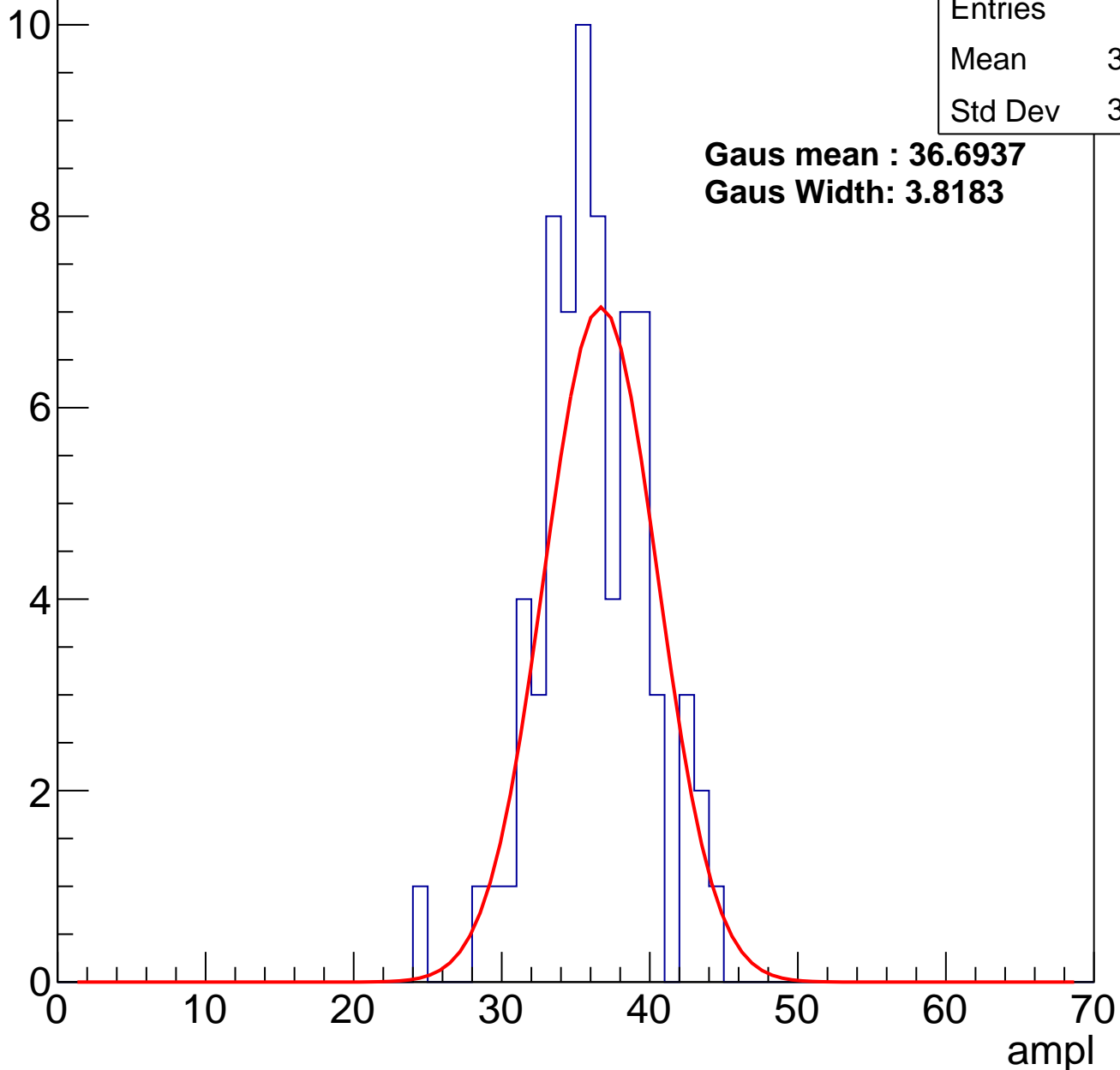
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	71
Mean	35.69
Std Dev	3.672

**Gaus mean : 36.6937**

**Gaus Width: 3.8183**

Entry



# B1L003S, U18-ch34, adc2

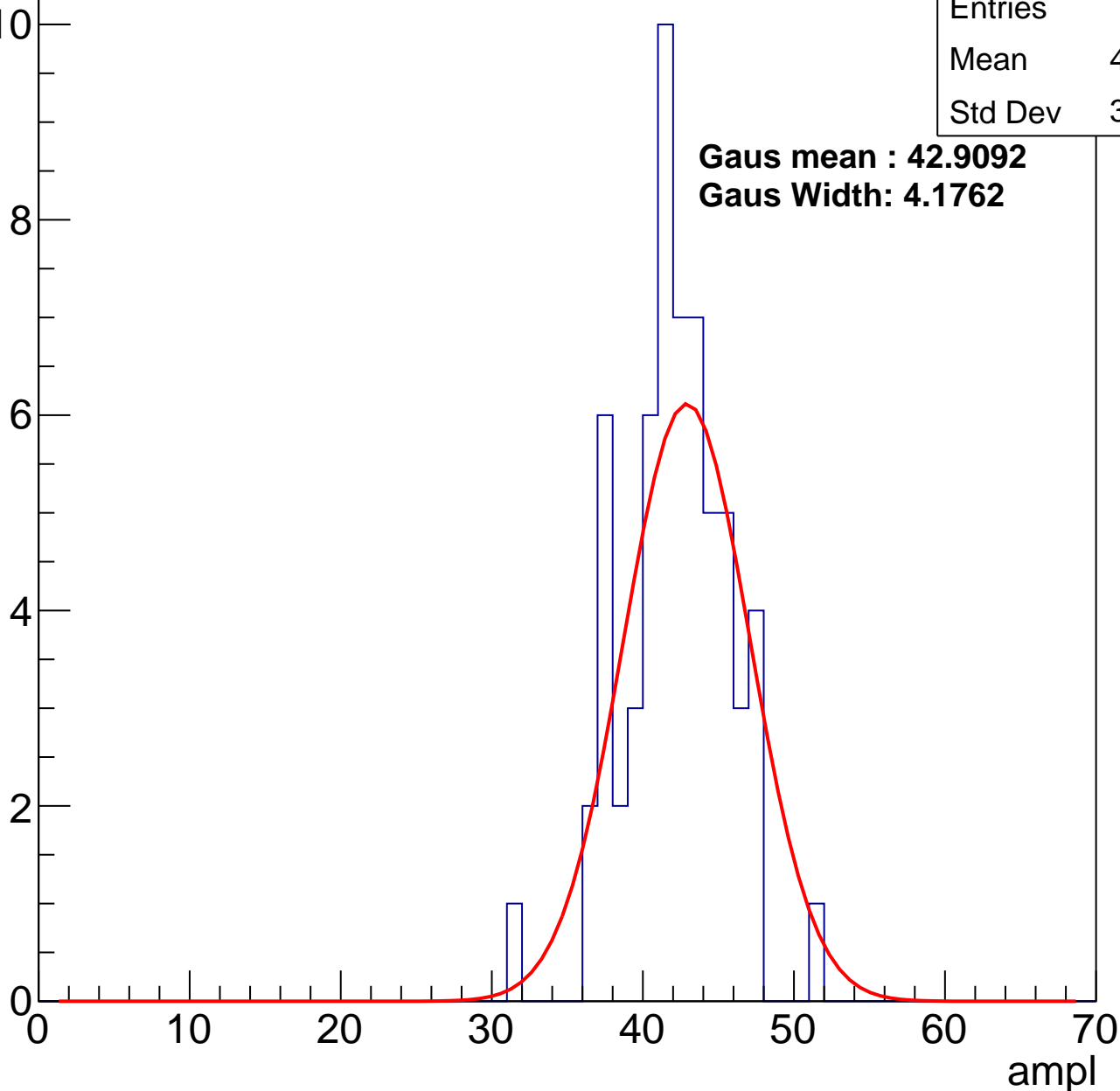
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	62
Mean	41.69
Std Dev	3.434

**Gaus mean : 42.9092**

**Gaus Width: 4.1762**



# B1L003S, U18-ch34, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

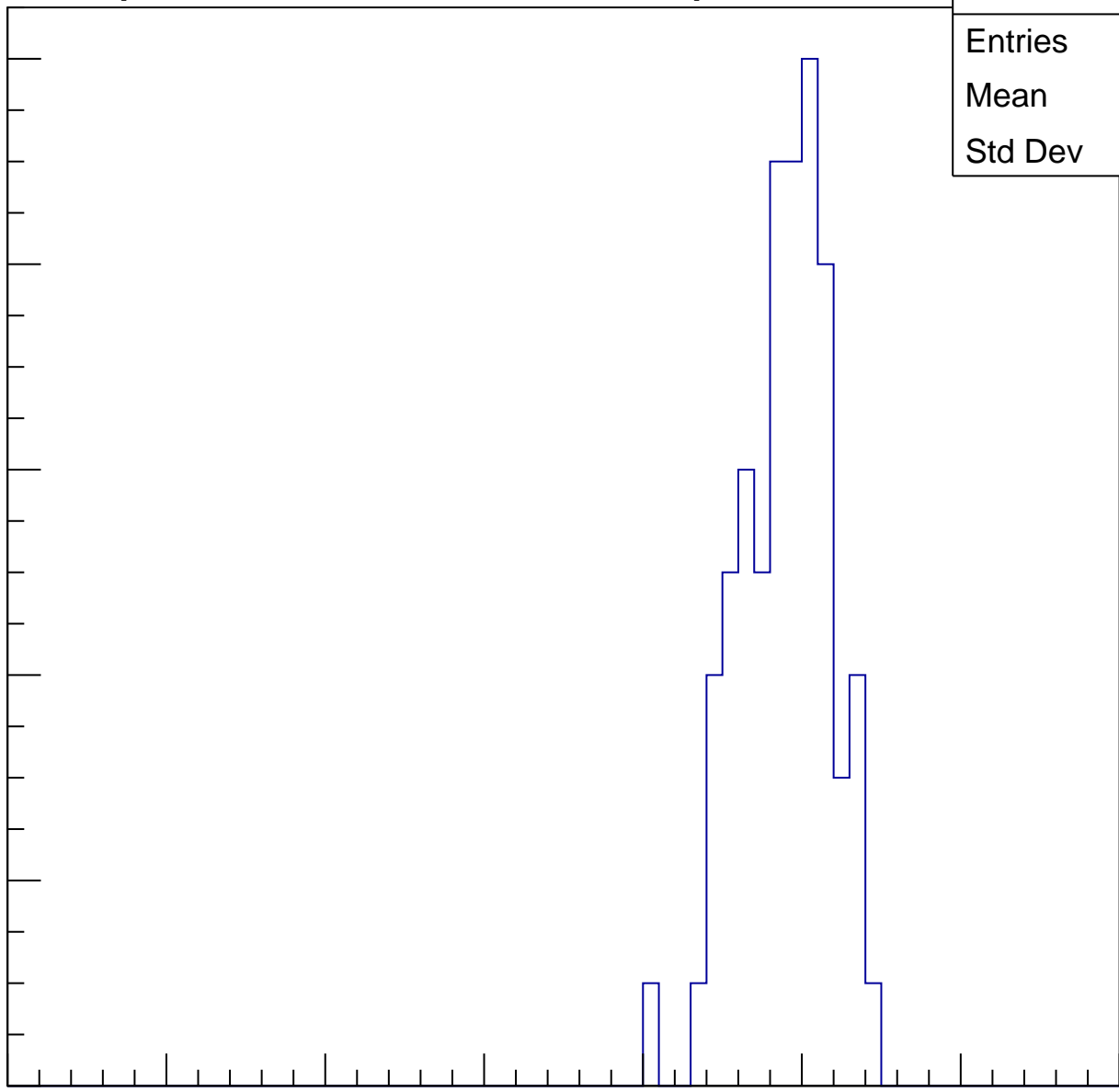
Entries	66
Mean	48.45
Std Dev	2.802

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

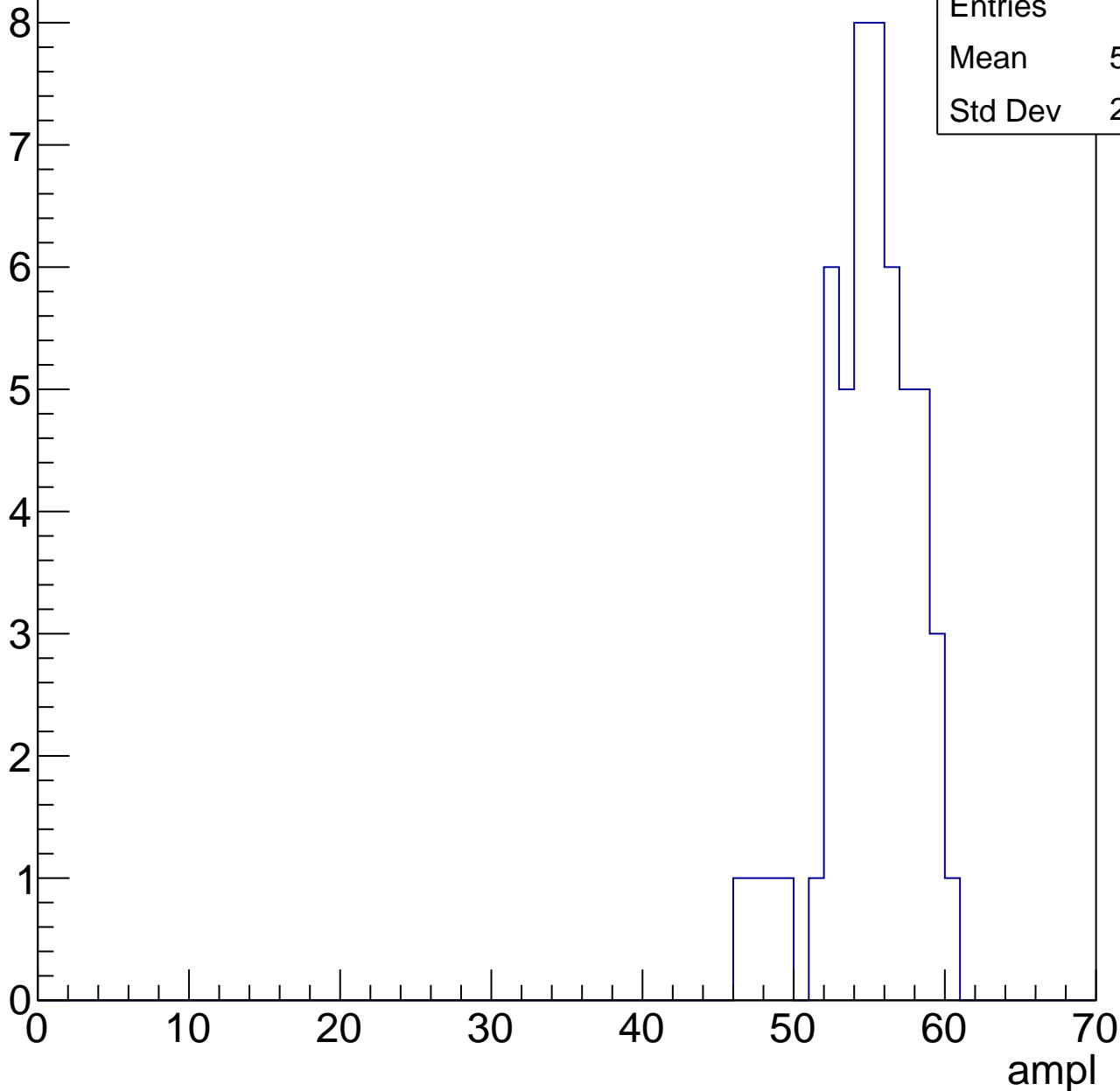


# B1L003S, U18-ch34, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	52
Mean	54.58
Std Dev	2.983

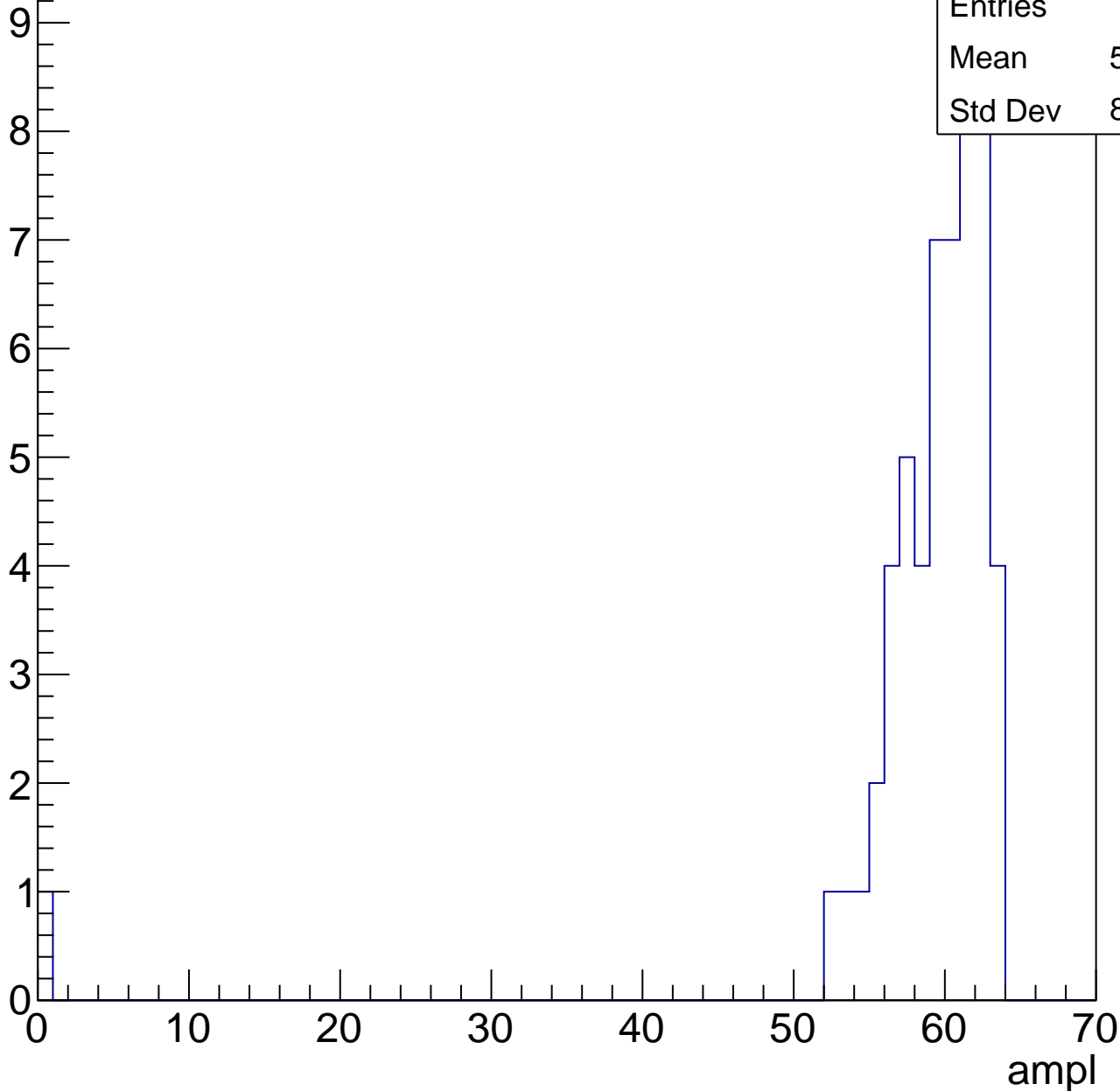


# B1L003S, U18-ch34, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	54
Mean	58.15
Std Dev	8.414

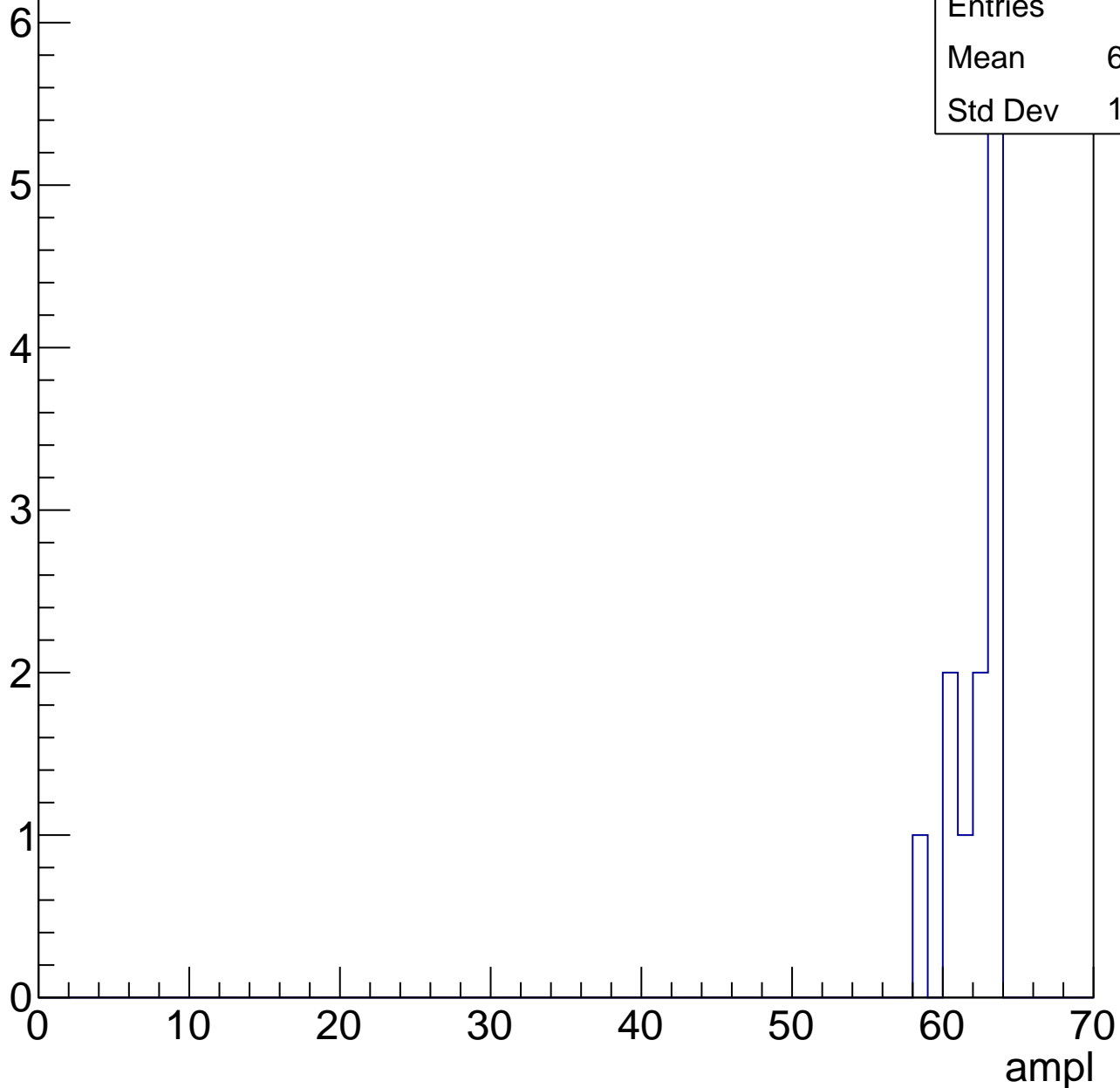


# B1L003S, U18-ch34, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	12
Mean	61.75
Std Dev	1.588





# B1L003S, U18-ch34, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch35, adc0

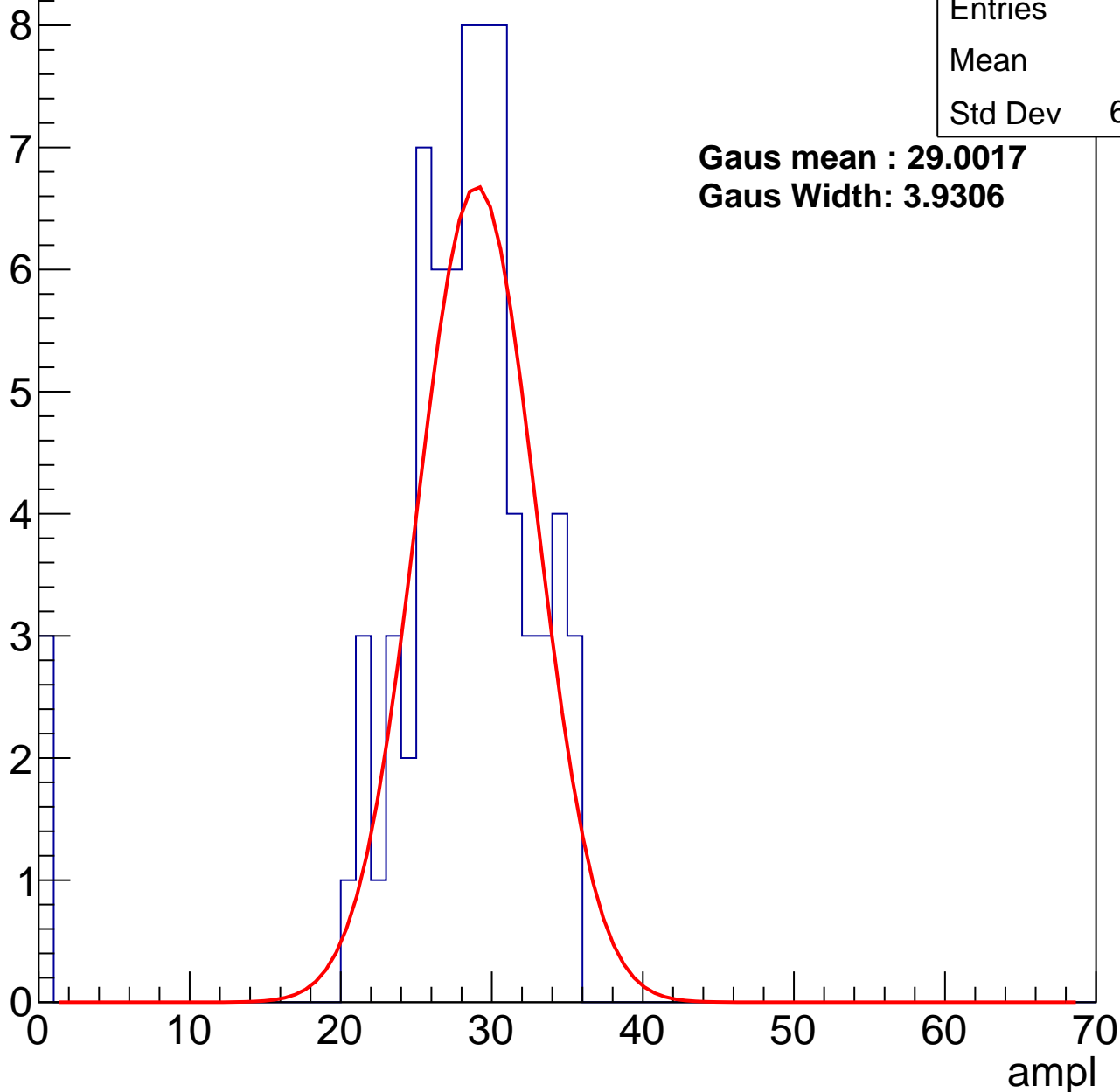
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	73
Mean	27
Std Dev	6.637

**Gaus mean : 29.0017**

**Gaus Width: 3.9306**



# B1L003S, U18-ch35, adc1

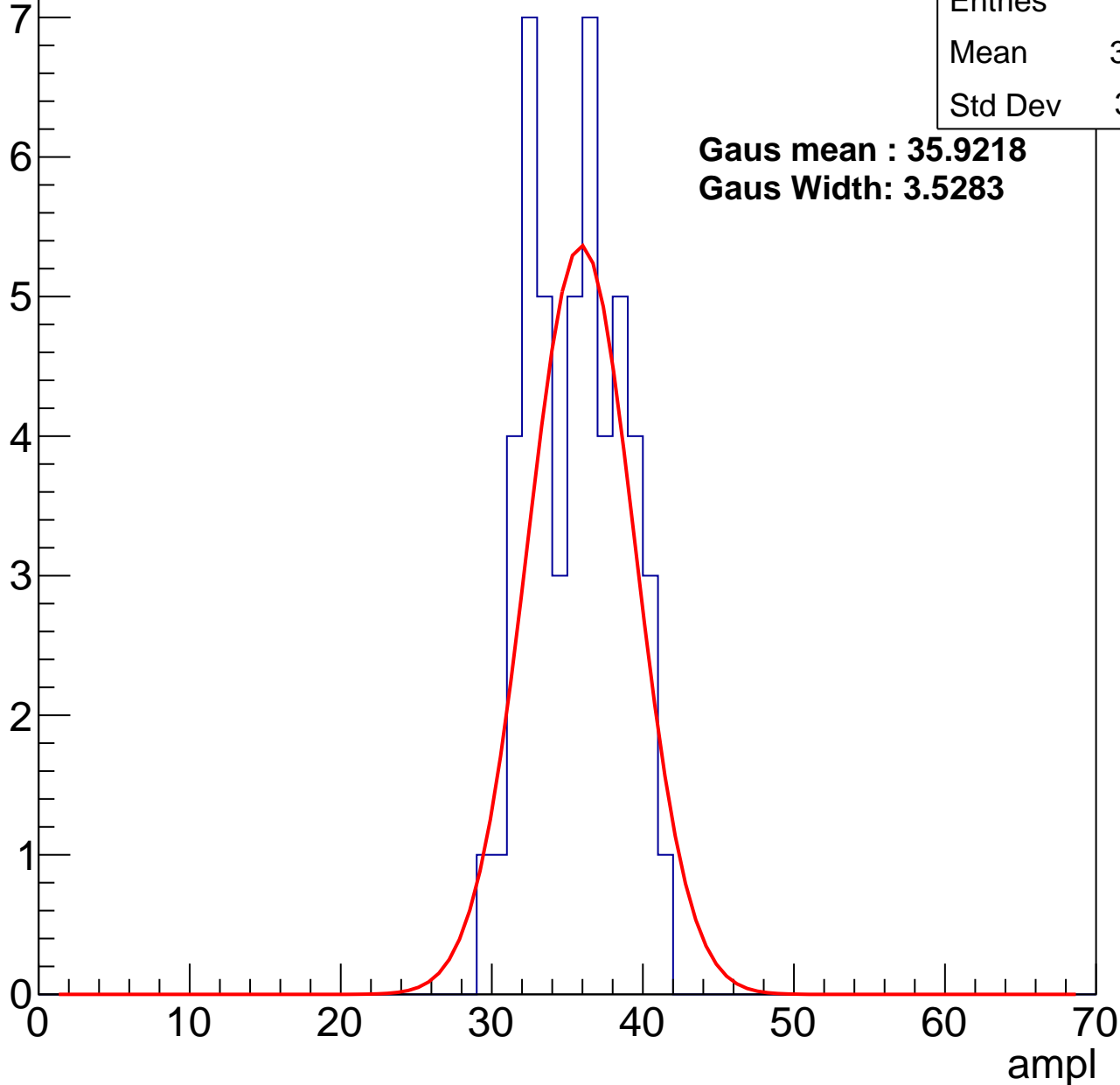
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	50
Mean	35.12
Std Dev	3.011

**Gaus mean : 35.9218**

**Gaus Width: 3.5283**



# B1L003S, U18-ch35, adc2

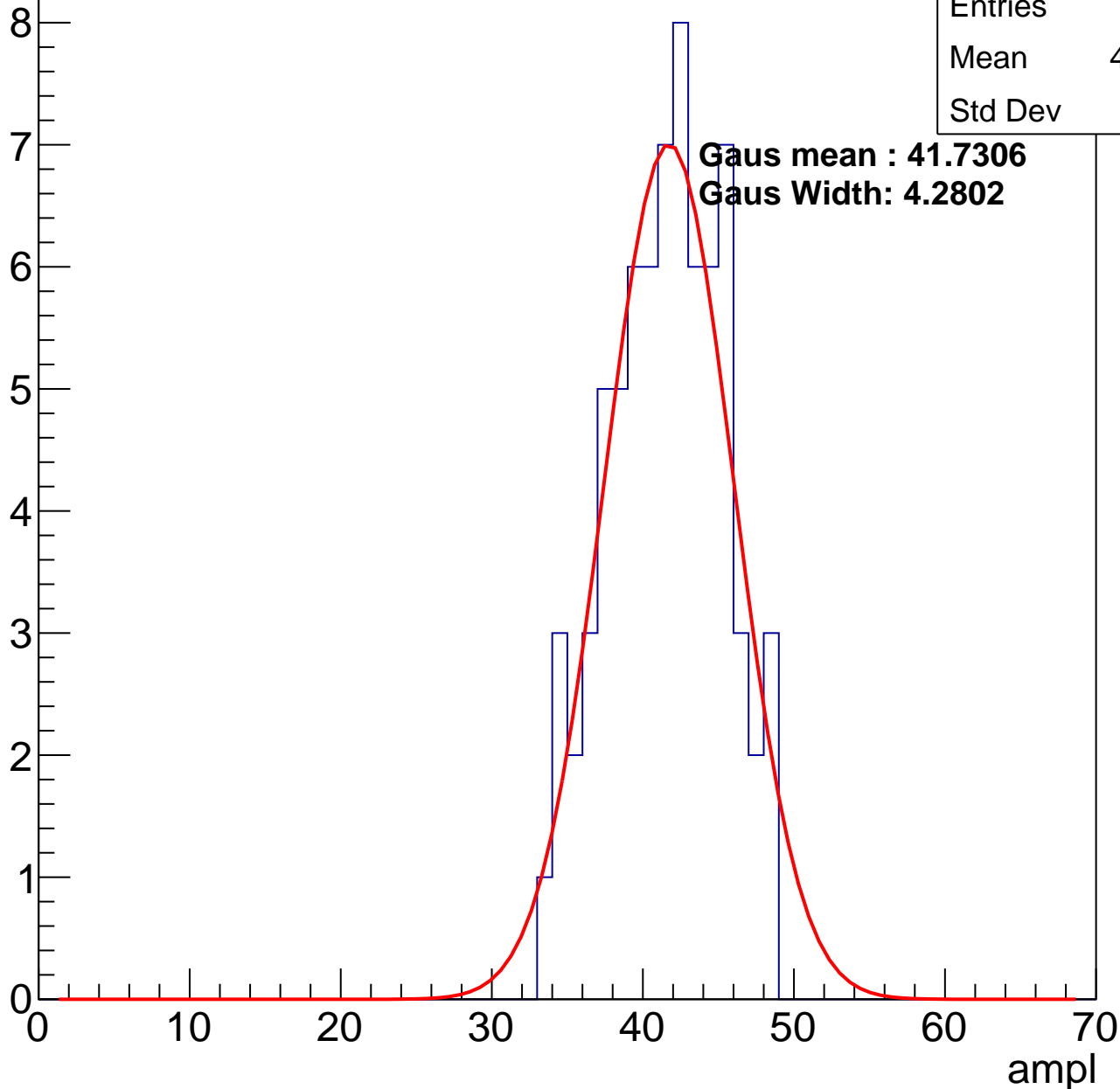
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	73
Mean	41.07
Std Dev	3.71

**Gaus mean : 41.7306**

**Gaus Width: 4.2802**

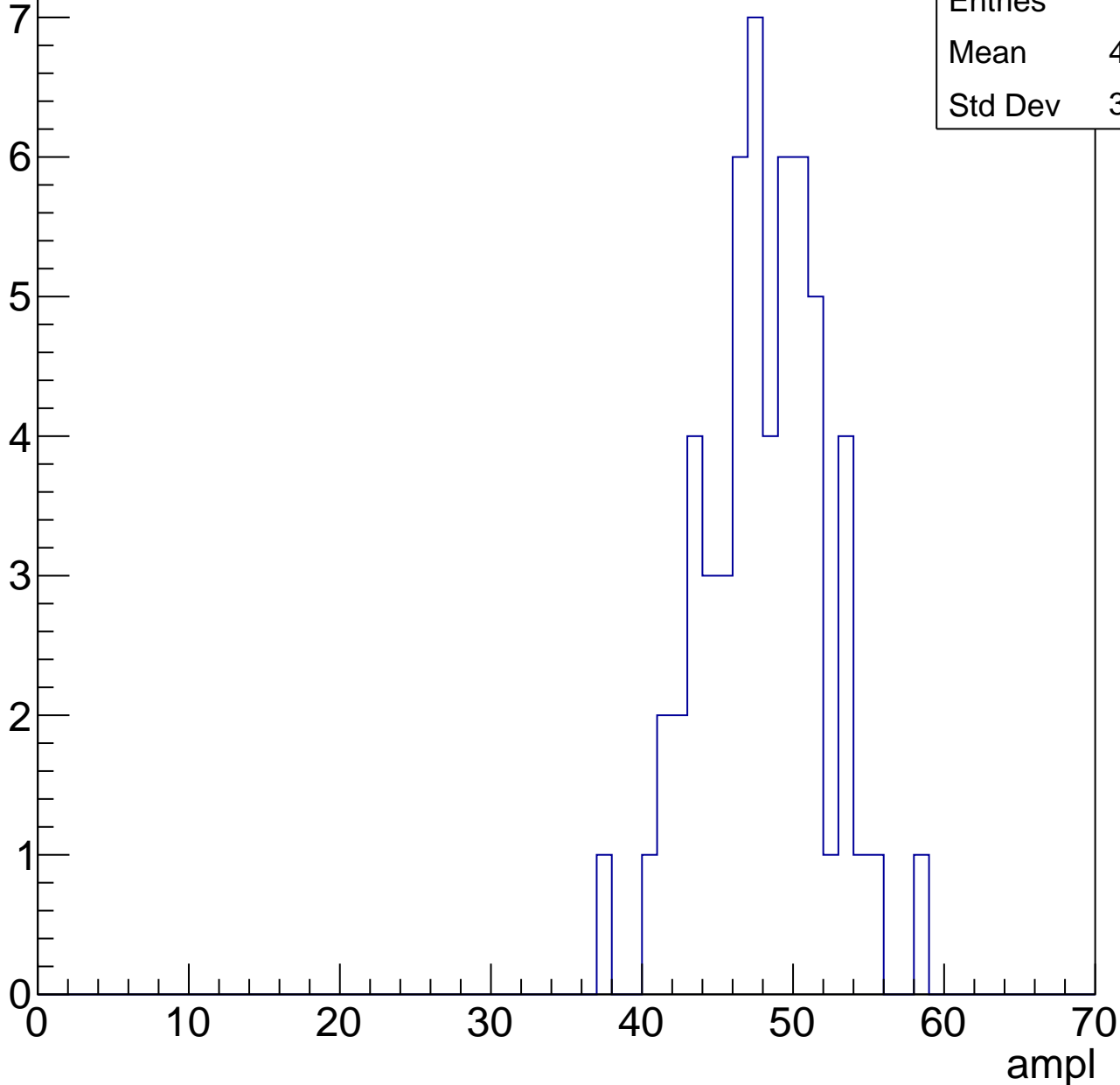


# B1L003S, U18-ch35, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	58
Mean	47.57
Std Dev	3.996

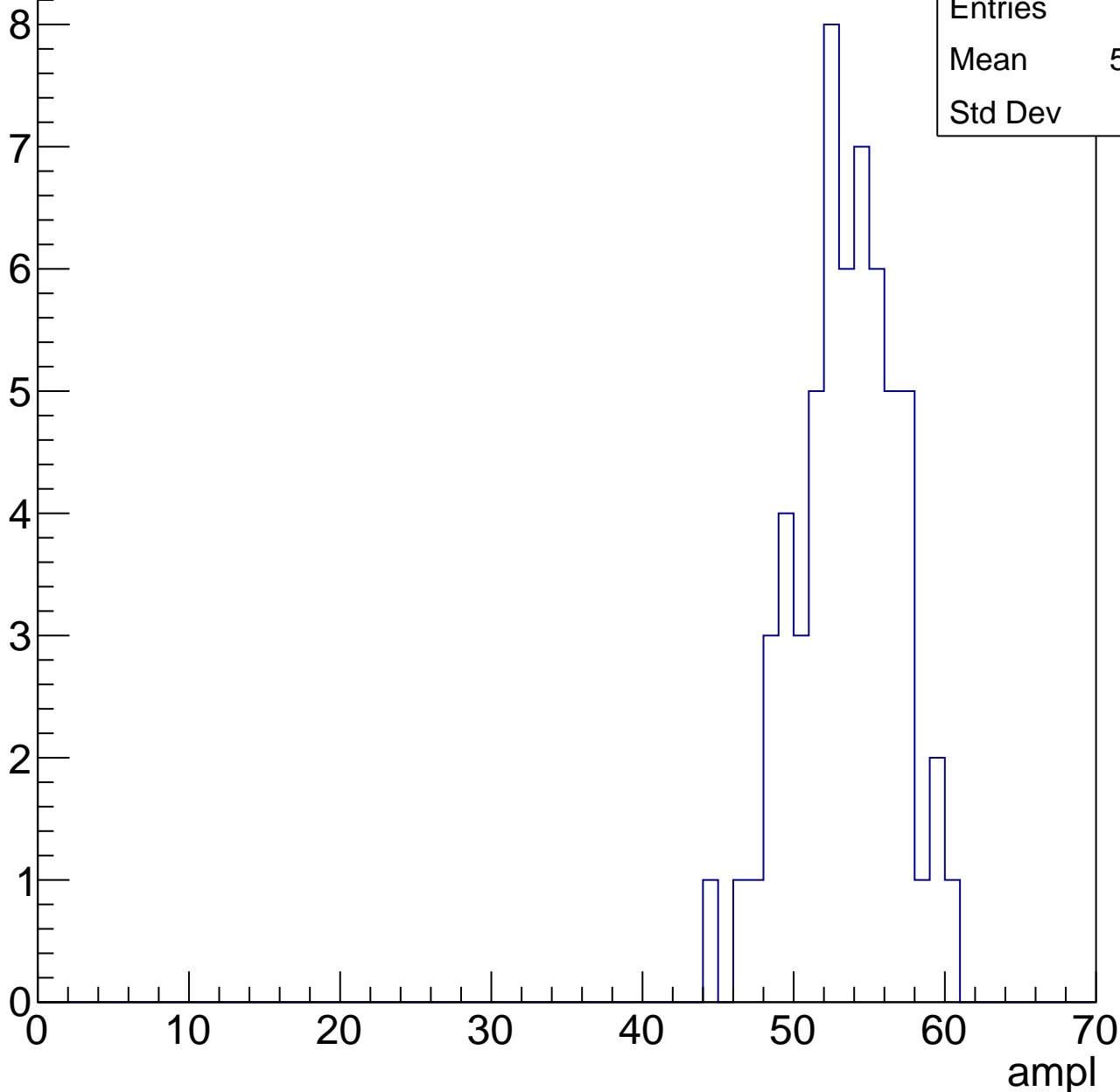


# B1L003S, U18-ch35, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	59
Mean	52.97
Std Dev	3.35

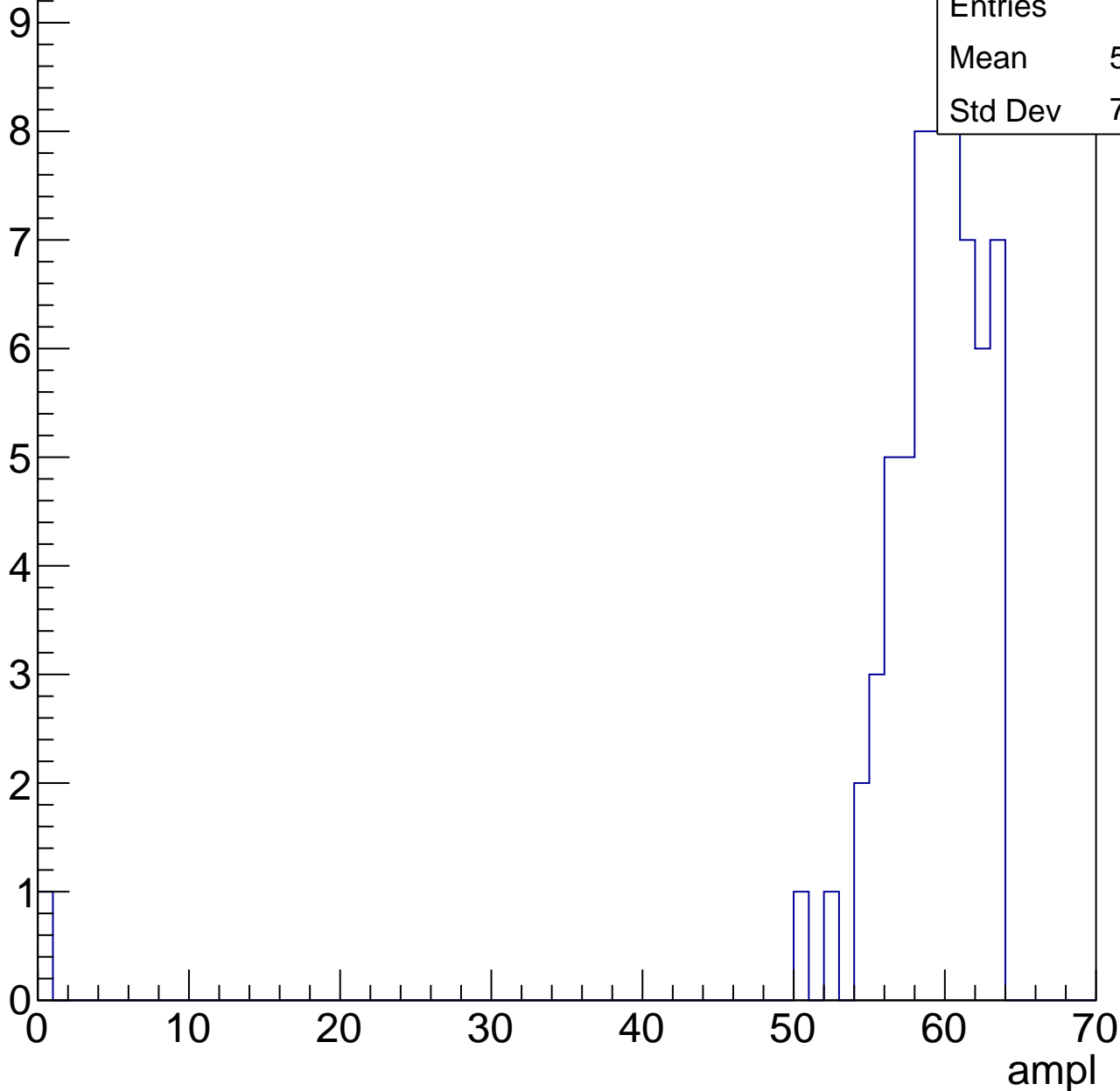


# B1L003S, U18-ch35, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	63
Mean	58.03
Std Dev	7.894



# B1L003S, U18-ch35, adc6

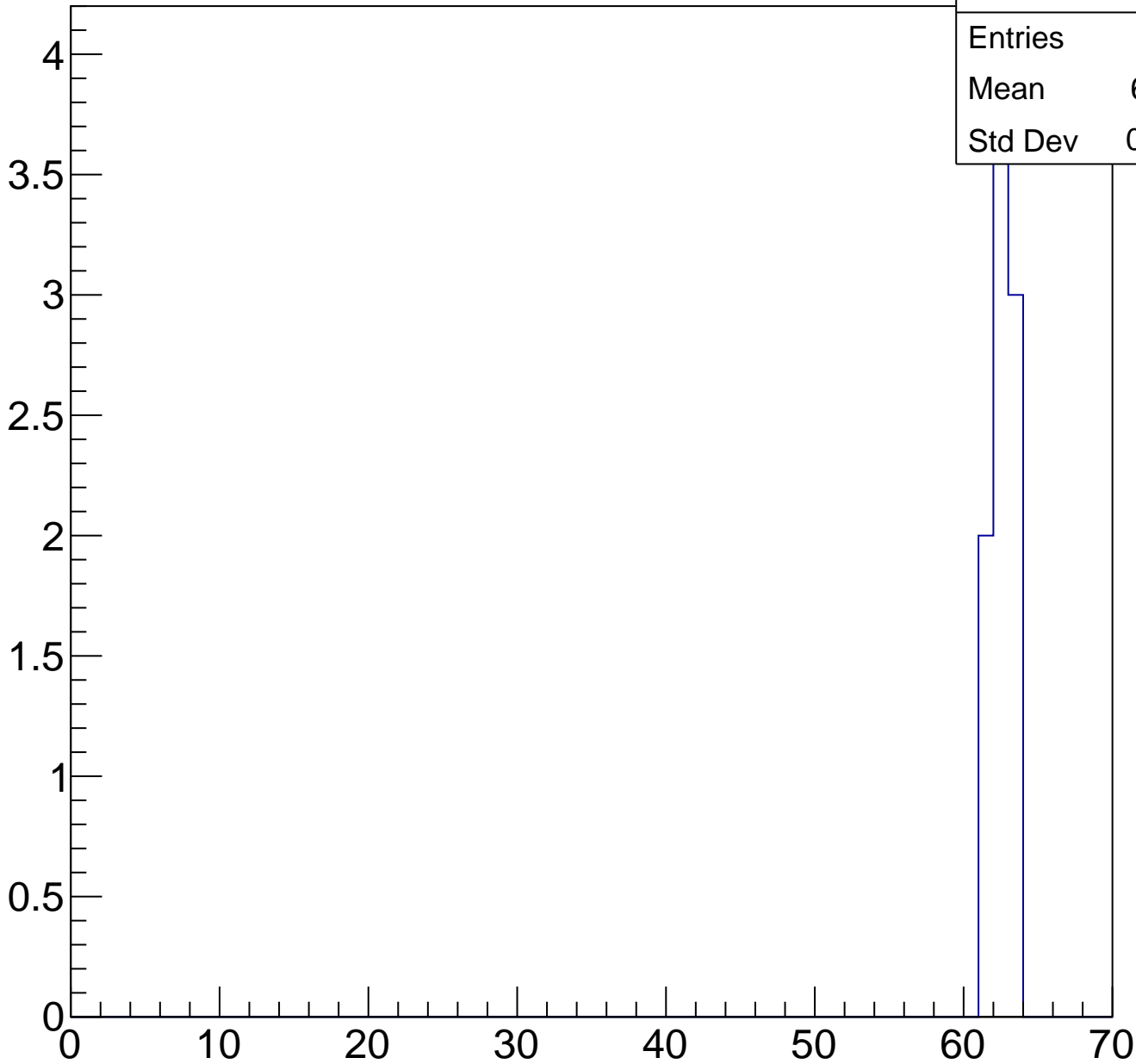
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

4  
3.5  
3  
2.5  
2  
1.5  
1  
0.5  
0

Entries	9
Mean	62.11
Std Dev	0.737

ampl





# B1L003S, U18-ch35, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U18-ch36, adc0

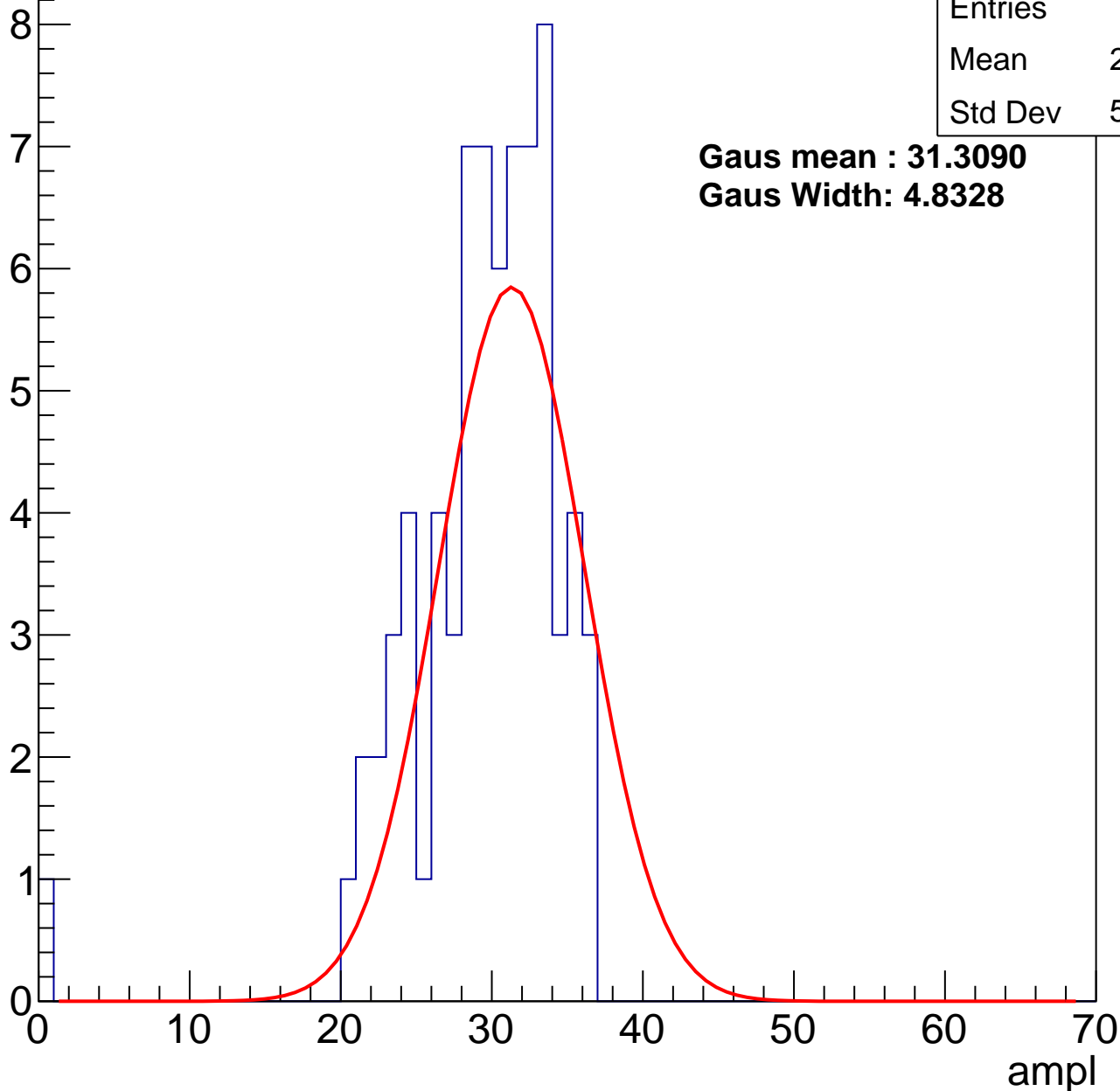
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	73
Mean	28.97
Std Dev	5.258

**Gaus mean : 31.3090**

**Gaus Width: 4.8328**



# B1L003S, U18-ch36, adc1

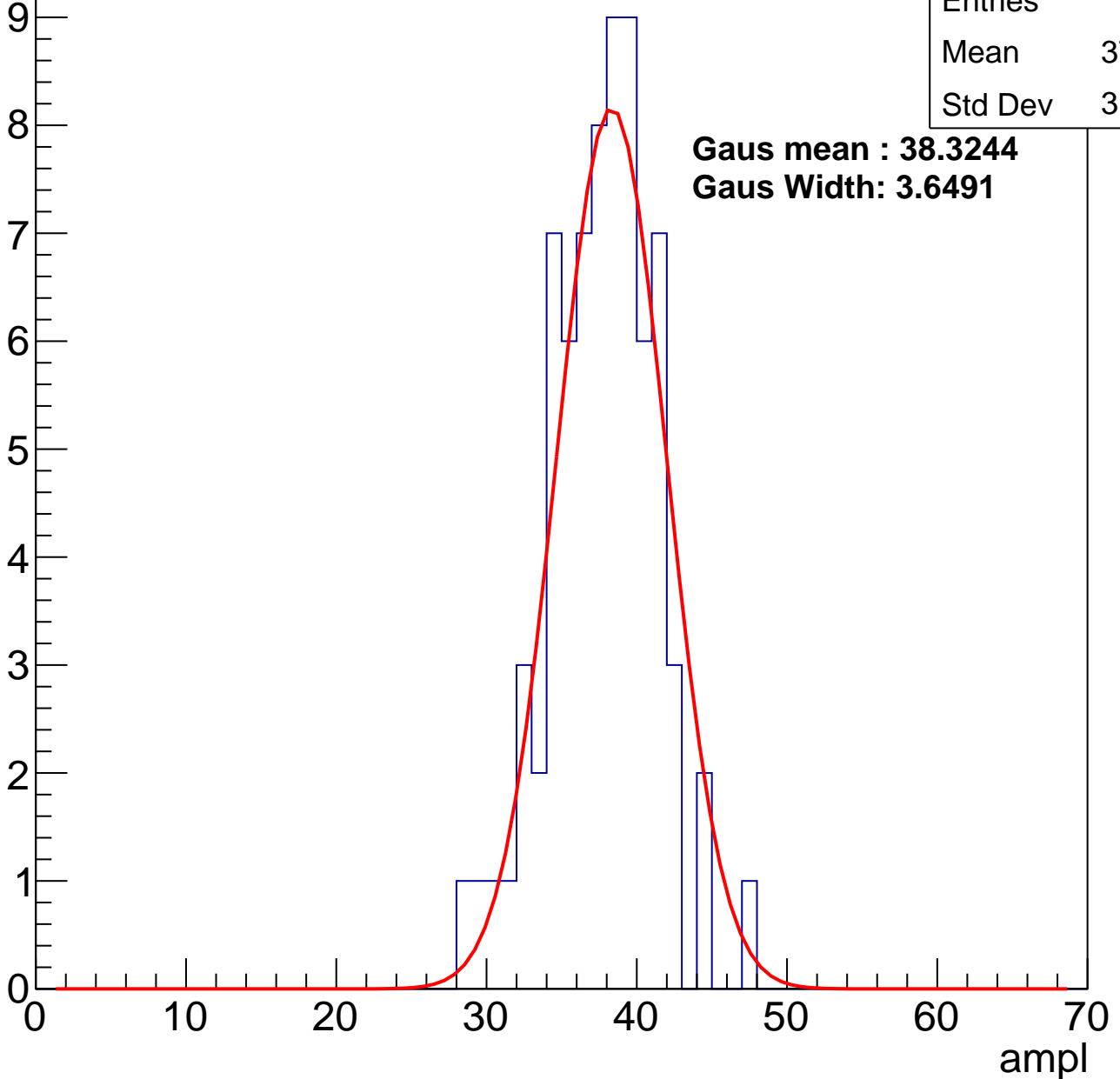
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	74
Mean	37.26
Std Dev	3.507

**Gaus mean : 38.3244**

**Gaus Width: 3.6491**



# B1L003S, U18-ch36, adc2

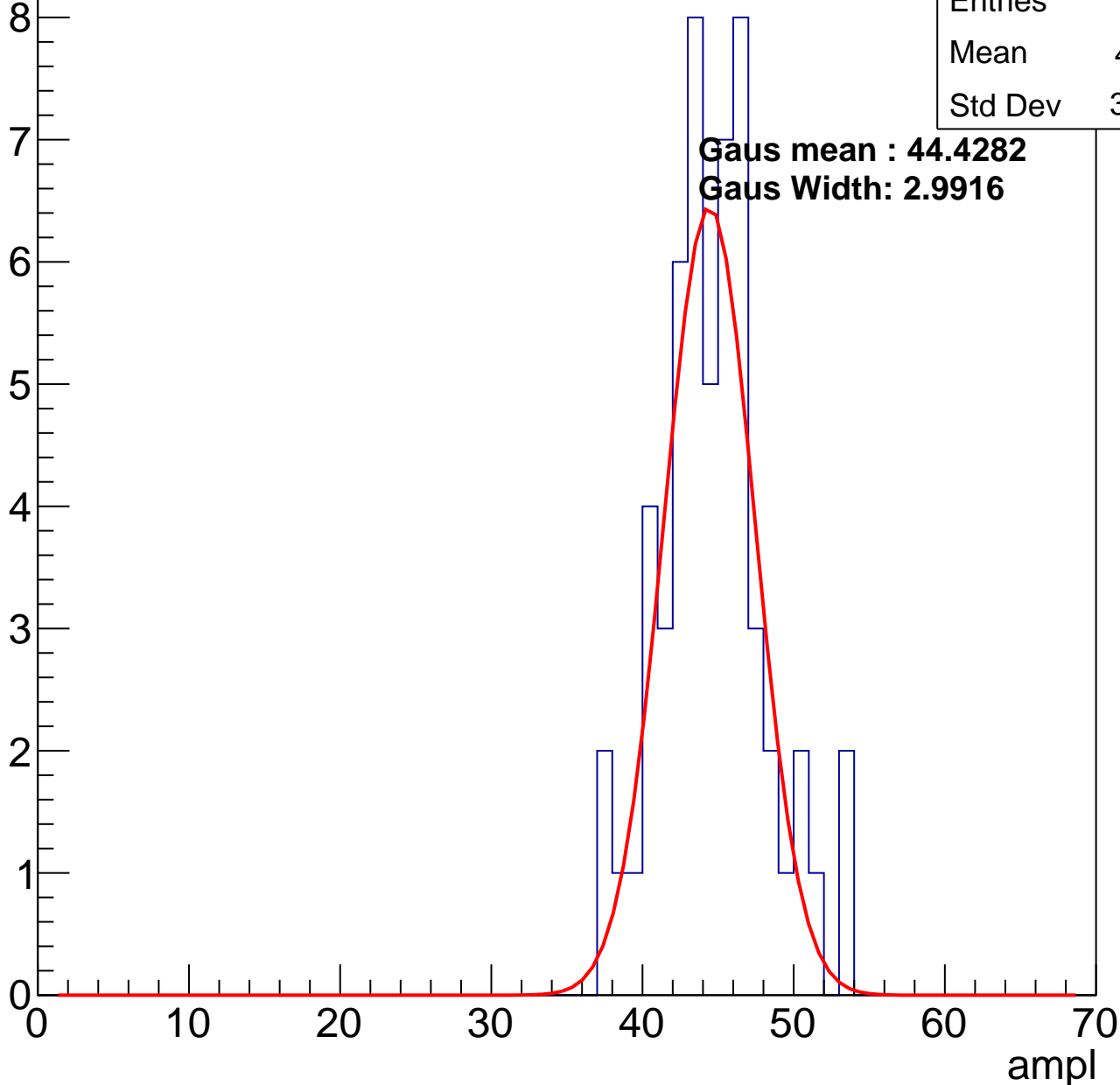
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	56
Mean	44.21
Std Dev	3.499

**Gaus mean : 44.4282**

**Gaus Width: 2.9916**

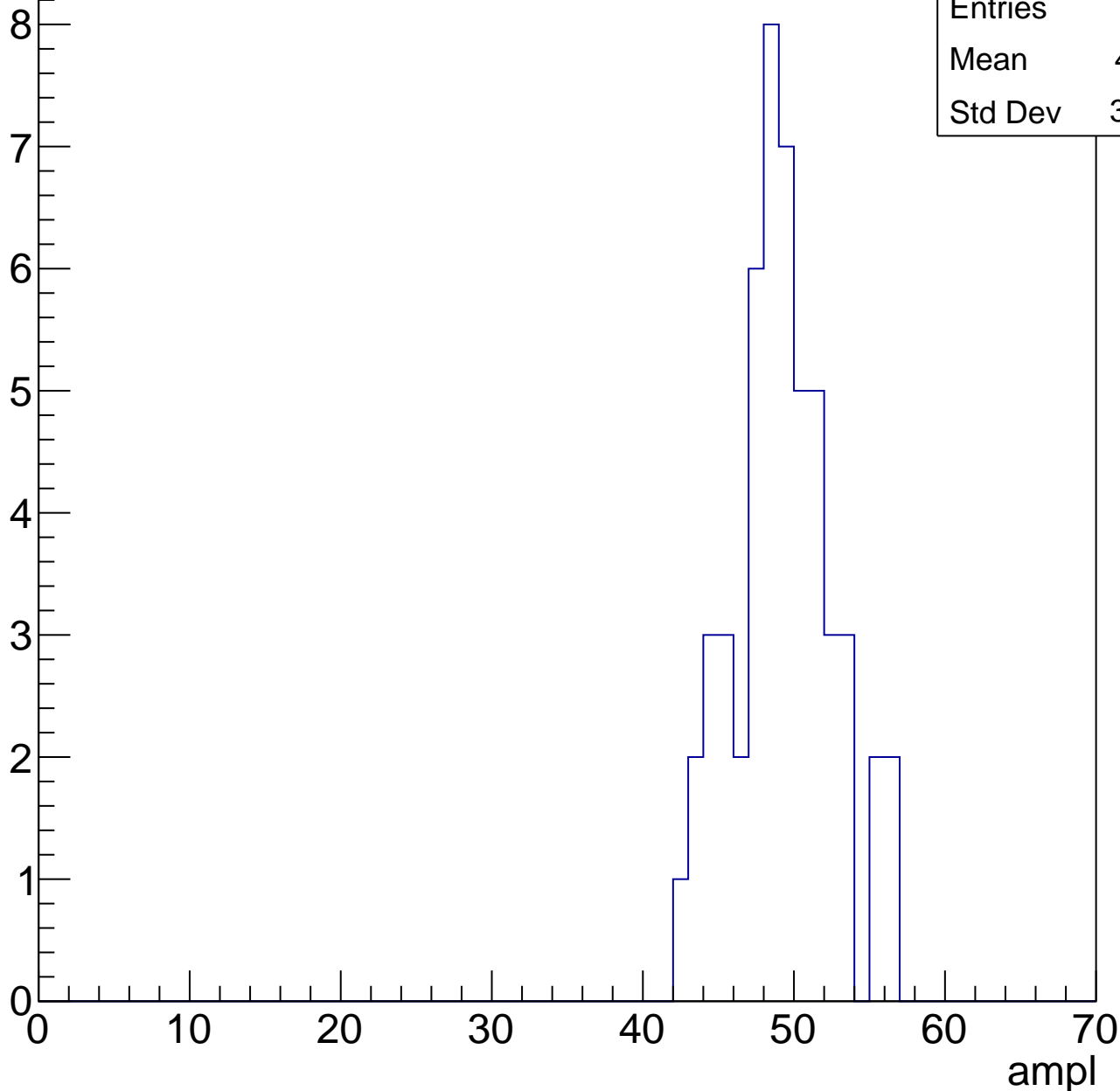


# B1L003S, U18-ch36, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	52
Mean	48.81
Std Dev	3.288



# B1L003S, U18-ch36, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	64
Mean	53.92
Std Dev	7.394

Entry

10

8

6

4

2

0

0

10

20

30

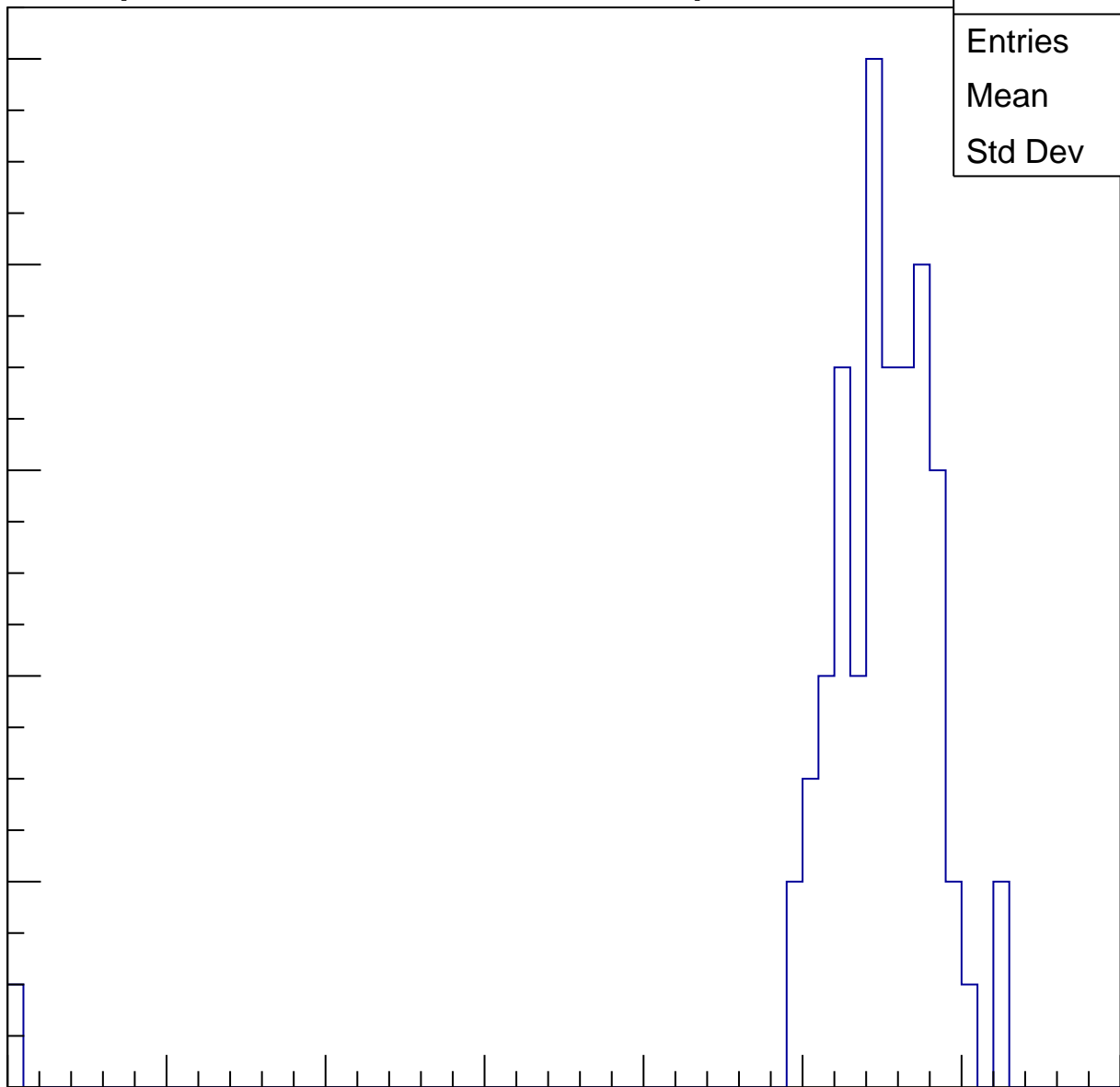
40

50

60

70

ampl



# B1L003S, U18-ch36, adc5

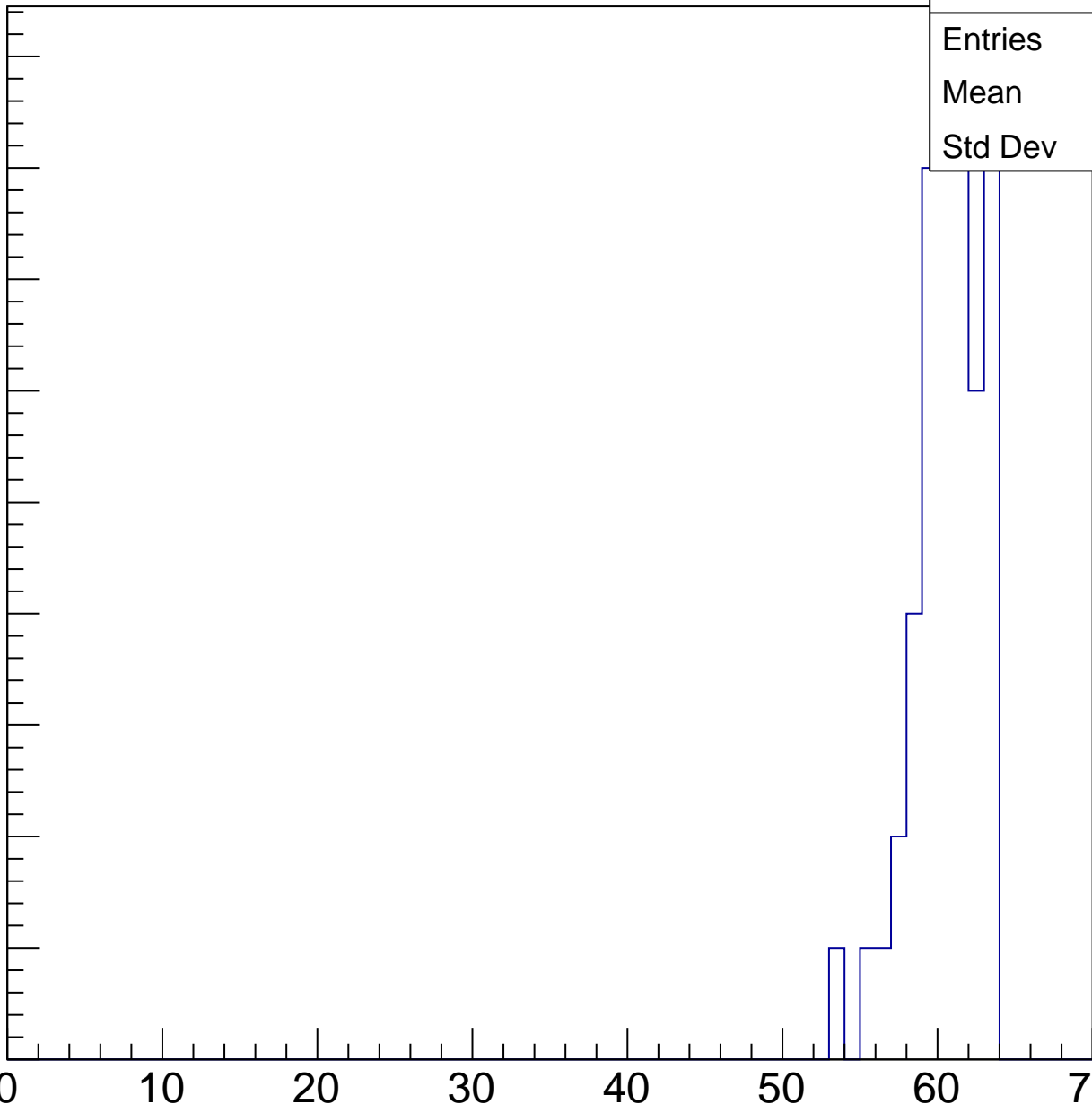
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	49
Mean	60.2
Std Dev	2.231

ampl



# B1L003S, U18-ch36, adc6

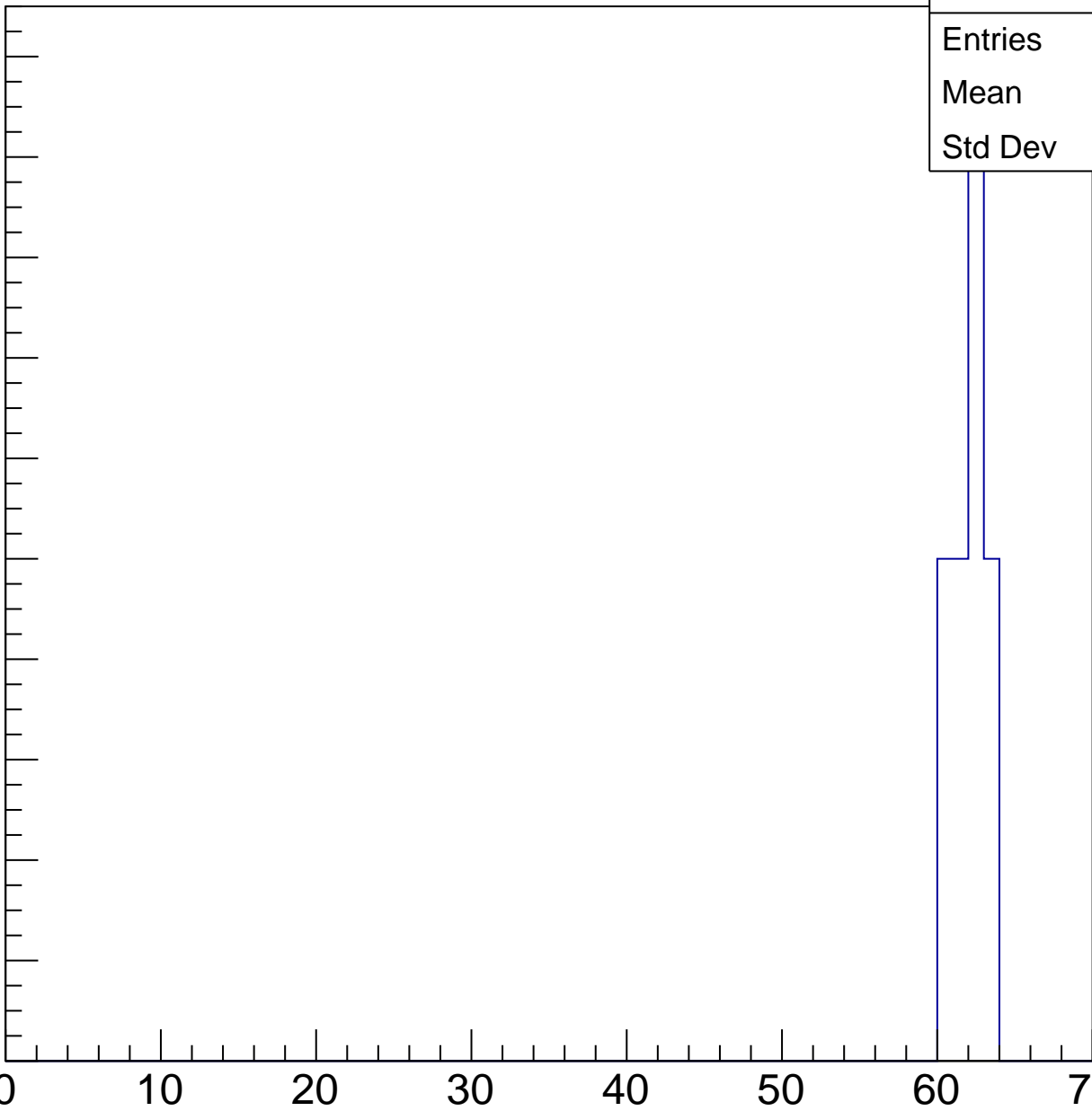
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	5
Mean	61.6
Std Dev	1.02

ampl





# B1L003S, U18-ch36, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U18-ch37, adc0

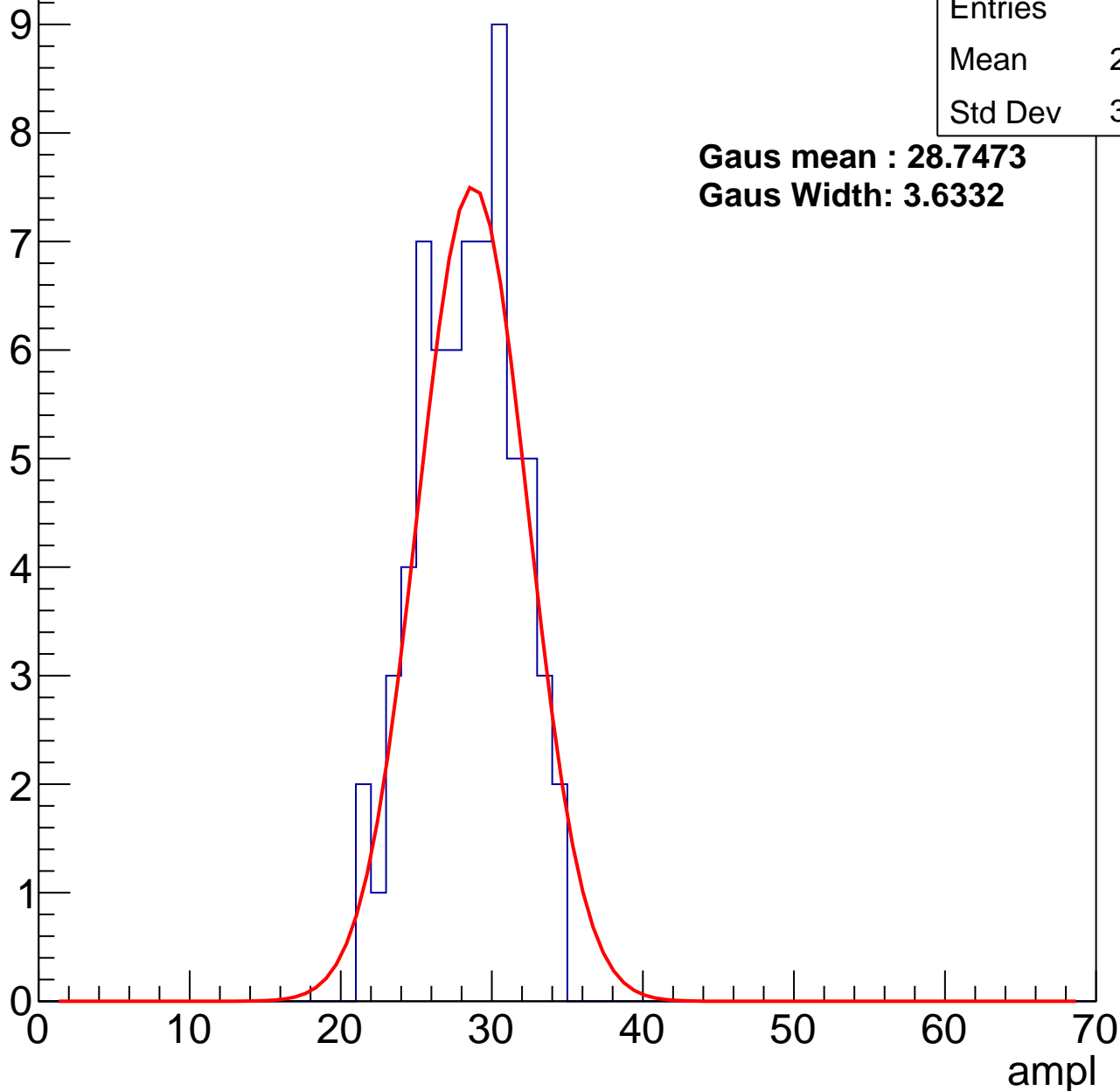
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	67
Mean	27.96
Std Dev	3.188

**Gaus mean : 28.7473**

**Gaus Width: 3.6332**



# B1L003S, U18-ch37, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	78
Mean	35.45
Std Dev	3.373

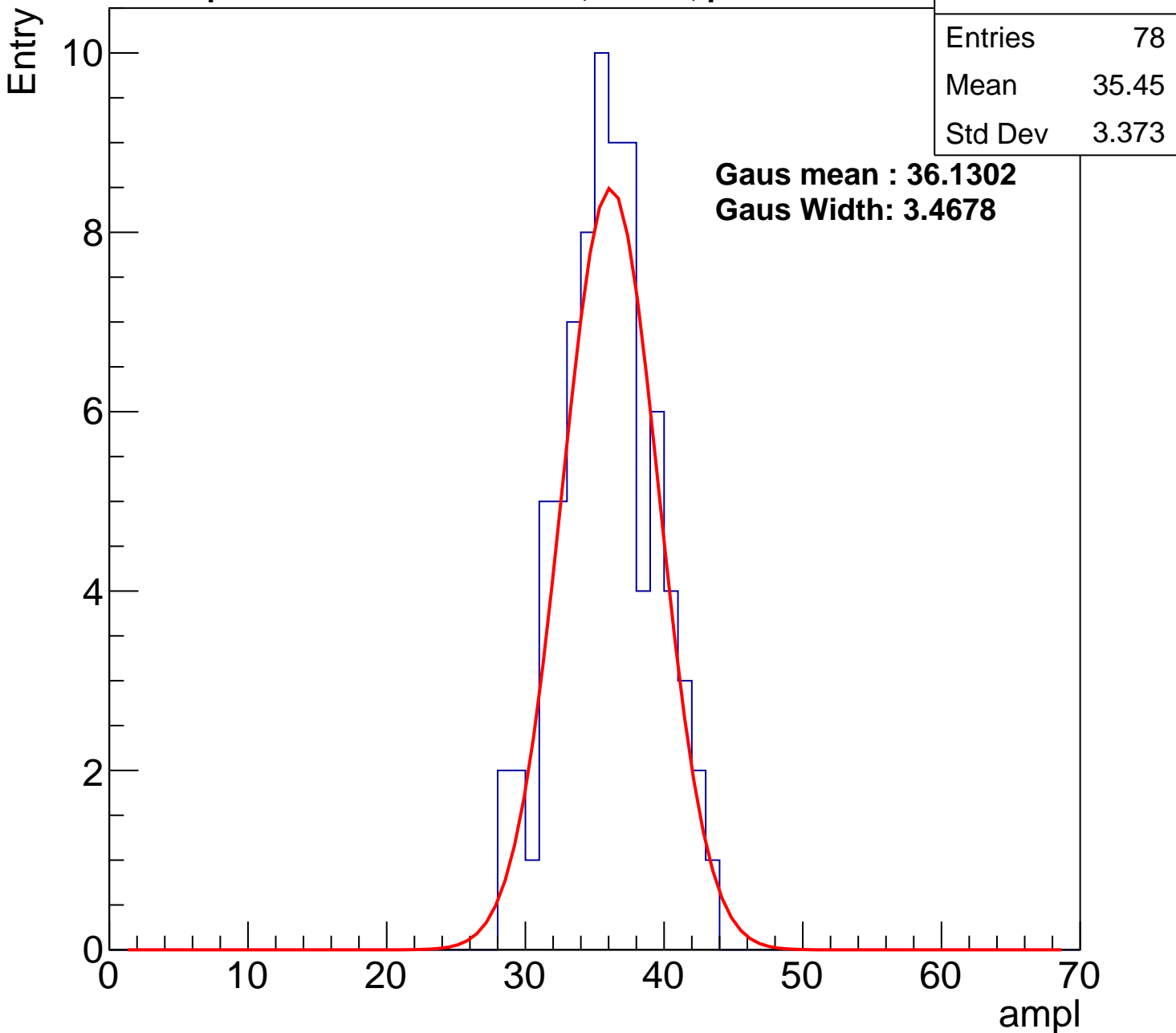
**Gaus mean : 36.1302**  
**Gaus Width: 3.4678**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L003S, U18-ch37, adc2

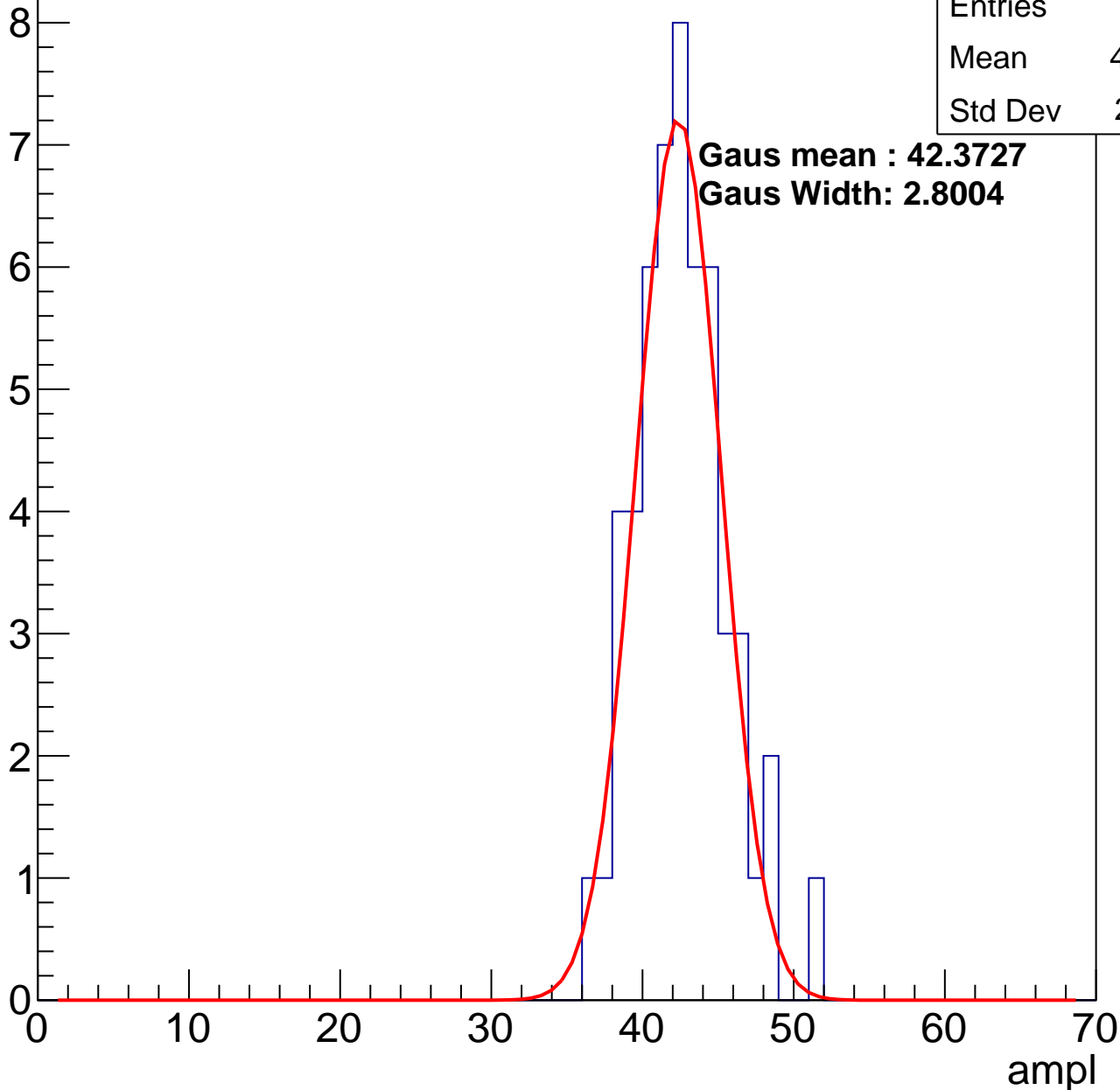
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	53
Mean	42.13
Std Dev	2.991

**Gaus mean : 42.3727**

**Gaus Width: 2.8004**

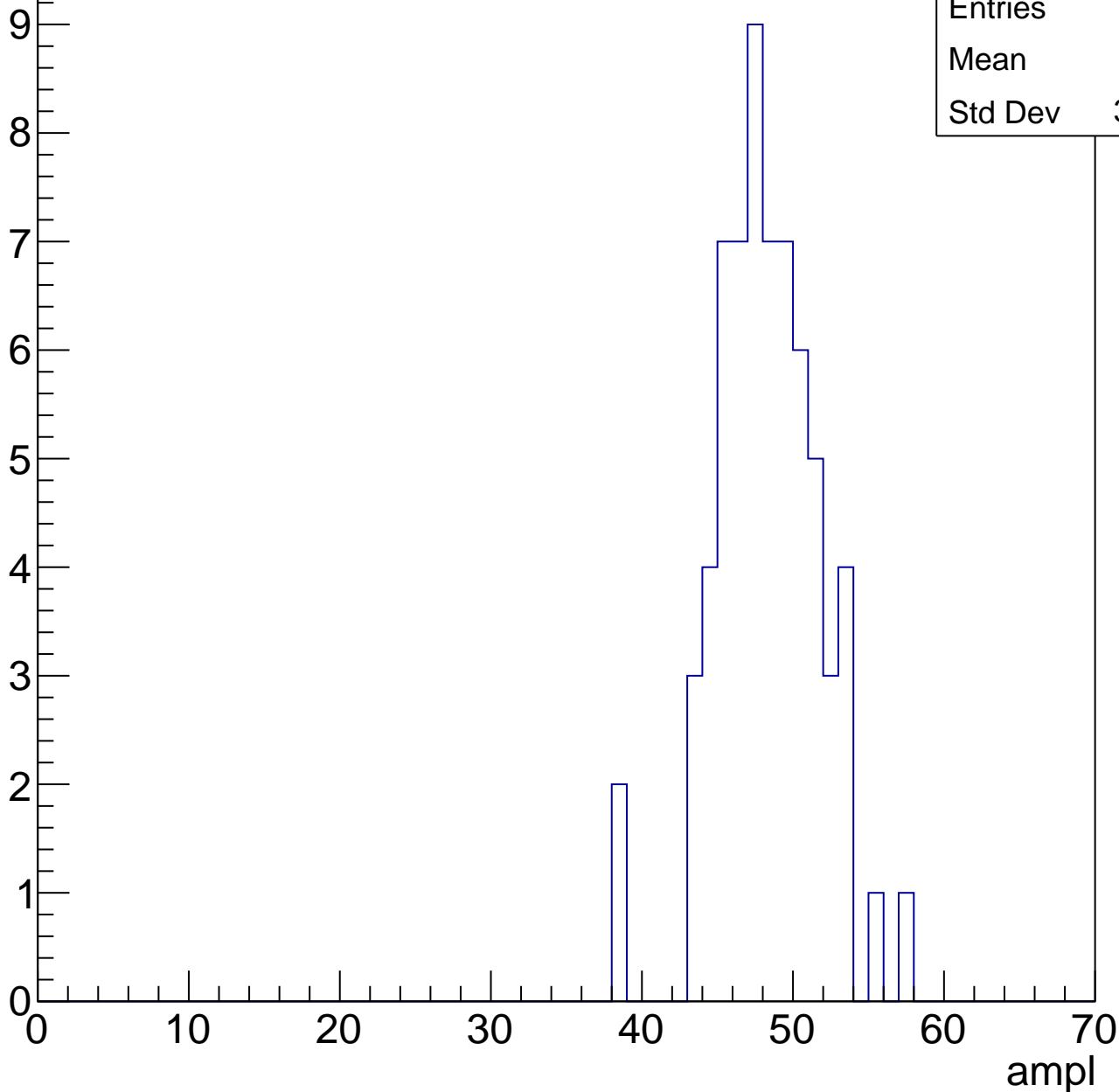


# B1L003S, U18-ch37, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	66
Mean	47.8
Std Dev	3.461



# B1L003S, U18-ch37, adc4

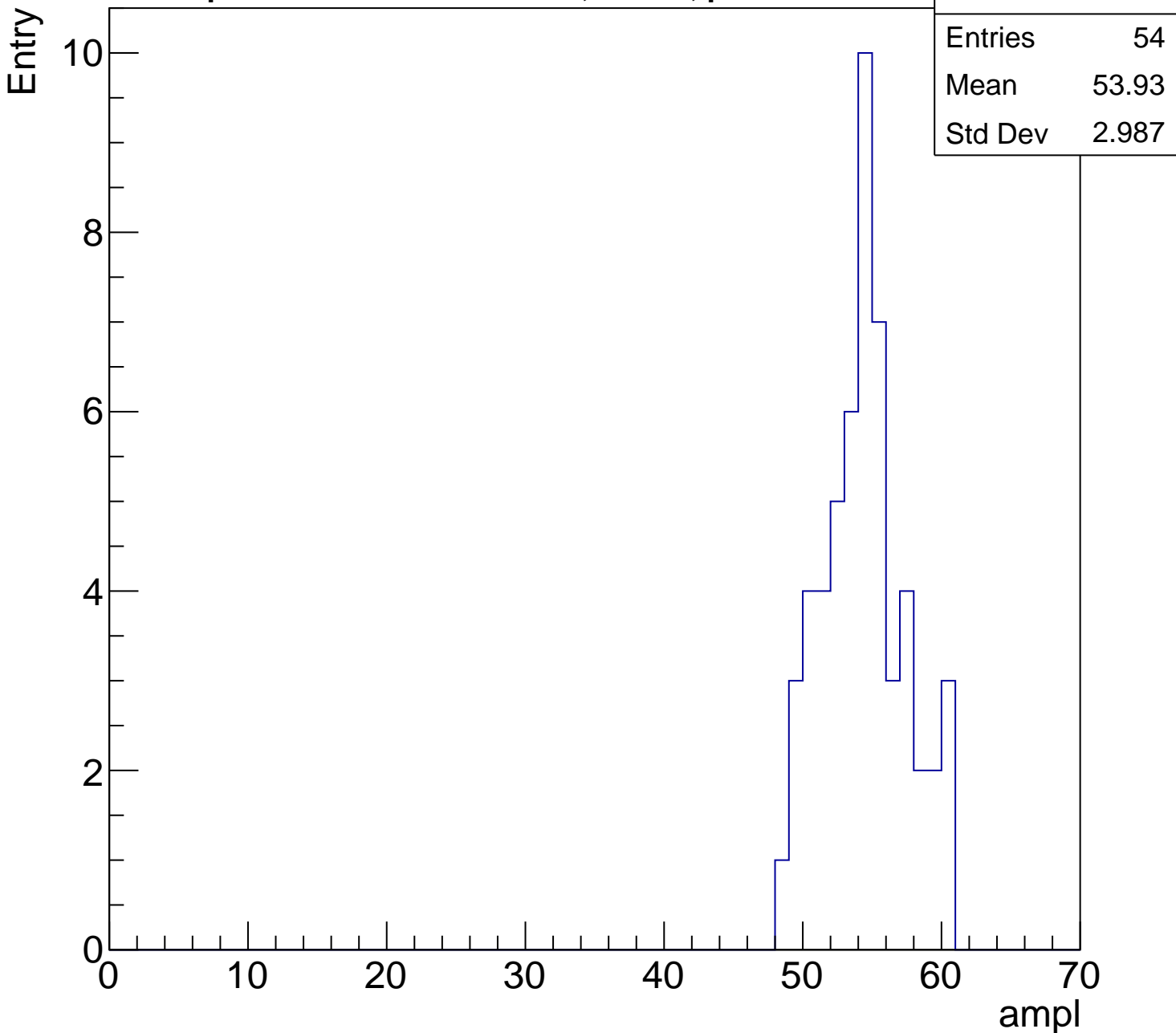
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	54
Mean	53.93
Std Dev	2.987

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70  
ampl



# B1L003S, U18-ch37, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	59
Mean	58.07
Std Dev	8.059

Entry

10

8

6

4

2

0

0

10

20

30

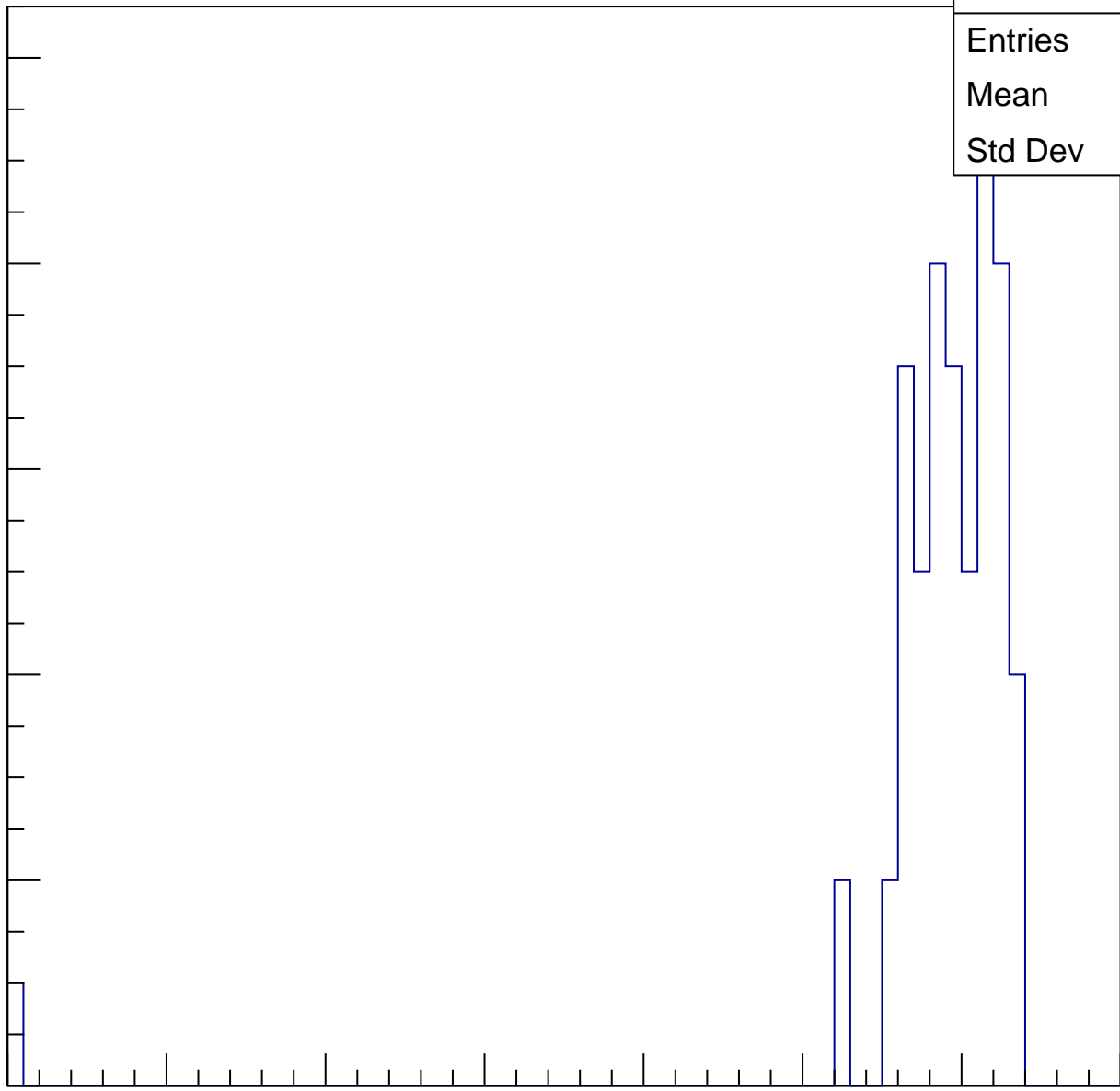
40

50

60

70

ampl

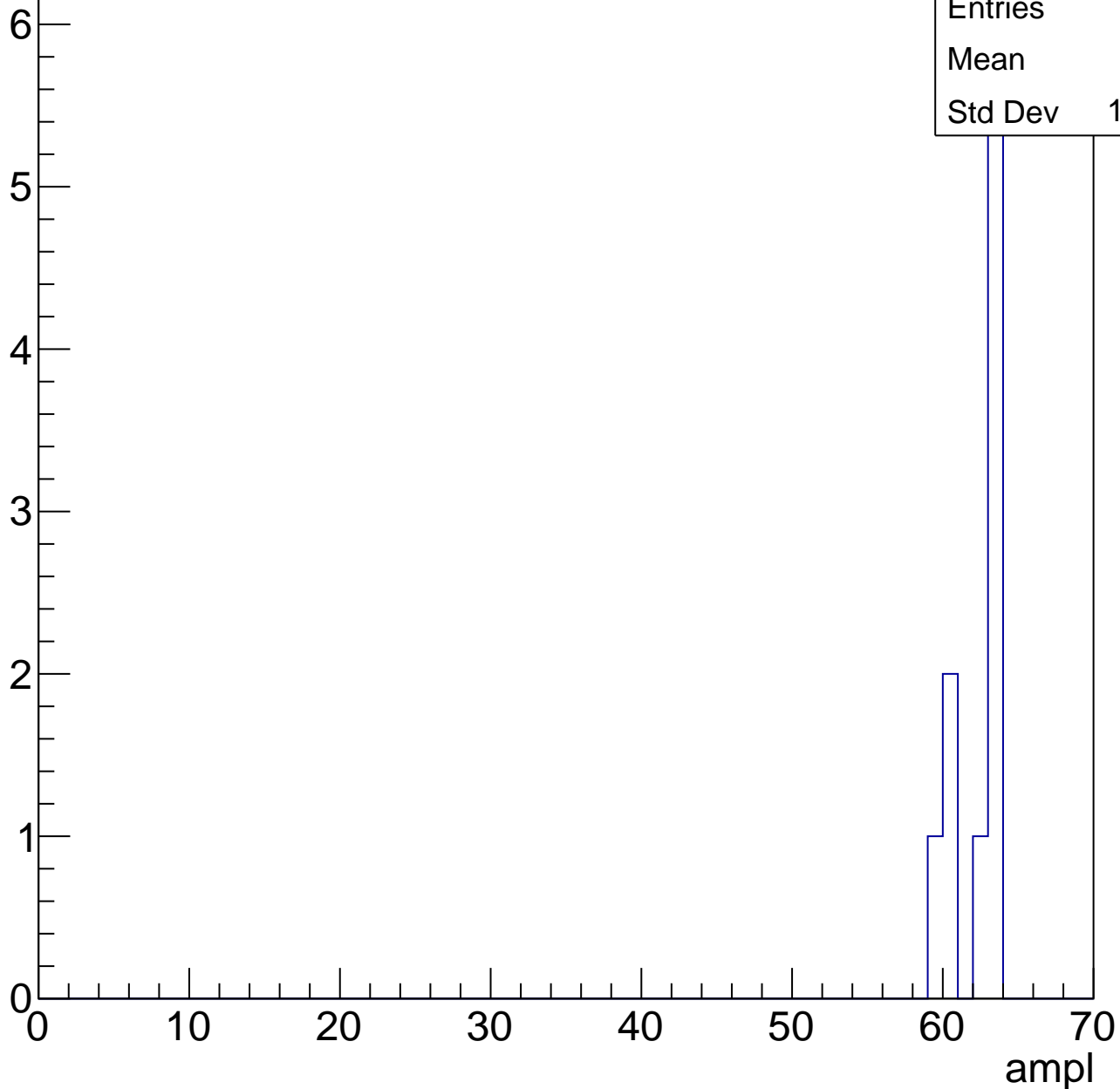


# B1L003S, U18-ch37, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	10
Mean	61.9
Std Dev	1.513

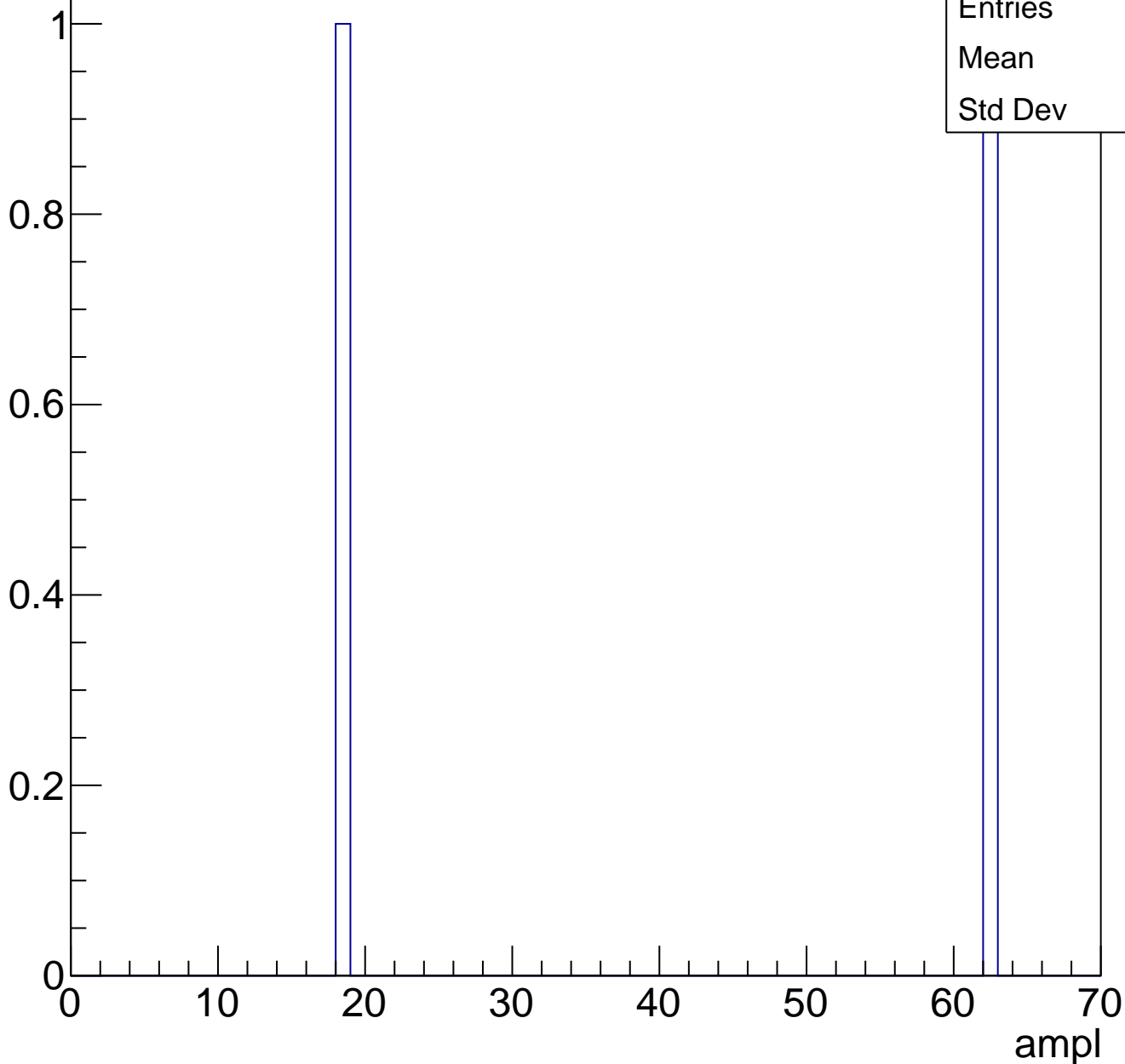




# B1L003S, U18-ch37, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U18-ch38, adc0

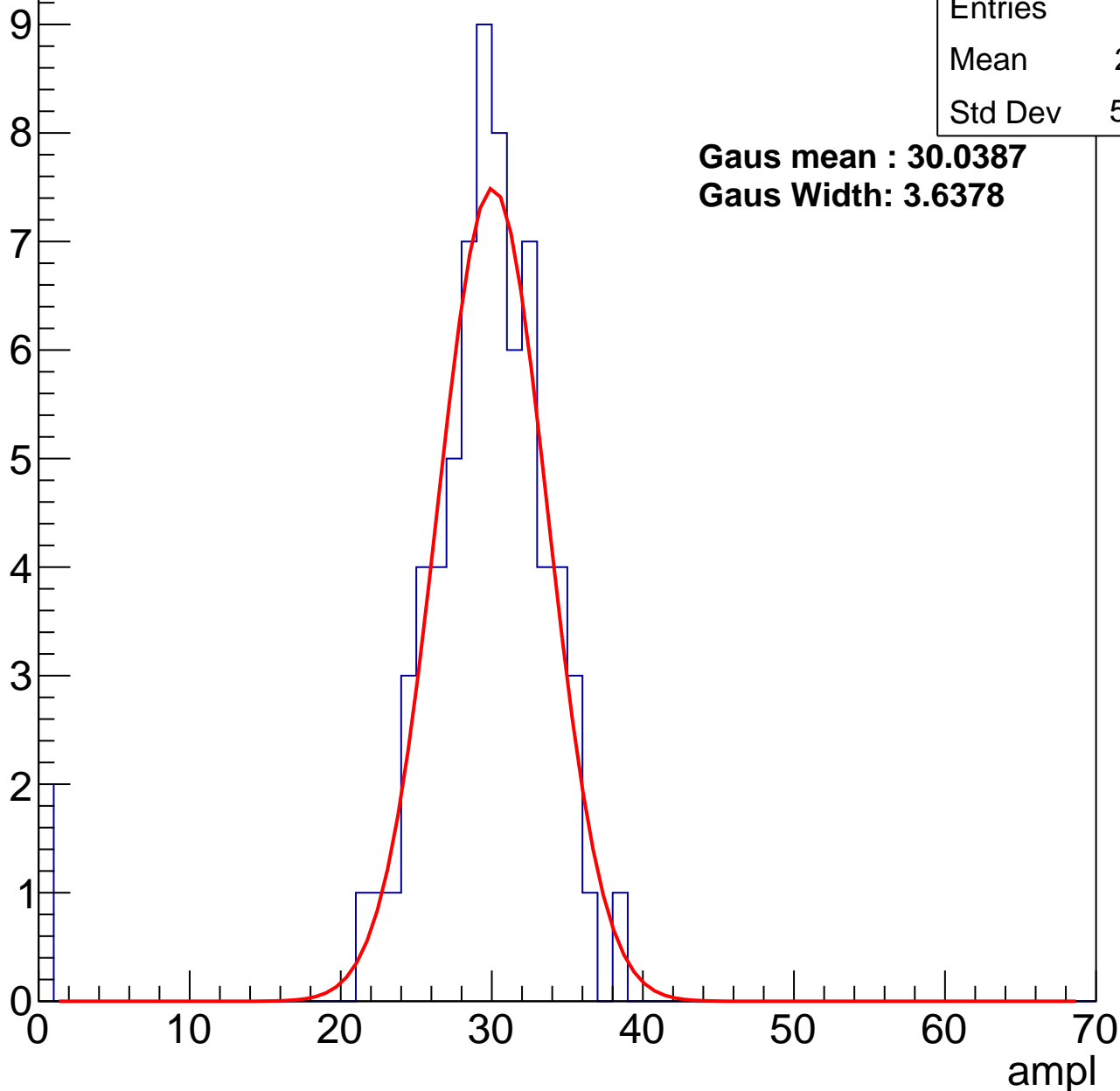
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	71
Mean	28.61
Std Dev	5.956

**Gaus mean : 30.0387**

**Gaus Width: 3.6378**



# B1L003S, U18-ch38, adc1

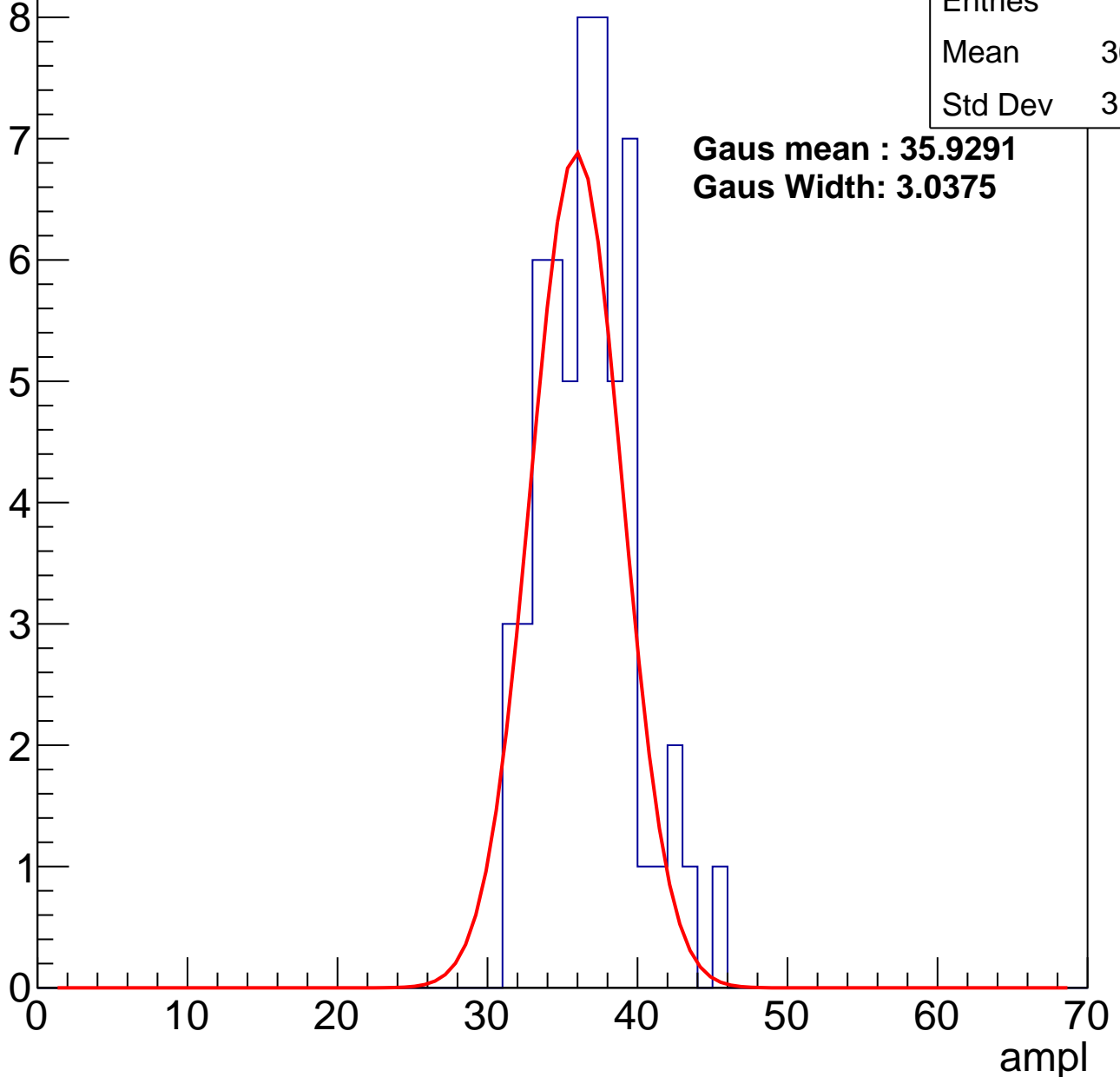
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	57
Mean	36.25
Std Dev	3.068

**Gaus mean : 35.9291**

**Gaus Width: 3.0375**



# B1L003S, U18-ch38, adc2

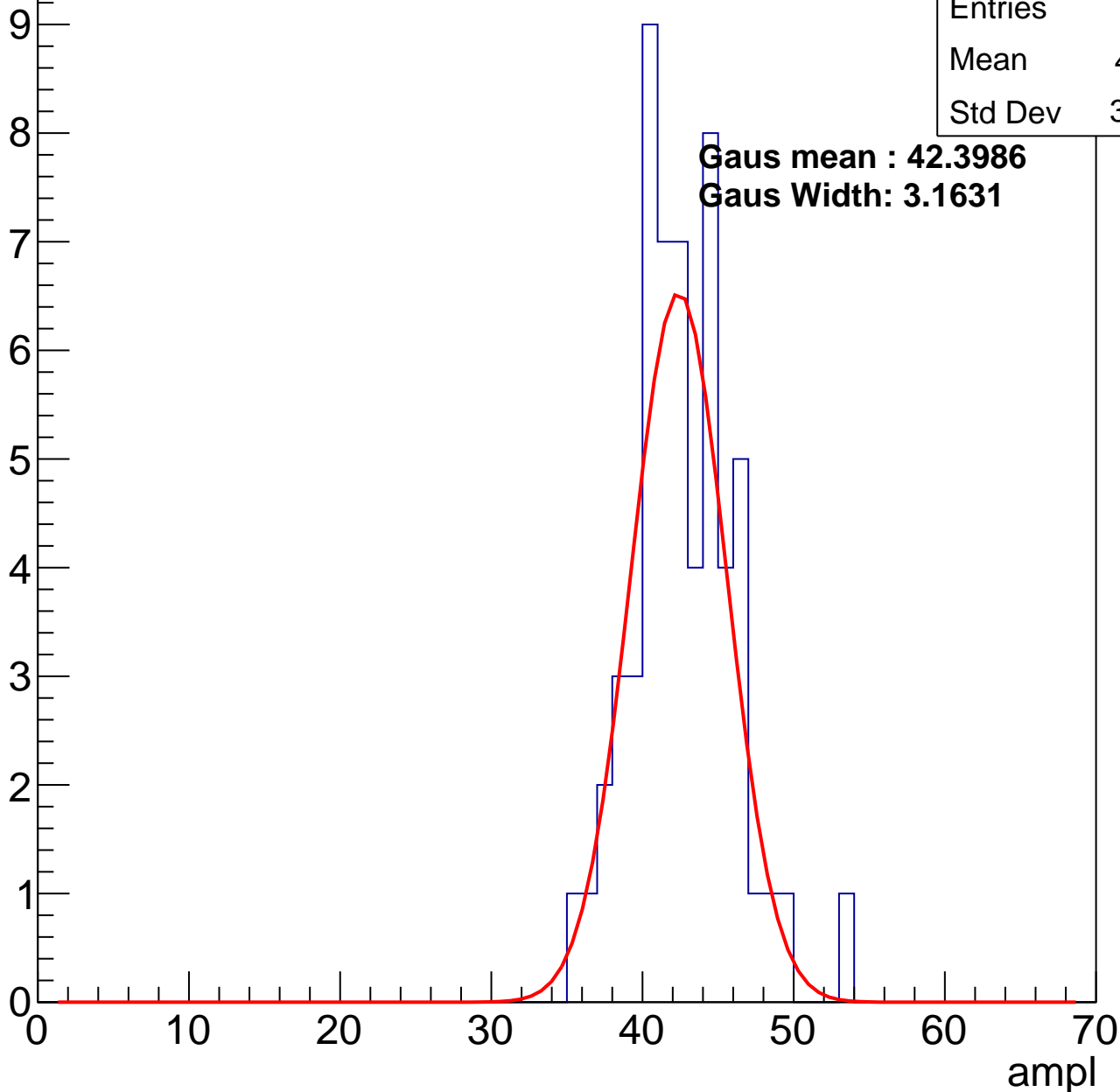
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	58
Mean	42.21
Std Dev	3.305

**Gaus mean : 42.3986**

**Gaus Width: 3.1631**

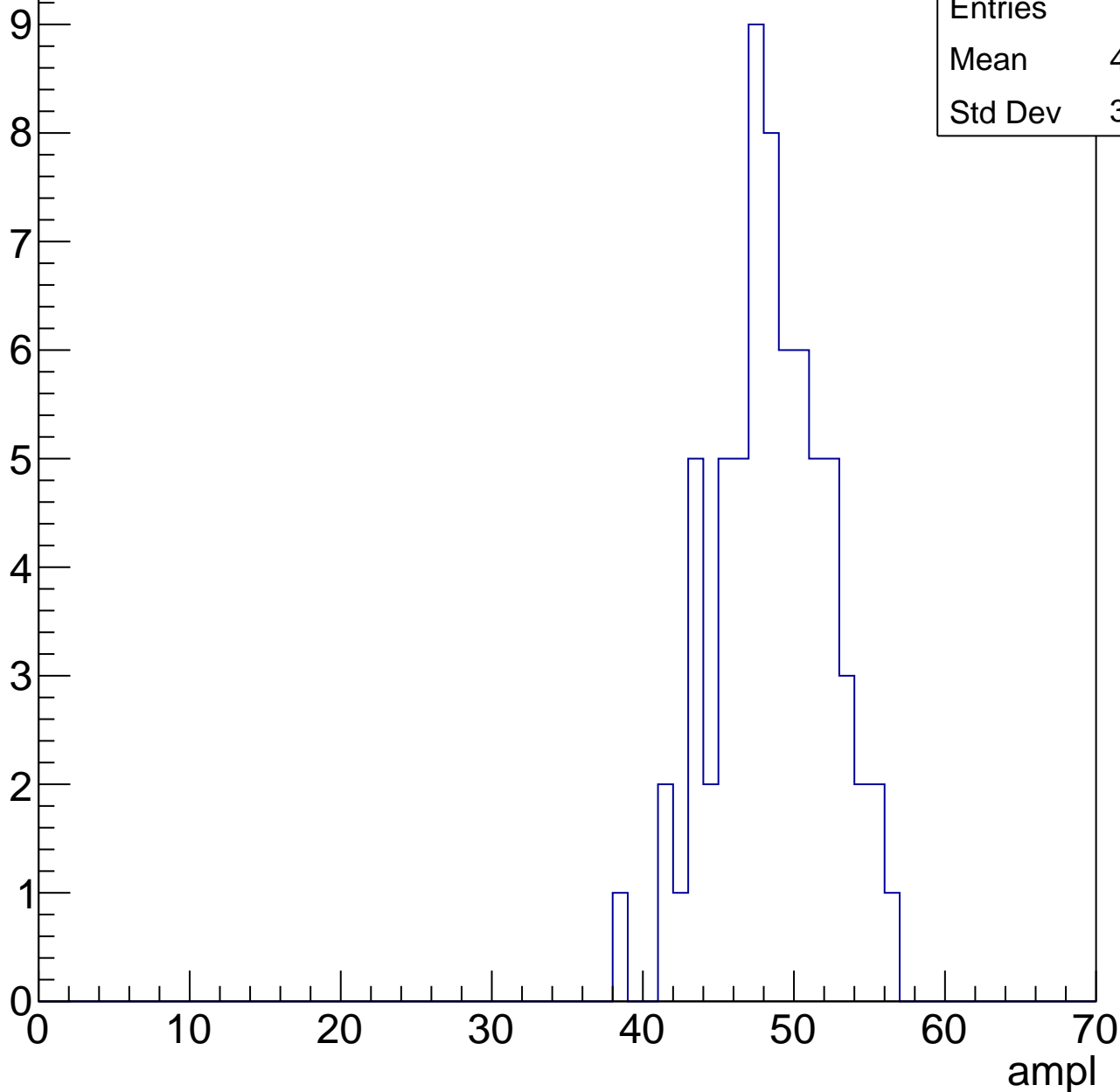


# B1L003S, U18-ch38, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

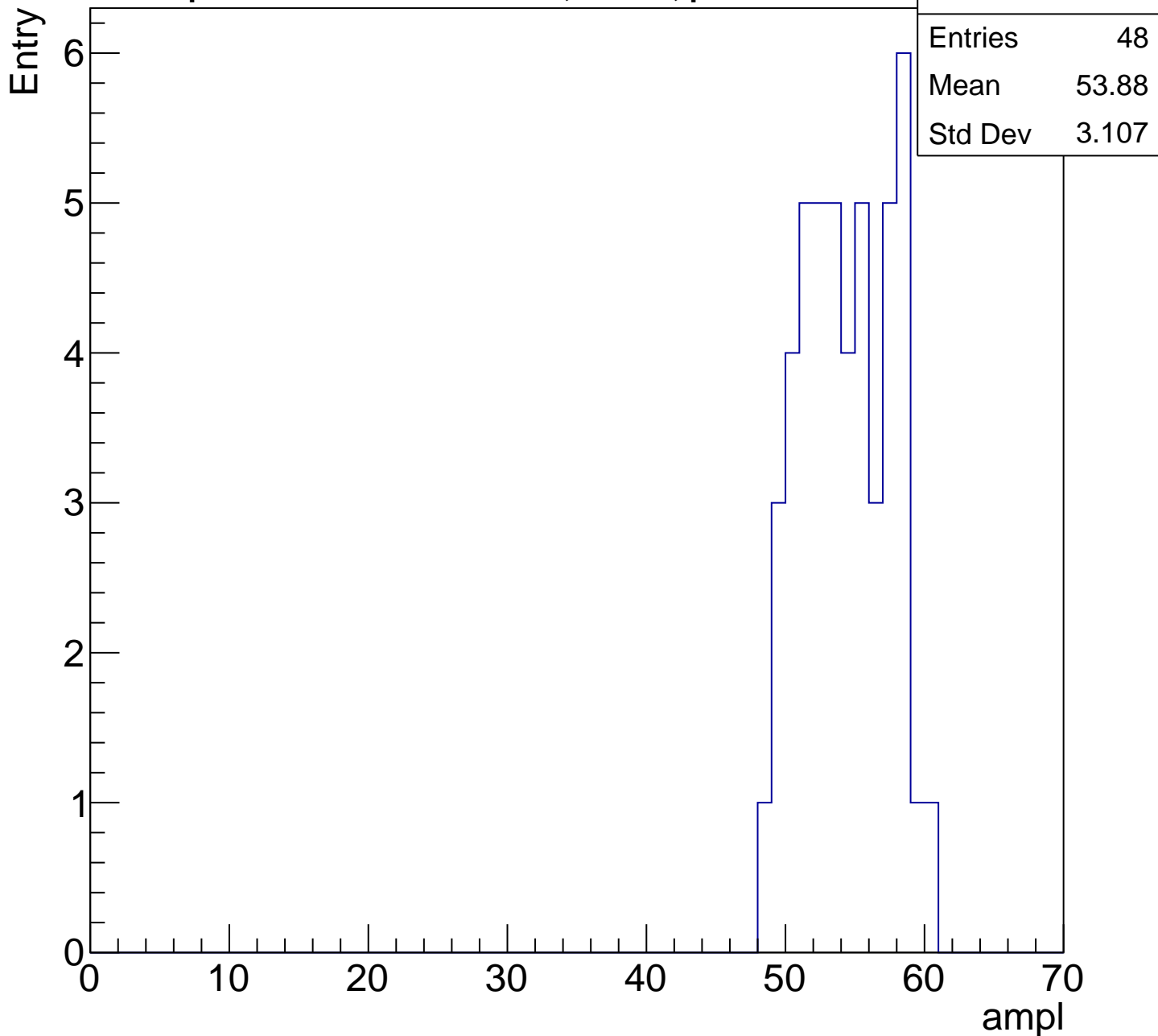
Entry

Entries	68
Mean	48.07
Std Dev	3.695



# B1L003S, U18-ch38, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2



# B1L003S, U18-ch38, adc5

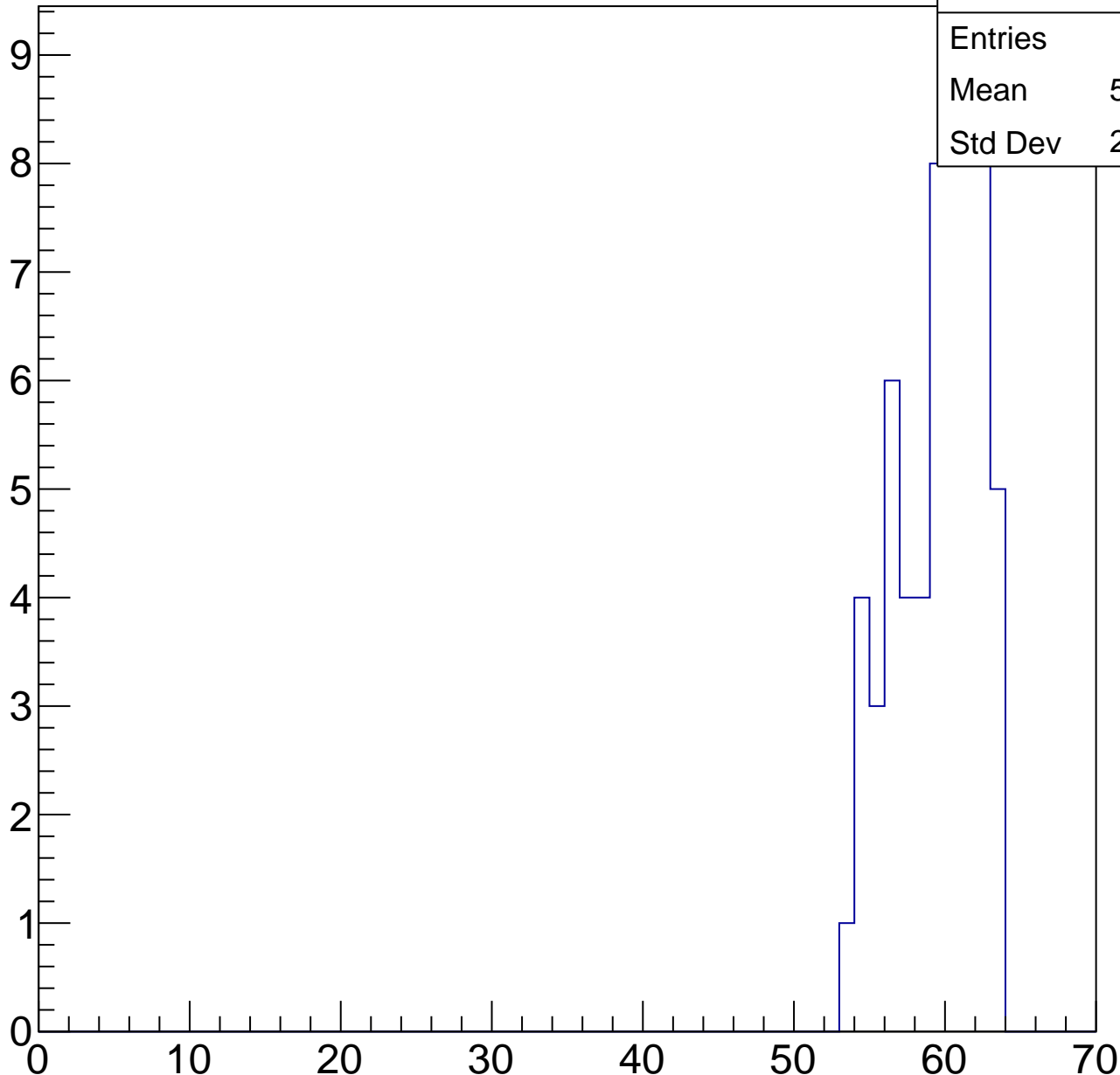
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	61
Mean	59.07
Std Dev	2.745

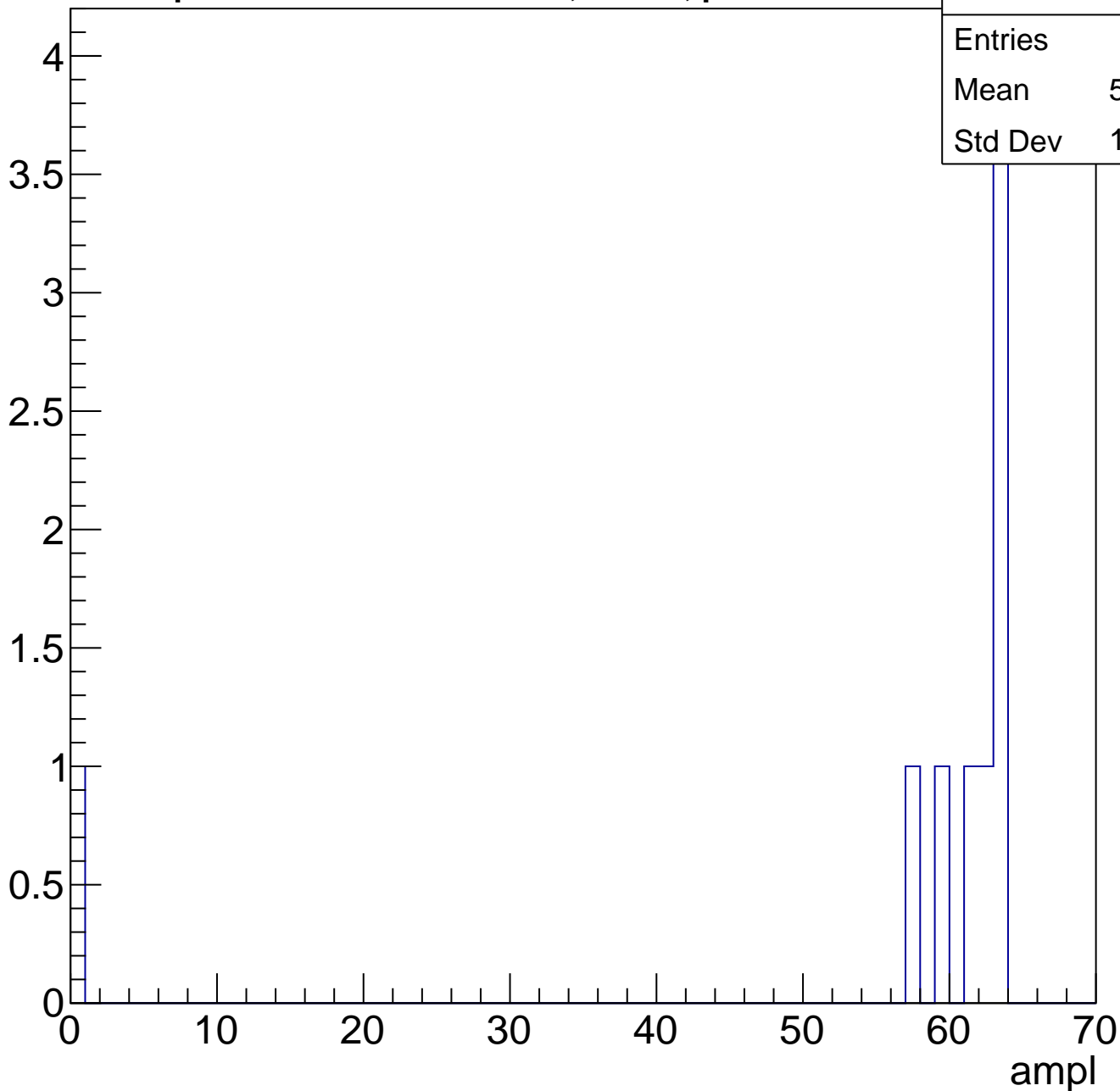
ampl



# B1L003S, U18-ch38, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

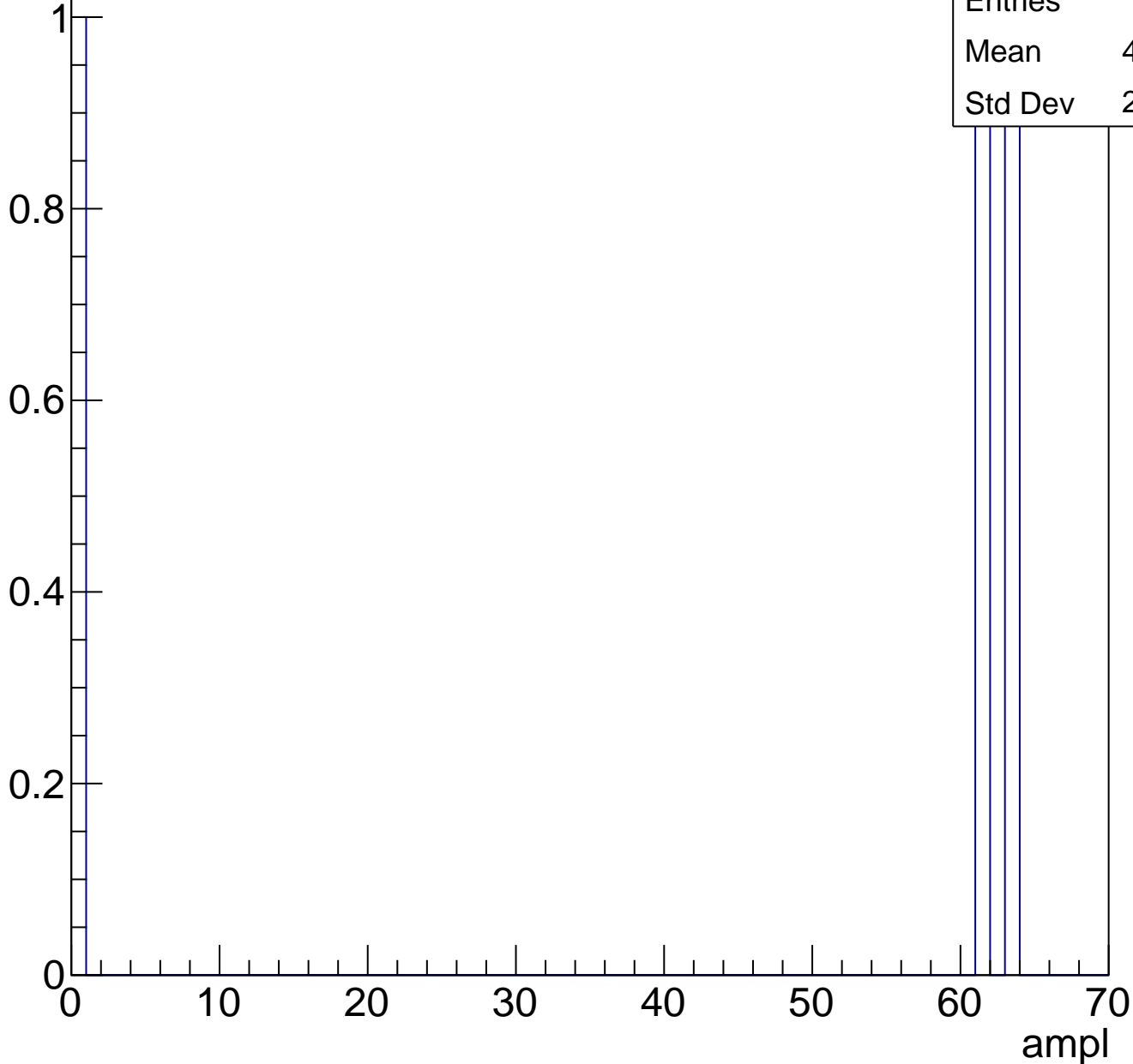




# B1L003S, U18-ch38, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U18-ch39, adc0

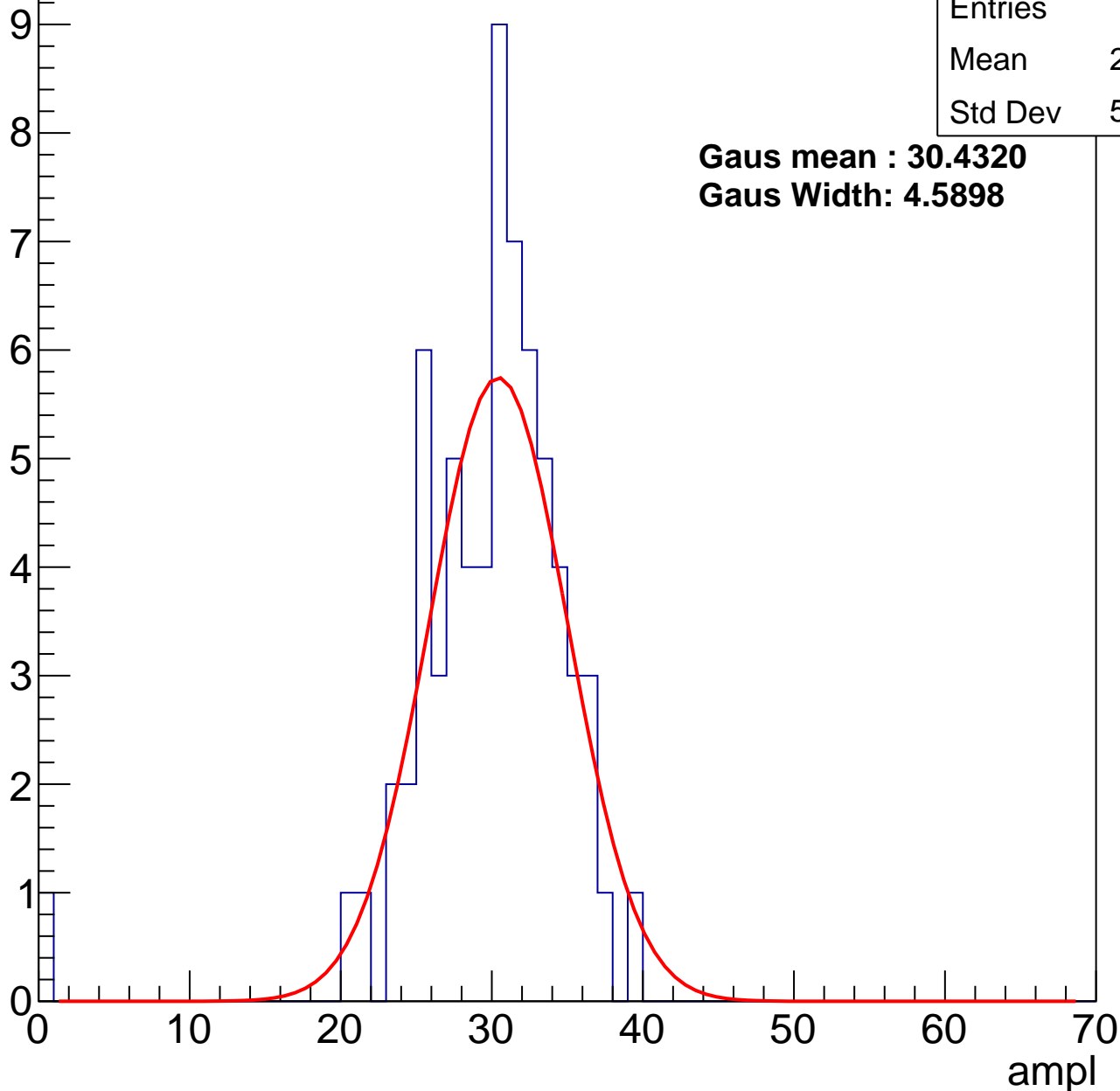
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	68
Mean	29.34
Std Dev	5.337

**Gaus mean : 30.4320**

**Gaus Width: 4.5898**



# B1L003S, U18-ch39, adc1

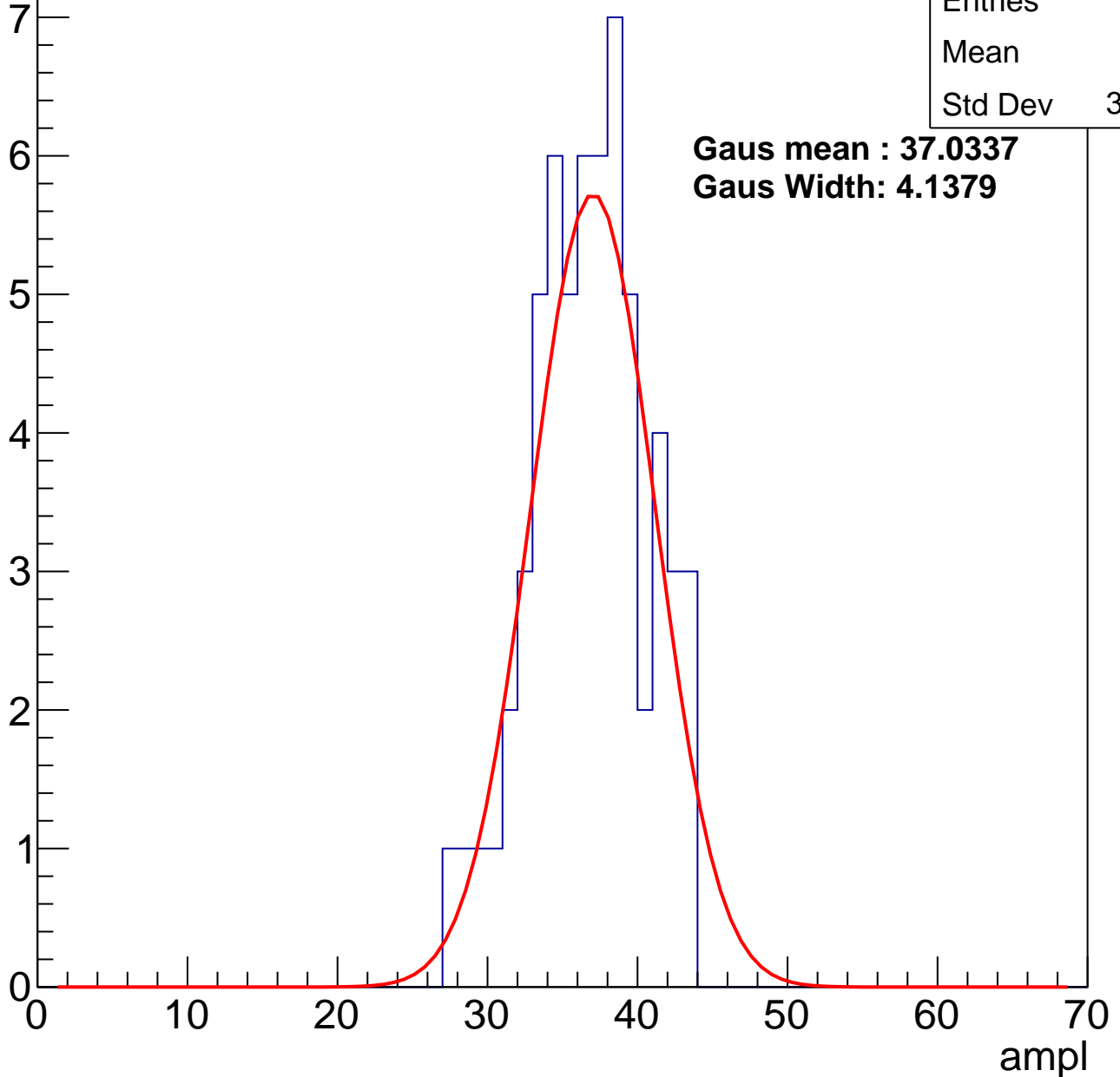
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	61
Mean	36.3
Std Dev	3.761

**Gaus mean : 37.0337**

**Gaus Width: 4.1379**



# B1L003S, U18-ch39, adc2

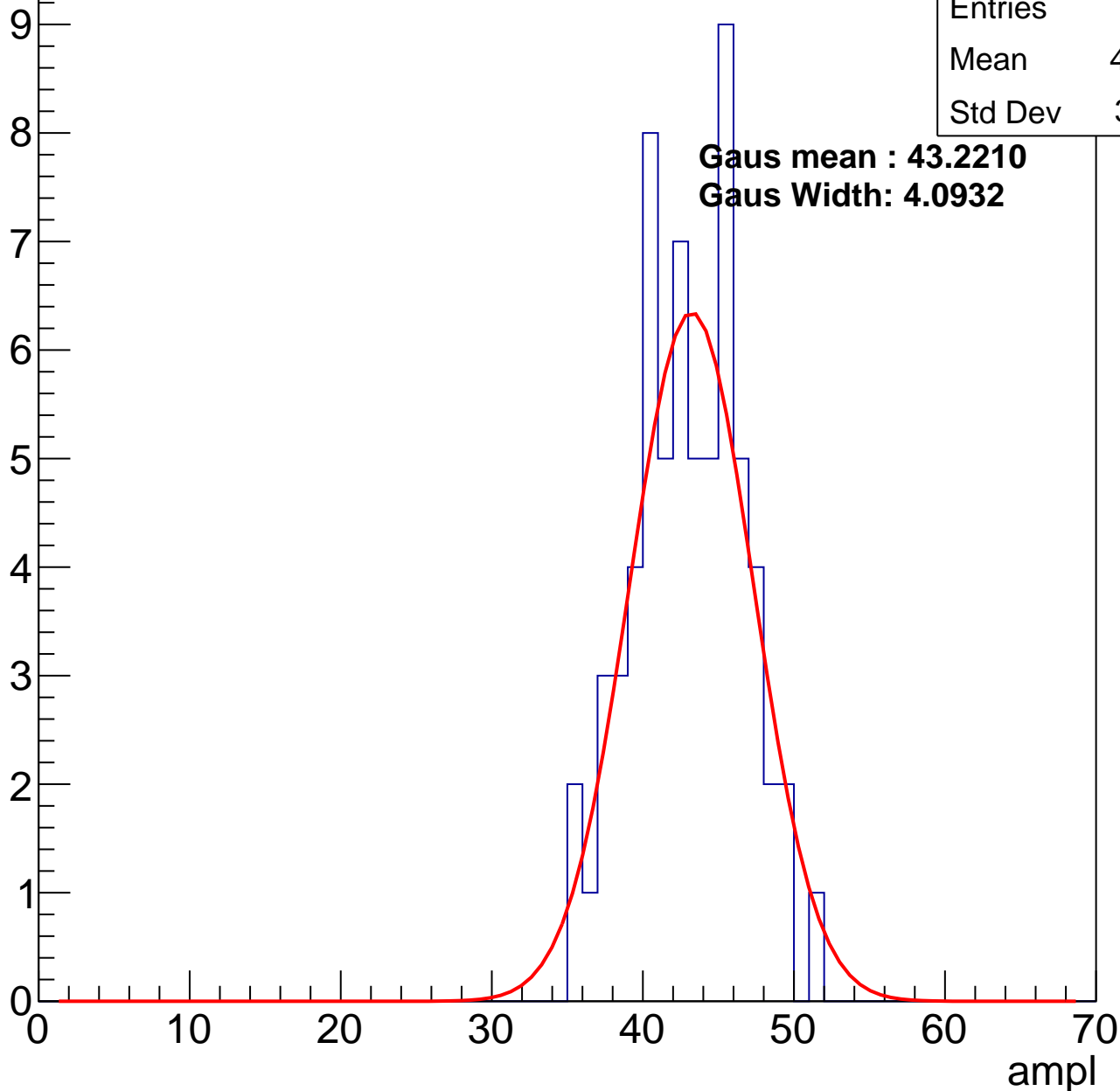
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	66
Mean	42.56
Std Dev	3.581

**Gaus mean : 43.2210**

**Gaus Width: 4.0932**

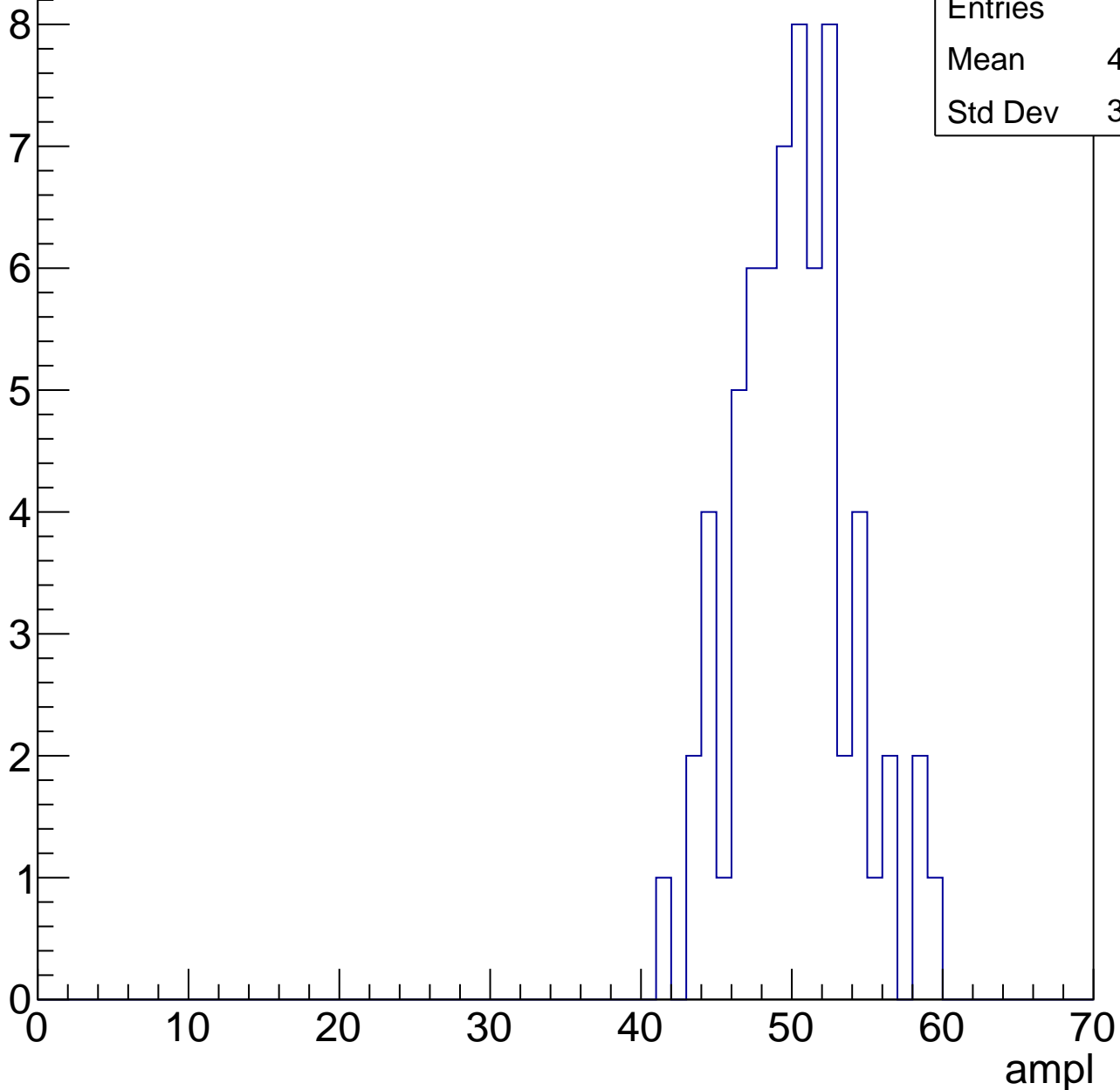


# B1L003S, U18-ch39, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	66
Mean	49.65
Std Dev	3.756

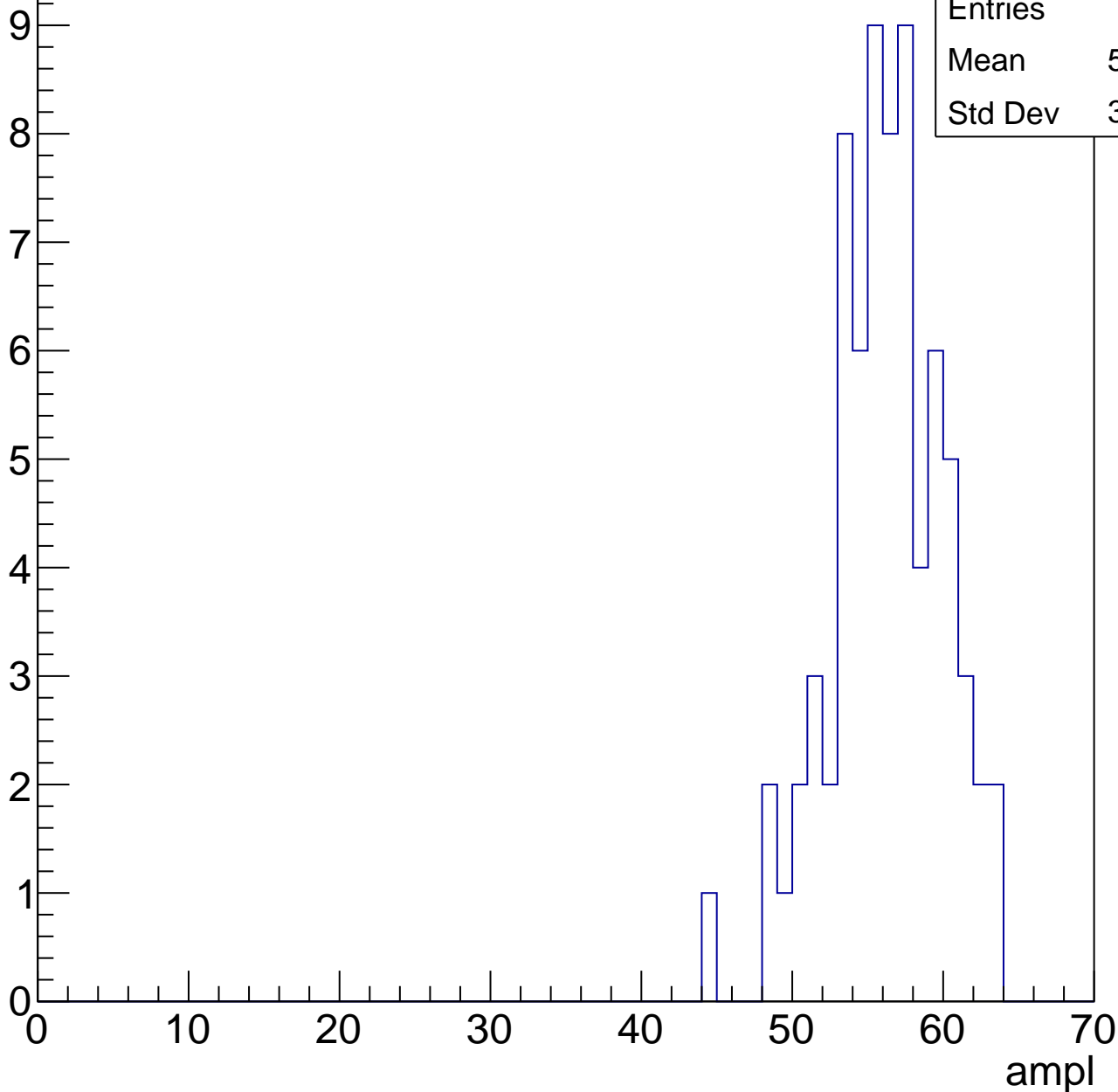


# B1L003S, U18-ch39, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	73
Mean	55.74
Std Dev	3.709

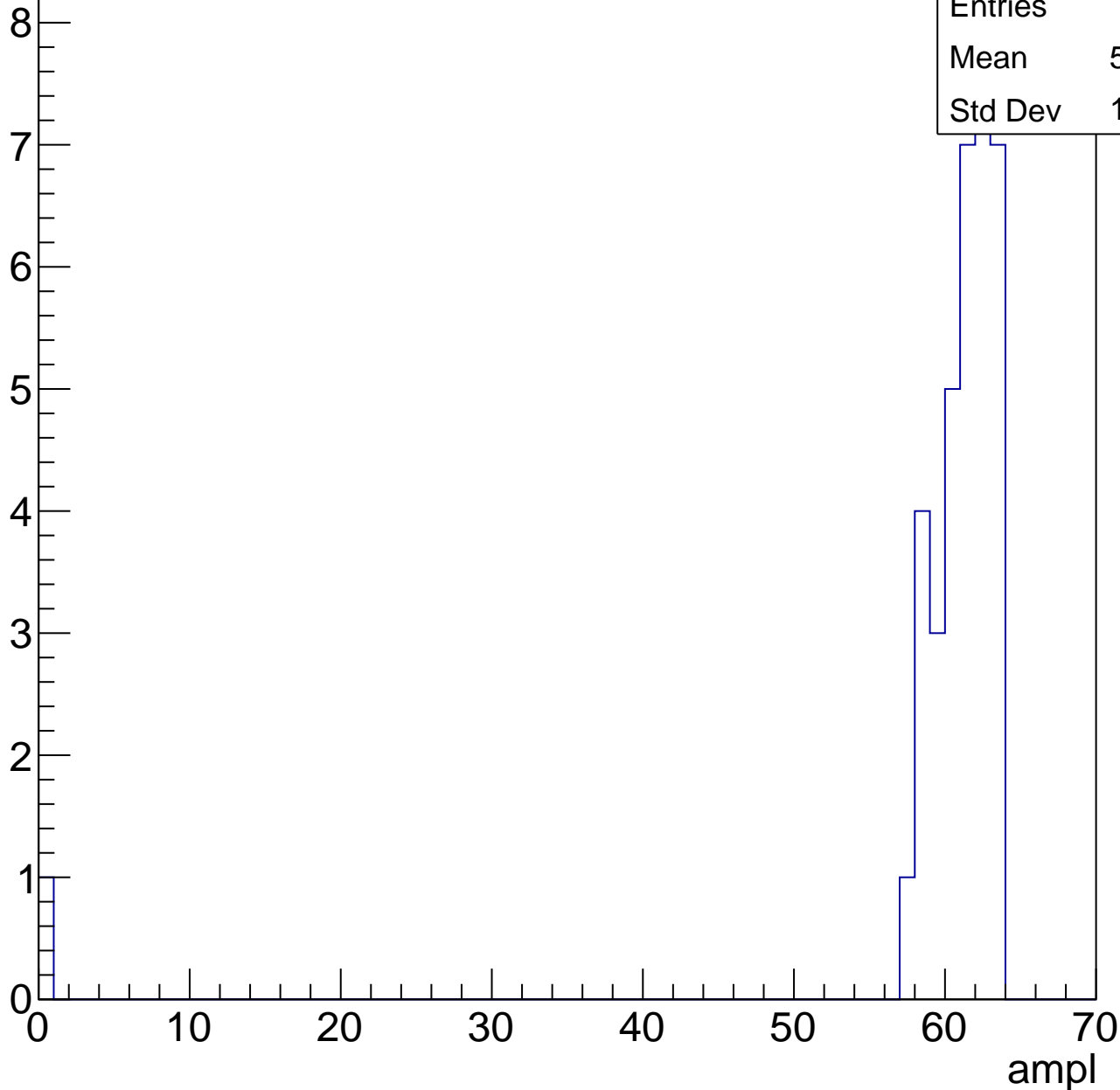


# B1L003S, U18-ch39, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	36
Mean	59.17
Std Dev	10.14



# B1L003S, U18-ch39, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	1
Mean	63
Std Dev	0



# B1L003S, U18-ch39, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch40, adc0

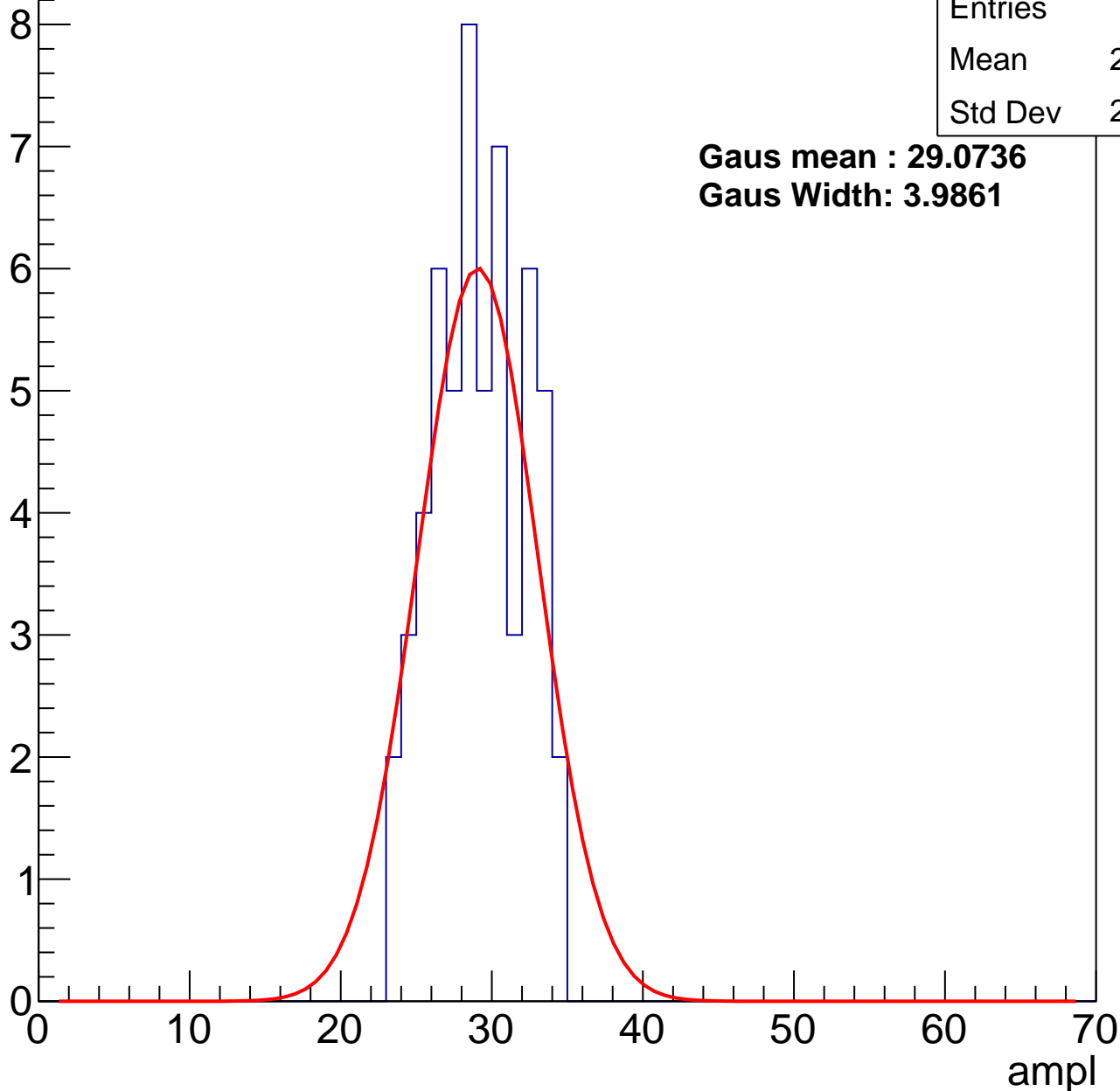
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	56
Mean	28.68
Std Dev	2.959

**Gaus mean : 29.0736**

**Gaus Width: 3.9861**



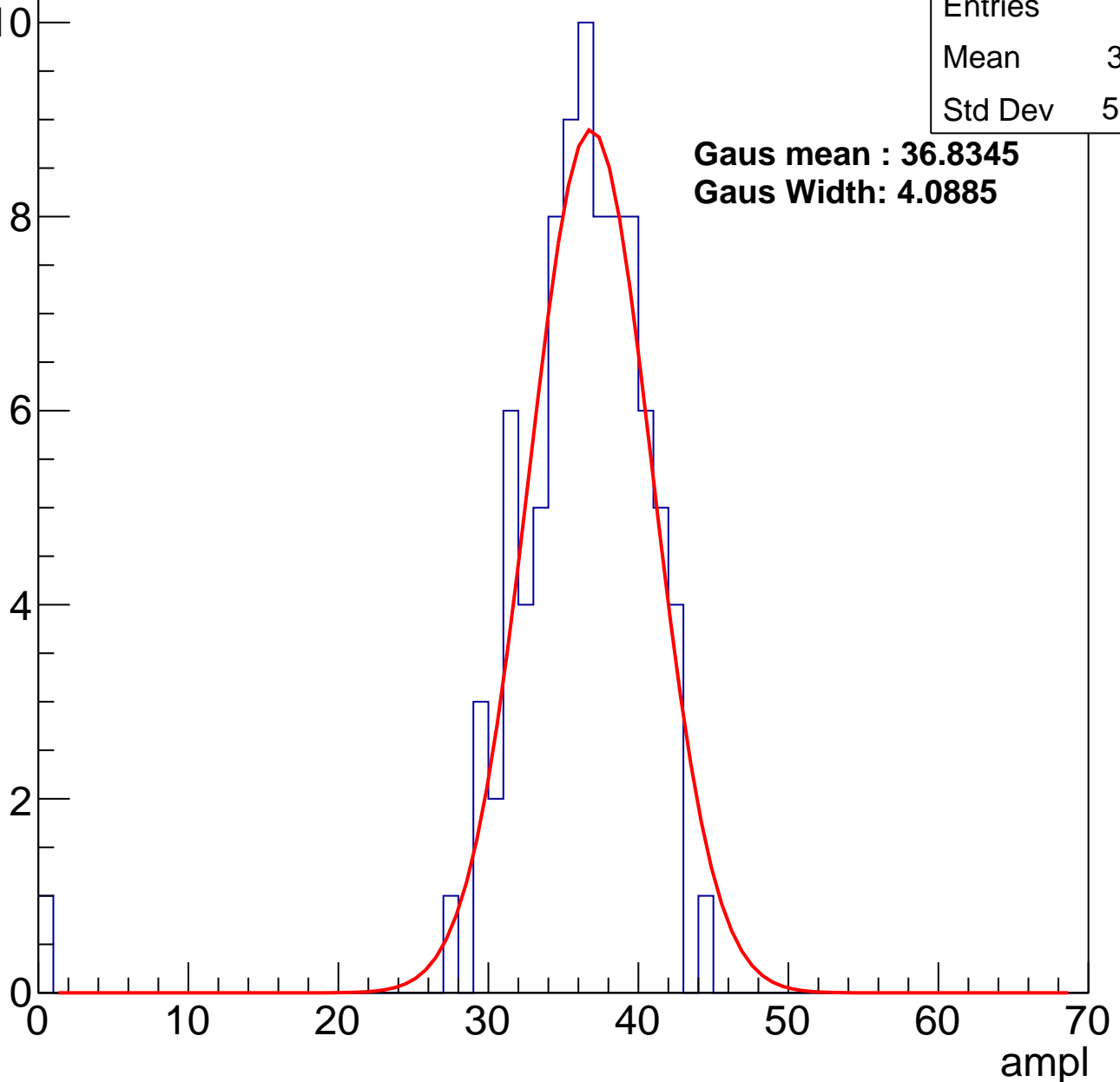
# B1L003S, U18-ch40, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	89
Mean	35.61
Std Dev	5.218

**Gaus mean : 36.8345**  
**Gaus Width: 4.0885**



# B1L003S, U18-ch40, adc2

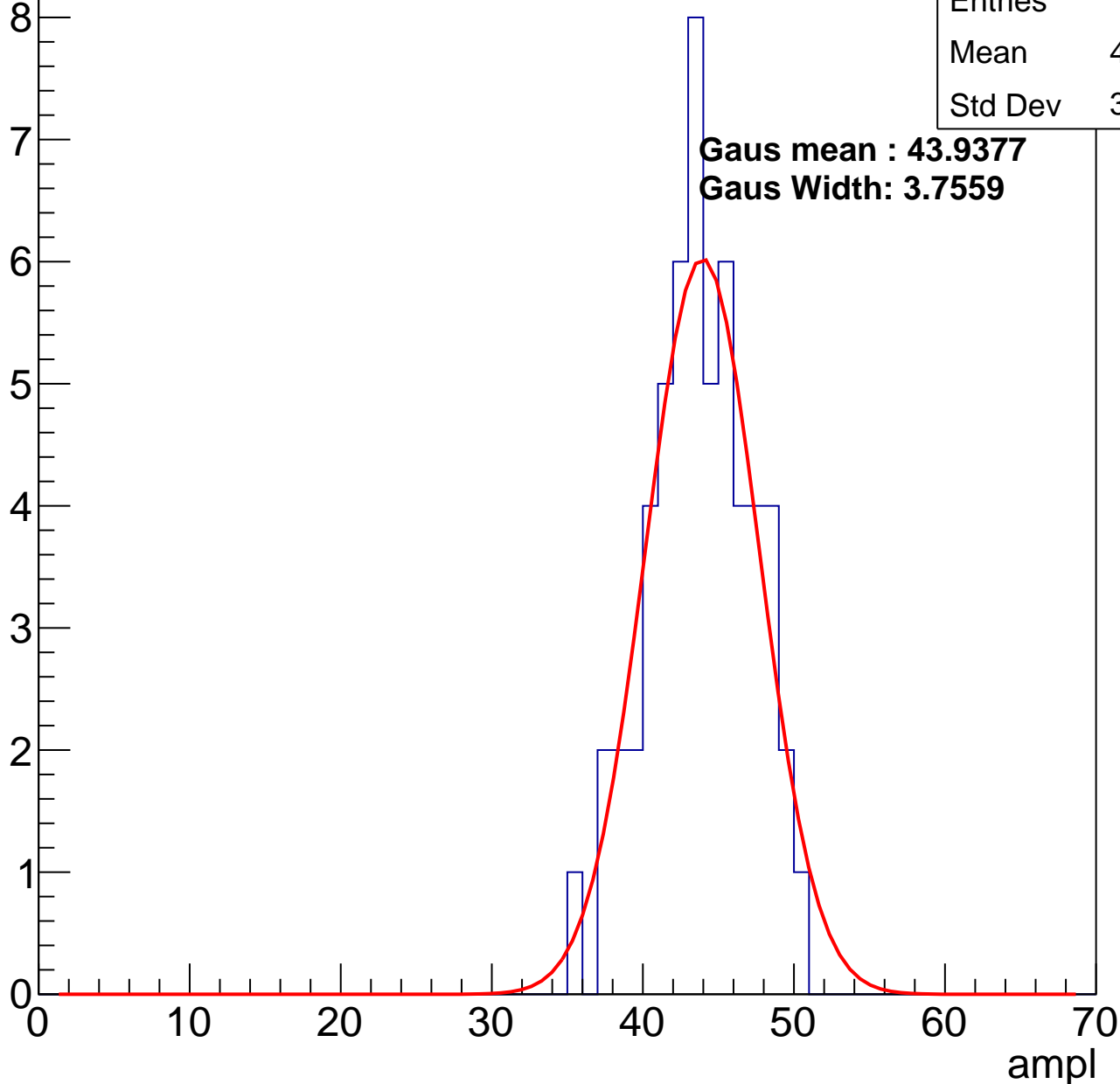
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	56
Mean	43.32
Std Dev	3.339

**Gaus mean : 43.9377**

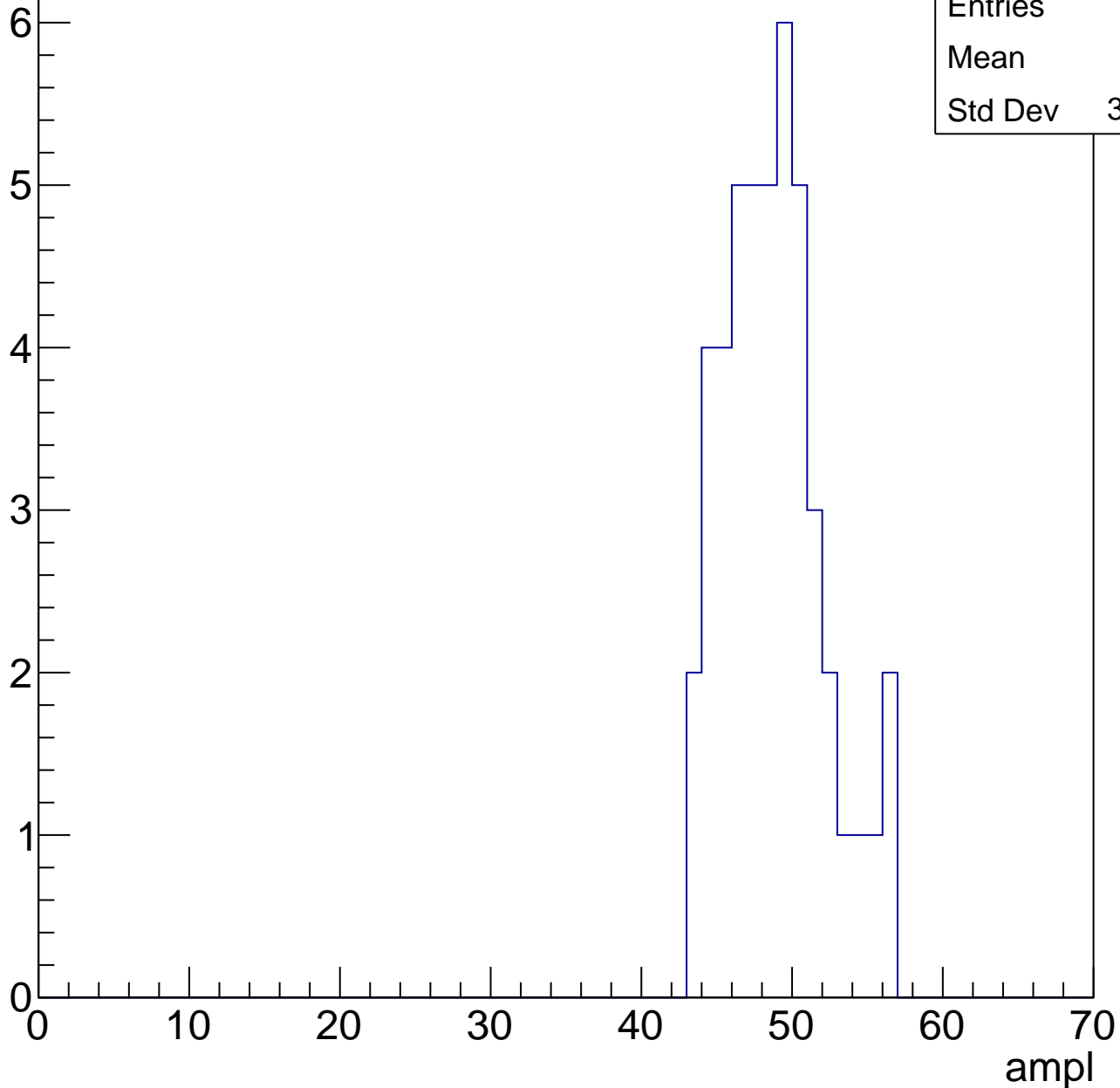
**Gaus Width: 3.7559**



# B1L003S, U18-ch40, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

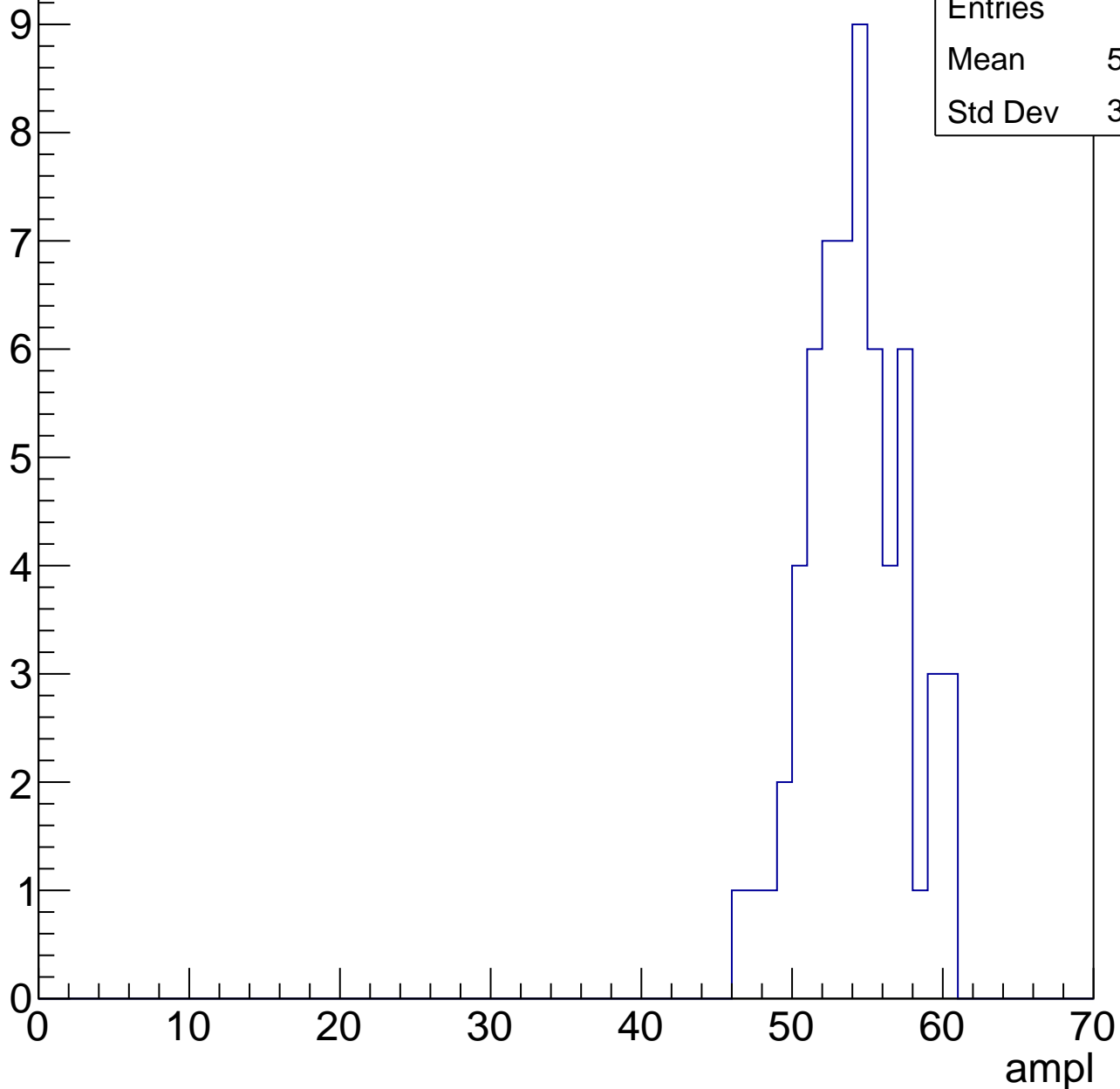
Entry



# B1L003S, U18-ch40, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



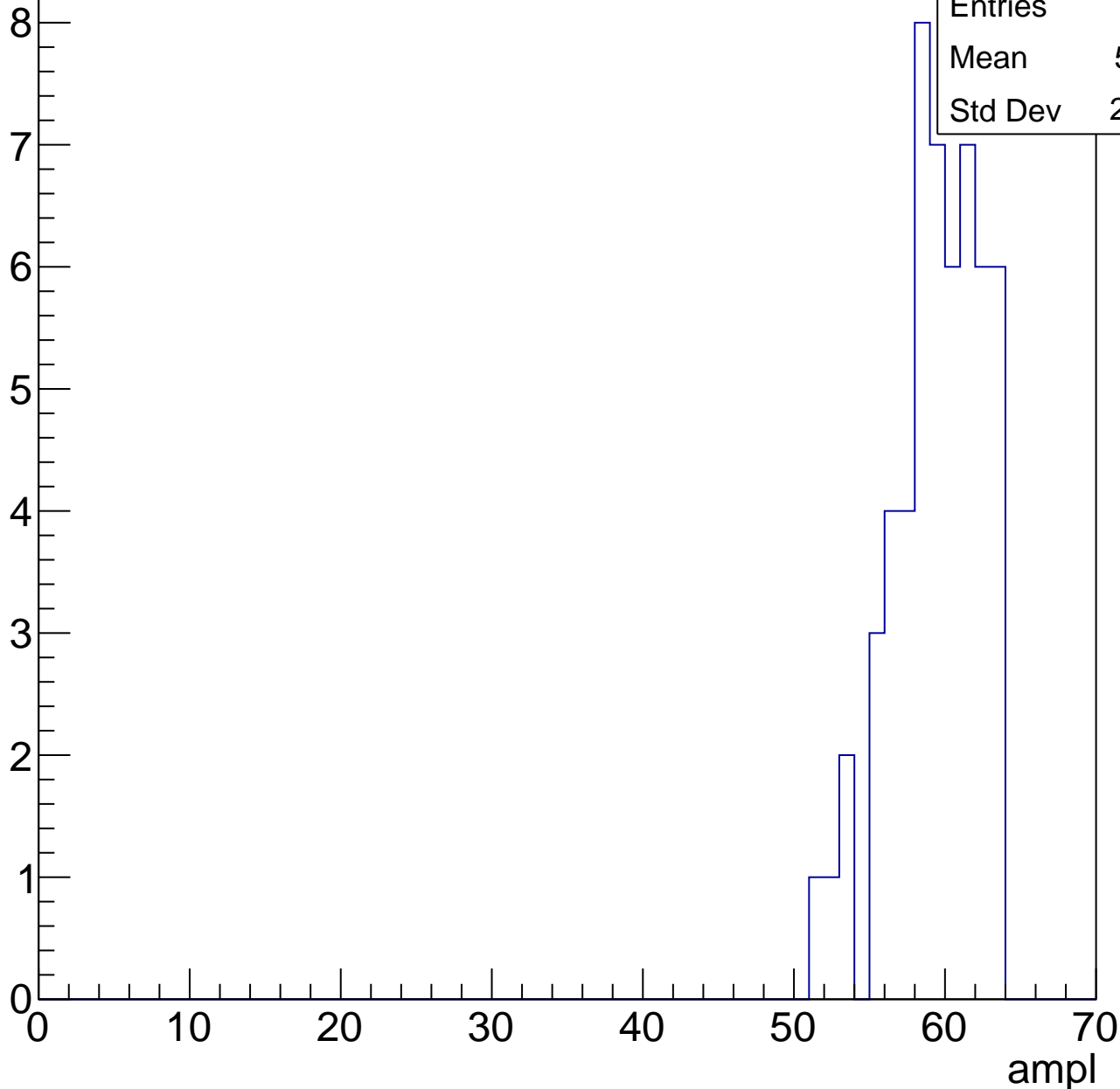
Entries	61
Mean	53.72
Std Dev	3.194

# B1L003S, U18-ch40, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

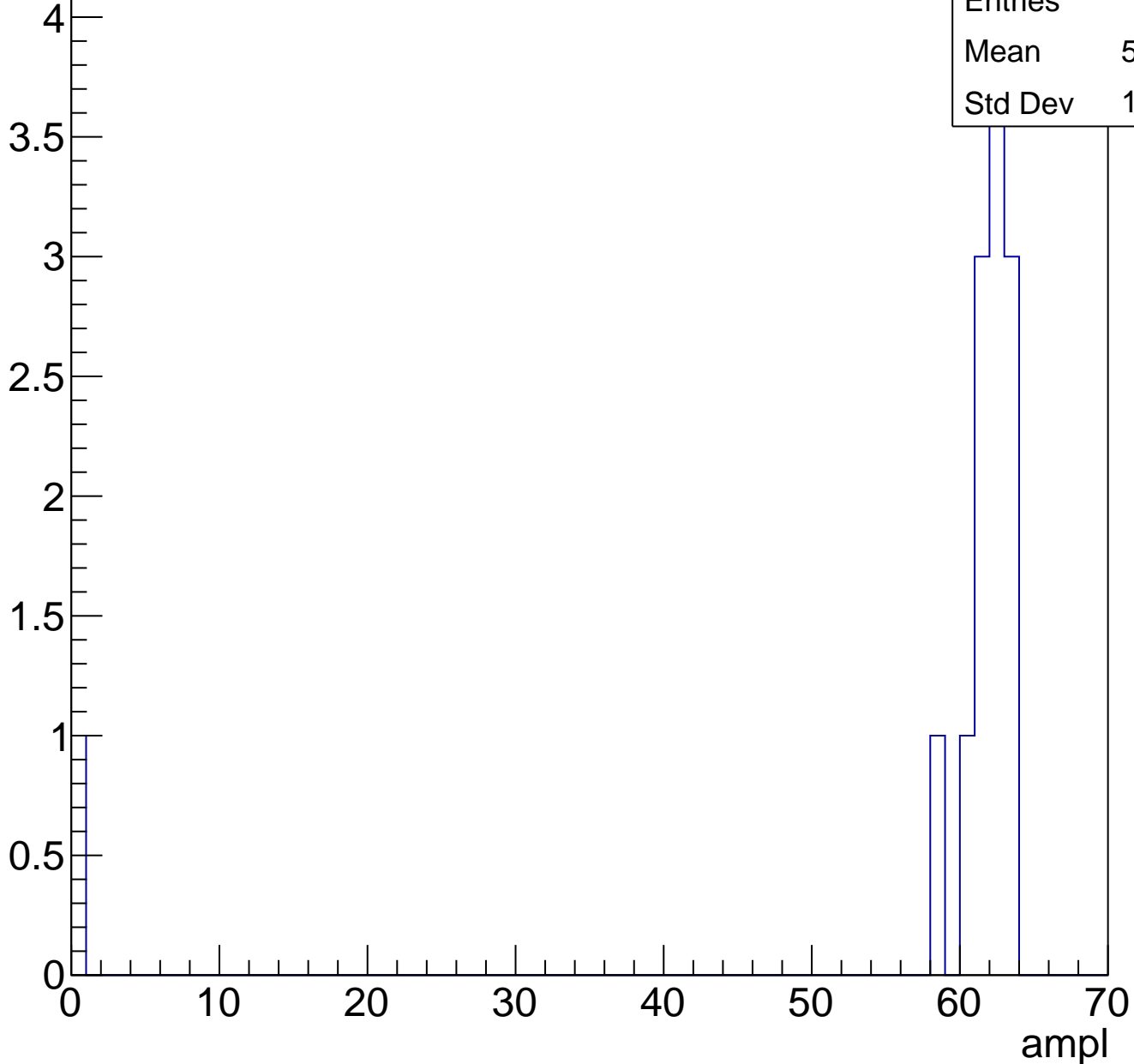
Entries	55
Mean	58.91
Std Dev	2.944



# B1L003S, U18-ch40, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U18-ch40, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

1  
0.8  
0.6  
0.4  
0.2  
0

Entries	2
Mean	43
Std Dev	20

ampl

# B1L003S, U18-ch41, adc0

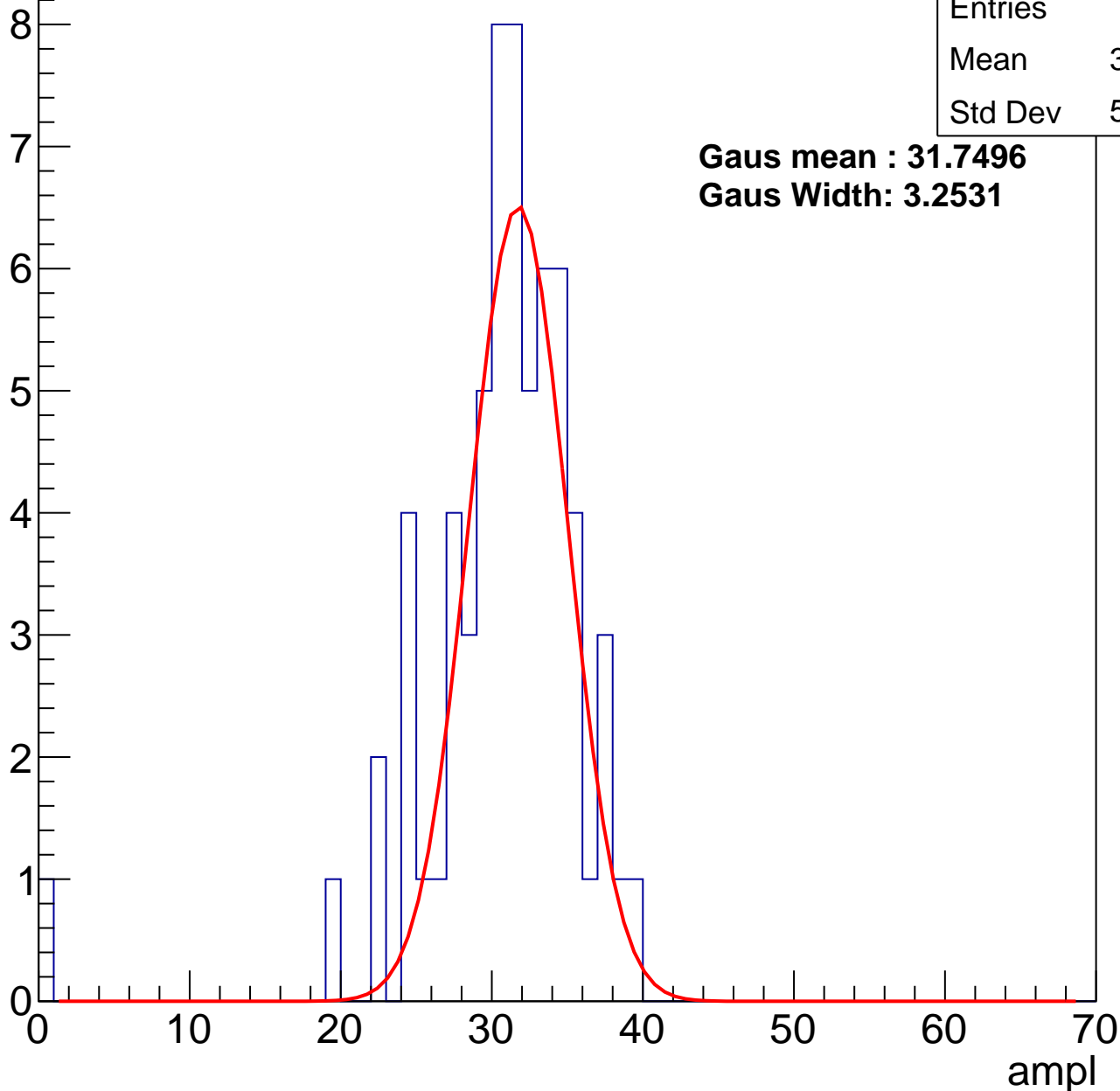
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	65
Mean	30.17
Std Dev	5.535

**Gaus mean : 31.7496**

**Gaus Width: 3.2531**



# B1L003S, U18-ch41, adc1

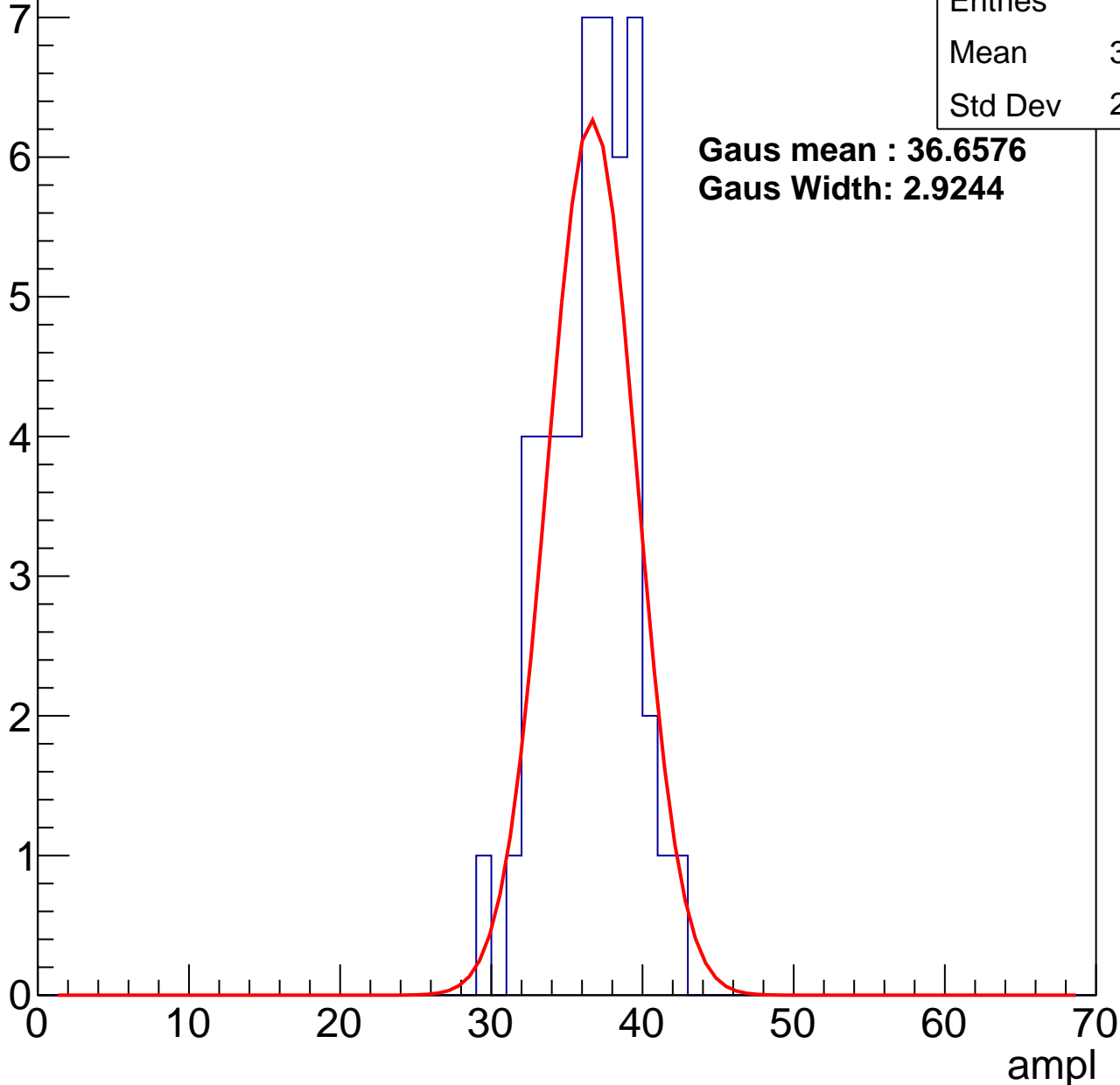
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	49
Mean	36.14
Std Dev	2.785

**Gaus mean : 36.6576**

**Gaus Width: 2.9244**



# B1L003S, U18-ch41, adc2

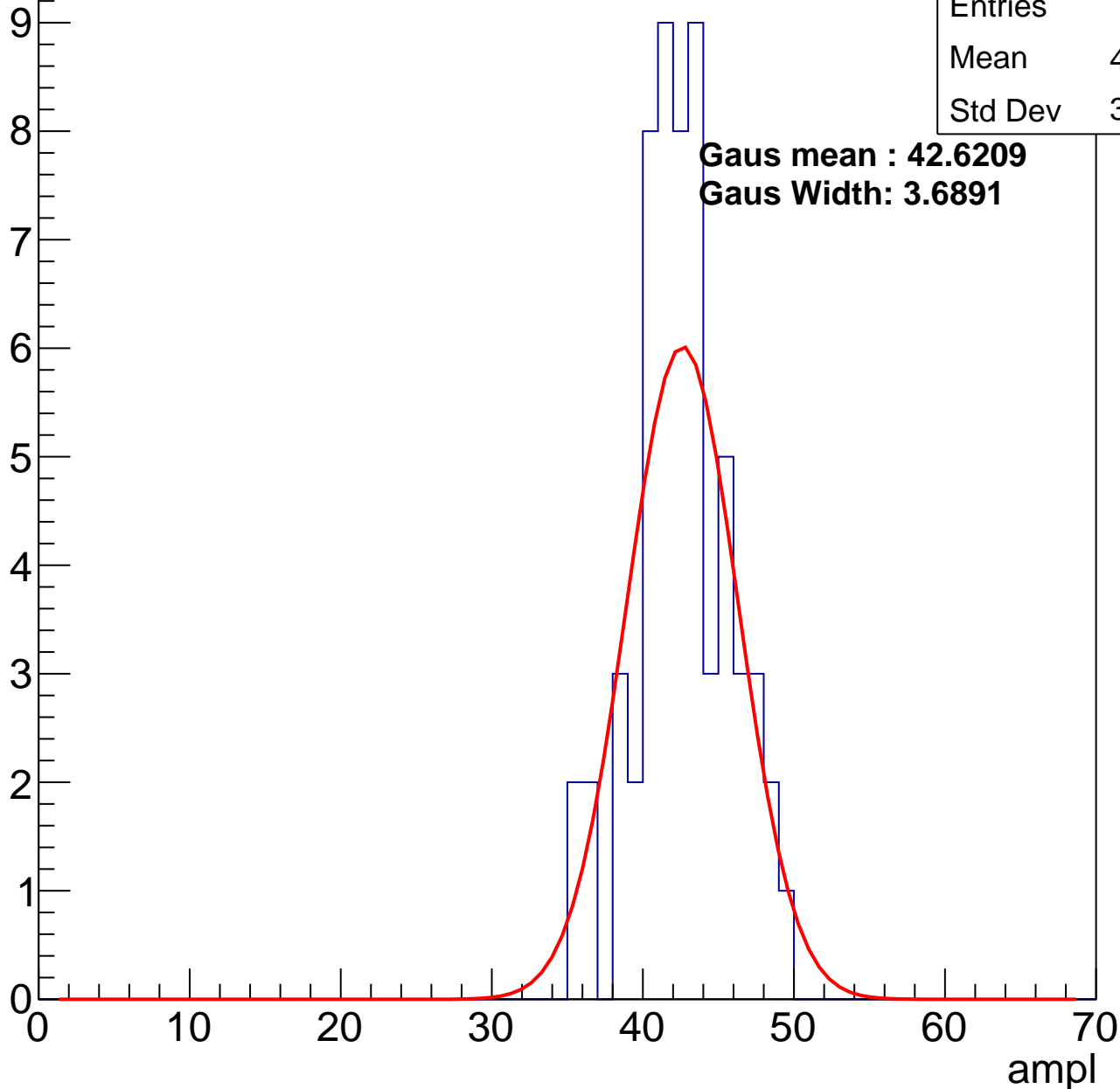
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	60
Mean	42.12
Std Dev	3.126

**Gaus mean : 42.6209**

**Gaus Width: 3.6891**

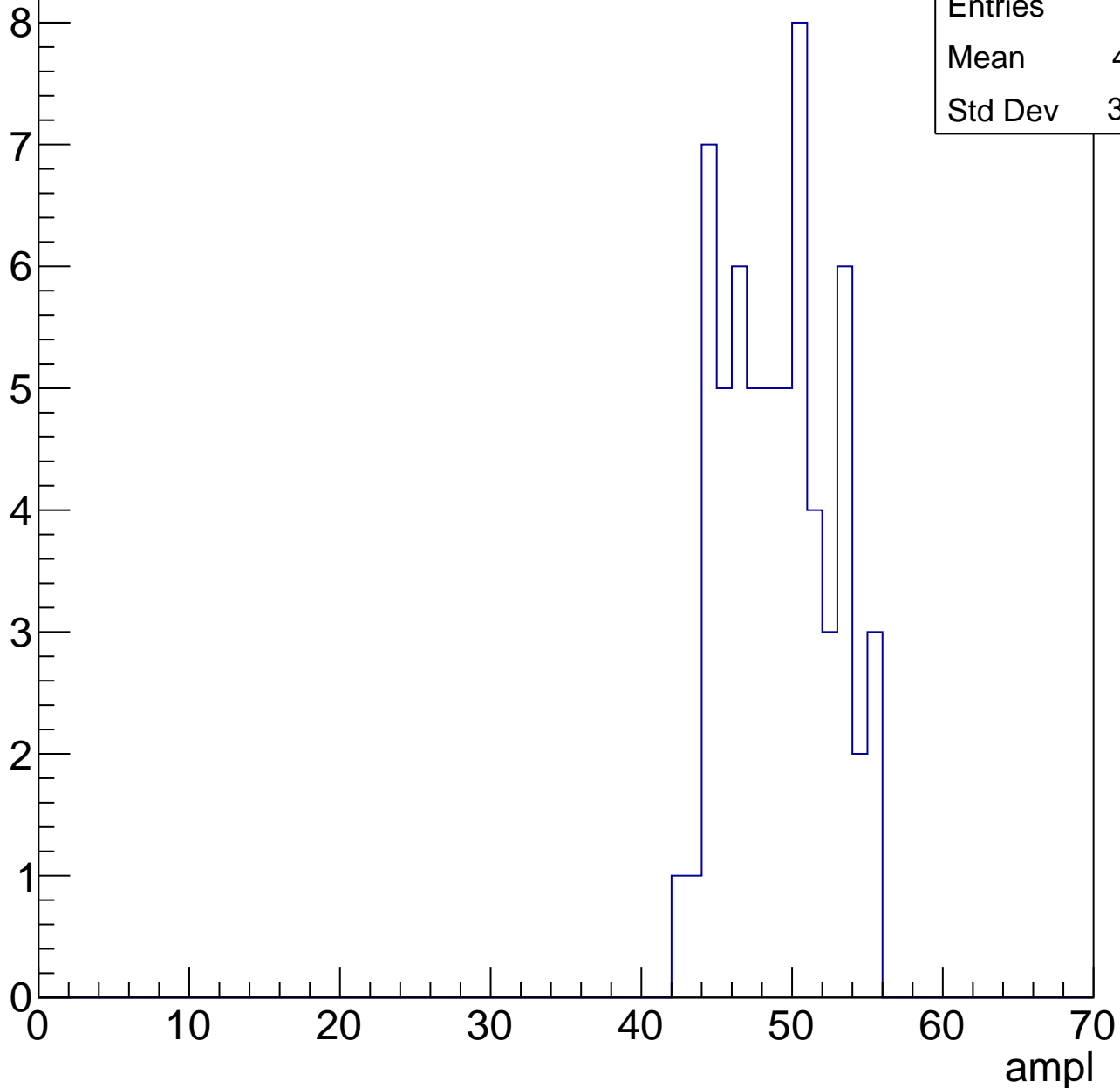


# B1L003S, U18-ch41, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	61
Mean	48.61
Std Dev	3.423

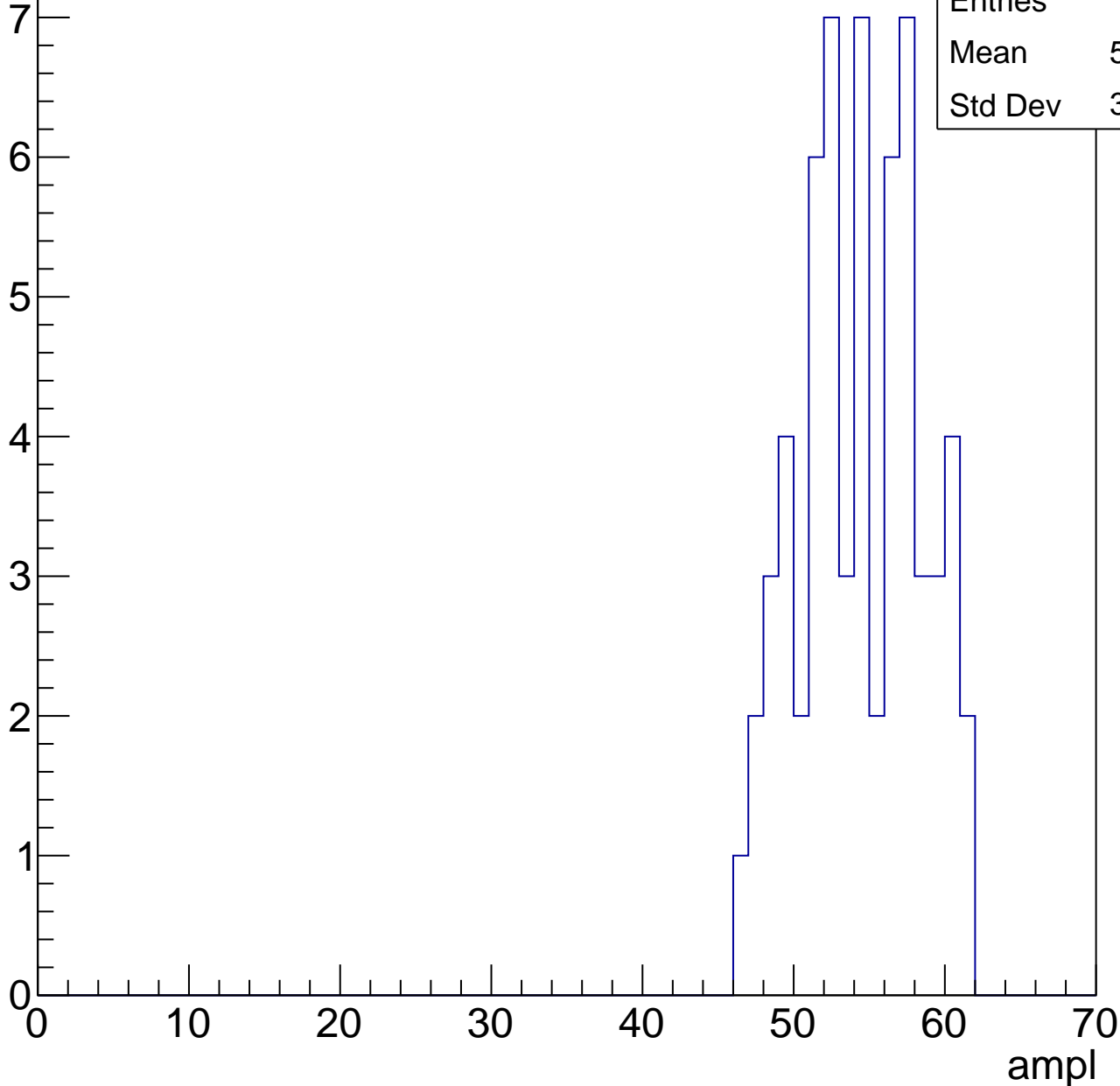


# B1L003S, U18-ch41, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	62
Mean	53.95
Std Dev	3.896



# B1L003S, U18-ch41, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	58
Mean	58.34
Std Dev	8.187

Entry

10

8

6

4

2

0

0

10

20

30

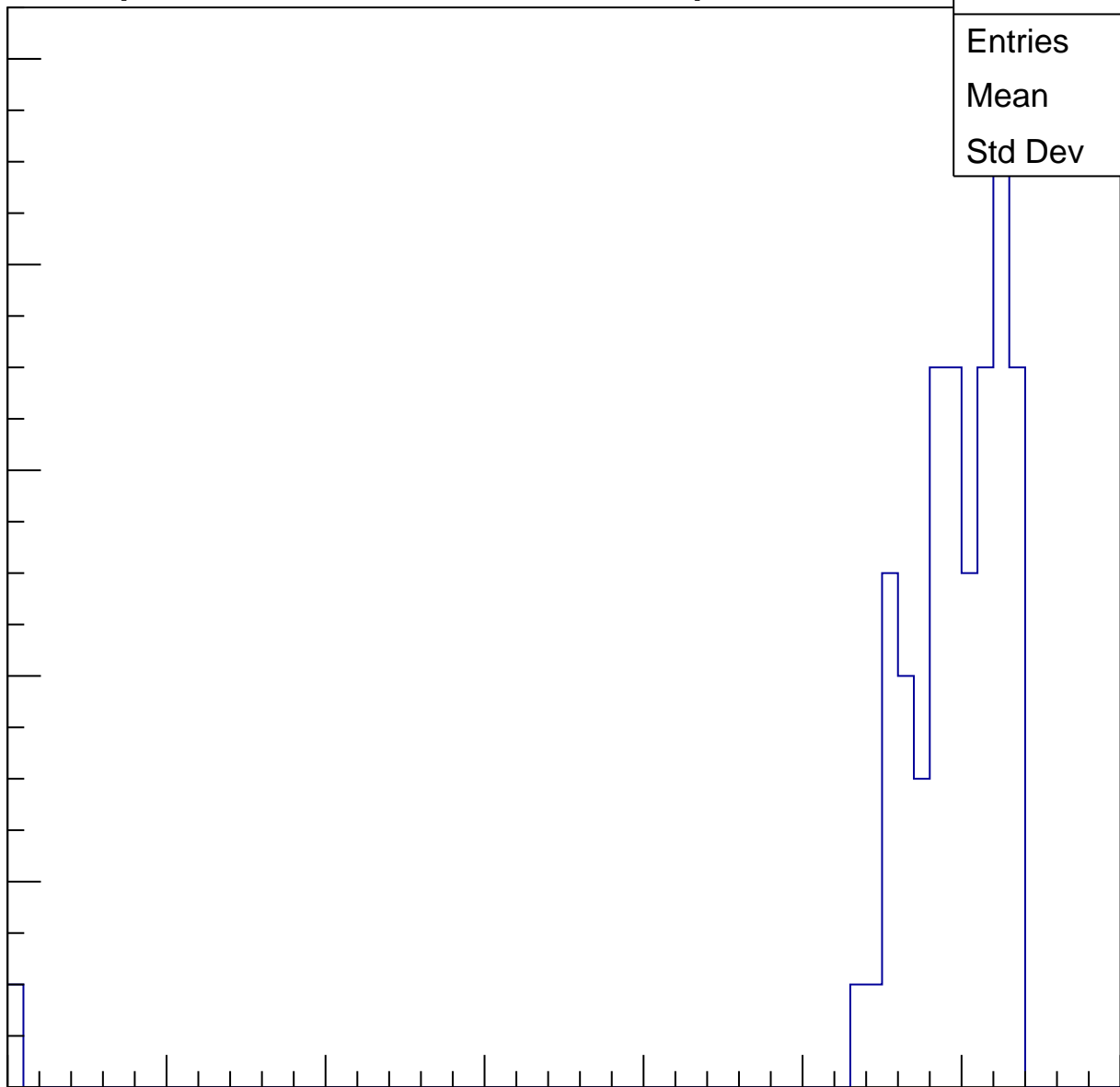
40

50

60

70

ampl



# B1L003S, U18-ch41, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U18-ch41, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch42, adc0

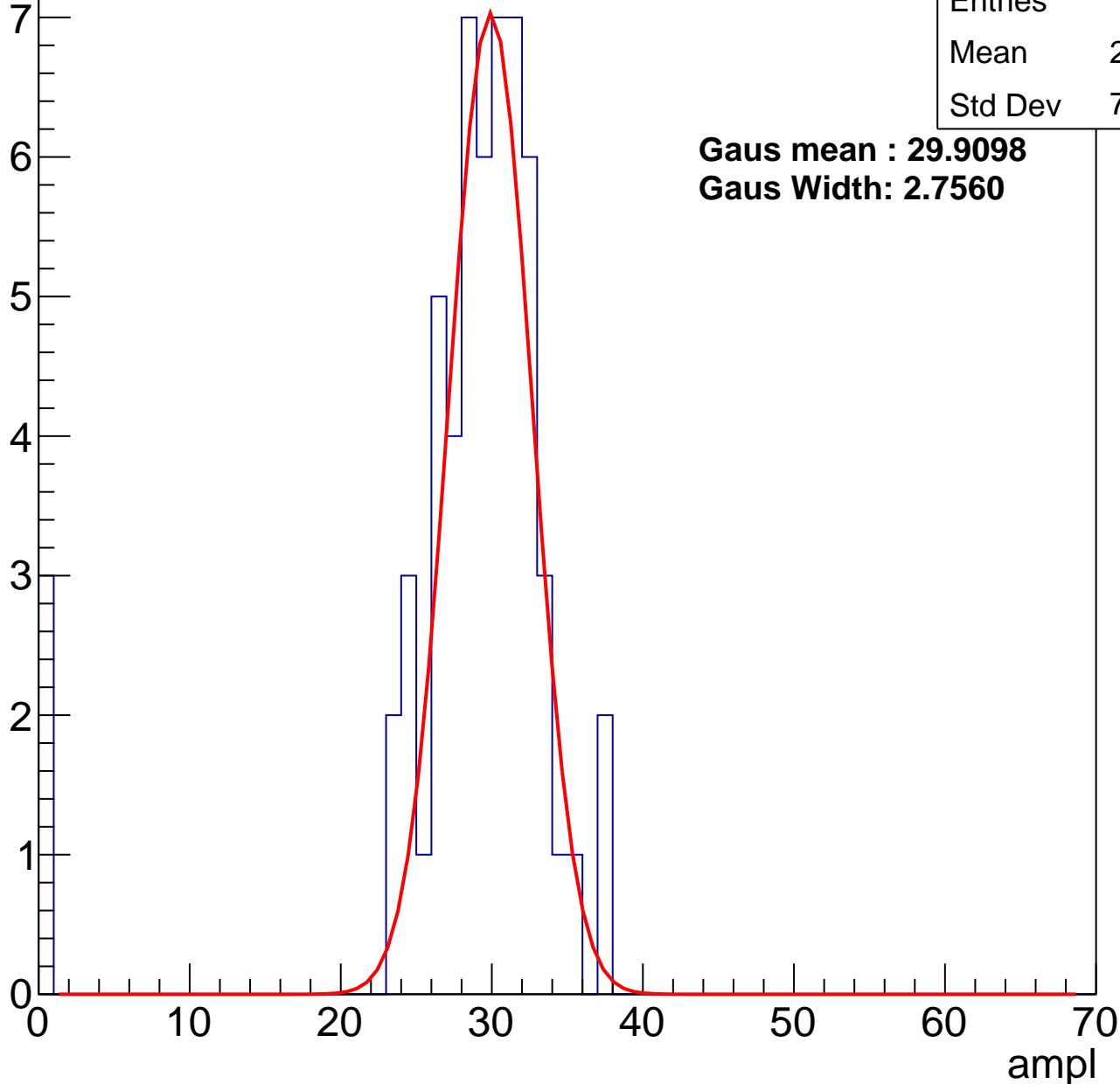
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	58
Mean	27.79
Std Dev	7.187

**Gaus mean : 29.9098**

**Gaus Width: 2.7560**



# B1L003S, U18-ch42, adc1

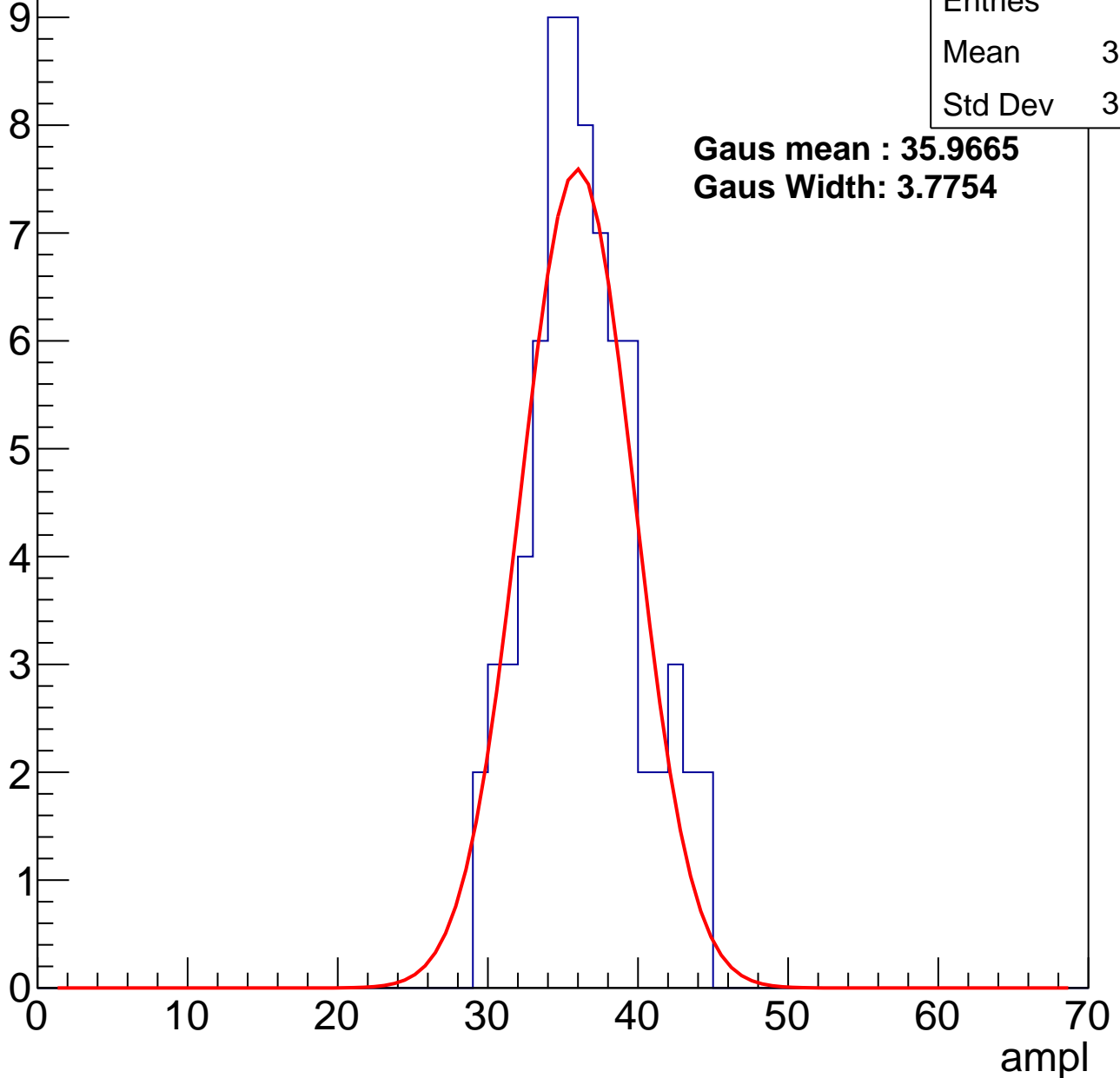
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	74
Mean	35.93
Std Dev	3.573

**Gaus mean : 35.9665**

**Gaus Width: 3.7754**



# B1L003S, U18-ch42, adc2

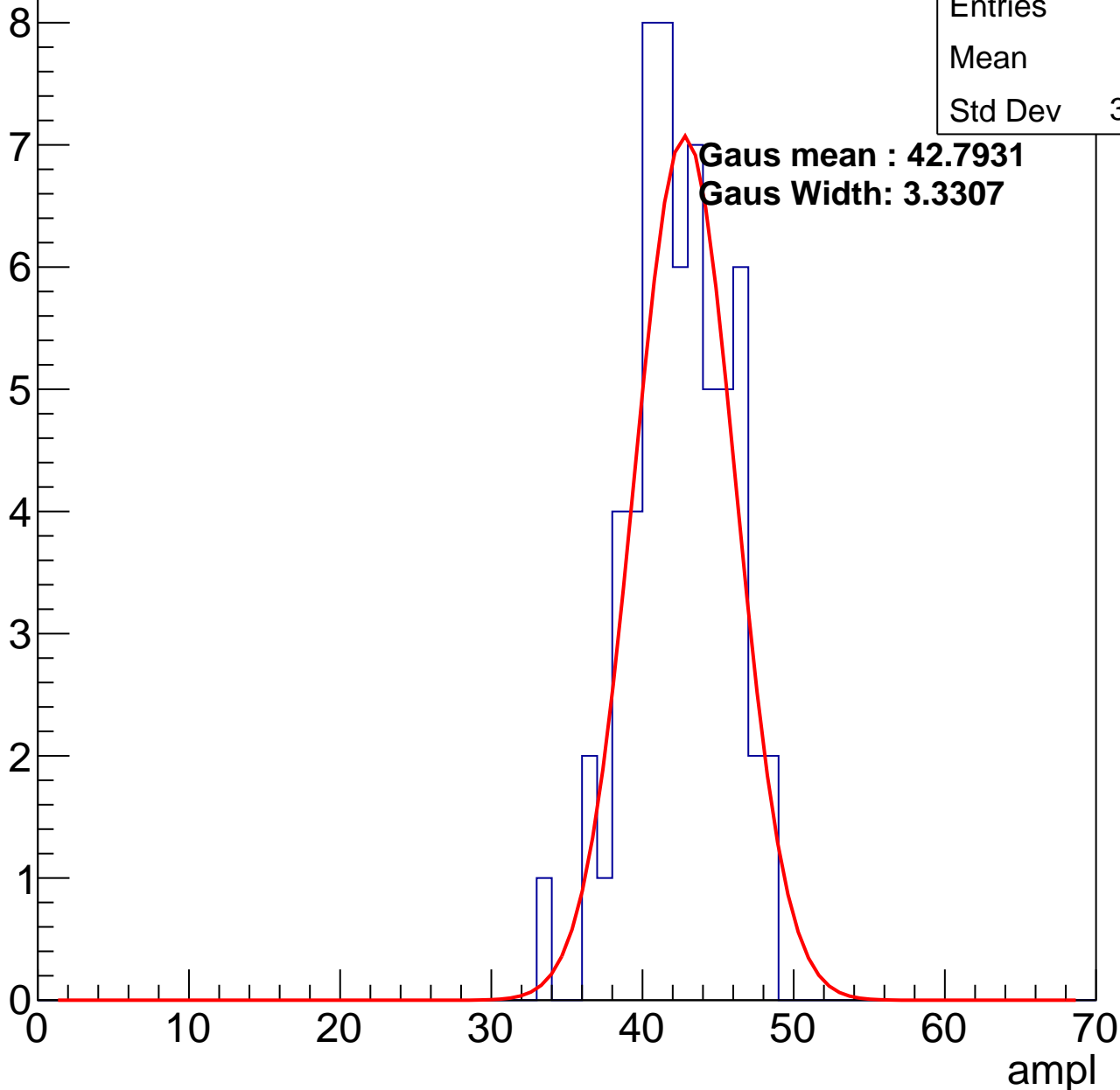
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	61
Mean	42
Std Dev	3.157

**Gaus mean : 42.7931**

**Gaus Width: 3.3307**

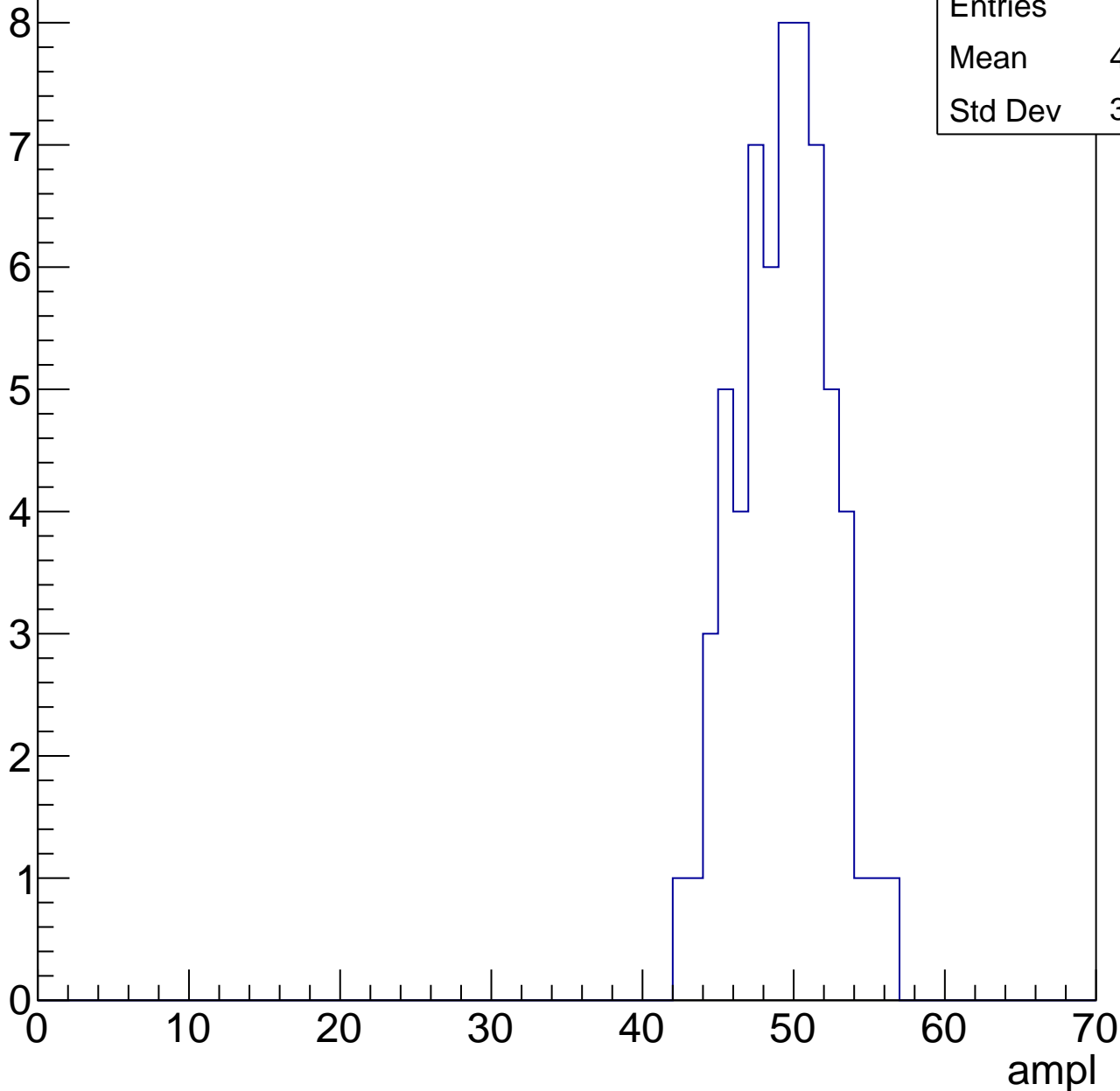


# B1L003S, U18-ch42, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

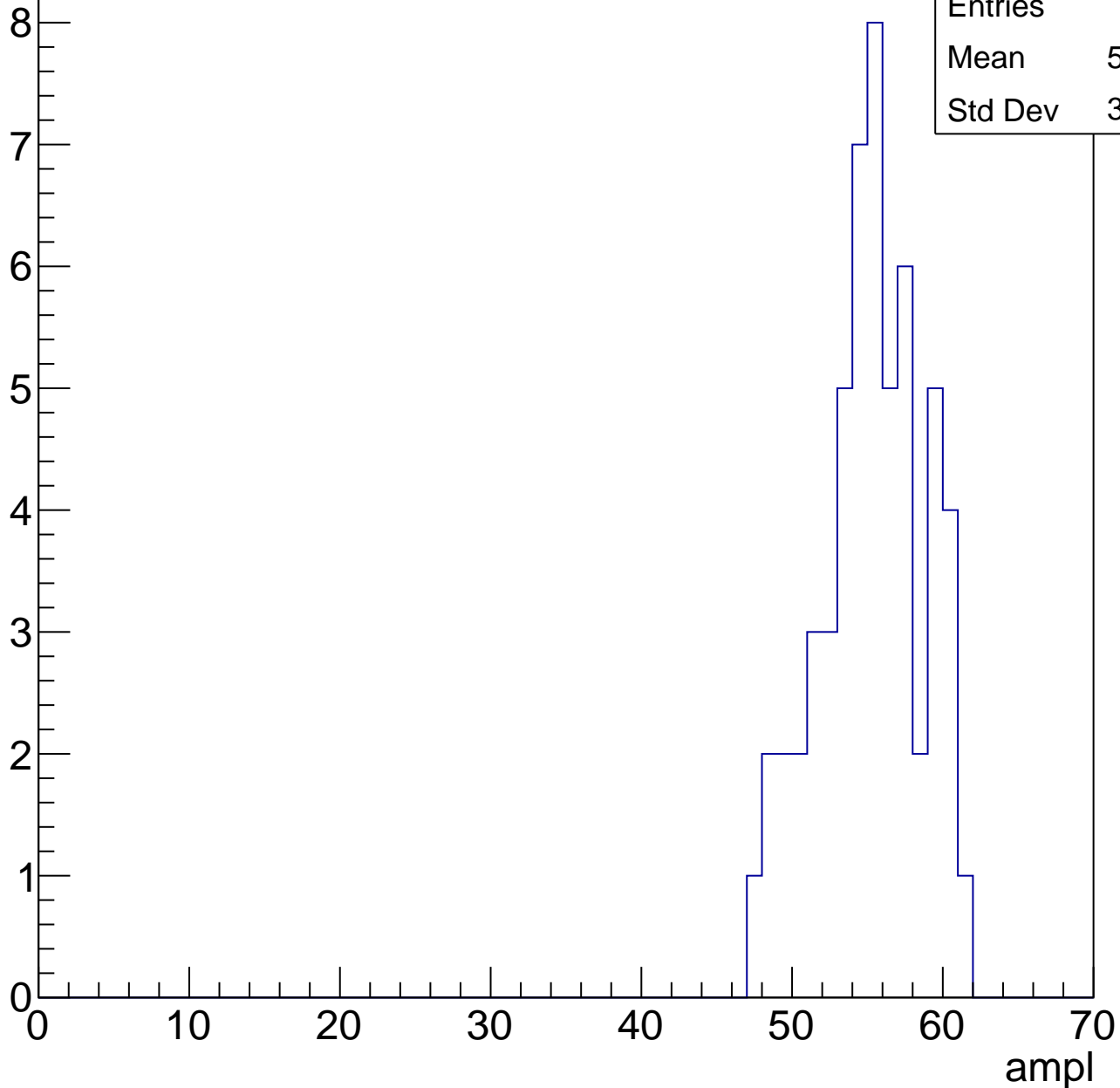
Entries	62
Mean	48.85
Std Dev	3.015



# B1L003S, U18-ch42, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

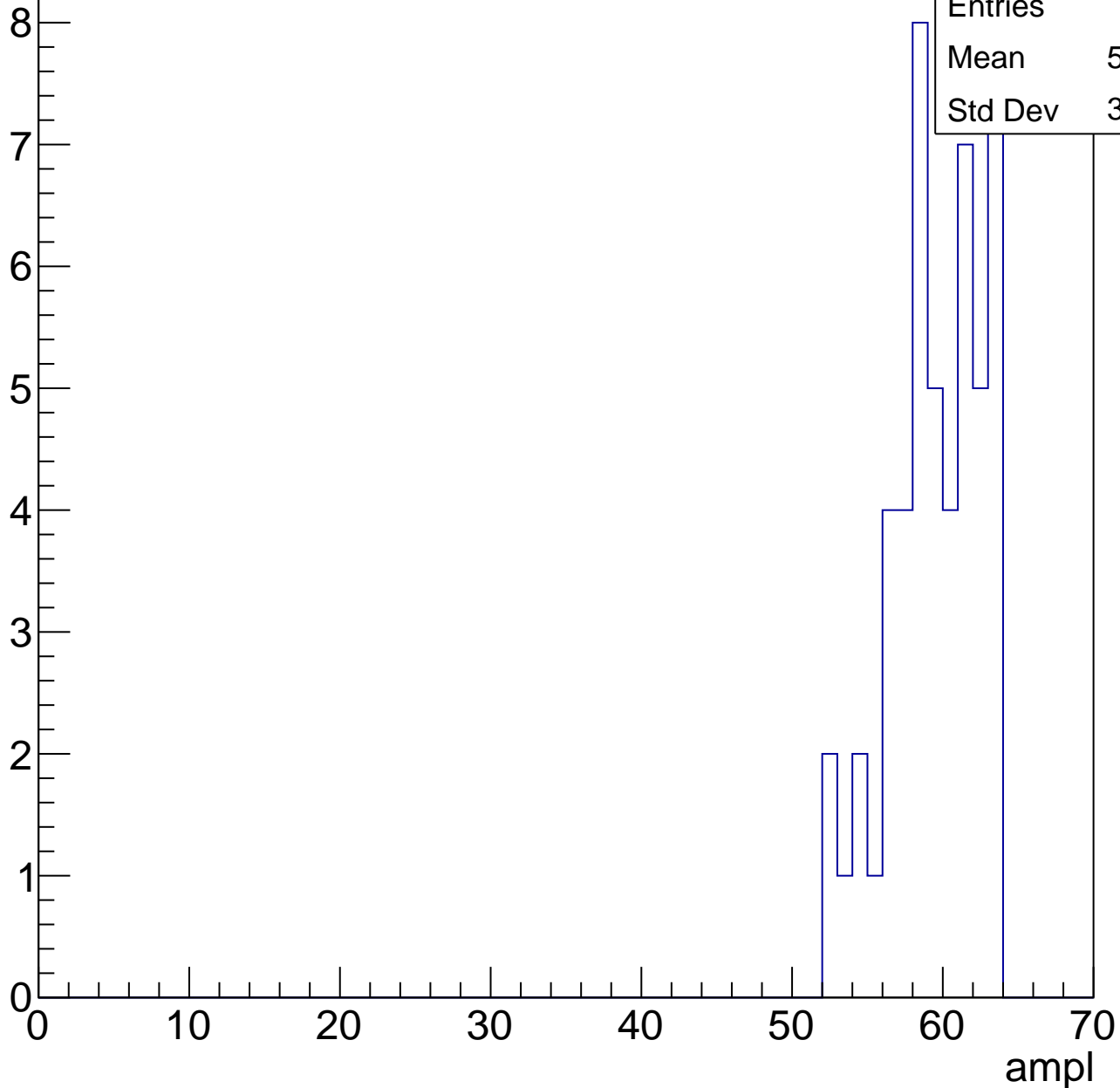
Entry



# B1L003S, U18-ch42, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

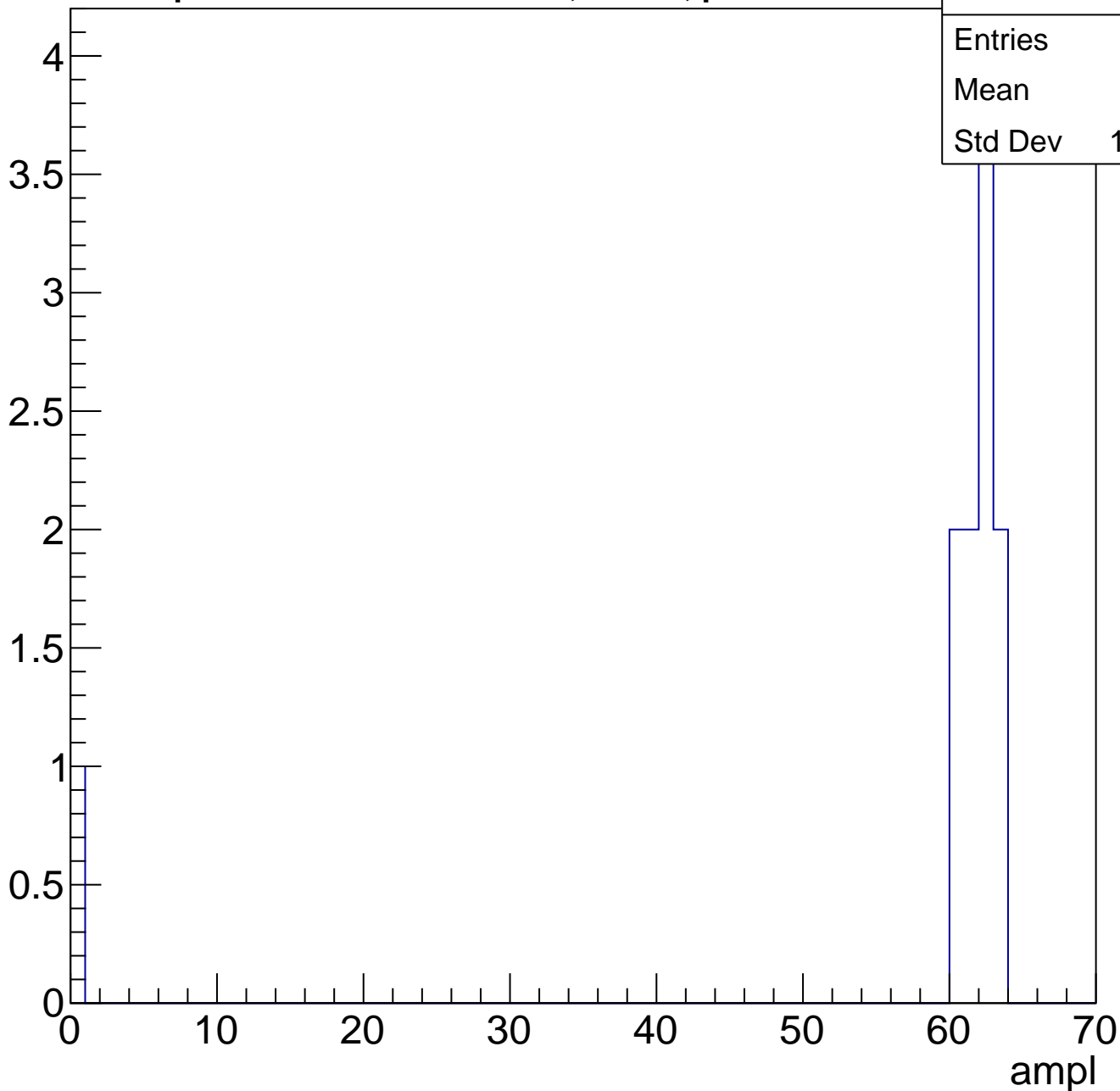
Entry



# B1L003S, U18-ch42, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



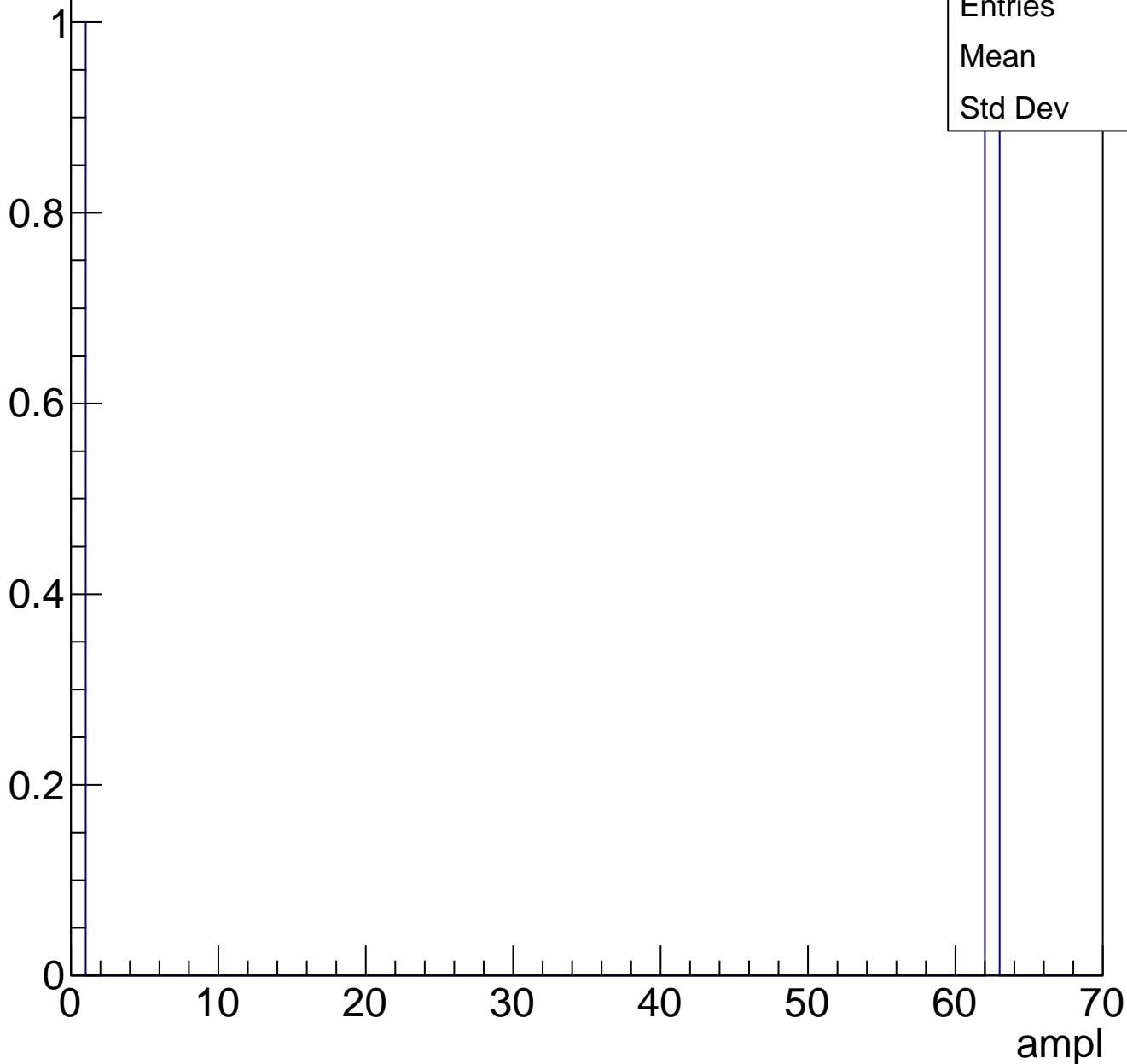
Entries	11
Mean	56
Std Dev	17.74



# B1L003S, U18-ch42, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	2
Mean	31
Std Dev	31

# B1L003S, U18-ch43, adc0

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	82
Mean	28.39
Std Dev	3.502

**Gaus mean : 28.4283**

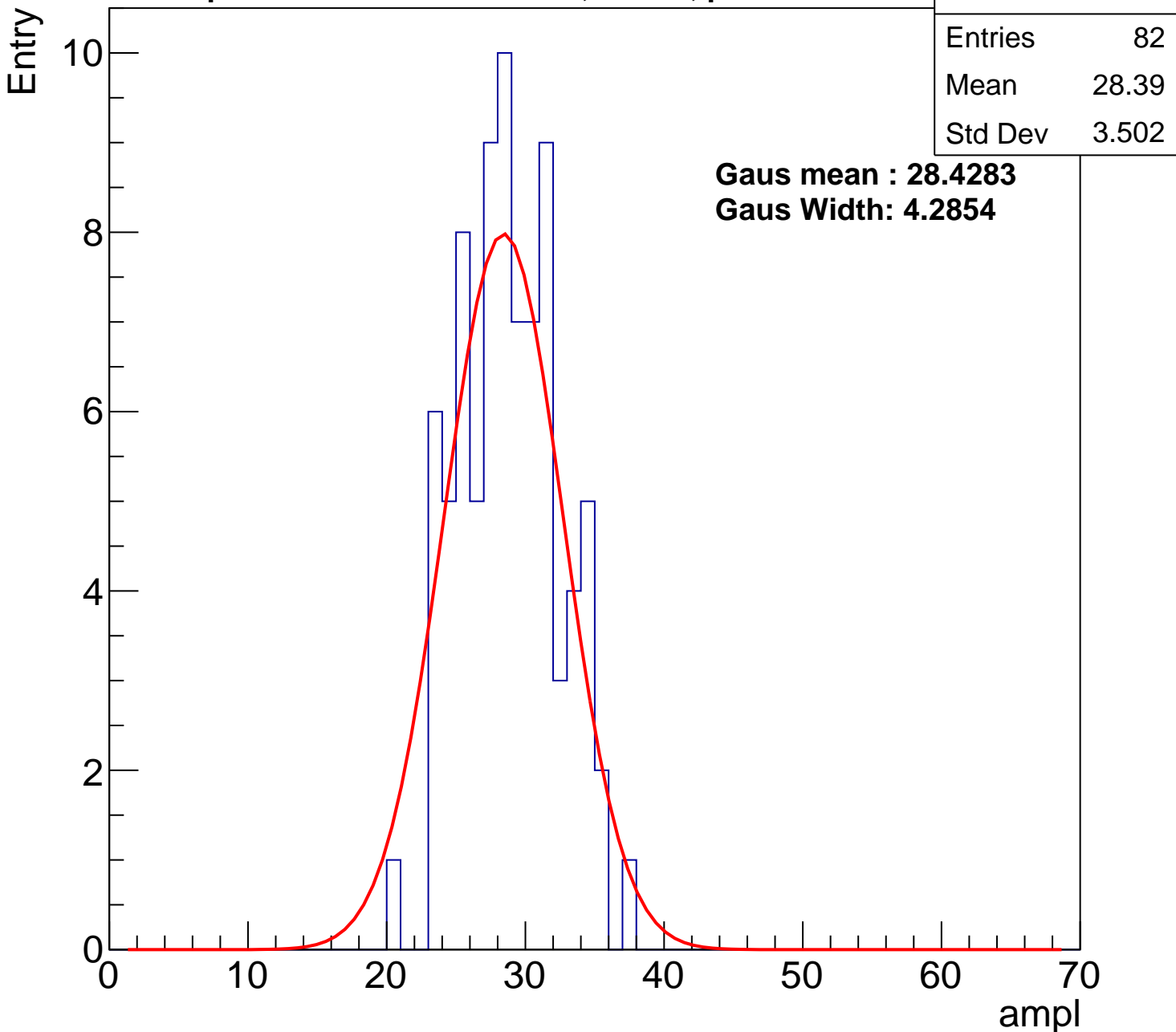
**Gaus Width: 4.2854**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



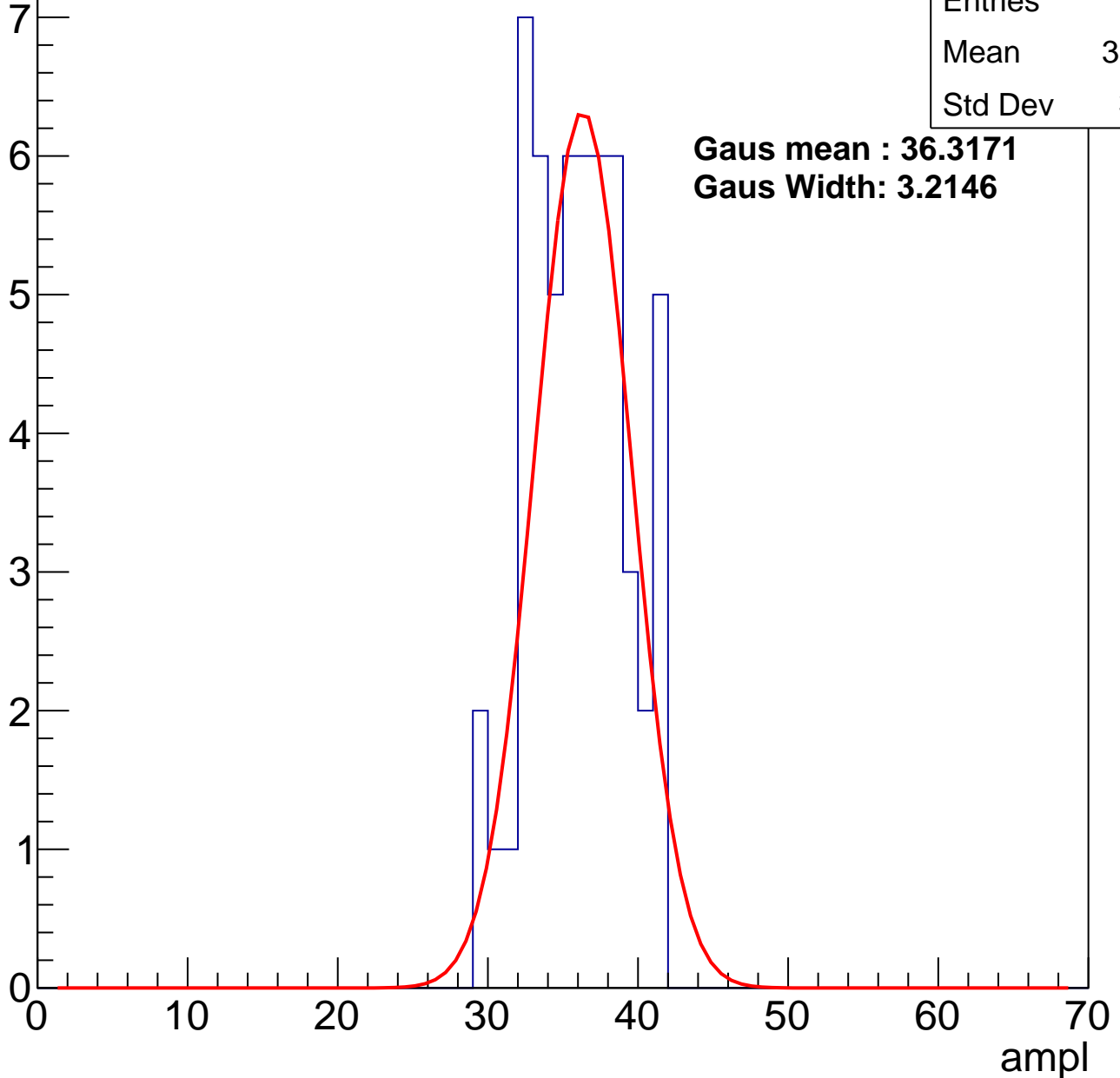
# B1L003S, U18-ch43, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	56
Mean	35.52
Std Dev	3.14

**Gaus mean : 36.3171**  
**Gaus Width: 3.2146**



# B1L003S, U18-ch43, adc2

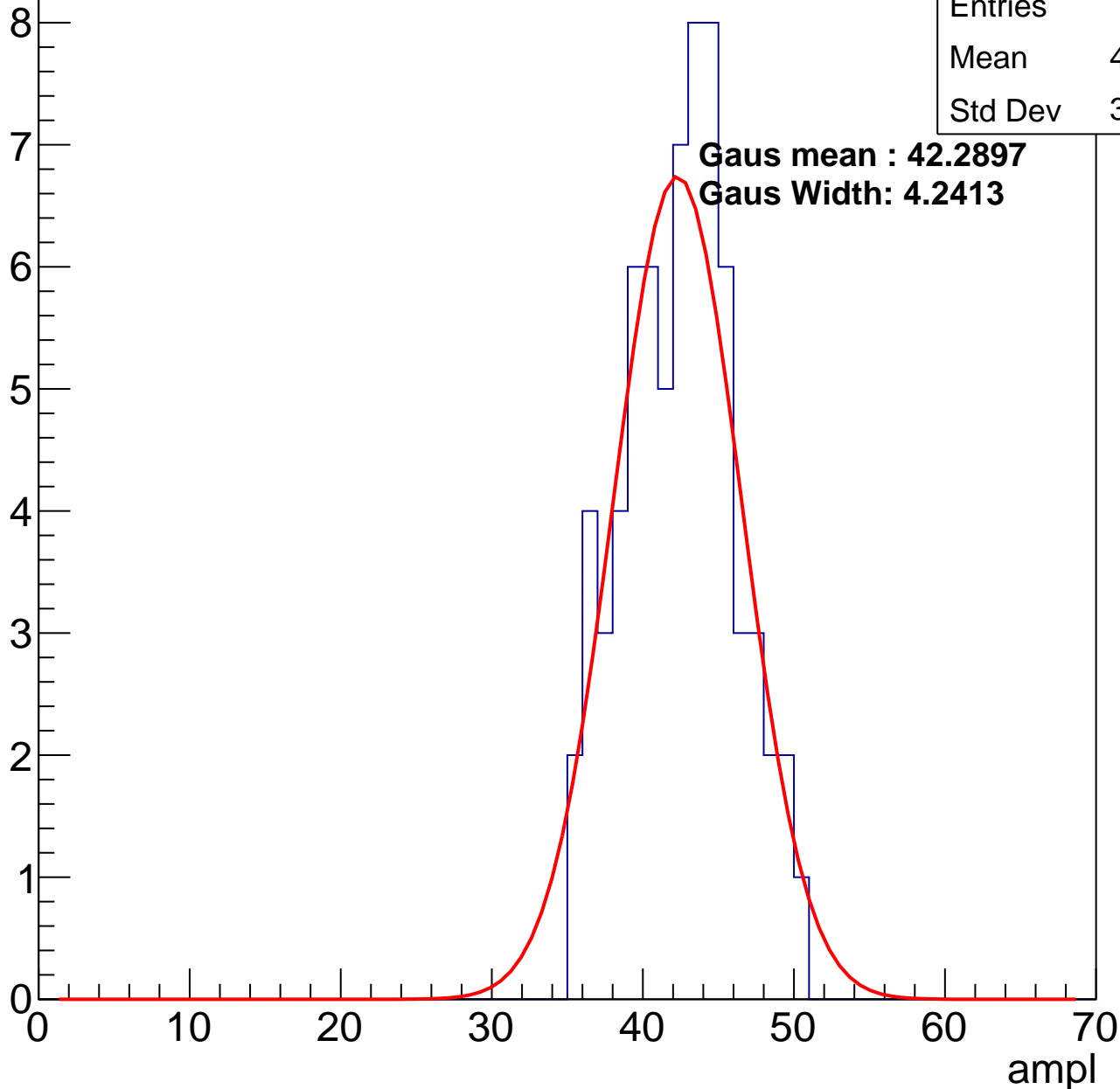
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	70
Mean	41.99
Std Dev	3.615

**Gaus mean : 42.2897**

**Gaus Width: 4.2413**

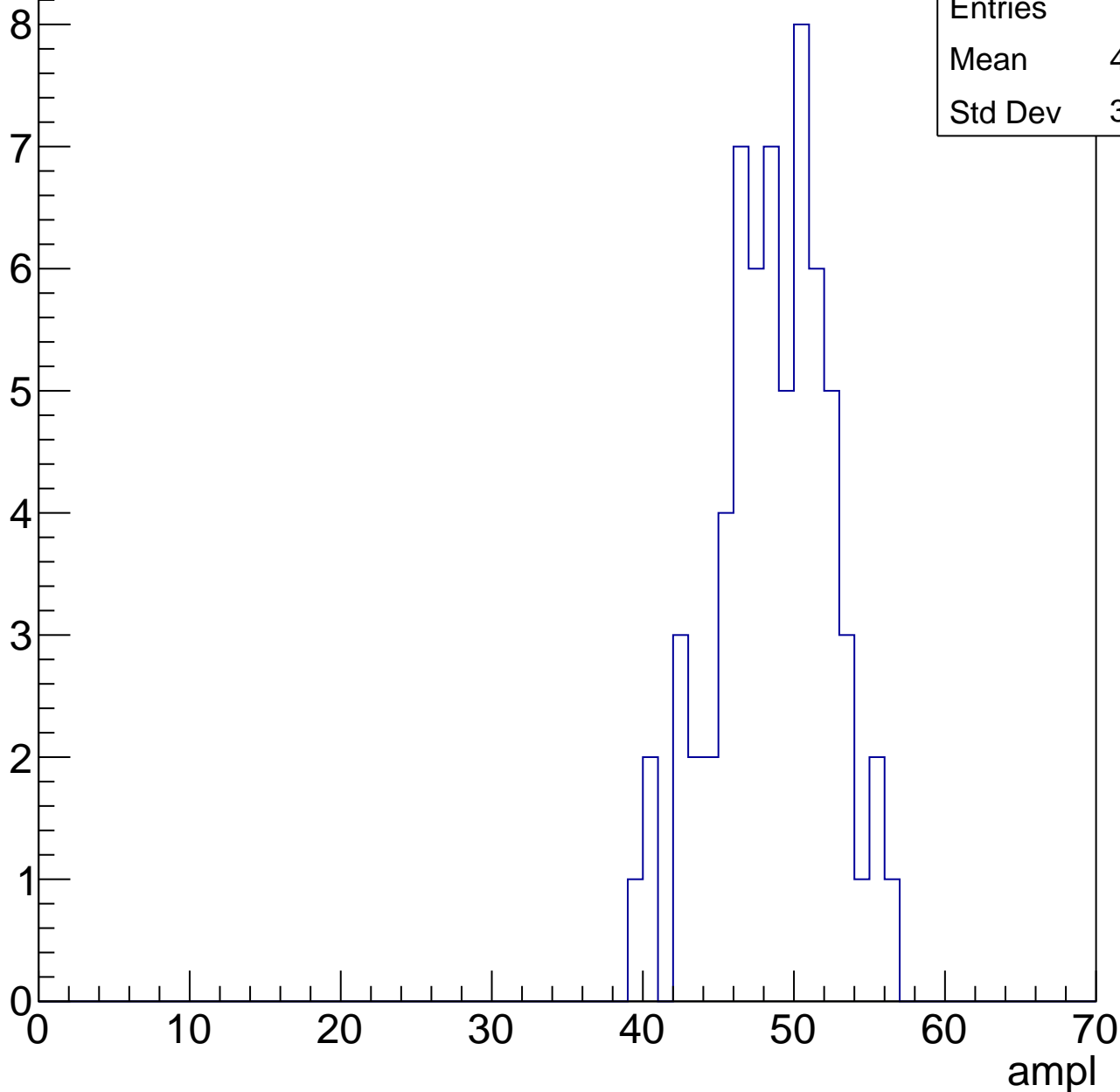


# B1L003S, U18-ch43, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	65
Mean	48.14
Std Dev	3.745

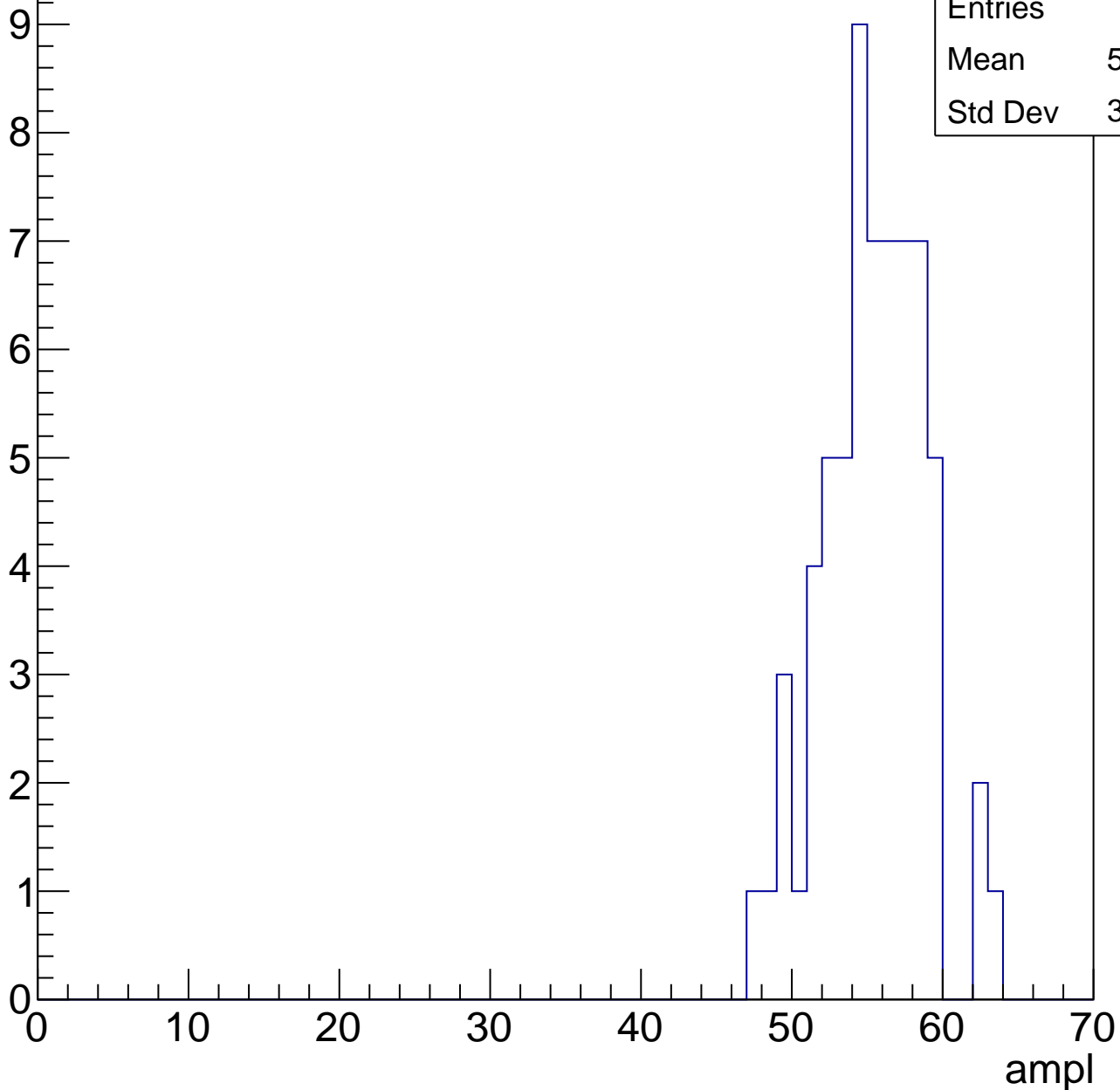


# B1L003S, U18-ch43, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	65
Mean	54.94
Std Dev	3.337

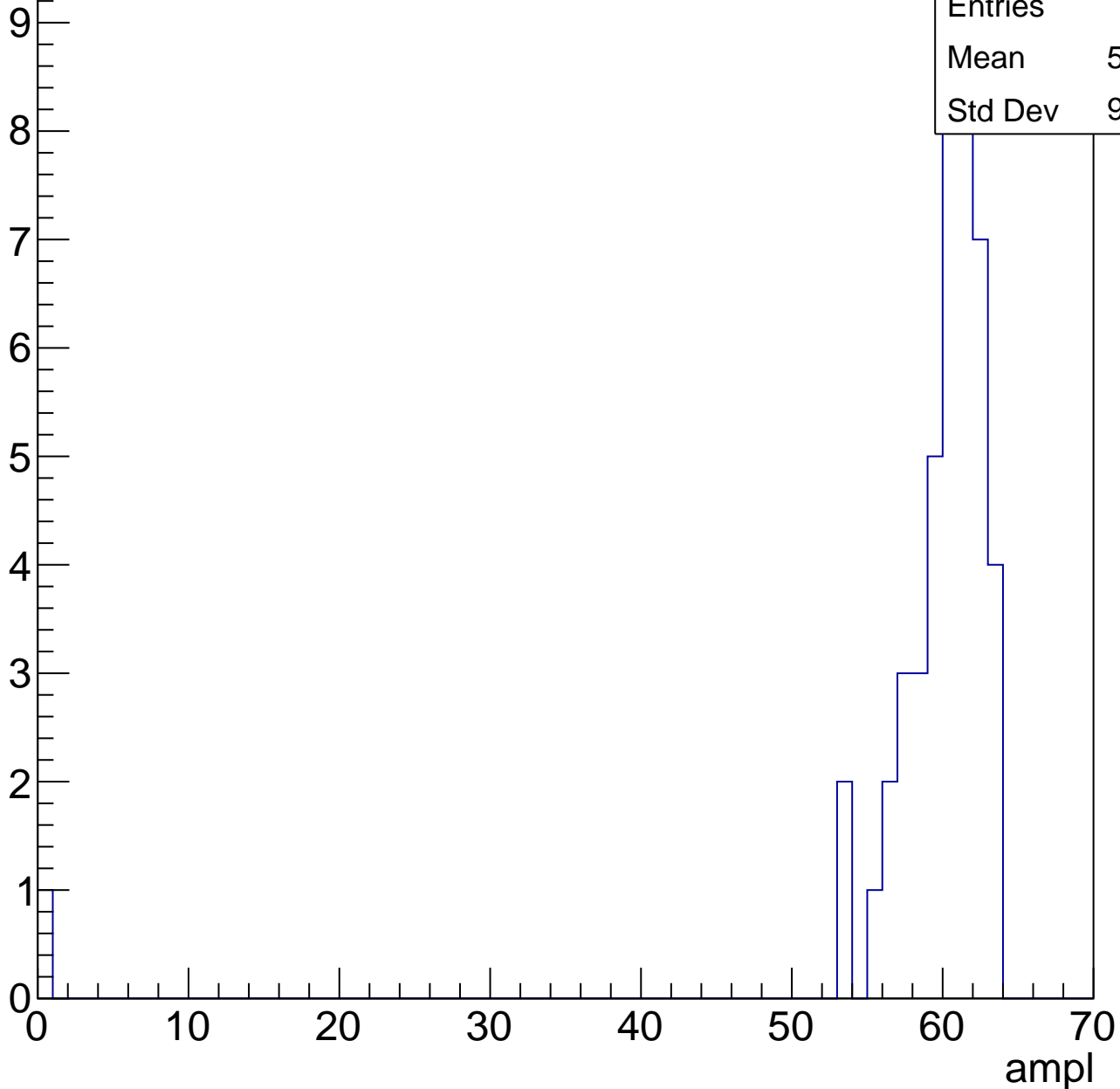


# B1L003S, U18-ch43, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	45
Mean	58.38
Std Dev	9.132

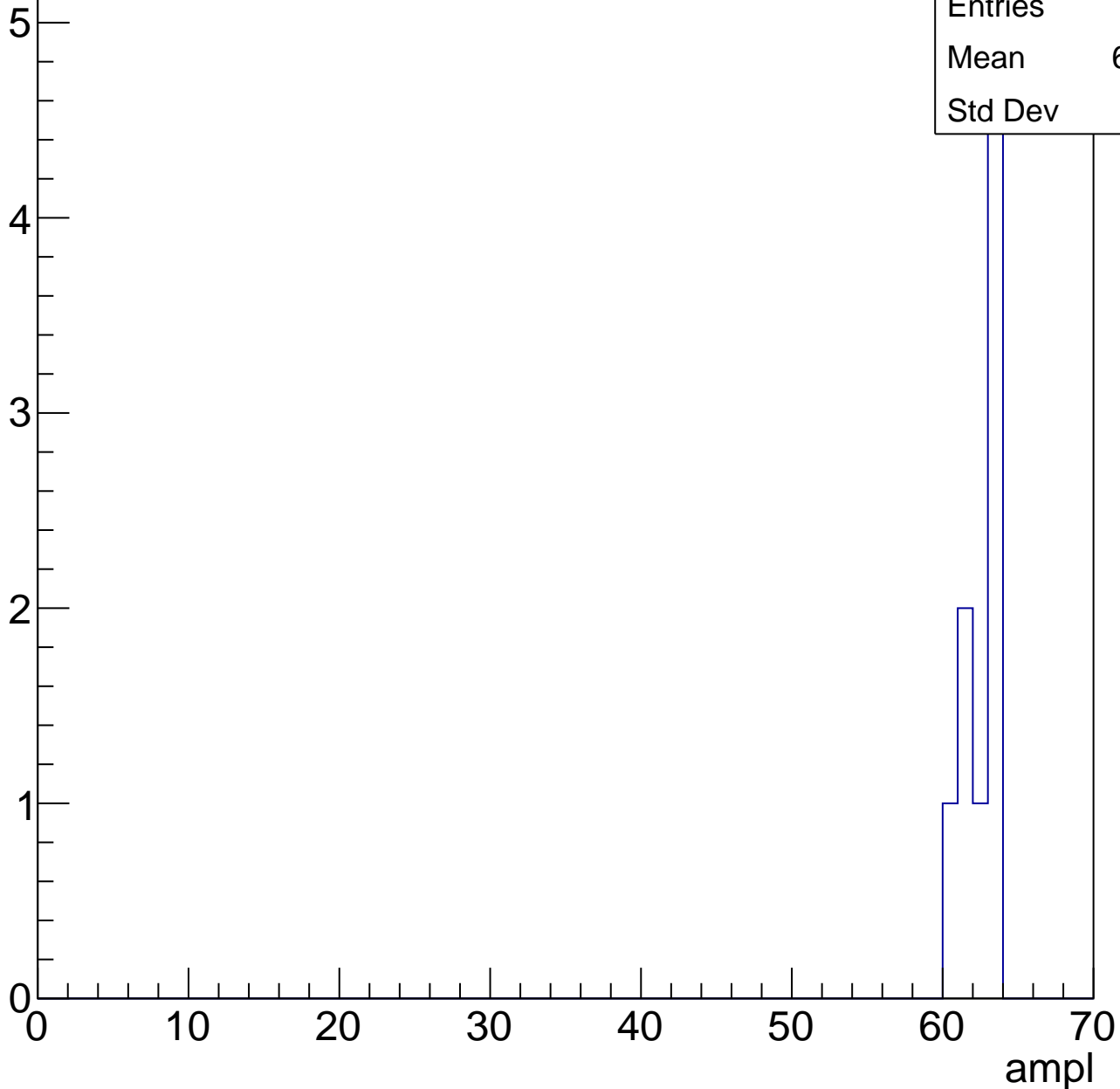


# B1L003S, U18-ch43, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	9
Mean	62.11
Std Dev	1.1





# B1L003S, U18-ch43, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	3
Mean	6
Std Dev	8.485

# B1L003S, U18-ch44, adc0

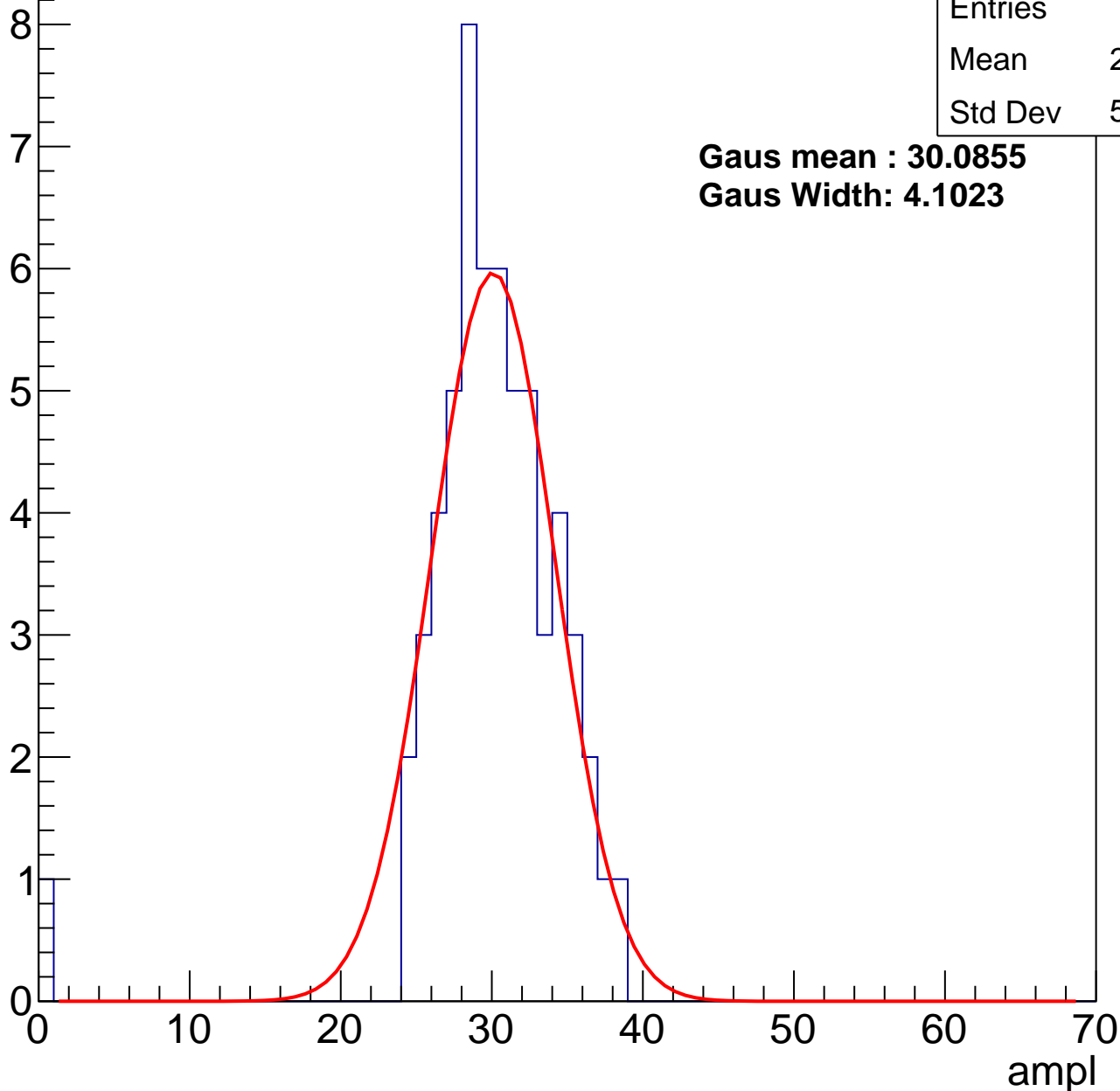
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	59
Mean	29.53
Std Dev	5.137

**Gaus mean : 30.0855**

**Gaus Width: 4.1023**



# B1L003S, U18-ch44, adc1

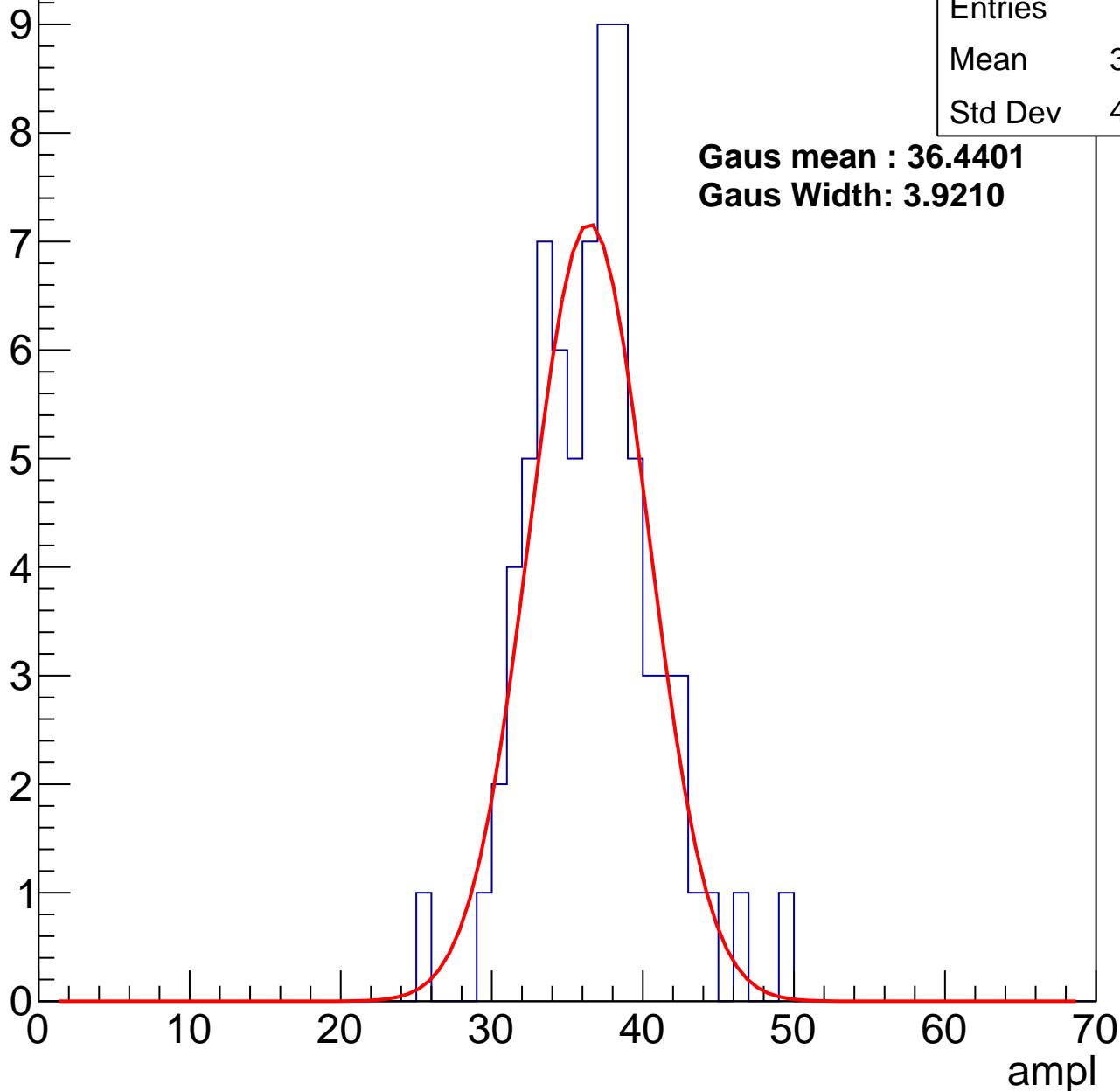
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	74
Mean	36.23
Std Dev	4.049

**Gaus mean : 36.4401**

**Gaus Width: 3.9210**



# B1L003S, U18-ch44, adc2

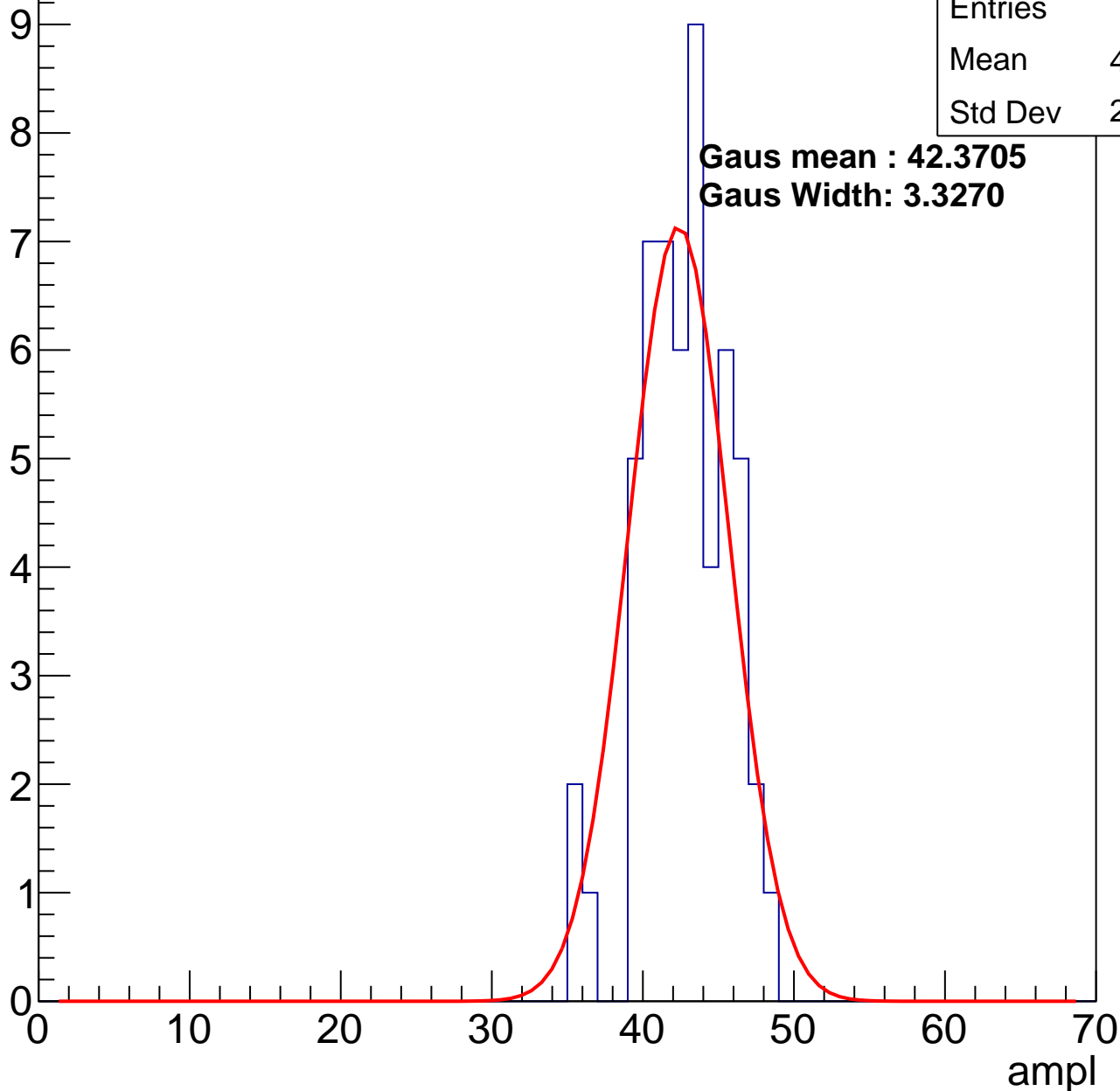
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	55
Mean	42.27
Std Dev	2.876

**Gaus mean : 42.3705**

**Gaus Width: 3.3270**

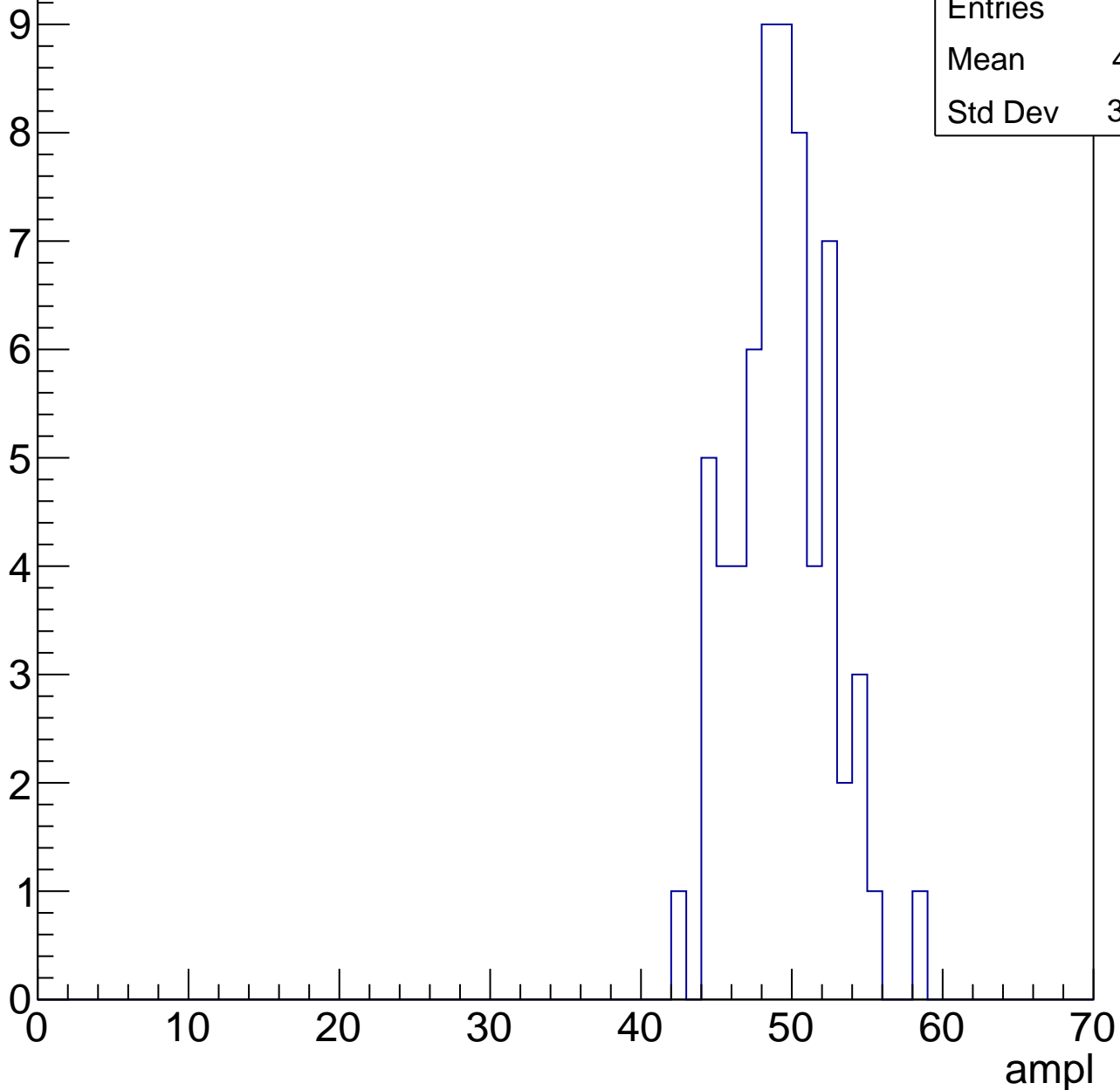


# B1L003S, U18-ch44, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	64
Mean	48.91
Std Dev	3.106

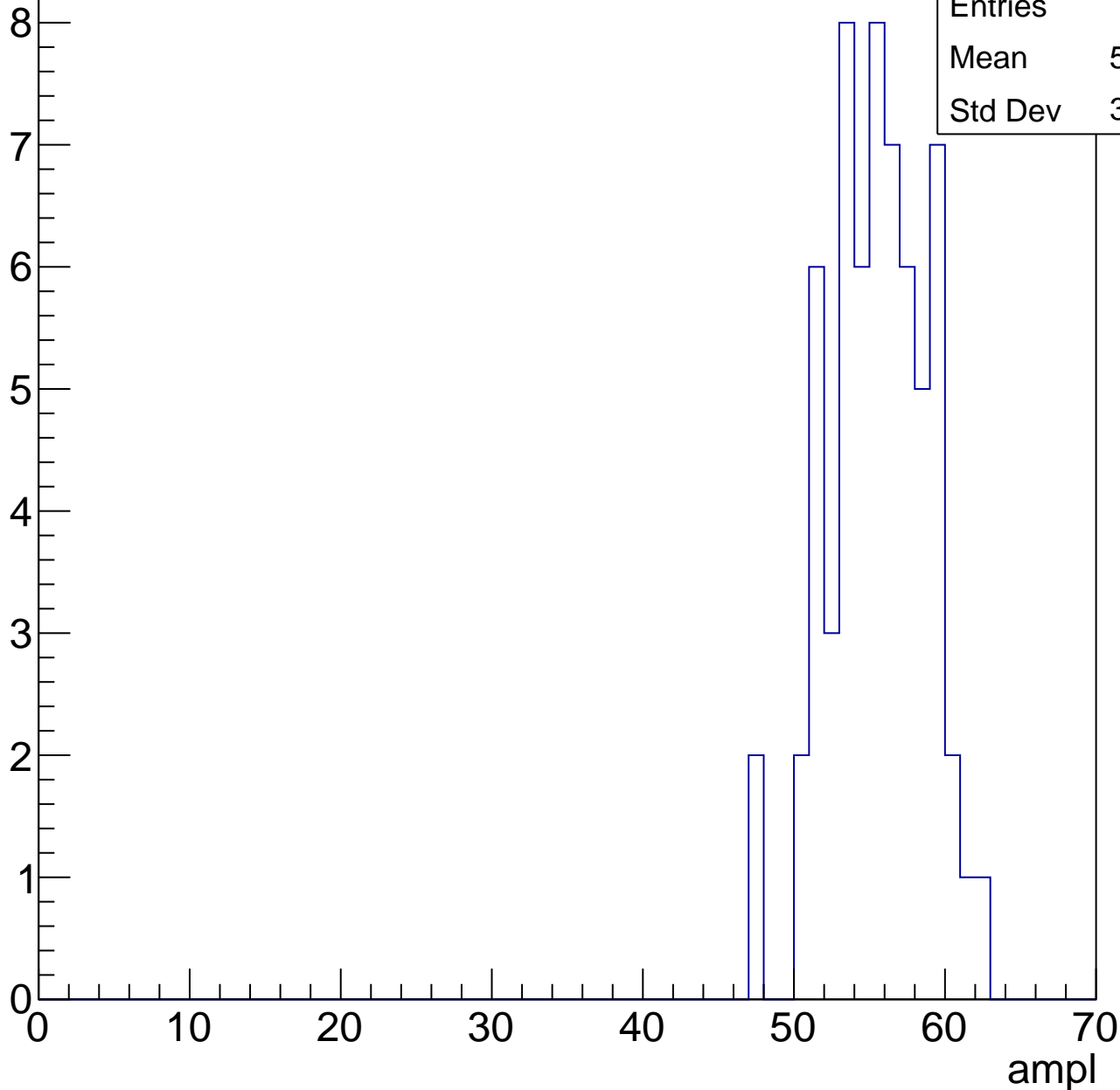


# B1L003S, U18-ch44, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	64
Mean	55.06
Std Dev	3.216



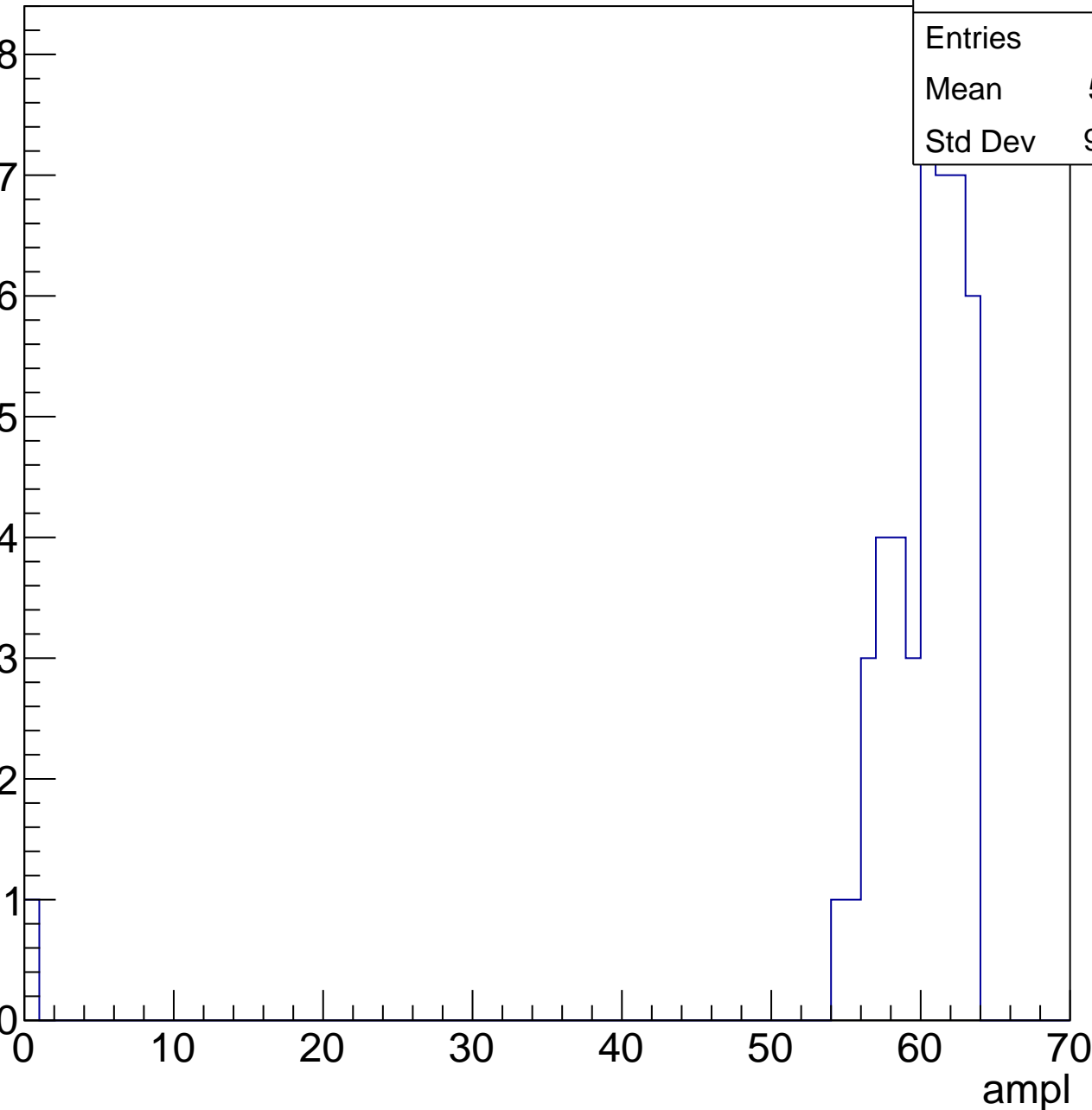
# B1L003S, U18-ch44, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	45
Mean	58.51
Std Dev	9.133

8  
7  
6  
5  
4  
3  
2  
1  
0



# B1L003S, U18-ch44, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U18-ch44, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L003S, U18-ch45, adc0

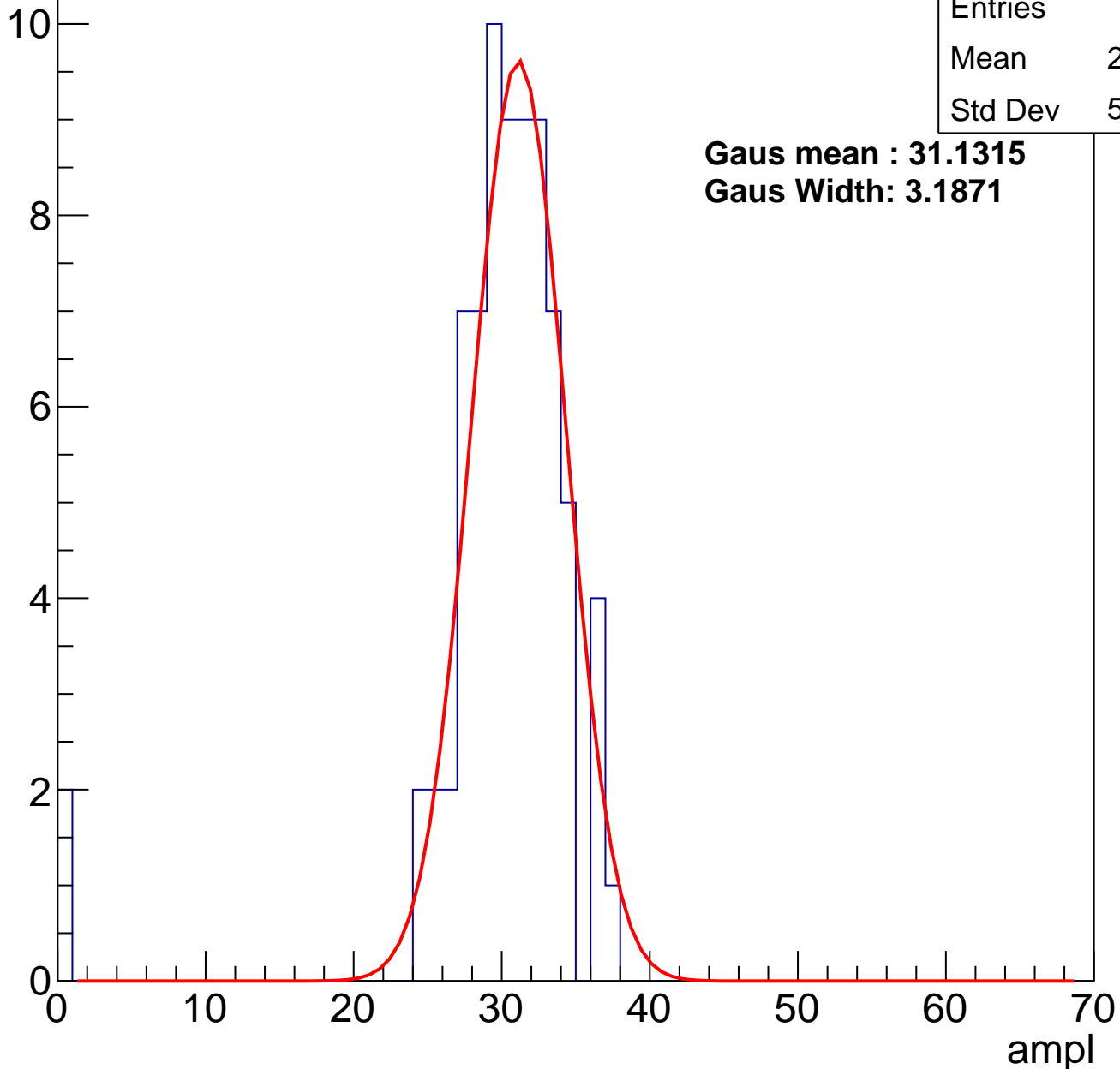
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	76
Mean	29.53
Std Dev	5.642

**Gaus mean : 31.1315**

**Gaus Width: 3.1871**

Entry



# B1L003S, U18-ch45, adc1

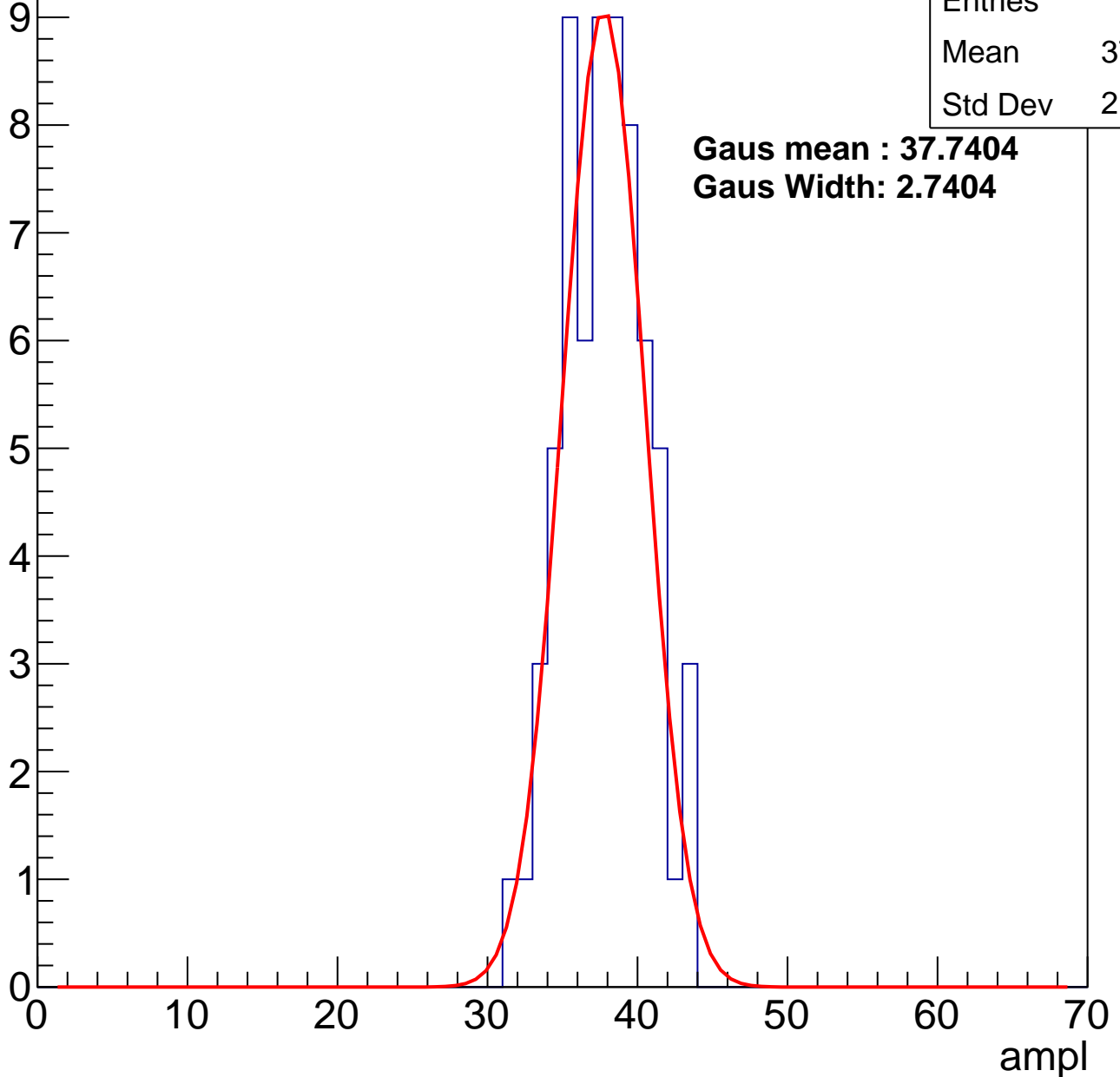
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	66
Mean	37.36
Std Dev	2.739

**Gaus mean : 37.7404**

**Gaus Width: 2.7404**



# B1L003S, U18-ch45, adc2

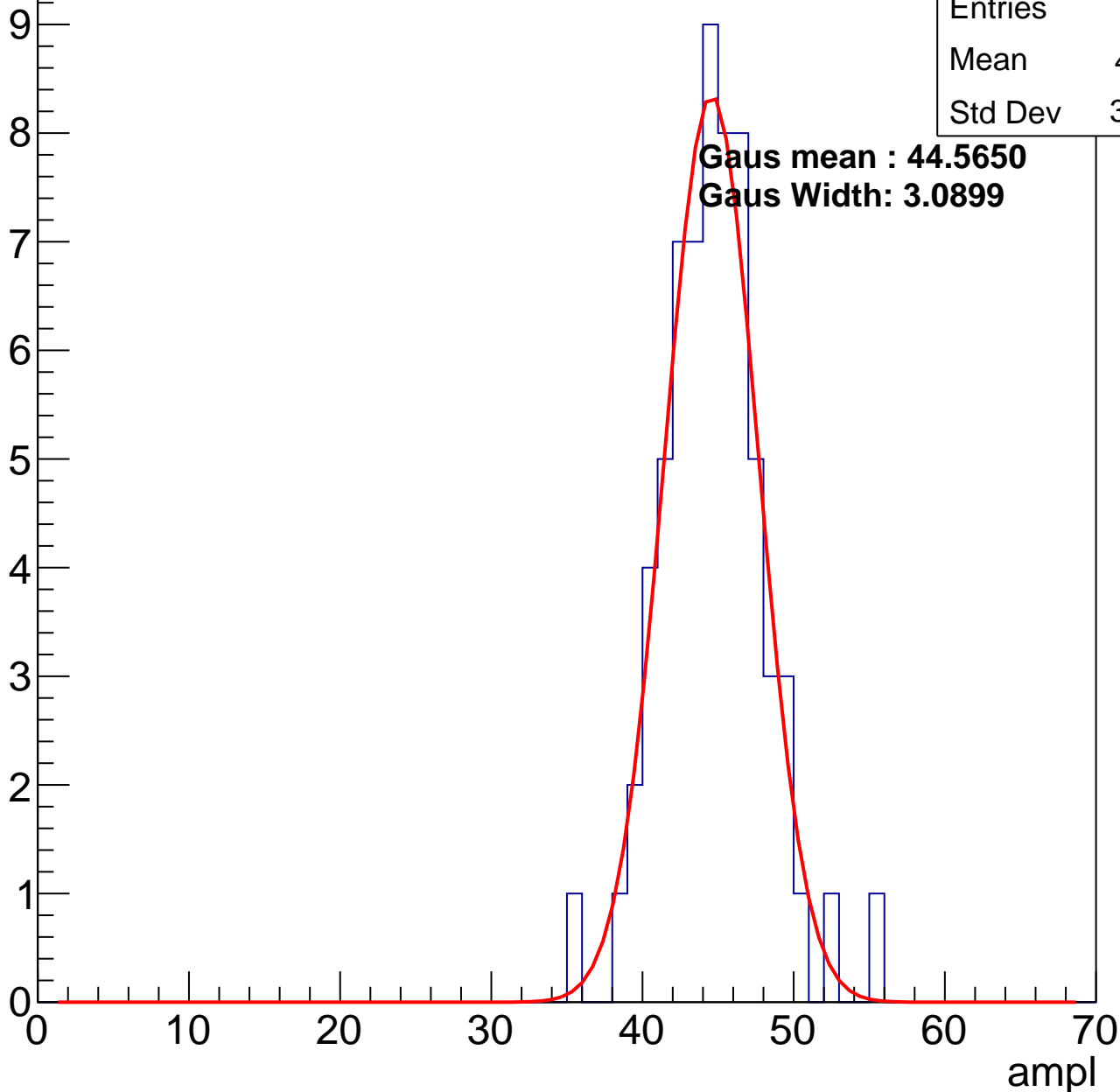
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	66
Mean	44.21
Std Dev	3.342

**Gaus mean : 44.5650**

**Gaus Width: 3.0899**

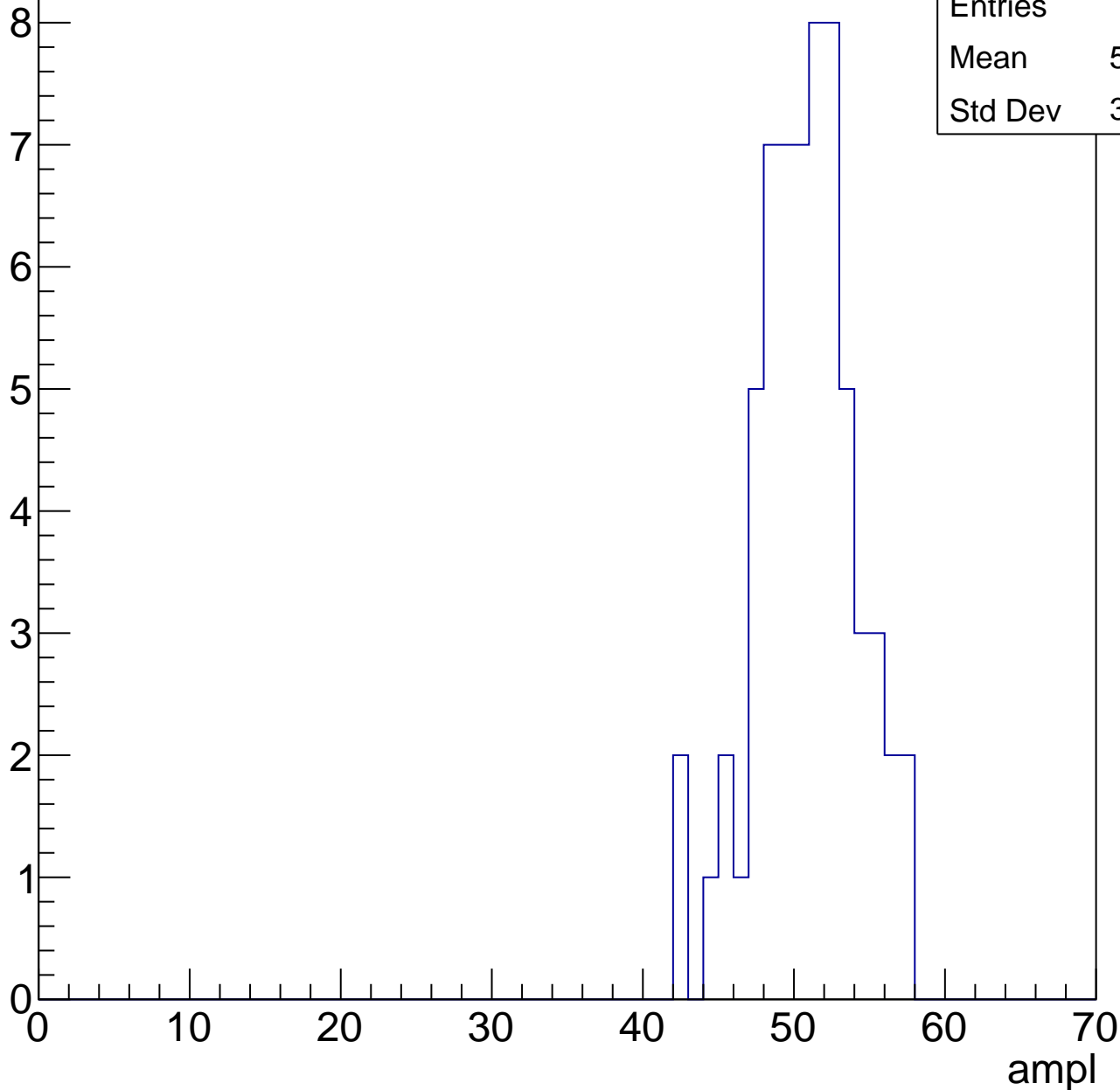


# B1L003S, U18-ch45, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	63
Mean	50.32
Std Dev	3.289

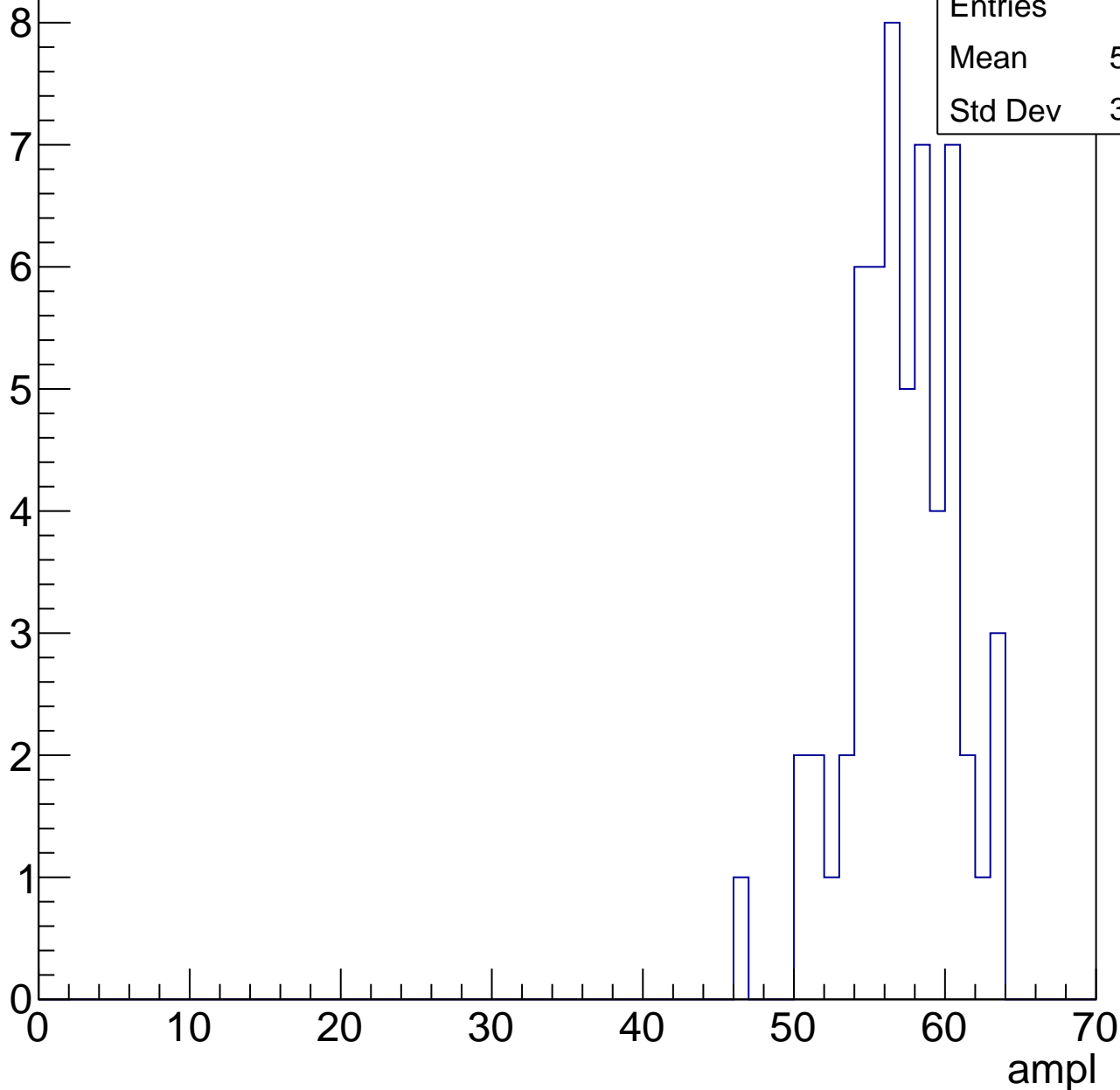


# B1L003S, U18-ch45, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	57
Mean	56.63
Std Dev	3.447

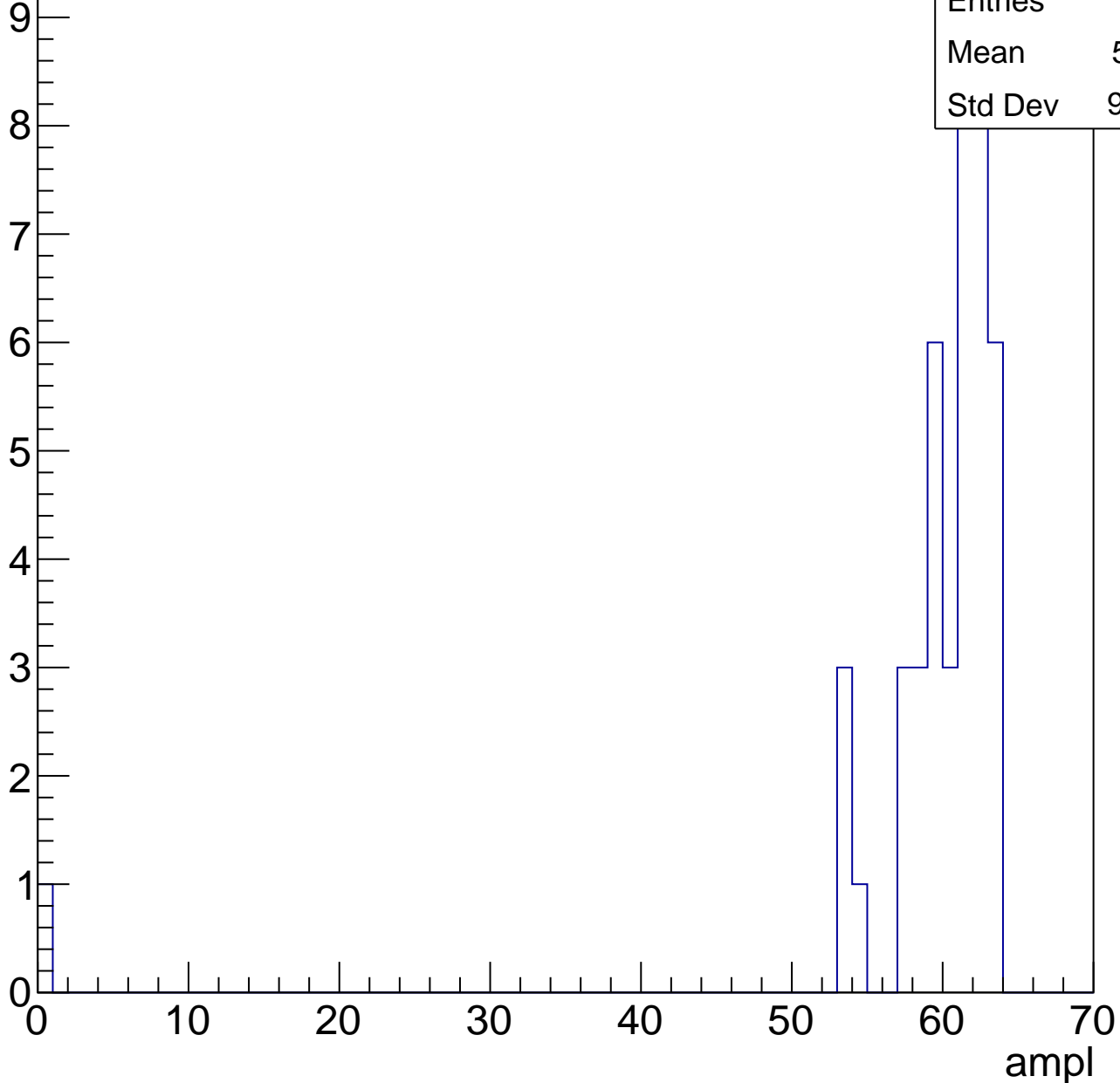


# B1L003S, U18-ch45, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	43
Mean	58.51
Std Dev	9.439



# B1L003S, U18-ch45, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

1

0.8

0.6

0.4

0.2

0

0

10

20

30

40

50

60

70

ampl

Entries

1

Mean

63

Std Dev

0



# B1L003S, U18-ch45, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U18-ch46, adc0

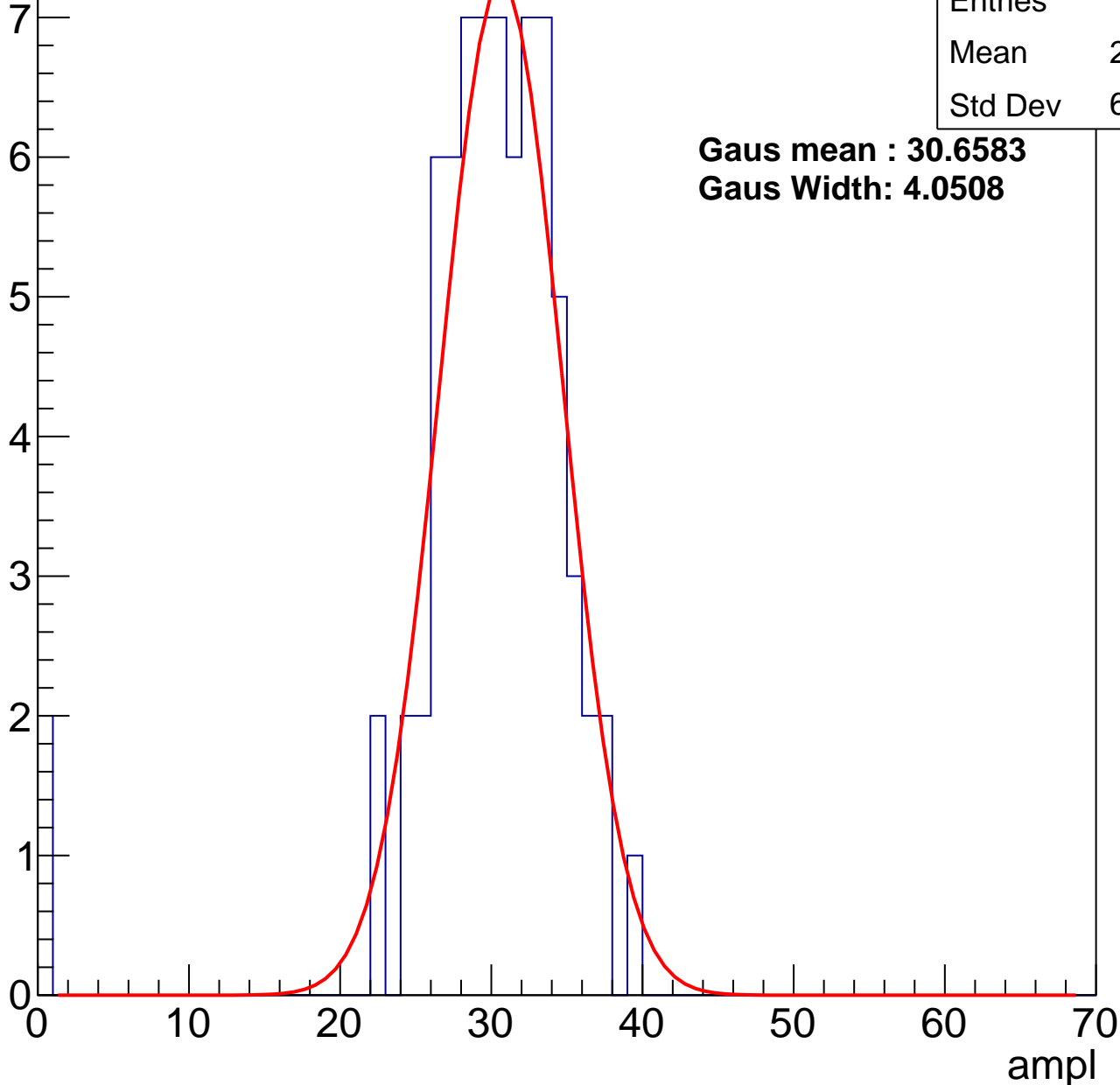
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	74
Mean	29.32
Std Dev	6.045

**Gaus mean : 30.6583**

**Gaus Width: 4.0508**



# B1L003S, U18-ch46, adc1

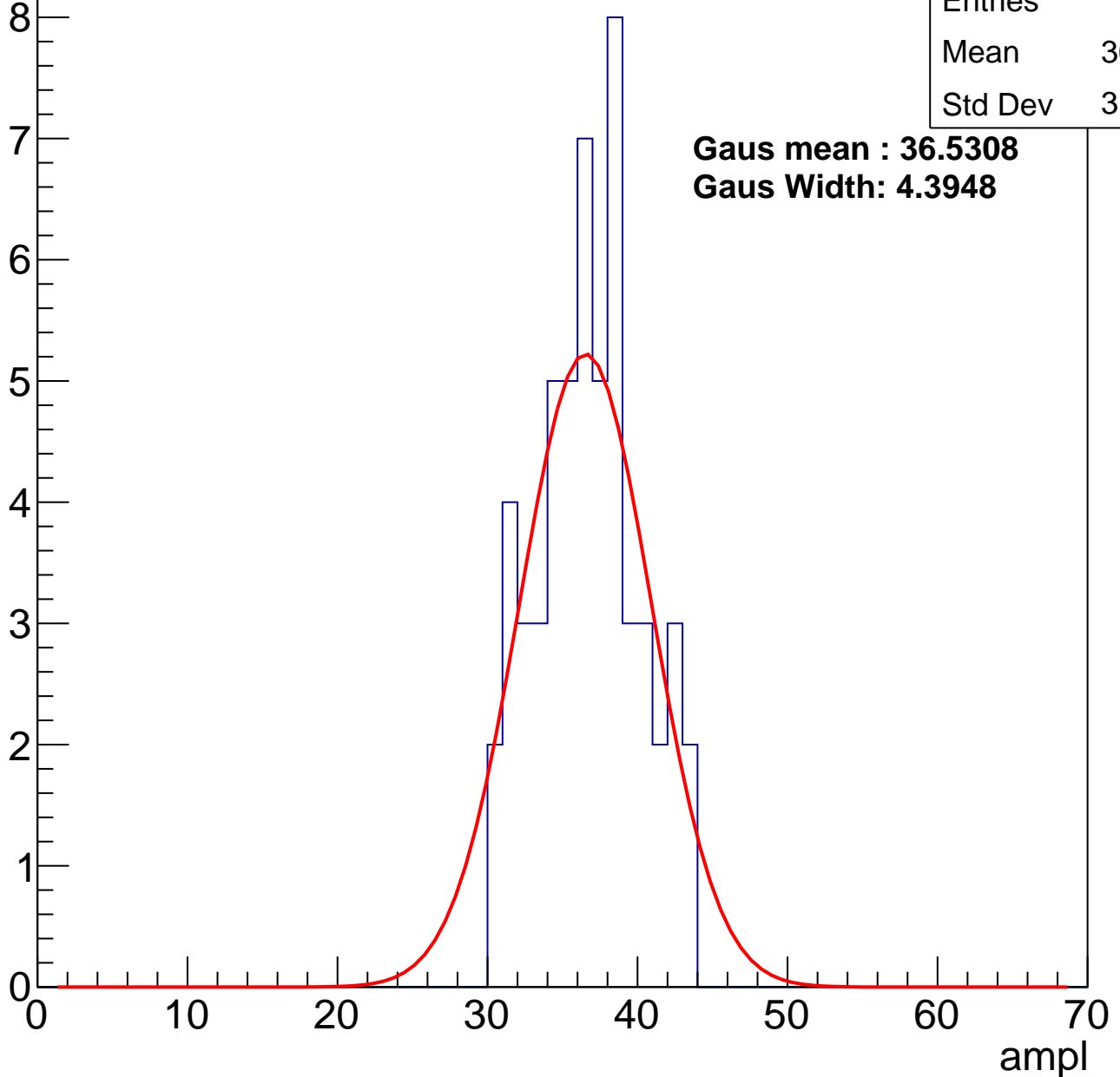
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	55
Mean	36.29
Std Dev	3.399

**Gaus mean : 36.5308**

**Gaus Width: 4.3948**



# B1L003S, U18-ch46, adc2

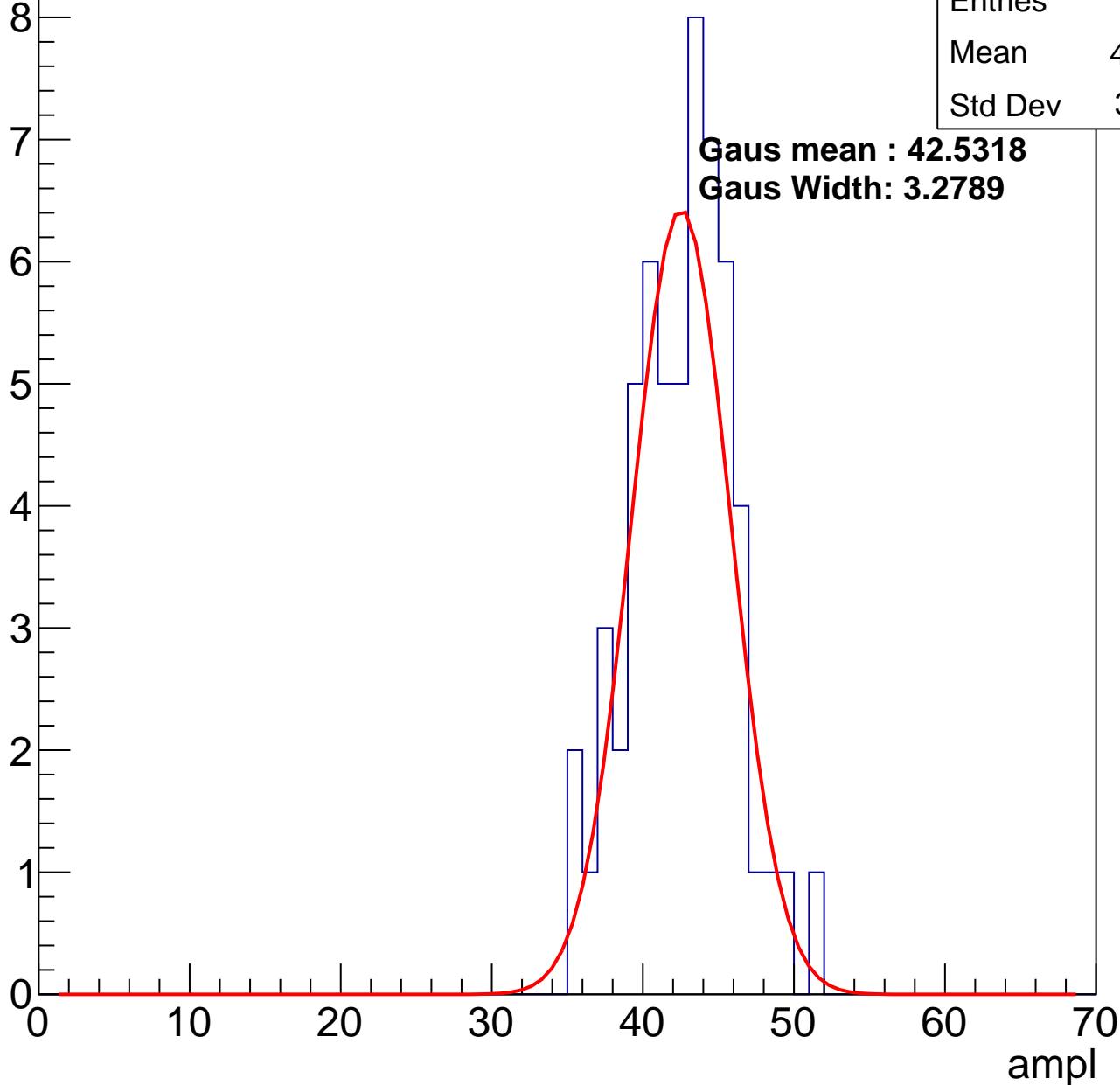
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	58
Mean	42.14
Std Dev	3.371

**Gaus mean : 42.5318**

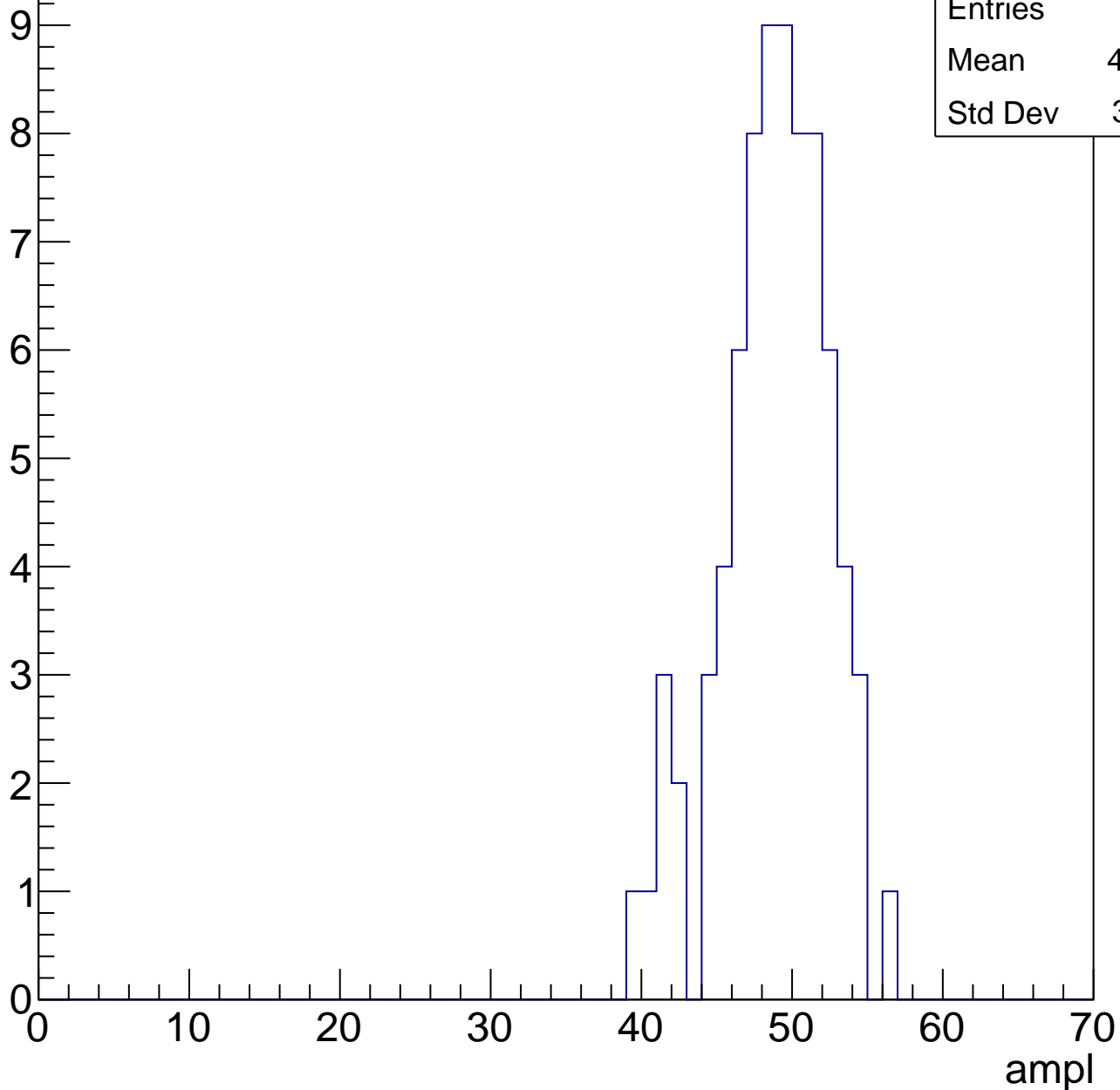
**Gaus Width: 3.2789**



# B1L003S, U18-ch46, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

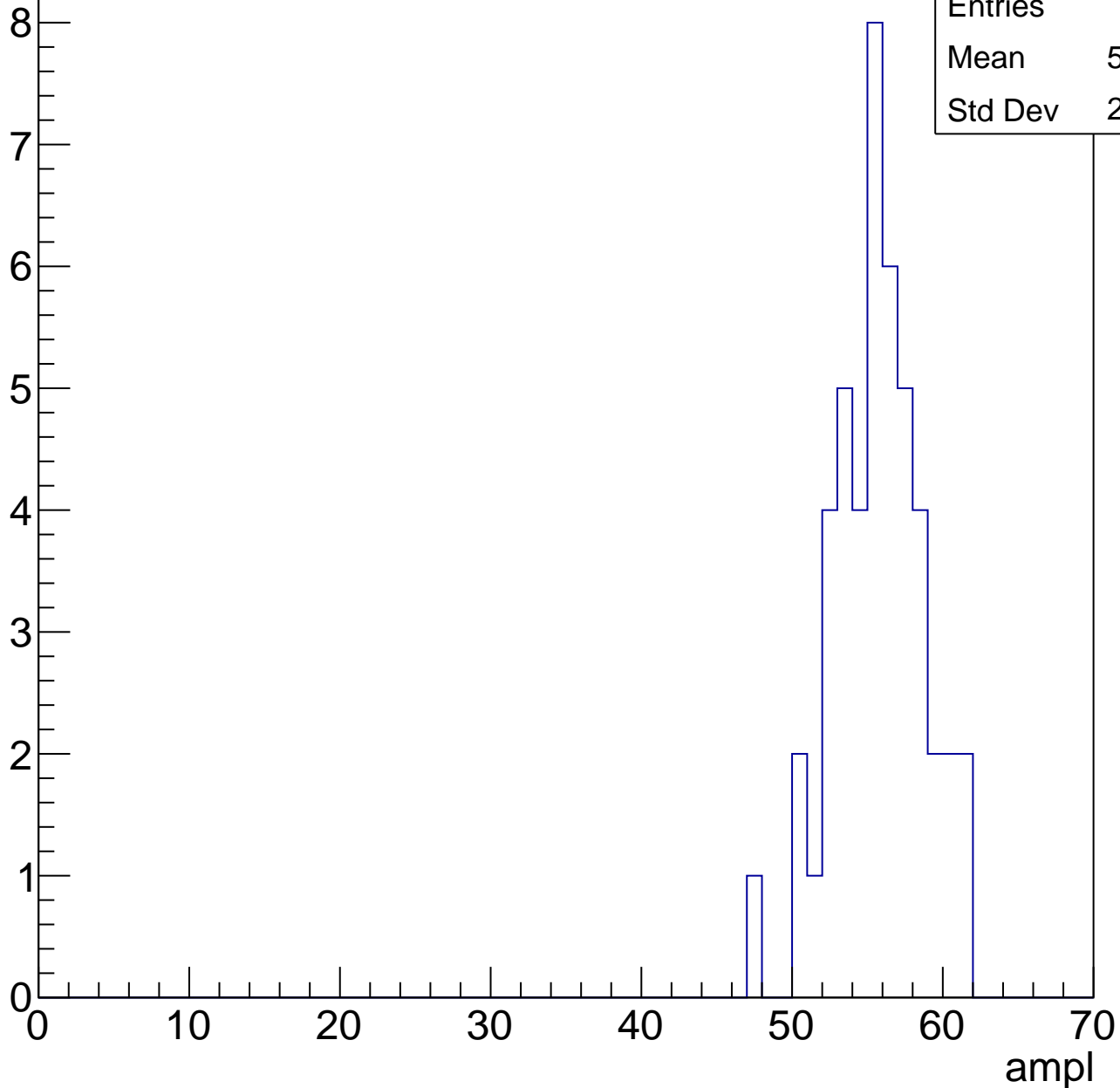


Entries	76
Mean	48.33
Std Dev	3.541

# B1L003S, U18-ch46, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

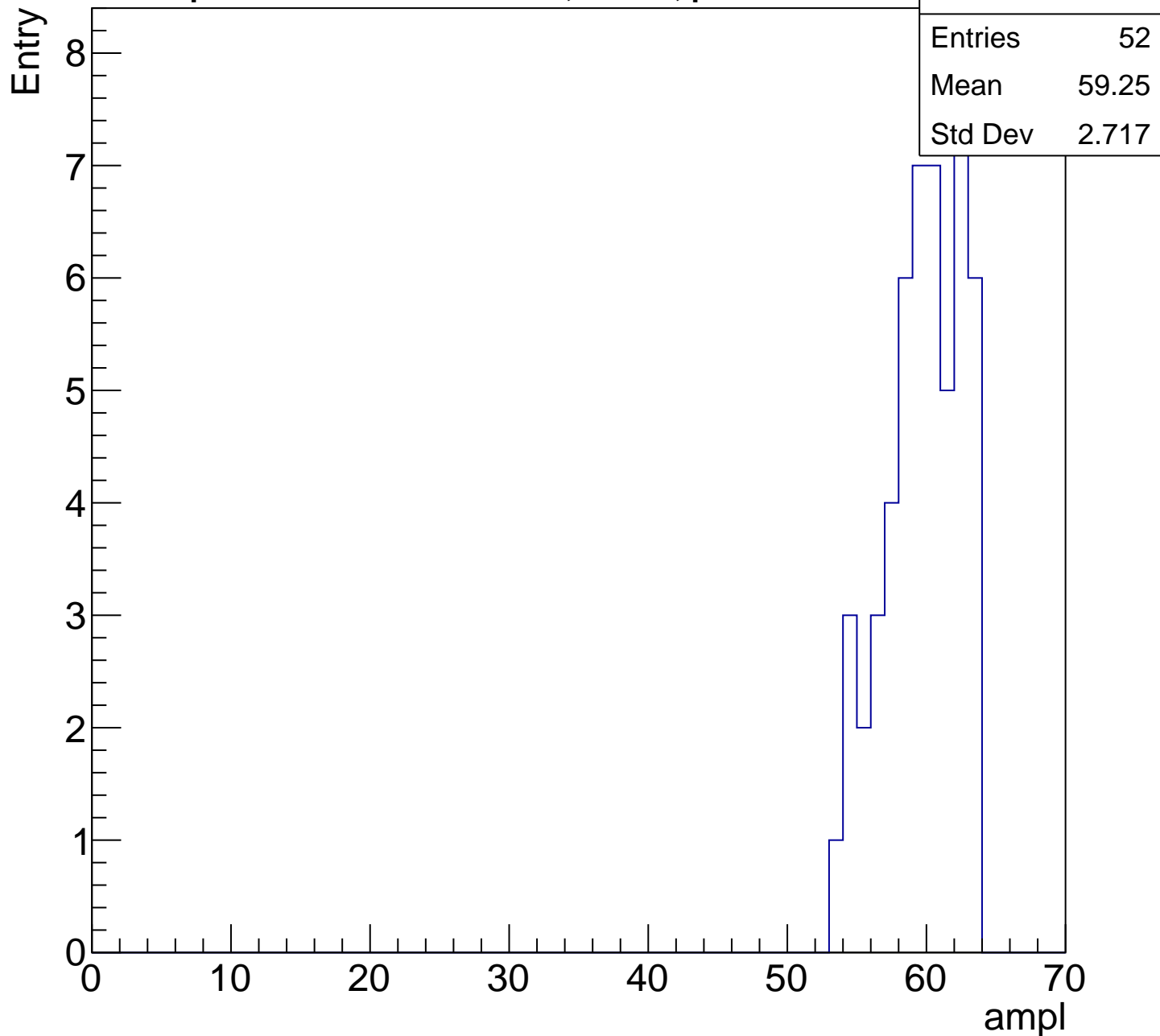
Entry



Entries	46
Mean	55.22
Std Dev	2.963

# B1L003S, U18-ch46, adc5

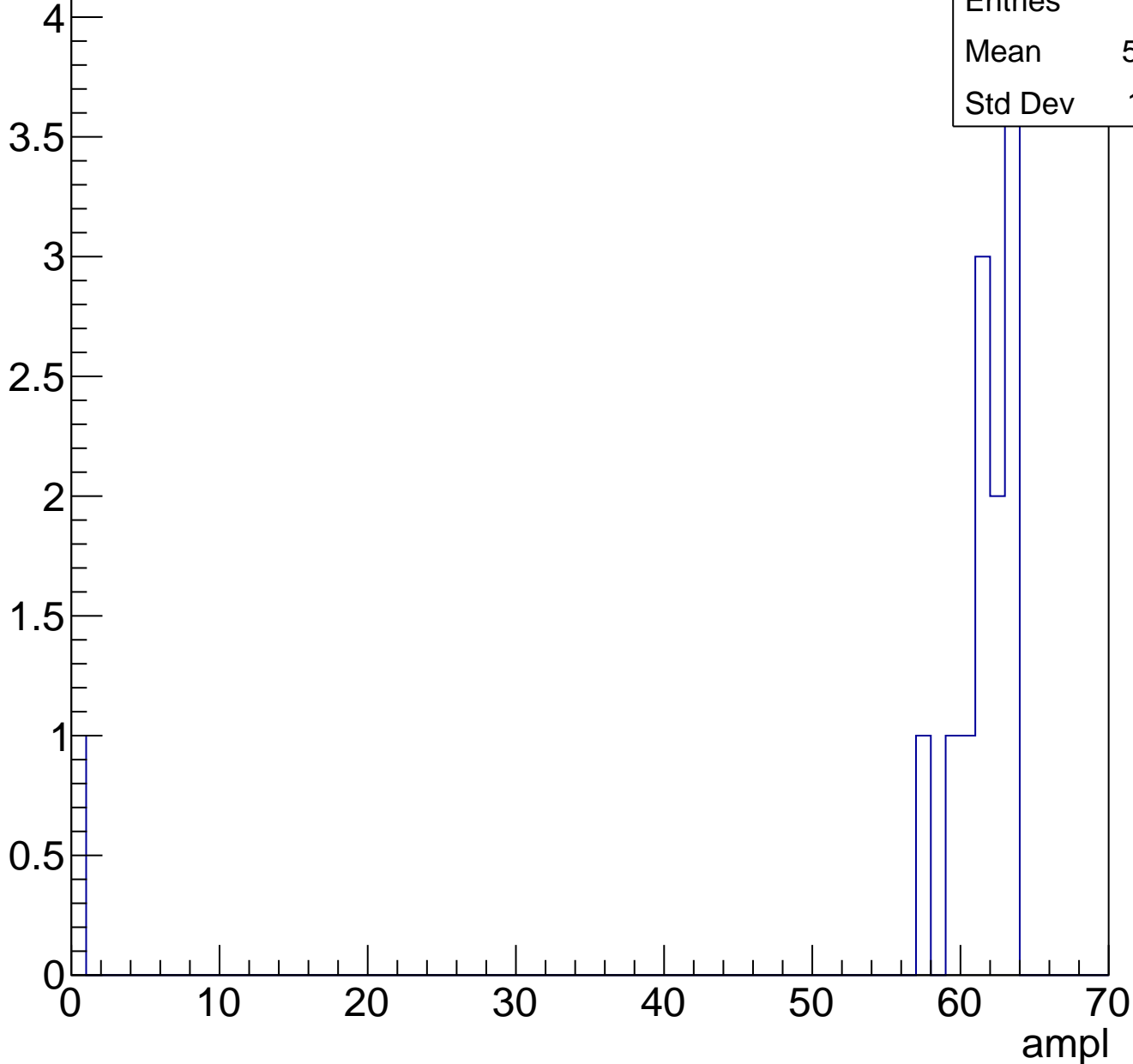
calib\_packv5\_042523\_0143.root, FC#13, port D2



# B1L003S, U18-ch46, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U18-ch46, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch47, adc0

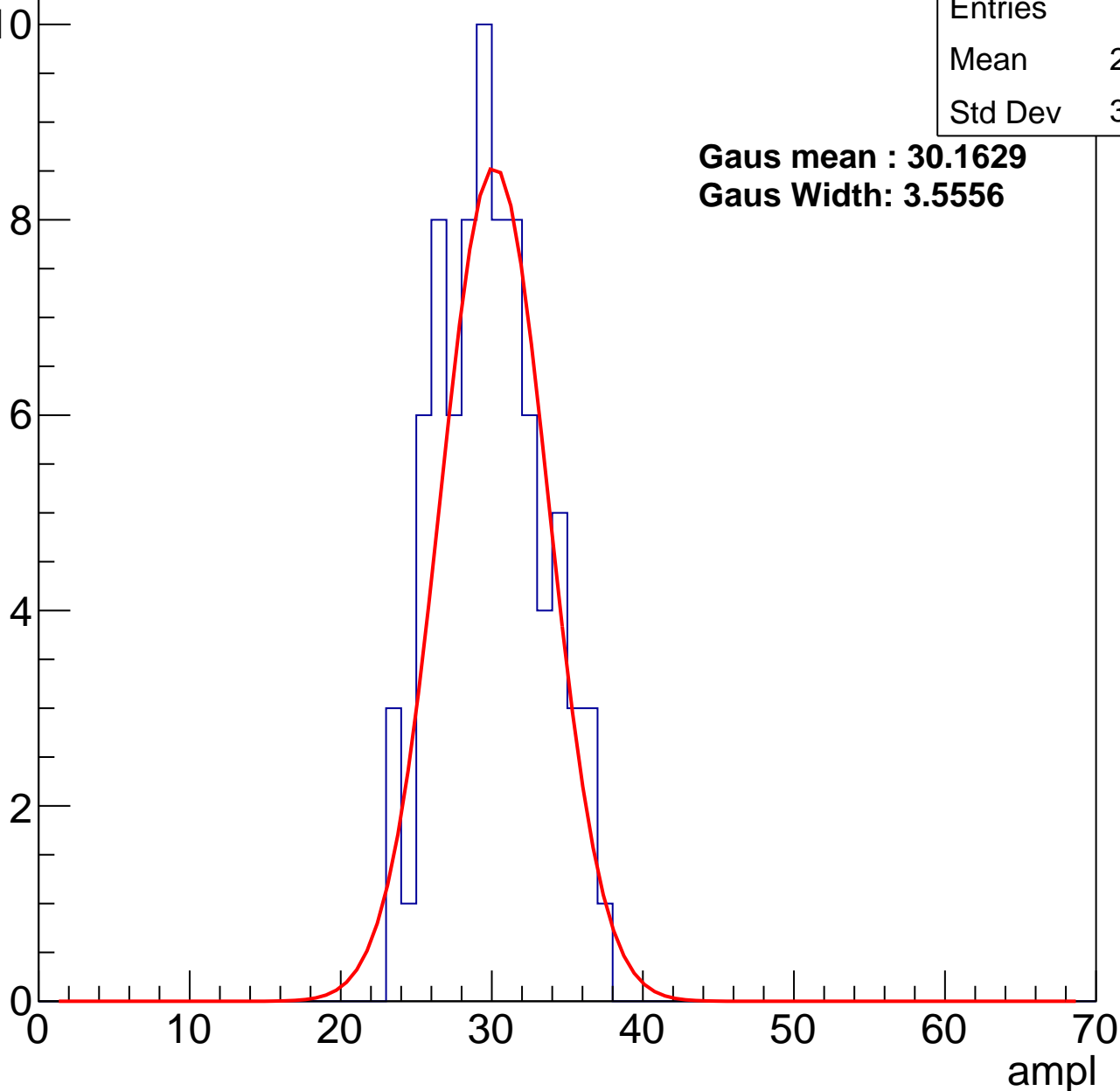
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	80
Mean	29.49
Std Dev	3.384

**Gaus mean : 30.1629**

**Gaus Width: 3.5556**



# B1L003S, U18-ch47, adc1

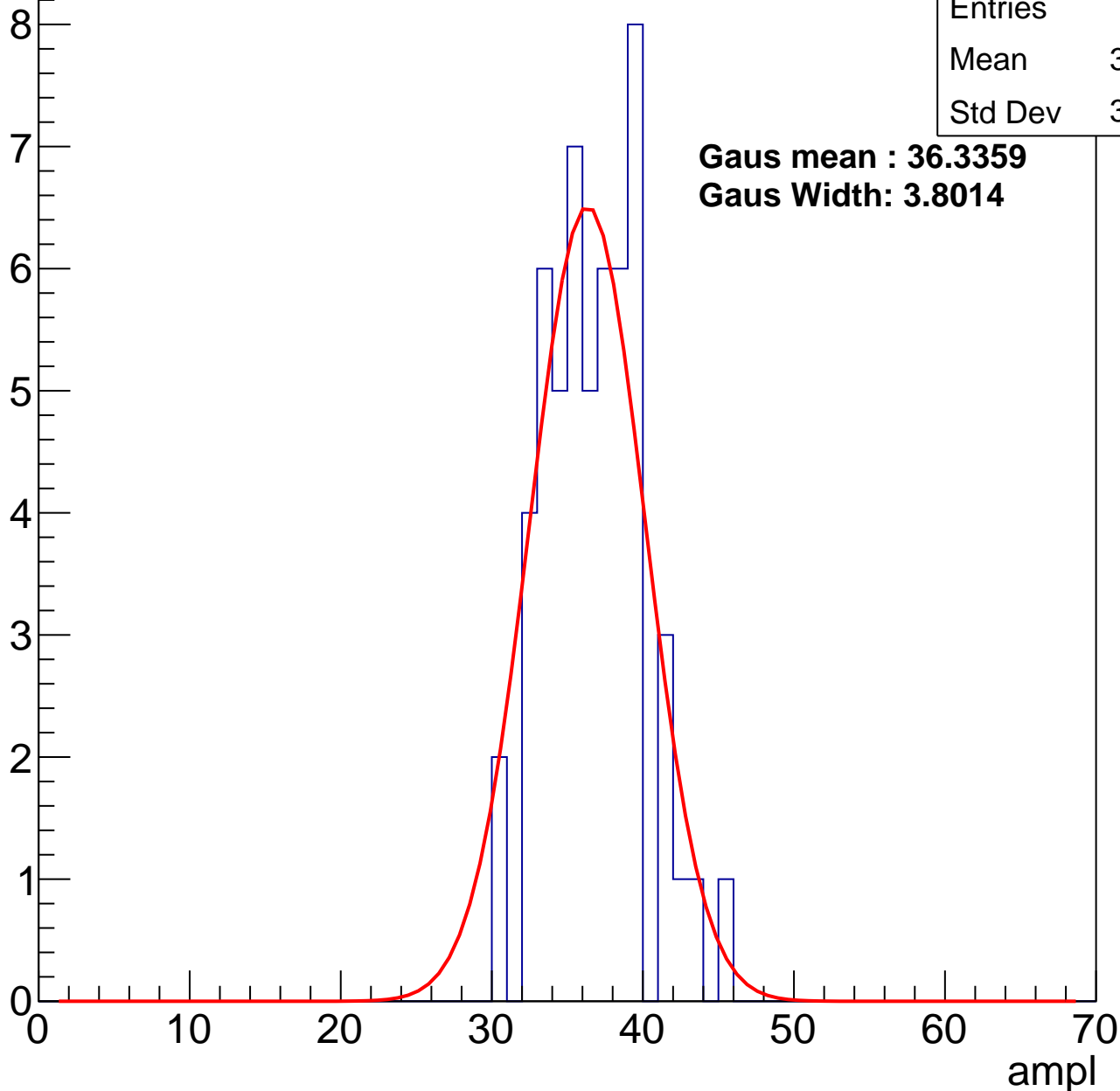
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	55
Mean	36.29
Std Dev	3.178

**Gaus mean : 36.3359**

**Gaus Width: 3.8014**



# B1L003S, U18-ch47, adc2

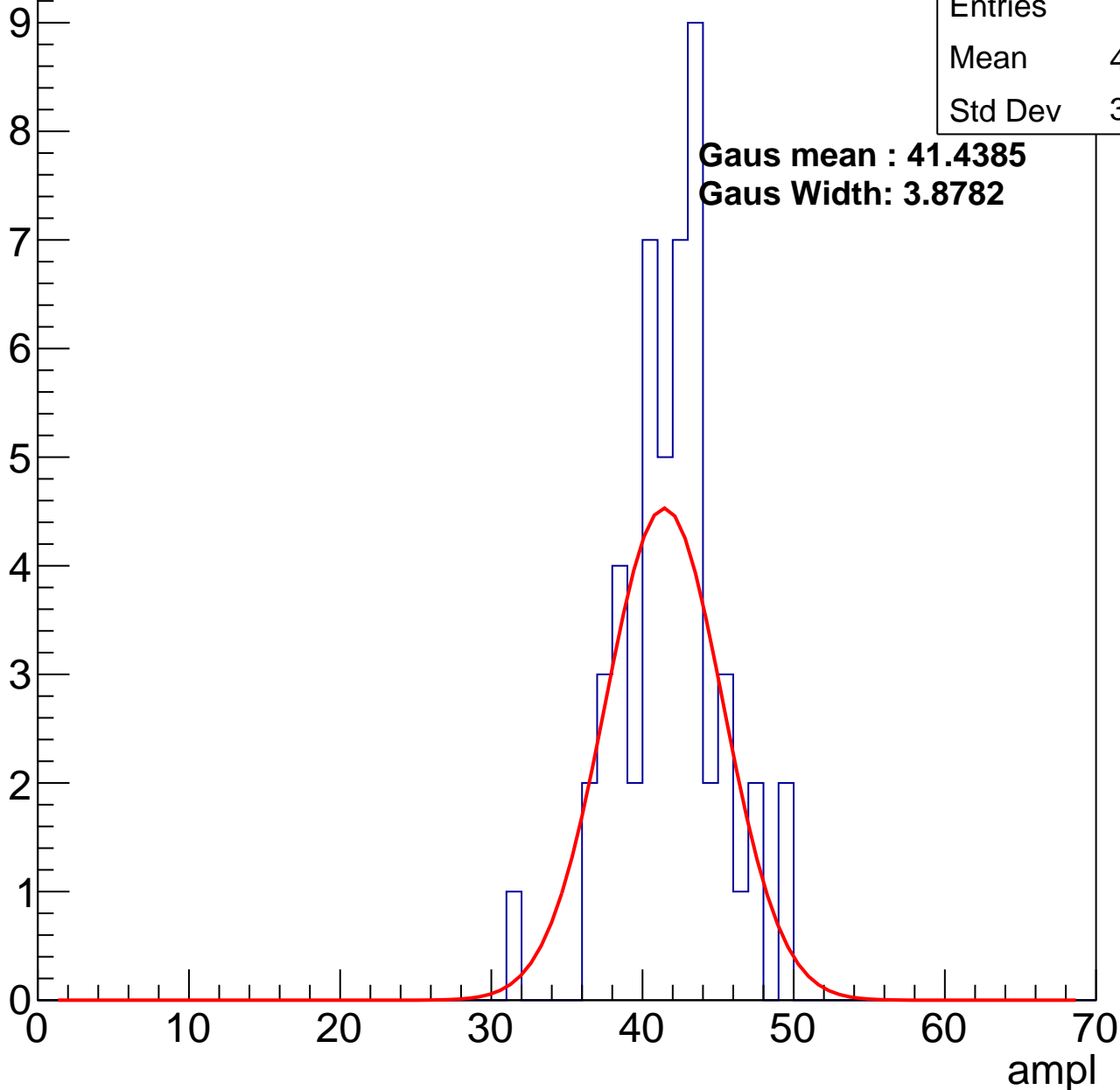
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	50
Mean	41.42
Std Dev	3.389

**Gaus mean : 41.4385**

**Gaus Width: 3.8782**

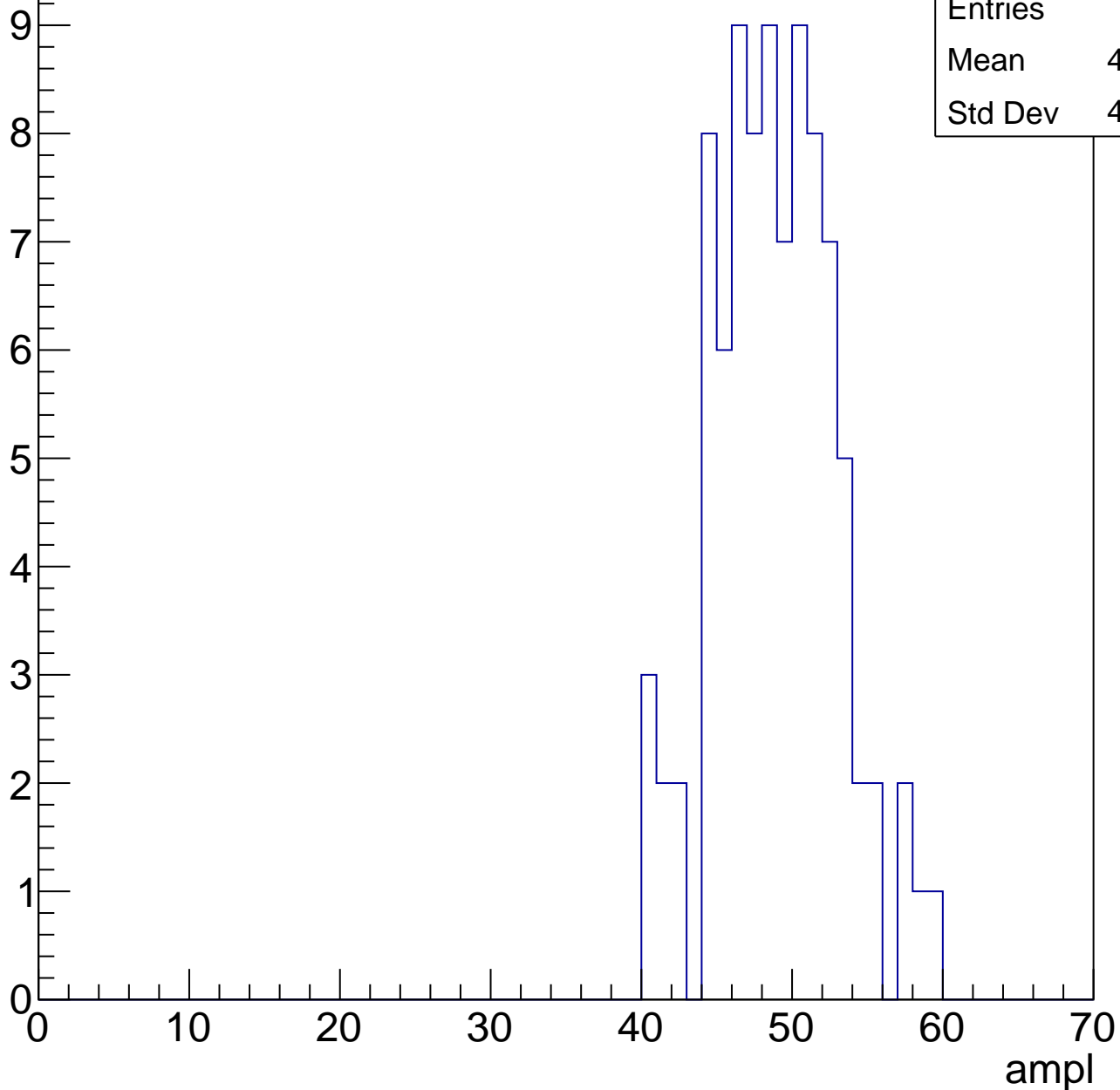


# B1L003S, U18-ch47, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	91
Mean	48.45
Std Dev	4.025

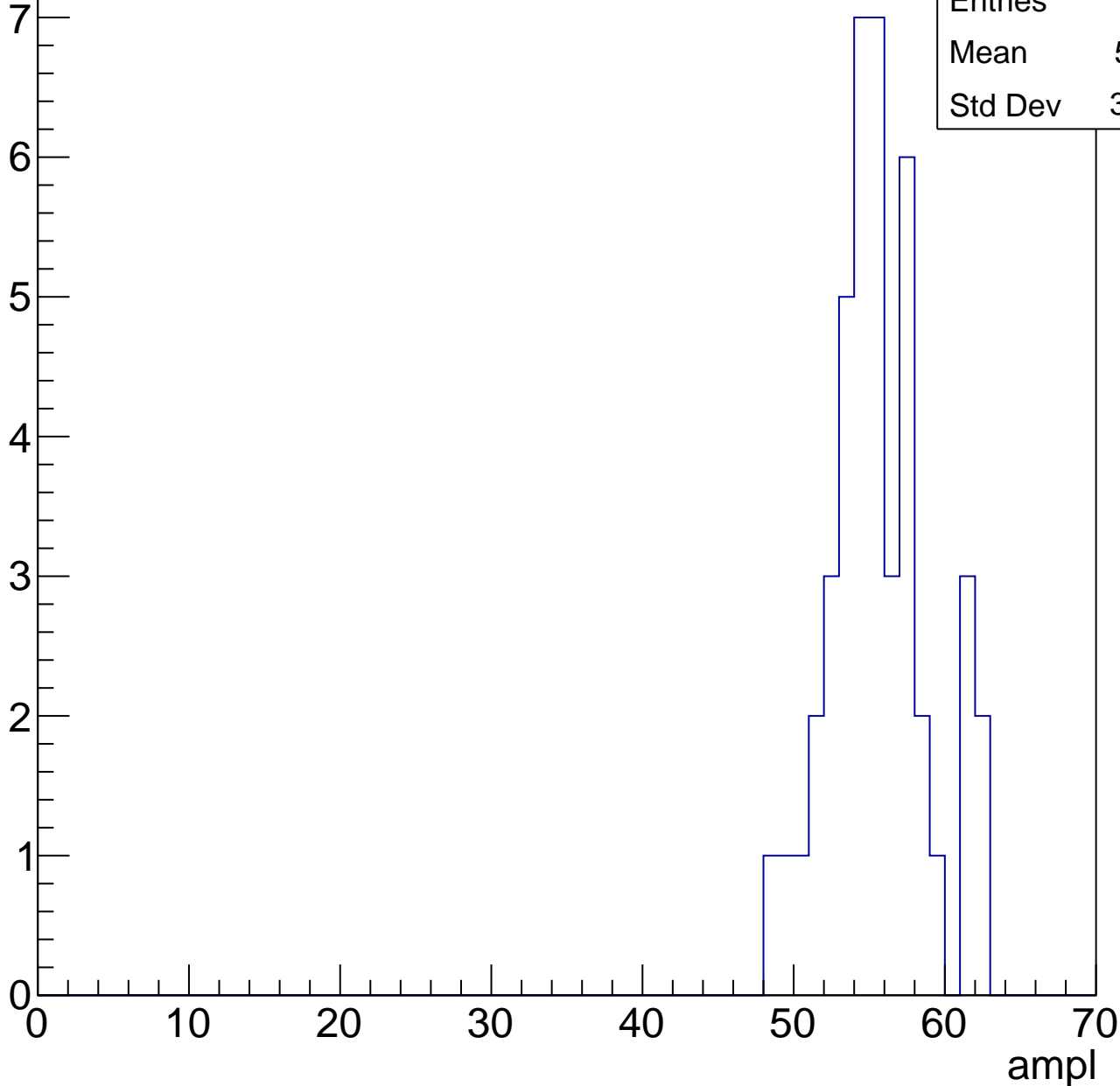


# B1L003S, U18-ch47, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	44
Mean	55.11
Std Dev	3.242

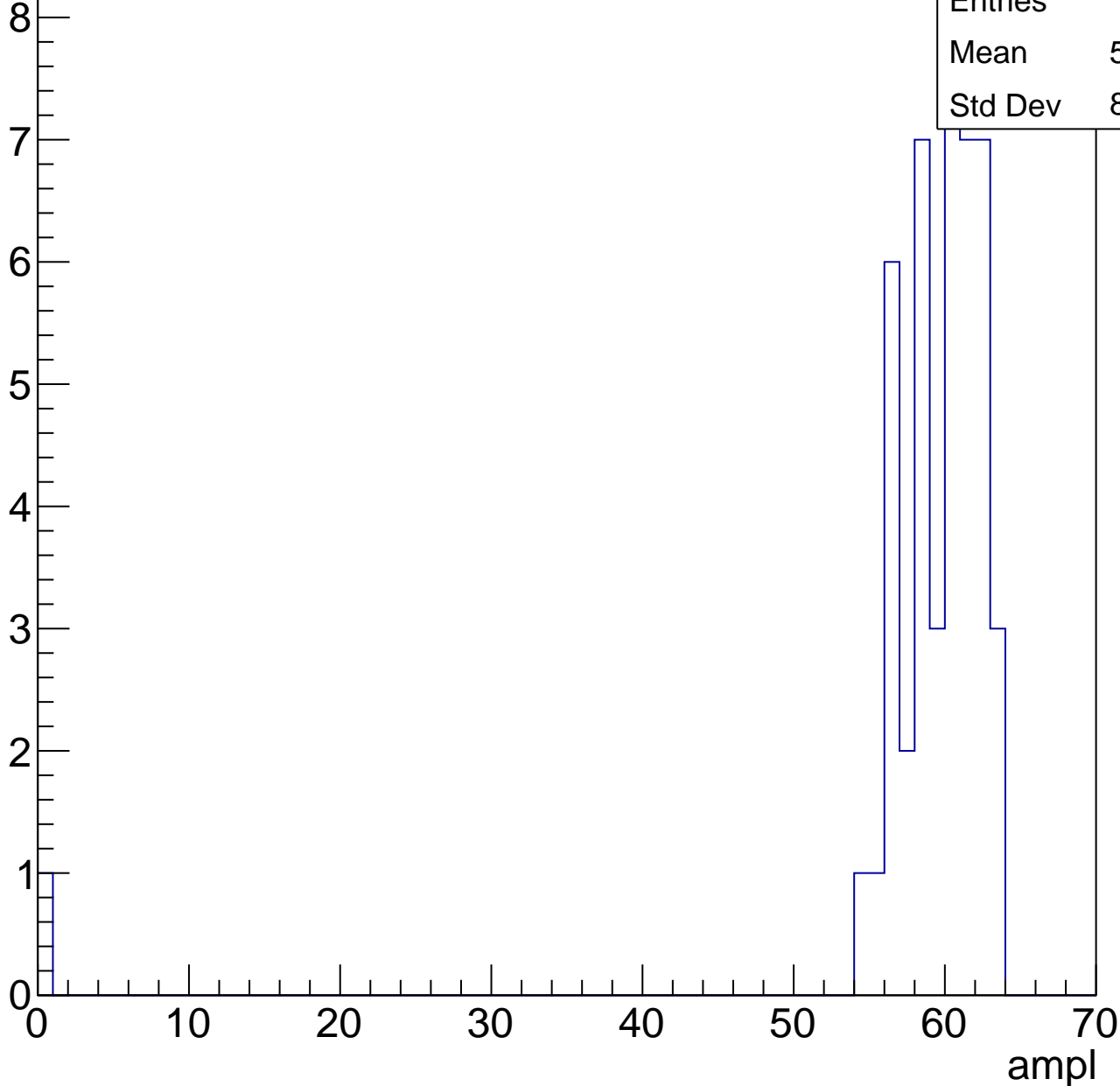


# B1L003S, U18-ch47, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	46
Mean	58.09
Std Dev	8.968

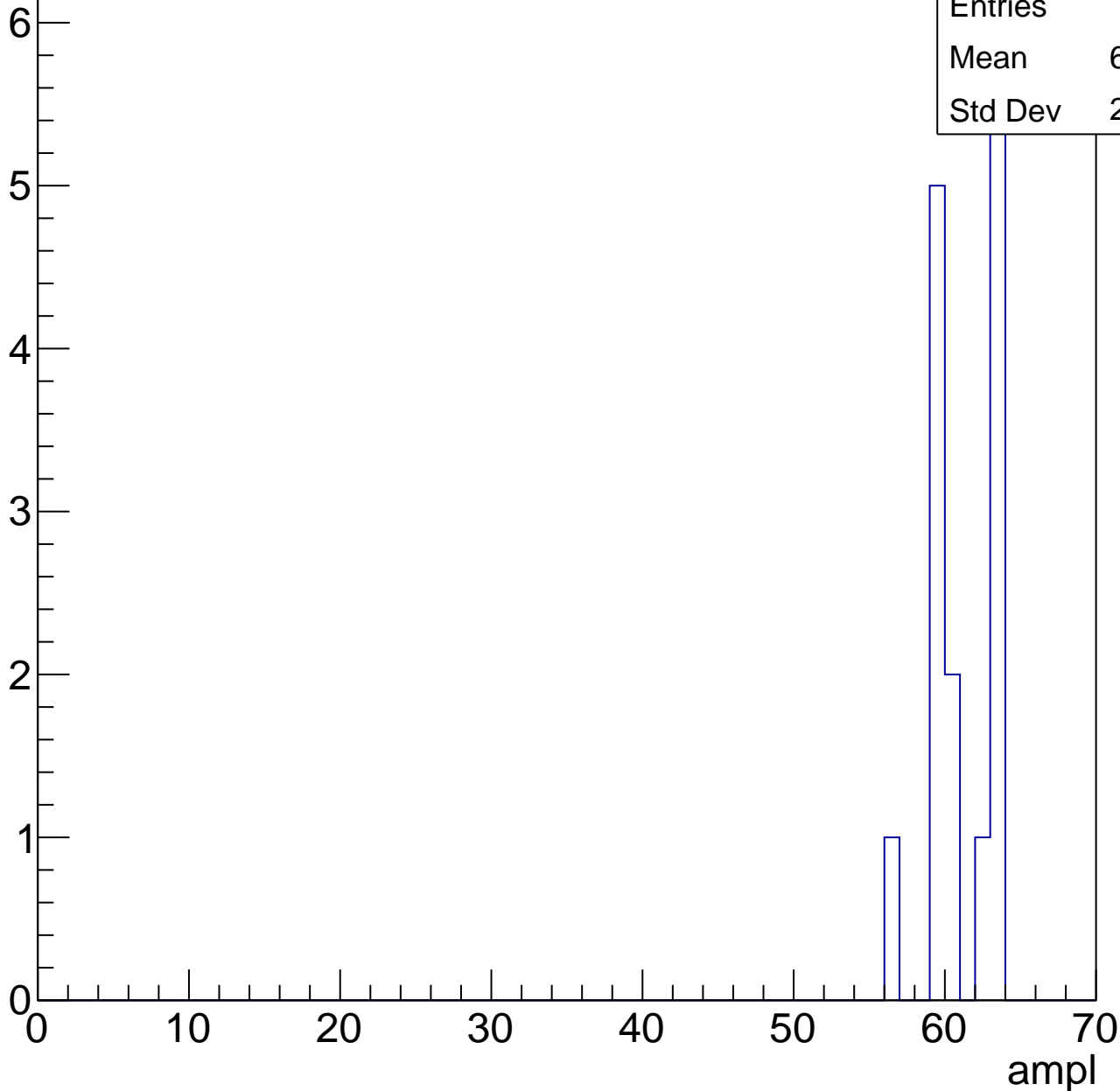


# B1L003S, U18-ch47, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	15
Mean	60.73
Std Dev	2.175





# B1L003S, U18-ch47, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U18-ch48, adc0

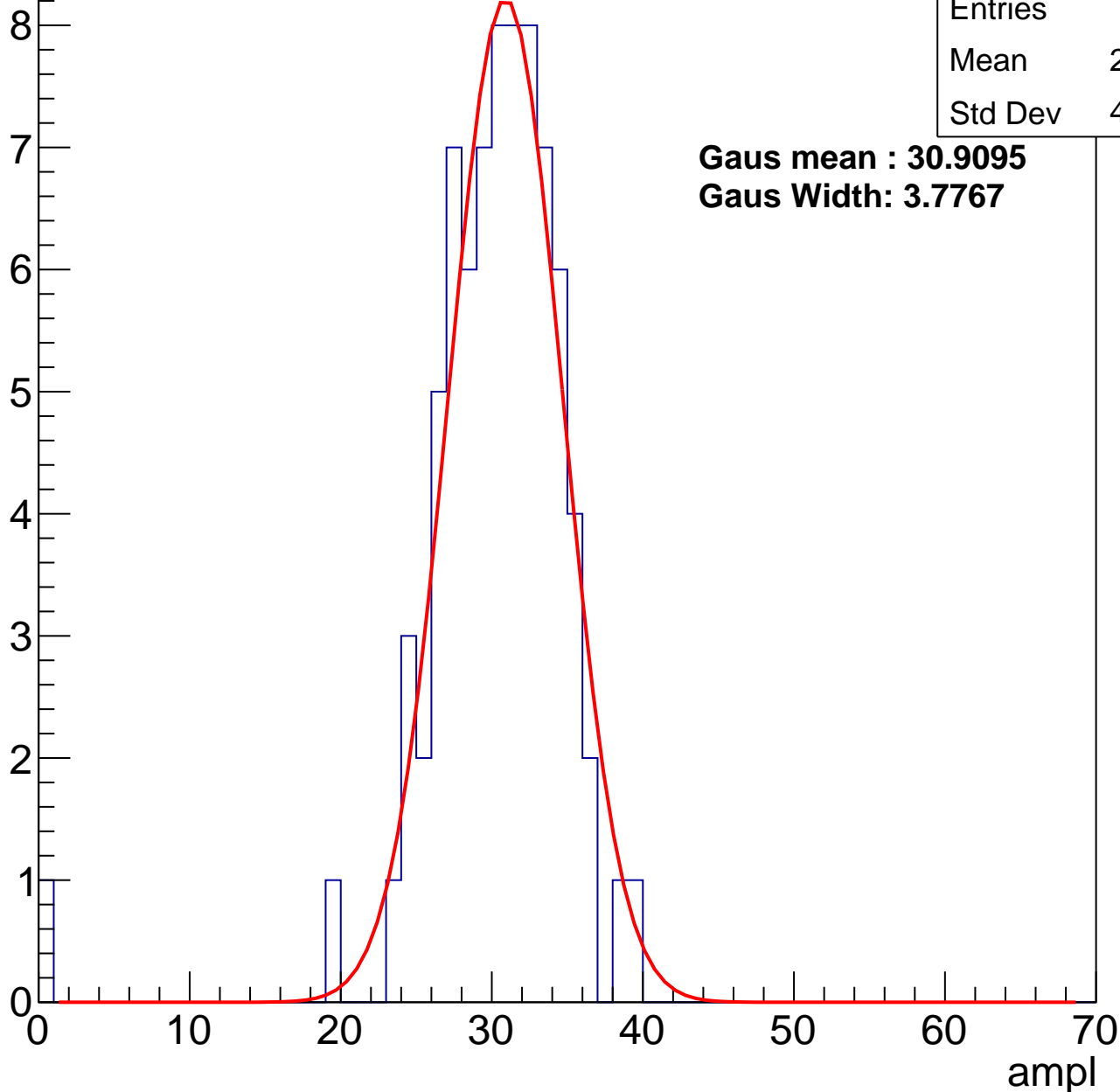
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	78
Mean	29.77
Std Dev	4.953

**Gaus mean : 30.9095**

**Gaus Width: 3.7767**



# B1L003S, U18-ch48, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	78
Mean	37.82
Std Dev	3.605

**Gaus mean : 38.4407**

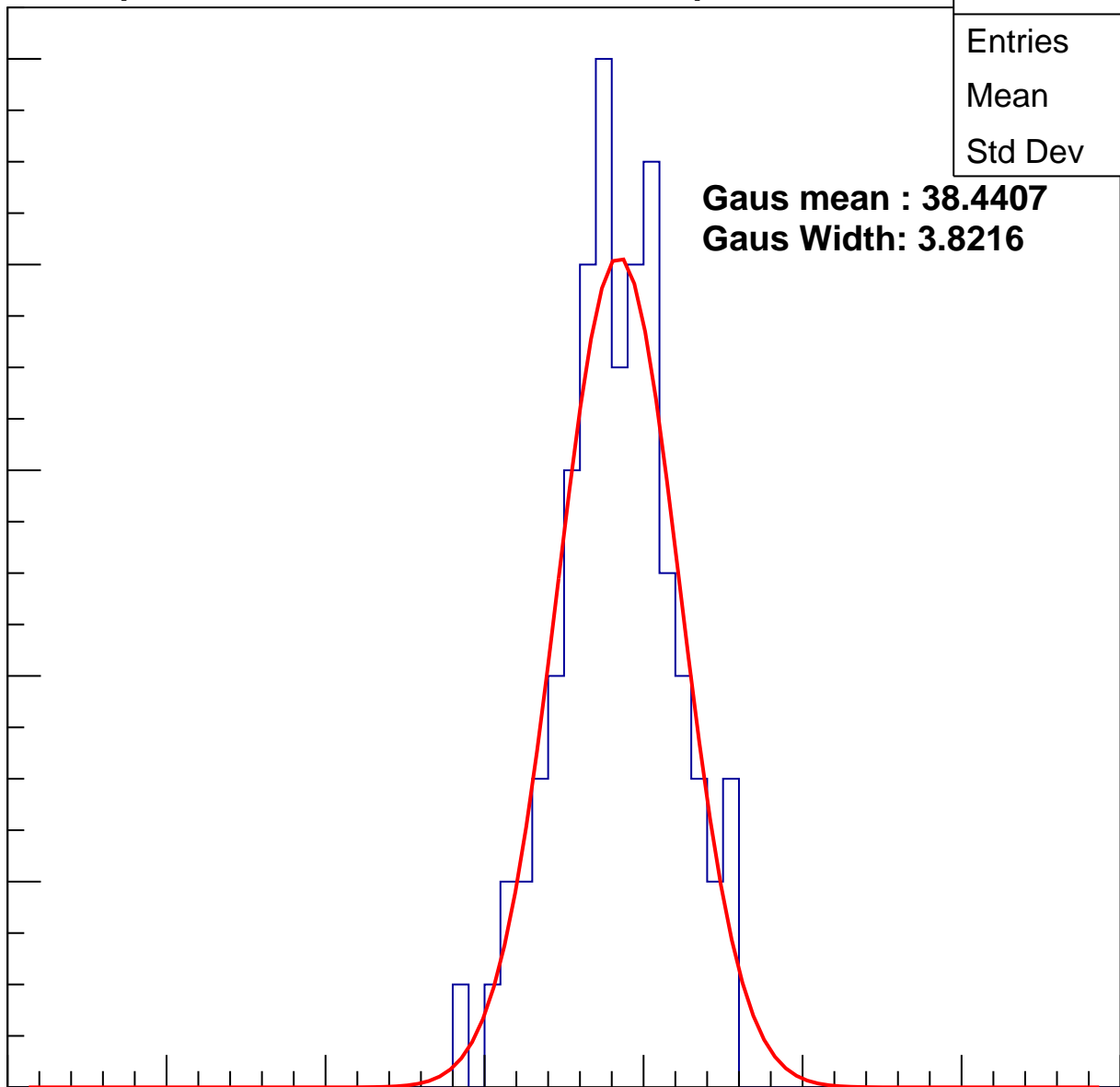
**Gaus Width: 3.8216**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B1L003S, U18-ch48, adc2

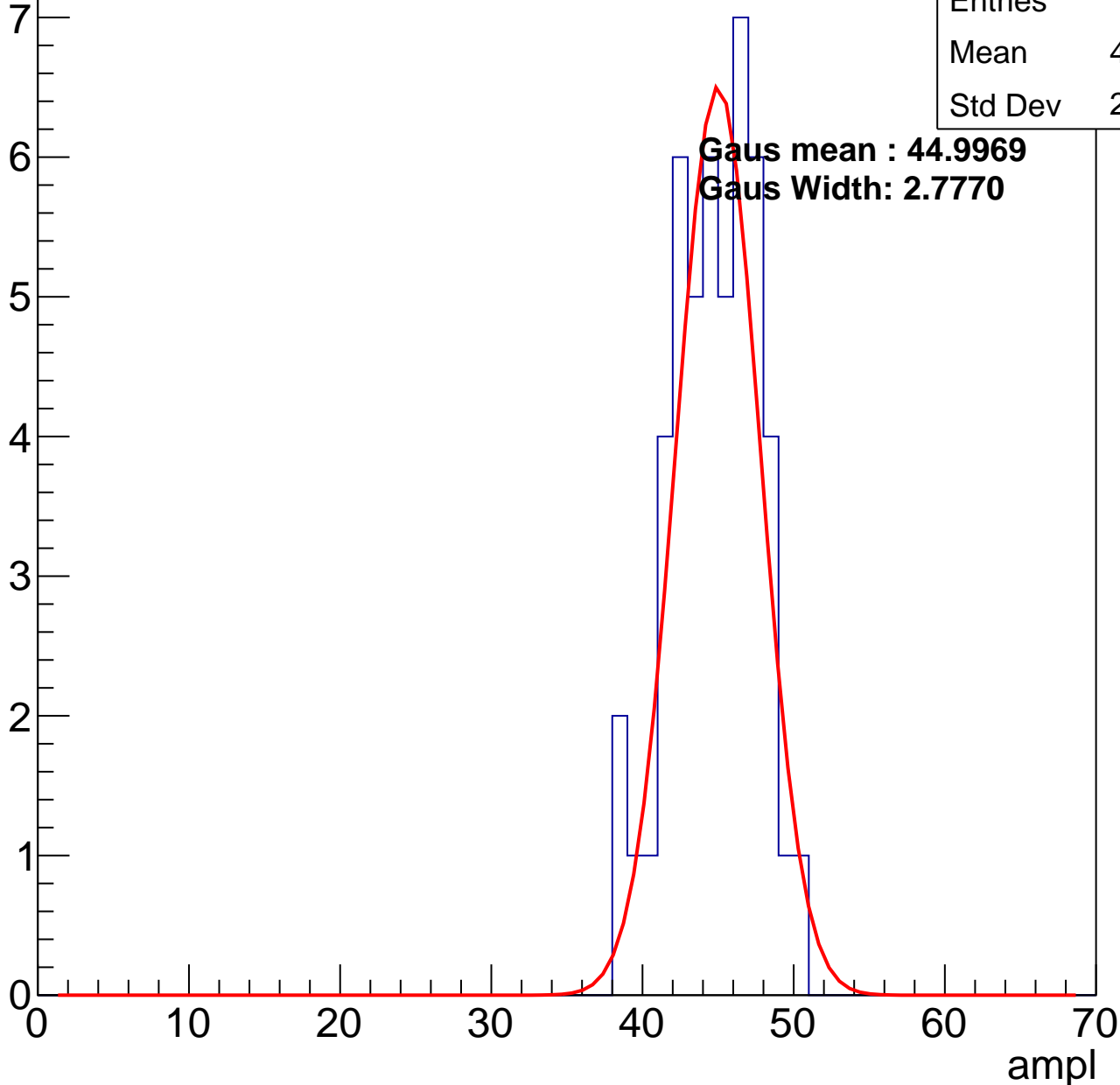
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	49
Mean	44.29
Std Dev	2.807

**Gaus mean : 44.9969**

**Gaus Width: 2.7770**

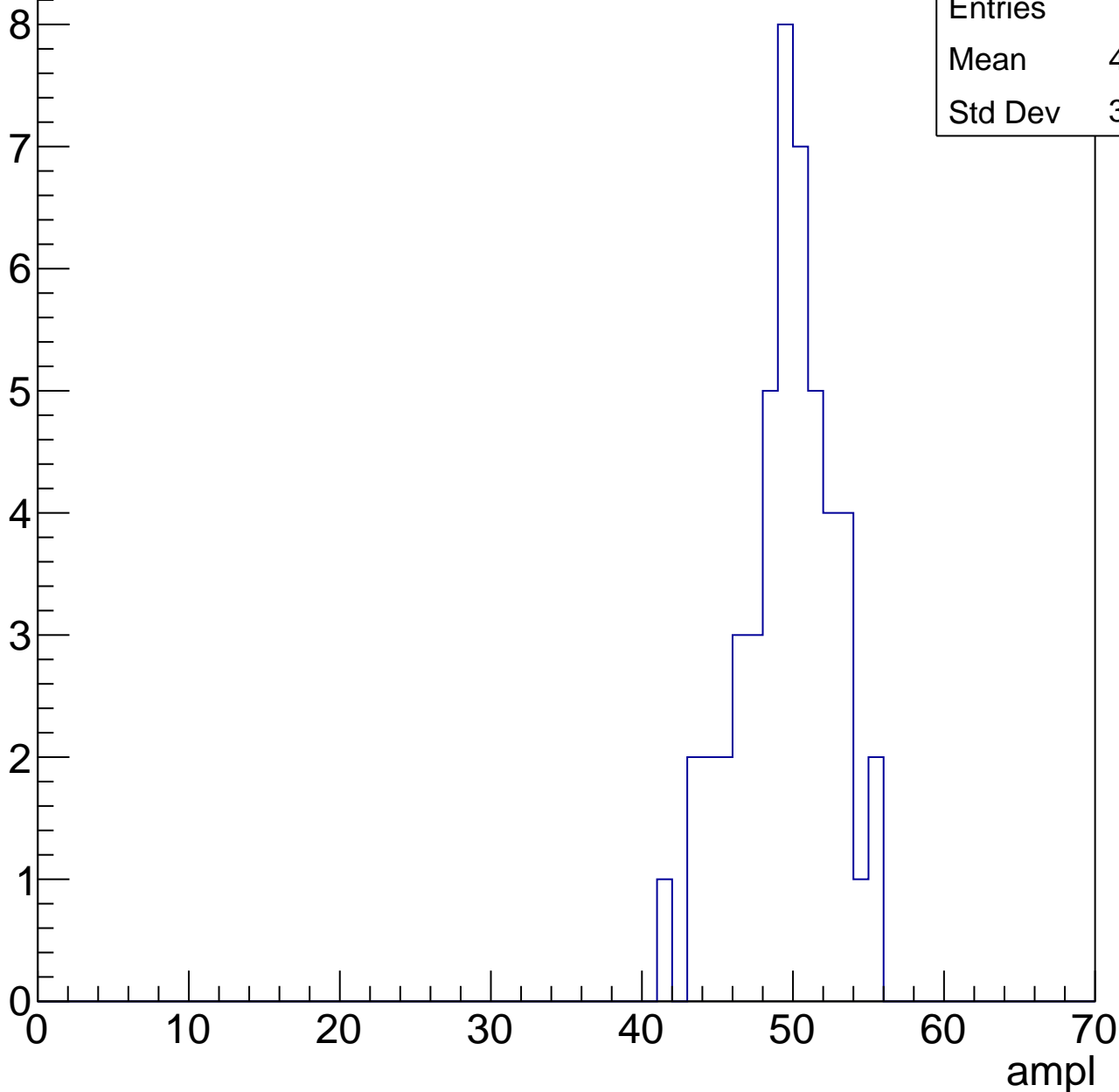


# B1L003S, U18-ch48, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

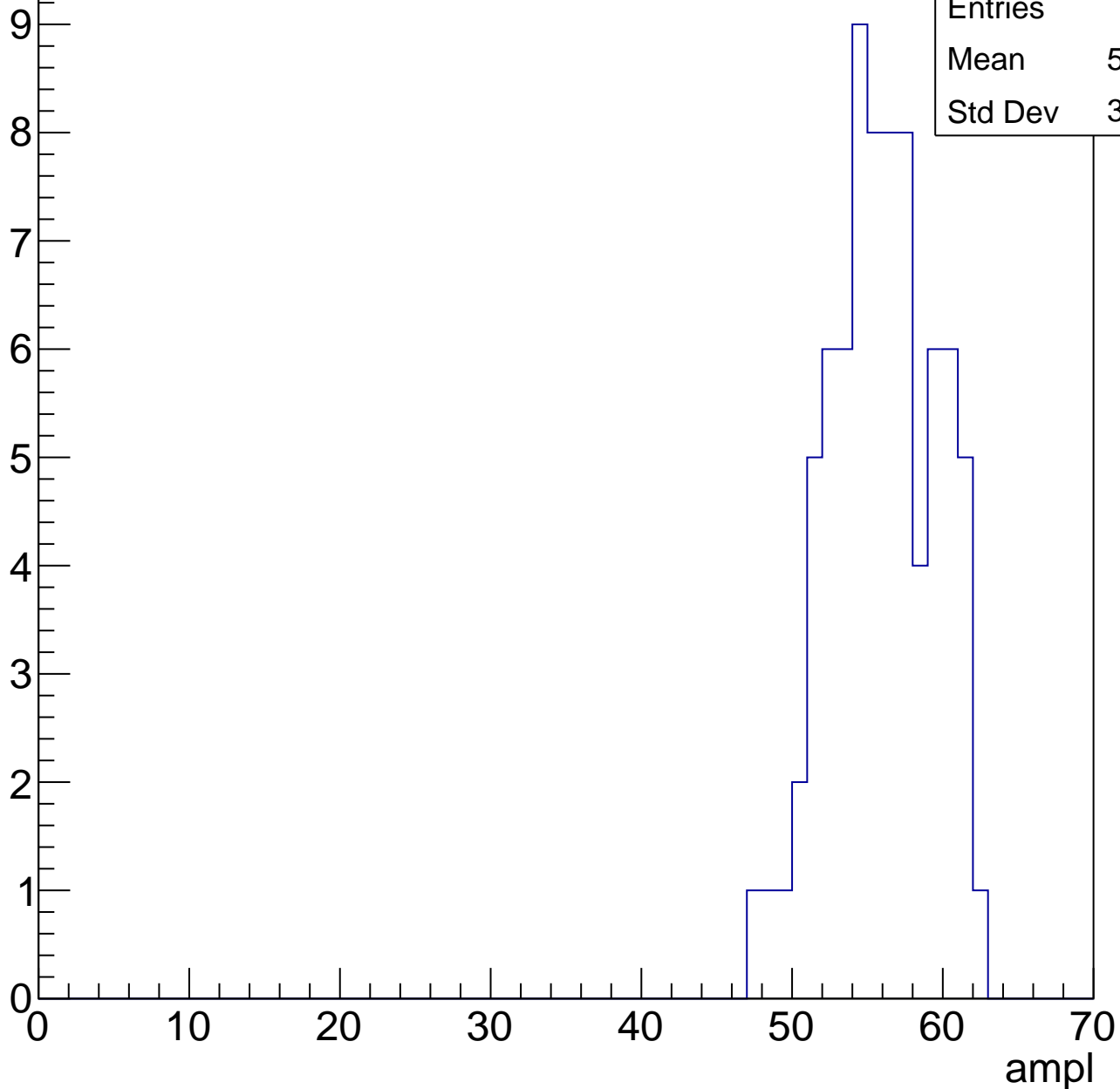
Entries	49
Mean	49.08
Std Dev	3.148



# B1L003S, U18-ch48, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

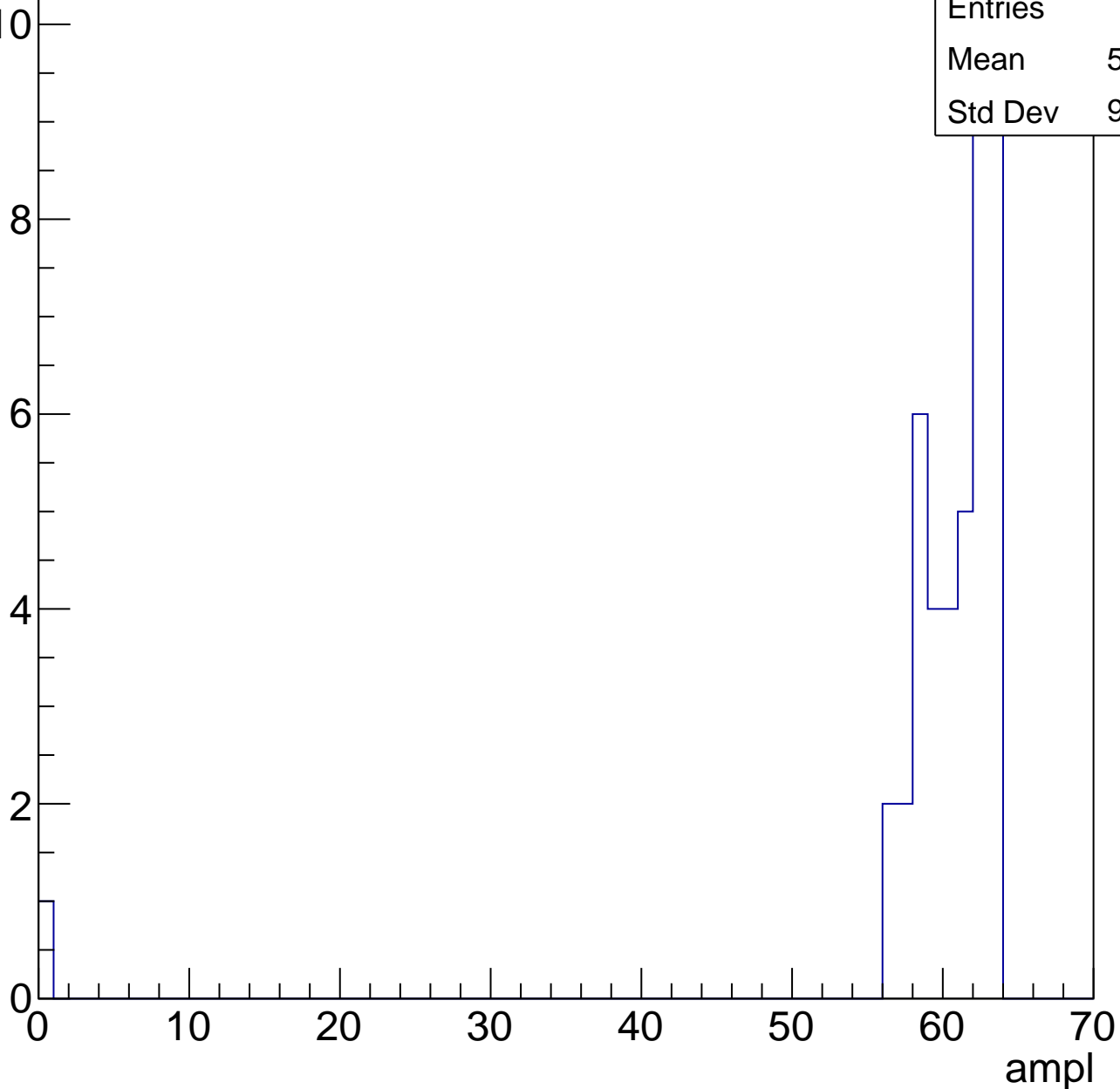


# B1L003S, U18-ch48, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	43
Mean	59.14
Std Dev	9.372



# B1L003S, U18-ch48, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

1

0.8

0.6

0.4

0.2

0

0

10

20

30

40

50

60

70

ampl

Entries

0

Mean

0

Std Dev

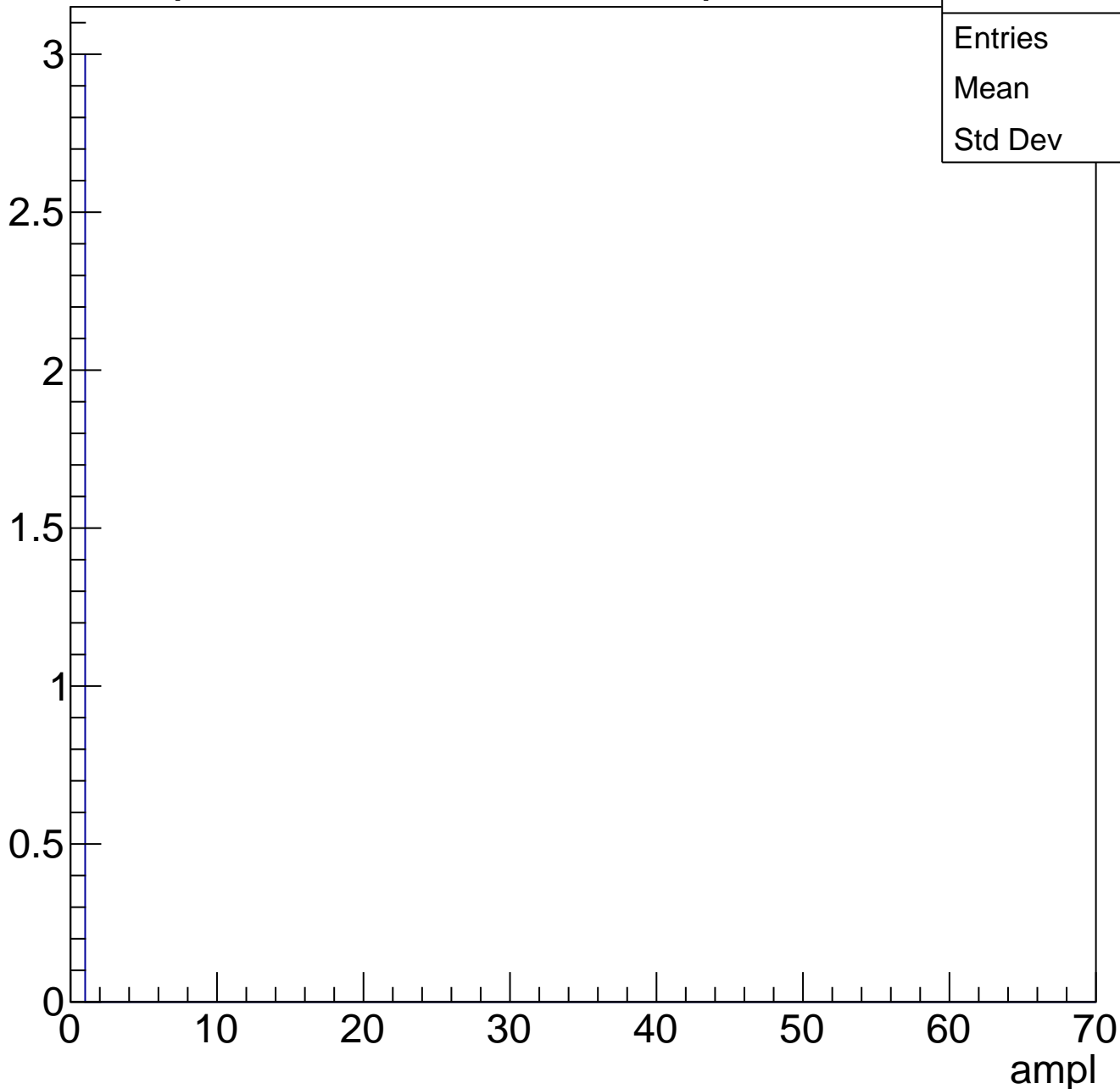
0



# B1L003S, U18-ch48, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	3
Mean	0
Std Dev	0

# B1L003S, U18-ch49, adc0

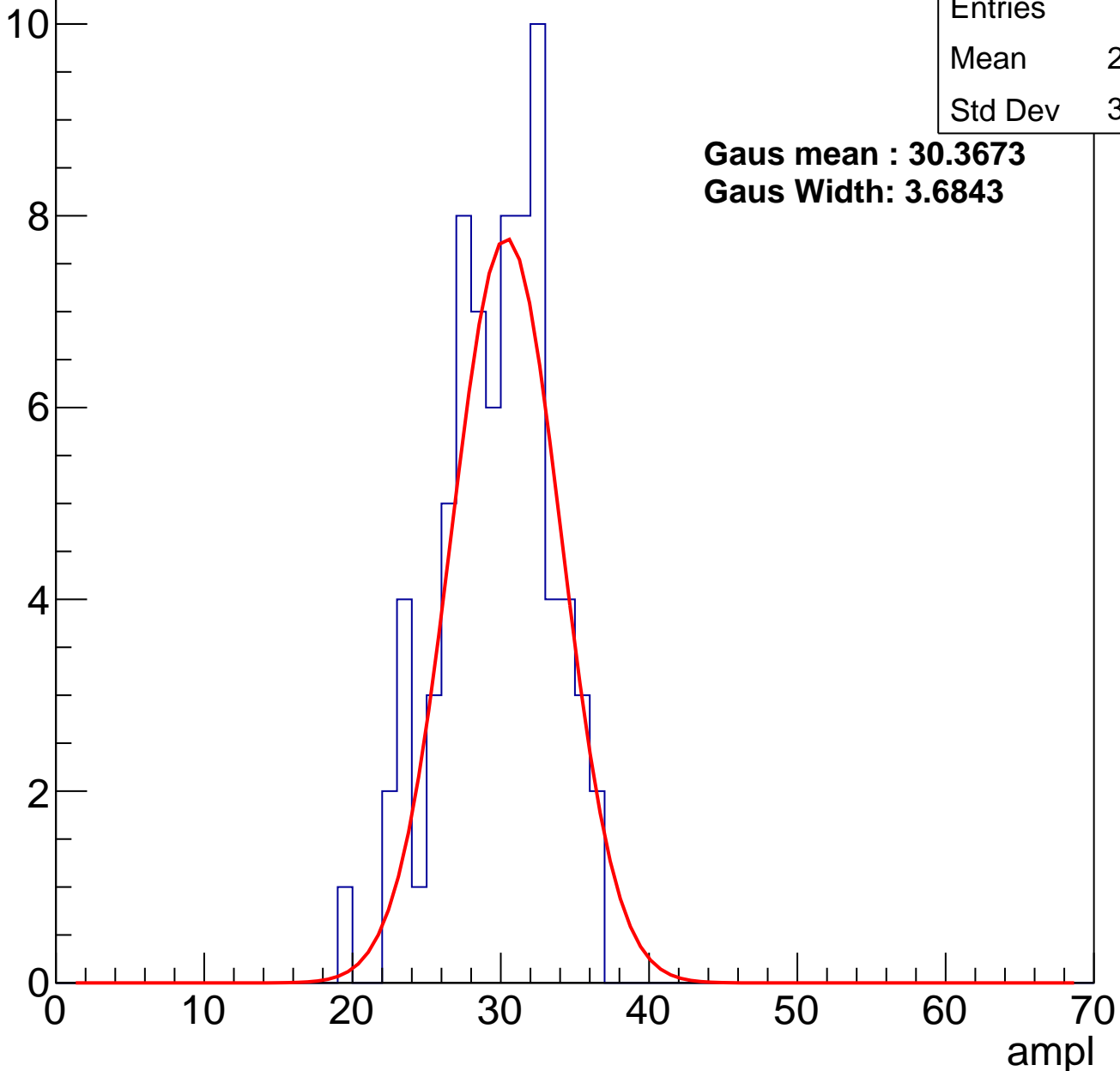
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	76
Mean	29.25
Std Dev	3.617

**Gaus mean : 30.3673**

**Gaus Width: 3.6843**

Entry



# B1L003S, U18-ch49, adc1

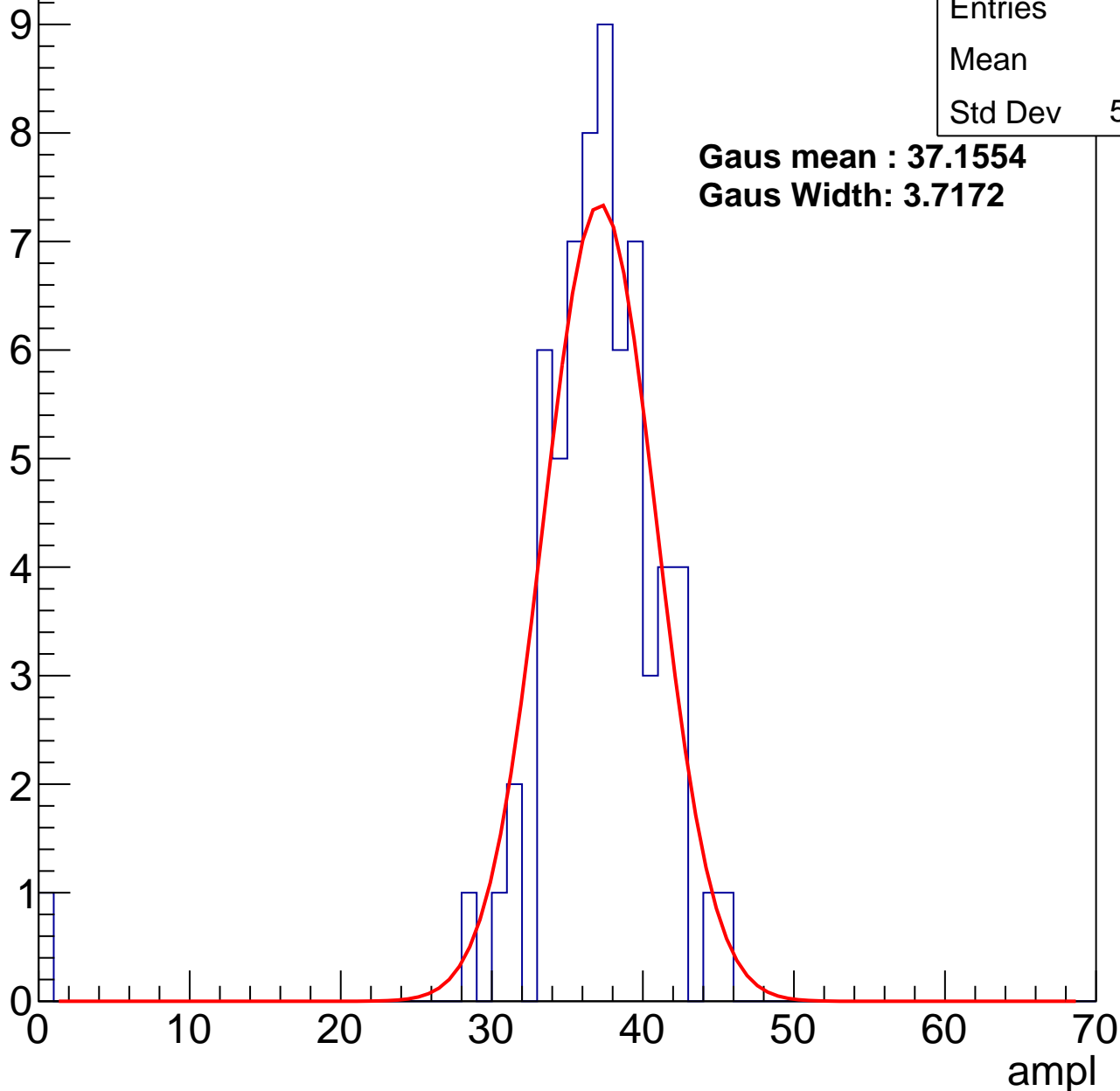
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	66
Mean	36.3
Std Dev	5.579

**Gaus mean : 37.1554**

**Gaus Width: 3.7172**



# B1L003S, U18-ch49, adc2

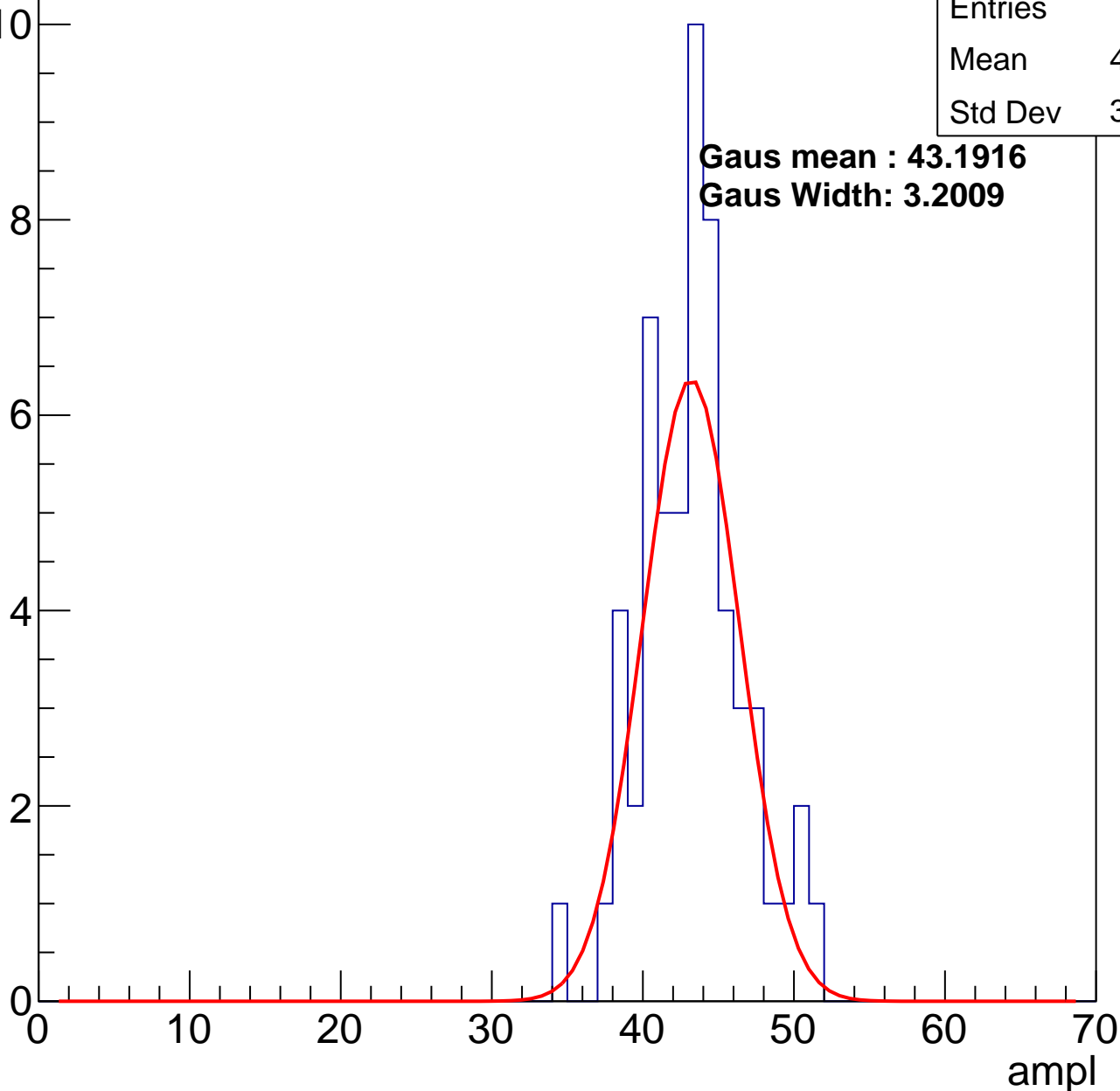
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	58
Mean	42.84
Std Dev	3.367

**Gaus mean : 43.1916**

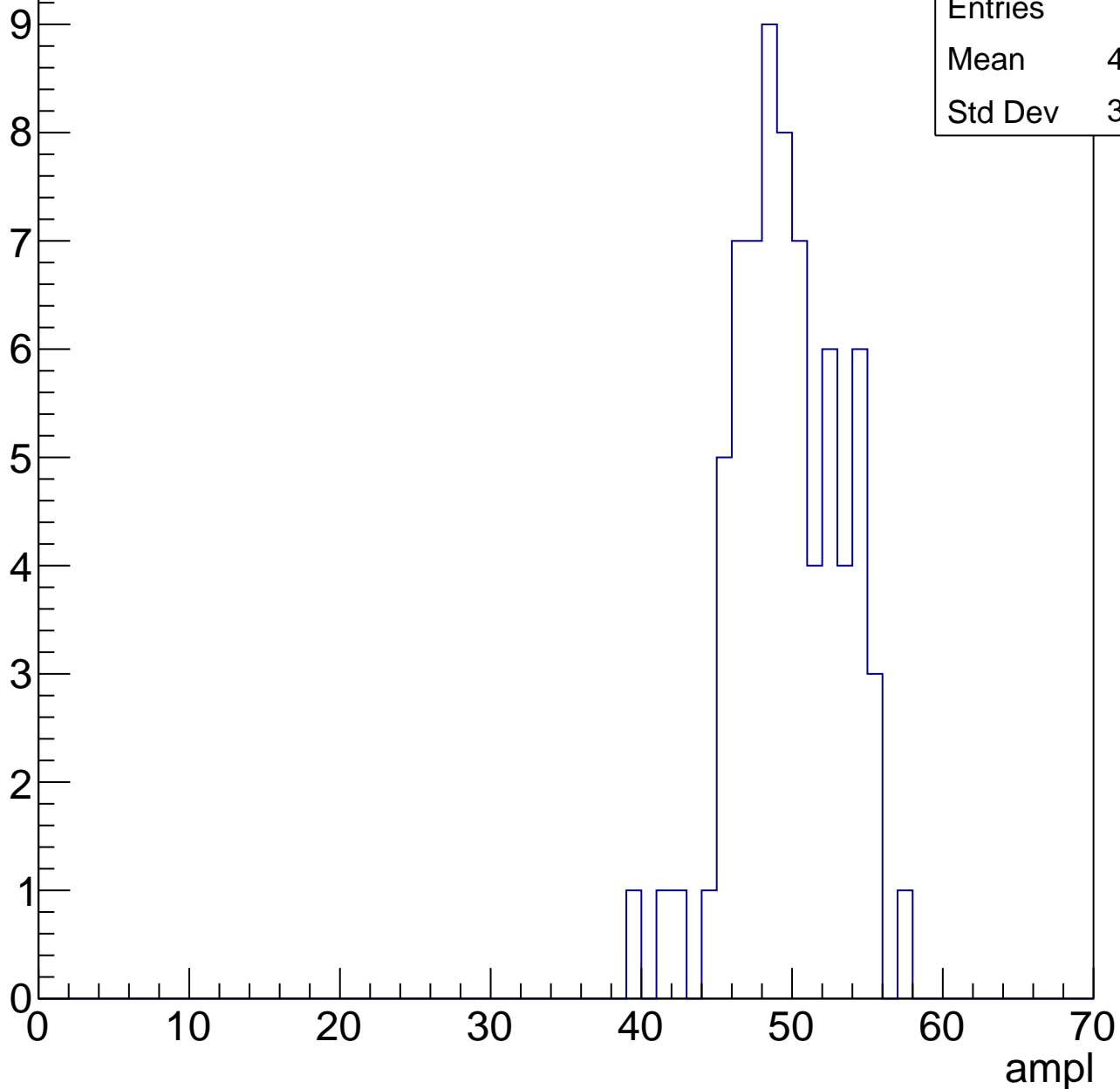
**Gaus Width: 3.2009**



# B1L003S, U18-ch49, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



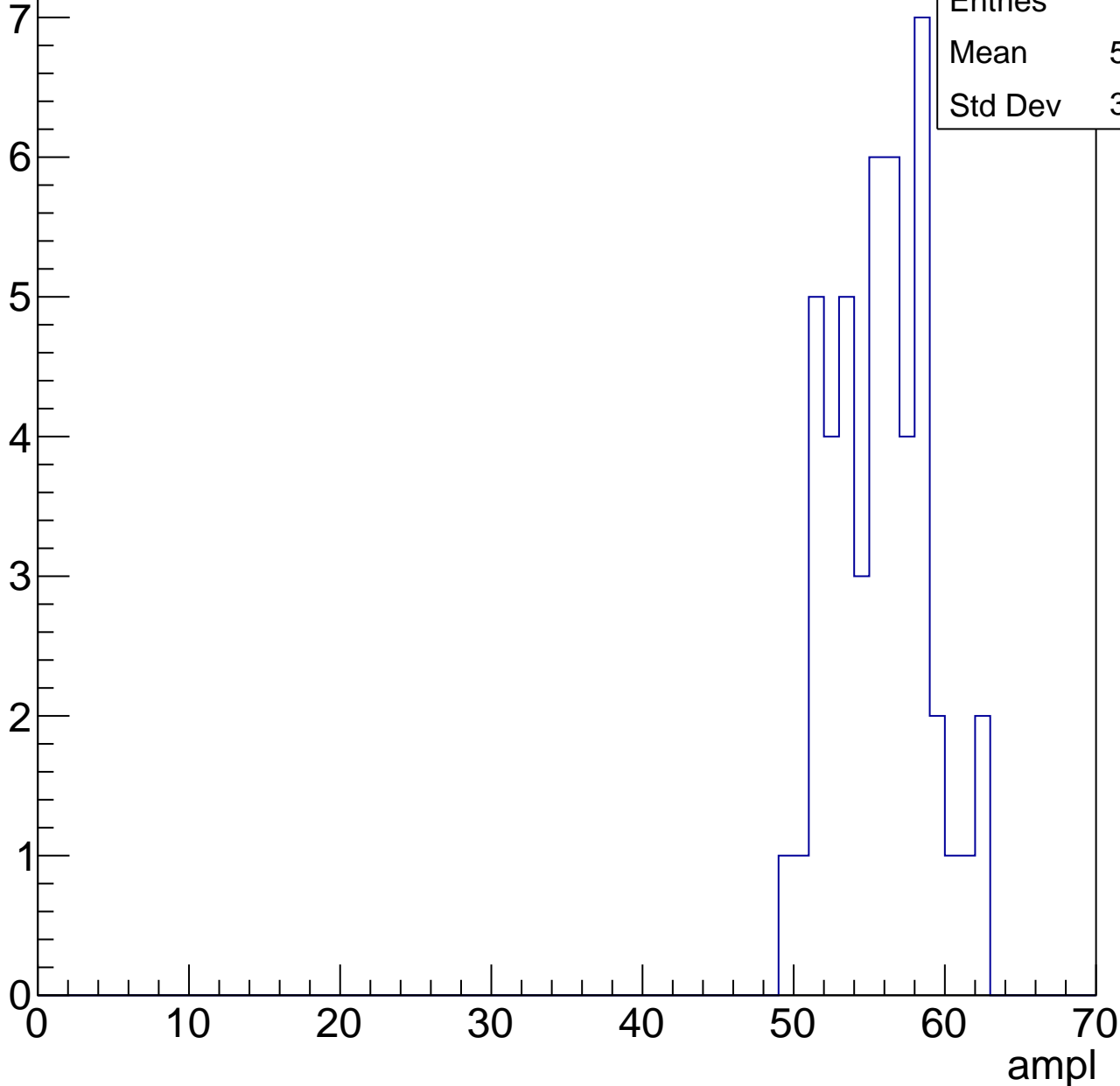
Entries	71
Mean	49.15
Std Dev	3.519

# B1L003S, U18-ch49, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	48
Mean	55.25
Std Dev	3.139



# B1L003S, U18-ch49, adc5

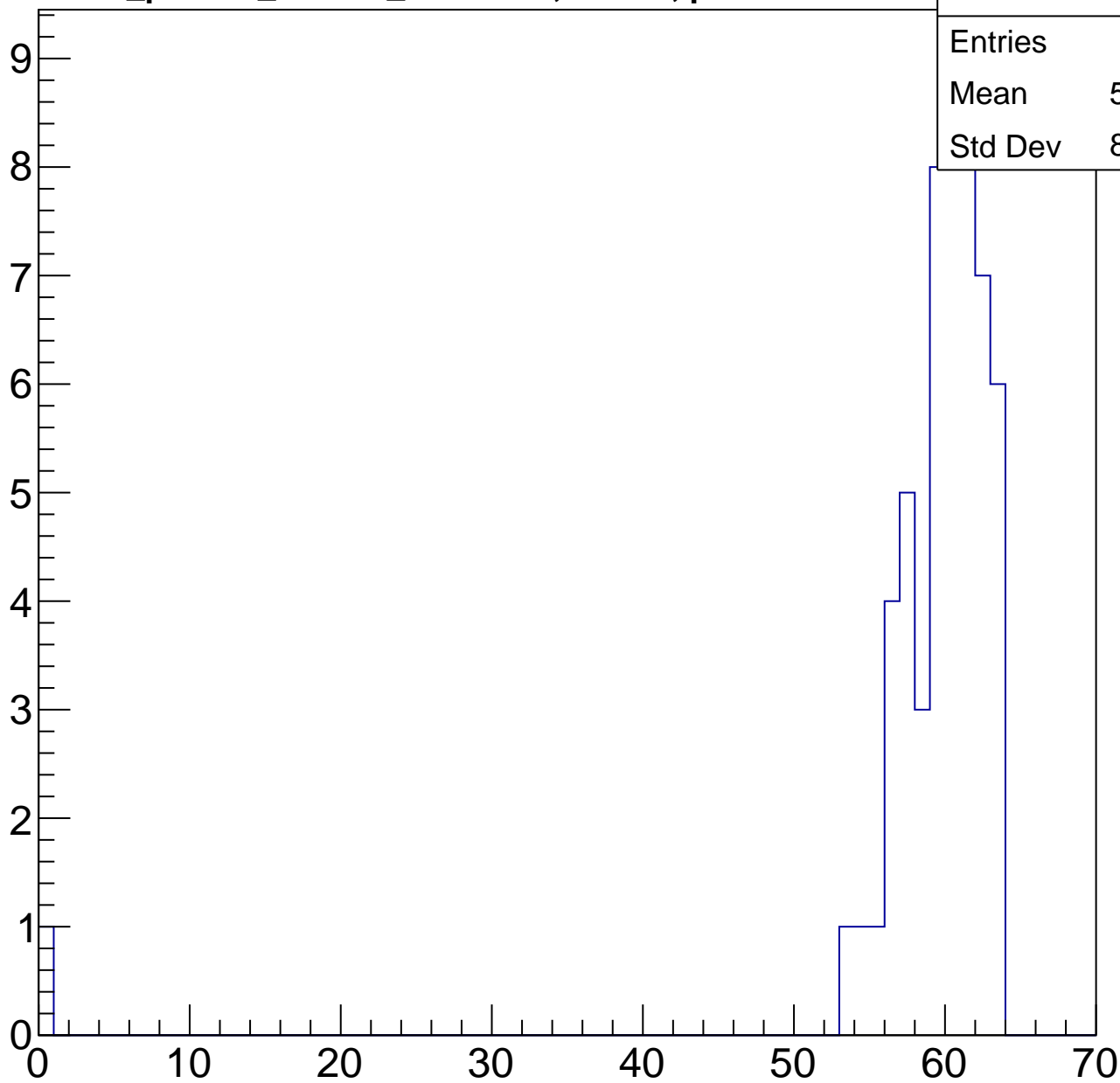
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	54
Mean	58.48
Std Dev	8.395

ampl



# B1L003S, U18-ch49, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U18-ch49, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U18-ch50, adc0

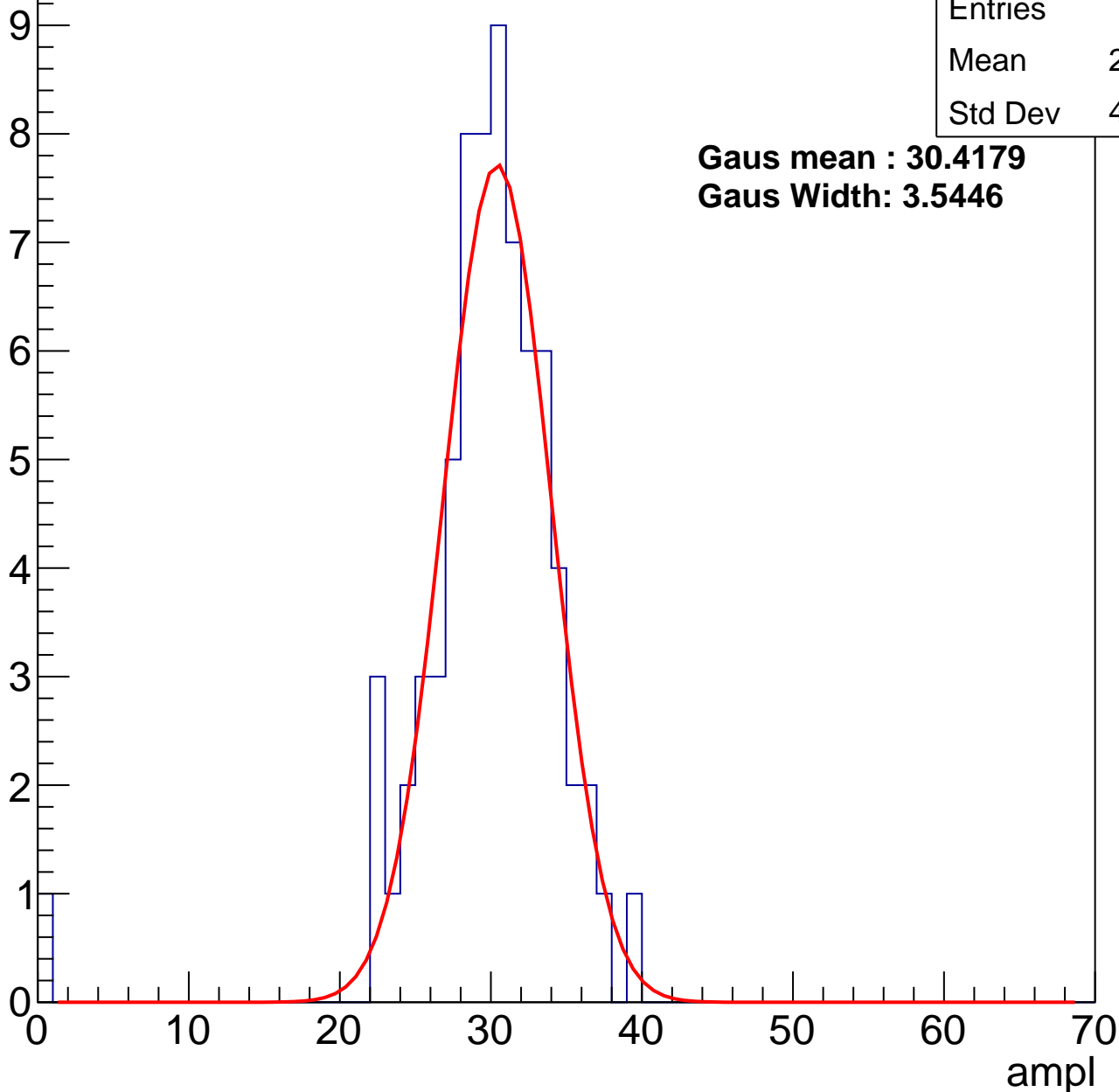
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	72
Mean	29.33
Std Dev	4.986

**Gaus mean : 30.4179**

**Gaus Width: 3.5446**



# B1L003S, U18-ch50, adc1

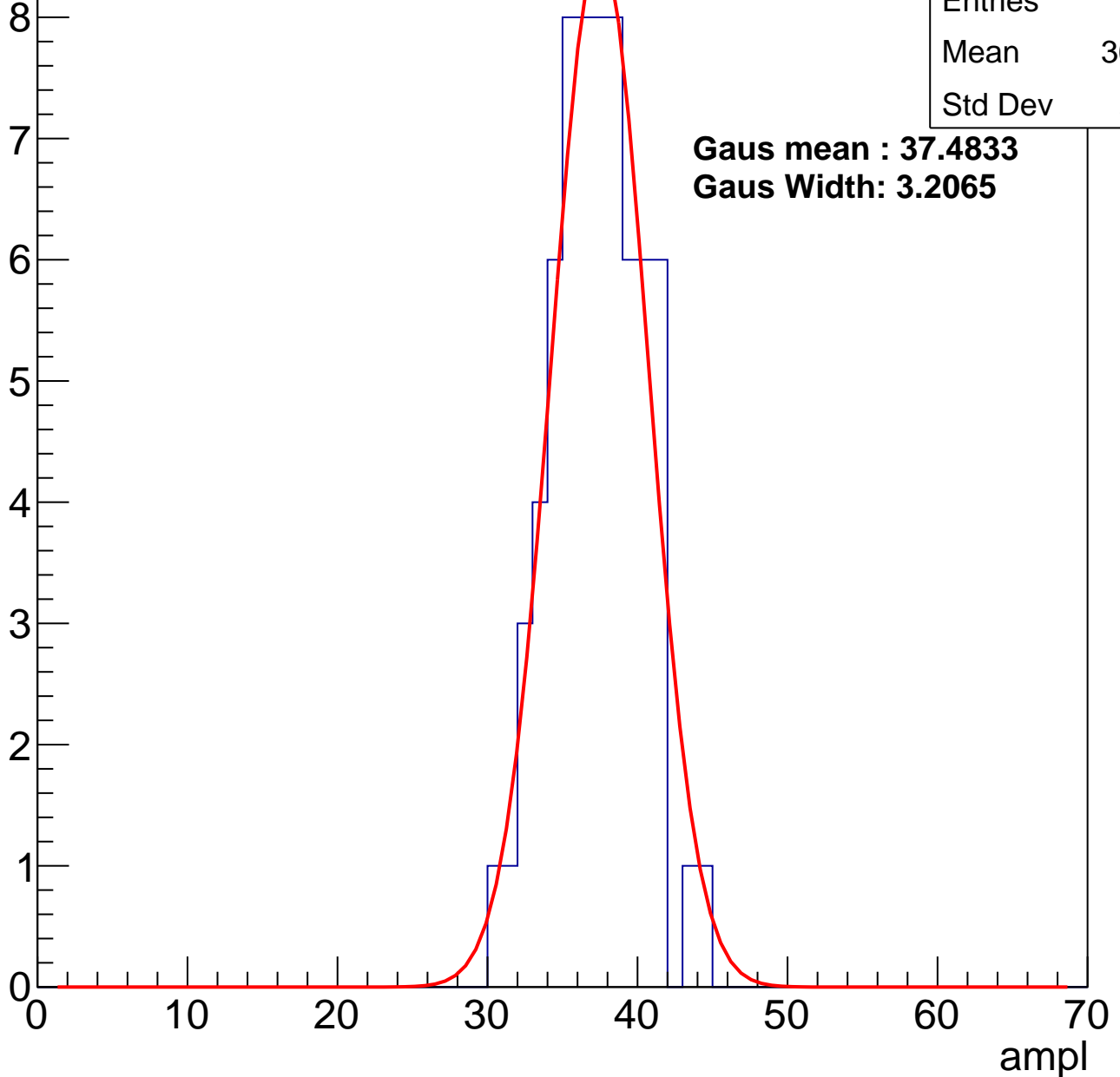
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	67
Mean	36.84
Std Dev	2.95

**Gaus mean : 37.4833**

**Gaus Width: 3.2065**



# B1L003S, U18-ch50, adc2

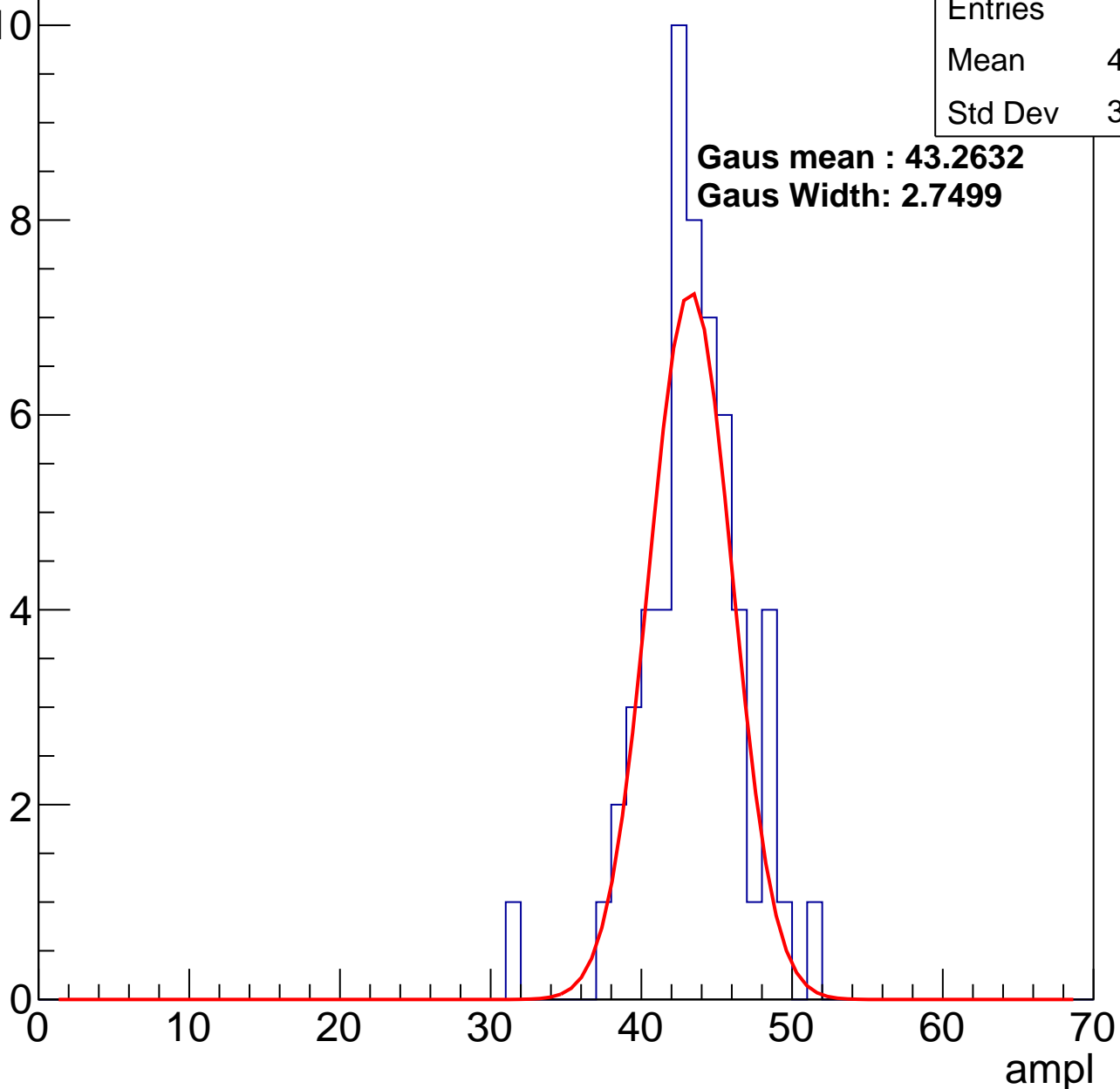
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	57
Mean	42.98
Std Dev	3.306

**Gaus mean : 43.2632**

**Gaus Width: 2.7499**

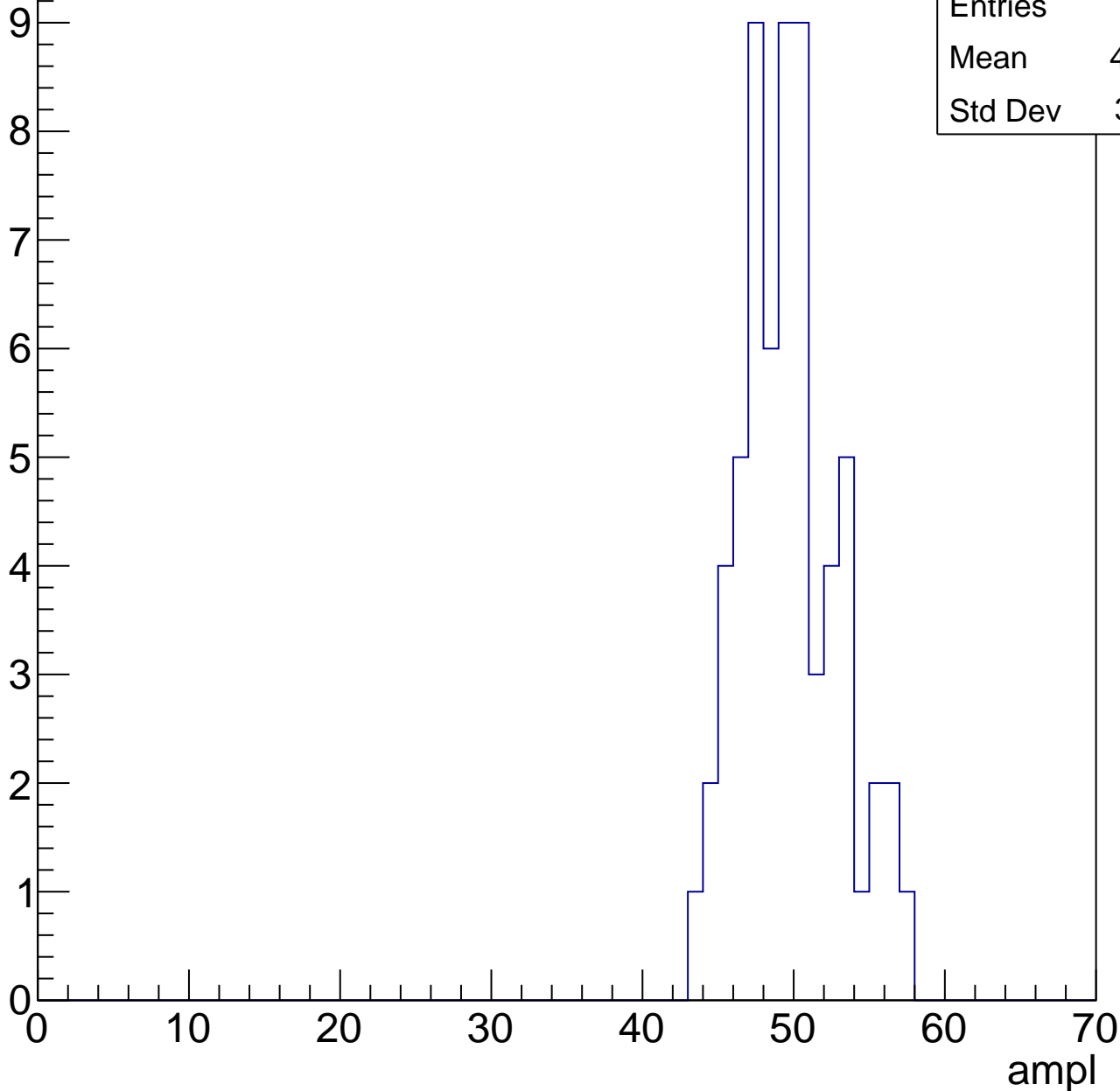


# B1L003S, U18-ch50, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	63
Mean	49.24
Std Dev	3.161

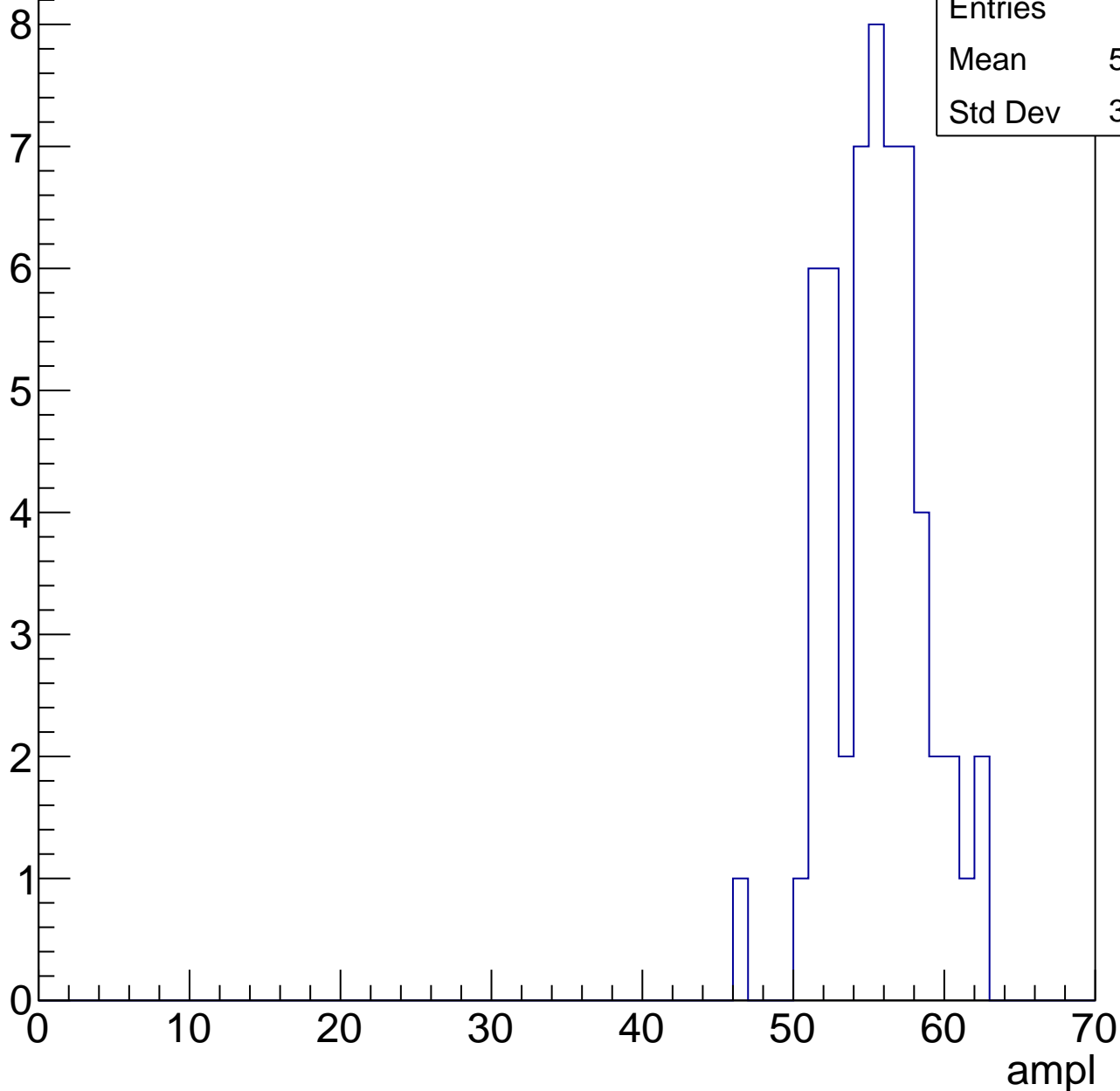


# B1L003S, U18-ch50, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	56
Mean	55.07
Std Dev	3.156

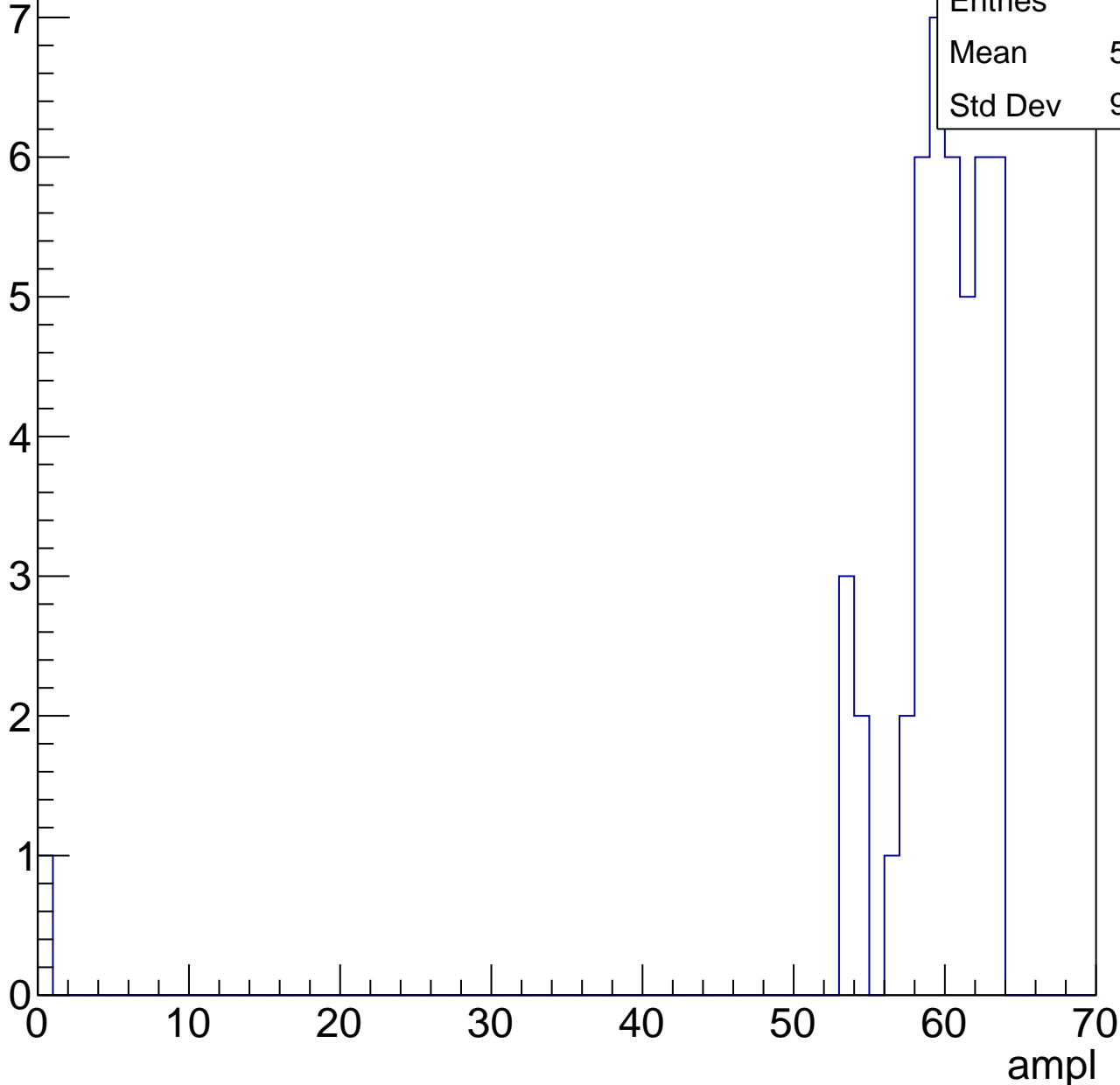


# B1L003S, U18-ch50, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

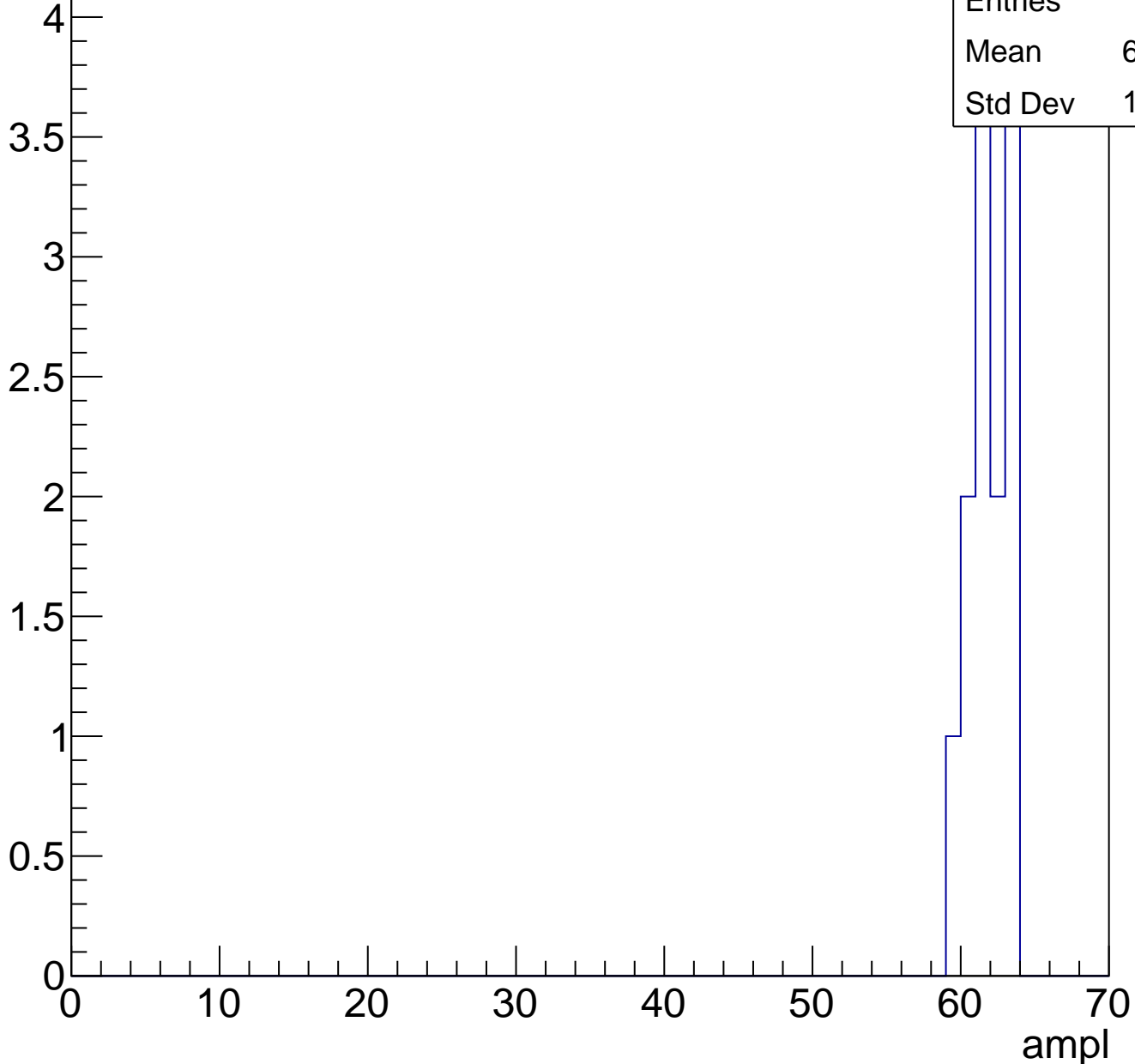
Entries	45
Mean	58.07
Std Dev	9.188



# B1L003S, U18-ch50, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	13
Mean	61.46
Std Dev	1.278



# B1L003S, U18-ch50, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch51, adc0

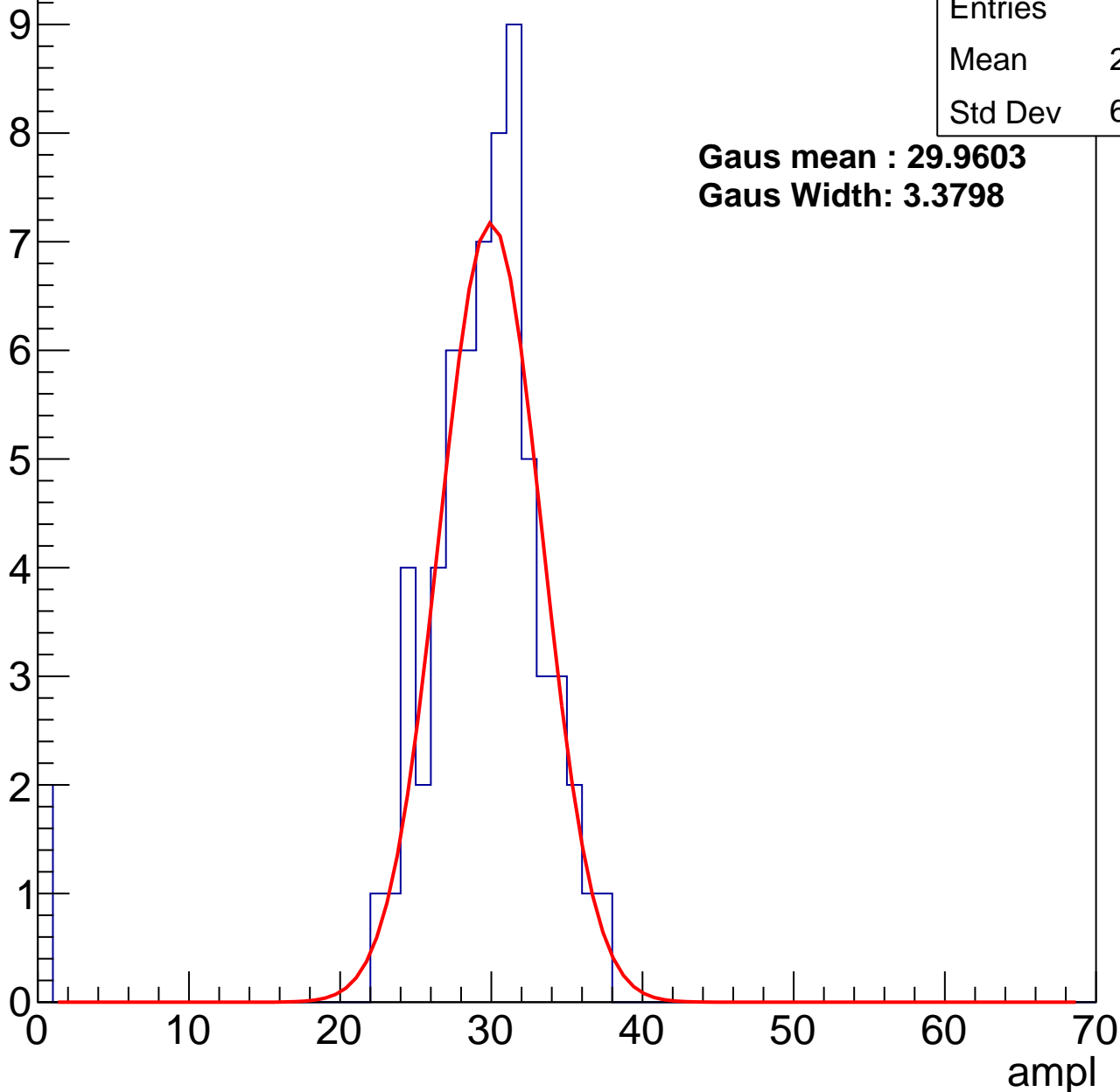
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	65
Mean	28.48
Std Dev	6.005

**Gaus mean : 29.9603**

**Gaus Width: 3.3798**



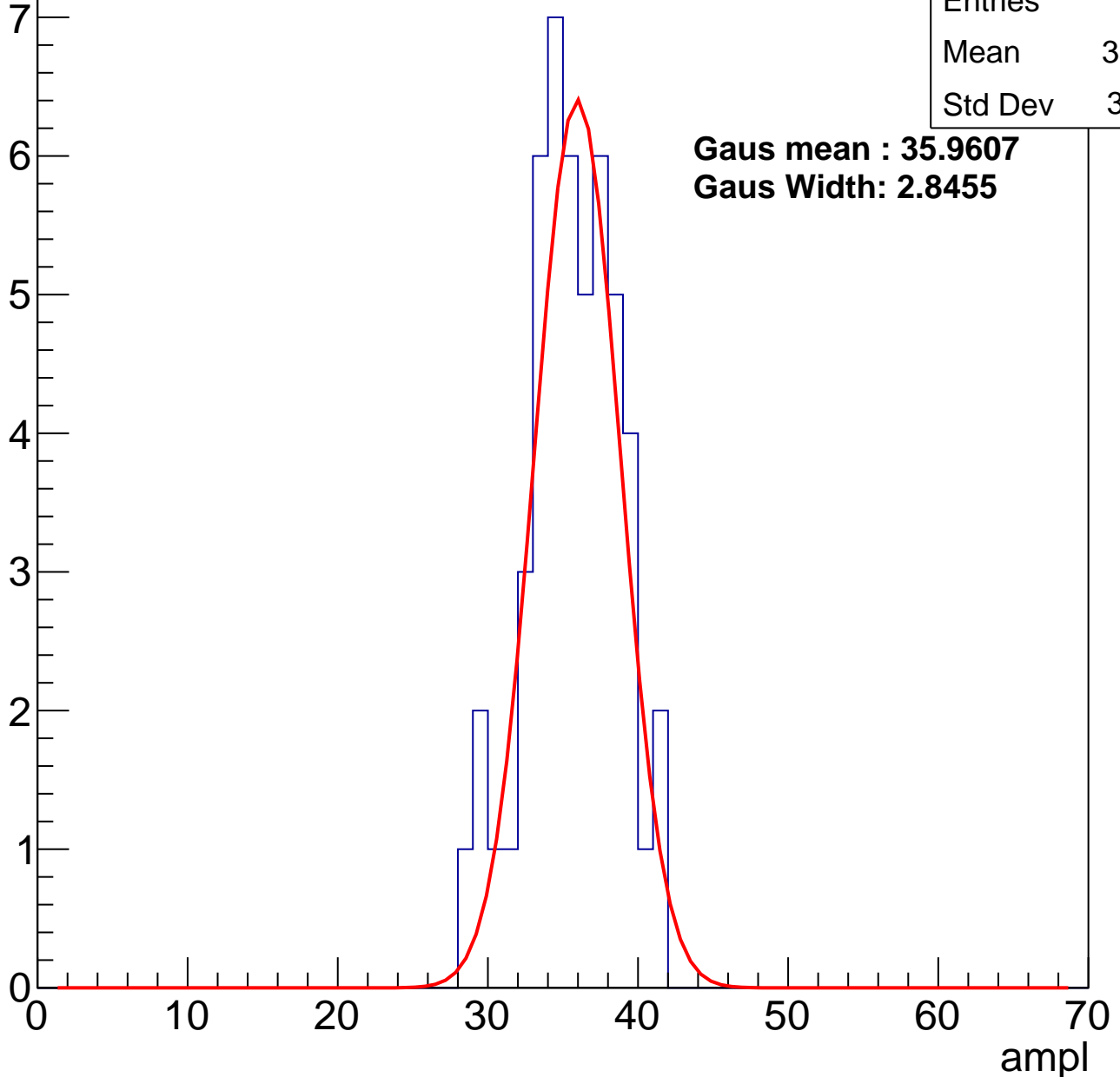
# B1L003S, U18-ch51, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	50
Mean	35.18
Std Dev	3.011

**Gaus mean : 35.9607**  
**Gaus Width: 2.8455**



# B1L003S, U18-ch51, adc2

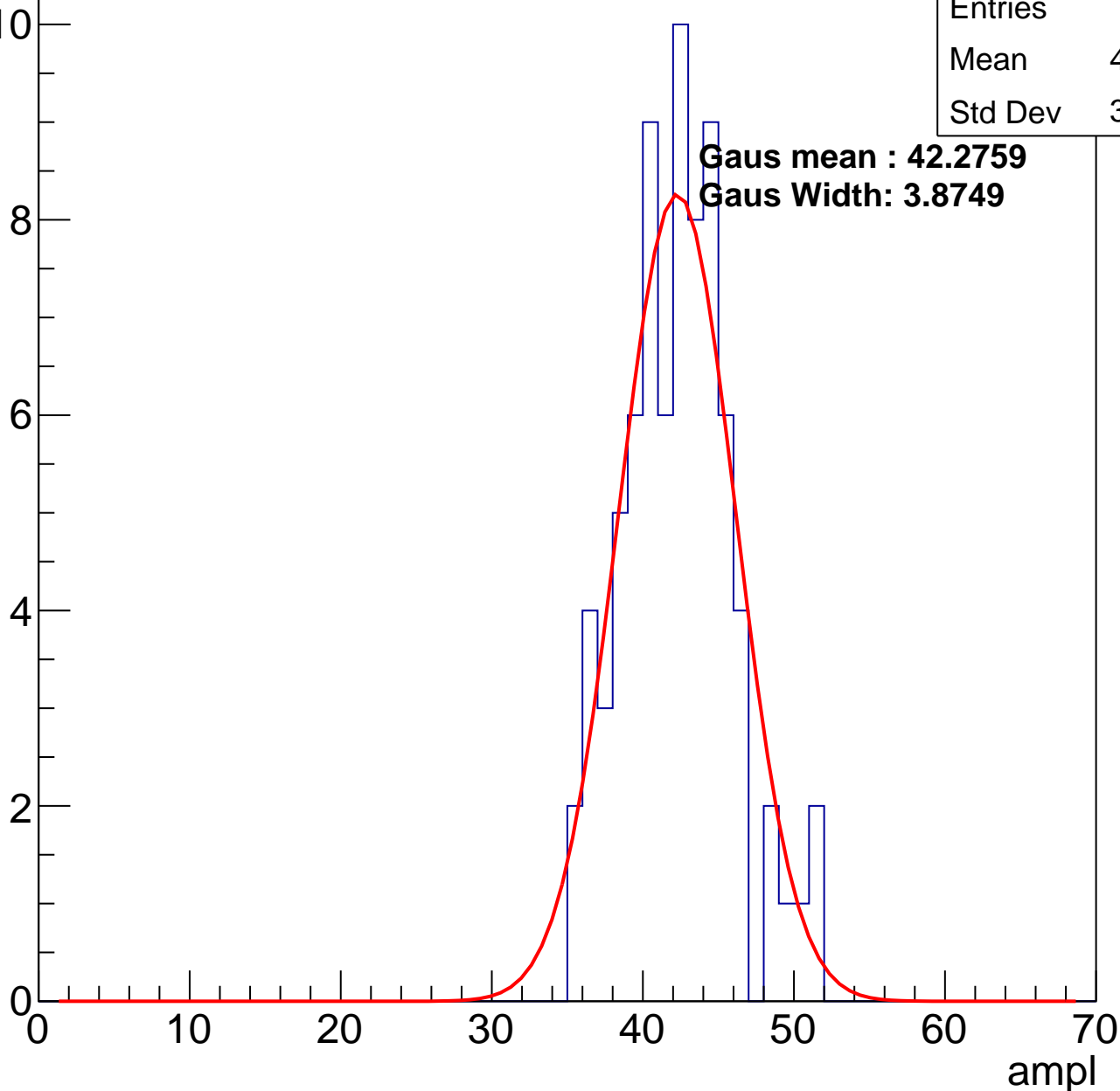
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	78
Mean	41.87
Std Dev	3.582

**Gaus mean : 42.2759**

**Gaus Width: 3.8749**

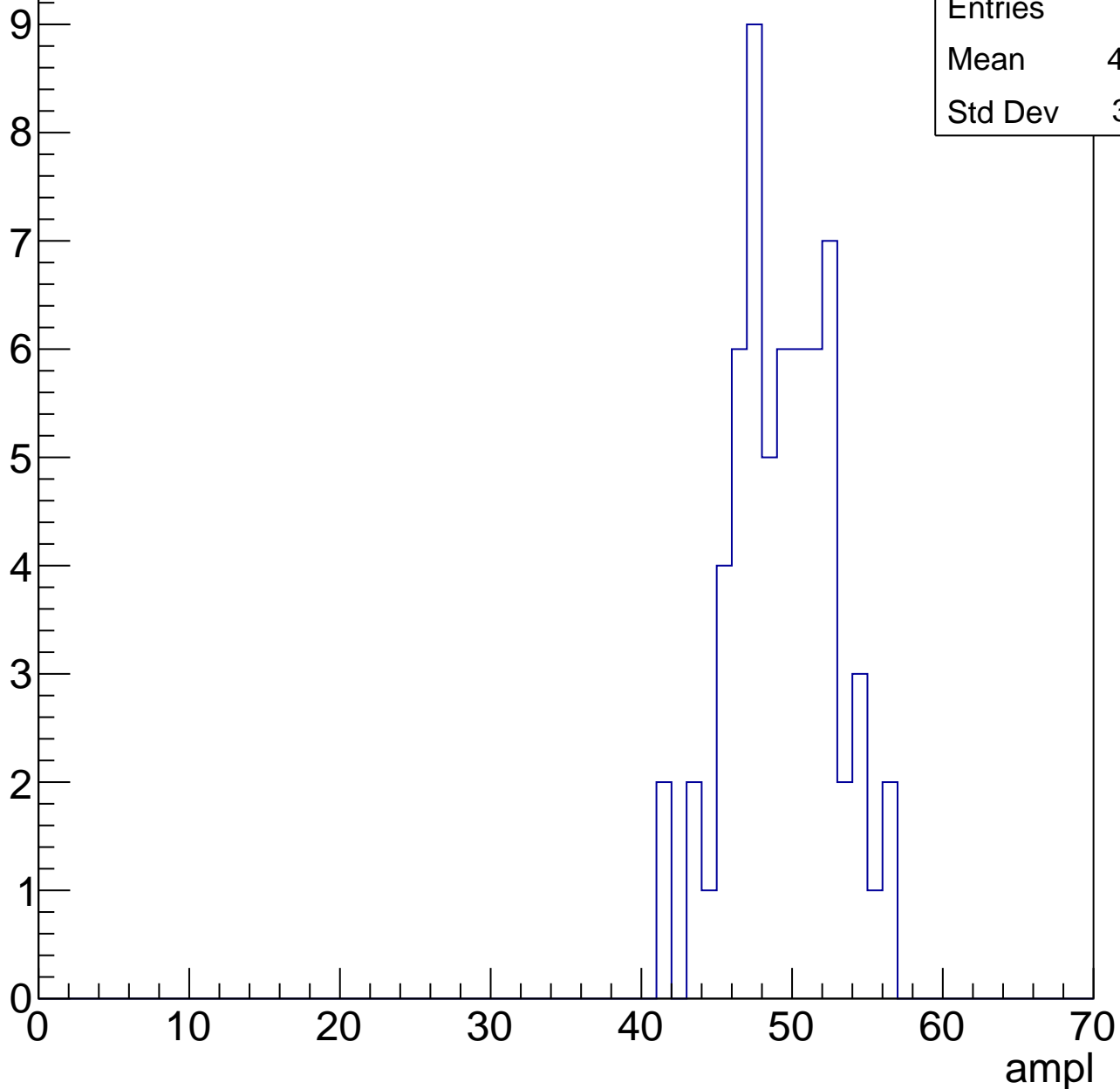


# B1L003S, U18-ch51, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	62
Mean	48.87
Std Dev	3.401

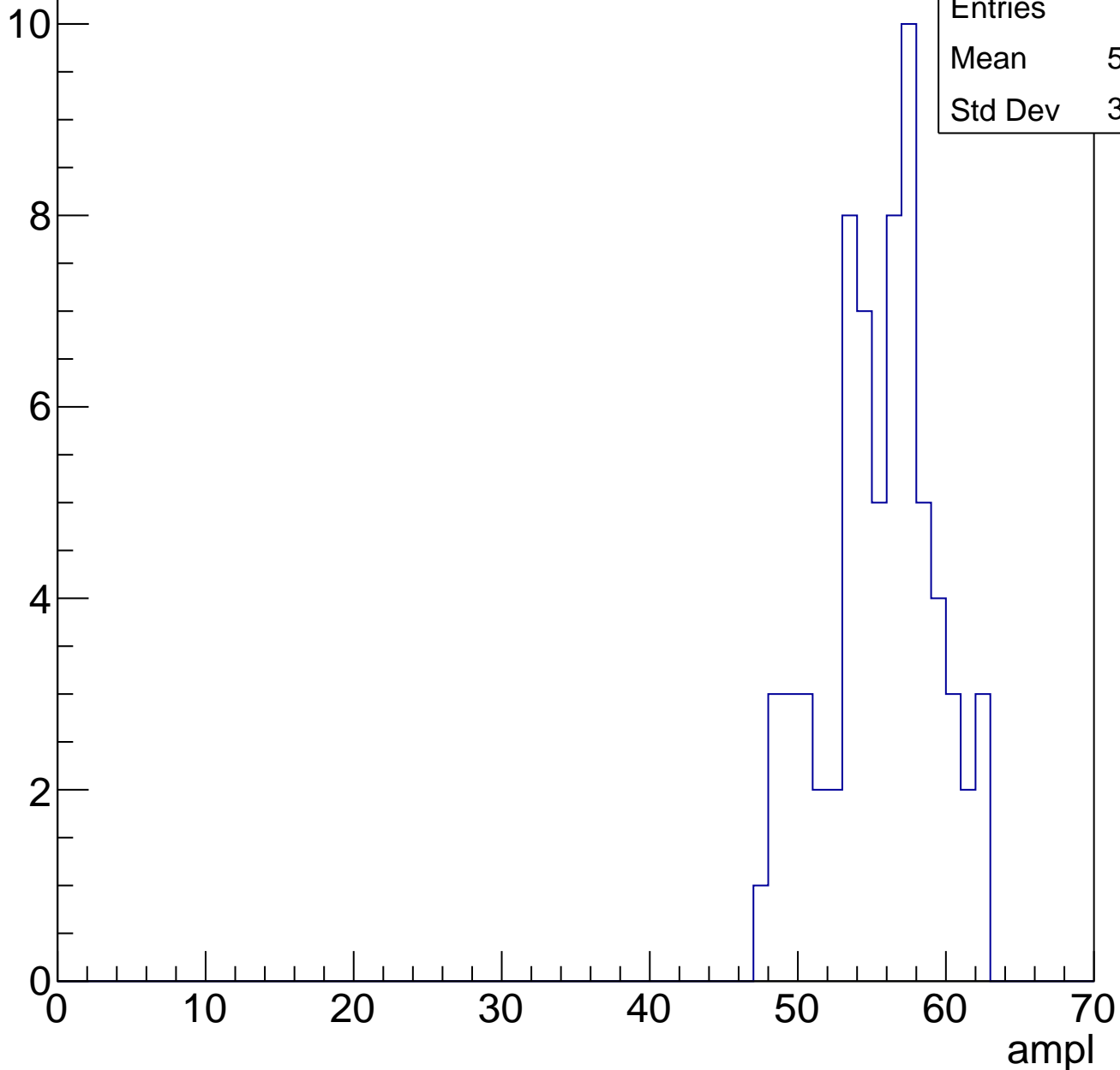


# B1L003S, U18-ch51, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	69
Mean	55.12
Std Dev	3.677

Entry

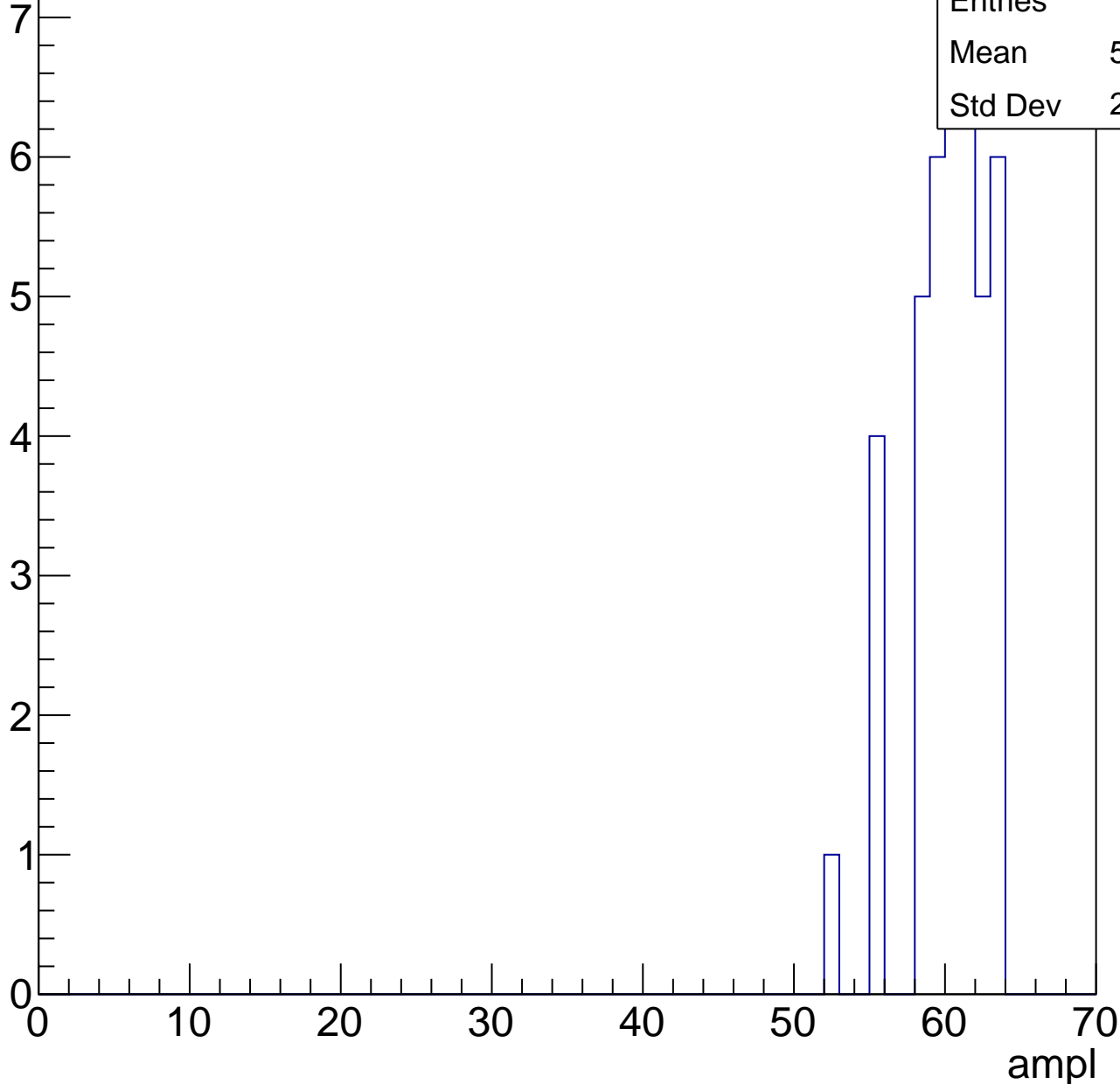


# B1L003S, U18-ch51, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

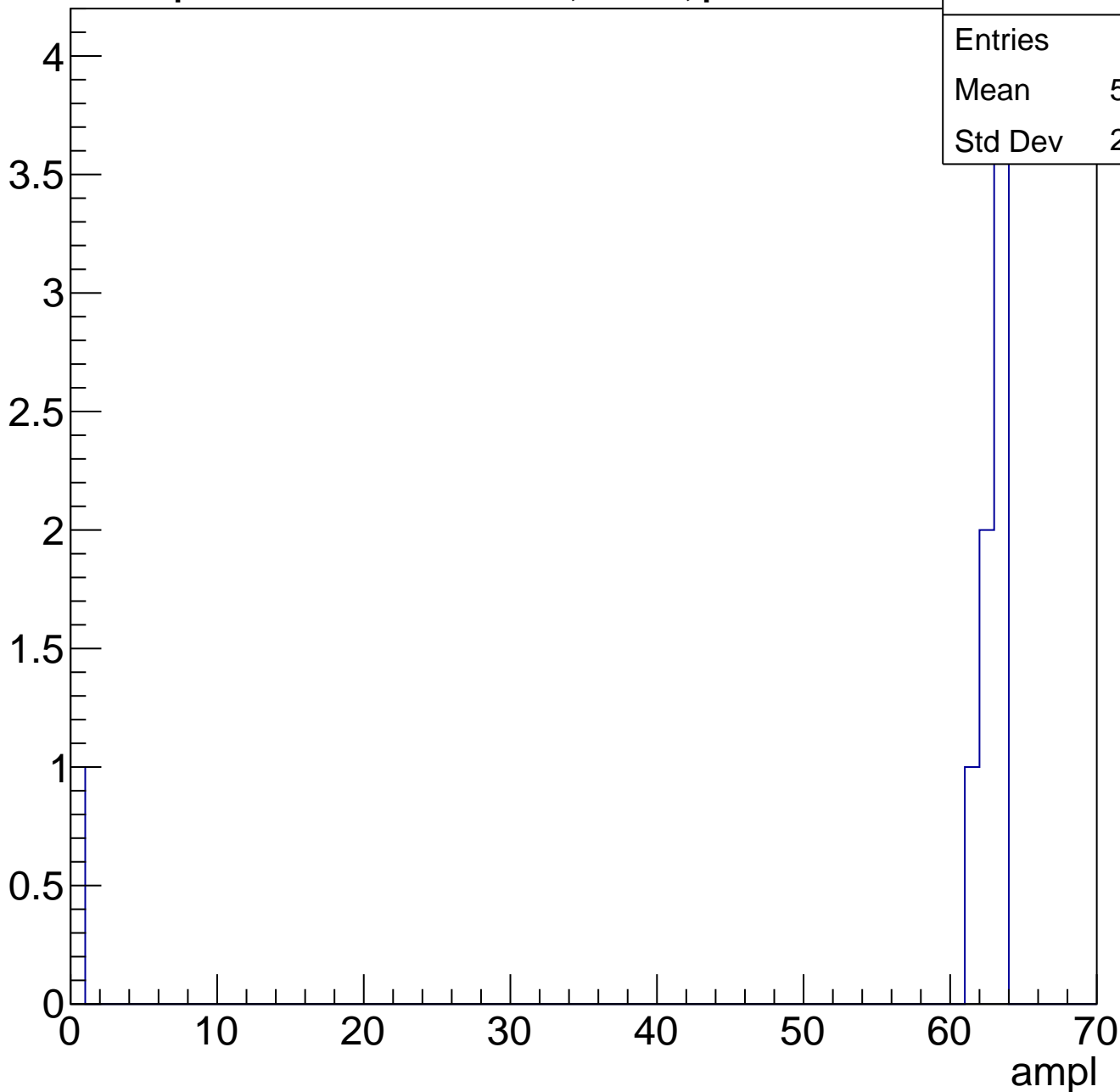
Entries	41
Mean	59.78
Std Dev	2.562



# B1L003S, U18-ch51, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U18-ch51, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U18-ch52, adc0

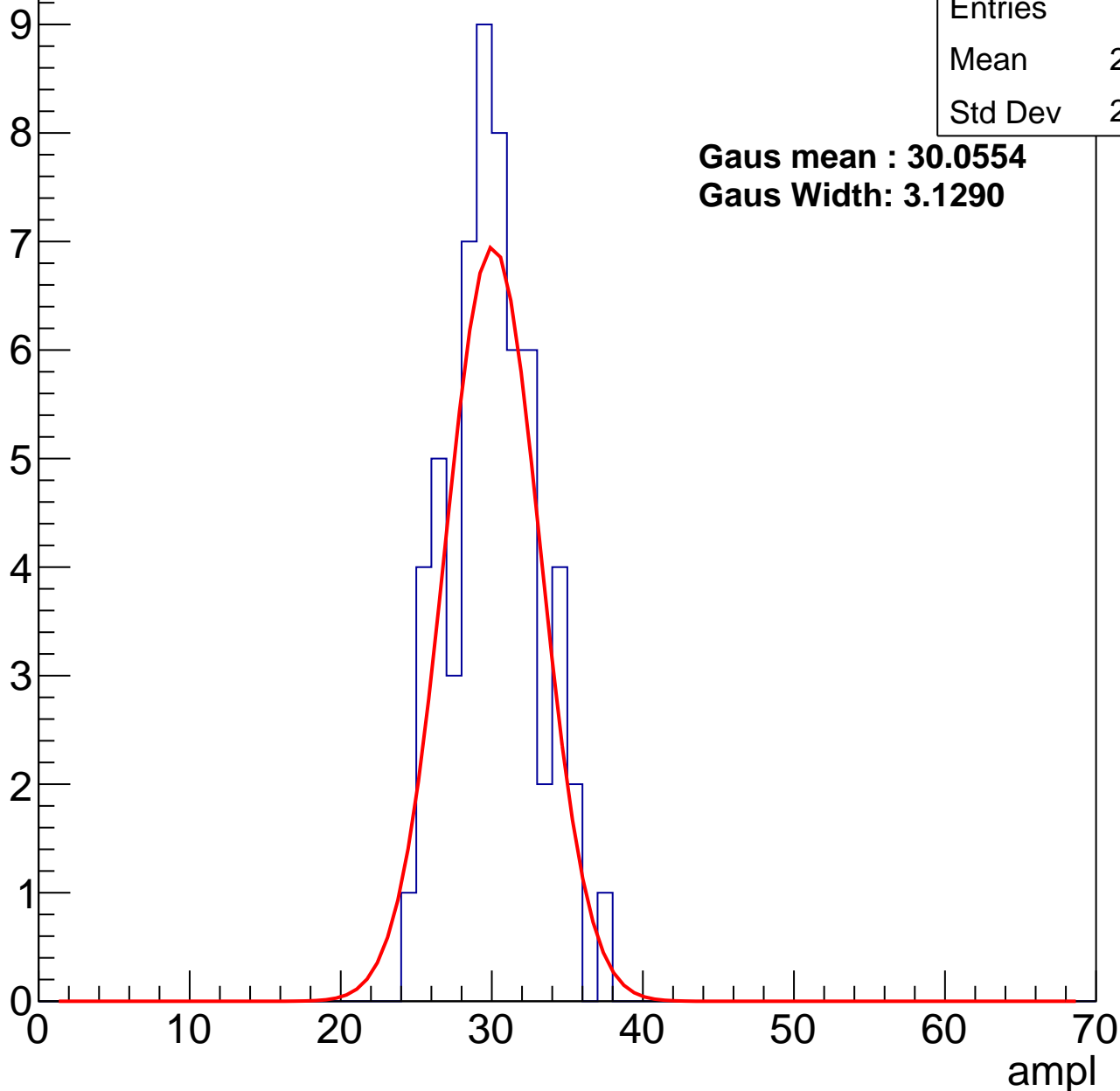
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	58
Mean	29.64
Std Dev	2.887

**Gaus mean : 30.0554**

**Gaus Width: 3.1290**



# B1L003S, U18-ch52, adc1

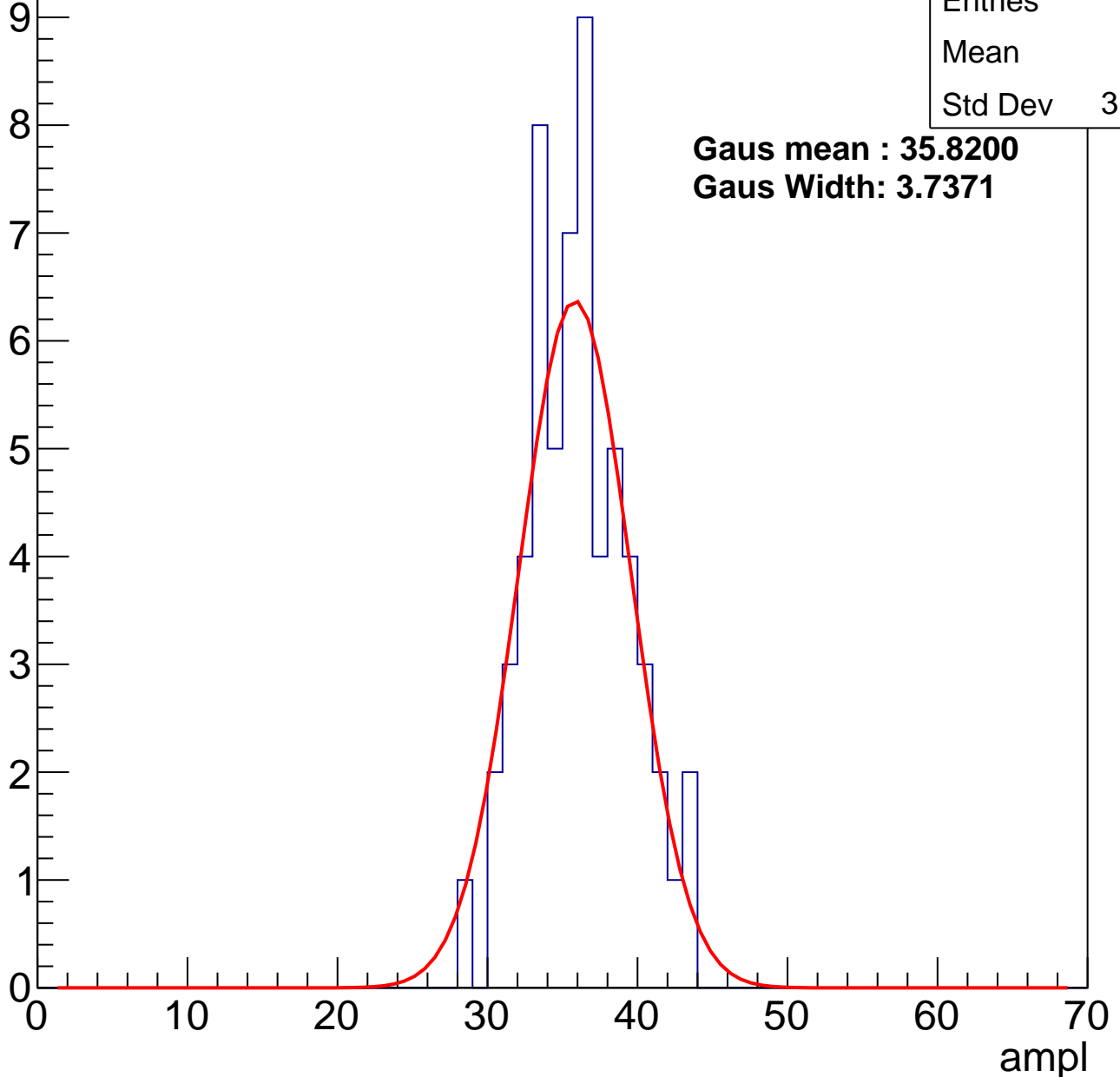
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	60
Mean	35.6
Std Dev	3.308

**Gaus mean : 35.8200**

**Gaus Width: 3.7371**



# B1L003S, U18-ch52, adc2

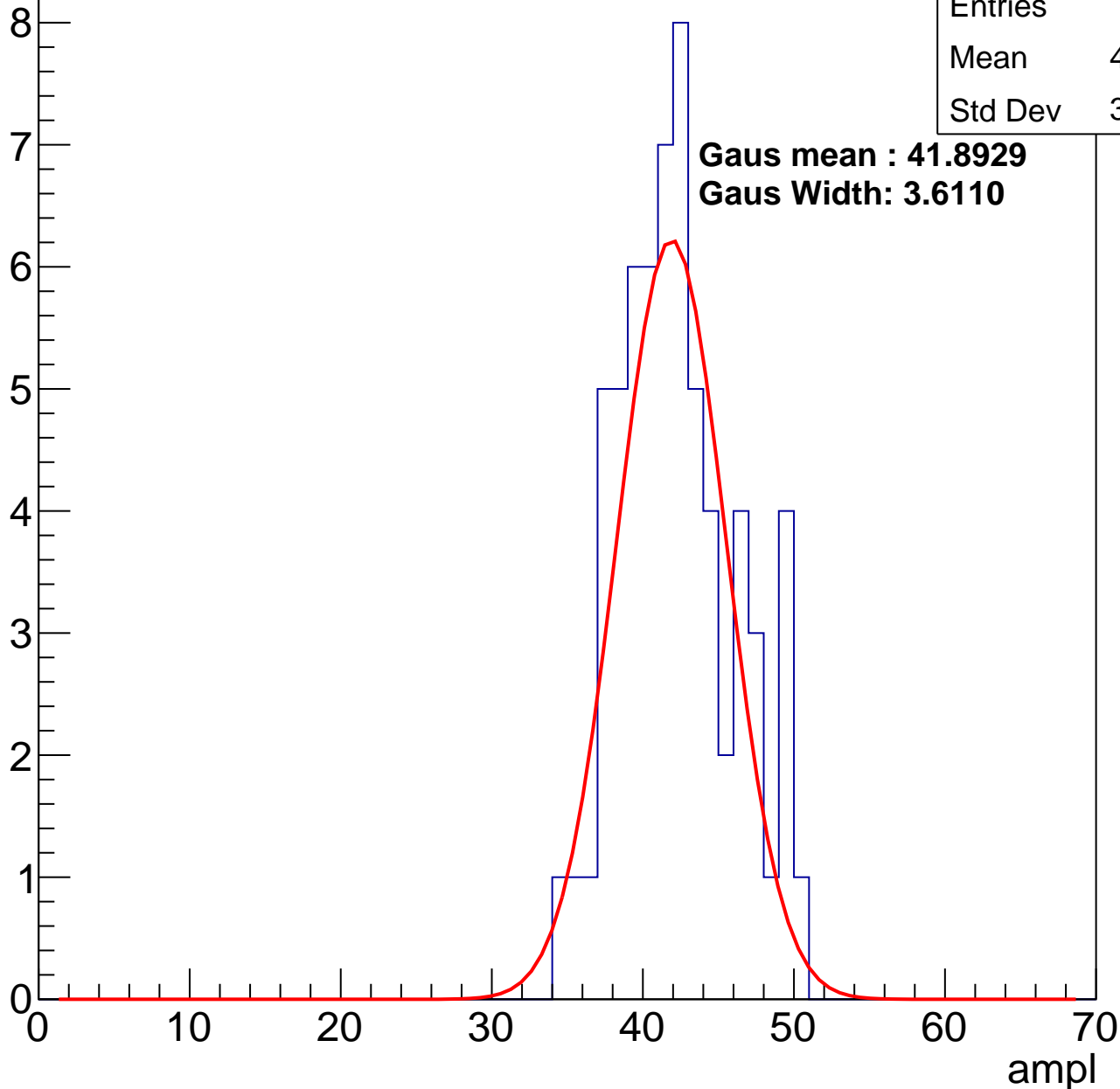
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	64
Mean	41.83
Std Dev	3.773

**Gaus mean : 41.8929**

**Gaus Width: 3.6110**

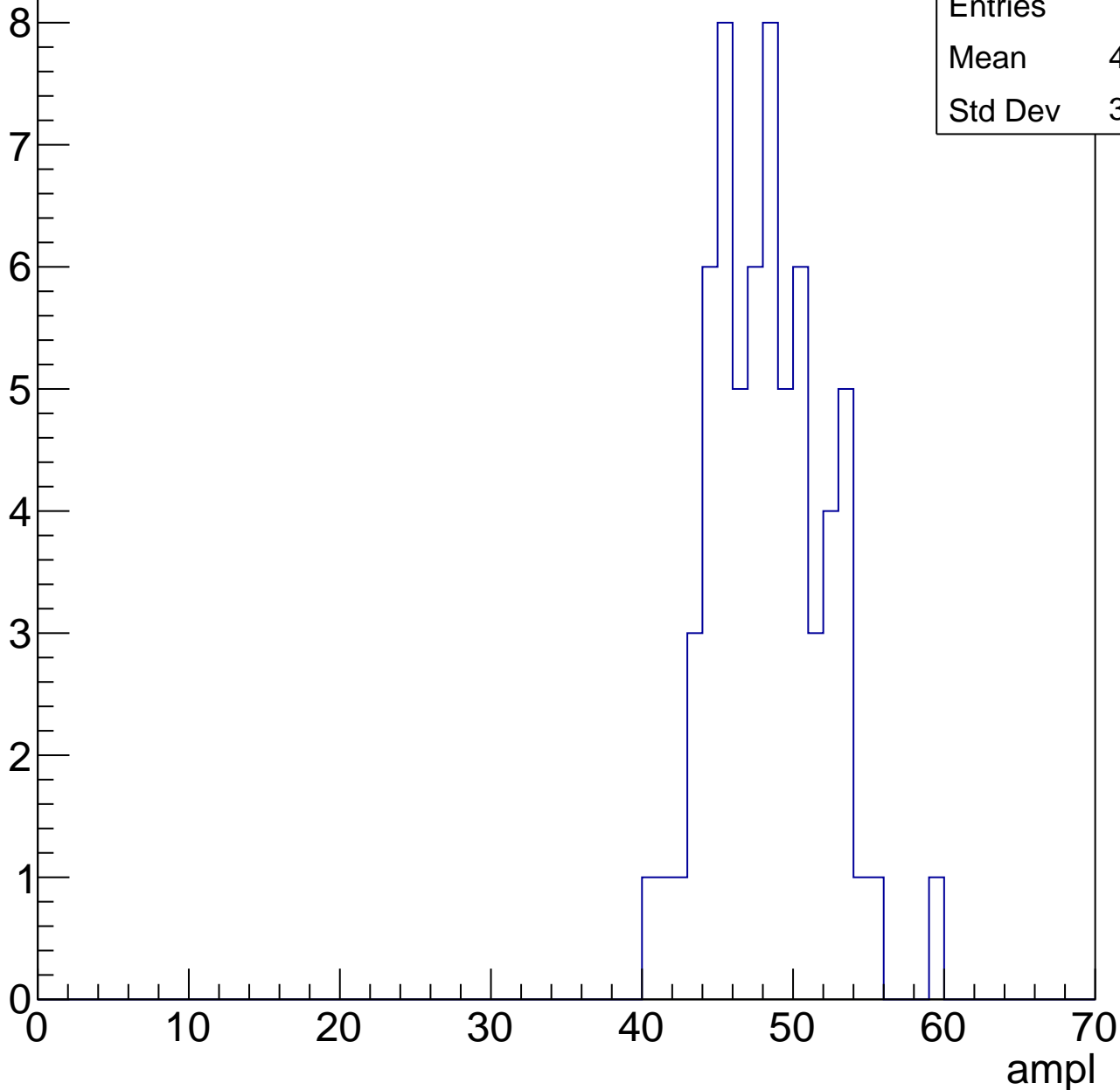


# B1L003S, U18-ch52, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	65
Mean	47.86
Std Dev	3.654

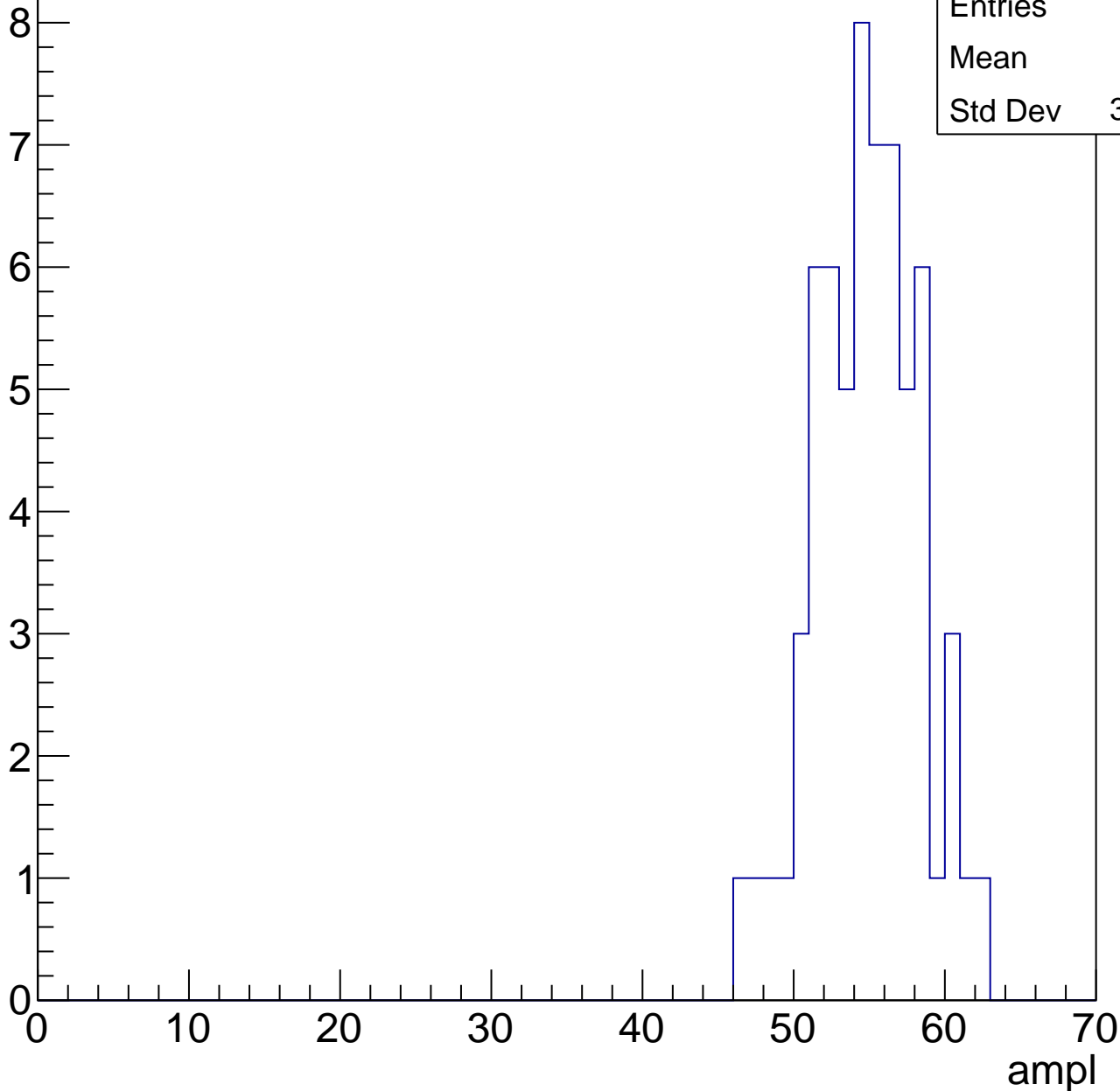


# B1L003S, U18-ch52, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	63
Mean	54.4
Std Dev	3.374



# B1L003S, U18-ch52, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	53
Mean	59.75
Std Dev	2.781

Entry

10

8

6

4

2

0

0

10

20

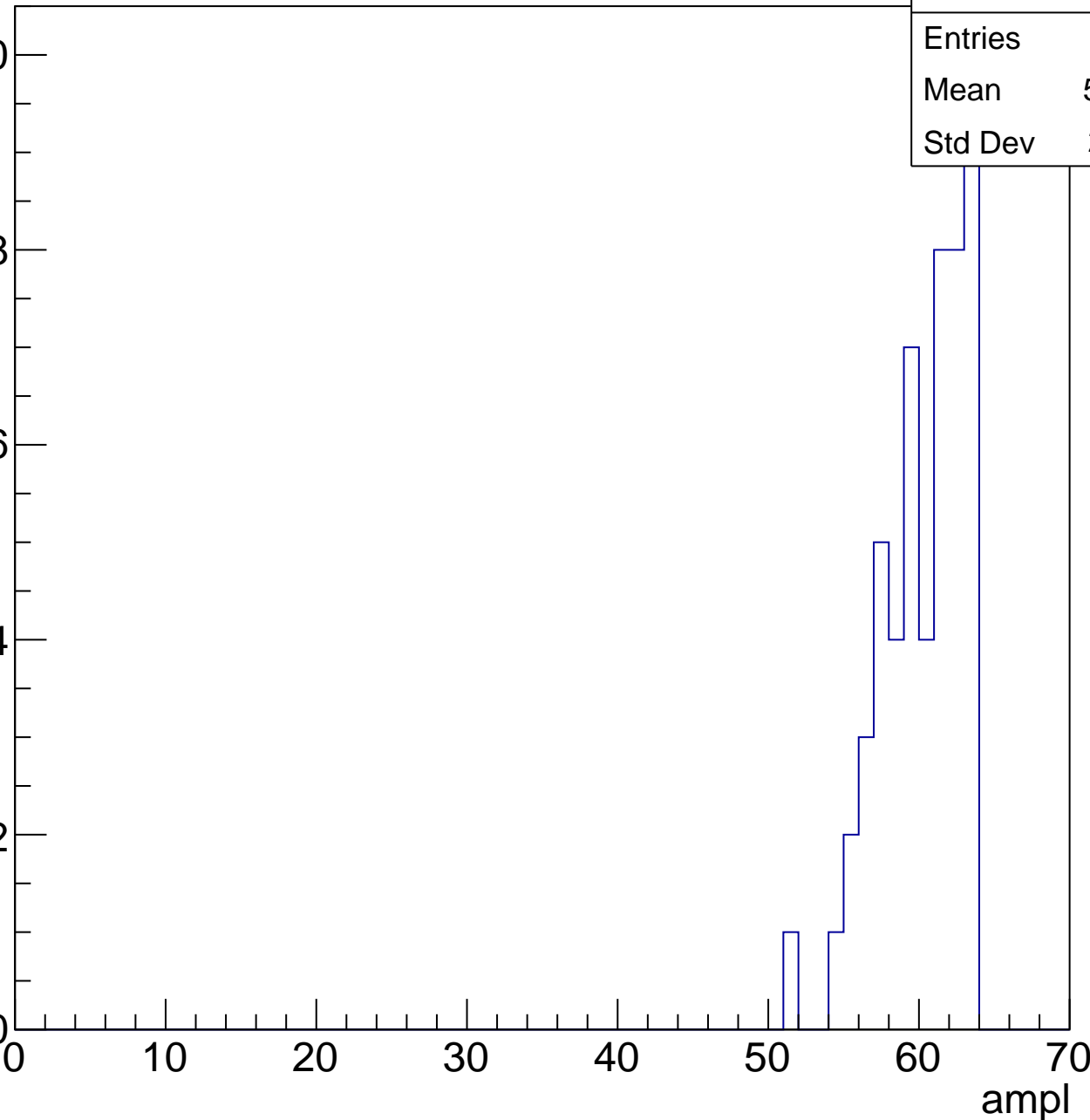
30

40

50

60

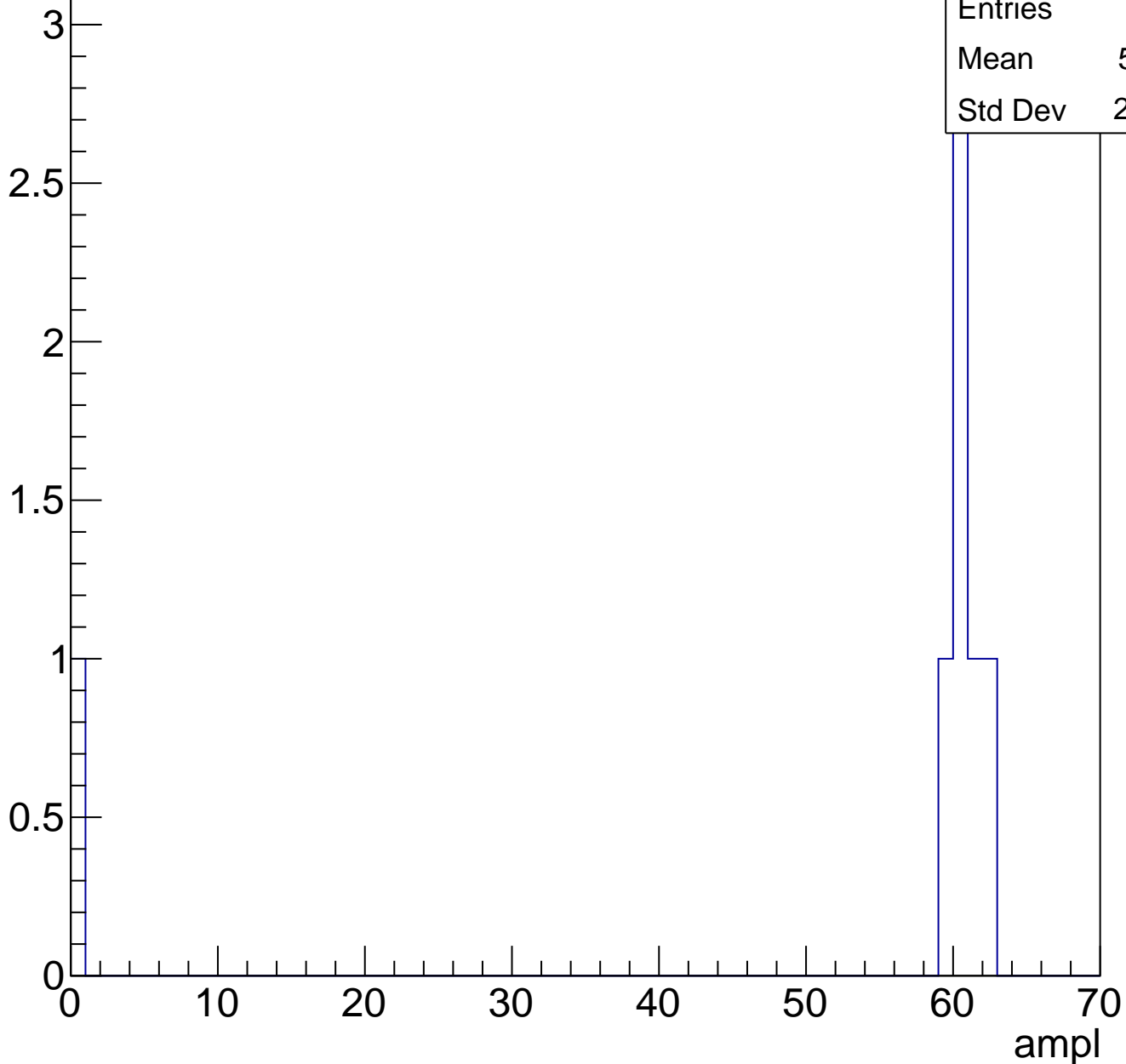
ampl



# B1L003S, U18-ch52, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	7
Mean	51.71
Std Dev	21.13



# B1L003S, U18-ch52, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

1  
0.8  
0.6  
0.4  
0.2  
0

Entries	1
Mean	24
Std Dev	0

ampl

# B1L003S, U18-ch53, adc0

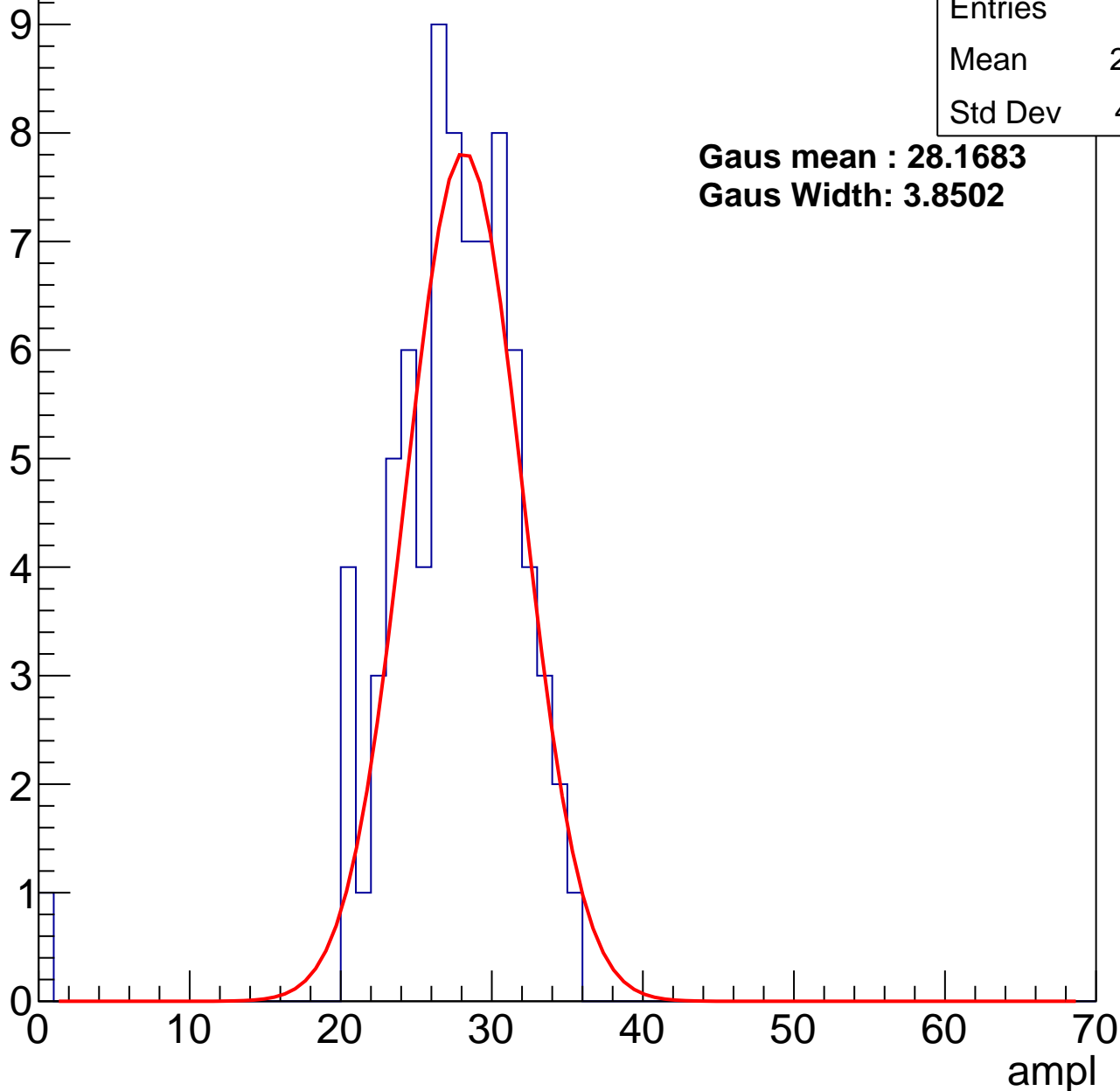
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	79
Mean	26.97
Std Dev	4.731

**Gaus mean : 28.1683**

**Gaus Width: 3.8502**



# B1L003S, U18-ch53, adc1

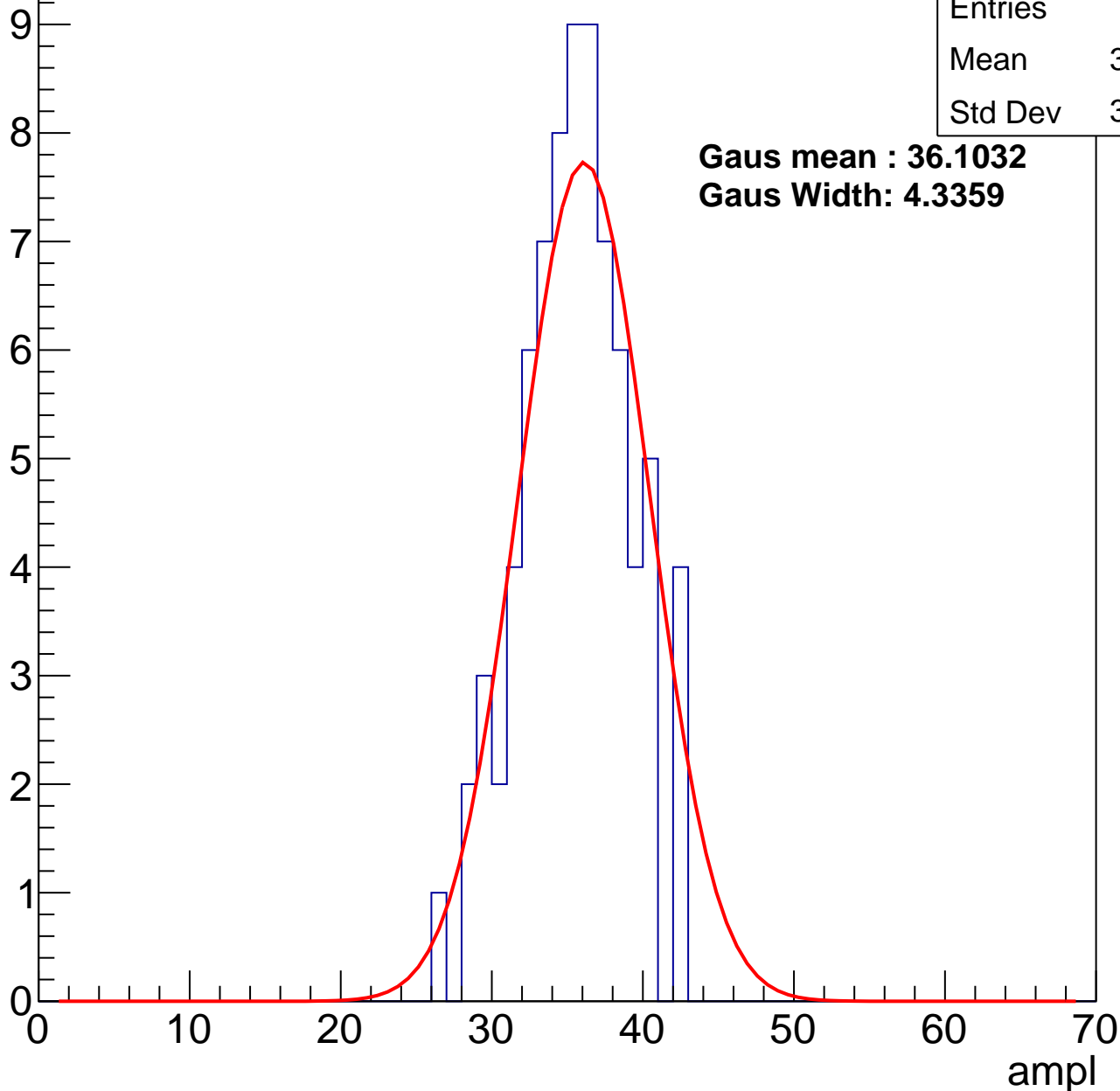
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	77
Mean	35.04
Std Dev	3.544

**Gaus mean : 36.1032**

**Gaus Width: 4.3359**



# B1L003S, U18-ch53, adc2

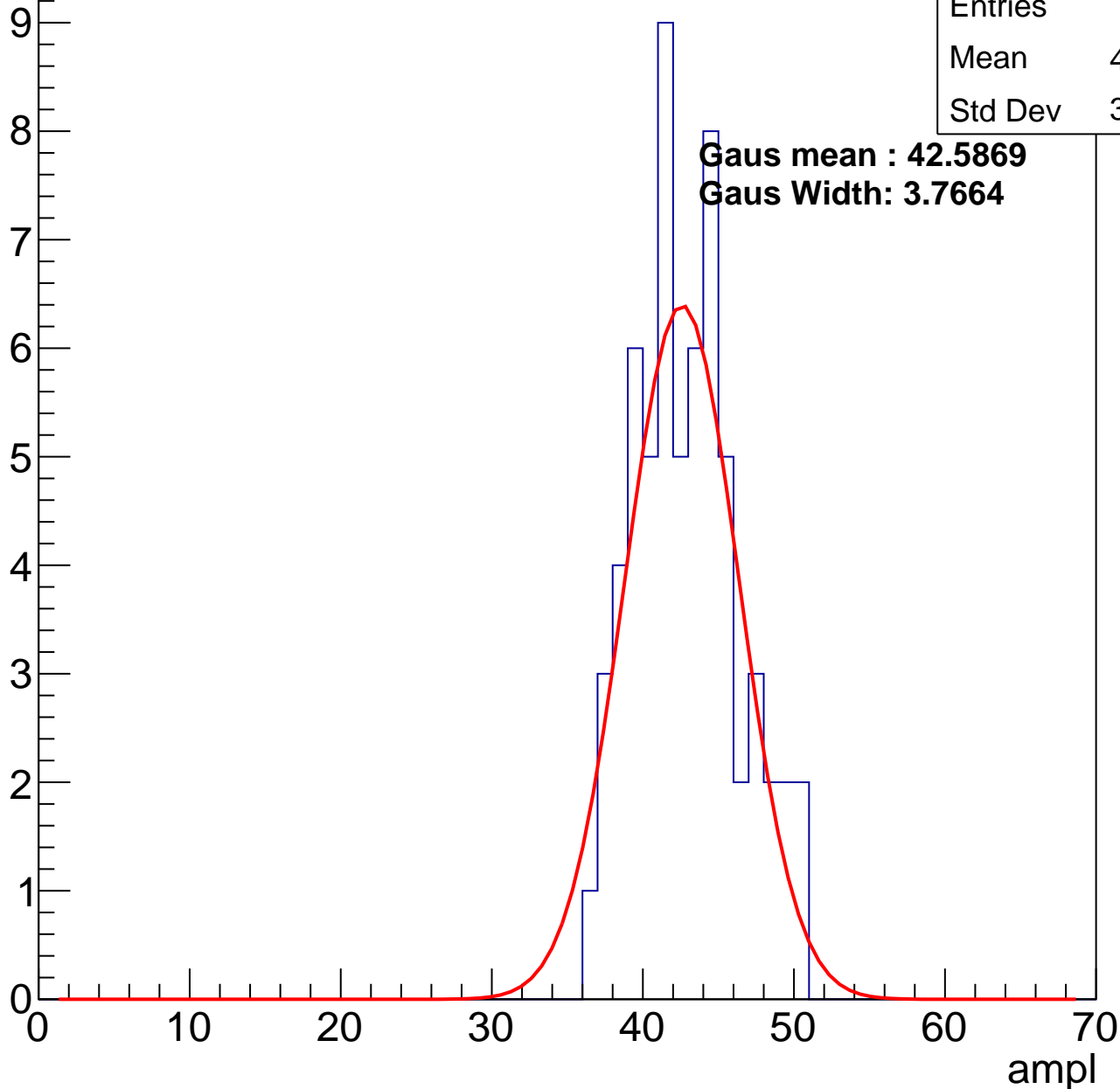
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	63
Mean	42.44
Std Dev	3.412

**Gaus mean : 42.5869**

**Gaus Width: 3.7664**

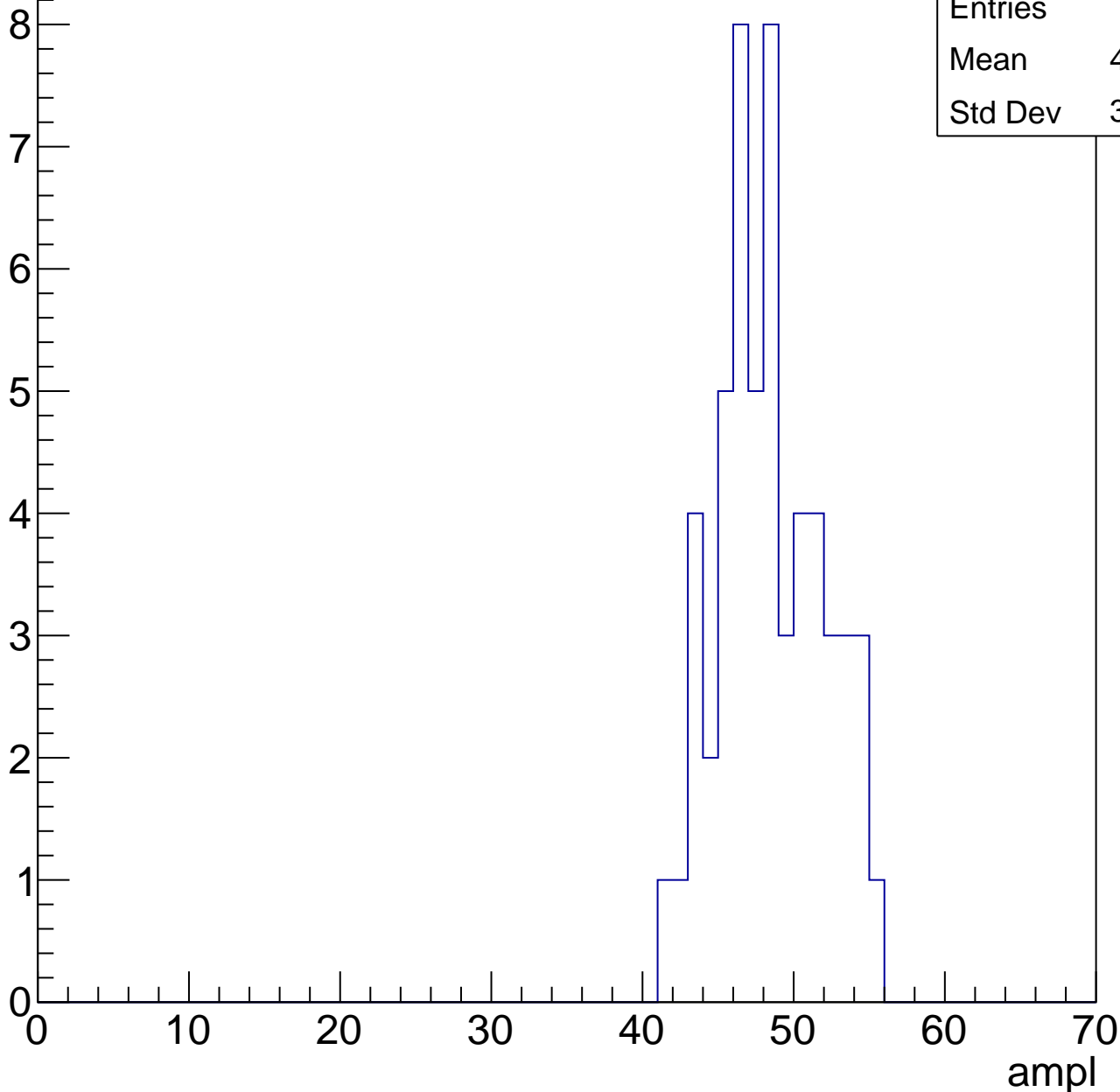


# B1L003S, U18-ch53, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

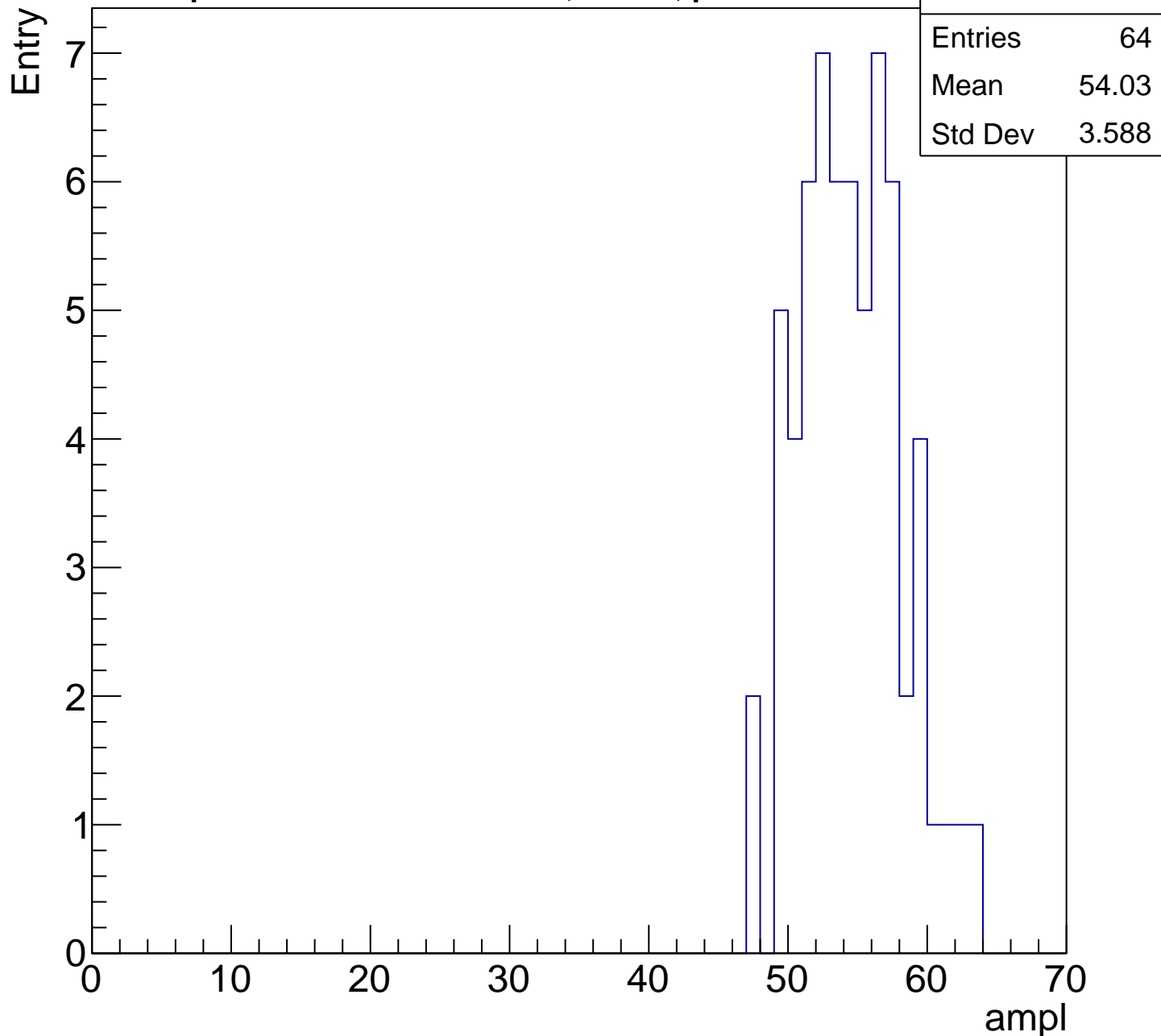
Entry

Entries	55
Mean	47.96
Std Dev	3.395



# B1L003S, U18-ch53, adc4

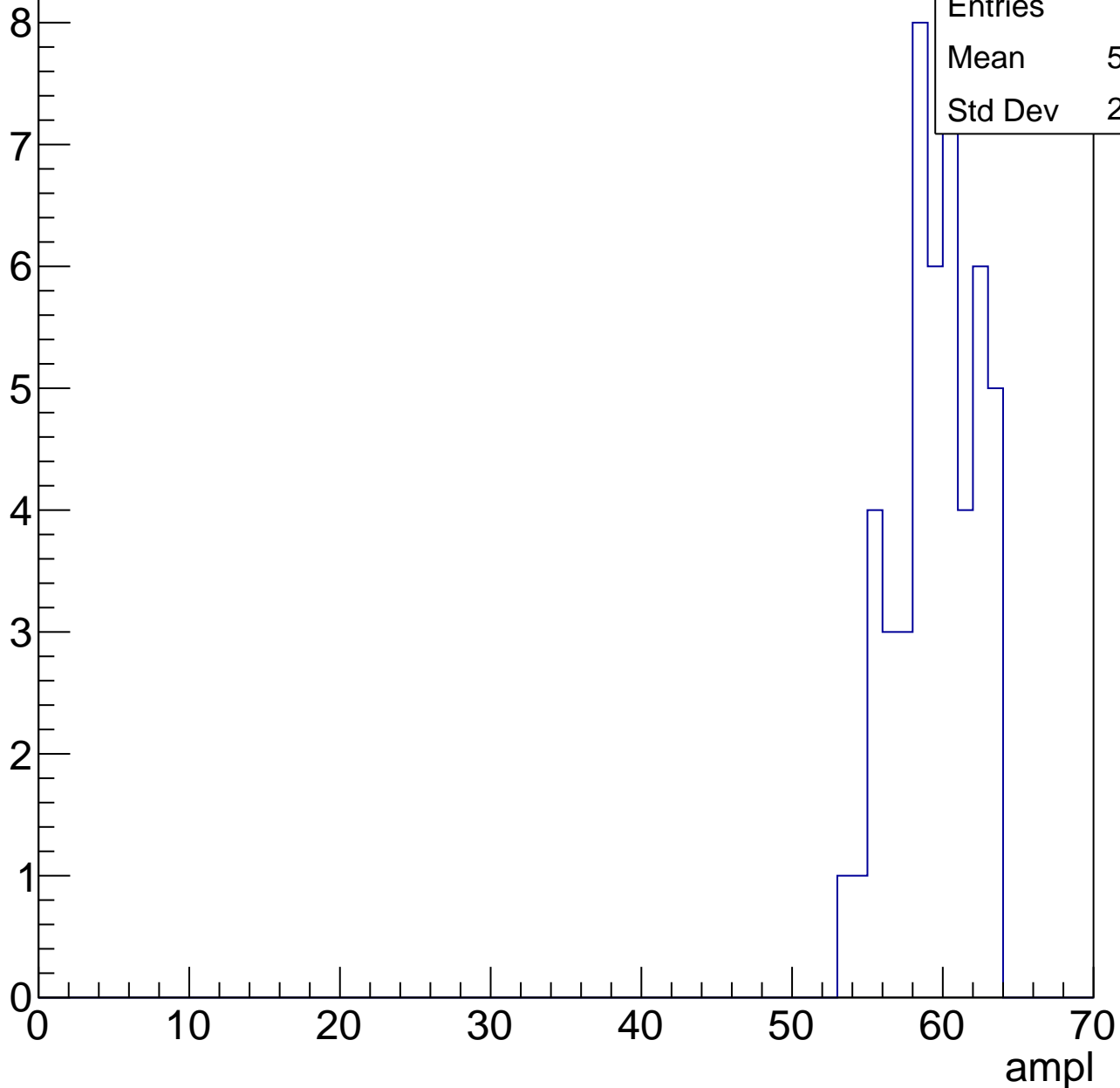
calib\_packv5\_042523\_0143.root, FC#13, port D2



# B1L003S, U18-ch53, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

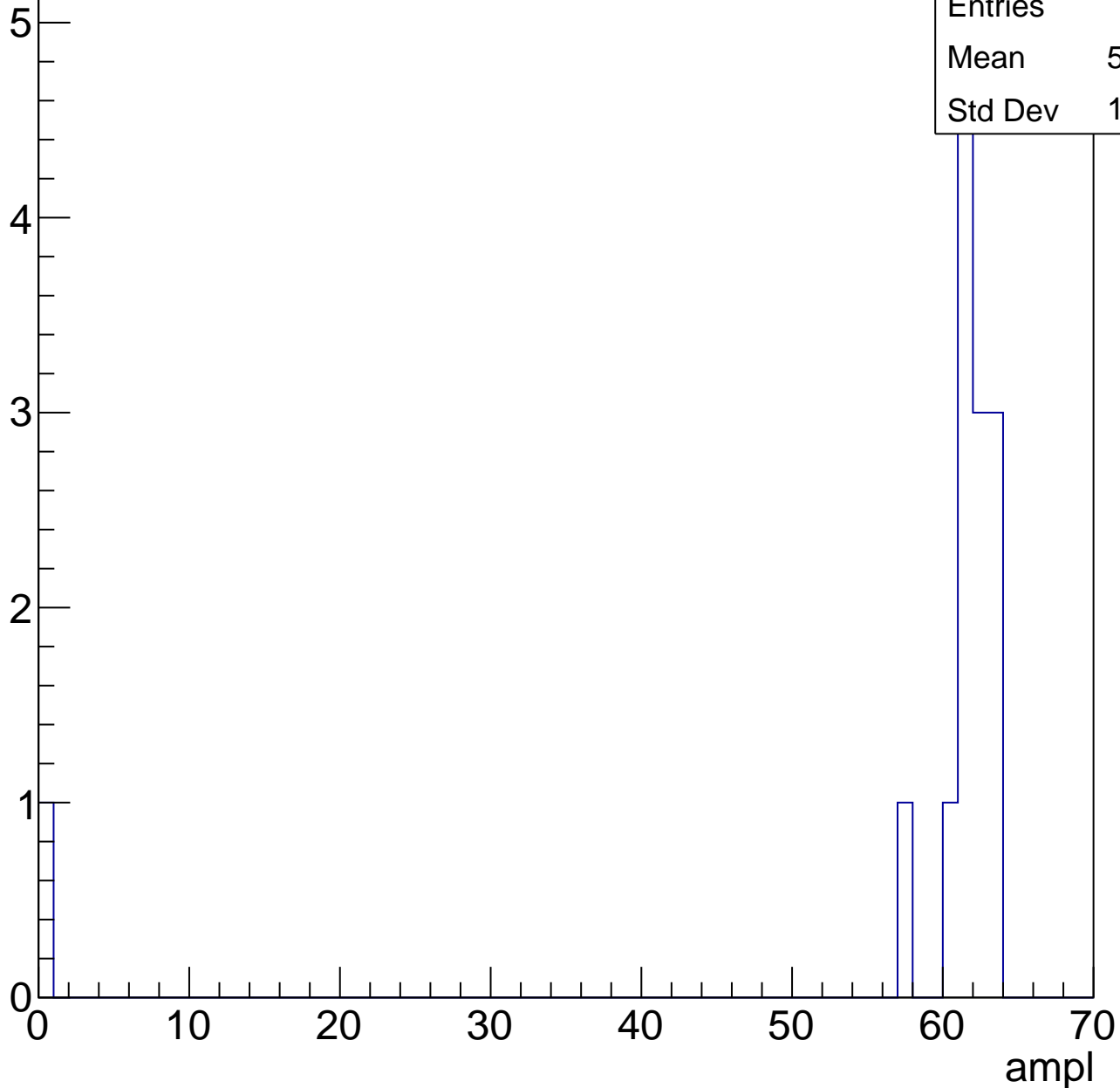


# B1L003S, U18-ch53, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	14
Mean	56.93
Std Dev	15.86





# B1L003S, U18-ch53, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U18-ch54, adc0

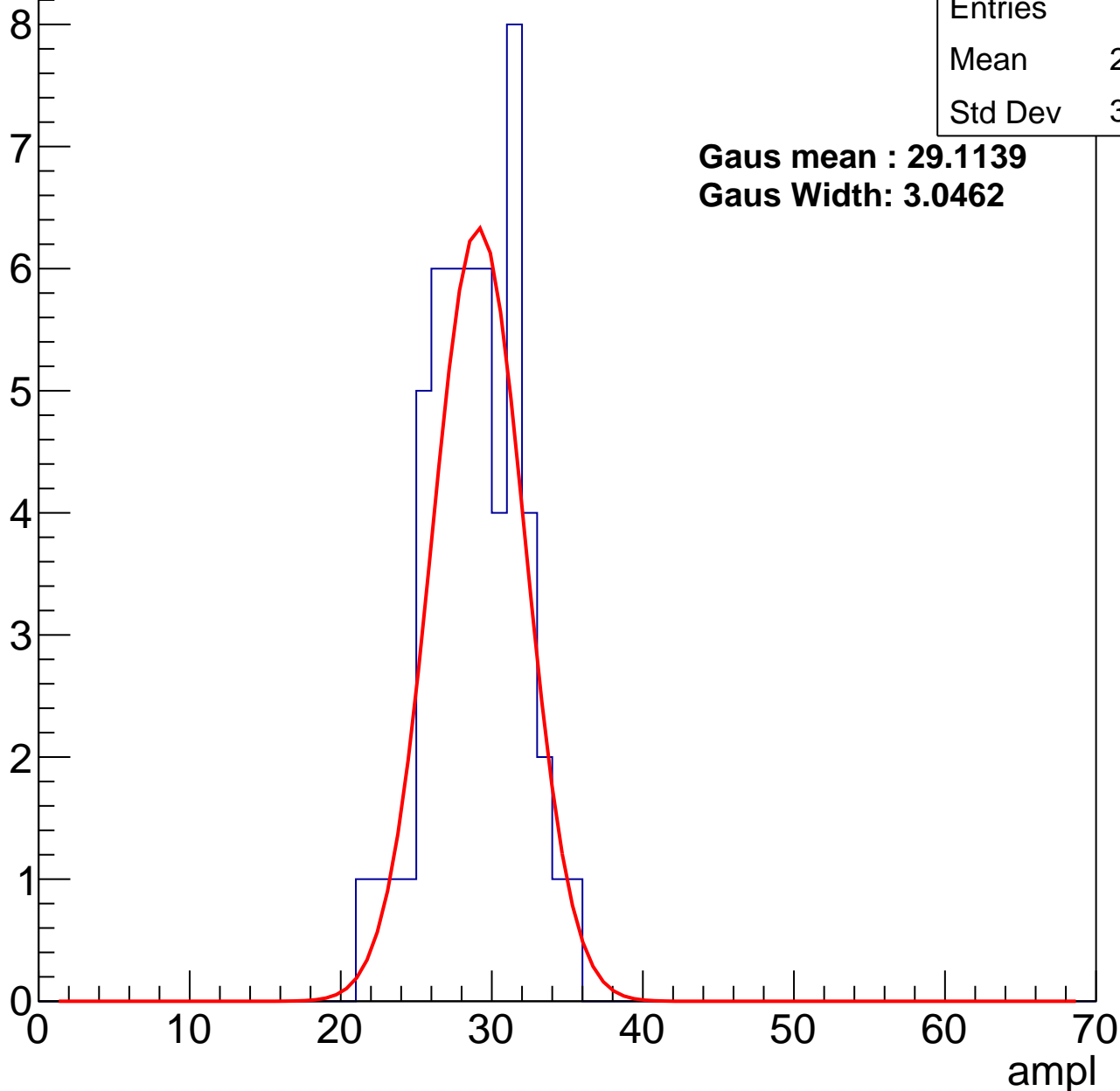
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	53
Mean	28.42
Std Dev	3.025

**Gaus mean : 29.1139**

**Gaus Width: 3.0462**



# B1L003S, U18-ch54, adc1

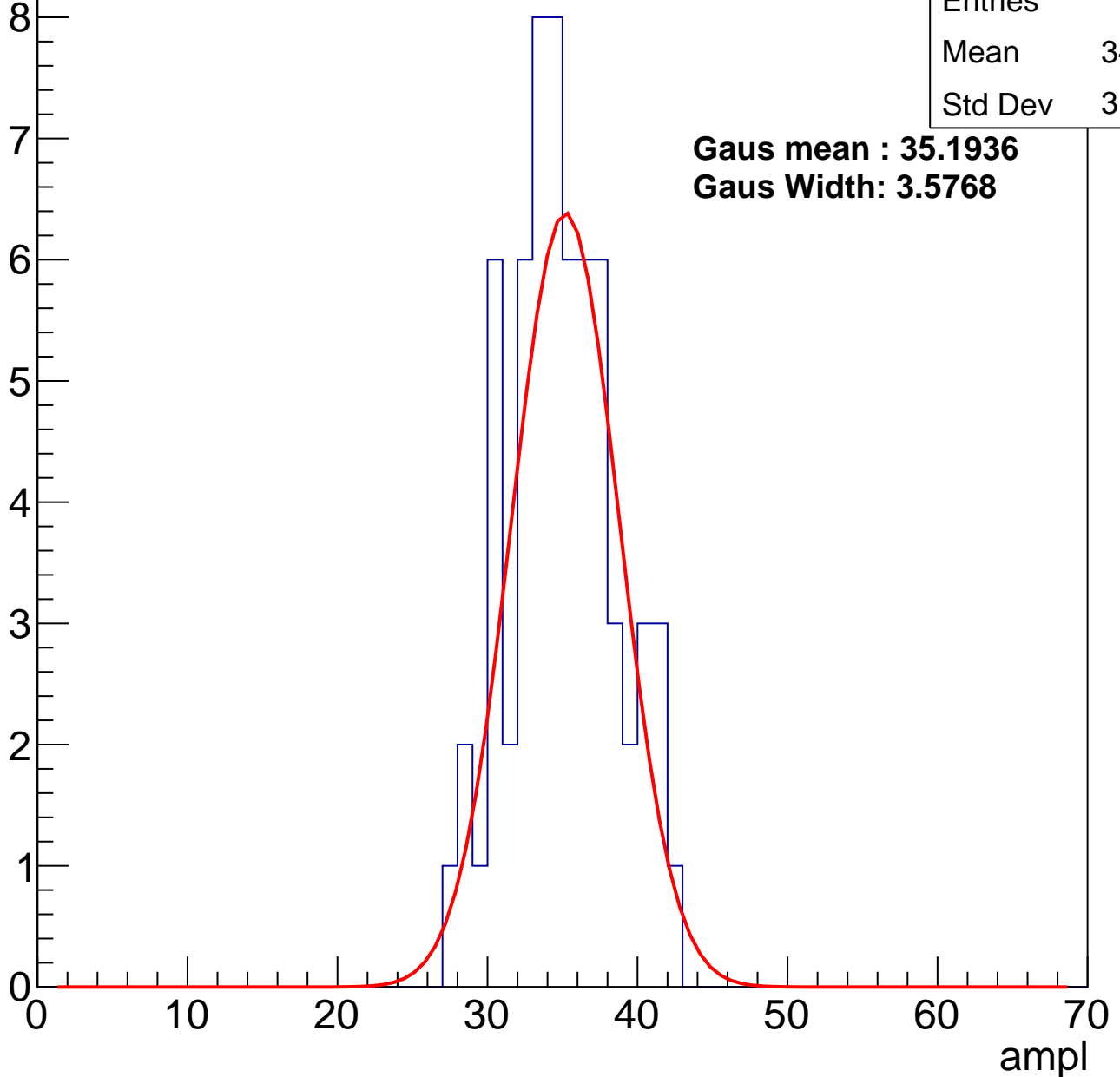
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	64
Mean	34.48
Std Dev	3.487

**Gaus mean : 35.1936**

**Gaus Width: 3.5768**



# B1L003S, U18-ch54, adc2

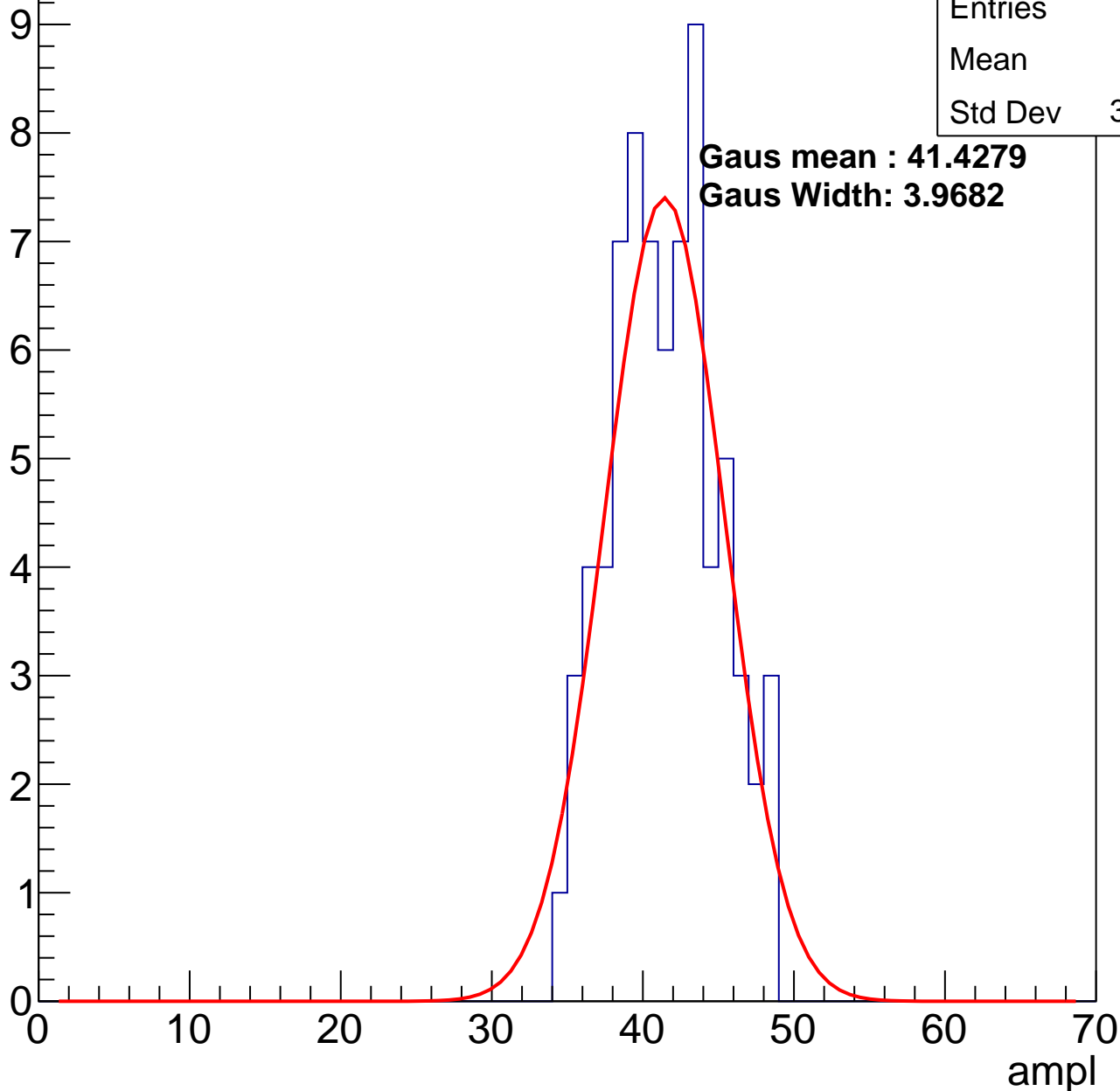
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	73
Mean	41
Std Dev	3.464

**Gaus mean : 41.4279**

**Gaus Width: 3.9682**

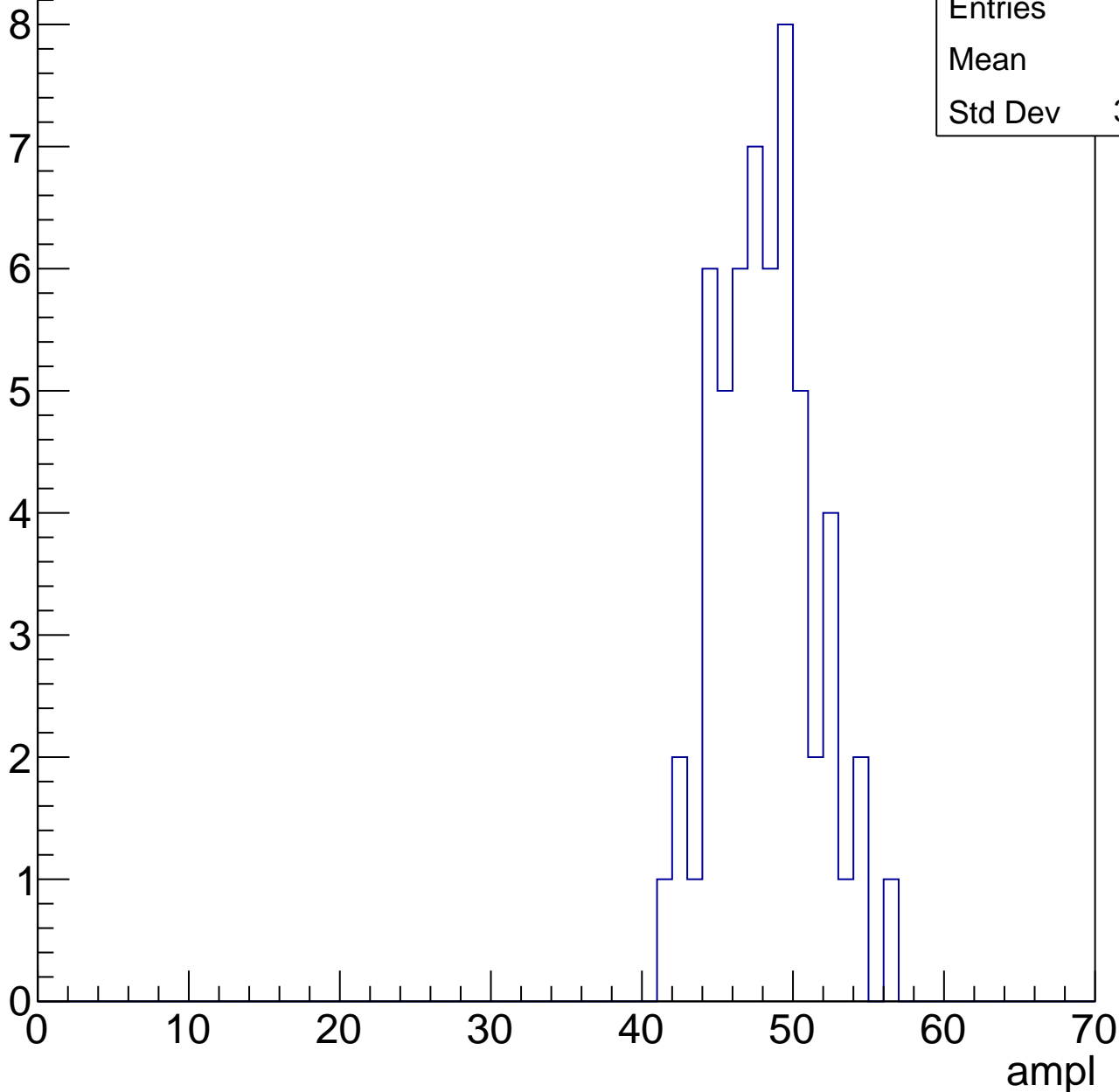


# B1L003S, U18-ch54, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	57
Mean	47.7
Std Dev	3.201

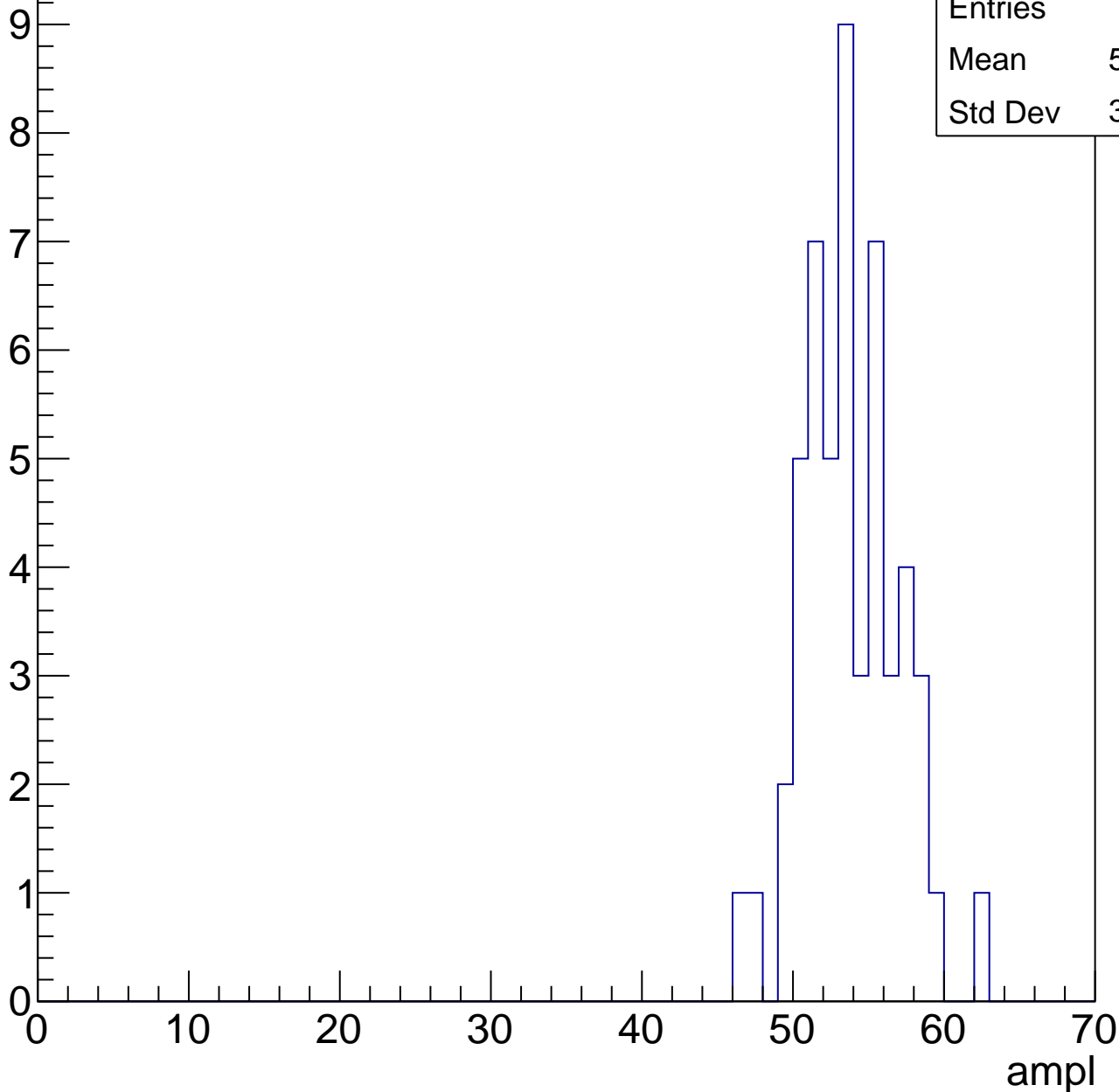


# B1L003S, U18-ch54, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	52
Mean	53.33
Std Dev	3.112

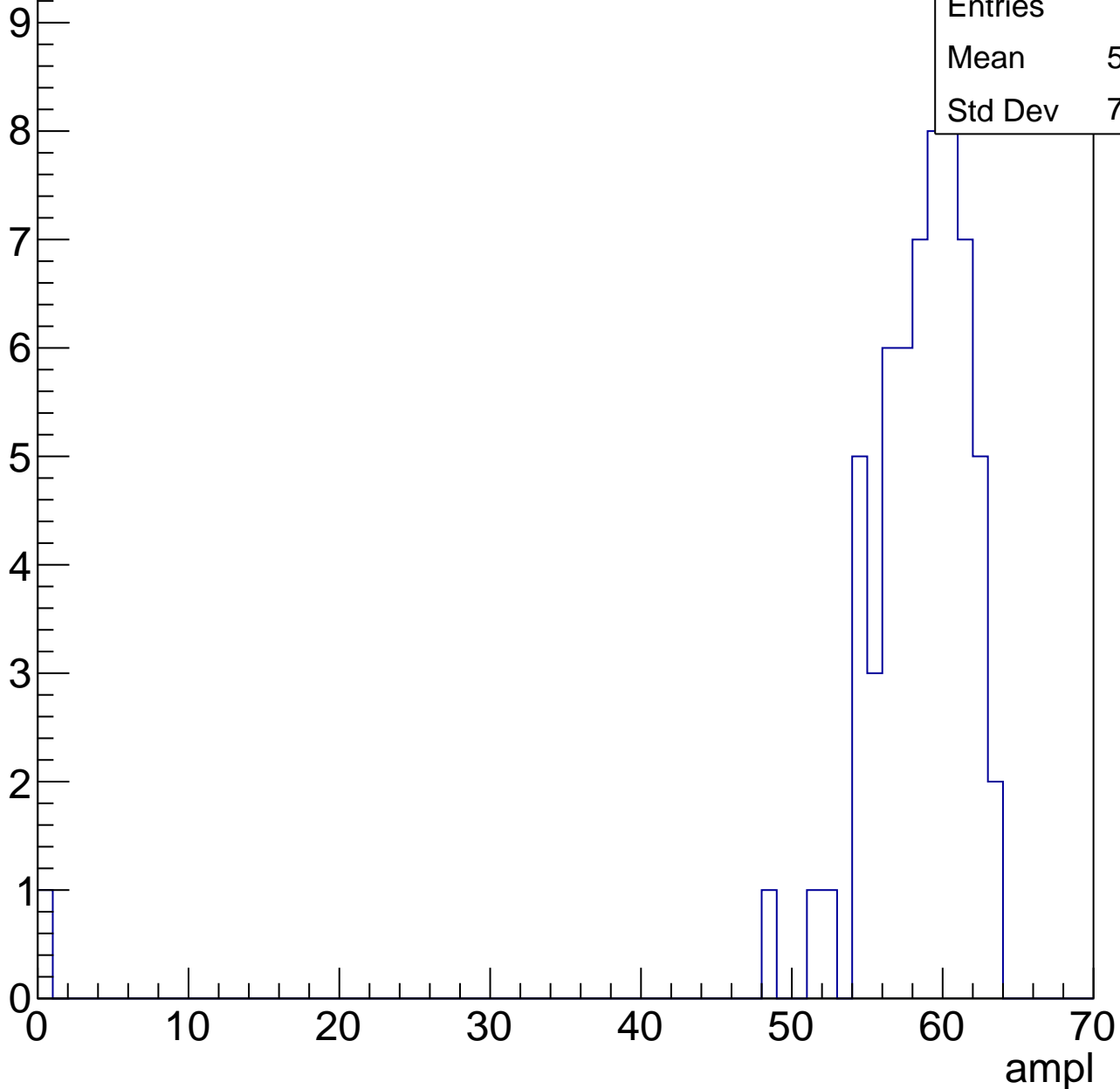


# B1L003S, U18-ch54, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	62
Mean	57.18
Std Dev	7.912

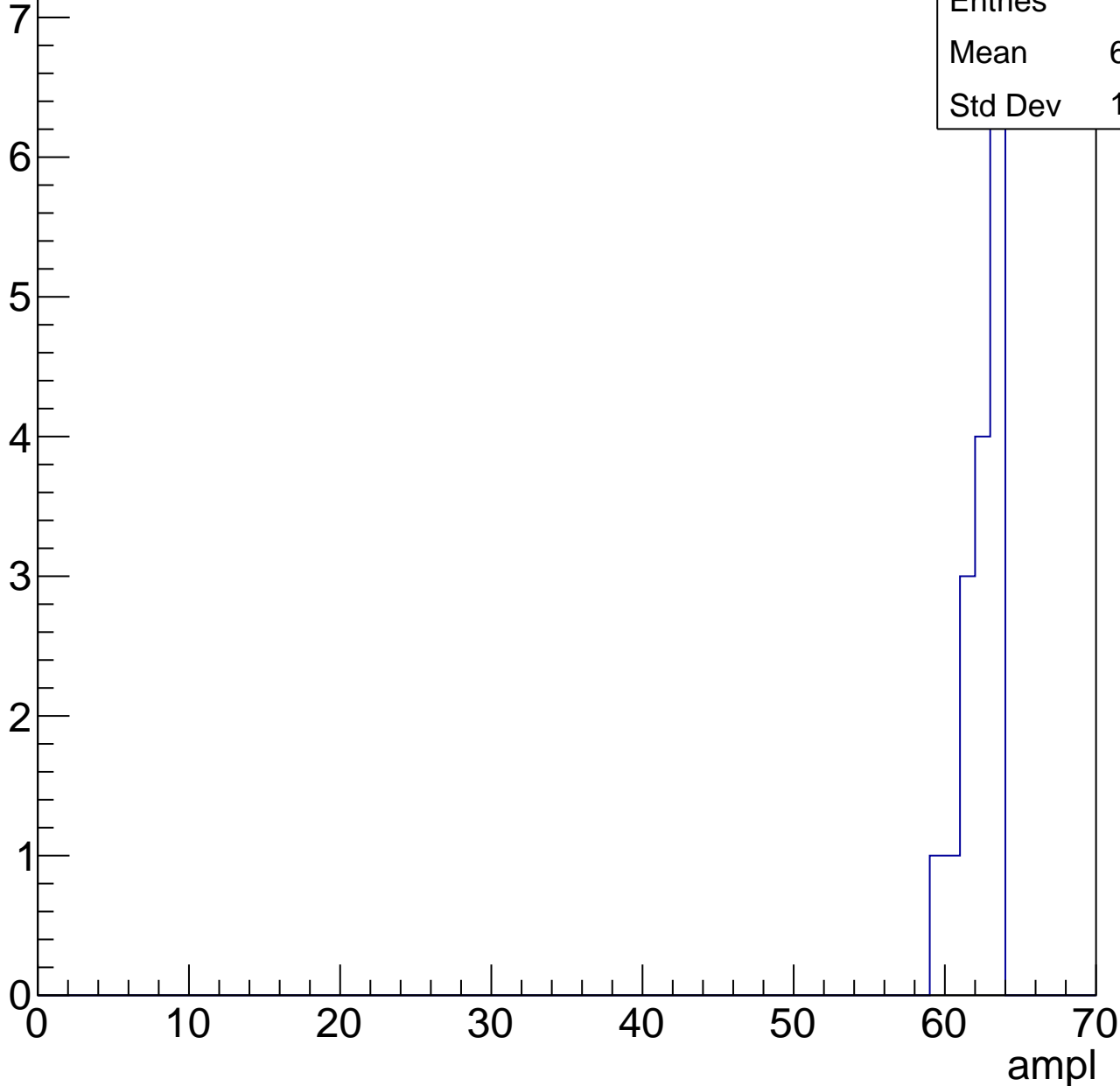


# B1L003S, U18-ch54, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	16
Mean	61.94
Std Dev	1.197

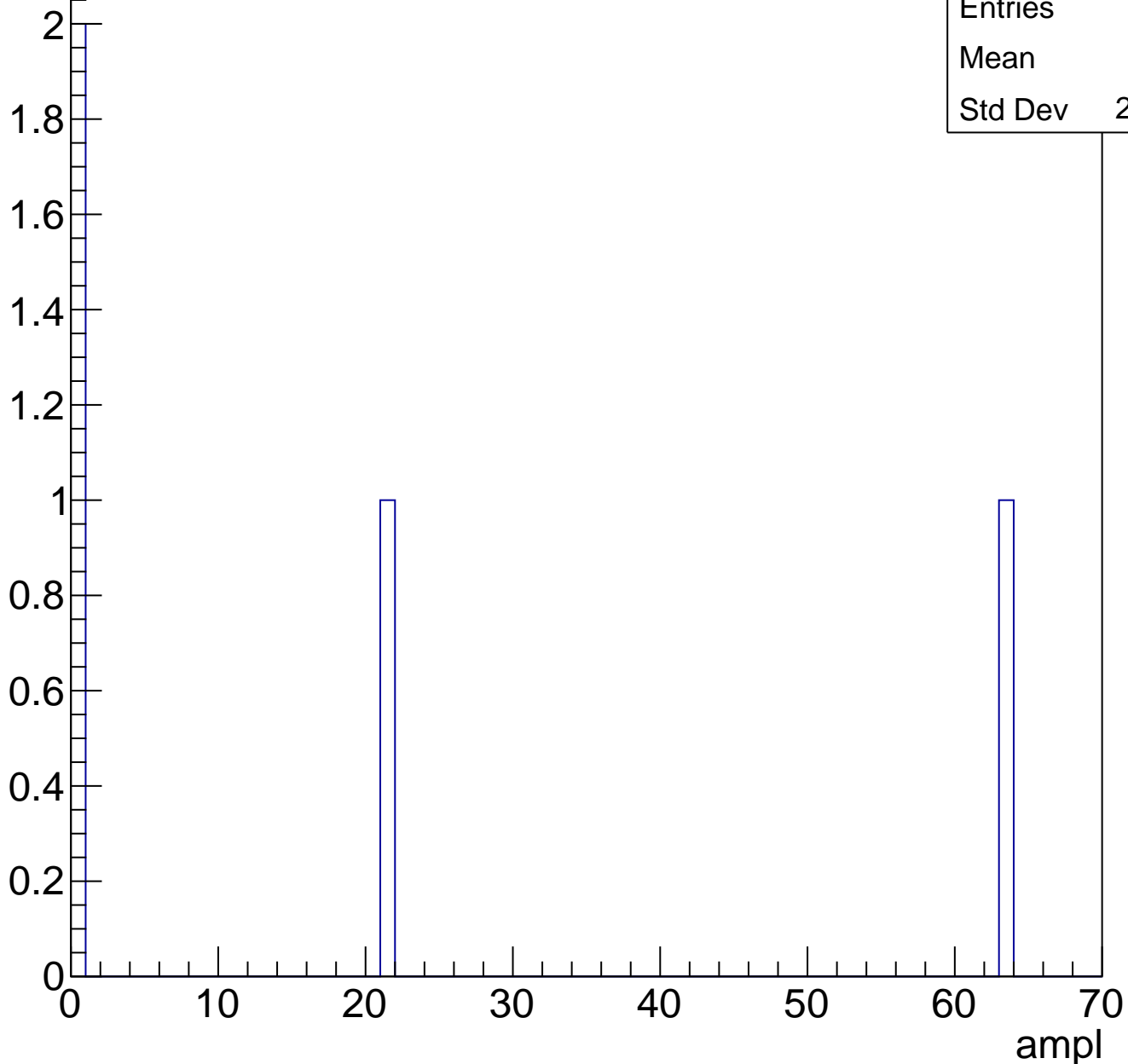




# B1L003S, U18-ch54, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	4
Mean	21
Std Dev	25.72

# B1L003S, U18-ch55, adc0

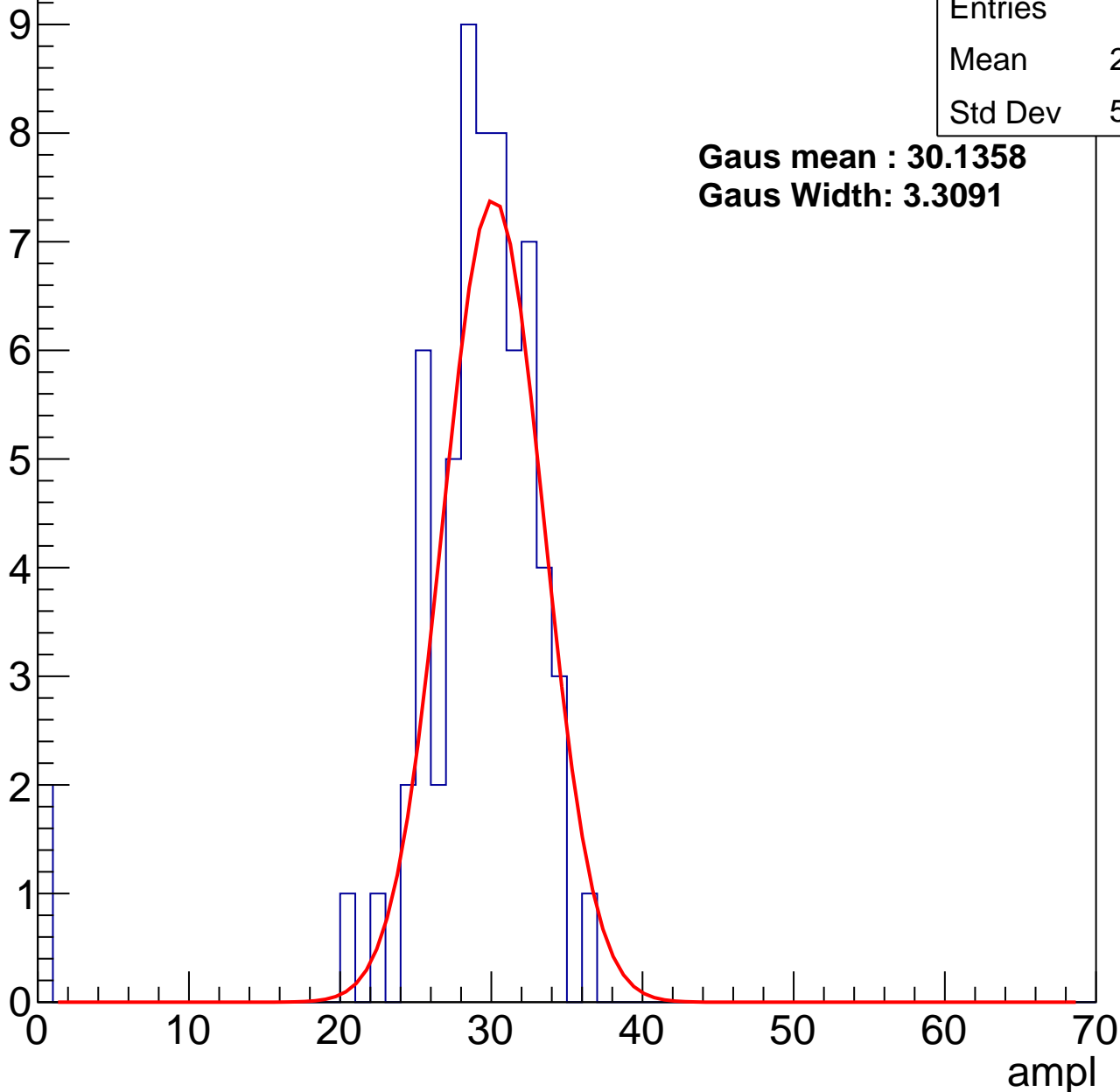
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	65
Mean	28.17
Std Dev	5.875

**Gaus mean : 30.1358**

**Gaus Width: 3.3091**



# B1L003S, U18-ch55, adc1

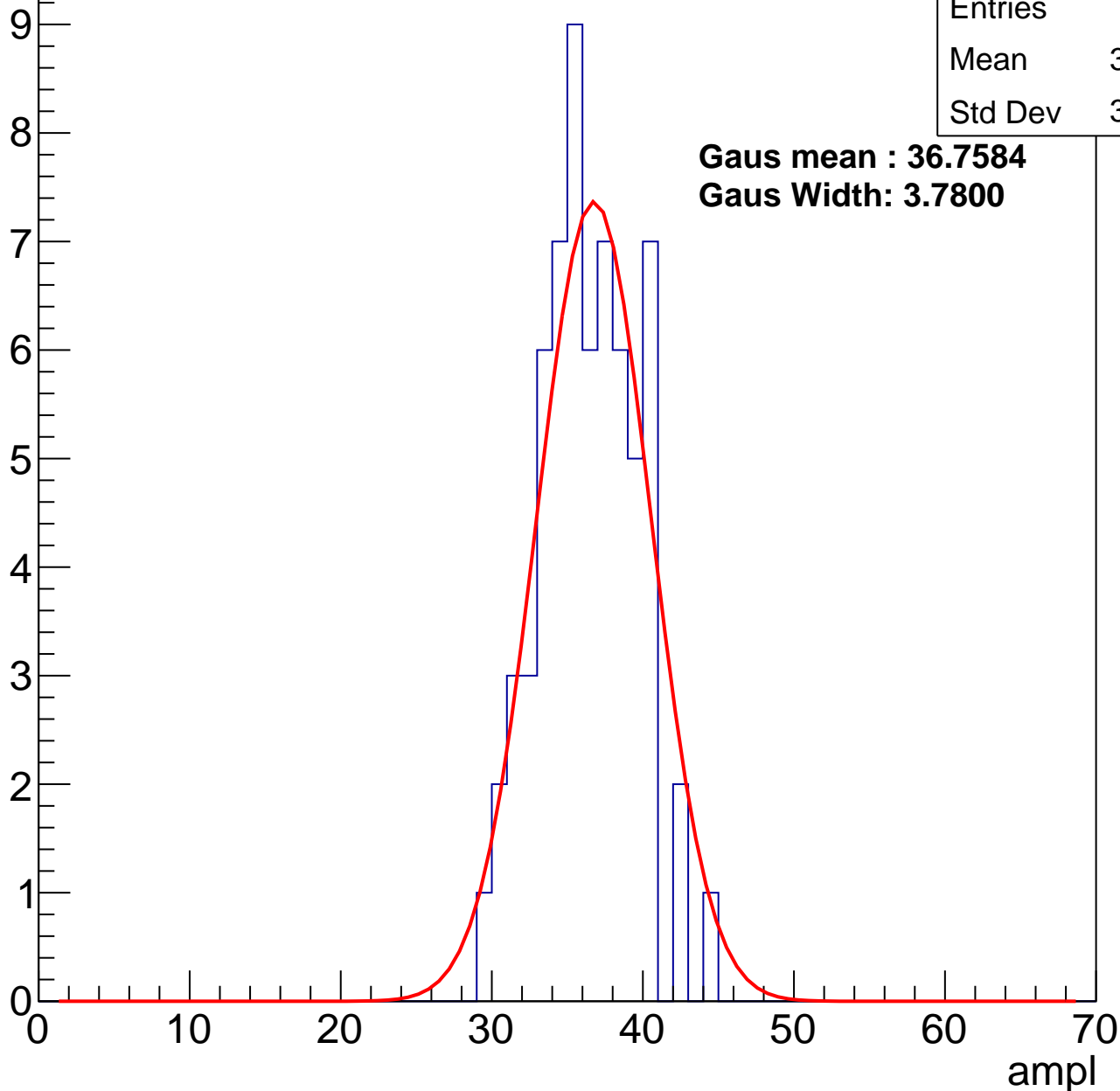
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	65
Mean	35.92
Std Dev	3.183

**Gaus mean : 36.7584**

**Gaus Width: 3.7800**



# B1L003S, U18-ch55, adc2

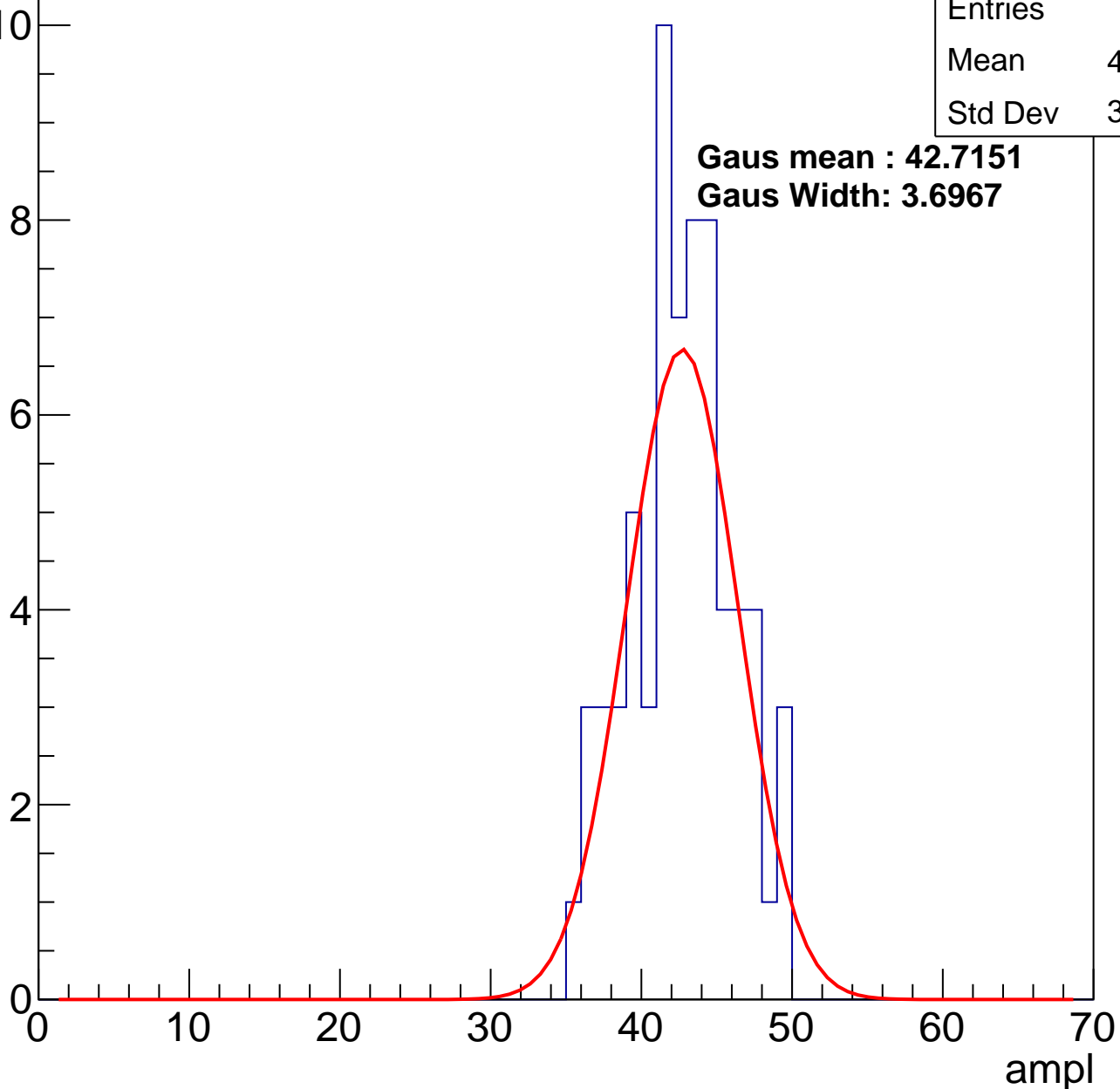
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	67
Mean	42.24
Std Dev	3.382

**Gaus mean : 42.7151**

**Gaus Width: 3.6967**

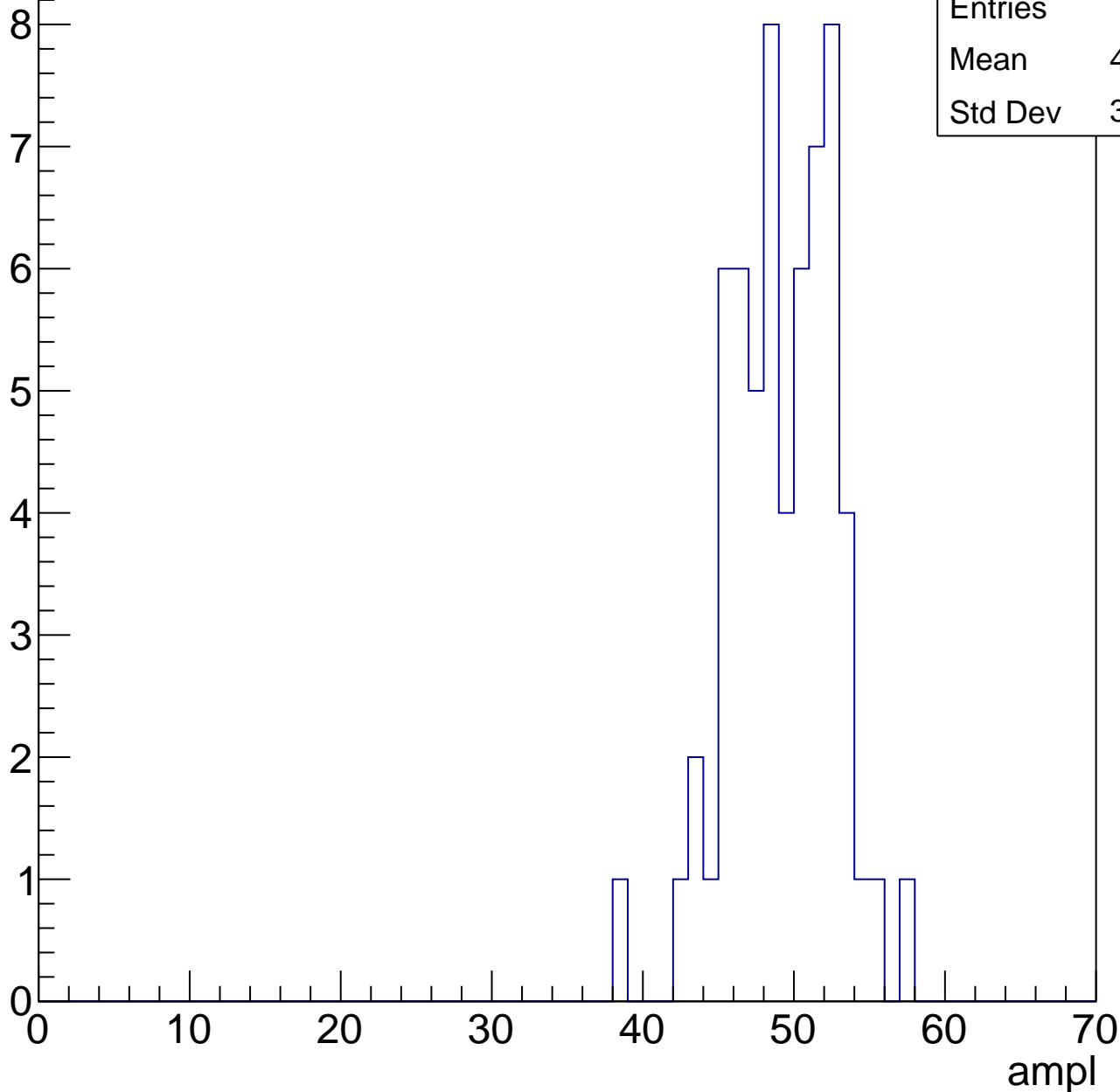


# B1L003S, U18-ch55, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

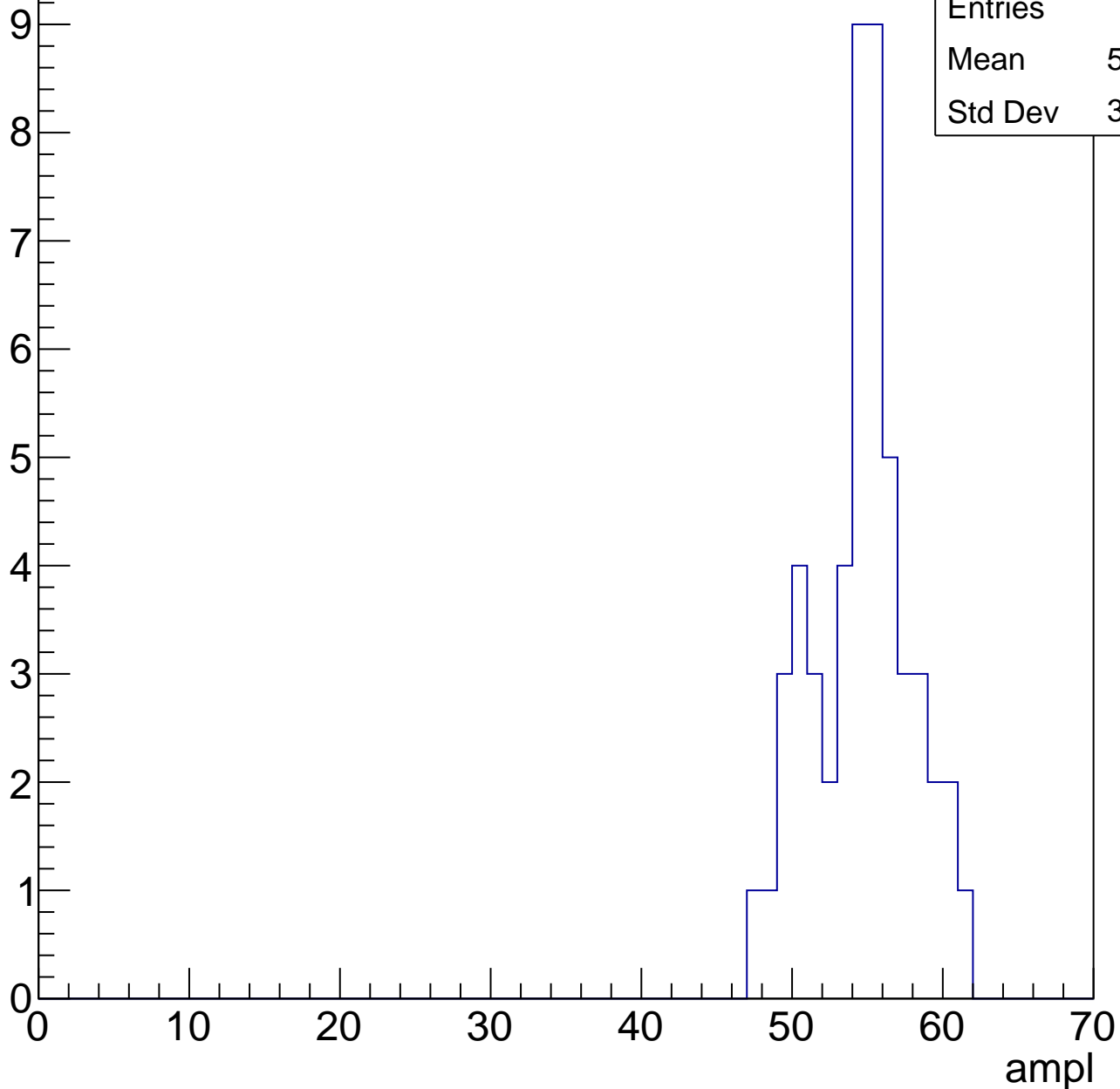
Entries	62
Mean	48.74
Std Dev	3.445



# B1L003S, U18-ch55, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



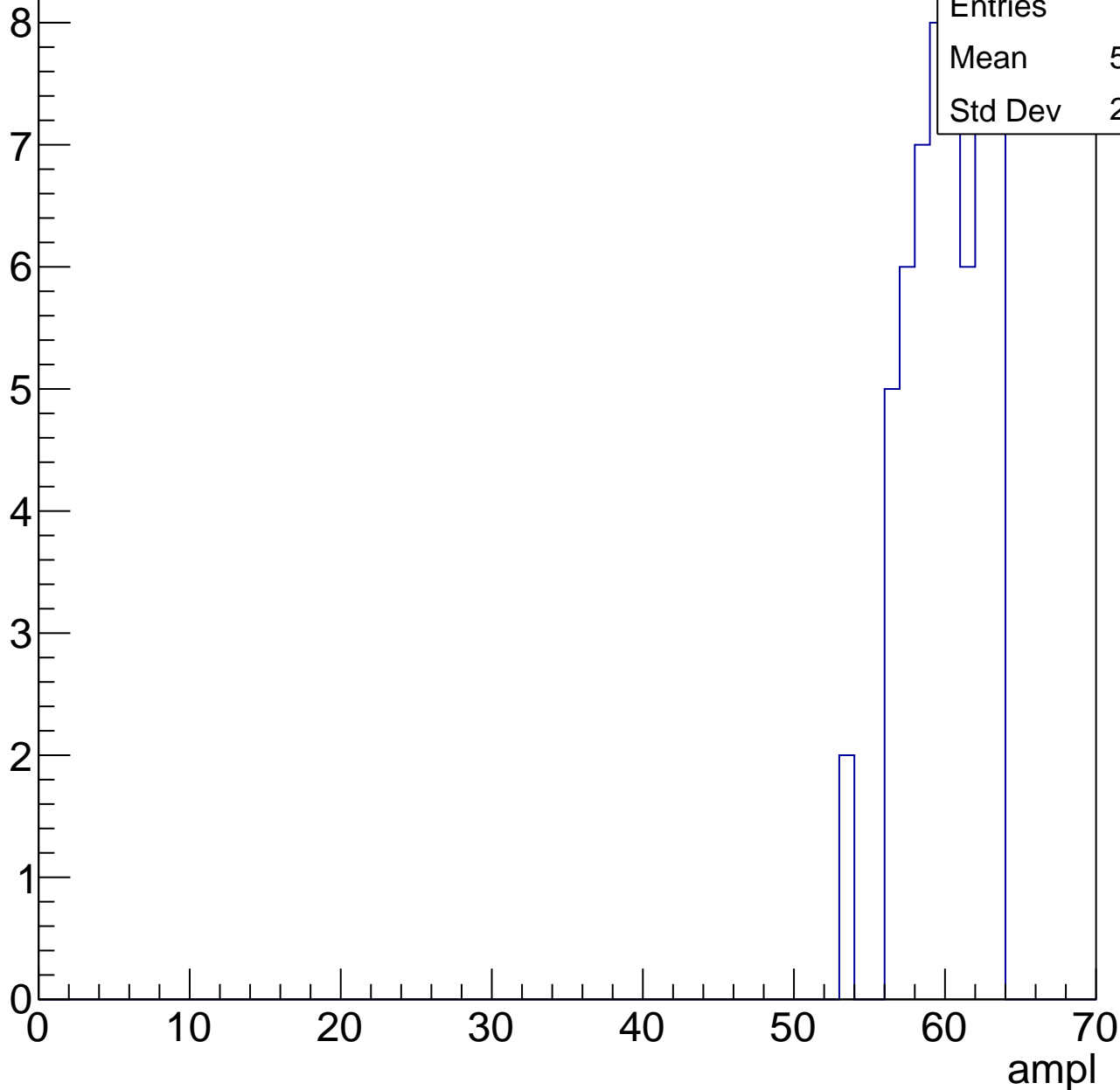
Entries	52
Mean	54.15
Std Dev	3.213

# B1L003S, U18-ch55, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

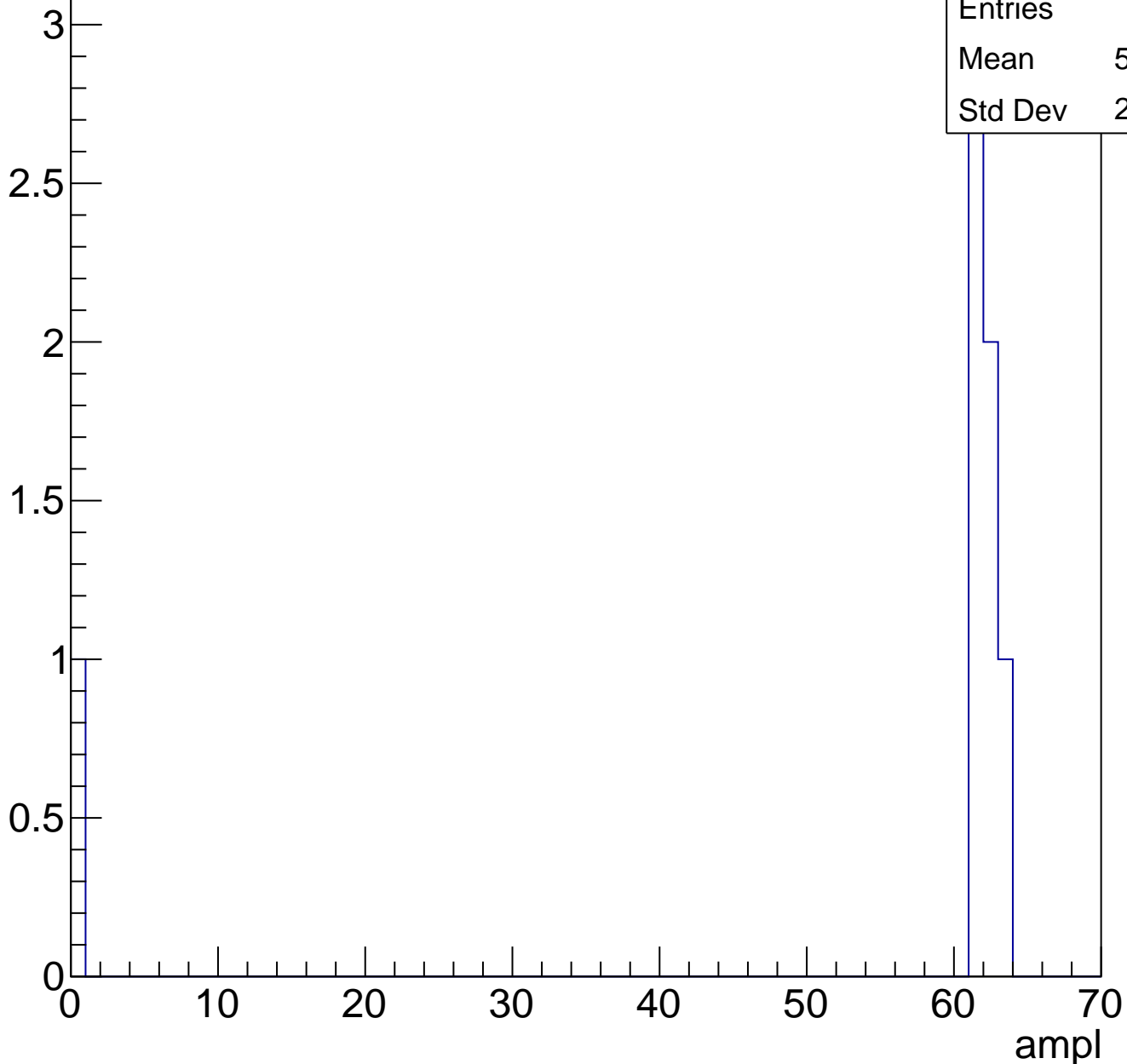
Entries	58
Mean	59.52
Std Dev	2.507



# B1L003S, U18-ch55, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	7
Mean	52.86
Std Dev	21.59



# B1L003S, U18-ch55, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U18-ch56, adc0

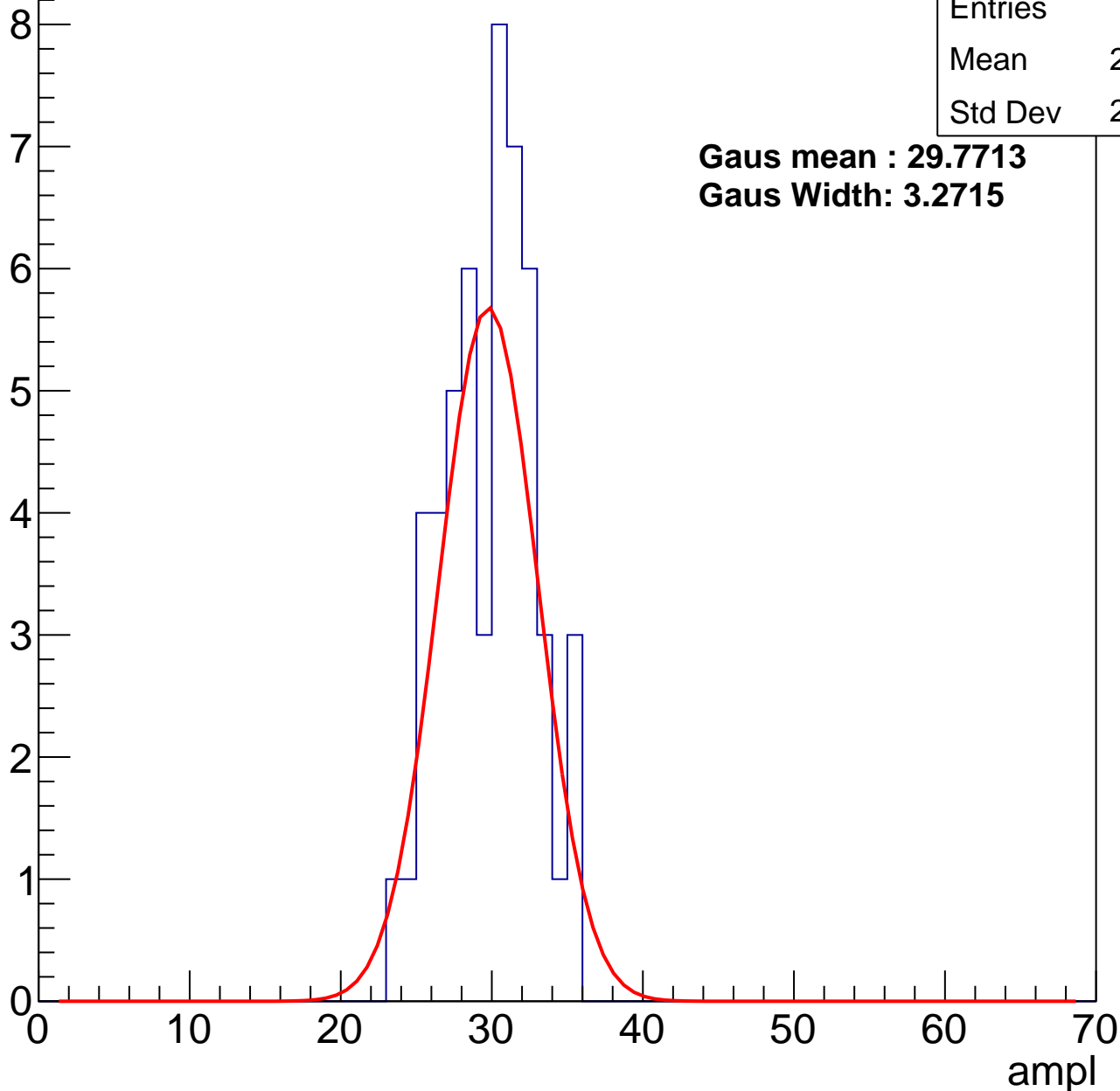
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	52
Mean	29.38
Std Dev	2.943

**Gaus mean : 29.7713**

**Gaus Width: 3.2715**



# B1L003S, U18-ch56, adc1

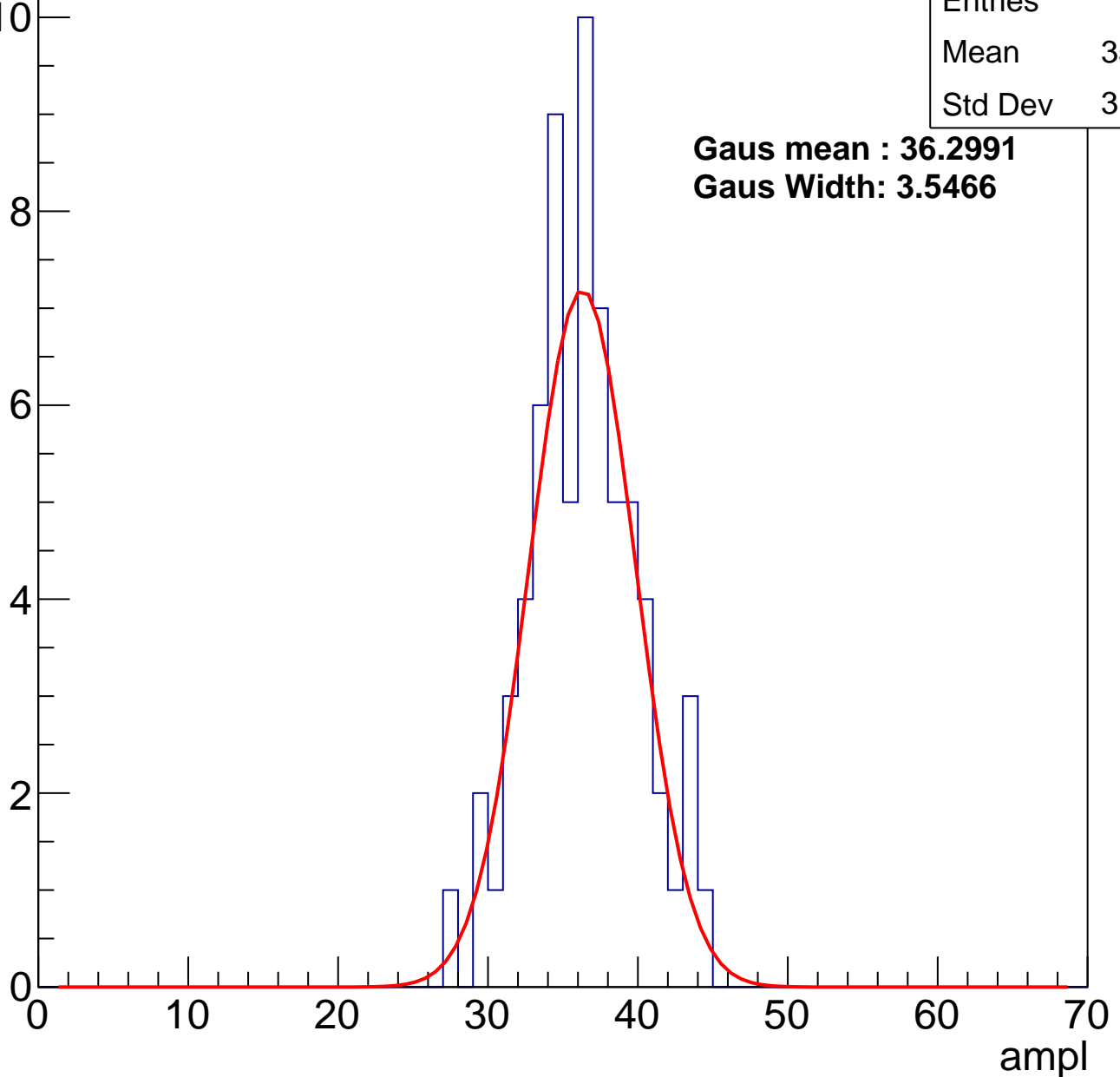
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	69
Mean	35.88
Std Dev	3.573

**Gaus mean : 36.2991**

**Gaus Width: 3.5466**



# B1L003S, U18-ch56, adc2

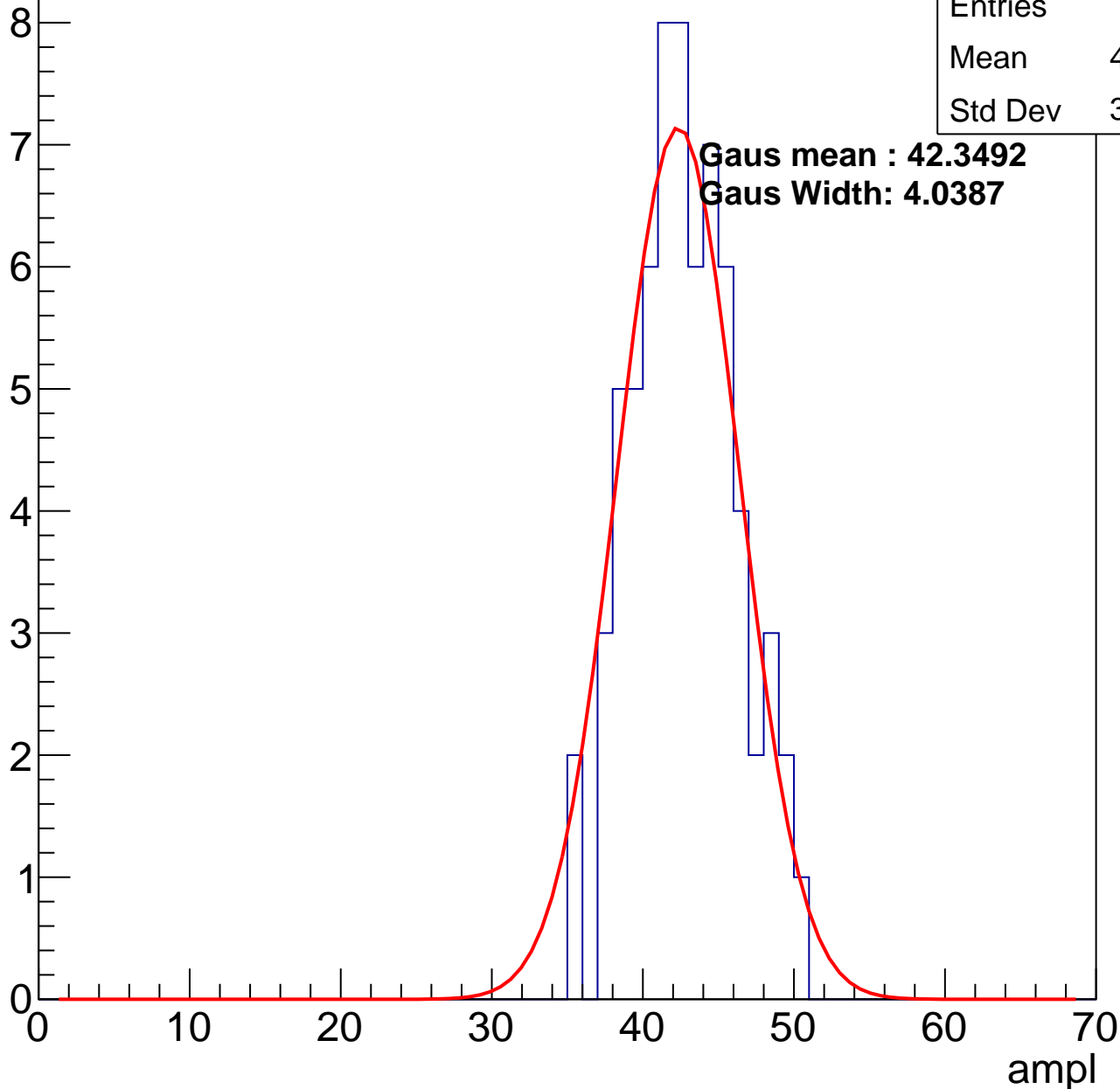
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	68
Mean	42.29
Std Dev	3.422

**Gaus mean : 42.3492**

**Gaus Width: 4.0387**

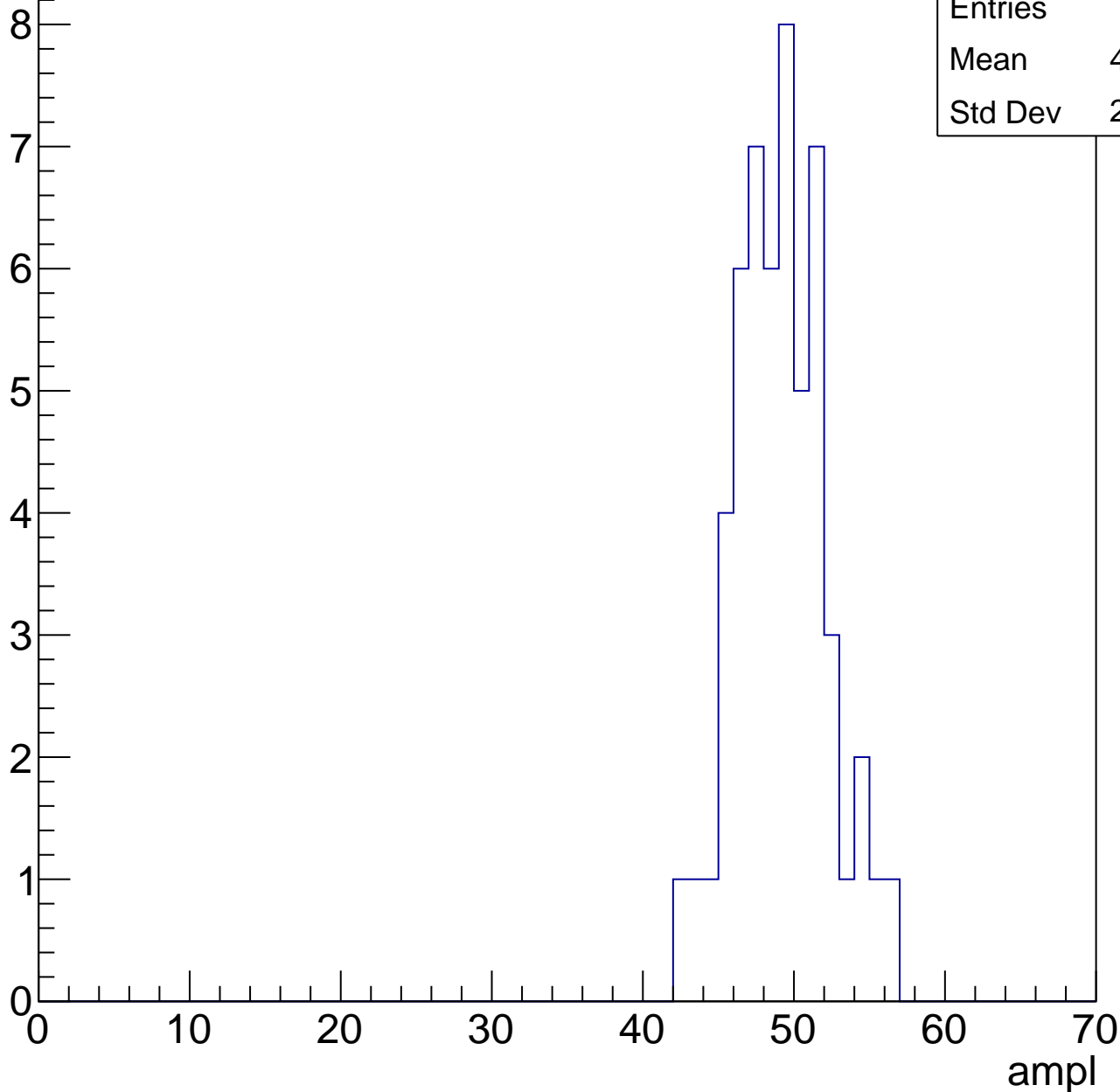


# B1L003S, U18-ch56, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

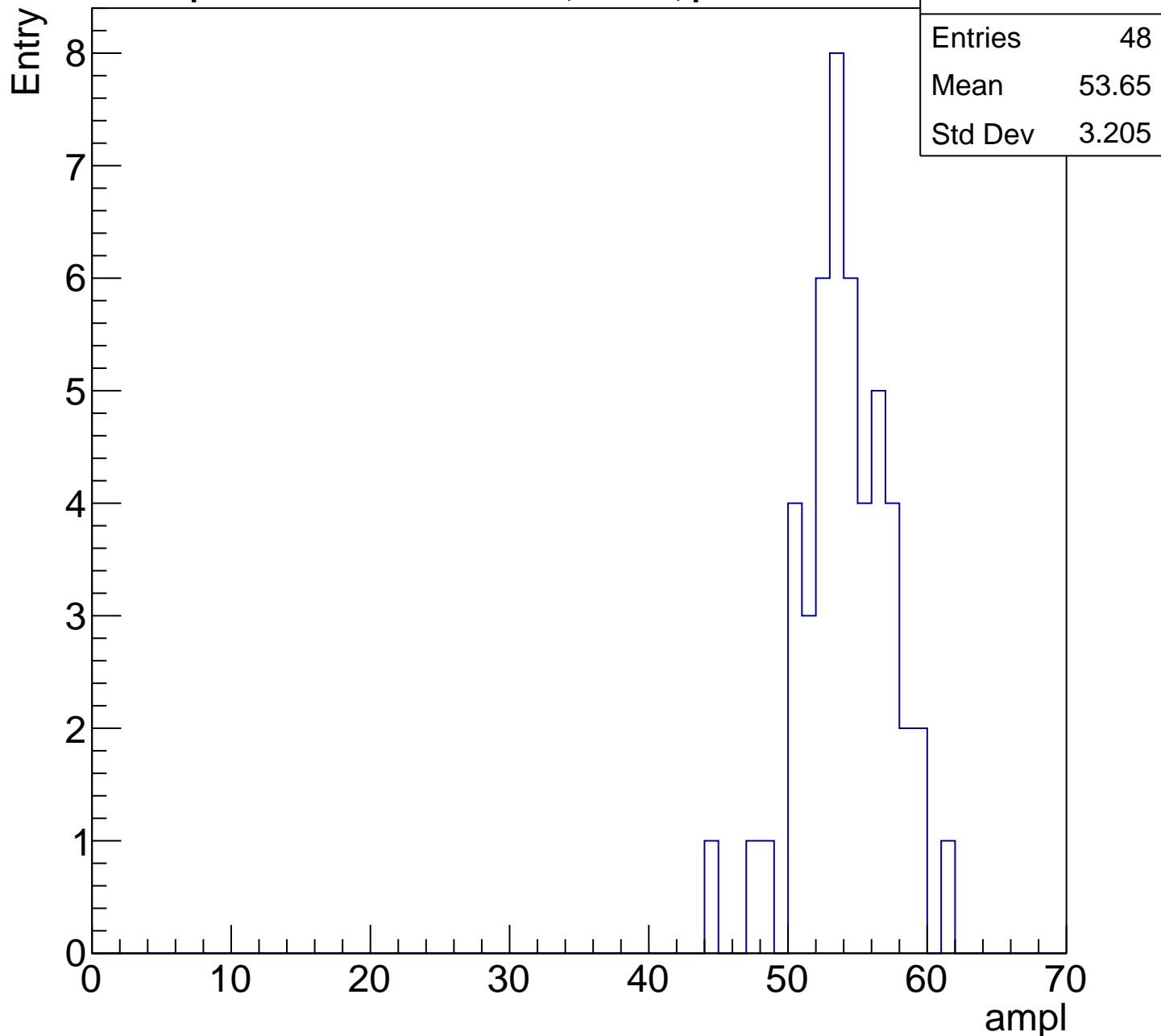
Entry

Entries	54
Mean	48.69
Std Dev	2.943



# B1L003S, U18-ch56, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2



# B1L003S, U18-ch56, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	68
Mean	58.1
Std Dev	7.585

Entry

10

8

6

4

2

0

0

10

20

30

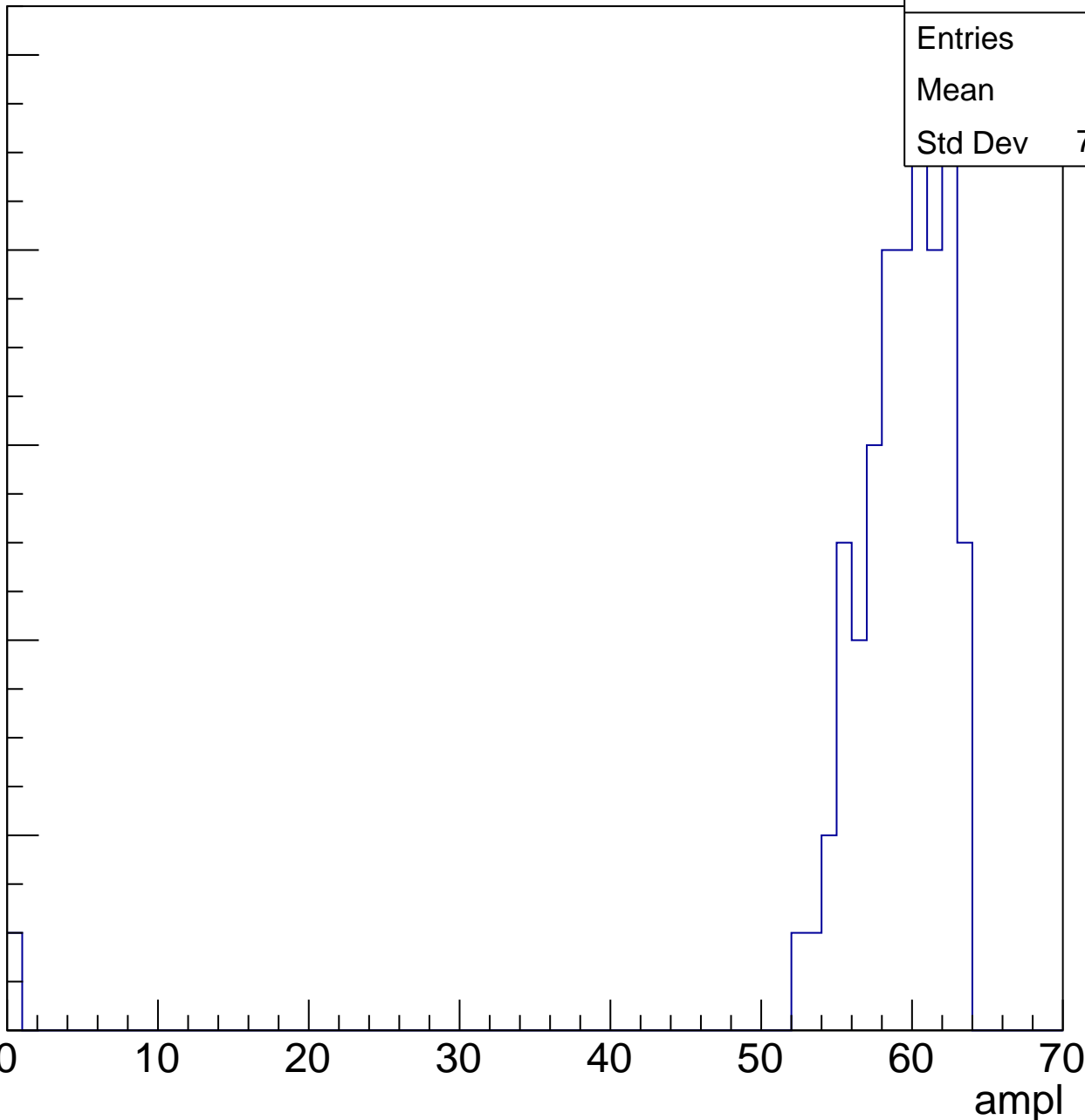
40

50

60

70

ampl

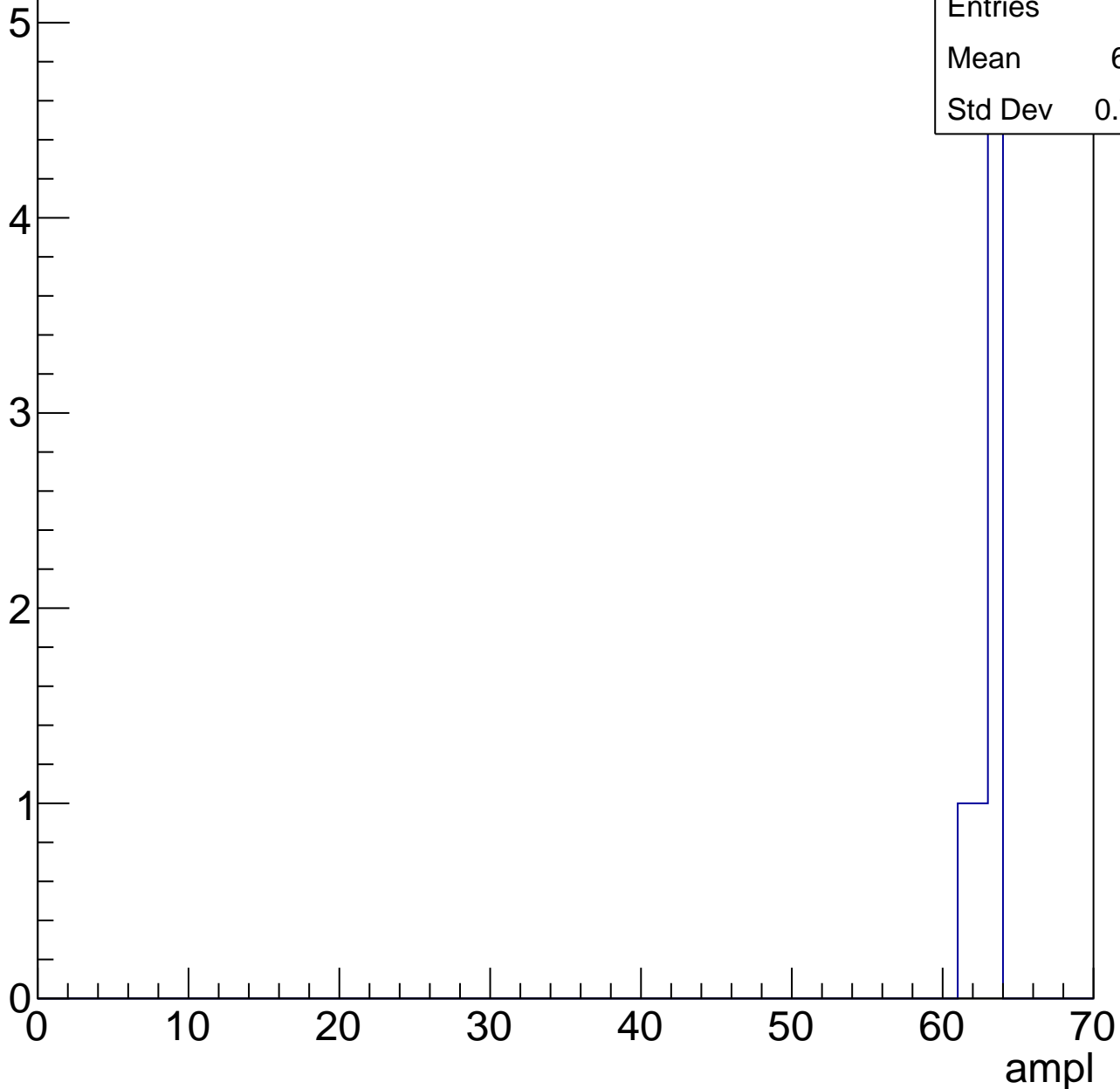


# B1L003S, U18-ch56, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	7
Mean	62.57
Std Dev	0.7284





# B1L003S, U18-ch56, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U18-ch57, adc0

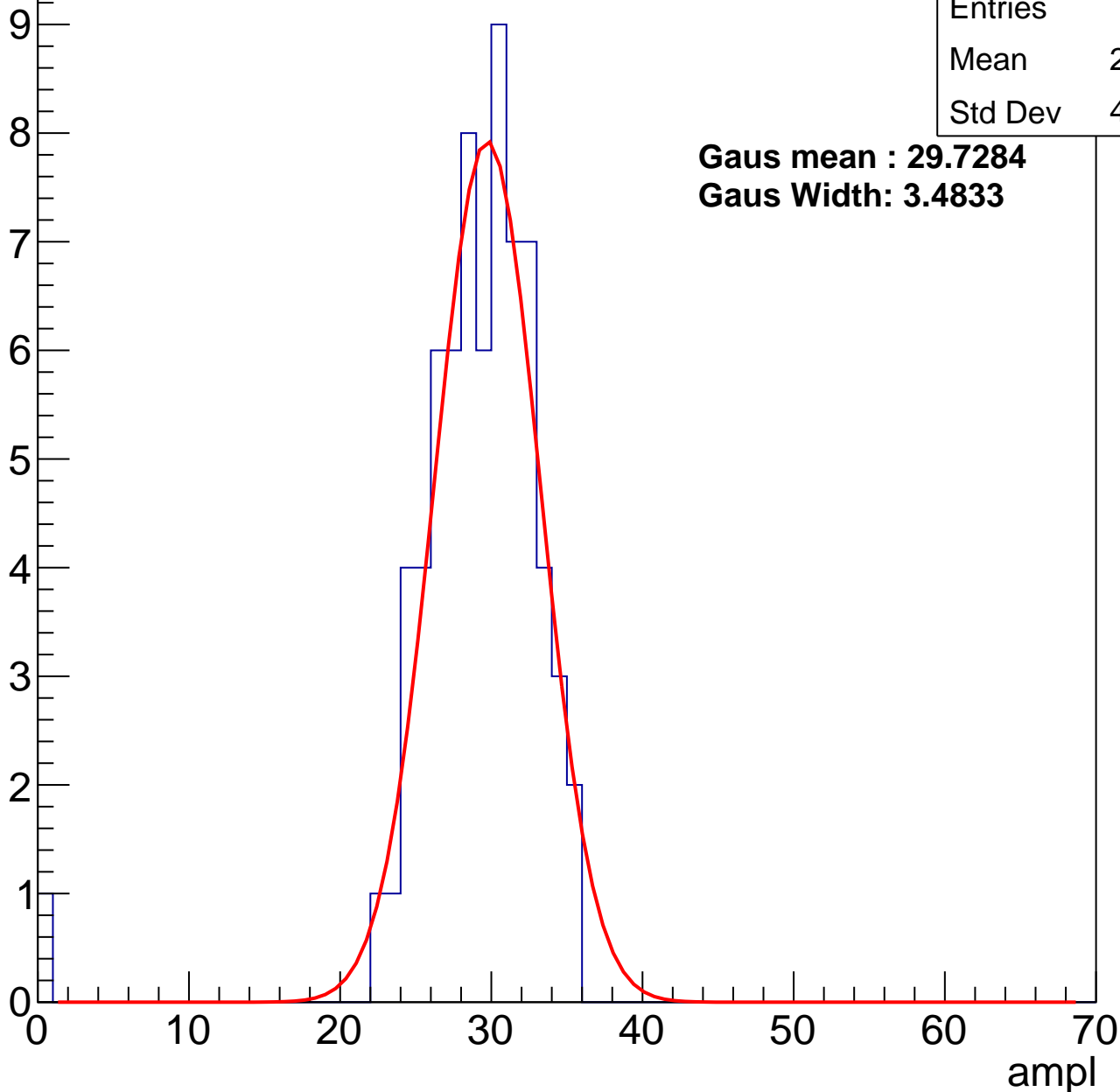
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	69
Mean	28.58
Std Dev	4.623

**Gaus mean : 29.7284**

**Gaus Width: 3.4833**



# B1L003S, U18-ch57, adc1

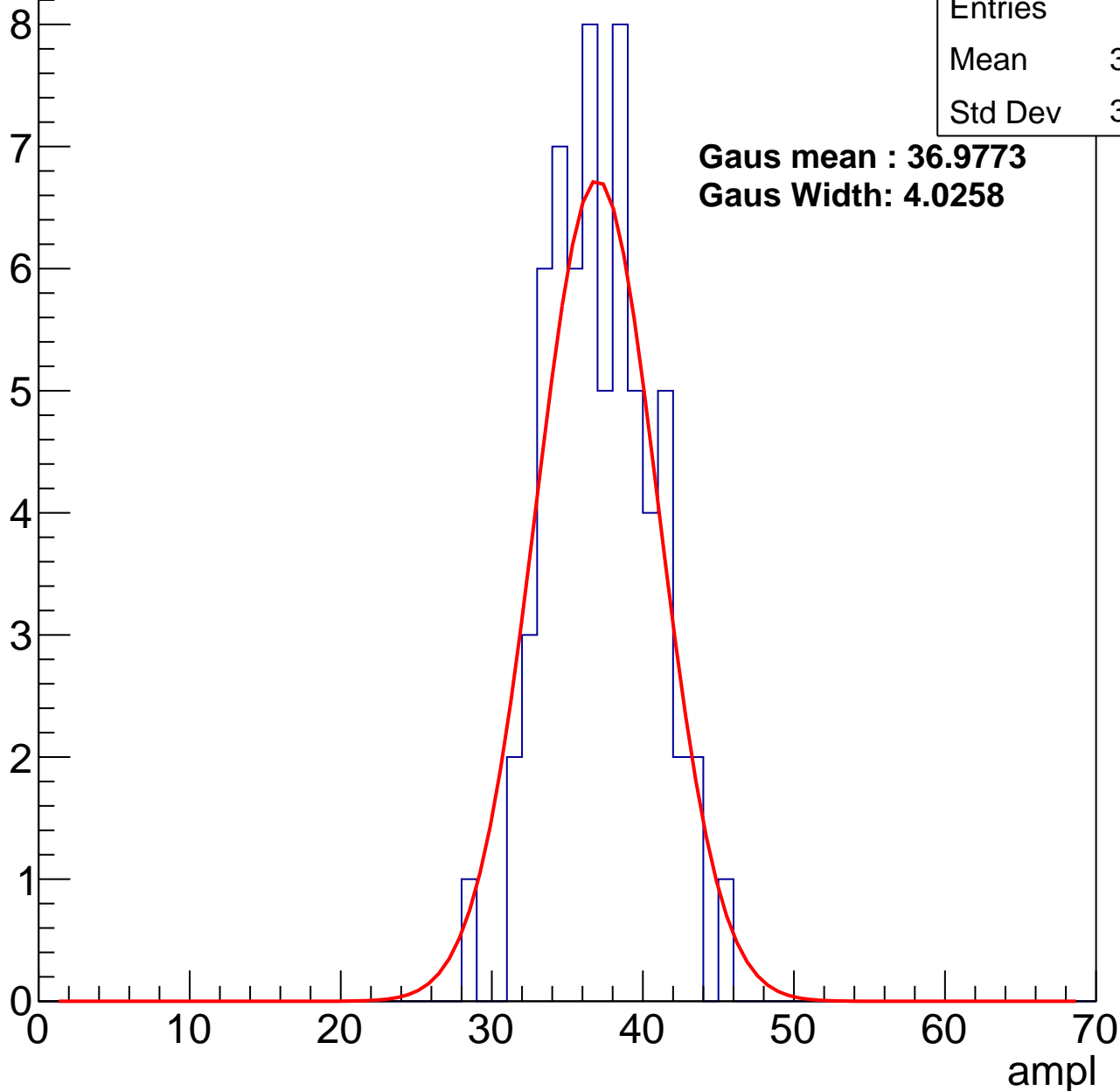
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	65
Mean	36.68
Std Dev	3.379

**Gaus mean : 36.9773**

**Gaus Width: 4.0258**

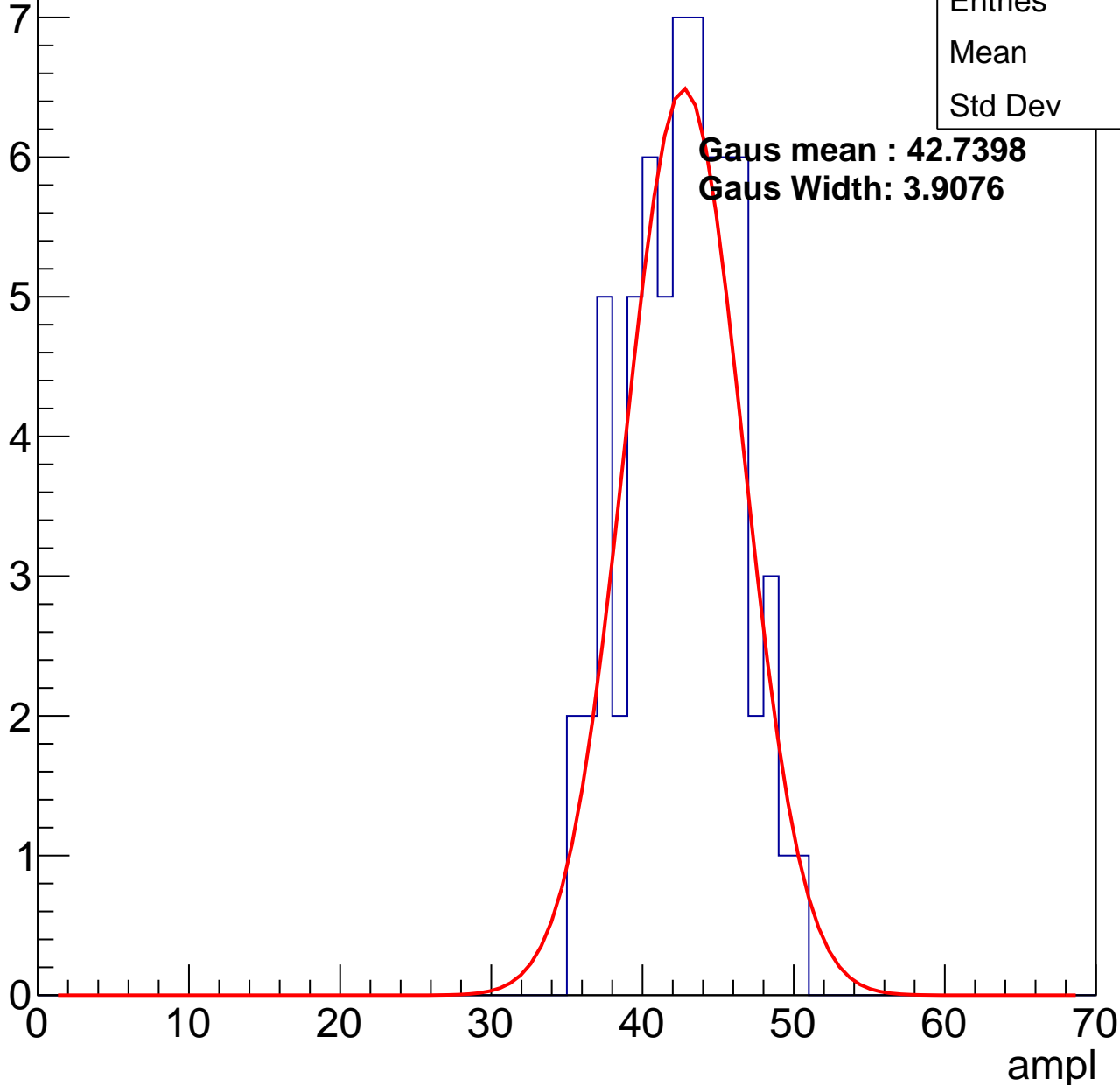


# B1L003S, U18-ch57, adc2

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

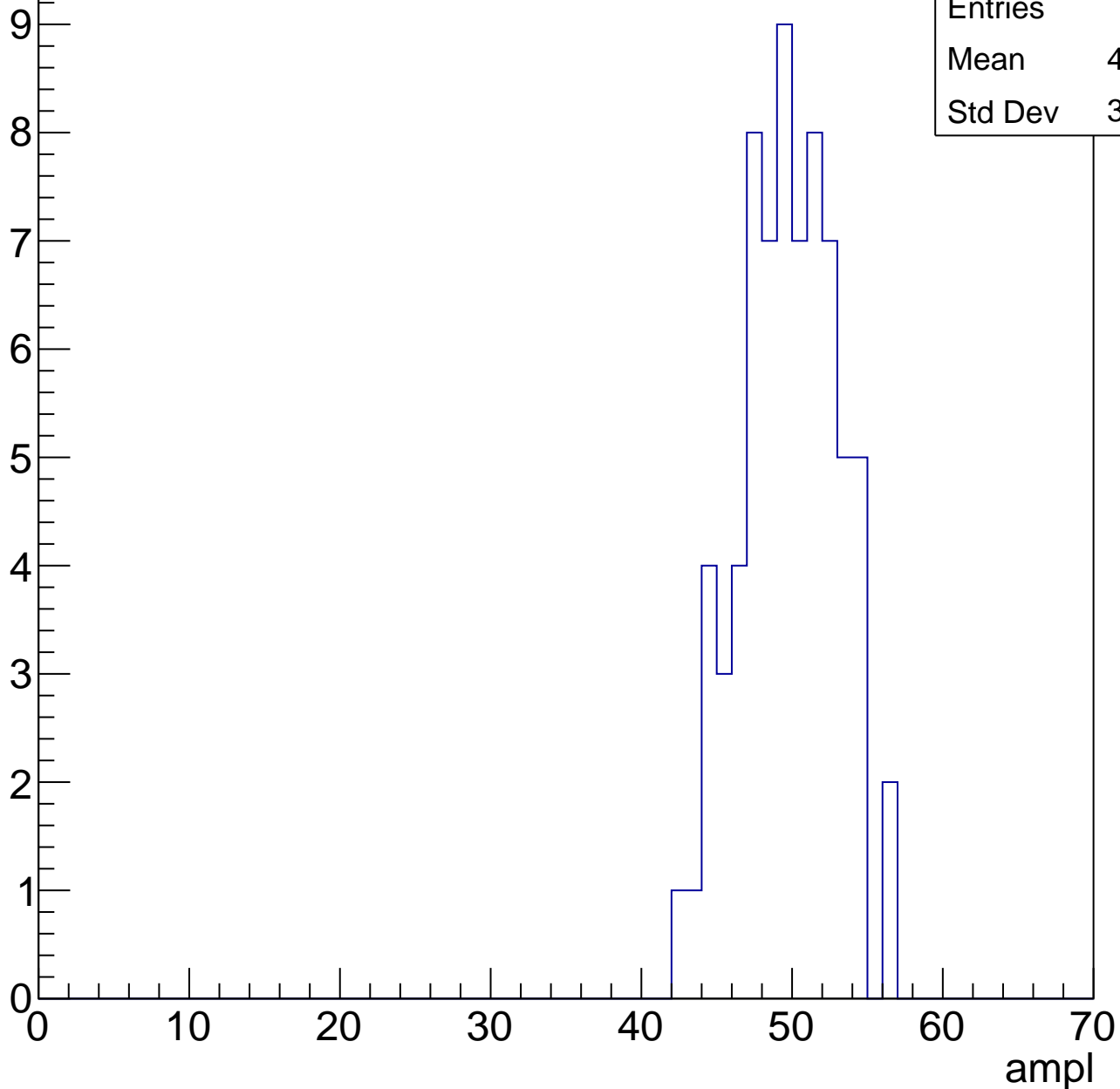
Entries	66
Mean	42.2
Std Dev	3.59



# B1L003S, U18-ch57, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

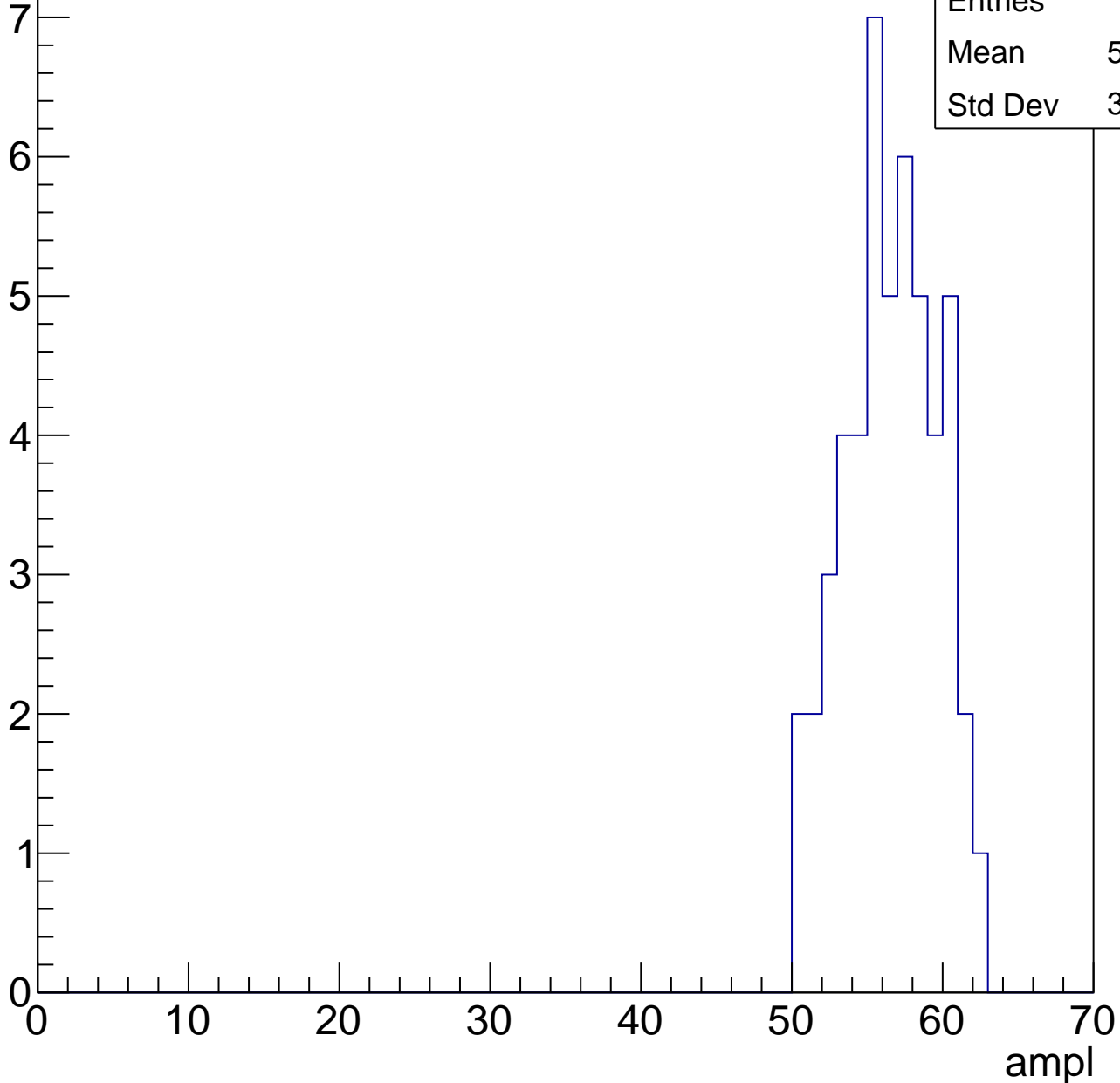


# B1L003S, U18-ch57, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	50
Mean	56.06
Std Dev	3.023

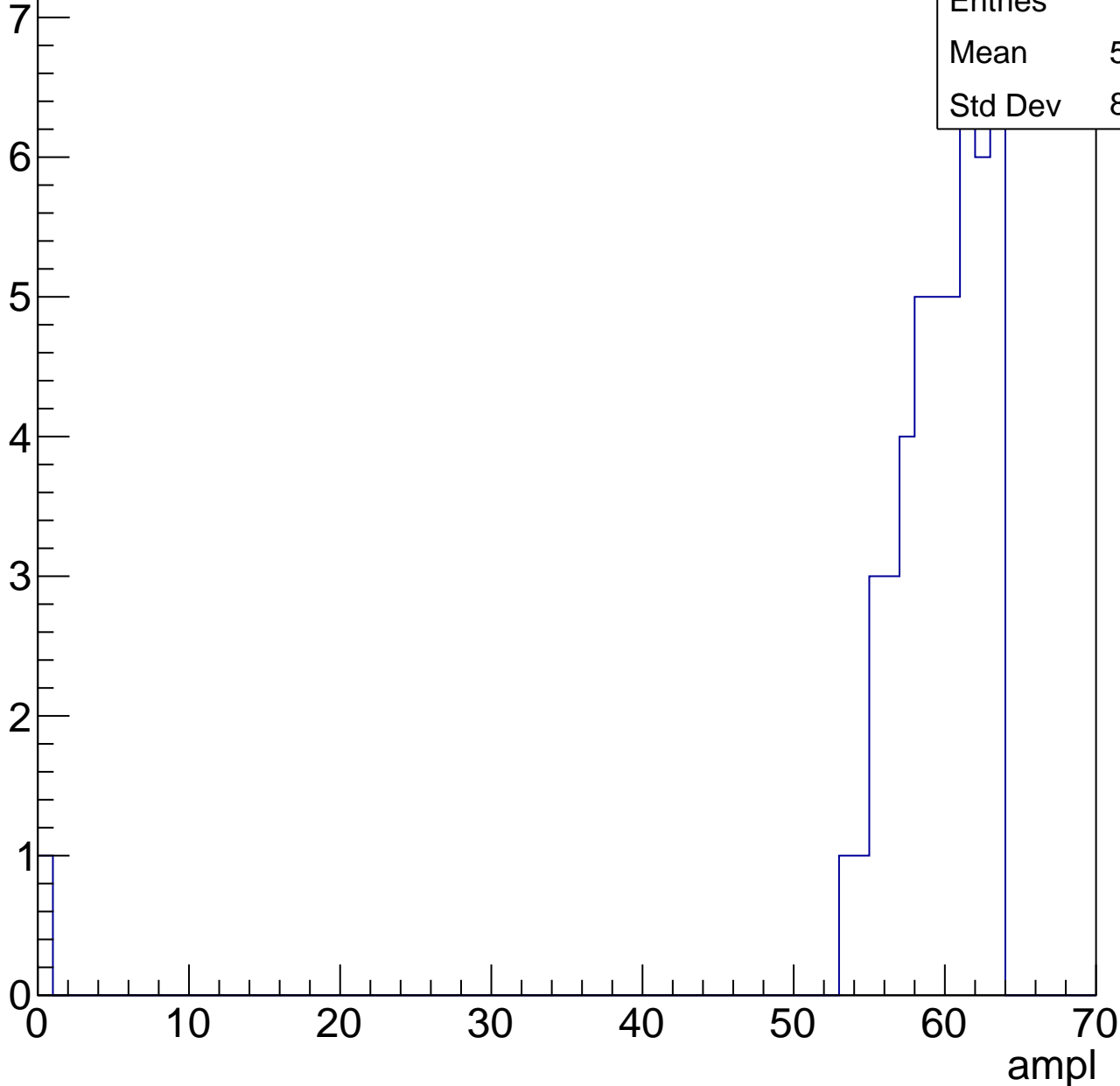


# B1L003S, U18-ch57, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

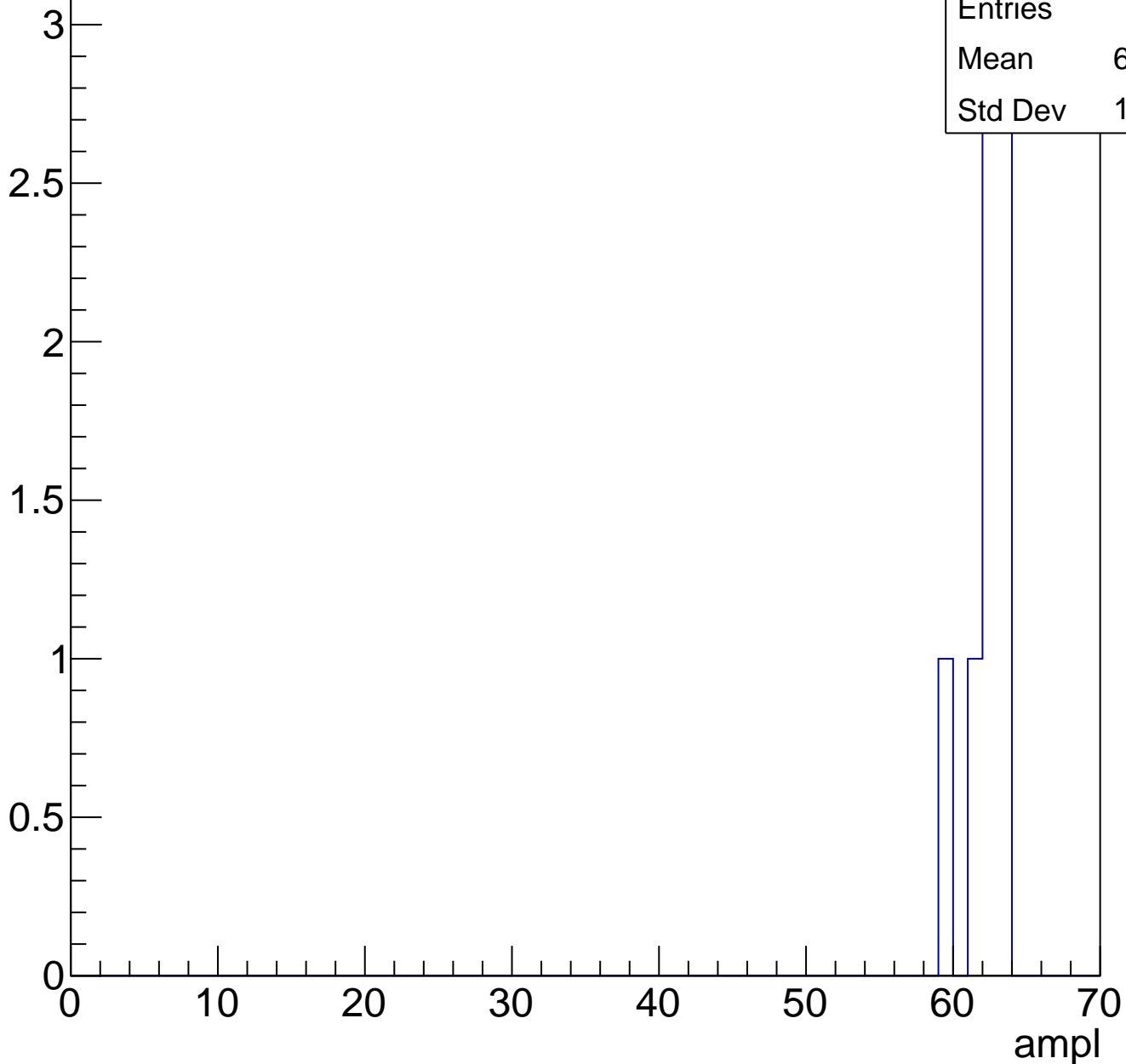
Entries	48
Mean	58.19
Std Dev	8.904



# B1L003S, U18-ch57, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

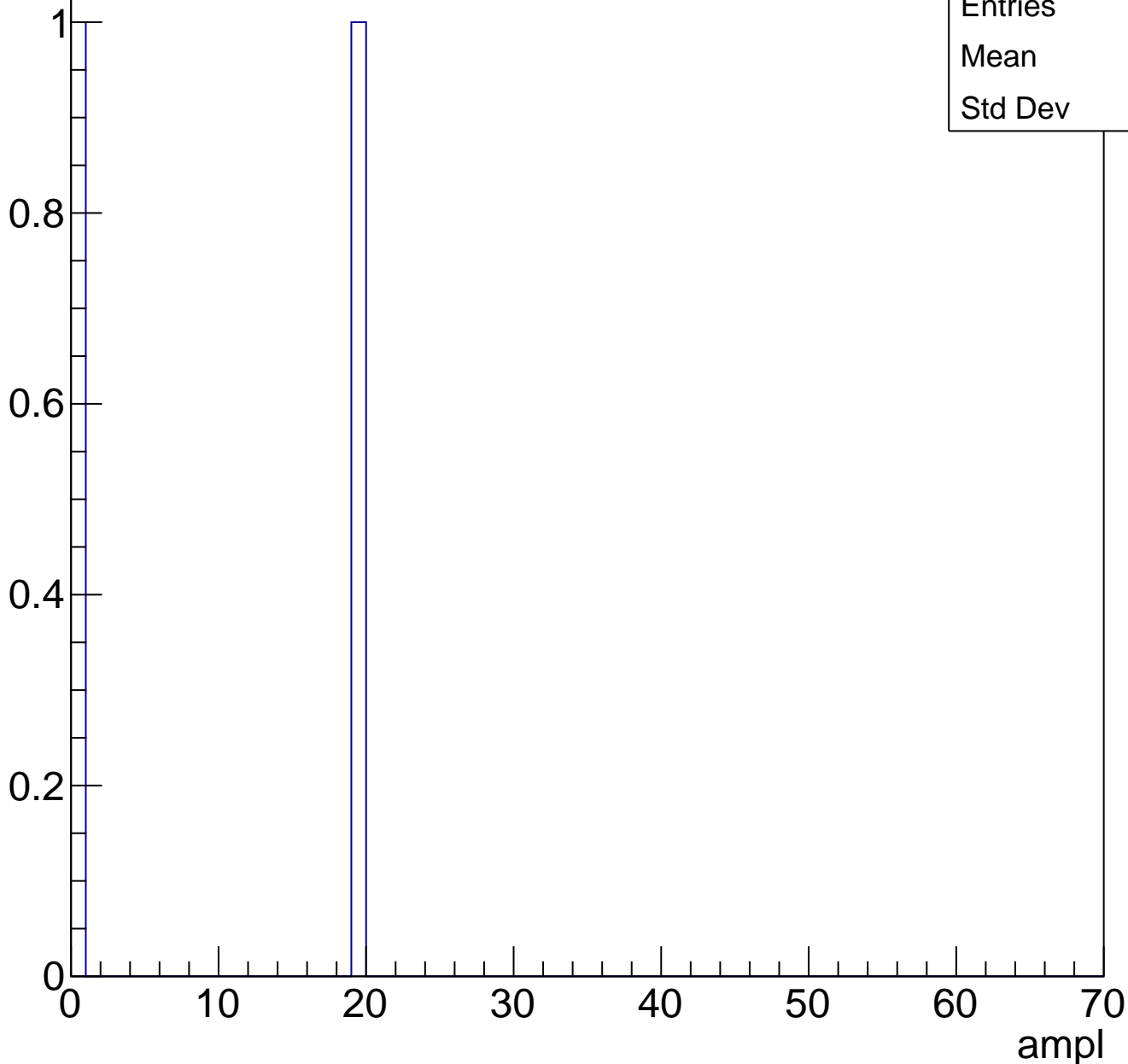




# B1L003S, U18-ch57, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	2
Mean	9.5
Std Dev	9.5

# B1L003S, U18-ch58, adc0

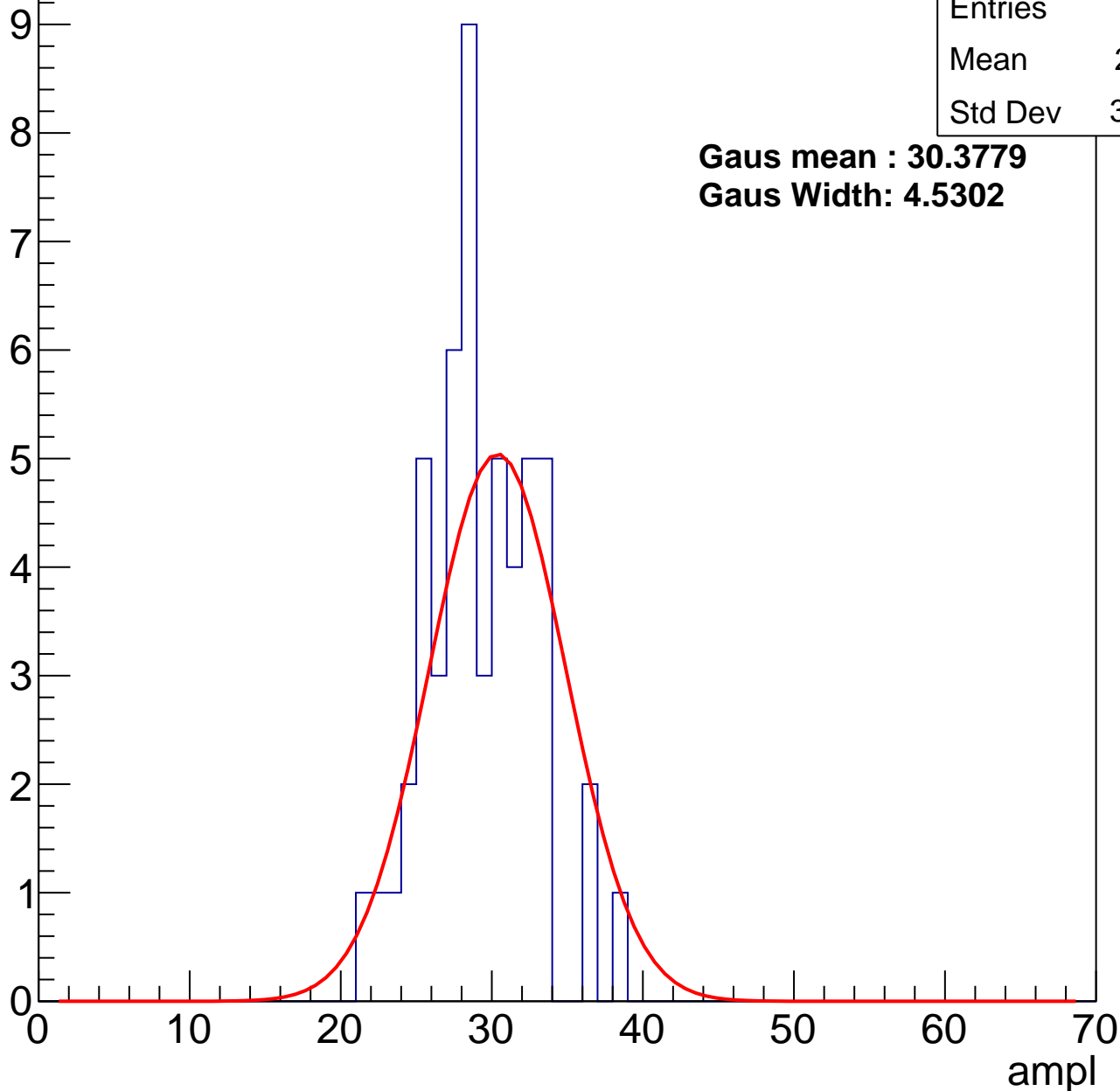
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	53
Mean	28.81
Std Dev	3.535

**Gaus mean : 30.3779**

**Gaus Width: 4.5302**



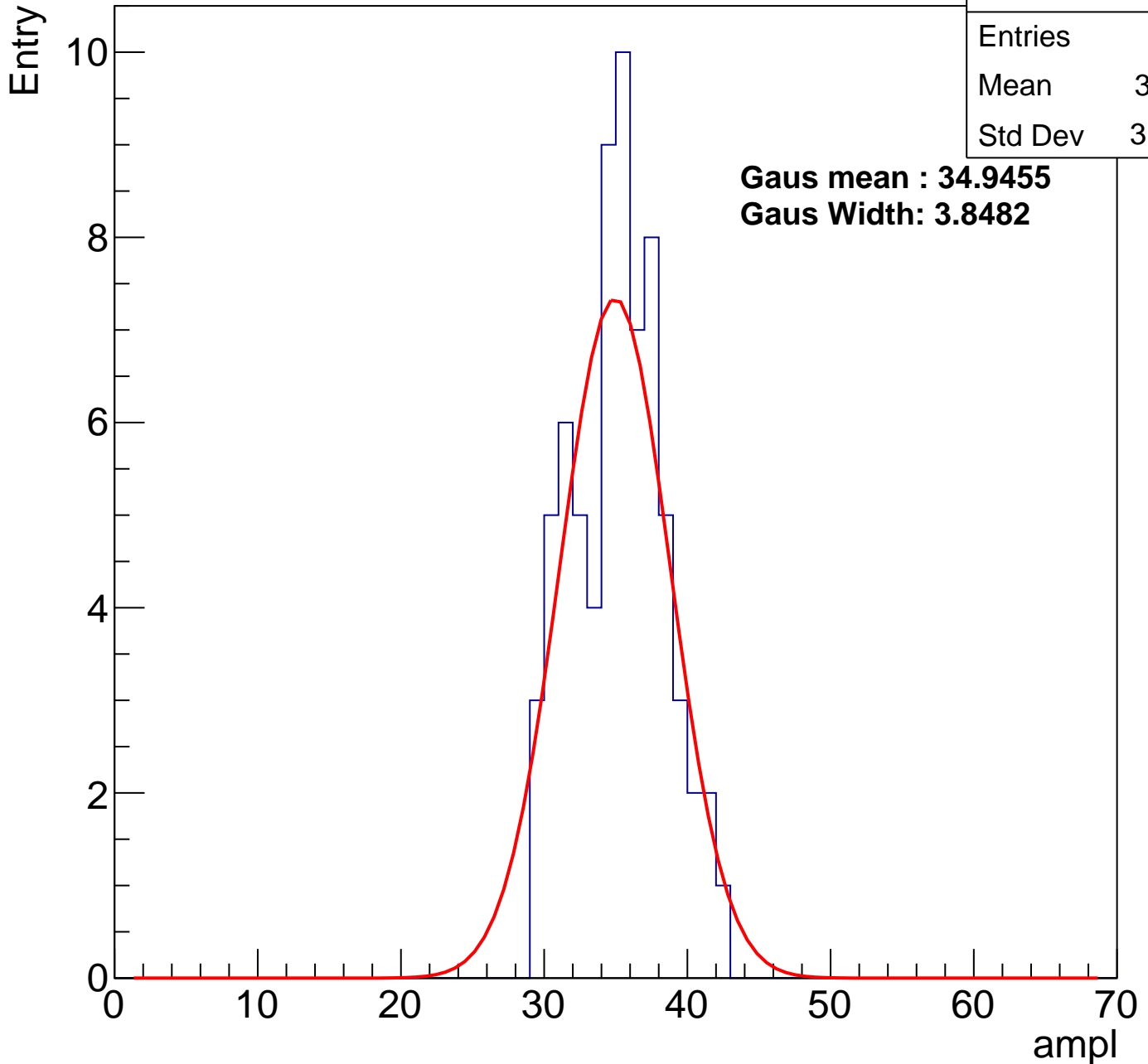
# B1L003S, U18-ch58, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	70
Mean	34.71
Std Dev	3.154

**Gaus mean : 34.9455**

**Gaus Width: 3.8482**



# B1L003S, U18-ch58, adc2

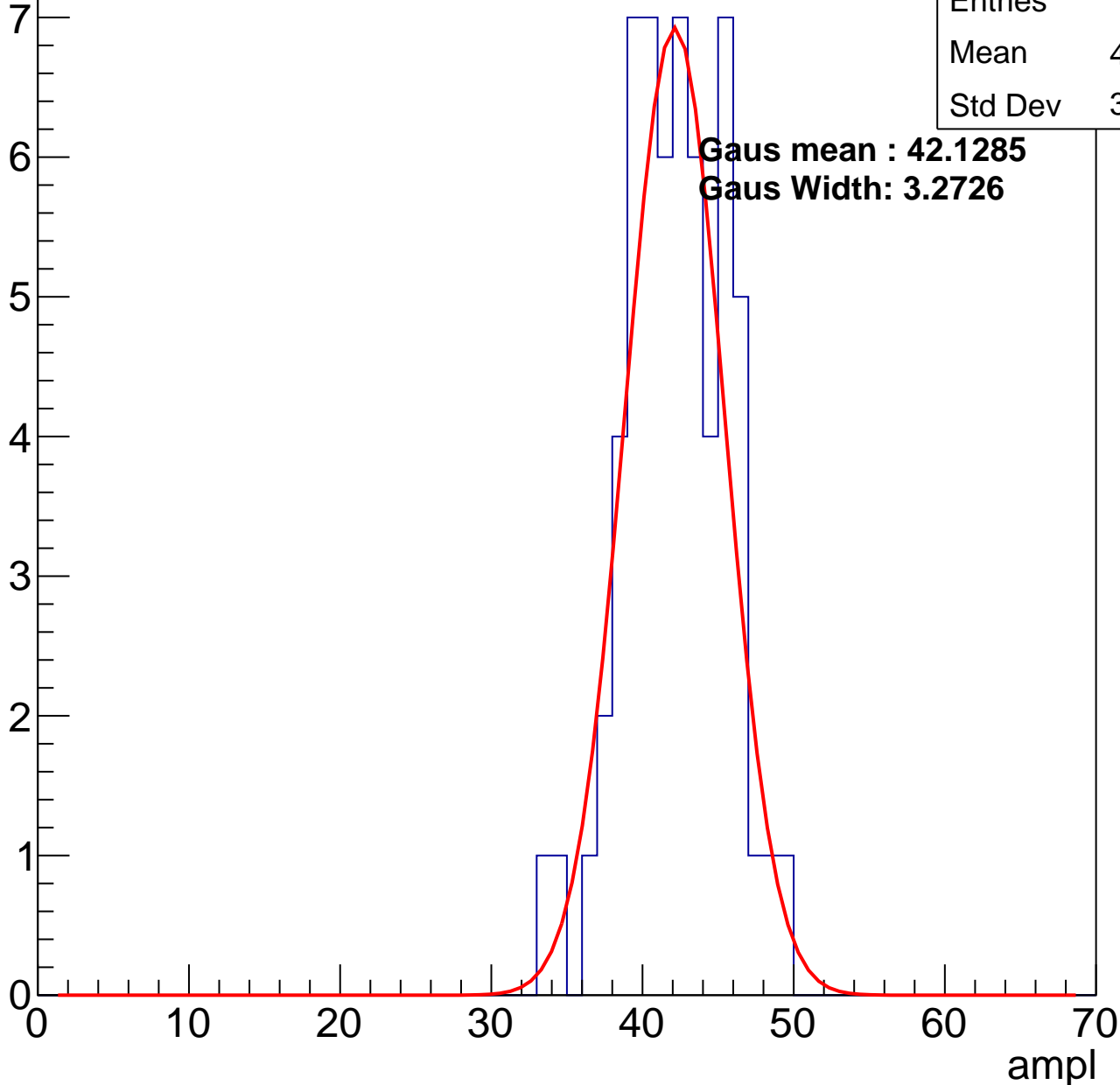
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	61
Mean	41.72
Std Dev	3.295

**Gaus mean : 42.1285**

**Gaus Width: 3.2726**

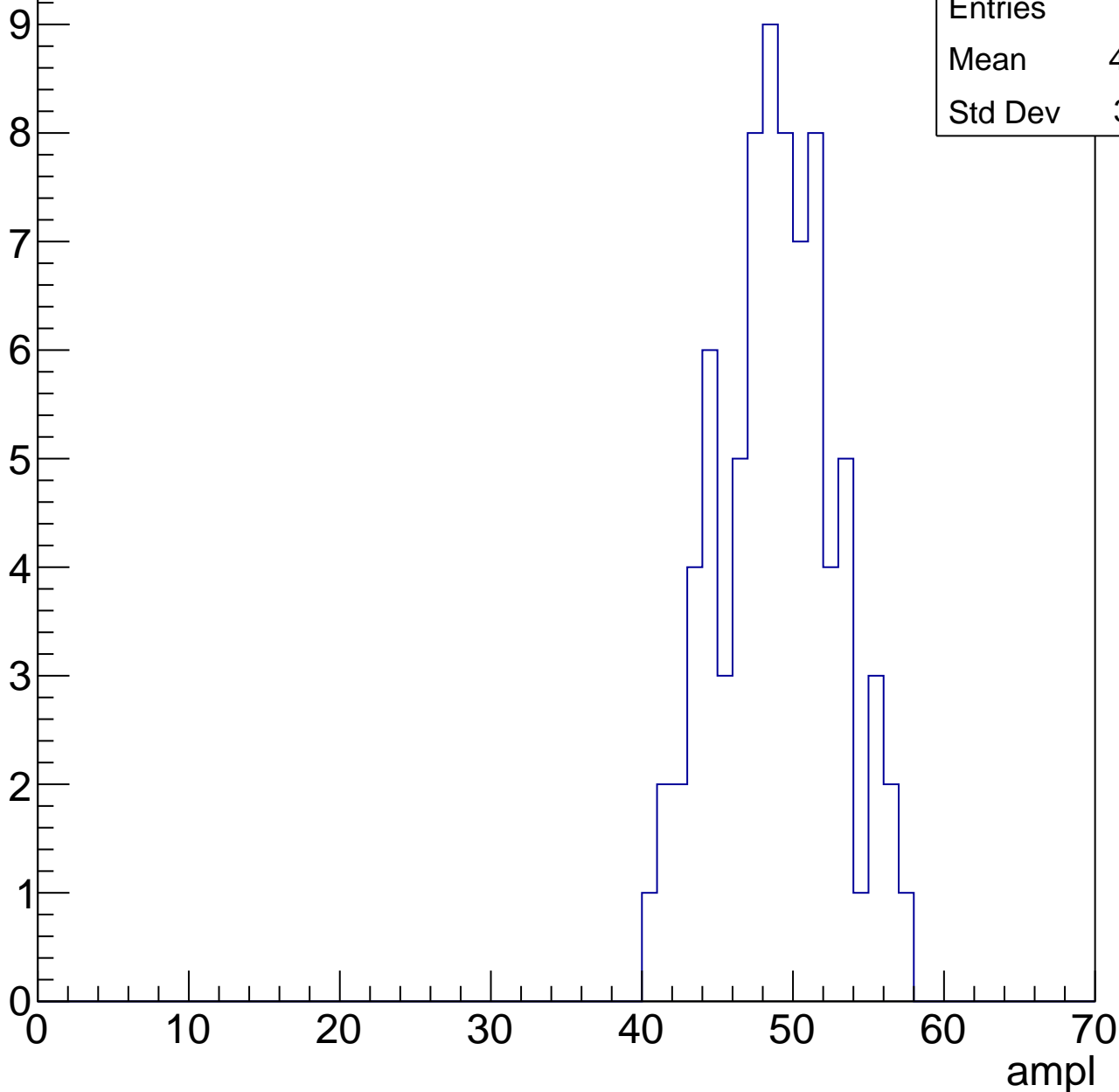


# B1L003S, U18-ch58, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	79
Mean	48.43
Std Dev	3.831

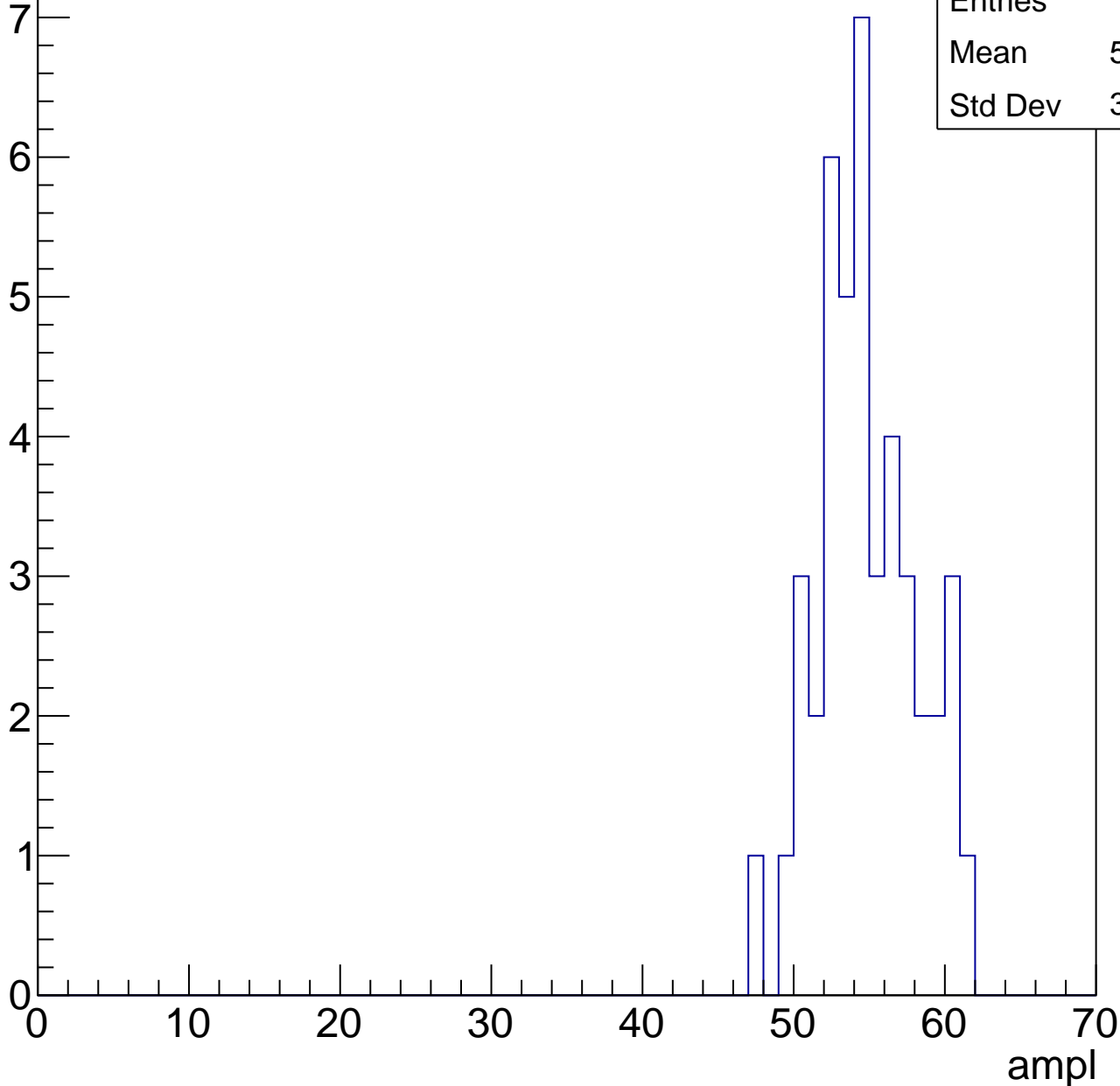


# B1L003S, U18-ch58, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

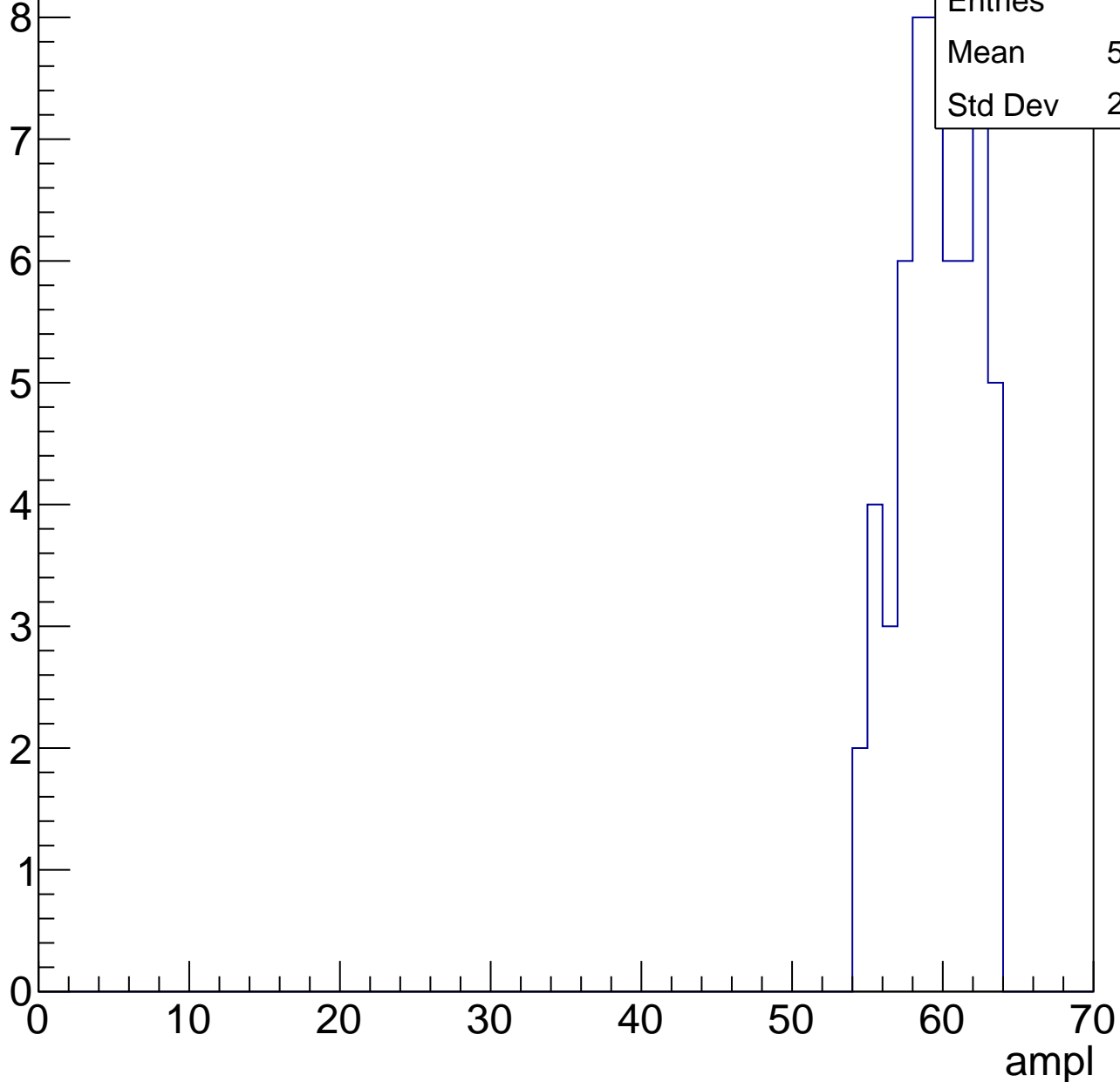
Entries	43
Mean	54.37
Std Dev	3.228



# B1L003S, U18-ch58, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

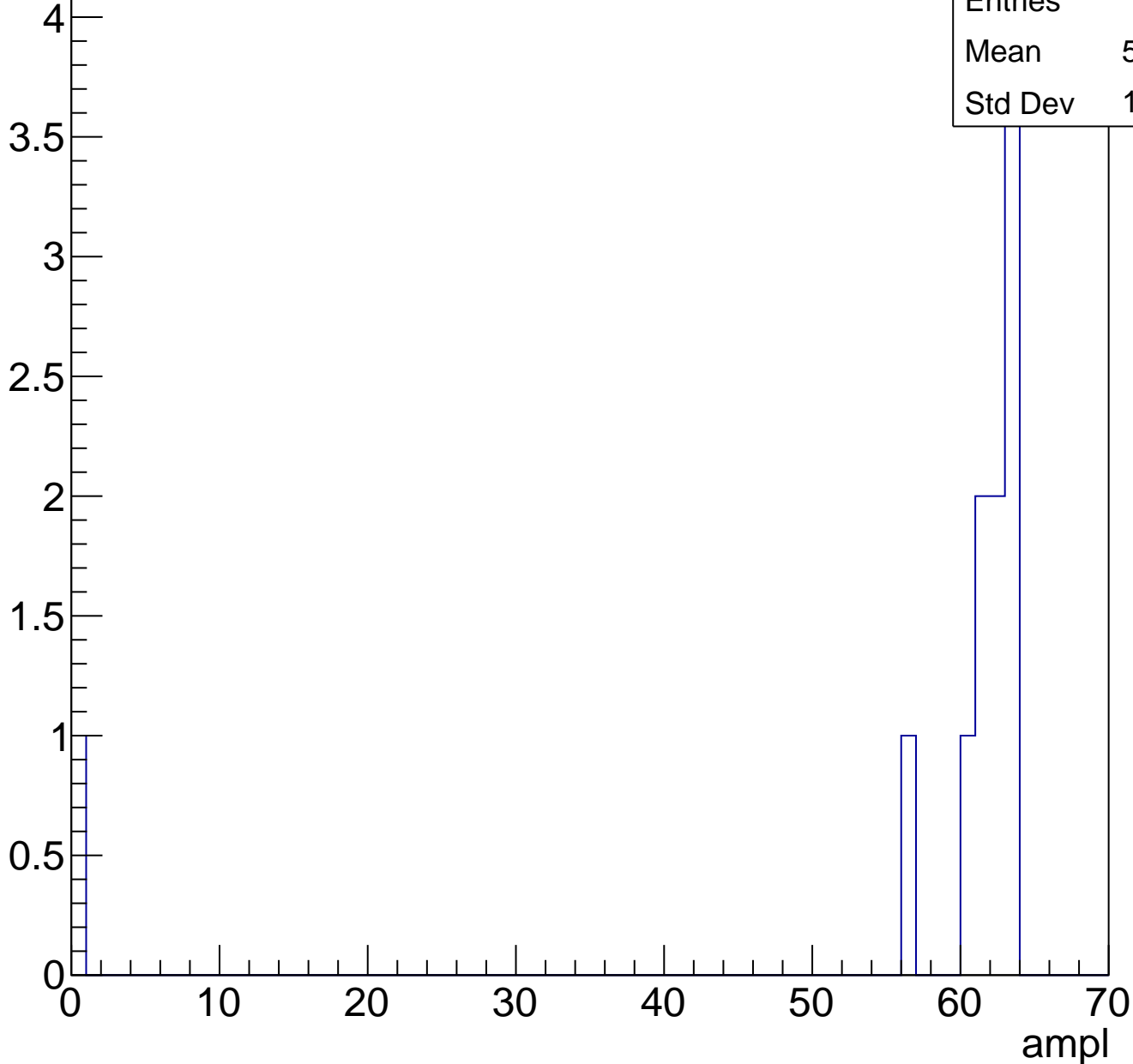
Entry



# B1L003S, U18-ch58, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

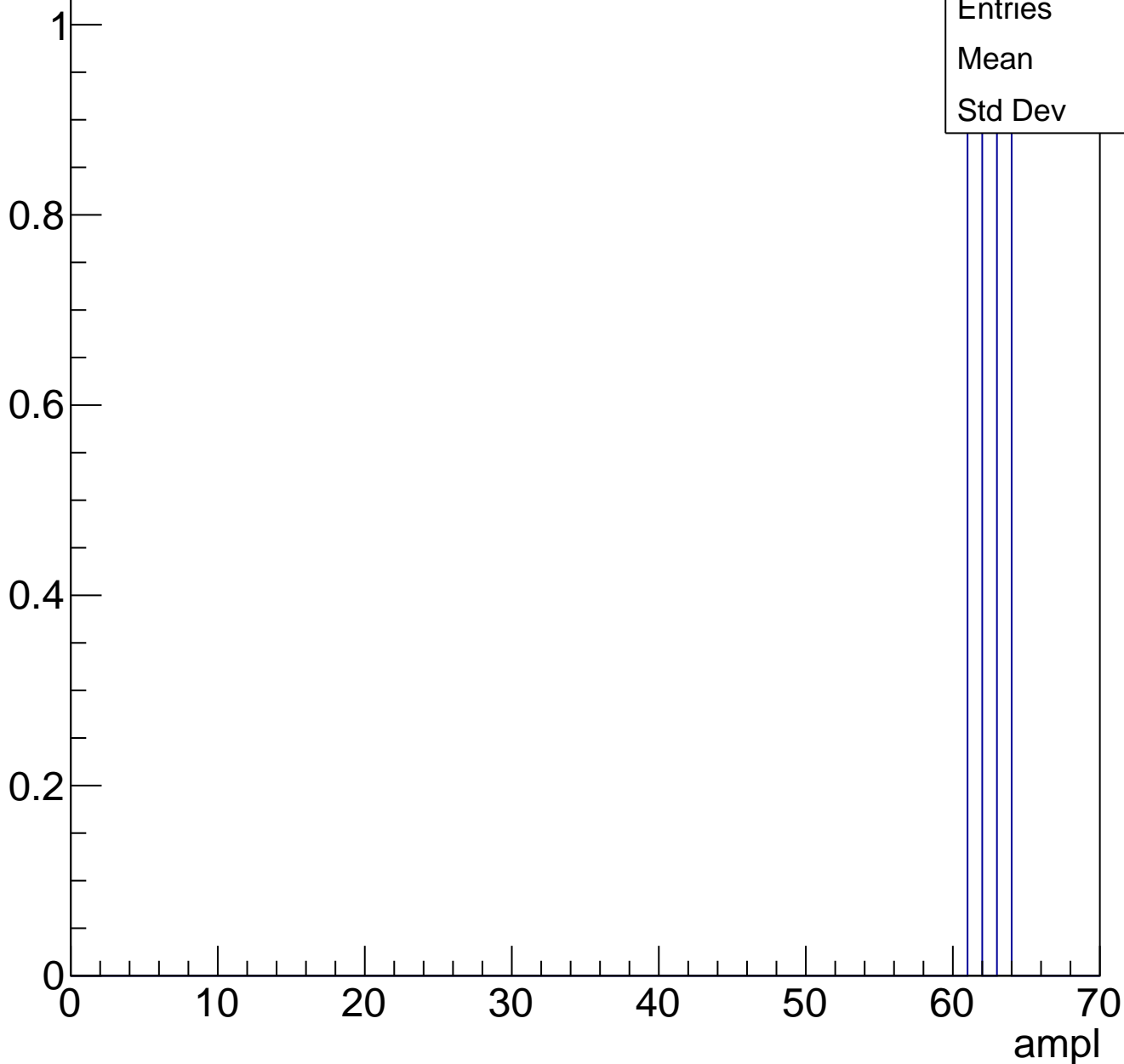




# B1L003S, U18-ch58, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U18-ch59, adc0

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	62
Mean	27.08
Std Dev	4.956

**Gaus mean : 28.6923**

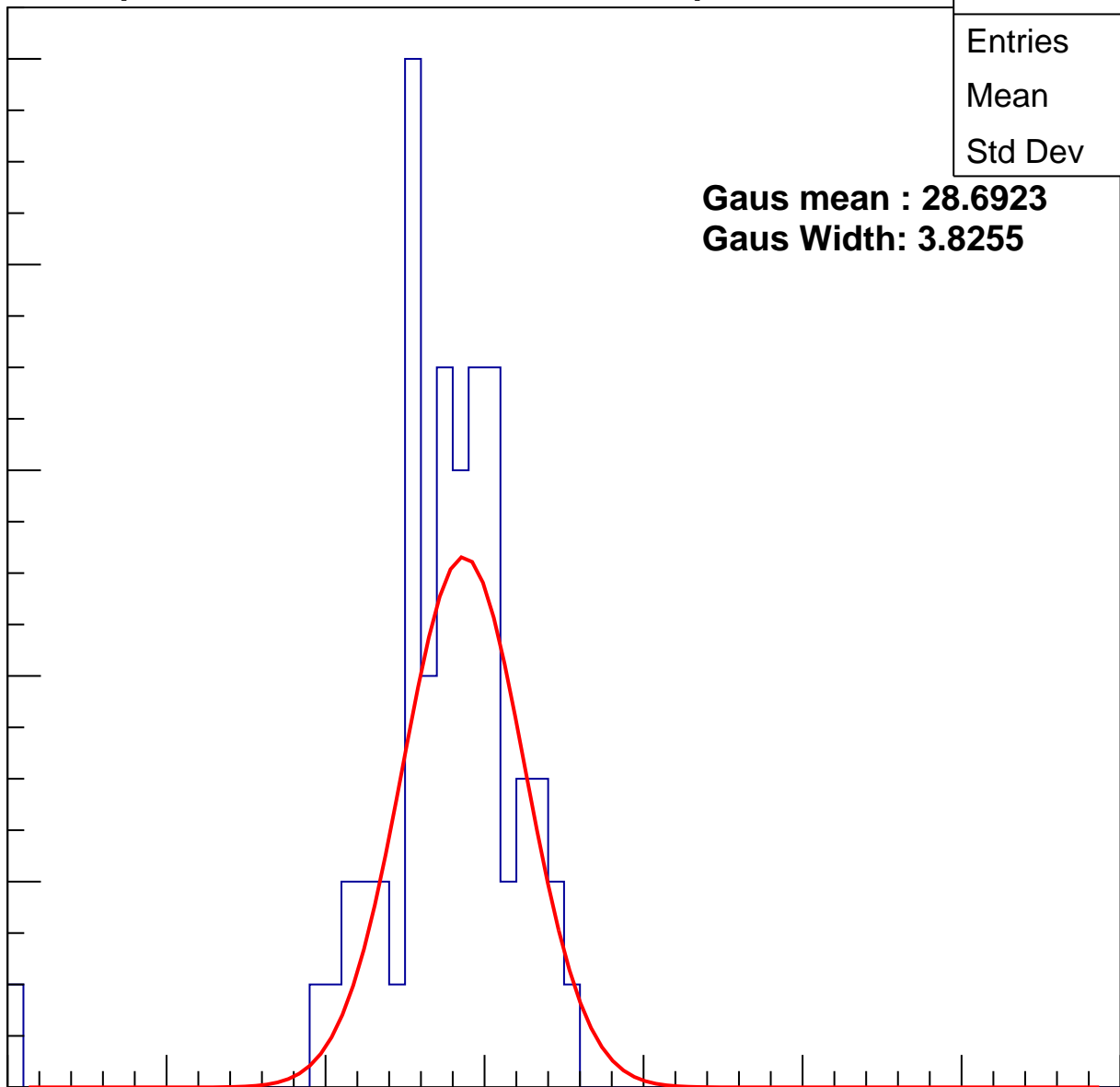
**Gaus Width: 3.8255**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



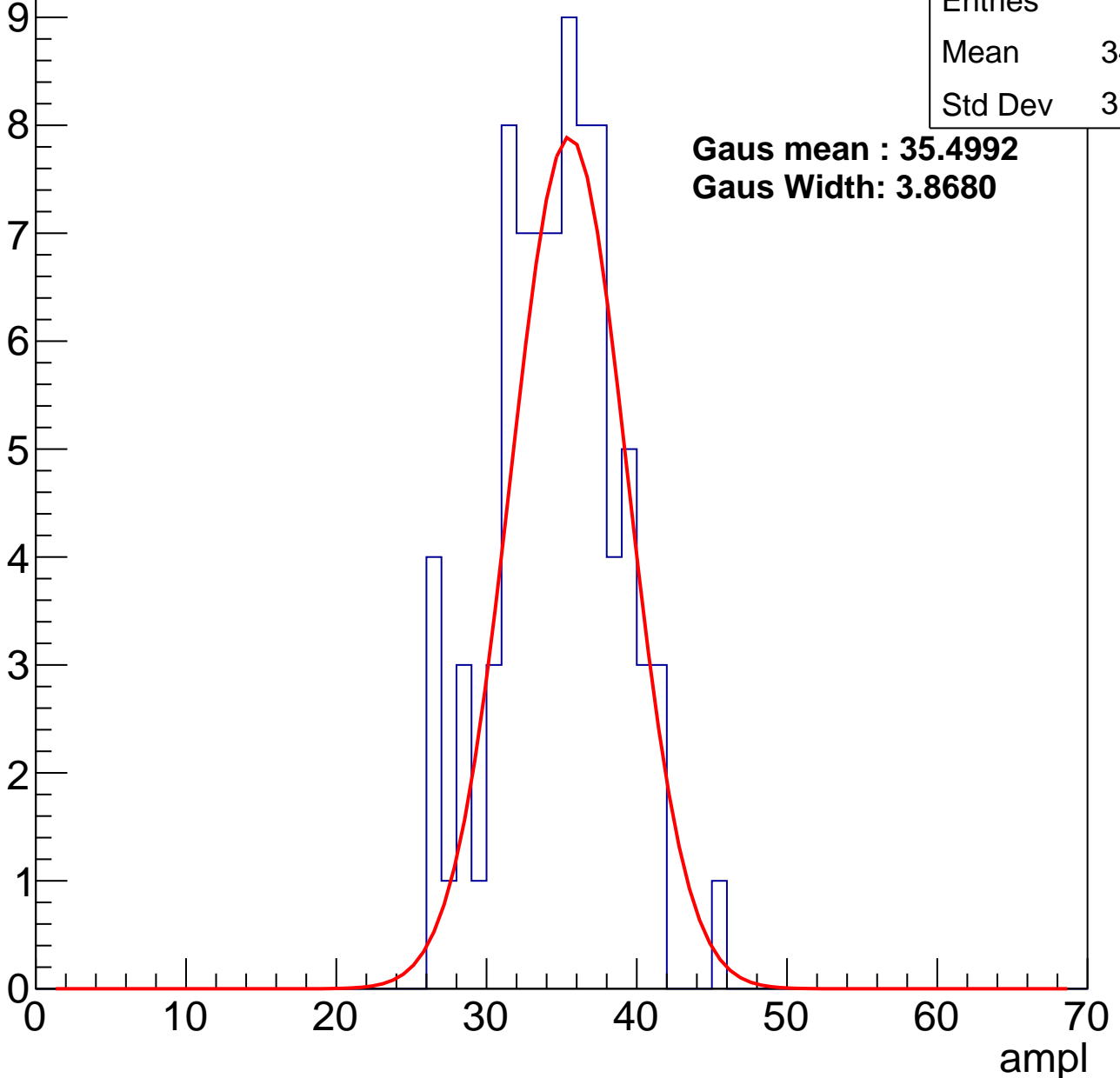
# B1L003S, U18-ch59, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	82
Mean	34.26
Std Dev	3.929

**Gaus mean : 35.4992**  
**Gaus Width: 3.8680**



# B1L003S, U18-ch59, adc2

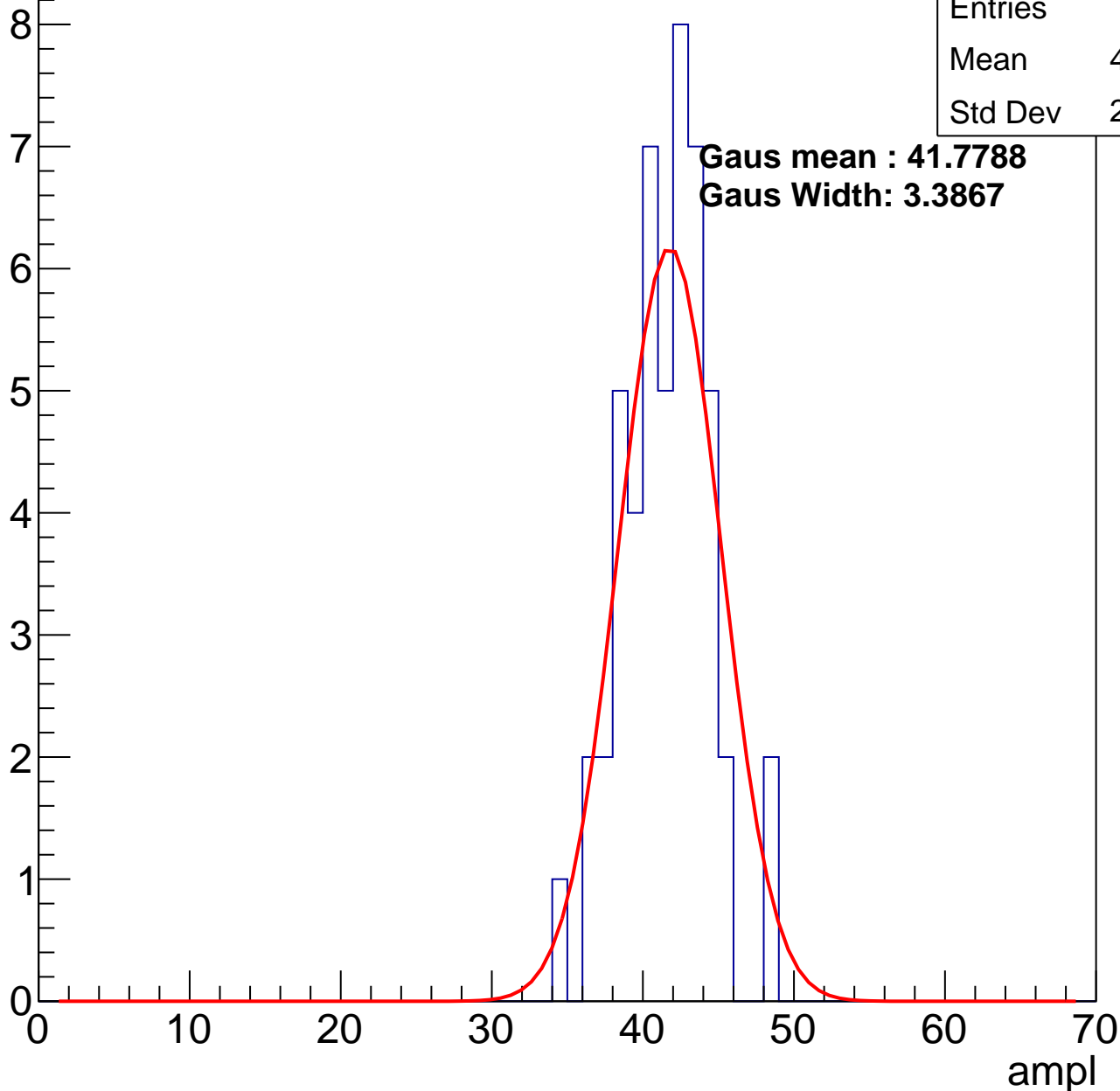
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	50
Mean	41.08
Std Dev	2.862

**Gaus mean : 41.7788**

**Gaus Width: 3.3867**

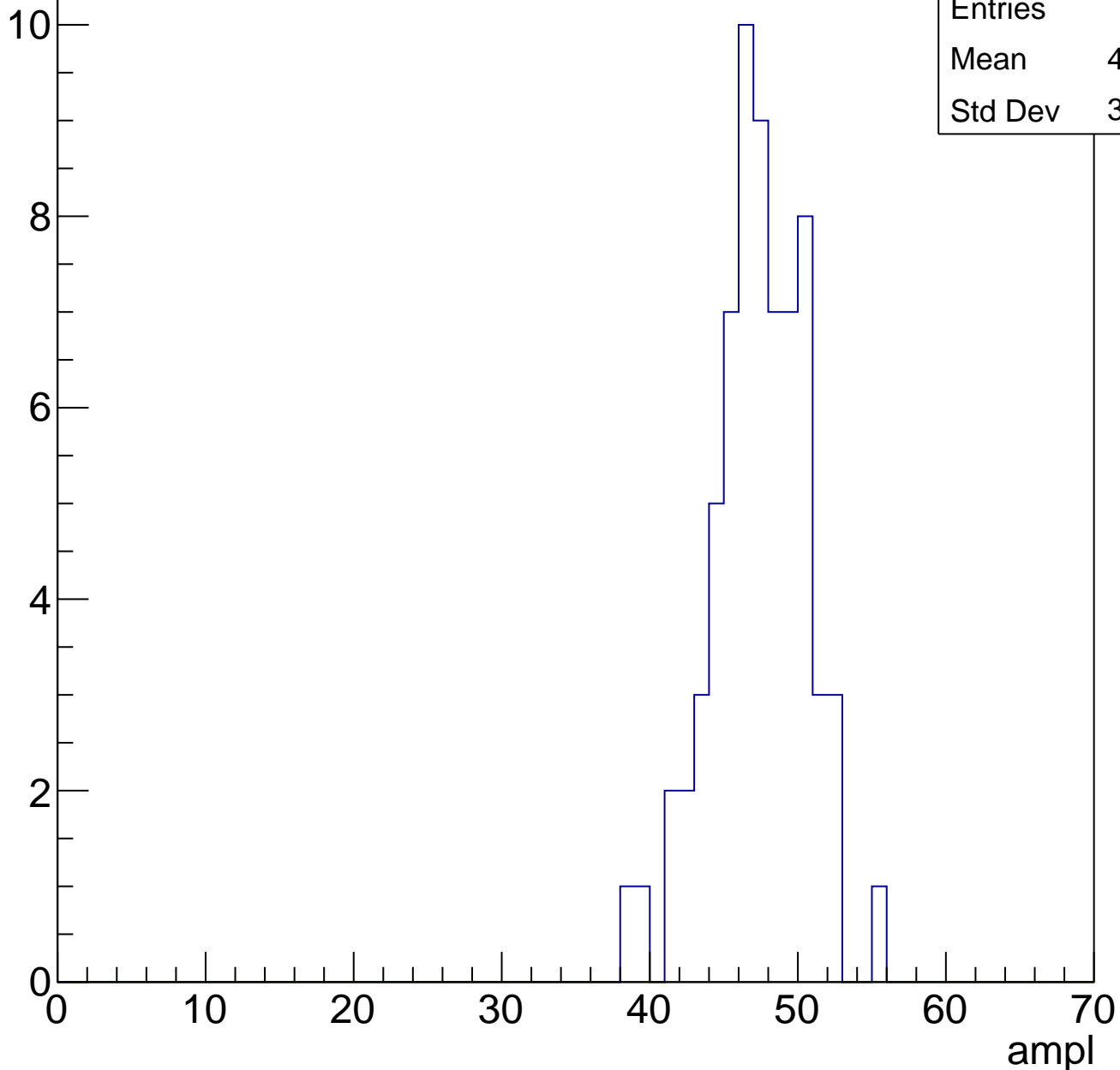


# B1L003S, U18-ch59, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	69
Mean	46.86
Std Dev	3.164

Entry

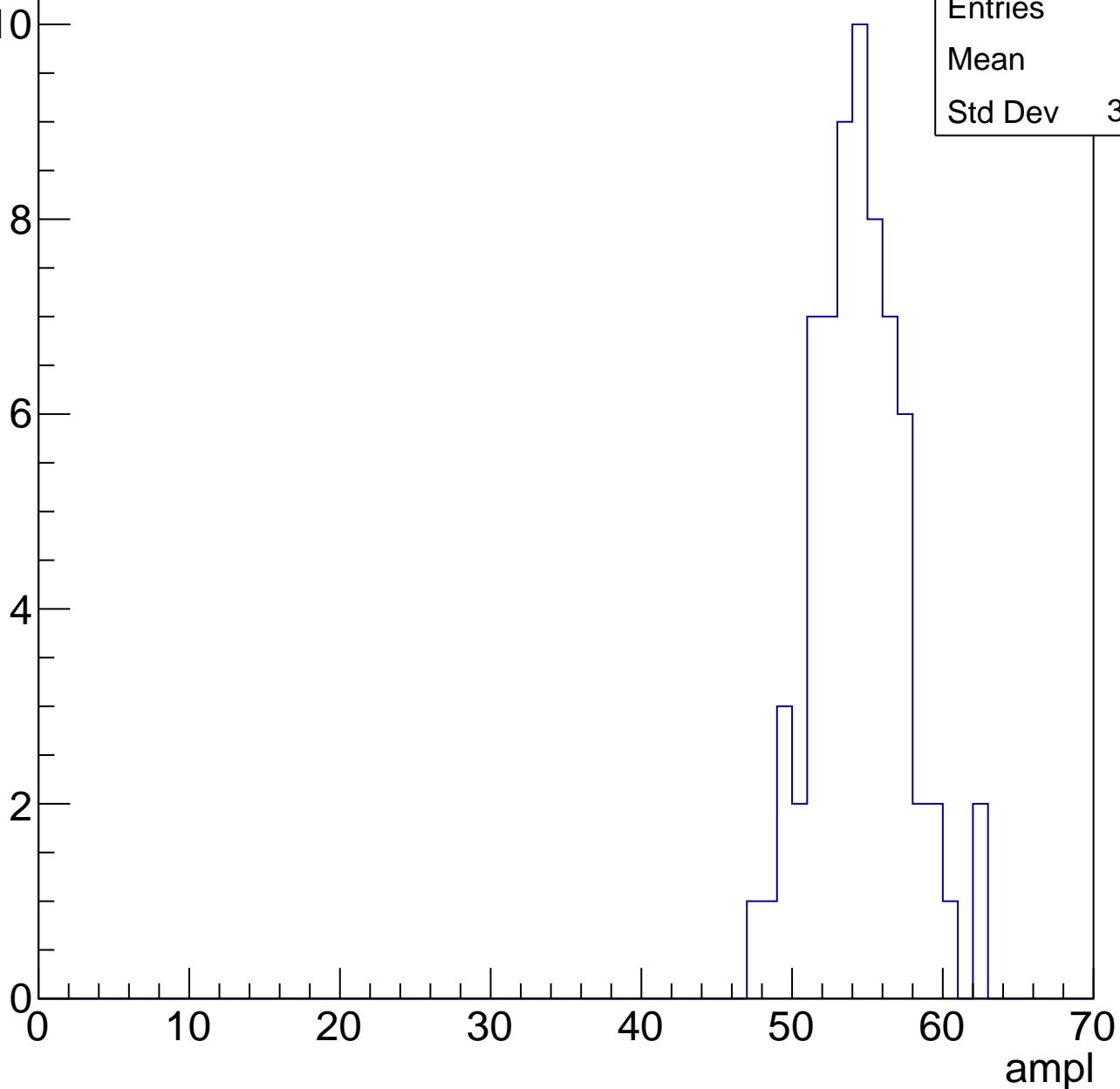


# B1L003S, U18-ch59, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	68
Mean	54
Std Dev	3.039

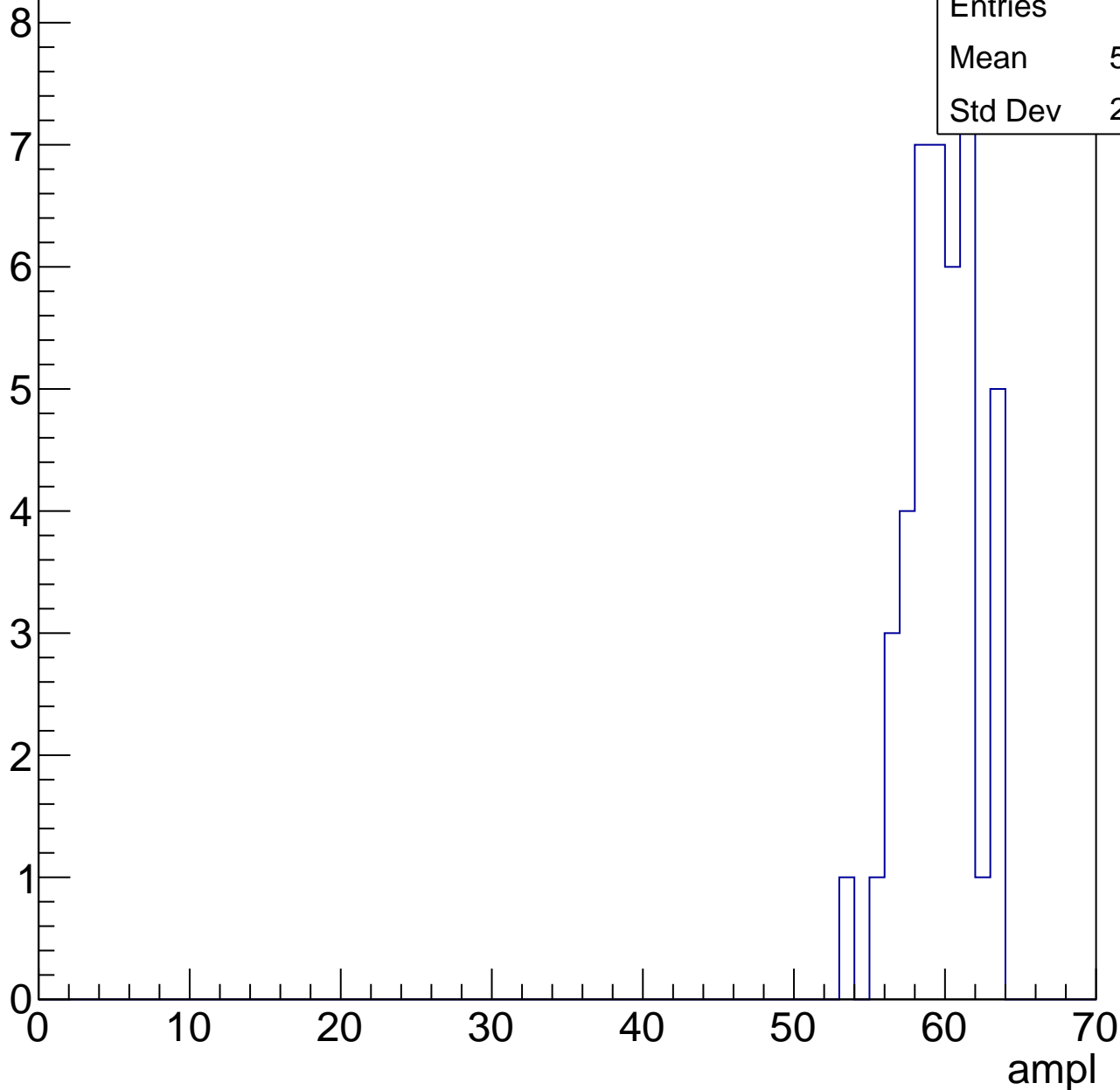


# B1L003S, U18-ch59, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	43
Mean	59.26
Std Dev	2.293

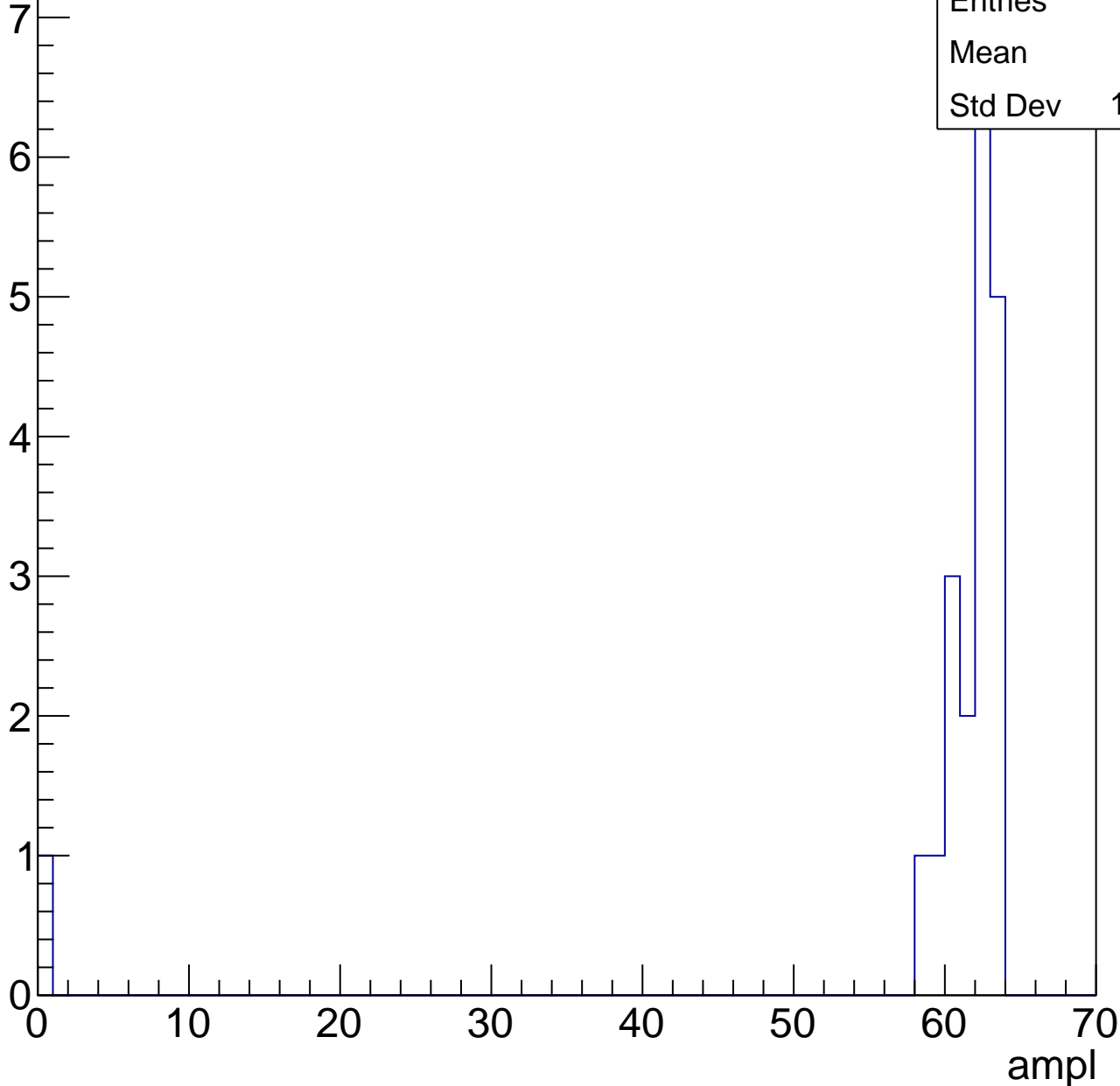


# B1L003S, U18-ch59, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	20
Mean	58.4
Std Dev	13.47





# B1L003S, U18-ch59, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch60, adc0

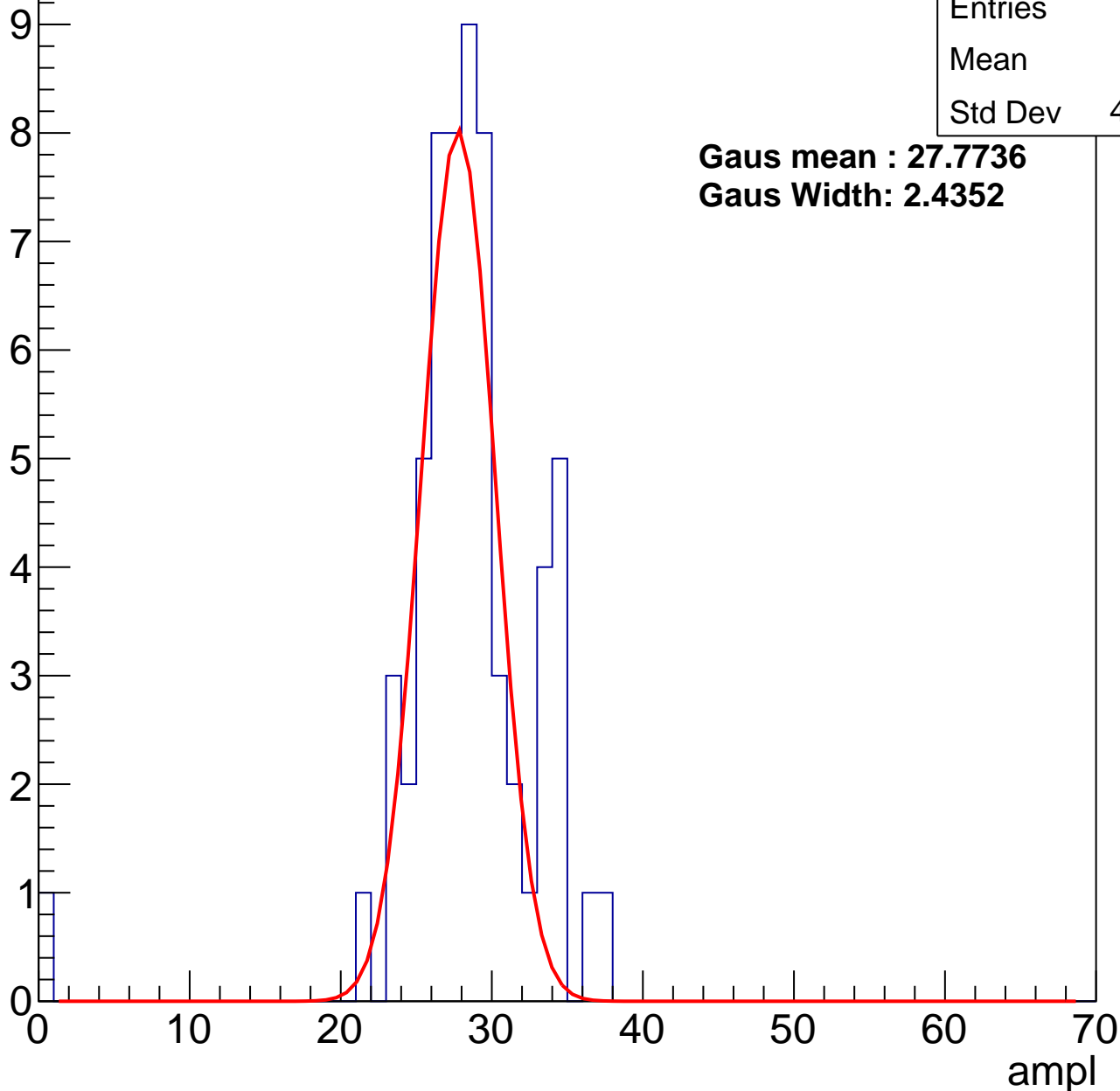
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	62
Mean	27.9
Std Dev	4.924

**Gaus mean : 27.7736**

**Gaus Width: 2.4352**



# B1L003S, U18-ch60, adc1

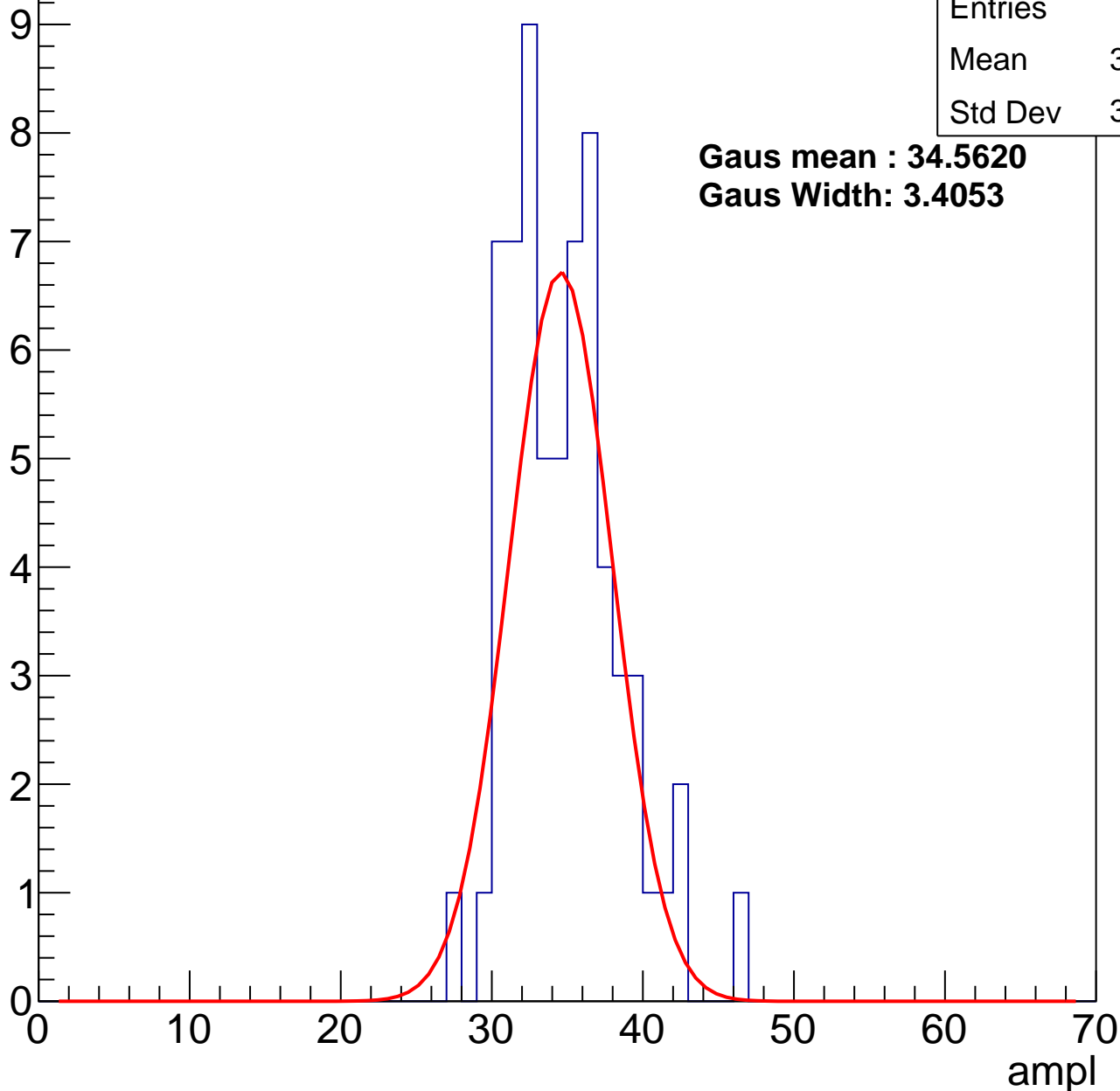
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	65
Mean	34.29
Std Dev	3.594

**Gaus mean : 34.5620**

**Gaus Width: 3.4053**



# B1L003S, U18-ch60, adc2

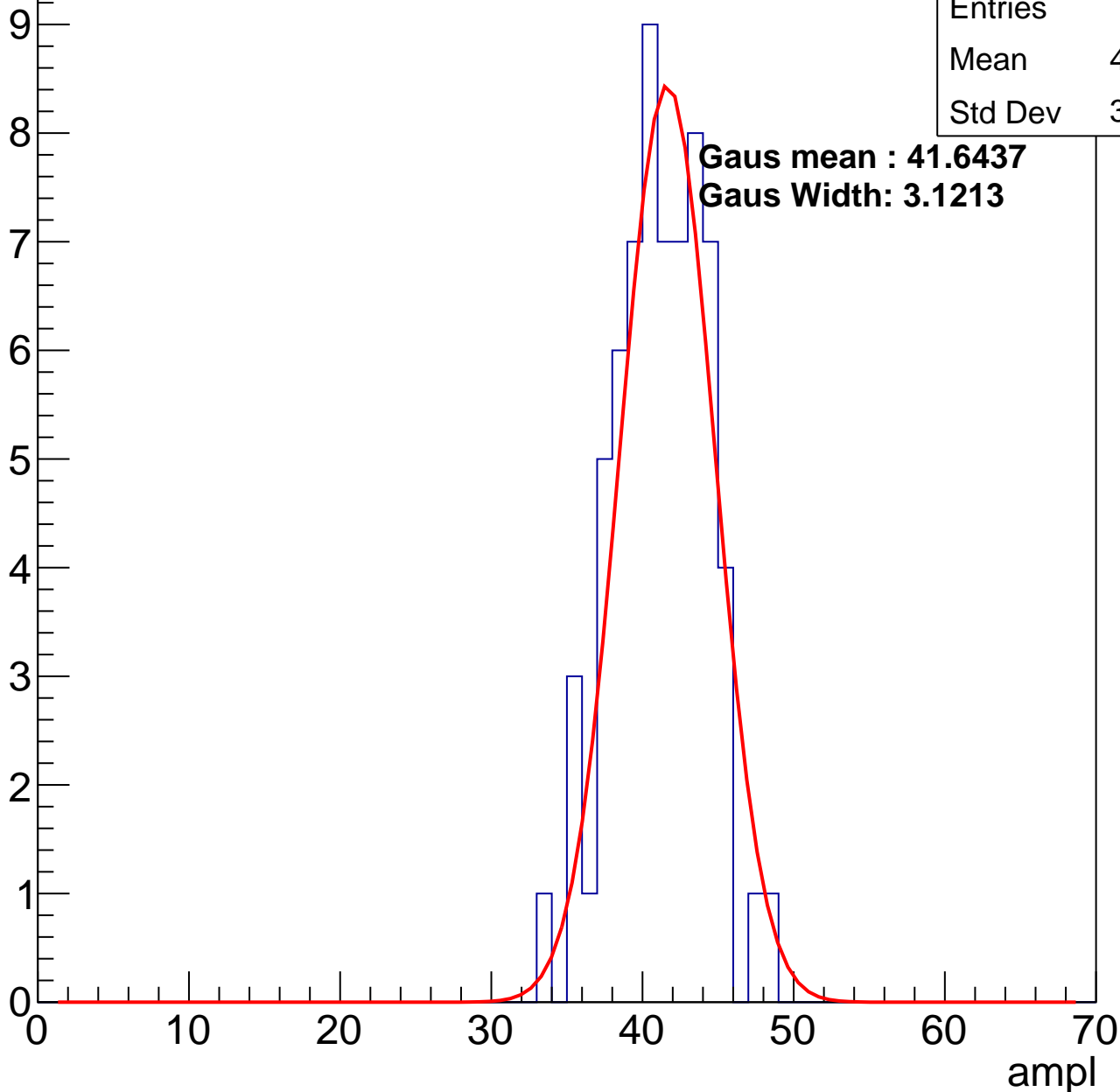
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	67
Mean	40.72
Std Dev	3.026

**Gaus mean : 41.6437**

**Gaus Width: 3.1213**

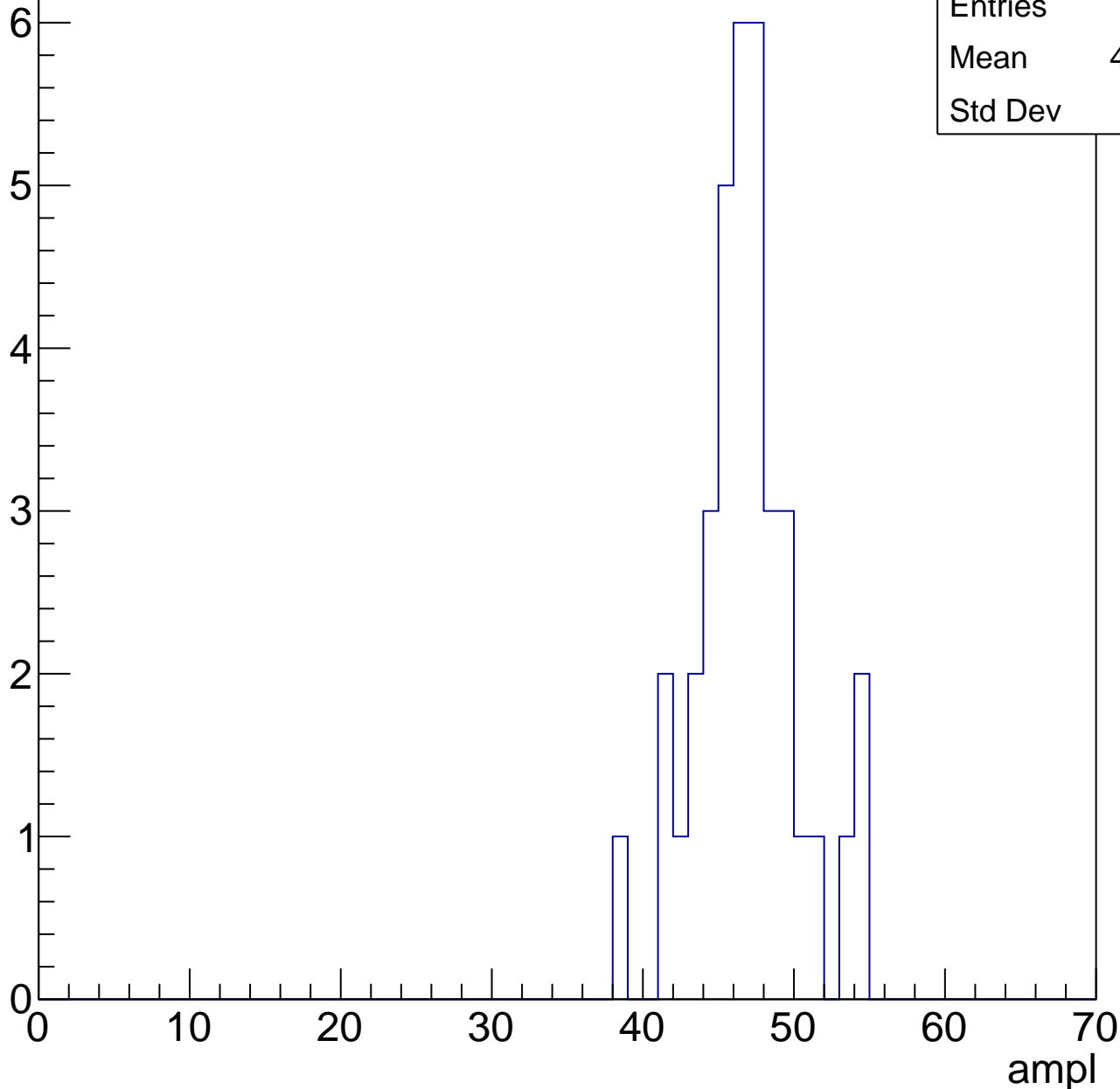


# B1L003S, U18-ch60, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	37
Mean	46.38
Std Dev	3.38

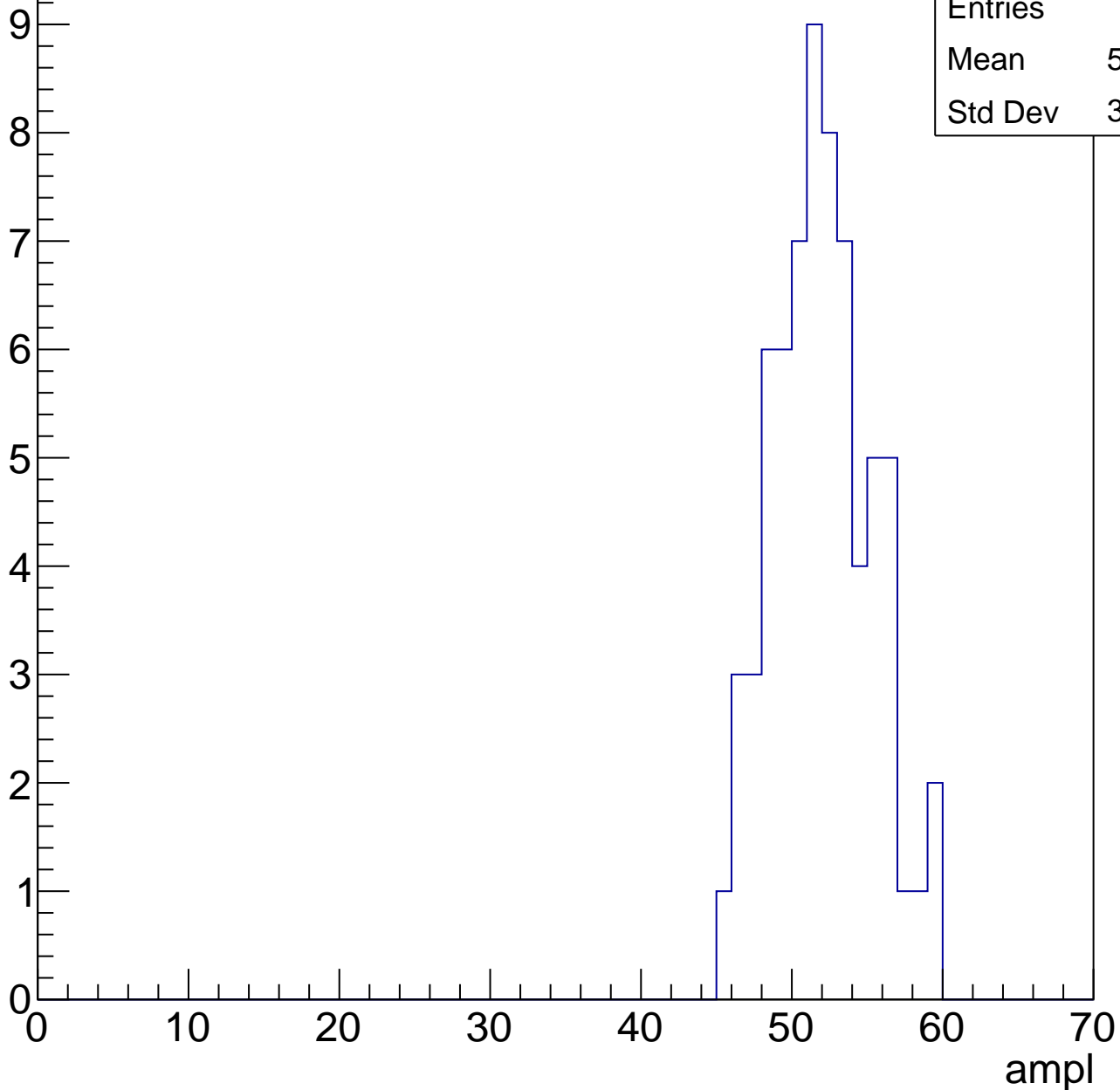


# B1L003S, U18-ch60, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	68
Mean	51.56
Std Dev	3.238

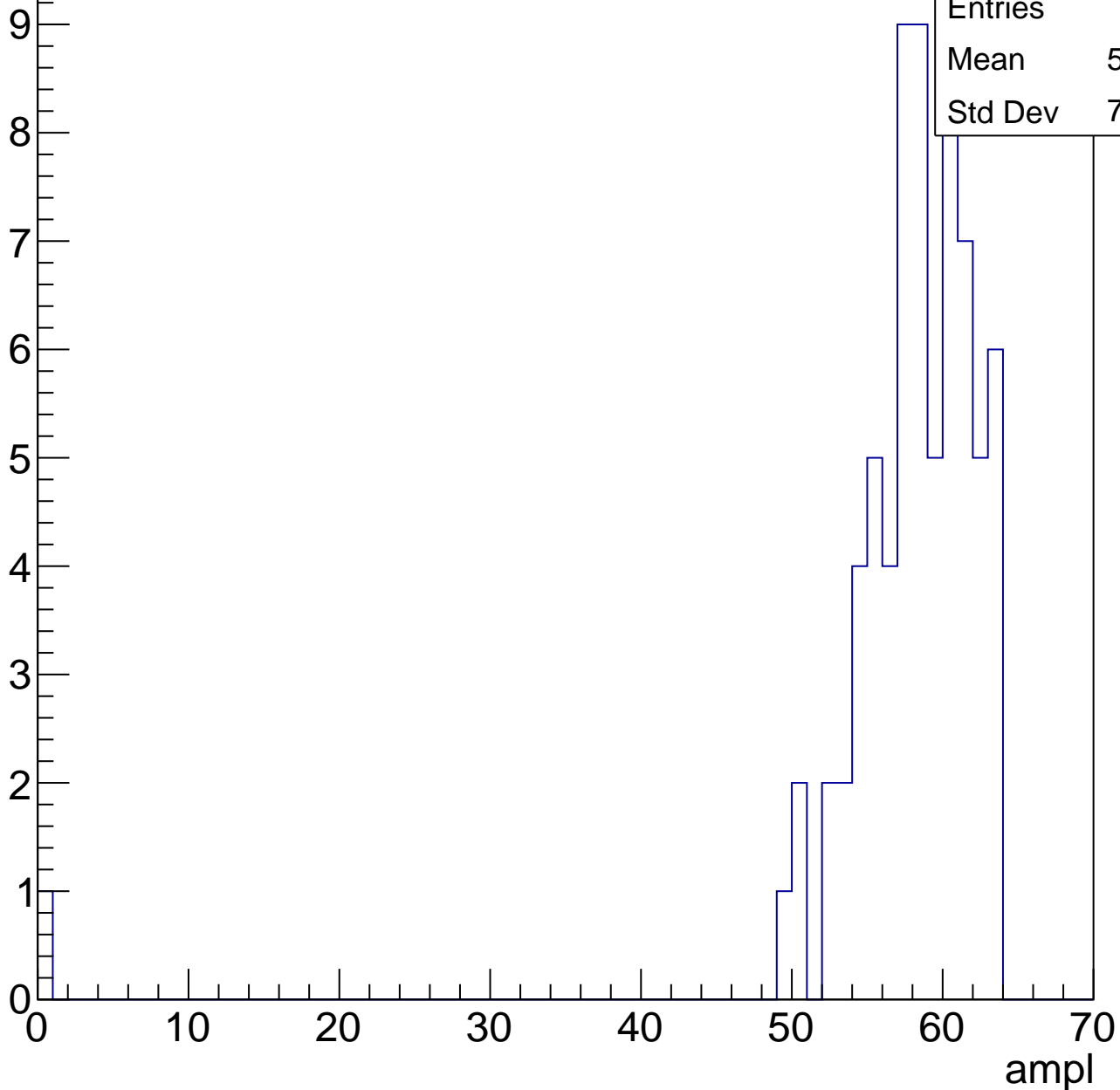


# B1L003S, U18-ch60, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	70
Mean	57.13
Std Dev	7.659

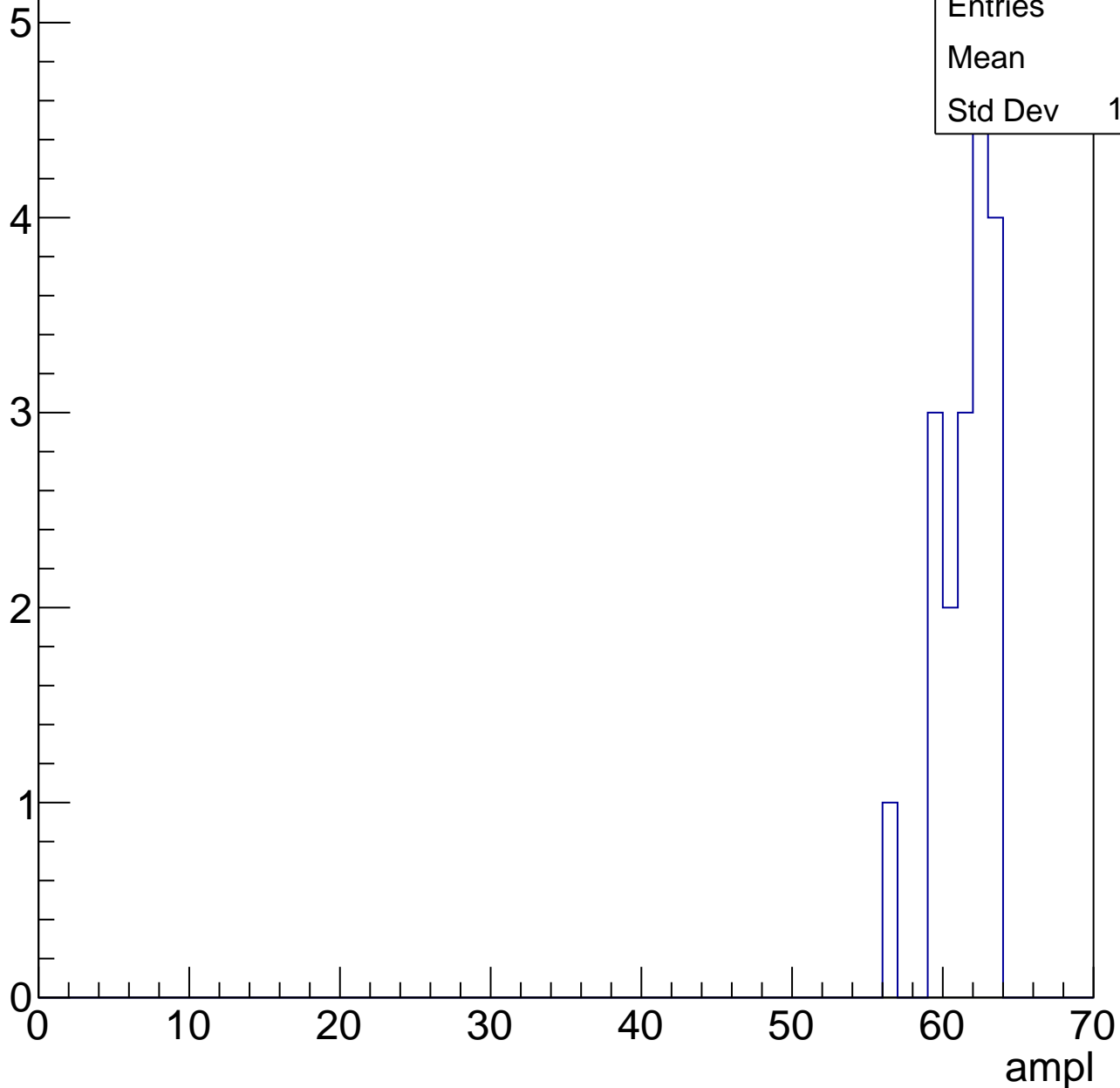


# B1L003S, U18-ch60, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	18
Mean	61
Std Dev	1.826





# B1L003S, U18-ch60, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

1  
0.8  
0.6  
0.4  
0.2  
0

Entries	1
Mean	20
Std Dev	0

ampl

# B1L003S, U18-ch61, adc0

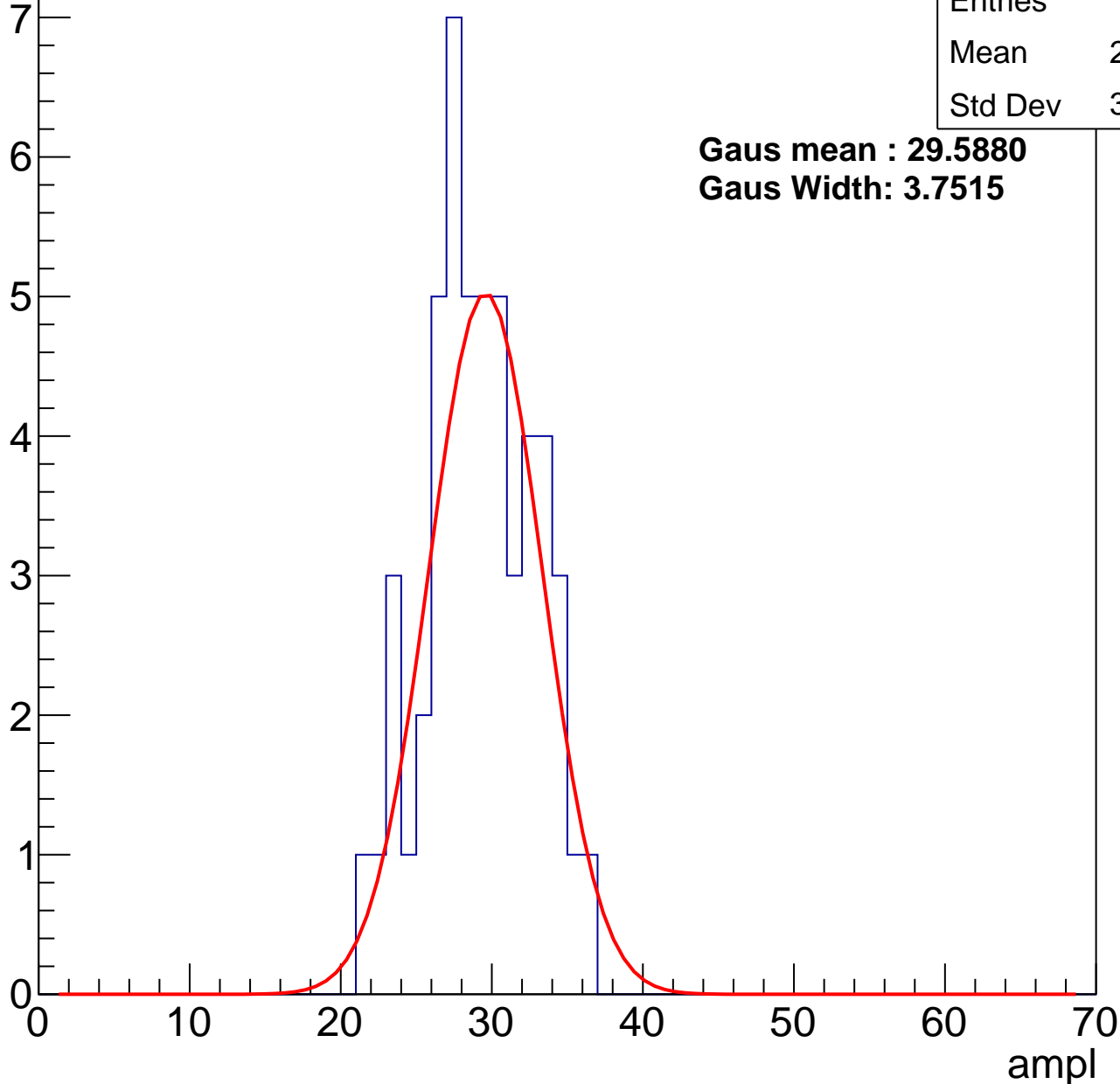
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	51
Mean	28.75
Std Dev	3.514

**Gaus mean : 29.5880**

**Gaus Width: 3.7515**



# B1L003S, U18-ch61, adc1

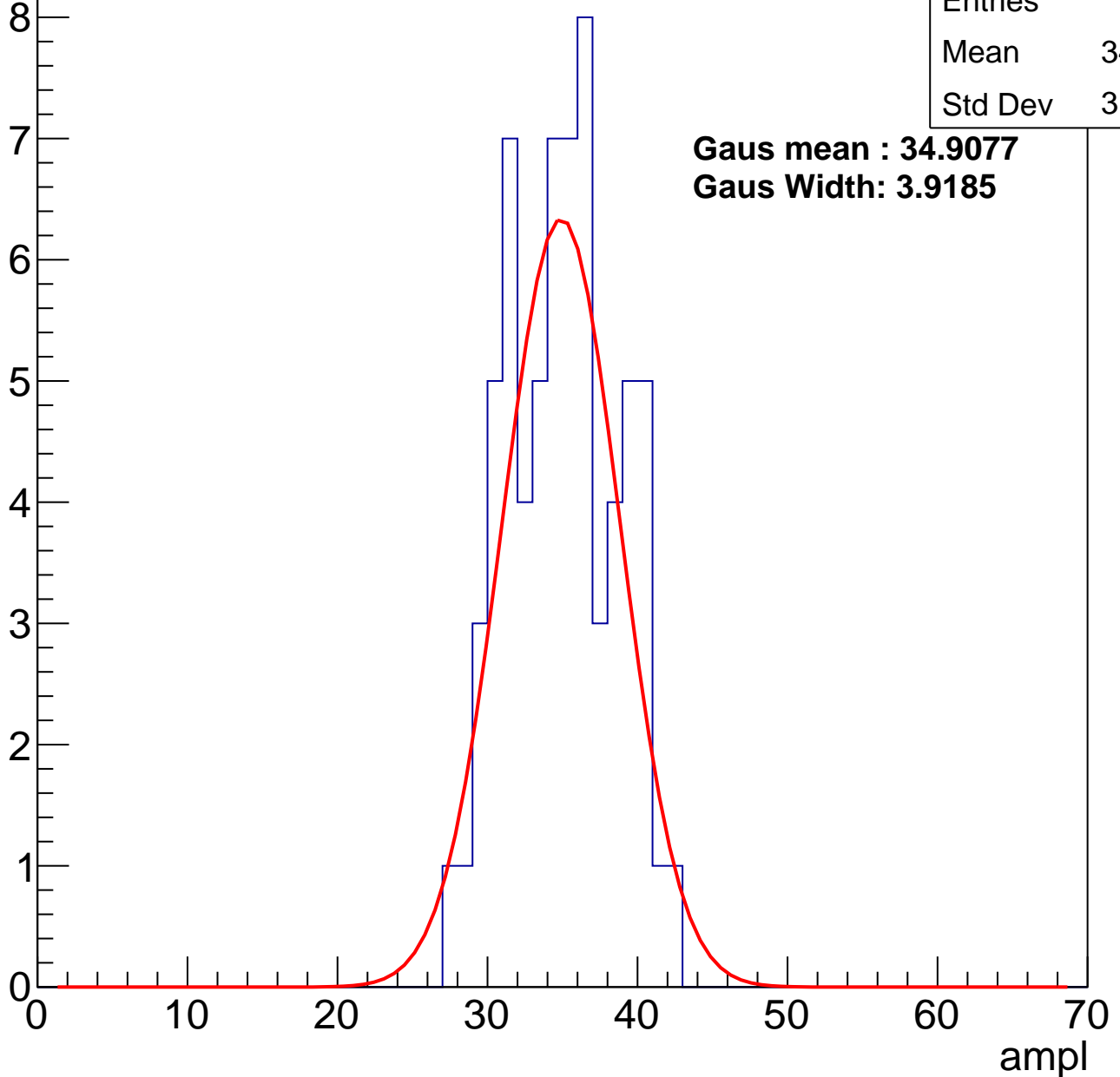
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	67
Mean	34.54
Std Dev	3.567

**Gaus mean : 34.9077**

**Gaus Width: 3.9185**



# B1L003S, U18-ch61, adc2

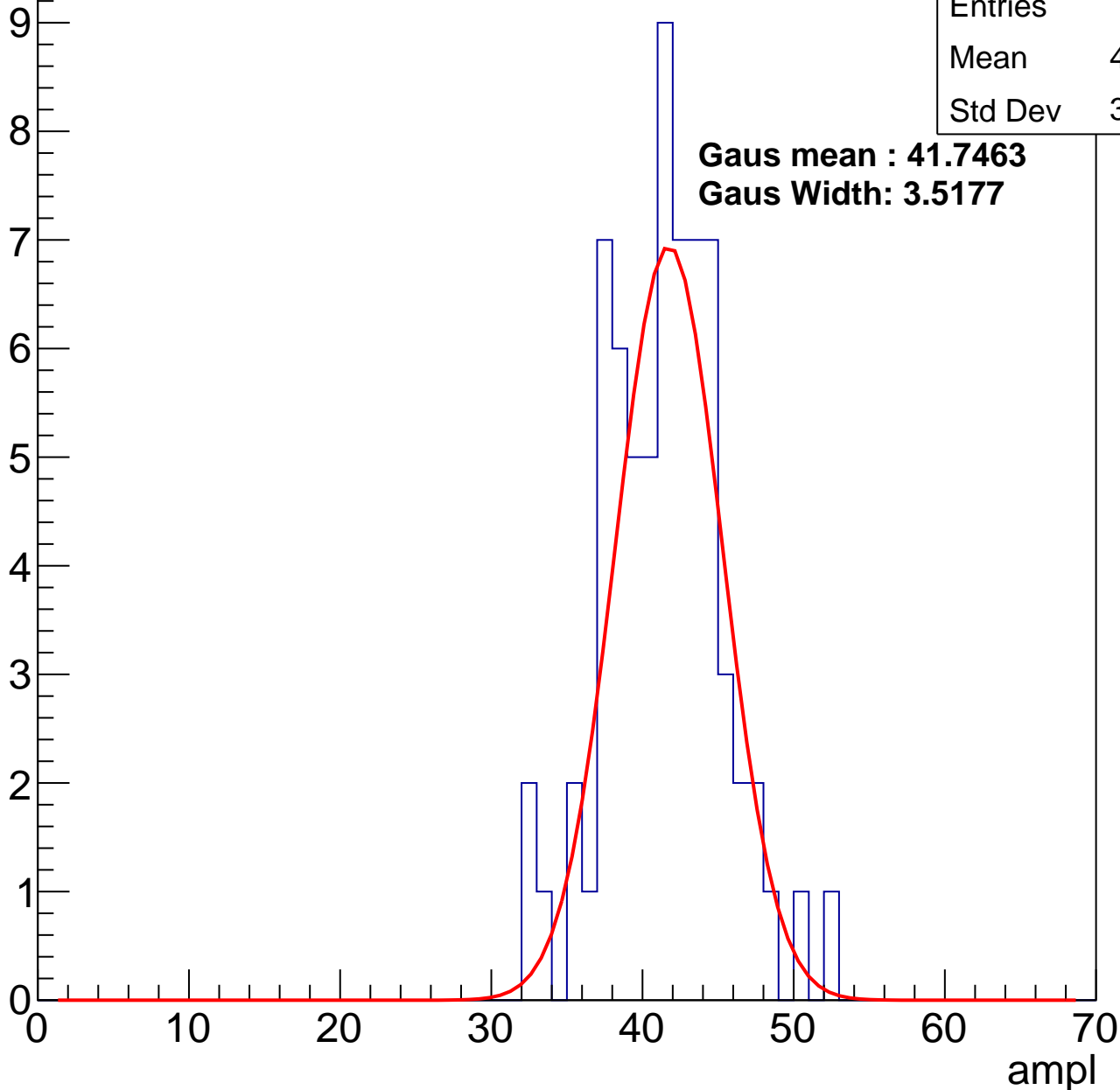
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	69
Mean	40.99
Std Dev	3.869

**Gaus mean : 41.7463**

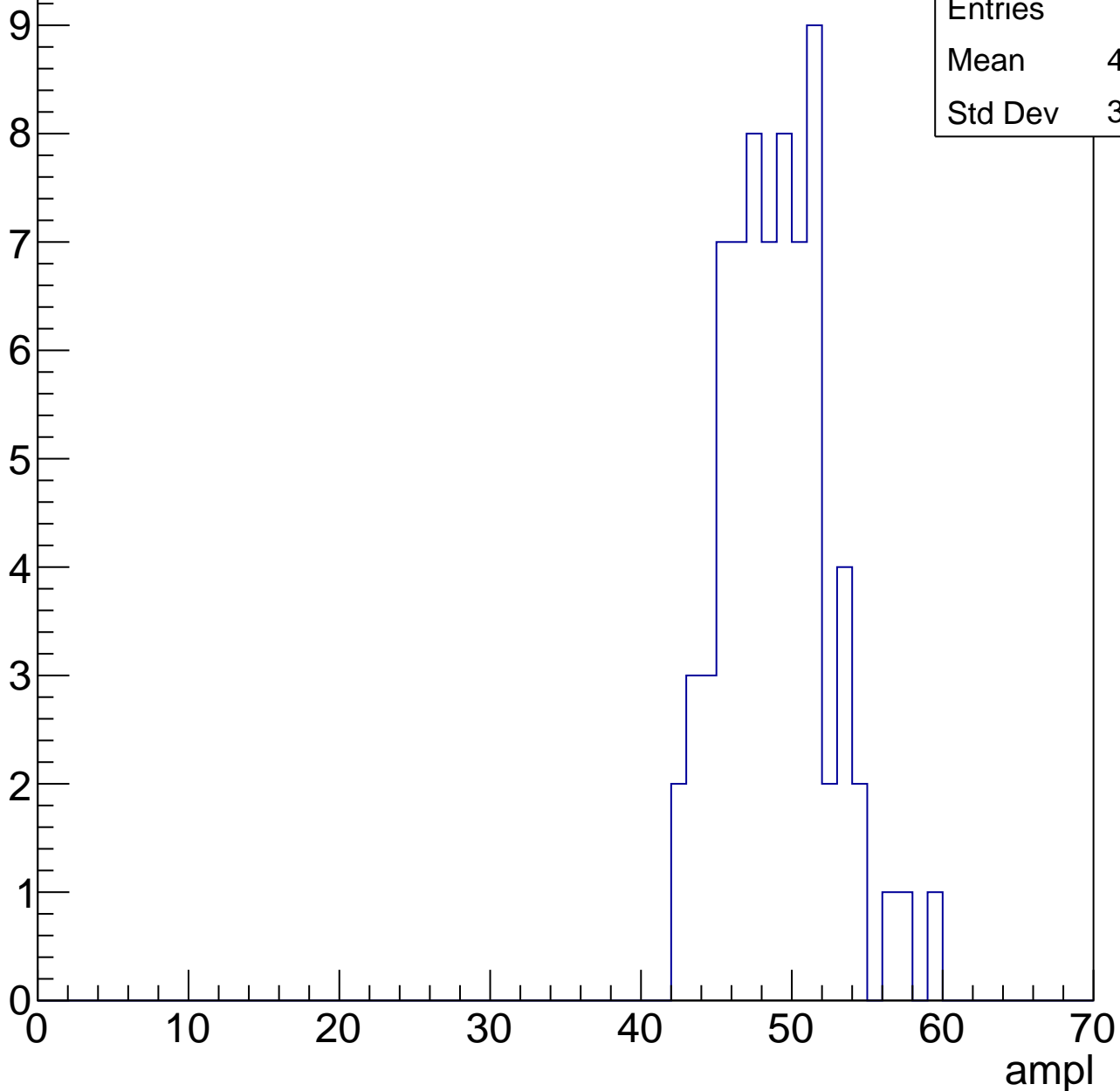
**Gaus Width: 3.5177**



# B1L003S, U18-ch61, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

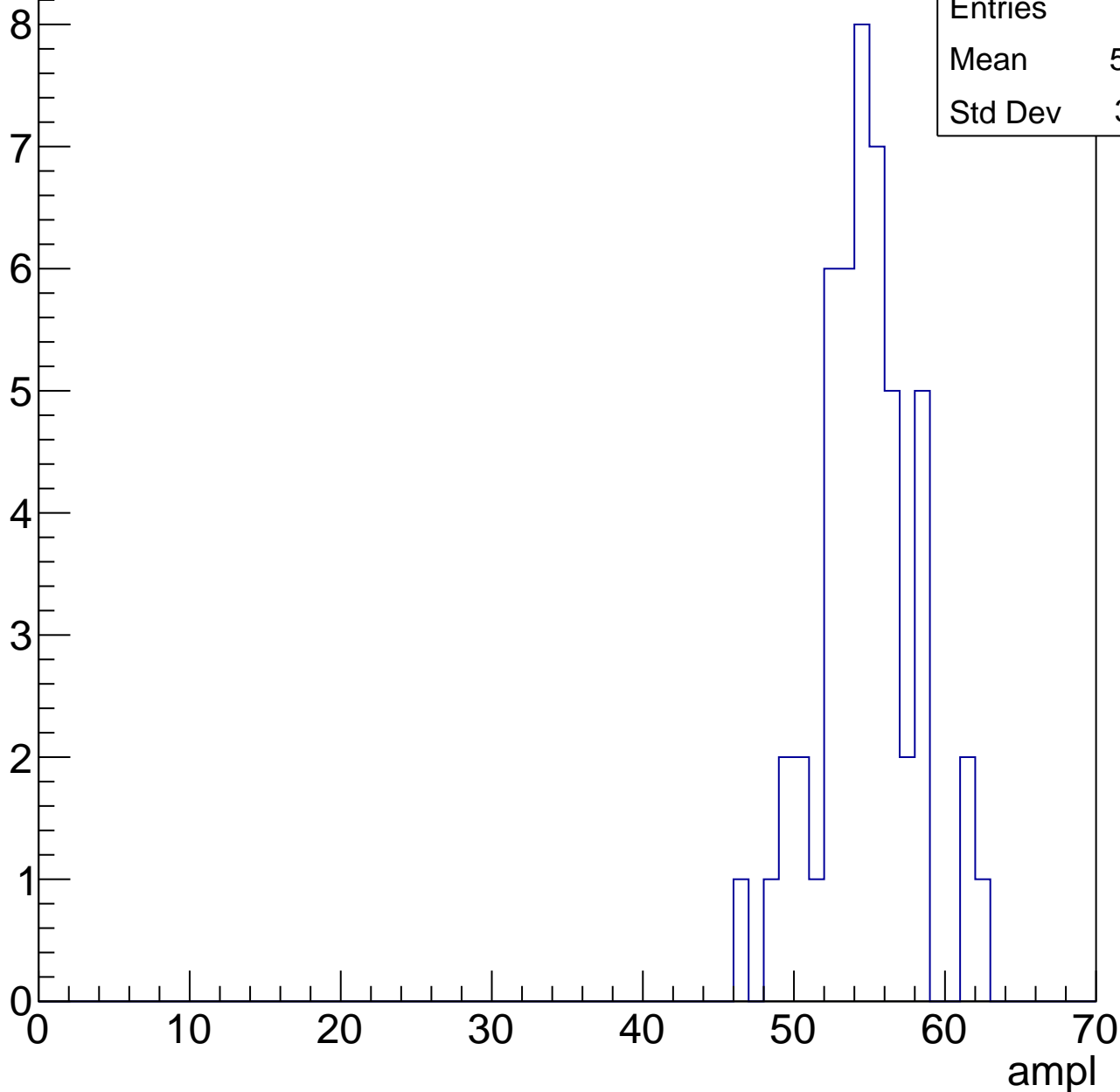


# B1L003S, U18-ch61, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	49
Mean	54.24
Std Dev	3.211

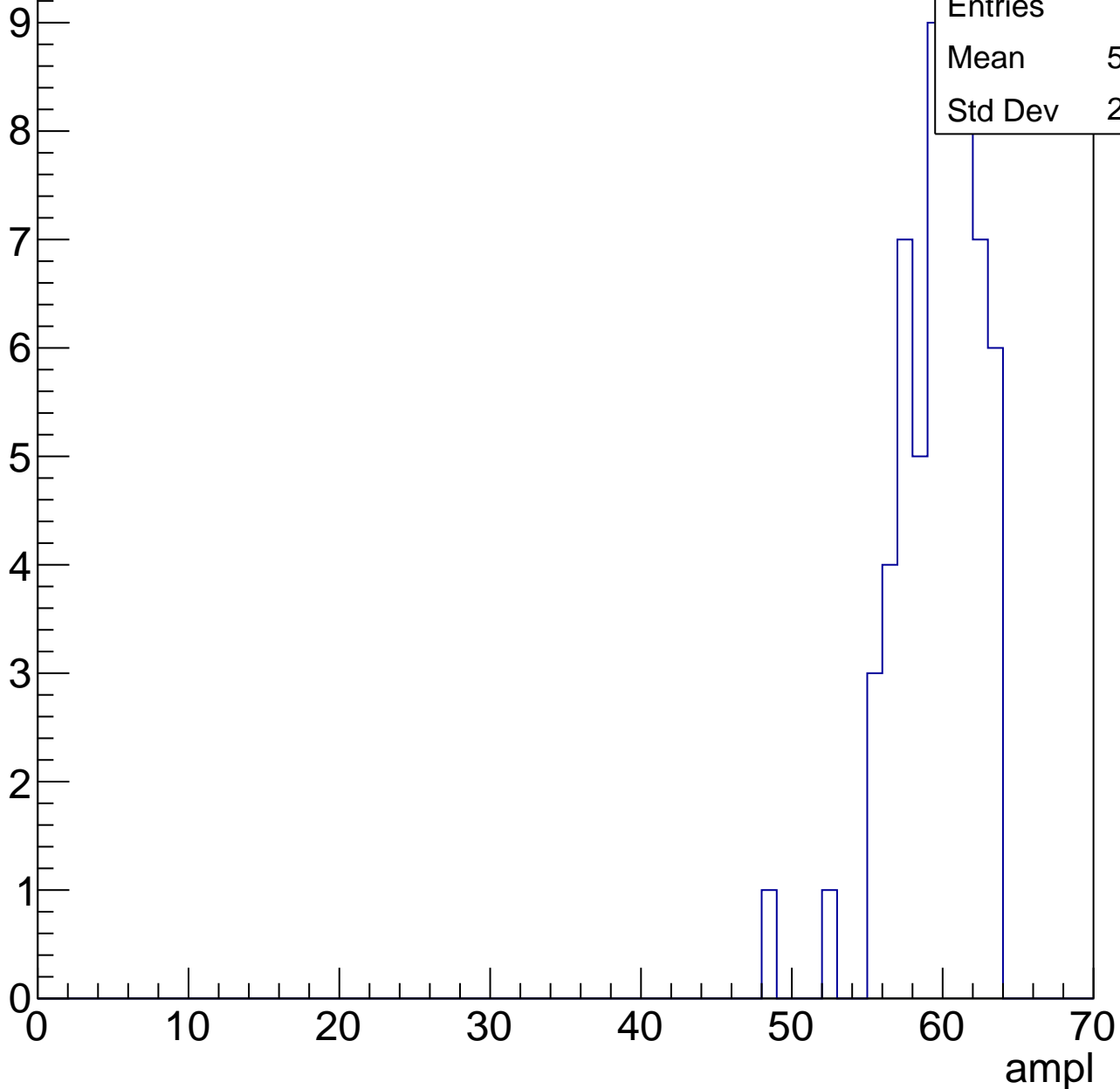


# B1L003S, U18-ch61, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

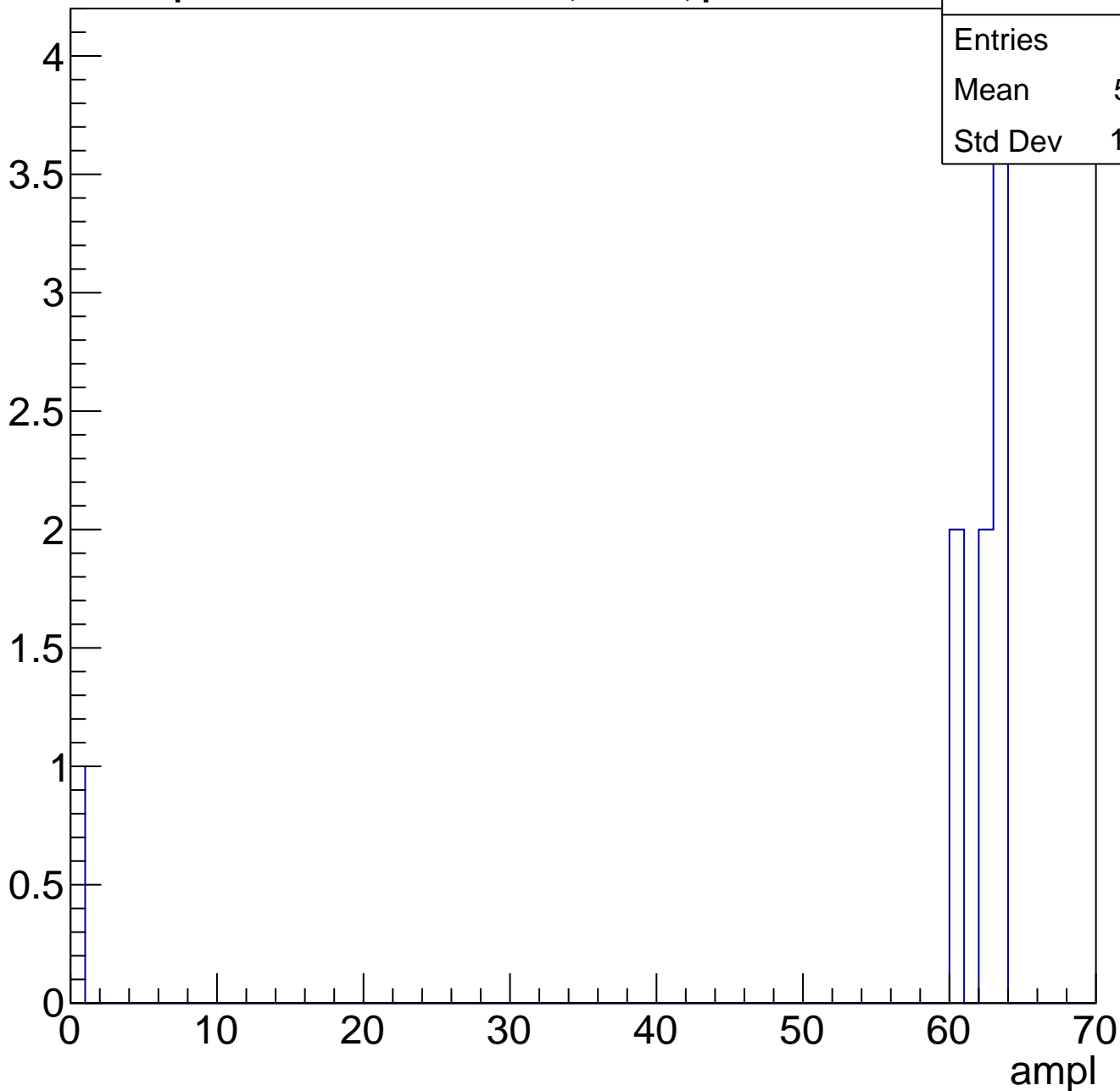
Entries	59
Mean	59.14
Std Dev	2.867



# B1L003S, U18-ch61, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	9
Mean	55.11
Std Dev	19.52



# B1L003S, U18-ch61, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch62, adc0

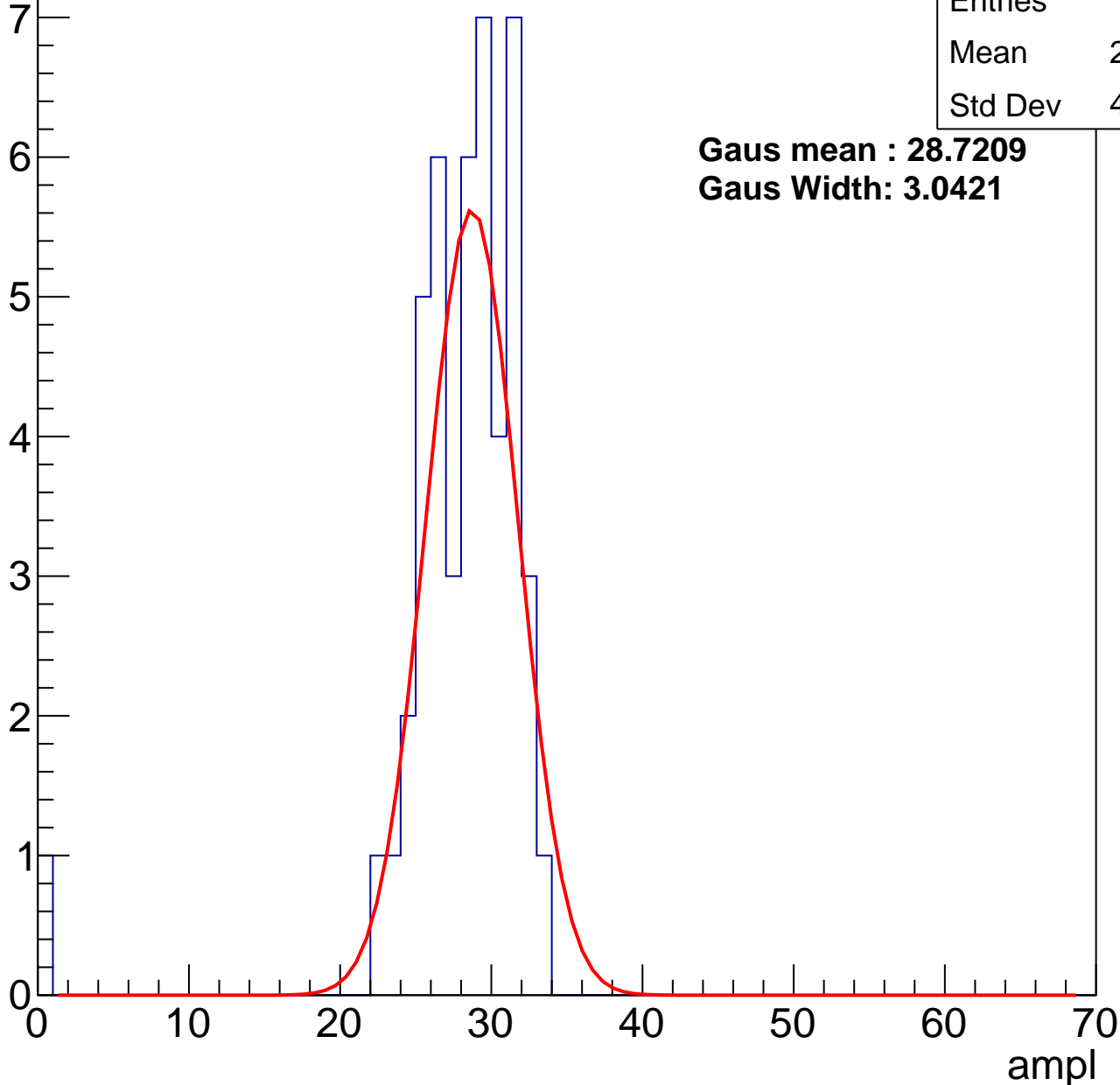
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	47
Mean	27.49
Std Dev	4.828

**Gaus mean : 28.7209**

**Gaus Width: 3.0421**



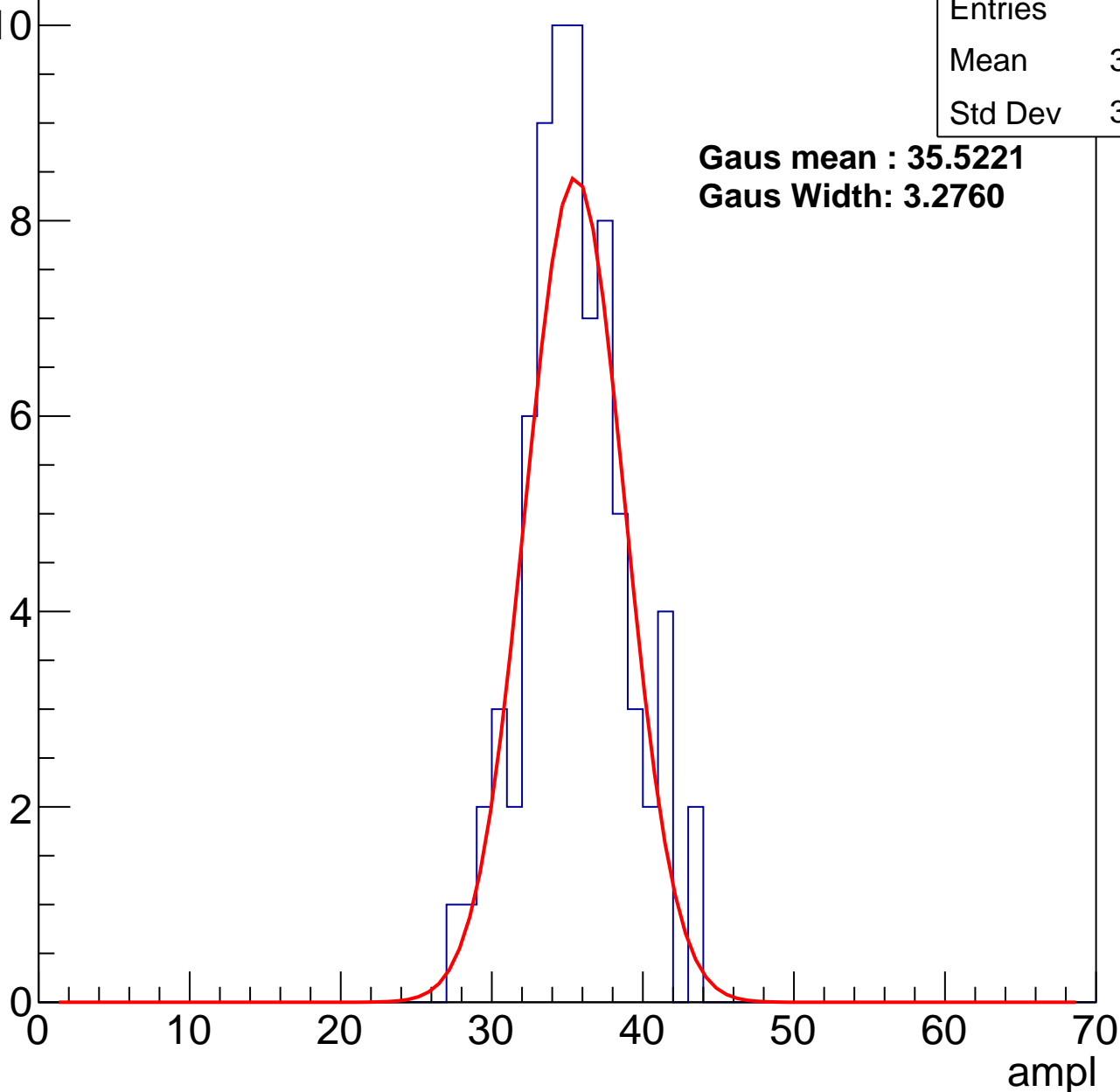
# B1L003S, U18-ch62, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	75
Mean	35.05
Std Dev	3.358

**Gaus mean : 35.5221**  
**Gaus Width: 3.2760**



# B1L003S, U18-ch62, adc2

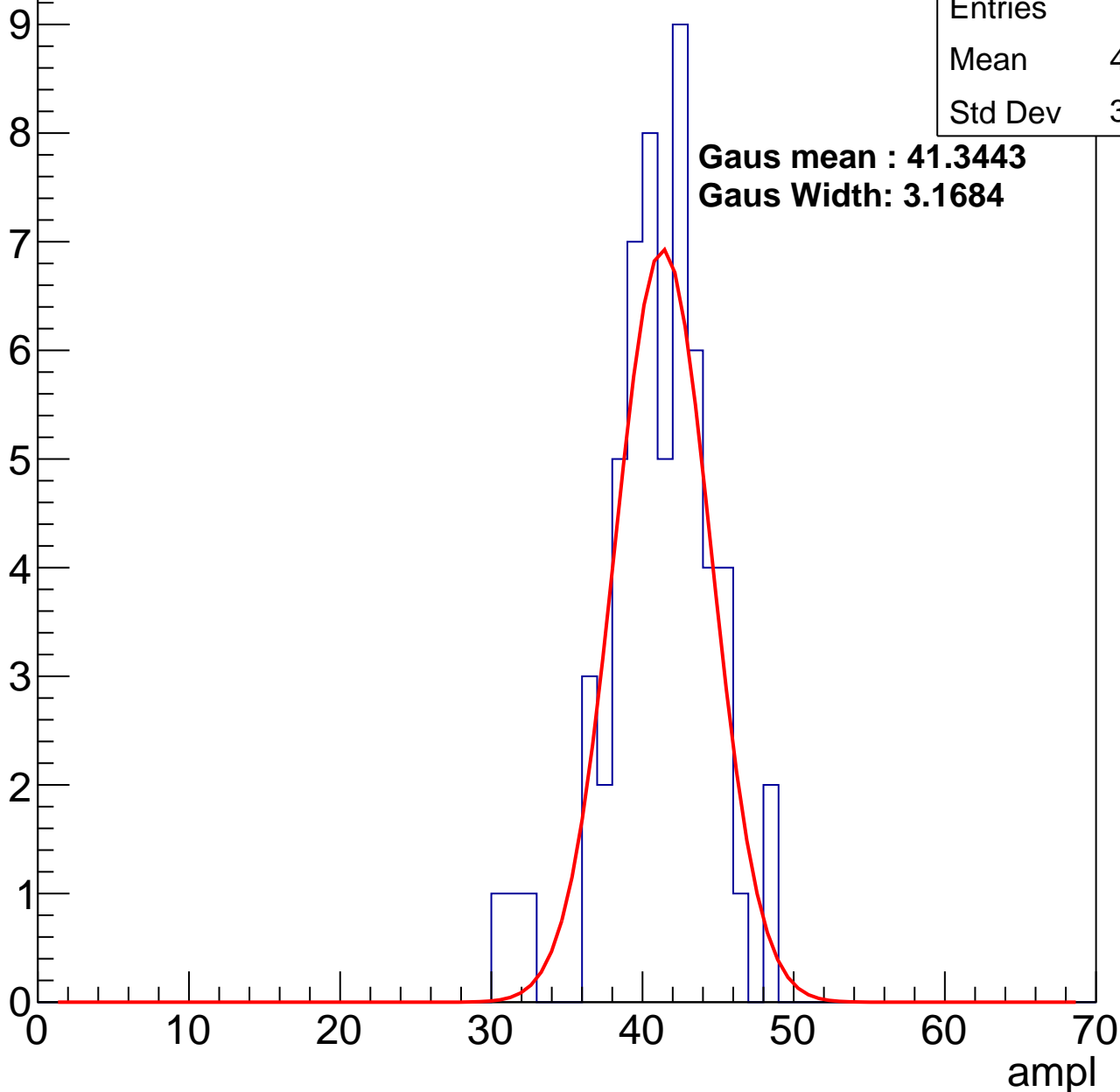
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	59
Mean	40.63
Std Dev	3.536

**Gaus mean : 41.3443**

**Gaus Width: 3.1684**

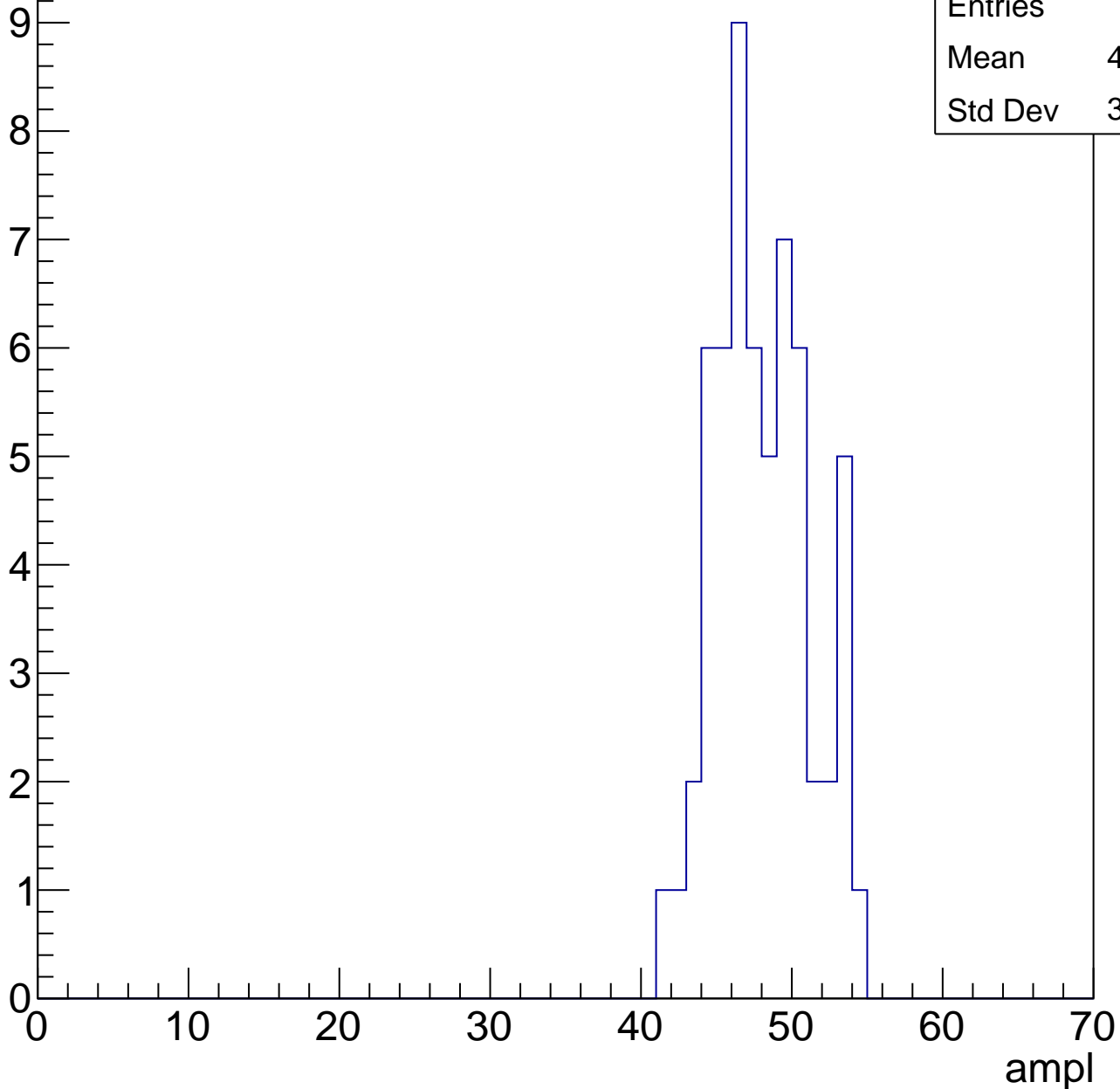


# B1L003S, U18-ch62, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	59
Mean	47.58
Std Dev	3.076

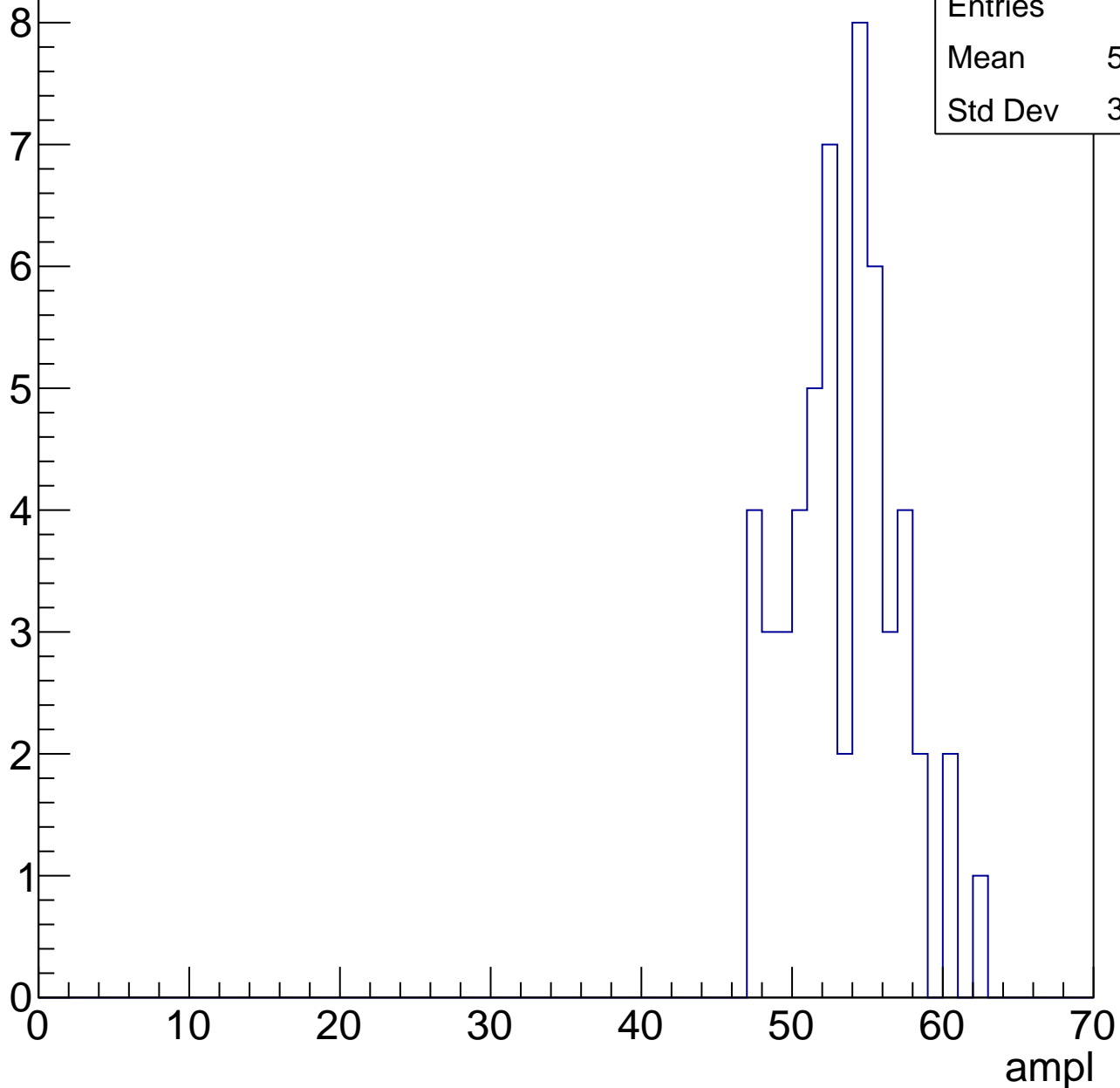


# B1L003S, U18-ch62, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	54
Mean	52.96
Std Dev	3.554

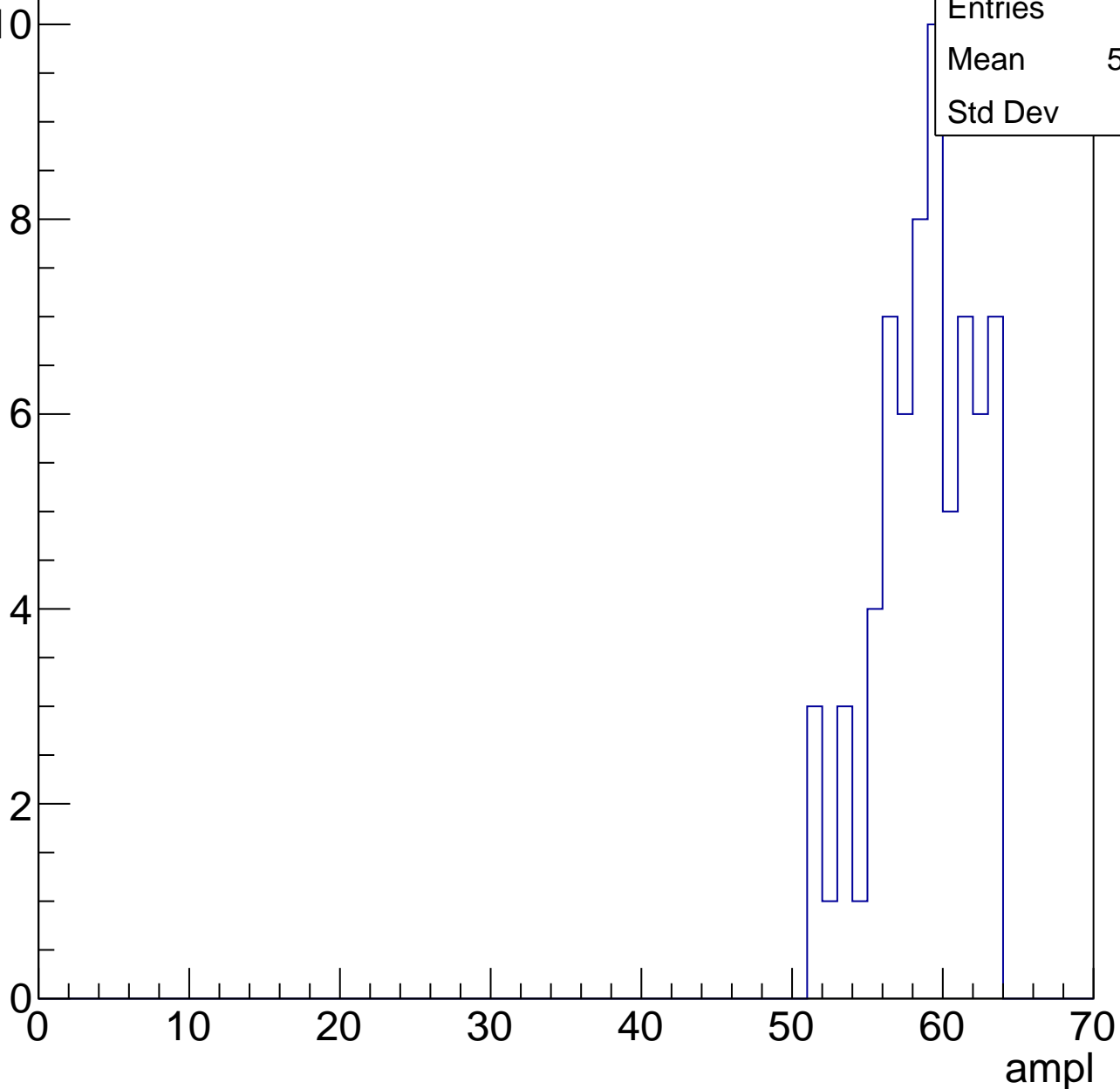


# B1L003S, U18-ch62, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	68
Mean	58.32
Std Dev	3.21



# B1L003S, U18-ch62, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

3

2.5

2

1.5

1

0.5

0

0

10

20

30

40

50

60

70

ampl

Entries	13
Mean	56.77
Std Dev	16.42



# B1L003S, U18-ch62, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L003S, U18-ch63, adc0

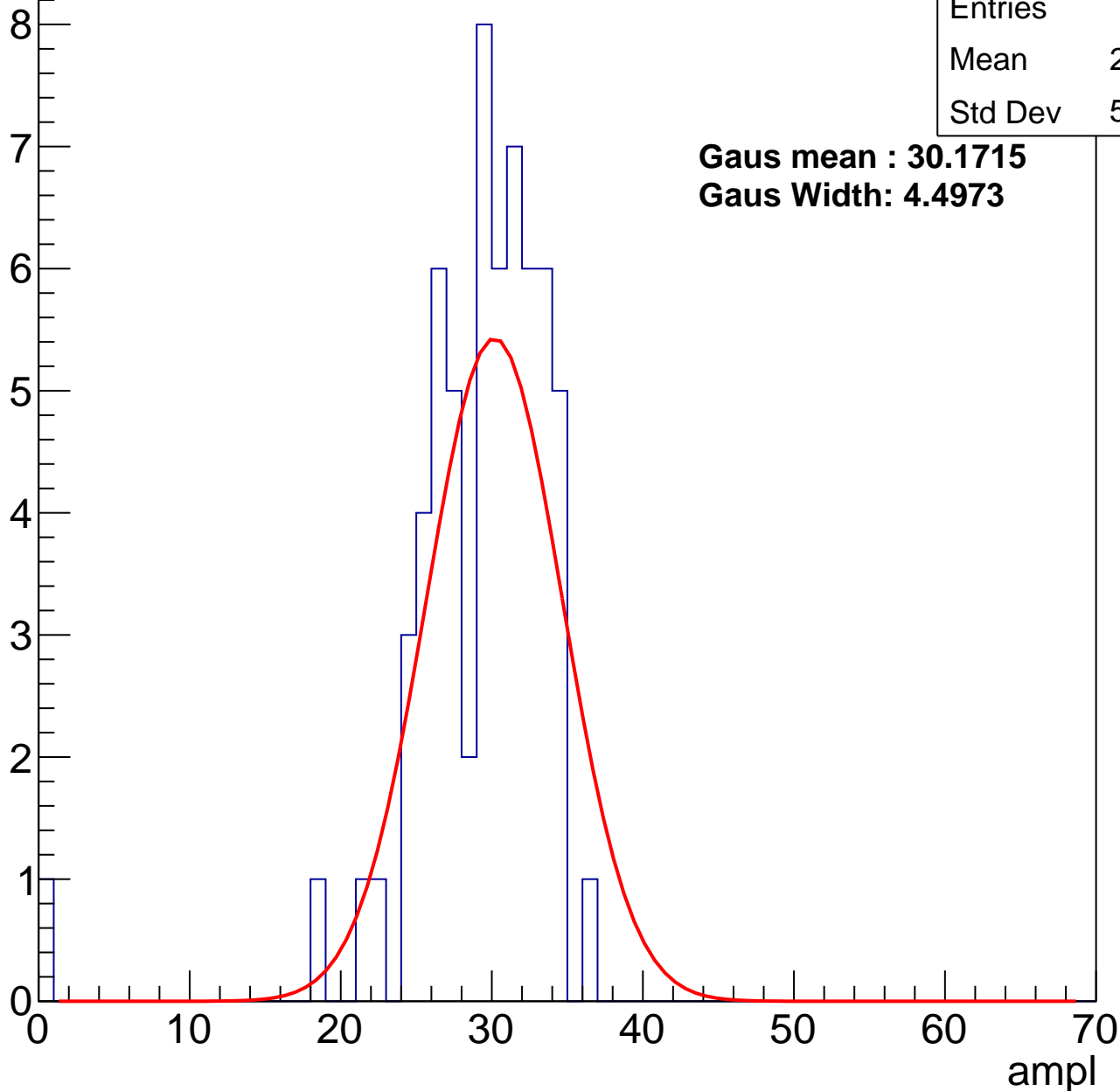
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	63
Mean	28.65
Std Dev	5.103

**Gaus mean : 30.1715**

**Gaus Width: 4.4973**



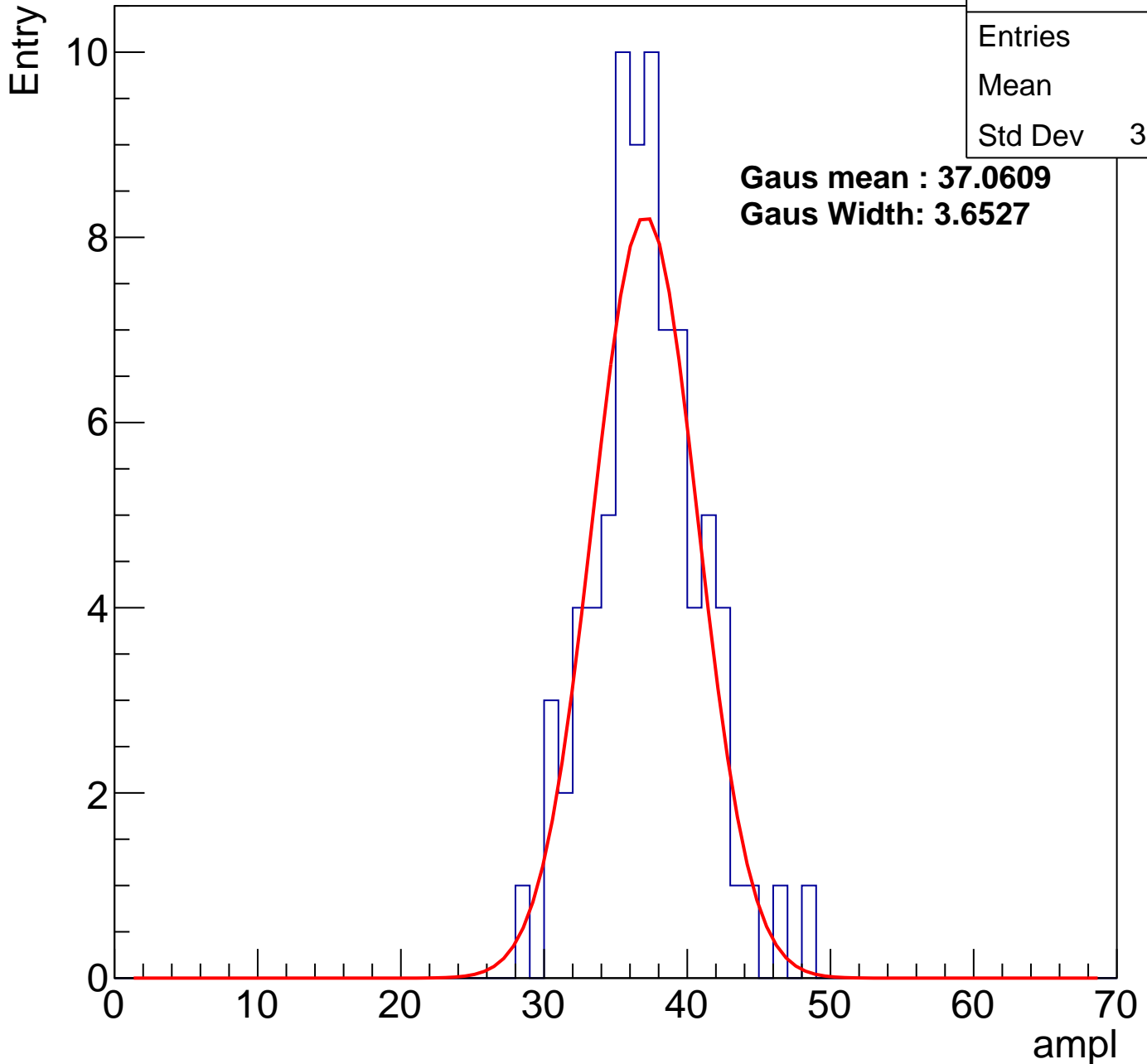
# B1L003S, U18-ch63, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	79
Mean	36.8
Std Dev	3.719

**Gaus mean : 37.0609**

**Gaus Width: 3.6527**



# B1L003S, U18-ch63, adc2

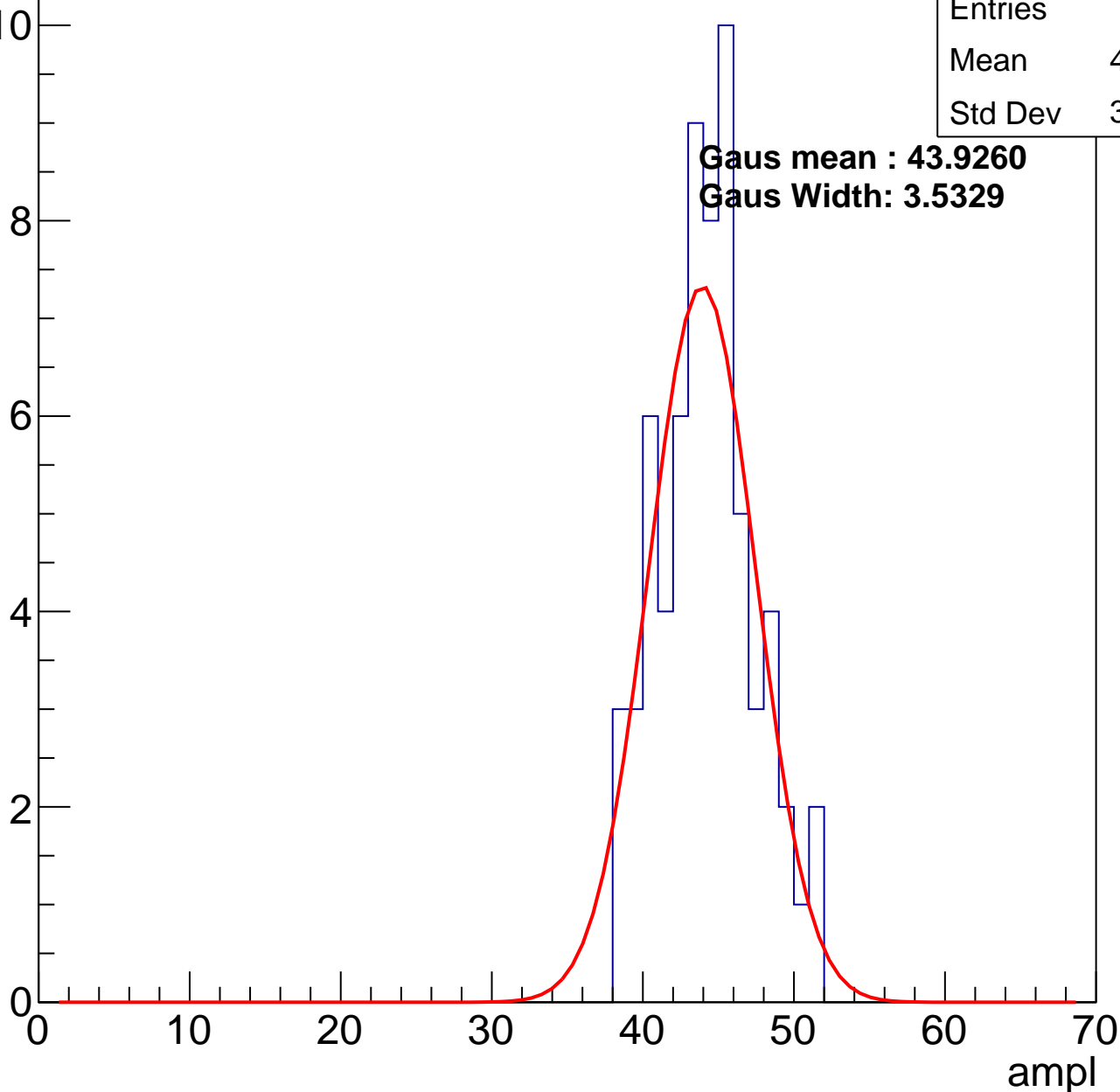
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	66
Mean	43.77
Std Dev	3.137

**Gaus mean : 43.9260**

**Gaus Width: 3.5329**

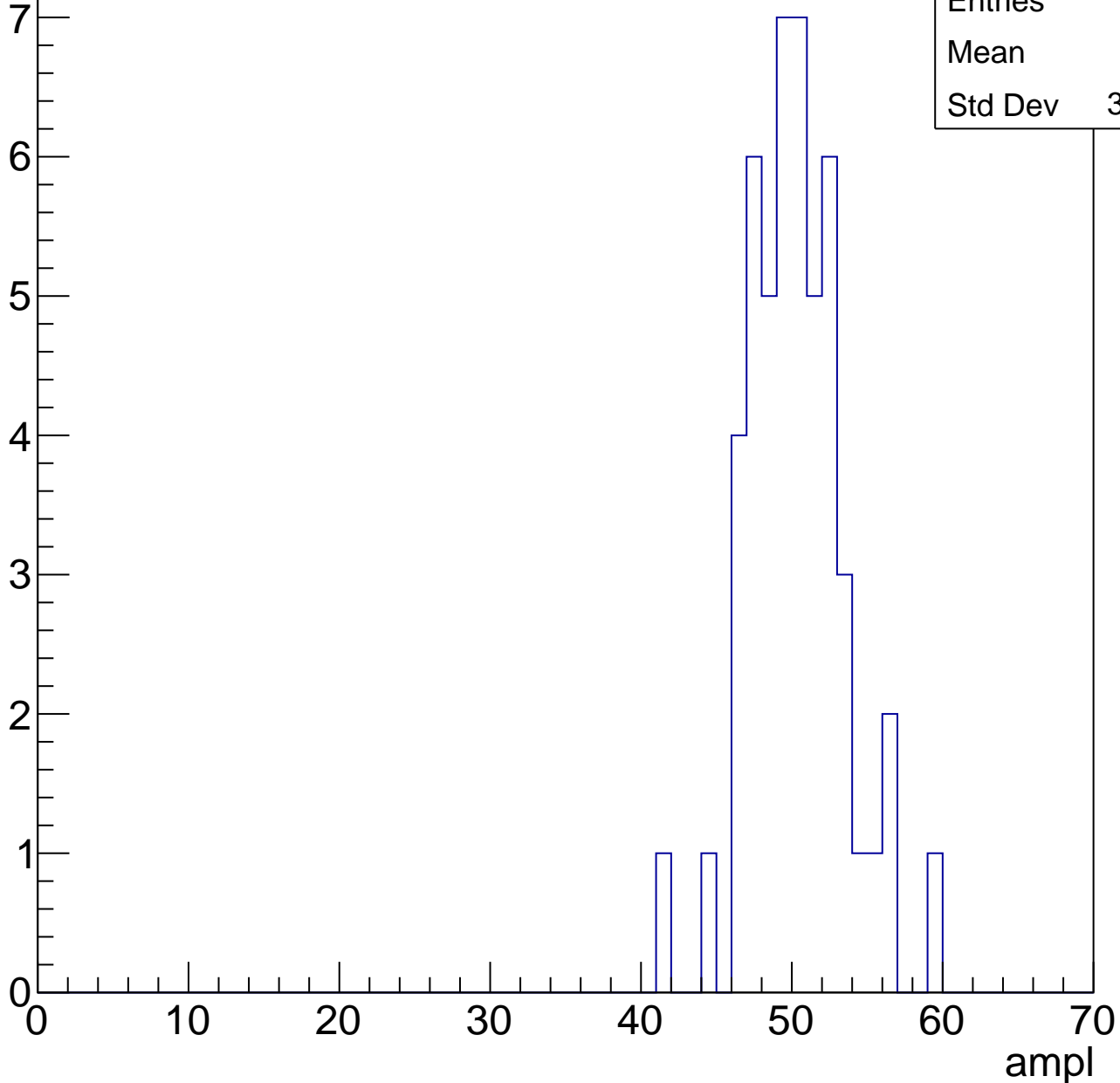


# B1L003S, U18-ch63, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	50
Mean	49.8
Std Dev	3.194

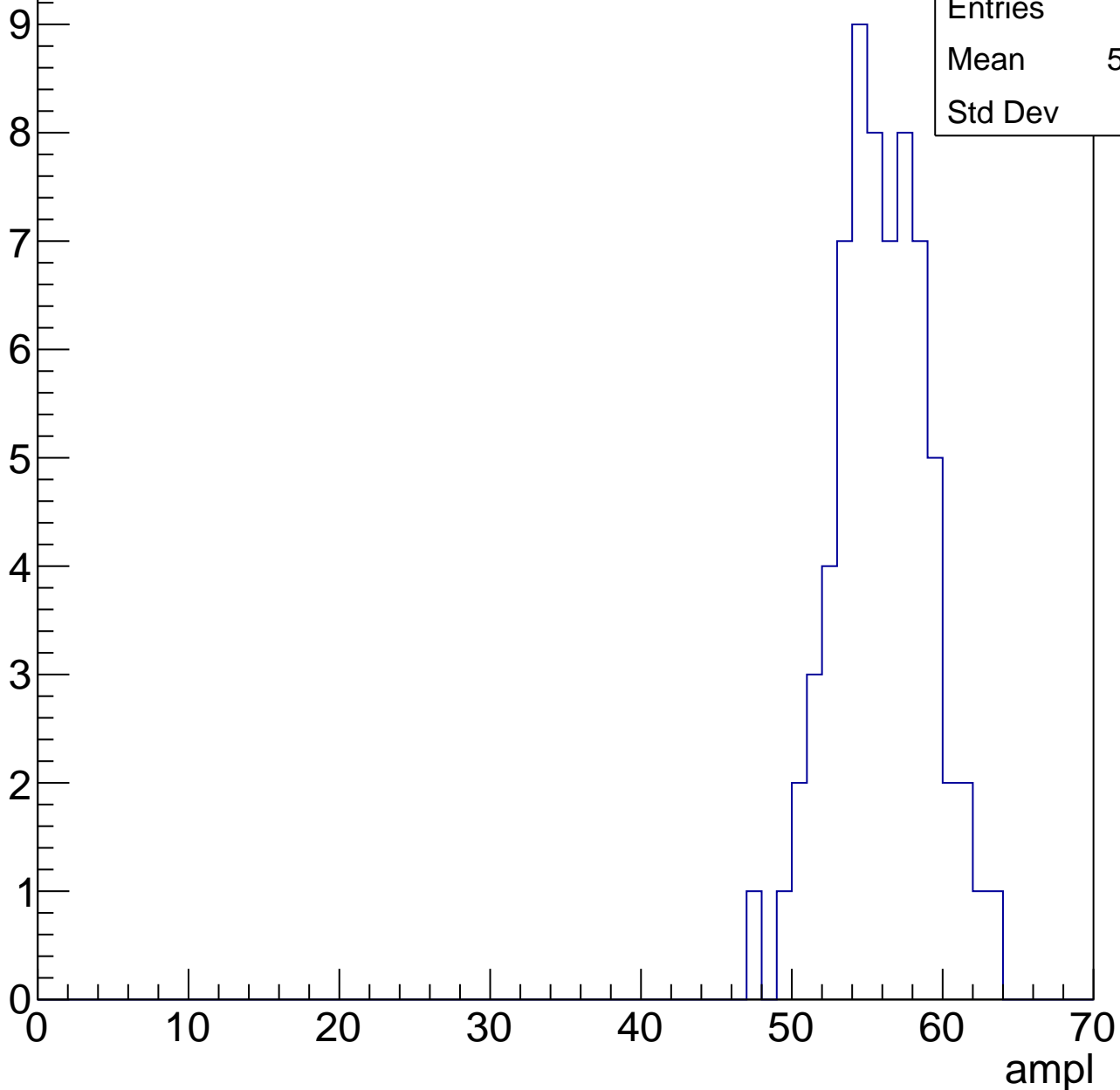


# B1L003S, U18-ch63, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

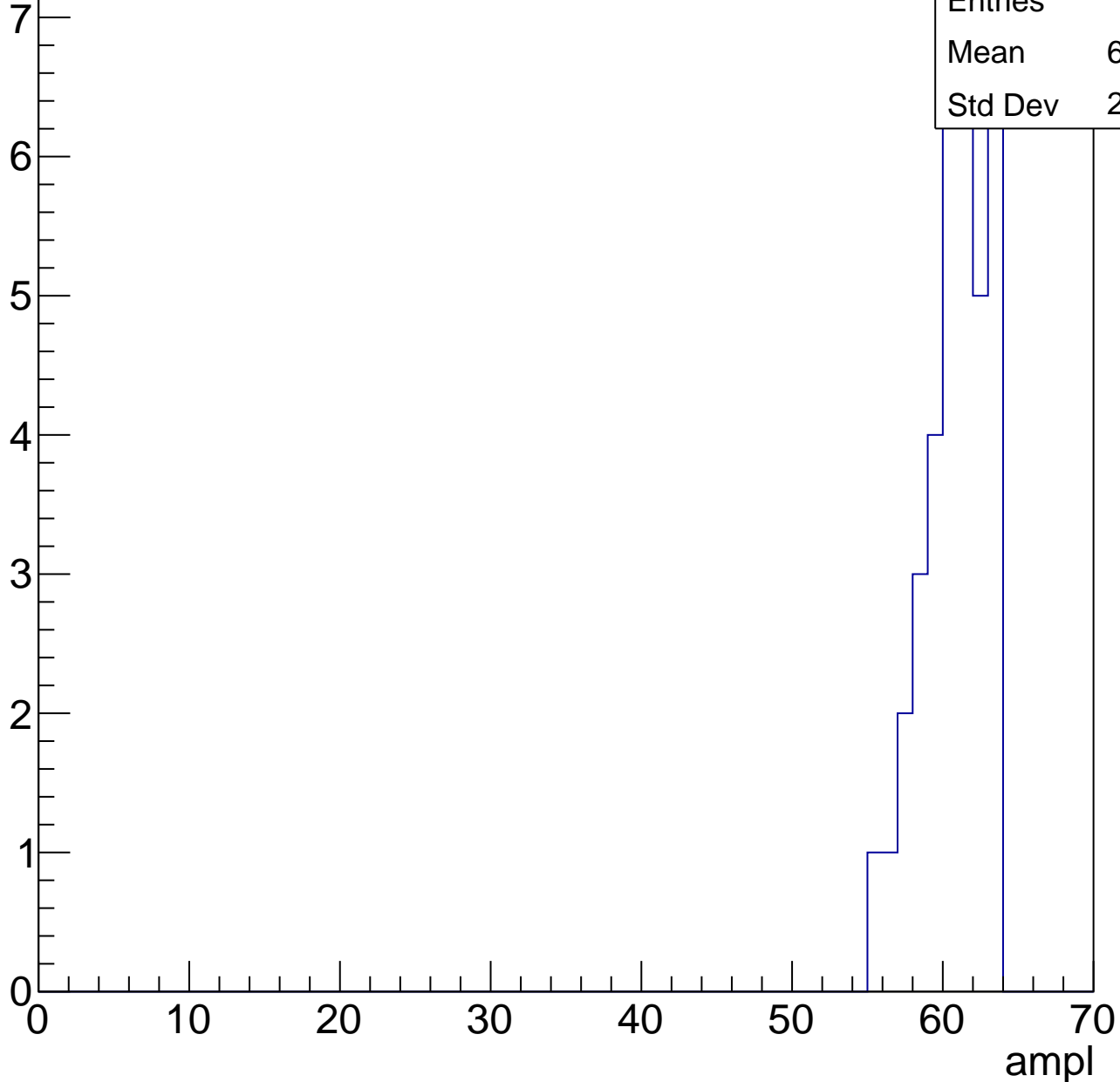
Entries	68
Mean	55.44
Std Dev	3.15



# B1L003S, U18-ch63, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

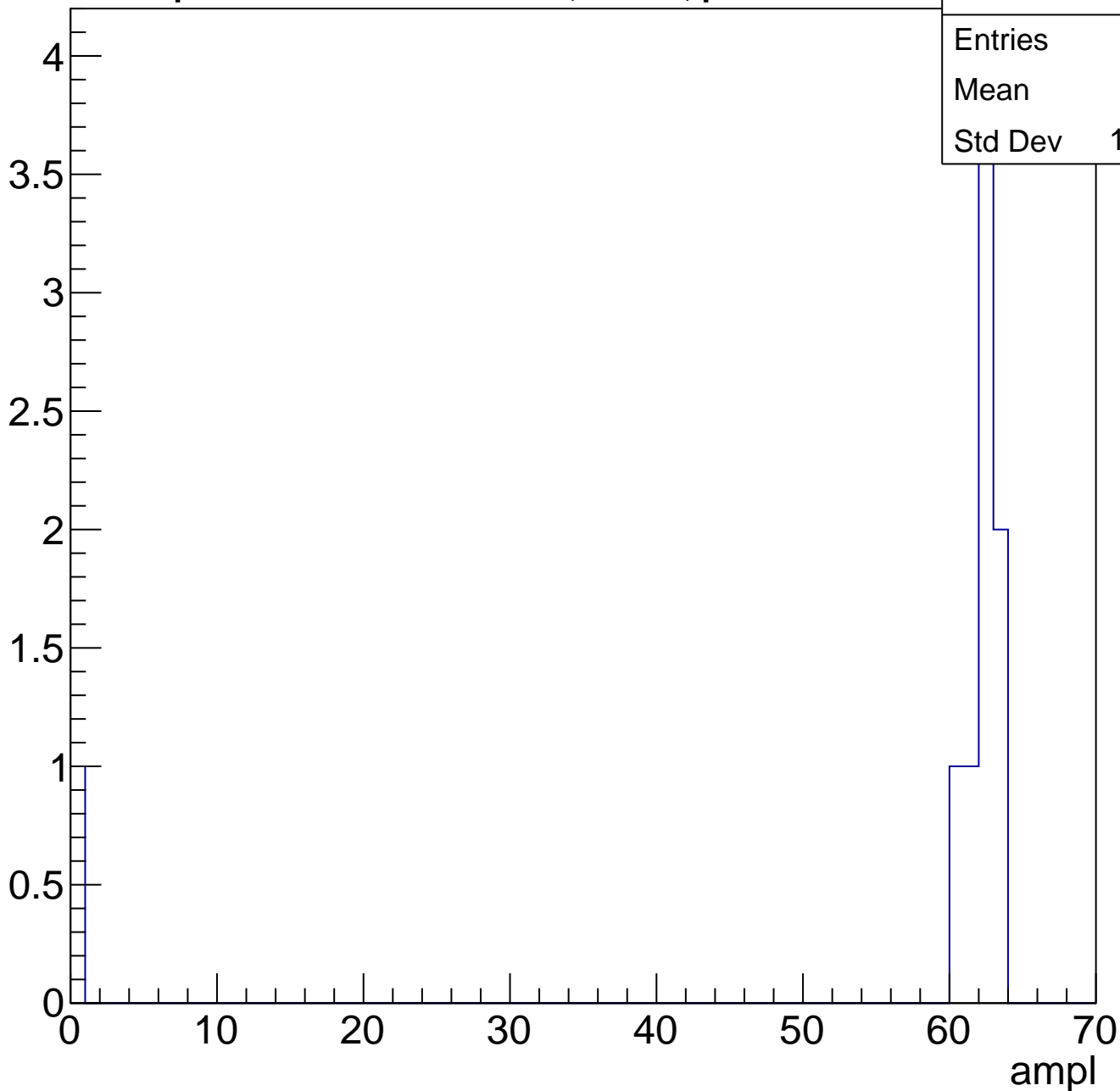


Entries	37
Mean	60.35
Std Dev	2.082

# B1L003S, U18-ch63, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

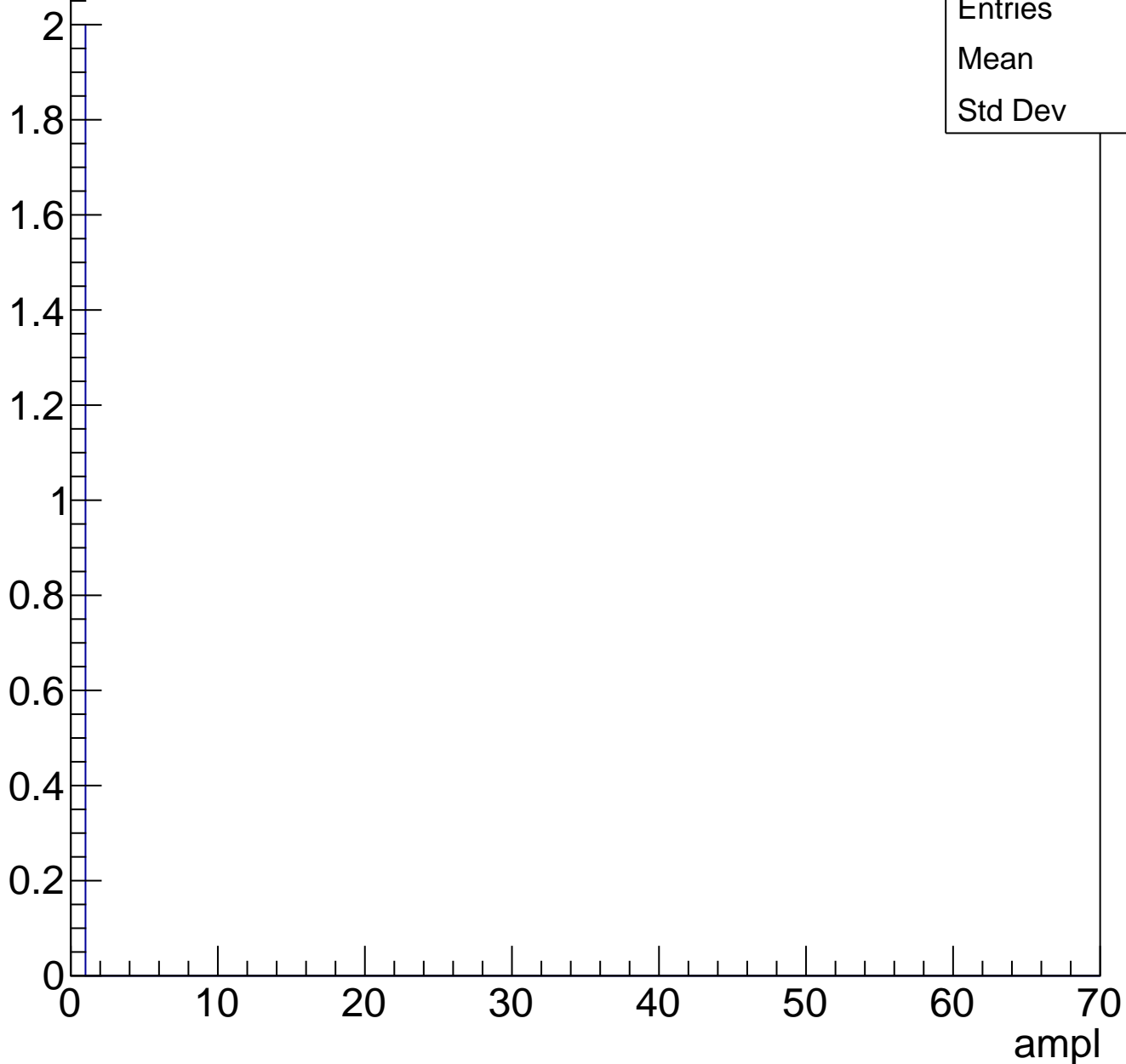




# B1L003S, U18-ch63, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U18-ch64, adc0

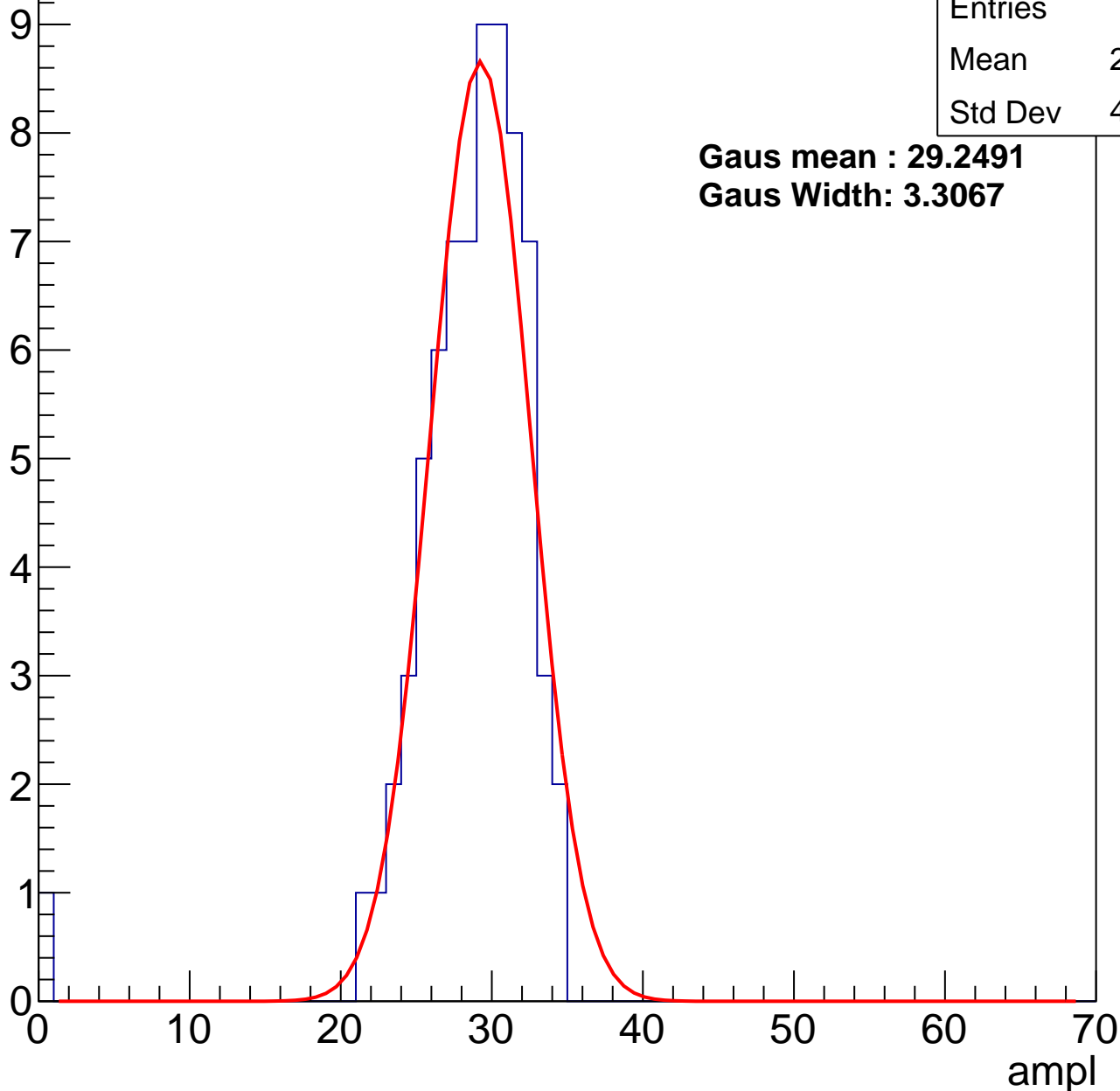
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	71
Mean	28.13
Std Dev	4.469

**Gaus mean : 29.2491**

**Gaus Width: 3.3067**



# B1L003S, U18-ch64, adc1

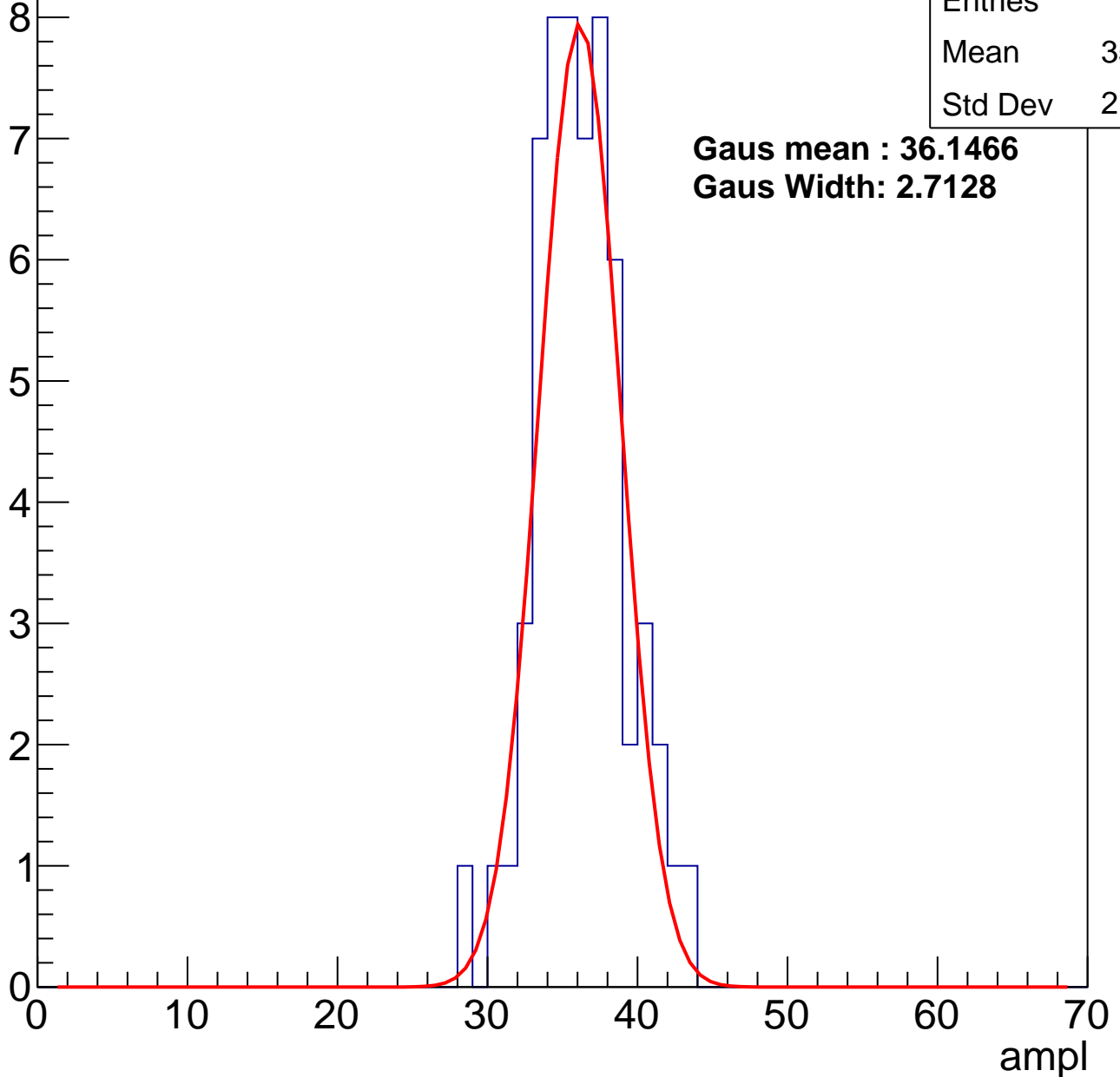
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	59
Mean	35.75
Std Dev	2.926

**Gaus mean : 36.1466**

**Gaus Width: 2.7128**



# B1L003S, U18-ch64, adc2

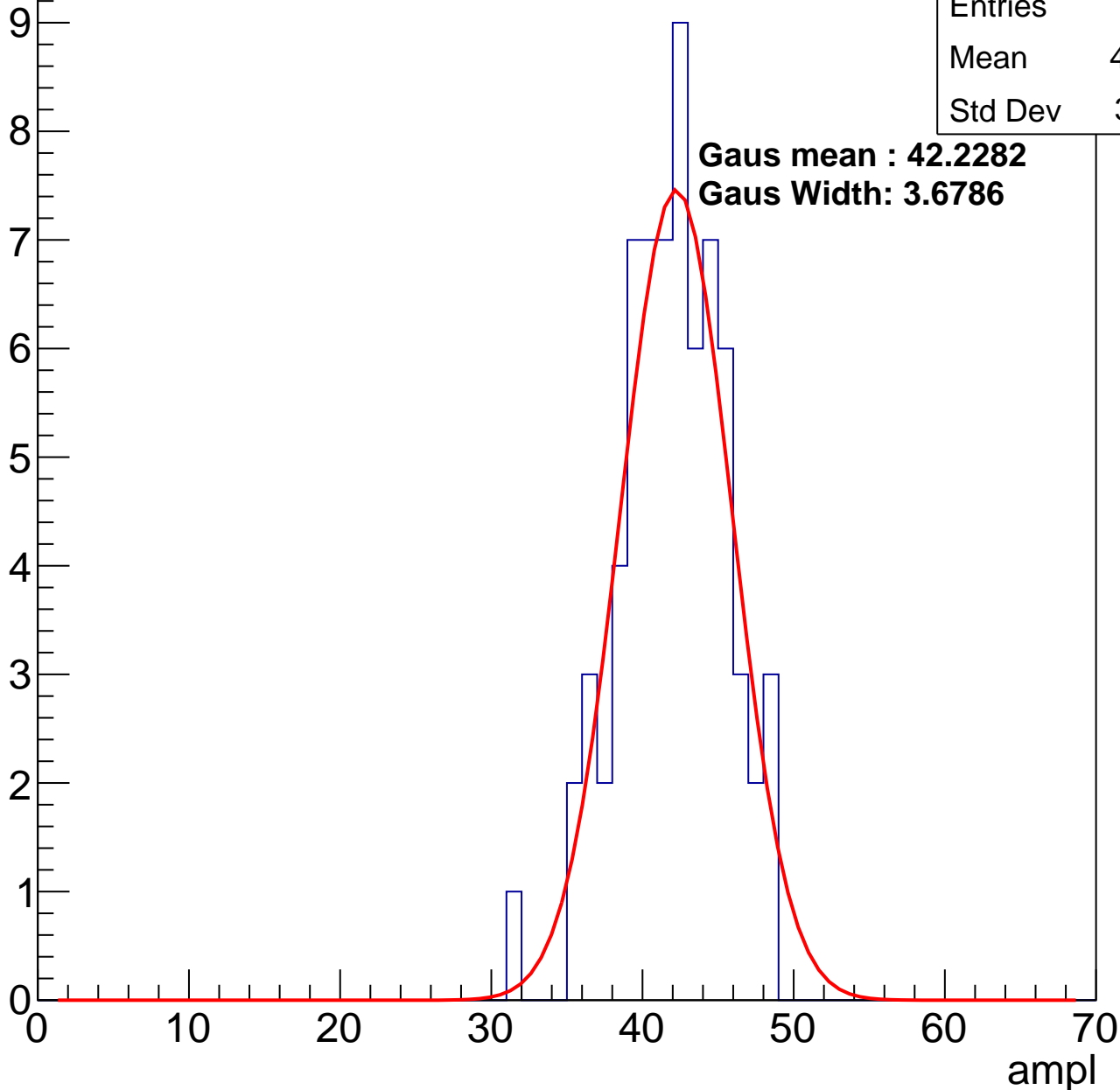
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	69
Mean	41.52
Std Dev	3.441

**Gaus mean : 42.2282**

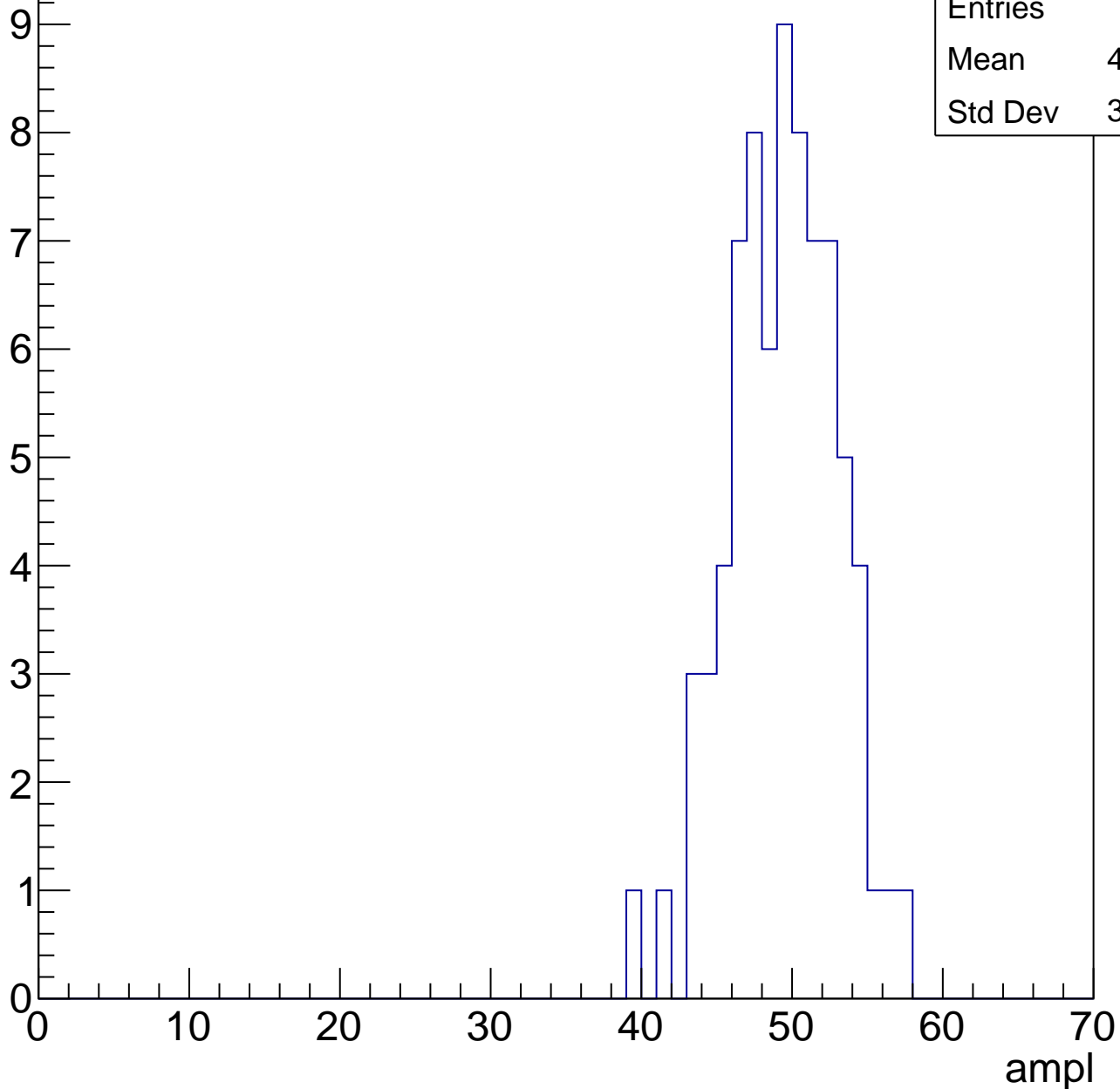
**Gaus Width: 3.6786**



# B1L003S, U18-ch64, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

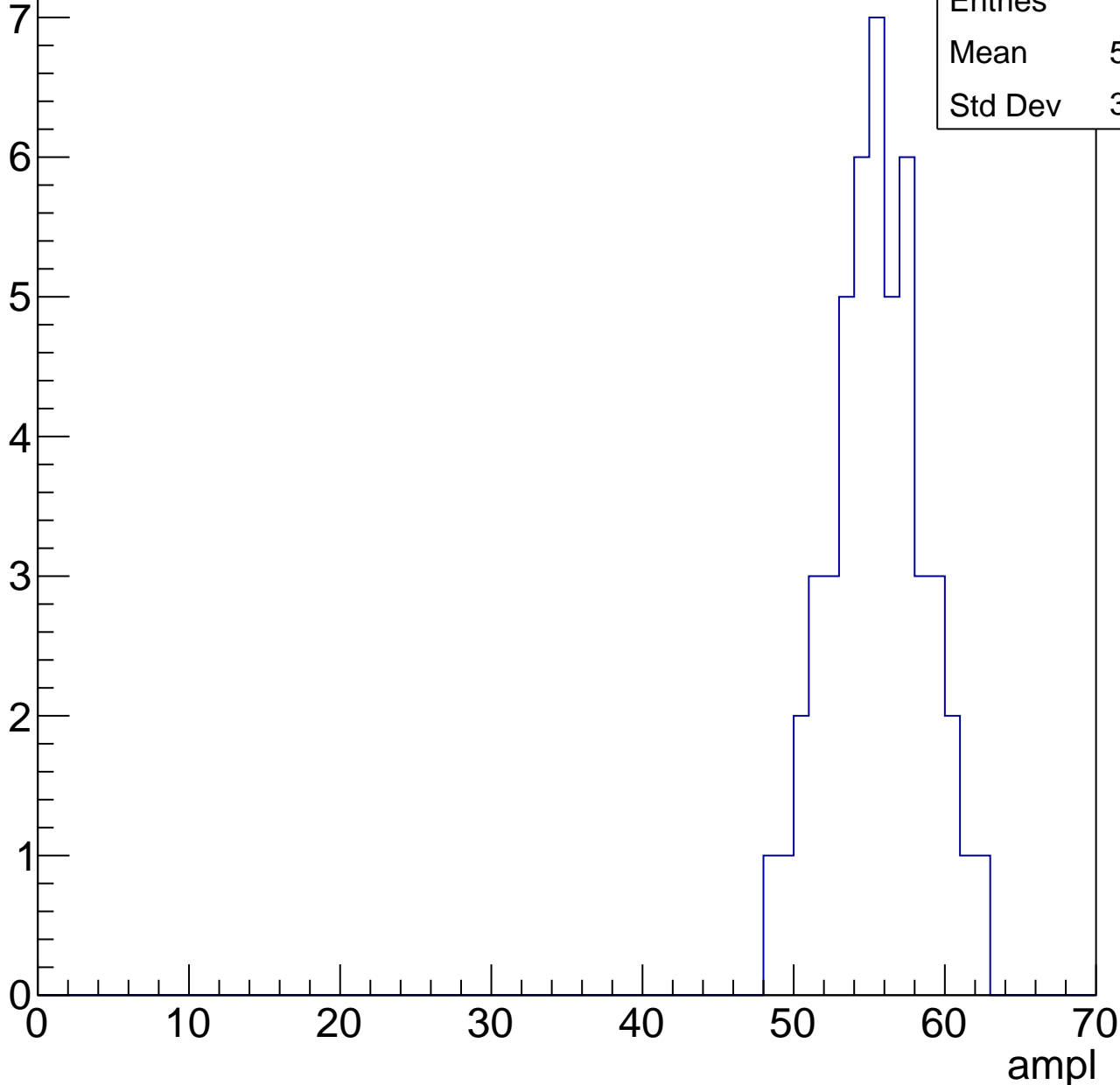


# B1L003S, U18-ch64, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	49
Mean	55.02
Std Dev	3.113

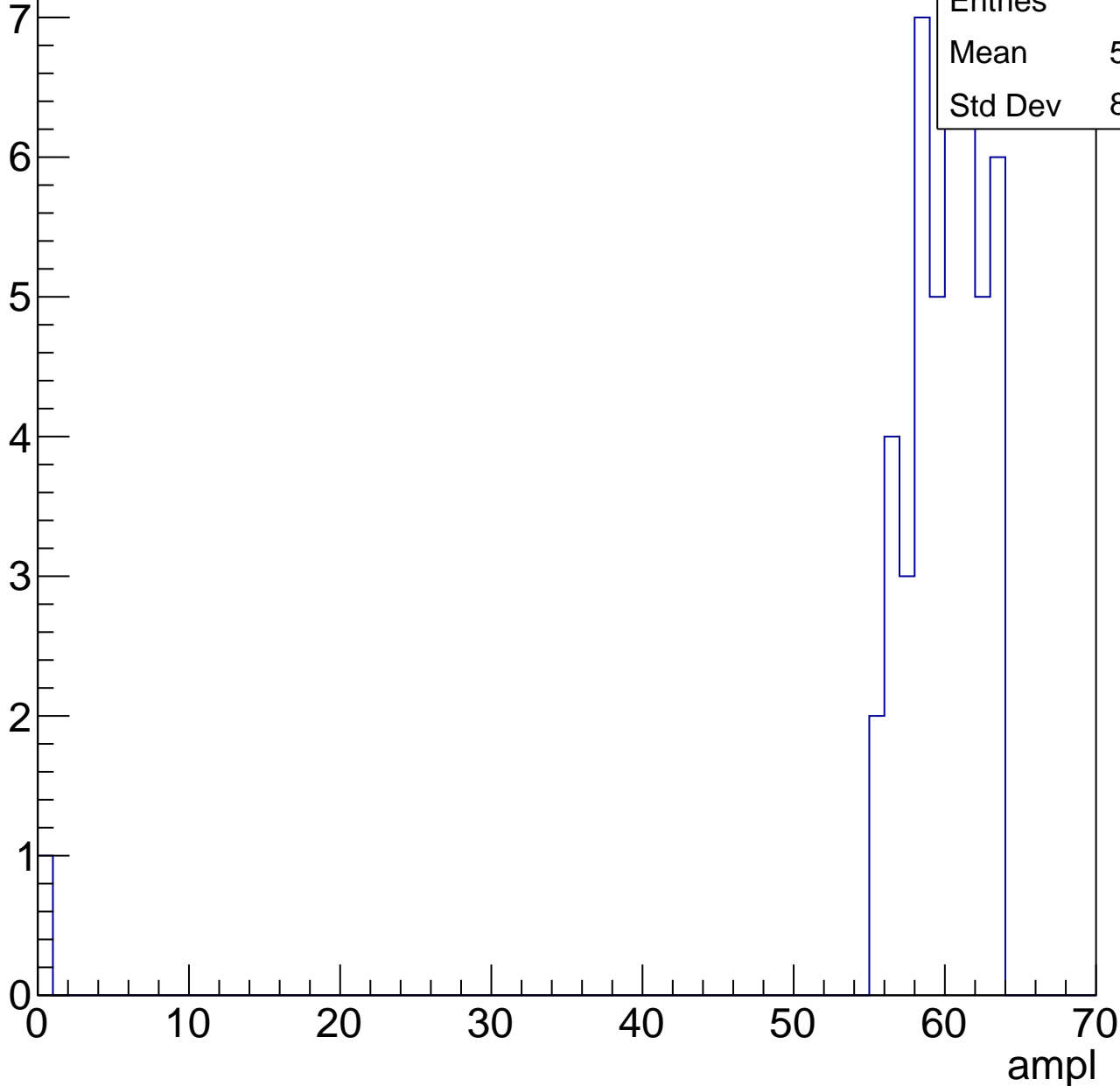


# B1L003S, U18-ch64, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

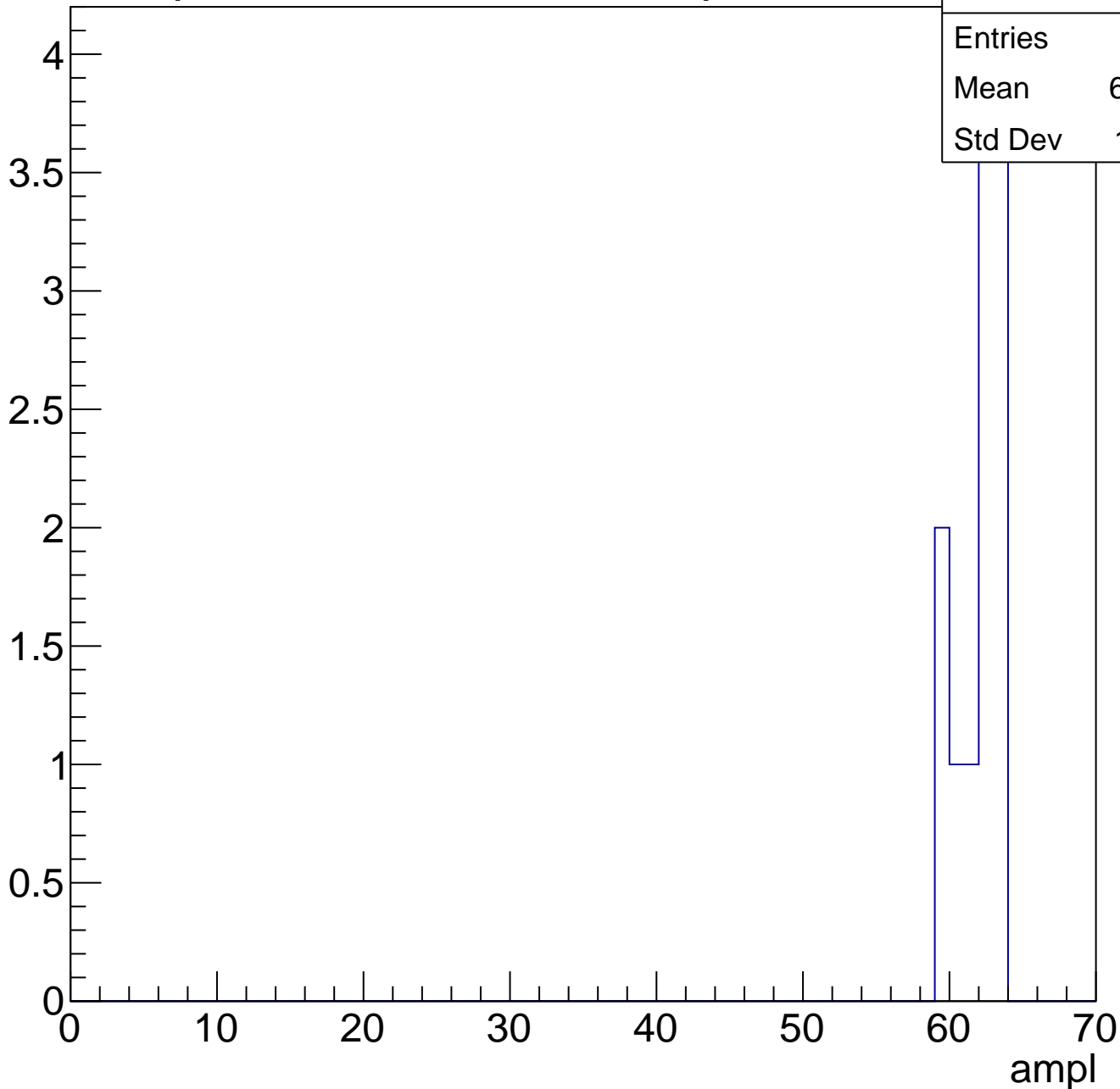
Entries	47
Mean	58.32
Std Dev	8.899



# B1L003S, U18-ch64, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

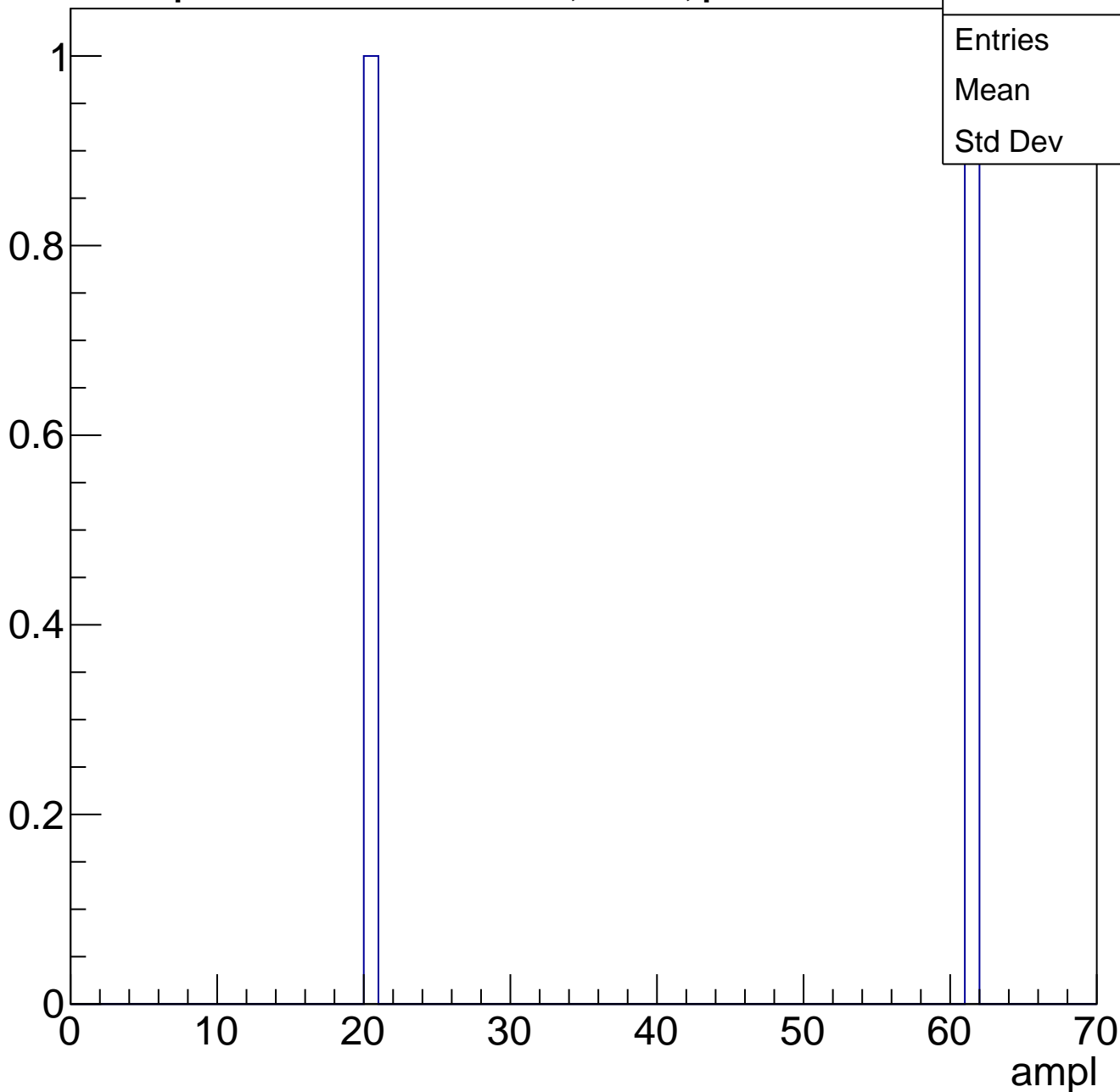




# B1L003S, U18-ch64, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	2
Mean	40.5
Std Dev	20.5

# B1L003S, U18-ch65, adc0

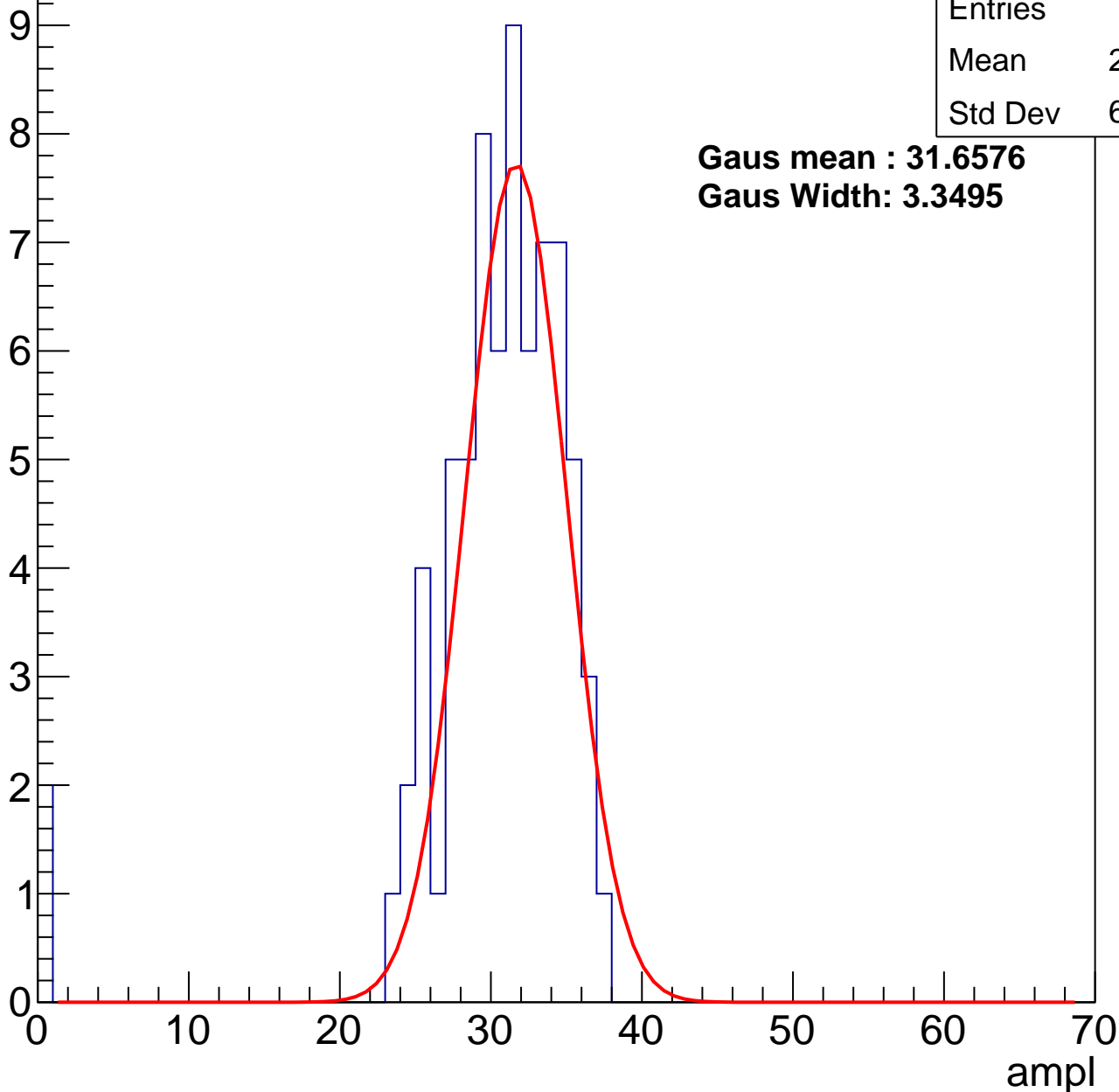
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	72
Mean	29.78
Std Dev	6.005

**Gaus mean : 31.6576**

**Gaus Width: 3.3495**



# B1L003S, U18-ch65, adc1

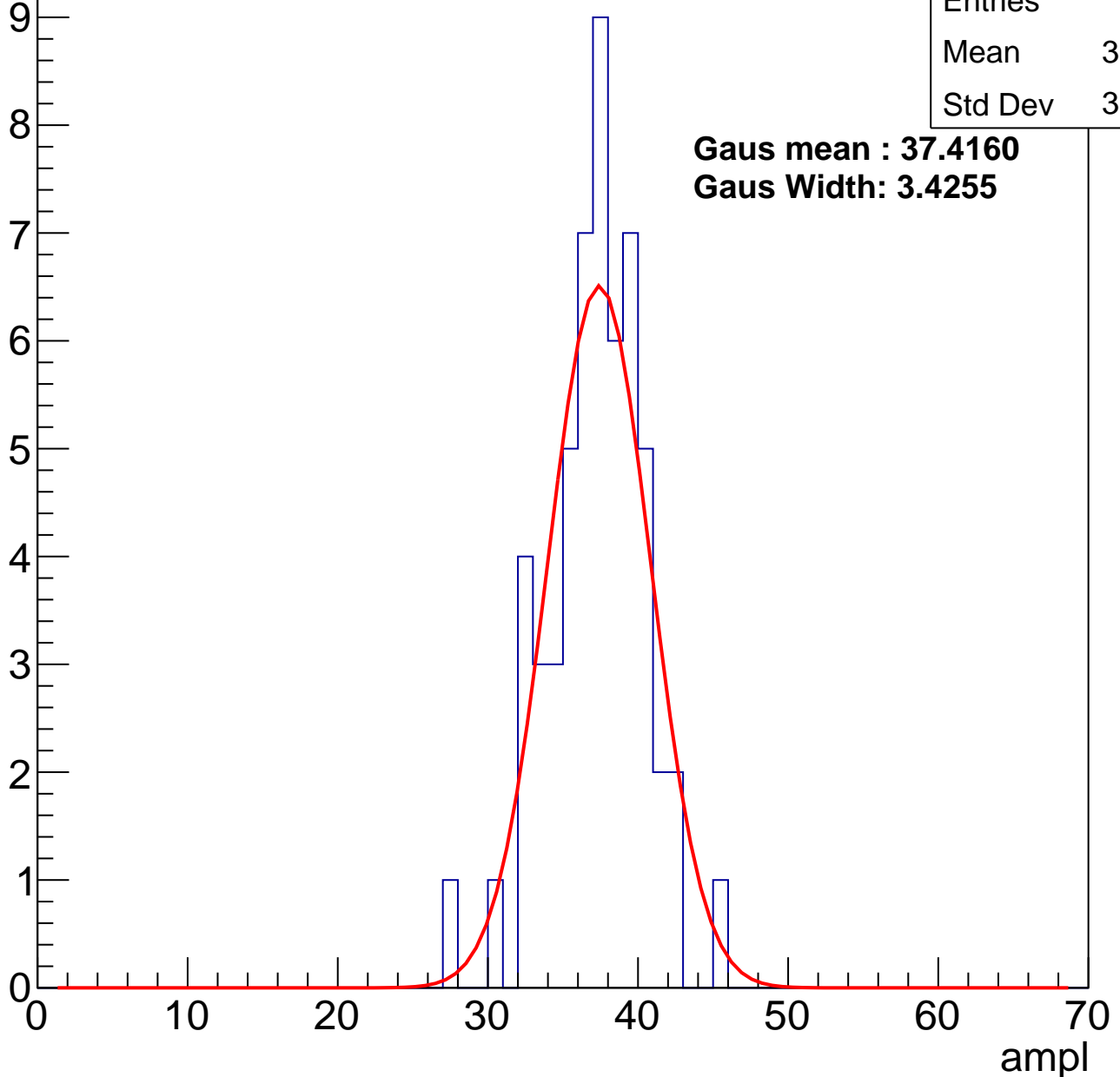
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	56
Mean	36.75
Std Dev	3.197

**Gaus mean : 37.4160**

**Gaus Width: 3.4255**



# B1L003S, U18-ch65, adc2

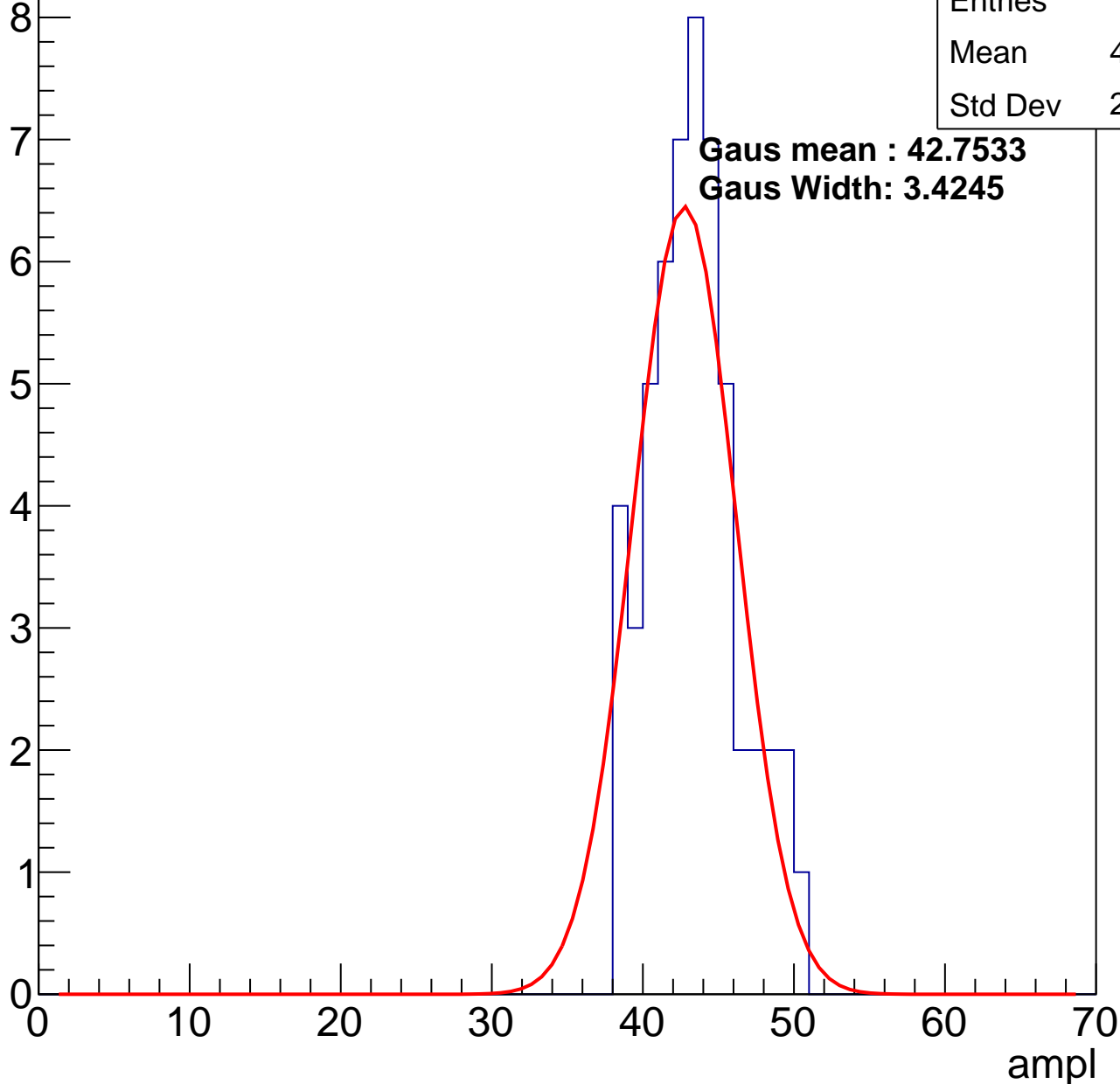
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	54
Mean	42.89
Std Dev	2.954

**Gaus mean : 42.7533**

**Gaus Width: 3.4245**

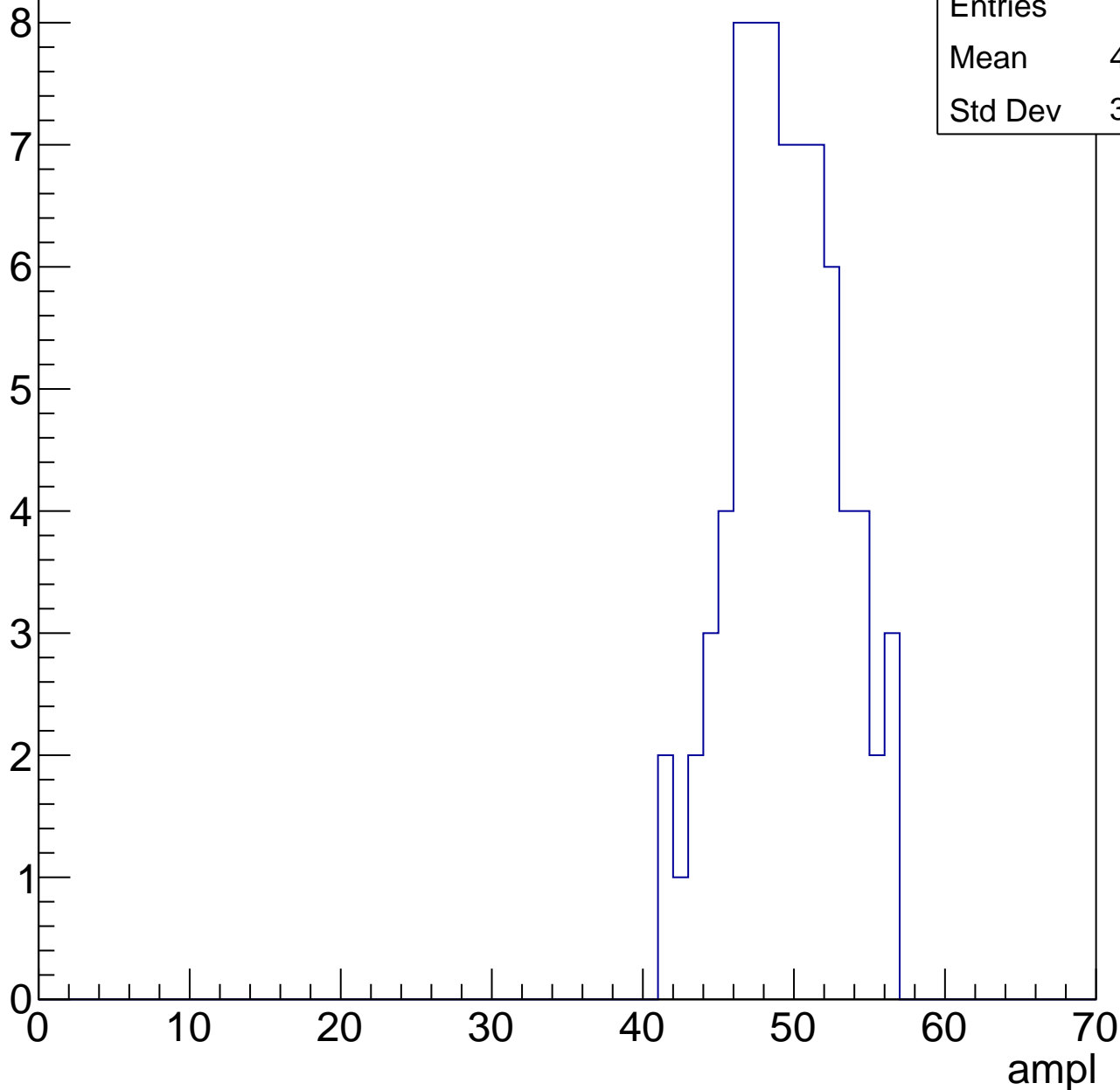


# B1L003S, U18-ch65, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

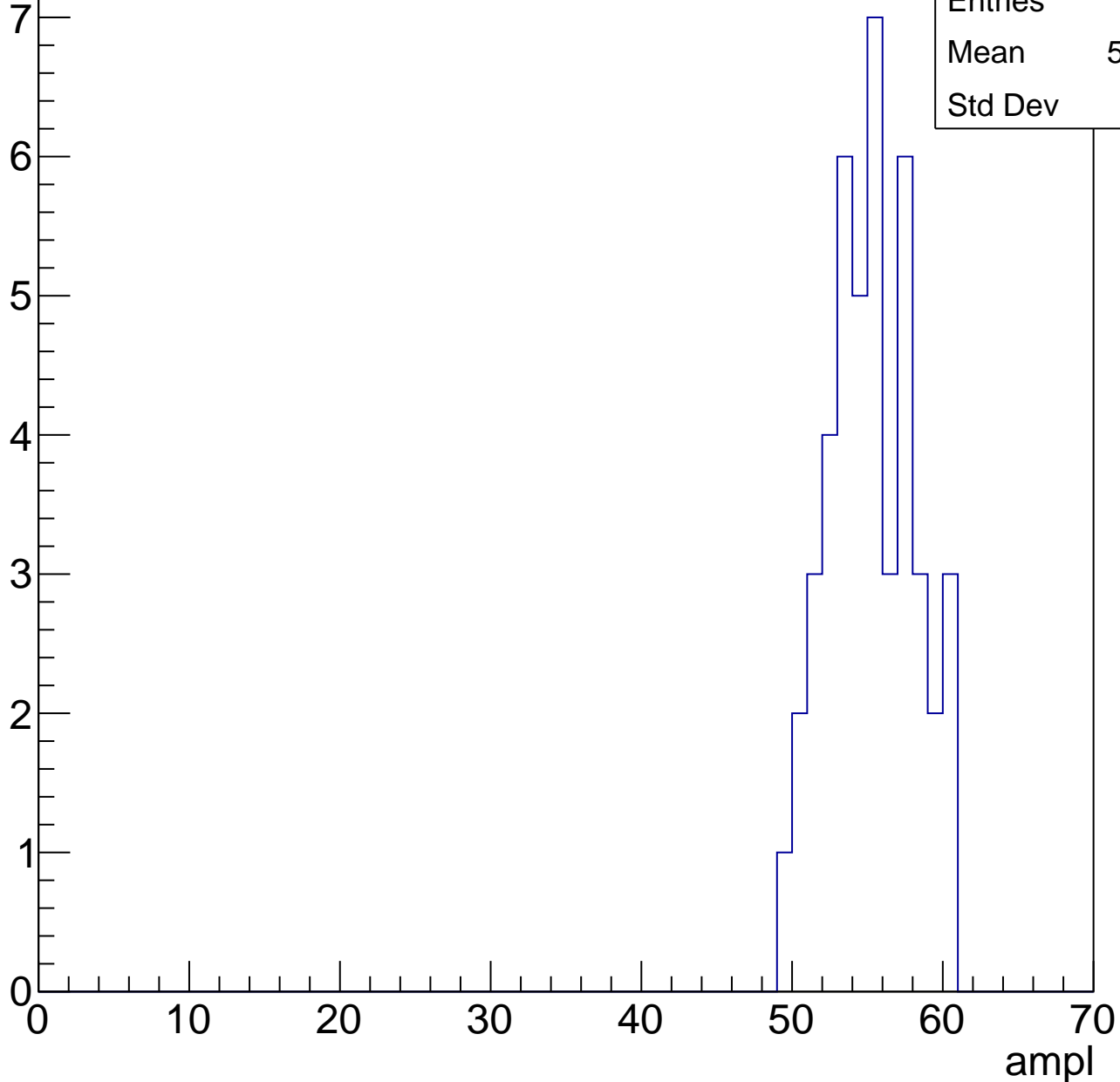
Entries	76
Mean	48.92
Std Dev	3.575



# B1L003S, U18-ch65, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

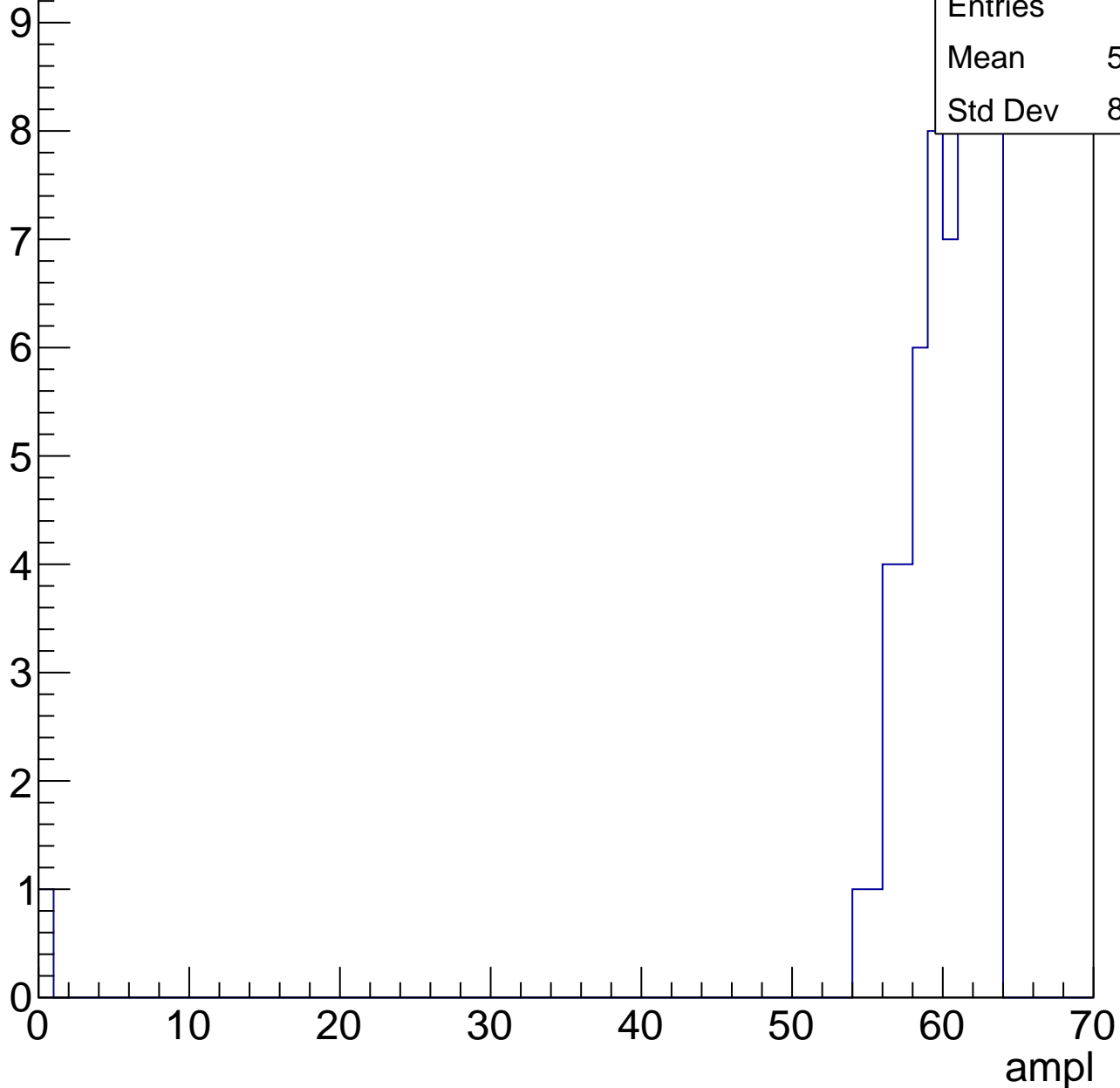
Entry



# B1L003S, U18-ch65, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

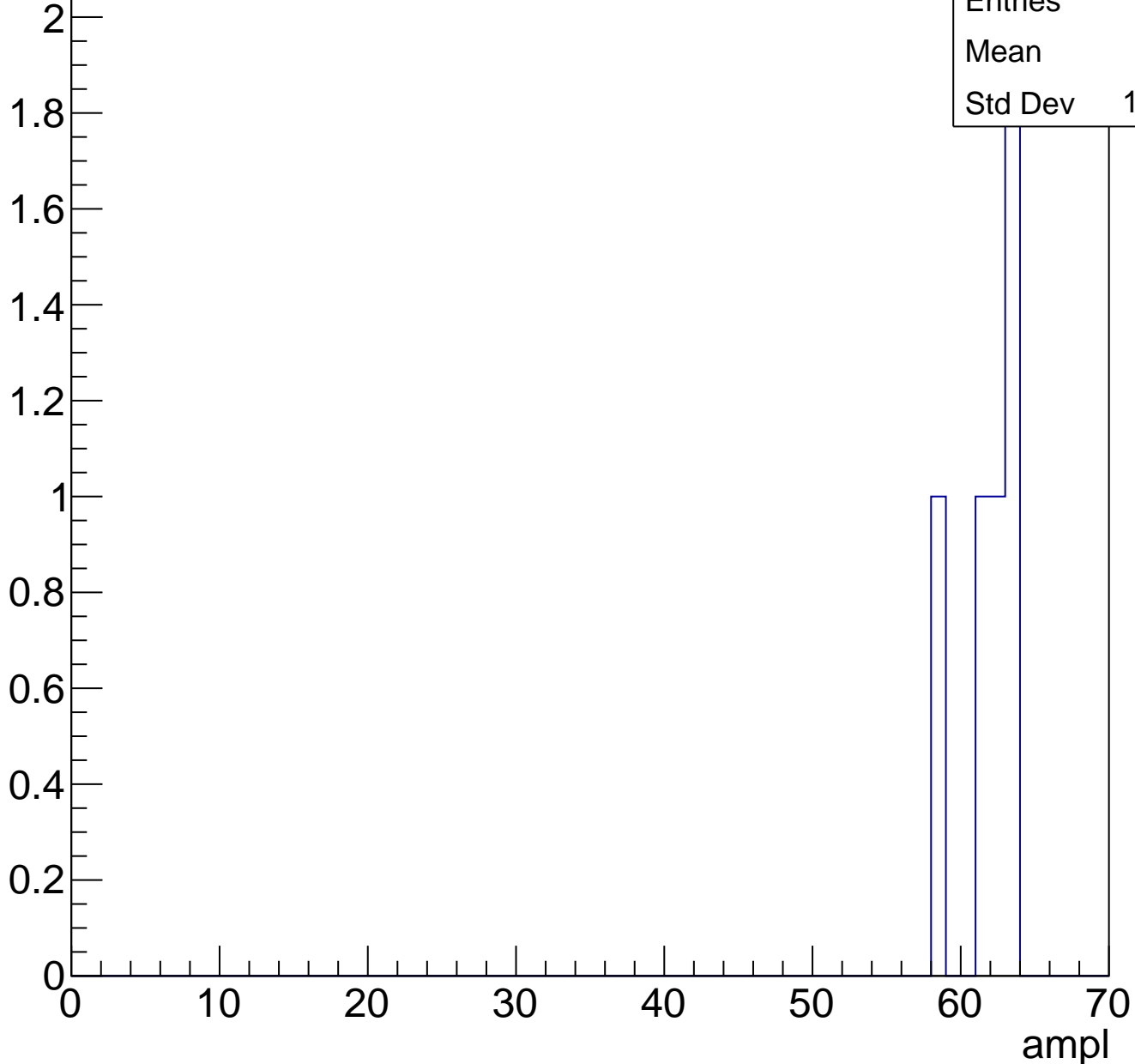
Entry



# B1L003S, U18-ch65, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	5
Mean	61.4
Std Dev	1.855



# B1L003S, U18-ch65, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U18-ch66, adc0

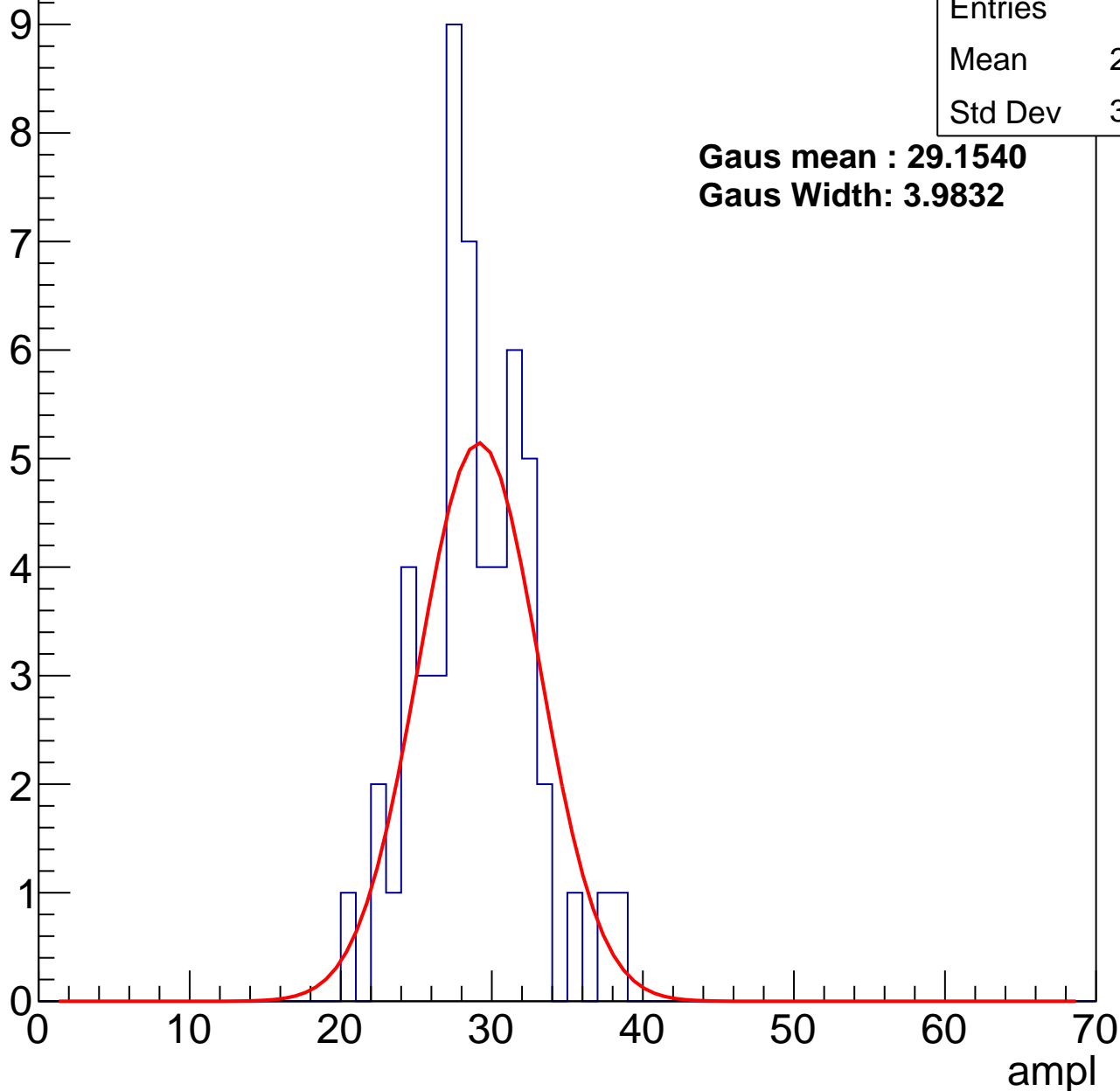
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	54
Mean	28.39
Std Dev	3.597

**Gaus mean : 29.1540**

**Gaus Width: 3.9832**



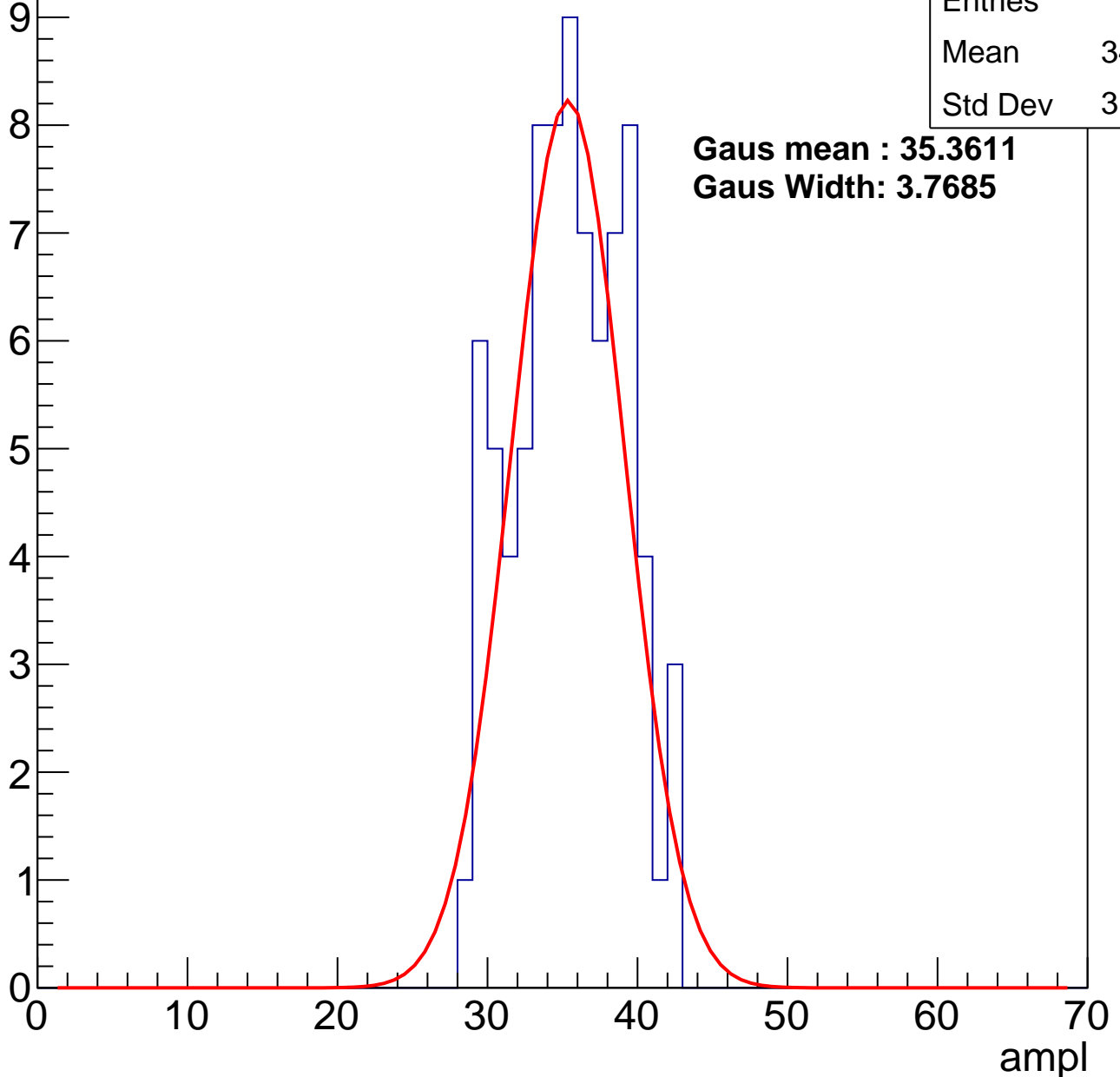
# B1L003S, U18-ch66, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	82
Mean	34.95
Std Dev	3.568

**Gaus mean : 35.3611**  
**Gaus Width: 3.7685**



# B1L003S, U18-ch66, adc2

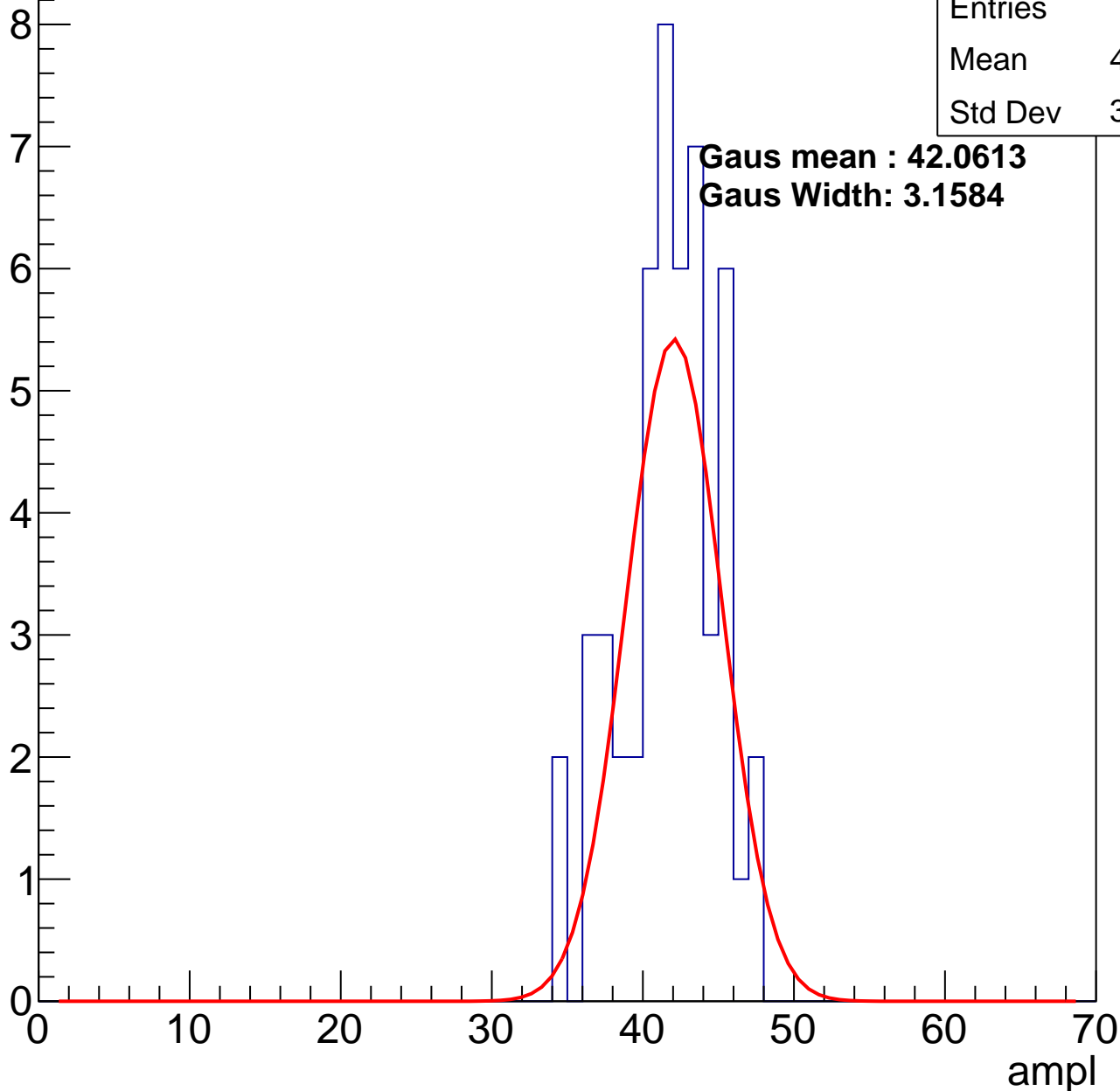
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	51
Mean	41.25
Std Dev	3.143

**Gaus mean : 42.0613**

**Gaus Width: 3.1584**

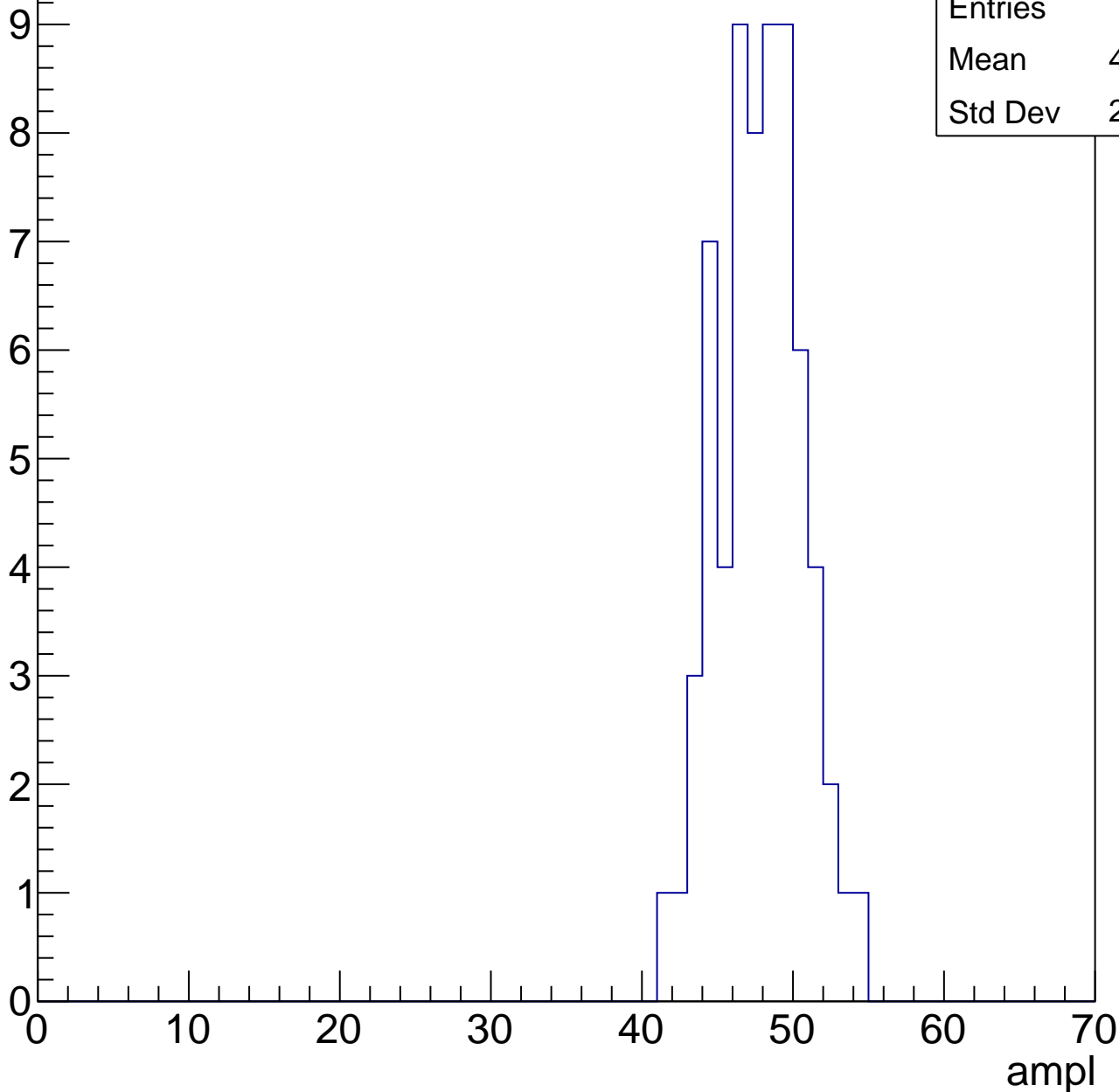


# B1L003S, U18-ch66, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

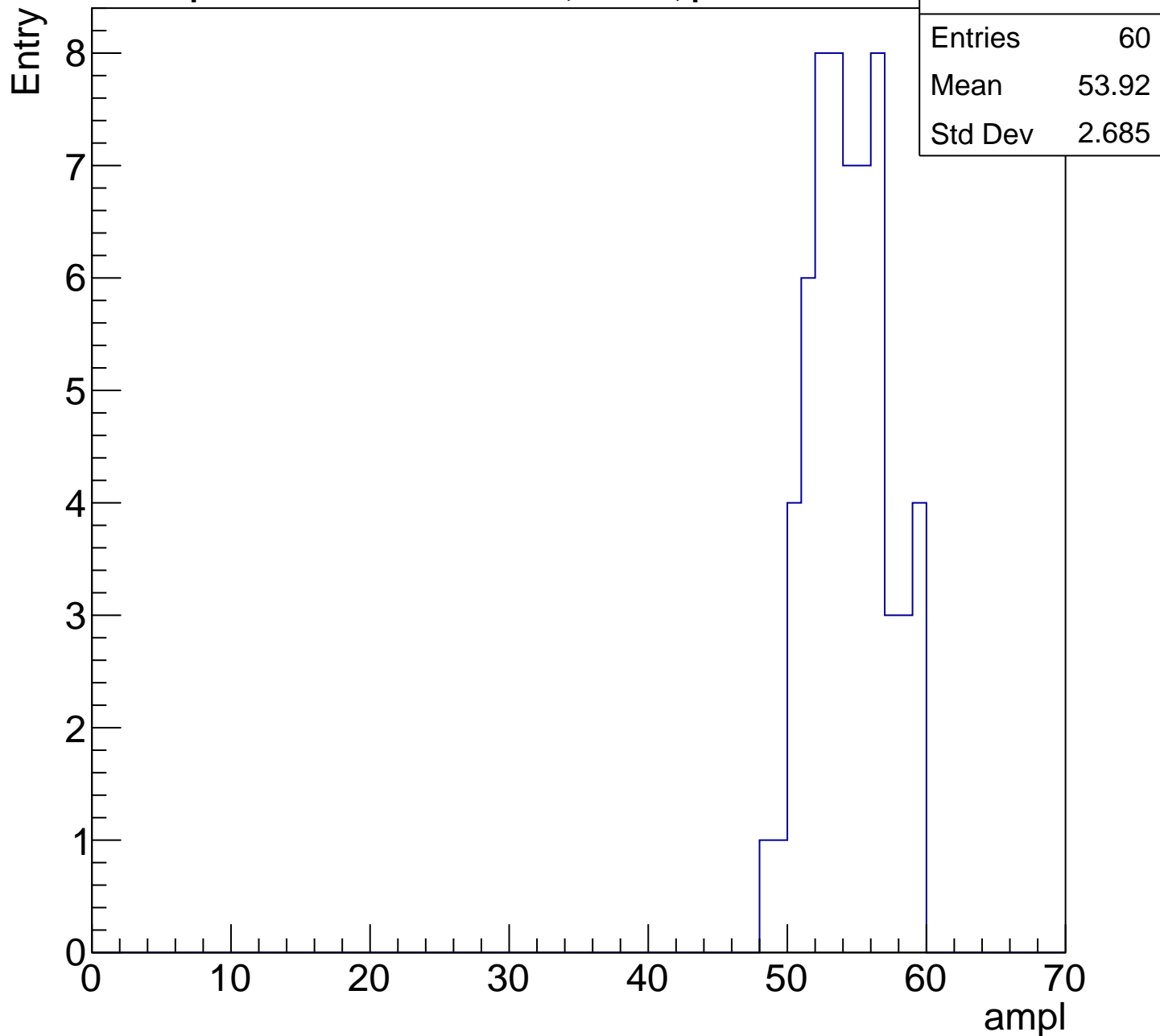
Entry

Entries	65
Mean	47.35
Std Dev	2.737



# B1L003S, U18-ch66, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

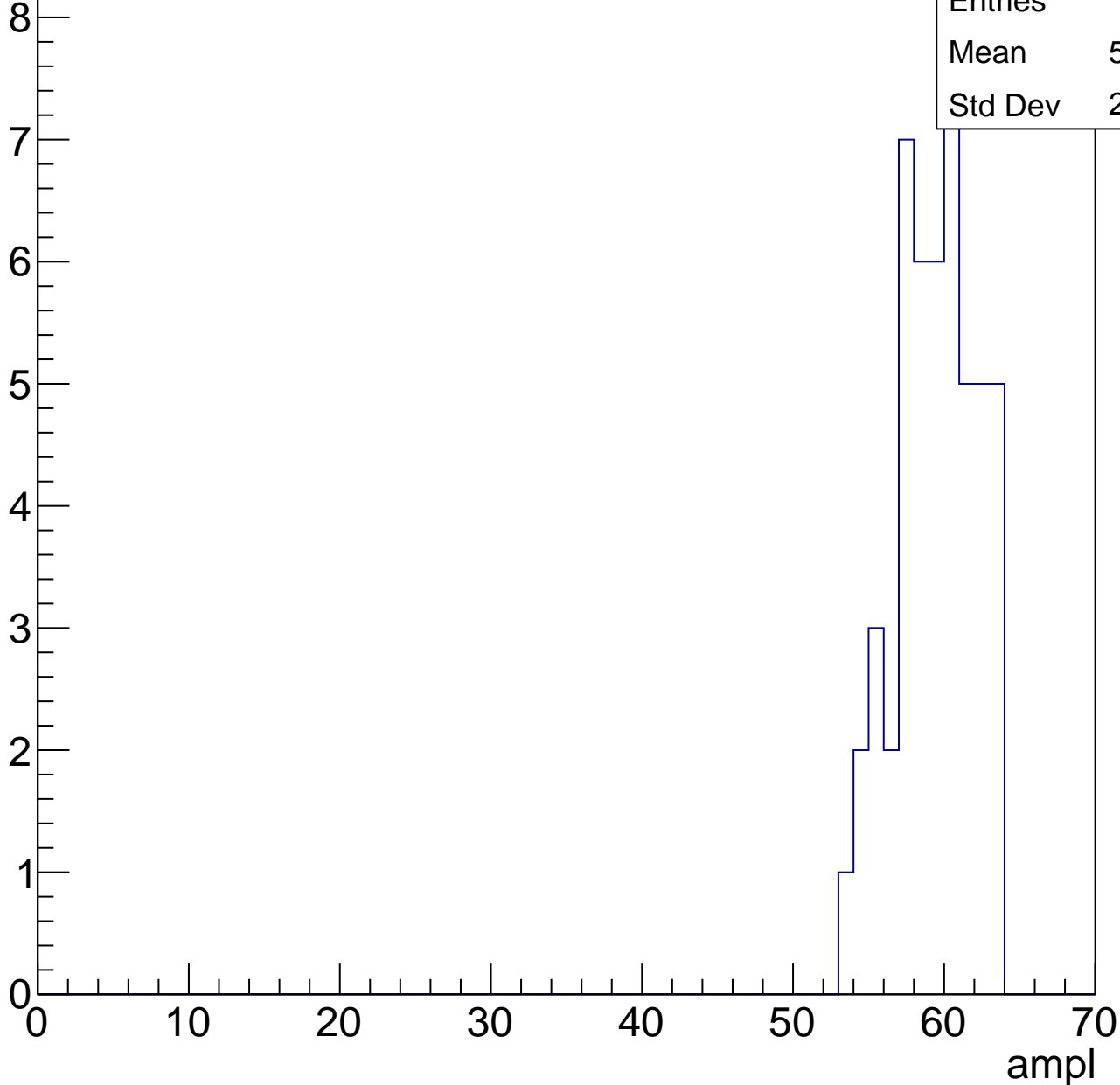


# B1L003S, U18-ch66, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

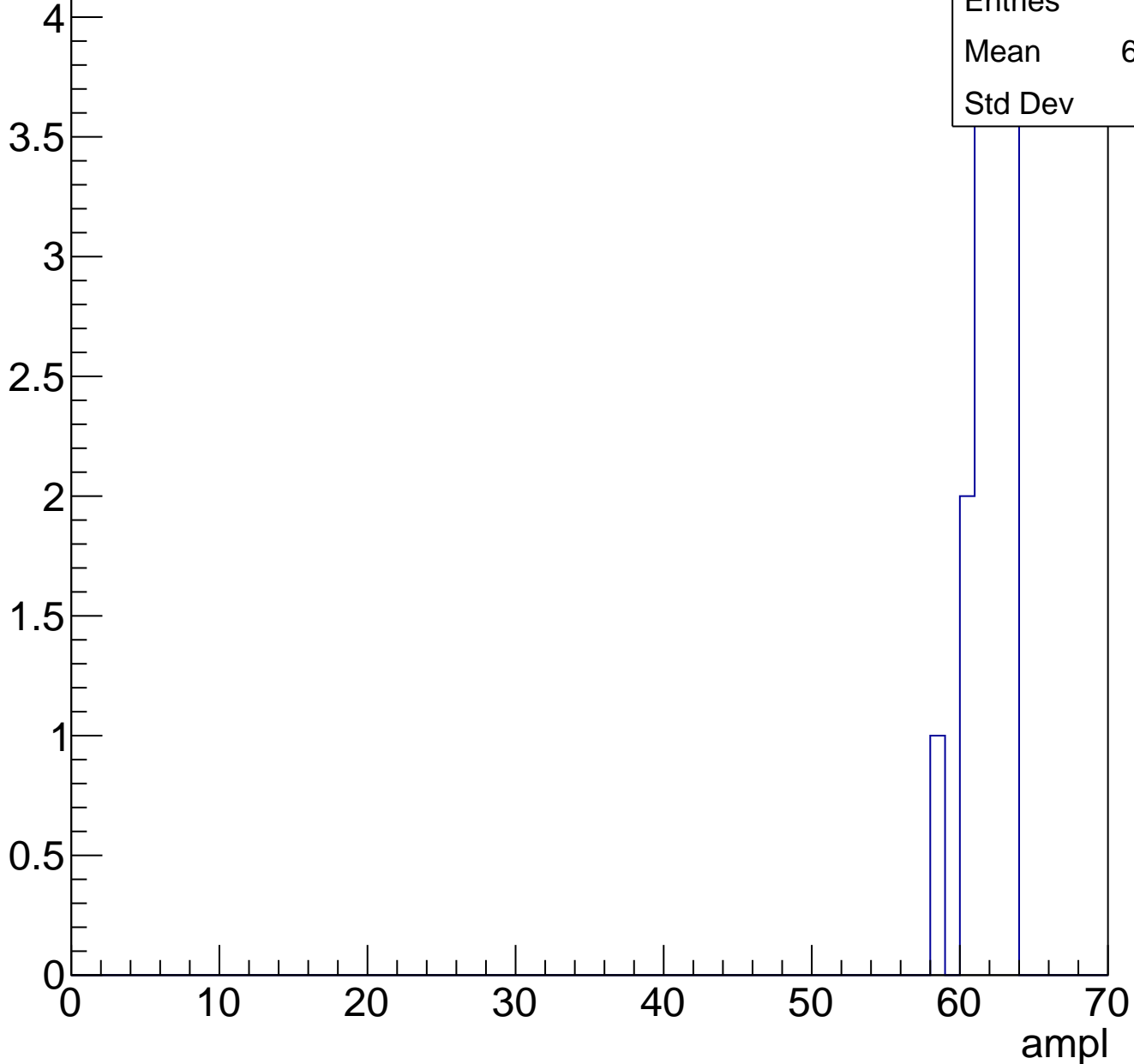
Entries	50
Mean	58.98
Std Dev	2.604



# B1L003S, U18-ch66, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

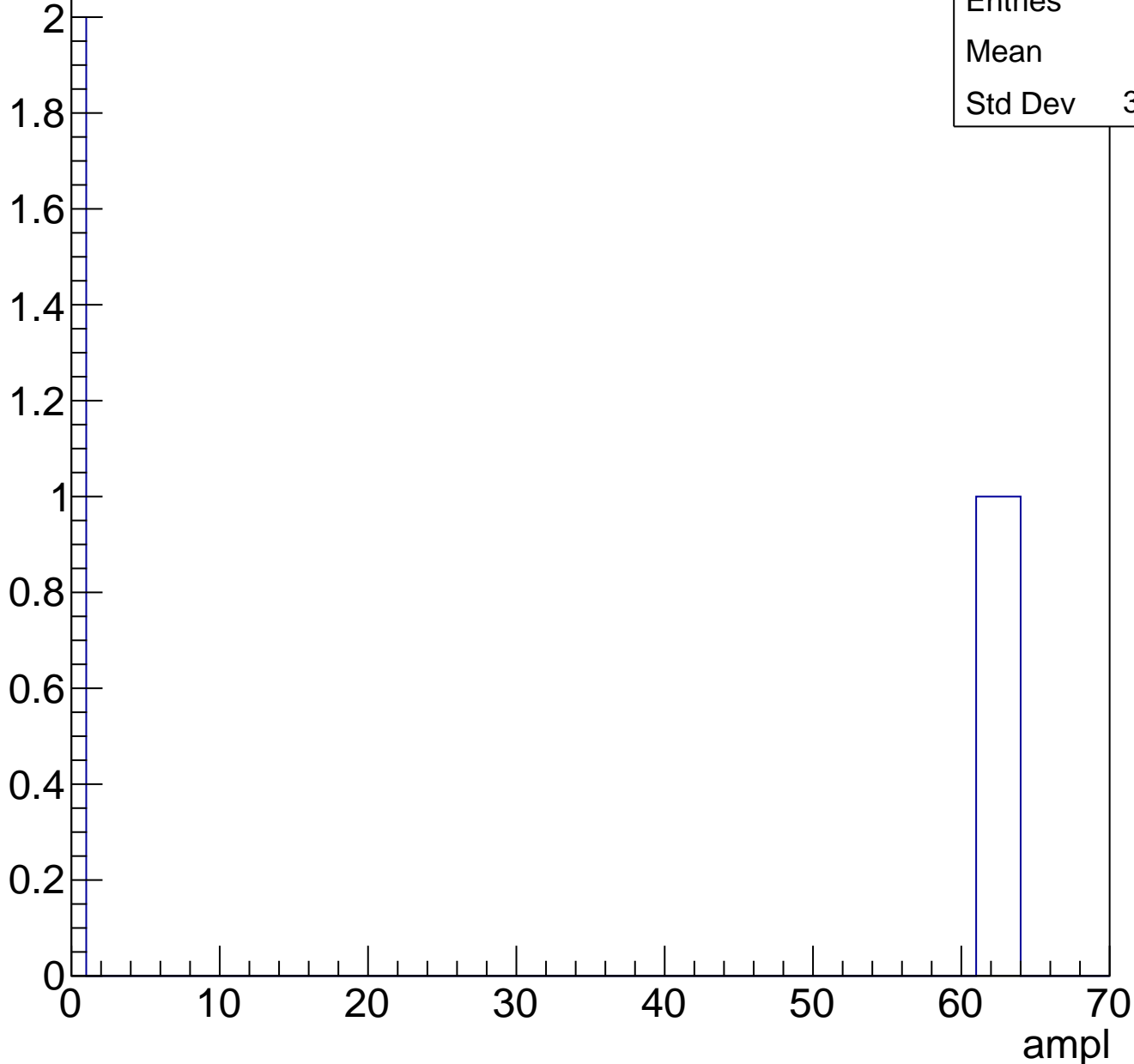




# B1L003S, U18-ch66, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U18-ch67, adc0

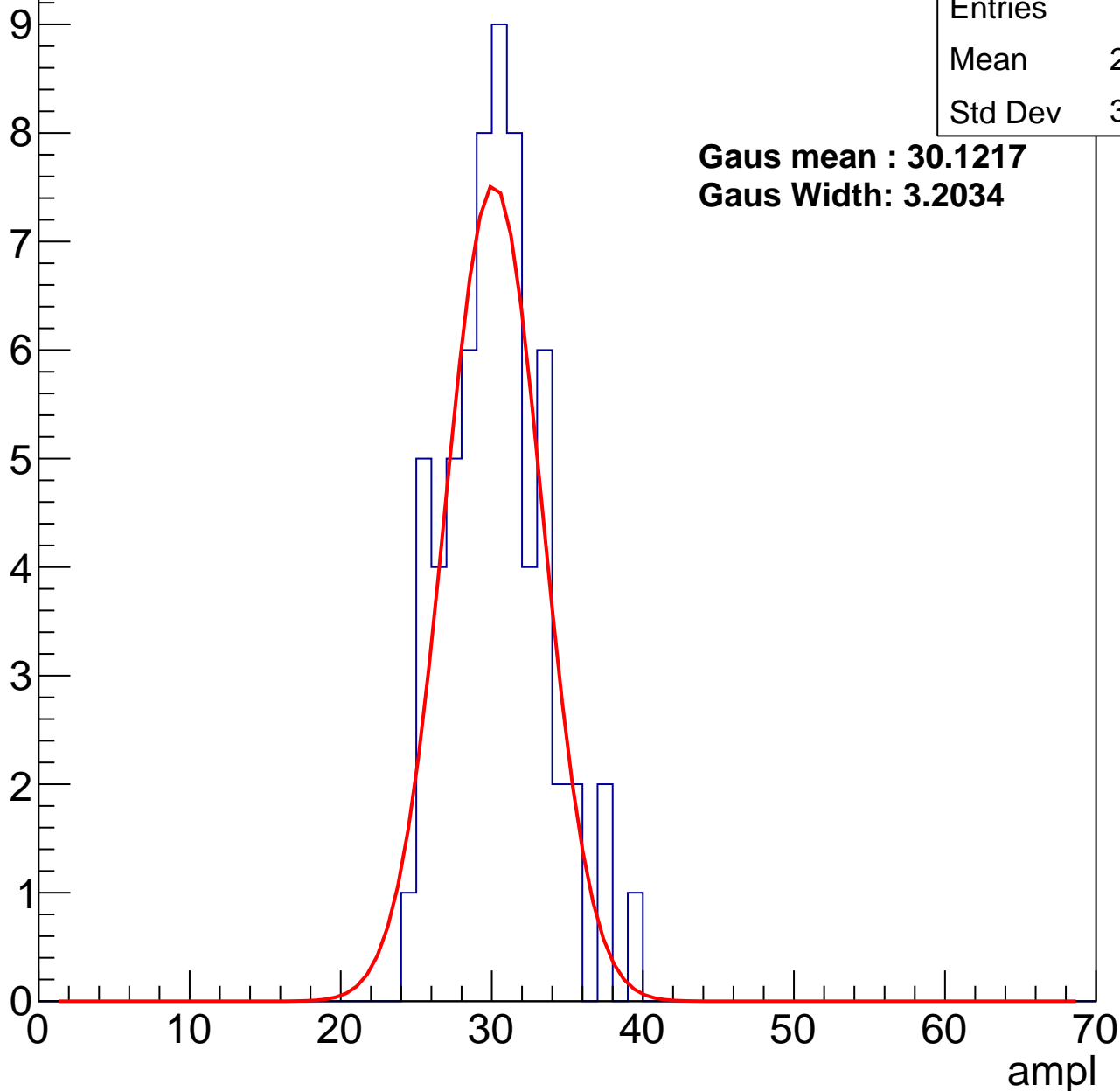
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	63
Mean	29.89
Std Dev	3.188

**Gaus mean : 30.1217**

**Gaus Width: 3.2034**

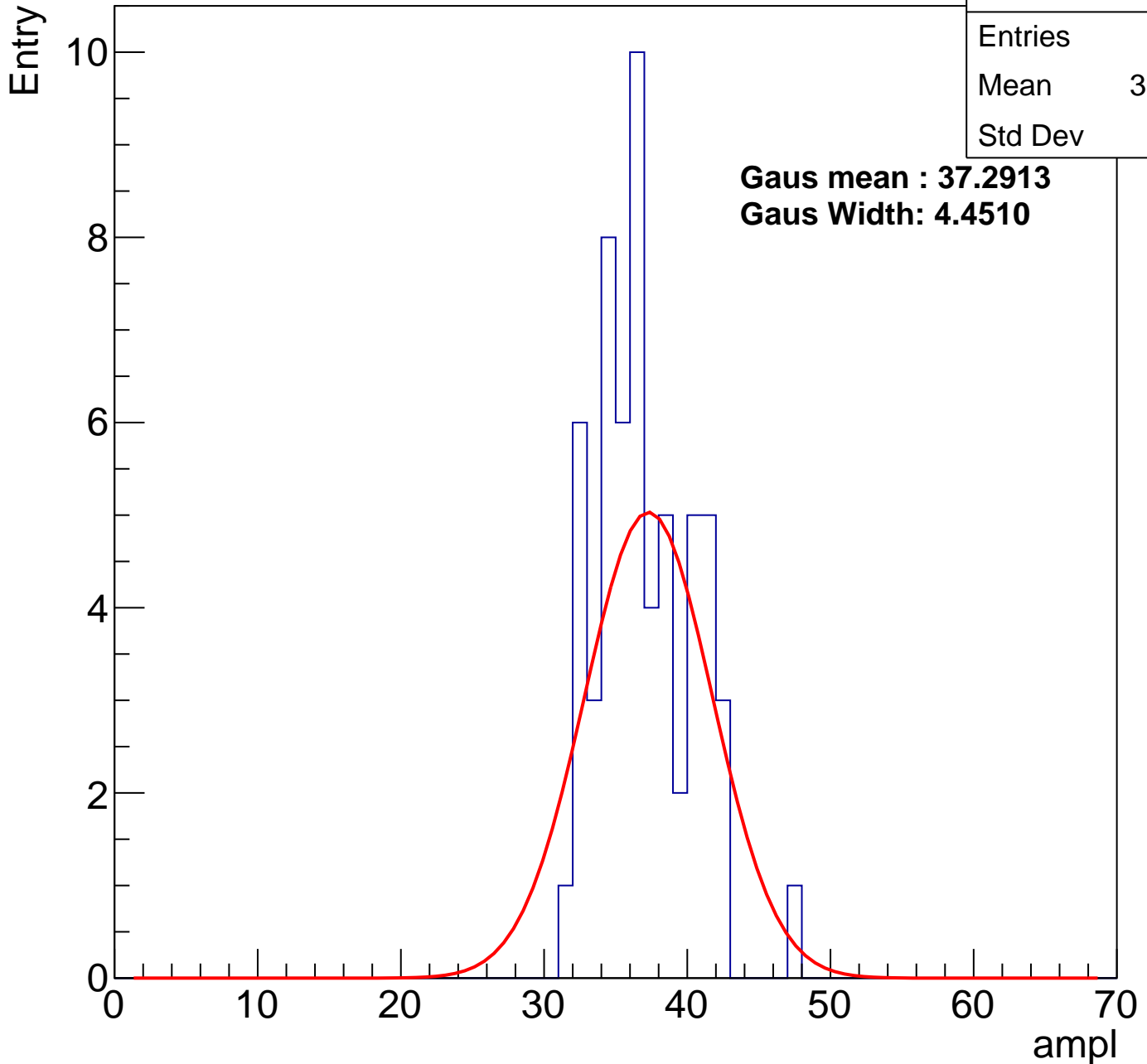


# B1L003S, U18-ch67, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	59
Mean	36.58
Std Dev	3.3

**Gaus mean : 37.2913**  
**Gaus Width: 4.4510**



# B1L003S, U18-ch67, adc2

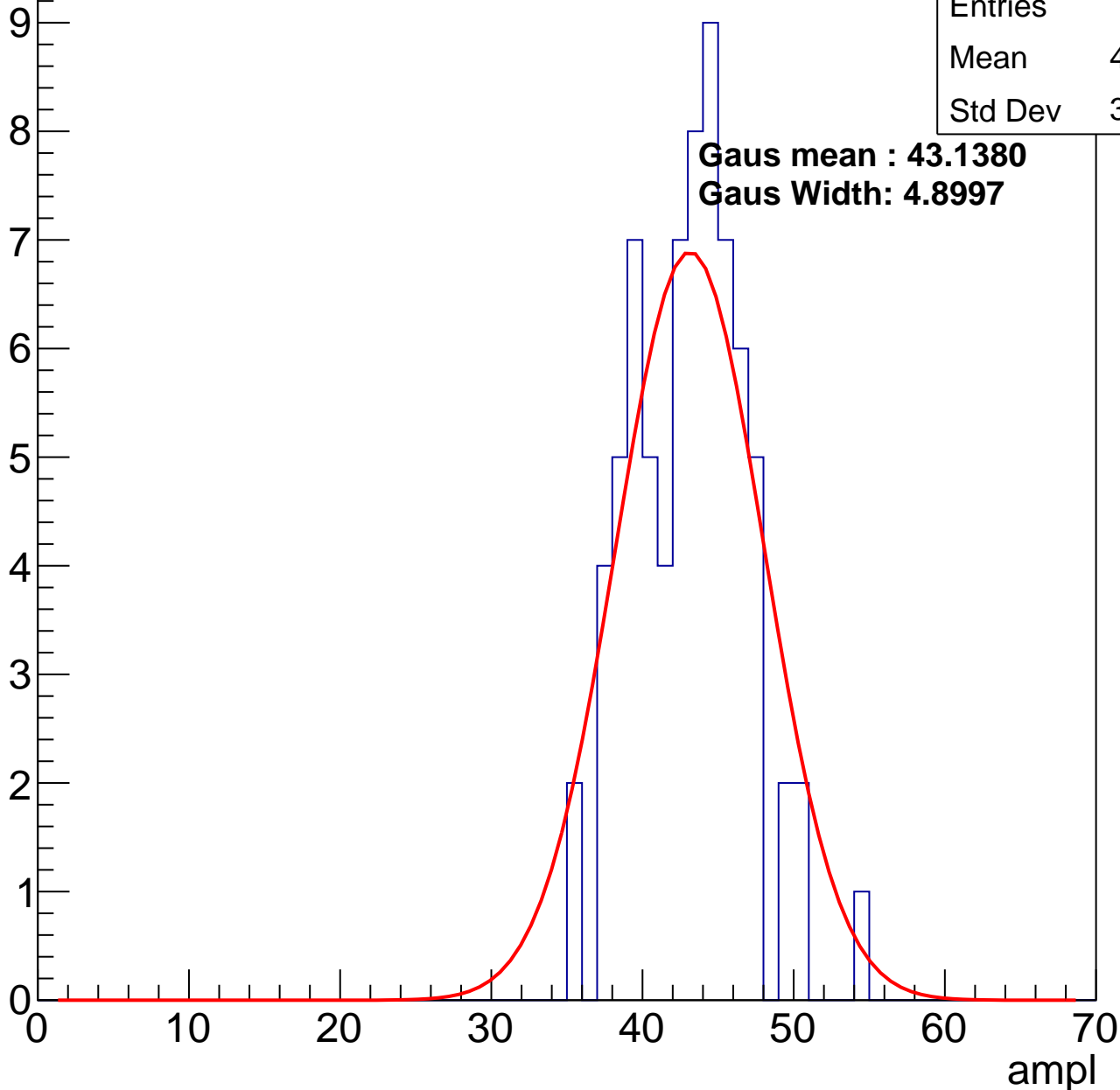
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	74
Mean	42.66
Std Dev	3.732

**Gaus mean : 43.1380**

**Gaus Width: 4.8997**

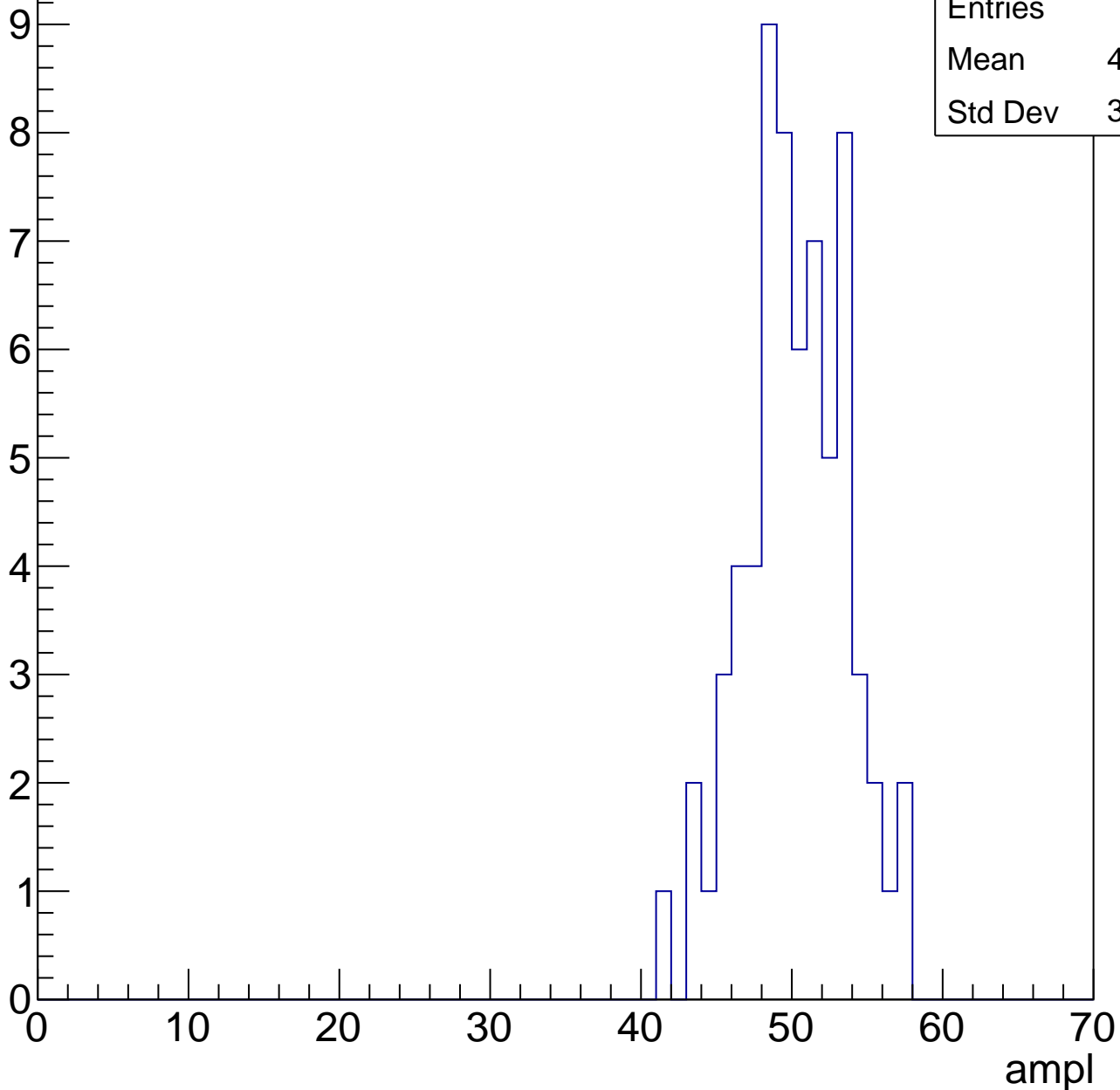


# B1L003S, U18-ch67, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

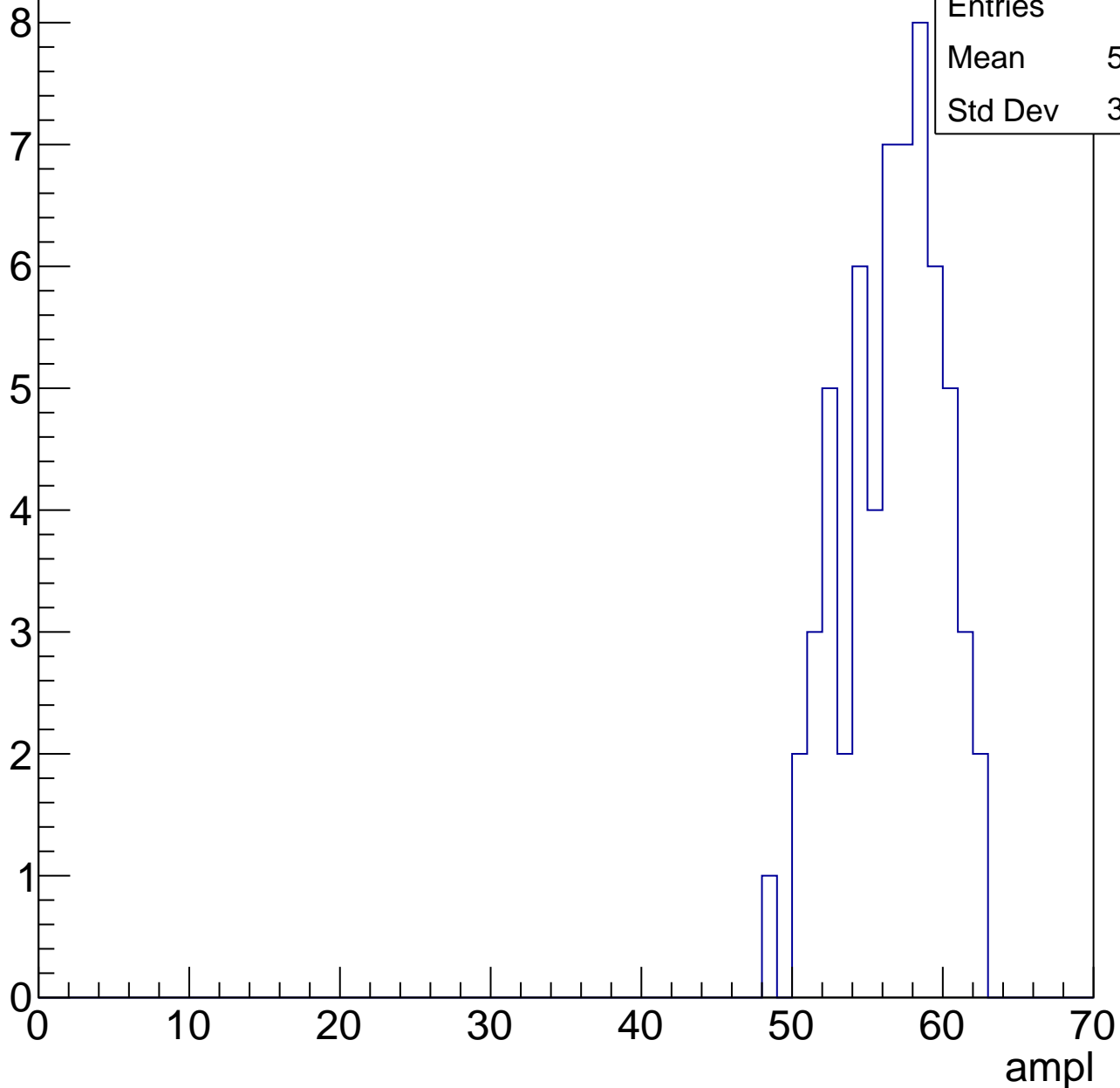
Entries	66
Mean	49.77
Std Dev	3.397



# B1L003S, U18-ch67, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



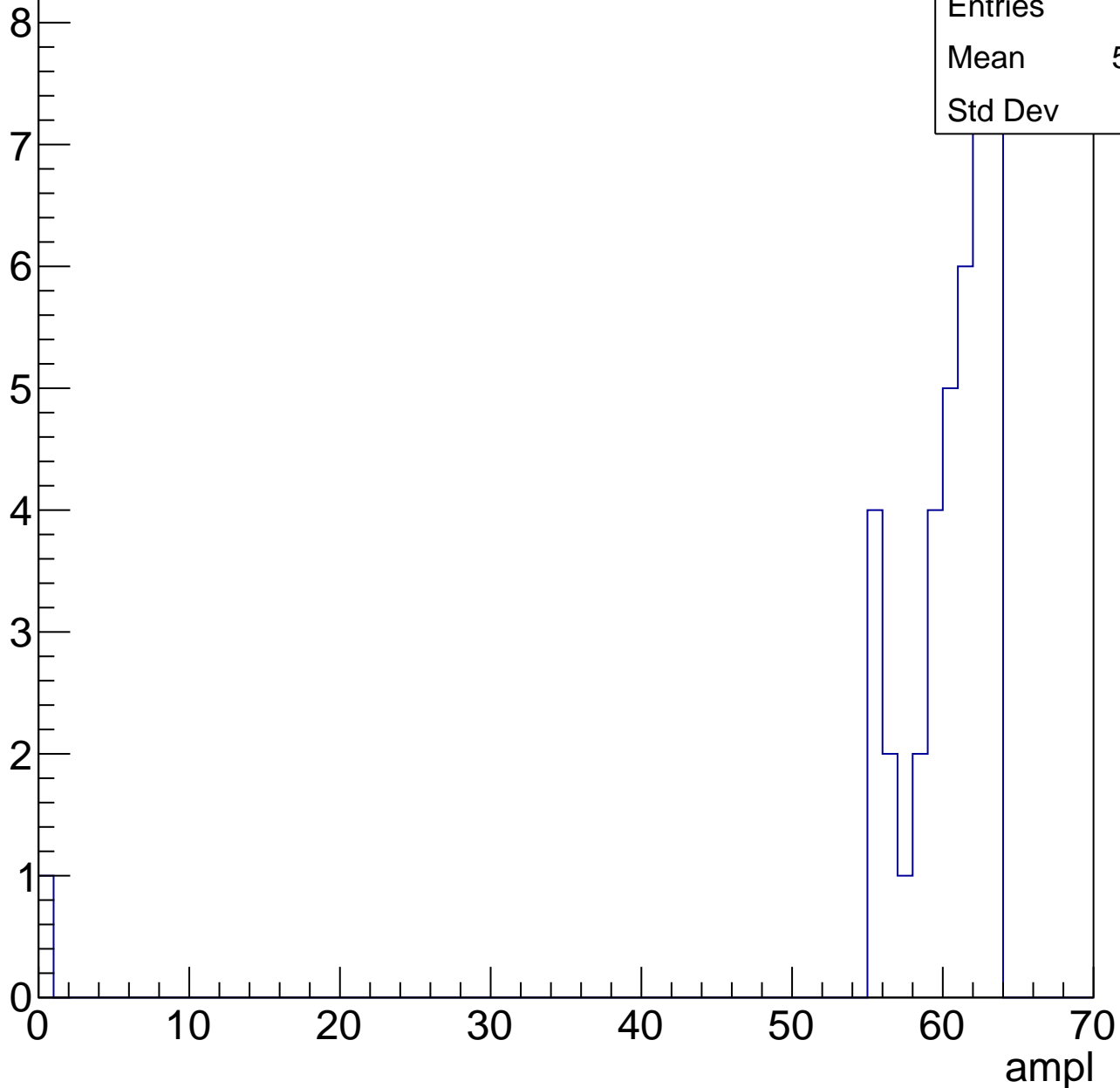
Entries	61
Mean	56.18
Std Dev	3.277

# B1L003S, U18-ch67, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	41
Mean	58.71
Std Dev	9.62



# B1L003S, U18-ch67, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

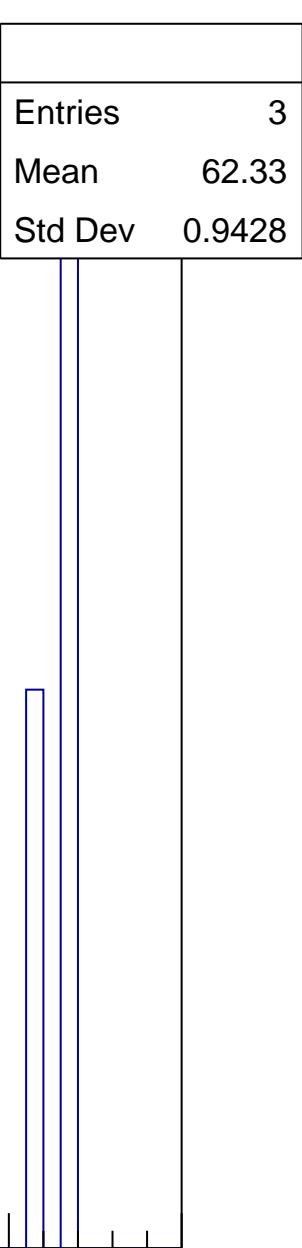
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	3
Mean	62.33
Std Dev	0.9428

0 10 20 30 40 50 60 70

ampl





# B1L003S, U18-ch67, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	3
Mean	7.667
Std Dev	10.84

# B1L003S, U18-ch68, adc0

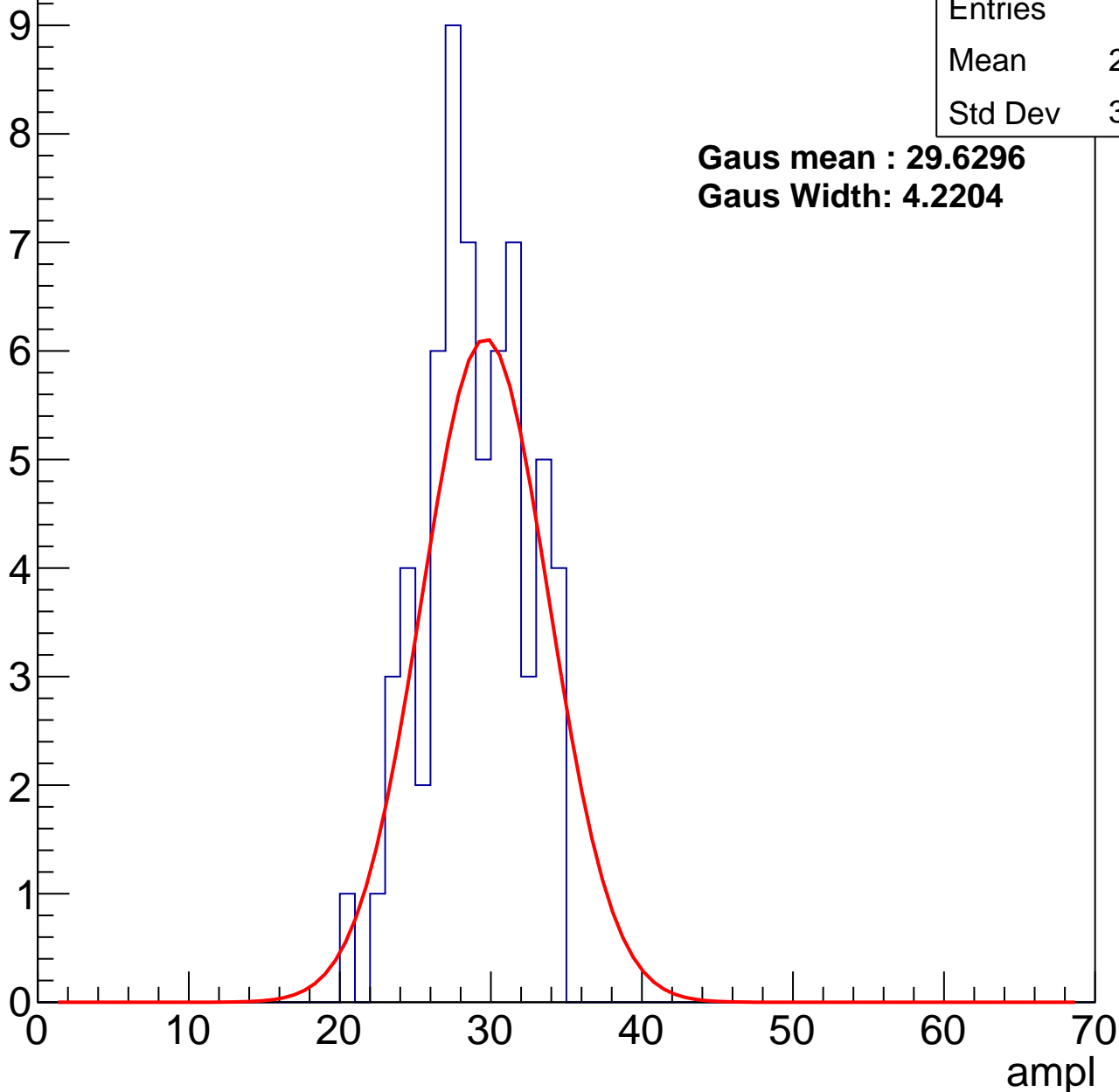
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	63
Mean	28.43
Std Dev	3.303

**Gaus mean : 29.6296**

**Gaus Width: 4.2204**



# B1L003S, U18-ch68, adc1

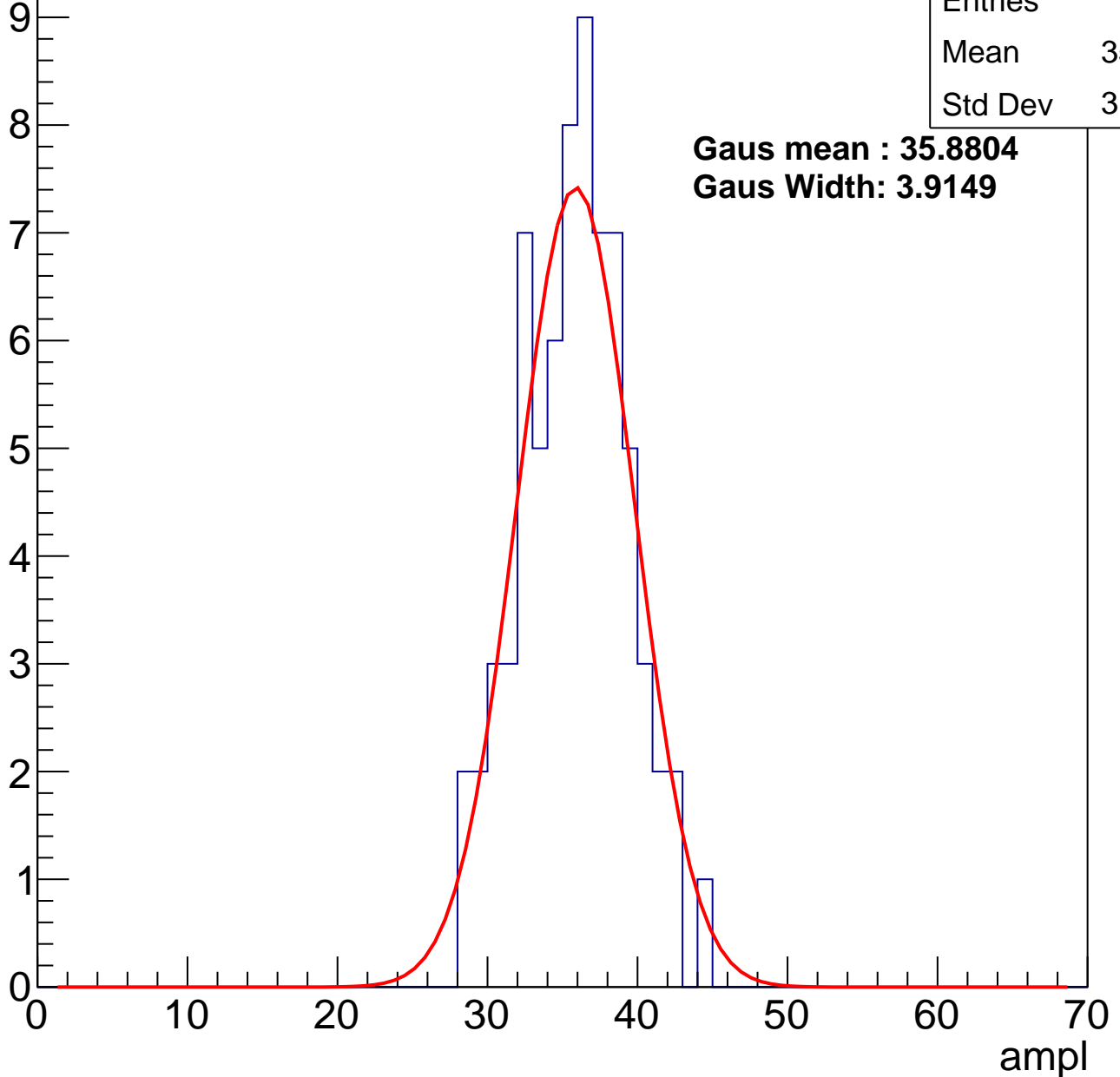
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	72
Mean	35.33
Std Dev	3.496

**Gaus mean : 35.8804**

**Gaus Width: 3.9149**



# B1L003S, U18-ch68, adc2

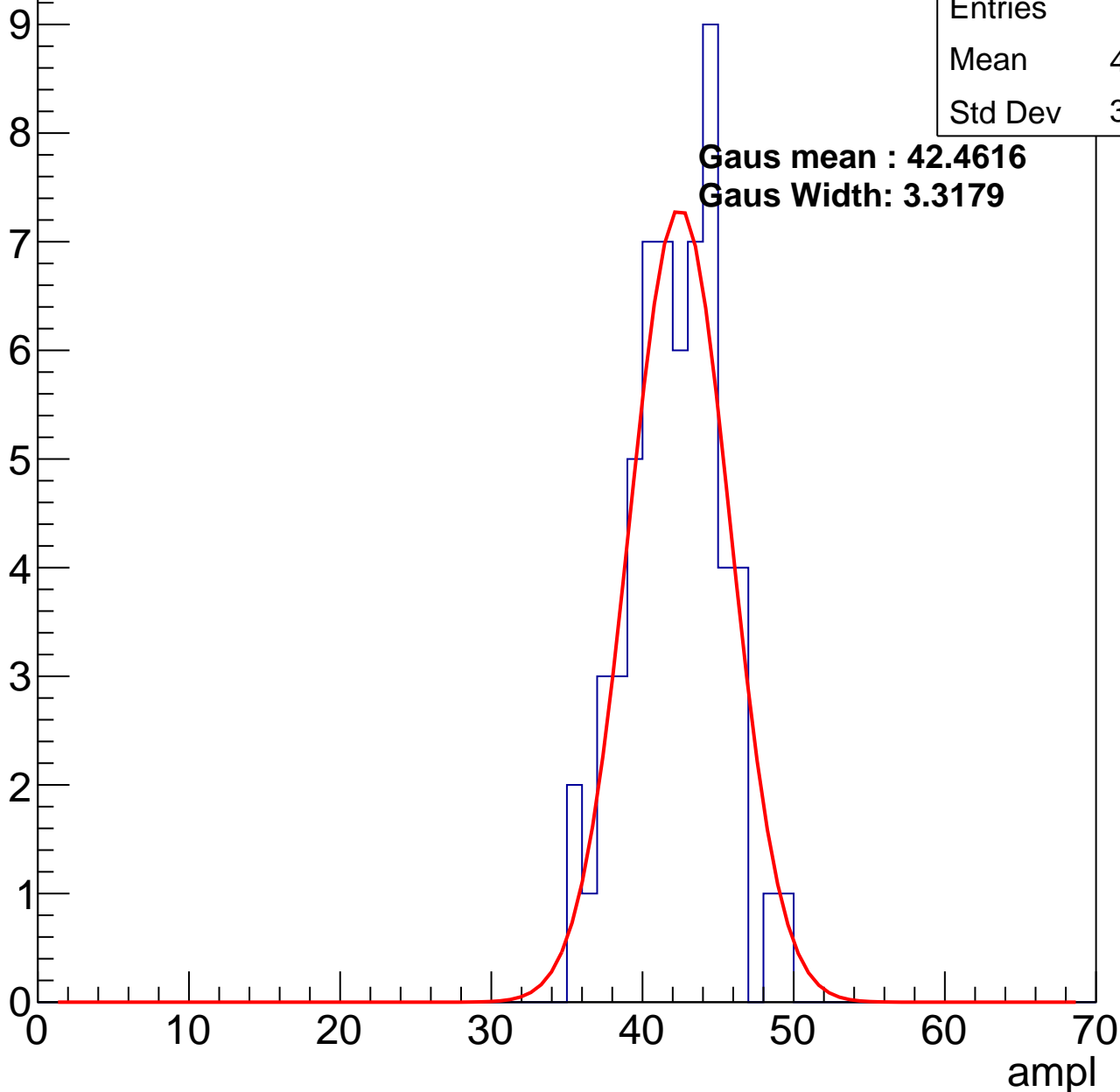
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	60
Mean	41.72
Std Dev	3.056

**Gaus mean : 42.4616**

**Gaus Width: 3.3179**

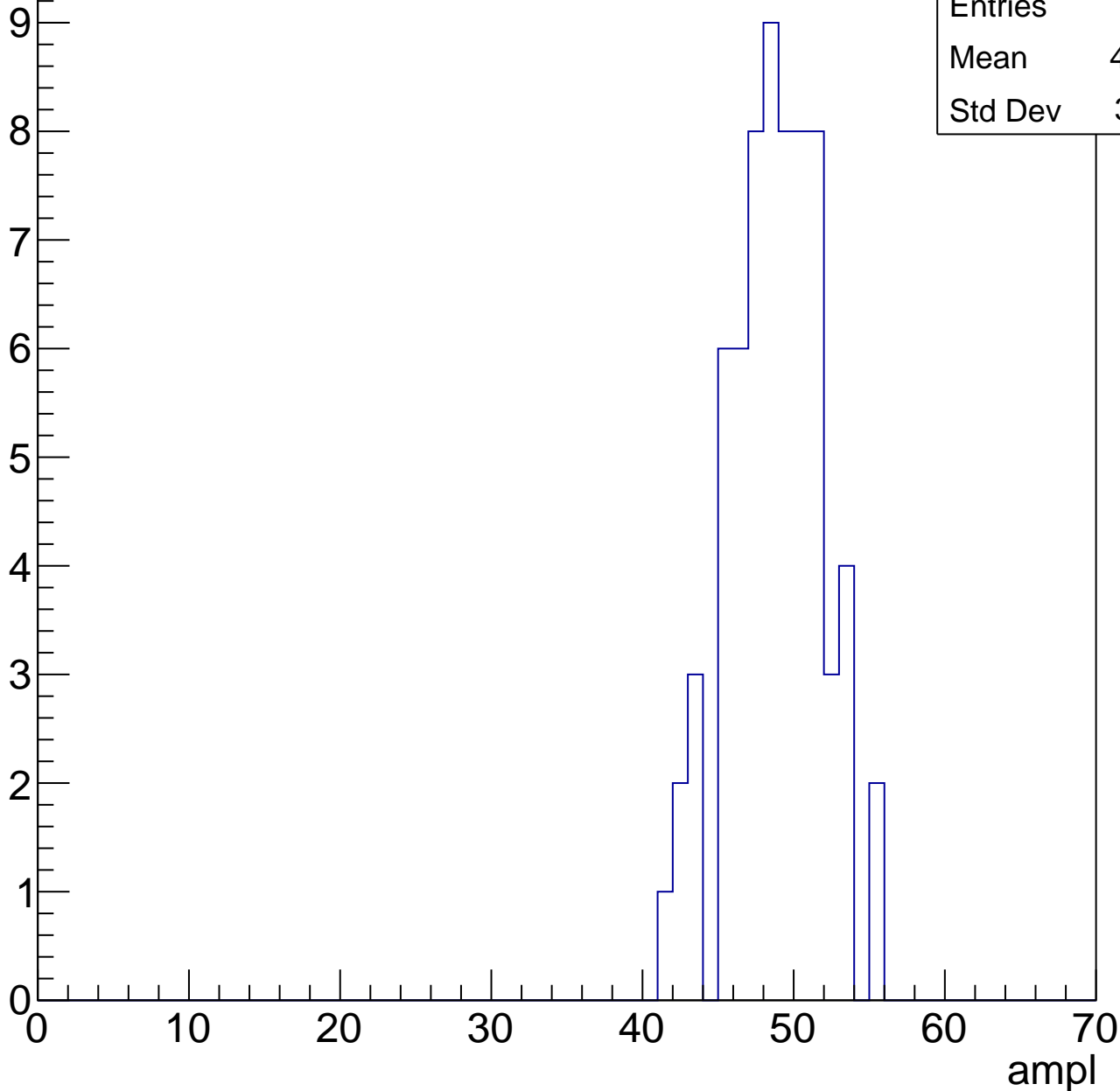


# B1L003S, U18-ch68, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	68
Mean	48.32
Std Dev	3.051

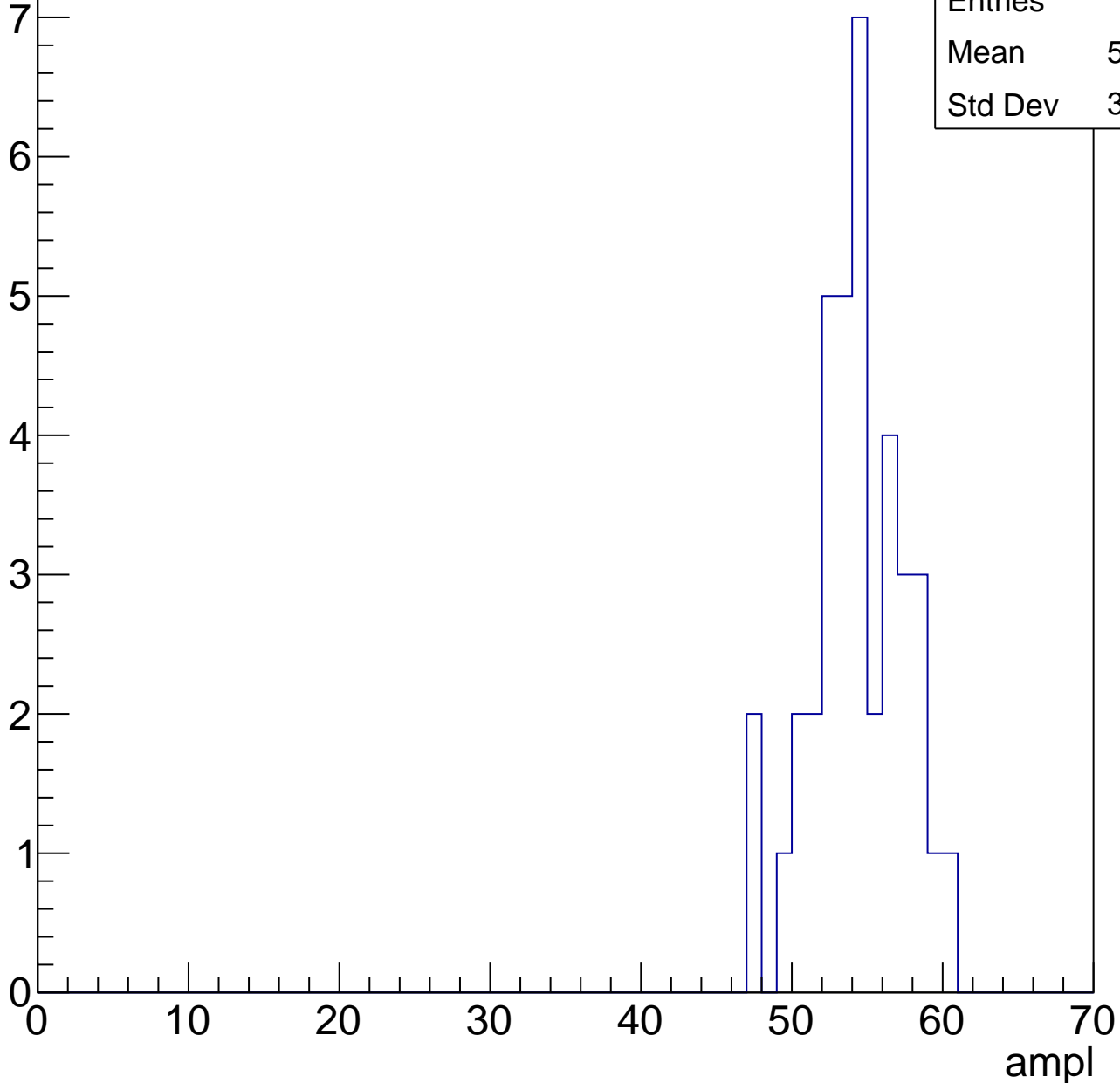


# B1L003S, U18-ch68, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	38
Mean	53.84
Std Dev	3.039

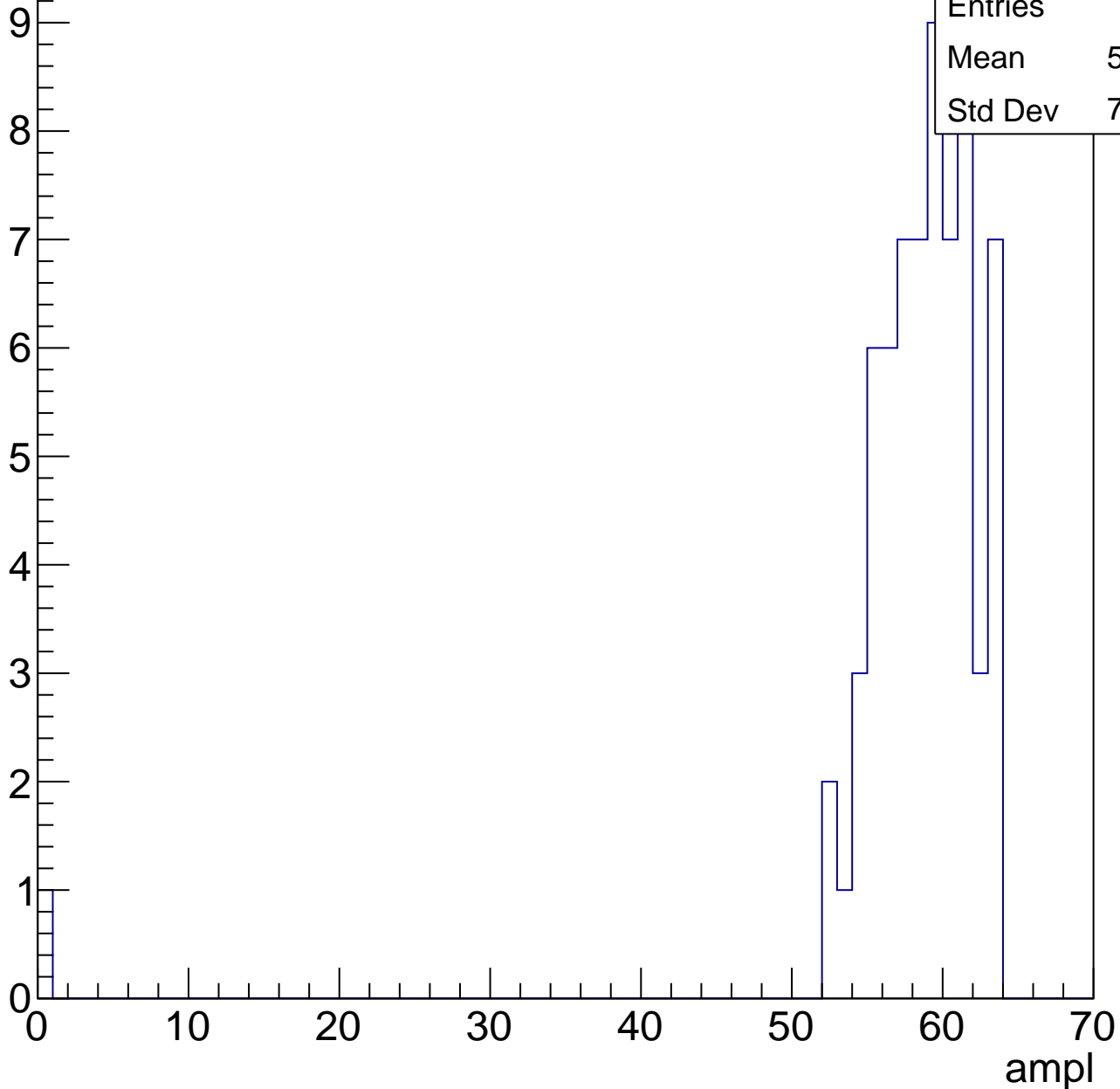


# B1L003S, U18-ch68, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	67
Mean	57.55
Std Dev	7.642

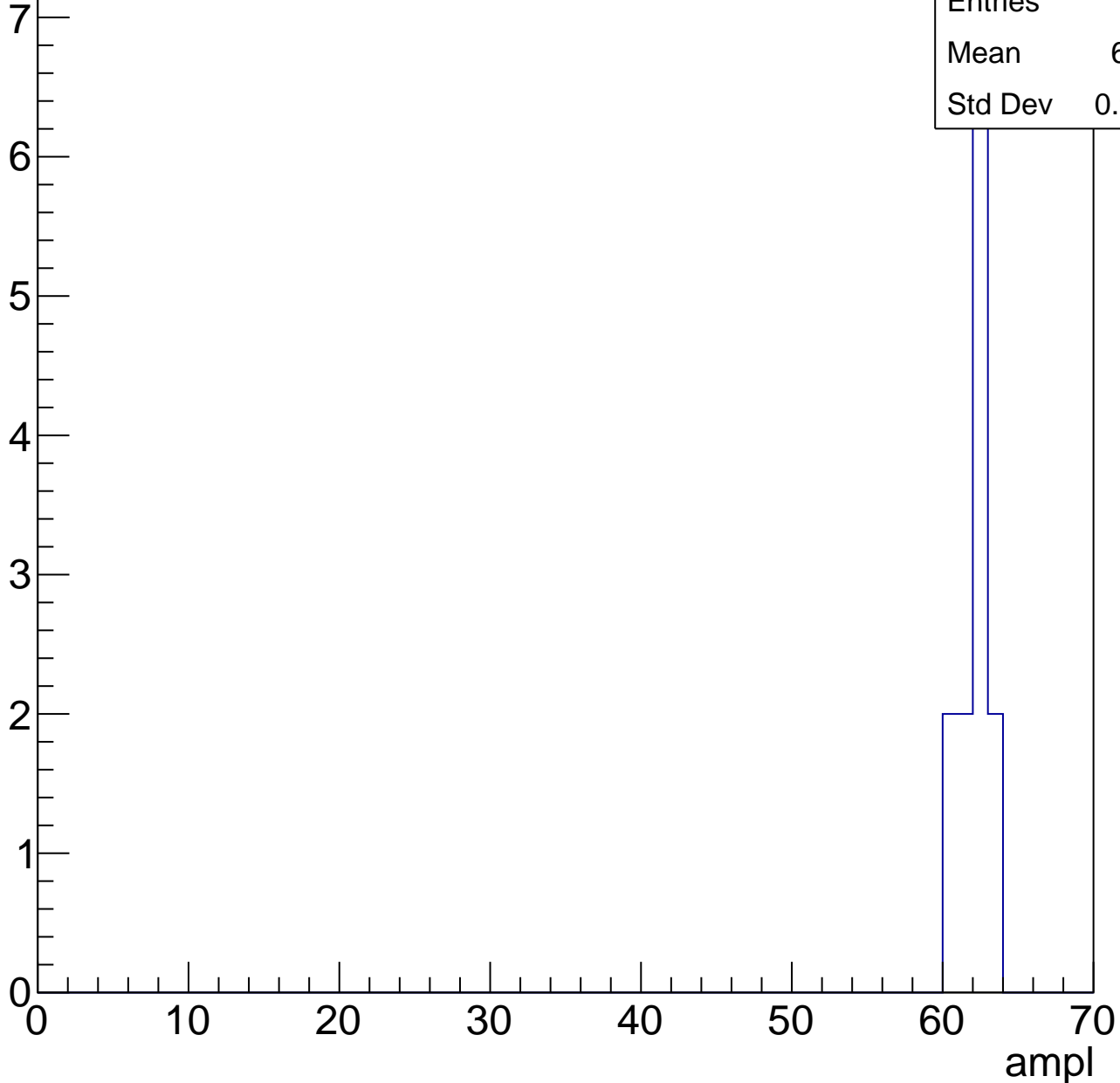


# B1L003S, U18-ch68, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	13
Mean	61.69
Std Dev	0.9102





# B1L003S, U18-ch68, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U18-ch69, adc0

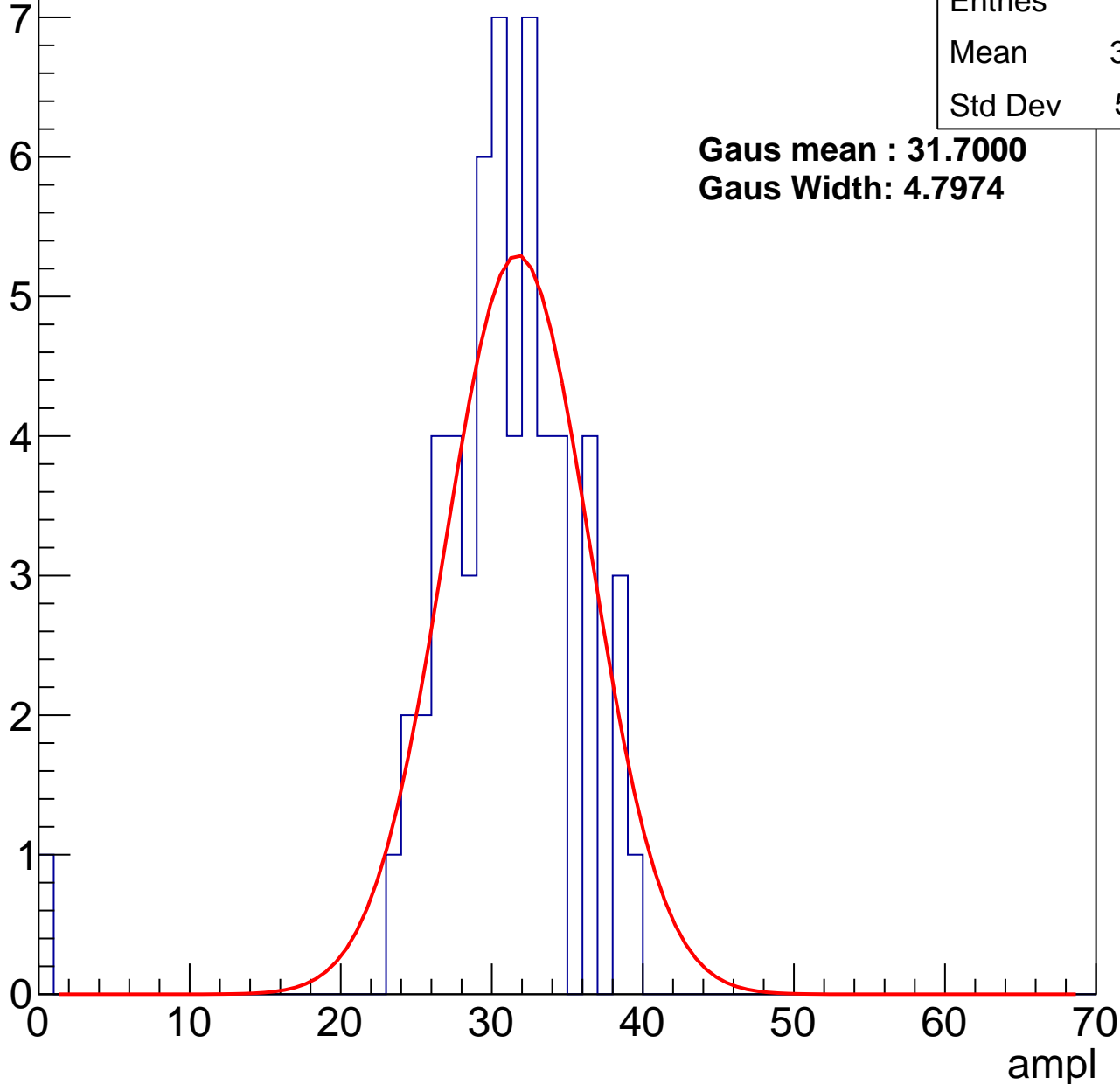
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	57
Mean	30.07
Std Dev	5.521

**Gaus mean : 31.7000**

**Gaus Width: 4.7974**



# B1L003S, U18-ch69, adc1

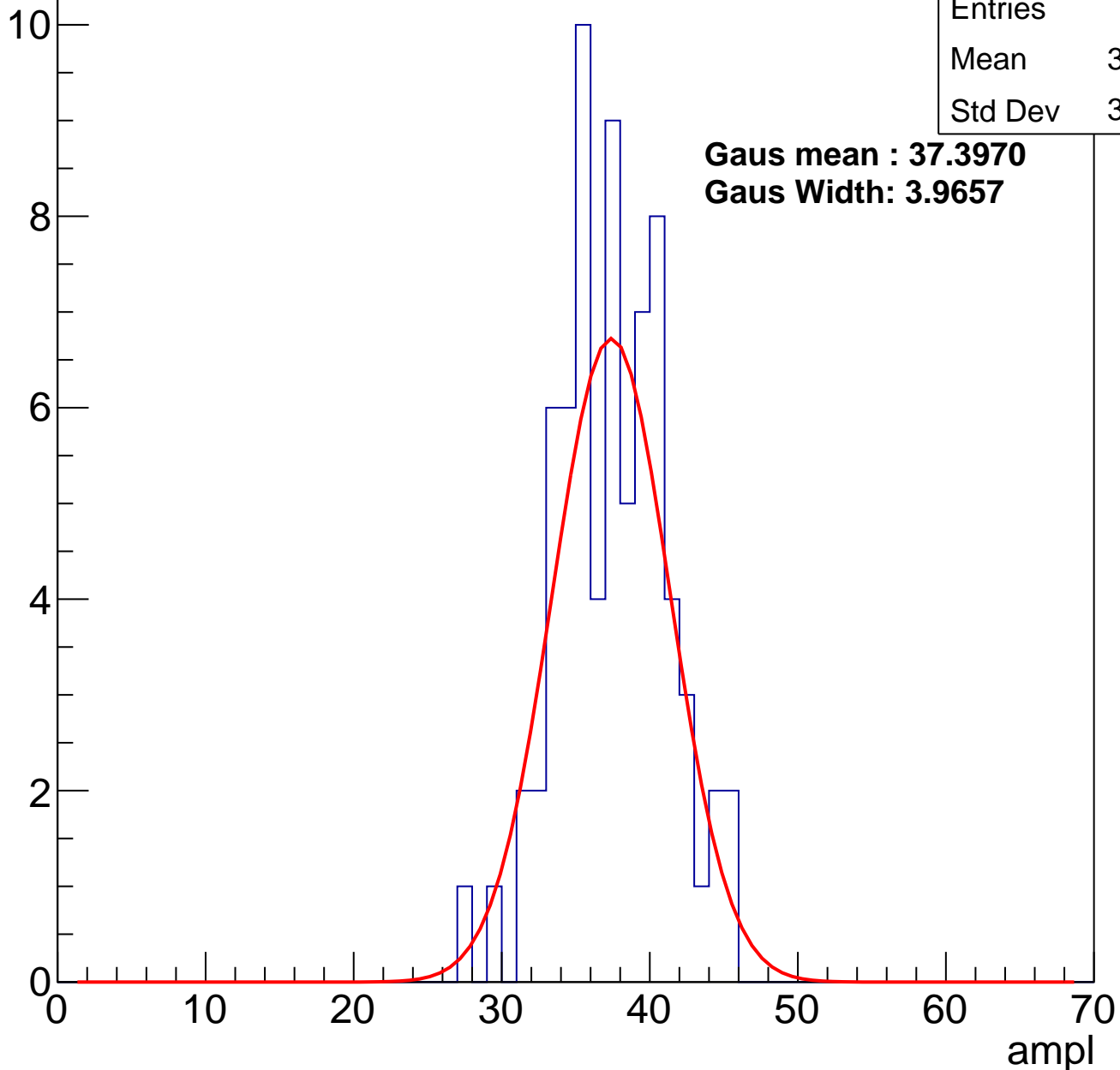
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	73
Mean	37.05
Std Dev	3.675

**Gaus mean : 37.3970**

**Gaus Width: 3.9657**

Entry



# B1L003S, U18-ch69, adc2

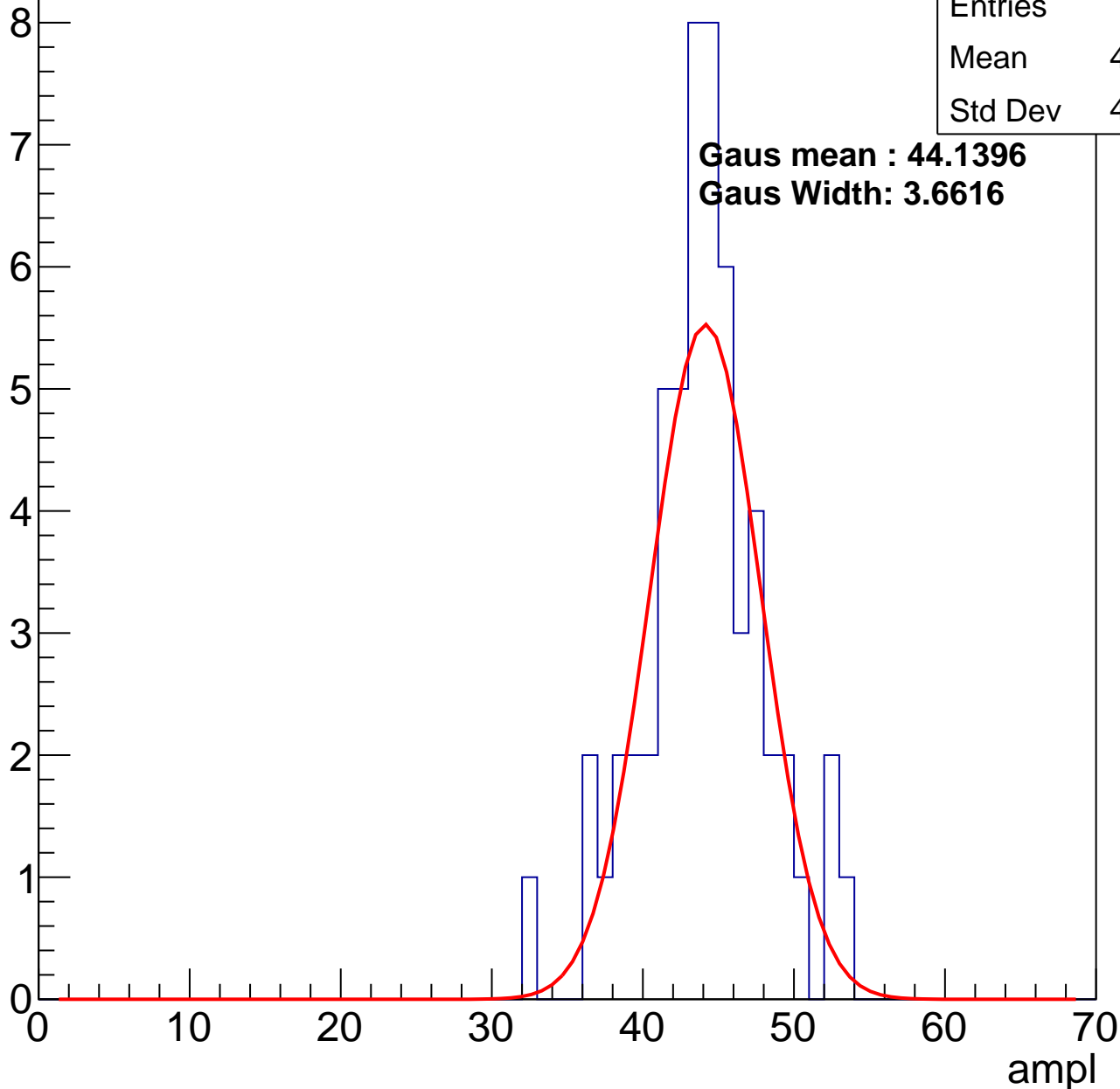
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	57
Mean	43.56
Std Dev	4.013

**Gaus mean : 44.1396**

**Gaus Width: 3.6616**

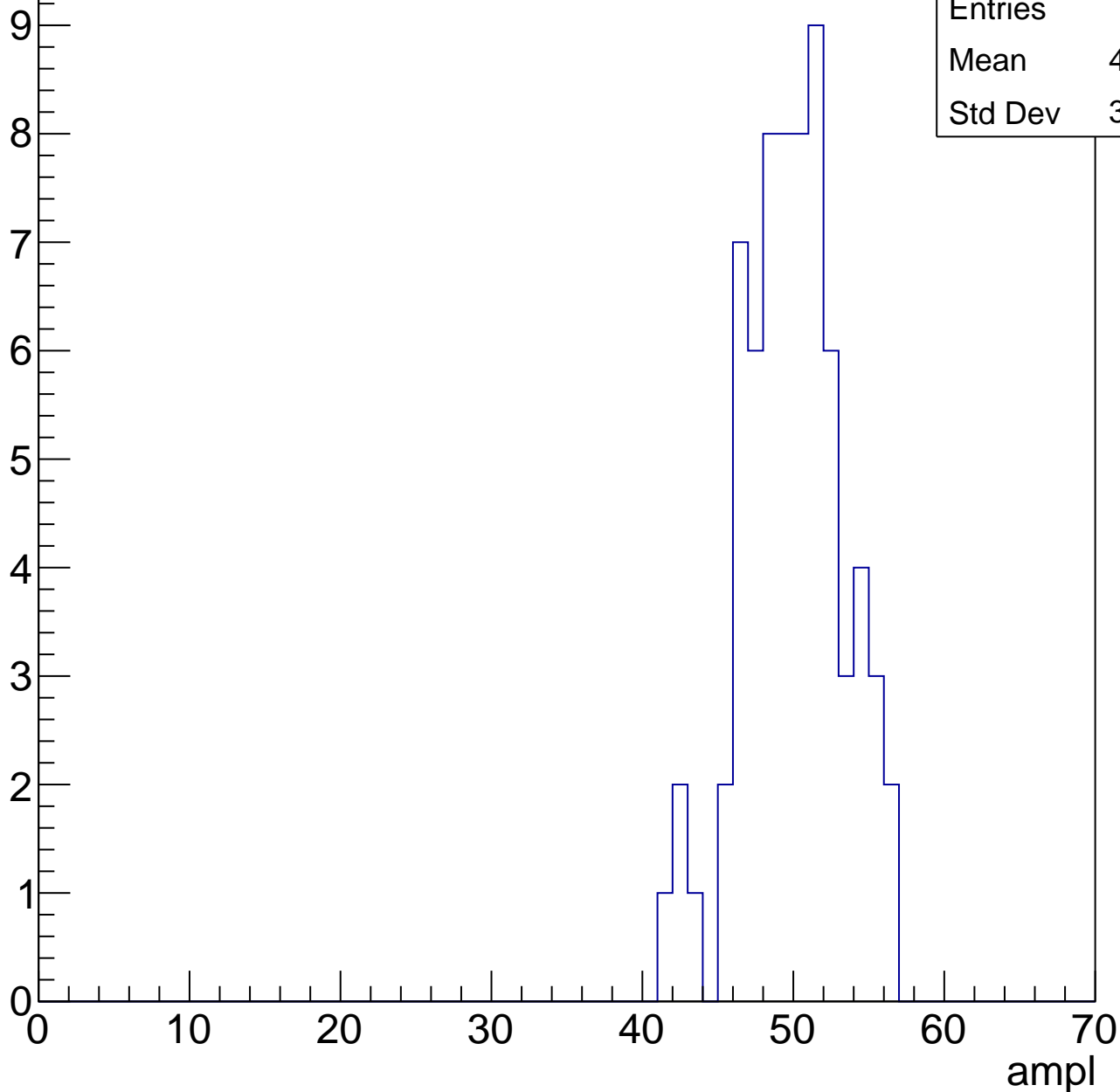


# B1L003S, U18-ch69, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

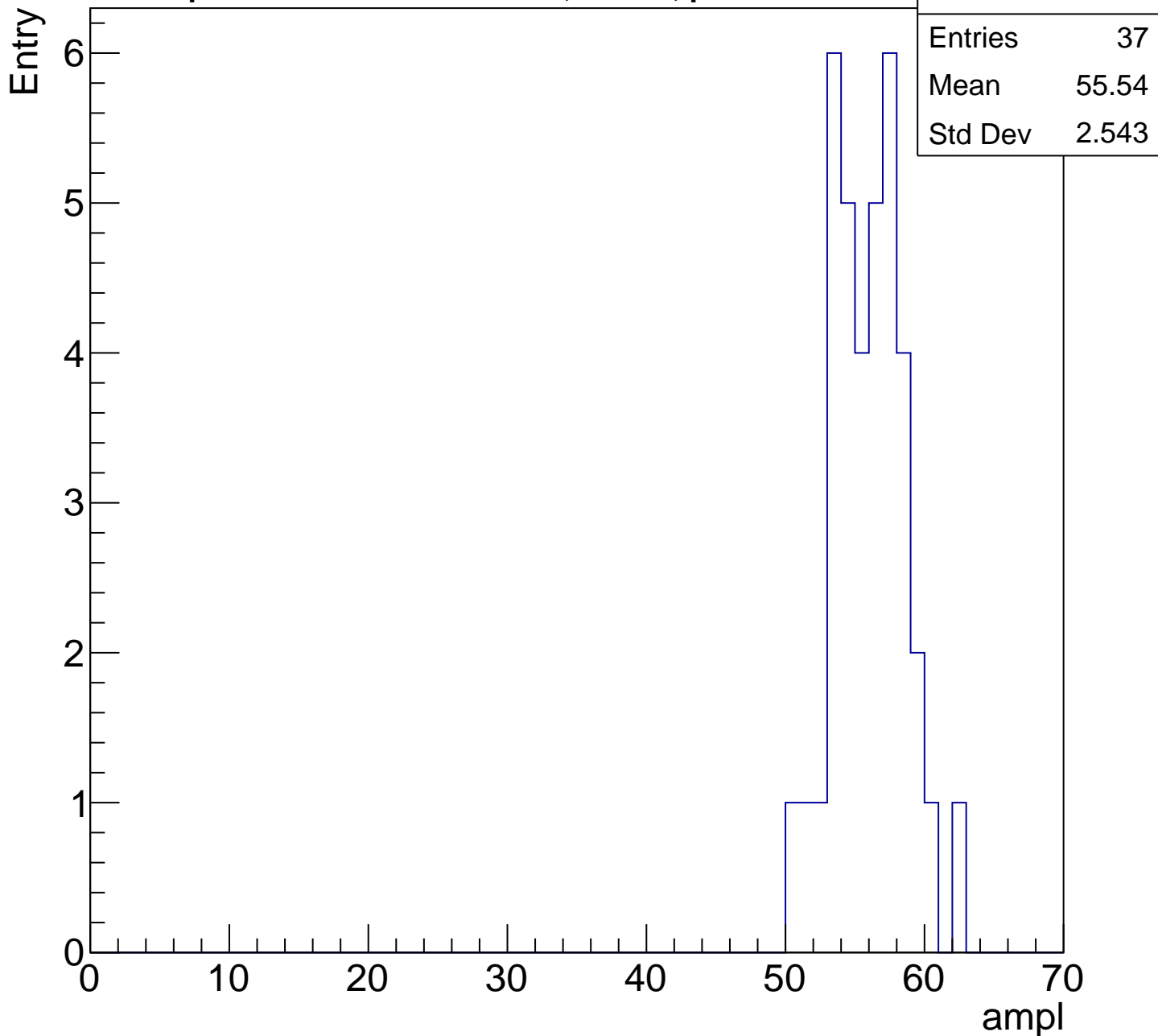
Entry

Entries	70
Mean	49.44
Std Dev	3.302



# B1L003S, U18-ch69, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2



# B1L003S, U18-ch69, adc5

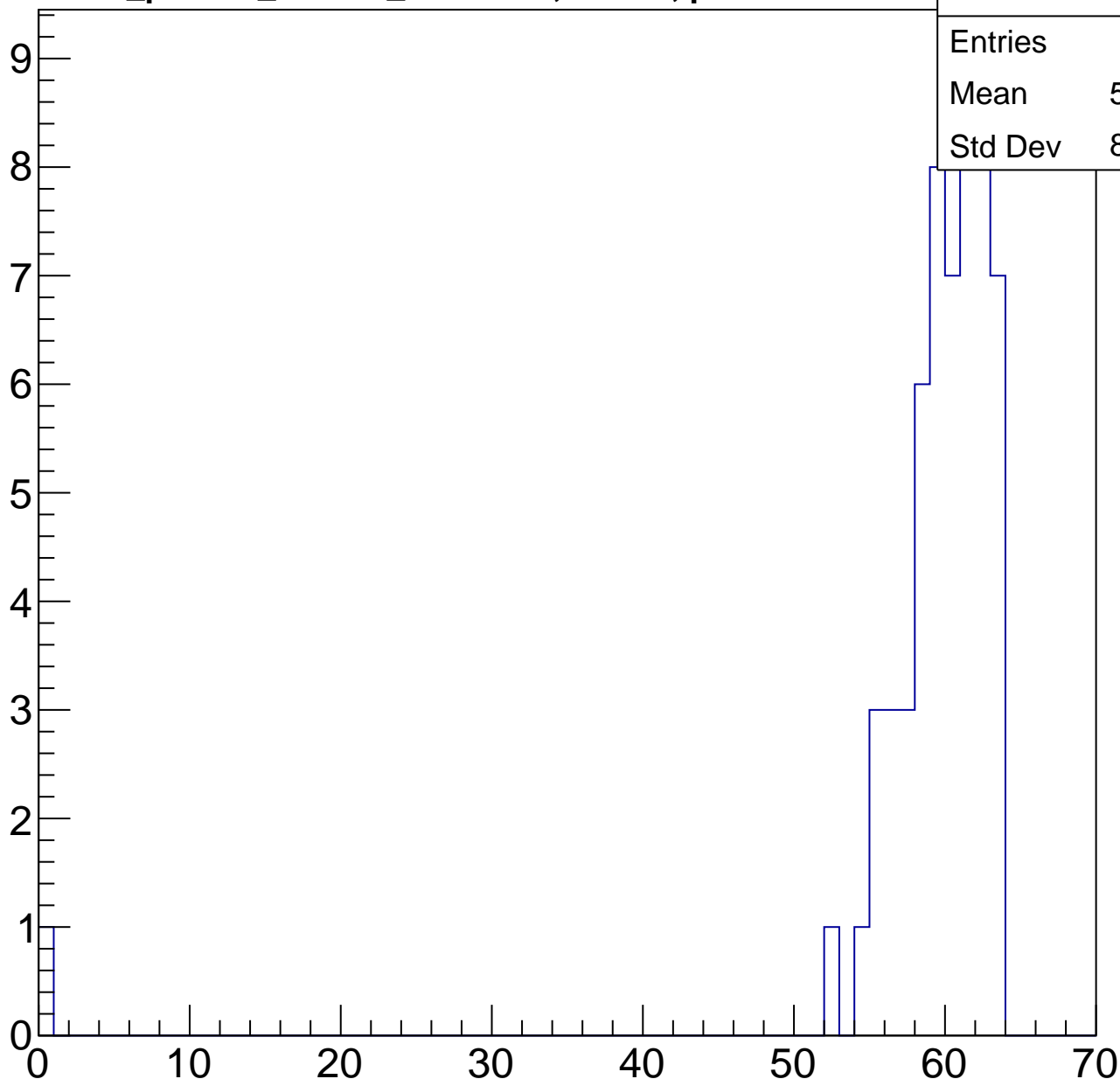
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	58
Mean	58.59
Std Dev	8.173

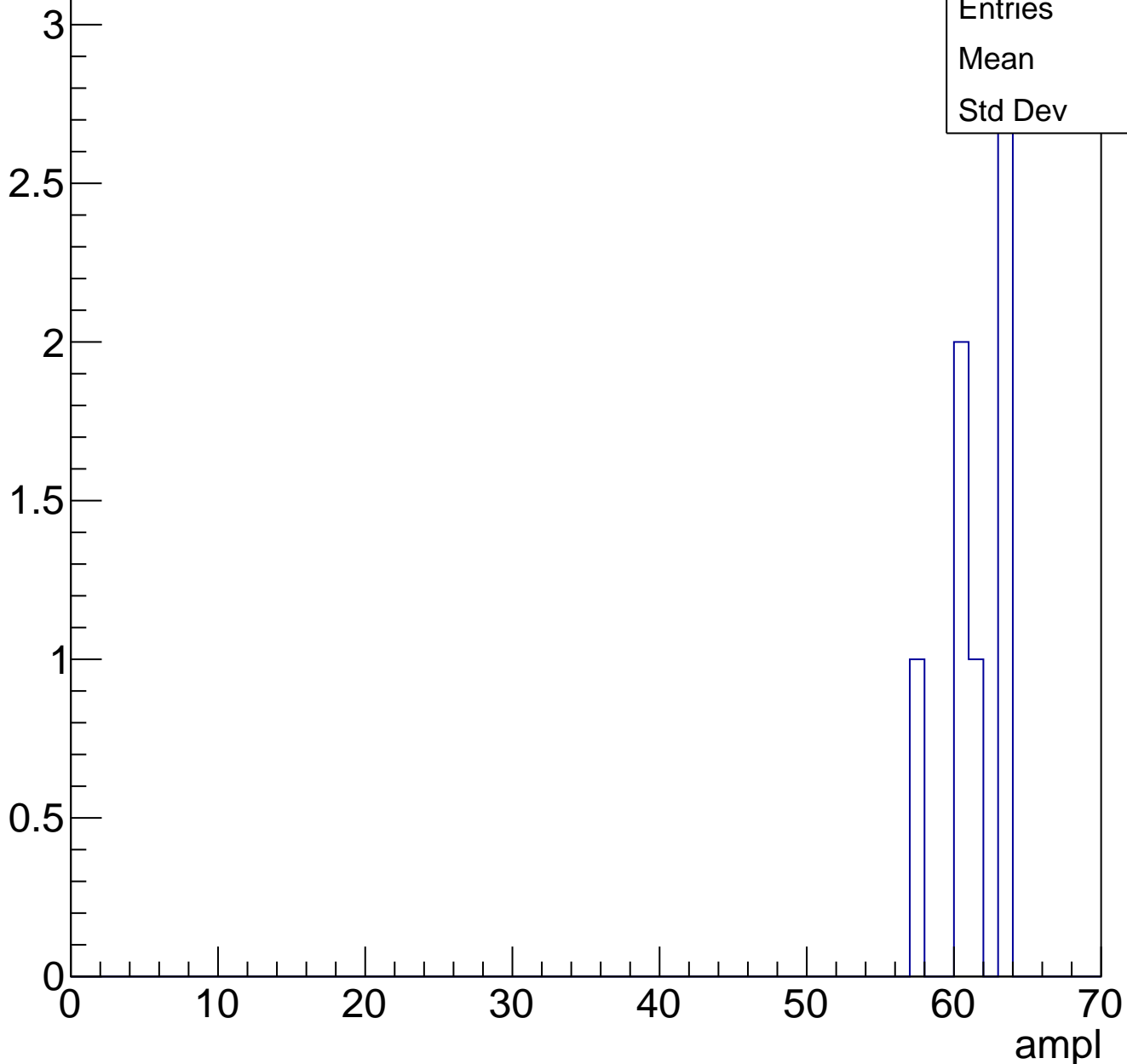
ampl



# B1L003S, U18-ch69, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U18-ch69, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch70, adc0

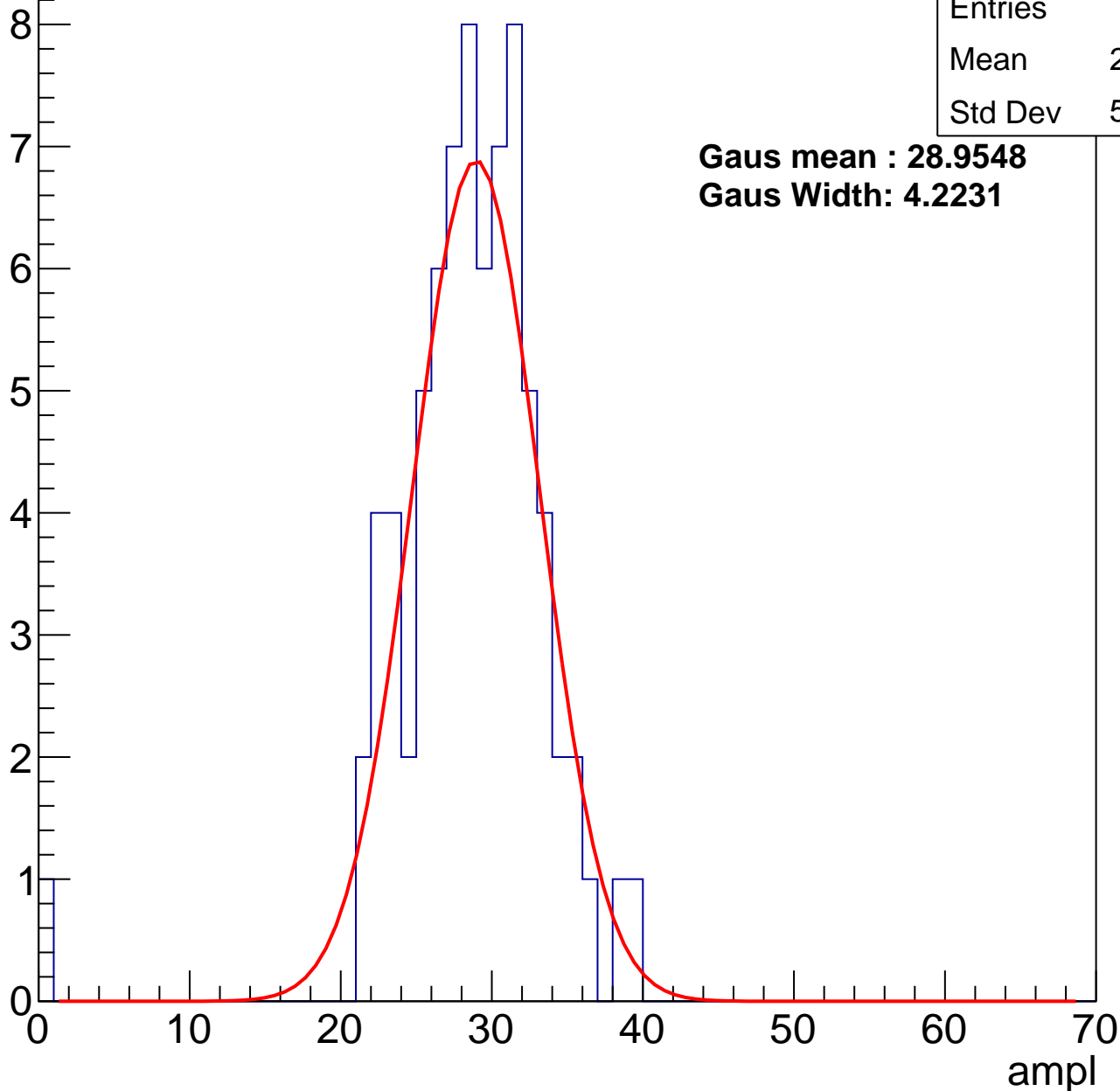
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	76
Mean	28.14
Std Dev	5.096

**Gaus mean : 28.9548**

**Gaus Width: 4.2231**



# B1L003S, U18-ch70, adc1

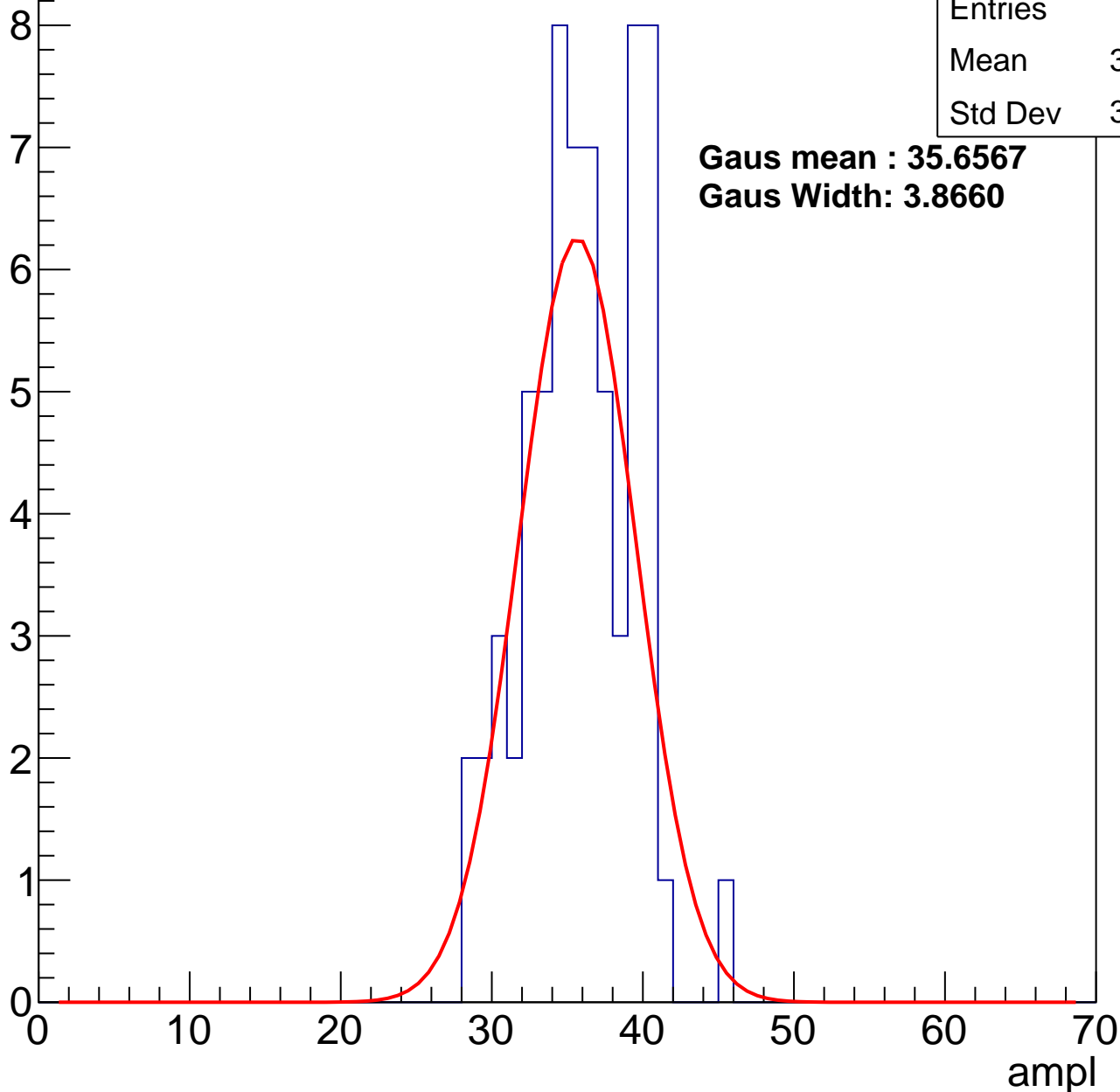
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	67
Mean	35.48
Std Dev	3.568

**Gaus mean : 35.6567**

**Gaus Width: 3.8660**



# B1L003S, U18-ch70, adc2

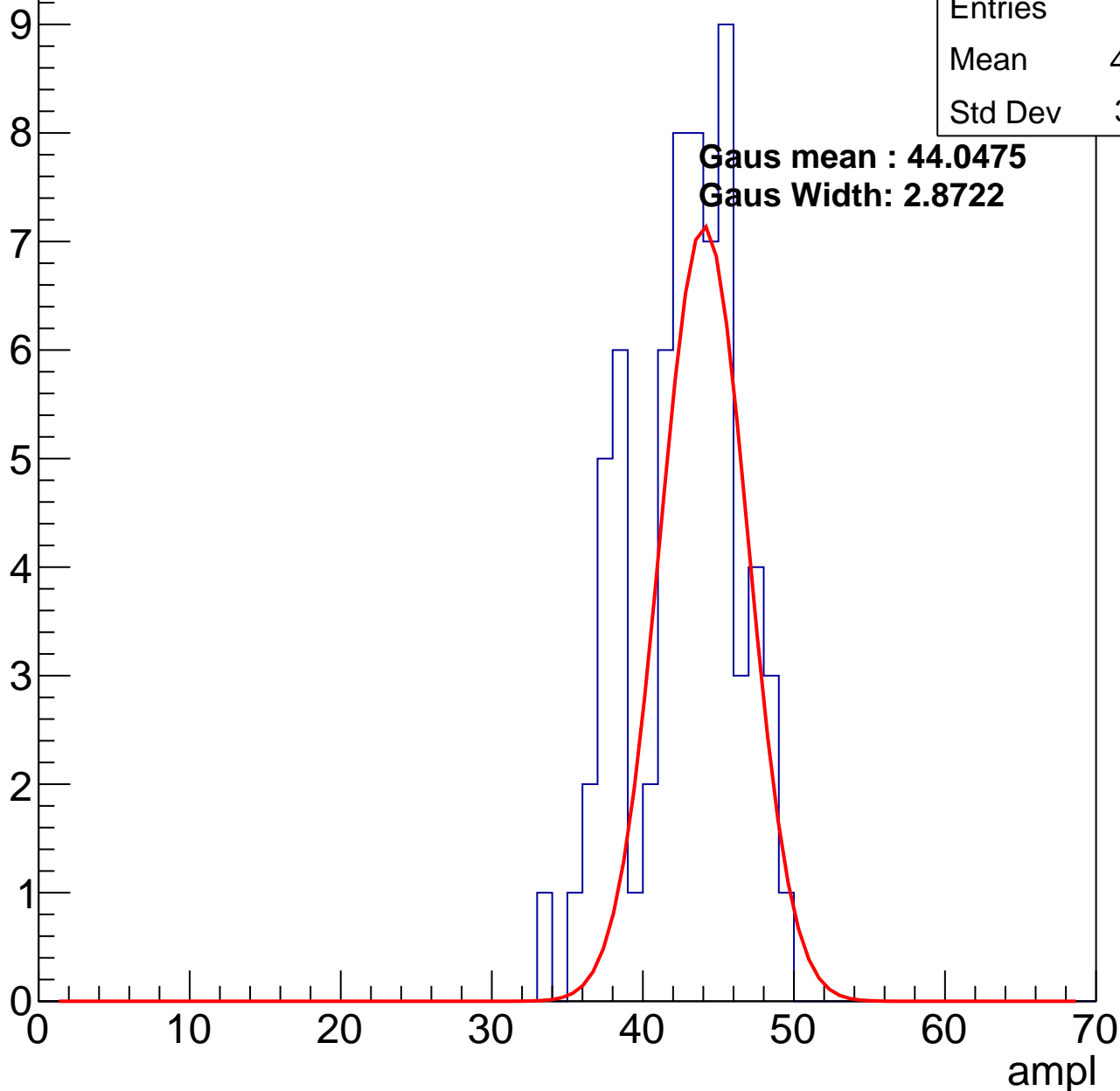
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	67
Mean	42.24
Std Dev	3.591

**Gaus mean : 44.0475**

**Gaus Width: 2.8722**

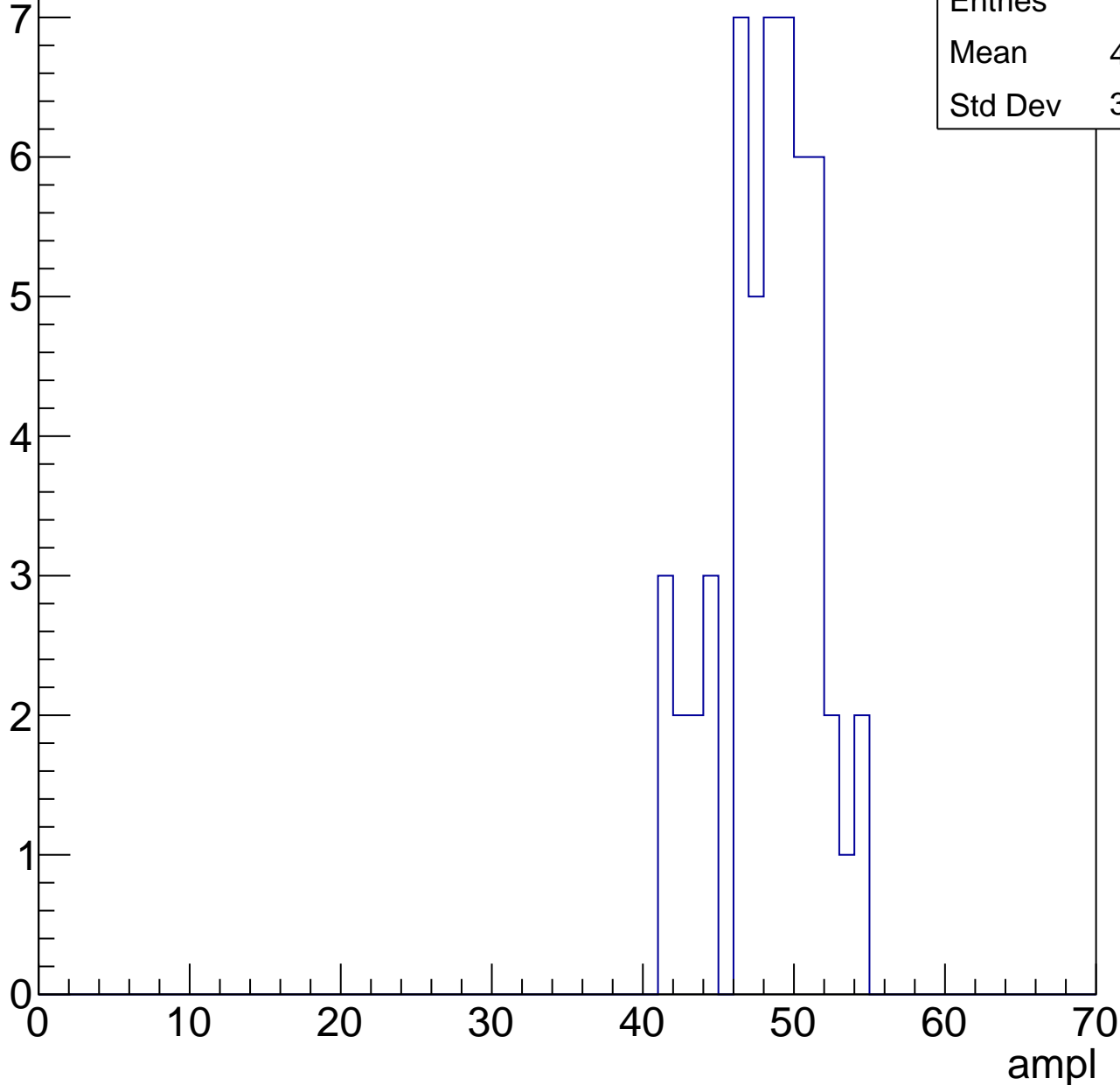


# B1L003S, U18-ch70, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

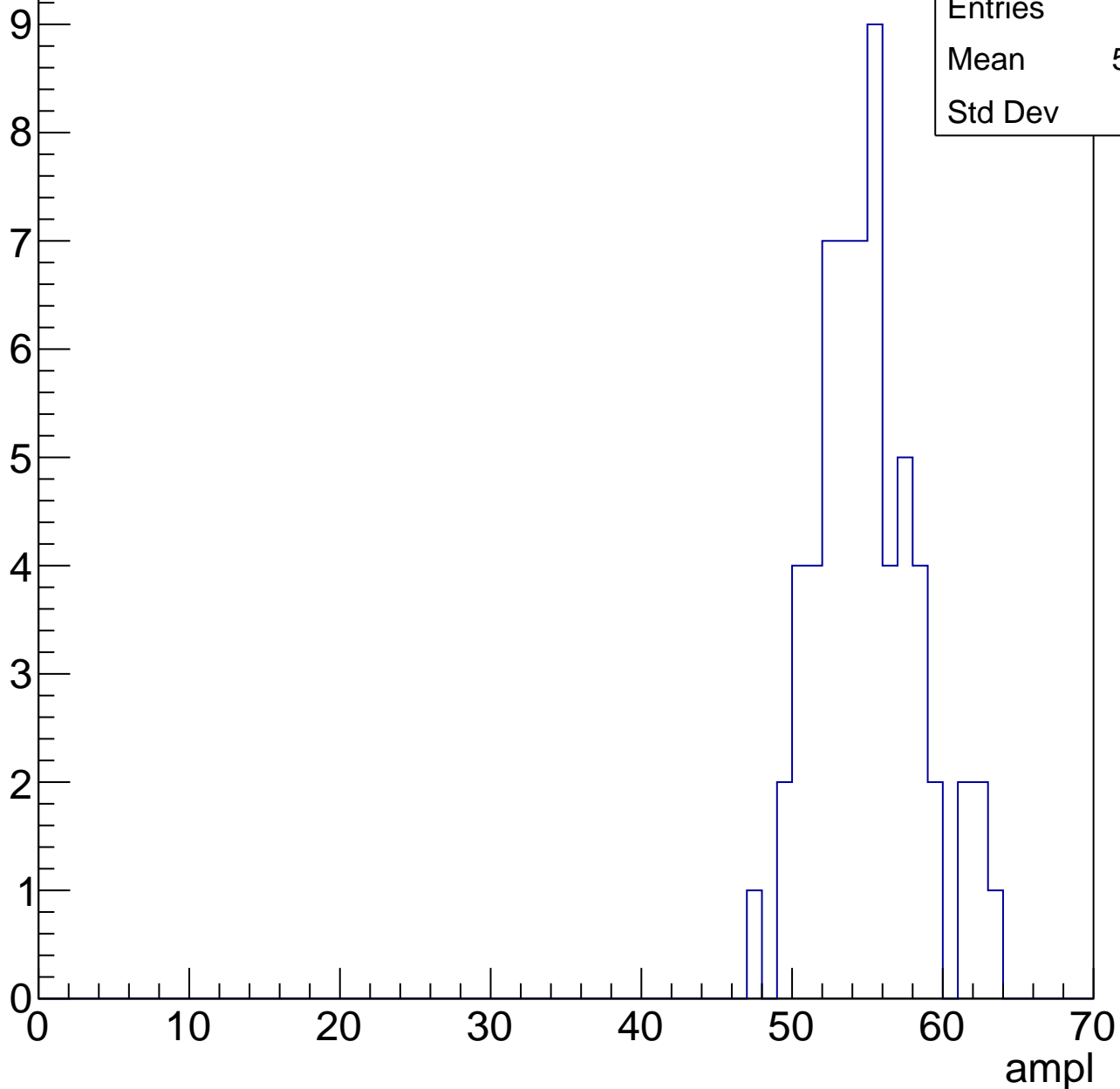
Entries	53
Mean	47.77
Std Dev	3.254



# B1L003S, U18-ch70, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U18-ch70, adc5

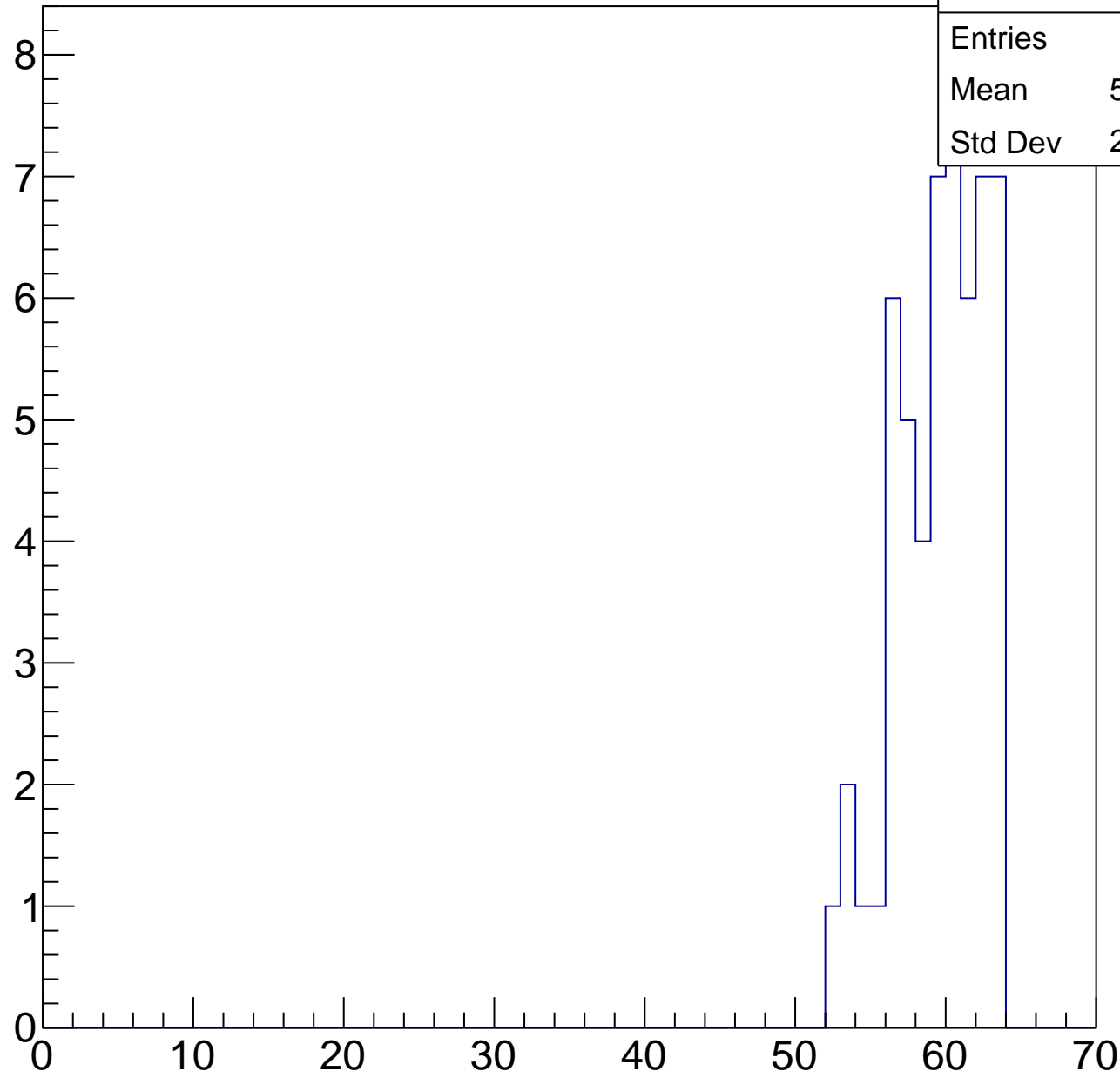
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	55
Mean	59.16
Std Dev	2.846

ampl



# B1L003S, U18-ch70, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	11
Mean	55
Std Dev	17.47

ampl

0 10 20 30 40 50 60 70



# B1L003S, U18-ch70, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U18-ch71, adc0

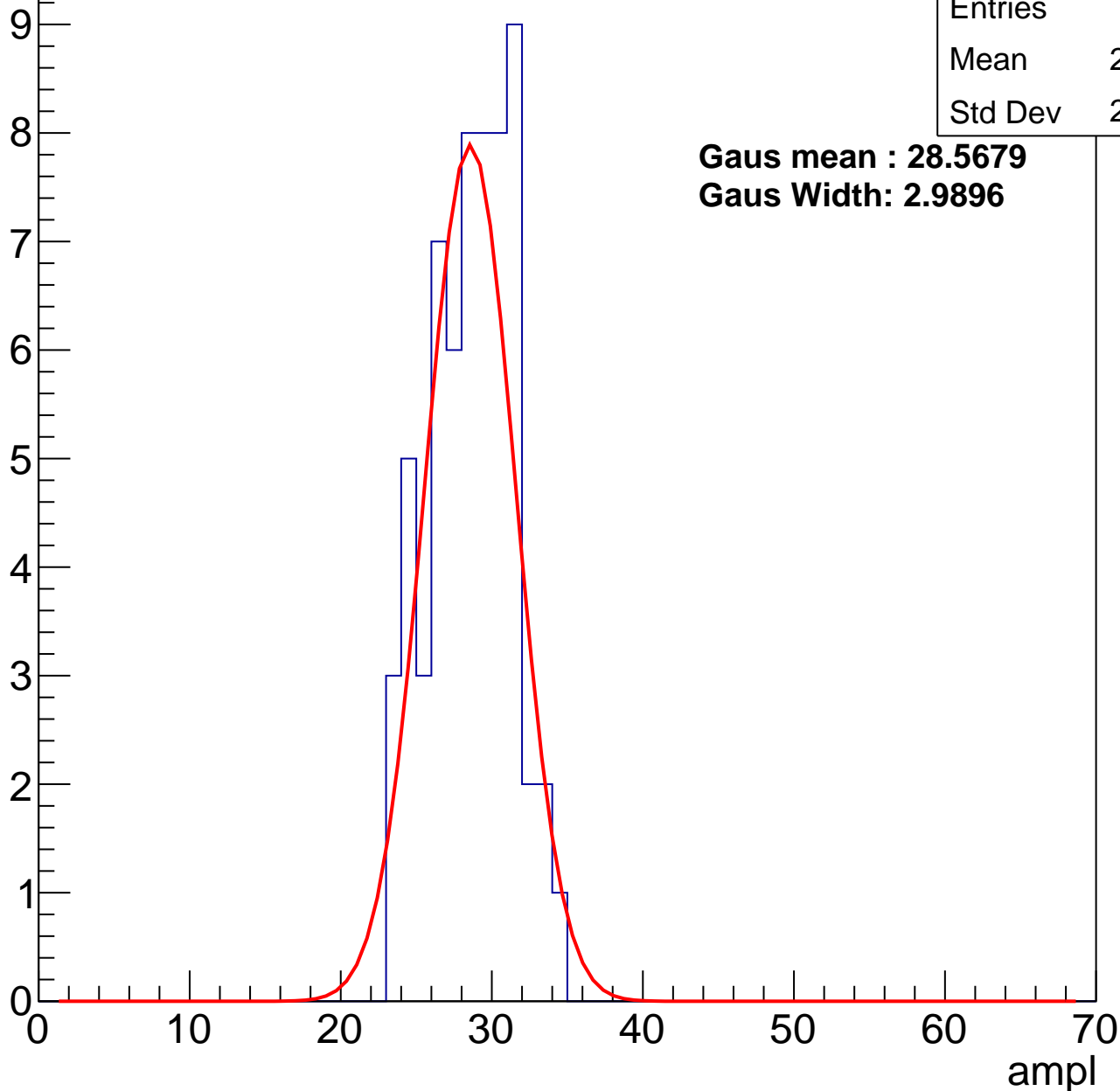
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	62
Mean	28.18
Std Dev	2.703

**Gaus mean : 28.5679**

**Gaus Width: 2.9896**



# B1L003S, U18-ch71, adc1

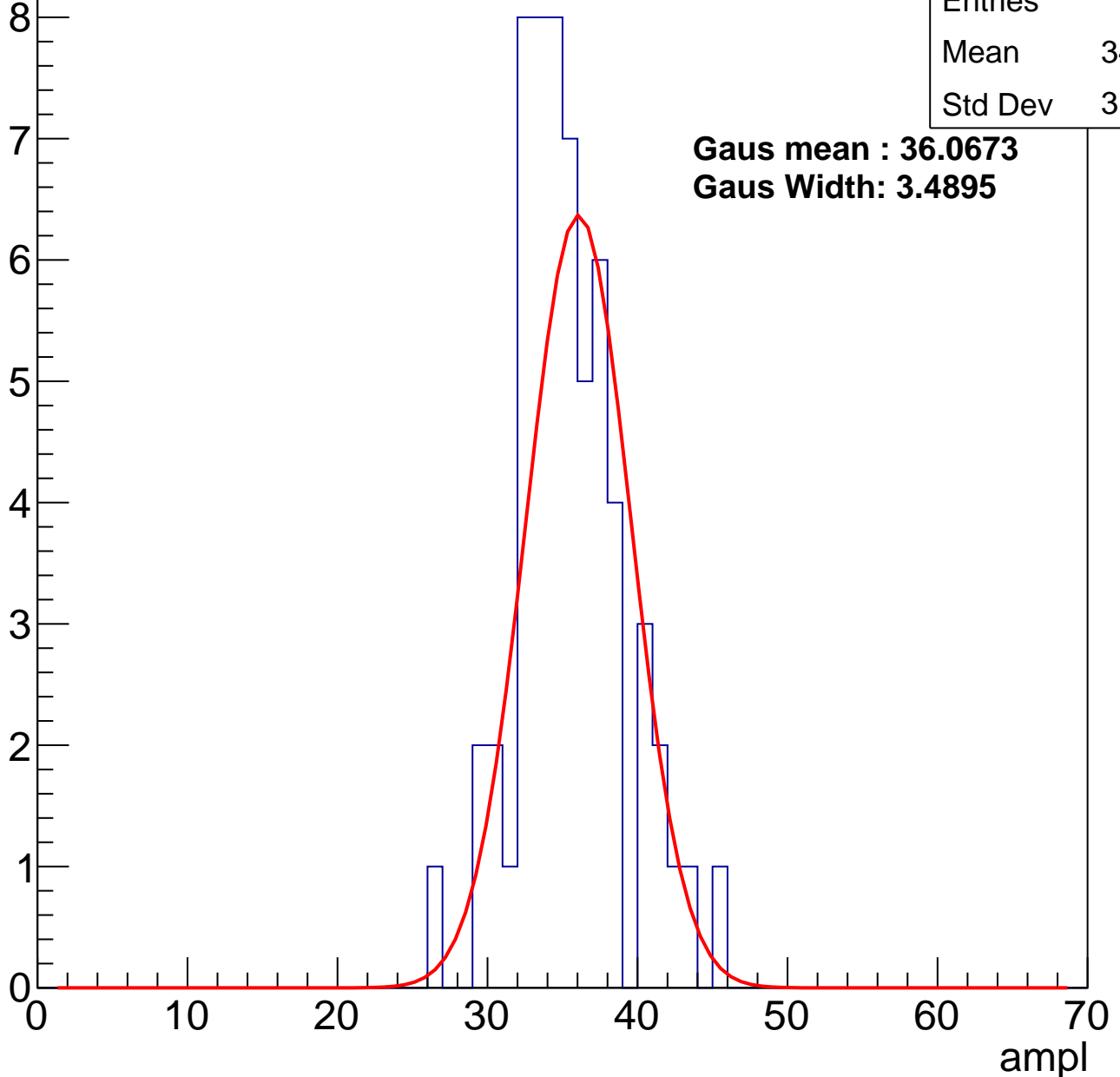
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	60
Mean	34.97
Std Dev	3.549

**Gaus mean : 36.0673**

**Gaus Width: 3.4895**



# B1L003S, U18-ch71, adc2

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	77
Mean	40.88
Std Dev	3.851

**Gaus mean : 41.5288**

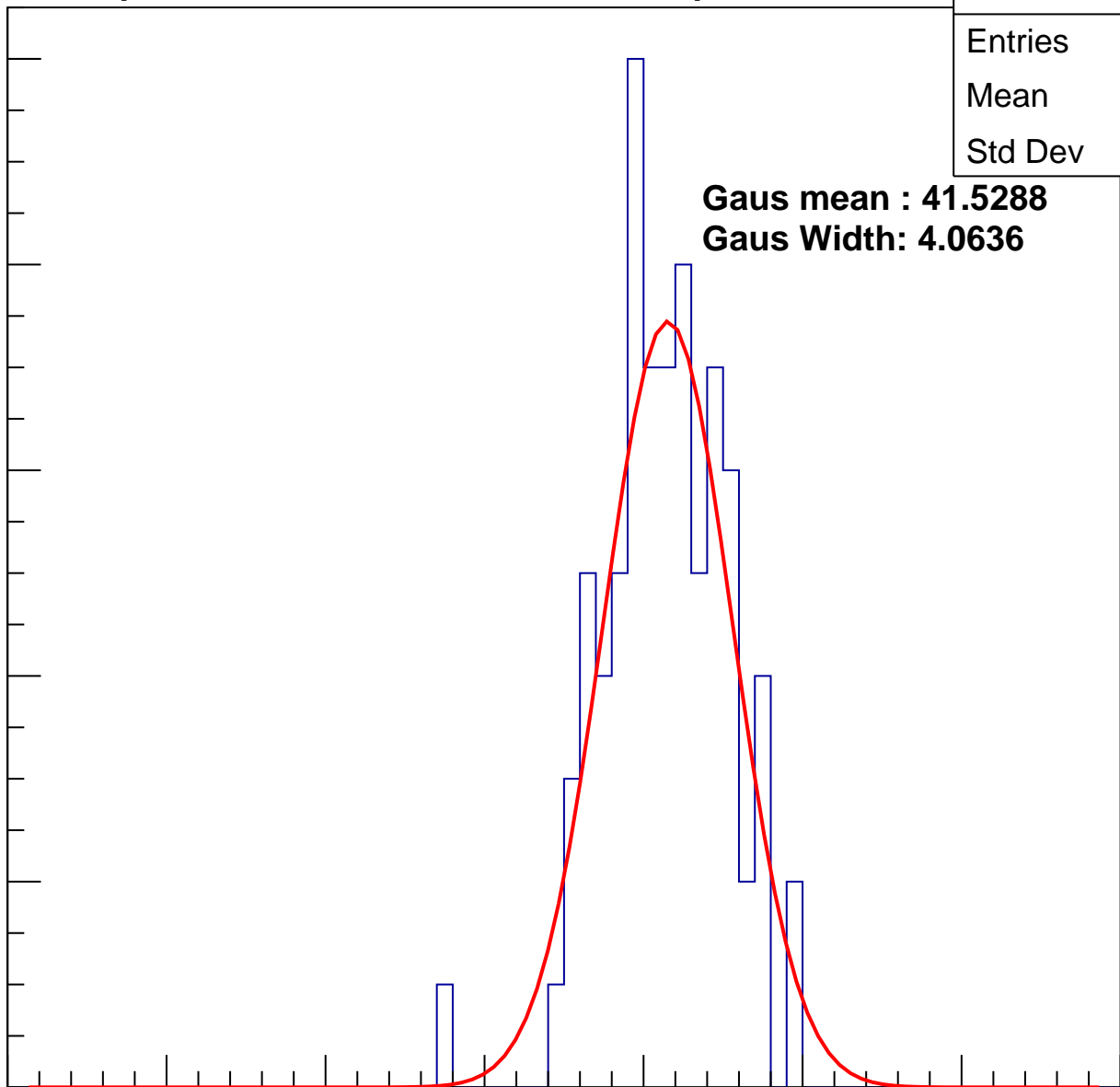
**Gaus Width: 4.0636**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L003S, U18-ch71, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

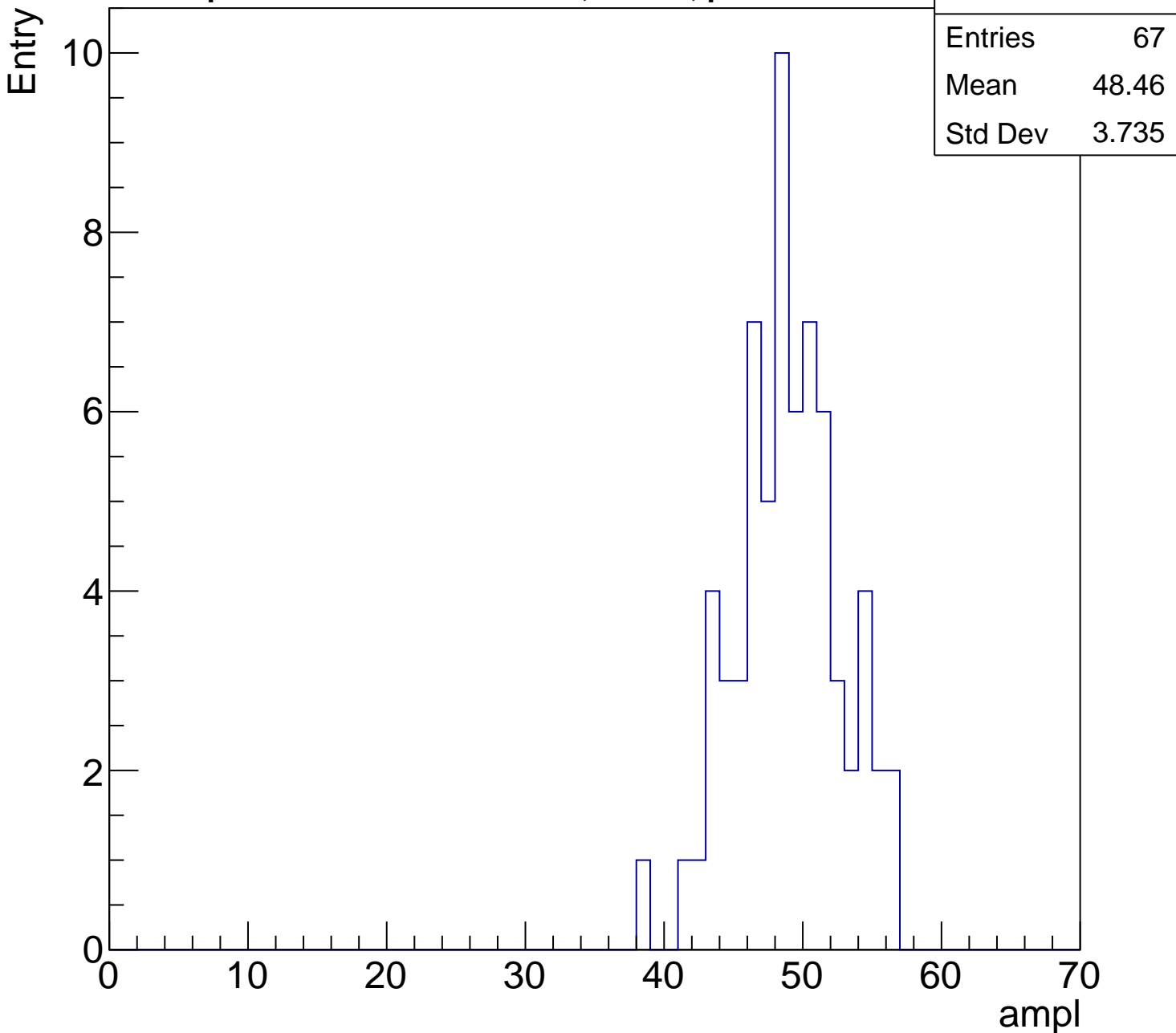
Entries	67
Mean	48.46
Std Dev	3.735

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

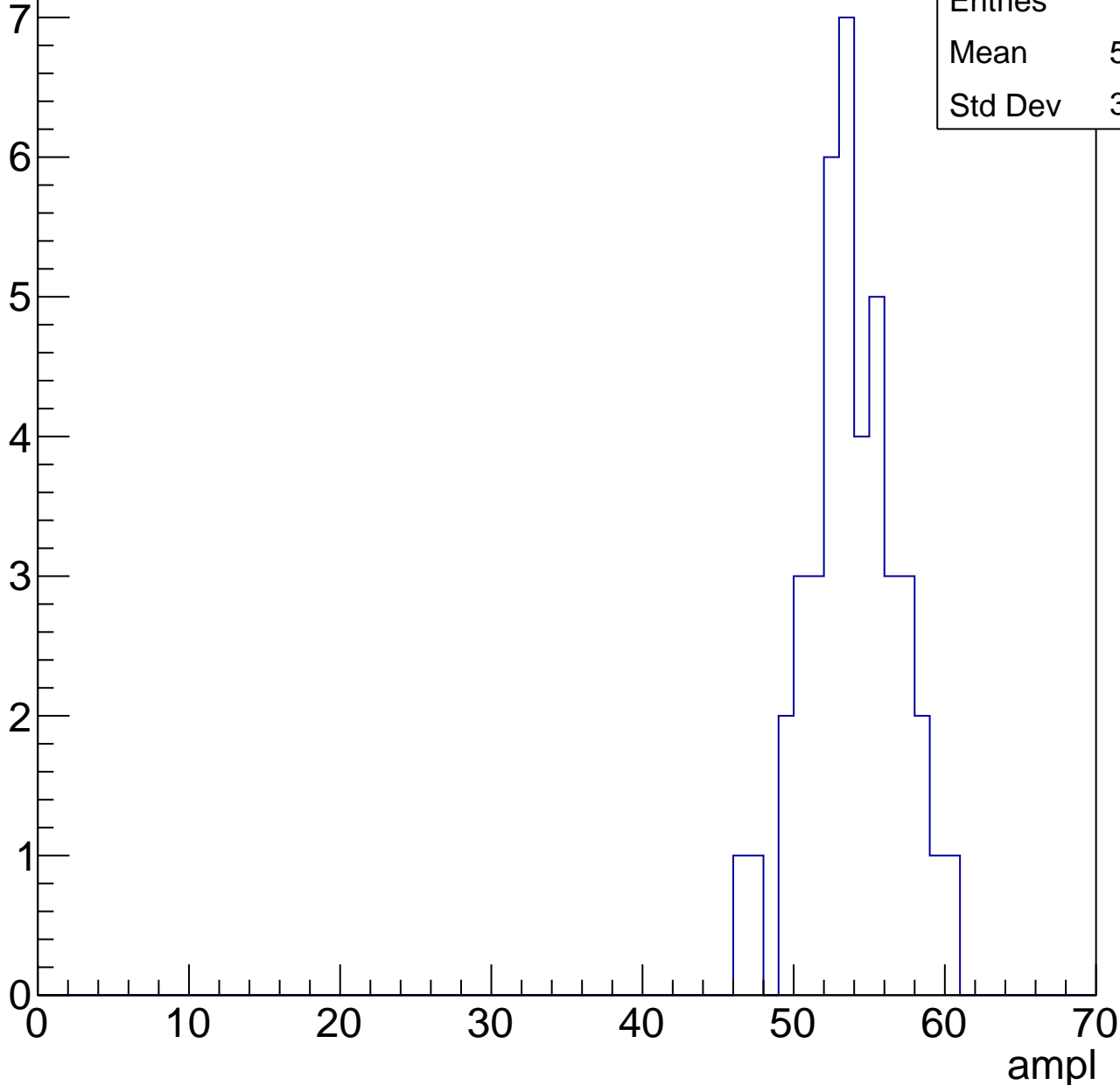


# B1L003S, U18-ch71, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

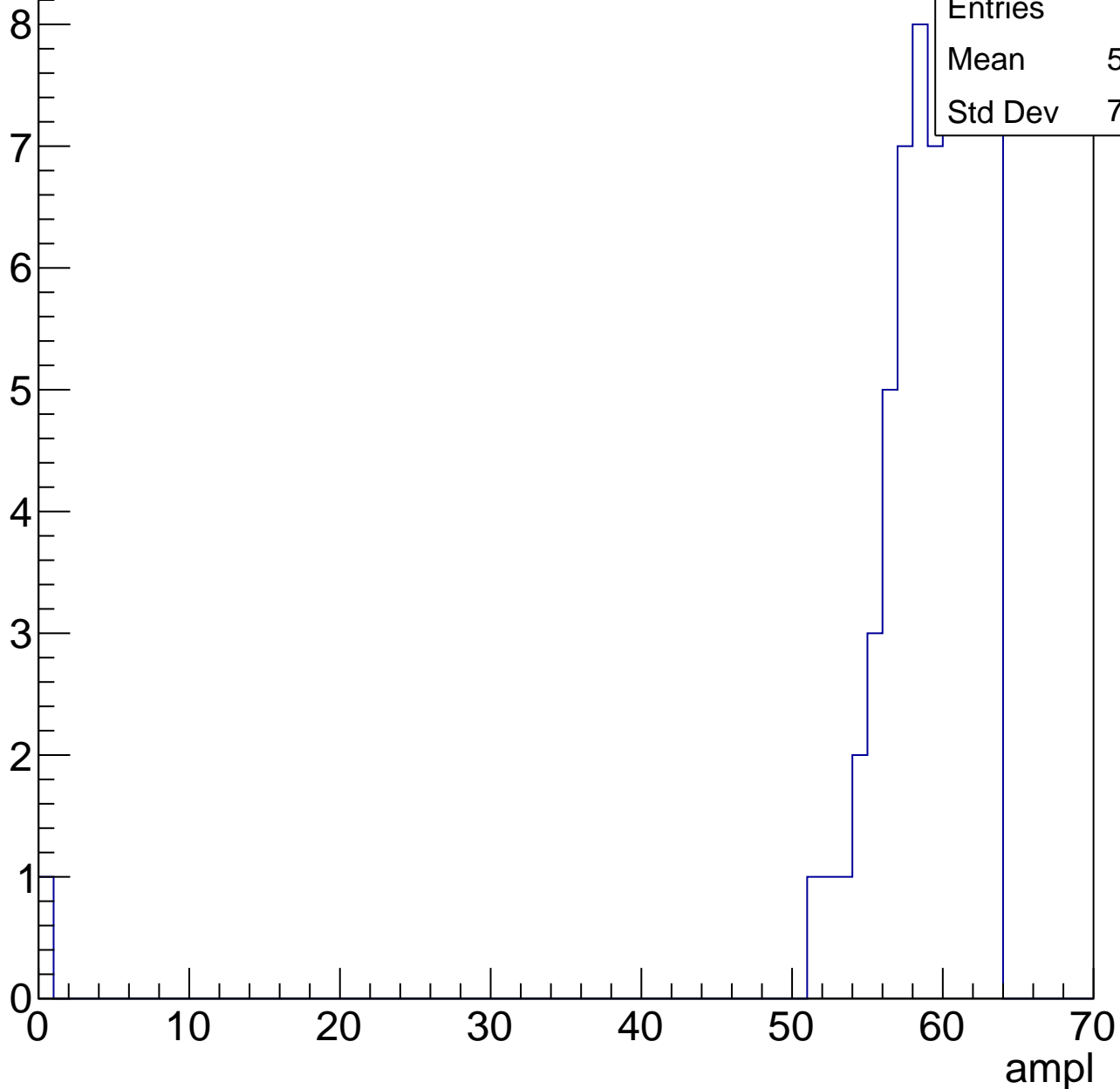
Entries	42
Mean	53.38
Std Dev	3.047



# B1L003S, U18-ch71, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U18-ch71, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	9
Mean	61.11
Std Dev	1.449

0 10 20 30 40 50 60 70

ampl



# B1L003S, U18-ch71, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

1  
0.8  
0.6  
0.4  
0.2  
0

Entries	1
Mean	22
Std Dev	0

ampl

# B1L003S, U18-ch72, adc0

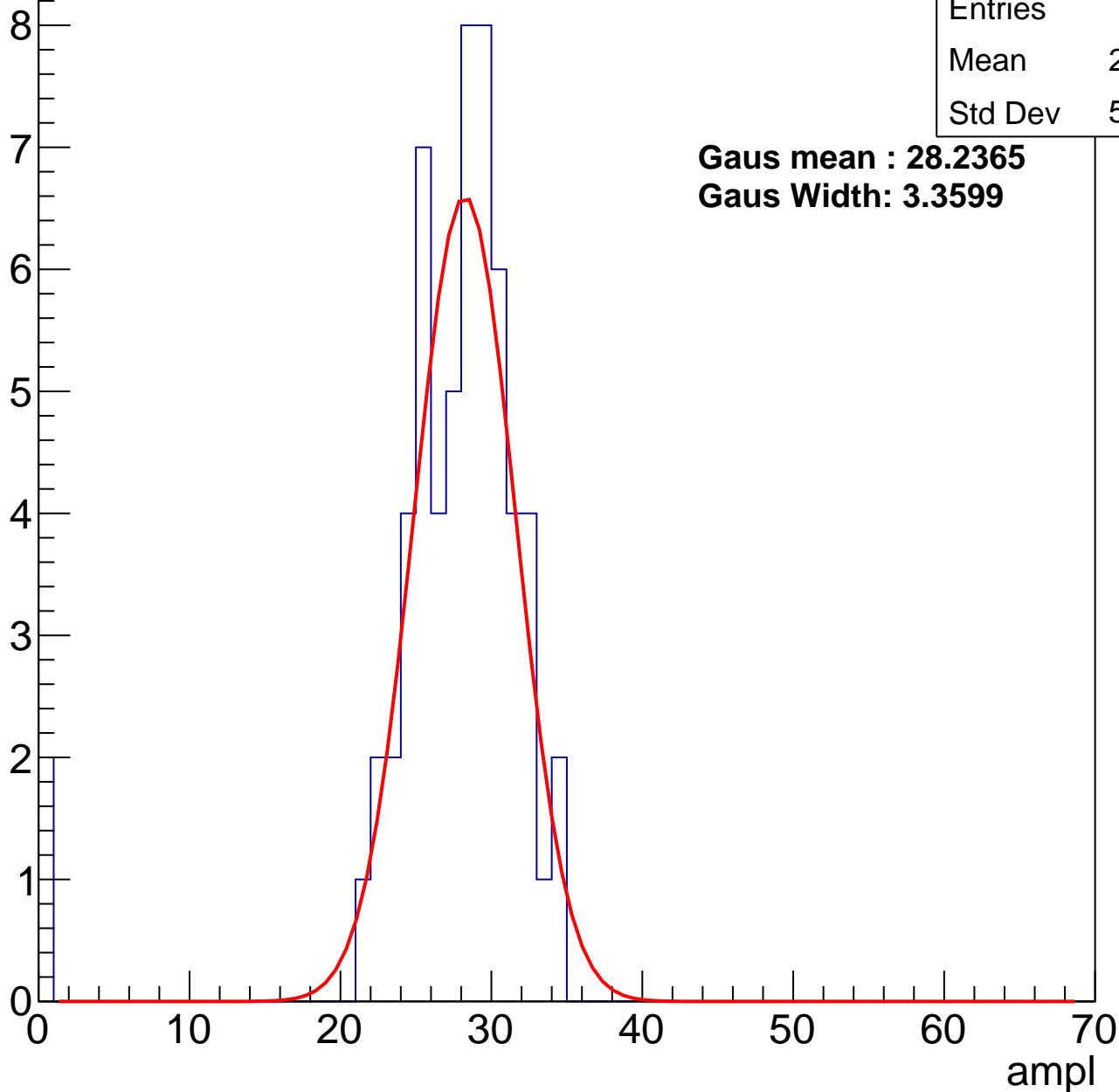
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	60
Mean	26.83
Std Dev	5.823

**Gaus mean : 28.2365**

**Gaus Width: 3.3599**



# B1L003S, U18-ch72, adc1

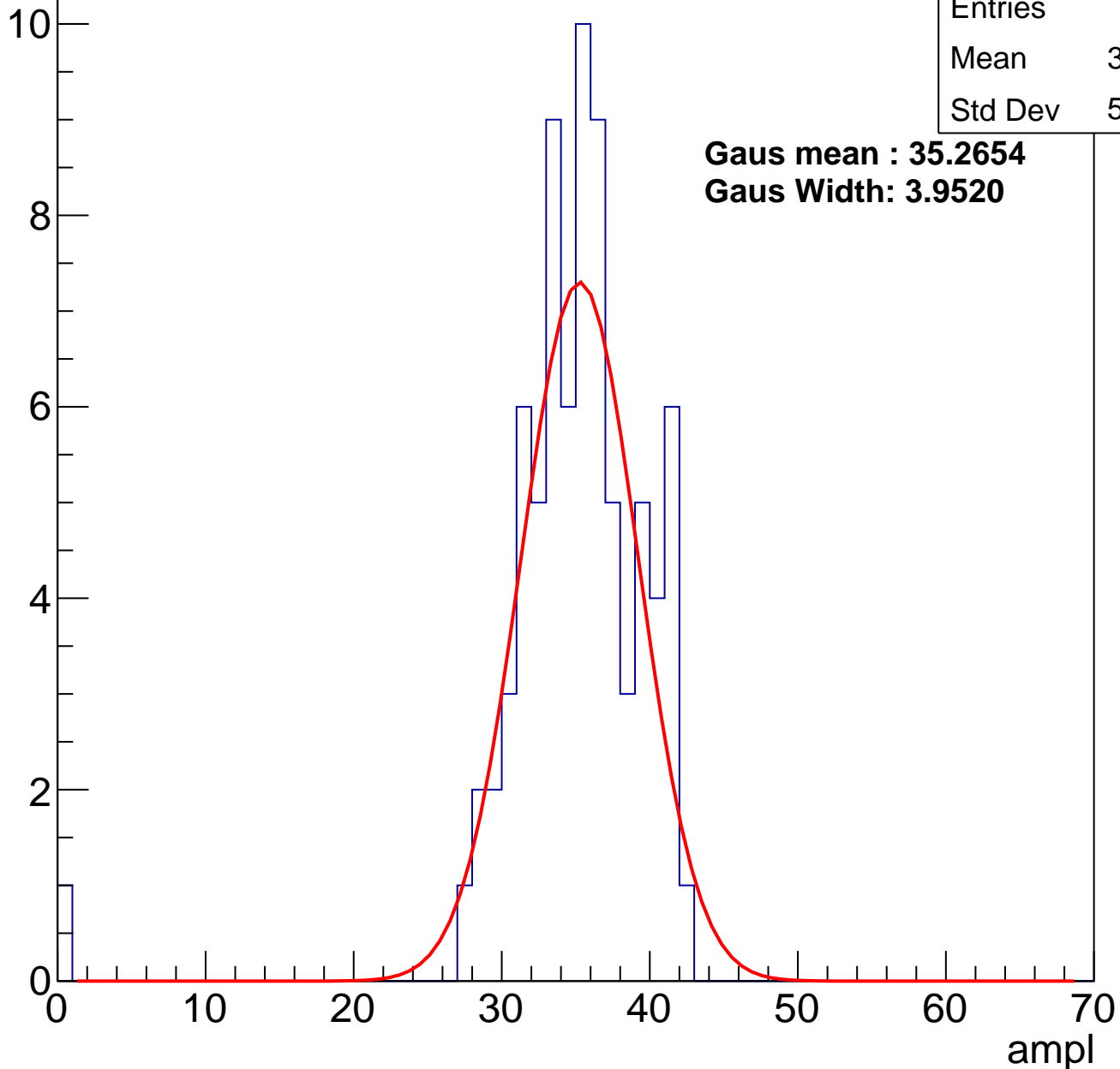
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	78
Mean	34.54
Std Dev	5.313

**Gaus mean : 35.2654**

**Gaus Width: 3.9520**

Entry



# B1L003S, U18-ch72, adc2

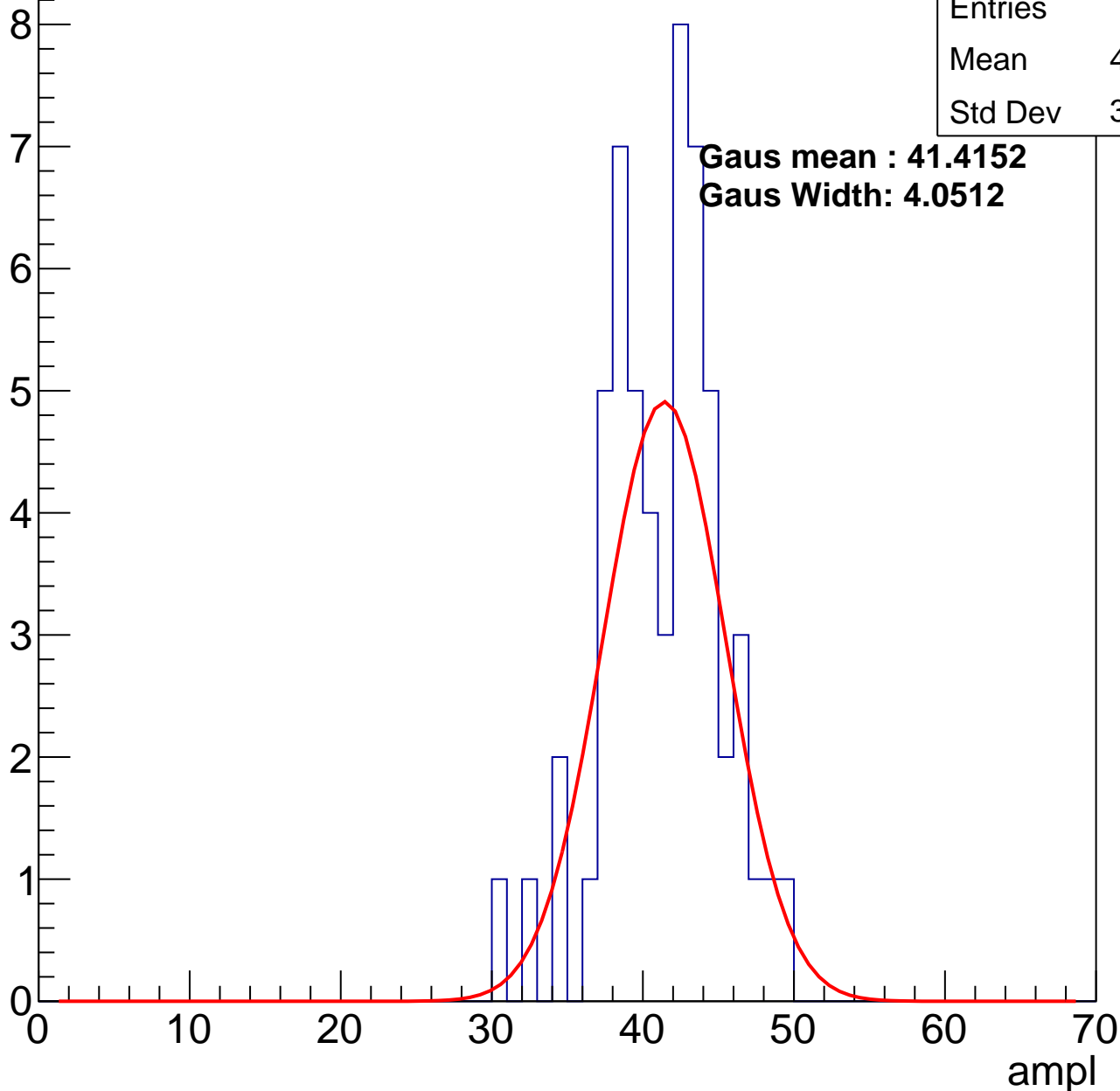
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	57
Mean	40.77
Std Dev	3.807

**Gaus mean : 41.4152**

**Gaus Width: 4.0512**

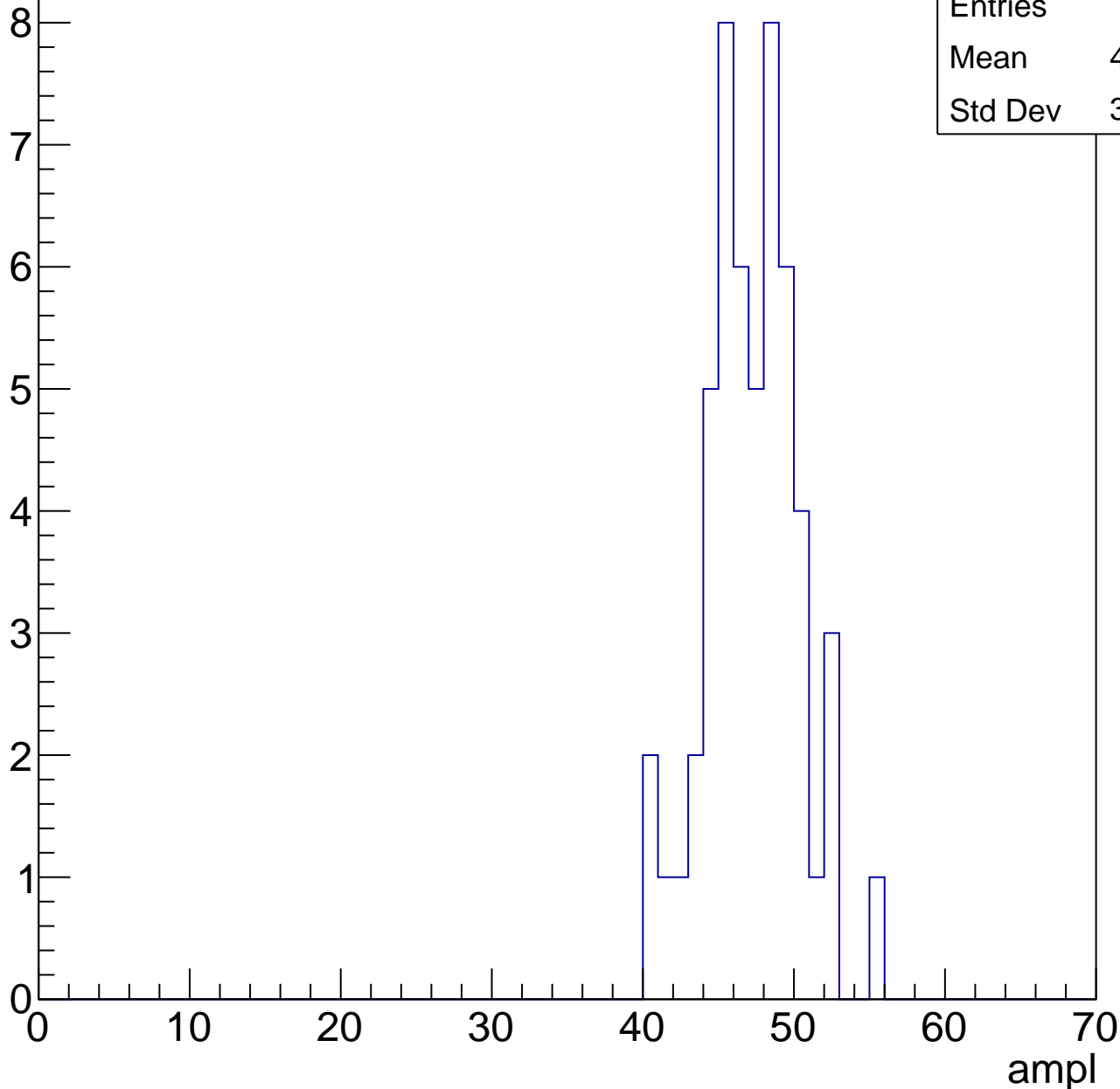


# B1L003S, U18-ch72, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	53
Mean	46.79
Std Dev	3.055

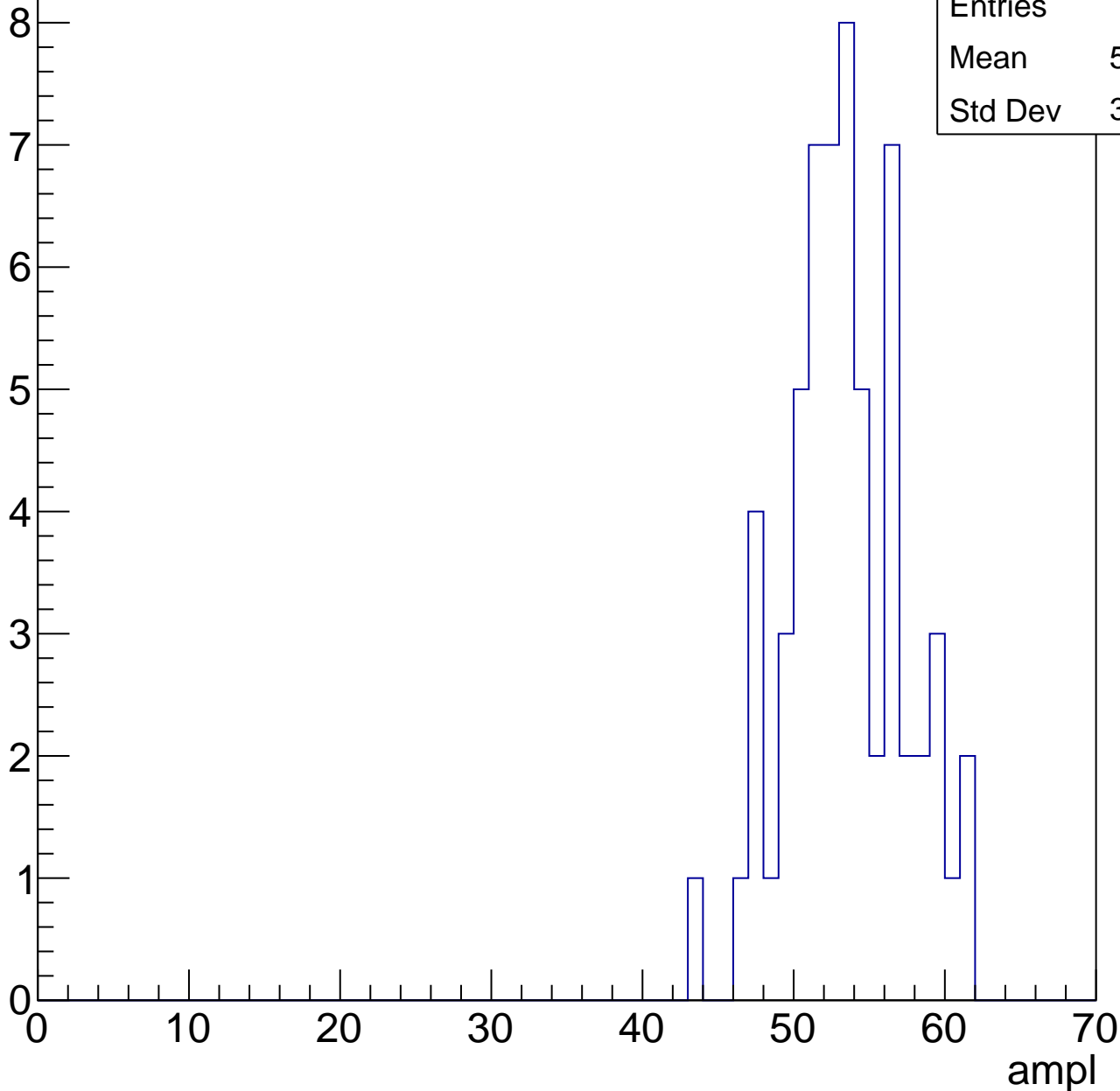


# B1L003S, U18-ch72, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	61
Mean	52.92
Std Dev	3.817

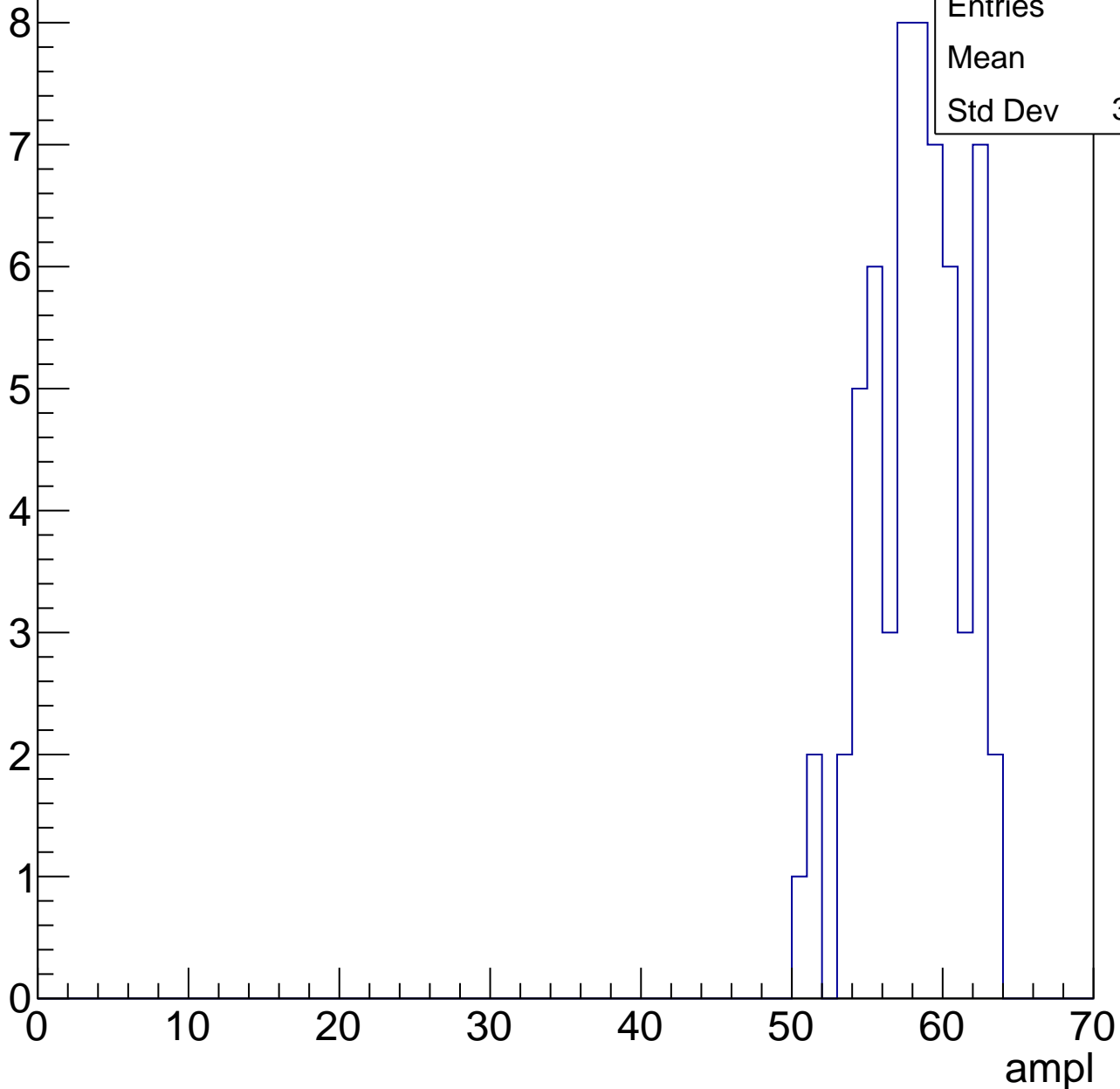


# B1L003S, U18-ch72, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	60
Mean	57.7
Std Dev	3.111

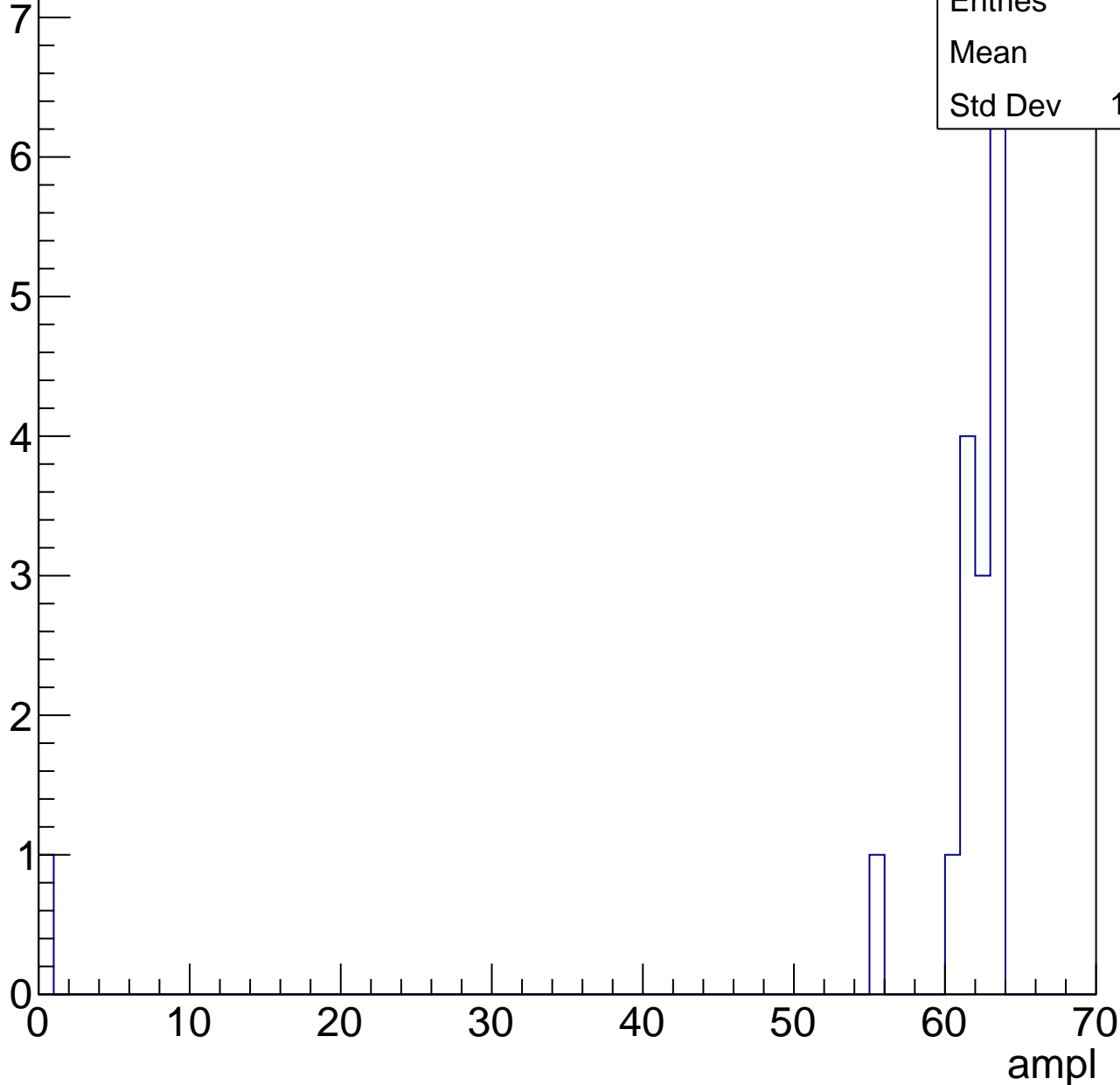


# B1L003S, U18-ch72, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	17
Mean	58
Std Dev	14.62





# B1L003S, U18-ch72, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

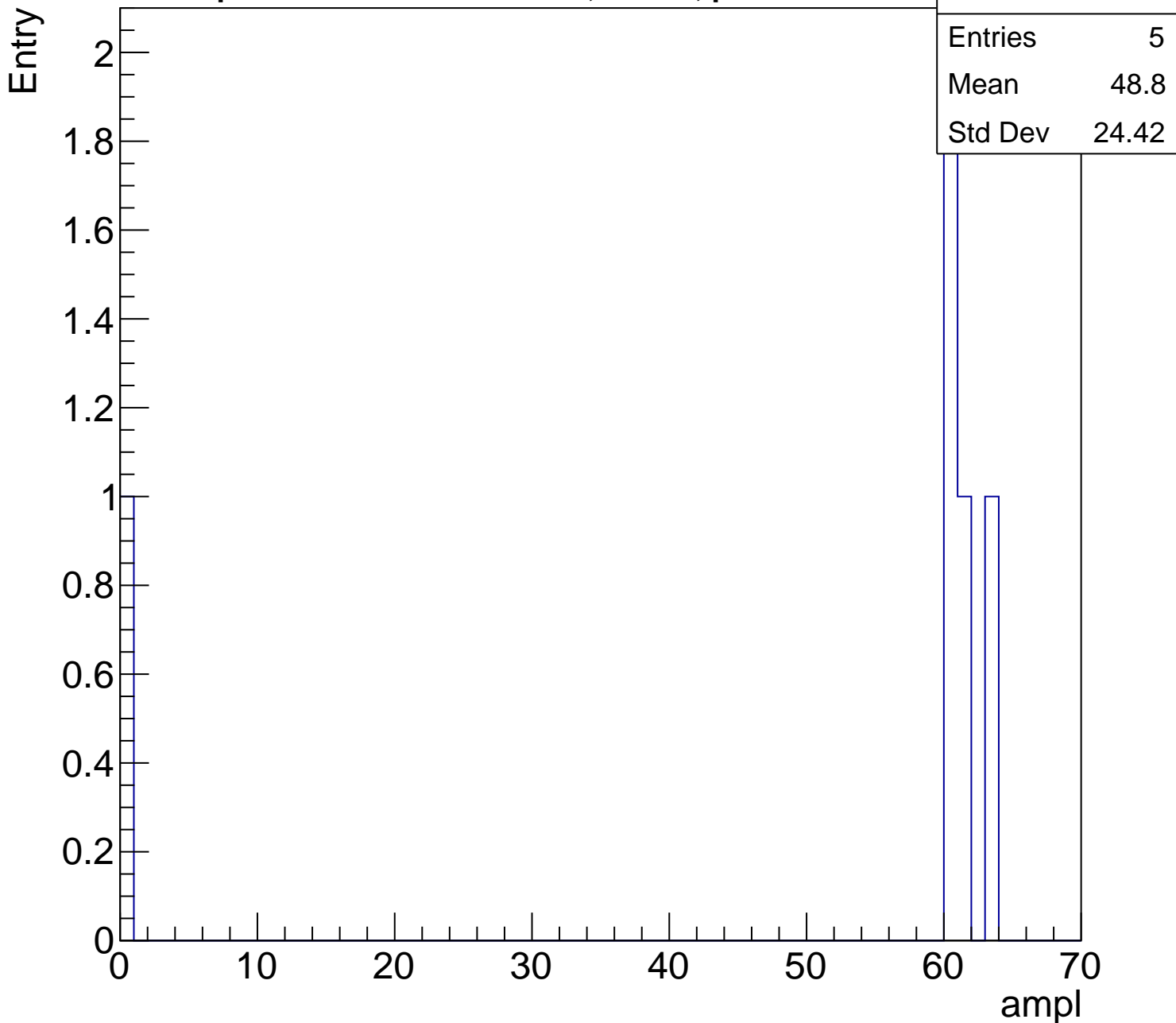
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	5
Mean	48.8
Std Dev	24.42

0 10 20 30 40 50 60 70

ampl



# B1L003S, U18-ch73, adc0

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	68
Mean	29.41
Std Dev	3.566

**Gaus mean : 29.2490**

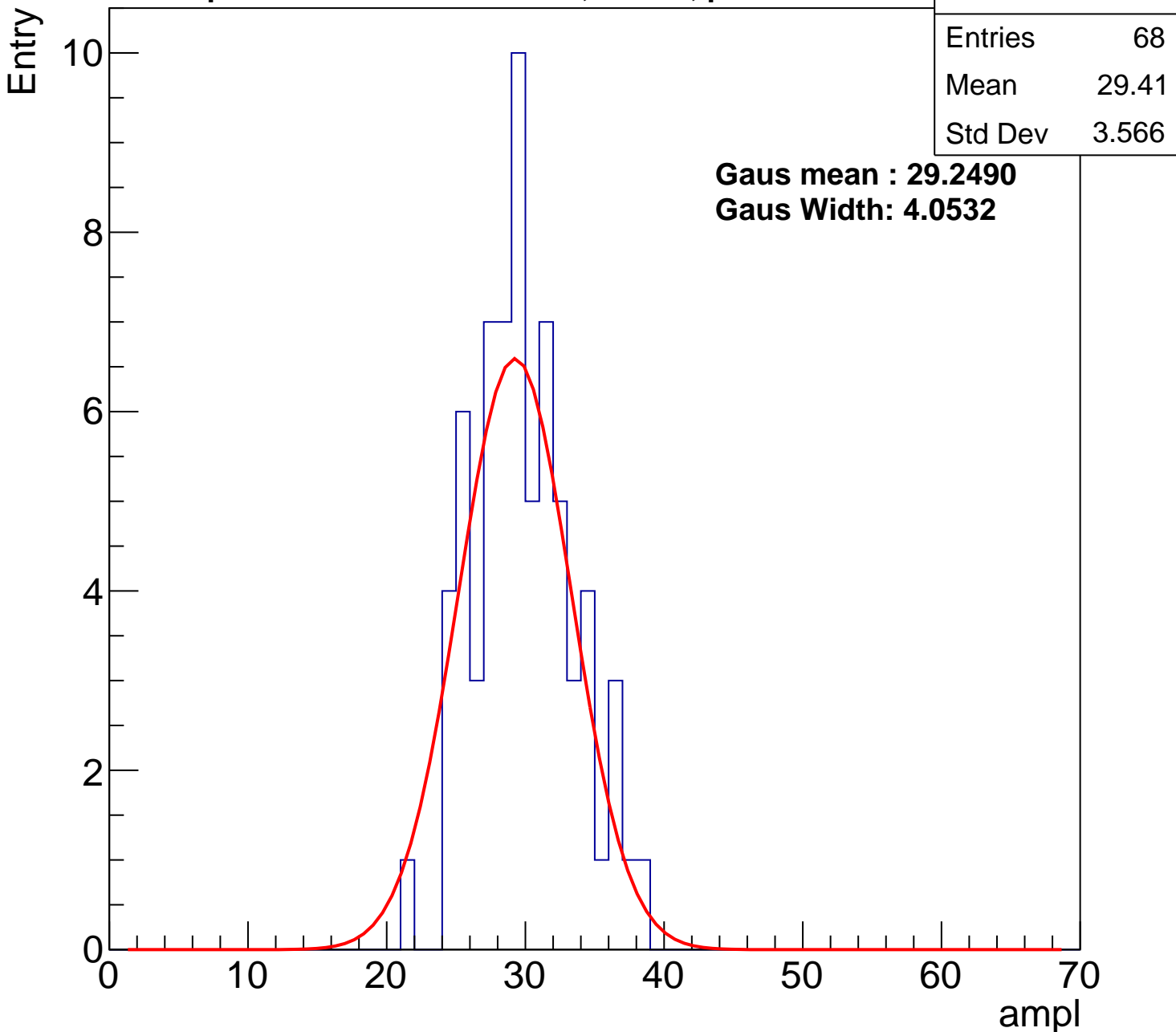
**Gaus Width: 4.0532**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L003S, U18-ch73, adc1

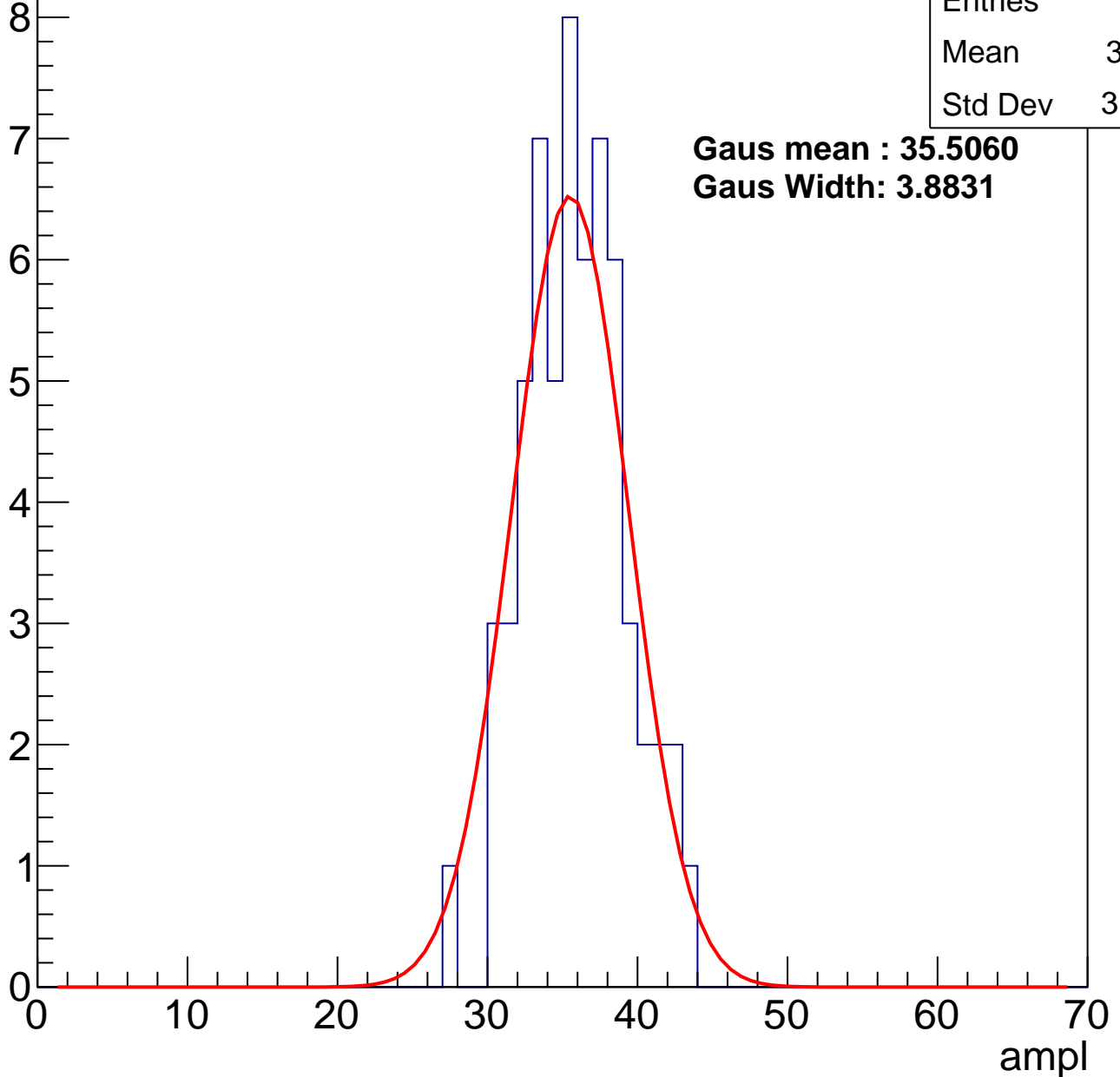
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	61
Mean	35.41
Std Dev	3.326

**Gaus mean : 35.5060**

**Gaus Width: 3.8831**



# B1L003S, U18-ch73, adc2

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	77
Mean	42.6
Std Dev	3.188

**Gaus mean : 42.8257**

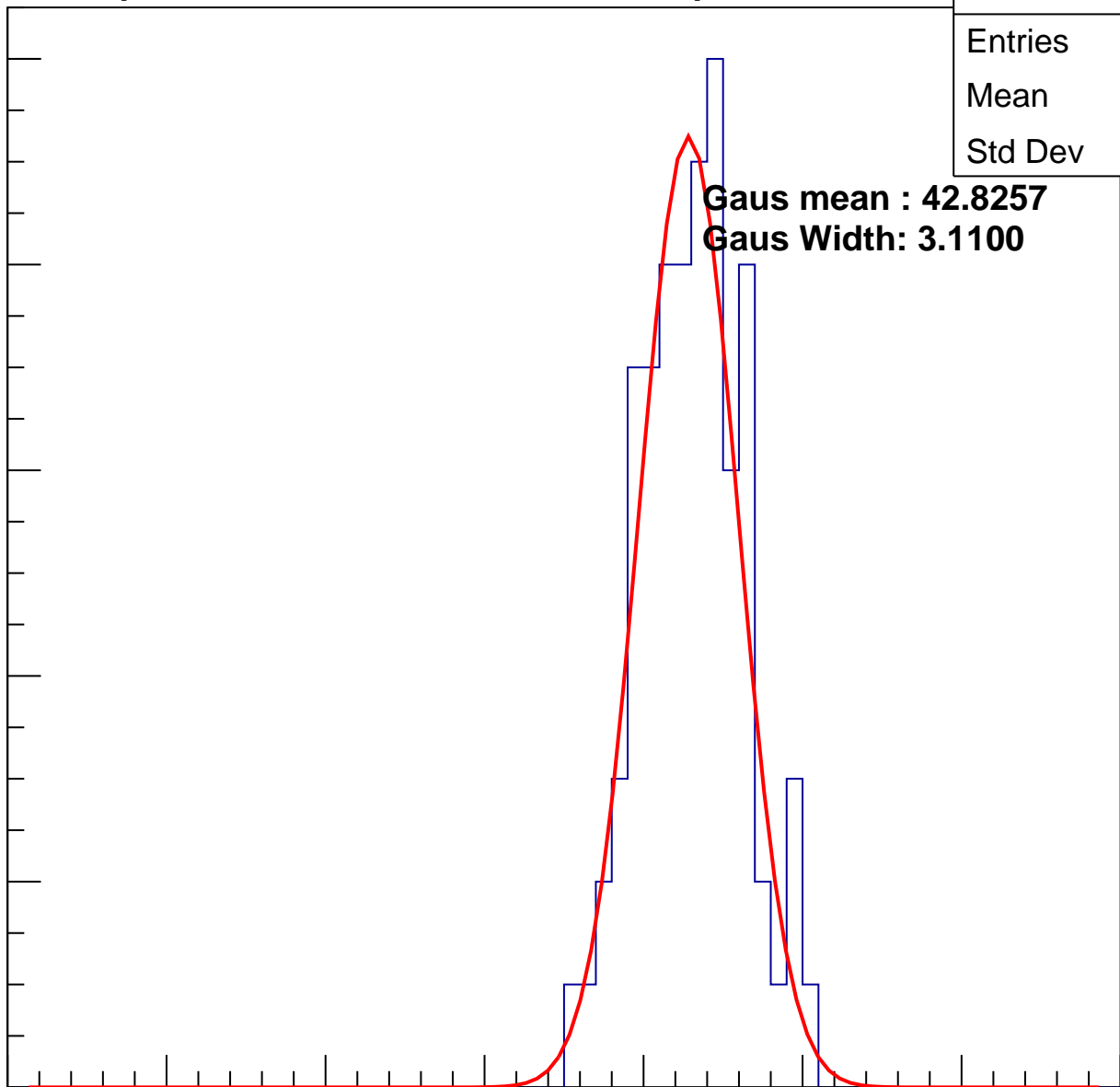
**Gaus Width: 3.1100**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

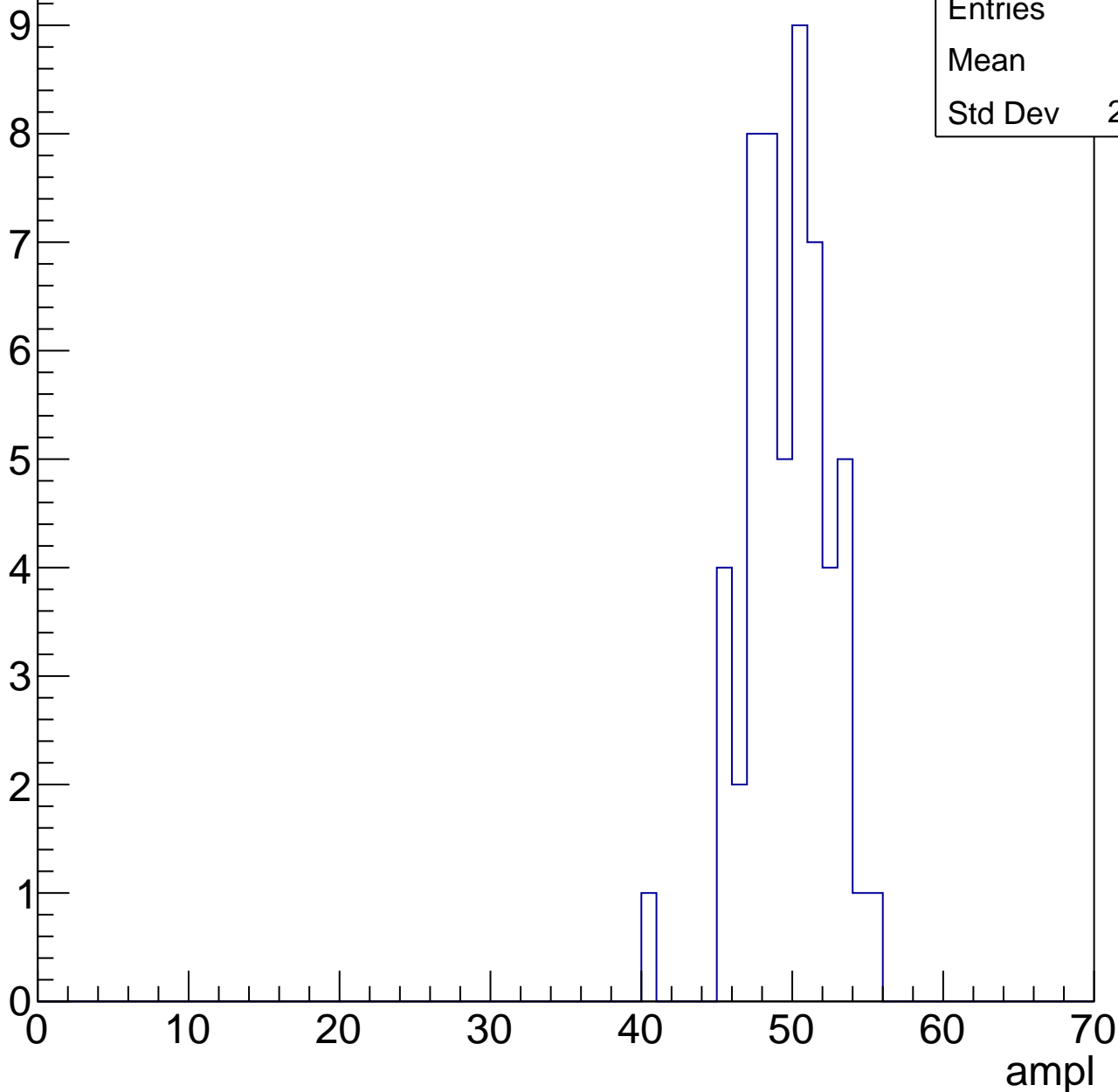


# B1L003S, U18-ch73, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

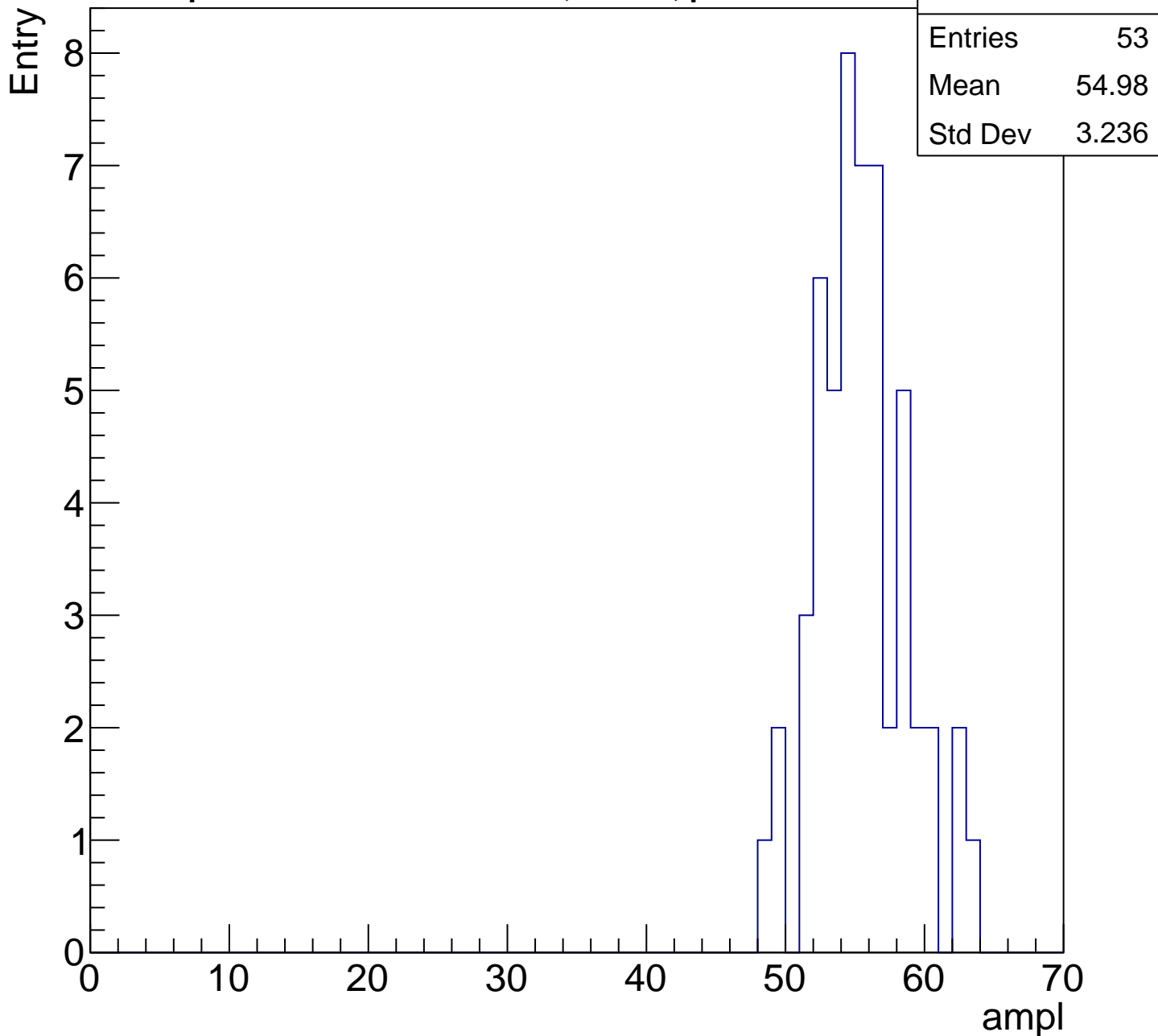
Entry

Entries	55
Mean	49.2
Std Dev	2.746



# B1L003S, U18-ch73, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2



# B1L003S, U18-ch73, adc5

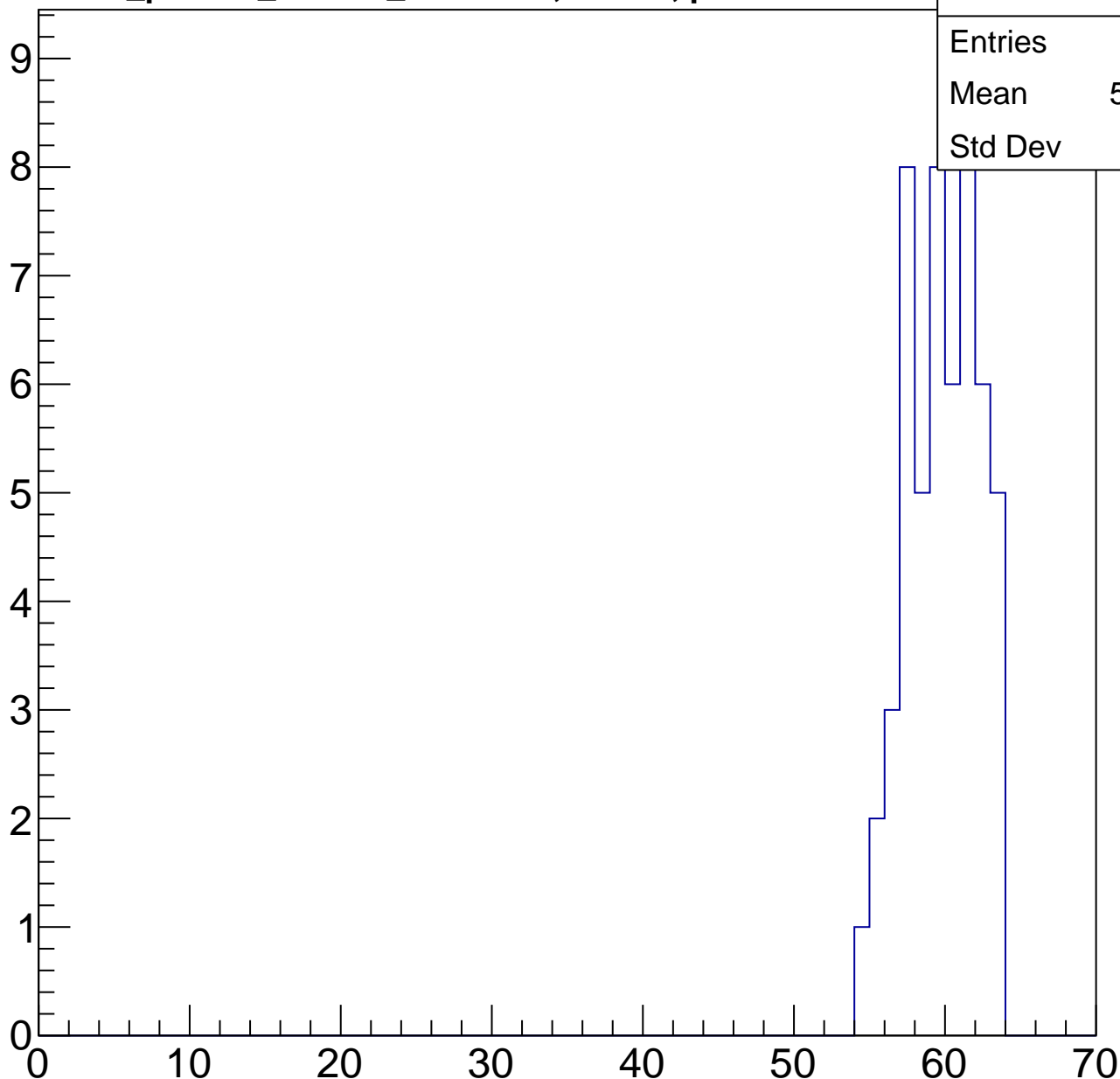
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	53
Mean	59.36
Std Dev	2.34

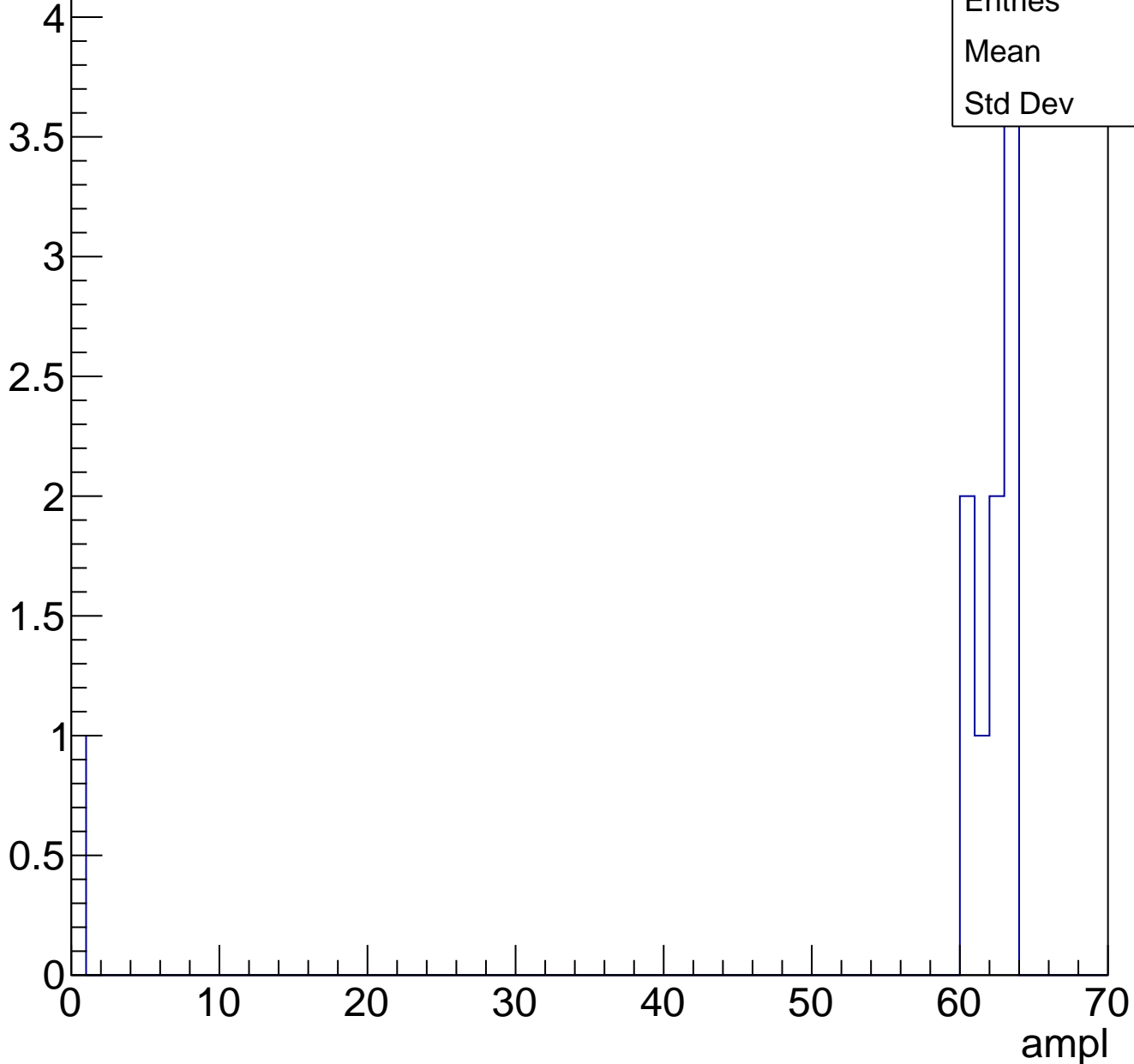
ampl



# B1L003S, U18-ch73, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U18-ch73, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L003S, U18-ch74, adc0

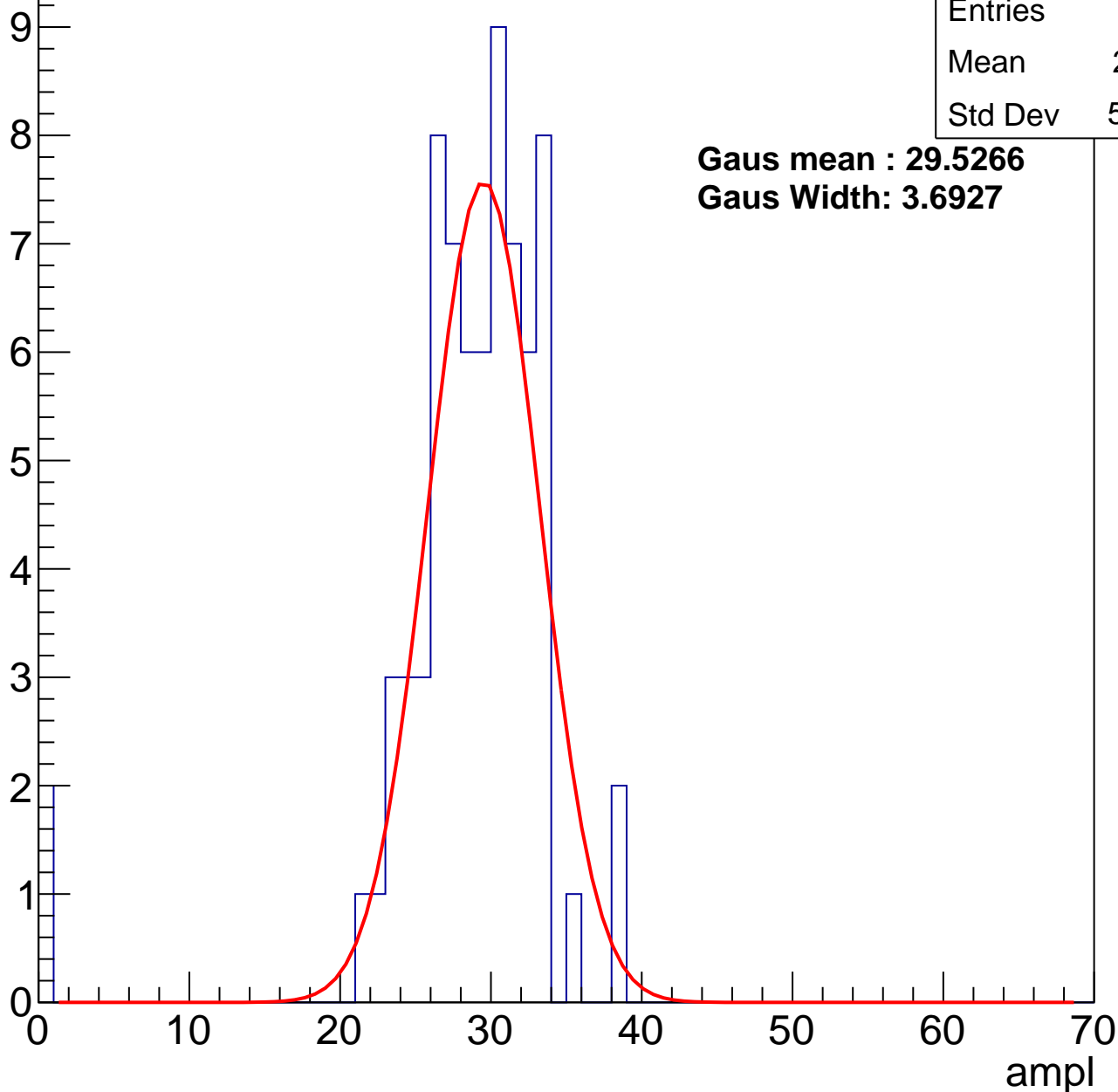
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	73
Mean	28.11
Std Dev	5.842

**Gaus mean : 29.5266**

**Gaus Width: 3.6927**



# B1L003S, U18-ch74, adc1

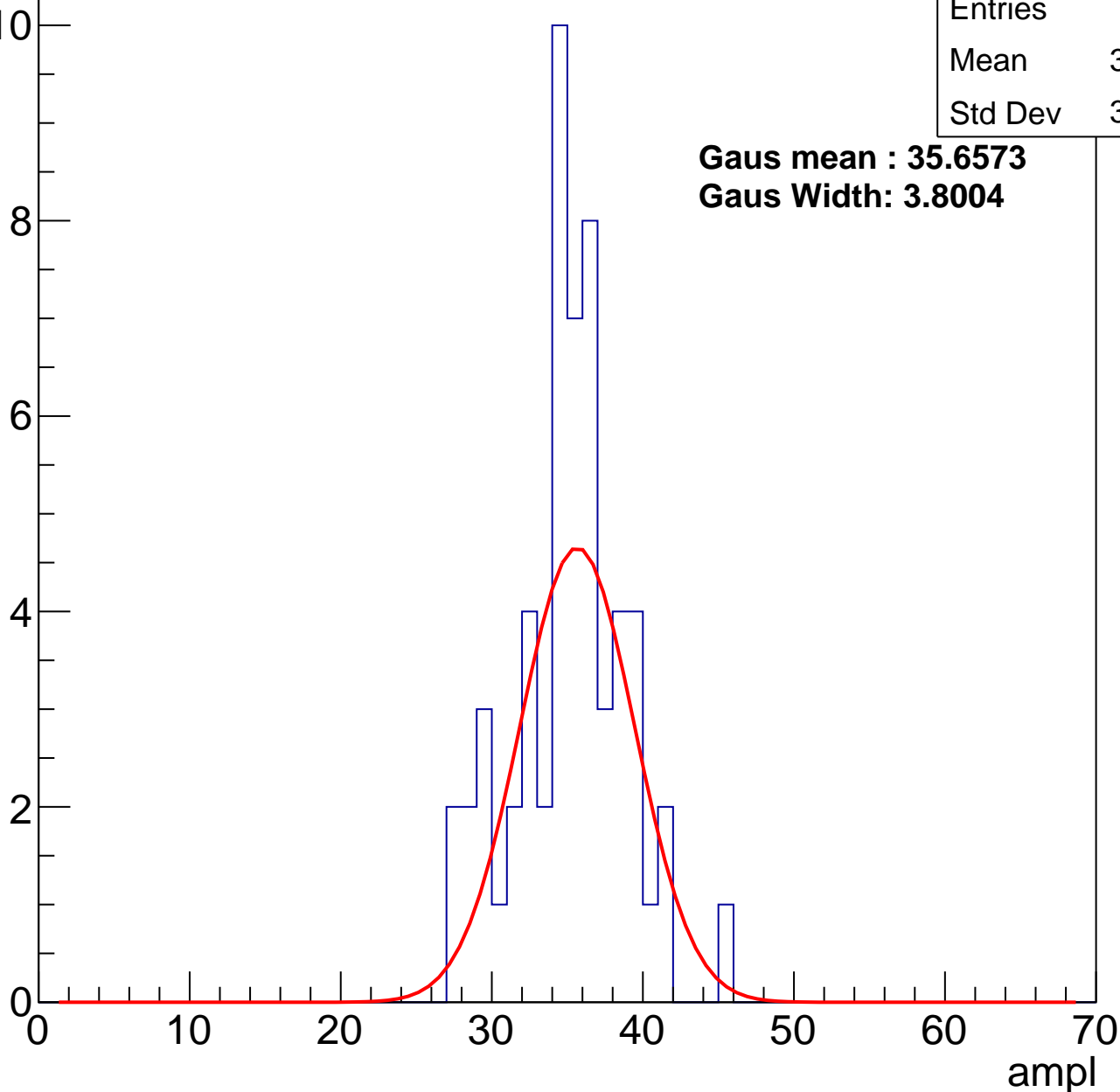
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	56
Mean	34.68
Std Dev	3.675

**Gaus mean : 35.6573**

**Gaus Width: 3.8004**



# B1L003S, U18-ch74, adc2

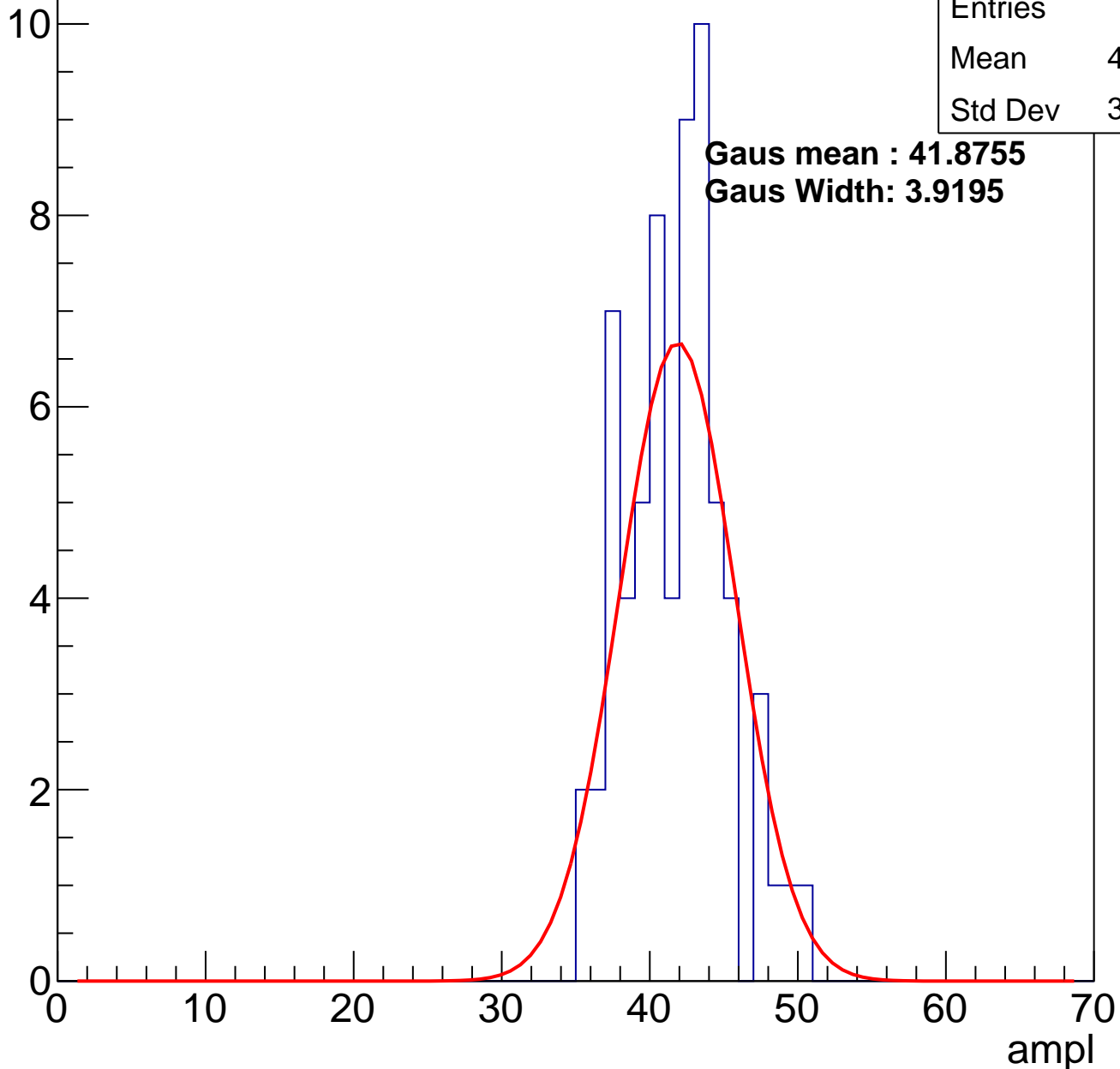
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	66
Mean	41.33
Std Dev	3.372

**Gaus mean : 41.8755**

**Gaus Width: 3.9195**

Entry

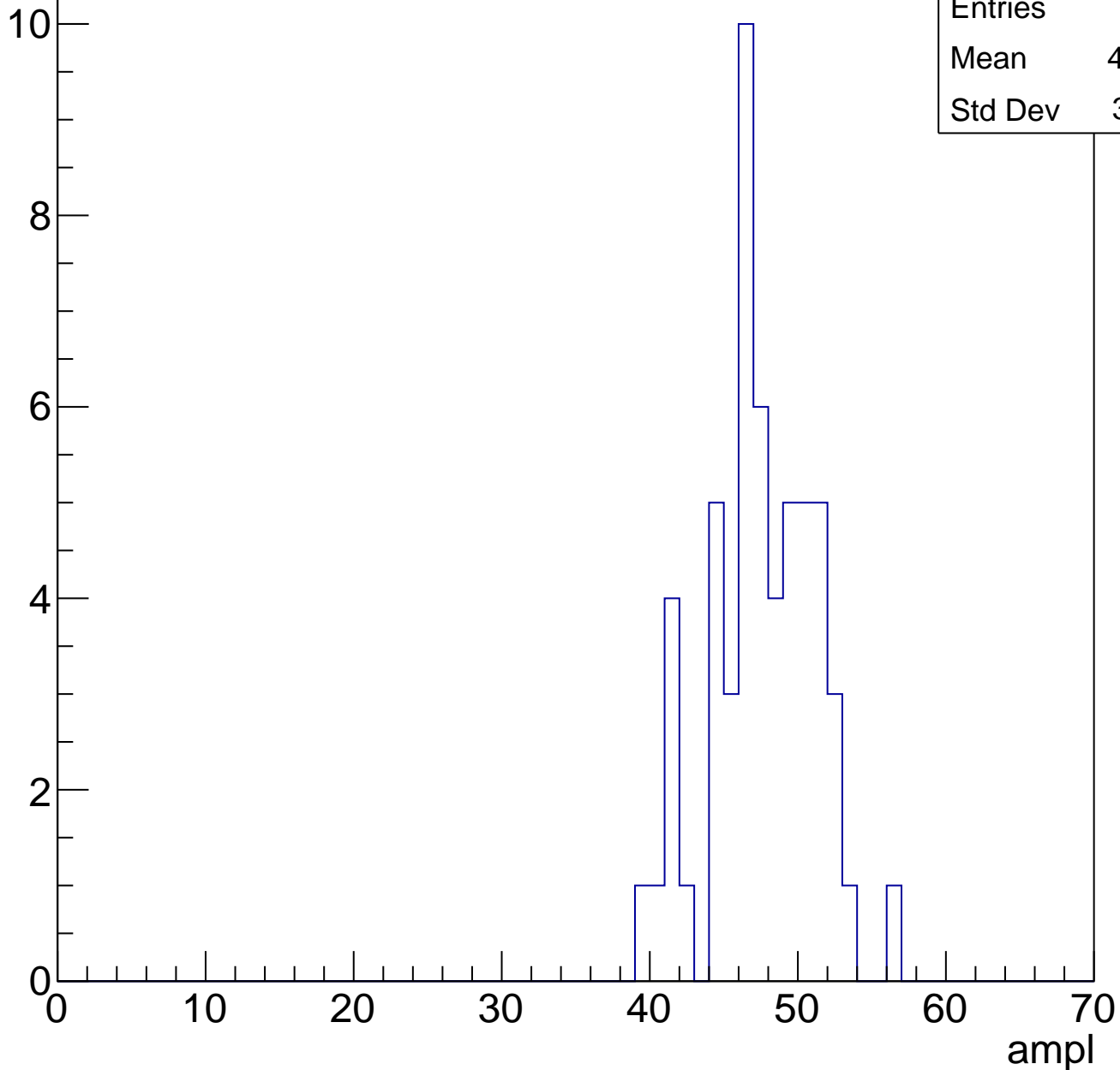


# B1L003S, U18-ch74, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	55
Mean	47.07
Std Dev	3.541

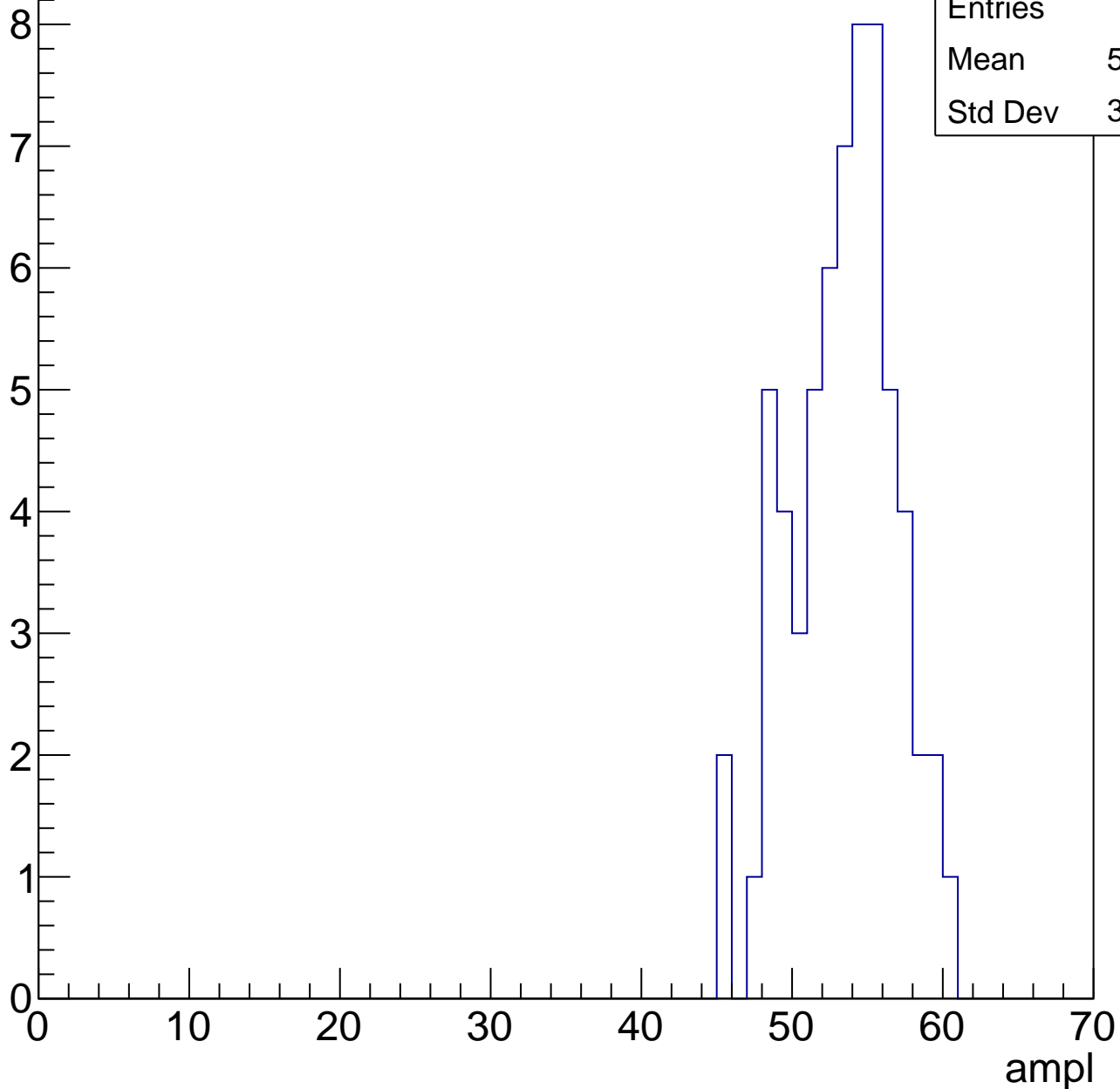
Entry



# B1L003S, U18-ch74, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

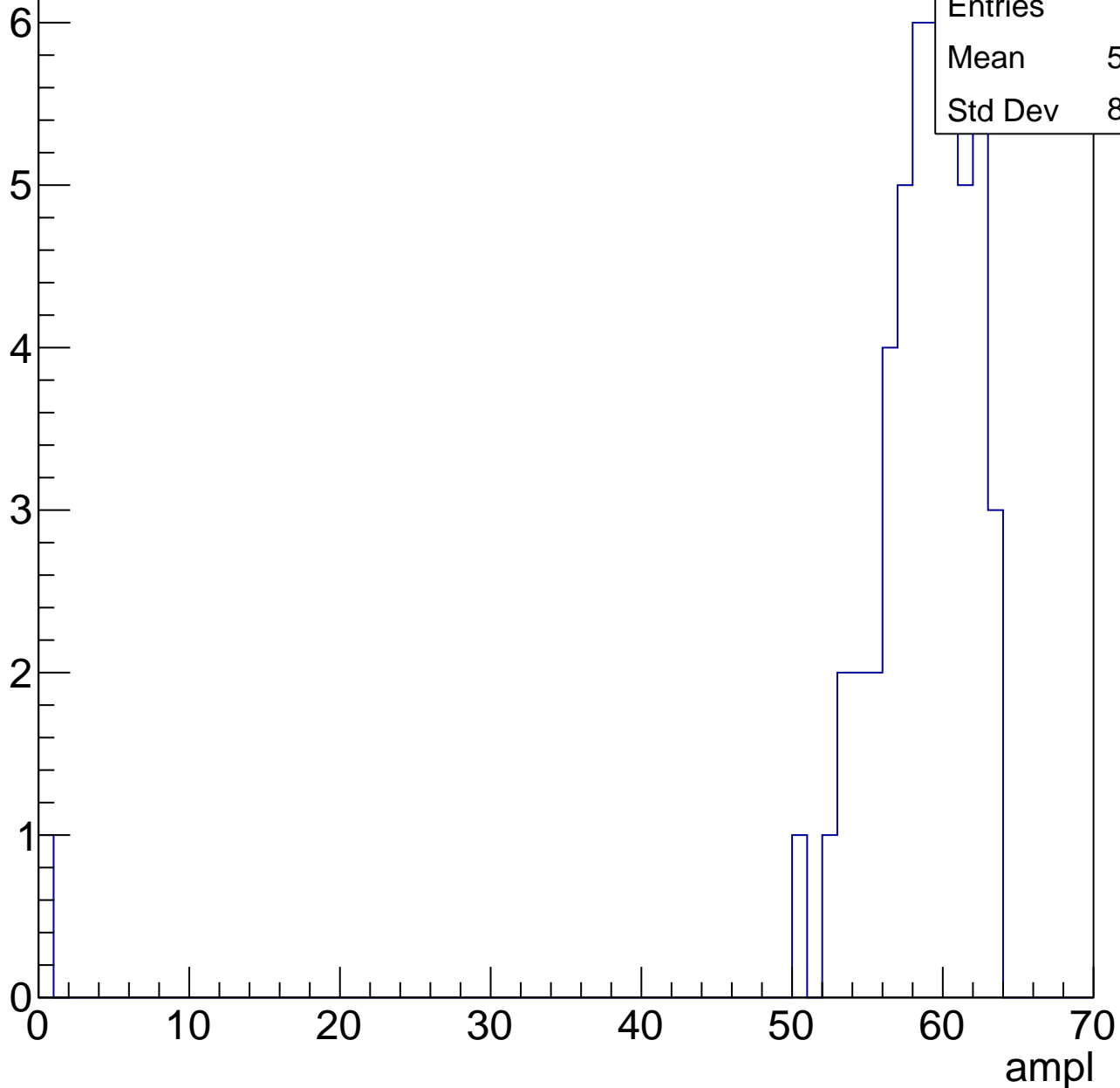


# B1L003S, U18-ch74, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	50
Mean	57.26
Std Dev	8.722

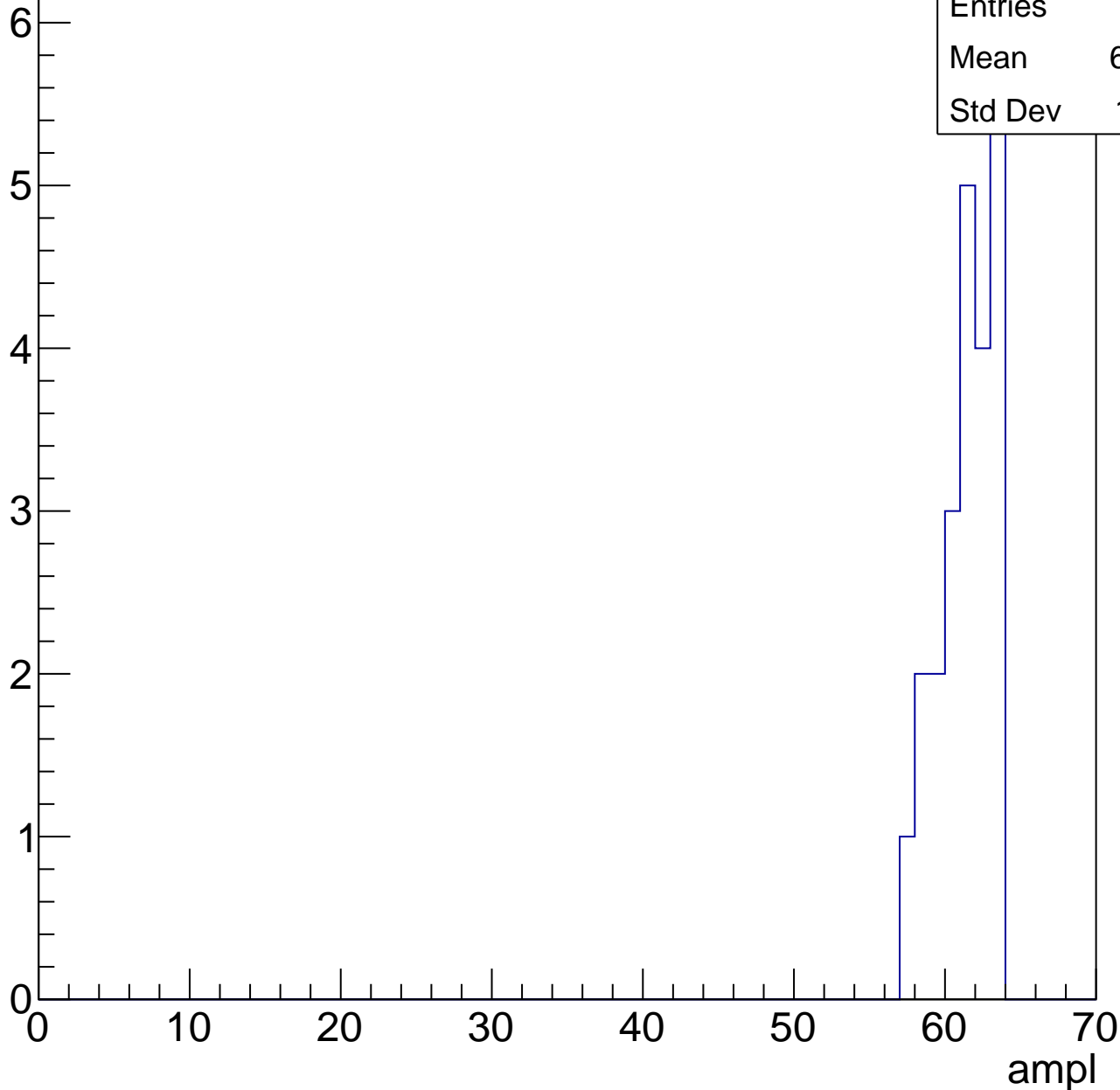


# B1L003S, U18-ch74, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	23
Mean	60.96
Std Dev	1.781





# B1L003S, U18-ch74, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U18-ch75, adc0

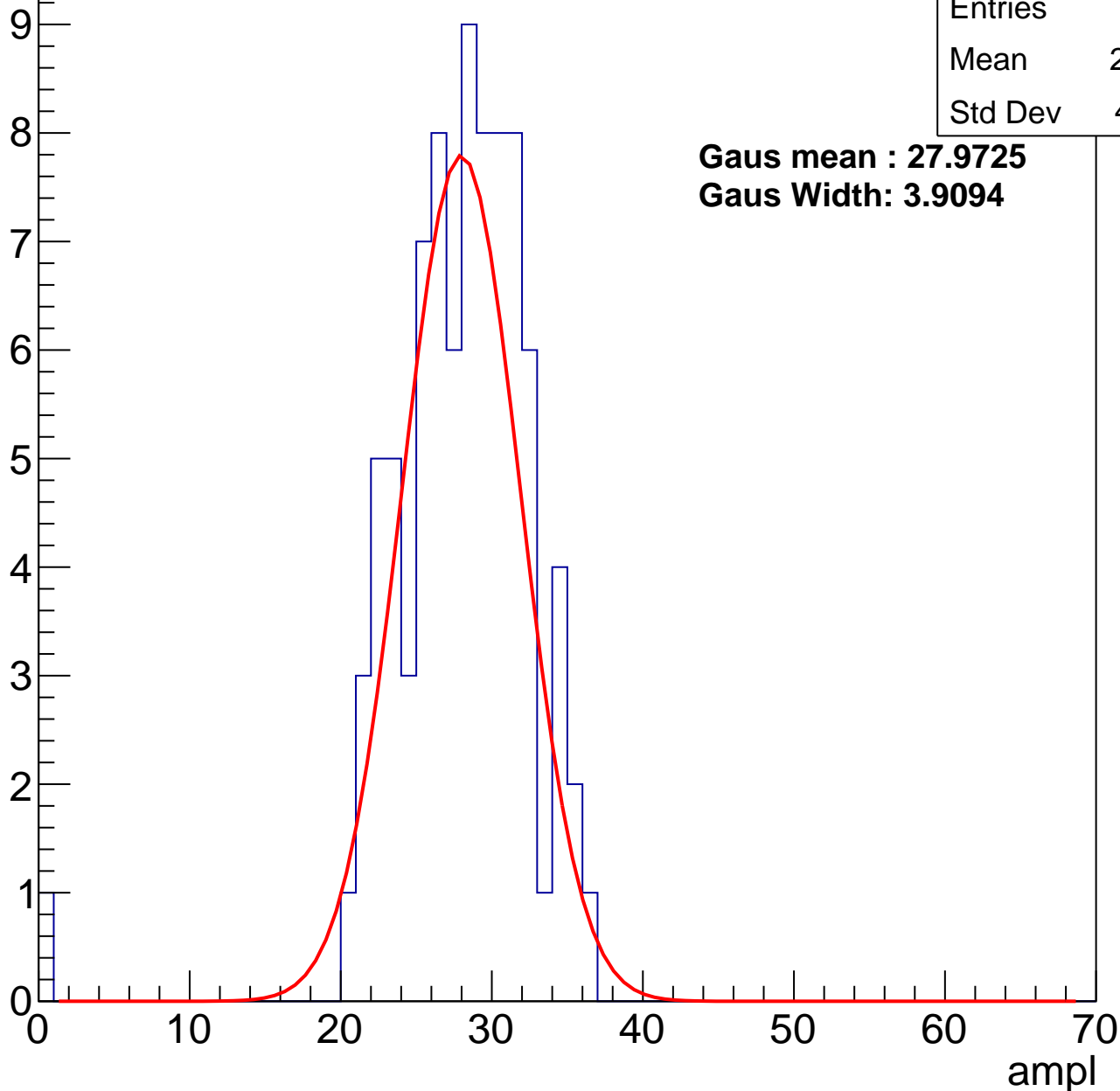
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	86
Mean	27.49
Std Dev	4.781

**Gaus mean : 27.9725**

**Gaus Width: 3.9094**



# B1L003S, U18-ch75, adc1

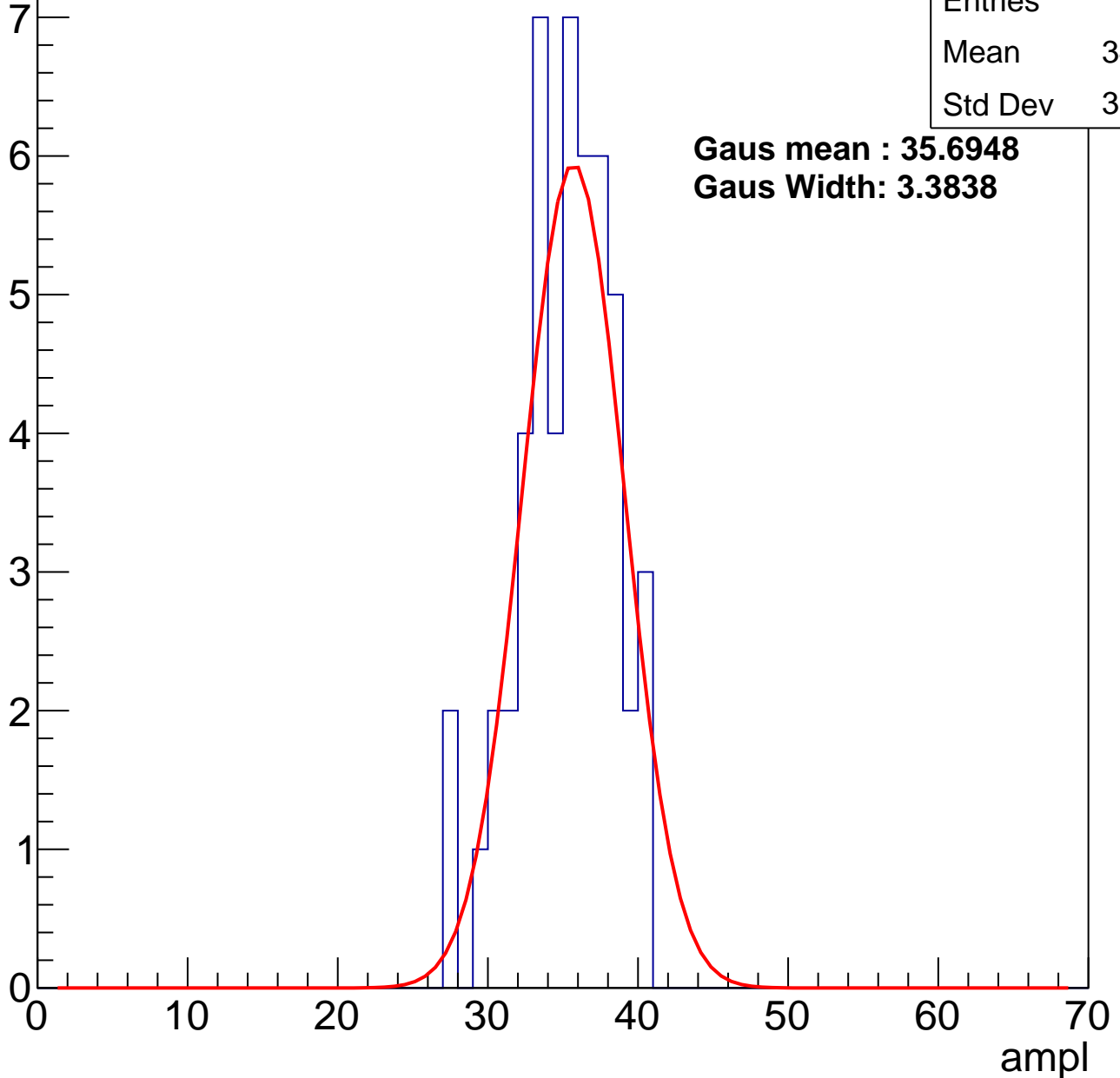
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	51
Mean	34.73
Std Dev	3.106

**Gaus mean : 35.6948**

**Gaus Width: 3.3838**



# B1L003S, U18-ch75, adc2

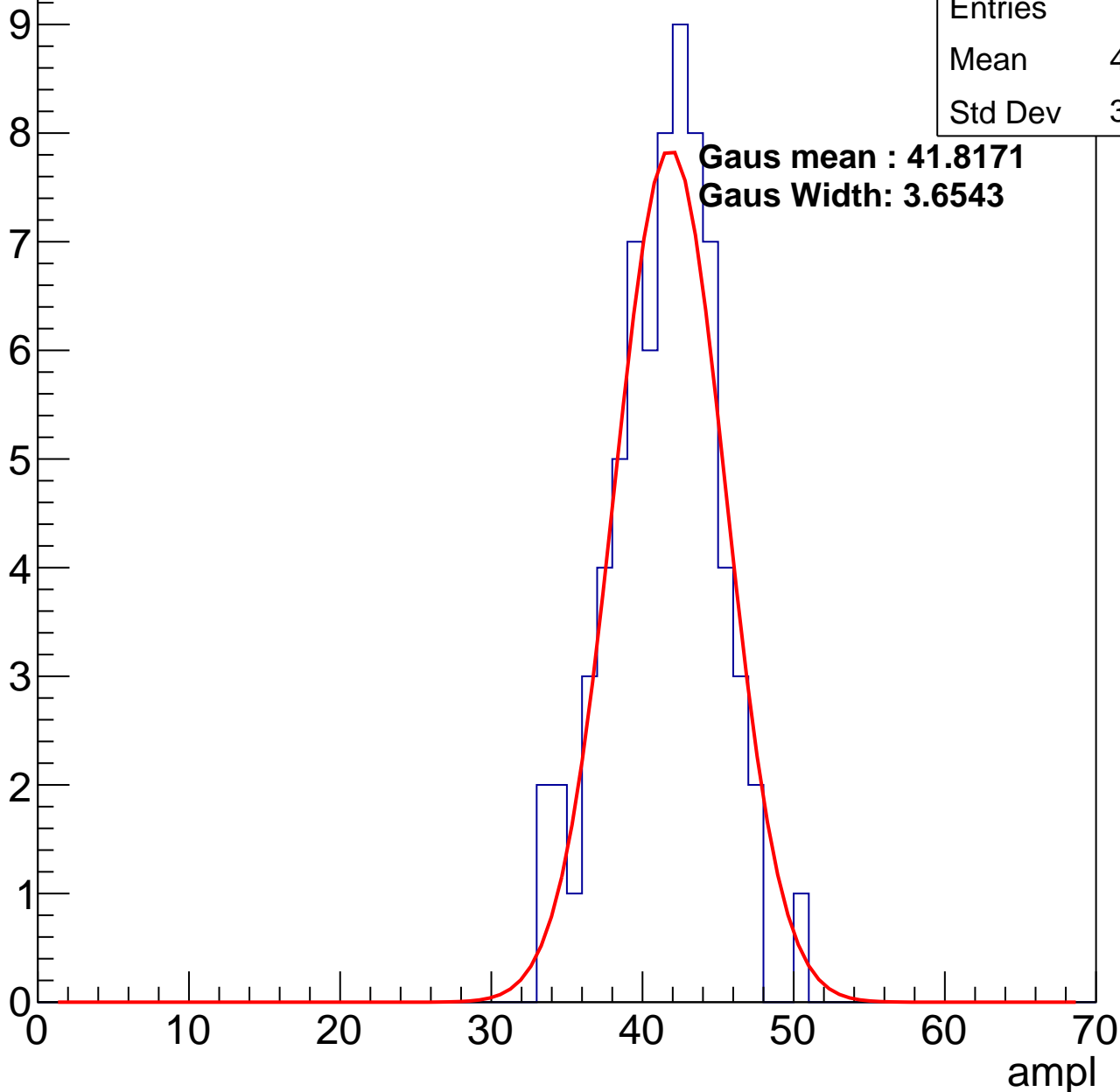
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	72
Mean	40.94
Std Dev	3.488

**Gaus mean : 41.8171**

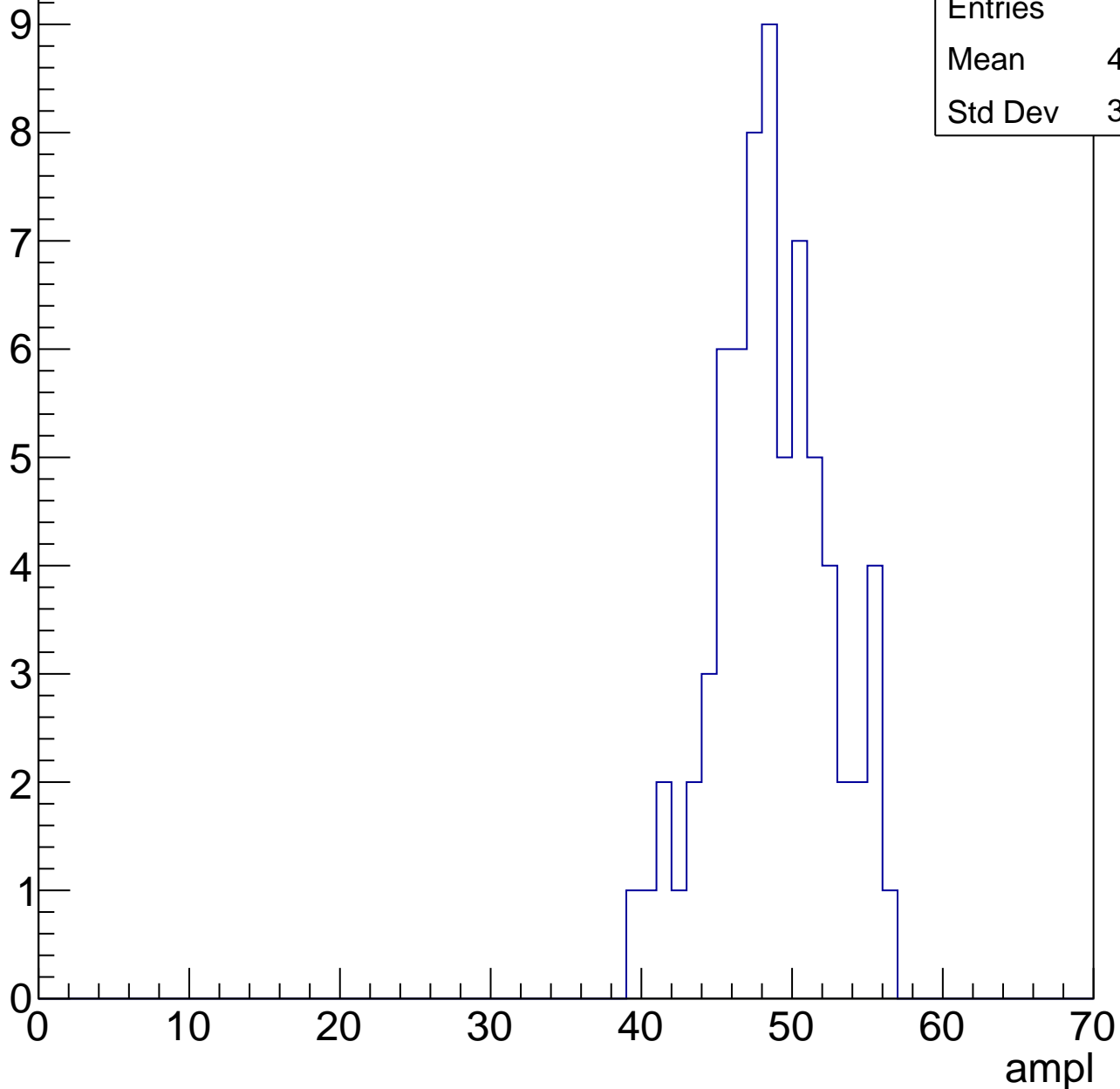
**Gaus Width: 3.6543**



# B1L003S, U18-ch75, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



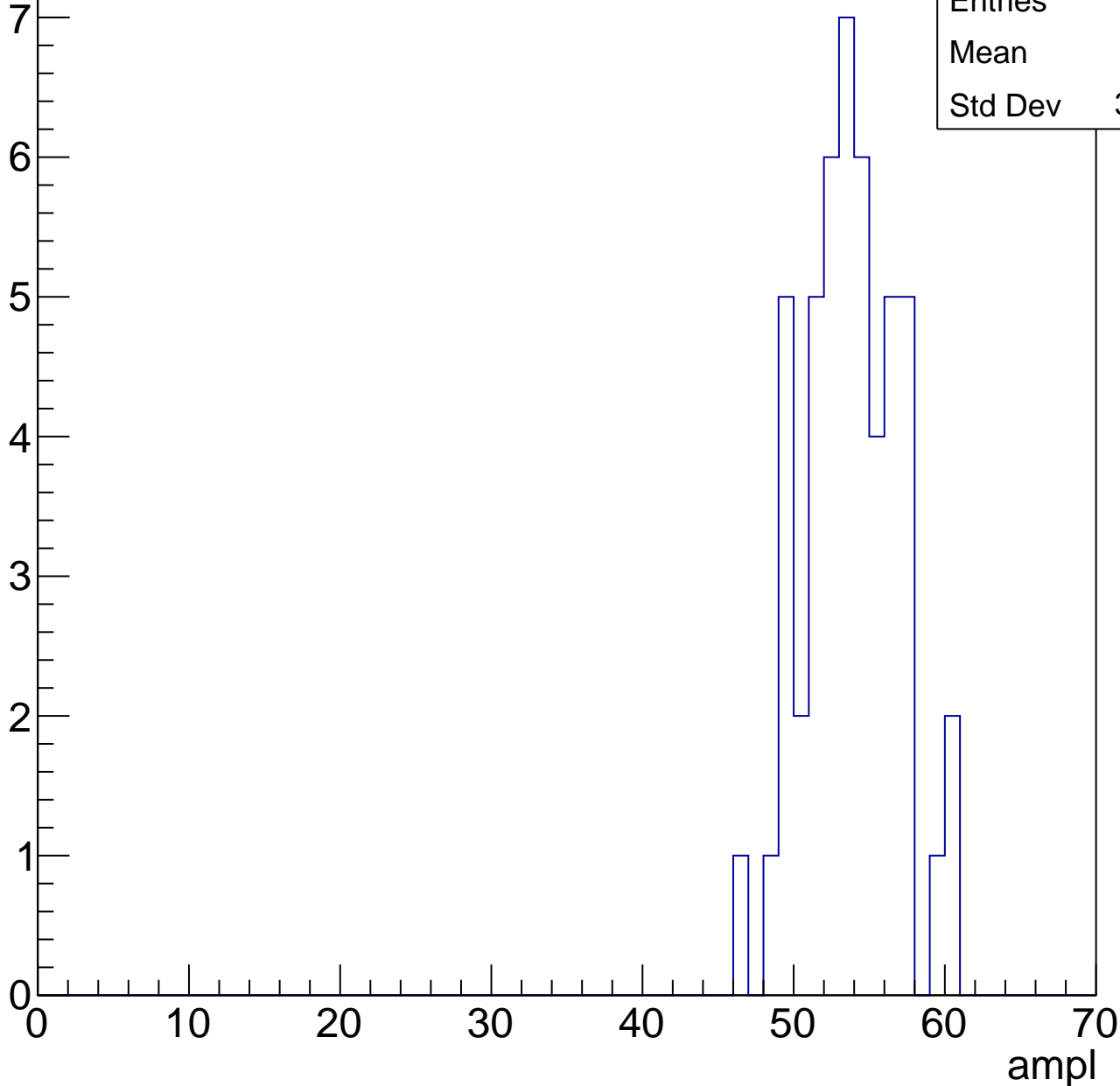
Entries	69
Mean	48.16
Std Dev	3.779

# B1L003S, U18-ch75, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	50
Mean	53.3
Std Dev	3.081



# B1L003S, U18-ch75, adc5

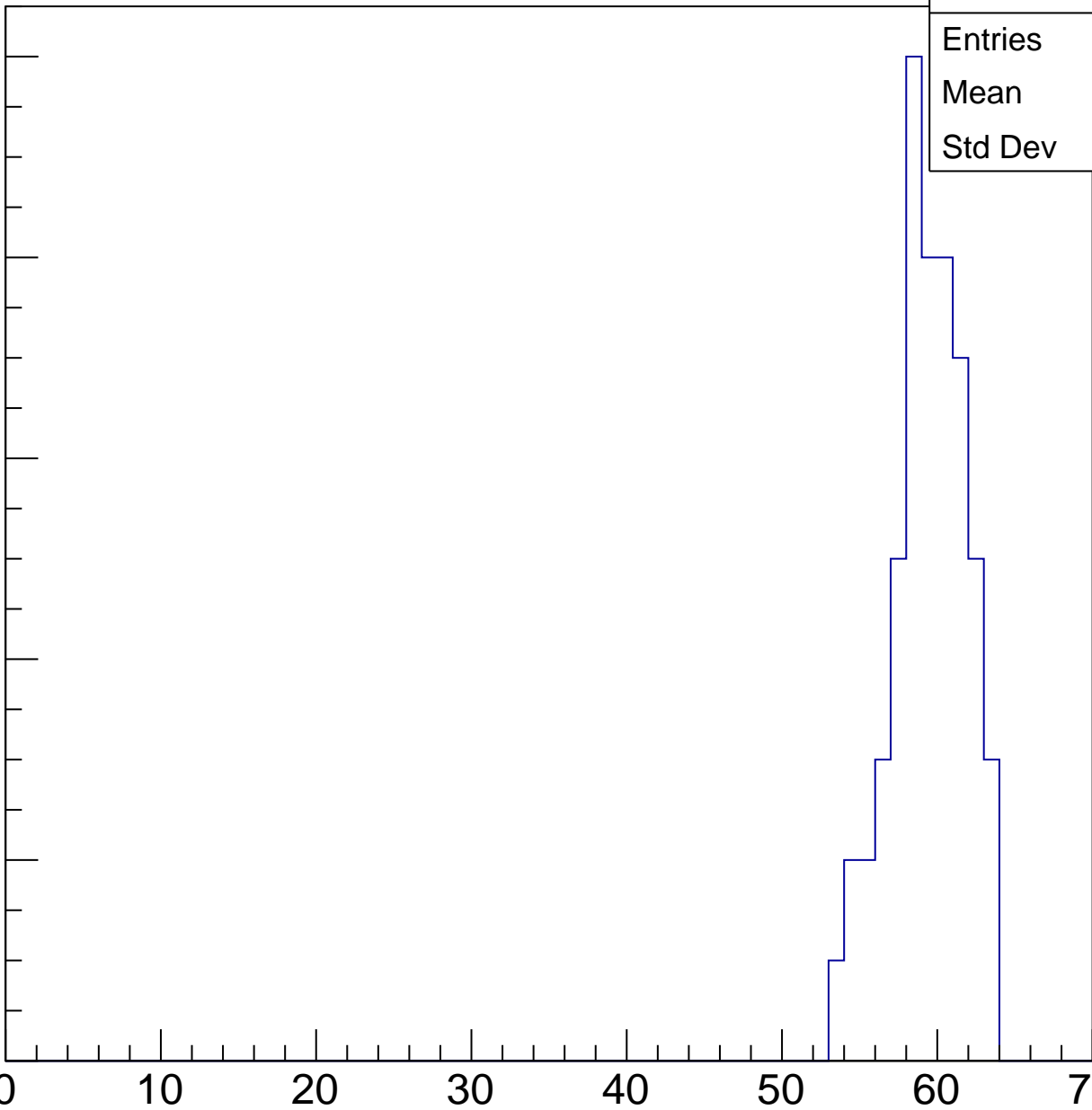
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

10  
8  
6  
4  
2  
0

Entries	54
Mean	58.93
Std Dev	2.372

ampl

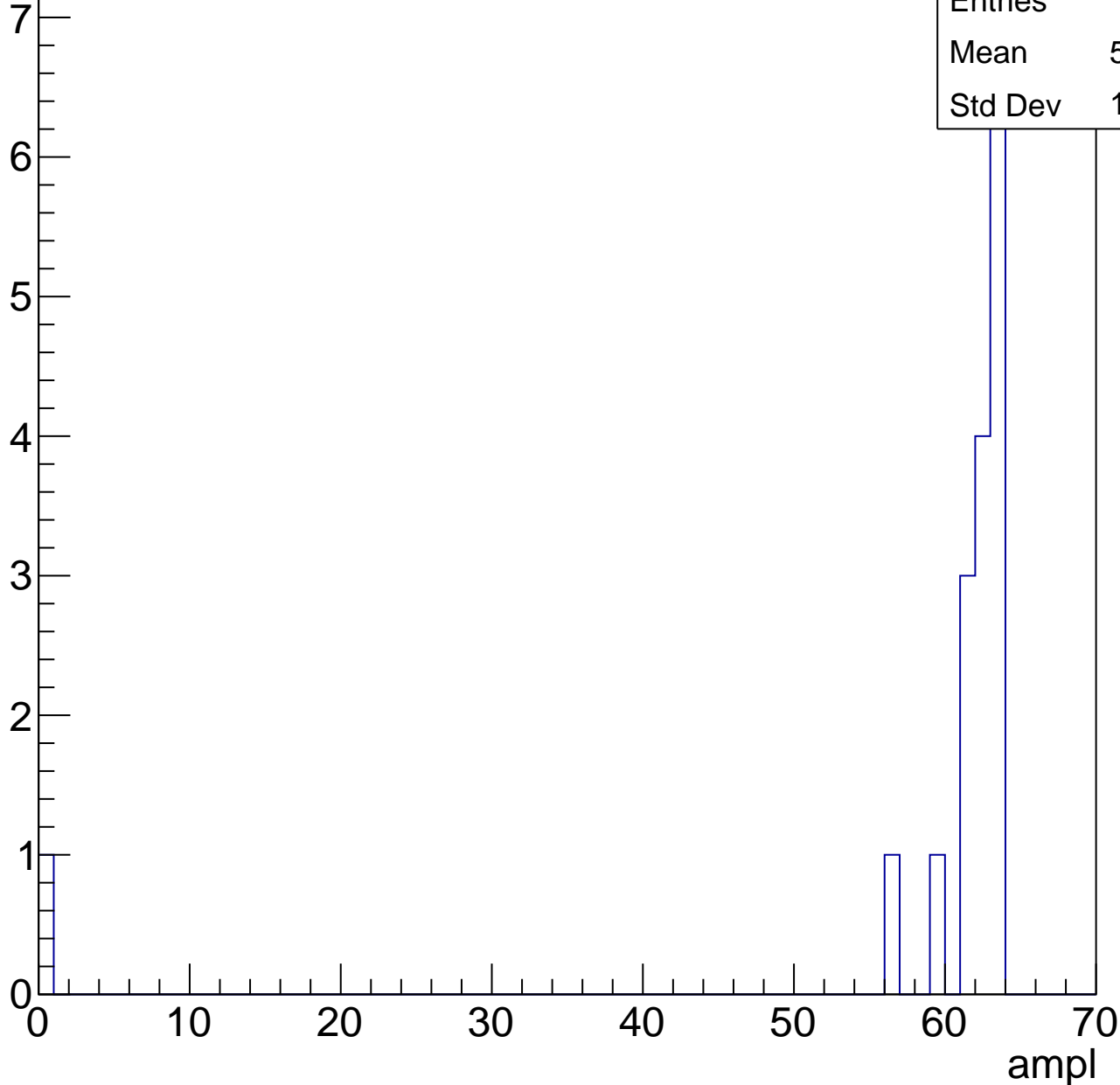


# B1L003S, U18-ch75, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	17
Mean	58.06
Std Dev	14.62





# B1L003S, U18-ch75, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U18-ch76, adc0

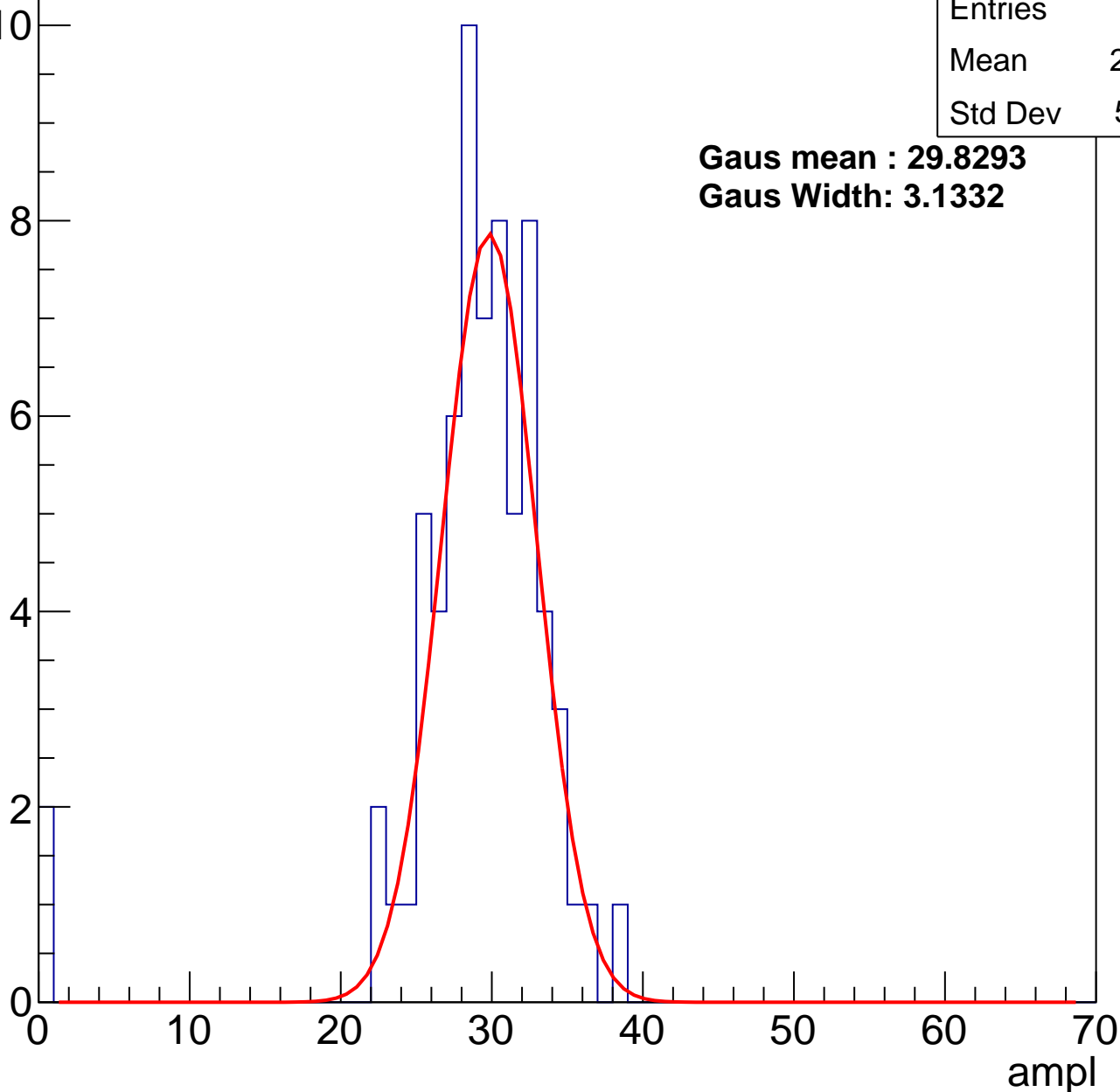
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	69
Mean	28.39
Std Dev	5.861

**Gaus mean : 29.8293**

**Gaus Width: 3.1332**



# B1L003S, U18-ch76, adc1

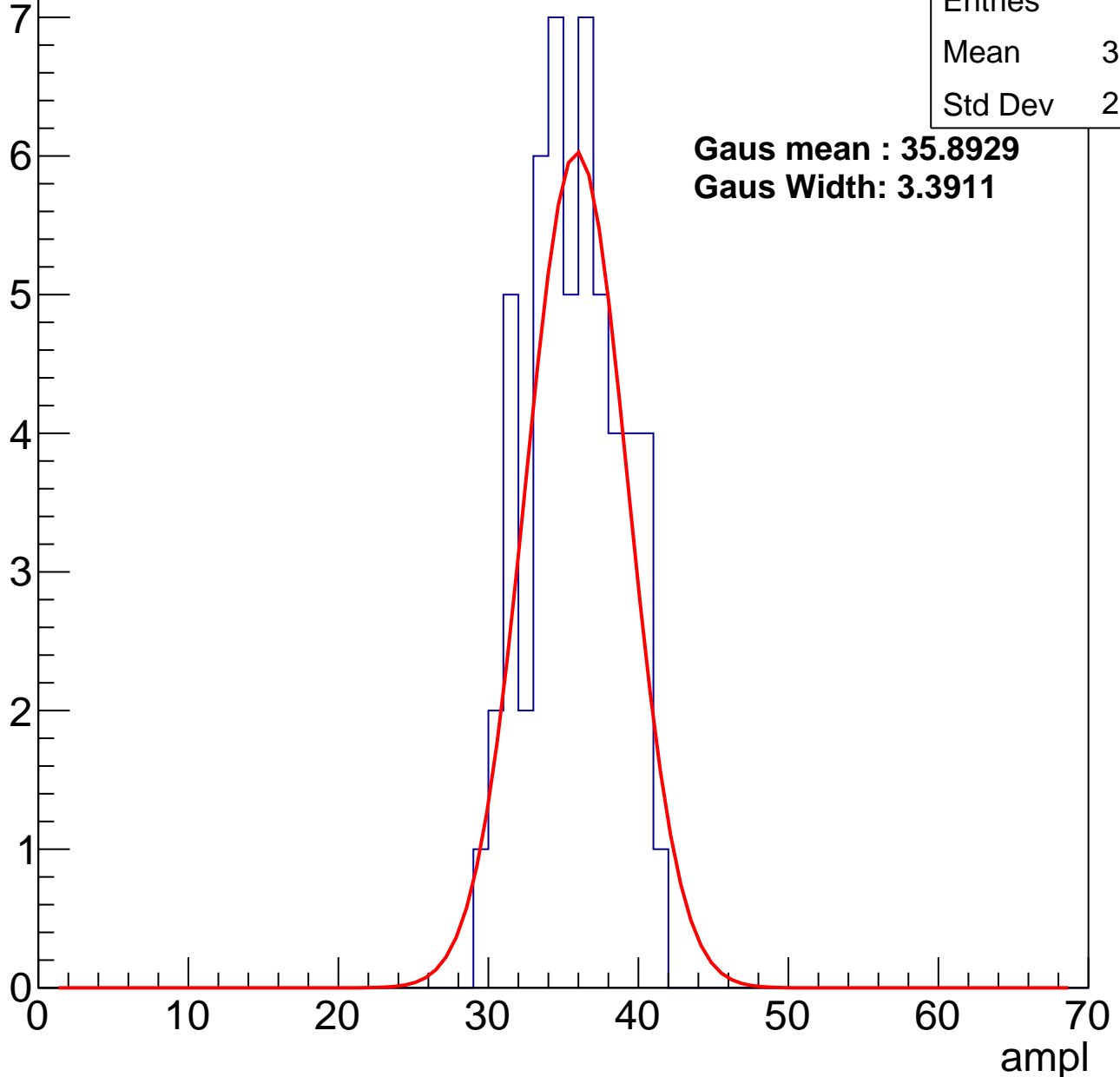
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	53
Mean	35.19
Std Dev	2.997

**Gaus mean : 35.8929**

**Gaus Width: 3.3911**



# B1L003S, U18-ch76, adc2

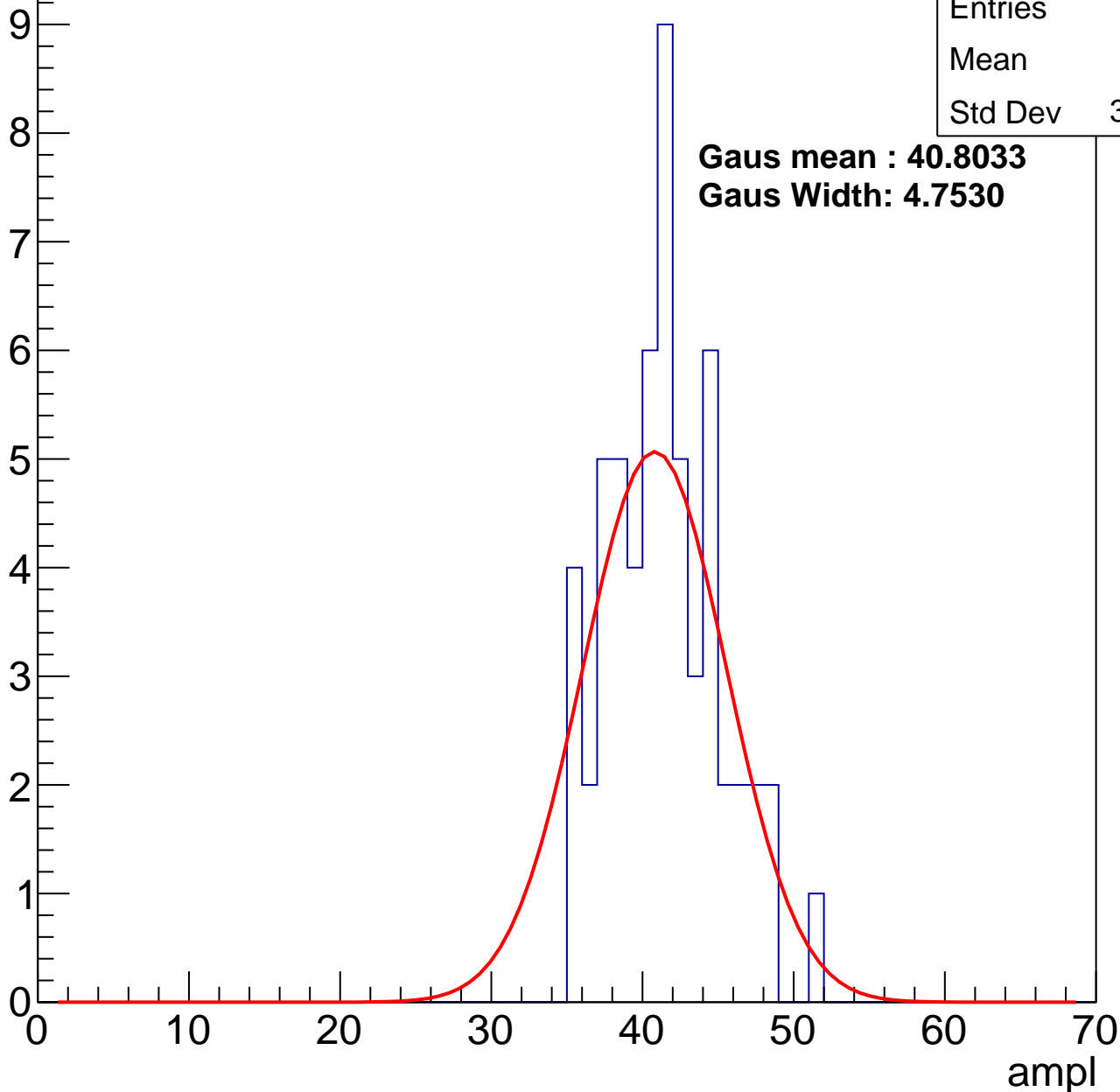
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	58
Mean	41
Std Dev	3.629

**Gaus mean : 40.8033**

**Gaus Width: 4.7530**

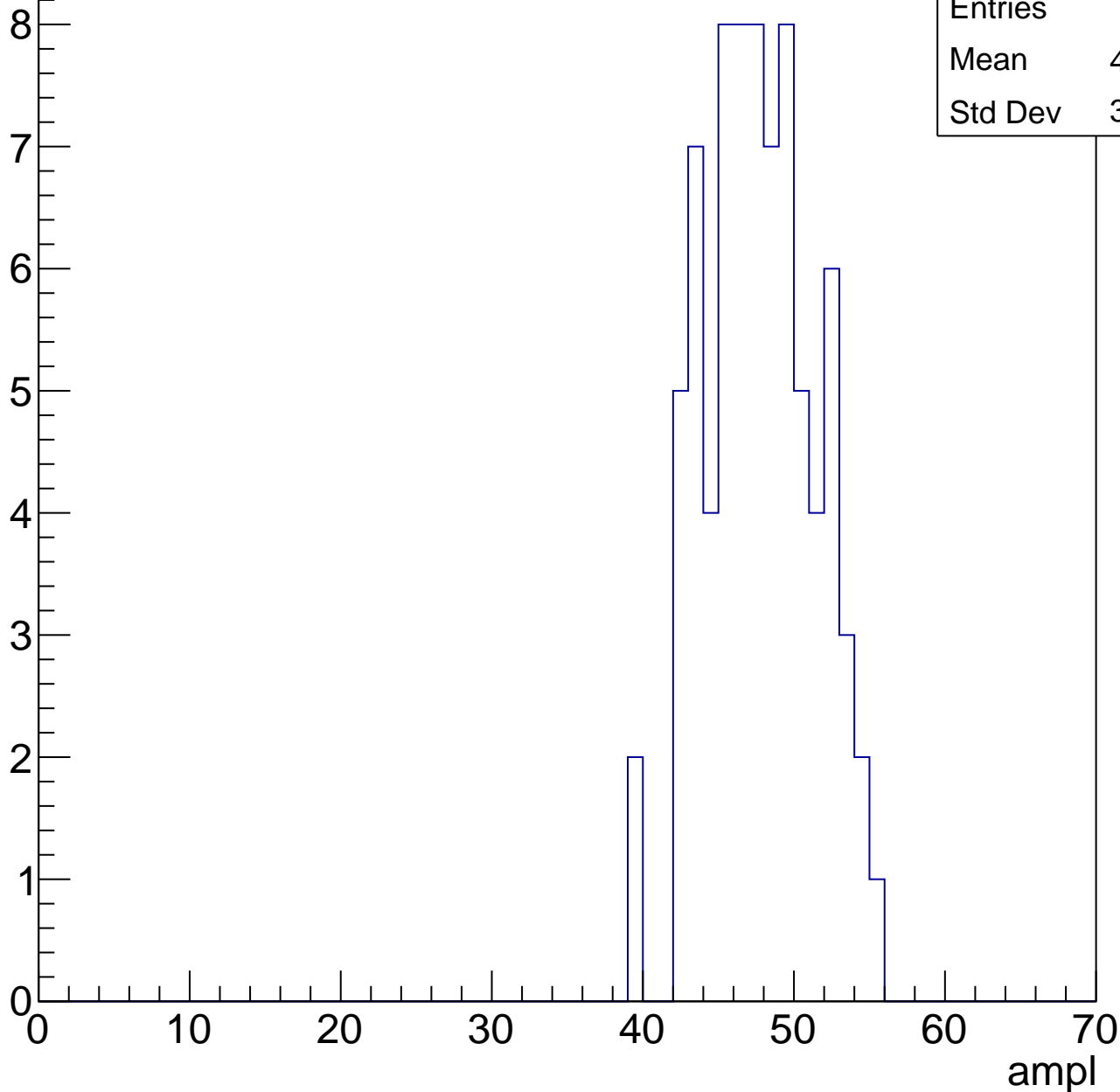


# B1L003S, U18-ch76, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

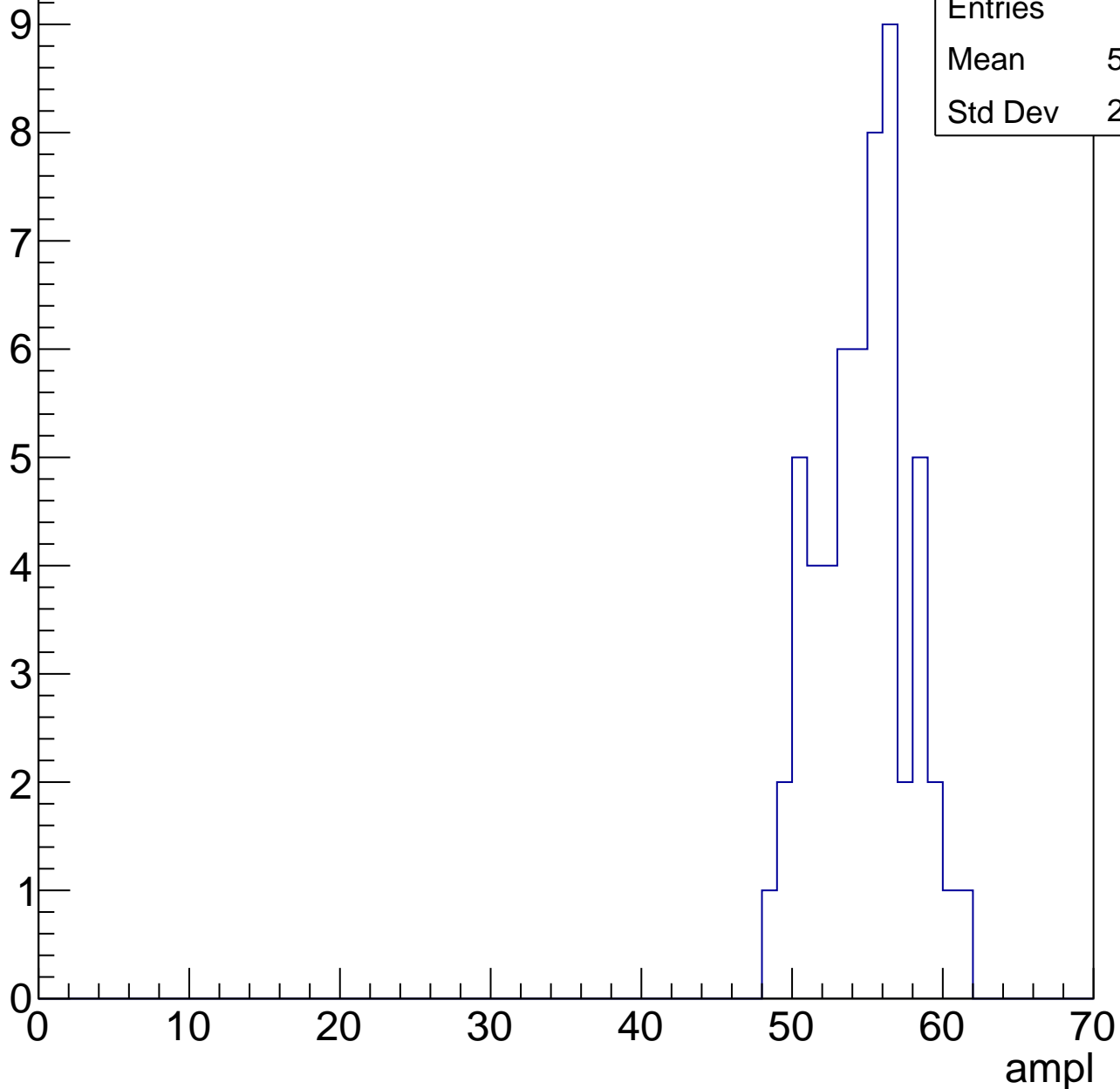
Entries	78
Mean	47.24
Std Dev	3.588



# B1L003S, U18-ch76, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

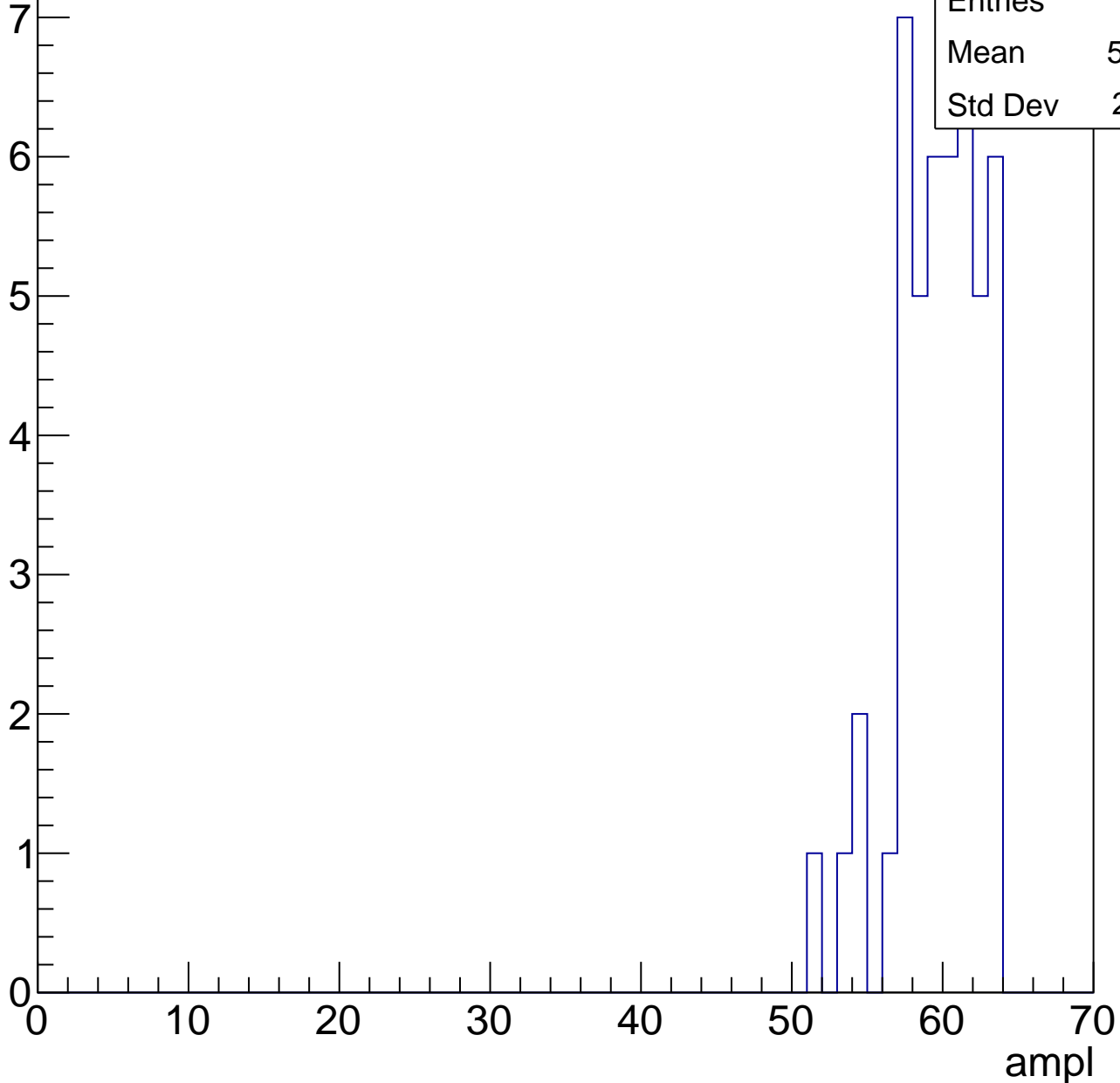


# B1L003S, U18-ch76, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	47
Mean	59.28
Std Dev	2.781

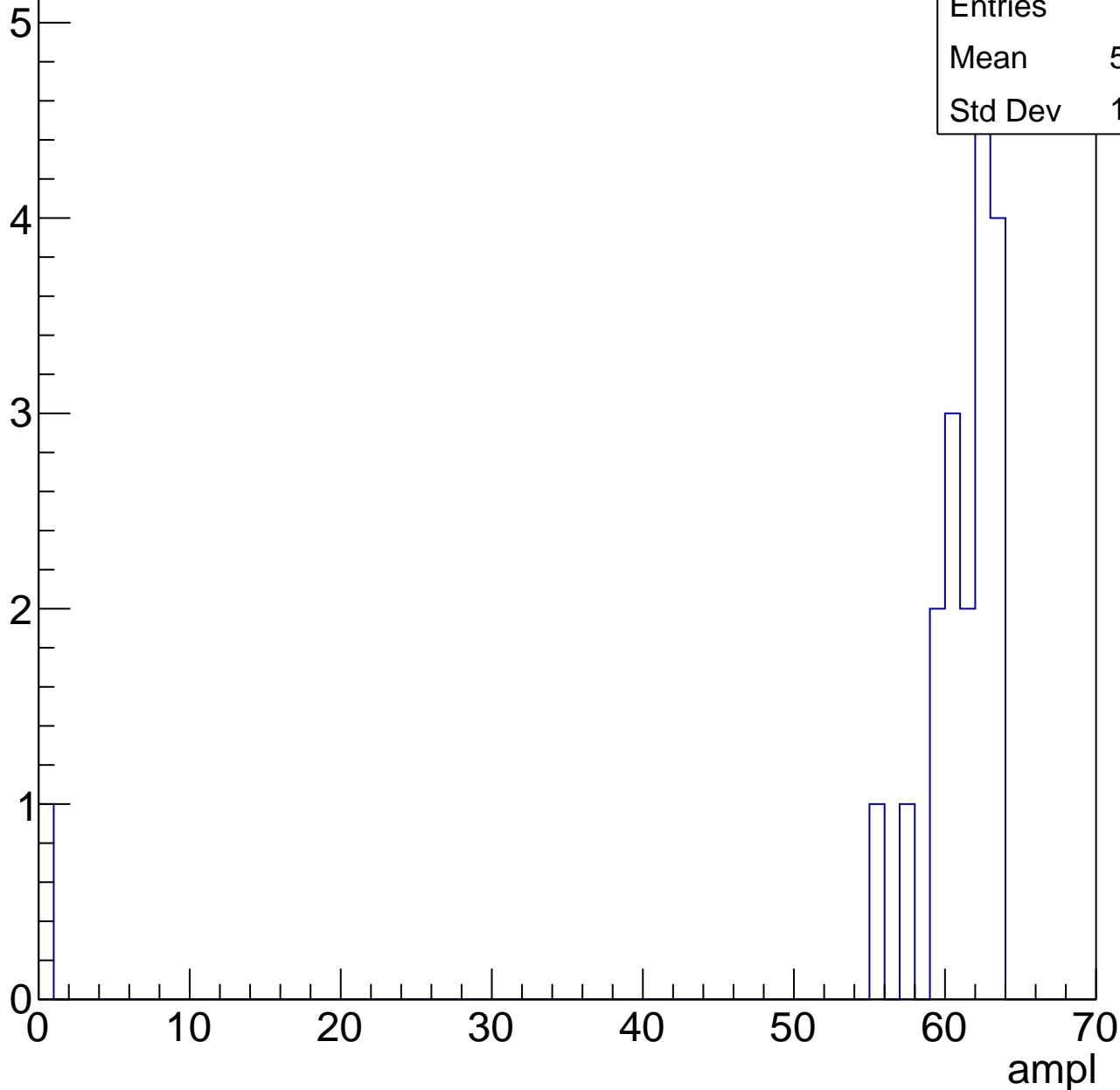


# B1L003S, U18-ch76, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	19
Mean	57.58
Std Dev	13.73





# B1L003S, U18-ch76, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U18-ch77, adc0

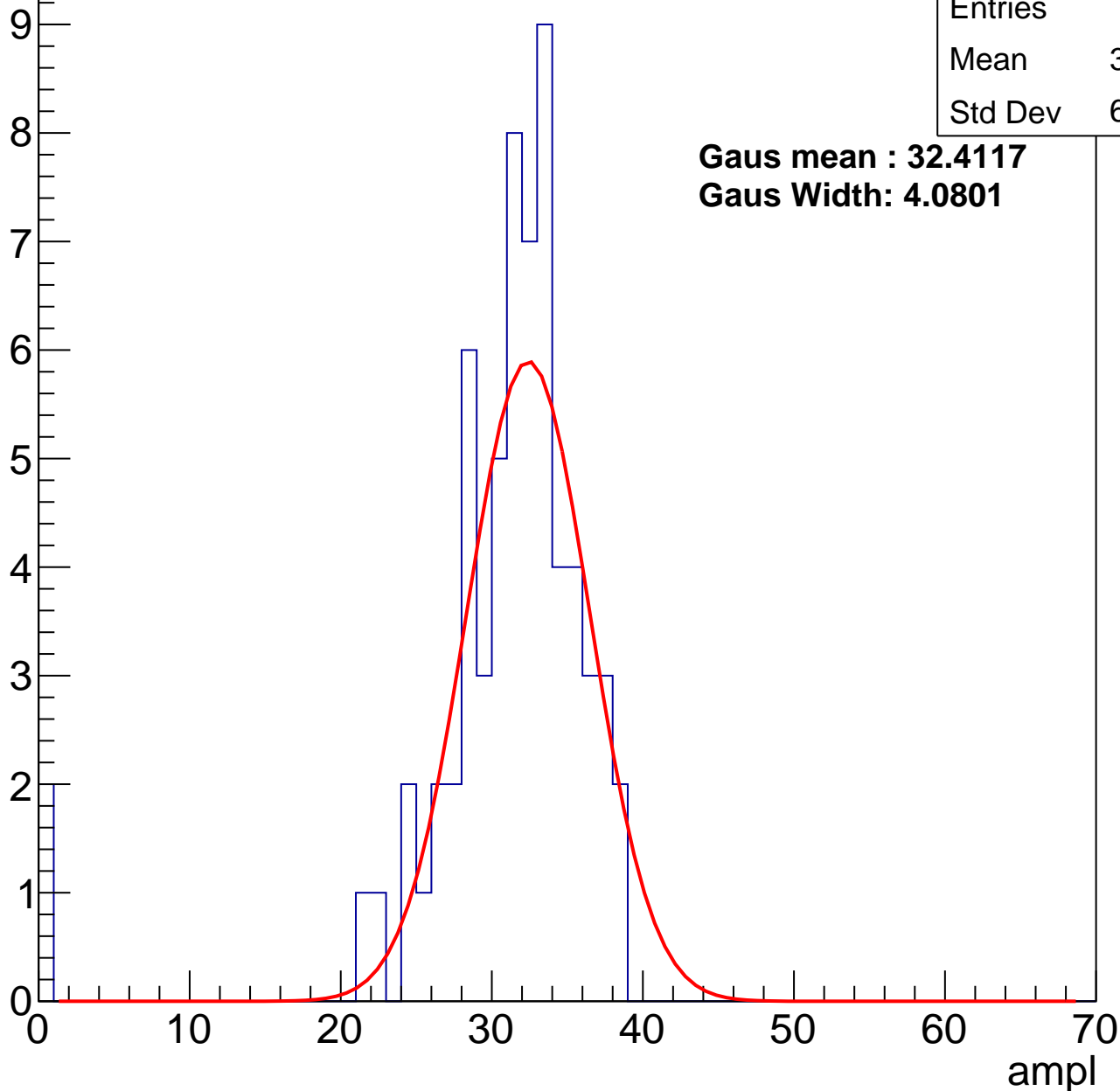
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	65
Mean	30.26
Std Dev	6.538

**Gaus mean : 32.4117**

**Gaus Width: 4.0801**



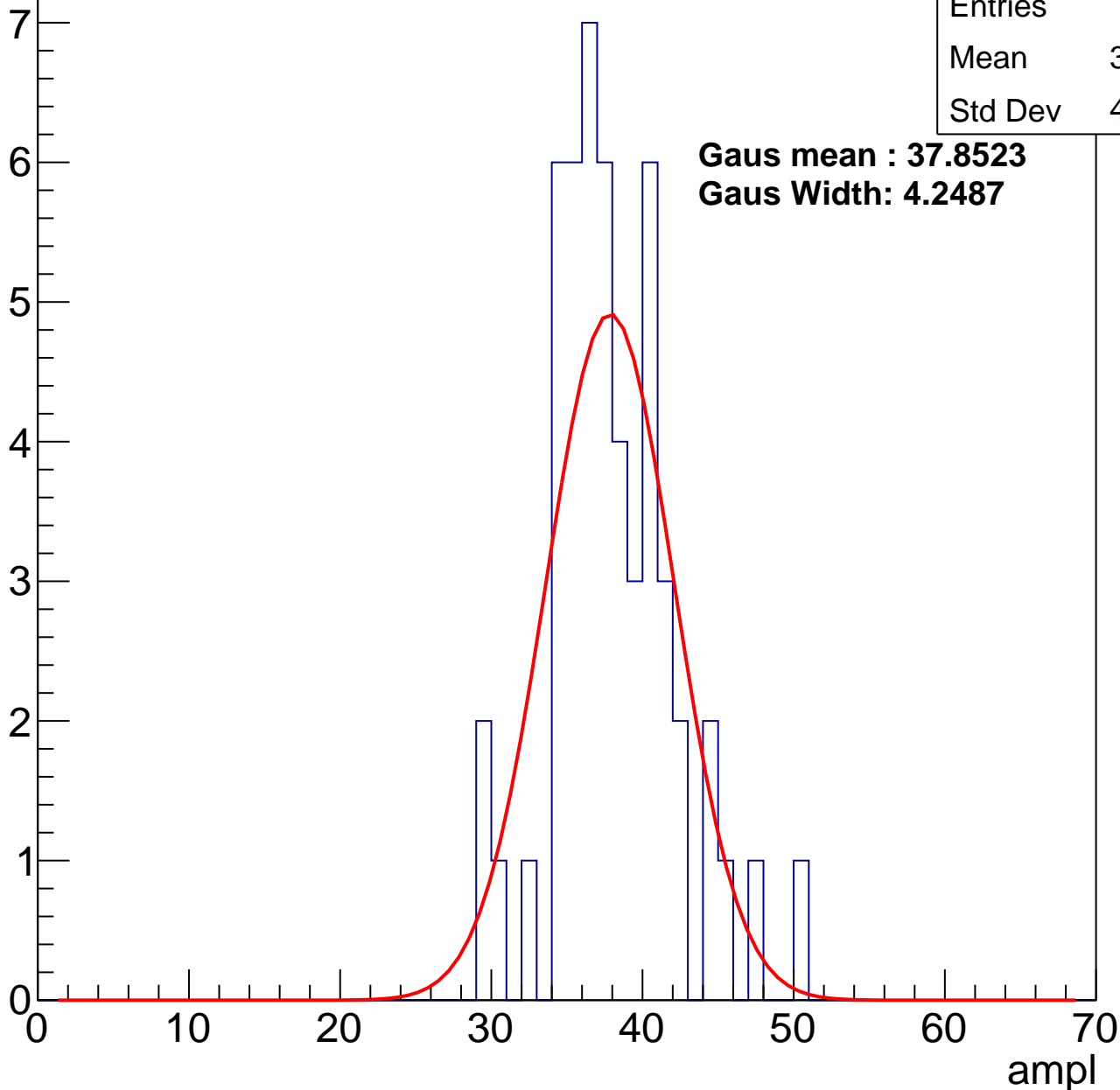
# B1L003S, U18-ch77, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	52
Mean	37.58
Std Dev	4.087

**Gaus mean : 37.8523**  
**Gaus Width: 4.2487**



# B1L003S, U18-ch77, adc2

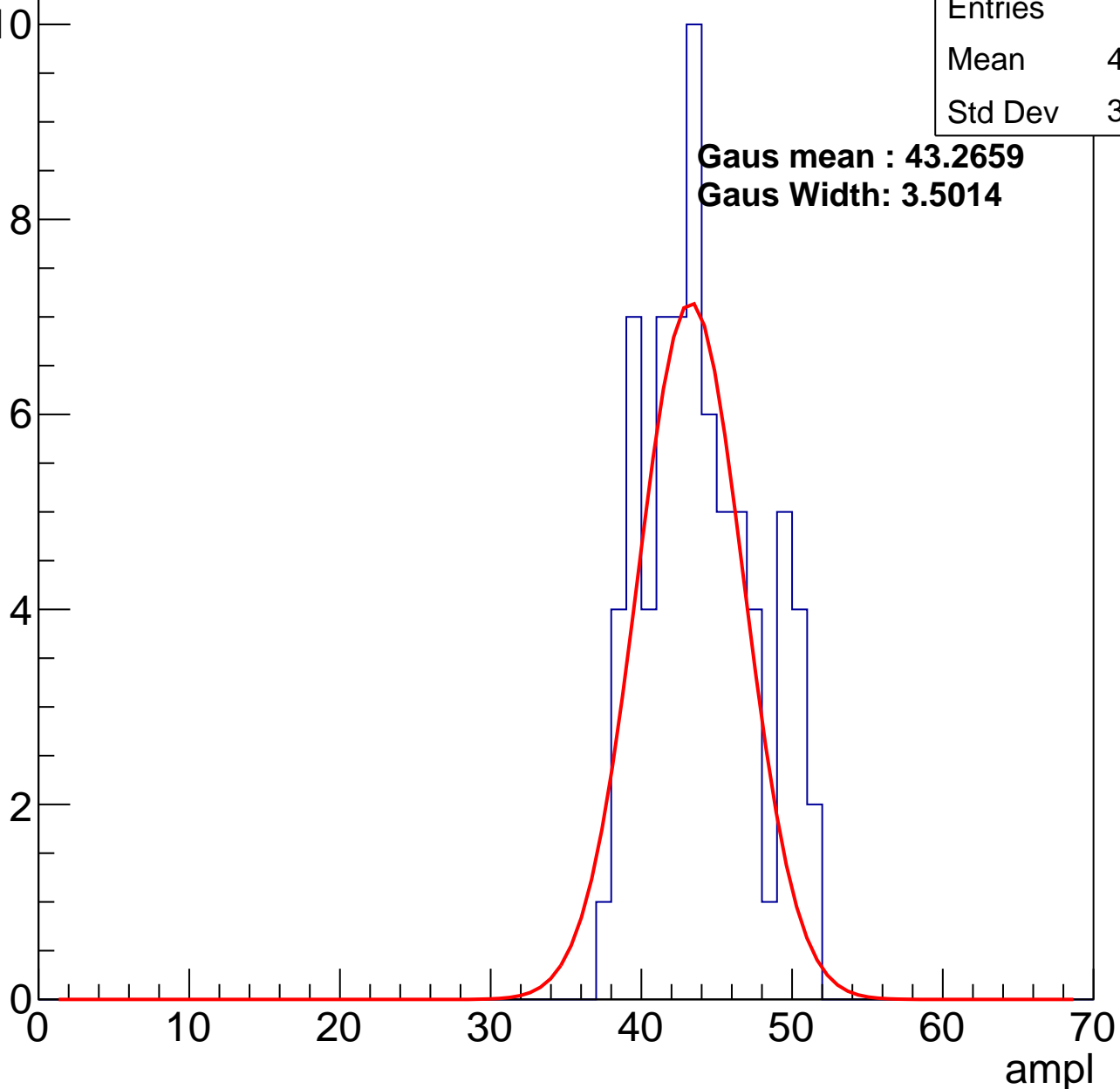
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	72
Mean	43.54
Std Dev	3.655

**Gaus mean : 43.2659**

**Gaus Width: 3.5014**

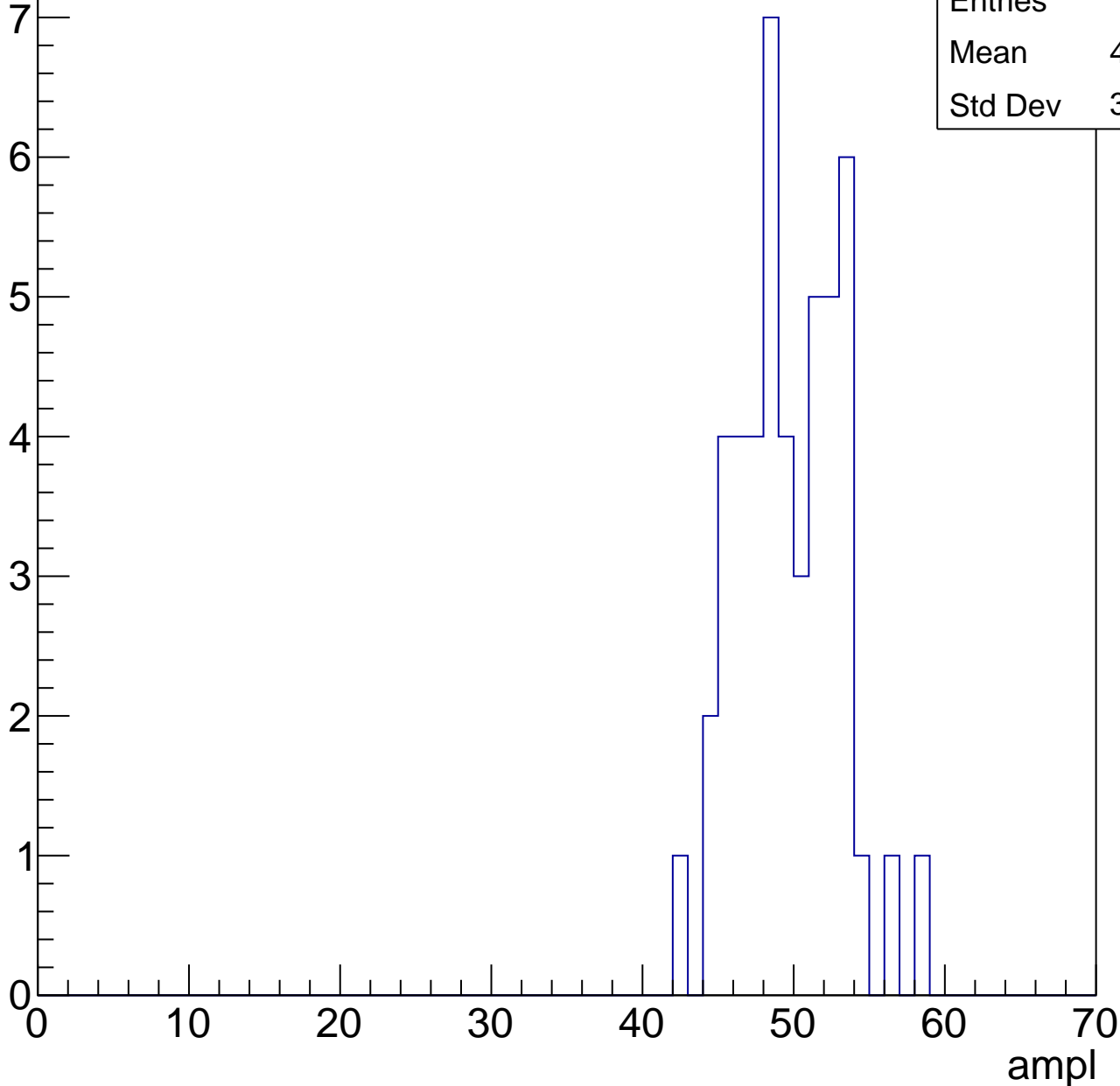


# B1L003S, U18-ch77, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	48
Mean	49.27
Std Dev	3.346

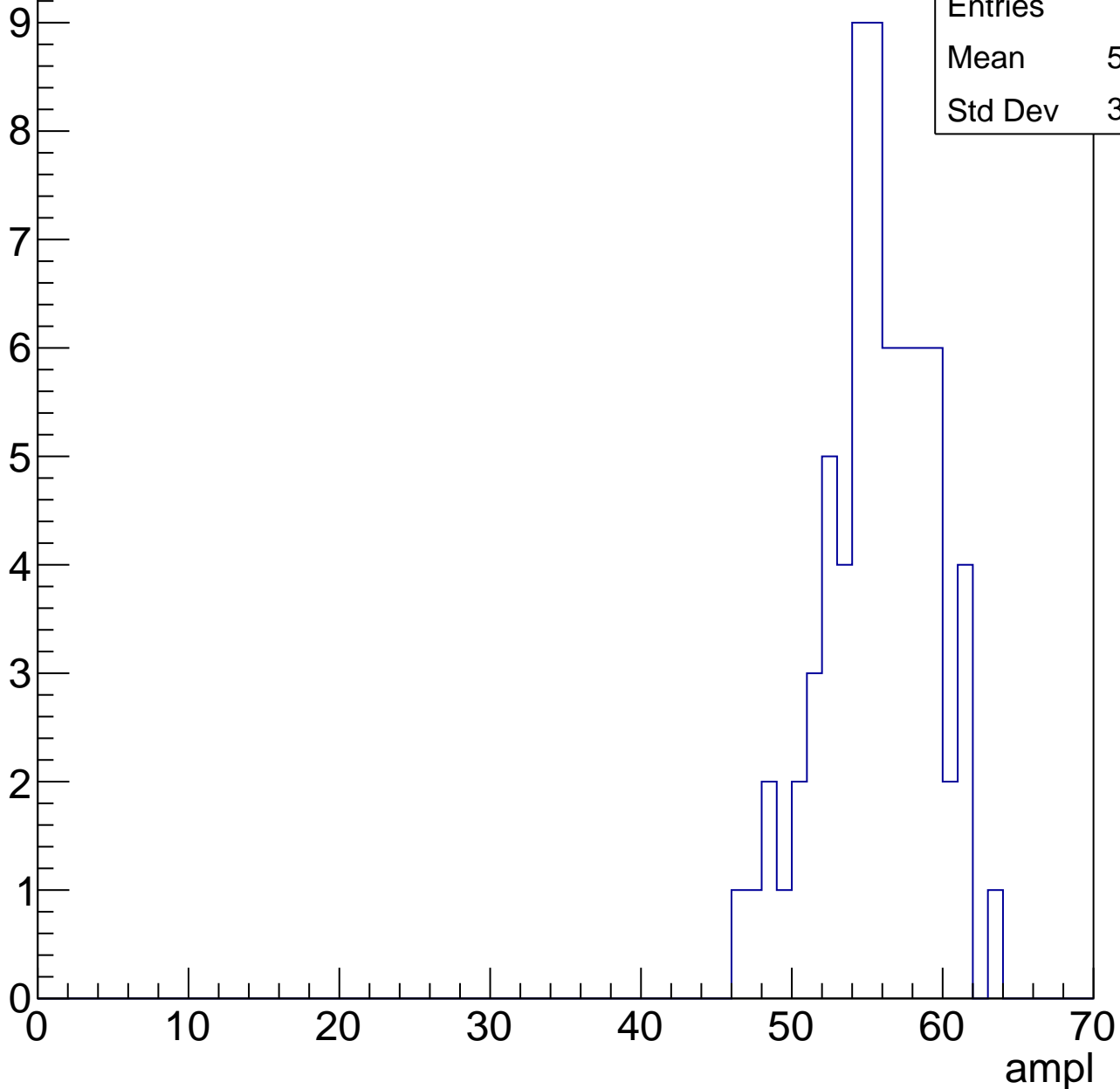


# B1L003S, U18-ch77, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	68
Mean	55.16
Std Dev	3.604

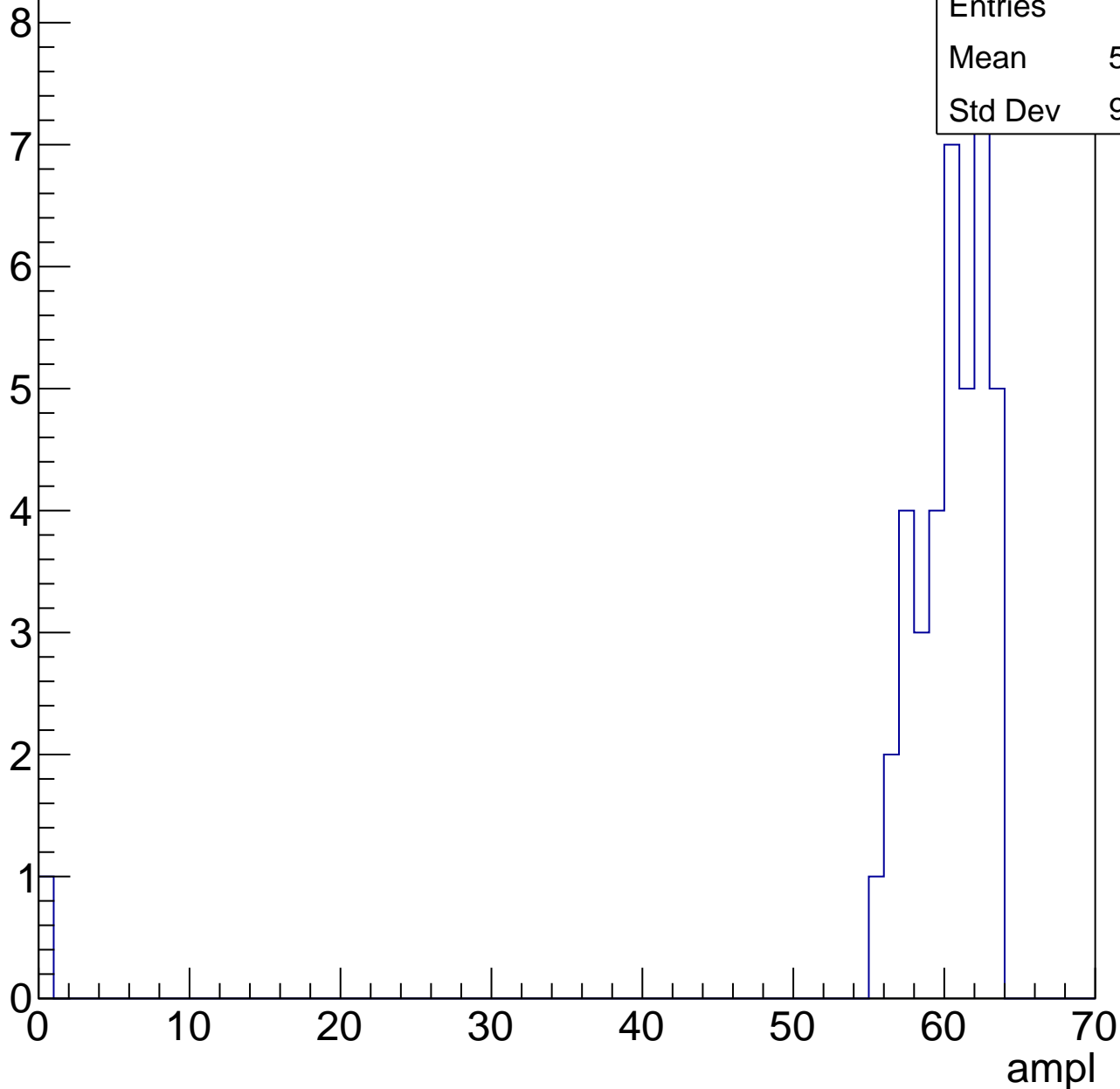


# B1L003S, U18-ch77, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

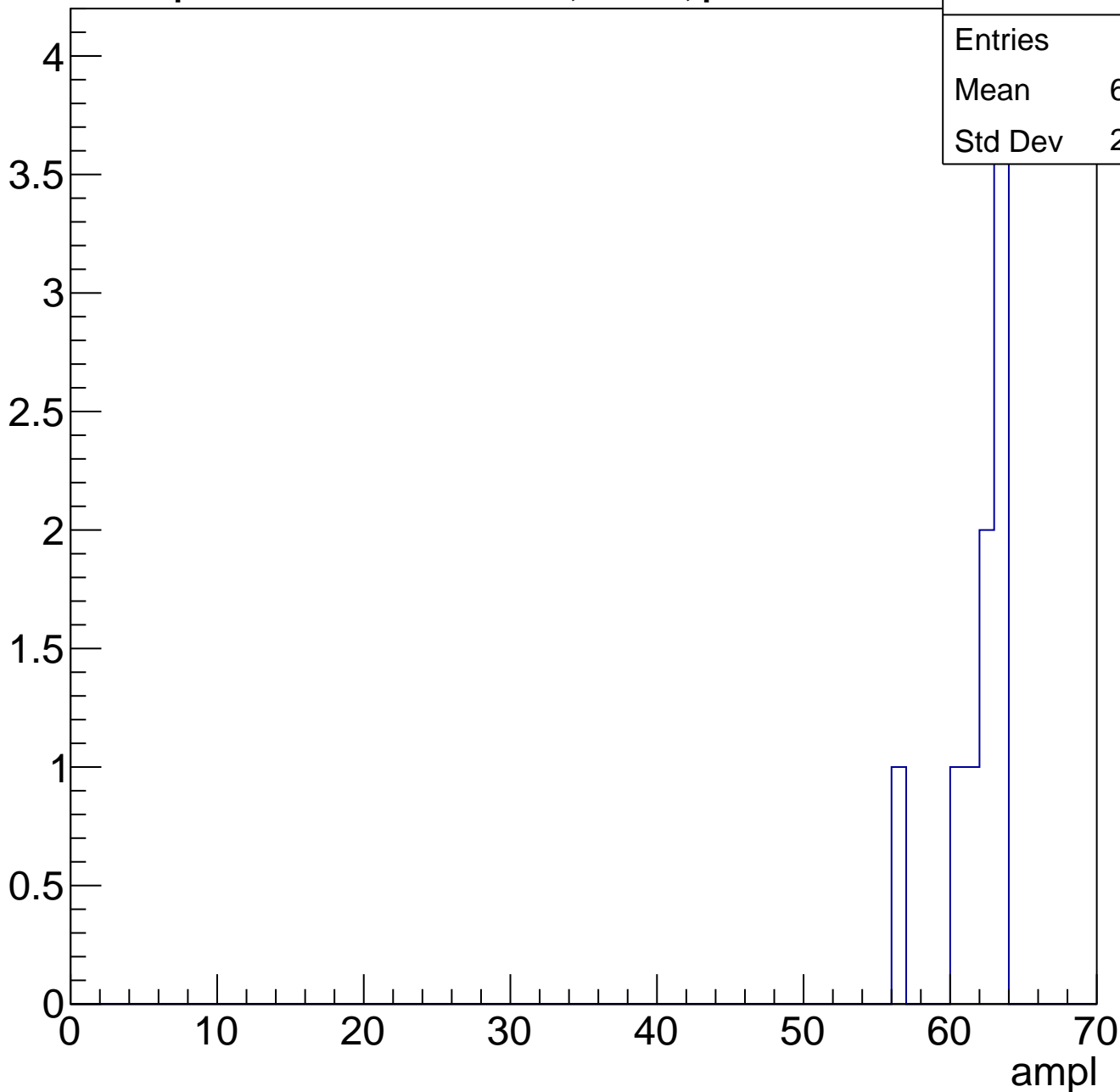
Entries	40
Mean	58.52
Std Dev	9.623



# B1L003S, U18-ch77, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U18-ch77, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L003S, U18-ch78, adc0

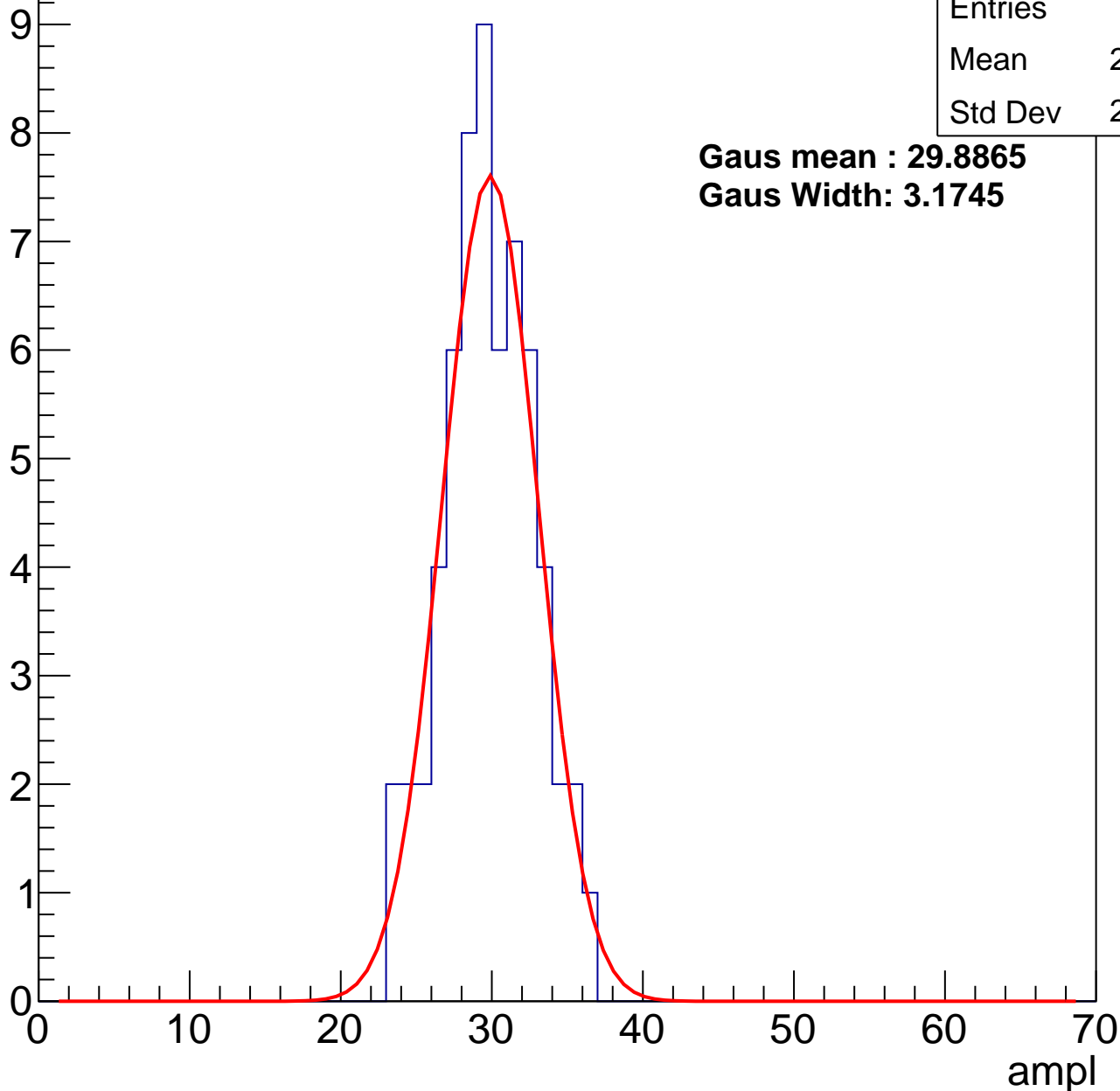
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	61
Mean	29.34
Std Dev	2.969

**Gaus mean : 29.8865**

**Gaus Width: 3.1745**



# B1L003S, U18-ch78, adc1

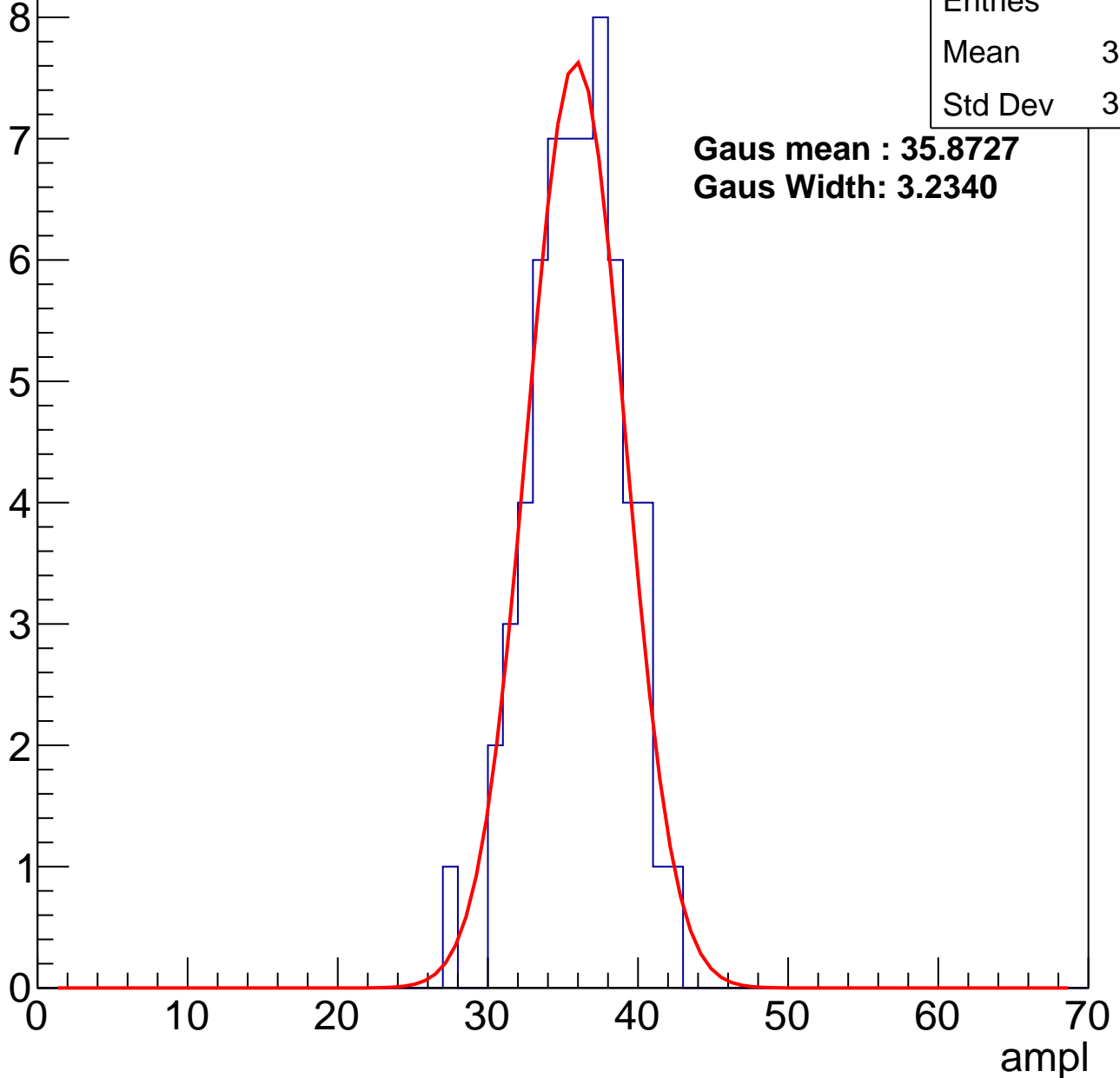
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	61
Mean	35.48
Std Dev	3.022

**Gaus mean : 35.8727**

**Gaus Width: 3.2340**



# B1L003S, U18-ch78, adc2

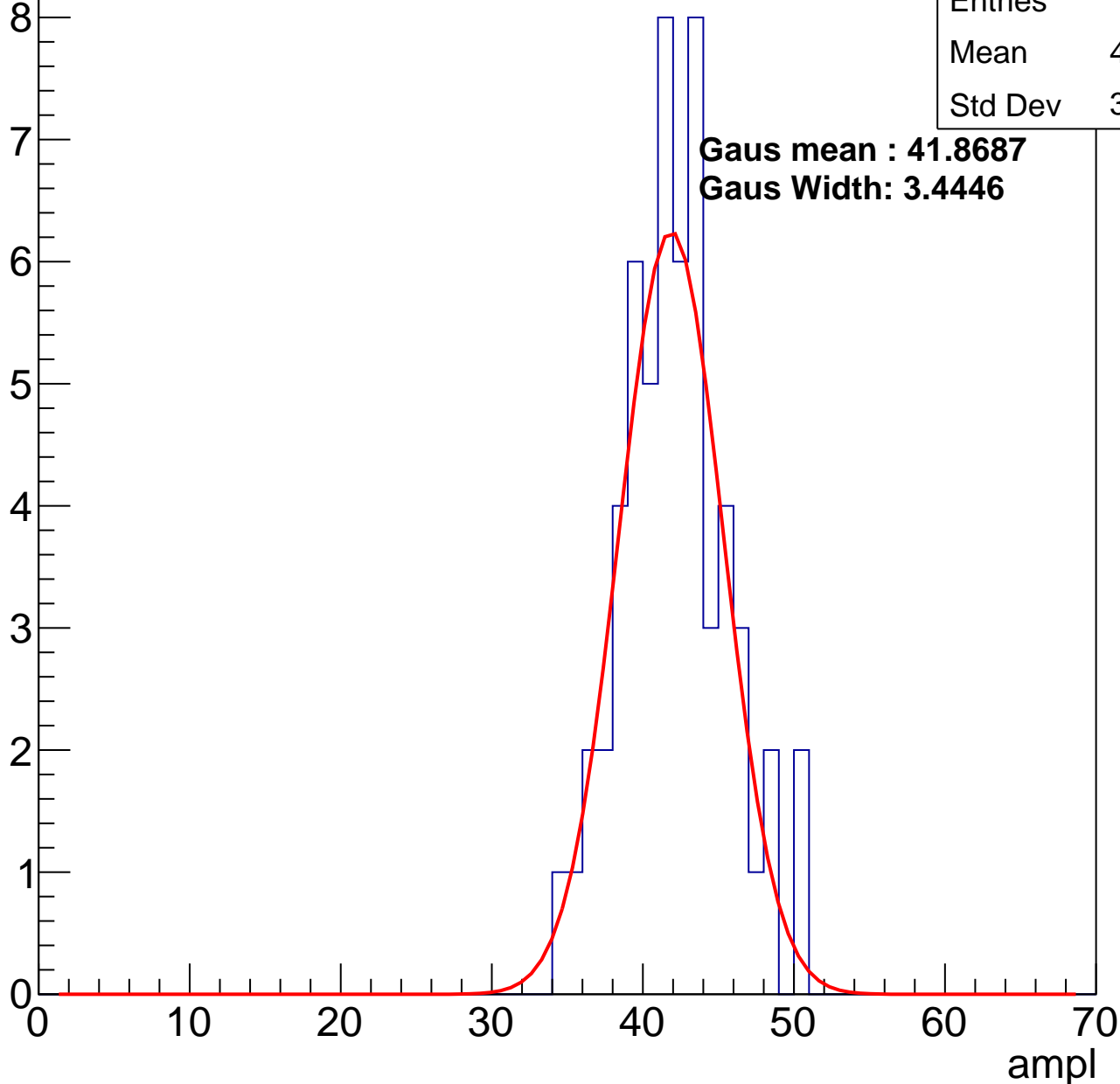
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	58
Mean	41.69
Std Dev	3.485

**Gaus mean : 41.8687**

**Gaus Width: 3.4446**

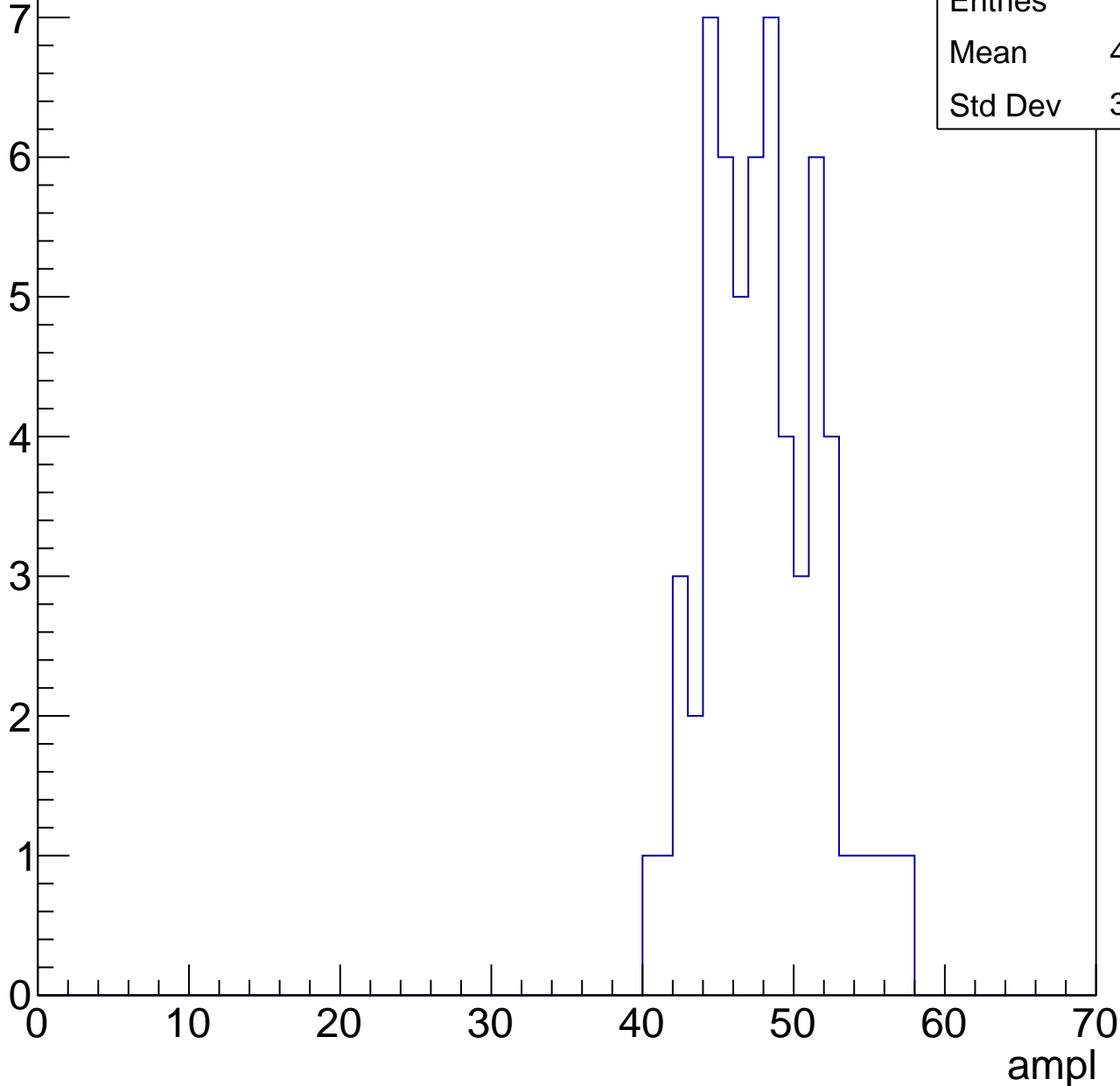


# B1L003S, U18-ch78, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	60
Mean	47.57
Std Dev	3.743

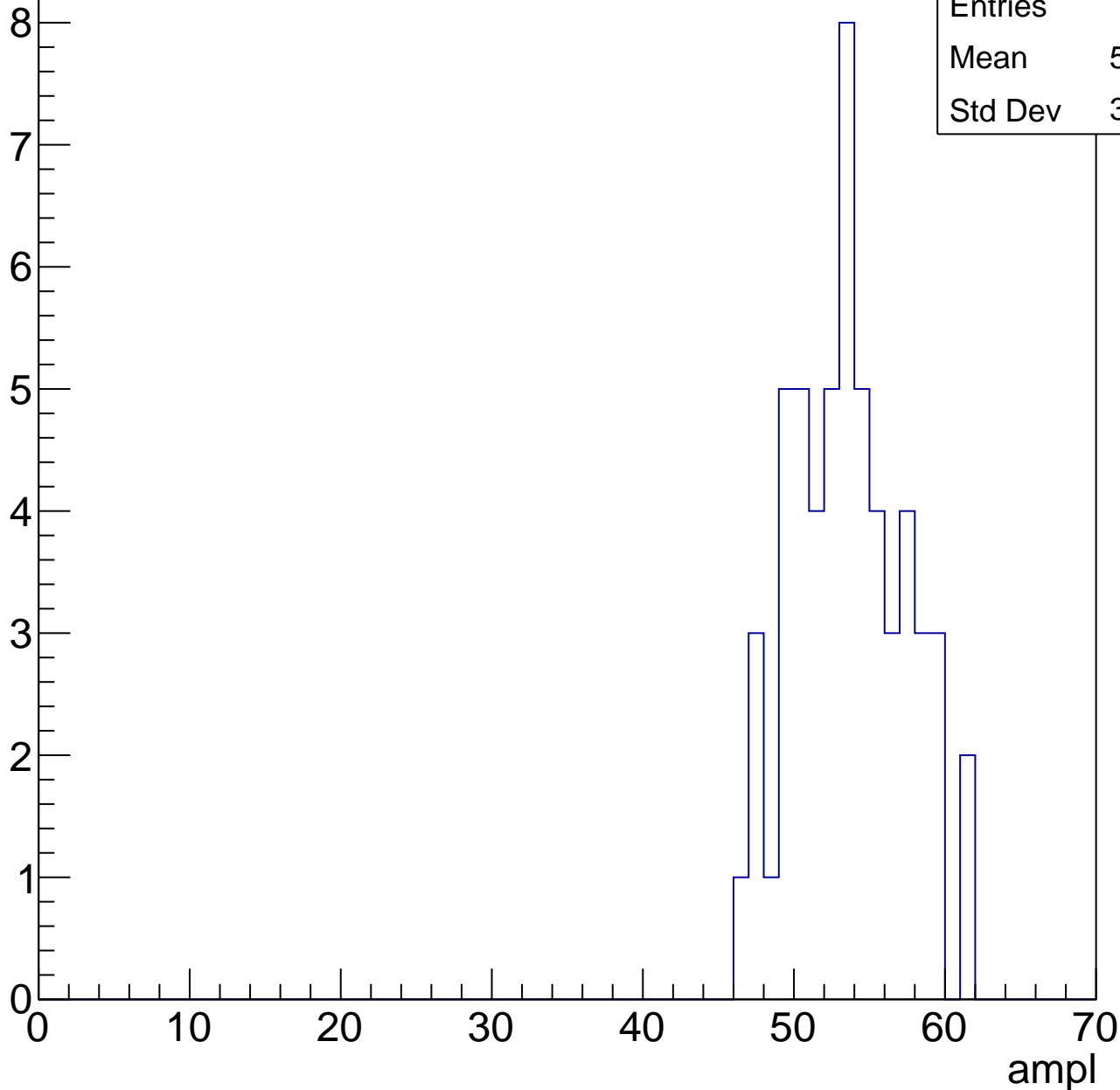


# B1L003S, U18-ch78, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	56
Mean	53.16
Std Dev	3.659

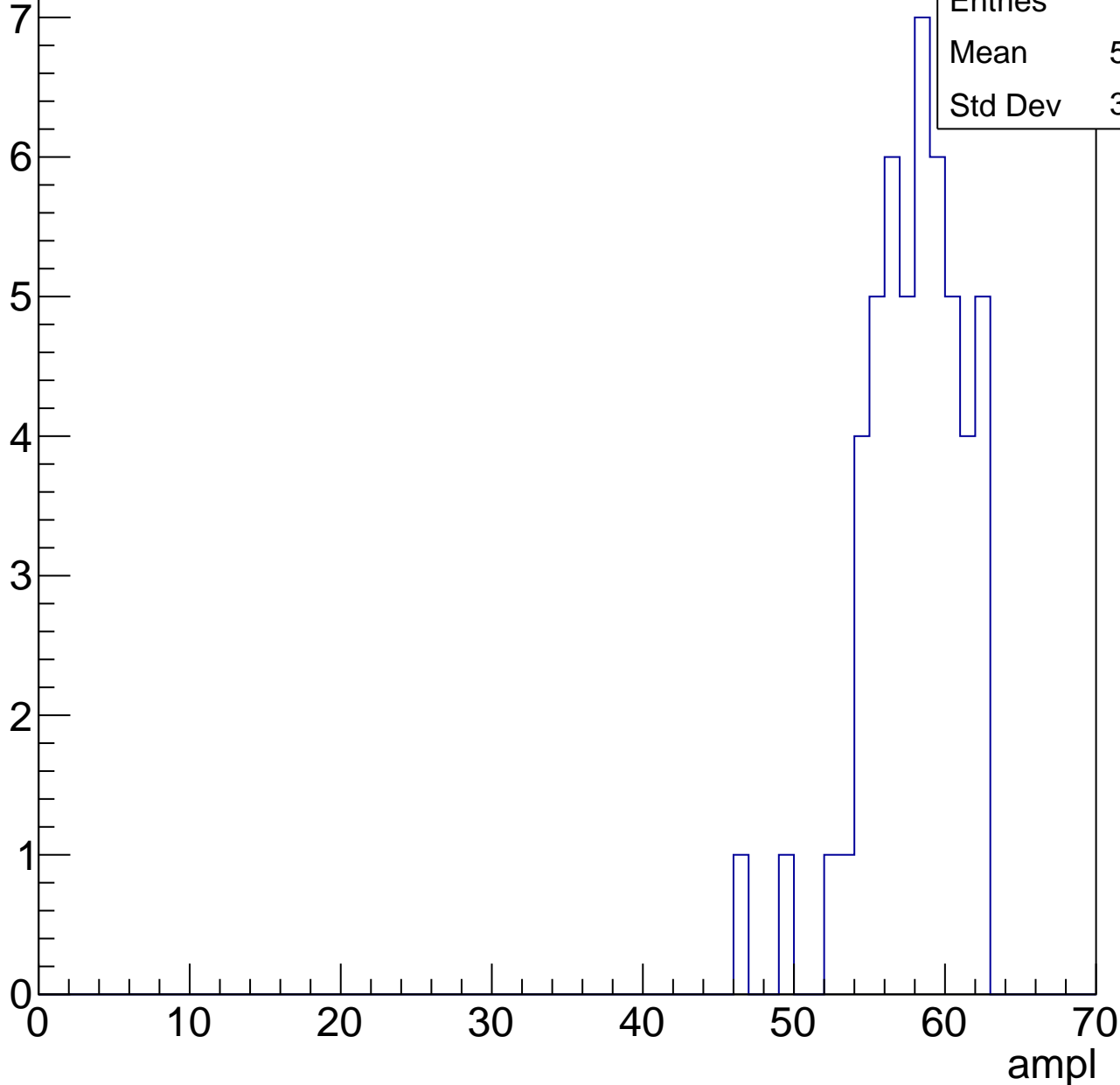


# B1L003S, U18-ch78, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	51
Mean	57.37
Std Dev	3.272

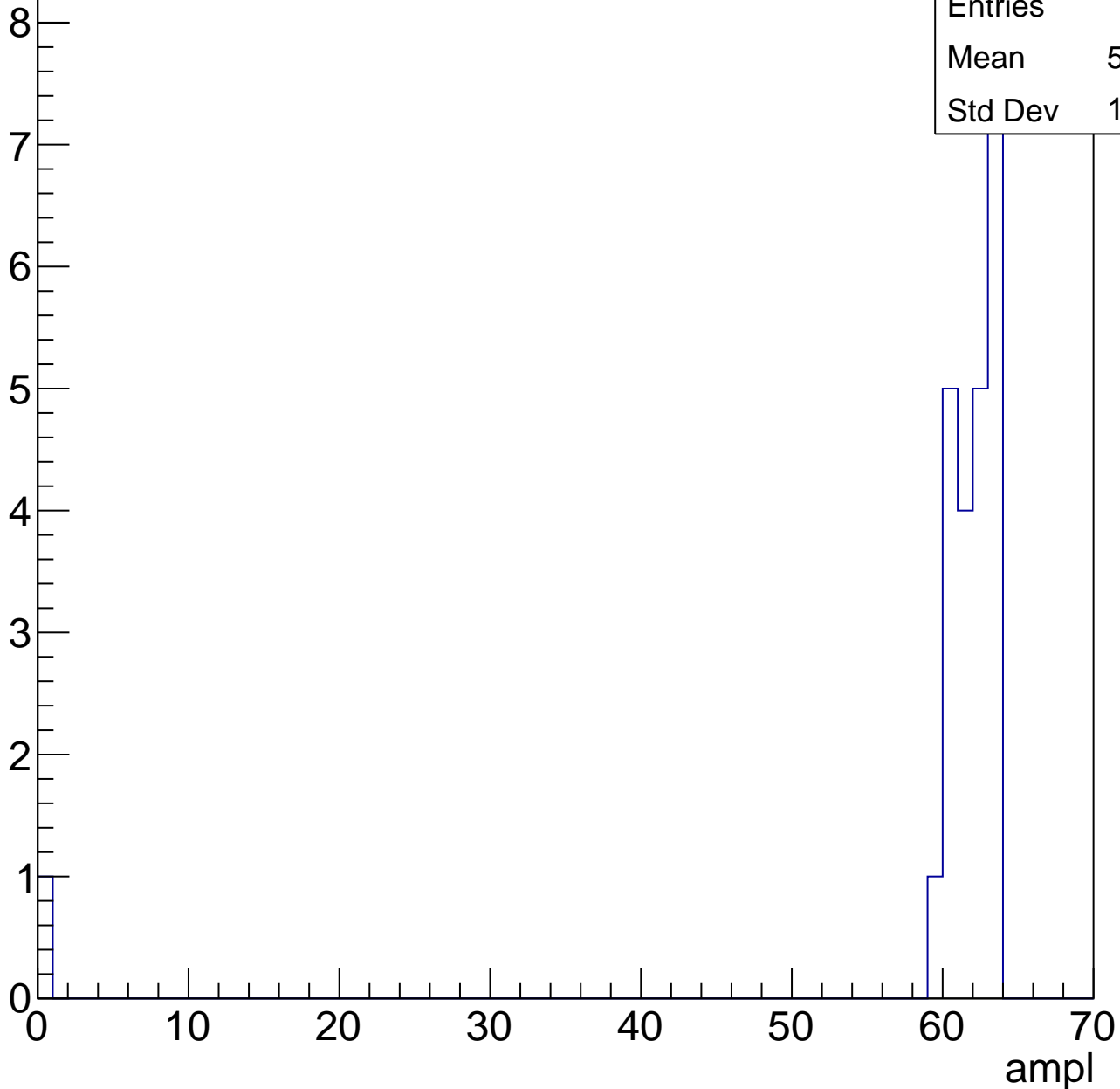


# B1L003S, U18-ch78, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	24
Mean	59.04
Std Dev	12.37





# B1L003S, U18-ch78, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U18-ch79, adc0

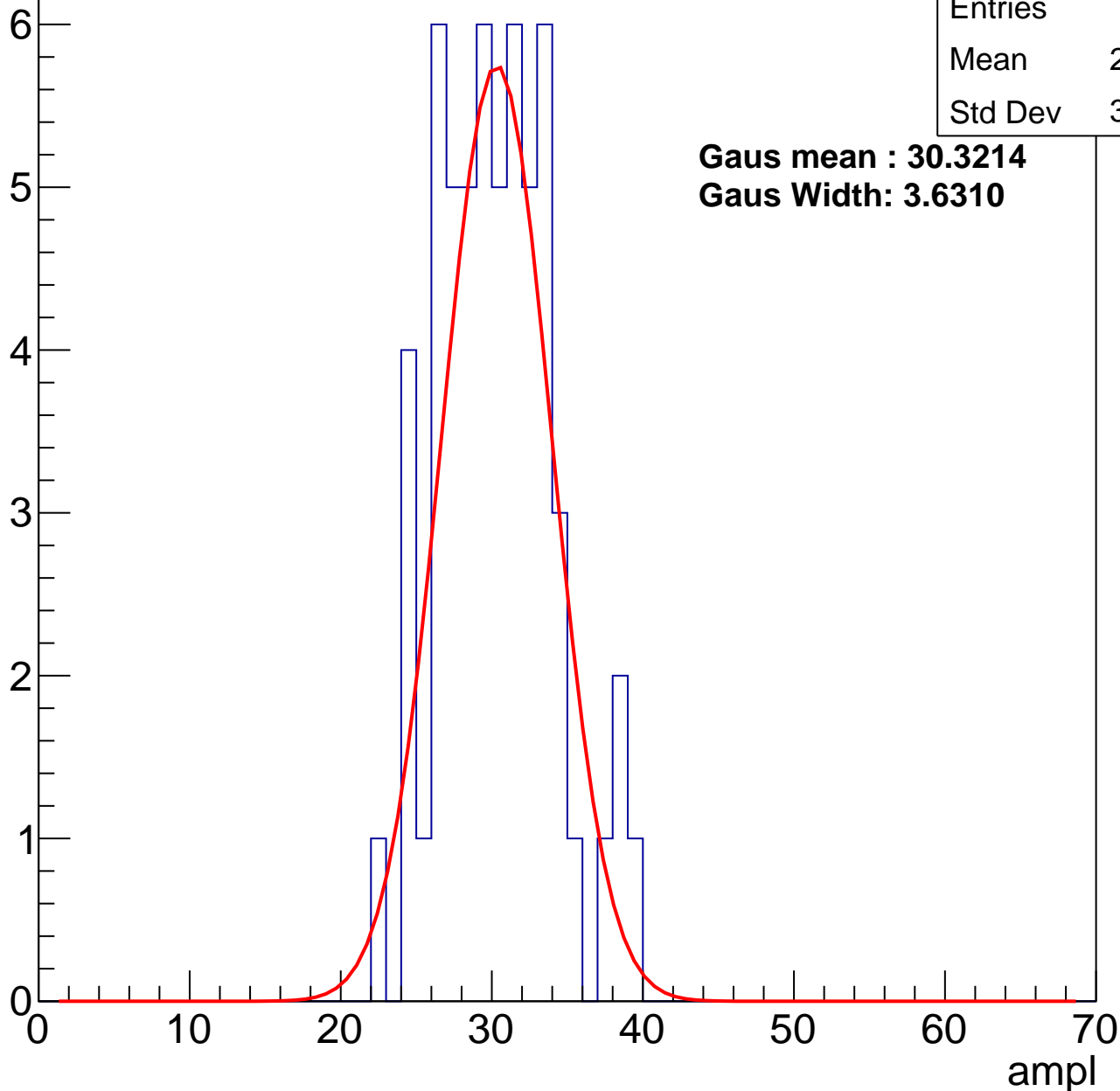
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	58
Mean	29.84
Std Dev	3.736

**Gaus mean : 30.3214**

**Gaus Width: 3.6310**



# B1L003S, U18-ch79, adc1

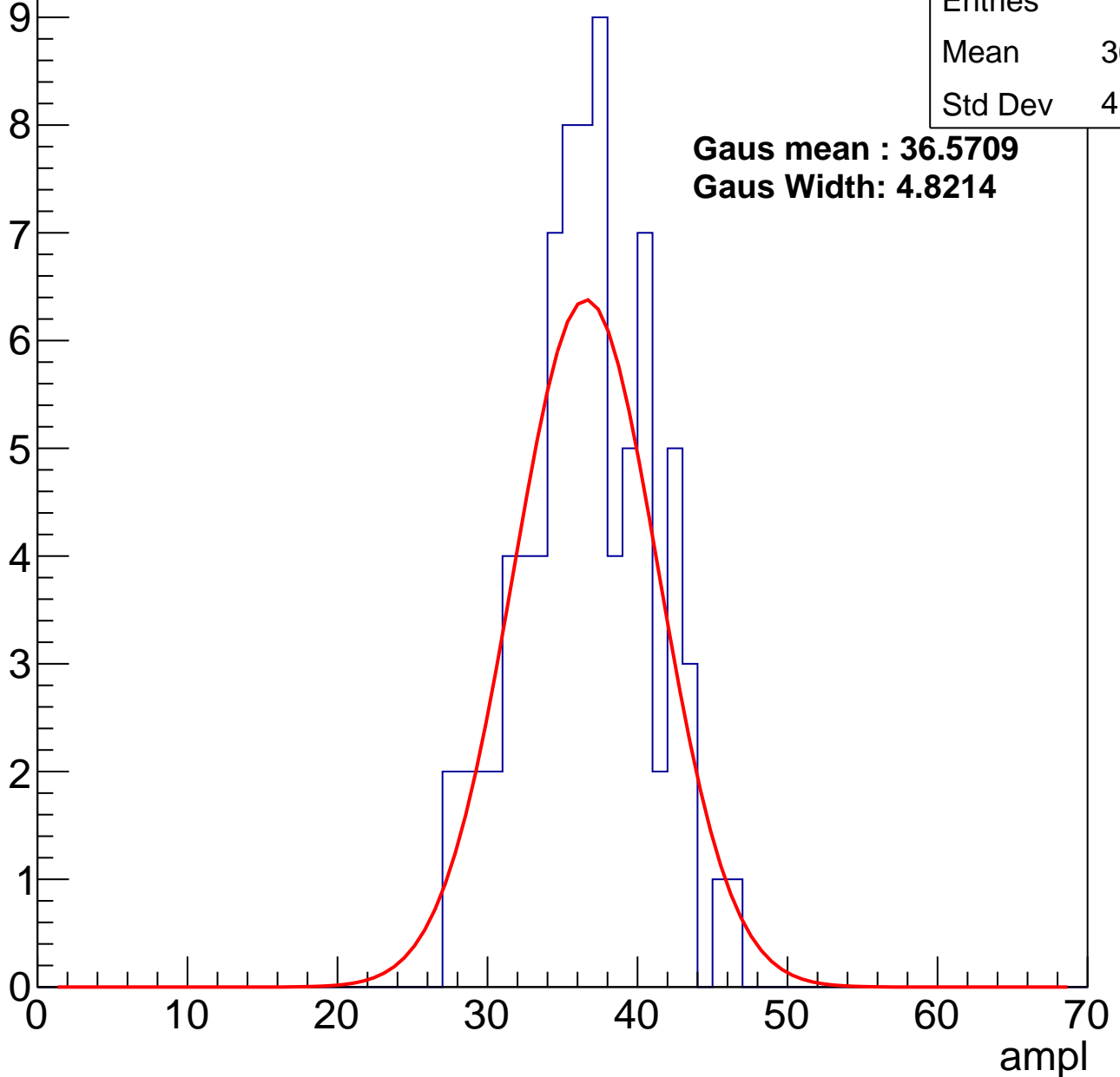
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	80
Mean	36.12
Std Dev	4.235

**Gaus mean : 36.5709**

**Gaus Width: 4.8214**



# B1L003S, U18-ch79, adc2

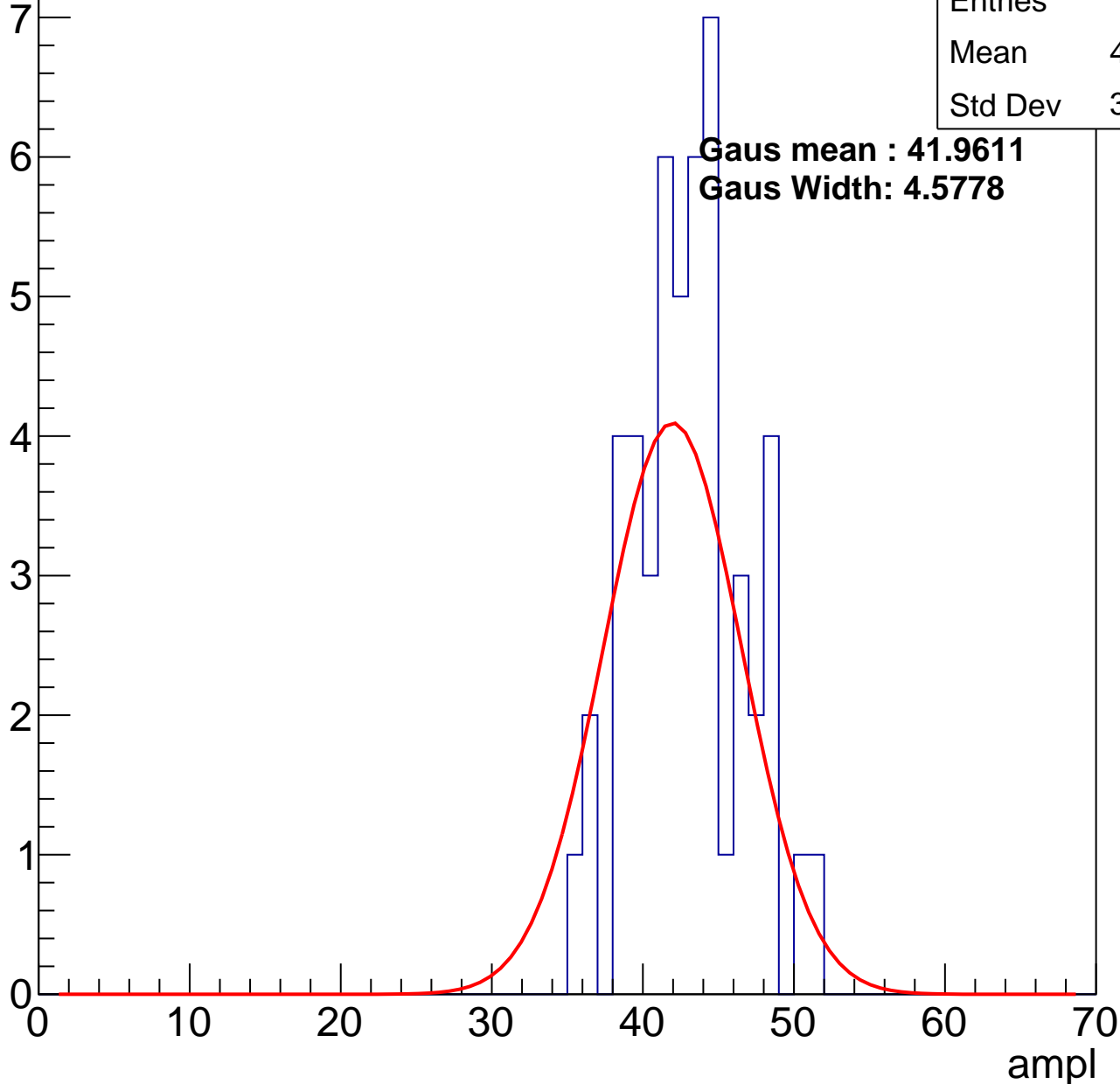
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	50
Mean	42.54
Std Dev	3.618

**Gaus mean : 41.9611**

**Gaus Width: 4.5778**

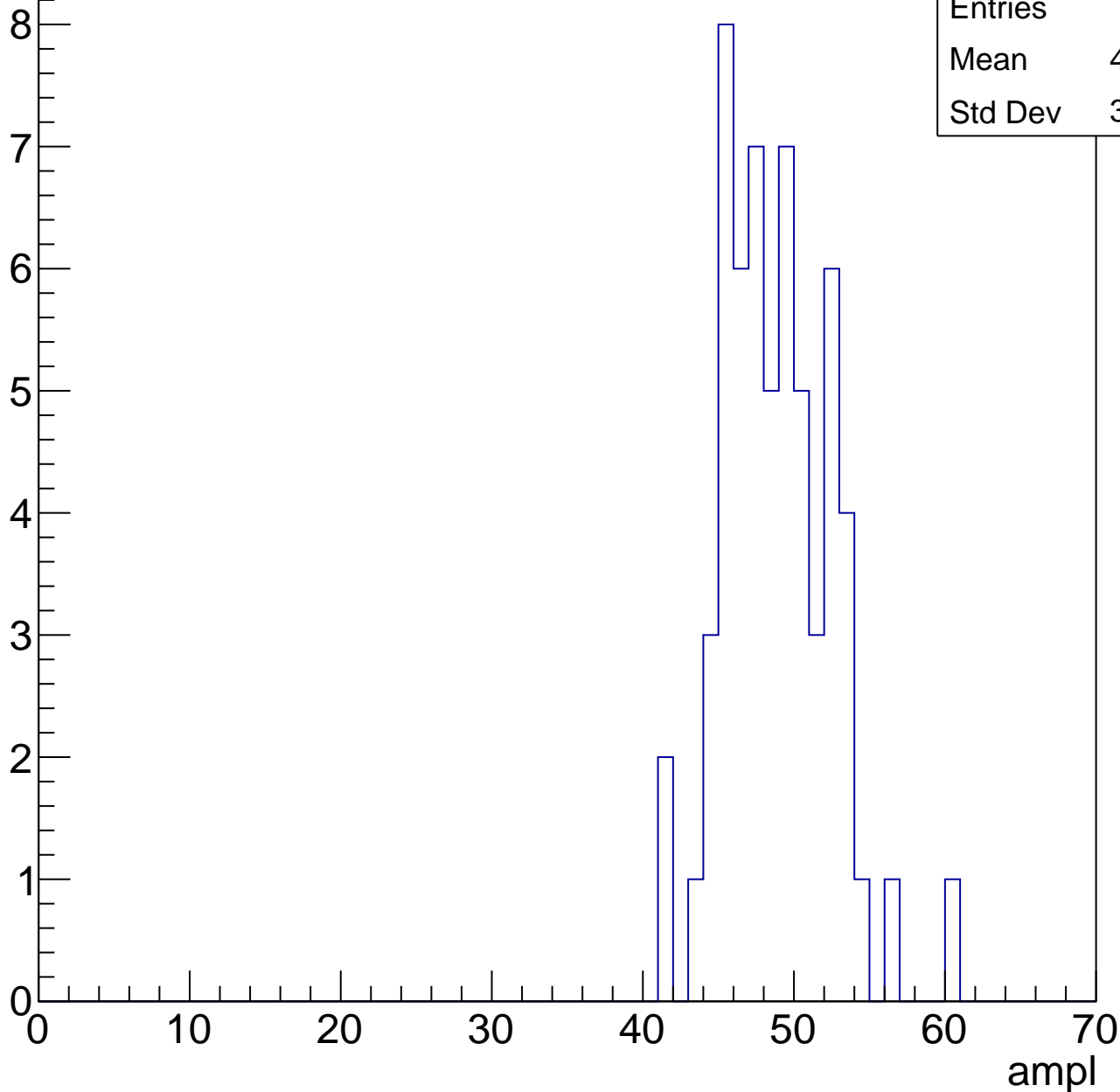


# B1L003S, U18-ch79, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	60
Mean	48.37
Std Dev	3.559

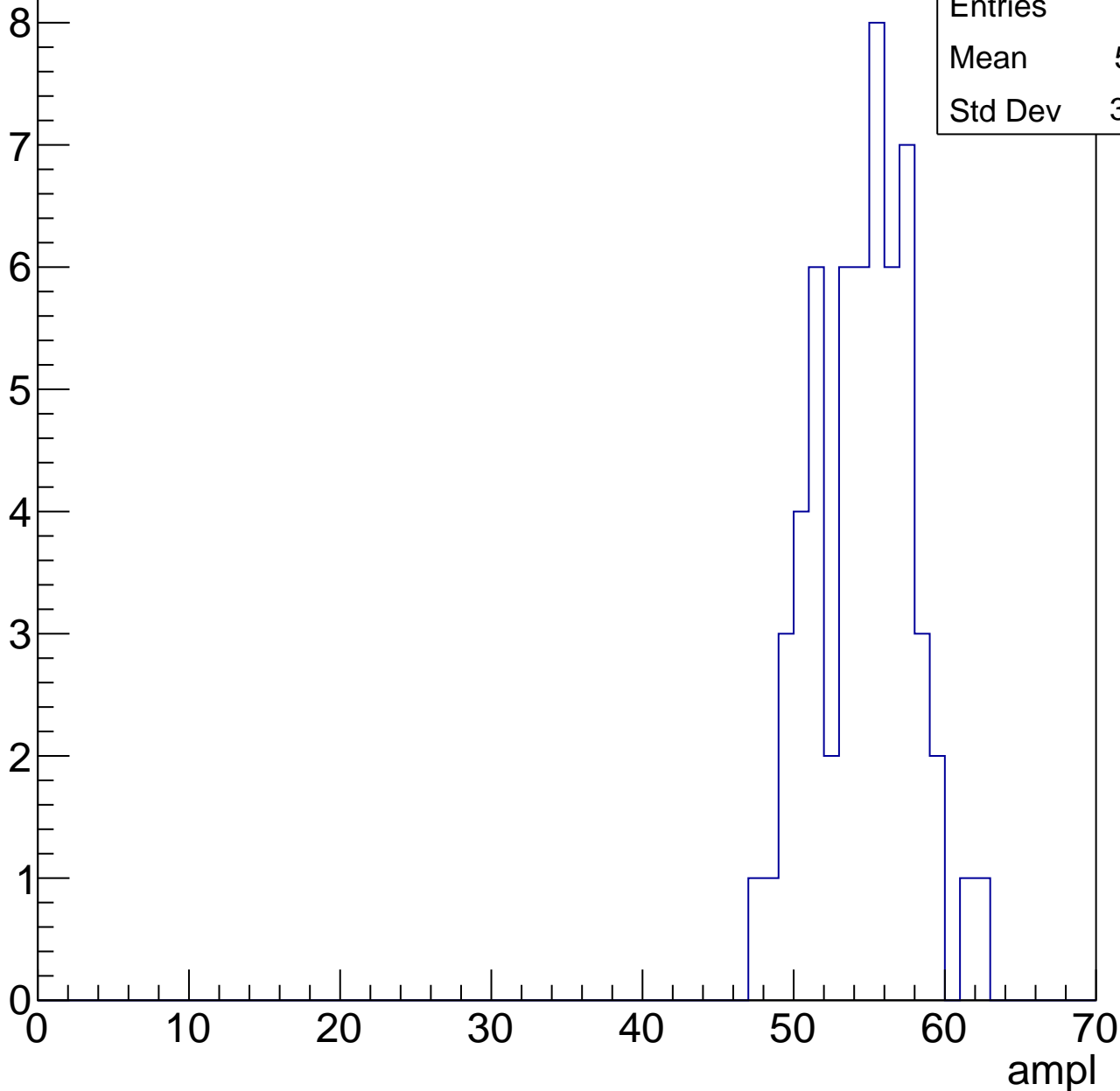


# B1L003S, U18-ch79, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

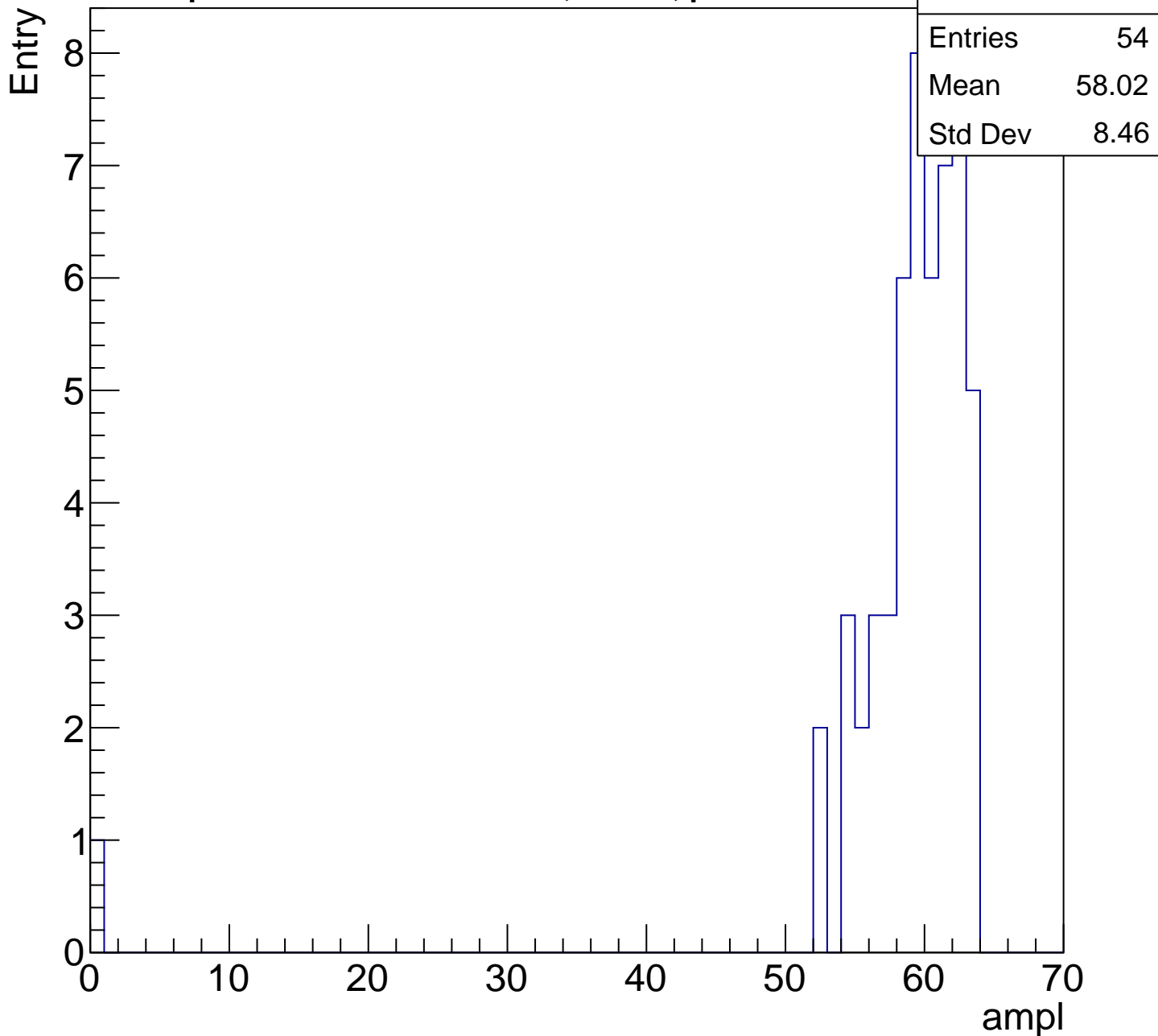
Entry

Entries	57
Mean	54.11
Std Dev	3.237



# B1L003S, U18-ch79, adc5

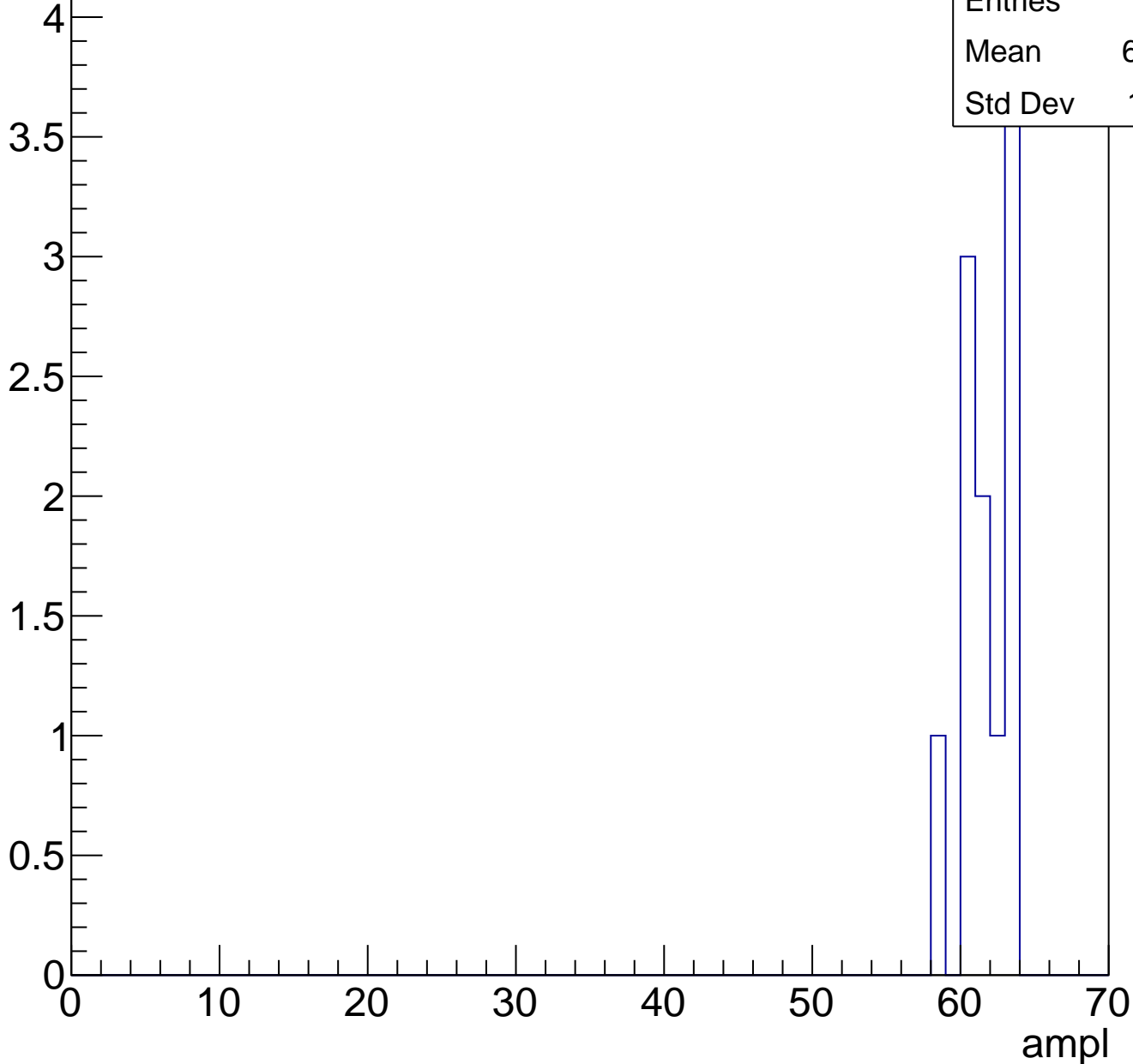
calib\_packv5\_042523\_0143.root, FC#13, port D2



# B1L003S, U18-ch79, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U18-ch79, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	3
Mean	21
Std Dev	29.7

# B1L003S, U18-ch80, adc0

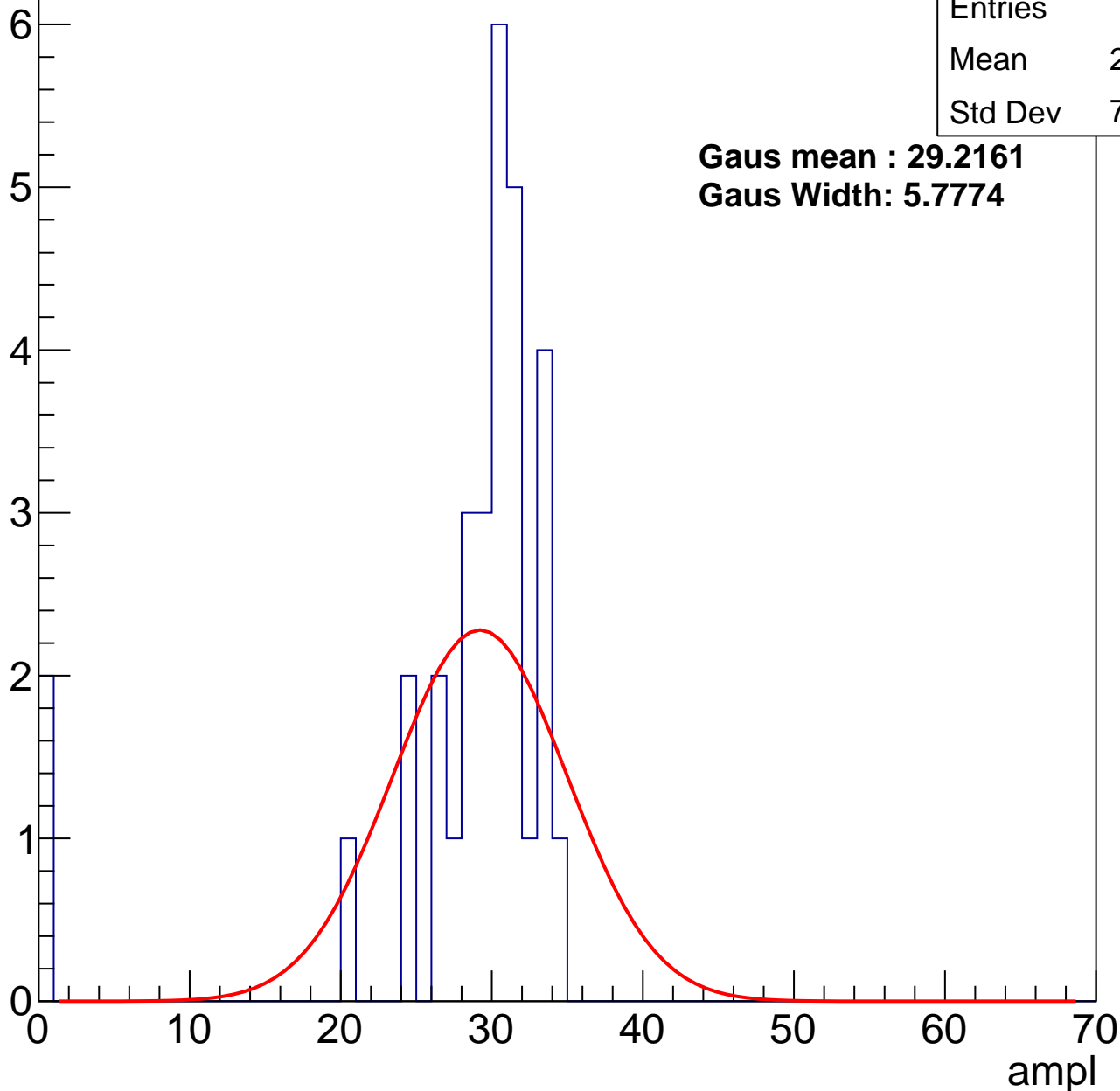
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	31
Mean	27.45
Std Dev	7.803

**Gaus mean : 29.2161**

**Gaus Width: 5.7774**



# B1L003S, U18-ch80, adc1

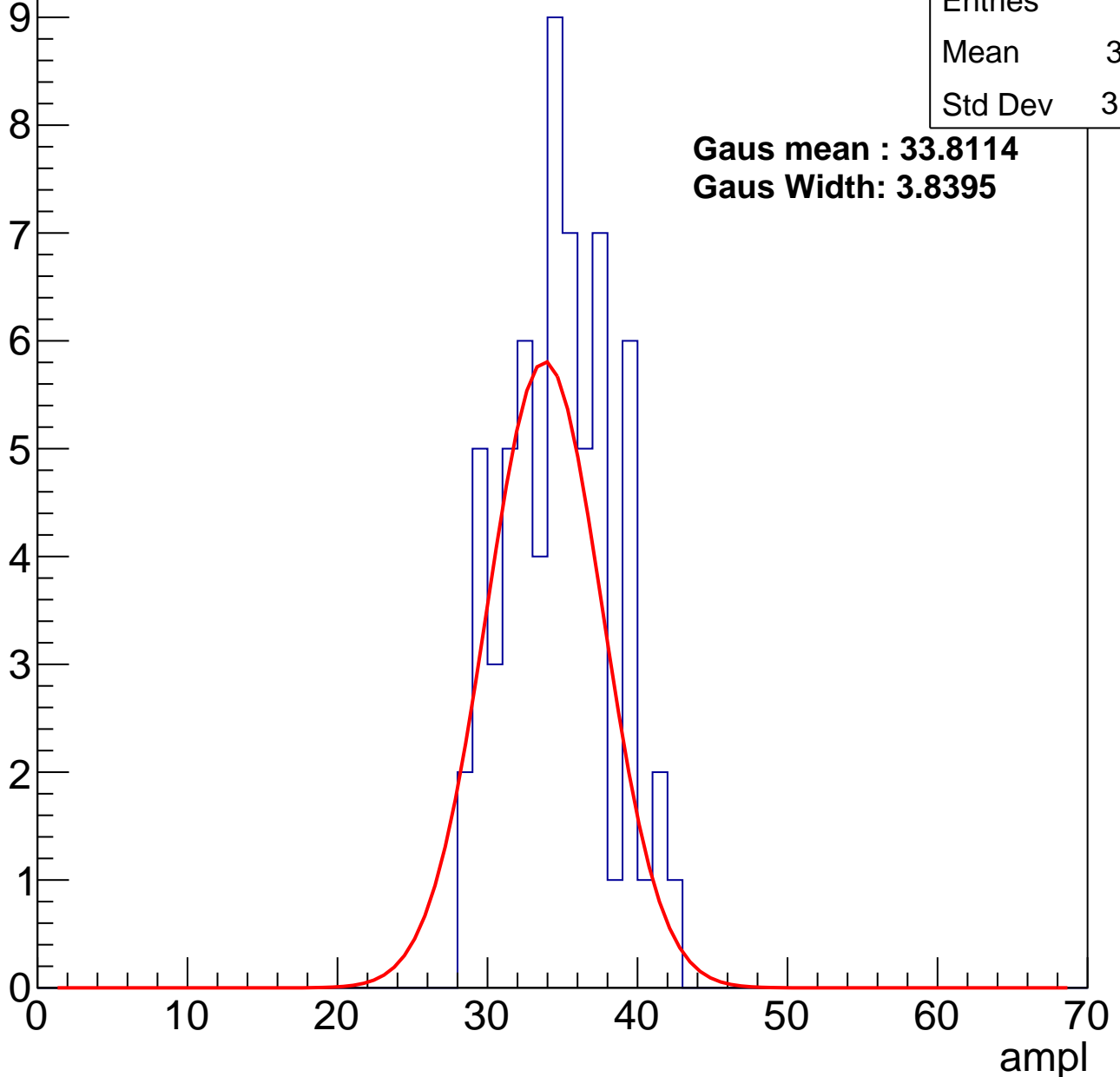
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	64
Mean	34.31
Std Dev	3.459

**Gaus mean : 33.8114**

**Gaus Width: 3.8395**



# B1L003S, U18-ch80, adc2

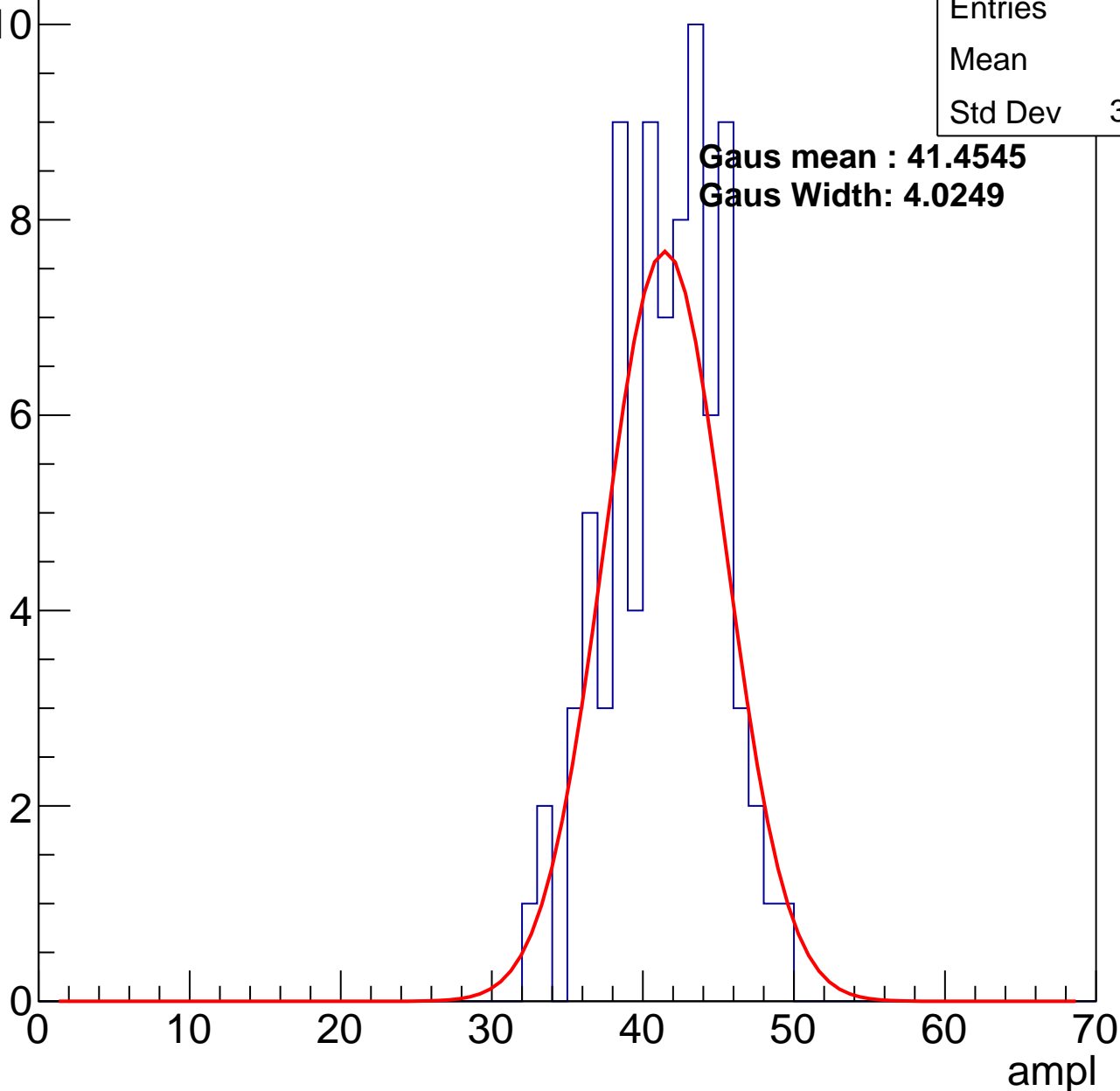
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	83
Mean	41
Std Dev	3.644

**Gaus mean : 41.4545**

**Gaus Width: 4.0249**

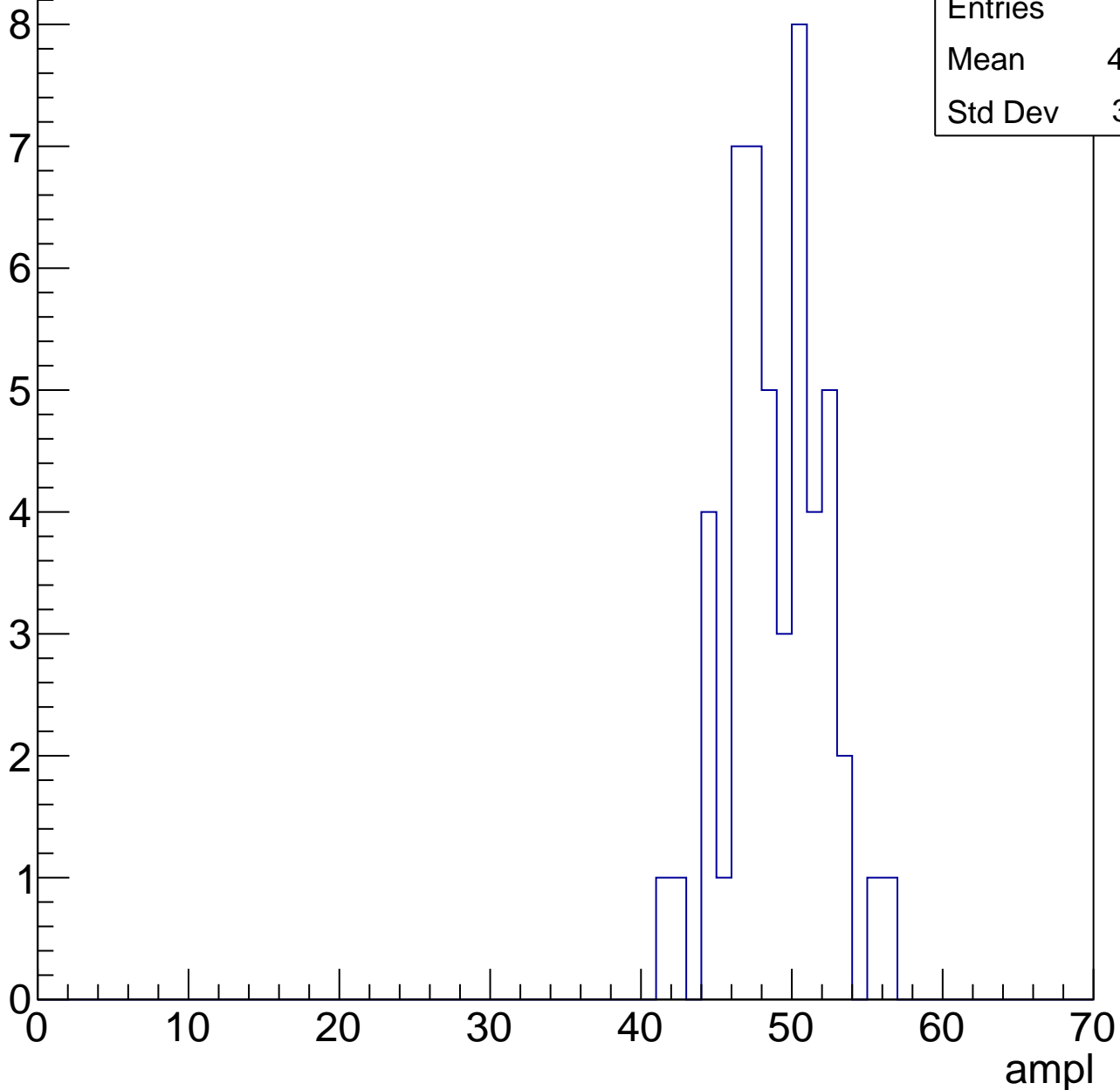


# B1L003S, U18-ch80, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	50
Mean	48.46
Std Dev	3.151

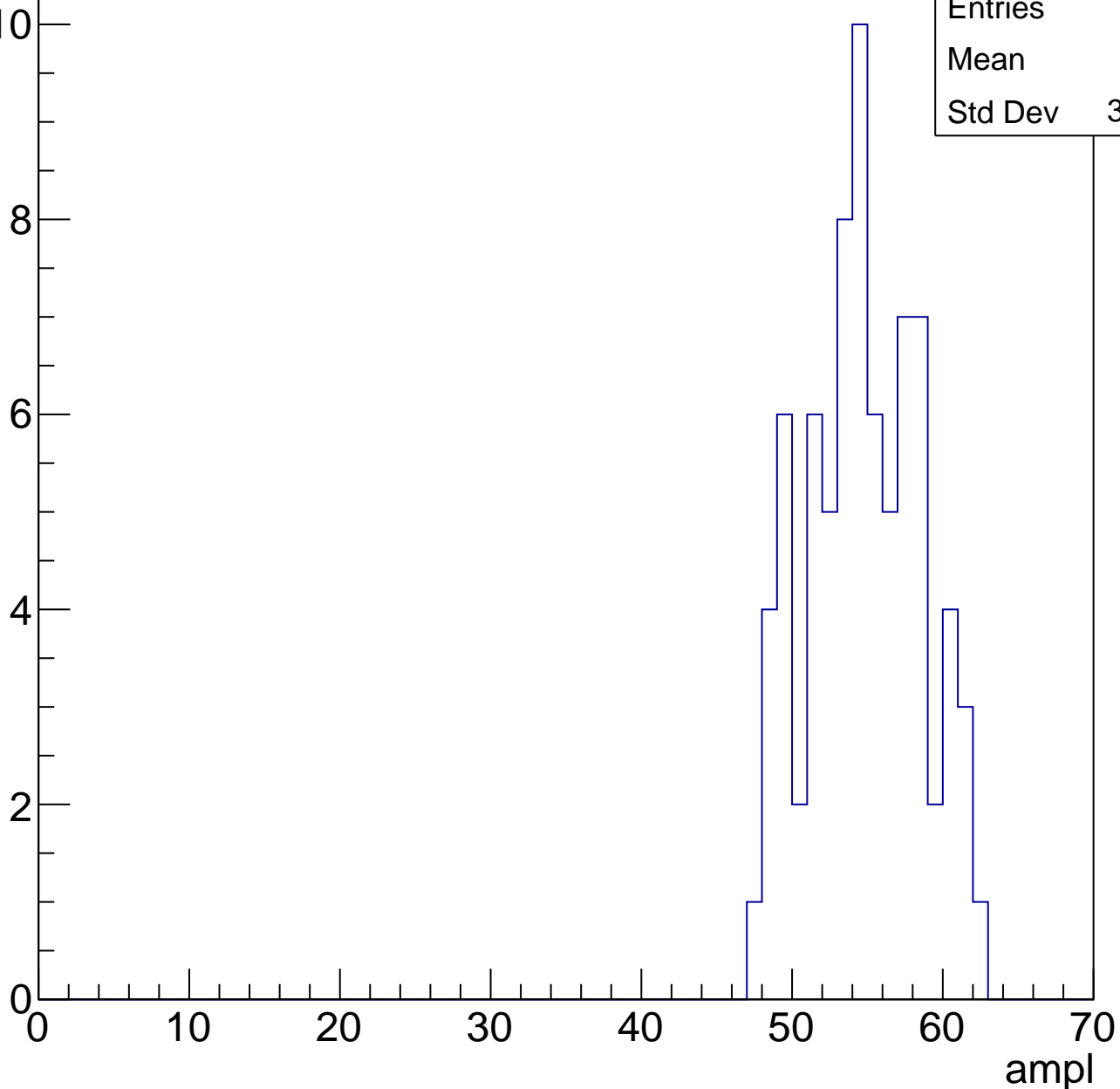


# B1L003S, U18-ch80, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

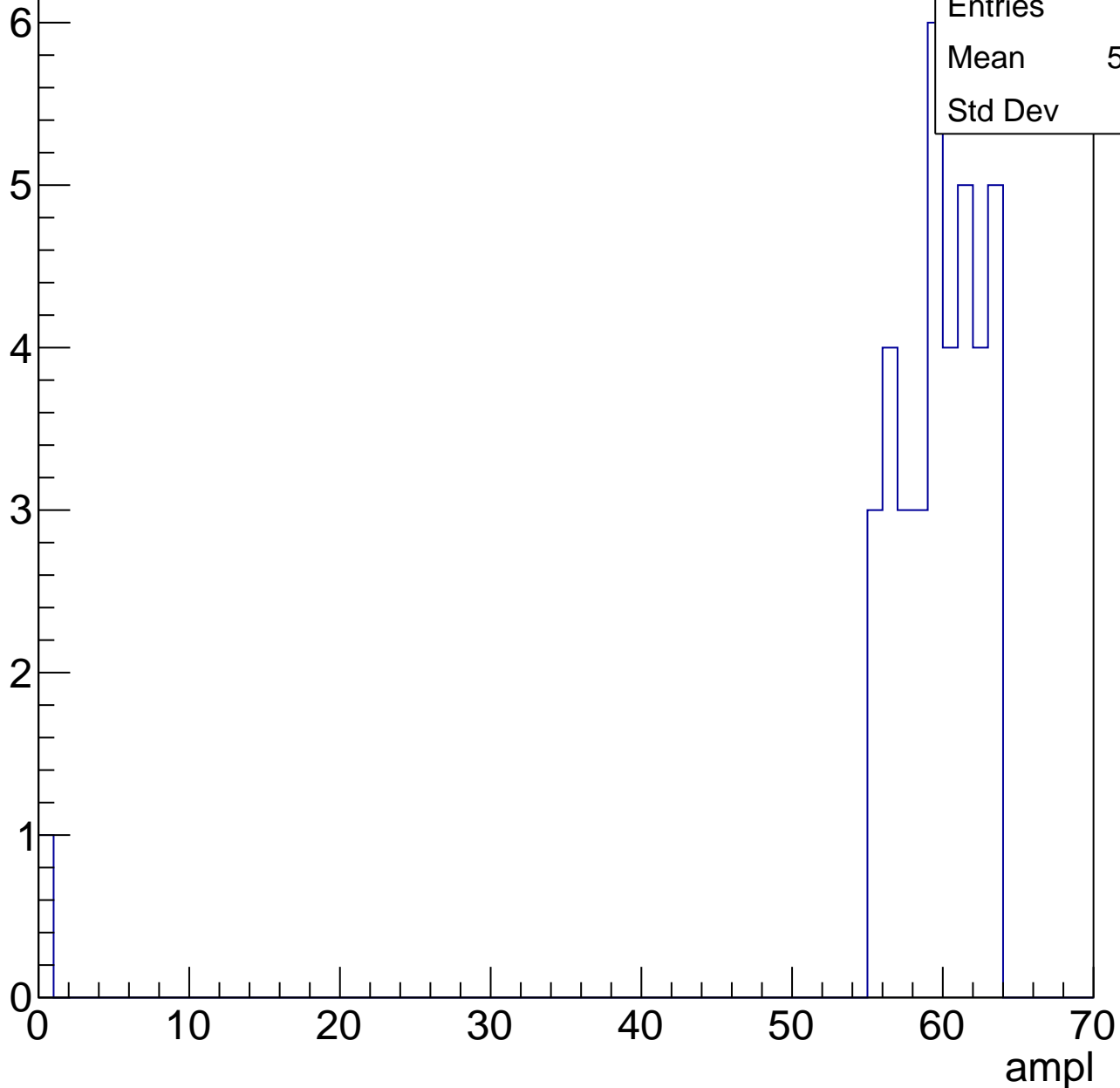
Entries	77
Mean	54.3
Std Dev	3.704



# B1L003S, U18-ch80, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

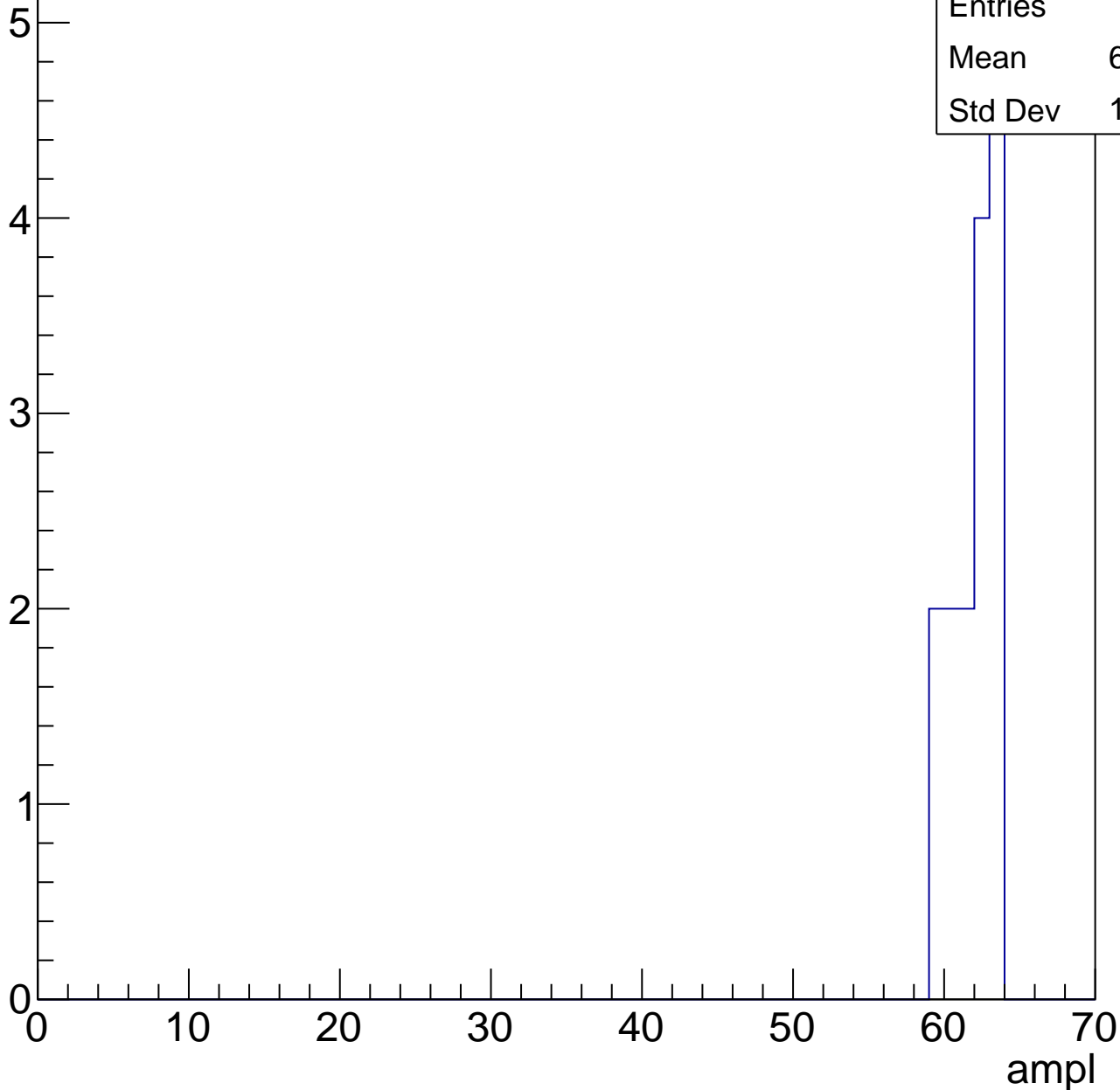


# B1L003S, U18-ch80, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	15
Mean	61.53
Std Dev	1.408





# B1L003S, U18-ch80, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U18-ch81, adc0

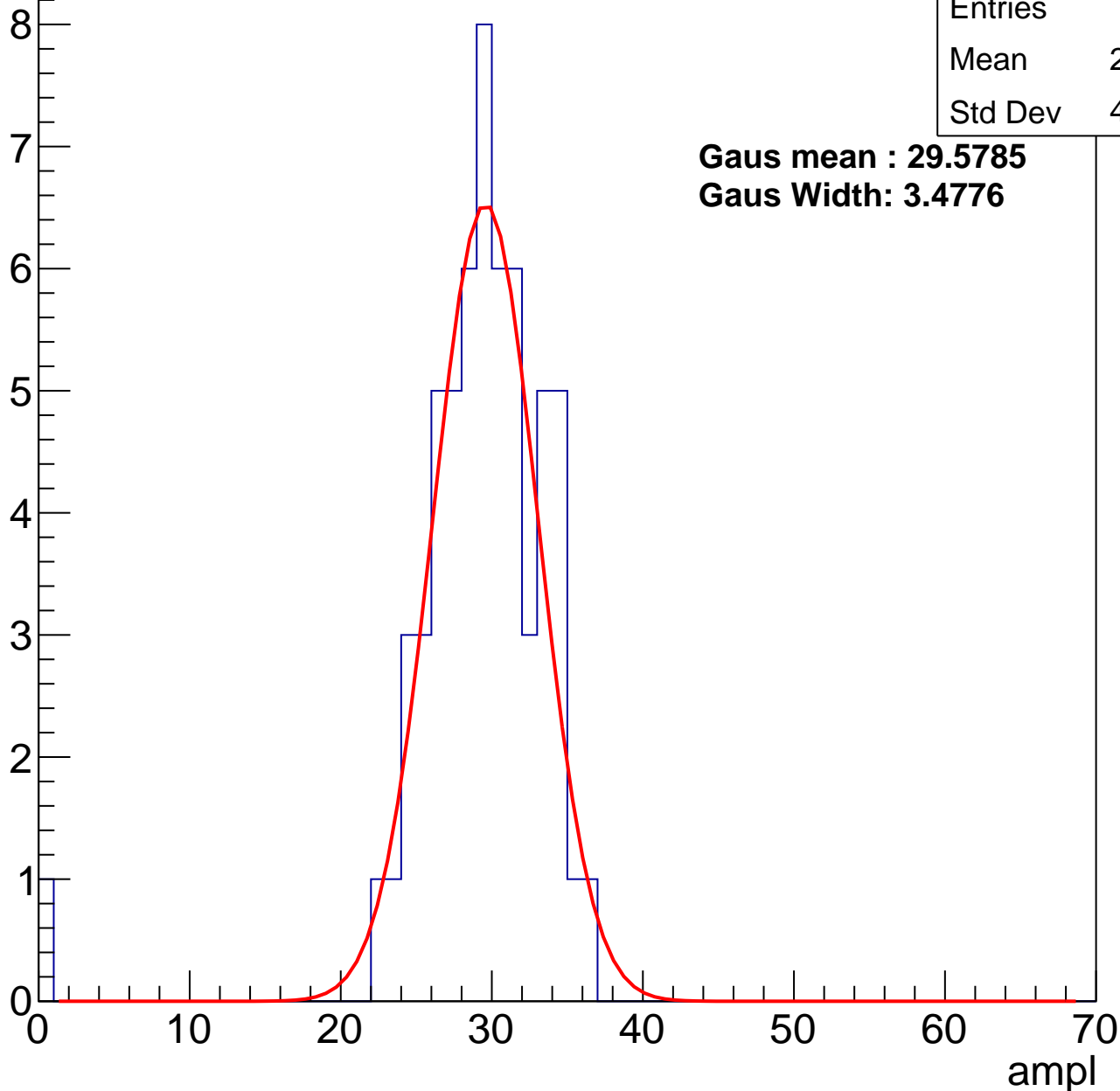
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	60
Mean	28.75
Std Dev	4.938

**Gaus mean : 29.5785**

**Gaus Width: 3.4776**



# B1L003S, U18-ch81, adc1

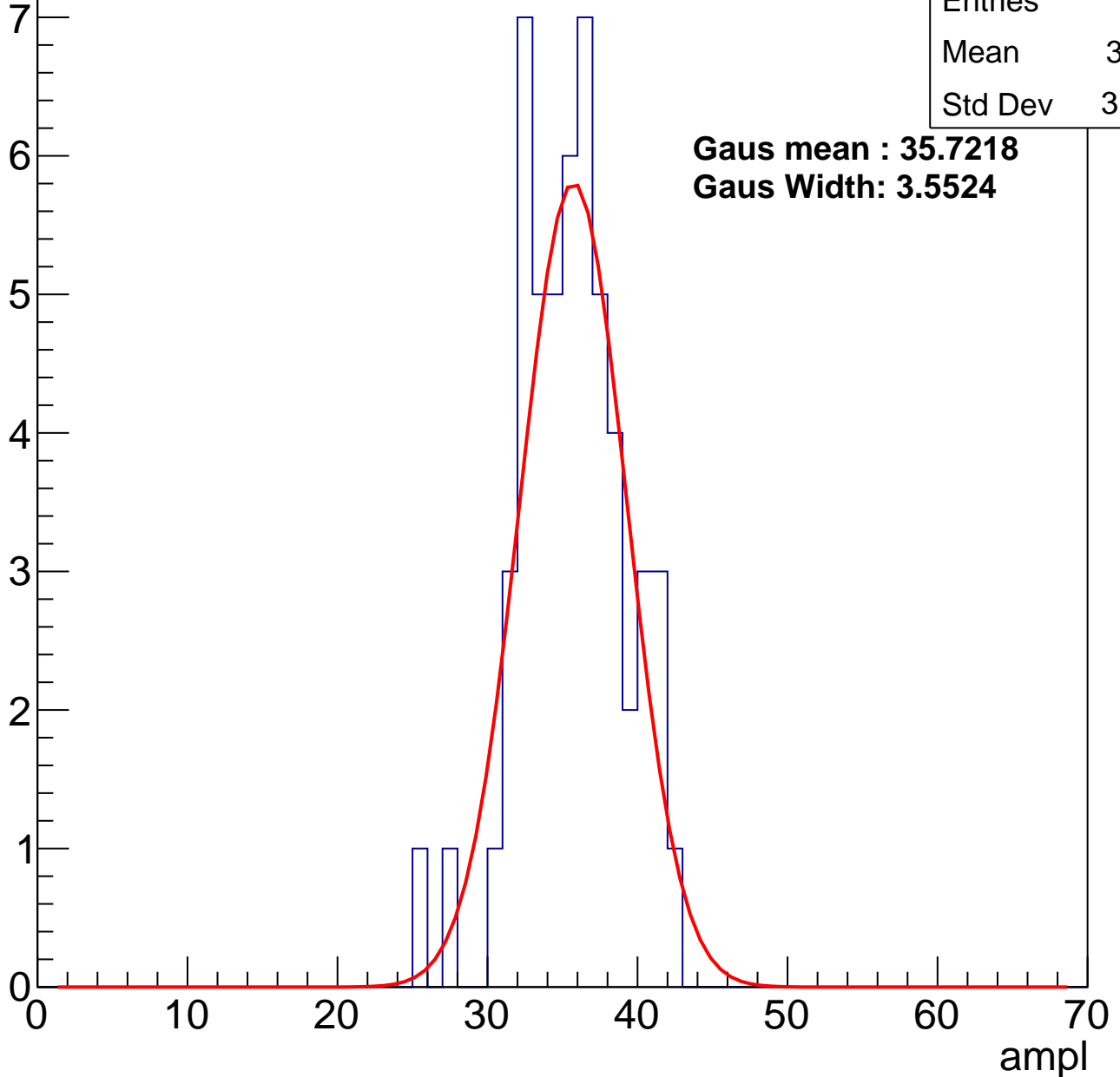
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	54
Mean	35.11
Std Dev	3.473

**Gaus mean : 35.7218**

**Gaus Width: 3.5524**



# B1L003S, U18-ch81, adc2

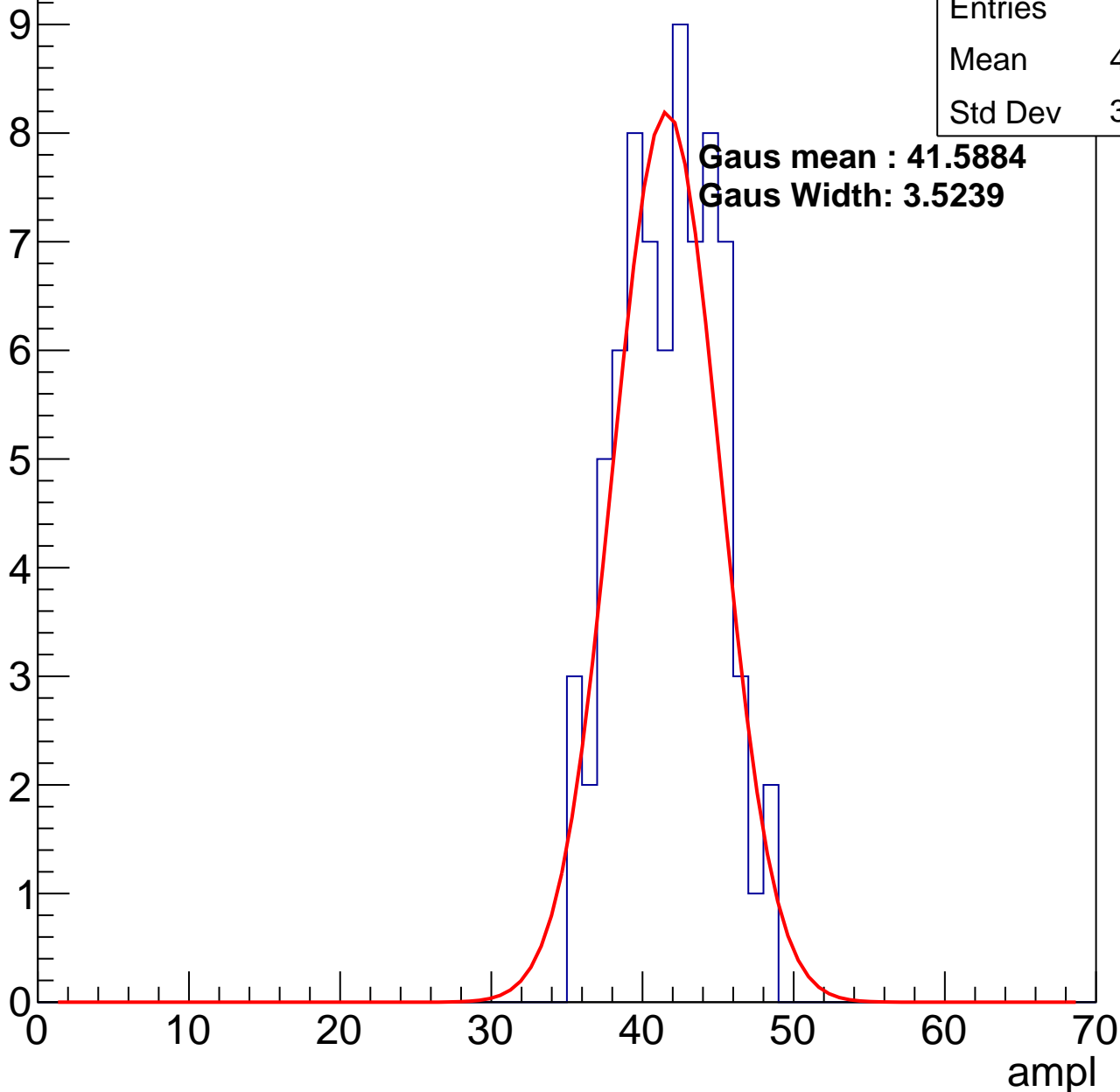
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	74
Mean	41.28
Std Dev	3.194

**Gaus mean : 41.5884**

**Gaus Width: 3.5239**

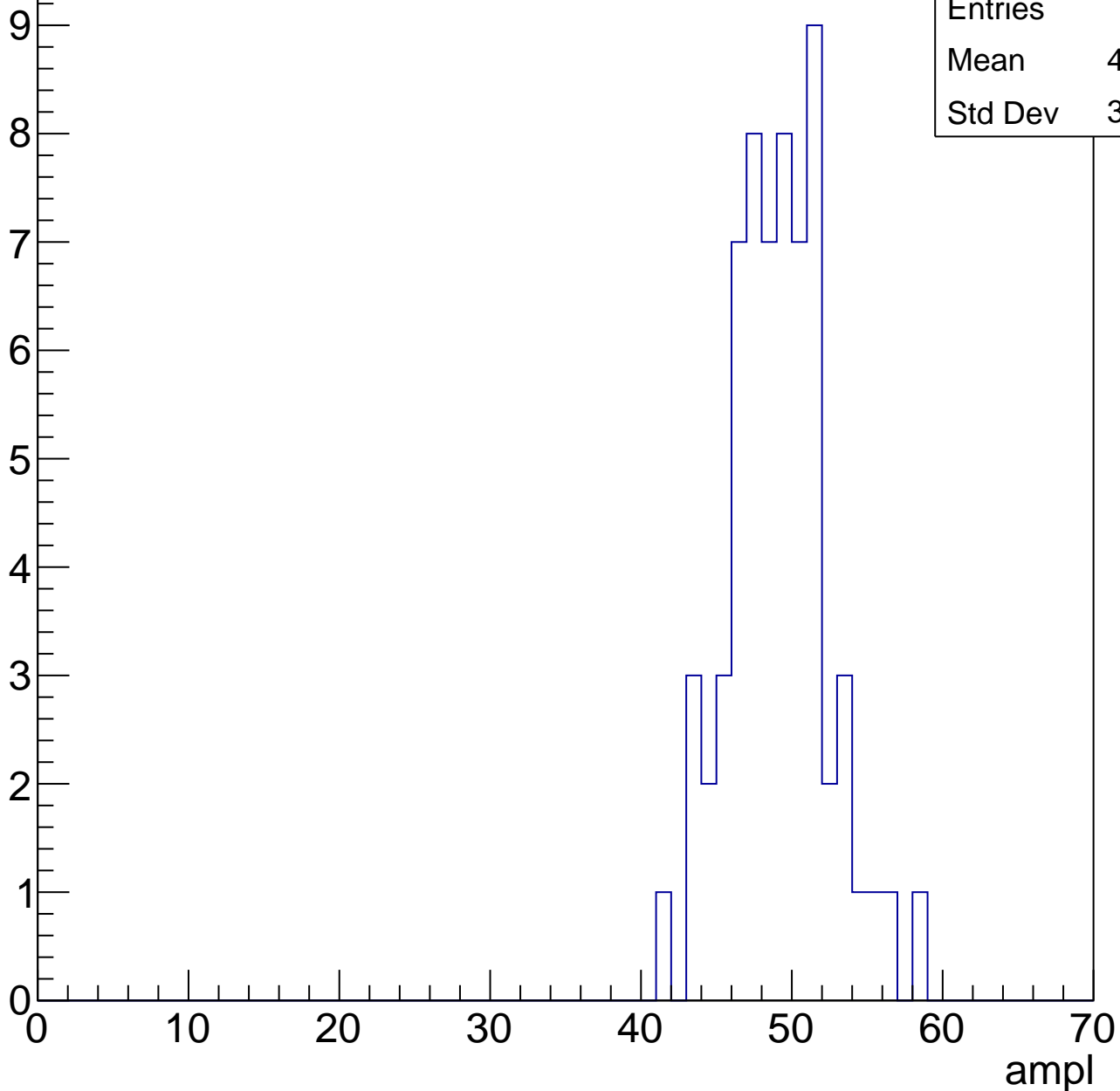


# B1L003S, U18-ch81, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	64
Mean	48.66
Std Dev	3.222

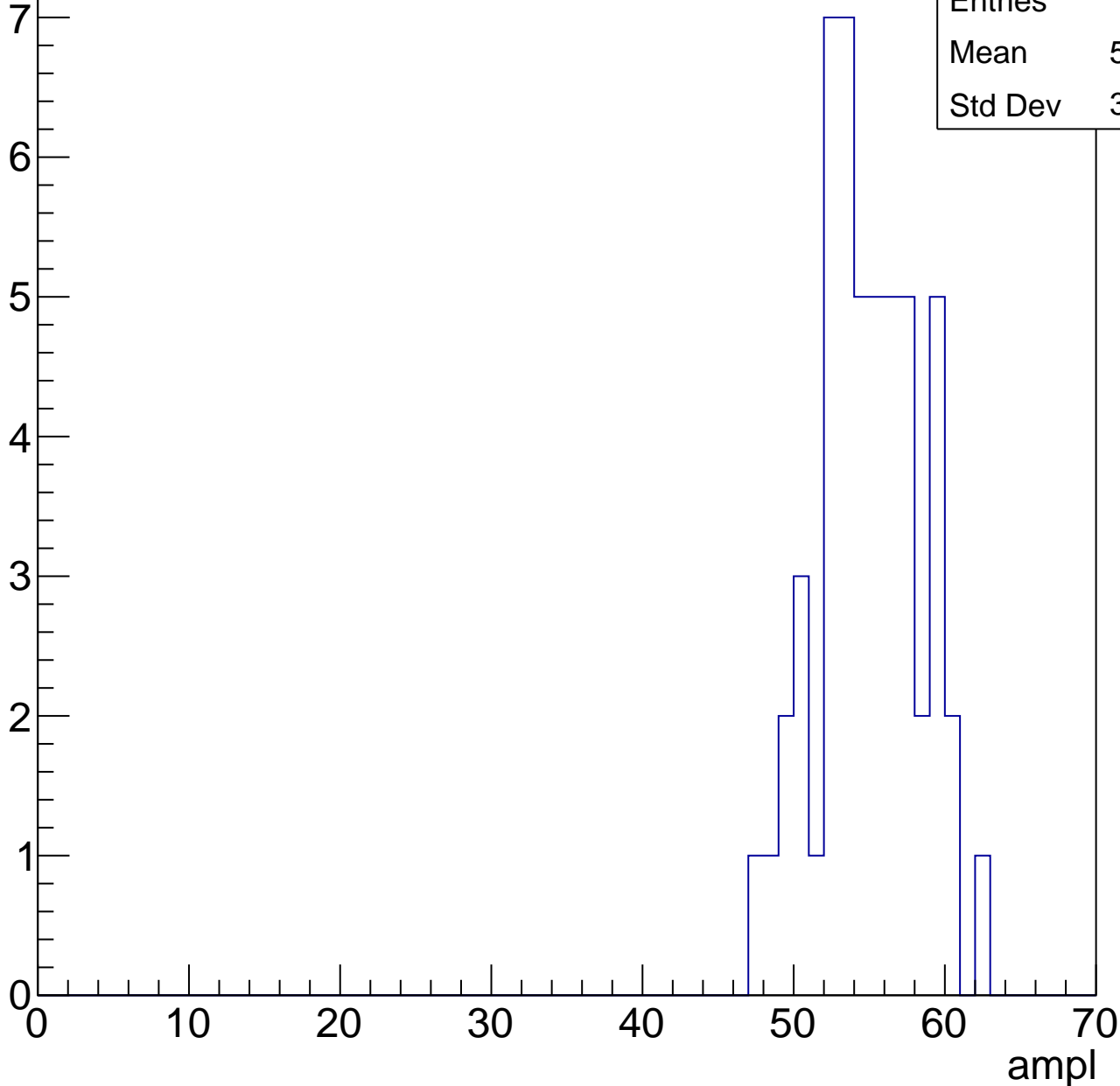


# B1L003S, U18-ch81, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	52
Mean	54.46
Std Dev	3.337

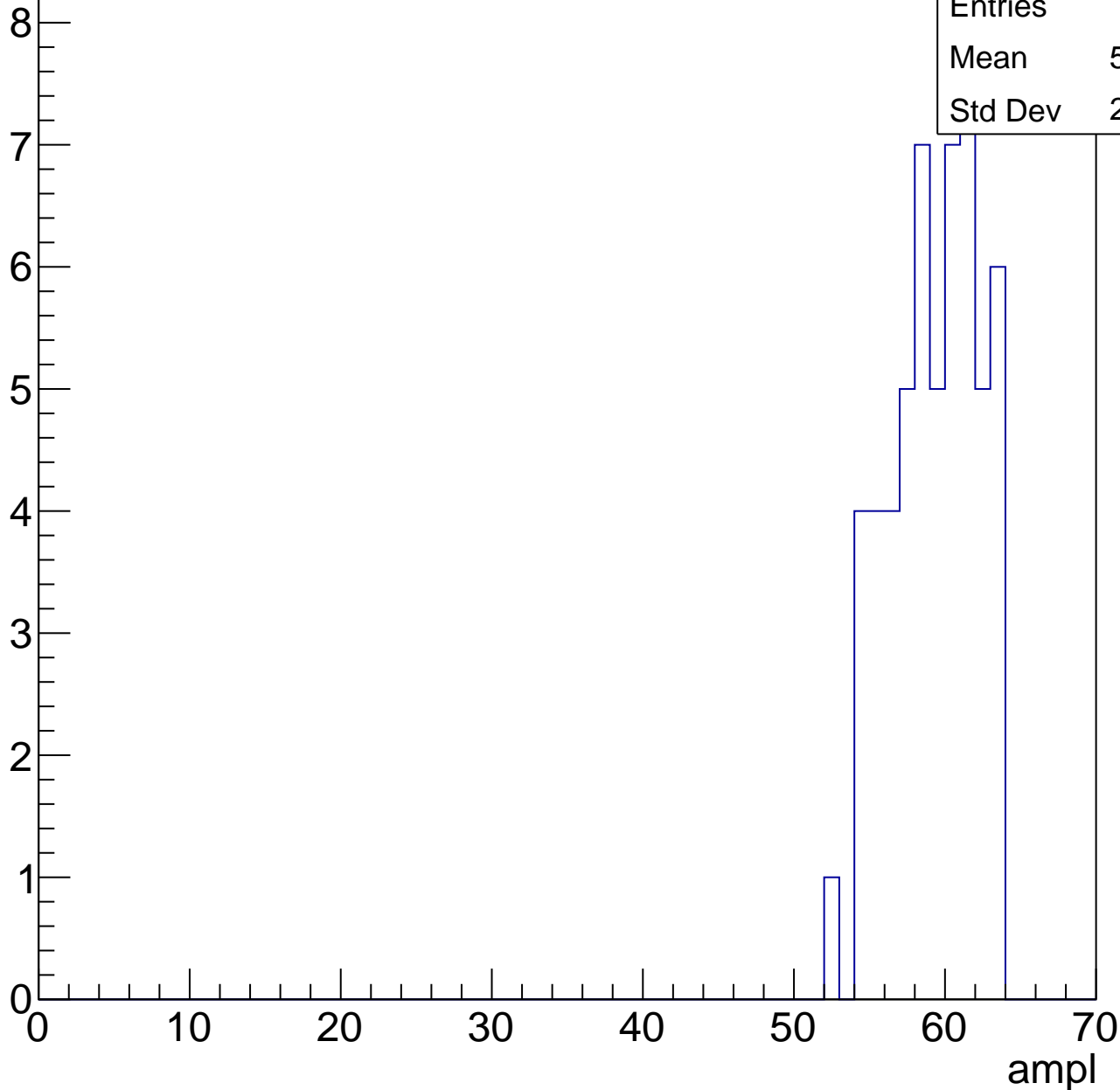


# B1L003S, U18-ch81, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

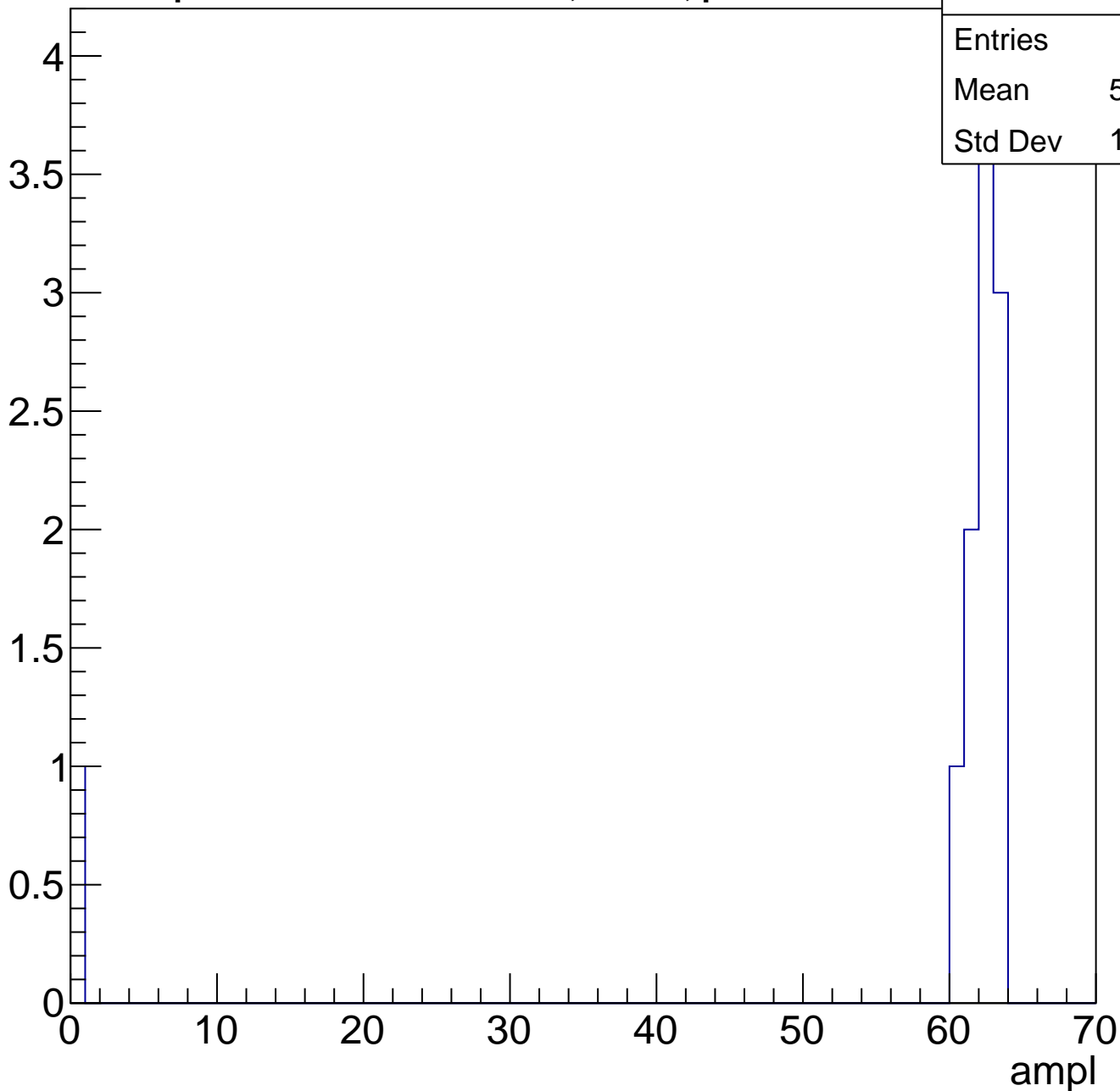
Entries	56
Mean	58.82
Std Dev	2.848



# B1L003S, U18-ch81, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

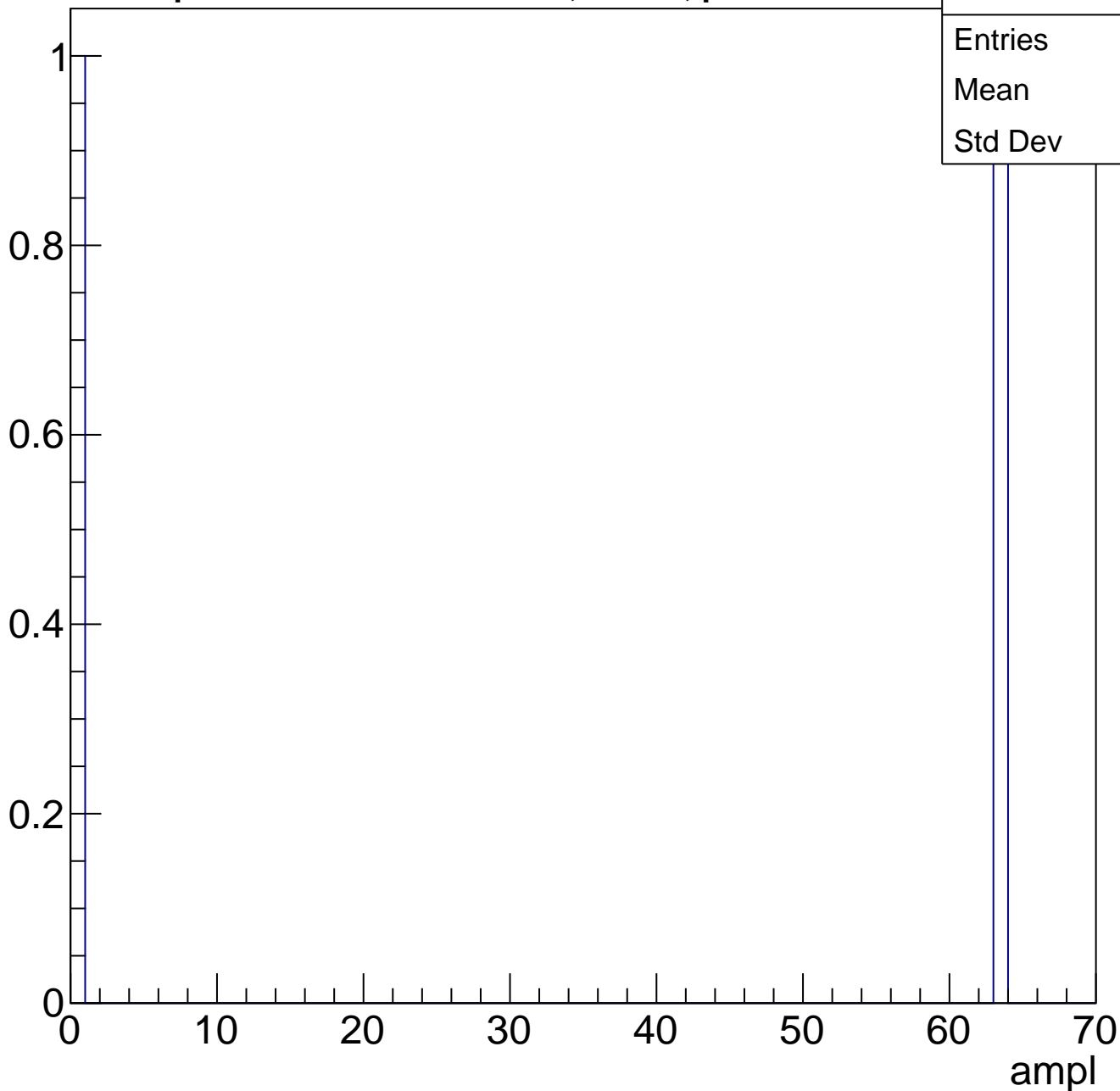




# B1L003S, U18-ch81, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U18-ch82, adc0

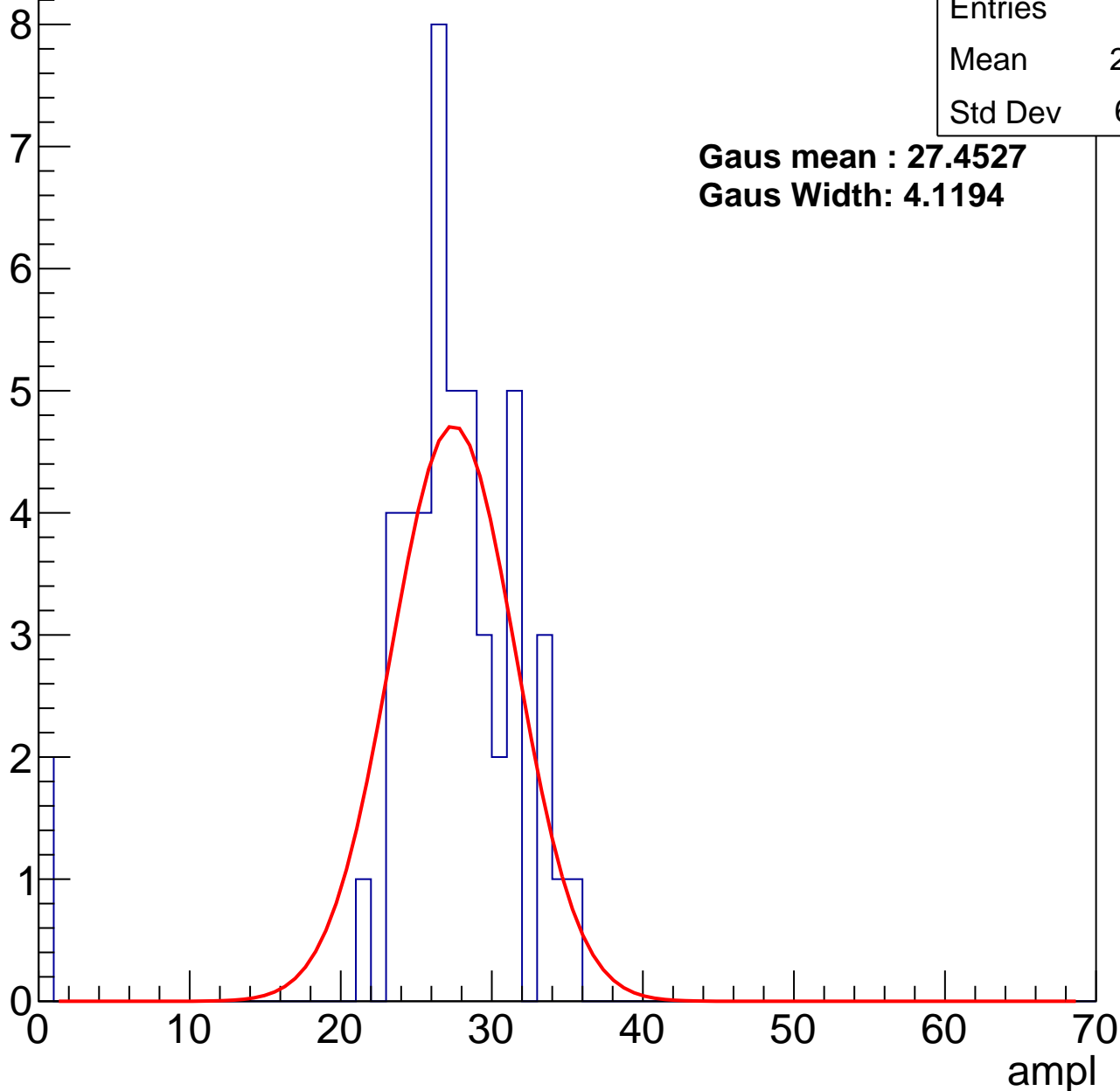
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	48
Mean	26.29
Std Dev	6.341

**Gaus mean : 27.4527**

**Gaus Width: 4.1194**



# B1L003S, U18-ch82, adc1

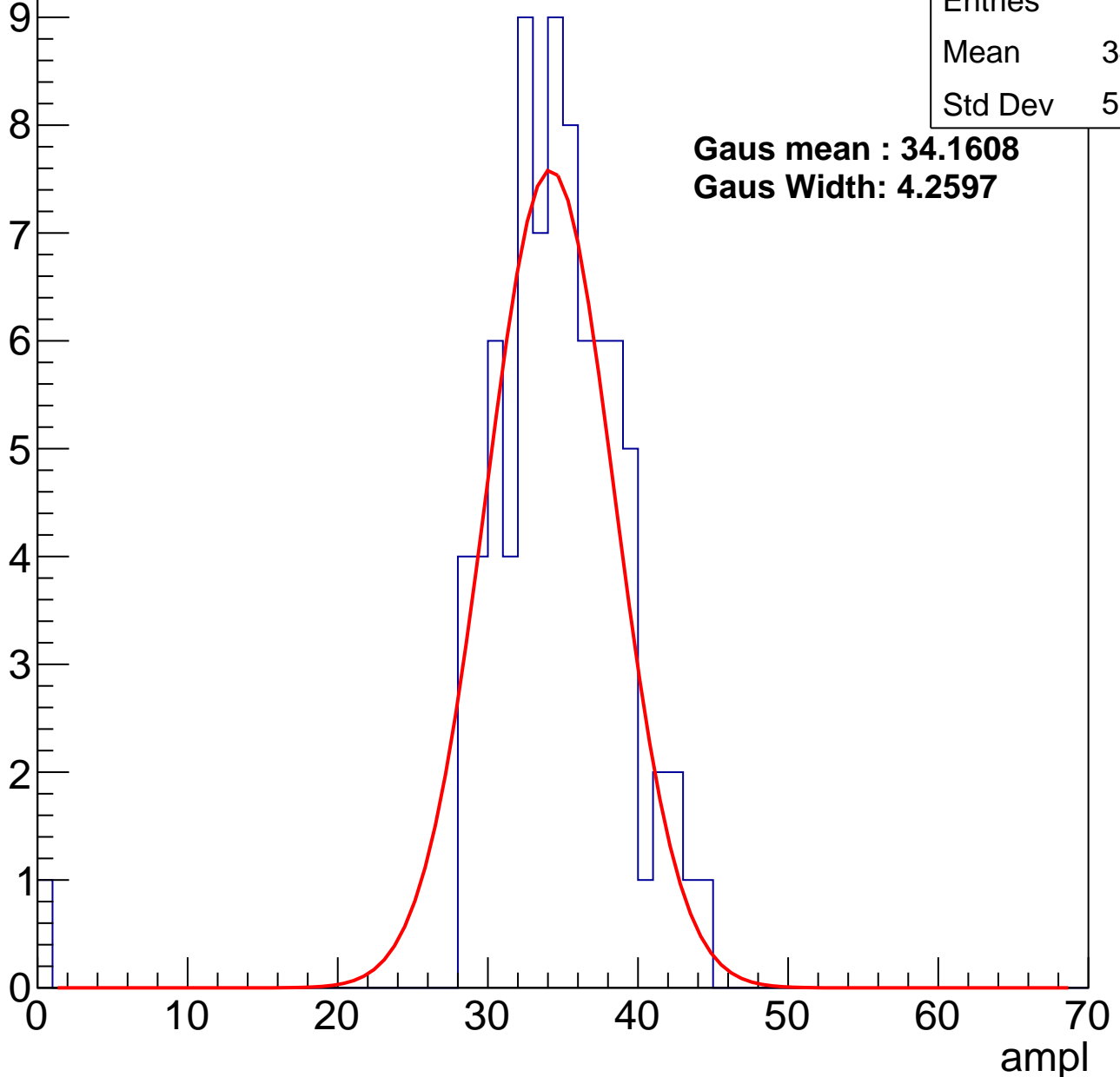
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	82
Mean	34.04
Std Dev	5.325

**Gaus mean : 34.1608**

**Gaus Width: 4.2597**



# B1L003S, U18-ch82, adc2

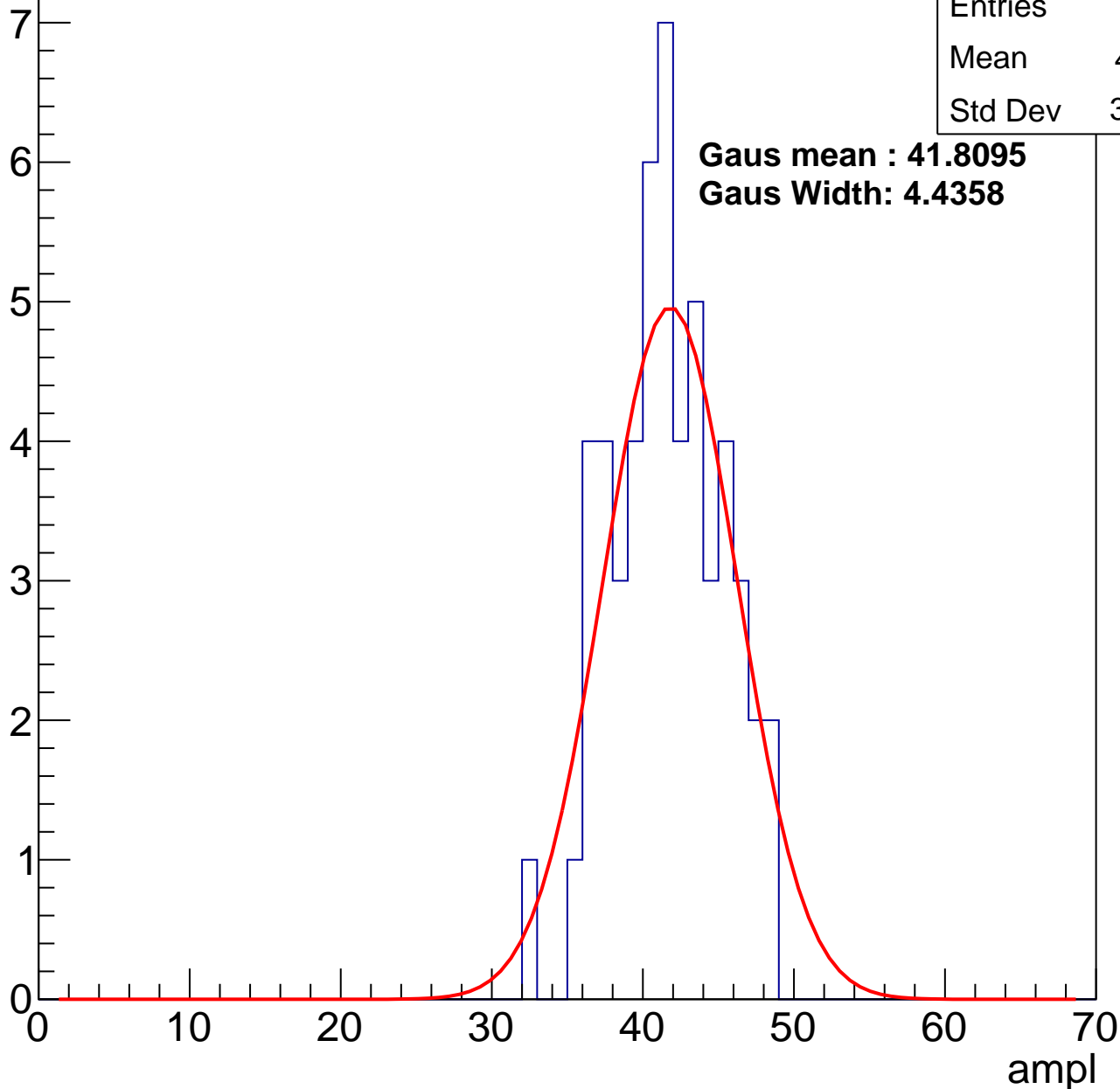
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	53
Mean	41.11
Std Dev	3.606

**Gaus mean : 41.8095**

**Gaus Width: 4.4358**

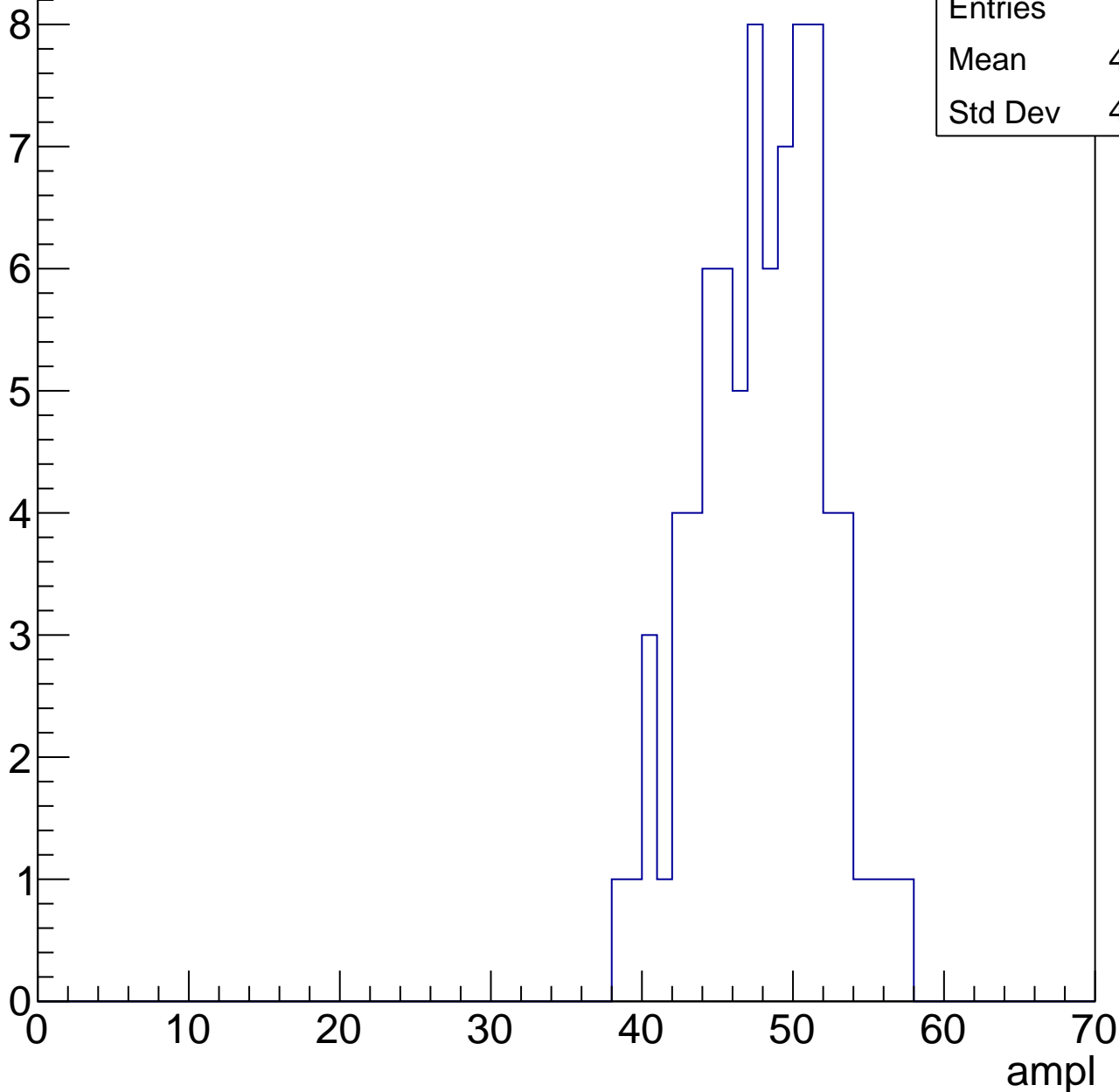


# B1L003S, U18-ch82, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	80
Mean	47.49
Std Dev	4.074

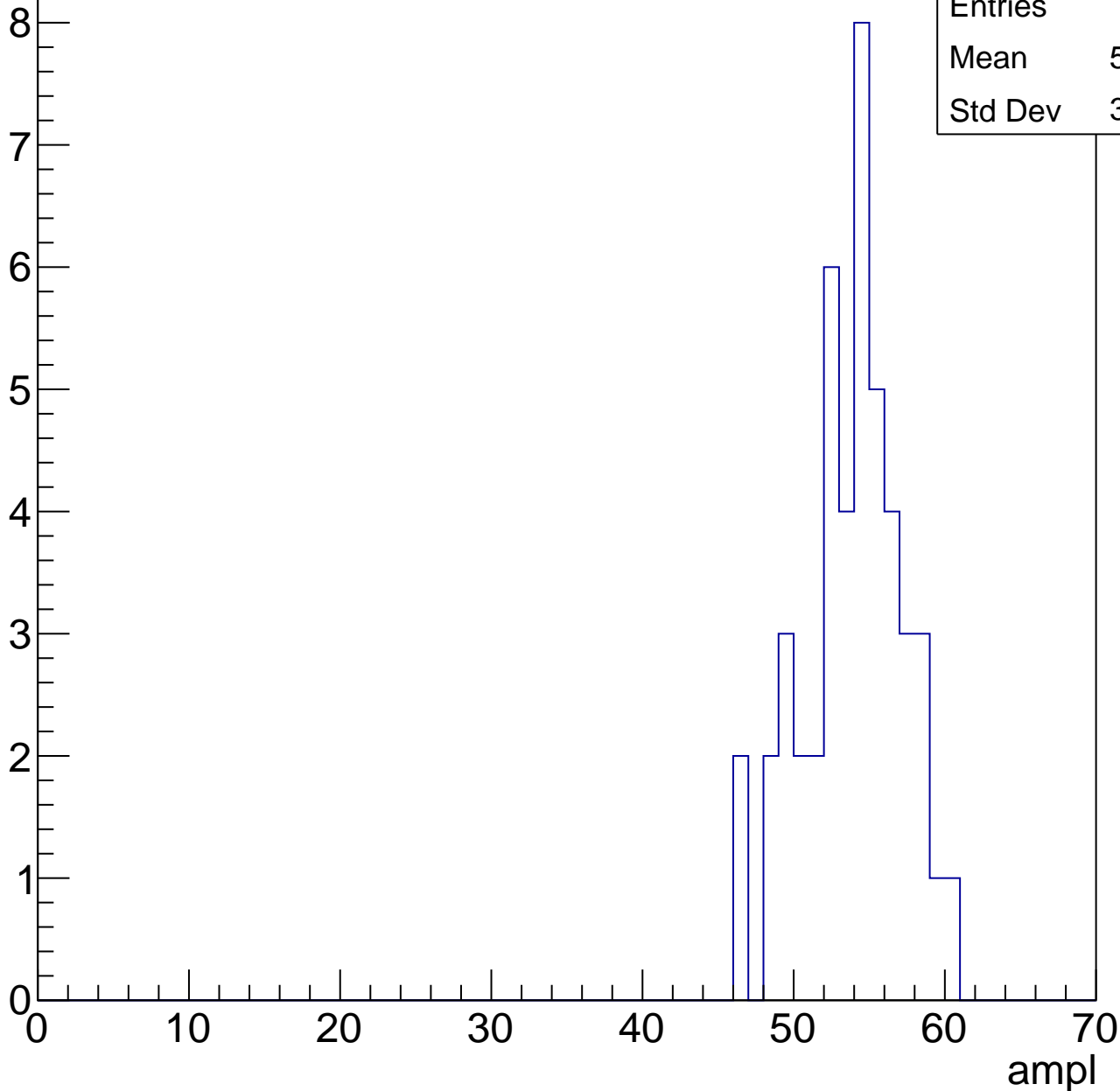


# B1L003S, U18-ch82, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

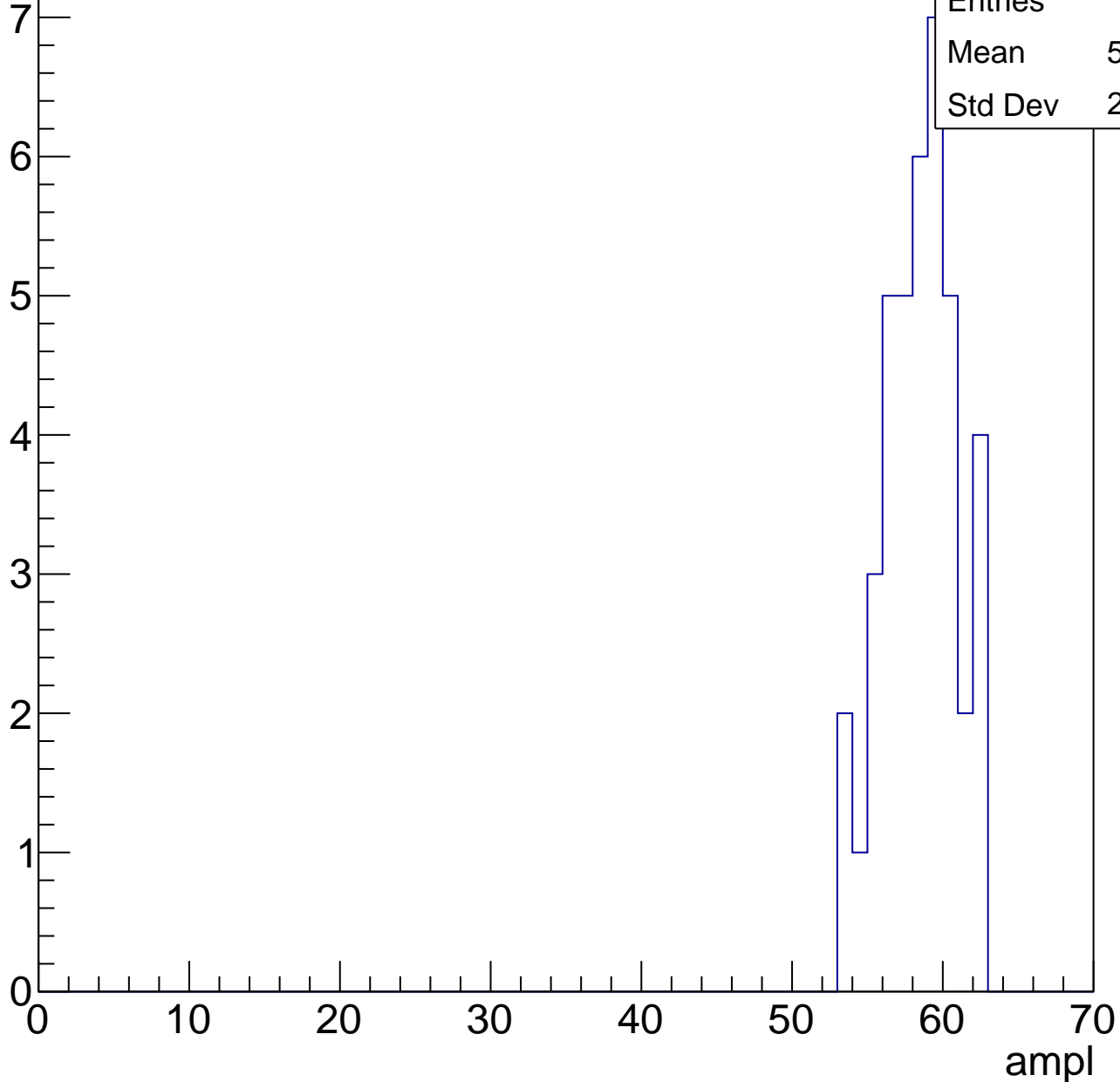
Entries	46
Mean	53.39
Std Dev	3.274



# B1L003S, U18-ch82, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

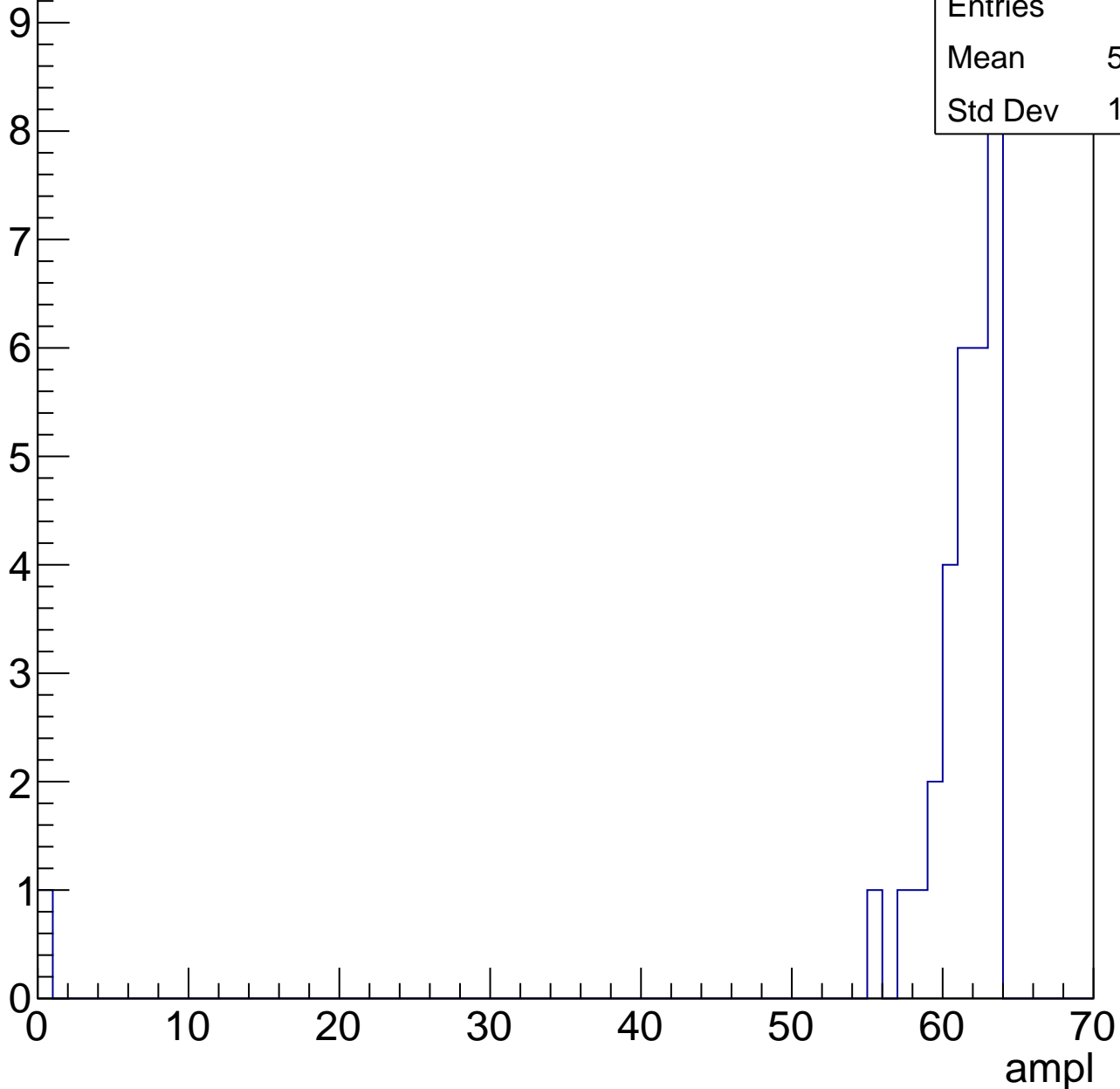


# B1L003S, U18-ch82, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	31
Mean	59.13
Std Dev	10.97

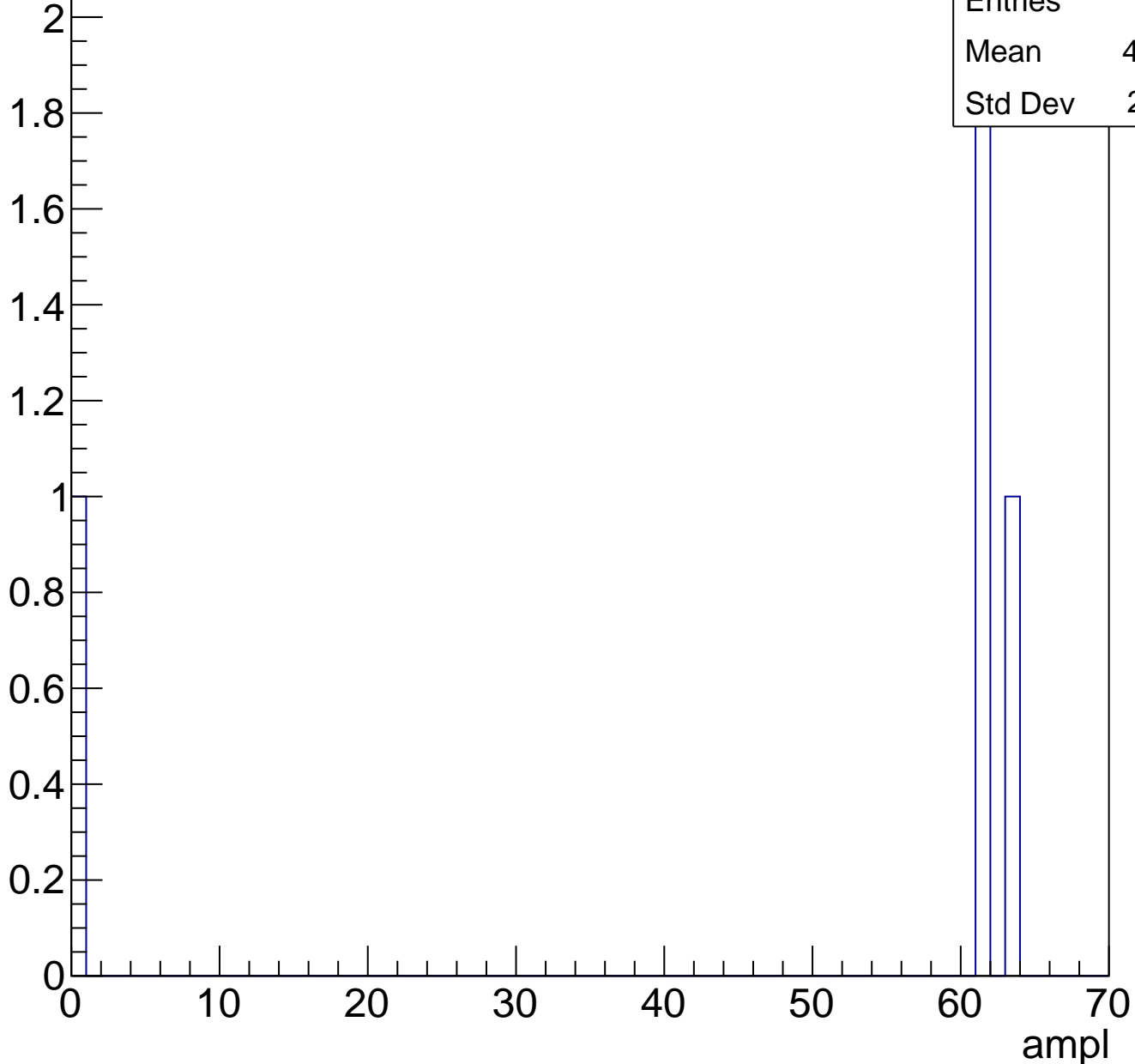




# B1L003S, U18-ch82, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	4
Mean	46.25
Std Dev	26.71

# B1L003S, U18-ch83, adc0

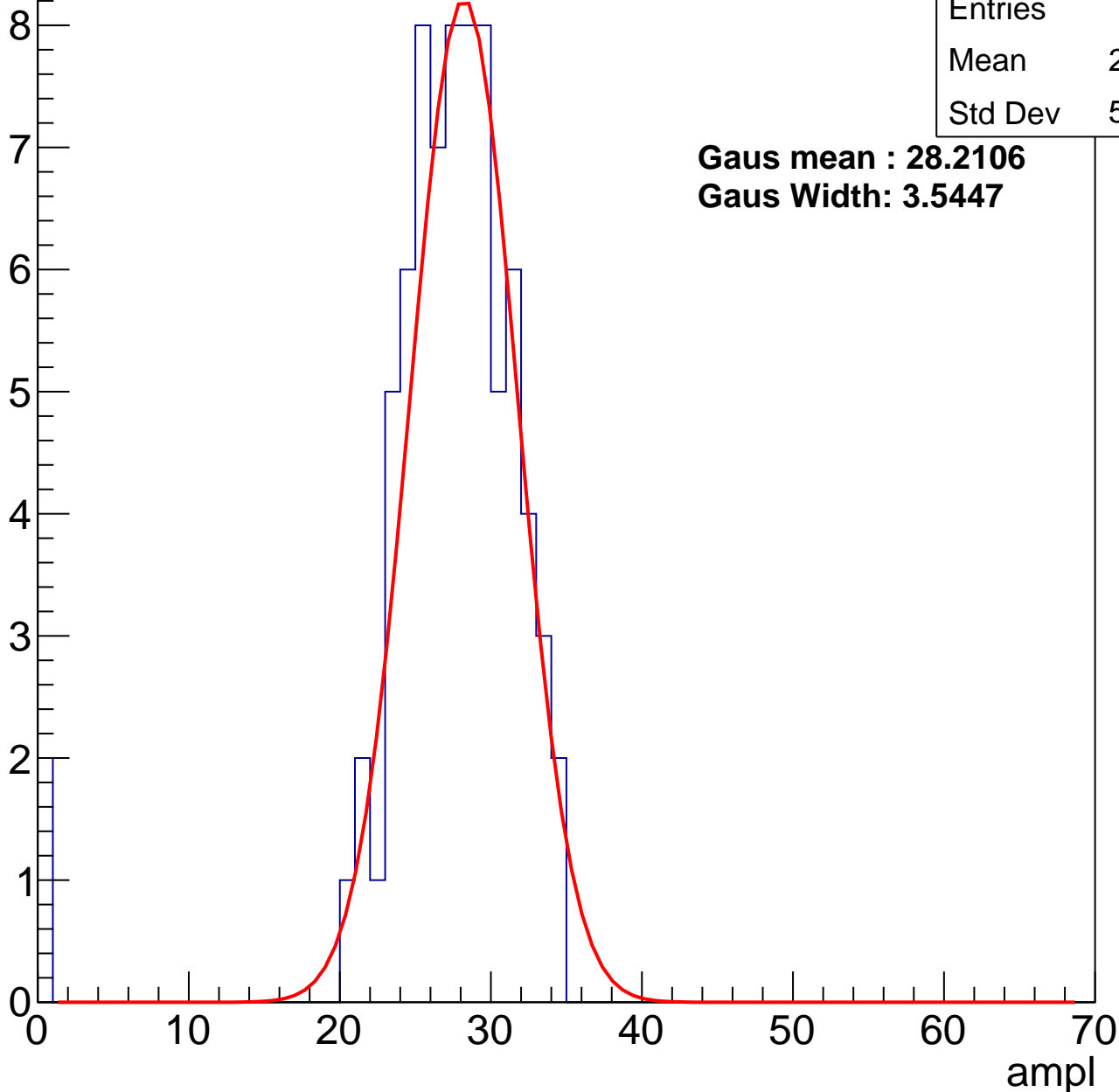
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	76
Mean	26.68
Std Dev	5.449

**Gaus mean : 28.2106**

**Gaus Width: 3.5447**



# B1L003S, U18-ch83, adc1

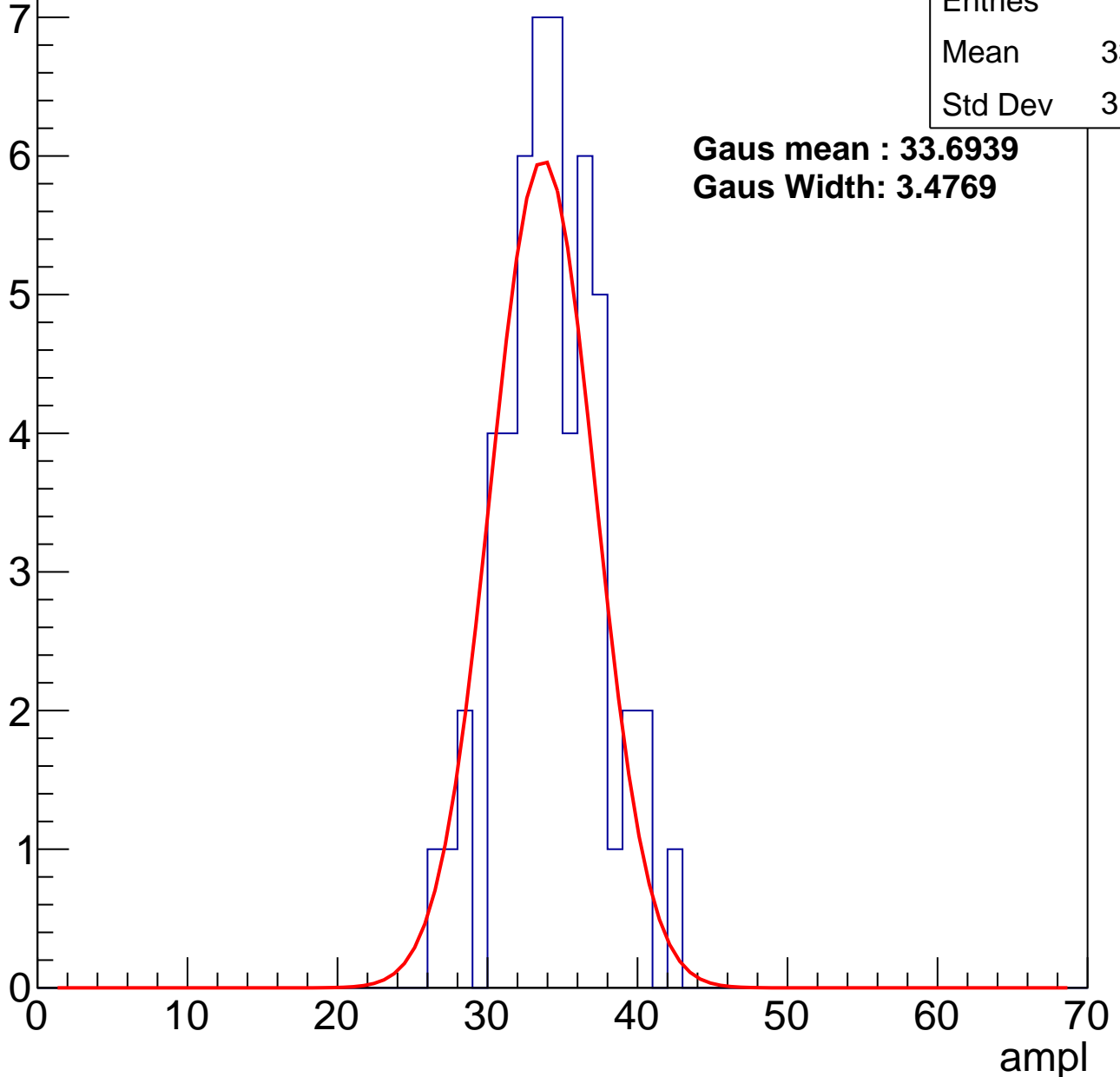
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	53
Mean	33.83
Std Dev	3.335

**Gaus mean : 33.6939**

**Gaus Width: 3.4769**



# B1L003S, U18-ch83, adc2

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	73
Mean	40.21
Std Dev	3.412

**Gaus mean : 40.5323**

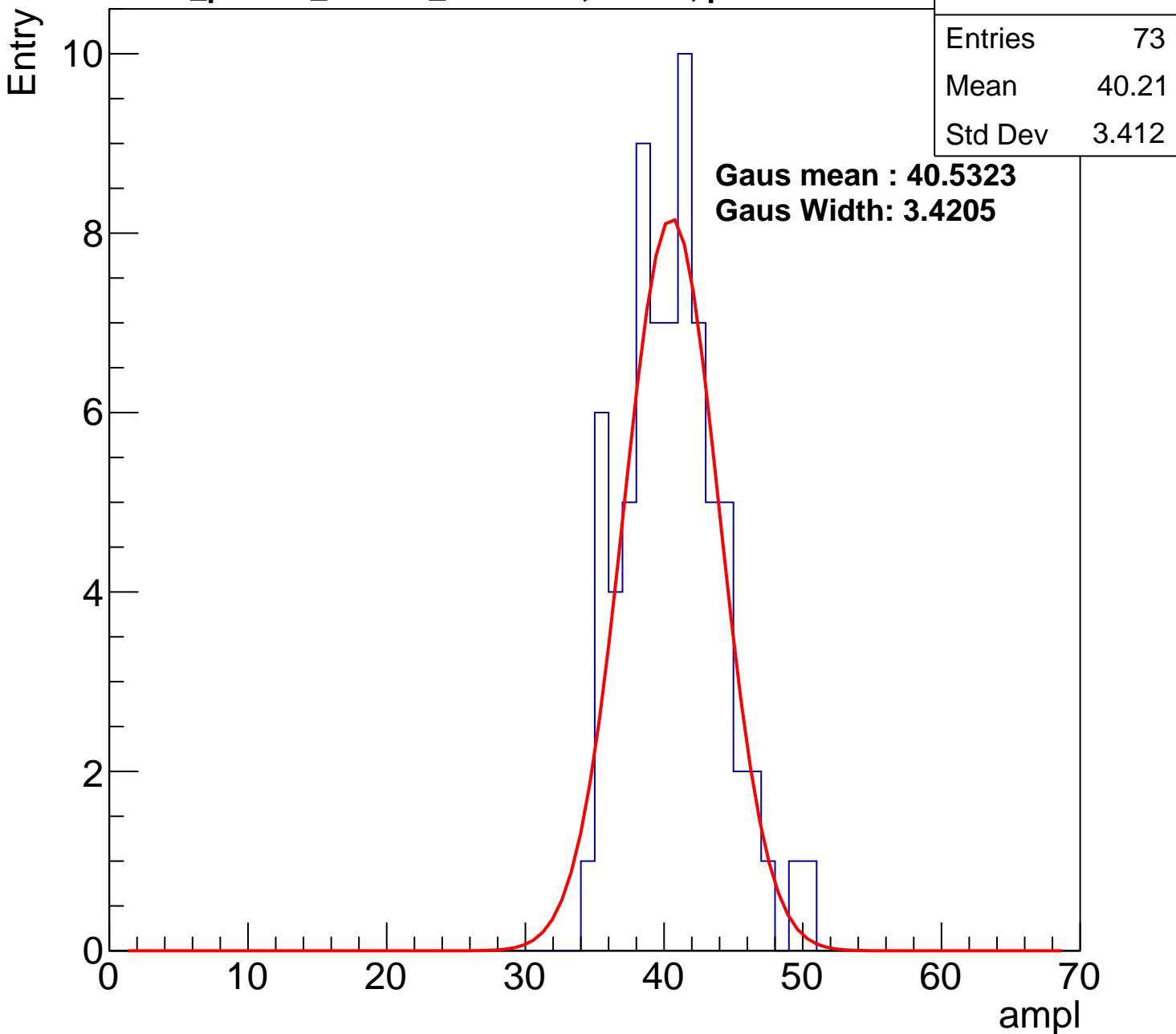
**Gaus Width: 3.4205**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

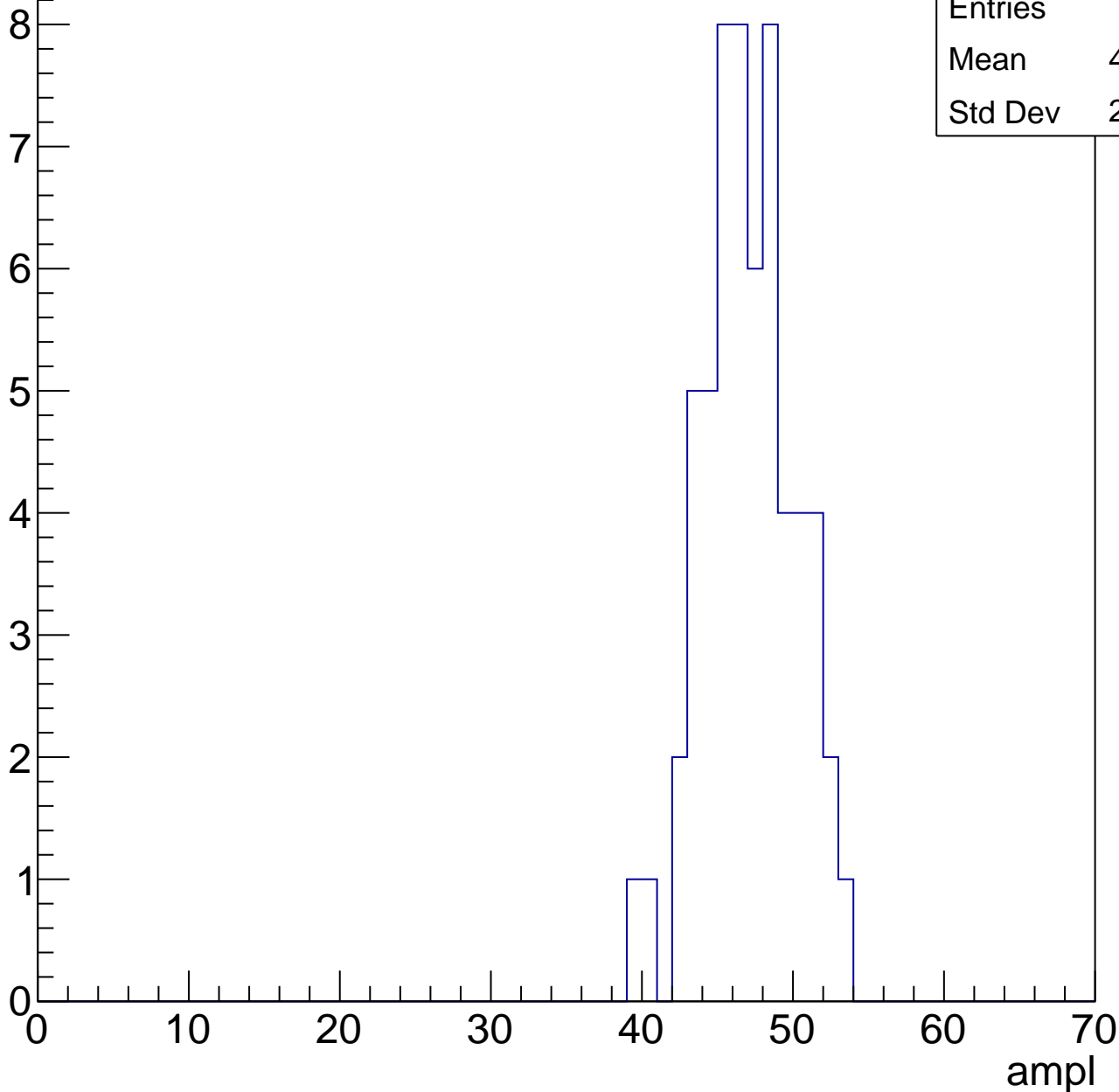


# B1L003S, U18-ch83, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	59
Mean	46.59
Std Dev	2.992

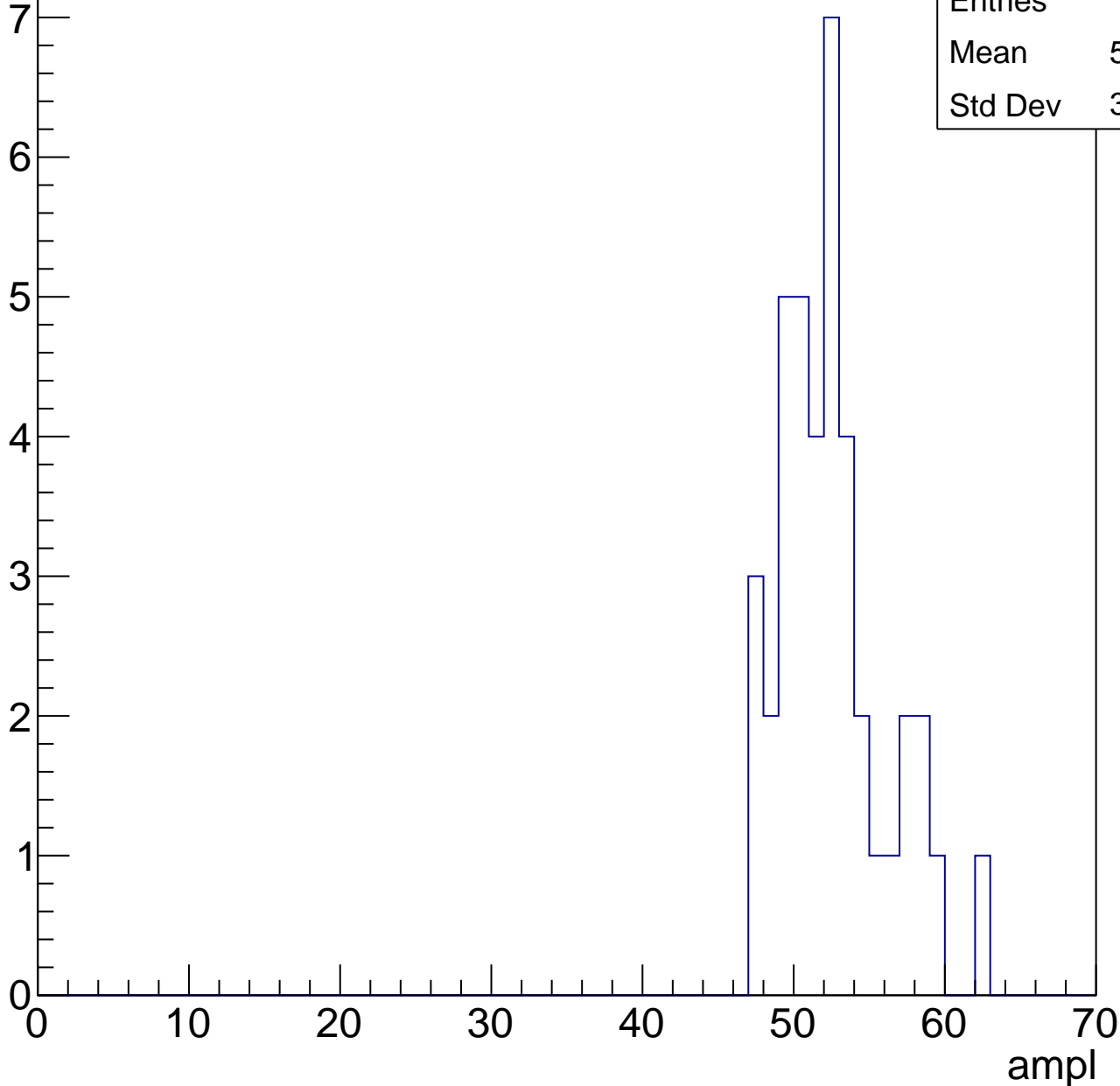


# B1L003S, U18-ch83, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

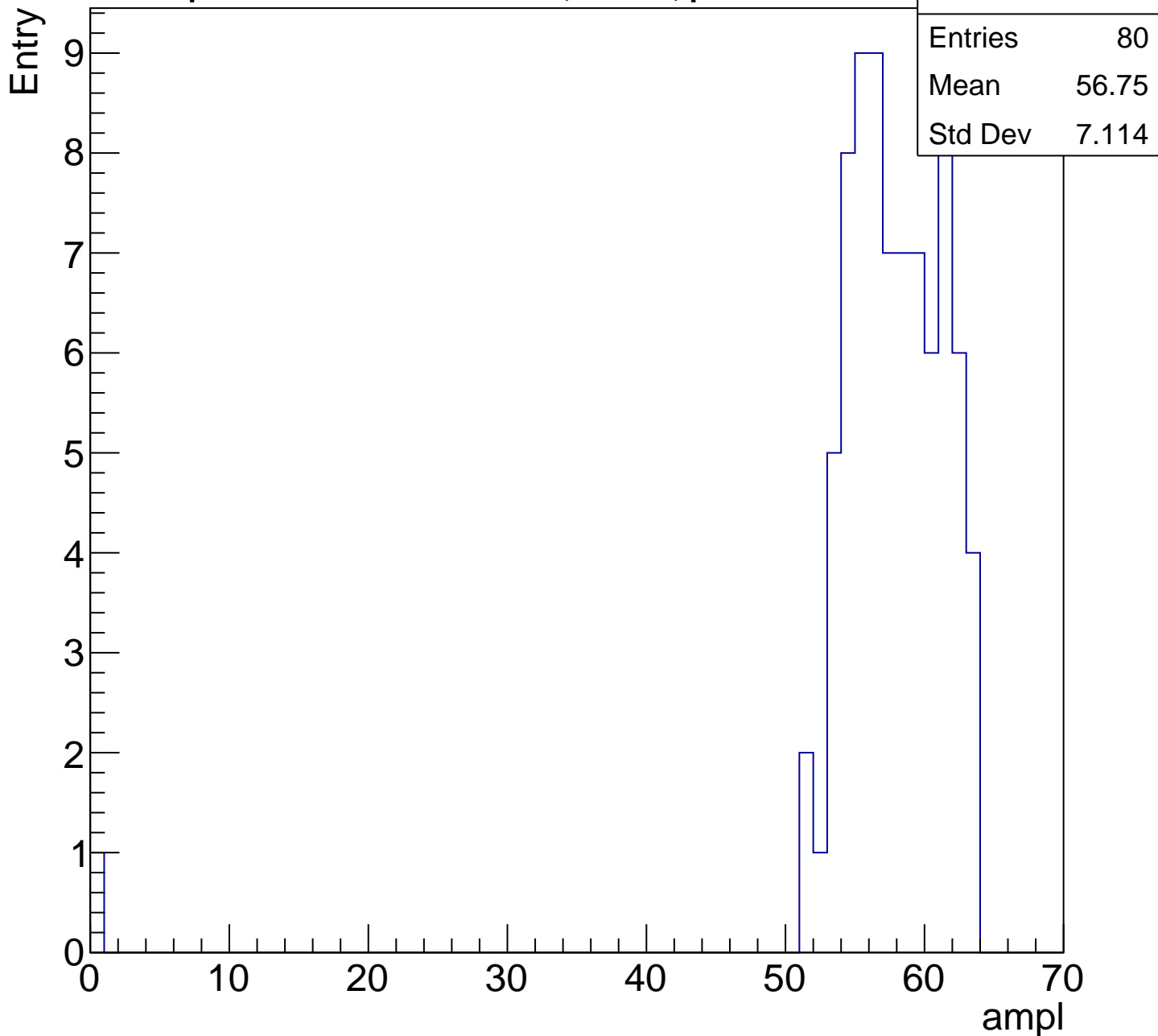
Entry

Entries	40
Mean	52.05
Std Dev	3.478



# B1L003S, U18-ch83, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

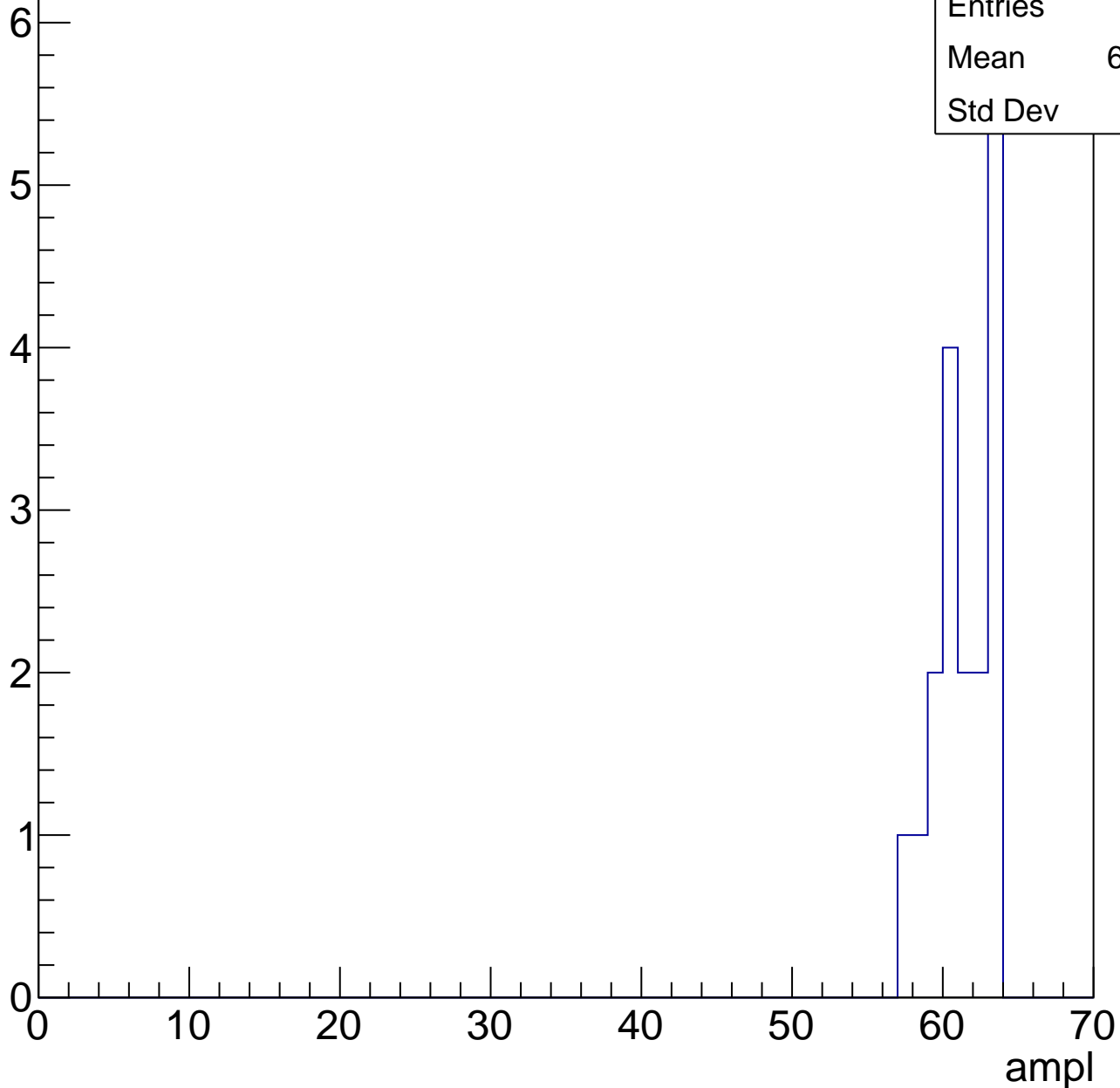


# B1L003S, U18-ch83, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	18
Mean	60.94
Std Dev	1.87

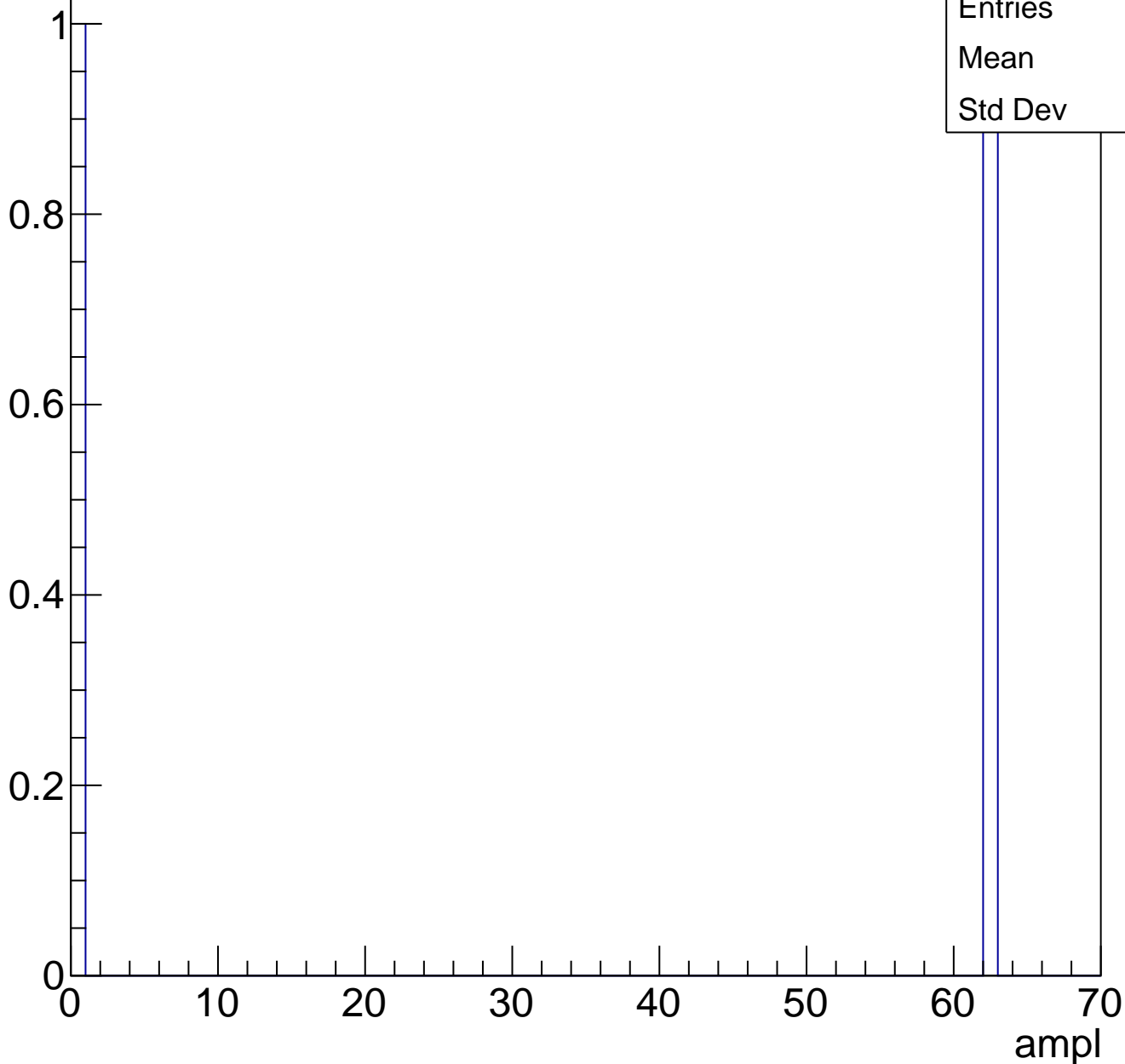




# B1L003S, U18-ch83, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U18-ch84, adc0

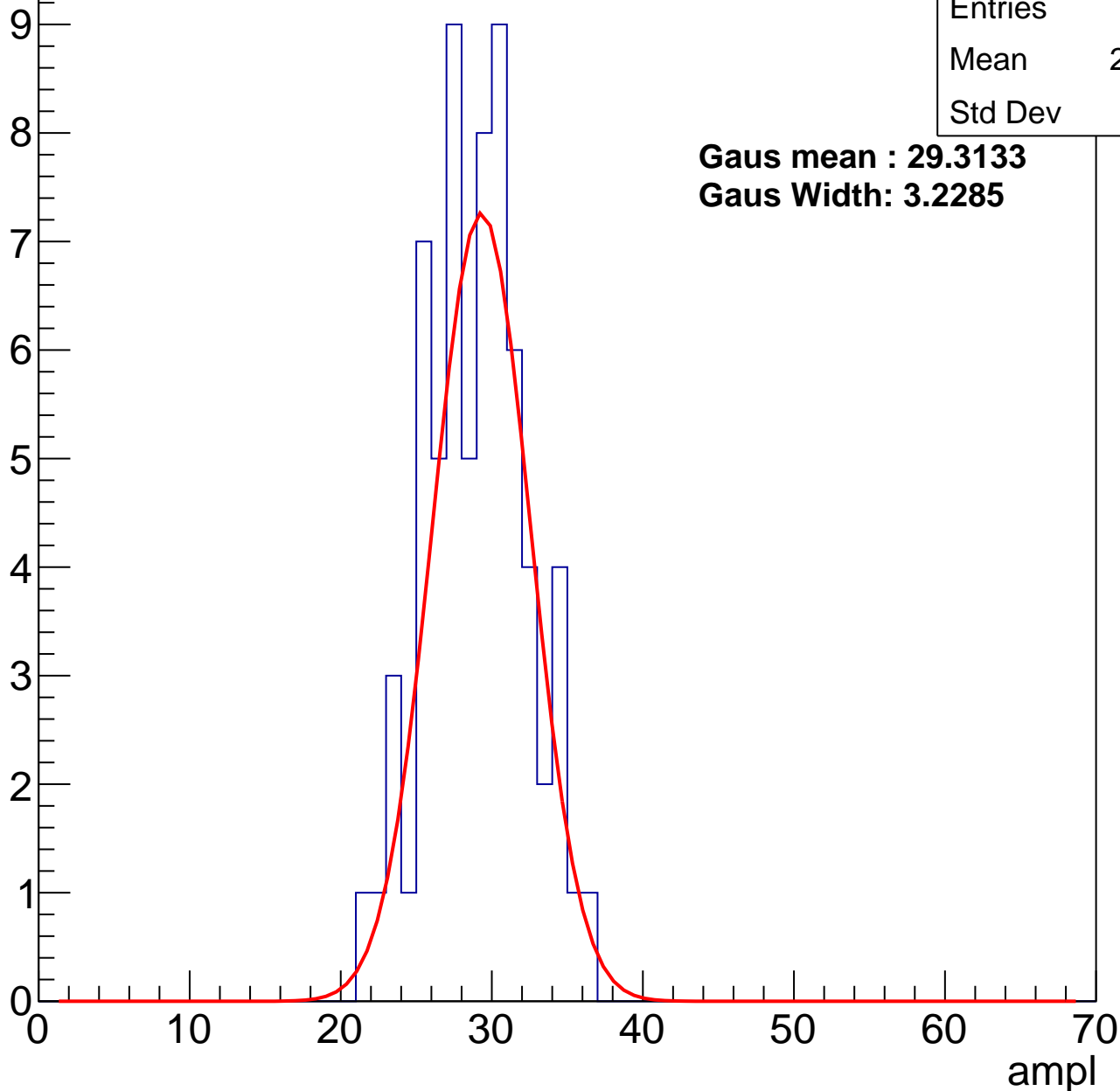
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	67
Mean	28.55
Std Dev	3.27

**Gaus mean : 29.3133**

**Gaus Width: 3.2285**



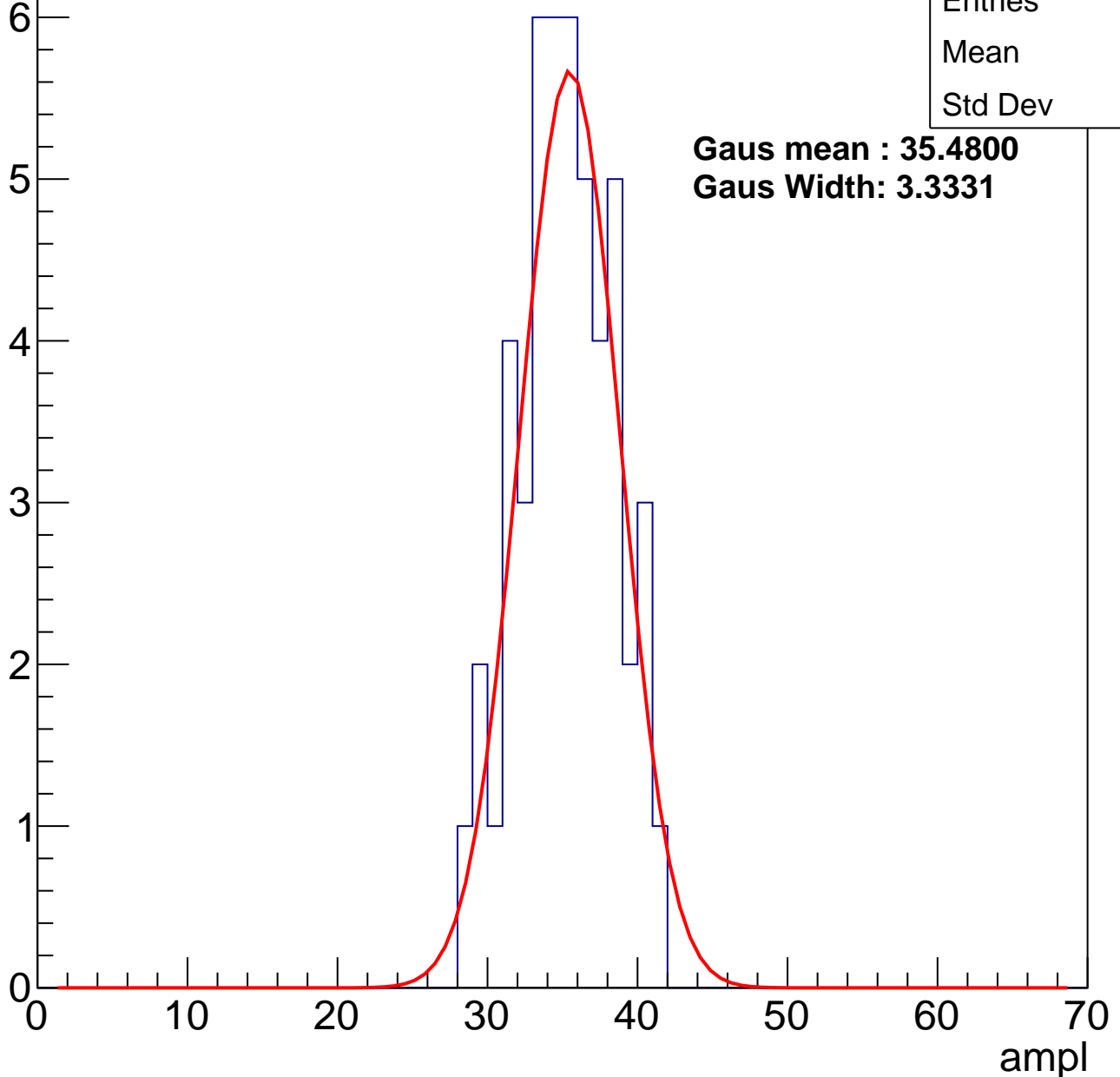
# B1L003S, U18-ch84, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	49
Mean	34.8
Std Dev	3.11

**Gaus mean : 35.4800**  
**Gaus Width: 3.3331**



# B1L003S, U18-ch84, adc2

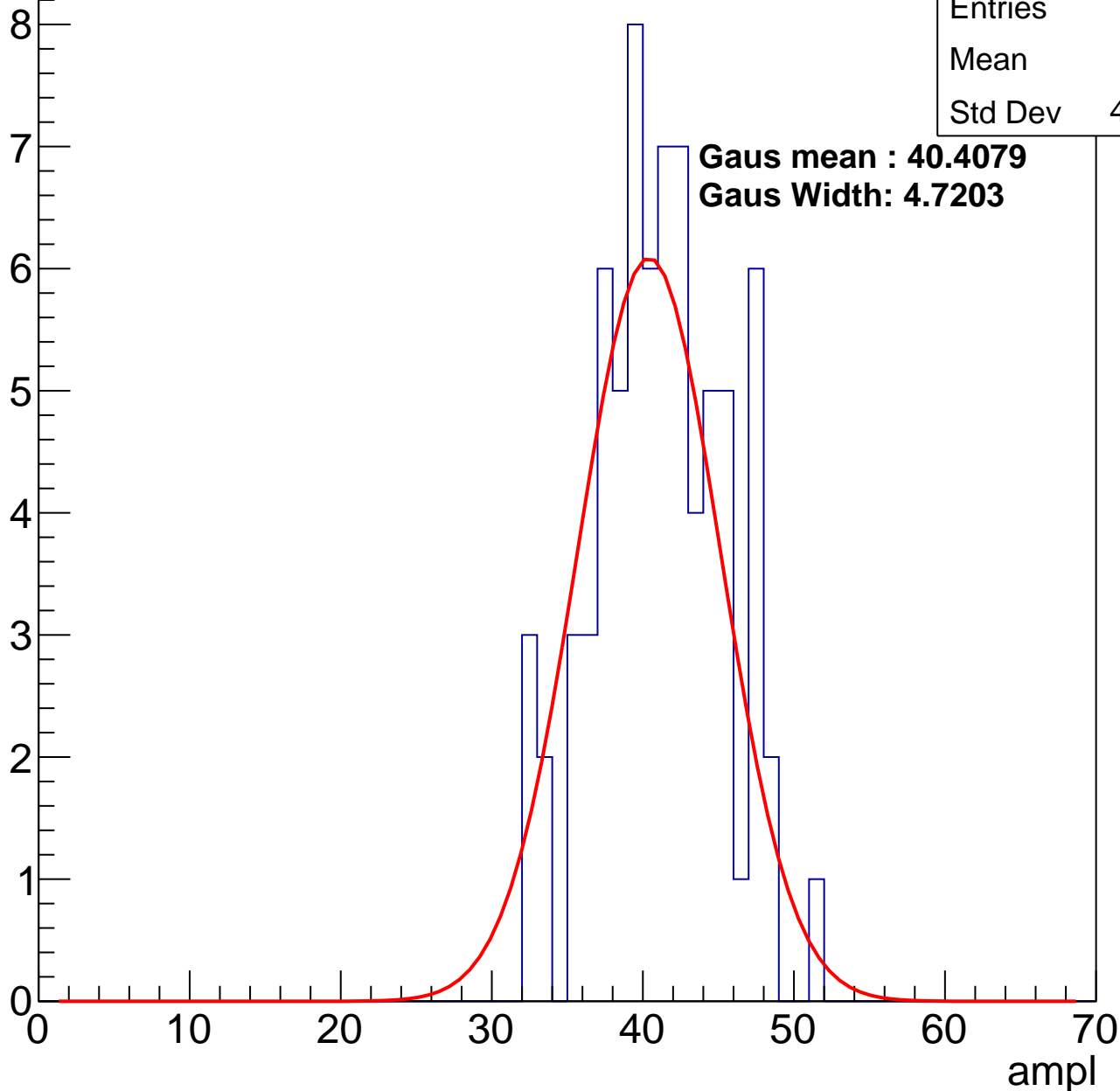
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	74
Mean	40.7
Std Dev	4.213

**Gaus mean : 40.4079**

**Gaus Width: 4.7203**

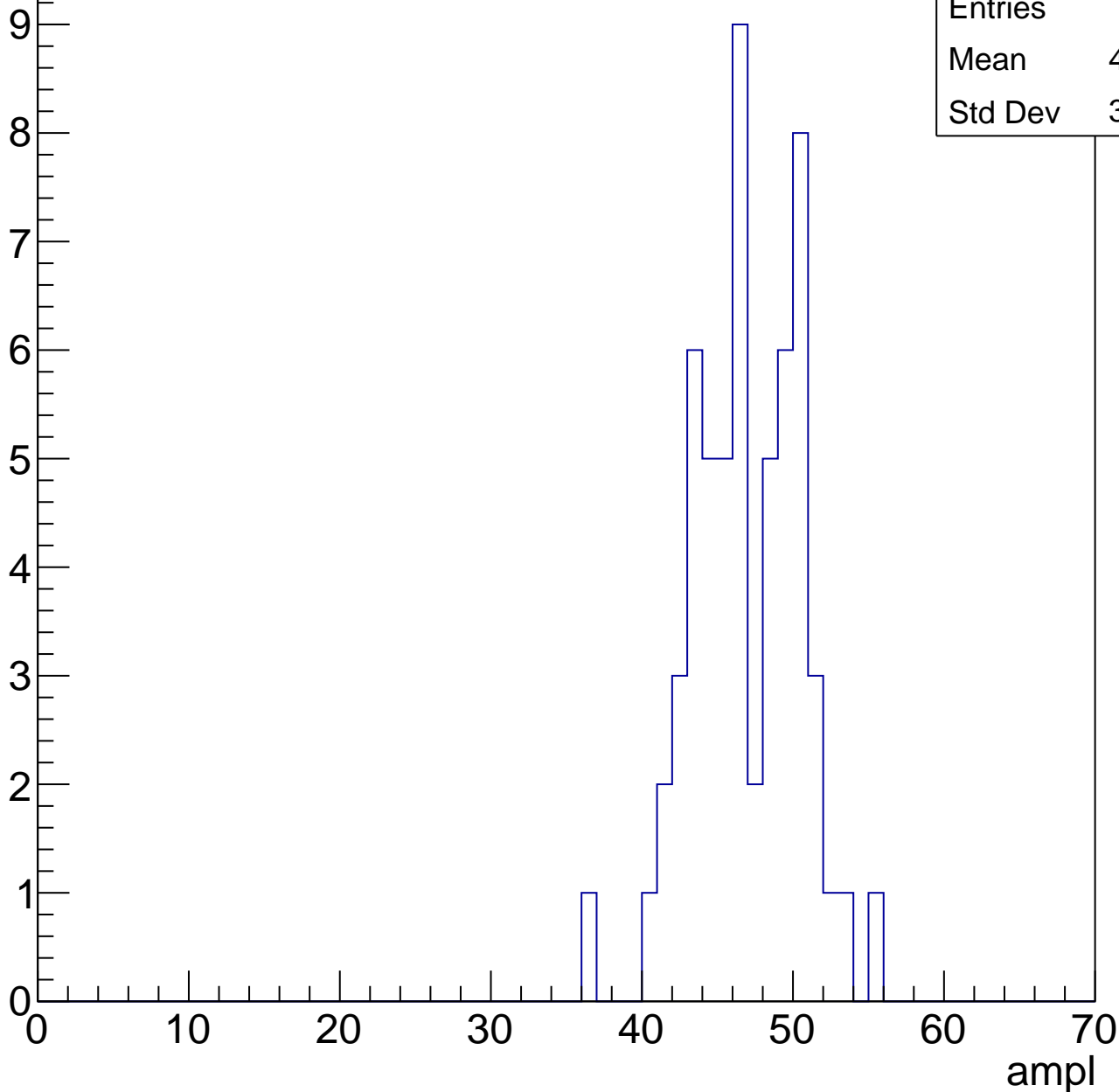


# B1L003S, U18-ch84, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	59
Mean	46.47
Std Dev	3.553

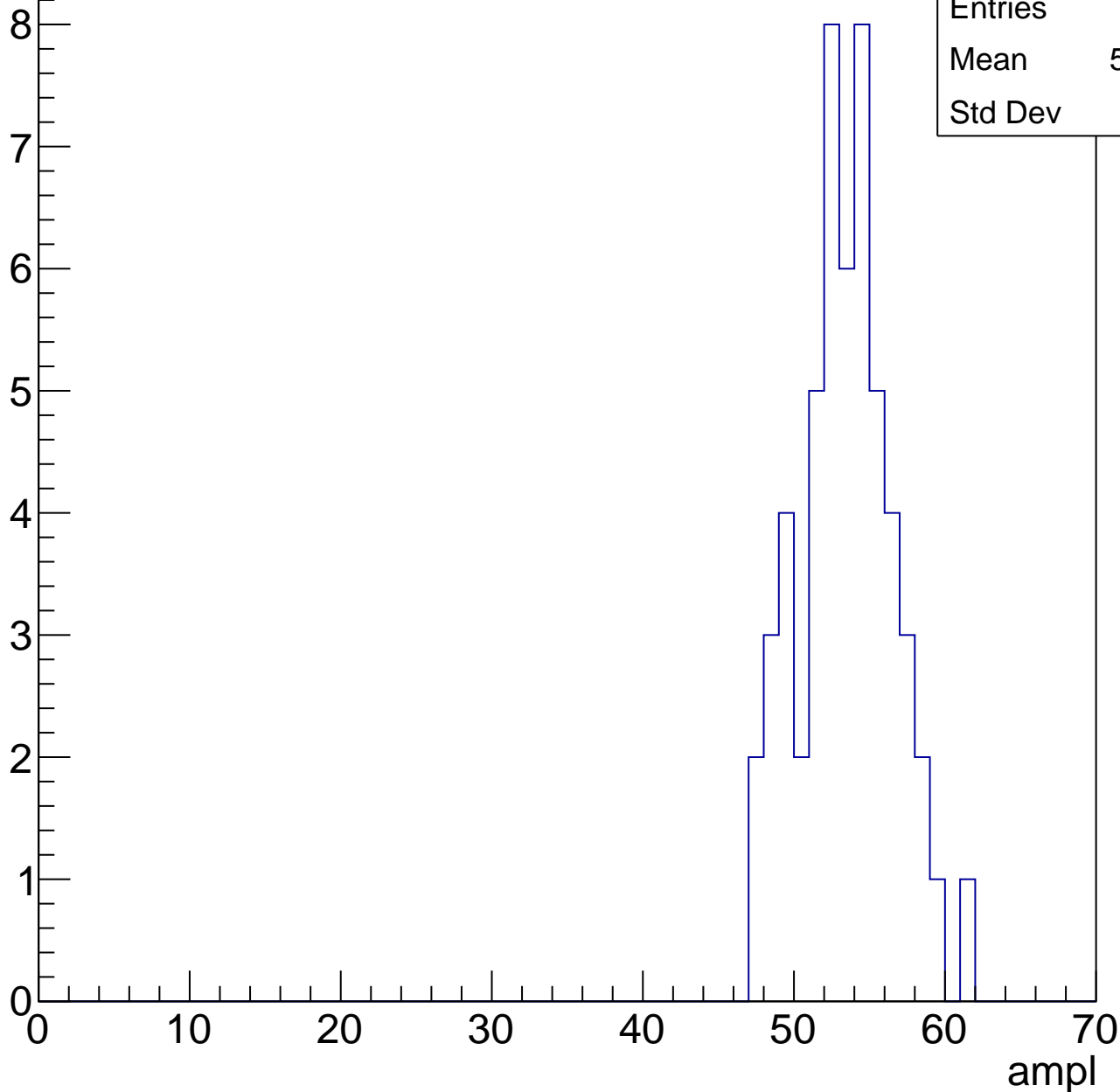


# B1L003S, U18-ch84, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

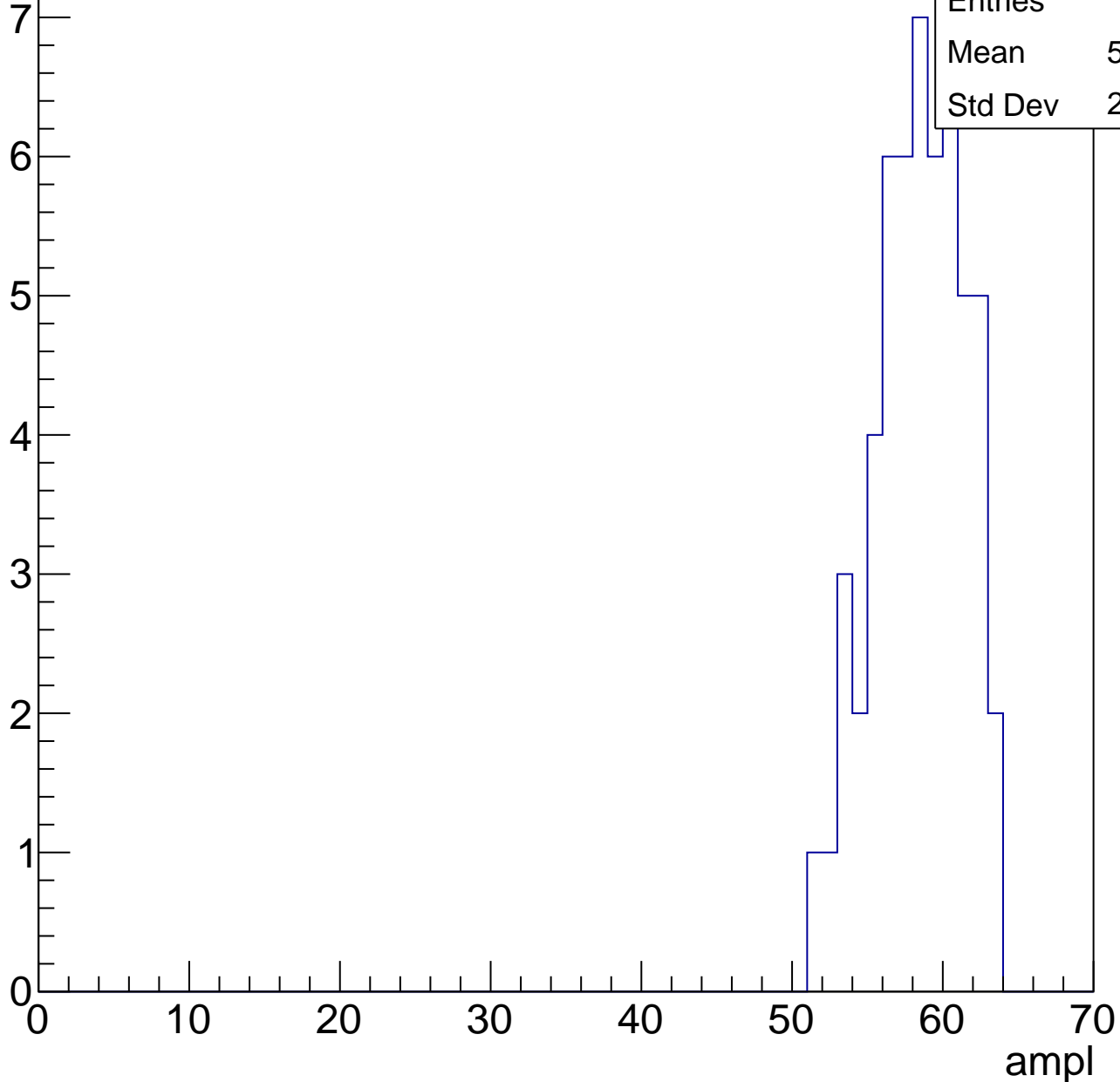
Entries	54
Mean	52.98
Std Dev	3.1



# B1L003S, U18-ch84, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

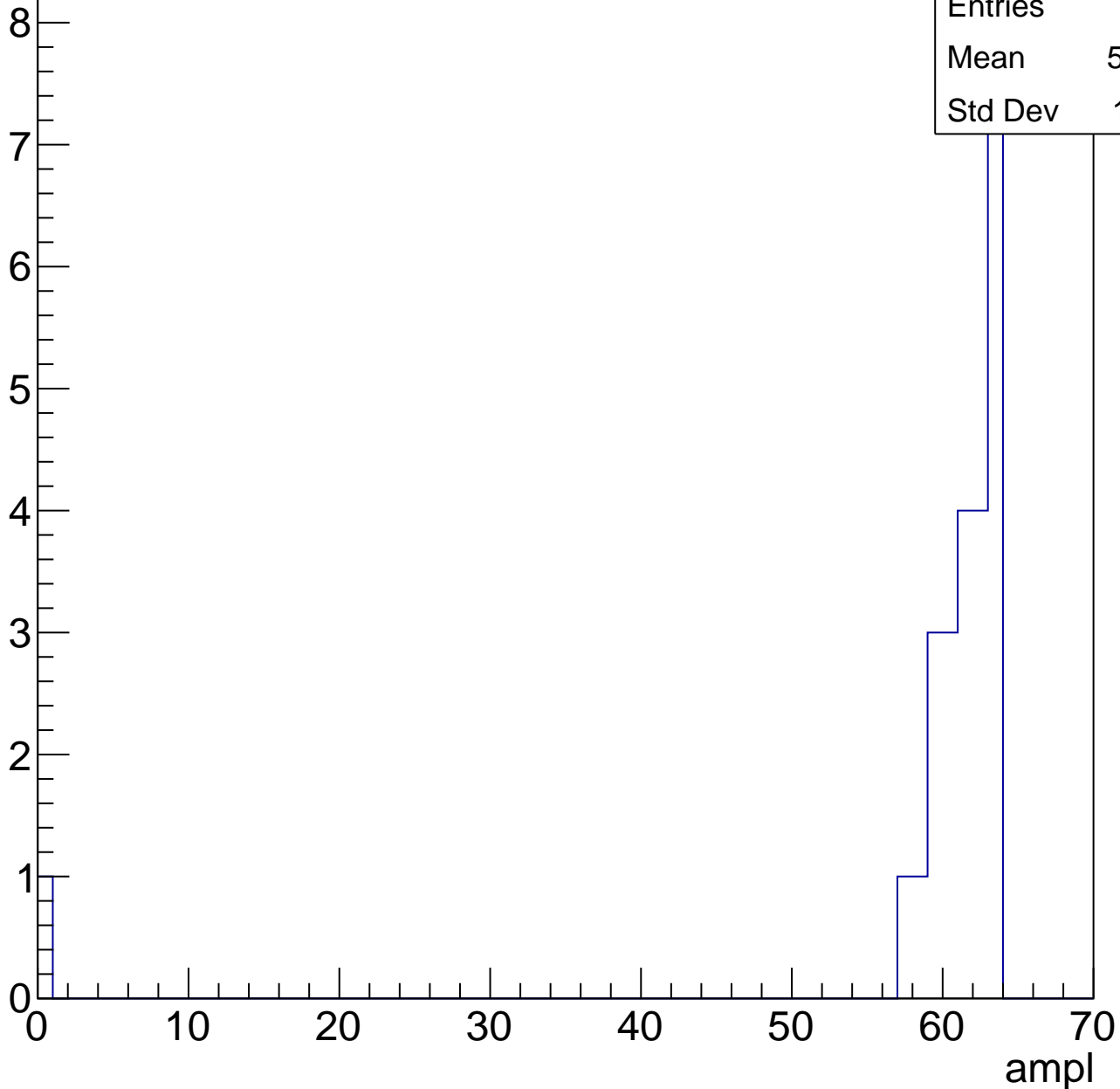


# B1L003S, U18-ch84, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	25
Mean	58.72
Std Dev	12.11





# B1L003S, U18-ch84, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U18-ch85, adc0

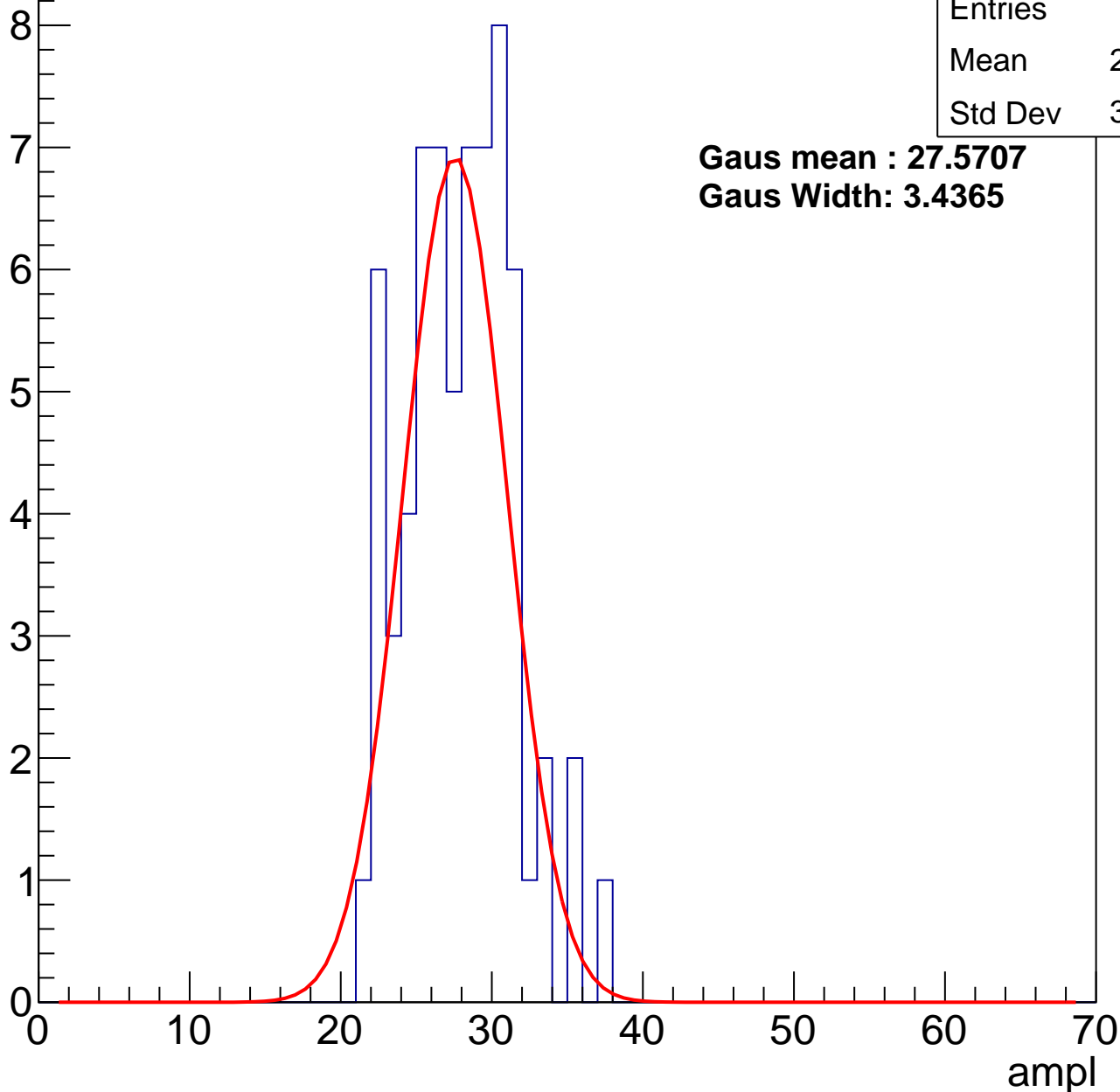
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	67
Mean	27.46
Std Dev	3.496

**Gaus mean : 27.5707**

**Gaus Width: 3.4365**



# B1L003S, U18-ch85, adc1

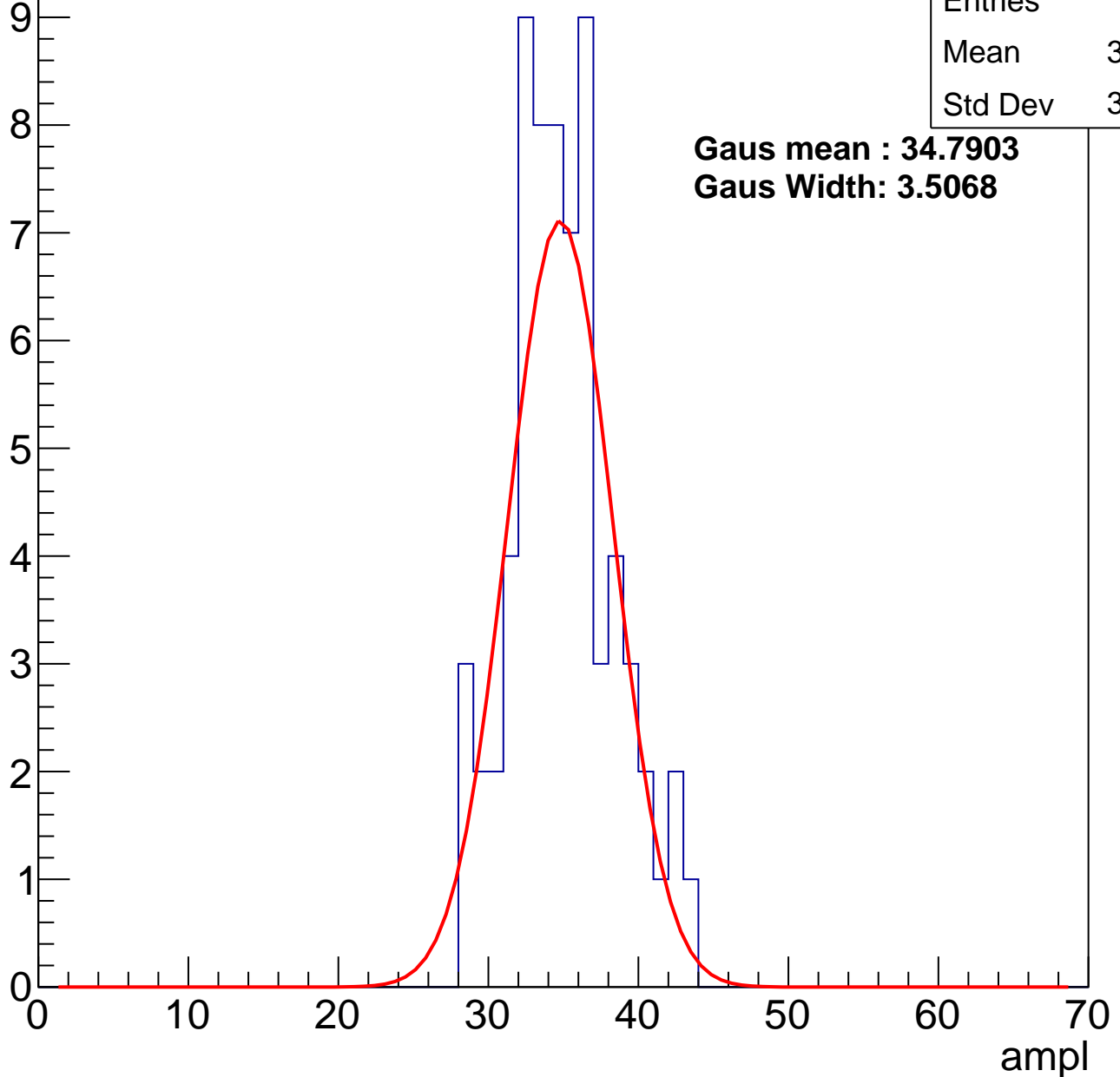
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	68
Mean	34.51
Std Dev	3.411

**Gaus mean : 34.7903**

**Gaus Width: 3.5068**



# B1L003S, U18-ch85, adc2

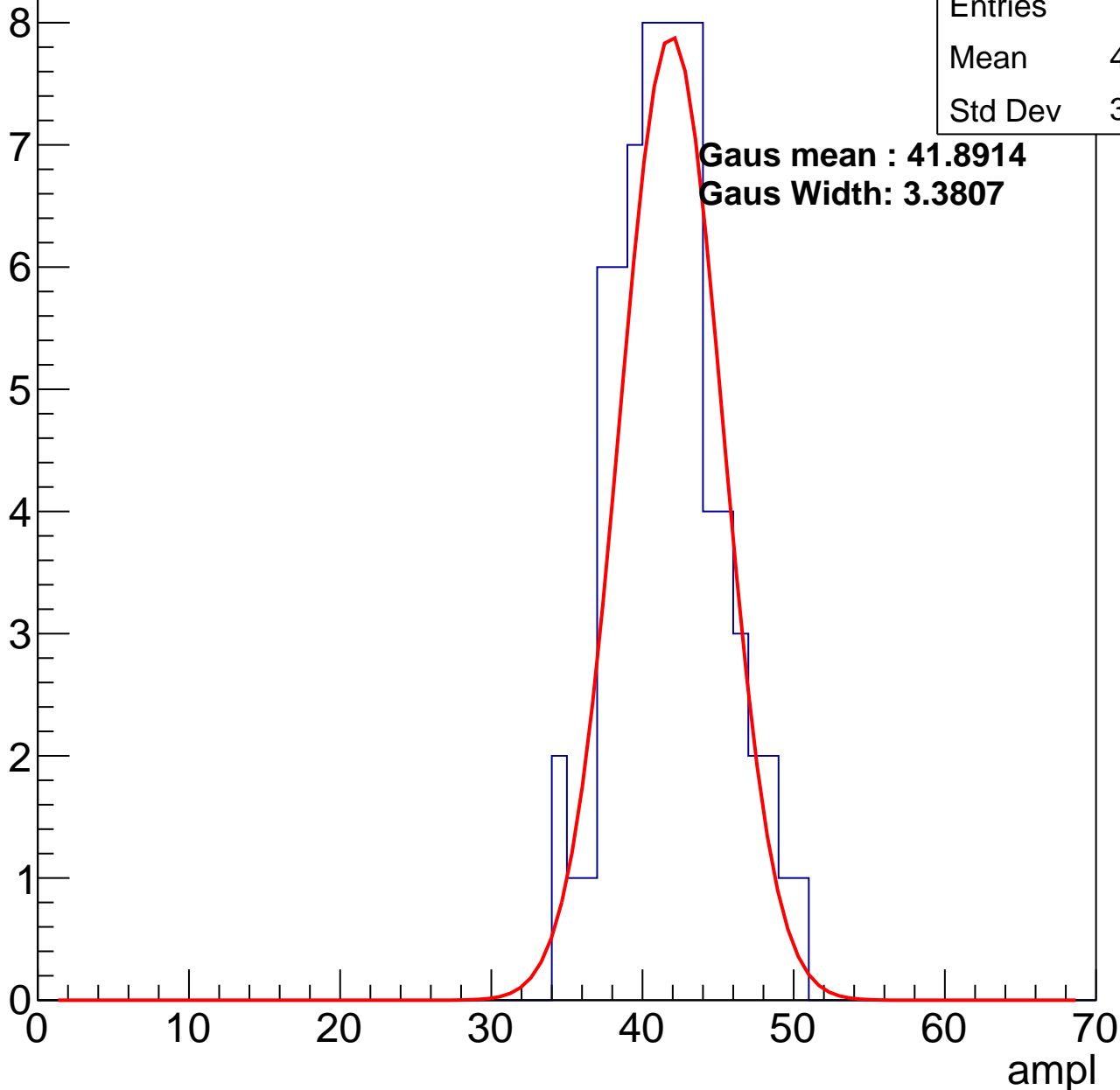
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	72
Mean	41.29
Std Dev	3.474

**Gaus mean : 41.8914**

**Gaus Width: 3.3807**

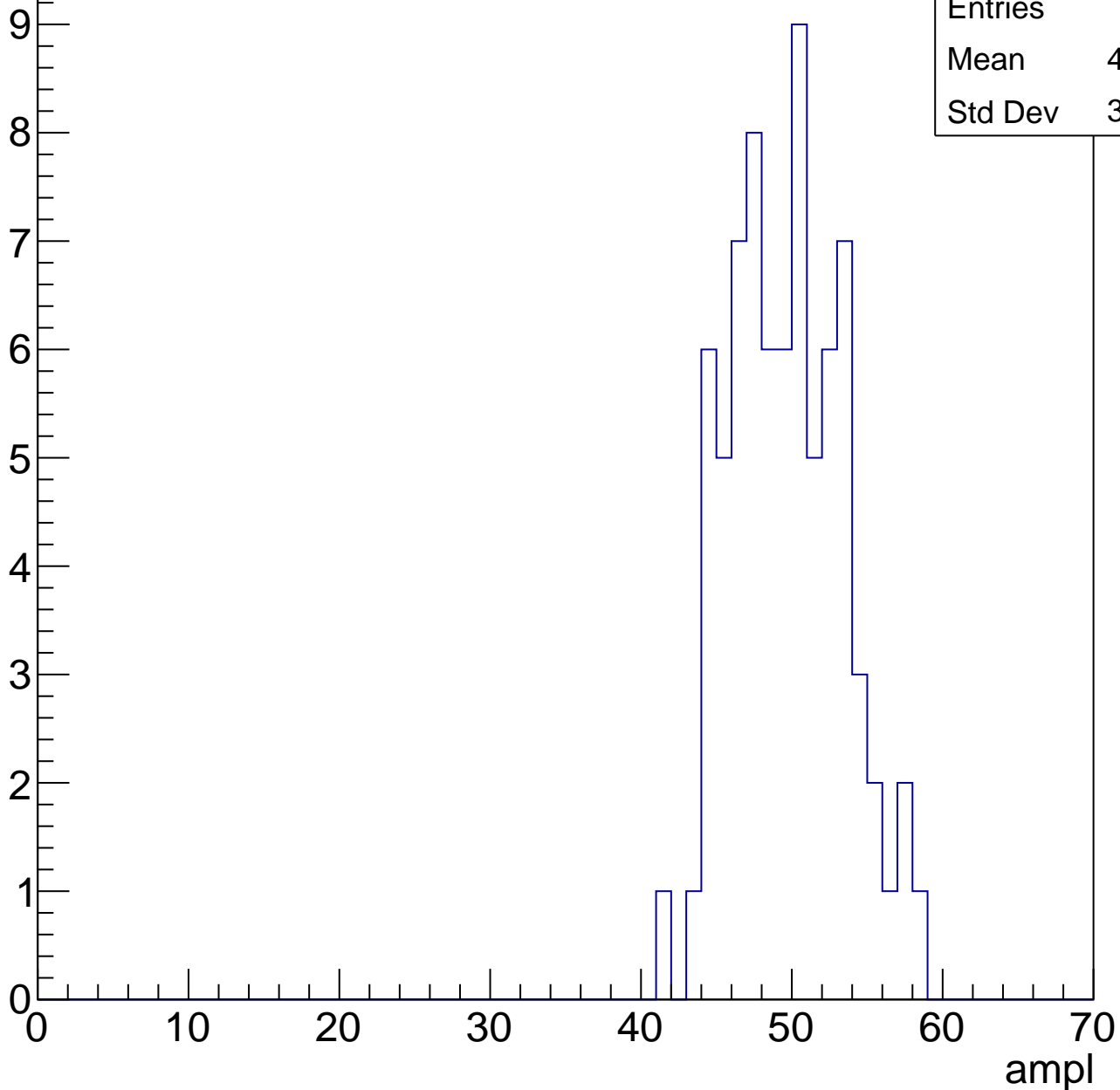


# B1L003S, U18-ch85, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	76
Mean	49.22
Std Dev	3.676

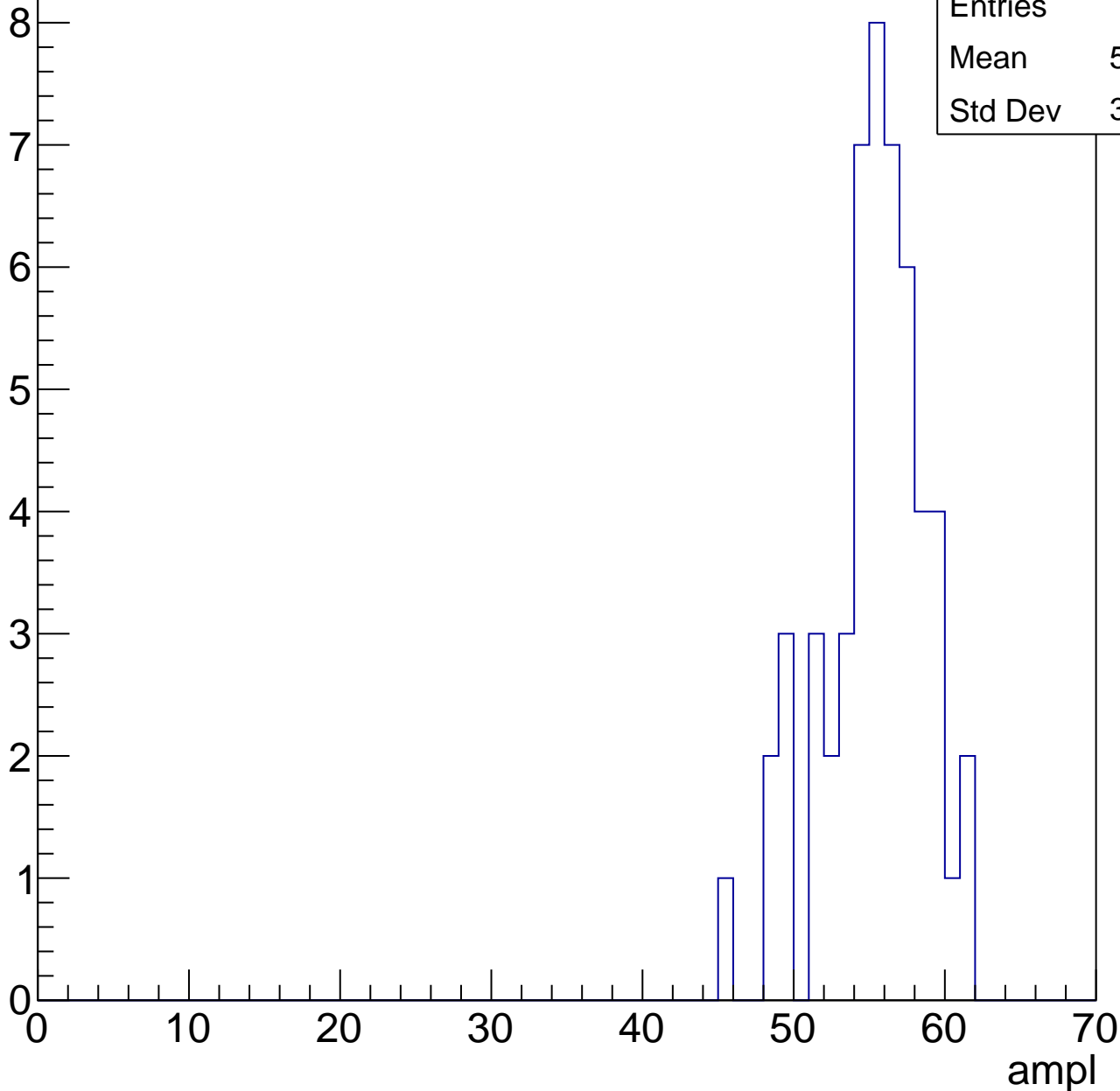


# B1L003S, U18-ch85, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	53
Mean	54.83
Std Dev	3.413



# B1L003S, U18-ch85, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

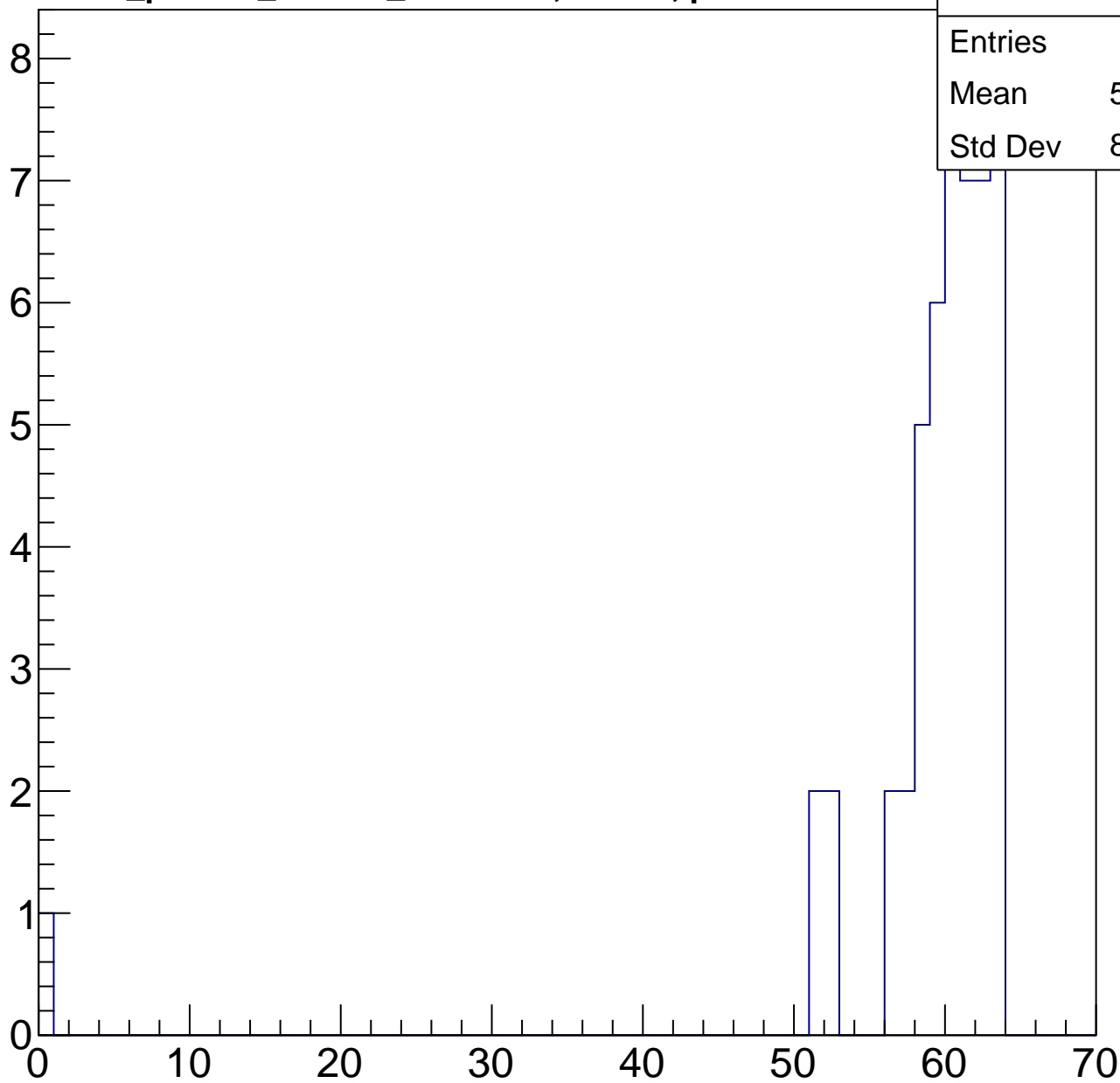
Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	50
Mean	58.42
Std Dev	8.886

ampl

0 10 20 30 40 50 60 70



# B1L003S, U18-ch85, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

3

2.5

2

1.5

1

0.5

0

0

10

20

30

40

50

60

70

ampl

Entries

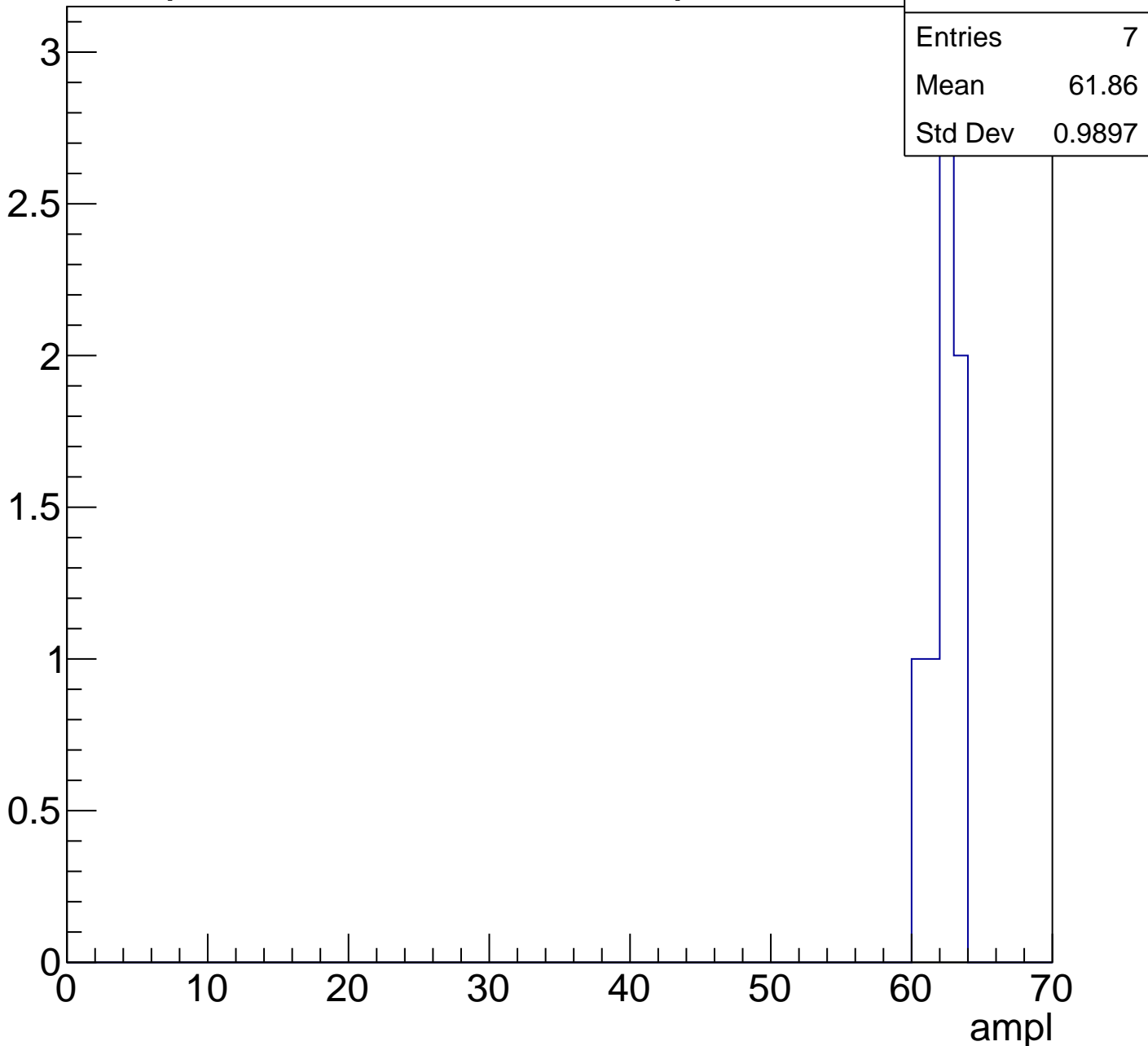
7

Mean

61.86

Std Dev

0.9897





# B1L003S, U18-ch85, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L003S, U18-ch86, adc0

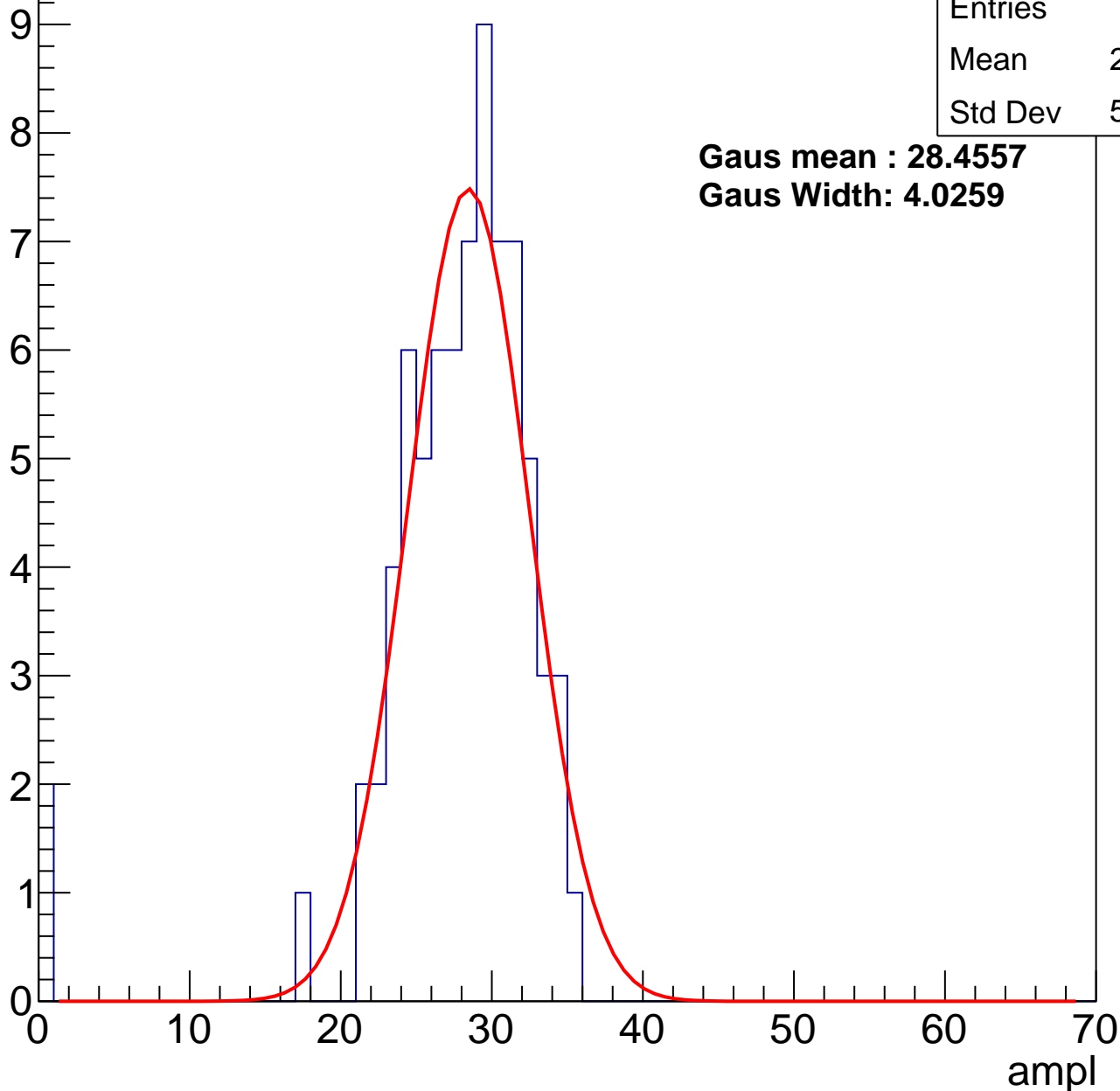
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	76
Mean	27.13
Std Dev	5.718

**Gaus mean : 28.4557**

**Gaus Width: 4.0259**



# B1L003S, U18-ch86, adc1

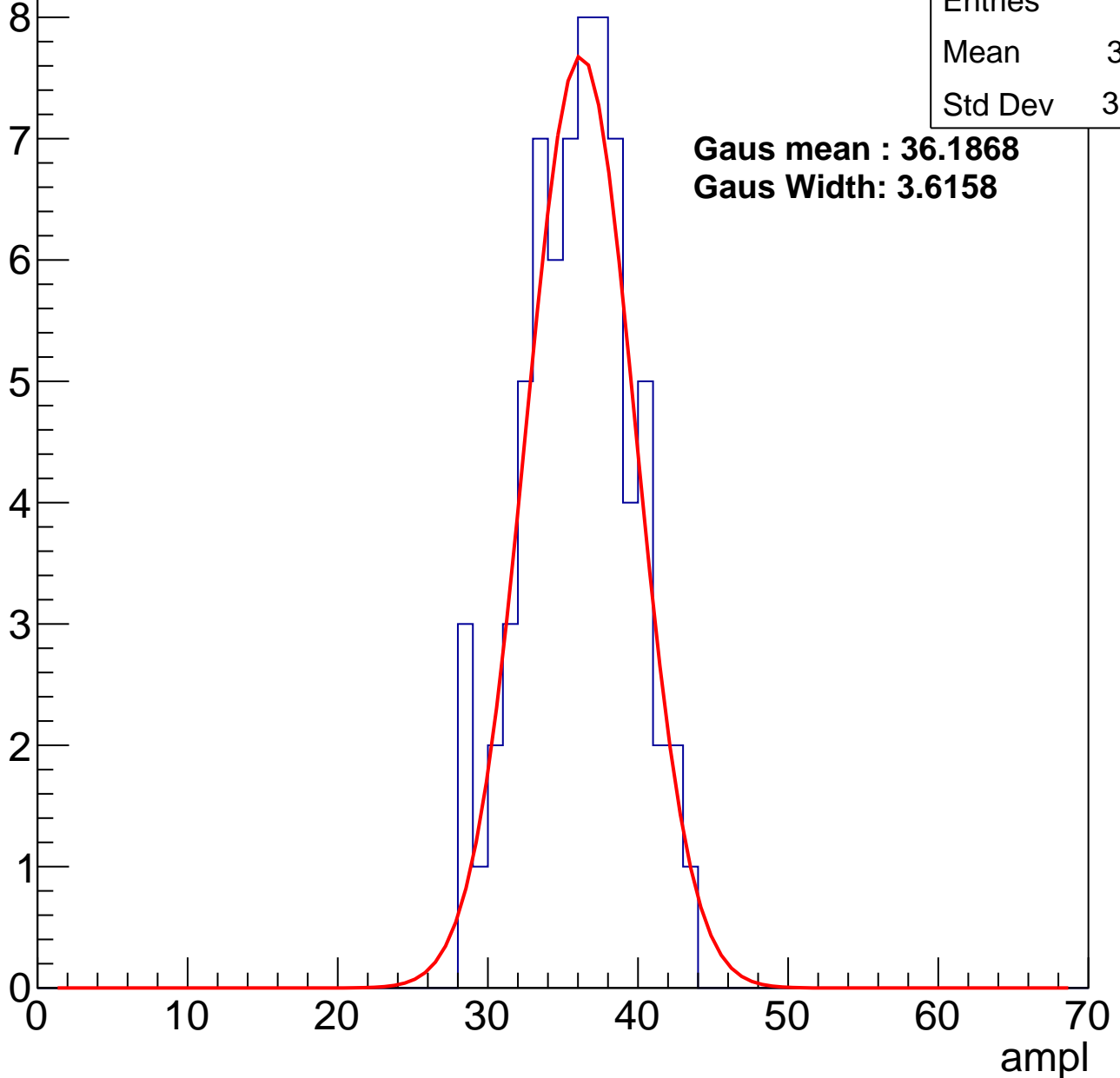
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	71
Mean	35.51
Std Dev	3.496

**Gaus mean : 36.1868**

**Gaus Width: 3.6158**



# B1L003S, U18-ch86, adc2

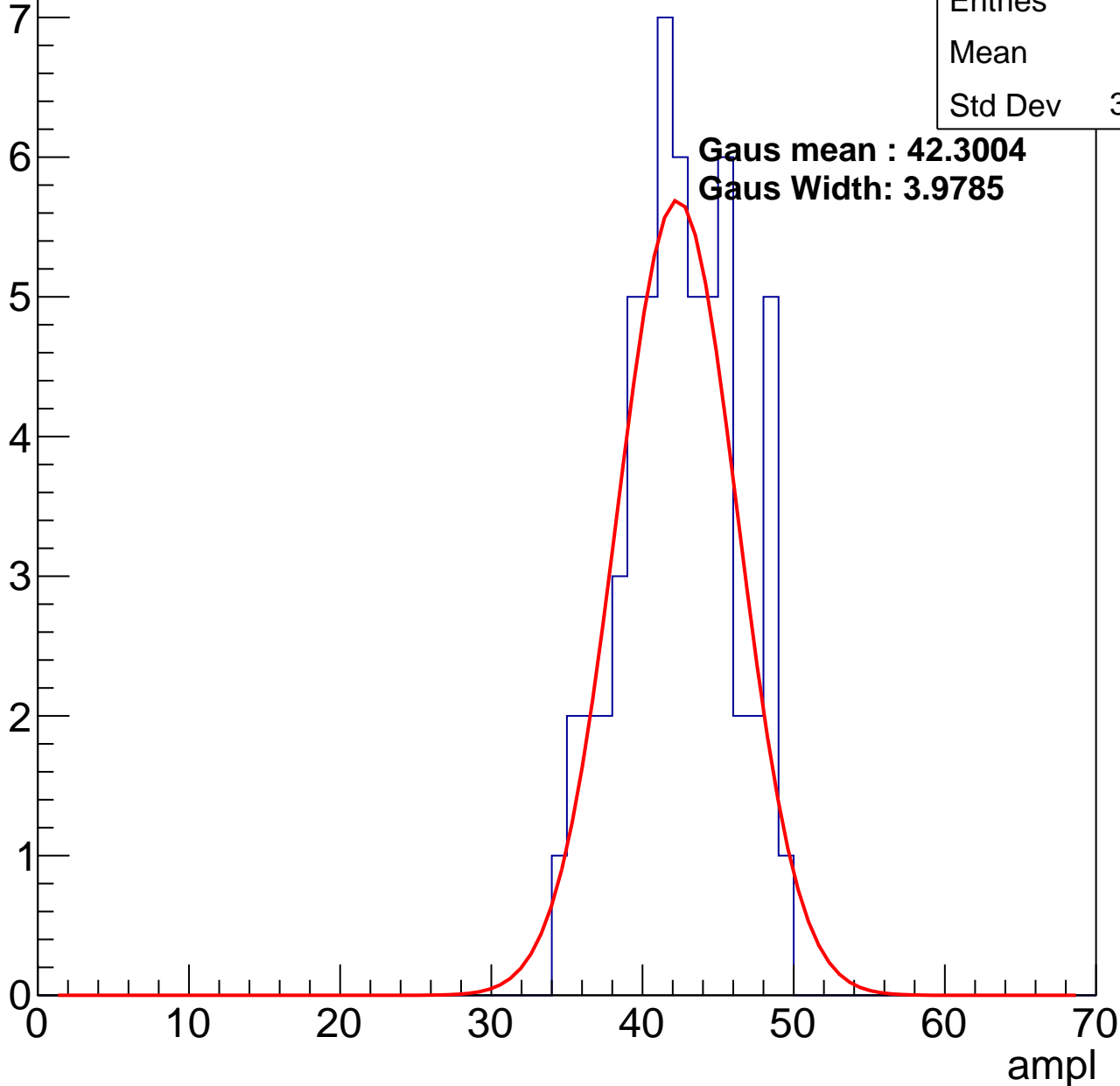
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	59
Mean	42
Std Dev	3.668

**Gaus mean : 42.3004**

**Gaus Width: 3.9785**

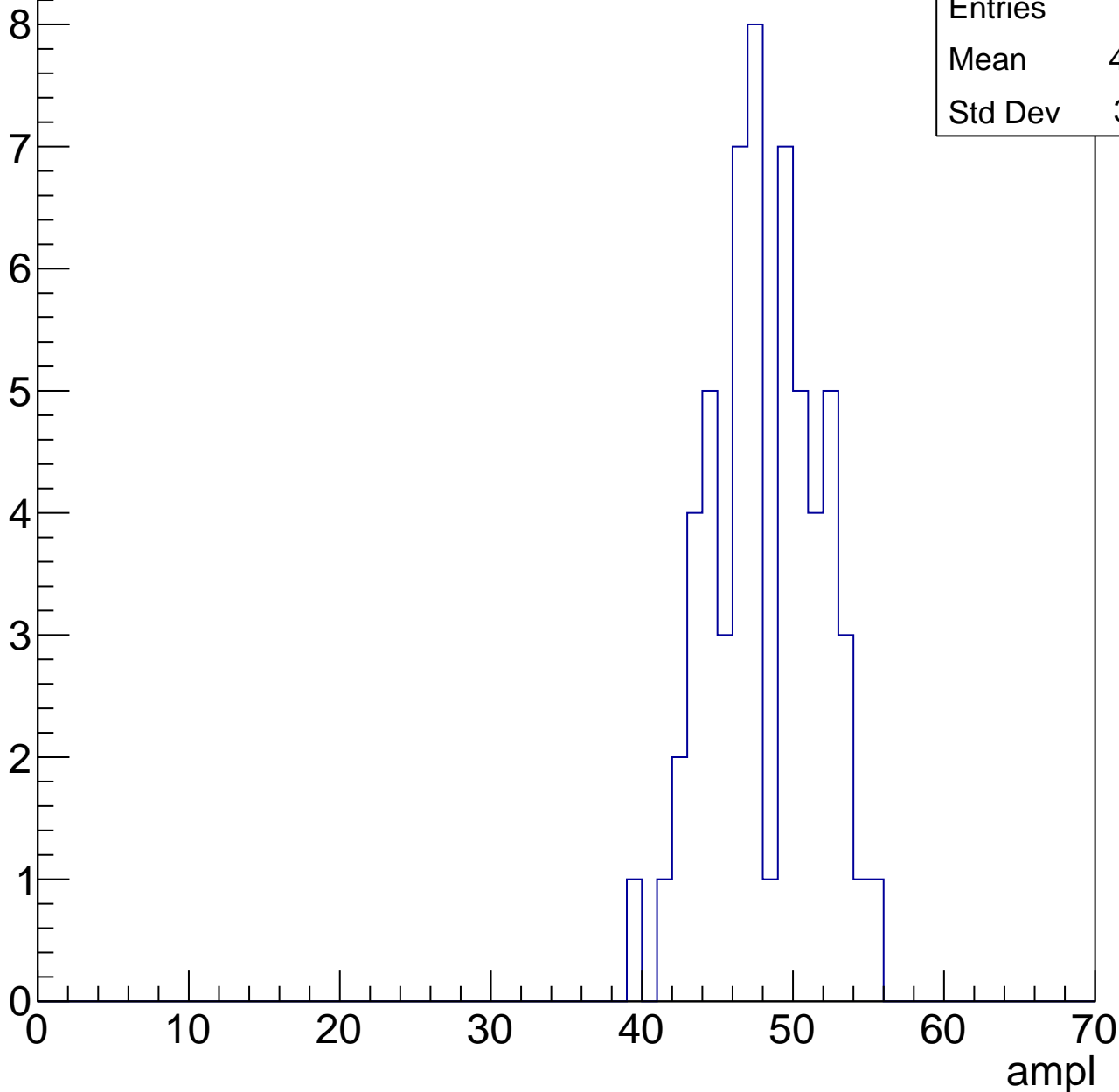


# B1L003S, U18-ch86, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	58
Mean	47.62
Std Dev	3.571

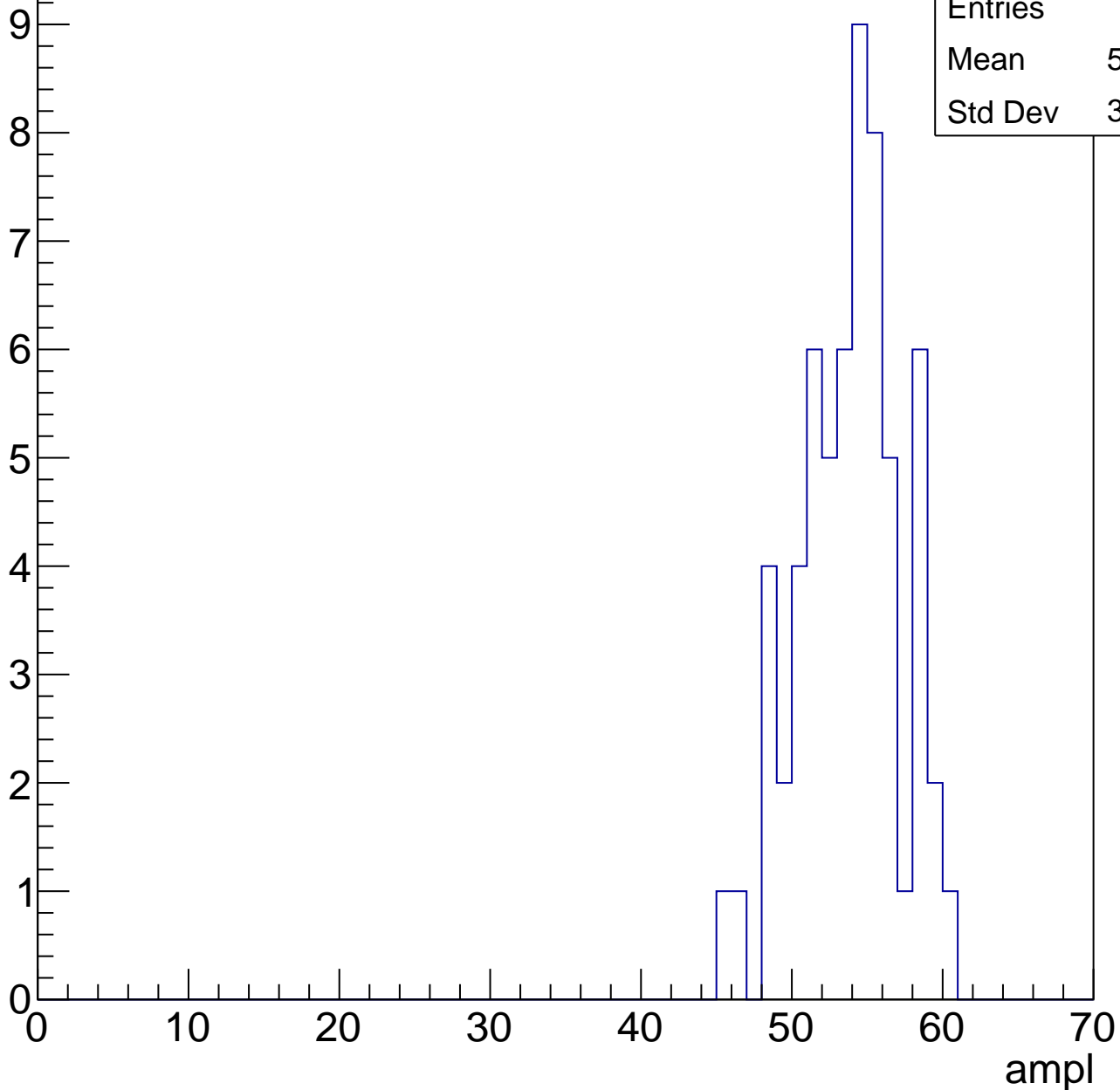


# B1L003S, U18-ch86, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

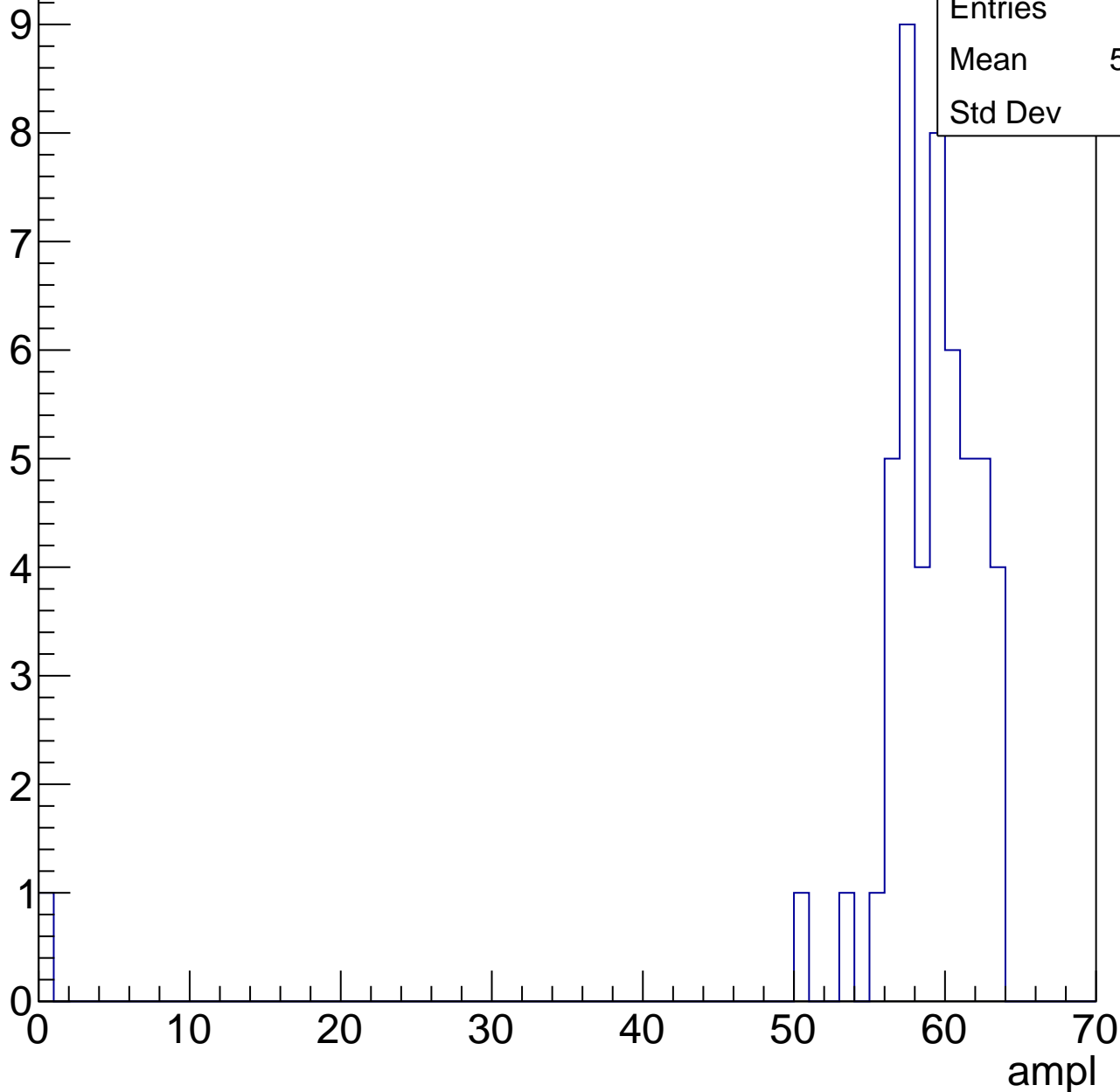
Entries	61
Mean	53.34
Std Dev	3.328



# B1L003S, U18-ch86, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

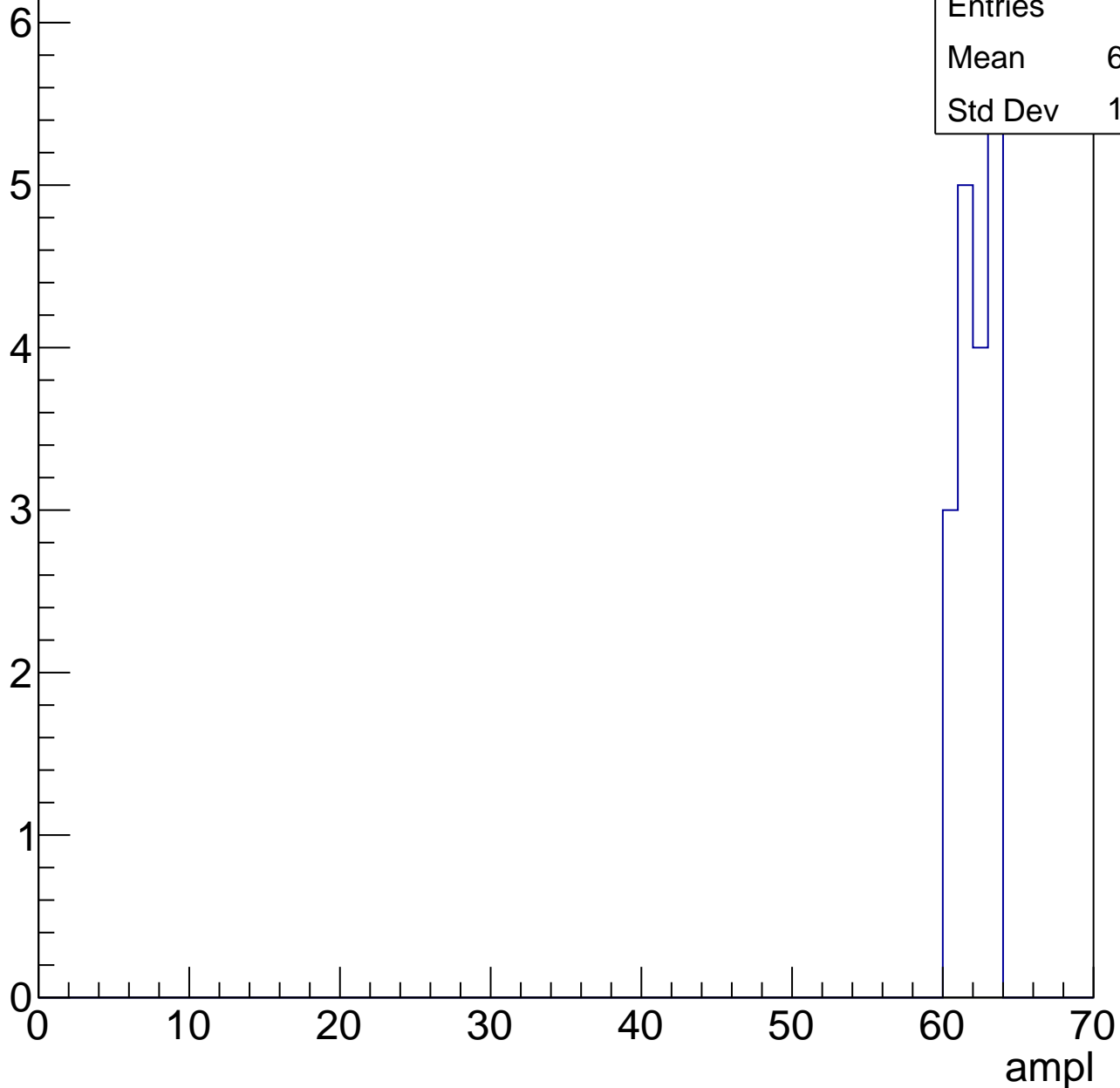


# B1L003S, U18-ch86, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	18
Mean	61.72
Std Dev	1.096

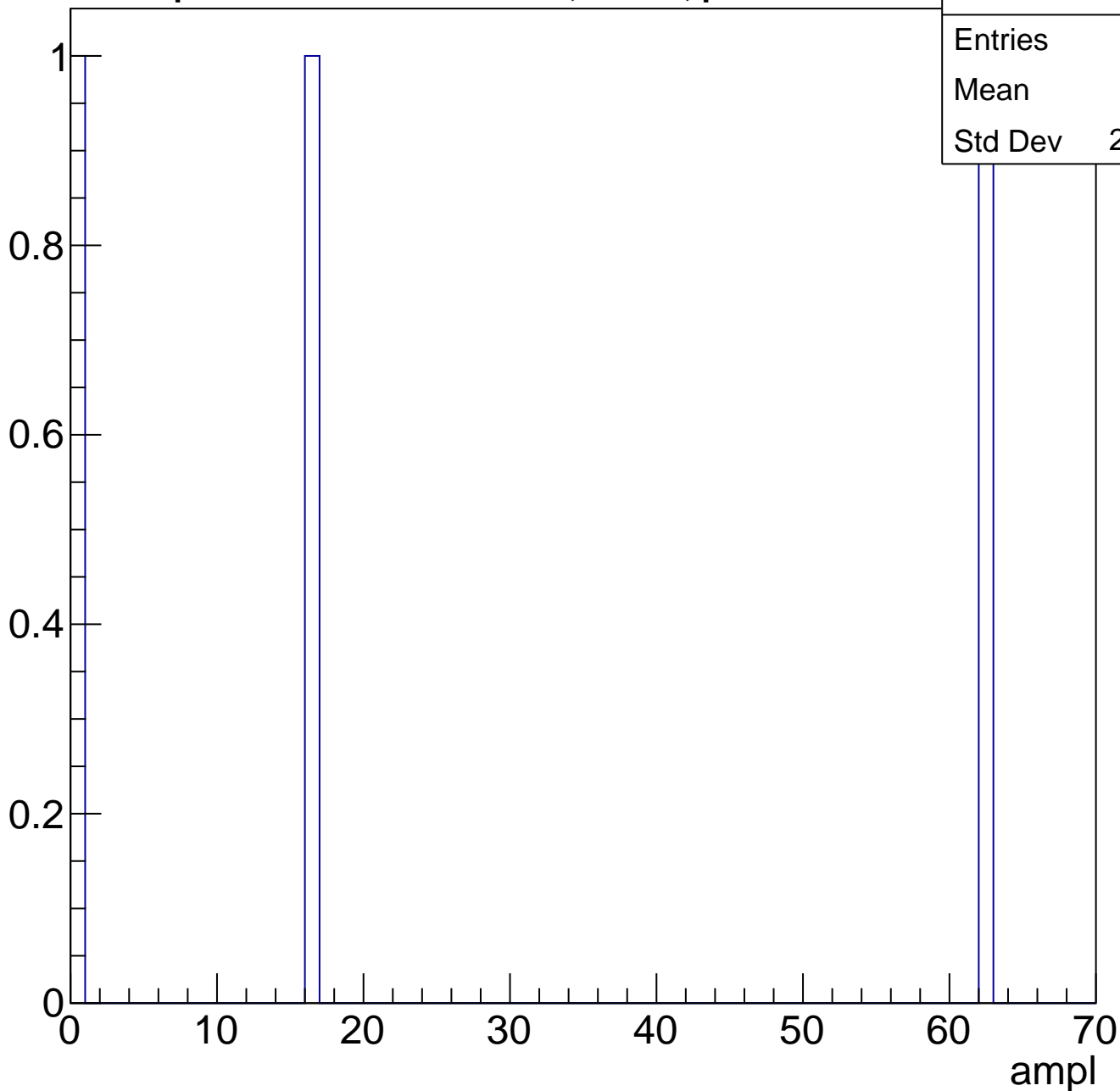




# B1L003S, U18-ch86, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	3
Mean	26
Std Dev	26.28

# B1L003S, U18-ch87, adc0

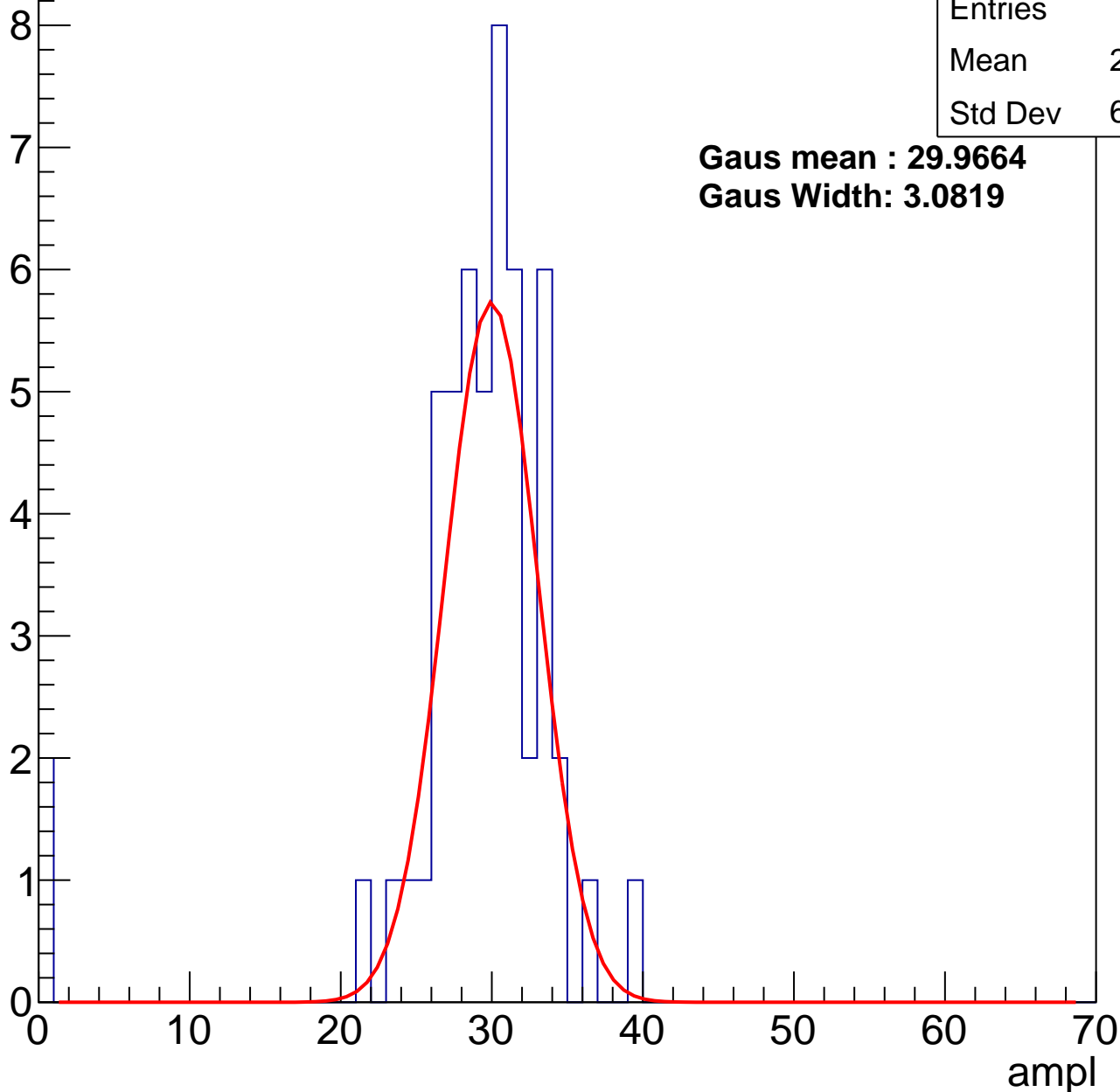
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	53
Mean	28.34
Std Dev	6.466

**Gaus mean : 29.9664**

**Gaus Width: 3.0819**



# B1L003S, U18-ch87, adc1

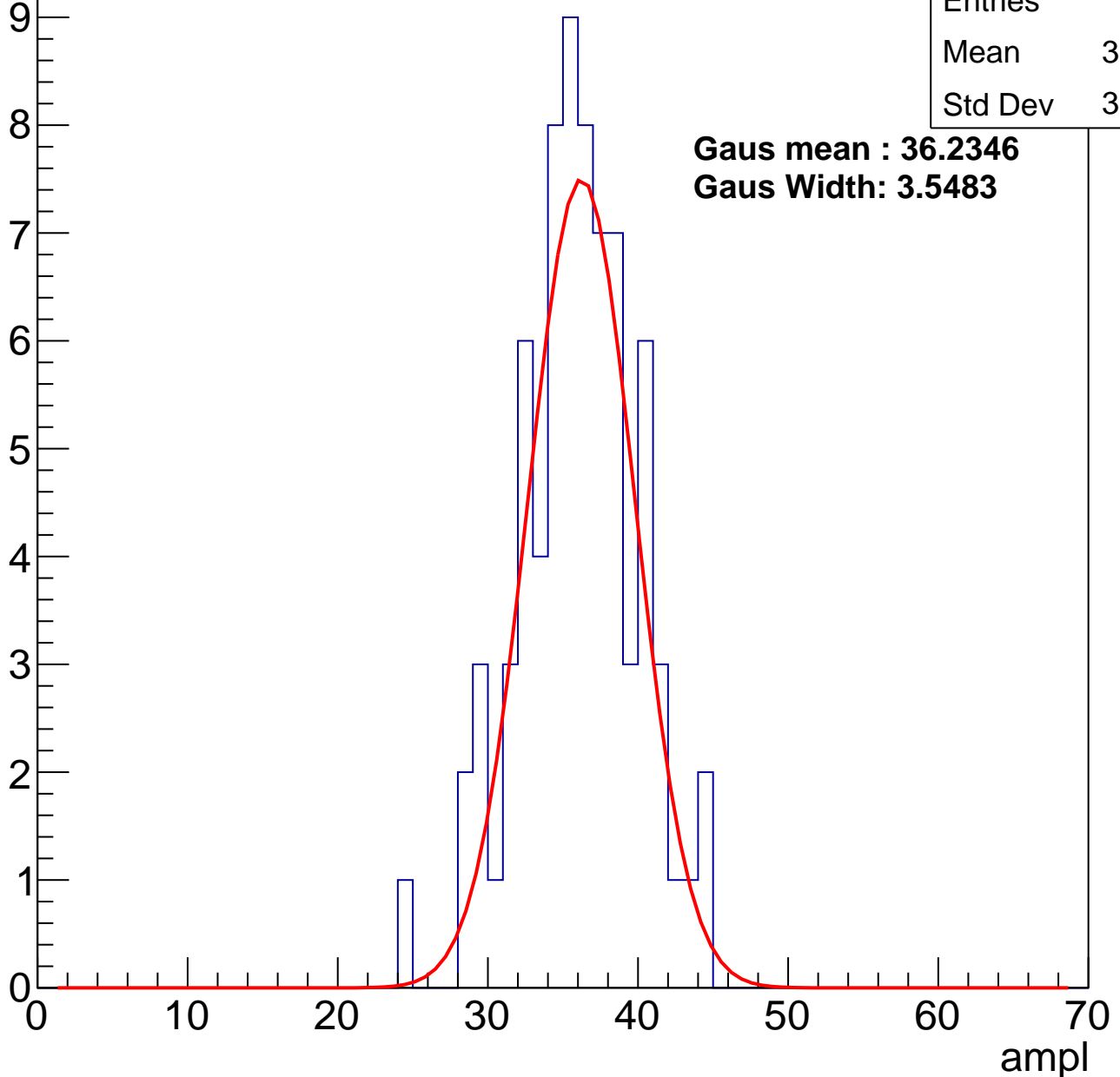
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	75
Mean	35.56
Std Dev	3.889

**Gaus mean : 36.2346**

**Gaus Width: 3.5483**



# B1L003S, U18-ch87, adc2

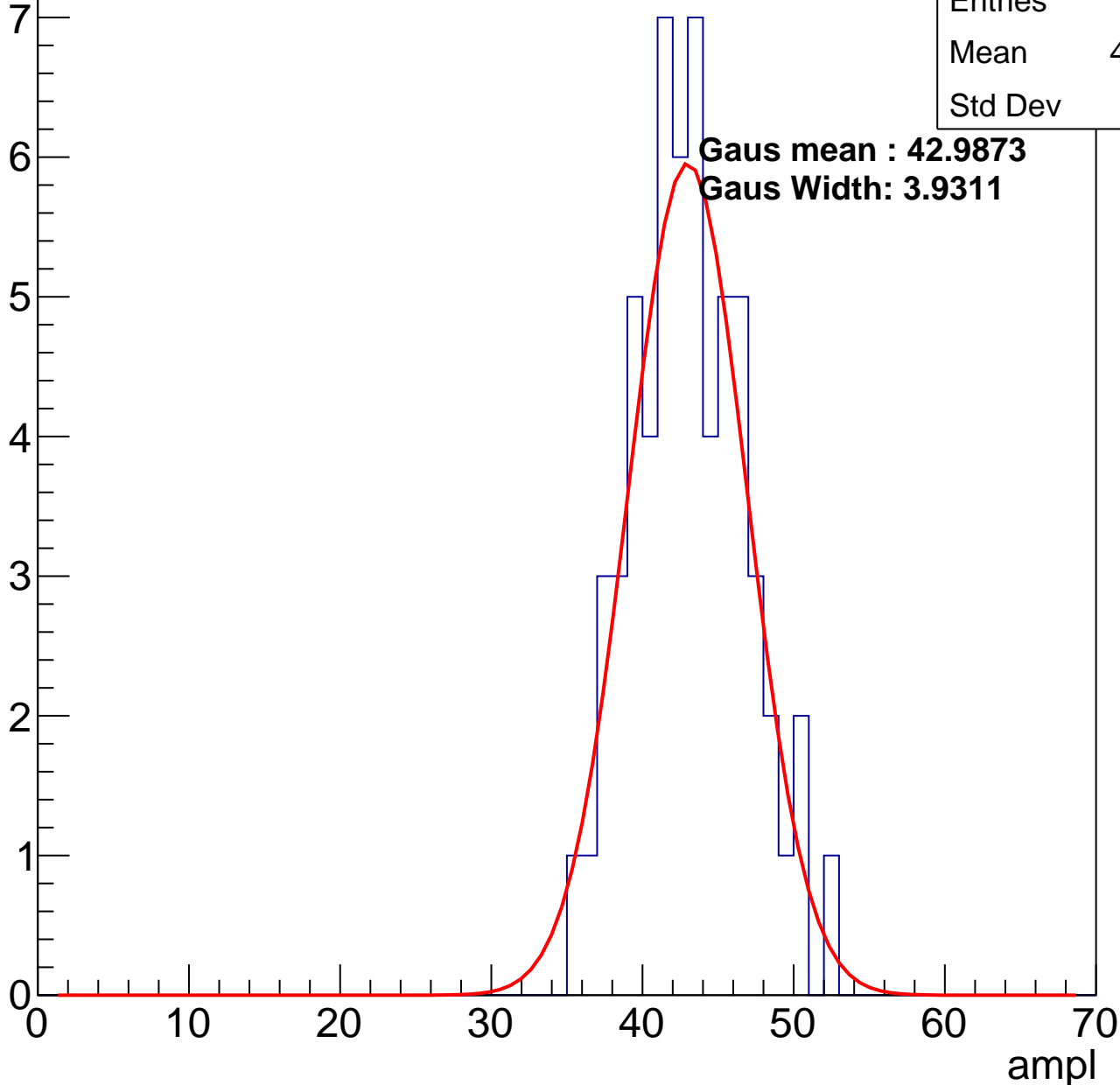
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	60
Mean	42.67
Std Dev	3.7

**Gaus mean : 42.9873**

**Gaus Width: 3.9311**

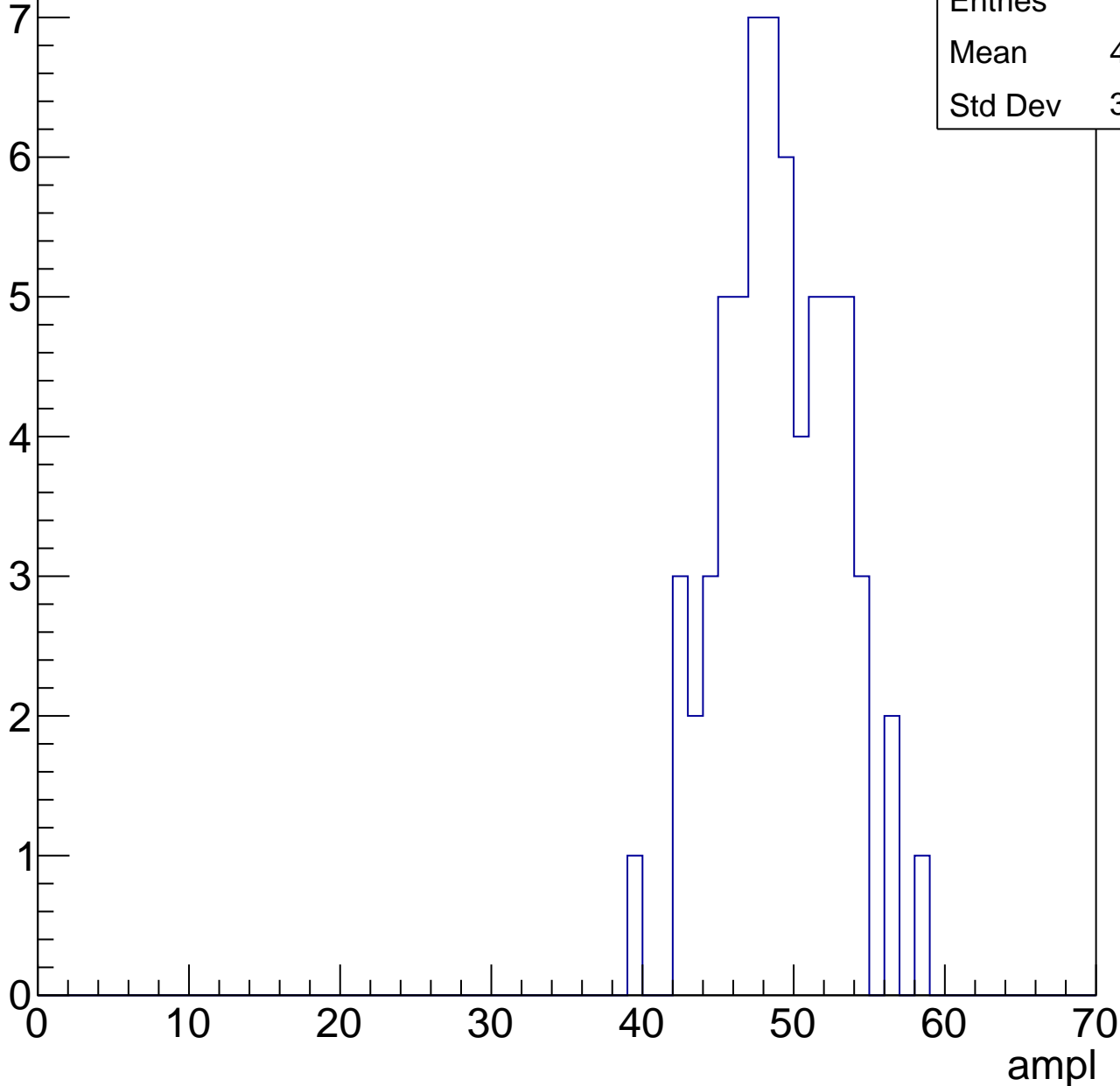


# B1L003S, U18-ch87, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	64
Mean	48.58
Std Dev	3.844

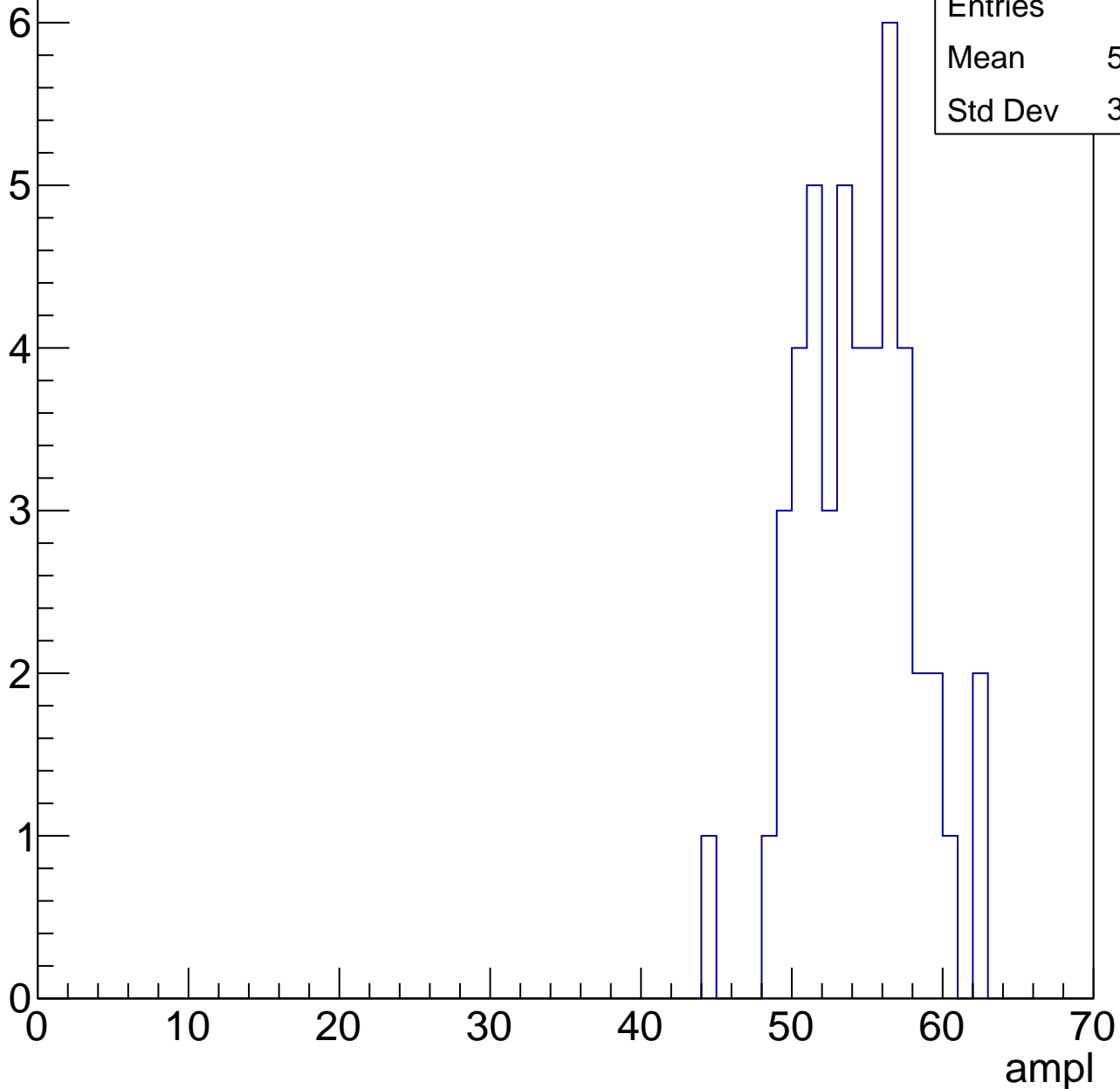


# B1L003S, U18-ch87, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

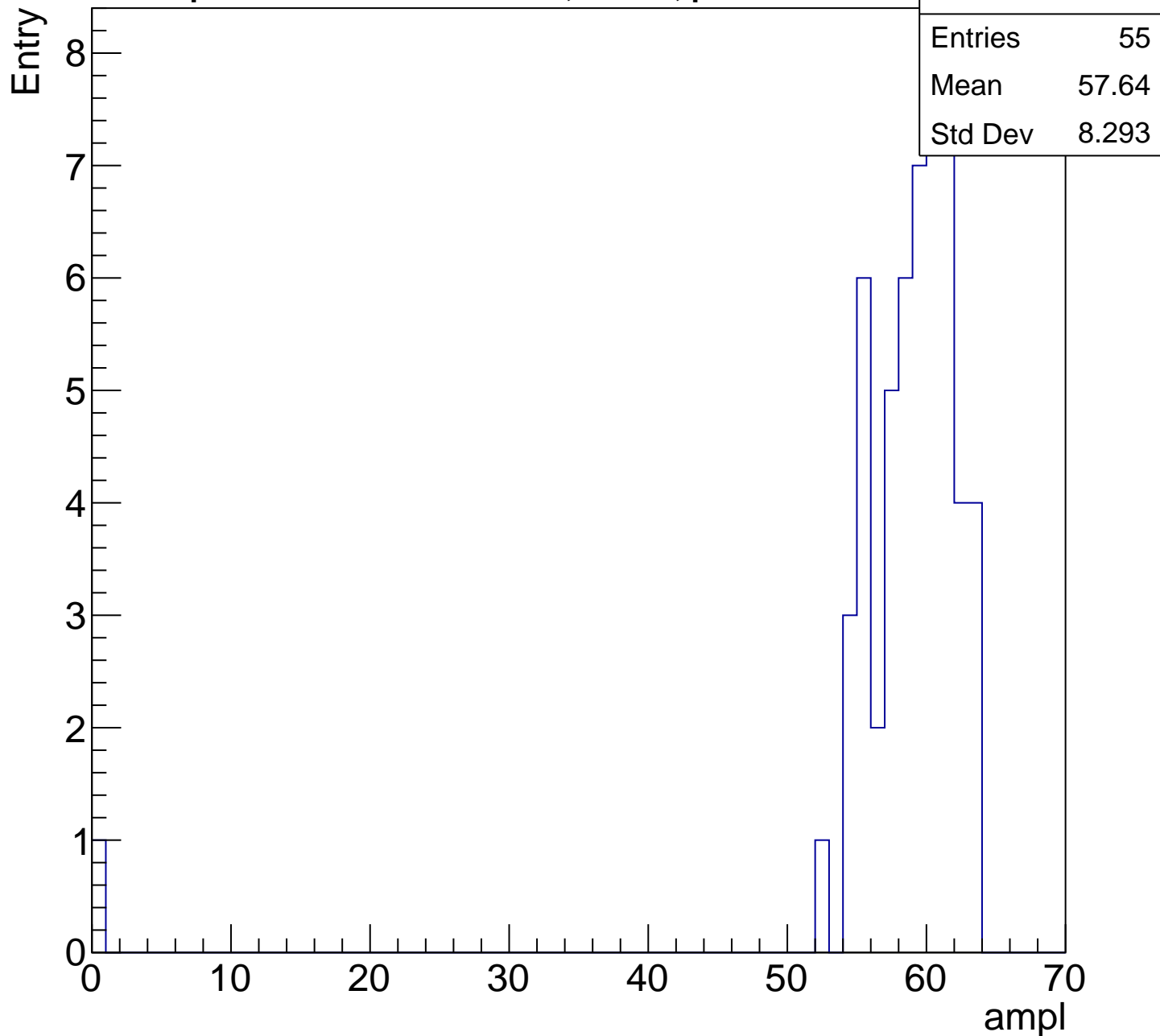
Entry

Entries	47
Mean	53.89
Std Dev	3.709



# B1L003S, U18-ch87, adc5

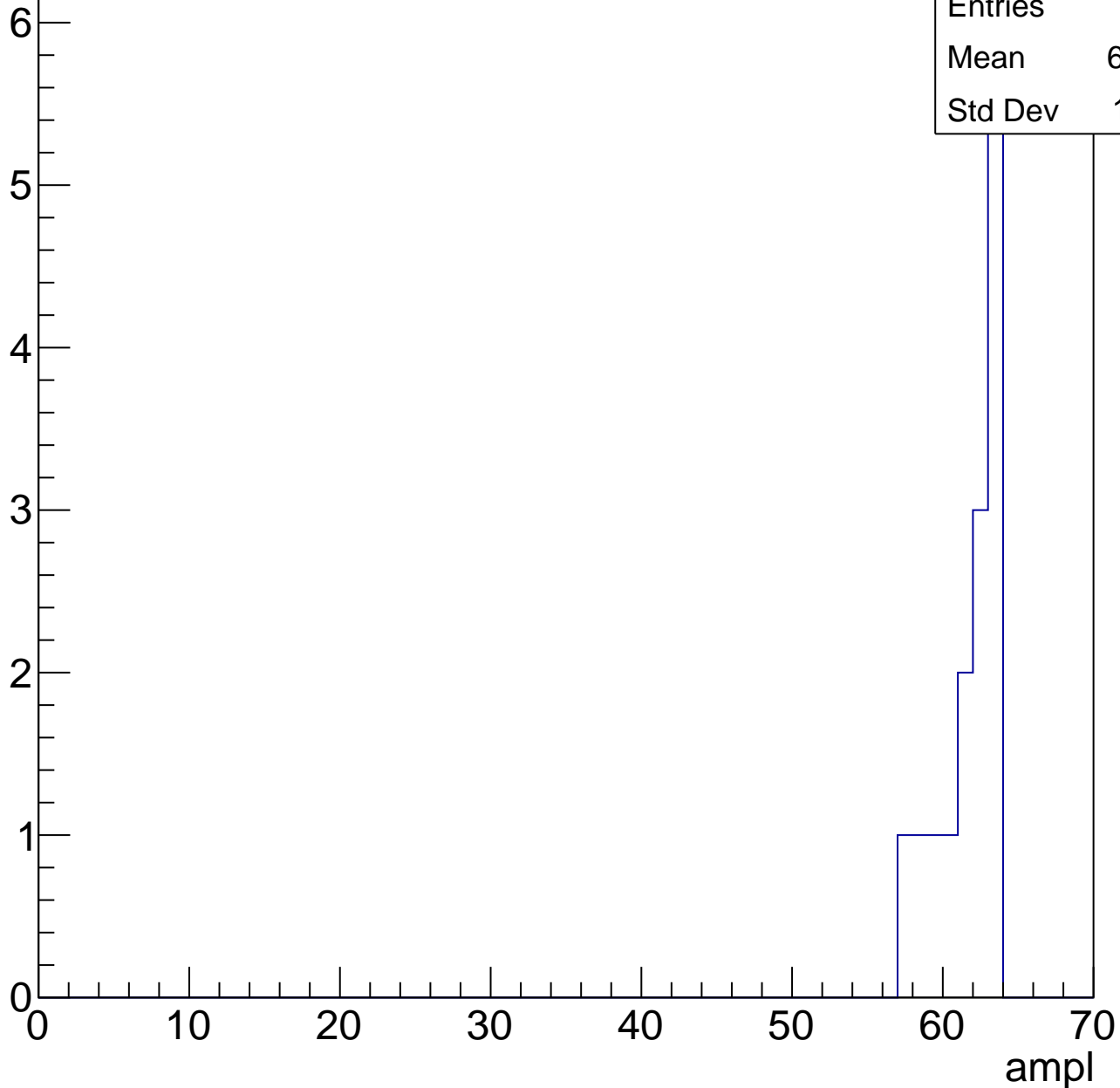
calib\_packv5\_042523\_0143.root, FC#13, port D2



# B1L003S, U18-ch87, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

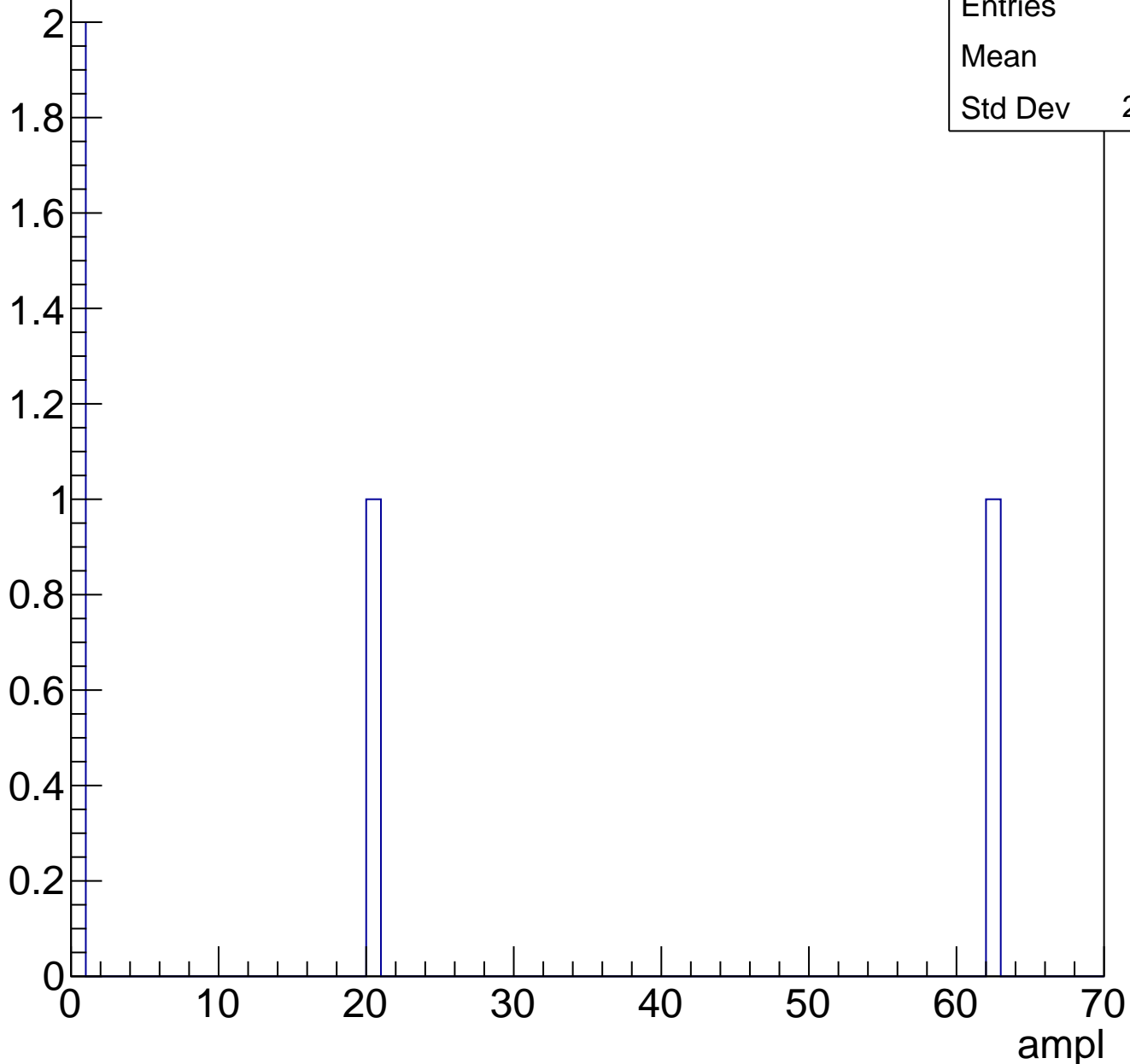




# B1L003S, U18-ch87, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	4
Mean	20.5
Std Dev	25.31

# B1L003S, U18-ch88, adc0

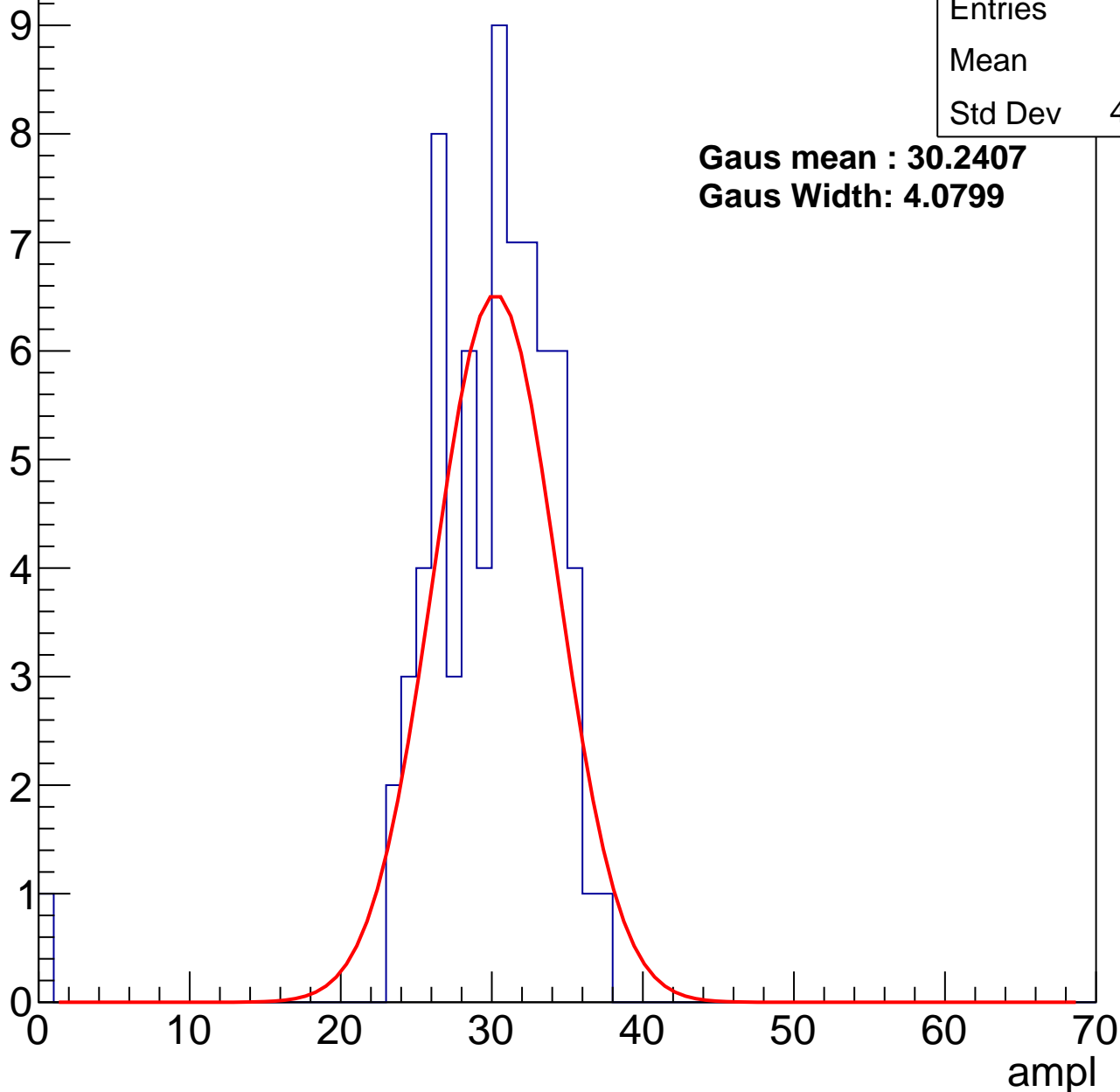
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	72
Mean	29.4
Std Dev	4.907

**Gaus mean : 30.2407**

**Gaus Width: 4.0799**



# B1L003S, U18-ch88, adc1

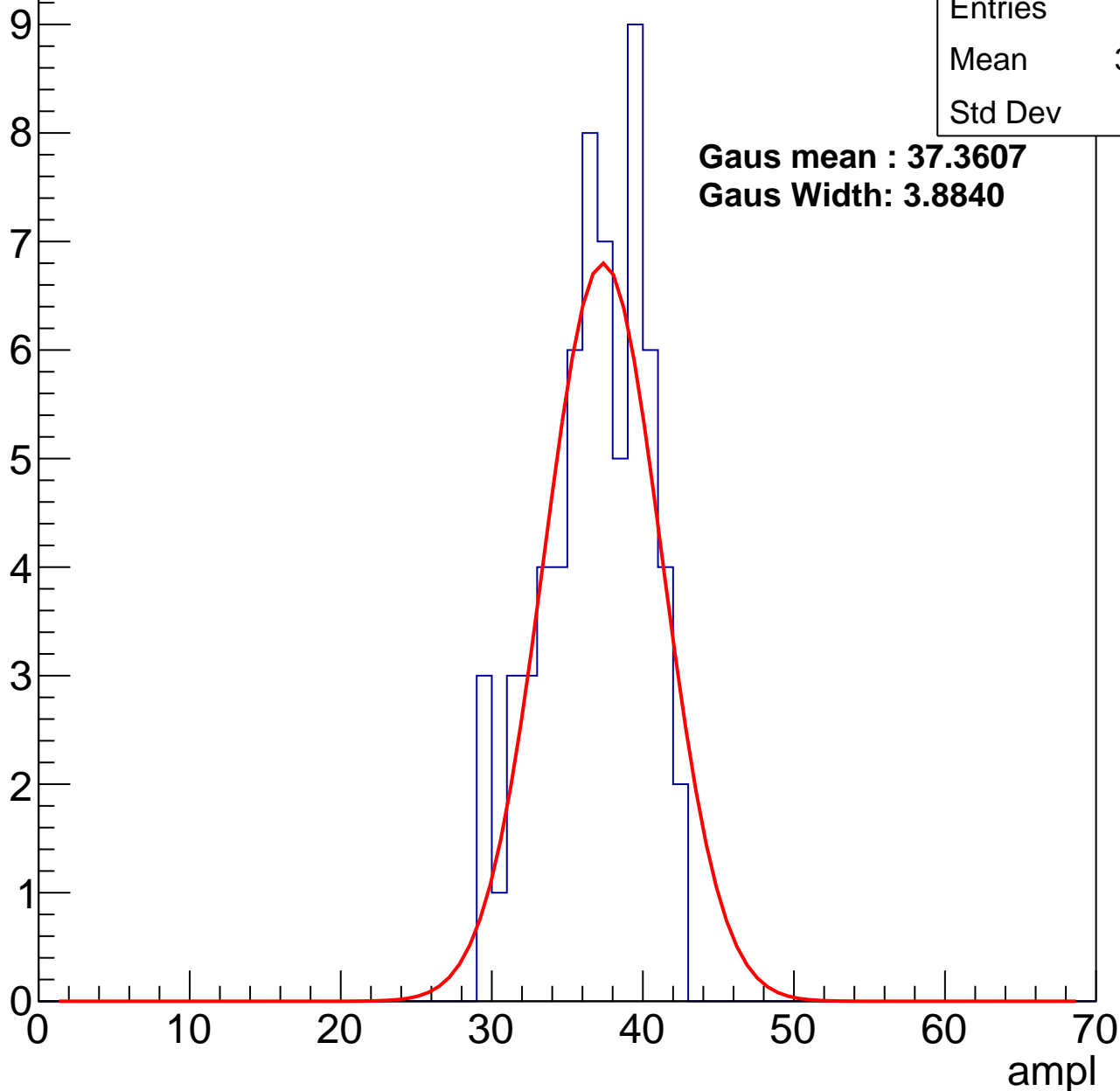
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	65
Mean	36.31
Std Dev	3.36

**Gaus mean : 37.3607**

**Gaus Width: 3.8840**



# B1L003S, U18-ch88, adc2

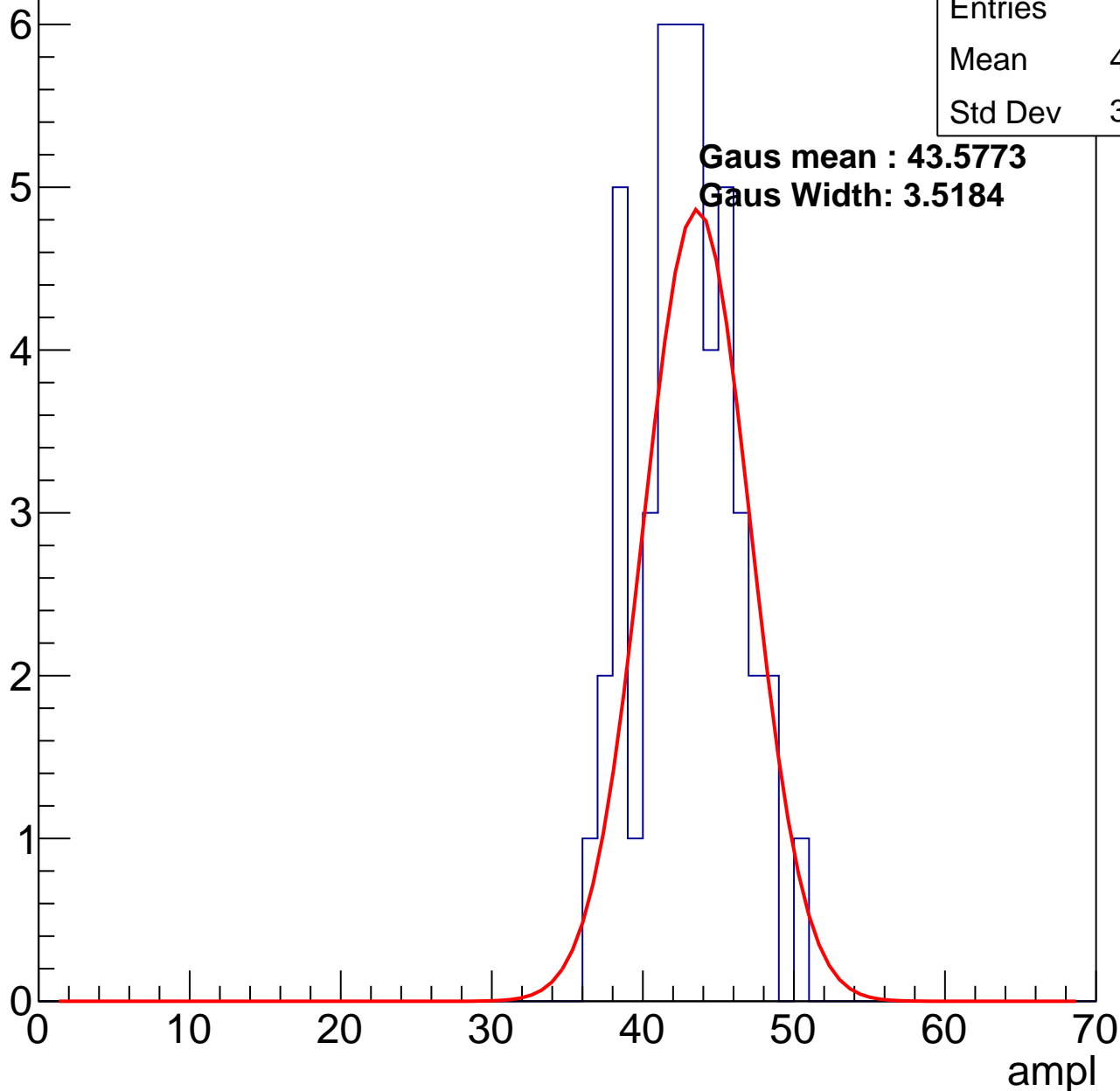
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	47
Mean	42.43
Std Dev	3.214

**Gaus mean : 43.5773**

**Gaus Width: 3.5184**

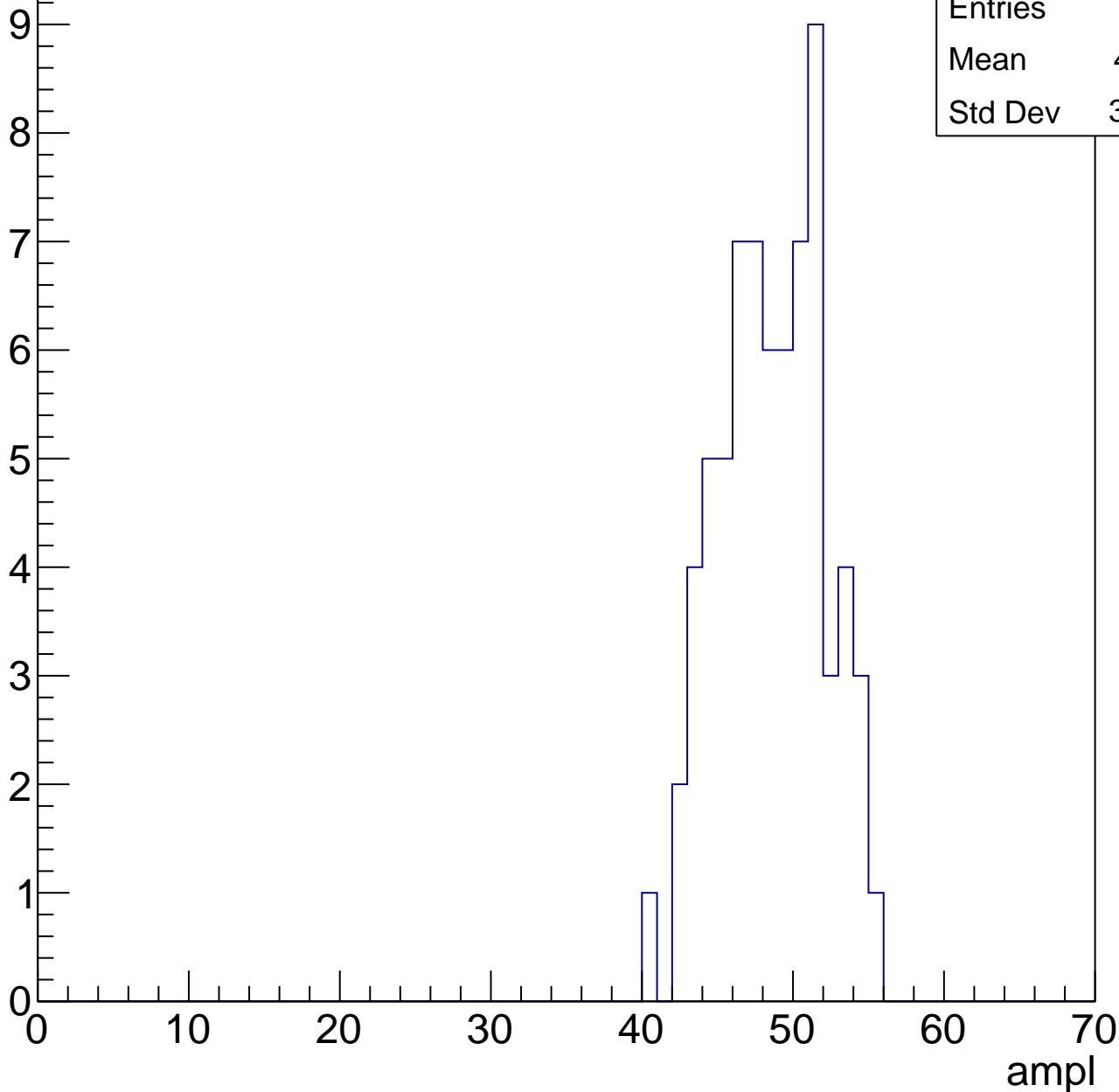


# B1L003S, U18-ch88, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

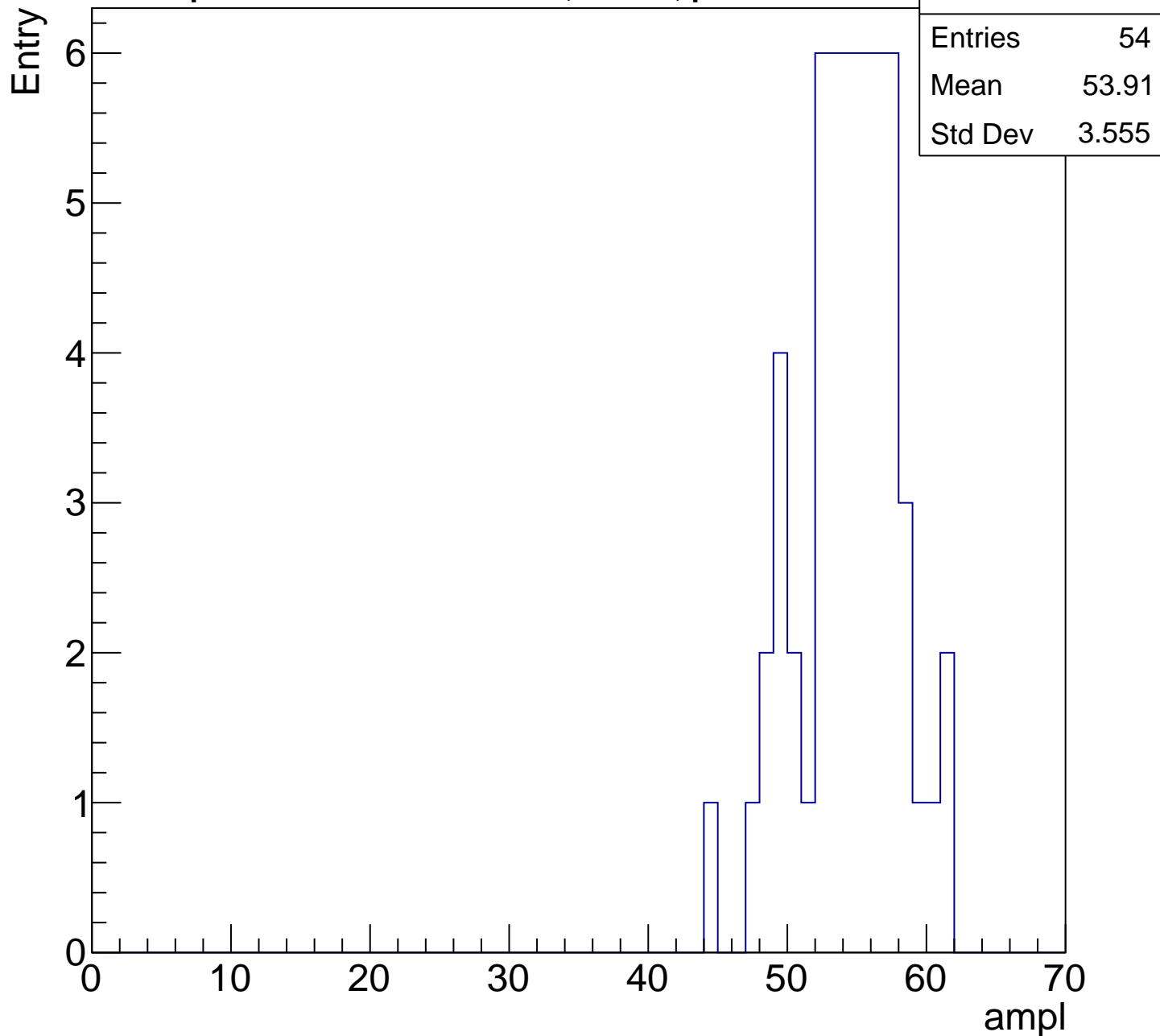
Entry

Entries	70
Mean	48.11
Std Dev	3.412



# B1L003S, U18-ch88, adc4

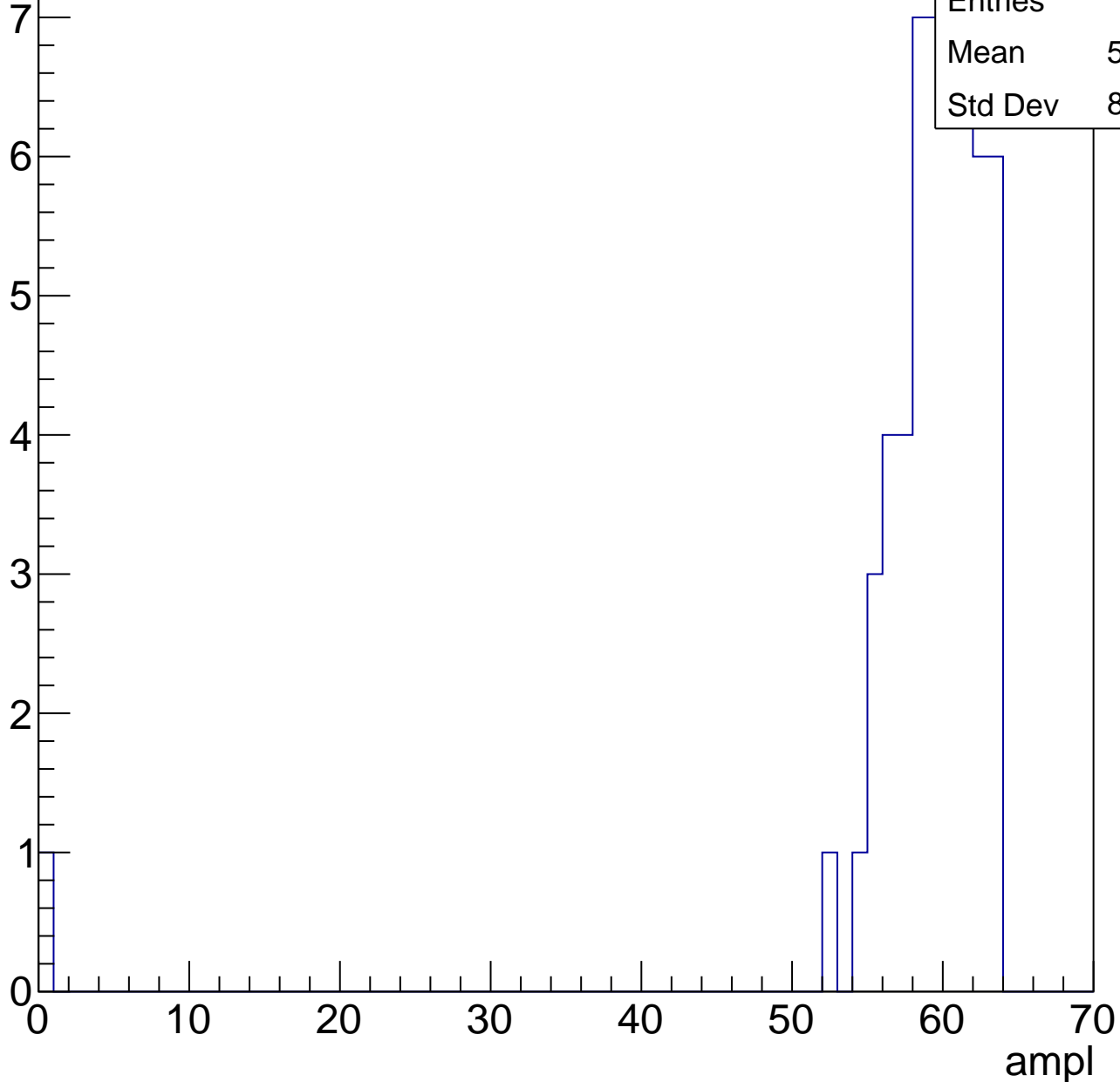
calib\_packv5\_042523\_0143.root, FC#13, port D2



# B1L003S, U18-ch88, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

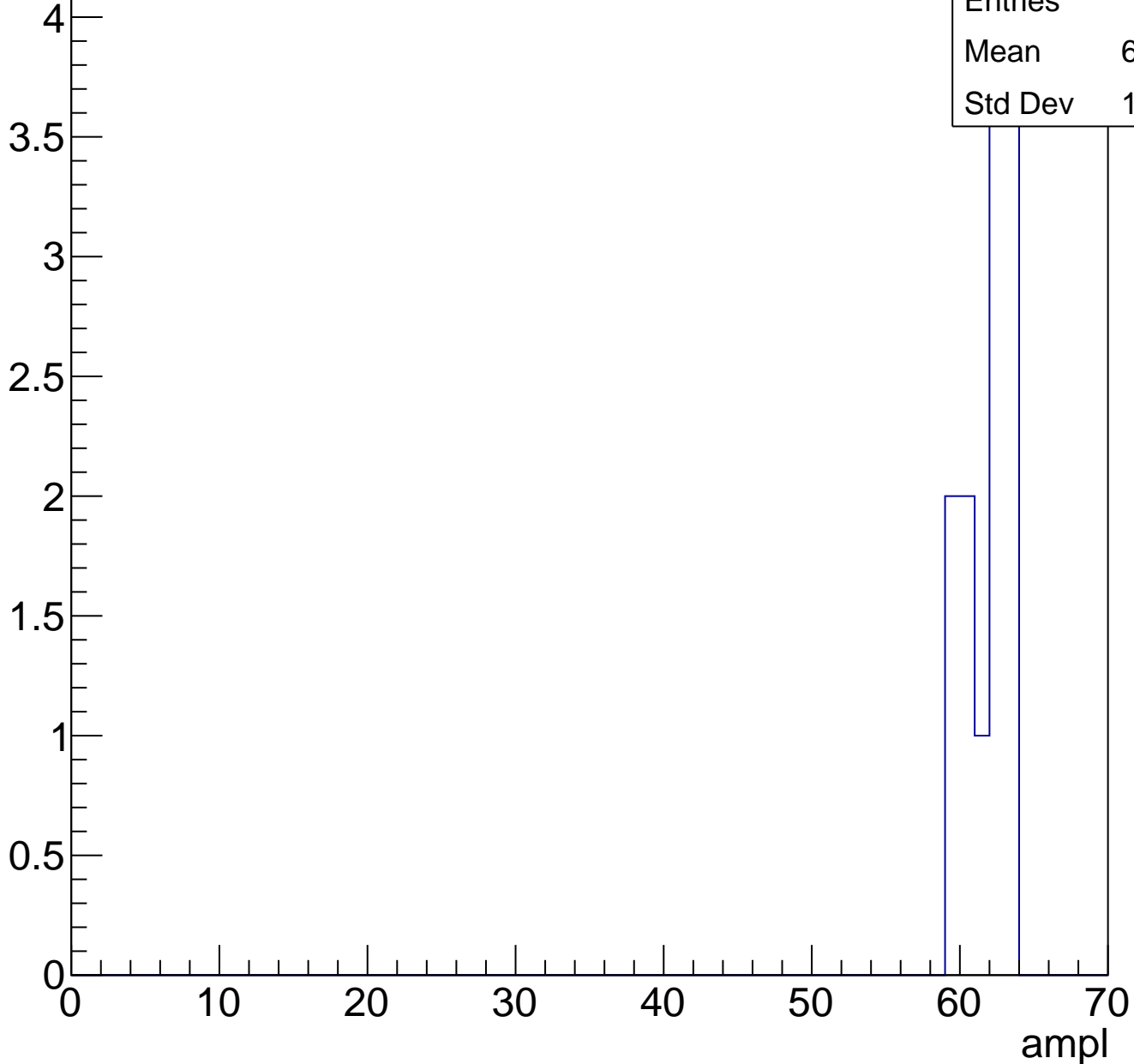
Entry



# B1L003S, U18-ch88, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U18-ch88, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L003S, U18-ch89, adc0

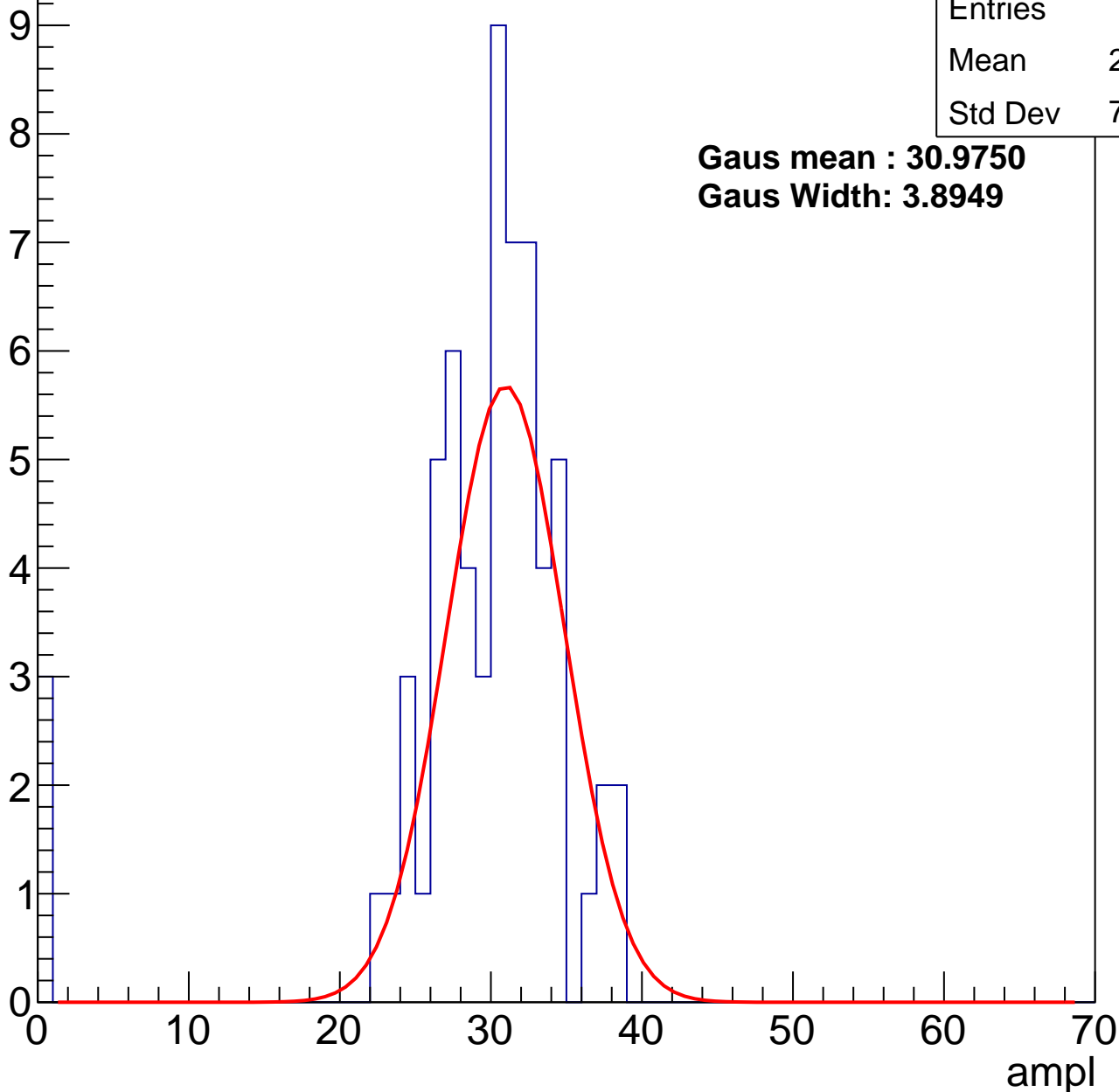
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	64
Mean	28.62
Std Dev	7.279

**Gaus mean : 30.9750**

**Gaus Width: 3.8949**

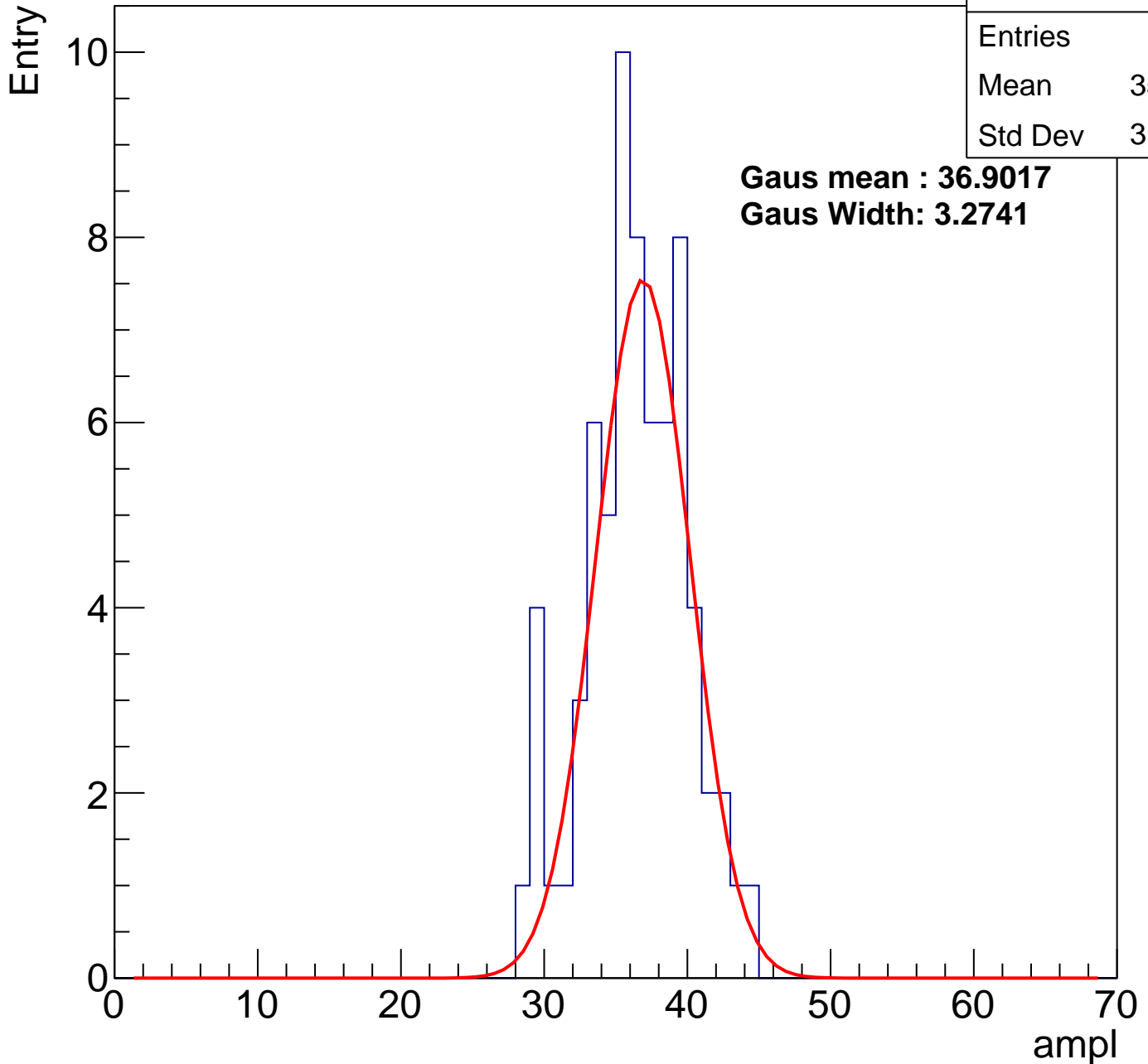


# B1L003S, U18-ch89, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	69
Mean	35.97
Std Dev	3.518

**Gaus mean : 36.9017**  
**Gaus Width: 3.2741**



# B1L003S, U18-ch89, adc2

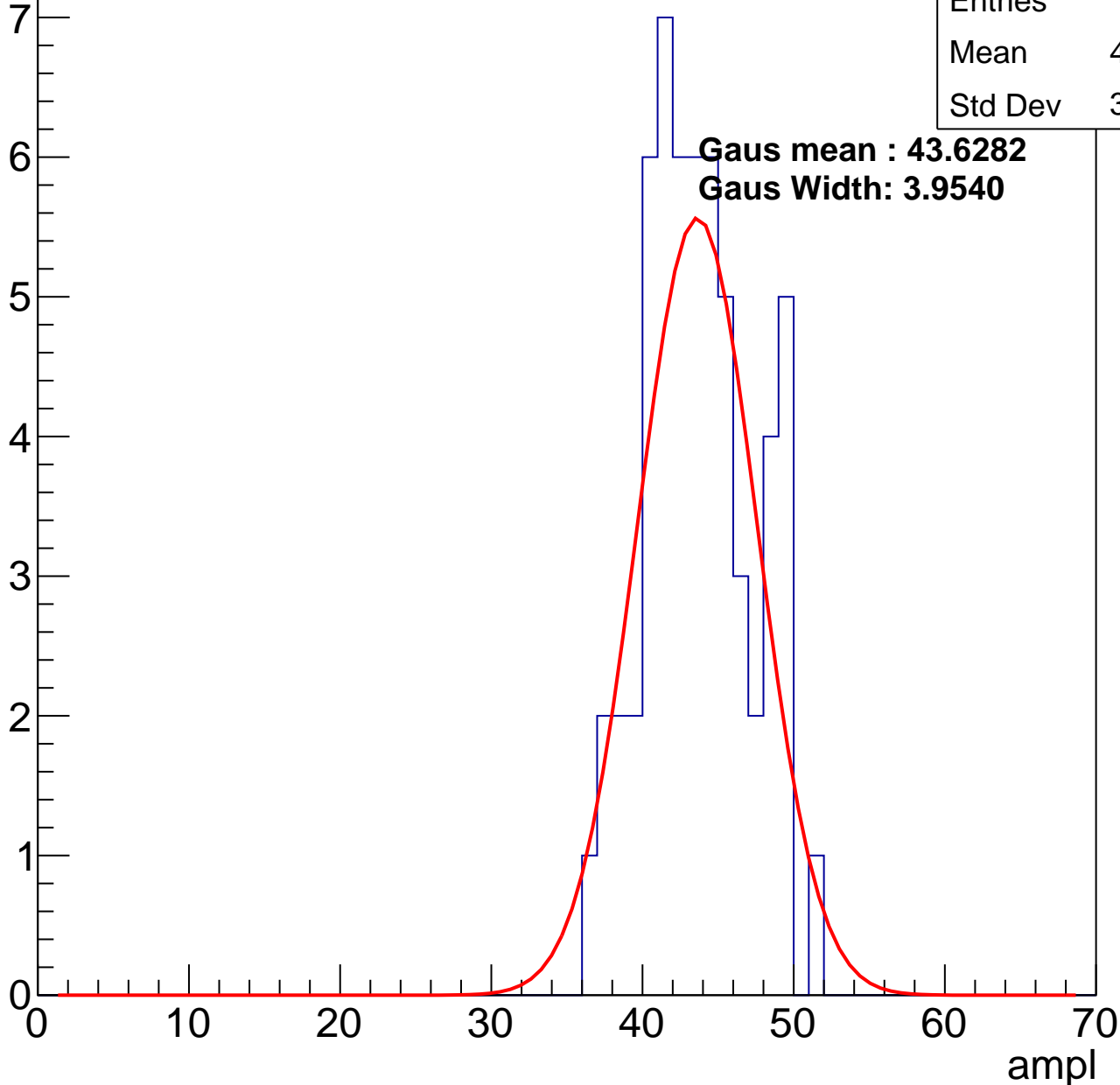
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	58
Mean	43.28
Std Dev	3.513

**Gaus mean : 43.6282**

**Gaus Width: 3.9540**

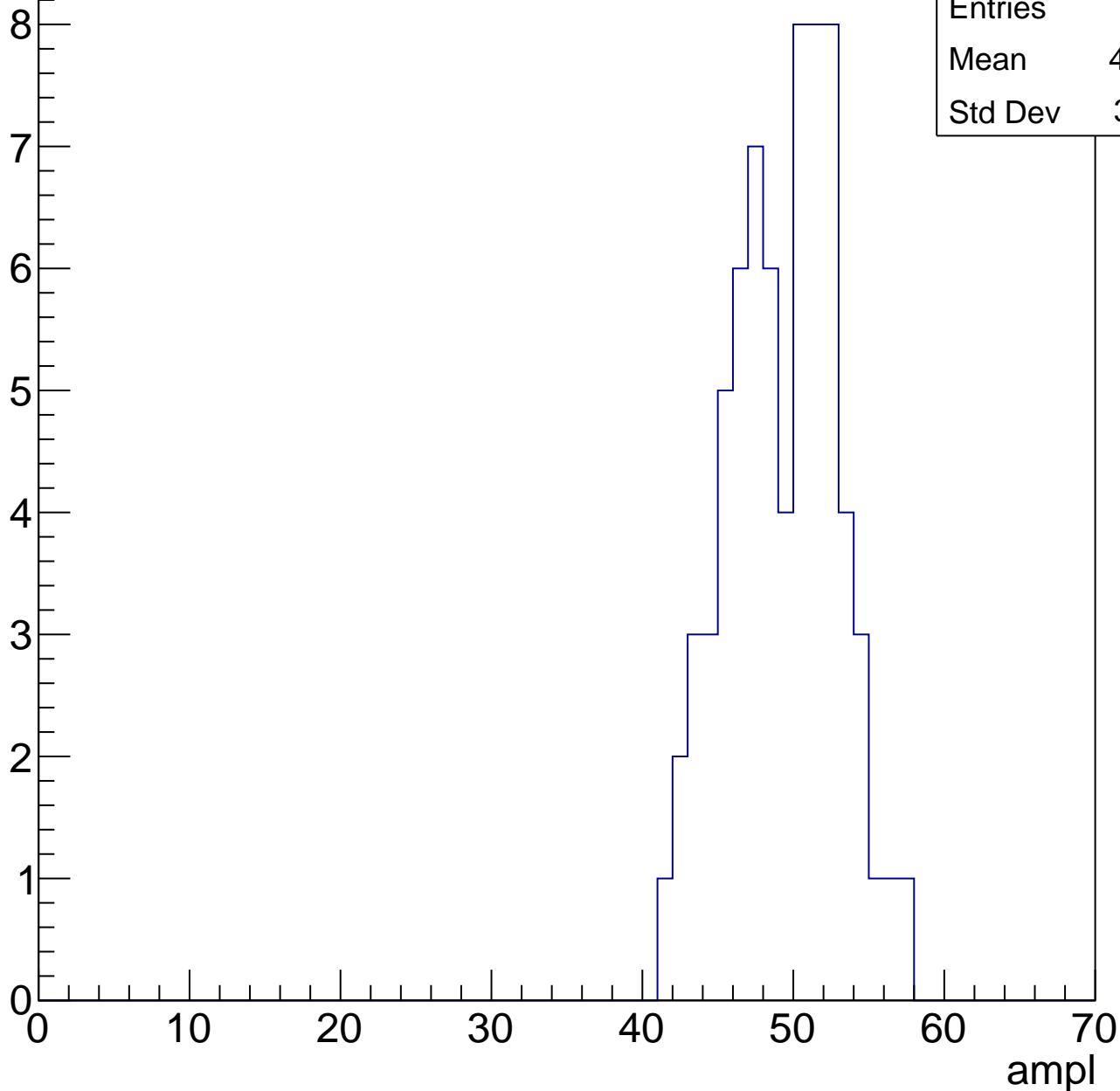


# B1L003S, U18-ch89, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	71
Mean	48.82
Std Dev	3.581

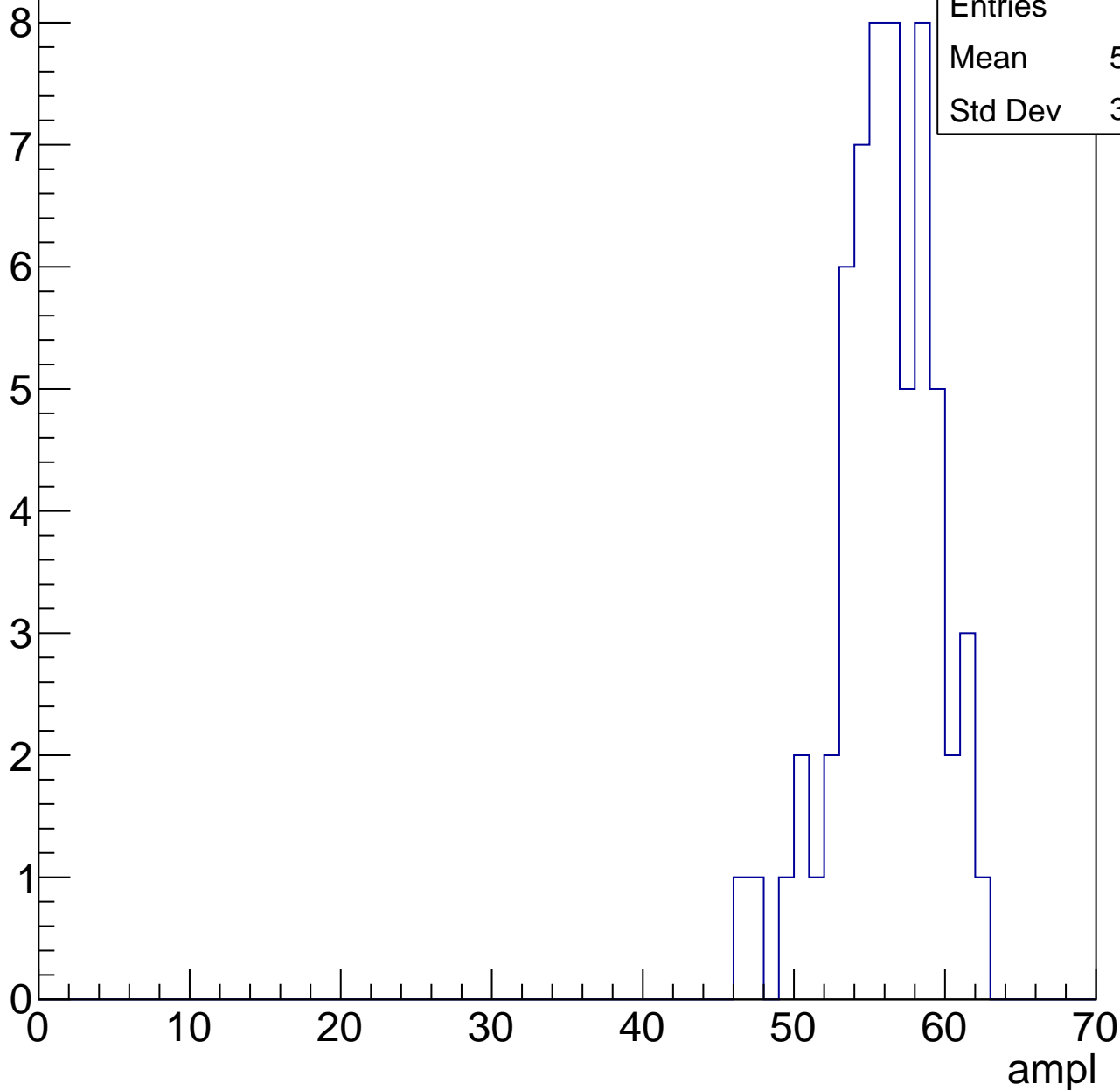


# B1L003S, U18-ch89, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

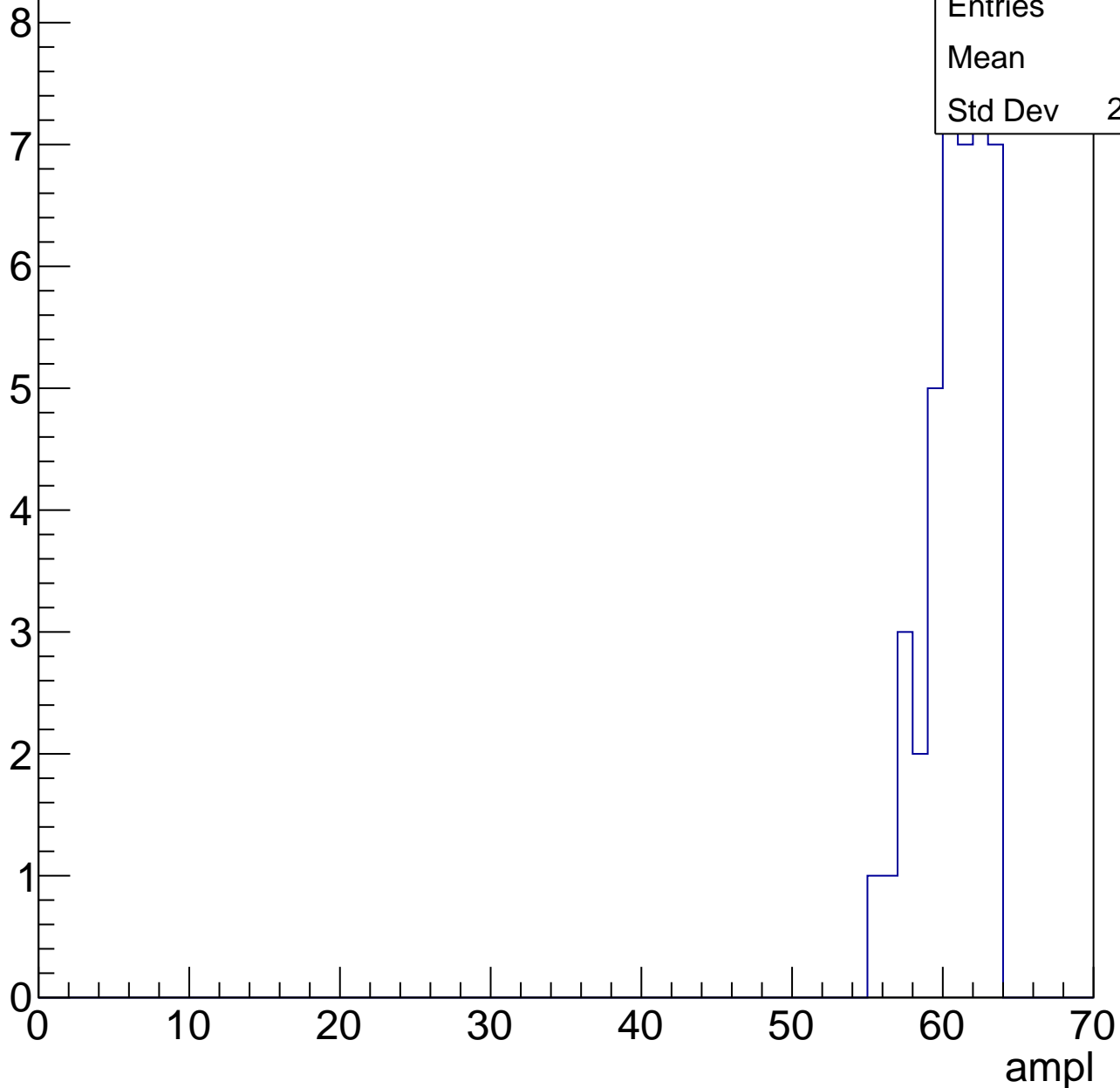
Entries	61
Mean	55.57
Std Dev	3.297



# B1L003S, U18-ch89, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

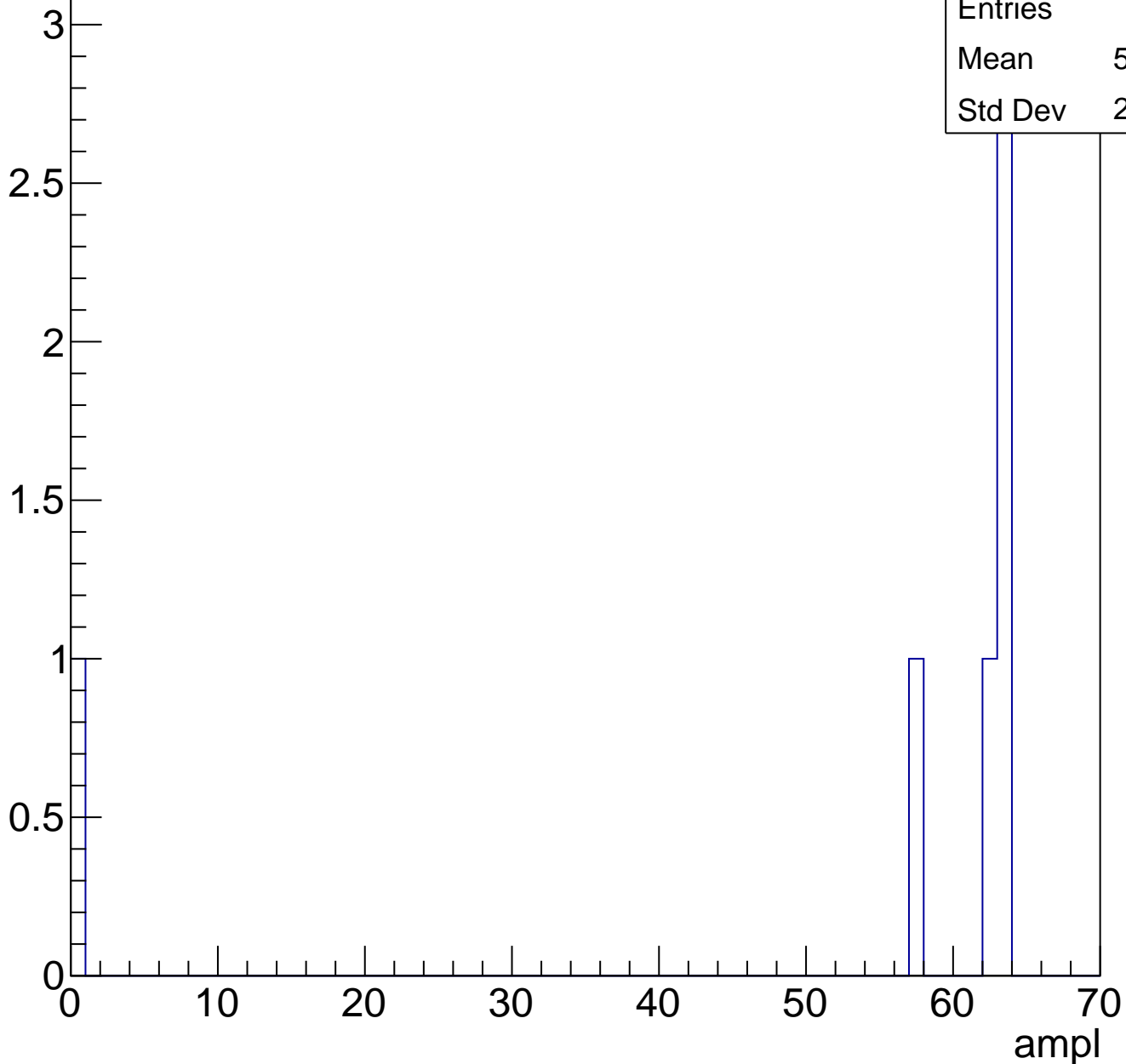


Entries	42
Mean	60.4
Std Dev	2.048

# B1L003S, U18-ch89, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U18-ch89, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch90, adc0

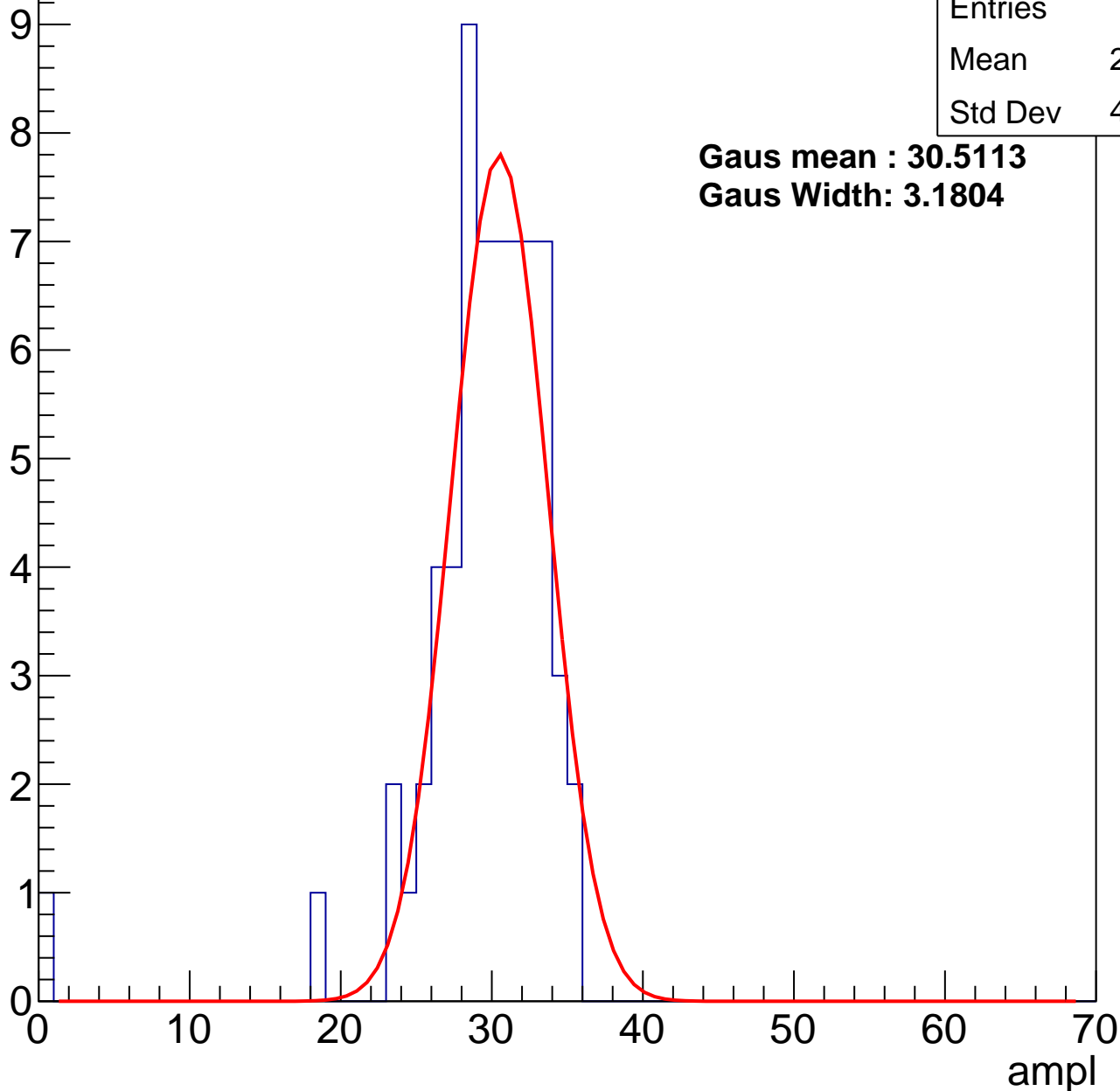
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	64
Mean	29.05
Std Dev	4.856

**Gaus mean : 30.5113**

**Gaus Width: 3.1804**



# B1L003S, U18-ch90, adc1

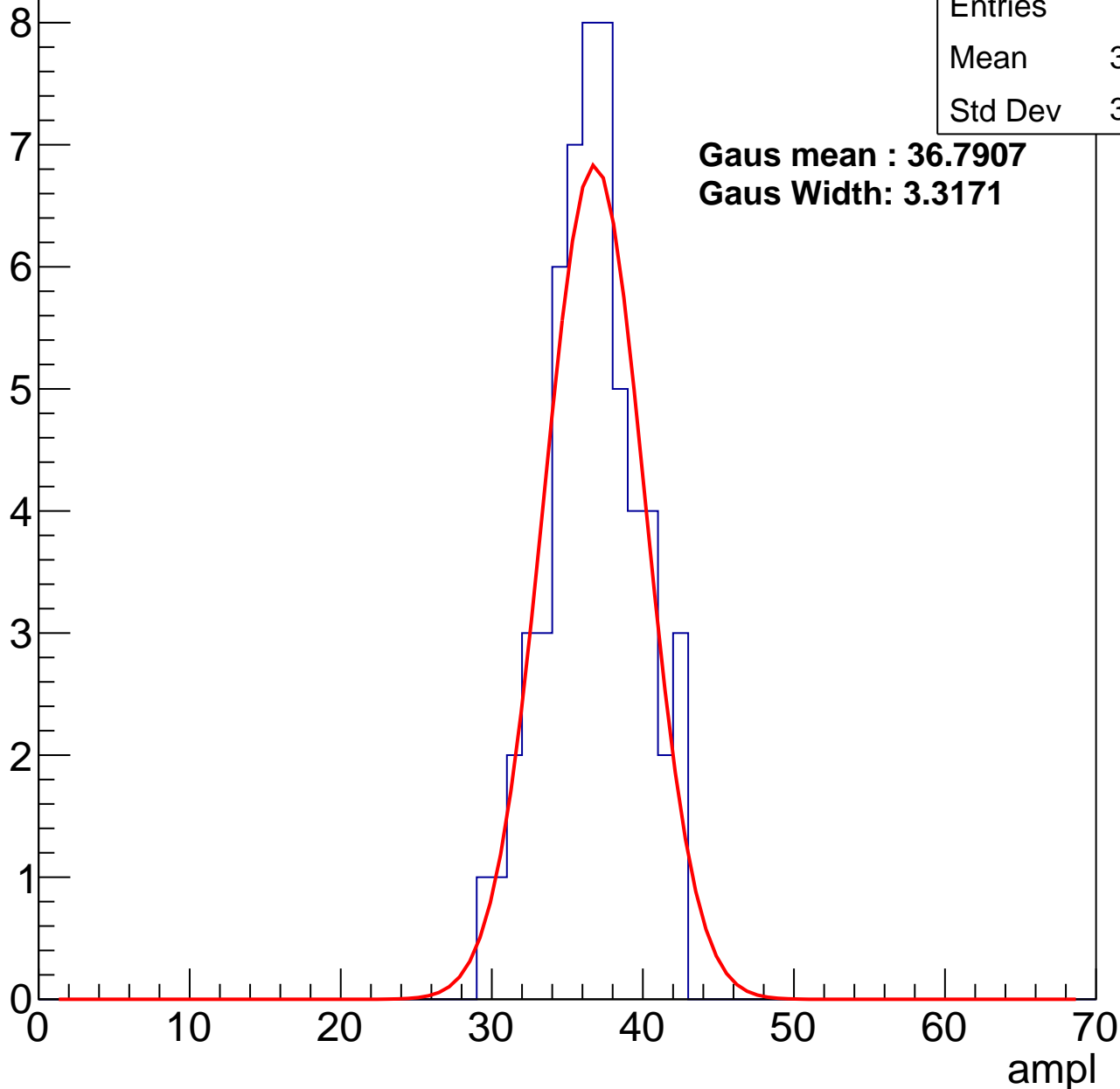
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	57
Mean	36.19
Std Dev	3.035

**Gaus mean : 36.7907**

**Gaus Width: 3.3171**



# B1L003S, U18-ch90, adc2

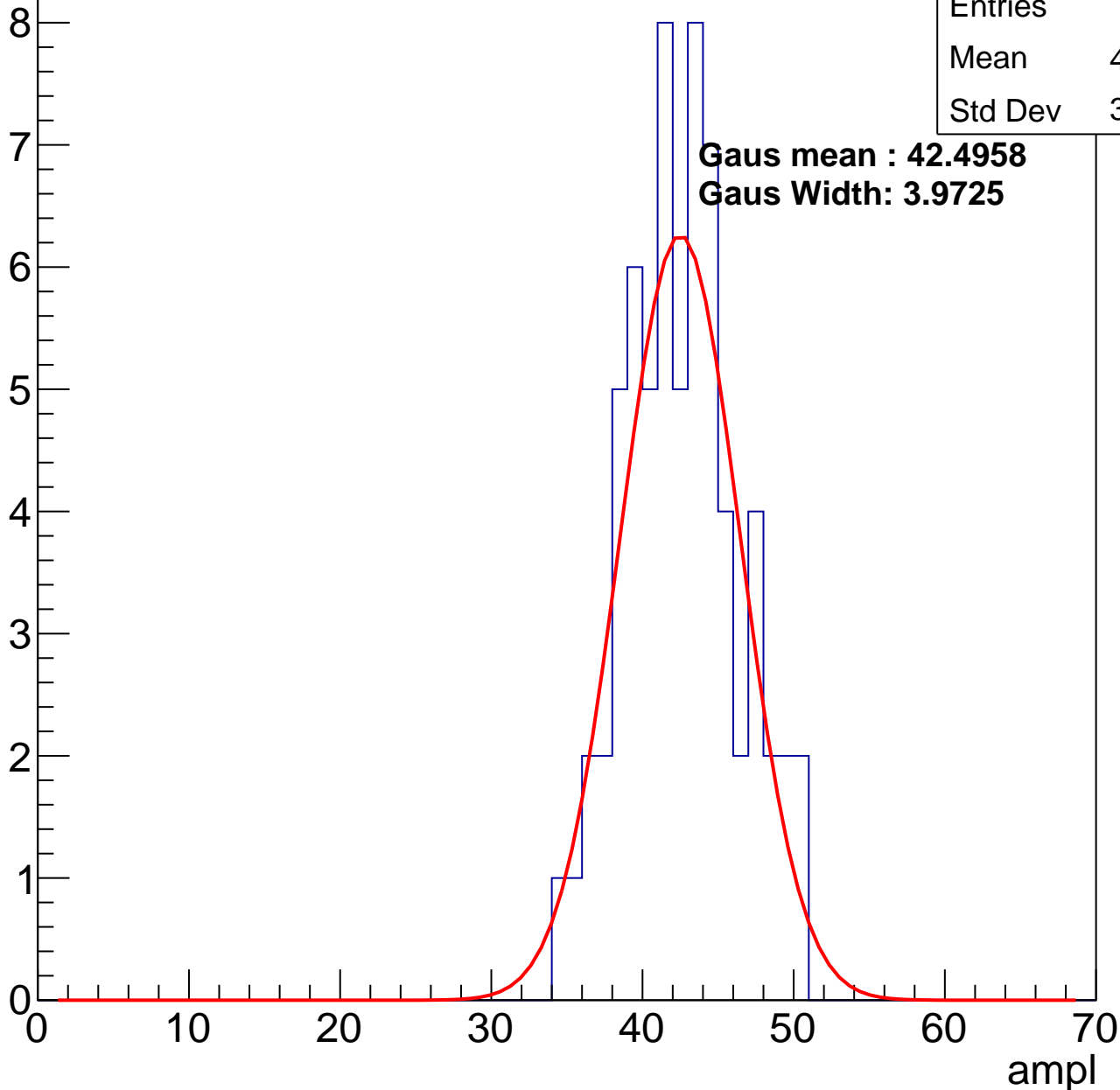
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	66
Mean	42.17
Std Dev	3.687

**Gaus mean : 42.4958**

**Gaus Width: 3.9725**

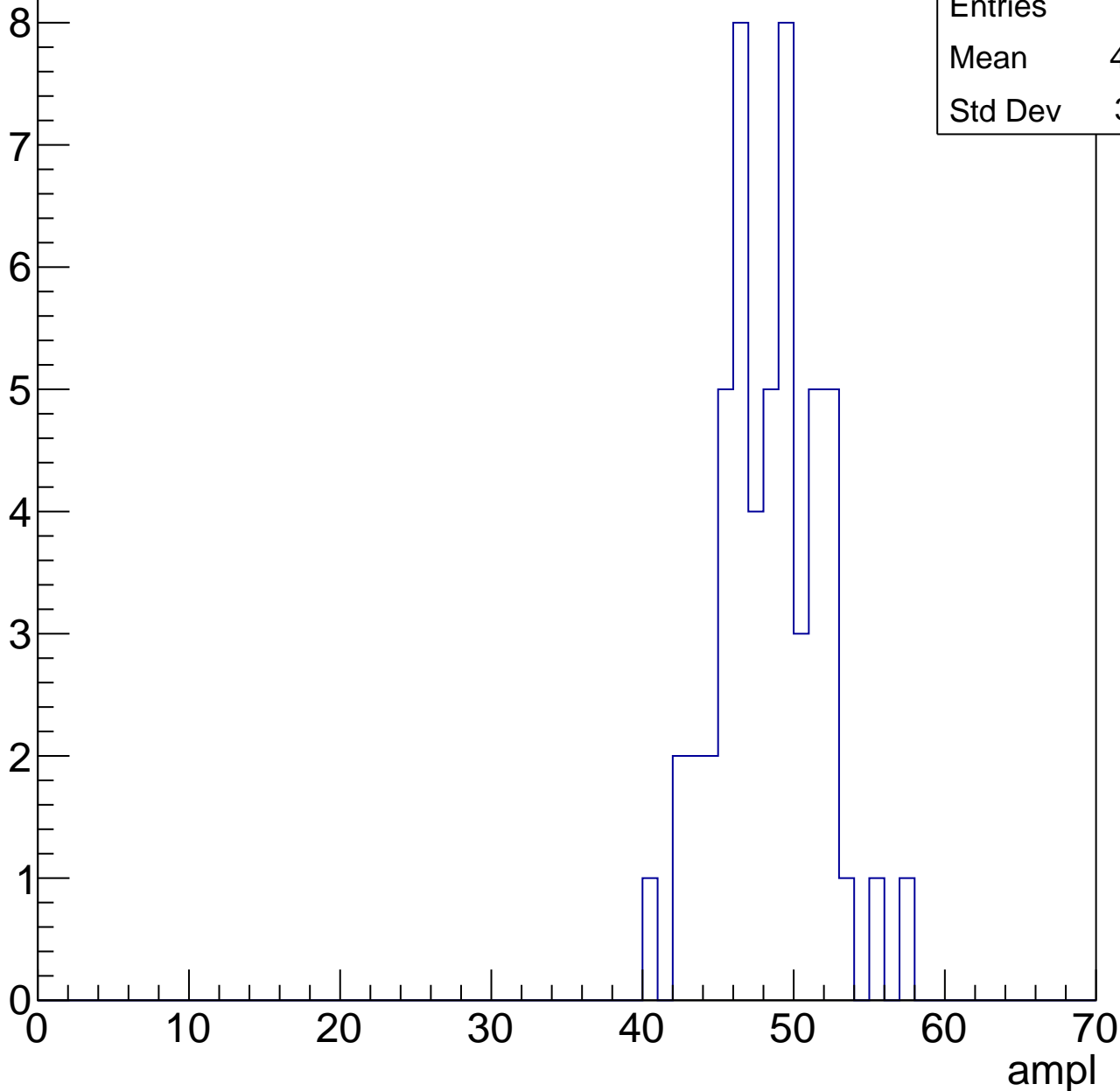


# B1L003S, U18-ch90, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	53
Mean	47.94
Std Dev	3.361

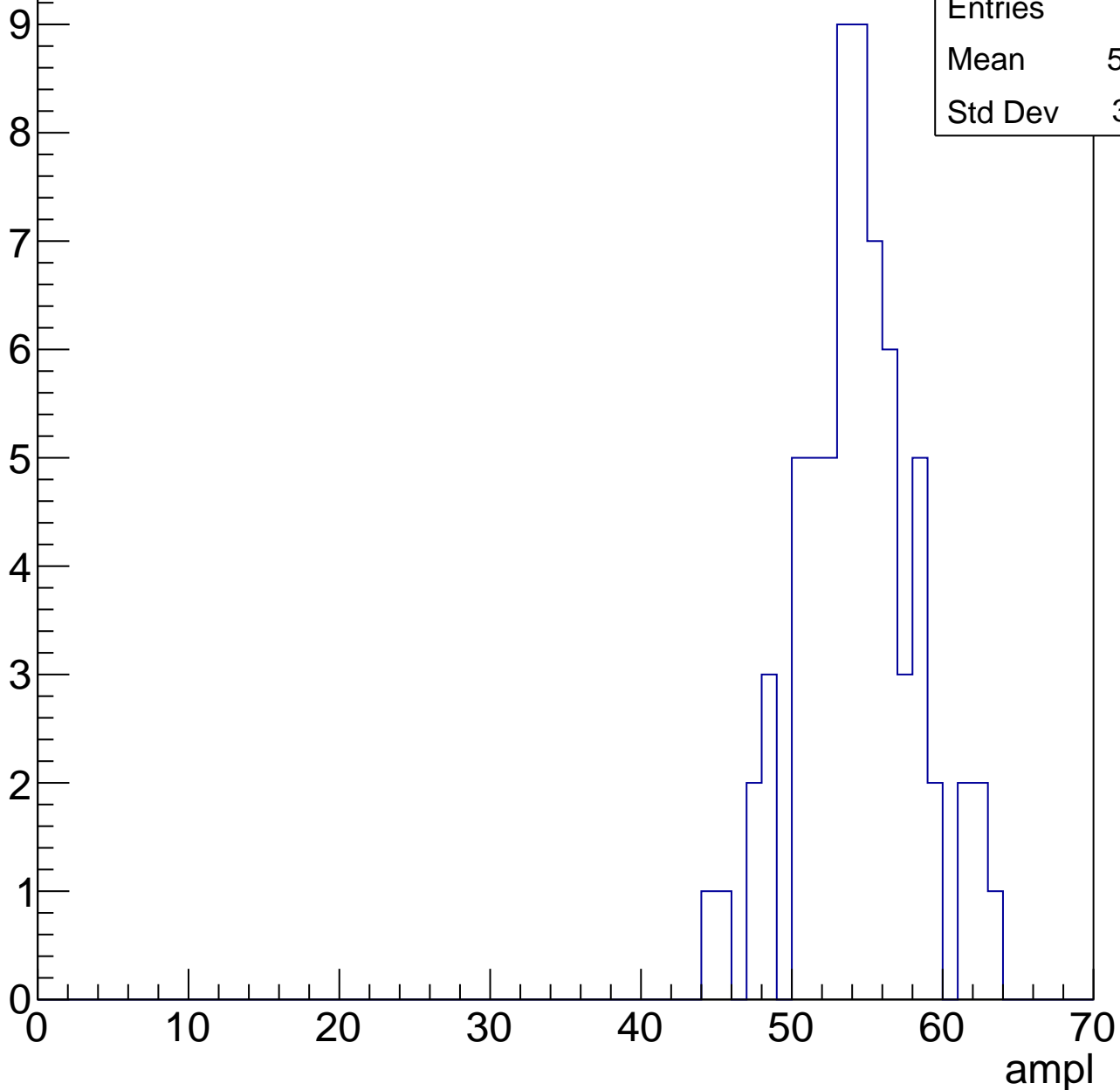


# B1L003S, U18-ch90, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	68
Mean	53.88
Std Dev	3.901

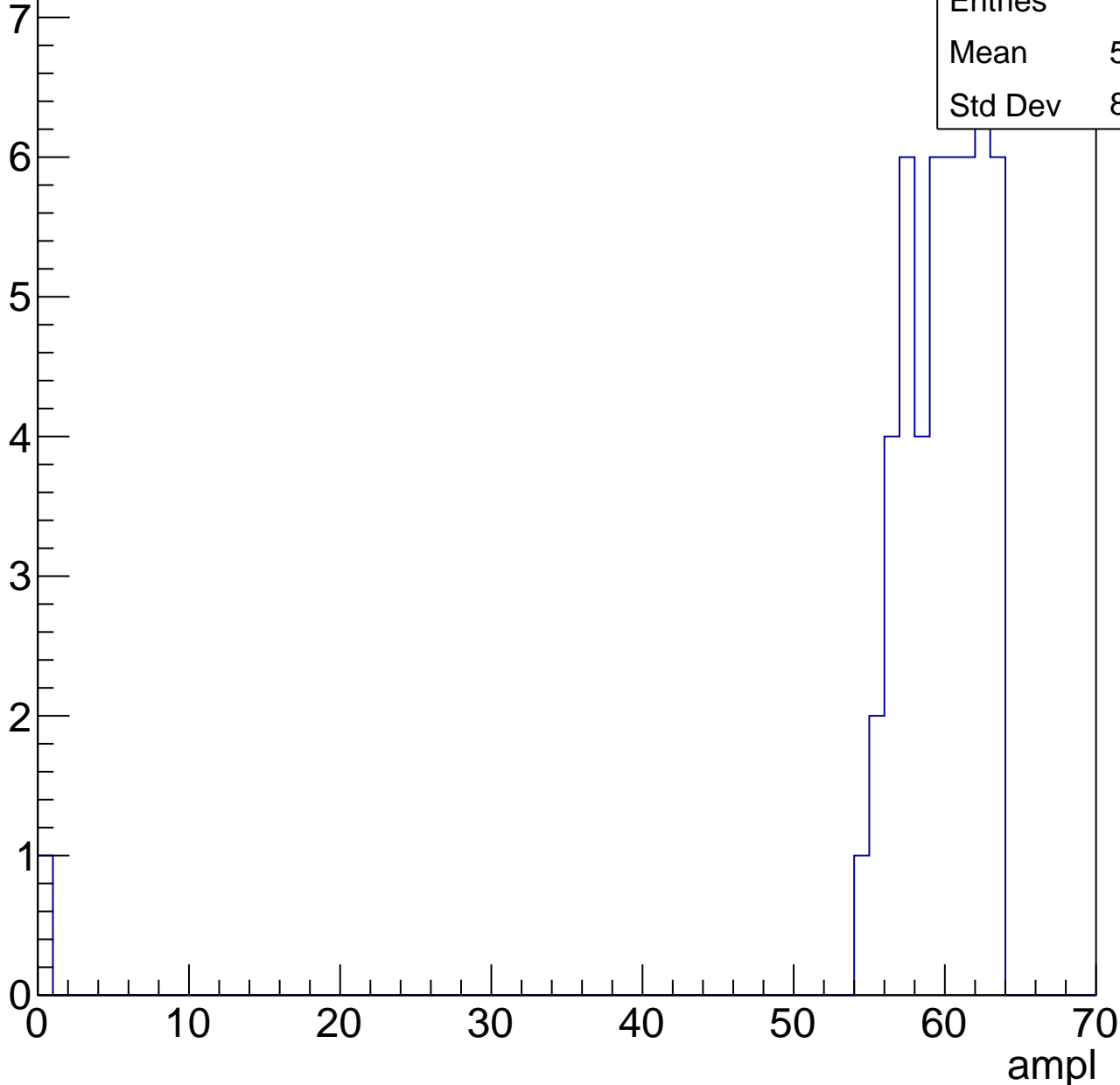


# B1L003S, U18-ch90, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

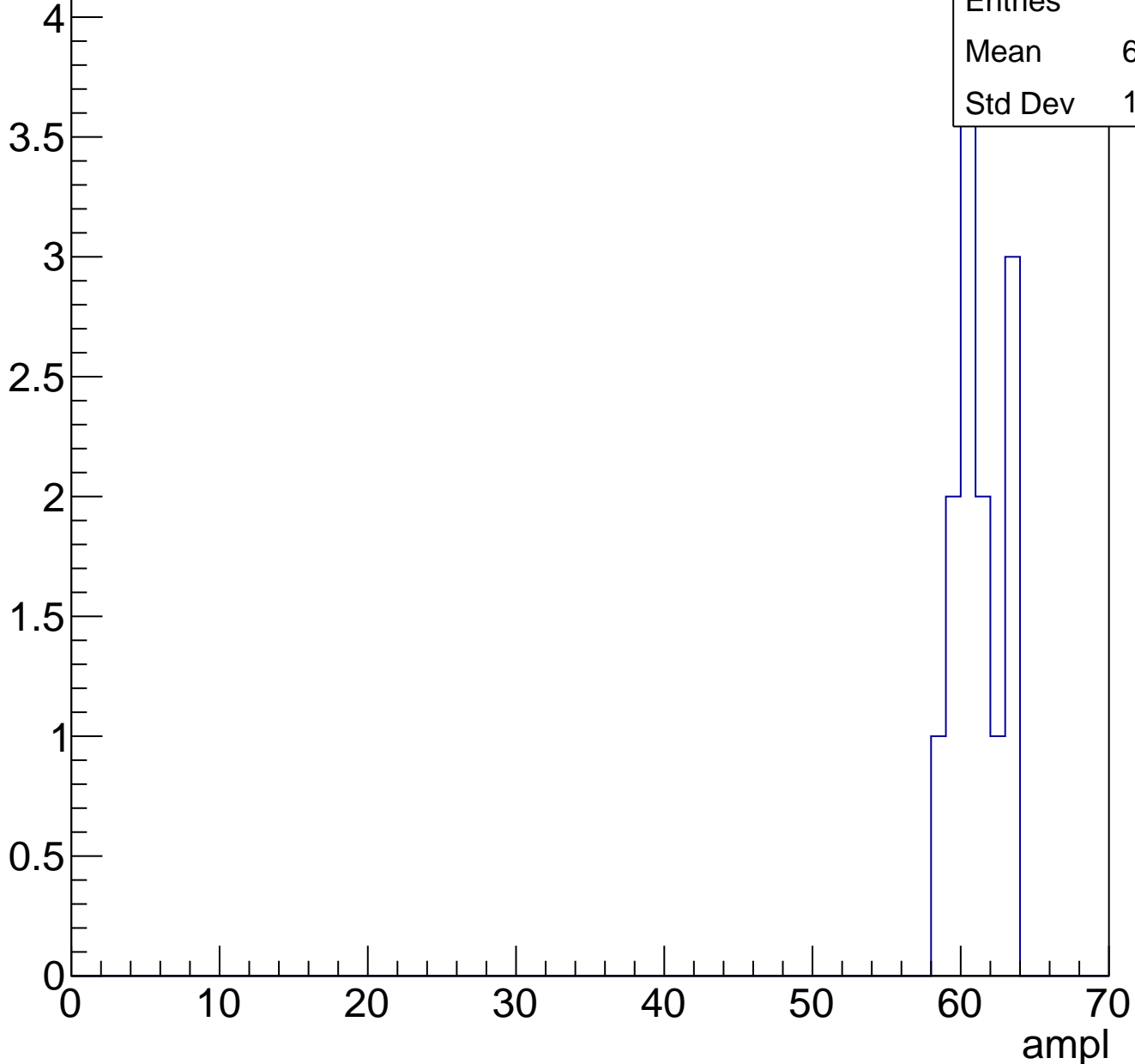
Entries	49
Mean	58.24
Std Dev	8.763



# B1L003S, U18-ch90, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	13
Mean	60.69
Std Dev	1.588



# B1L003S, U18-ch90, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U18-ch91, adc0

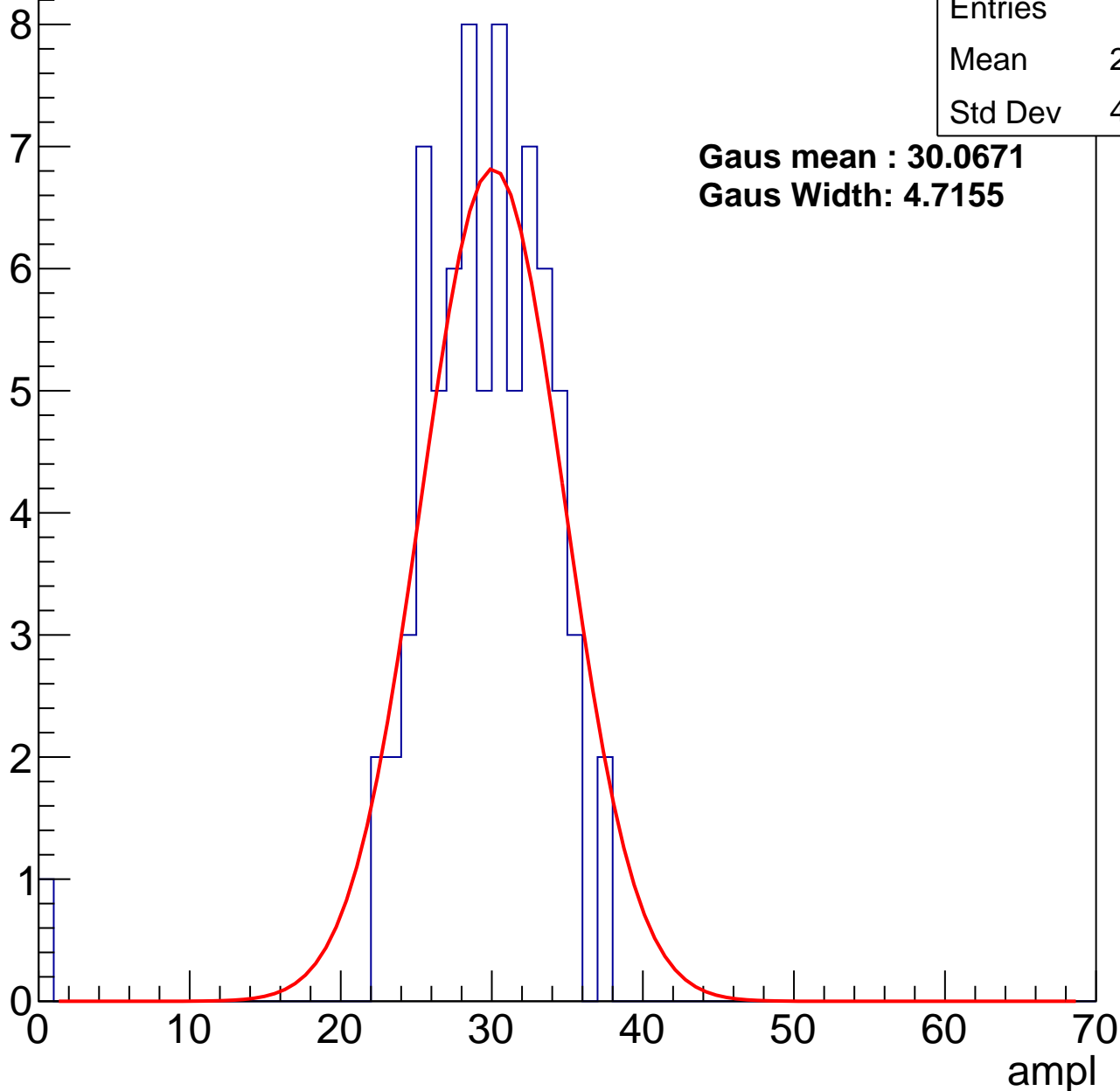
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	75
Mean	28.85
Std Dev	4.928

**Gaus mean : 30.0671**

**Gaus Width: 4.7155**



# B1L003S, U18-ch91, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	75
Mean	36.31
Std Dev	3.812

**Gaus mean : 37.6913**

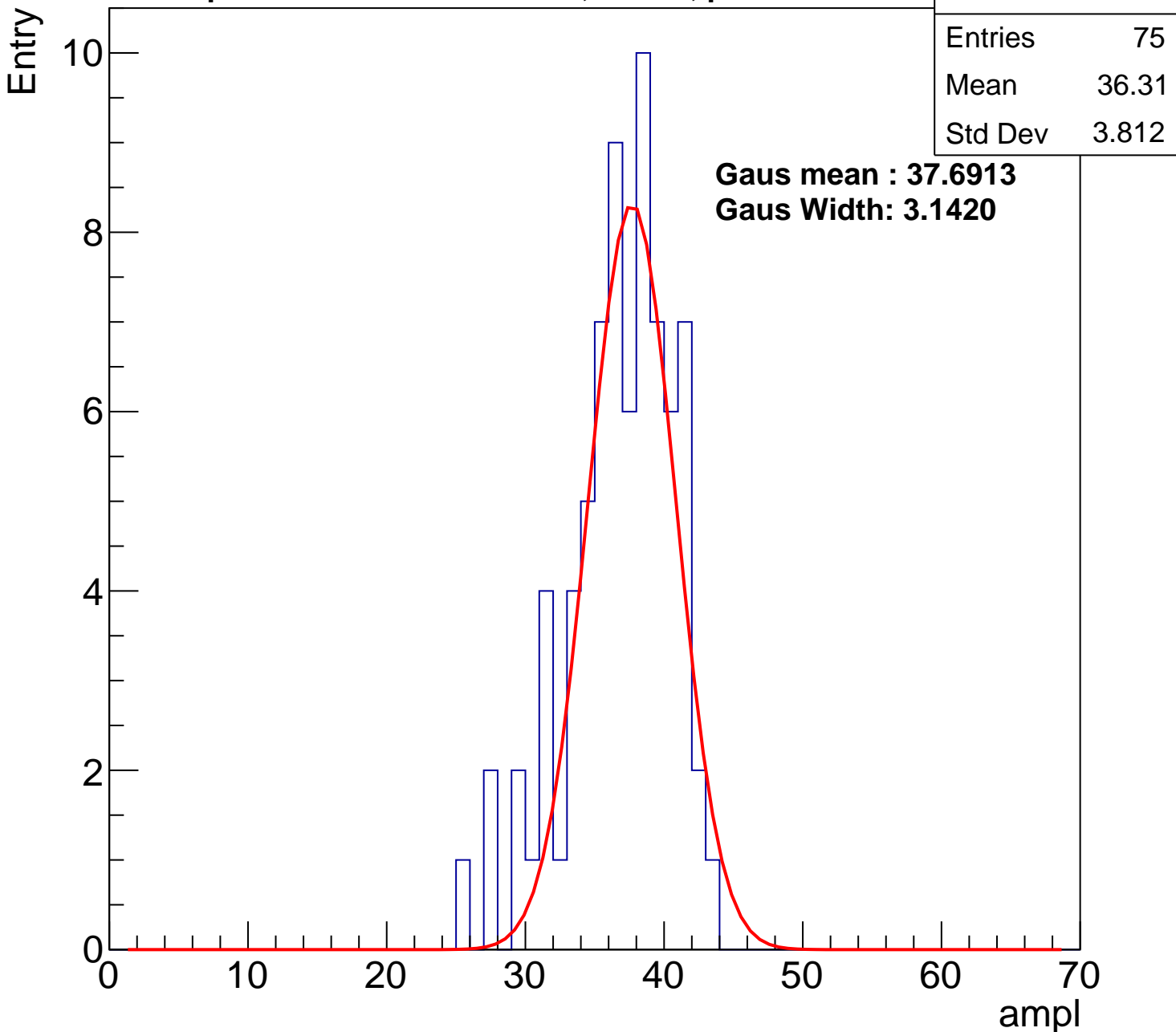
**Gaus Width: 3.1420**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L003S, U18-ch91, adc2

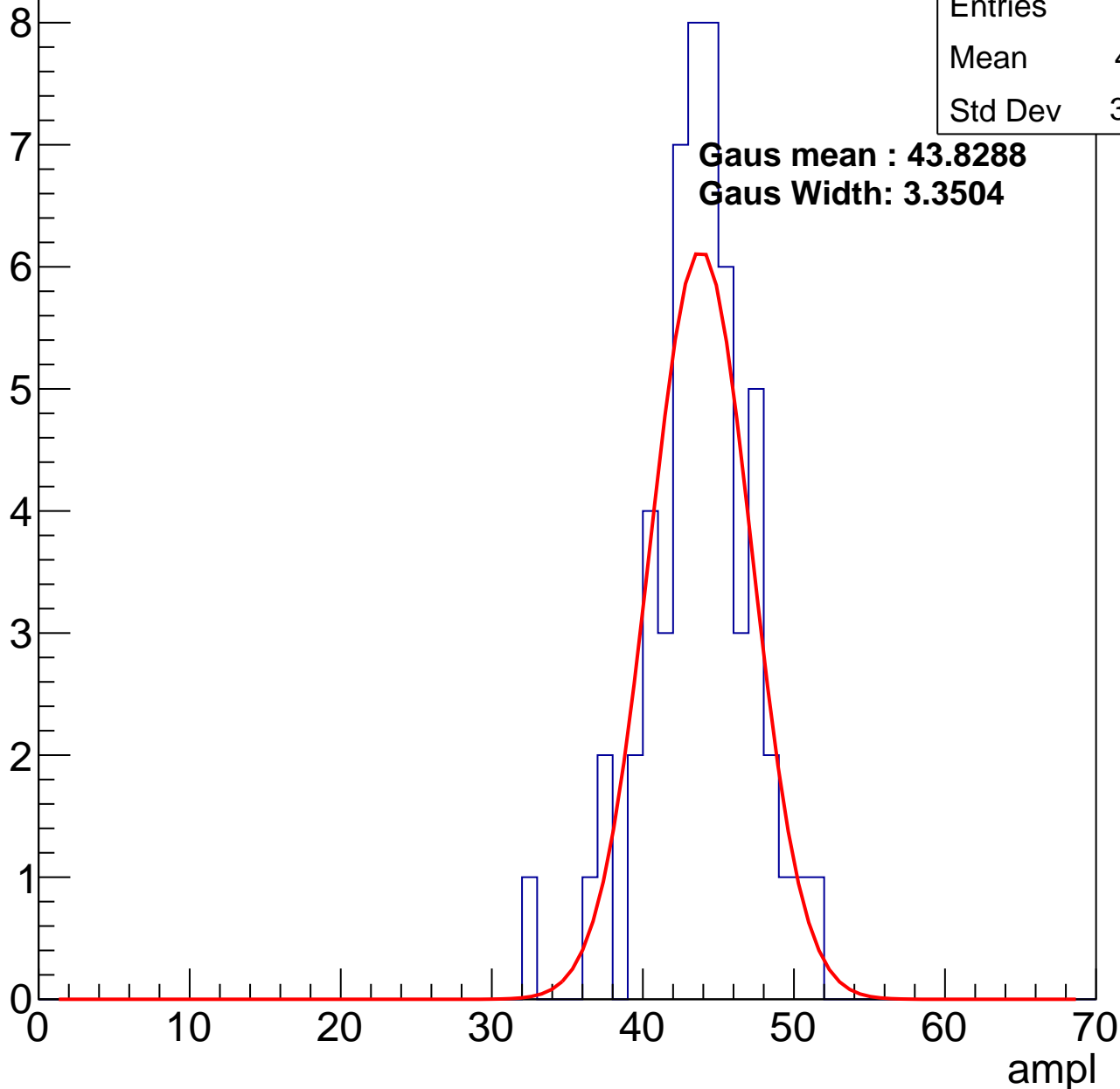
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	55
Mean	43.31
Std Dev	3.469

**Gaus mean : 43.8288**

**Gaus Width: 3.3504**

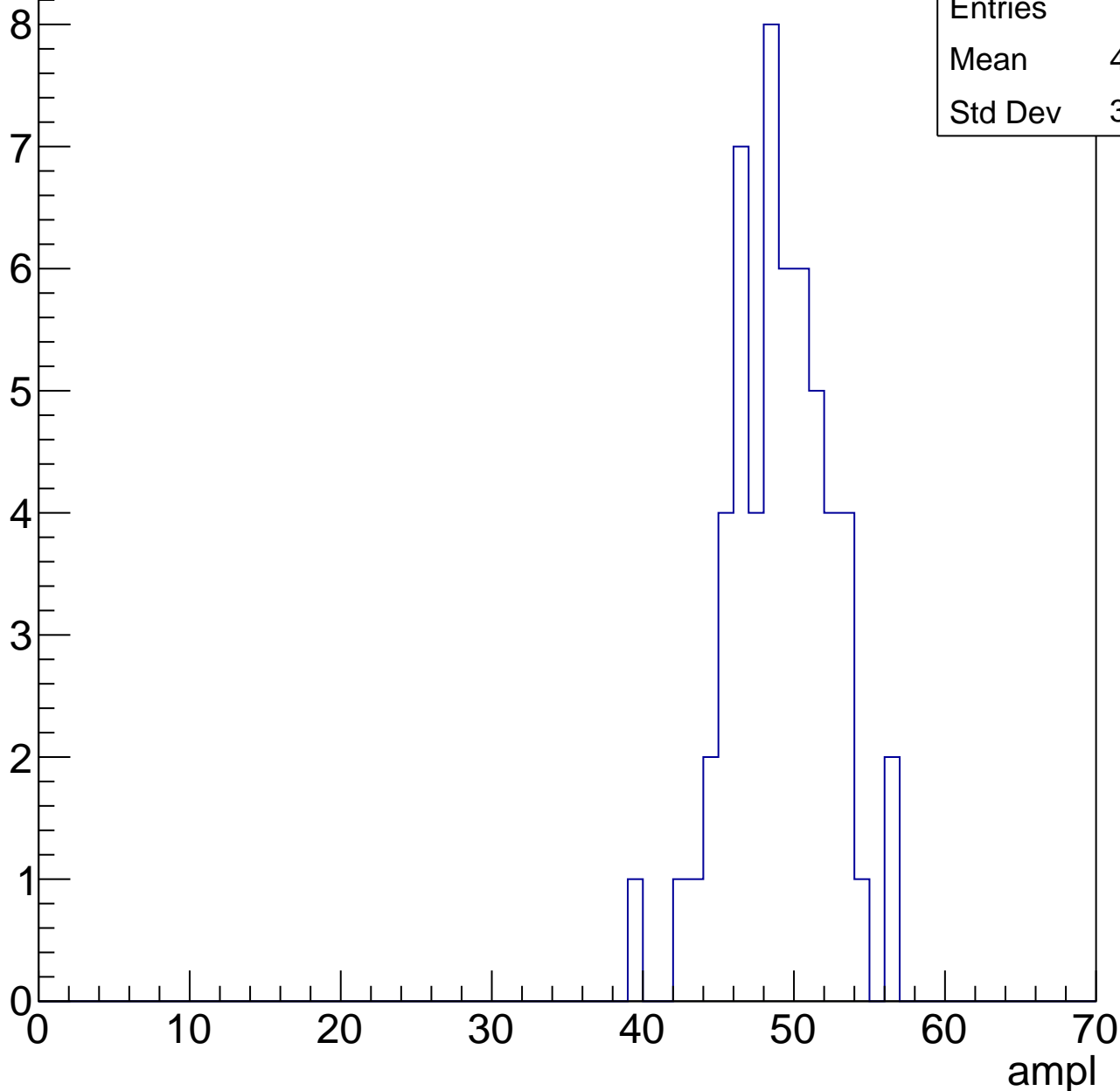


# B1L003S, U18-ch91, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	56
Mean	48.59
Std Dev	3.342

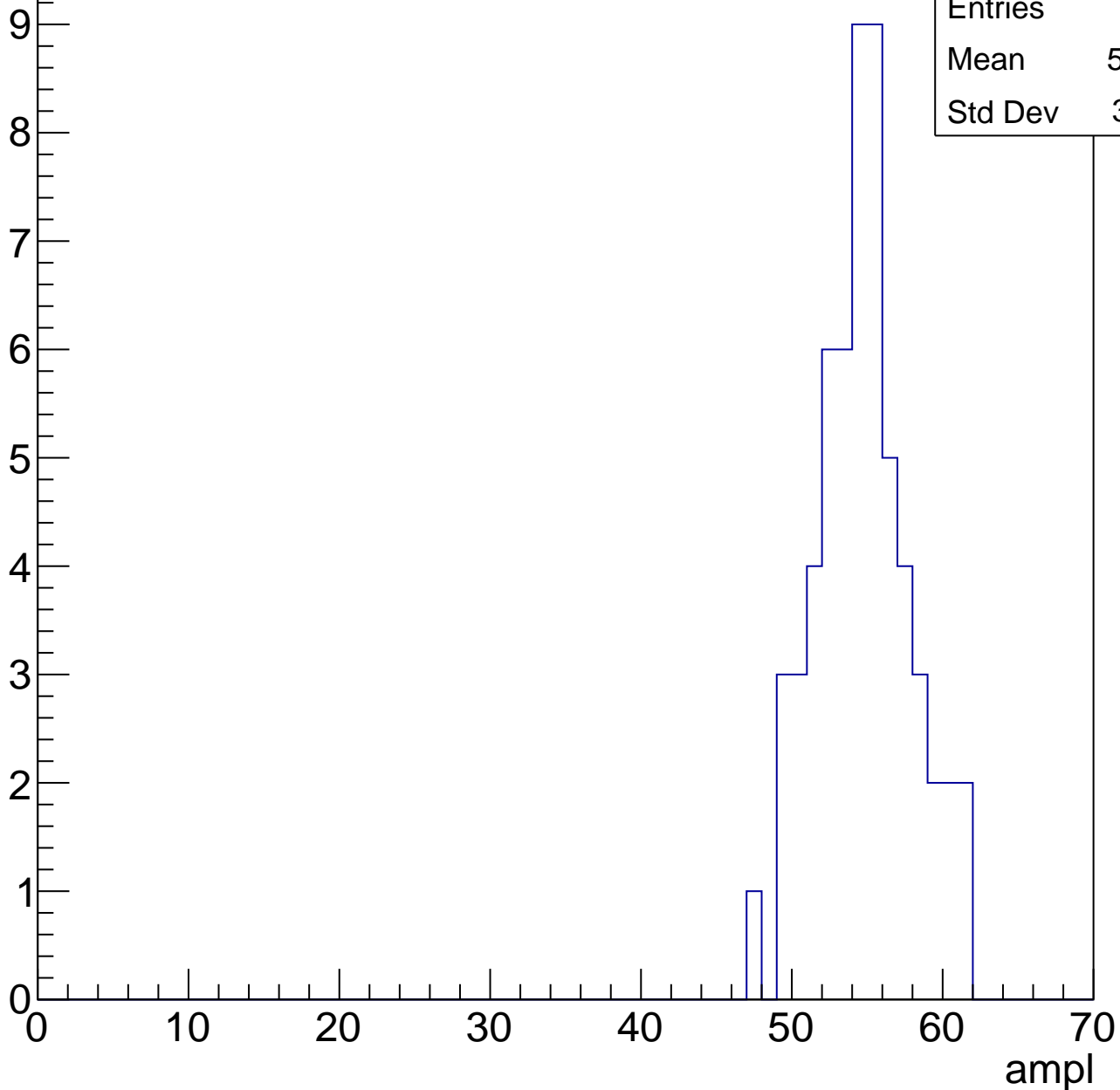


# B1L003S, U18-ch91, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

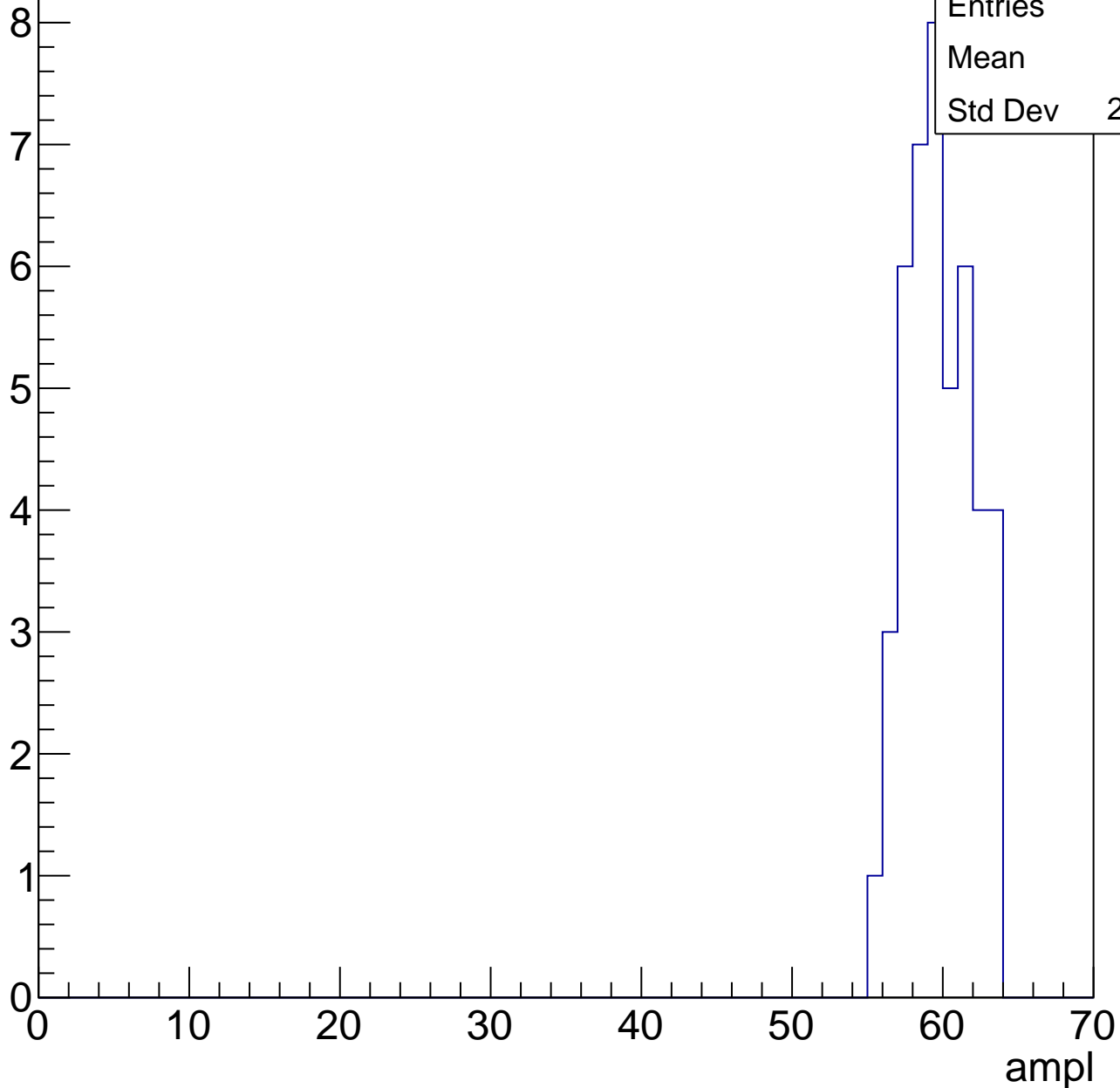
Entries	59
Mean	54.25
Std Dev	3.101



# B1L003S, U18-ch91, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

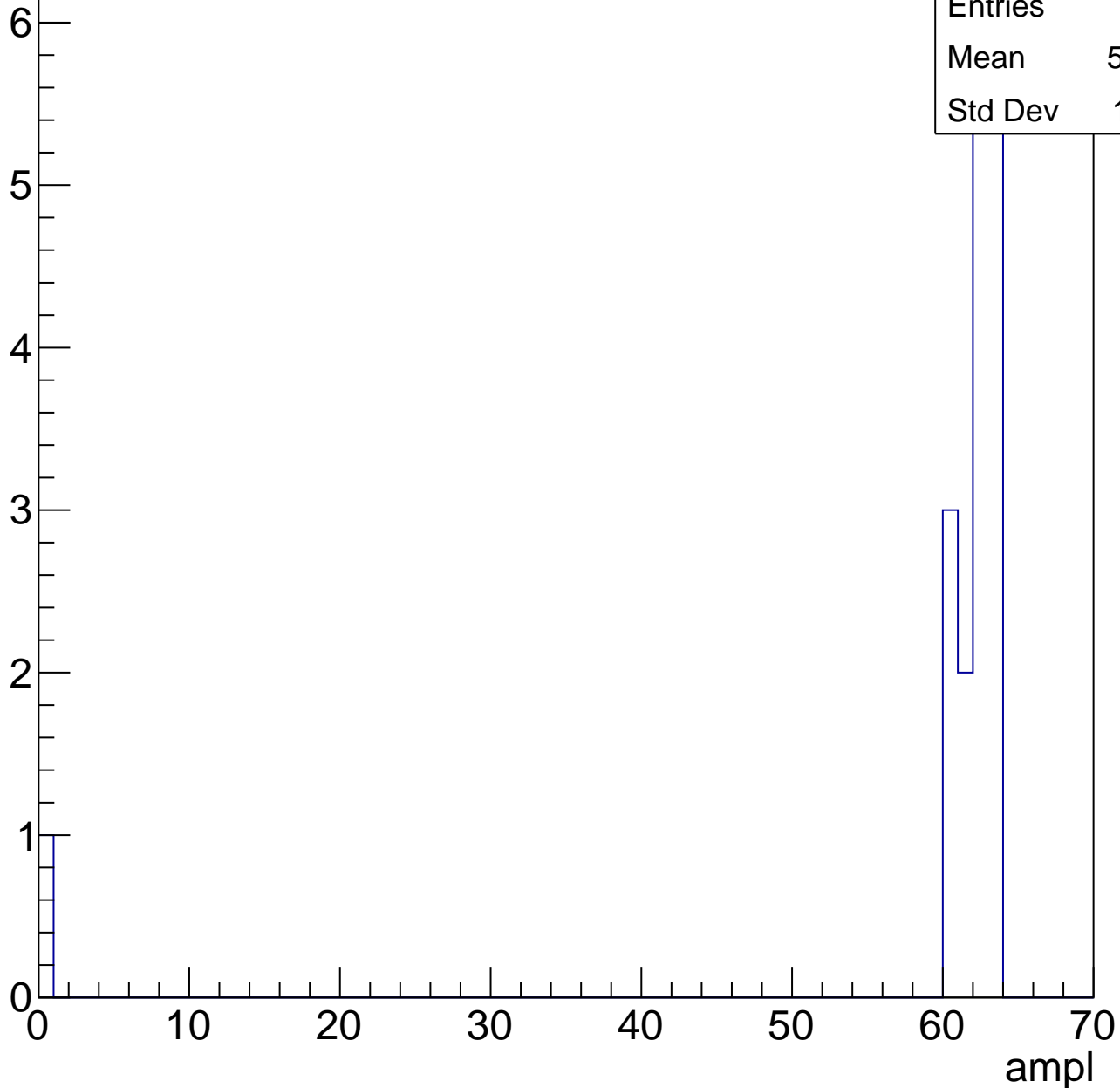
Entry



# B1L003S, U18-ch91, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U18-ch91, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch92, adc0

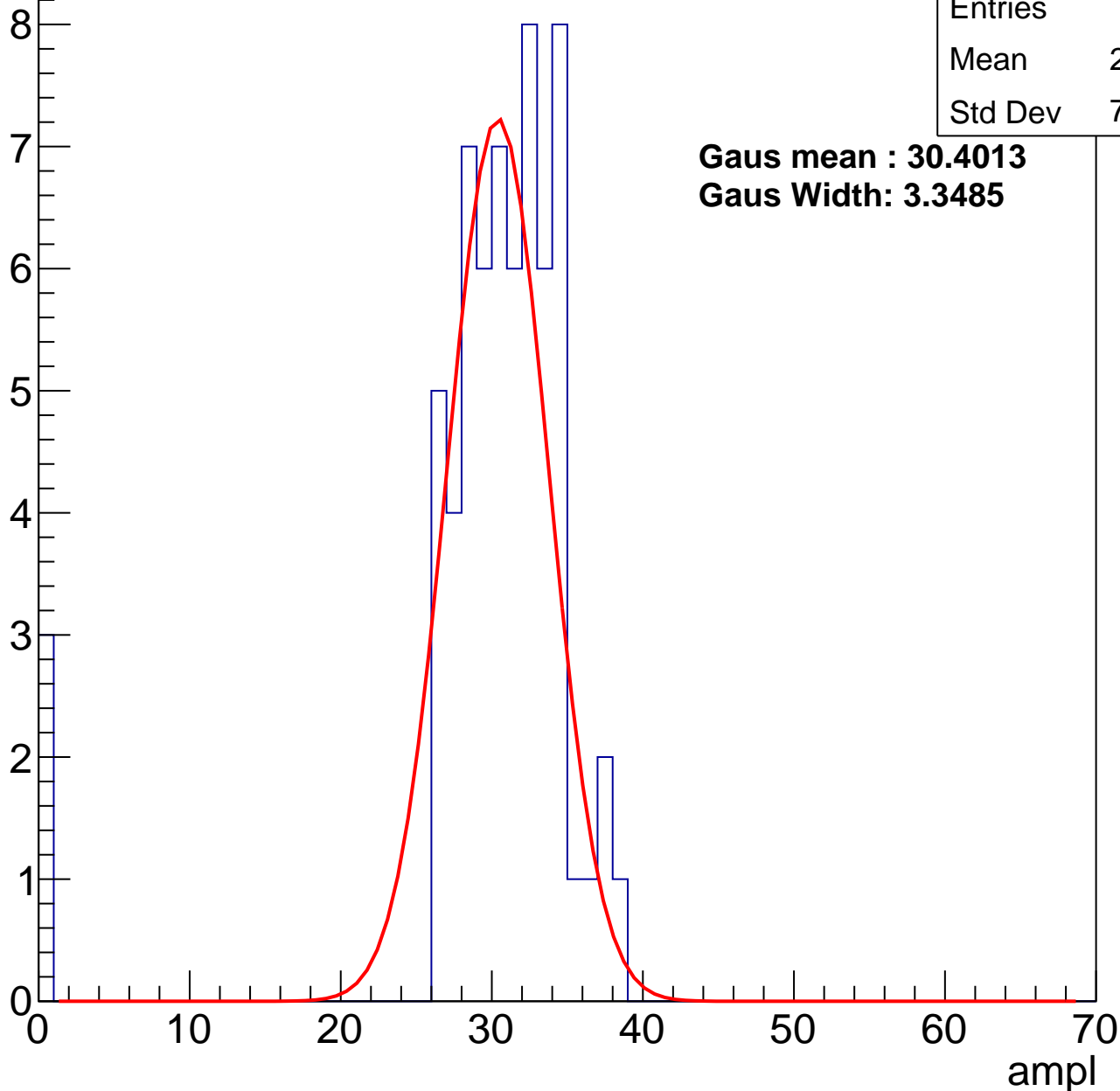
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	65
Mean	29.43
Std Dev	7.095

**Gaus mean : 30.4013**

**Gaus Width: 3.3485**



# B1L003S, U18-ch92, adc1

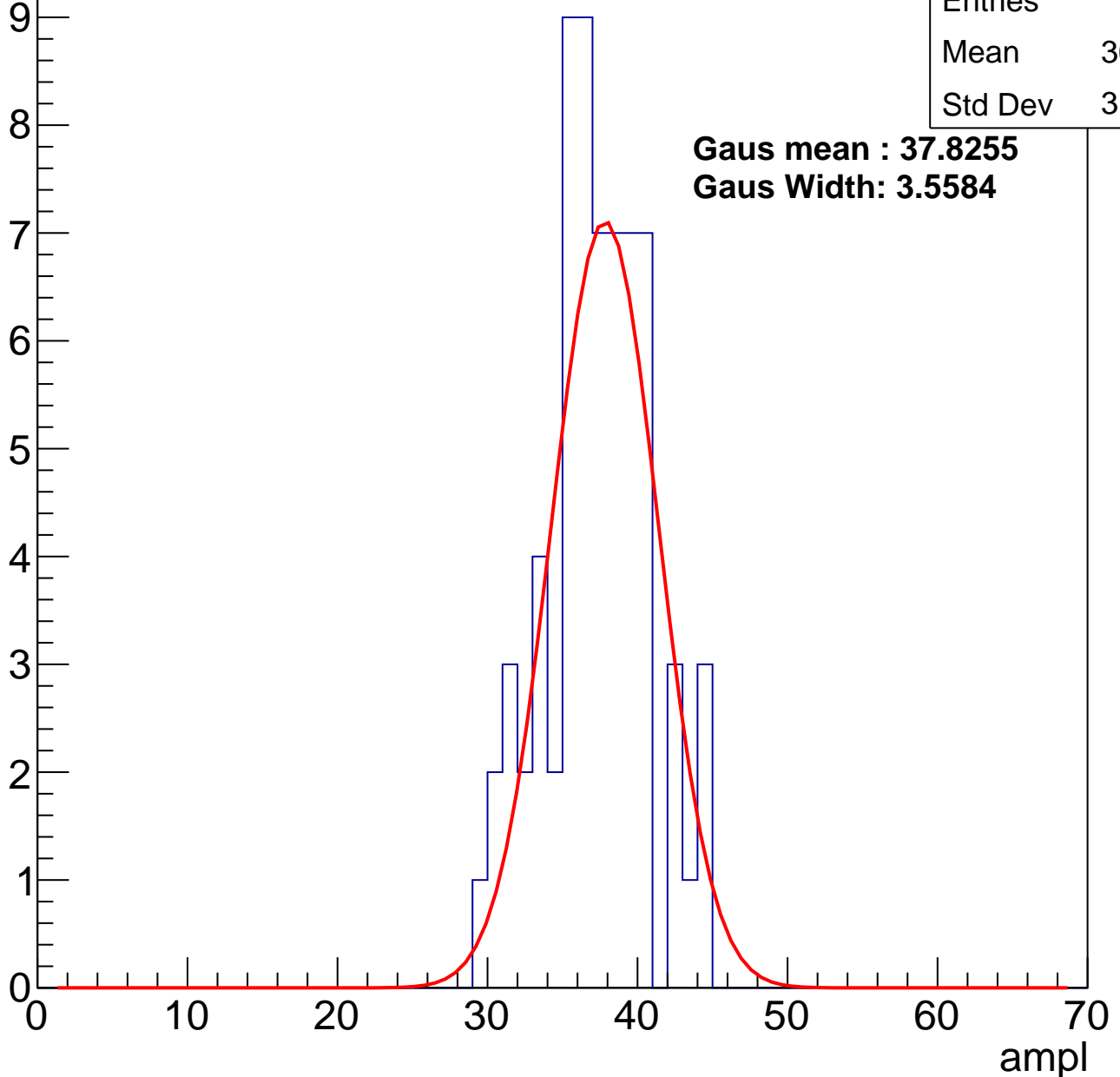
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	67
Mean	36.78
Std Dev	3.455

**Gaus mean : 37.8255**

**Gaus Width: 3.5584**



# B1L003S, U18-ch92, adc2

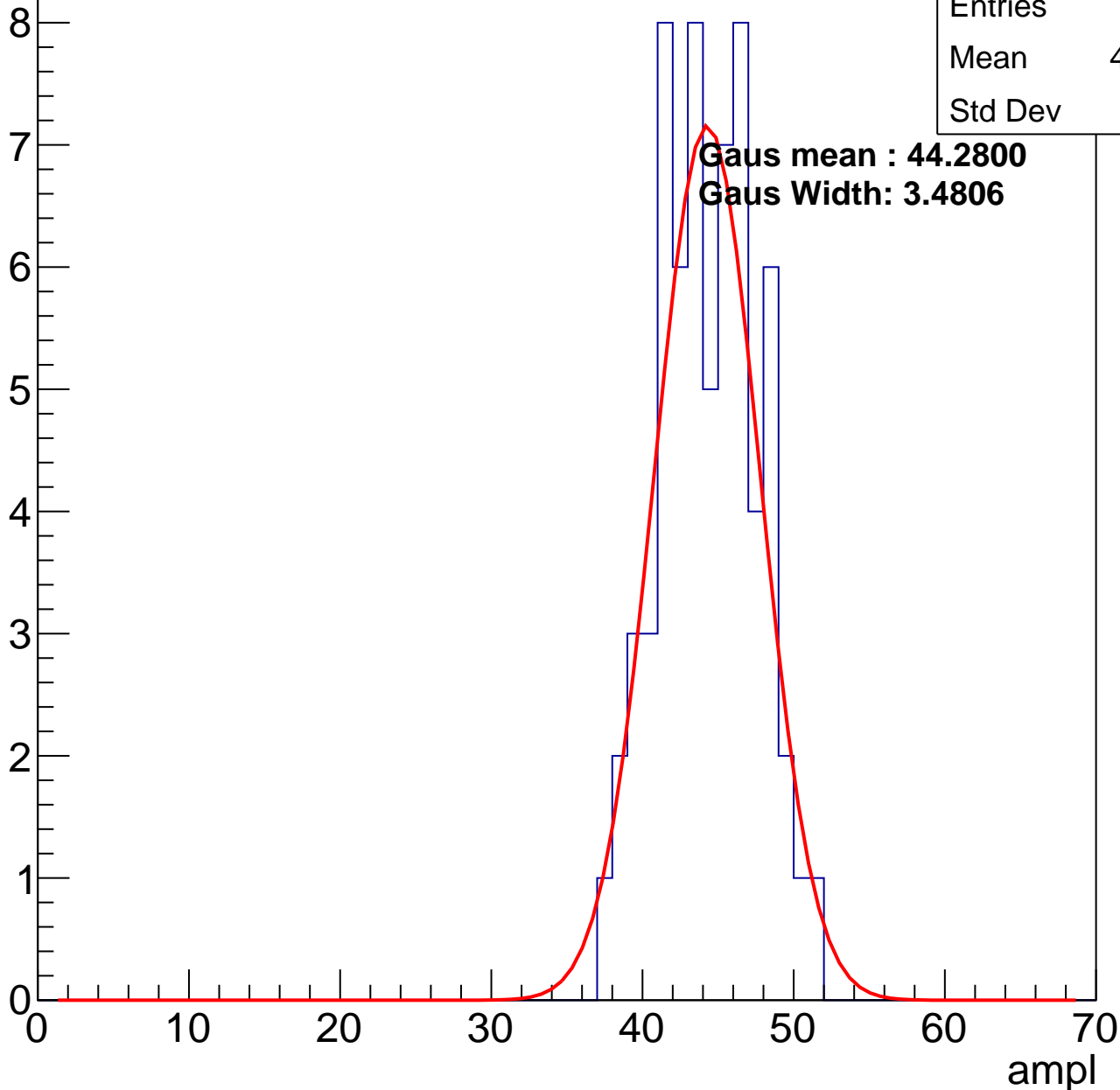
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	65
Mean	43.88
Std Dev	3.17

**Gaus mean : 44.2800**

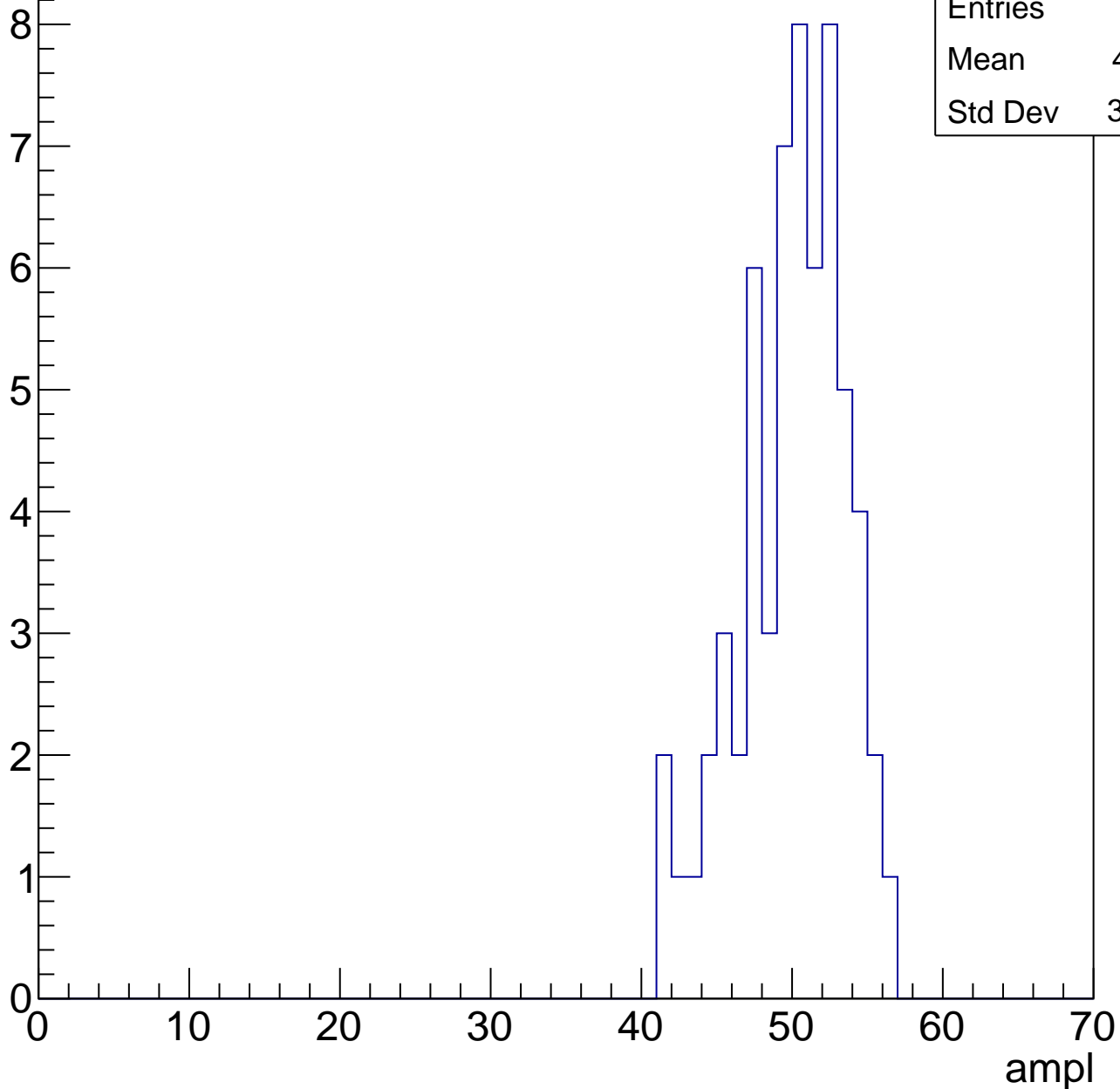
**Gaus Width: 3.4806**



# B1L003S, U18-ch92, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

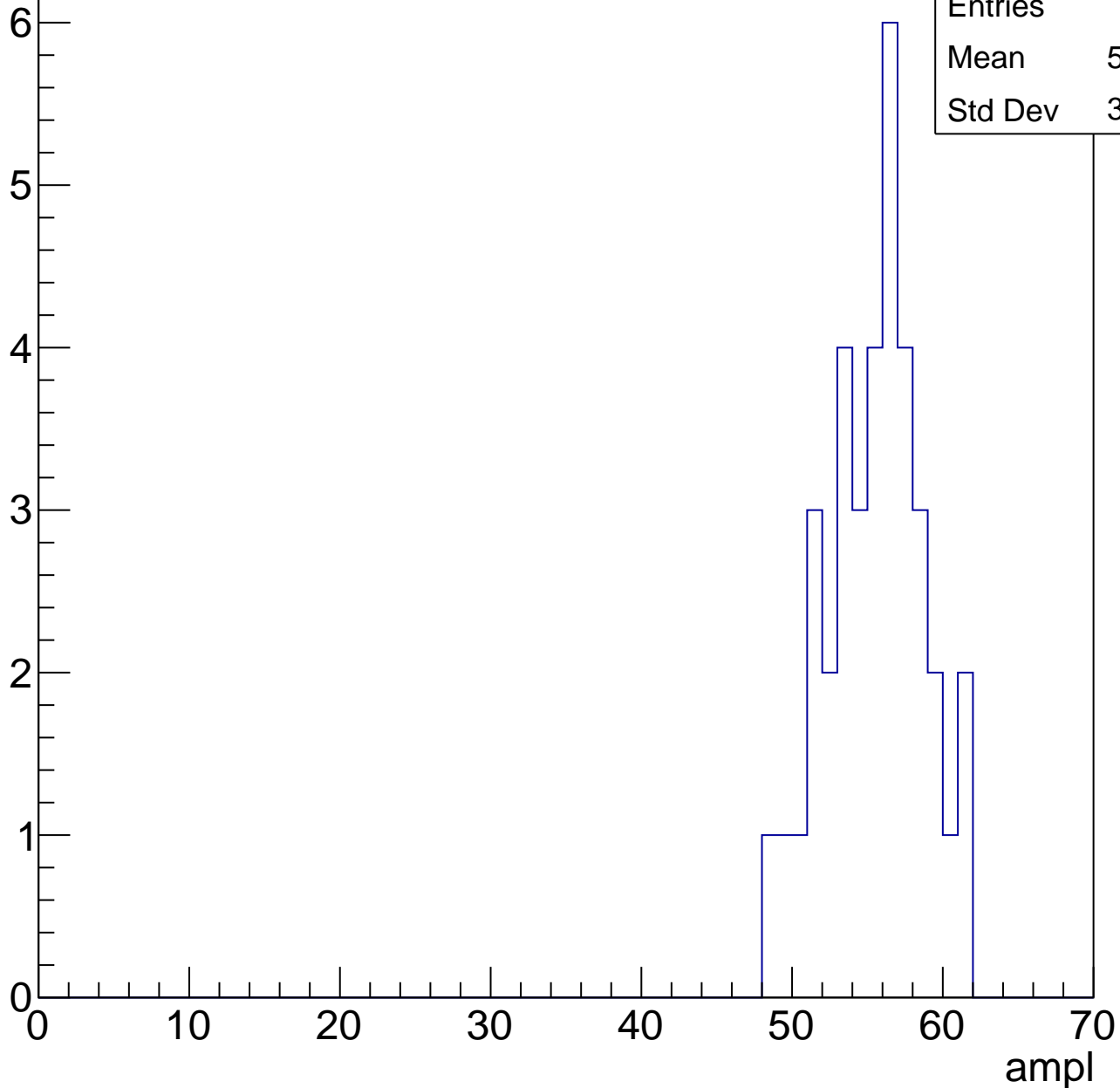
Entry



# B1L003S, U18-ch92, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



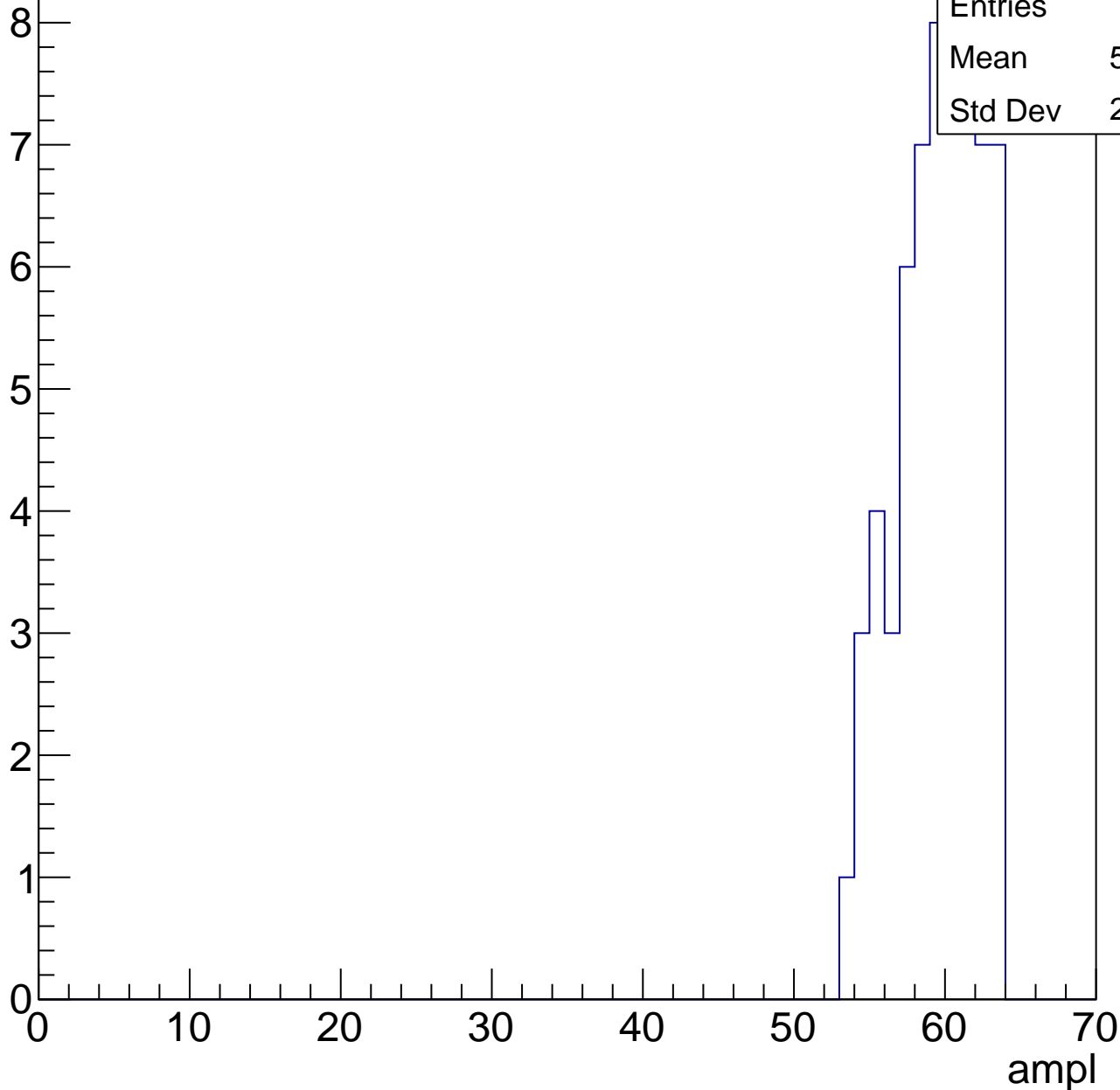
Entries	37
Mean	55.03
Std Dev	3.175

# B1L003S, U18-ch92, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	62
Mean	59.13
Std Dev	2.685



# B1L003S, U18-ch92, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

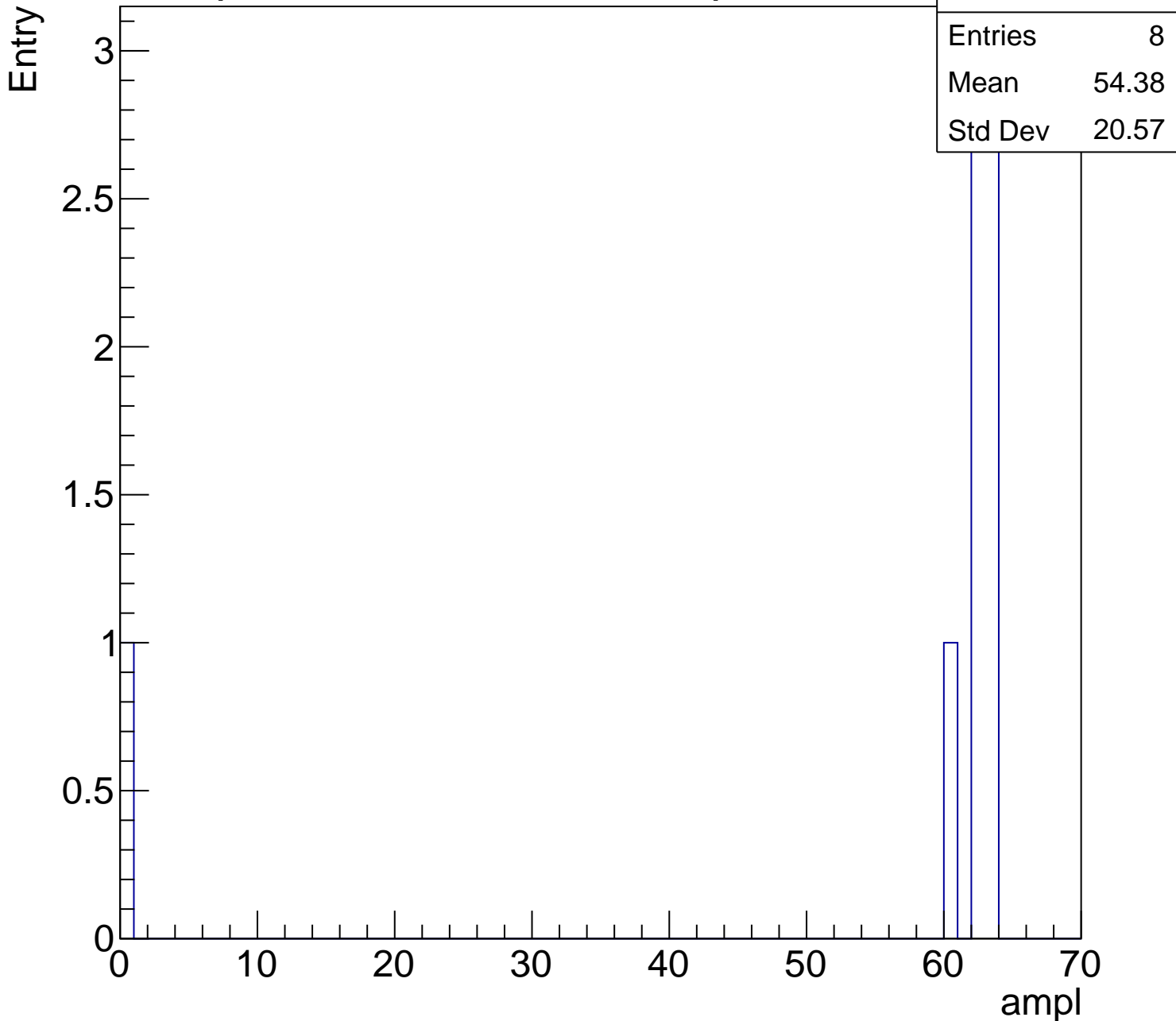
Entry

3  
2.5  
2  
1.5  
1  
0.5  
0

Entries	8
Mean	54.38
Std Dev	20.57

ampl

0 10 20 30 40 50 60 70





# B1L003S, U18-ch92, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U18-ch93, adc0

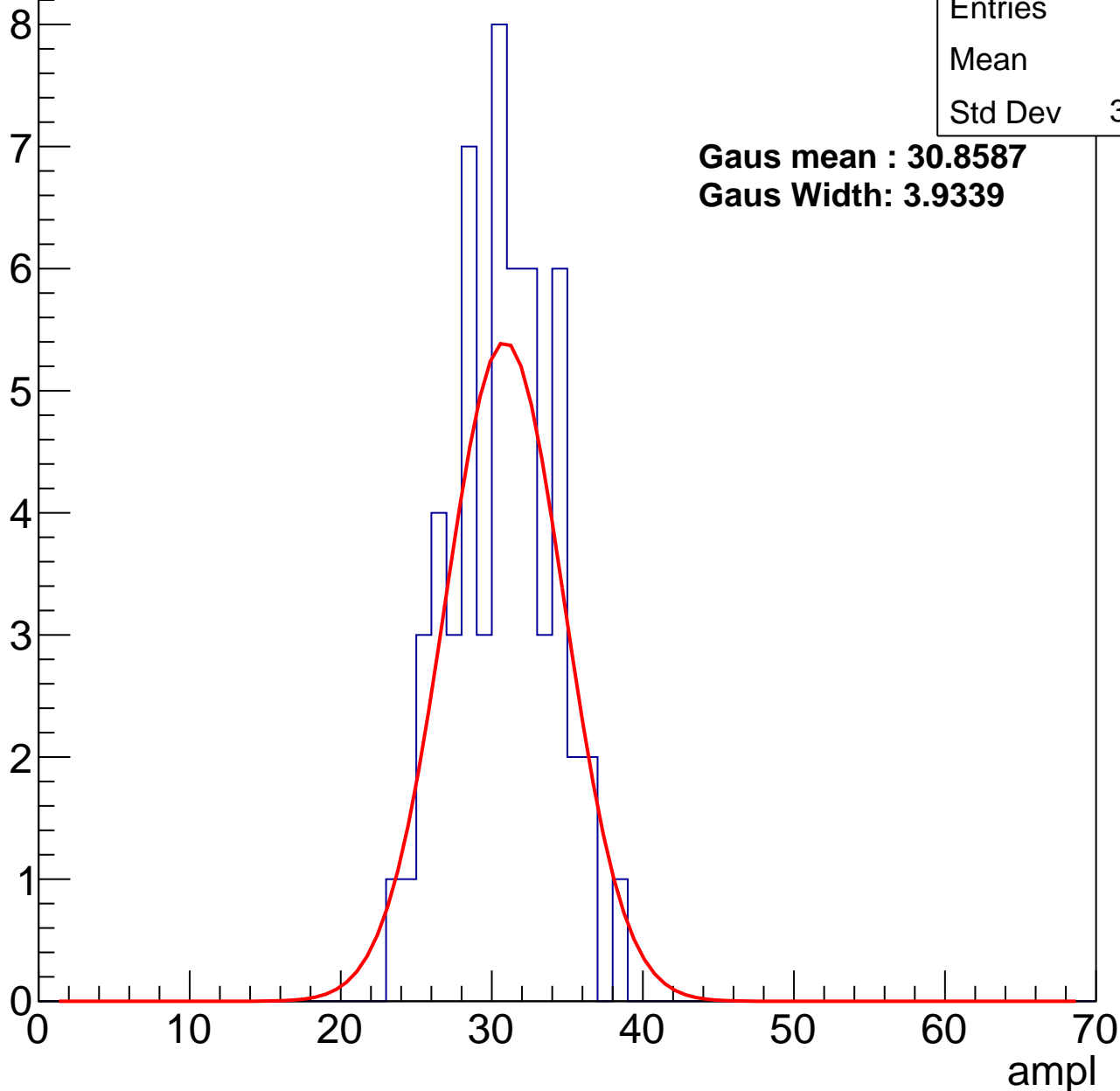
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	56
Mean	30.2
Std Dev	3.324

**Gaus mean : 30.8587**

**Gaus Width: 3.9339**



# B1L003S, U18-ch93, adc1

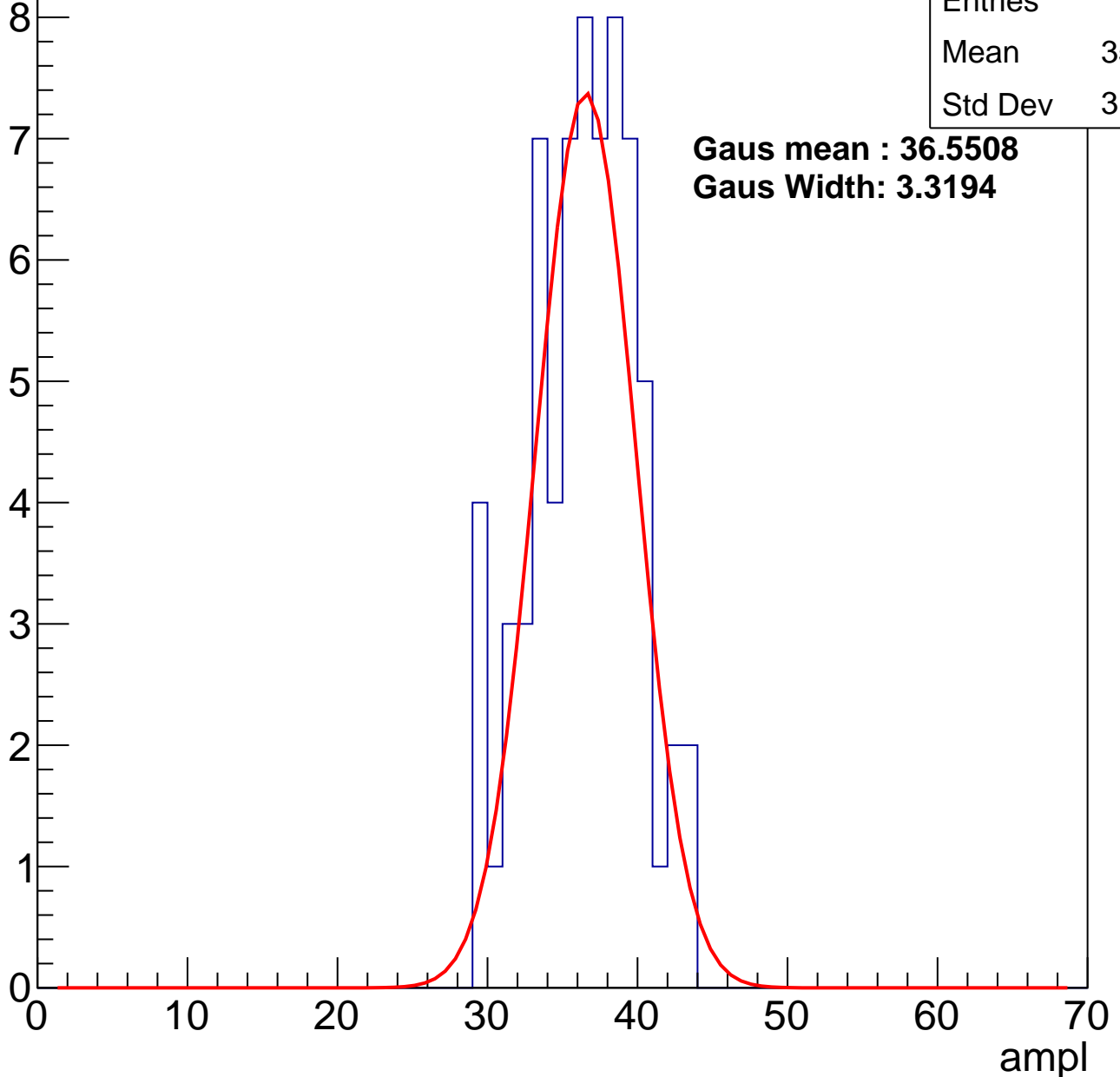
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	69
Mean	35.97
Std Dev	3.443

**Gaus mean : 36.5508**

**Gaus Width: 3.3194**



# B1L003S, U18-ch93, adc2

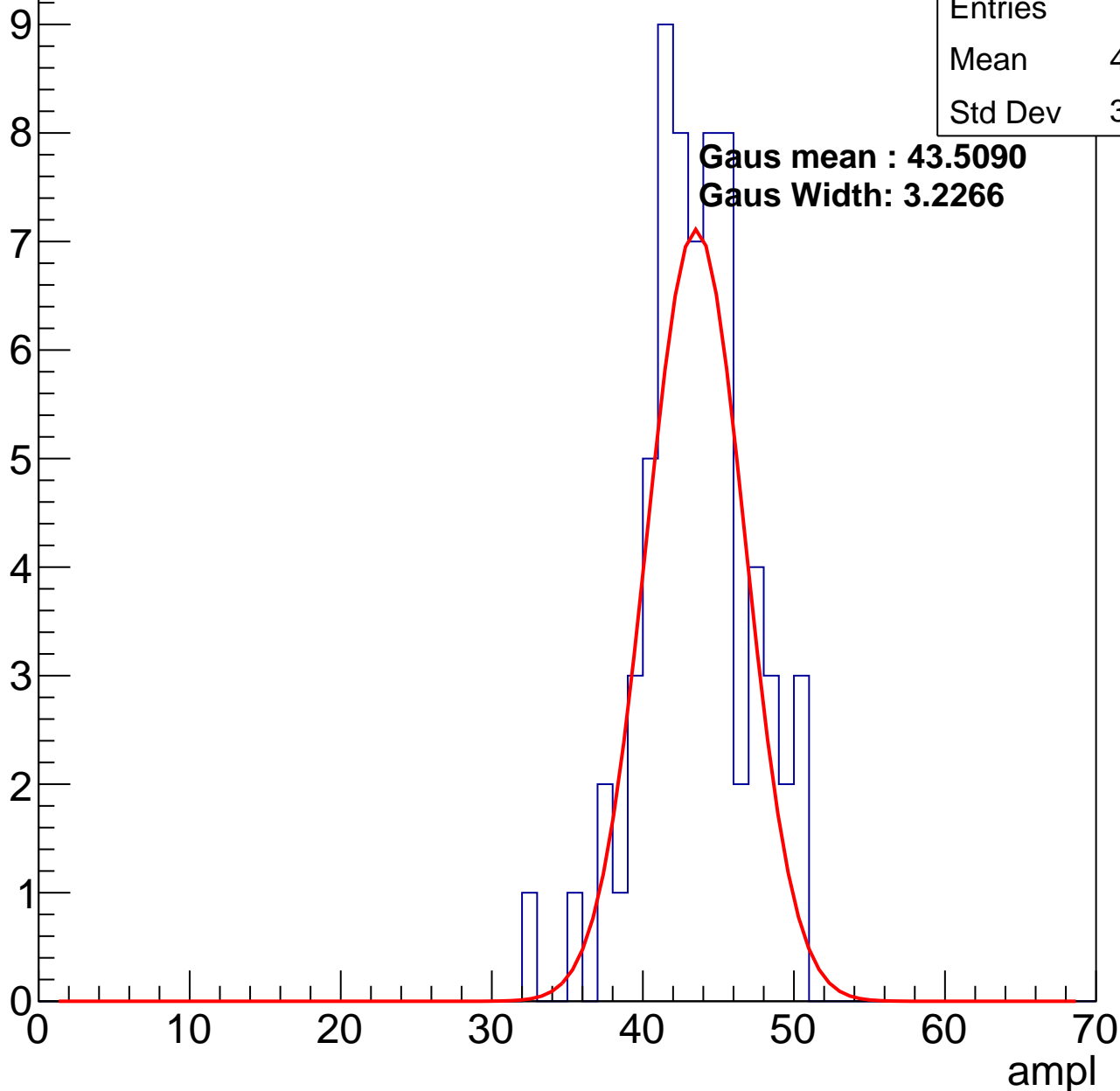
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	67
Mean	43.07
Std Dev	3.529

**Gaus mean : 43.5090**

**Gaus Width: 3.2266**

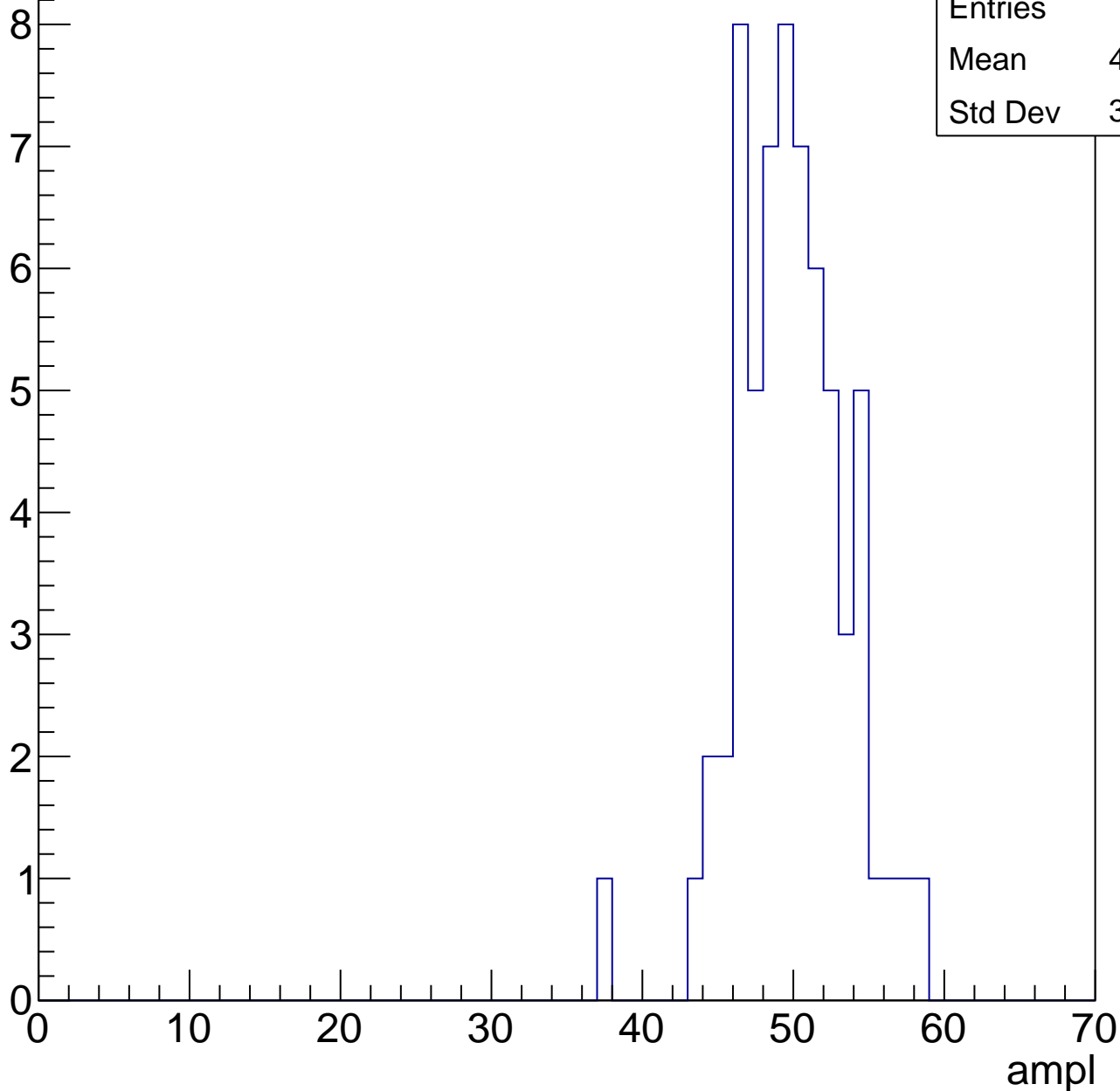


# B1L003S, U18-ch93, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	64
Mean	49.38
Std Dev	3.603

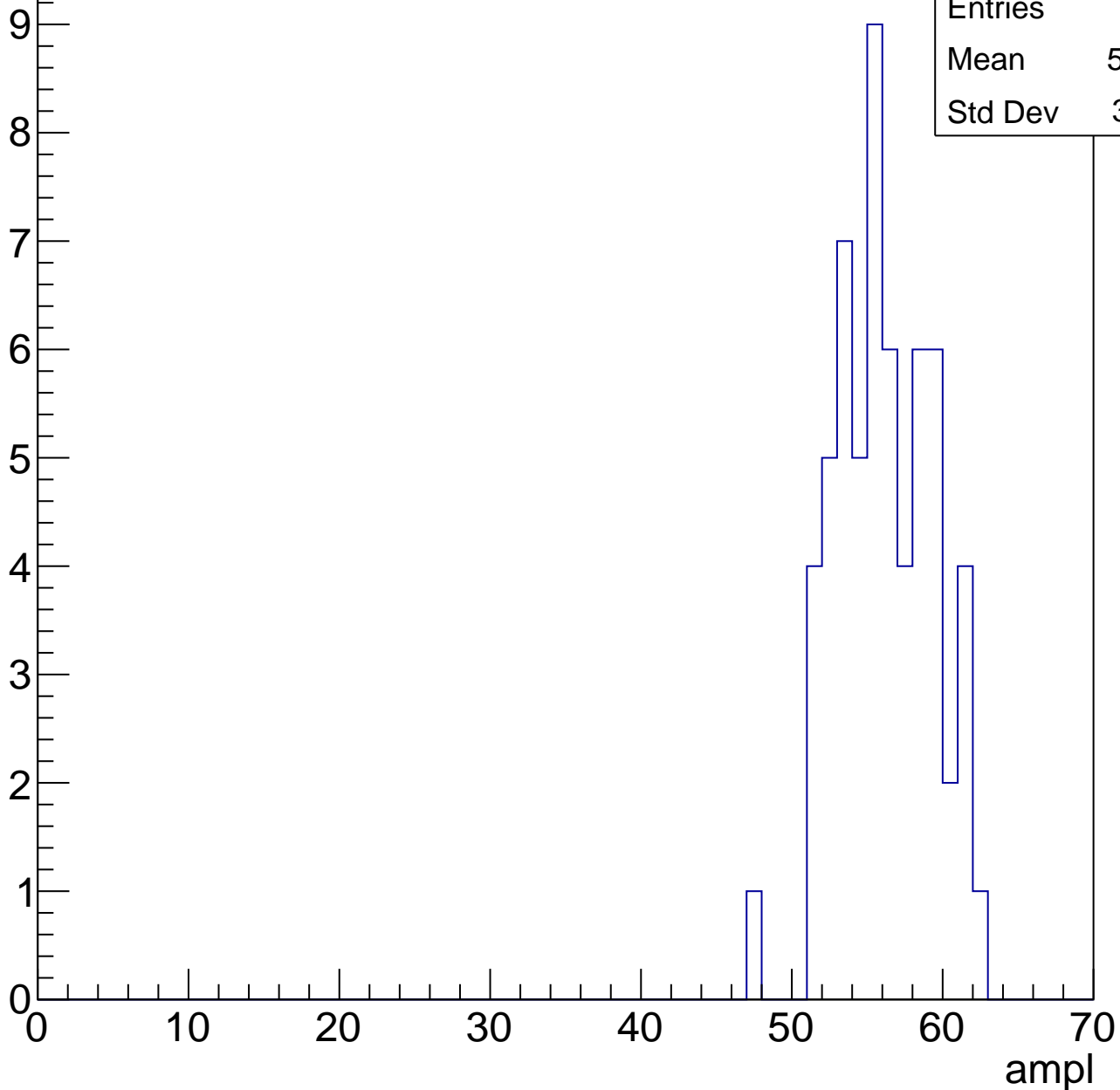


# B1L003S, U18-ch93, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	60
Mean	55.65
Std Dev	3.151

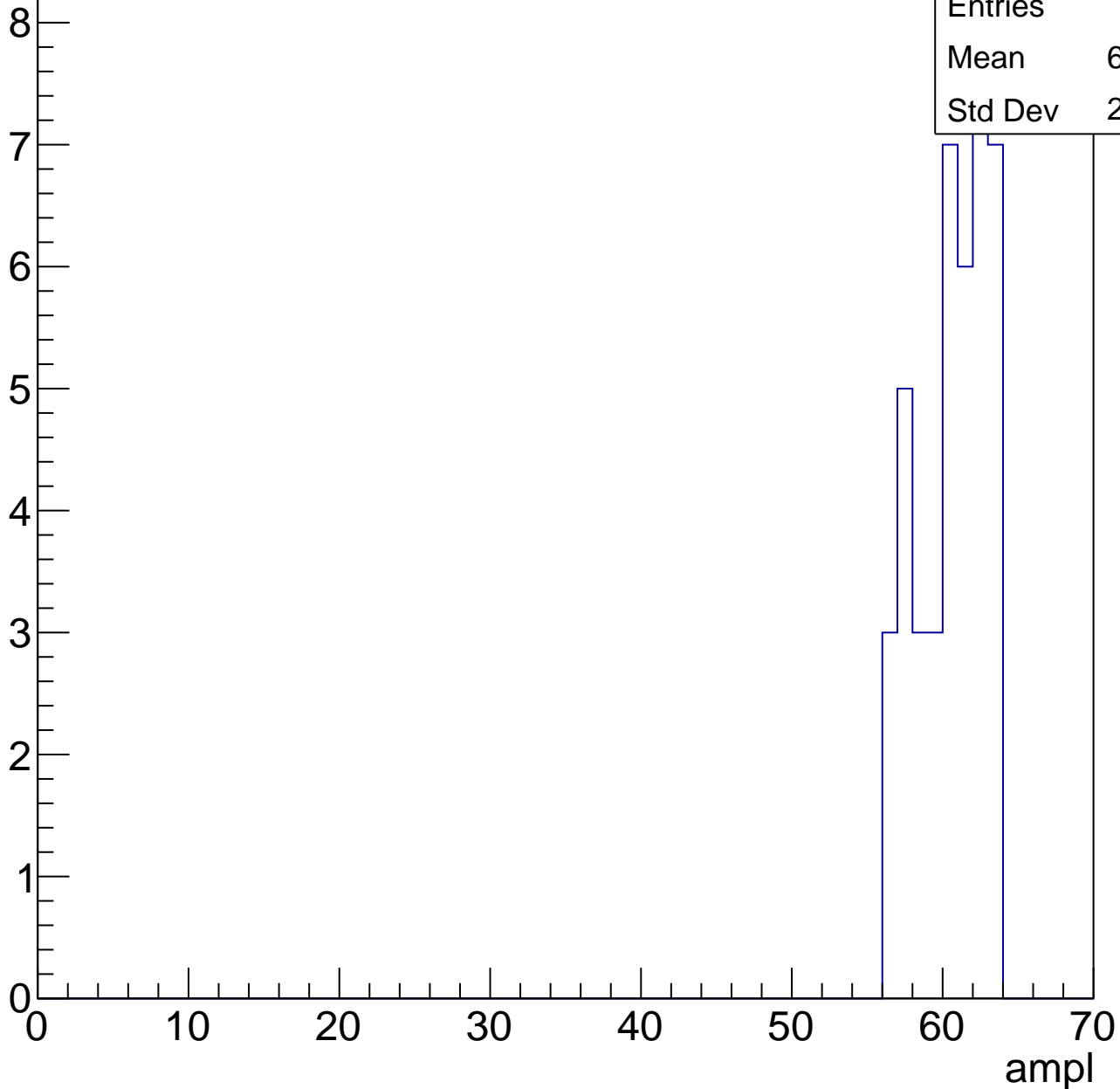


# B1L003S, U18-ch93, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

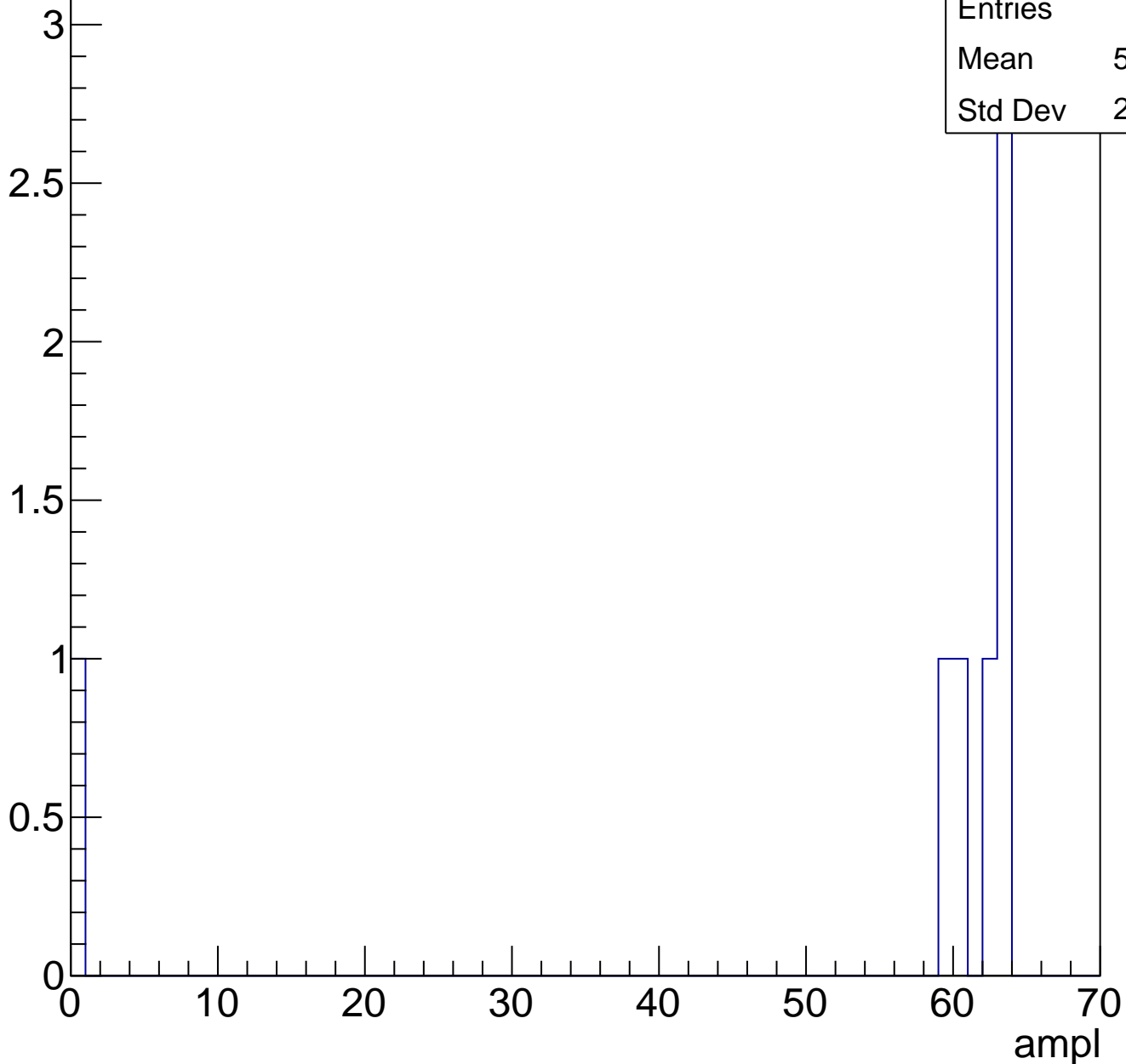
Entries	42
Mean	60.17
Std Dev	2.225



# B1L003S, U18-ch93, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U18-ch93, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch94, adc0

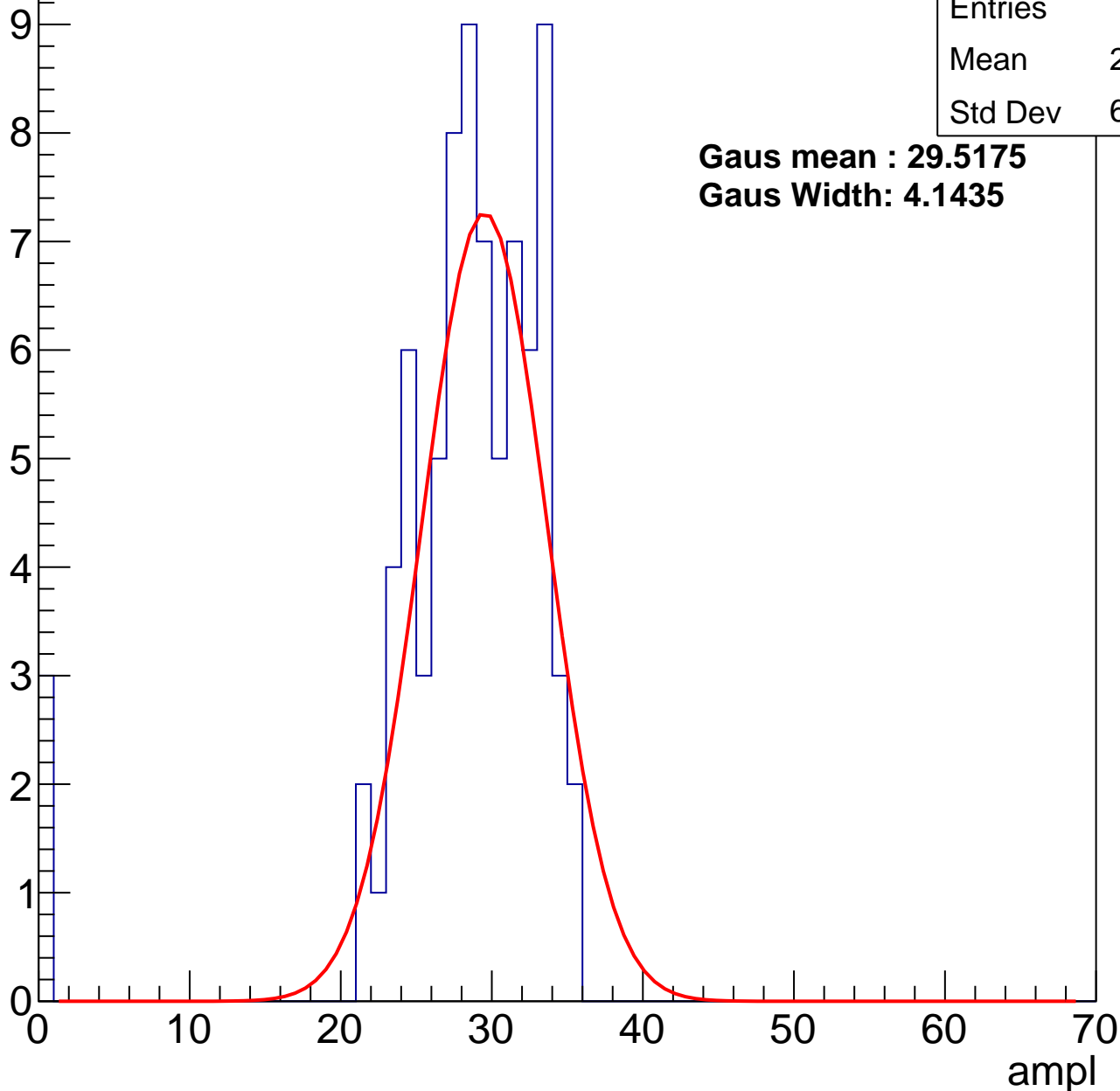
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	80
Mean	27.55
Std Dev	6.459

**Gaus mean : 29.5175**

**Gaus Width: 4.1435**



# B1L003S, U18-ch94, adc1

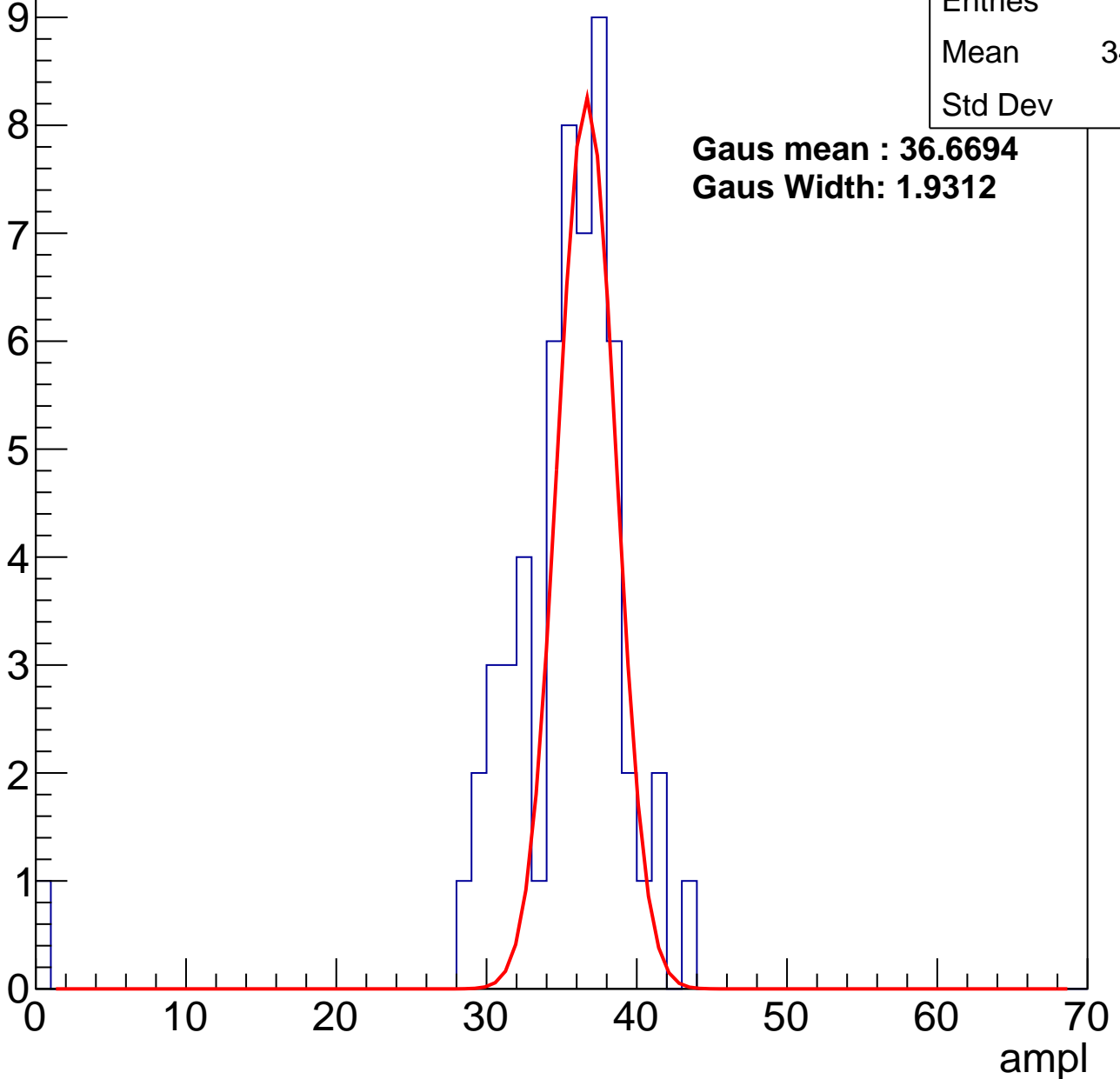
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	57
Mean	34.56
Std Dev	5.61

**Gaus mean : 36.6694**

**Gaus Width: 1.9312**



# B1L003S, U18-ch94, adc2

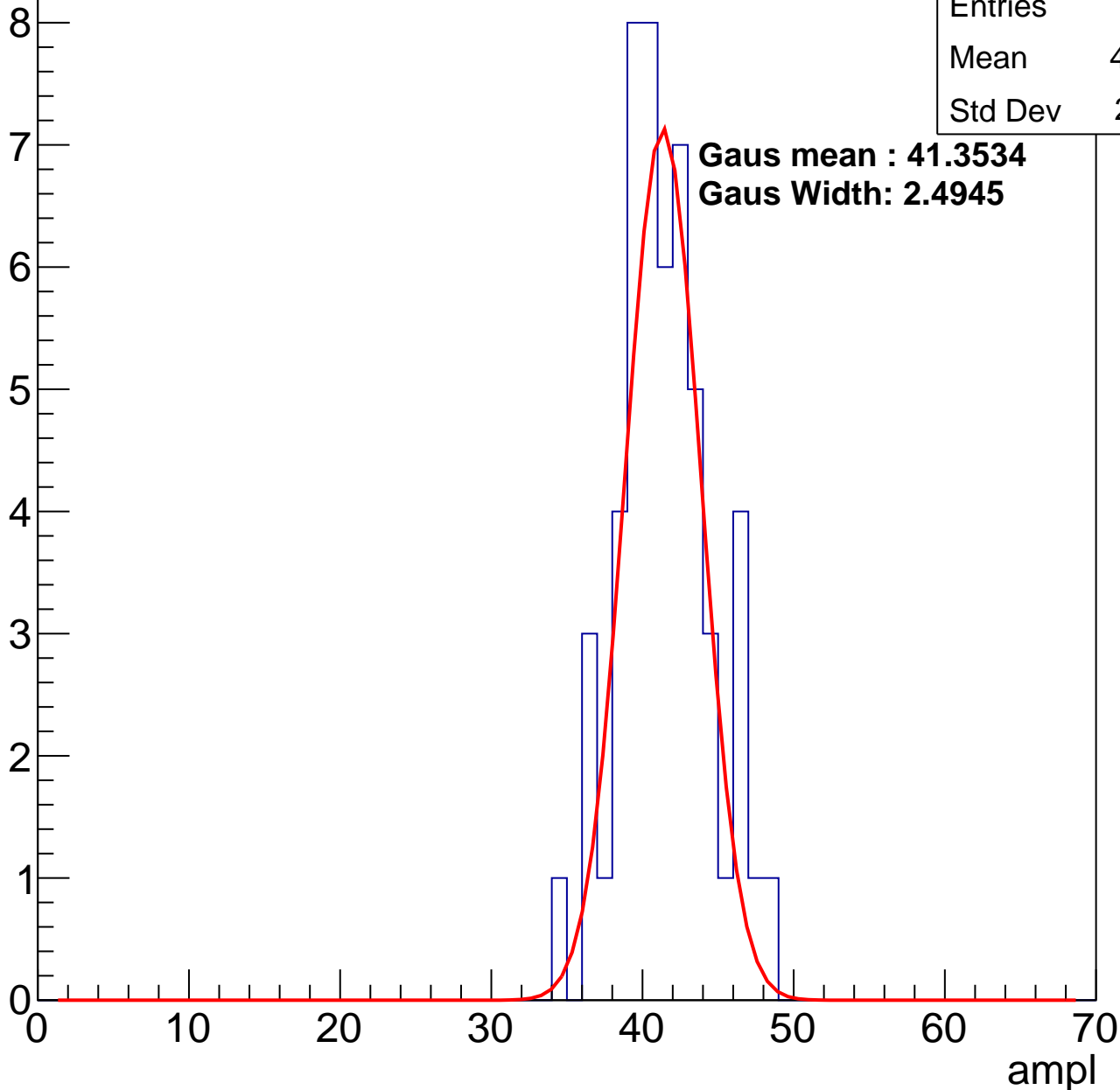
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	53
Mean	41.02
Std Dev	2.981

**Gaus mean : 41.3534**

**Gaus Width: 2.4945**

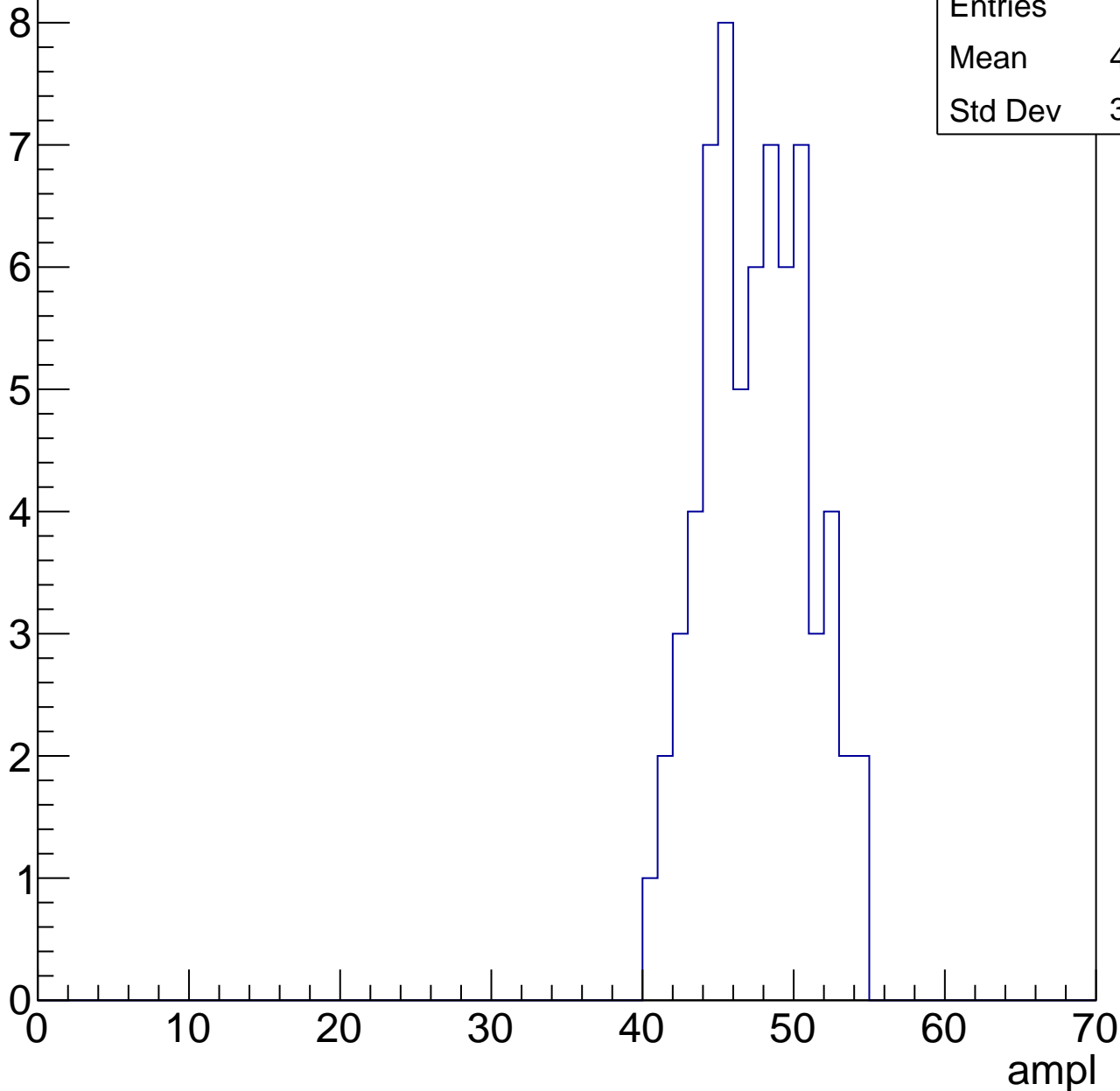


# B1L003S, U18-ch94, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	67
Mean	47.09
Std Dev	3.393

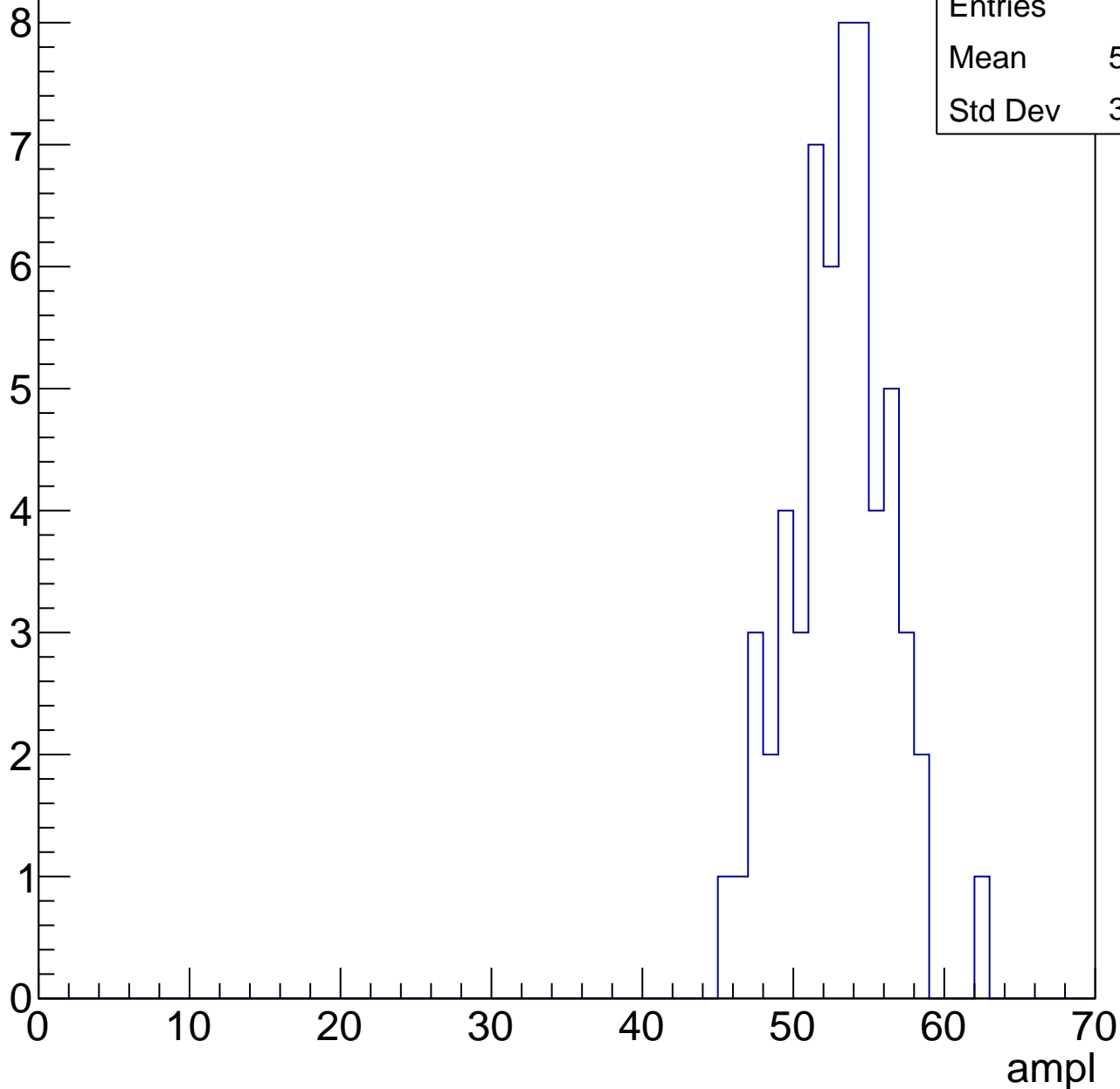


# B1L003S, U18-ch94, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	58
Mean	52.55
Std Dev	3.302

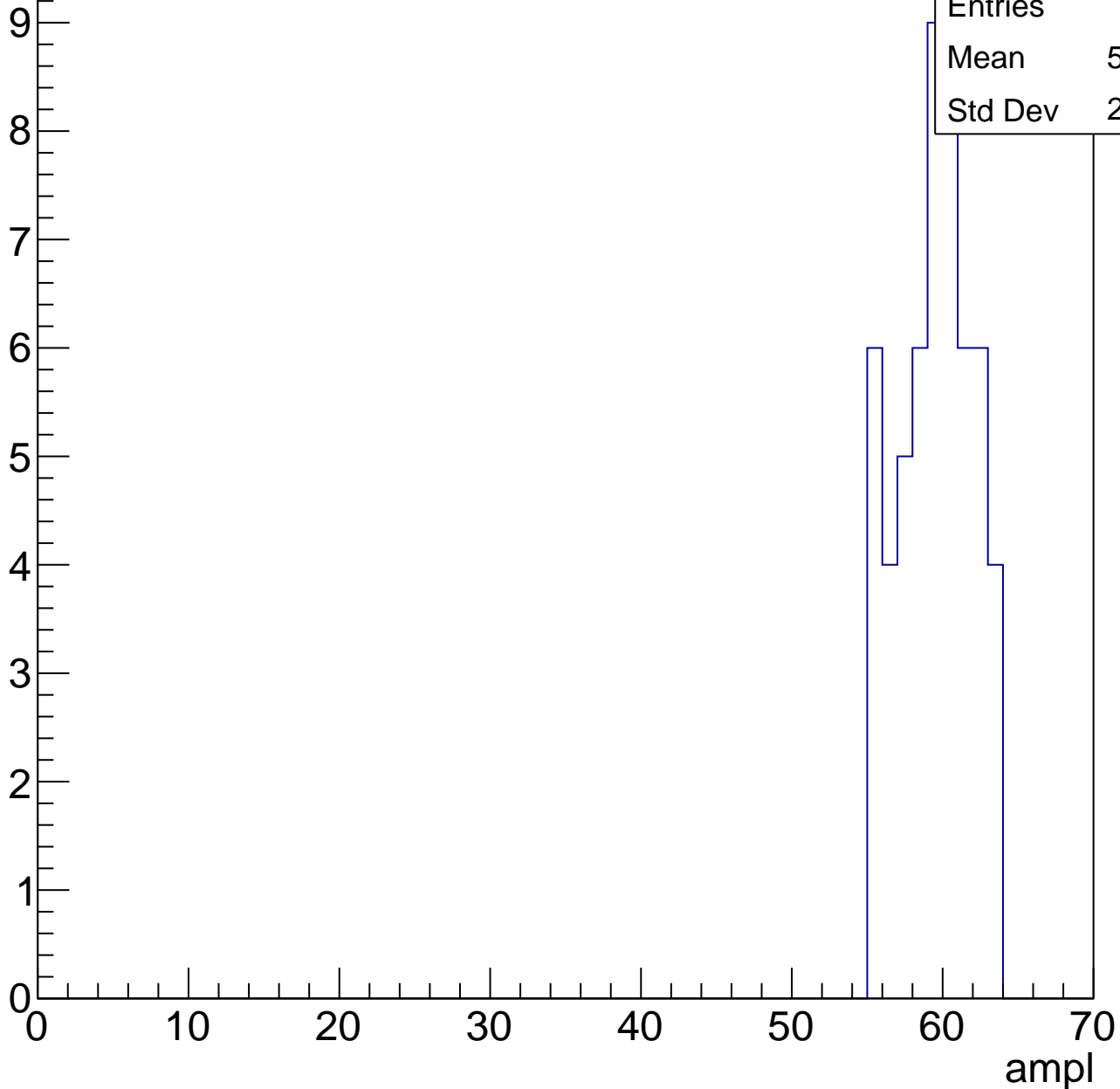


# B1L003S, U18-ch94, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	54
Mean	59.04
Std Dev	2.388

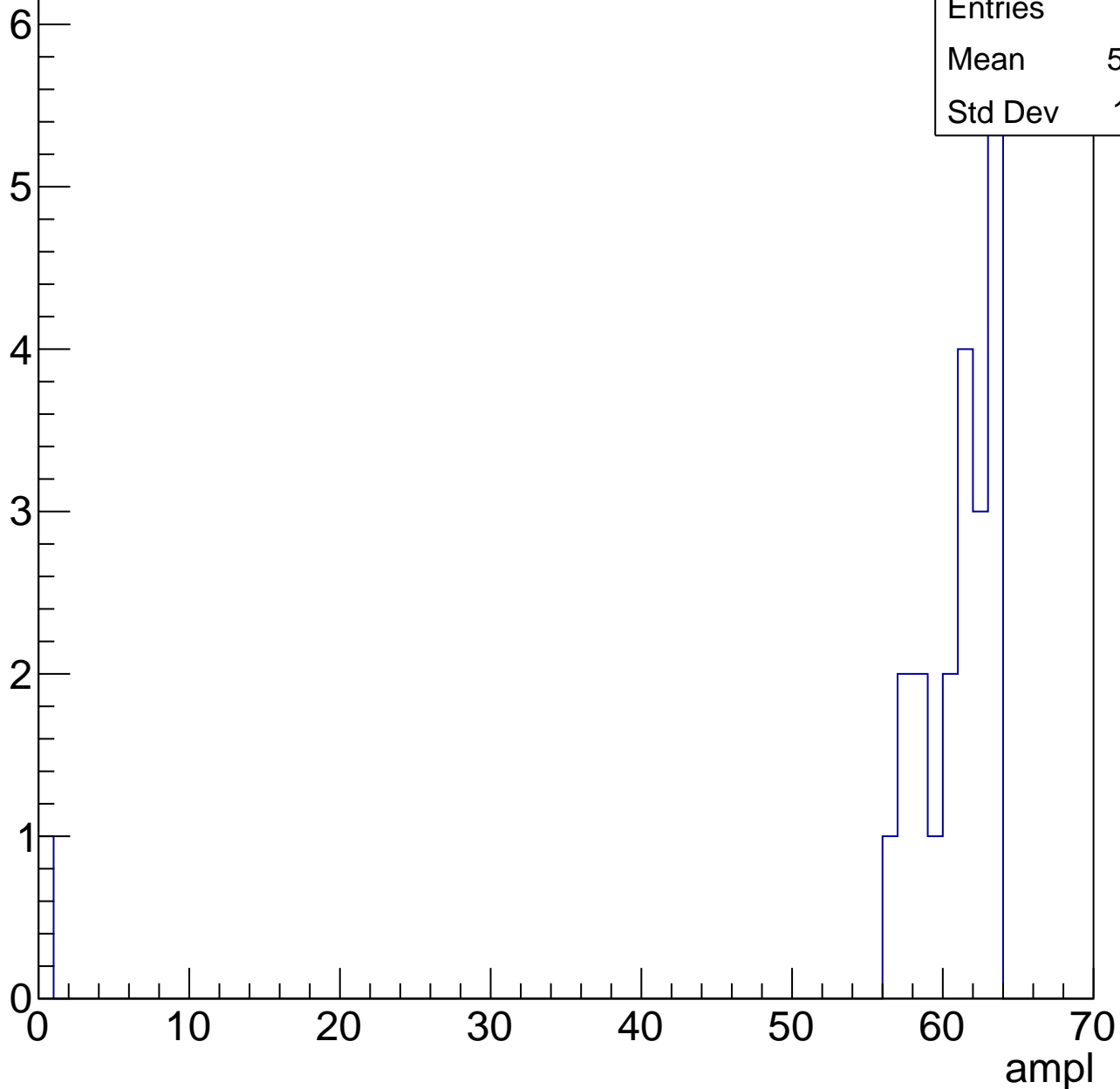


# B1L003S, U18-ch94, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	22
Mean	57.86
Std Dev	12.81





# B1L003S, U18-ch94, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U18-ch95, adc0

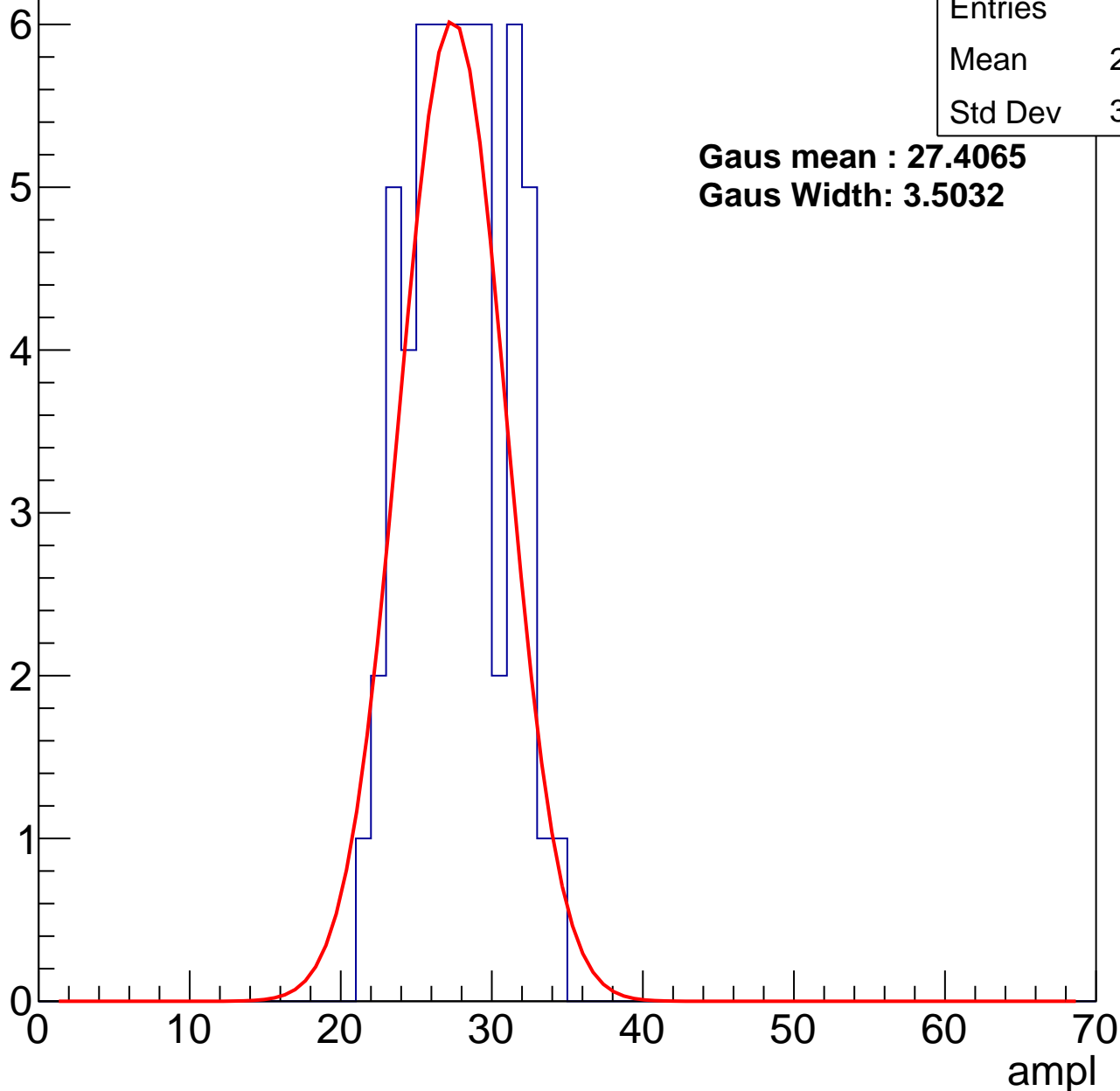
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	57
Mean	27.35
Std Dev	3.187

**Gaus mean : 27.4065**

**Gaus Width: 3.5032**

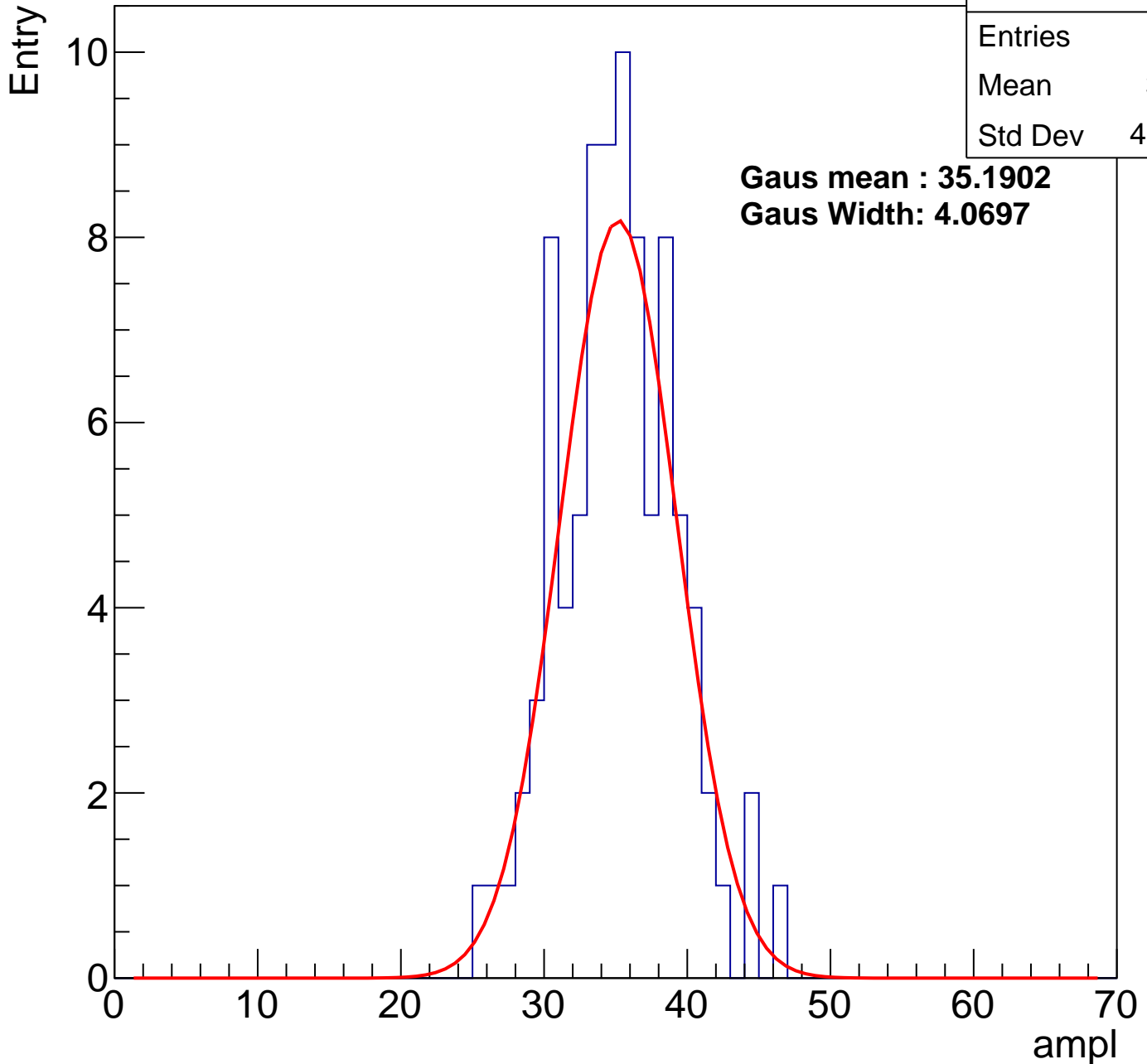


# B1L003S, U18-ch95, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	89
Mean	34.7
Std Dev	4.079

**Gaus mean : 35.1902**  
**Gaus Width: 4.0697**



# B1L003S, U18-ch95, adc2

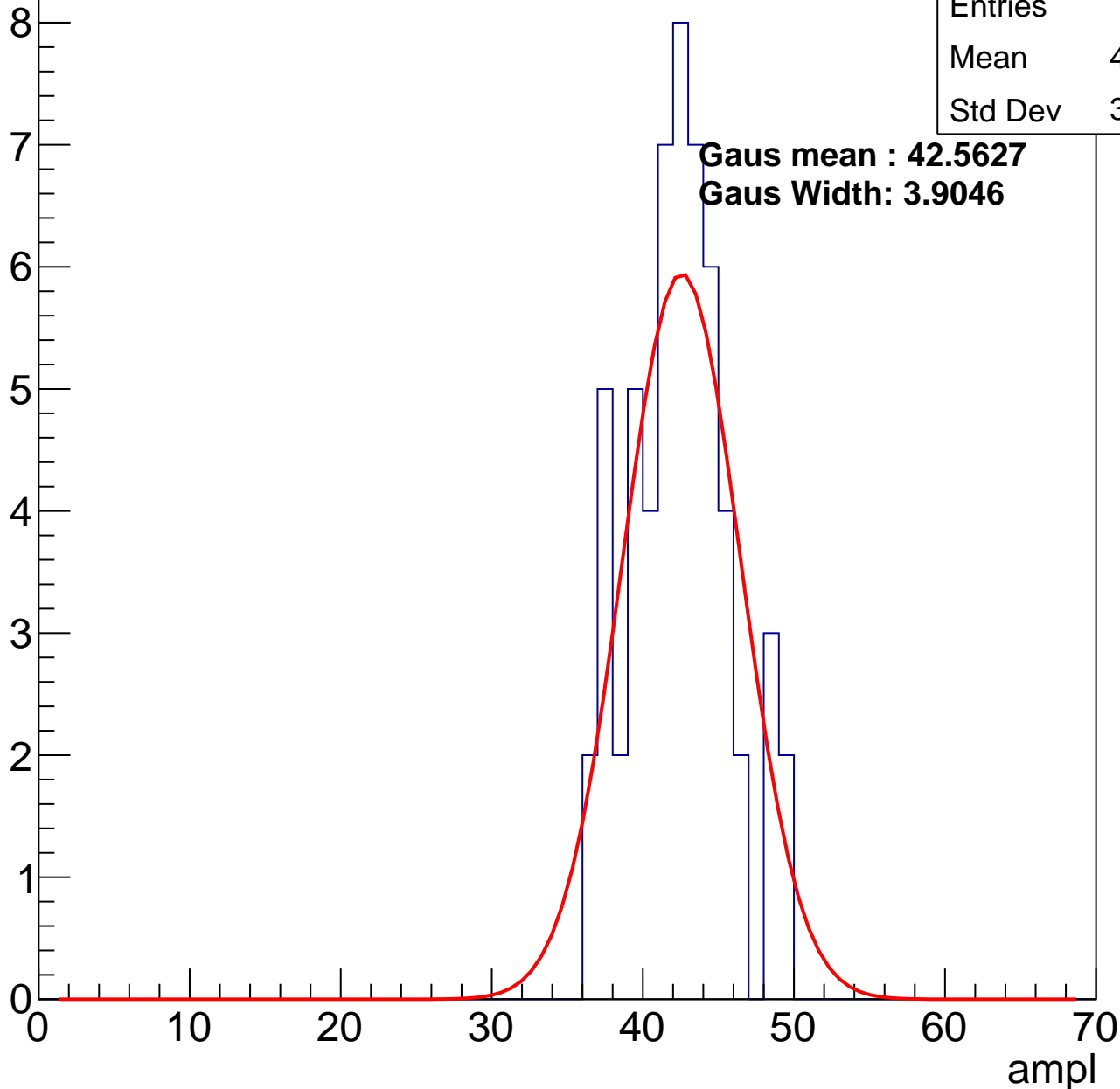
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	57
Mean	41.93
Std Dev	3.249

**Gaus mean : 42.5627**

**Gaus Width: 3.9046**

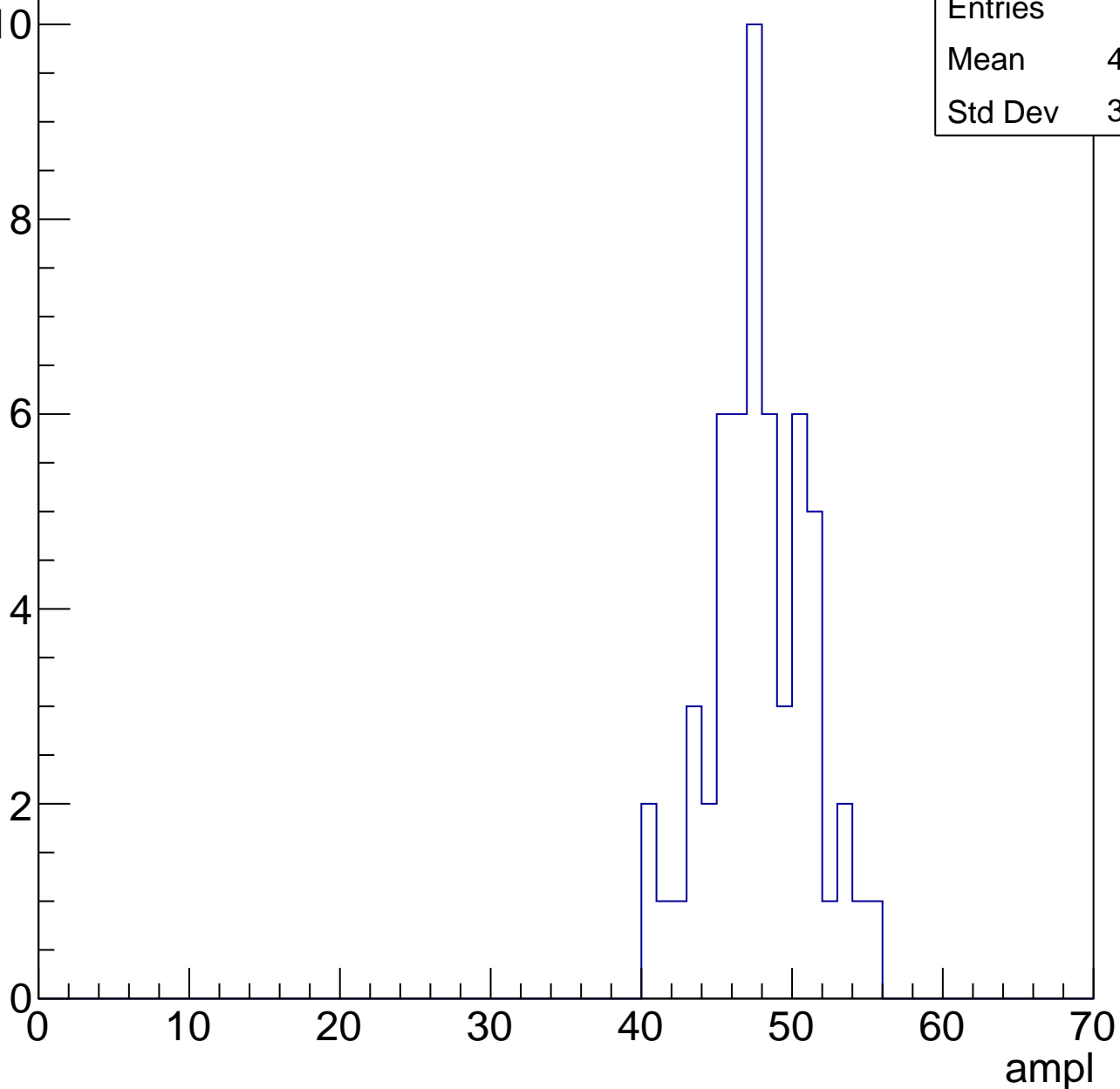


# B1L003S, U18-ch95, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	56
Mean	47.38
Std Dev	3.298

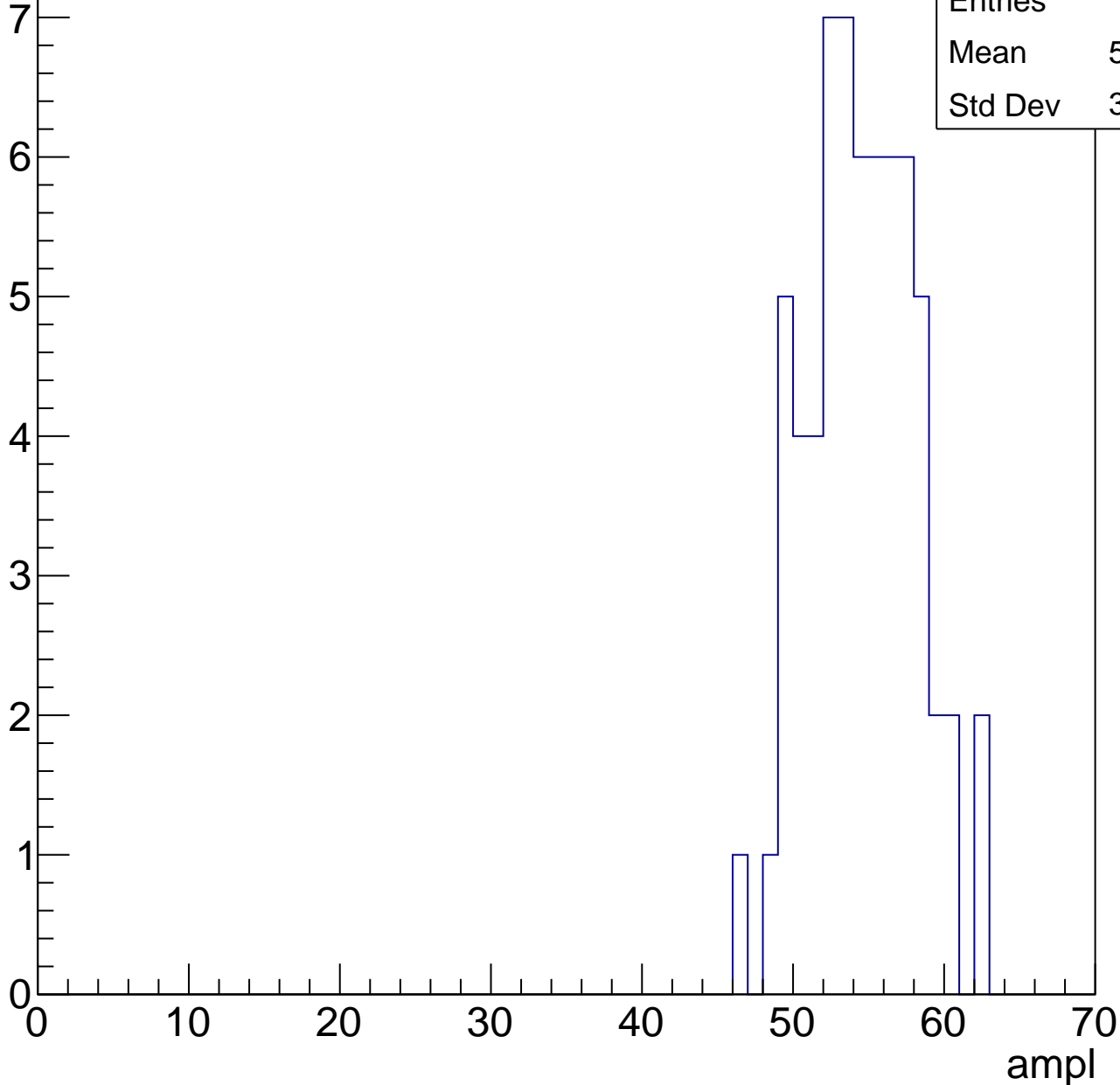


# B1L003S, U18-ch95, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	64
Mean	54.09
Std Dev	3.476

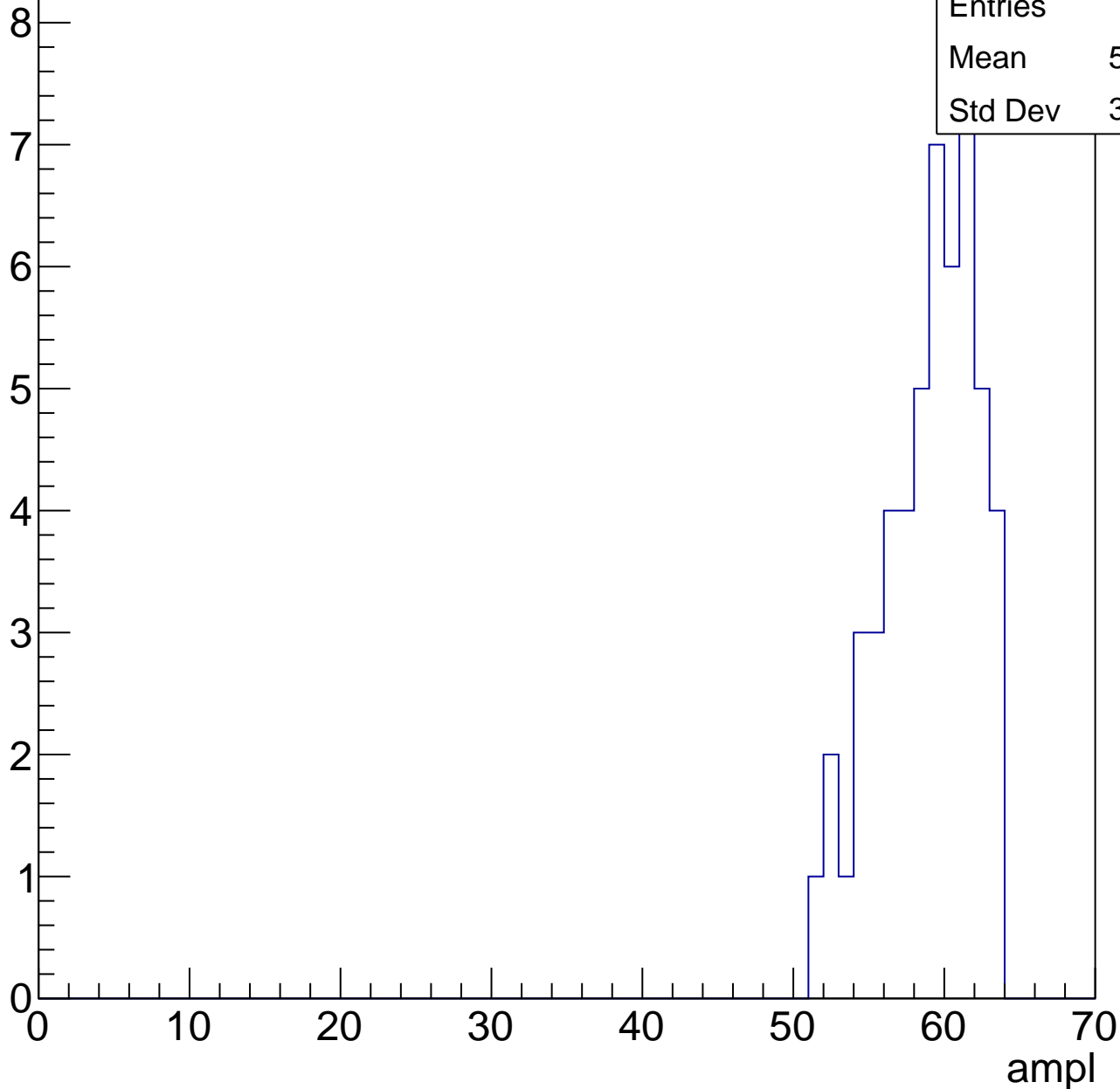


# B1L003S, U18-ch95, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	53
Mean	58.49
Std Dev	3.106

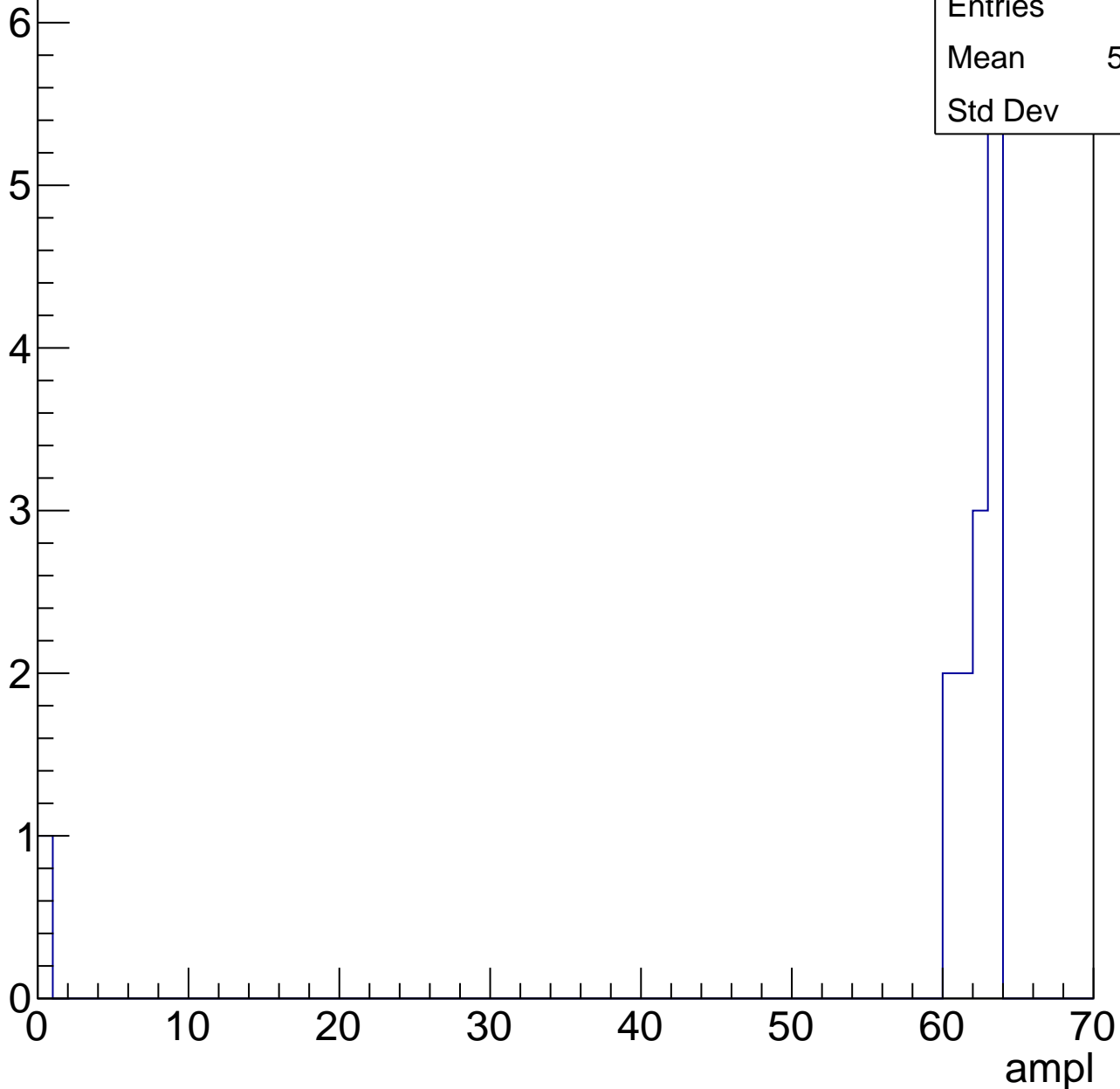


# B1L003S, U18-ch95, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	14
Mean	57.57
Std Dev	16

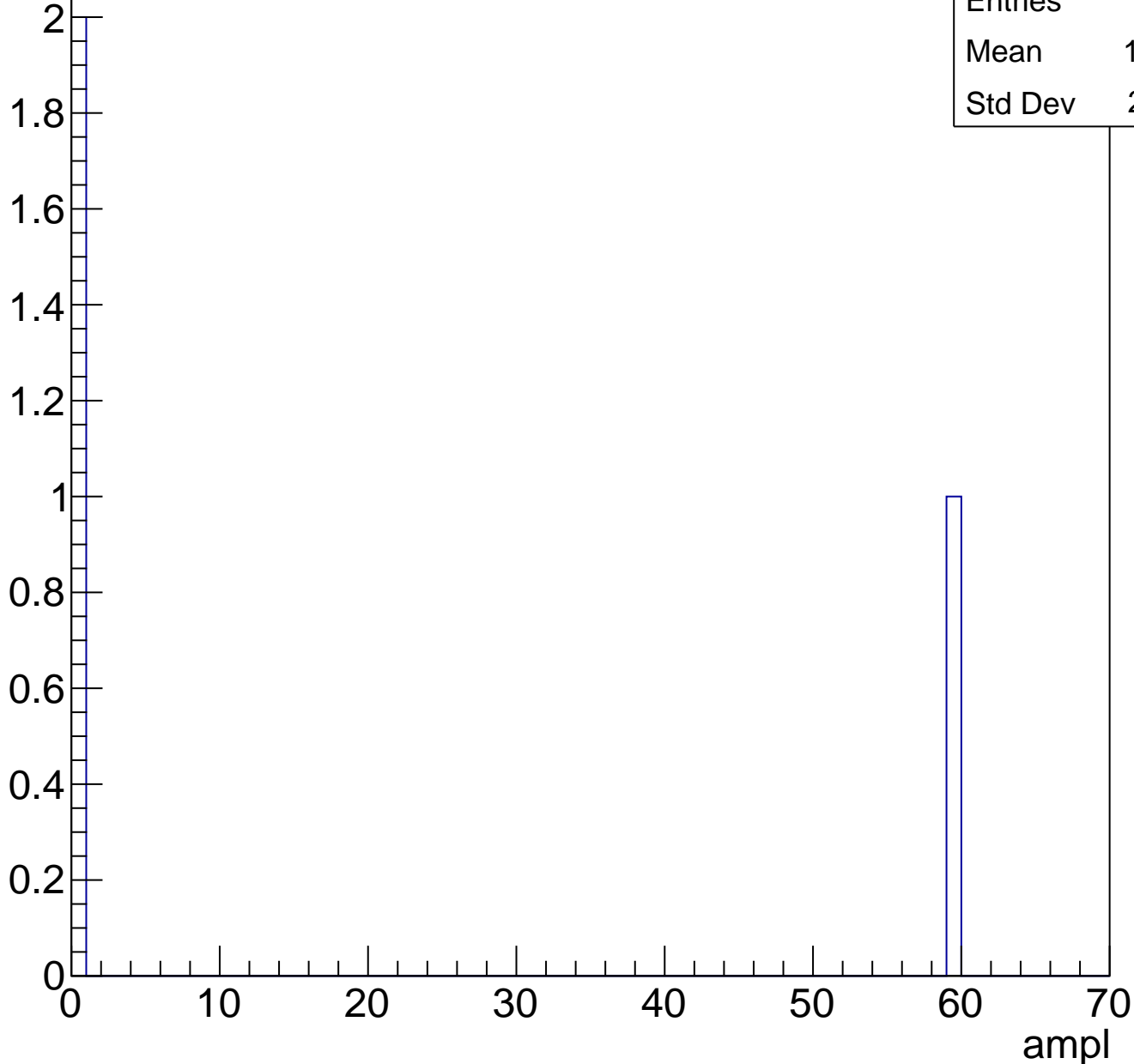




# B1L003S, U18-ch95, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U18-ch96, adc0

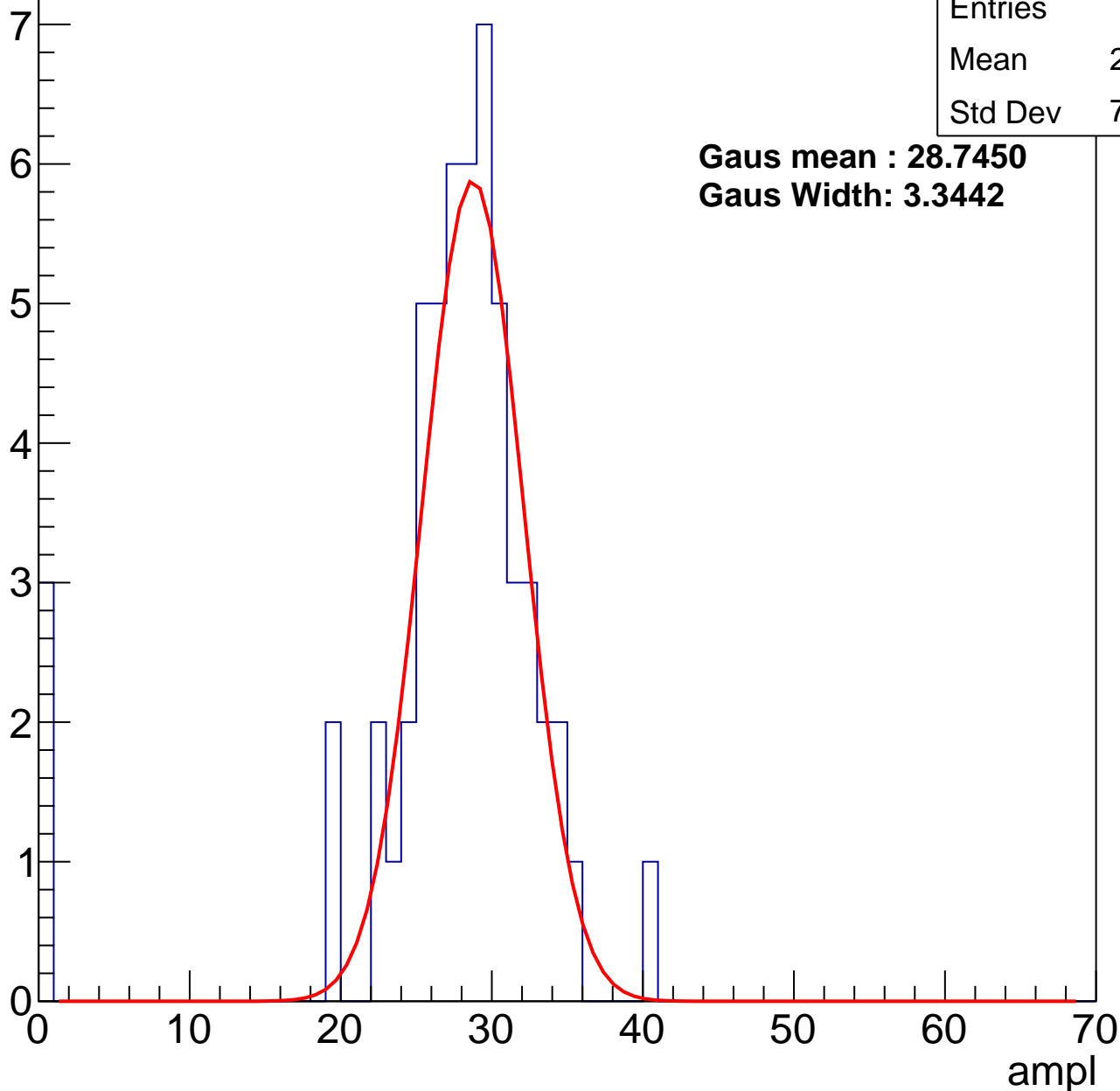
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	56
Mean	26.59
Std Dev	7.343

**Gaus mean : 28.7450**

**Gaus Width: 3.3442**



# B1L003S, U18-ch96, adc1

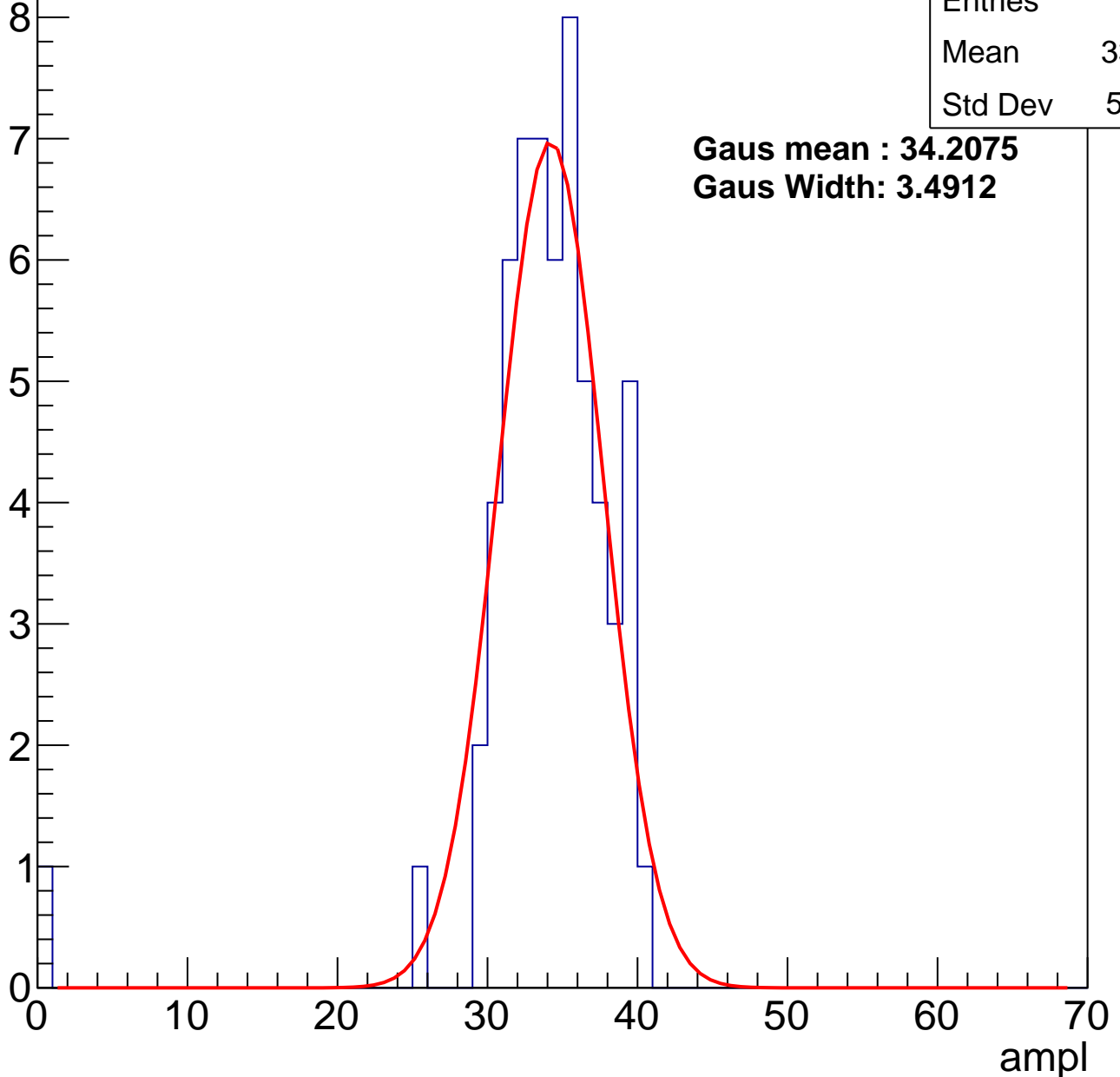
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	60
Mean	33.42
Std Dev	5.311

**Gaus mean : 34.2075**

**Gaus Width: 3.4912**



# B1L003S, U18-ch96, adc2

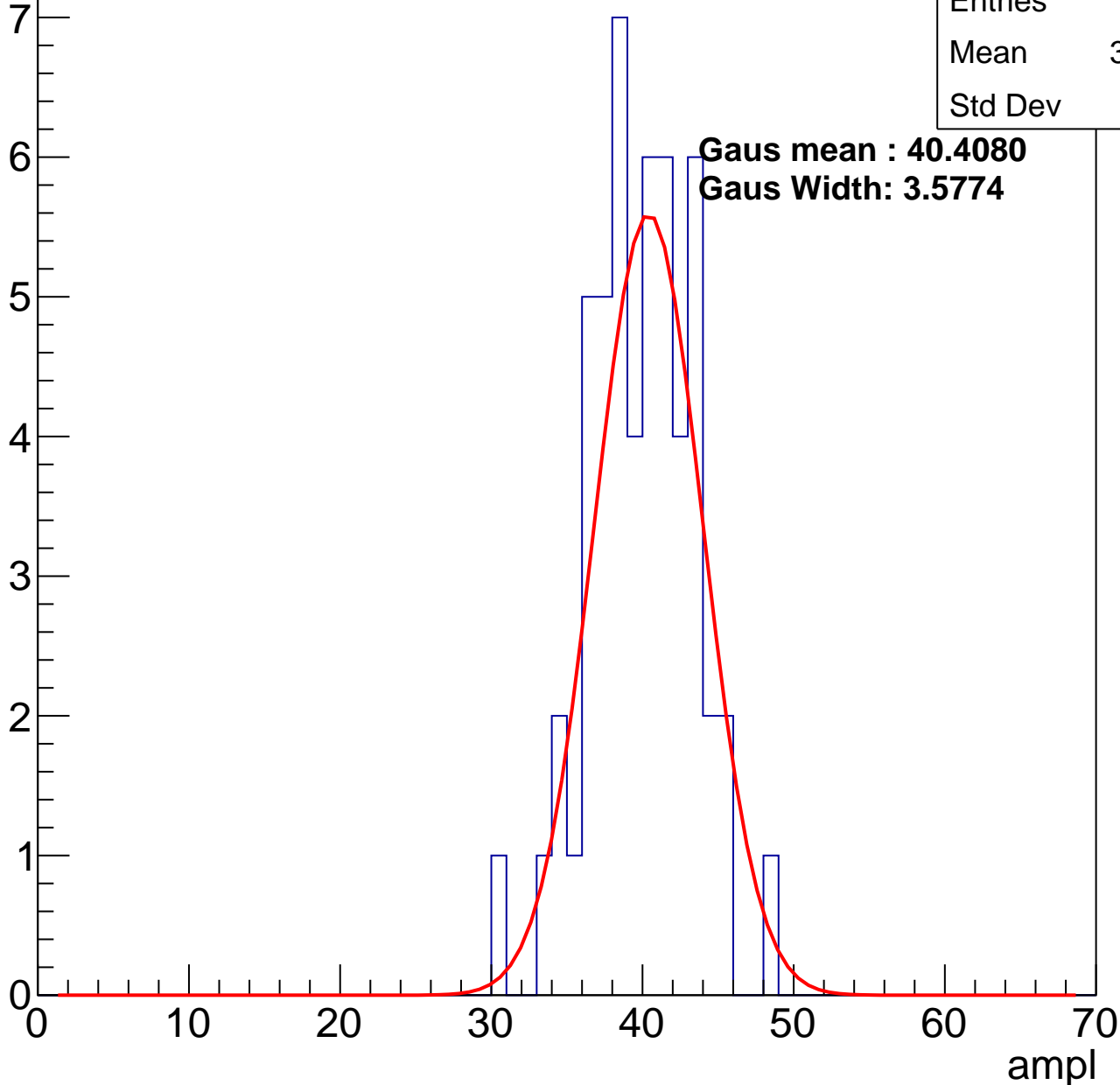
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	53
Mean	39.45
Std Dev	3.39

**Gaus mean : 40.4080**

**Gaus Width: 3.5774**



# B1L003S, U18-ch96, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	77
Mean	45.83
Std Dev	3.304

Entry

10

8

6

4

2

0

0

10

20

30

40

50

60

ampl

0

2

4

6

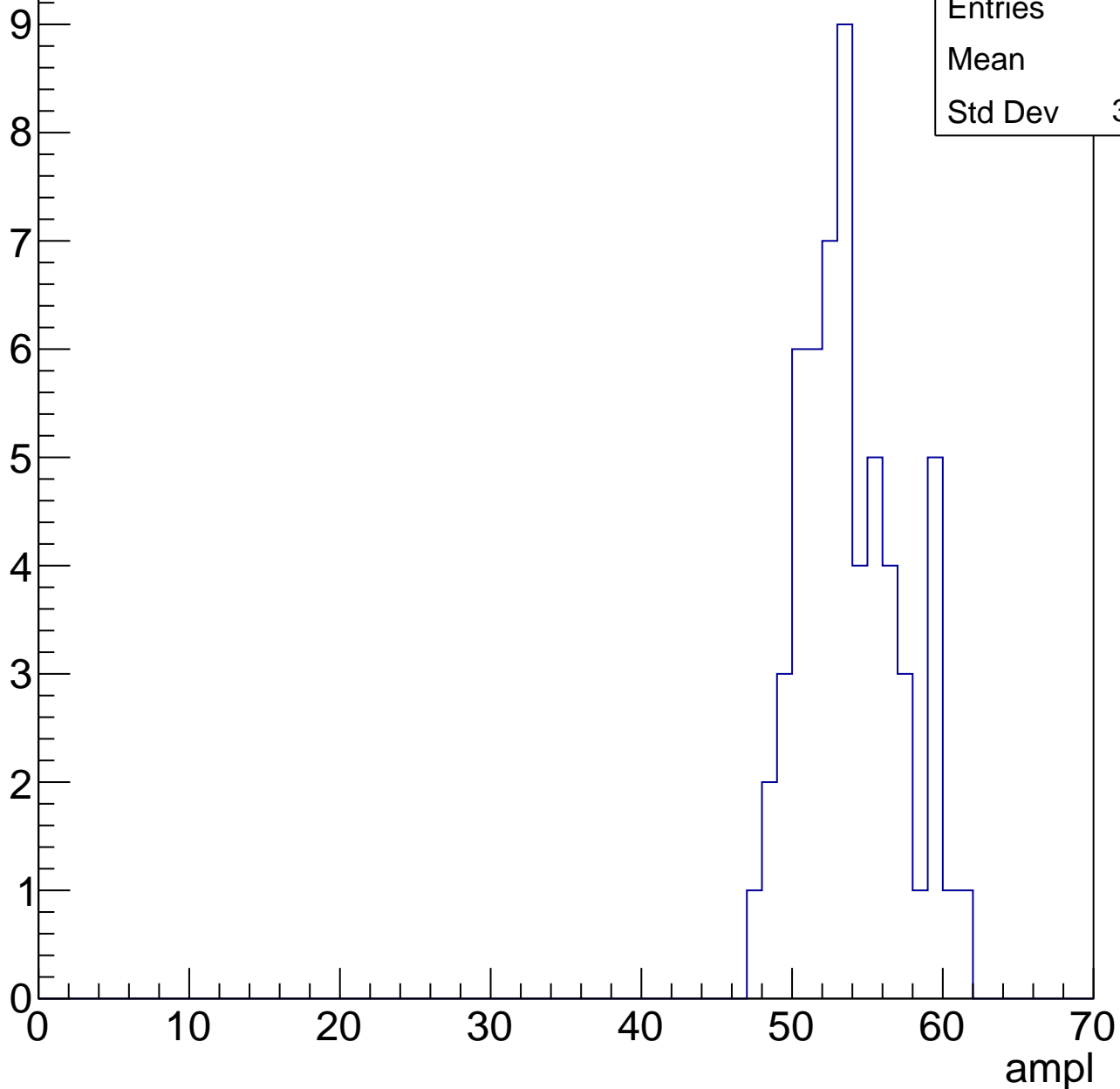
8

10

# B1L003S, U18-ch96, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



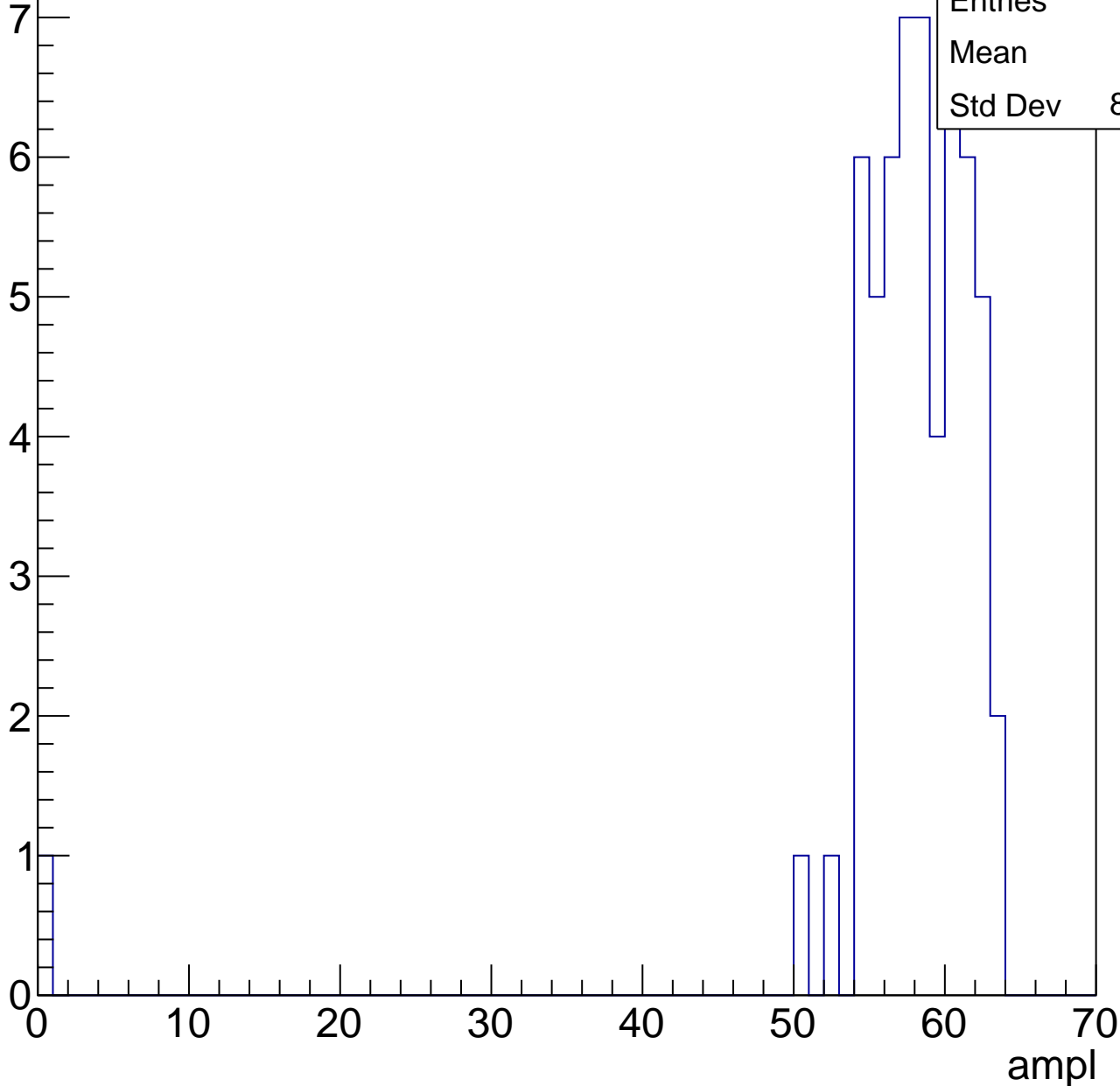
Entries	58
Mean	53.4
Std Dev	3.311

# B1L003S, U18-ch96, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	58
Mean	56.9
Std Dev	8.074

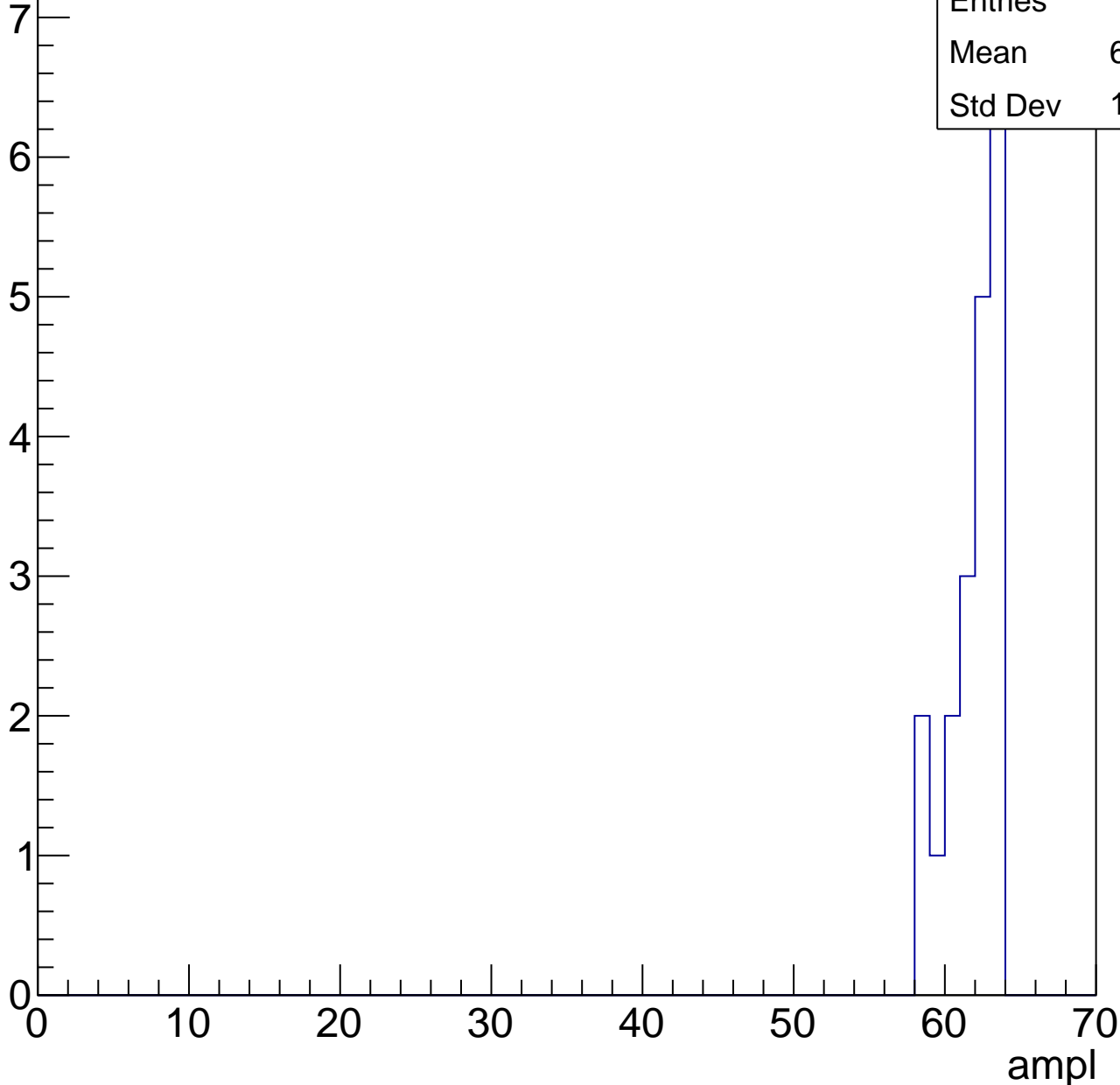


# B1L003S, U18-ch96, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	20
Mean	61.45
Std Dev	1.627

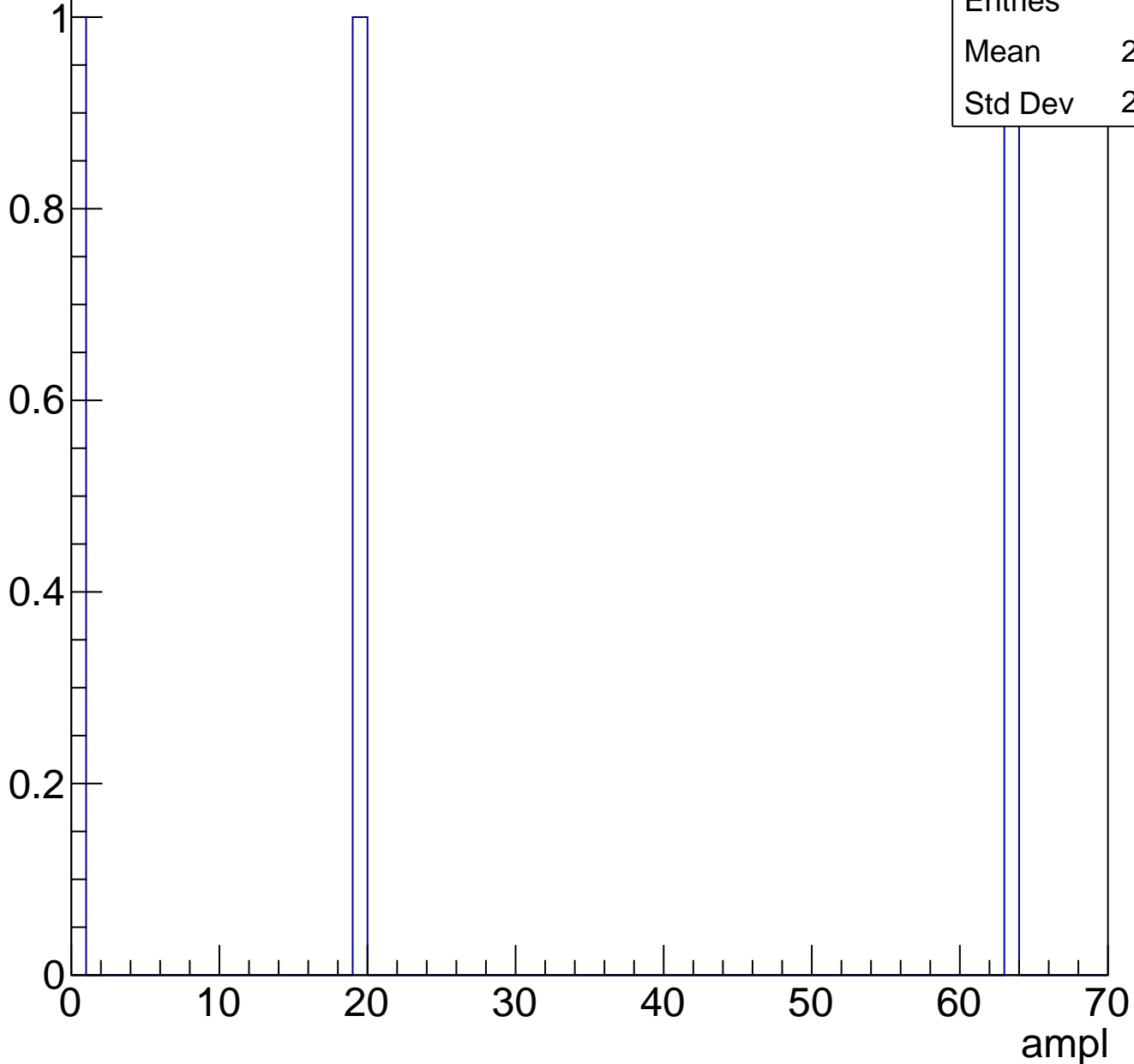




# B1L003S, U18-ch96, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	3
Mean	27.33
Std Dev	26.39

# B1L003S, U18-ch97, adc0

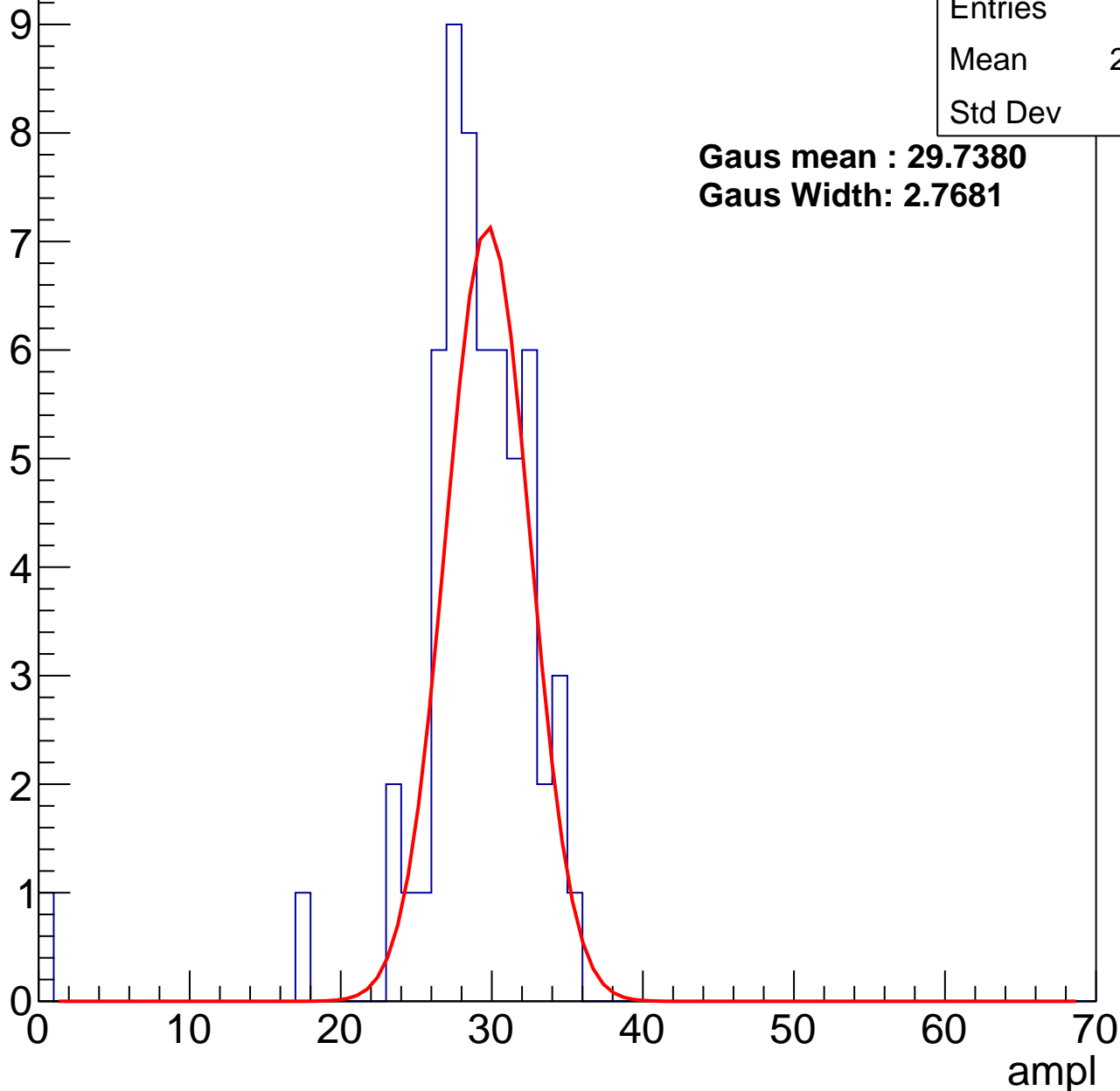
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	58
Mean	28.26
Std Dev	4.89

**Gaus mean : 29.7380**

**Gaus Width: 2.7681**



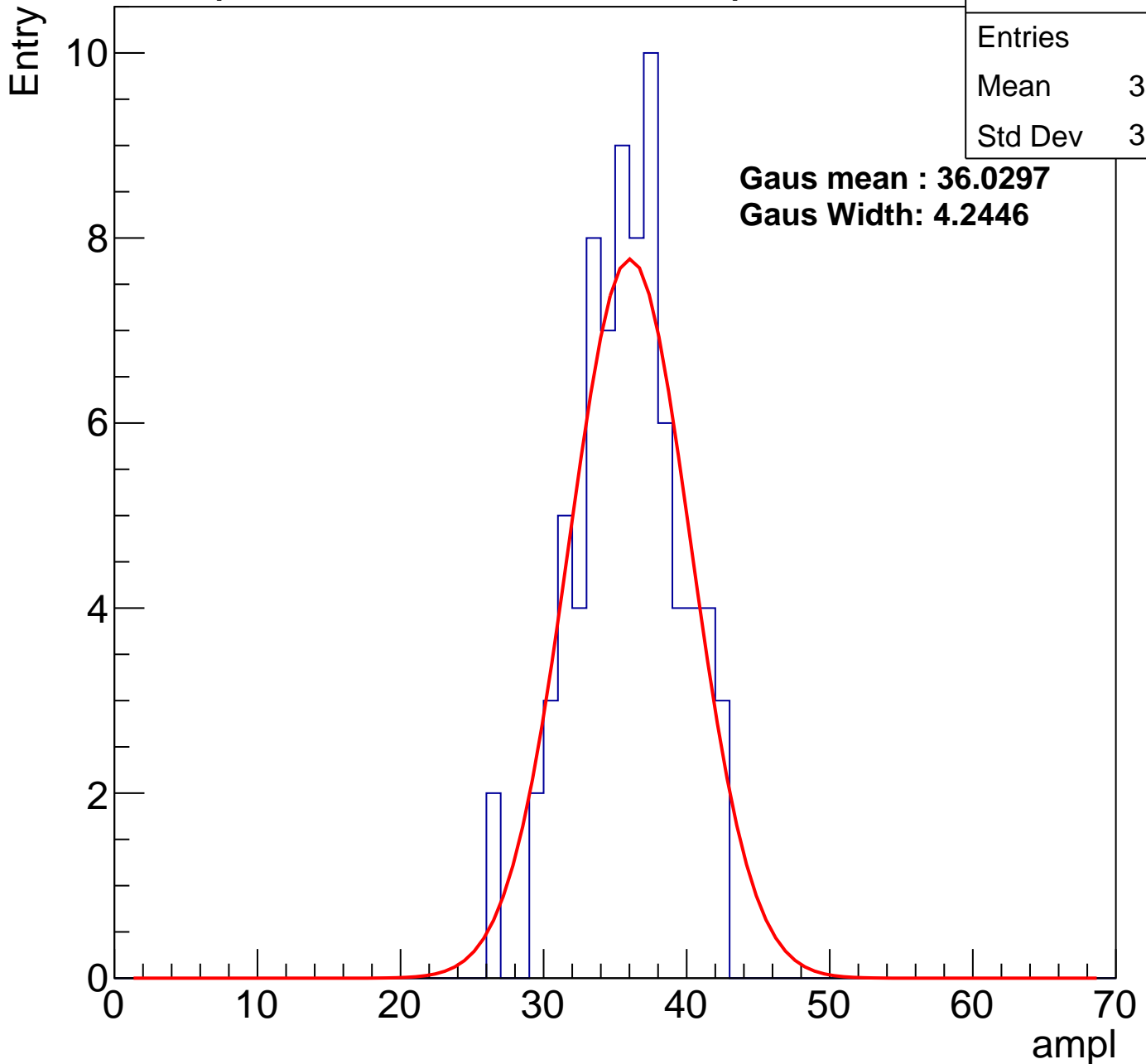
# B1L003S, U18-ch97, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	79
Mean	35.34
Std Dev	3.579

**Gaus mean : 36.0297**

**Gaus Width: 4.2446**



# B1L003S, U18-ch97, adc2

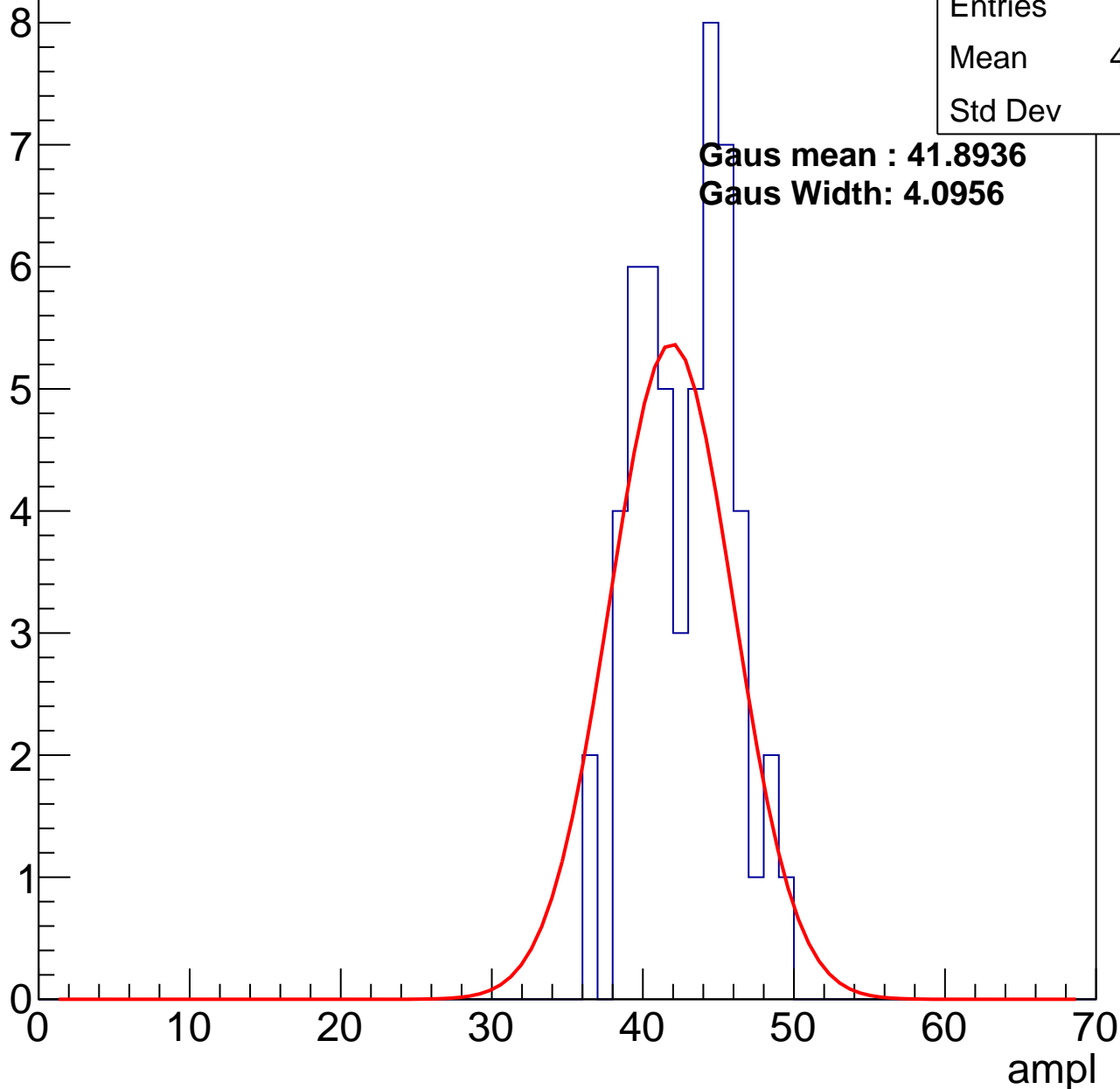
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	54
Mean	42.35
Std Dev	3.11

**Gaus mean : 41.8936**

**Gaus Width: 4.0956**

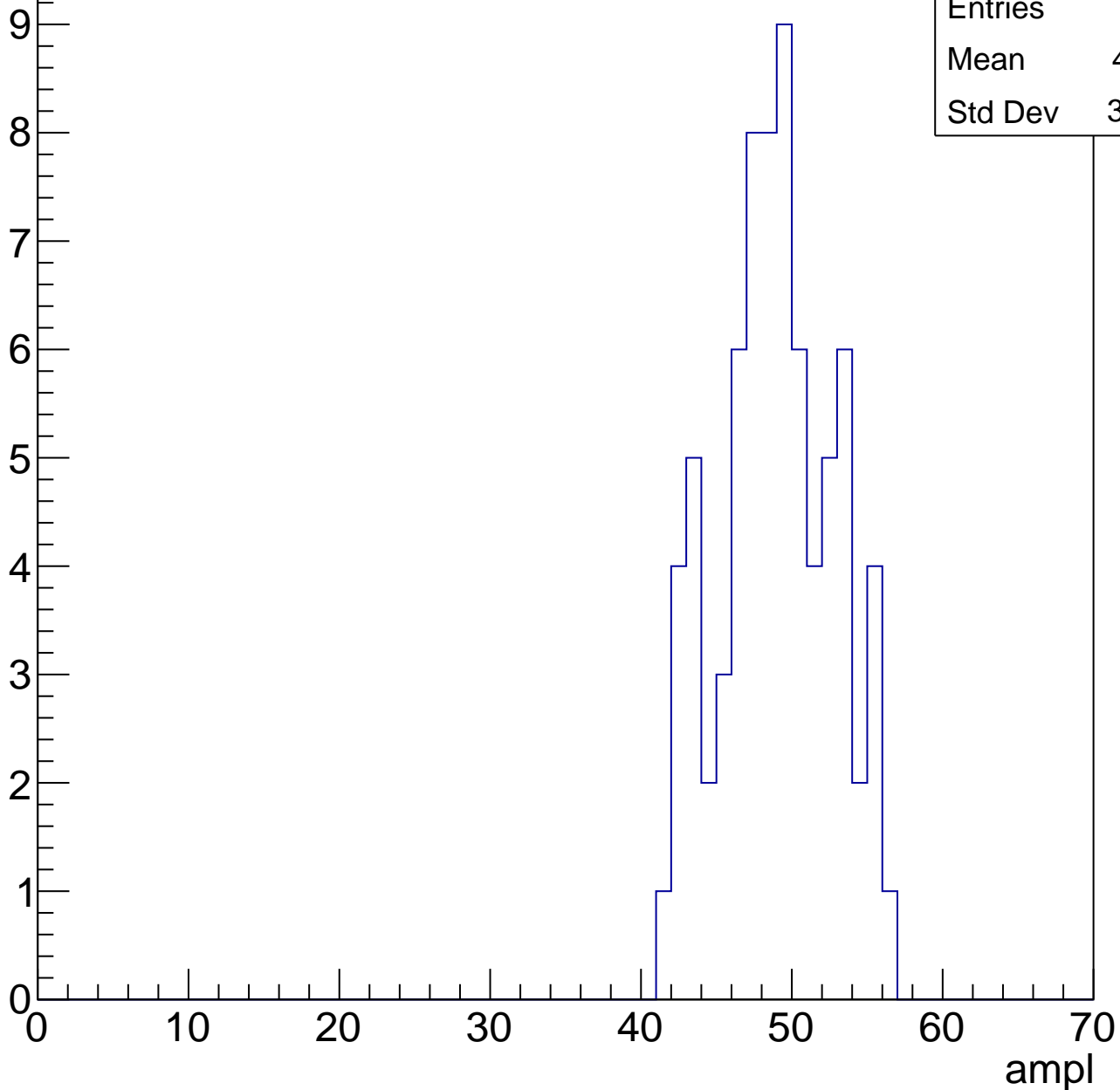


# B1L003S, U18-ch97, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

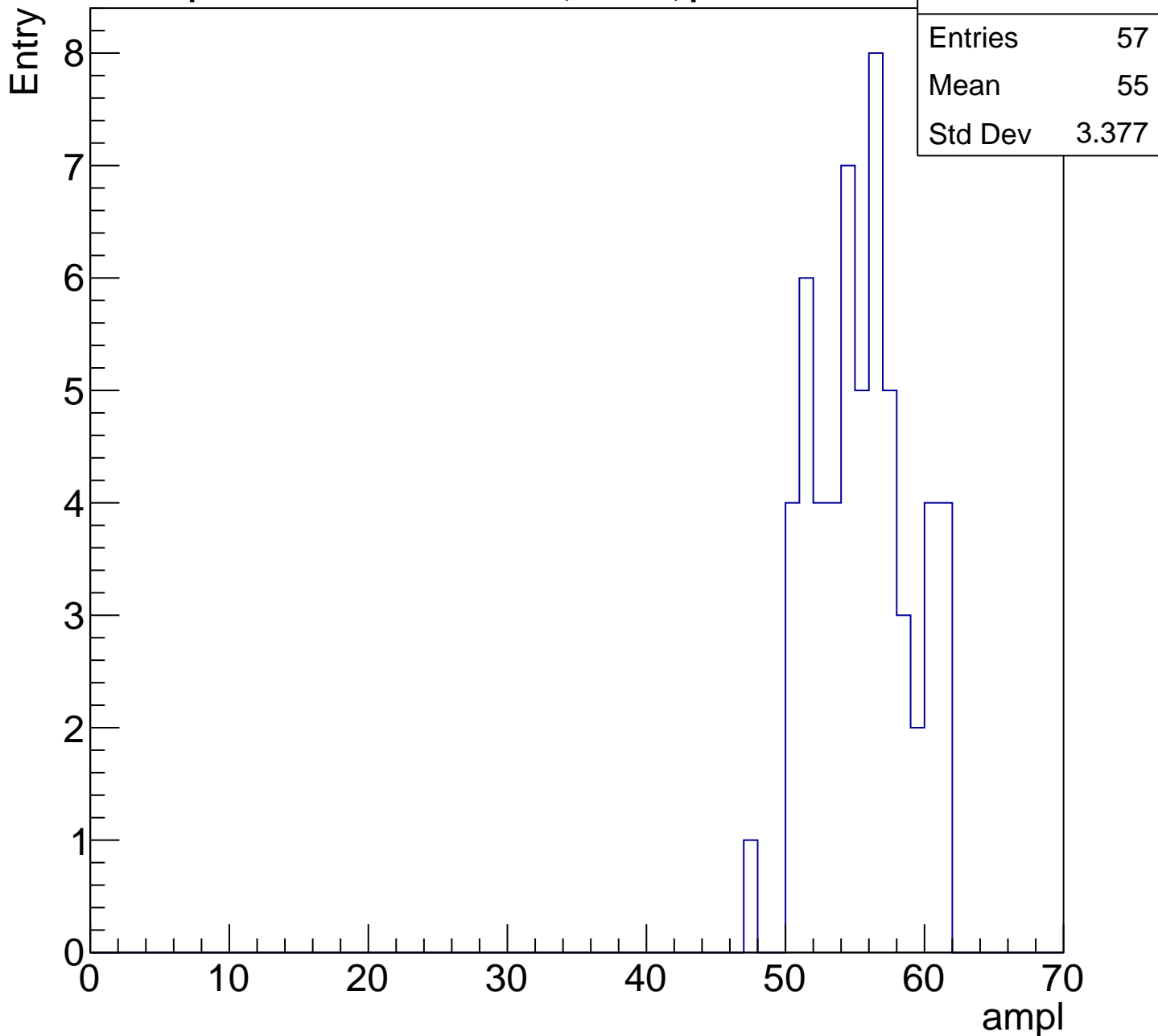
Entry

Entries	74
Mean	48.51
Std Dev	3.714



# B1L003S, U18-ch97, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

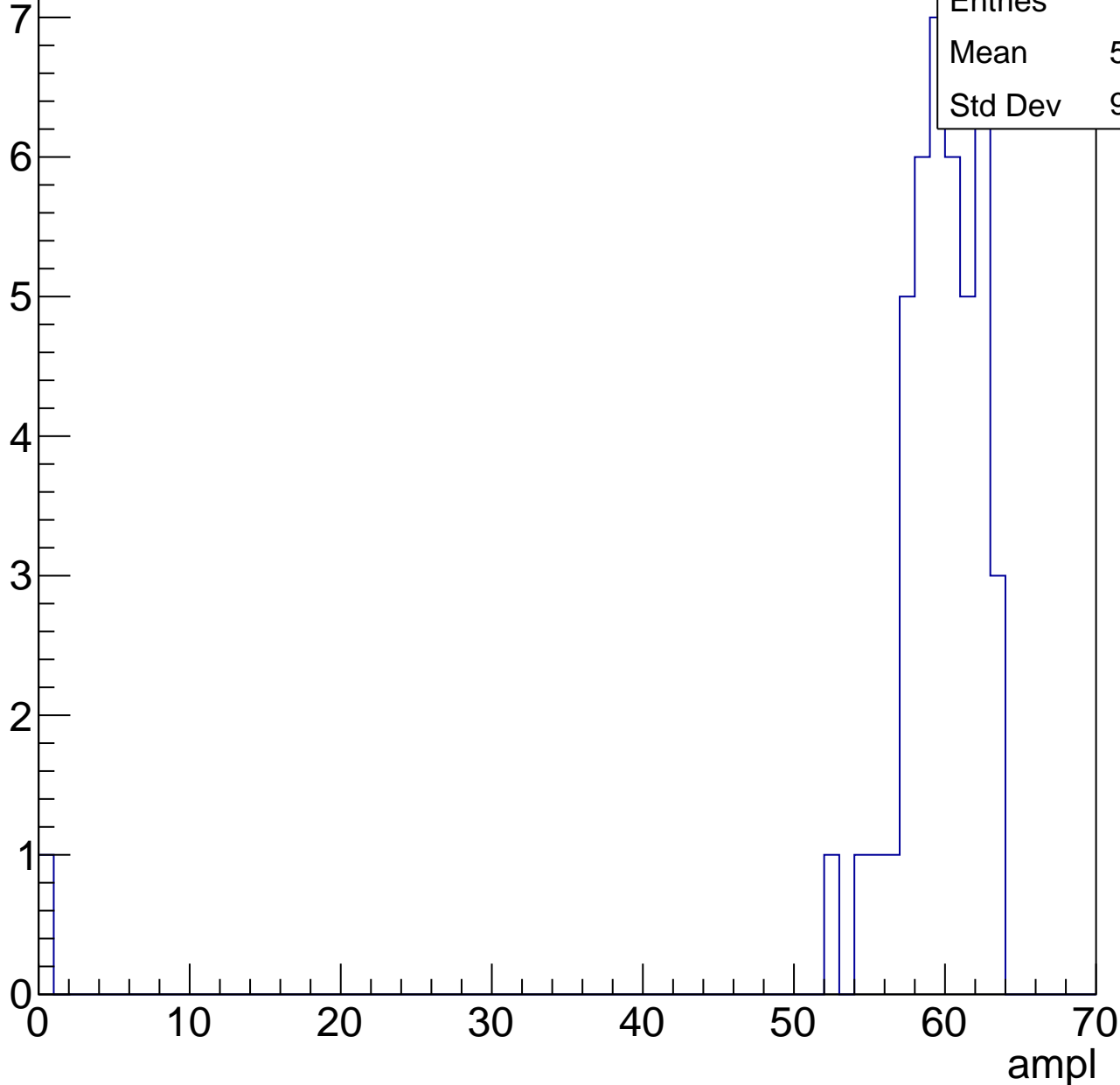


# B1L003S, U18-ch97, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	44
Mean	57.98
Std Dev	9.166

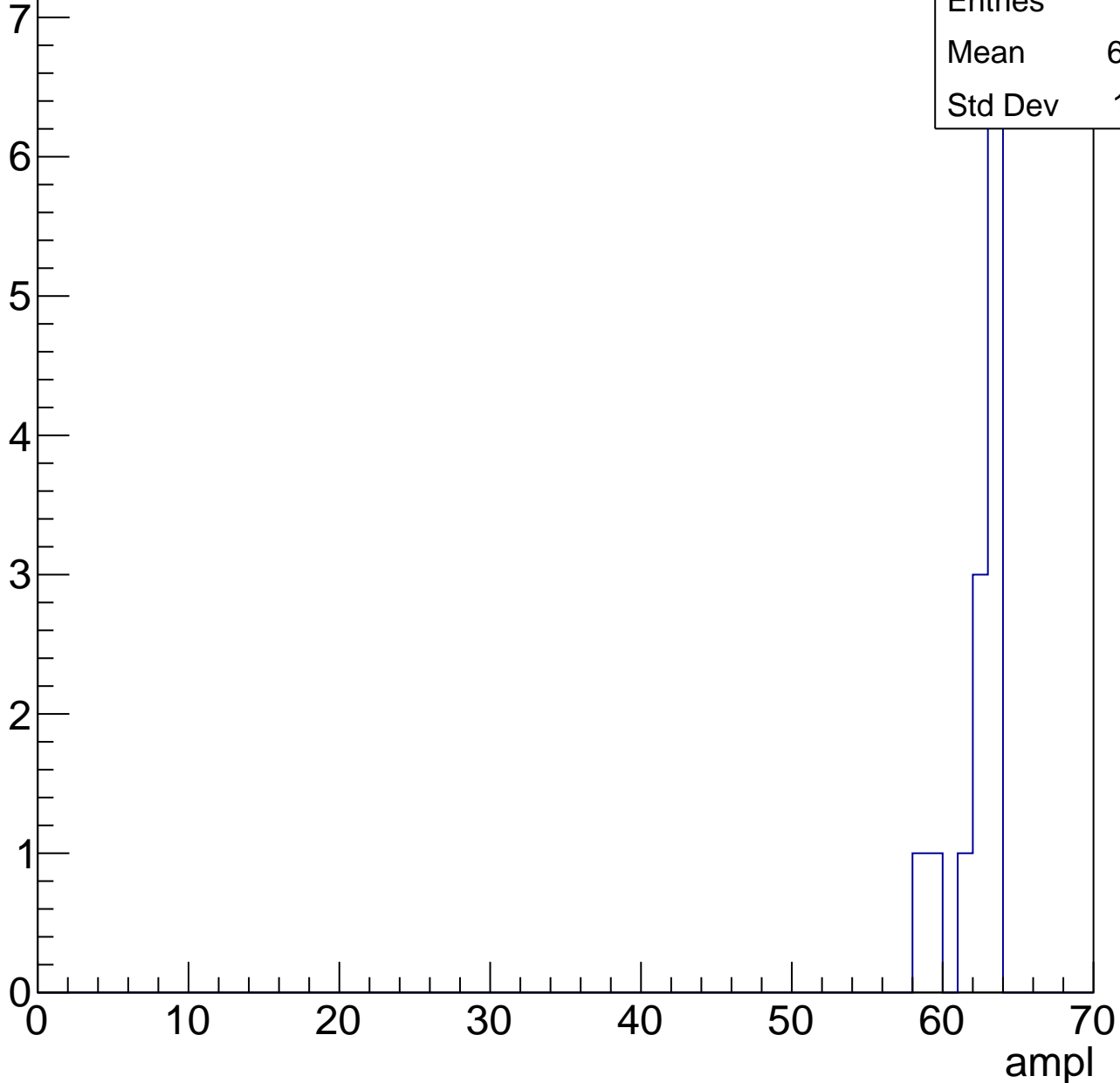


# B1L003S, U18-ch97, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	13
Mean	61.92
Std Dev	1.591





# B1L003S, U18-ch97, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

1

0.8

0.6

0.4

0.2

0

0

10

20

30

40

50

60

70

ampl

Entries

0

Mean

0

Std Dev

0

# B1L003S, U18-ch98, adc0

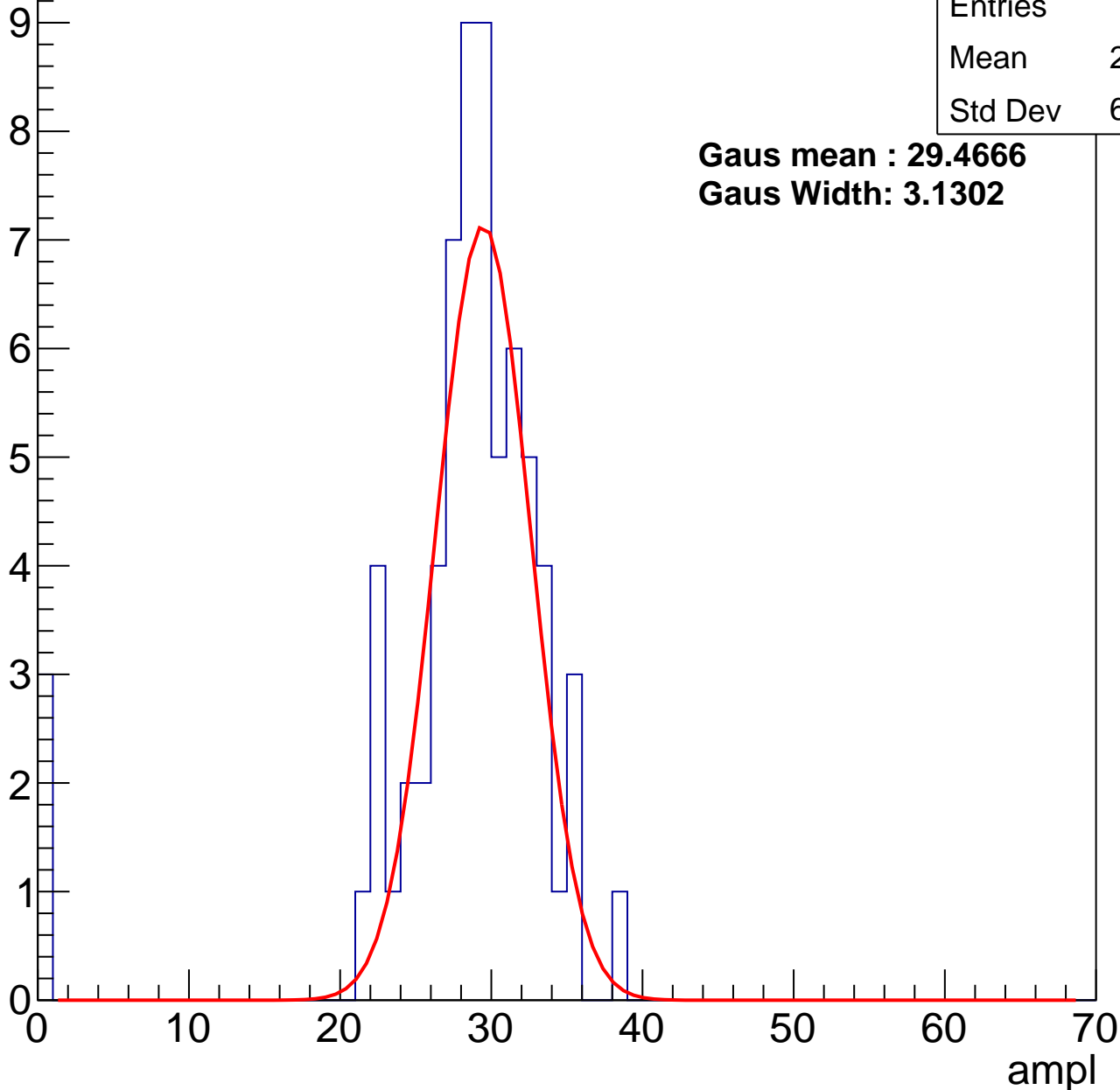
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	67
Mean	27.48
Std Dev	6.879

**Gaus mean : 29.4666**

**Gaus Width: 3.1302**



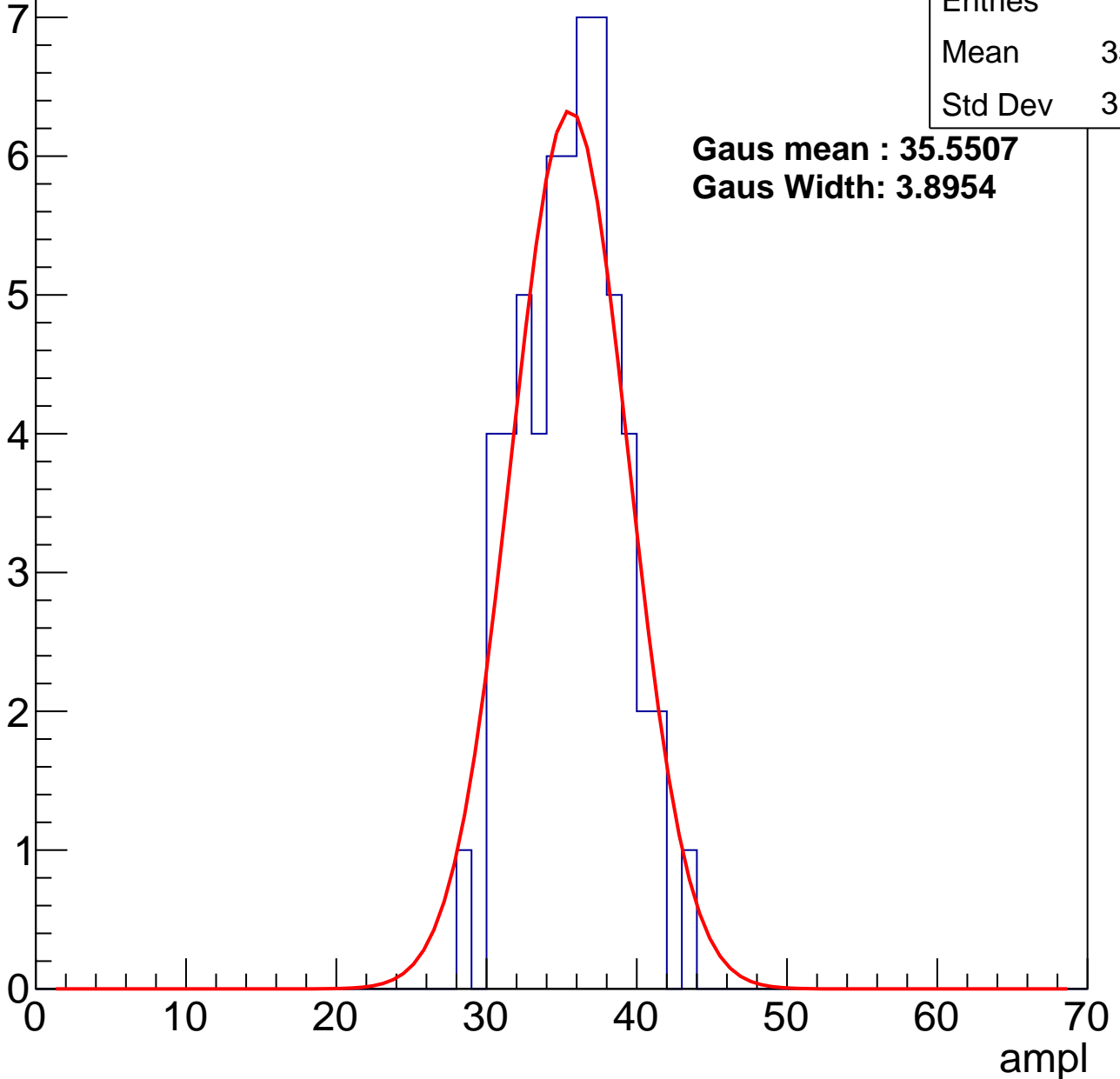
# B1L003S, U18-ch98, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	58
Mean	35.17
Std Dev	3.238

**Gaus mean : 35.5507**  
**Gaus Width: 3.8954**



# B1L003S, U18-ch98, adc2

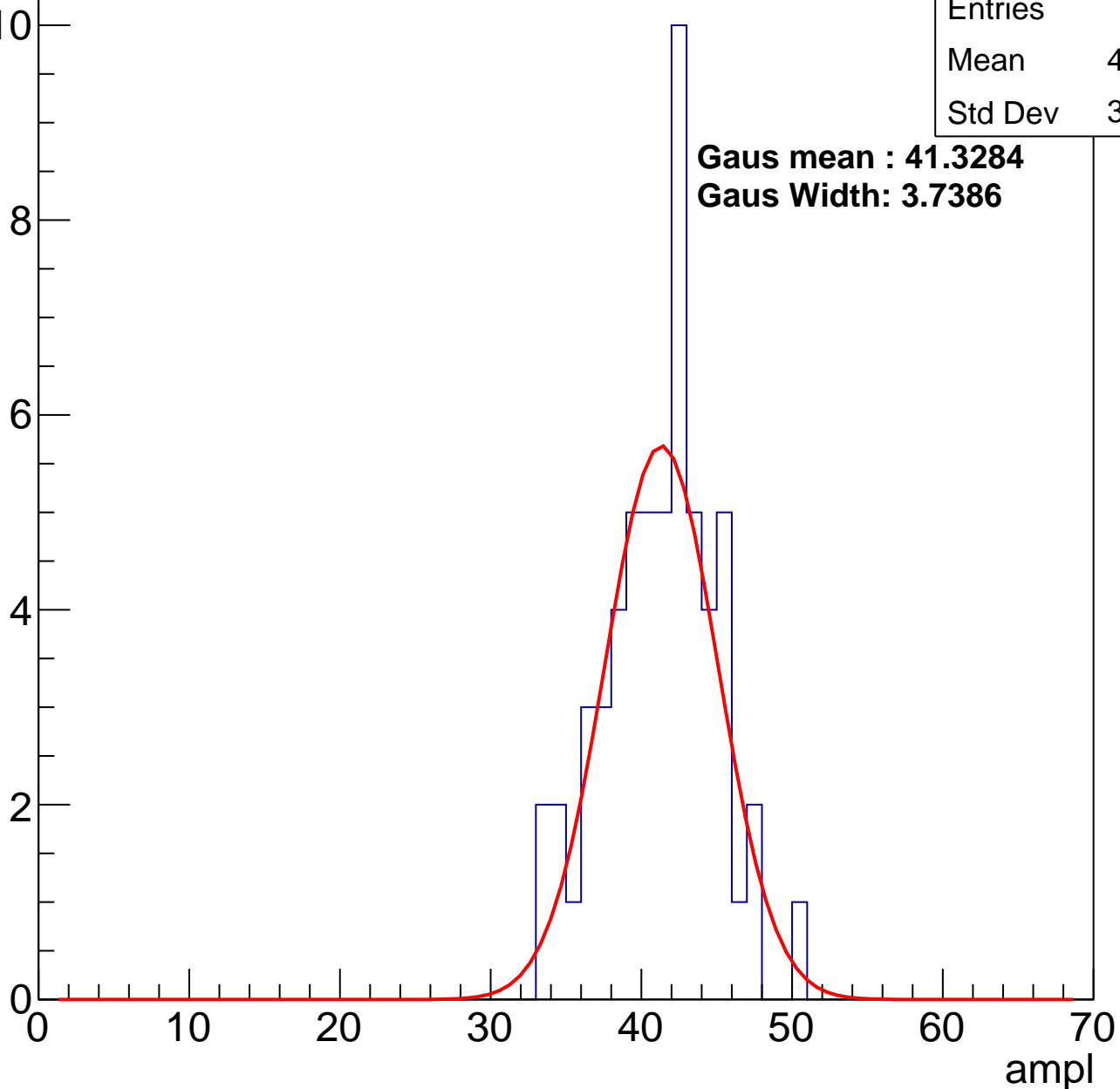
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	58
Mean	40.79
Std Dev	3.638

**Gaus mean : 41.3284**

**Gaus Width: 3.7386**

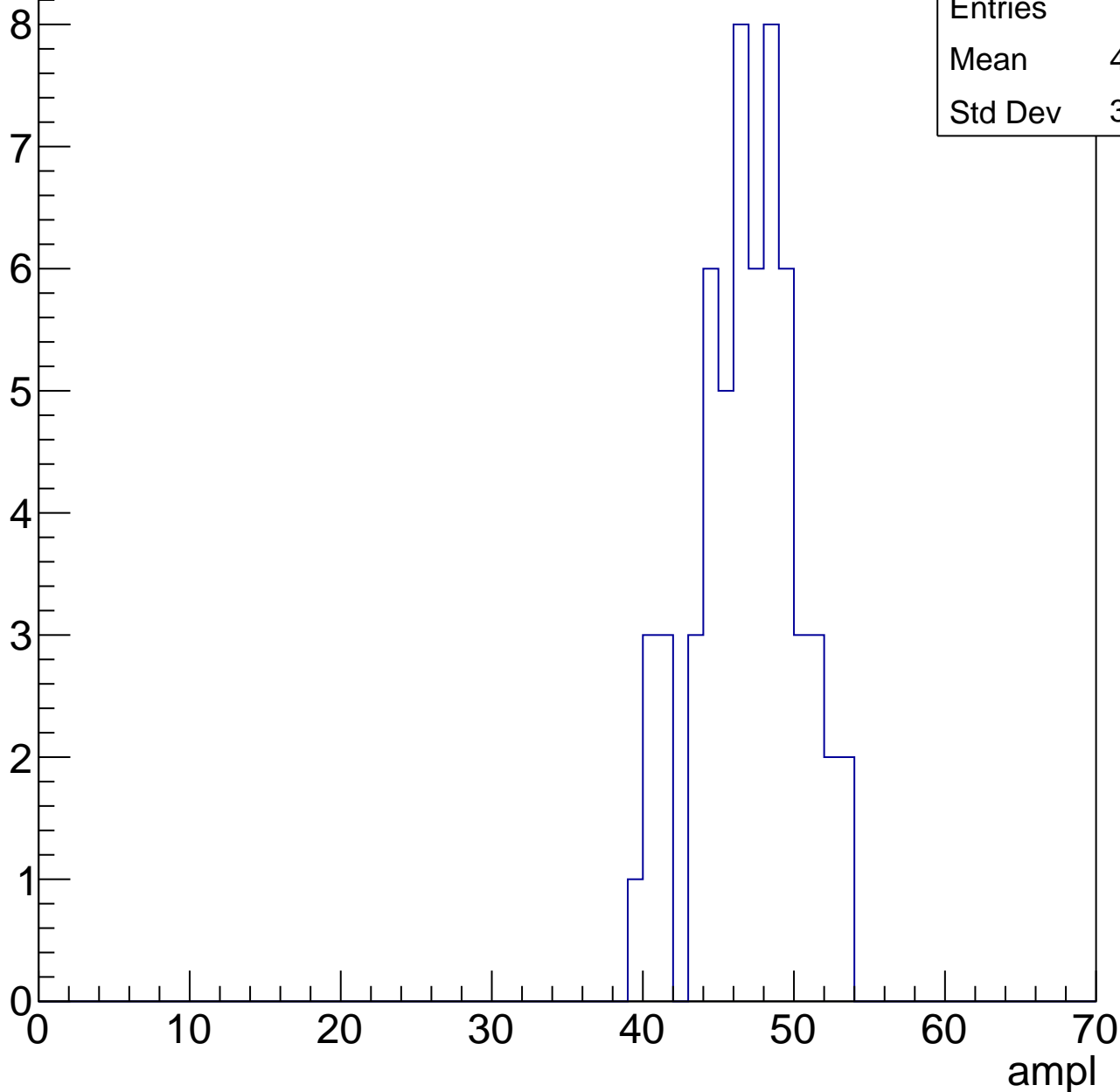


# B1L003S, U18-ch98, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	59
Mean	46.46
Std Dev	3.346

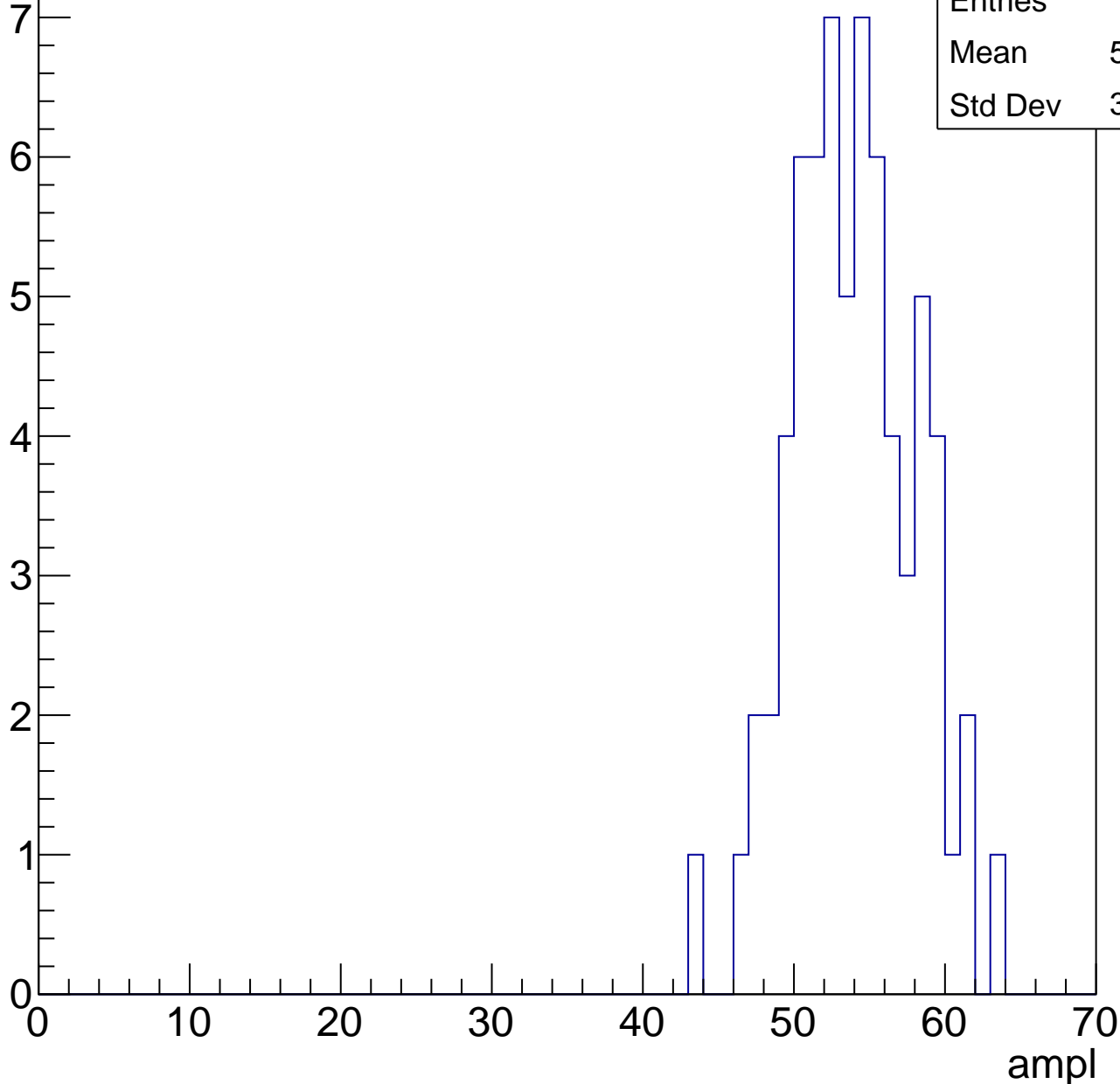


# B1L003S, U18-ch98, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

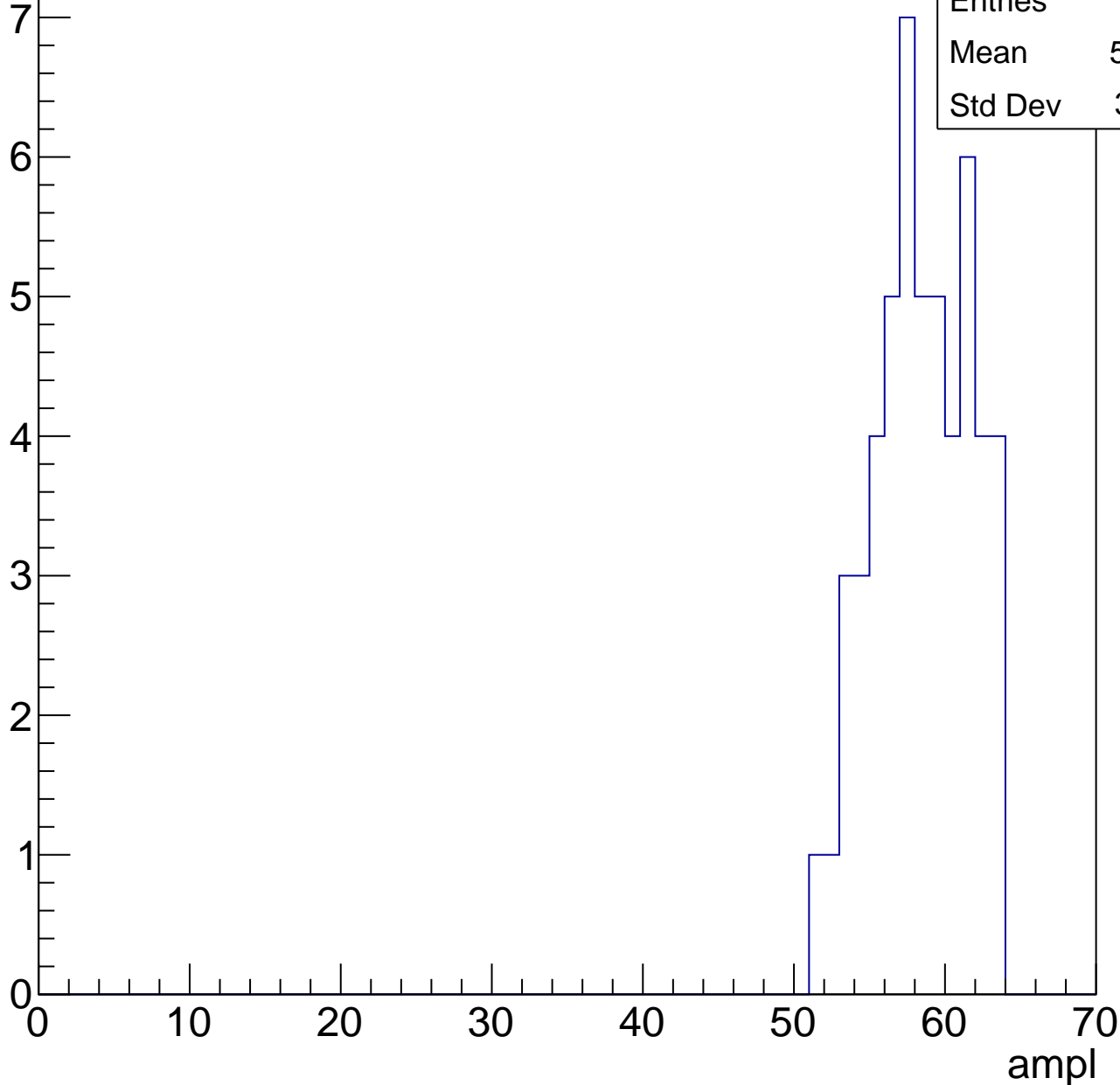
Entries	67
Mean	53.49
Std Dev	3.986



# B1L003S, U18-ch98, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

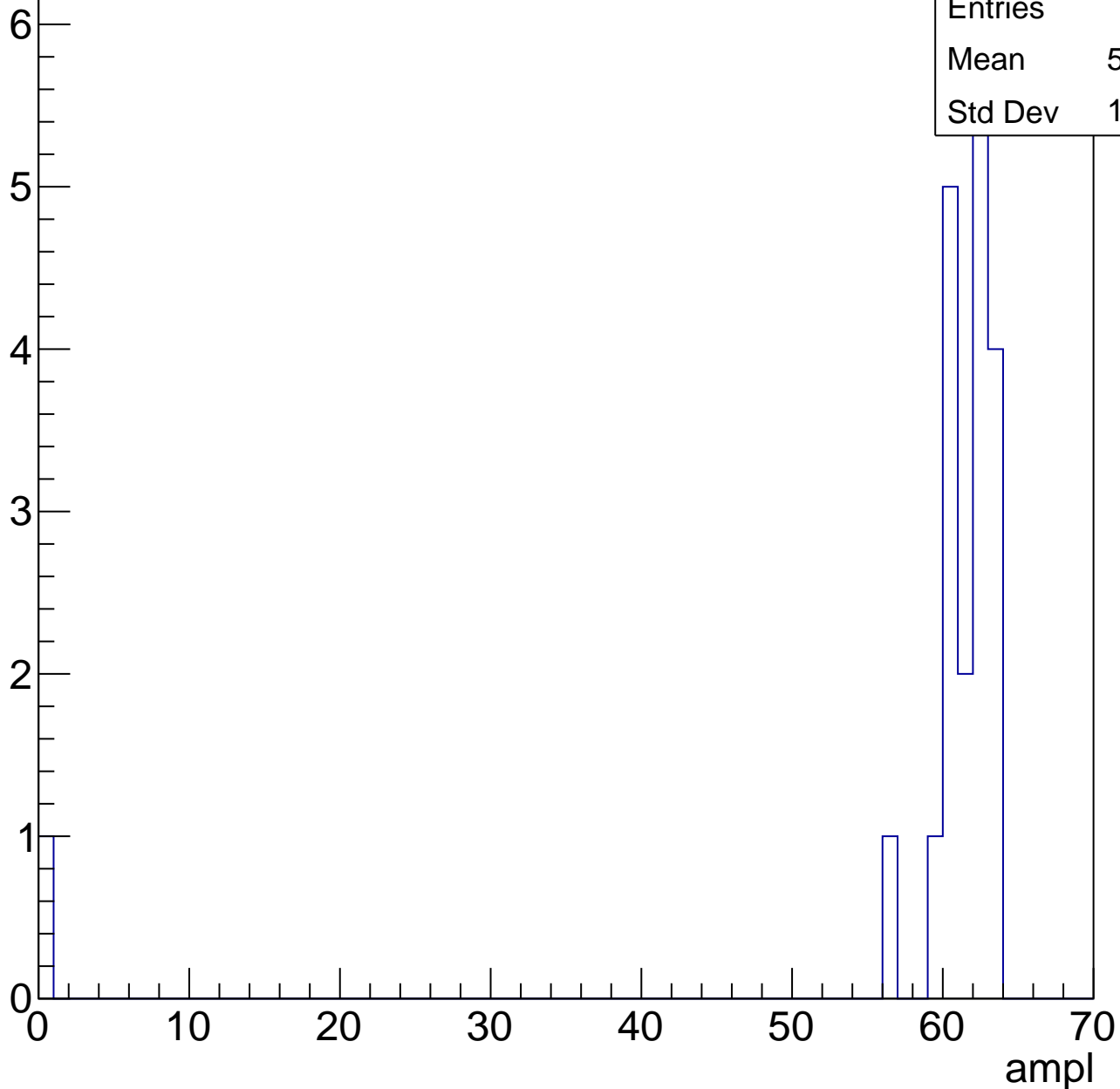


# B1L003S, U18-ch98, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	20
Mean	58.05
Std Dev	13.42

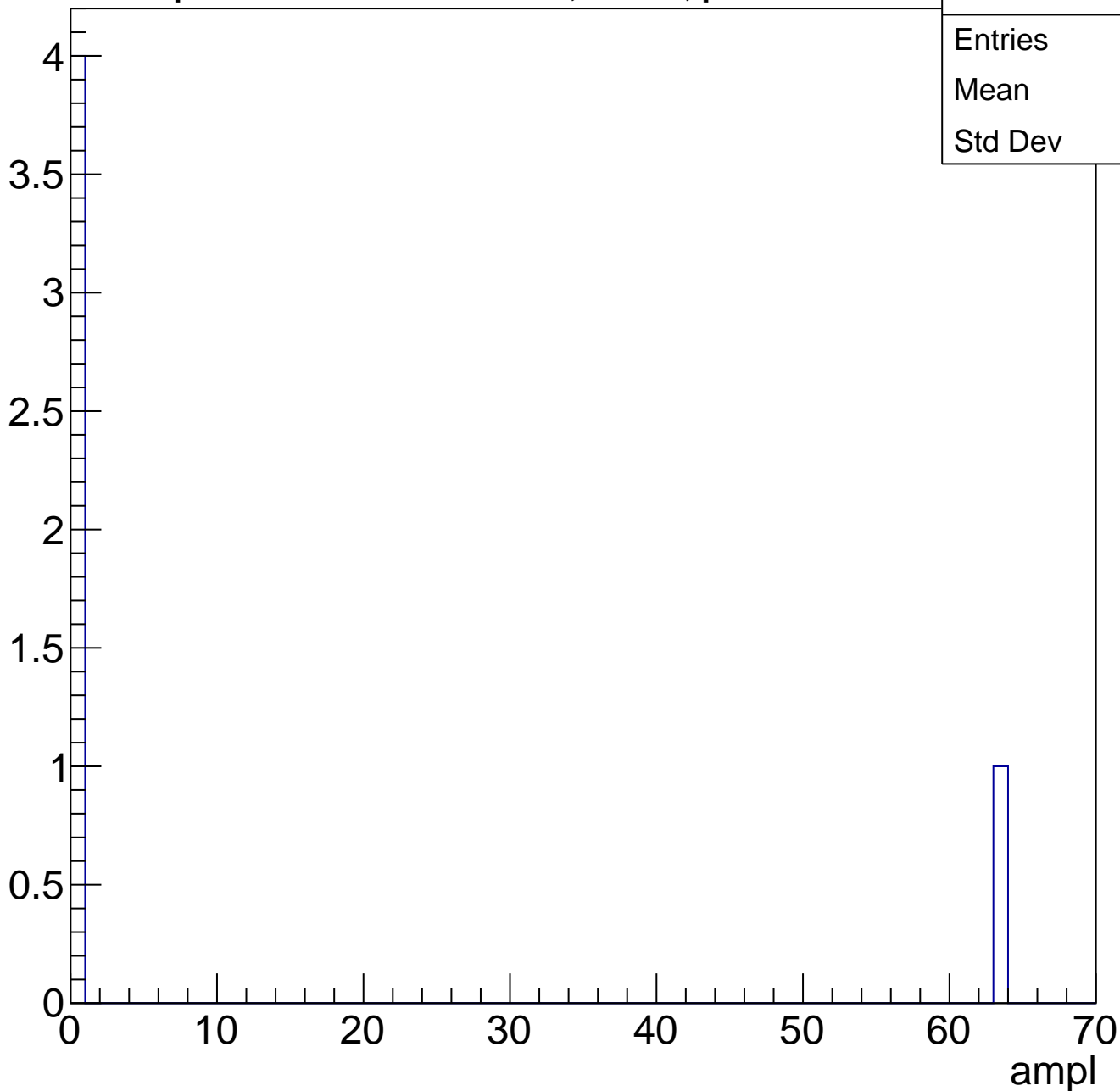




# B1L003S, U18-ch98, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U18-ch99, adc0

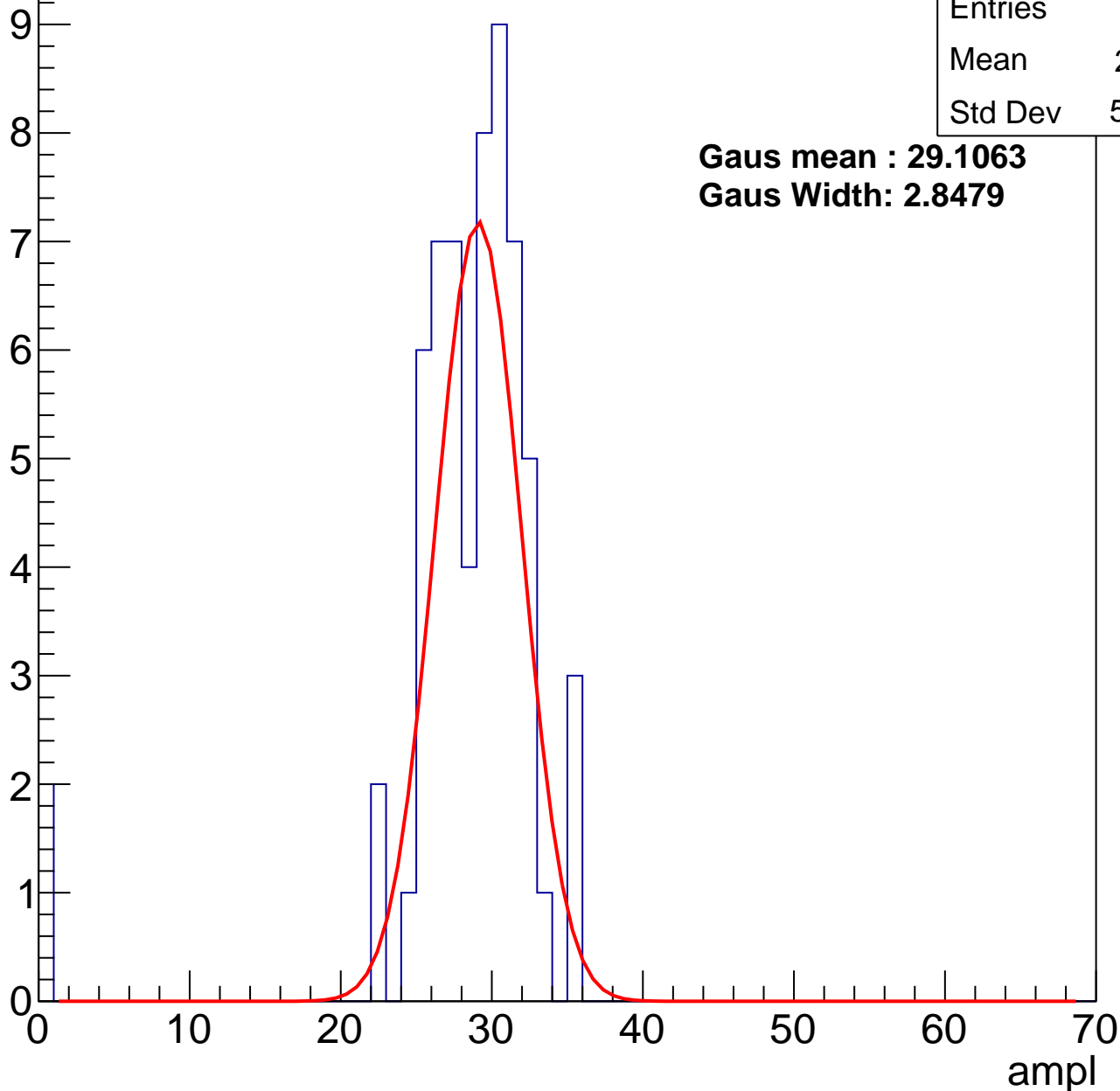
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	62
Mean	27.71
Std Dev	5.818

**Gaus mean : 29.1063**

**Gaus Width: 2.8479**

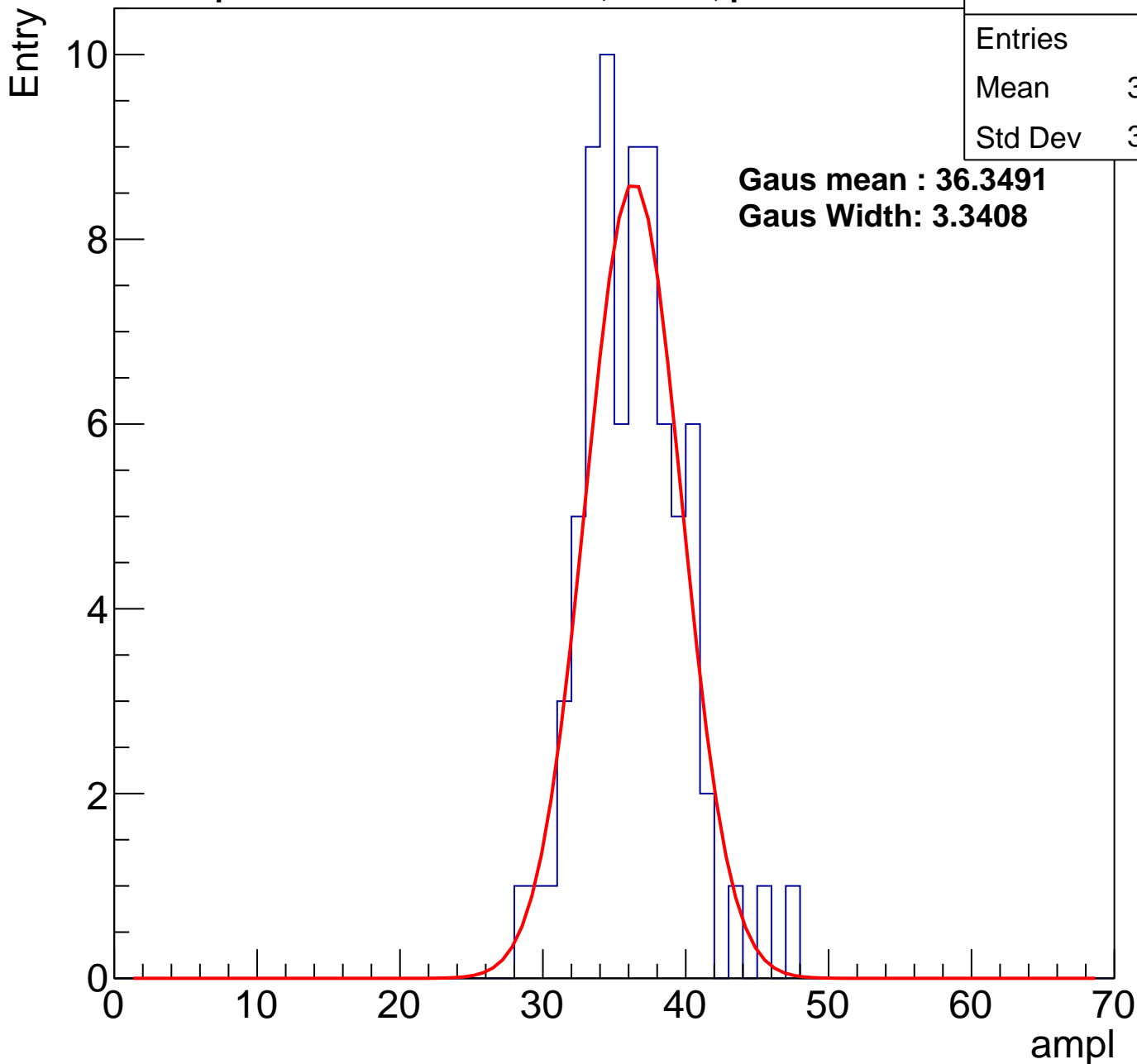


# B1L003S, U18-ch99, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	76
Mean	35.84
Std Dev	3.449

**Gaus mean : 36.3491**  
**Gaus Width: 3.3408**



# B1L003S, U18-ch99, adc2

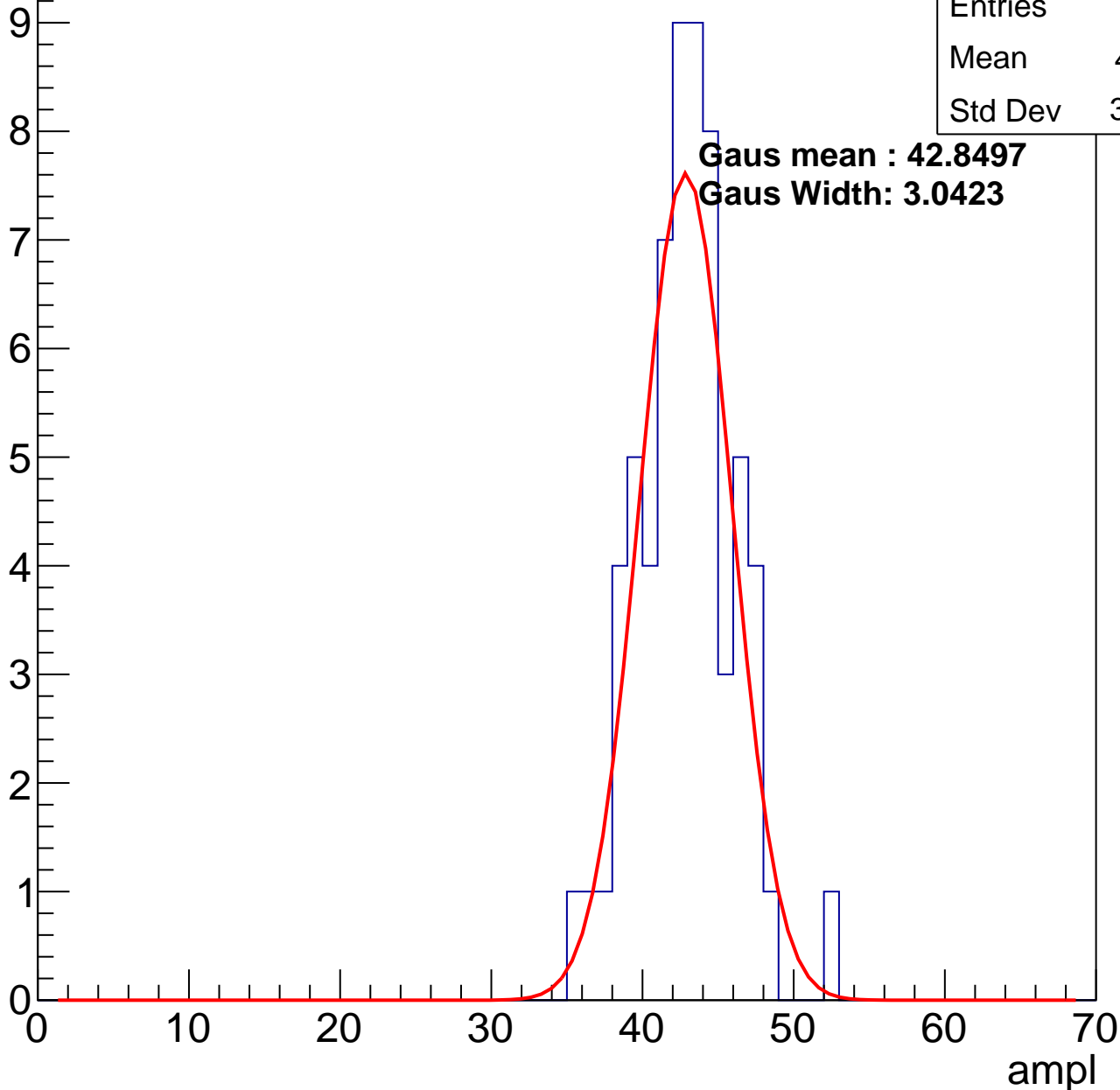
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	63
Mean	42.41
Std Dev	3.125

**Gaus mean : 42.8497**

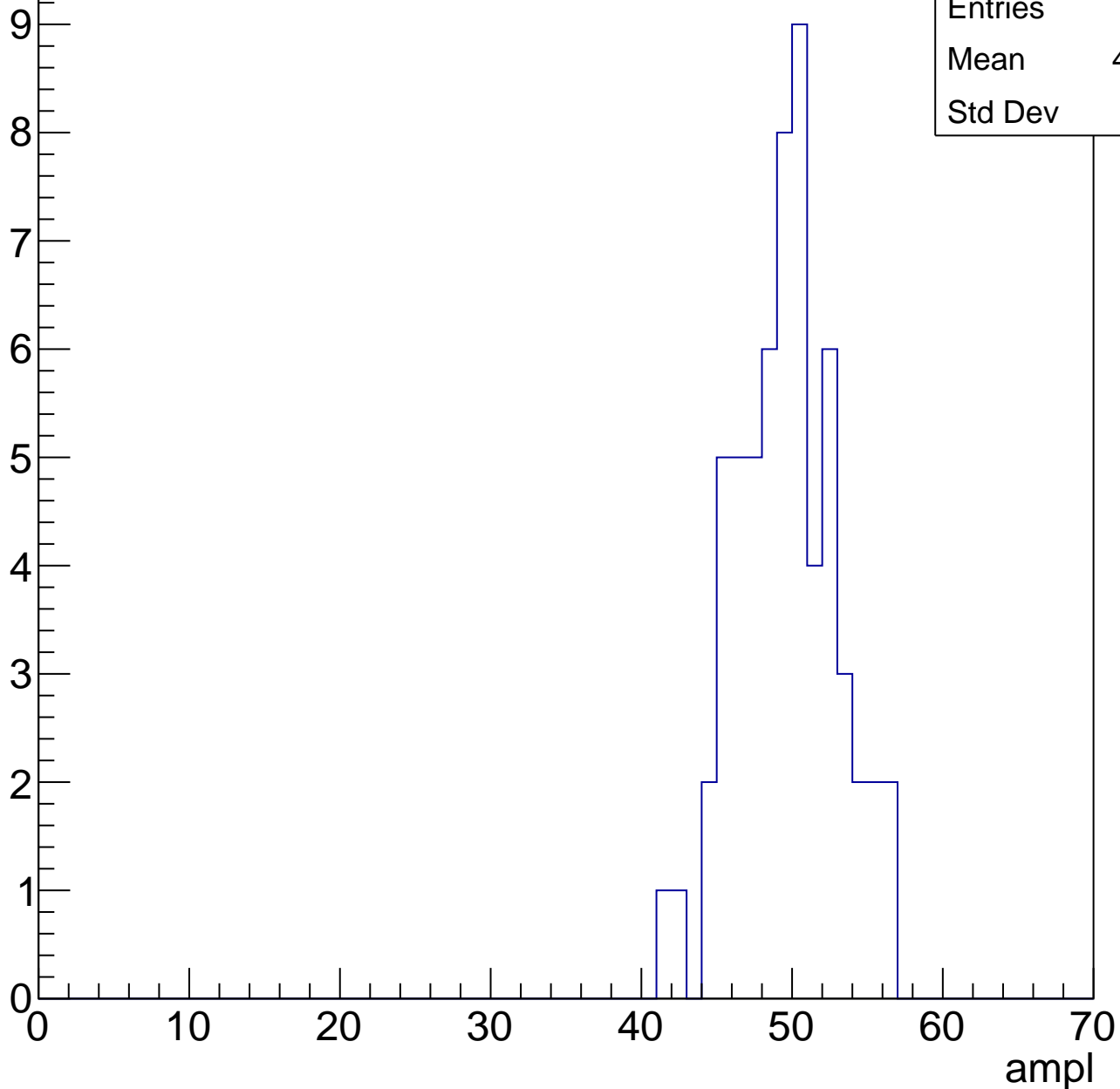
**Gaus Width: 3.0423**



# B1L003S, U18-ch99, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



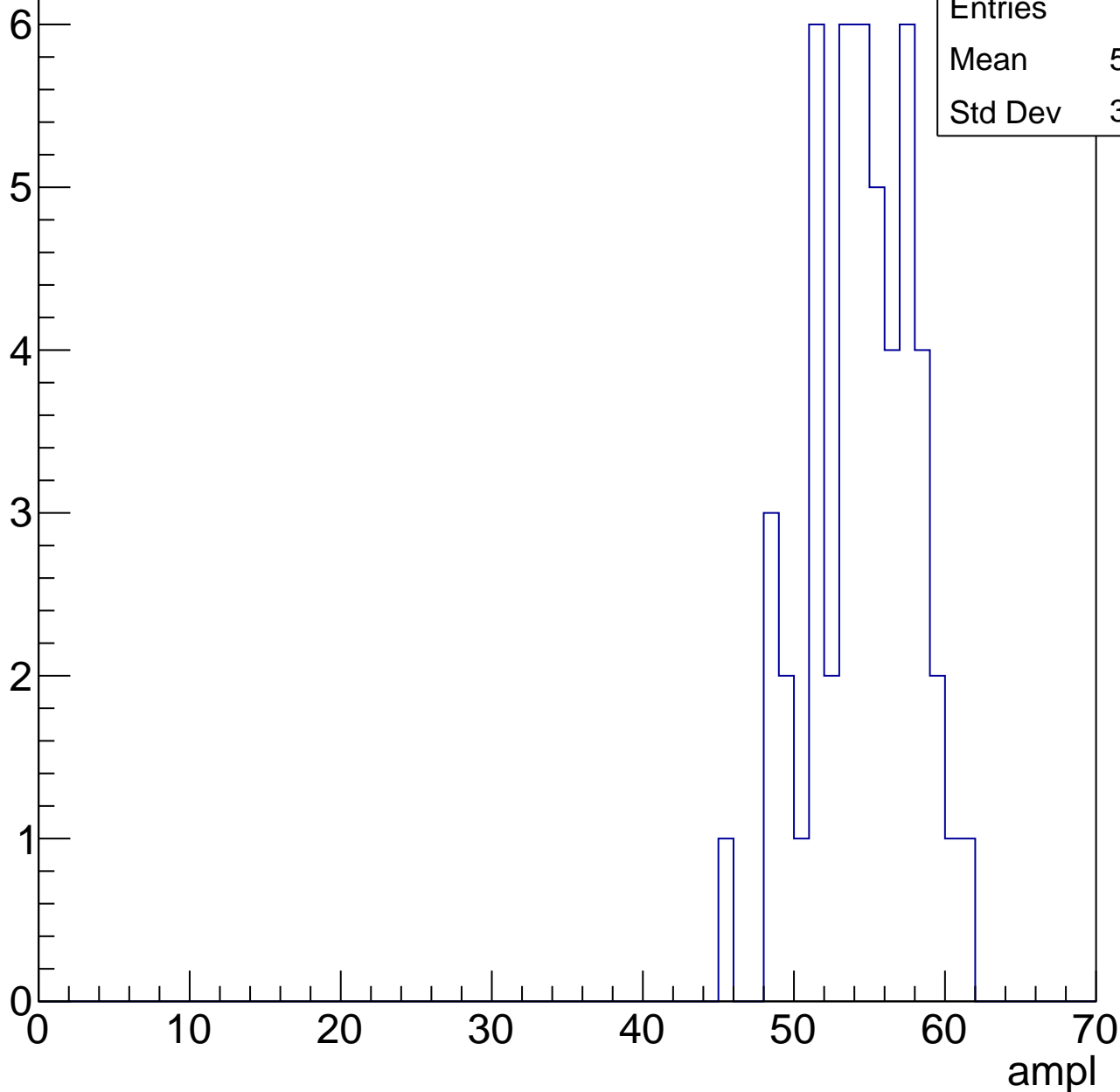
Entries	61
Mean	49.11
Std Dev	3.29

# B1L003S, U18-ch99, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	50
Mean	54.02
Std Dev	3.455

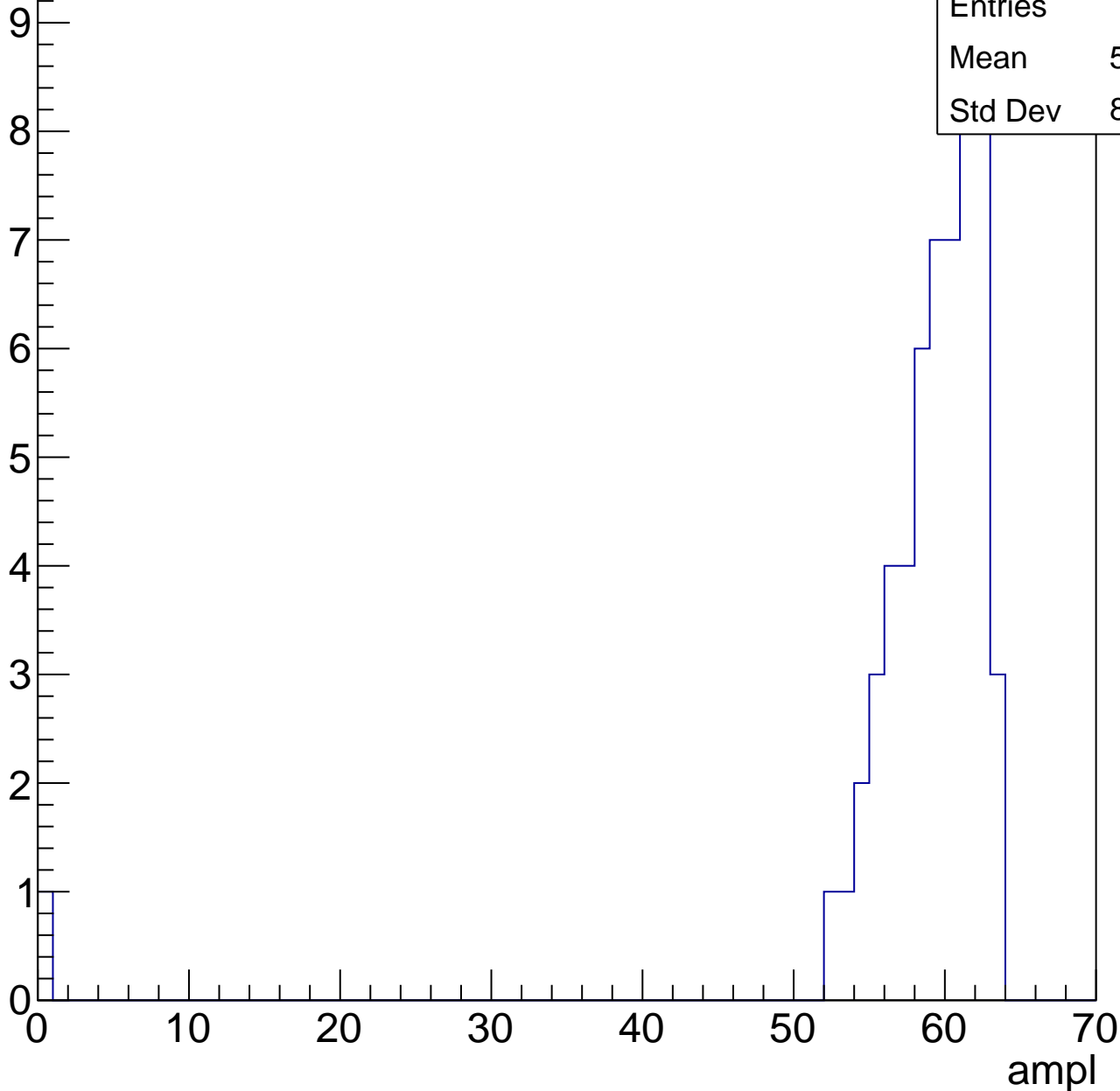


# B1L003S, U18-ch99, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	57
Mean	58.02
Std Dev	8.207

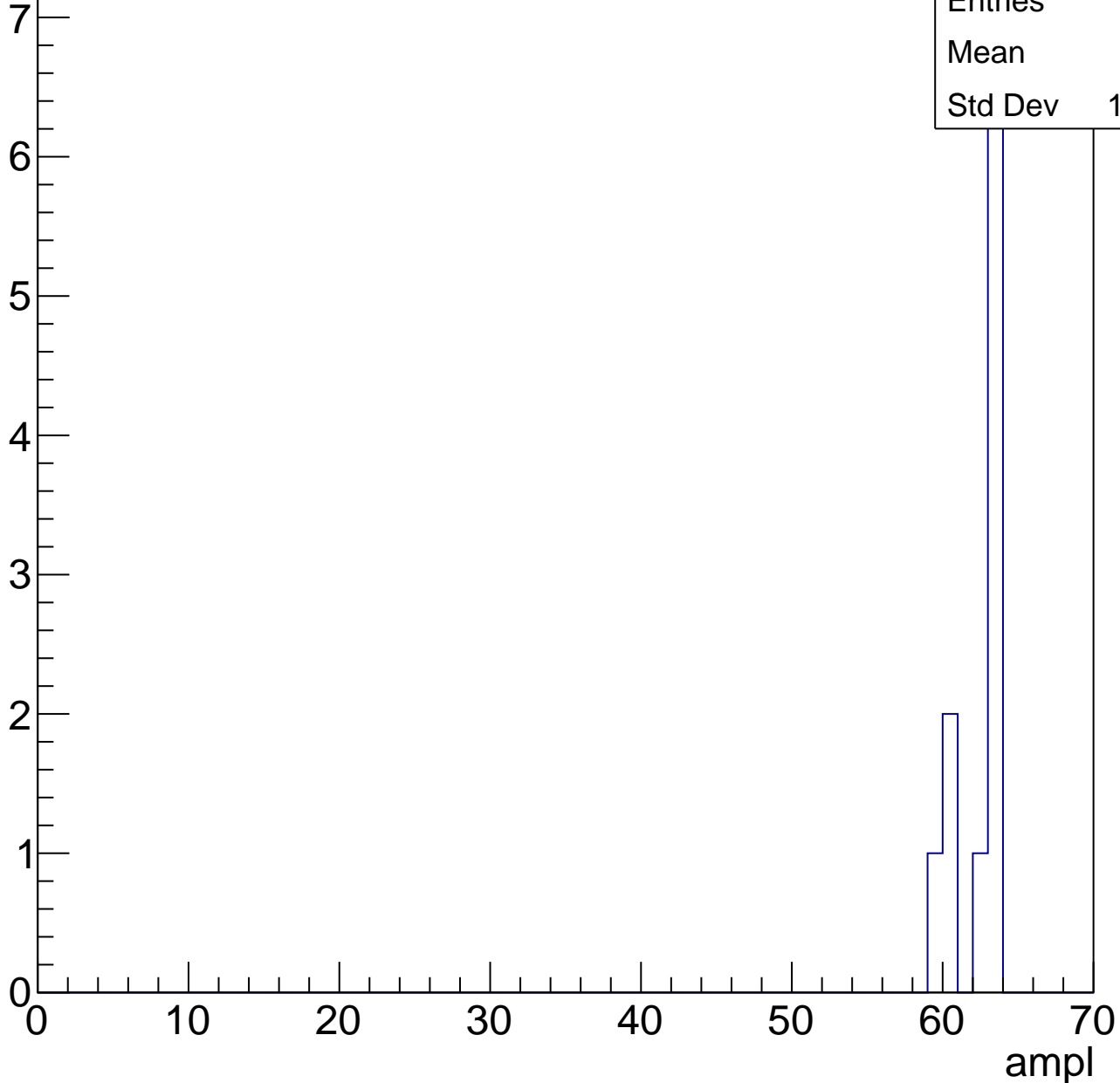


# B1L003S, U18-ch99, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	11
Mean	62
Std Dev	1.477





# B1L003S, U18-ch99, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U18-ch100, adc0

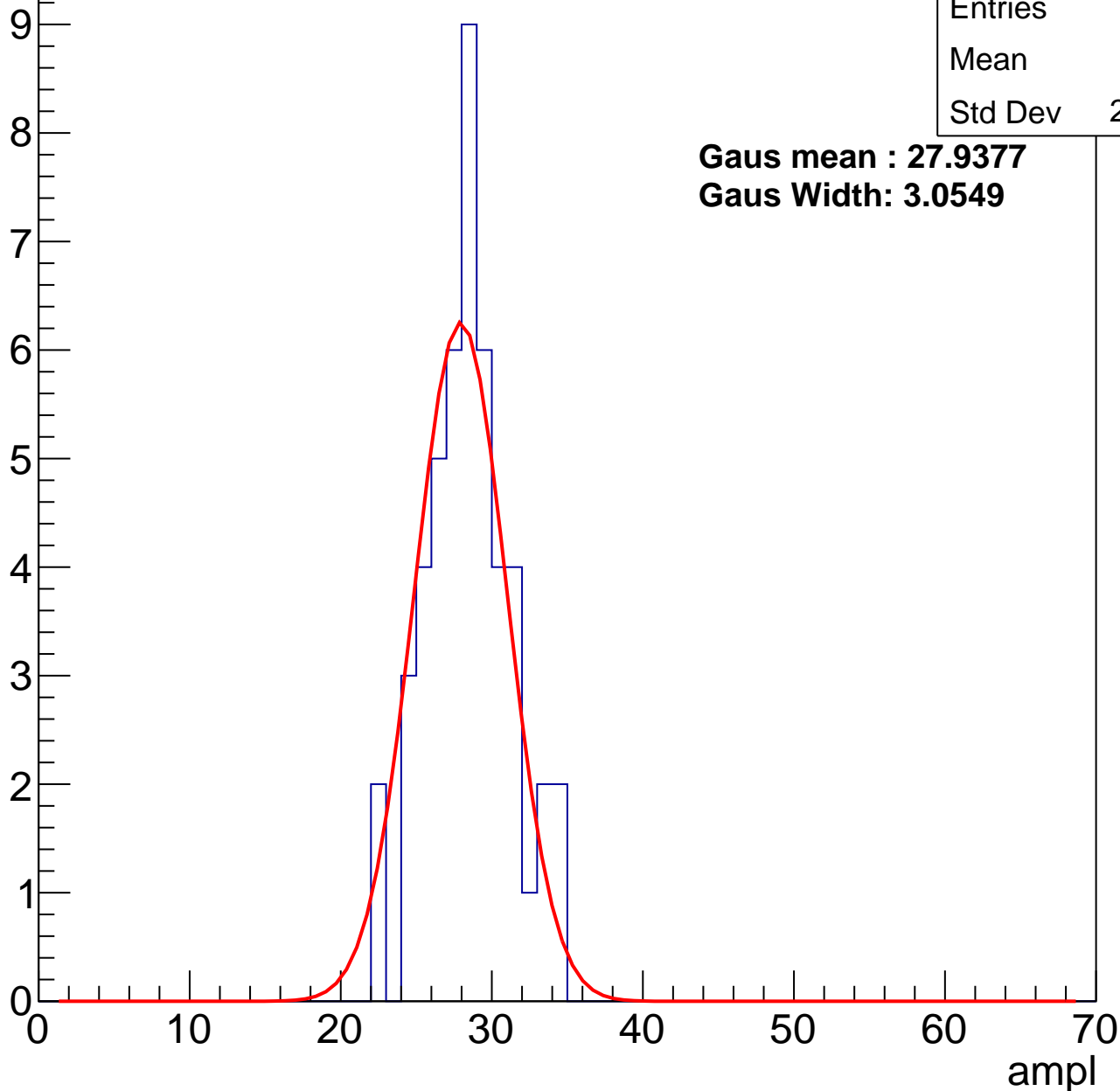
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	48
Mean	28
Std Dev	2.806

**Gaus mean : 27.9377**

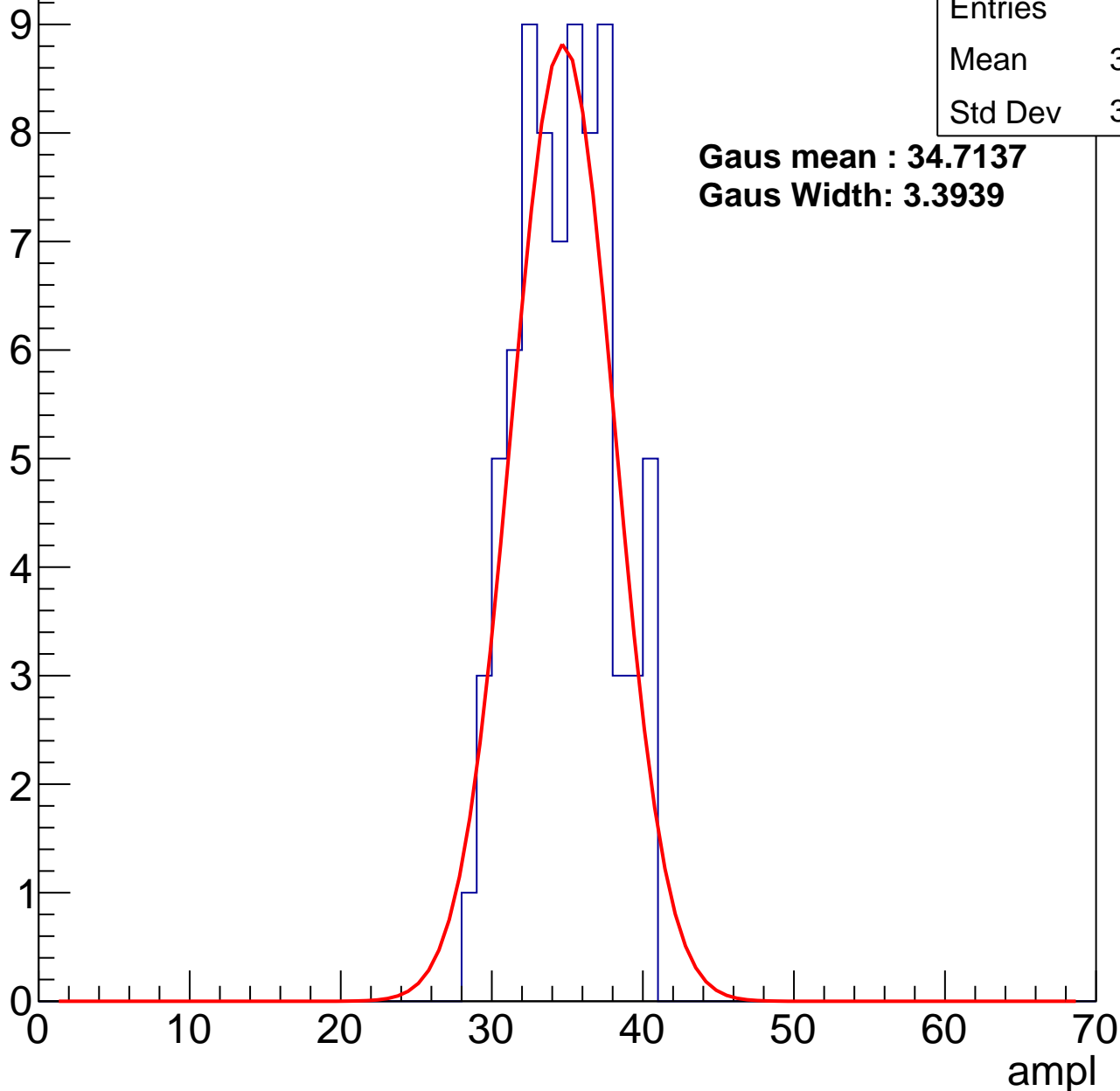
**Gaus Width: 3.0549**



# B1L003S, U18-ch100, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U18-ch100, adc2

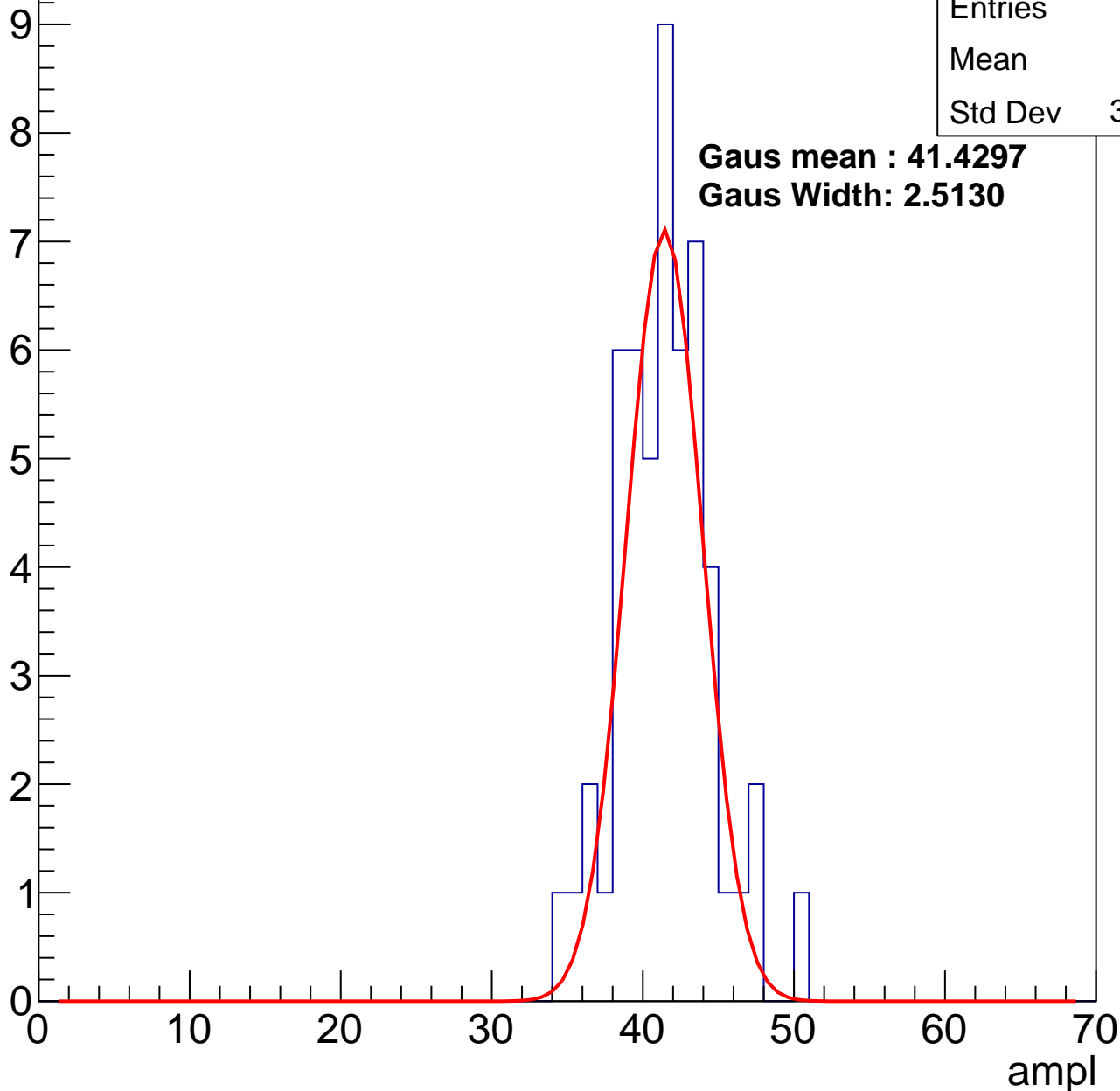
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	53
Mean	41
Std Dev	3.065

**Gaus mean : 41.4297**

**Gaus Width: 2.5130**

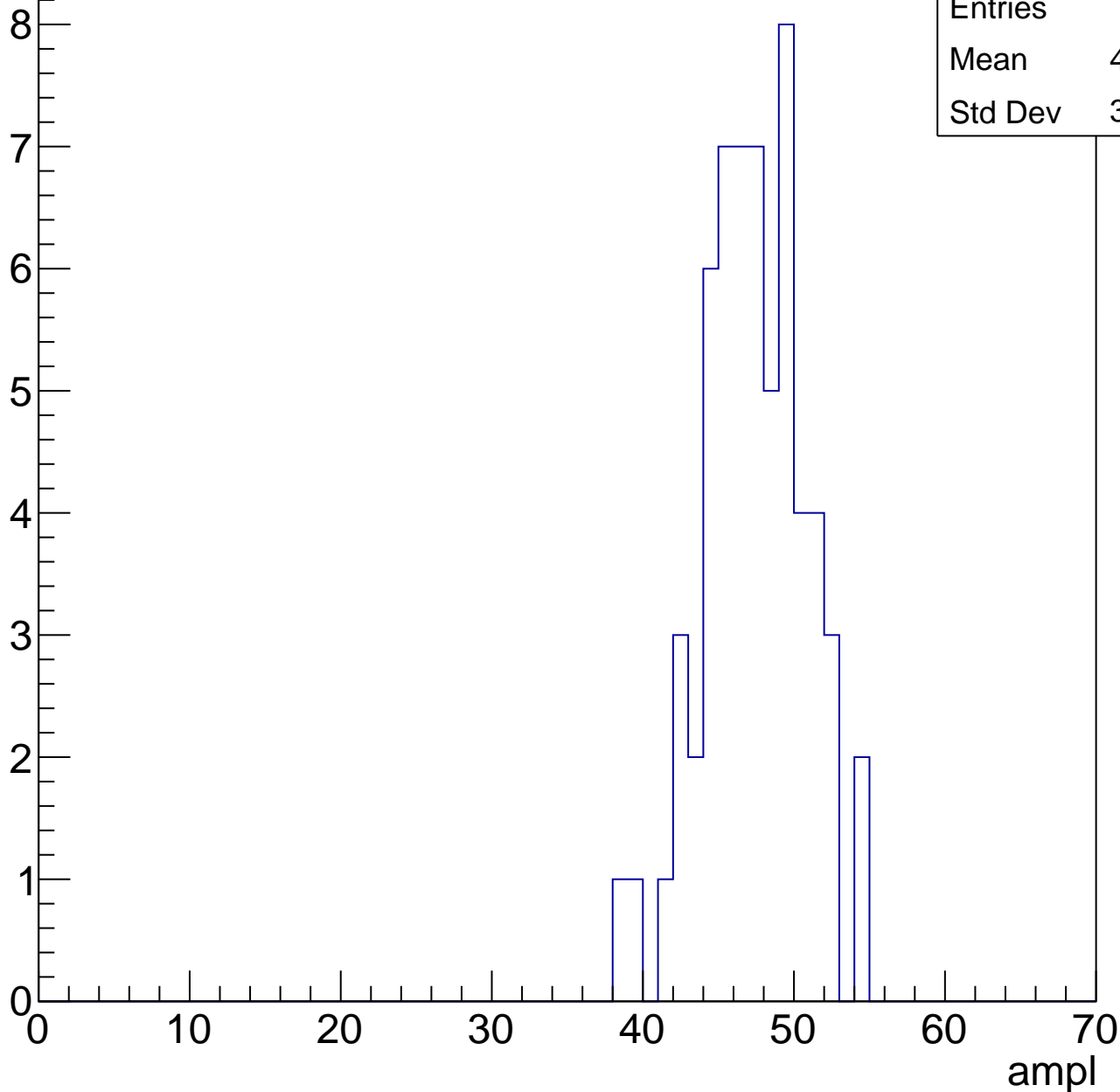


# B1L003S, U18-ch100, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	61
Mean	46.89
Std Dev	3.354

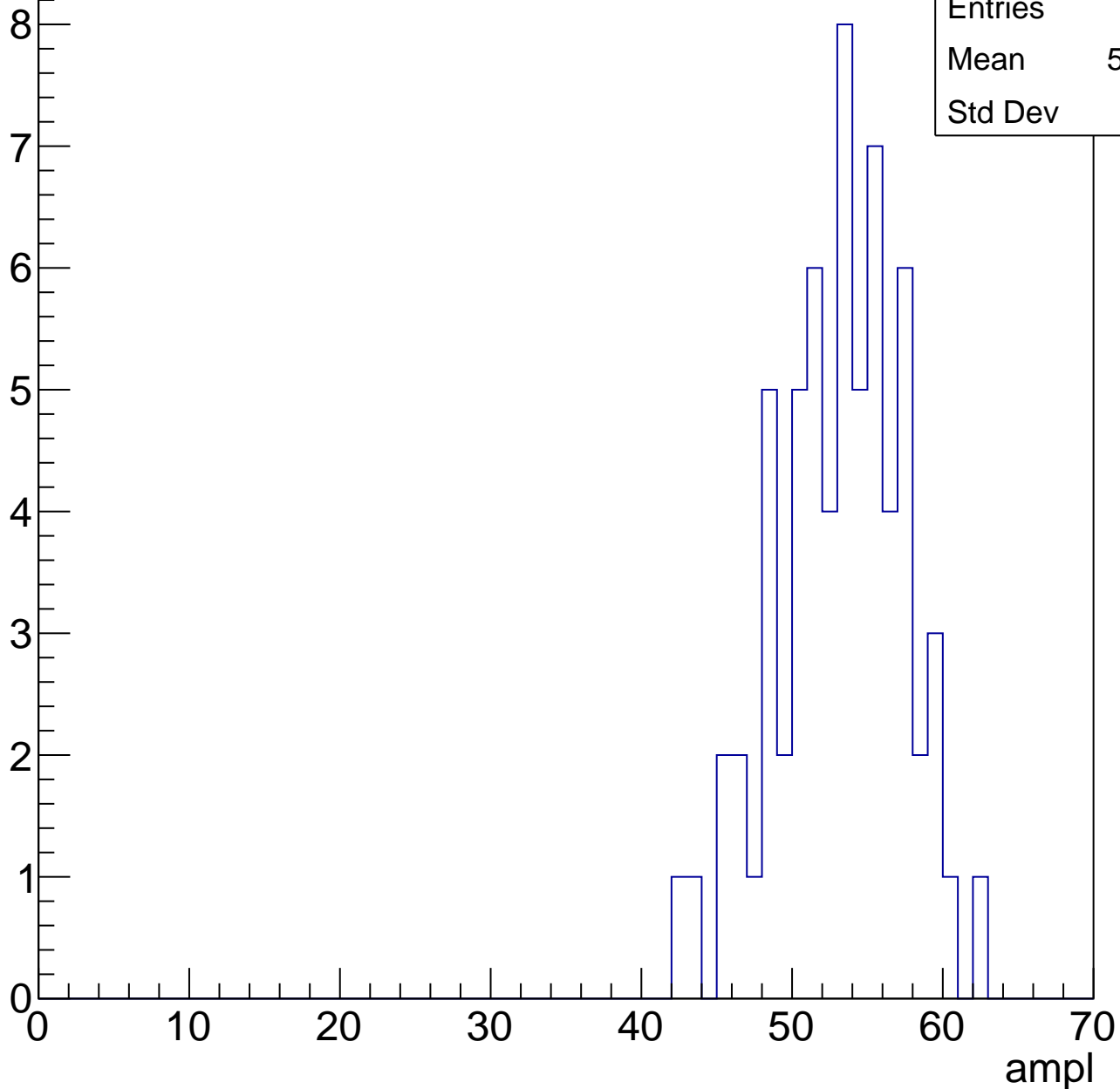


# B1L003S, U18-ch100, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	66
Mean	52.67
Std Dev	4.19

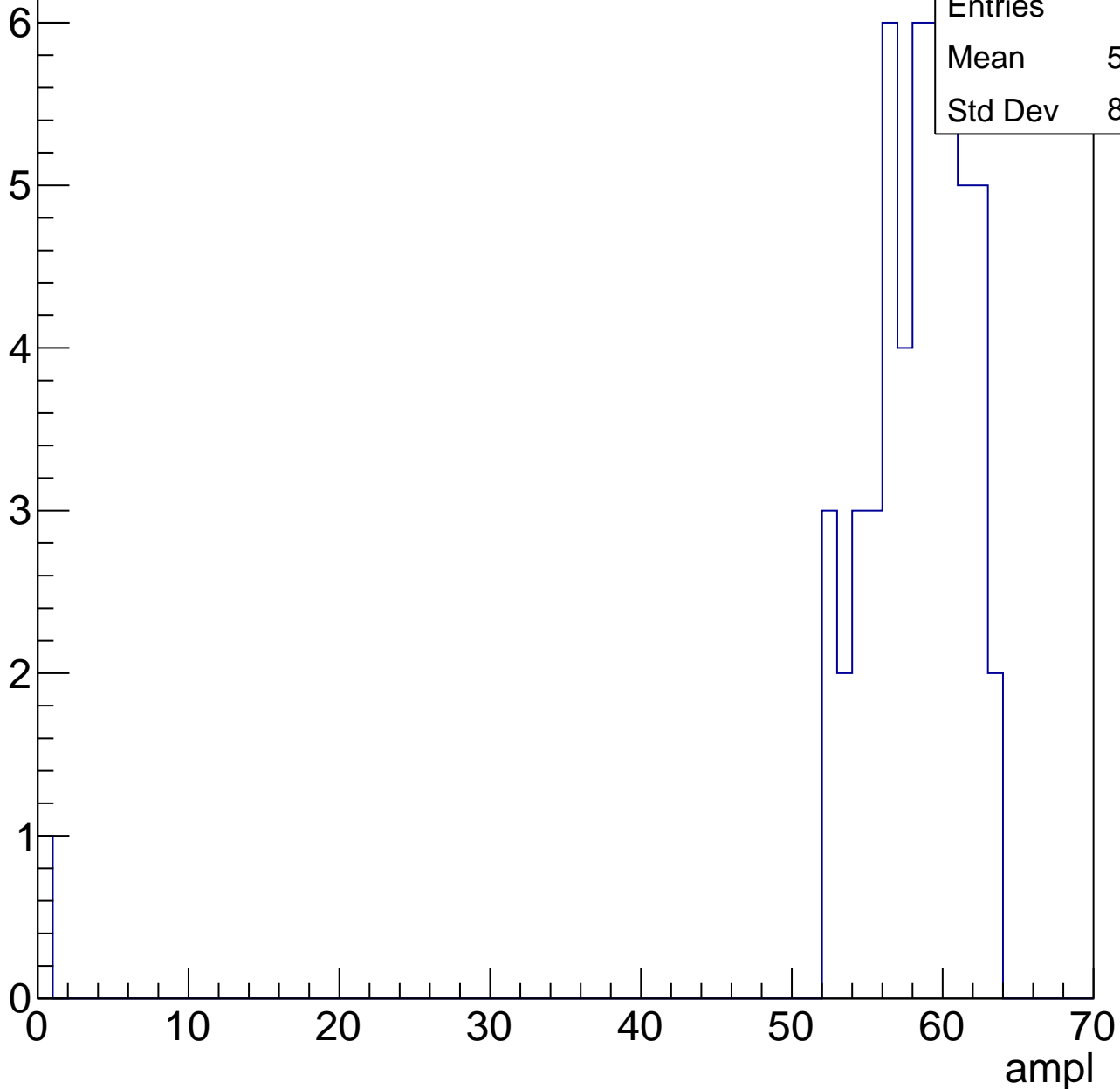


# B1L003S, U18-ch100, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	52
Mean	56.85
Std Dev	8.504

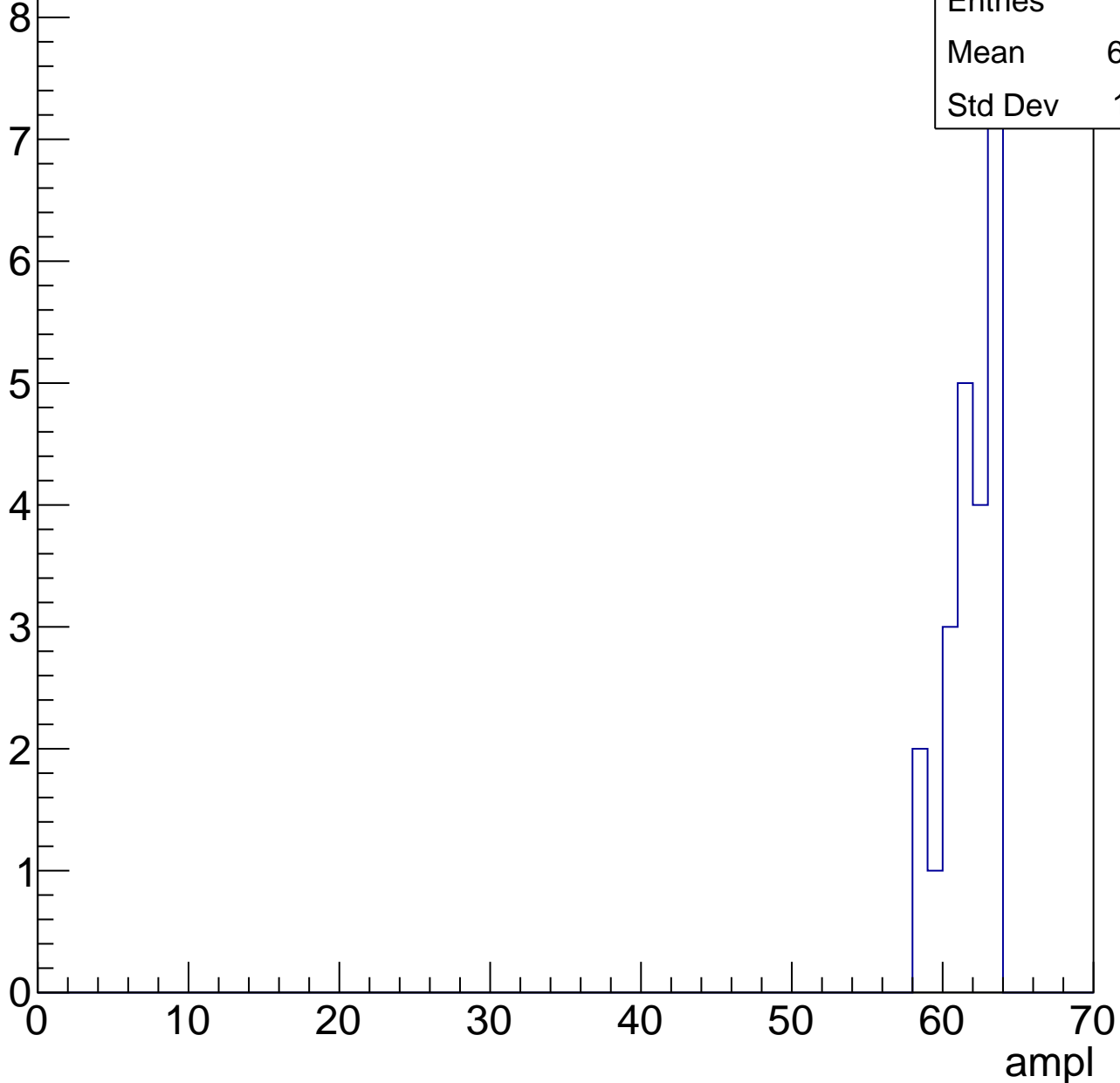


# B1L003S, U18-ch100, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	23
Mean	61.39
Std Dev	1.581





# B1L003S, U18-ch100, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch101, adc0

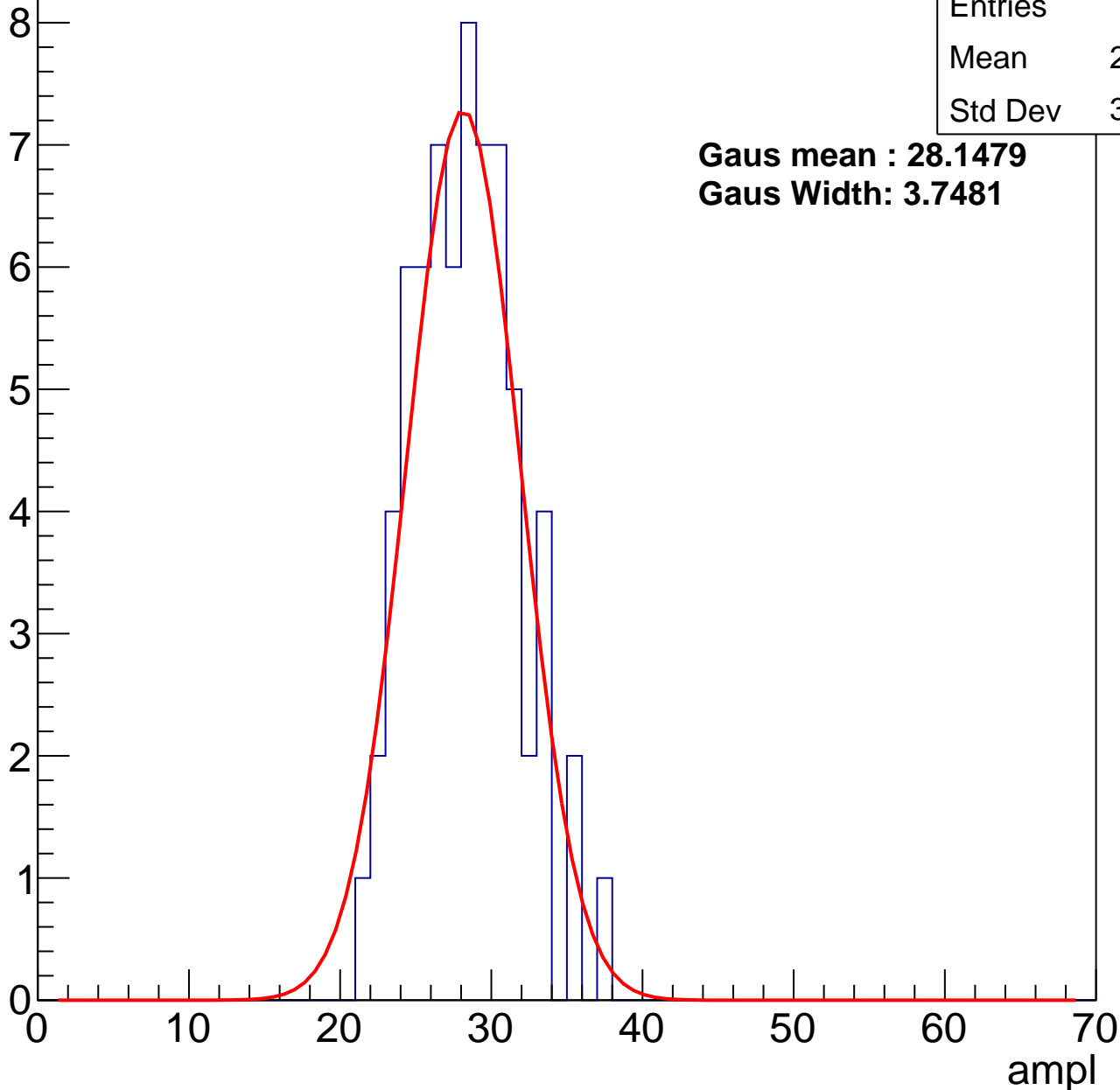
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	68
Mean	27.79
Std Dev	3.415

**Gaus mean : 28.1479**

**Gaus Width: 3.7481**



# B1L003S, U18-ch101, adc1

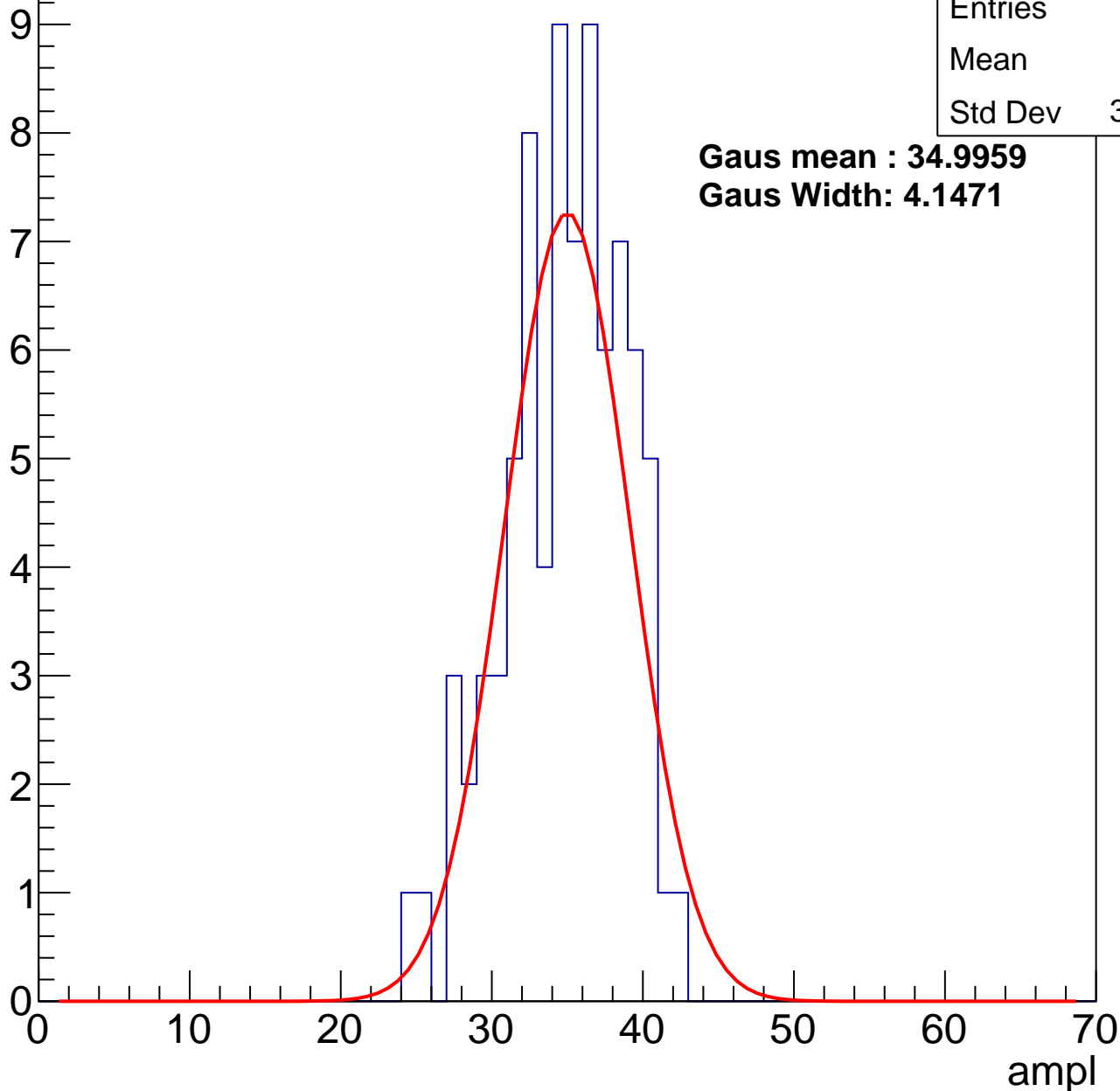
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	81
Mean	34.4
Std Dev	3.918

**Gaus mean : 34.9959**

**Gaus Width: 4.1471**



# B1L003S, U18-ch101, adc2

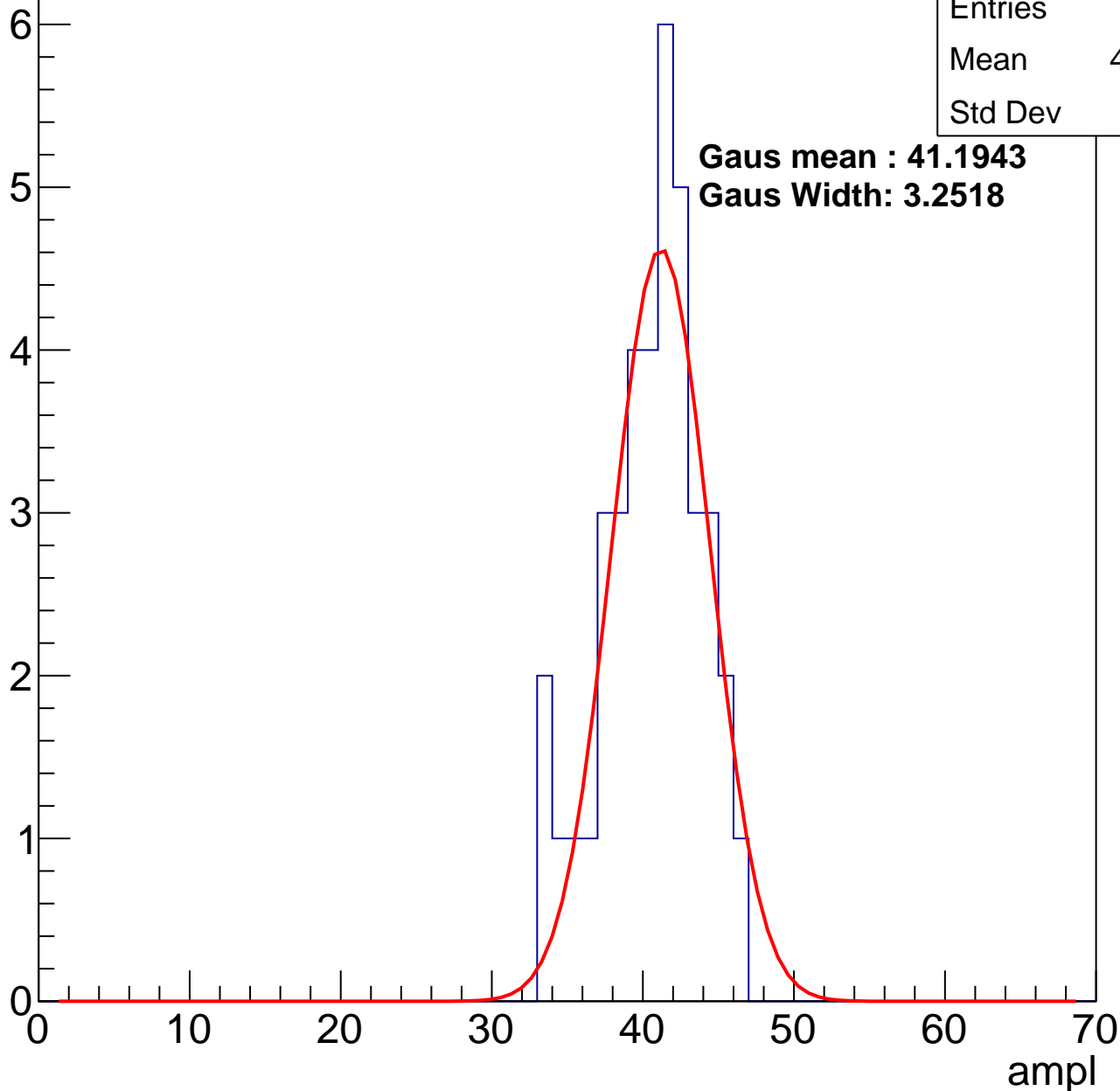
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	39
Mean	40.13
Std Dev	3.22

**Gaus mean : 41.1943**

**Gaus Width: 3.2518**

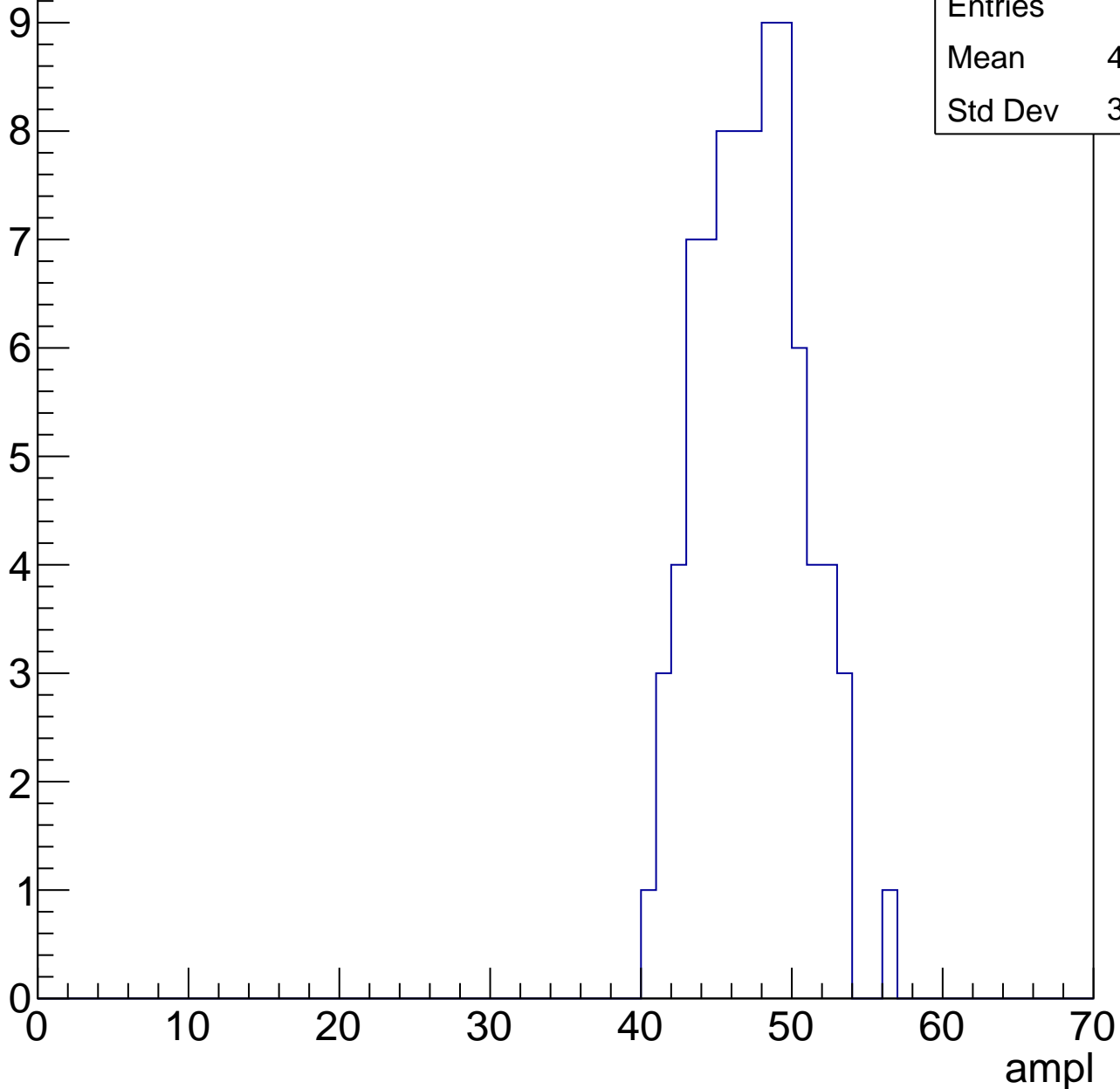


# B1L003S, U18-ch101, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	82
Mean	46.88
Std Dev	3.355

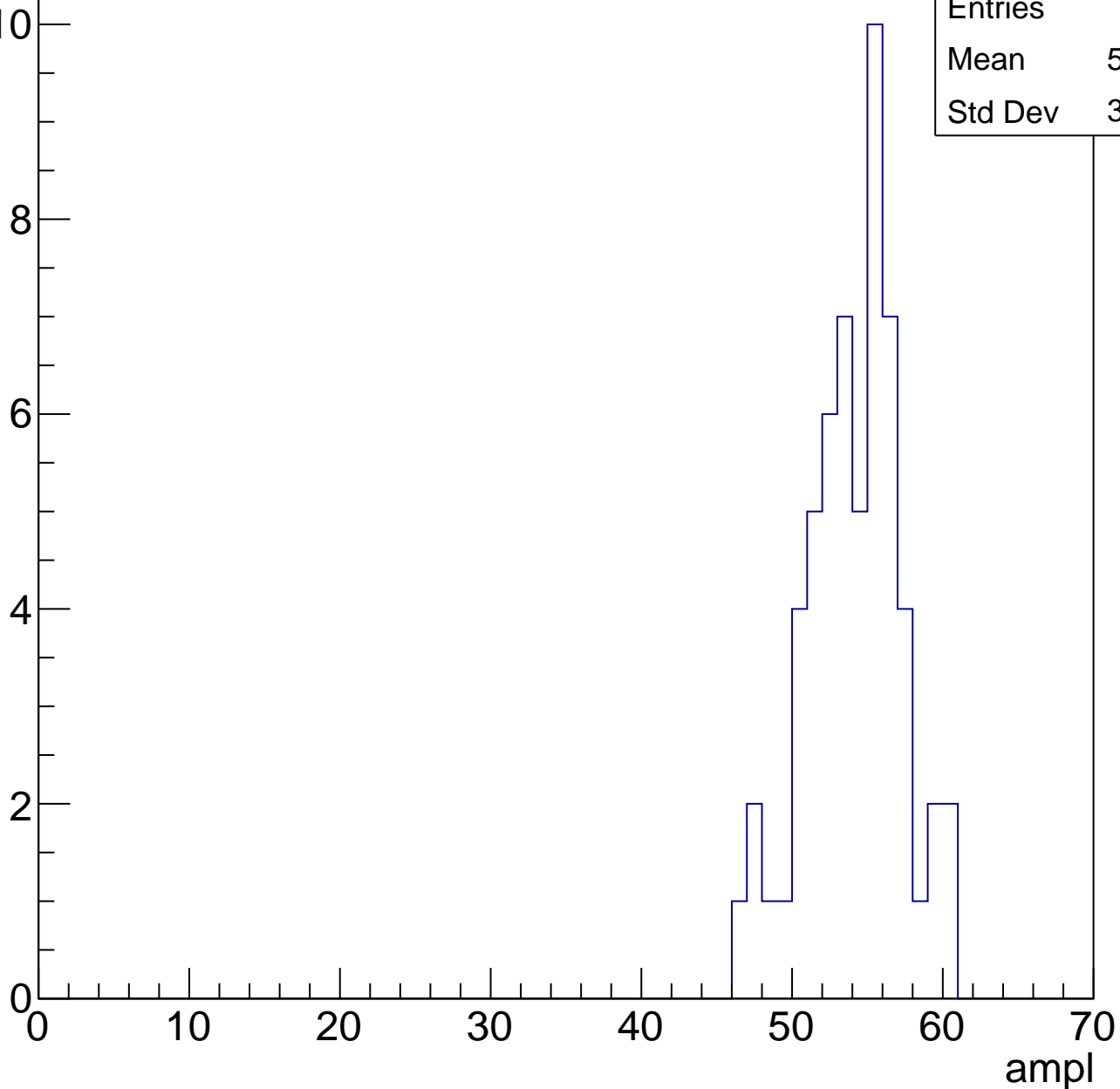


# B1L003S, U18-ch101, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	58
Mean	53.64
Std Dev	3.128

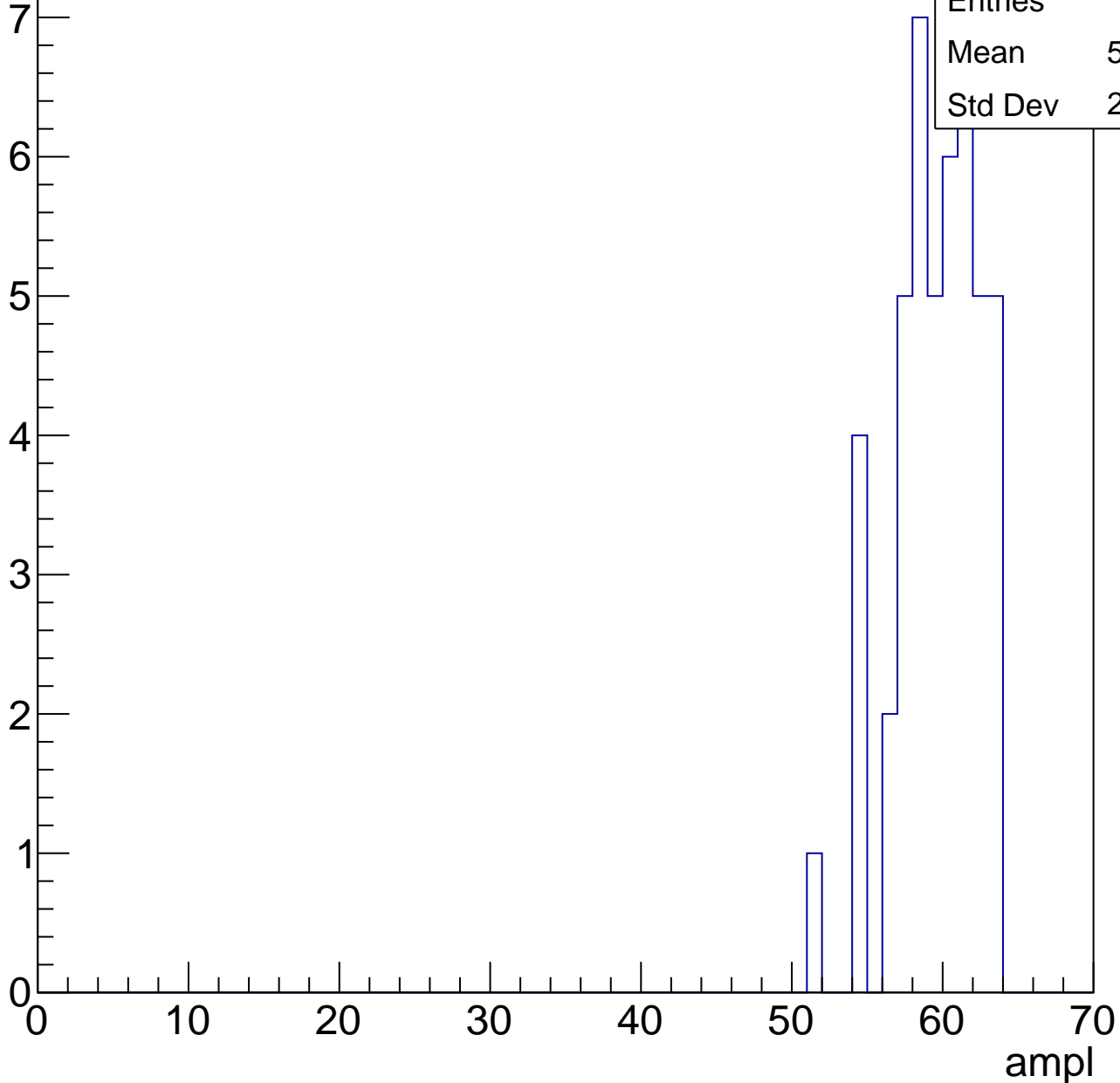


# B1L003S, U18-ch101, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	47
Mean	59.09
Std Dev	2.797

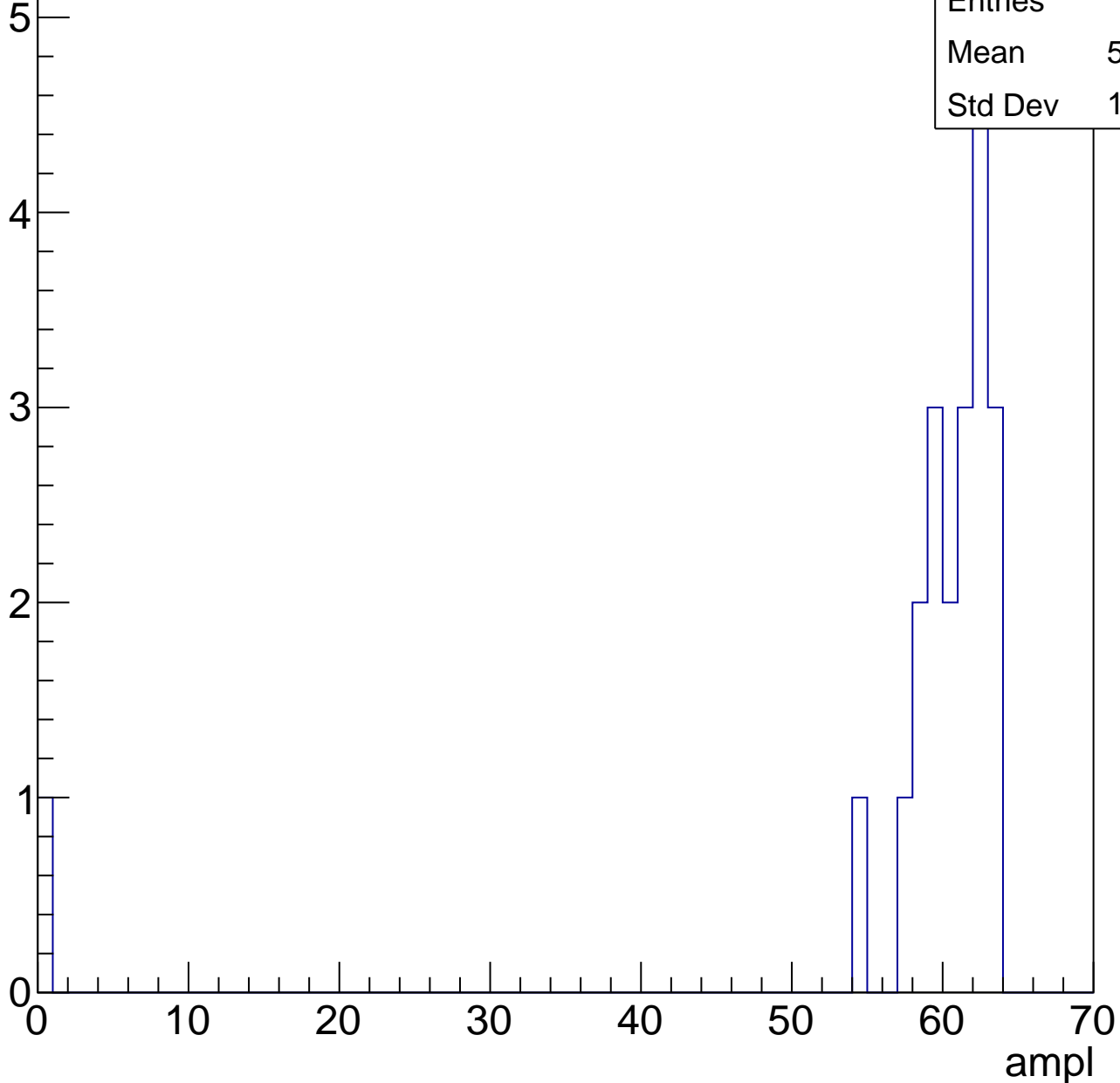


# B1L003S, U18-ch101, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	21
Mean	57.43
Std Dev	13.03

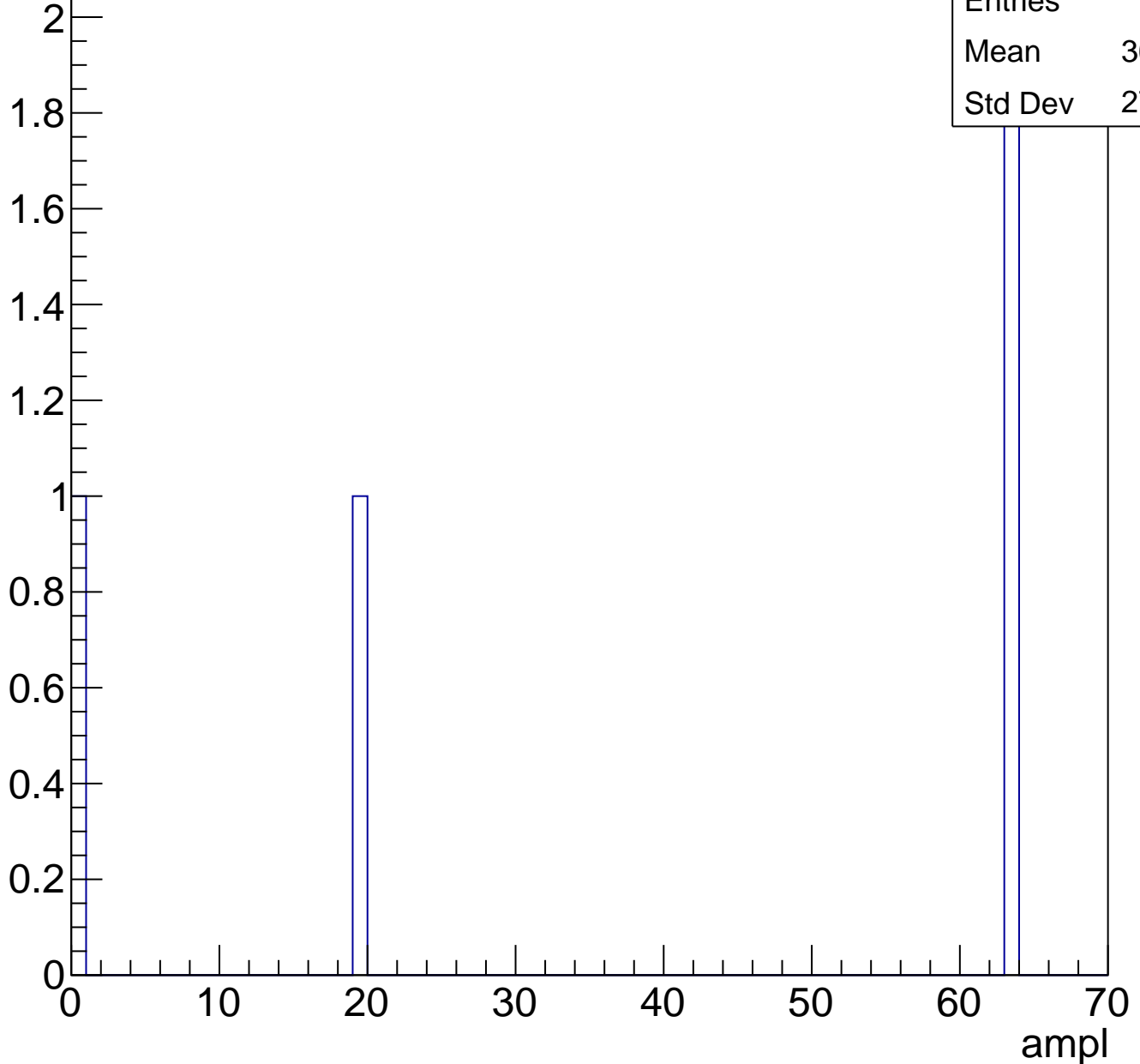




# B1L003S, U18-ch101, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	4
Mean	36.25
Std Dev	27.58

# B1L003S, U18-ch102, adc0

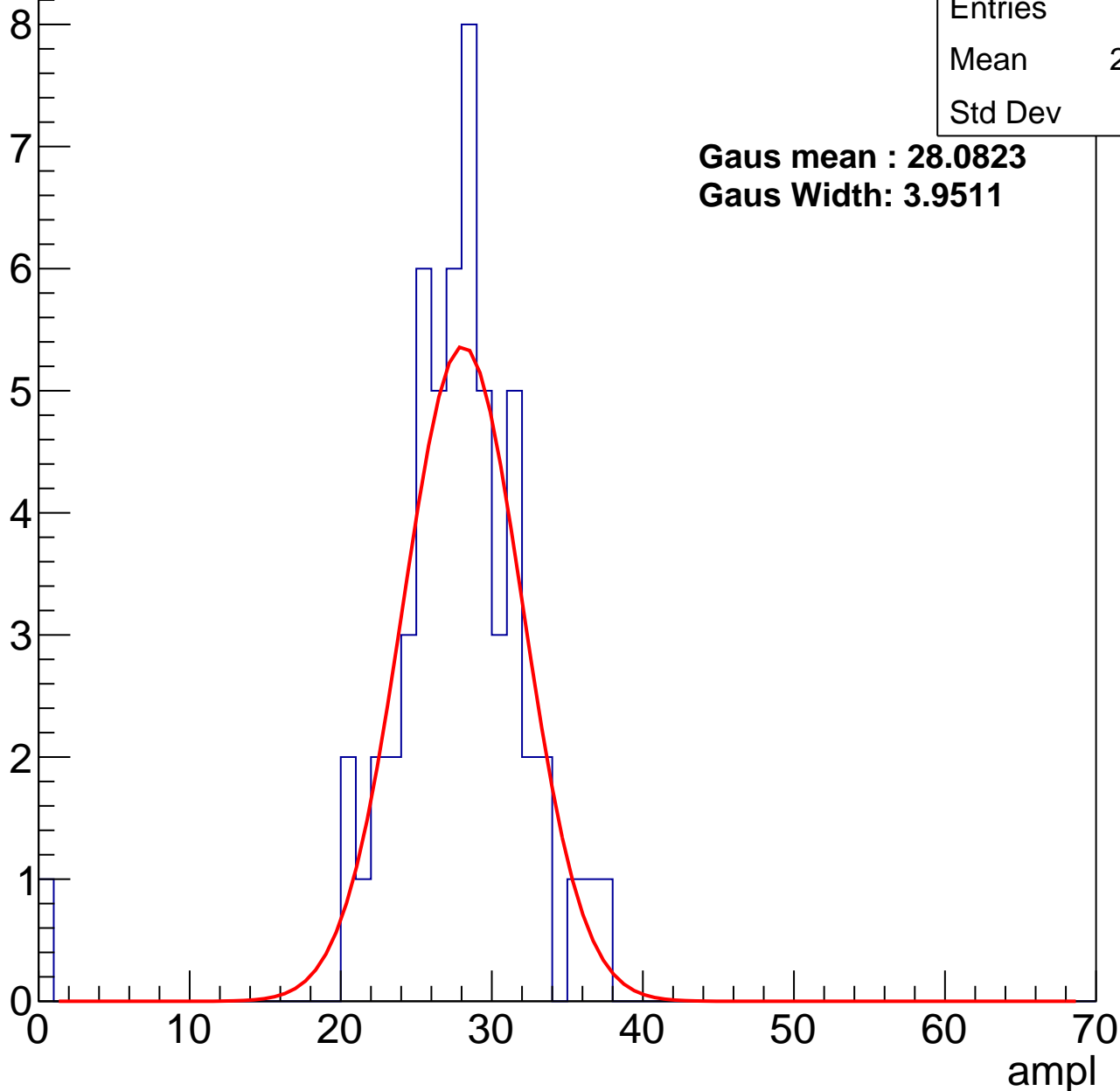
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	56
Mean	27.09
Std Dev	5.18

**Gaus mean : 28.0823**

**Gaus Width: 3.9511**



# B1L003S, U18-ch102, adc1

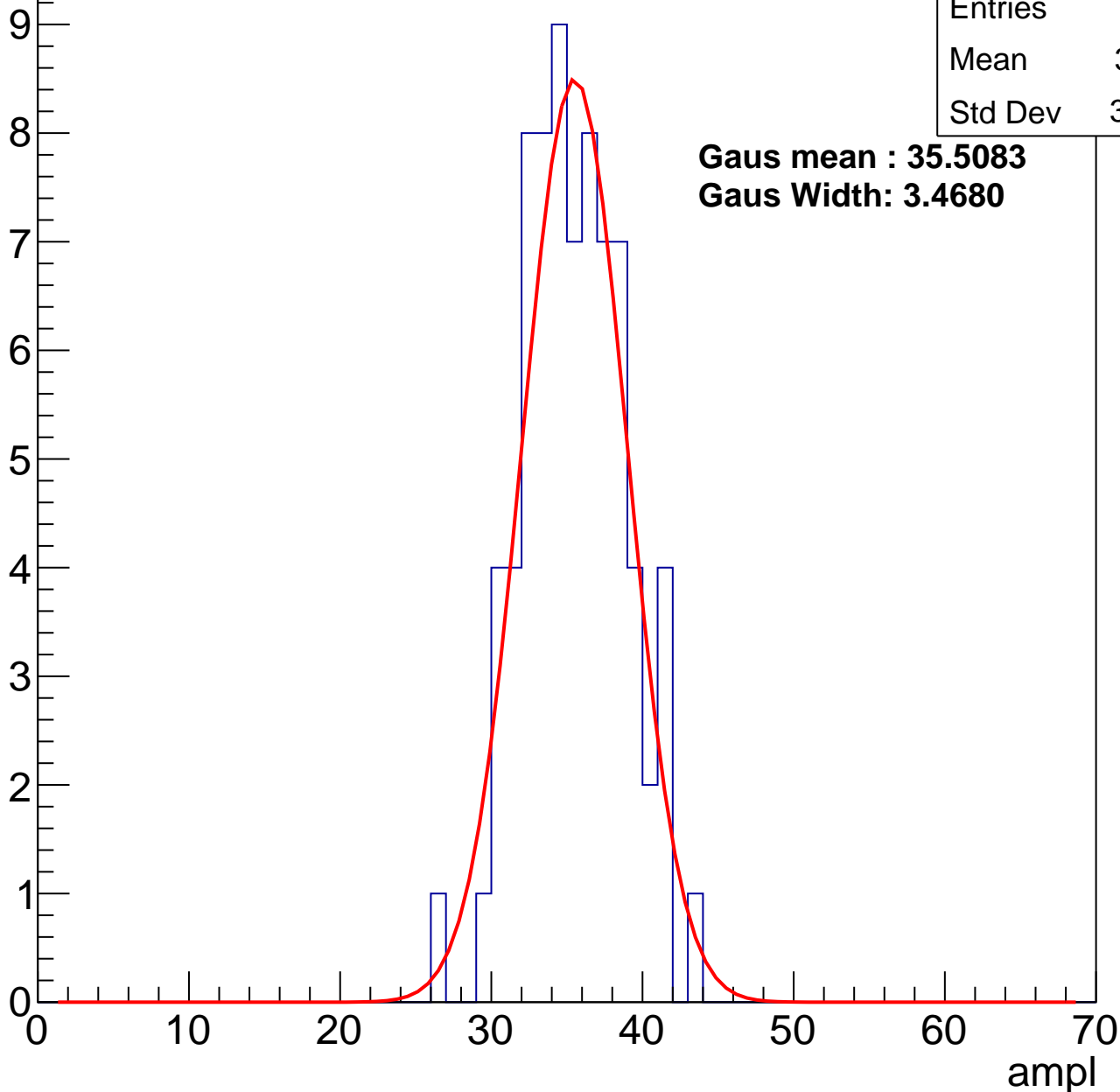
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	75
Mean	35.01
Std Dev	3.296

**Gaus mean : 35.5083**

**Gaus Width: 3.4680**



# B1L003S, U18-ch102, adc2

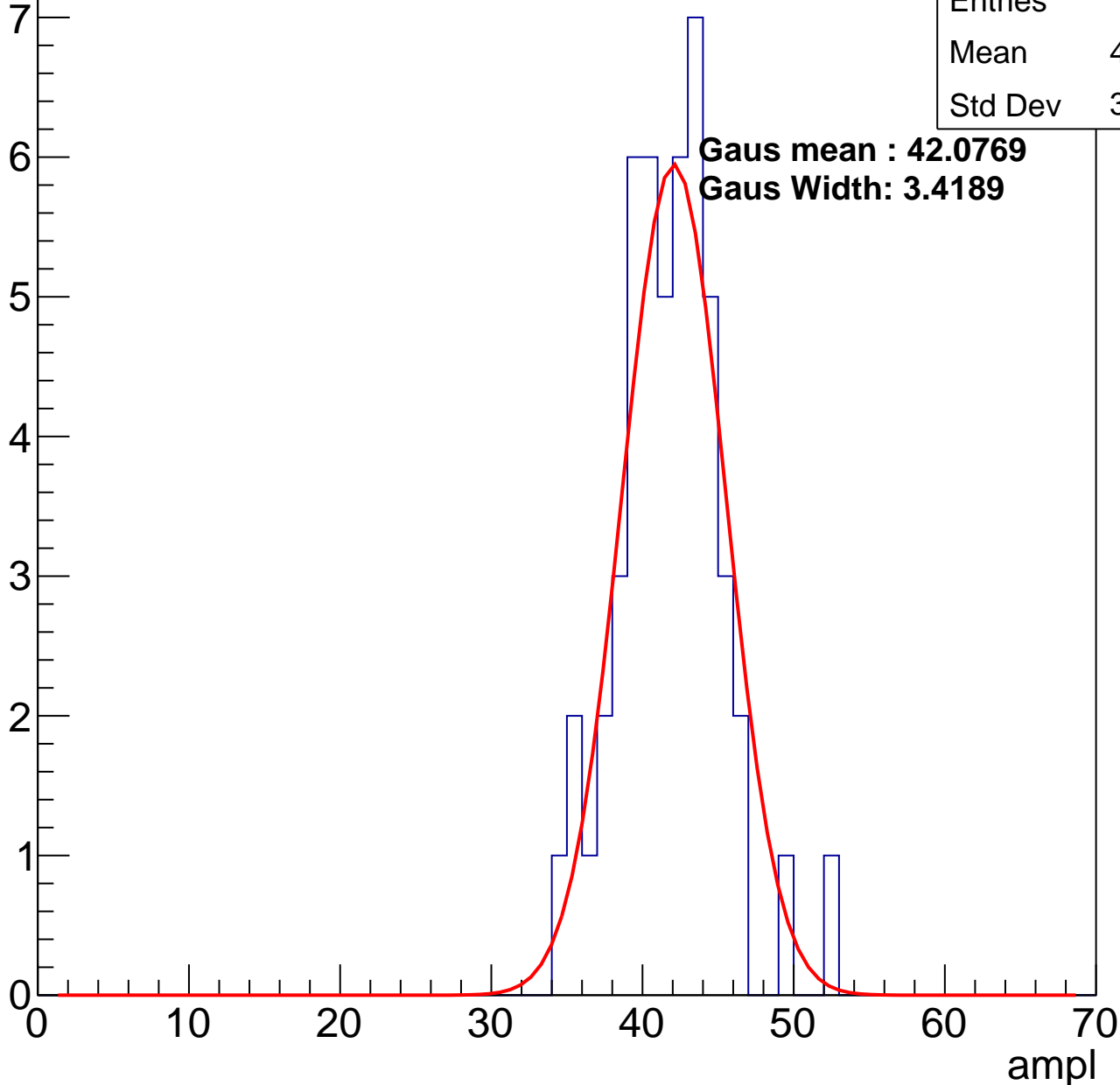
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	51
Mean	41.33
Std Dev	3.405

**Gaus mean : 42.0769**

**Gaus Width: 3.4189**

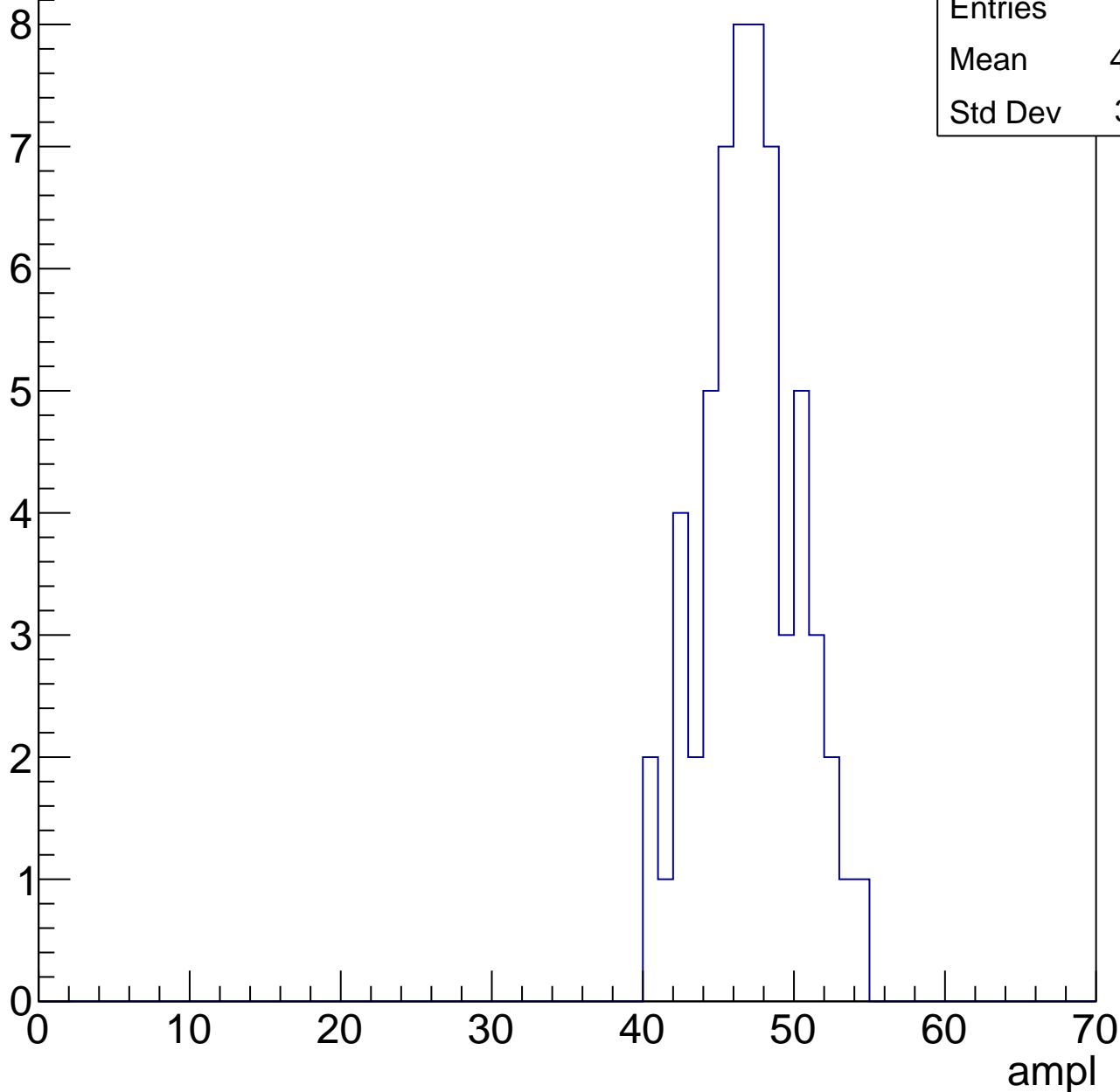


# B1L003S, U18-ch102, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	59
Mean	46.63
Std Dev	3.151

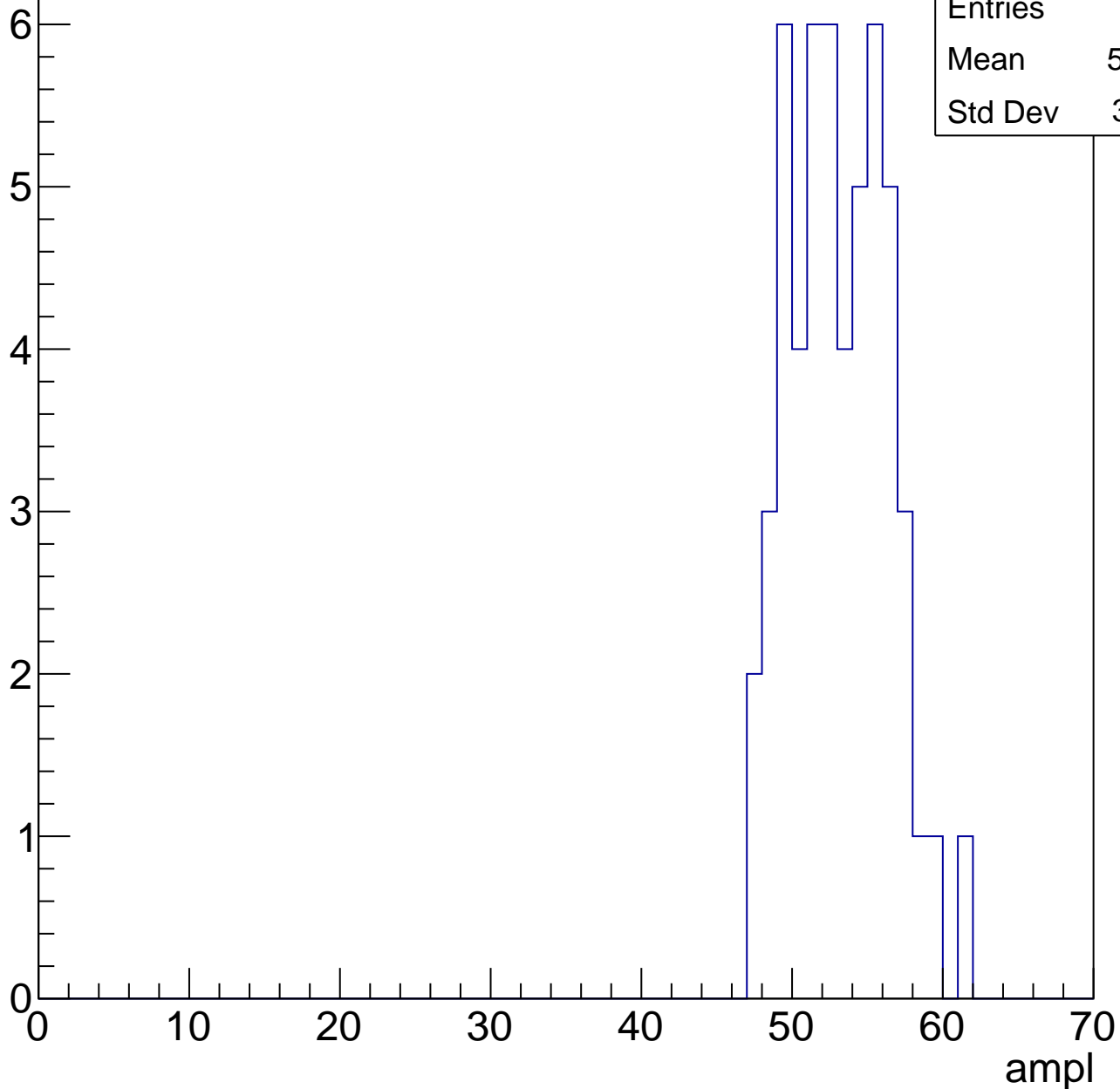


# B1L003S, U18-ch102, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	53
Mean	52.66
Std Dev	3.221

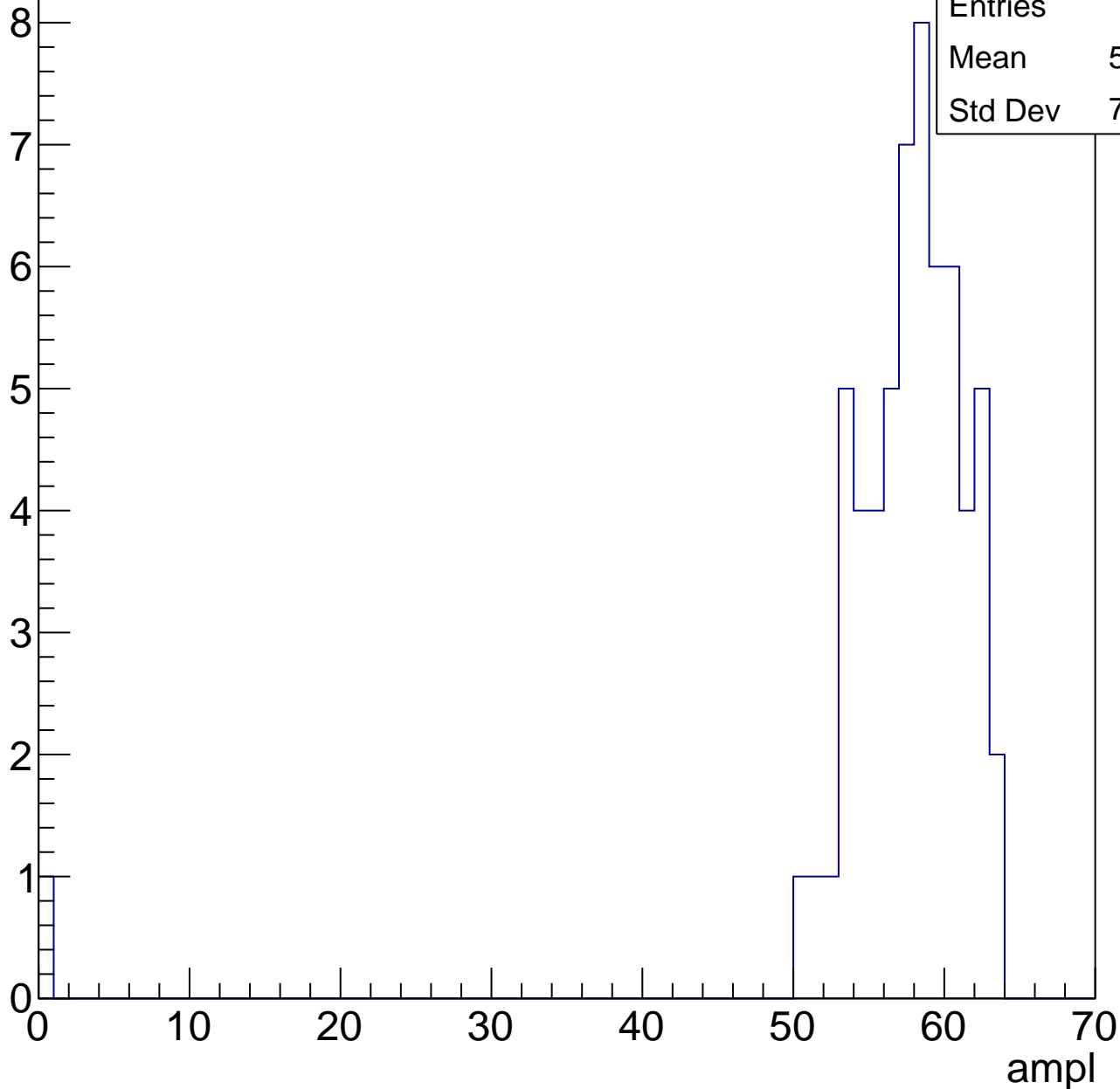


# B1L003S, U18-ch102, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	60
Mean	56.52
Std Dev	7.989

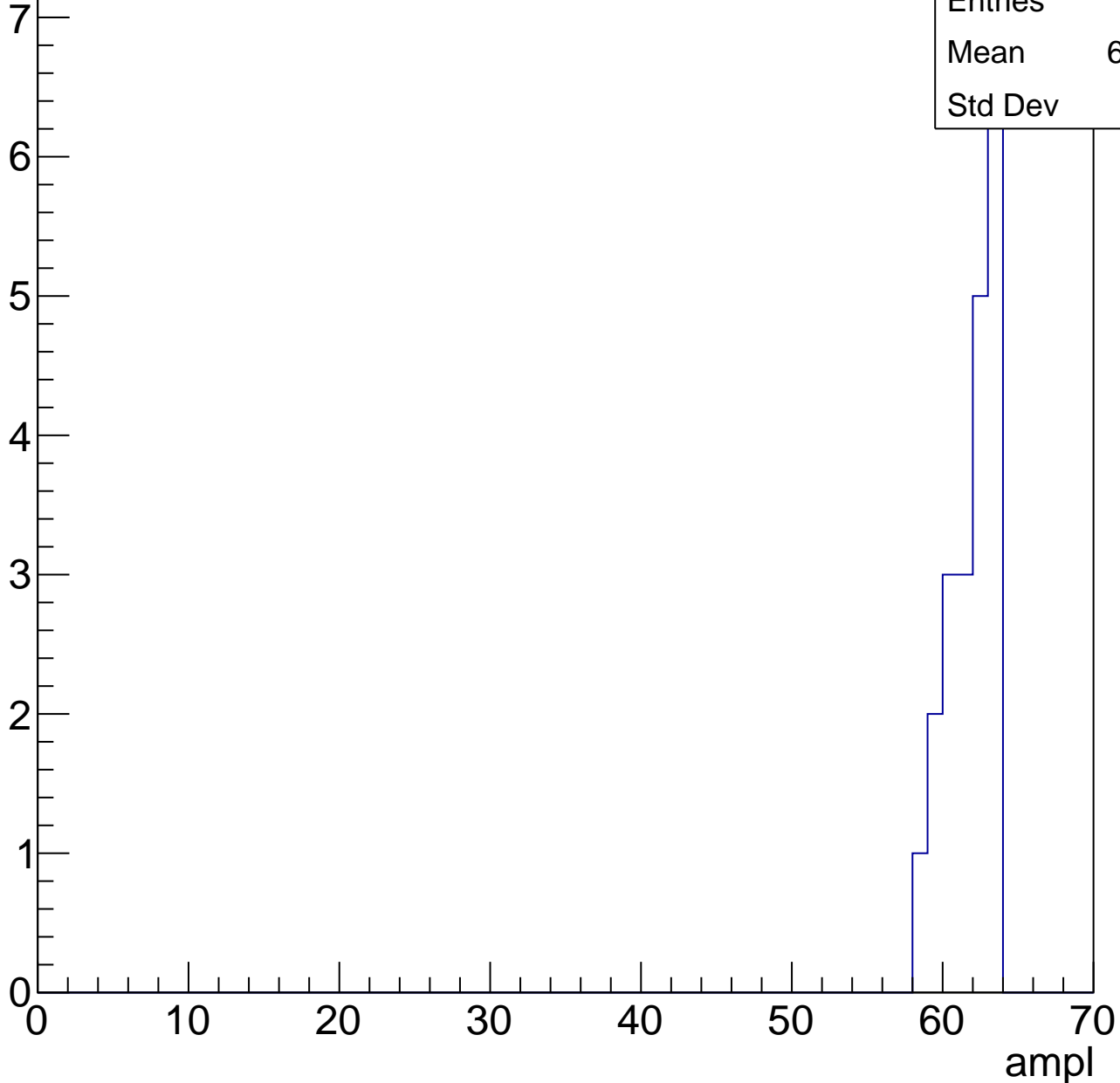


# B1L003S, U18-ch102, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	21
Mean	61.43
Std Dev	1.53





# B1L003S, U18-ch102, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

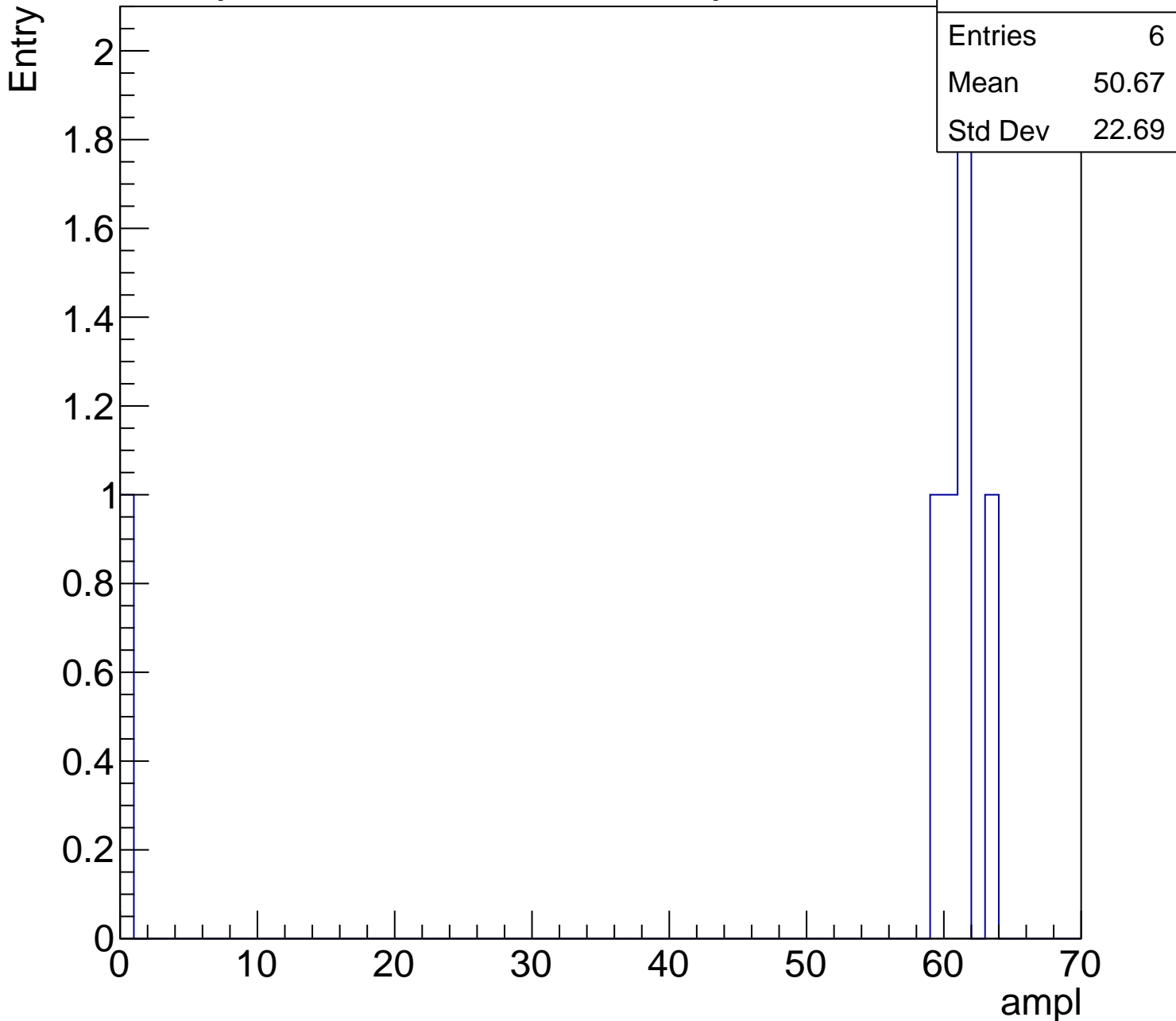
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	6
Mean	50.67
Std Dev	22.69

0 10 20 30 40 50 60 70

ampl



# B1L003S, U18-ch103, adc0

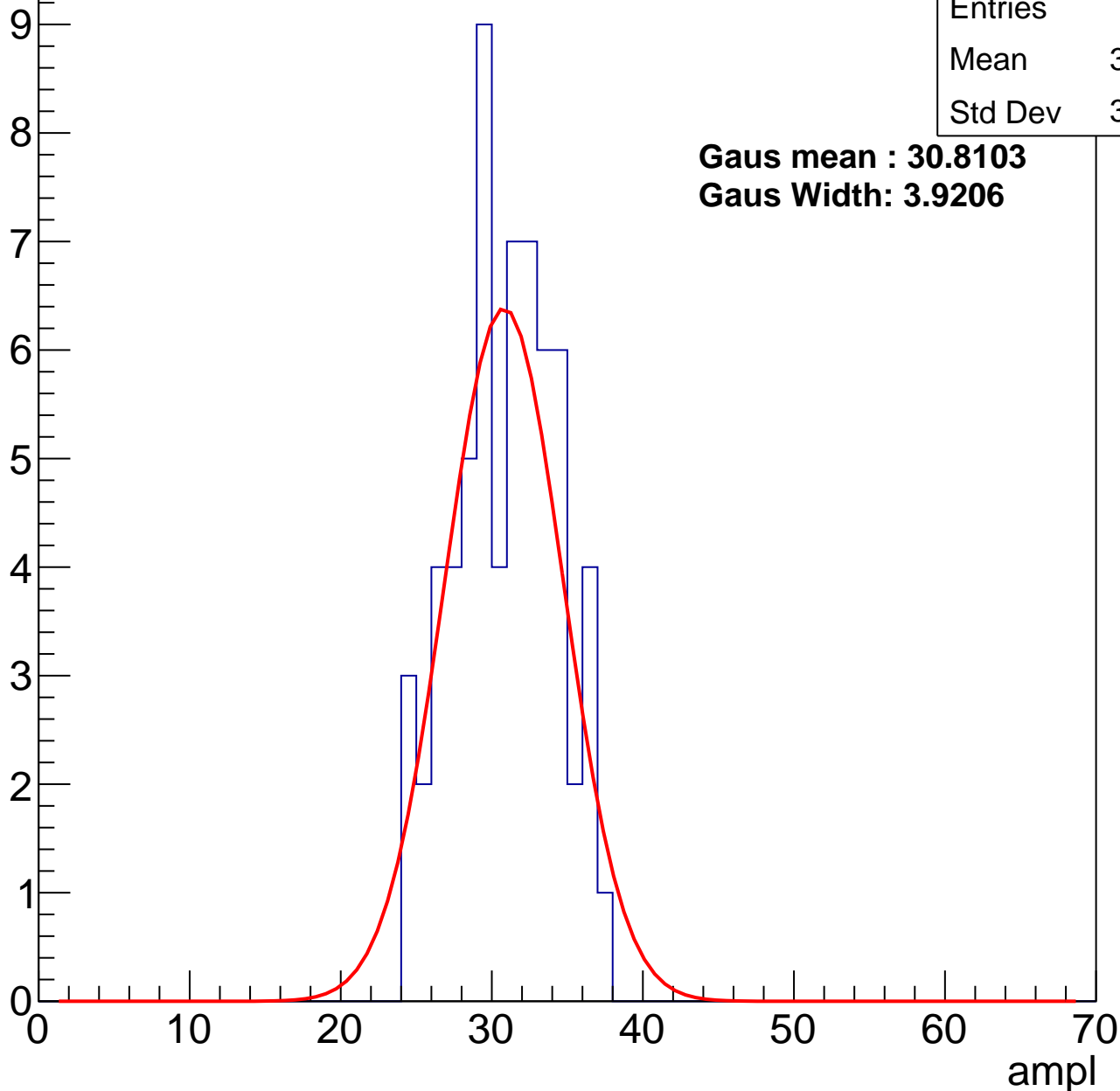
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	64
Mean	30.45
Std Dev	3.312

**Gaus mean : 30.8103**

**Gaus Width: 3.9206**



# B1L003S, U18-ch103, adc1

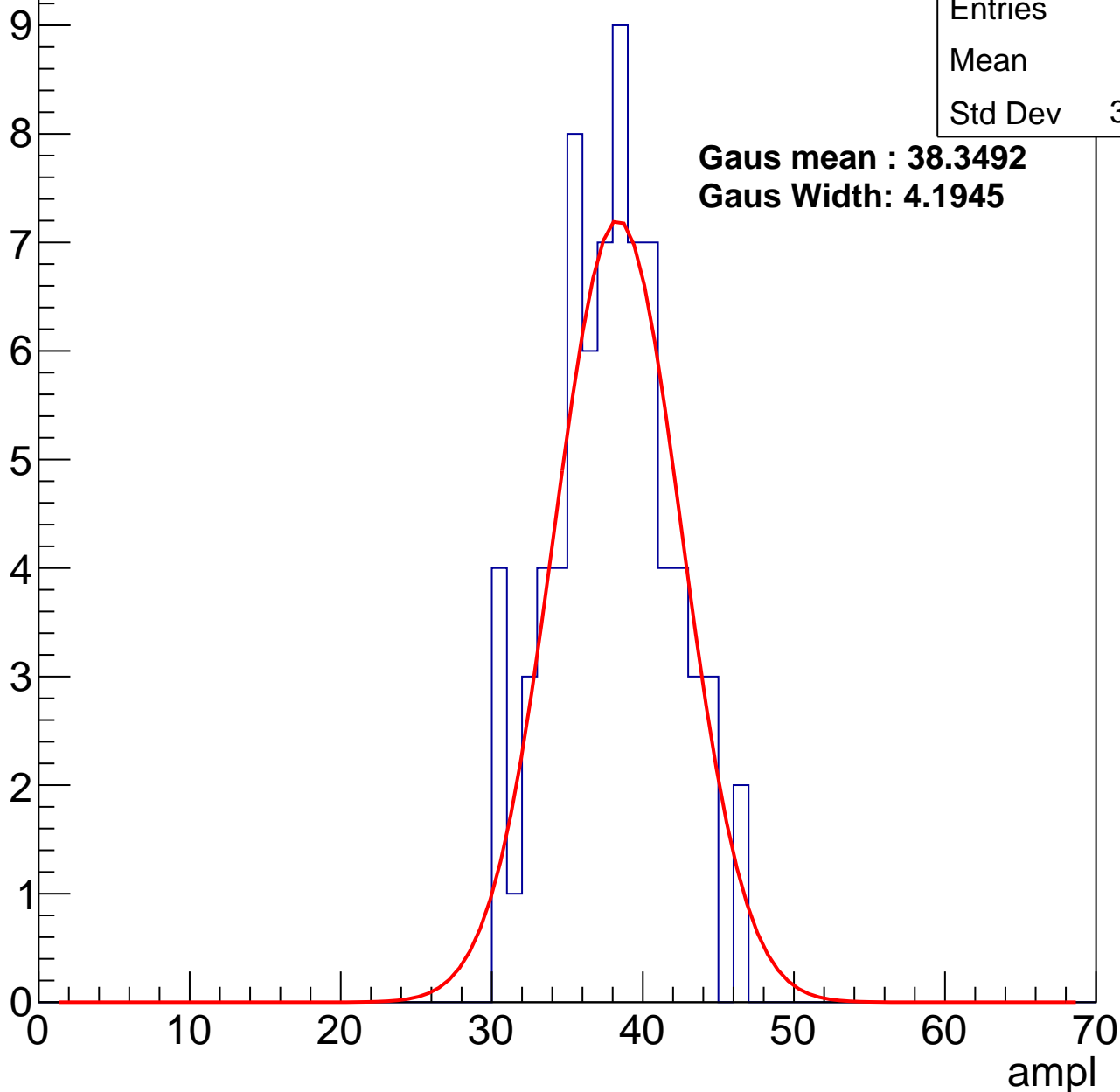
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	76
Mean	37.5
Std Dev	3.817

**Gaus mean : 38.3492**

**Gaus Width: 4.1945**



# B1L003S, U18-ch103, adc2

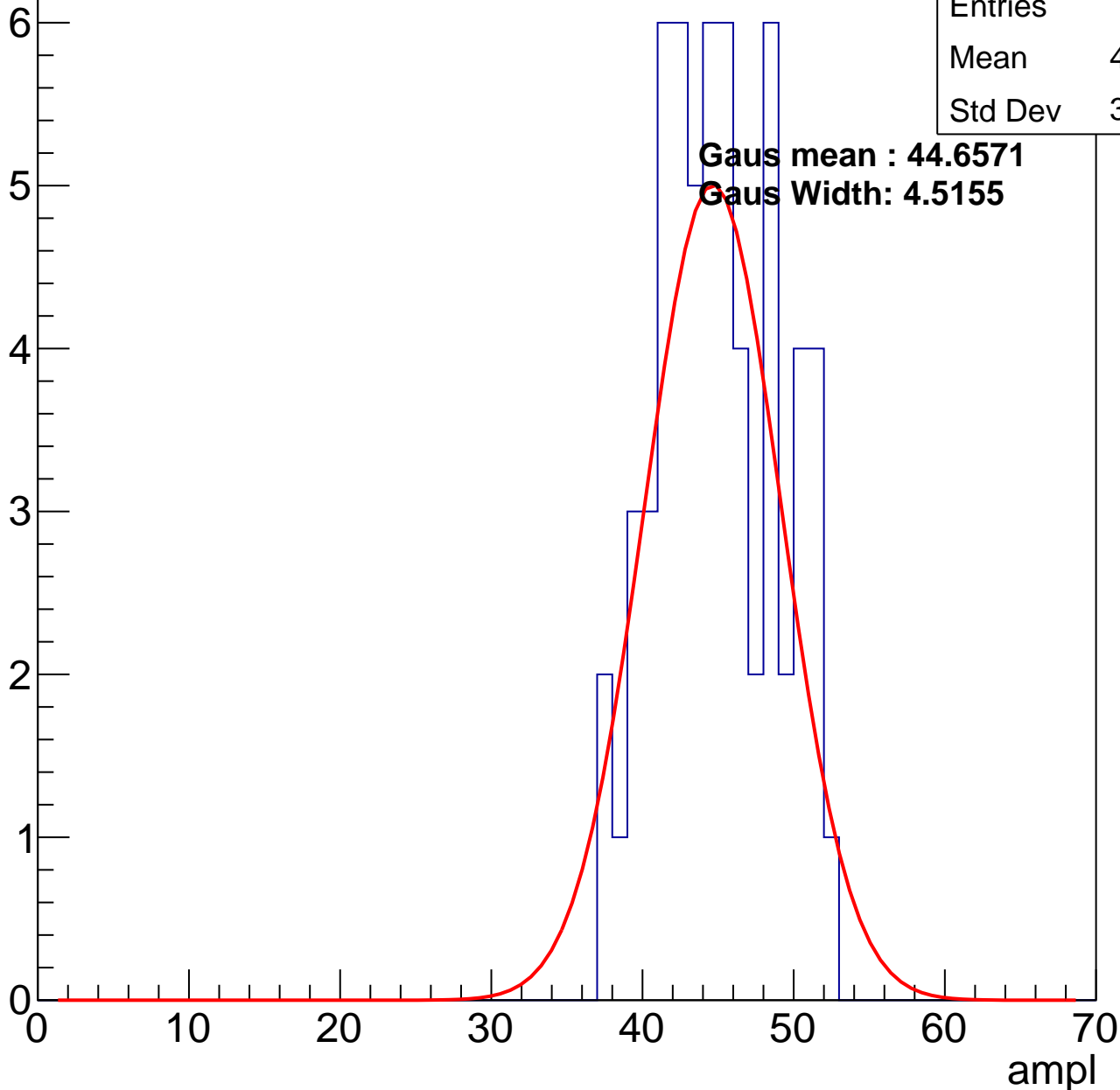
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	61
Mean	44.52
Std Dev	3.869

**Gaus mean : 44.6571**

**Gaus Width: 4.5155**

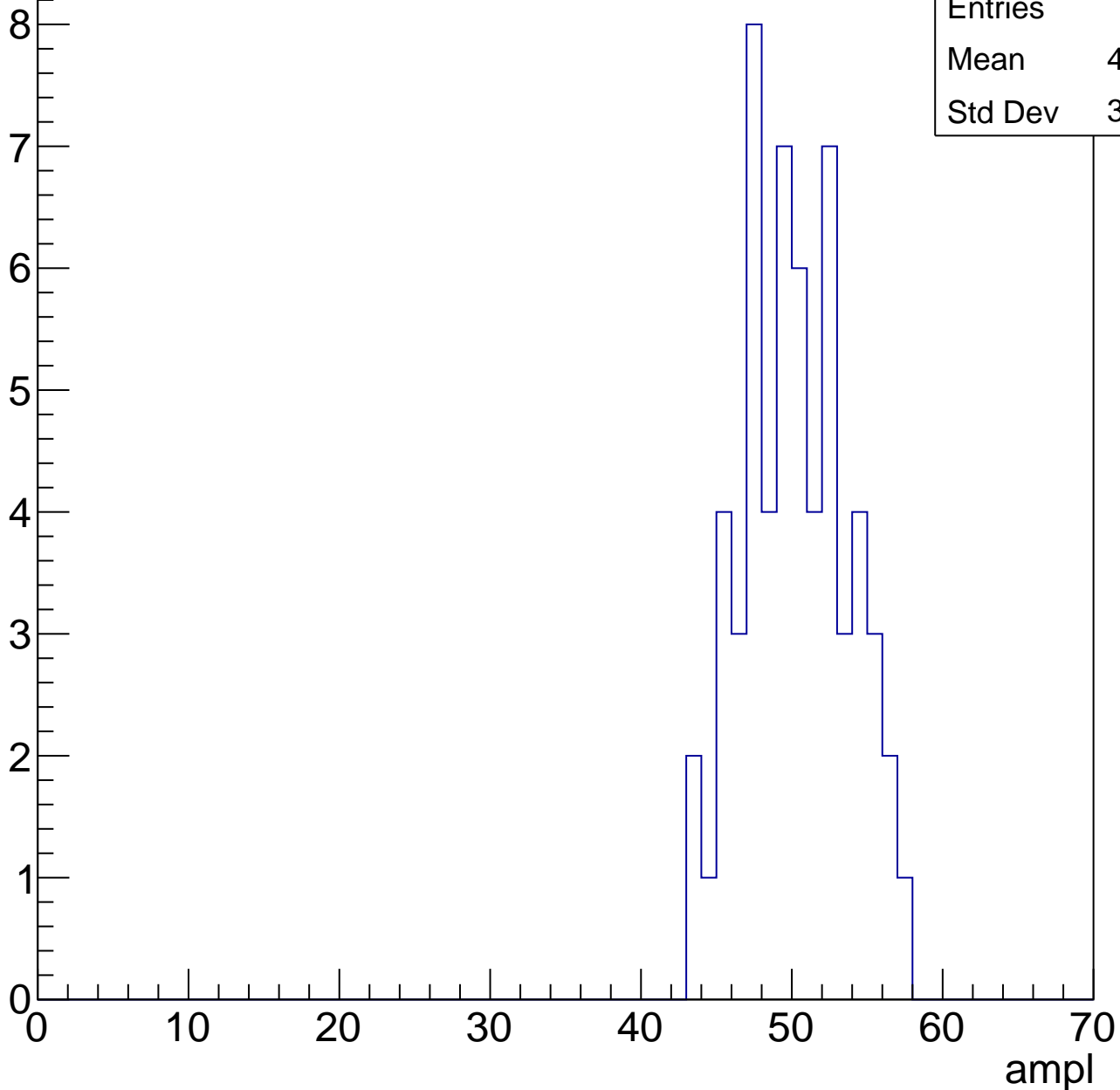


# B1L003S, U18-ch103, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	59
Mean	49.76
Std Dev	3.426

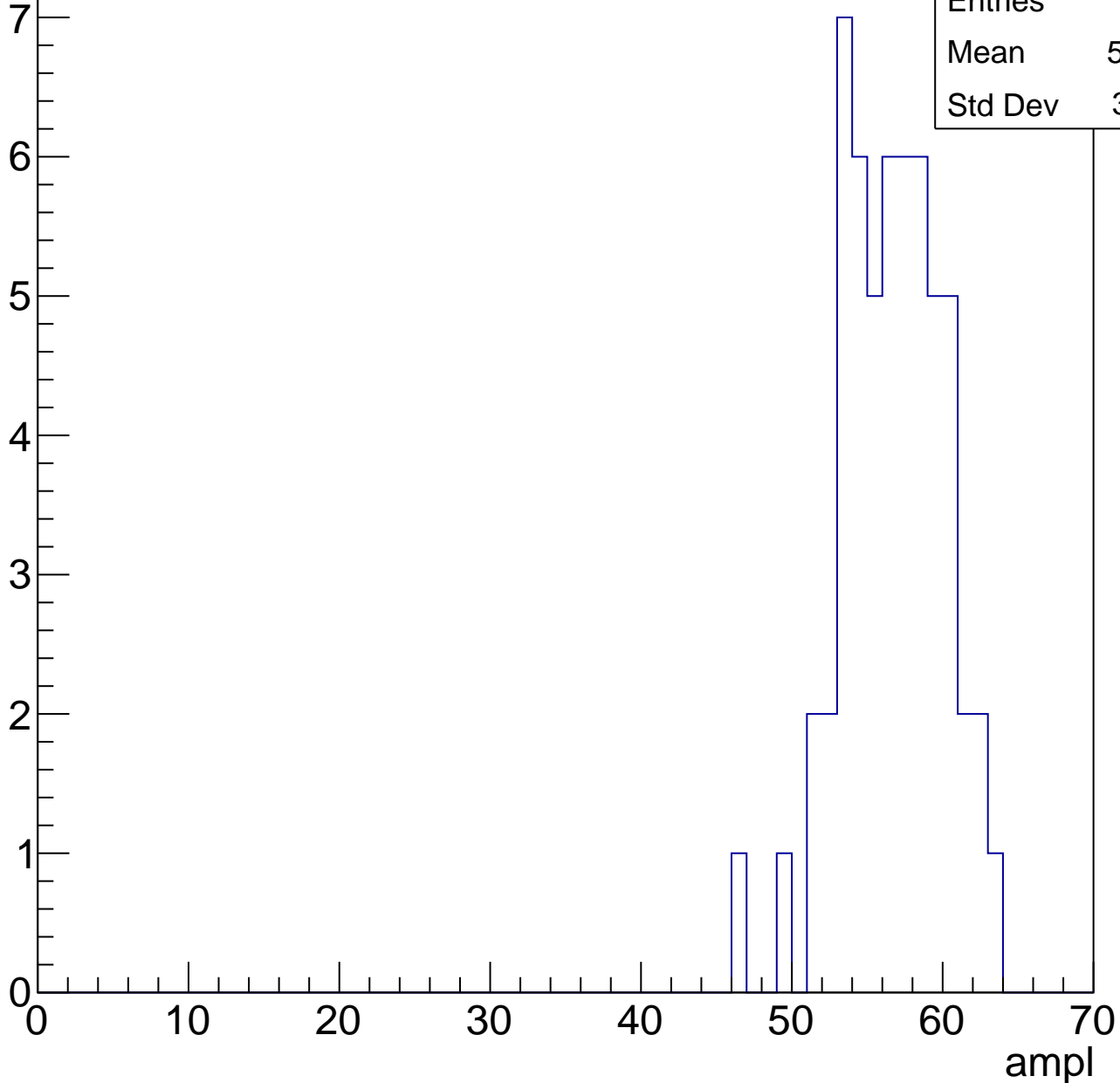


# B1L003S, U18-ch103, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	57
Mean	56.16
Std Dev	3.371

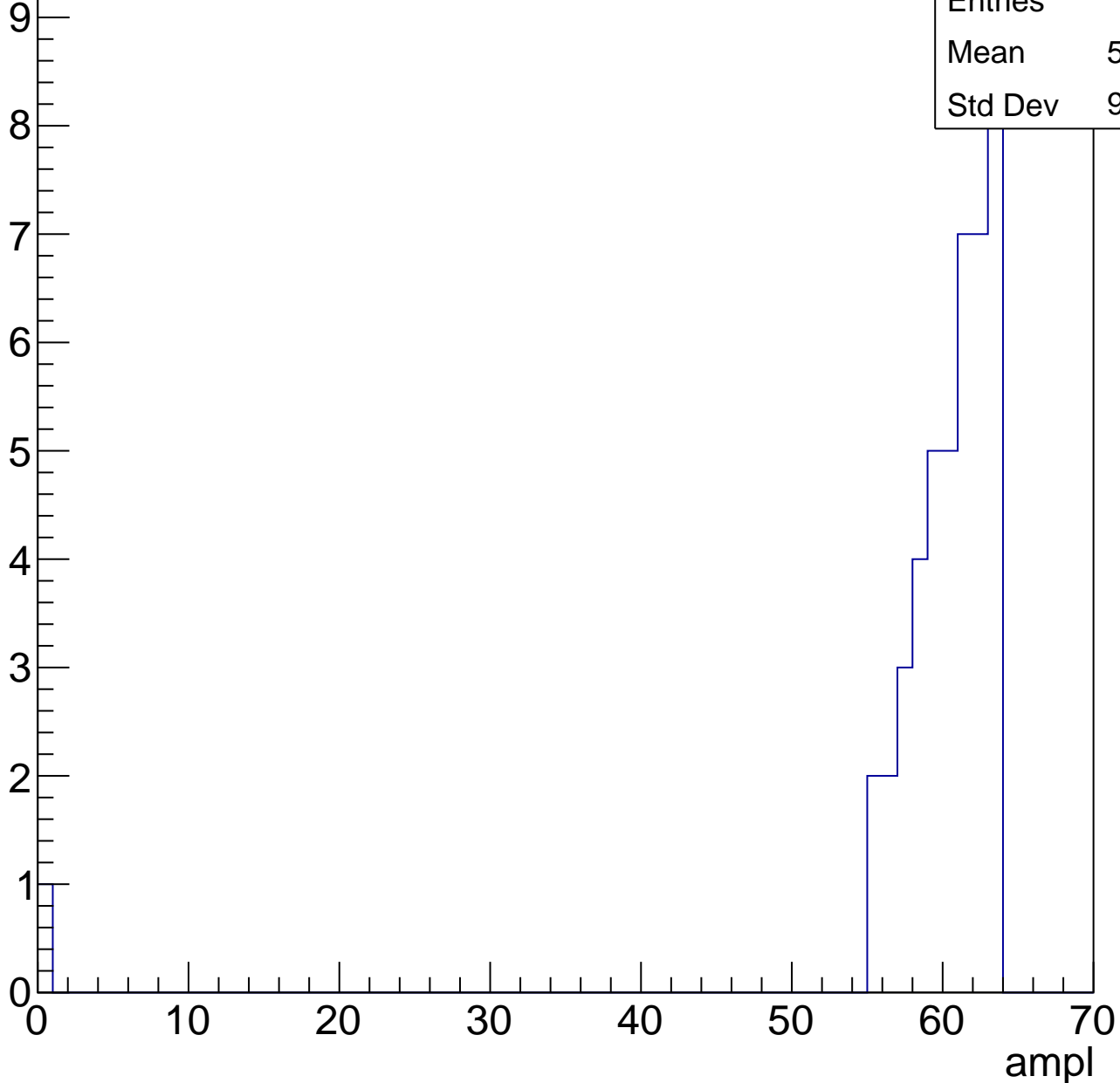


# B1L003S, U18-ch103, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	45
Mean	58.84
Std Dev	9.172



# B1L003S, U18-ch103, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U18-ch103, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L003S, U18-ch104, adc0

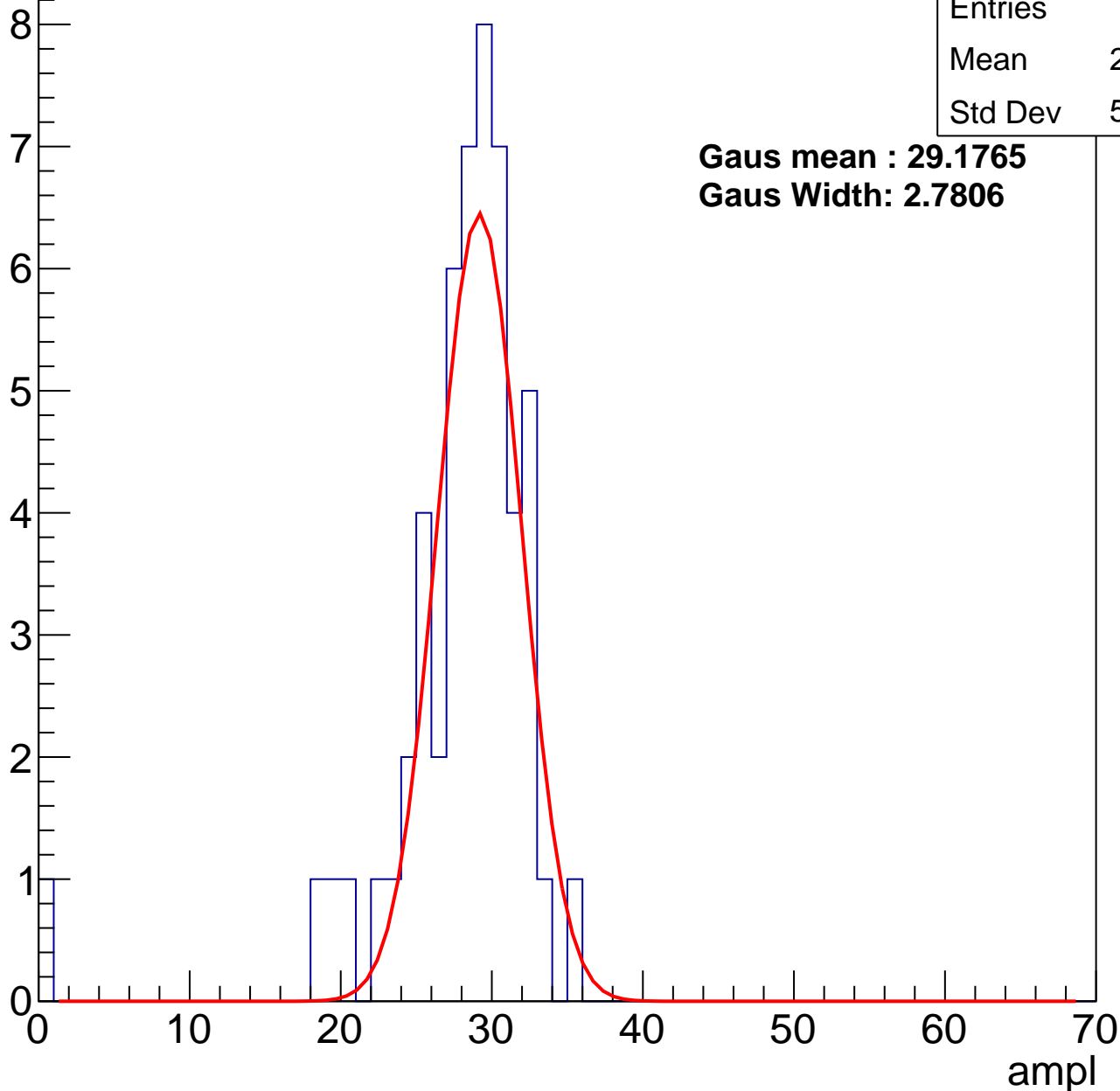
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	53
Mean	27.43
Std Dev	5.105

**Gaus mean : 29.1765**

**Gaus Width: 2.7806**



# B1L003S, U18-ch104, adc1

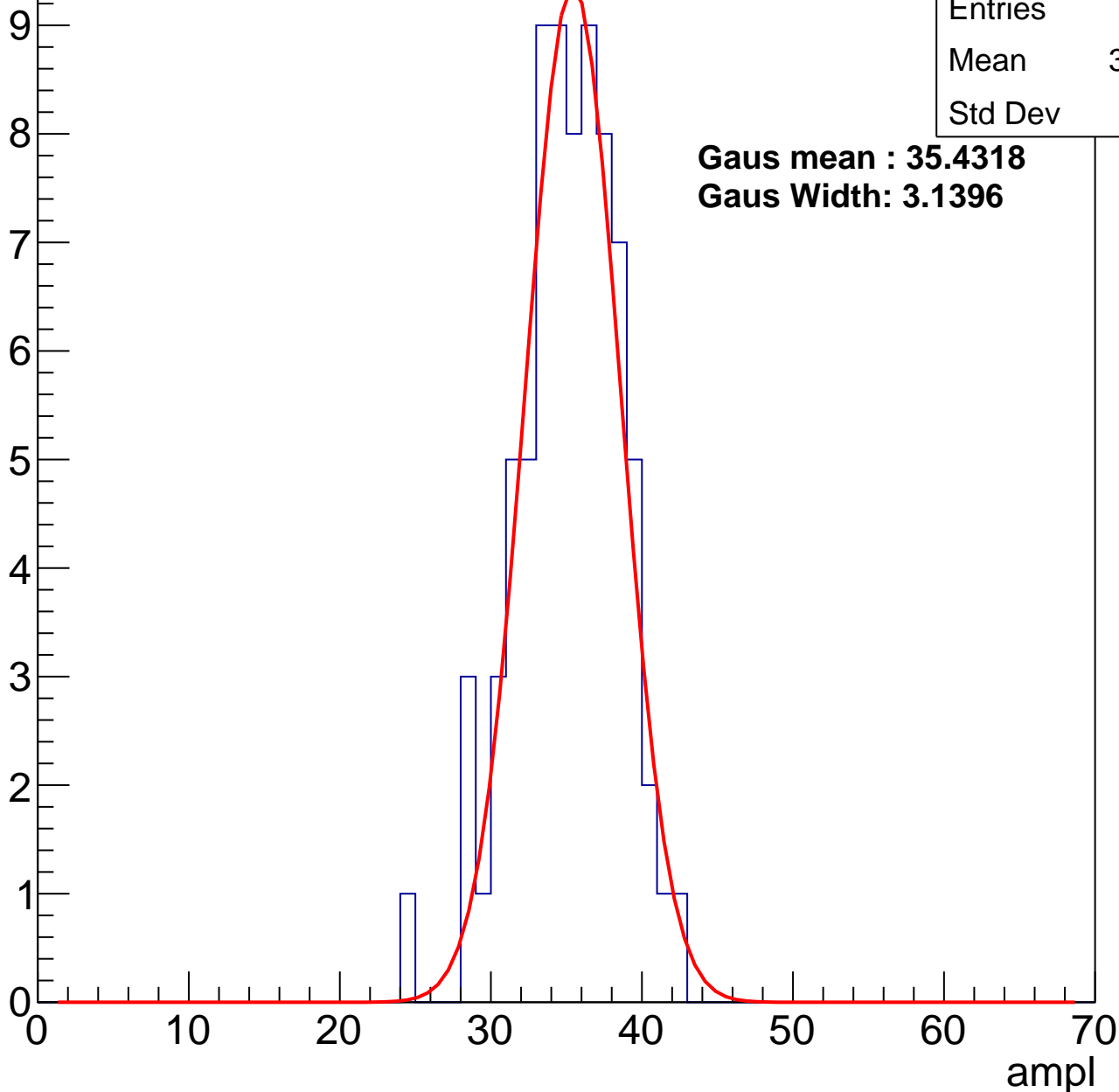
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	77
Mean	34.66
Std Dev	3.34

**Gaus mean : 35.4318**

**Gaus Width: 3.1396**



# B1L003S, U18-ch104, adc2

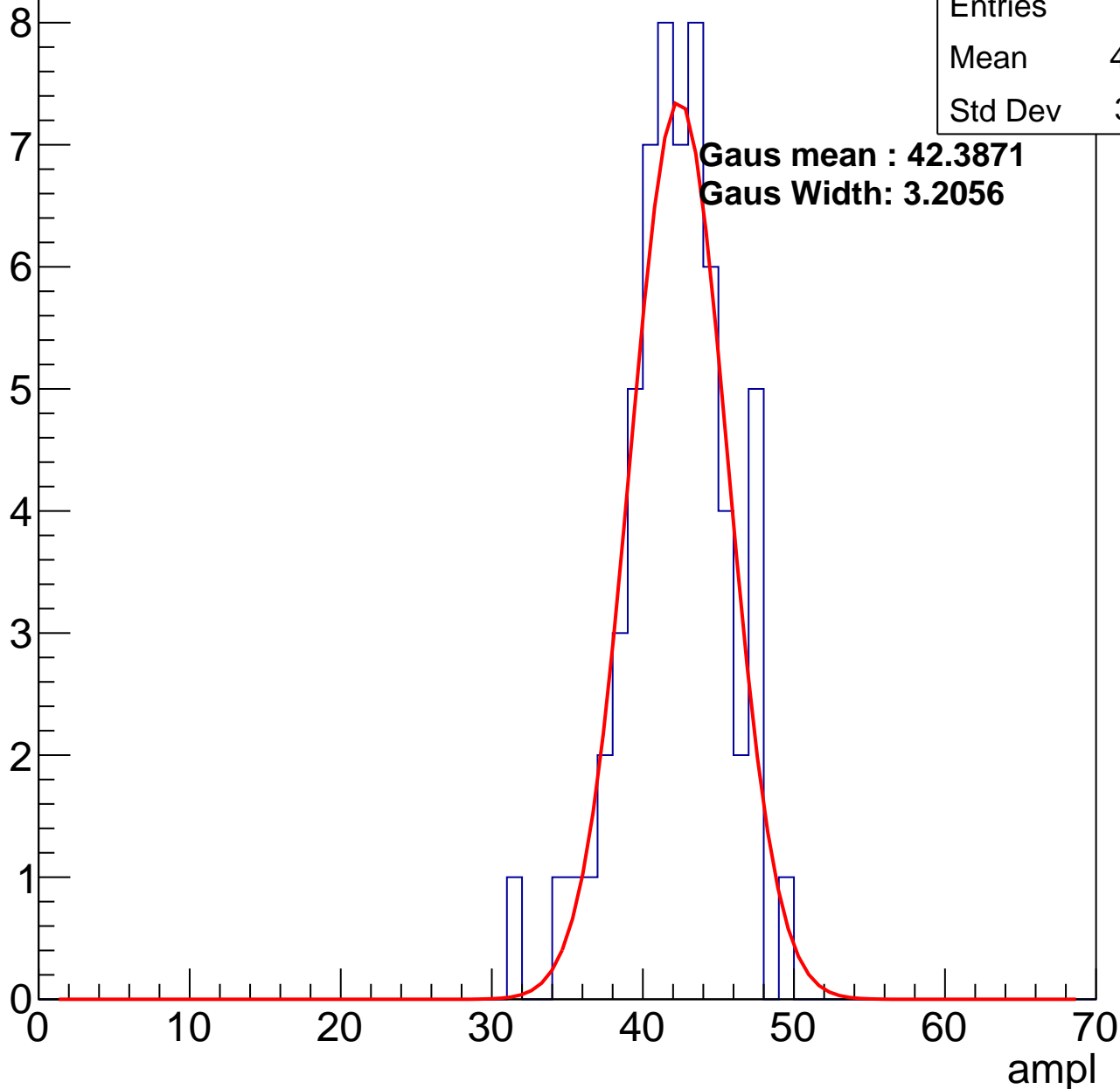
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	62
Mean	41.69
Std Dev	3.401

**Gaus mean : 42.3871**

**Gaus Width: 3.2056**

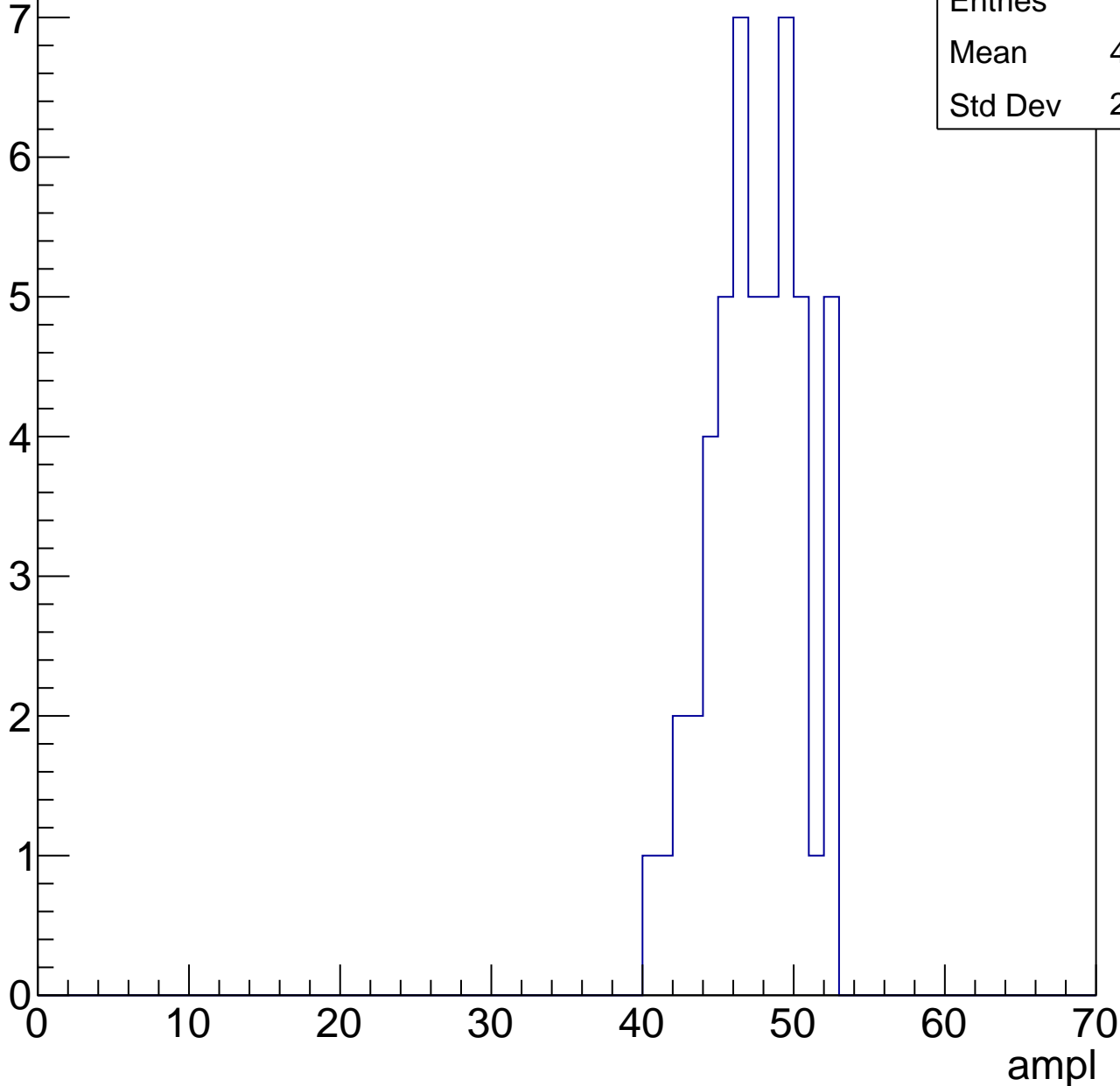


# B1L003S, U18-ch104, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	50
Mean	47.06
Std Dev	2.996

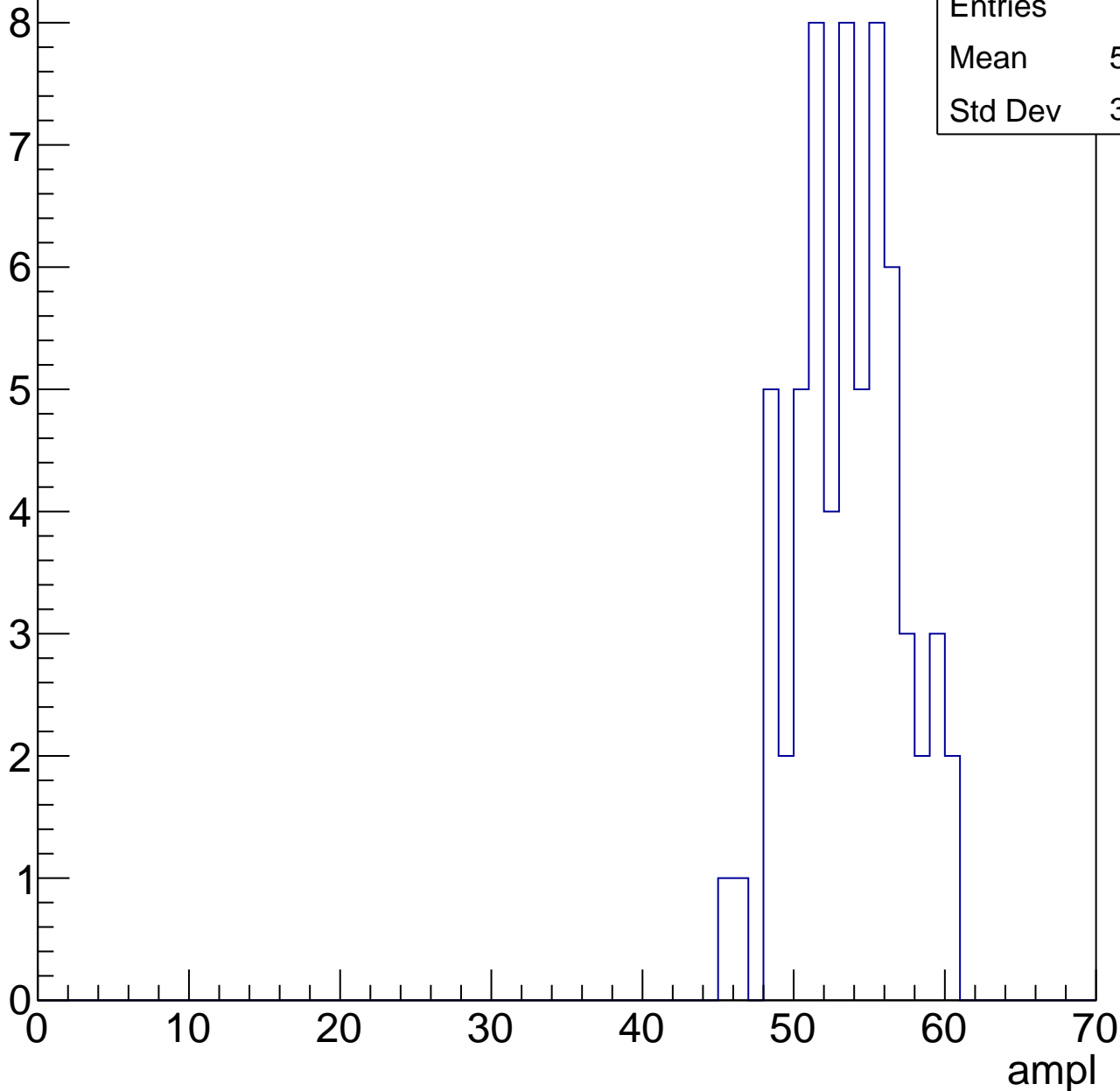


# B1L003S, U18-ch104, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	63
Mean	53.16
Std Dev	3.437

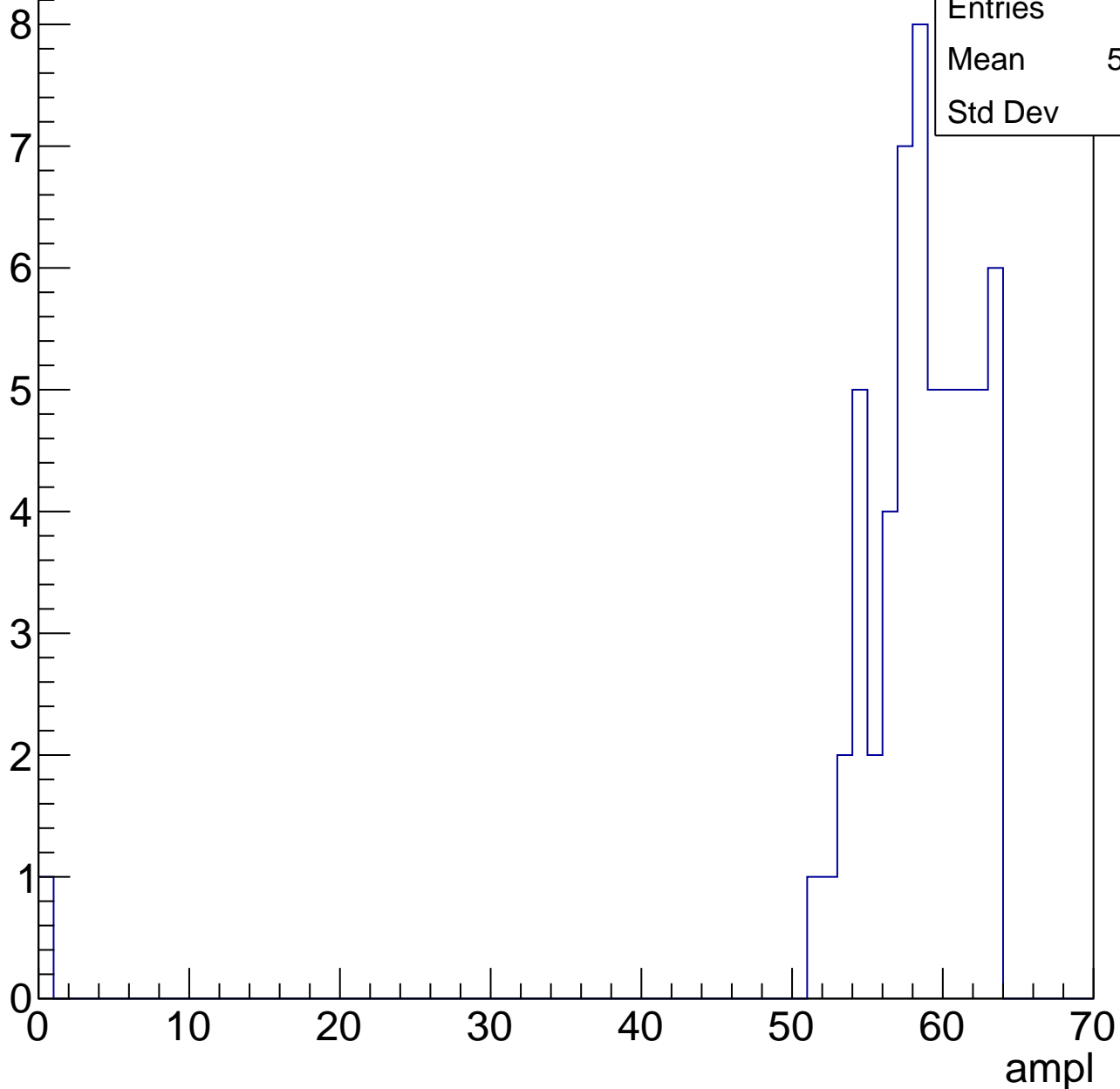


# B1L003S, U18-ch104, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	57
Mean	57.26
Std Dev	8.26

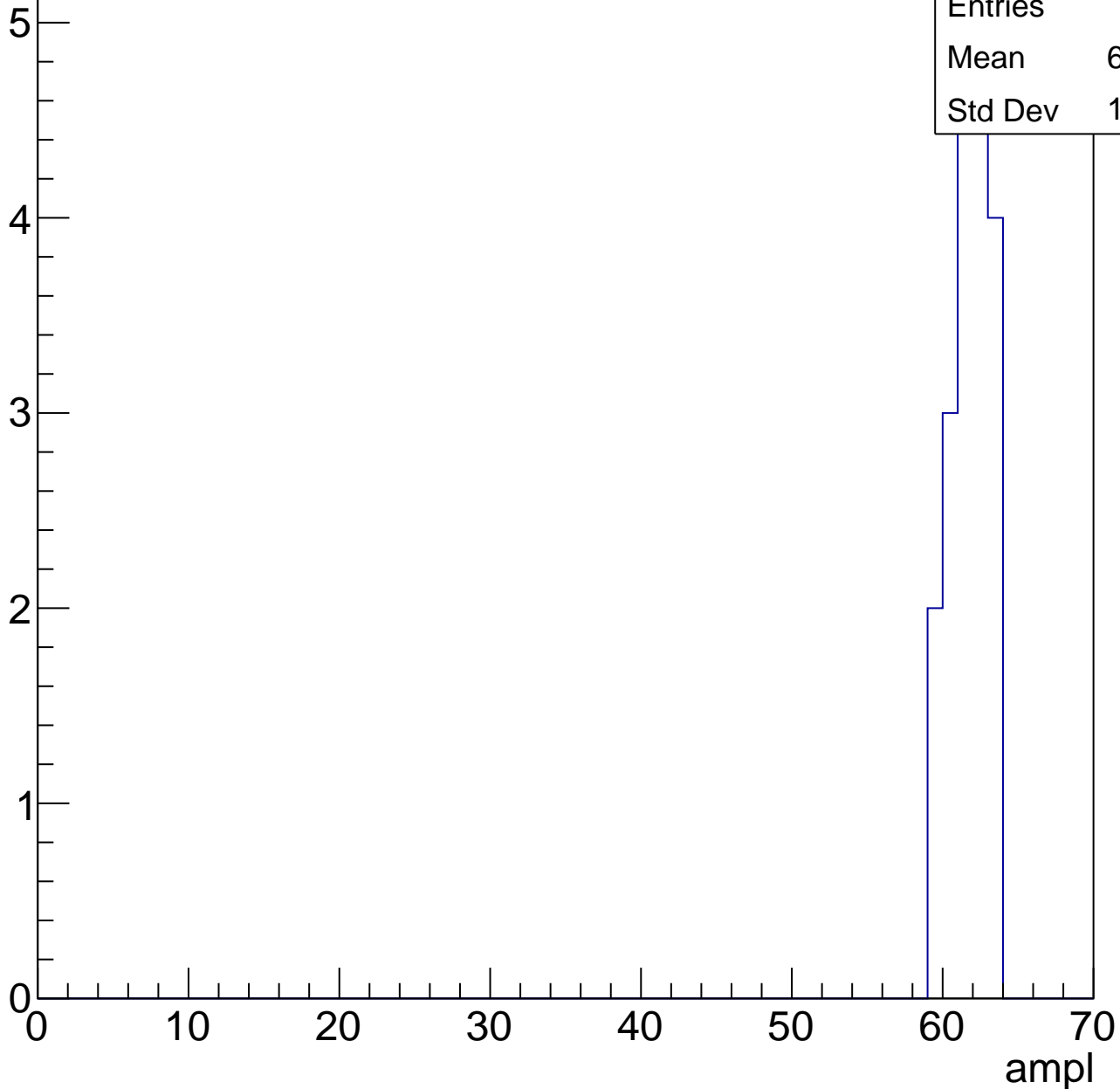


# B1L003S, U18-ch104, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	19
Mean	61.32
Std Dev	1.259





# B1L003S, U18-ch104, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch105, adc0

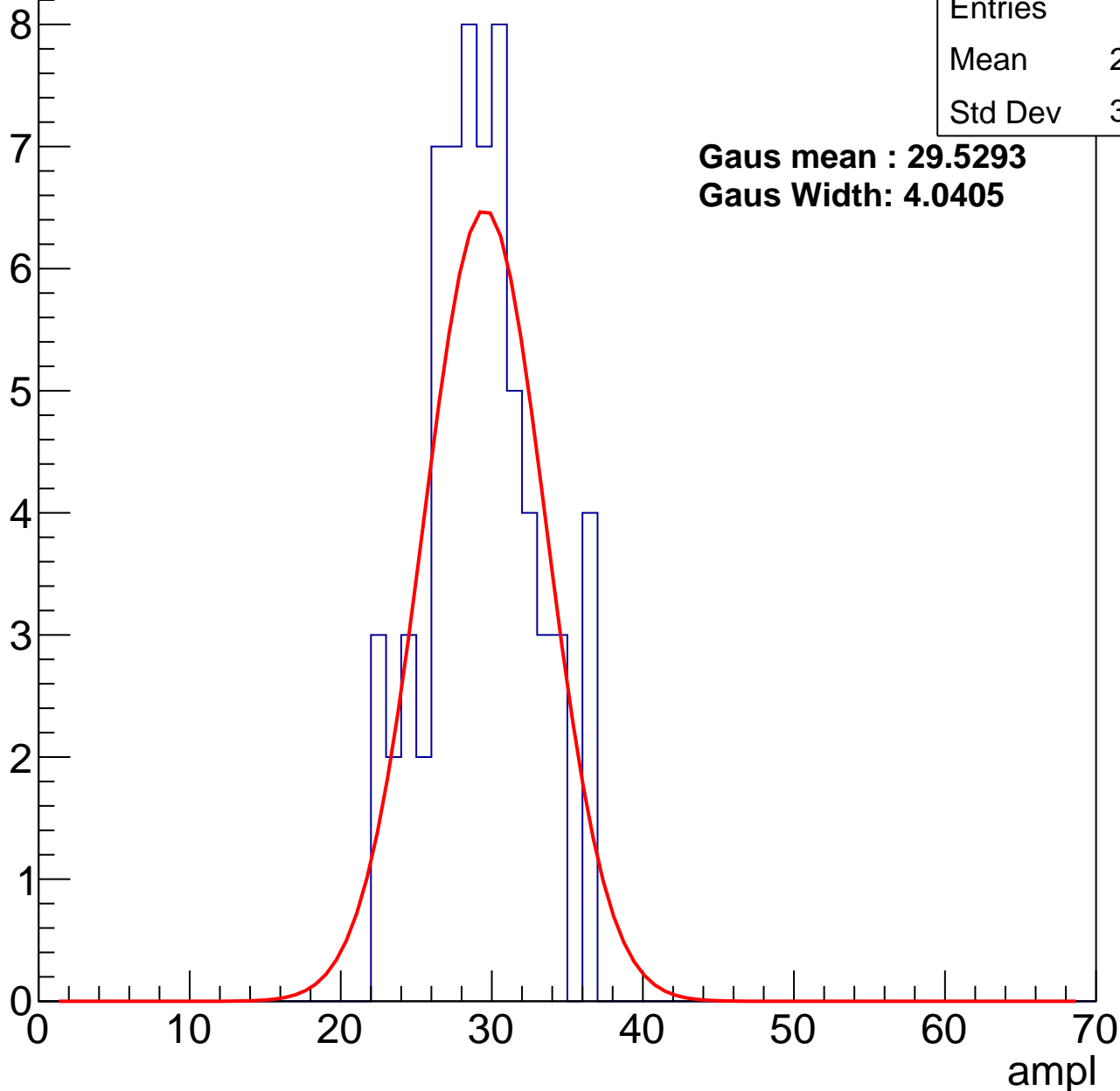
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	66
Mean	28.79
Std Dev	3.492

**Gaus mean : 29.5293**

**Gaus Width: 4.0405**



# B1L003S, U18-ch105, adc1

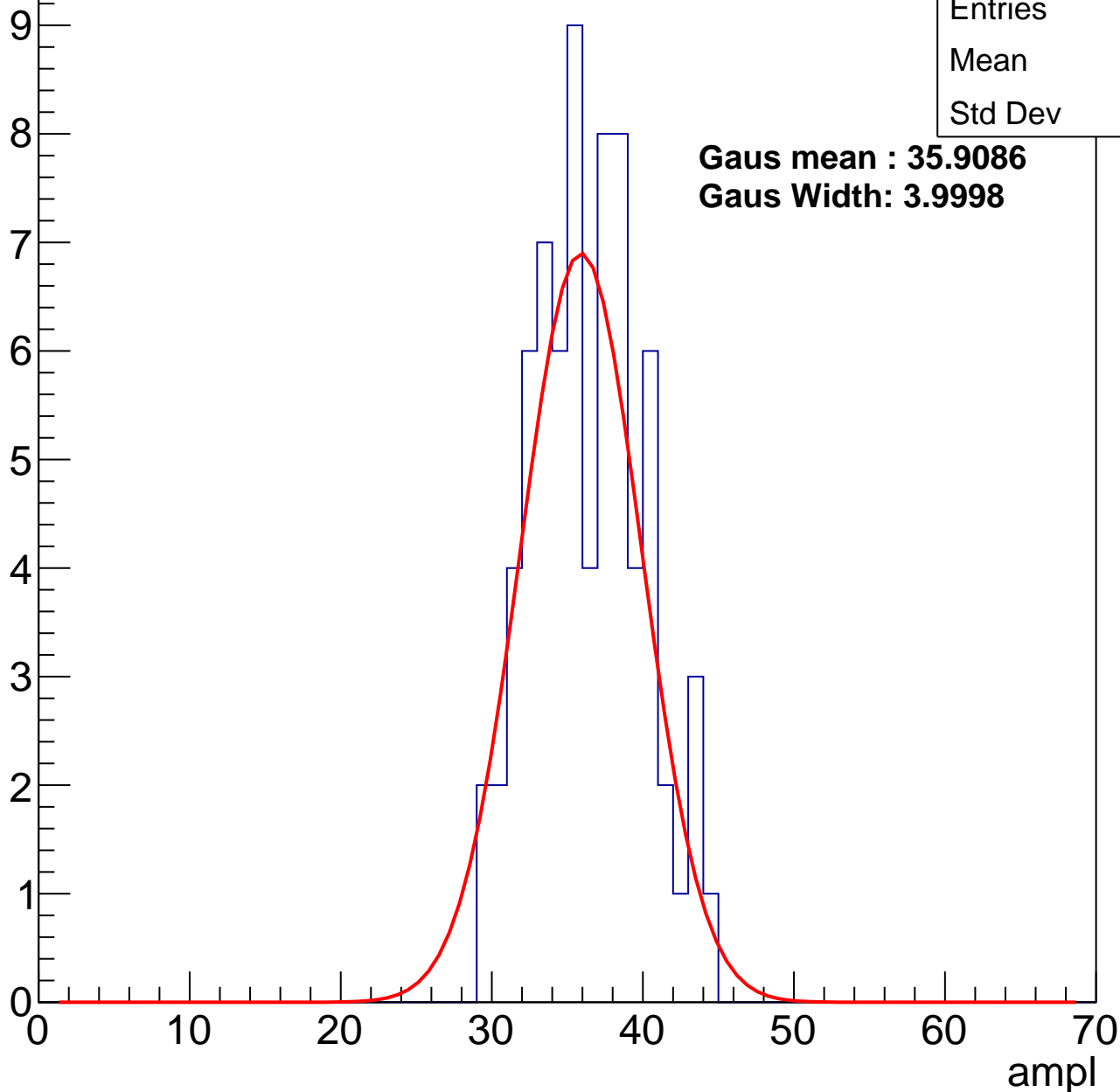
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	73
Mean	35.9
Std Dev	3.57

**Gaus mean : 35.9086**

**Gaus Width: 3.9998**



# B1L003S, U18-ch105, adc2

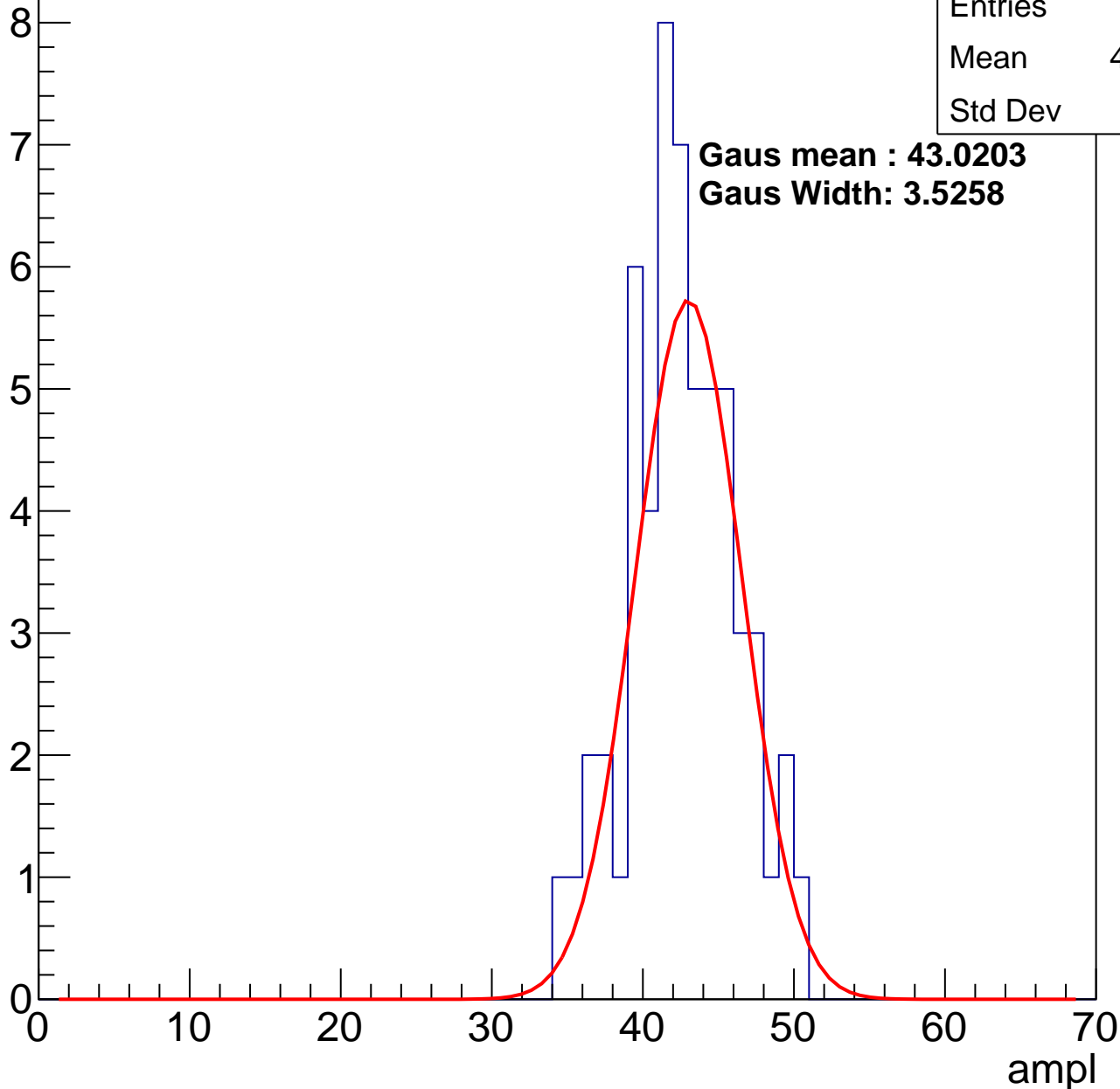
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	57
Mean	42.18
Std Dev	3.55

**Gaus mean : 43.0203**

**Gaus Width: 3.5258**

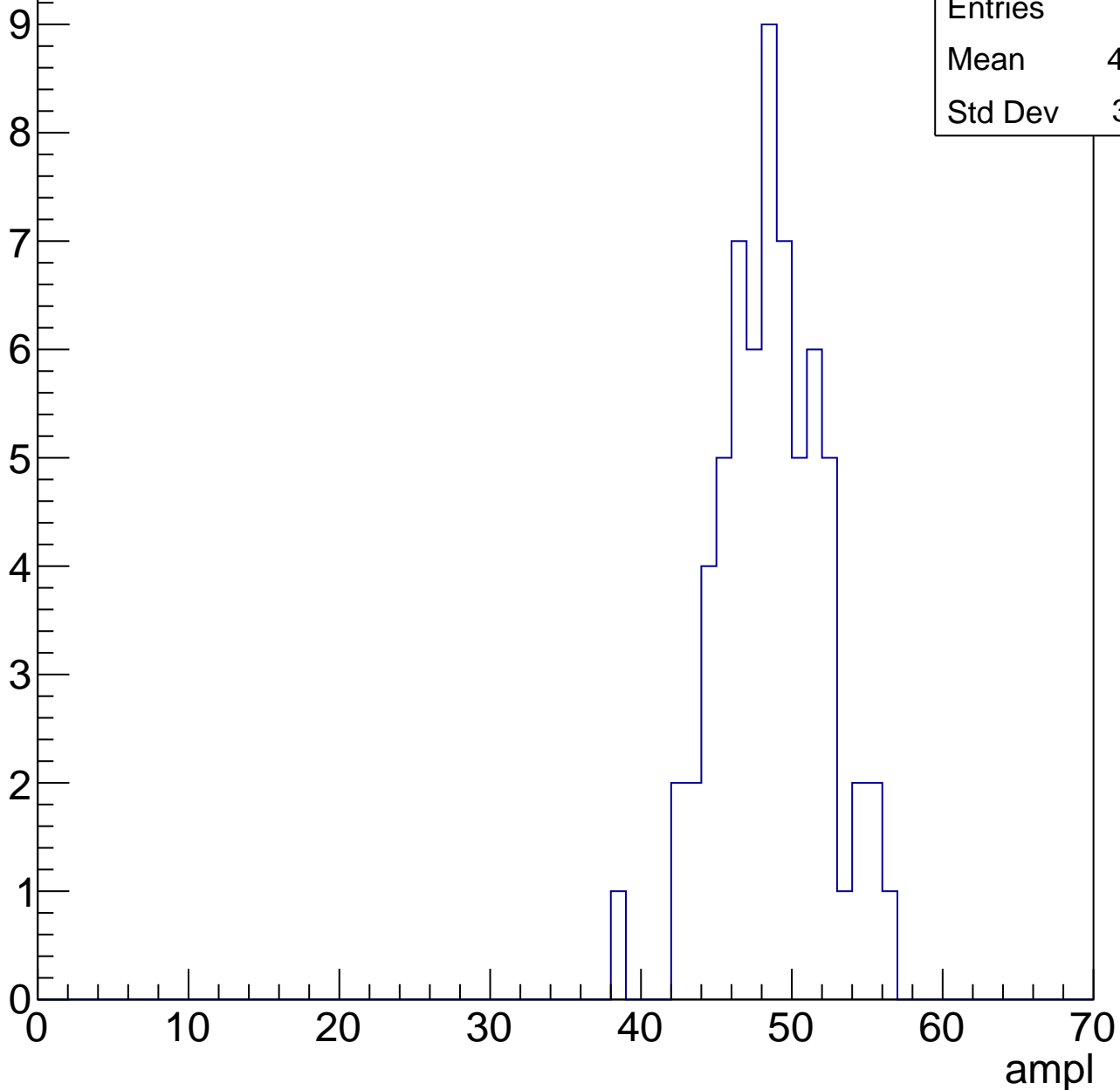


# B1L003S, U18-ch105, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	65
Mean	48.17
Std Dev	3.471

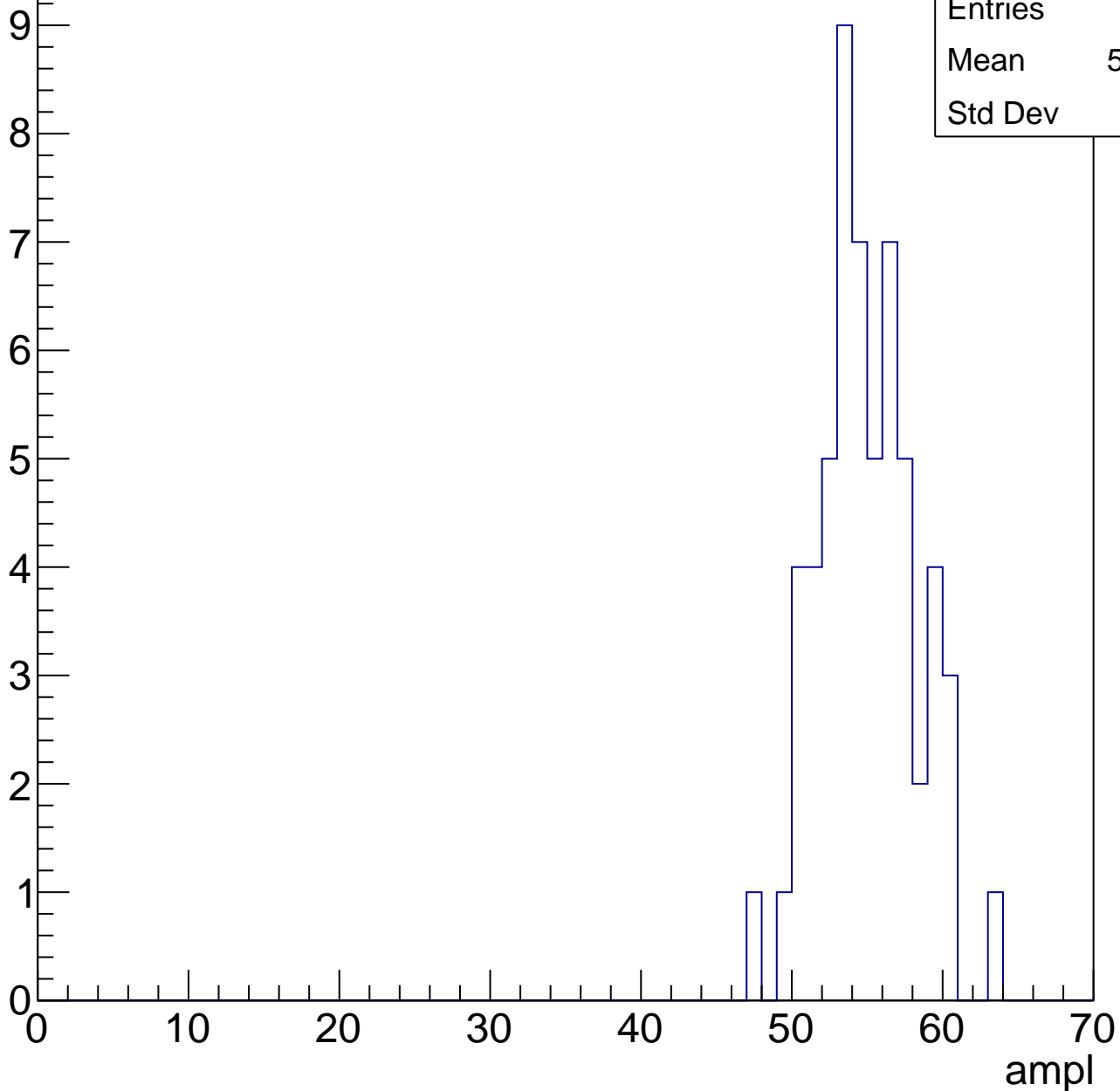


# B1L003S, U18-ch105, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	58
Mean	54.52
Std Dev	3.18

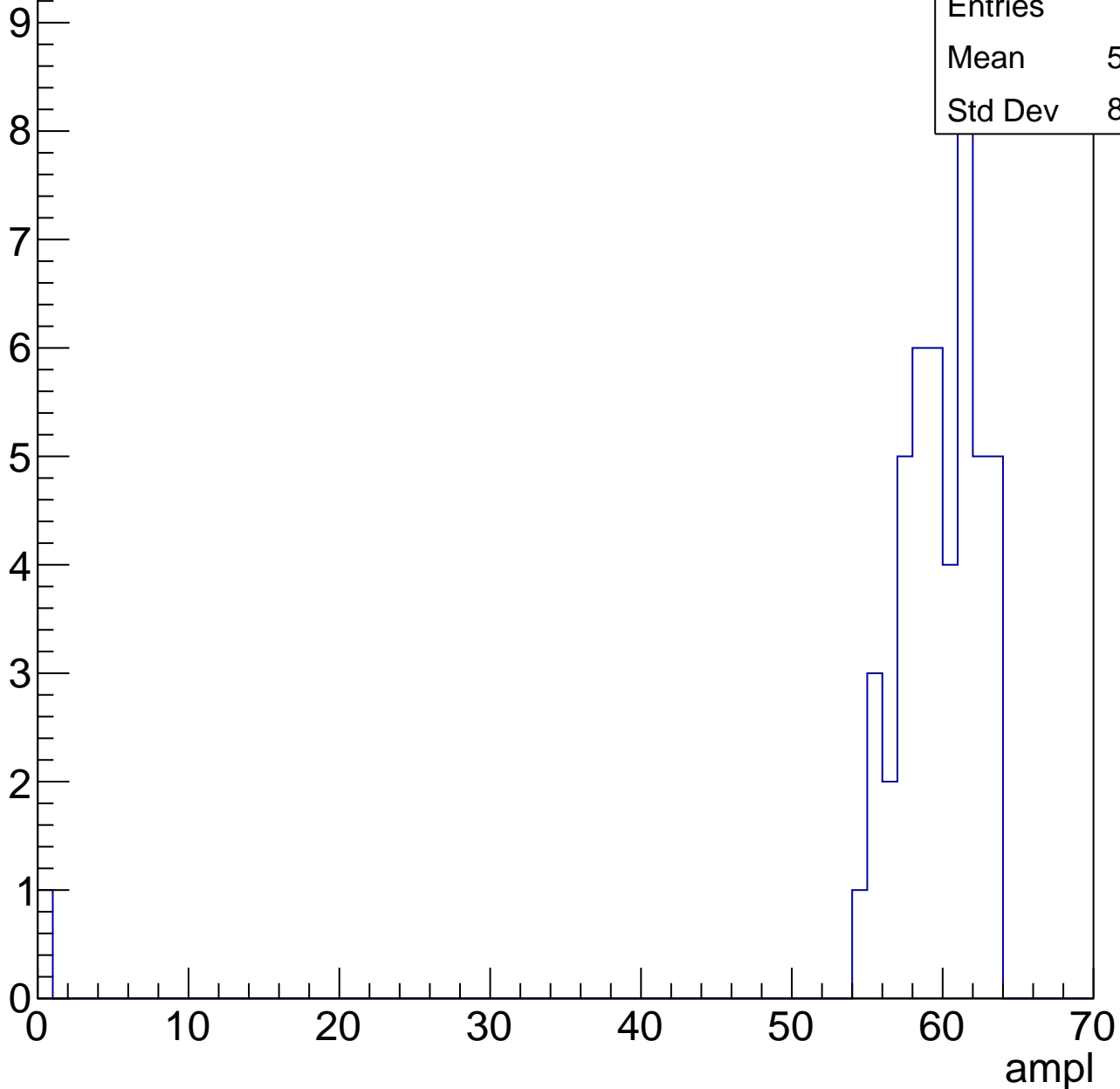


# B1L003S, U18-ch105, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	47
Mean	58.13
Std Dev	8.905

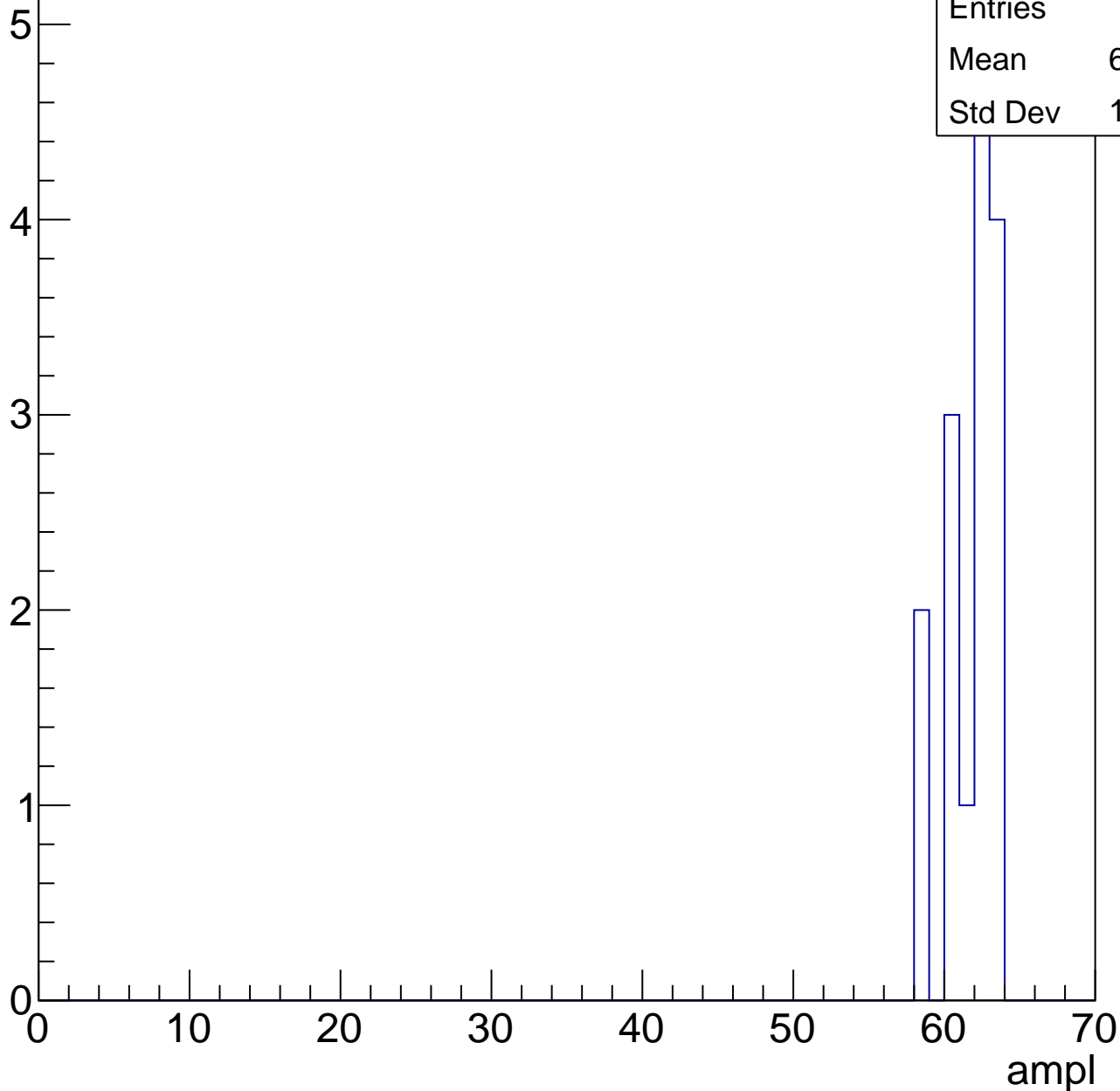


# B1L003S, U18-ch105, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	15
Mean	61.27
Std Dev	1.652





# B1L003S, U18-ch105, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L003S, U18-ch106, adc0

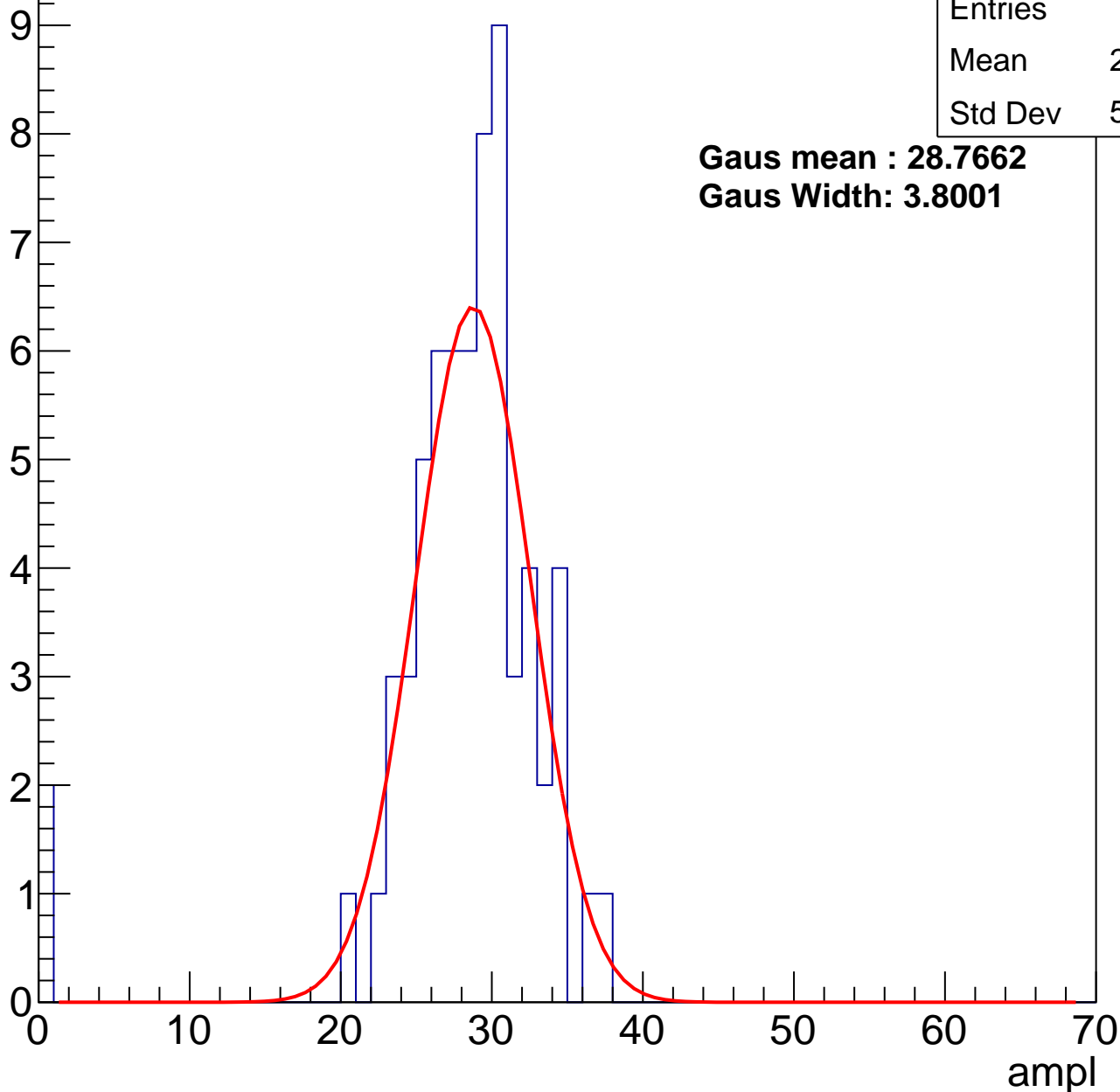
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	65
Mean	27.57
Std Dev	5.985

**Gaus mean : 28.7662**

**Gaus Width: 3.8001**



# B1L003S, U18-ch106, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	67
Mean	35.46
Std Dev	3.014

**Gaus mean : 34.7585**

**Gaus Width: 3.8369**

10

8

6

4

2

0

0

10

20

30

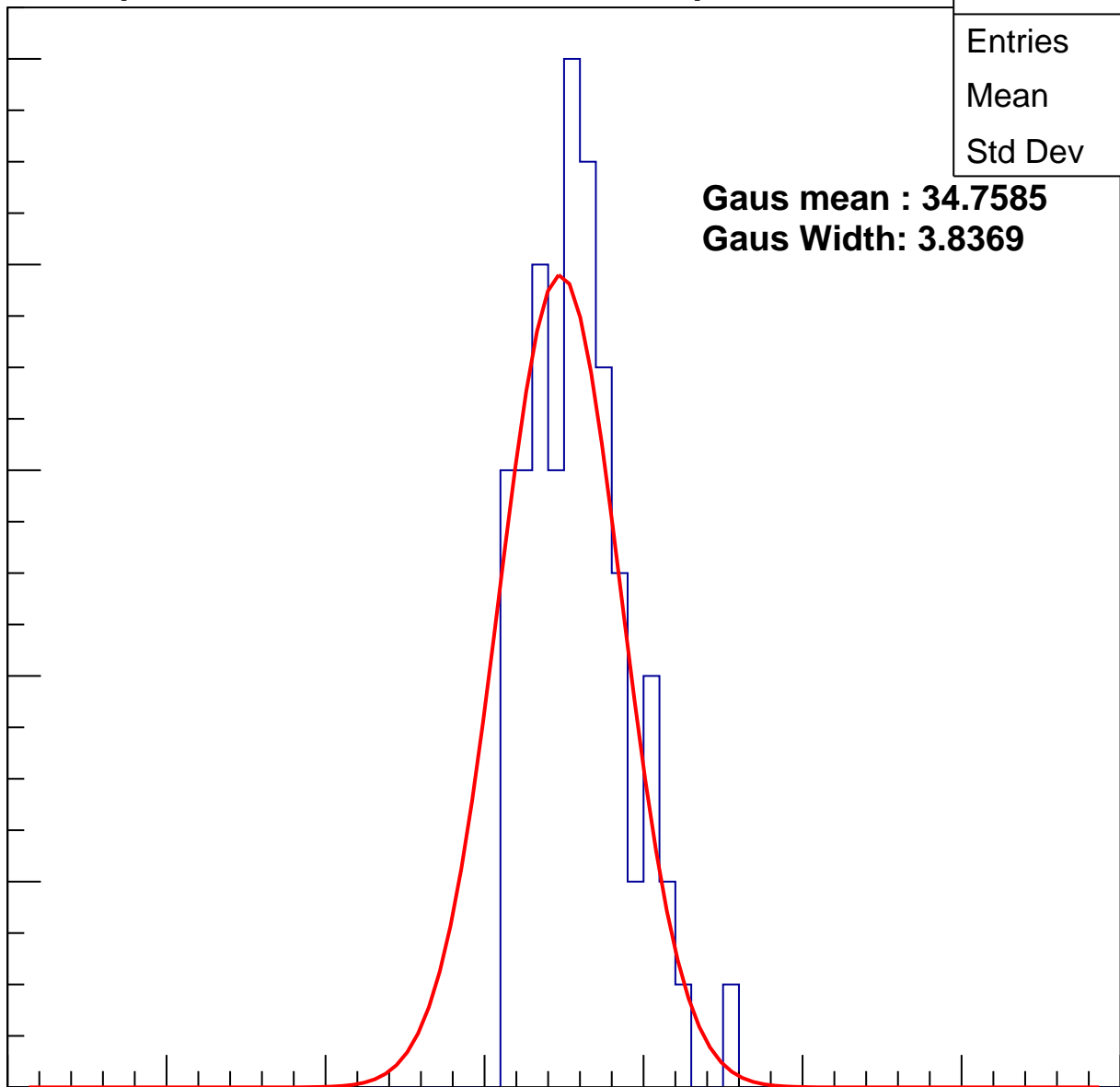
40

50

60

70

ampl



# B1L003S, U18-ch106, adc2

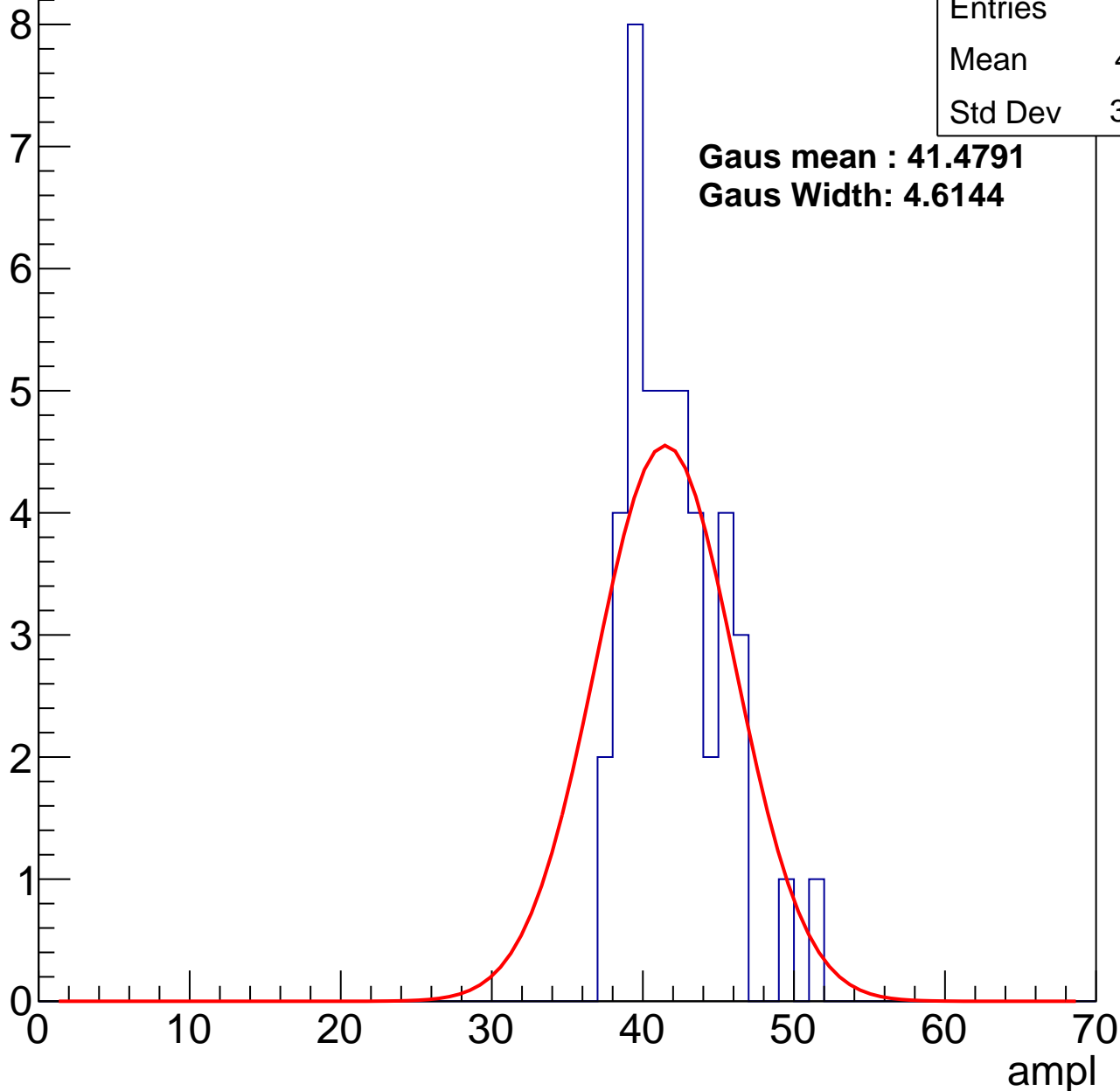
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	44
Mean	41.61
Std Dev	3.128

**Gaus mean : 41.4791**

**Gaus Width: 4.6144**

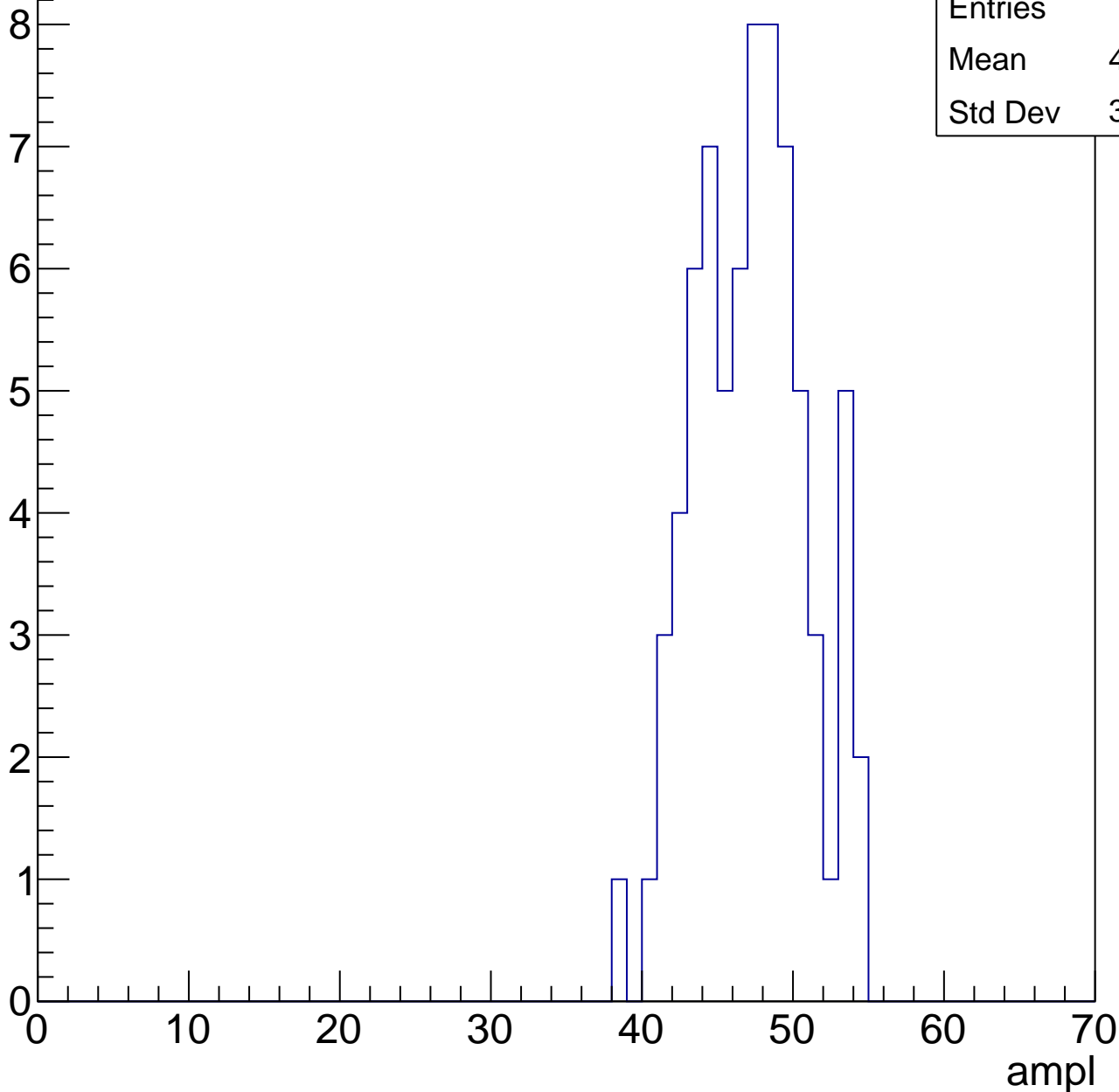


# B1L003S, U18-ch106, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	72
Mean	46.76
Std Dev	3.634

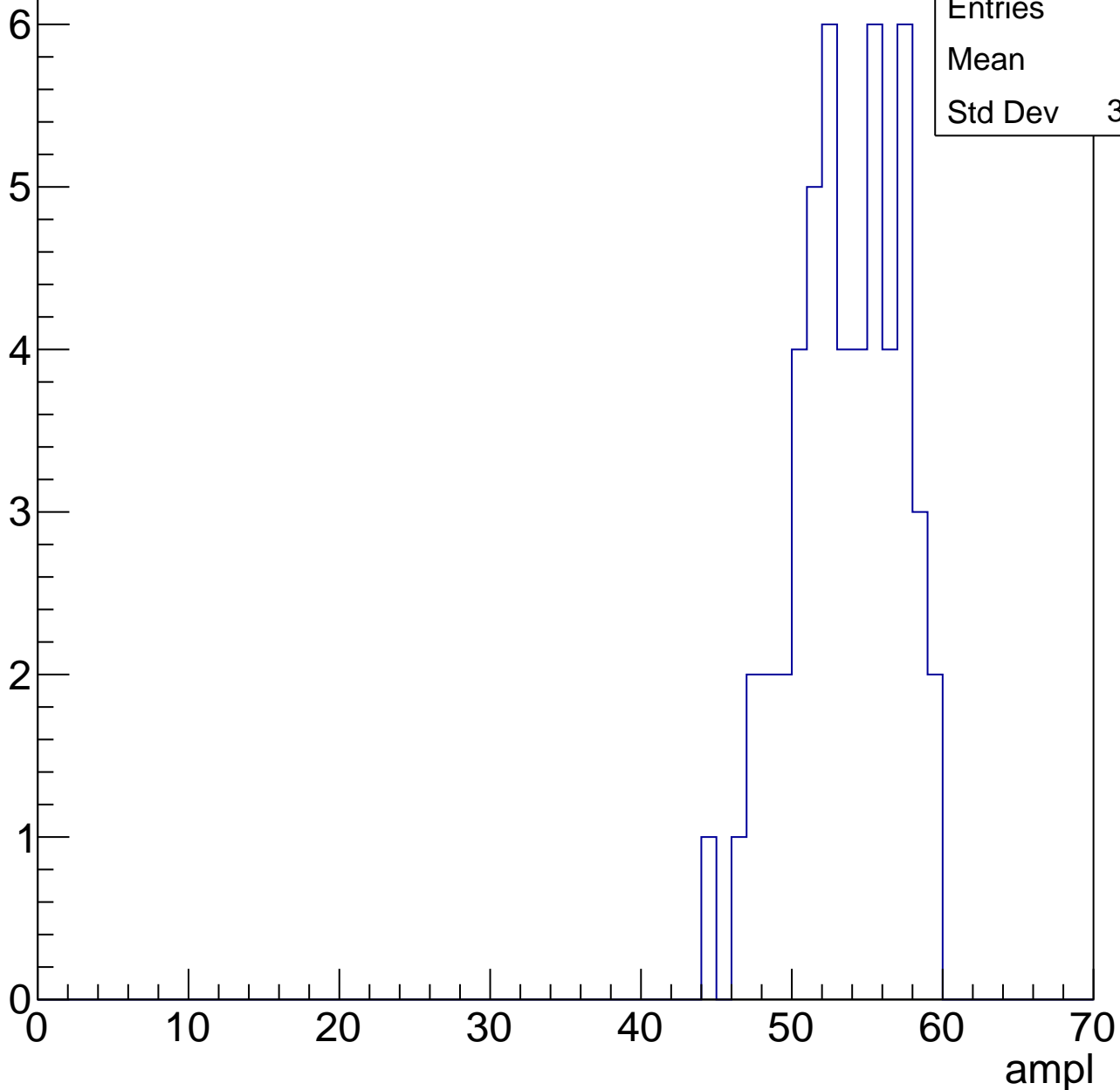


# B1L003S, U18-ch106, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	52
Mean	53.1
Std Dev	3.542

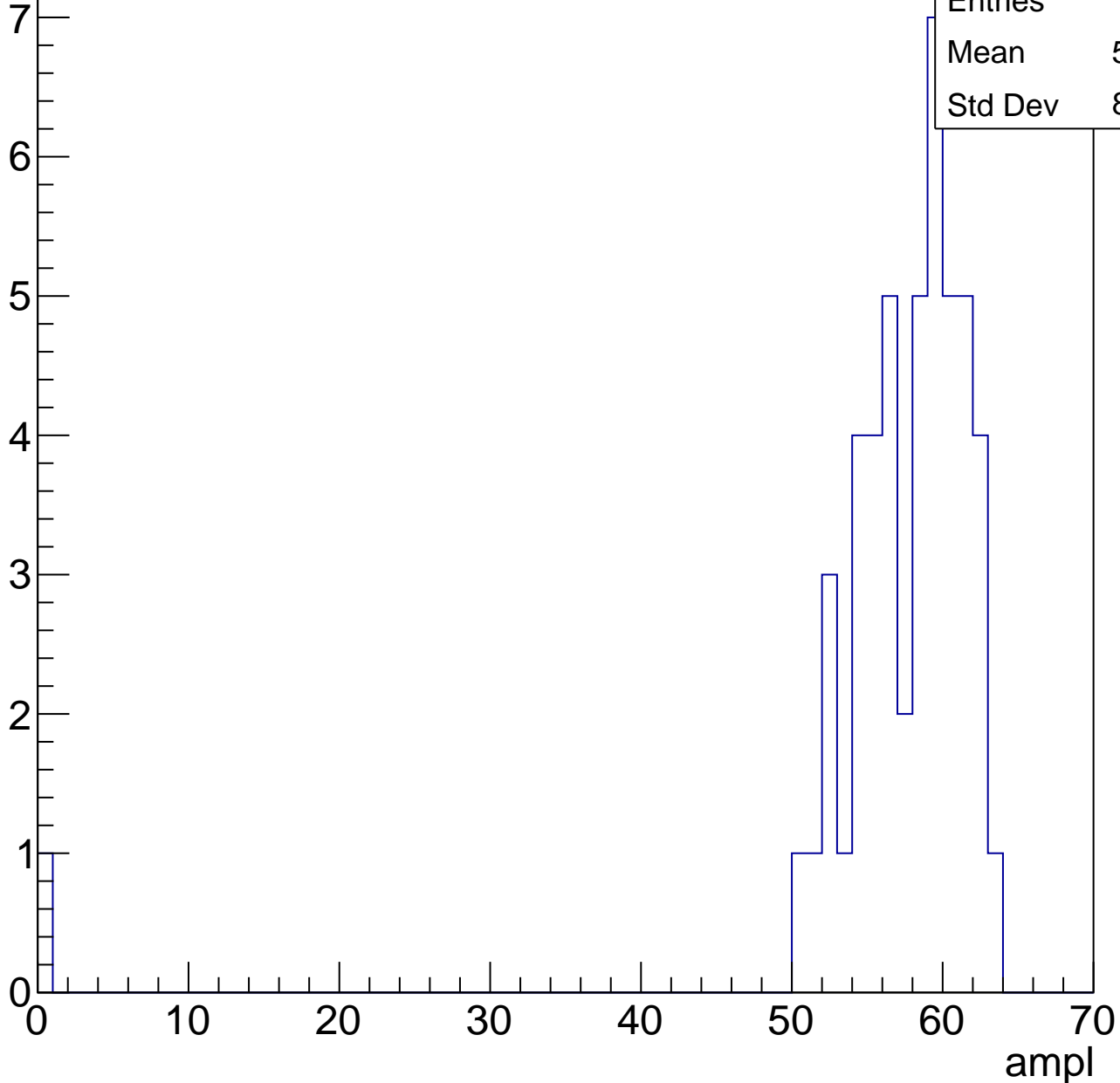


# B1L003S, U18-ch106, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	49
Mean	56.31
Std Dev	8.751

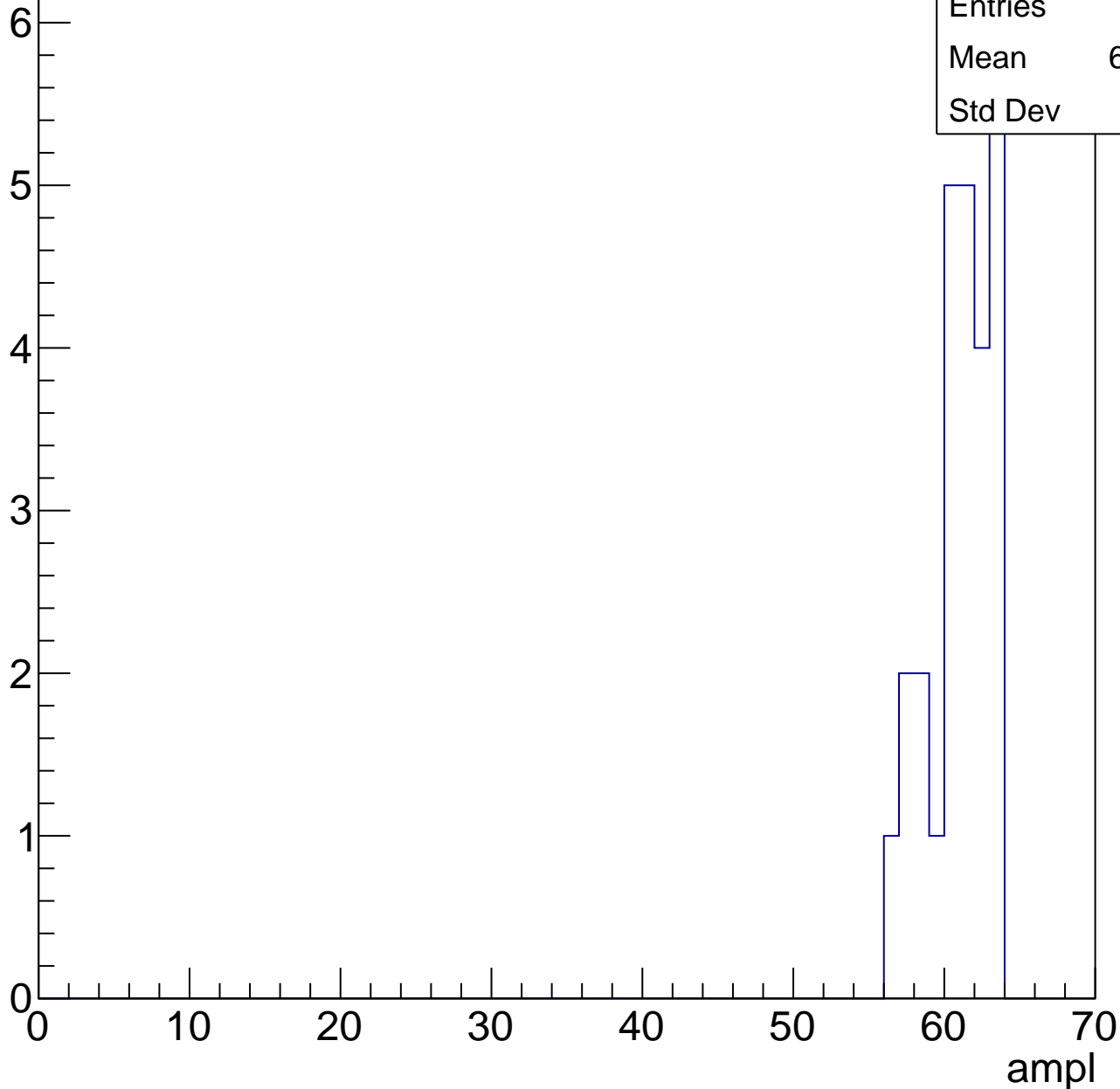


# B1L003S, U18-ch106, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	26
Mean	60.62
Std Dev	2.04

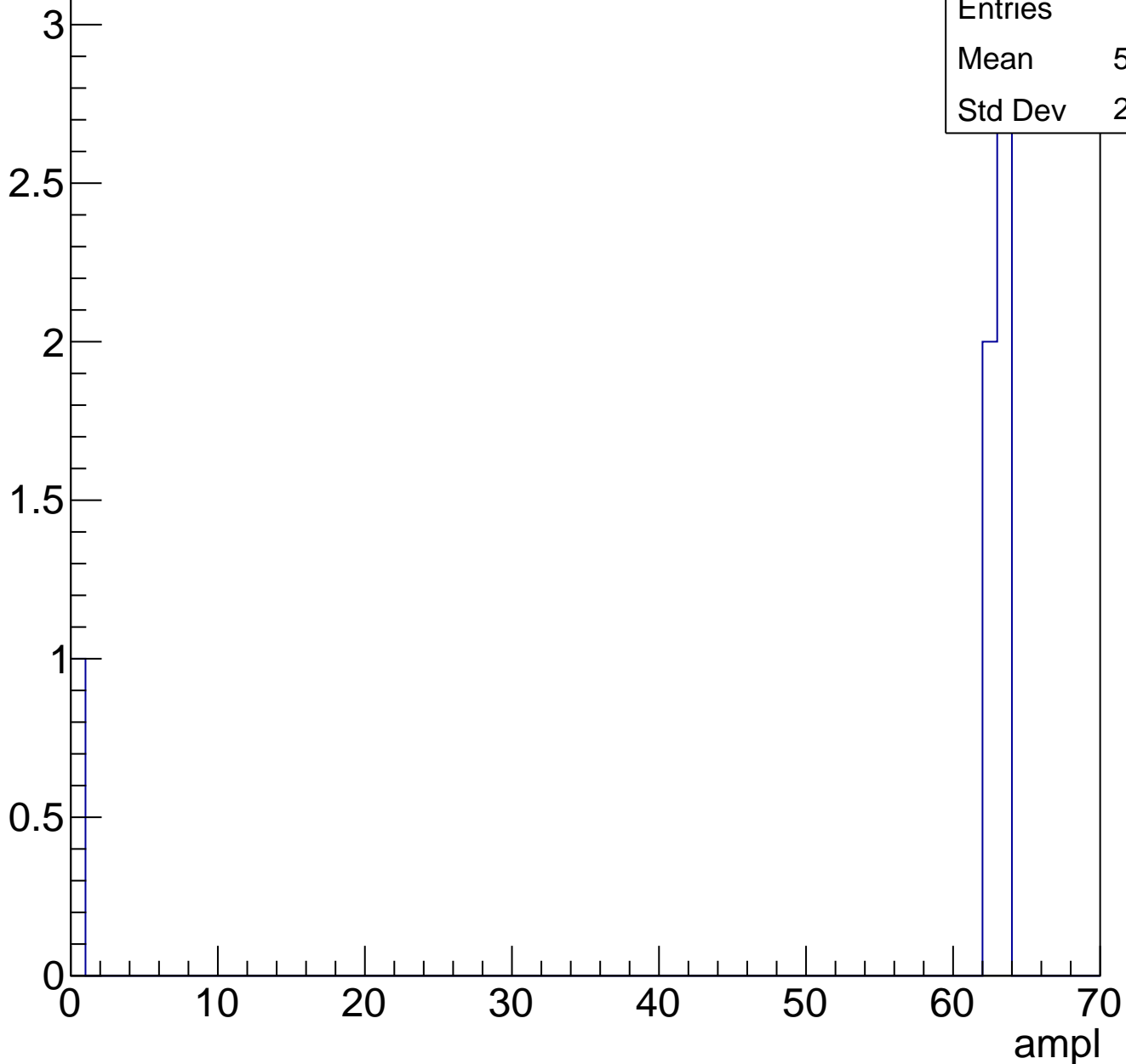




# B1L003S, U18-ch106, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U18-ch107, adc0

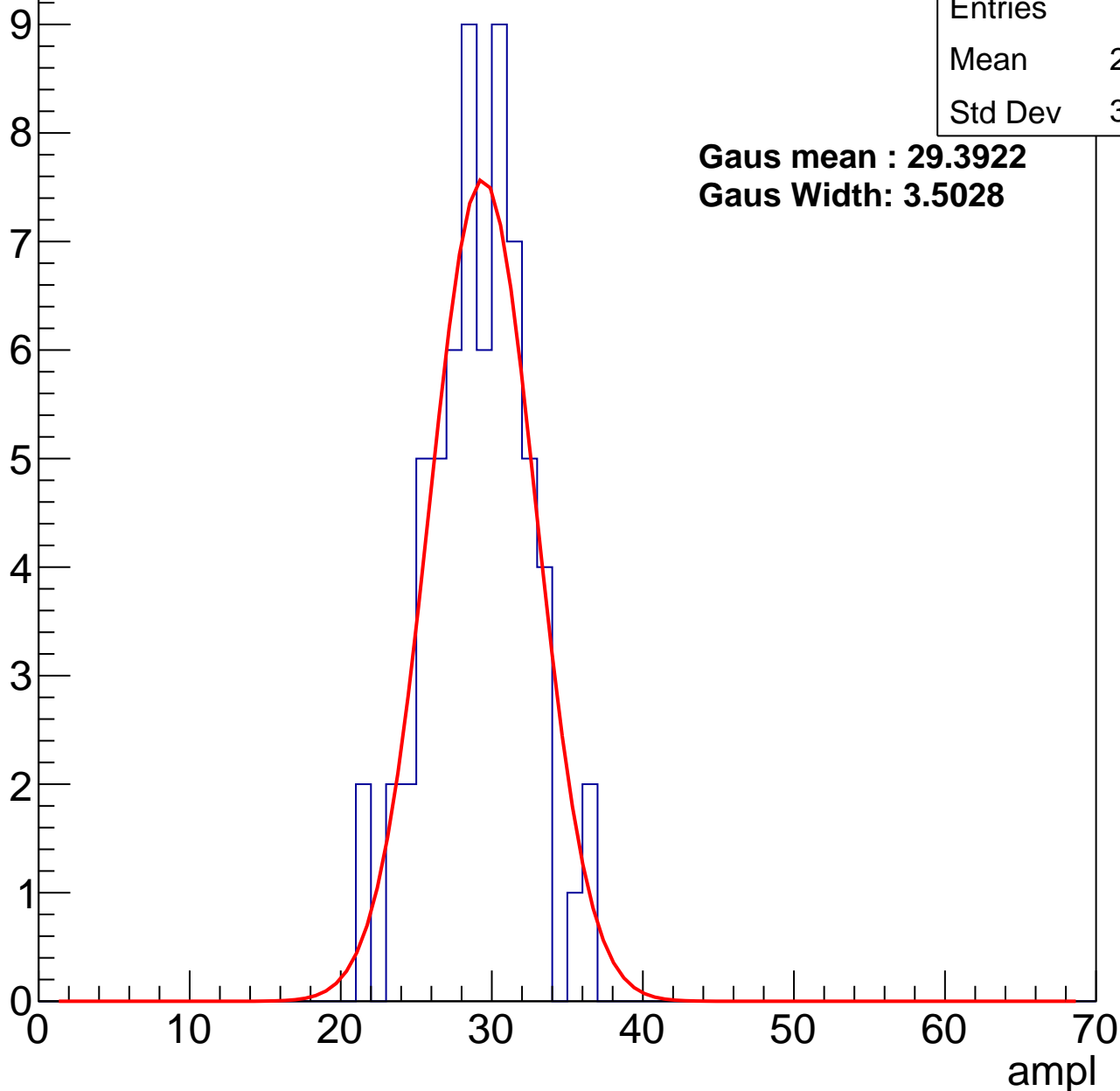
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	65
Mean	28.69
Std Dev	3.239

**Gaus mean : 29.3922**

**Gaus Width: 3.5028**



# B1L003S, U18-ch107, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	71
Mean	35.23
Std Dev	3.238

**Gaus mean : 35.4210**

**Gaus Width: 3.0322**

Entry

10  
8  
6  
4  
2  
0

ampl

0

10

20

30

40

50

60

70

# B1L003S, U18-ch107, adc2

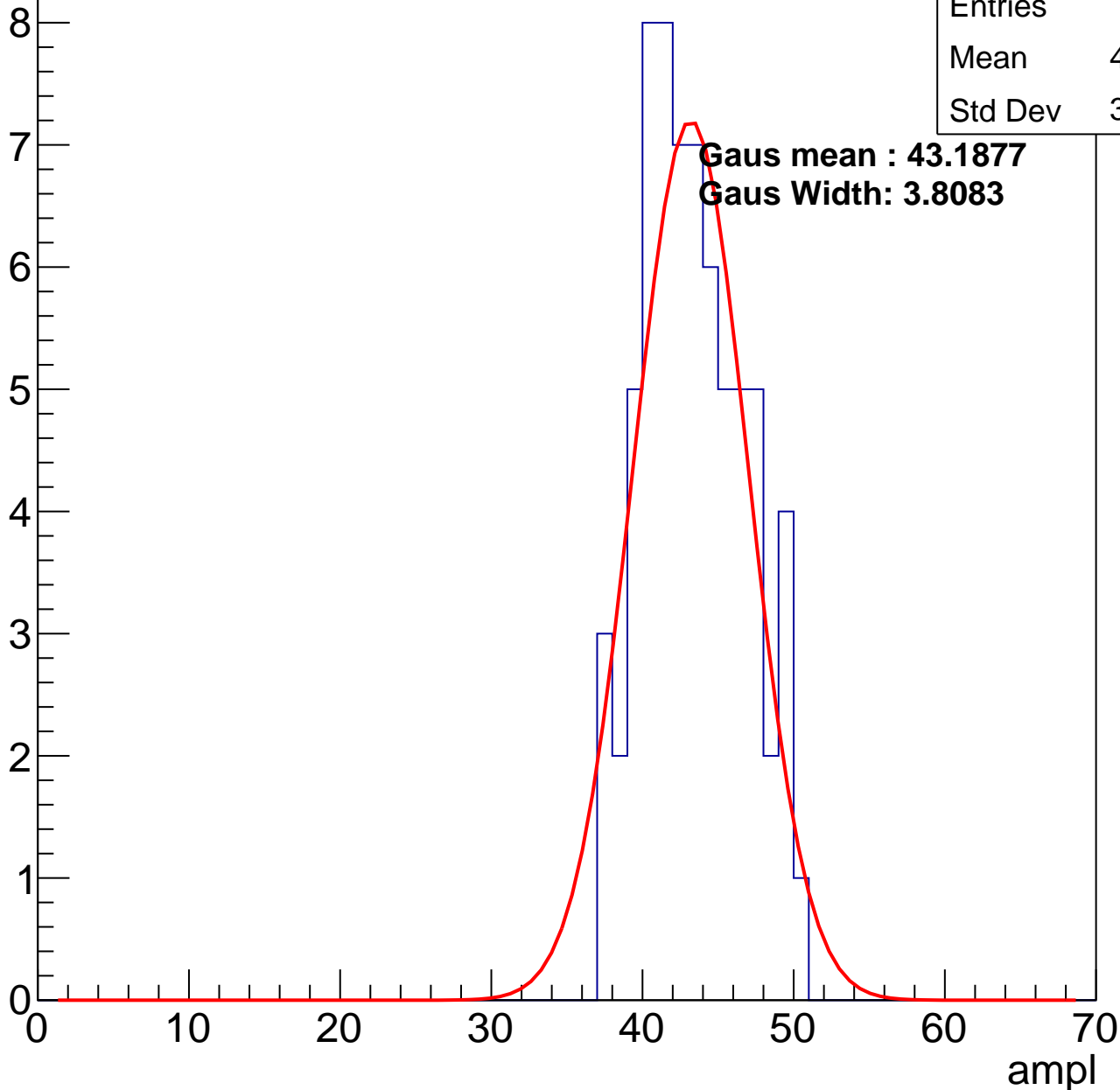
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	68
Mean	42.96
Std Dev	3.305

**Gaus mean : 43.1877**

**Gaus Width: 3.8083**

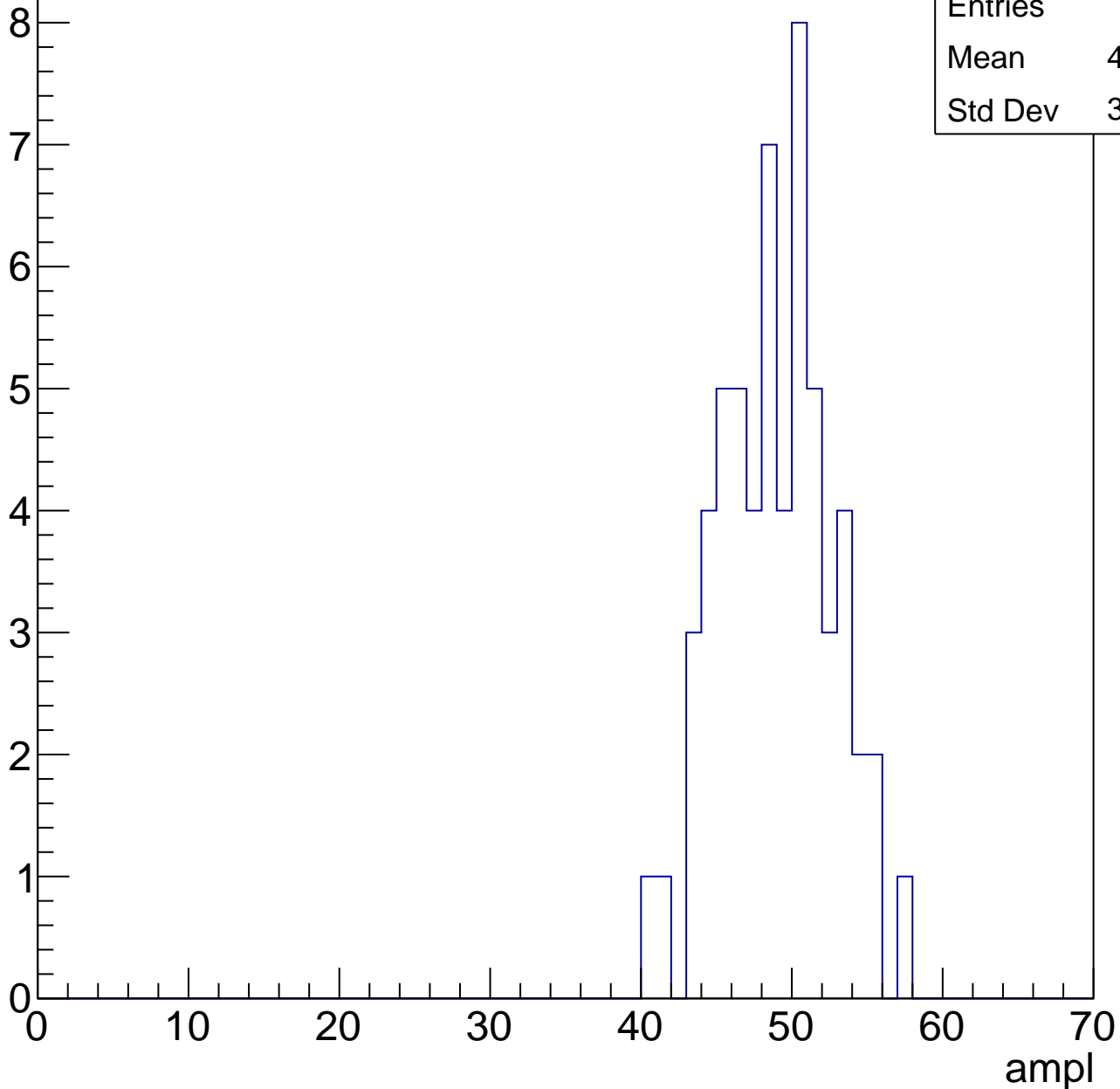


# B1L003S, U18-ch107, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	59
Mean	48.46
Std Dev	3.656

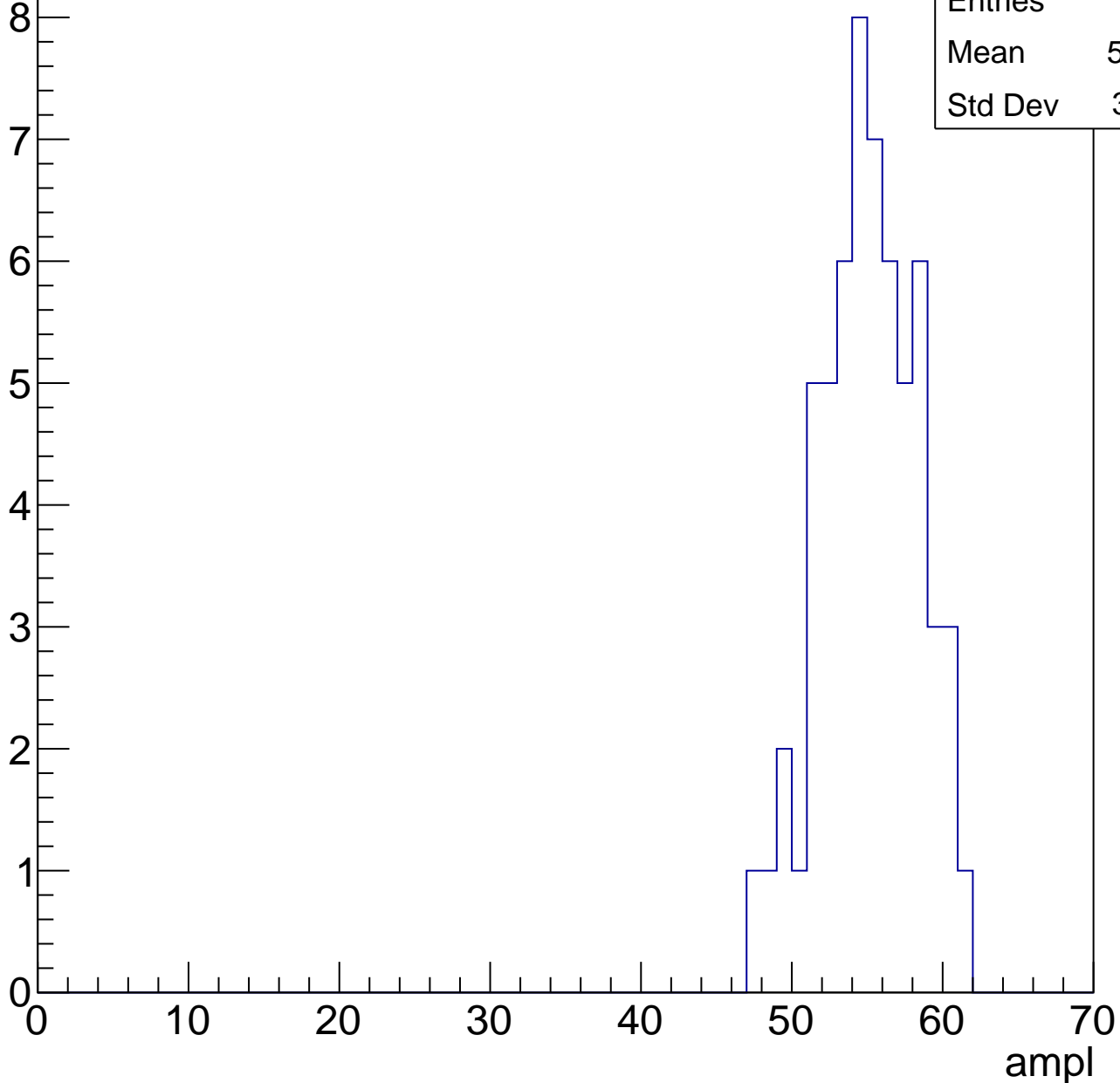


# B1L003S, U18-ch107, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	60
Mean	54.67
Std Dev	3.161

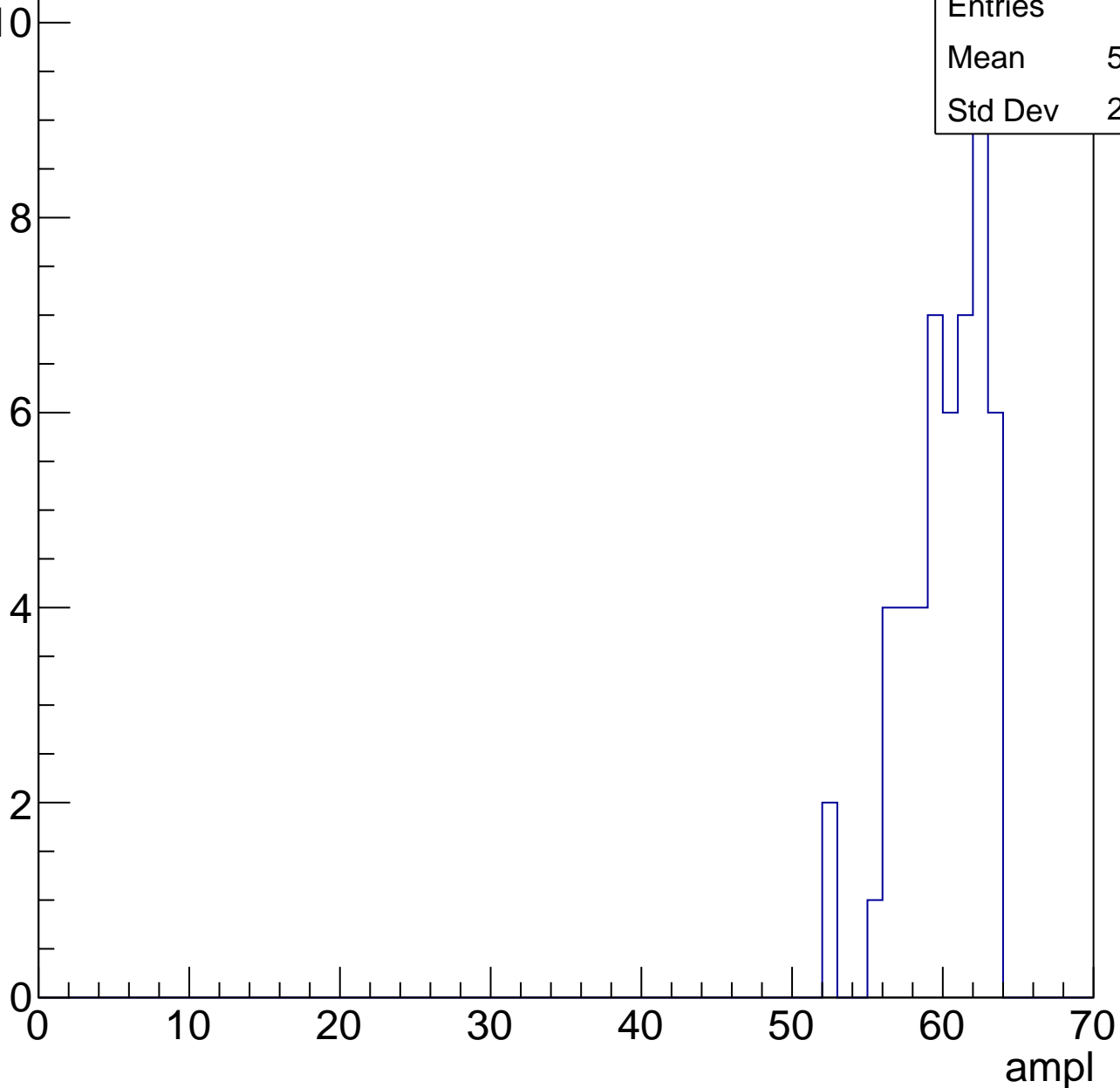


# B1L003S, U18-ch107, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

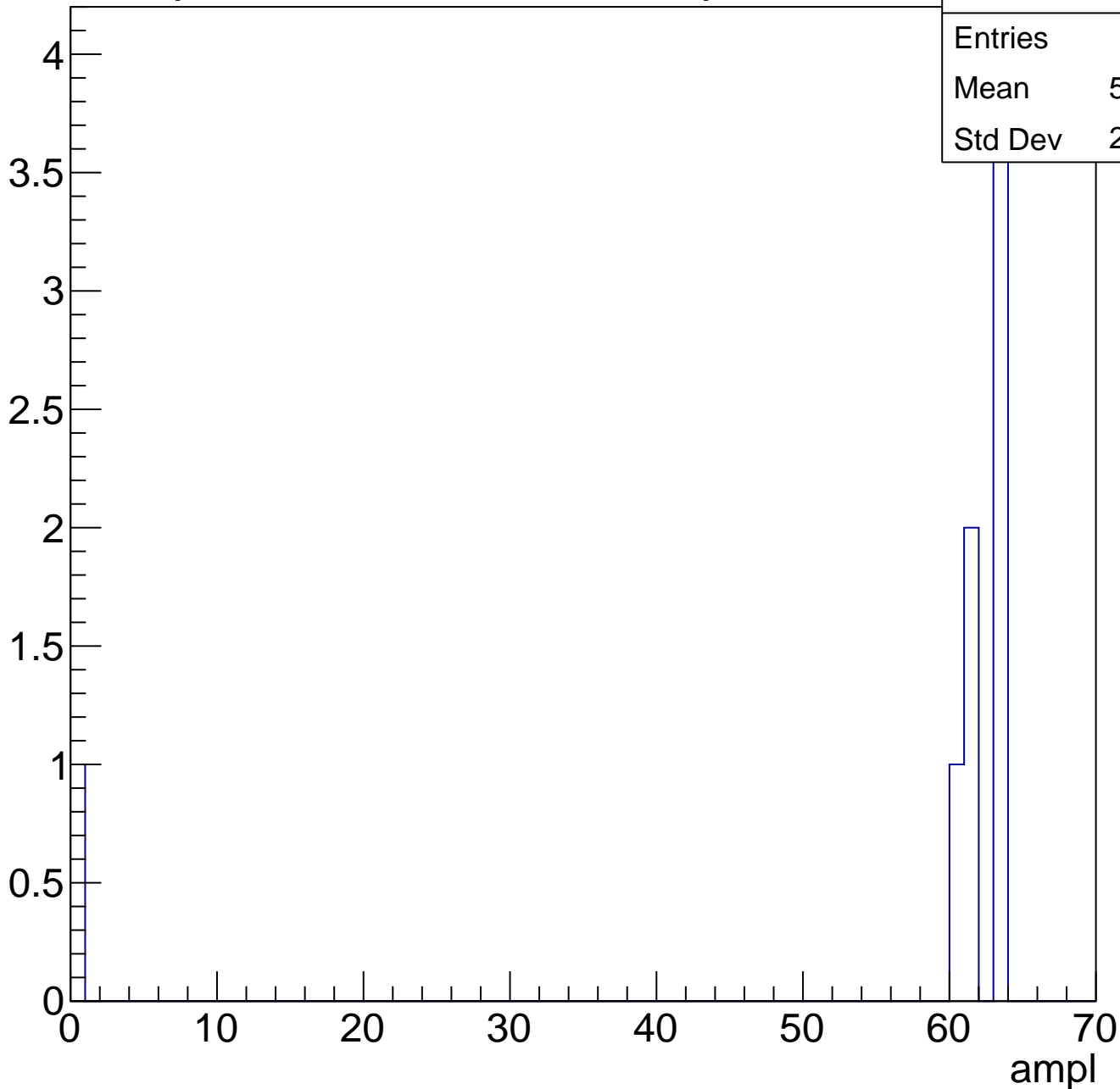
Entries	51
Mean	59.63
Std Dev	2.693



# B1L003S, U18-ch107, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U18-ch107, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	1
Mean	20
Std Dev	0

# B1L003S, U18-ch108, adc0

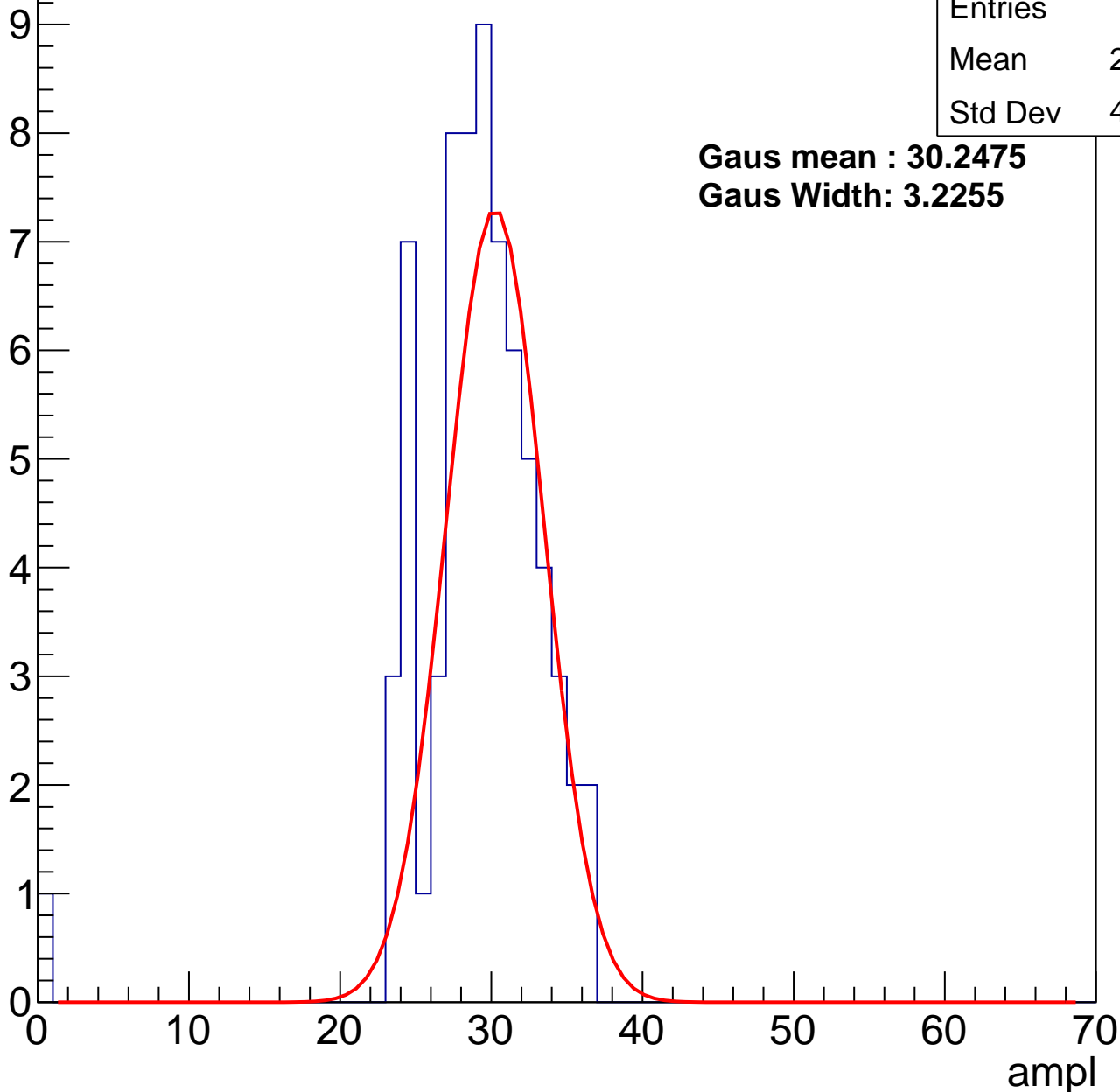
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	69
Mean	28.59
Std Dev	4.786

**Gaus mean : 30.2475**

**Gaus Width: 3.2255**



# B1L003S, U18-ch108, adc1

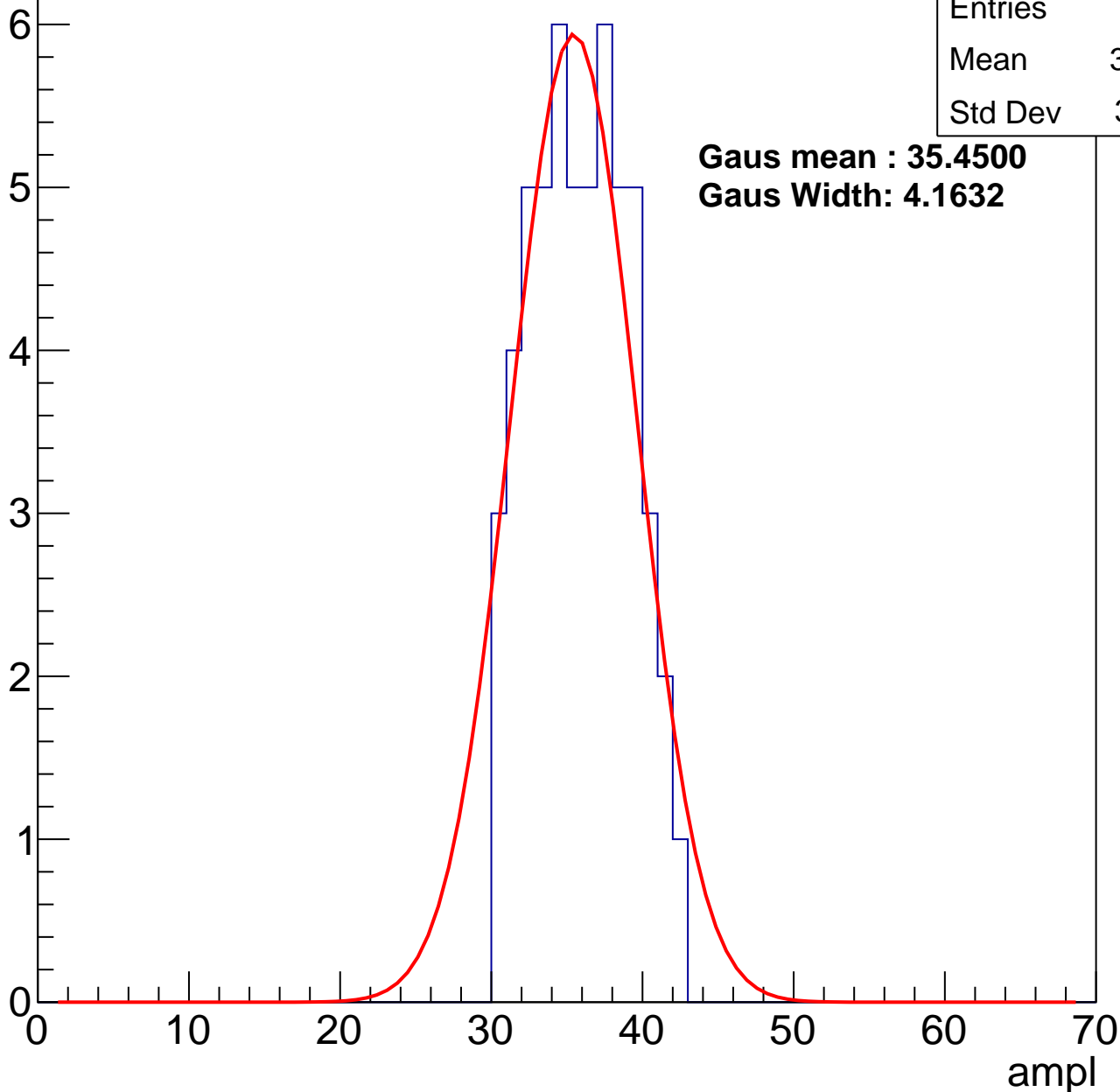
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	55
Mean	35.44
Std Dev	3.161

**Gaus mean : 35.4500**

**Gaus Width: 4.1632**



# B1L003S, U18-ch108, adc2

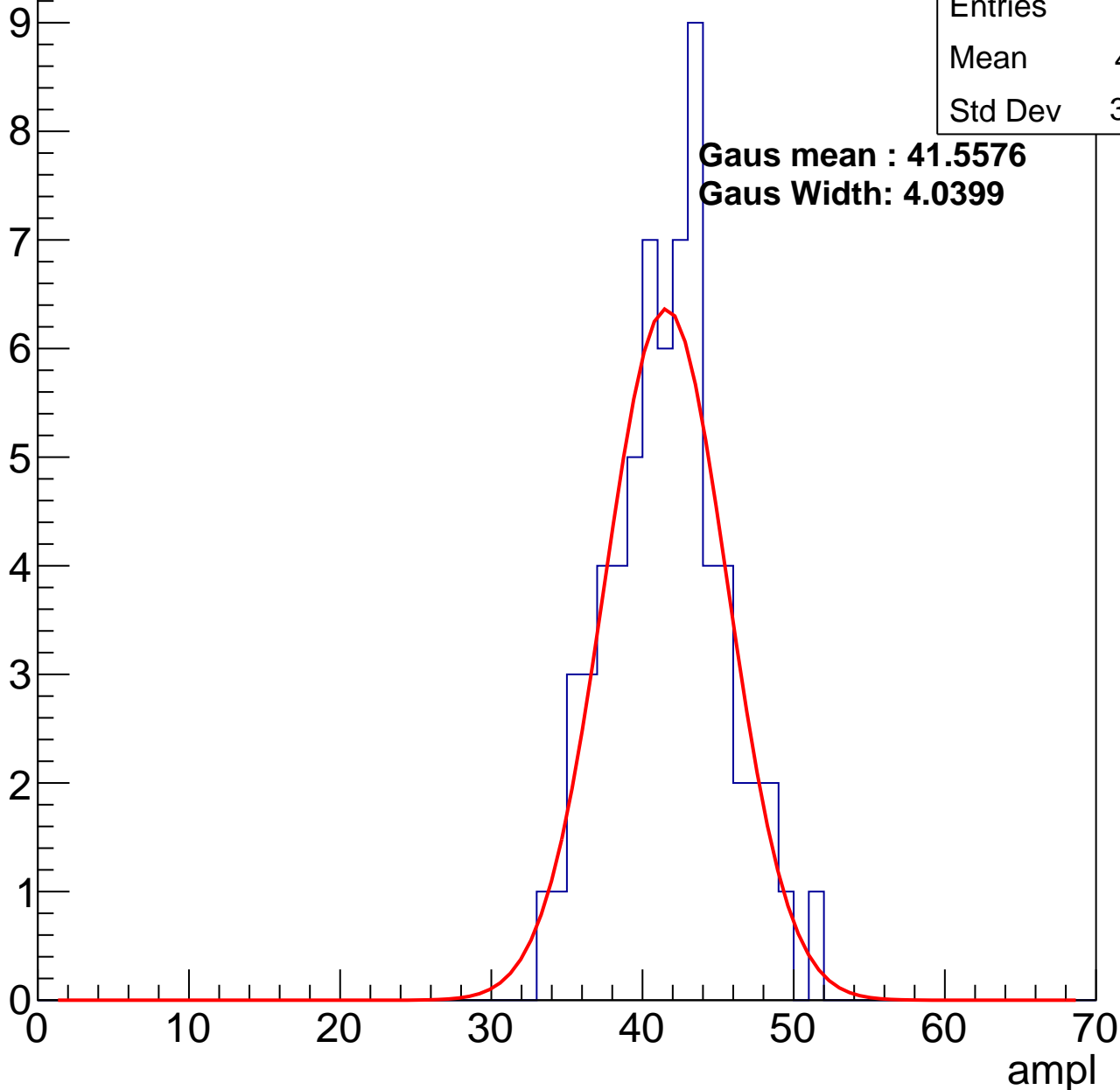
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	66
Mean	41.21
Std Dev	3.788

**Gaus mean : 41.5576**

**Gaus Width: 4.0399**

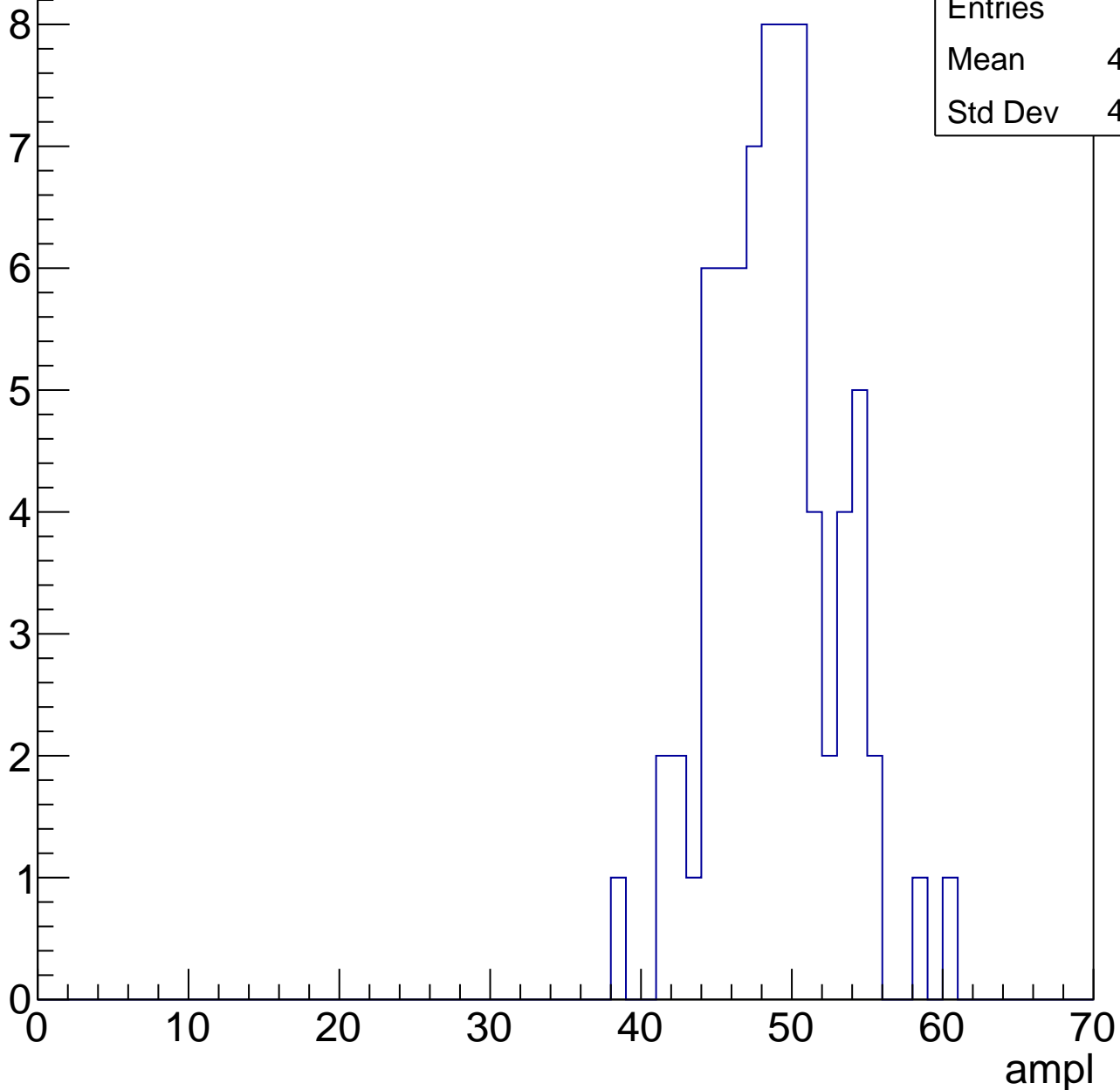


# B1L003S, U18-ch108, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	74
Mean	48.38
Std Dev	4.019

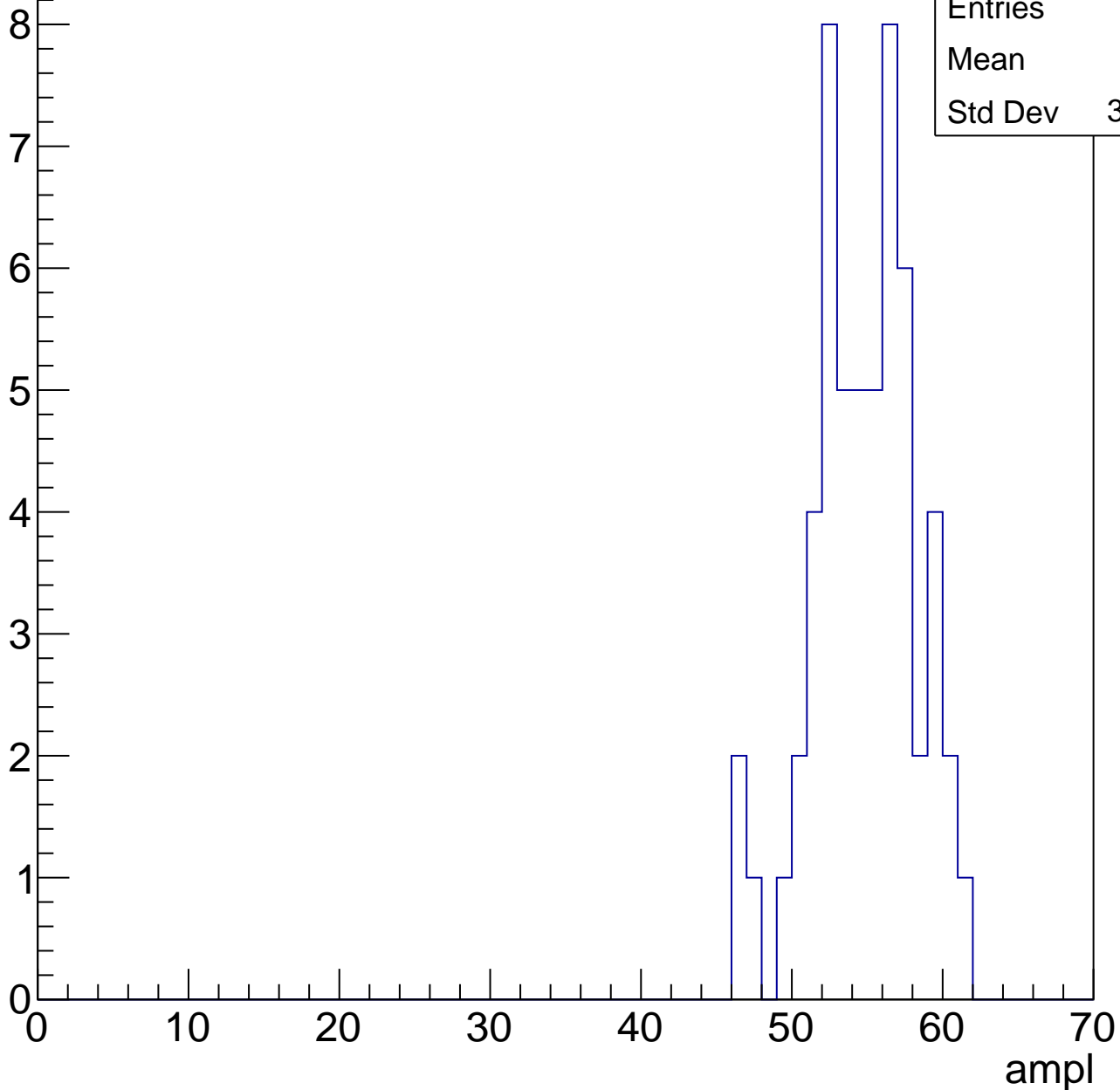


# B1L003S, U18-ch108, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	56
Mean	54.3
Std Dev	3.396

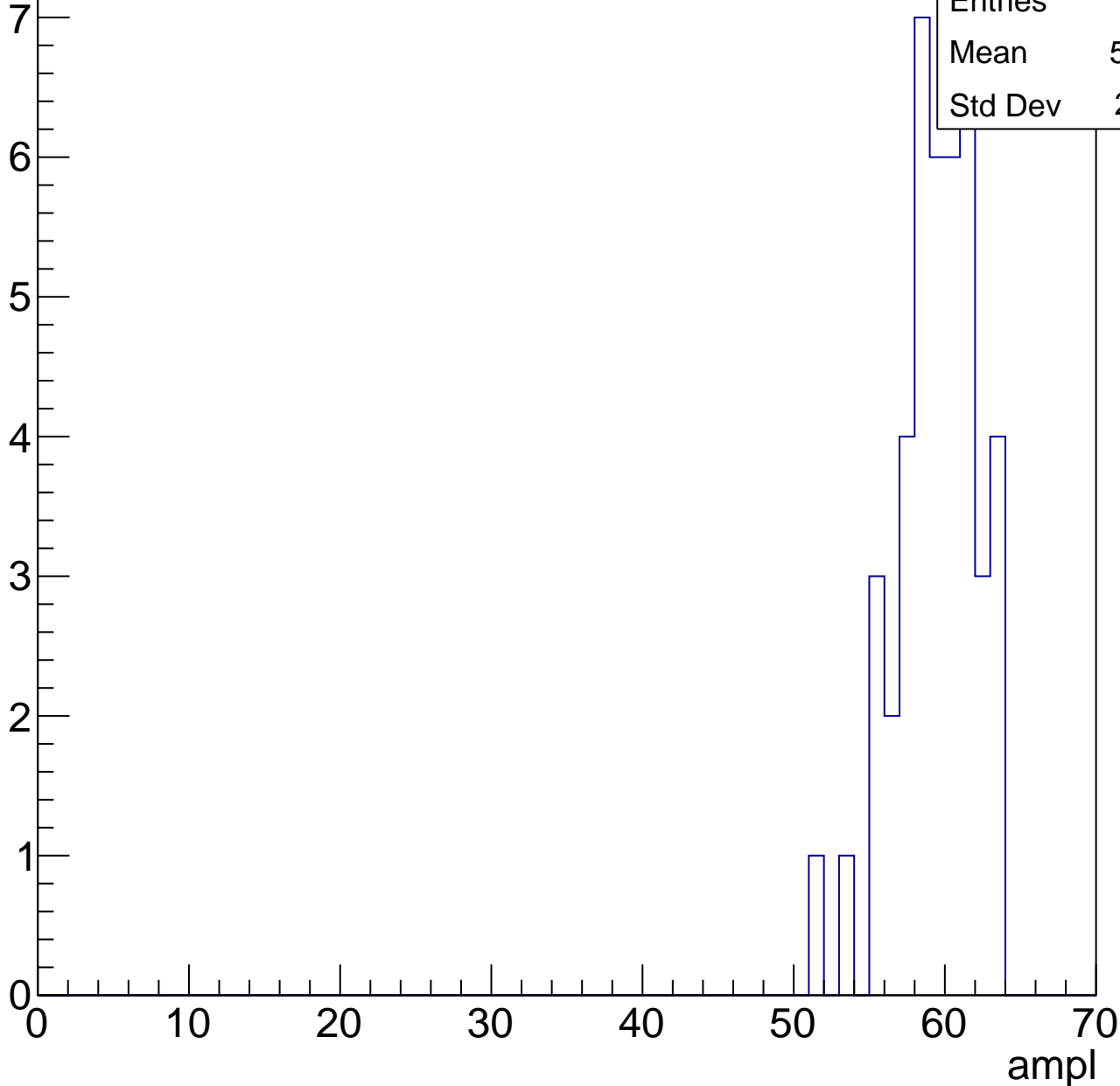


# B1L003S, U18-ch108, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	44
Mean	58.95
Std Dev	2.671

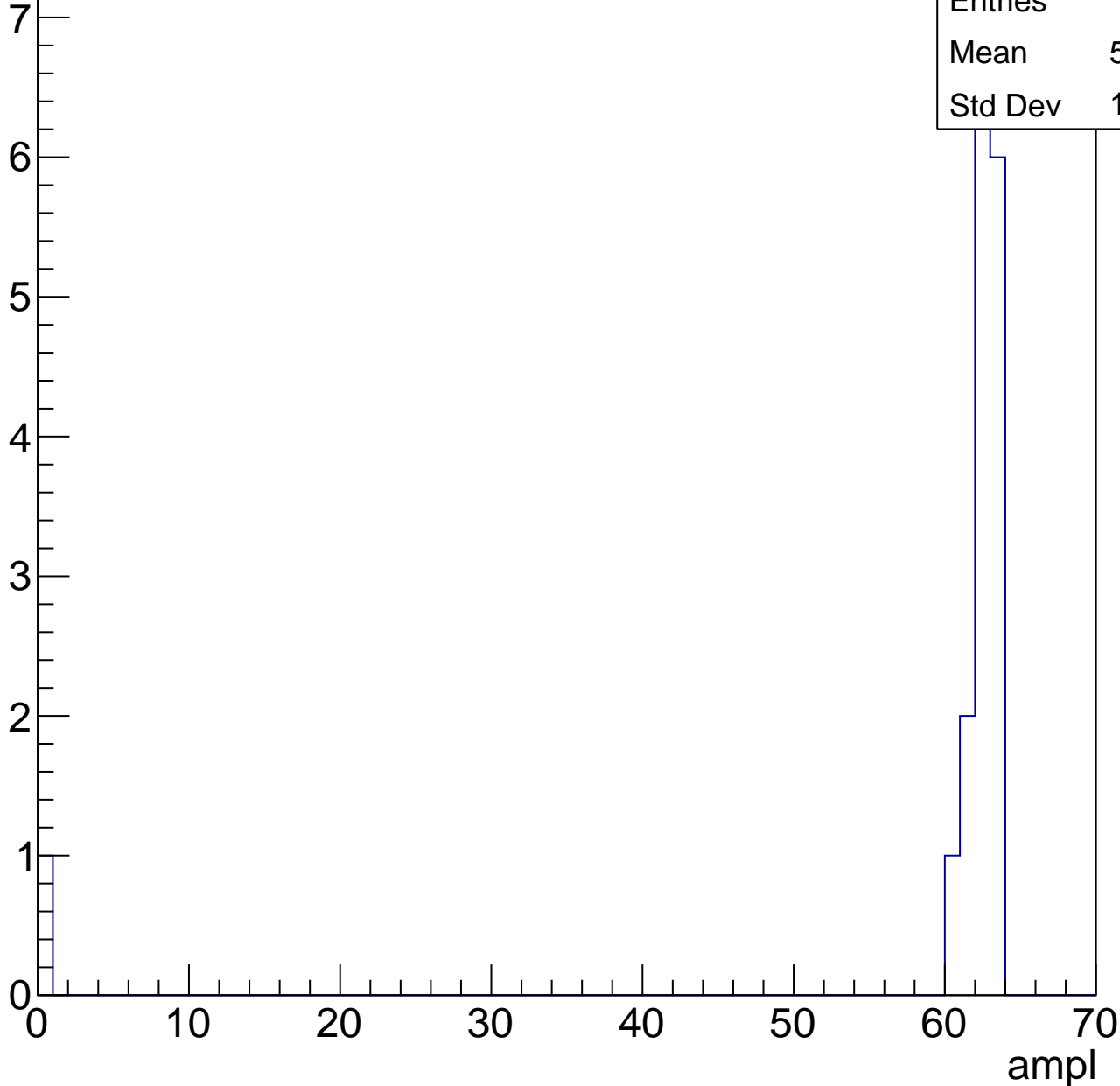


# B1L003S, U18-ch108, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	17
Mean	58.47
Std Dev	14.64





# B1L003S, U18-ch108, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L003S, U18-ch109, adc0

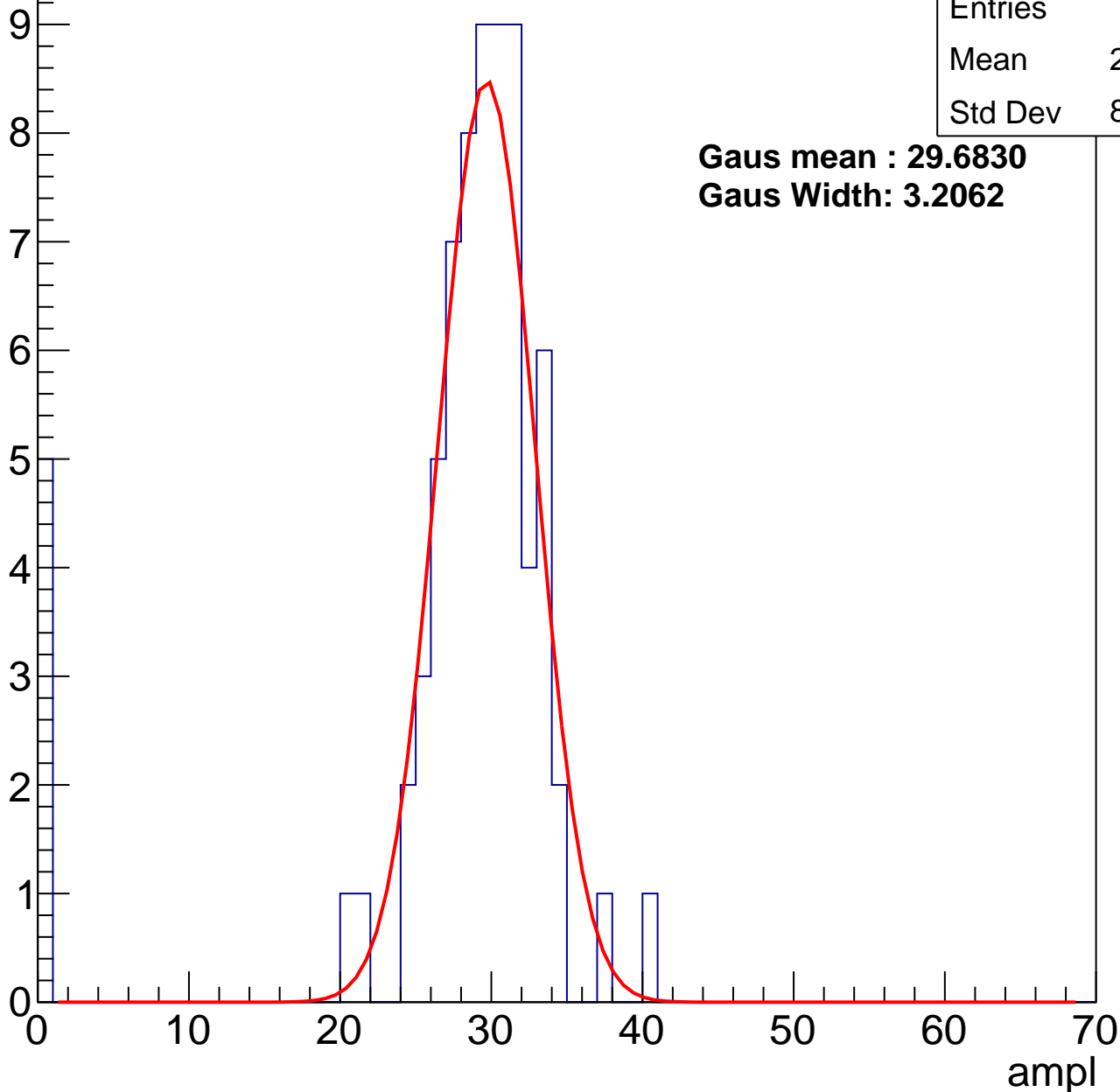
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	73
Mean	27.23
Std Dev	8.035

**Gaus mean : 29.6830**

**Gaus Width: 3.2062**



# B1L003S, U18-ch109, adc1

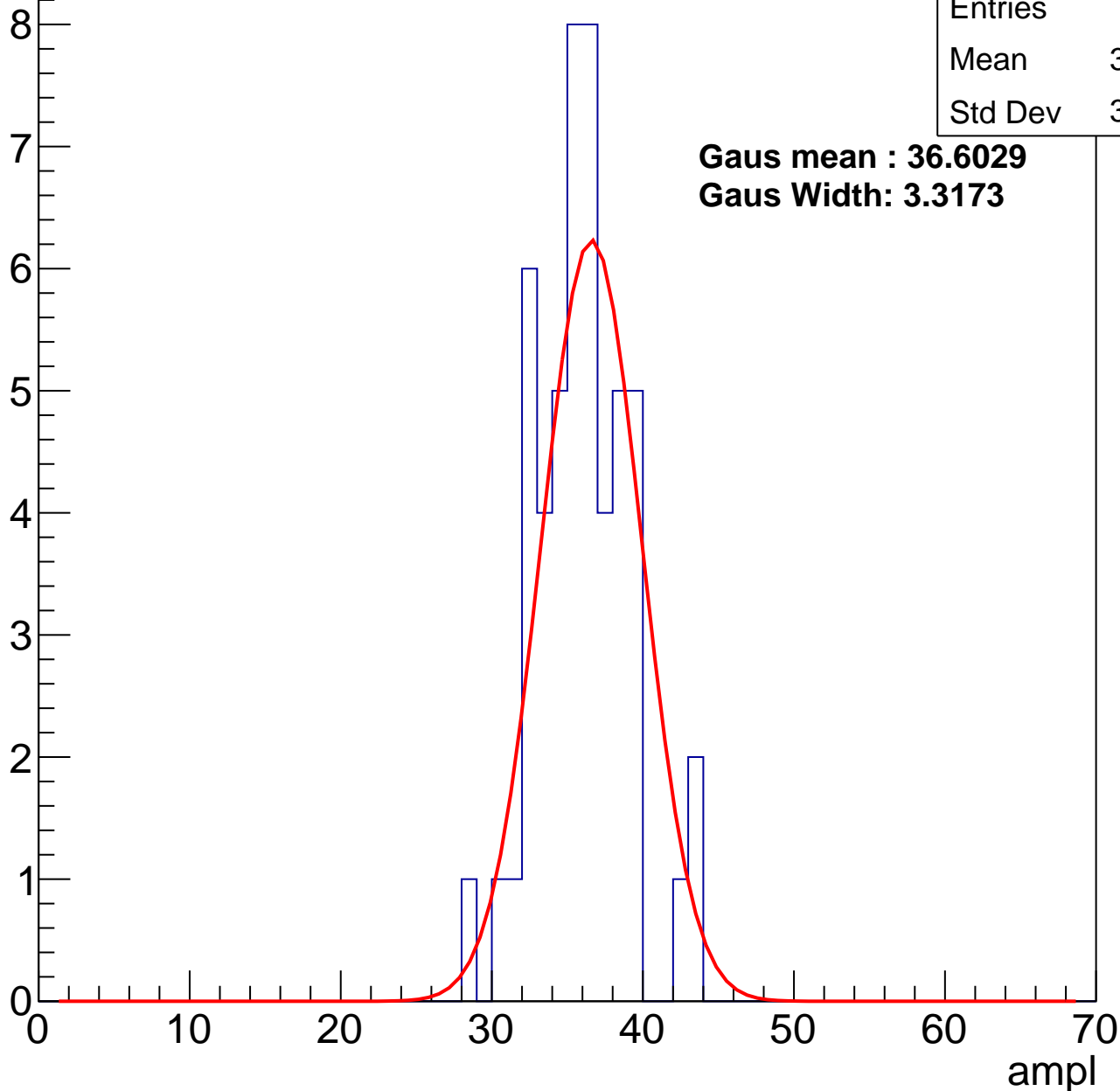
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	51
Mean	35.53
Std Dev	3.057

**Gaus mean : 36.6029**

**Gaus Width: 3.3173**



# B1L003S, U18-ch109, adc2

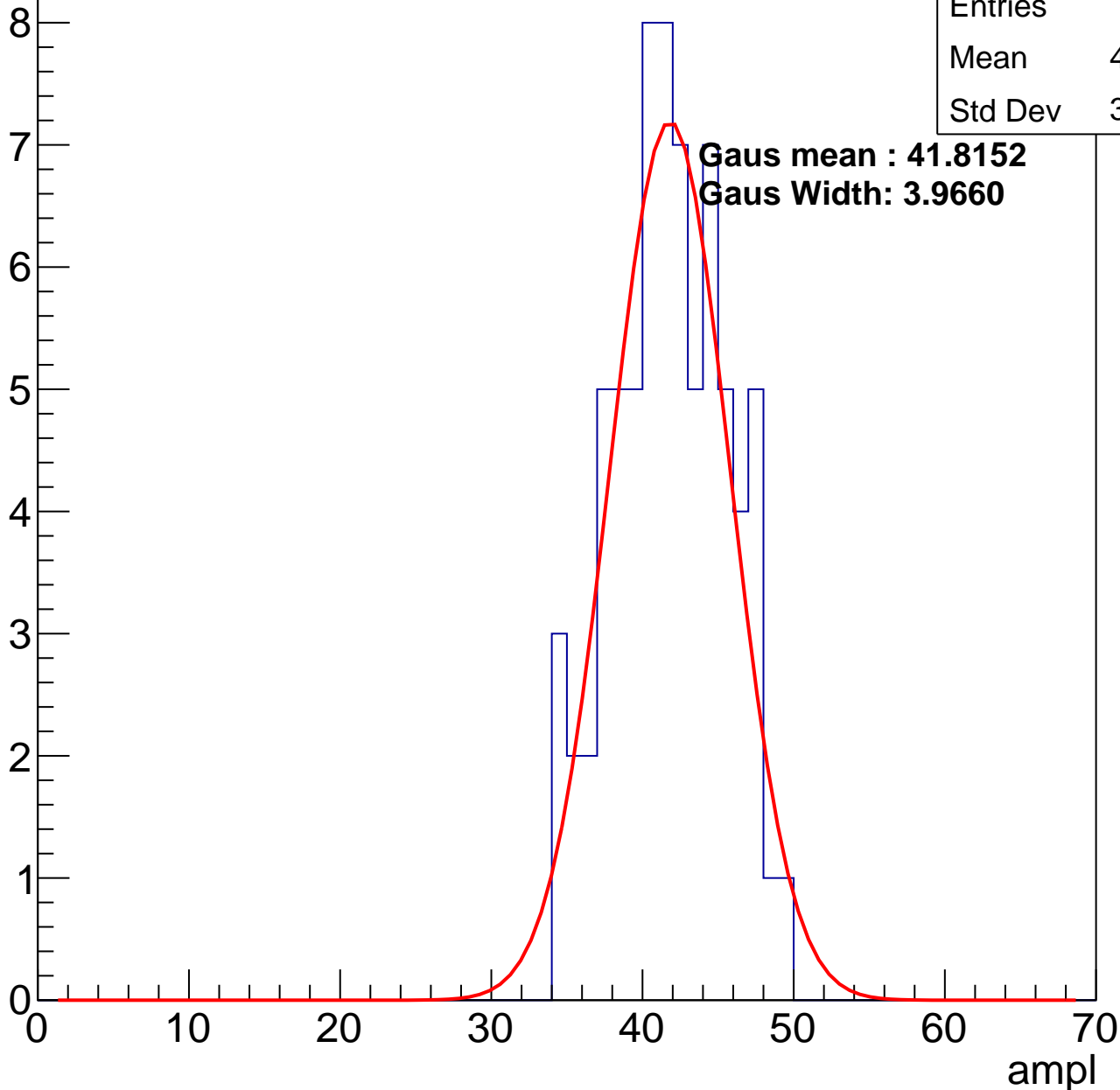
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	73
Mean	41.37
Std Dev	3.655

**Gaus mean : 41.8152**

**Gaus Width: 3.9660**

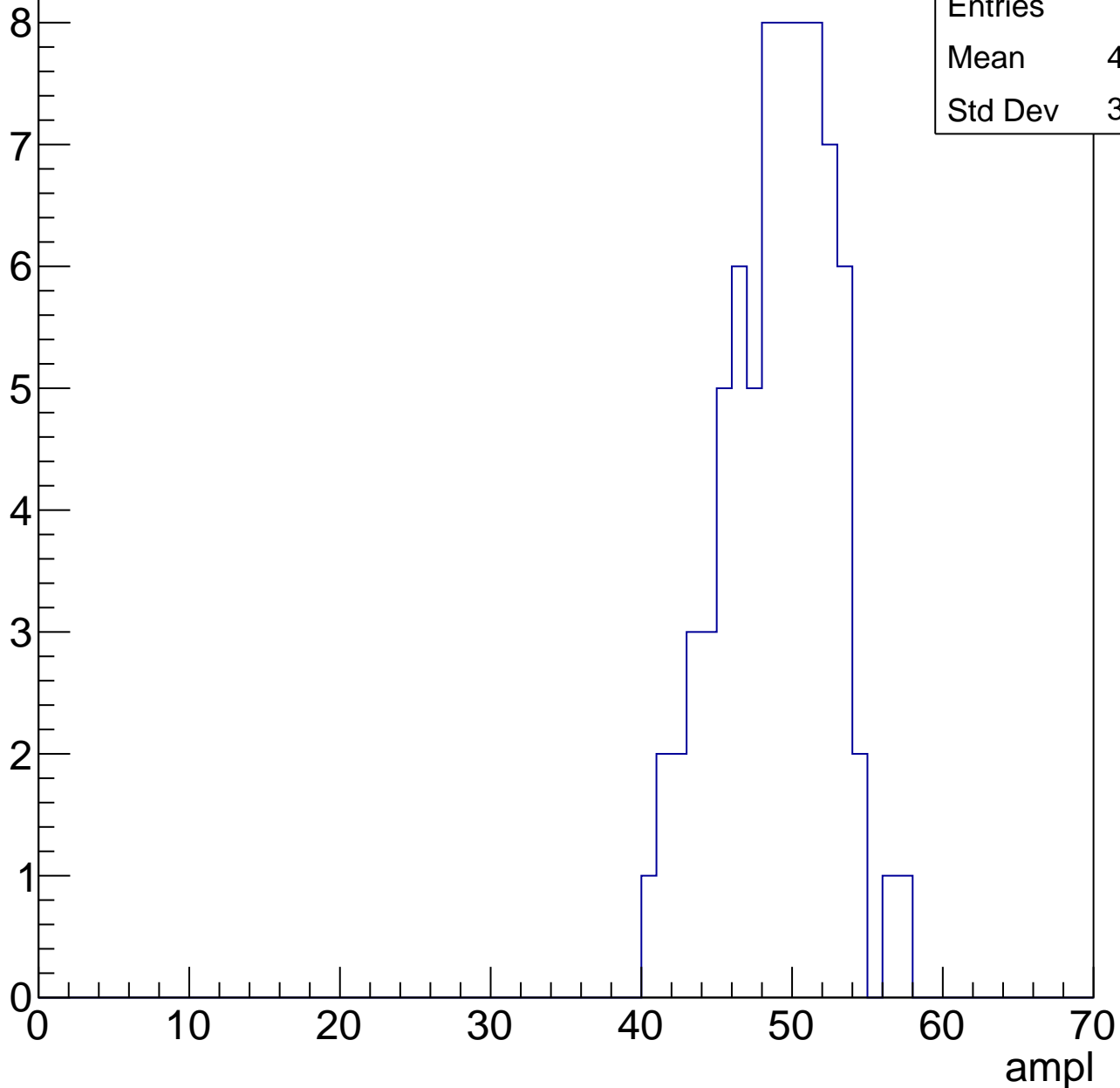


# B1L003S, U18-ch109, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	76
Mean	48.55
Std Dev	3.625

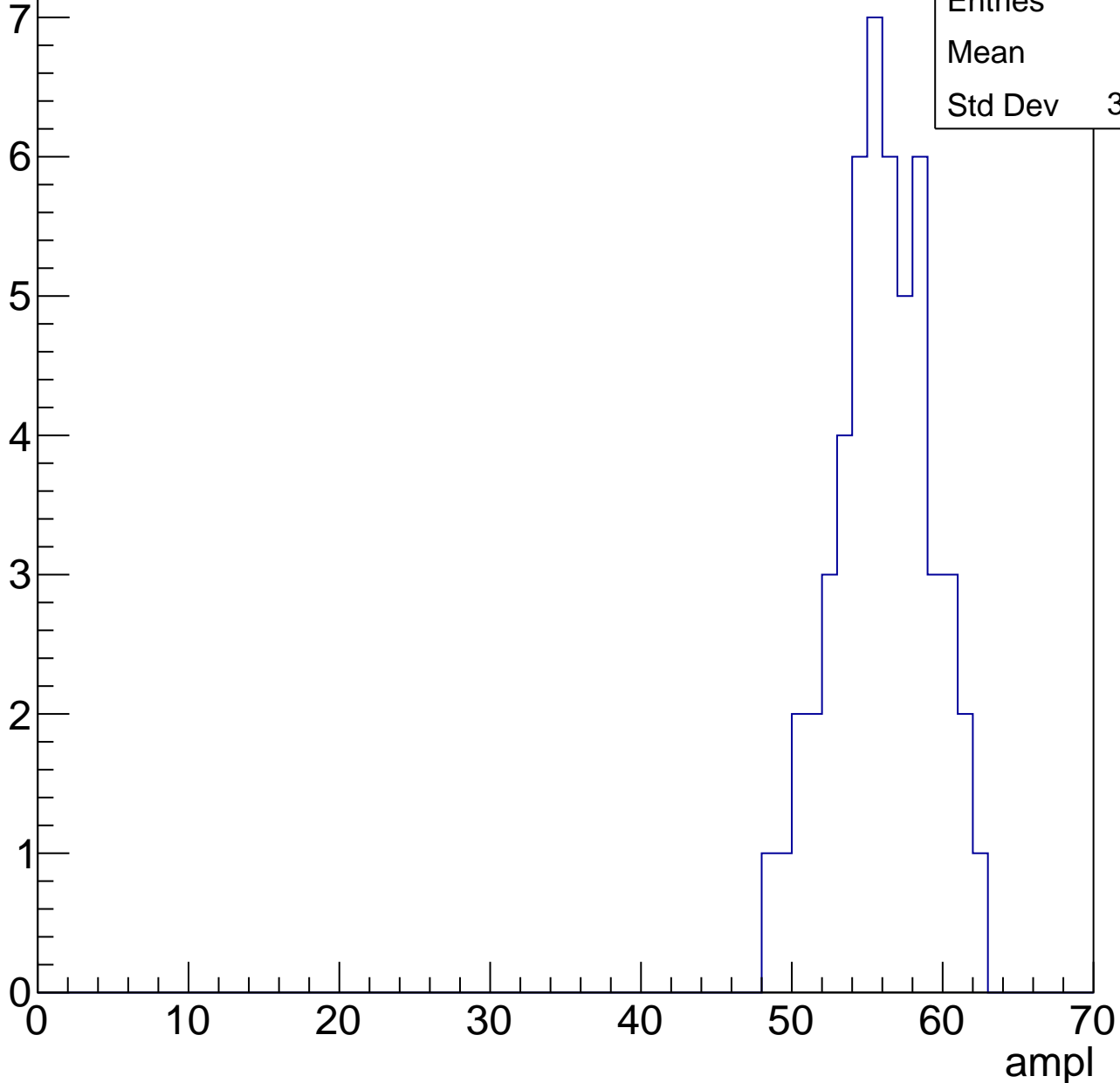


# B1L003S, U18-ch109, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

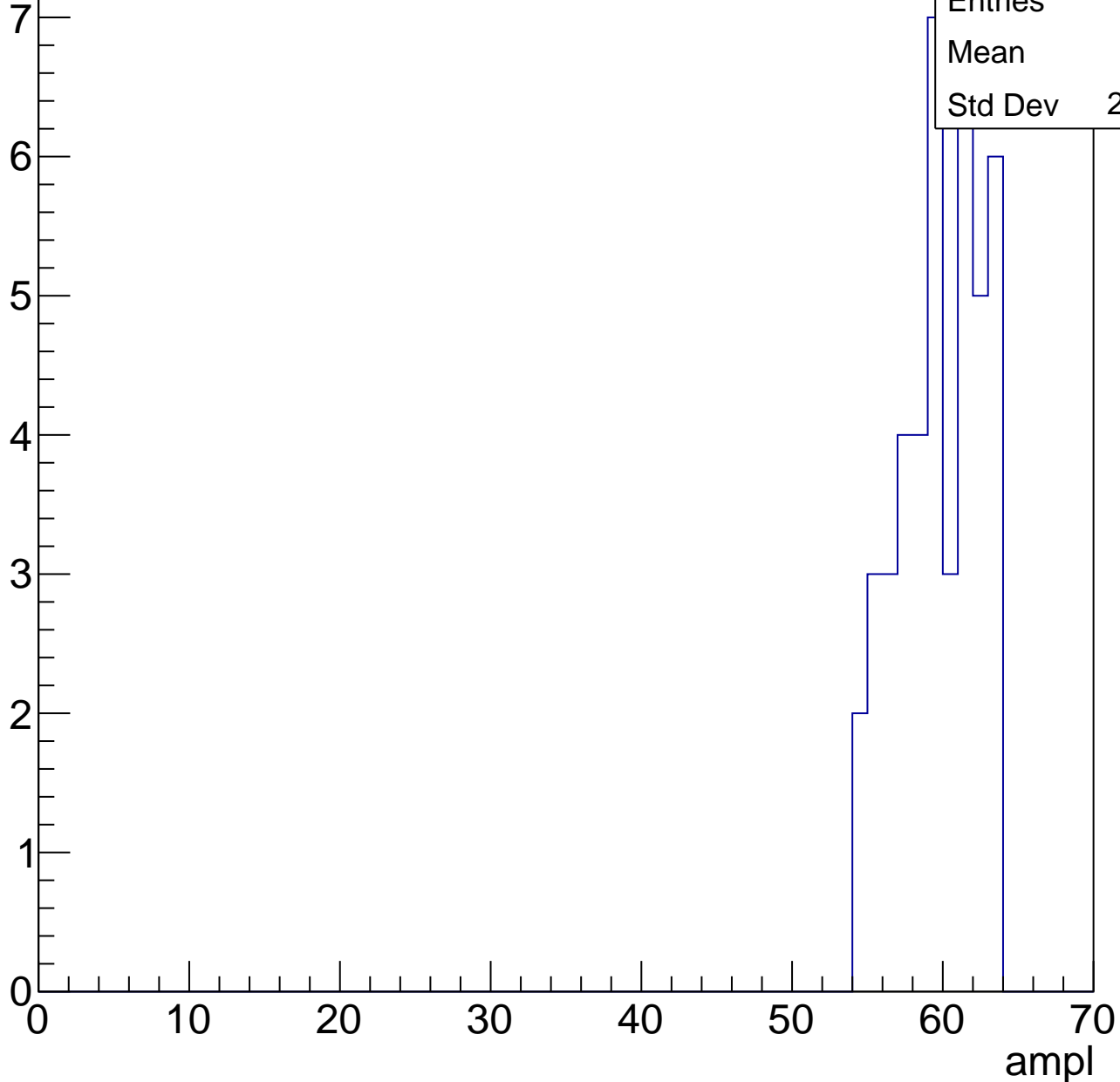
Entries	52
Mean	55.5
Std Dev	3.183



# B1L003S, U18-ch109, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	44
Mean	59.3
Std Dev	2.668

# B1L003S, U18-ch109, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

4  
3.5  
3  
2.5  
2  
1.5  
1  
0.5  
0

Entries	14
Mean	57.21
Std Dev	15.91

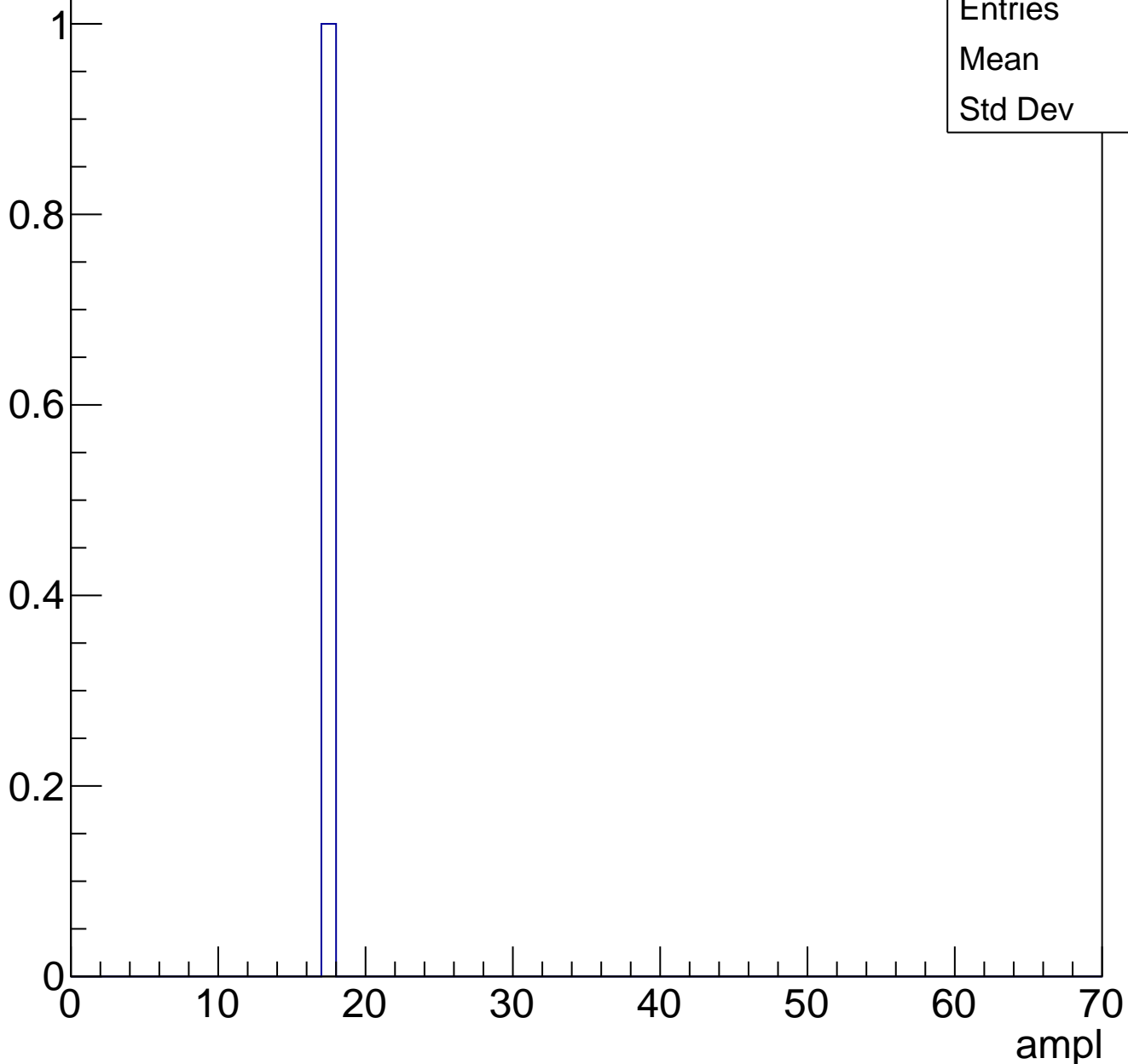
ampl



# B1L003S, U18-ch109, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	1
Mean	17
Std Dev	0

# B1L003S, U18-ch110, adc0

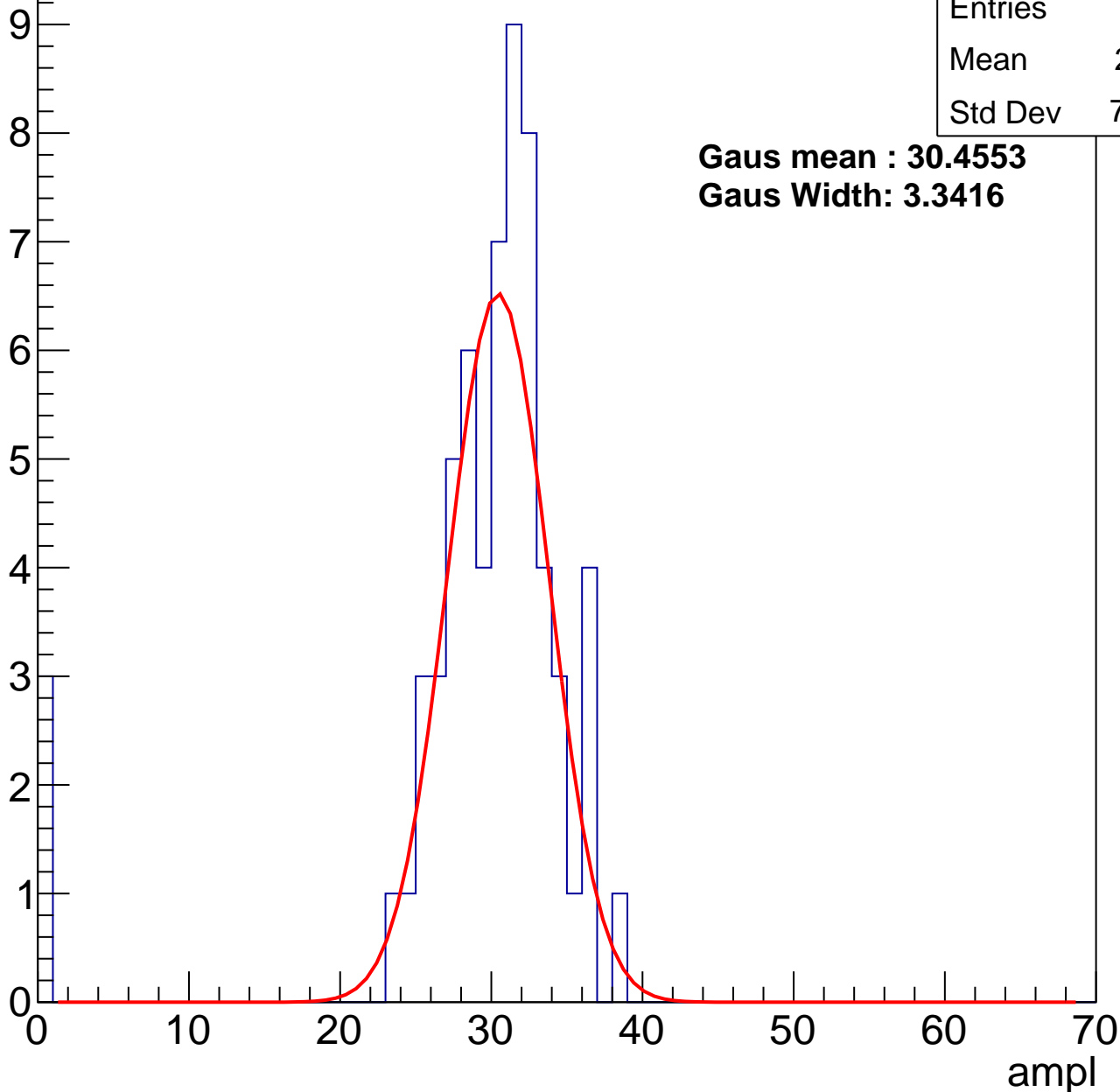
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	63
Mean	28.81
Std Dev	7.182

**Gaus mean : 30.4553**

**Gaus Width: 3.3416**



# B1L003S, U18-ch110, adc1

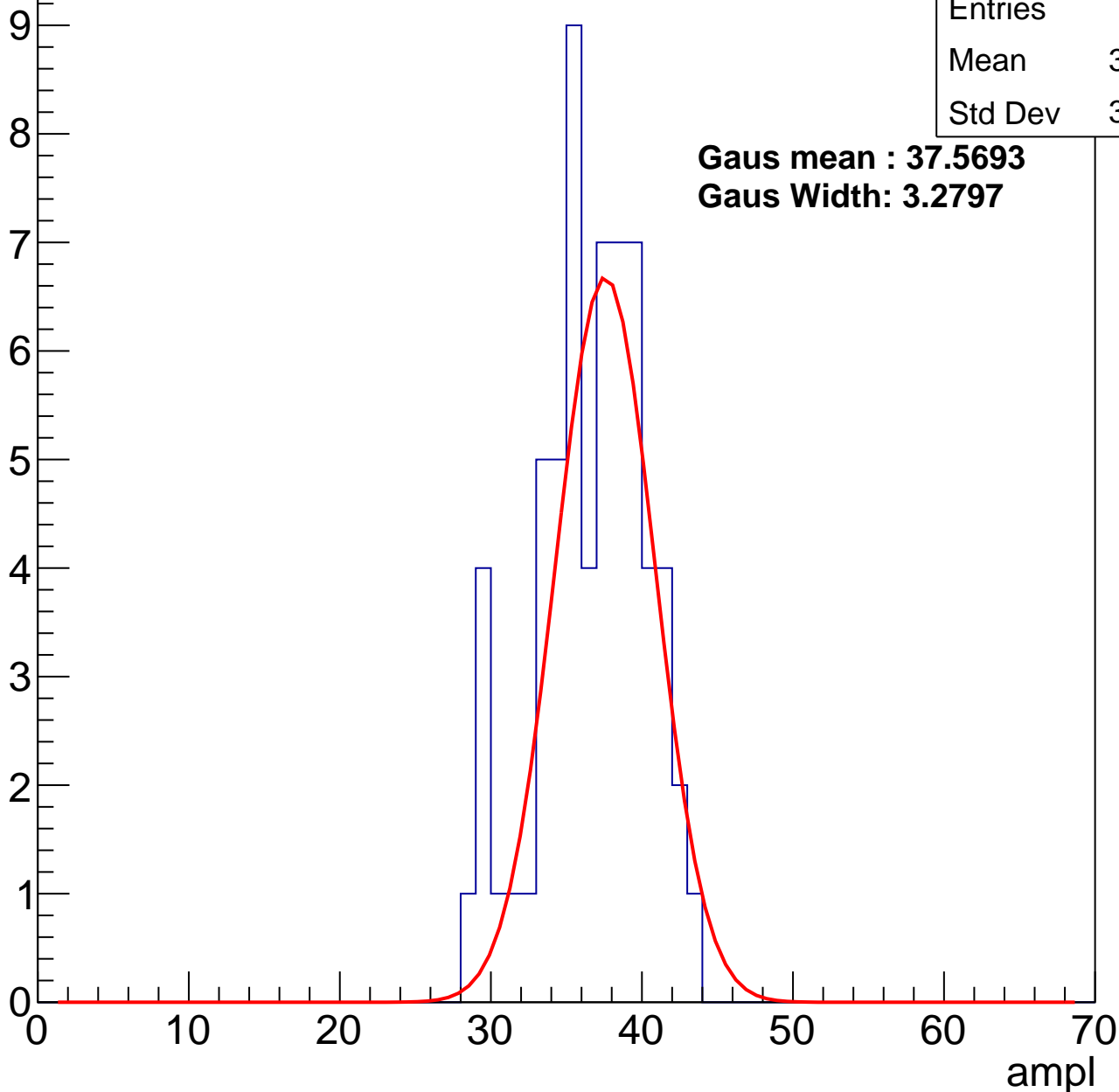
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	63
Mean	36.19
Std Dev	3.545

**Gaus mean : 37.5693**

**Gaus Width: 3.2797**

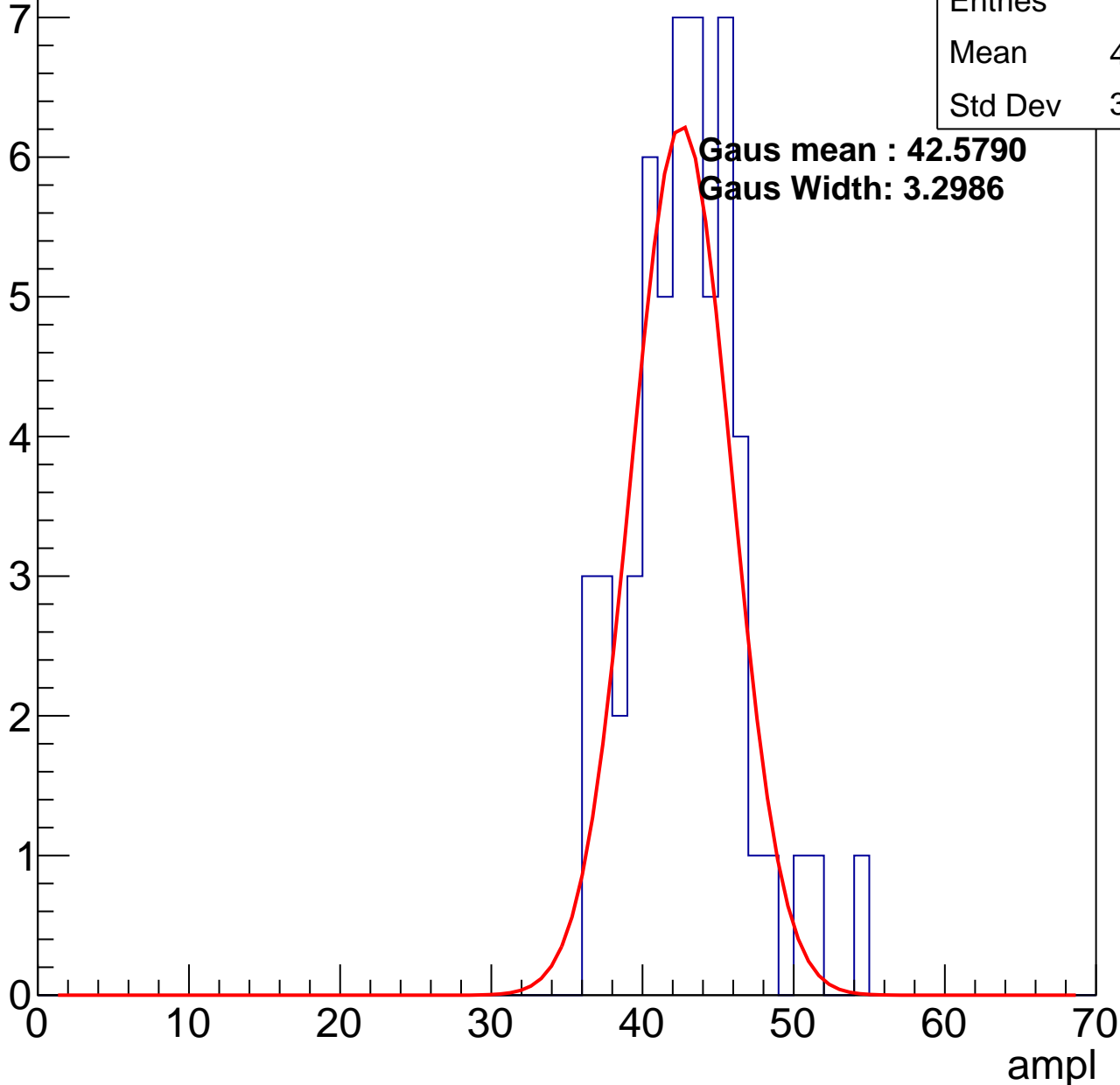


# B1L003S, U18-ch110, adc2

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	57
Mean	42.47
Std Dev	3.657

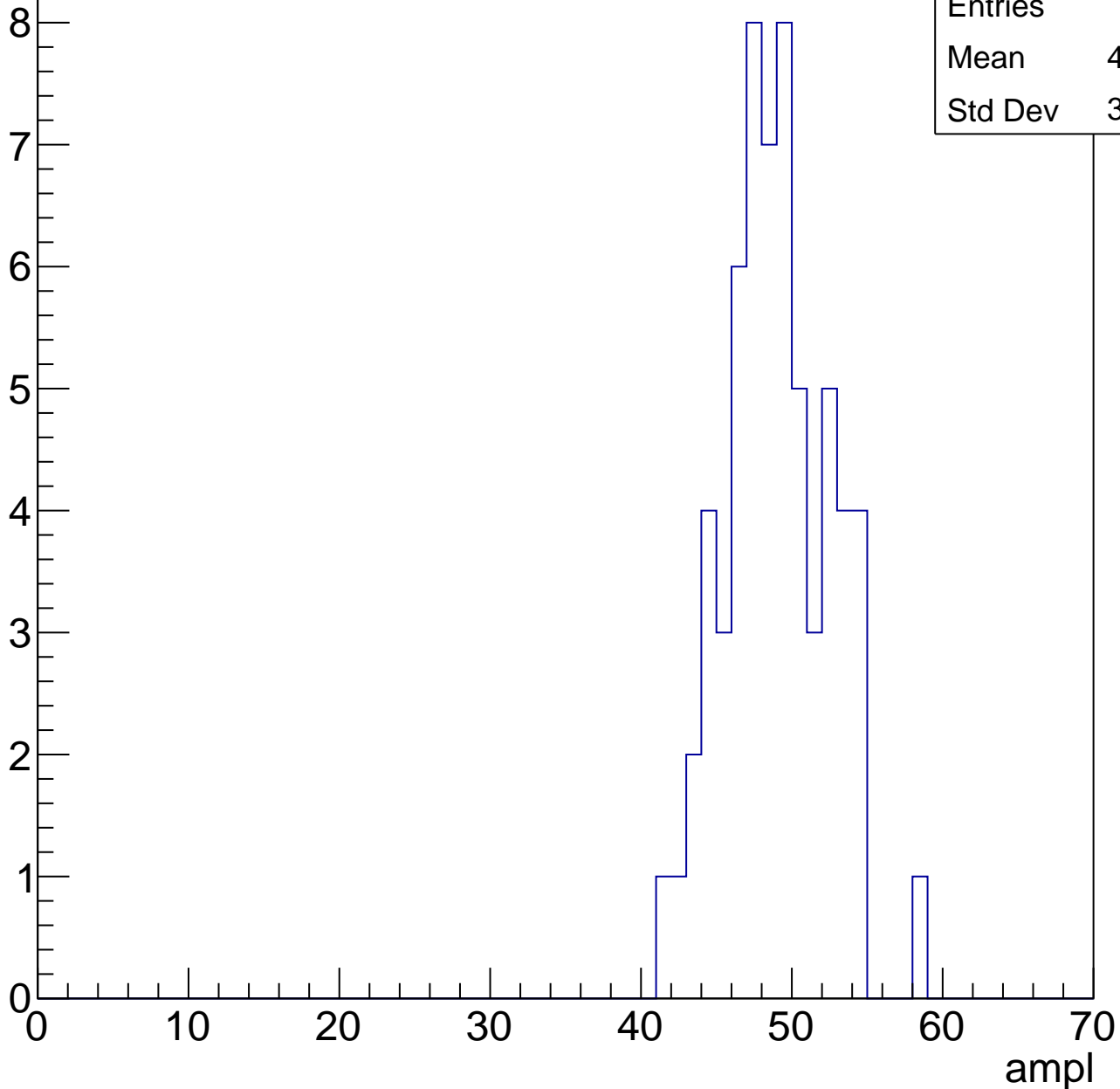


# B1L003S, U18-ch110, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	62
Mean	48.53
Std Dev	3.406

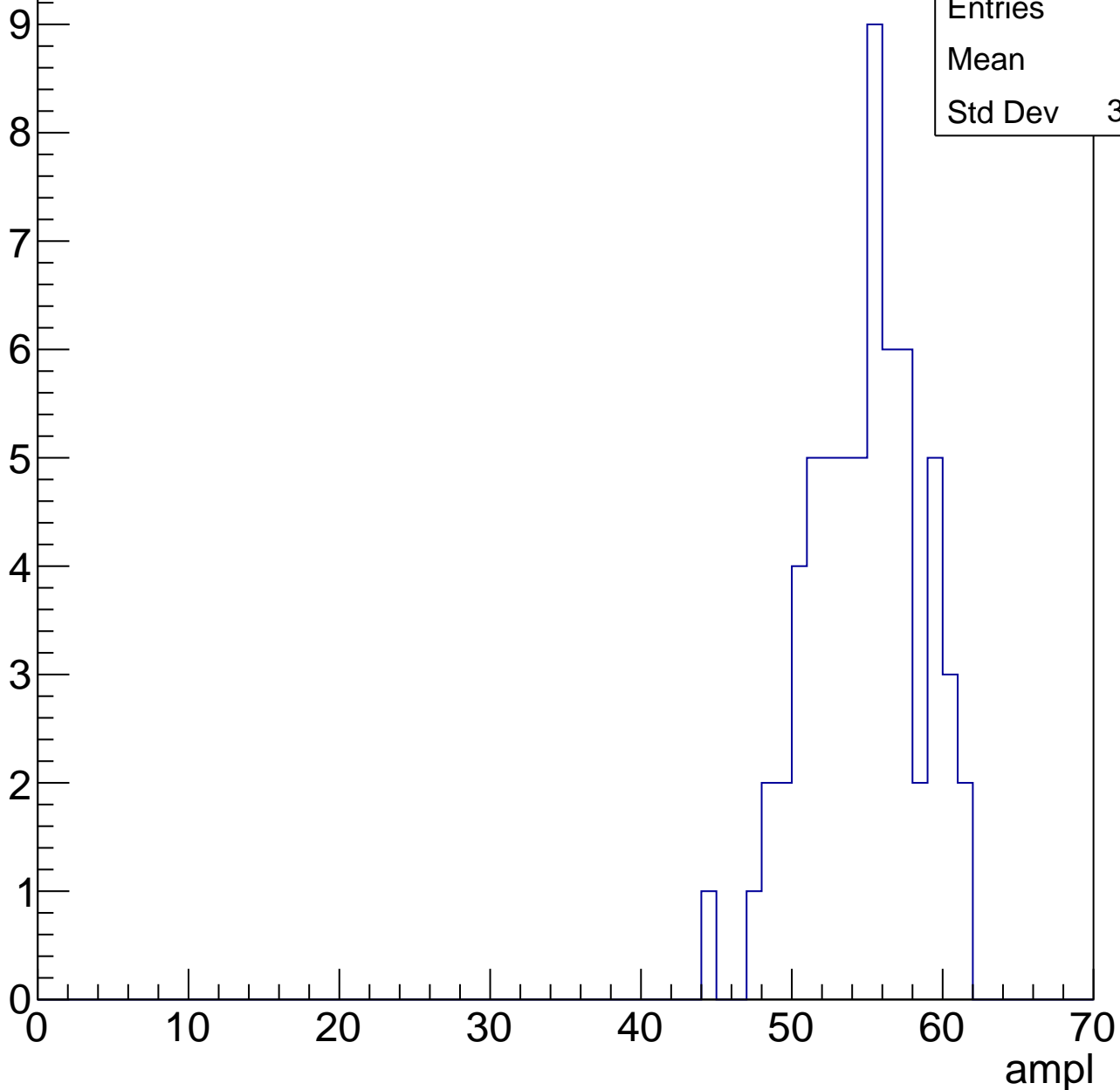


# B1L003S, U18-ch110, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	63
Mean	54.3
Std Dev	3.672

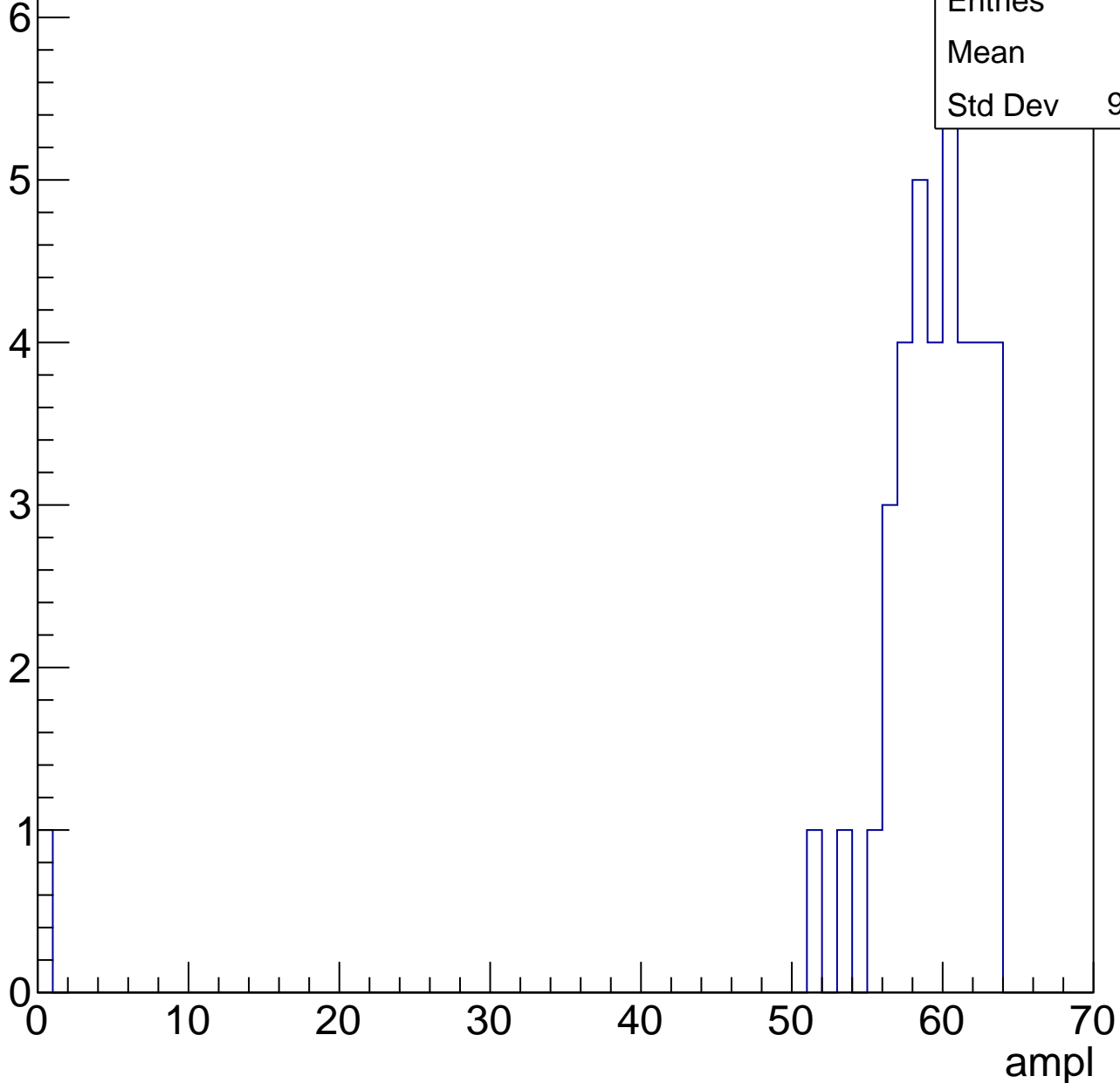


# B1L003S, U18-ch110, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	38
Mean	57.5
Std Dev	9.843

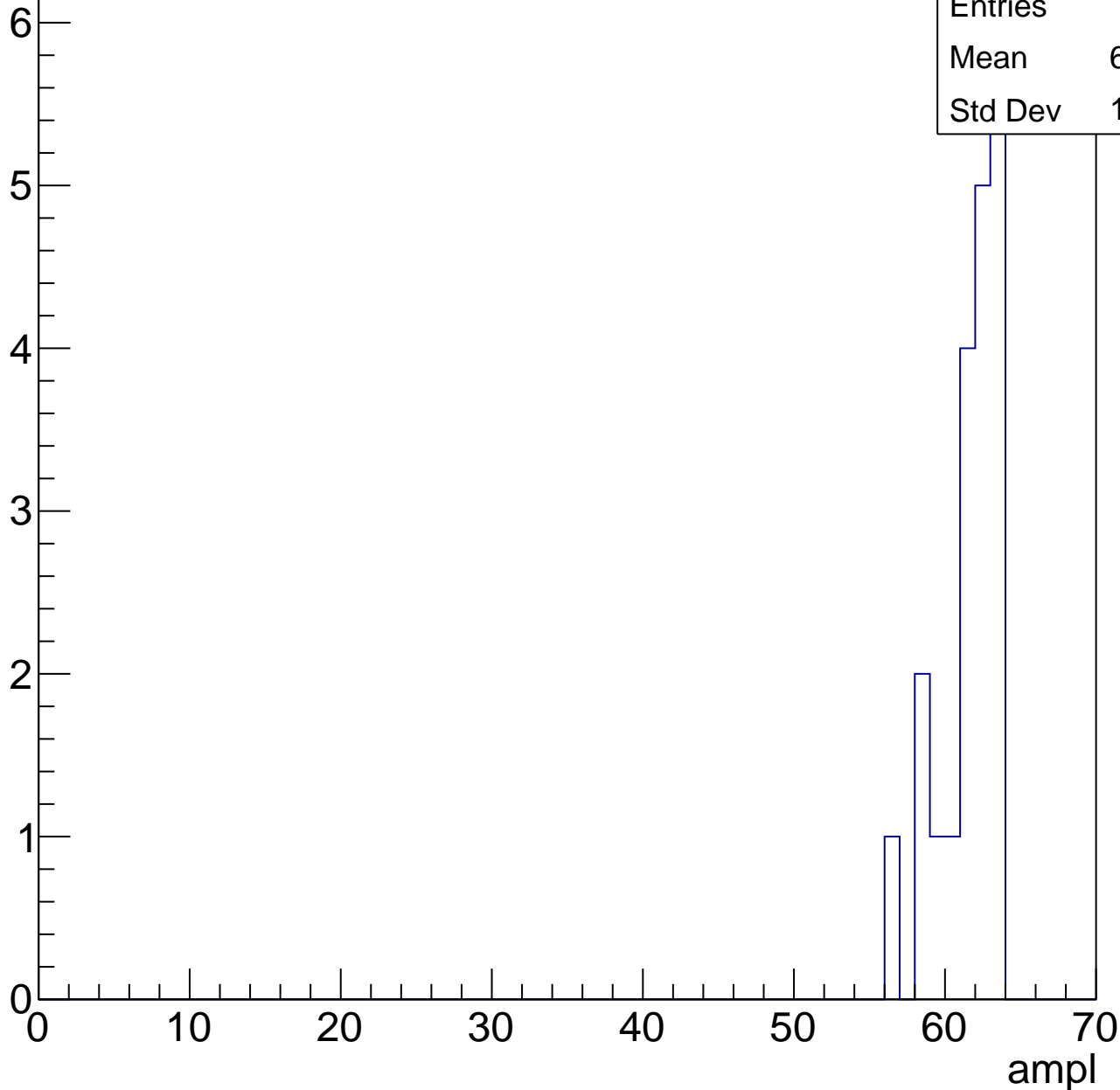


# B1L003S, U18-ch110, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	20
Mean	61.15
Std Dev	1.956





# B1L003S, U18-ch110, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U18-ch111, adc0

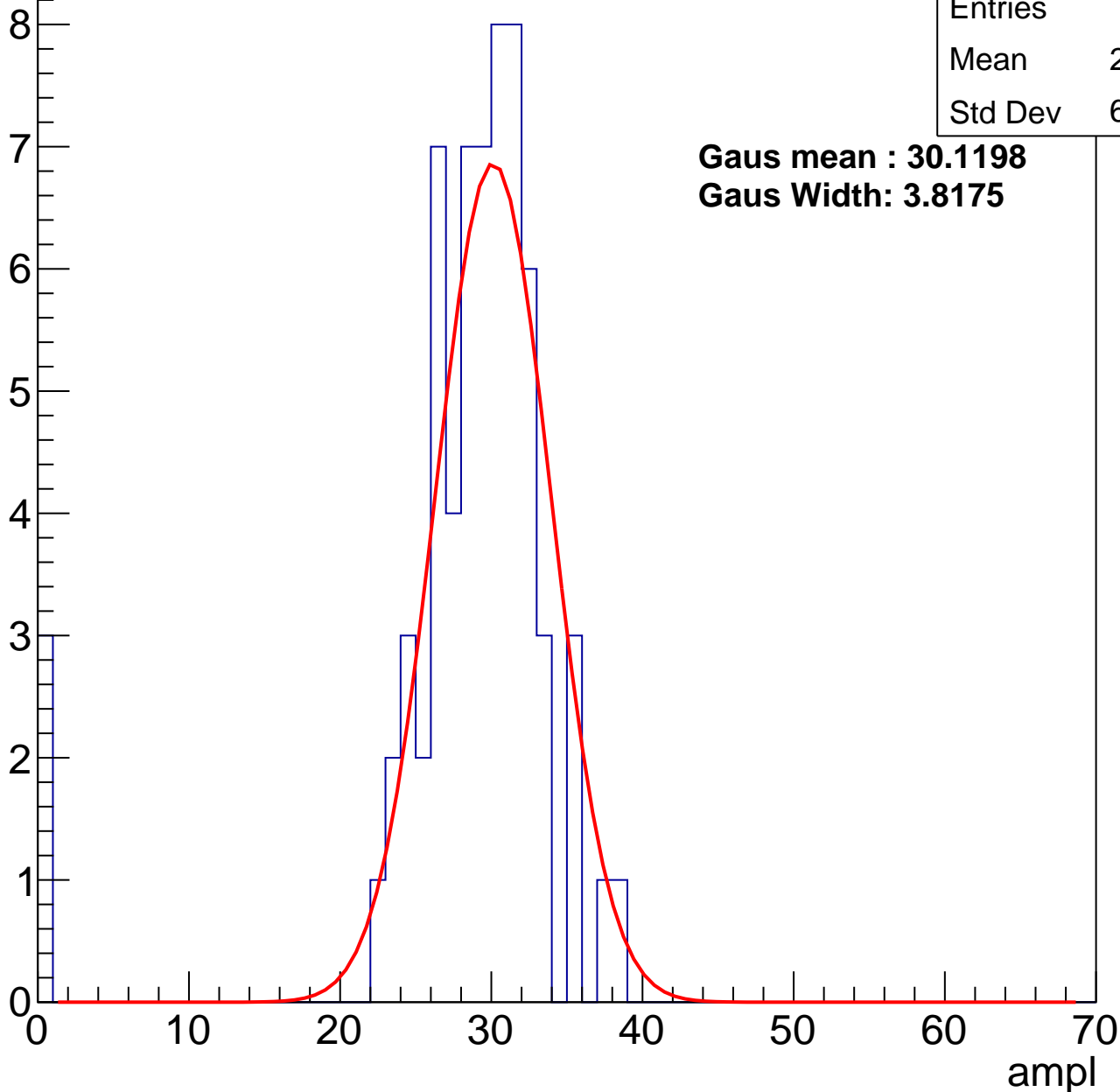
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	66
Mean	27.85
Std Dev	6.902

**Gaus mean : 30.1198**

**Gaus Width: 3.8175**



# B1L003S, U18-ch111, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	79
Mean	36
Std Dev	3.607

**Gaus mean : 36.9195**

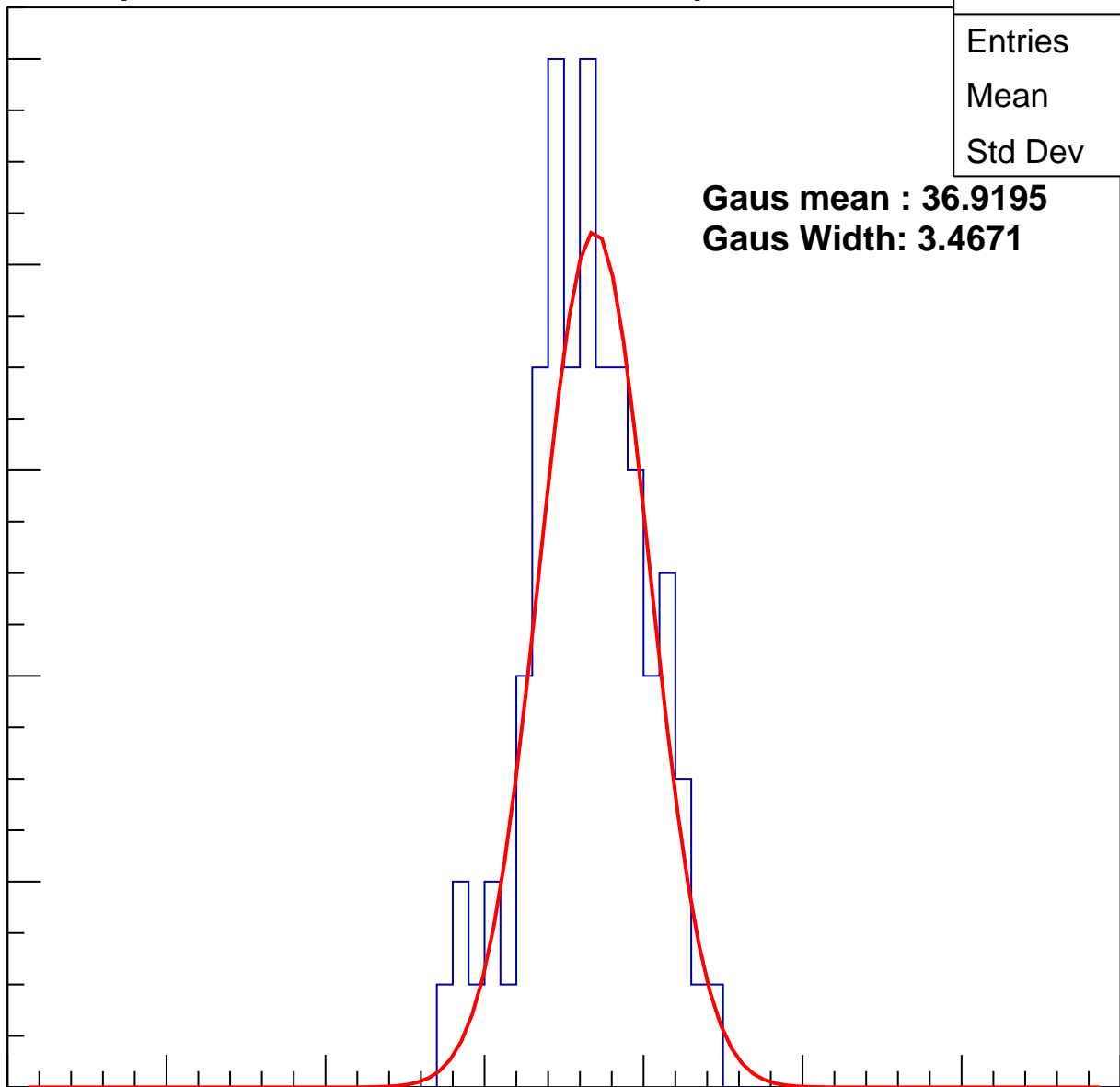
**Gaus Width: 3.4671**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

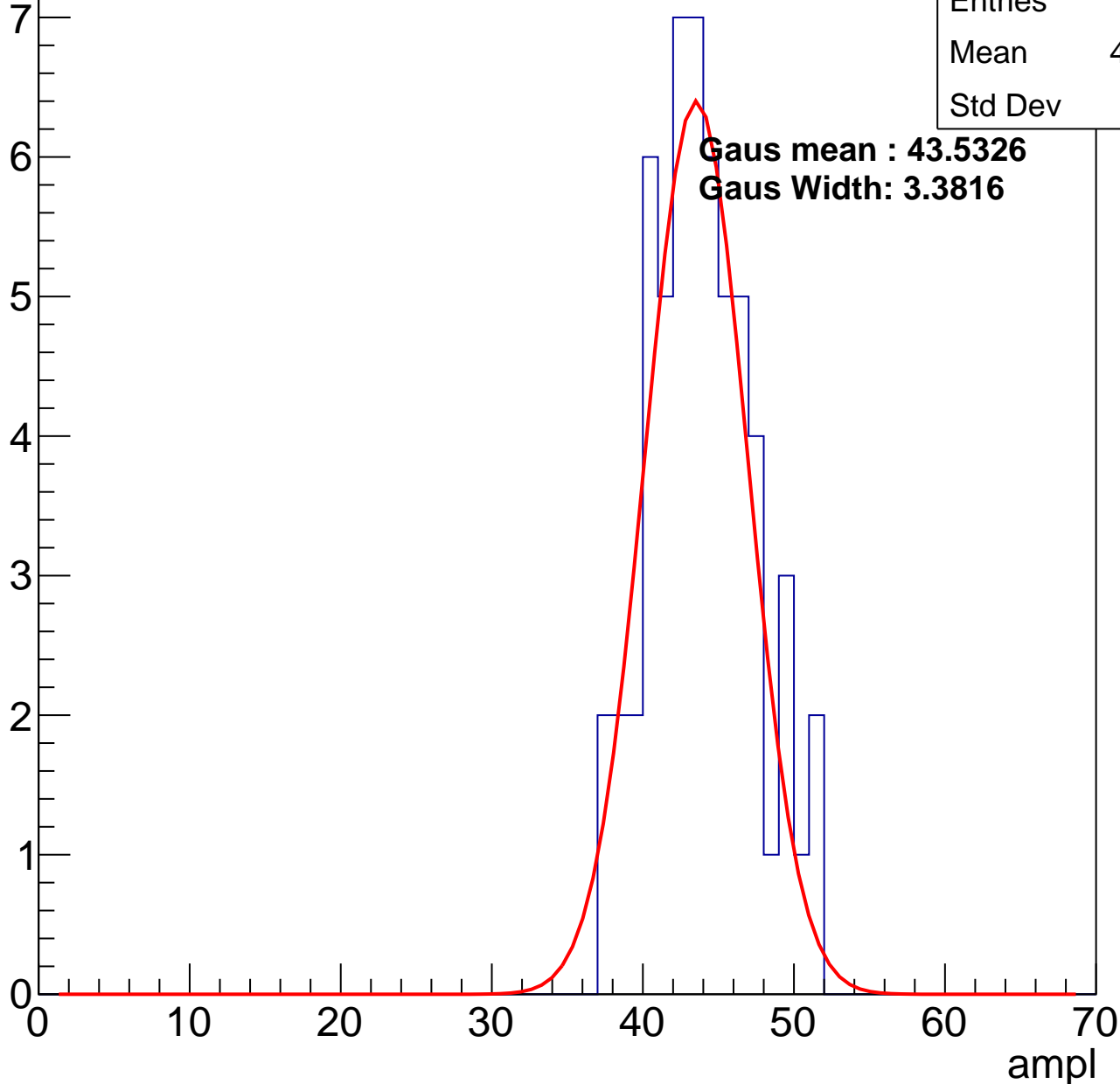


# B1L003S, U18-ch111, adc2

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	58
Mean	43.48
Std Dev	3.39

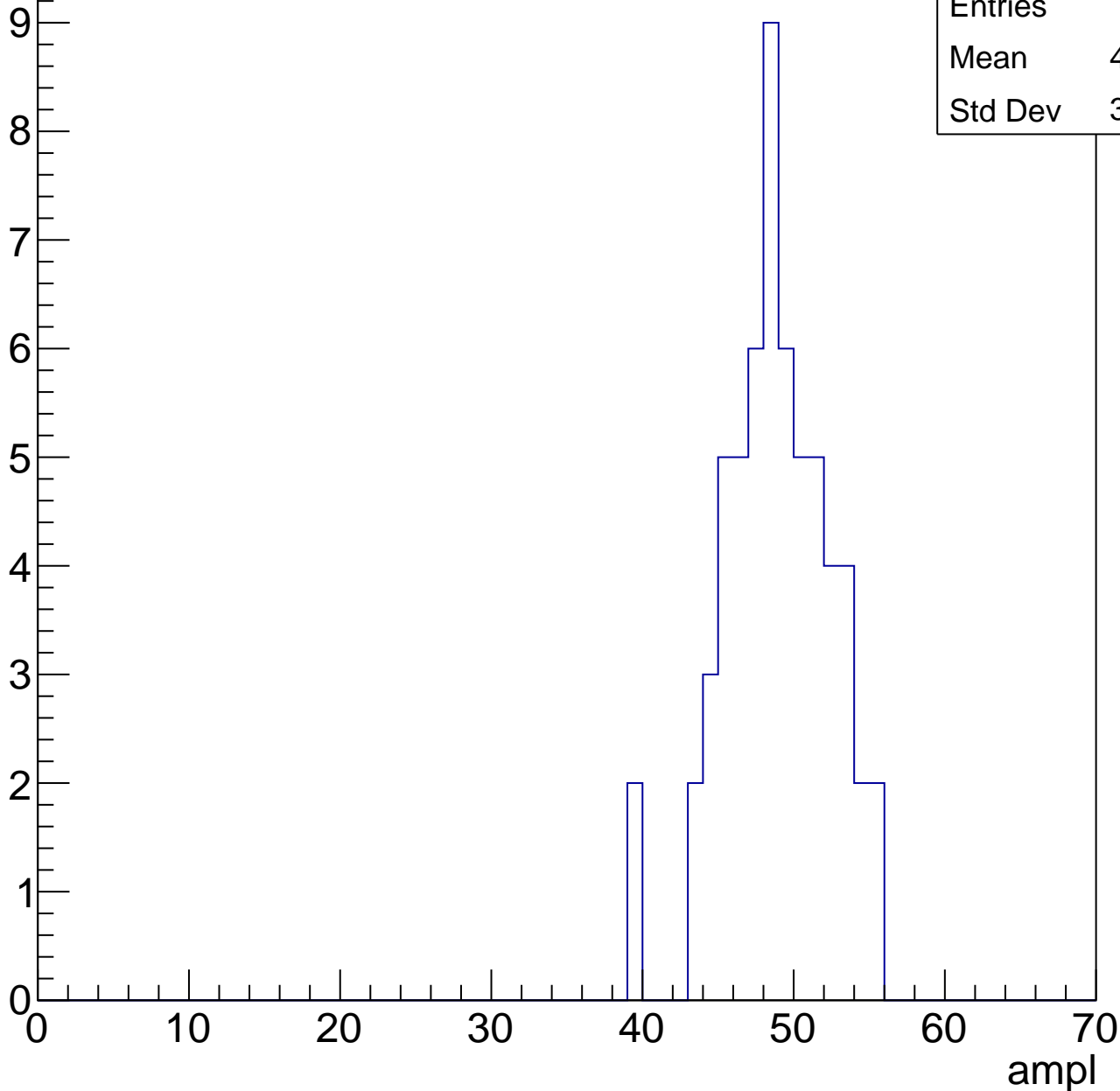


# B1L003S, U18-ch111, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

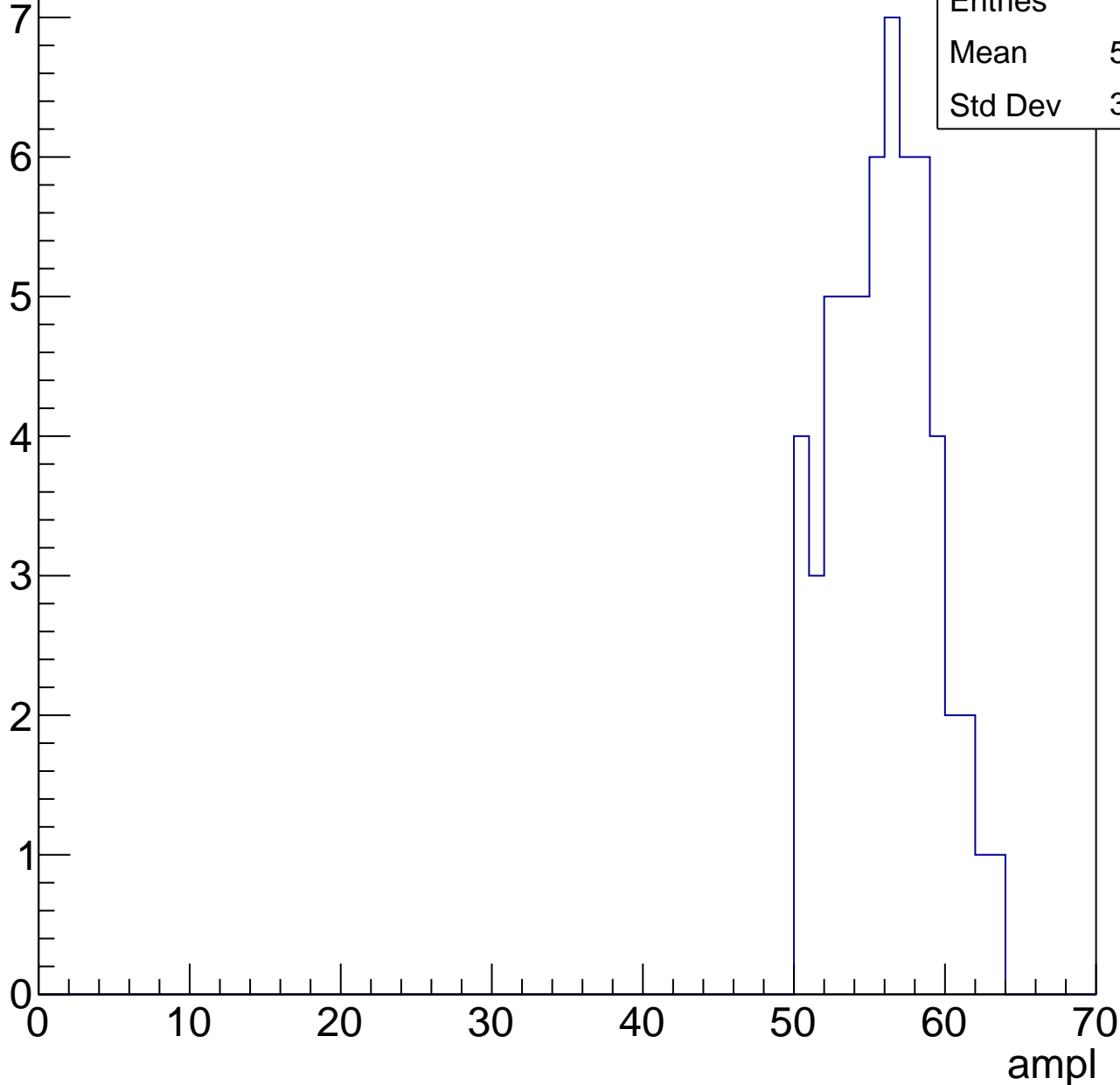
Entries	60
Mean	48.37
Std Dev	3.483



# B1L003S, U18-ch111, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

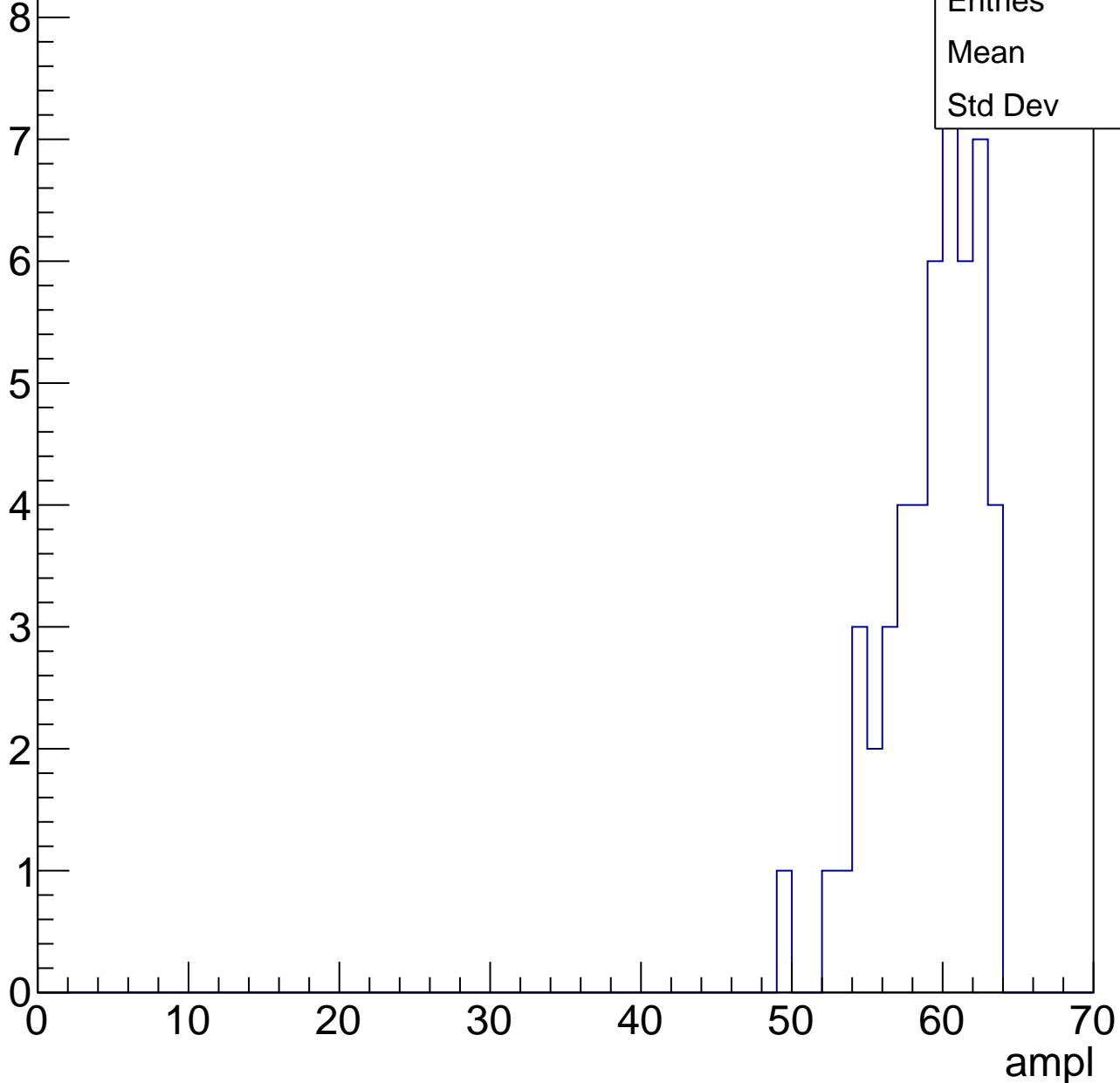


# B1L003S, U18-ch111, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

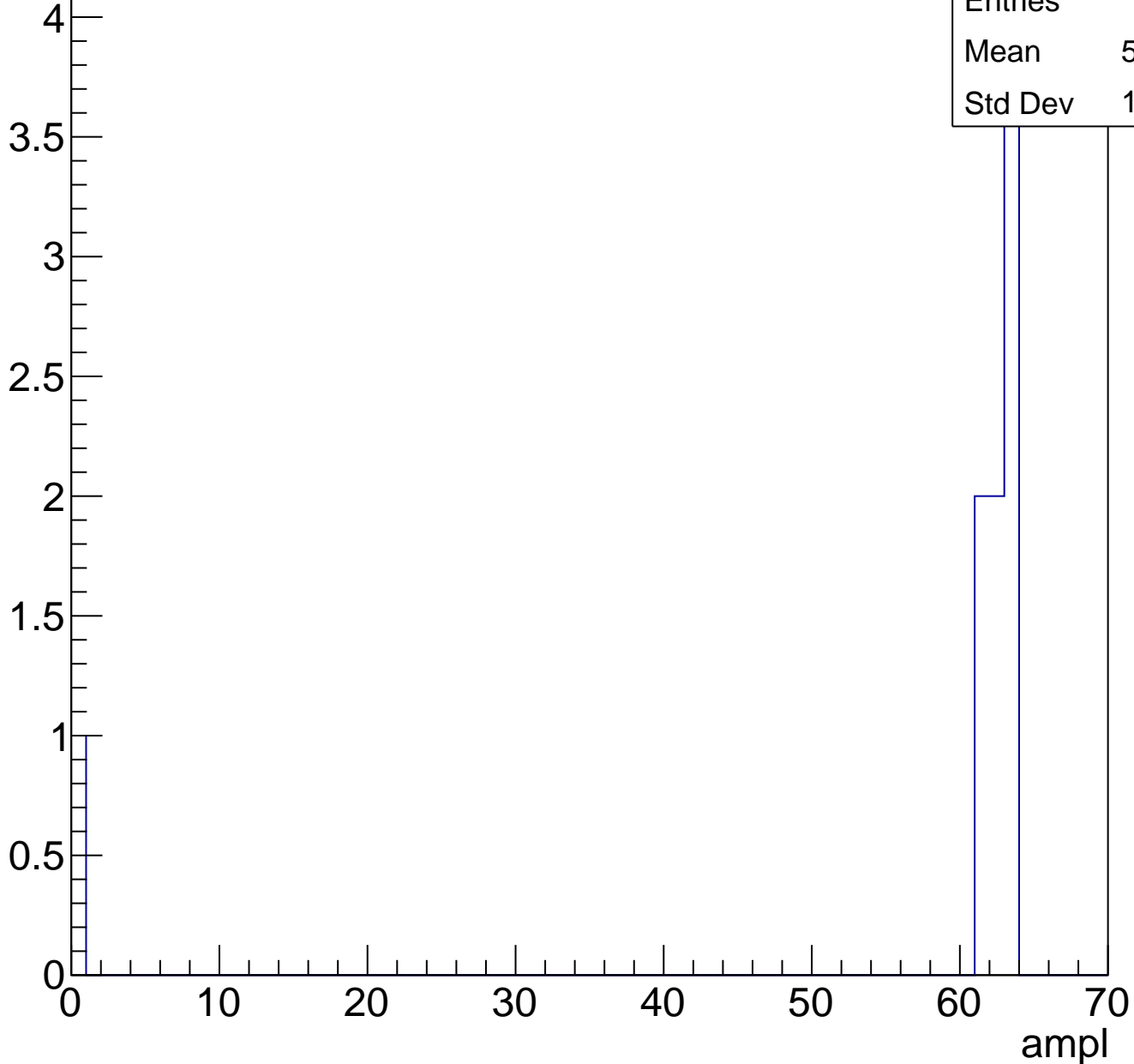
Entries	50
Mean	58.8
Std Dev	3.15



# B1L003S, U18-ch111, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



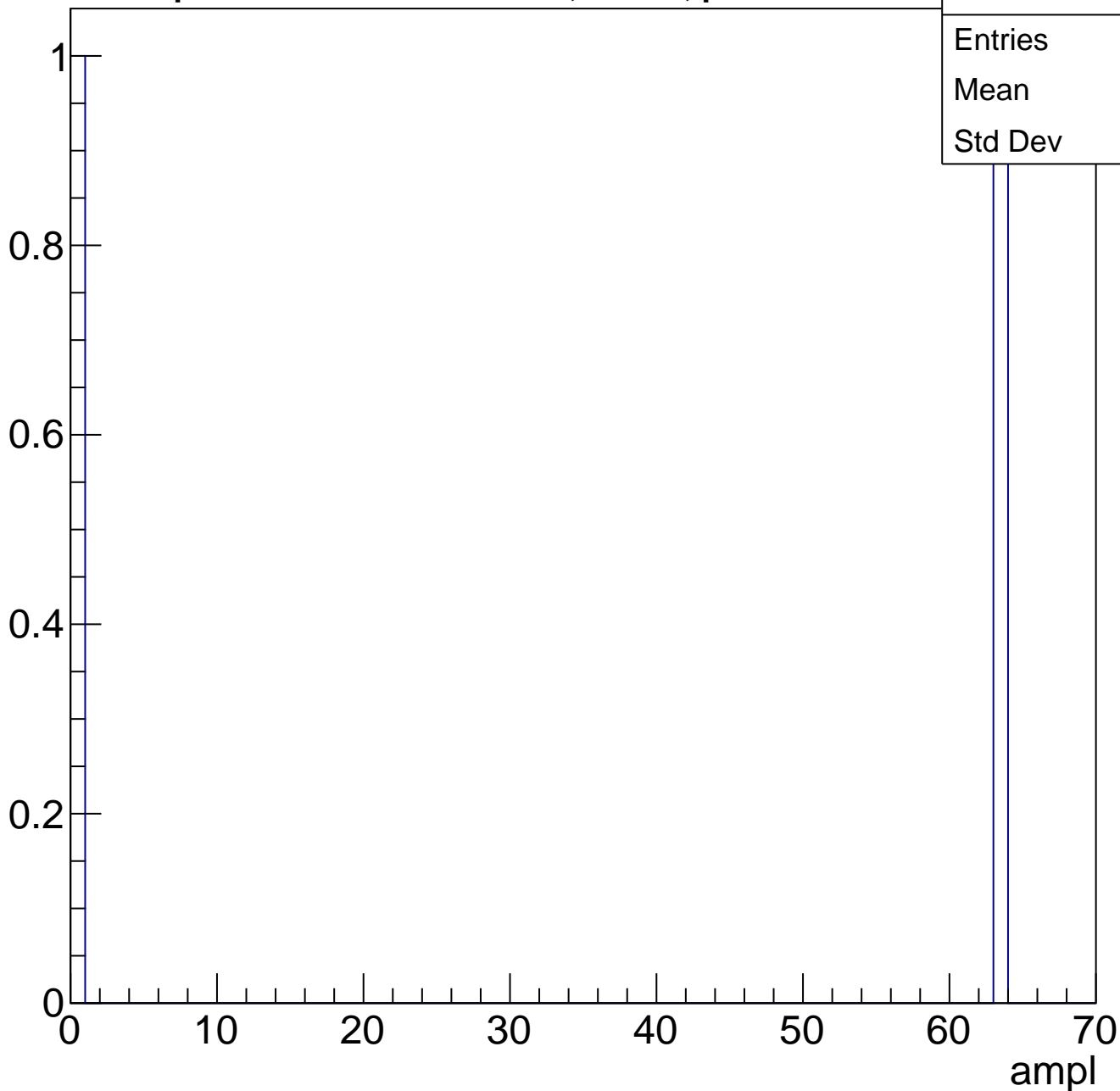
Entries	9
Mean	55.33
Std Dev	19.58



# B1L003S, U18-ch111, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U18-ch112, adc0

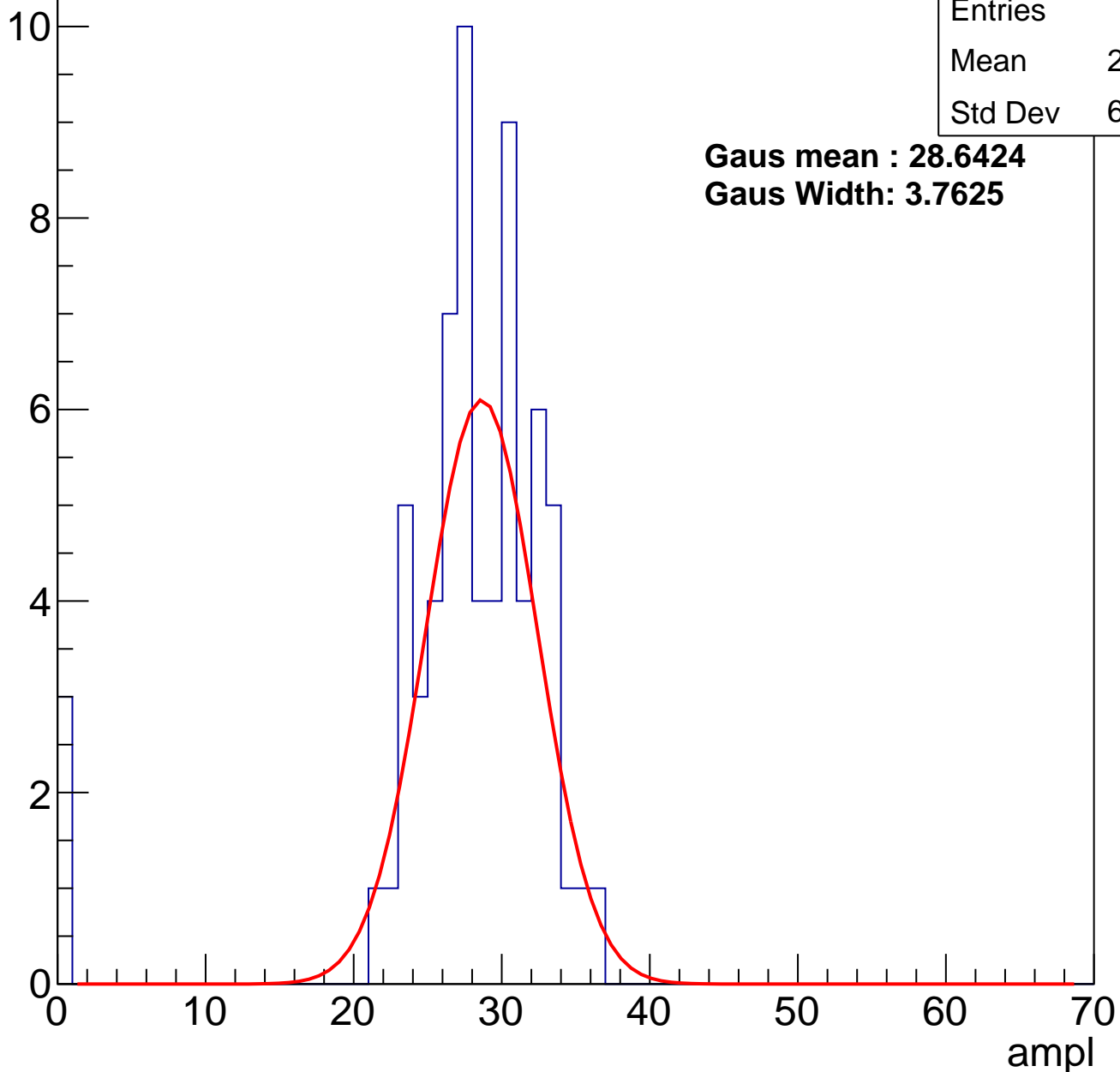
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	69
Mean	27.04
Std Dev	6.667

**Gaus mean : 28.6424**

**Gaus Width: 3.7625**

Entry



# B1L003S, U18-ch112, adc1

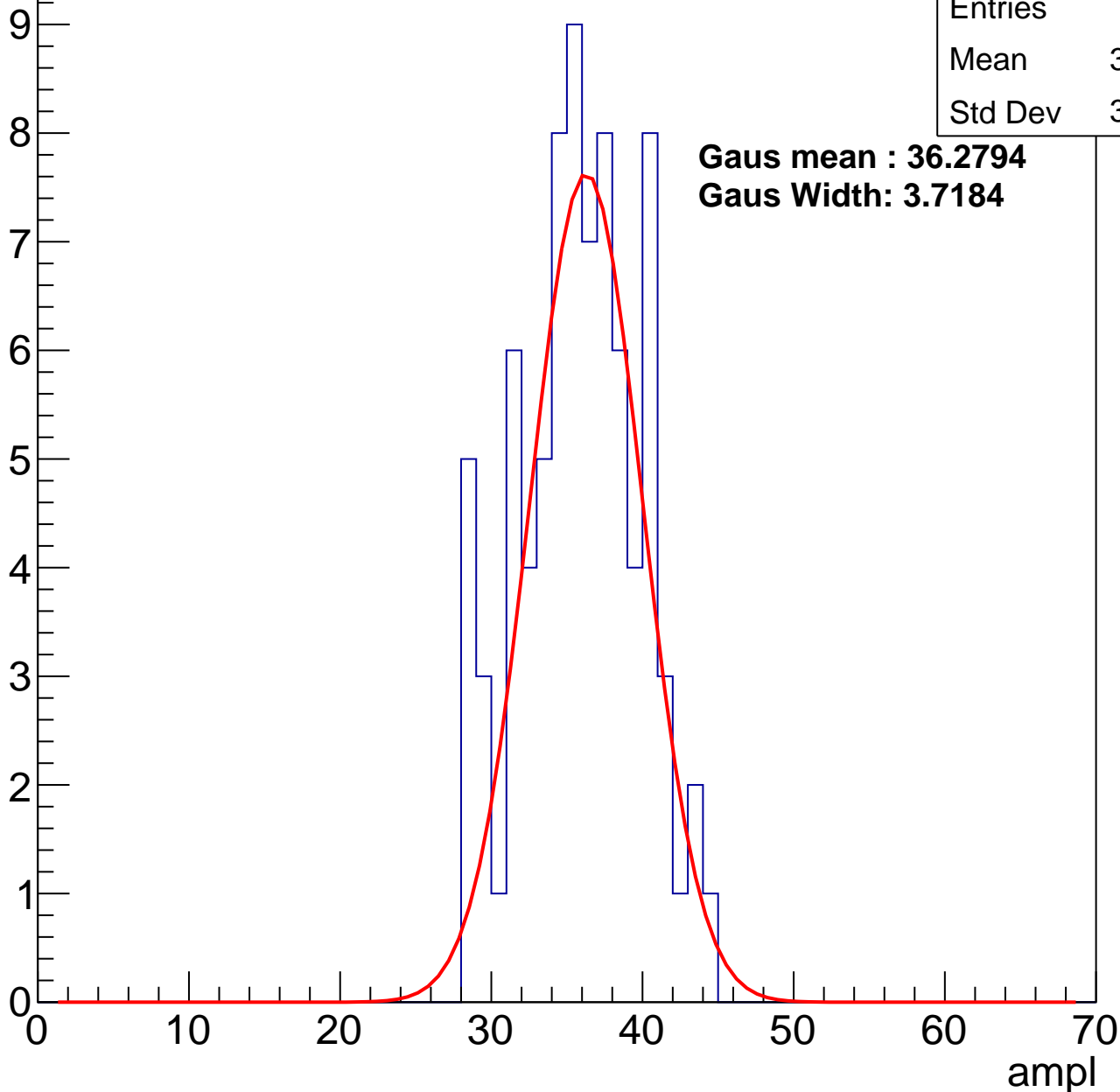
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	81
Mean	35.43
Std Dev	3.922

**Gaus mean : 36.2794**

**Gaus Width: 3.7184**



# B1L003S, U18-ch112, adc2

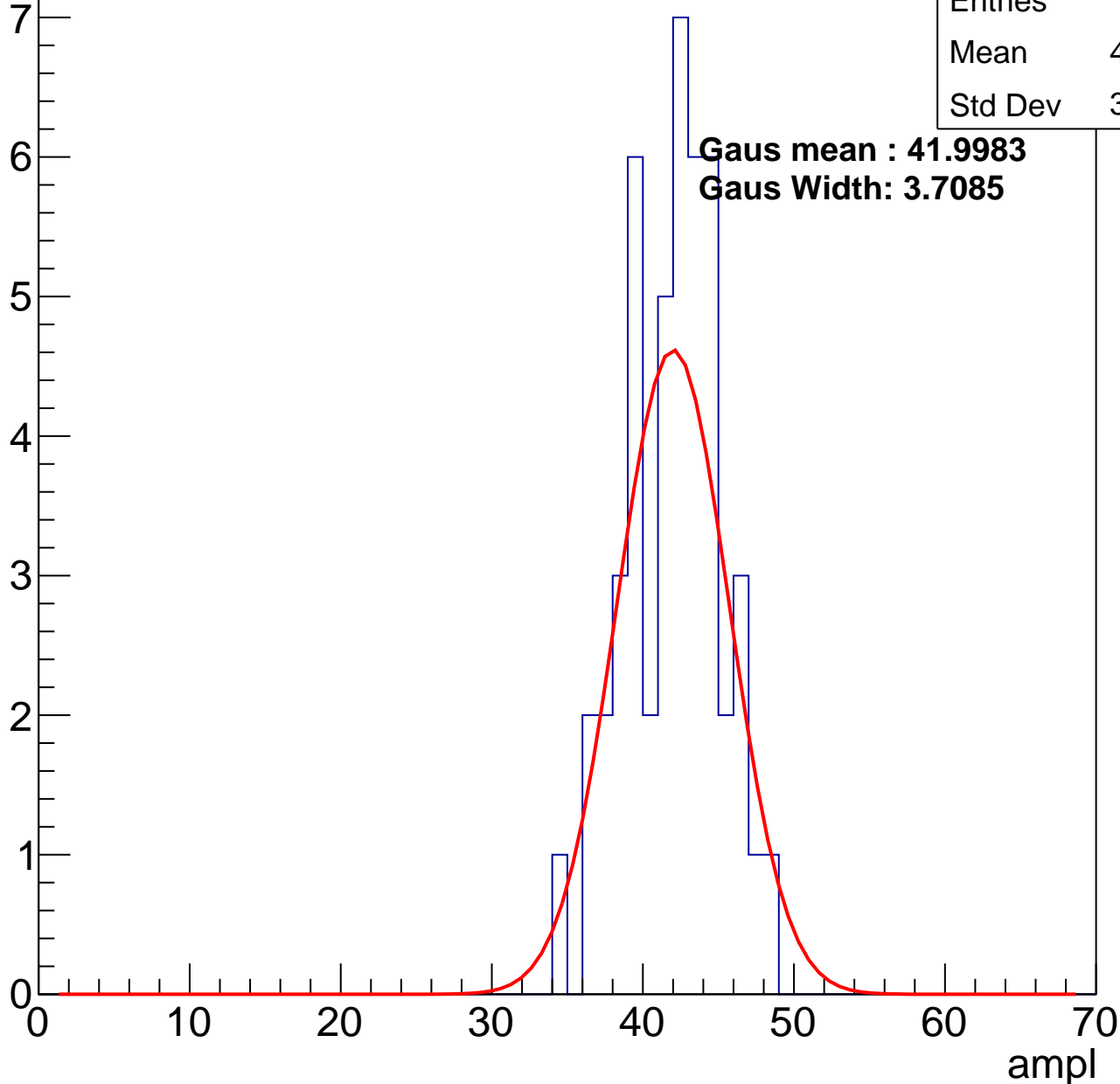
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	47
Mean	41.53
Std Dev	3.086

**Gaus mean : 41.9983**

**Gaus Width: 3.7085**

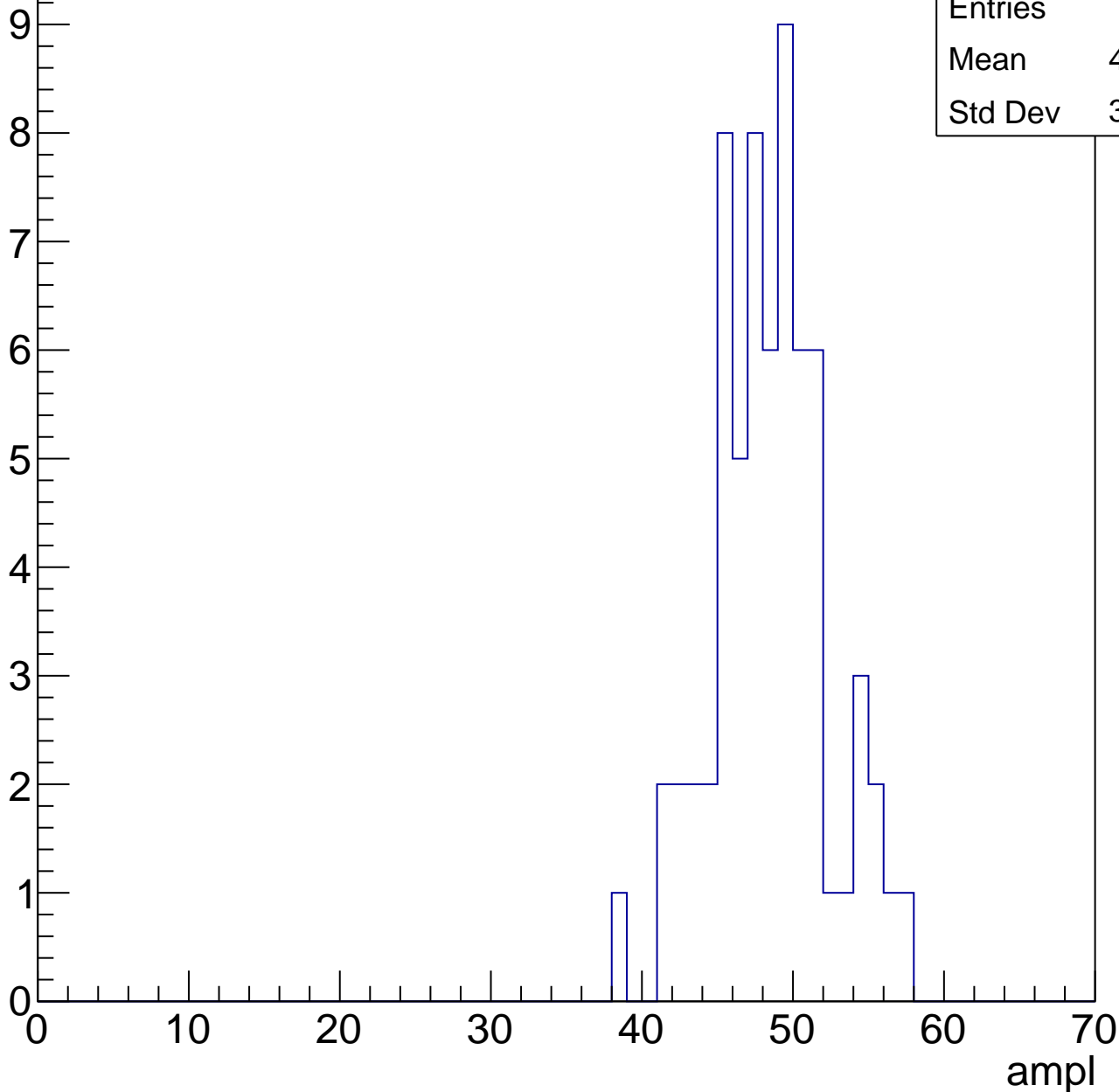


# B1L003S, U18-ch112, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	66
Mean	48.02
Std Dev	3.756

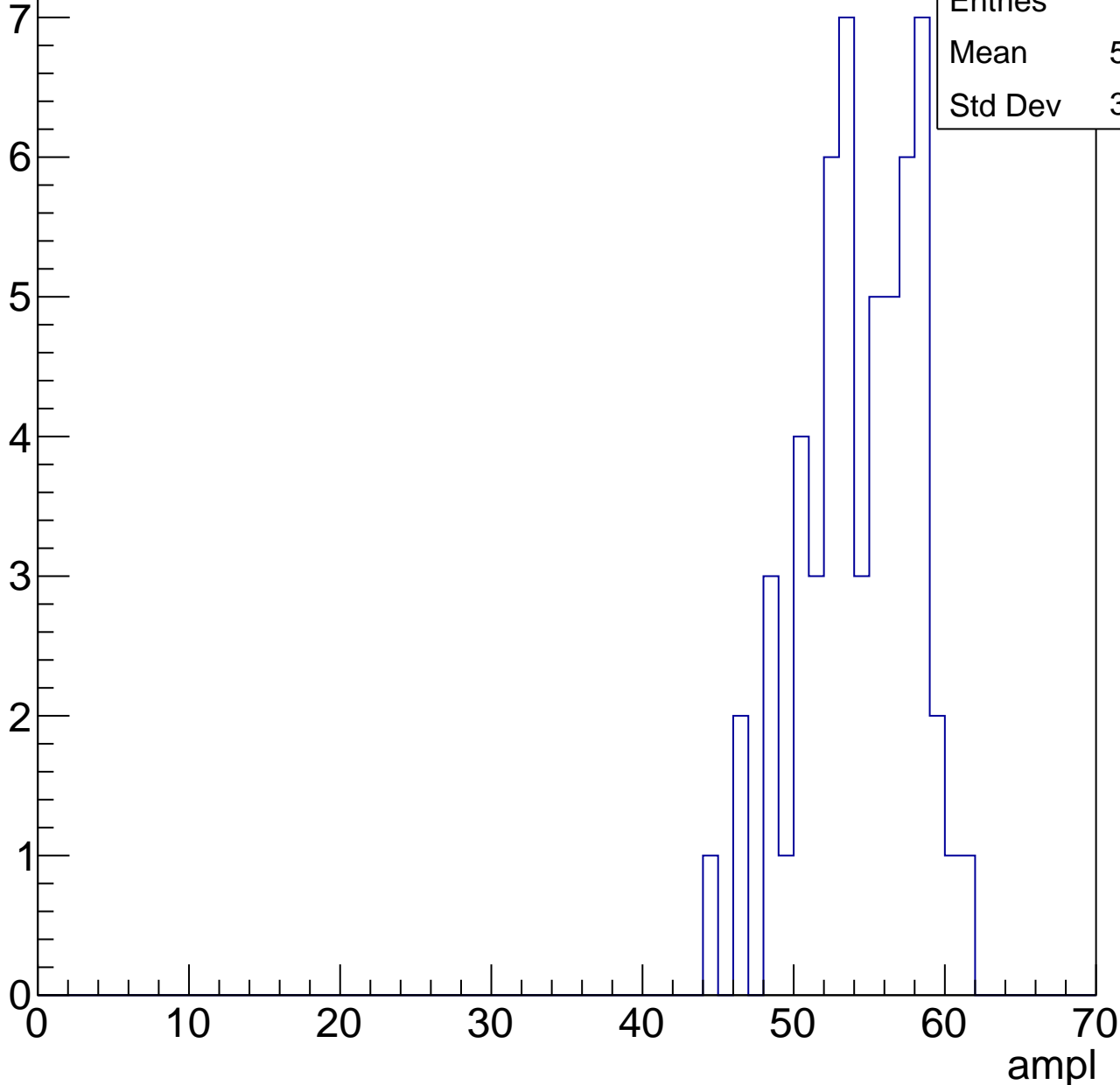


# B1L003S, U18-ch112, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	57
Mean	53.84
Std Dev	3.764

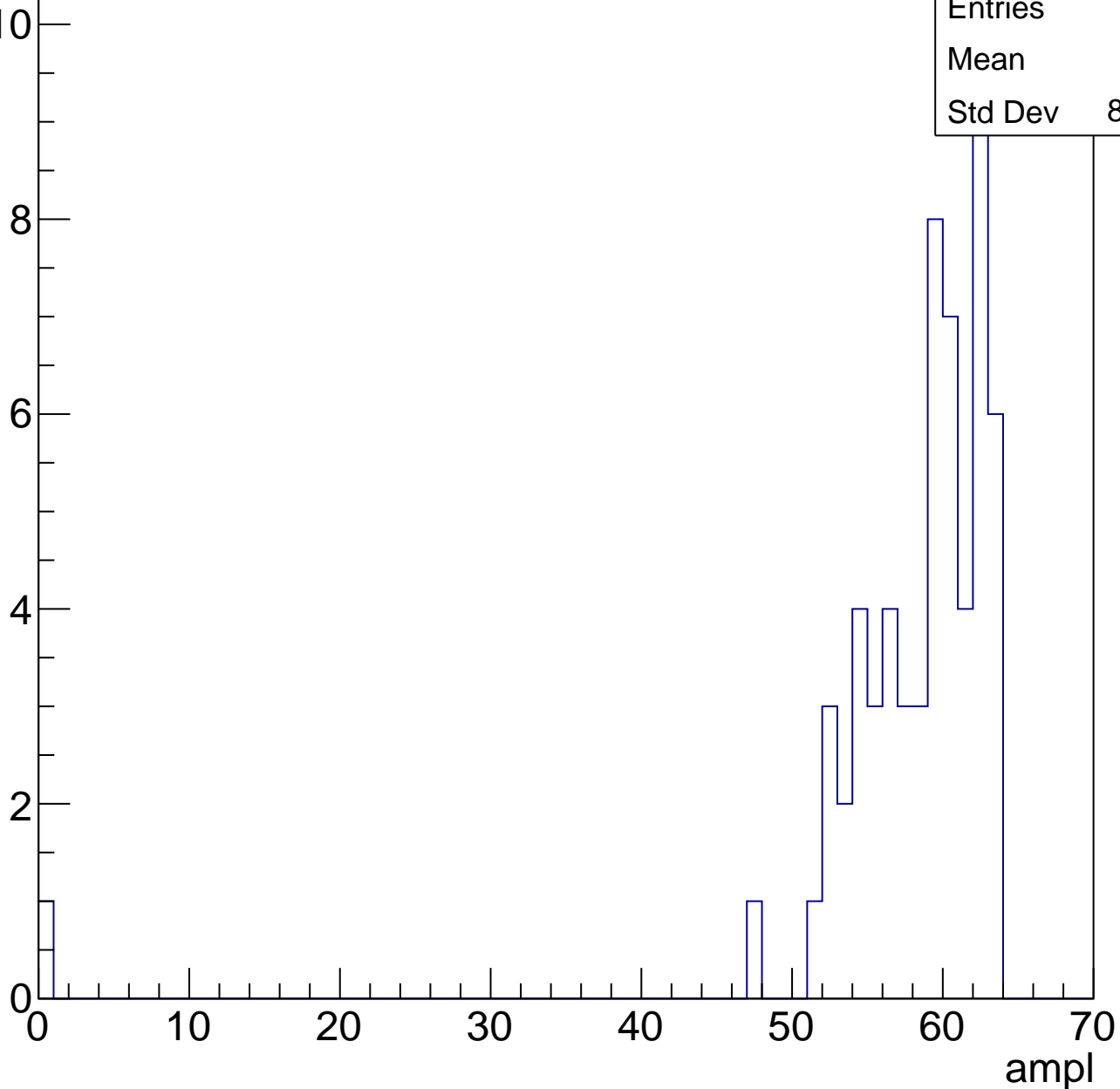


# B1L003S, U18-ch112, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	60
Mean	57.4
Std Dev	8.329

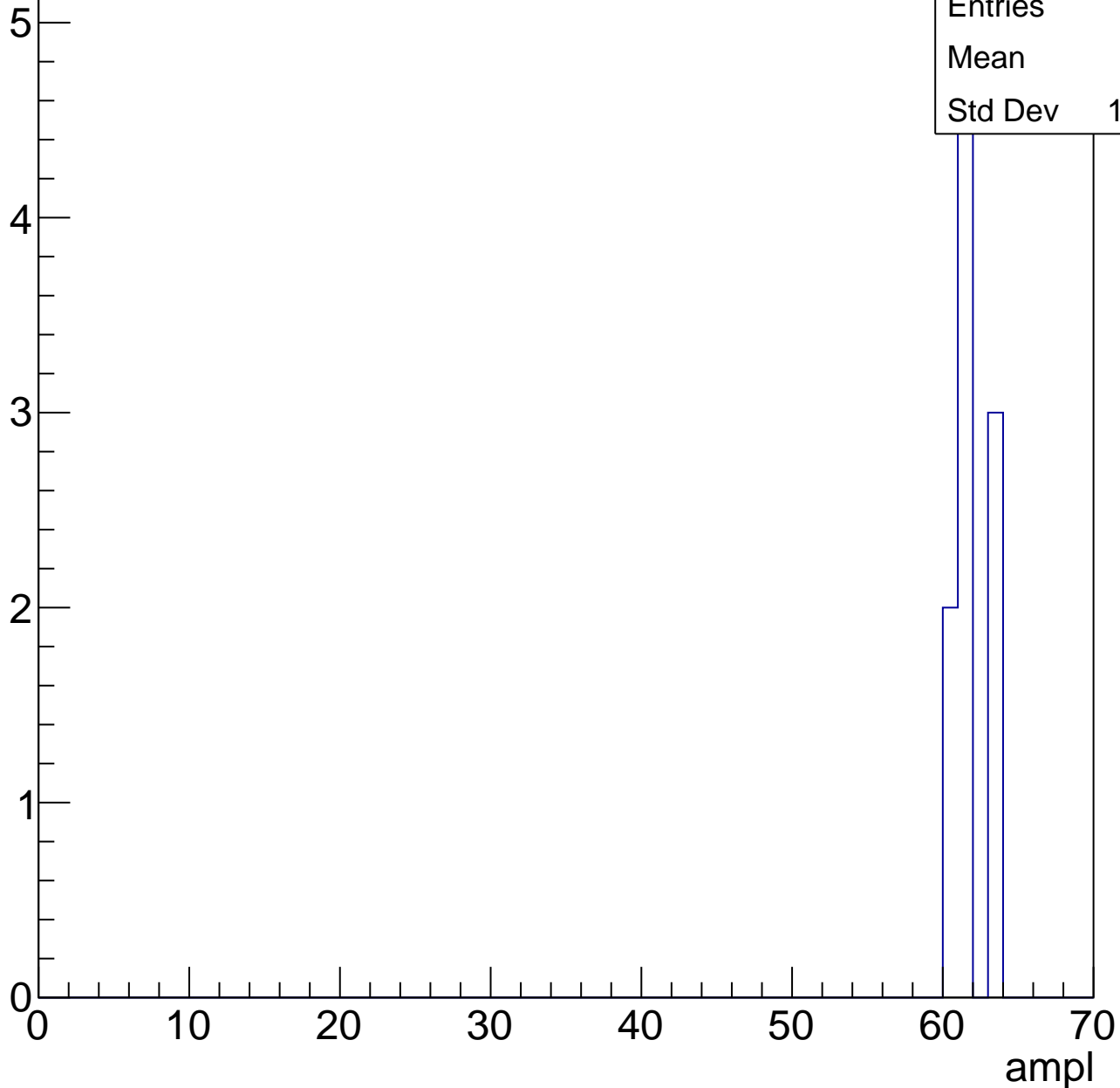


# B1L003S, U18-ch112, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	10
Mean	61.4
Std Dev	1.114





# B1L003S, U18-ch112, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U18-ch113, adc0

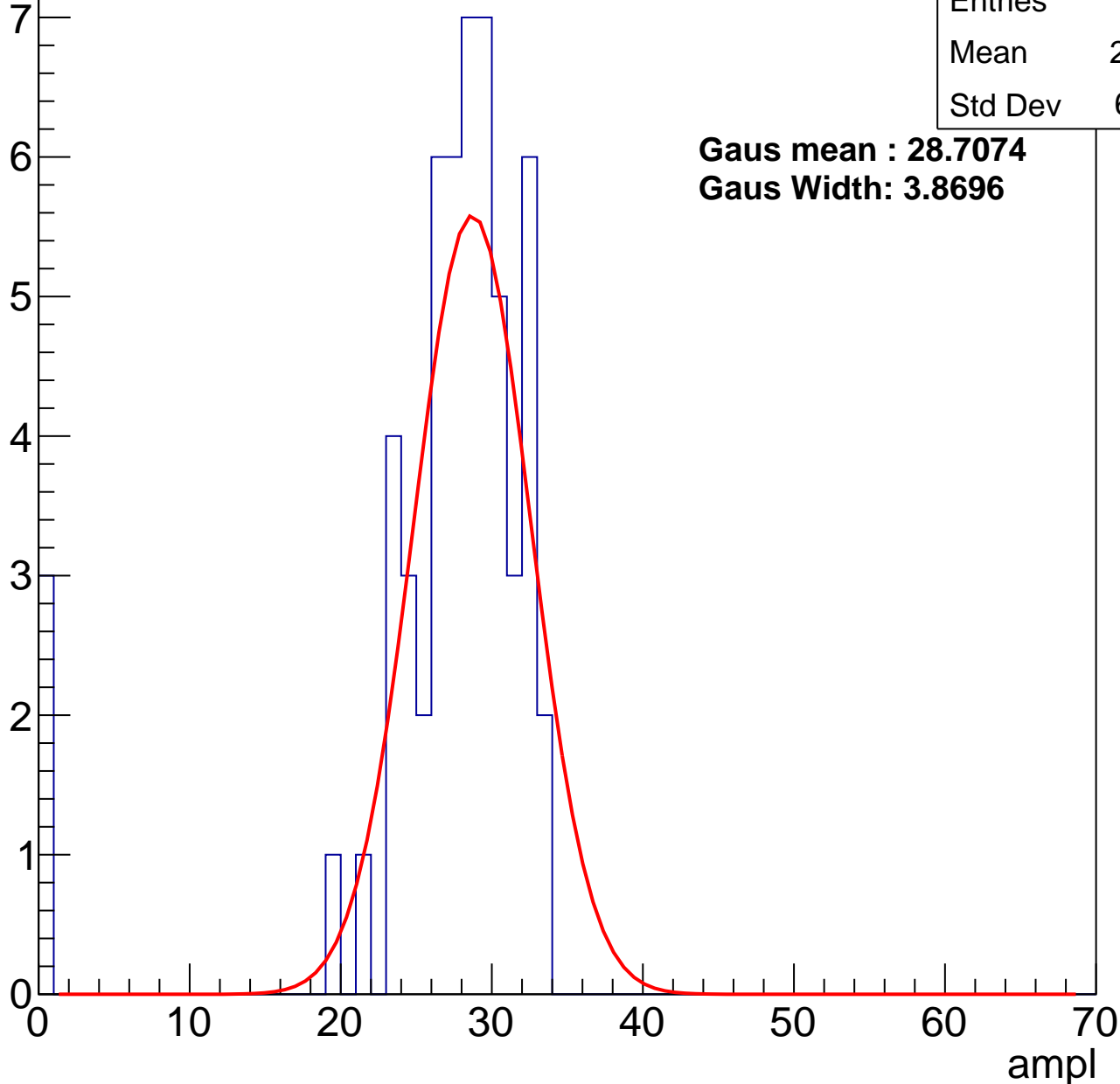
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	56
Mean	26.29
Std Dev	6.961

**Gaus mean : 28.7074**

**Gaus Width: 3.8696**



# B1L003S, U18-ch113, adc1

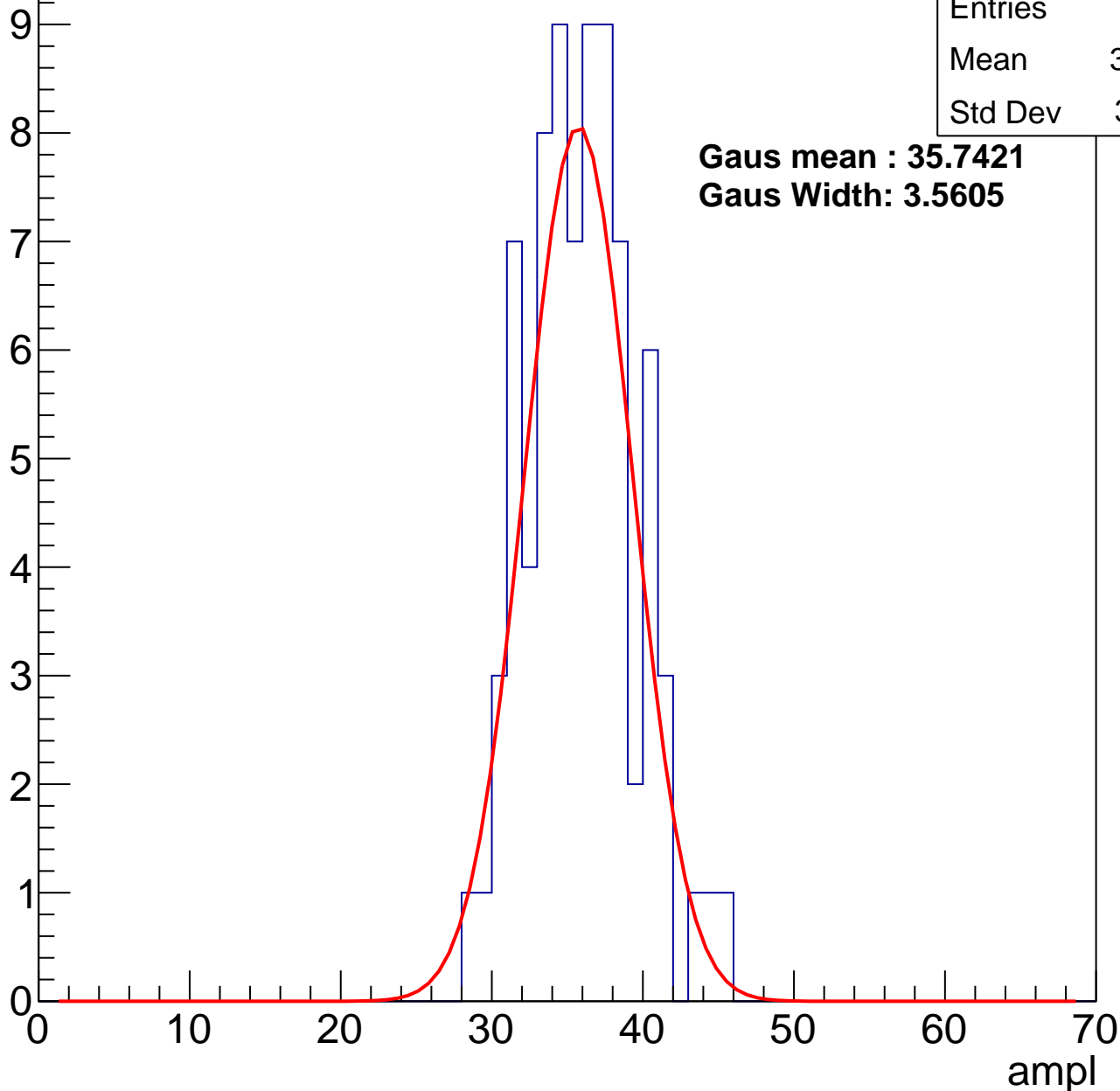
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	79
Mean	35.48
Std Dev	3.511

**Gaus mean : 35.7421**

**Gaus Width: 3.5605**



# B1L003S, U18-ch113, adc2

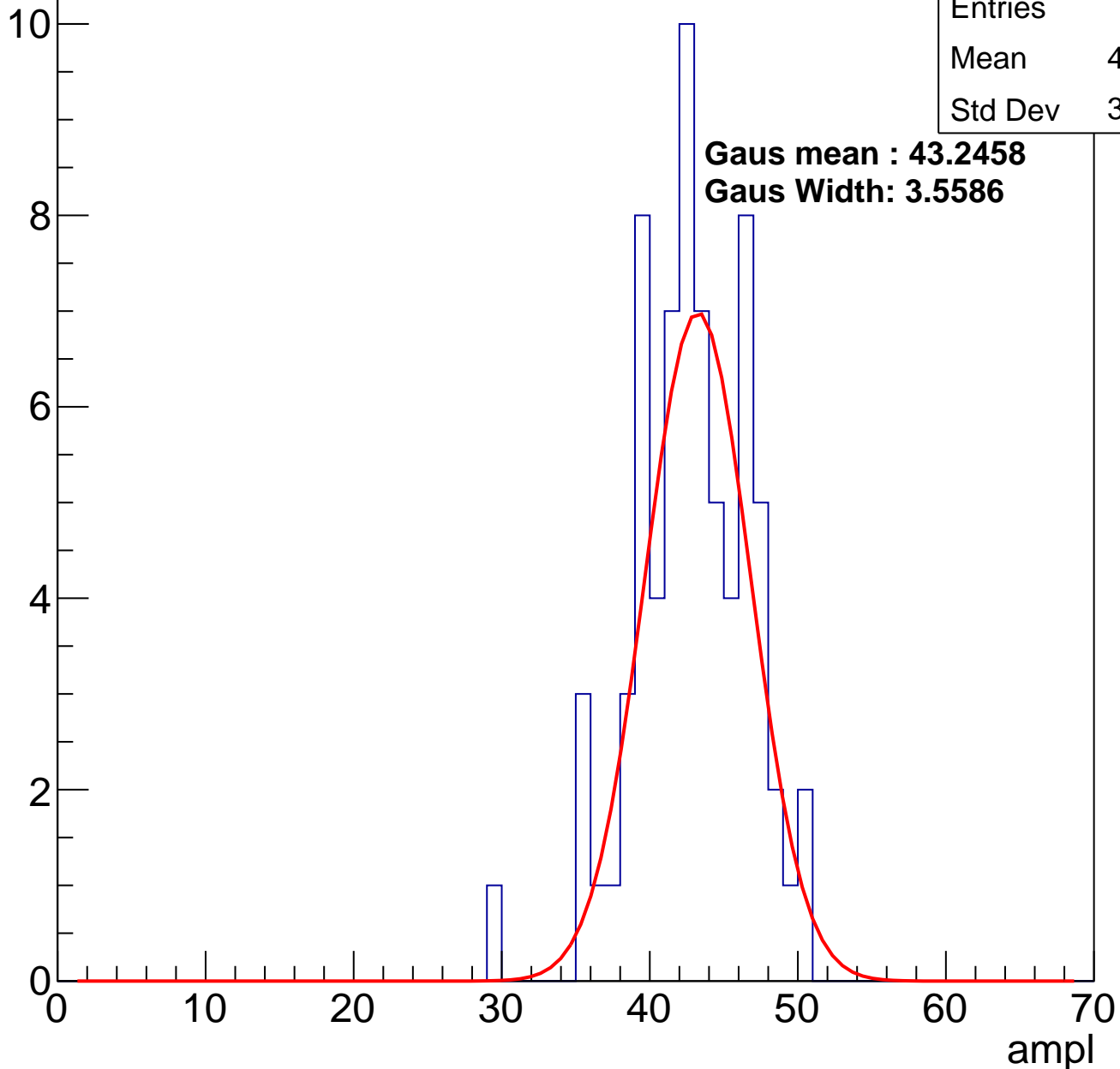
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	72
Mean	42.35
Std Dev	3.866

**Gaus mean : 43.2458**

**Gaus Width: 3.5586**

Entry

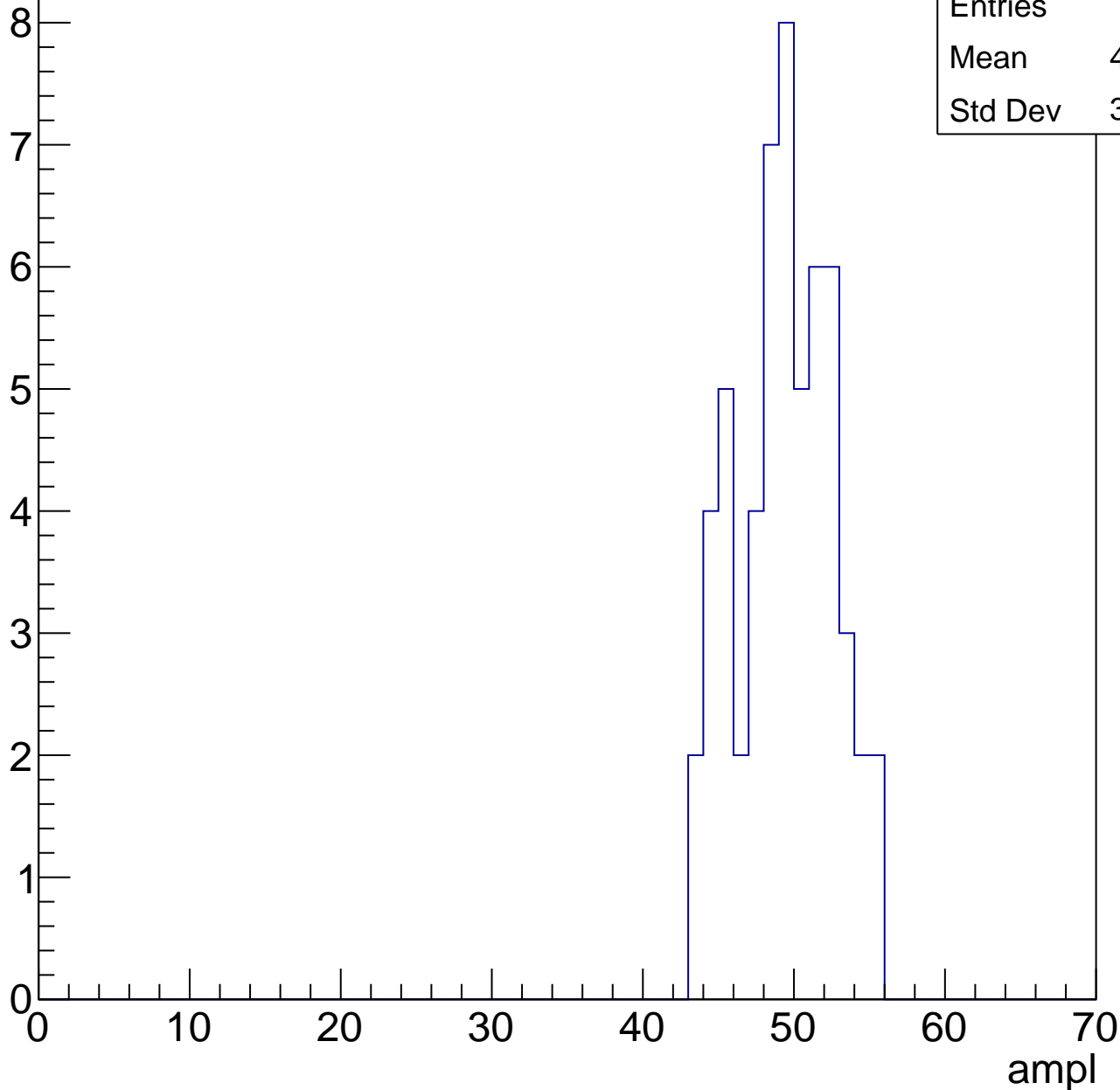


# B1L003S, U18-ch113, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	56
Mean	48.93
Std Dev	3.122

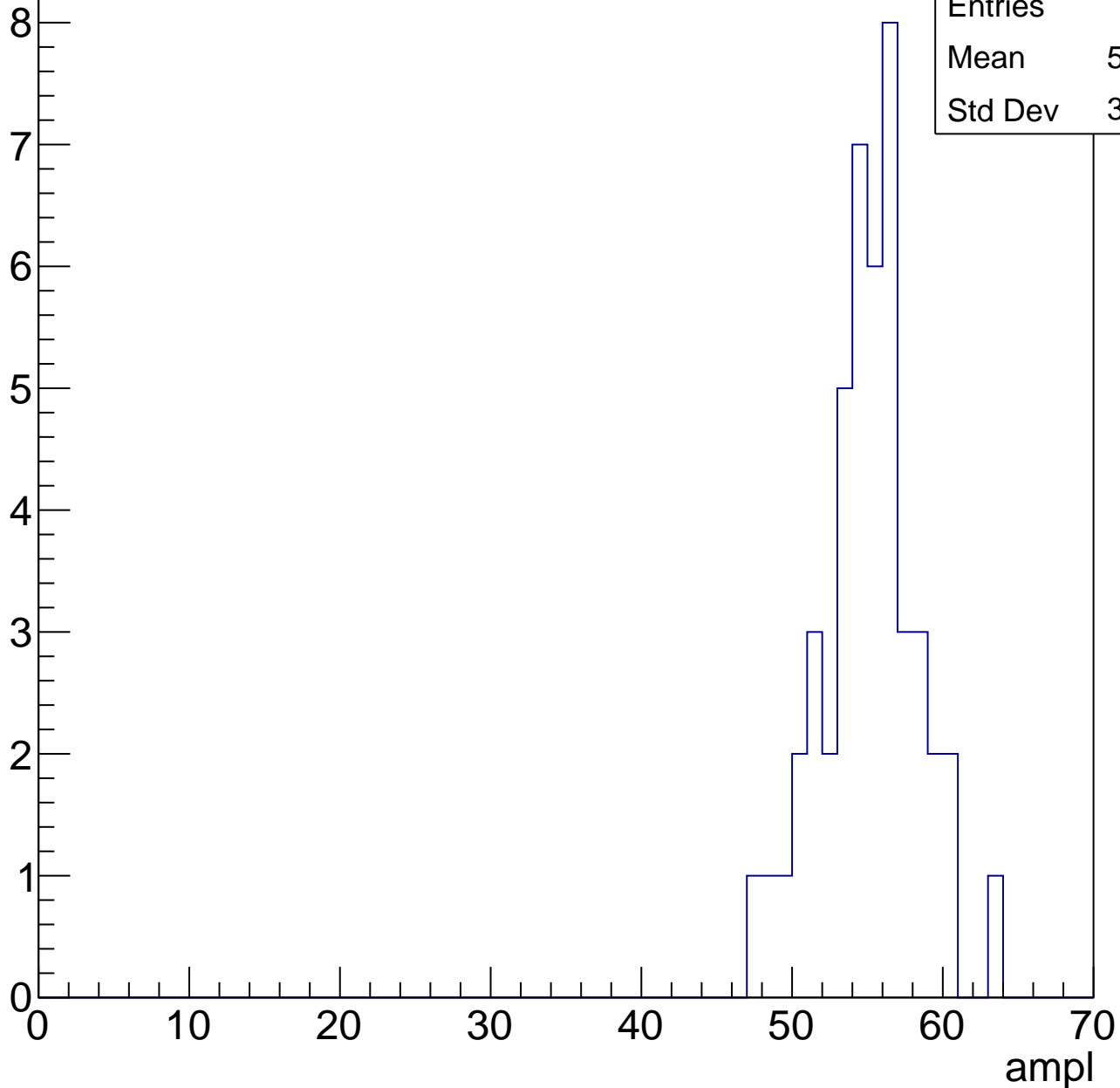


# B1L003S, U18-ch113, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	47
Mean	54.64
Std Dev	3.192

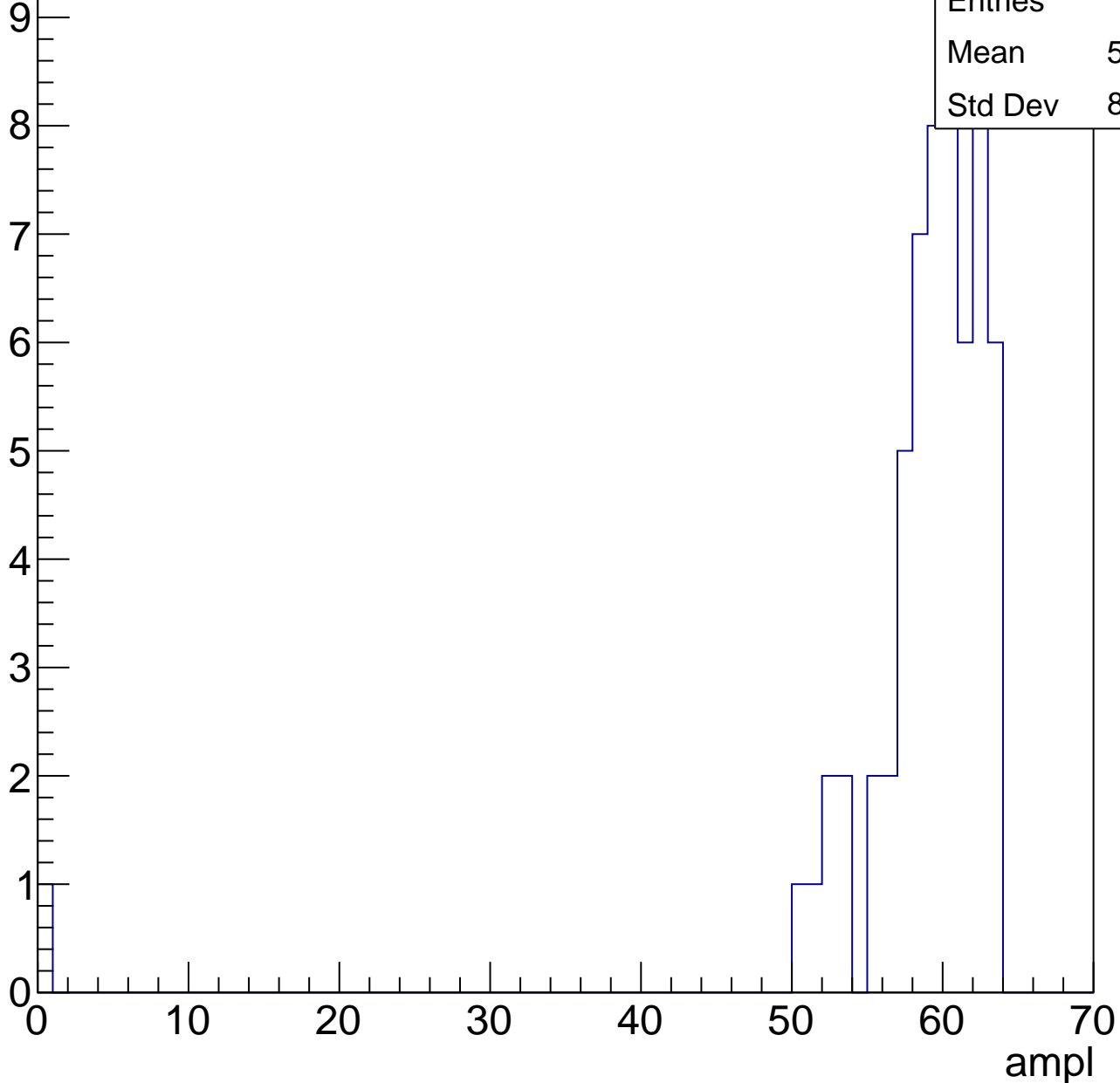


# B1L003S, U18-ch113, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

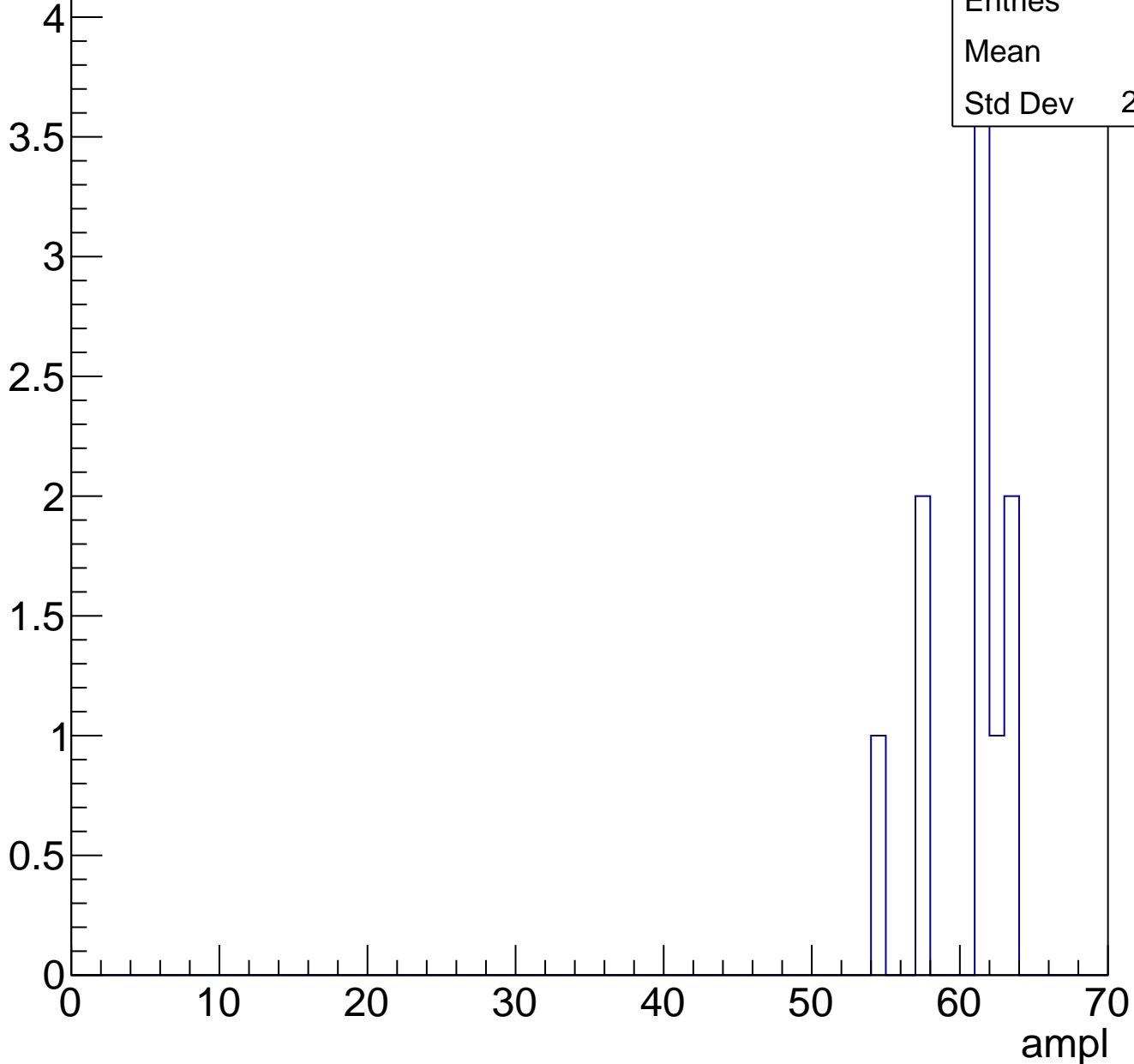
Entries	60
Mean	57.97
Std Dev	8.183



# B1L003S, U18-ch113, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U18-ch113, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U18-ch114, adc0

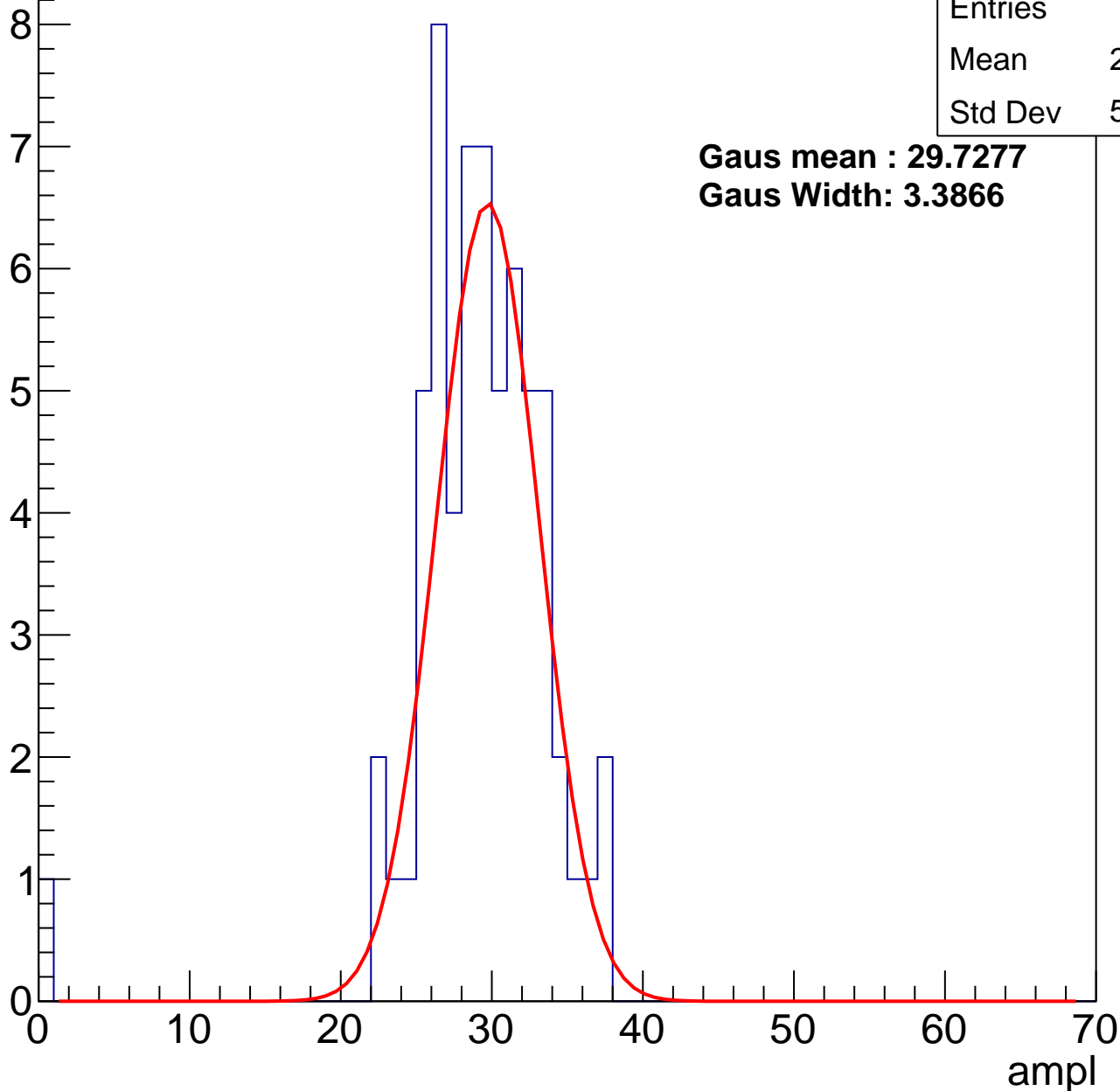
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	63
Mean	28.65
Std Dev	5.015

**Gaus mean : 29.7277**

**Gaus Width: 3.3866**



# B1L003S, U18-ch114, adc1

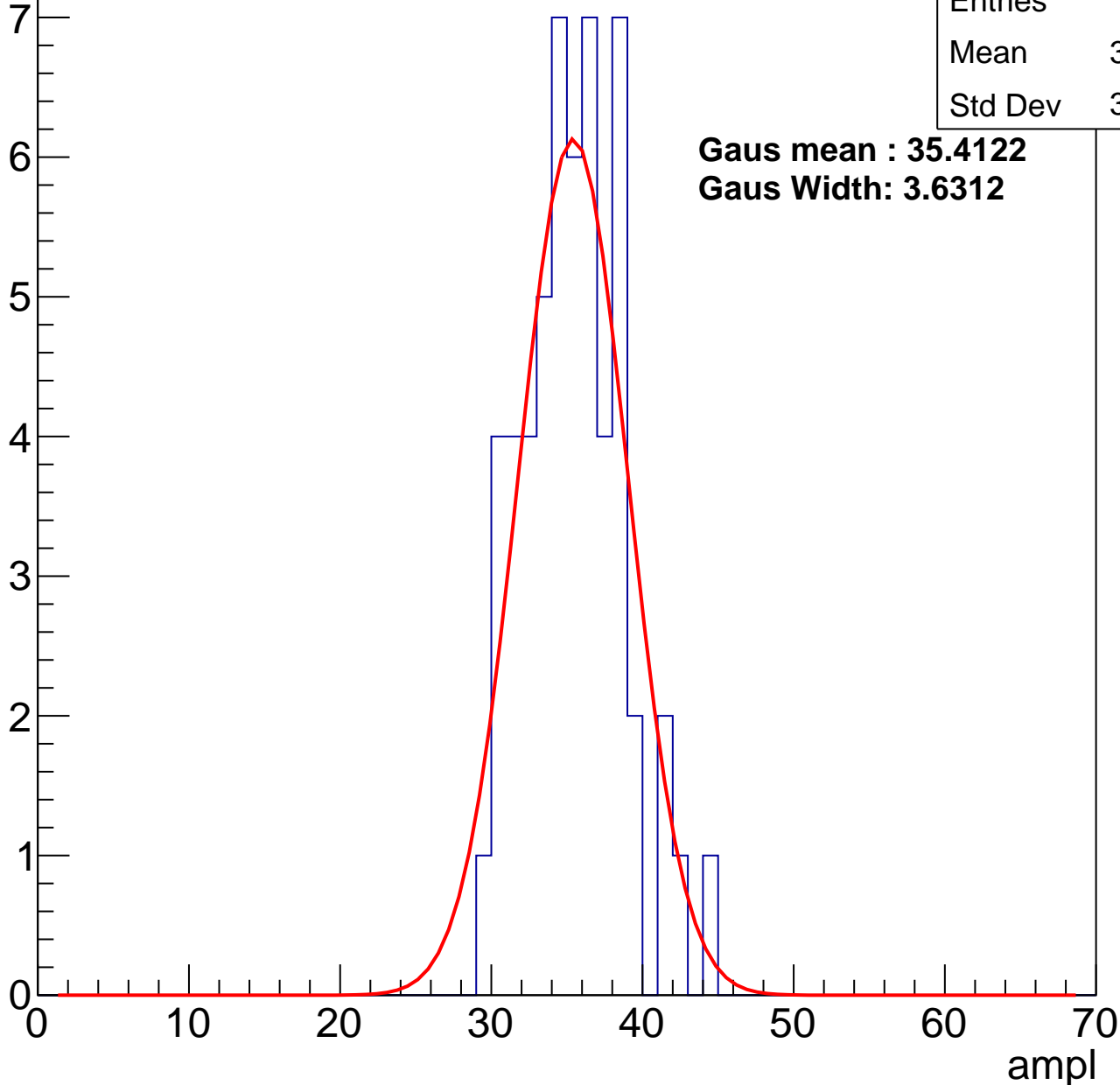
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	55
Mean	35.02
Std Dev	3.256

**Gaus mean : 35.4122**

**Gaus Width: 3.6312**



# B1L003S, U18-ch114, adc2

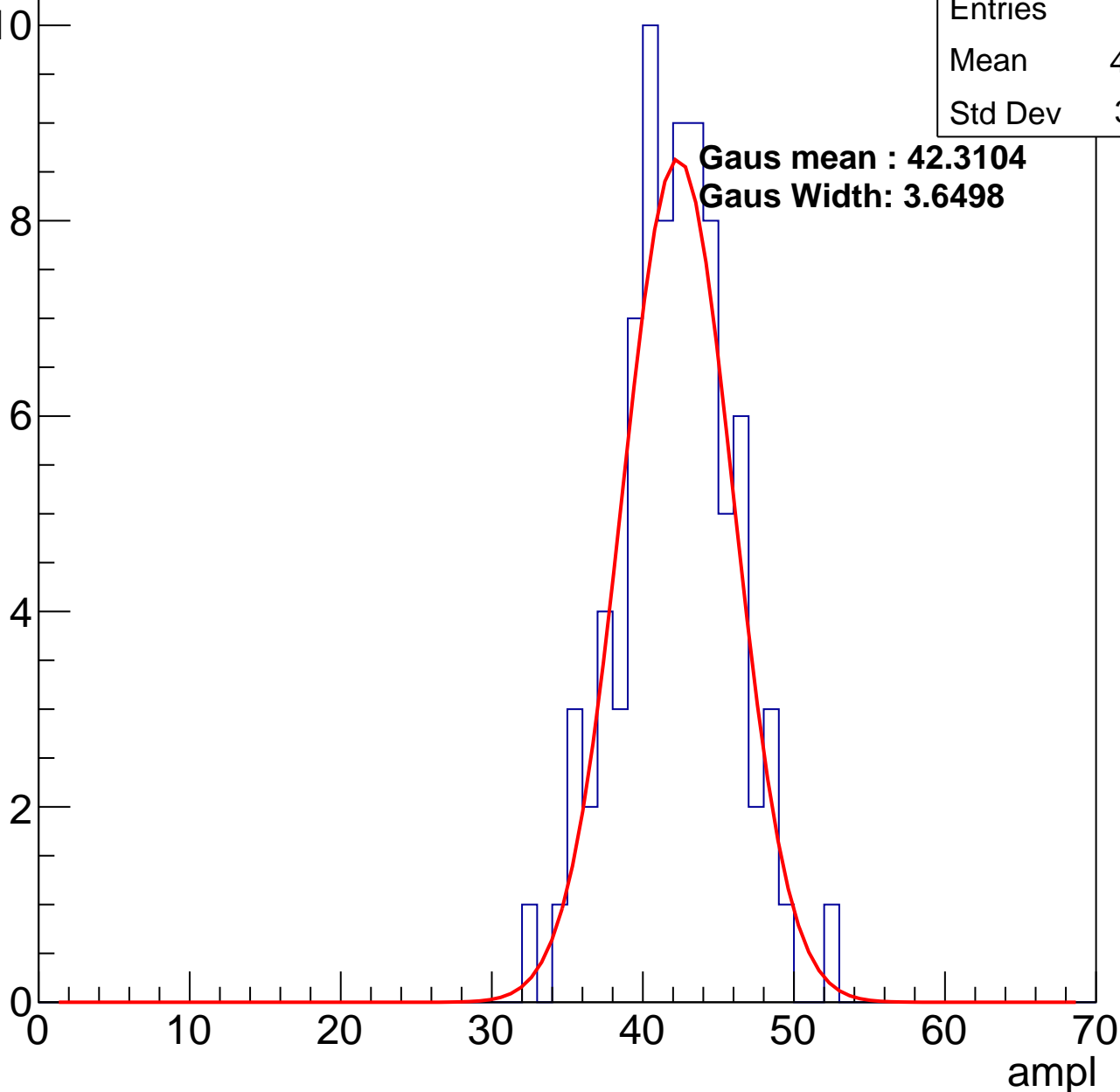
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	83
Mean	41.72
Std Dev	3.681

**Gaus mean : 42.3104**

**Gaus Width: 3.6498**

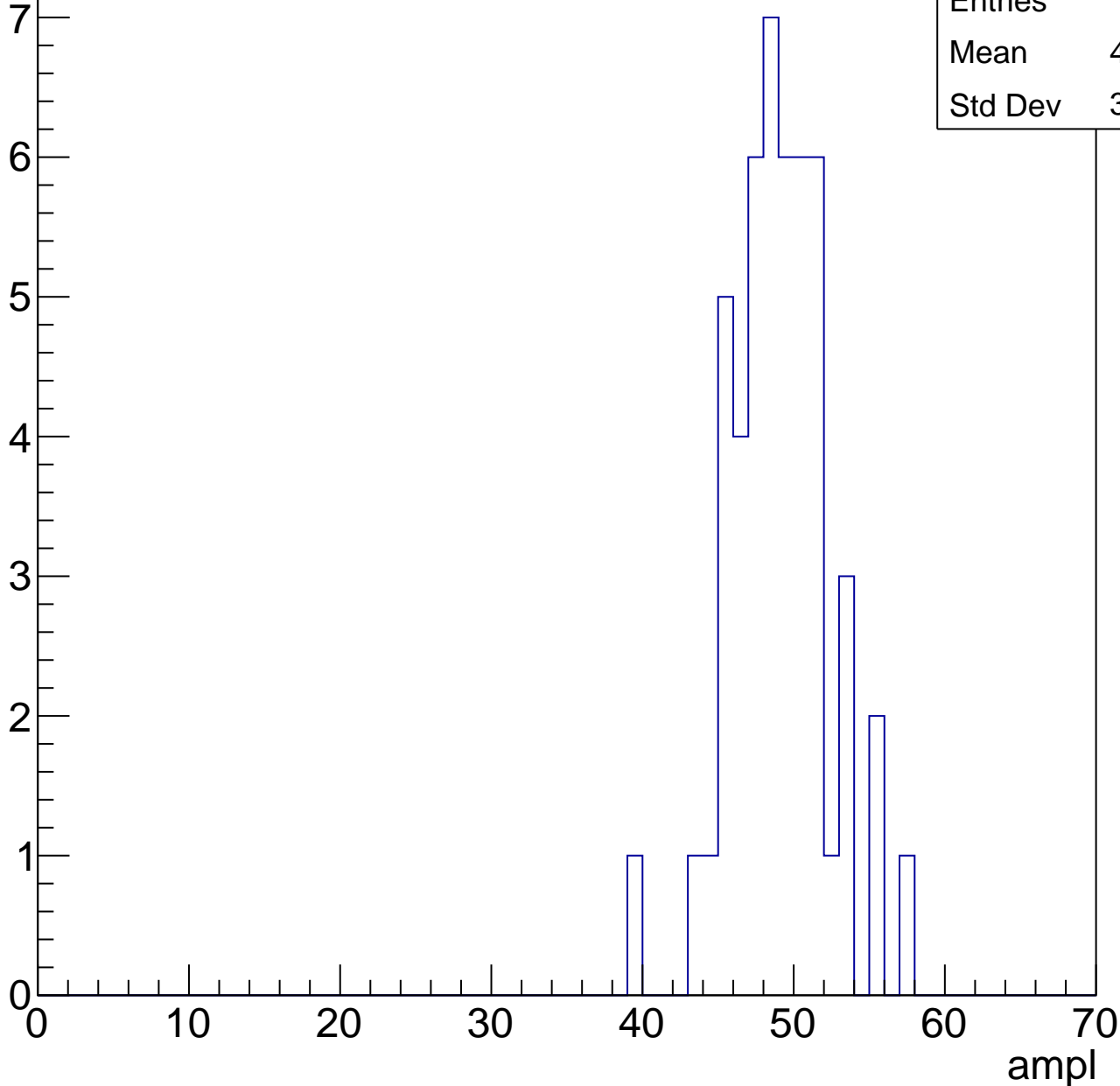


# B1L003S, U18-ch114, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	50
Mean	48.62
Std Dev	3.237

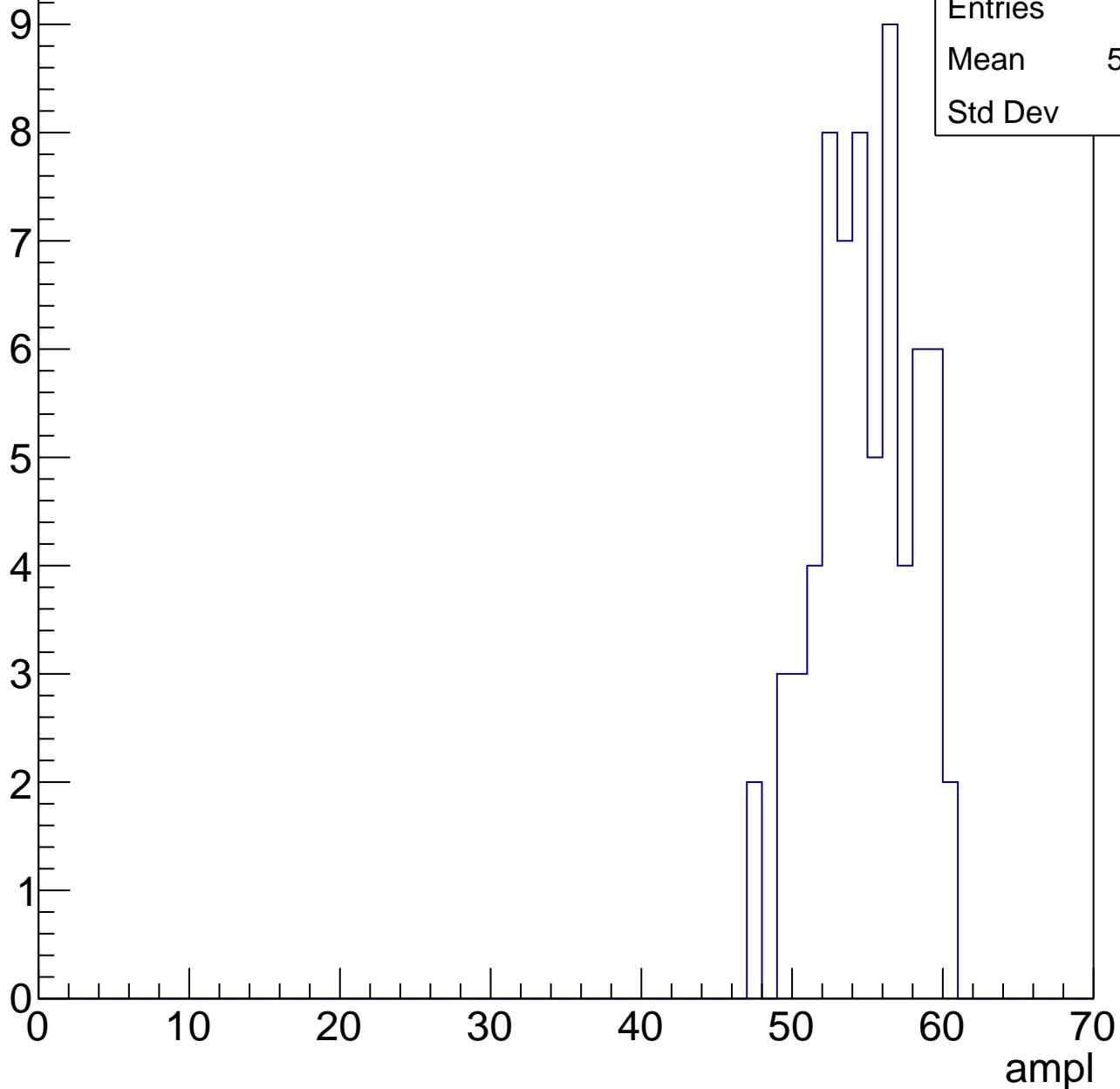


# B1L003S, U18-ch114, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	67
Mean	54.37
Std Dev	3.19



# B1L003S, U18-ch114, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	48
Mean	59.46
Std Dev	2.908

Entry

10

8

6

4

2

0

0

10

20

30

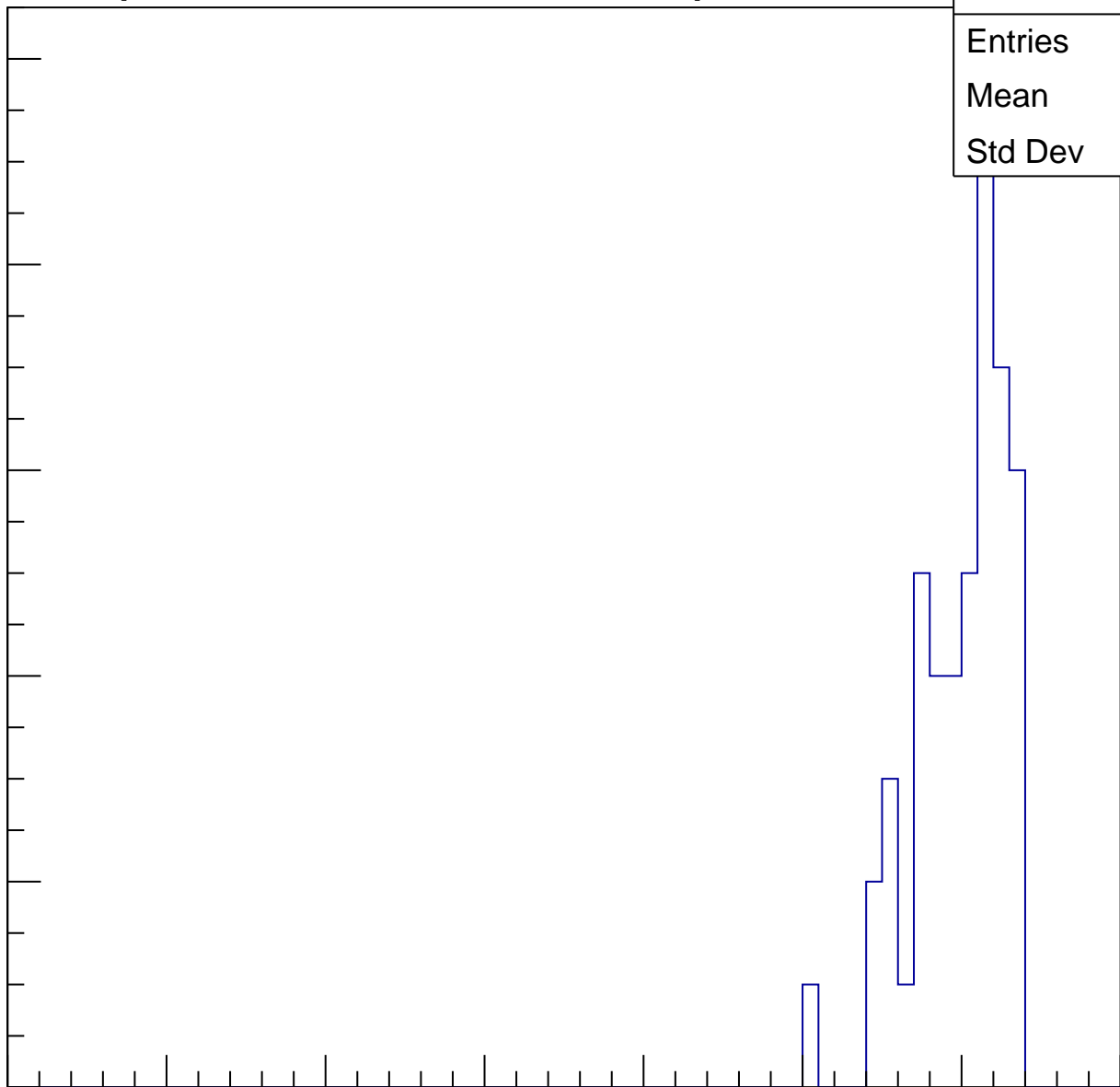
40

50

60

70

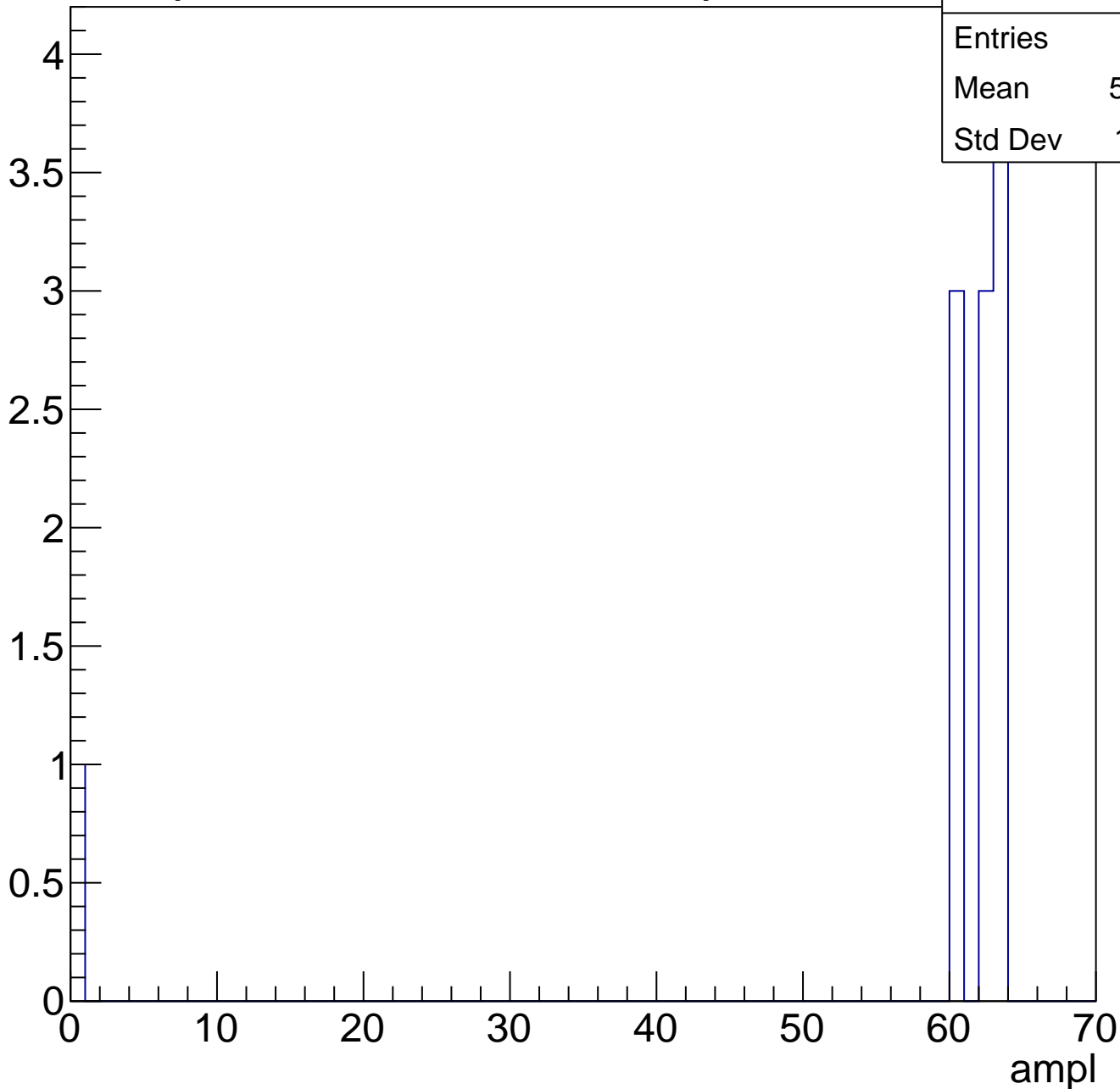
ampl



# B1L003S, U18-ch114, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



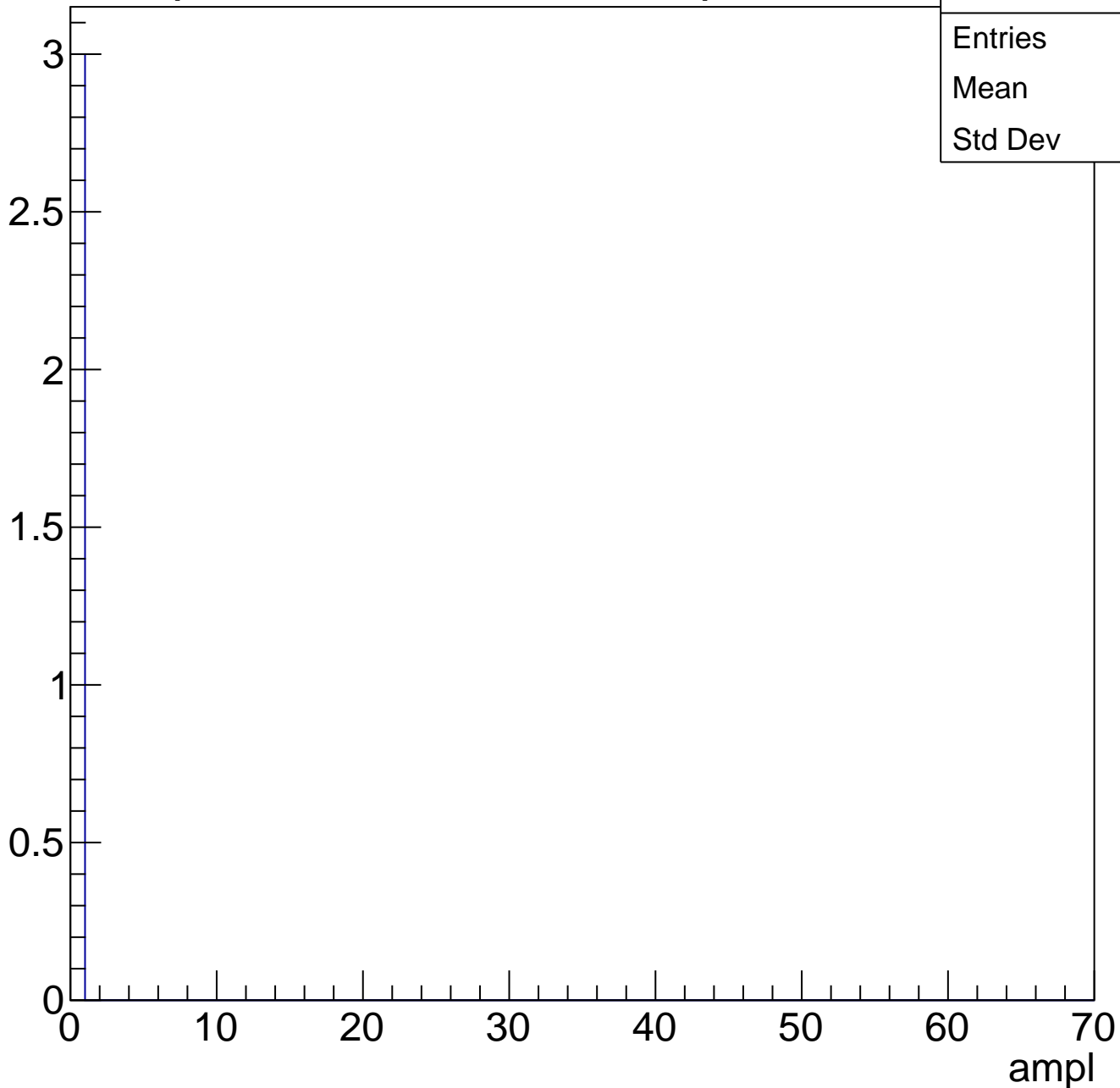
Entries	11
Mean	56.18
Std Dev	17.81



# B1L003S, U18-ch114, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	3
Mean	0
Std Dev	0

# B1L003S, U18-ch115, adc0

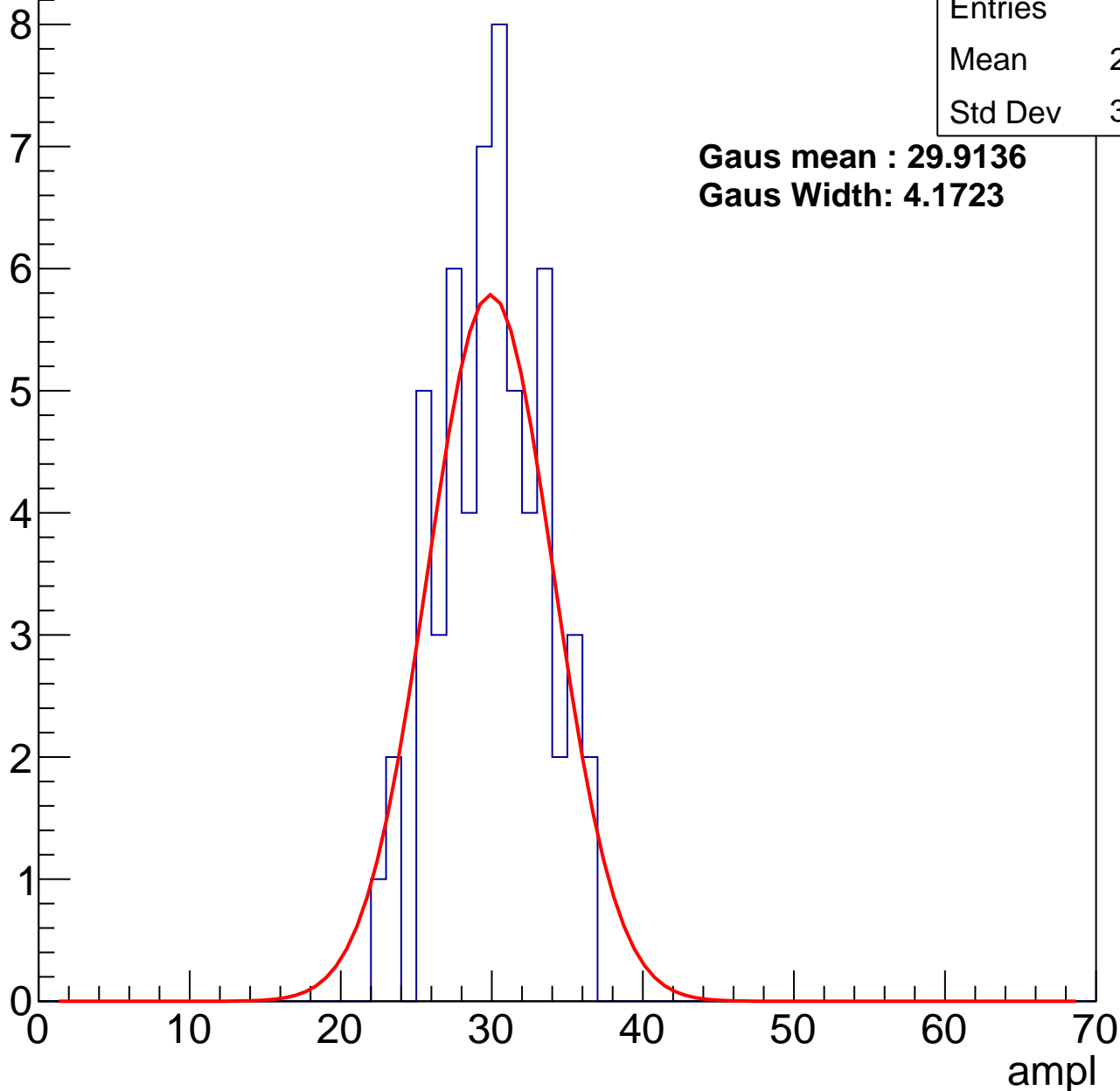
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	58
Mean	29.55
Std Dev	3.359

**Gaus mean : 29.9136**

**Gaus Width: 4.1723**



# B1L003S, U18-ch115, adc1

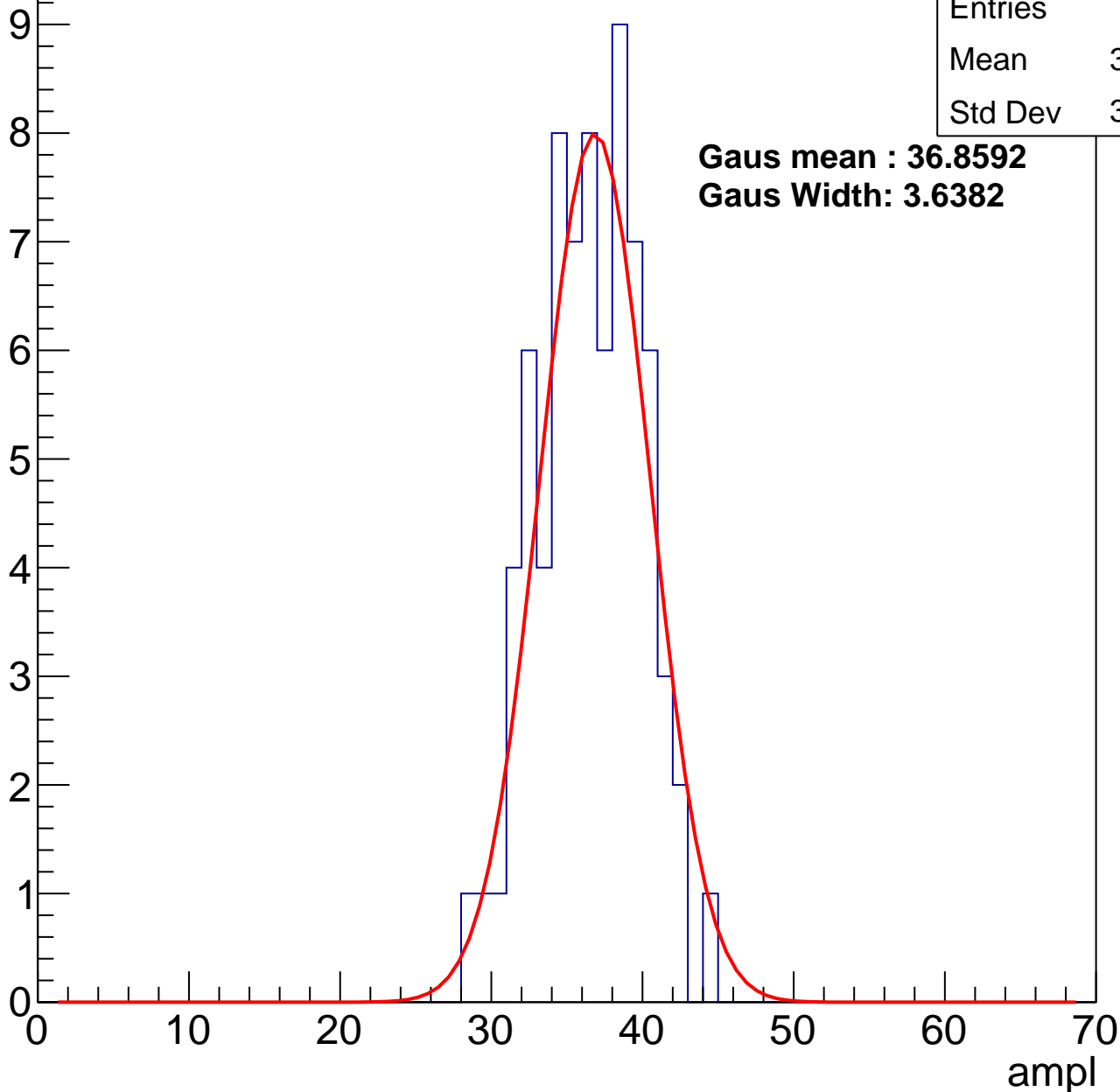
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	74
Mean	36.05
Std Dev	3.353

**Gaus mean : 36.8592**

**Gaus Width: 3.6382**



# B1L003S, U18-ch115, adc2

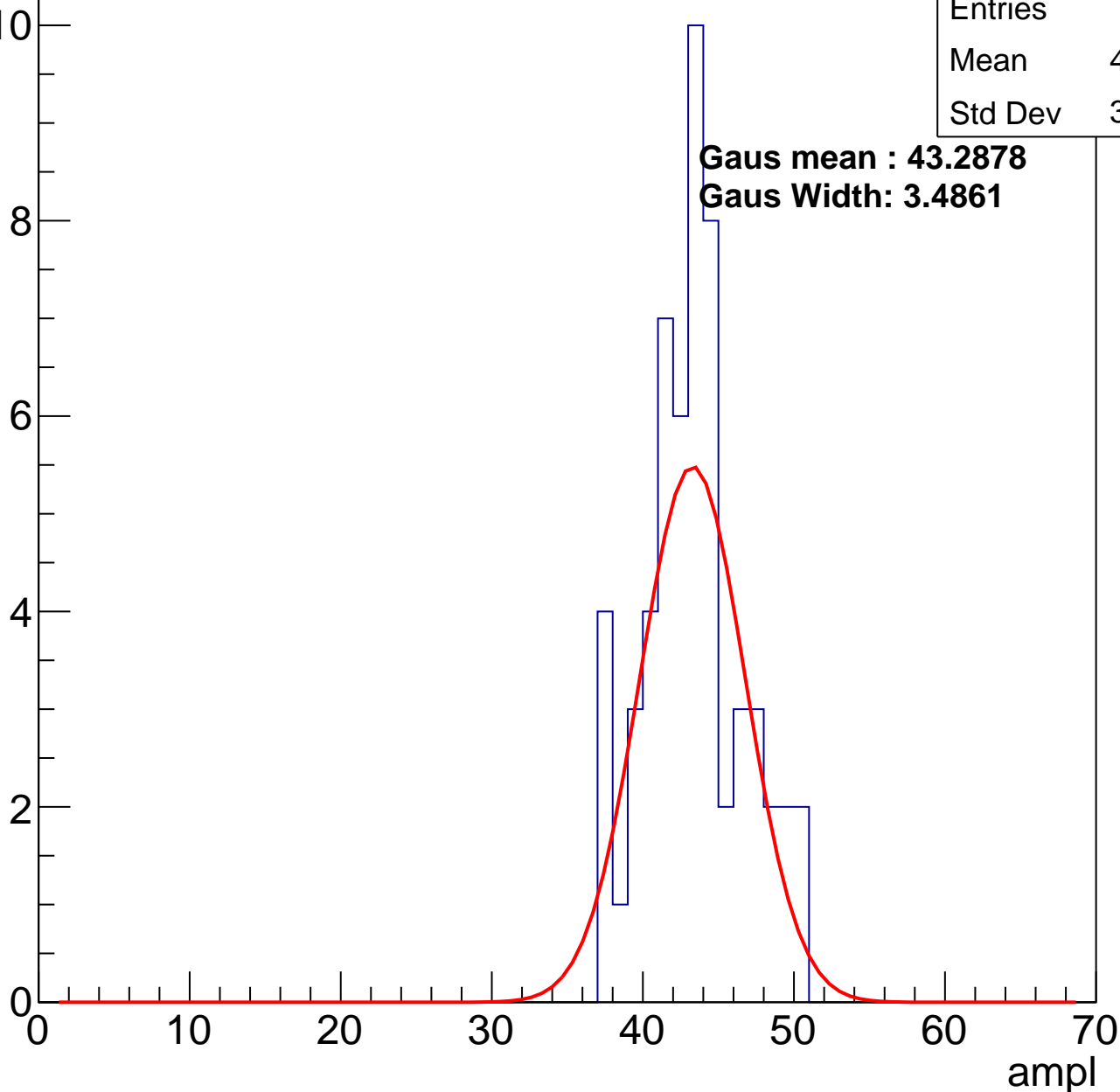
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	57
Mean	42.93
Std Dev	3.238

**Gaus mean : 43.2878**

**Gaus Width: 3.4861**

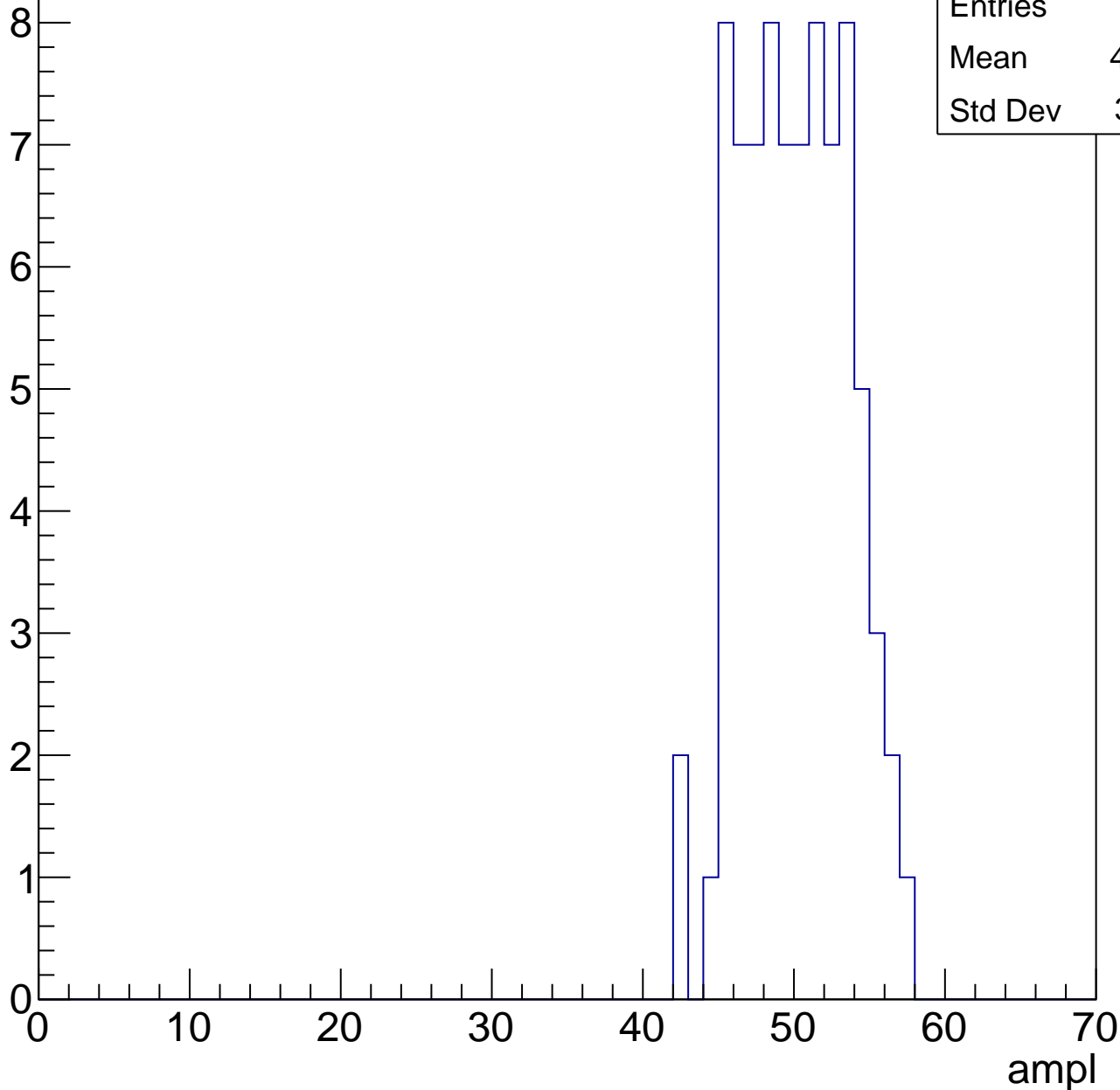


# B1L003S, U18-ch115, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

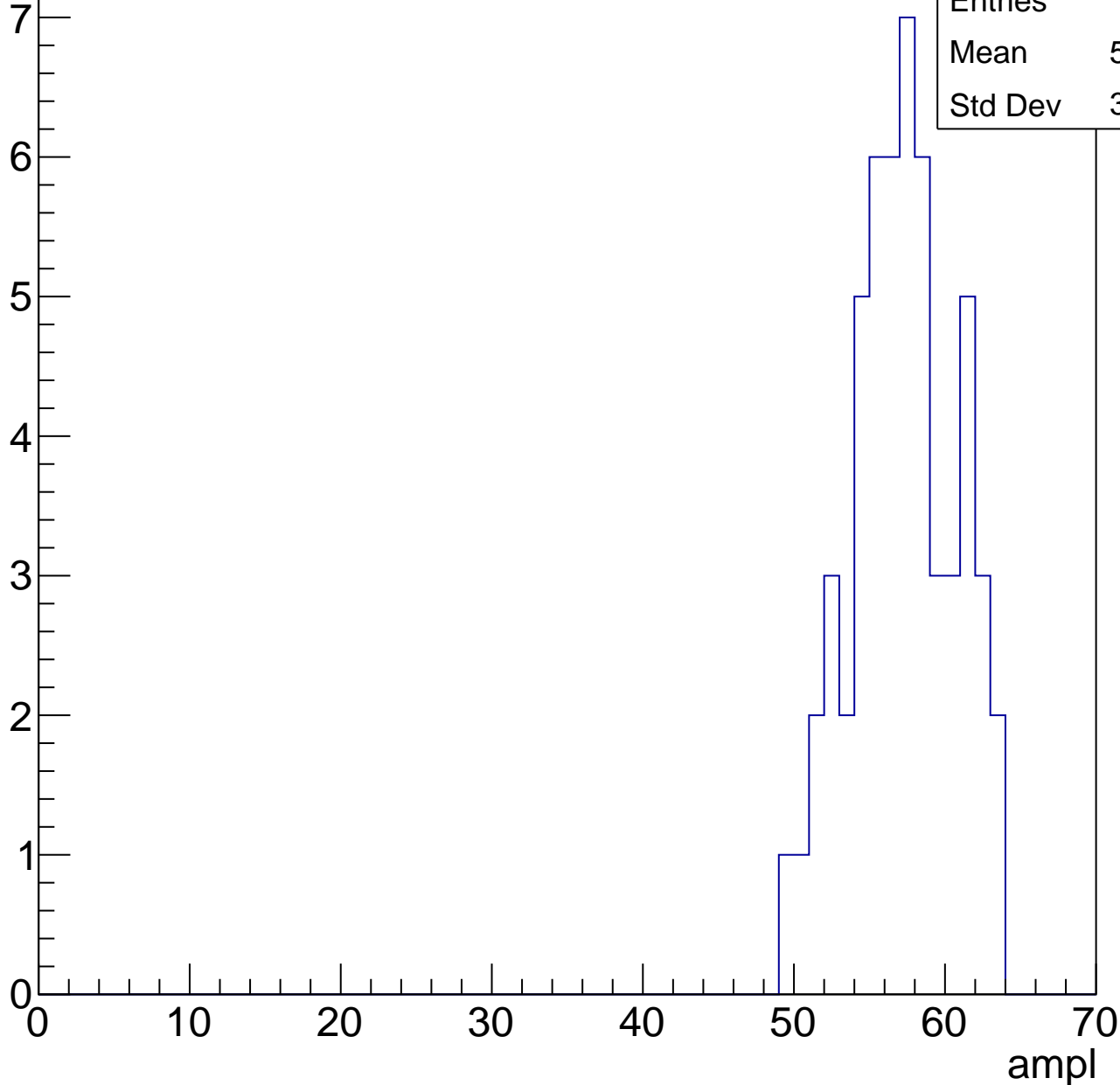
Entries	81
Mean	49.58
Std Dev	3.421



# B1L003S, U18-ch115, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

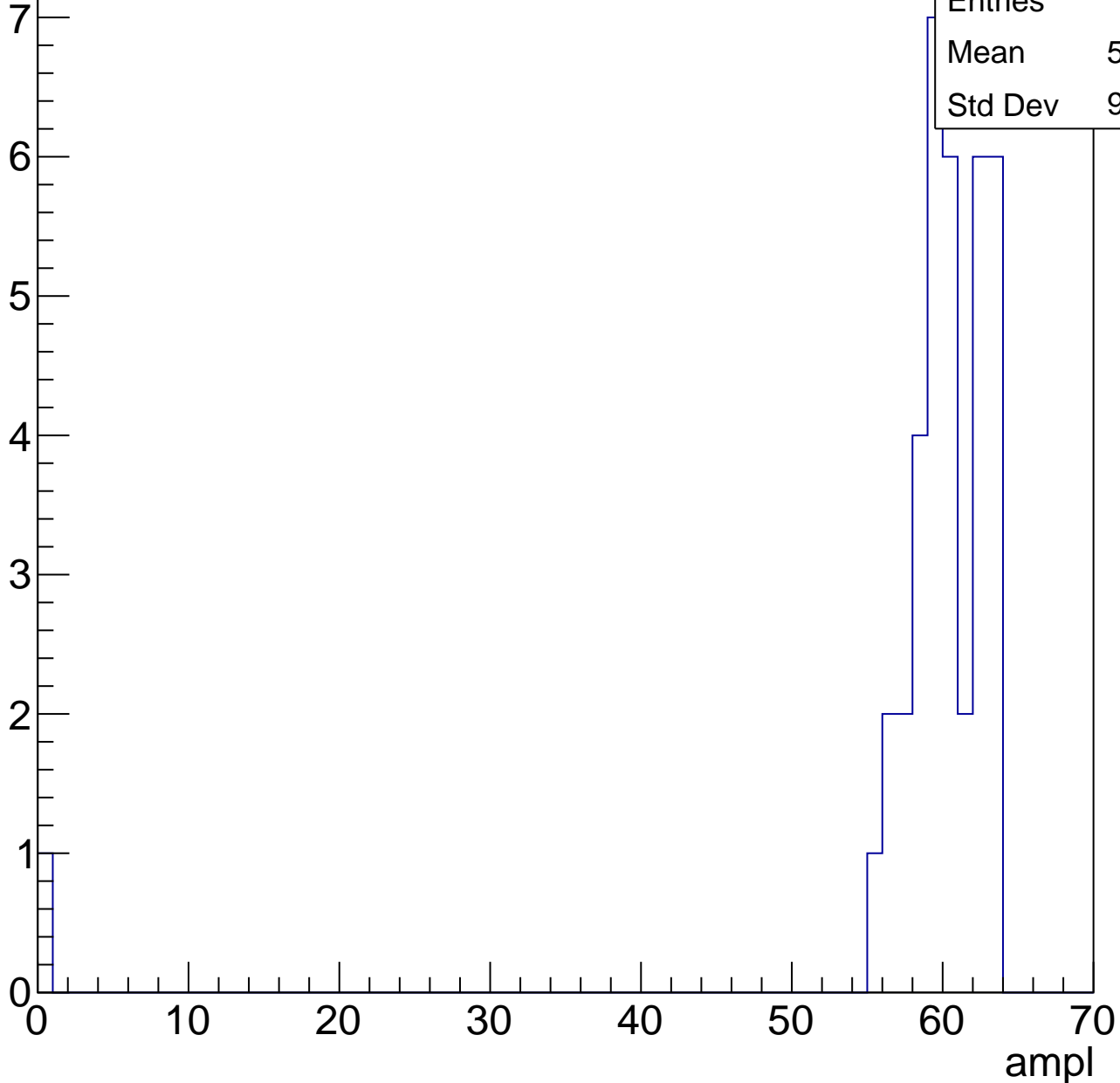


# B1L003S, U18-ch115, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

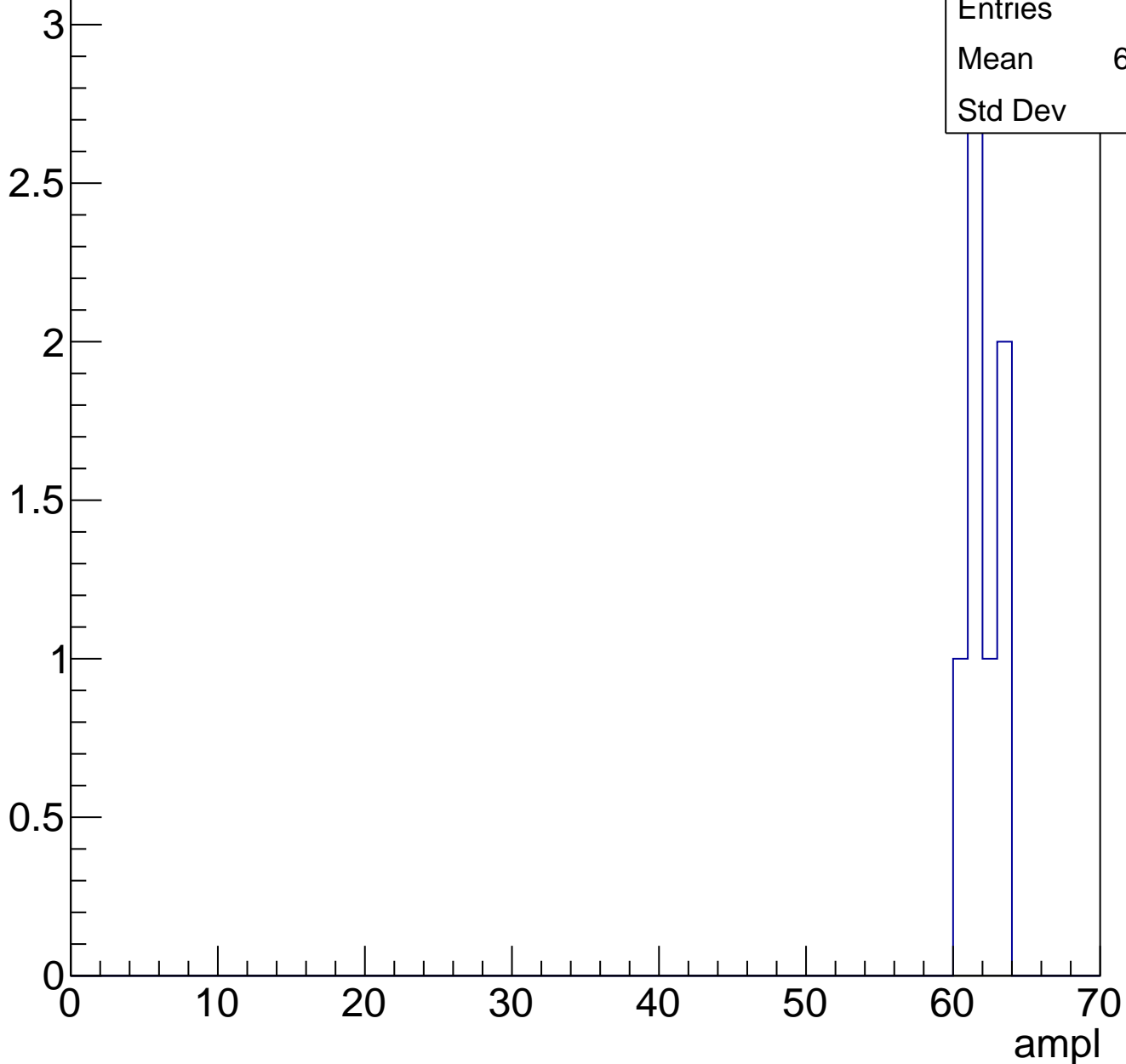
Entries	37
Mean	58.32
Std Dev	9.965



# B1L003S, U18-ch115, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U18-ch115, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch116, adc0

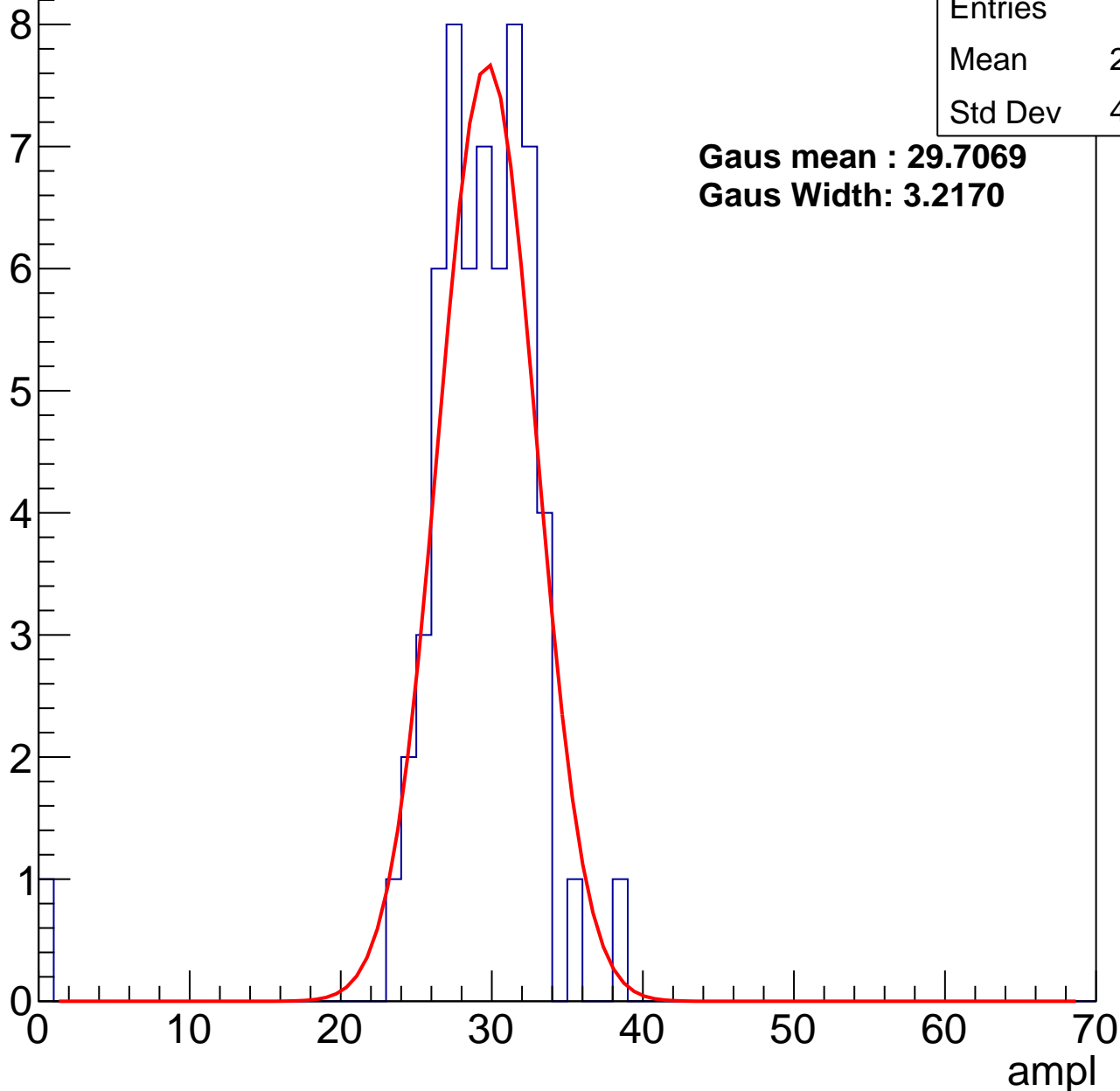
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	61
Mean	28.62
Std Dev	4.687

**Gaus mean : 29.7069**

**Gaus Width: 3.2170**



# B1L003S, U18-ch116, adc1

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	76
Mean	36.29
Std Dev	3.448

**Gaus mean : 36.6432**

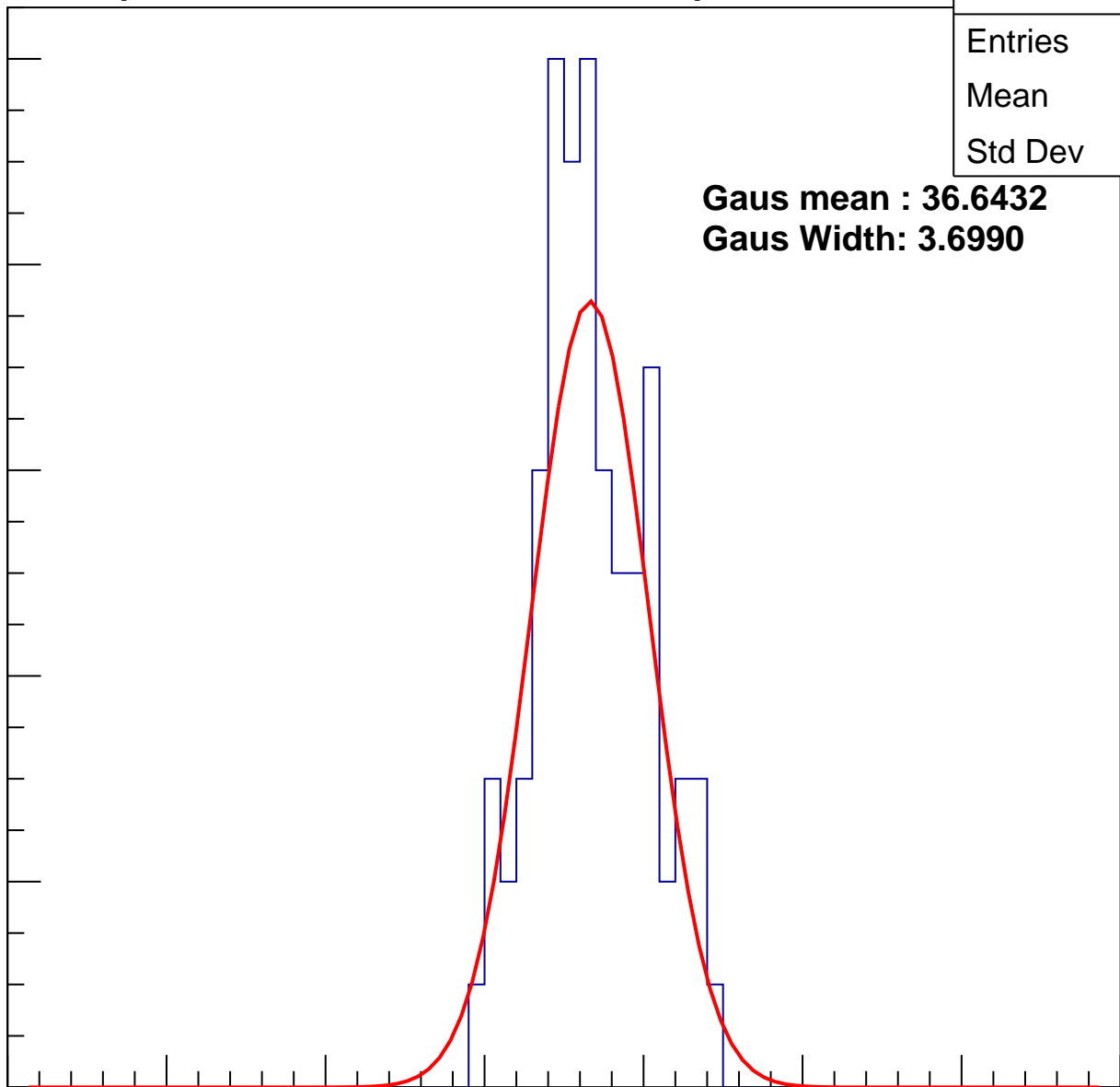
**Gaus Width: 3.6990**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L003S, U18-ch116, adc2

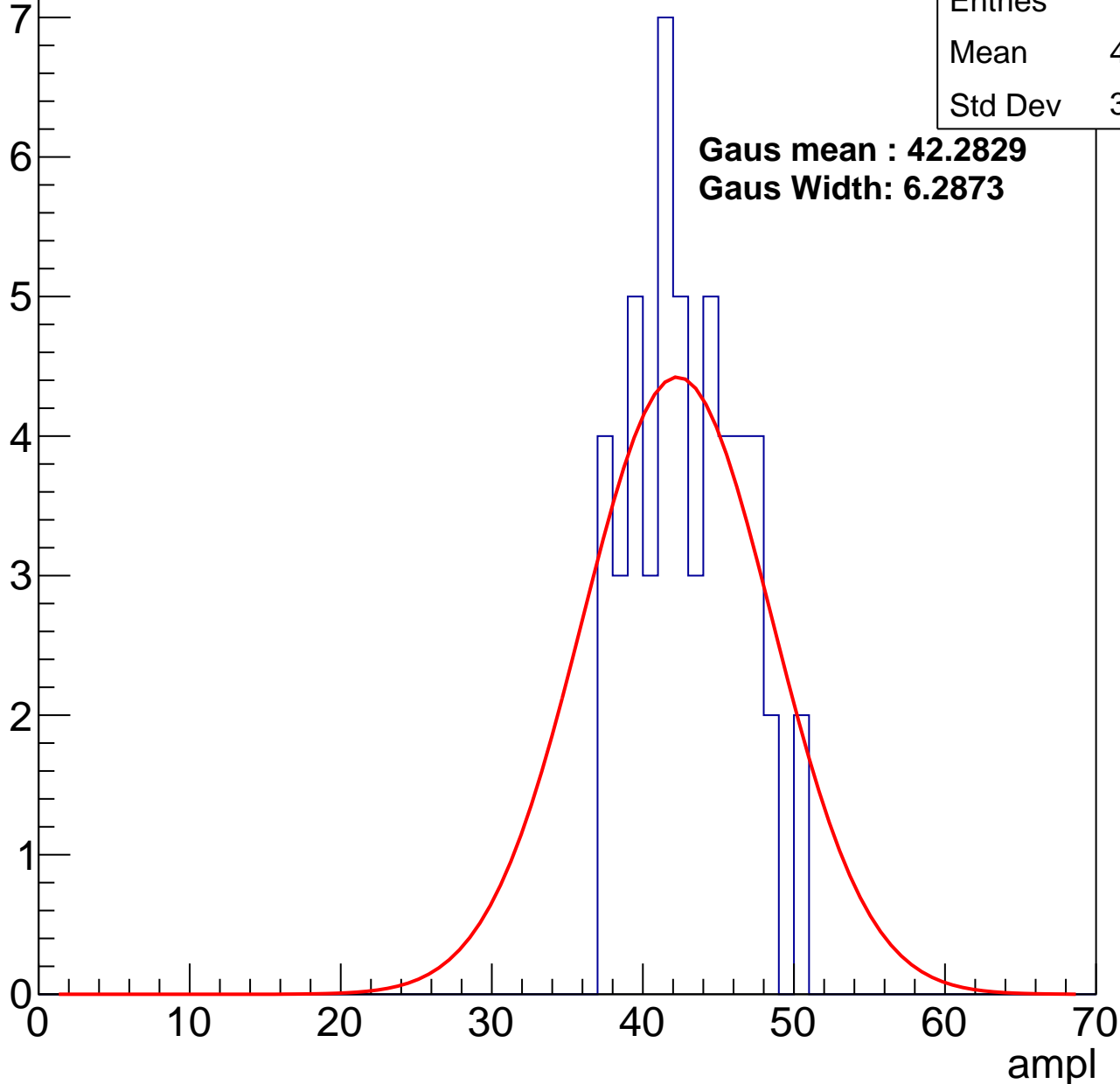
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	51
Mean	42.57
Std Dev	3.482

**Gaus mean : 42.2829**

**Gaus Width: 6.2873**

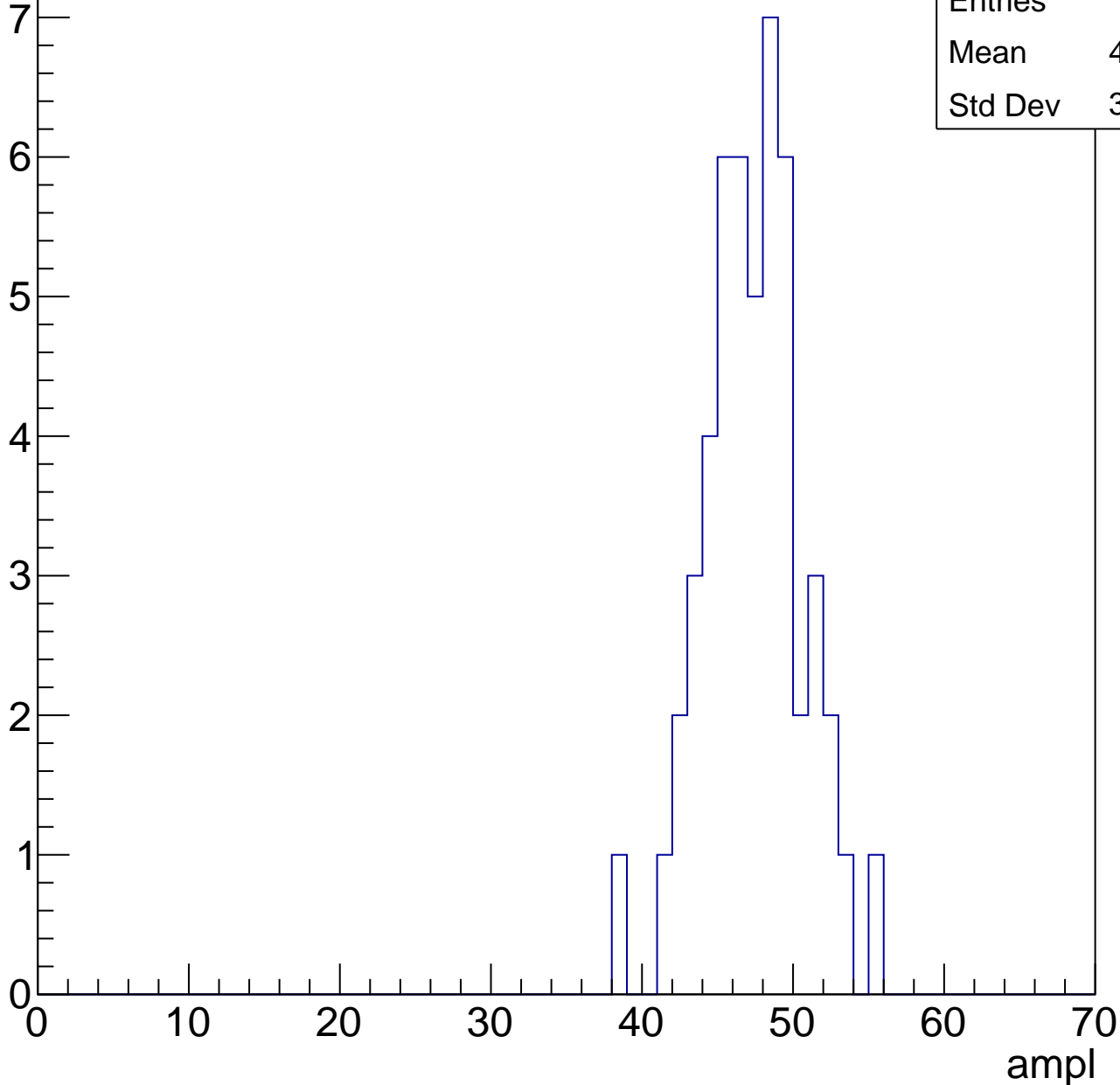


# B1L003S, U18-ch116, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	50
Mean	46.88
Std Dev	3.247

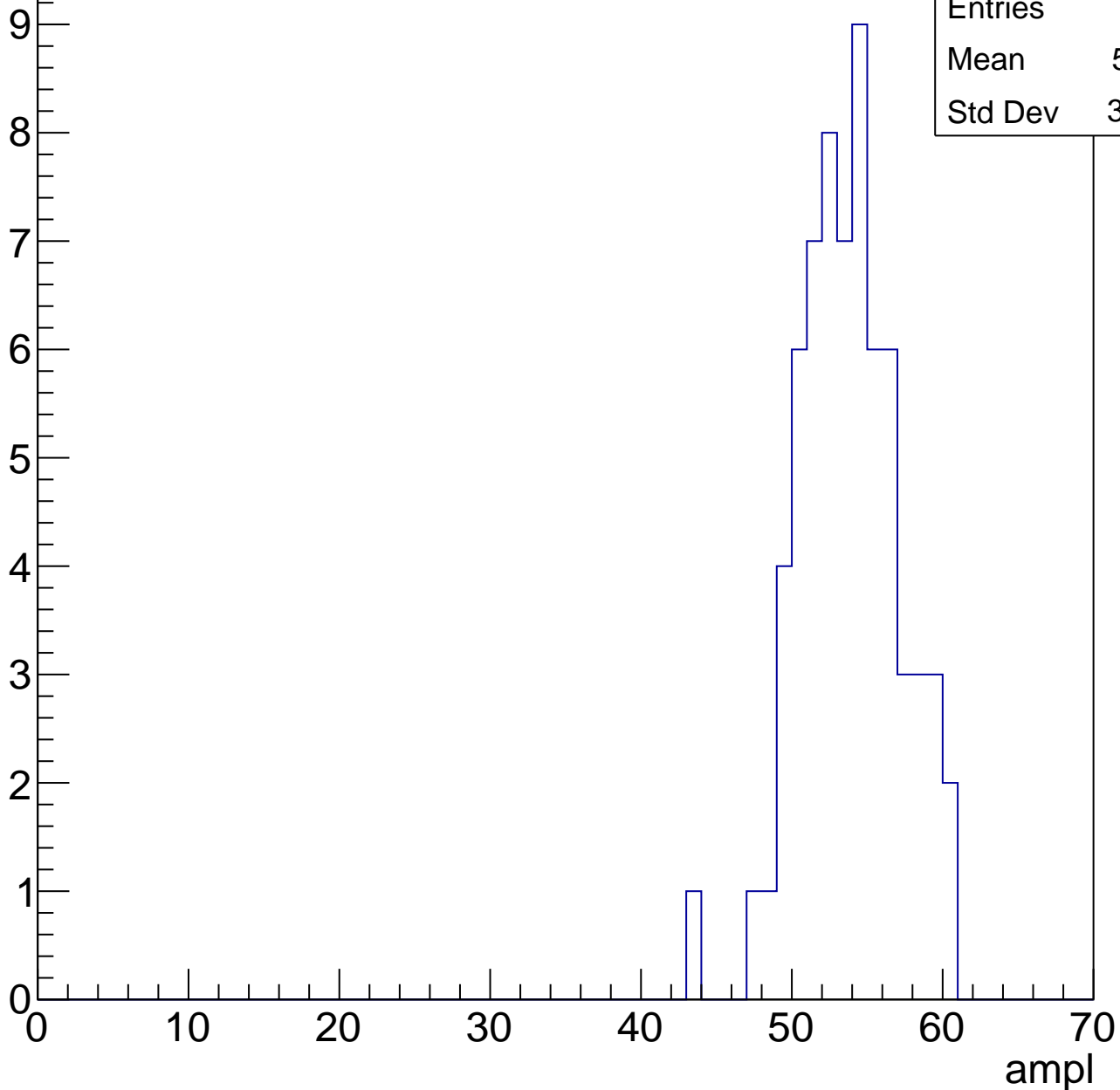


# B1L003S, U18-ch116, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

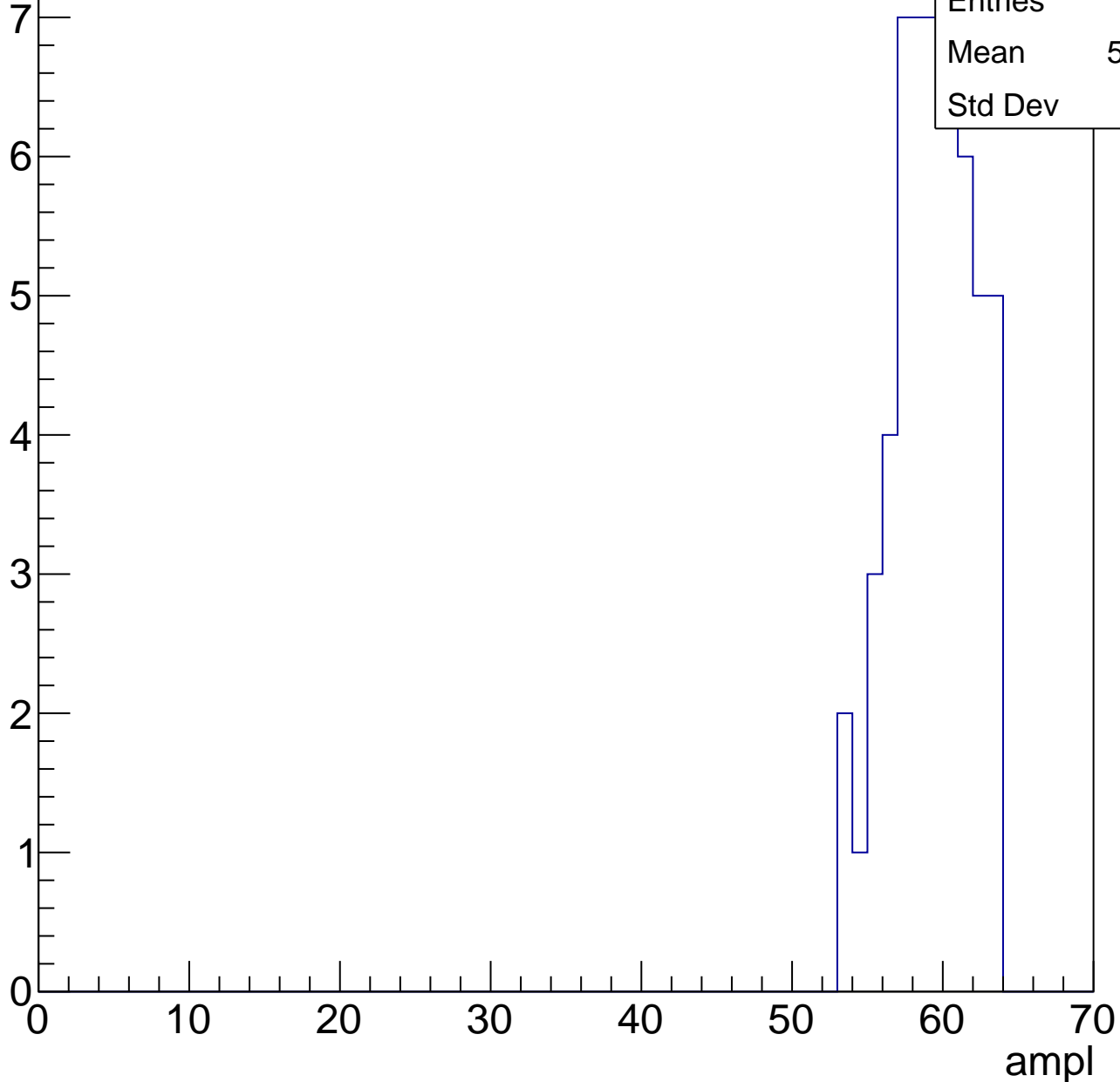
Entries	67
Mean	53.31
Std Dev	3.288



# B1L003S, U18-ch116, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

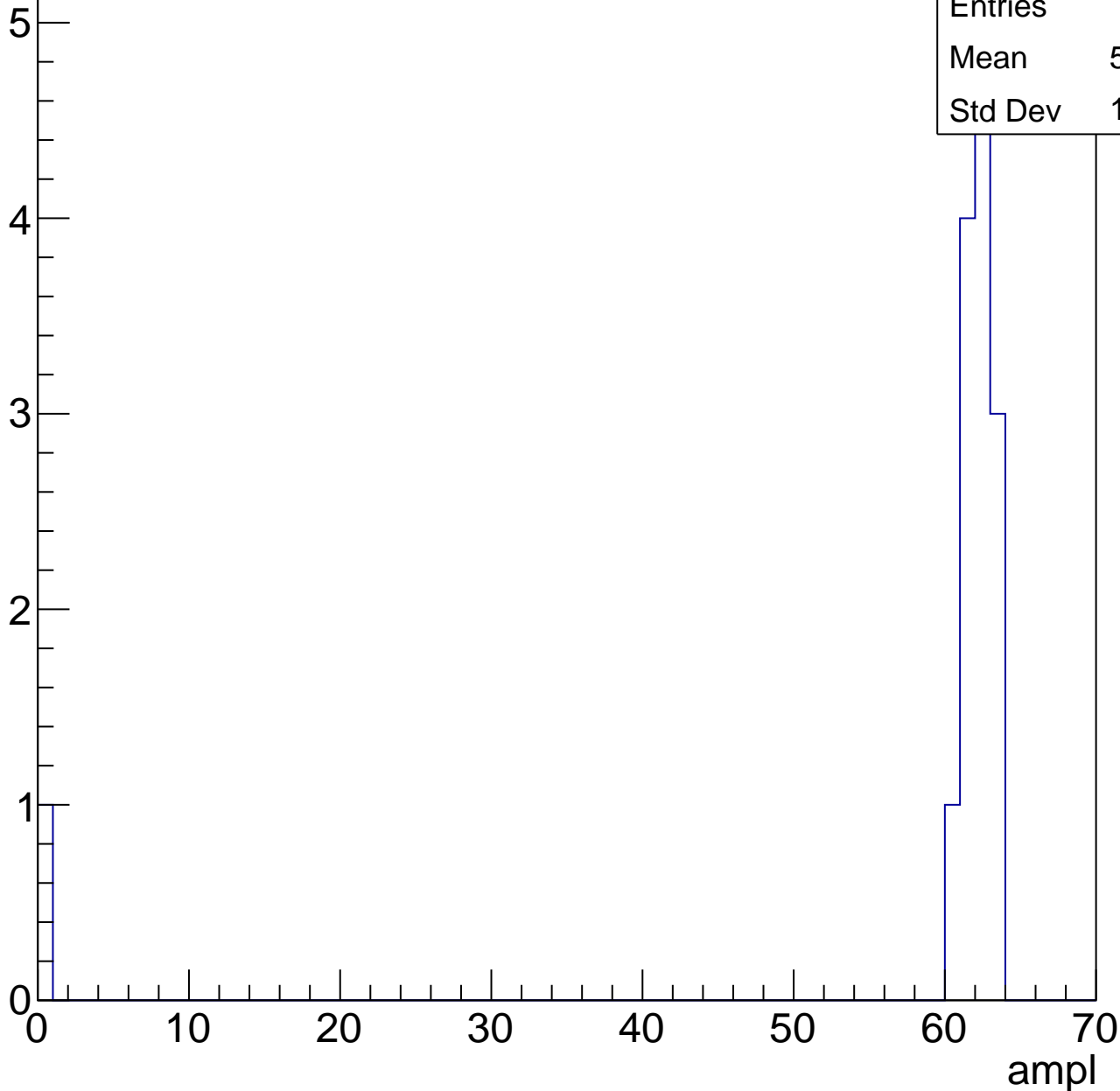


# B1L003S, U18-ch116, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	14
Mean	57.36
Std Dev	15.93

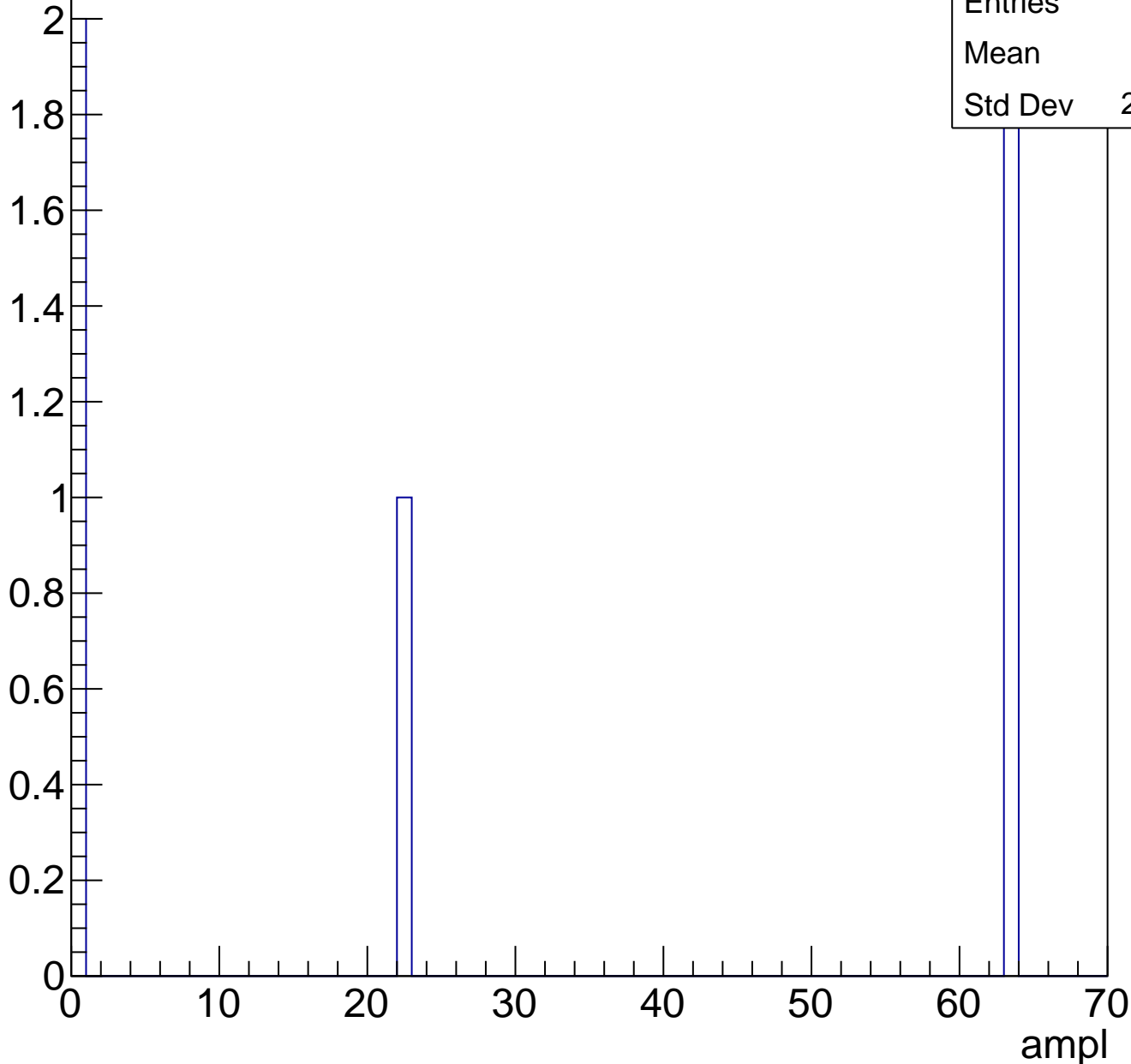




# B1L003S, U18-ch116, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U18-ch117, adc0

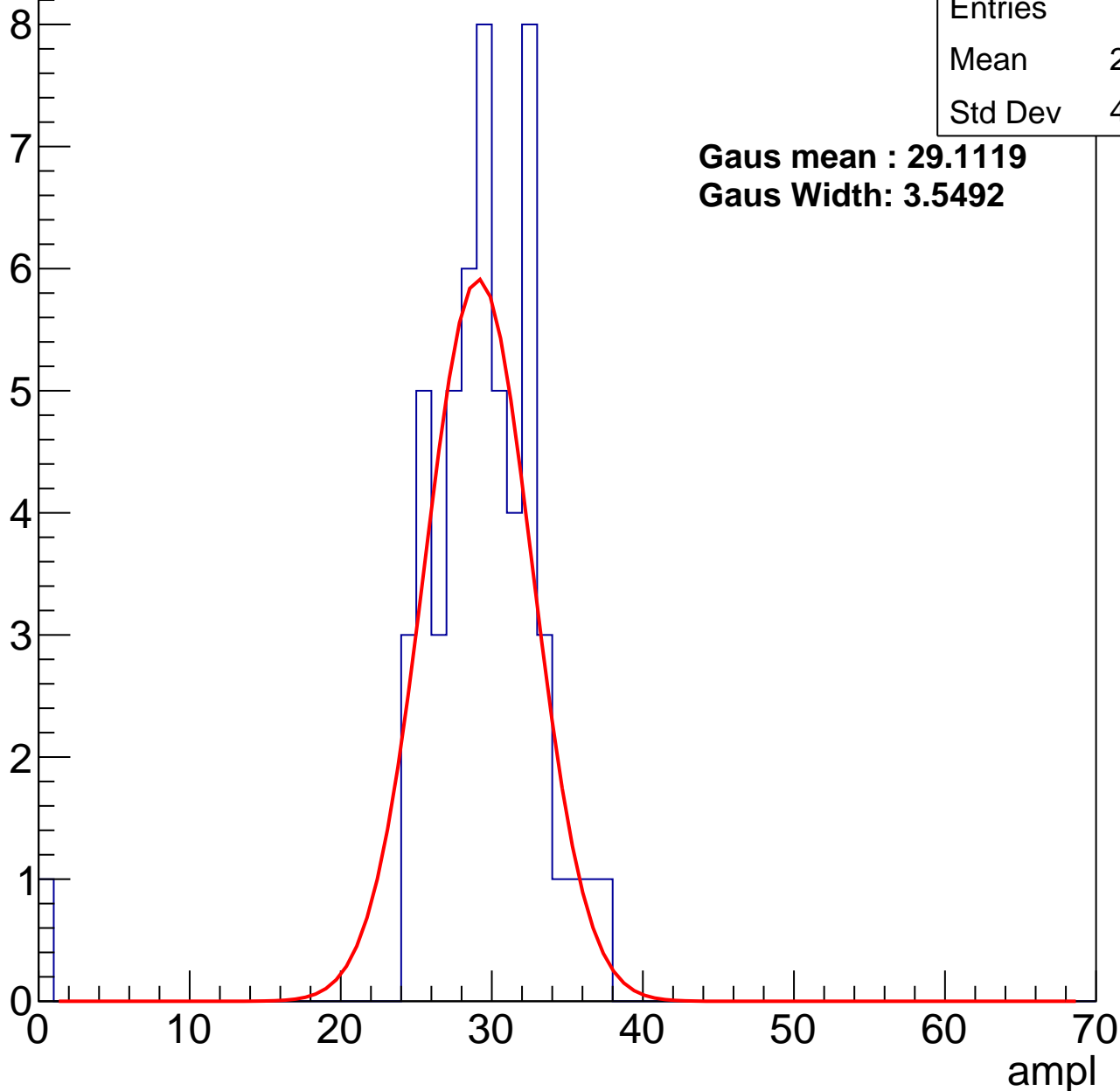
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	55
Mean	28.75
Std Dev	4.973

**Gaus mean : 29.1119**

**Gaus Width: 3.5492**



# B1L003S, U18-ch117, adc1

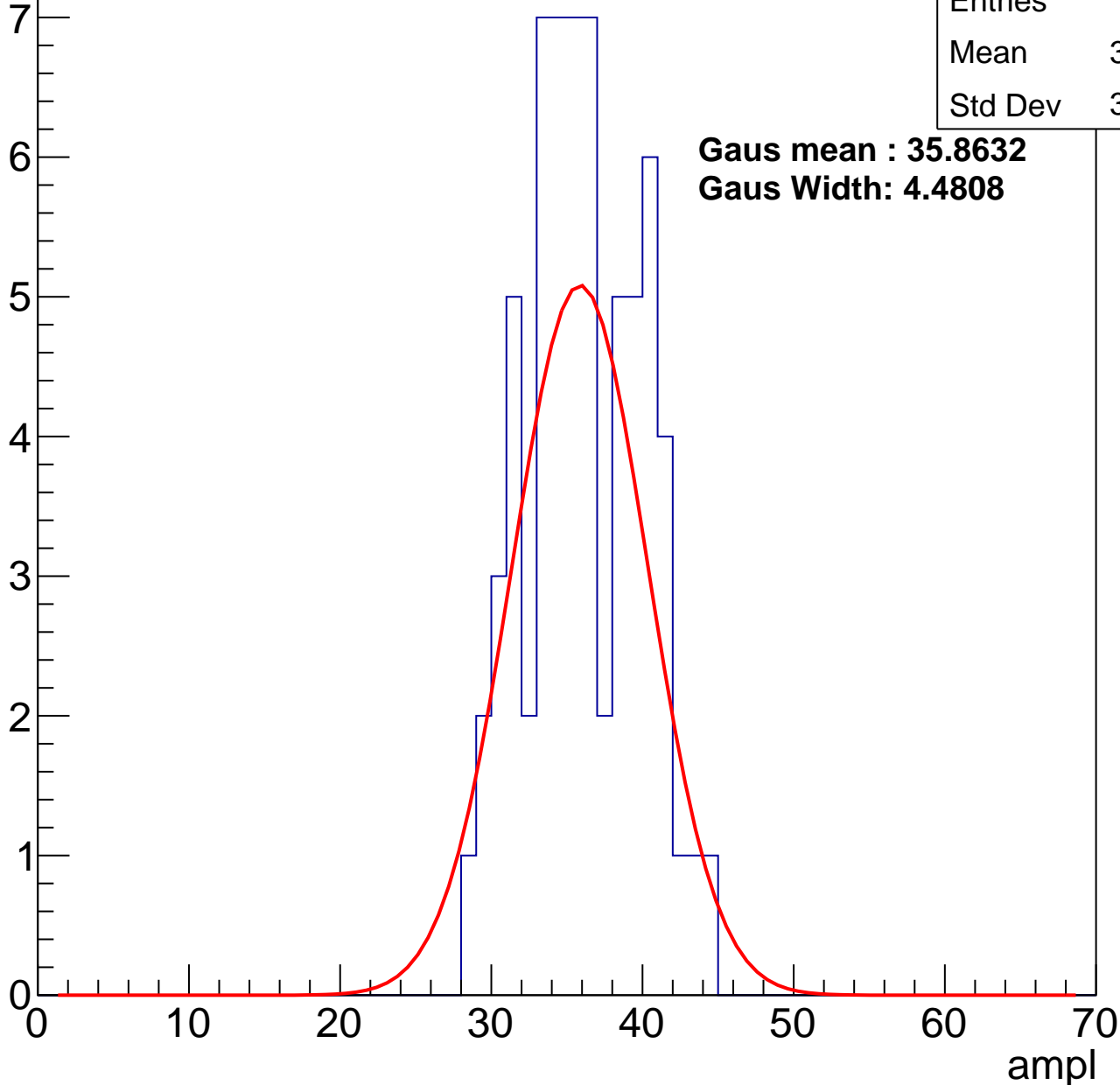
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	66
Mean	35.65
Std Dev	3.752

**Gaus mean : 35.8632**

**Gaus Width: 4.4808**



# B1L003S, U18-ch117, adc2

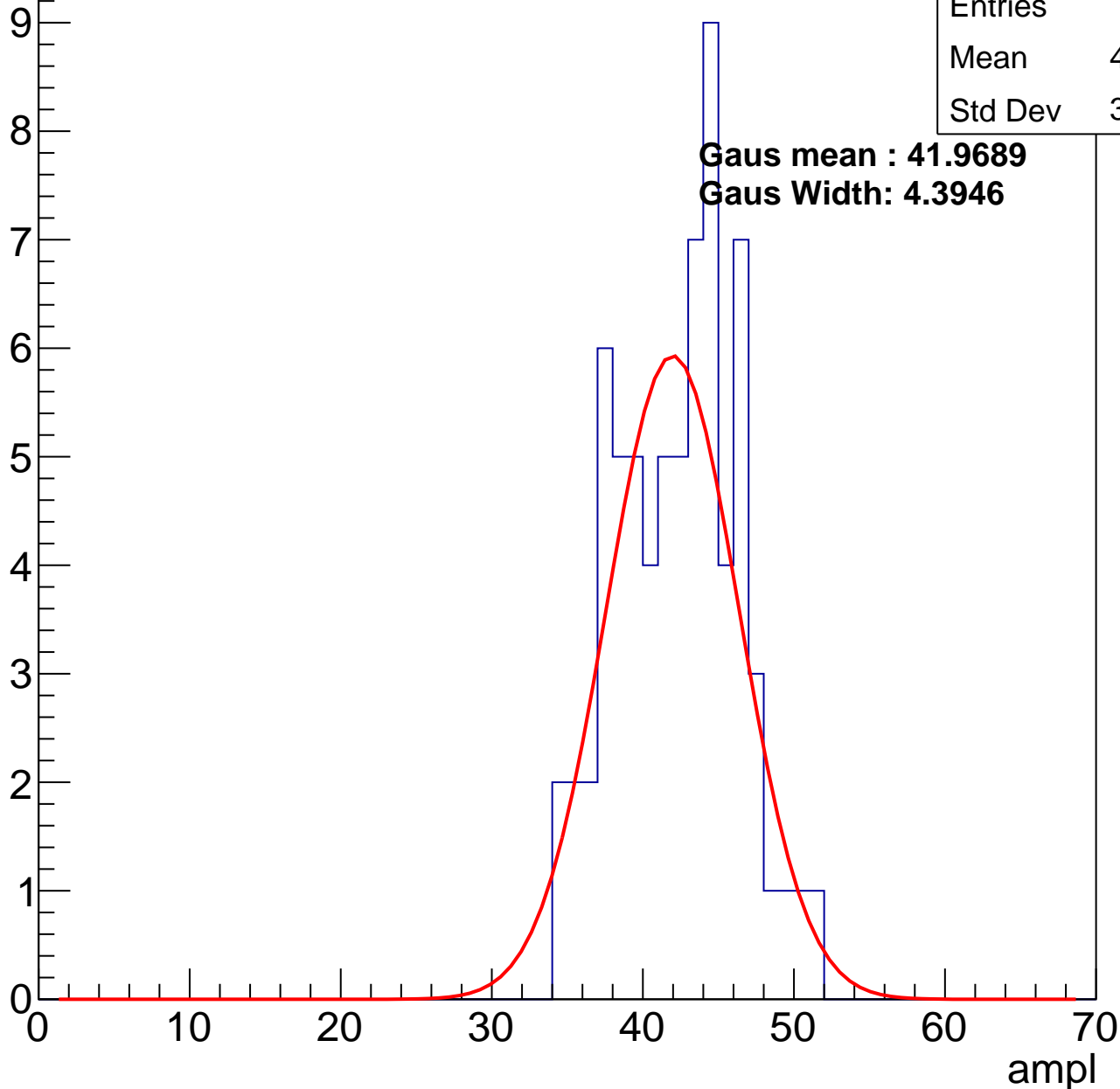
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	70
Mean	41.86
Std Dev	3.943

**Gaus mean : 41.9689**

**Gaus Width: 4.3946**

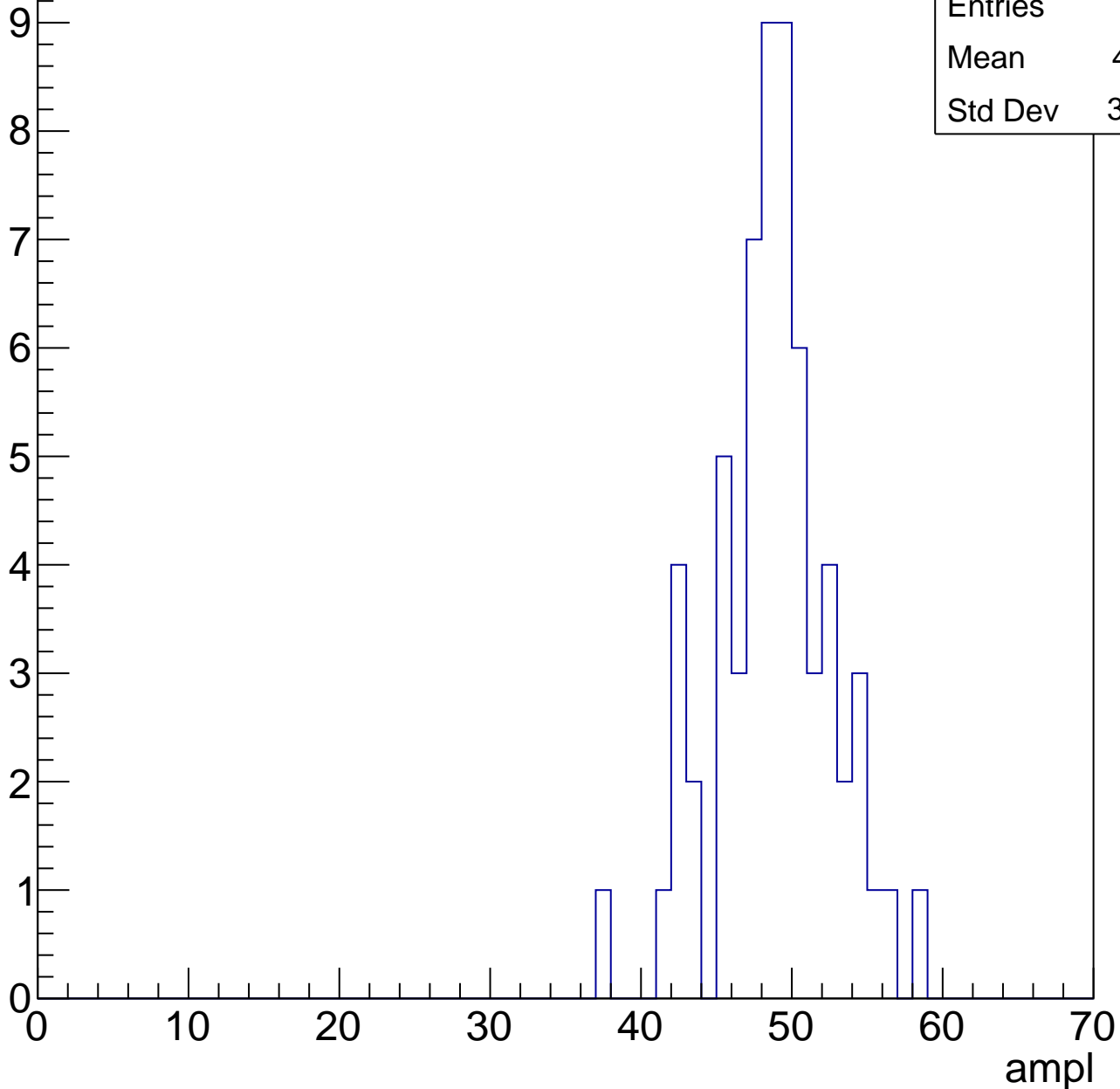


# B1L003S, U18-ch117, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	62
Mean	48.31
Std Dev	3.846

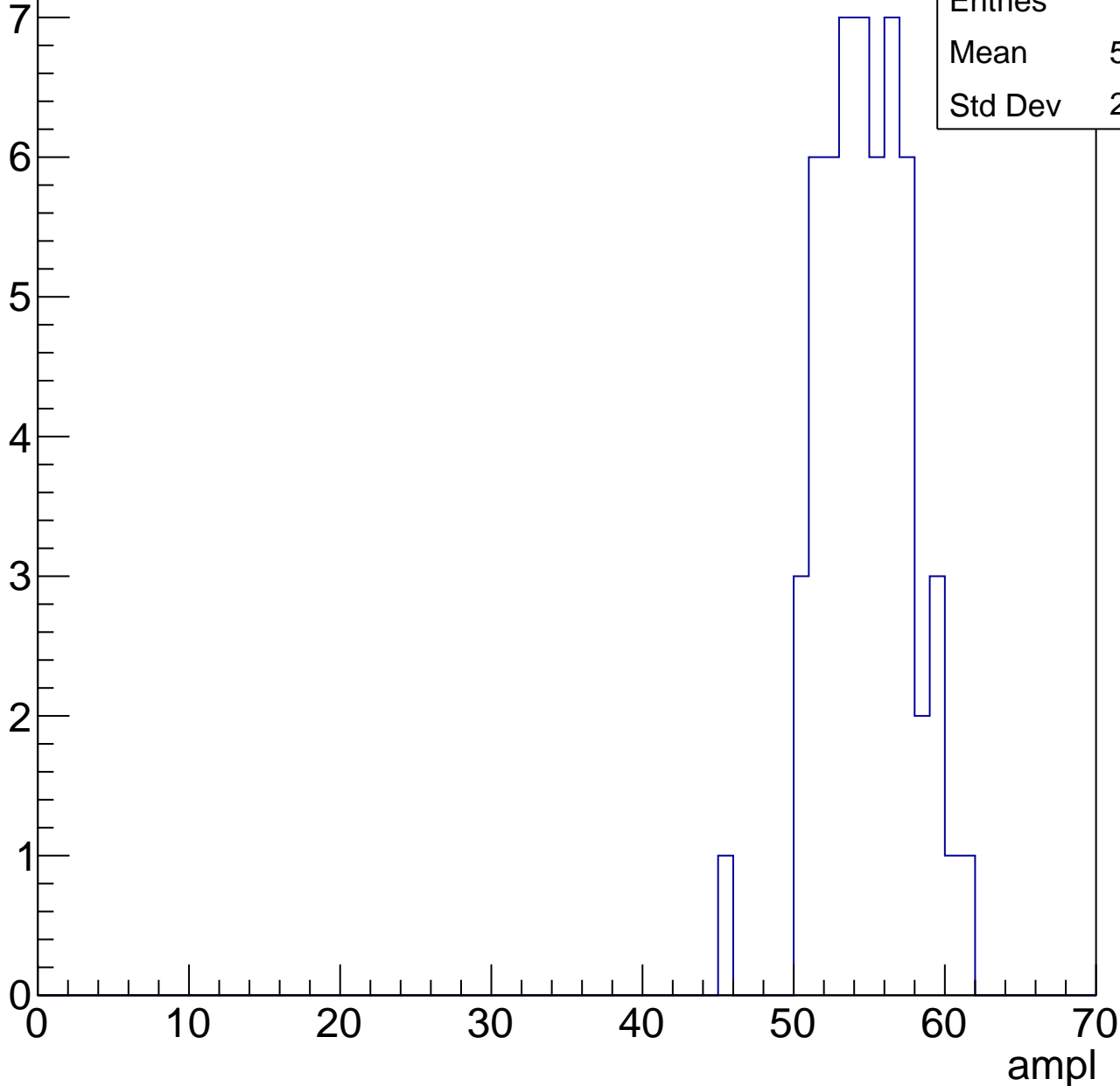


# B1L003S, U18-ch117, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	56
Mean	54.29
Std Dev	2.956

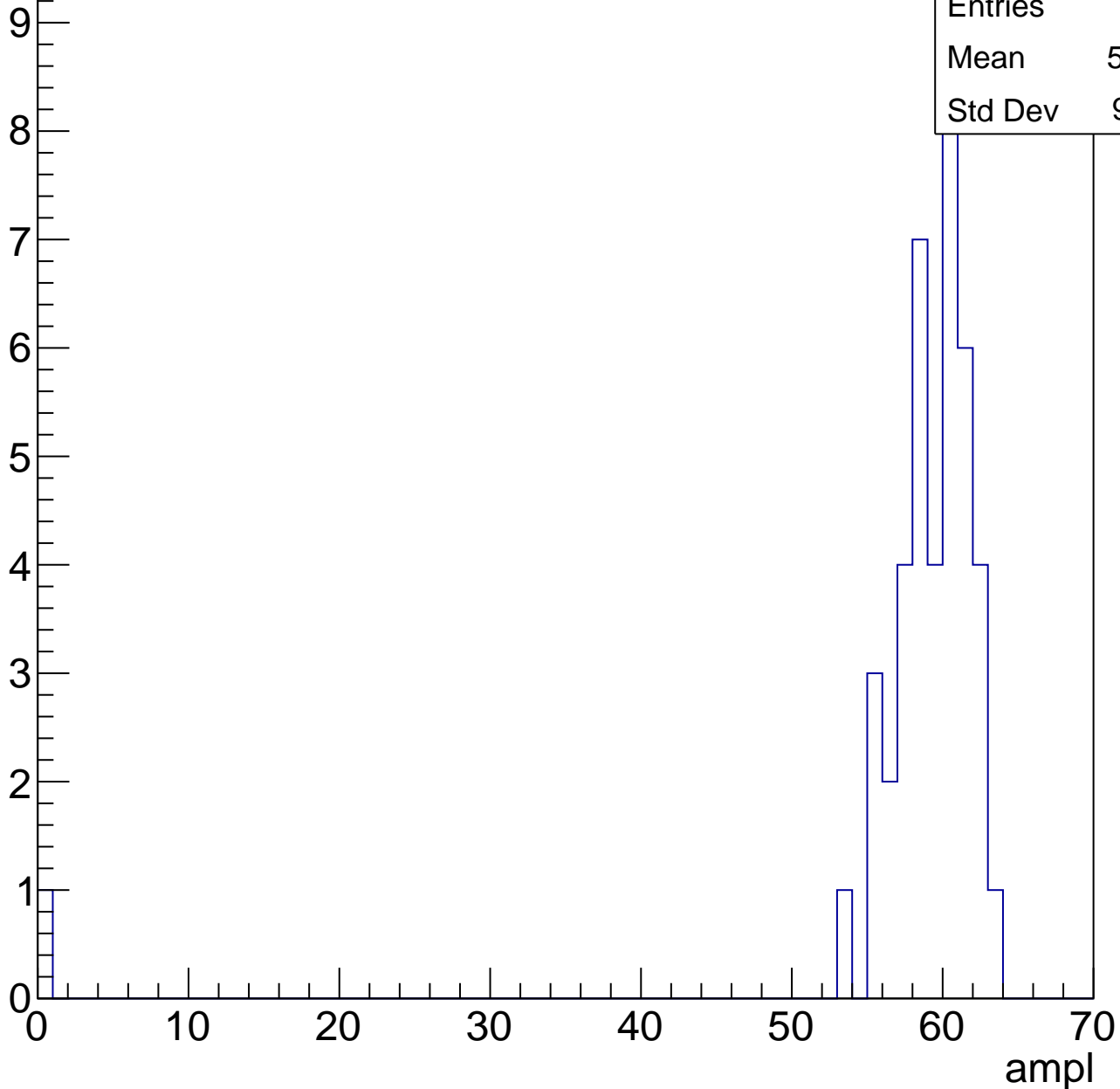


# B1L003S, U18-ch117, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	42
Mean	57.55
Std Dev	9.261

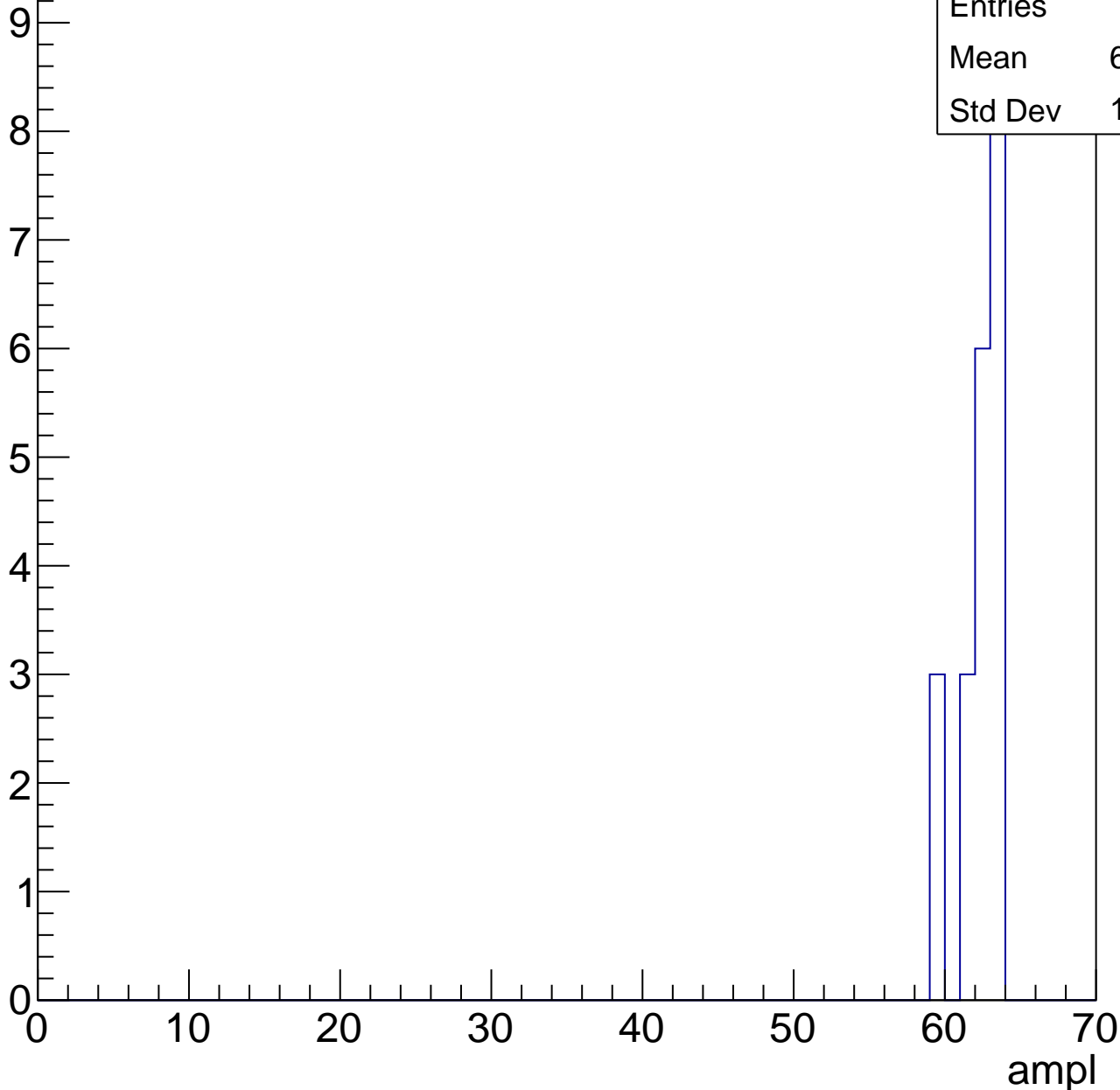


# B1L003S, U18-ch117, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	21
Mean	61.86
Std Dev	1.355





# B1L003S, U18-ch117, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch118, adc0

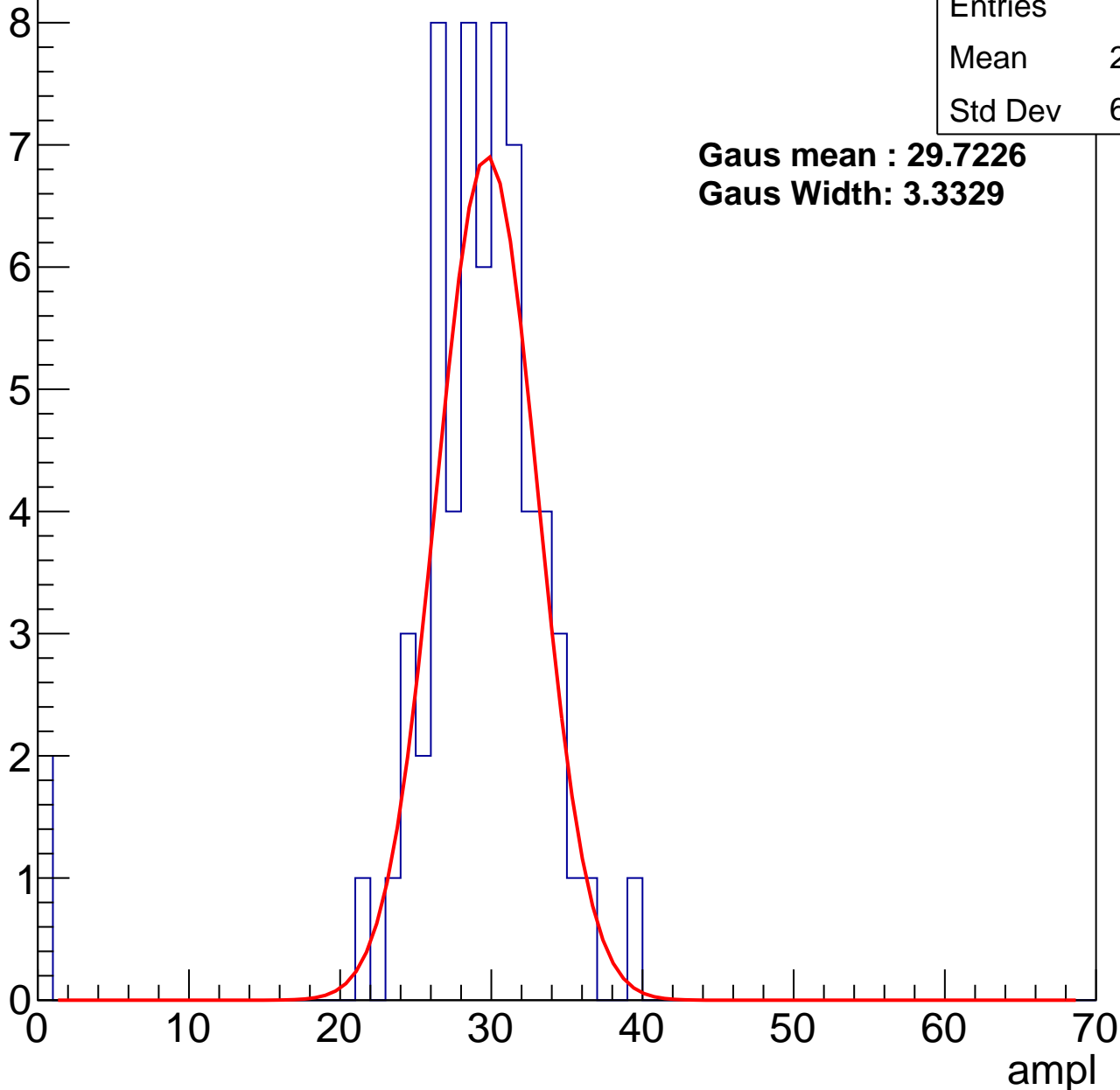
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	64
Mean	28.27
Std Dev	6.055

**Gaus mean : 29.7226**

**Gaus Width: 3.3329**



# B1L003S, U18-ch118, adc1

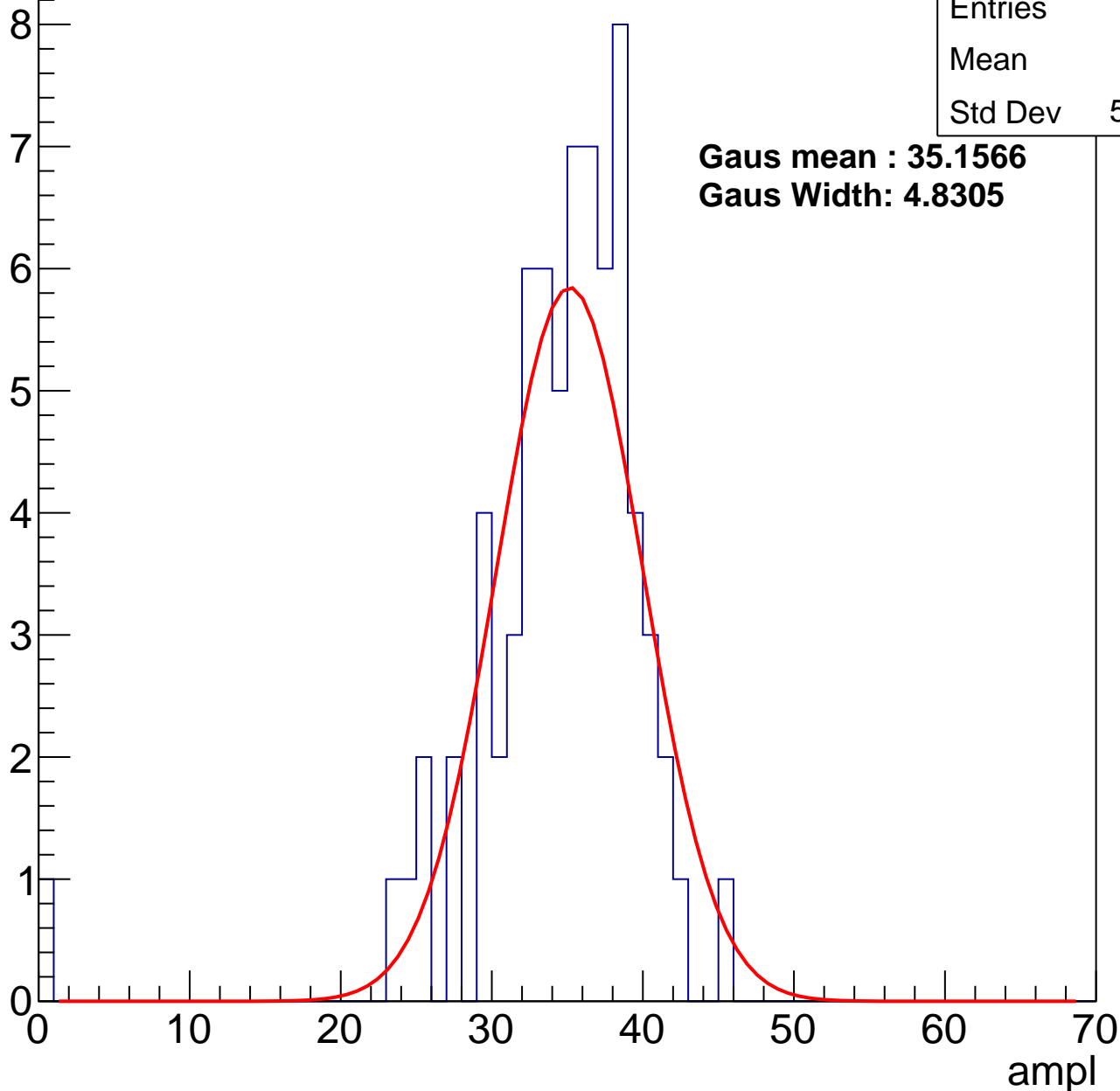
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	72
Mean	34
Std Dev	5.932

**Gaus mean : 35.1566**

**Gaus Width: 4.8305**



# B1L003S, U18-ch118, adc2

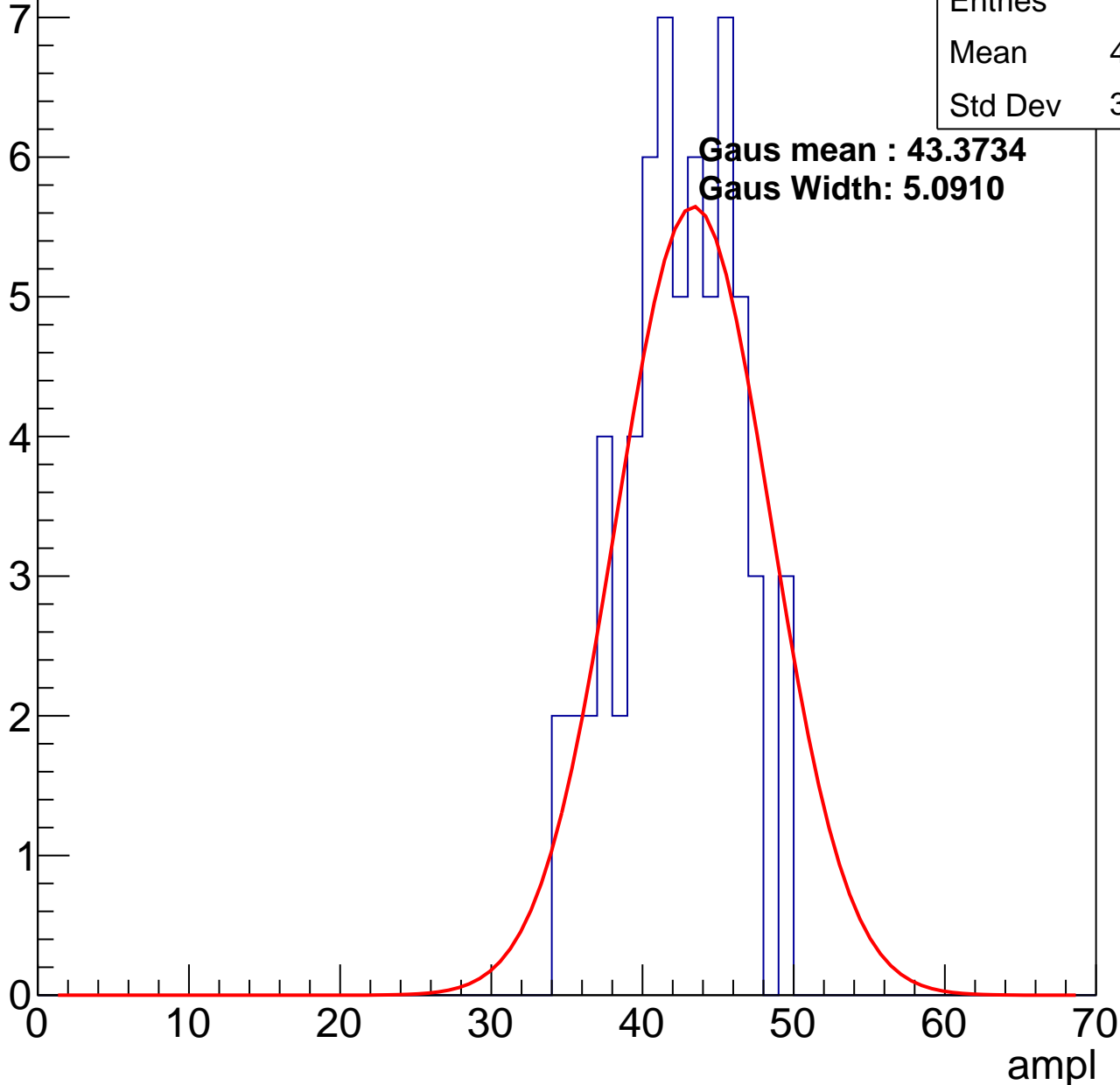
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	63
Mean	41.87
Std Dev	3.752

**Gaus mean : 43.3734**

**Gaus Width: 5.0910**

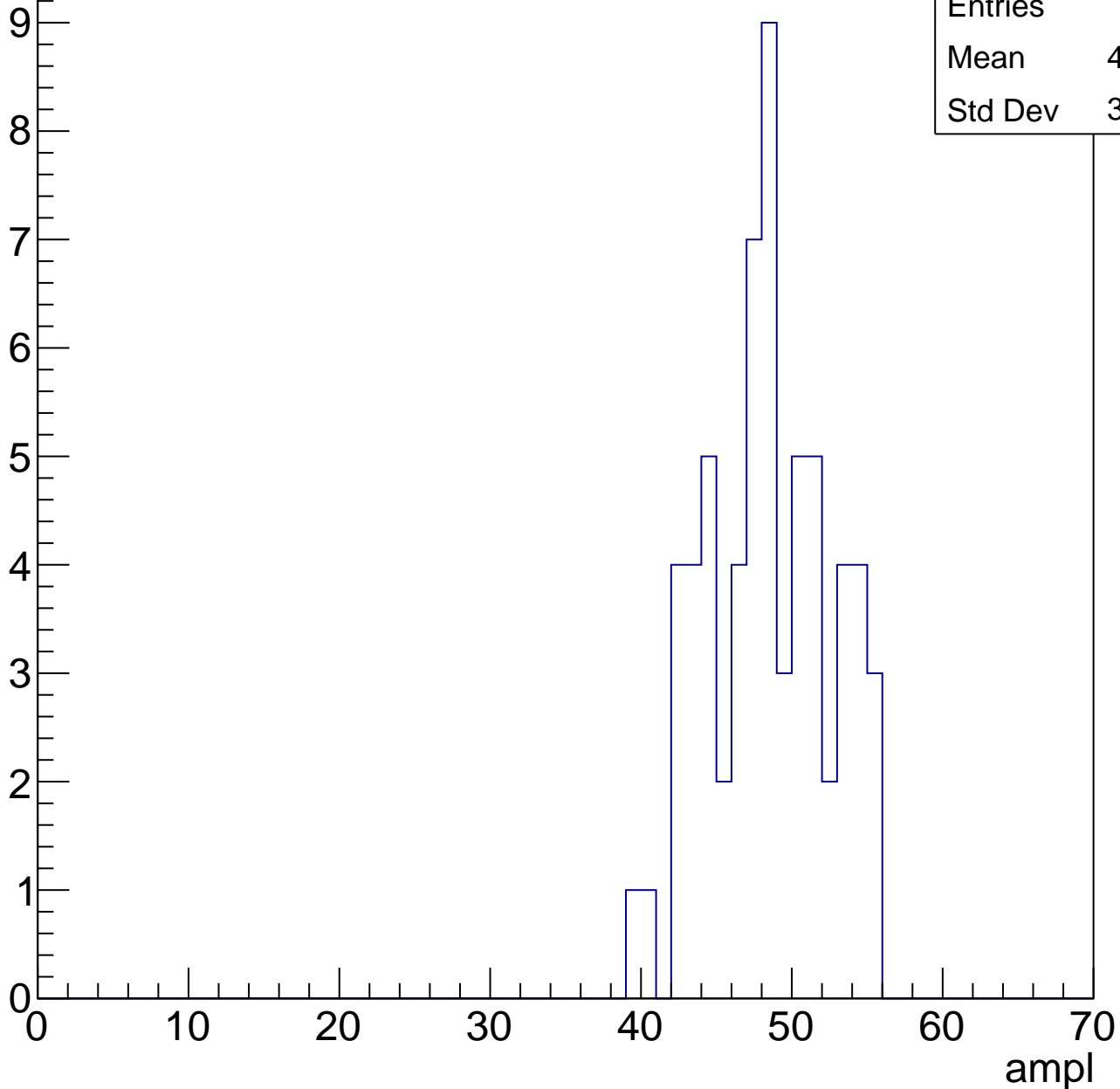


# B1L003S, U18-ch118, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	63
Mean	47.98
Std Dev	3.986

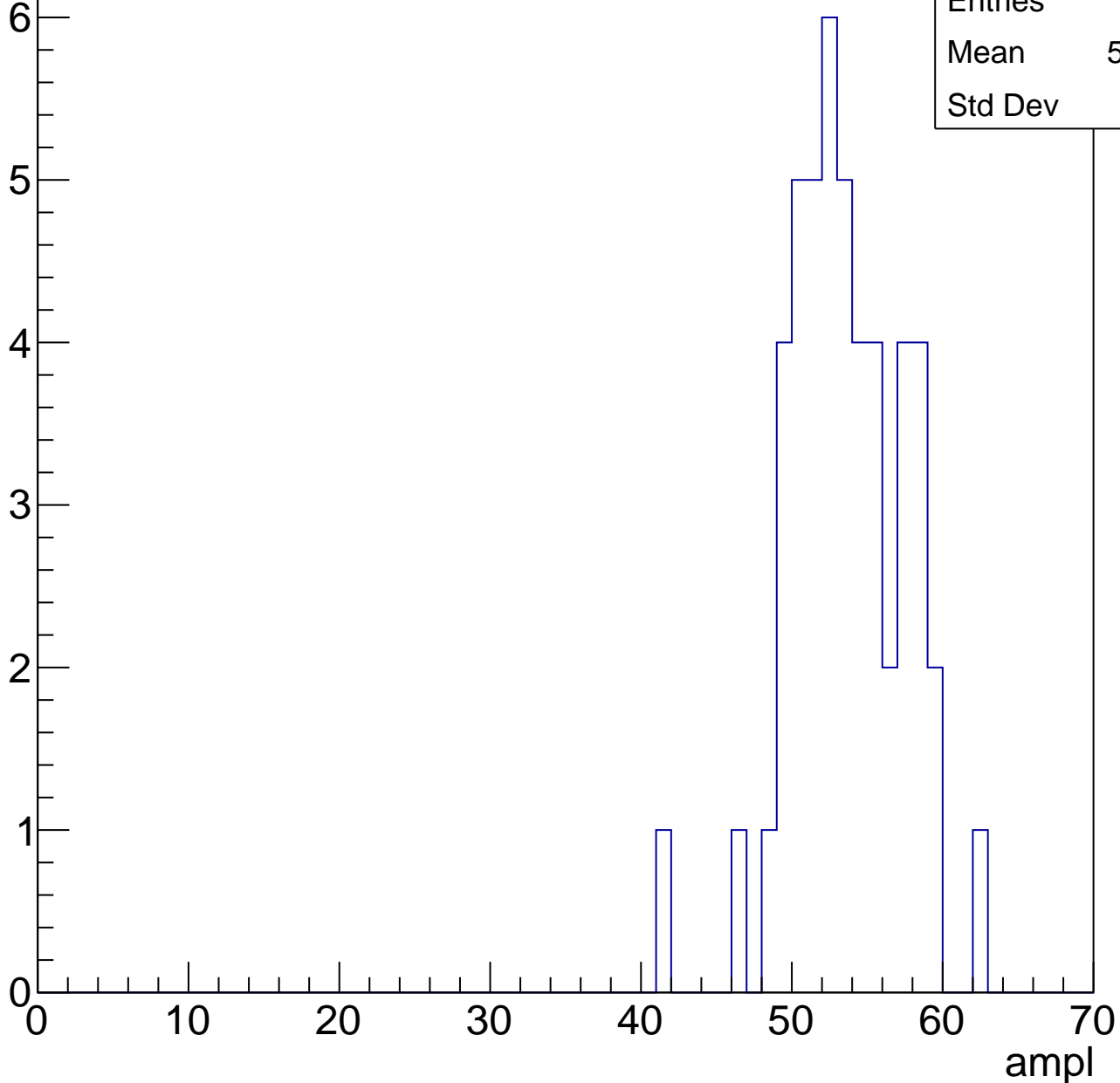


# B1L003S, U18-ch118, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	49
Mean	53.08
Std Dev	3.8

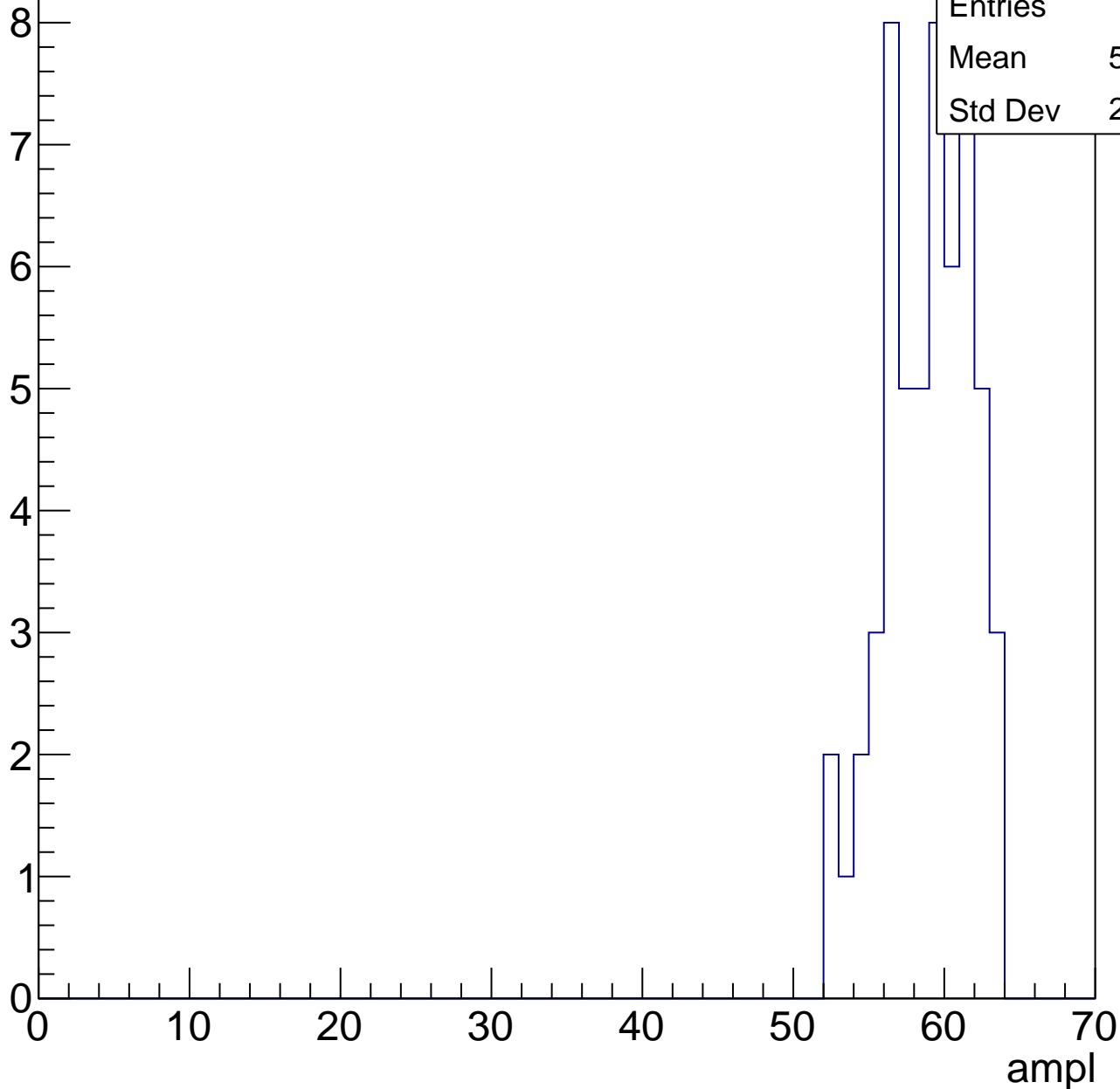


# B1L003S, U18-ch118, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	56
Mean	58.43
Std Dev	2.809

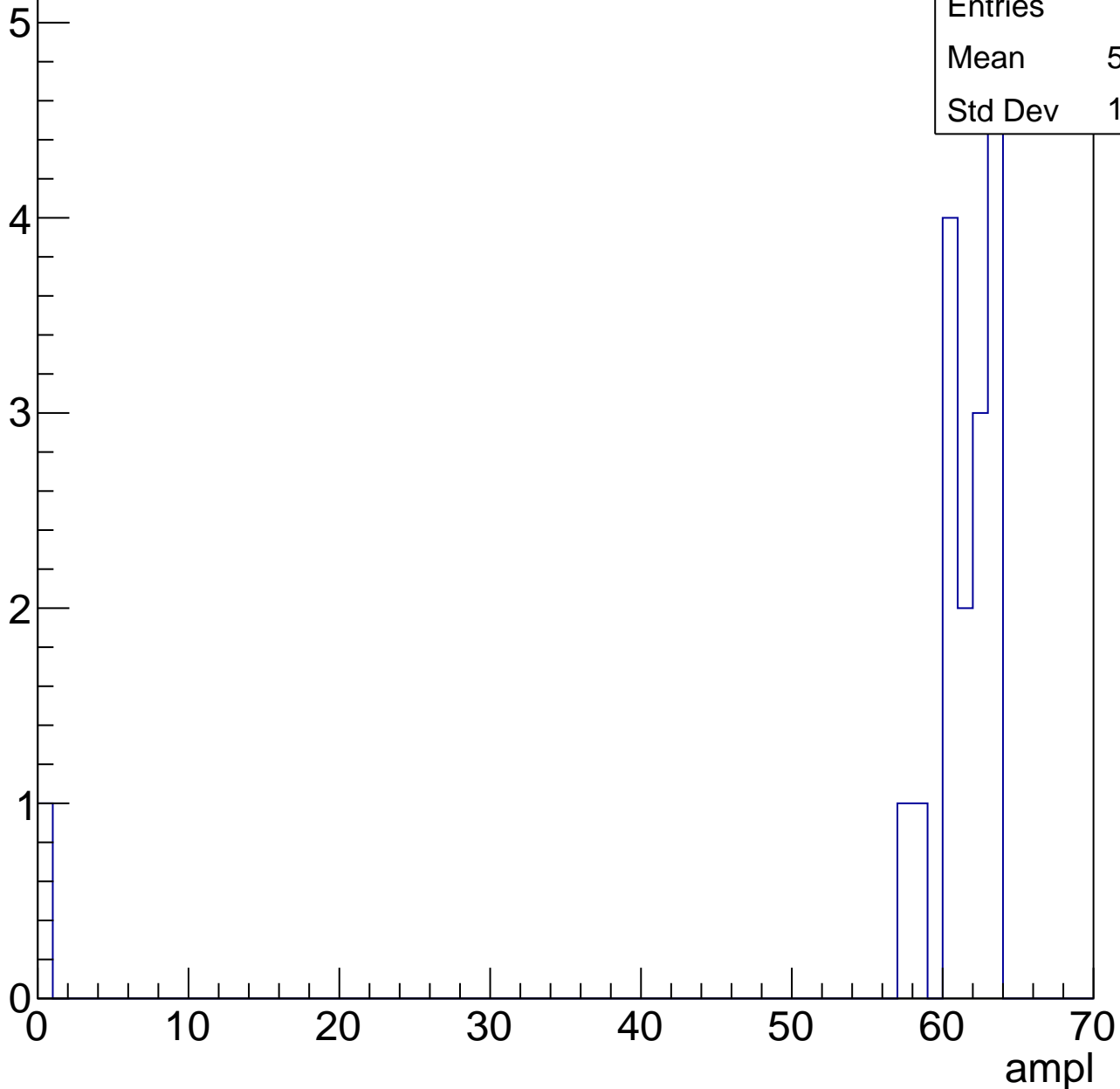


# B1L003S, U18-ch118, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	17
Mean	57.53
Std Dev	14.49

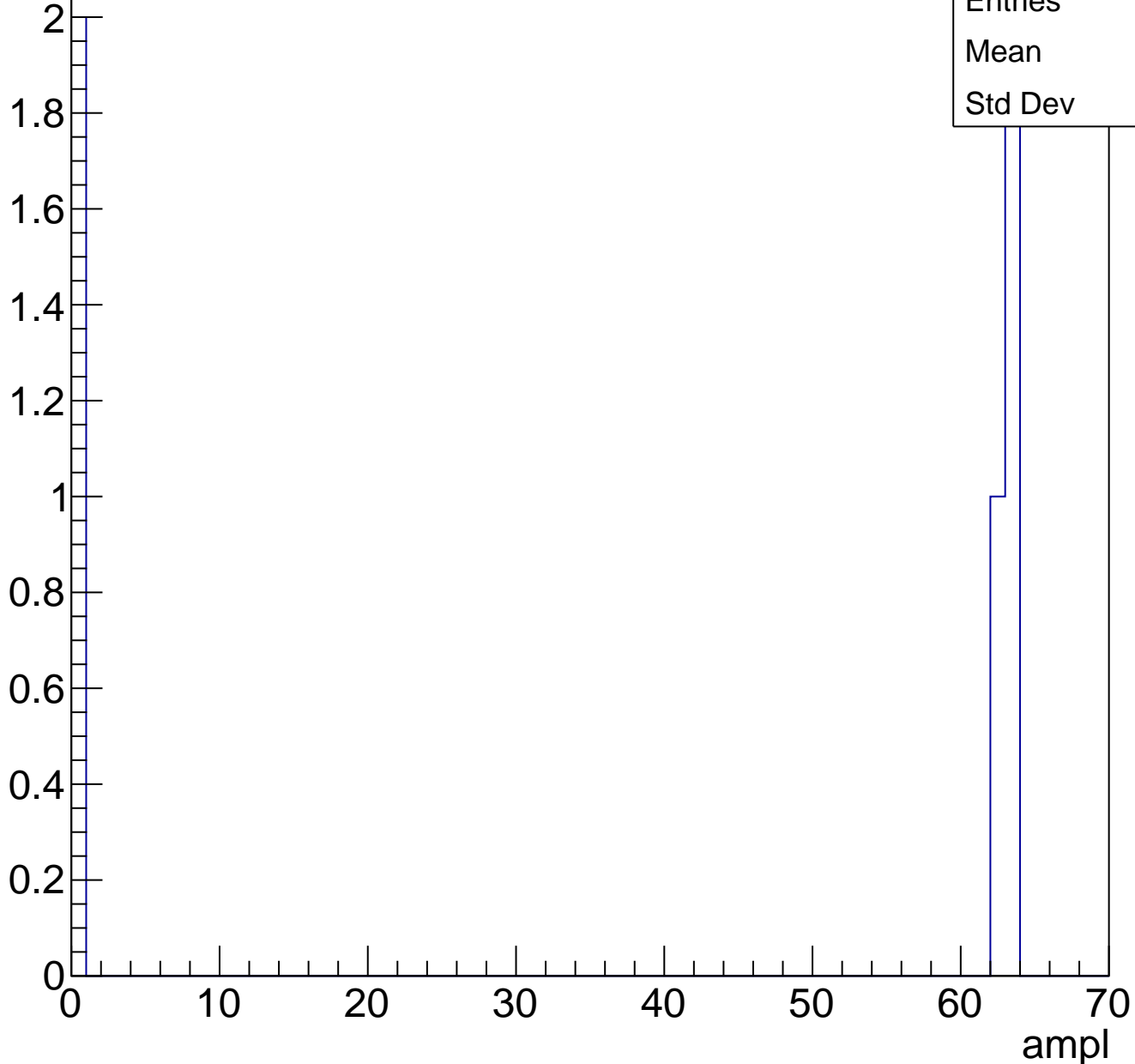




# B1L003S, U18-ch118, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	5
Mean	37.6
Std Dev	30.7

# B1L003S, U18-ch119, adc0

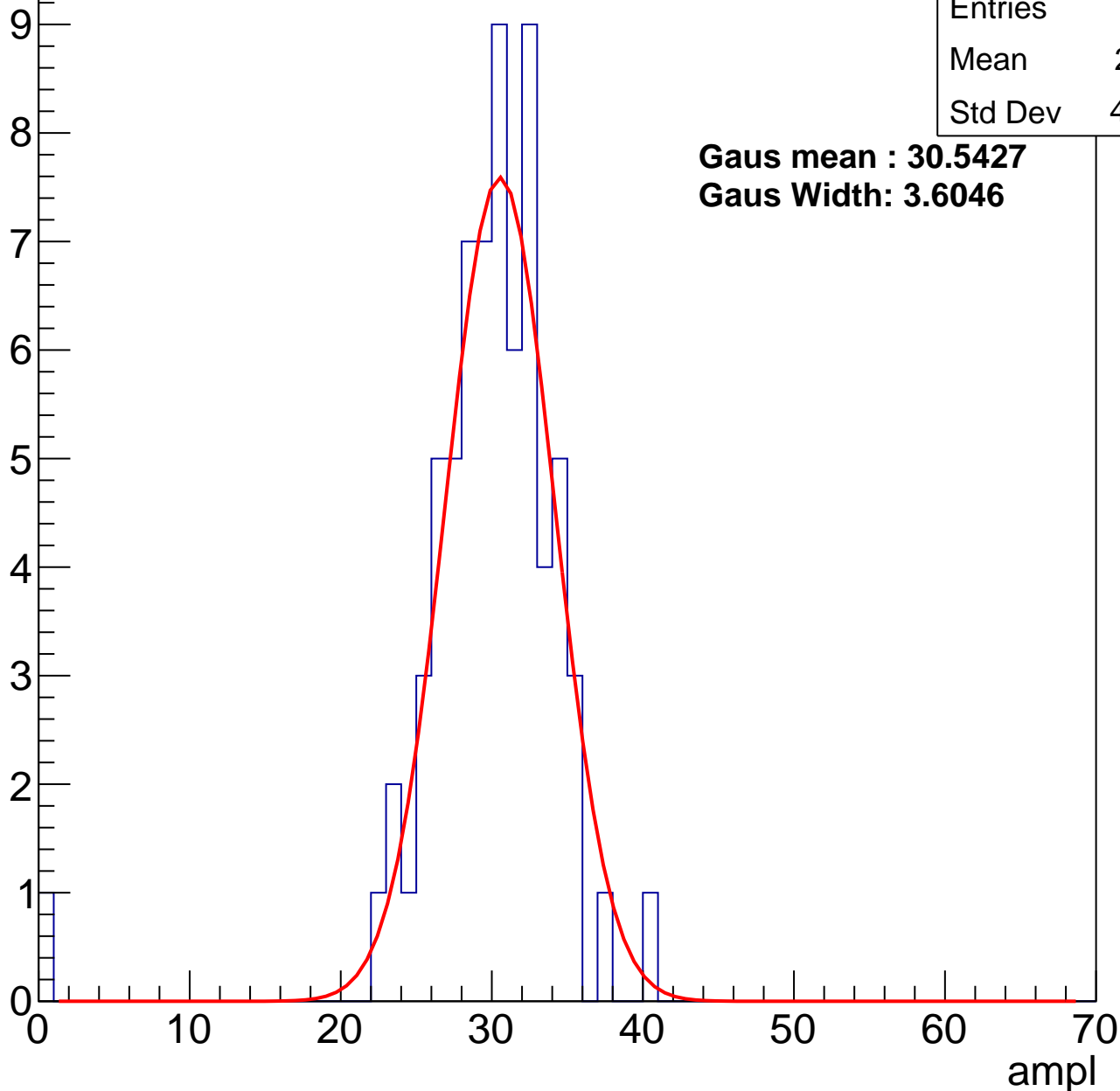
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	70
Mean	29.41
Std Dev	4.915

**Gaus mean : 30.5427**

**Gaus Width: 3.6046**



# B1L003S, U18-ch119, adc1

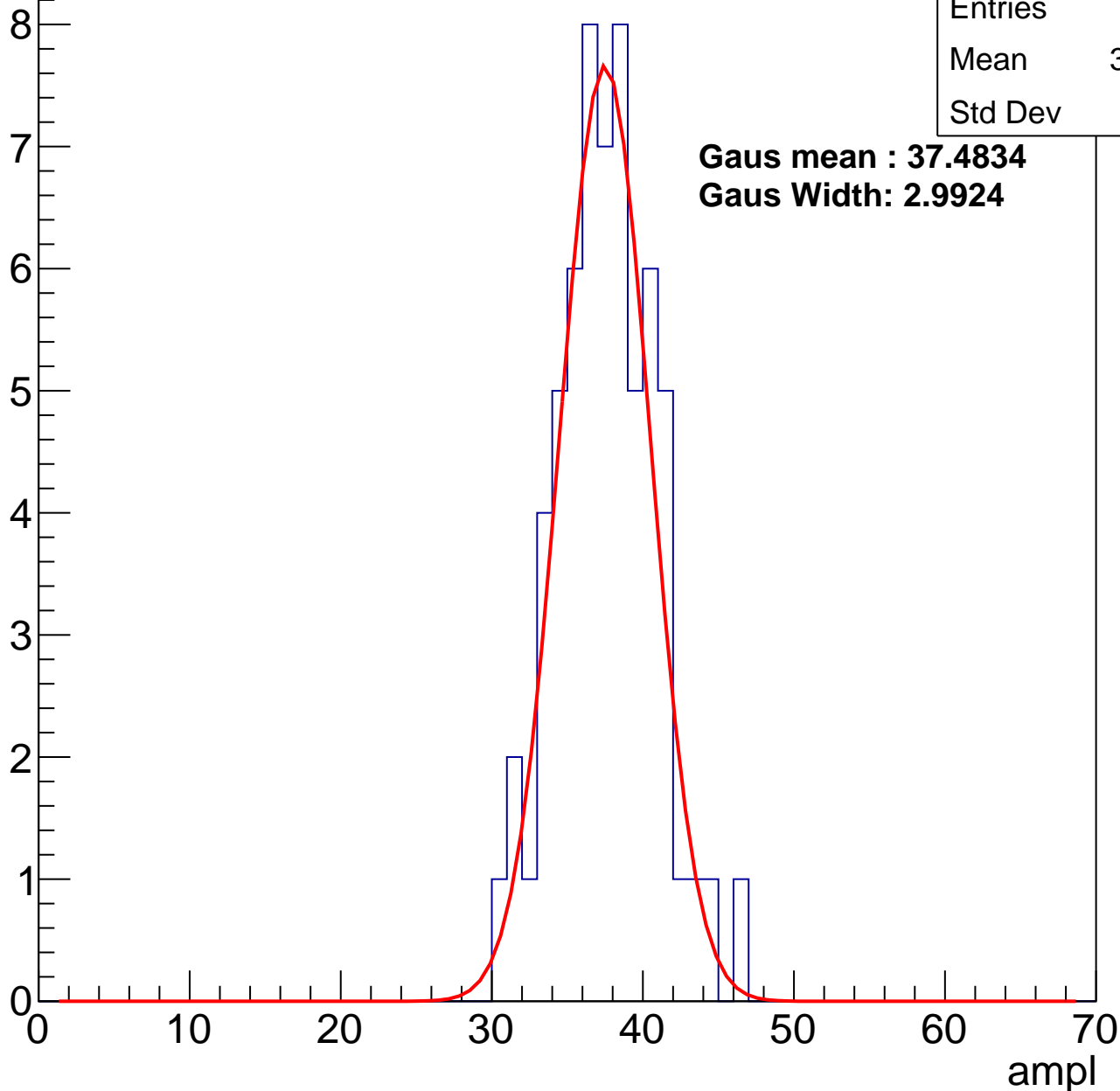
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	62
Mean	37.13
Std Dev	3.21

**Gaus mean : 37.4834**

**Gaus Width: 2.9924**



# B1L003S, U18-ch119, adc2

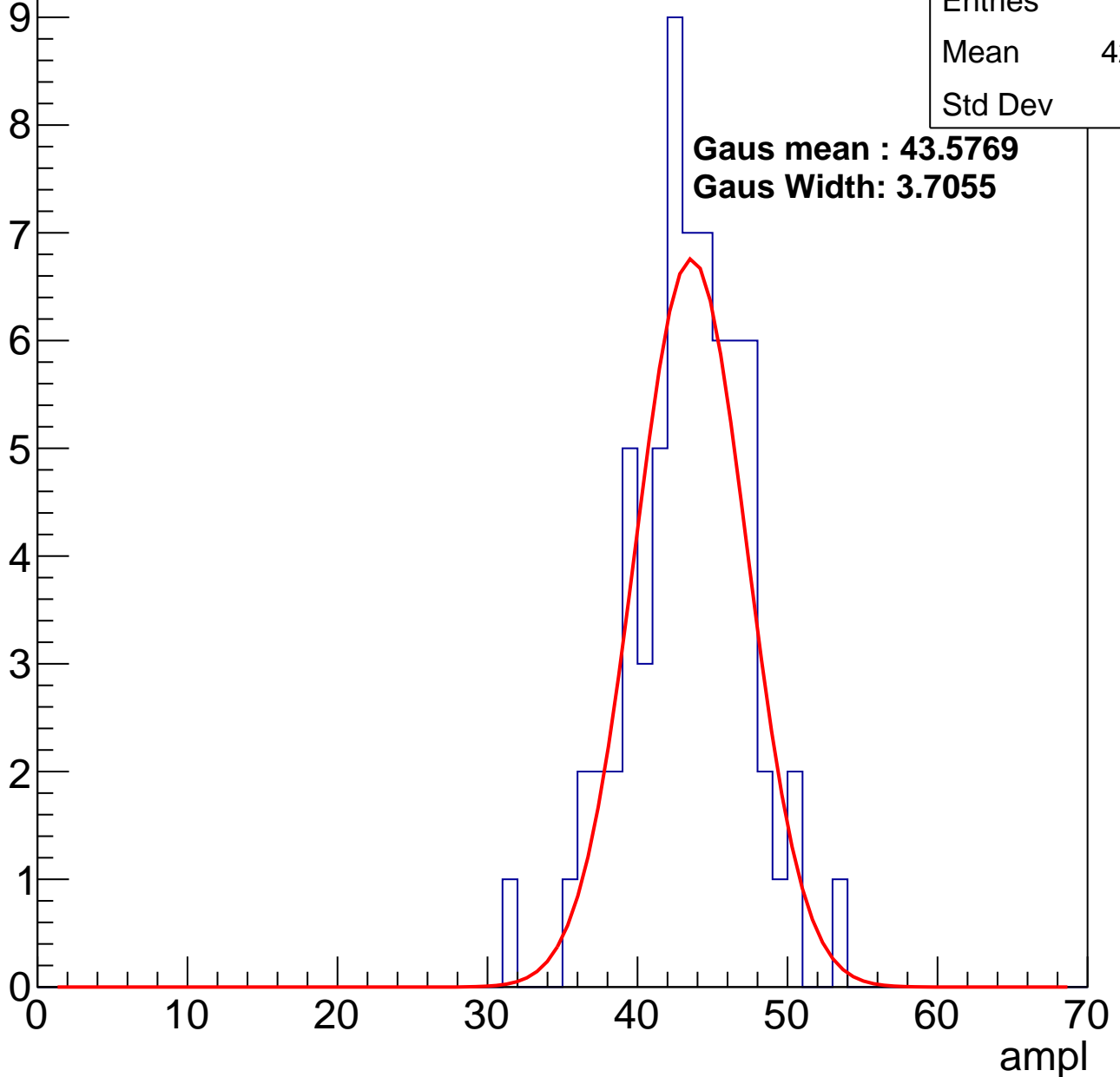
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	68
Mean	42.96
Std Dev	3.89

**Gaus mean : 43.5769**

**Gaus Width: 3.7055**

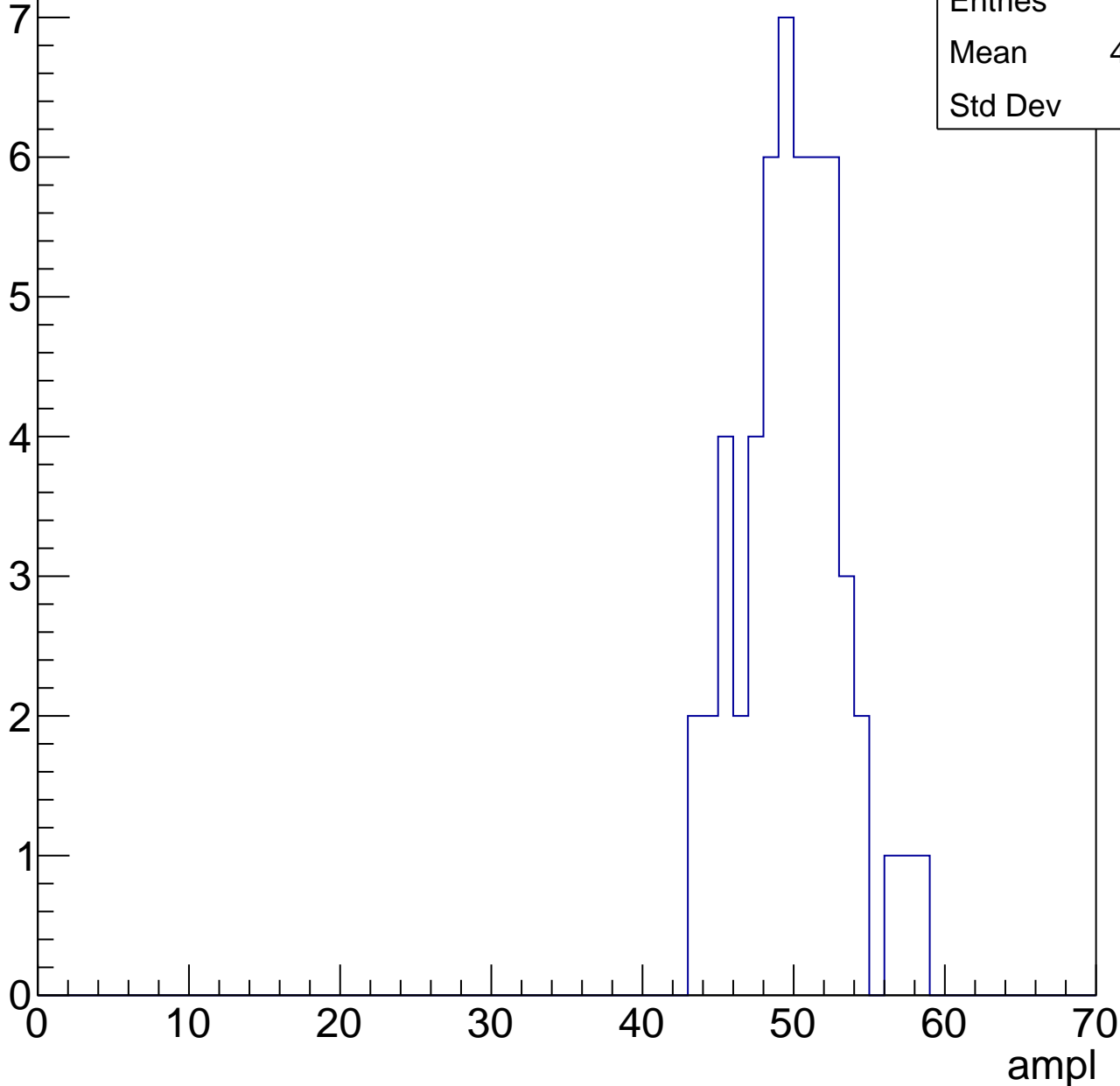


# B1L003S, U18-ch119, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	53
Mean	49.45
Std Dev	3.34

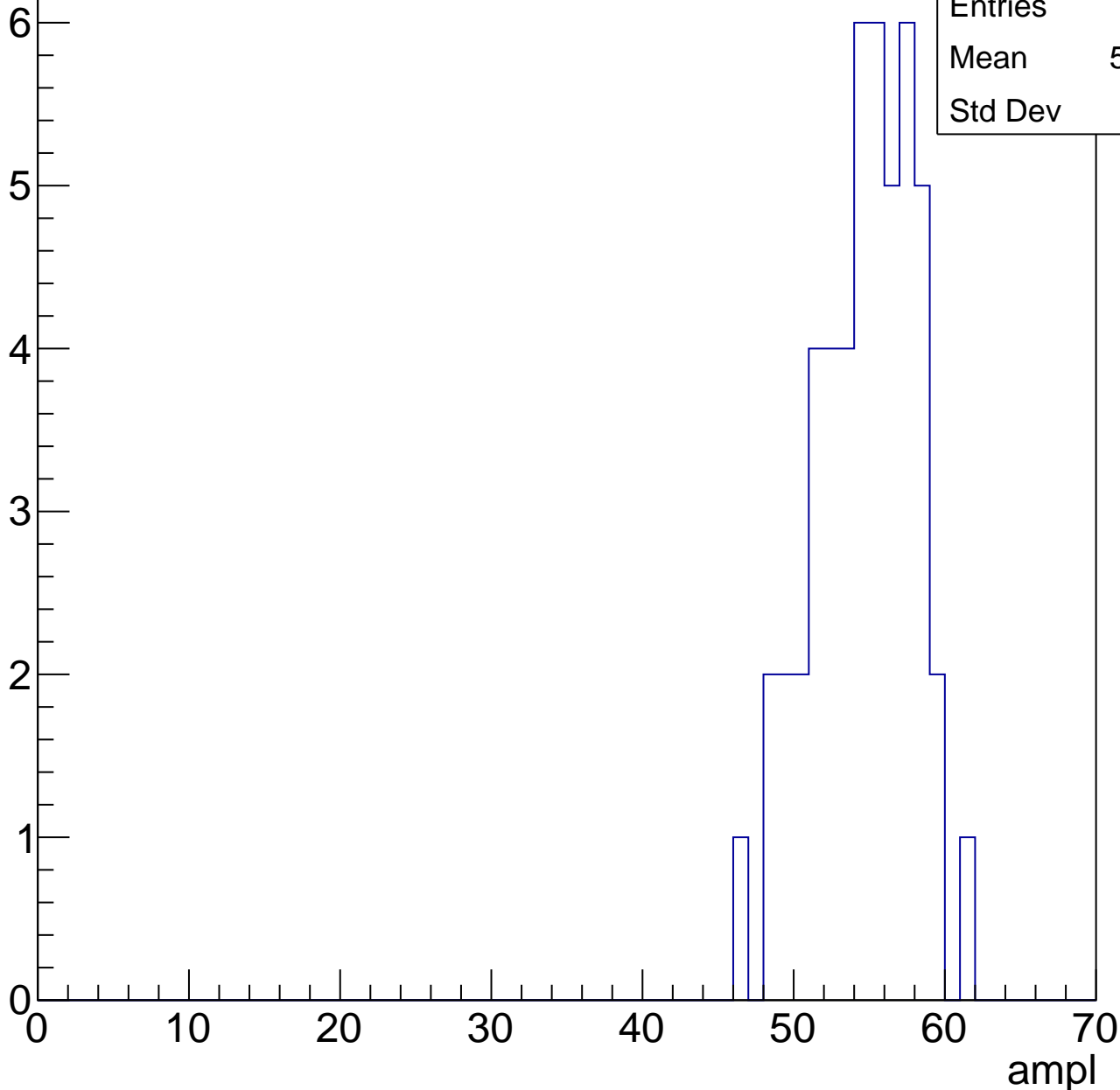


# B1L003S, U18-ch119, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	50
Mean	54.18
Std Dev	3.26

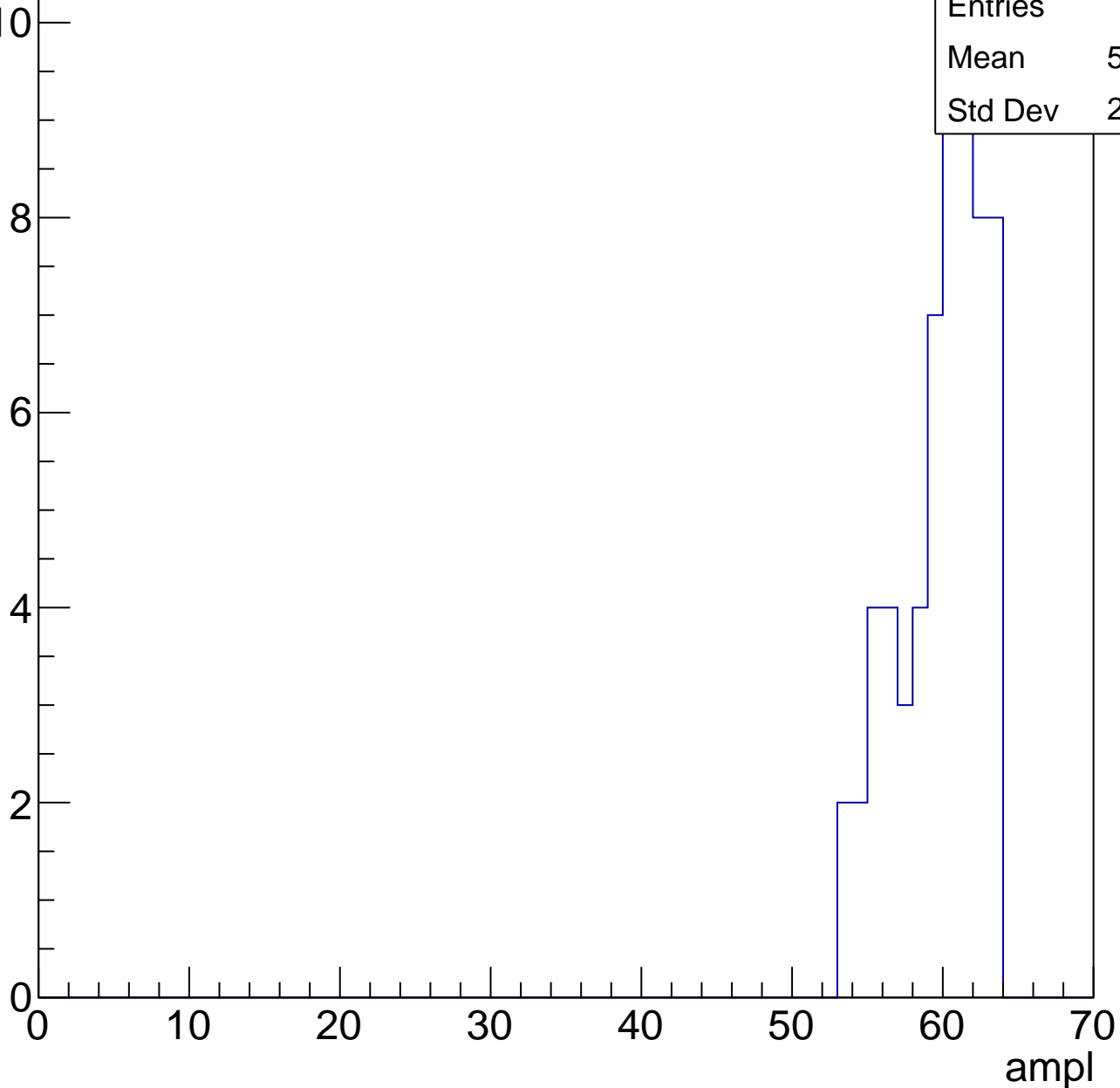


# B1L003S, U18-ch119, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

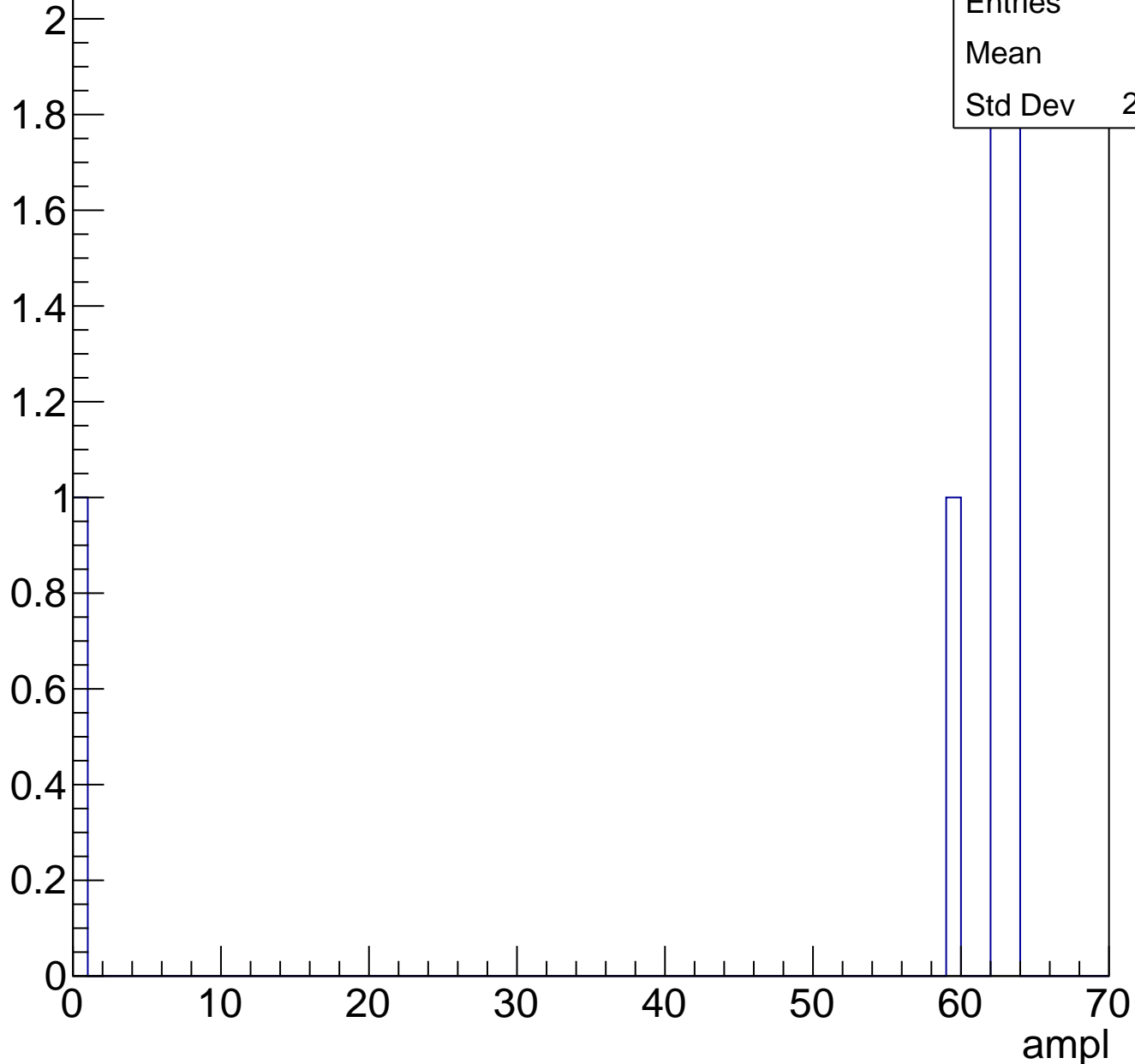
Entries	61
Mean	59.39
Std Dev	2.789



# B1L003S, U18-ch119, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U18-ch119, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U18-ch120, adc0

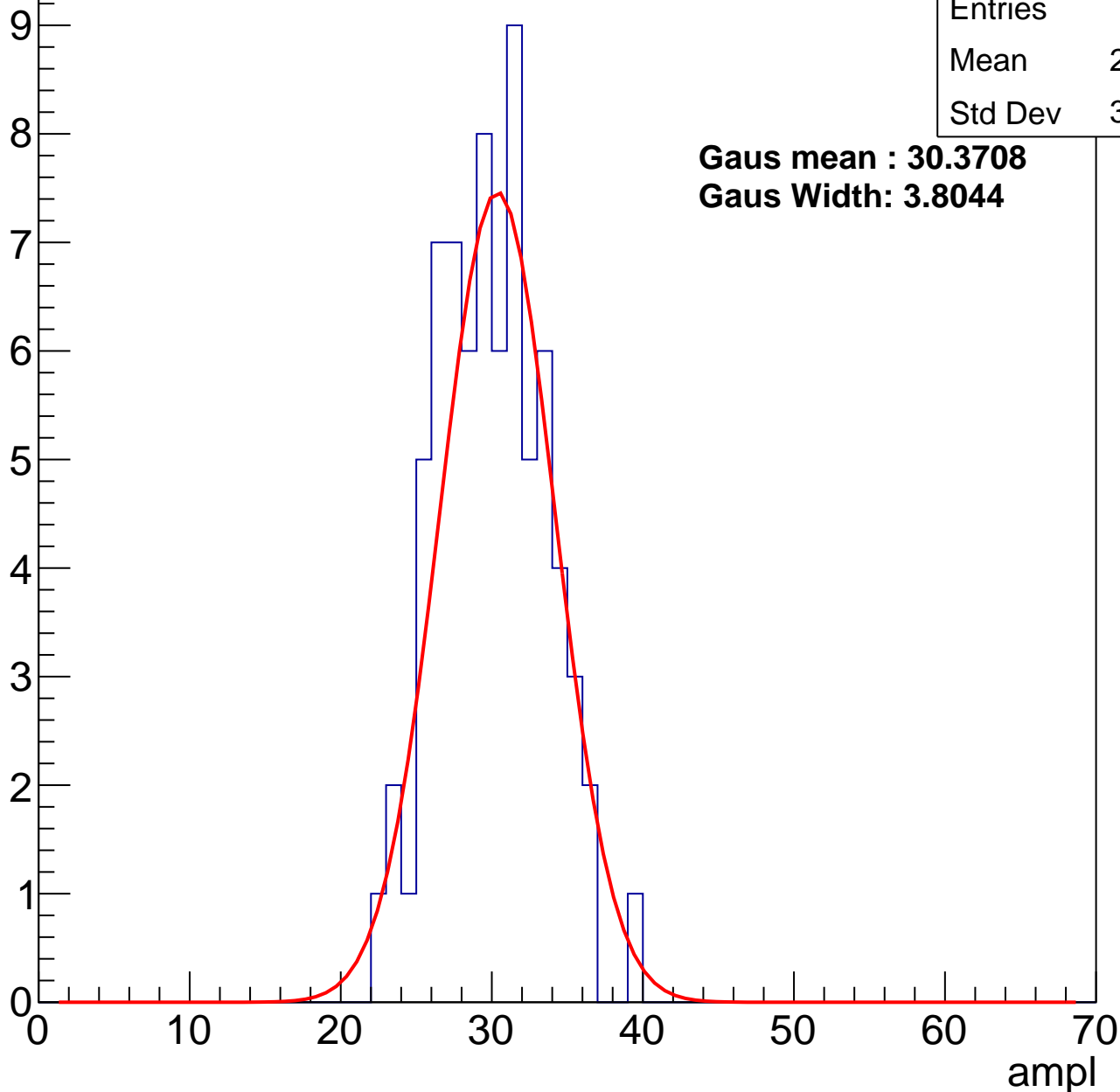
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	73
Mean	29.55
Std Dev	3.492

**Gaus mean : 30.3708**

**Gaus Width: 3.8044**



# B1L003S, U18-ch120, adc1

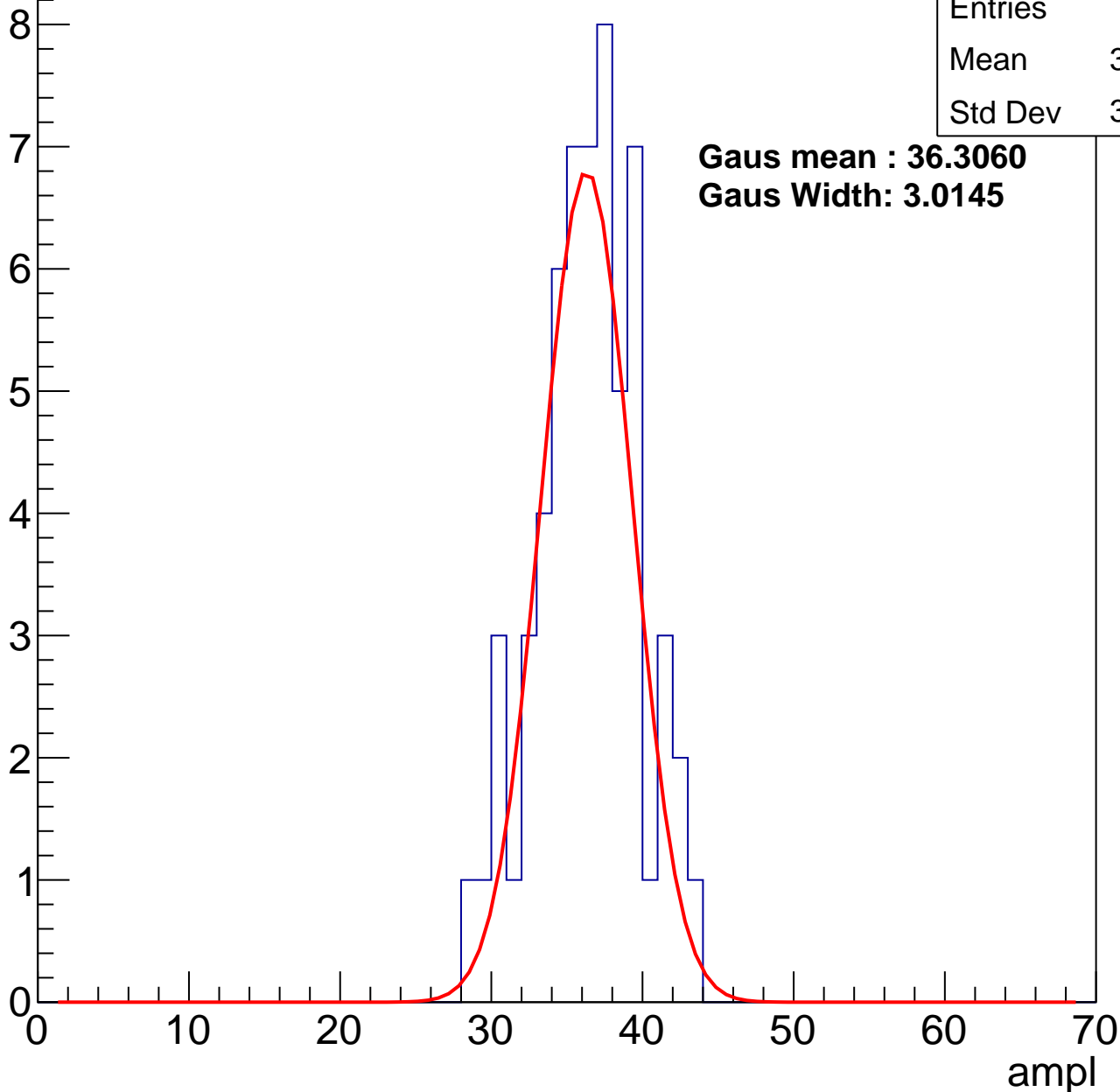
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	60
Mean	35.93
Std Dev	3.326

**Gaus mean : 36.3060**

**Gaus Width: 3.0145**



# B1L003S, U18-ch120, adc2

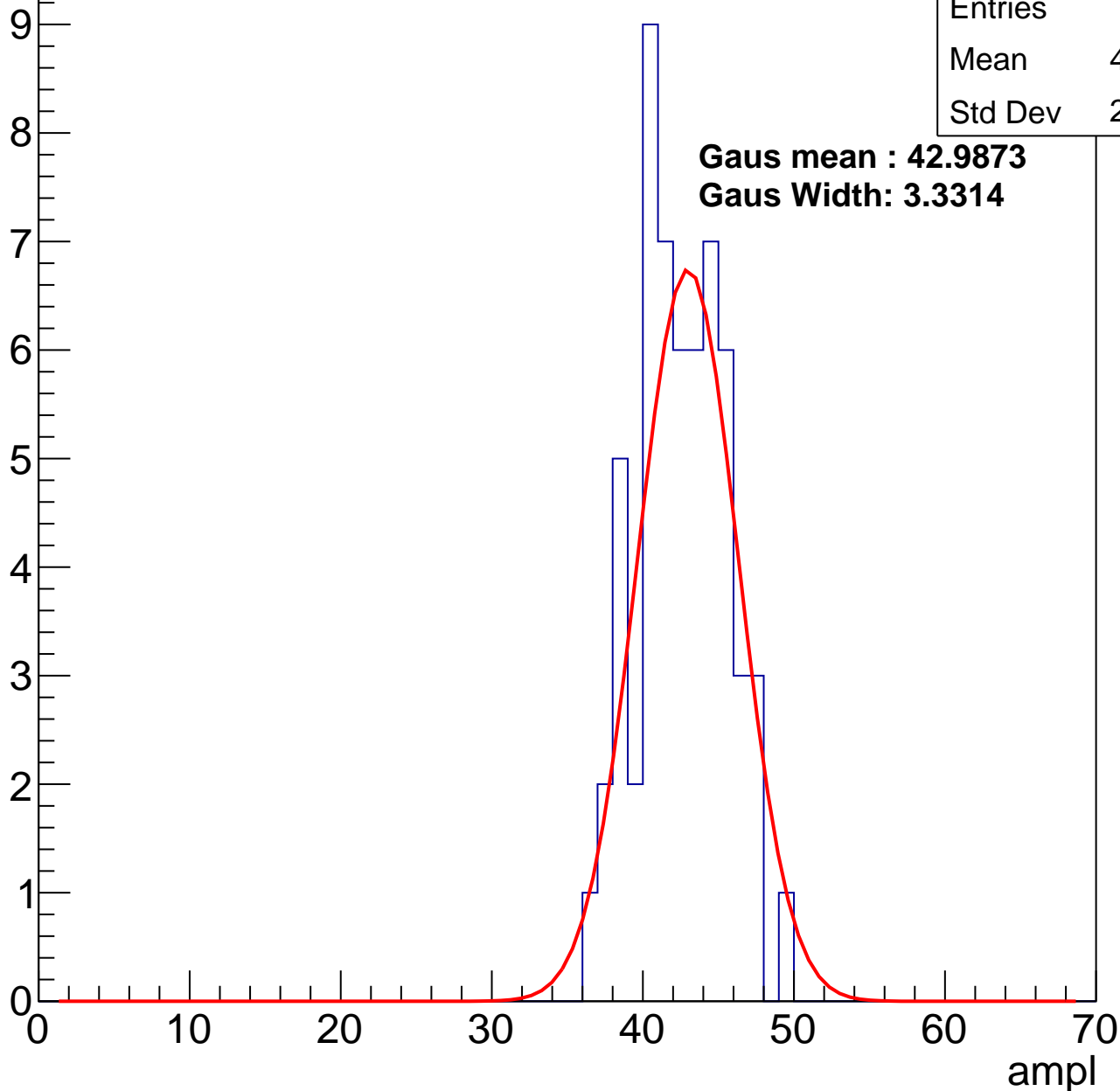
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	58
Mean	42.09
Std Dev	2.896

**Gaus mean : 42.9873**

**Gaus Width: 3.3314**

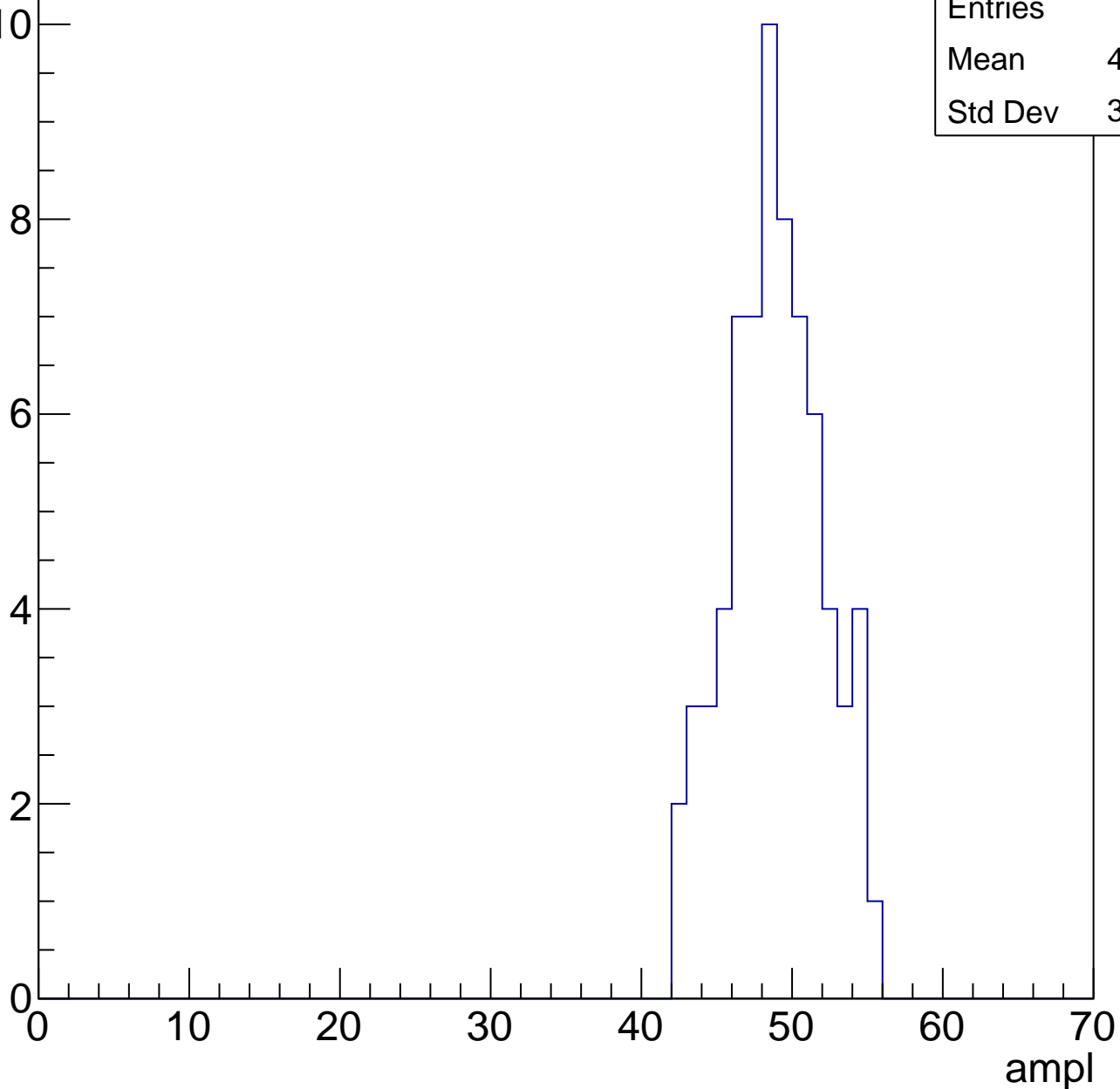


# B1L003S, U18-ch120, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	69
Mean	48.43
Std Dev	3.128

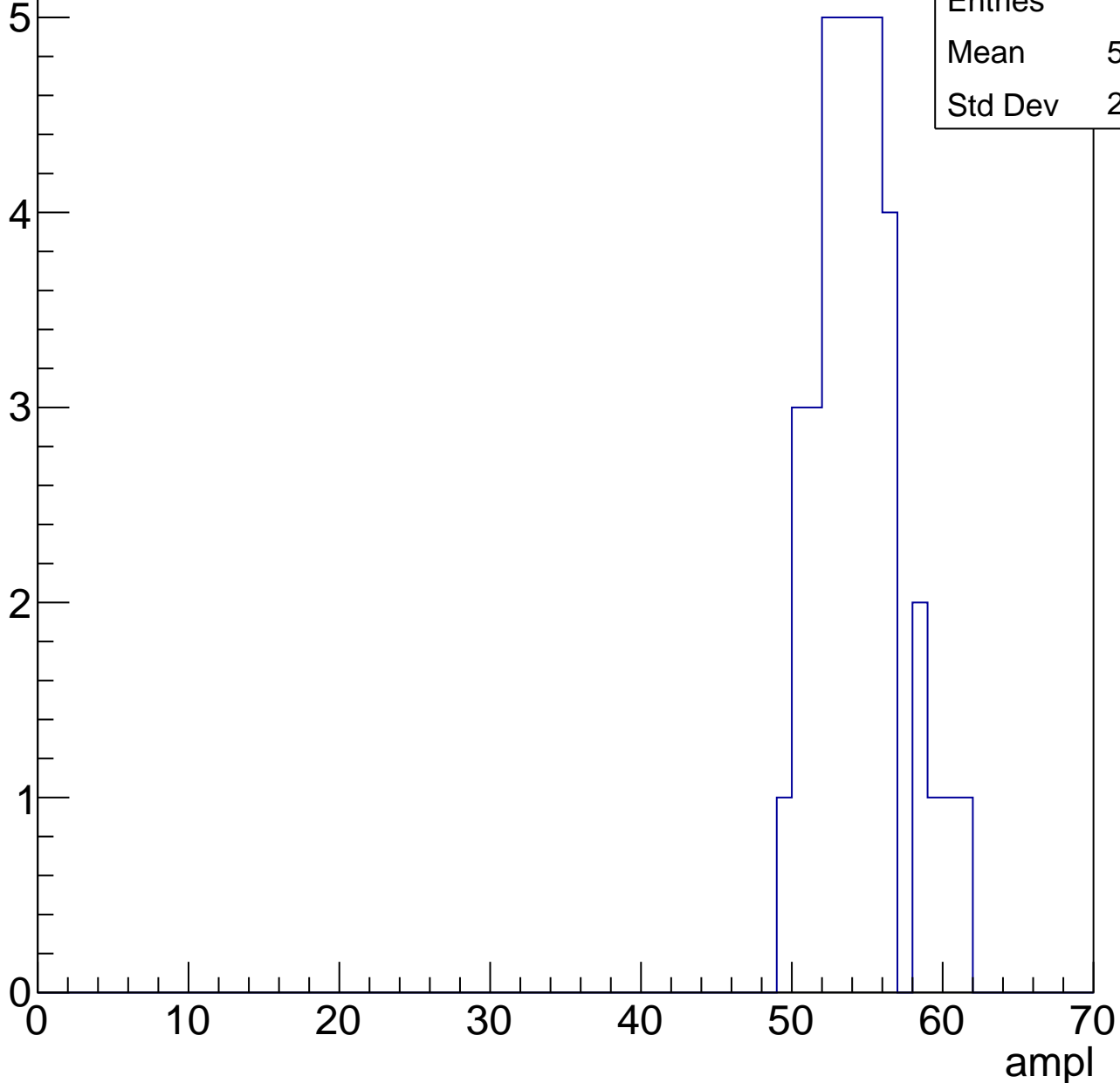


# B1L003S, U18-ch120, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

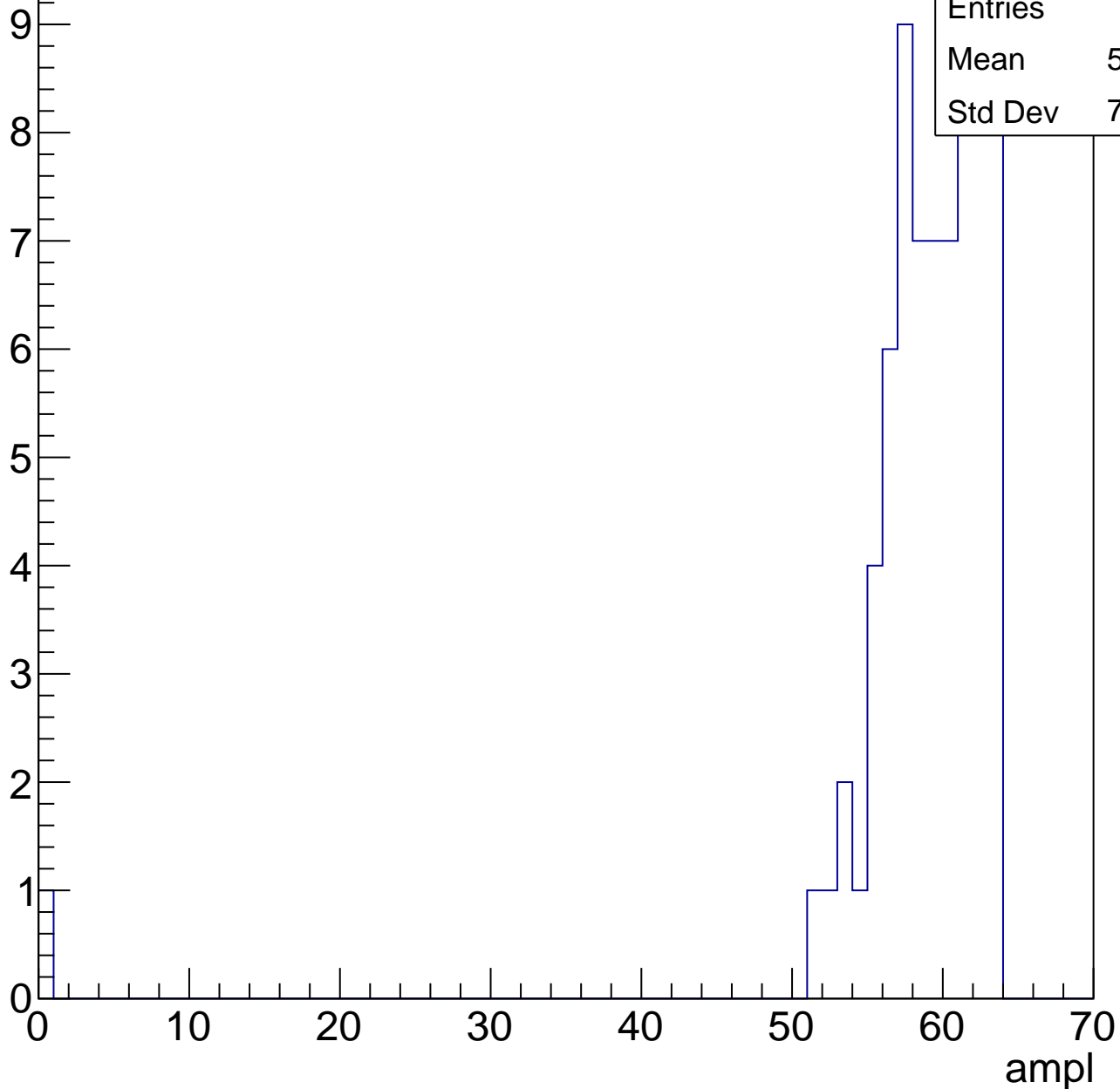
Entries	36
Mean	53.94
Std Dev	2.828



# B1L003S, U18-ch120, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U18-ch120, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

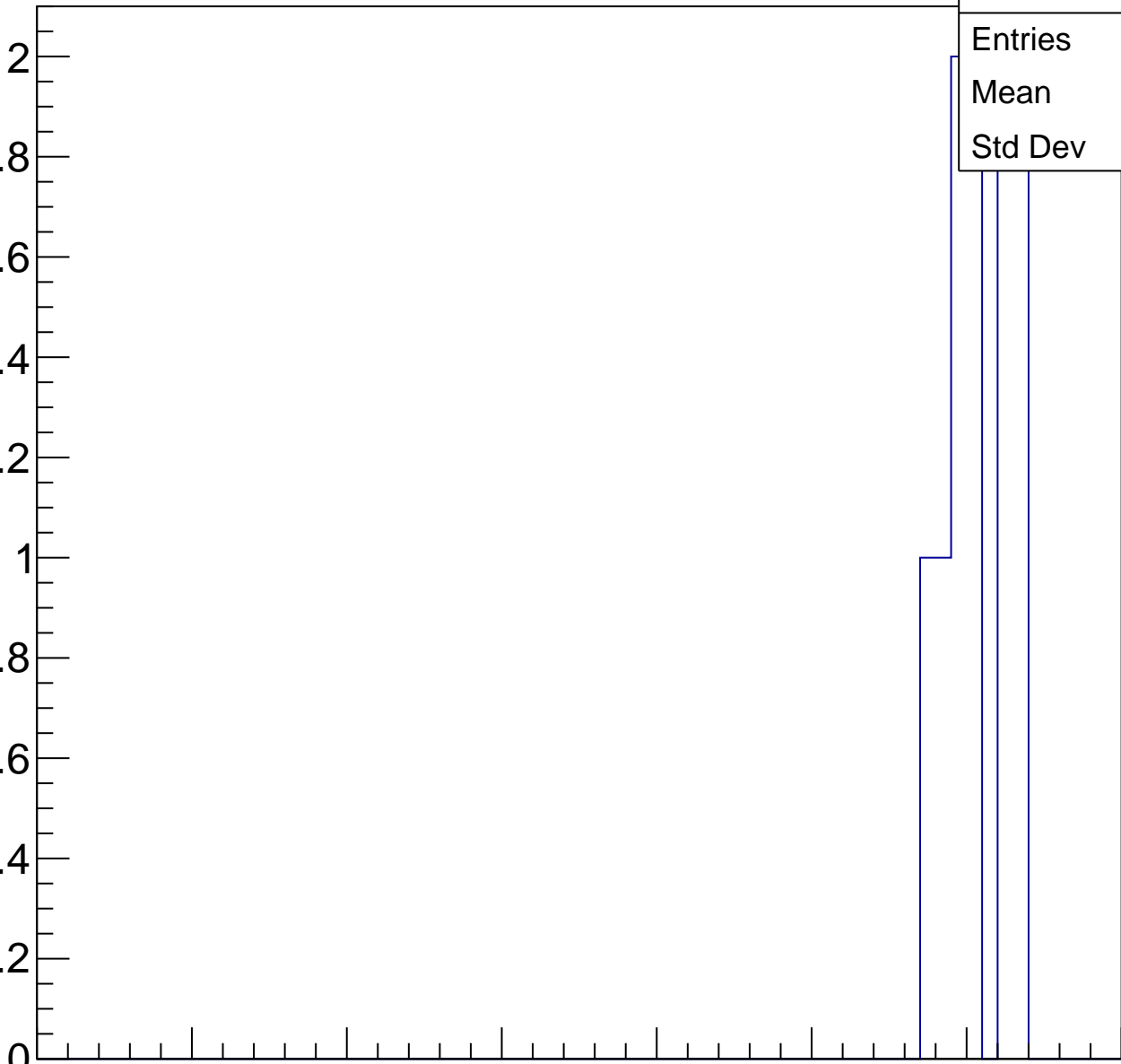
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	10
Mean	60.3
Std Dev	2.002

0 10 20 30 40 50 60 70

ampl





# B1L003S, U18-ch120, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

1  
0.8  
0.6  
0.4  
0.2  
0

Entries	1
Mean	20
Std Dev	0

ampl

# B1L003S, U18-ch121, adc0

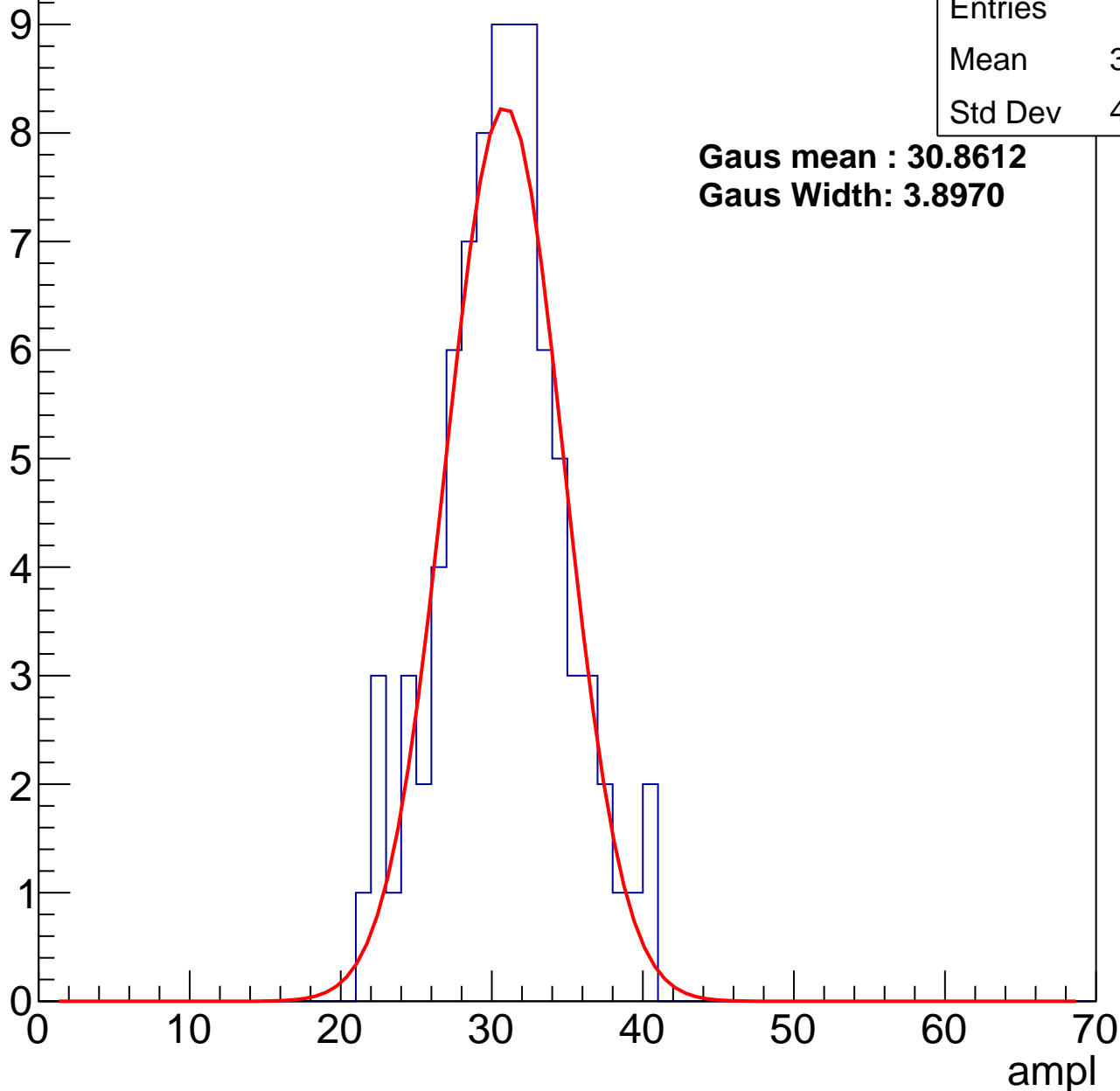
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	85
Mean	30.29
Std Dev	4.104

**Gaus mean : 30.8612**

**Gaus Width: 3.8970**



# B1L003S, U18-ch121, adc1

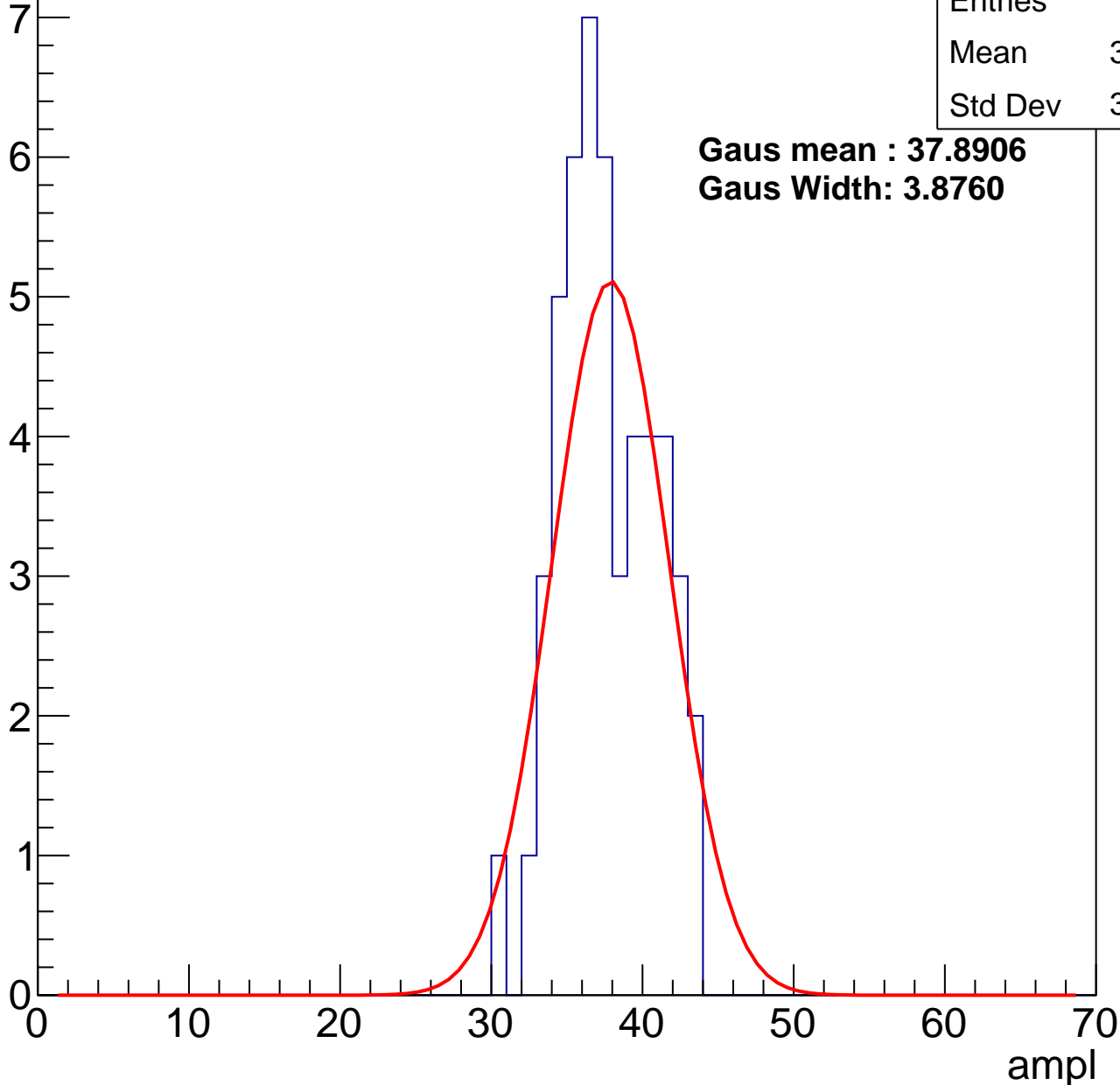
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	49
Mean	37.16
Std Dev	3.073

**Gaus mean : 37.8906**

**Gaus Width: 3.8760**



# B1L003S, U18-ch121, adc2

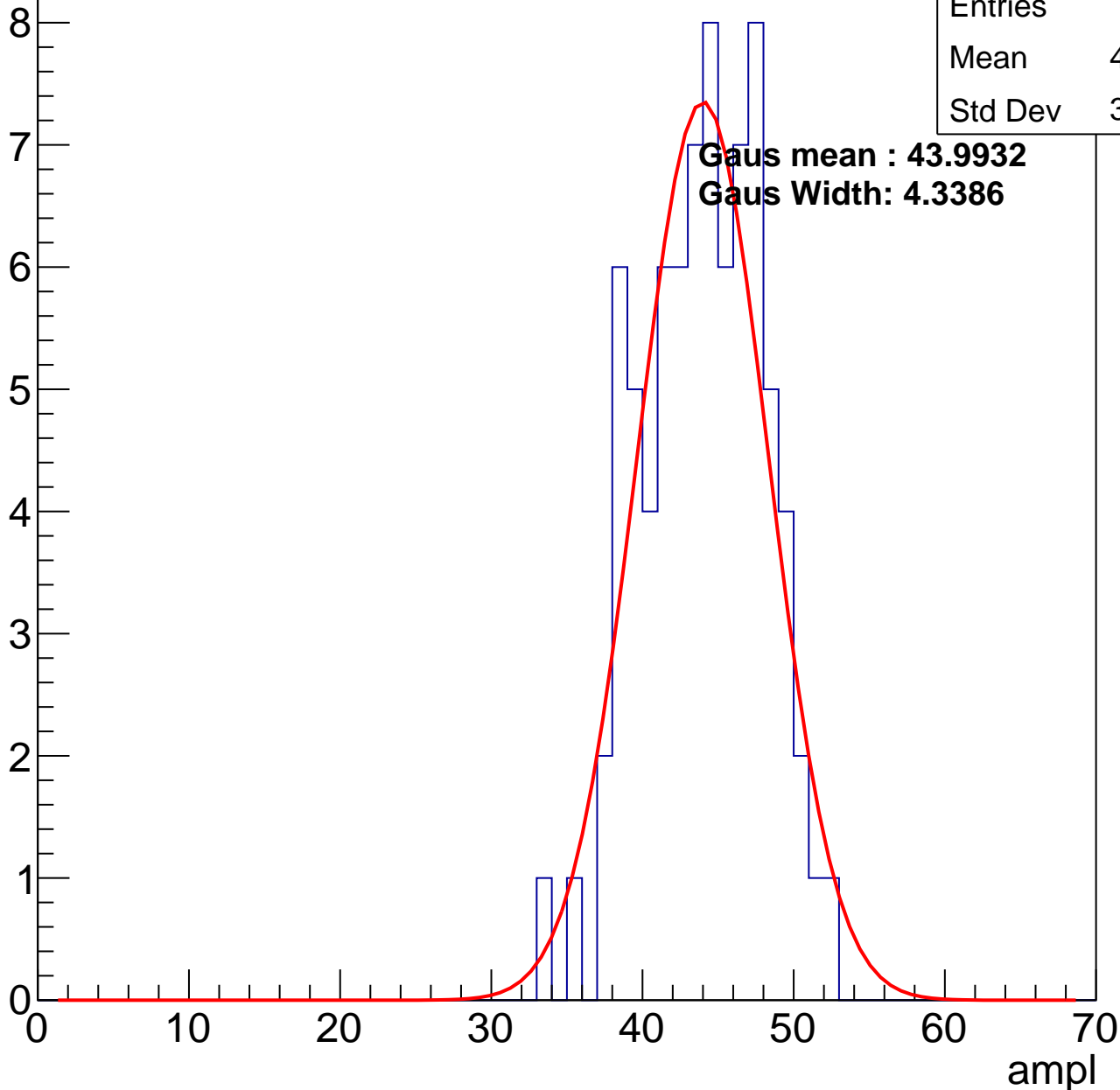
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	80
Mean	43.54
Std Dev	3.943

**Gaus mean : 43.9932**

**Gaus Width: 4.3386**

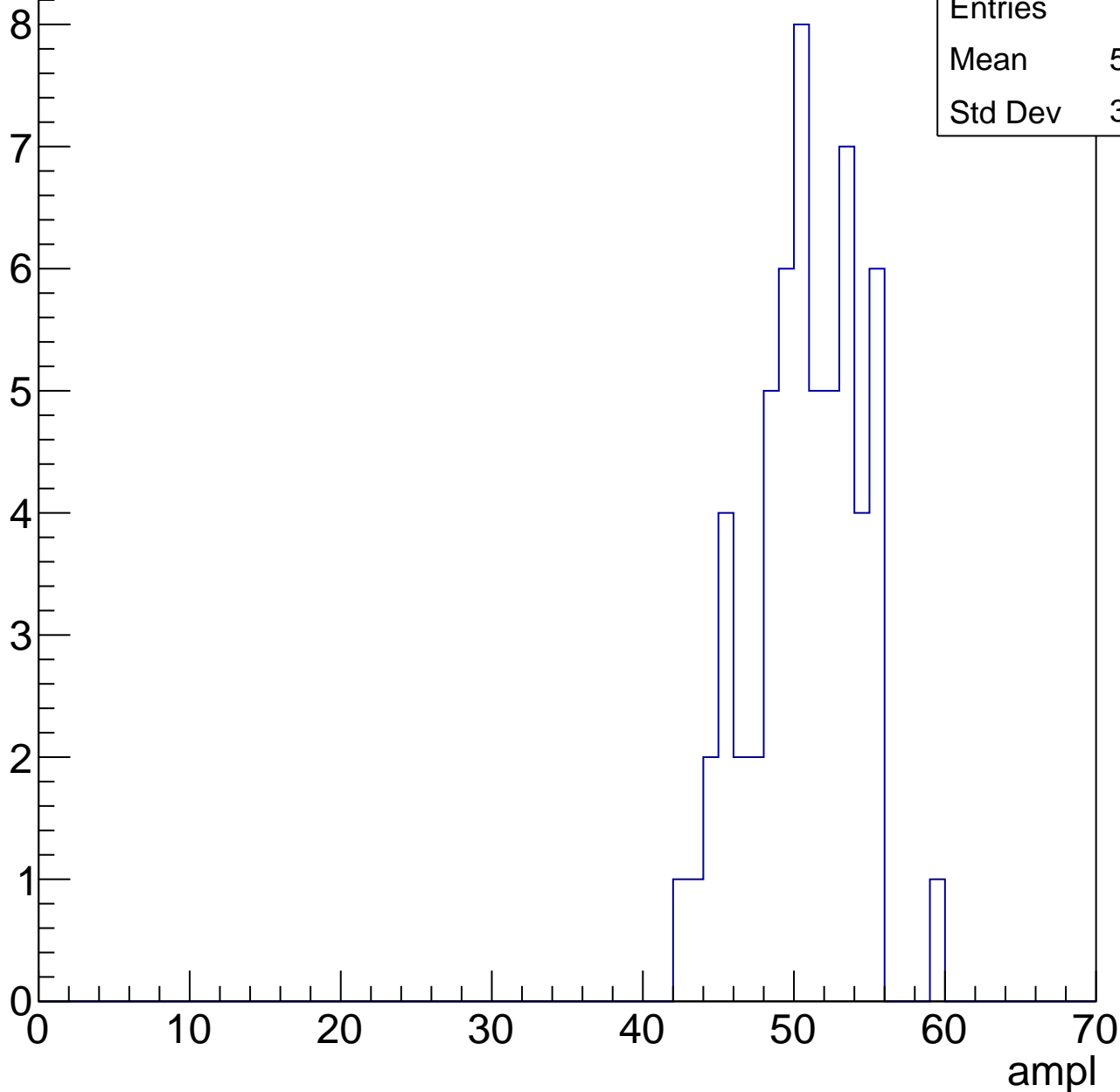


# B1L003S, U18-ch121, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

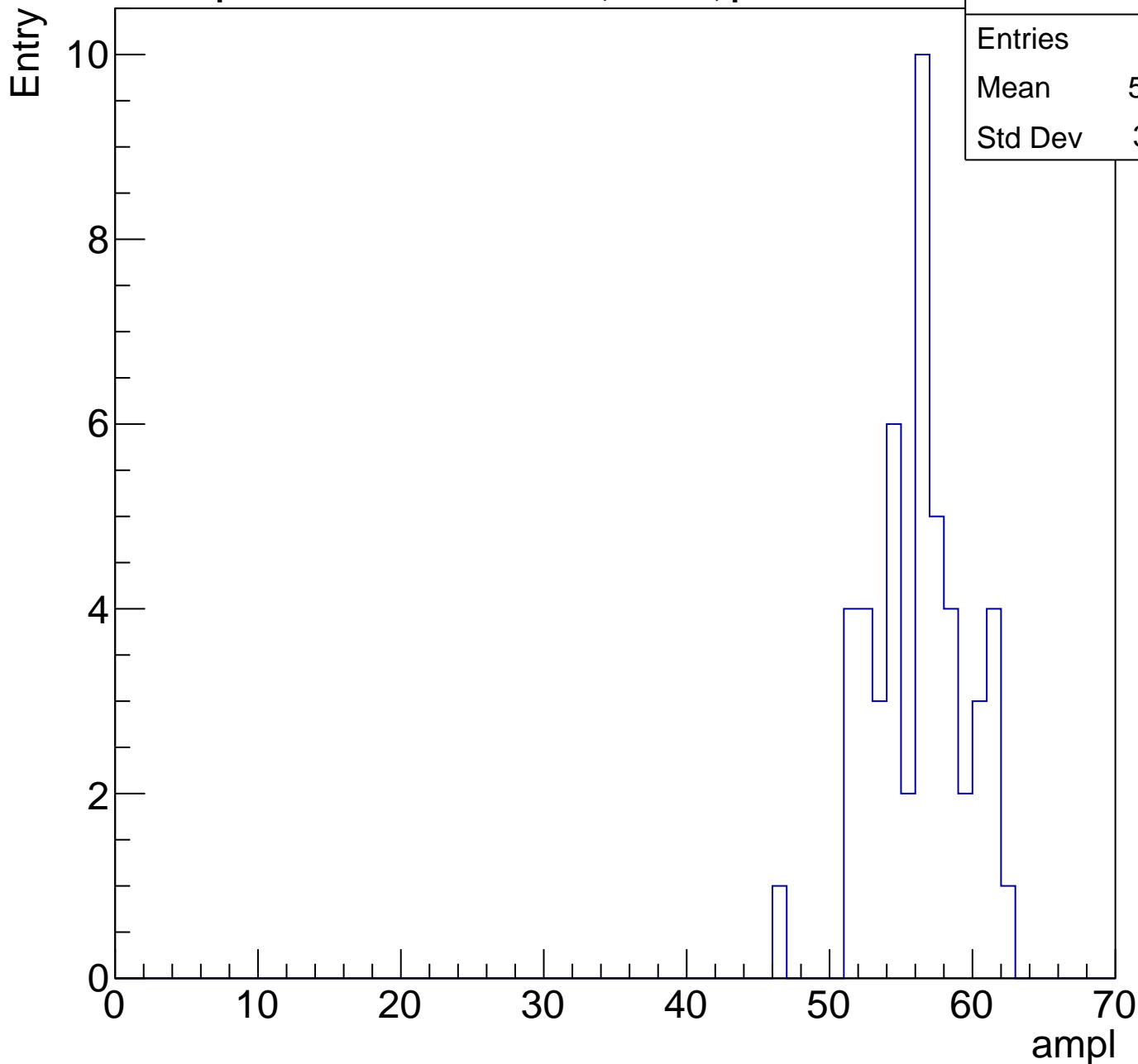
Entries	59
Mean	50.24
Std Dev	3.543



# B1L003S, U18-ch121, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

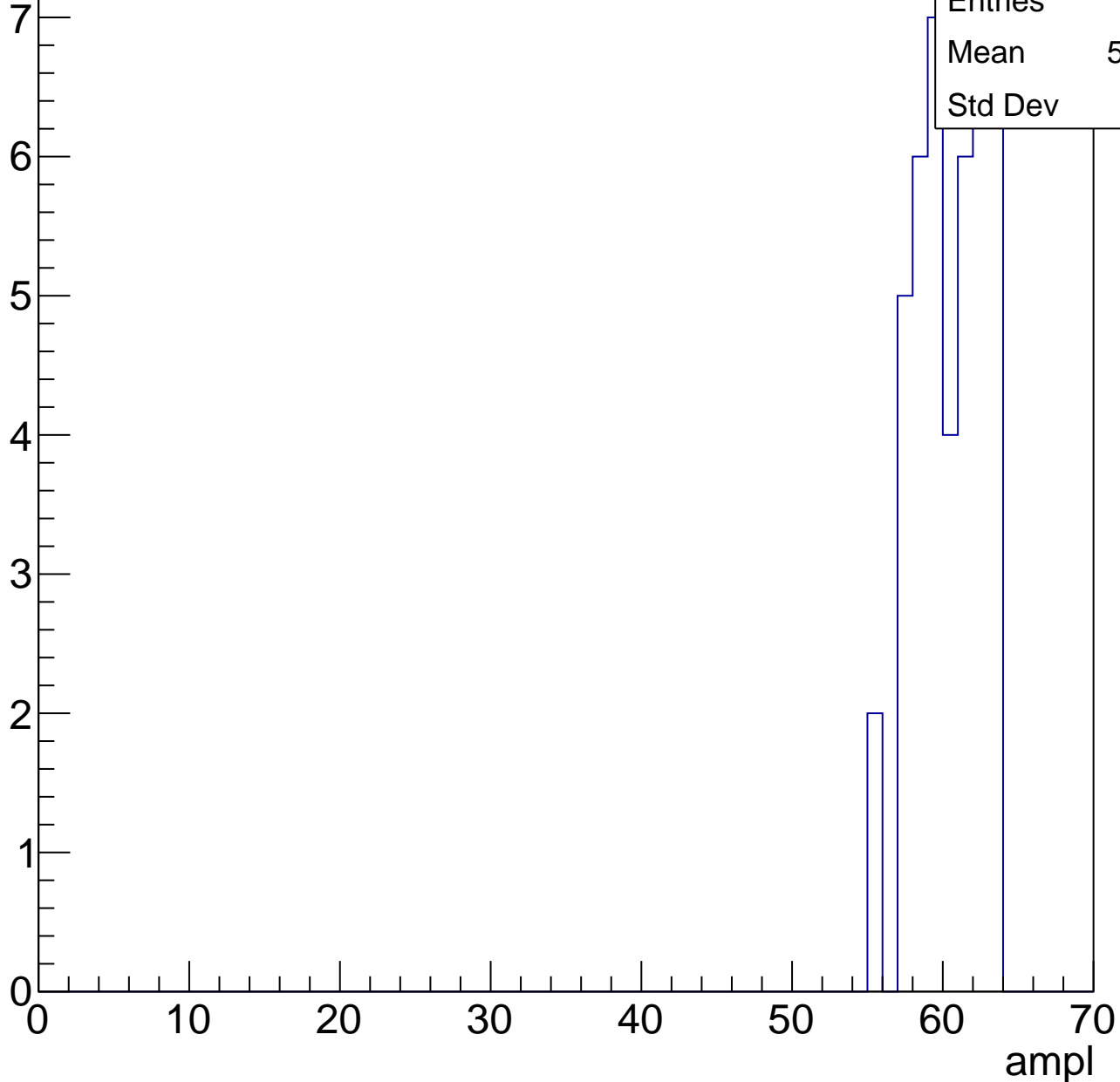
Entries	49
Mean	55.76
Std Dev	3.311



# B1L003S, U18-ch121, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U18-ch121, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

3

2.5

2

1.5

1

0.5

0

0

10

20

30

40

50

60

70

ampl

Entries

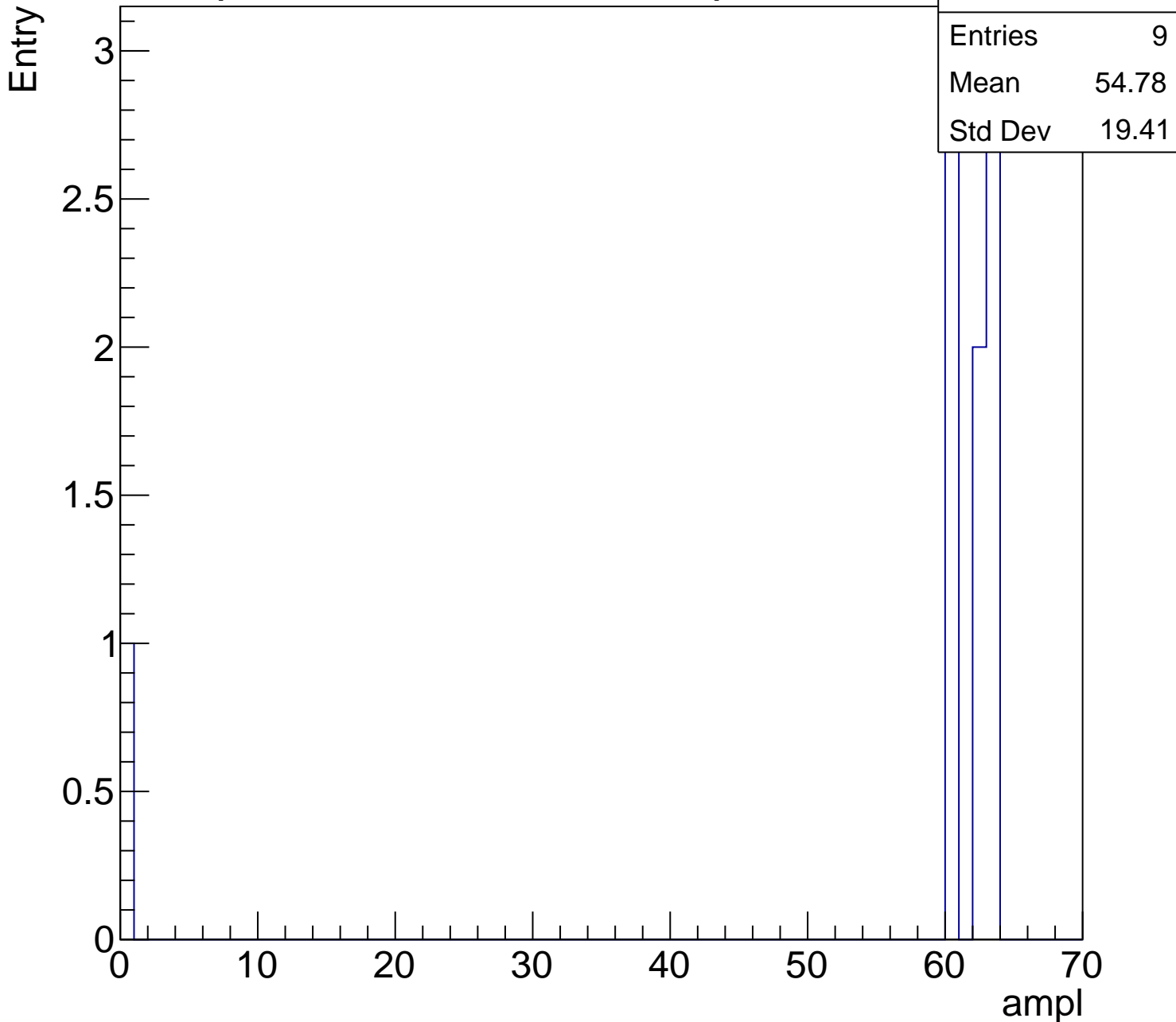
9

Mean

54.78

Std Dev

19.41





# B1L003S, U18-ch121, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U18-ch122, adc0

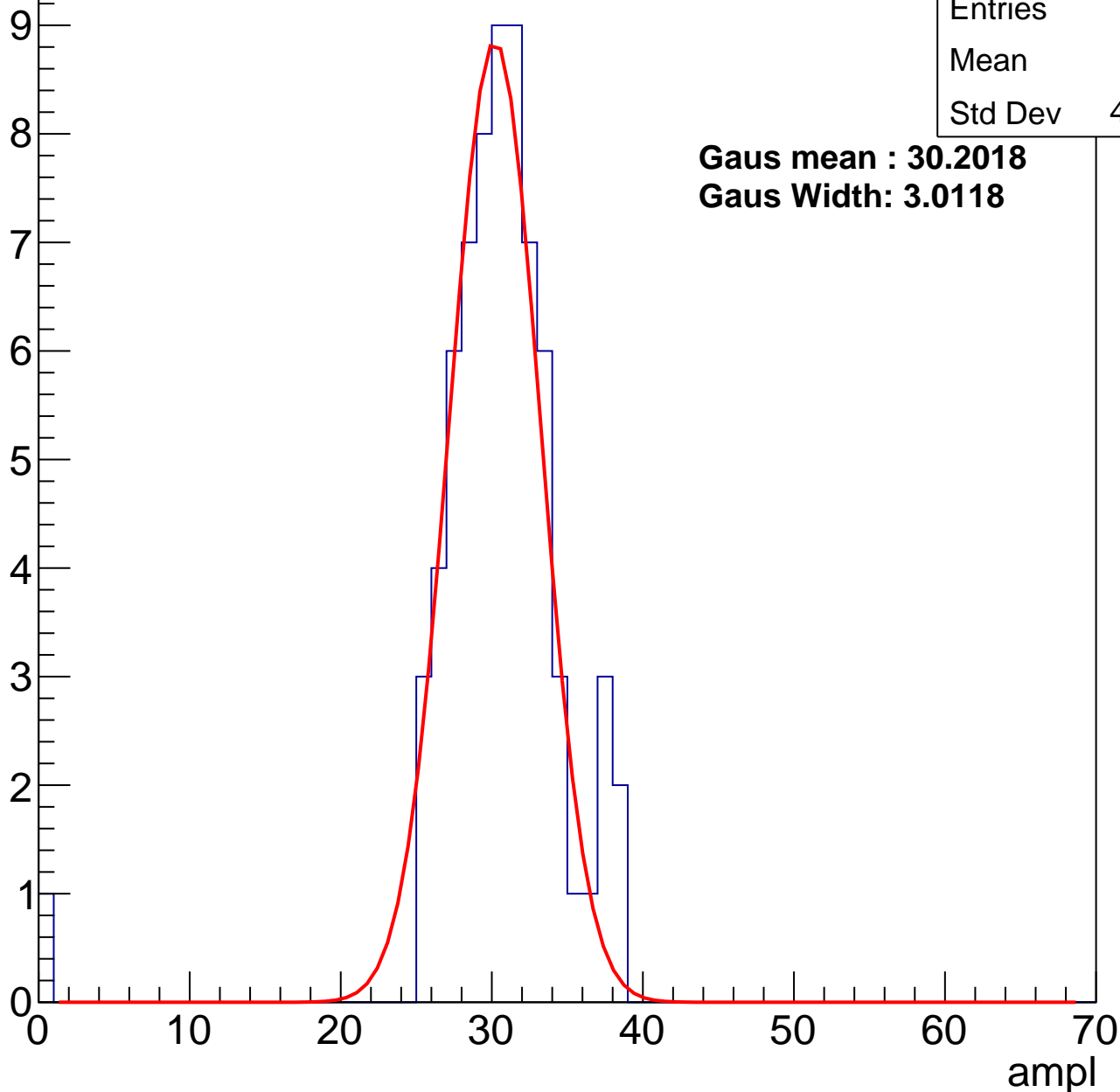
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	70
Mean	30
Std Dev	4.787

**Gaus mean : 30.2018**

**Gaus Width: 3.0118**



# B1L003S, U18-ch122, adc1

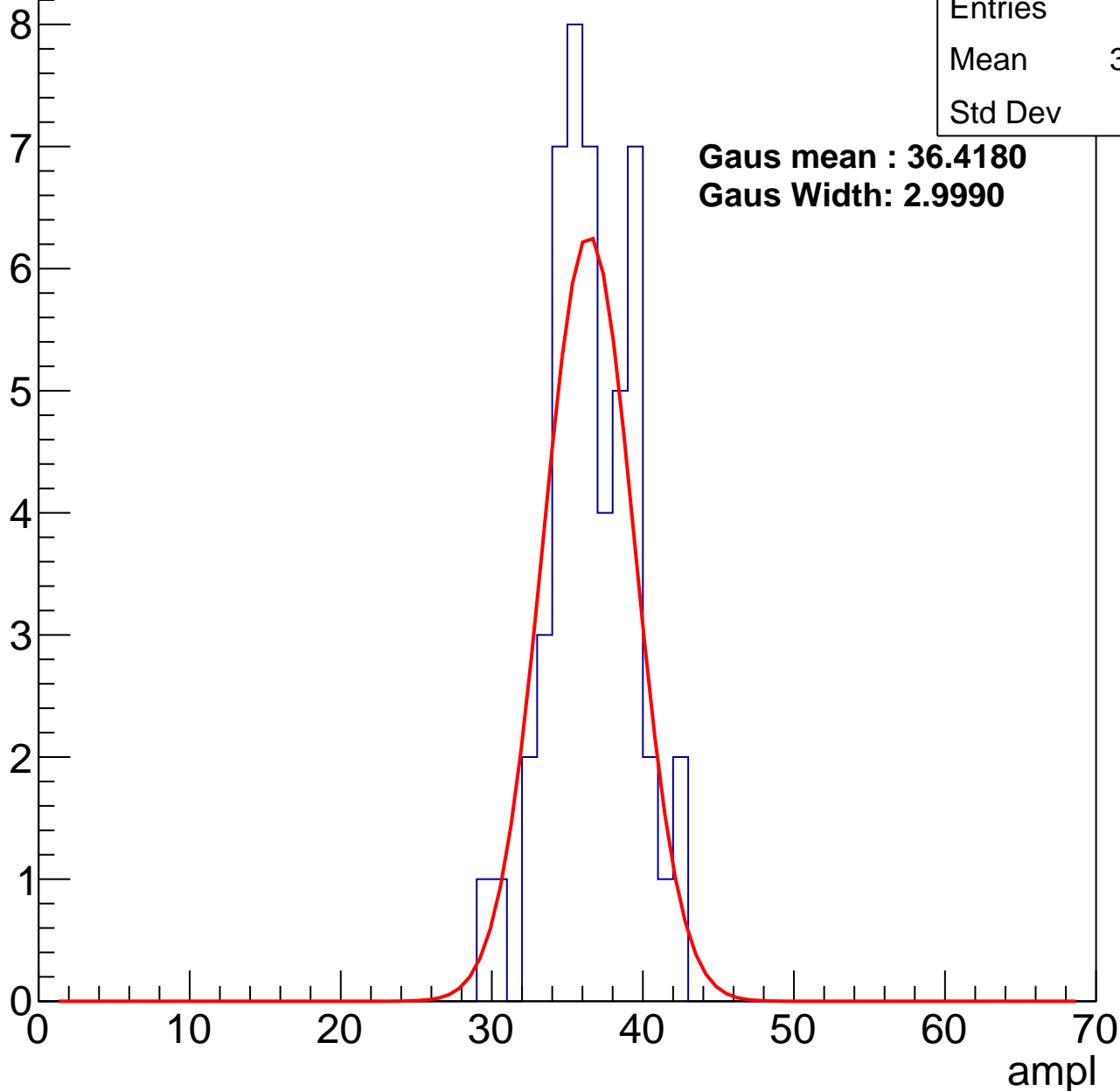
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	50
Mean	36.16
Std Dev	2.81

**Gaus mean : 36.4180**

**Gaus Width: 2.9990**



# B1L003S, U18-ch122, adc2

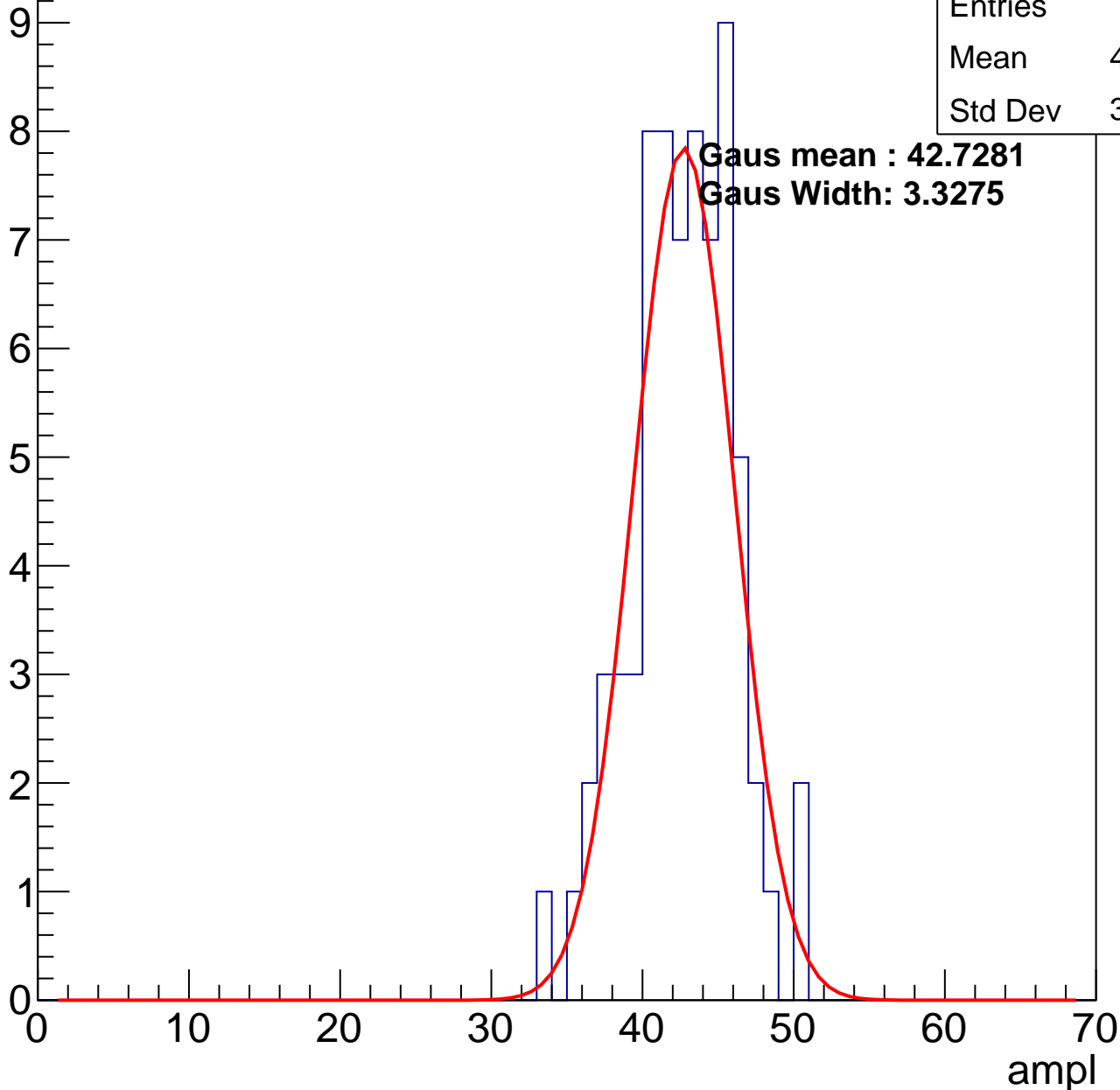
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	70
Mean	42.19
Std Dev	3.382

**Gaus mean : 42.7281**

**Gaus Width: 3.3275**

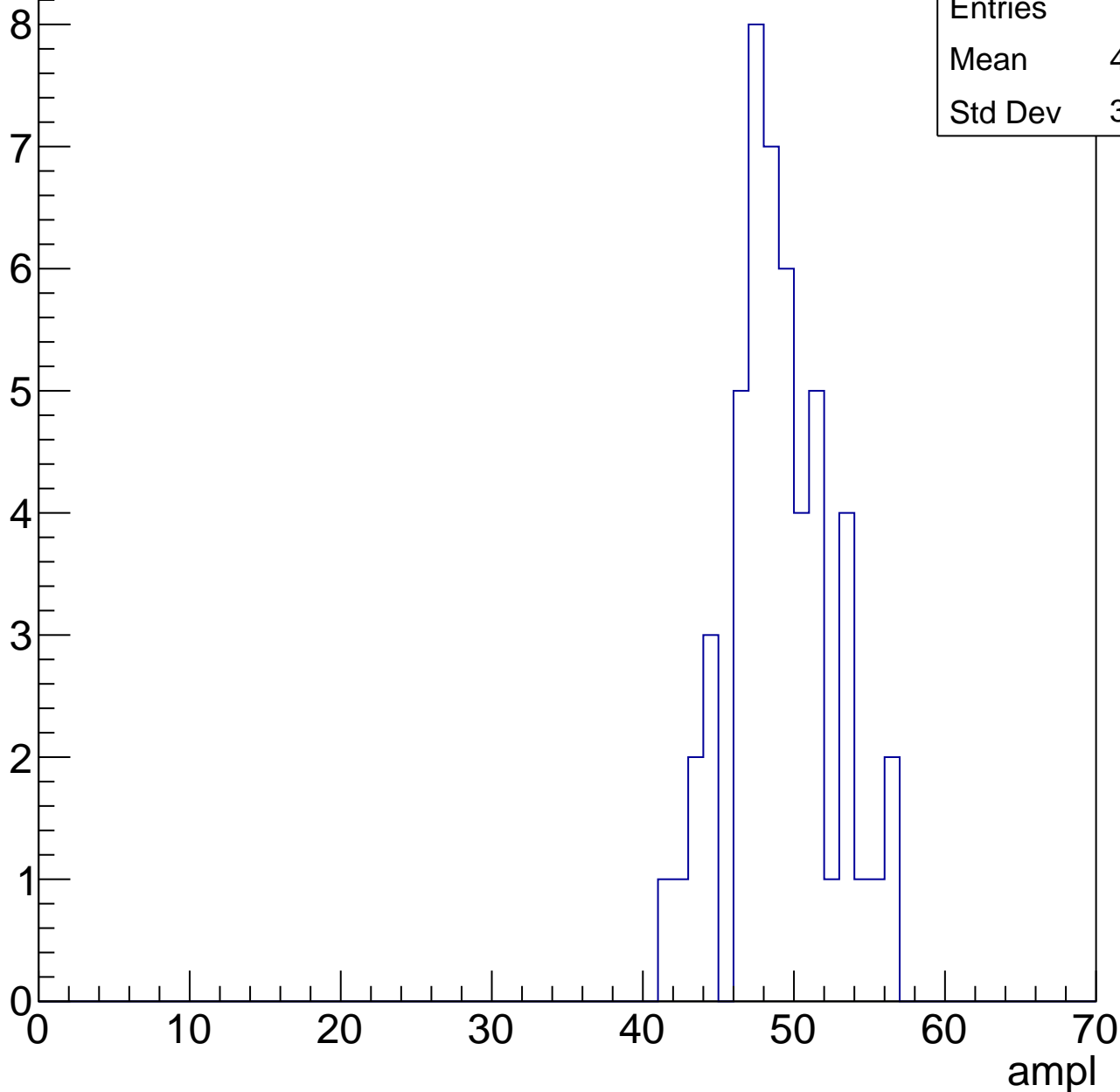


# B1L003S, U18-ch122, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	51
Mean	48.57
Std Dev	3.403

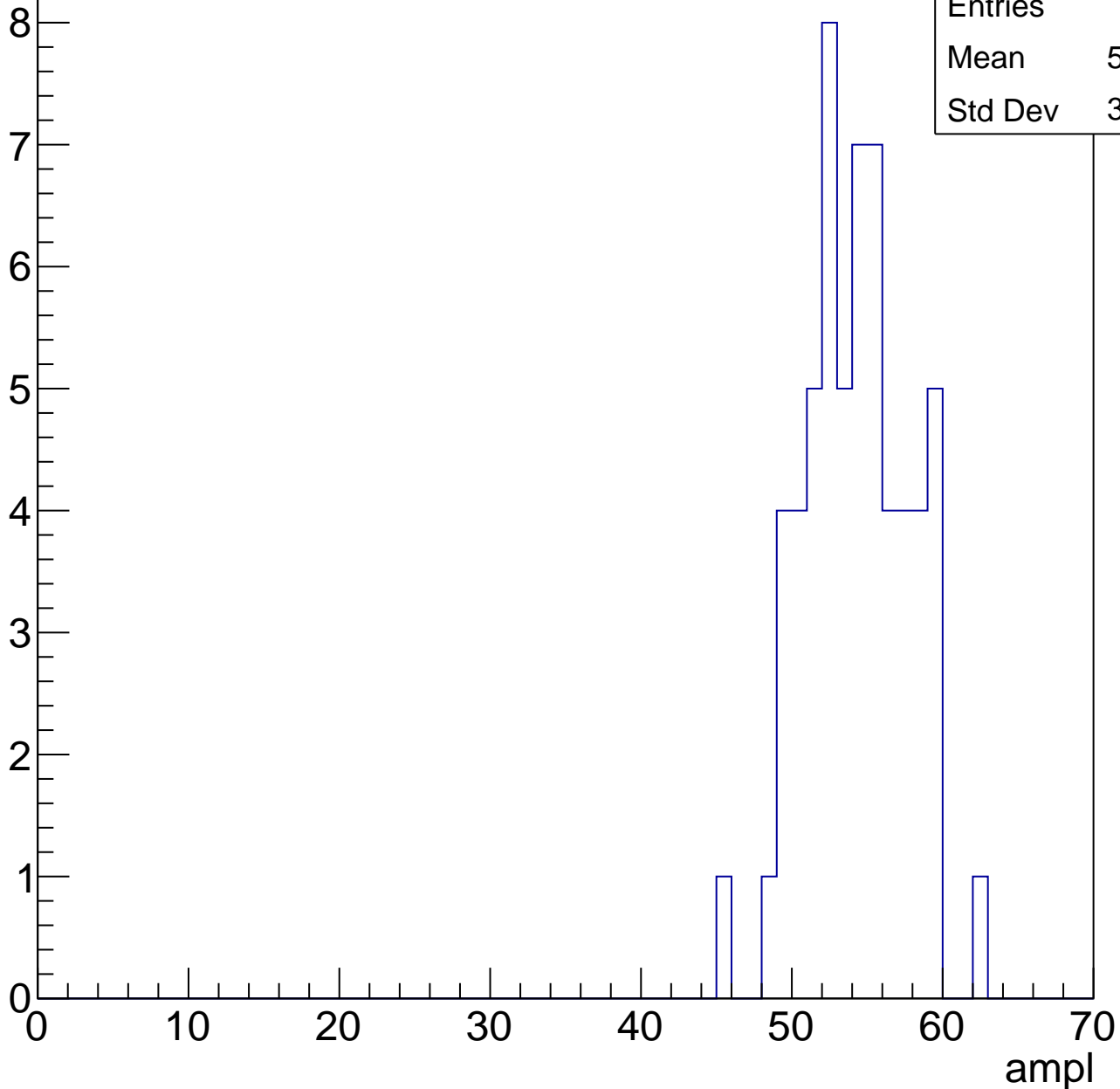


# B1L003S, U18-ch122, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	60
Mean	53.82
Std Dev	3.349

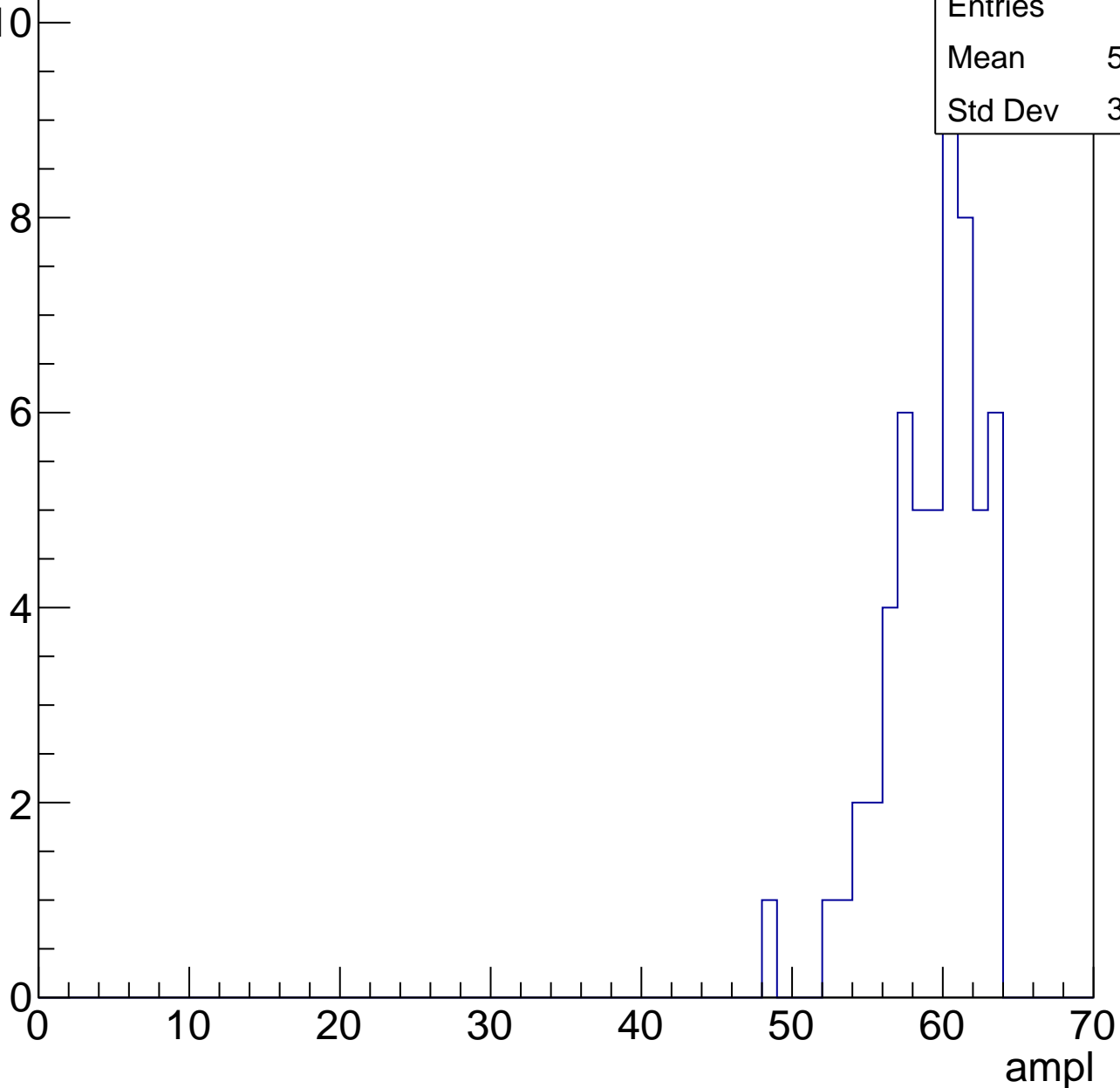


# B1L003S, U18-ch122, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

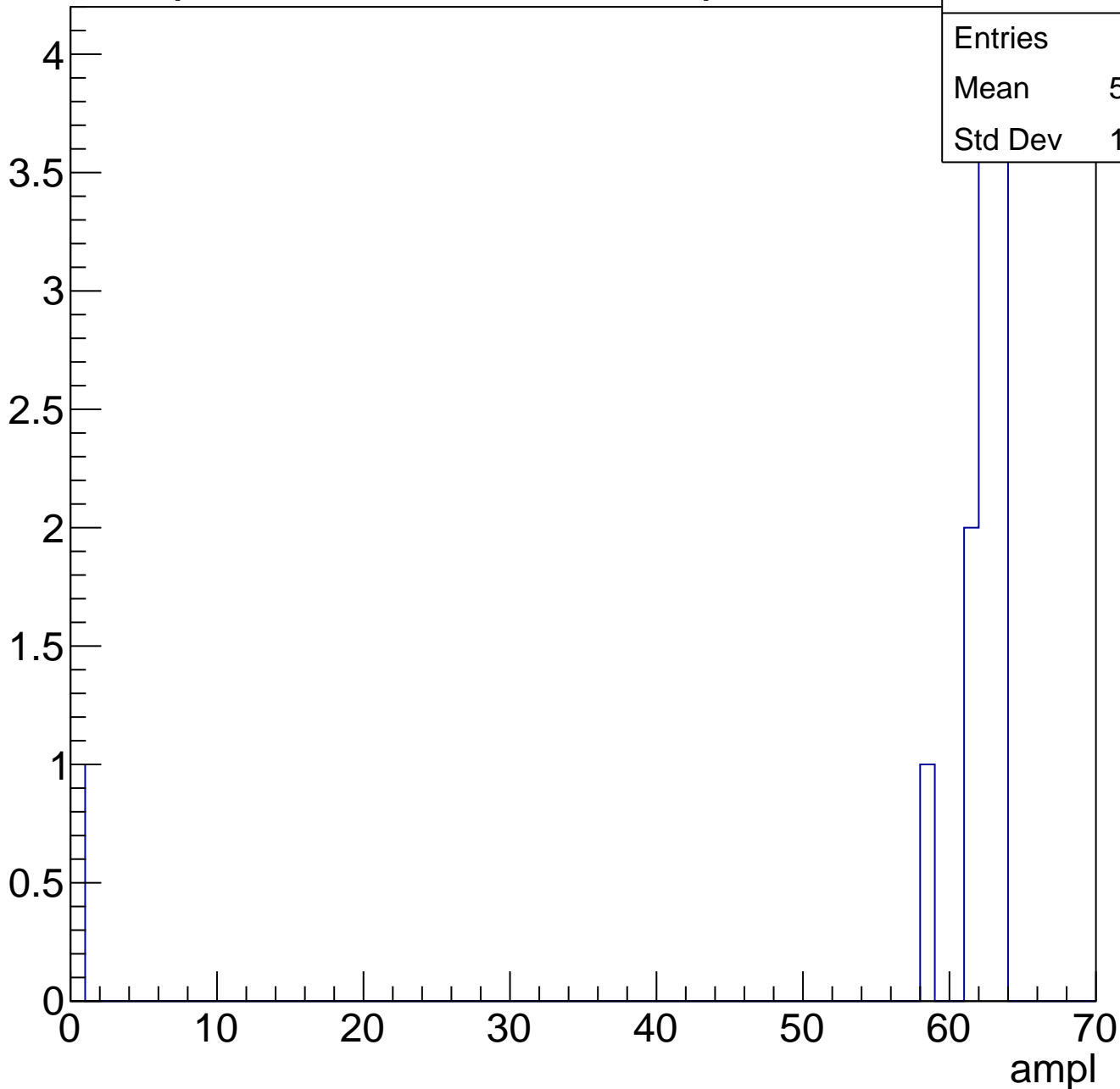
Entries	56
Mean	58.89
Std Dev	3.092



# B1L003S, U18-ch122, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U18-ch122, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U18-ch123, adc0

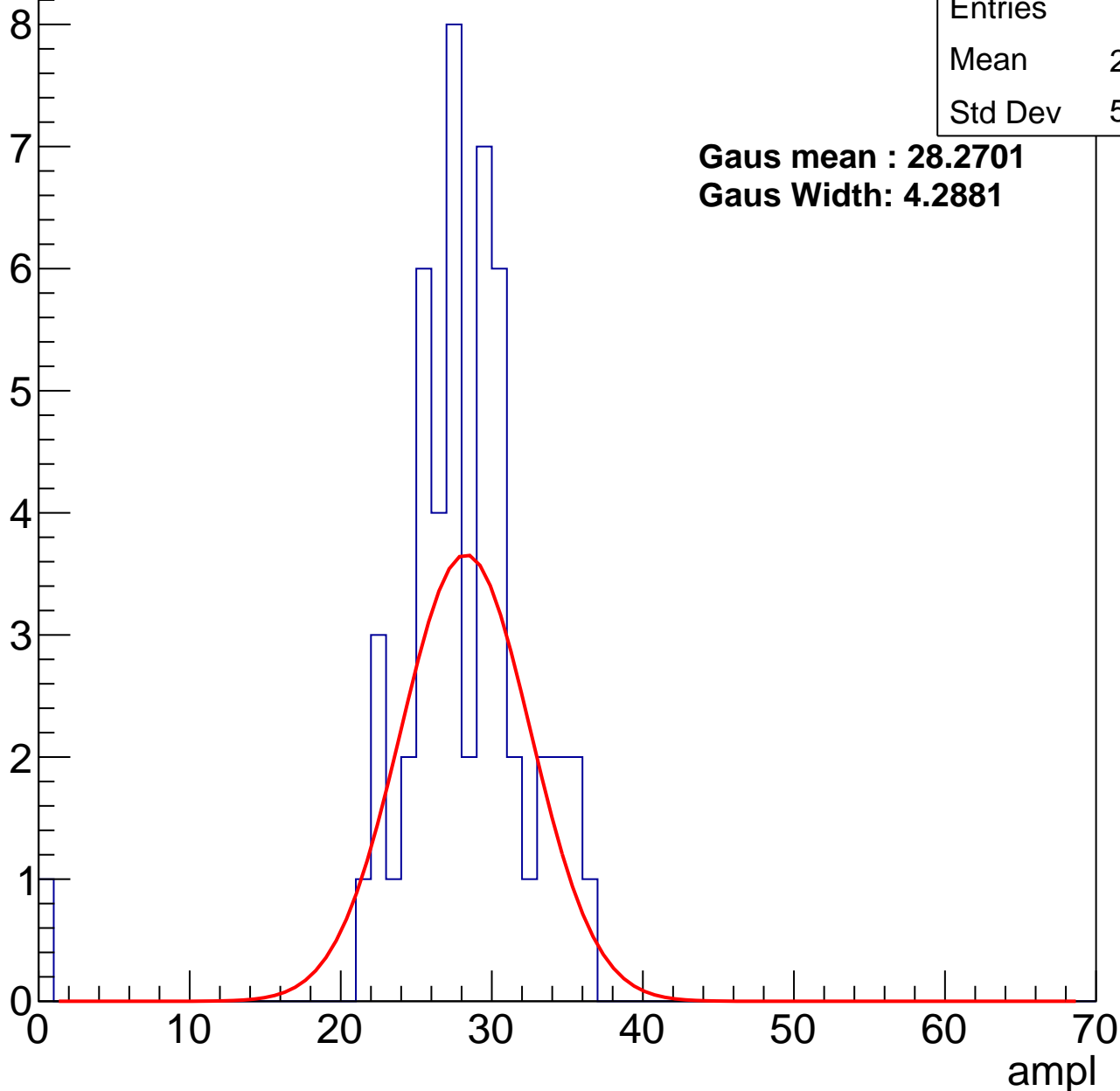
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	51
Mean	27.47
Std Dev	5.259

**Gaus mean : 28.2701**

**Gaus Width: 4.2881**



# B1L003S, U18-ch123, adc1

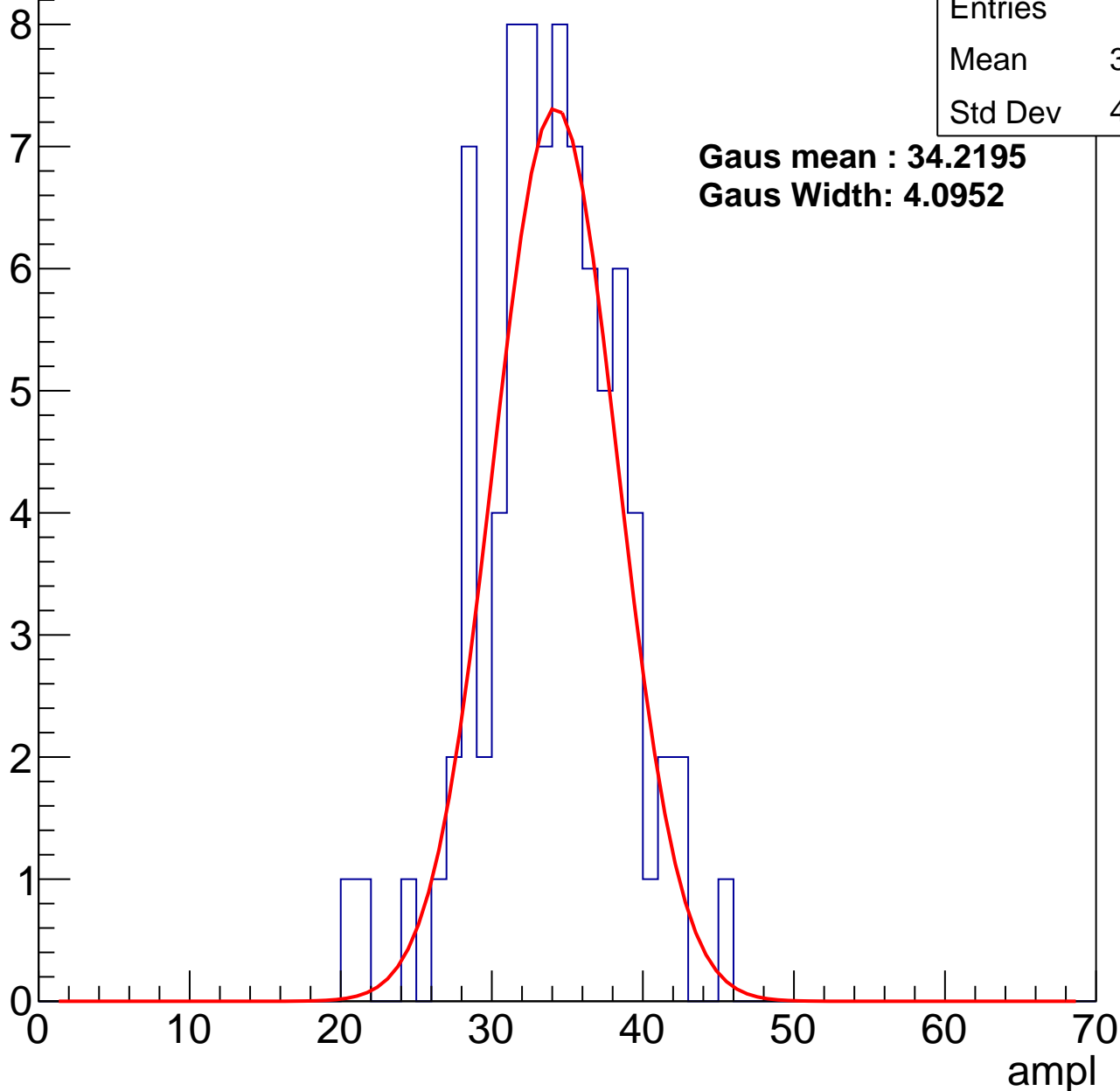
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	84
Mean	33.42
Std Dev	4.539

**Gaus mean : 34.2195**

**Gaus Width: 4.0952**



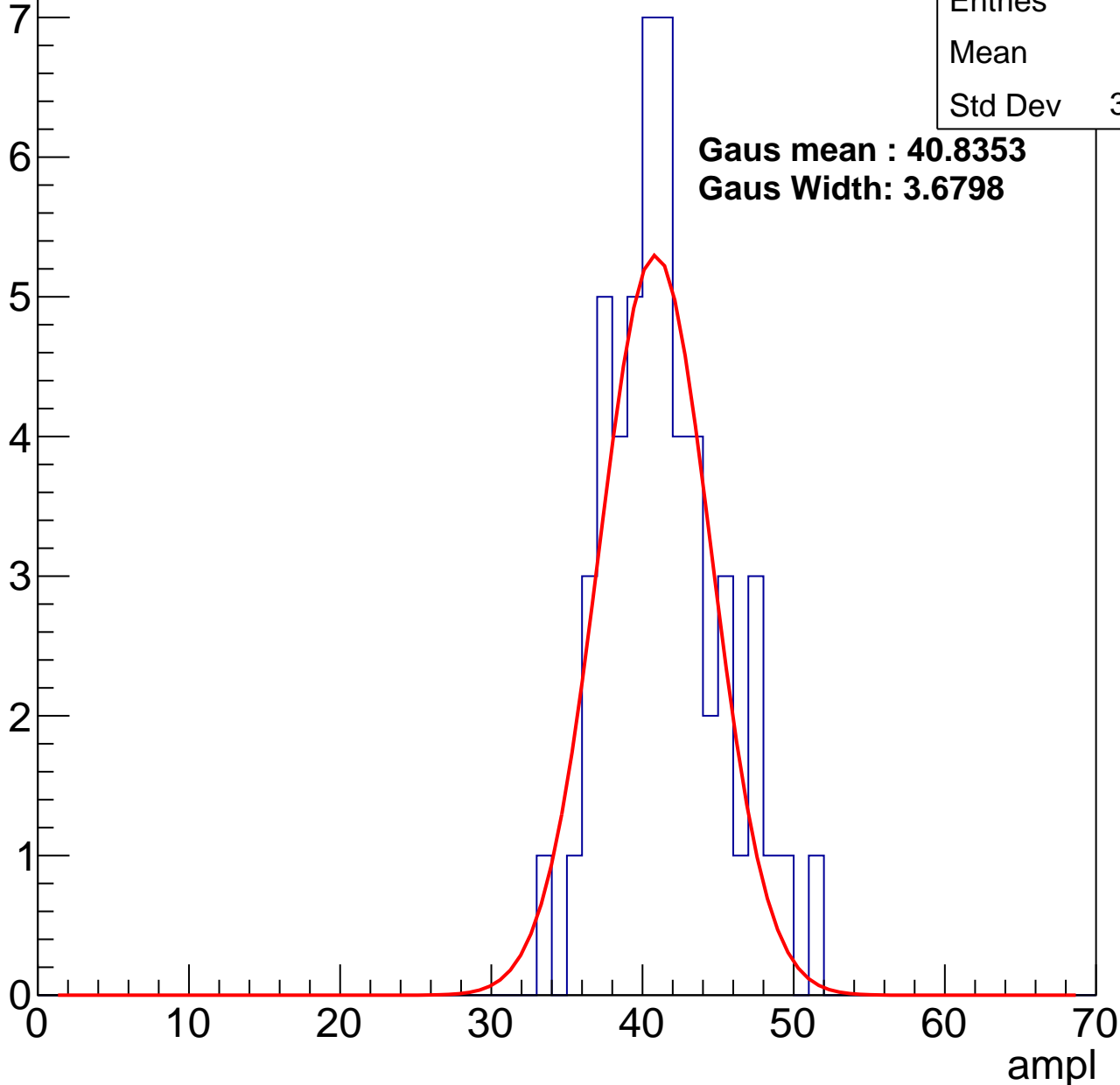
# B1L003S, U18-ch123, adc2

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	53
Mean	41
Std Dev	3.762

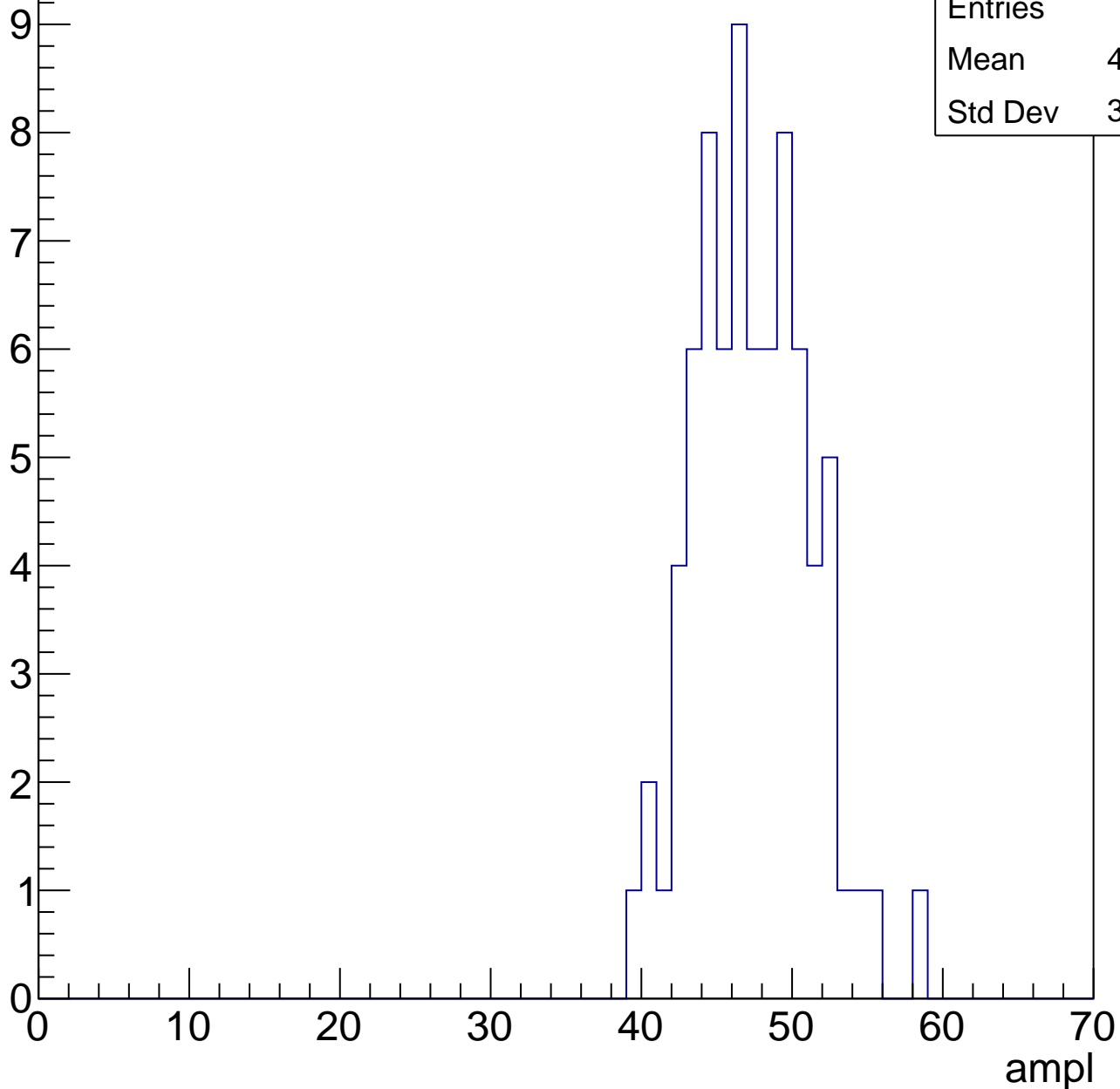
**Gaus mean : 40.8353**  
**Gaus Width: 3.6798**



# B1L003S, U18-ch123, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U18-ch123, adc4

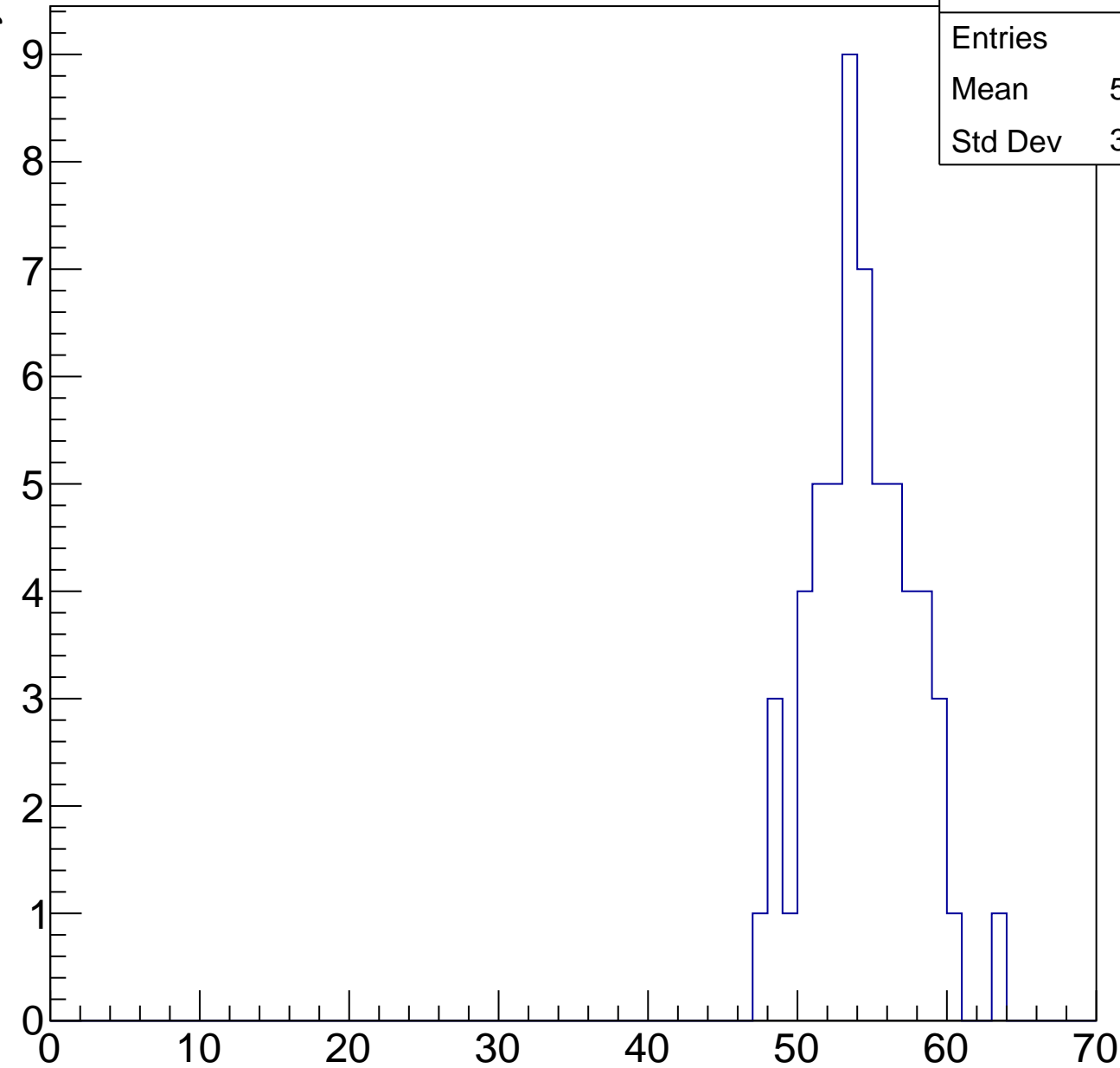
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	58
Mean	53.88
Std Dev	3.312

ampl

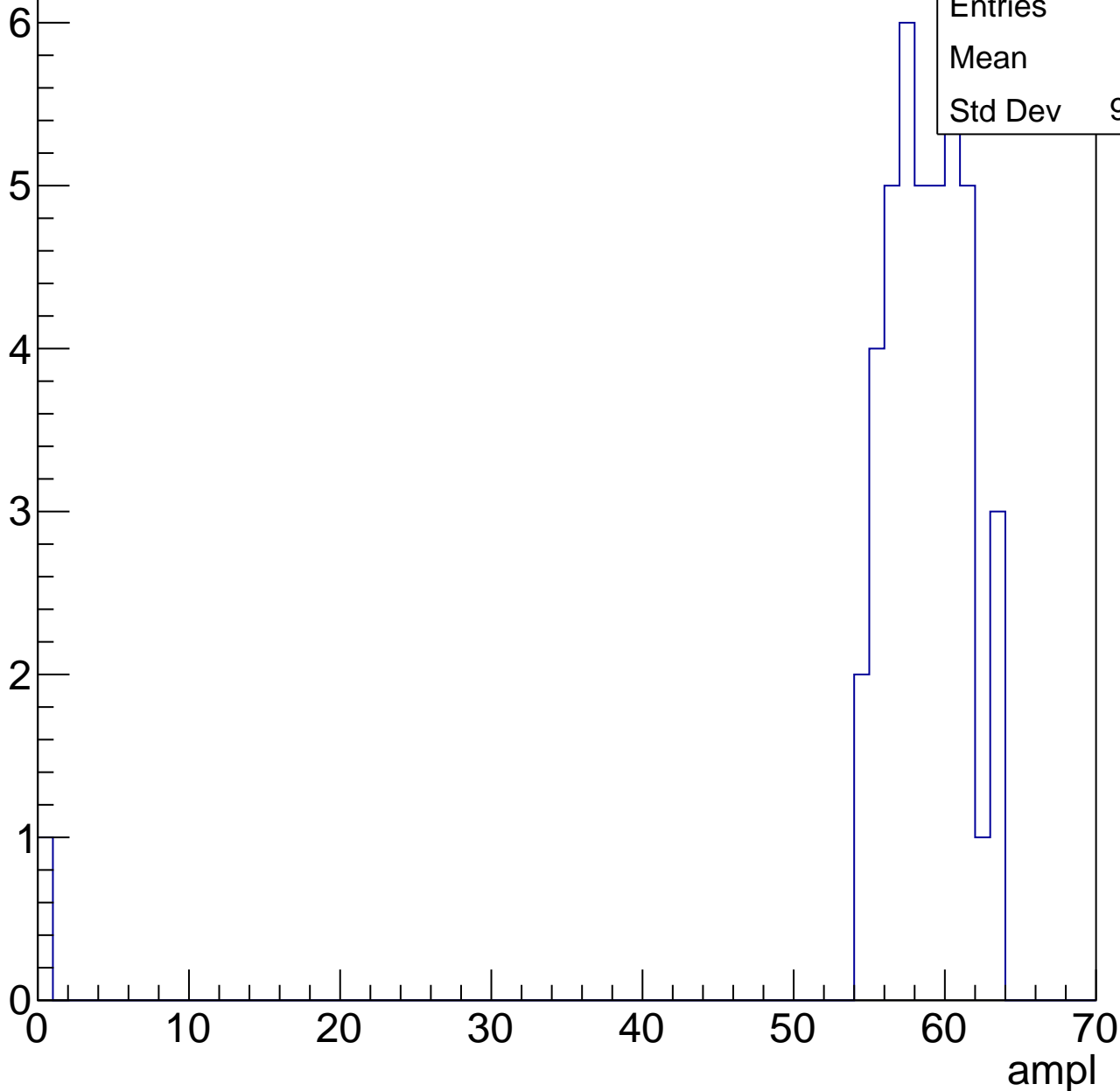


# B1L003S, U18-ch123, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	43
Mean	57
Std Dev	9.124

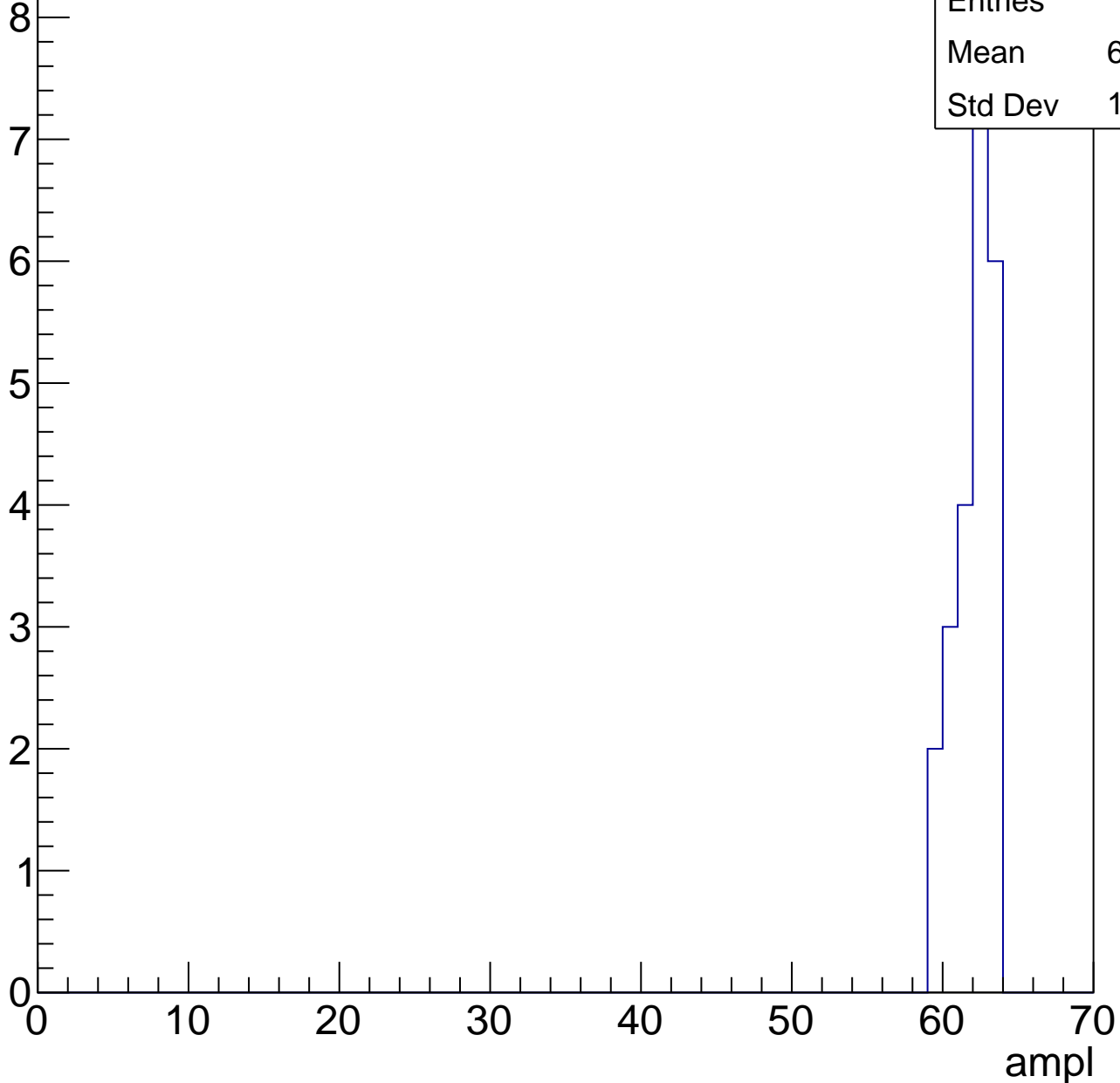


# B1L003S, U18-ch123, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	23
Mean	61.57
Std Dev	1.245

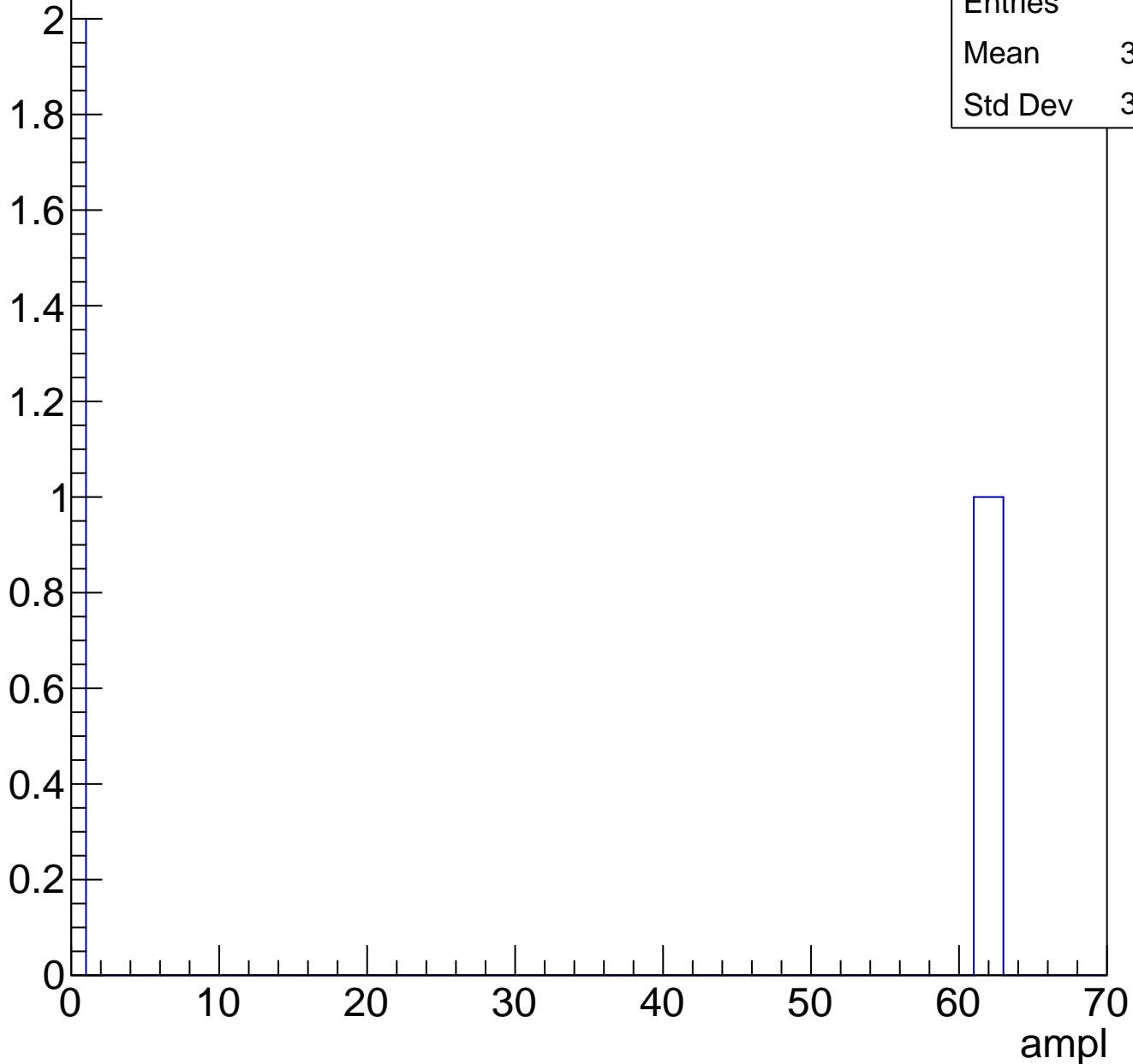




# B1L003S, U18-ch123, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



# B1L003S, U18-ch124, adc0

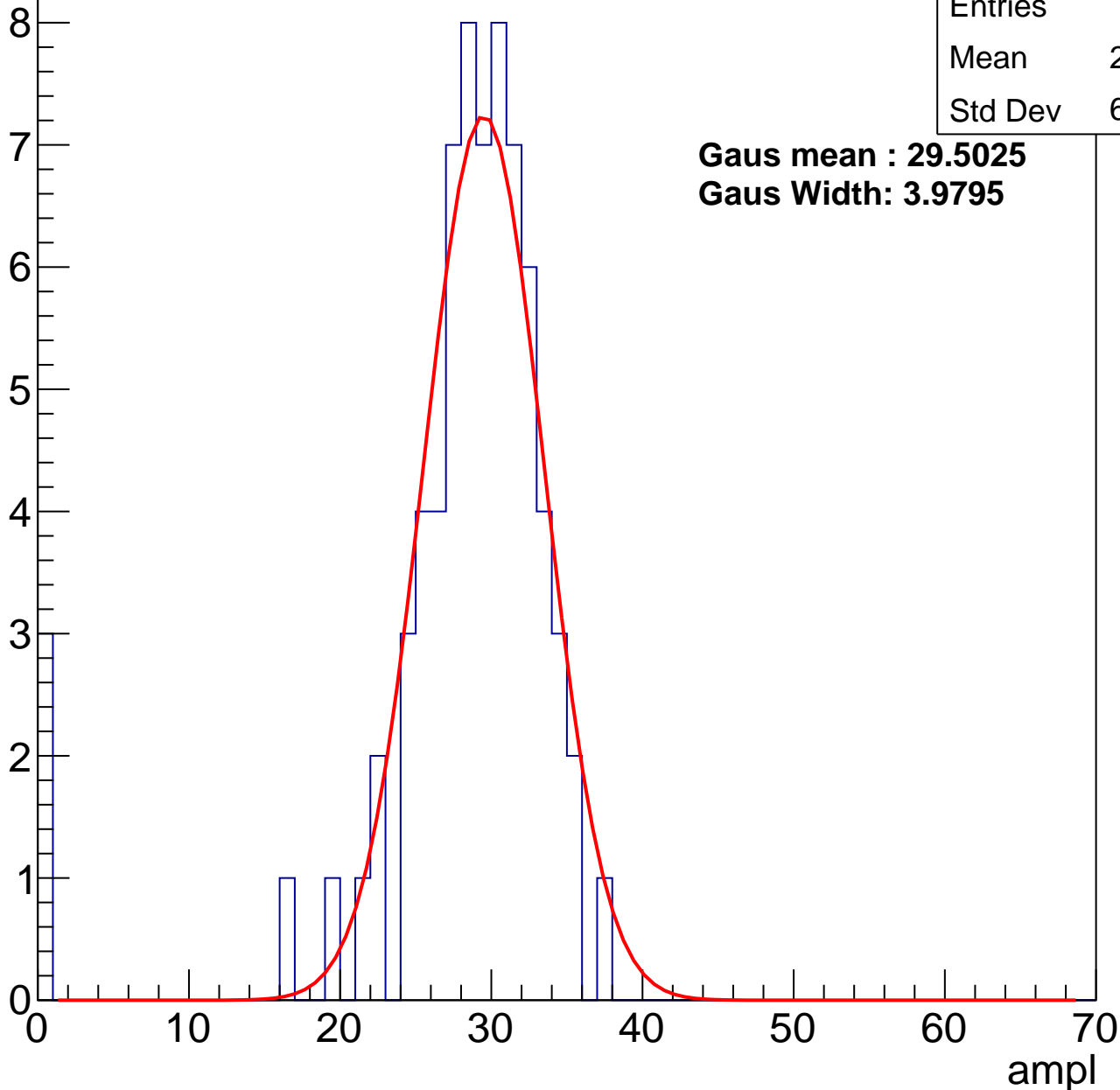
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	72
Mean	27.53
Std Dev	6.845

**Gaus mean : 29.5025**

**Gaus Width: 3.9795**



# B1L003S, U18-ch124, adc1

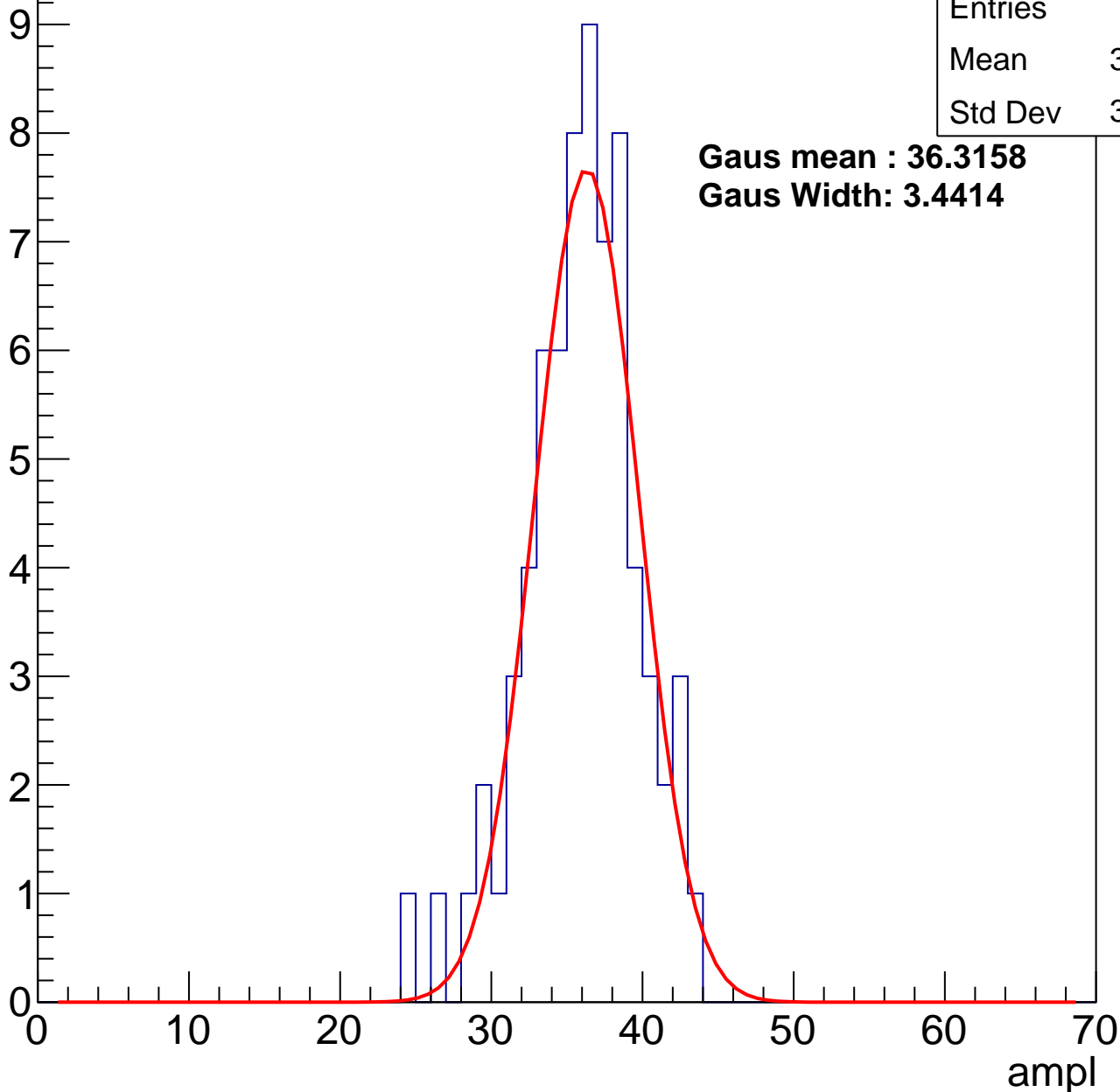
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	70
Mean	35.47
Std Dev	3.737

**Gaus mean : 36.3158**

**Gaus Width: 3.4414**



# B1L003S, U18-ch124, adc2

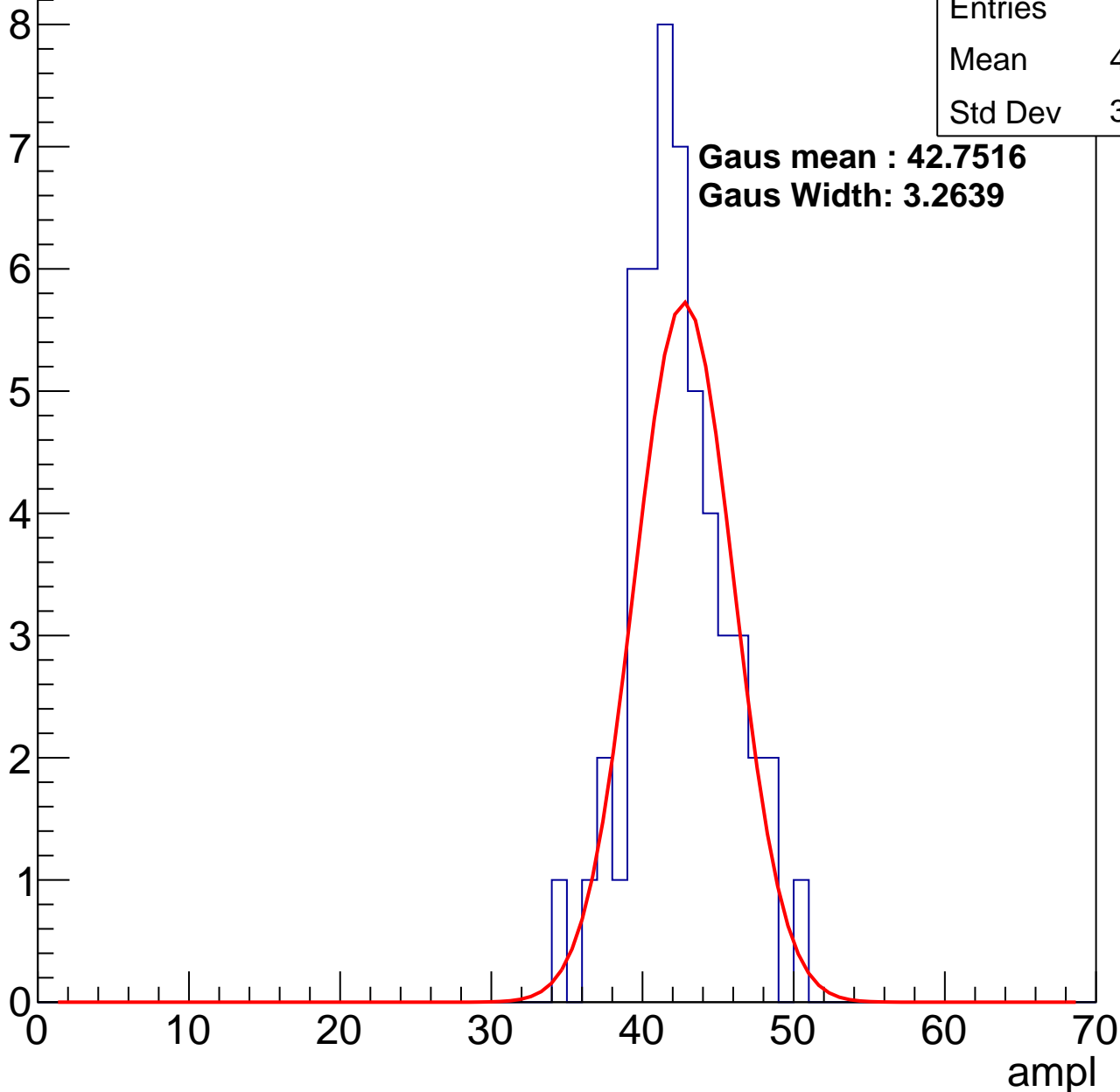
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	52
Mean	41.96
Std Dev	3.204

**Gaus mean : 42.7516**

**Gaus Width: 3.2639**

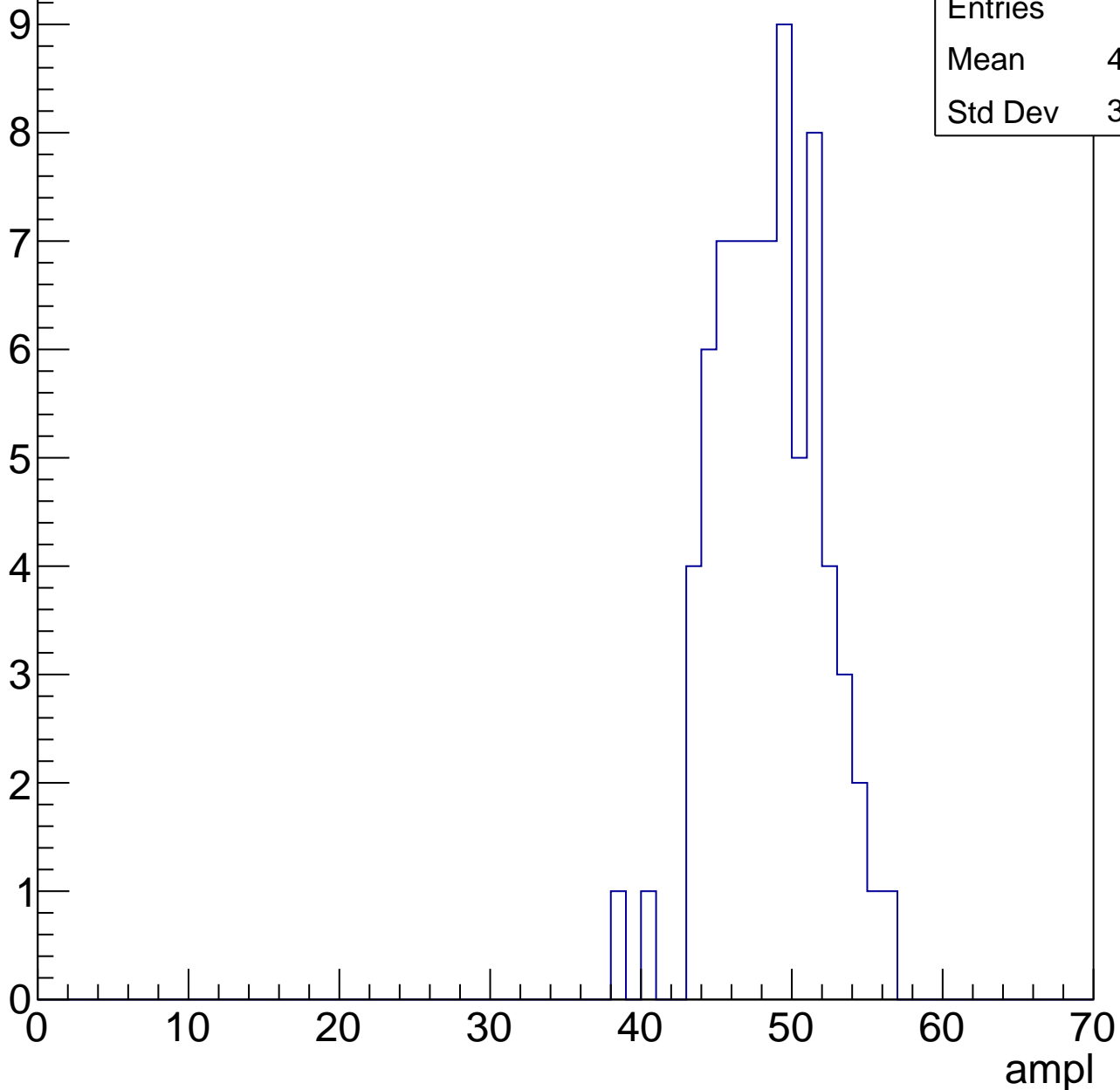


# B1L003S, U18-ch124, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

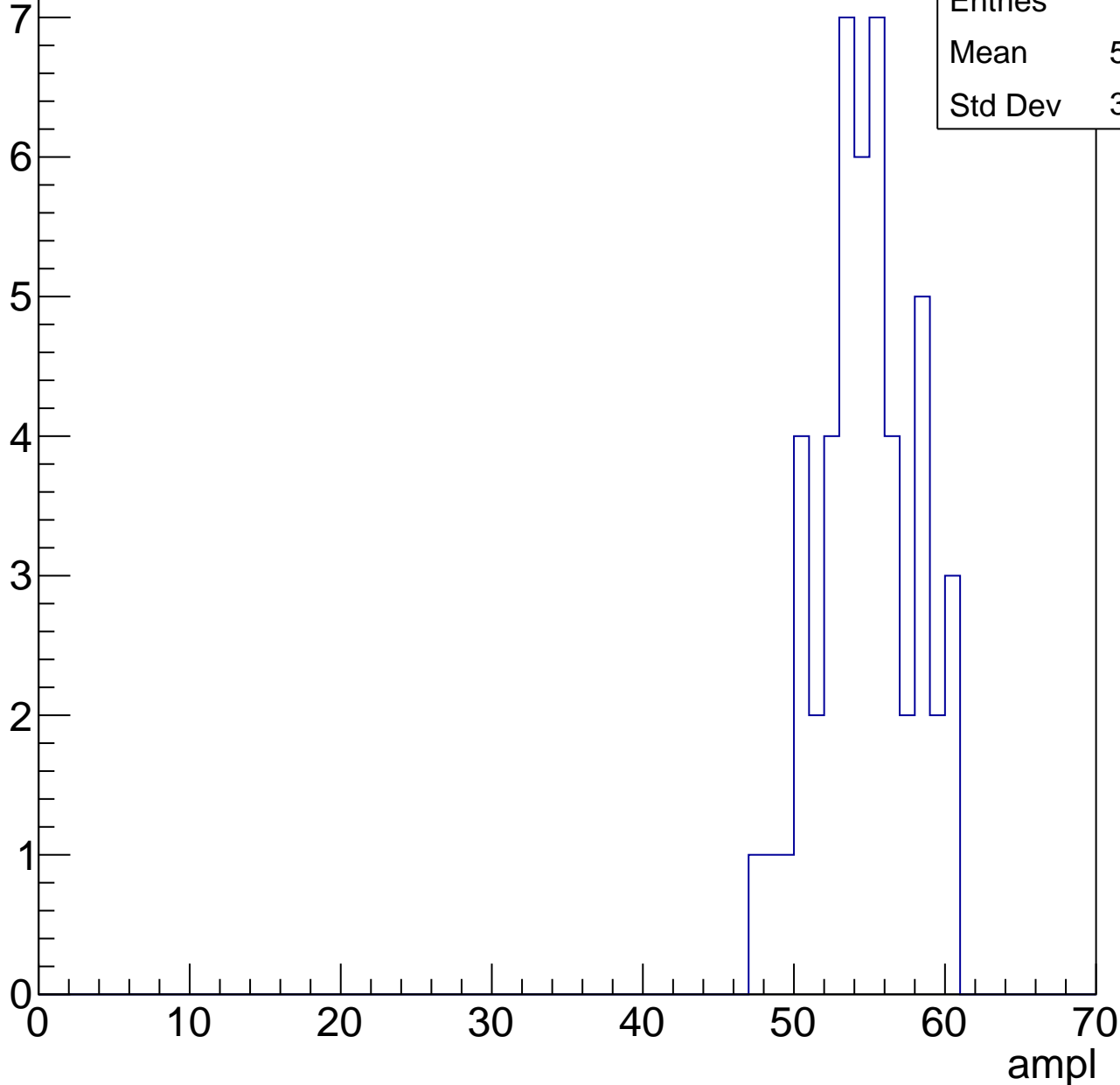
Entries	73
Mean	47.96
Std Dev	3.478



# B1L003S, U18-ch124, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



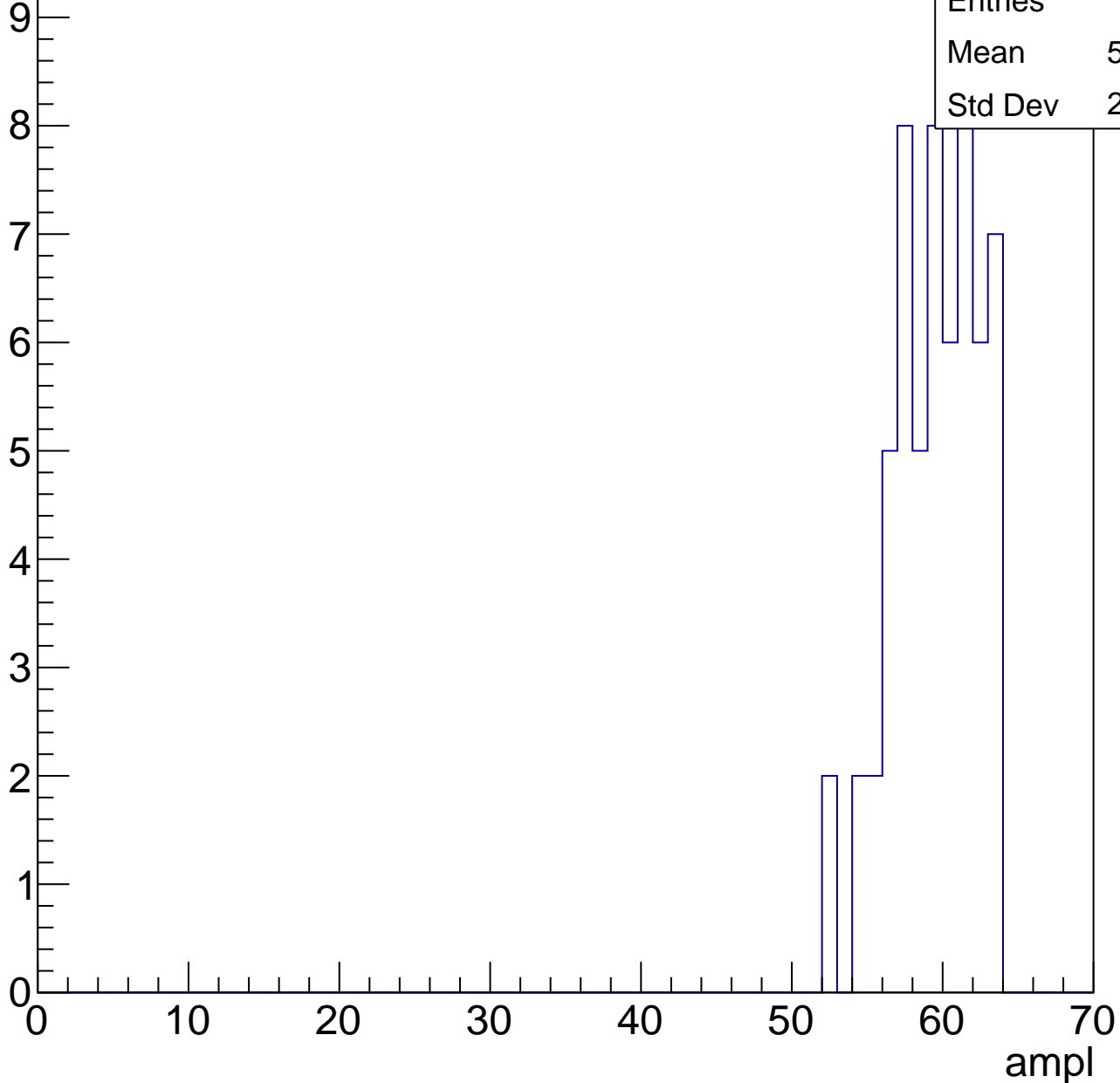
Entries	49
Mean	54.29
Std Dev	3.162

# B1L003S, U18-ch124, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

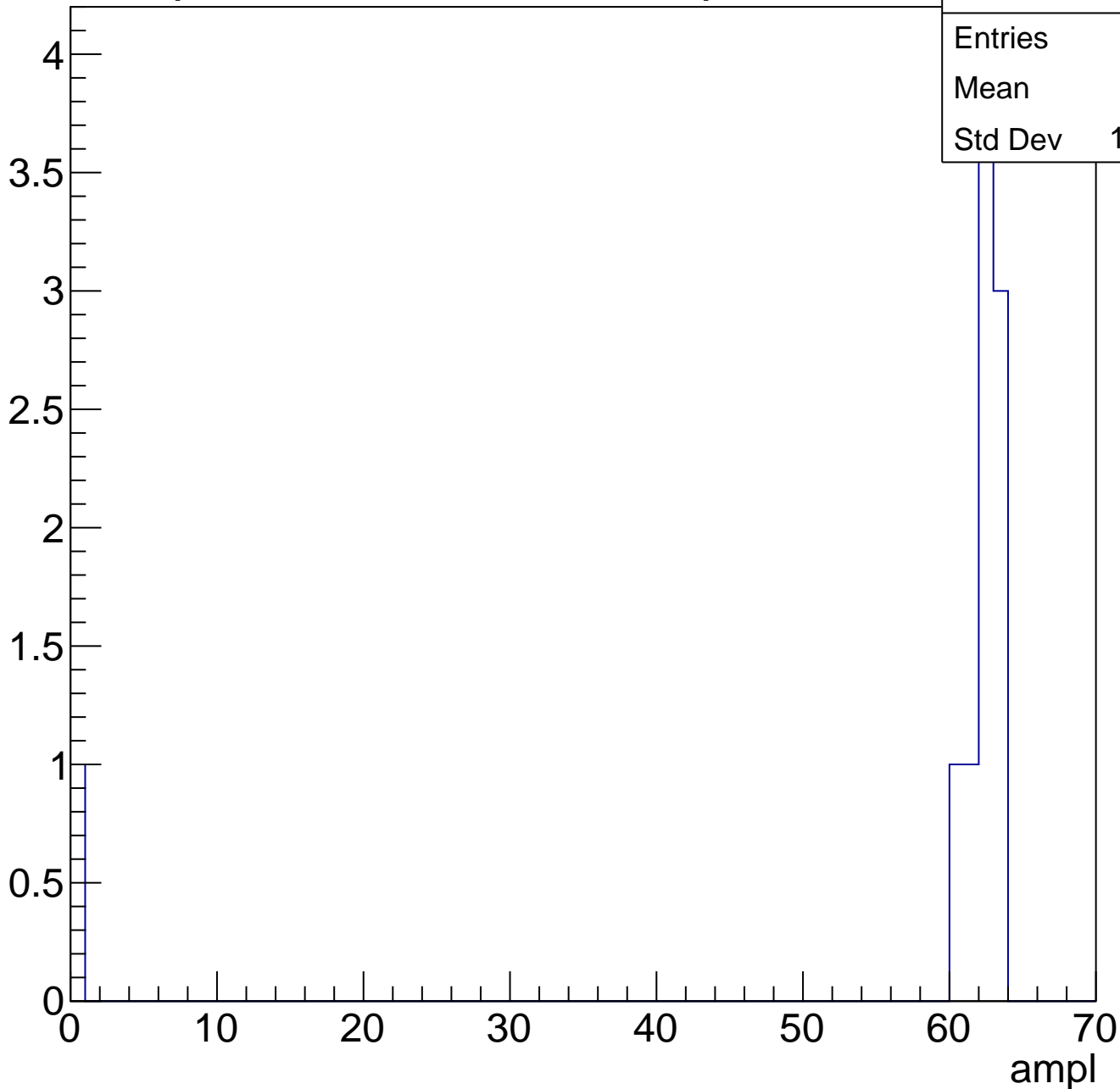
Entries	60
Mean	59.03
Std Dev	2.799



# B1L003S, U18-ch124, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry





# B1L003S, U18-ch124, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L003S, U18-ch125, adc0

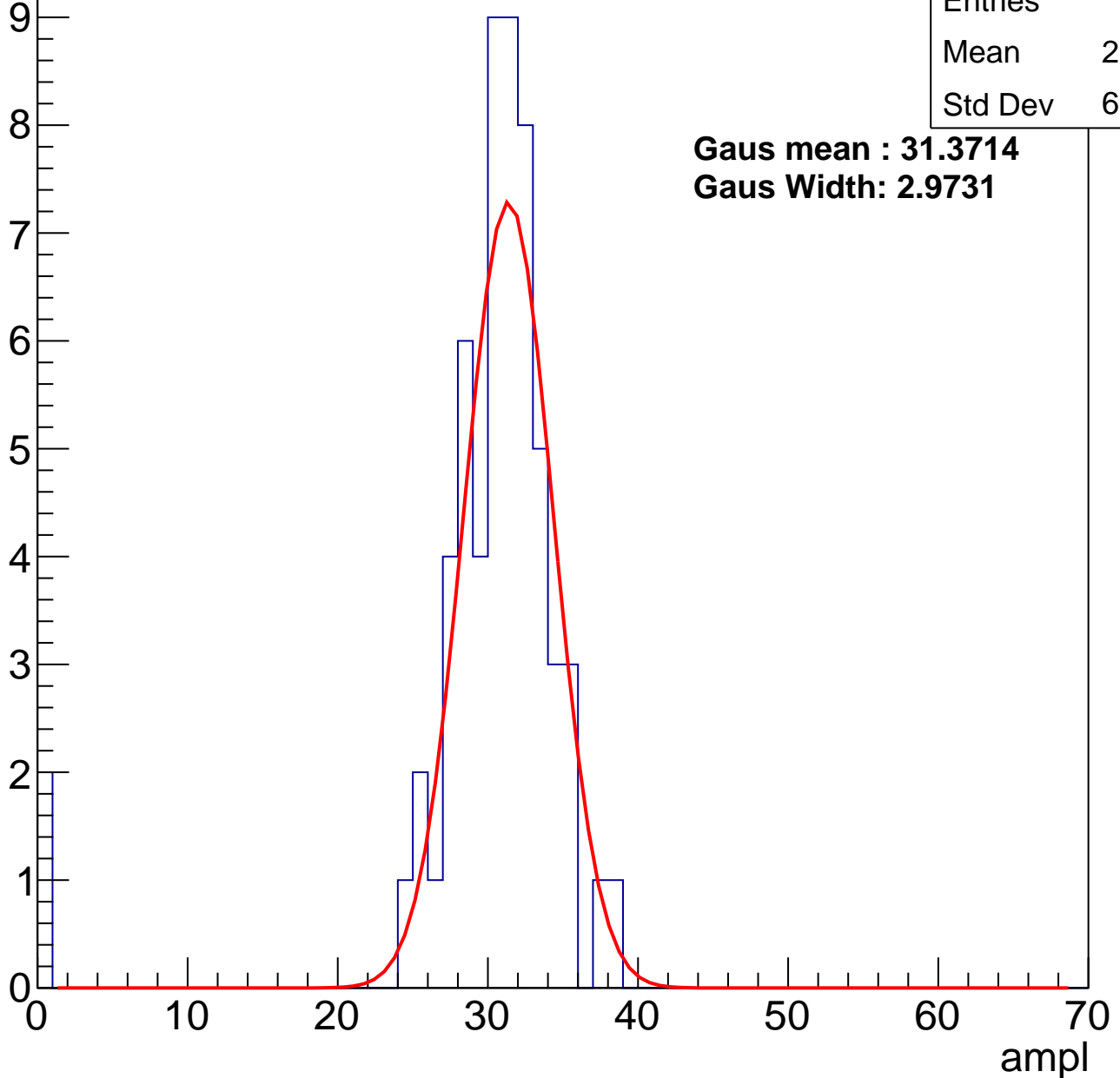
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	59
Mean	29.56
Std Dev	6.212

**Gaus mean : 31.3714**

**Gaus Width: 2.9731**



# B1L003S, U18-ch125, adc1

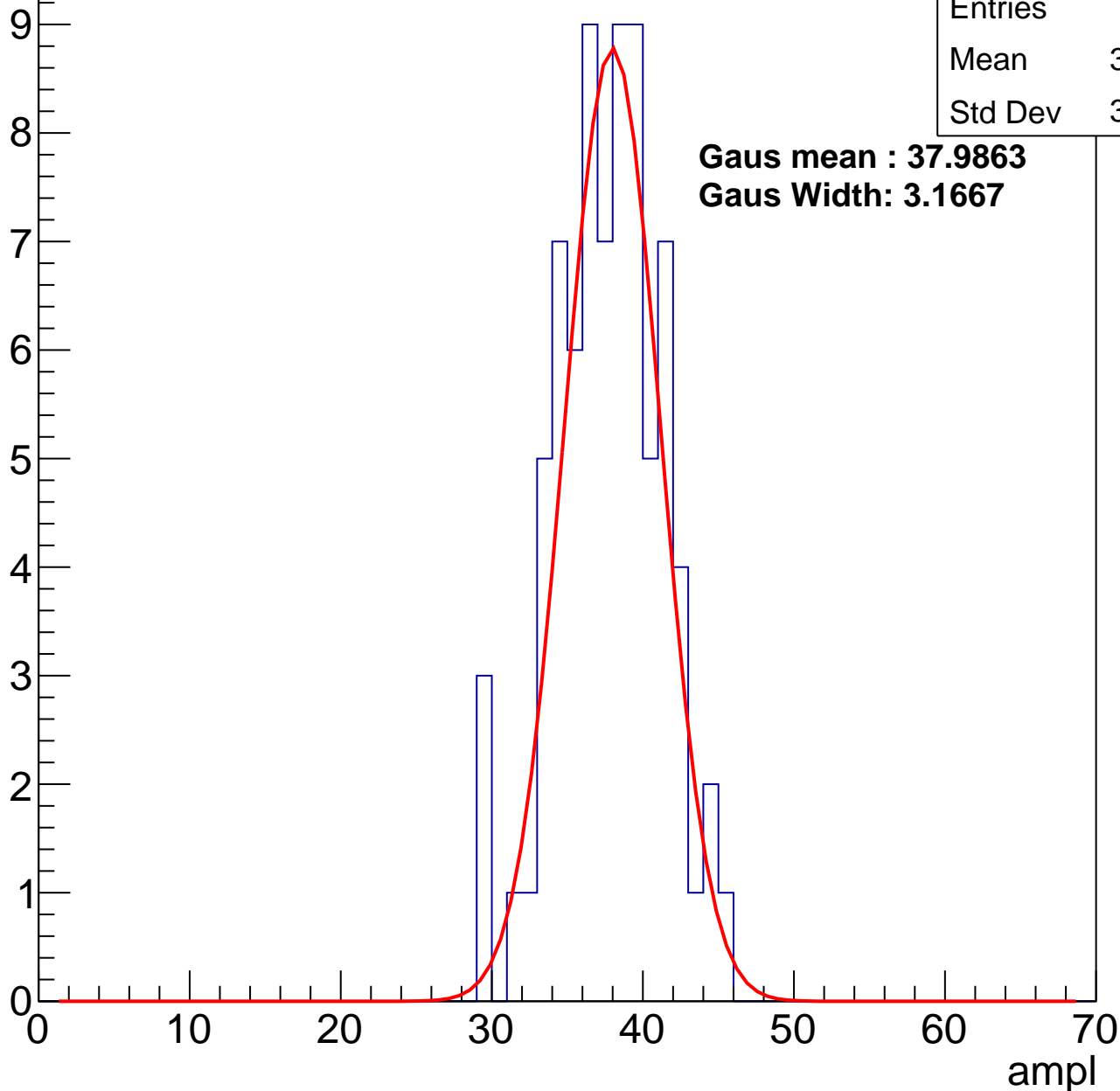
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	77
Mean	37.27
Std Dev	3.463

**Gaus mean : 37.9863**

**Gaus Width: 3.1667**



# B1L003S, U18-ch125, adc2

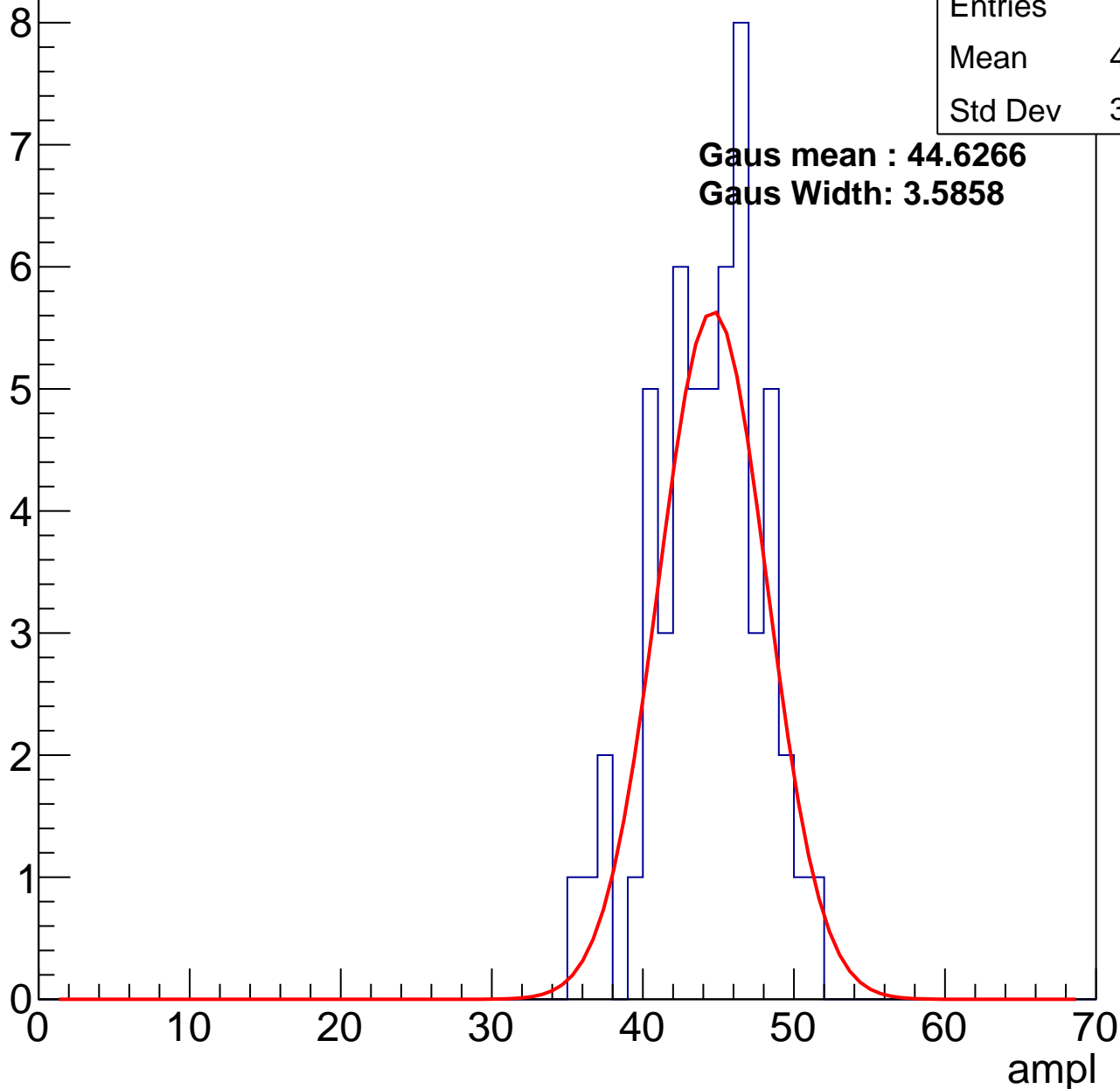
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	55
Mean	43.85
Std Dev	3.524

**Gaus mean : 44.6266**

**Gaus Width: 3.5858**

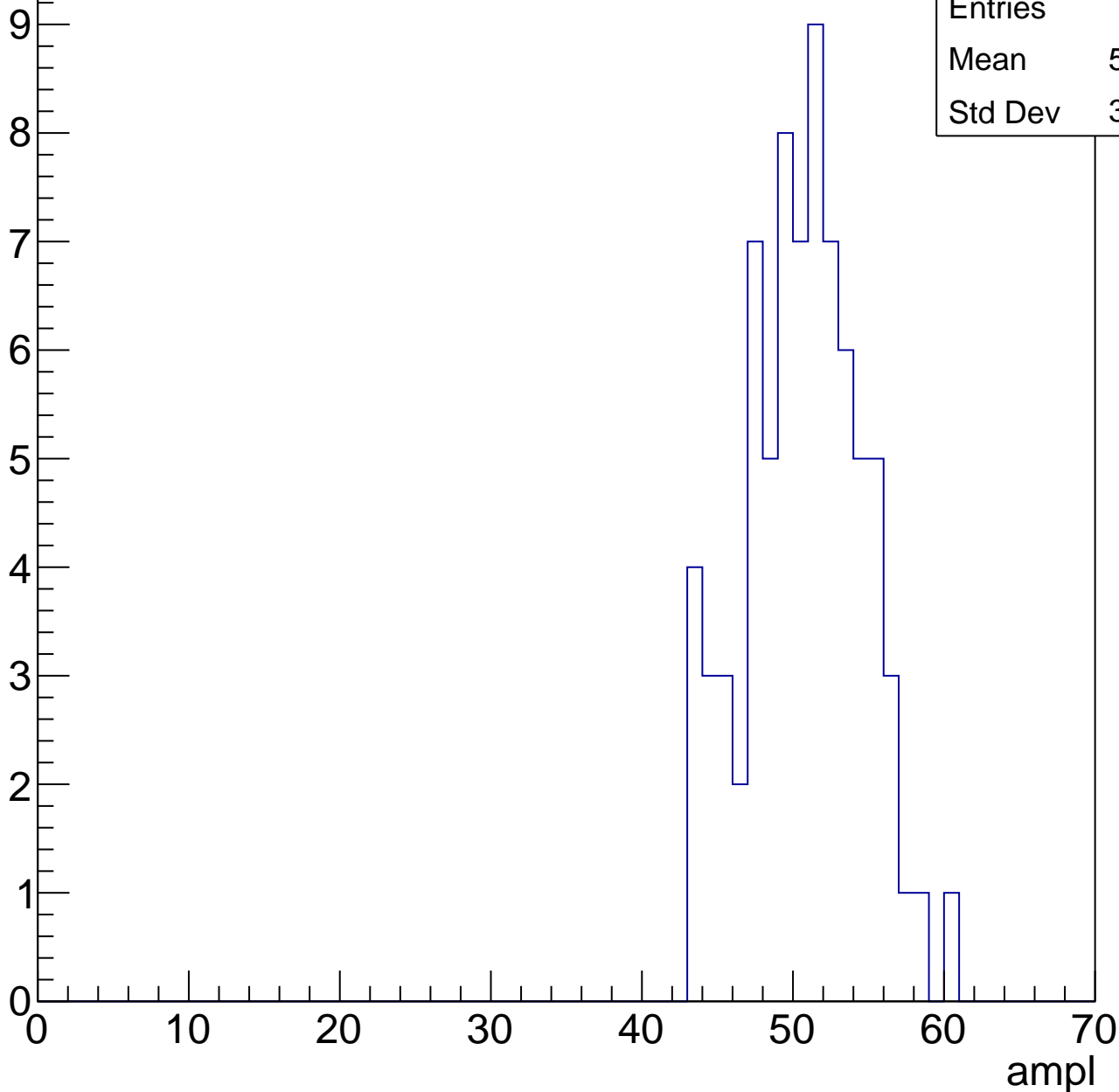


# B1L003S, U18-ch125, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	77
Mean	50.27
Std Dev	3.802

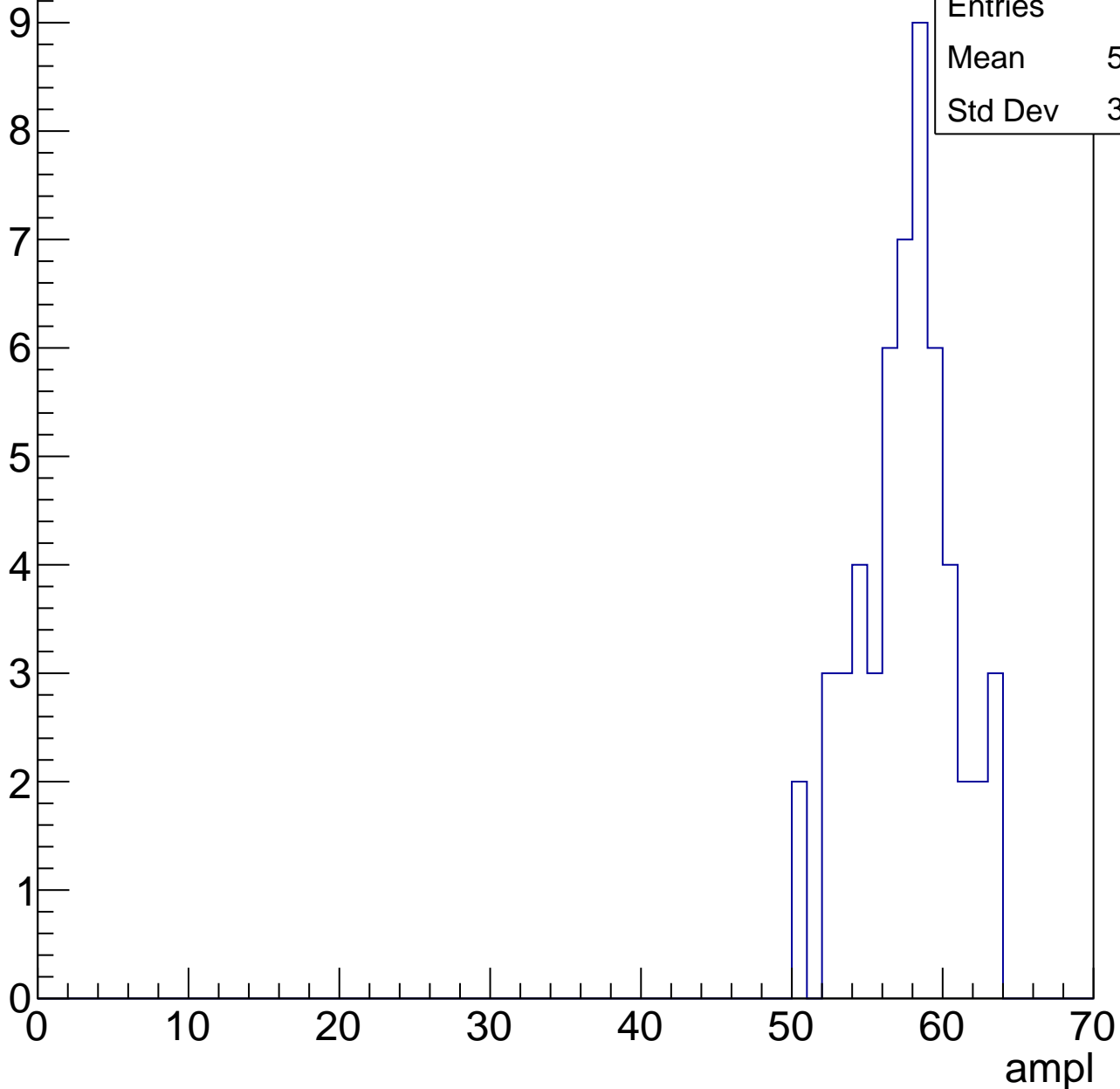


# B1L003S, U18-ch125, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	54
Mean	57.07
Std Dev	3.144

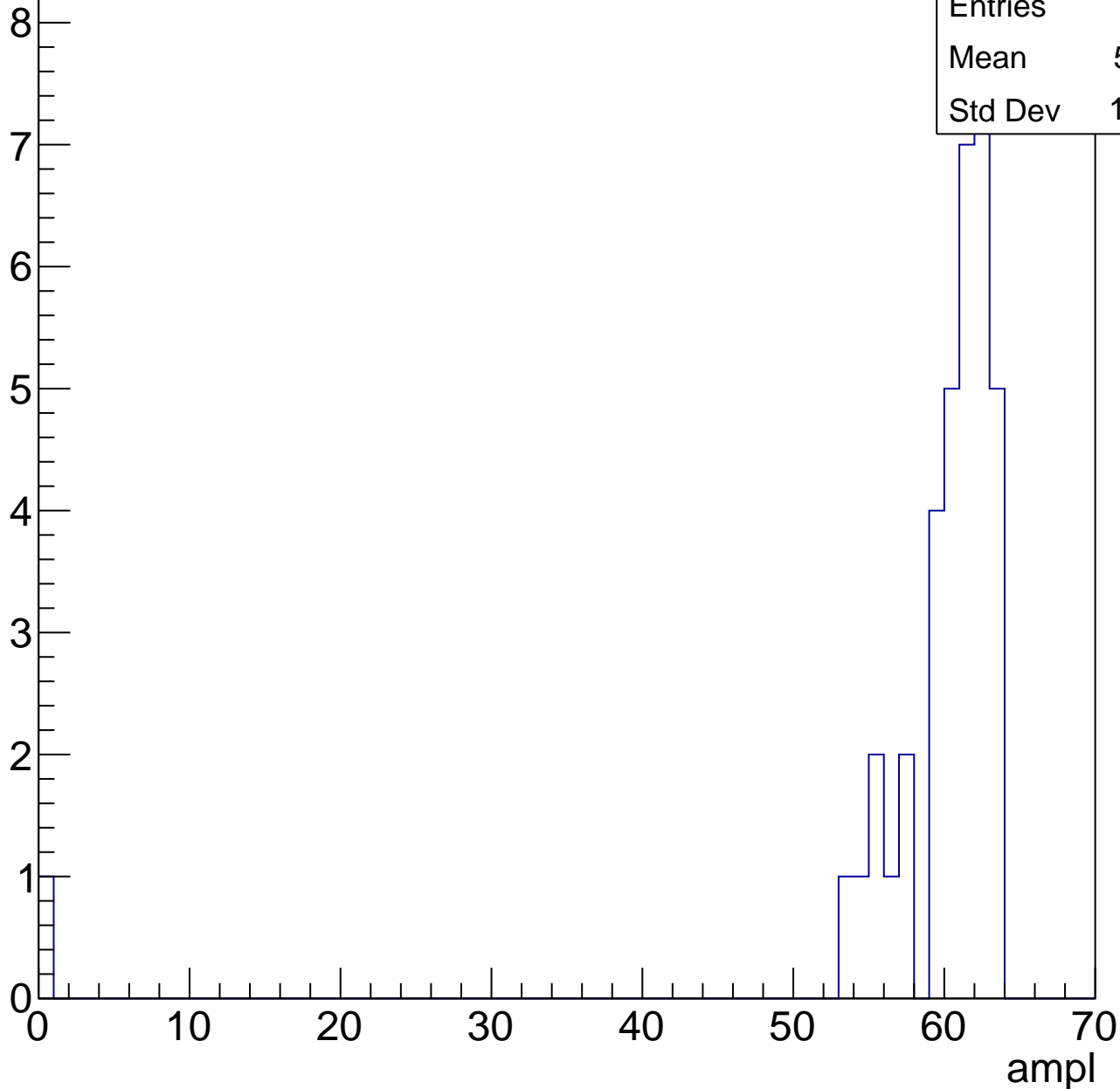


# B1L003S, U18-ch125, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	37
Mean	58.41
Std Dev	10.08



# B1L003S, U18-ch125, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	3
Mean	62.33
Std Dev	0.9428

0 10 20 30 40 50 60 70

ampl





# B1L003S, U18-ch125, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L003S, U18-ch126, adc0

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entries	80
Mean	27.93
Std Dev	7.271

**Gaus mean : 30.0476**

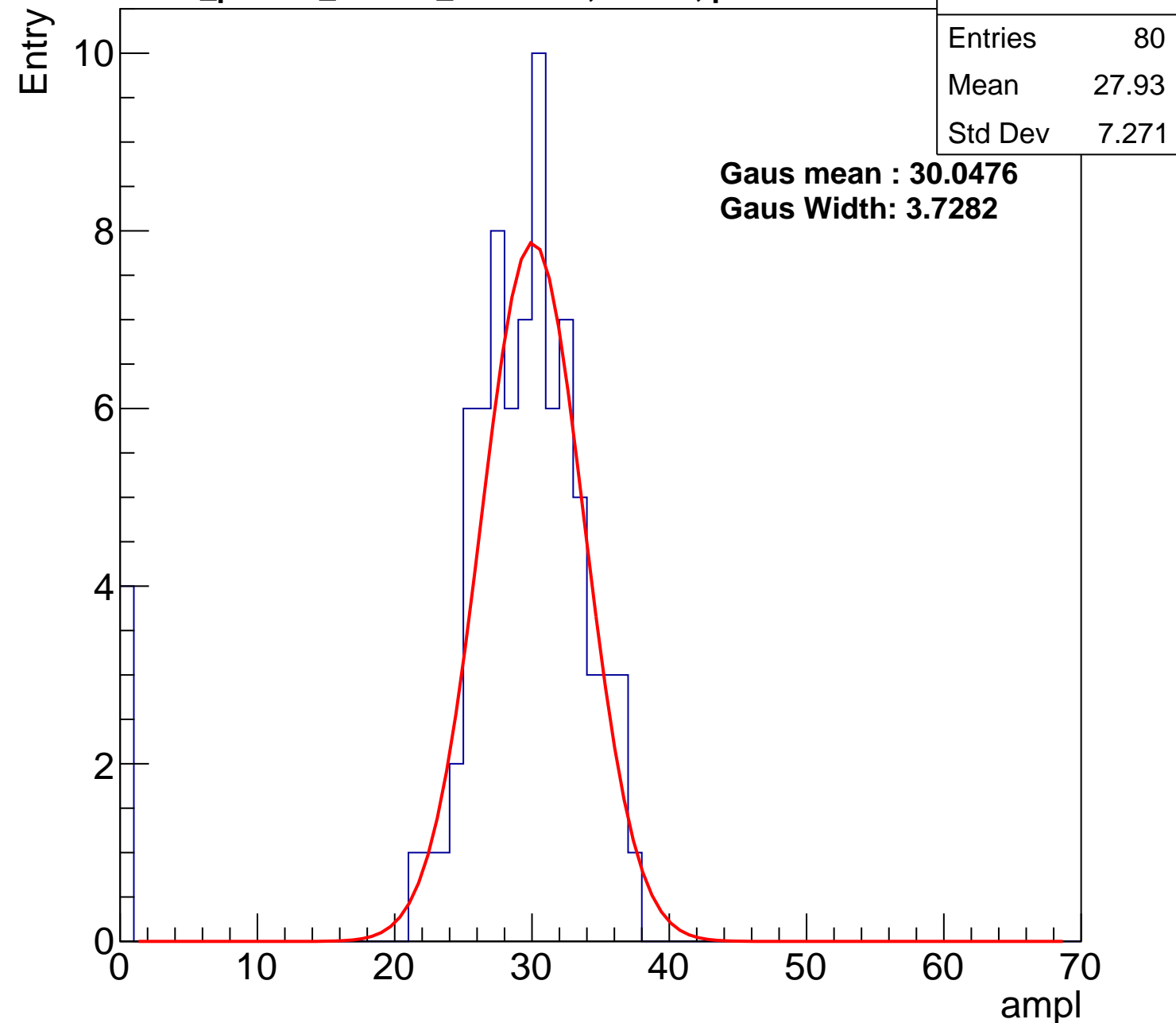
**Gaus Width: 3.7282**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L003S, U18-ch126, adc1

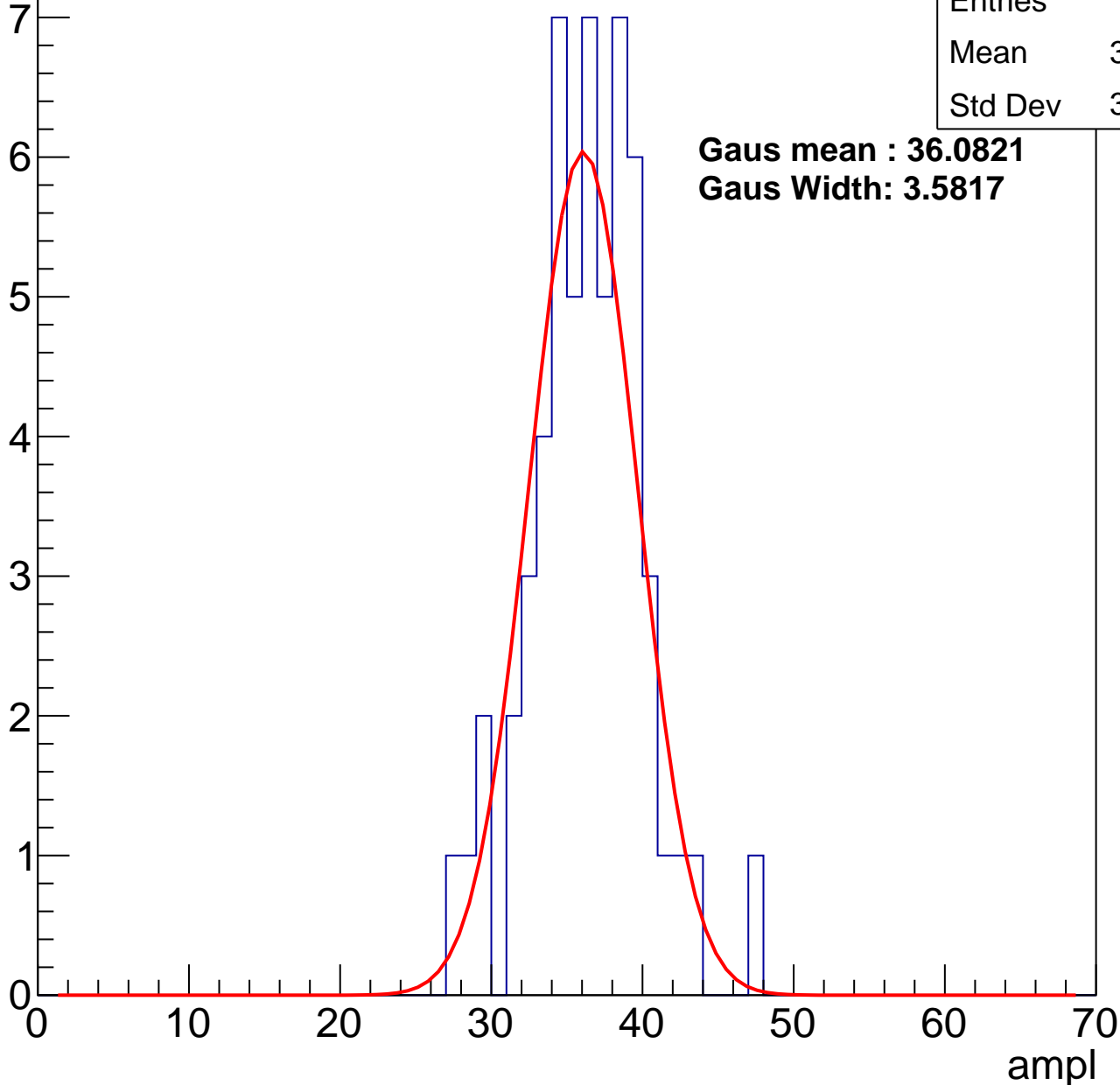
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	57
Mean	35.89
Std Dev	3.688

**Gaus mean : 36.0821**

**Gaus Width: 3.5817**



# B1L003S, U18-ch126, adc2

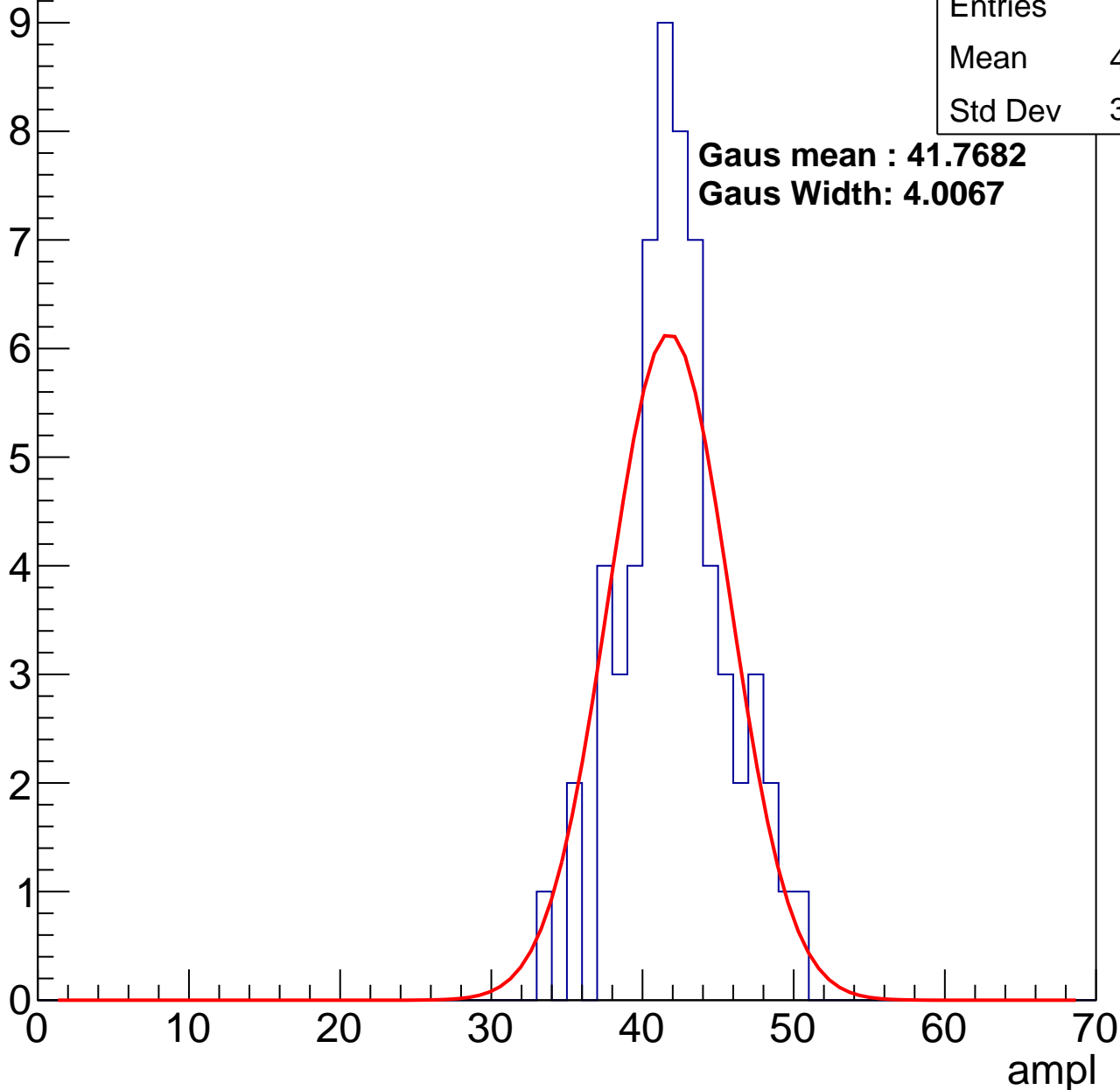
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	61
Mean	41.74
Std Dev	3.478

**Gaus mean : 41.7682**

**Gaus Width: 4.0067**

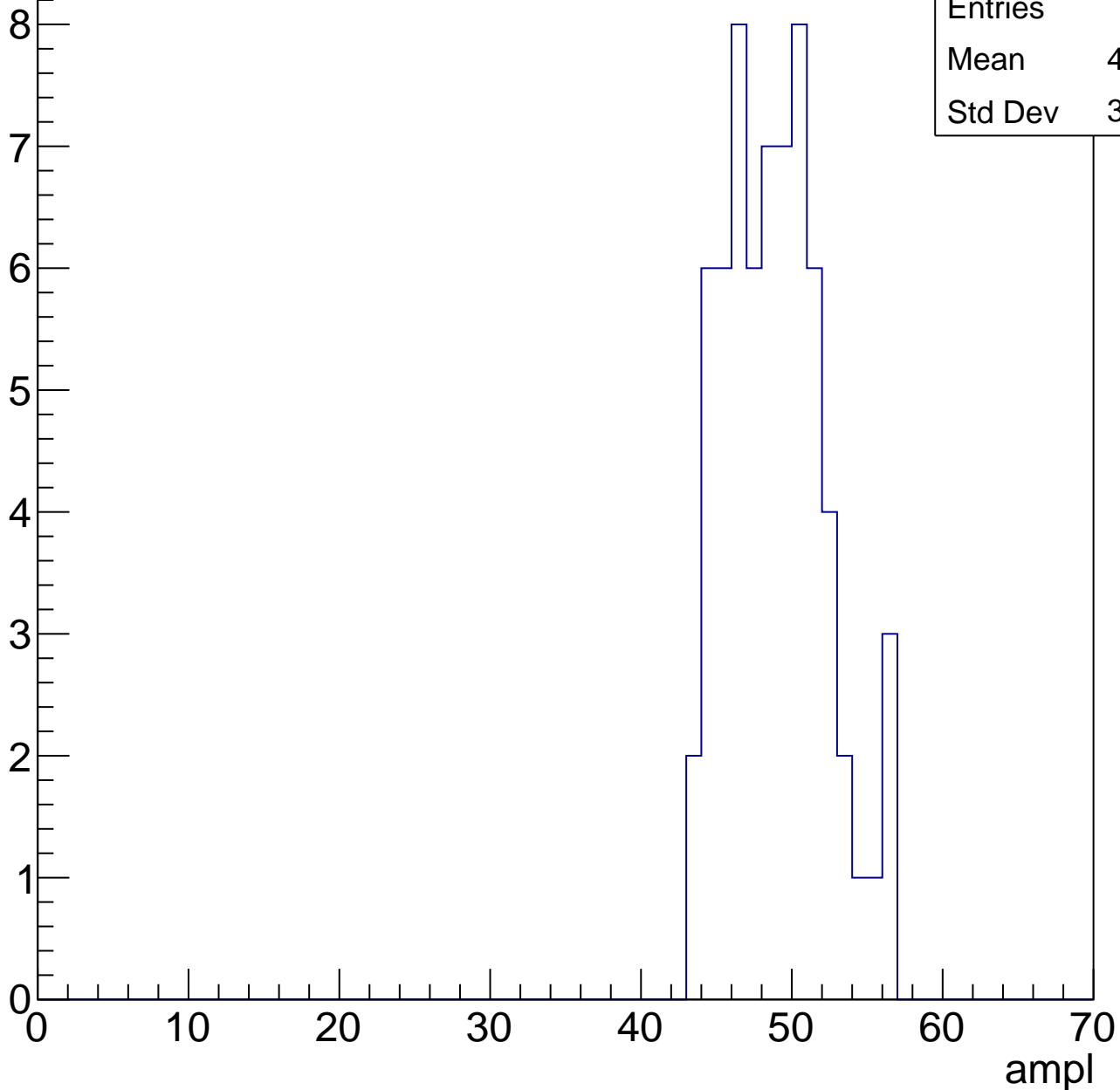


# B1L003S, U18-ch126, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	67
Mean	48.45
Std Dev	3.252

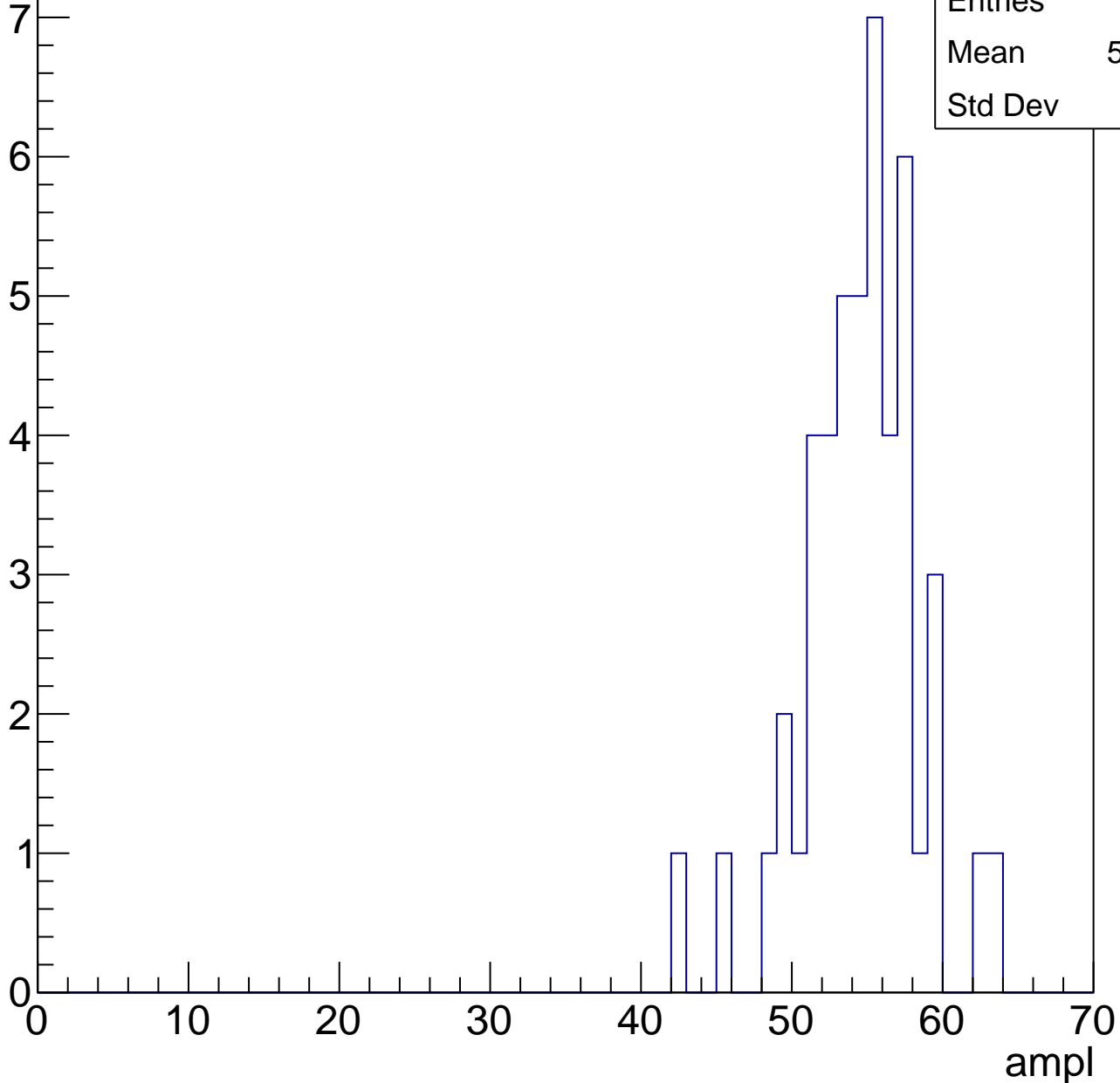


# B1L003S, U18-ch126, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

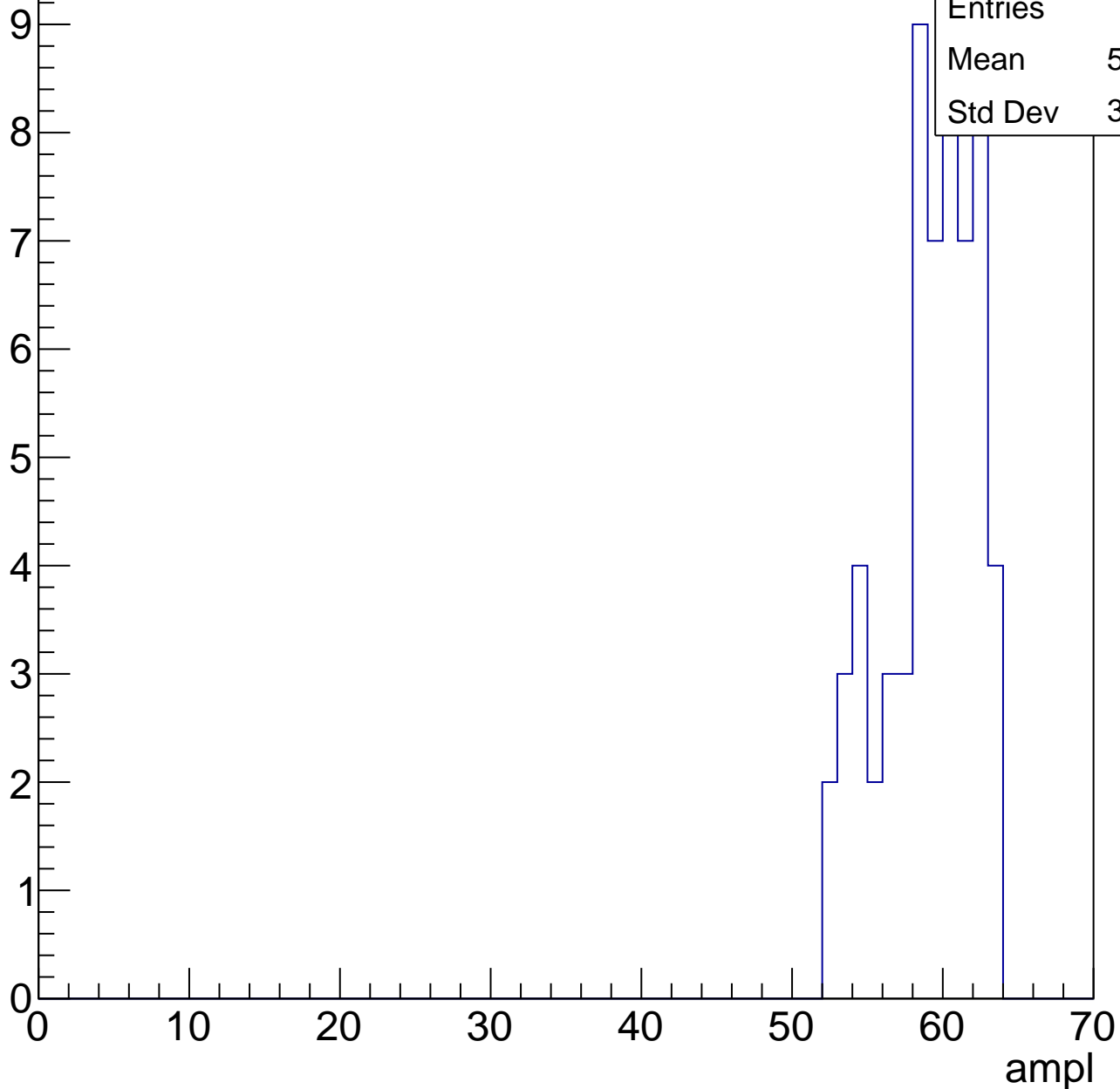
Entries	47
Mean	54.06
Std Dev	3.85



# B1L003S, U18-ch126, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

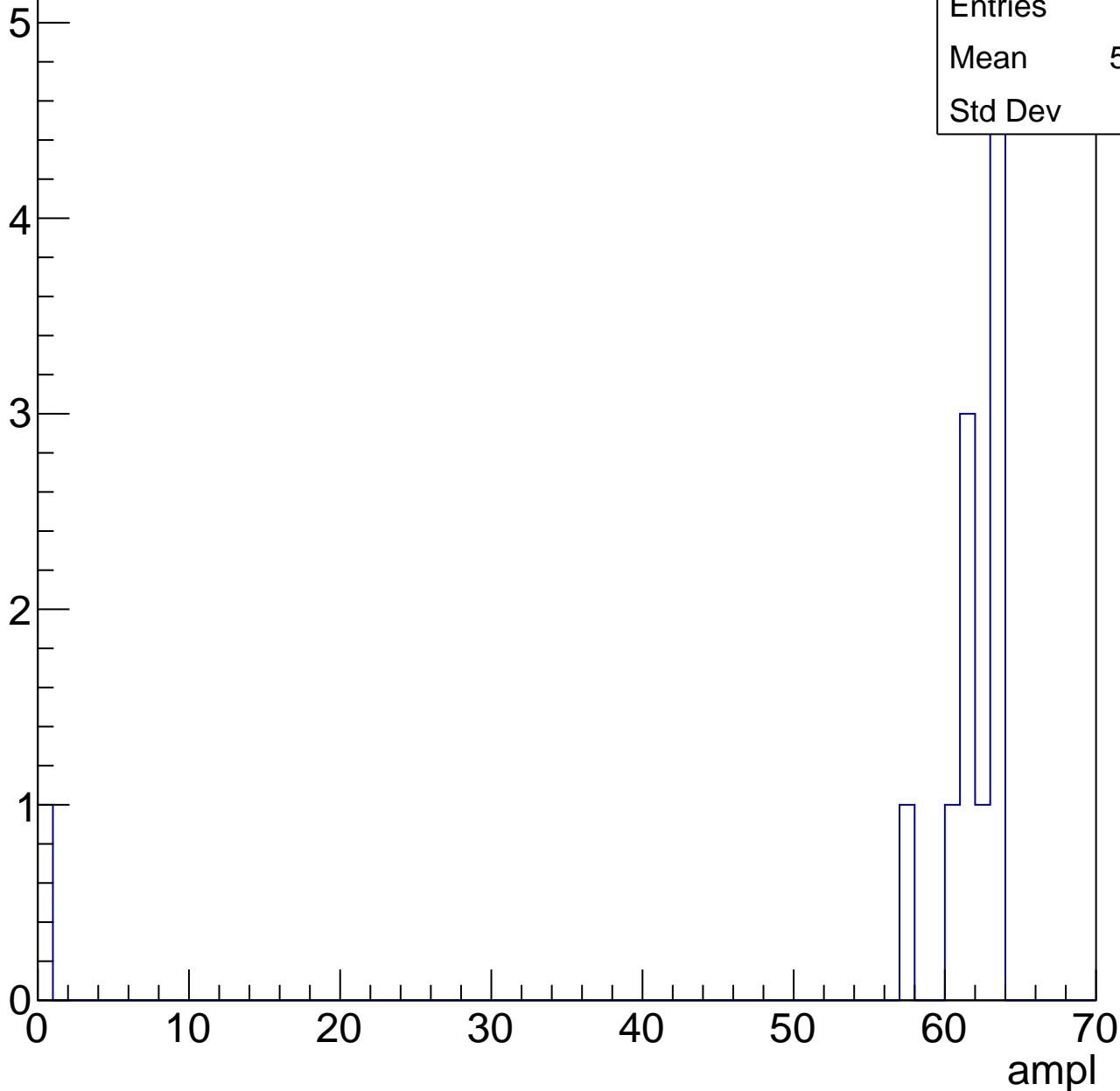


# B1L003S, U18-ch126, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	12
Mean	56.42
Std Dev	17.1





# B1L003S, U18-ch126, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L003S, U18-ch127, adc0

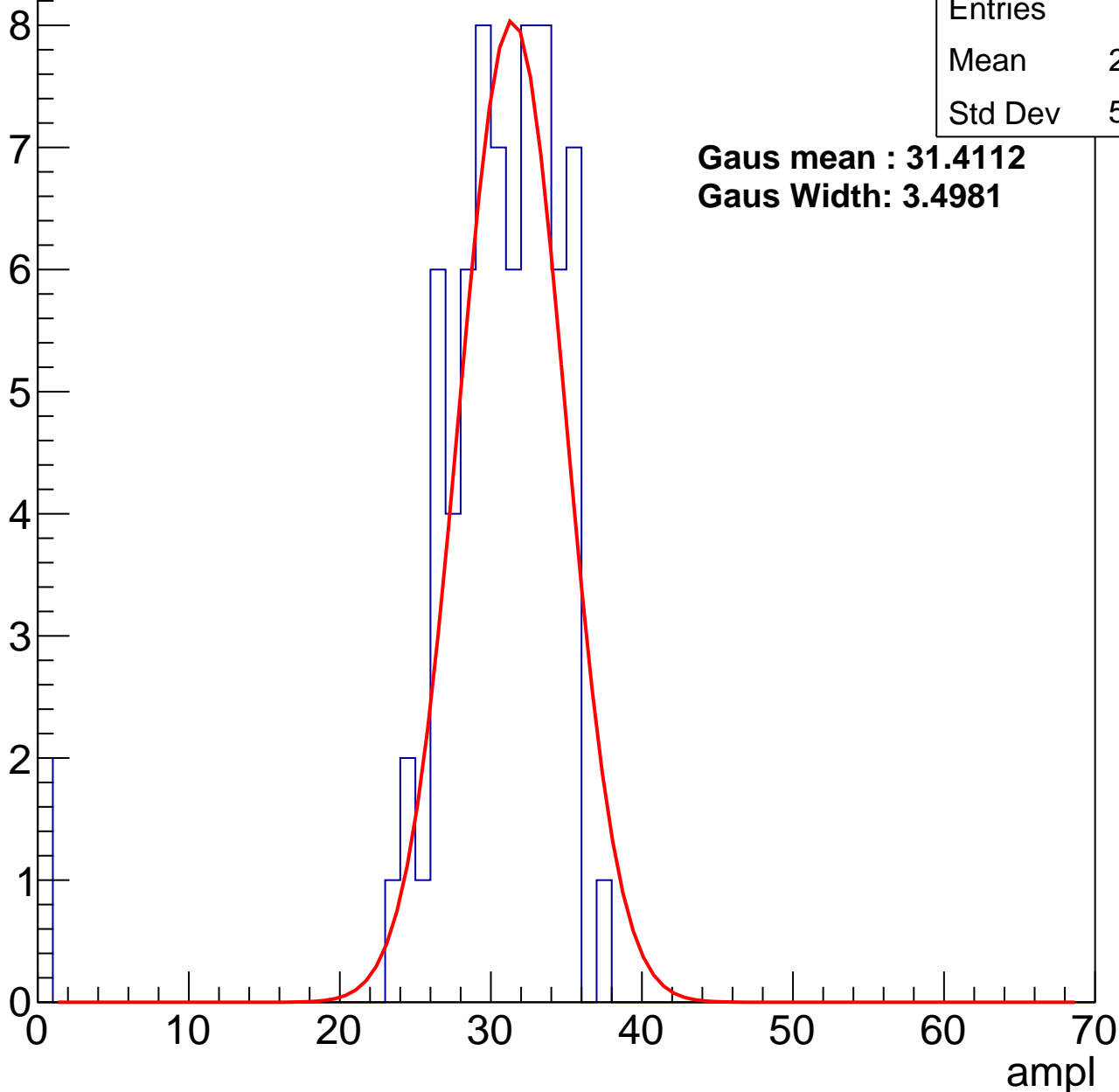
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	73
Mean	29.62
Std Dev	5.886

**Gaus mean : 31.4112**

**Gaus Width: 3.4981**



# B1L003S, U18-ch127, adc1

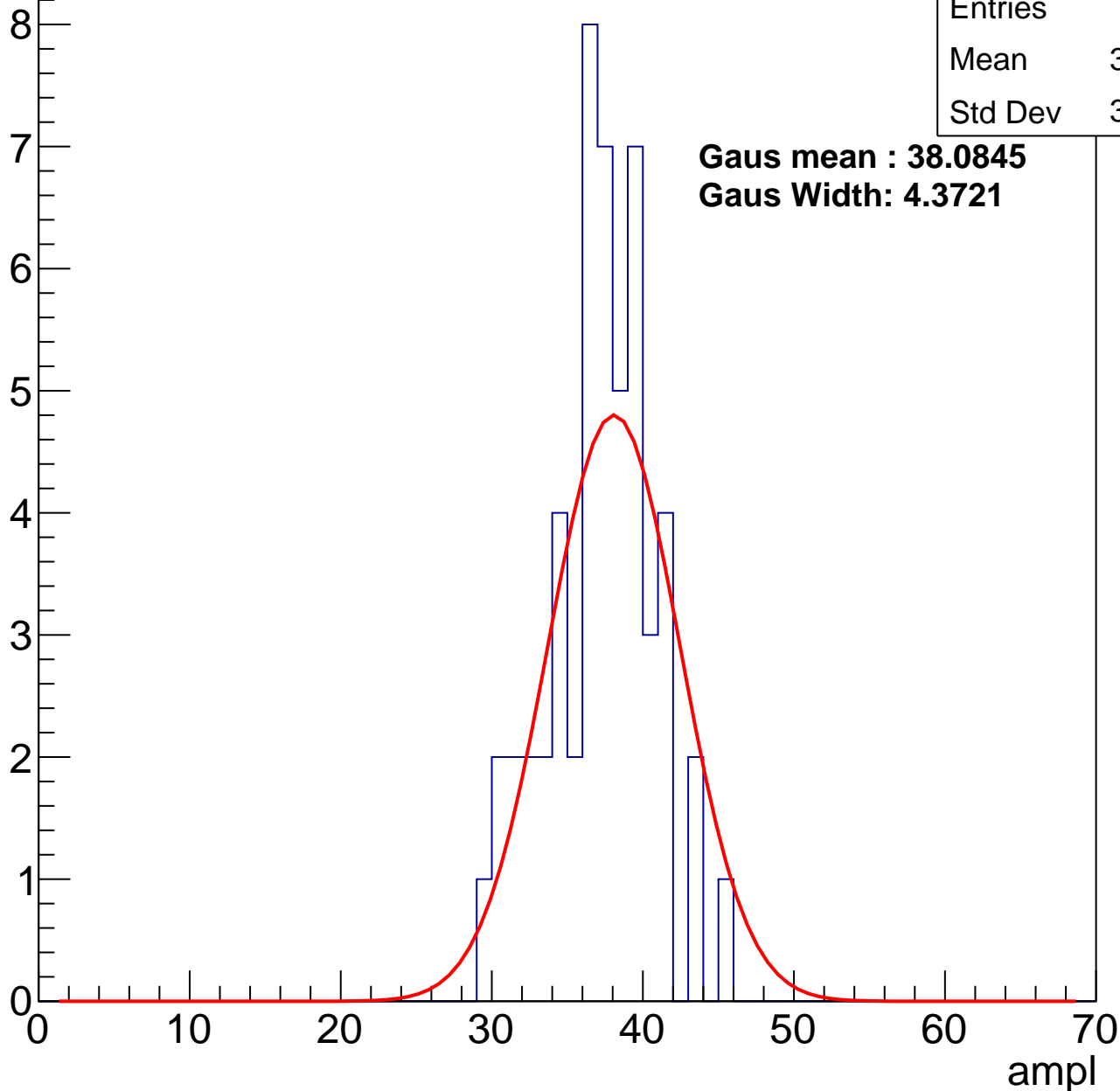
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	52
Mean	36.77
Std Dev	3.468

**Gaus mean : 38.0845**

**Gaus Width: 4.3721**



# B1L003S, U18-ch127, adc2

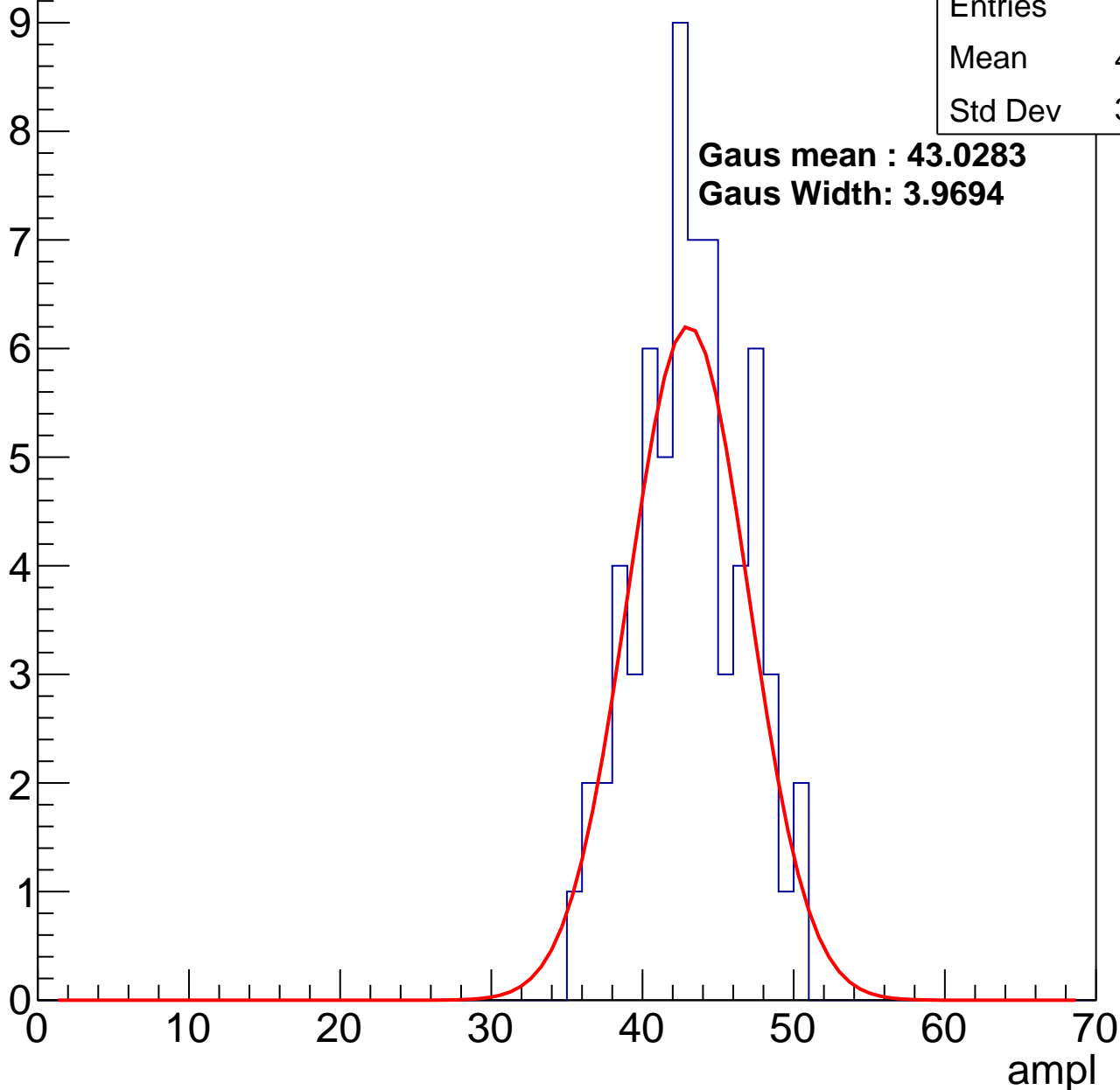
calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	65
Mean	42.71
Std Dev	3.551

**Gaus mean : 43.0283**

**Gaus Width: 3.9694**

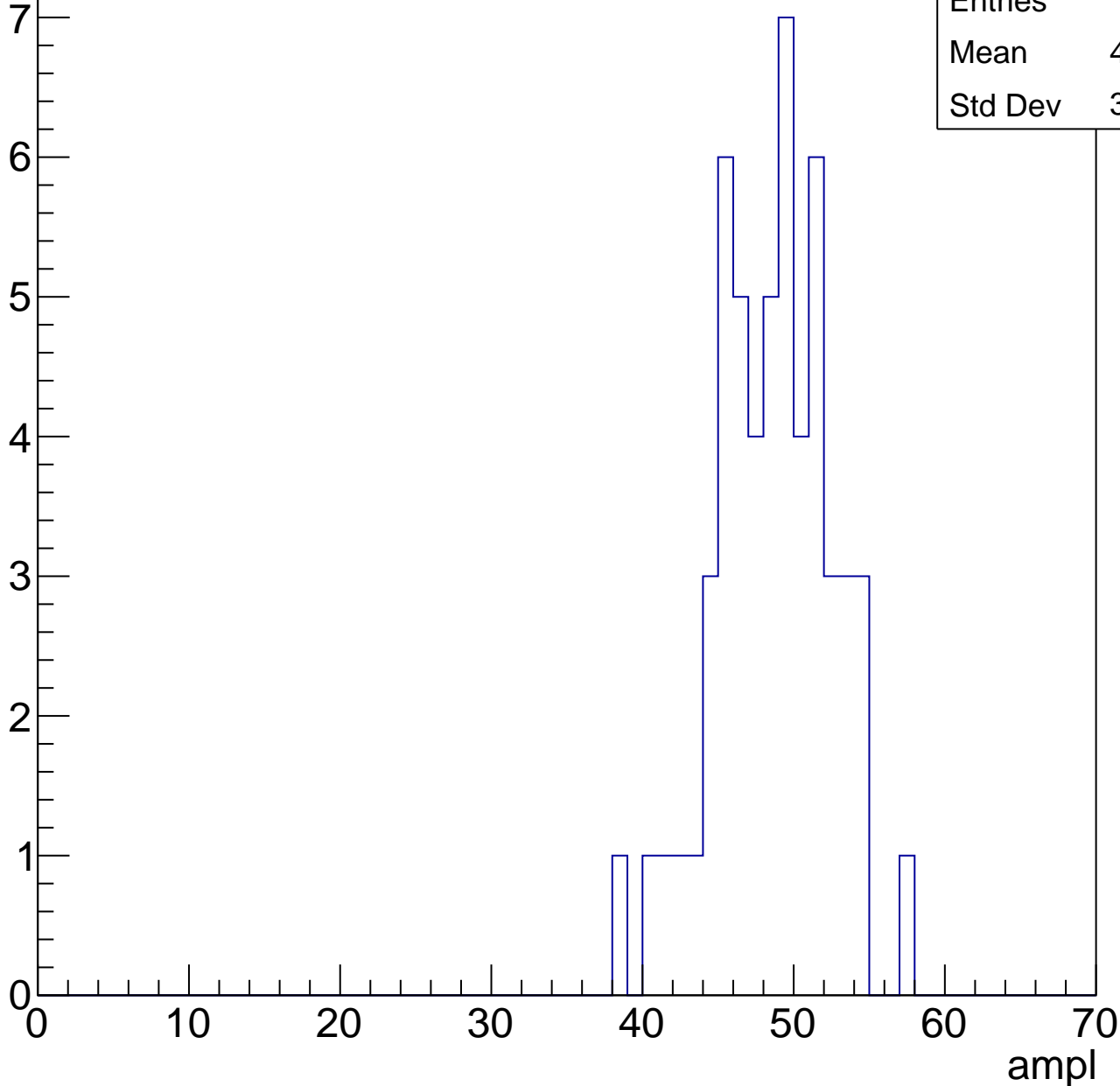


# B1L003S, U18-ch127, adc3

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	55
Mean	48.13
Std Dev	3.785



# B1L003S, U18-ch127, adc4

calib\_packv5\_042523\_0143.root, FC#13, port D2

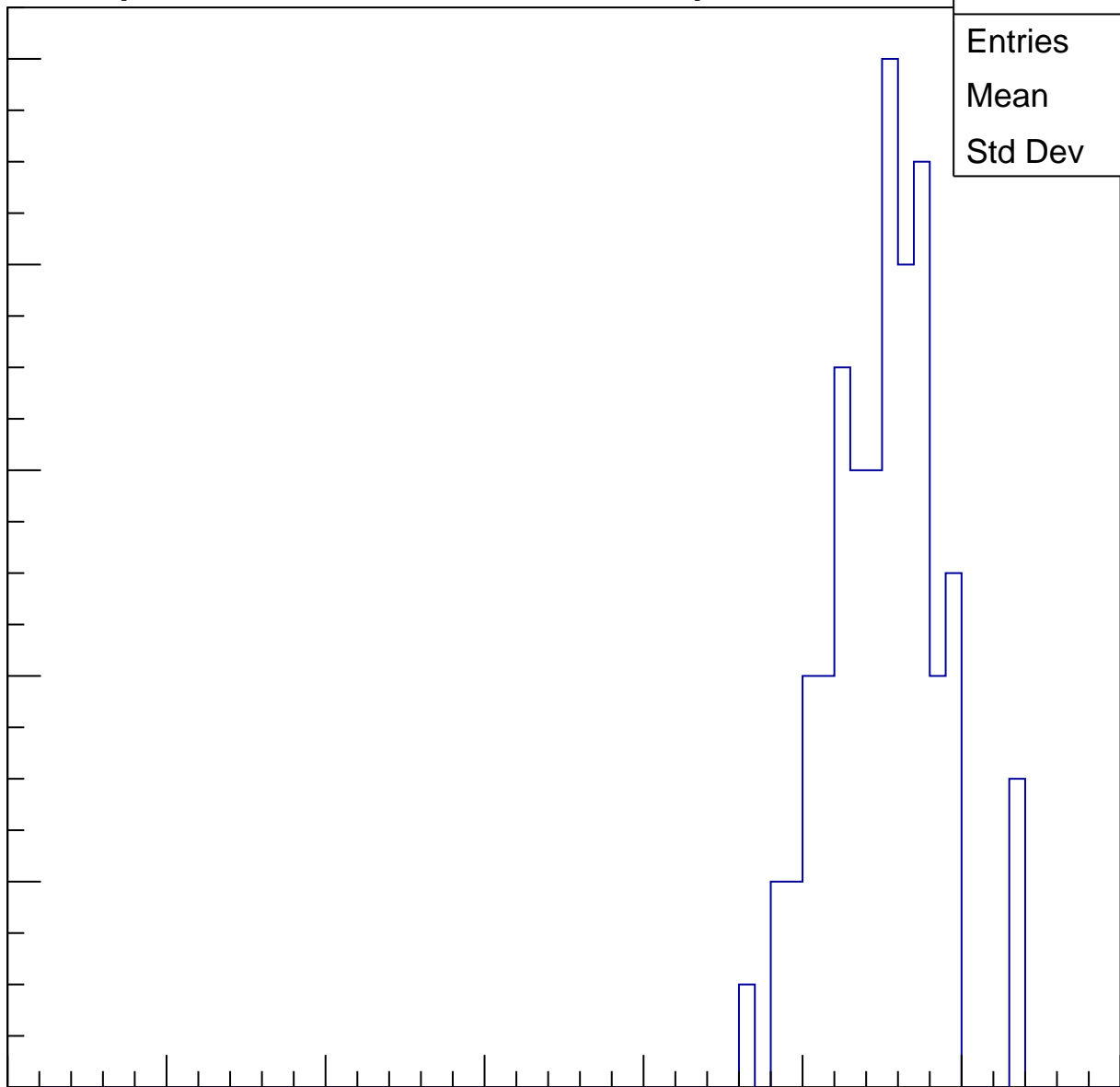
Entries	71
Mean	54.61
Std Dev	3.458

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

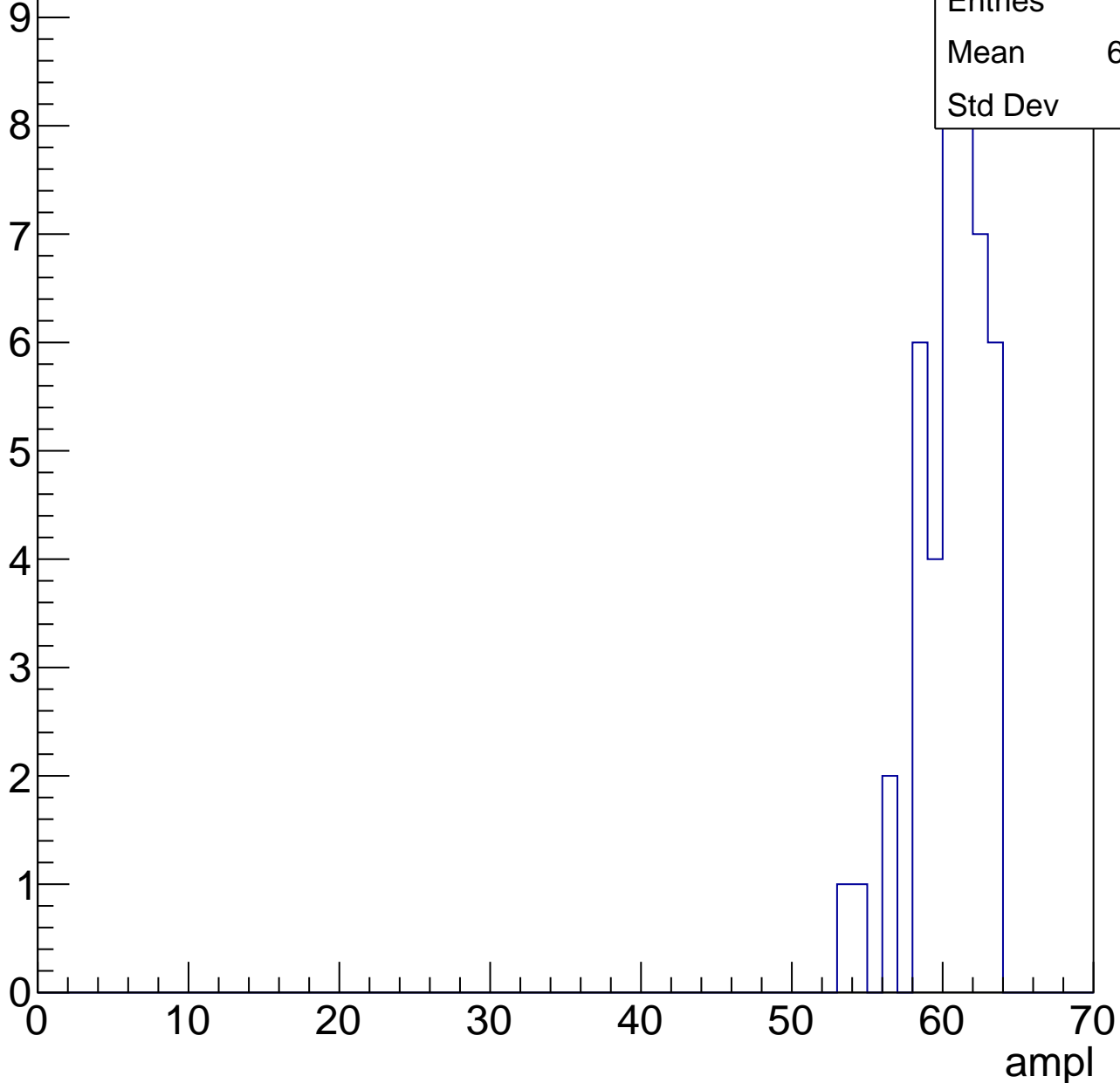


# B1L003S, U18-ch127, adc5

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

Entries	44
Mean	60.07
Std Dev	2.31



# B1L003S, U18-ch127, adc6

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

3

2.5

2

1.5

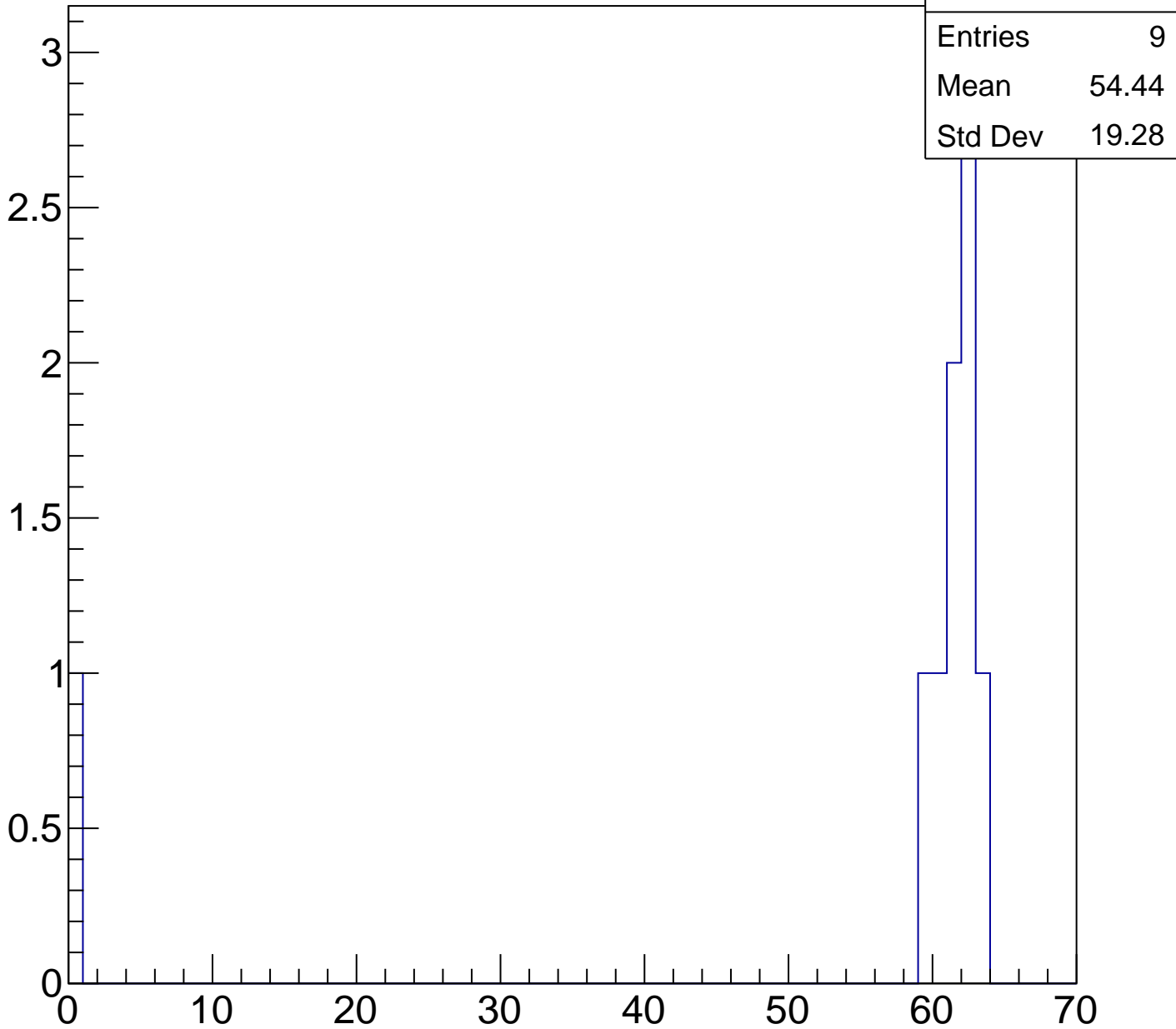
1

0.5

0

ampl

Entries	9
Mean	54.44
Std Dev	19.28





# B1L003S, U18-ch127, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry

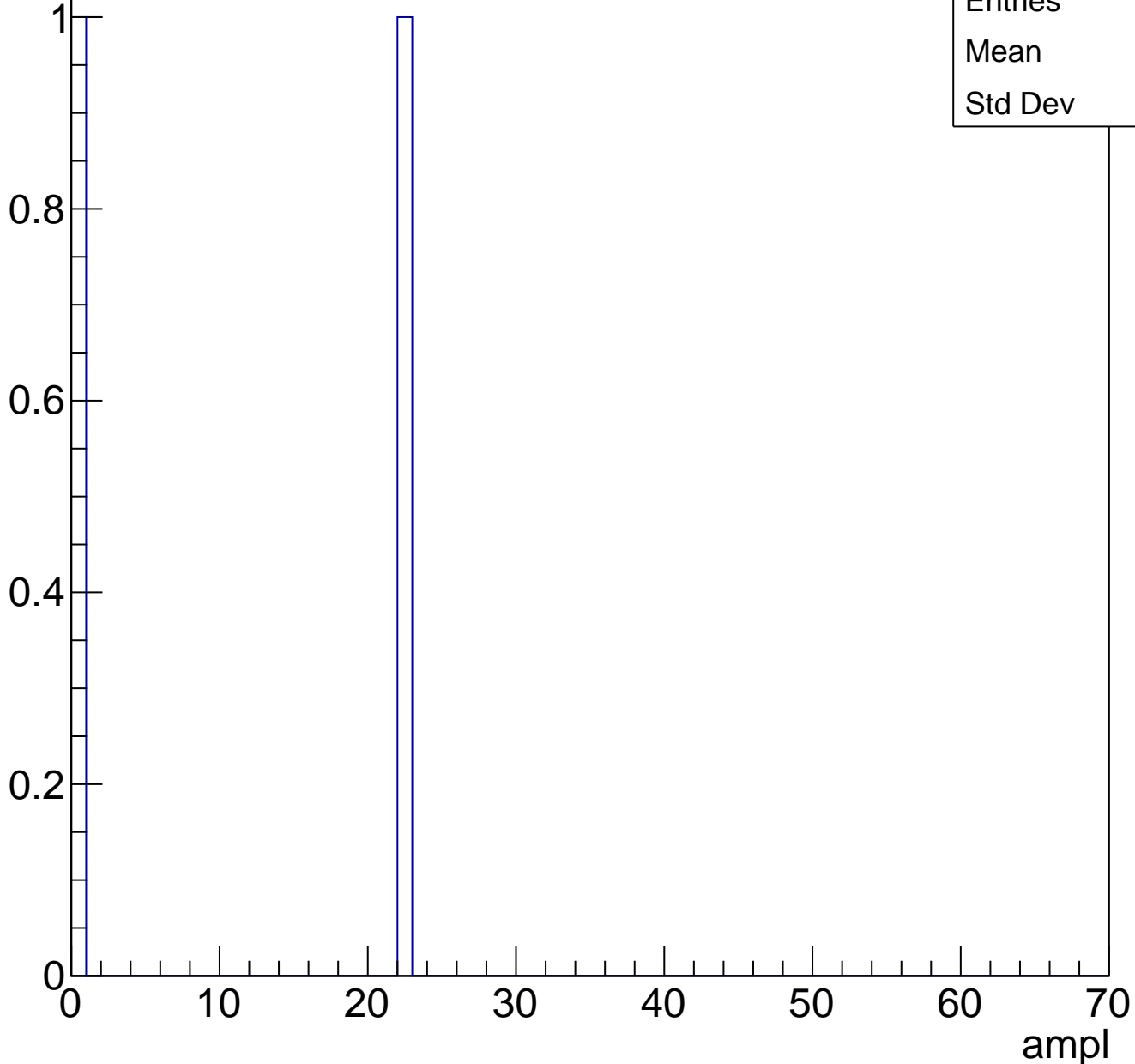


Entries	2
Mean	11
Std Dev	11

# B1L003S, U18-ch127, adc7

calib\_packv5\_042523\_0143.root, FC#13, port D2

Entry



Entries	2
Mean	11
Std Dev	11