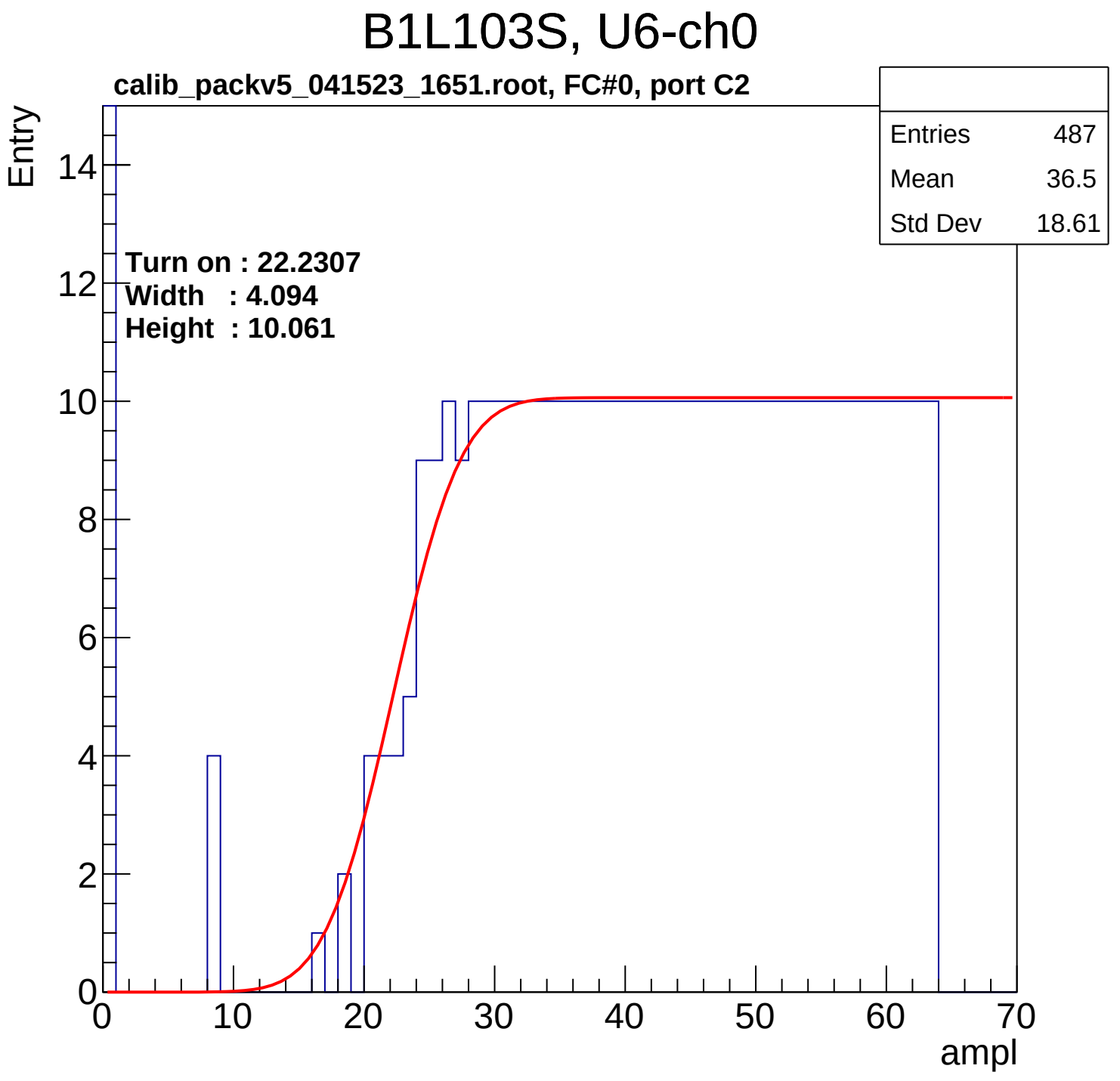
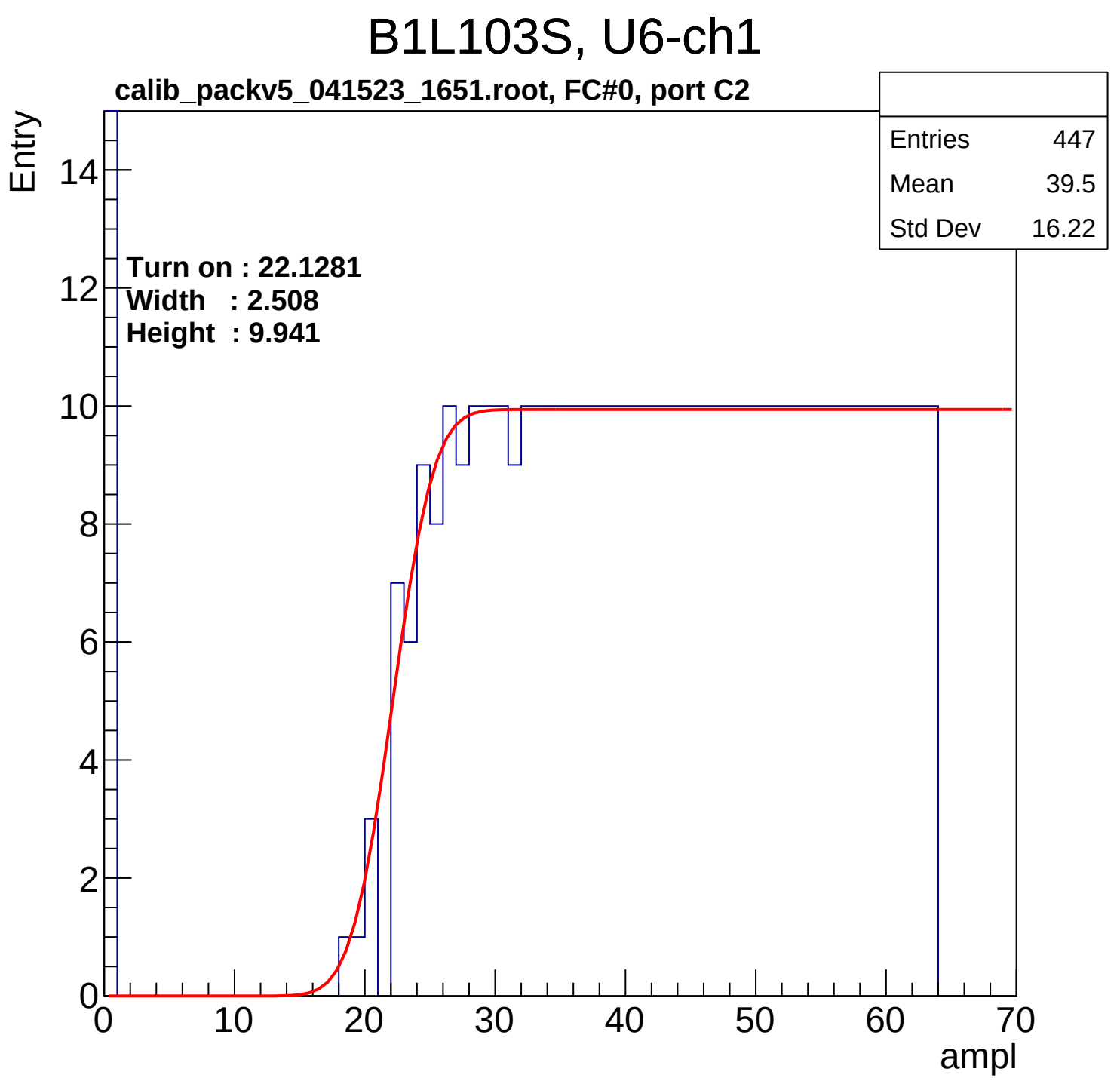
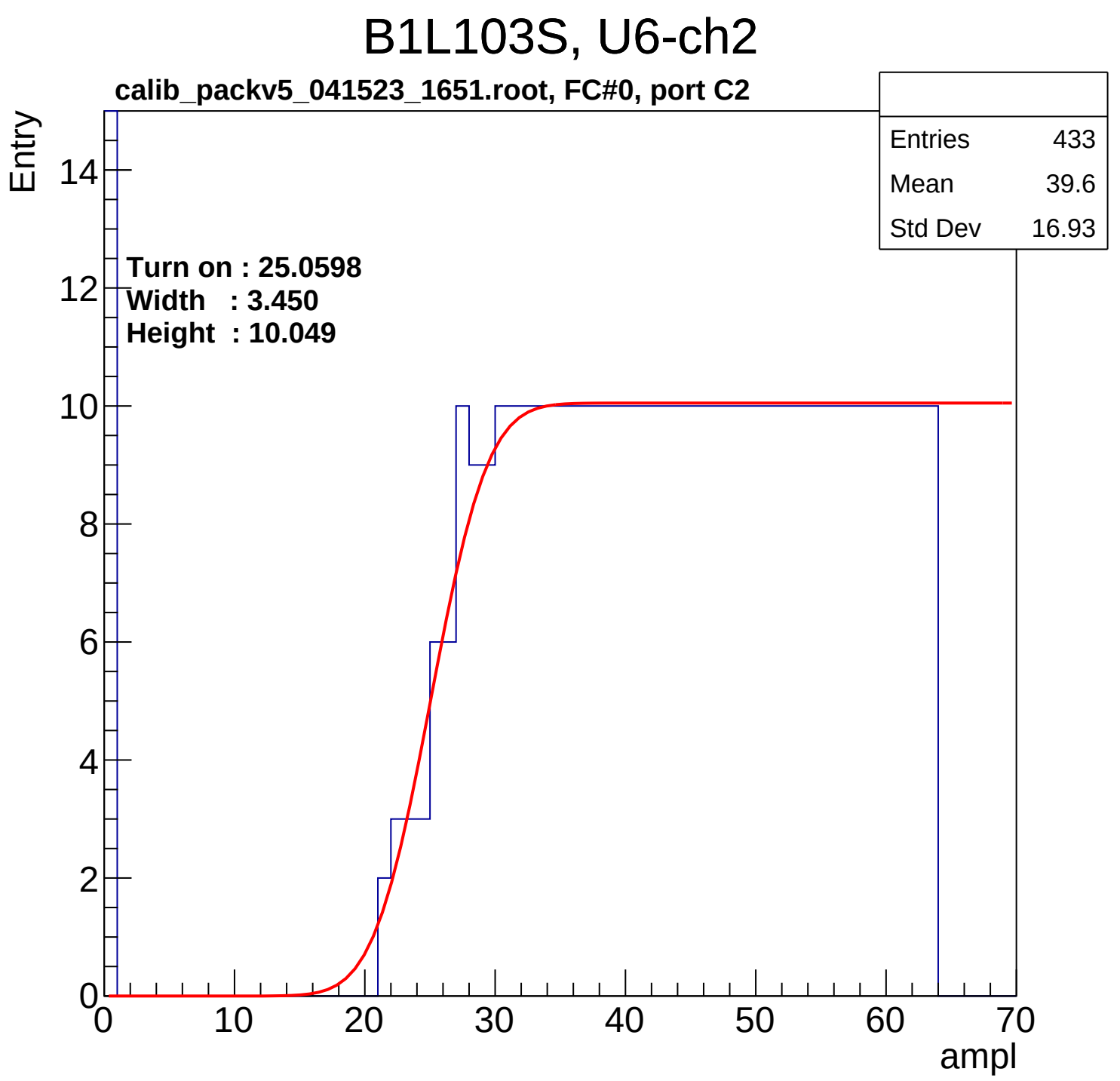
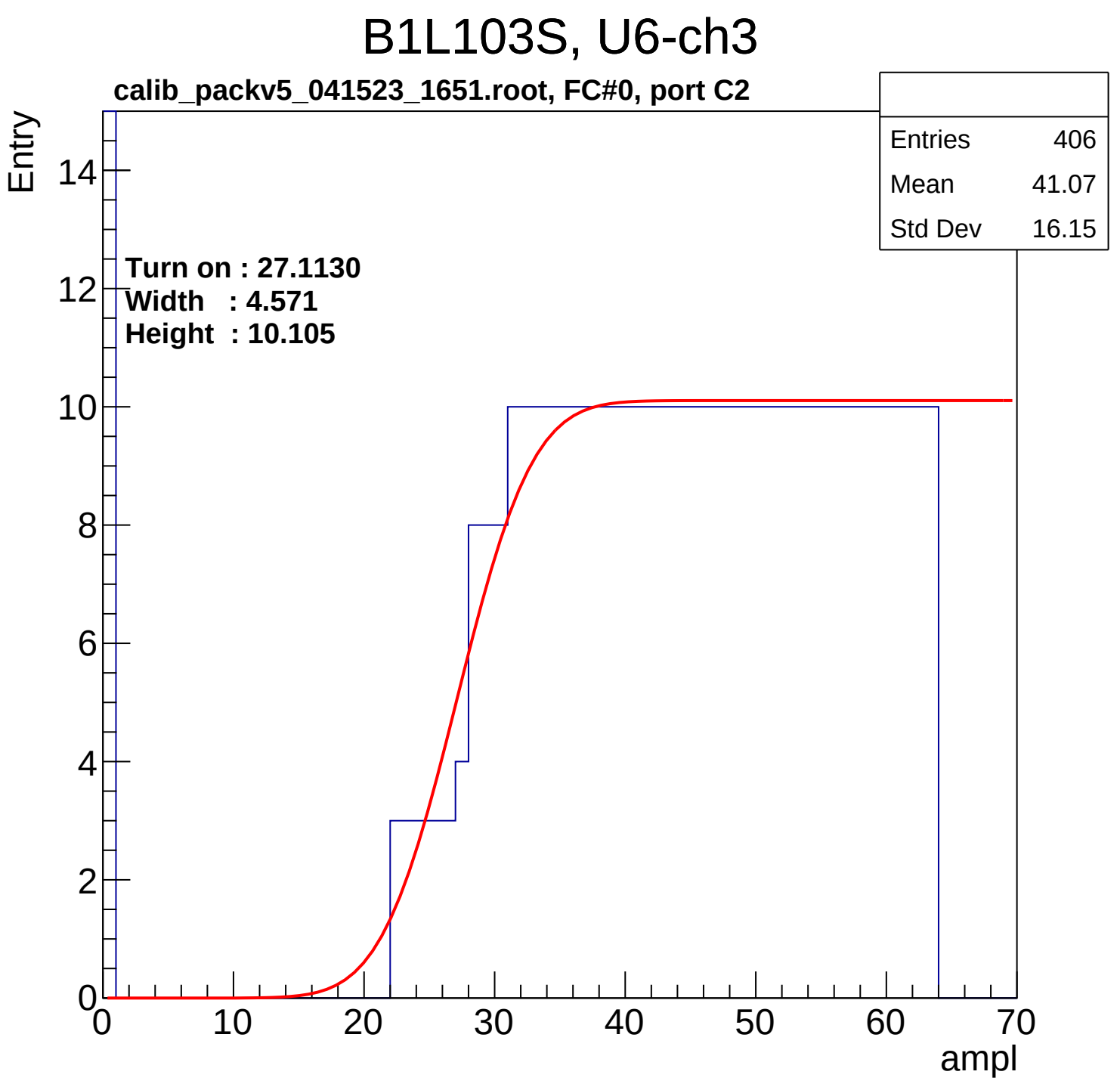
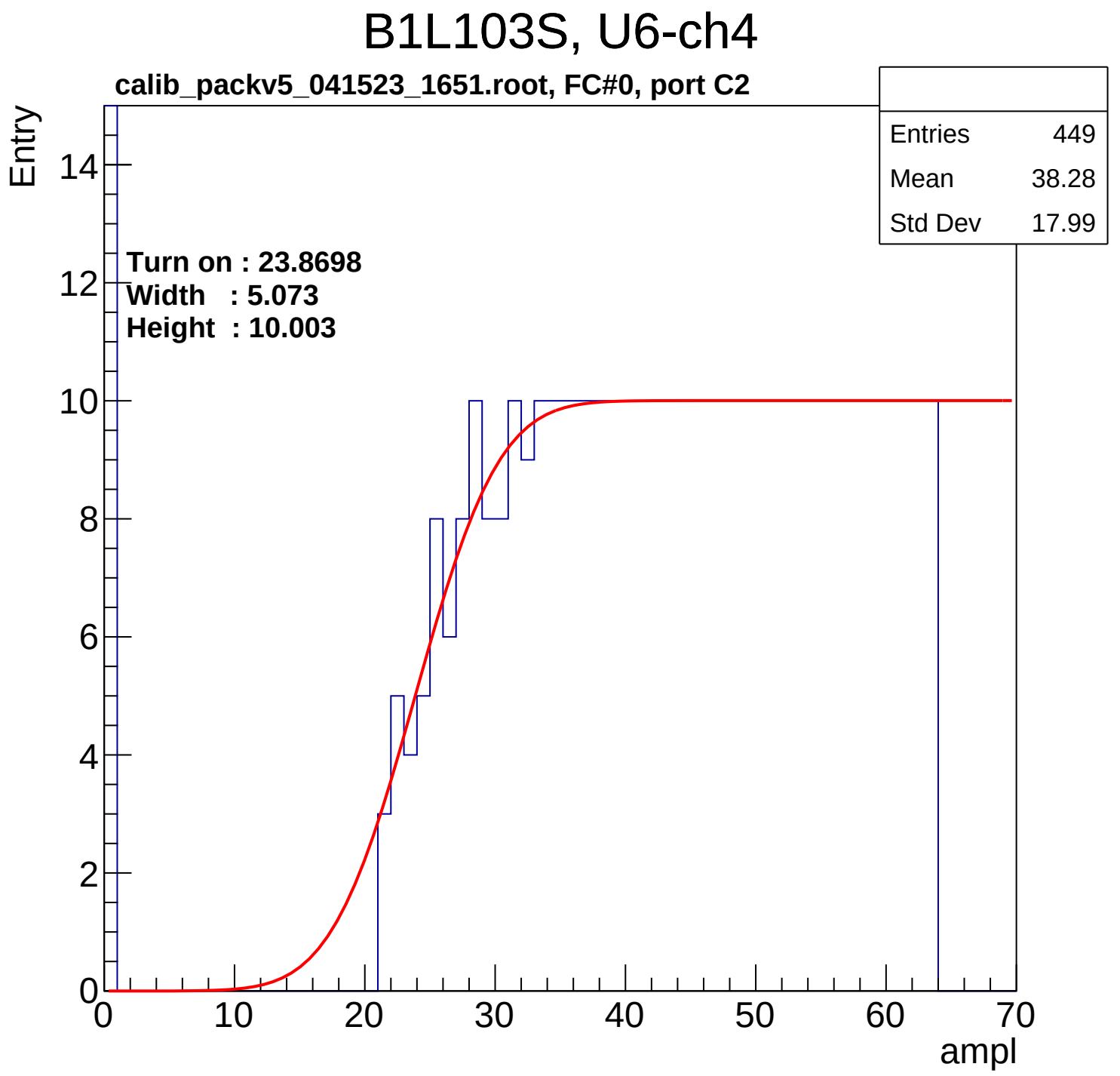
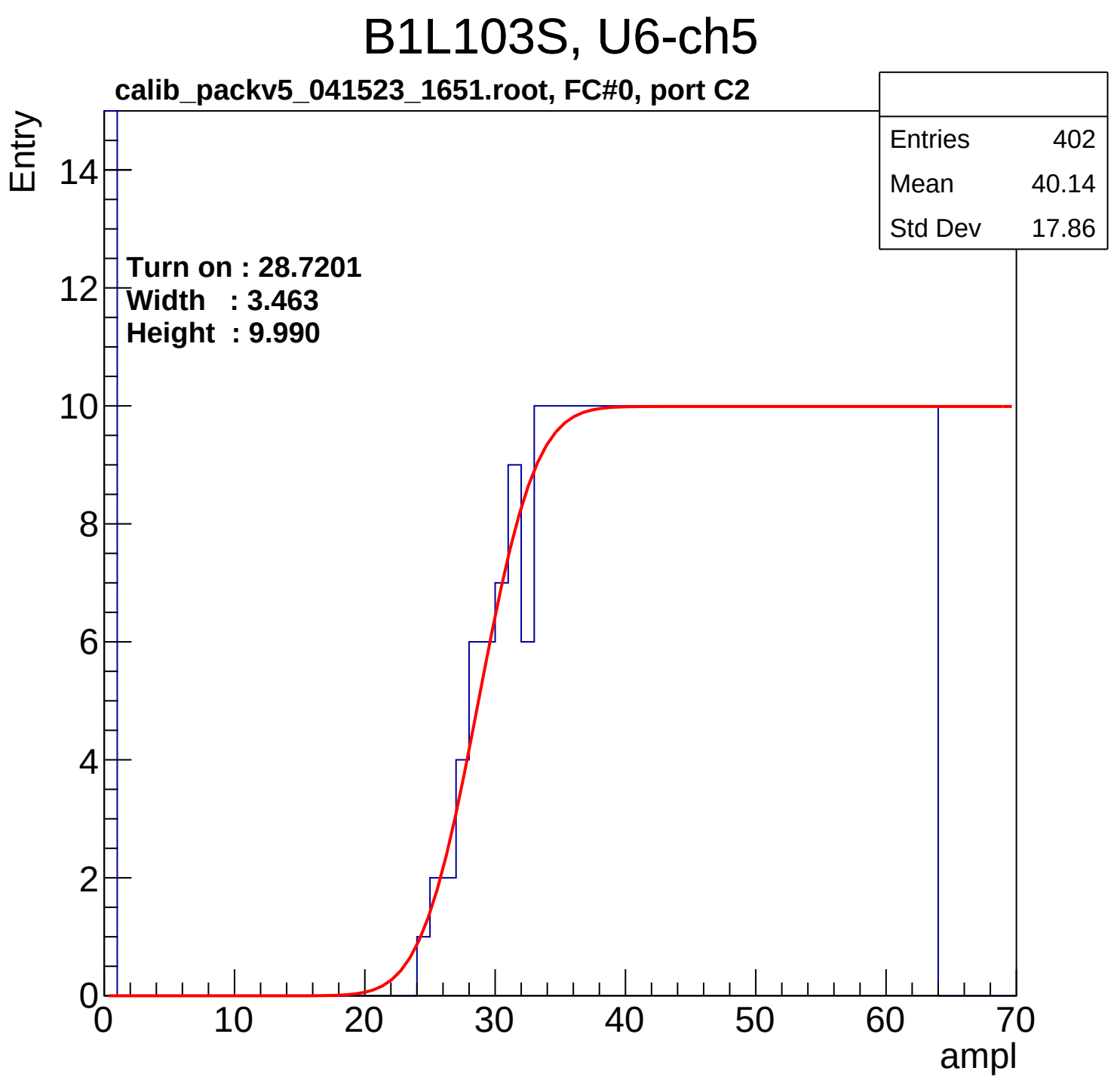

B1L103S, U6-ch0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 487
Mean 36.5
Std Dev 18.61
Turn on : 22.2307
Width : 4.094
Height : 10.061
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

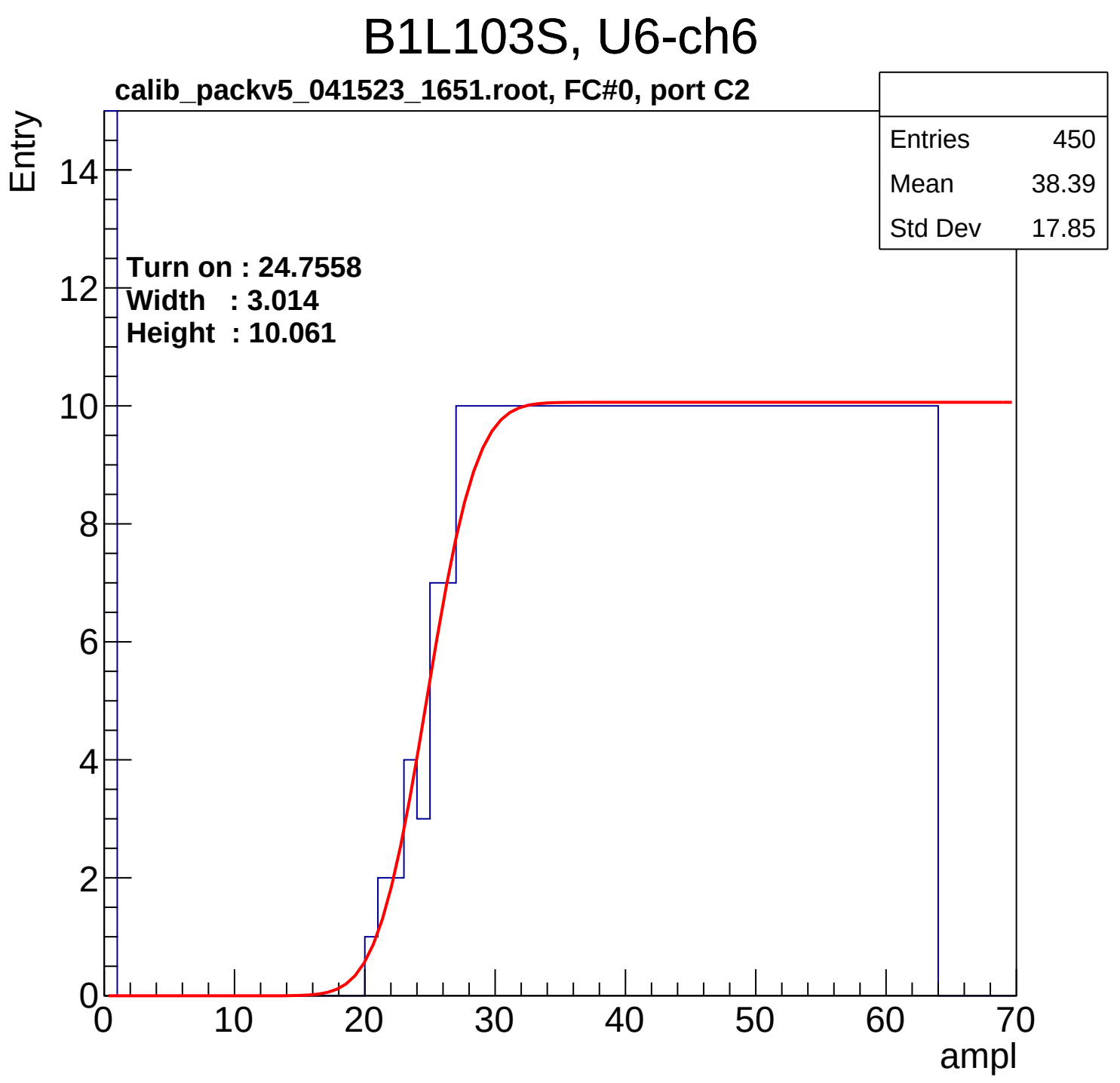

B1L103S, U6-ch1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 447
Mean 39.5
Std Dev 16.22
Turn on : 22.1281
Width : 2.508
Height : 9.941
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

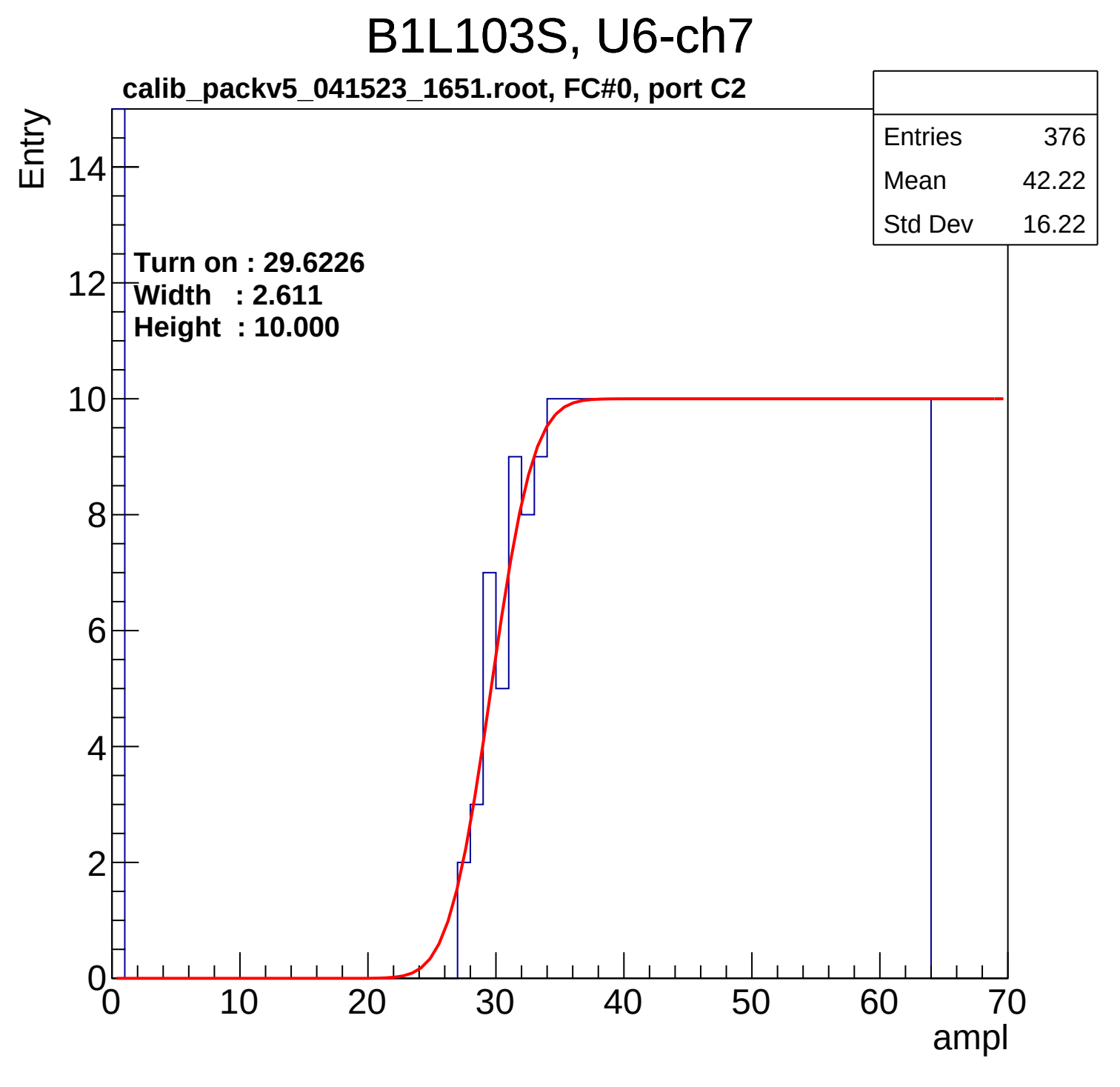

B1L103S, U6-ch2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 433
Mean 39.6
Std Dev 16.93
Turn on : 25.0598
Width : 3.450
Height : 10.049
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

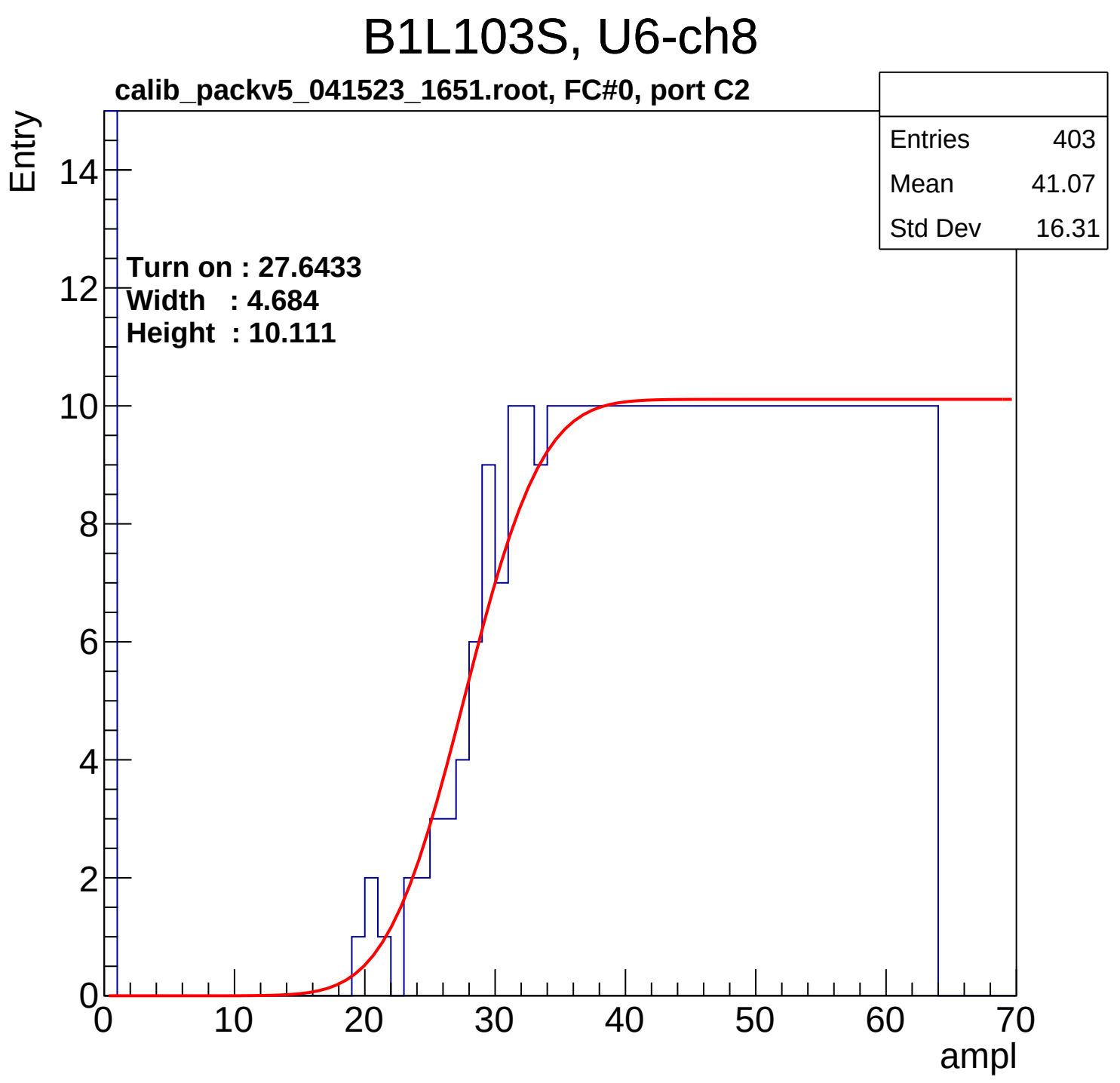

B1L103S, U6-ch3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 406
Mean 41.07
Std Dev 16.15
Turn on : 27.1130
Width : 4.571
Height : 10.105
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

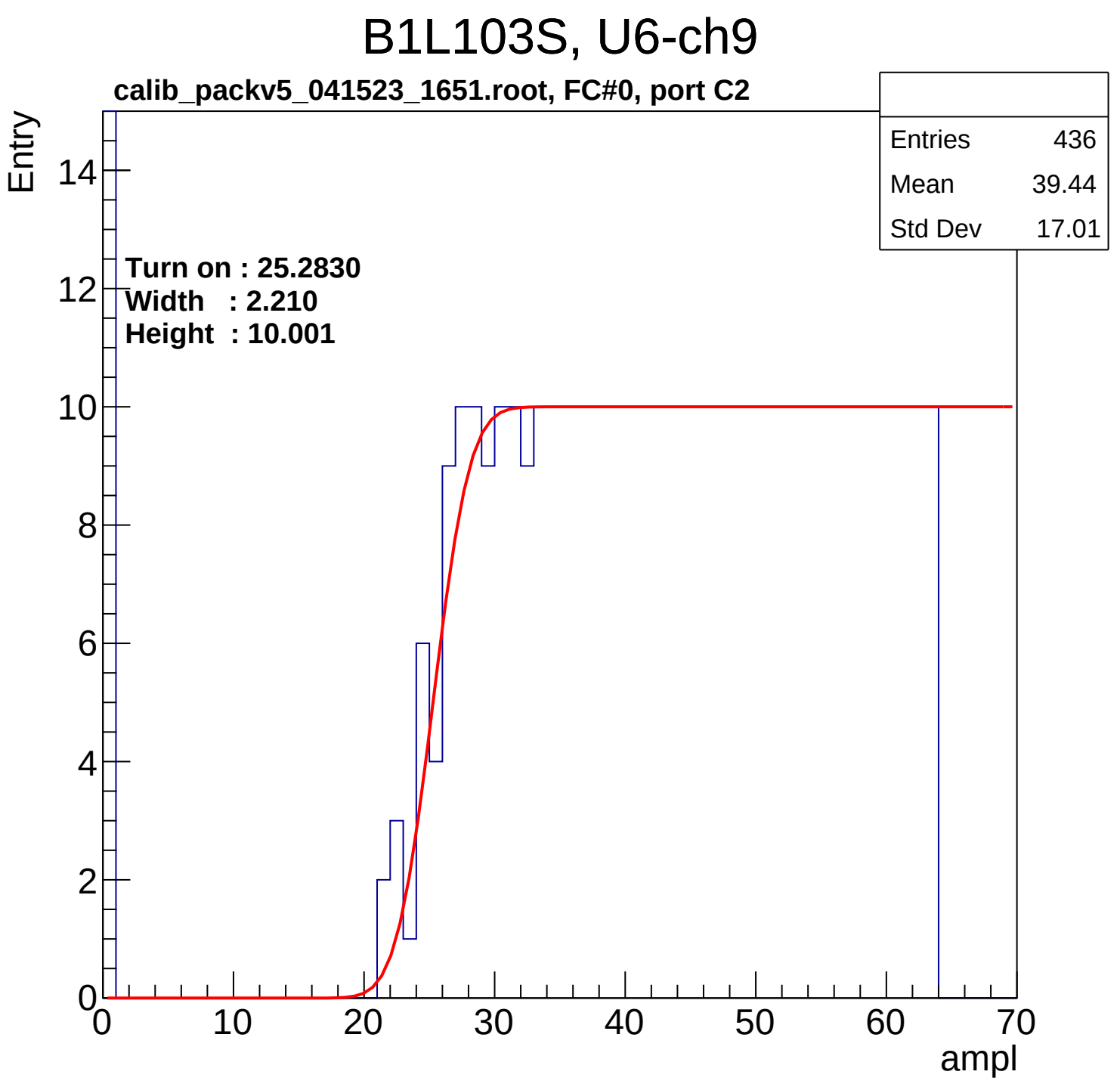

B1L103S, U6-ch4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 449
Mean 38.28
Std Dev 17.99
Turn on : 23.8698
Width : 5.073
Height : 10.003
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

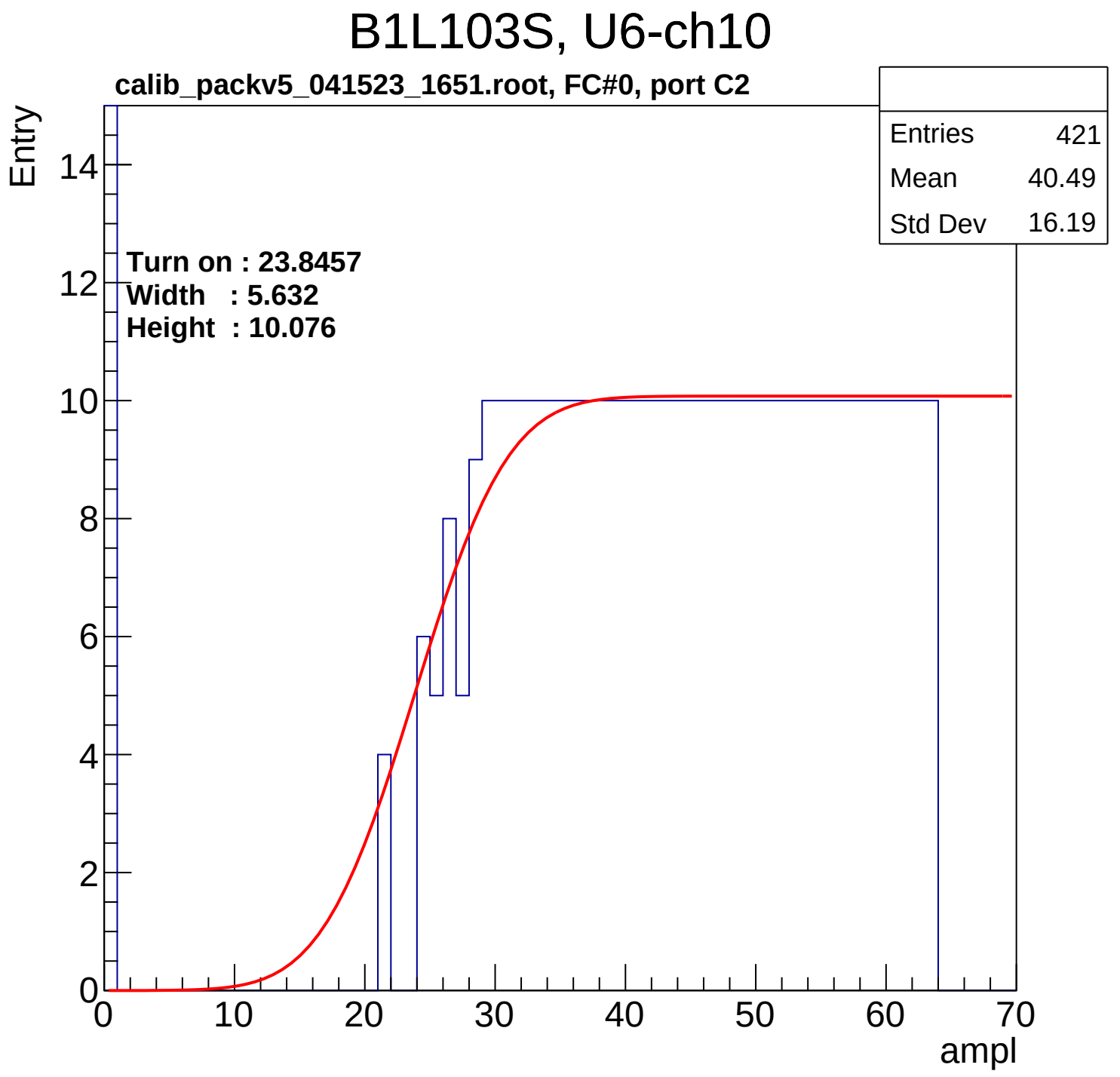

B1L103S, U6-ch5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 402
Mean 40.14
Std Dev 17.86
Turn on : 28.7201
Width : 3.463
Height : 9.990
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

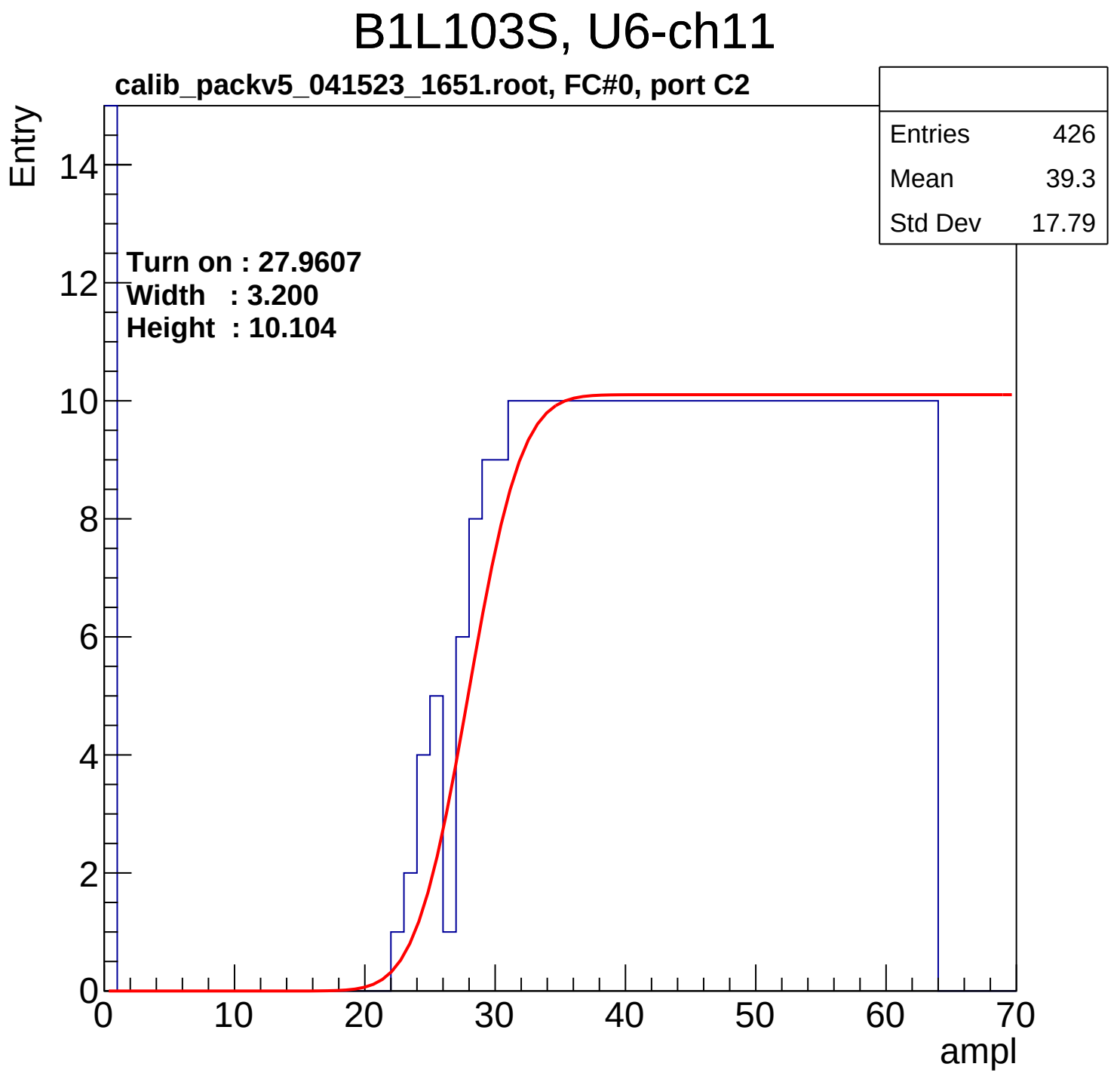

B1L103S, U6-ch6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 450
Mean 38.39
Std Dev 17.85
Turn on : 24.7558
Width : 3.014
Height : 10.061
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

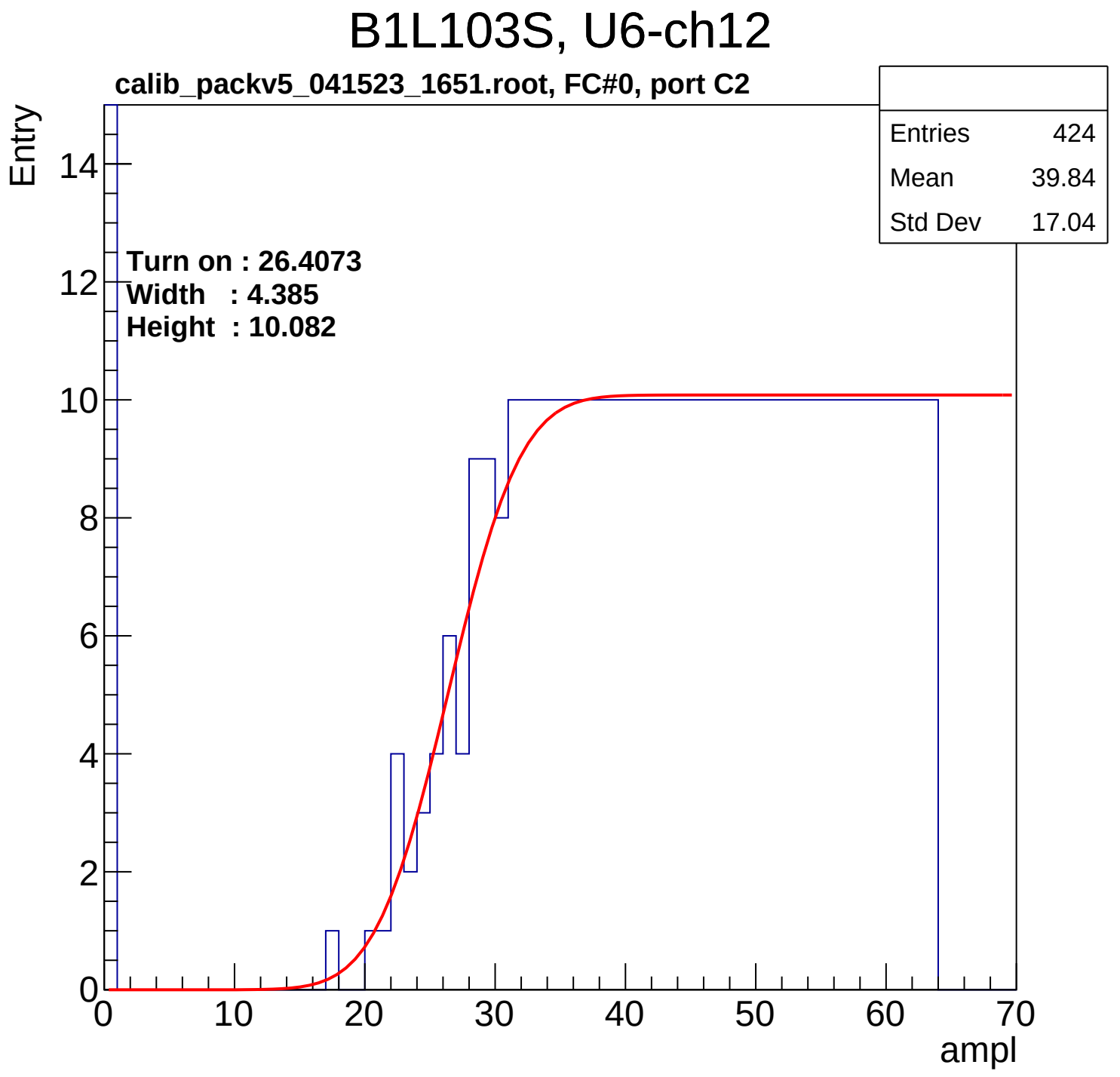

B1L103S, U6-ch7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 376
Mean 42.22
Std Dev 16.22
Turn on : 29.6226
Width : 2.611
Height : 10.000
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

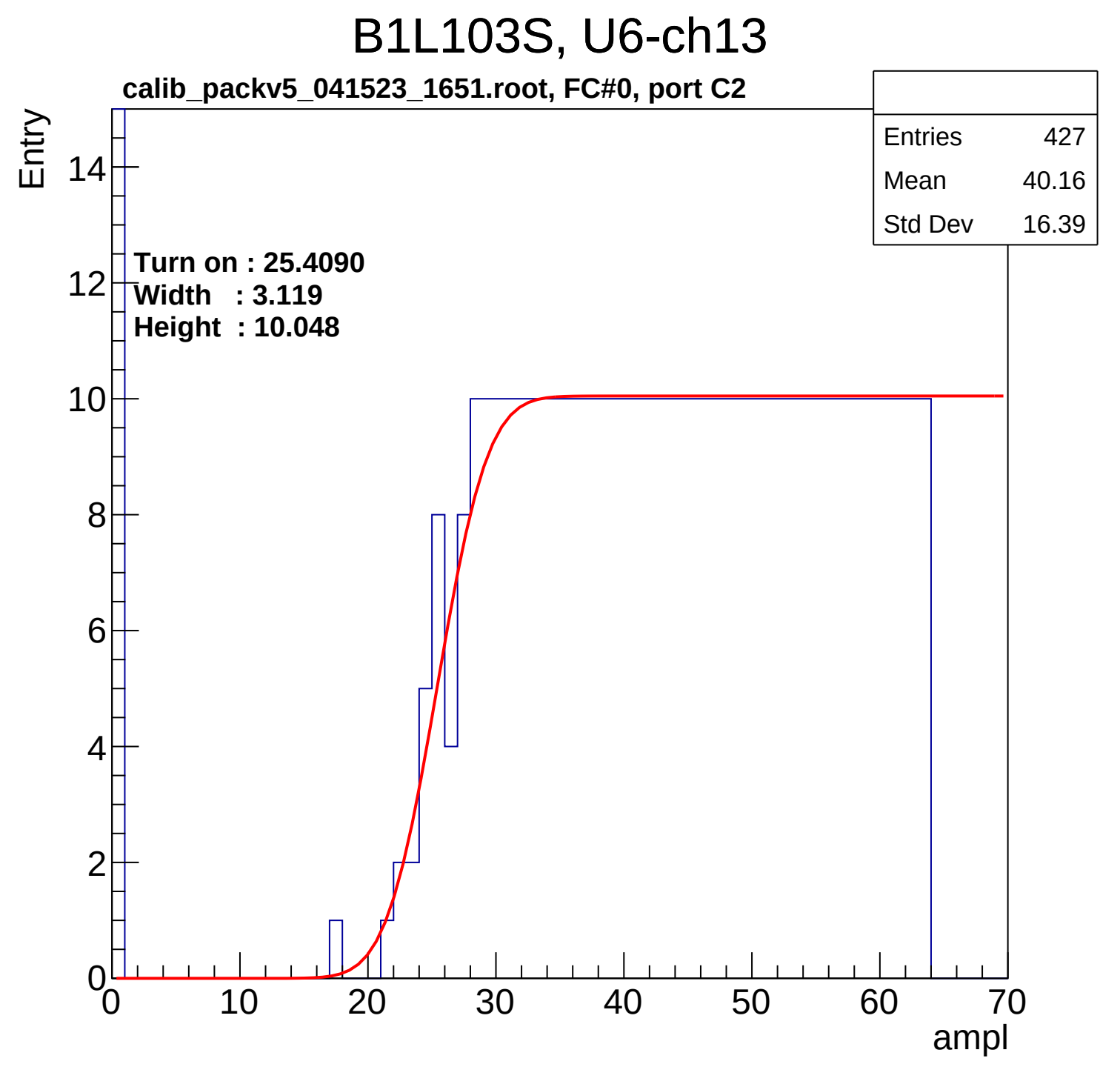

B1L103S, U6-ch8
calib_packv5_041523_1651.root, FC#0, port C2
Entries 403
Mean 41.07
Std Dev 16.31
Turn on : 27.6433
Width : 4.684
Height : 10.111
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

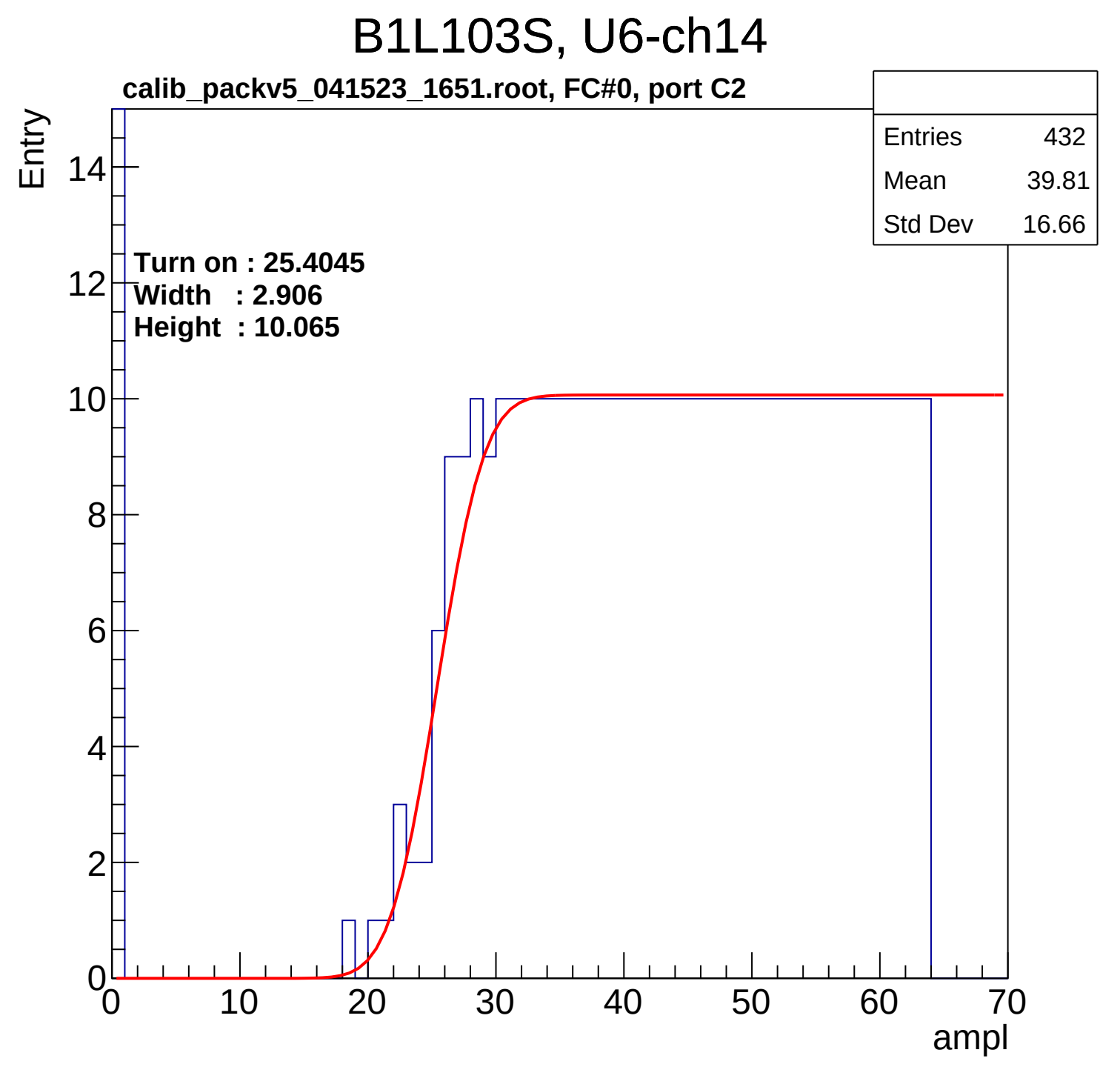

B1L103S, U6-ch9
calib_packv5_041523_1651.root, FC#0, port C2
Entries 436
Mean 39.44
Std Dev 17.01
Turn on : 25.2830
Width : 2.210
Height : 10.001
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

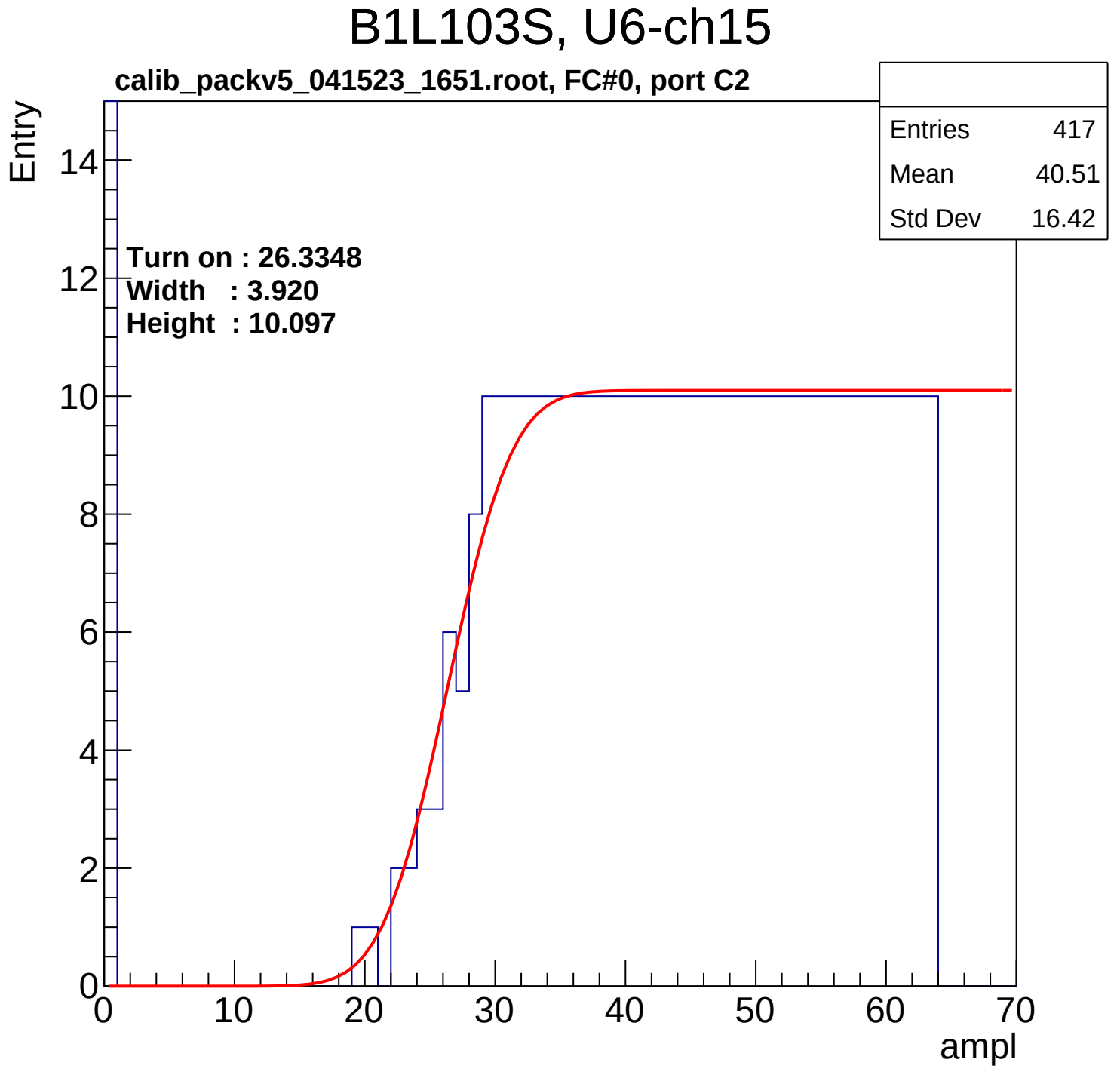

B1L103S, U6-ch10
calib_packv5_041523_1651.root, FC#0, port C2
Entries 421
Mean 40.49
Std Dev 16.19
Turn on : 23.8457
Width : 5.632
Height : 10.076
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

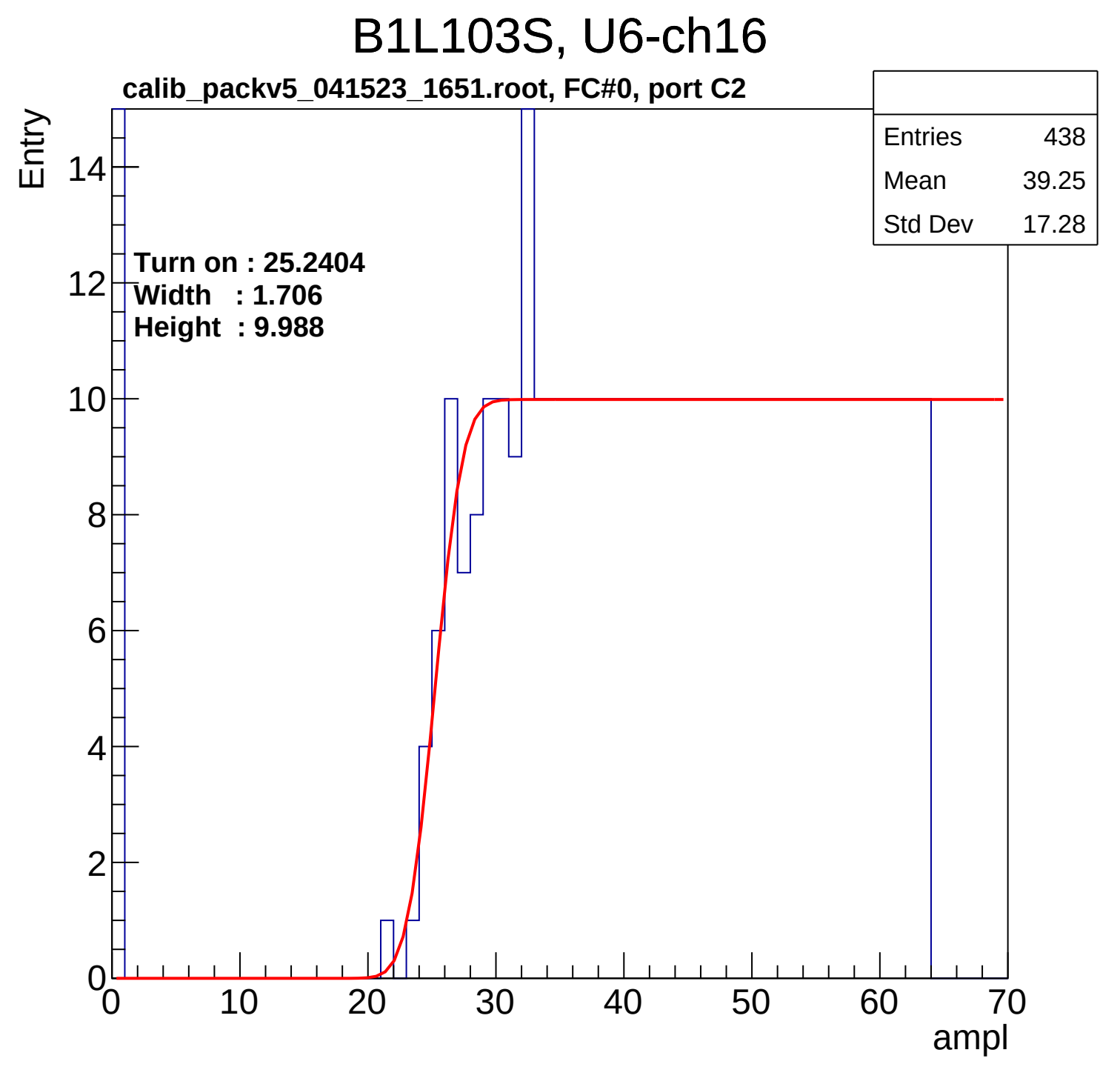

B1L103S, U6-ch11
calib_packv5_041523_1651.root, FC#0, port C2
Entries 426
Mean 39.3
Std Dev 17.79
Turn on : 27.9607
Width : 3.200
Height : 10.104
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

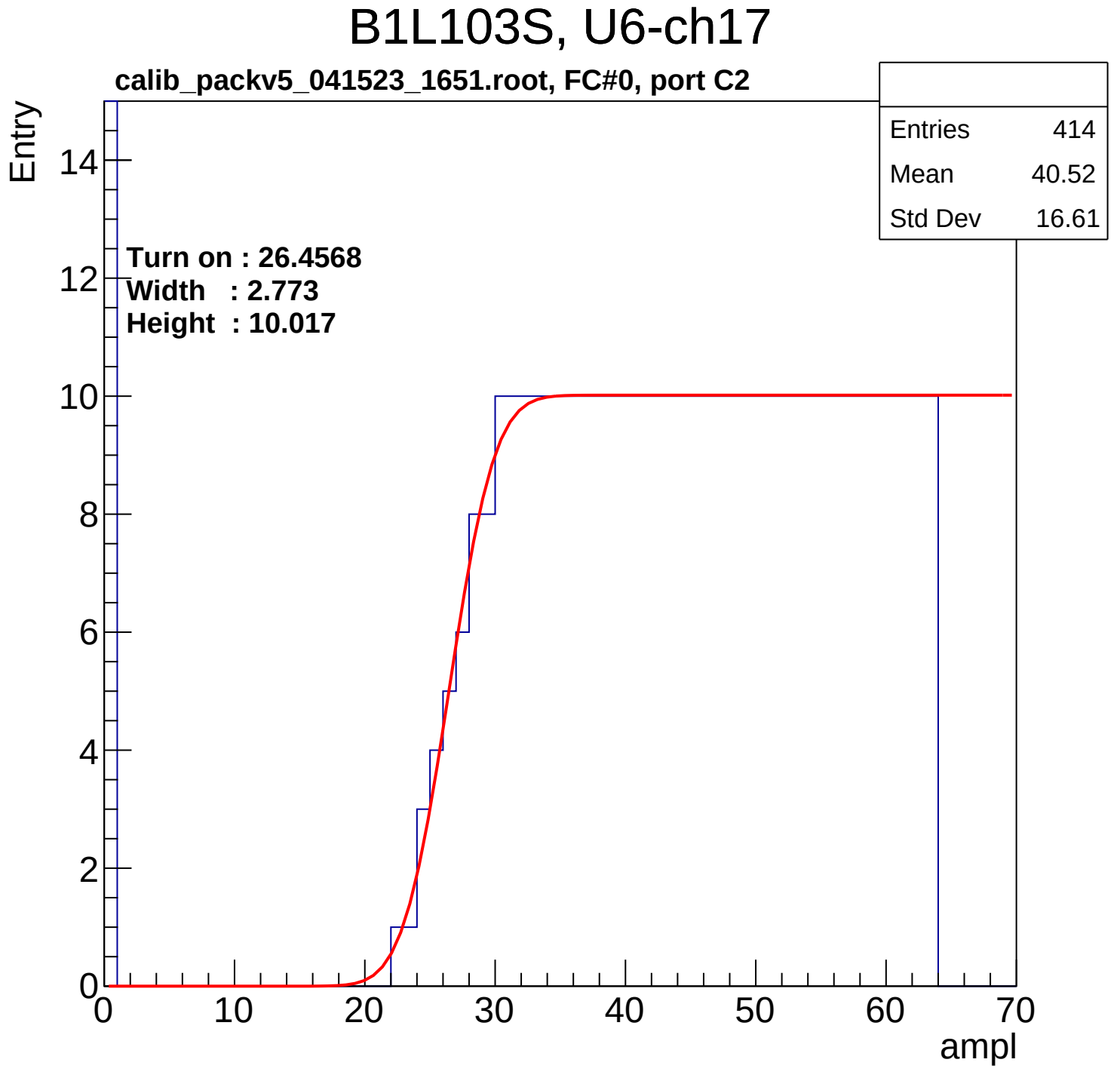

B1L103S, U6-ch12
calib_packv5_041523_1651.root, FC#0, port C2
Entries 424
Mean 39.84
Std Dev 17.04
Turn on : 26.4073
Width : 4.385
Height : 10.082
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

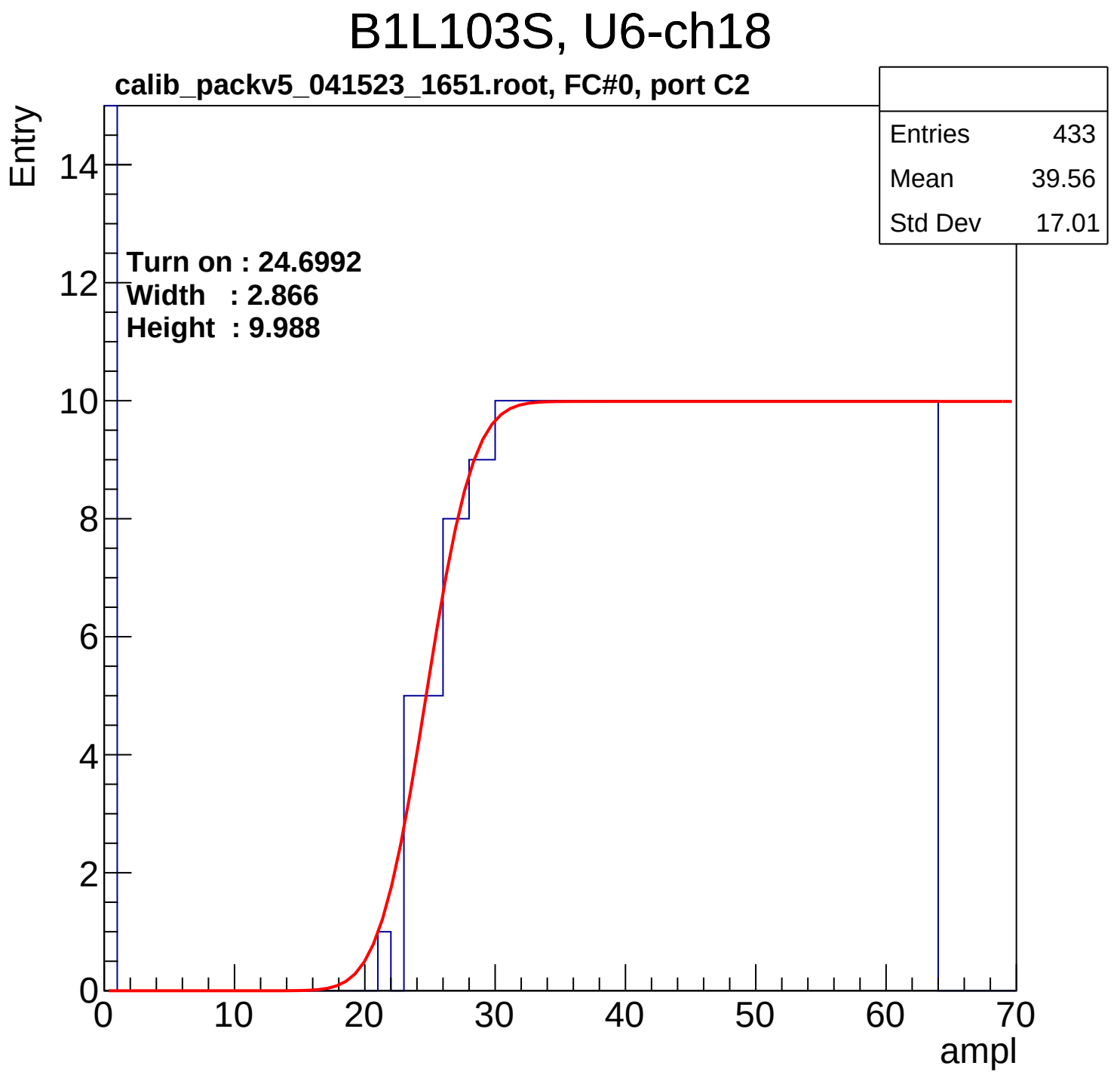

B1L103S, U6-ch13
calib_packv5_041523_1651.root, FC#0, port C2
Entries 427
Mean 40.16
Std Dev 16.39
Turn on : 25.4090
Width : 3.119
Height : 10.048
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

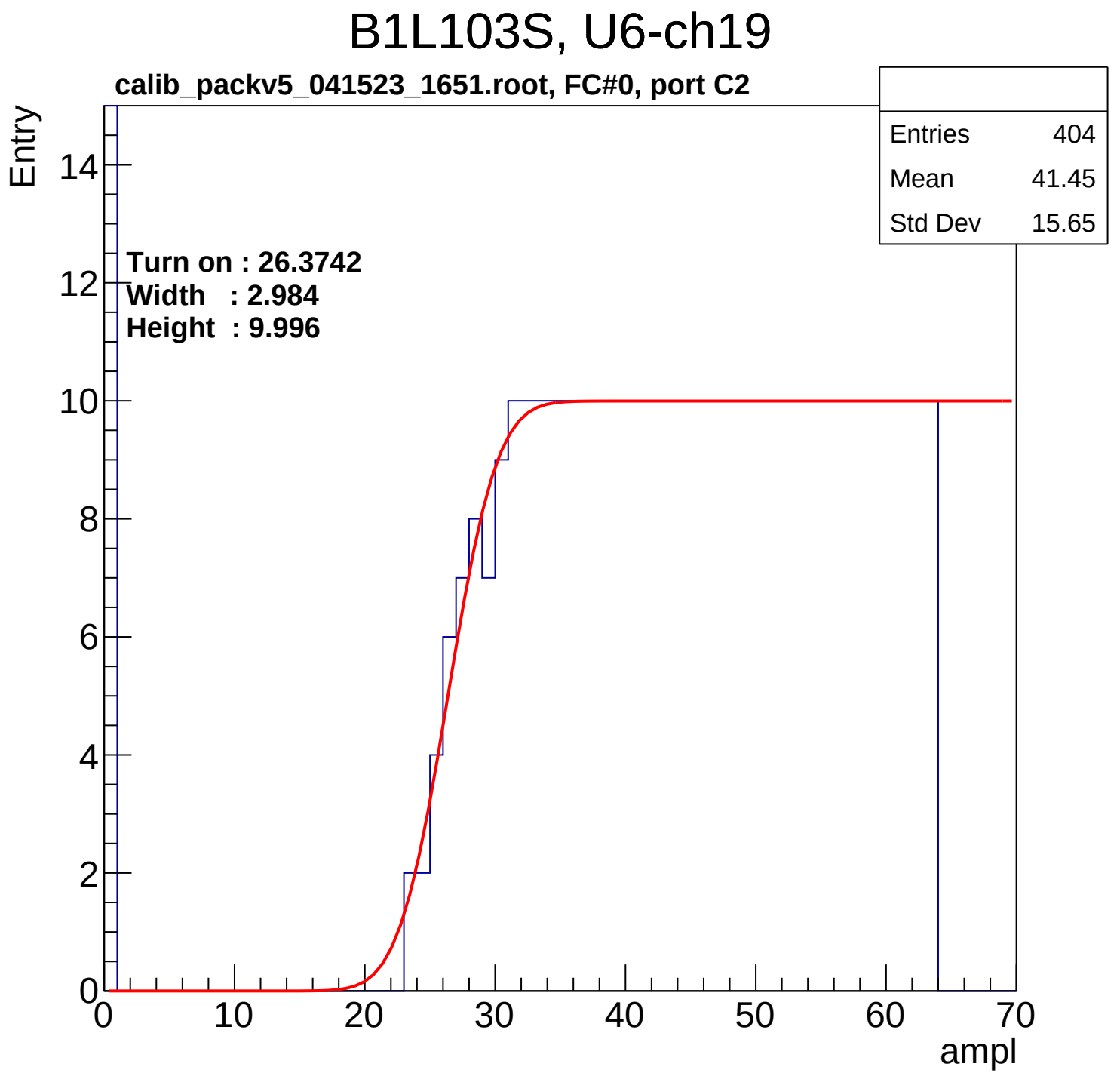

B1L103S, U6-ch14
calib_packv5_041523_1651.root, FC#0, port C2
Entries 432
Mean 39.81
Std Dev 16.66
Turn on : 25.4045
Width : 2.906
Height : 10.065
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

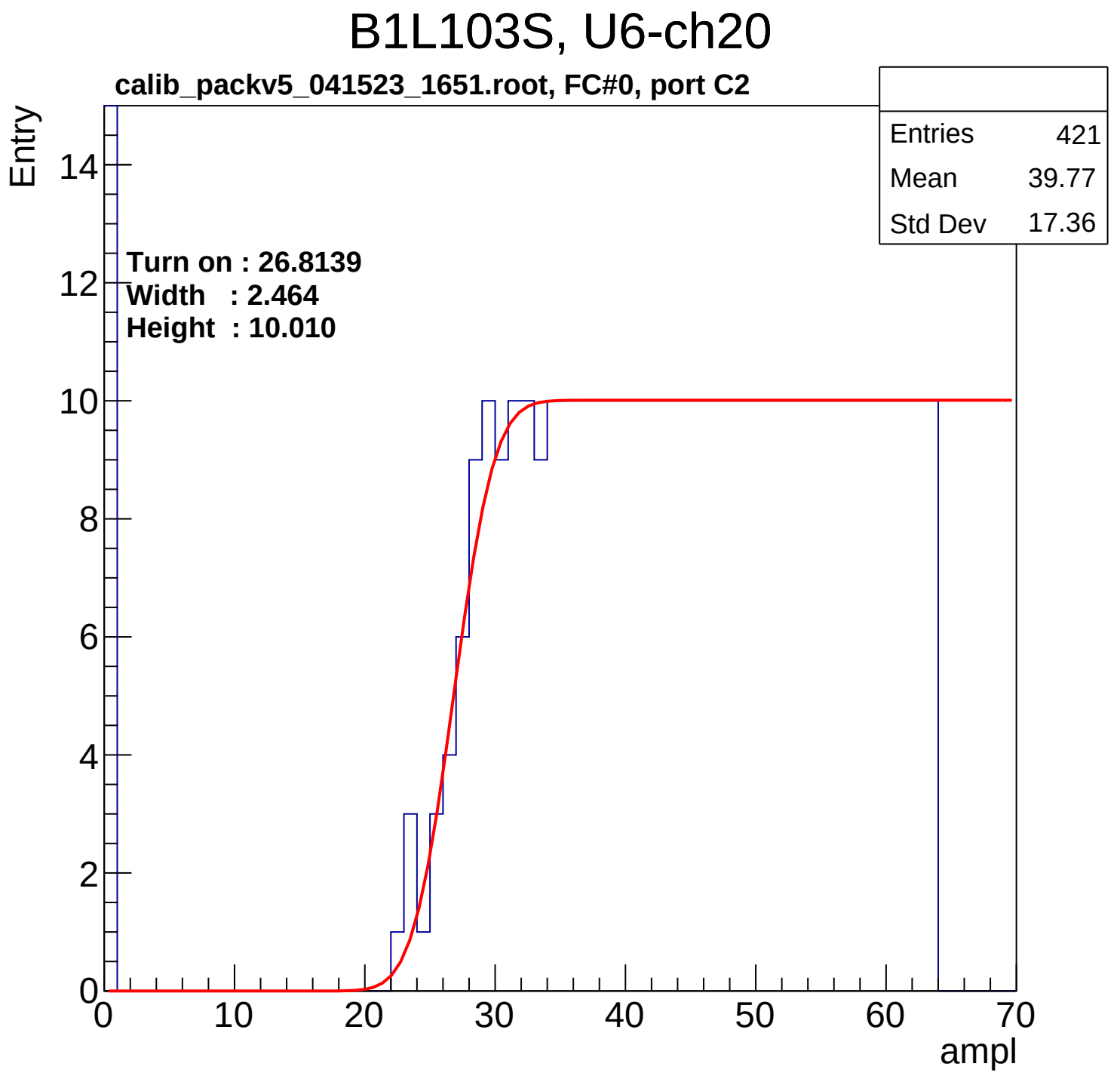

B1L103S, U6-ch15
calib_packv5_041523_1651.root, FC#0, port C2
Entries 417
Mean 40.51
Std Dev 16.42
Turn on : 26.3348
Width : 3.920
Height : 10.097
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

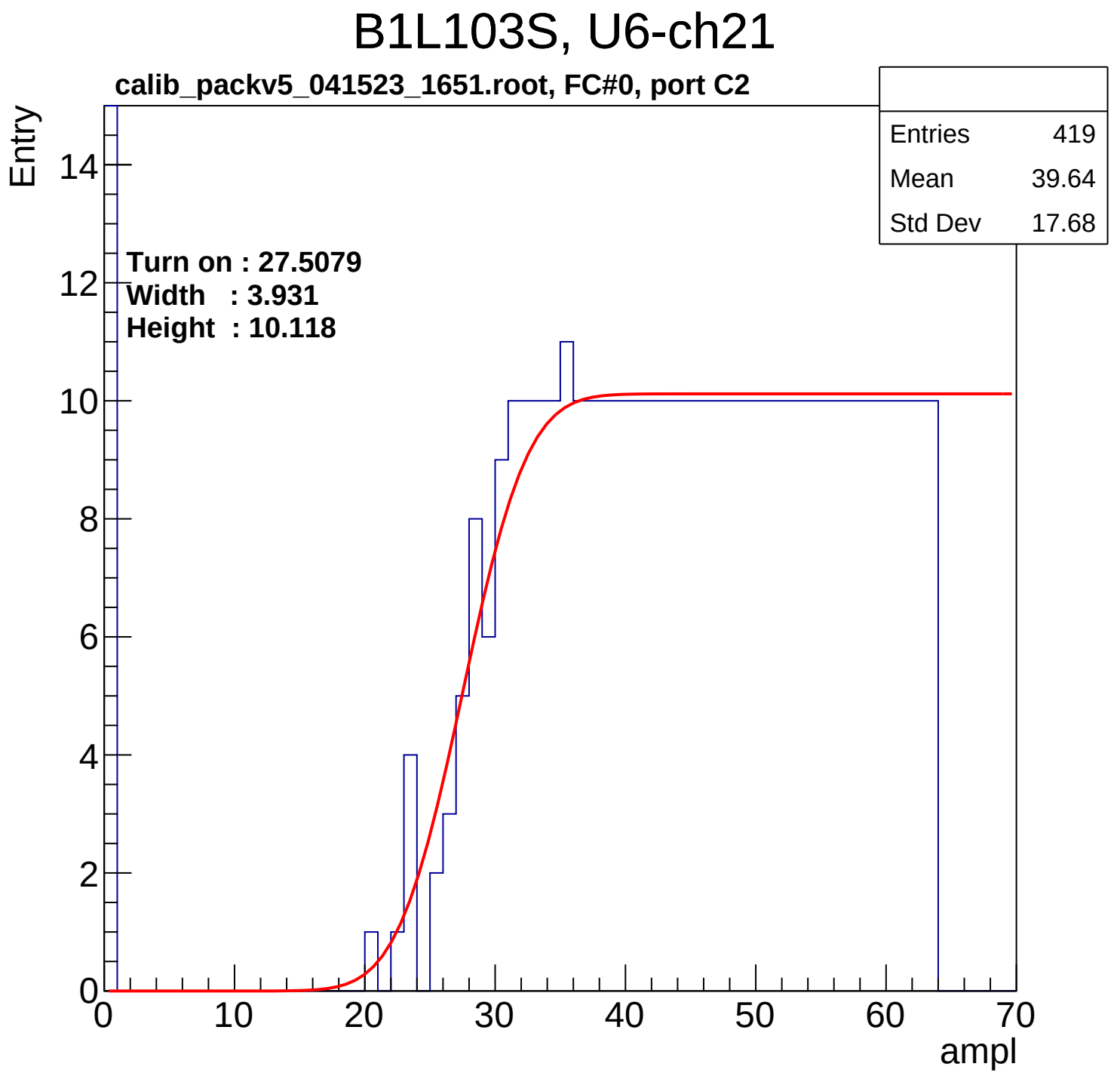

B1L103S, U6-ch16
calib_packv5_041523_1651.root, FC#0, port C2
Entries 438
Mean 39.25
Std Dev 17.28
Turn on : 25.2404
Width : 1.706
Height : 9.988
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

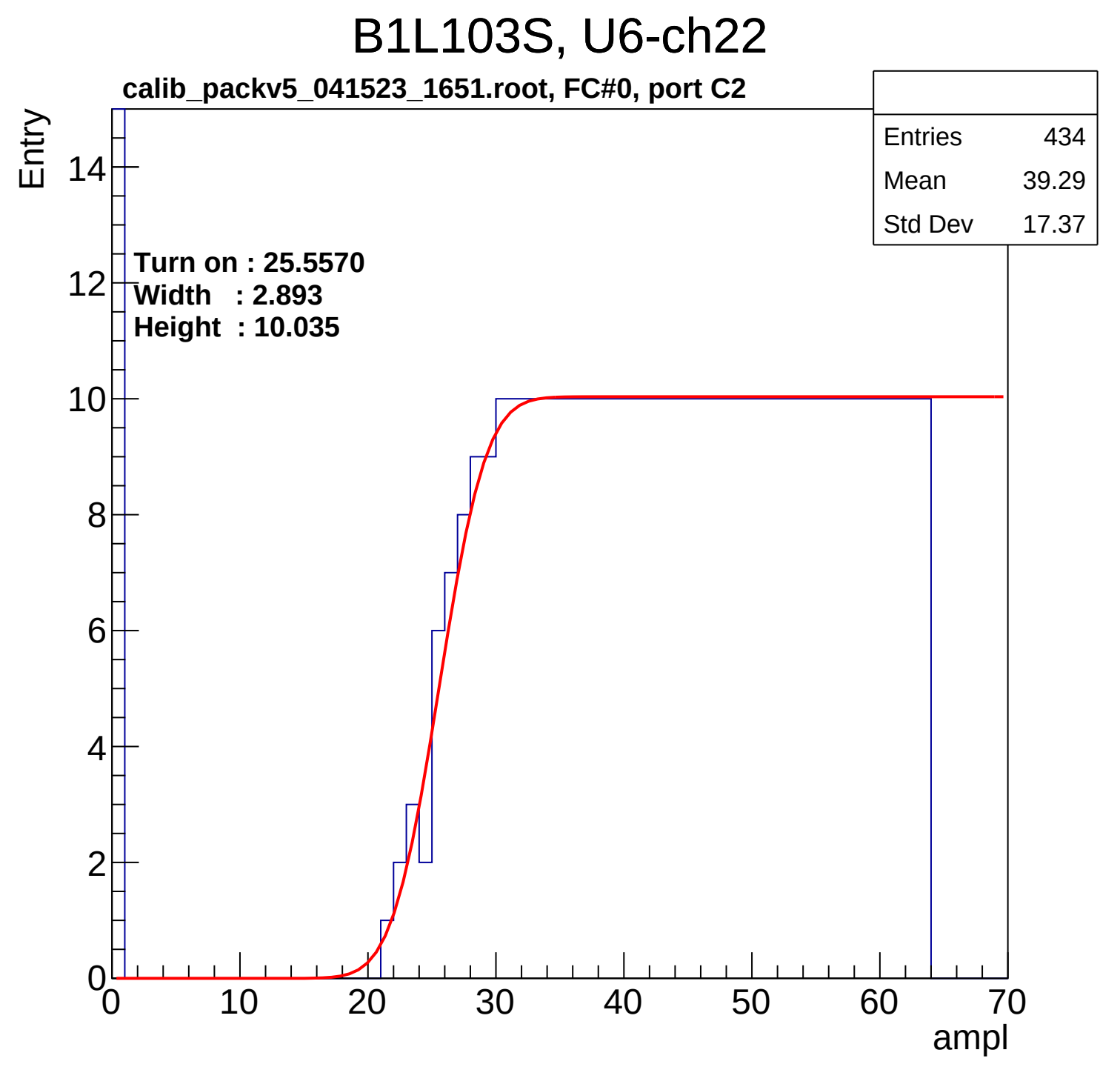

B1L103S, U6-ch17
calib_packv5_041523_1651.root, FC#0, port C2
Entries 414
Mean 40.52
Std Dev 16.61
Turn on : 26.4568
Width : 2.773
Height : 10.017
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

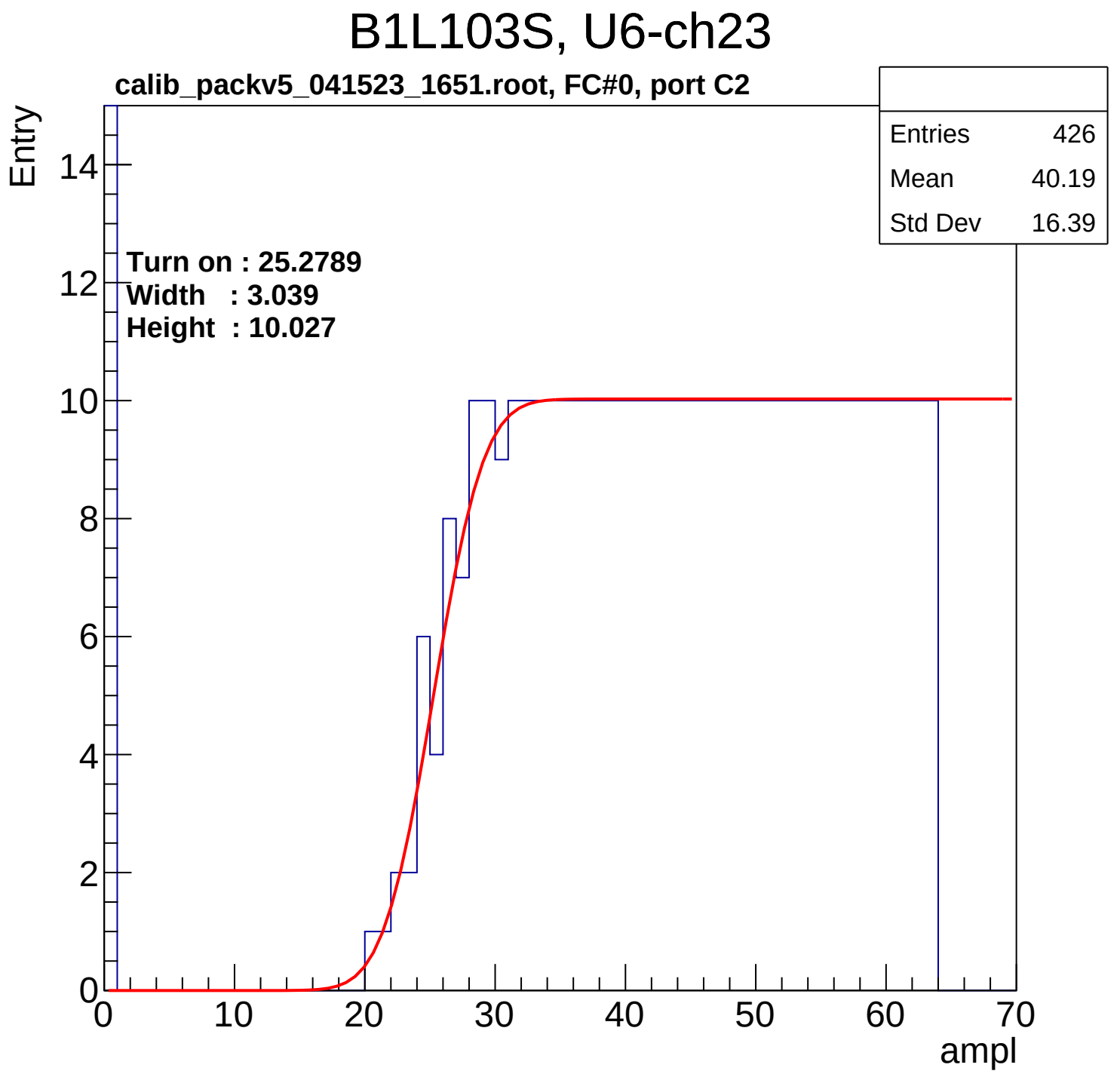

B1L103S, U6-ch18
calib_packv5_041523_1651.root, FC#0, port C2
Entries 433
Mean 39.56
Std Dev 17.01
Turn on : 24.6992
Width : 2.866
Height : 9.988
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

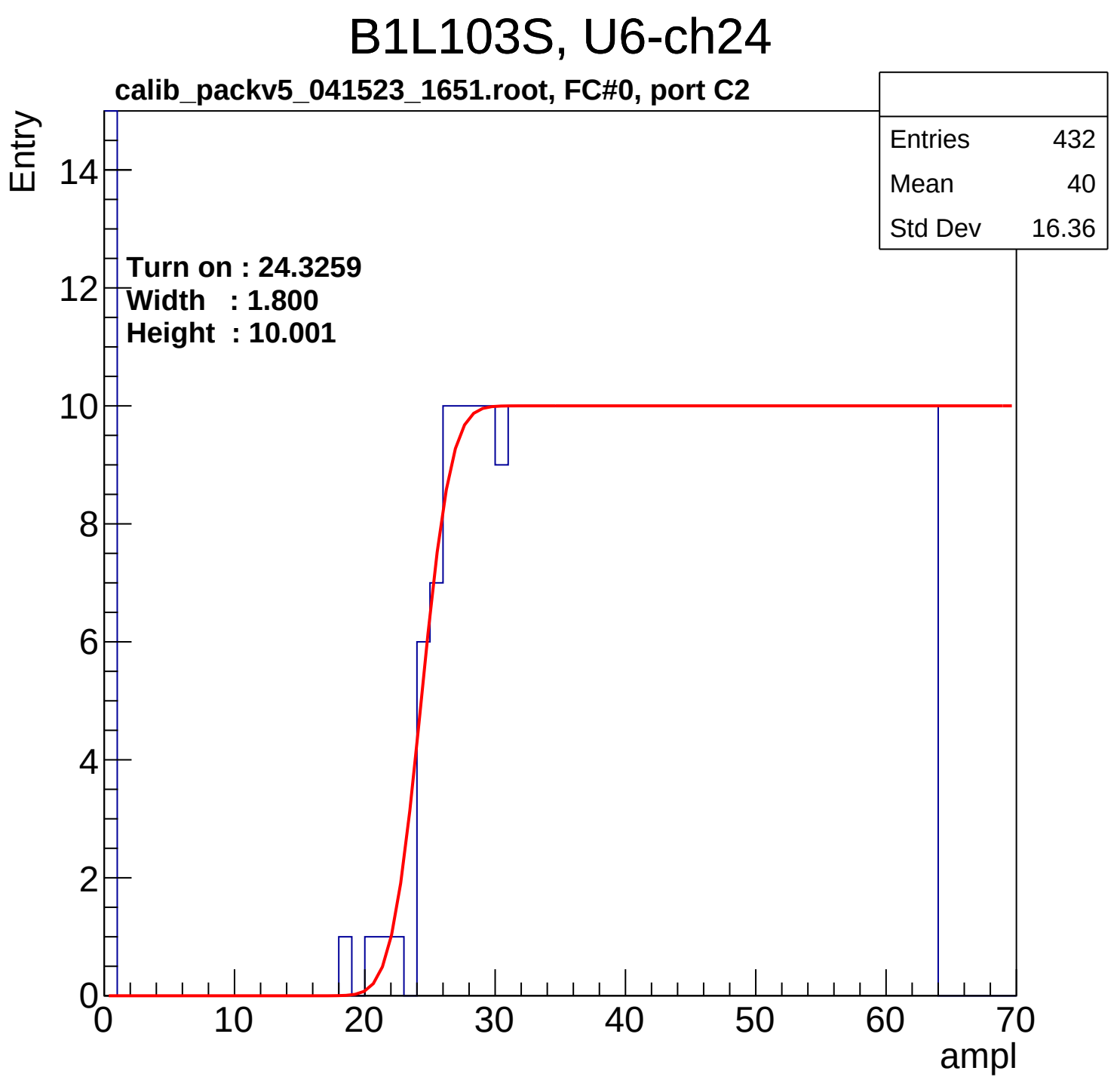

B1L103S, U6-ch19
calib_packv5_041523_1651.root, FC#0, port C2
Entries 404
Mean 41.45
Std Dev 15.65
Turn on : 26.3742
Width : 2.984
Height : 9.996
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

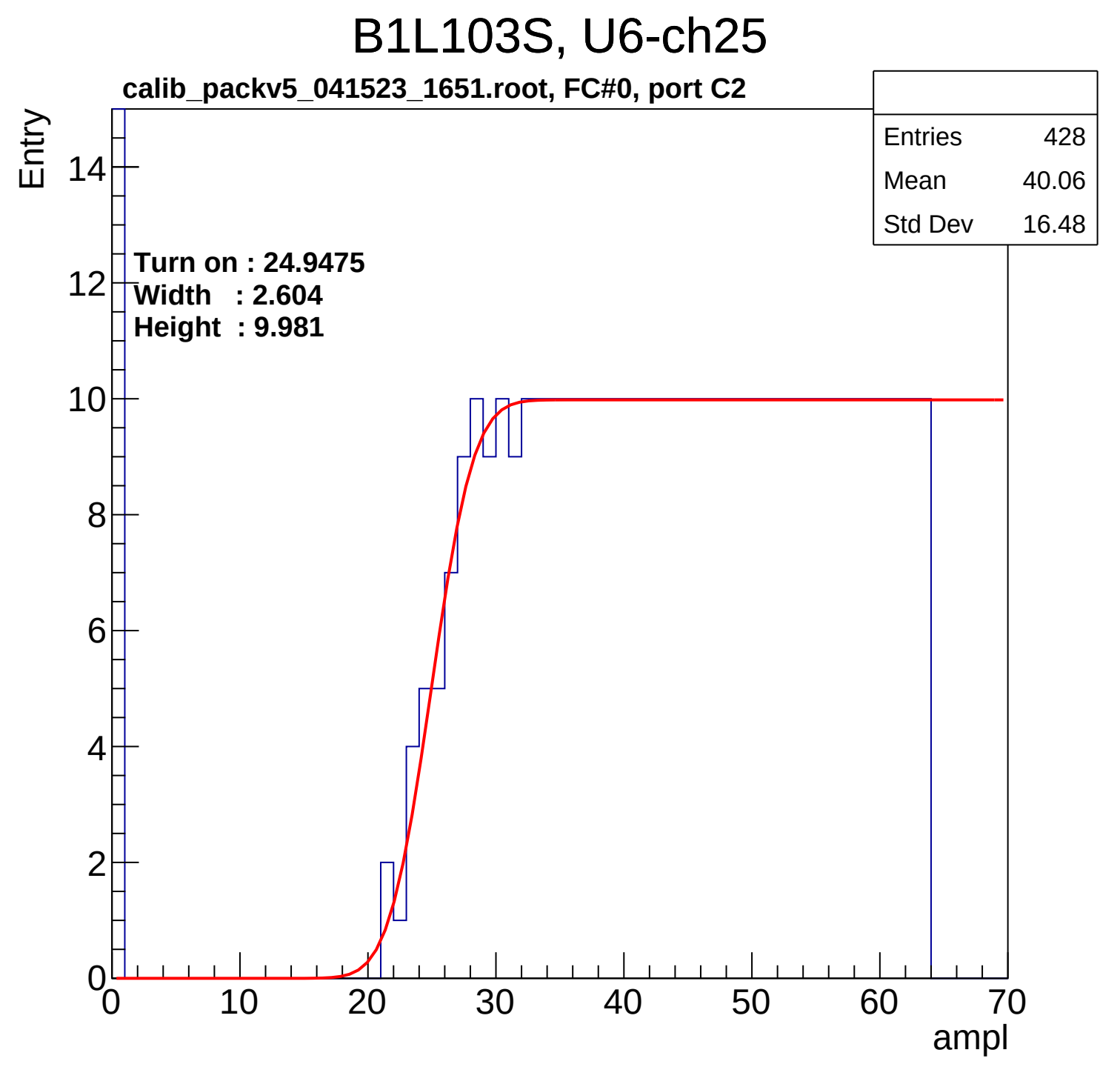

B1L103S, U6-ch20
calib_packv5_041523_1651.root, FC#0, port C2
Entries 421
Mean 39.77
Std Dev 17.36
Turn on : 26.8139
Width : 2.464
Height : 10.010
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

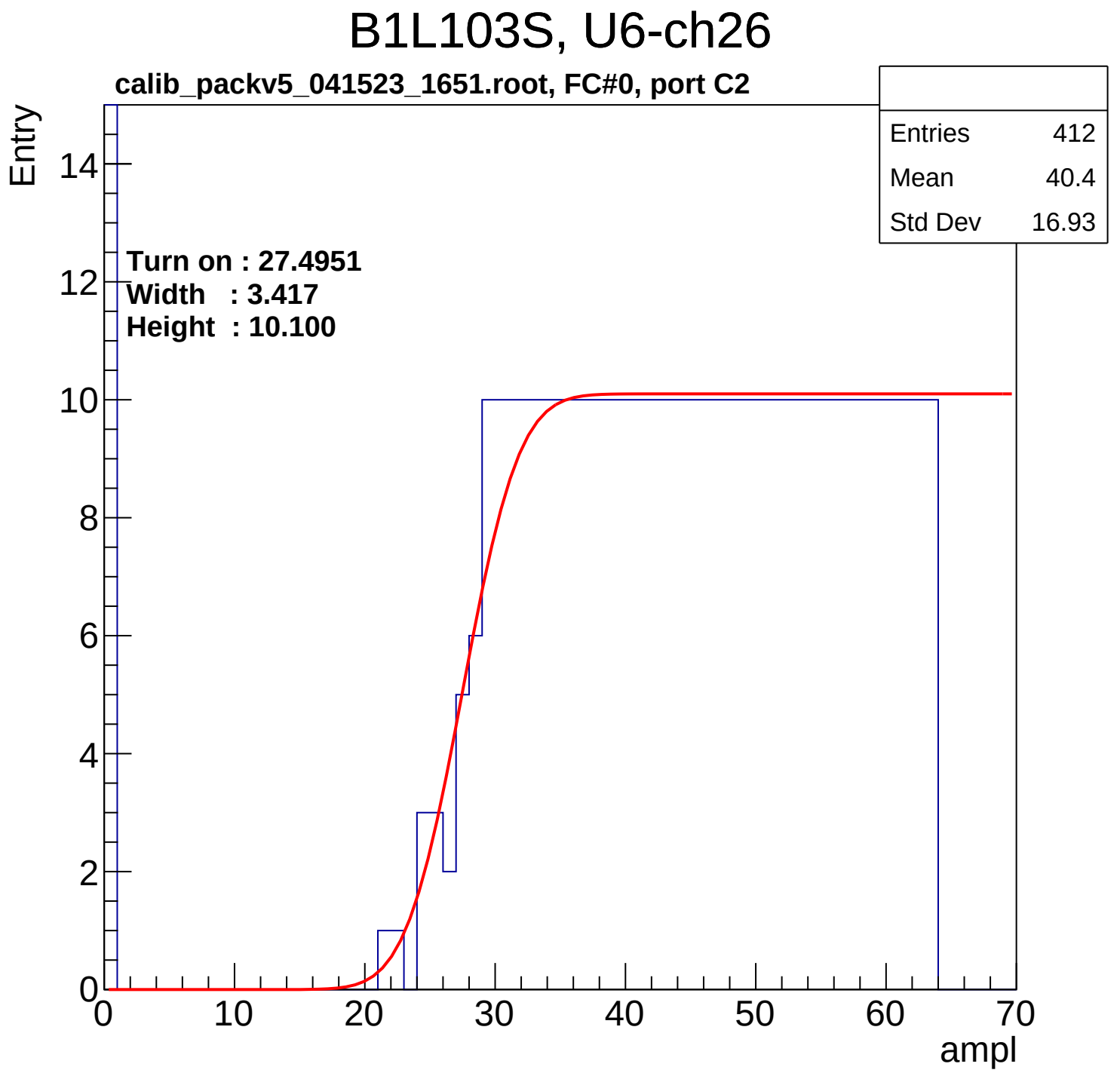

B1L103S, U6-ch21
calib_packv5_041523_1651.root, FC#0, port C2
Entries 419
Mean 39.64
Std Dev 17.68
Turn on : 27.5079
Width : 3.931
Height : 10.118
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

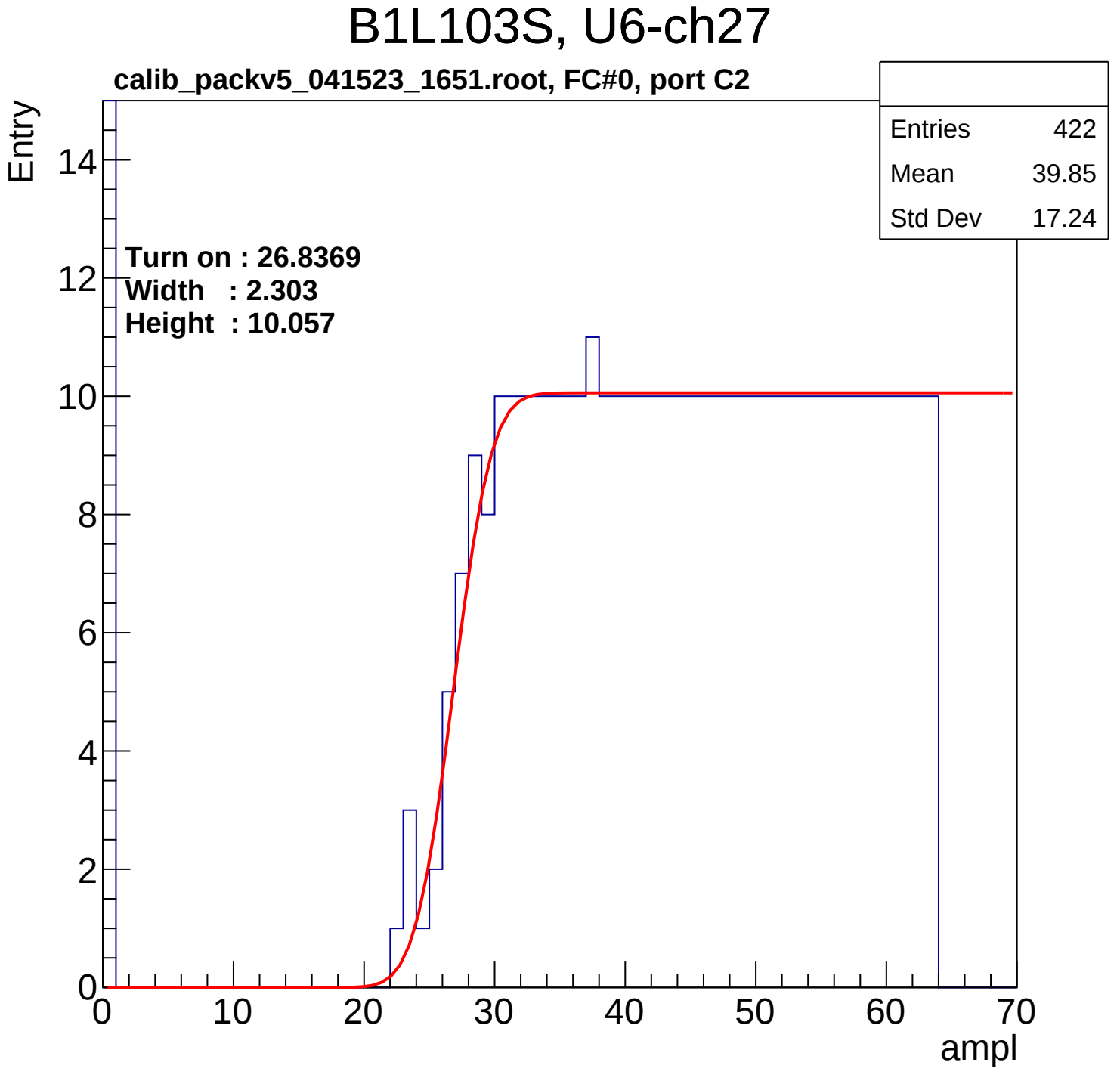

B1L103S, U6-ch22
calib_packv5_041523_1651.root, FC#0, port C2
Entries 434
Mean 39.29
Std Dev 17.37
Turn on : 25.5570
Width : 2.893
Height : 10.035
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

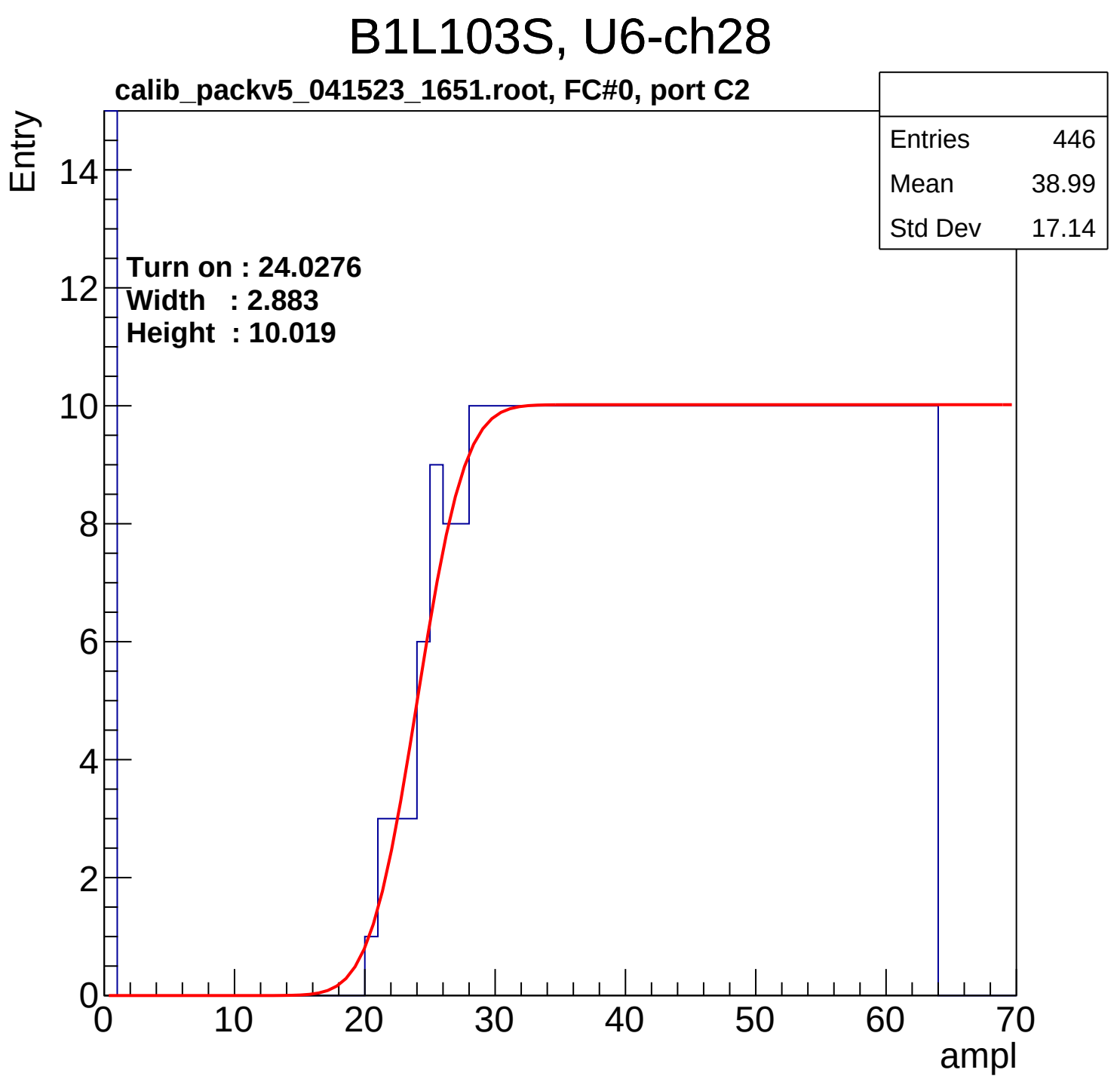

B1L103S, U6-ch23
calib_packv5_041523_1651.root, FC#0, port C2
Entries 426
Mean 40.19
Std Dev 16.39
Turn on : 25.2789
Width : 3.039
Height : 10.027
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

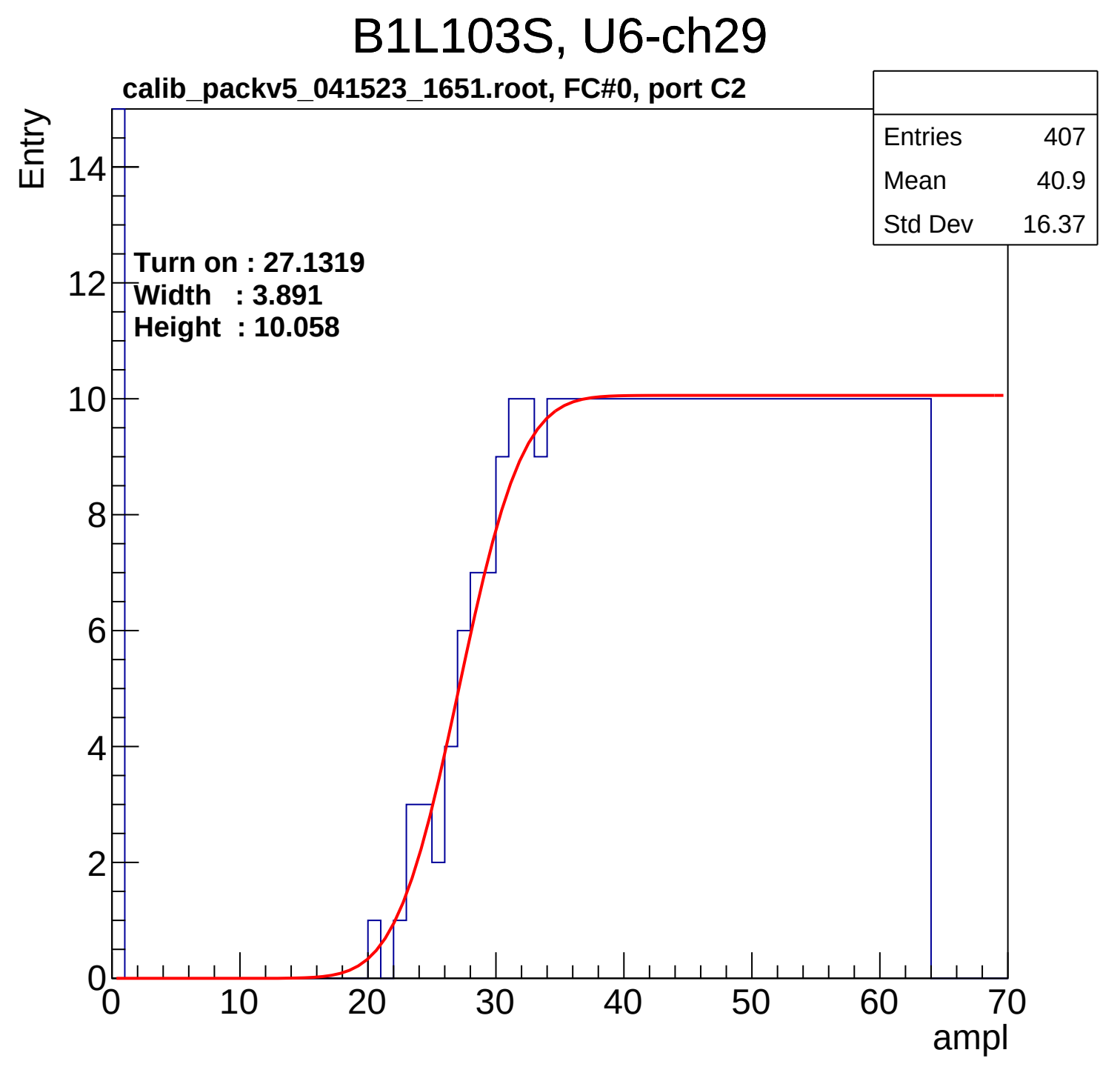

B1L103S, U6-ch24
calib_packv5_041523_1651.root, FC#0, port C2
Entries 432
Mean 40
Std Dev 16.36
Turn on : 24.3259
Width : 1.800
Height : 10.001
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

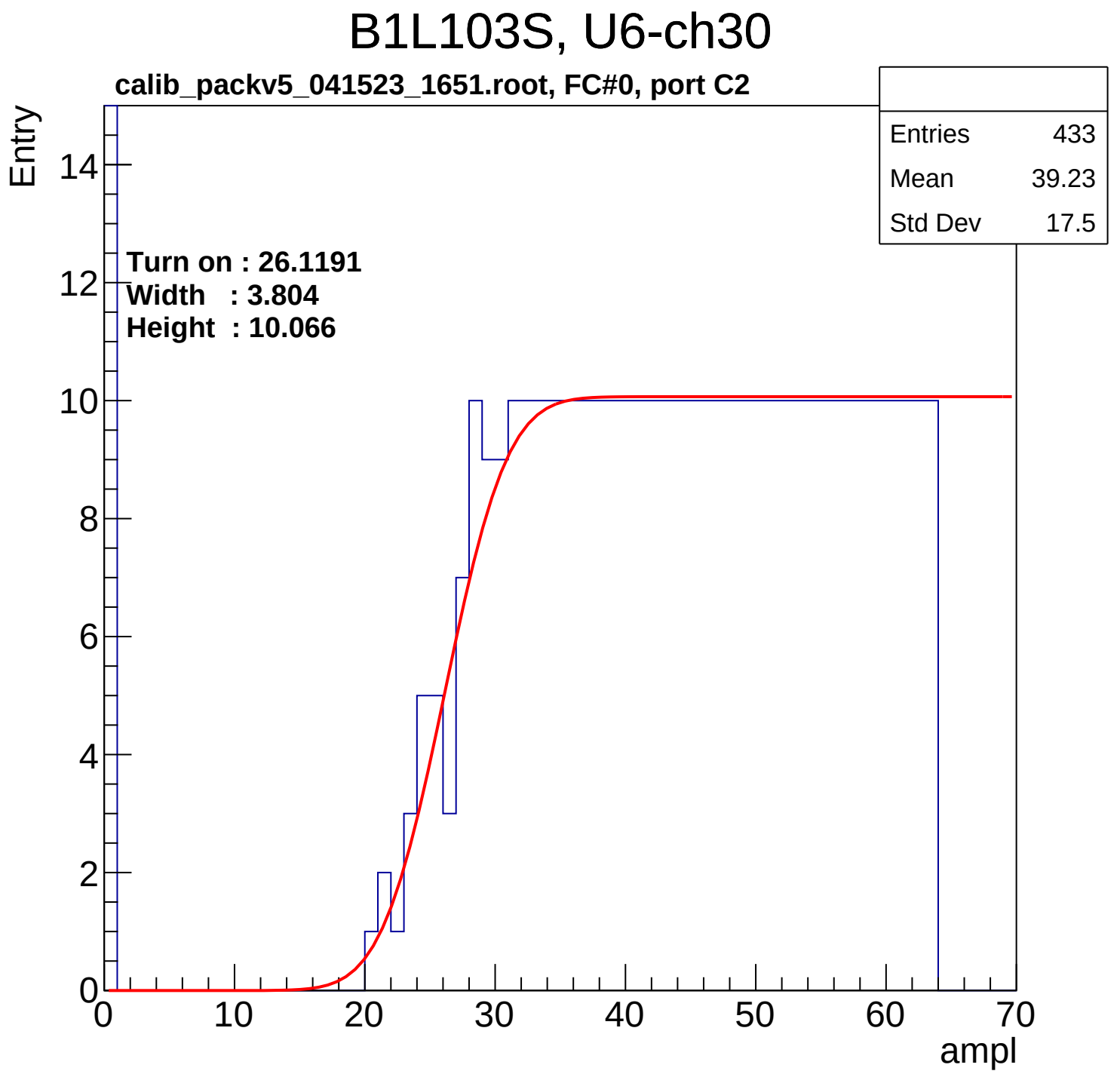

B1L103S, U6-ch25
calib_packv5_041523_1651.root, FC#0, port C2
Entries 428
Mean 40.06
Std Dev 16.48
Turn on : 24.9475
Width : 2.604
Height : 9.981
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

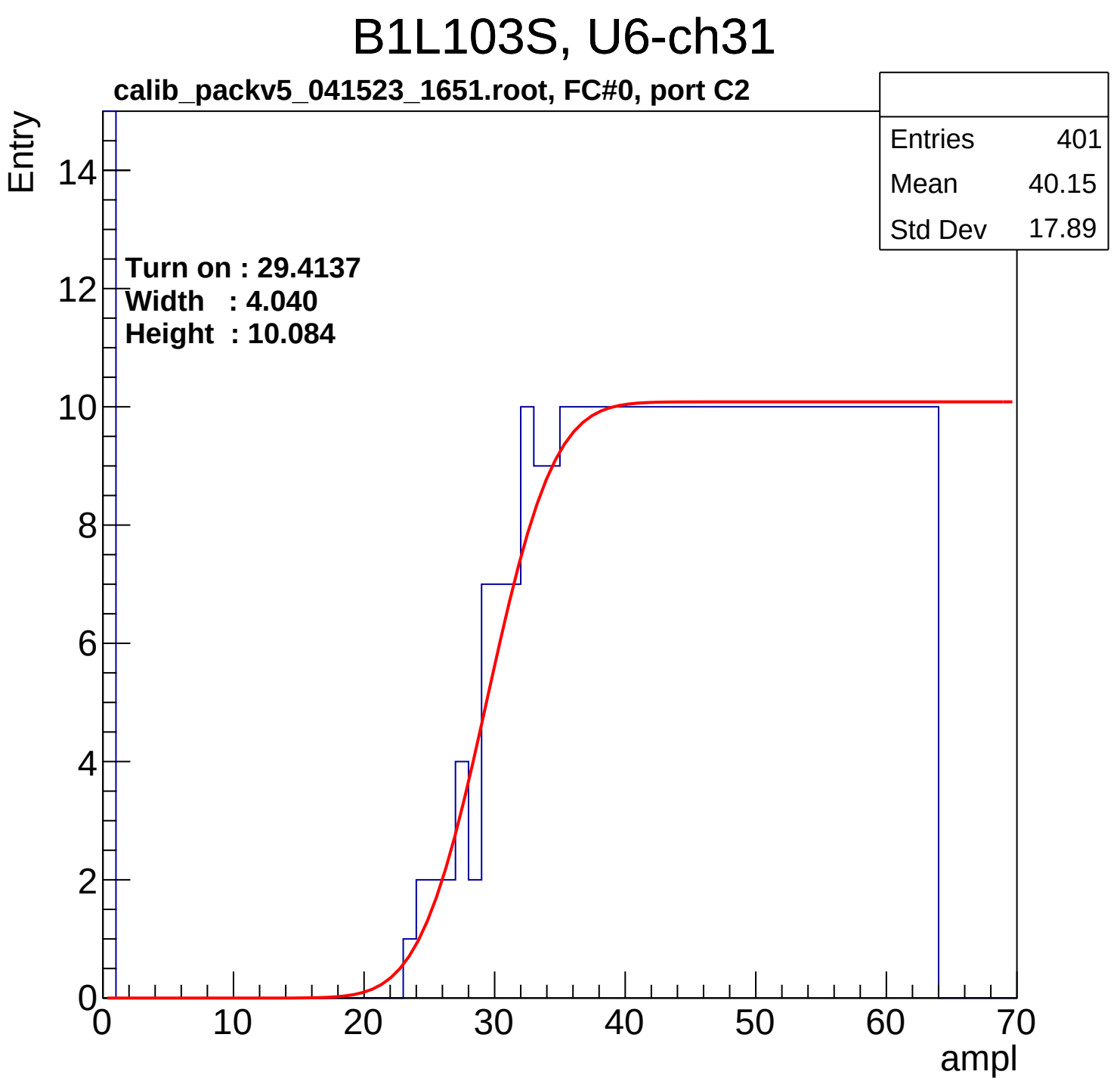

B1L103S, U6-ch26
calib_packv5_041523_1651.root, FC#0, port C2
Entries 412
Mean 40.4
Std Dev 16.93
Turn on : 27.4951
Width : 3.417
Height : 10.100
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

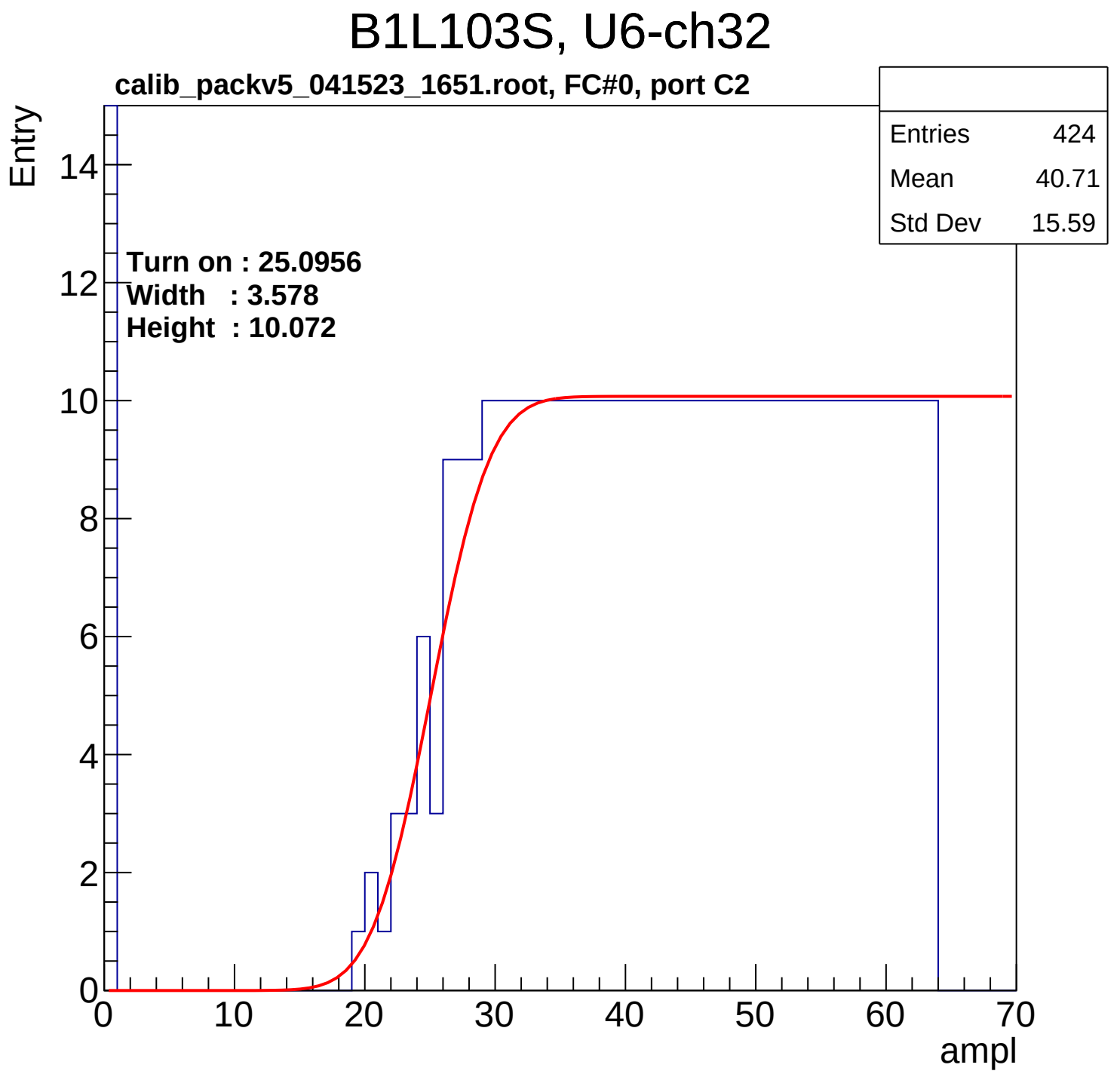

B1L103S, U6-ch27
calib_packv5_041523_1651.root, FC#0, port C2
Entries 422
Mean 39.85
Std Dev 17.24
Turn on : 26.8369
Width : 2.303
Height : 10.057
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

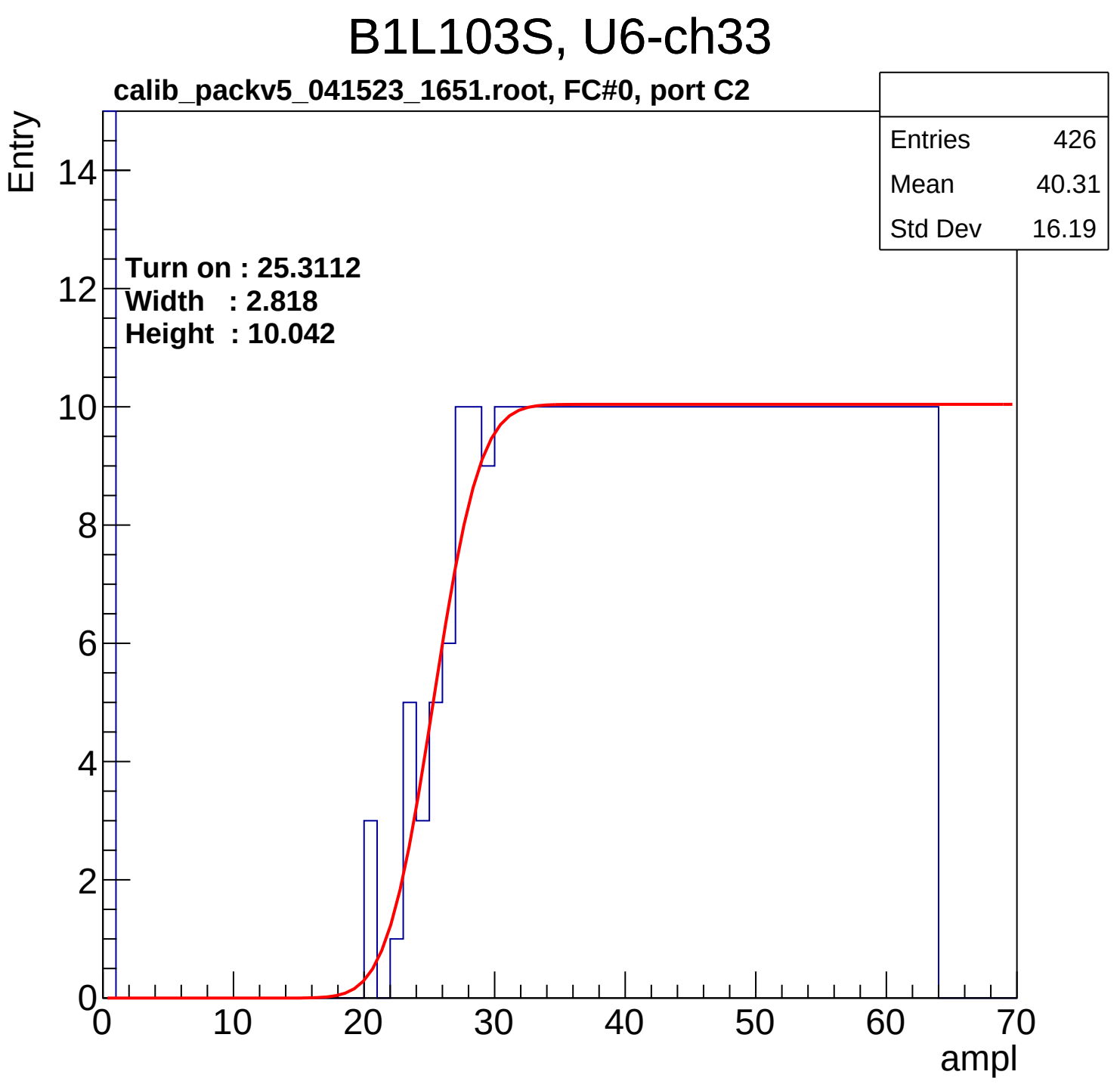

B1L103S, U6-ch28
calib_packv5_041523_1651.root, FC#0, port C2
Entries 446
Mean 38.99
Std Dev 17.14
Turn on : 24.0276
Width : 2.883
Height : 10.019
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

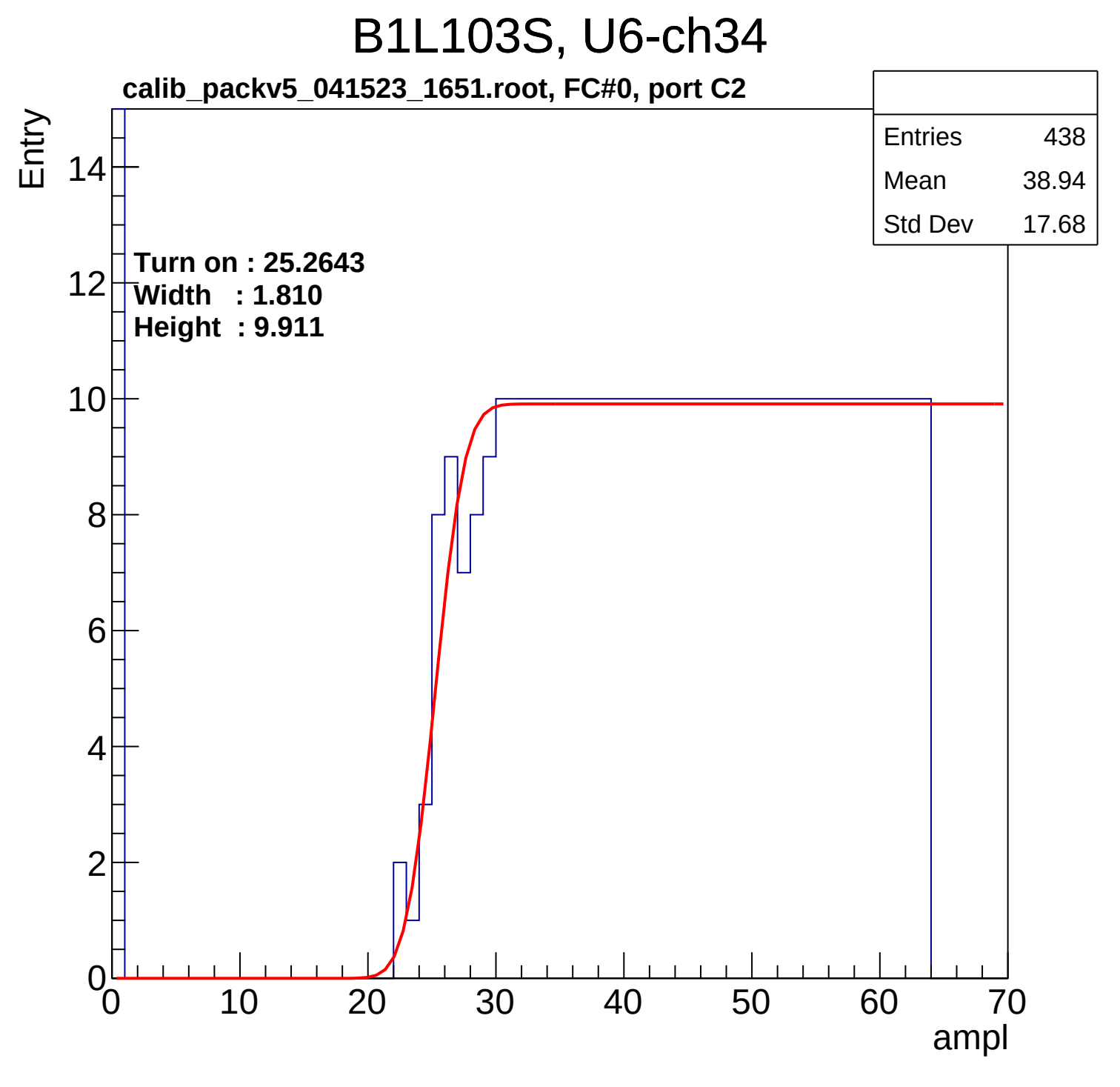

B1L103S, U6-ch29
calib_packv5_041523_1651.root, FC#0, port C2
Entries 407
Mean 40.9
Std Dev 16.37
Turn on : 27.1319
Width : 3.891
Height : 10.058
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

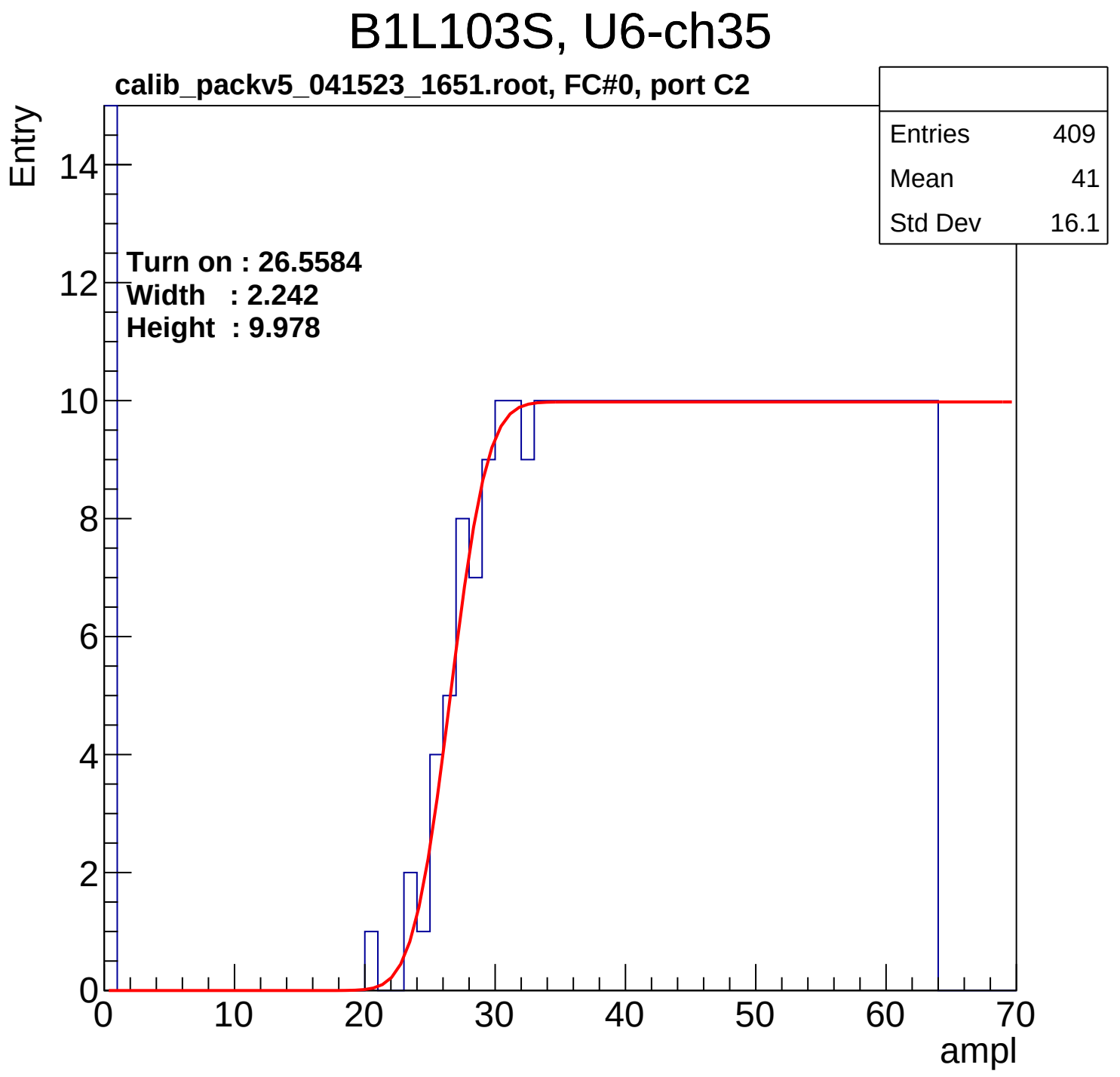

B1L103S, U6-ch30
calib_packv5_041523_1651.root, FC#0, port C2
Entries 433
Mean 39.23
Std Dev 17.5
Turn on : 26.1191
Width : 3.804
Height : 10.066
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

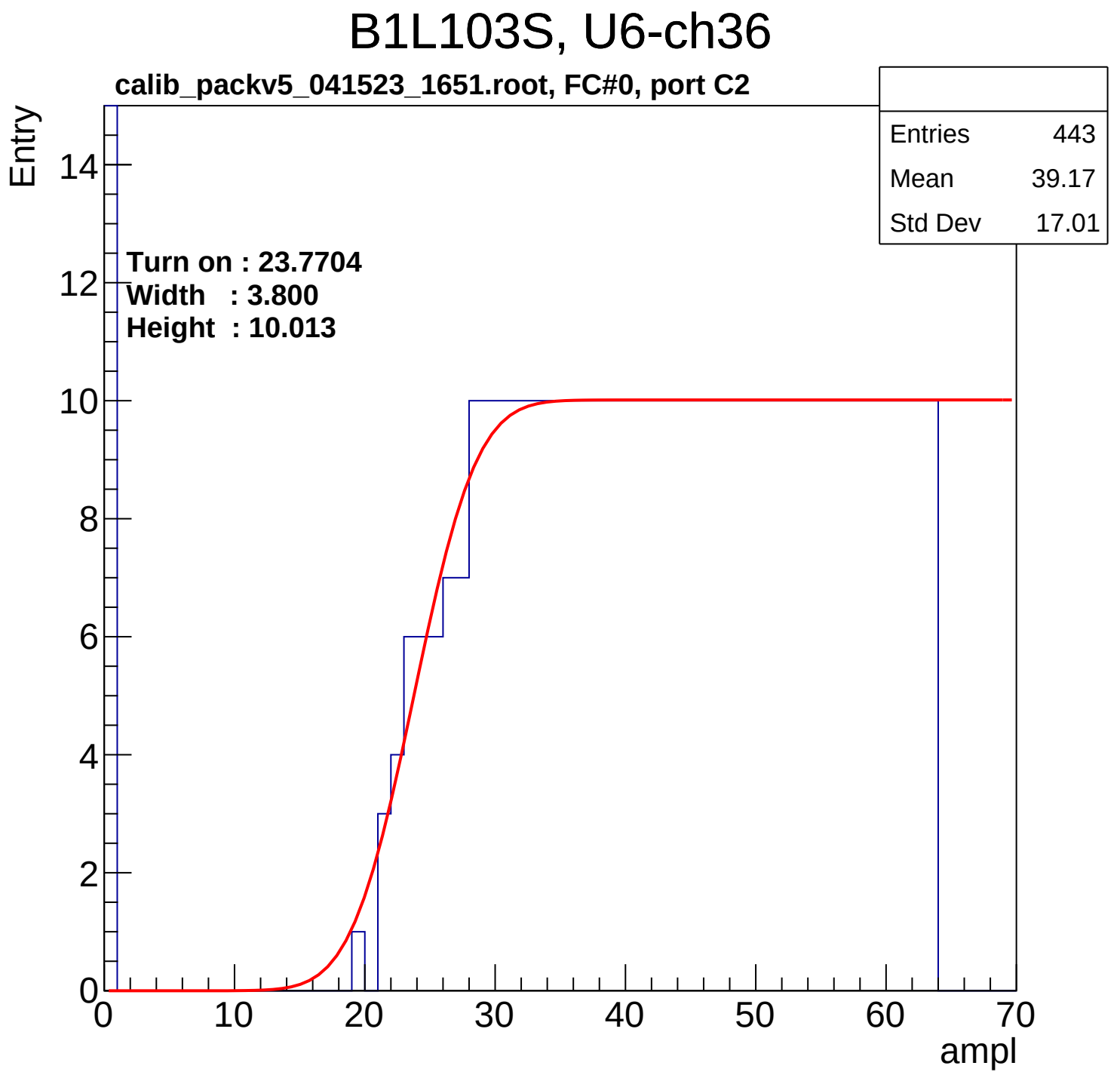

B1L103S, U6-ch31
calib_packv5_041523_1651.root, FC#0, port C2
Entries 401
Mean 40.15
Std Dev 17.89
Turn on : 29.4137
Width : 4.040
Height : 10.084
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

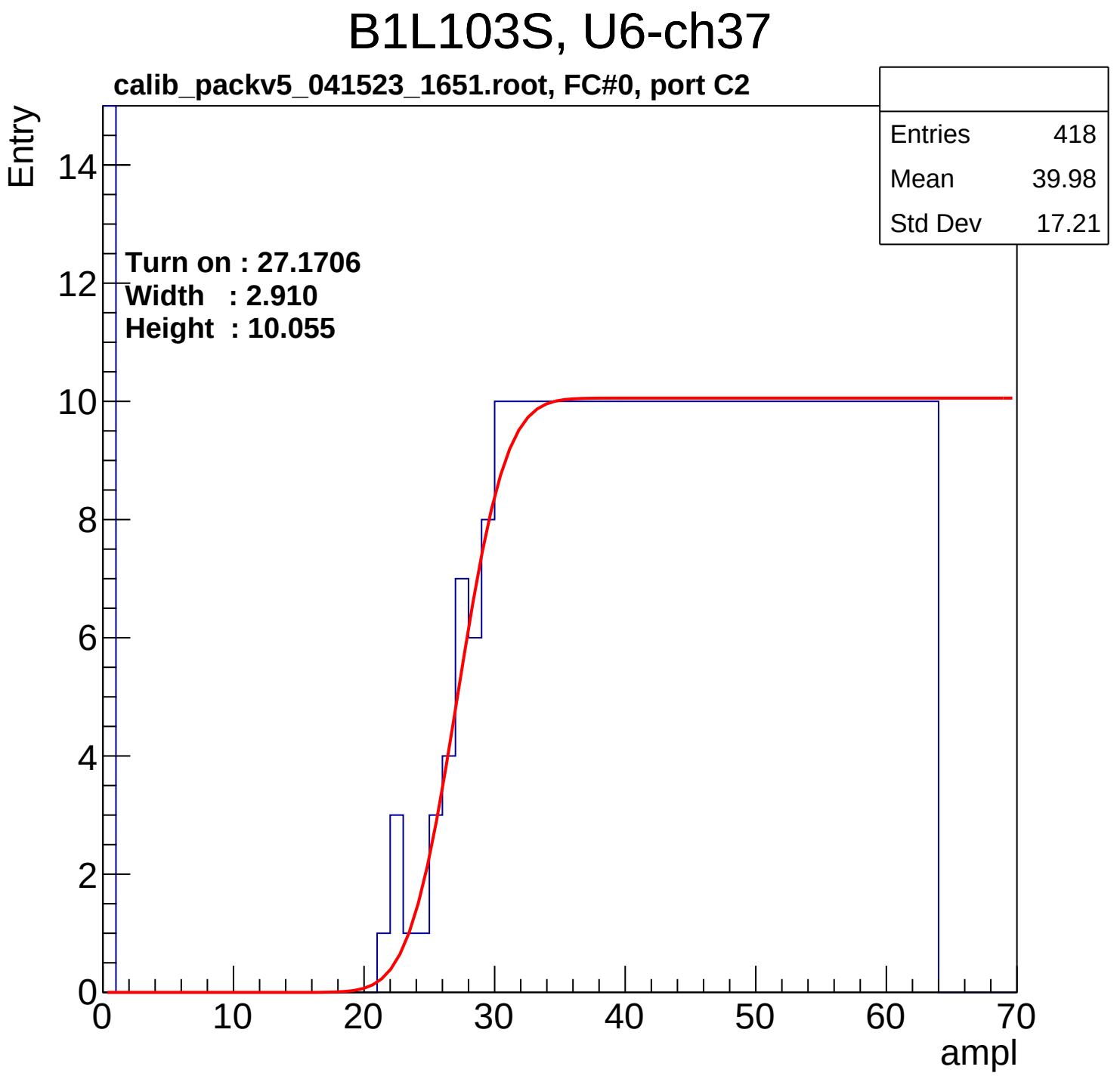

B1L103S, U6-ch32
calib_packv5_041523_1651.root, FC#0, port C2
Entries 424
Mean 40.71
Std Dev 15.59
Turn on : 25.0956
Width : 3.578
Height : 10.072
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

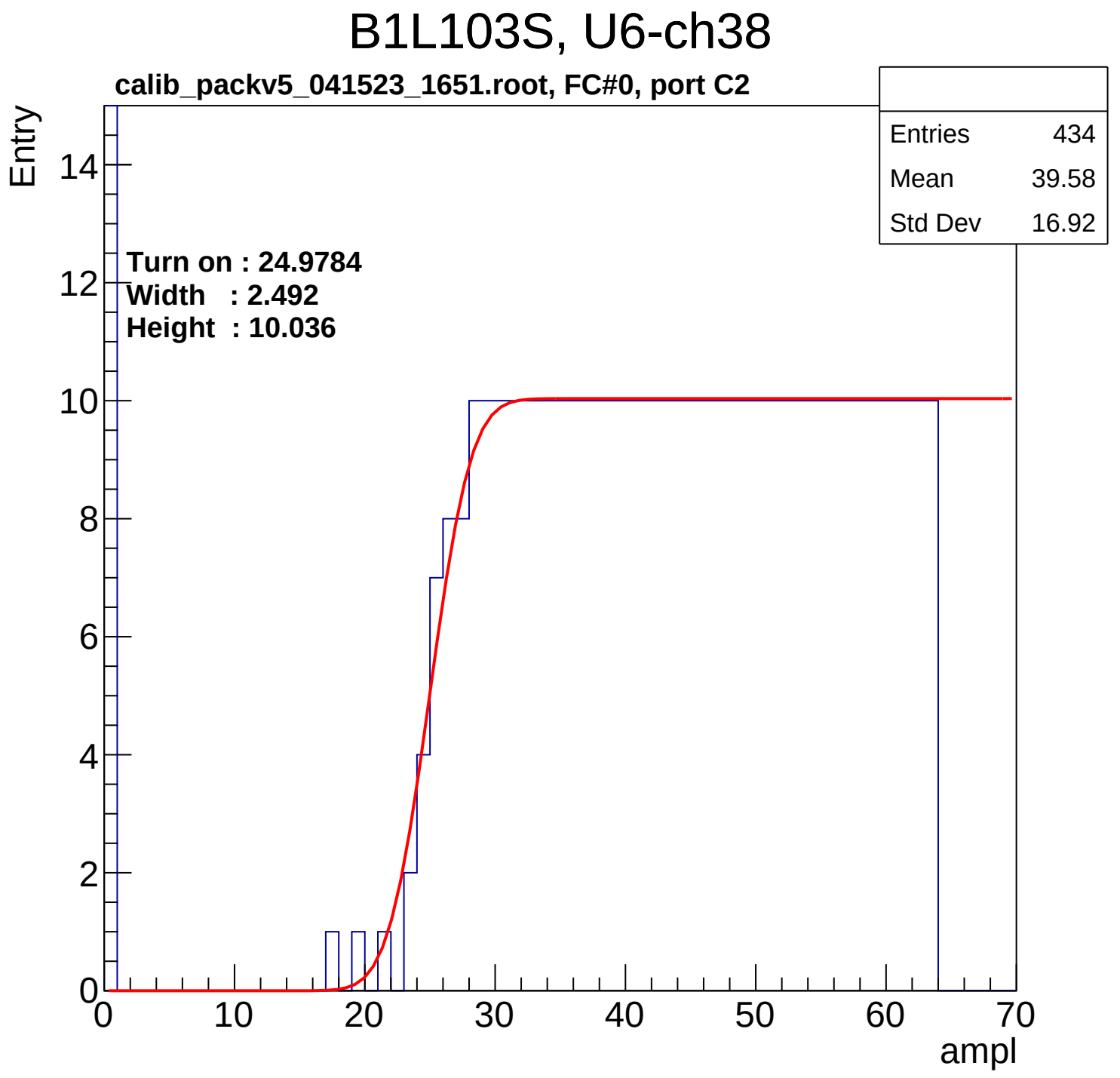

B1L103S, U6-ch33
calib_packv5_041523_1651.root, FC#0, port C2
Entries 426
Mean 40.31
Std Dev 16.19
Turn on : 25.3112
Width : 2.818
Height : 10.042
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

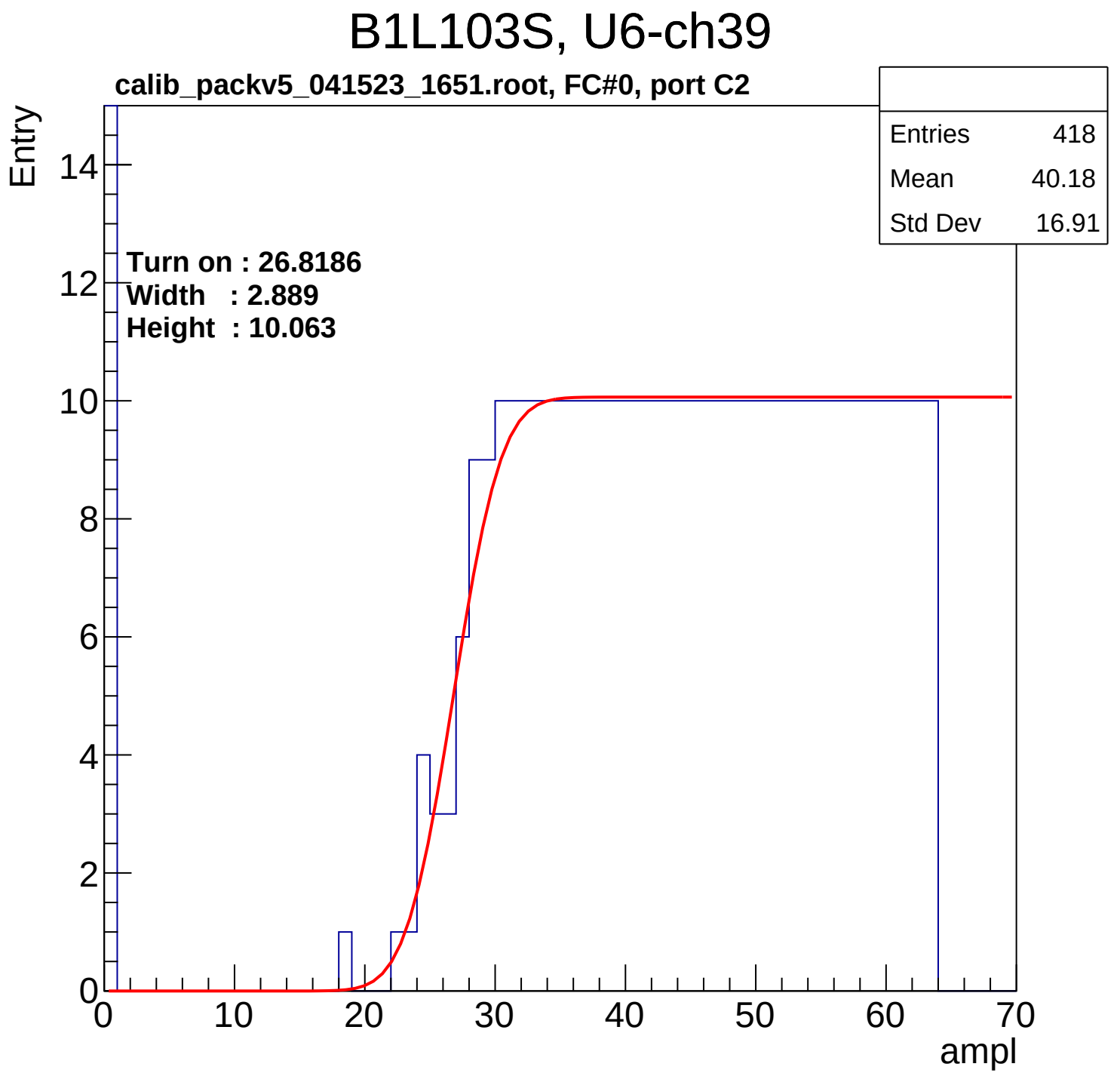

B1L103S, U6-ch34
calib_packv5_041523_1651.root, FC#0, port C2
Entries 438
Mean 38.94
Std Dev 17.68
Turn on : 25.2643
Width : 1.810
Height : 9.911
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

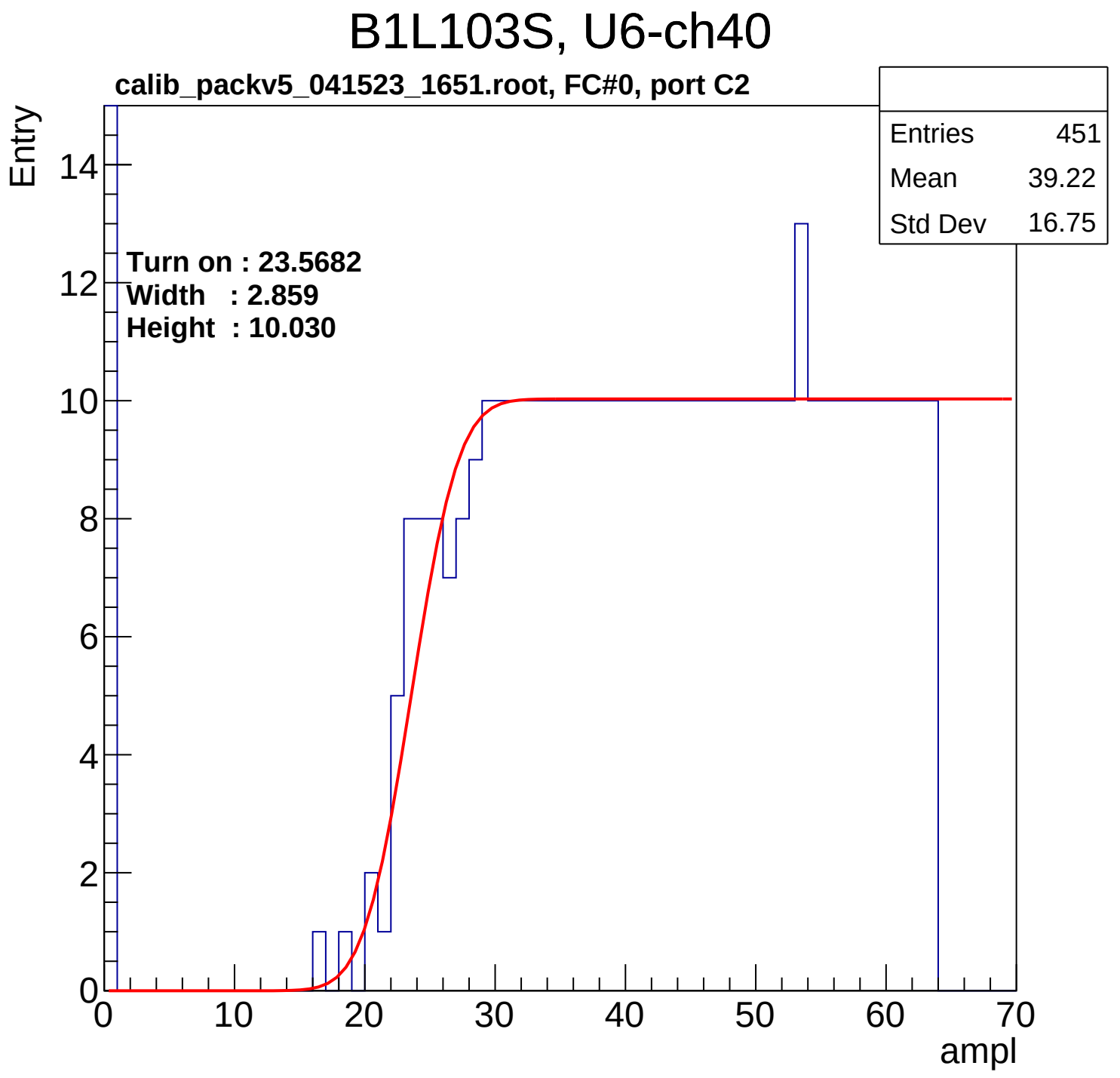

B1L103S, U6-ch35
calib_packv5_041523_1651.root, FC#0, port C2
Entries 409
Mean 41
Std Dev 16.1
Turn on : 26.5584
Width : 2.242
Height : 9.978
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

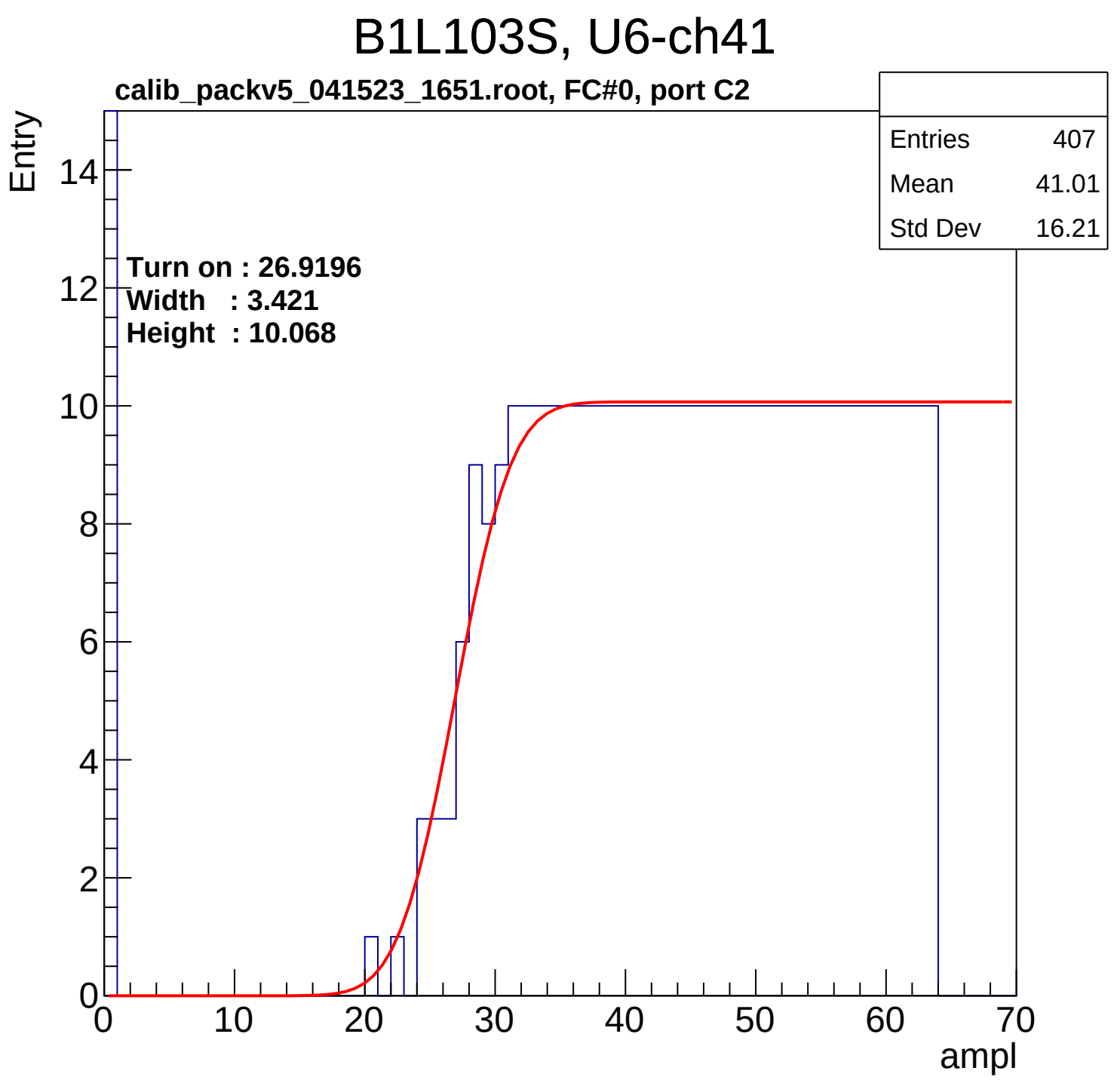

B1L103S, U6-ch36
calib_packv5_041523_1651.root, FC#0, port C2
Entries 443
Mean 39.17
Std Dev 17.01
Turn on : 23.7704
Width : 3.800
Height : 10.013
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

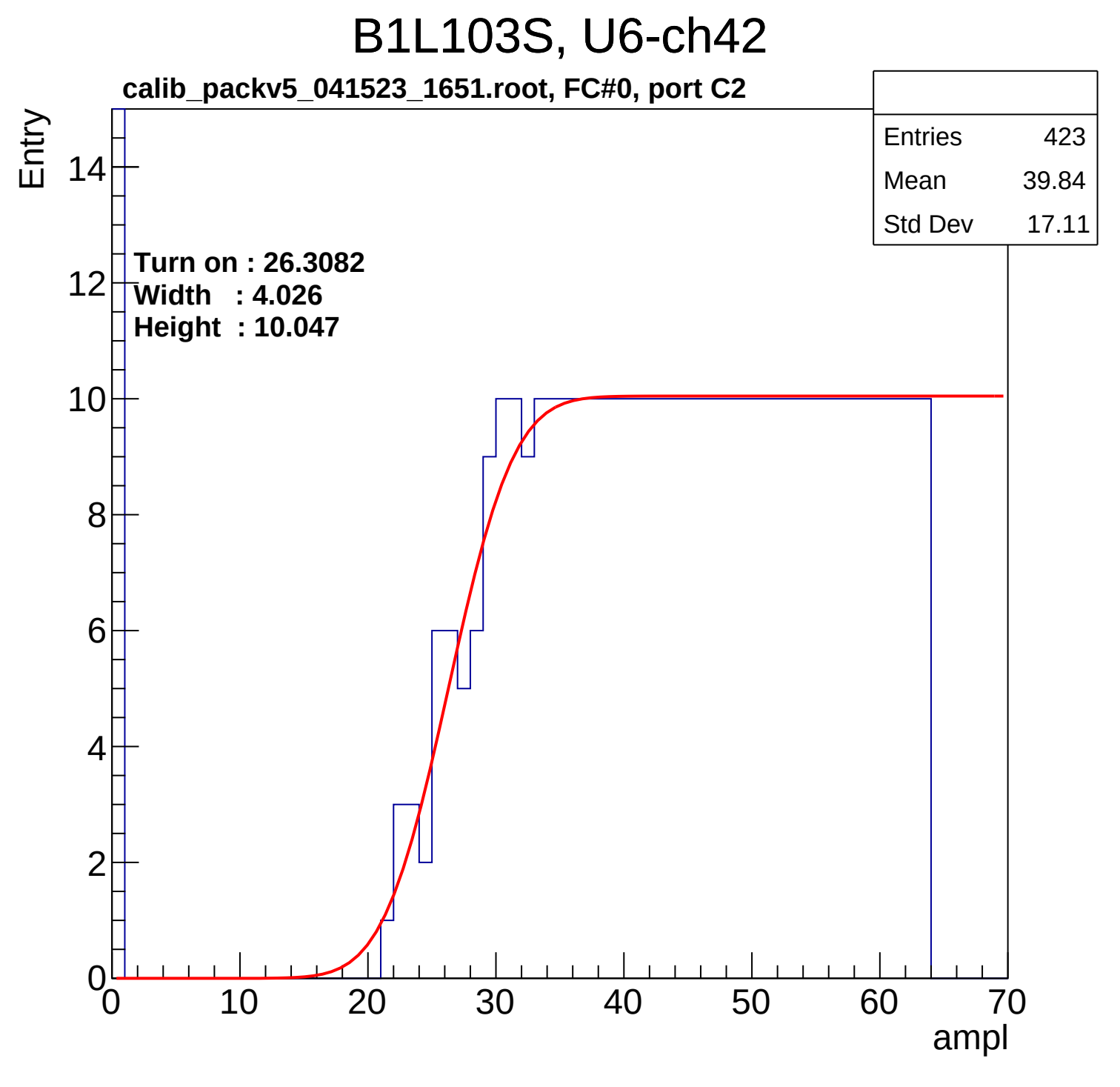

B1L103S, U6-ch37
calib_packv5_041523_1651.root, FC#0, port C2
Entries 418
Mean 39.98
Std Dev 17.21
Turn on : 27.1706
Width : 2.910
Height : 10.055
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

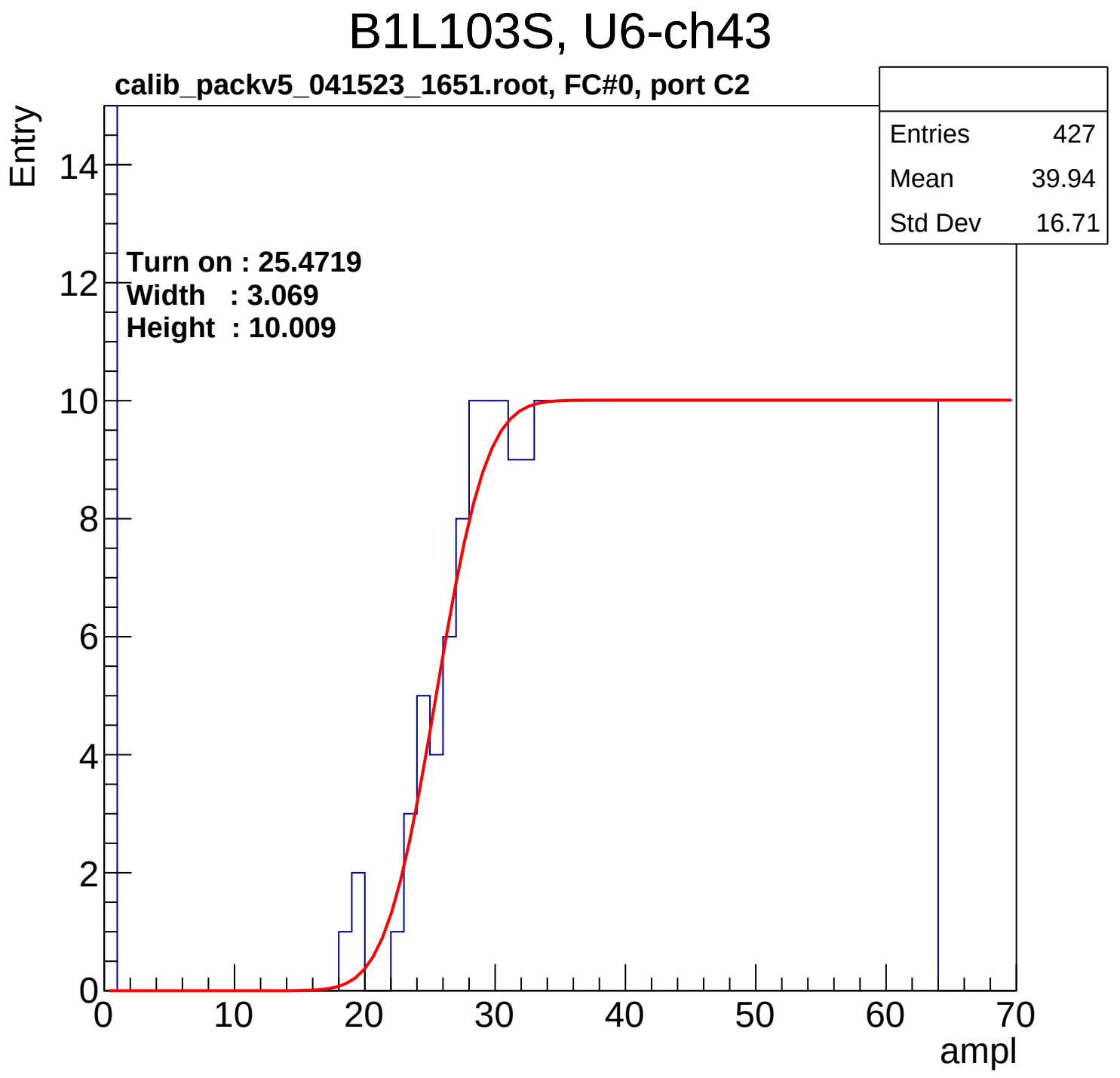

B1L103S, U6-ch38
calib_packv5_041523_1651.root, FC#0, port C2
Entries 434
Mean 39.58
Std Dev 16.92
Turn on : 24.9784
Width : 2.492
Height : 10.036
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

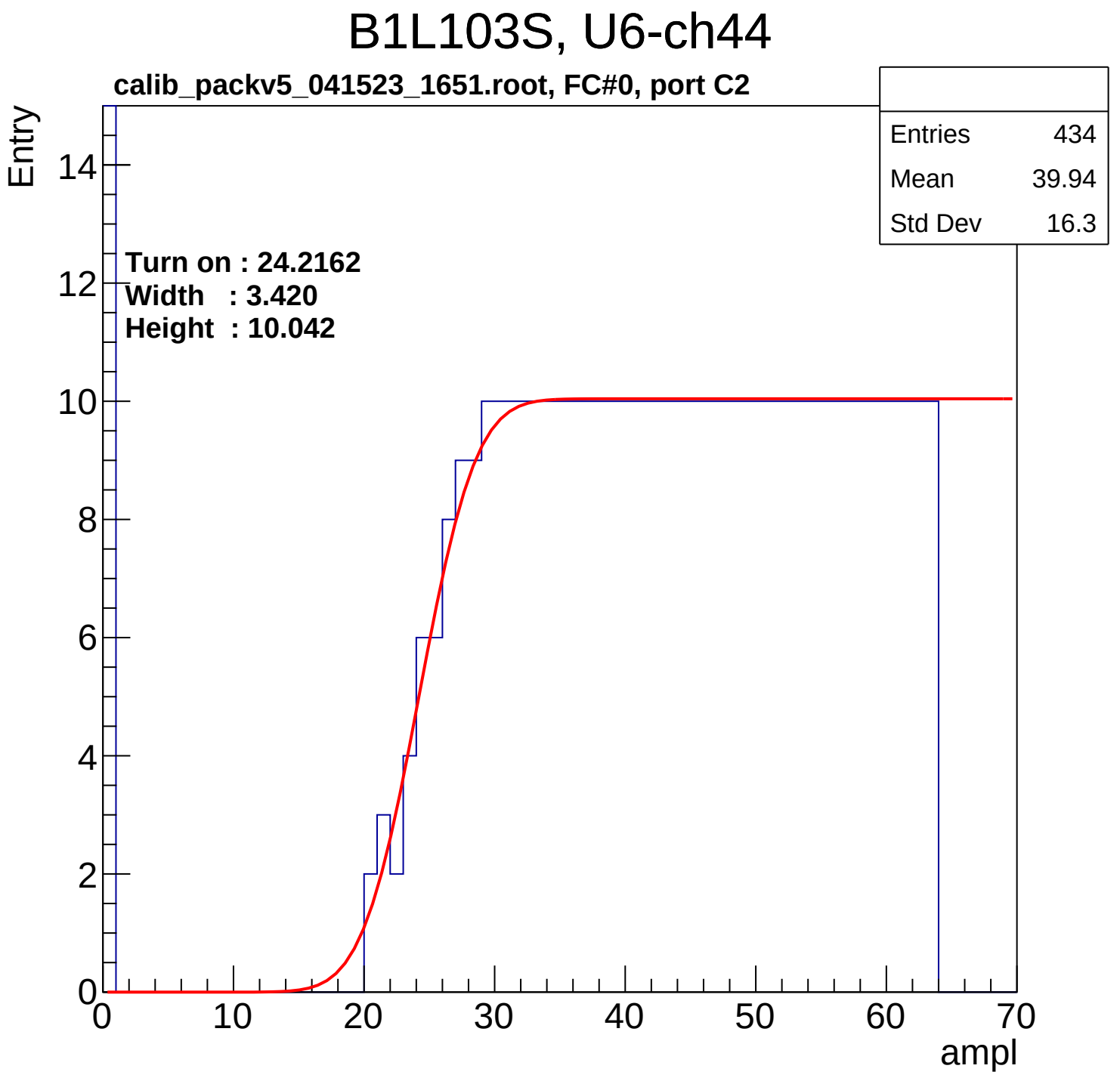

B1L103S, U6-ch39
calib_packv5_041523_1651.root, FC#0, port C2
Entries 418
Mean 40.18
Std Dev 16.91
Turn on : 26.8186
Width : 2.889
Height : 10.063
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

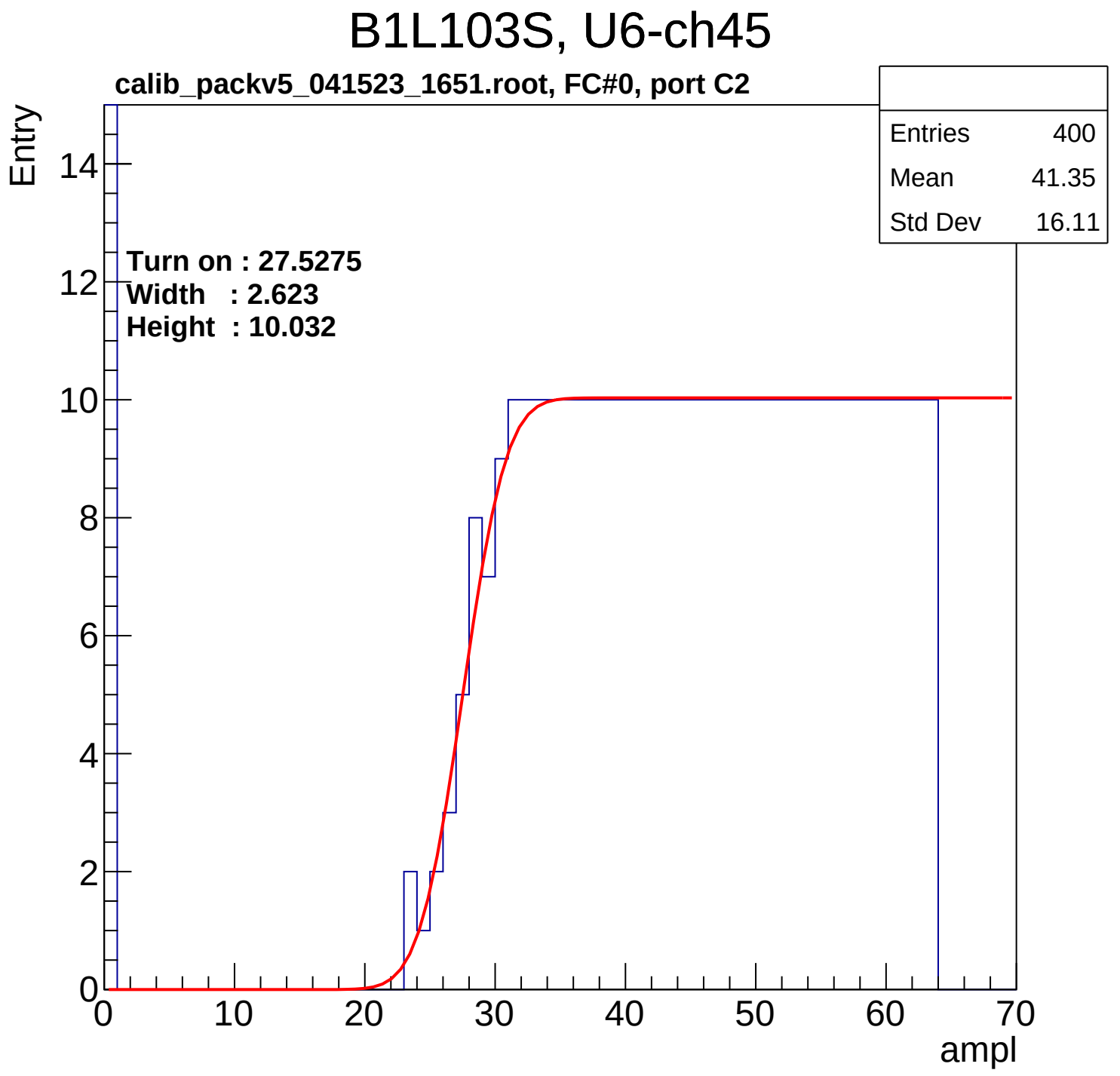

B1L103S, U6-ch40
calib_packv5_041523_1651.root, FC#0, port C2
Entries 451
Mean 39.22
Std Dev 16.75
Turn on : 23.5682
Width : 2.859
Height : 10.030
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

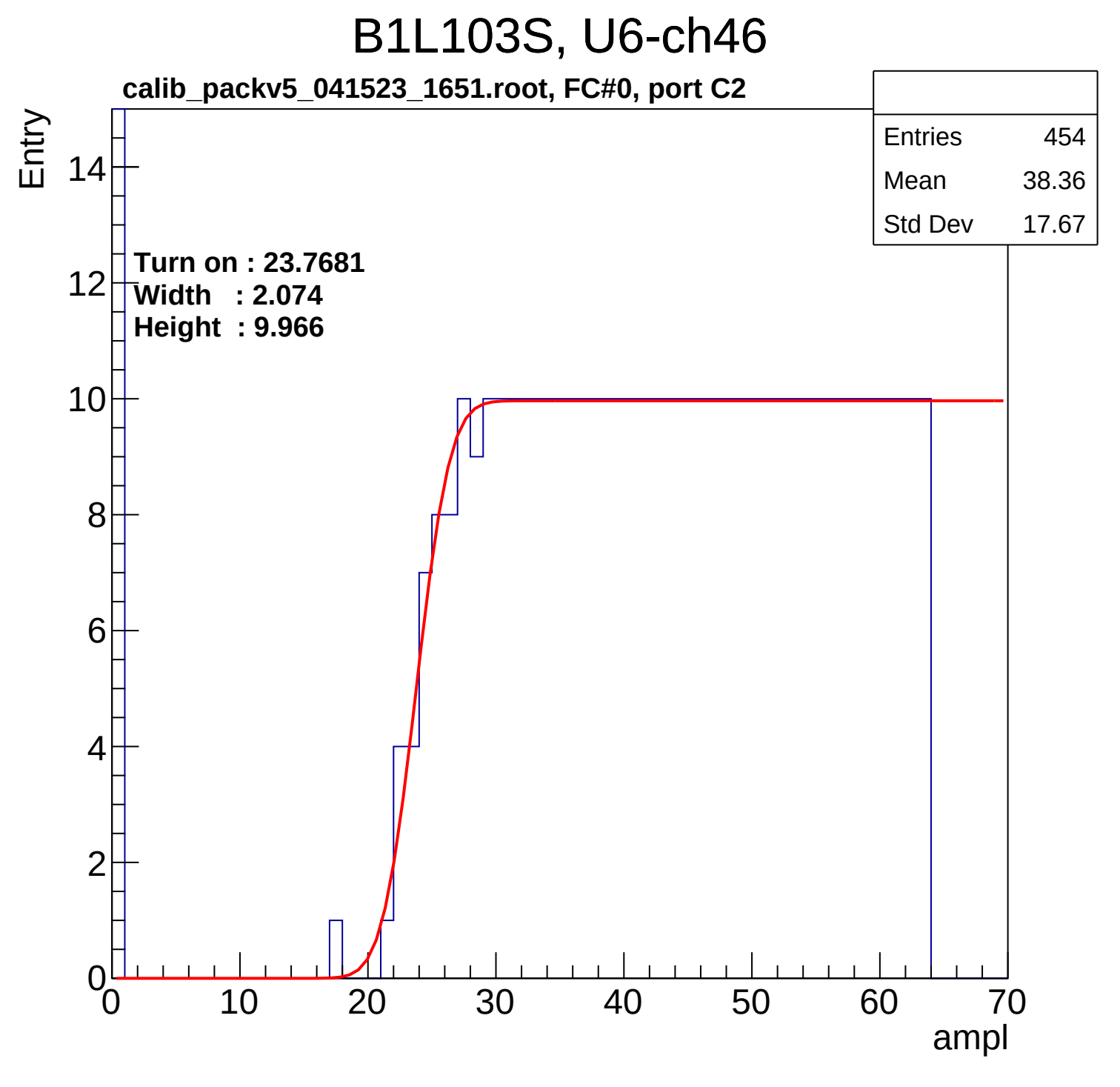

B1L103S, U6-ch41
calib_packv5_041523_1651.root, FC#0, port C2
Entries 407
Mean 41.01
Std Dev 16.21
Turn on : 26.9196
Width : 3.421
Height : 10.068
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

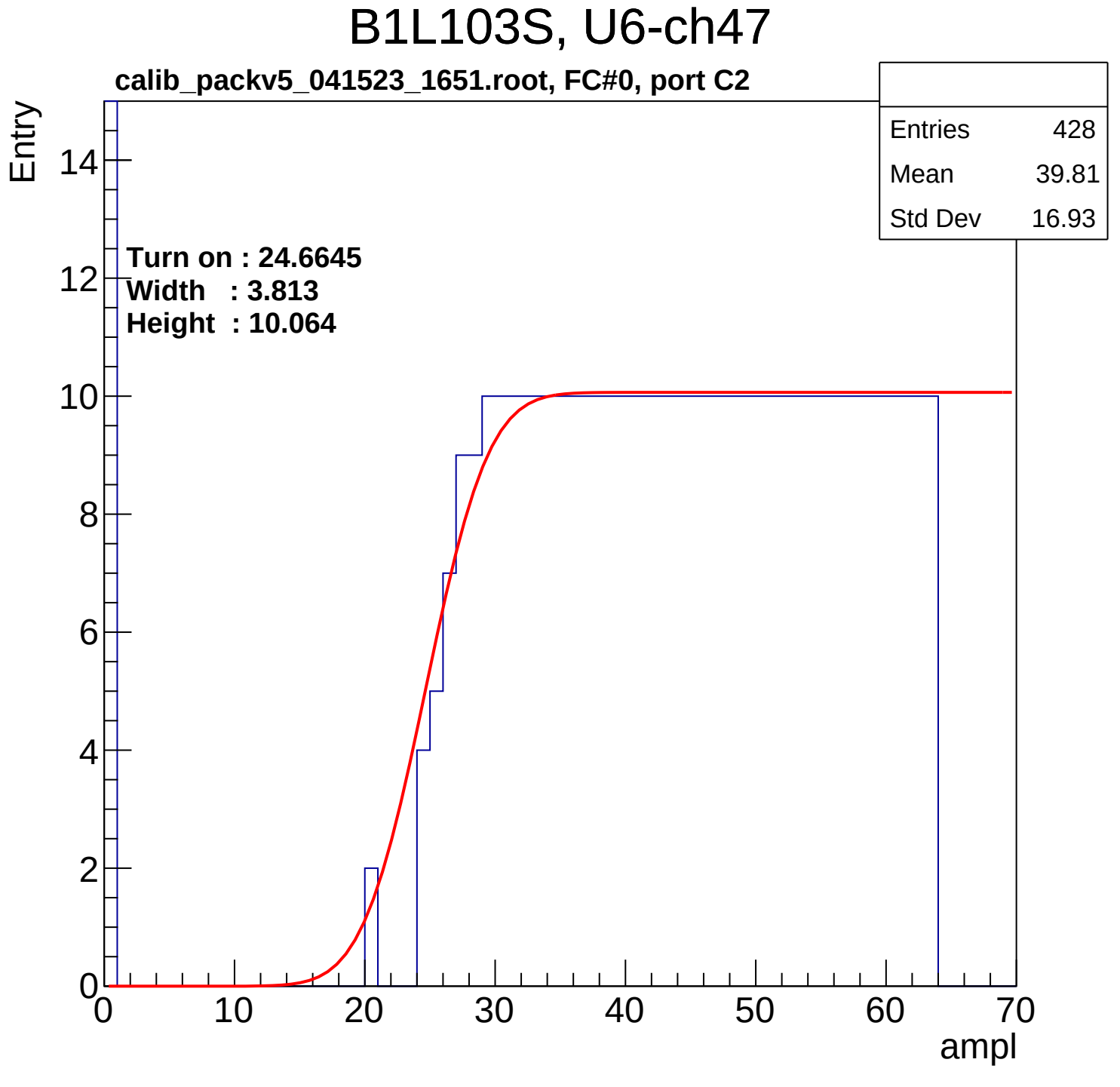

B1L103S, U6-ch42
calib_packv5_041523_1651.root, FC#0, port C2
Entries 423
Mean 39.84
Std Dev 17.11
Turn on : 26.3082
Width : 4.026
Height : 10.047
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

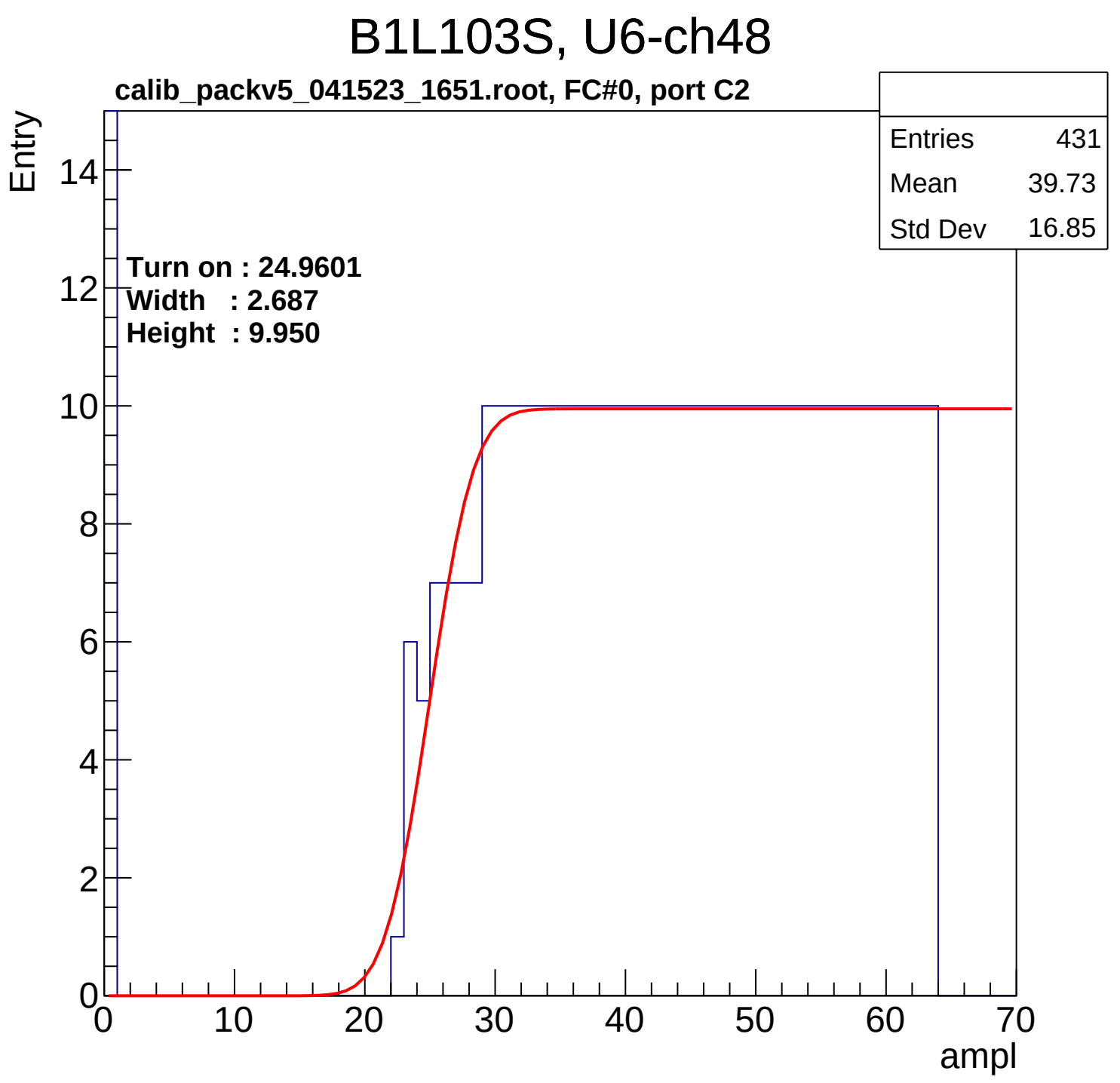

B1L103S, U6-ch43
calib_packv5_041523_1651.root, FC#0, port C2
Entries 427
Mean 39.94
Std Dev 16.71
Turn on : 25.4719
Width : 3.069
Height : 10.009
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

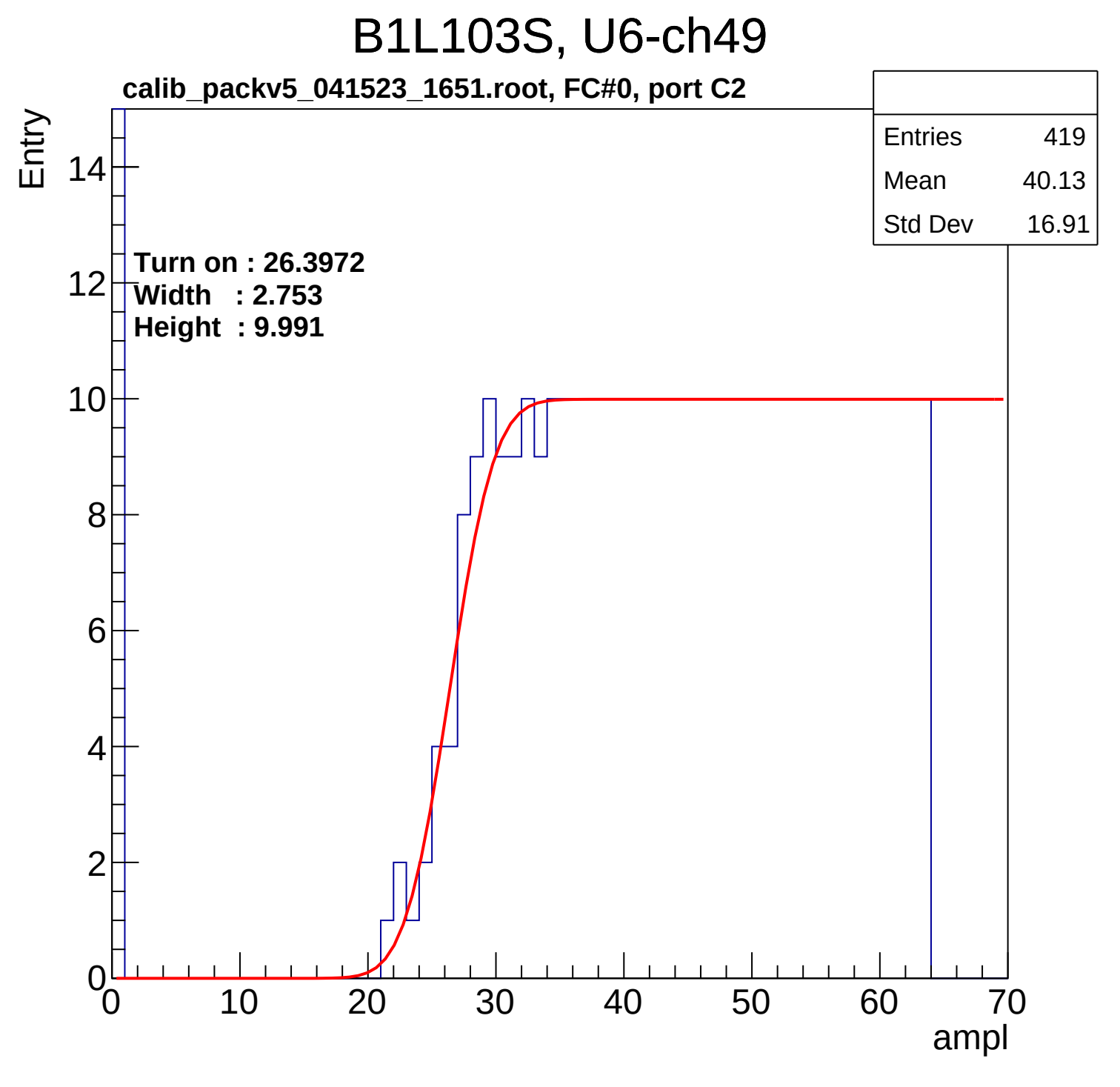

B1L103S, U6-ch44
calib_packv5_041523_1651.root, FC#0, port C2
Entries 434
Mean 39.94
Std Dev 16.3
Turn on : 24.2162
Width : 3.420
Height : 10.042
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

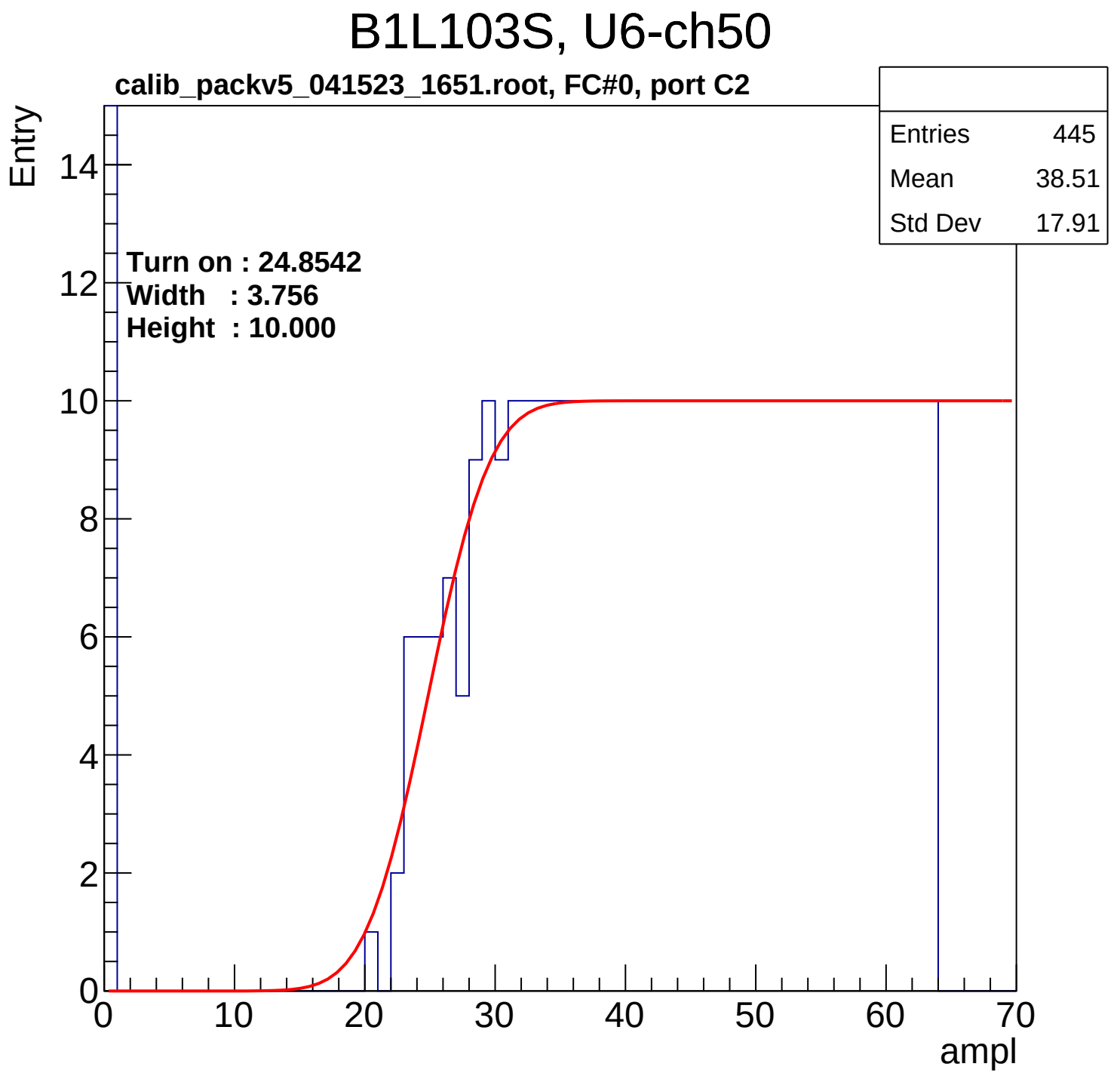

B1L103S, U6-ch45
calib_packv5_041523_1651.root, FC#0, port C2
Entries 400
Mean 41.35
Std Dev 16.11
Turn on : 27.5275
Width : 2.623
Height : 10.032
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

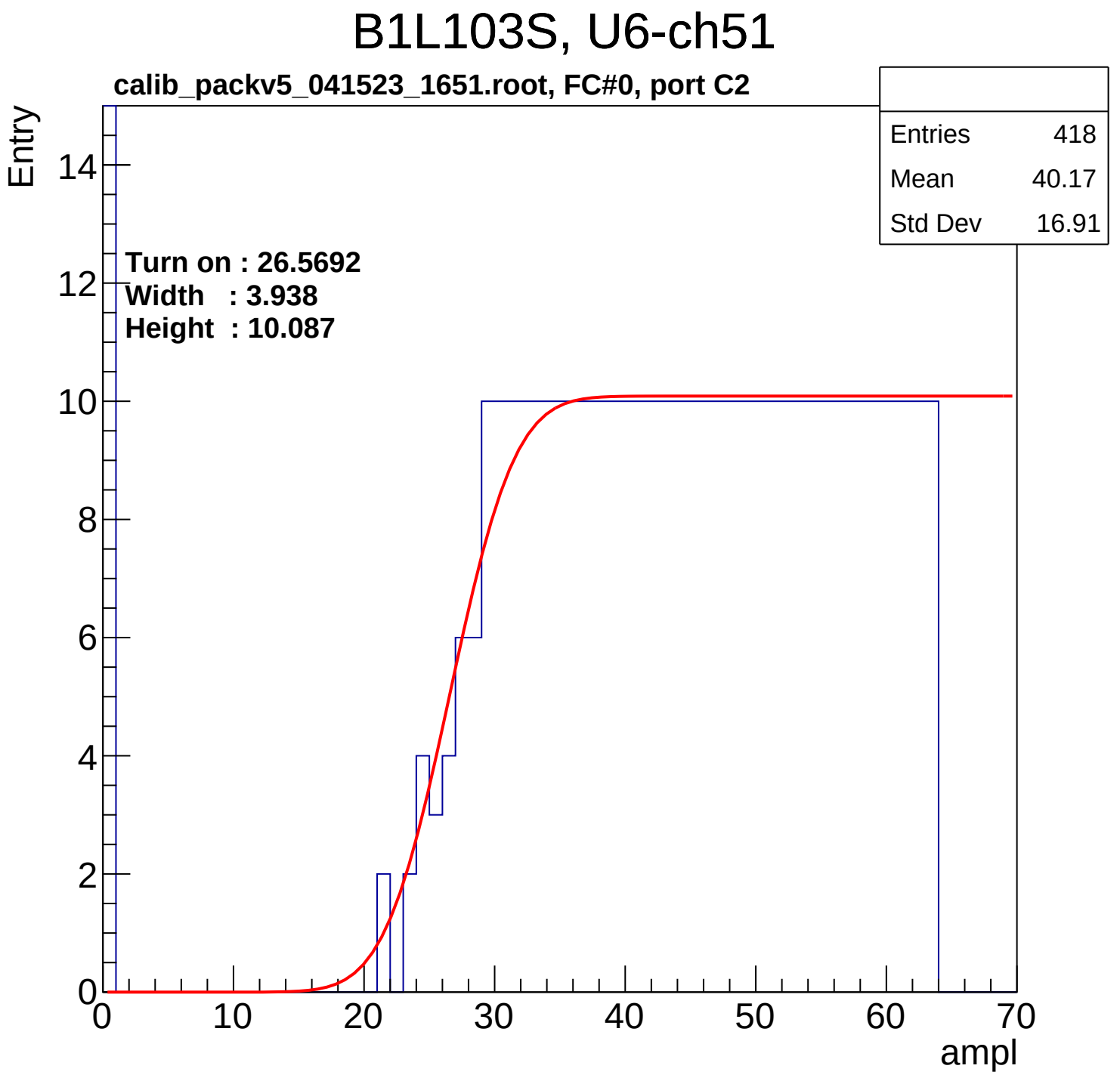

B1L103S, U6-ch46
calib_packv5_041523_1651.root, FC#0, port C2
Entries 454
Mean 38.36
Std Dev 17.67
Turn on : 23.7681
Width : 2.074
Height : 9.966
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

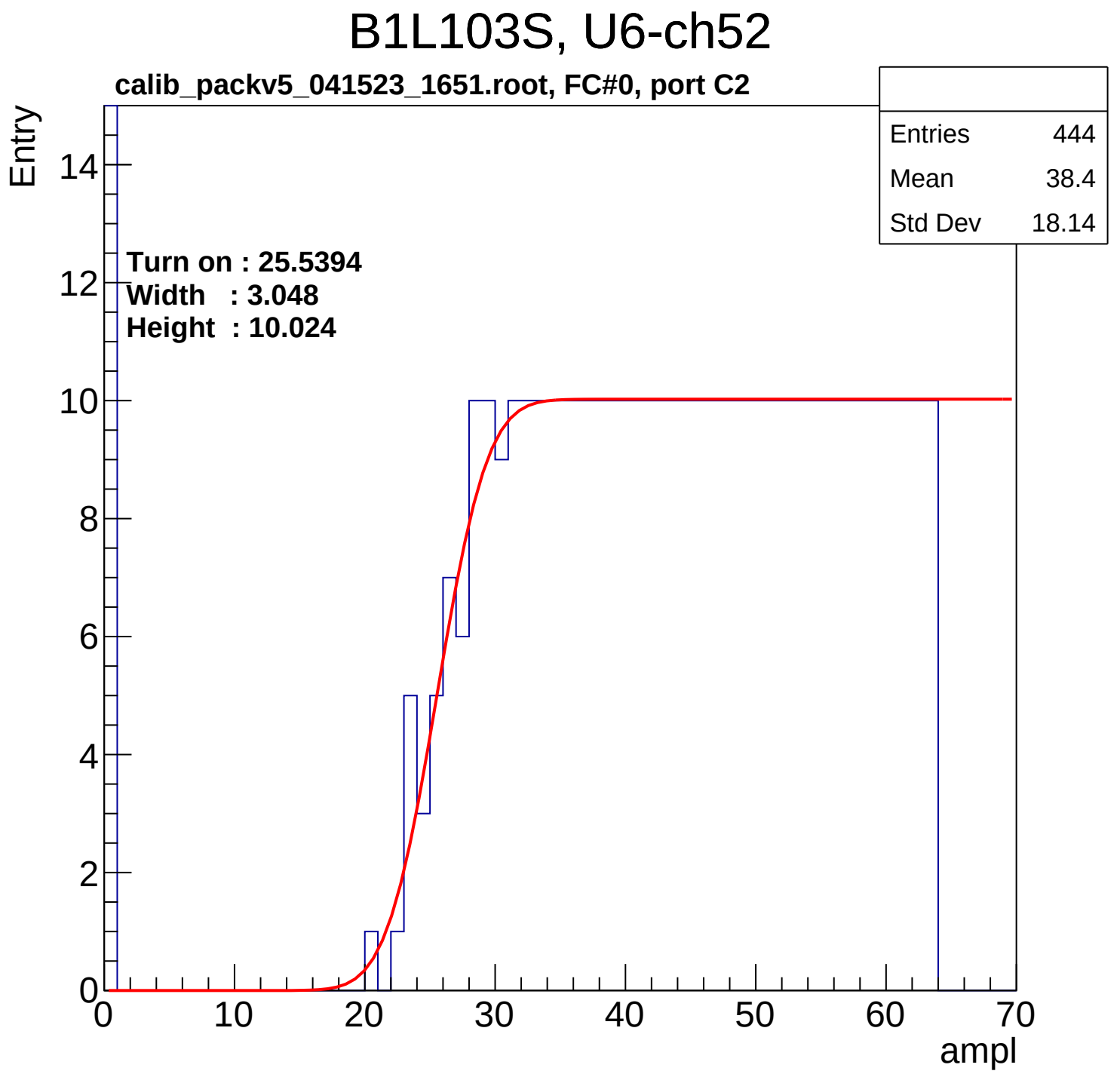

B1L103S, U6-ch47
calib_packv5_041523_1651.root, FC#0, port C2
Entries 428
Mean 39.81
Std Dev 16.93
Turn on : 24.6645
Width : 3.813
Height : 10.064
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

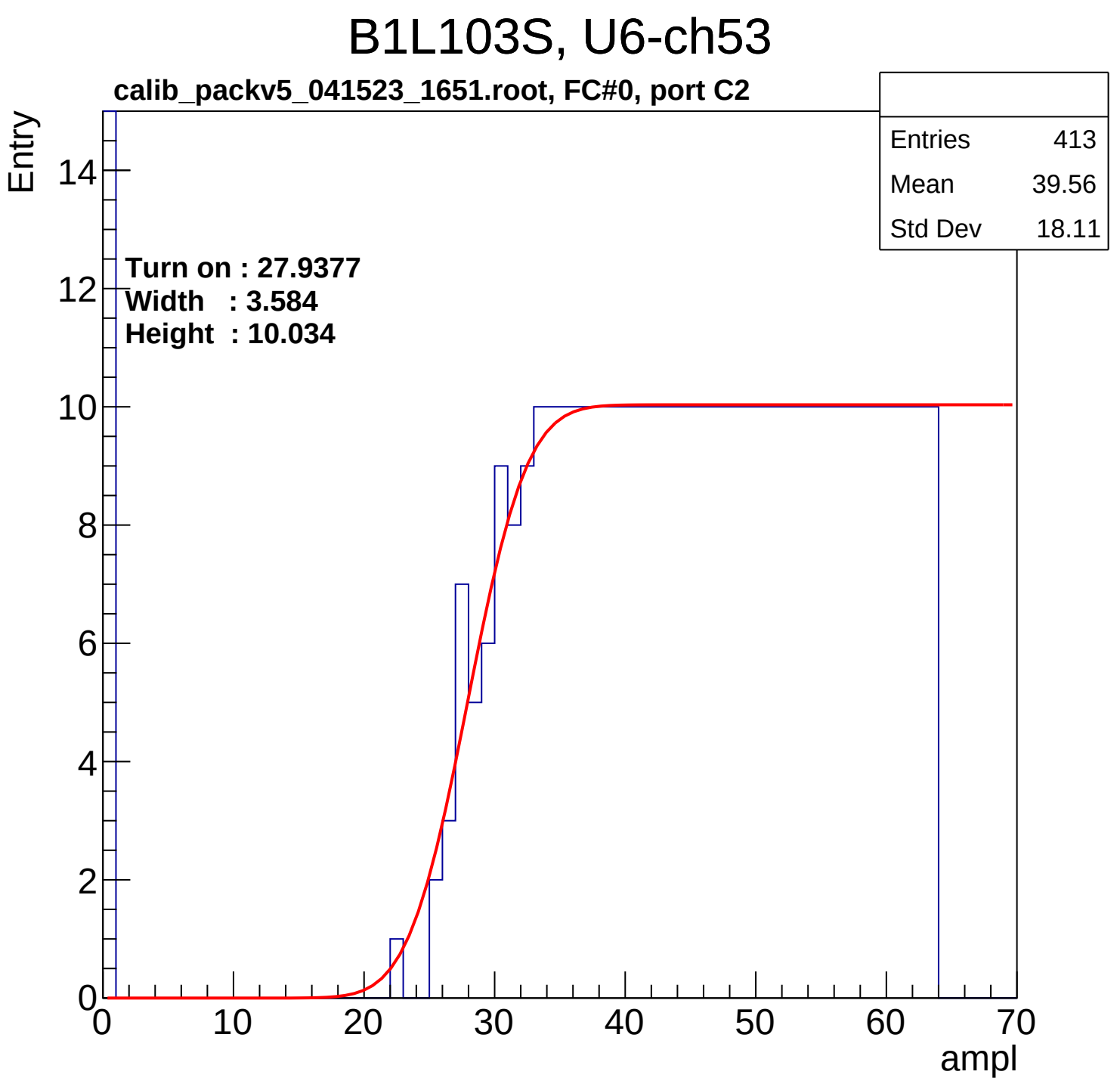

B1L103S, U6-ch48
calib_packv5_041523_1651.root, FC#0, port C2
Entries 431
Mean 39.73
Std Dev 16.85
Turn on : 24.9601
Width : 2.687
Height : 9.950
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

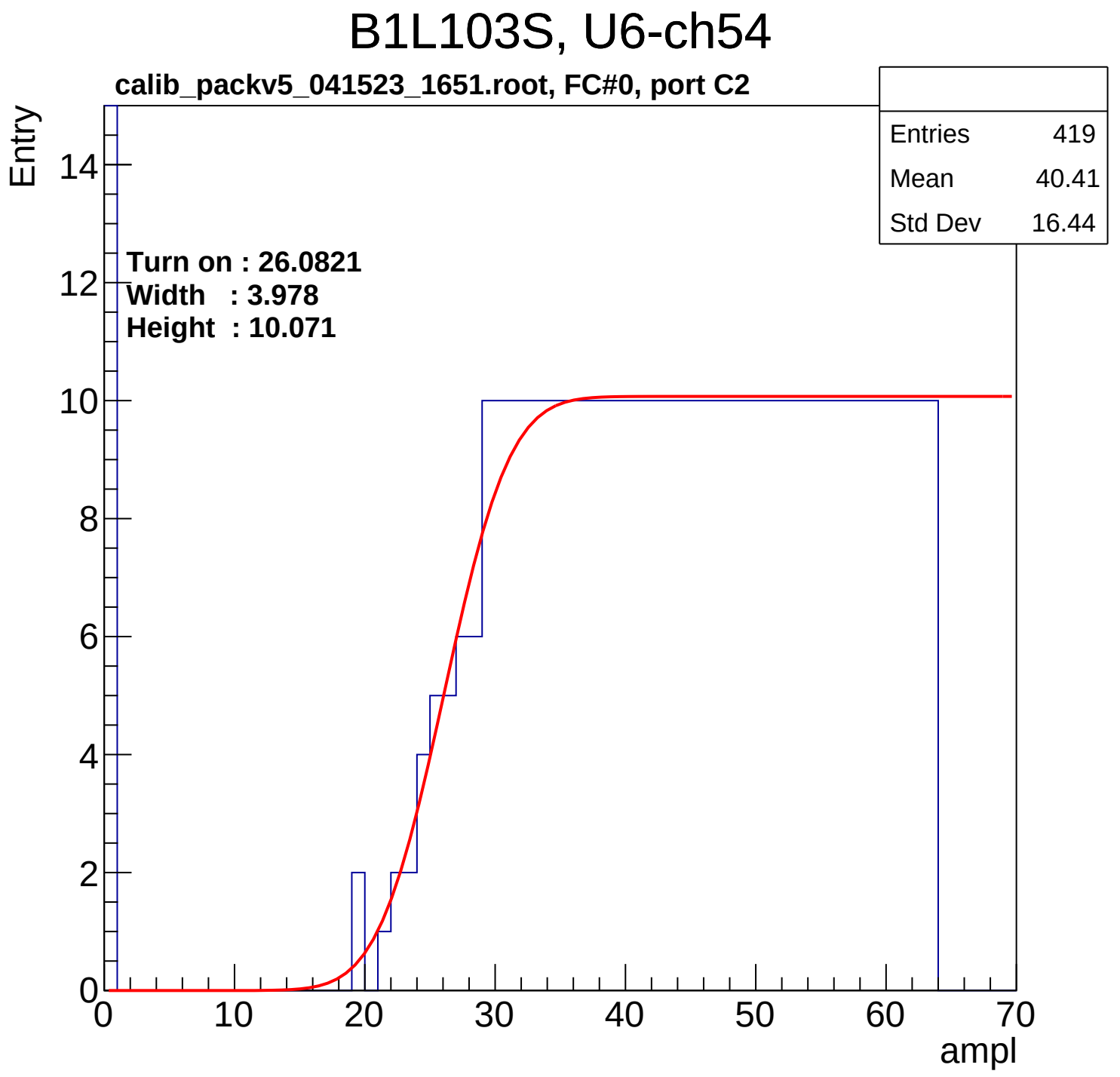

B1L103S, U6-ch49
calib_packv5_041523_1651.root, FC#0, port C2
Entries 419
Mean 40.13
Std Dev 16.91
Turn on : 26.3972
Width : 2.753
Height : 9.991
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

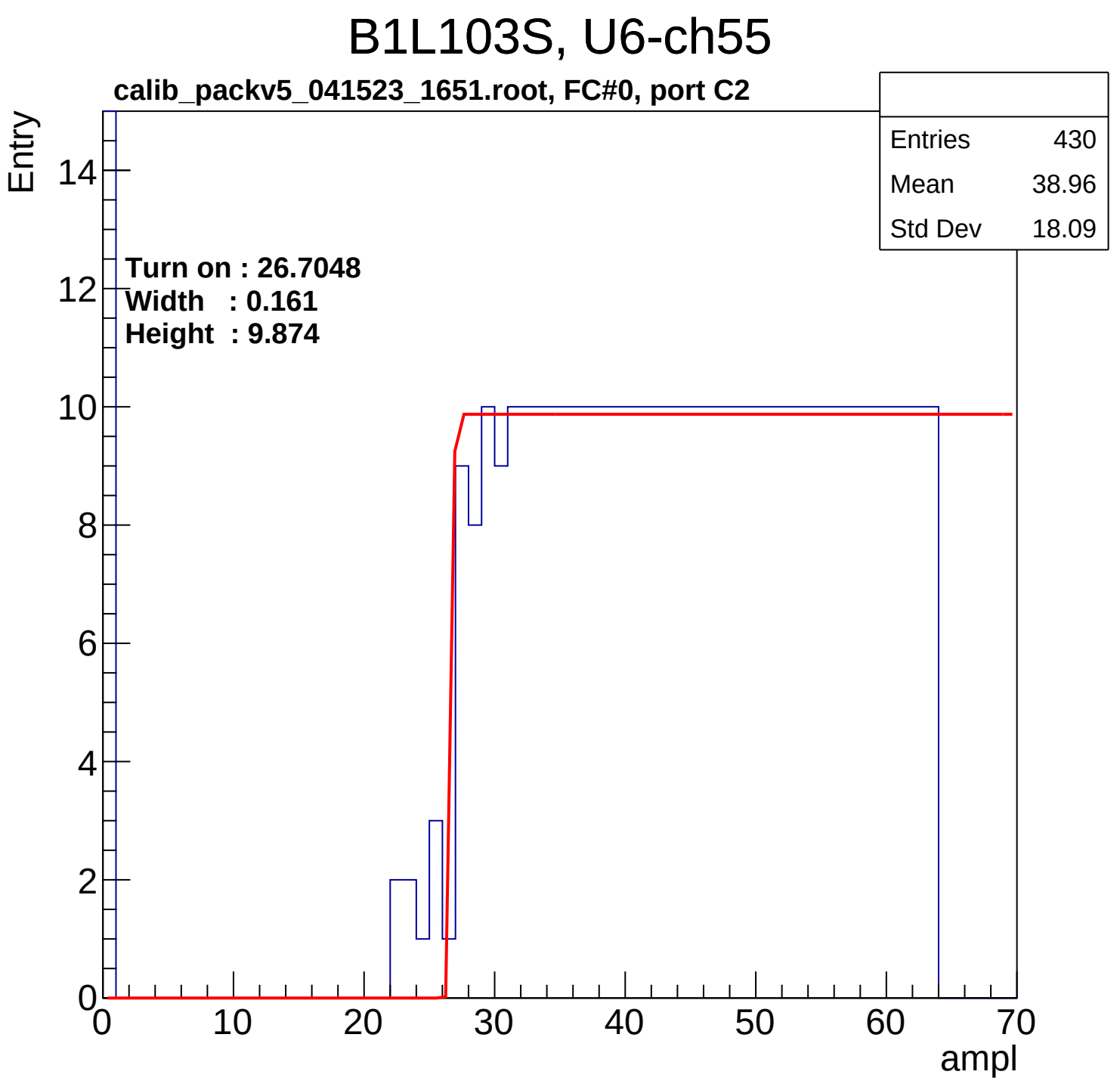

B1L103S, U6-ch50
calib_packv5_041523_1651.root, FC#0, port C2
Entries 445
Mean 38.51
Std Dev 17.91
Turn on : 24.8542
Width : 3.756
Height : 10.000
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

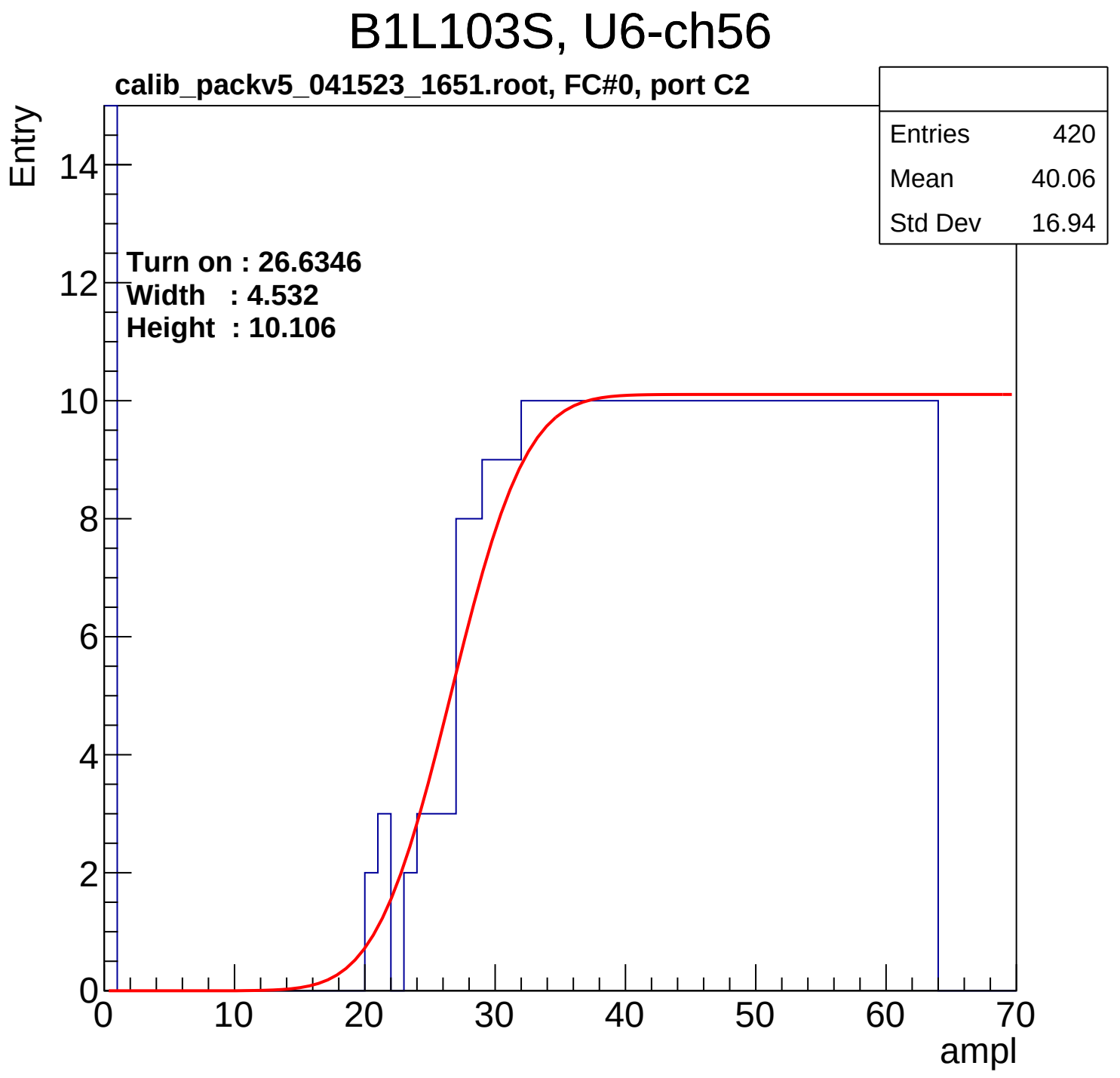

B1L103S, U6-ch51
calib_packv5_041523_1651.root, FC#0, port C2
Entries 418
Mean 40.17
Std Dev 16.91
Turn on : 26.5692
Width : 3.938
Height : 10.087
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

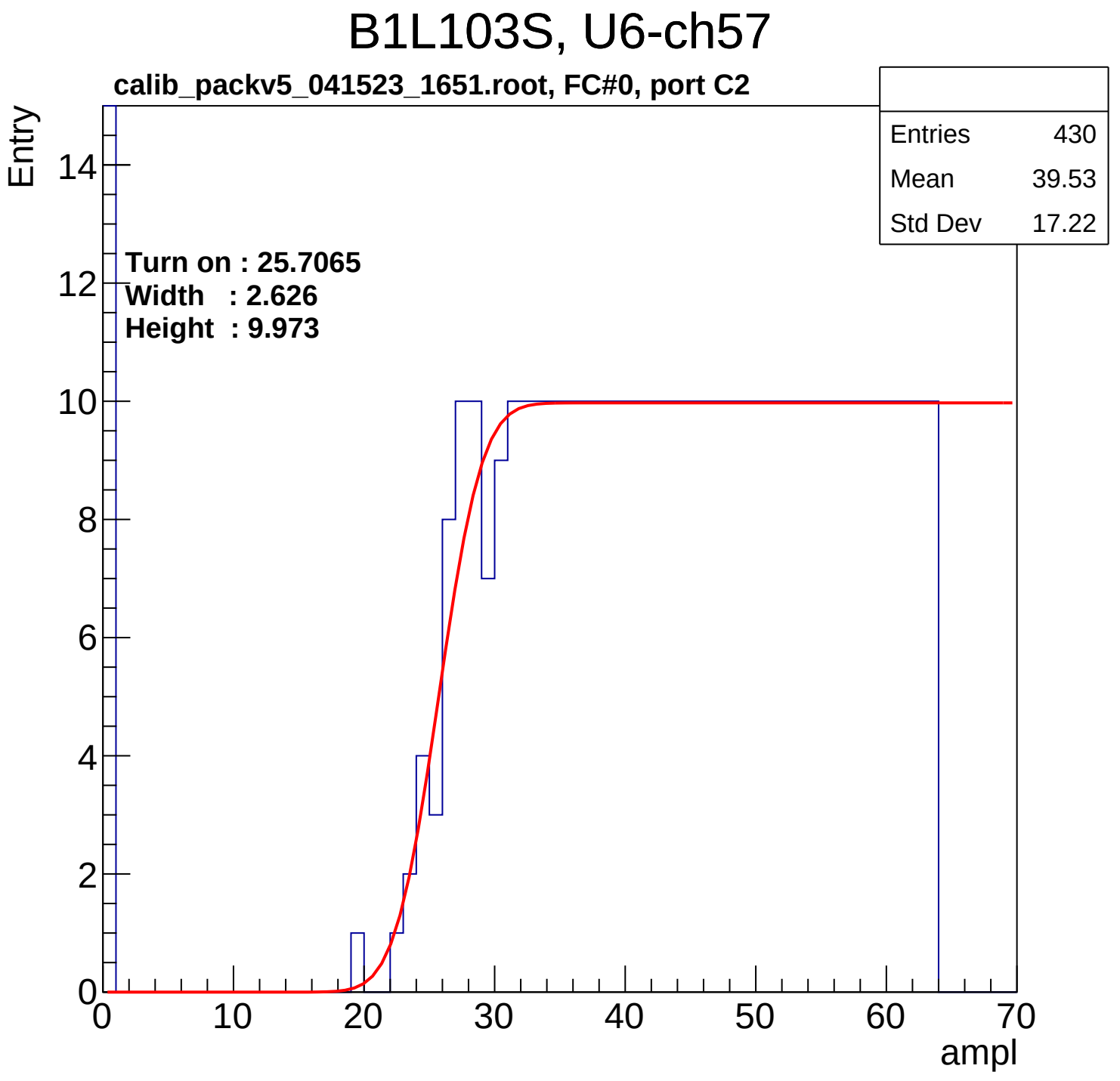

B1L103S, U6-ch52
calib_packv5_041523_1651.root, FC#0, port C2
Entries 444
Mean 38.4
Std Dev 18.14
Turn on : 25.5394
Width : 3.048
Height : 10.024
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

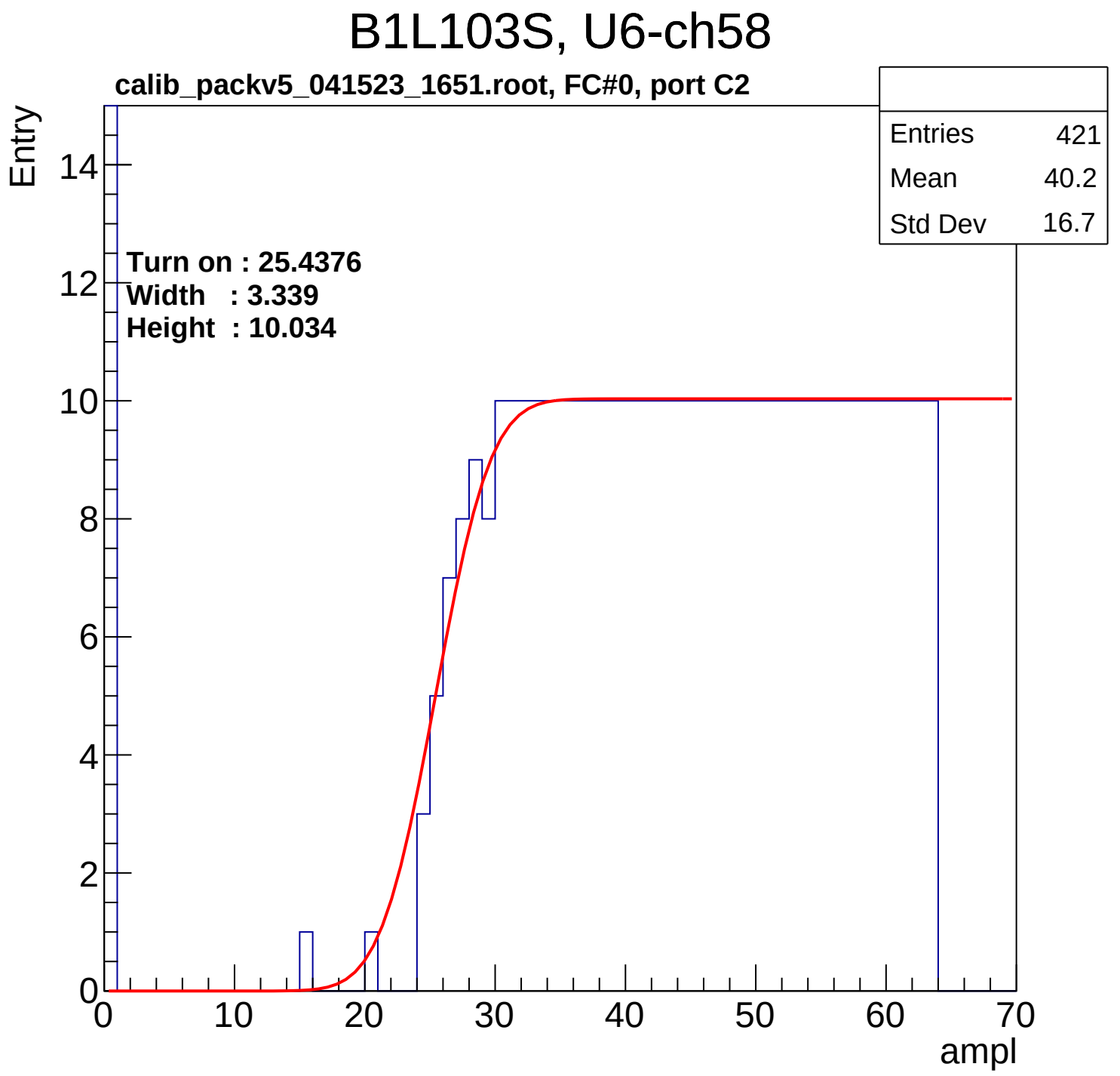

B1L103S, U6-ch53
calib_packv5_041523_1651.root, FC#0, port C2
Entries 413
Mean 39.56
Std Dev 18.11
Turn on : 27.9377
Width : 3.584
Height : 10.034
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

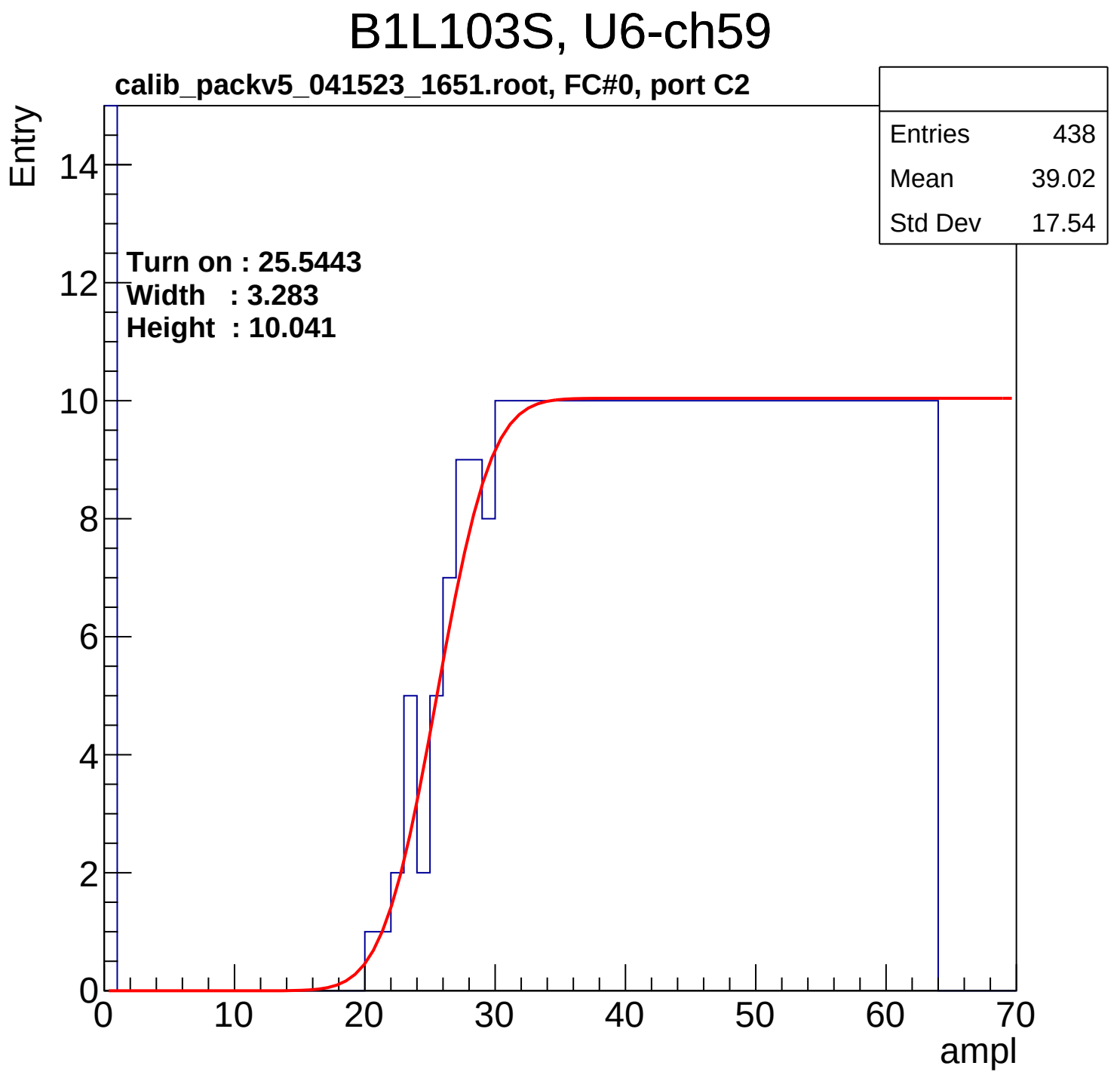

B1L103S, U6-ch54
calib_packv5_041523_1651.root, FC#0, port C2
Entries 419
Mean 40.41
Std Dev 16.44
Turn on : 26.0821
Width : 3.978
Height : 10.071
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

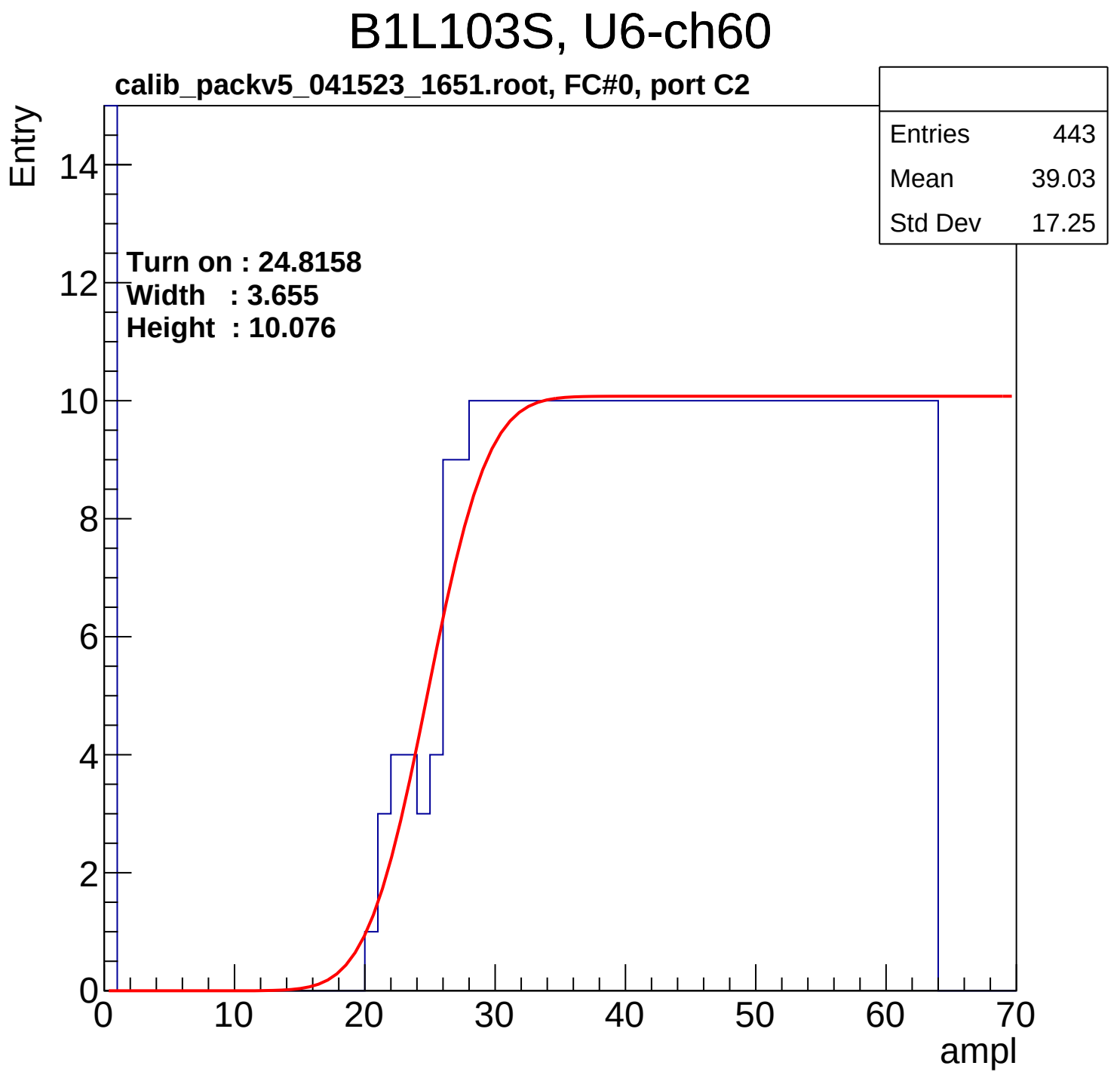

B1L103S, U6-ch55
calib_packv5_041523_1651.root, FC#0, port C2
Entries 430
Mean 38.96
Std Dev 18.09
Turn on : 26.7048
Width : 0.161
Height : 9.874
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

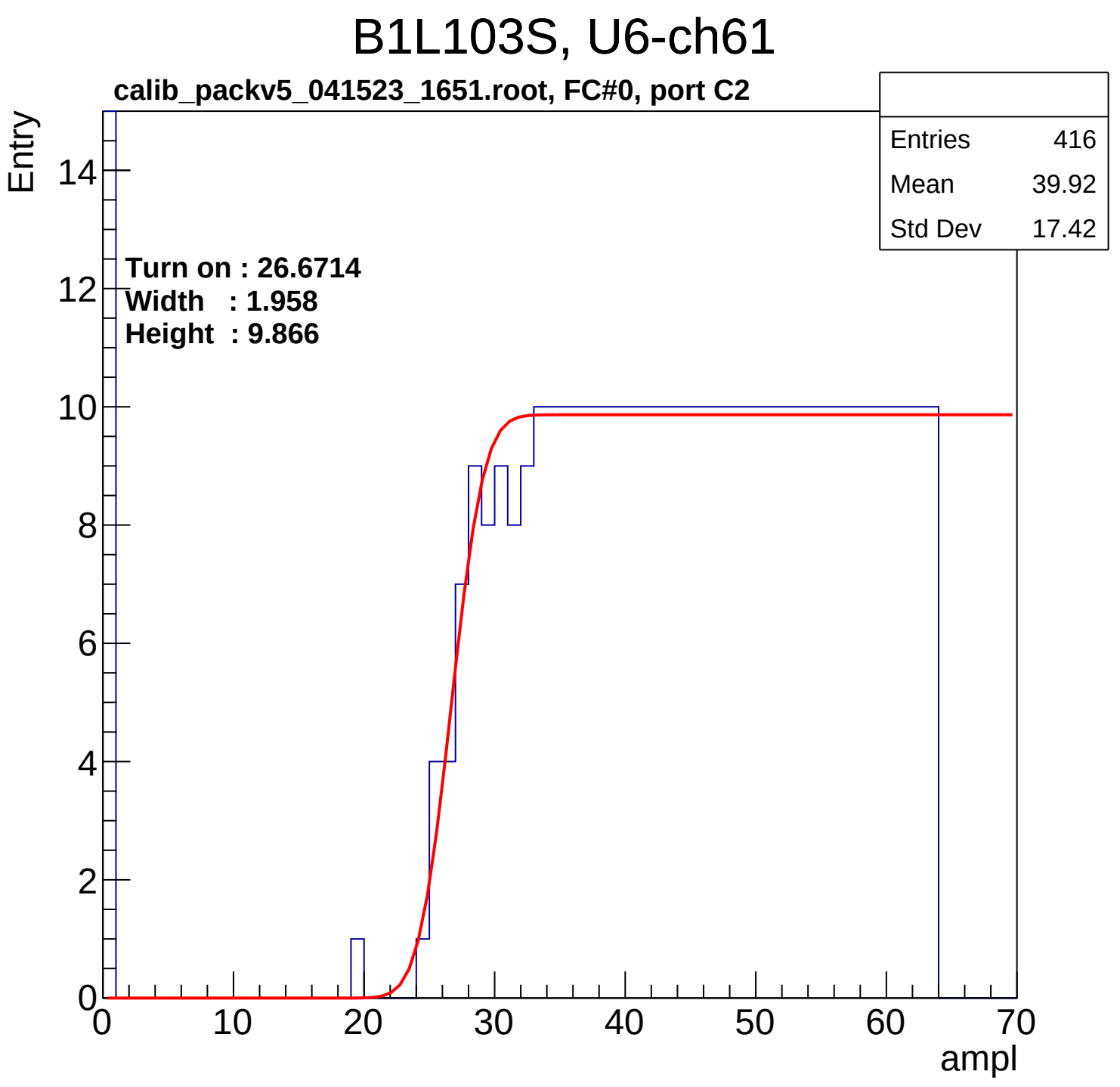

B1L103S, U6-ch56
calib_packv5_041523_1651.root, FC#0, port C2
Entries 420
Mean 40.06
Std Dev 16.94
Turn on : 26.6346
Width : 4.532
Height : 10.106
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

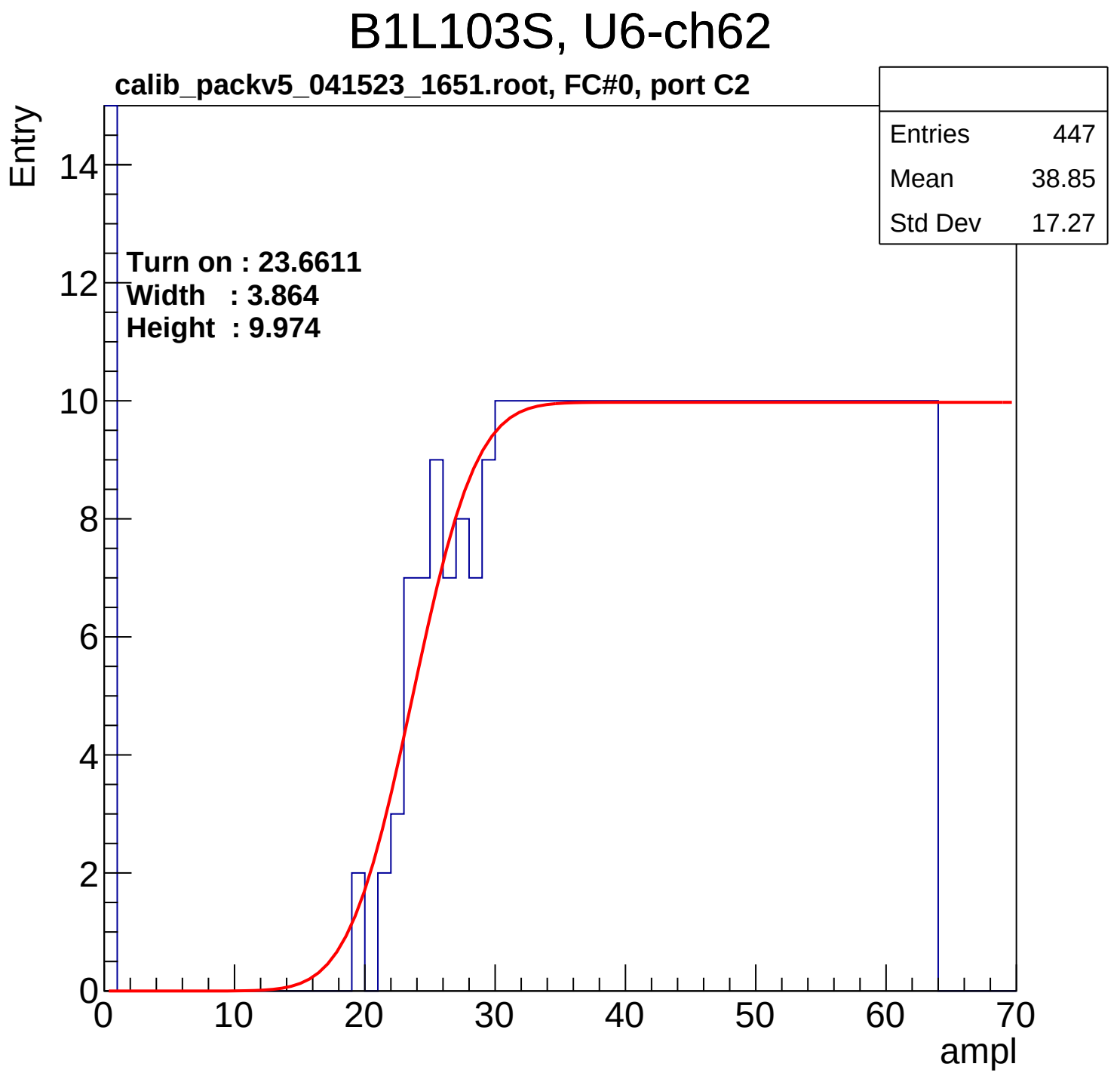

B1L103S, U6-ch57
calib_packv5_041523_1651.root, FC#0, port C2
Entries 430
Mean 39.53
Std Dev 17.22
Turn on : 25.7065
Width : 2.626
Height : 9.973
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

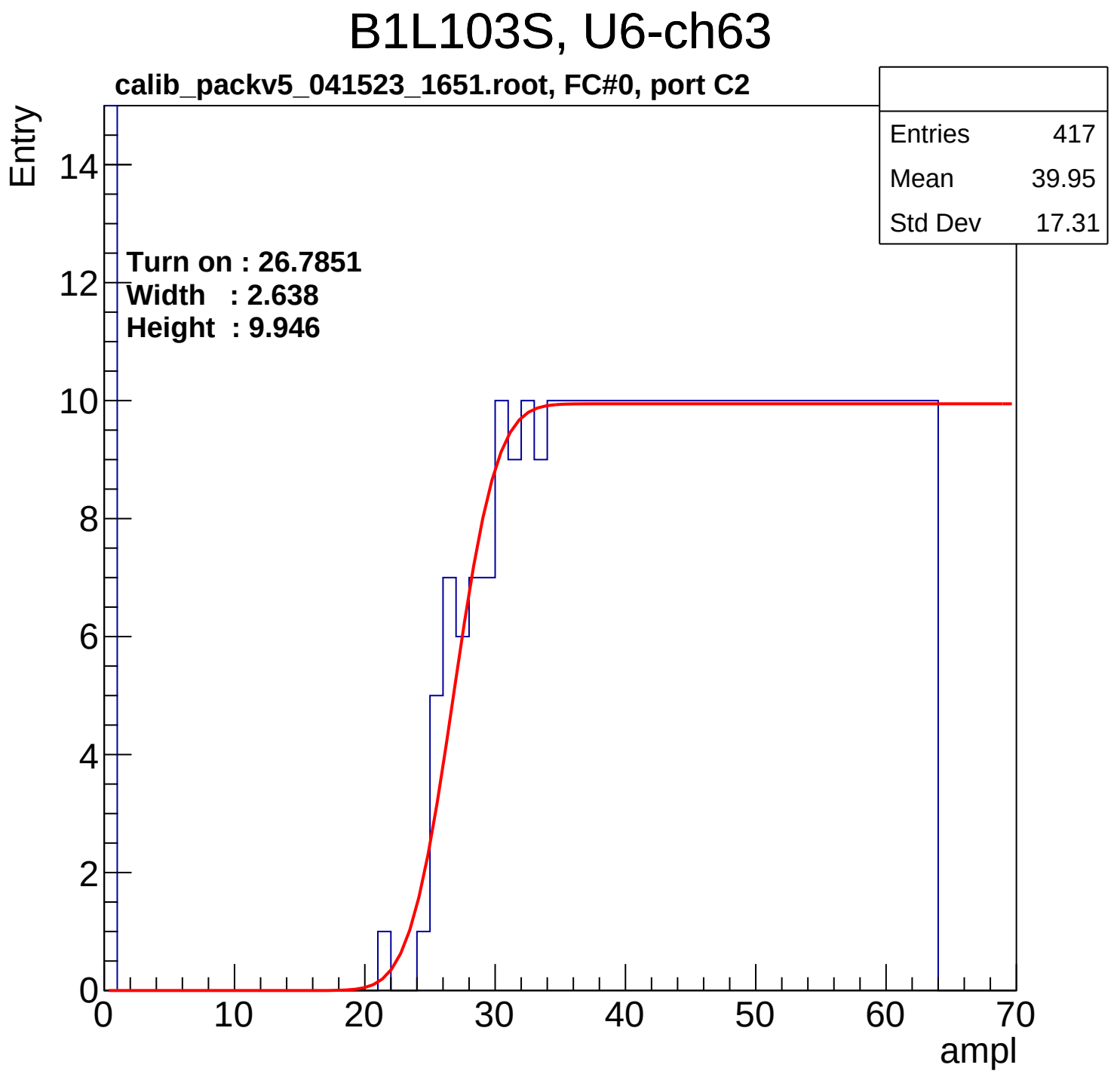

B1L103S, U6-ch58
calib_packv5_041523_1651.root, FC#0, port C2
Entries 421
Mean 40.2
Std Dev 16.7
Turn on : 25.4376
Width : 3.339
Height : 10.034
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

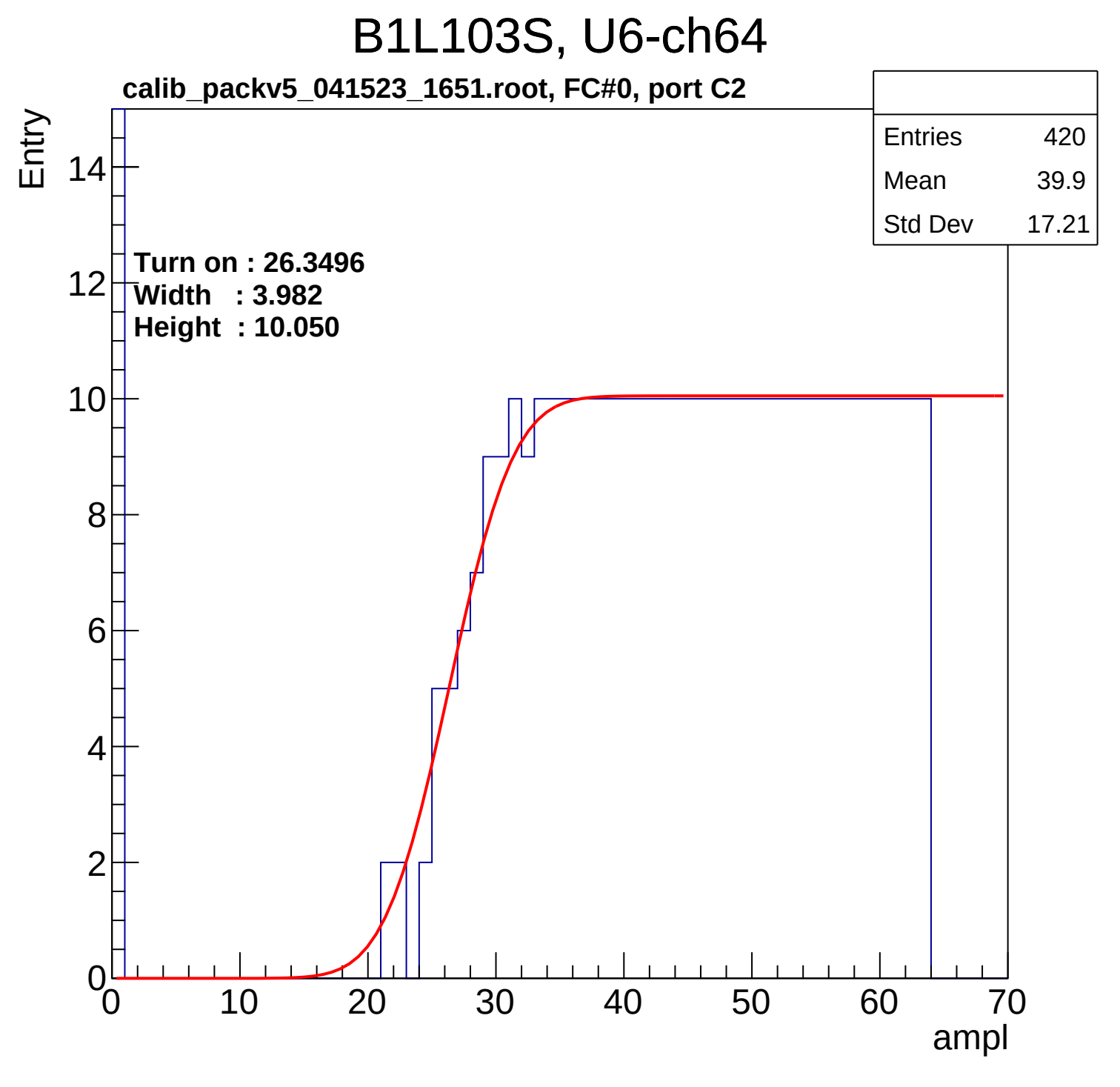

B1L103S, U6-ch59
calib_packv5_041523_1651.root, FC#0, port C2
Entries 438
Mean 39.02
Std Dev 17.54
Turn on : 25.5443
Width : 3.283
Height : 10.041
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

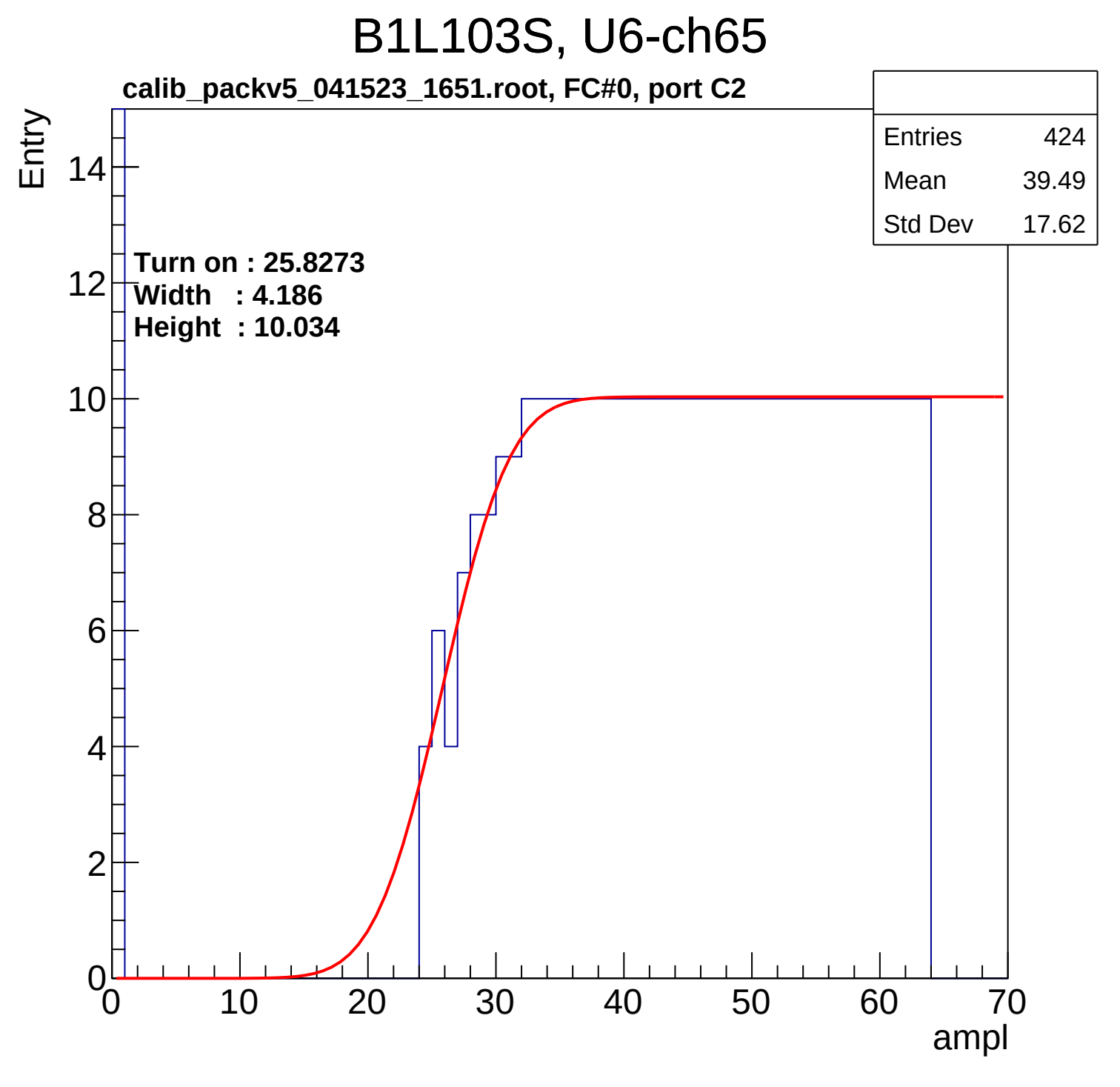

B1L103S, U6-ch60
calib_packv5_041523_1651.root, FC#0, port C2
Entries 443
Mean 39.03
Std Dev 17.25
Turn on : 24.8158
Width : 3.655
Height : 10.076
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

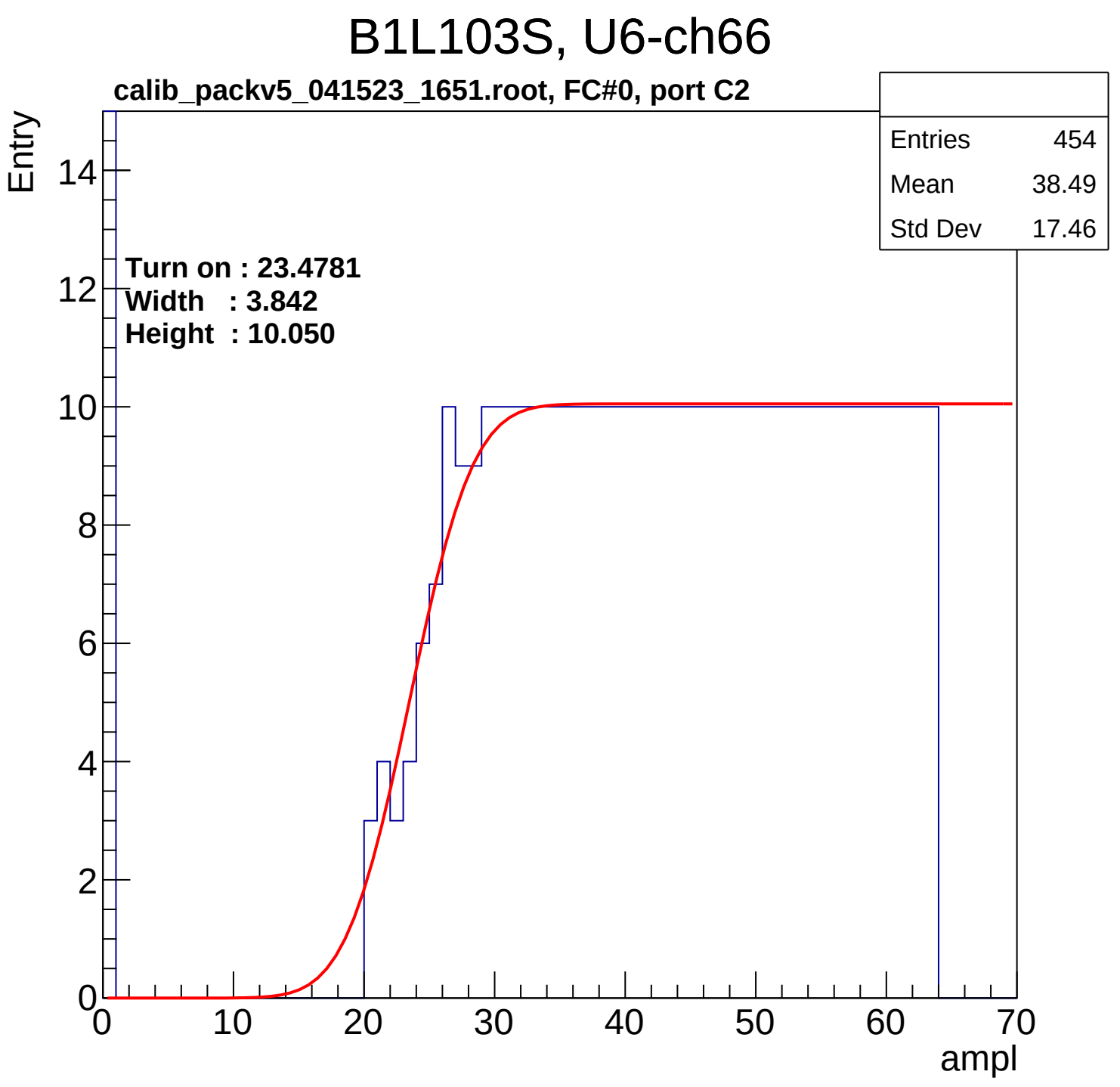

B1L103S, U6-ch61
calib_packv5_041523_1651.root, FC#0, port C2
Entries 416
Mean 39.92
Std Dev 17.42
Turn on : 26.6714
Width : 1.958
Height : 9.866
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

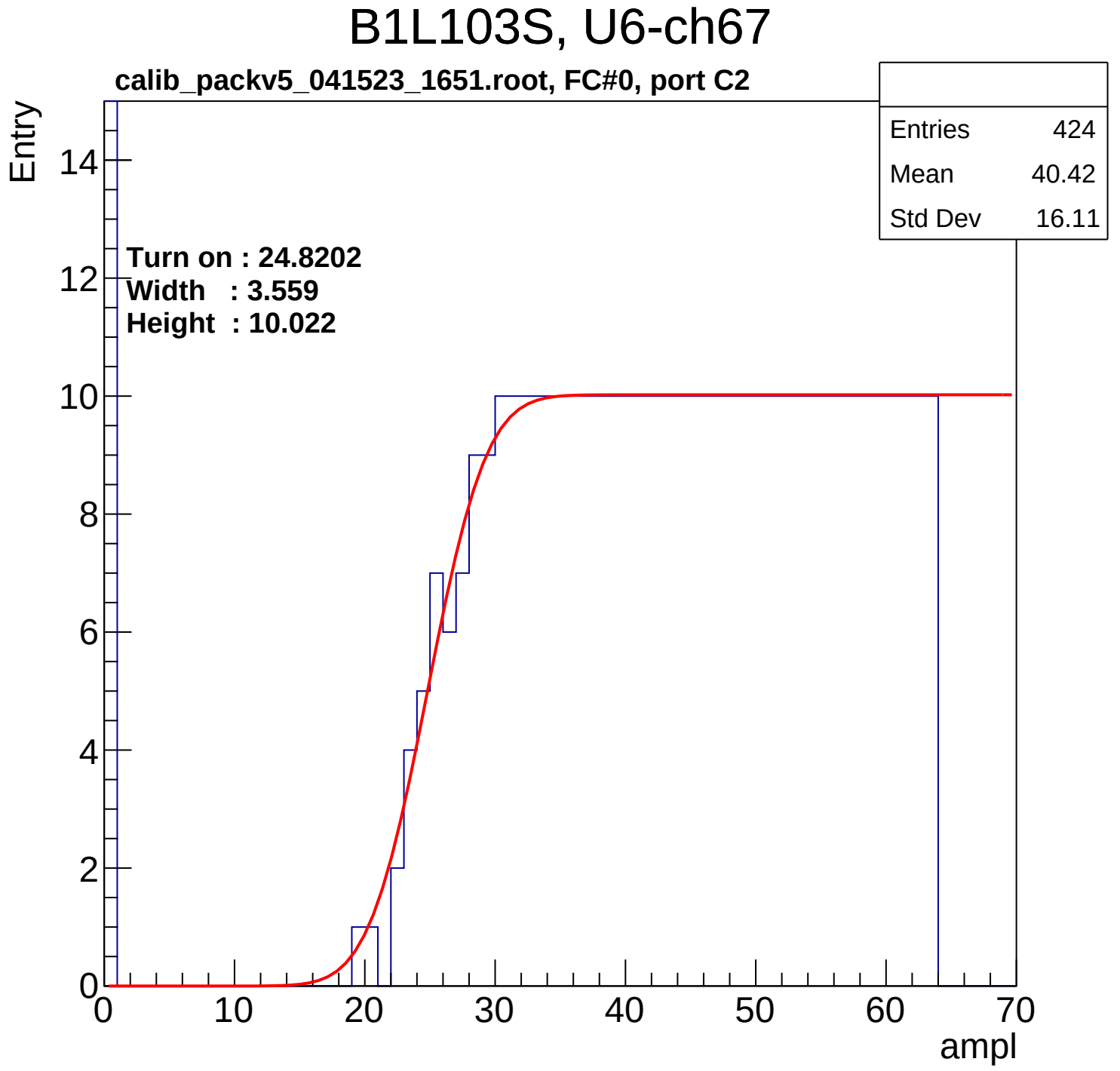

B1L103S, U6-ch62
calib_packv5_041523_1651.root, FC#0, port C2
Entries 447
Mean 38.85
Std Dev 17.27
Turn on : 23.6611
Width : 3.864
Height : 9.974
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

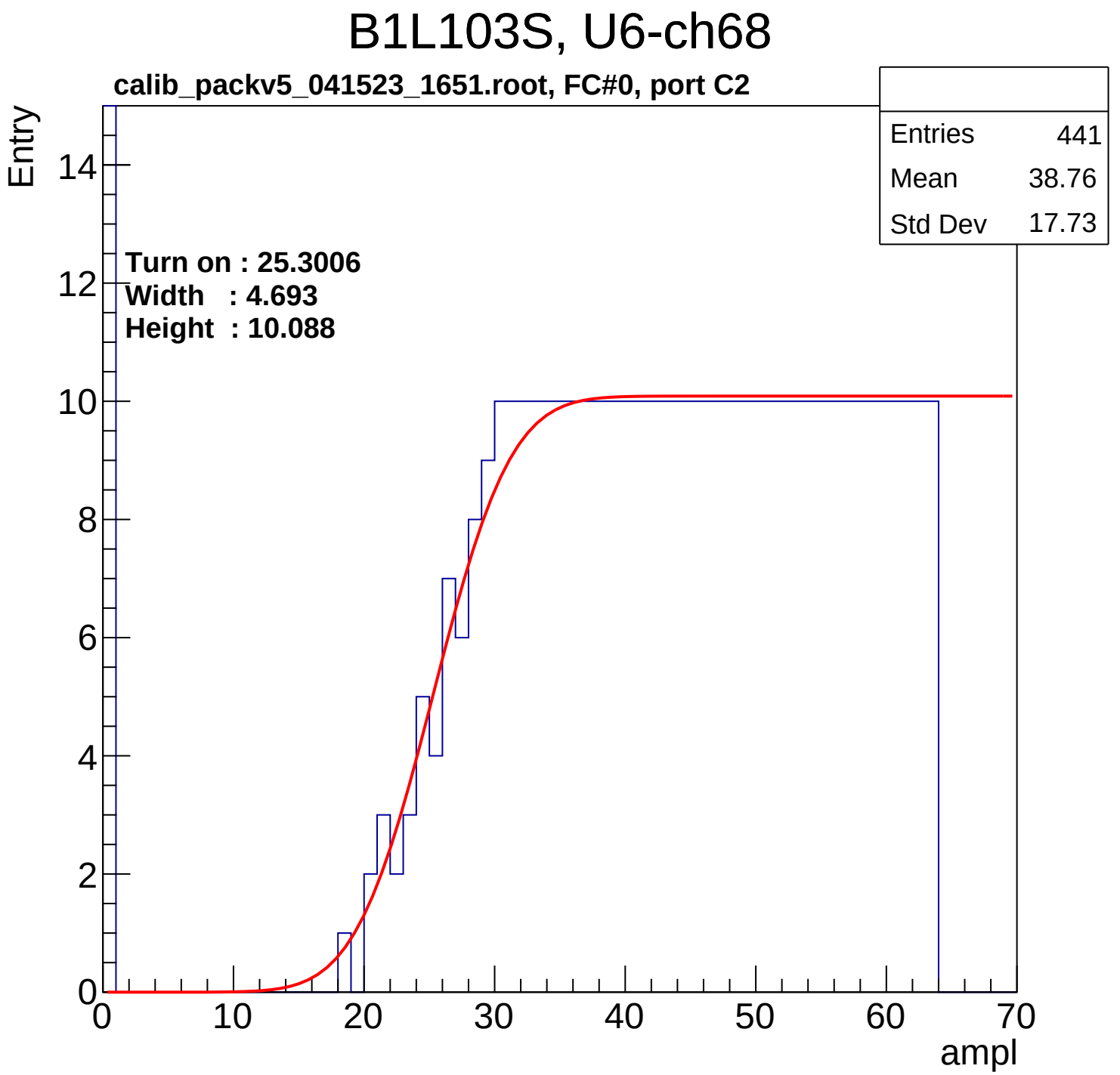

B1L103S, U6-ch63
calib_packv5_041523_1651.root, FC#0, port C2
Entries 417
Mean 39.95
Std Dev 17.31
Turn on : 26.7851
Width : 2.638
Height : 9.946
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

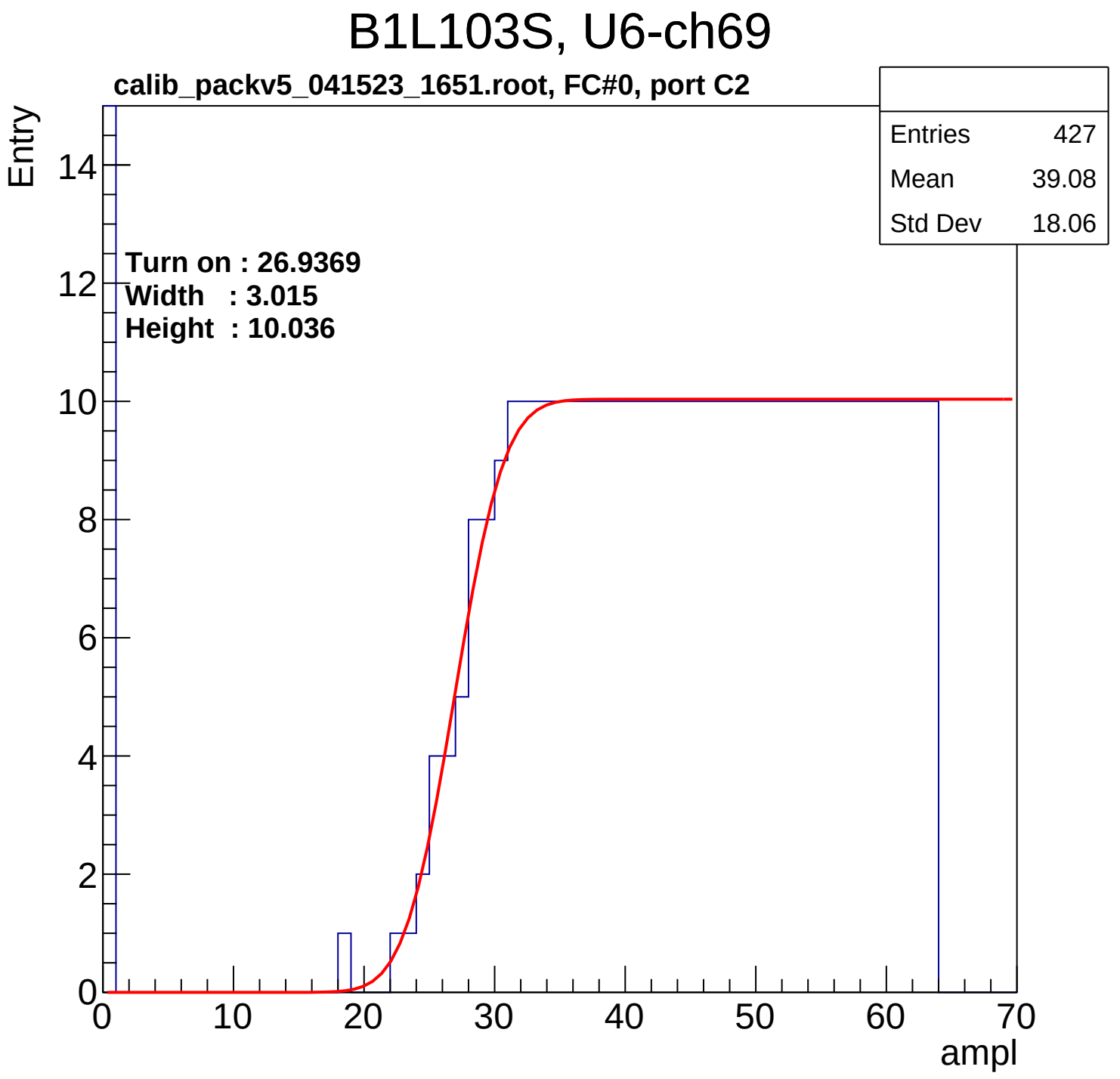

B1L103S, U6-ch64
calib_packv5_041523_1651.root, FC#0, port C2
Entries 420
Mean 39.9
Std Dev 17.21
Turn on : 26.3496
Width : 3.982
Height : 10.050
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

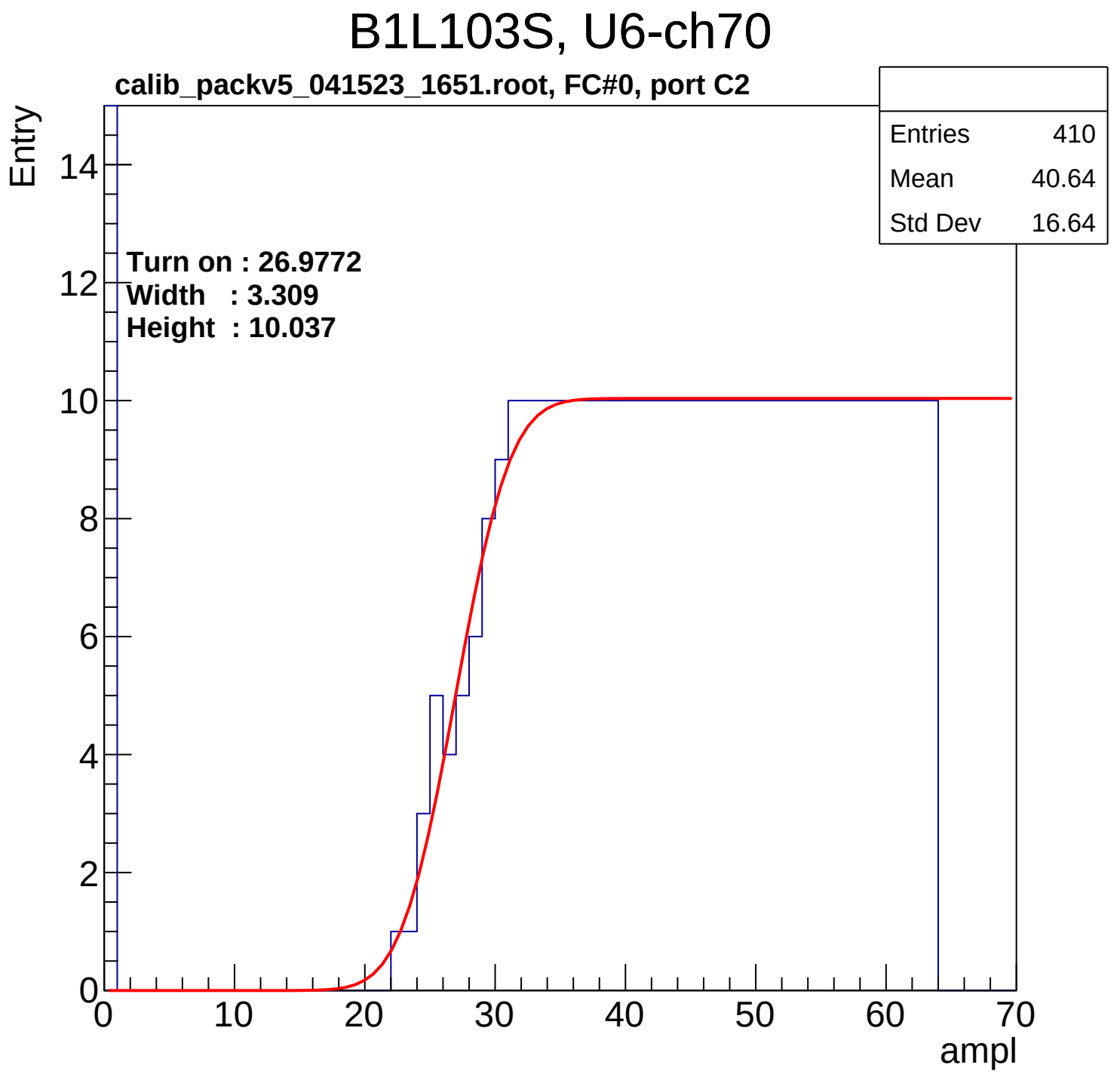

B1L103S, U6-ch65
calib_packv5_041523_1651.root, FC#0, port C2
Entries 424
Mean 39.49
Std Dev 17.62
Turn on : 25.8273
Width : 4.186
Height : 10.034
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

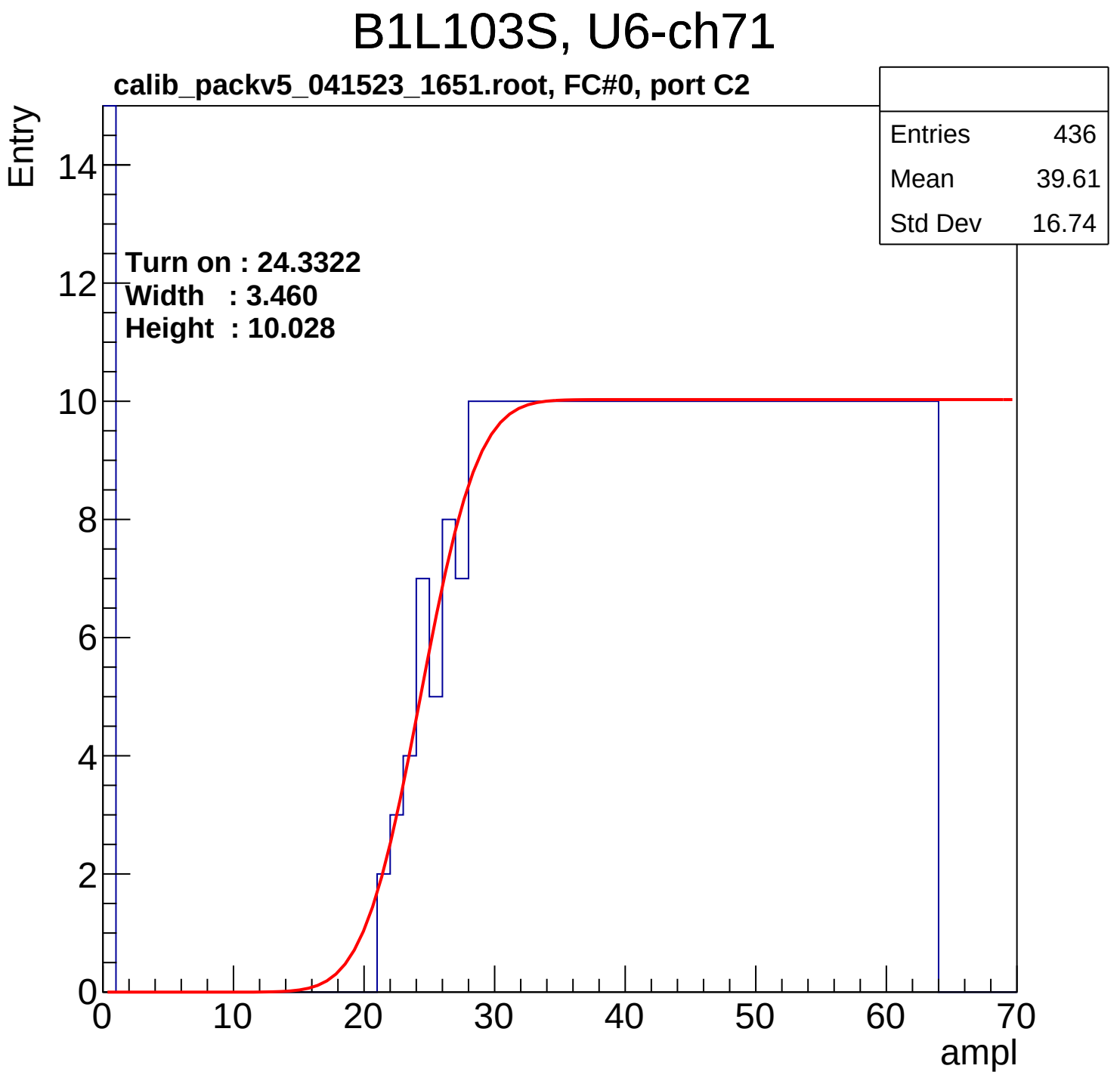

B1L103S, U6-ch66
calib_packv5_041523_1651.root, FC#0, port C2
Entries 454
Mean 38.49
Std Dev 17.46
Turn on : 23.4781
Width : 3.842
Height : 10.050
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

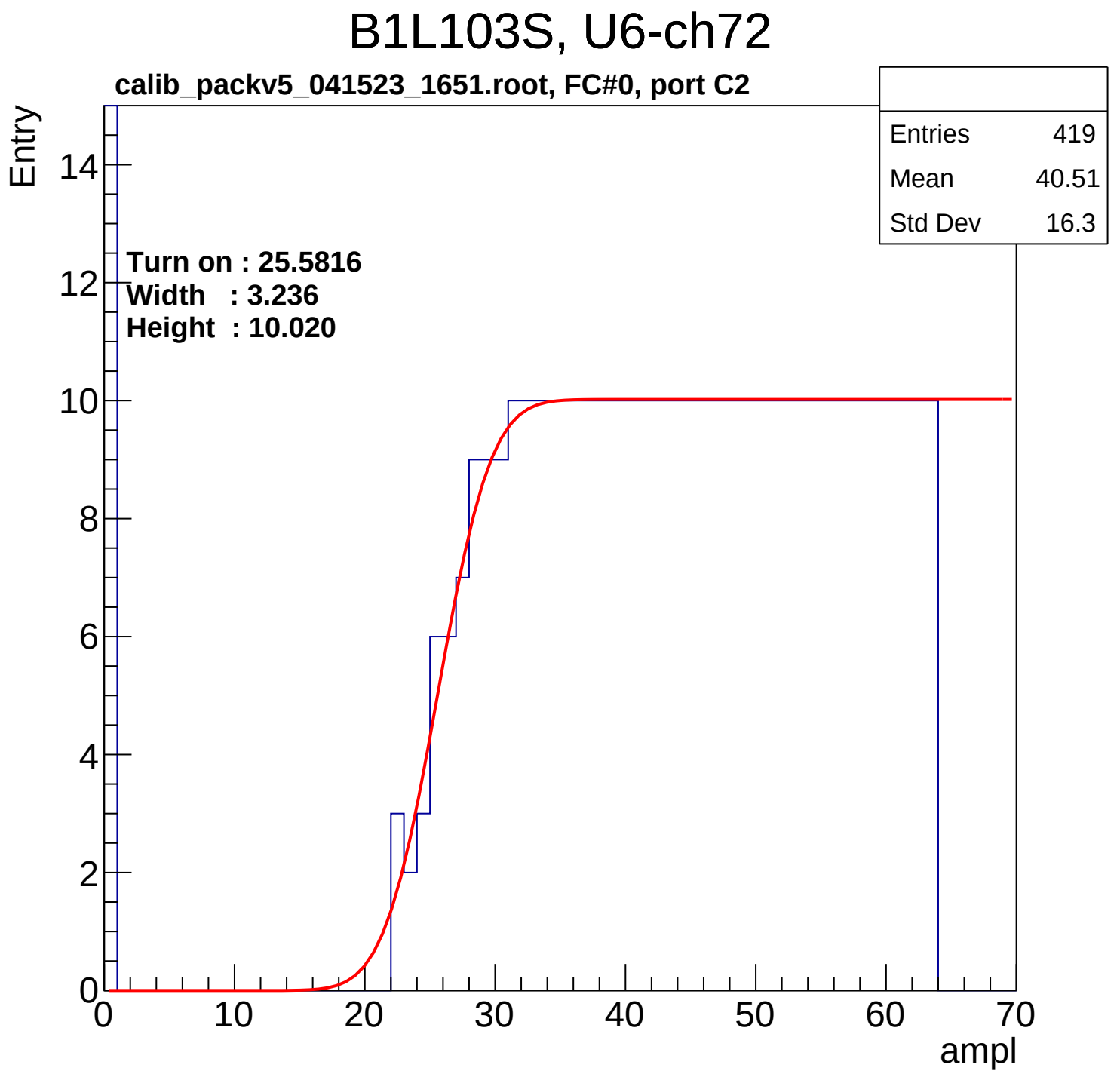

B1L103S, U6-ch67
calib_packv5_041523_1651.root, FC#0, port C2
Entries 424
Mean 40.42
Std Dev 16.11
Turn on : 24.8202
Width : 3.559
Height : 10.022
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

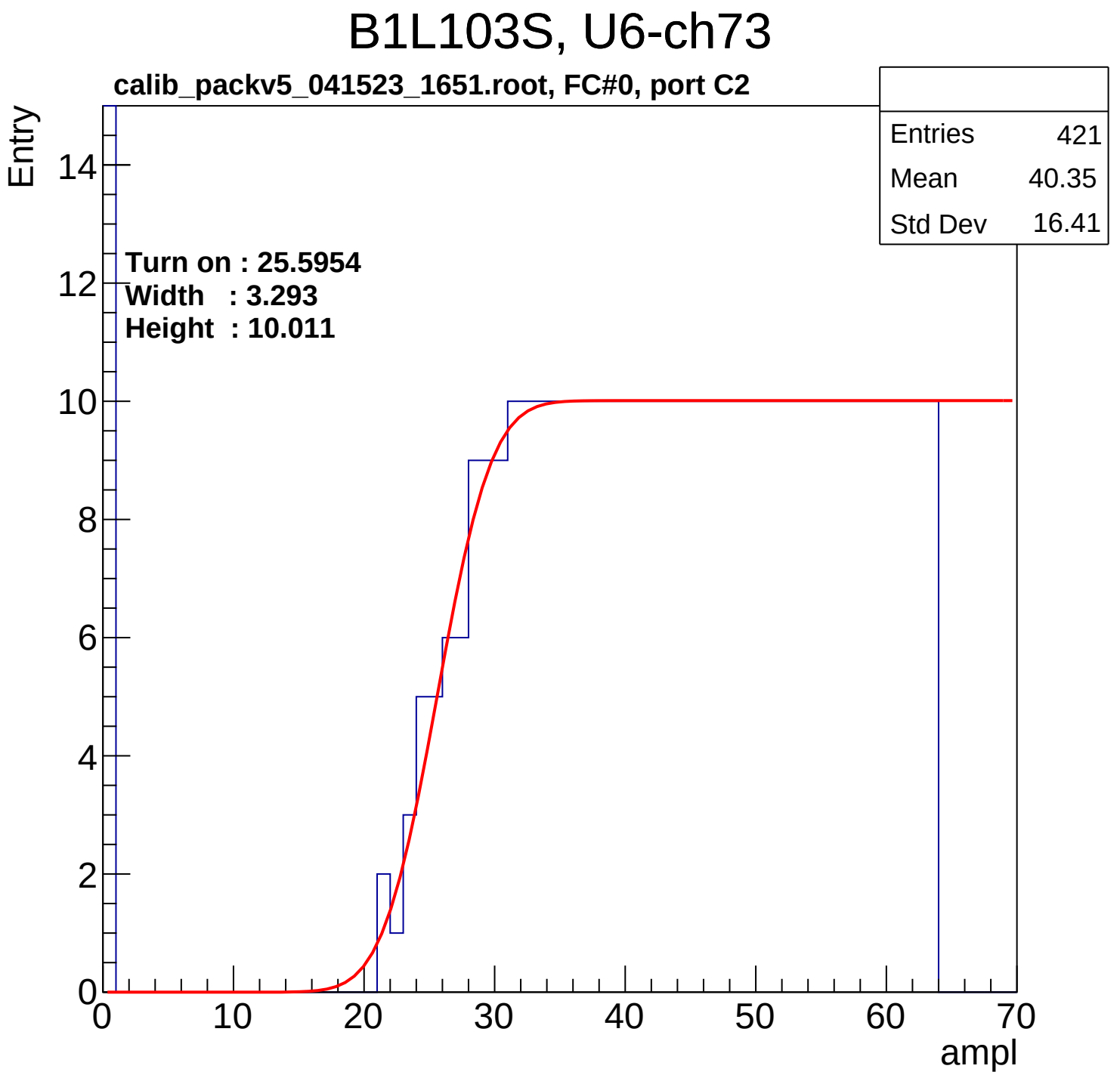

B1L103S, U6-ch68
calib_packv5_041523_1651.root, FC#0, port C2
Entries 441
Mean 38.76
Std Dev 17.73
Turn on : 25.3006
Width : 4.693
Height : 10.088
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

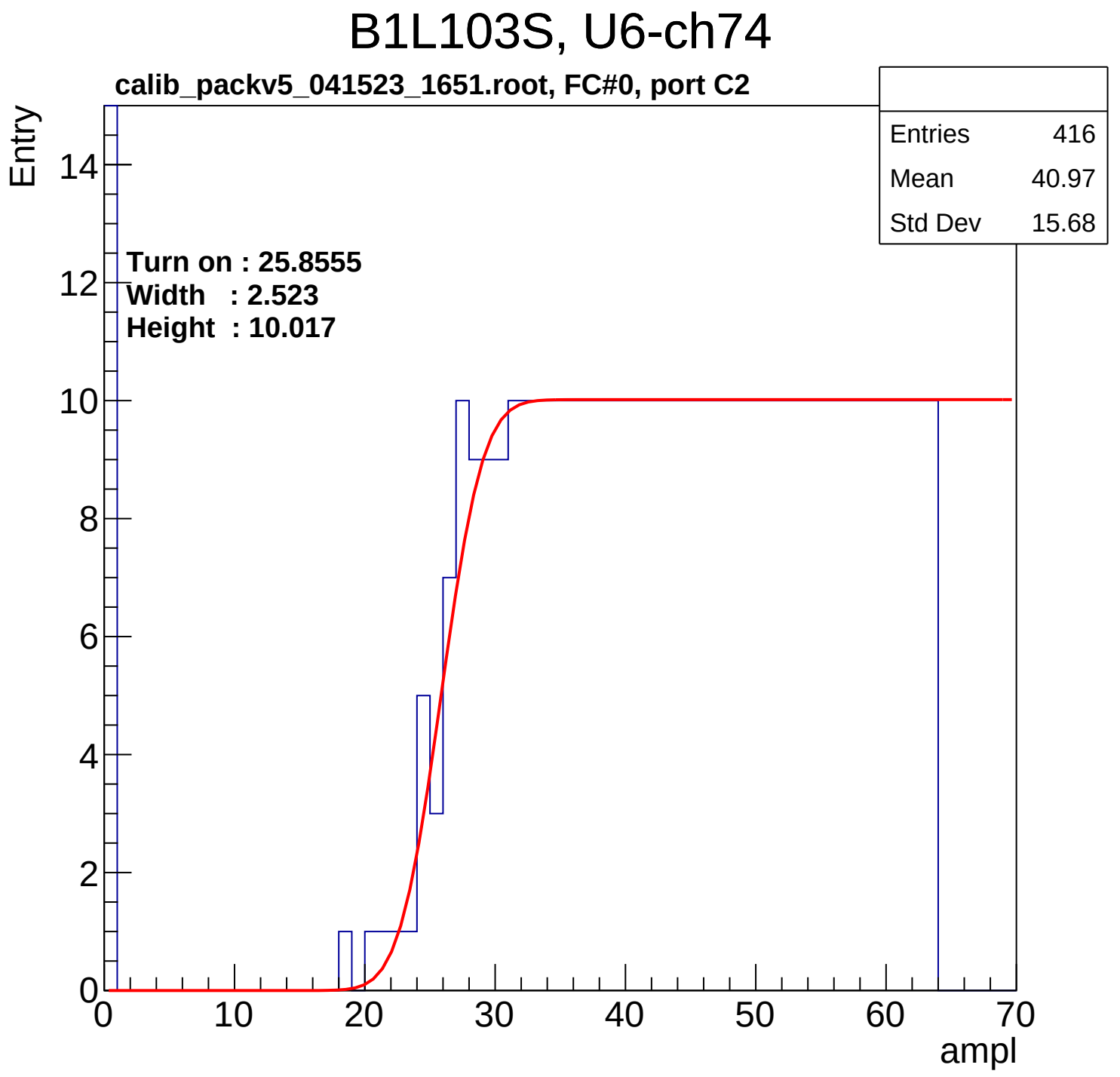

B1L103S, U6-ch69
calib_packv5_041523_1651.root, FC#0, port C2
Entries 427
Mean 39.08
Std Dev 18.06
Turn on : 26.9369
Width : 3.015
Height : 10.036
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

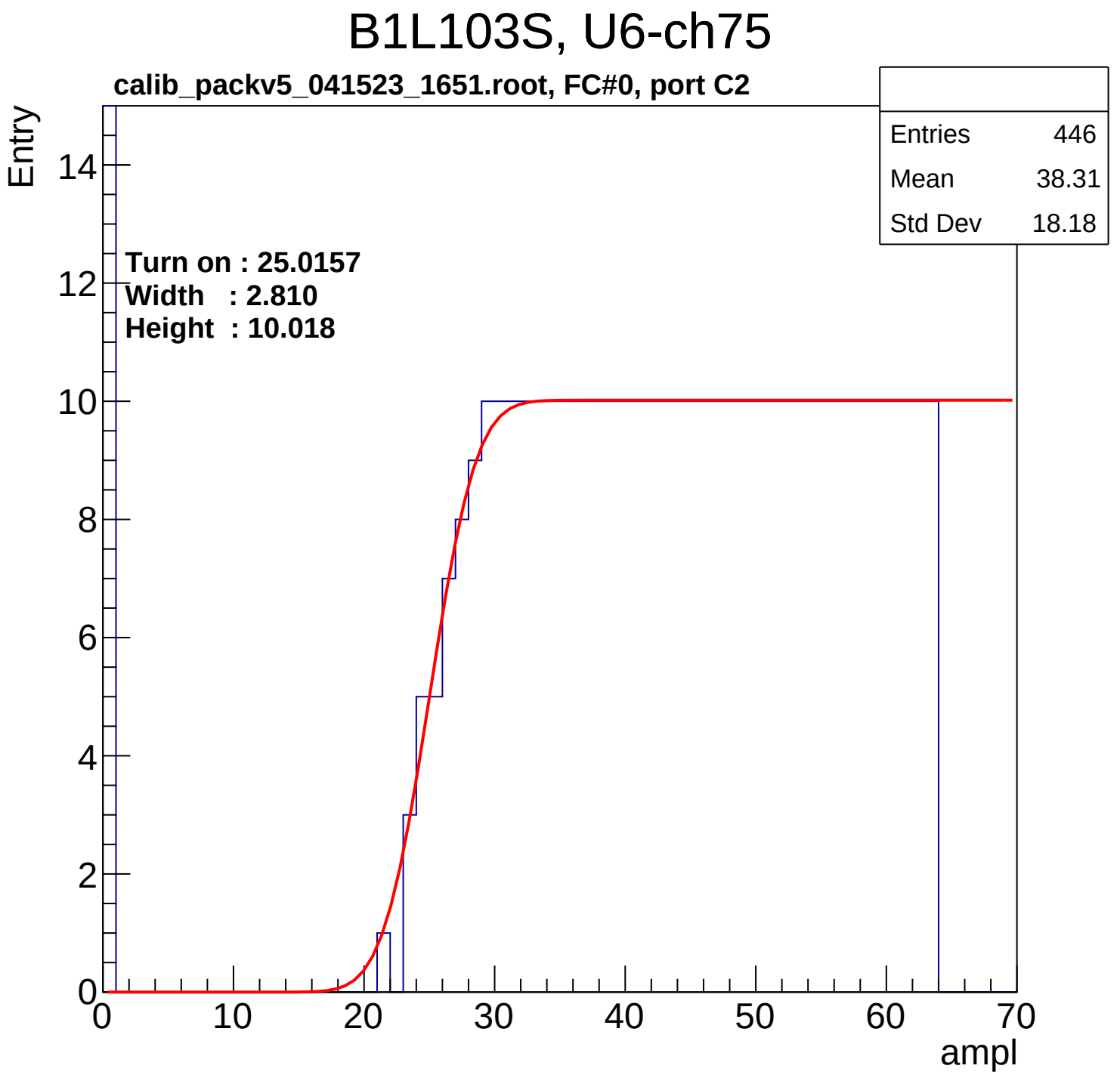

B1L103S, U6-ch70
calib_packv5_041523_1651.root, FC#0, port C2
Entries 410
Mean 40.64
Std Dev 16.64
Turn on : 26.9772
Width : 3.309
Height : 10.037
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

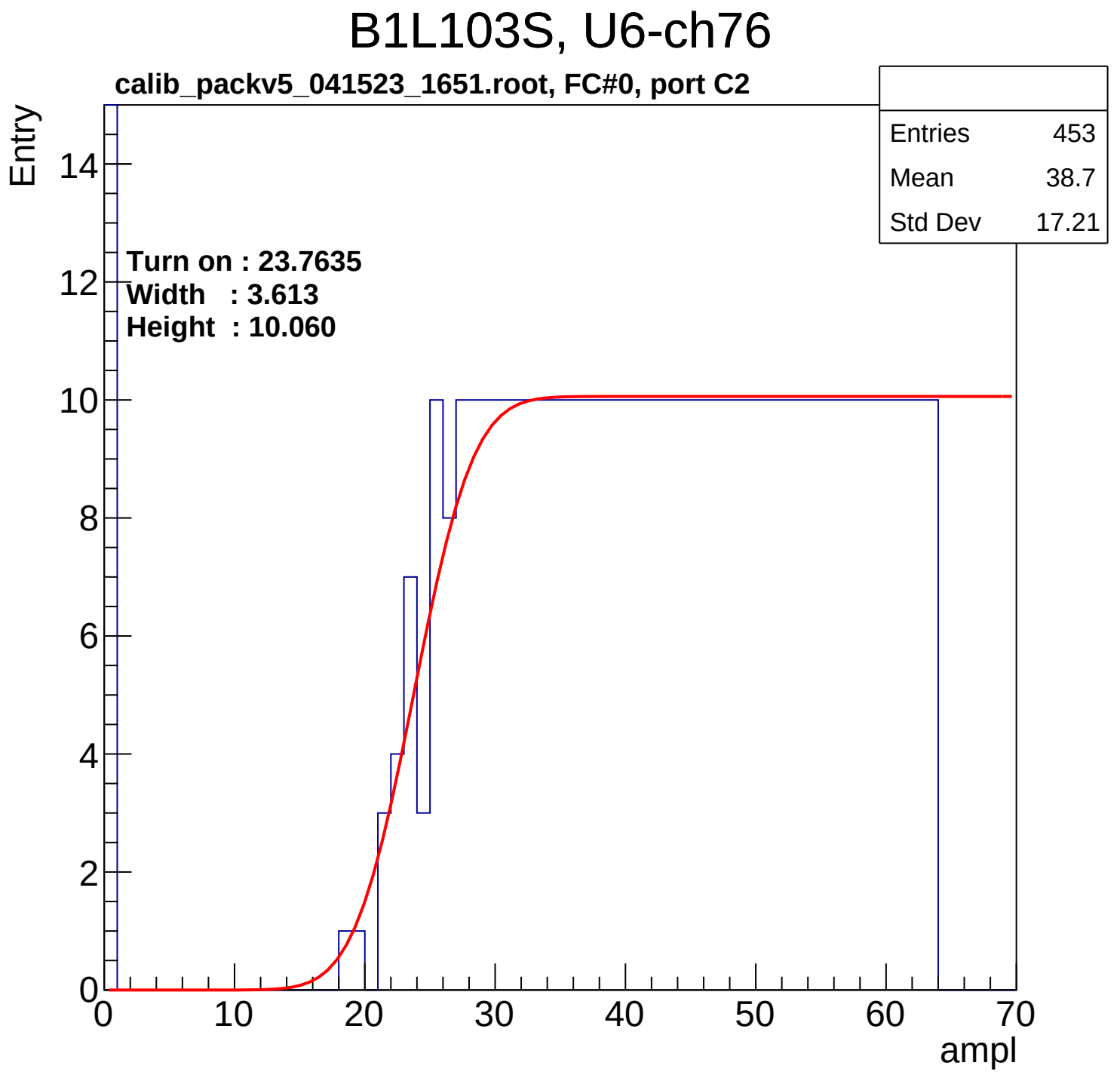

B1L103S, U6-ch71
calib_packv5_041523_1651.root, FC#0, port C2
Entries 436
Mean 39.61
Std Dev 16.74
Turn on : 24.3322
Width : 3.460
Height : 10.028
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

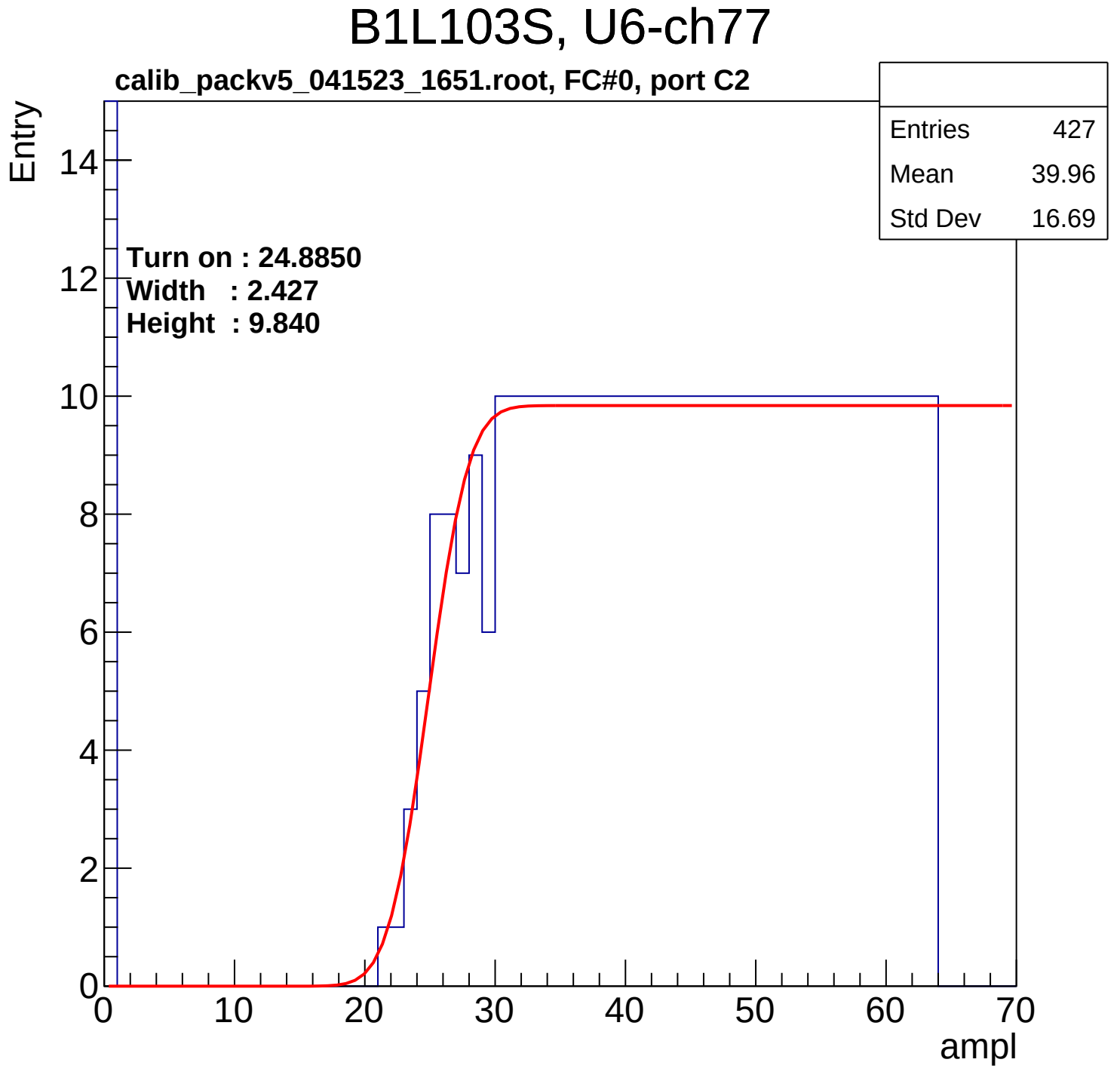

B1L103S, U6-ch72
calib_packv5_041523_1651.root, FC#0, port C2
Entries 419
Mean 40.51
Std Dev 16.3
Turn on : 25.5816
Width : 3.236
Height : 10.020
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

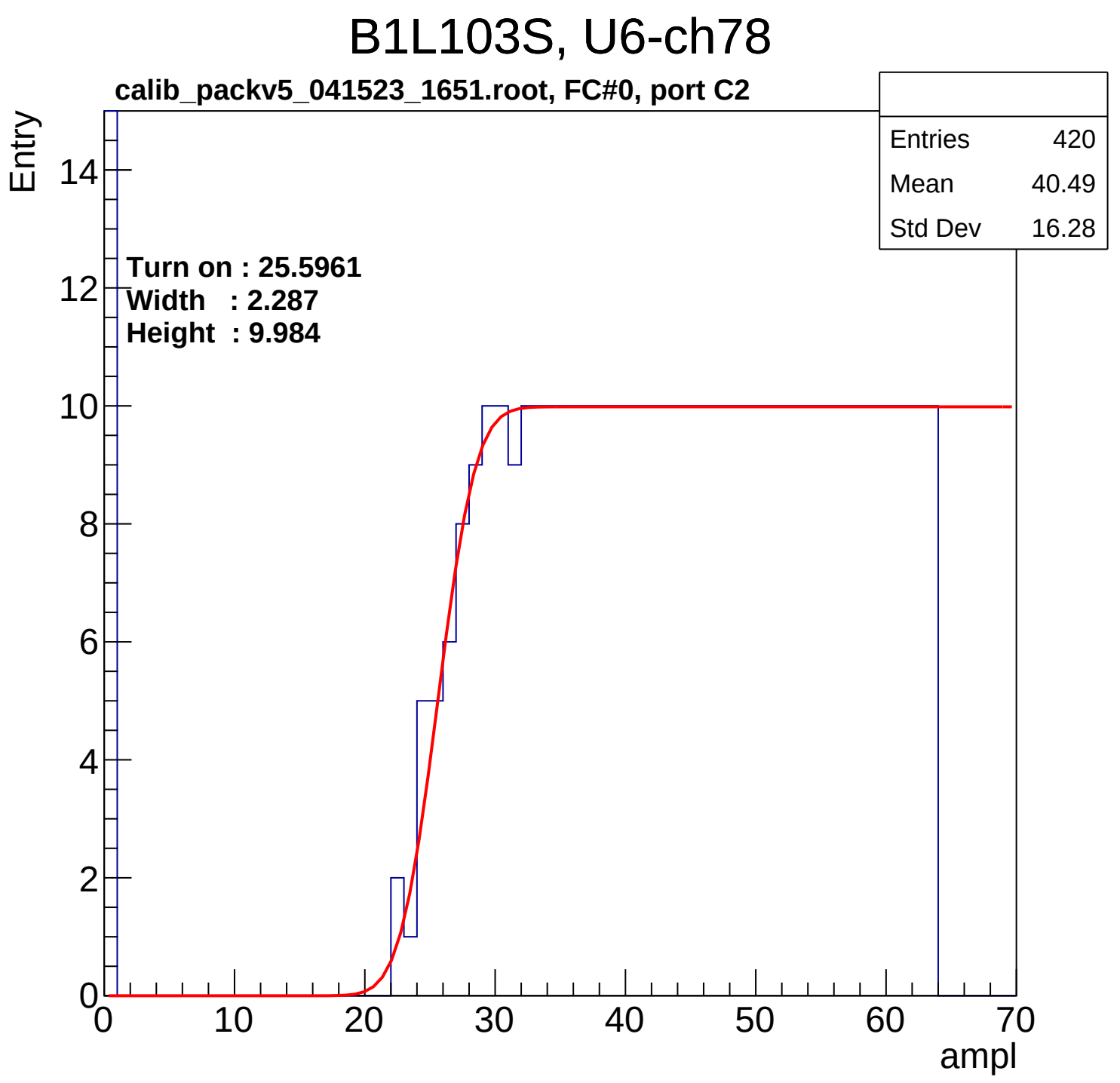

B1L103S, U6-ch73
calib_packv5_041523_1651.root, FC#0, port C2
Entries 421
Mean 40.35
Std Dev 16.41
Turn on : 25.5954
Width : 3.293
Height : 10.011
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

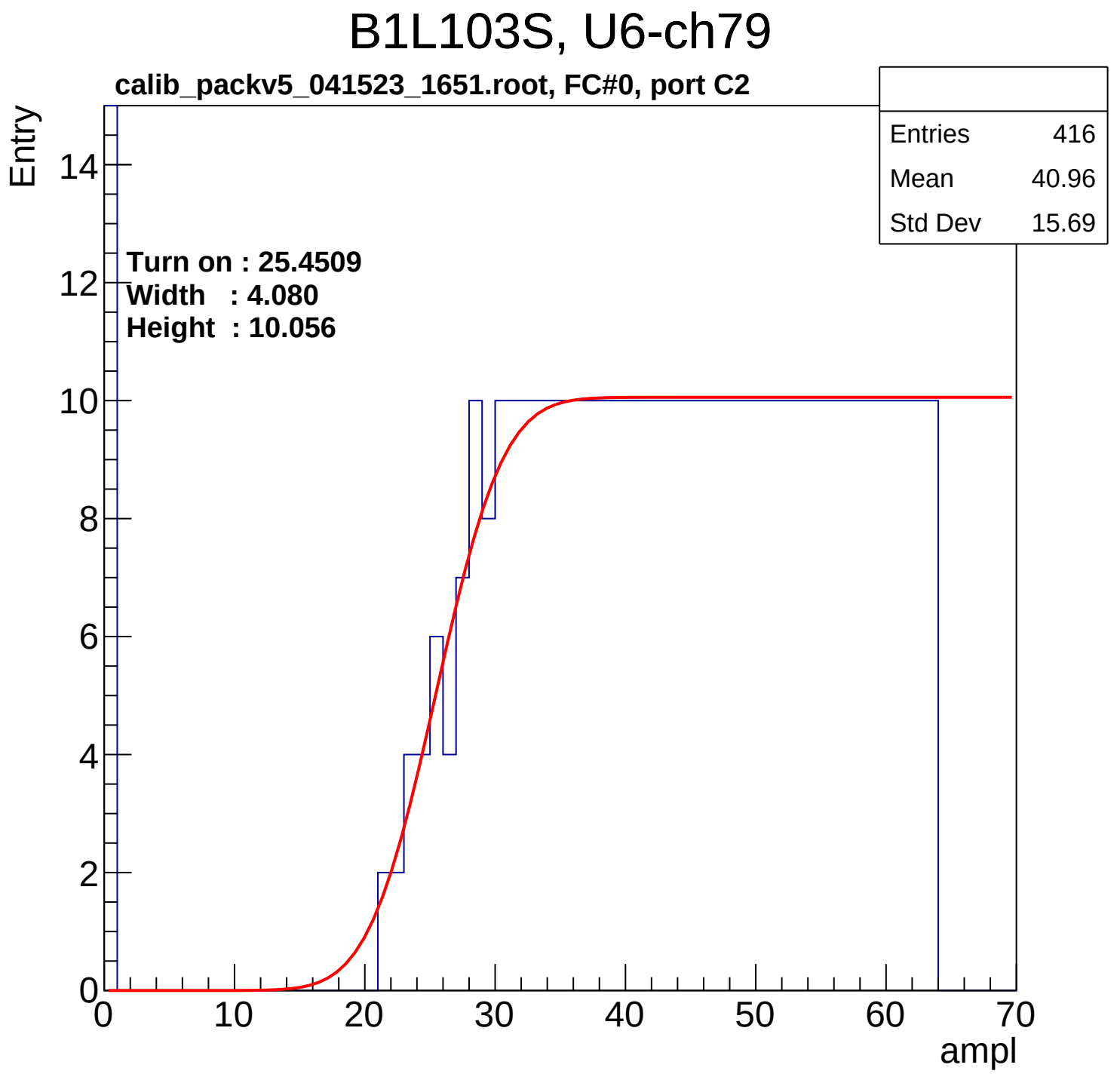

B1L103S, U6-ch74
calib_packv5_041523_1651.root, FC#0, port C2
Entries 416
Mean 40.97
Std Dev 15.68
Turn on : 25.8555
Width : 2.523
Height : 10.017
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

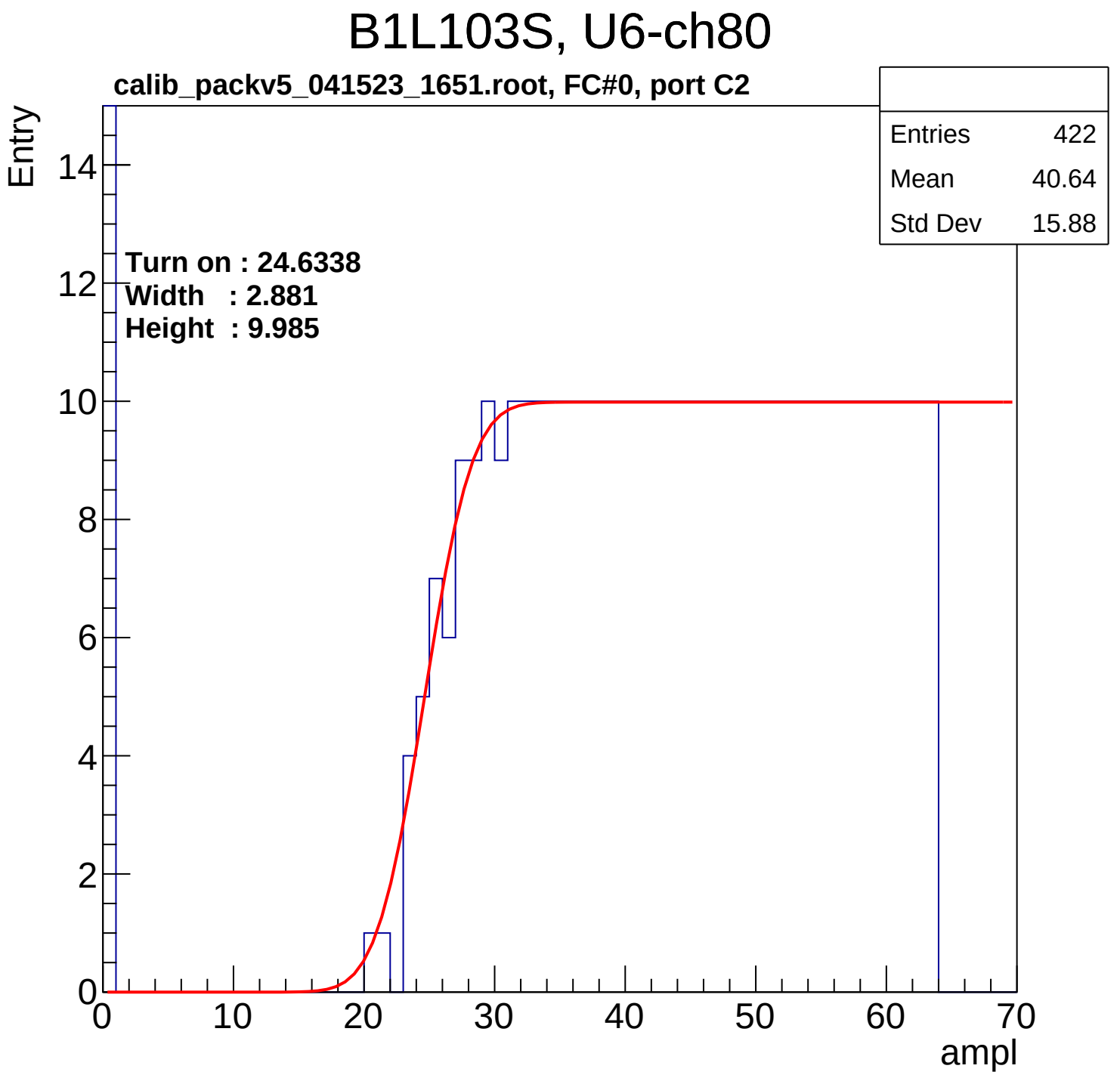

B1L103S, U6-ch75
calib_packv5_041523_1651.root, FC#0, port C2
Entries 446
Mean 38.31
Std Dev 18.18
Turn on : 25.0157
Width : 2.810
Height : 10.018
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

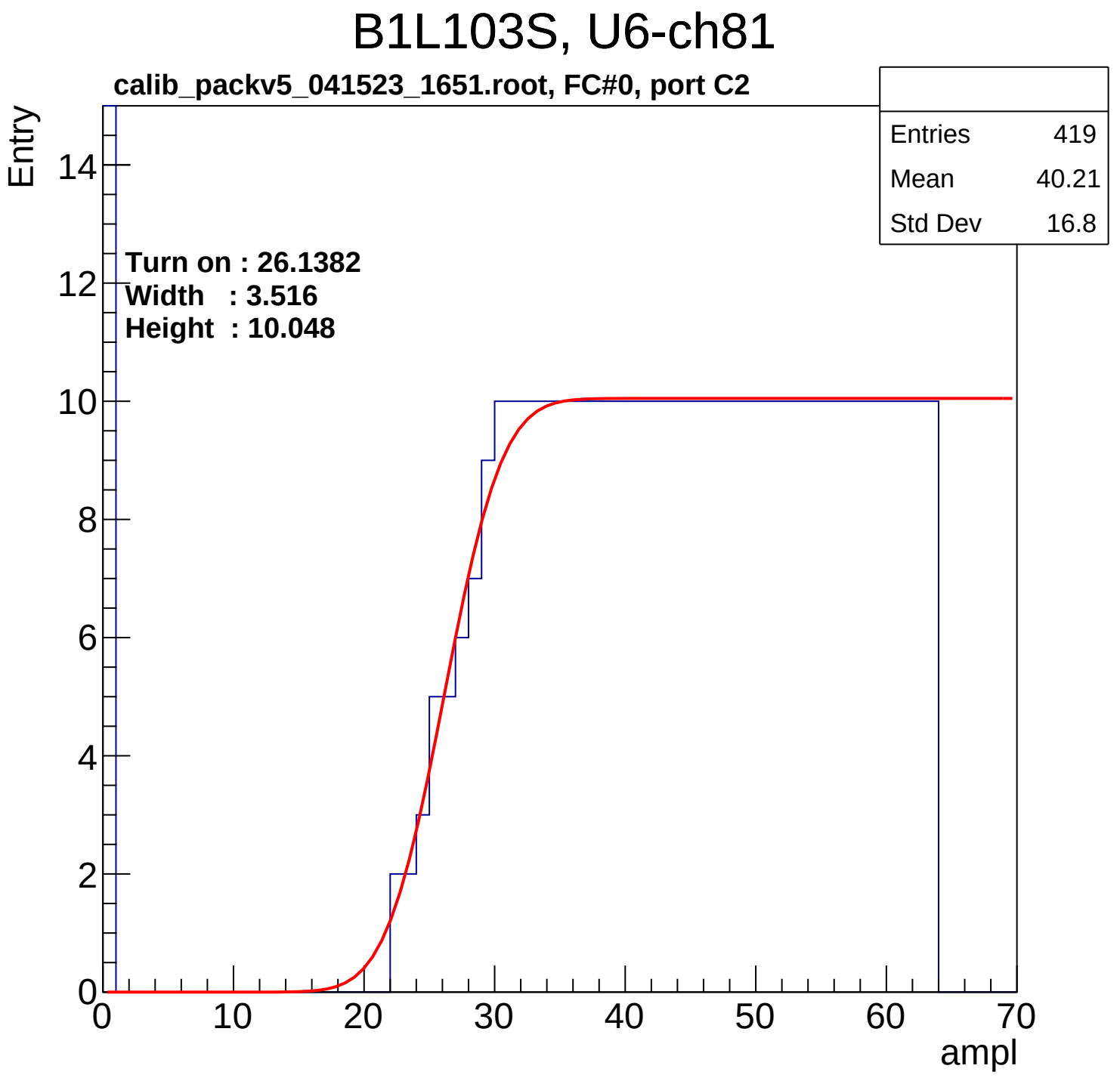

B1L103S, U6-ch76
calib_packv5_041523_1651.root, FC#0, port C2
Entries 453
Mean 38.7
Std Dev 17.21
Turn on : 23.7635
Width : 3.613
Height : 10.060
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

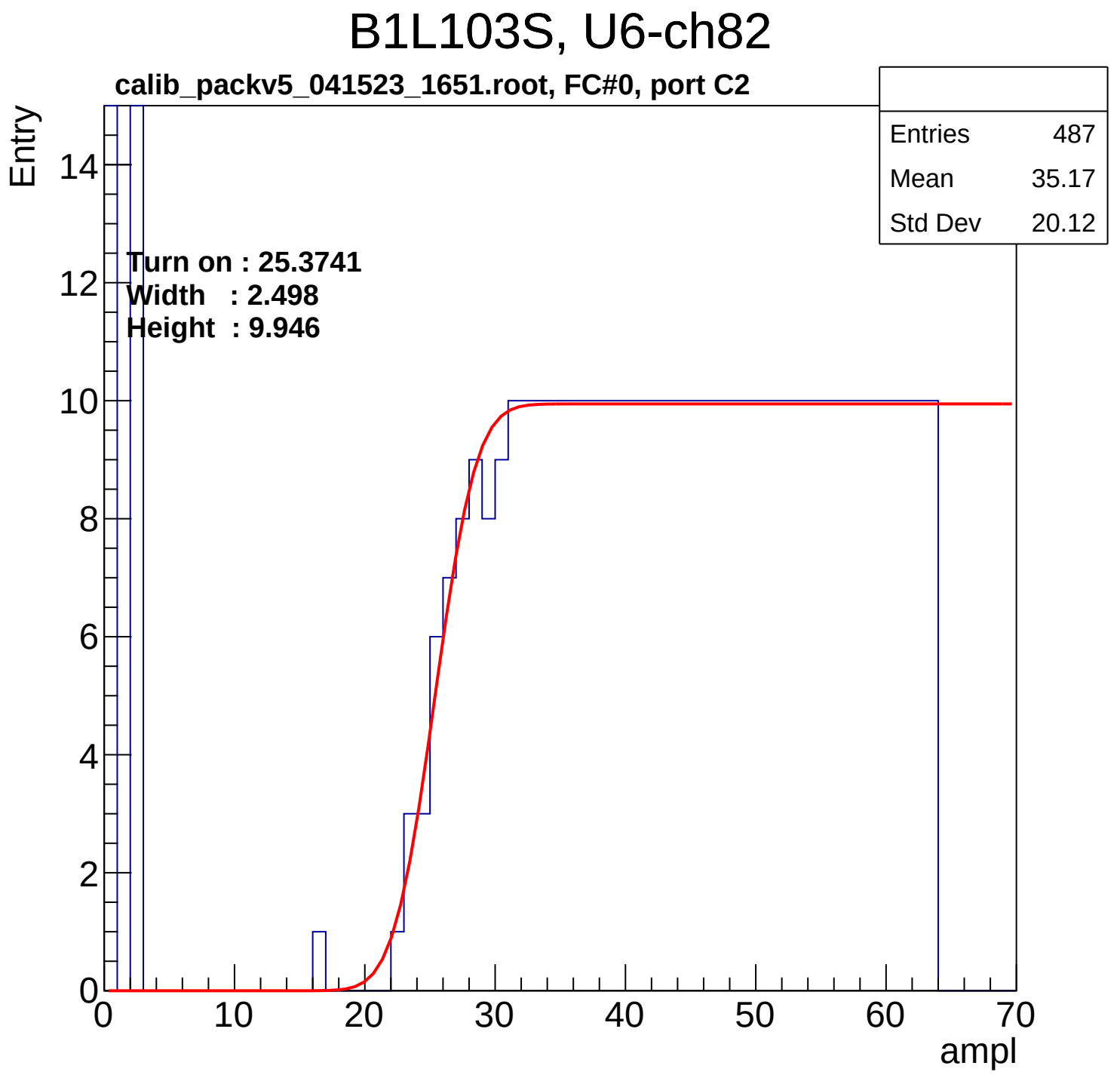

B1L103S, U6-ch77
calib_packv5_041523_1651.root, FC#0, port C2
Entries 427
Mean 39.96
Std Dev 16.69
Turn on : 24.8850
Width : 2.427
Height : 9.840
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

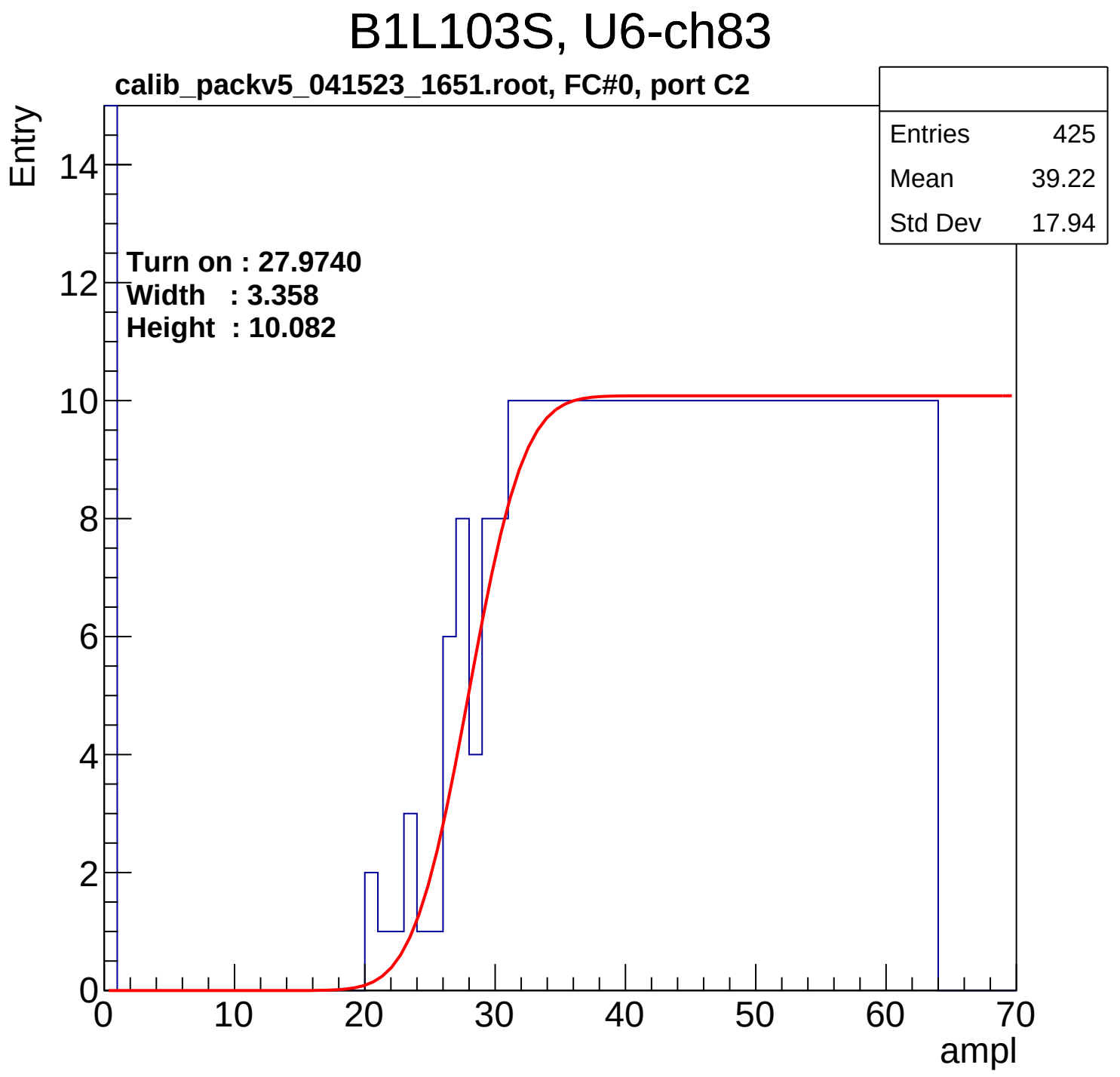

B1L103S, U6-ch78
calib_packv5_041523_1651.root, FC#0, port C2
Entries 420
Mean 40.49
Std Dev 16.28
Turn on : 25.5961
Width : 2.287
Height : 9.984
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

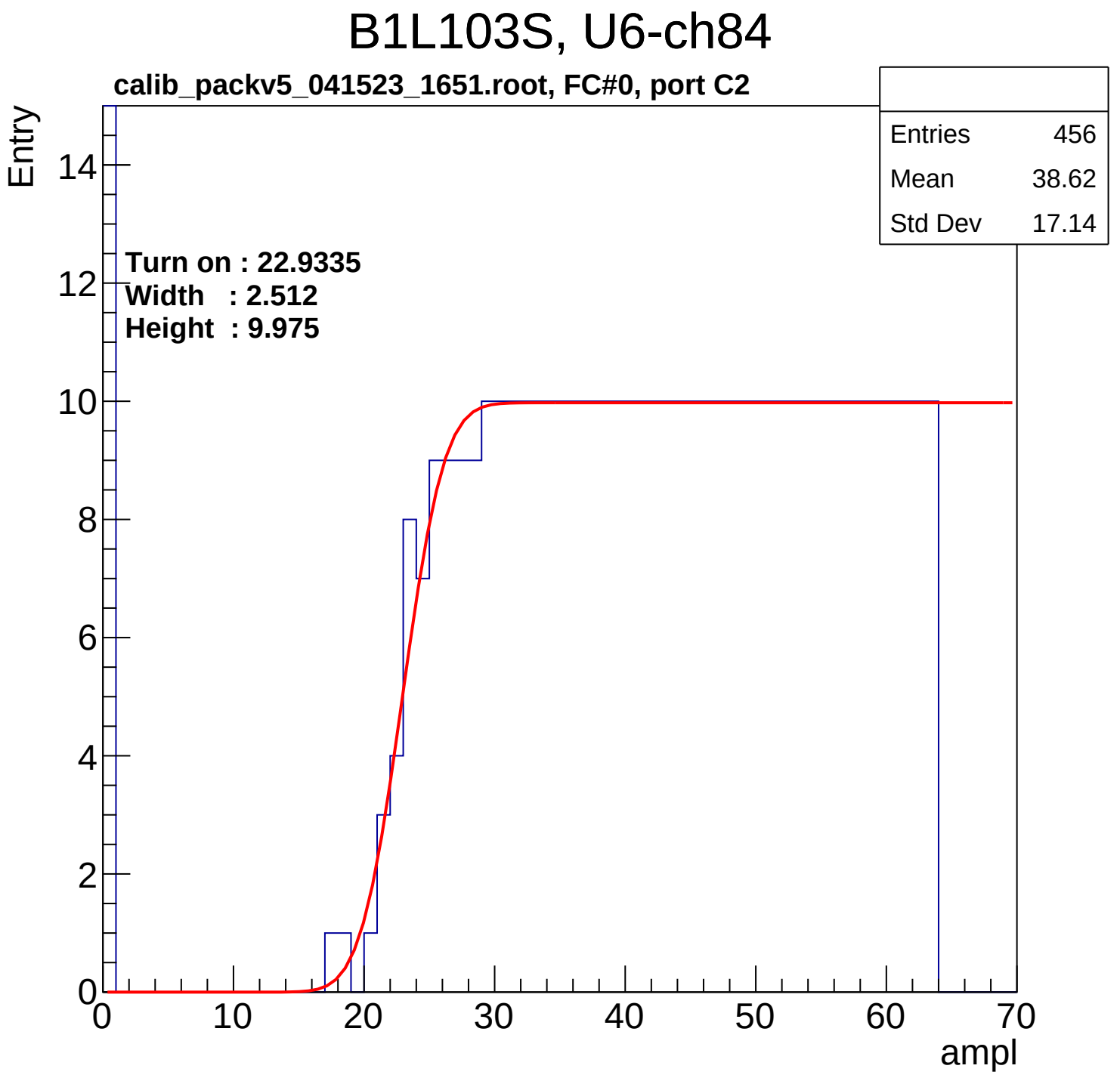

B1L103S, U6-ch79
calib_packv5_041523_1651.root, FC#0, port C2
Entries 416
Mean 40.96
Std Dev 15.69
Turn on : 25.4509
Width : 4.080
Height : 10.056
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

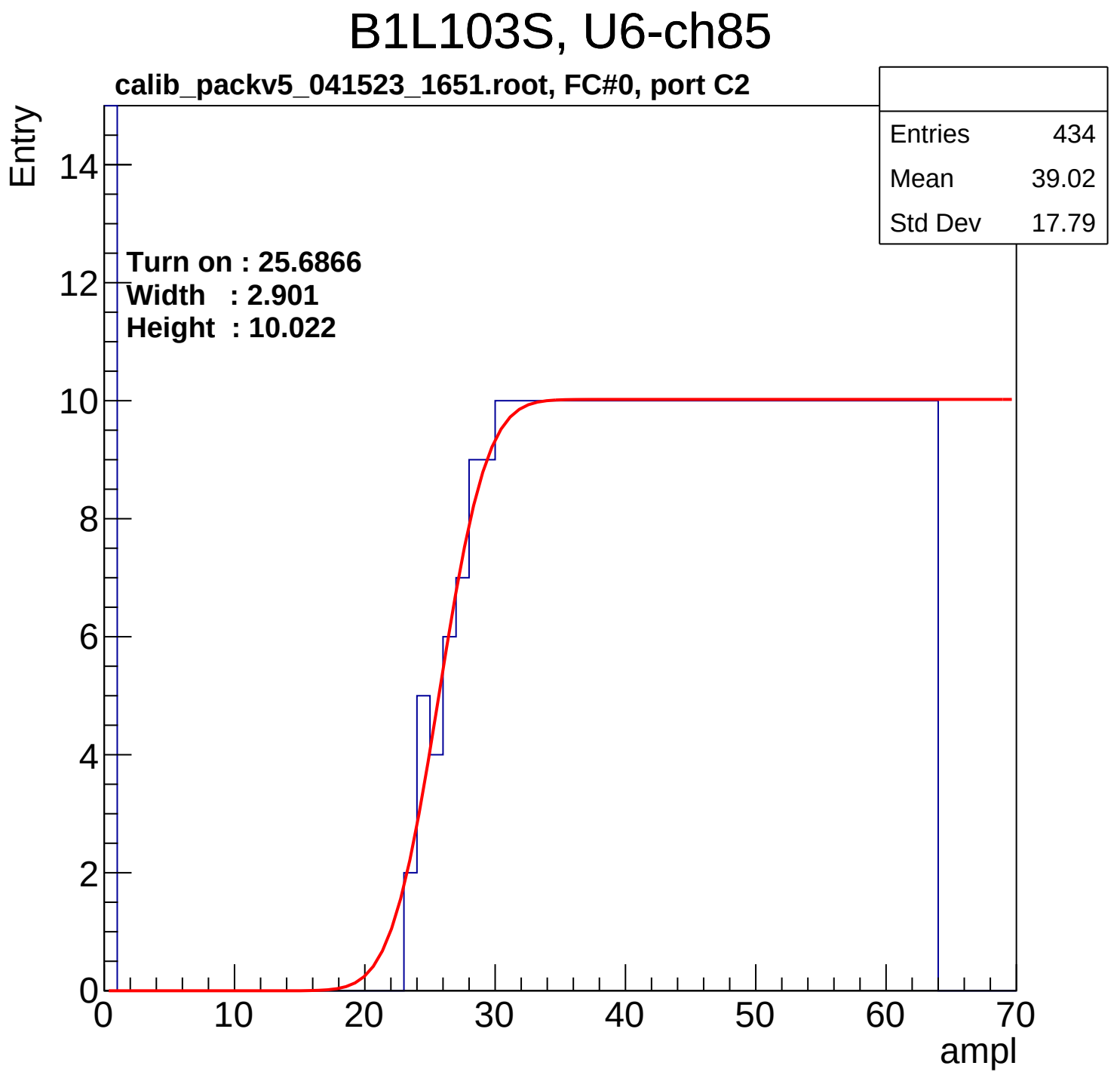

B1L103S, U6-ch80
calib_packv5_041523_1651.root, FC#0, port C2
Entries 422
Mean 40.64
Std Dev 15.88
Turn on : 24.6338
Width : 2.881
Height : 9.985
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

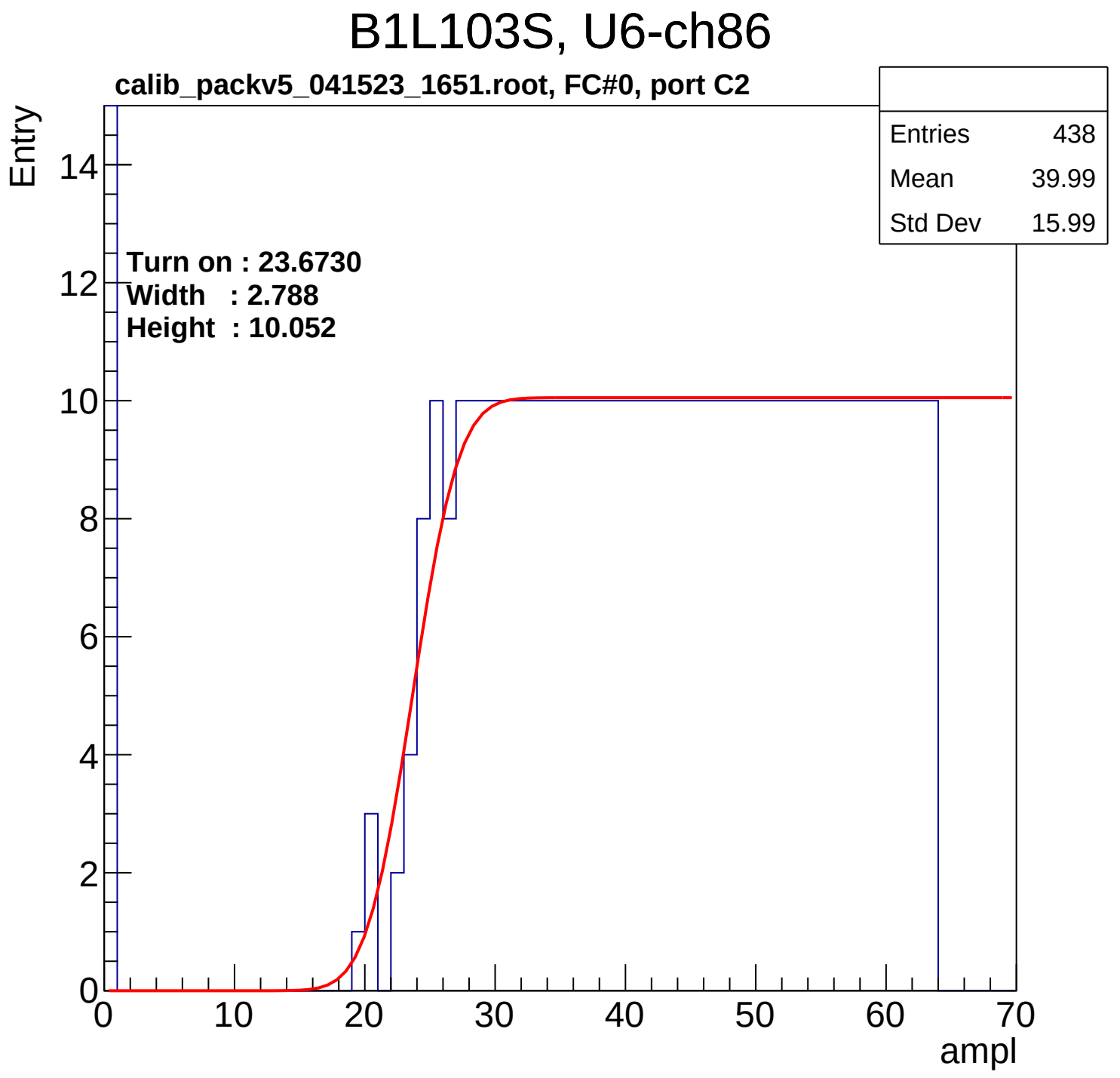

B1L103S, U6-ch81
calib_packv5_041523_1651.root, FC#0, port C2
Entries 419
Mean 40.21
Std Dev 16.8
Turn on : 26.1382
Width : 3.516
Height : 10.048
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

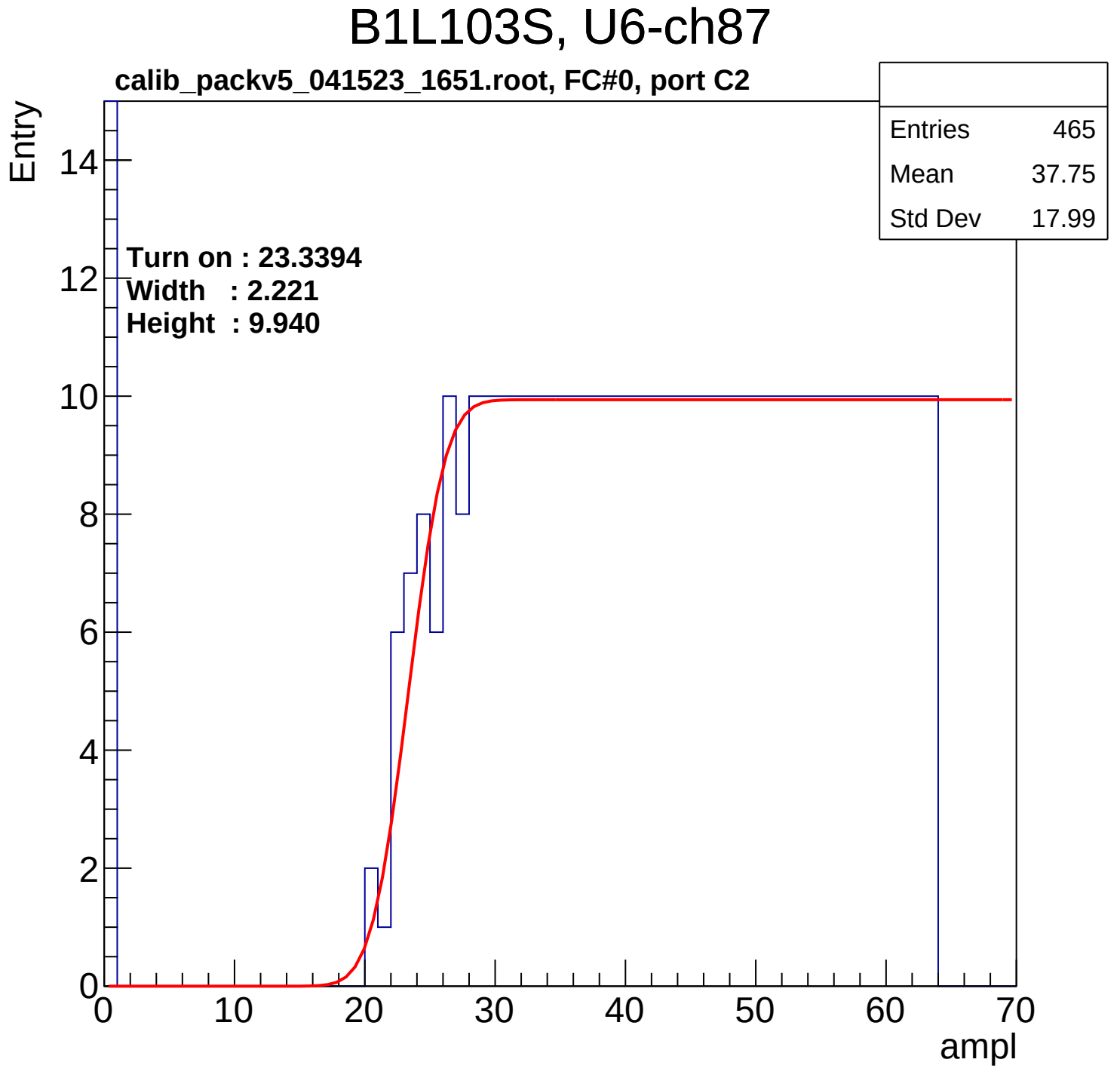

B1L103S, U6-ch82
calib_packv5_041523_1651.root, FC#0, port C2
Entries 487
Mean 35.17
Std Dev 20.12
Turn on : 25.3741
Width : 2.498
Height : 9.946
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

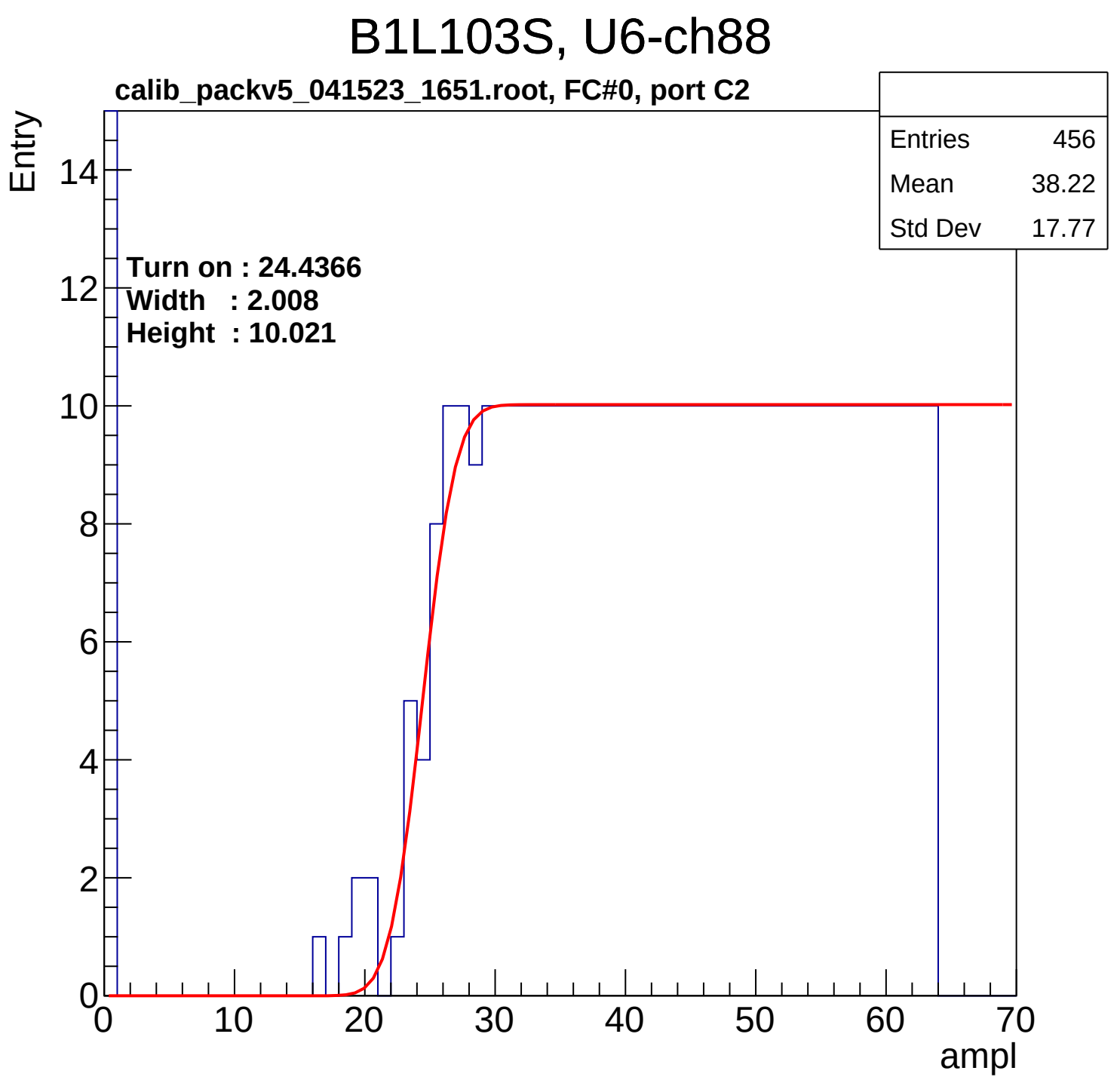

B1L103S, U6-ch83
calib_packv5_041523_1651.root, FC#0, port C2
Entries 425
Mean 39.22
Std Dev 17.94
Turn on : 27.9740
Width : 3.358
Height : 10.082
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

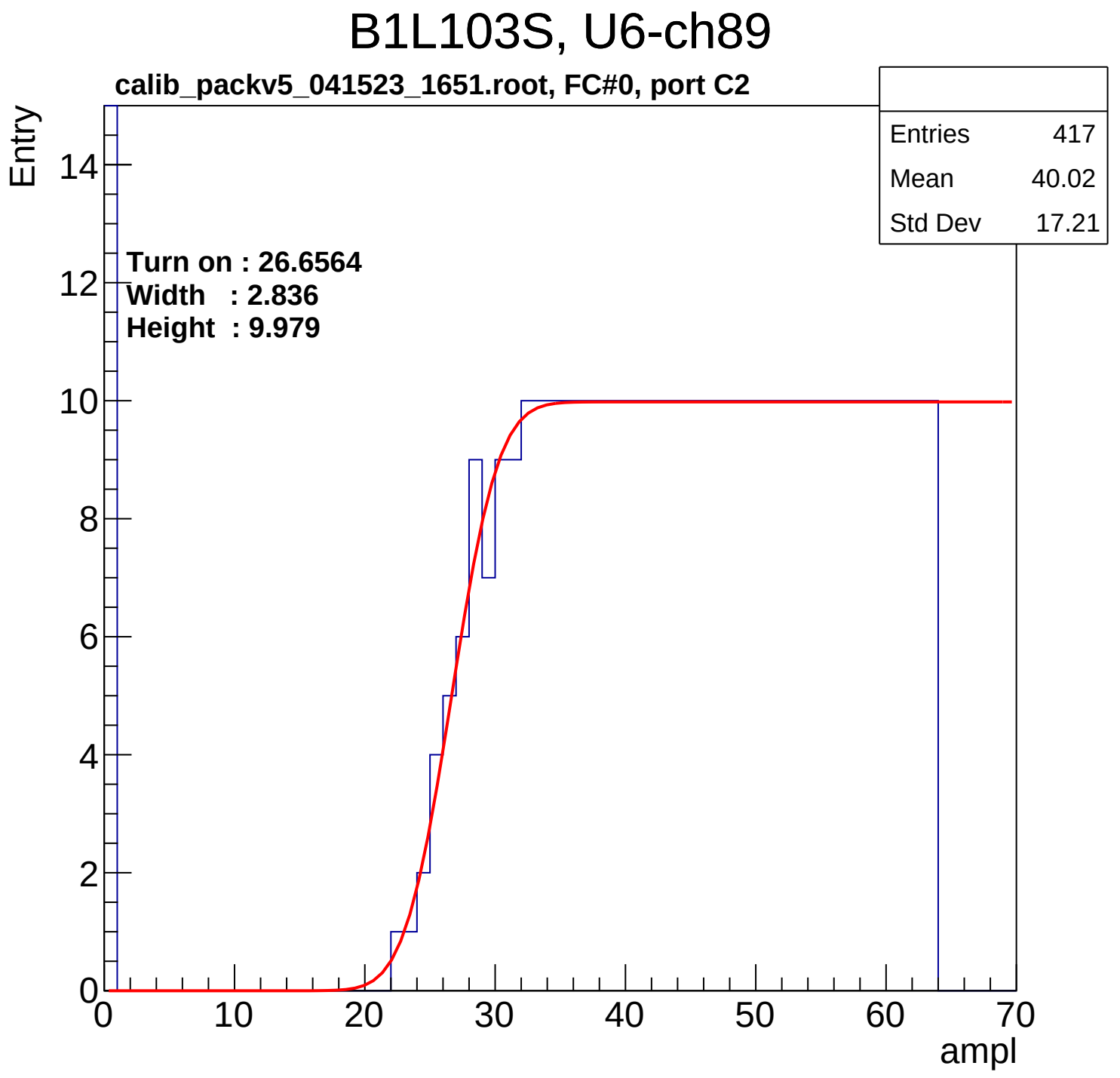

B1L103S, U6-ch84
calib_packv5_041523_1651.root, FC#0, port C2
Entries 456
Mean 38.62
Std Dev 17.14
Turn on : 22.9335
Width : 2.512
Height : 9.975
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

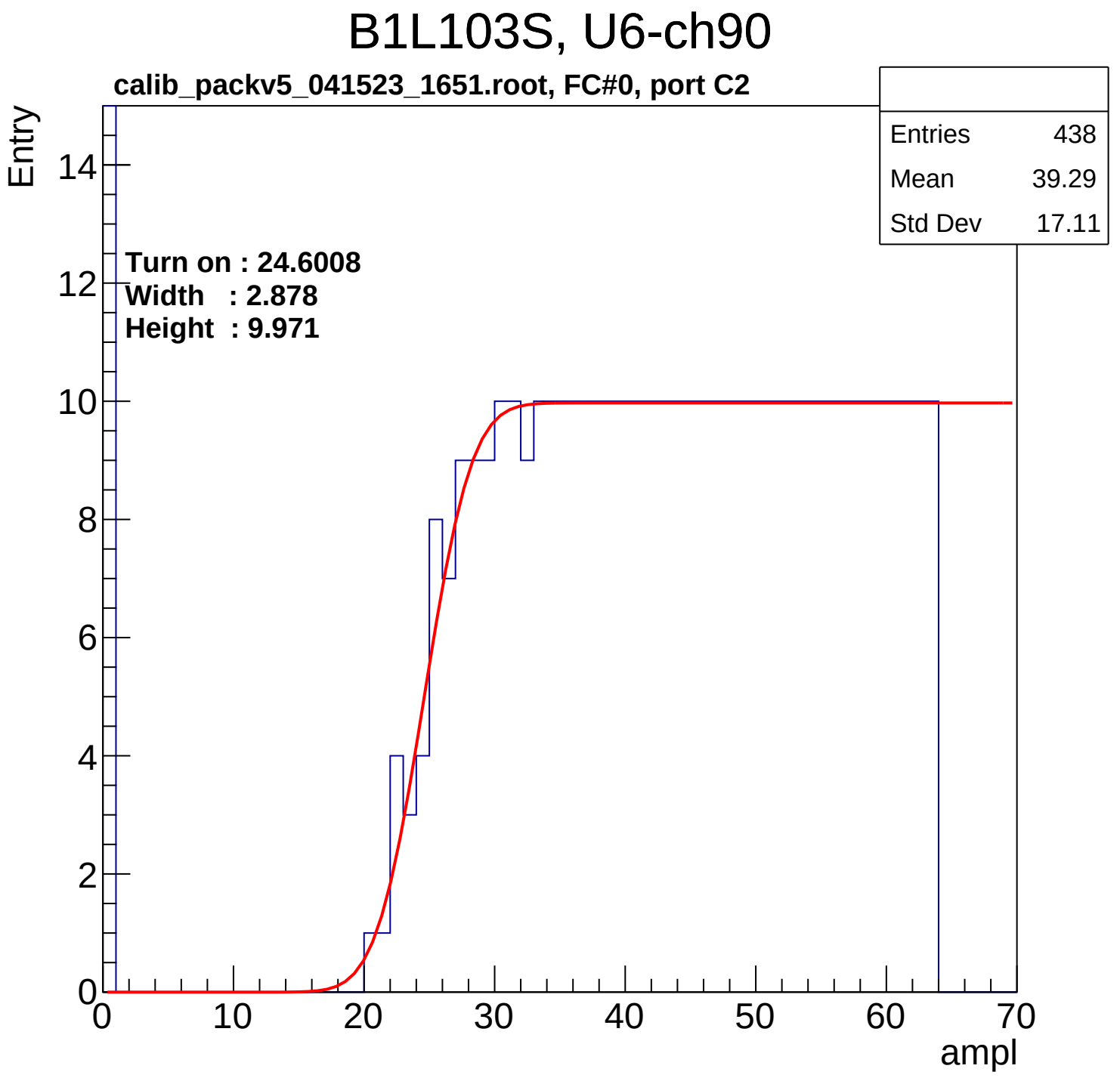

B1L103S, U6-ch85
calib_packv5_041523_1651.root, FC#0, port C2
Entries 434
Mean 39.02
Std Dev 17.79
Turn on : 25.6866
Width : 2.901
Height : 10.022
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

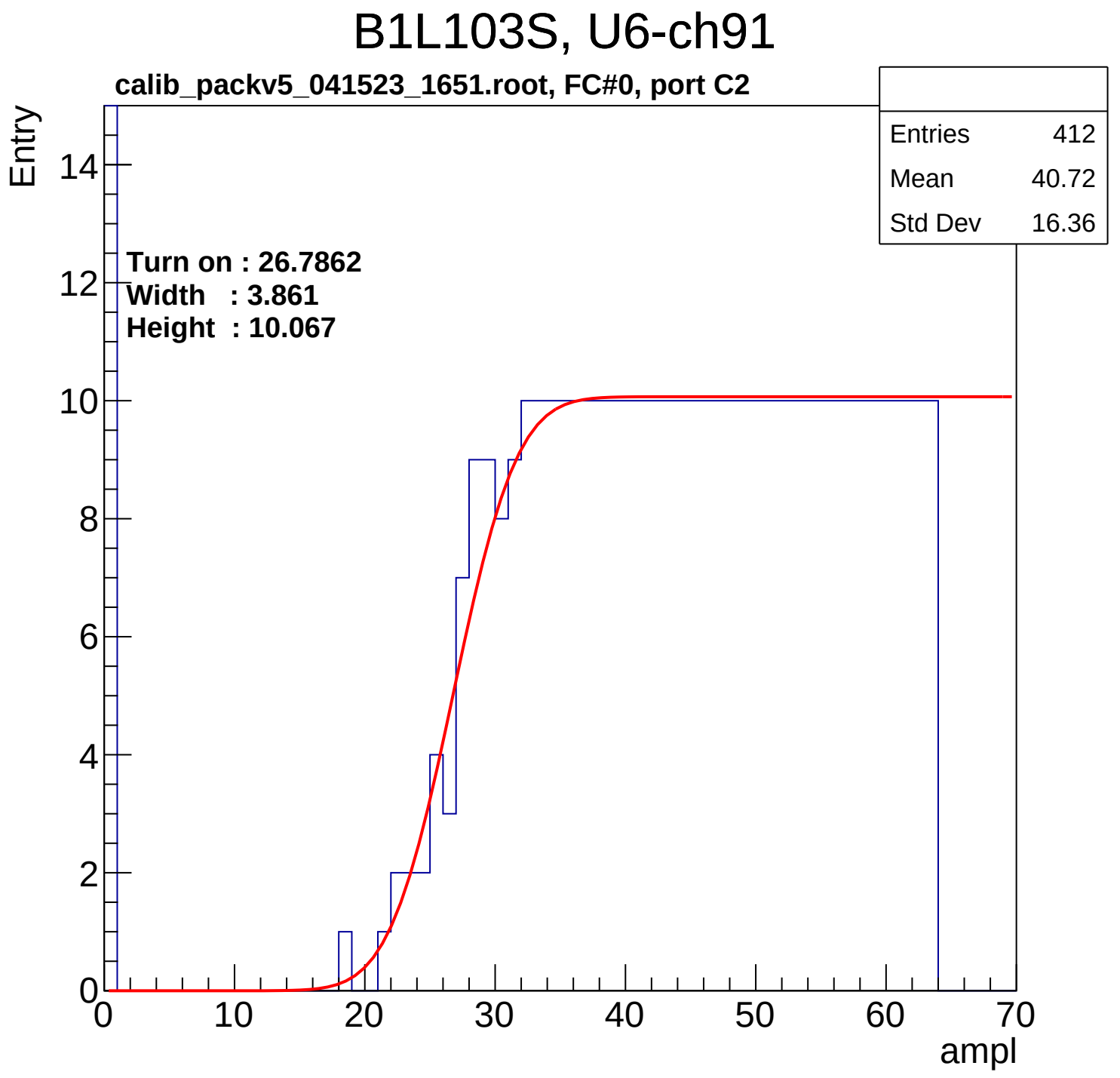

B1L103S, U6-ch86
calib_packv5_041523_1651.root, FC#0, port C2
Entries 438
Mean 39.99
Std Dev 15.99
Turn on : 23.6730
Width : 2.788
Height : 10.052
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

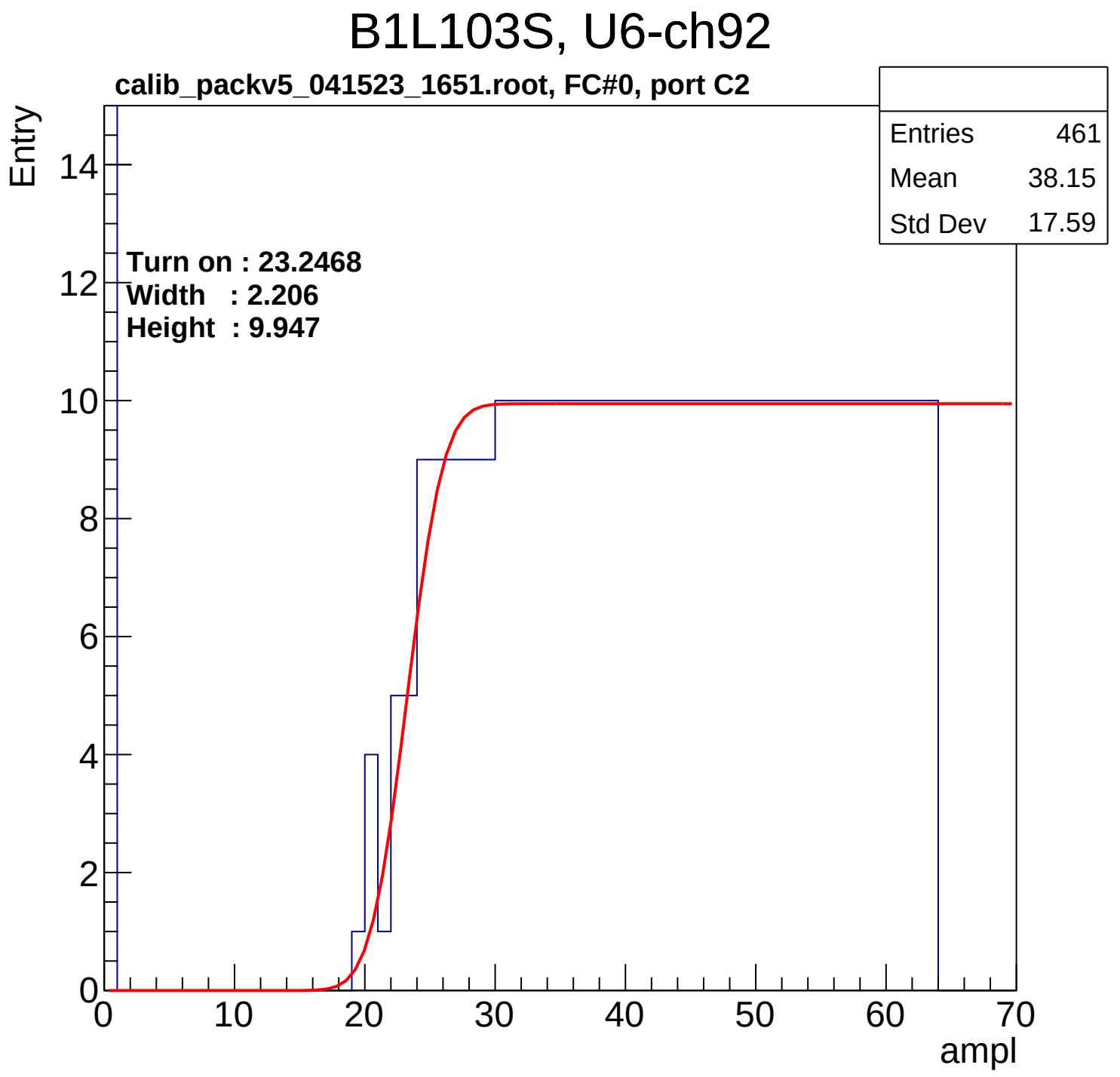

B1L103S, U6-ch87
calib_packv5_041523_1651.root, FC#0, port C2
Entries 465
Mean 37.75
Std Dev 17.99
Turn on : 23.3394
Width : 2.221
Height : 9.940
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

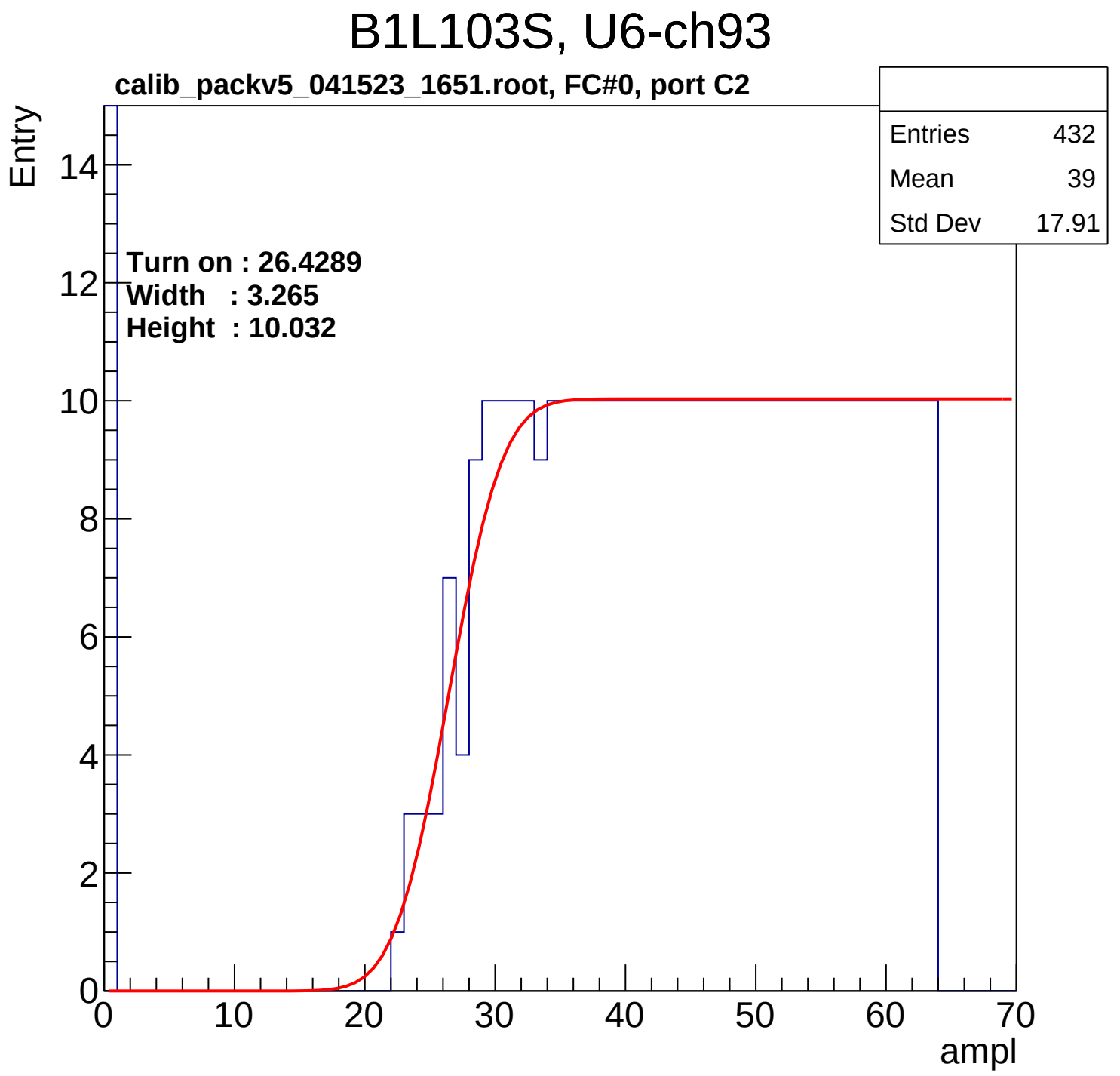

B1L103S, U6-ch88
calib_packv5_041523_1651.root, FC#0, port C2
Entries 456
Mean 38.22
Std Dev 17.77
Turn on : 24.4366
Width : 2.008
Height : 10.021
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

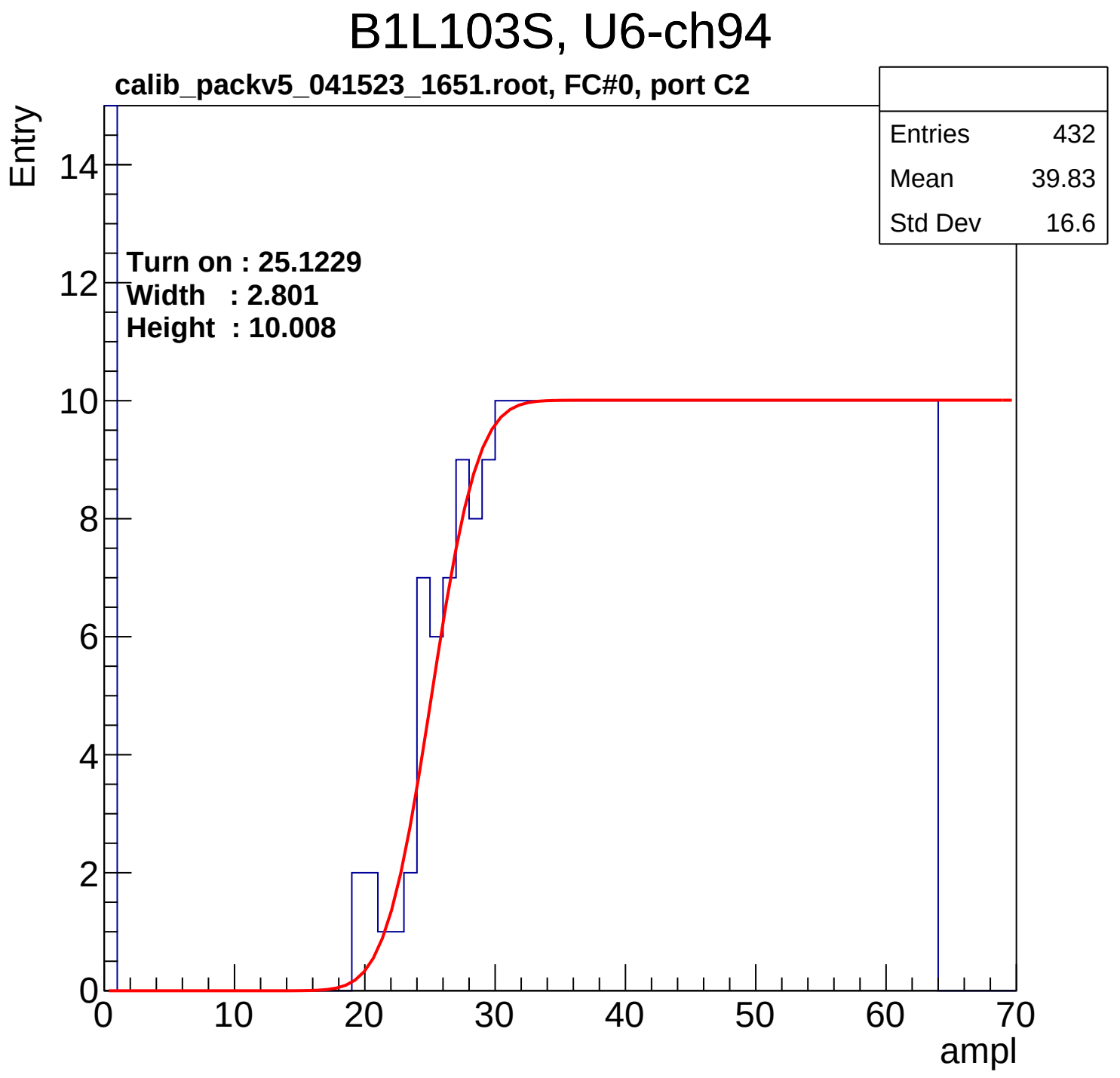

B1L103S, U6-ch89
calib_packv5_041523_1651.root, FC#0, port C2
Entries 417
Mean 40.02
Std Dev 17.21
Turn on : 26.6564
Width : 2.836
Height : 9.979
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

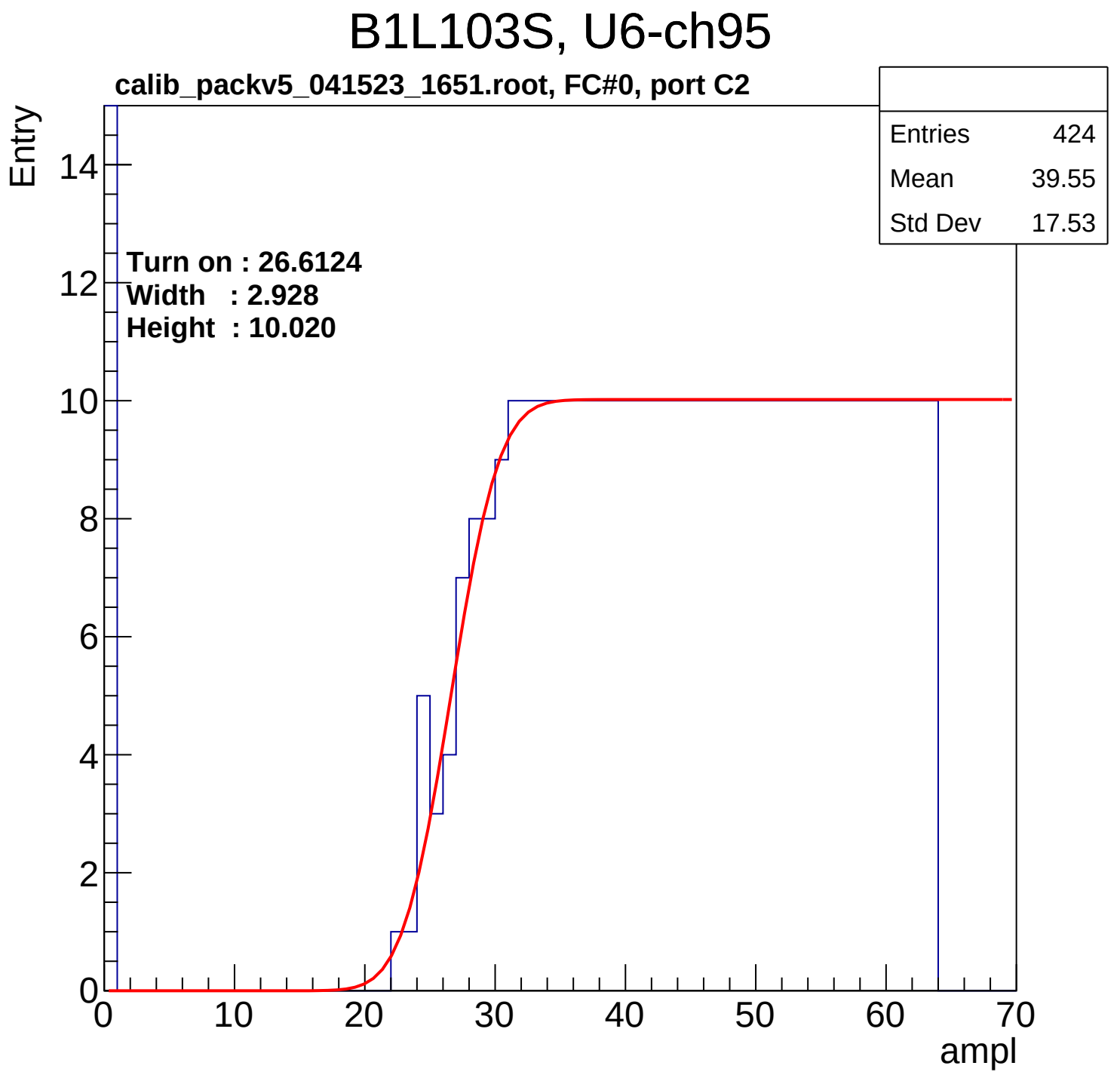

B1L103S, U6-ch90
calib_packv5_041523_1651.root, FC#0, port C2
Entries 438
Mean 39.29
Std Dev 17.11
Turn on : 24.6008
Width : 2.878
Height : 9.971
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

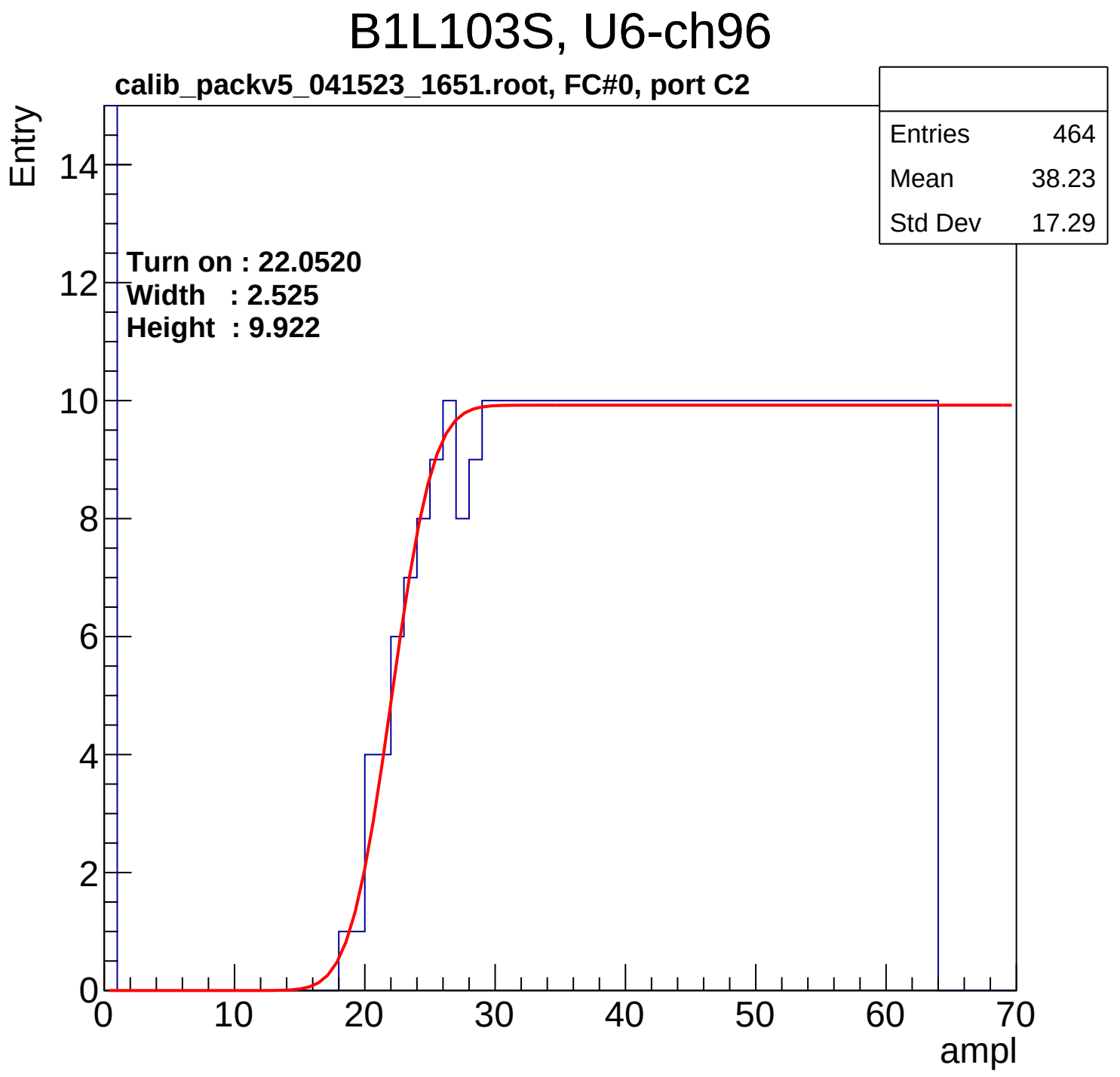

B1L103S, U6-ch91
calib_packv5_041523_1651.root, FC#0, port C2
Entries 412
Mean 40.72
Std Dev 16.36
Turn on : 26.7862
Width : 3.861
Height : 10.067
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

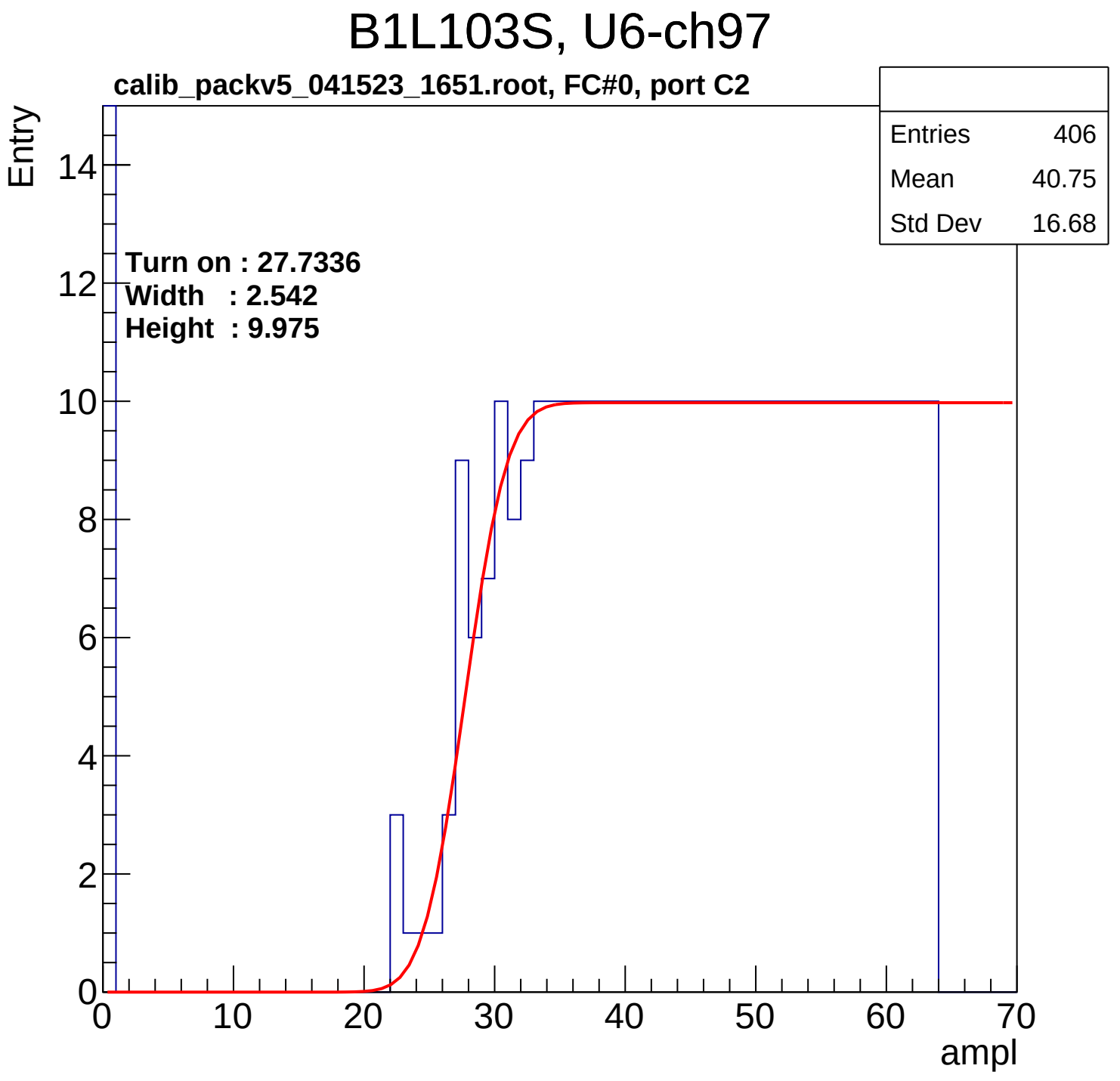

B1L103S, U6-ch92
calib_packv5_041523_1651.root, FC#0, port C2
Entries 461
Mean 38.15
Std Dev 17.59
Turn on : 23.2468
Width : 2.206
Height : 9.947
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

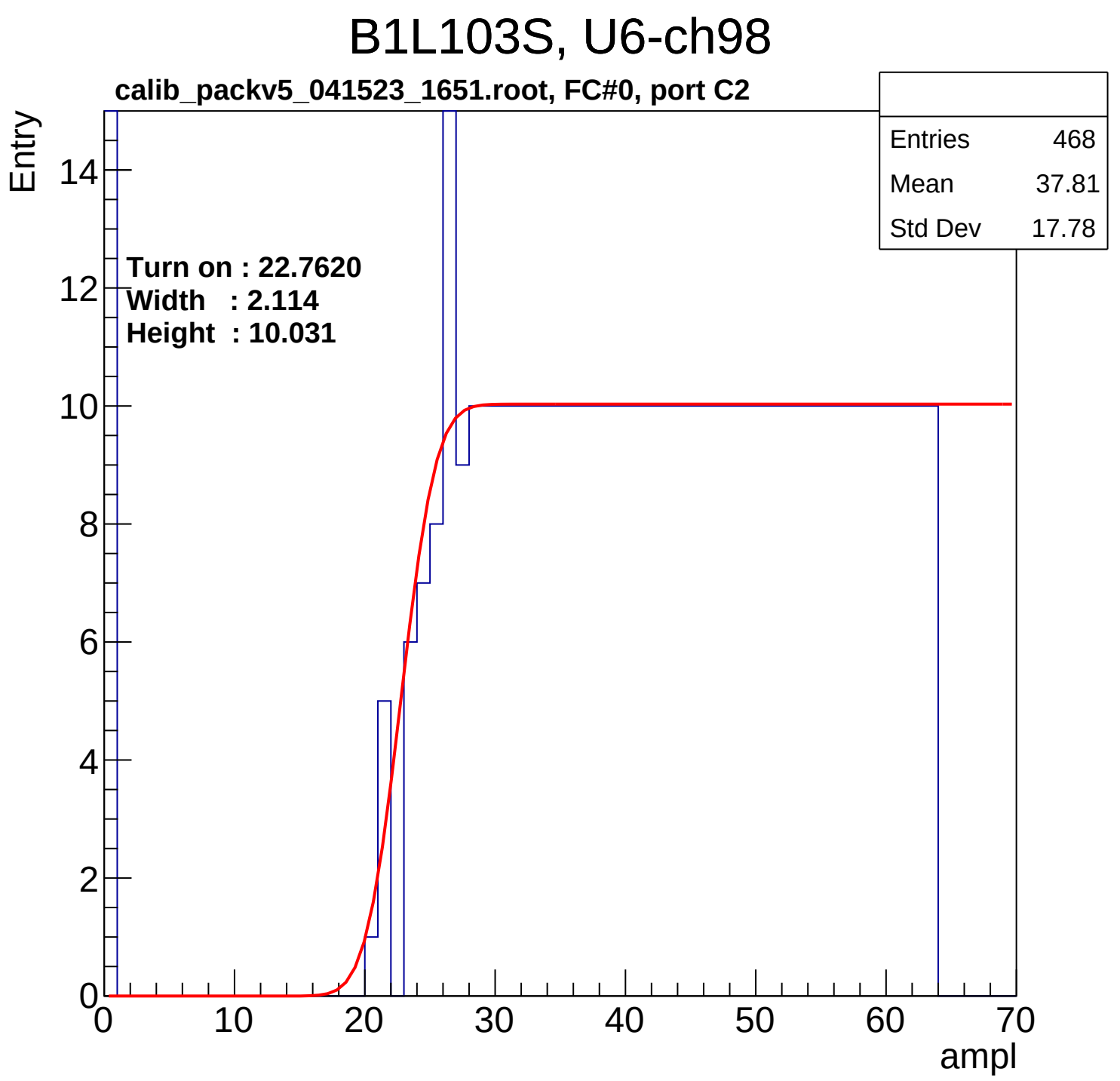

B1L103S, U6-ch93
calib_packv5_041523_1651.root, FC#0, port C2
Entries 432
Mean 39
Std Dev 17.91
Turn on : 26.4289
Width : 3.265
Height : 10.032
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

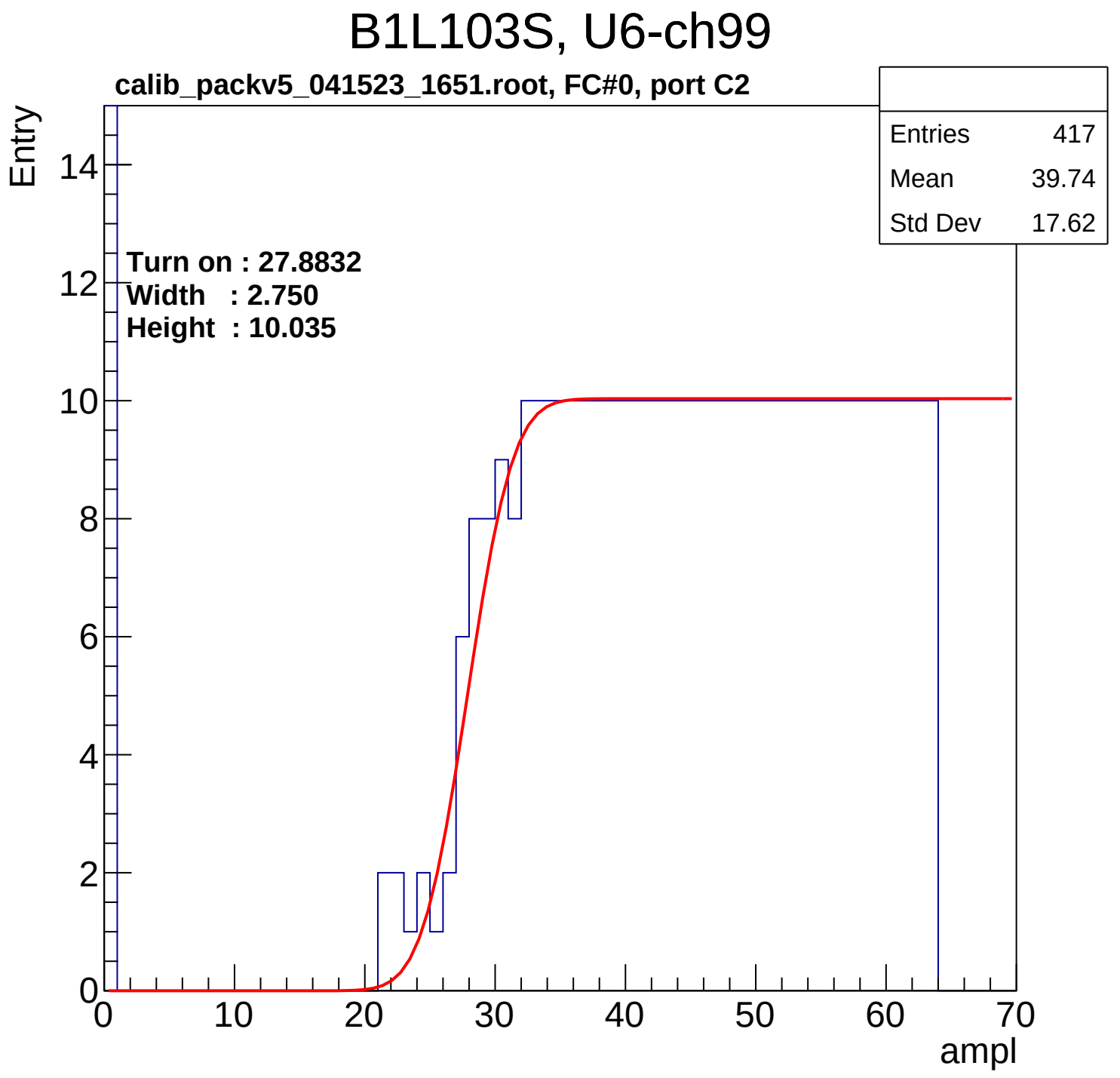

B1L103S, U6-ch94
calib_packv5_041523_1651.root, FC#0, port C2
Entries 432
Mean 39.83
Std Dev 16.6
Turn on : 25.1229
Width : 2.801
Height : 10.008
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

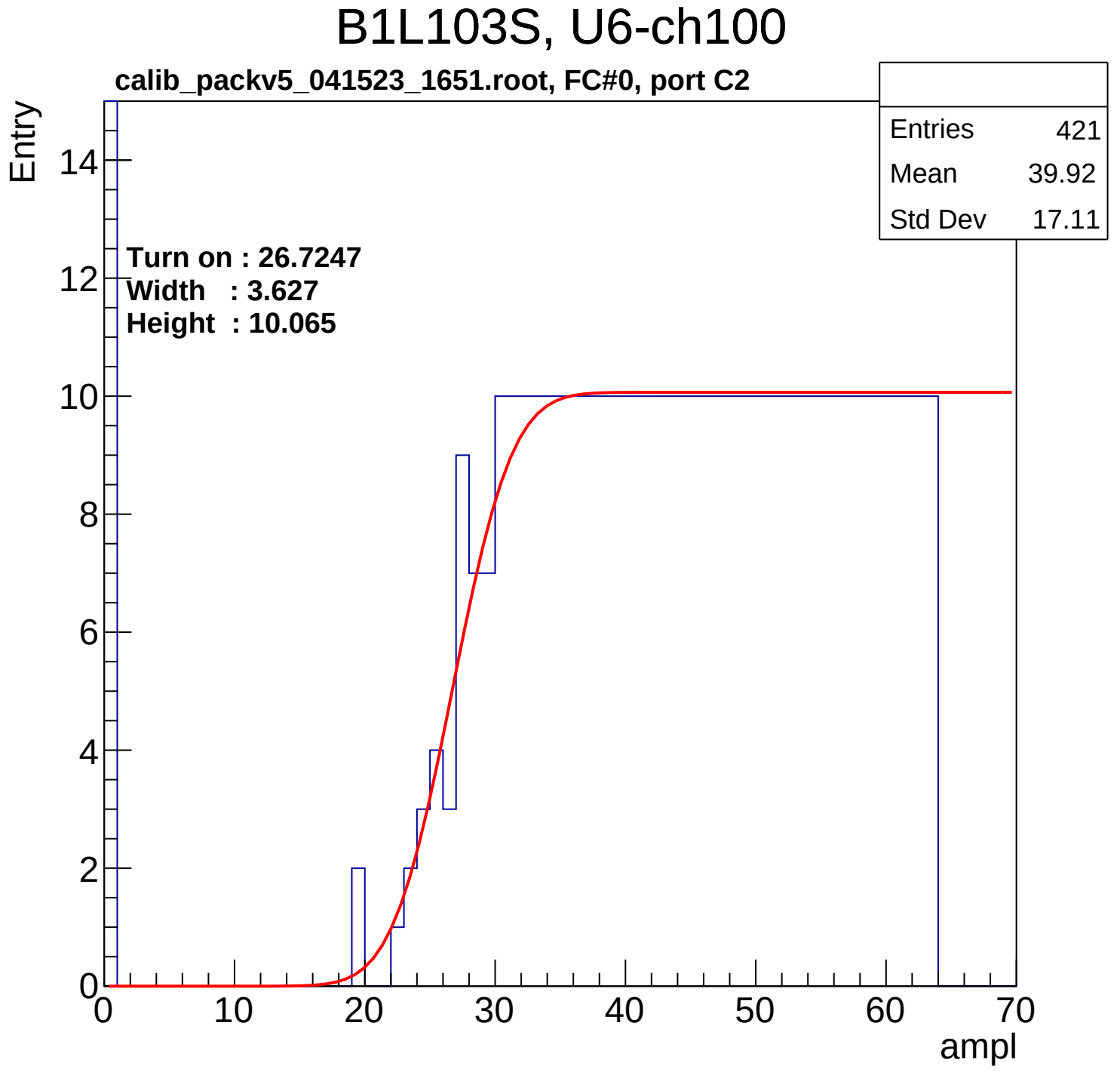

B1L103S, U6-ch95
calib_packv5_041523_1651.root, FC#0, port C2
Entries 424
Mean 39.55
Std Dev 17.53
Turn on : 26.6124
Width : 2.928
Height : 10.020
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

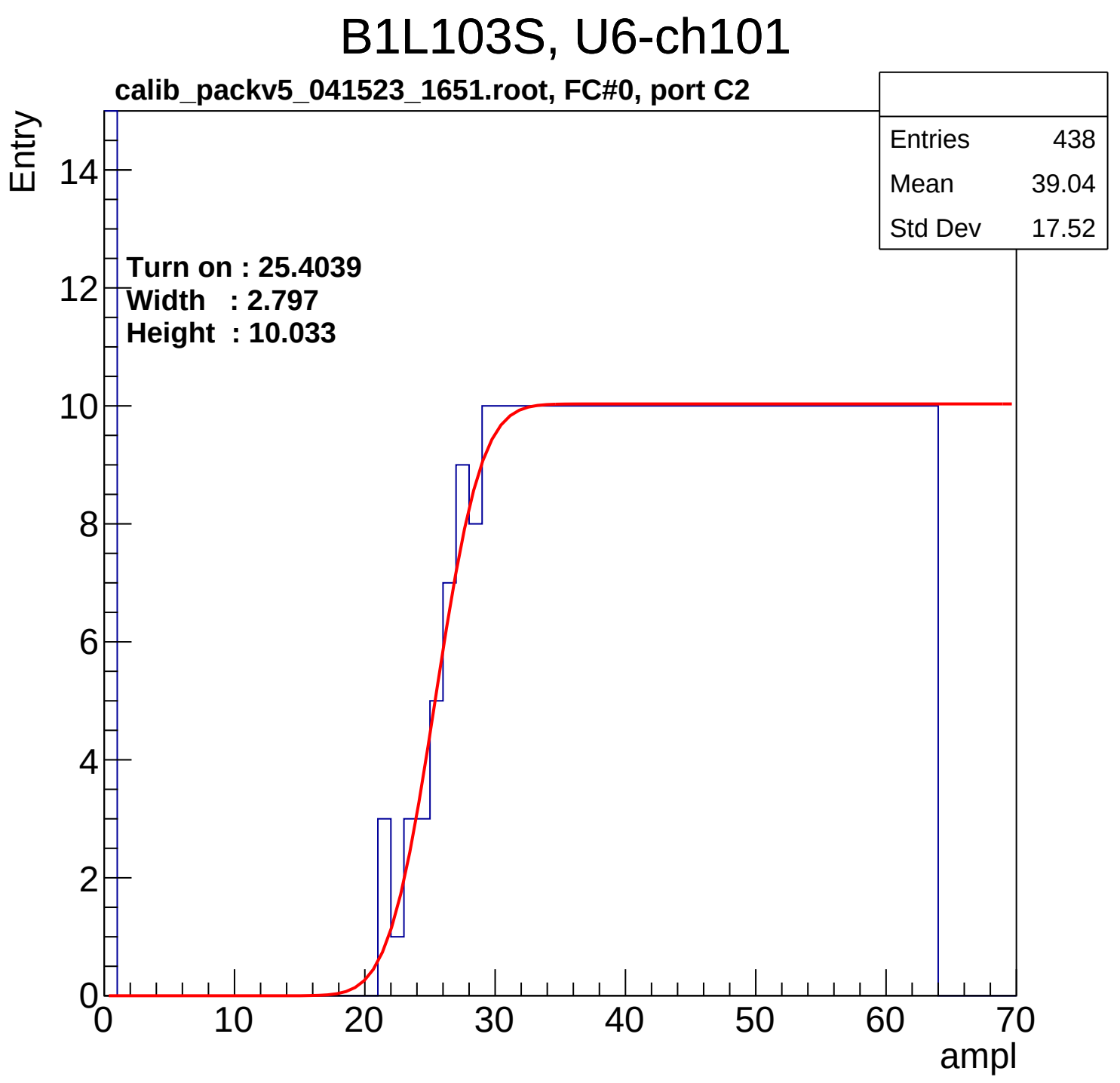

B1L103S, U6-ch96
calib_packv5_041523_1651.root, FC#0, port C2
Entries 464
Mean 38.23
Std Dev 17.29
Turn on : 22.0520
Width : 2.525
Height : 9.922
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

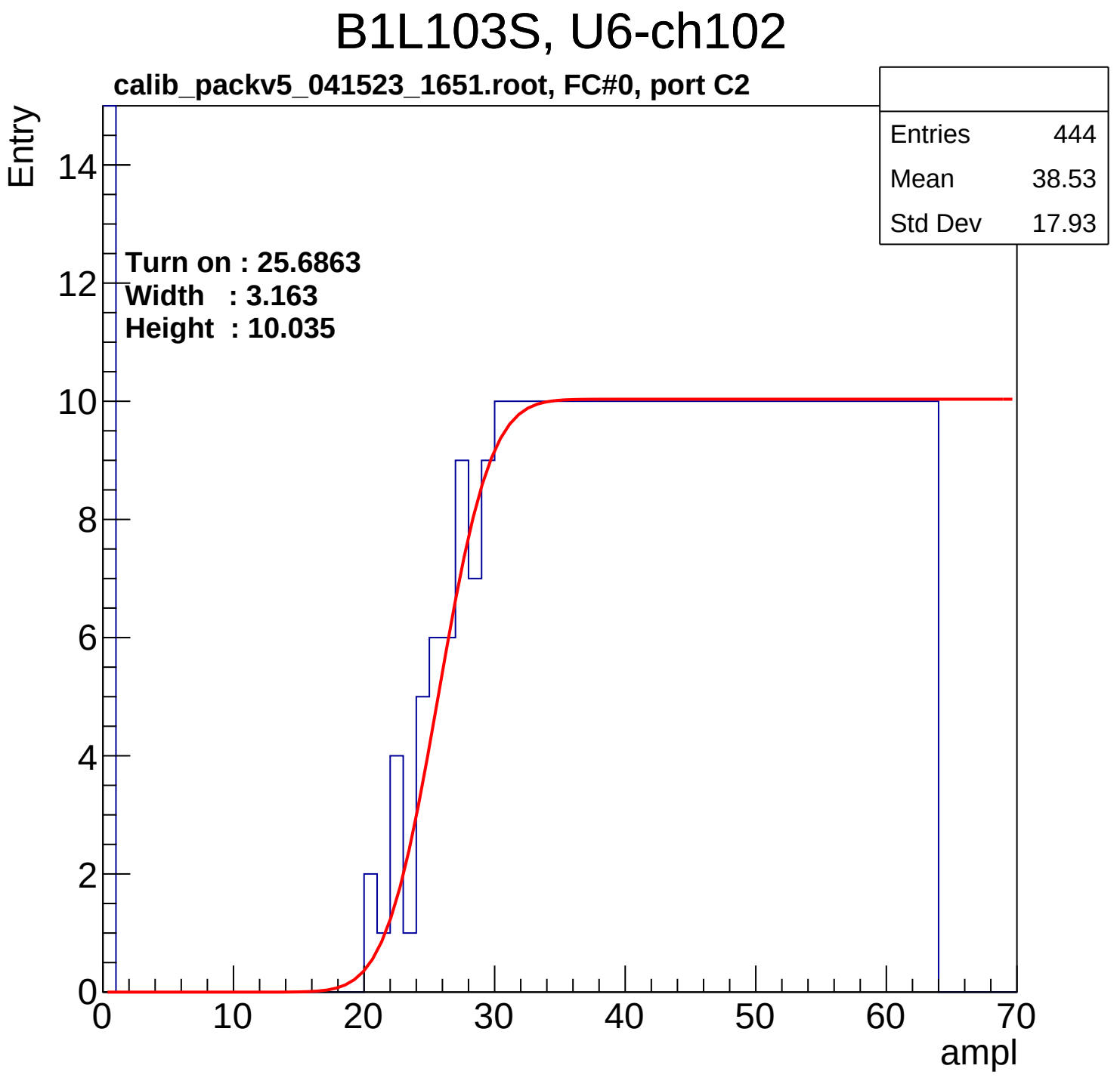

B1L103S, U6-ch97
calib_packv5_041523_1651.root, FC#0, port C2
Entries 406
Mean 40.75
Std Dev 16.68
Turn on : 27.7336
Width : 2.542
Height : 9.975
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

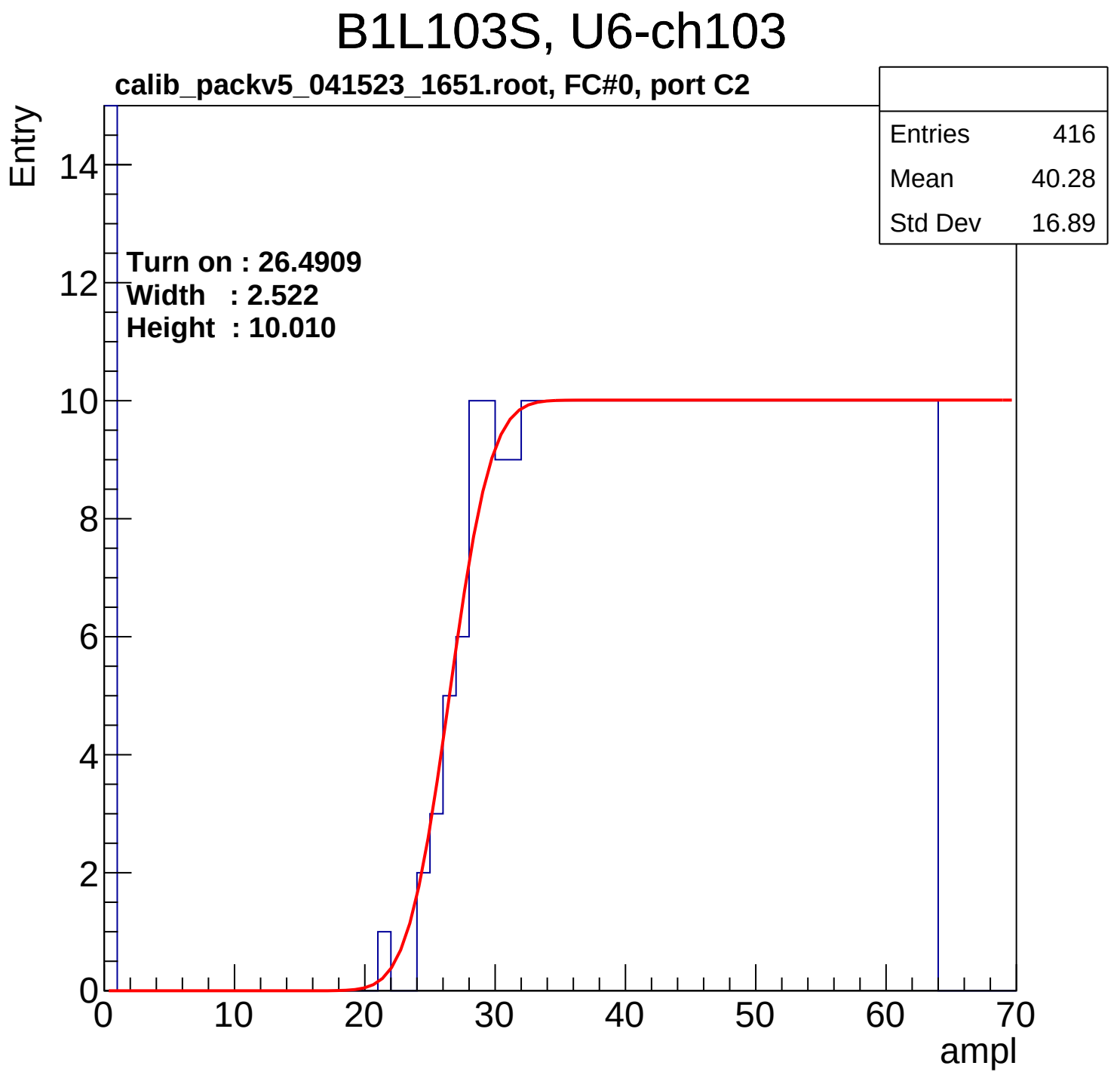

B1L103S, U6-ch98
calib_packv5_041523_1651.root, FC#0, port C2
Entries 468
Mean 37.81
Std Dev 17.78
Turn on : 22.7620
Width : 2.114
Height : 10.031
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

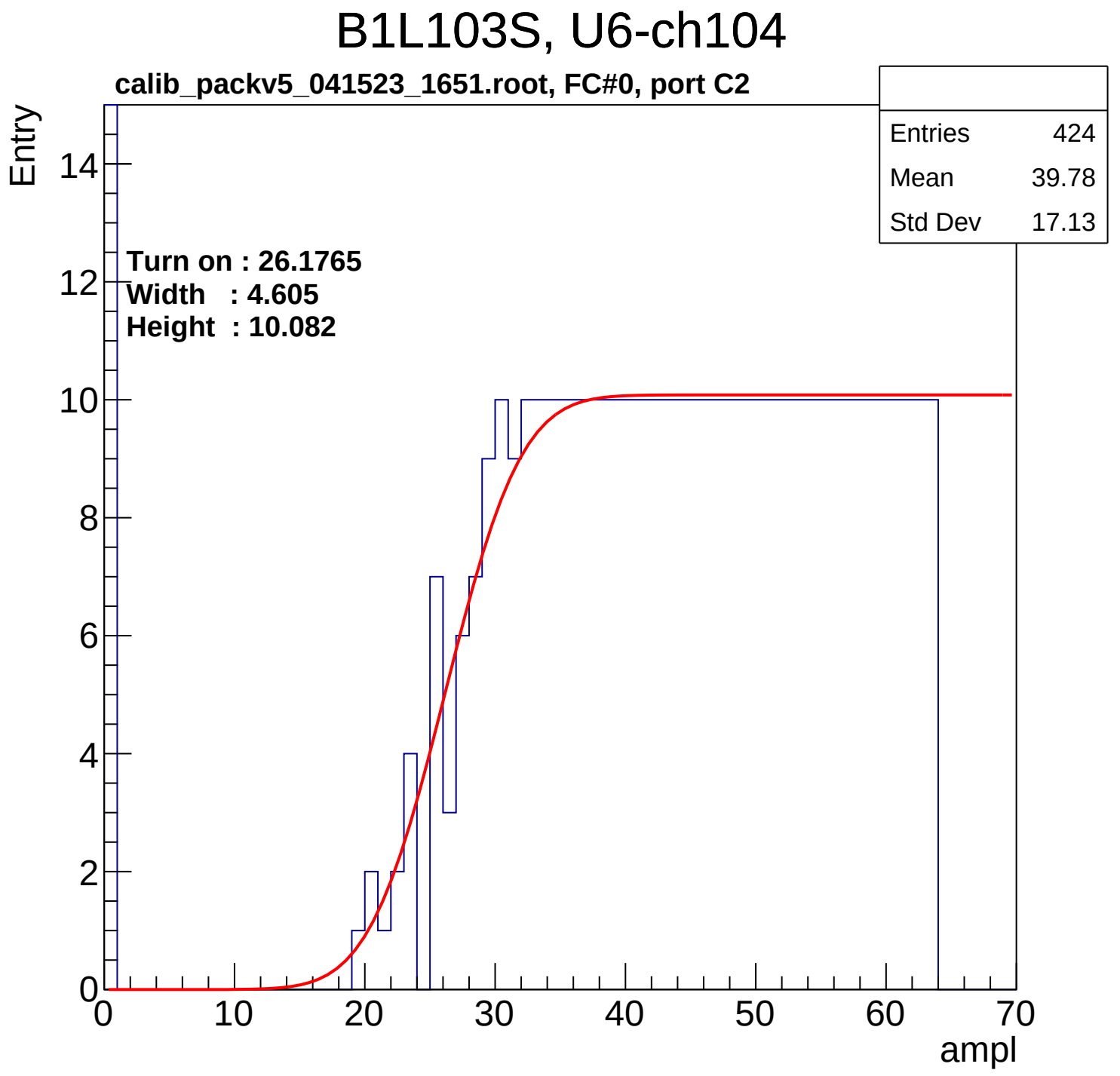

B1L103S, U6-ch99
calib_packv5_041523_1651.root, FC#0, port C2
Entries 417
Mean 39.74
Std Dev 17.62
Turn on : 27.8832
Width : 2.750
Height : 10.035
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

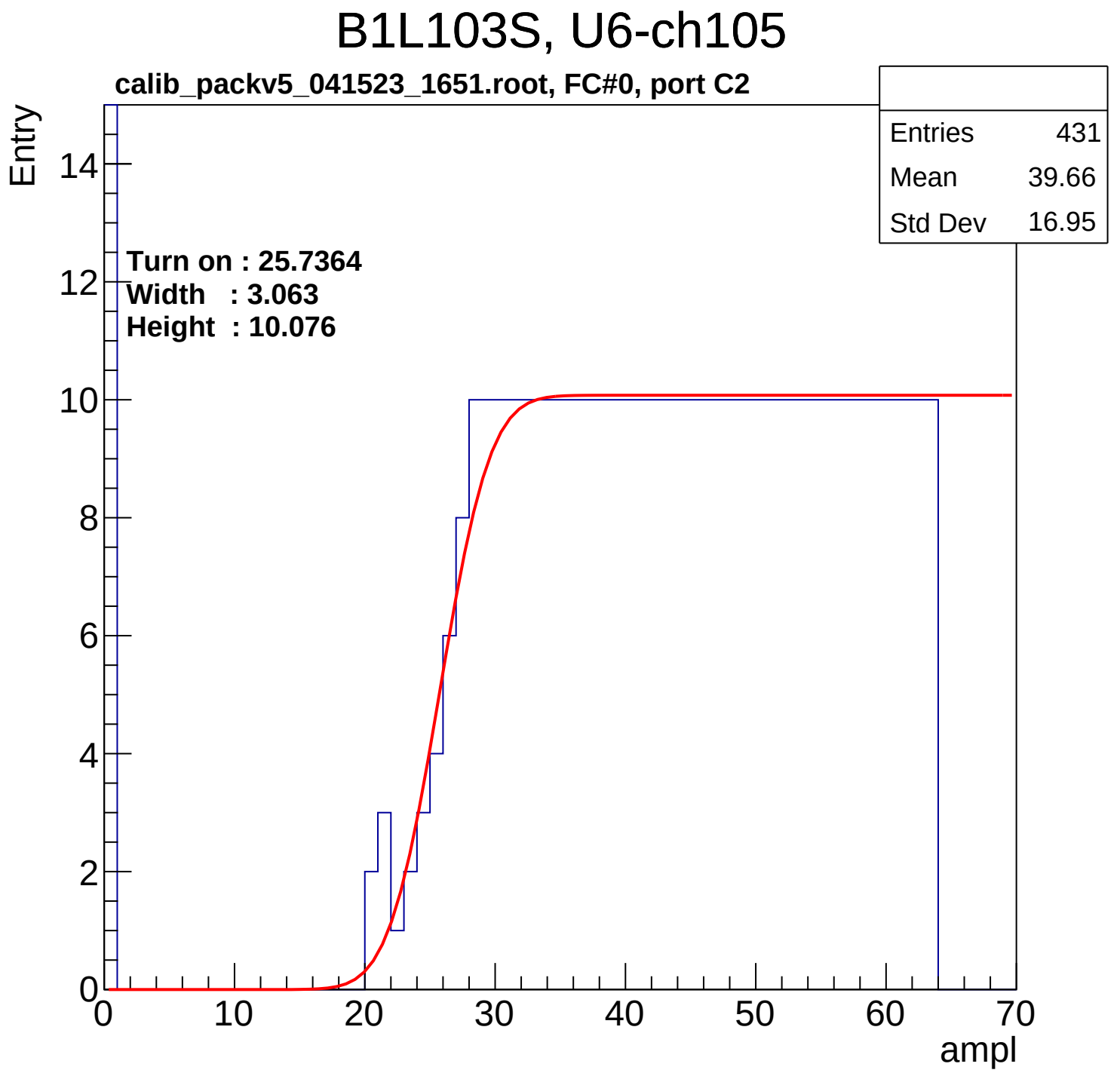

B1L103S, U6-ch100
calib_packv5_041523_1651.root, FC#0, port C2
Entries 421
Mean 39.92
Std Dev 17.11
Turn on : 26.7247
Width : 3.627
Height : 10.065
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

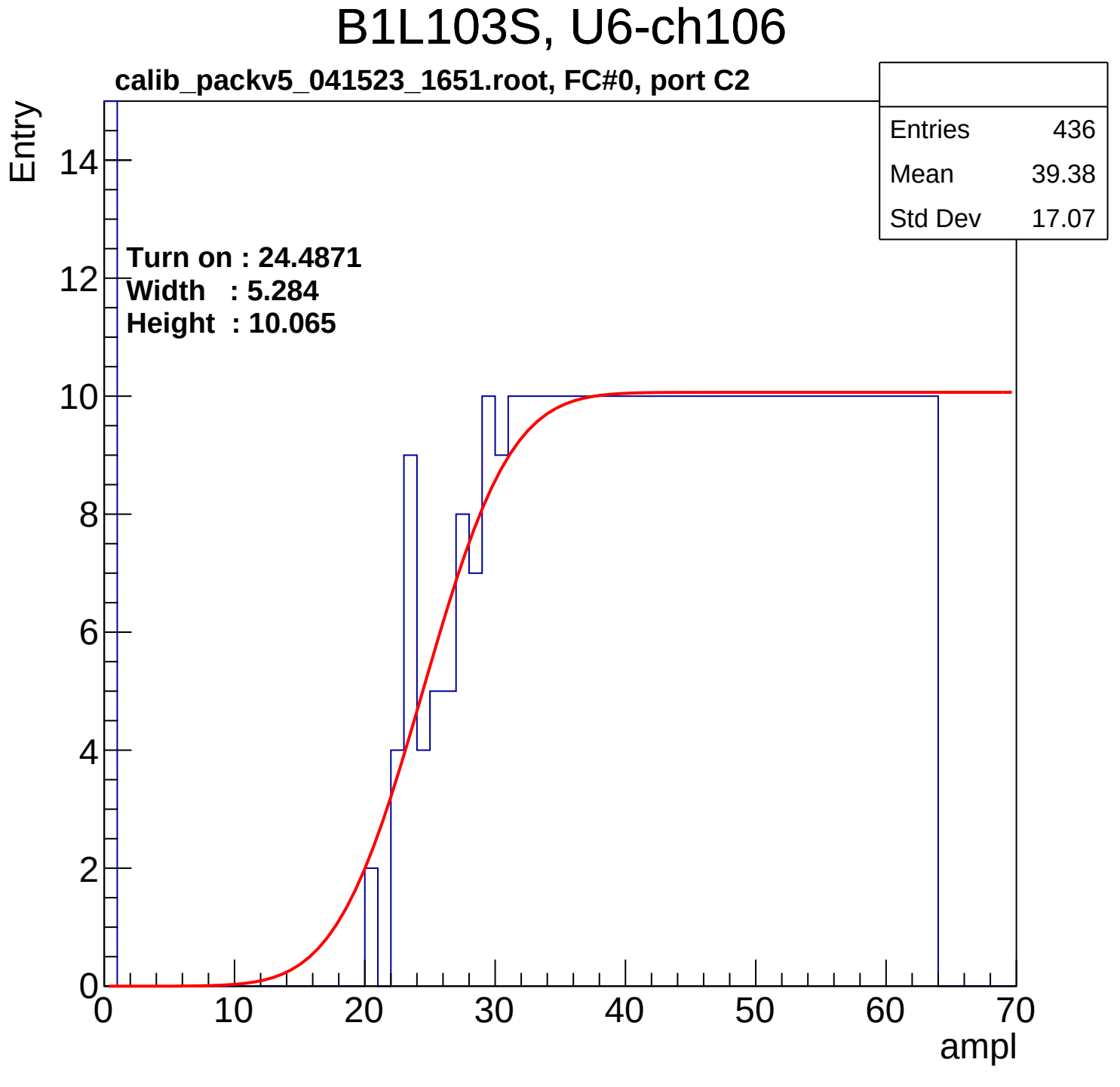

B1L103S, U6-ch101
calib_packv5_041523_1651.root, FC#0, port C2
Entries 438
Mean 39.04
Std Dev 17.52
Turn on : 25.4039
Width : 2.797
Height : 10.033
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

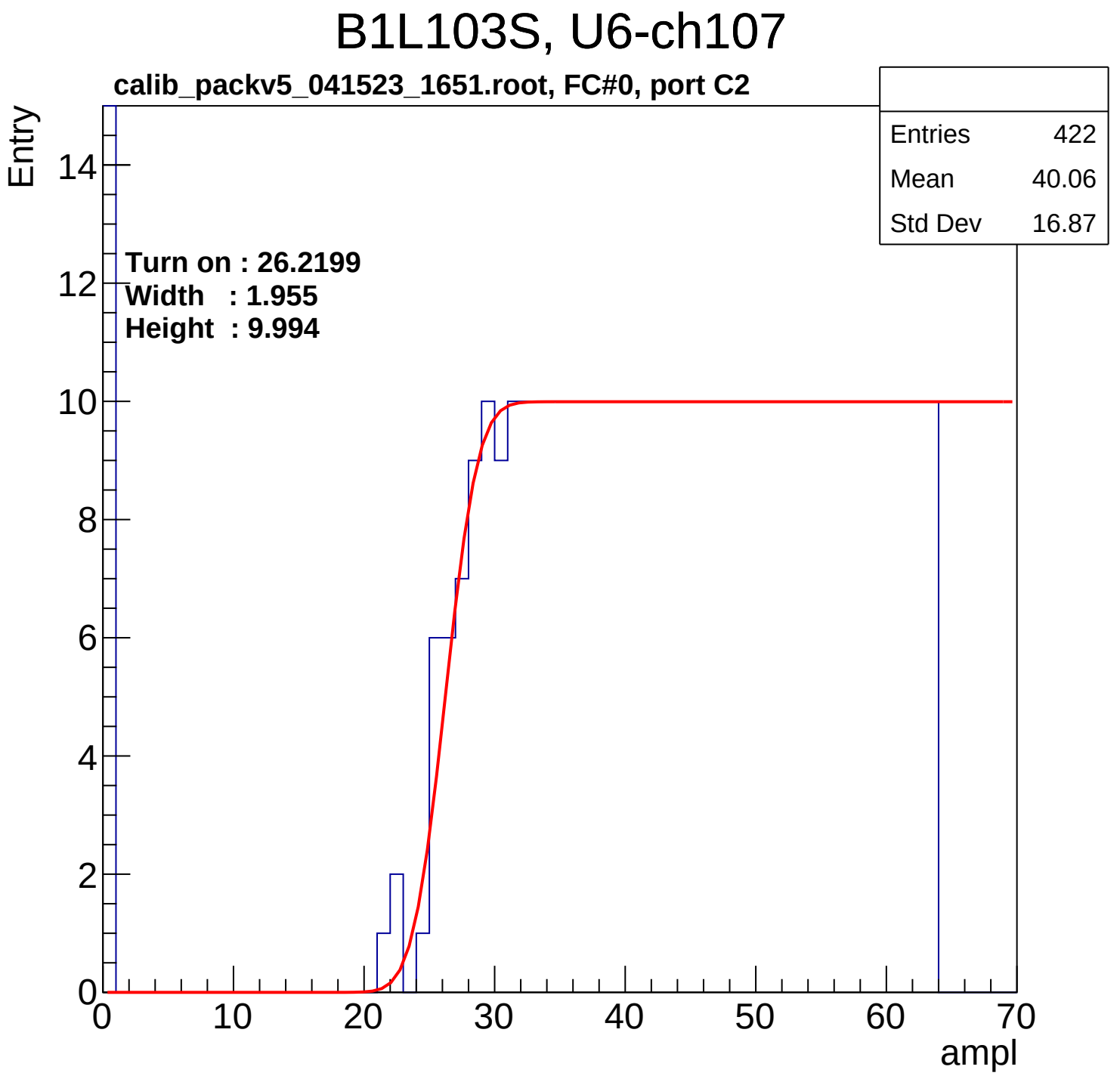

B1L103S, U6-ch102
calib_packv5_041523_1651.root, FC#0, port C2
Entries 444
Mean 38.53
Std Dev 17.93
Turn on : 25.6863
Width : 3.163
Height : 10.035
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

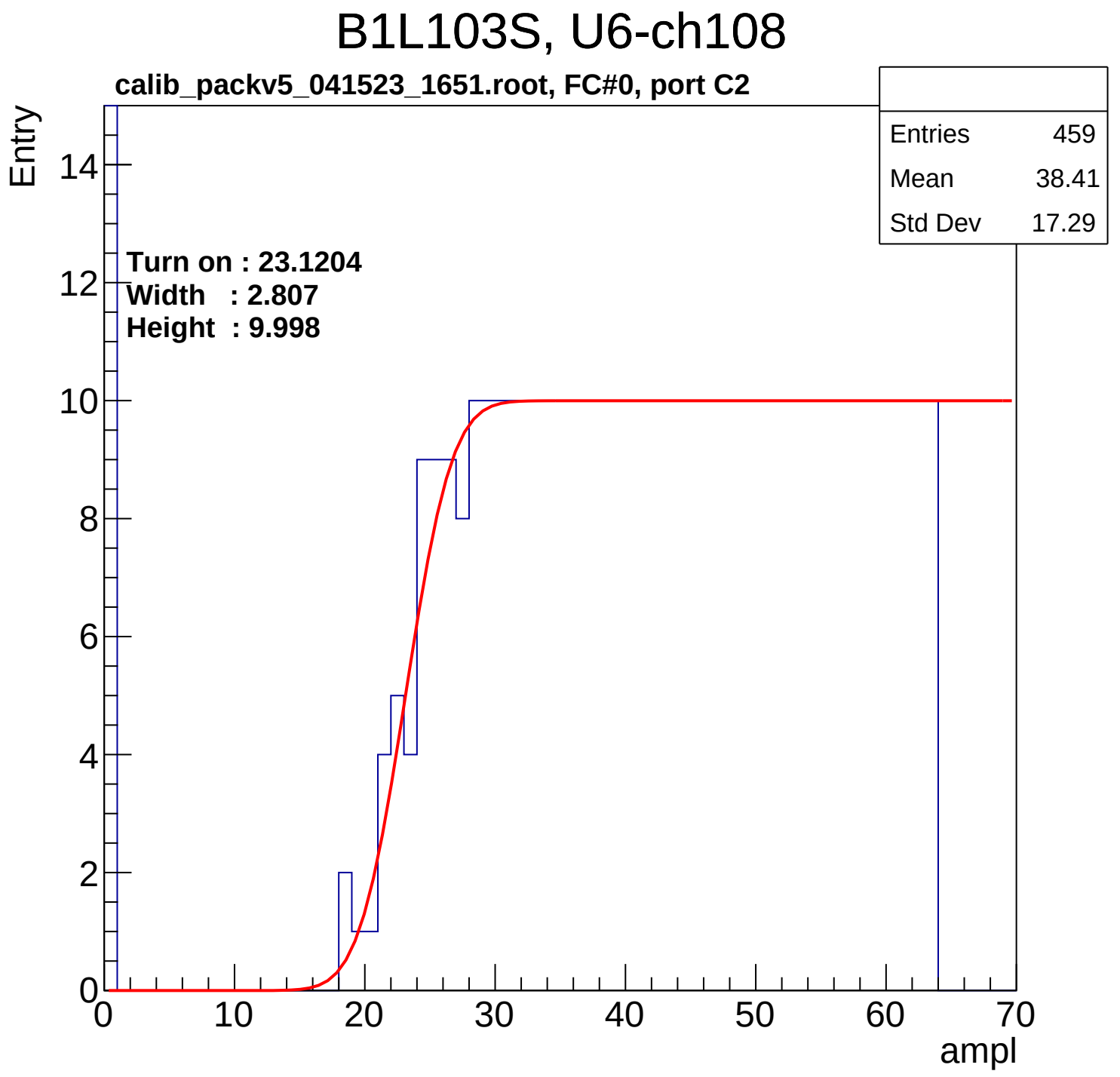

B1L103S, U6-ch103
calib_packv5_041523_1651.root, FC#0, port C2
Entries 416
Mean 40.28
Std Dev 16.89
Turn on : 26.4909
Width : 2.522
Height : 10.010
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

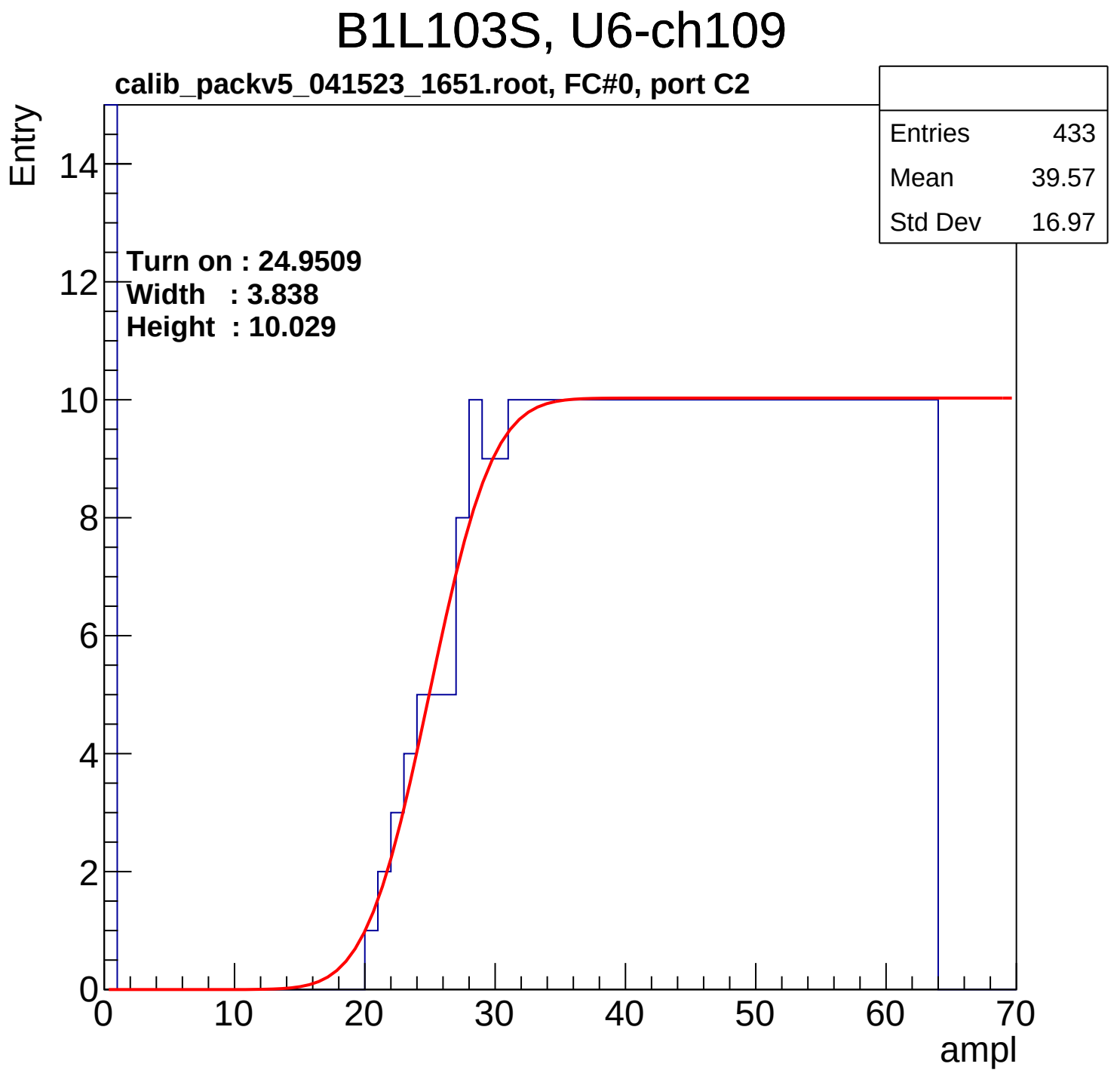

B1L103S, U6-ch104
calib_packv5_041523_1651.root, FC#0, port C2
Entries 424
Mean 39.78
Std Dev 17.13
Turn on : 26.1765
Width : 4.605
Height : 10.082
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

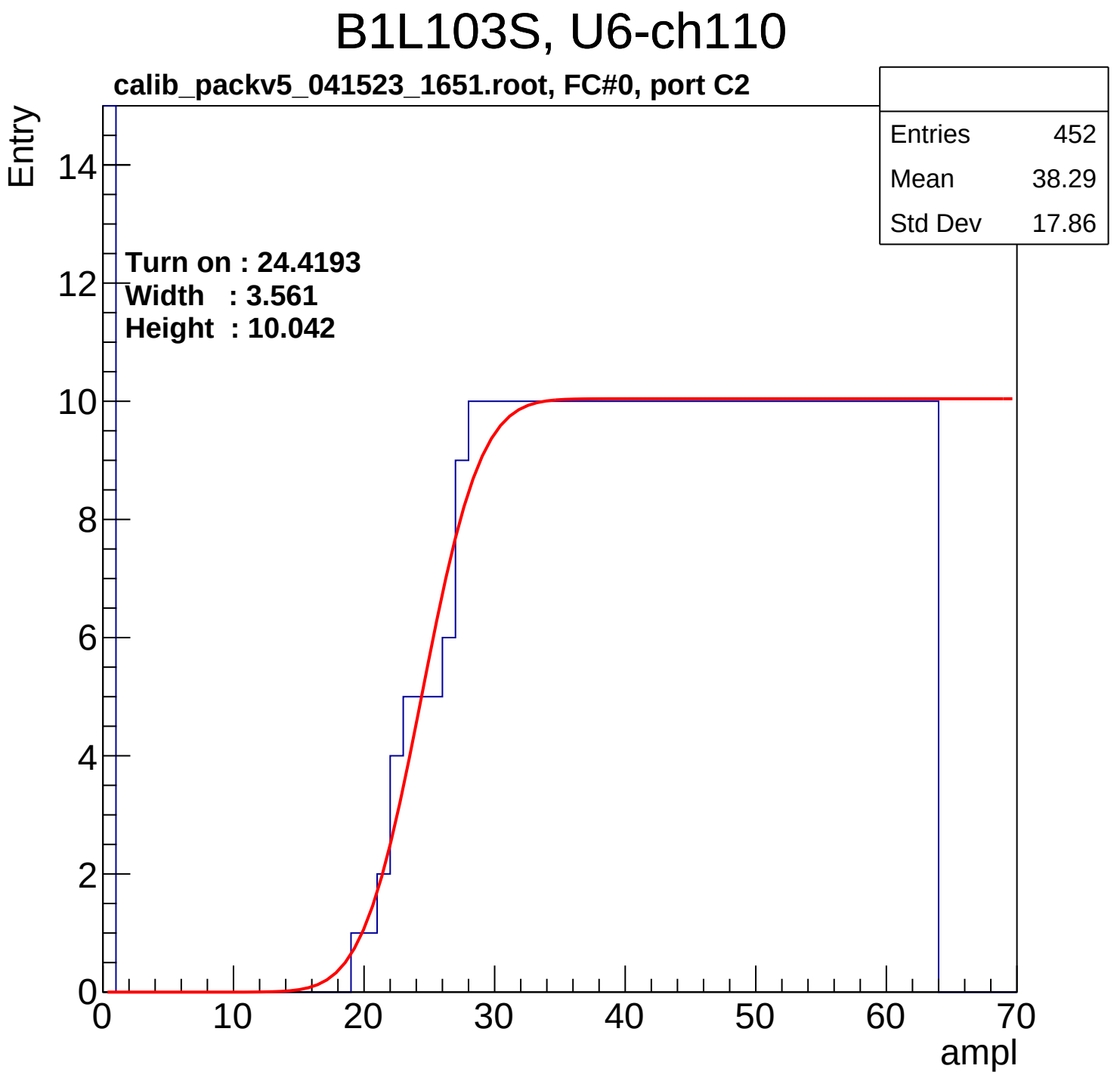

B1L103S, U6-ch105
calib_packv5_041523_1651.root, FC#0, port C2
Entries 431
Mean 39.66
Std Dev 16.95
Turn on : 25.7364
Width : 3.063
Height : 10.076
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

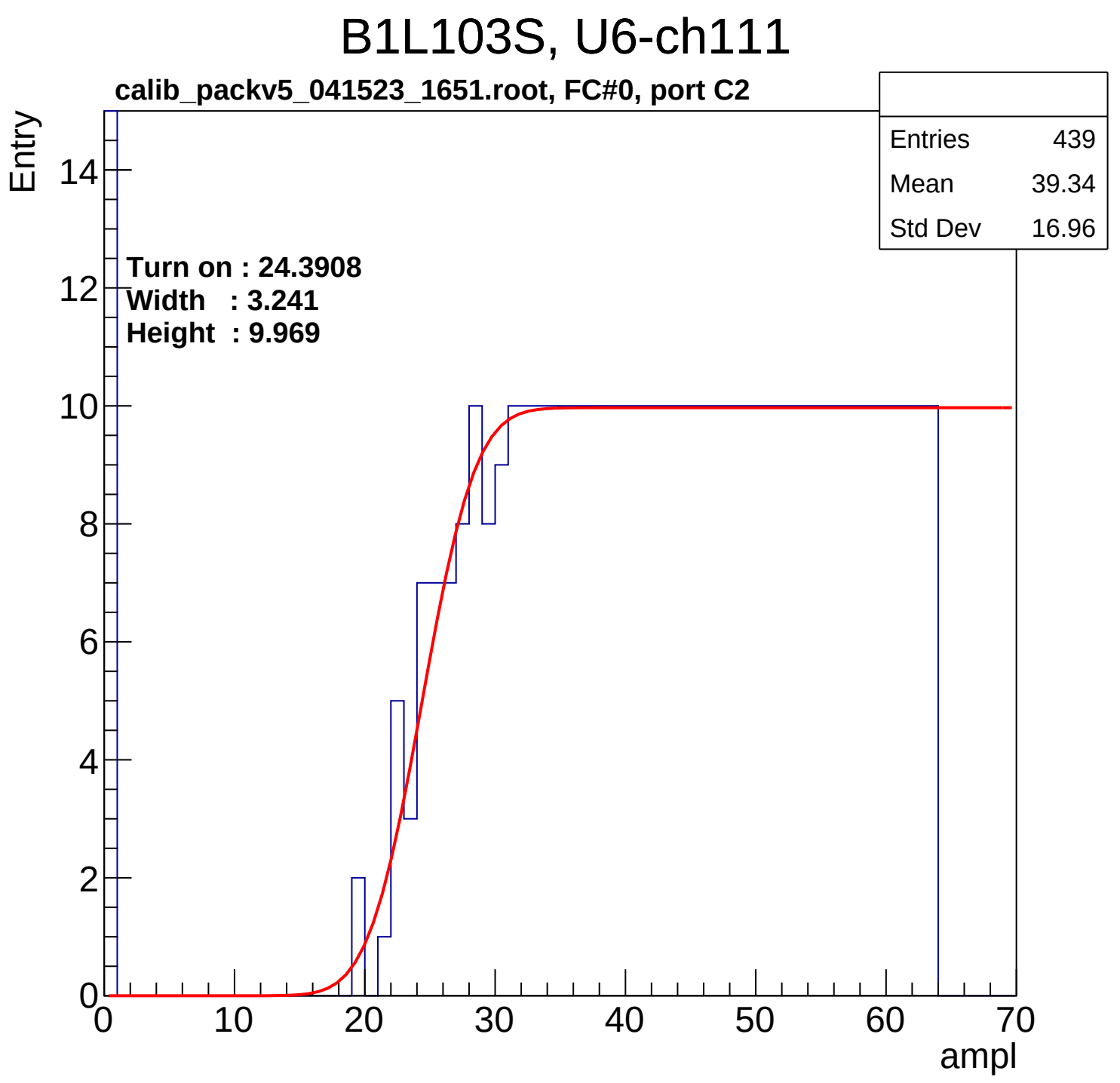

B1L103S, U6-ch106
calib_packv5_041523_1651.root, FC#0, port C2
Entries 436
Mean 39.38
Std Dev 17.07
Turn on : 24.4871
Width : 5.284
Height : 10.065
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

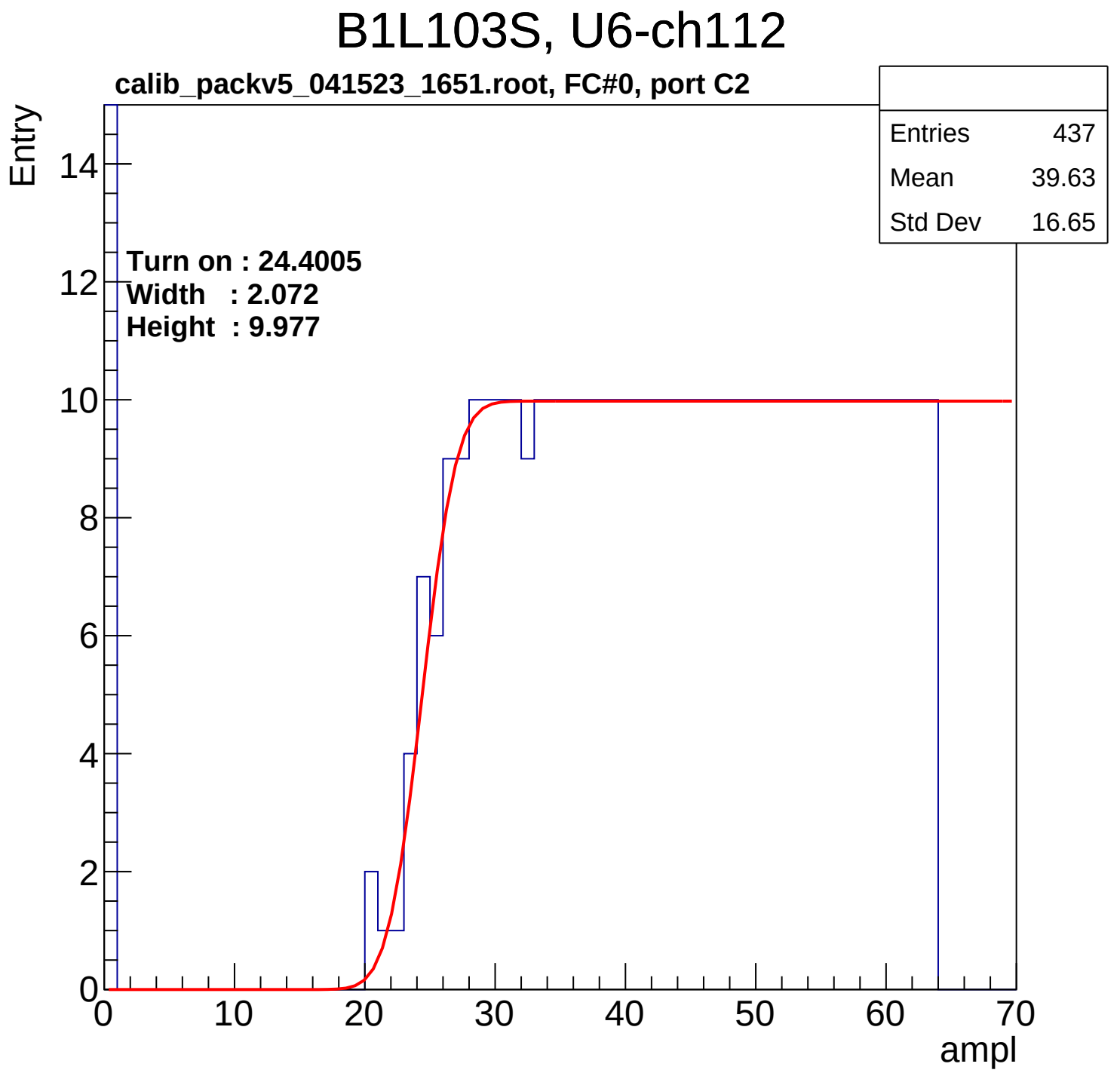

B1L103S, U6-ch107
calib_packv5_041523_1651.root, FC#0, port C2
Entries 422
Mean 40.06
Std Dev 16.87
Turn on : 26.2199
Width : 1.955
Height : 9.994
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

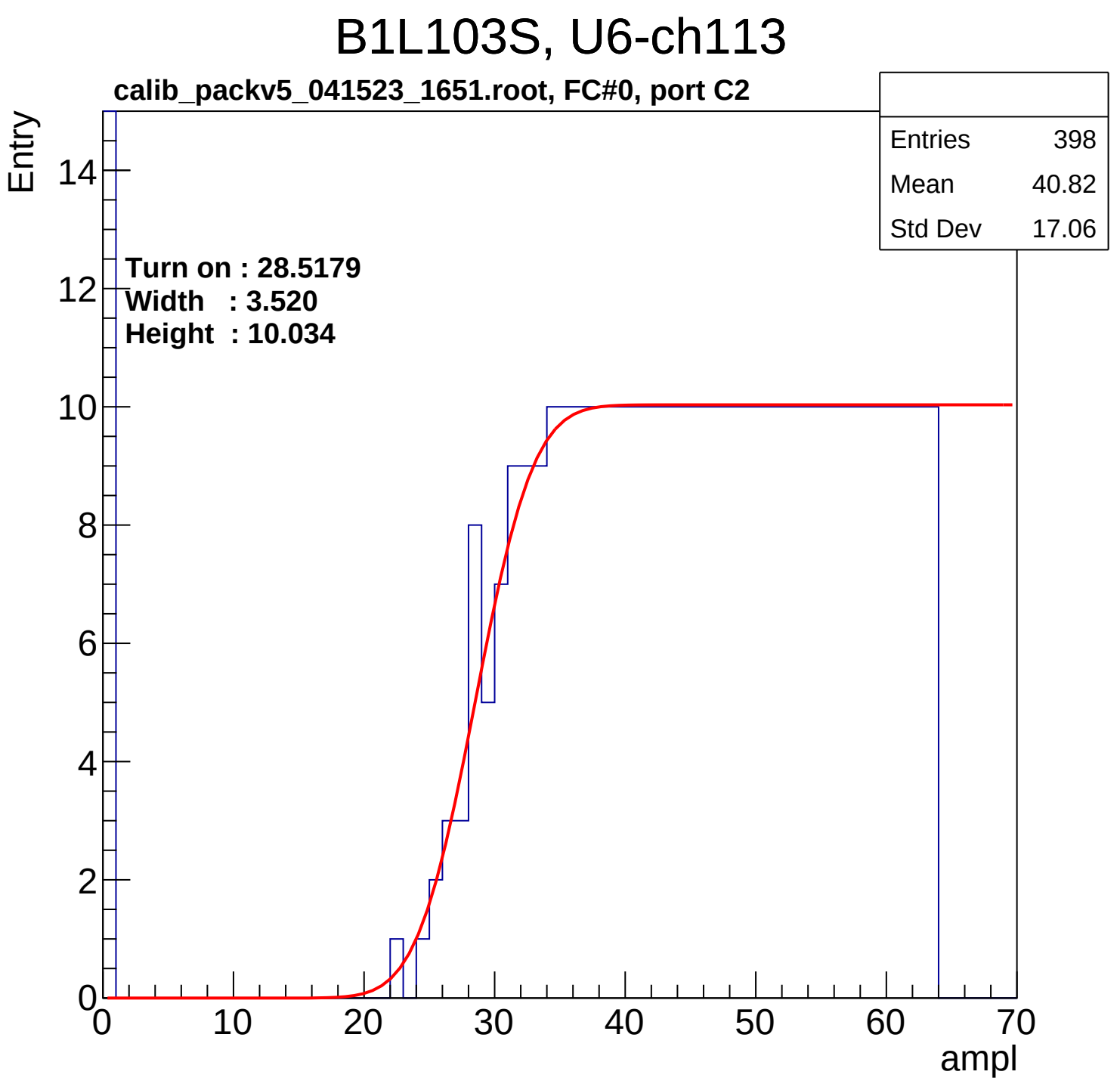

B1L103S, U6-ch108
calib_packv5_041523_1651.root, FC#0, port C2
Entries 459
Mean 38.41
Std Dev 17.29
Turn on : 23.1204
Width : 2.807
Height : 9.998
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

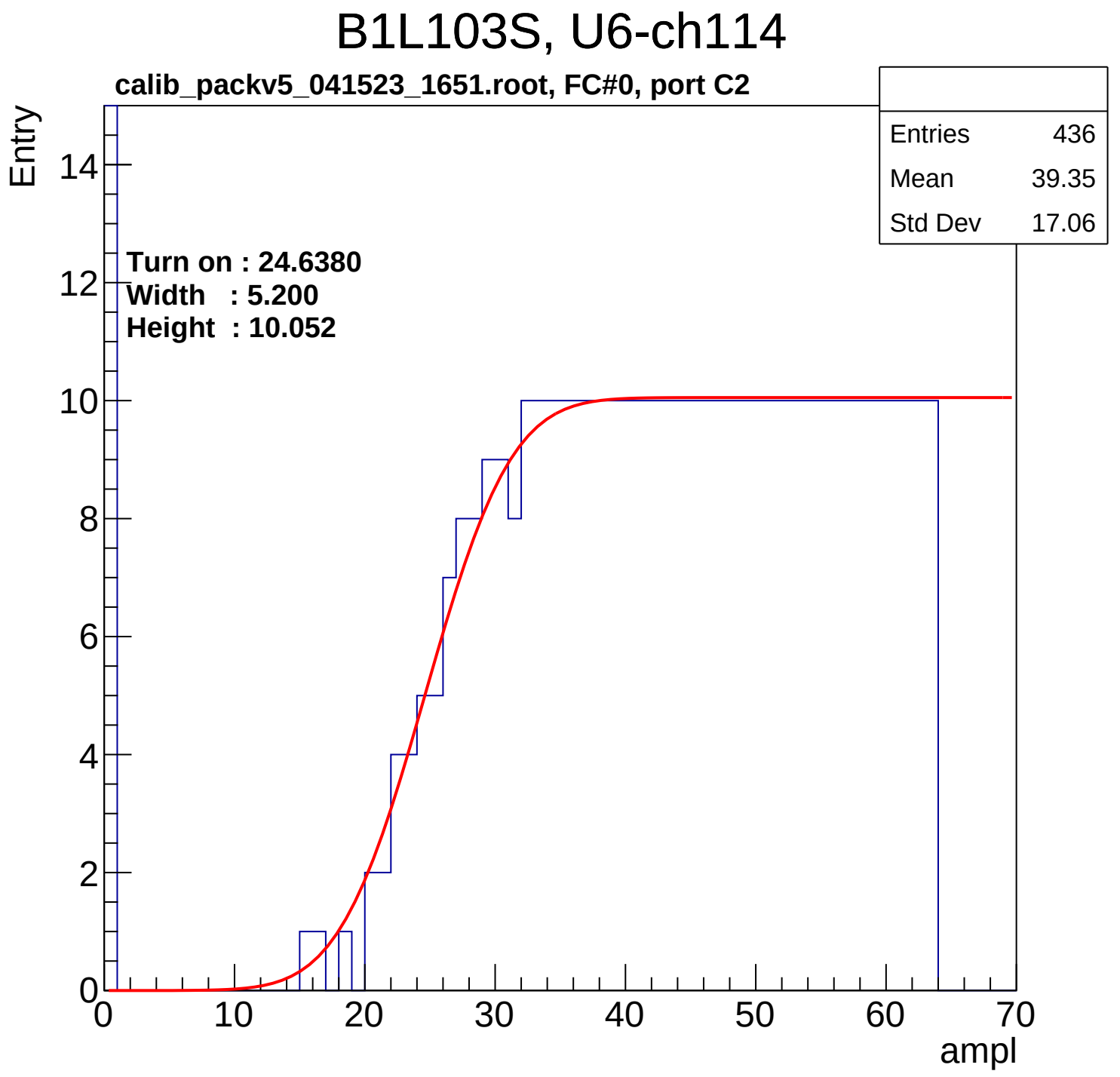

B1L103S, U6-ch109
calib_packv5_041523_1651.root, FC#0, port C2
Entries 433
Mean 39.57
Std Dev 16.97
Turn on : 24.9509
Width : 3.838
Height : 10.029
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

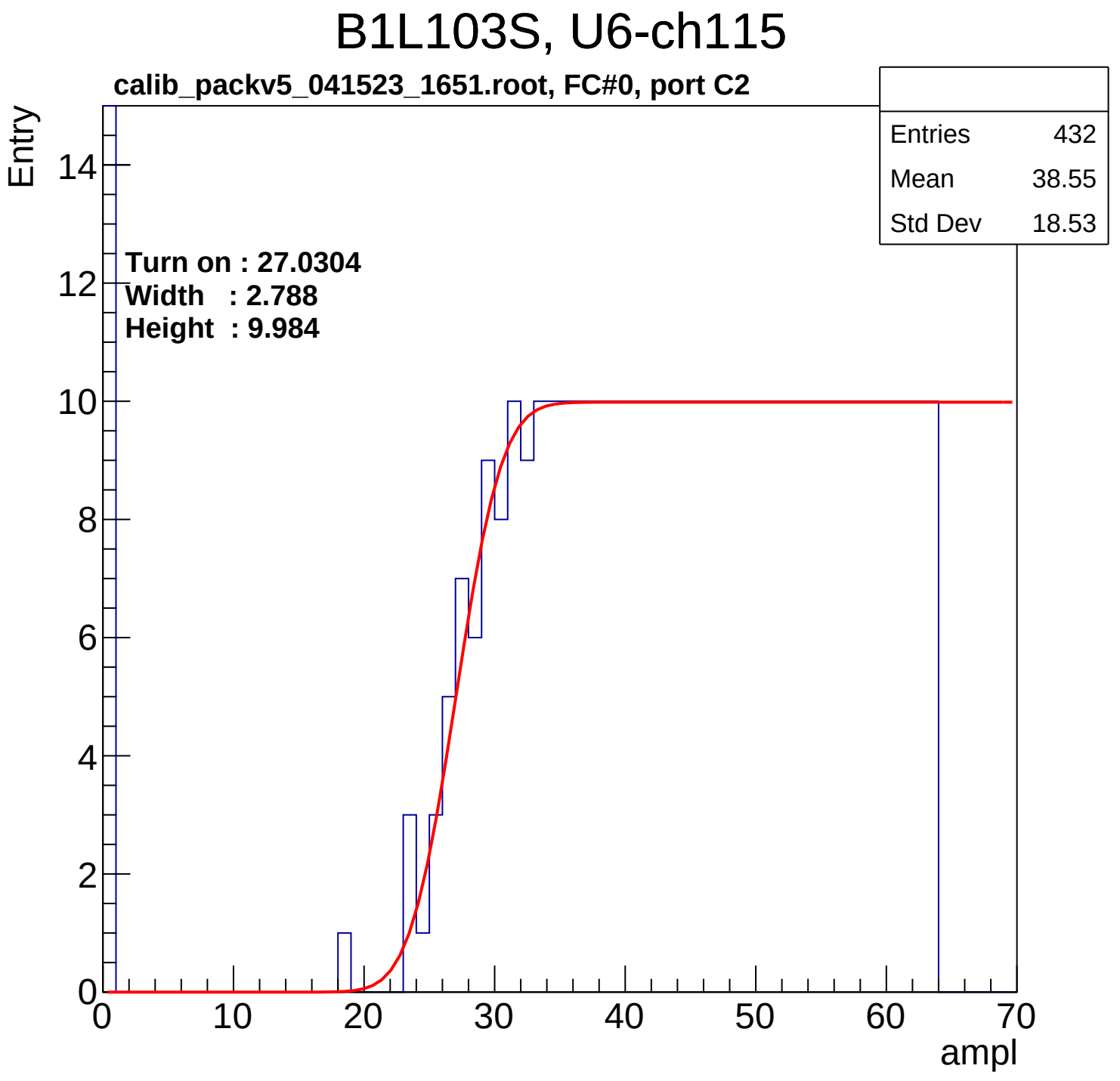

B1L103S, U6-ch110
calib_packv5_041523_1651.root, FC#0, port C2
Entries 452
Mean 38.29
Std Dev 17.86
Turn on : 24.4193
Width : 3.561
Height : 10.042
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

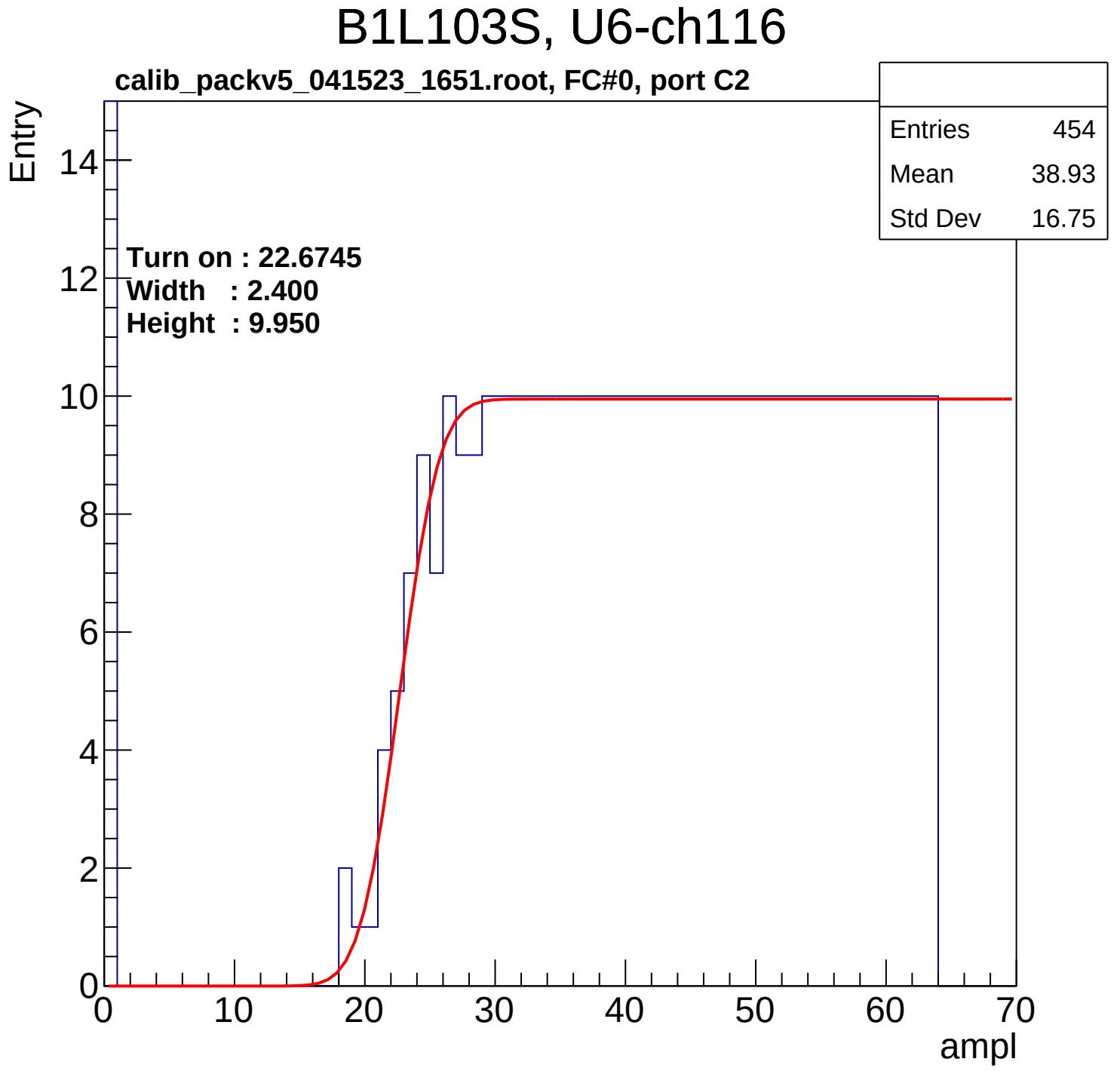

B1L103S, U6-ch111
calib_packv5_041523_1651.root, FC#0, port C2
Entries 439
Mean 39.34
Std Dev 16.96
Turn on : 24.3908
Width : 3.241
Height : 9.969
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

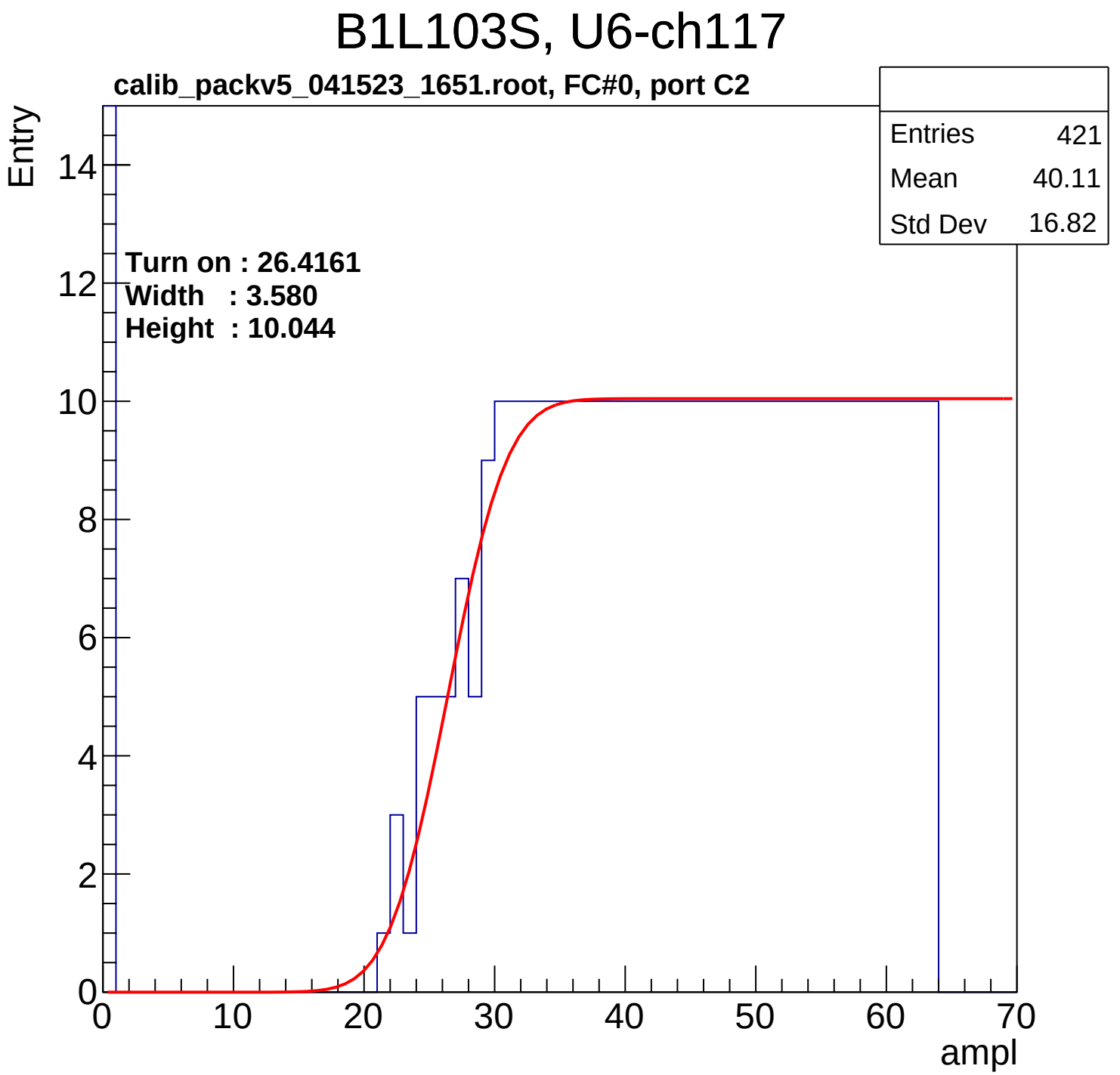

B1L103S, U6-ch112
calib_packv5_041523_1651.root, FC#0, port C2
Entries 437
Mean 39.63
Std Dev 16.65
Turn on : 24.4005
Width : 2.072
Height : 9.977
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

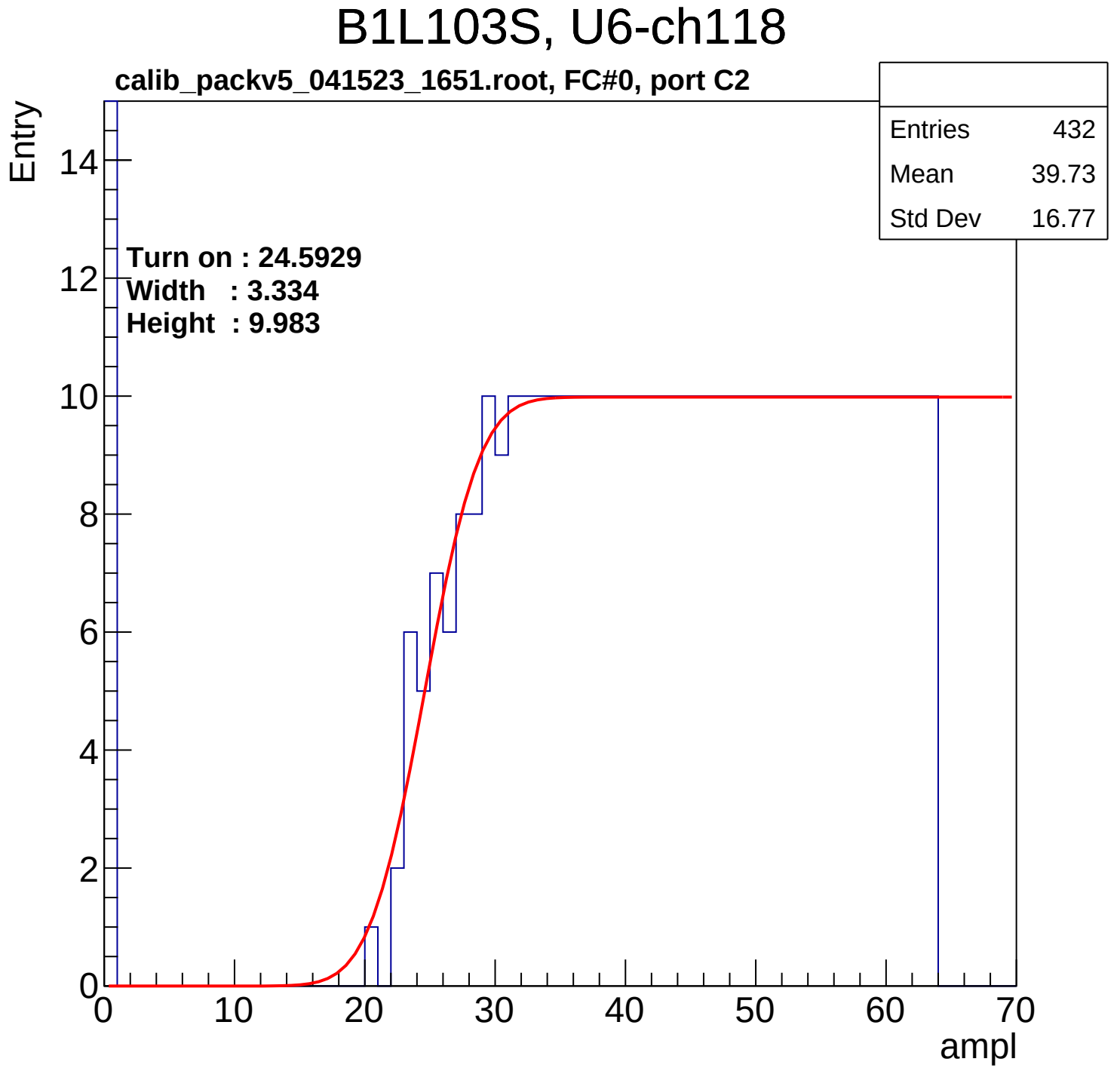

B1L103S, U6-ch113
calib_packv5_041523_1651.root, FC#0, port C2
Entries 398
Mean 40.82
Std Dev 17.06
Turn on : 28.5179
Width : 3.520
Height : 10.034
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

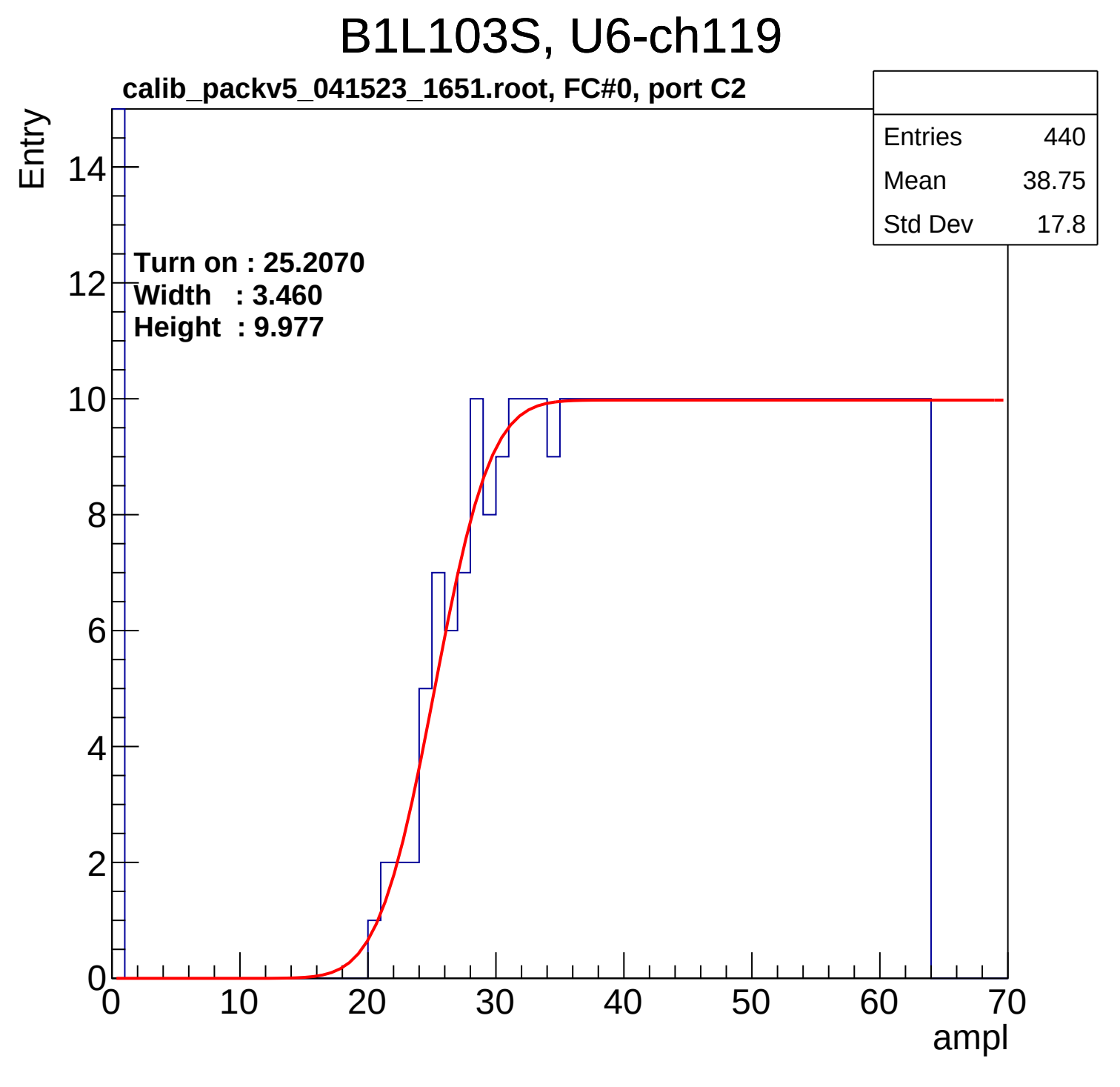

B1L103S, U6-ch114
calib_packv5_041523_1651.root, FC#0, port C2
Entries 436
Mean 39.35
Std Dev 17.06
Turn on : 24.6380
Width : 5.200
Height : 10.052
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

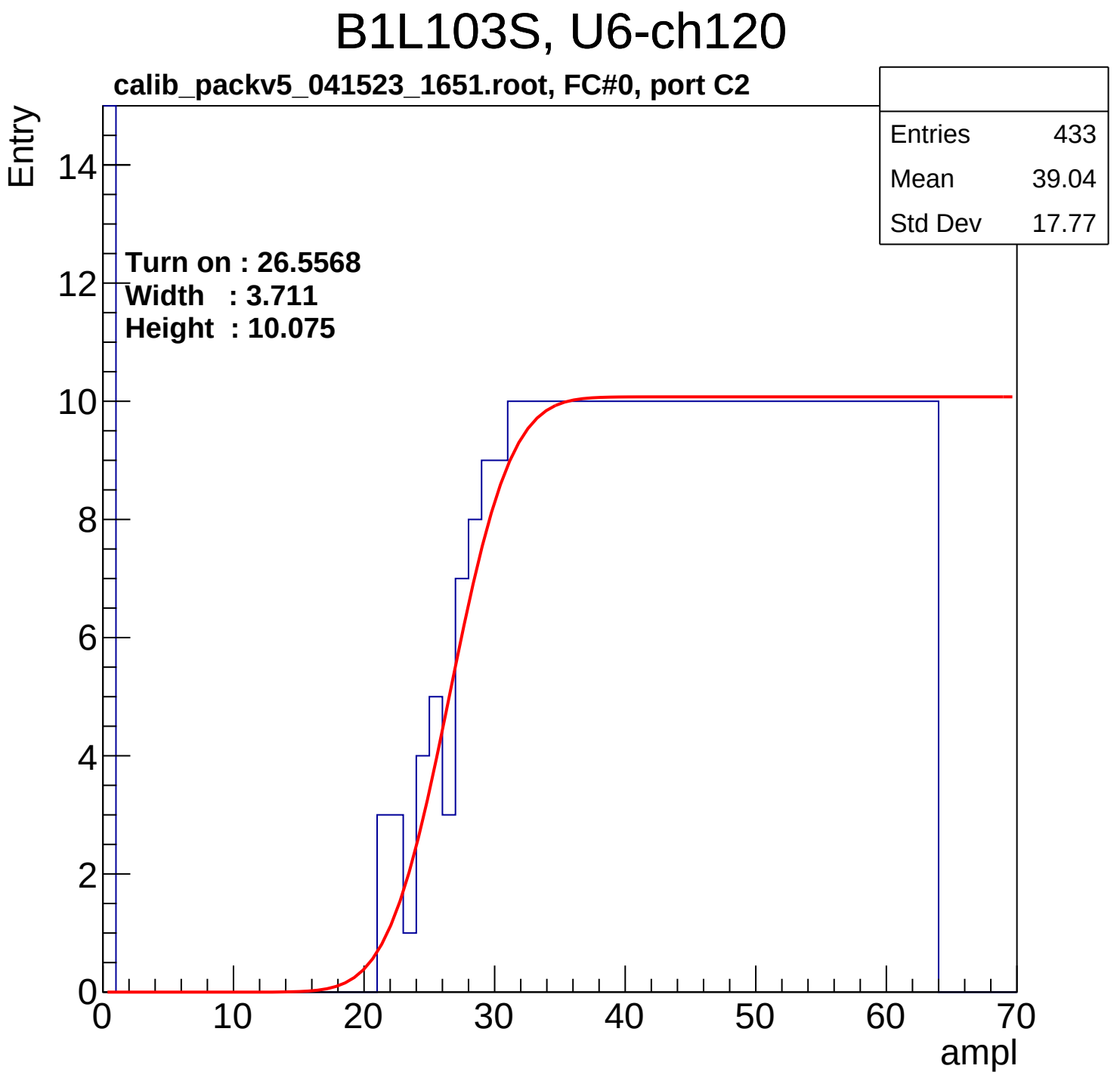

B1L103S, U6-ch115
calib_packv5_041523_1651.root, FC#0, port C2
Entries 432
Mean 38.55
Std Dev 18.53
Turn on : 27.0304
Width : 2.788
Height : 9.984
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

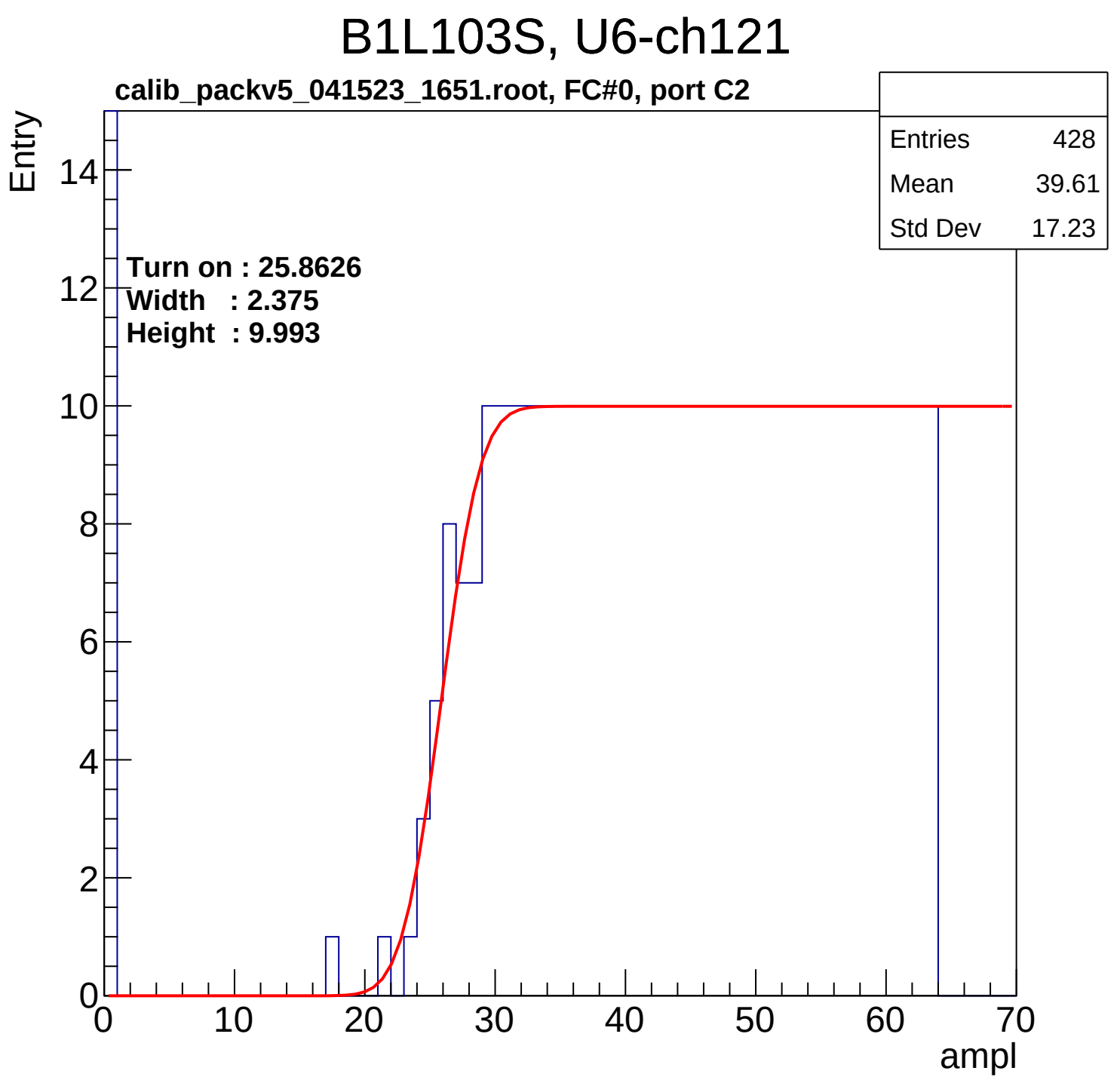

B1L103S, U6-ch116
calib_packv5_041523_1651.root, FC#0, port C2
Entries 454
Mean 38.93
Std Dev 16.75
Turn on : 22.6745
Width : 2.400
Height : 9.950
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

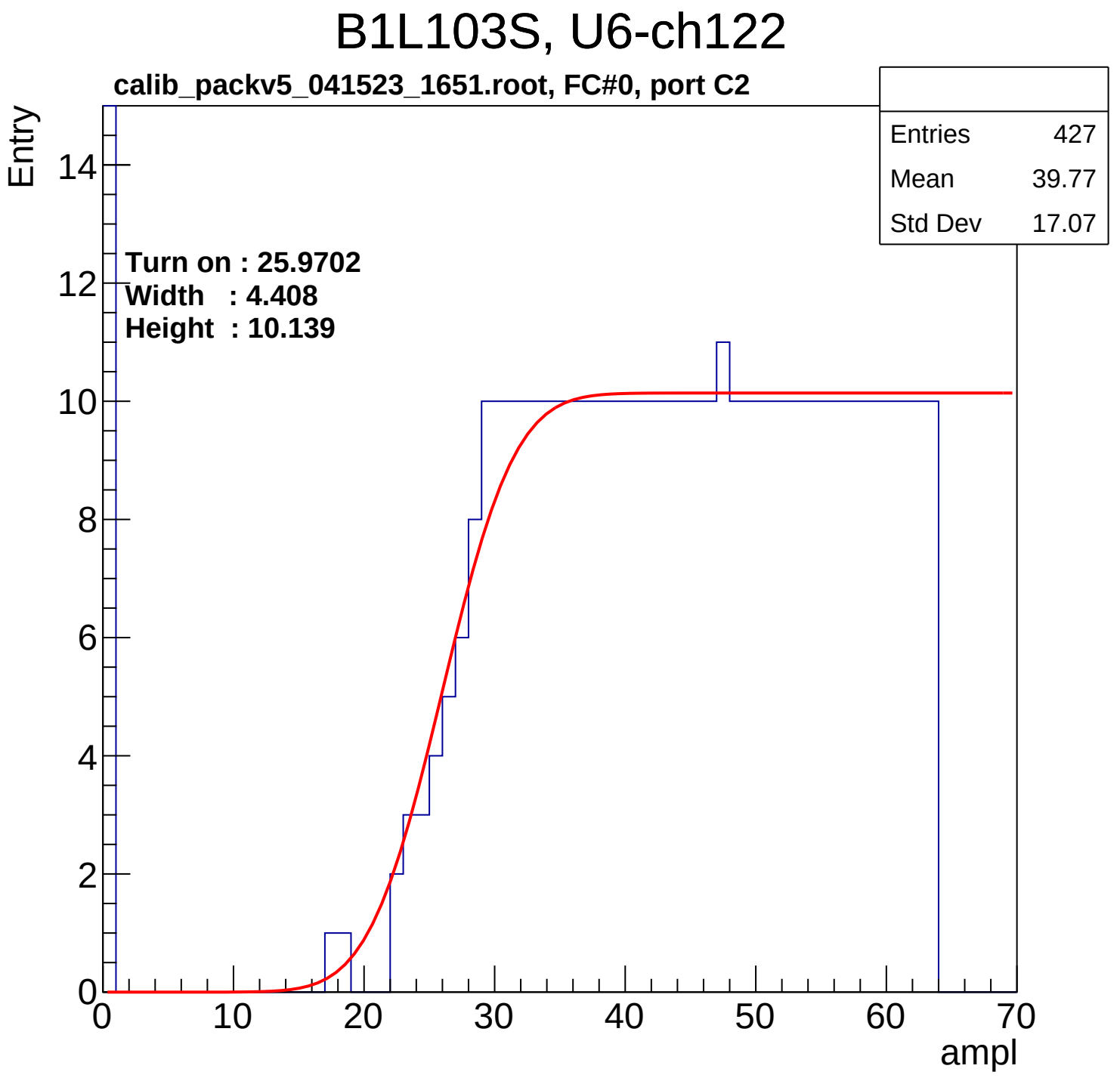

B1L103S, U6-ch117
calib_packv5_041523_1651.root, FC#0, port C2
Entries 421
Mean 40.11
Std Dev 16.82
Turn on : 26.4161
Width : 3.580
Height : 10.044
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

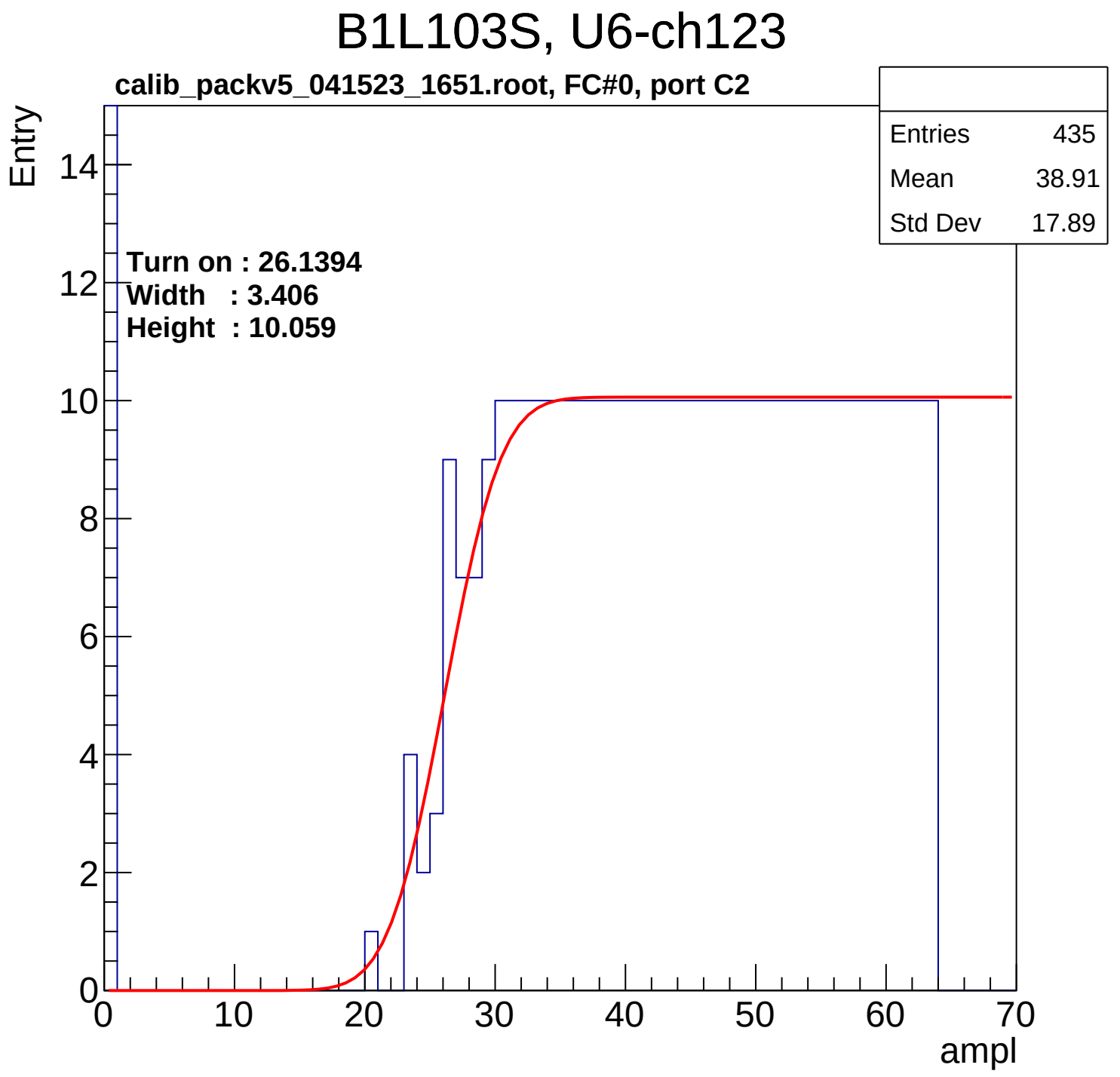

B1L103S, U6-ch118
calib_packv5_041523_1651.root, FC#0, port C2
Entries 432
Mean 39.73
Std Dev 16.77
Turn on : 24.5929
Width : 3.334
Height : 9.983
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

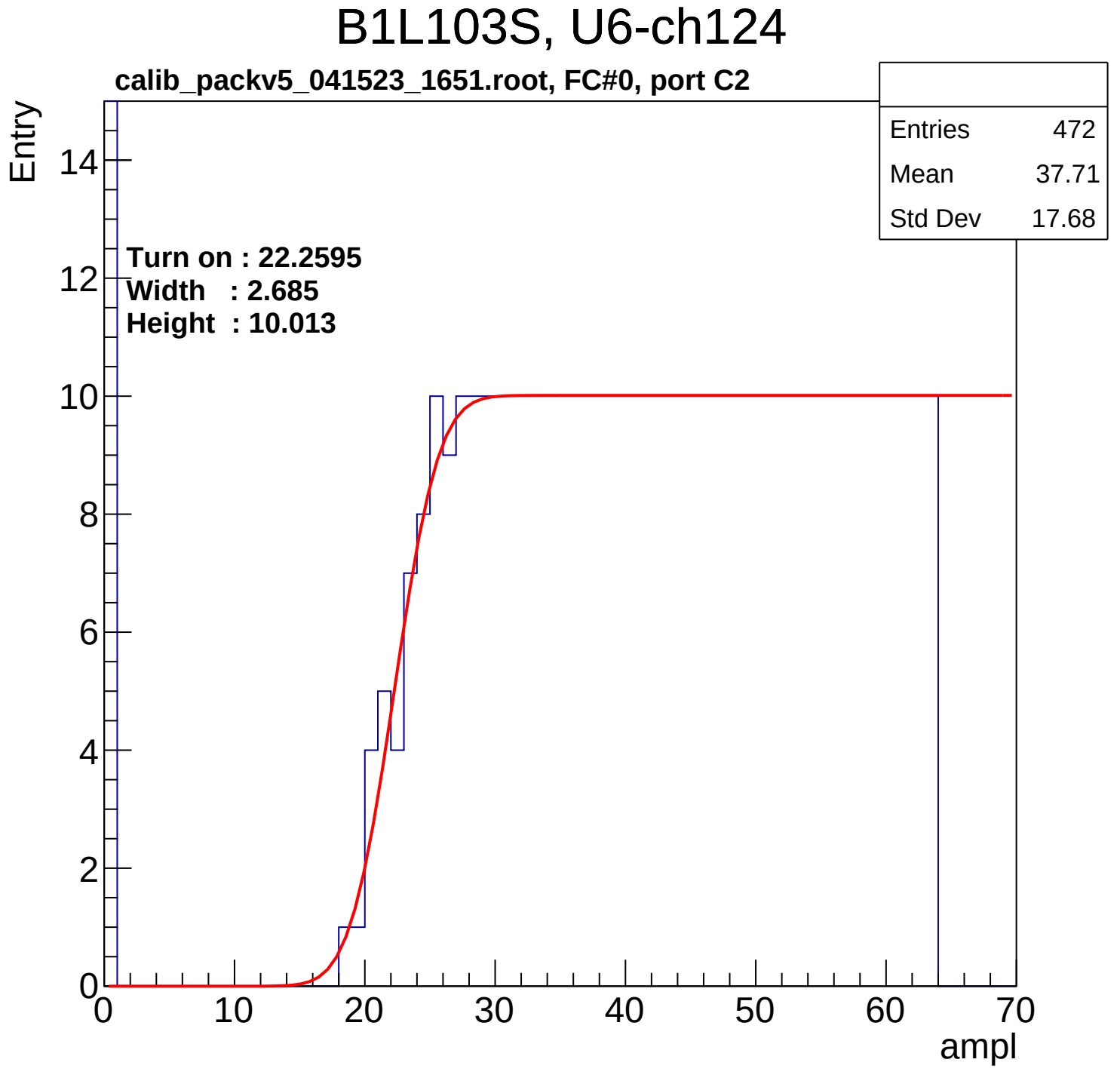

B1L103S, U6-ch119
calib_packv5_041523_1651.root, FC#0, port C2
Entries 440
Mean 38.75
Std Dev 17.8
Turn on : 25.2070
Width : 3.460
Height : 9.977
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

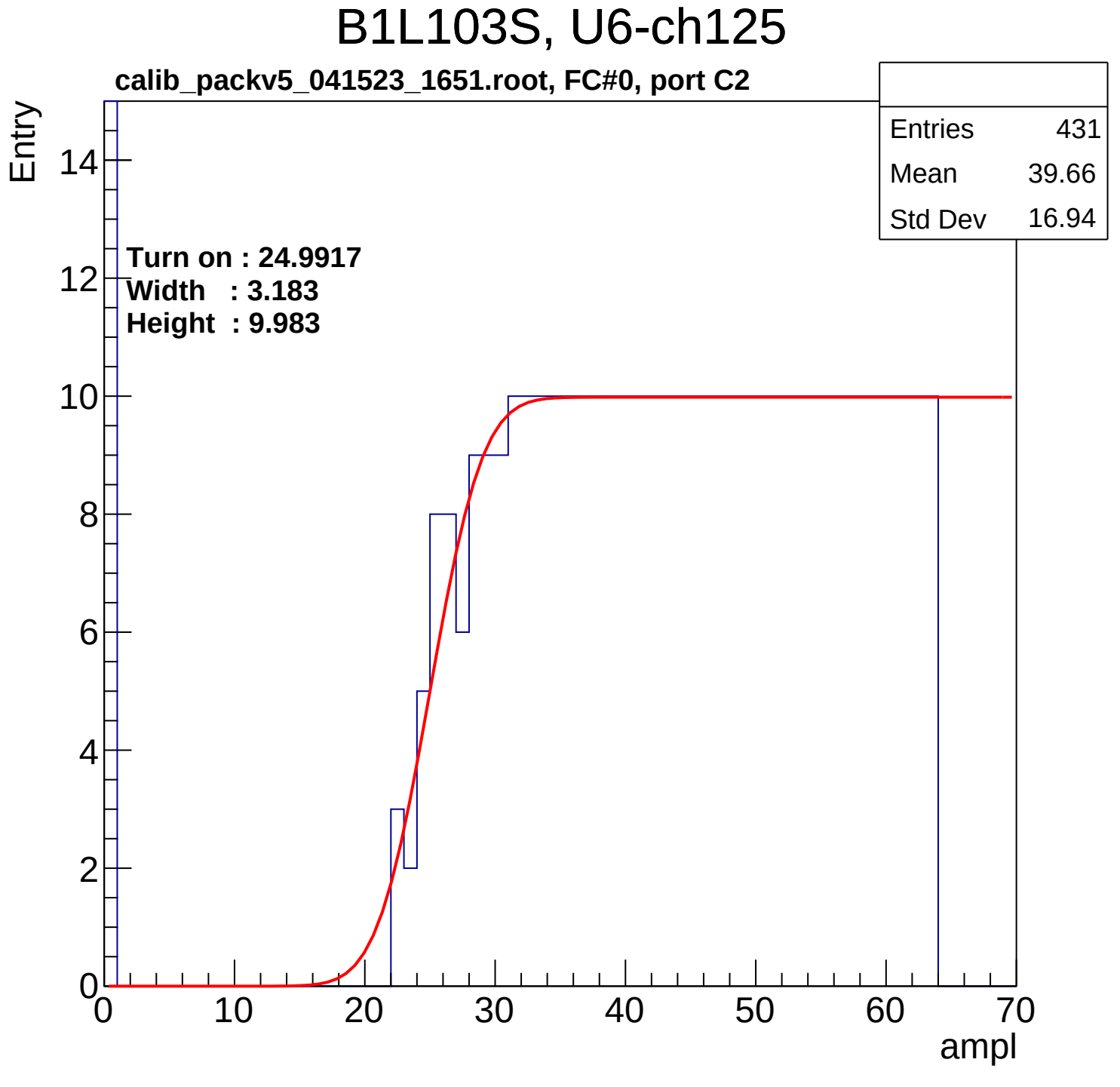

B1L103S, U6-ch120
calib_packv5_041523_1651.root, FC#0, port C2
Entries 433
Mean 39.04
Std Dev 17.77
Turn on : 26.5568
Width : 3.711
Height : 10.075
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

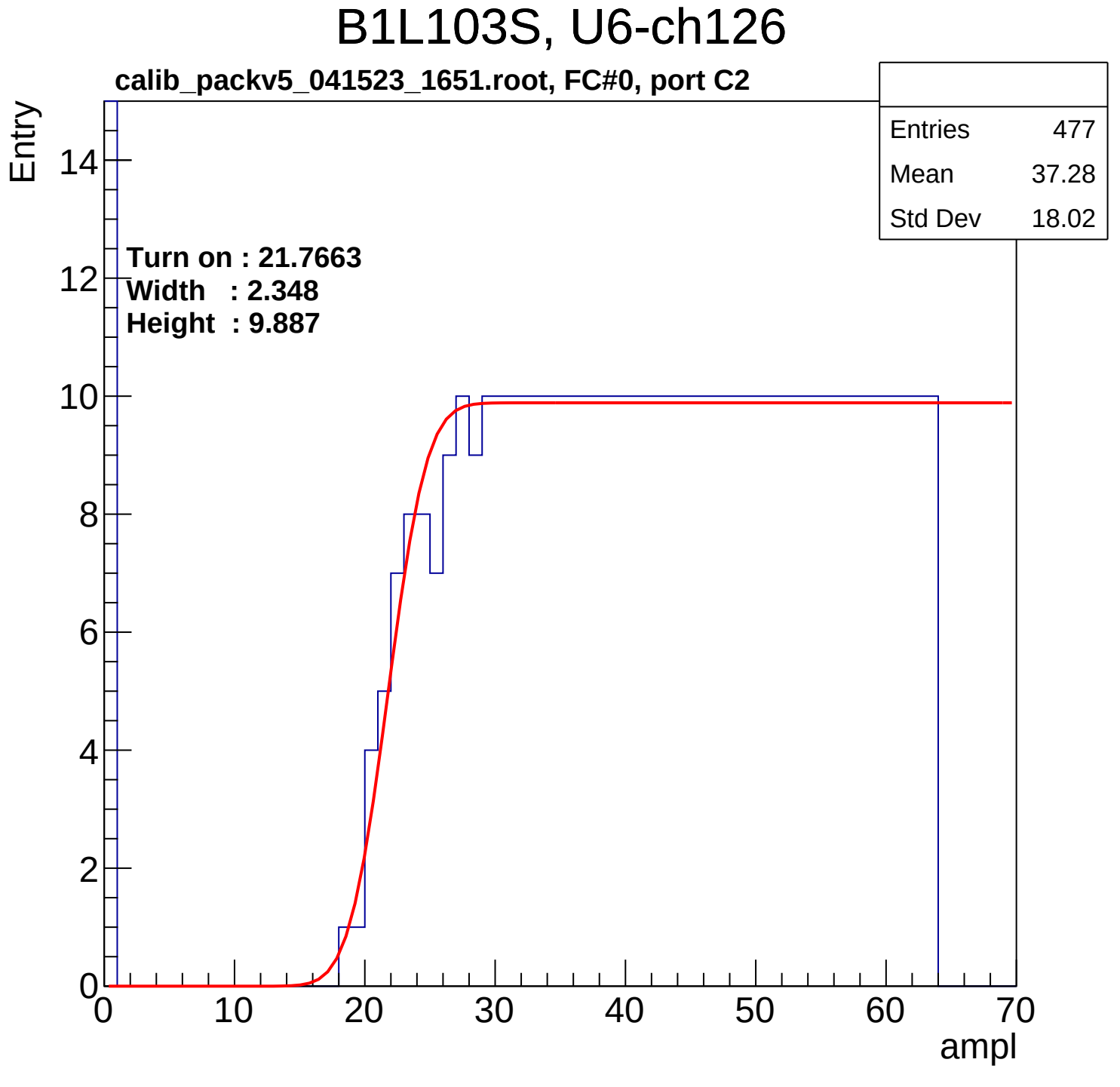

B1L103S, U6-ch121
calib_packv5_041523_1651.root, FC#0, port C2
Entries 428
Mean 39.61
Std Dev 17.23
Turn on : 25.8626
Width : 2.375
Height : 9.993
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

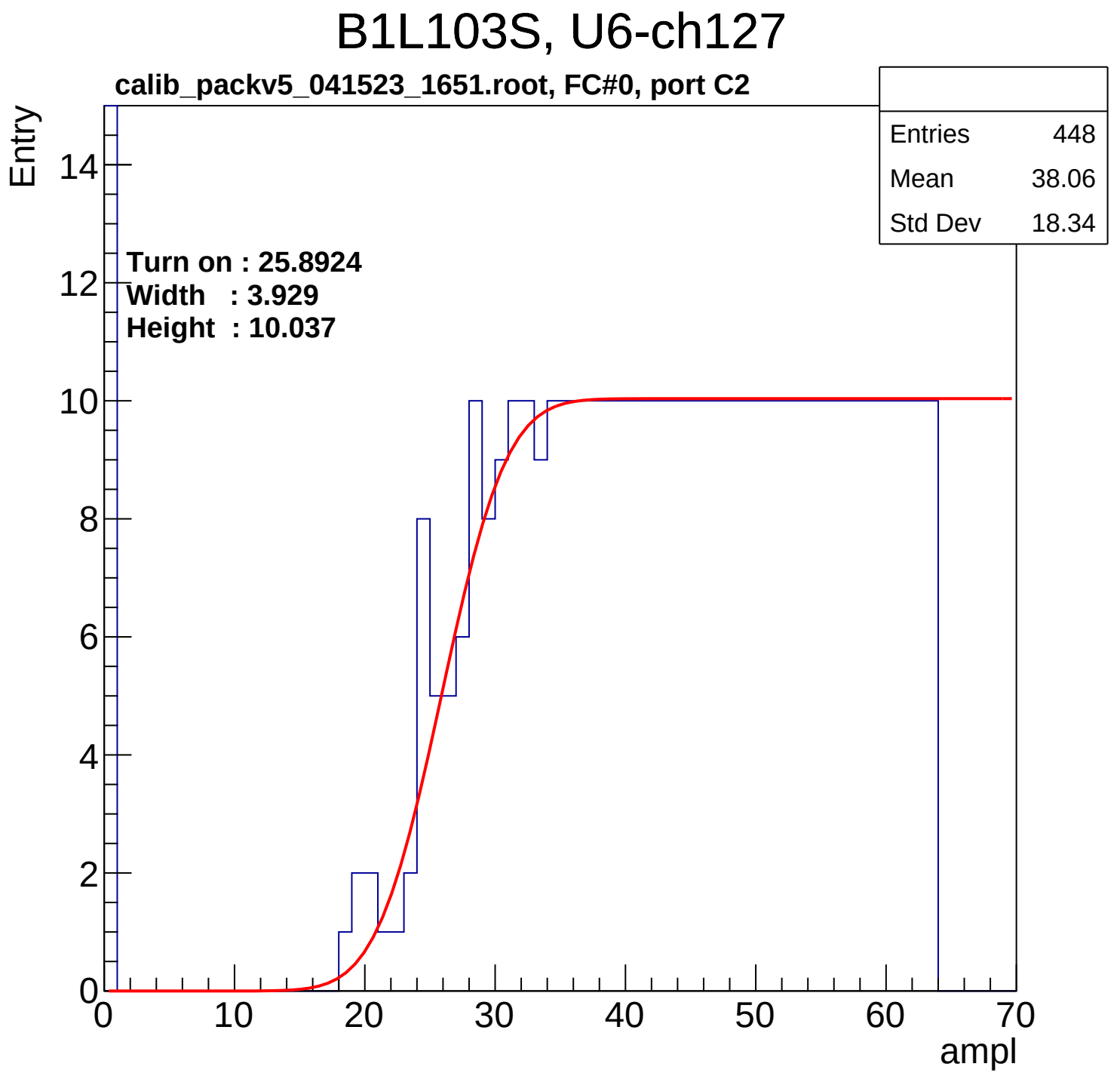

B1L103S, U6-ch122
calib_packv5_041523_1651.root, FC#0, port C2
Entries 427
Mean 39.77
Std Dev 17.07
Turn on : 25.9702
Width : 4.408
Height : 10.139
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

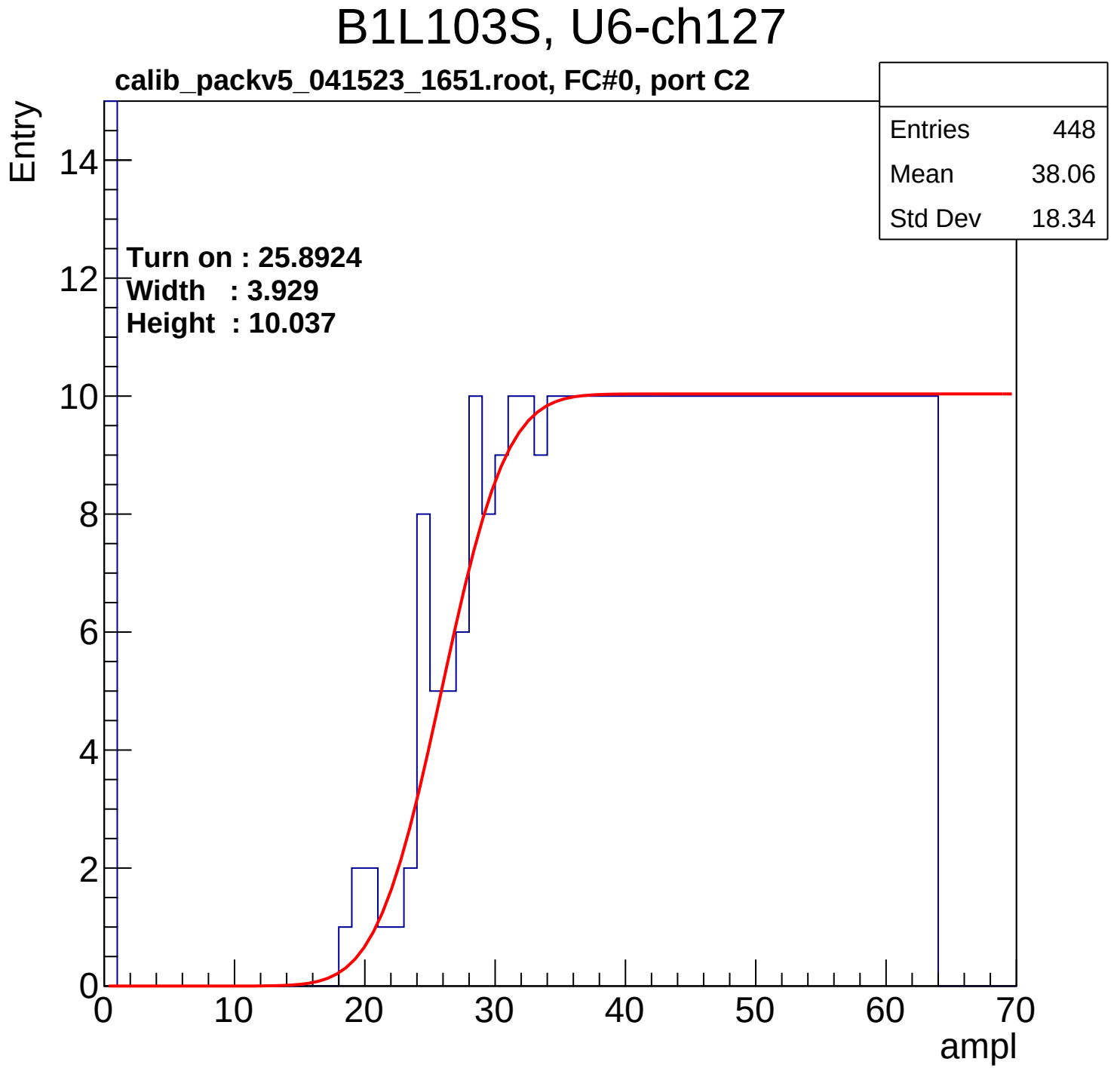

B1L103S, U6-ch123
calib_packv5_041523_1651.root, FC#0, port C2
Entries 435
Mean 38.91
Std Dev 17.89
Turn on : 26.1394
Width : 3.406
Height : 10.059
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L103S, U6-ch124
calib_packv5_041523_1651.root, FC#0, port C2
Entries 472
Mean 37.71
Std Dev 17.68
Turn on : 22.2595
Width : 2.685
Height : 10.013
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L103S, U6-ch125
calib_packv5_041523_1651.root, FC#0, port C2
Entries 431
Mean 39.66
Std Dev 16.94
Turn on : 24.9917
Width : 3.183
Height : 9.983
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L103S, U6-ch126
calib_packv5_041523_1651.root, FC#0, port C2
Entries 477
Mean 37.28
Std Dev 18.02
Turn on : 21.7663
Width : 2.348
Height : 9.887
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L103S, U6-ch127
calib_packv5_041523_1651.root, FC#0, port C2
Entries 448
Mean 38.06
Std Dev 18.34
Turn on : 25.8924
Width : 3.929
Height : 10.037
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L103S, U6-ch127
calib_packv5_041523_1651.root, FC#0, port C2
Entries 448
Mean 38.06
Std Dev 18.34
Turn on : 25.8924
Width : 3.929
Height : 10.037
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70