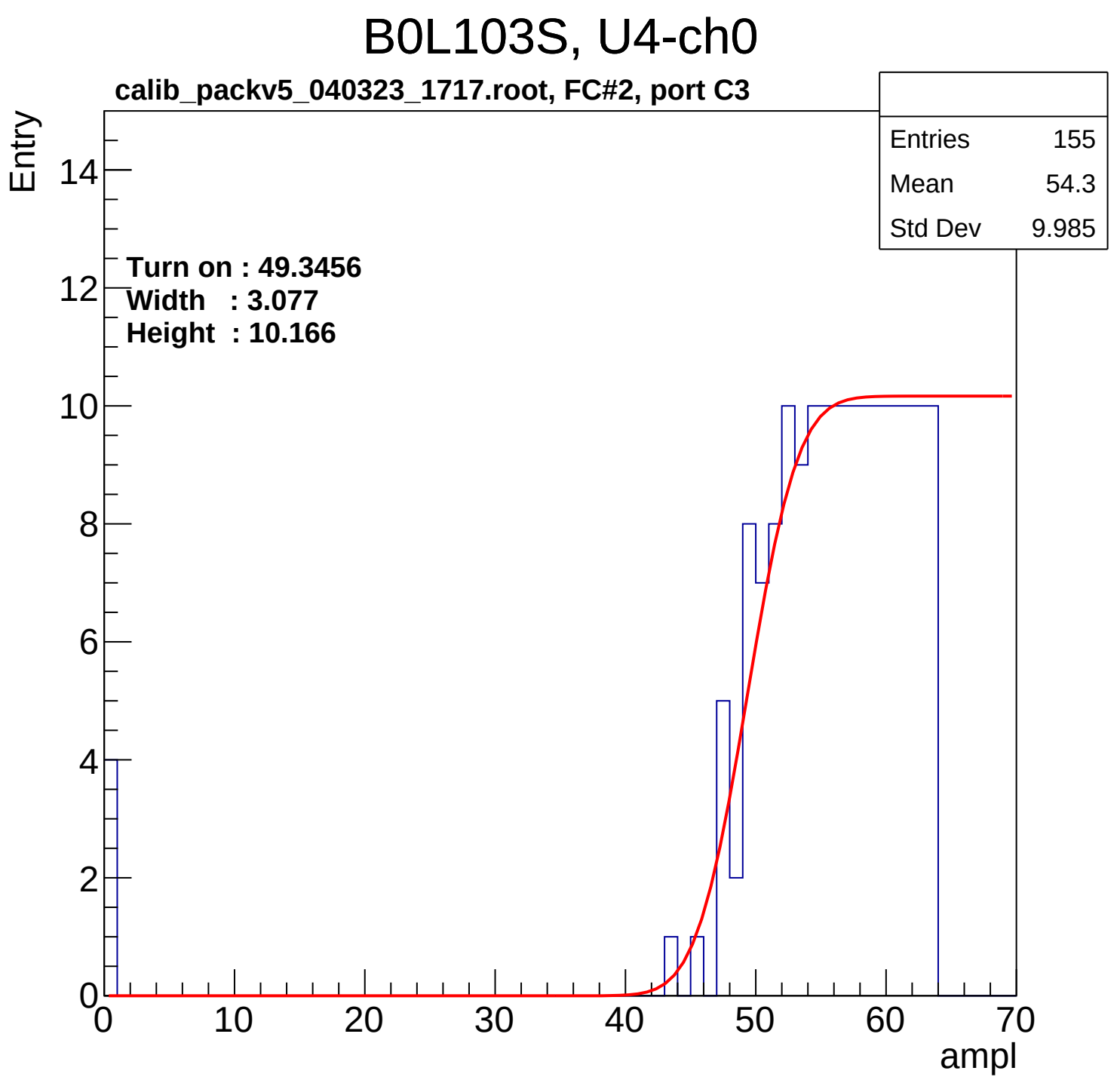
B0L103S, U4-ch0
calib_packv5_040323_1717.root, FC#2, port C3
Entries 155
Mean 54.3
Std Dev 9.985
Turn on : 49.3456
Width : 3.077
Height : 10.166
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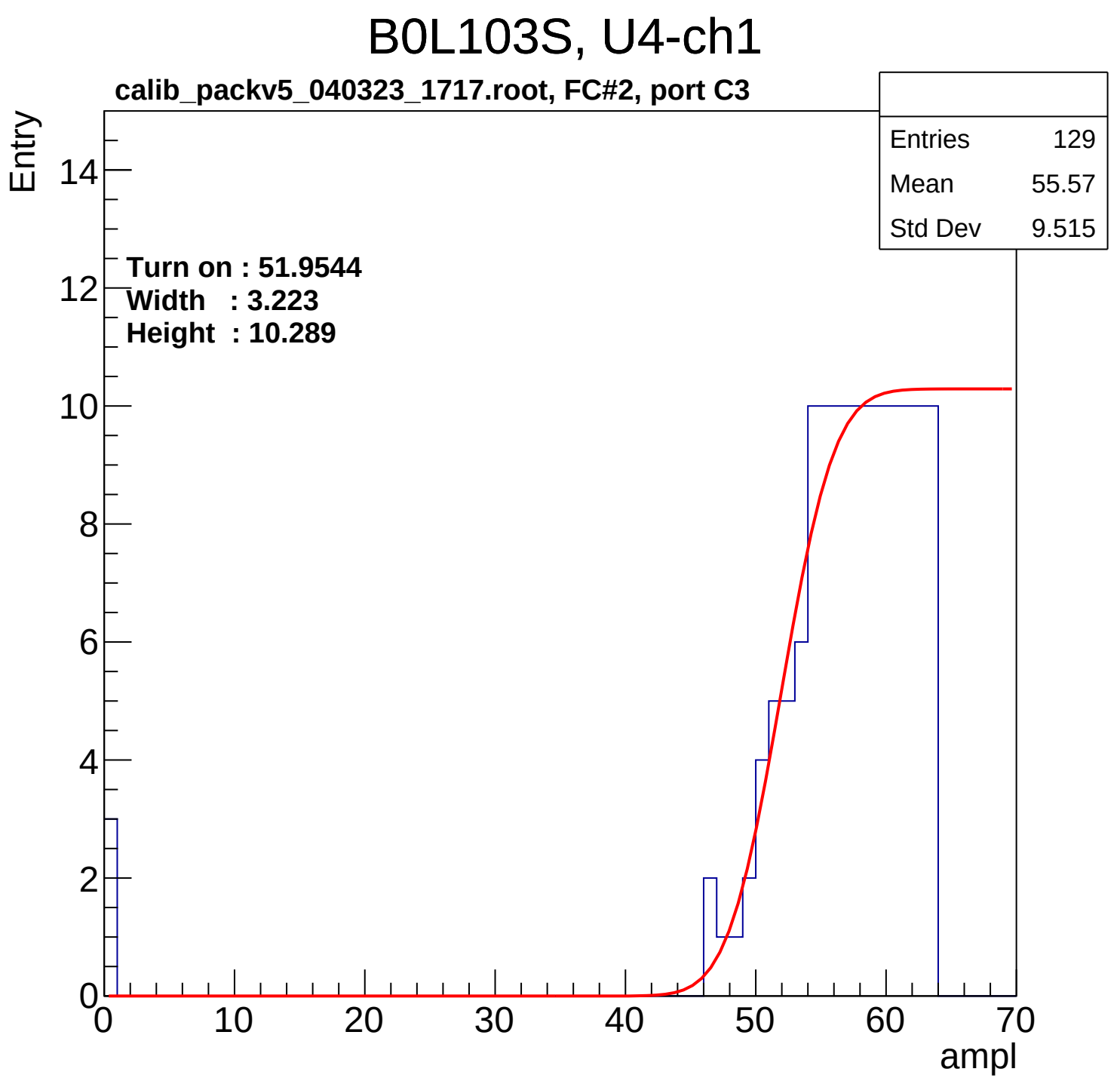
B0L103S, U4-ch1
calib_packv5_040323_1717.root, FC#2, port C3
Entries 129
Mean 55.57
Std Dev 9.515
Turn on : 51.9544
Width : 3.223
Height : 10.289
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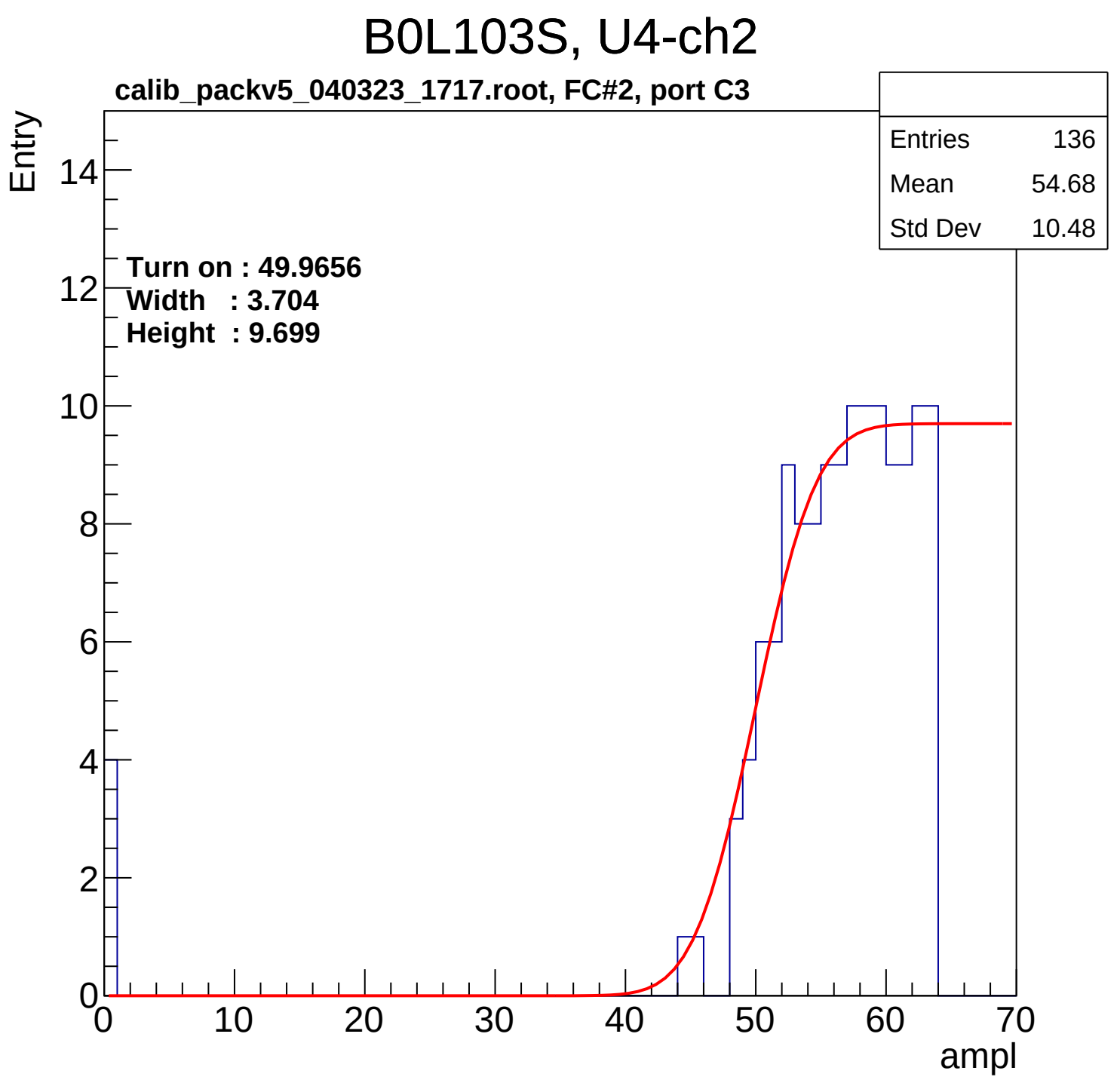
B0L103S, U4-ch2
calib_packv5_040323_1717.root, FC#2, port C3
Entries 136
Mean 54.68
Std Dev 10.48
Turn on : 49.9656
Width : 3.704
Height : 9.699
Entry
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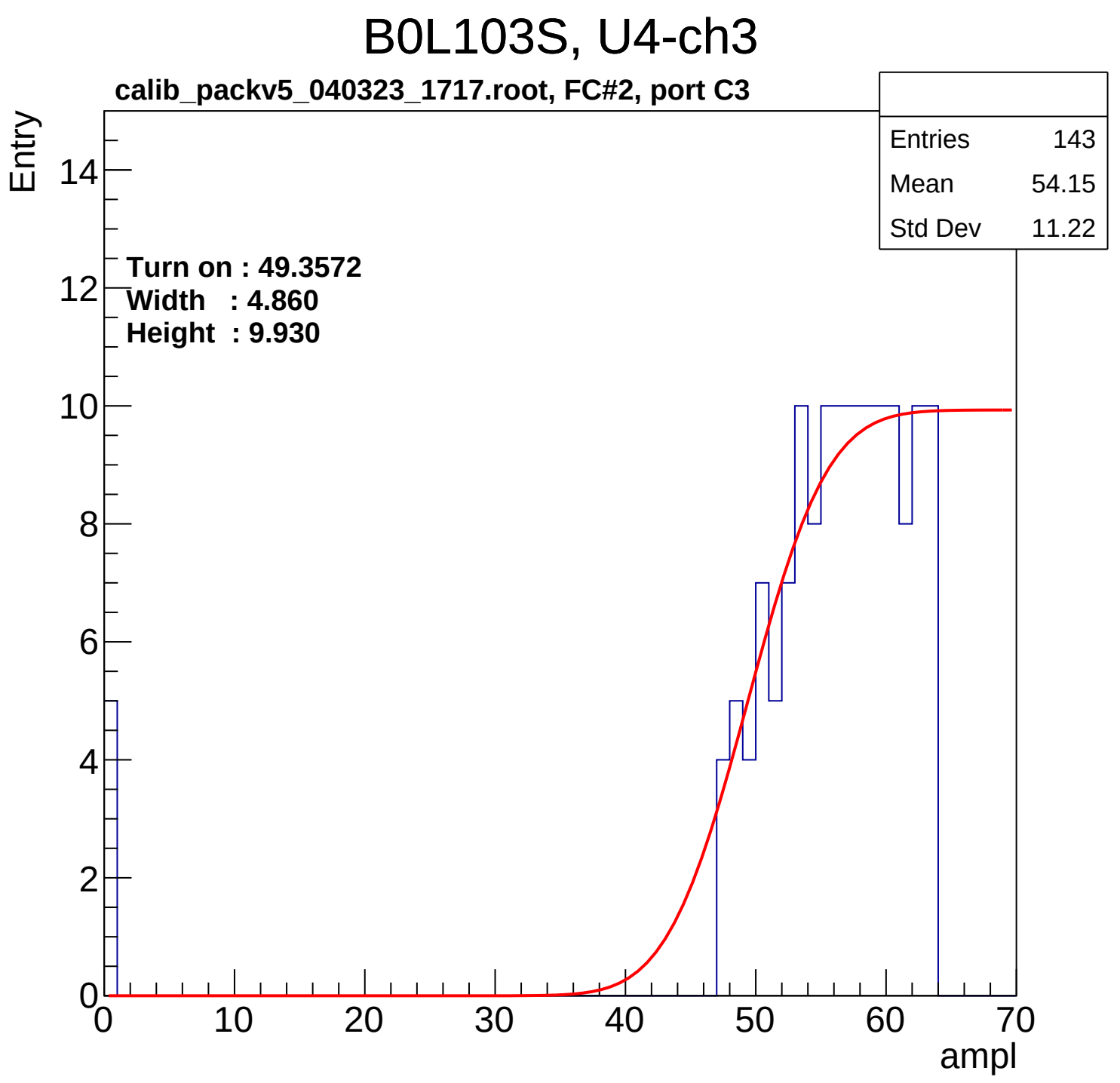
B0L103S, U4-ch3
calib_packv5_040323_1717.root, FC#2, port C3
Entries 143
Mean 54.15
Std Dev 11.22
Turn on : 49.3572
Width : 4.860
Height : 9.930
Entry
ampl
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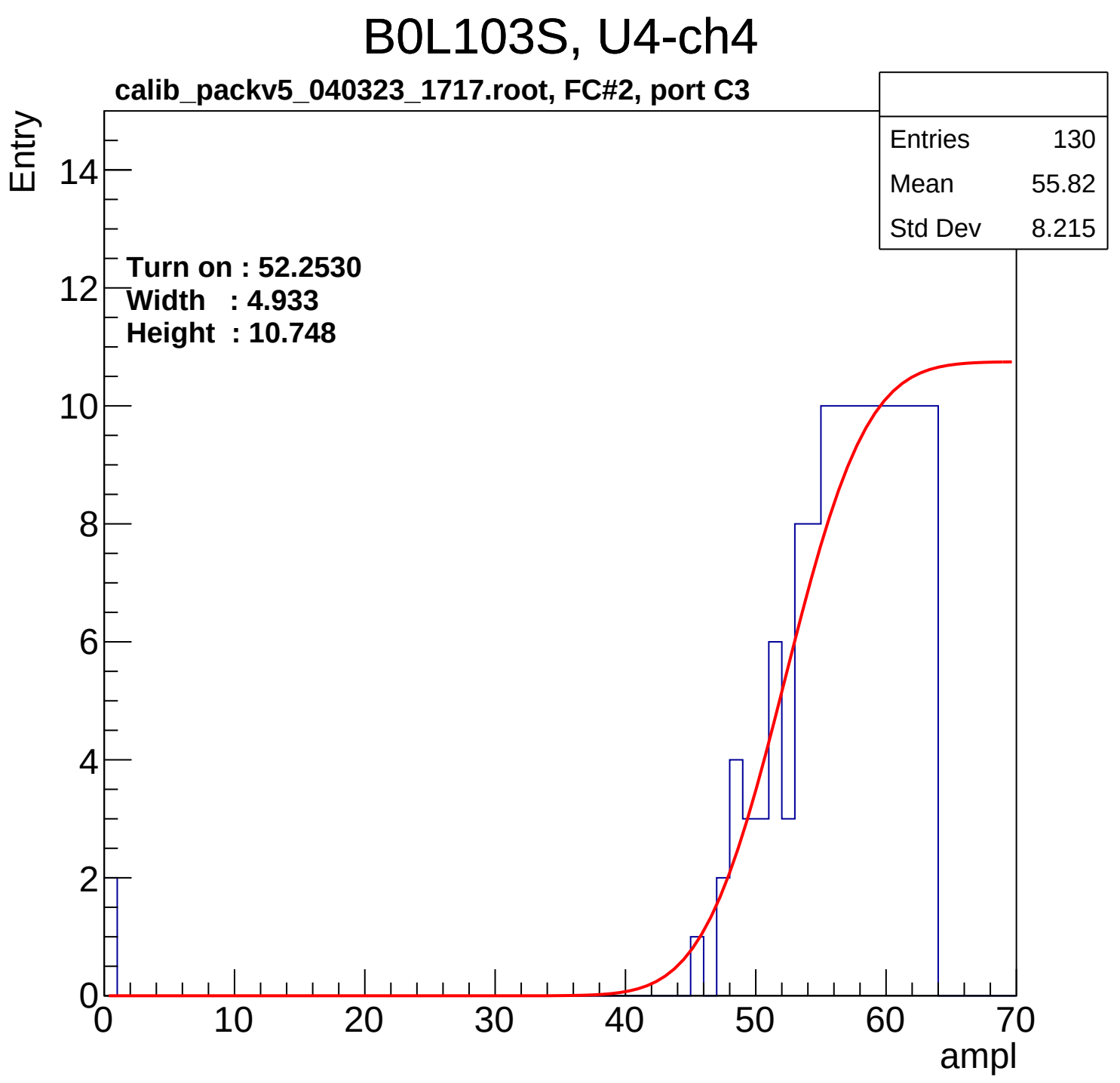
B0L103S, U4-ch4
calib_packv5_040323_1717.root, FC#2, port C3
Entries 130
Mean 55.82
Std Dev 8.215
Turn on : 52.2530
Width : 4.933
Height : 10.748
Entry
ampl
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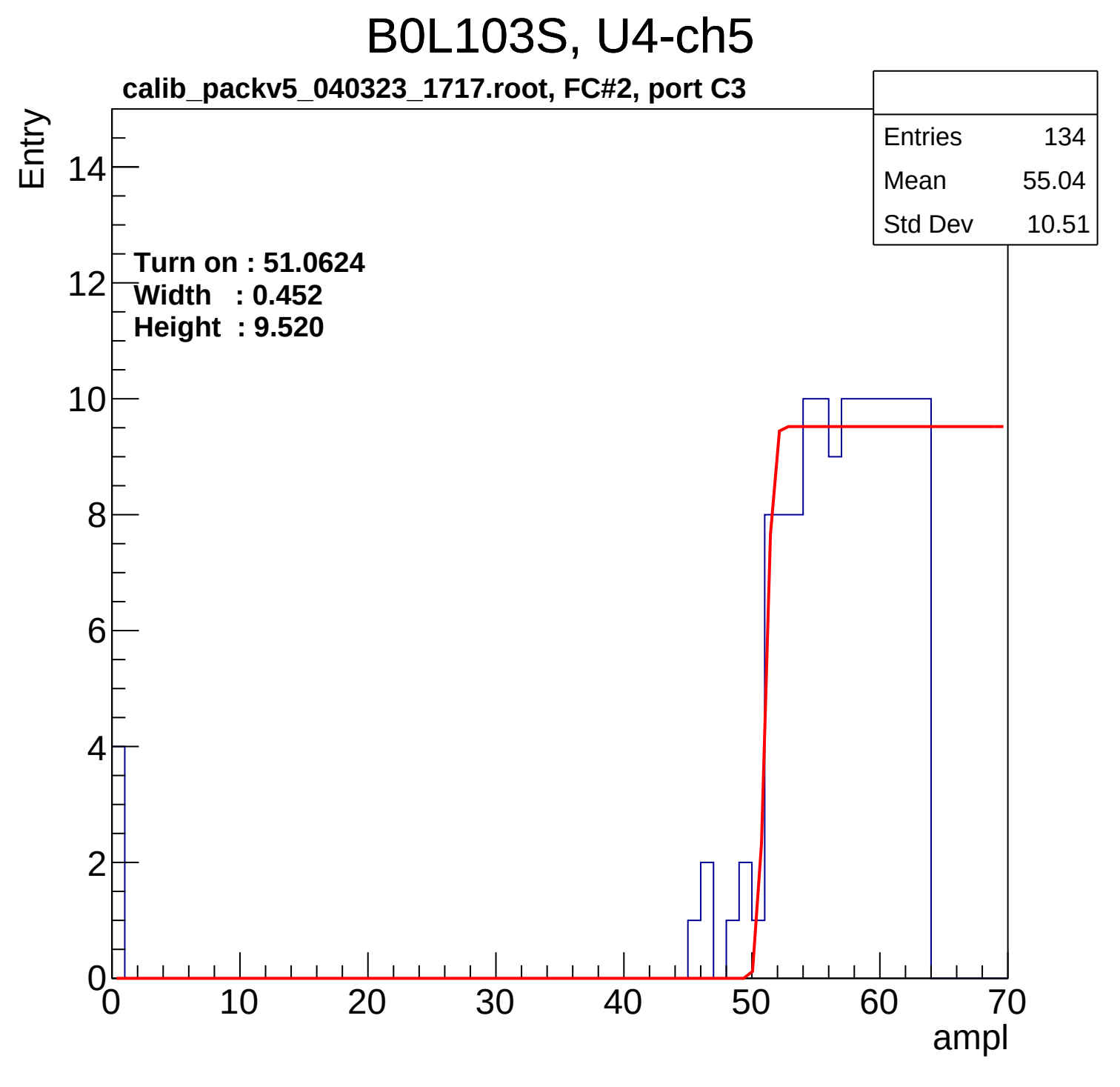
B0L103S, U4-ch5
calib_packv5_040323_1717.root, FC#2, port C3
Entries 134
Mean 55.04
Std Dev 10.51
Turn on : 51.0624
Width : 0.452
Height : 9.520
Entry
ampl
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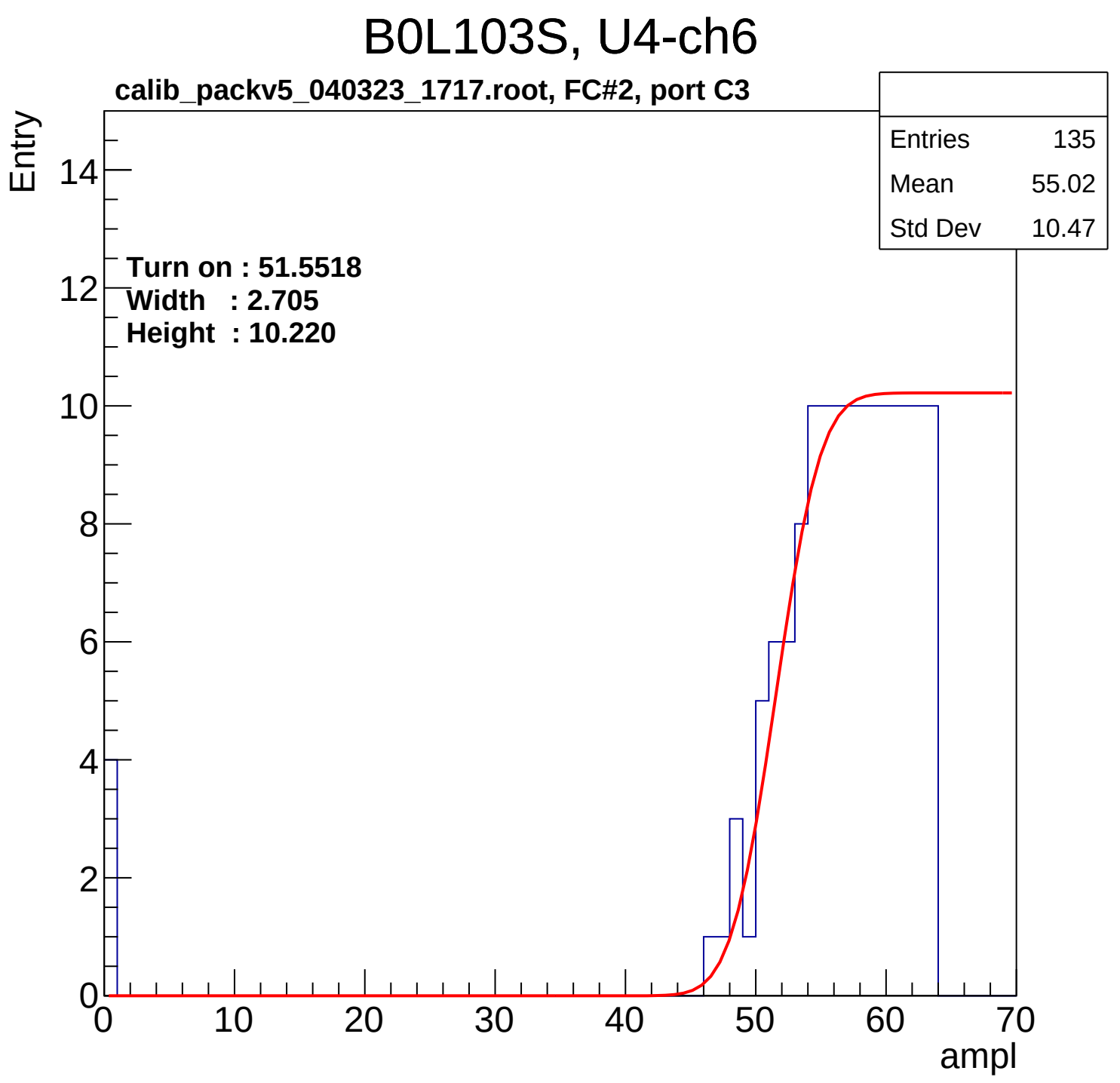
B0L103S, U4-ch6
calib_packv5_040323_1717.root, FC#2, port C3
Entries 135
Mean 55.02
Std Dev 10.47
Turn on : 51.5518
Width : 2.705
Height : 10.220
Entry
ampl
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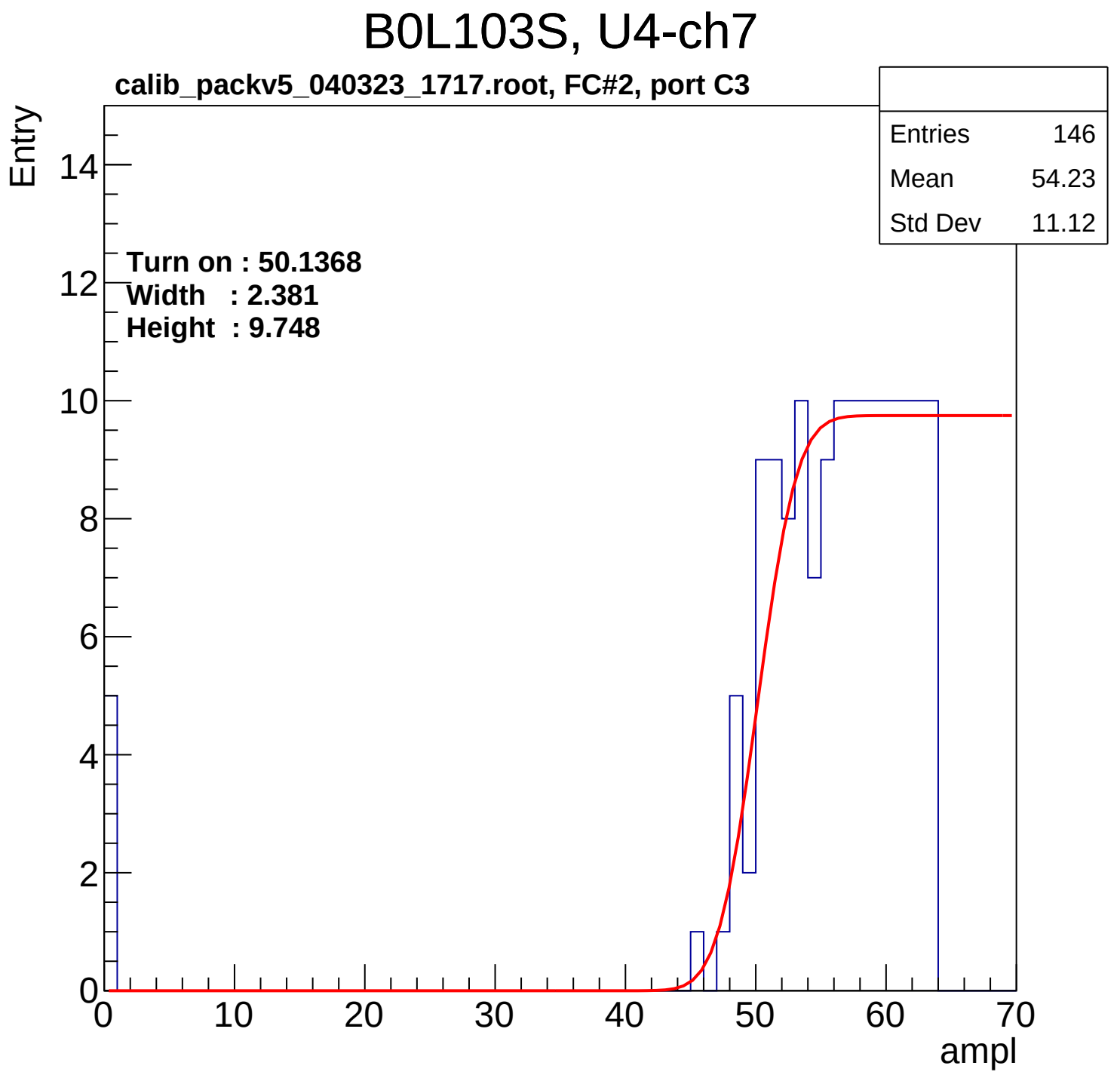
B0L103S, U4-ch7
calib_packv5_040323_1717.root, FC#2, port C3
Entries 146
Mean 54.23
Std Dev 11.12
Turn on : 50.1368
Width : 2.381
Height : 9.748
Entry
ampl
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2
4
6
8
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60
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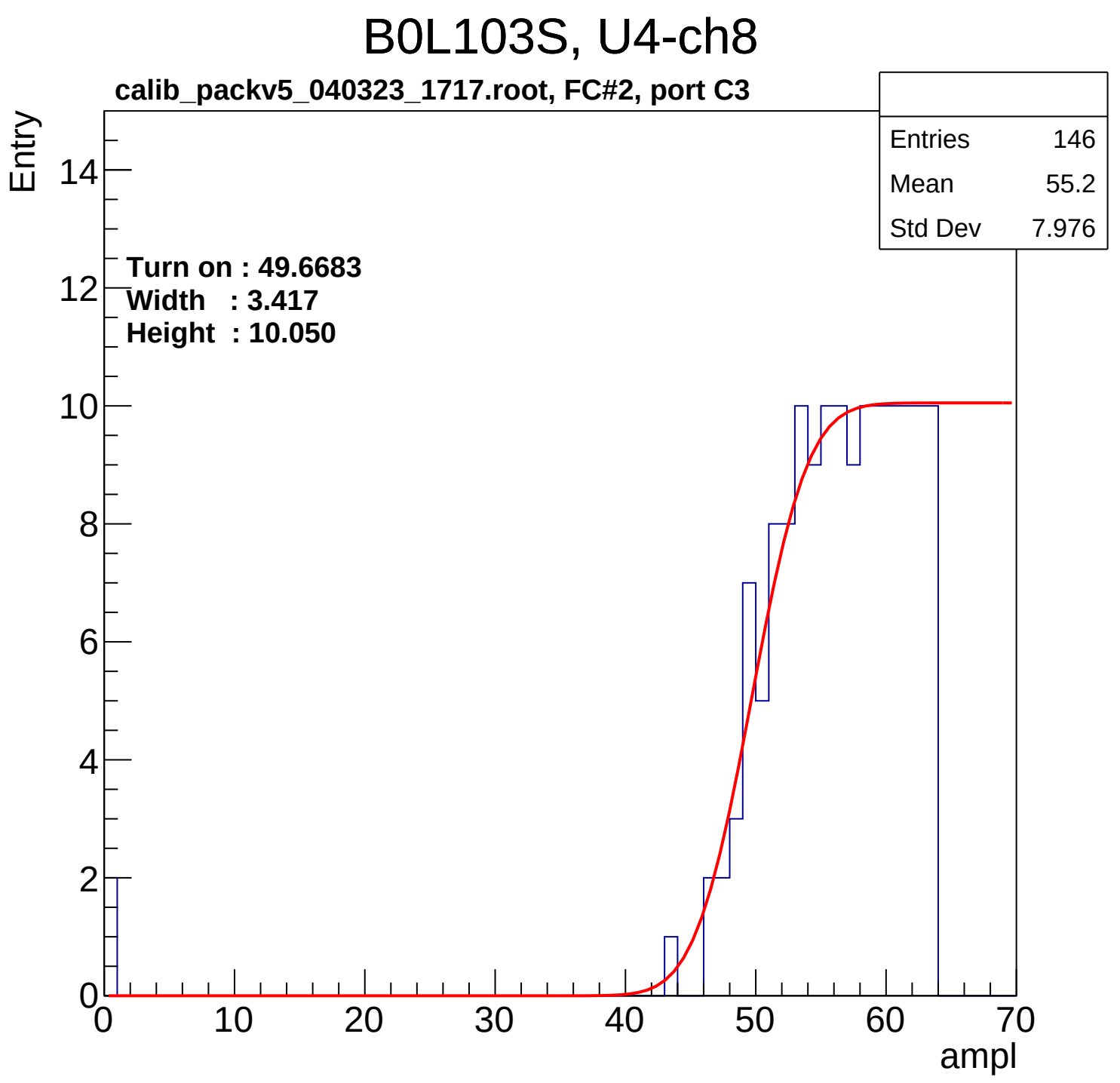
B0L103S, U4-ch8
calib_packv5_040323_1717.root, FC#2, port C3
Entries 146
Mean 55.2
Std Dev 7.976
Turn on : 49.6683
Width : 3.417
Height : 10.050
Entry
ampl
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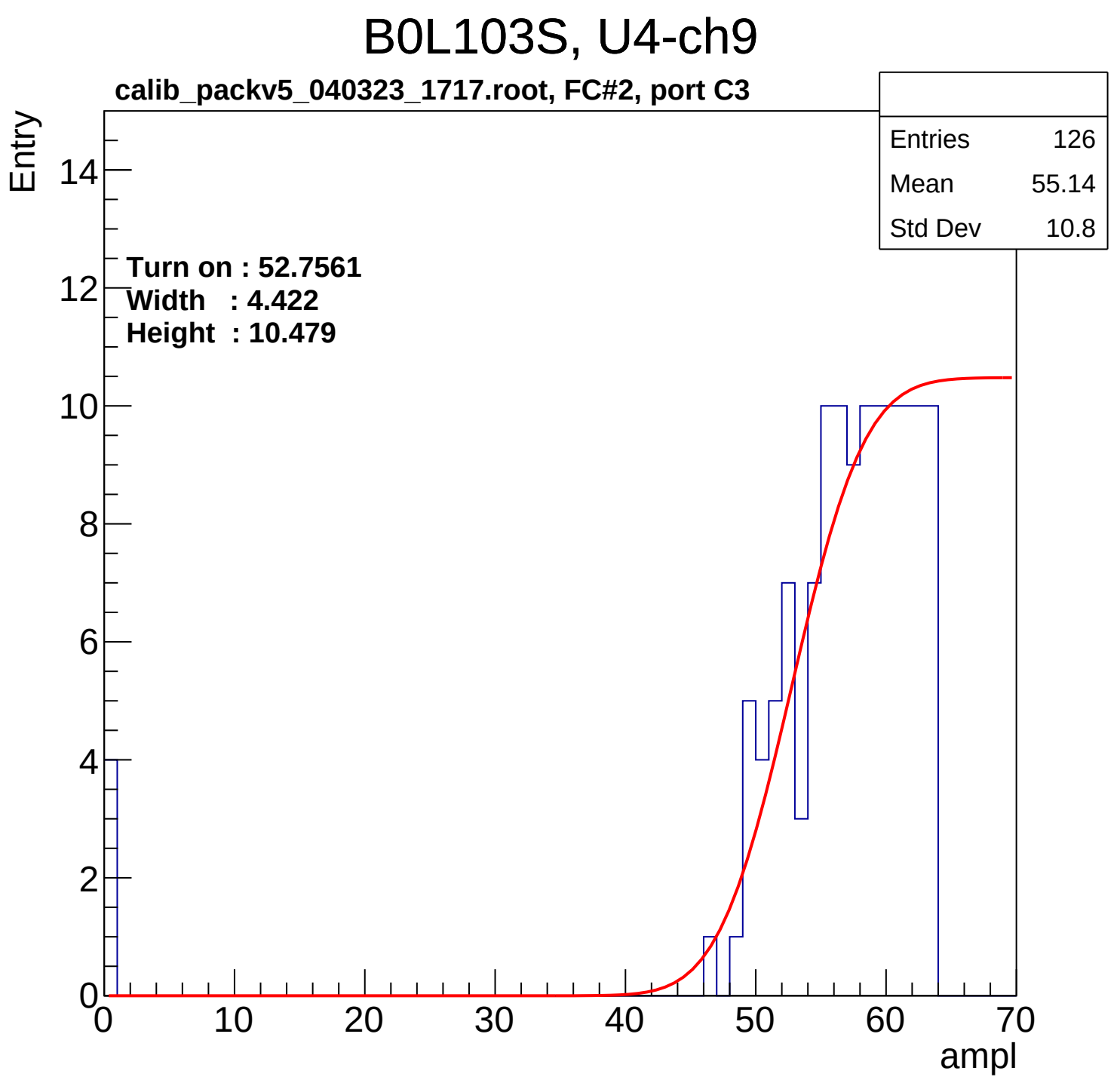
B0L103S, U4-ch9
calib_packv5_040323_1717.root, FC#2, port C3
Entries 126
Mean 55.14
Std Dev 10.8
Turn on : 52.7561
Width : 4.422
Height : 10.479
Entry
ampl
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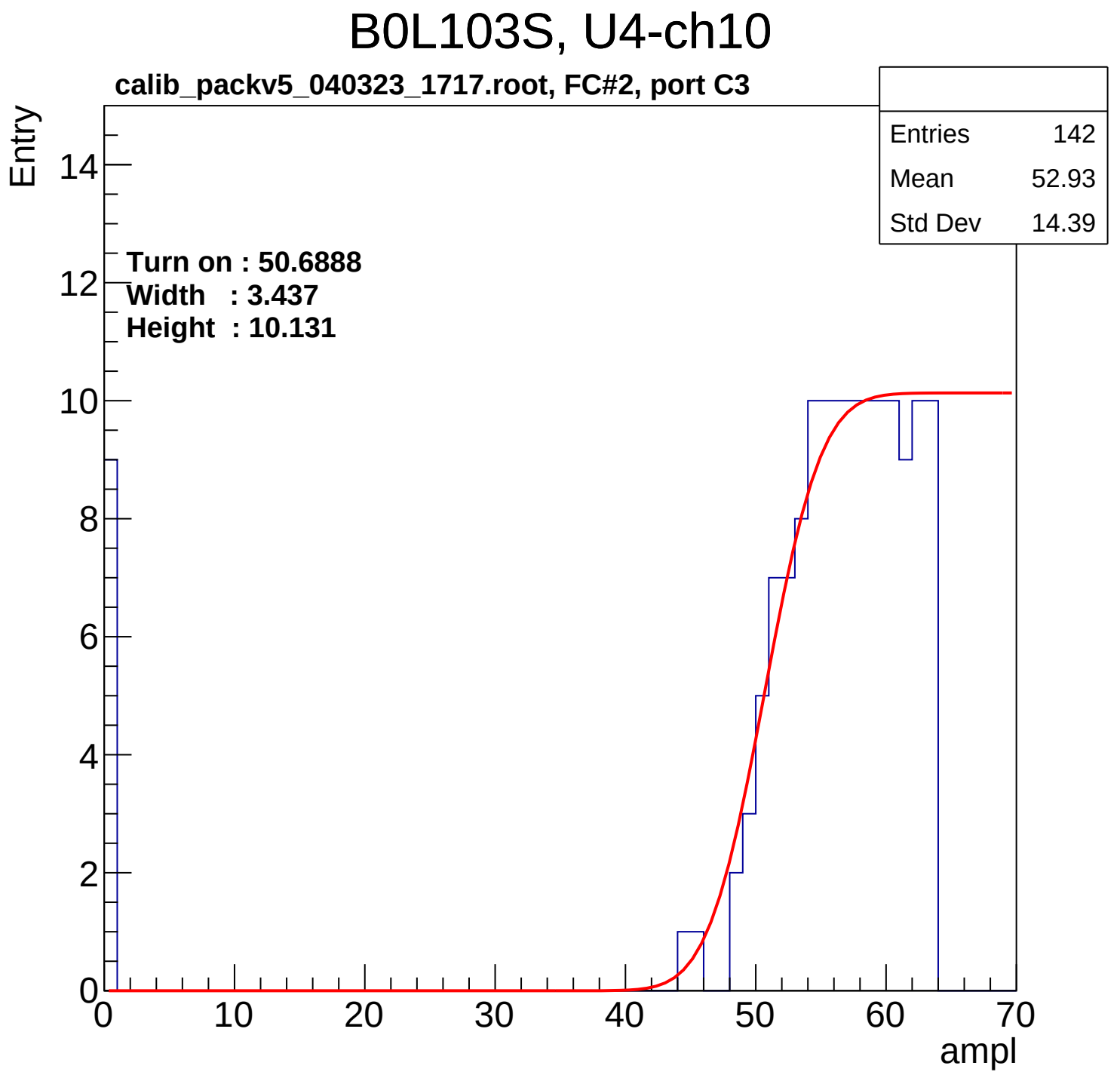
B0L103S, U4-ch10
calib_packv5_040323_1717.root, FC#2, port C3
Entries 142
Mean 52.93
Std Dev 14.39
Turn on : 50.6888
Width : 3.437
Height : 10.131
Entry
ampl
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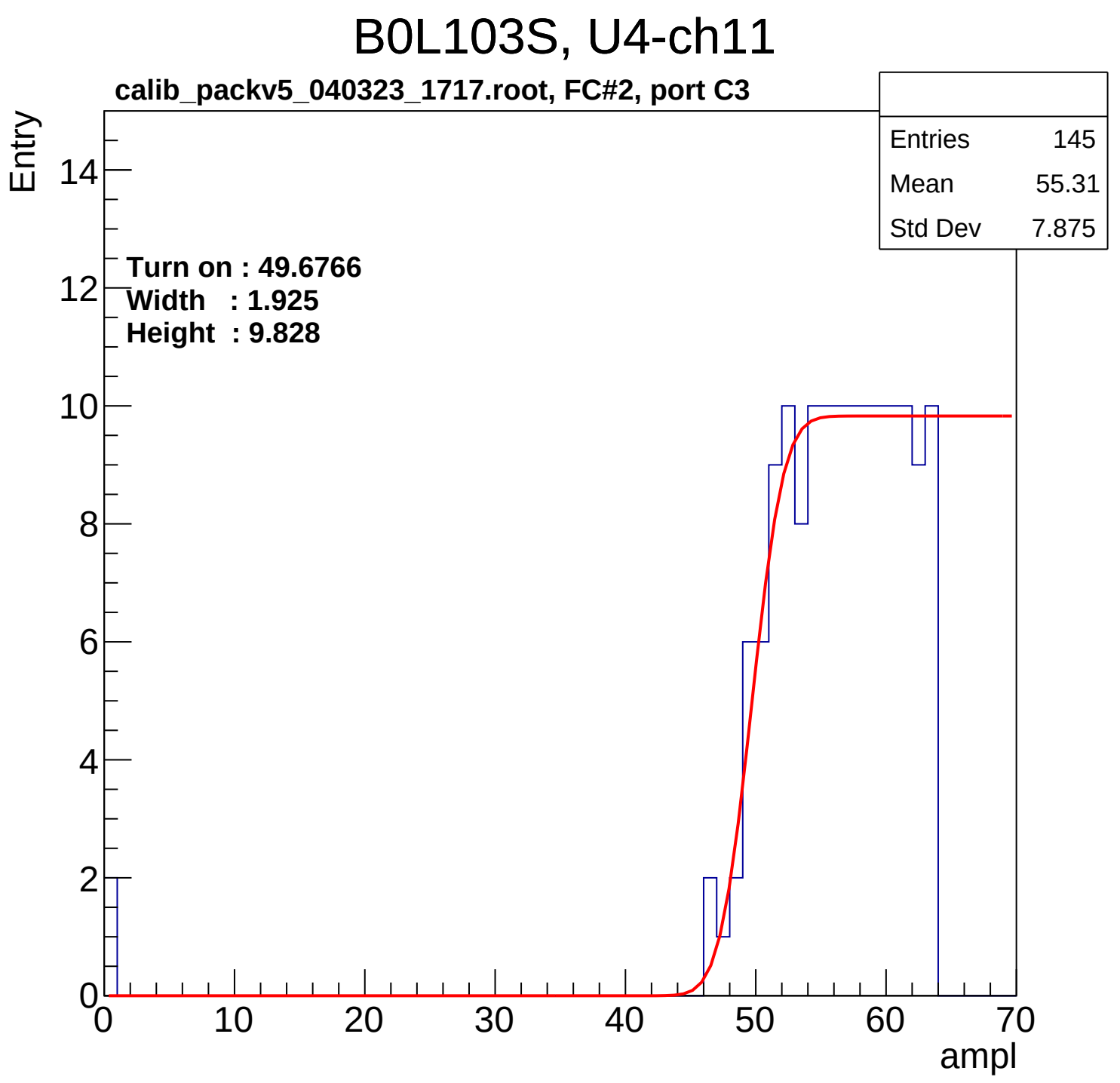
B0L103S, U4-ch11
calib_packv5_040323_1717.root, FC#2, port C3
Entries 145
Mean 55.31
Std Dev 7.875
Turn on : 49.6766
Width : 1.925
Height : 9.828
Entry
ampl
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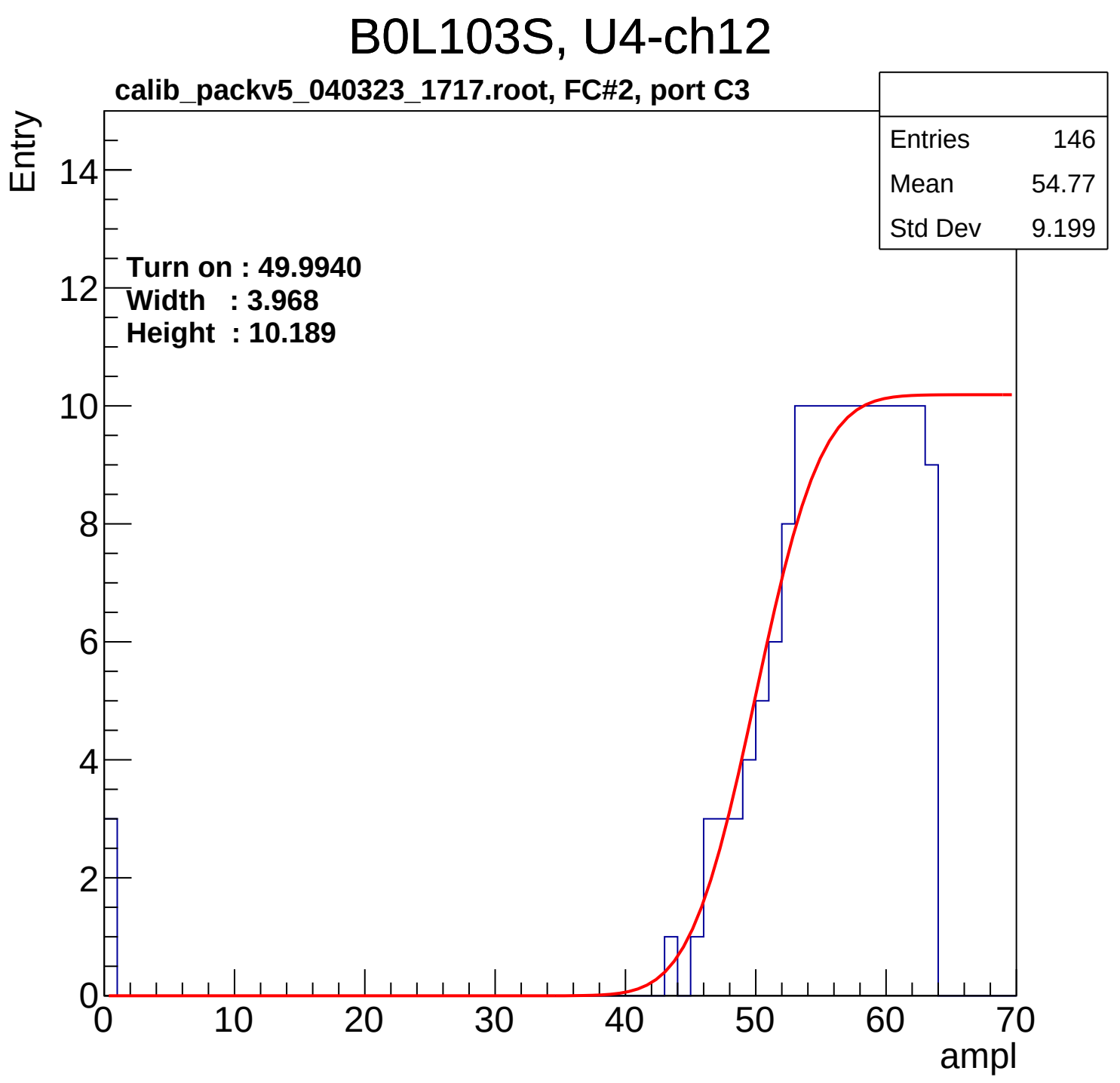
B0L103S, U4-ch12
calib_packv5_040323_1717.root, FC#2, port C3
Entries 146
Mean 54.77
Std Dev 9.199
Turn on : 49.9940
Width : 3.968
Height : 10.189
Entry
ampl
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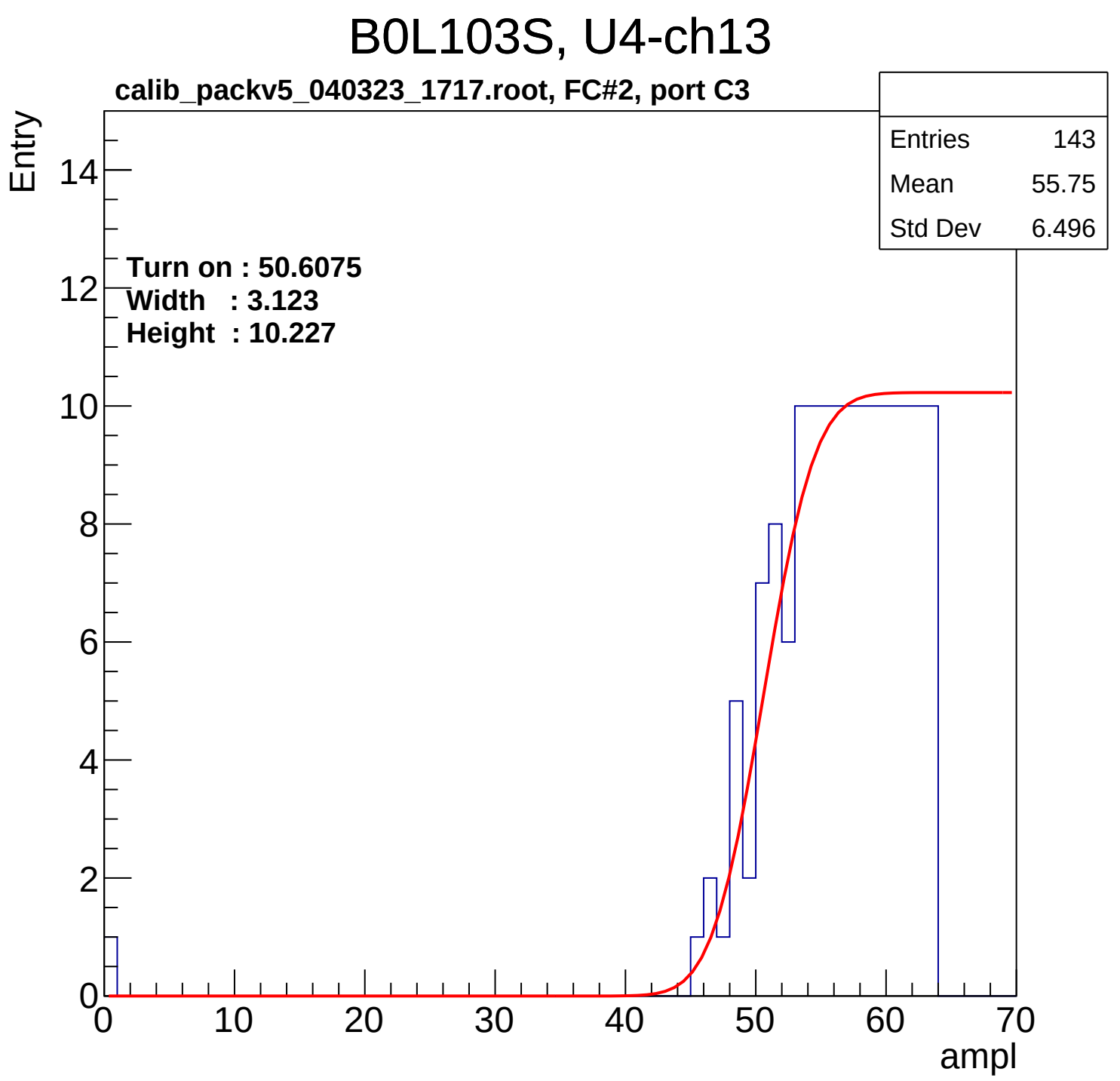
B0L103S, U4-ch13
calib_packv5_040323_1717.root, FC#2, port C3
Entries 143
Mean 55.75
Std Dev 6.496
Turn on : 50.6075
Width : 3.123
Height : 10.227
Entry
ampl
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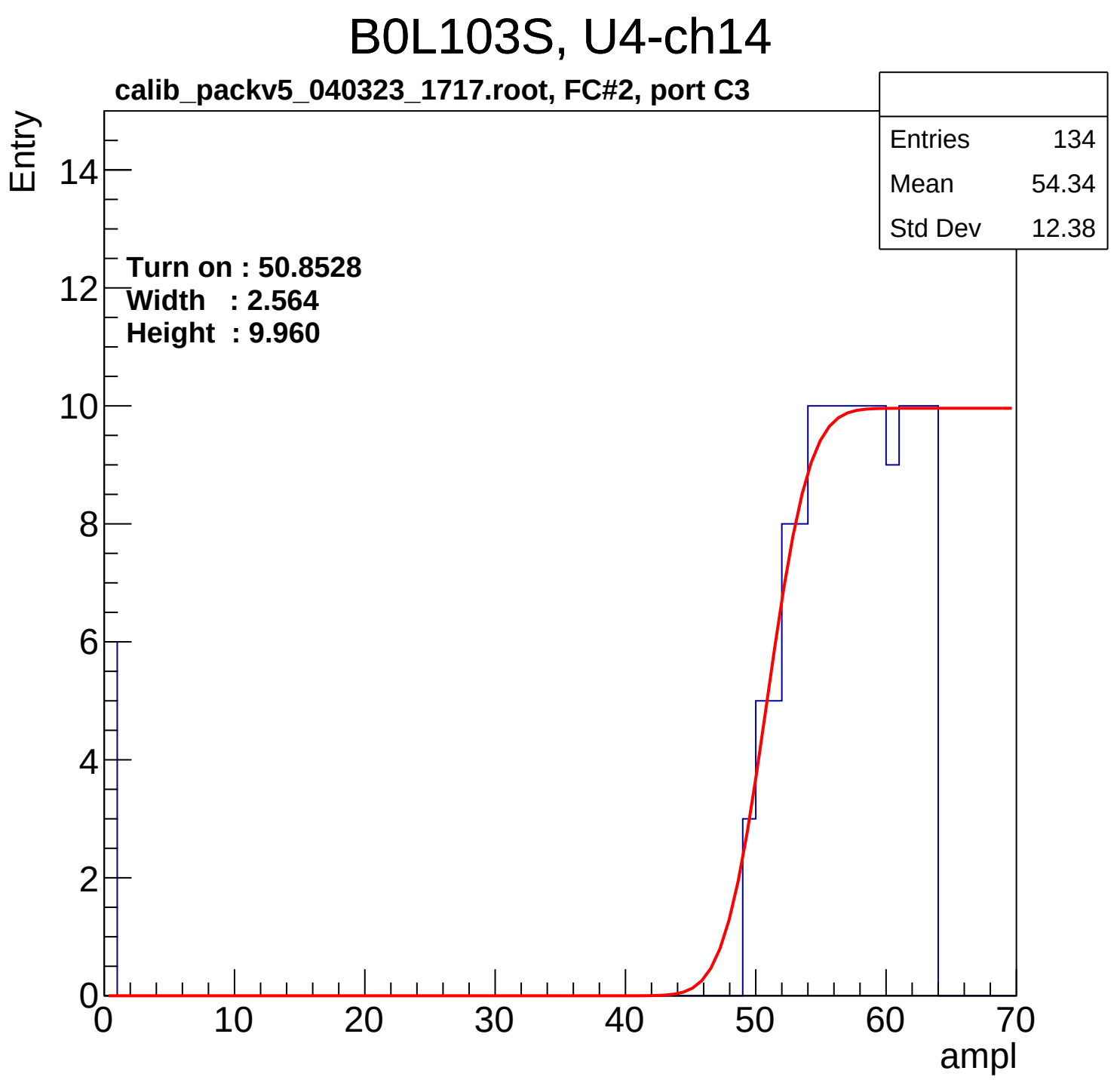
B0L103S, U4-ch14
calib_packv5_040323_1717.root, FC#2, port C3
Entries 134
Mean 54.34
Std Dev 12.38
Turn on : 50.8528
Width : 2.564
Height : 9.960
Entry
ampl
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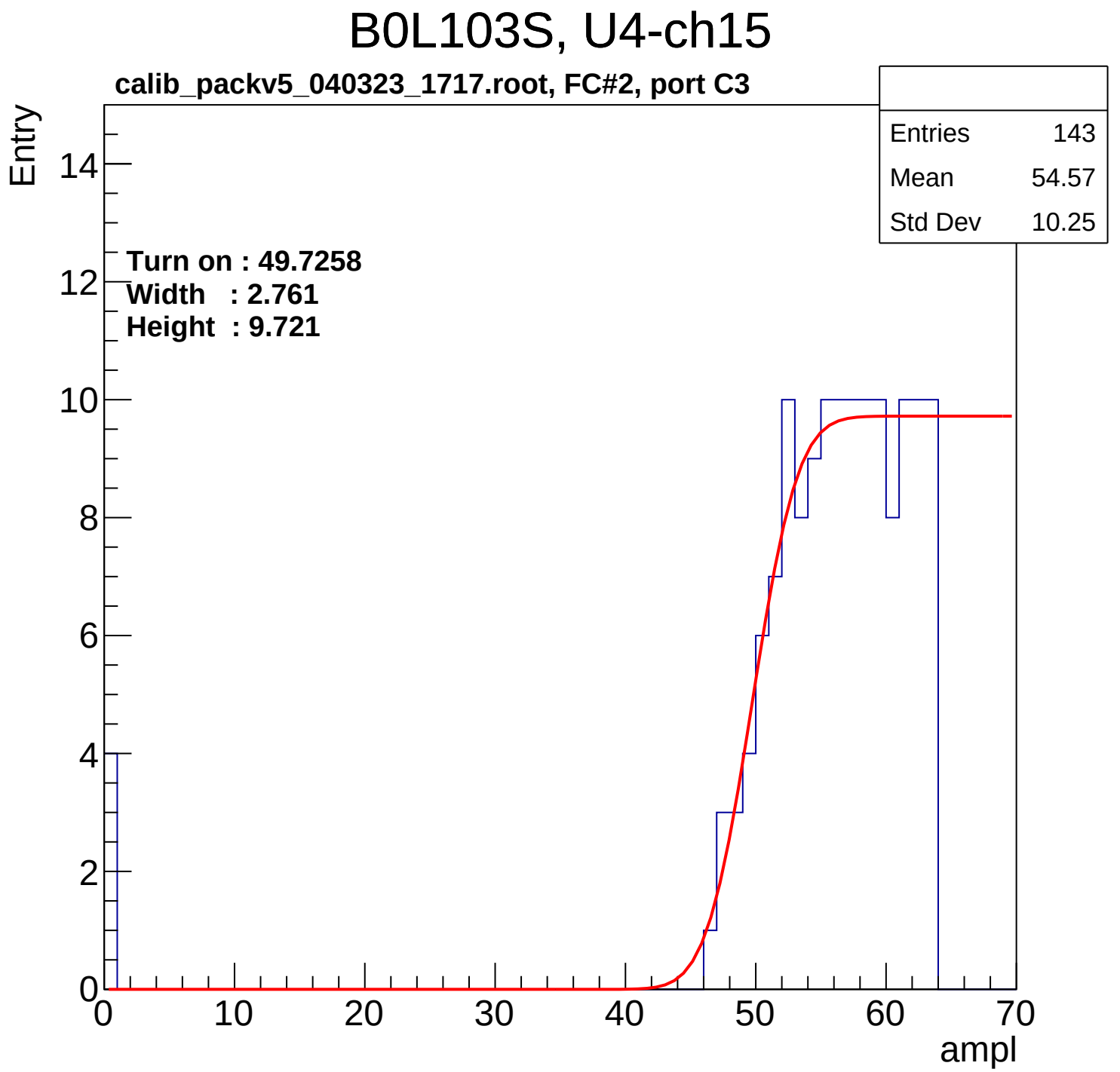
B0L103S, U4-ch15
calib_packv5_040323_1717.root, FC#2, port C3
Entries 143
Mean 54.57
Std Dev 10.25
Turn on : 49.7258
Width : 2.761
Height : 9.721
Entry
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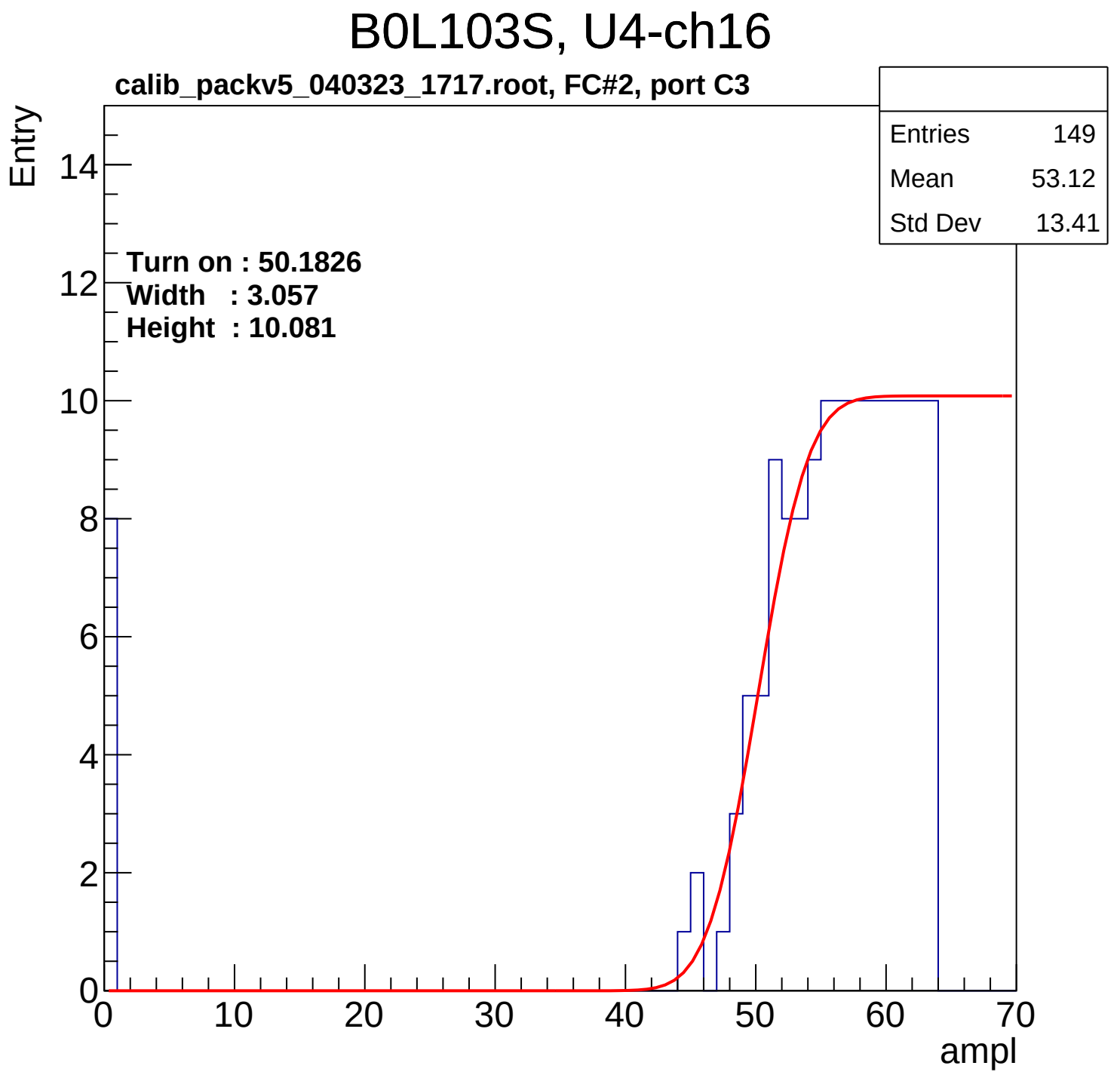
B0L103S, U4-ch16
calib_packv5_040323_1717.root, FC#2, port C3
Entries 149
Mean 53.12
Std Dev 13.41
Turn on : 50.1826
Width : 3.057
Height : 10.081
Entry
ampl
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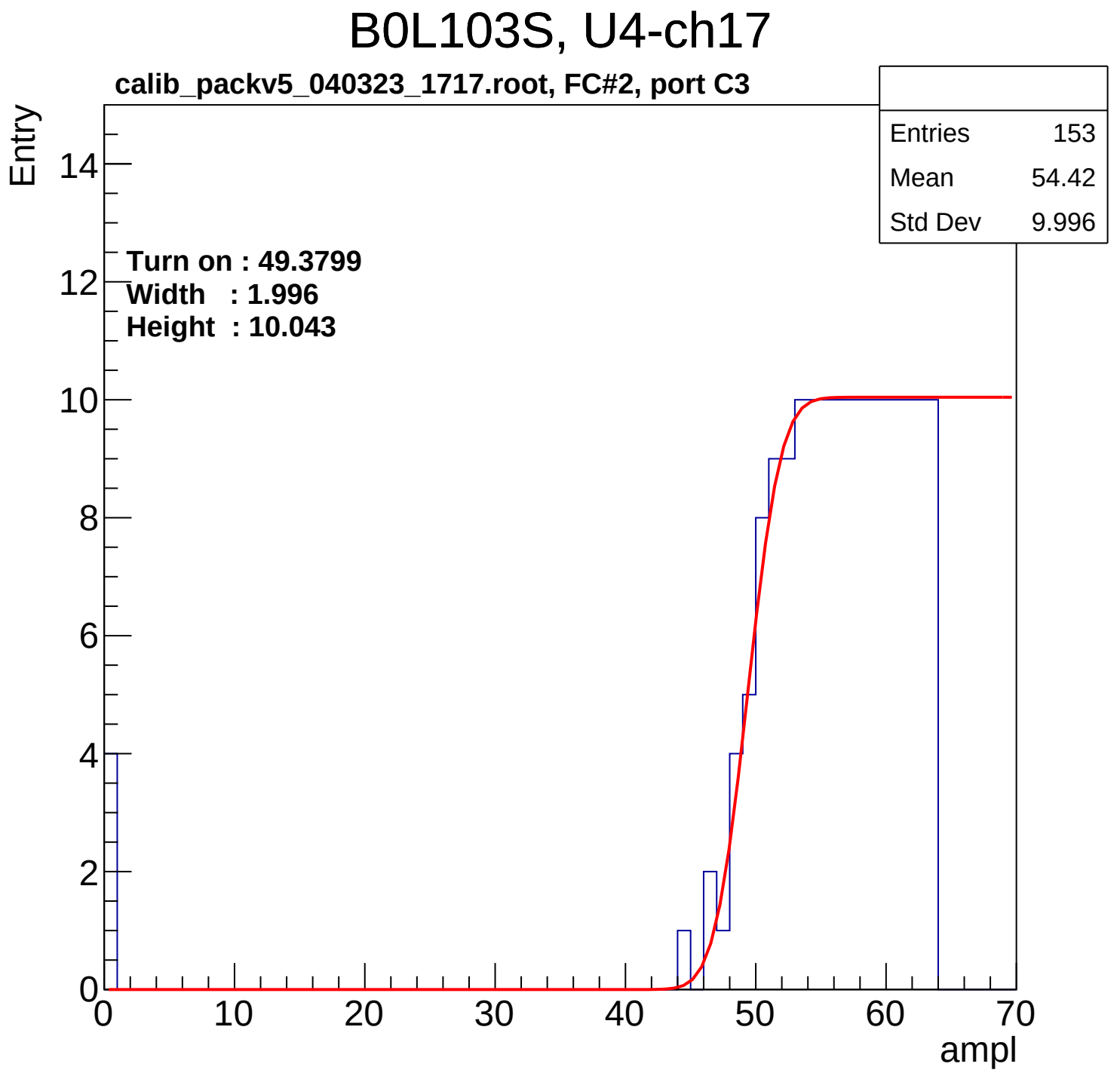
B0L103S, U4-ch17
calib_packv5_040323_1717.root, FC#2, port C3
Entries 153
Mean 54.42
Std Dev 9.996
Turn on : 49.3799
Width : 1.996
Height : 10.043
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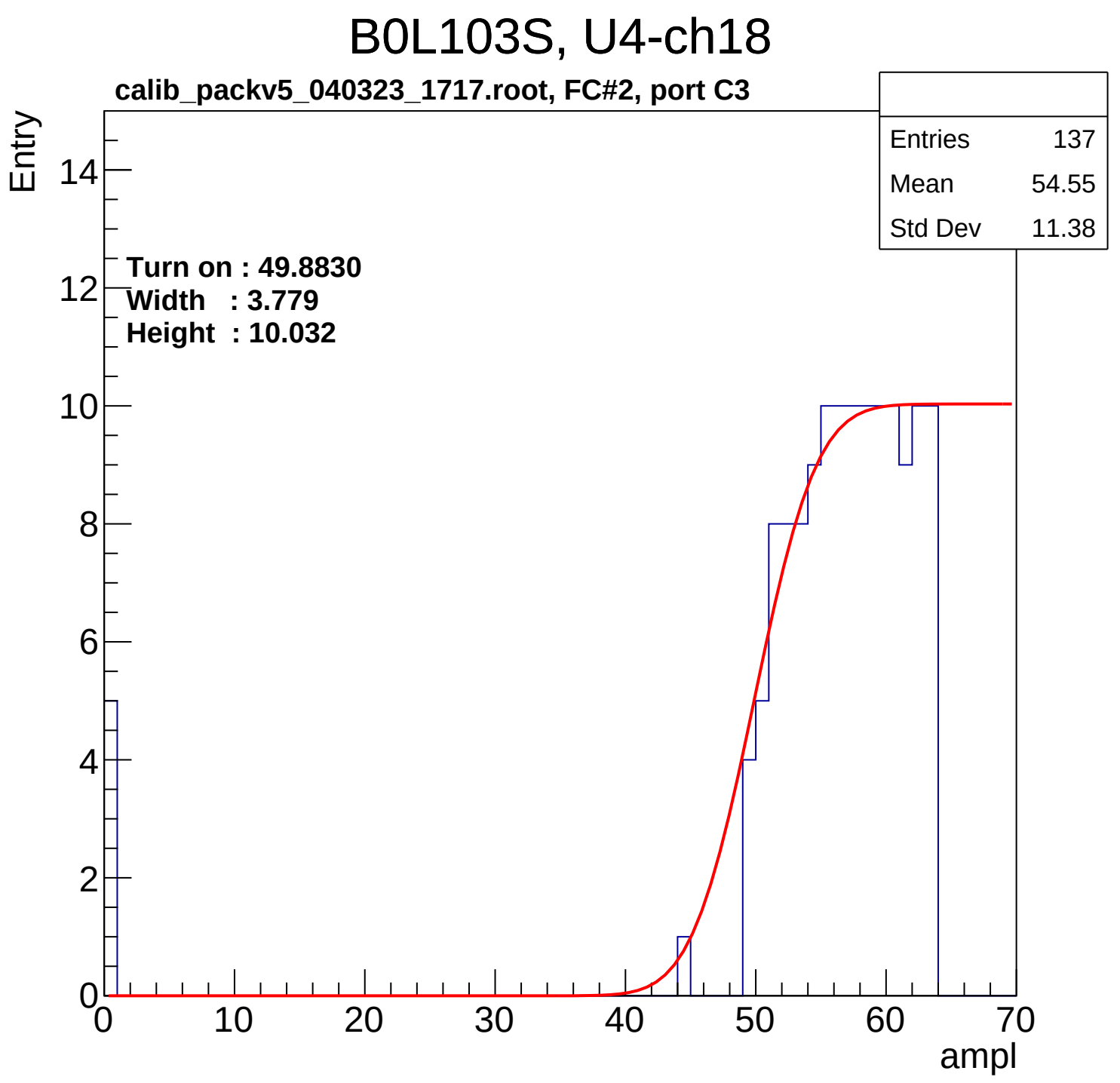
B0L103S, U4-ch18
calib_packv5_040323_1717.root, FC#2, port C3
Entries 137
Mean 54.55
Std Dev 11.38
Turn on : 49.8830
Width : 3.779
Height : 10.032
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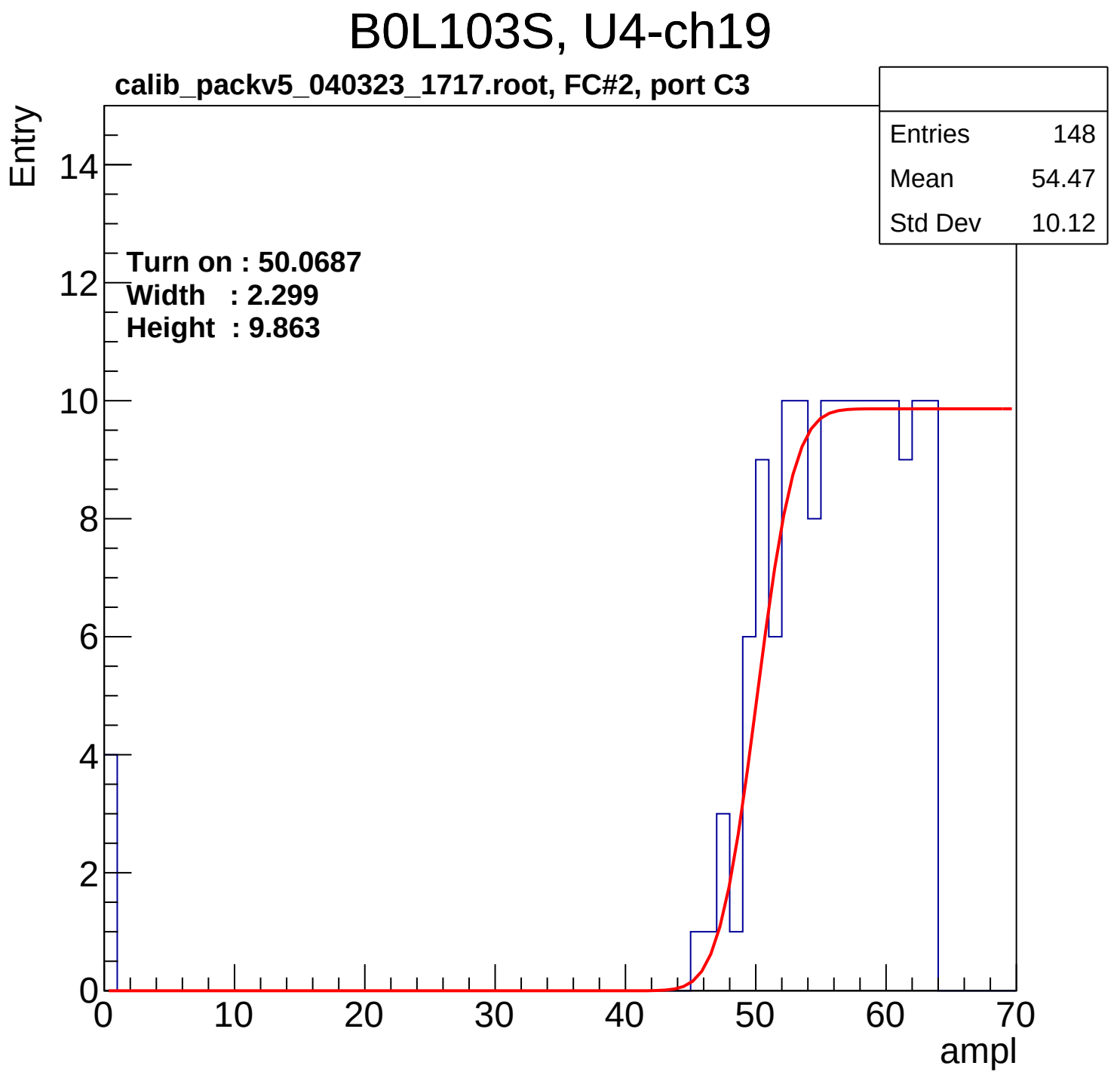
B0L103S, U4-ch19
calib_packv5_040323_1717.root, FC#2, port C3
Entries 148
Mean 54.47
Std Dev 10.12
Turn on : 50.0687
Width : 2.299
Height : 9.863
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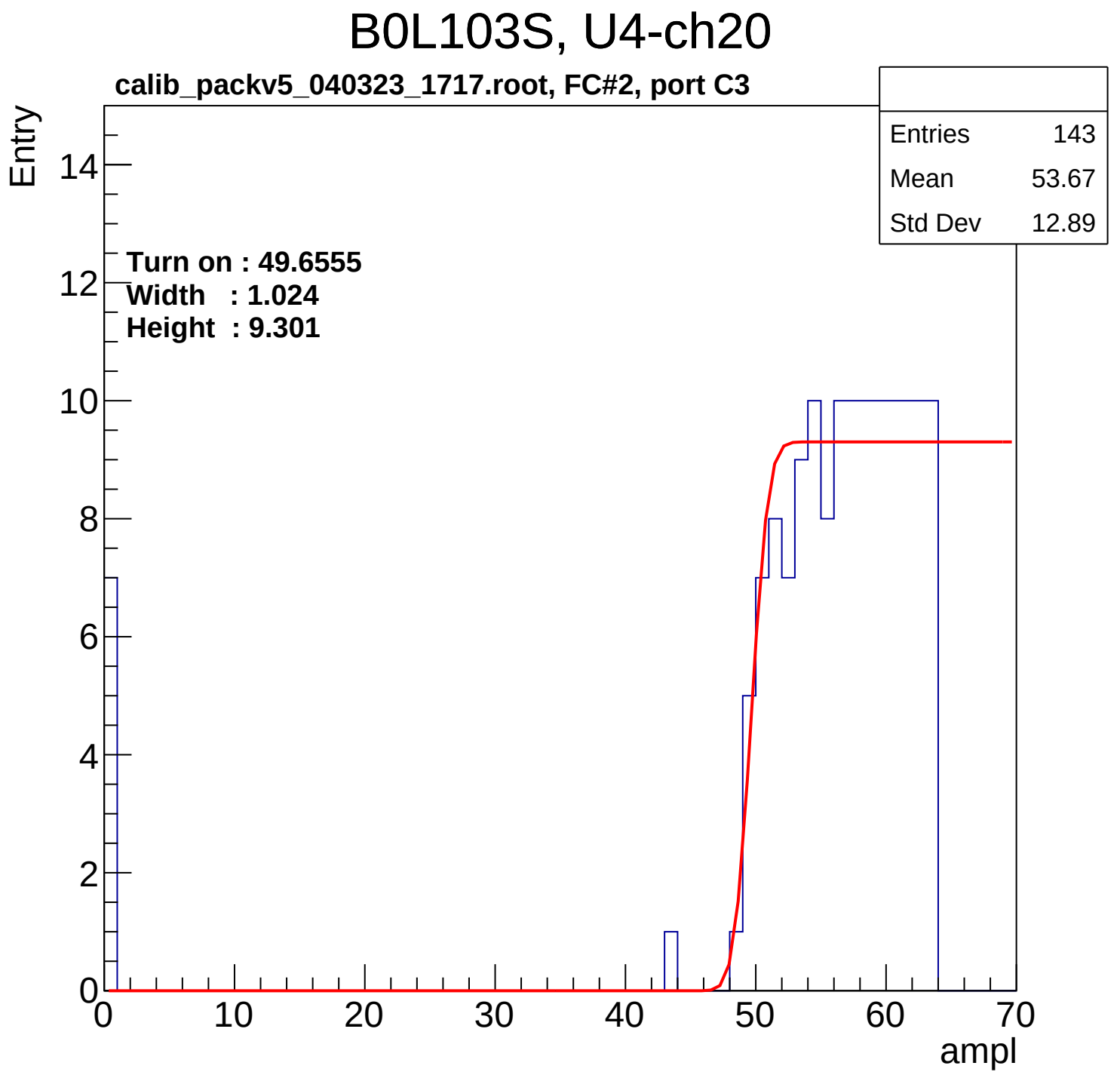
B0L103S, U4-ch20
calib_packv5_040323_1717.root, FC#2, port C3
Entries 143
Mean 53.67
Std Dev 12.89
Turn on : 49.6555
Width : 1.024
Height : 9.301
Entry
ampl
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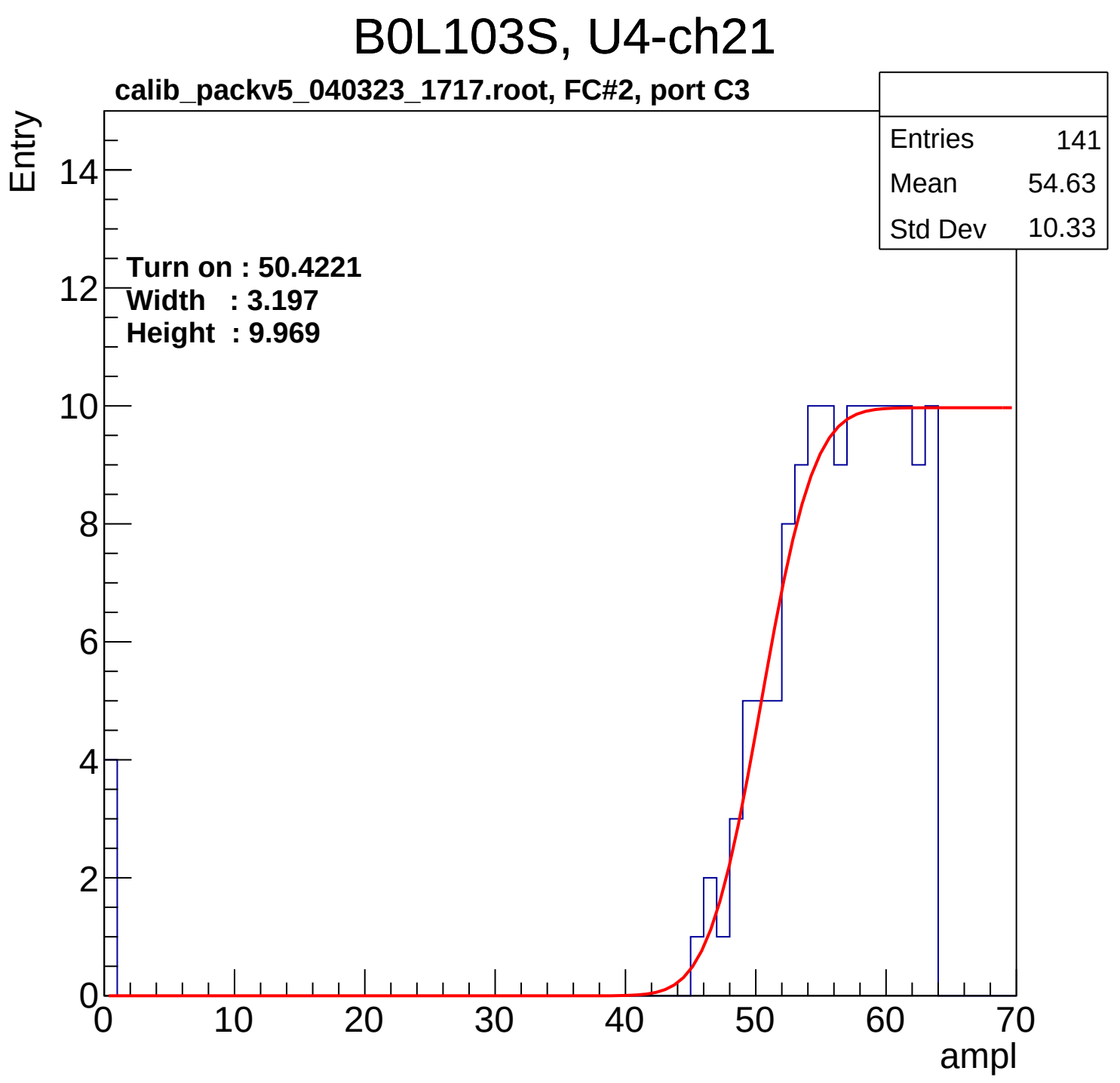
B0L103S, U4-ch21
calib_packv5_040323_1717.root, FC#2, port C3
Entries 141
Mean 54.63
Std Dev 10.33
Turn on : 50.4221
Width : 3.197
Height : 9.969
Entry
ampl
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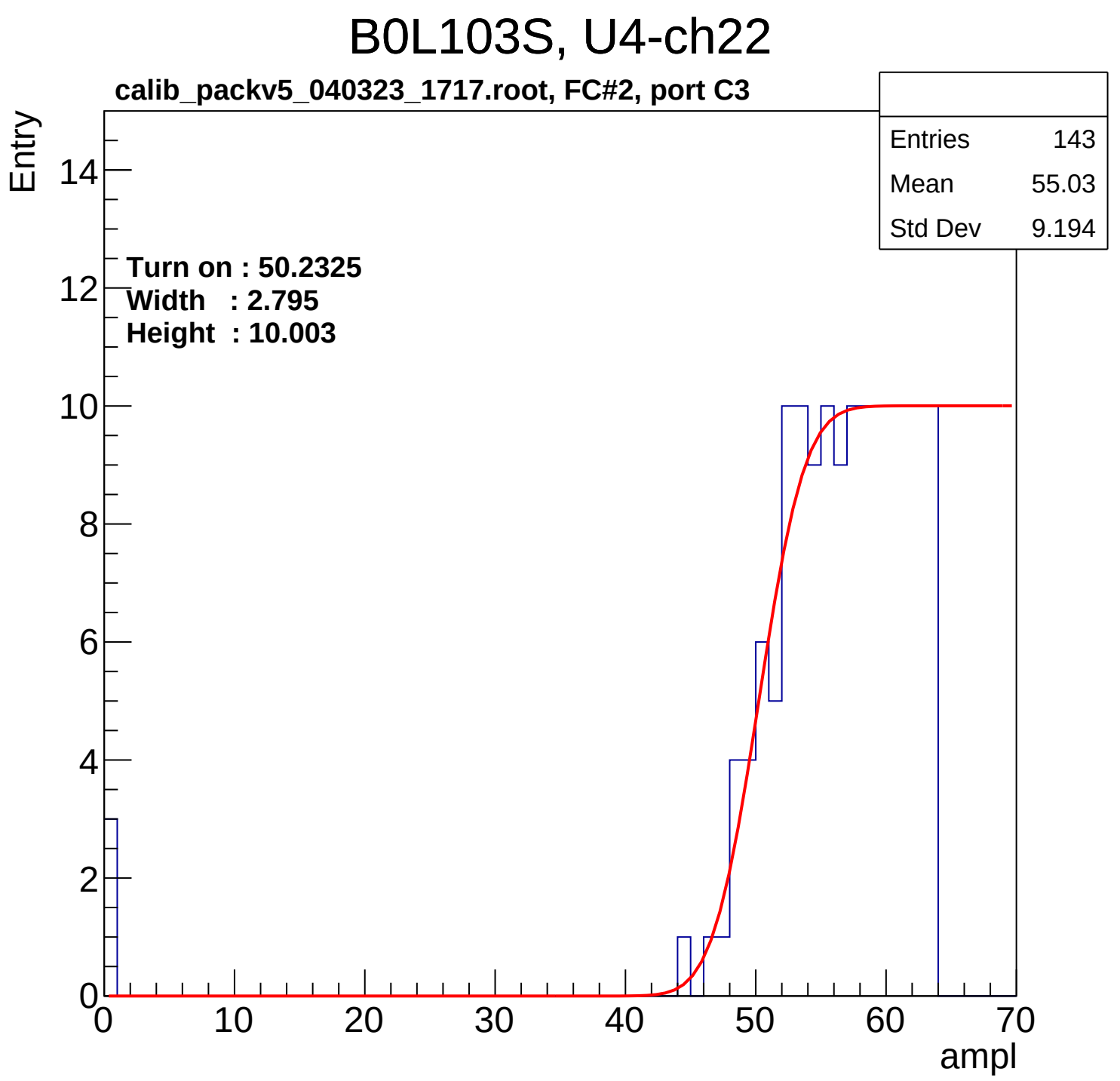
B0L103S, U4-ch22
calib_packv5_040323_1717.root, FC#2, port C3
Entries 143
Mean 55.03
Std Dev 9.194
Turn on : 50.2325
Width : 2.795
Height : 10.003
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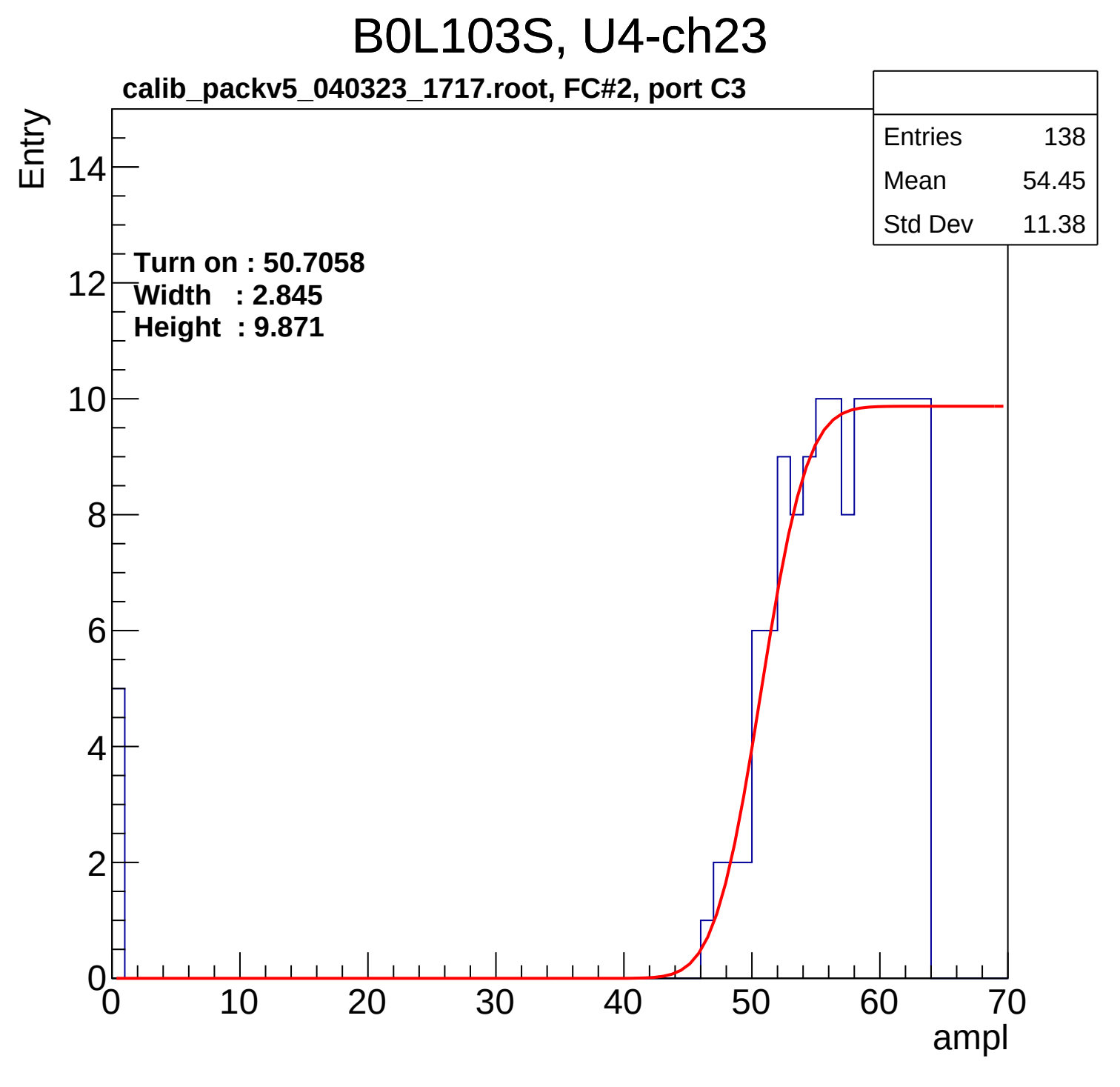
B0L103S, U4-ch23
calib_packv5_040323_1717.root, FC#2, port C3
Entries 138
Mean 54.45
Std Dev 11.38
Turn on : 50.7058
Width : 2.845
Height : 9.871
Entry
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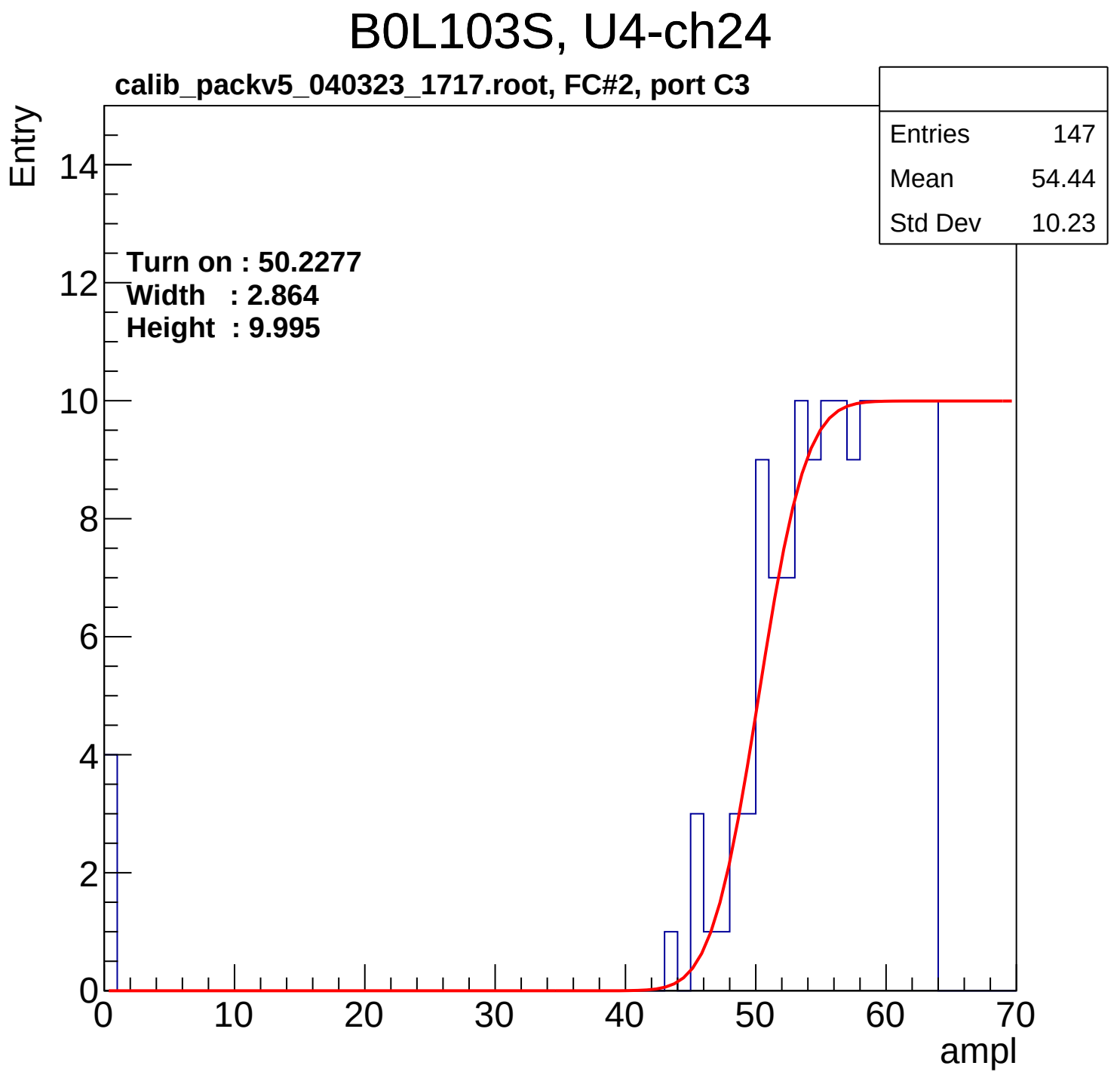
B0L103S, U4-ch24
calib_packv5_040323_1717.root, FC#2, port C3
Entries 147
Mean 54.44
Std Dev 10.23
Turn on : 50.2277
Width : 2.864
Height : 9.995
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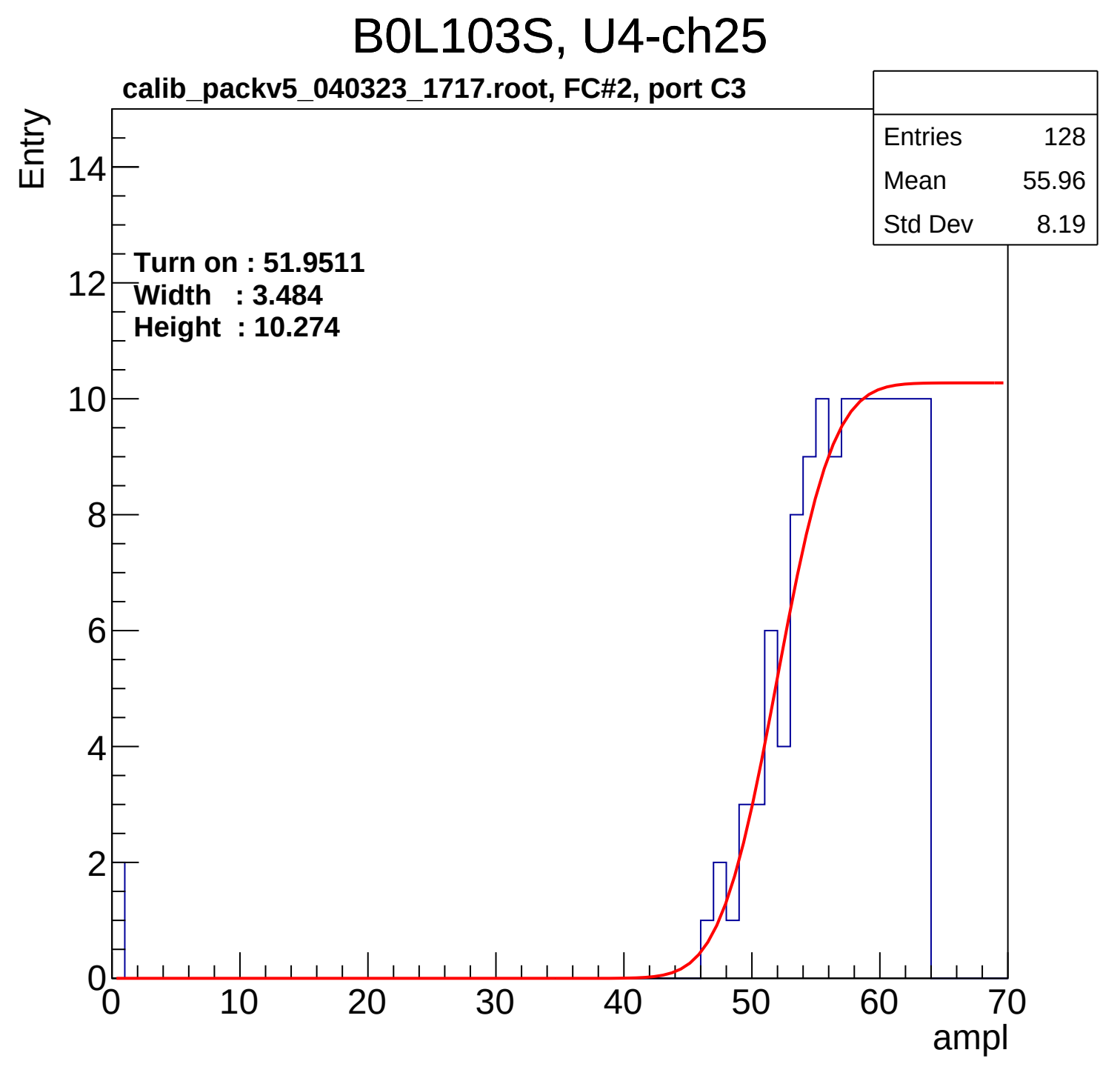
B0L103S, U4-ch25
calib_packv5_040323_1717.root, FC#2, port C3
Entries 128
Mean 55.96
Std Dev 8.19
Turn on : 51.9511
Width : 3.484
Height : 10.274
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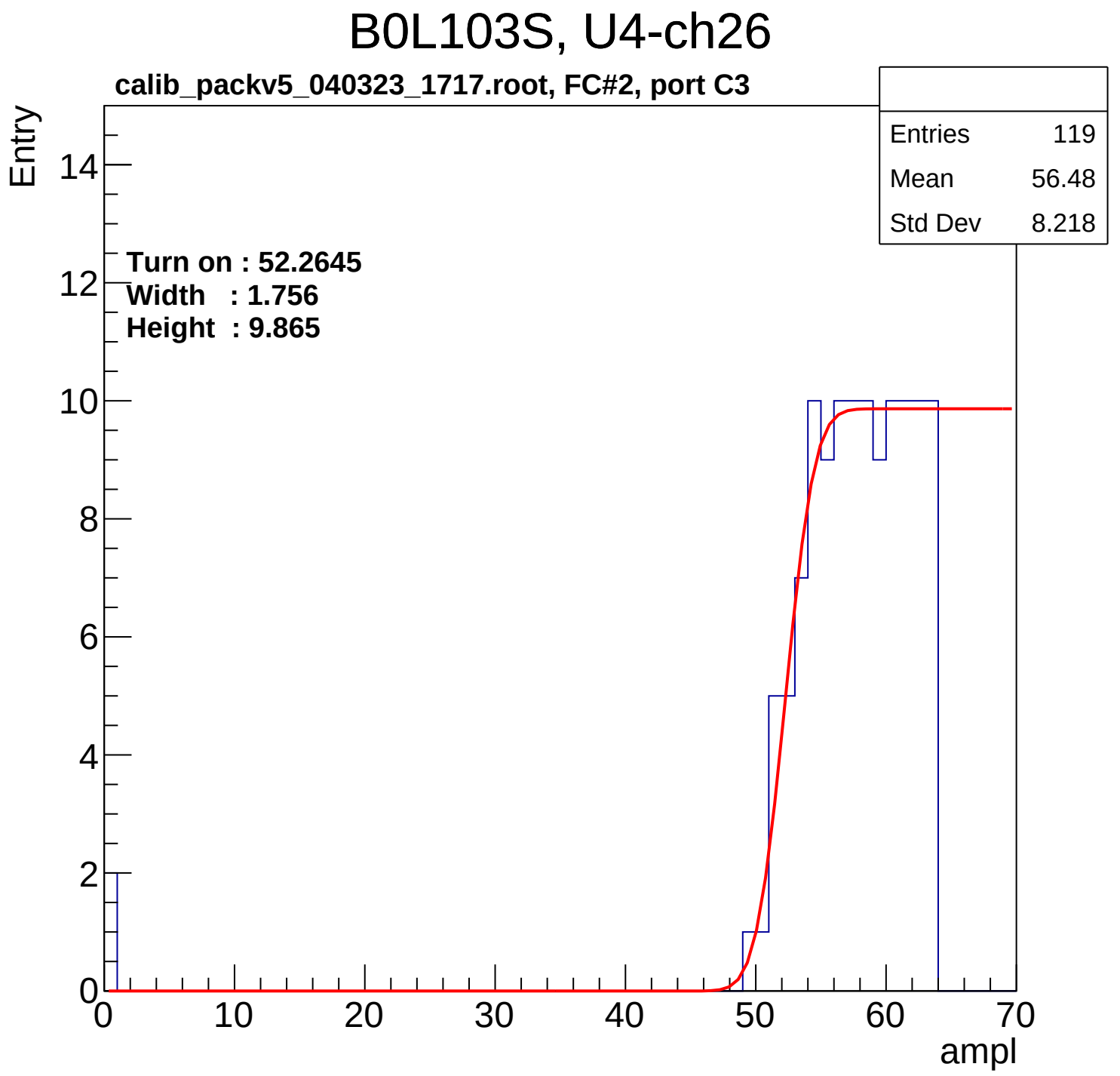
B0L103S, U4-ch26
calib_packv5_040323_1717.root, FC#2, port C3
Entries 119
Mean 56.48
Std Dev 8.218
Turn on : 52.2645
Width : 1.756
Height : 9.865
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ampl
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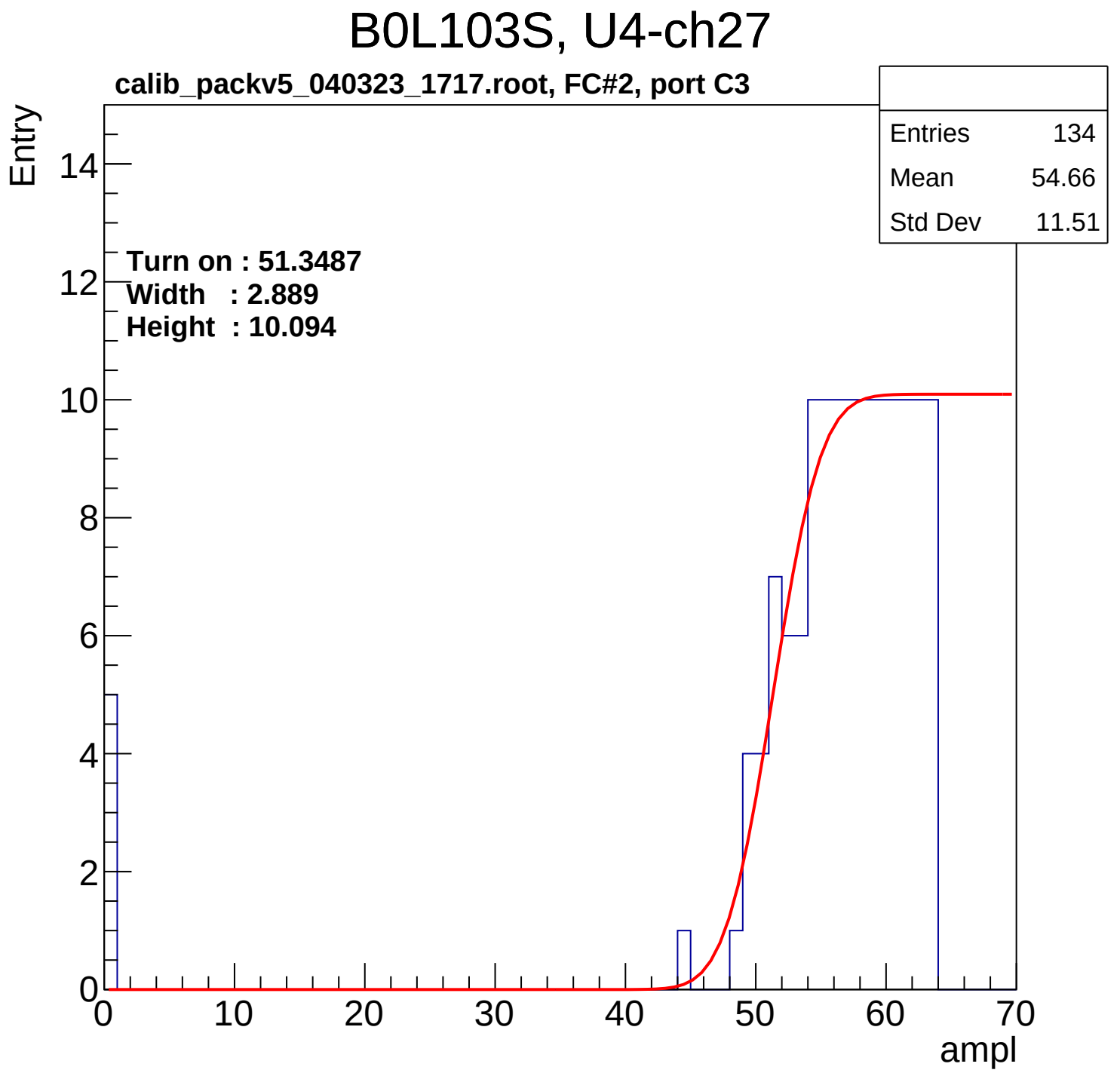
B0L103S, U4-ch27
calib_packv5_040323_1717.root, FC#2, port C3
Entries 134
Mean 54.66
Std Dev 11.51
Turn on : 51.3487
Width : 2.889
Height : 10.094
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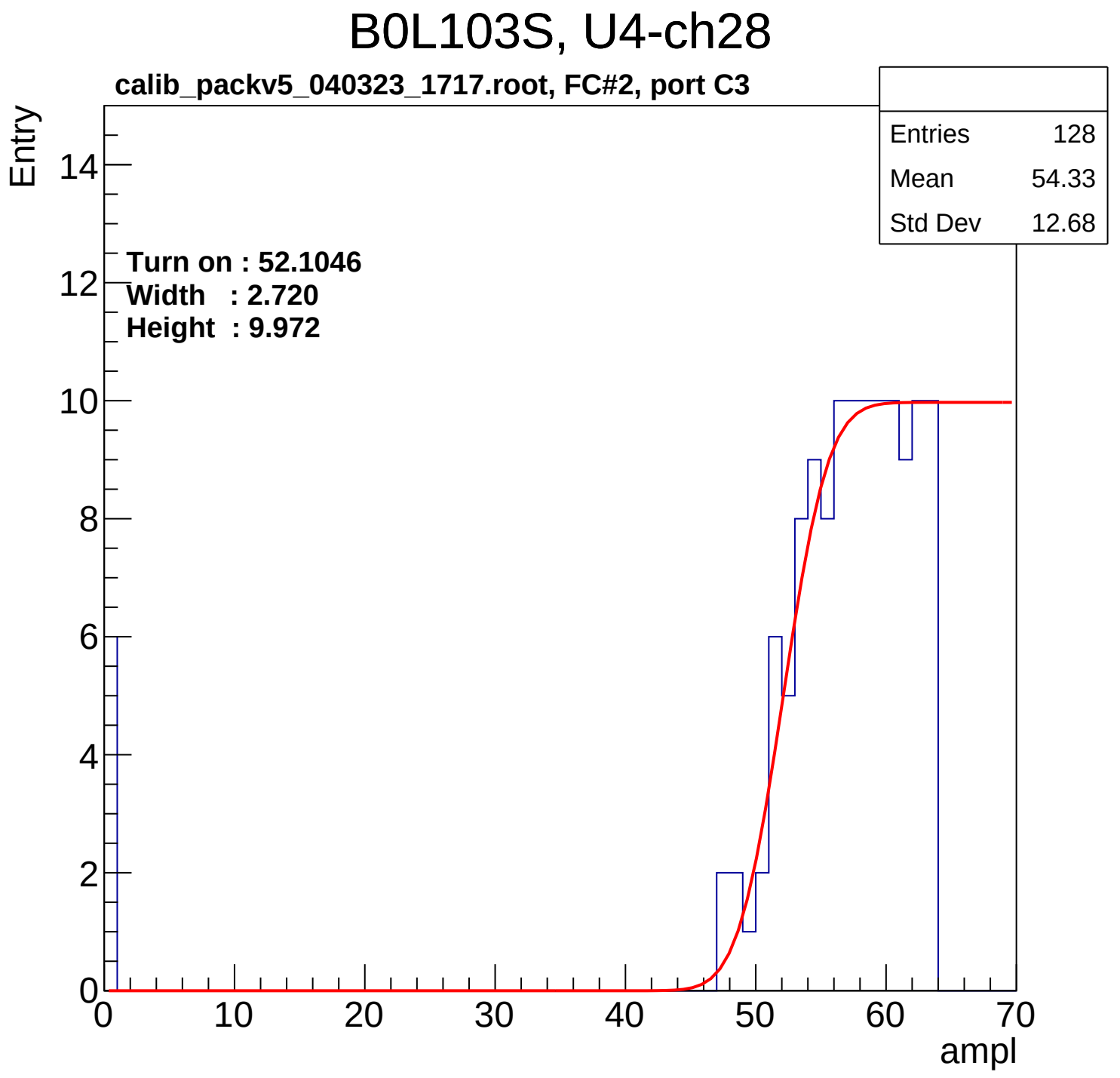
B0L103S, U4-ch28
calib_packv5_040323_1717.root, FC#2, port C3
Entries 128
Mean 54.33
Std Dev 12.68
Turn on : 52.1046
Width : 2.720
Height : 9.972
Entry
ampl
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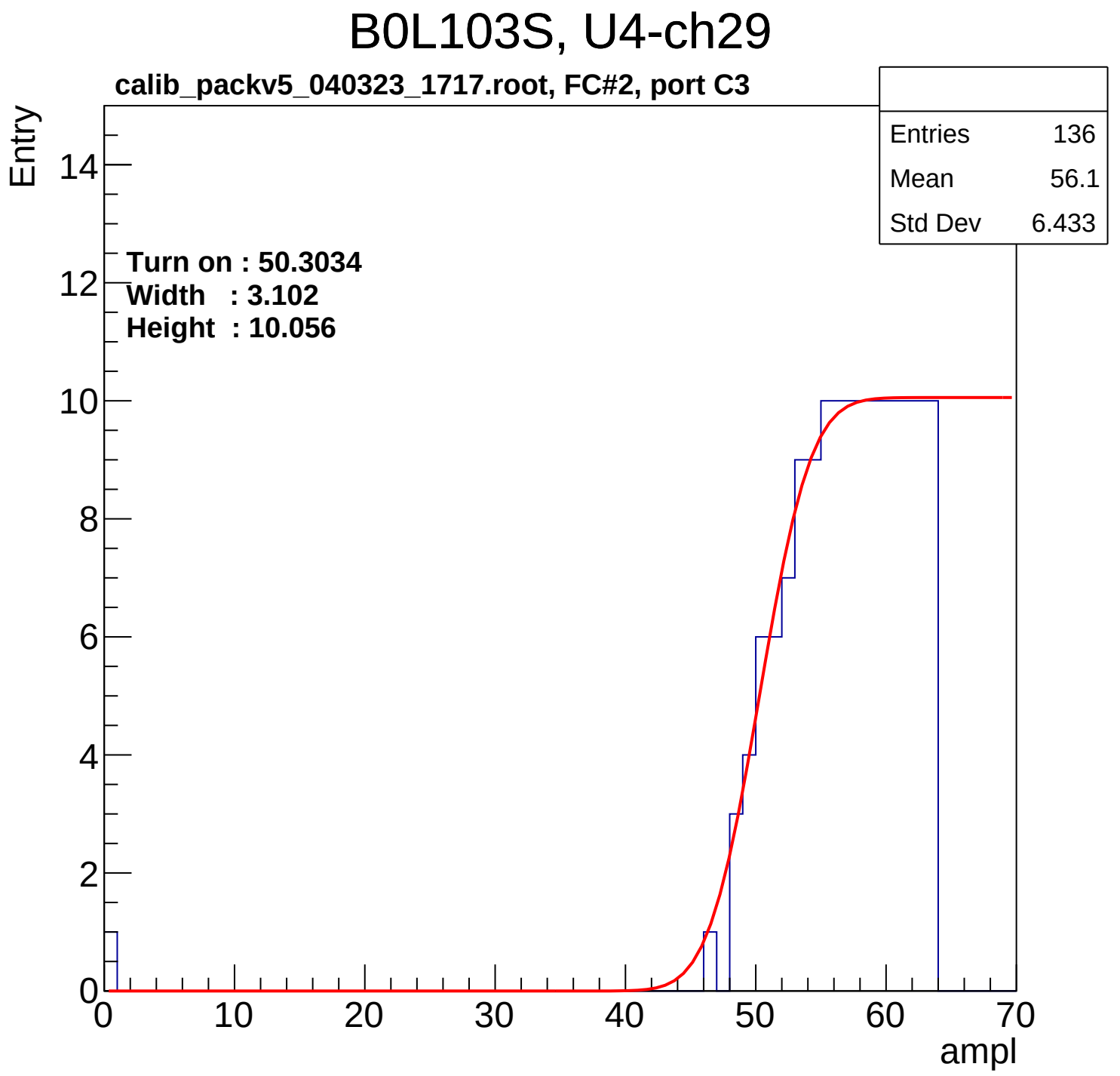
B0L103S, U4-ch29
calib_packv5_040323_1717.root, FC#2, port C3
Entries 136
Mean 56.1
Std Dev 6.433
Turn on : 50.3034
Width : 3.102
Height : 10.056
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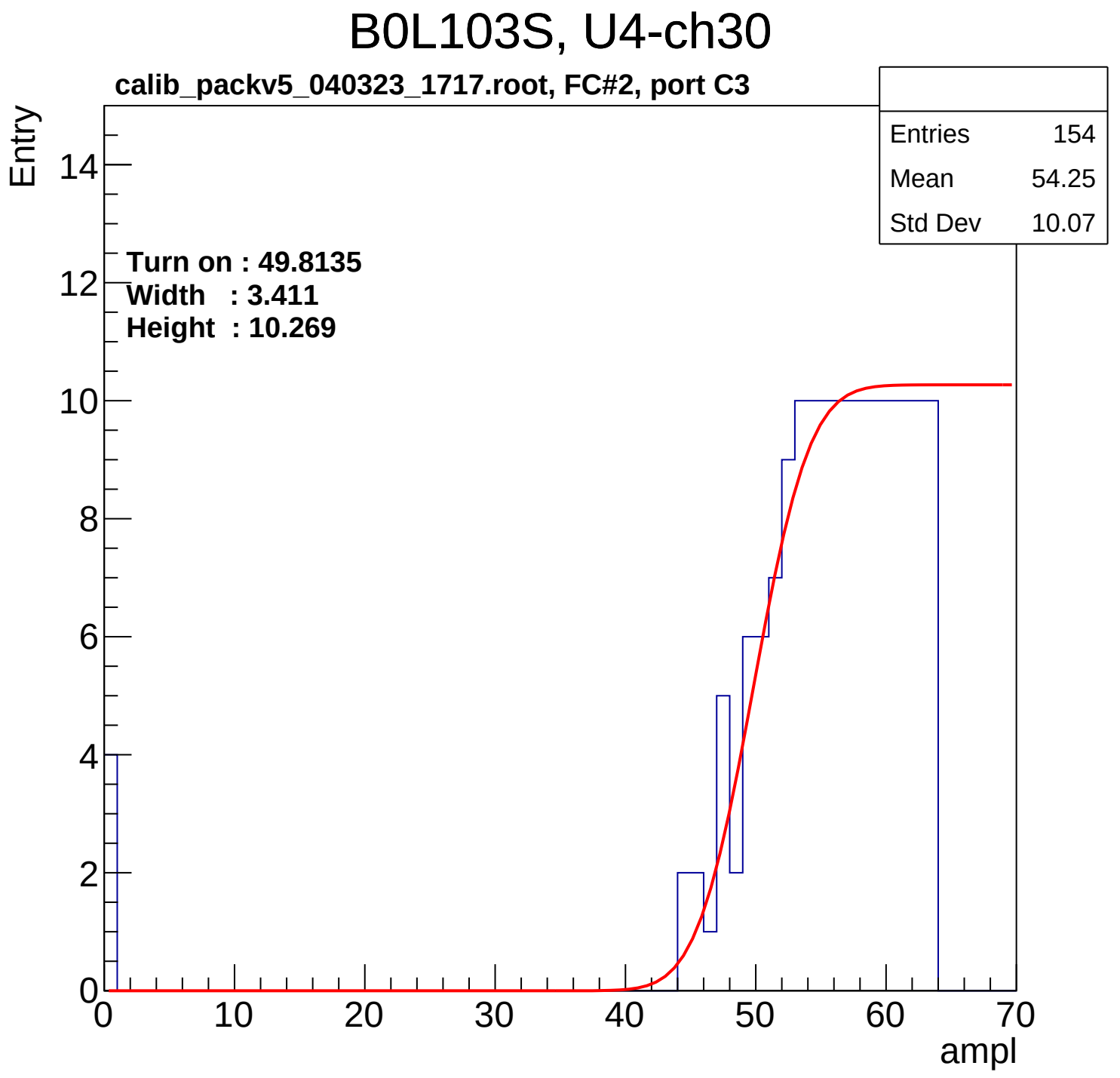
B0L103S, U4-ch30
calib_packv5_040323_1717.root, FC#2, port C3
Entries 154
Mean 54.25
Std Dev 10.07
Turn on : 49.8135
Width : 3.411
Height : 10.269
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ampl
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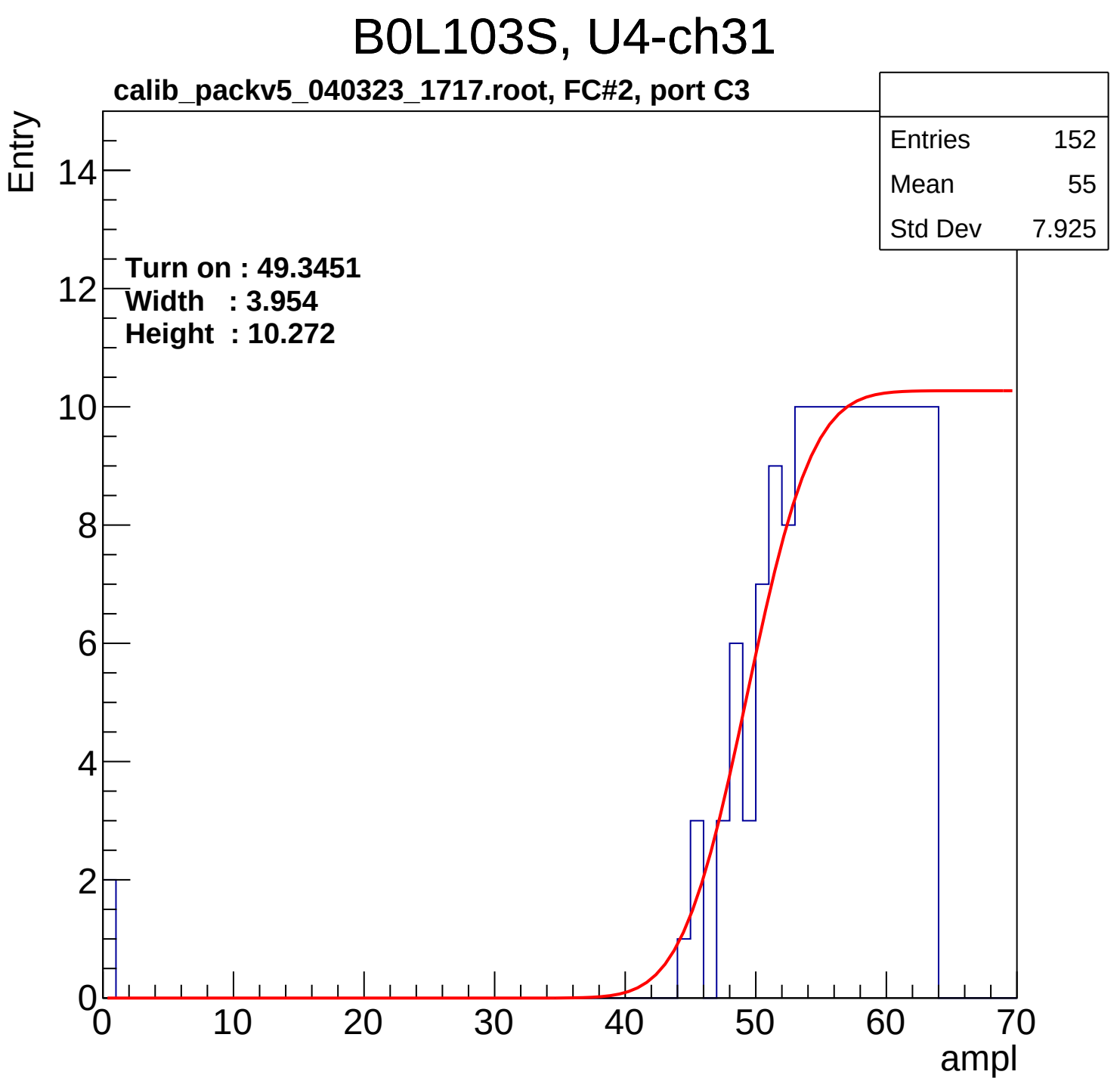
B0L103S, U4-ch31
calib_packv5_040323_1717.root, FC#2, port C3
Entries 152
Mean 55
Std Dev 7.925
Turn on : 49.3451
Width : 3.954
Height : 10.272
Entry
ampl
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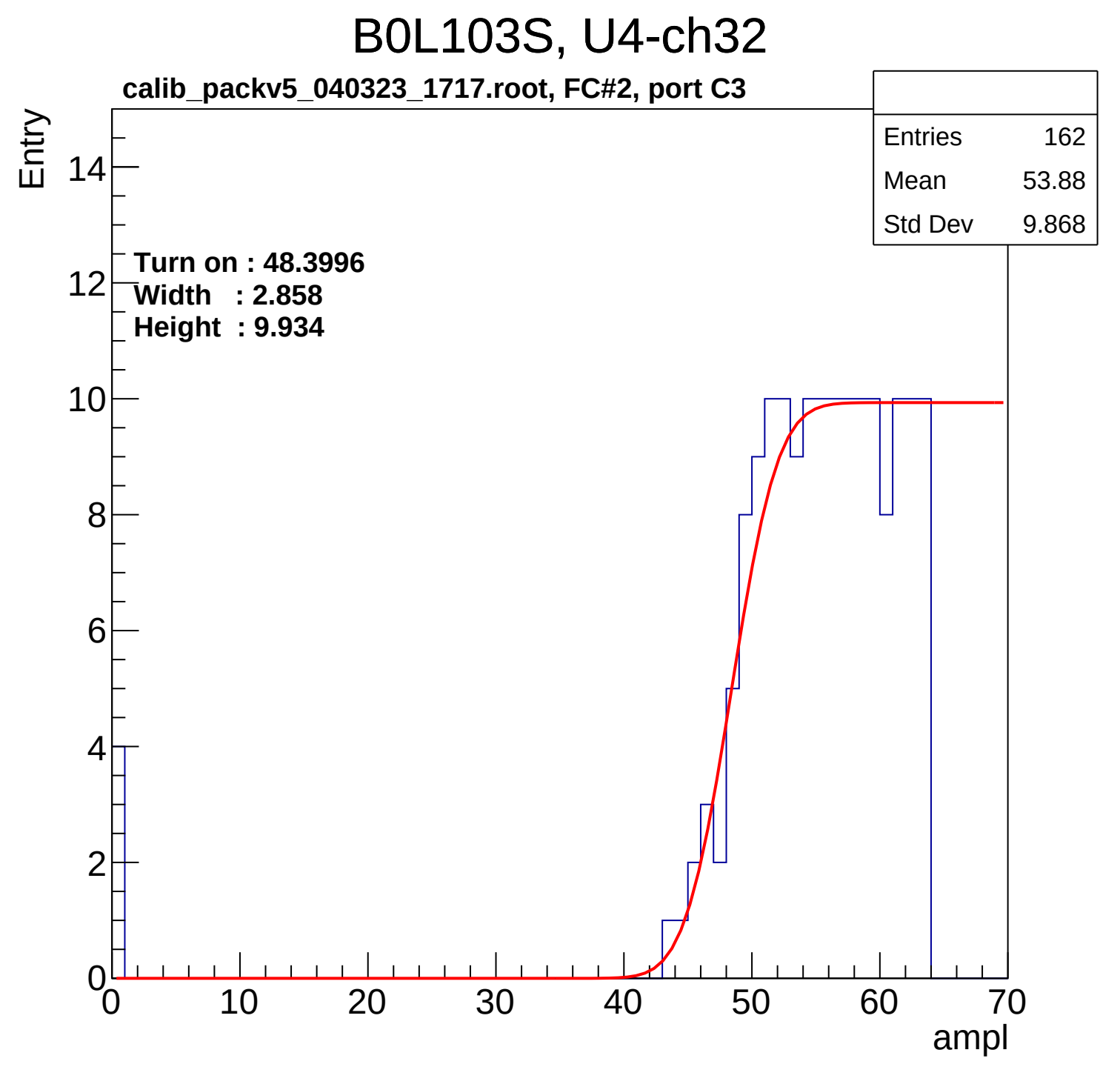
B0L103S, U4-ch32
calib_packv5_040323_1717.root, FC#2, port C3
Entries 162
Mean 53.88
Std Dev 9.868
Turn on : 48.3996
Width : 2.858
Height : 9.934
Entry
ampl
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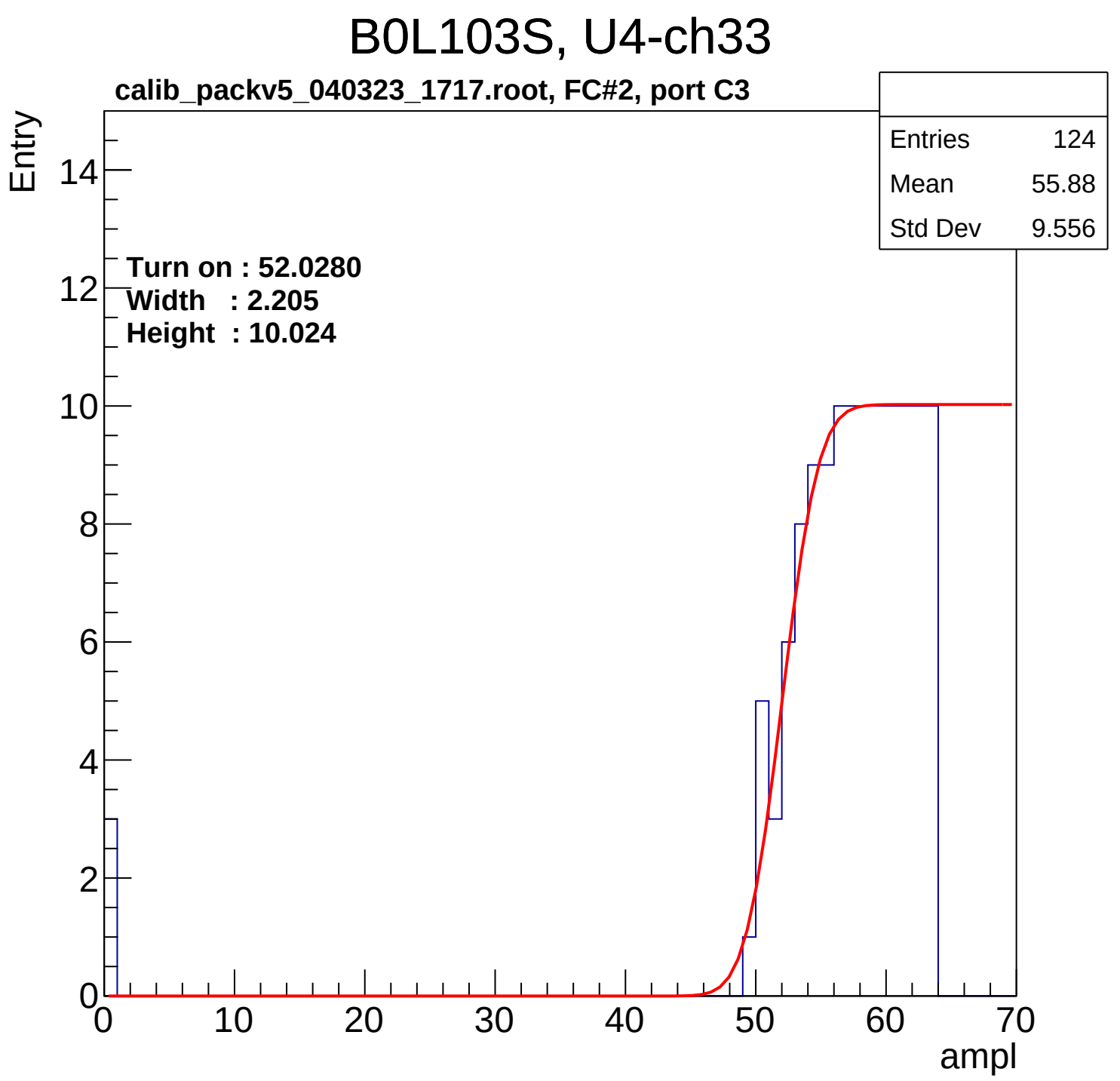
B0L103S, U4-ch33
calib_packv5_040323_1717.root, FC#2, port C3
Entries 124
Mean 55.88
Std Dev 9.556
Turn on : 52.0280
Width : 2.205
Height : 10.024
Entry
ampl
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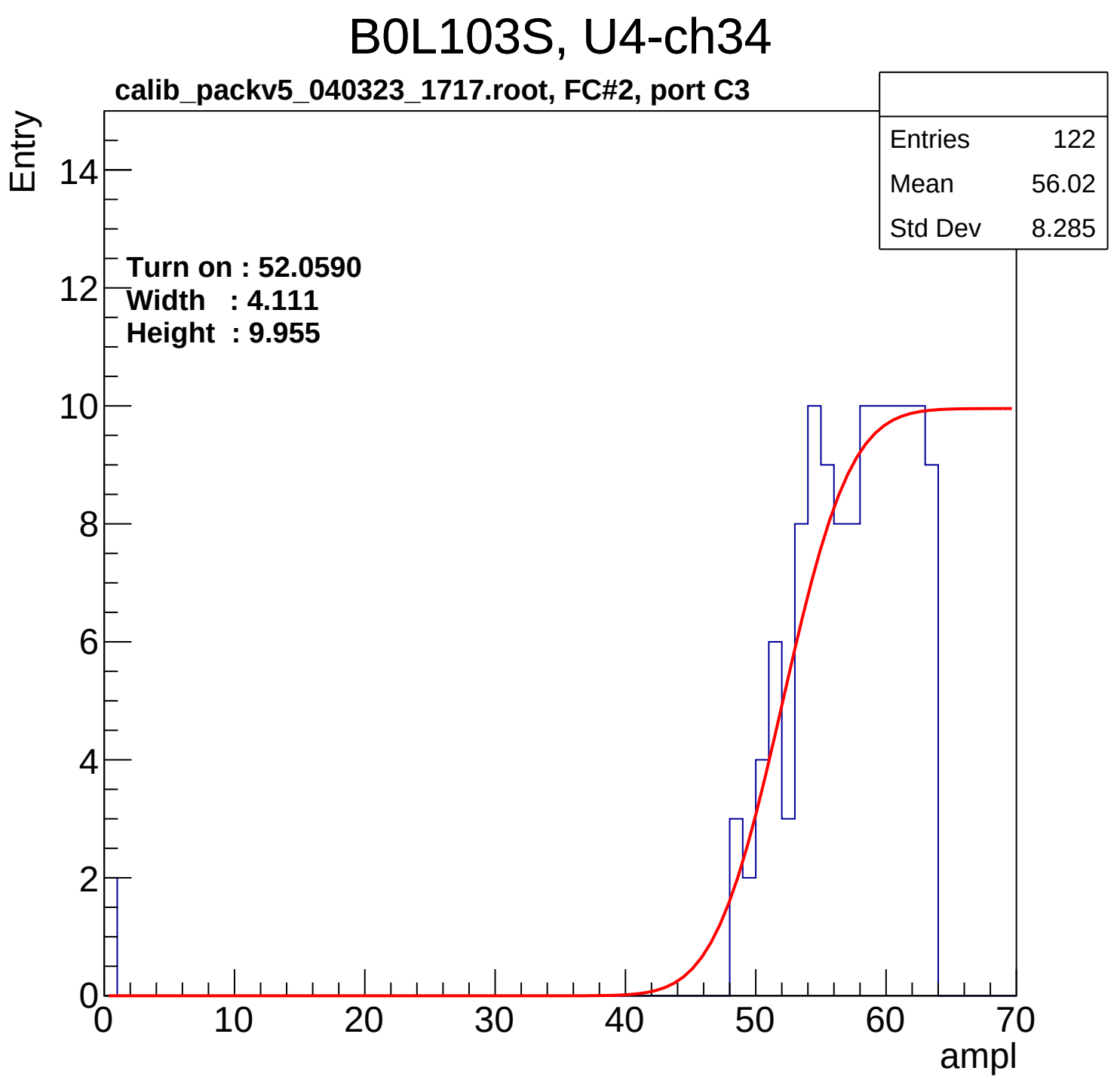
B0L103S, U4-ch34
calib_packv5_040323_1717.root, FC#2, port C3
Entries 122
Mean 56.02
Std Dev 8.285
Turn on : 52.0590
Width : 4.111
Height : 9.955
Entry
ampl
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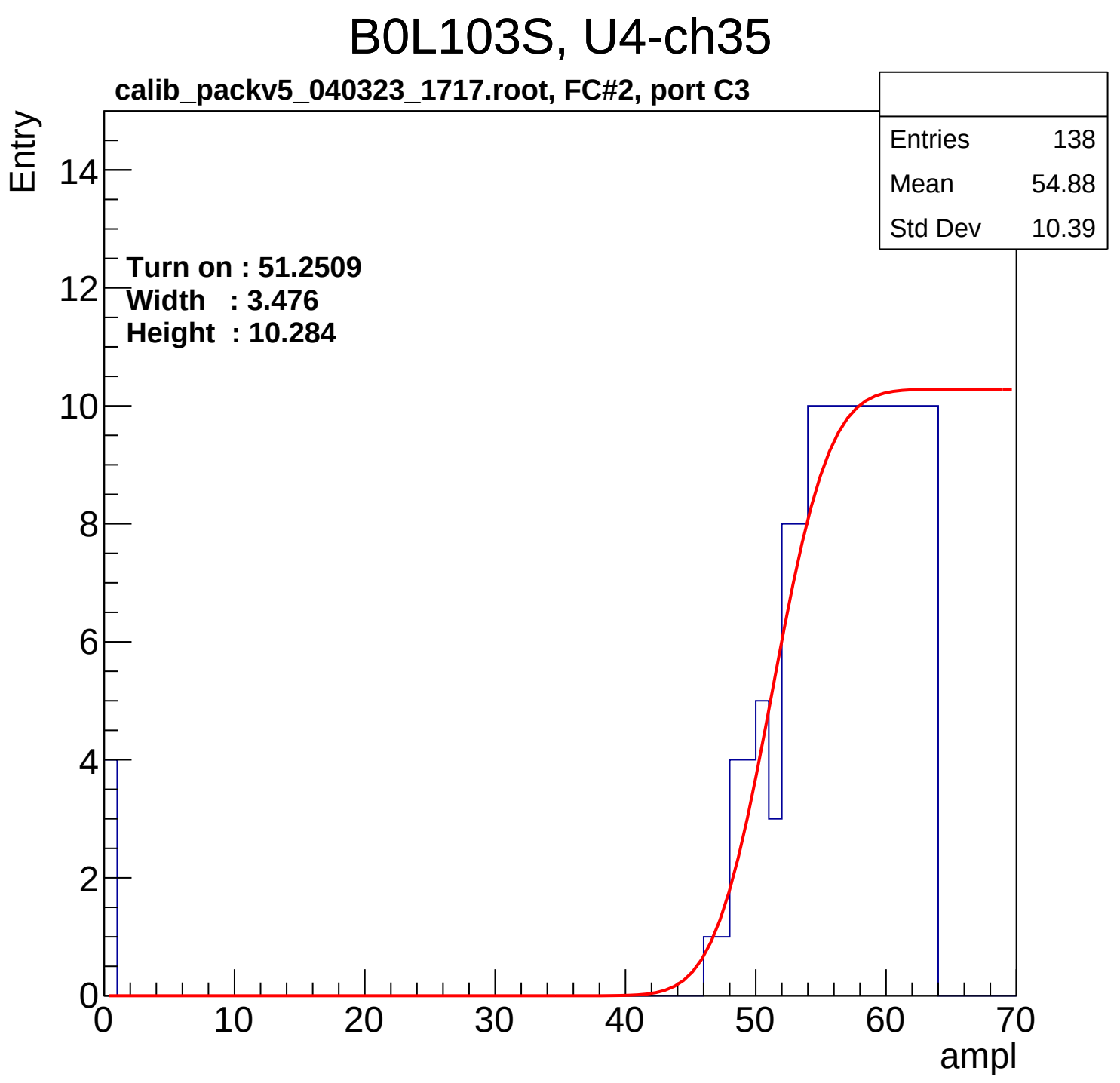
B0L103S, U4-ch35
calib_packv5_040323_1717.root, FC#2, port C3
Entries 138
Mean 54.88
Std Dev 10.39
Turn on : 51.2509
Width : 3.476
Height : 10.284
Entry
ampl
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2
4
6
8
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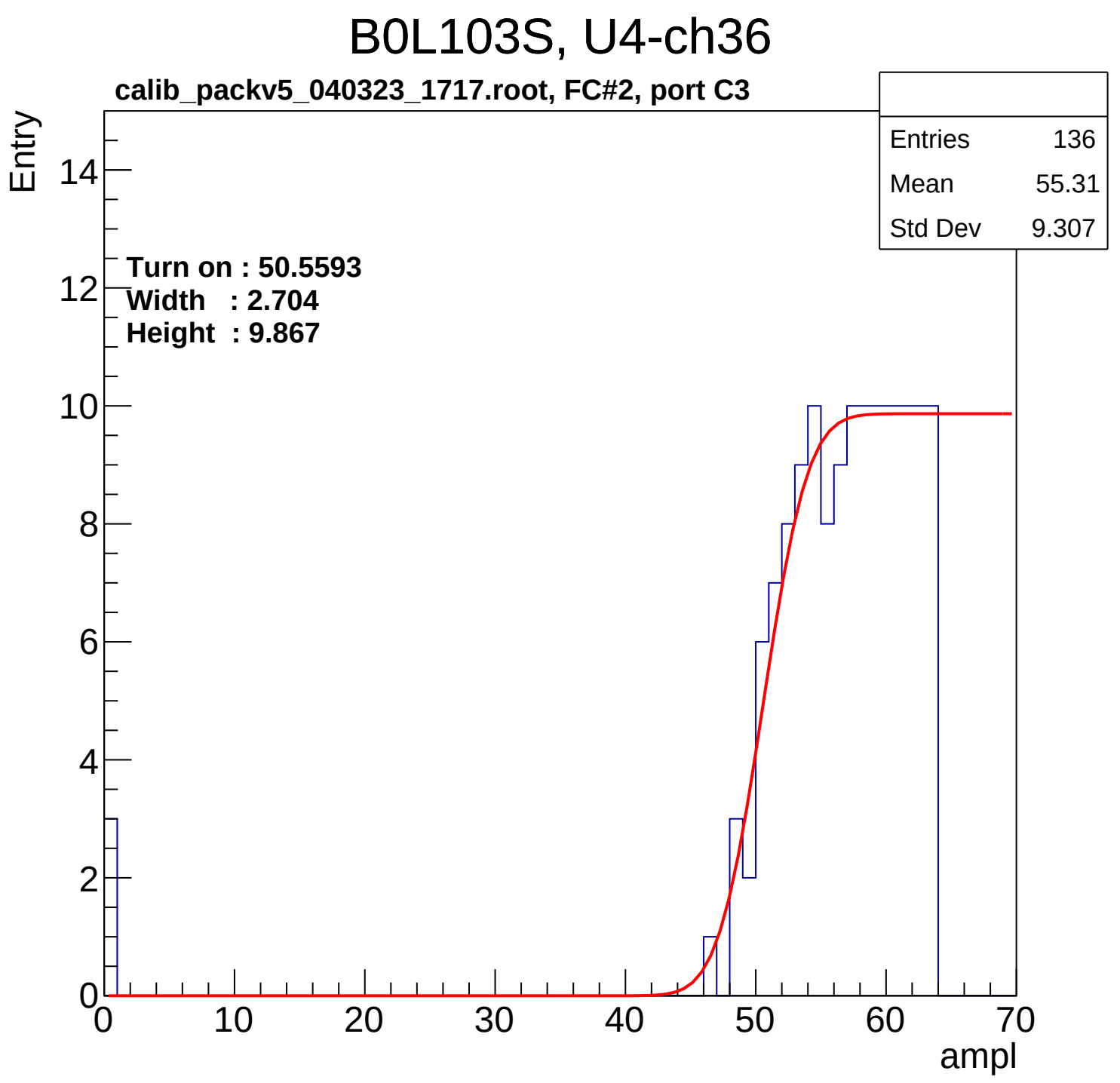
B0L103S, U4-ch36
calib_packv5_040323_1717.root, FC#2, port C3
Entries 136
Mean 55.31
Std Dev 9.307
Turn on : 50.5593
Width : 2.704
Height : 9.867
Entry
ampl
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2
4
6
8
10
12
14
0
10
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60
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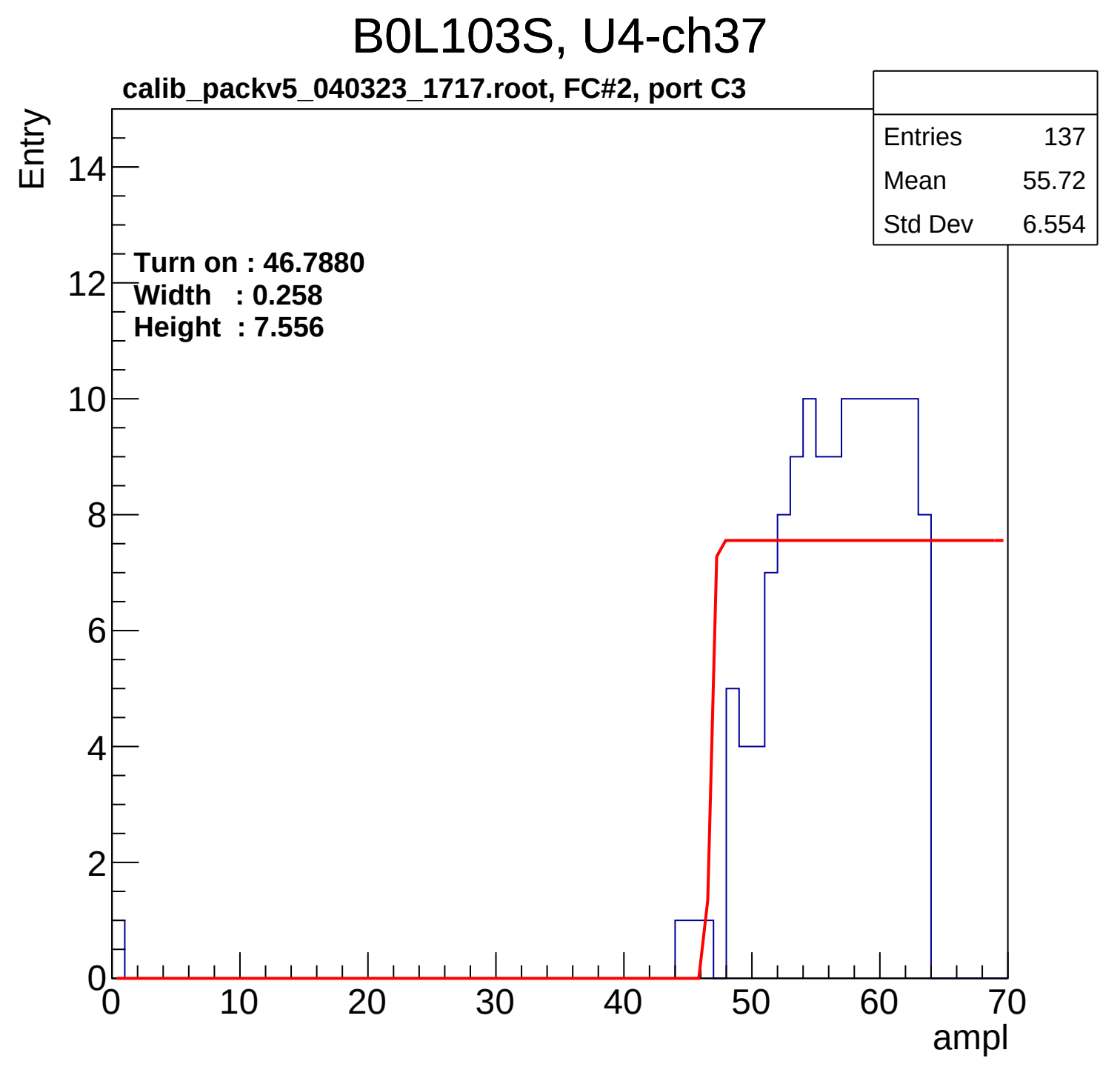
B0L103S, U4-ch37
calib_packv5_040323_1717.root, FC#2, port C3
Entries 137
Mean 55.72
Std Dev 6.554
Turn on : 46.7880
Width : 0.258
Height : 7.556
Entry
ampl
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4
6
8
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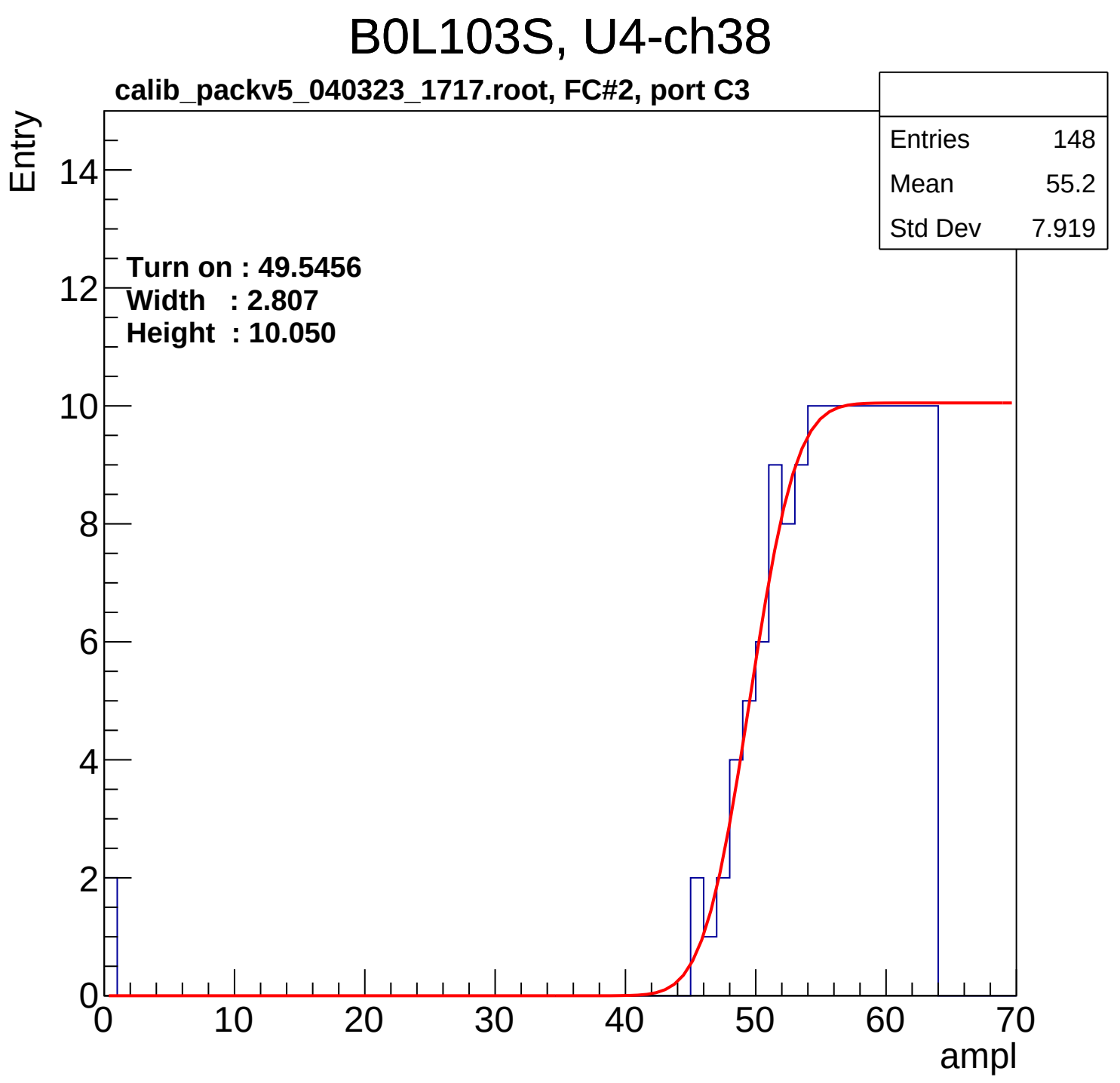
B0L103S, U4-ch38
calib_packv5_040323_1717.root, FC#2, port C3
Entries 148
Mean 55.2
Std Dev 7.919
Turn on : 49.5456
Width : 2.807
Height : 10.050
Entry
ampl
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2
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6
8
10
12
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60
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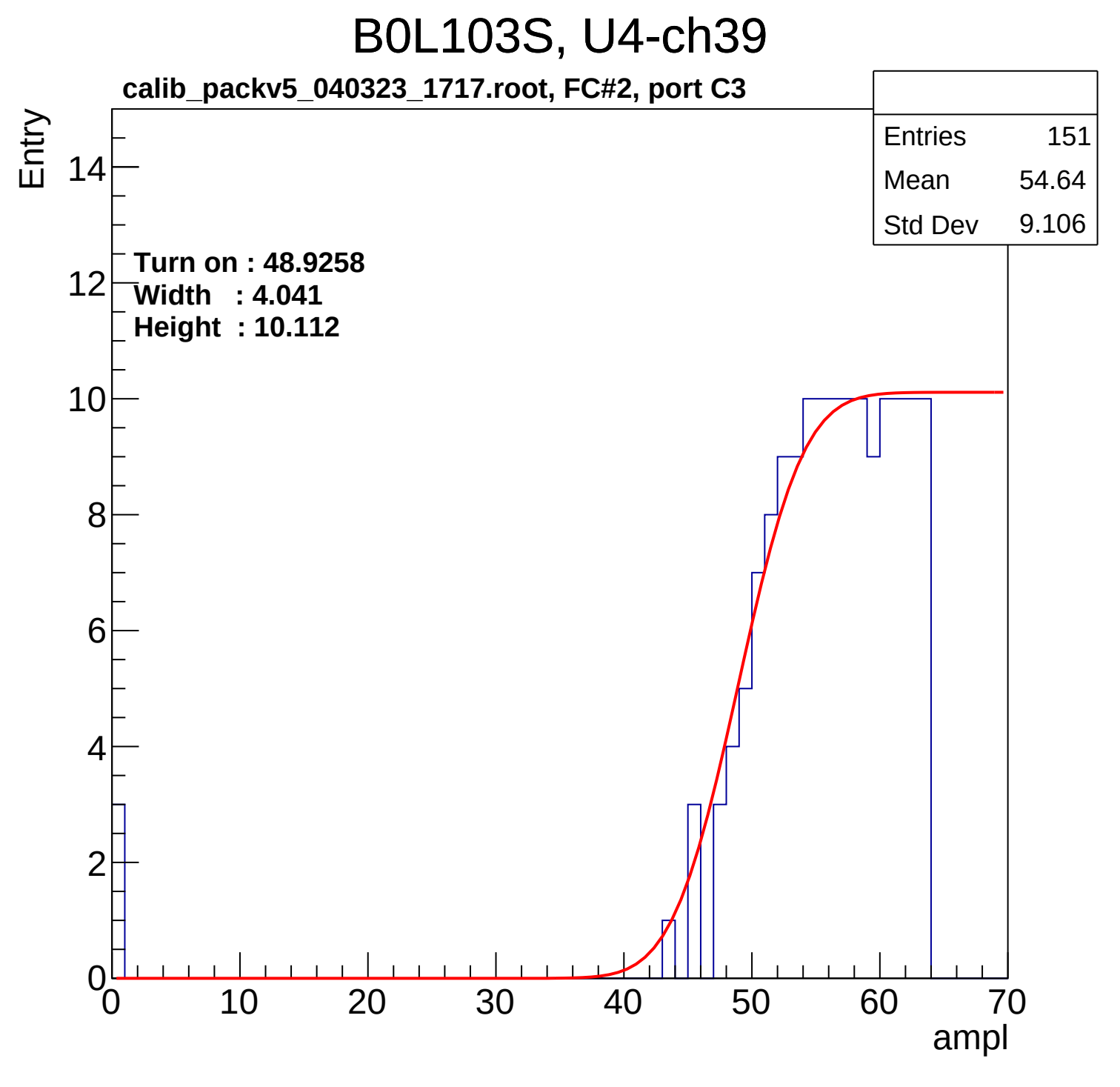
B0L103S, U4-ch39
calib_packv5_040323_1717.root, FC#2, port C3
Entries 151
Mean 54.64
Std Dev 9.106
Turn on : 48.9258
Width : 4.041
Height : 10.112
Entry
ampl
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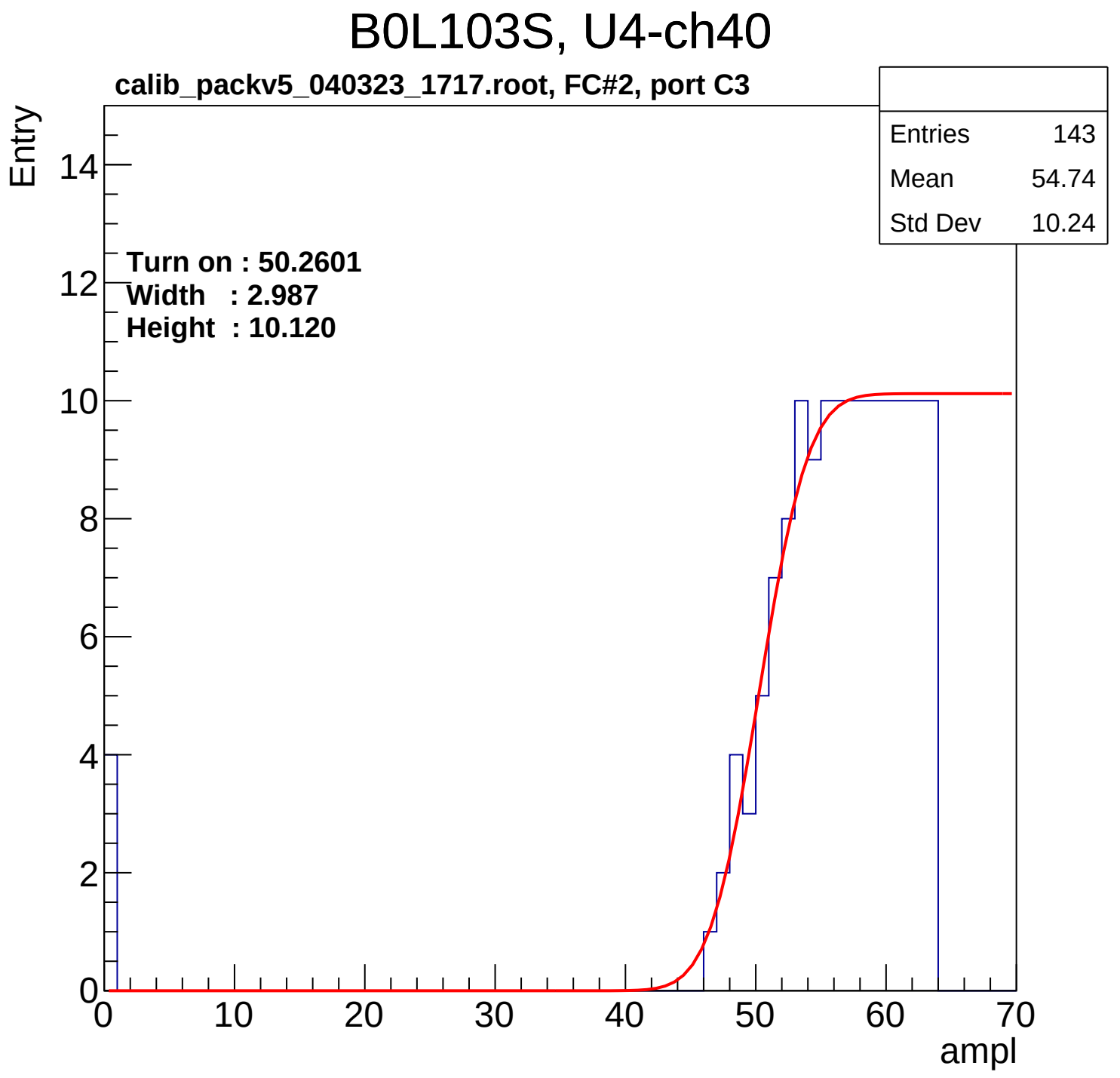
B0L103S, U4-ch40
calib_packv5_040323_1717.root, FC#2, port C3
Entries 143
Mean 54.74
Std Dev 10.24
Turn on : 50.2601
Width : 2.987
Height : 10.120
Entry
ampl
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8
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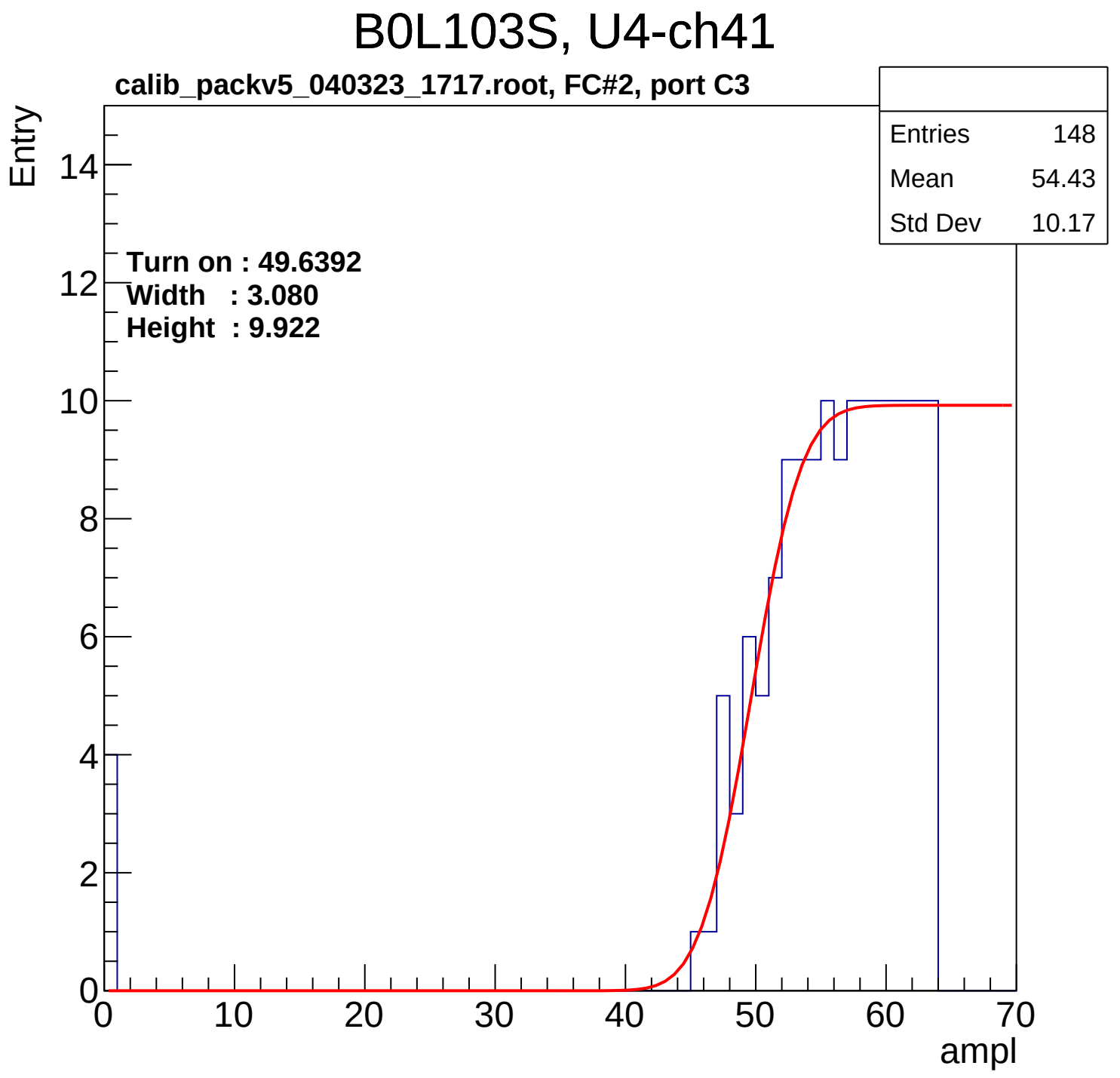
B0L103S, U4-ch41
calib_packv5_040323_1717.root, FC#2, port C3
Entries 148
Mean 54.43
Std Dev 10.17
Turn on : 49.6392
Width : 3.080
Height : 9.922
Entry
ampl
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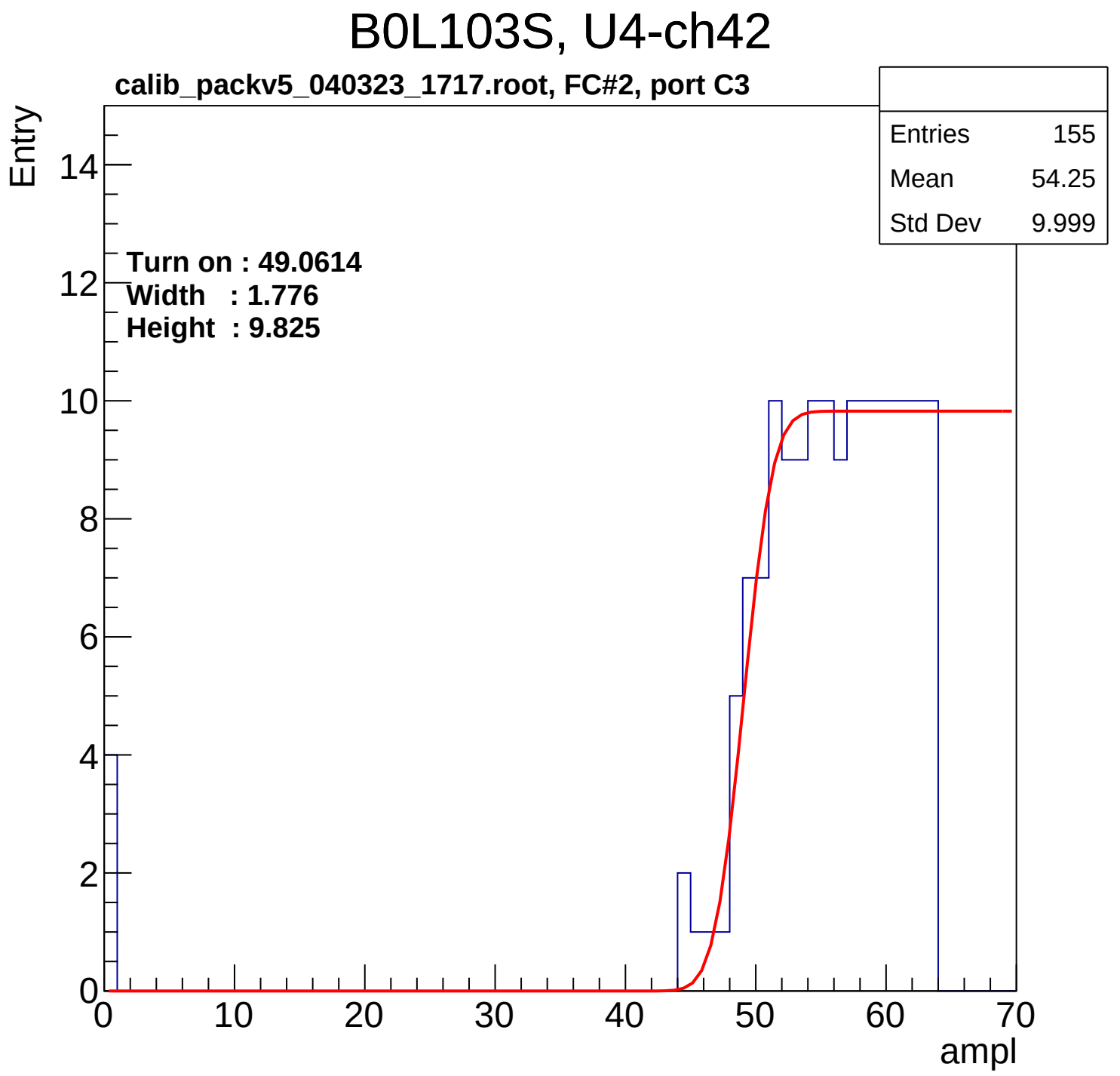
B0L103S, U4-ch42
calib_packv5_040323_1717.root, FC#2, port C3
Entries 155
Mean 54.25
Std Dev 9.999
Turn on : 49.0614
Width : 1.776
Height : 9.825
Entry
ampl
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8
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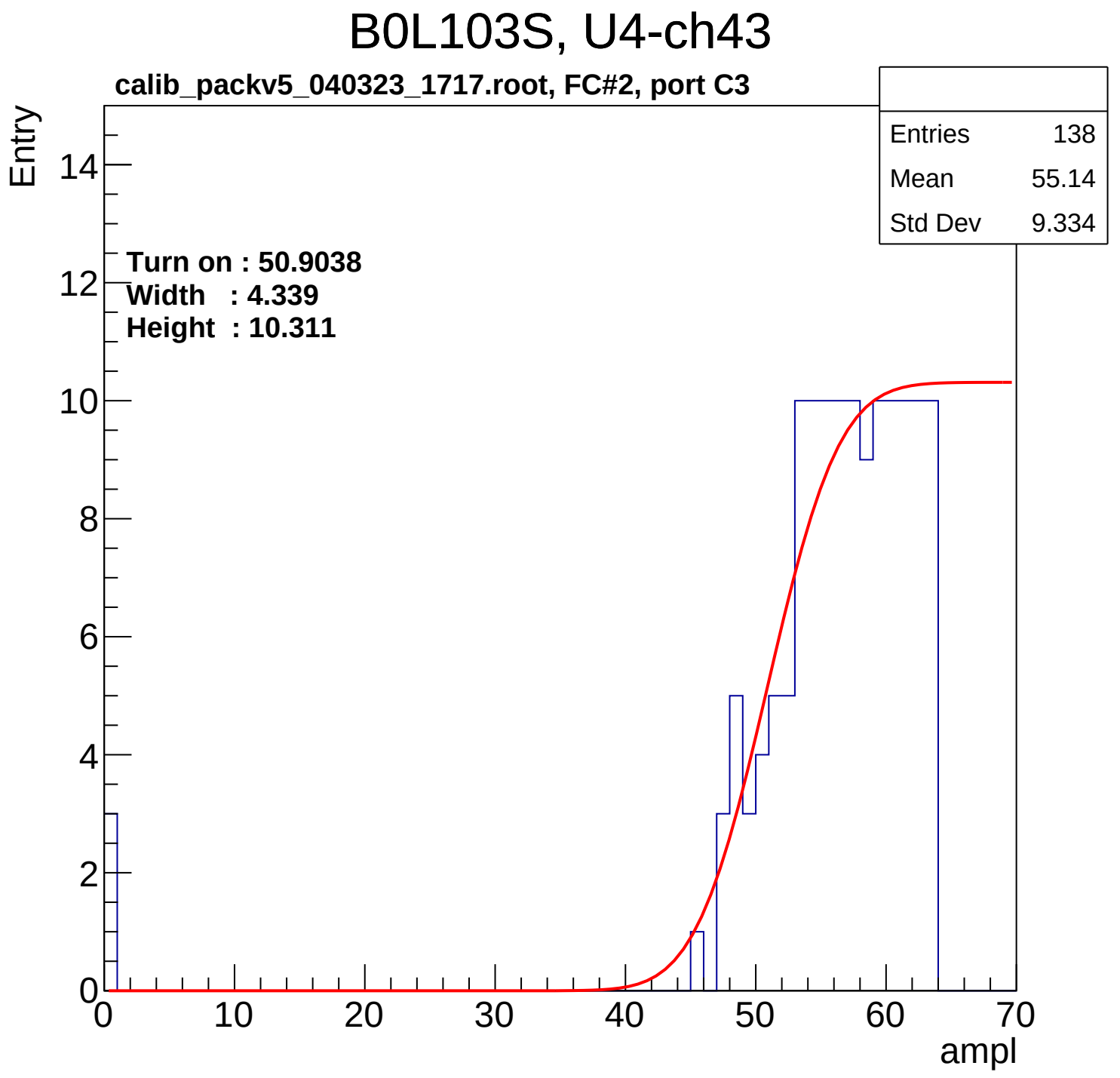
B0L103S, U4-ch43
calib_packv5_040323_1717.root, FC#2, port C3
Entries 138
Mean 55.14
Std Dev 9.334
Turn on : 50.9038
Width : 4.339
Height : 10.311
Entry
ampl
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8
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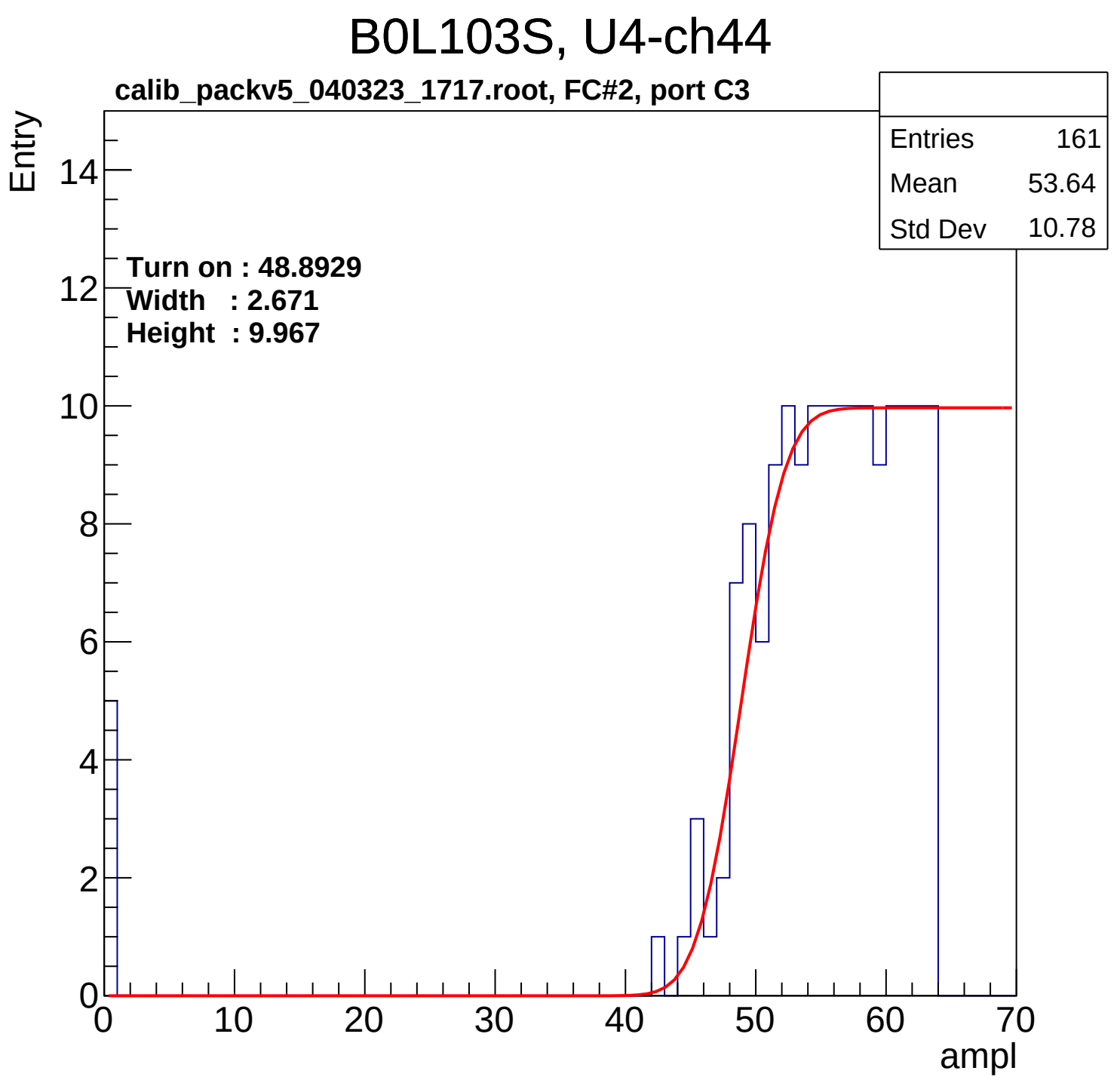
B0L103S, U4-ch44
calib_packv5_040323_1717.root, FC#2, port C3
Entries 161
Mean 53.64
Std Dev 10.78
Turn on : 48.8929
Width : 2.671
Height : 9.967
Entry
ampl
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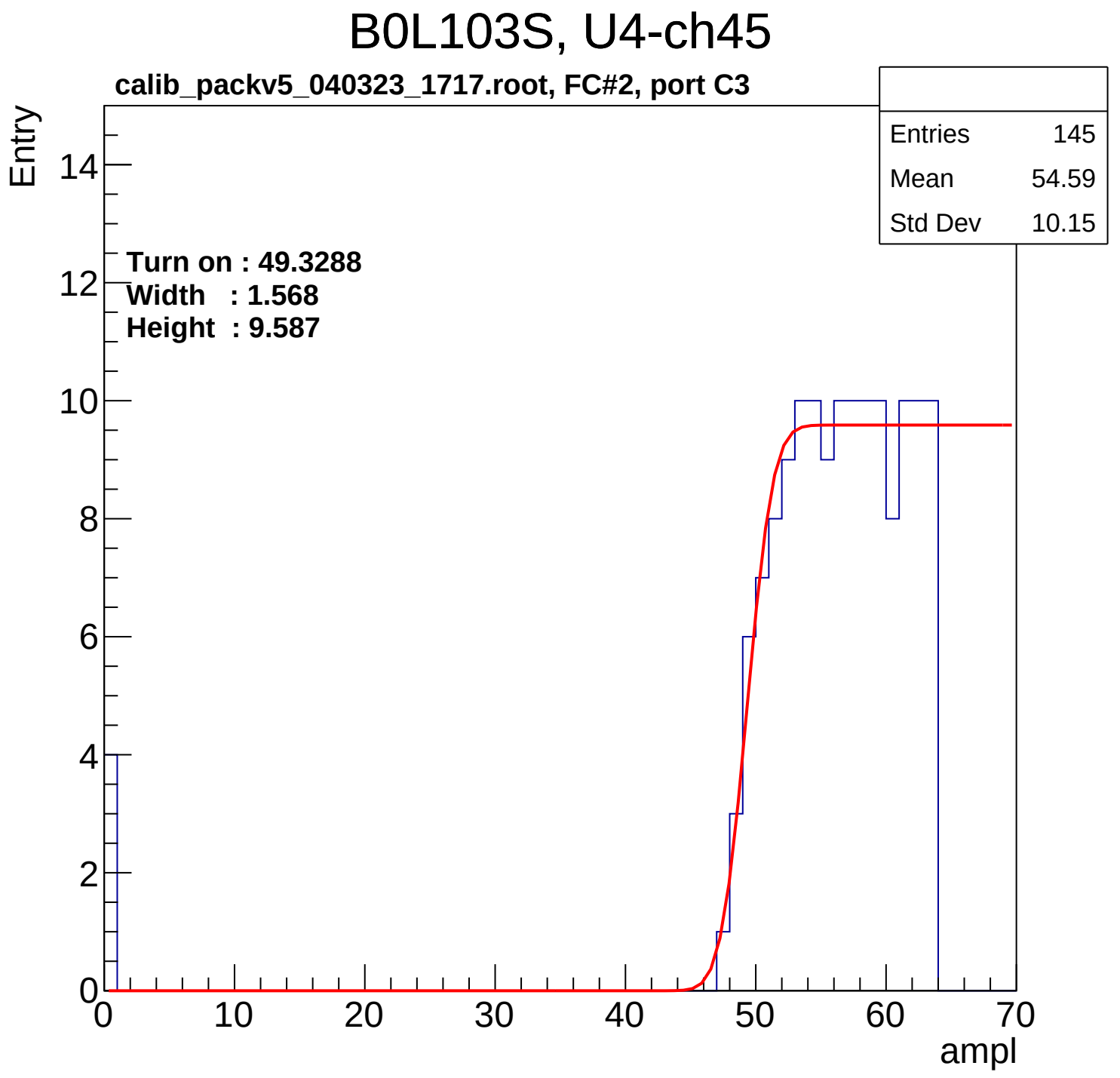
B0L103S, U4-ch45
calib_packv5_040323_1717.root, FC#2, port C3
Entries 145
Mean 54.59
Std Dev 10.15
Turn on : 49.3288
Width : 1.568
Height : 9.587
Entry
ampl
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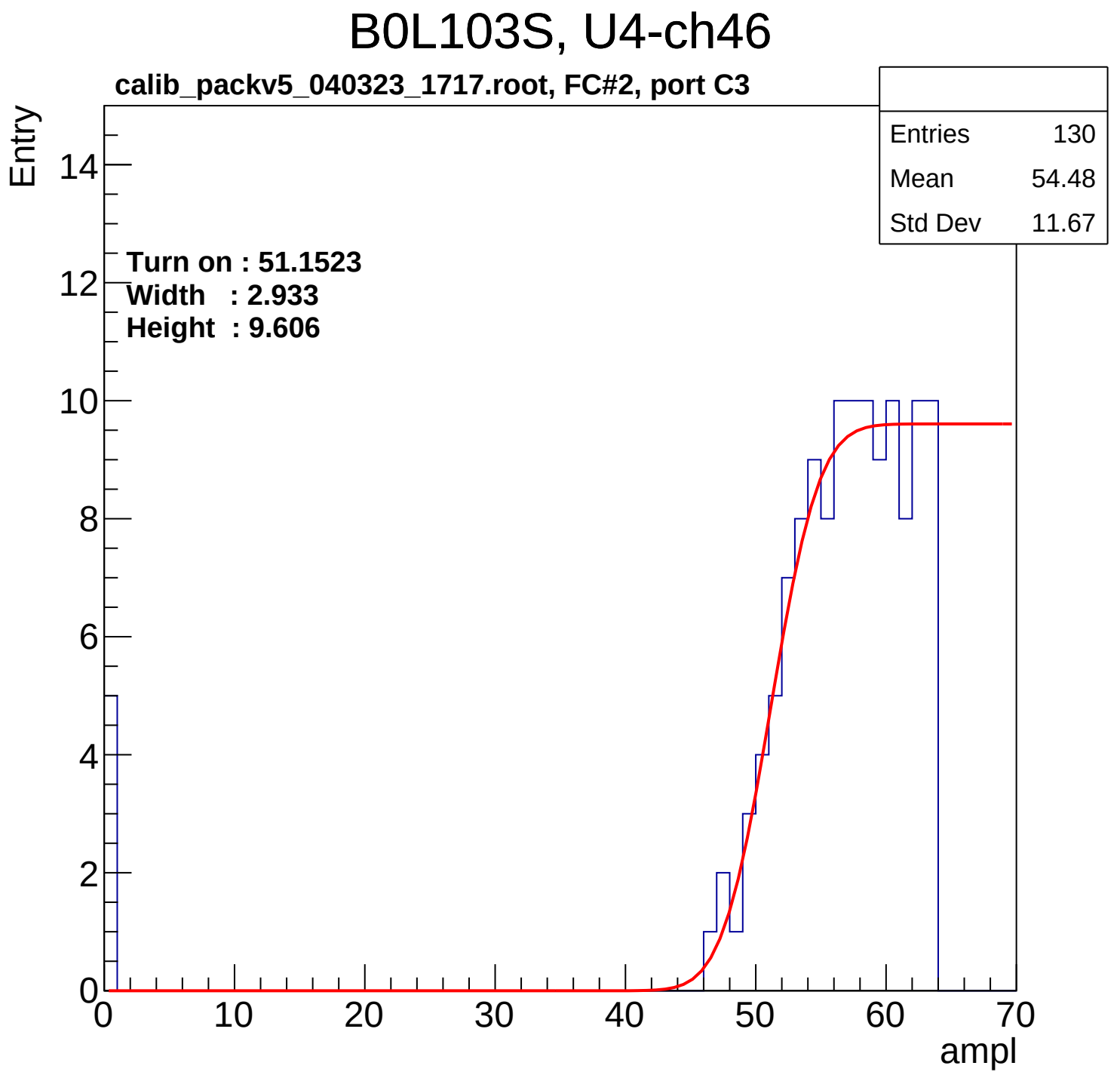
B0L103S, U4-ch46
calib_packv5_040323_1717.root, FC#2, port C3
Entries 130
Mean 54.48
Std Dev 11.67
Turn on : 51.1523
Width : 2.933
Height : 9.606
Entry
ampl
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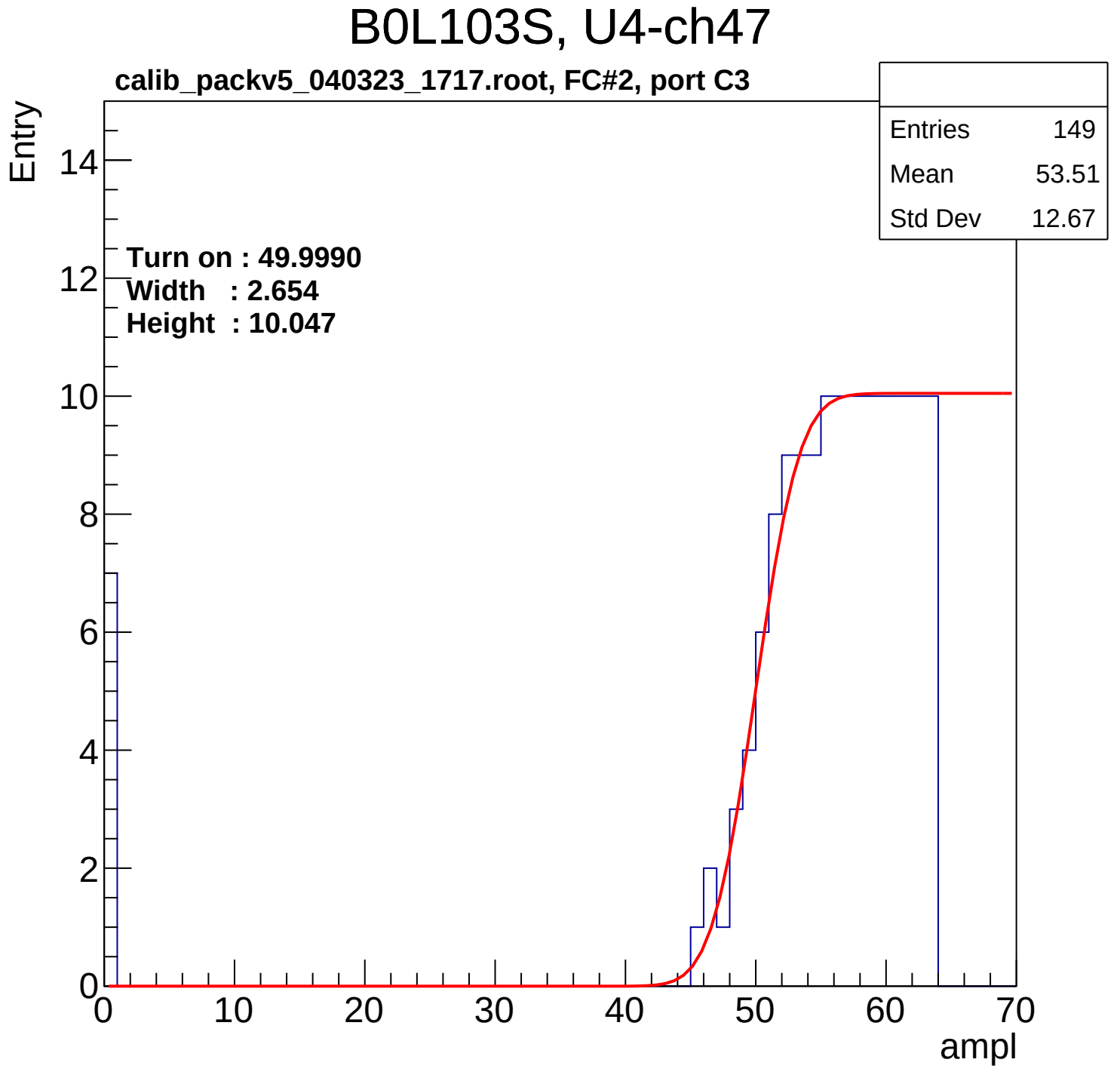
B0L103S, U4-ch47
calib_packv5_040323_1717.root, FC#2, port C3
Entries 149
Mean 53.51
Std Dev 12.67
Turn on : 49.9990
Width : 2.654
Height : 10.047
Entry
ampl
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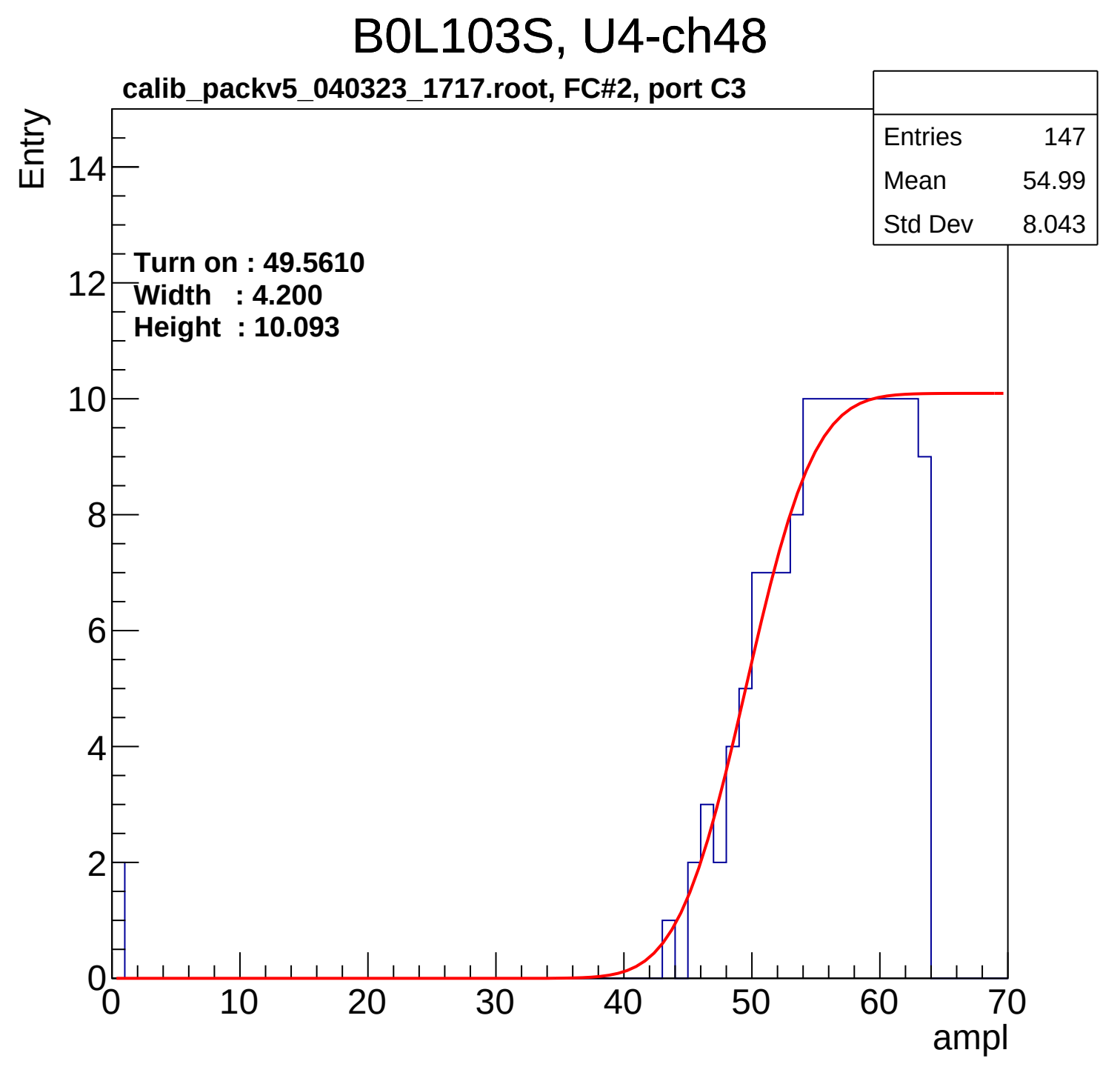
B0L103S, U4-ch48
calib_packv5_040323_1717.root, FC#2, port C3
Entries 147
Mean 54.99
Std Dev 8.043
Turn on : 49.5610
Width : 4.200
Height : 10.093
Entry
ampl
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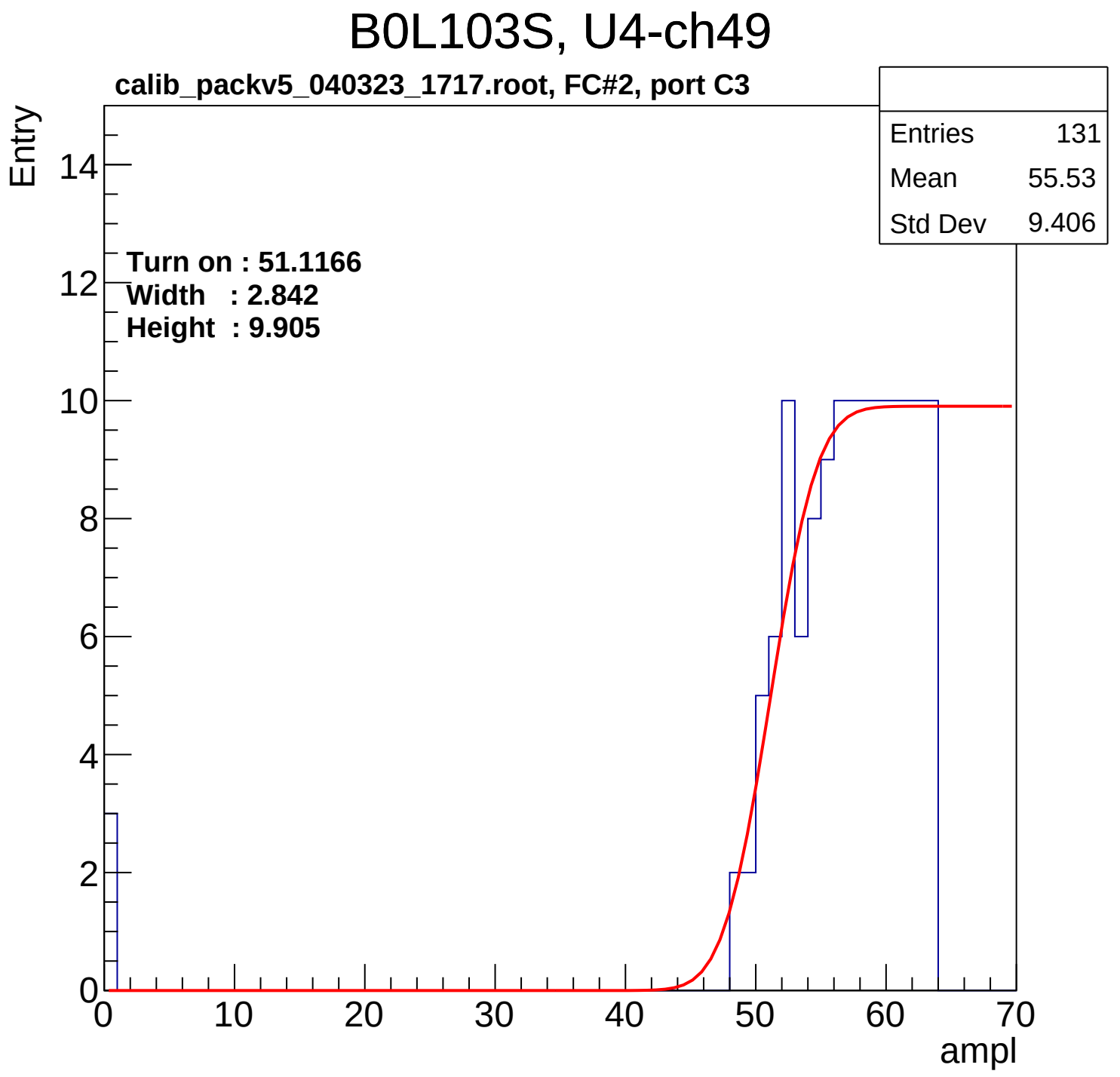
B0L103S, U4-ch49
calib_packv5_040323_1717.root, FC#2, port C3
Entries 131
Mean 55.53
Std Dev 9.406
Turn on : 51.1166
Width : 2.842
Height : 9.905
Entry
ampl
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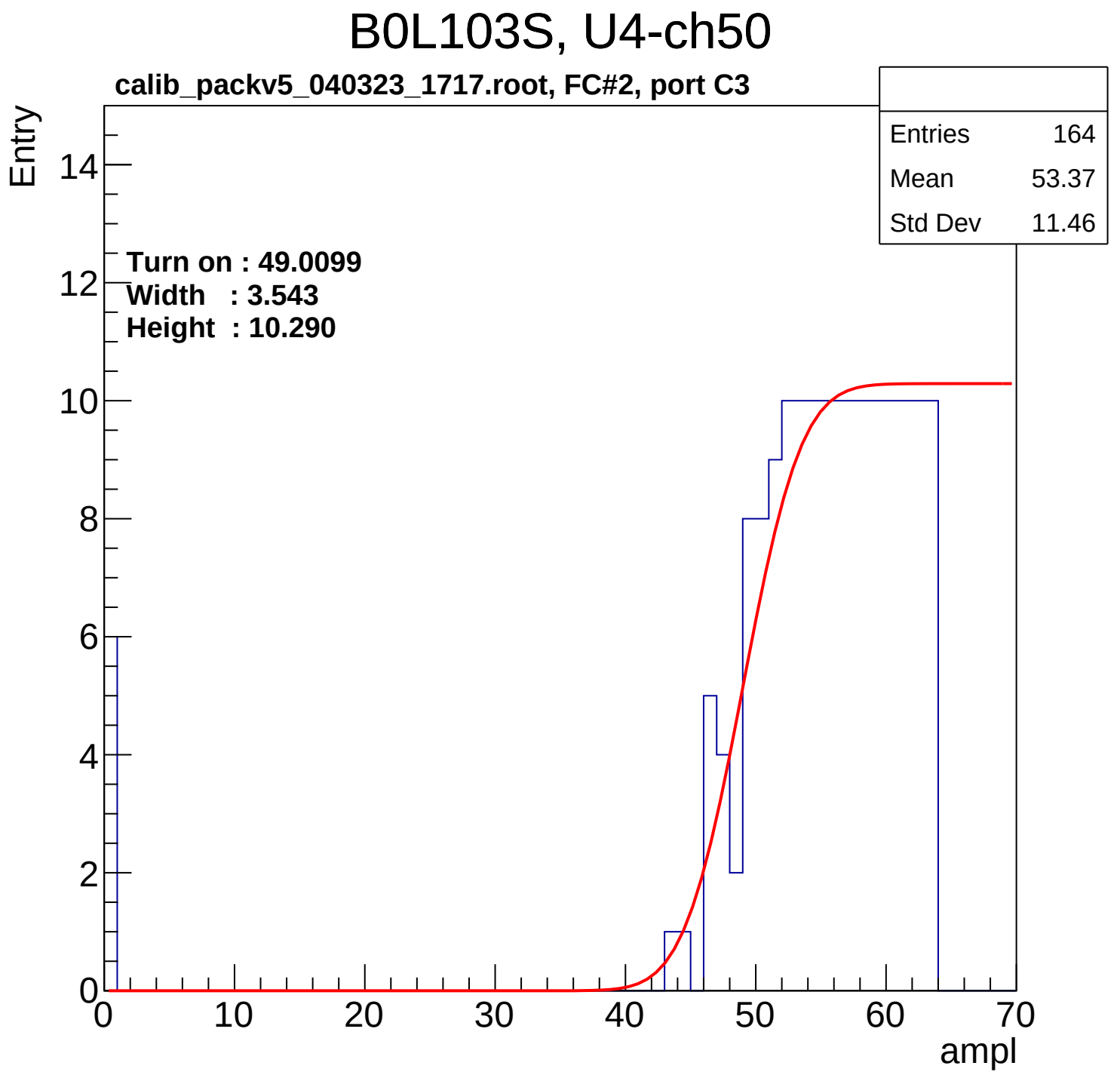
B0L103S, U4-ch50
calib_packv5_040323_1717.root, FC#2, port C3
Entries 164
Mean 53.37
Std Dev 11.46
Turn on : 49.0099
Width : 3.543
Height : 10.290
Entry
ampl
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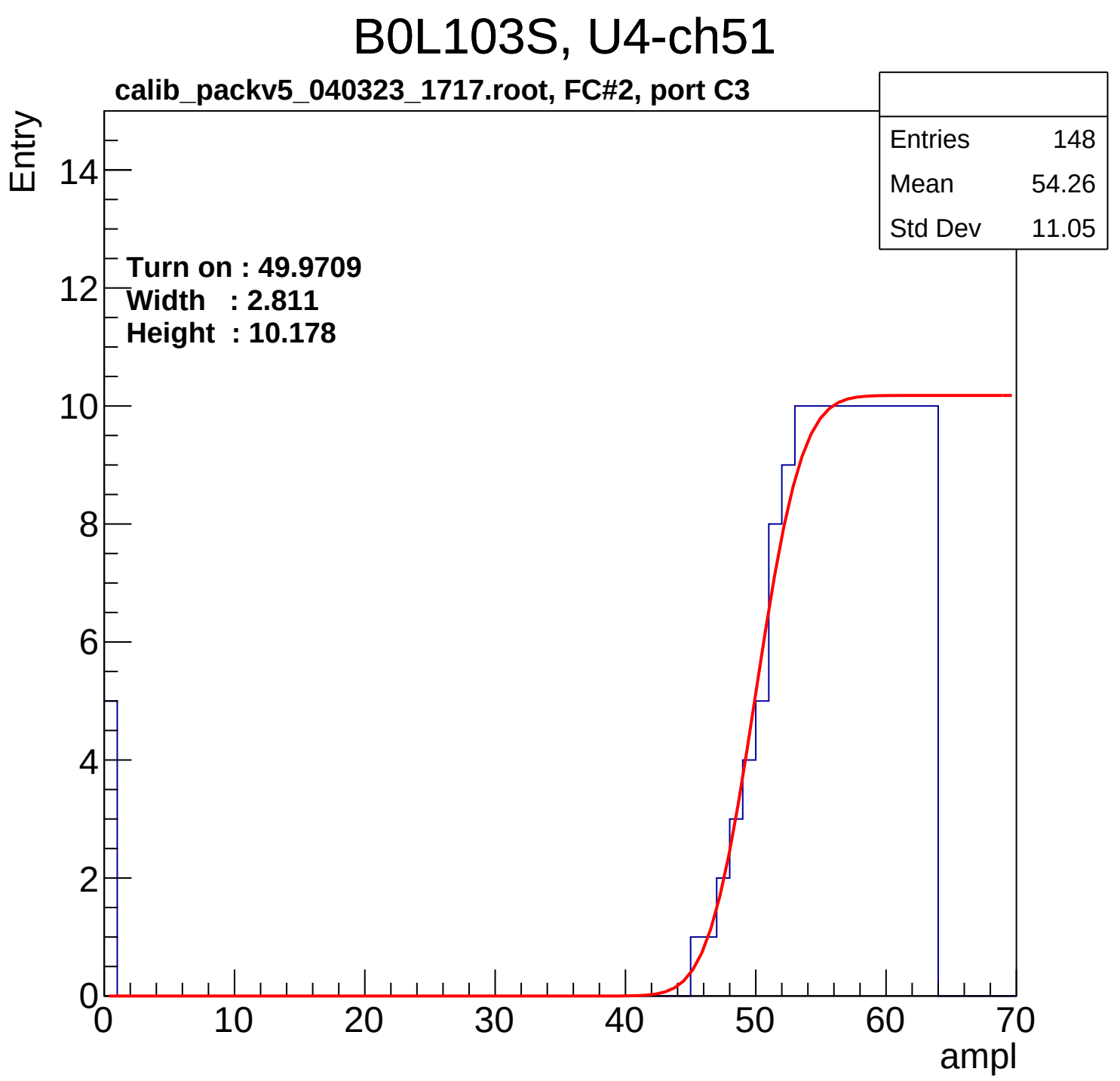
B0L103S, U4-ch51
calib_packv5_040323_1717.root, FC#2, port C3
Entries 148
Mean 54.26
Std Dev 11.05
Turn on : 49.9709
Width : 2.811
Height : 10.178
Entry
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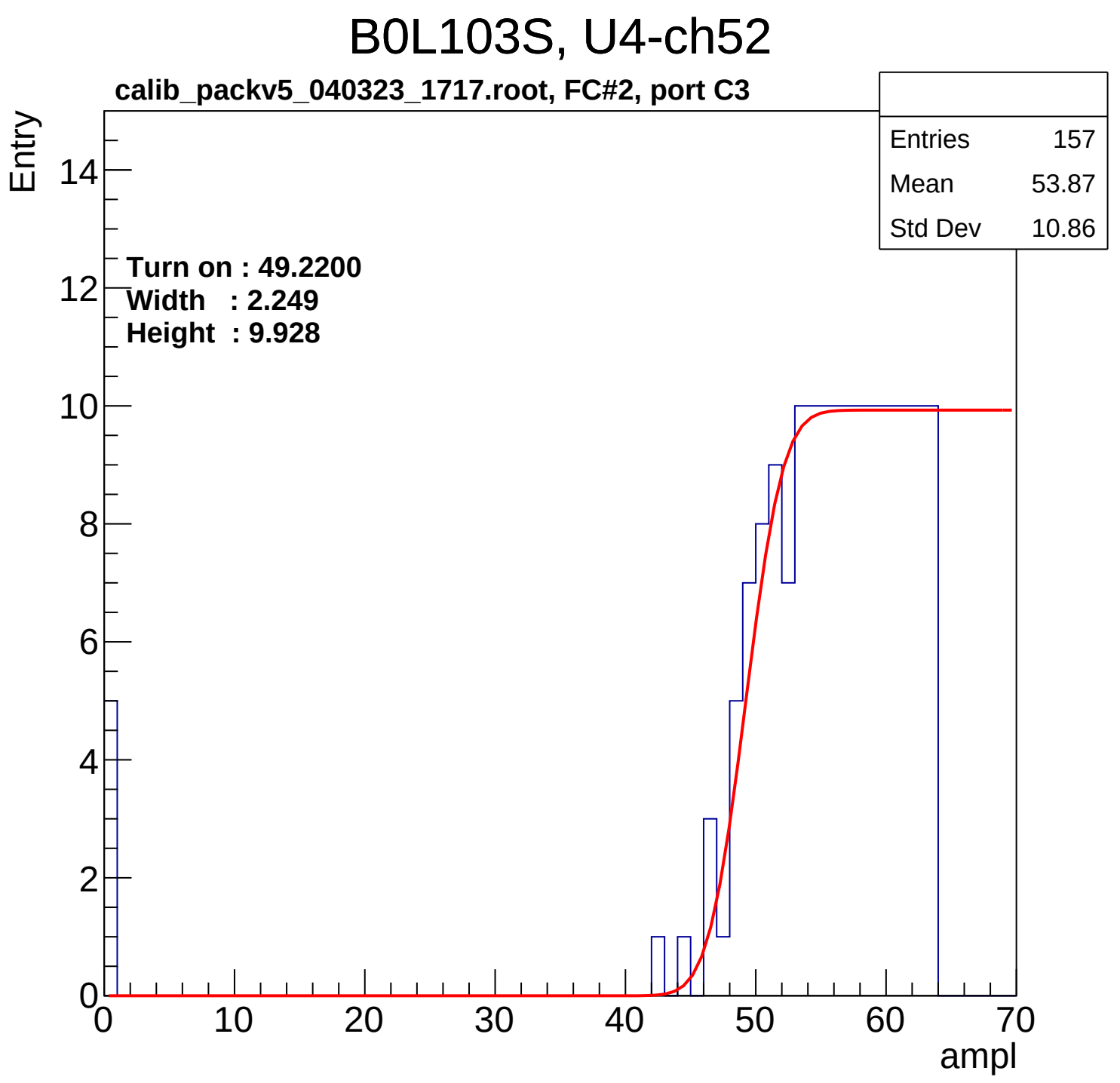
B0L103S, U4-ch52
calib_packv5_040323_1717.root, FC#2, port C3
Entries 157
Mean 53.87
Std Dev 10.86
Turn on : 49.2200
Width : 2.249
Height : 9.928
Entry
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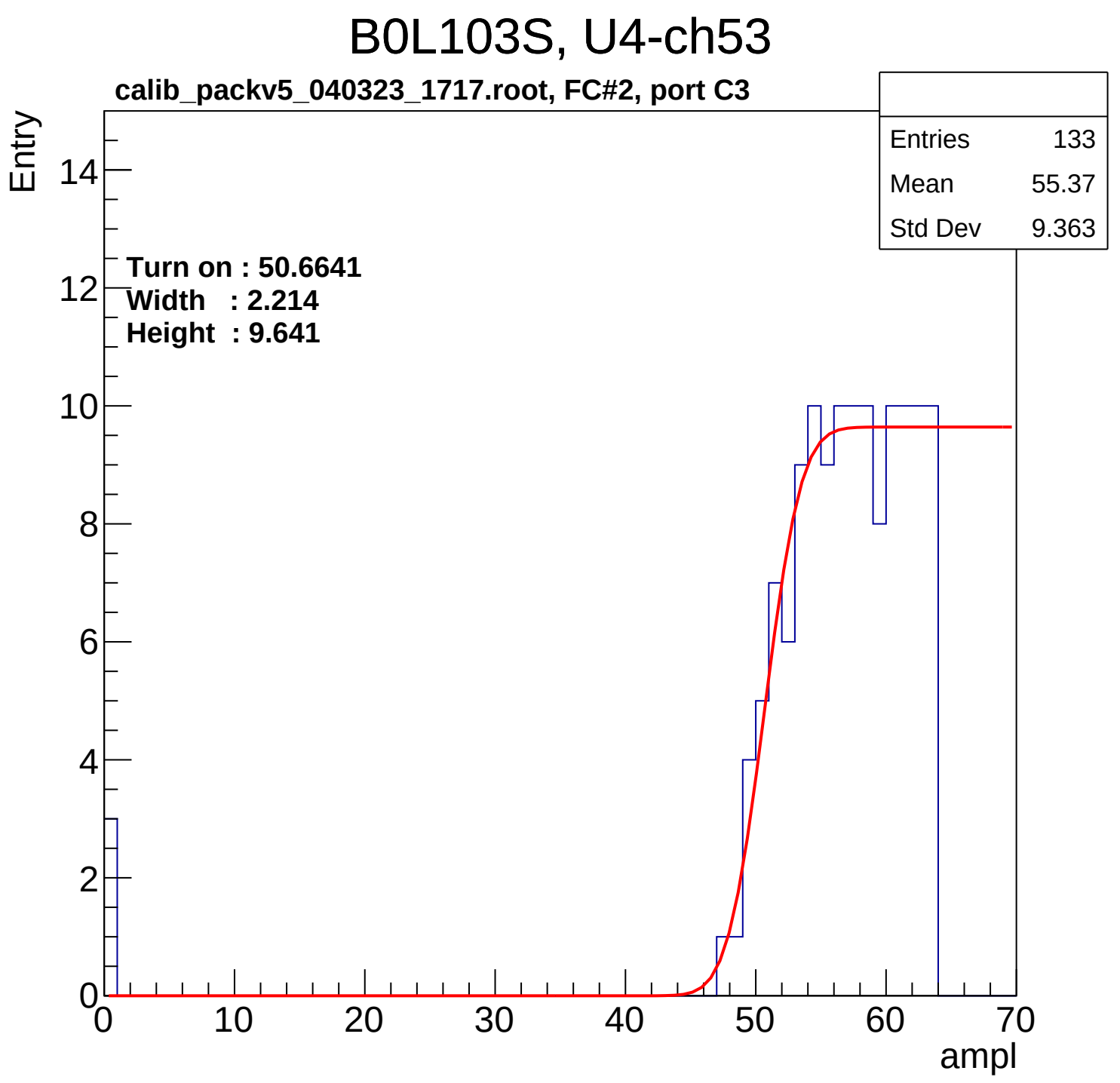
B0L103S, U4-ch53
calib_packv5_040323_1717.root, FC#2, port C3
Entries 133
Mean 55.37
Std Dev 9.363
Turn on : 50.6641
Width : 2.214
Height : 9.641
Entry
ampl
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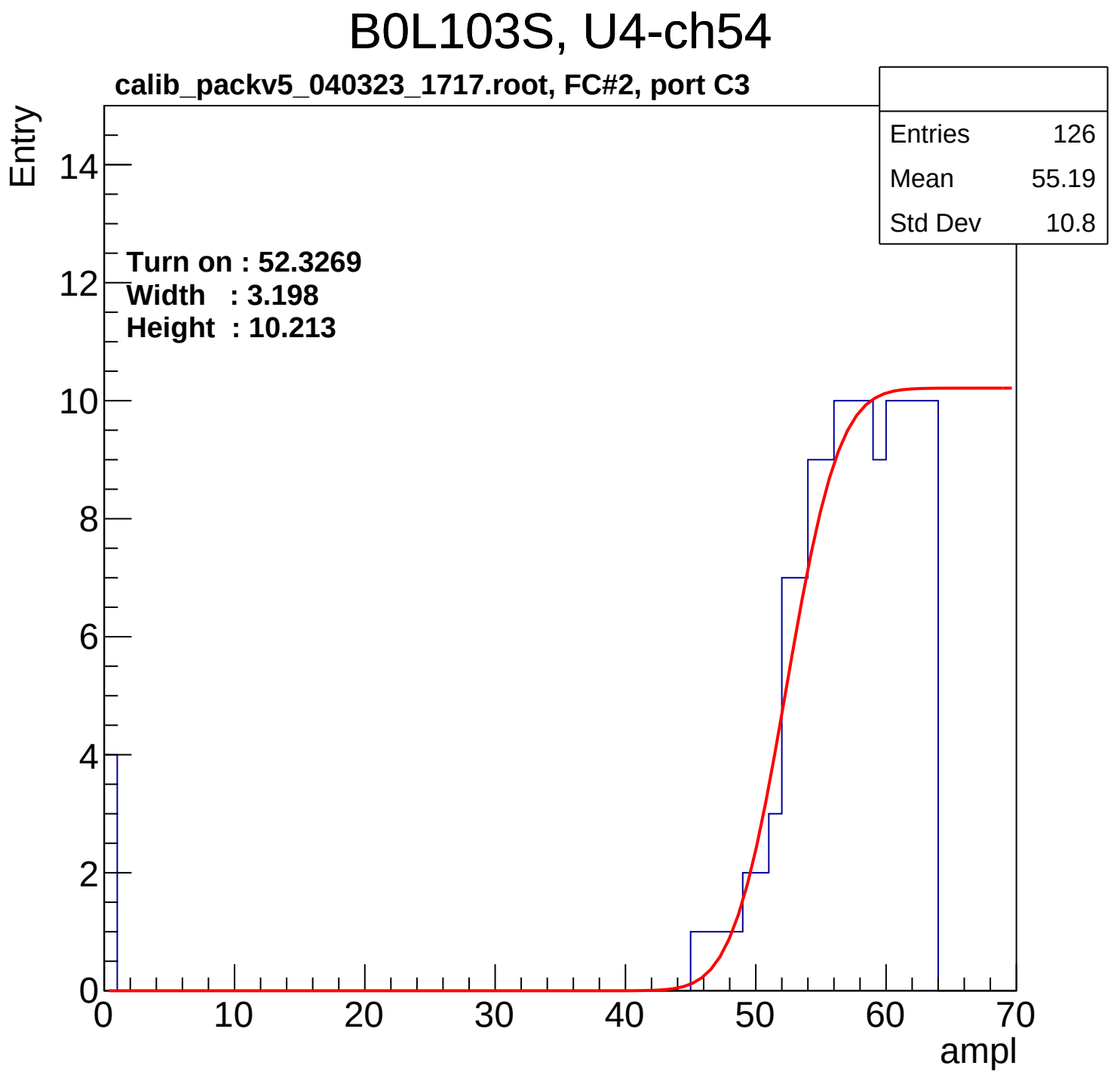
B0L103S, U4-ch54
calib_packv5_040323_1717.root, FC#2, port C3
Entries 126
Mean 55.19
Std Dev 10.8
Turn on : 52.3269
Width : 3.198
Height : 10.213
Entry
ampl
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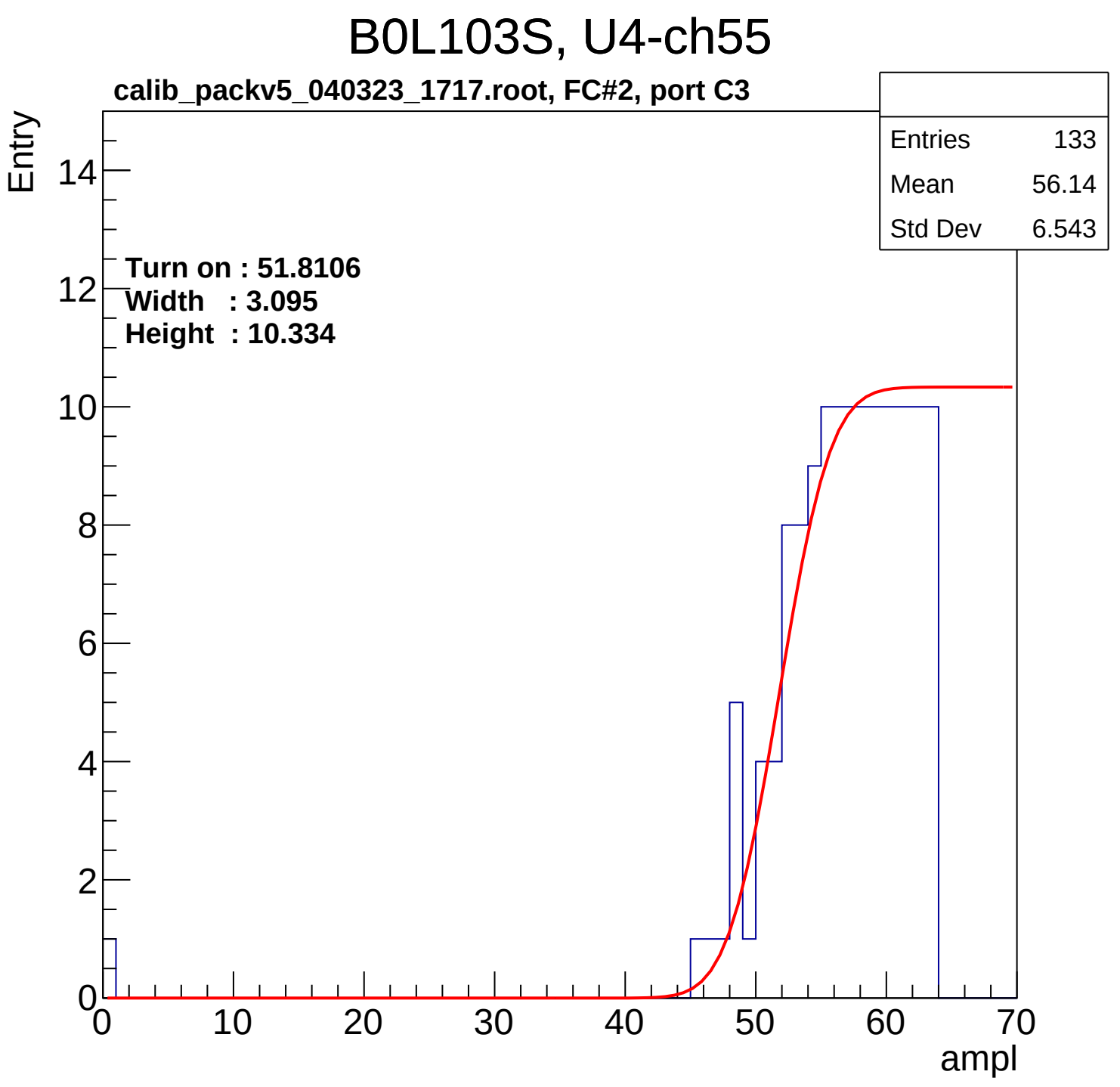
B0L103S, U4-ch55
calib_packv5_040323_1717.root, FC#2, port C3
Entries 133
Mean 56.14
Std Dev 6.543
Turn on : 51.8106
Width : 3.095
Height : 10.334
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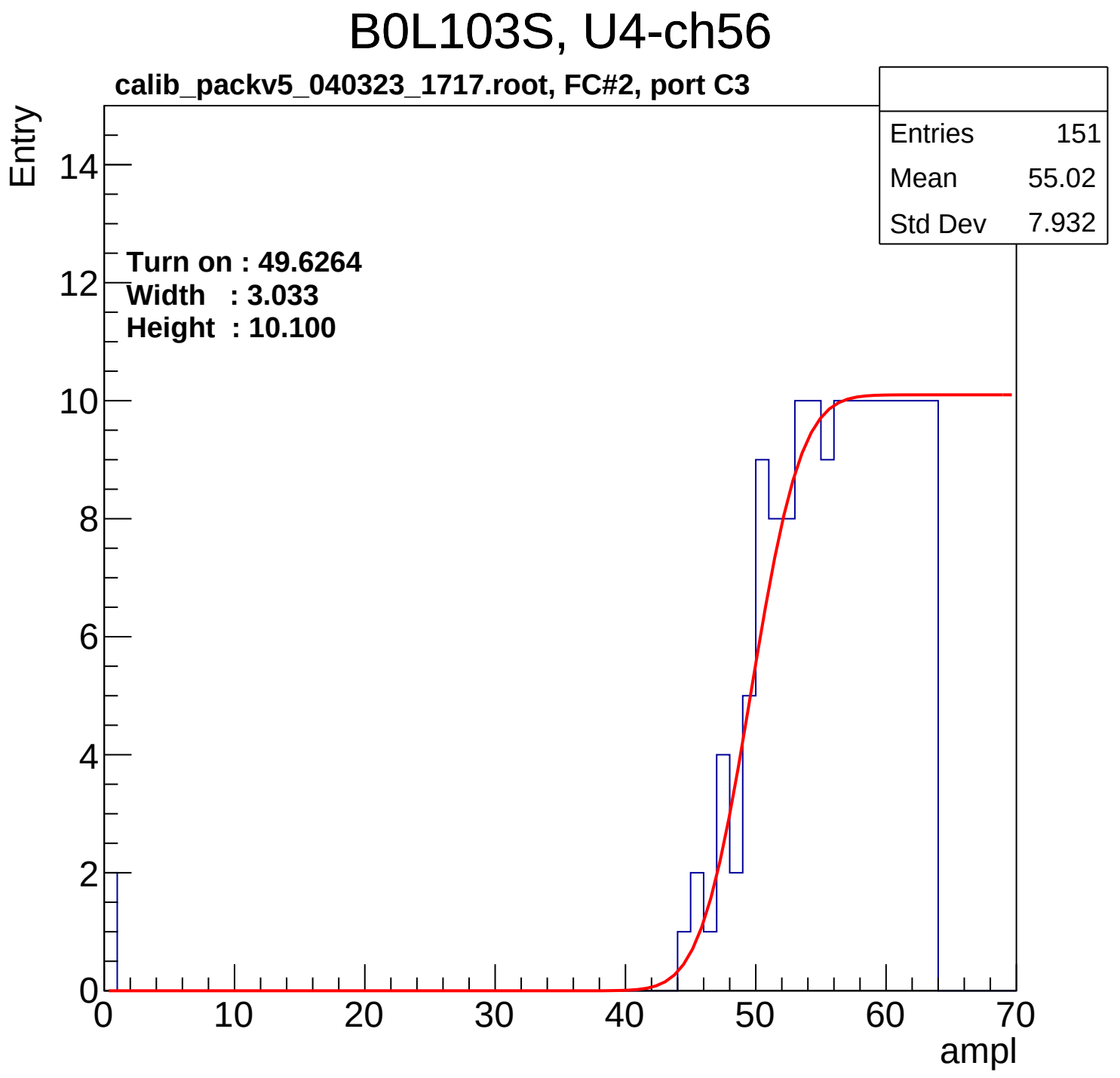
B0L103S, U4-ch56
calib_packv5_040323_1717.root, FC#2, port C3
Entries 151
Mean 55.02
Std Dev 7.932
Turn on : 49.6264
Width : 3.033
Height : 10.100
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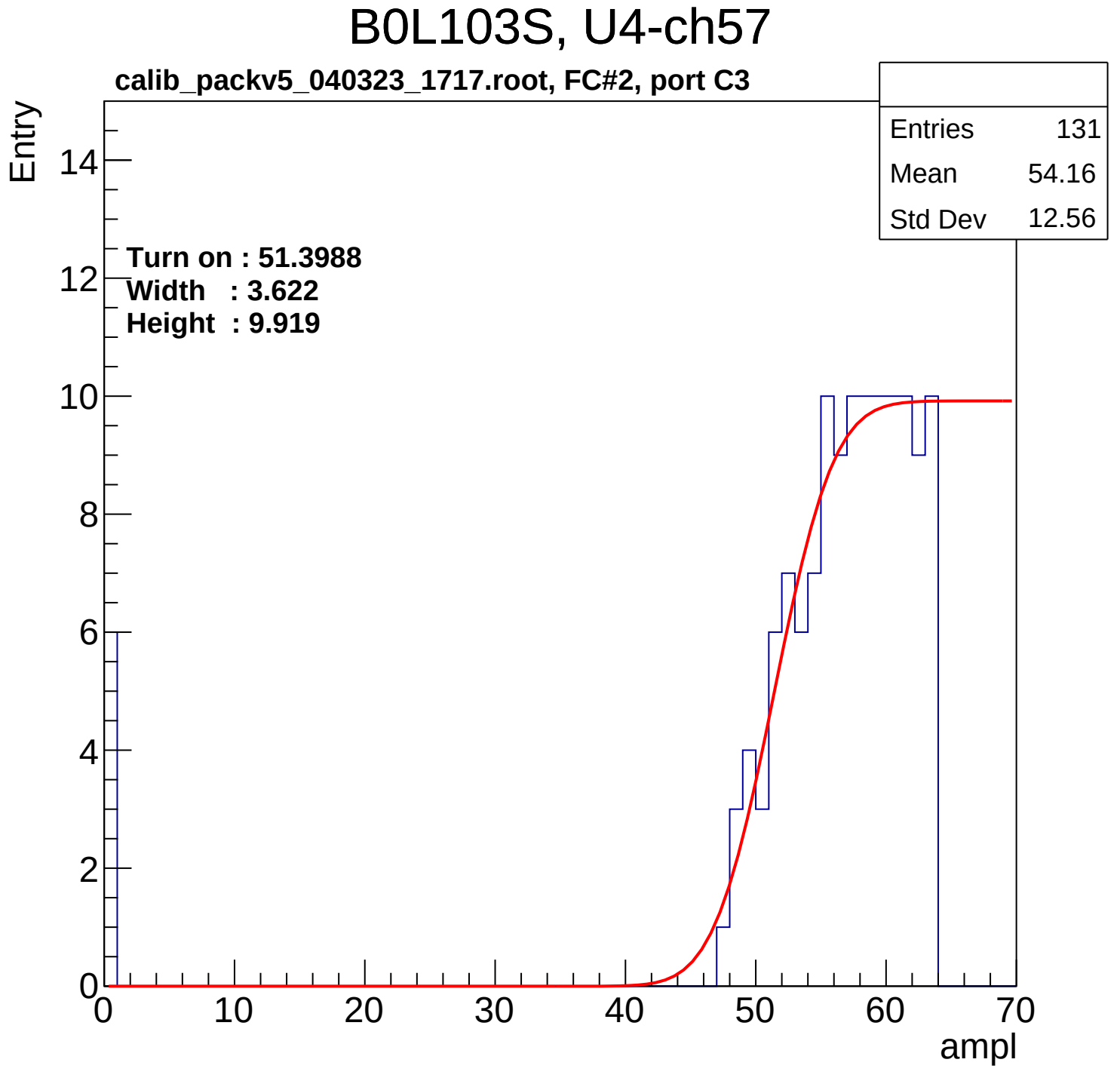
B0L103S, U4-ch57
calib_packv5_040323_1717.root, FC#2, port C3
Entries 131
Mean 54.16
Std Dev 12.56
Turn on : 51.3988
Width : 3.622
Height : 9.919
Entry
ampl
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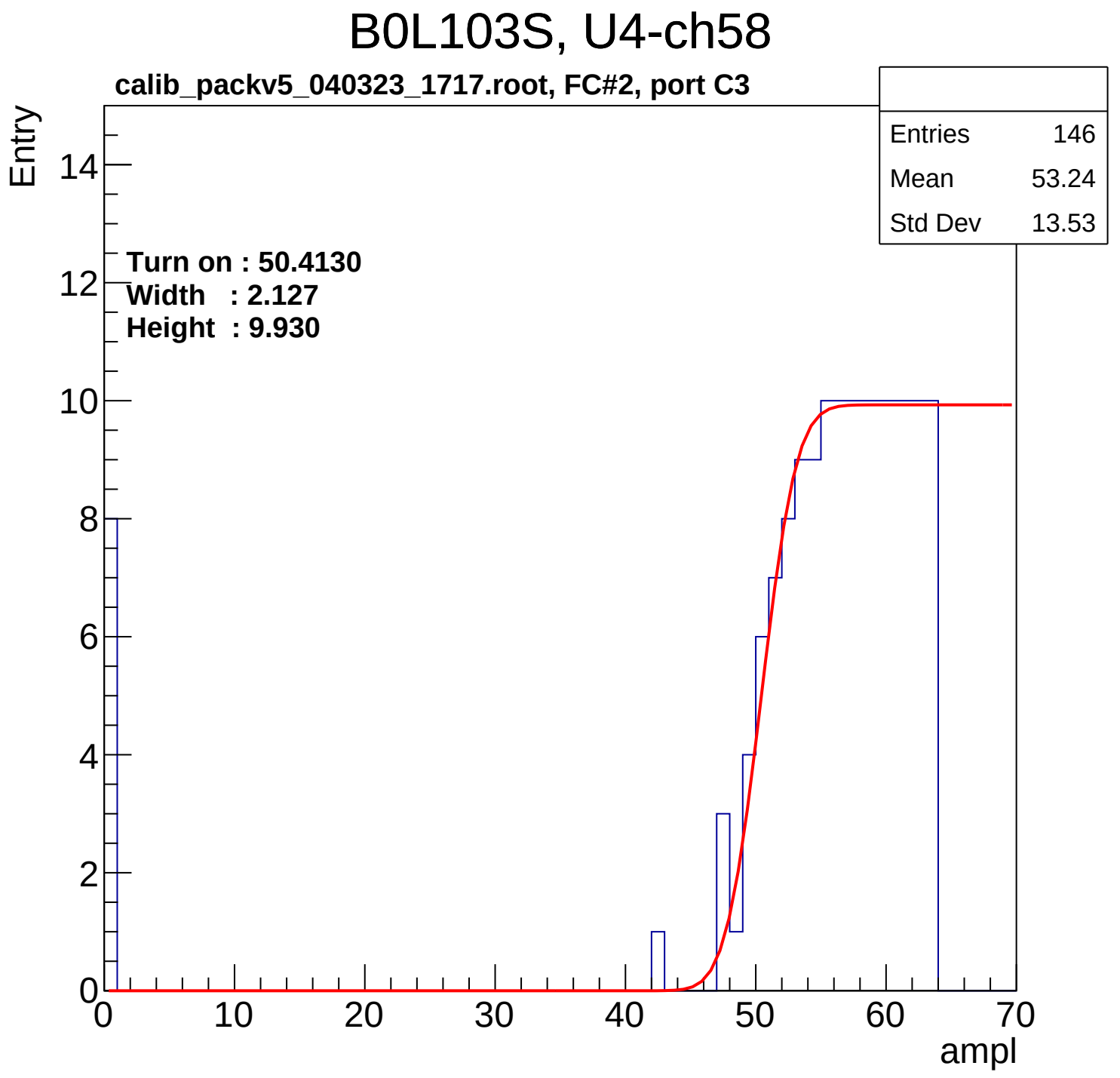
B0L103S, U4-ch58
calib_packv5_040323_1717.root, FC#2, port C3
Entries 146
Mean 53.24
Std Dev 13.53
Turn on : 50.4130
Width : 2.127
Height : 9.930
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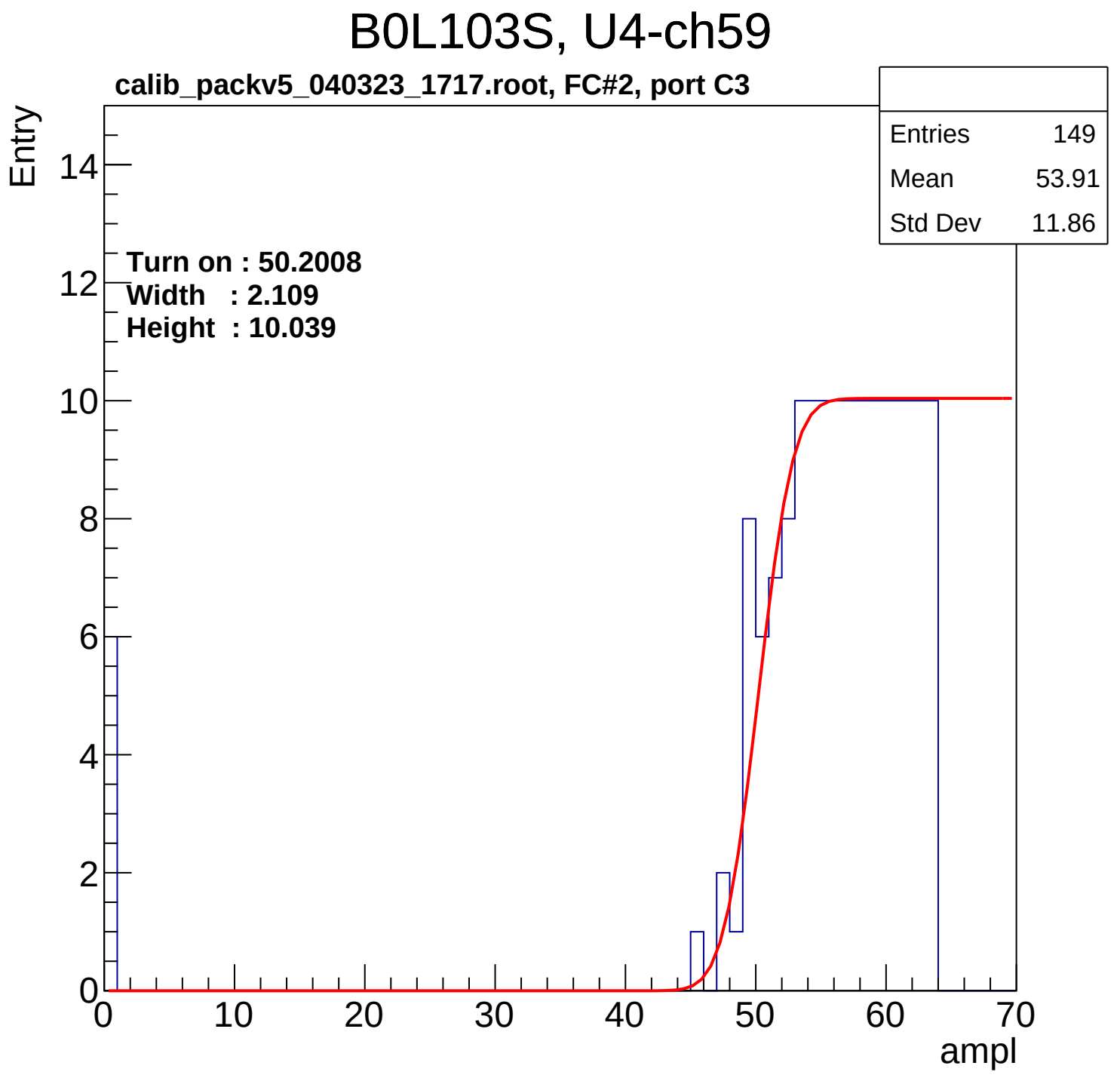
B0L103S, U4-ch59
calib_packv5_040323_1717.root, FC#2, port C3
Entries 149
Mean 53.91
Std Dev 11.86
Turn on : 50.2008
Width : 2.109
Height : 10.039
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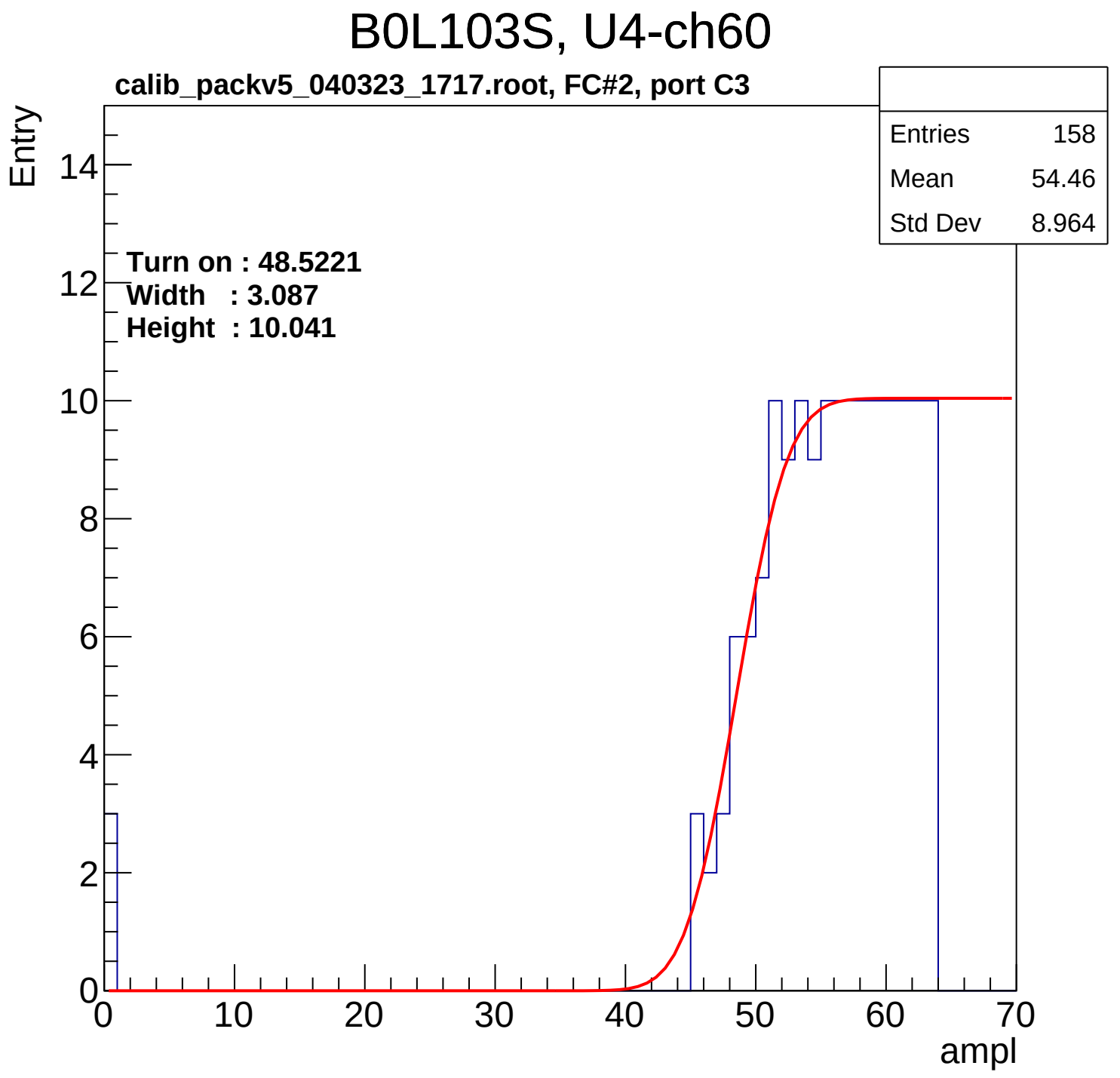
B0L103S, U4-ch60
calib_packv5_040323_1717.root, FC#2, port C3
Entries 158
Mean 54.46
Std Dev 8.964
Turn on : 48.5221
Width : 3.087
Height : 10.041
Entry
ampl
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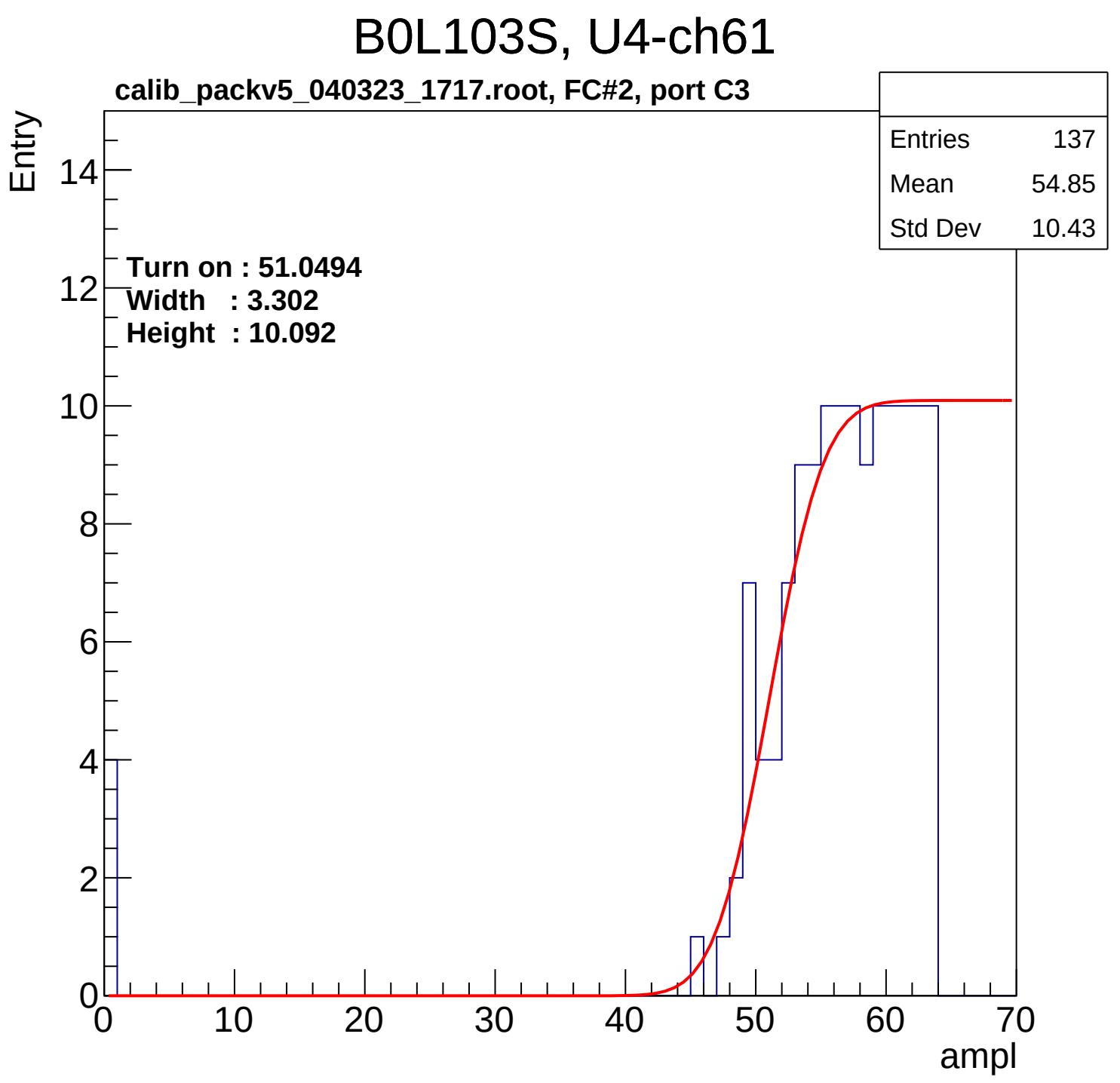
B0L103S, U4-ch61
calib_packv5_040323_1717.root, FC#2, port C3
Entries 137
Mean 54.85
Std Dev 10.43
Turn on : 51.0494
Width : 3.302
Height : 10.092
Entry
ampl
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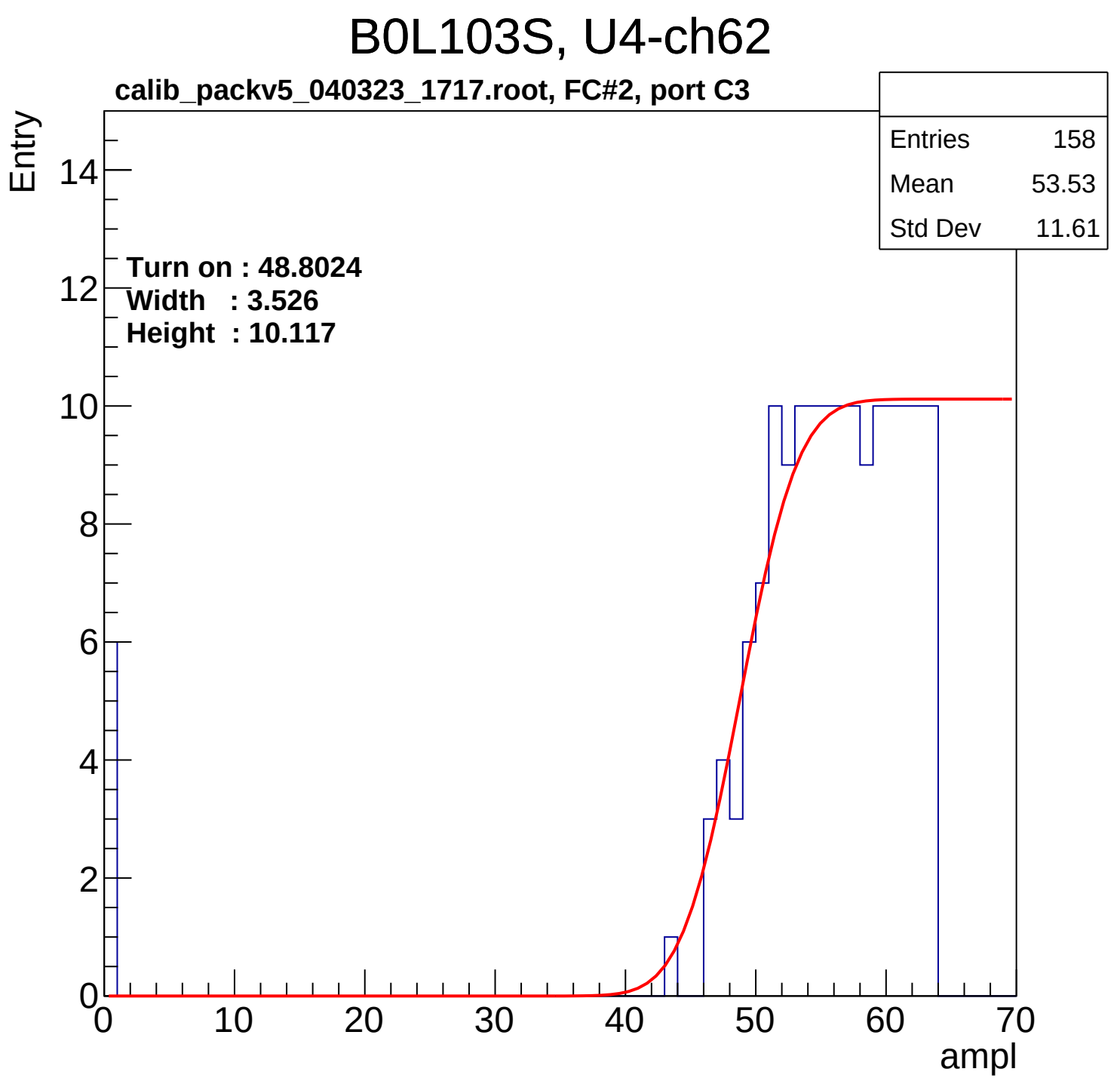
B0L103S, U4-ch62
calib_packv5_040323_1717.root, FC#2, port C3
Entries 158
Mean 53.53
Std Dev 11.61
Turn on : 48.8024
Width : 3.526
Height : 10.117
Entry
ampl
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8
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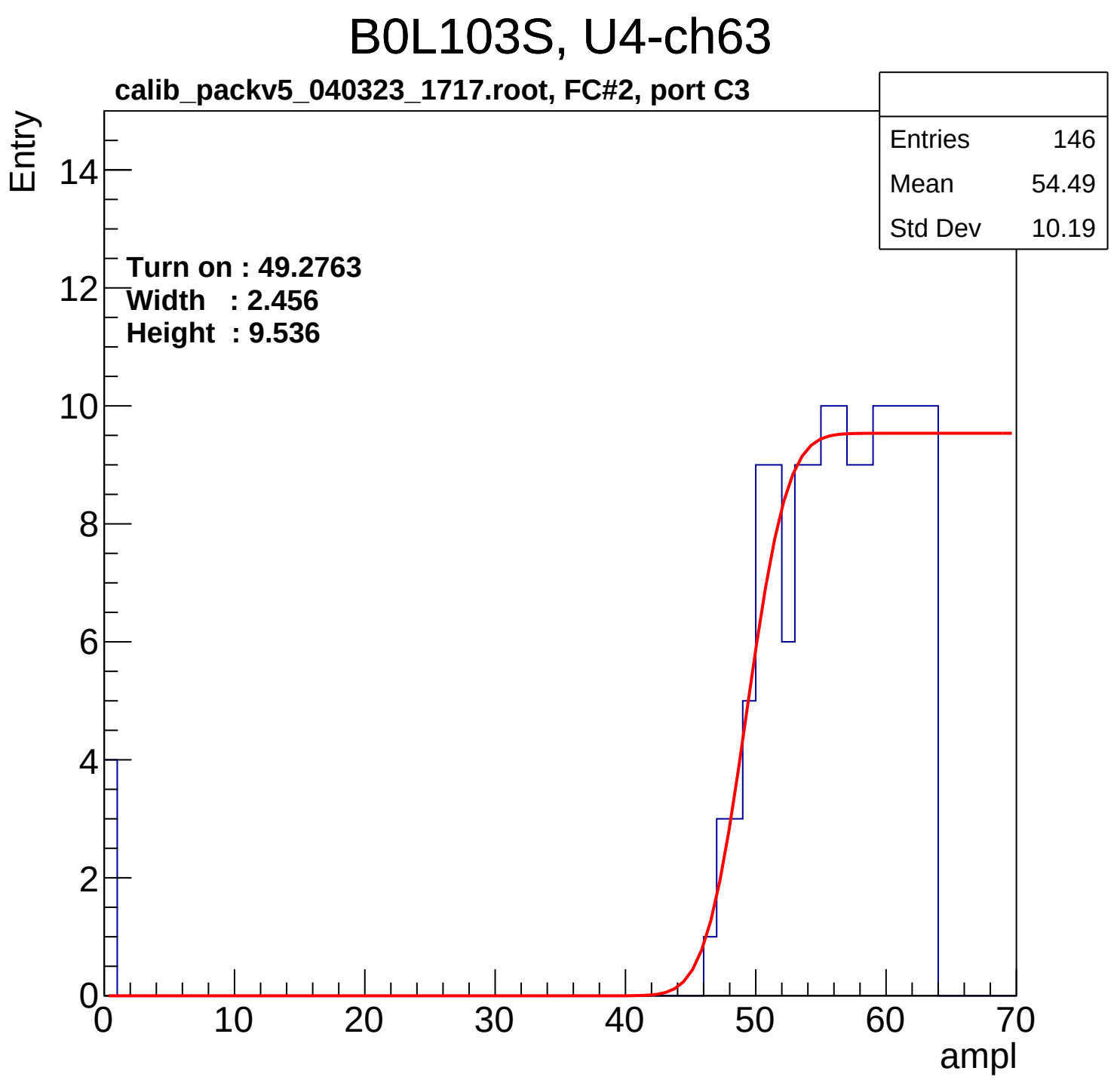
B0L103S, U4-ch63
calib_packv5_040323_1717.root, FC#2, port C3
Entries 146
Mean 54.49
Std Dev 10.19
Turn on : 49.2763
Width : 2.456
Height : 9.536
Entry
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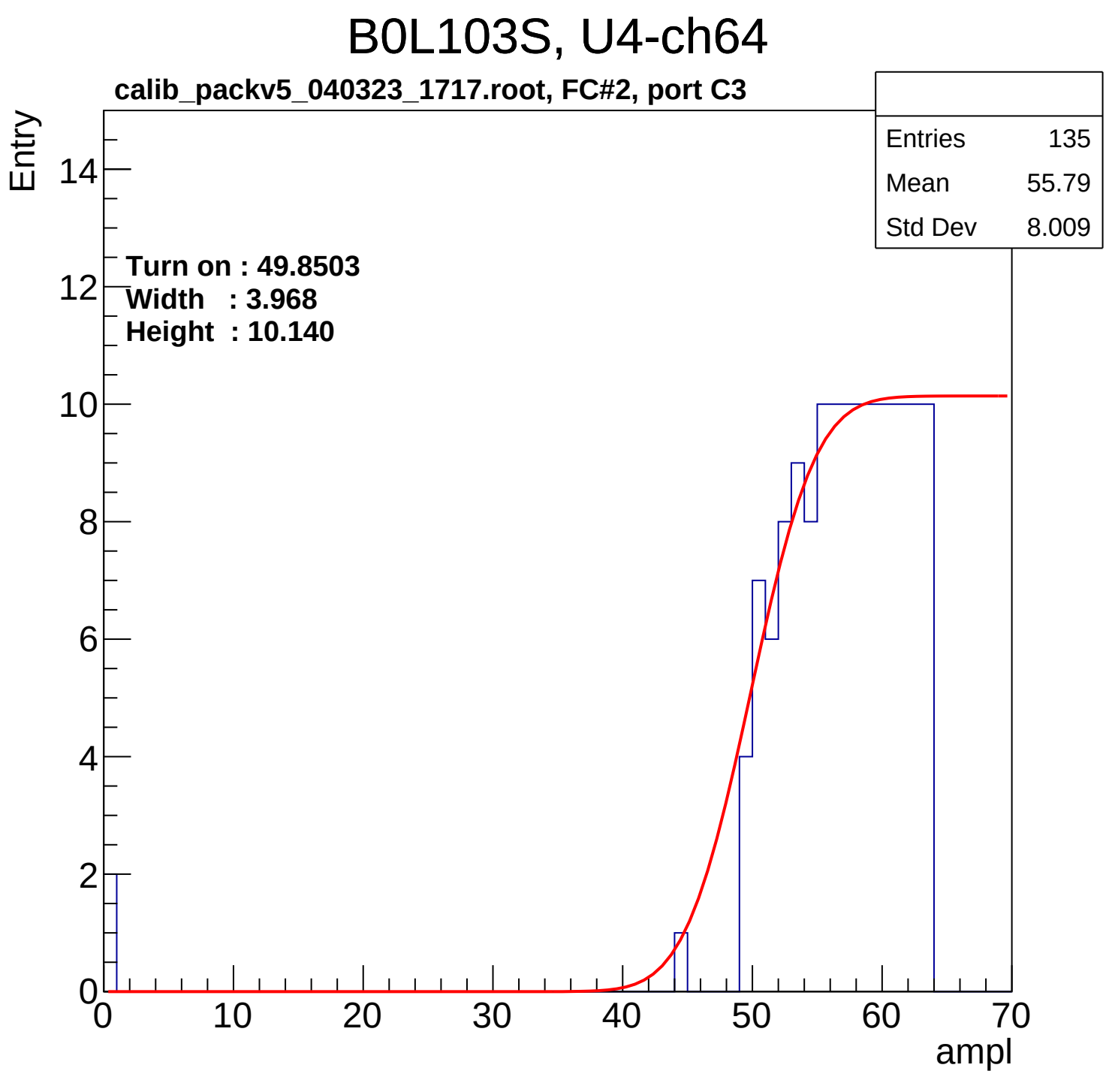
B0L103S, U4-ch64
calib_packv5_040323_1717.root, FC#2, port C3
Entries 135
Mean 55.79
Std Dev 8.009
Turn on : 49.8503
Width : 3.968
Height : 10.140
Entry
ampl
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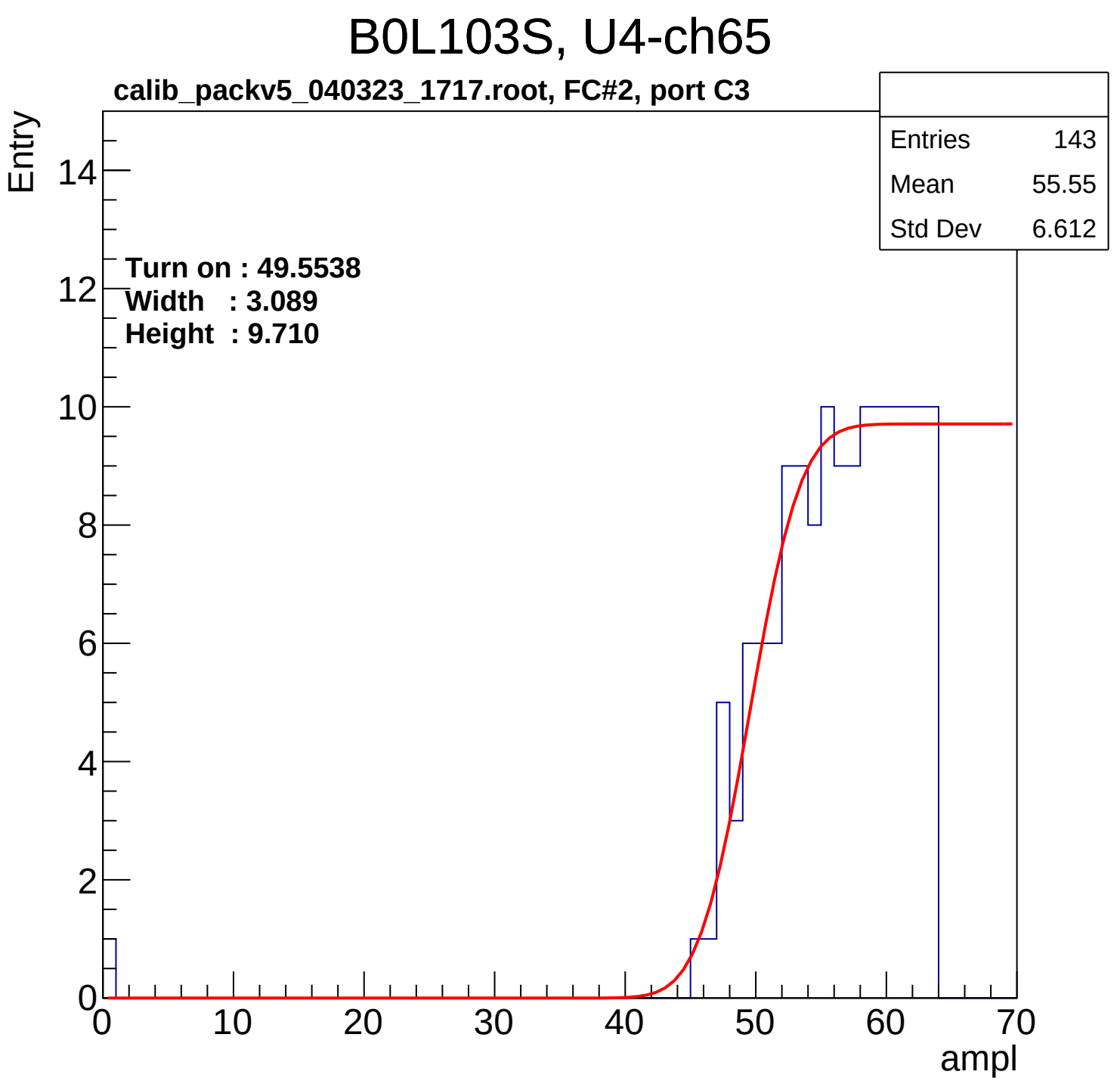
B0L103S, U4-ch65
calib_packv5_040323_1717.root, FC#2, port C3
Entries 143
Mean 55.55
Std Dev 6.612
Turn on : 49.5538
Width : 3.089
Height : 9.710
Entry
ampl
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6
8
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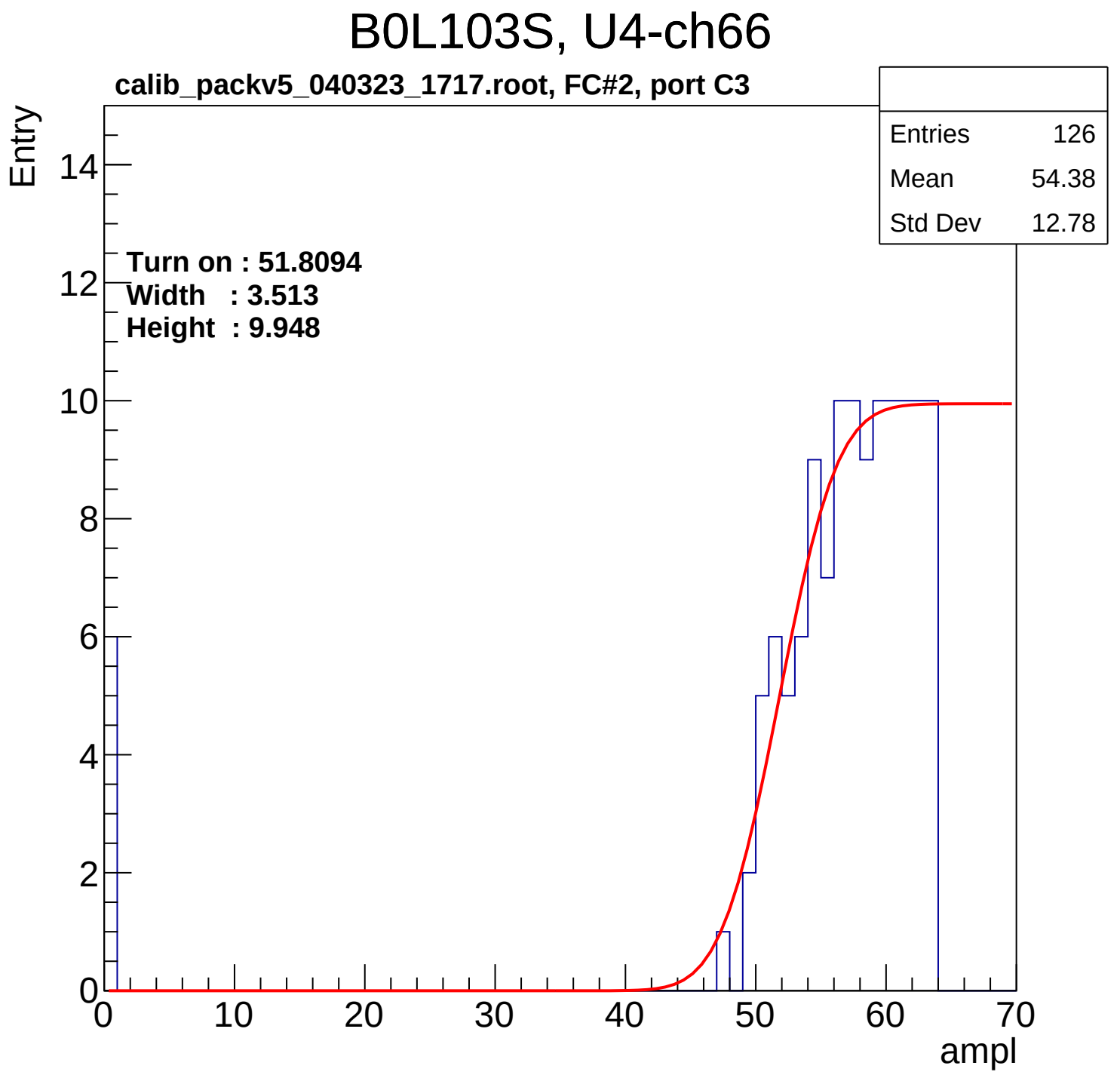
B0L103S, U4-ch66
calib_packv5_040323_1717.root, FC#2, port C3
Entries 126
Mean 54.38
Std Dev 12.78
Turn on : 51.8094
Width : 3.513
Height : 9.948
Entry
ampl
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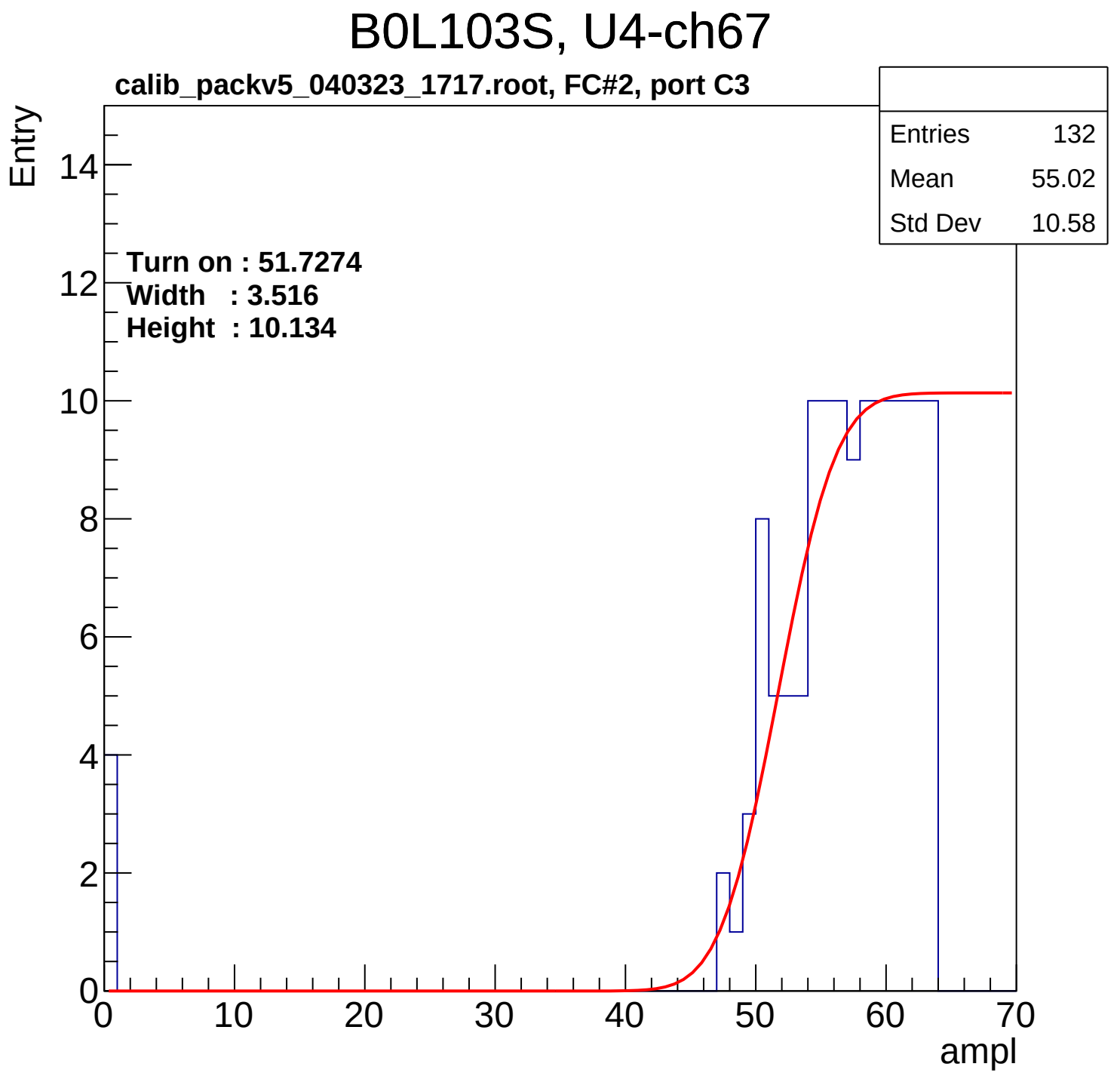
B0L103S, U4-ch67
calib_packv5_040323_1717.root, FC#2, port C3
Entries 132
Mean 55.02
Std Dev 10.58
Turn on : 51.7274
Width : 3.516
Height : 10.134
Entry
ampl
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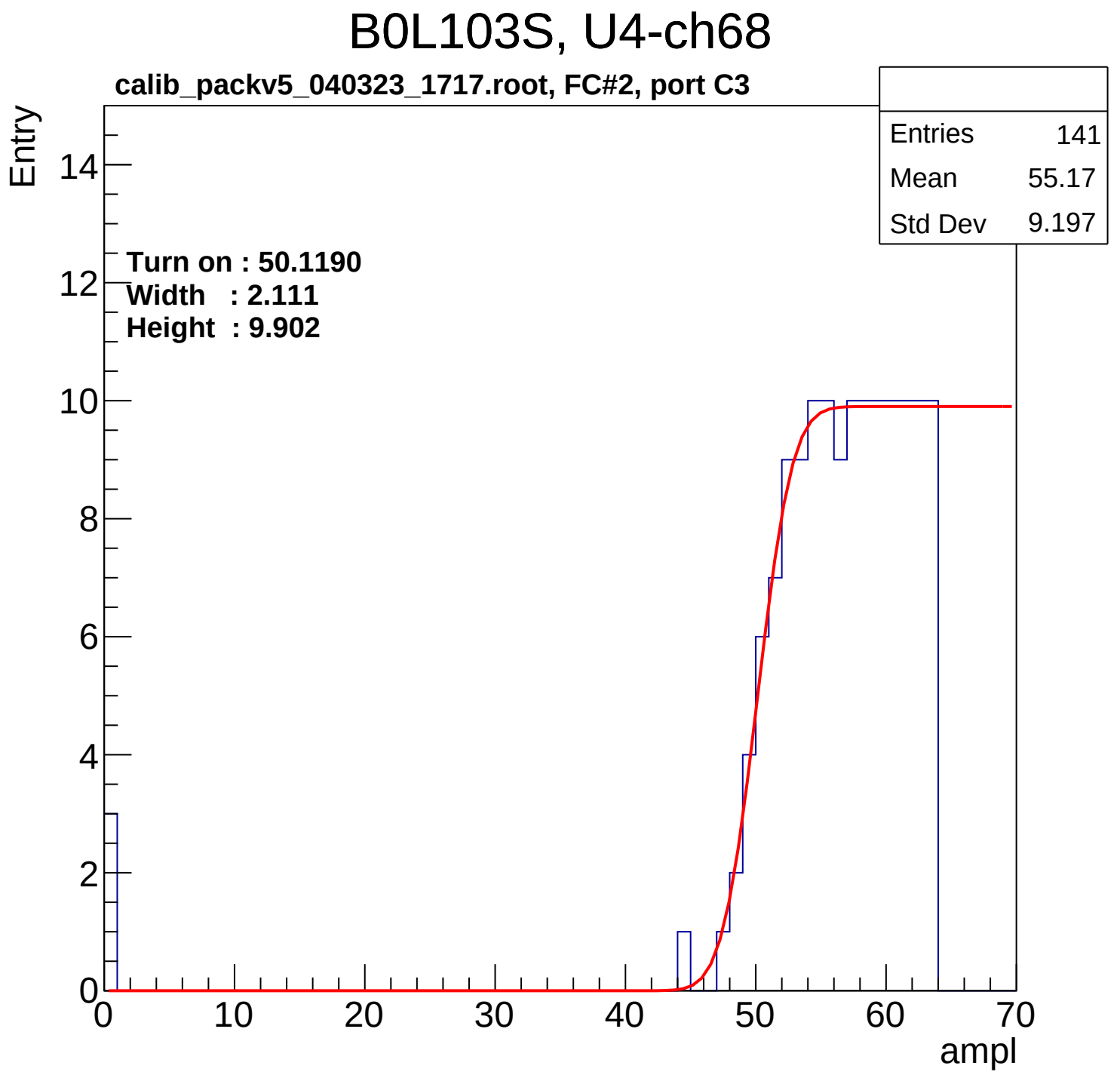
B0L103S, U4-ch68
calib_packv5_040323_1717.root, FC#2, port C3
Entries 141
Mean 55.17
Std Dev 9.197
Turn on : 50.1190
Width : 2.111
Height : 9.902
Entry
ampl
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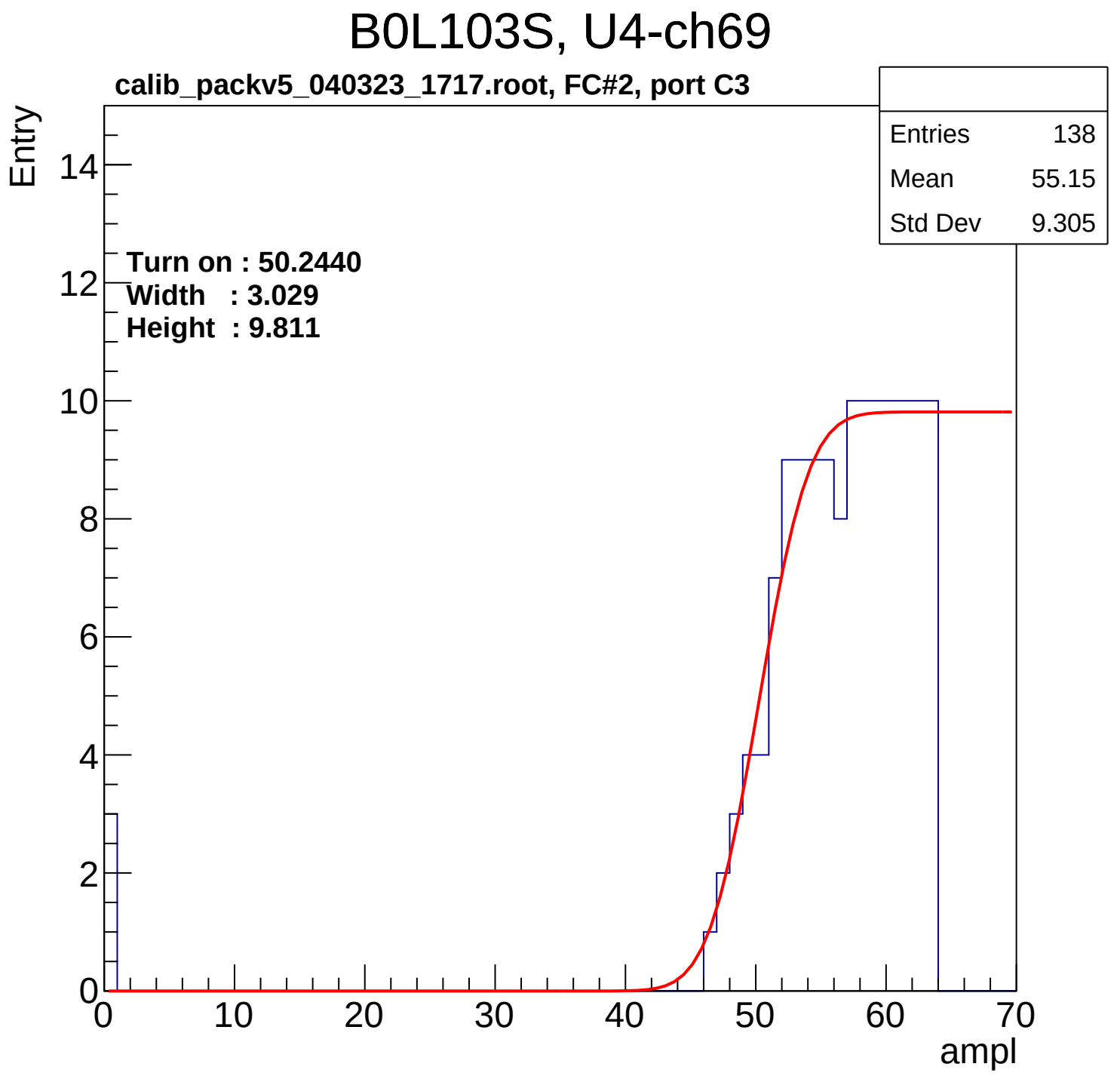
B0L103S, U4-ch69
calib_packv5_040323_1717.root, FC#2, port C3
Entries 138
Mean 55.15
Std Dev 9.305
Turn on : 50.2440
Width : 3.029
Height : 9.811
Entry
ampl
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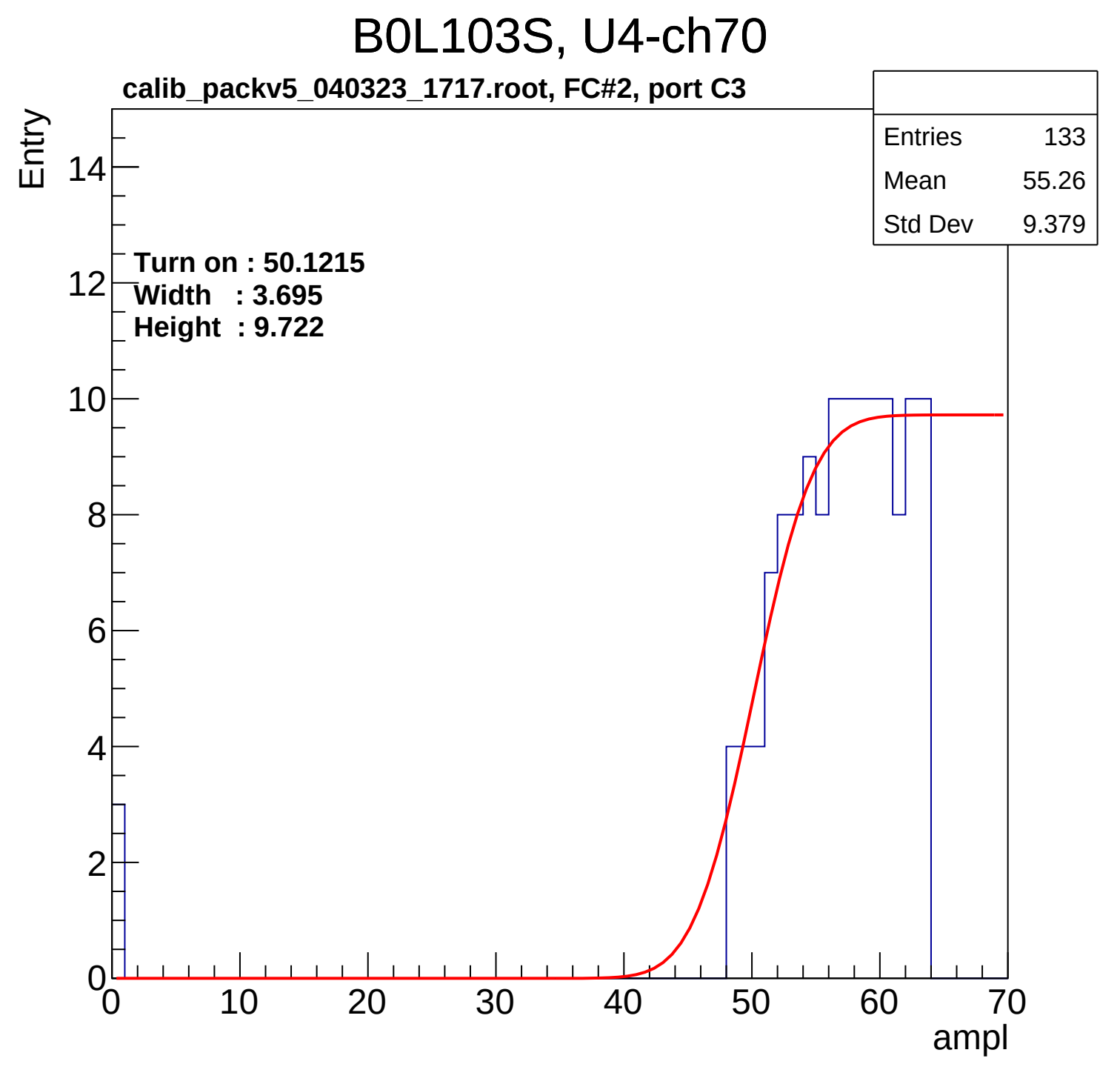
B0L103S, U4-ch70
calib_packv5_040323_1717.root, FC#2, port C3
Entries 133
Mean 55.26
Std Dev 9.379
Turn on : 50.1215
Width : 3.695
Height : 9.722
Entry
ampl
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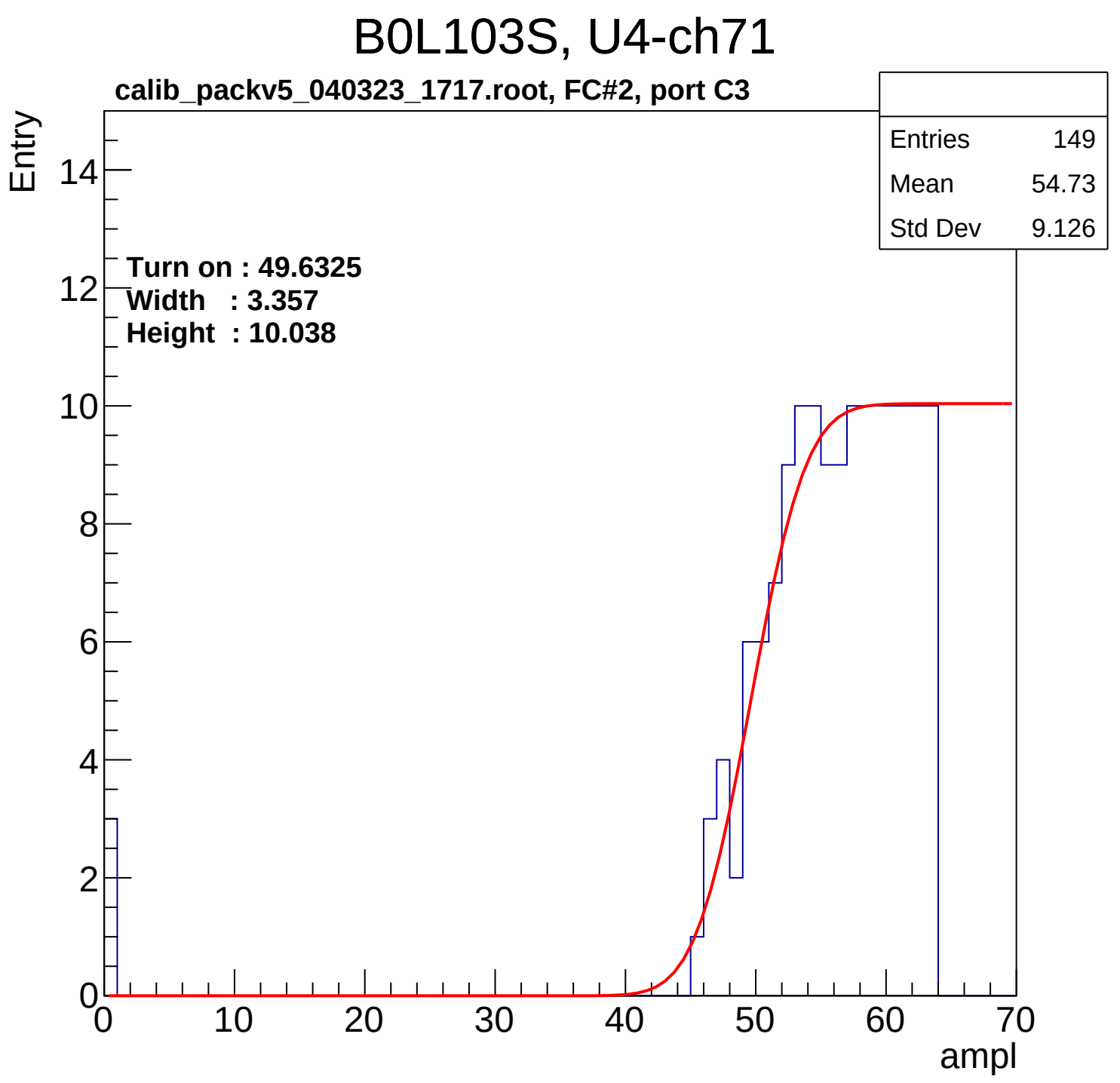
B0L103S, U4-ch71
calib_packv5_040323_1717.root, FC#2, port C3
Entries 149
Mean 54.73
Std Dev 9.126
Turn on : 49.6325
Width : 3.357
Height : 10.038
Entry
ampl
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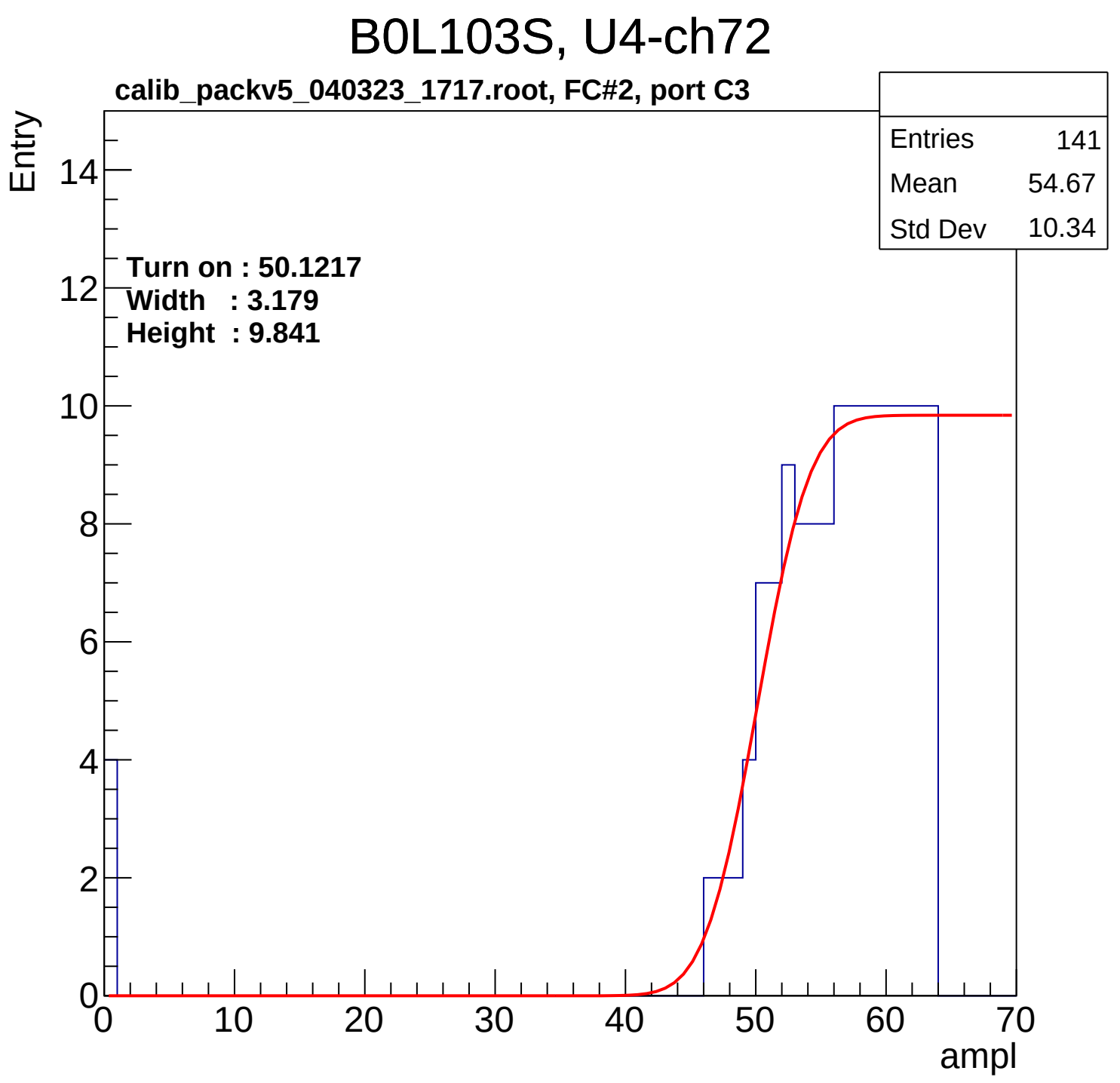
B0L103S, U4-ch72
calib_packv5_040323_1717.root, FC#2, port C3
Entries 141
Mean 54.67
Std Dev 10.34
Turn on : 50.1217
Width : 3.179
Height : 9.841
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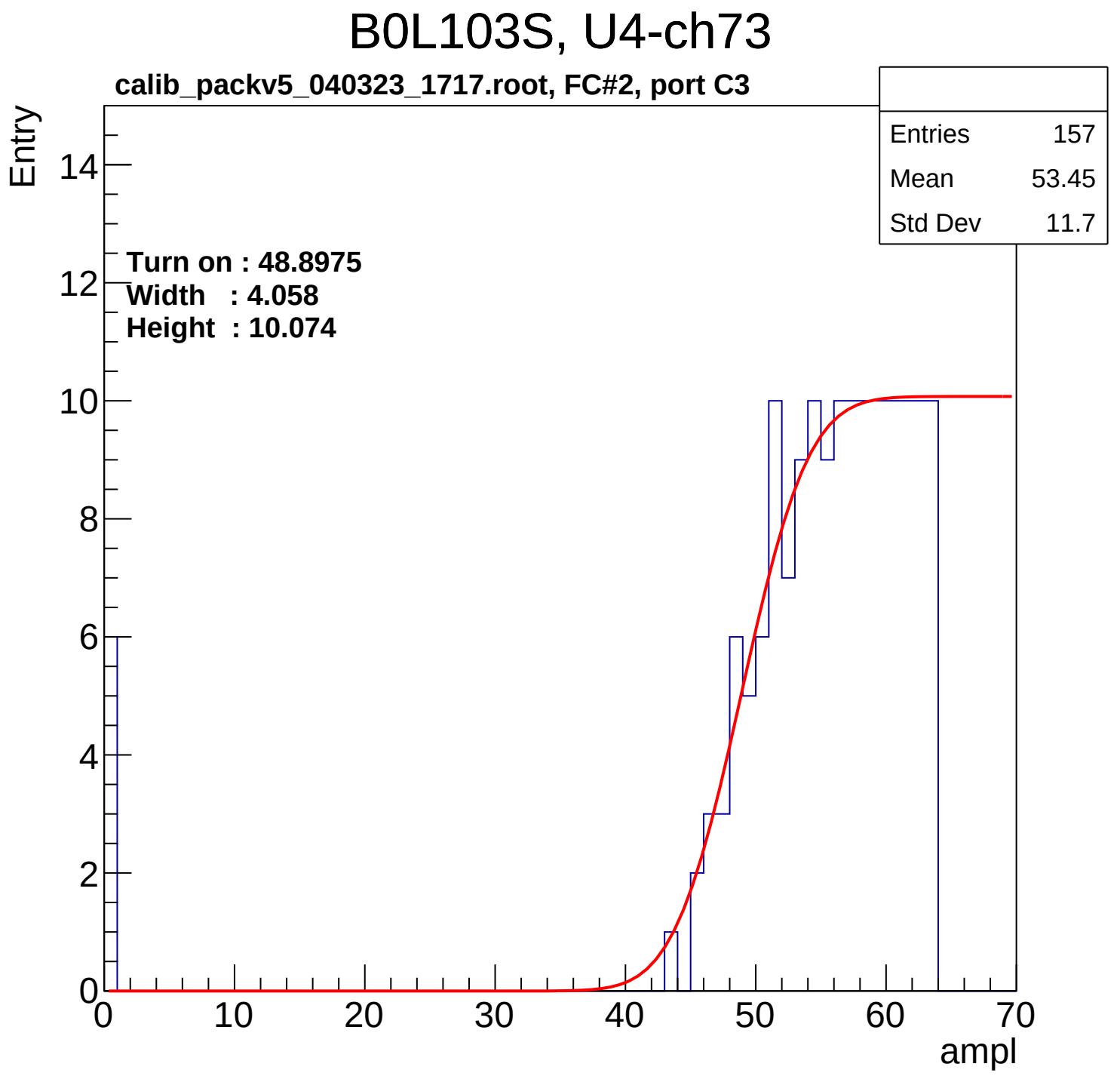
B0L103S, U4-ch73
calib_packv5_040323_1717.root, FC#2, port C3
Entries 157
Mean 53.45
Std Dev 11.7
Turn on : 48.8975
Width : 4.058
Height : 10.074
Entry
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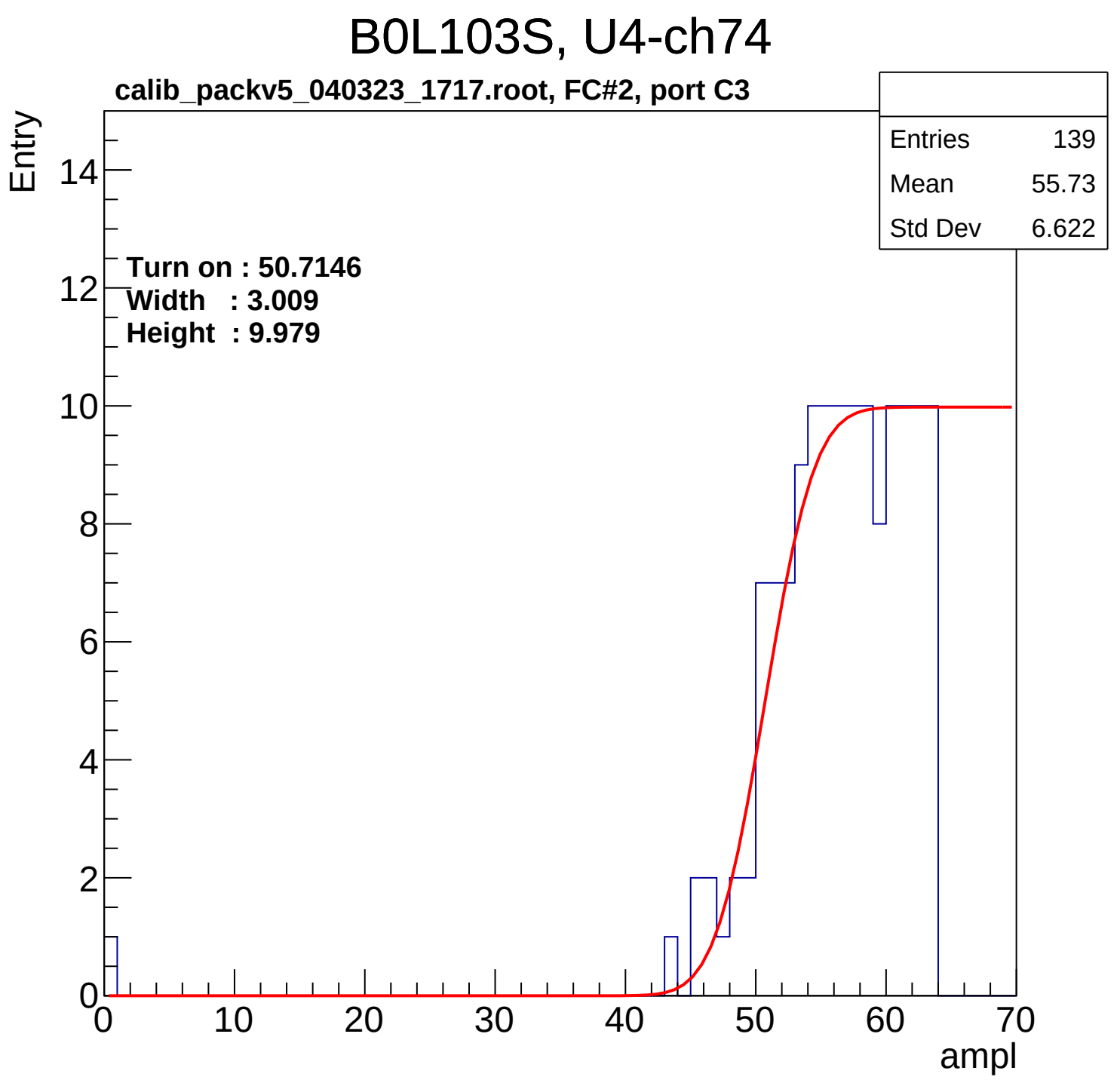
B0L103S, U4-ch74
calib_packv5_040323_1717.root, FC#2, port C3
Entries 139
Mean 55.73
Std Dev 6.622
Turn on : 50.7146
Width : 3.009
Height : 9.979
Entry
ampl
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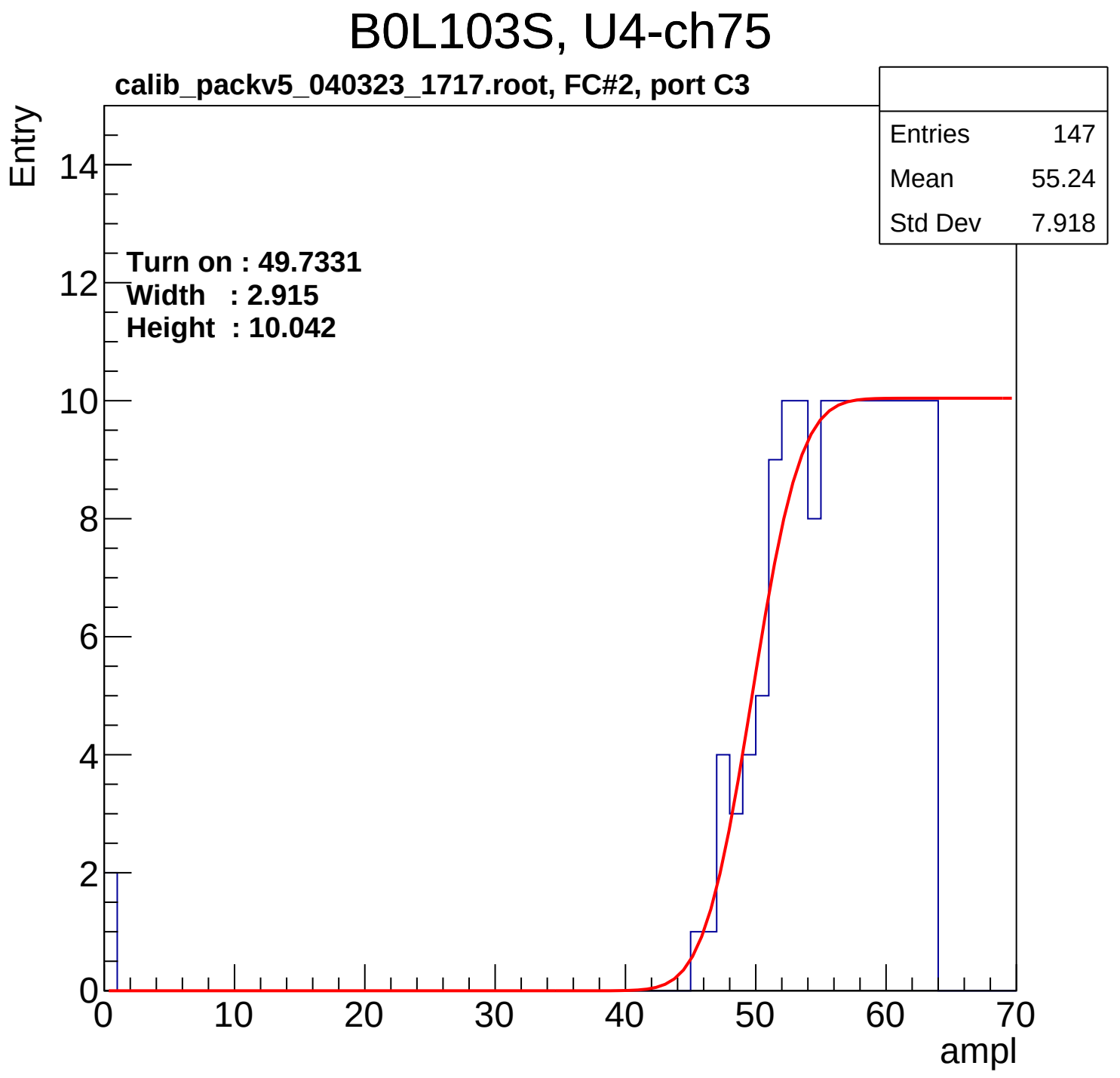
B0L103S, U4-ch75
calib_packv5_040323_1717.root, FC#2, port C3
Entries 147
Mean 55.24
Std Dev 7.918
Turn on : 49.7331
Width : 2.915
Height : 10.042
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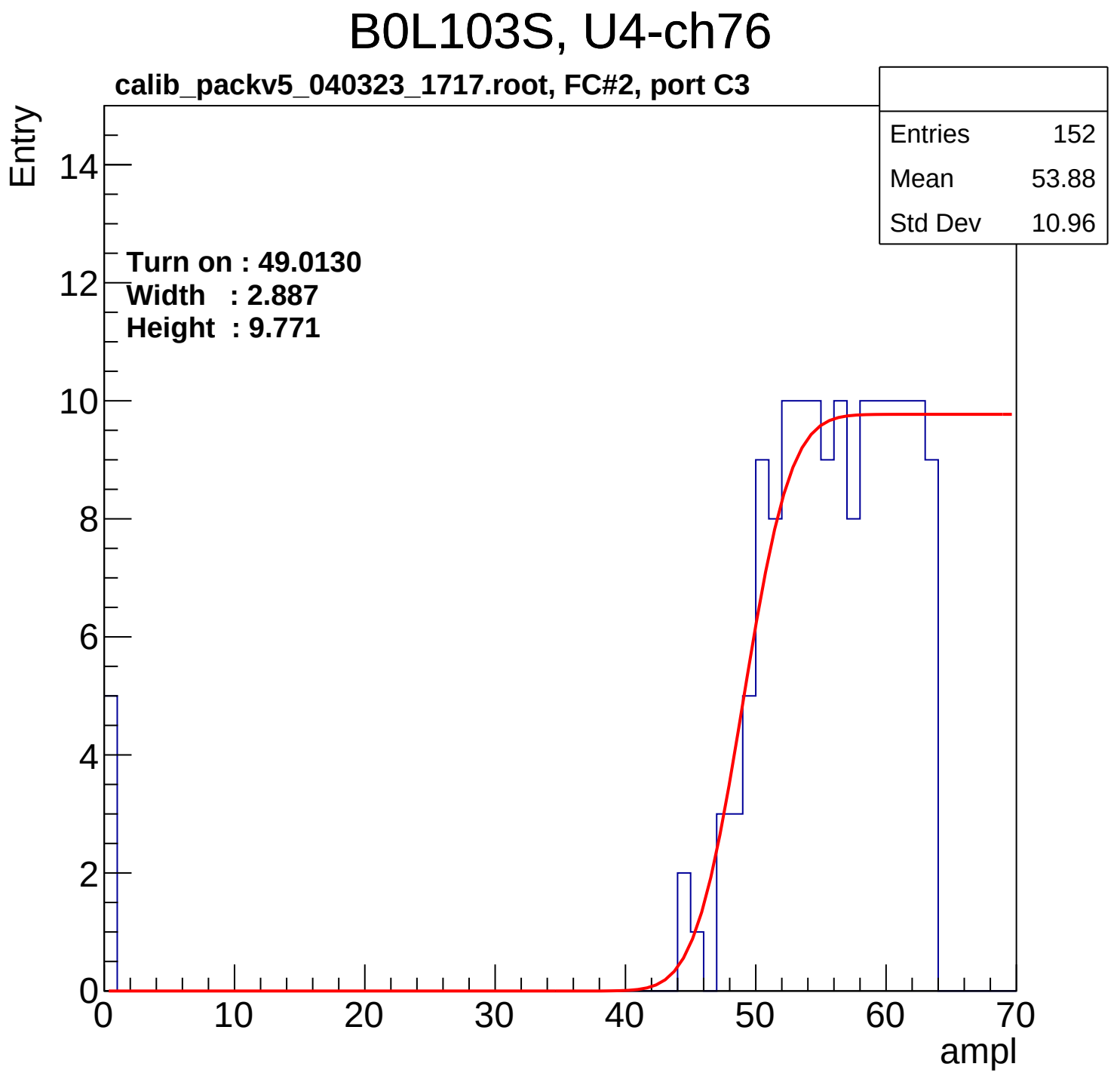
B0L103S, U4-ch76
calib_packv5_040323_1717.root, FC#2, port C3
Entries 152
Mean 53.88
Std Dev 10.96
Turn on : 49.0130
Width : 2.887
Height : 9.771
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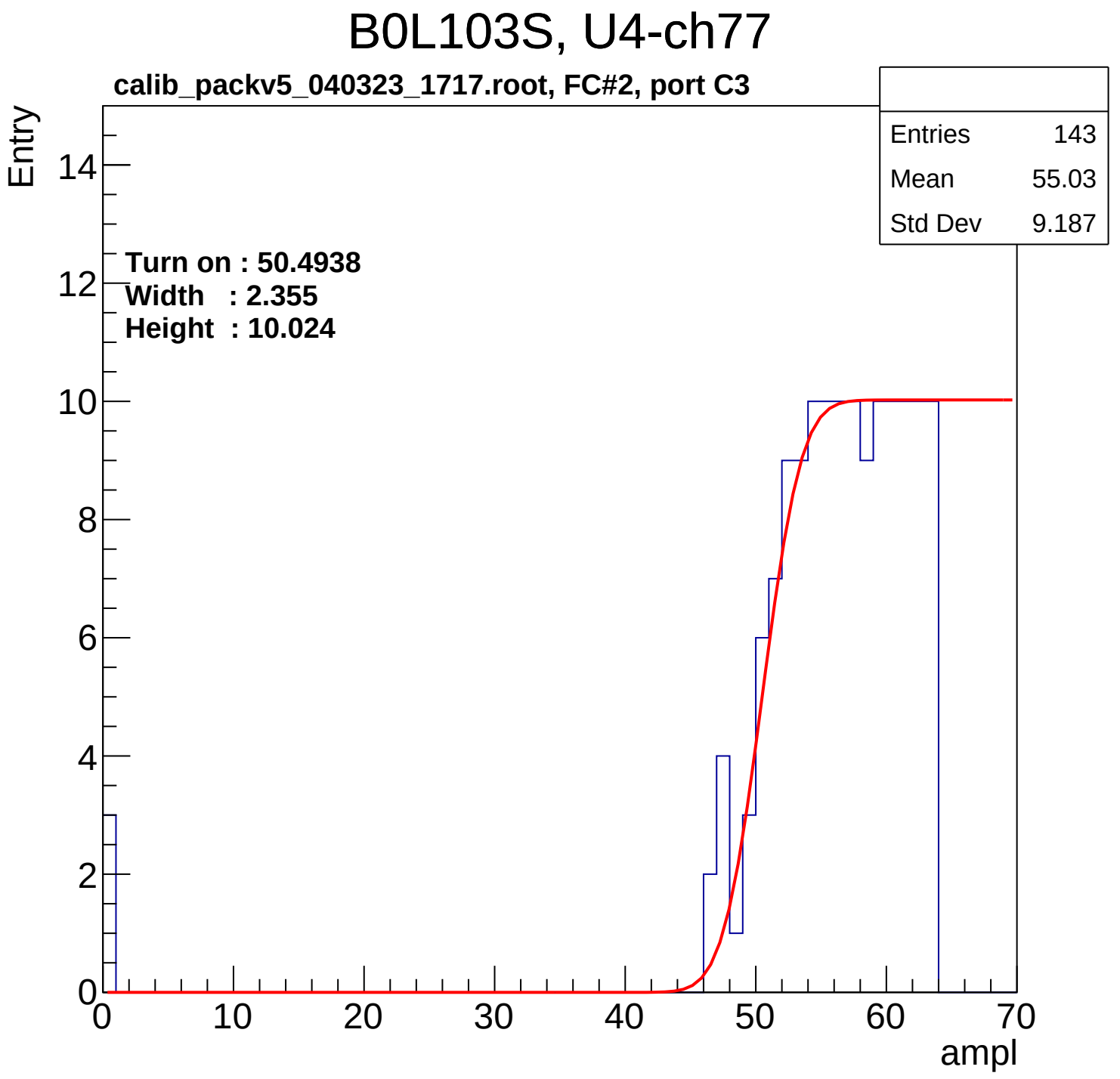
B0L103S, U4-ch77
calib_packv5_040323_1717.root, FC#2, port C3
Entries 143
Mean 55.03
Std Dev 9.187
Turn on : 50.4938
Width : 2.355
Height : 10.024
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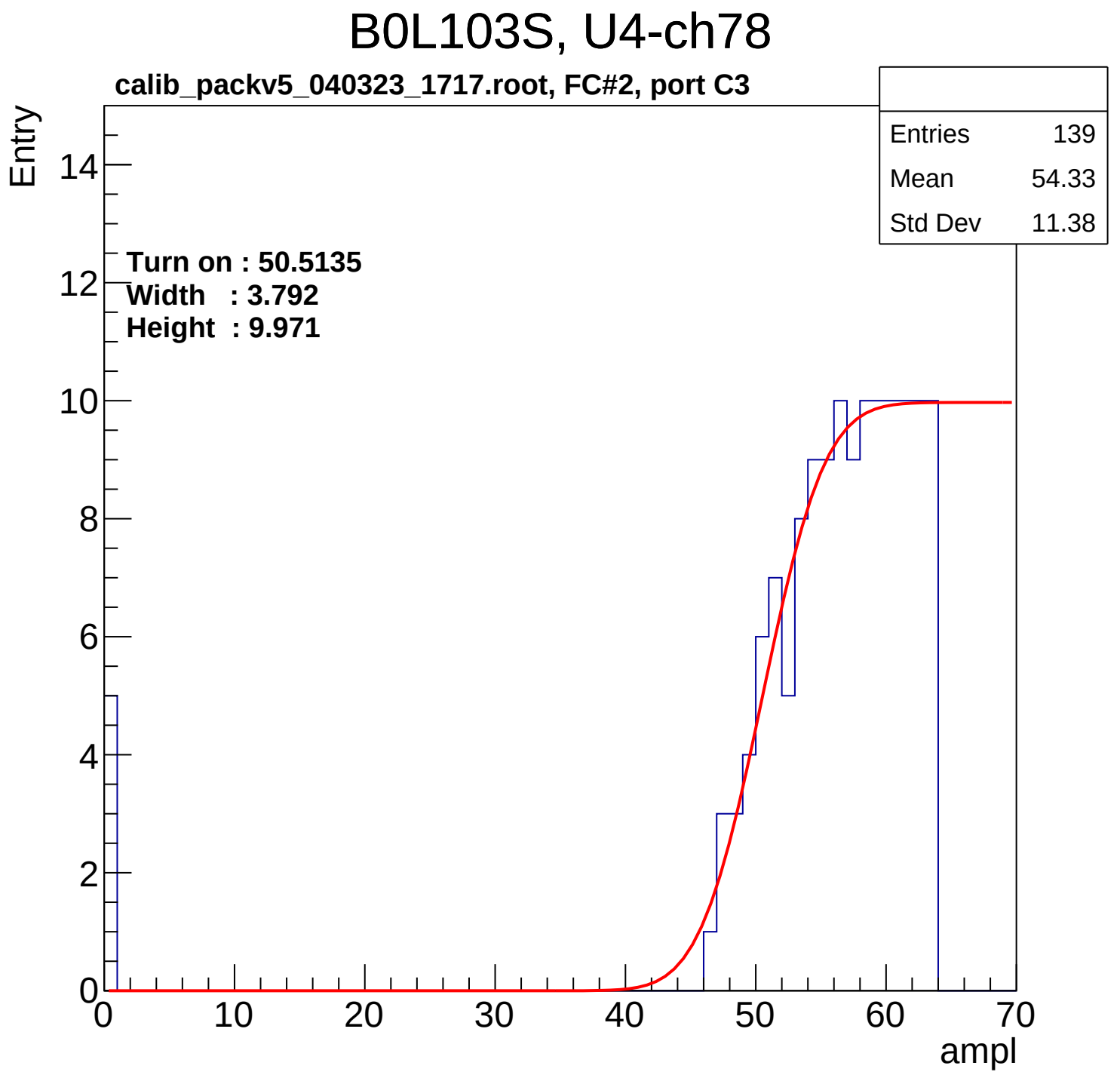
B0L103S, U4-ch78
calib_packv5_040323_1717.root, FC#2, port C3
Entries 139
Mean 54.33
Std Dev 11.38
Turn on : 50.5135
Width : 3.792
Height : 9.971
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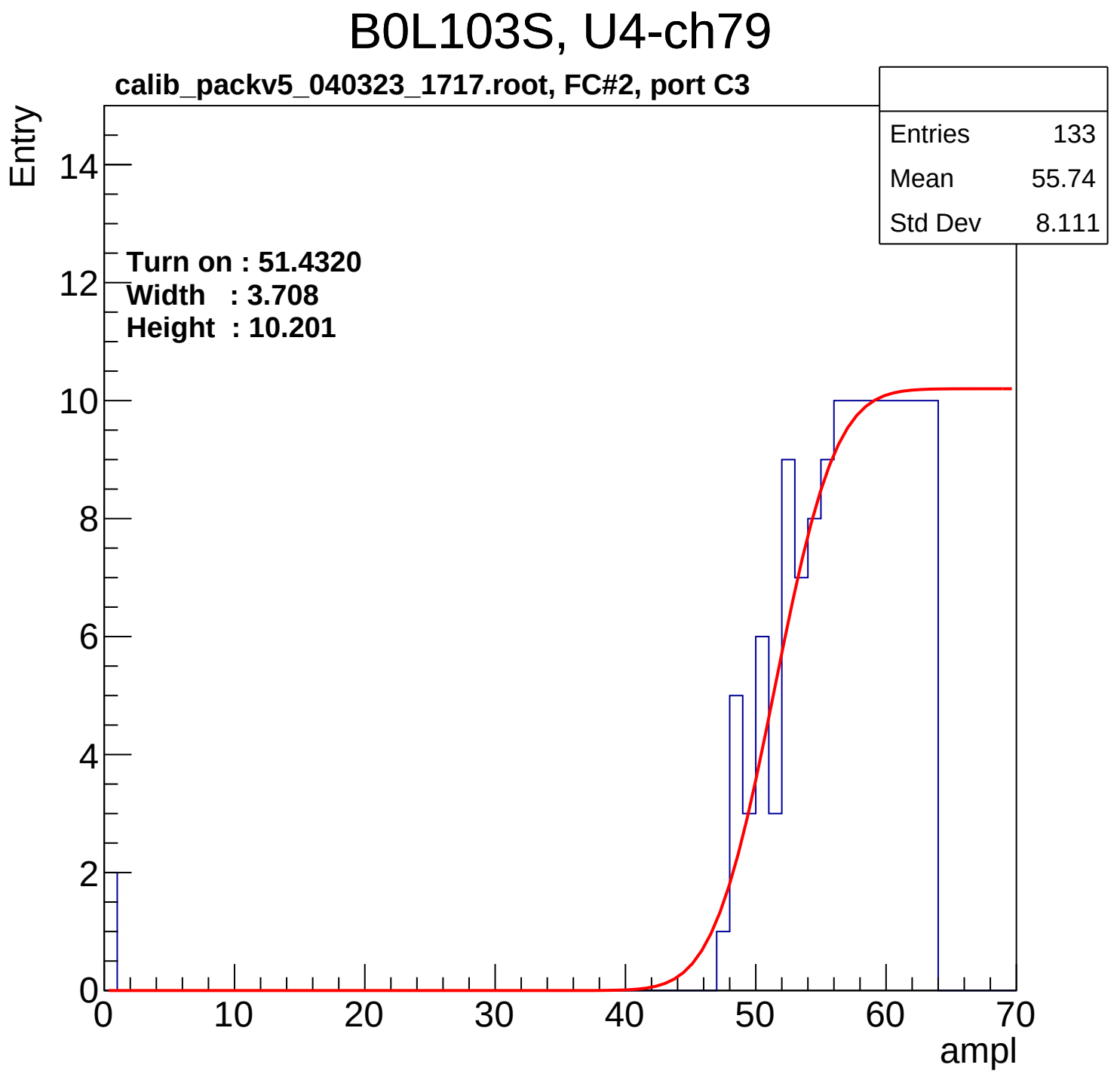
B0L103S, U4-ch79
calib_packv5_040323_1717.root, FC#2, port C3
Entries 133
Mean 55.74
Std Dev 8.111
Turn on : 51.4320
Width : 3.708
Height : 10.201
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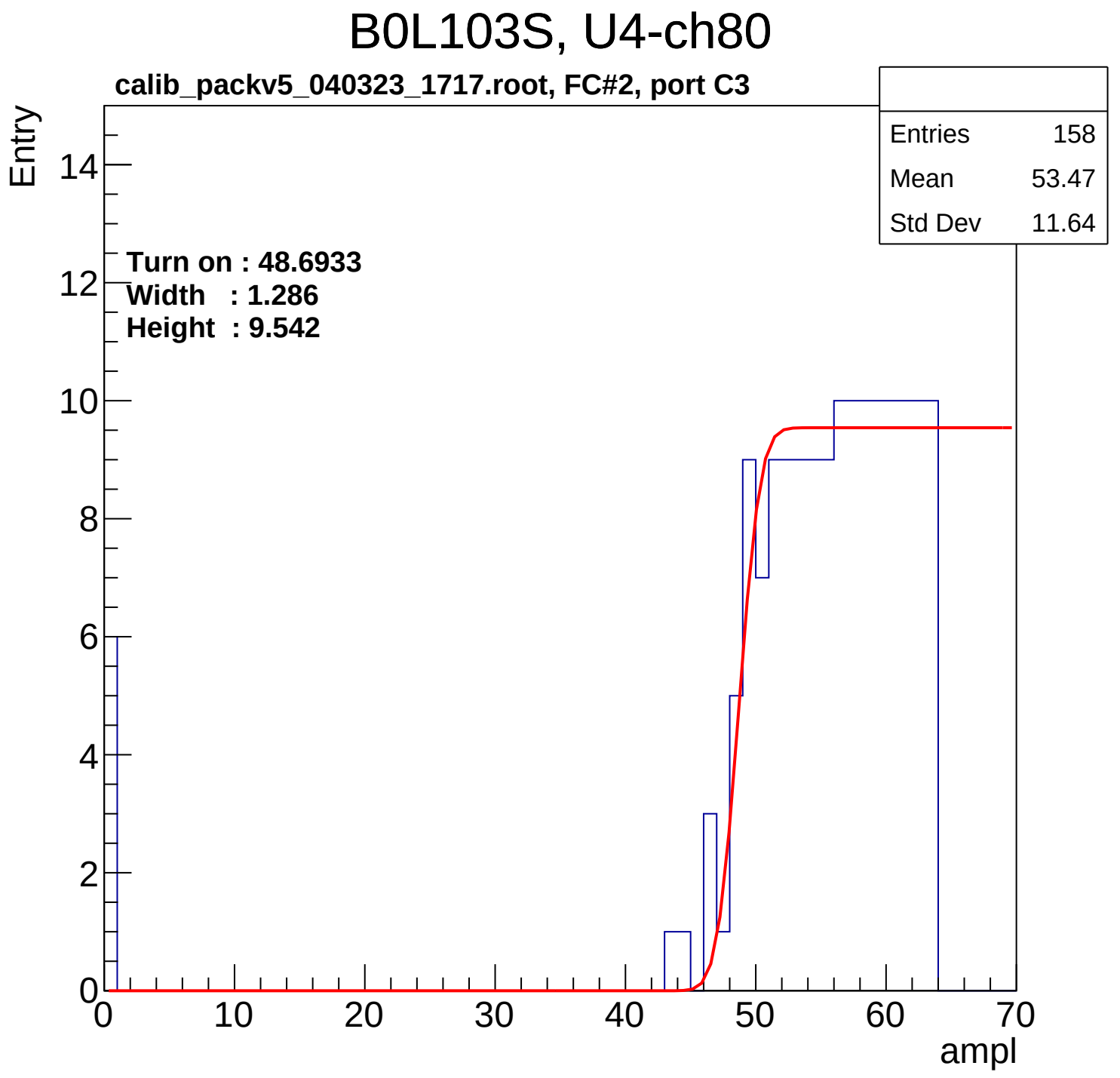
B0L103S, U4-ch80
calib_packv5_040323_1717.root, FC#2, port C3
Entries 158
Mean 53.47
Std Dev 11.64
Turn on : 48.6933
Width : 1.286
Height : 9.542
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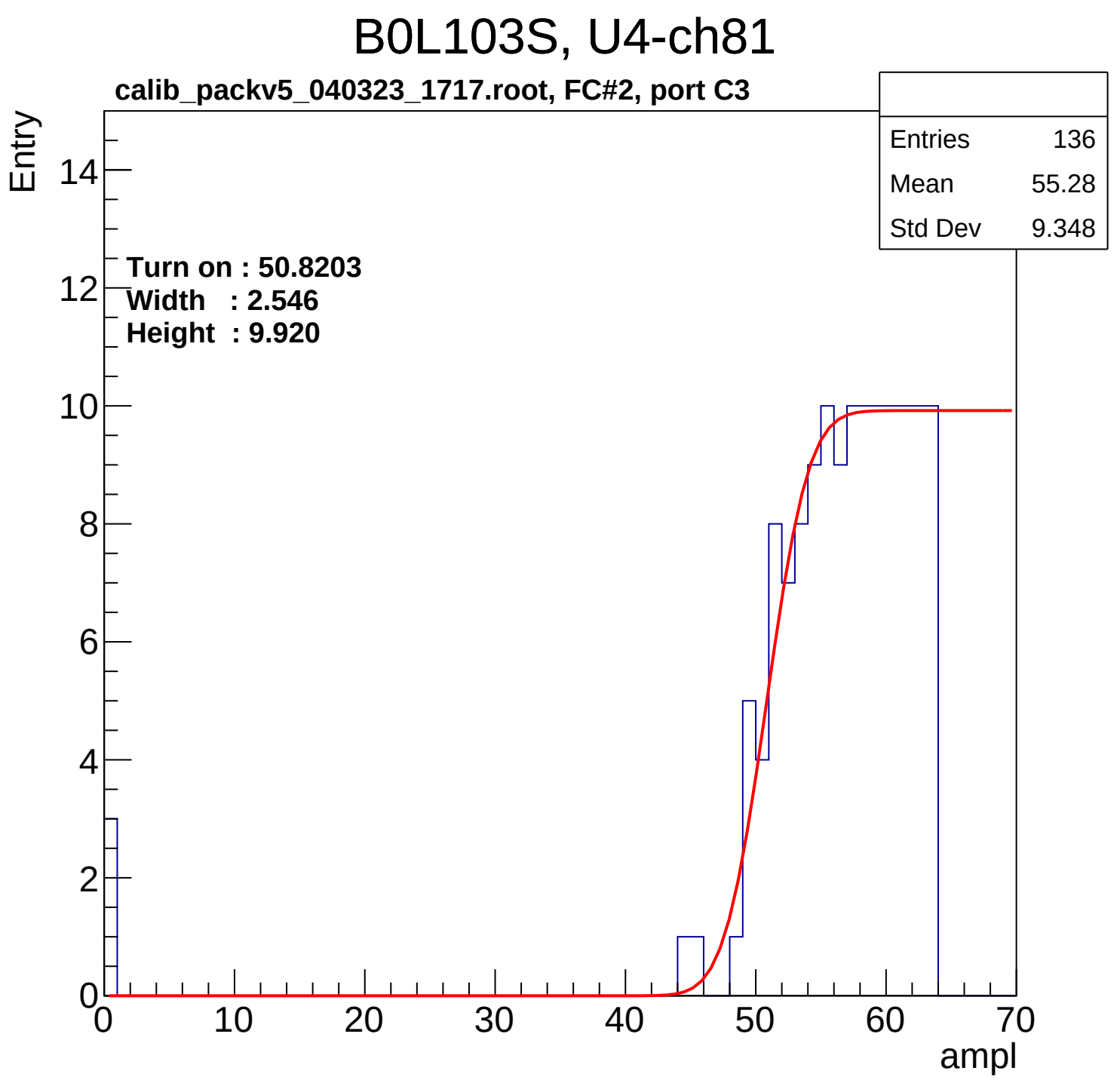
B0L103S, U4-ch81
calib_packv5_040323_1717.root, FC#2, port C3
Entries 136
Mean 55.28
Std Dev 9.348
Turn on : 50.8203
Width : 2.546
Height : 9.920
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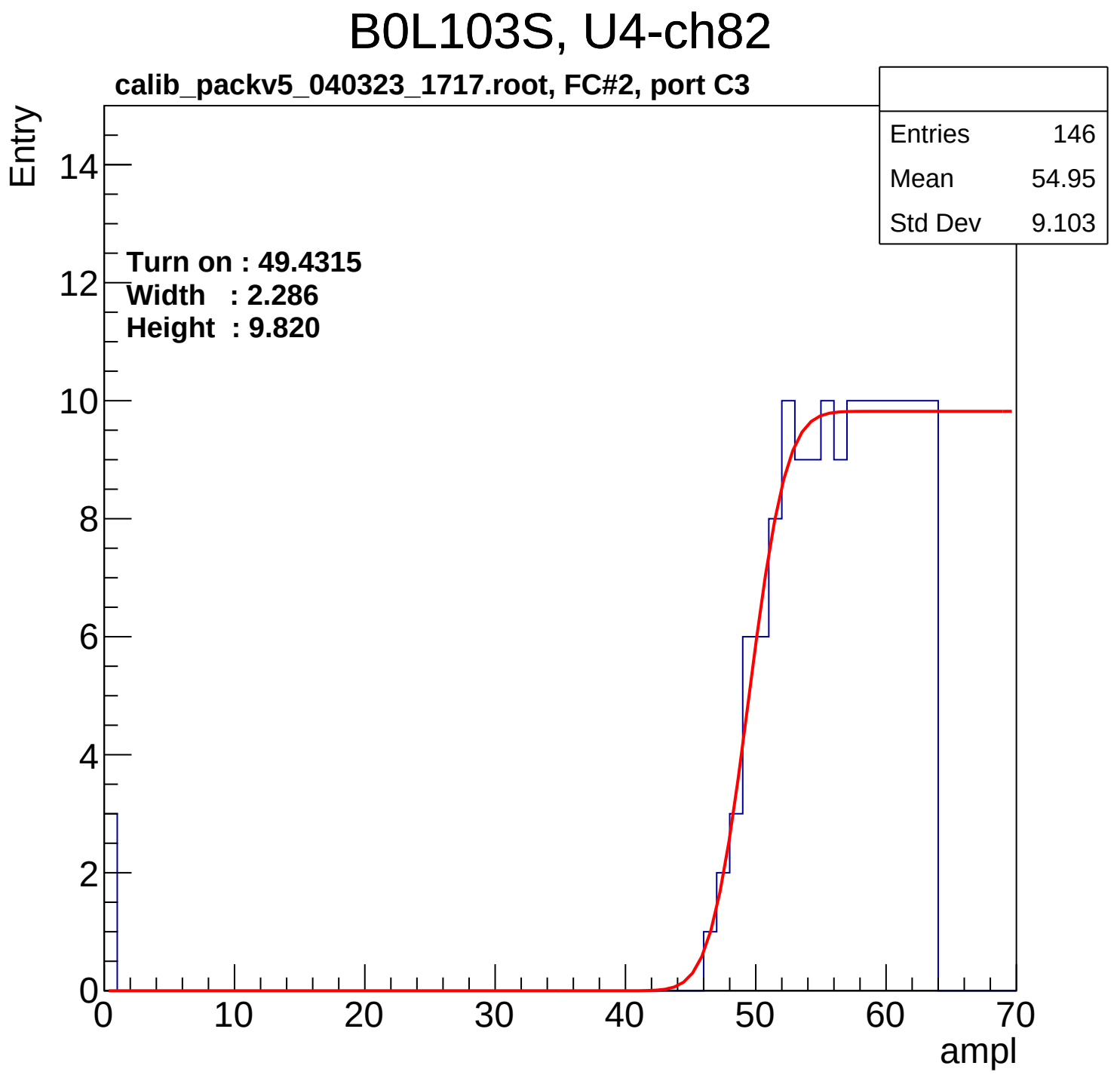
B0L103S, U4-ch82
calib_packv5_040323_1717.root, FC#2, port C3
Entries 146
Mean 54.95
Std Dev 9.103
Turn on : 49.4315
Width : 2.286
Height : 9.820
Entry
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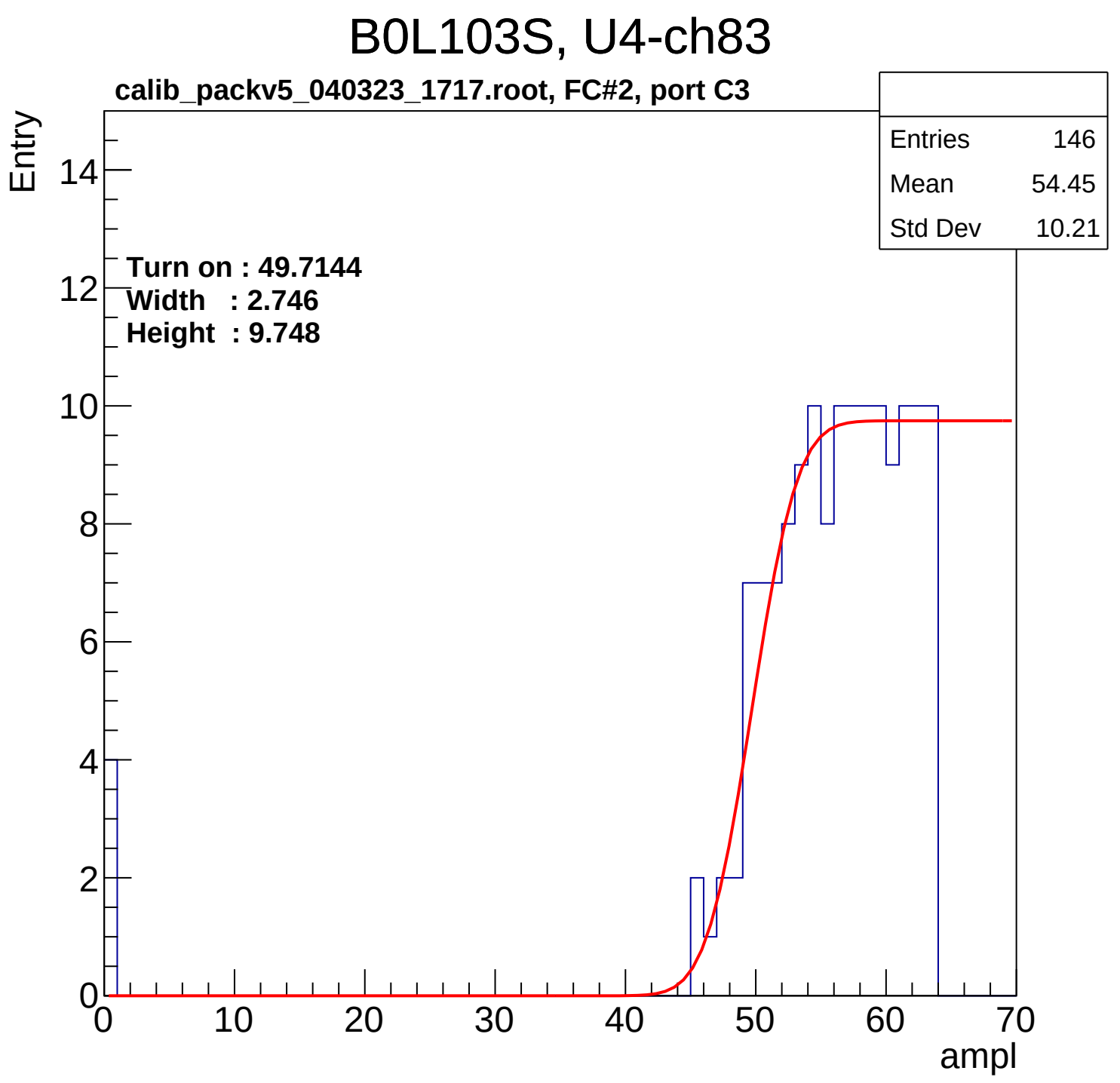
B0L103S, U4-ch83
calib_packv5_040323_1717.root, FC#2, port C3
Entries 146
Mean 54.45
Std Dev 10.21
Turn on : 49.7144
Width : 2.746
Height : 9.748
Entry
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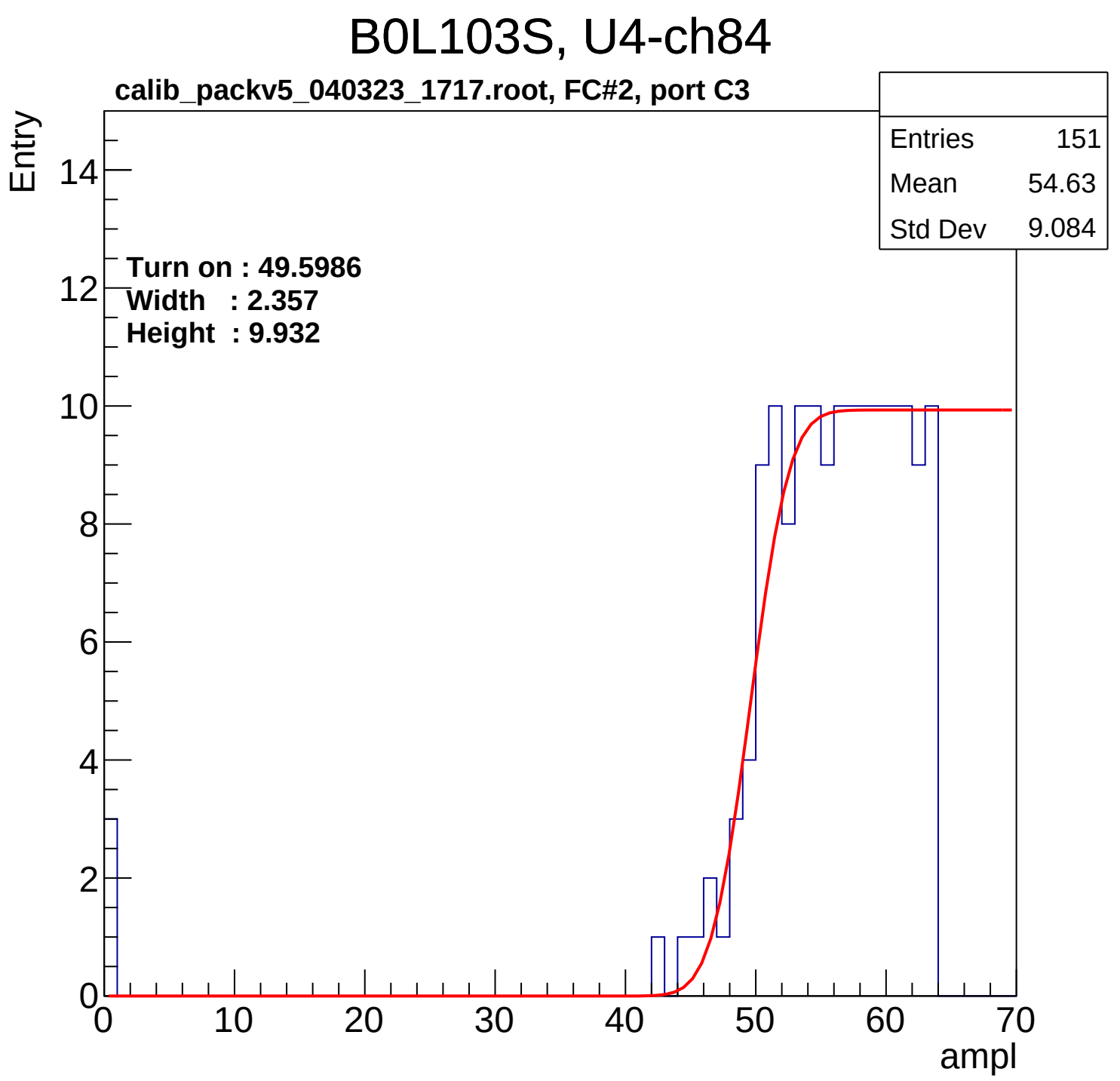
B0L103S, U4-ch84
calib_packv5_040323_1717.root, FC#2, port C3
Entries 151
Mean 54.63
Std Dev 9.084
Turn on : 49.5986
Width : 2.357
Height : 9.932
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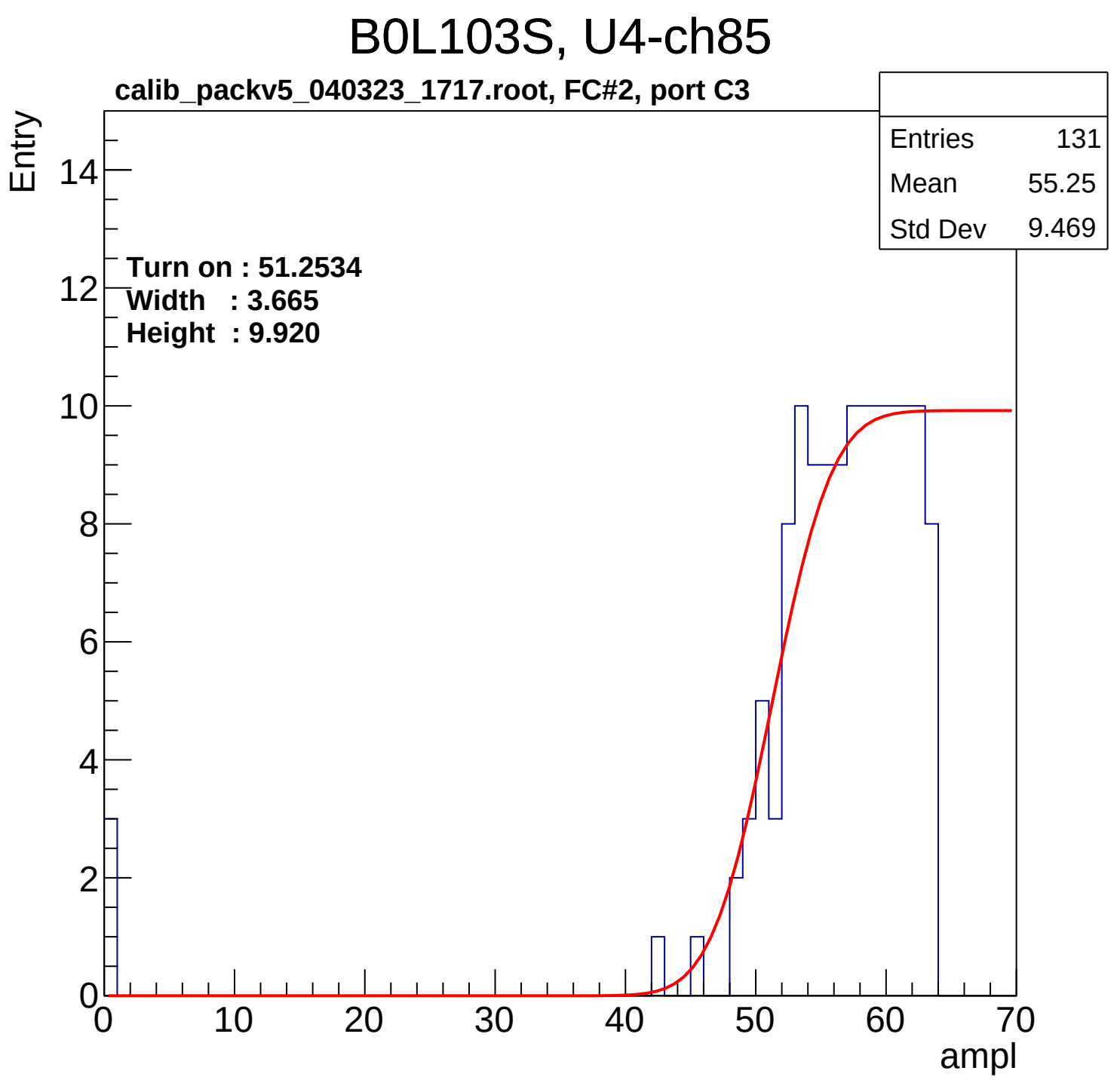
B0L103S, U4-ch85
calib_packv5_040323_1717.root, FC#2, port C3
Entries 131
Mean 55.25
Std Dev 9.469
Turn on : 51.2534
Width : 3.665
Height : 9.920
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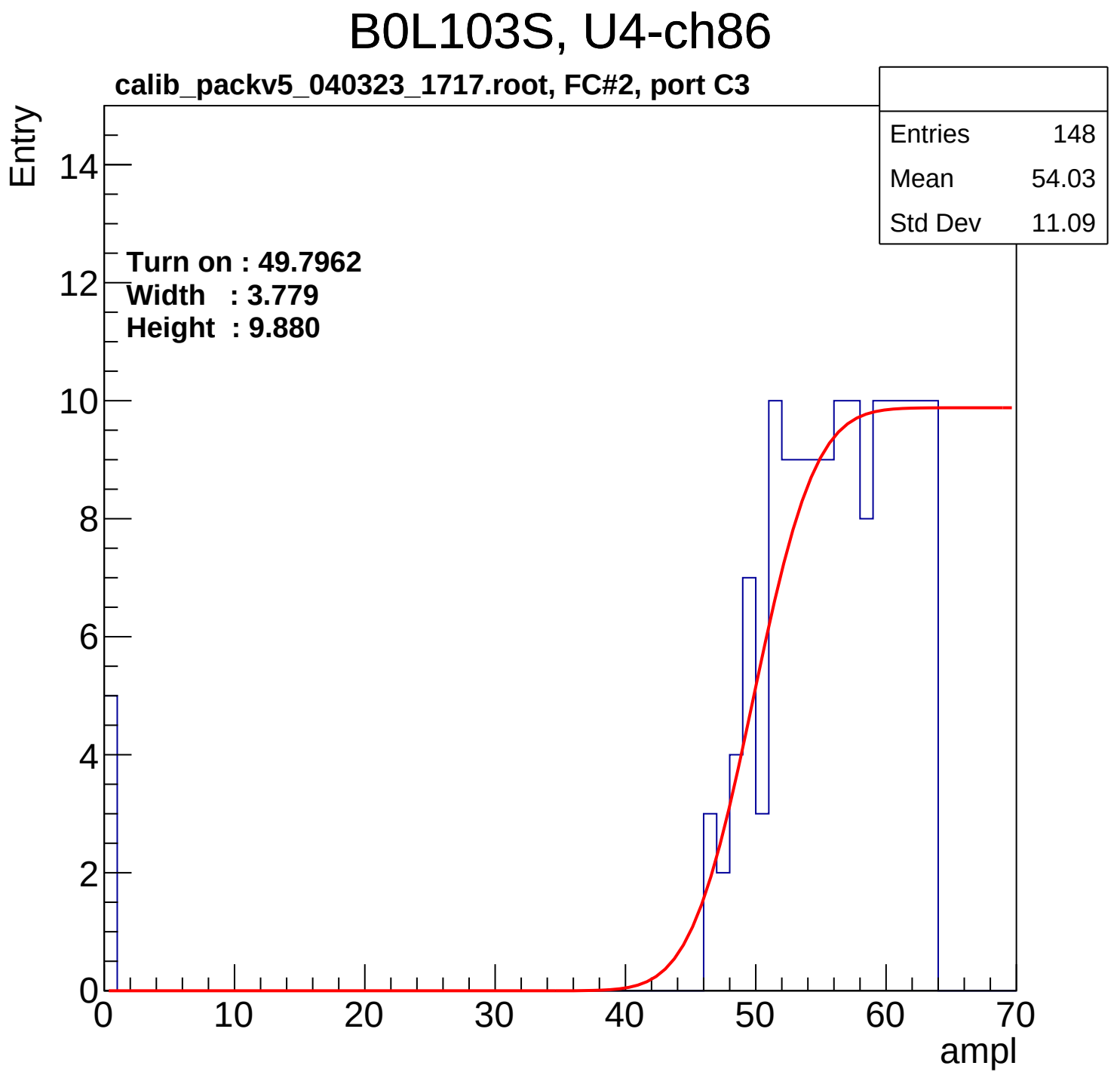
B0L103S, U4-ch86
calib_packv5_040323_1717.root, FC#2, port C3
Entries 148
Mean 54.03
Std Dev 11.09
Turn on : 49.7962
Width : 3.779
Height : 9.880
Entry
ampl
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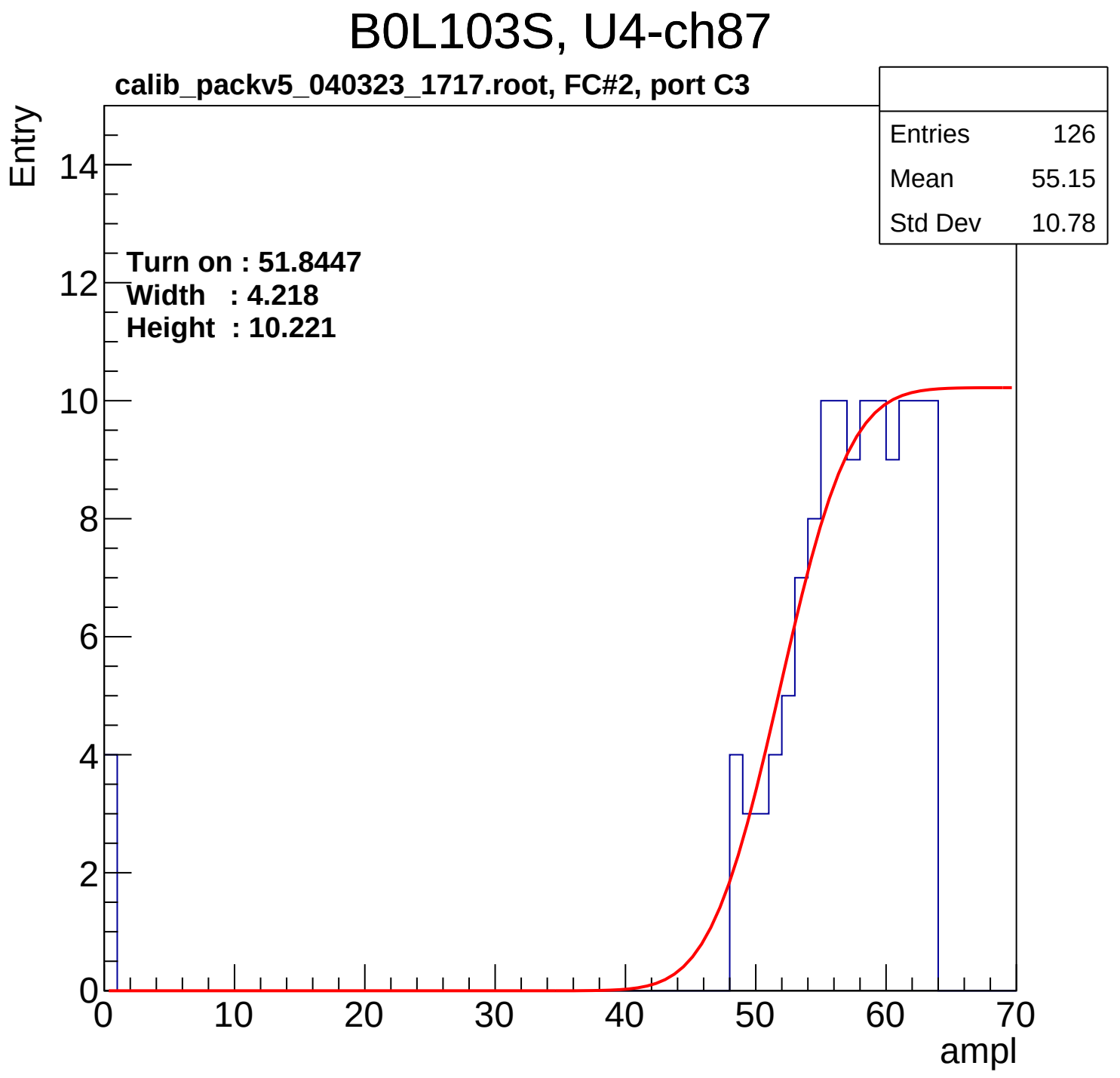
B0L103S, U4-ch87
calib_packv5_040323_1717.root, FC#2, port C3
Entries 126
Mean 55.15
Std Dev 10.78
Turn on : 51.8447
Width : 4.218
Height : 10.221
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ampl
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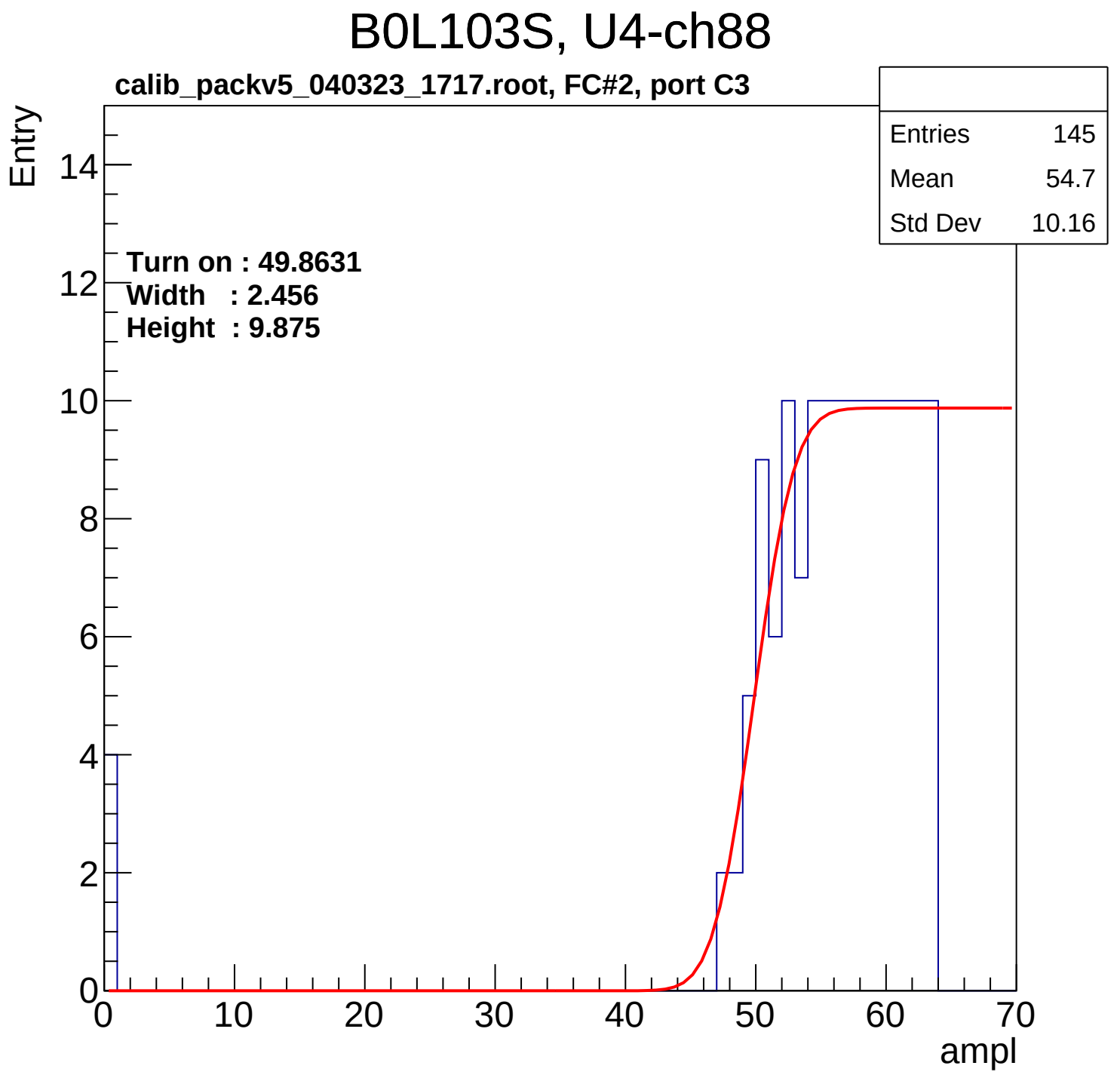
B0L103S, U4-ch88
calib_packv5_040323_1717.root, FC#2, port C3
Entries 145
Mean 54.7
Std Dev 10.16
Turn on : 49.8631
Width : 2.456
Height : 9.875
Entry
ampl
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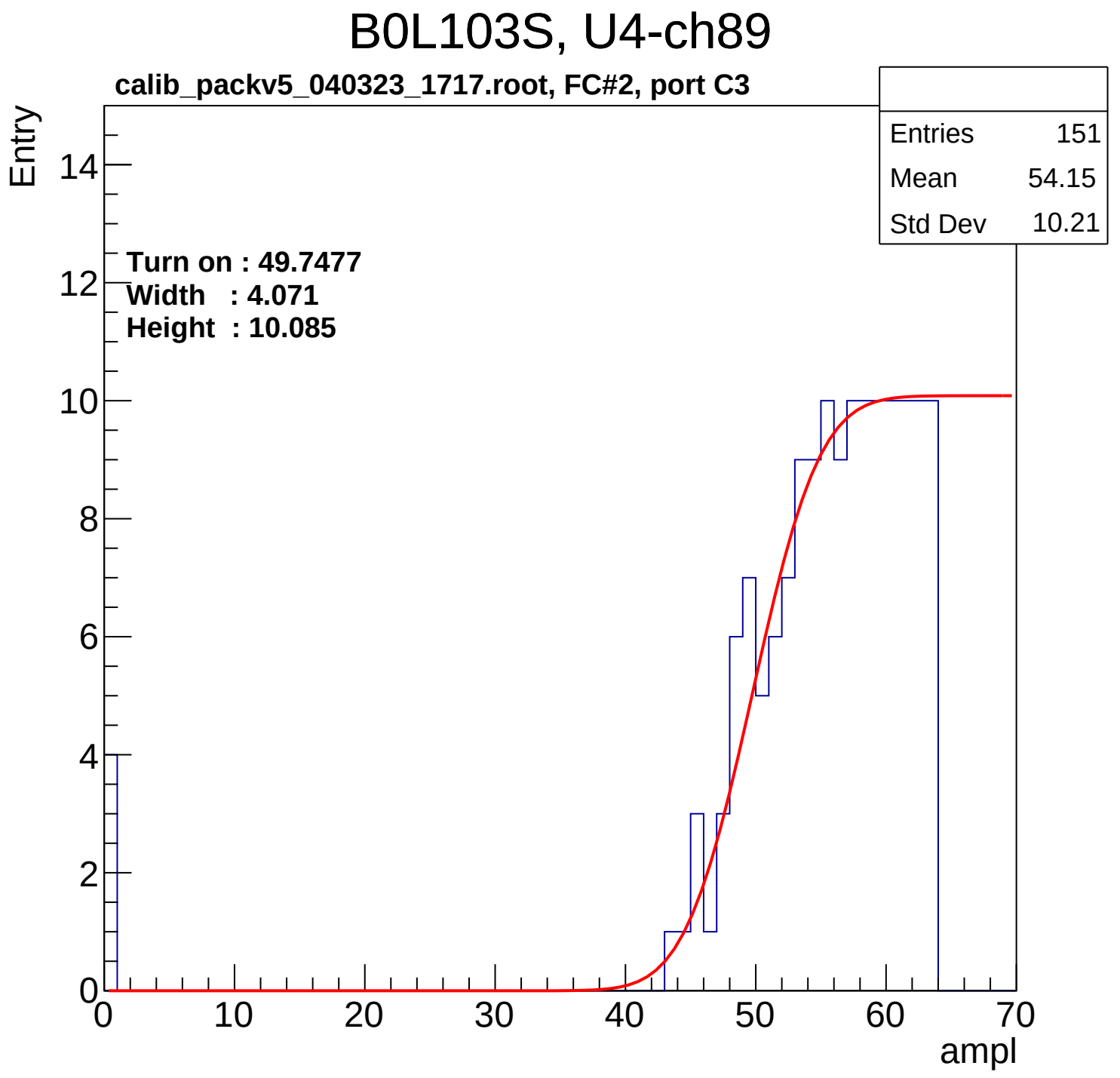
B0L103S, U4-ch89
calib_packv5_040323_1717.root, FC#2, port C3
Entries 151
Mean 54.15
Std Dev 10.21
Turn on : 49.7477
Width : 4.071
Height : 10.085
Entry
ampl
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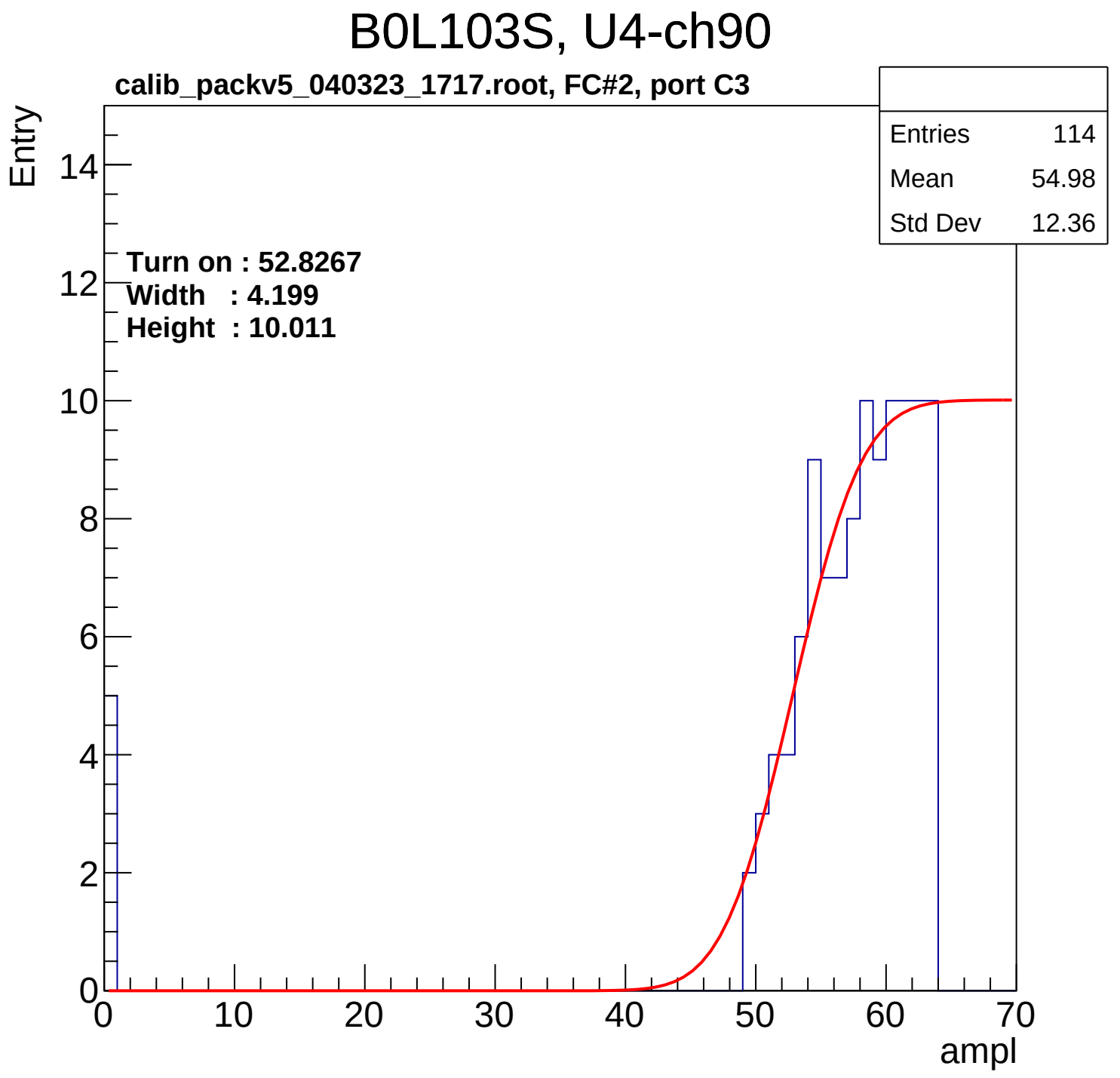
B0L103S, U4-ch90
calib_packv5_040323_1717.root, FC#2, port C3
Entries 114
Mean 54.98
Std Dev 12.36
Turn on : 52.8267
Width : 4.199
Height : 10.011
Entry
ampl
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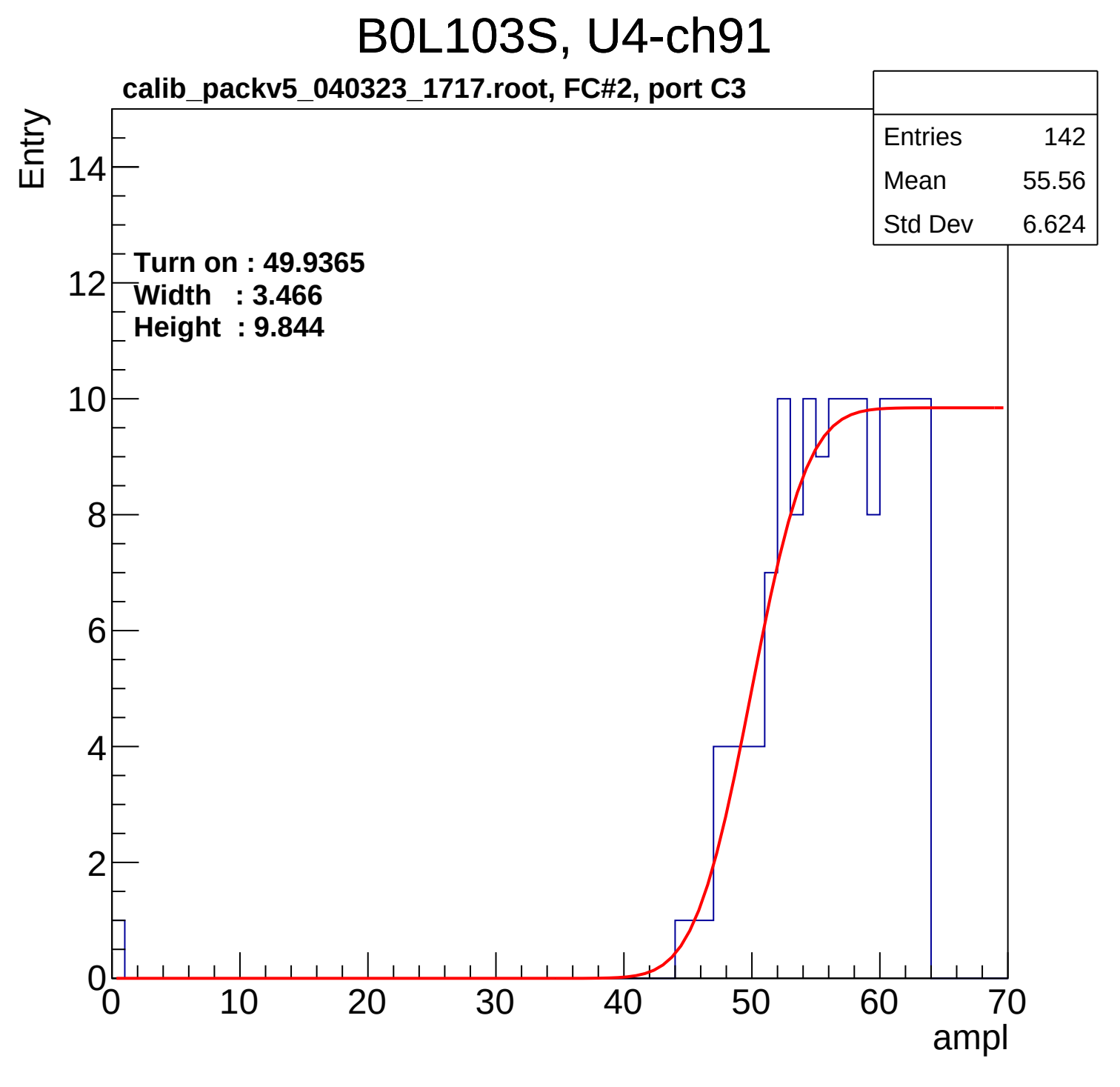
B0L103S, U4-ch91
calib_packv5_040323_1717.root, FC#2, port C3
Entries 142
Mean 55.56
Std Dev 6.624
Turn on : 49.9365
Width : 3.466
Height : 9.844
Entry
ampl
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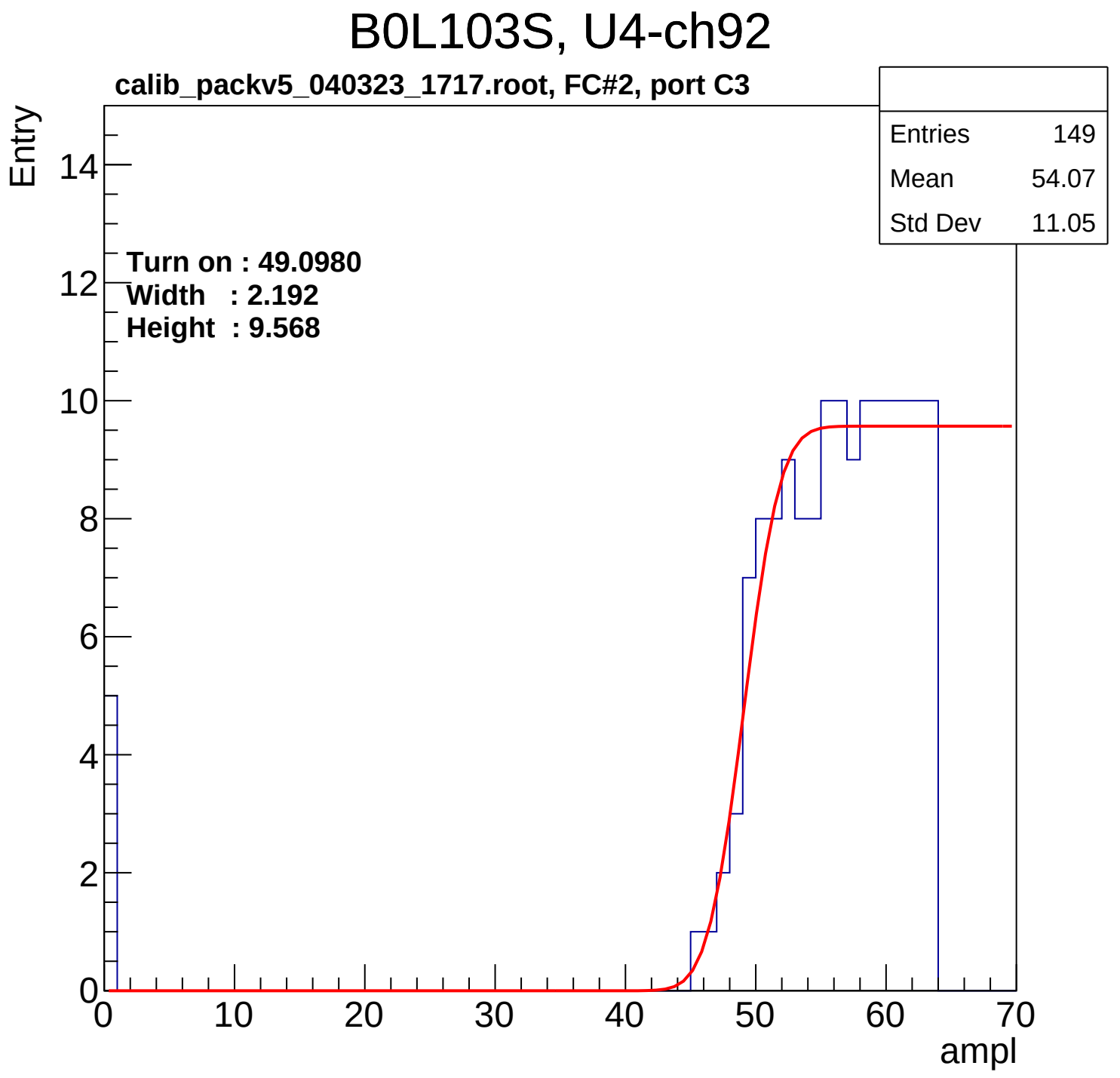
B0L103S, U4-ch92
calib_packv5_040323_1717.root, FC#2, port C3
Entries 149
Mean 54.07
Std Dev 11.05
Turn on : 49.0980
Width : 2.192
Height : 9.568
Entry
ampl
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2
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6
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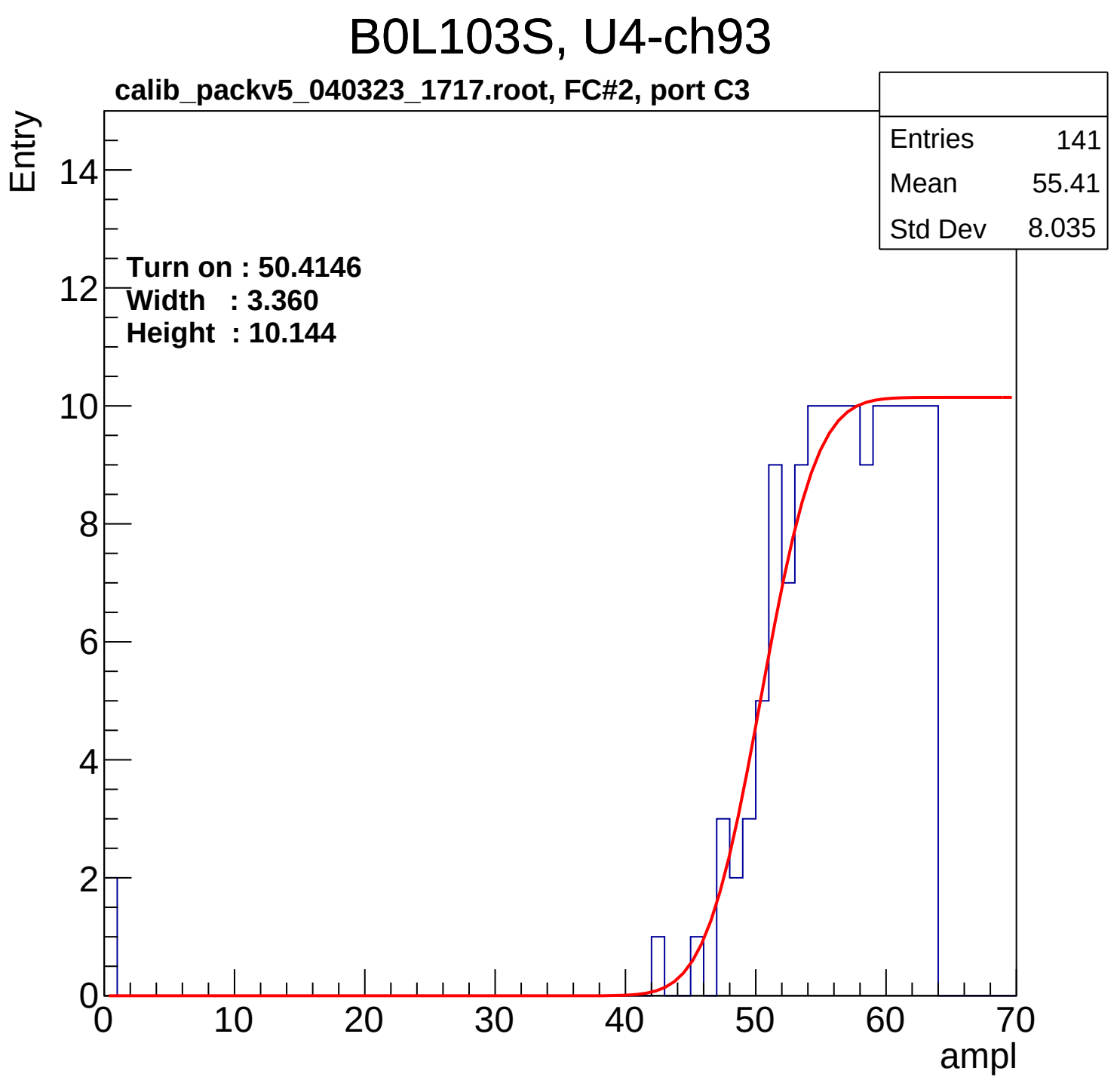
B0L103S, U4-ch93
calib_packv5_040323_1717.root, FC#2, port C3
Entries 141
Mean 55.41
Std Dev 8.035
Turn on : 50.4146
Width : 3.360
Height : 10.144
Entry
ampl
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8
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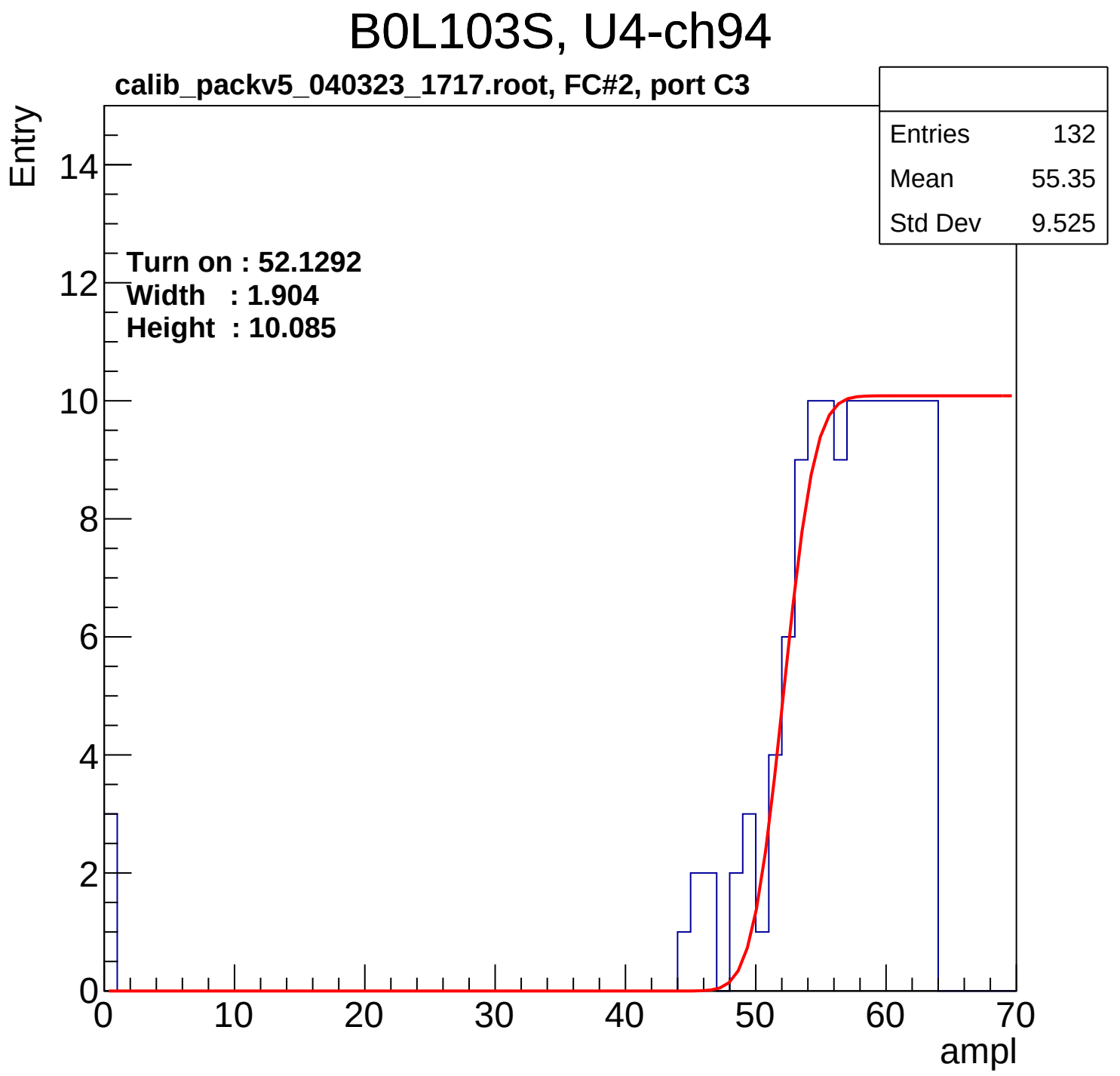
B0L103S, U4-ch94
calib_packv5_040323_1717.root, FC#2, port C3
Entries 132
Mean 55.35
Std Dev 9.525
Turn on : 52.1292
Width : 1.904
Height : 10.085
Entry
ampl
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4
6
8
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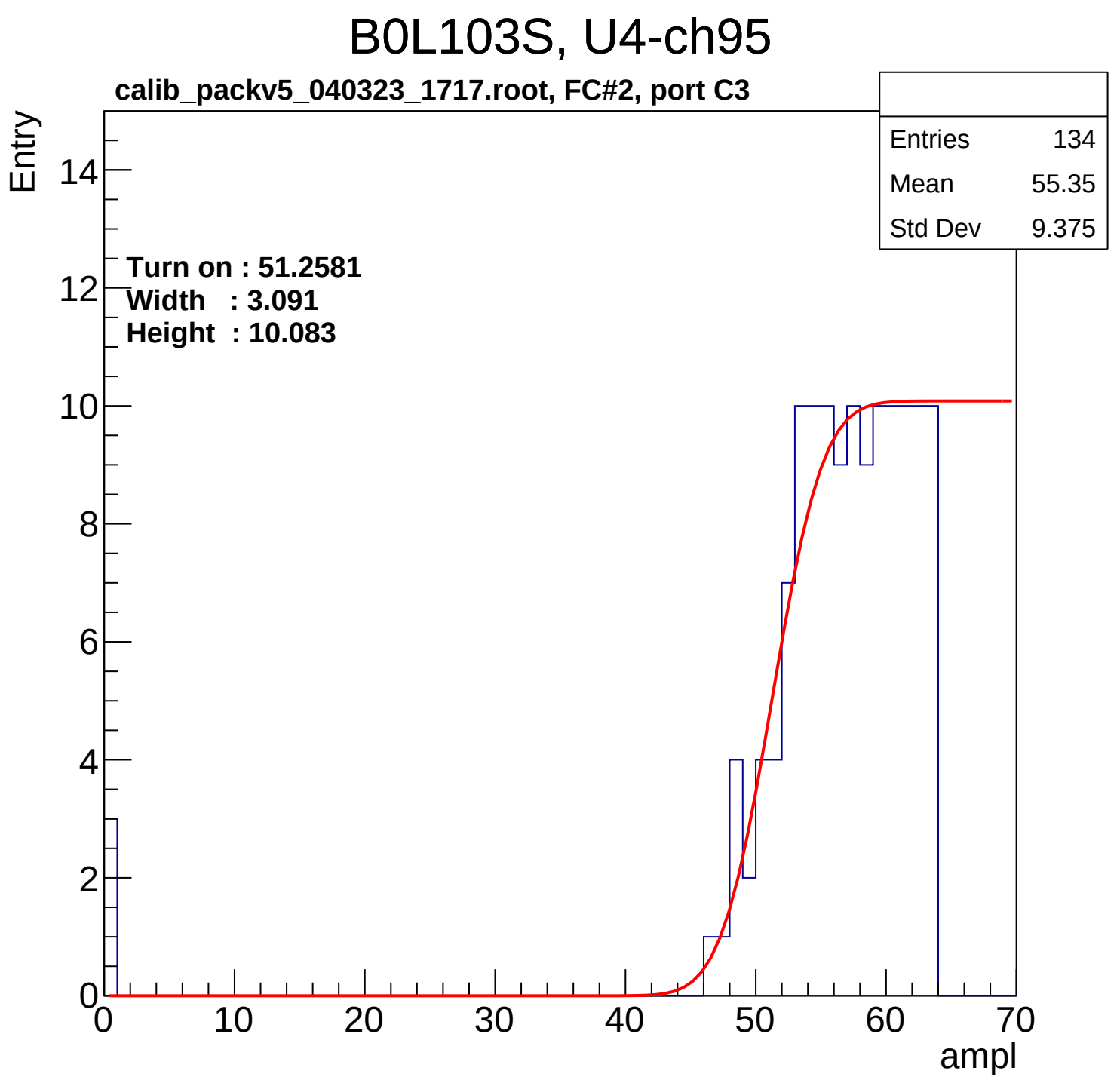
B0L103S, U4-ch95
calib_packv5_040323_1717.root, FC#2, port C3
Entries 134
Mean 55.35
Std Dev 9.375
Turn on : 51.2581
Width : 3.091
Height : 10.083
Entry
ampl
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6
8
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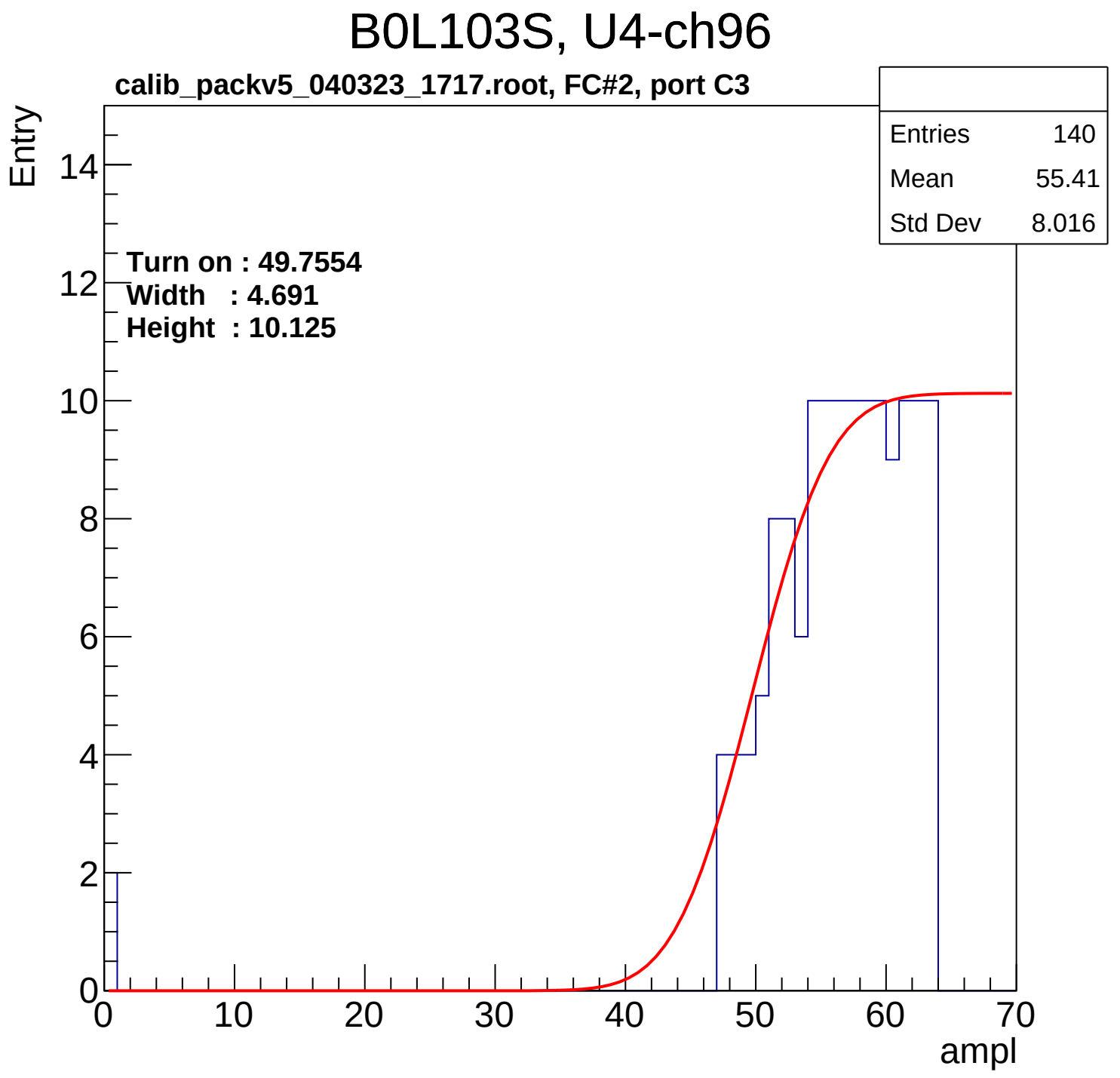
B0L103S, U4-ch96
calib_packv5_040323_1717.root, FC#2, port C3
Entries 140
Mean 55.41
Std Dev 8.016
Turn on : 49.7554
Width : 4.691
Height : 10.125
Entry
ampl
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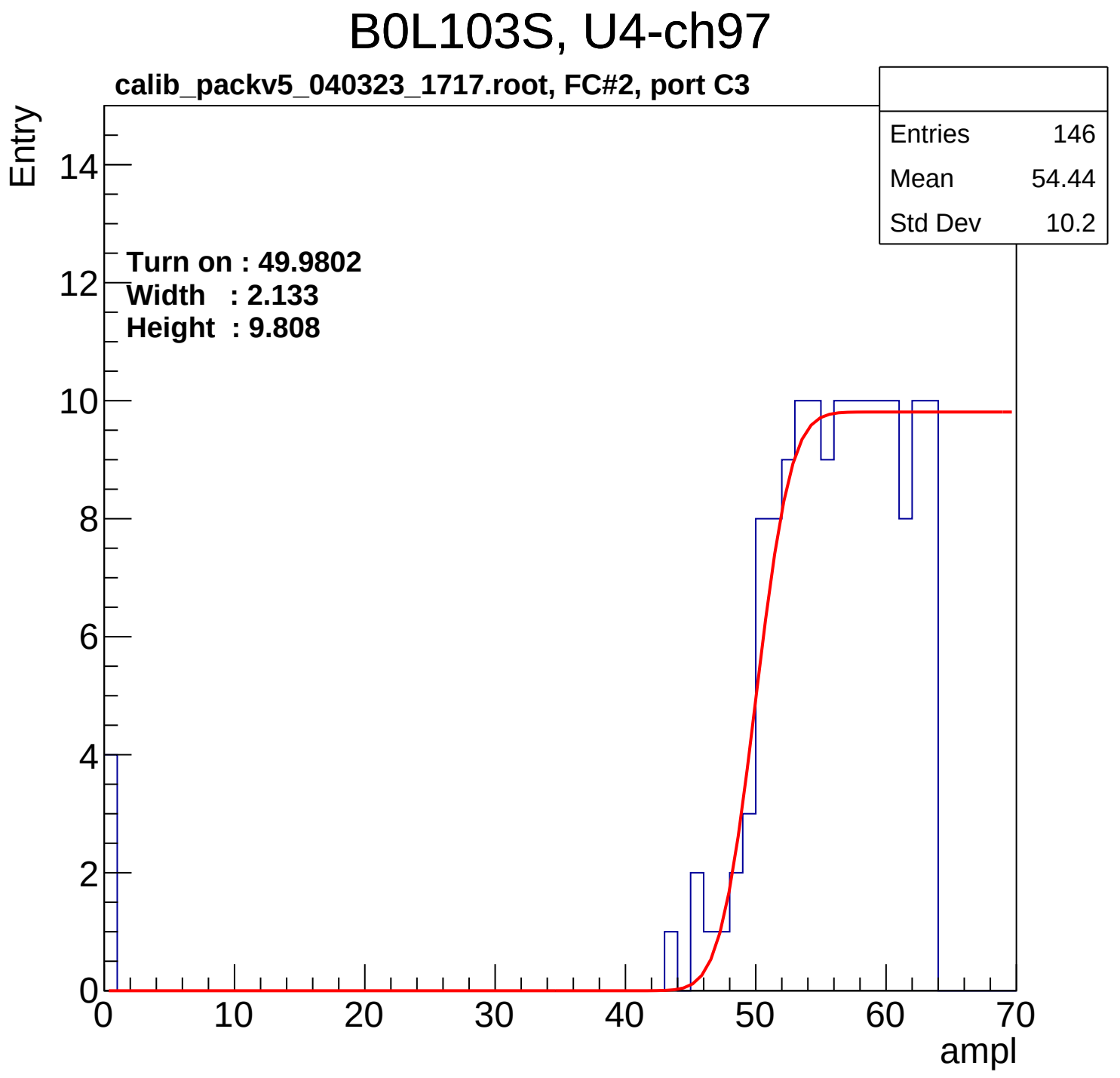
B0L103S, U4-ch97
calib_packv5_040323_1717.root, FC#2, port C3
Entries 146
Mean 54.44
Std Dev 10.2
Turn on : 49.9802
Width : 2.133
Height : 9.808
Entry
ampl
0
2
4
6
8
10
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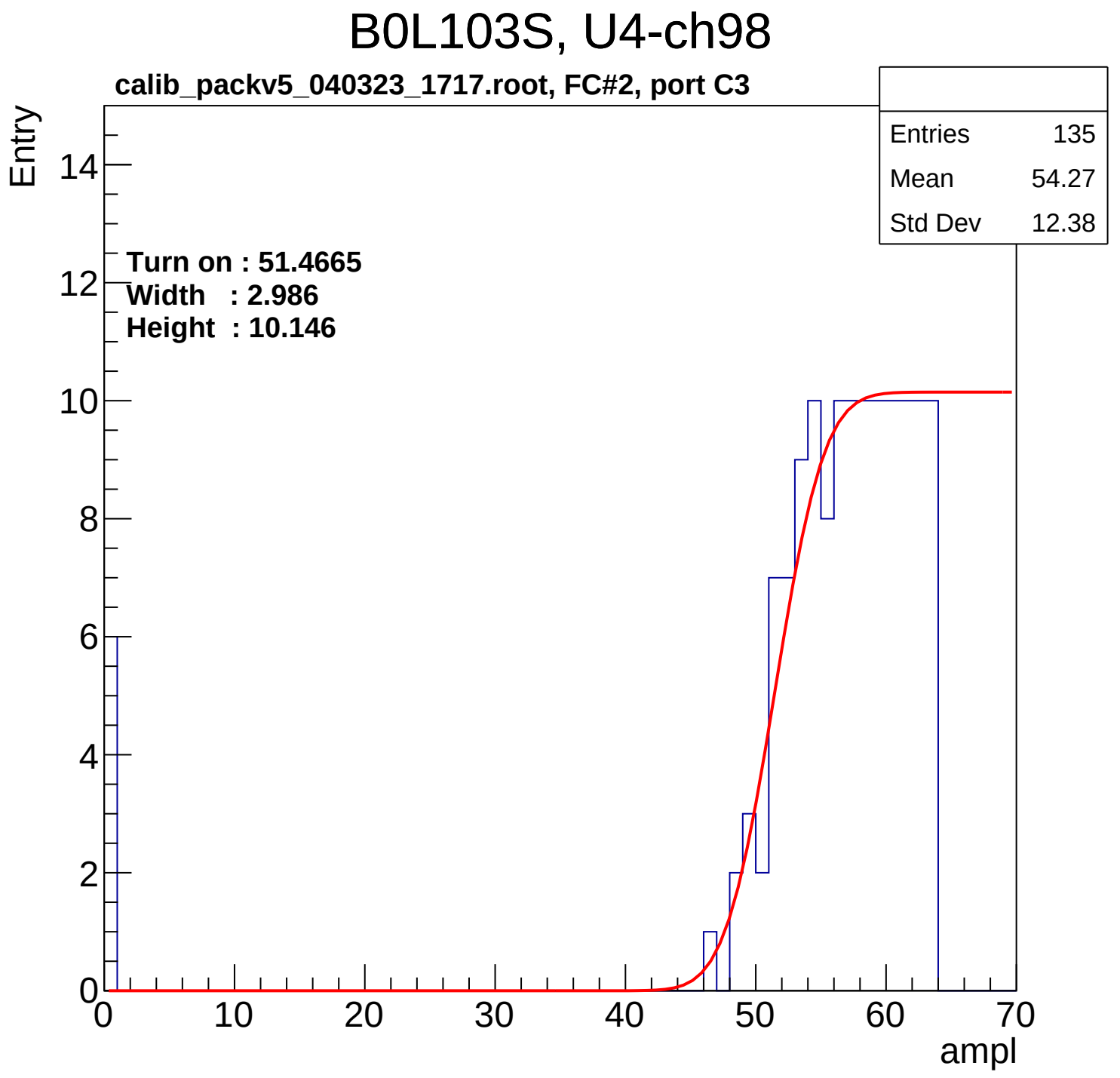
B0L103S, U4-ch98
calib_packv5_040323_1717.root, FC#2, port C3
Entries 135
Mean 54.27
Std Dev 12.38
Turn on : 51.4665
Width : 2.986
Height : 10.146
Entry
ampl
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6
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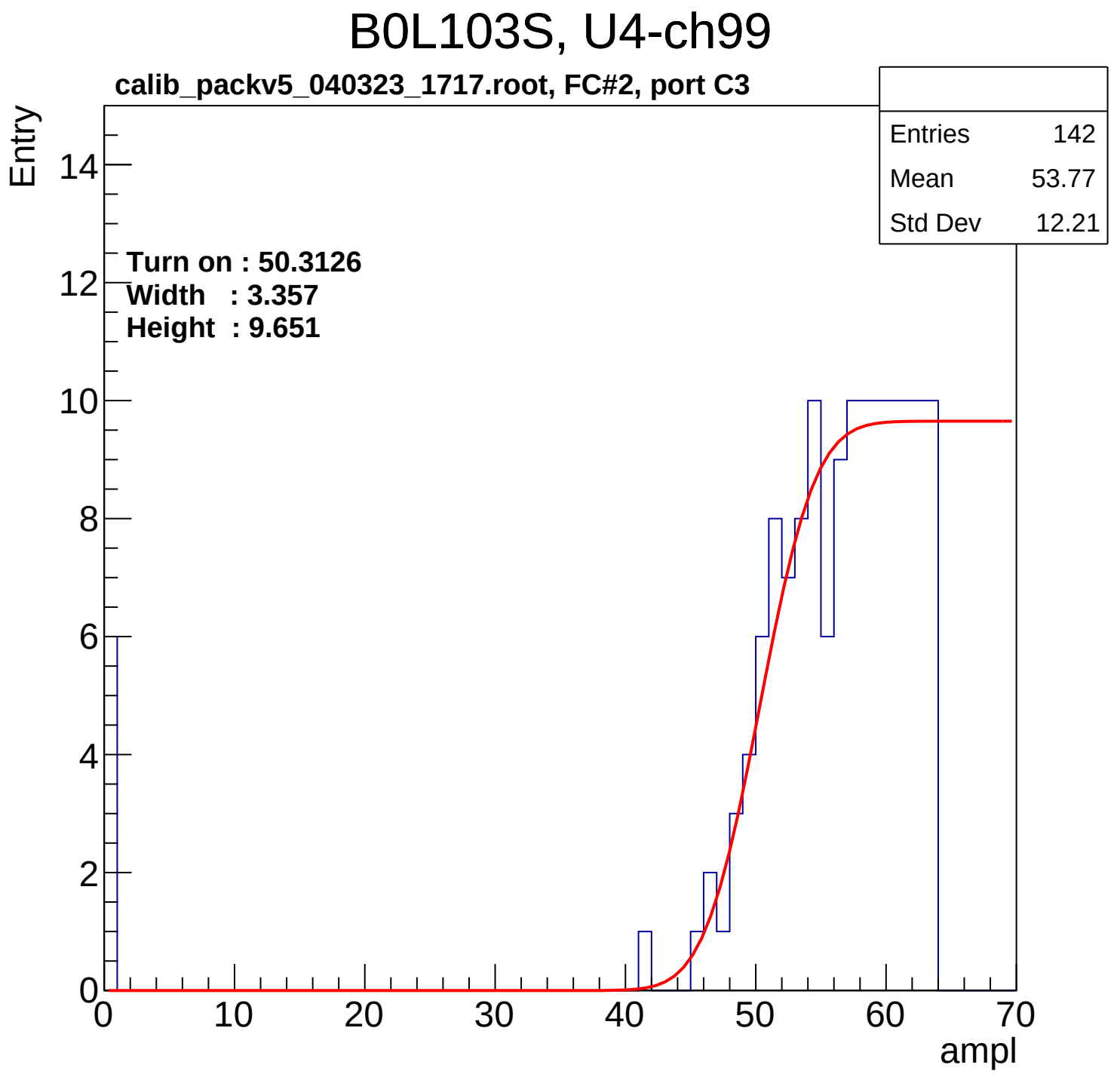
B0L103S, U4-ch99
calib_packv5_040323_1717.root, FC#2, port C3
Entries 142
Mean 53.77
Std Dev 12.21
Turn on : 50.3126
Width : 3.357
Height : 9.651
Entry
ampl
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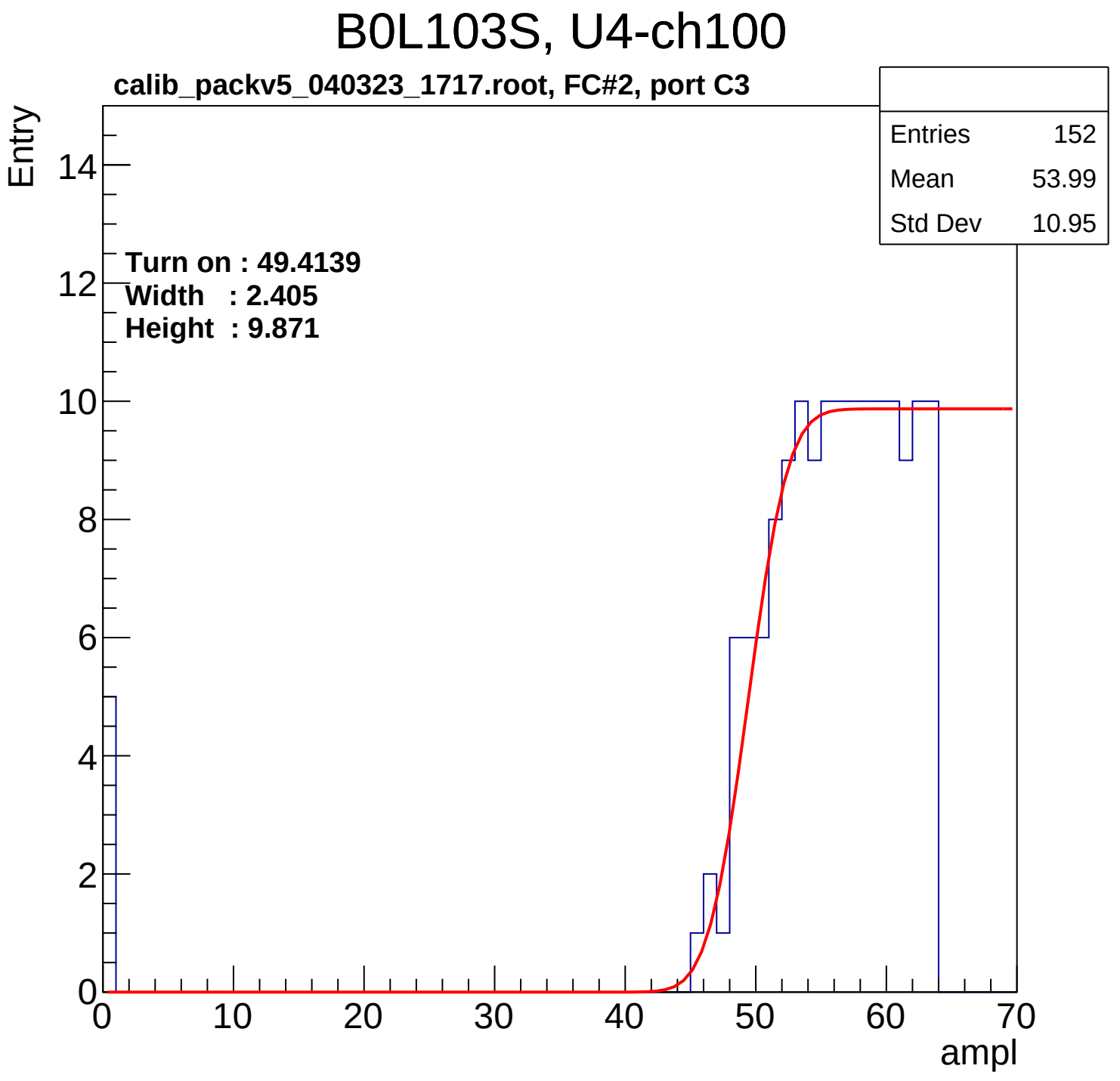
B0L103S, U4-ch100
calib_packv5_040323_1717.root, FC#2, port C3
Entries 152
Mean 53.99
Std Dev 10.95
Turn on : 49.4139
Width : 2.405
Height : 9.871
Entry
ampl
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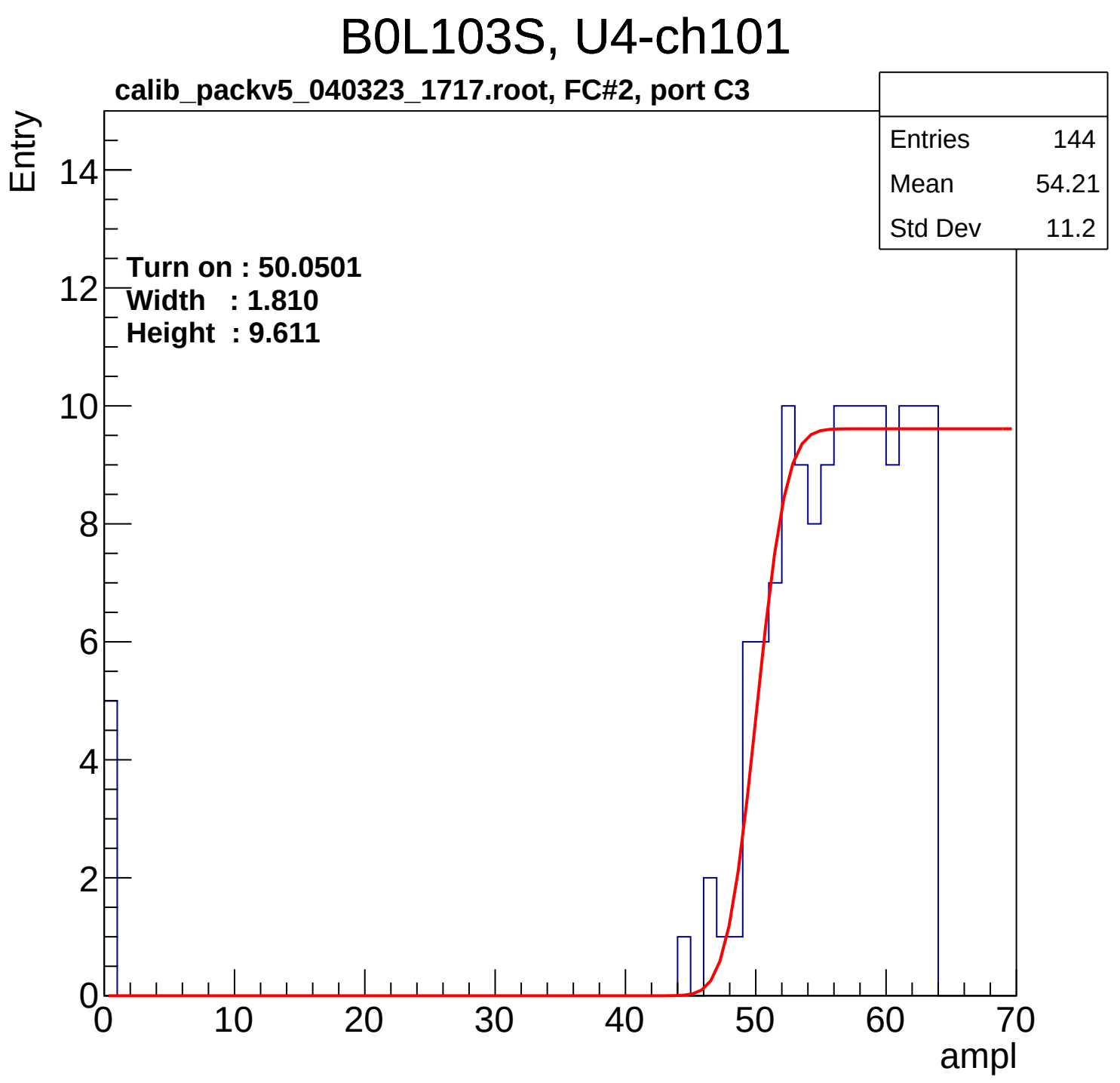
B0L103S, U4-ch101
calib_packv5_040323_1717.root, FC#2, port C3
Entries 144
Mean 54.21
Std Dev 11.2
Turn on : 50.0501
Width : 1.810
Height : 9.611
Entry
ampl
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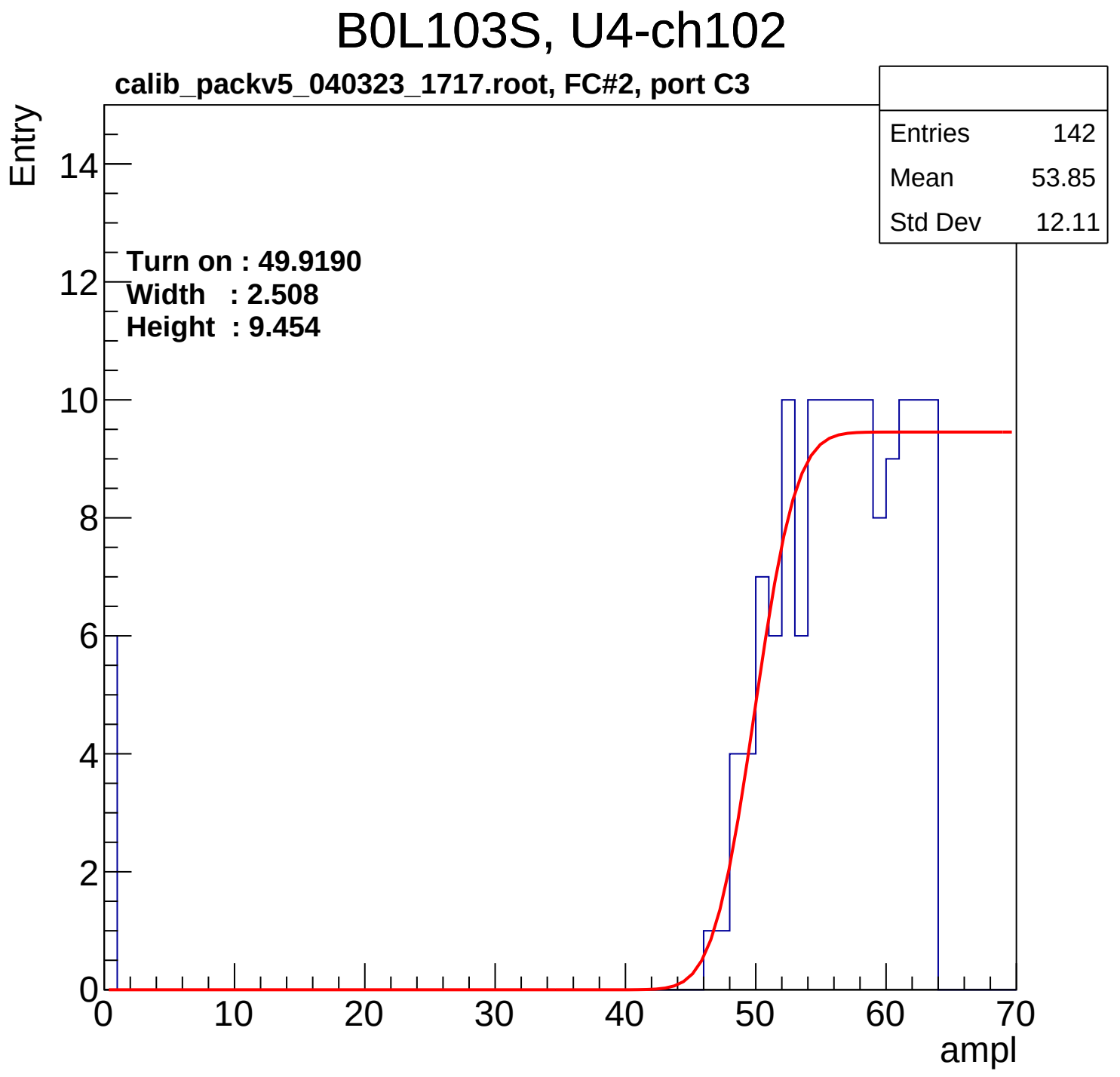
B0L103S, U4-ch102
calib_packv5_040323_1717.root, FC#2, port C3
Entries 142
Mean 53.85
Std Dev 12.11
Turn on : 49.9190
Width : 2.508
Height : 9.454
Entry
ampl
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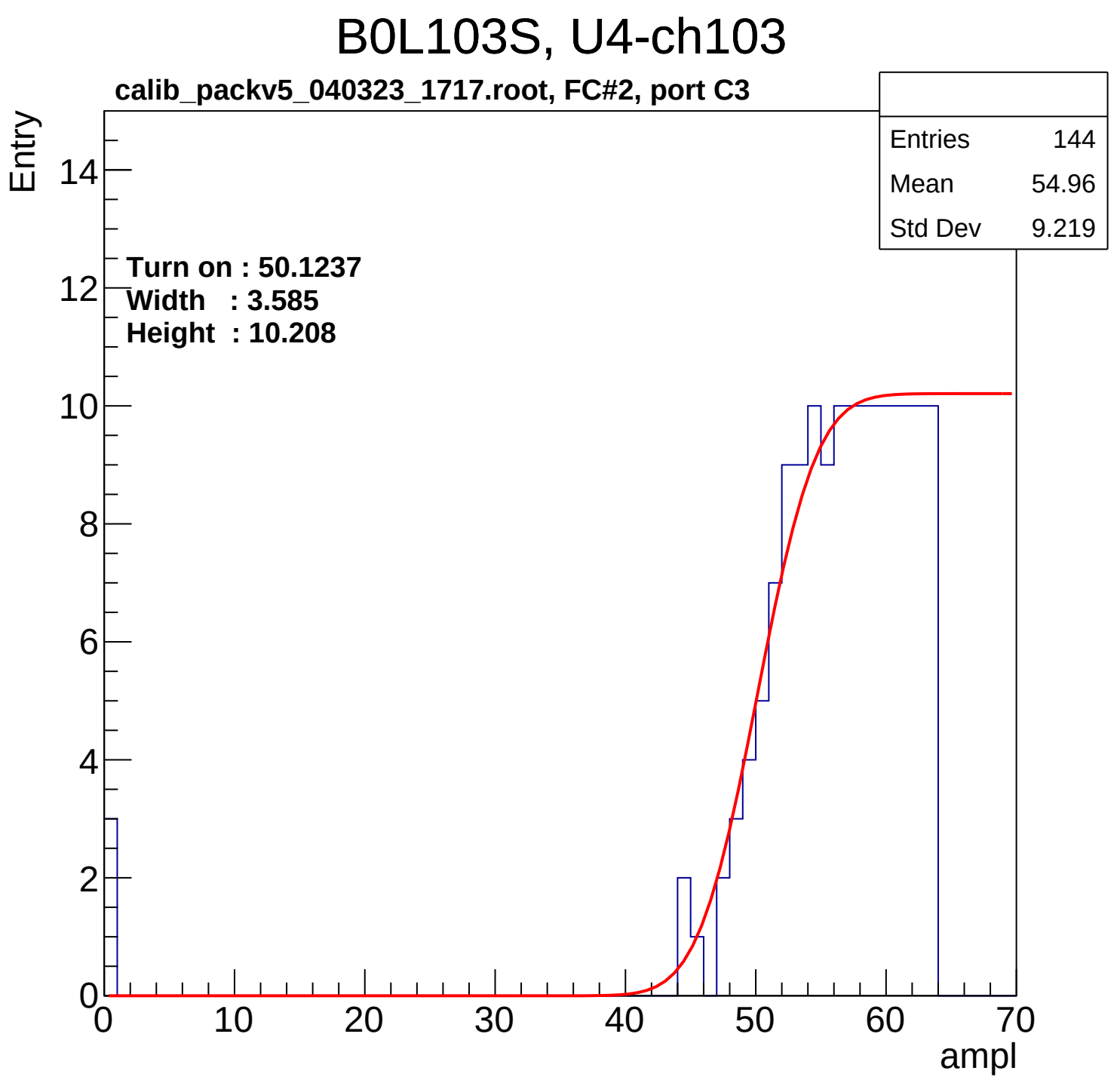
B0L103S, U4-ch103
calib_packv5_040323_1717.root, FC#2, port C3
Entries 144
Mean 54.96
Std Dev 9.219
Turn on : 50.1237
Width : 3.585
Height : 10.208
Entry
ampl
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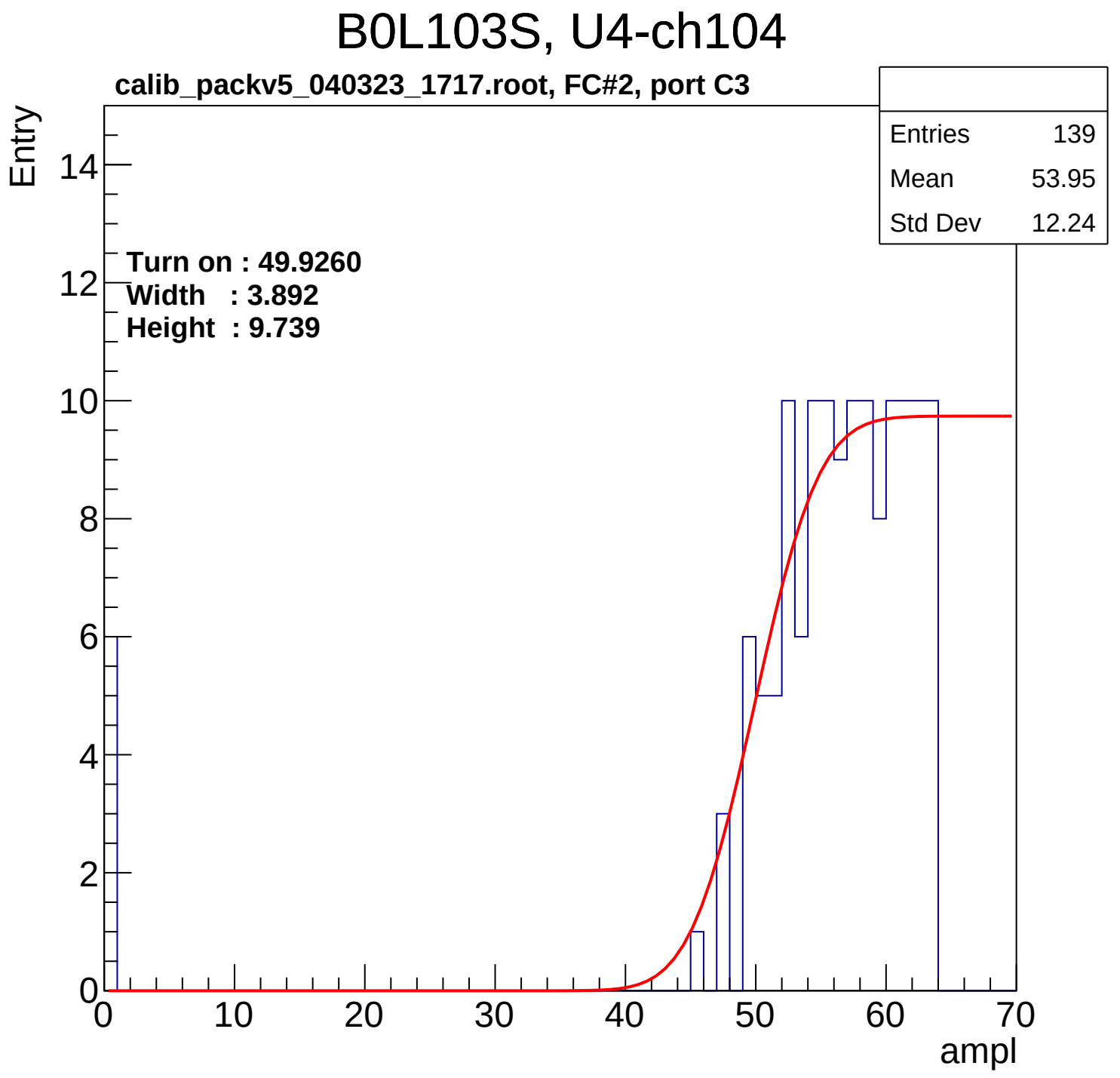
B0L103S, U4-ch104
calib_packv5_040323_1717.root, FC#2, port C3
Entries 139
Mean 53.95
Std Dev 12.24
Turn on : 49.9260
Width : 3.892
Height : 9.739
Entry
ampl
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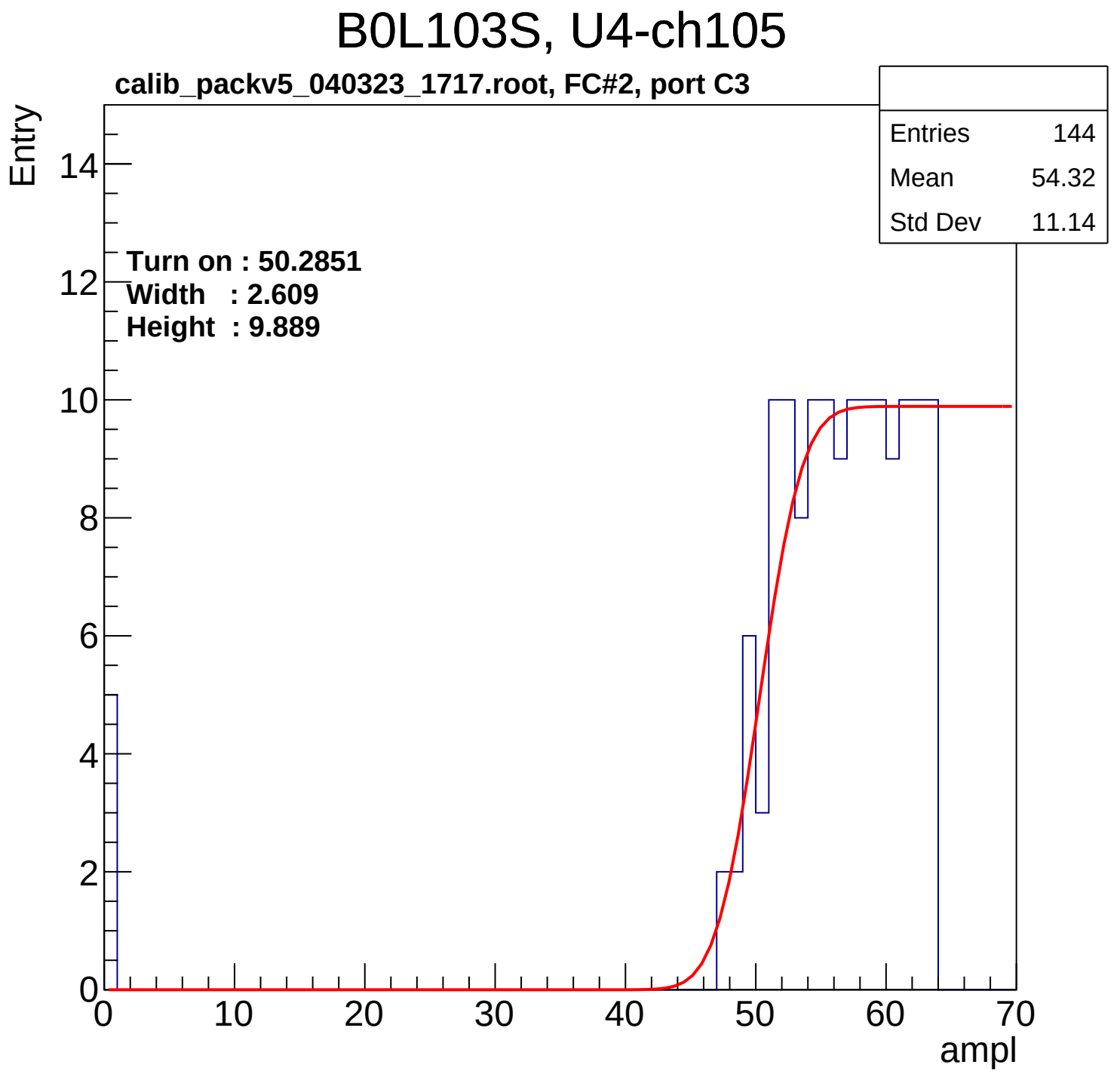
B0L103S, U4-ch105
calib_packv5_040323_1717.root, FC#2, port C3
Entries 144
Mean 54.32
Std Dev 11.14
Turn on : 50.2851
Width : 2.609
Height : 9.889
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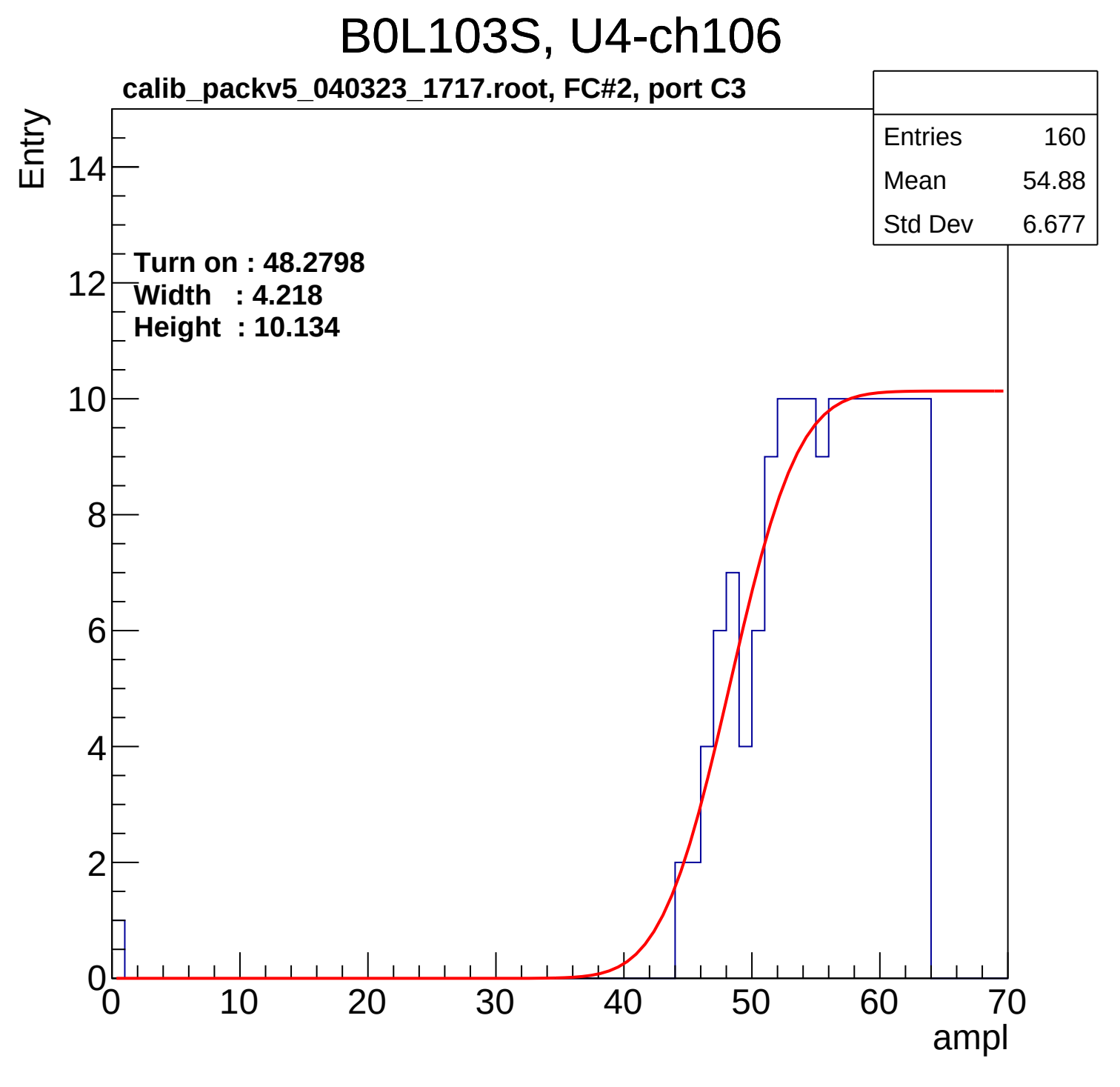
B0L103S, U4-ch106
calib_packv5_040323_1717.root, FC#2, port C3
Entries 160
Mean 54.88
Std Dev 6.677
Turn on : 48.2798
Width : 4.218
Height : 10.134
Entry
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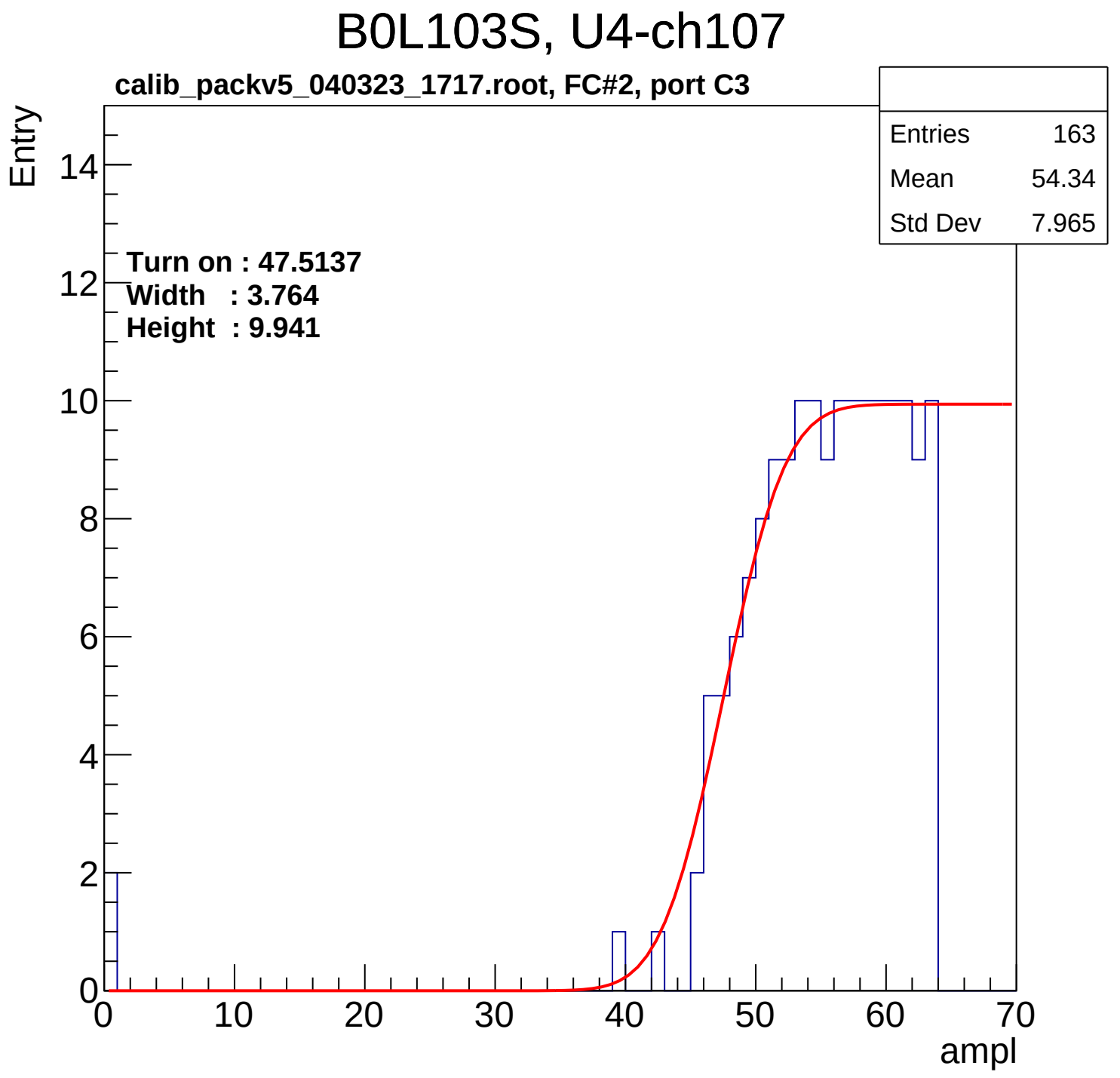
B0L103S, U4-ch107
calib_packv5_040323_1717.root, FC#2, port C3
Entries 163
Mean 54.34
Std Dev 7.965
Turn on : 47.5137
Width : 3.764
Height : 9.941
Entry
ampl
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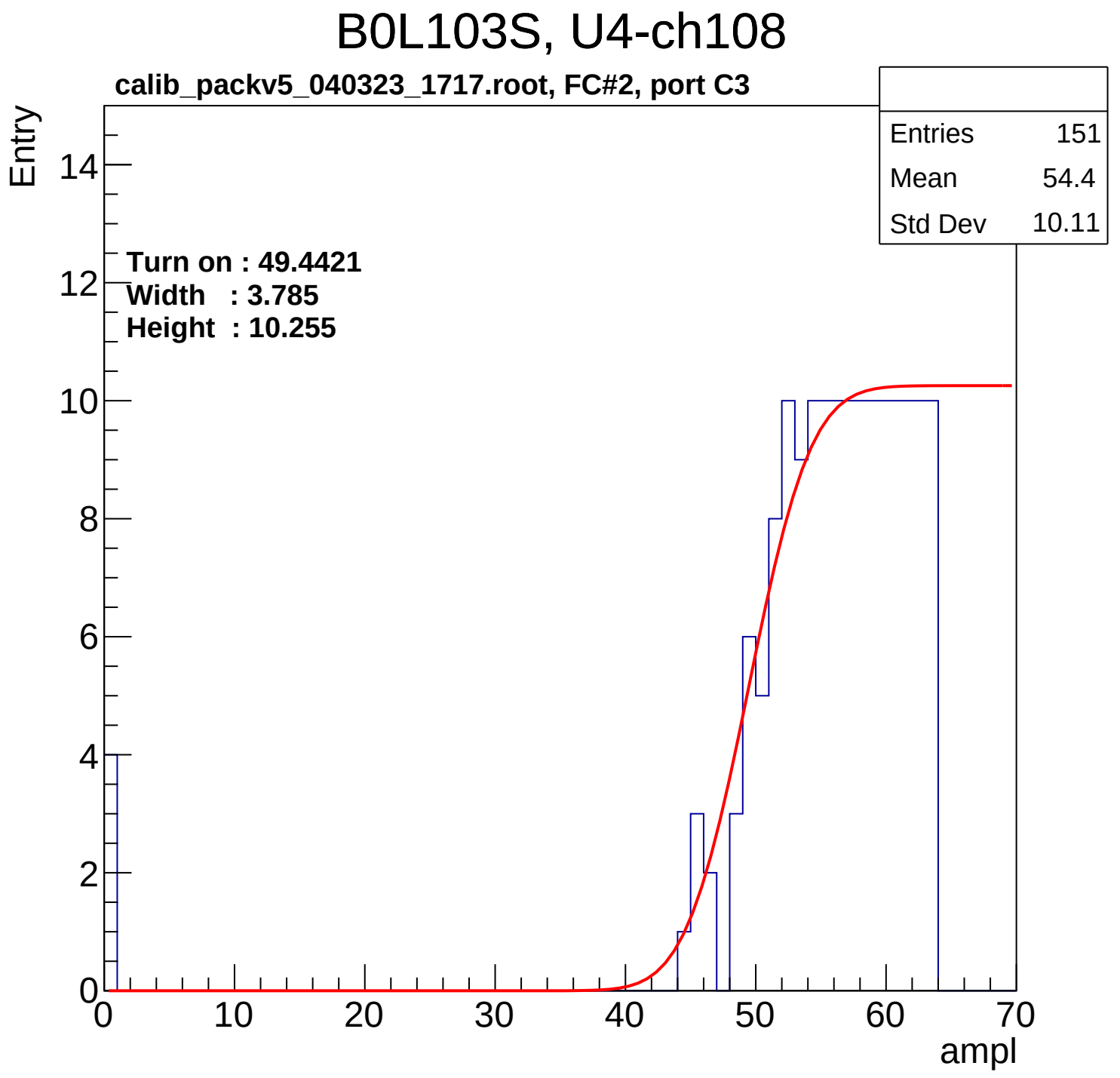
B0L103S, U4-ch108
calib_packv5_040323_1717.root, FC#2, port C3
Entries 151
Mean 54.4
Std Dev 10.11
Turn on : 49.4421
Width : 3.785
Height : 10.255
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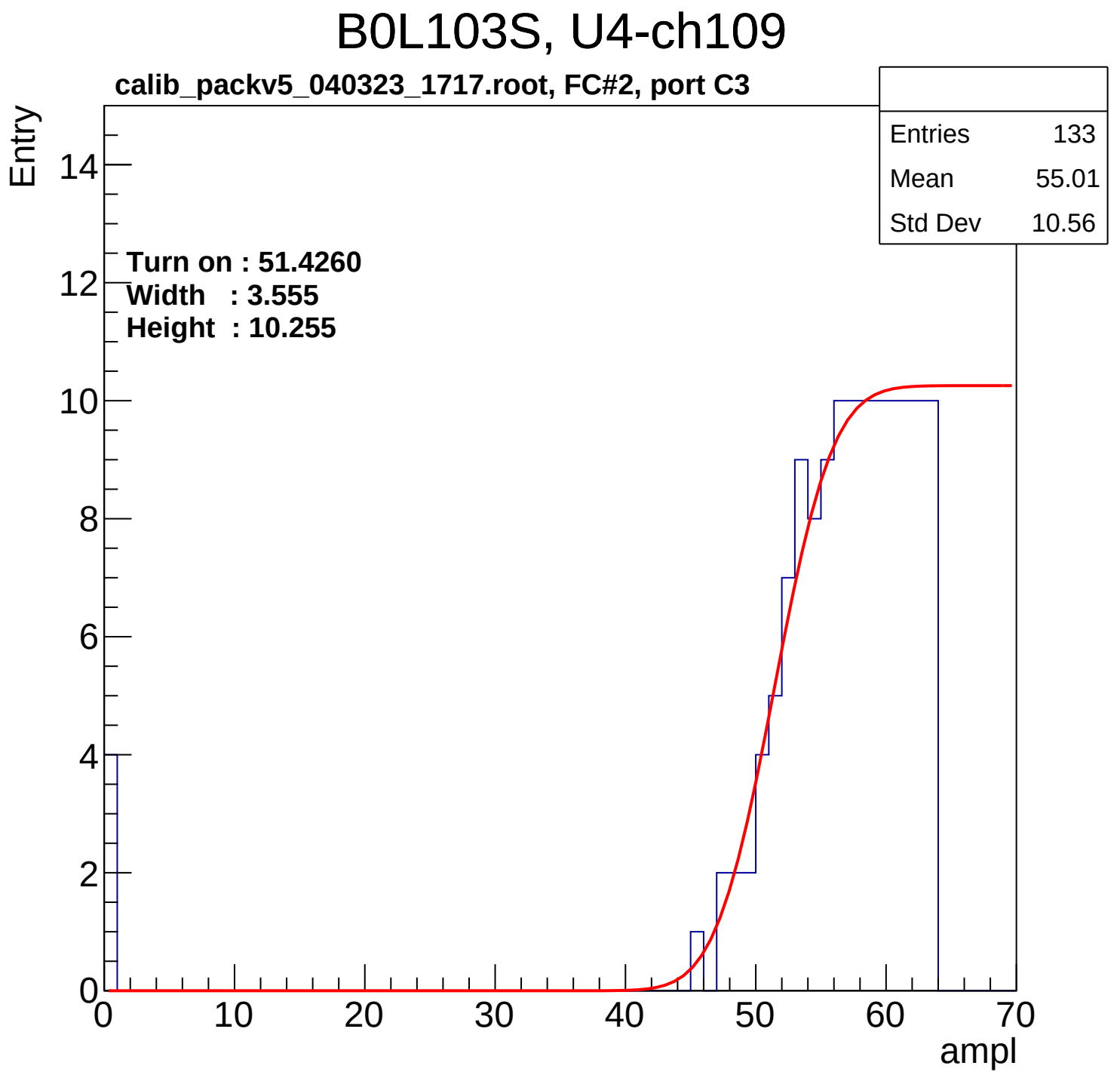
B0L103S, U4-ch109
calib_packv5_040323_1717.root, FC#2, port C3
Entries 133
Mean 55.01
Std Dev 10.56
Turn on : 51.4260
Width : 3.555
Height : 10.255
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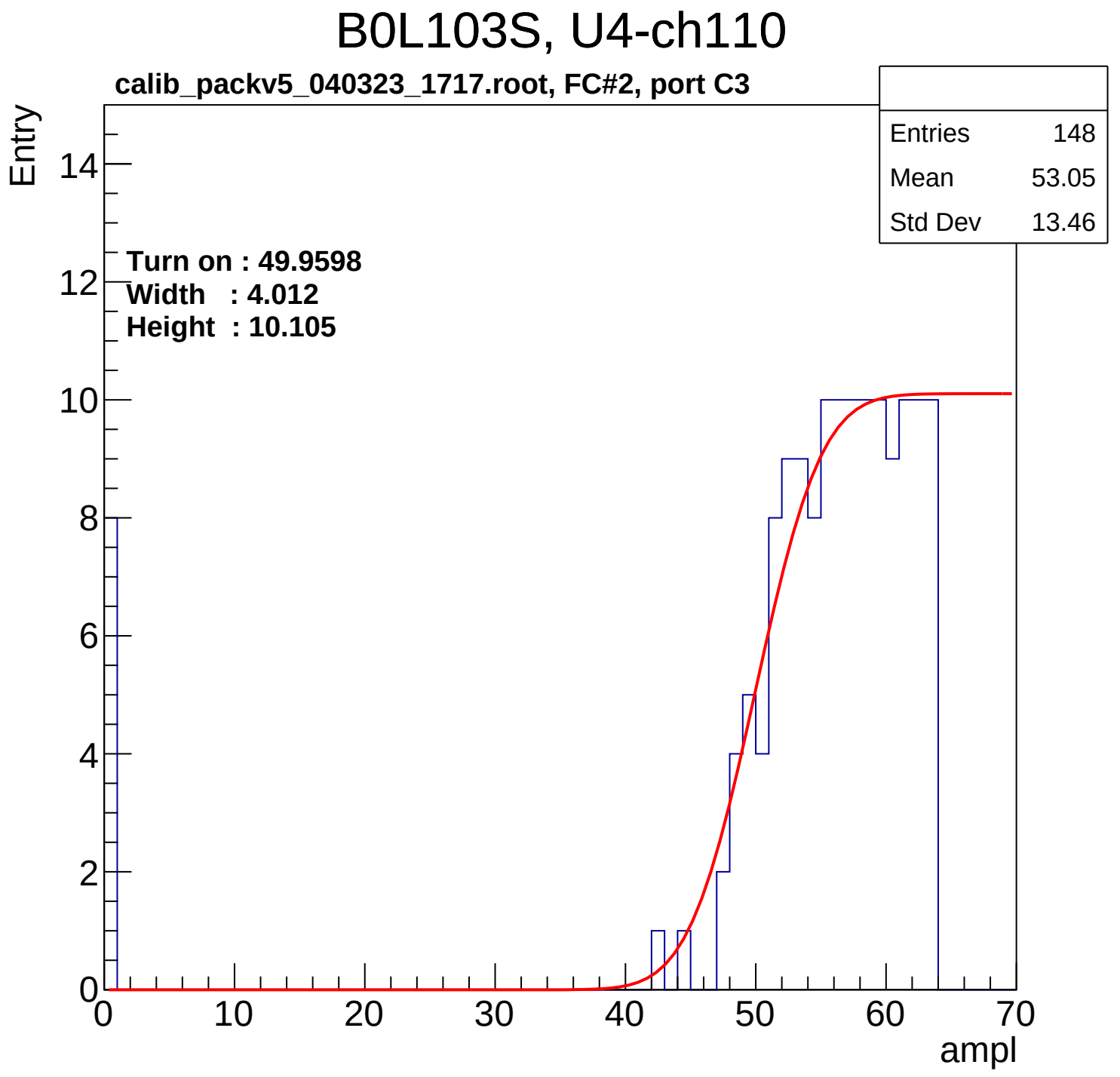
B0L103S, U4-ch110
calib_packv5_040323_1717.root, FC#2, port C3
Entries 148
Mean 53.05
Std Dev 13.46
Turn on : 49.9598
Width : 4.012
Height : 10.105
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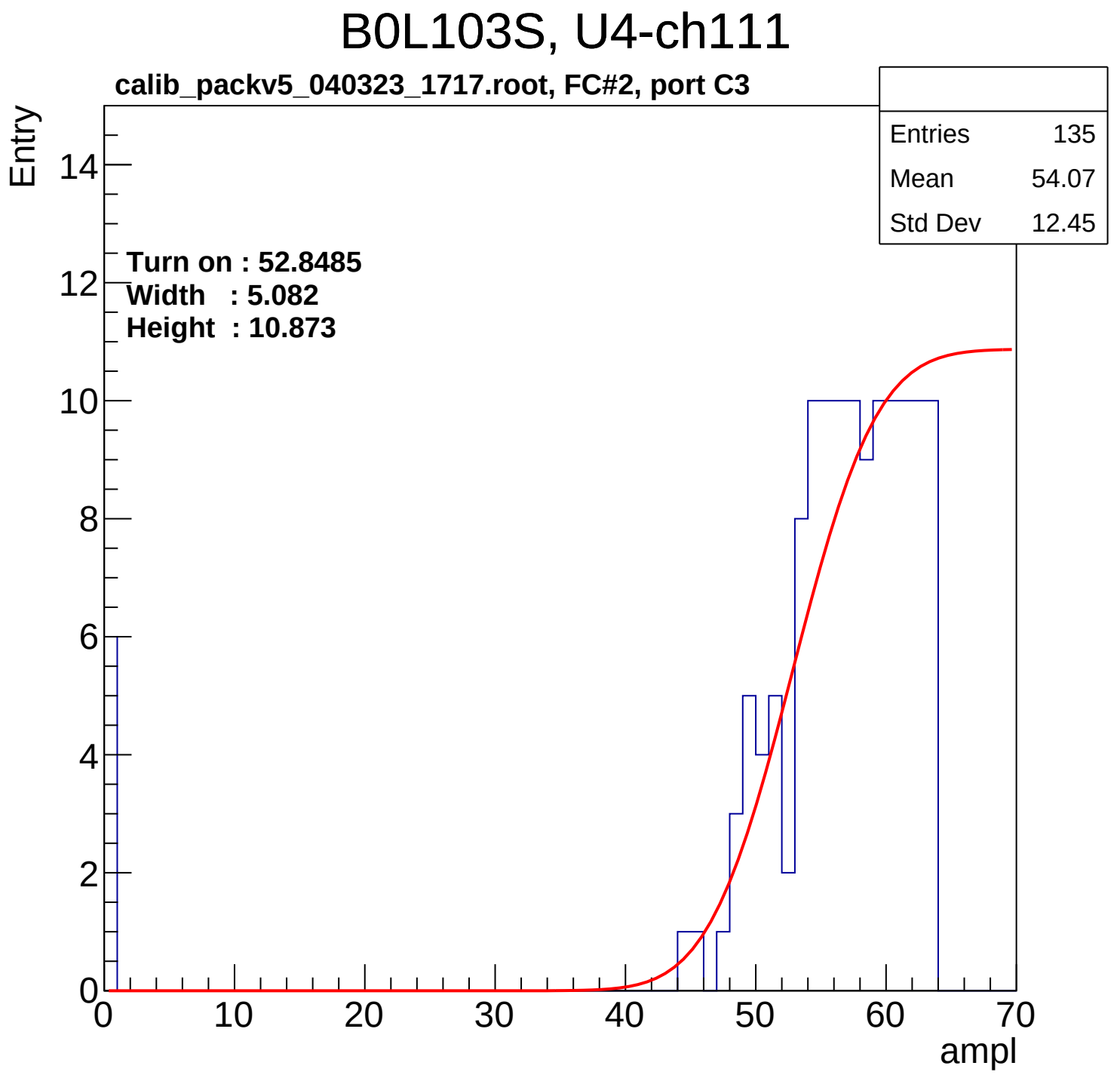
B0L103S, U4-ch111
calib_packv5_040323_1717.root, FC#2, port C3
Entries 135
Mean 54.07
Std Dev 12.45
Turn on : 52.8485
Width : 5.082
Height : 10.873
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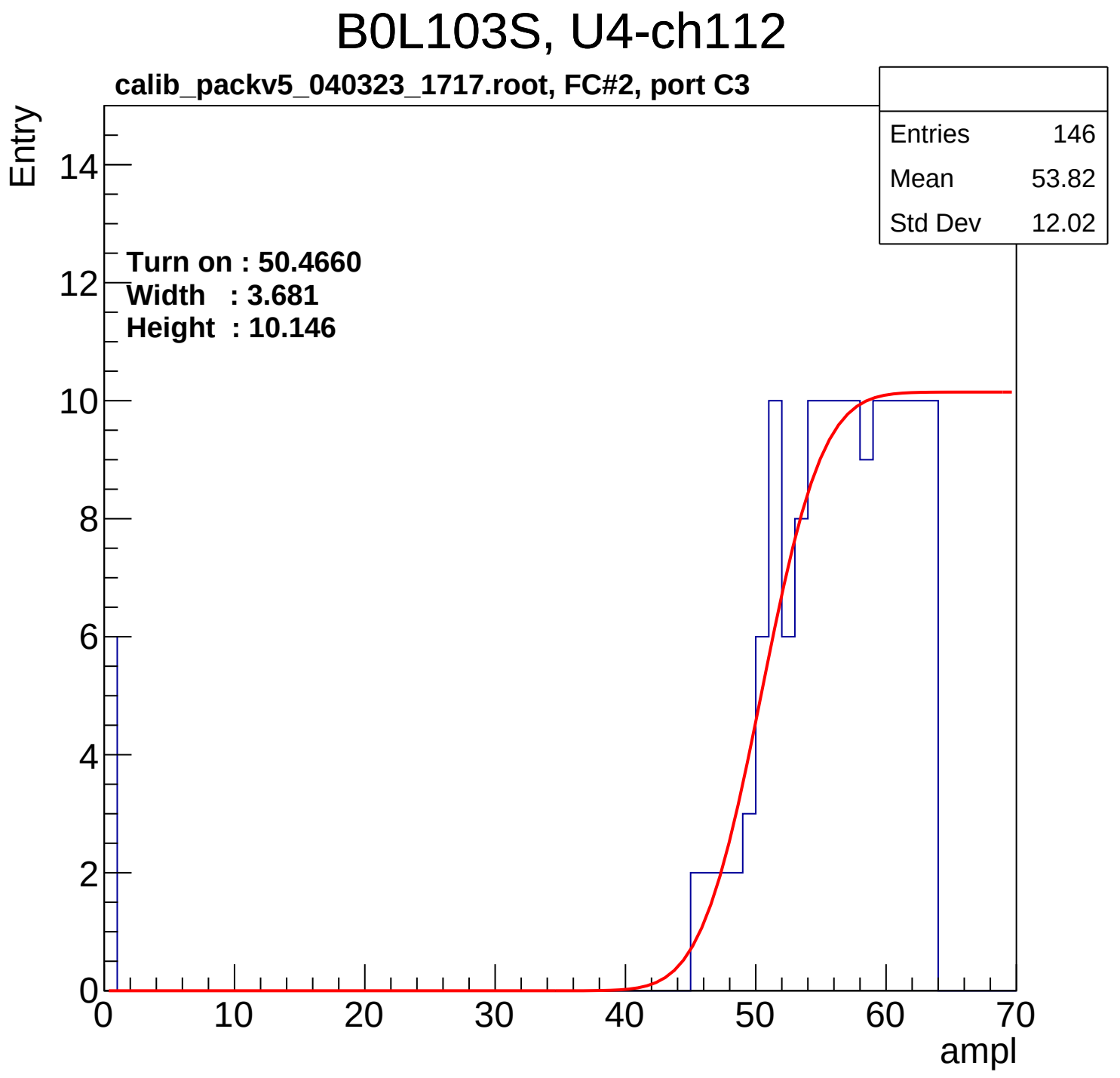
B0L103S, U4-ch112
calib_packv5_040323_1717.root, FC#2, port C3
Entries 146
Mean 53.82
Std Dev 12.02
Turn on : 50.4660
Width : 3.681
Height : 10.146
Entry
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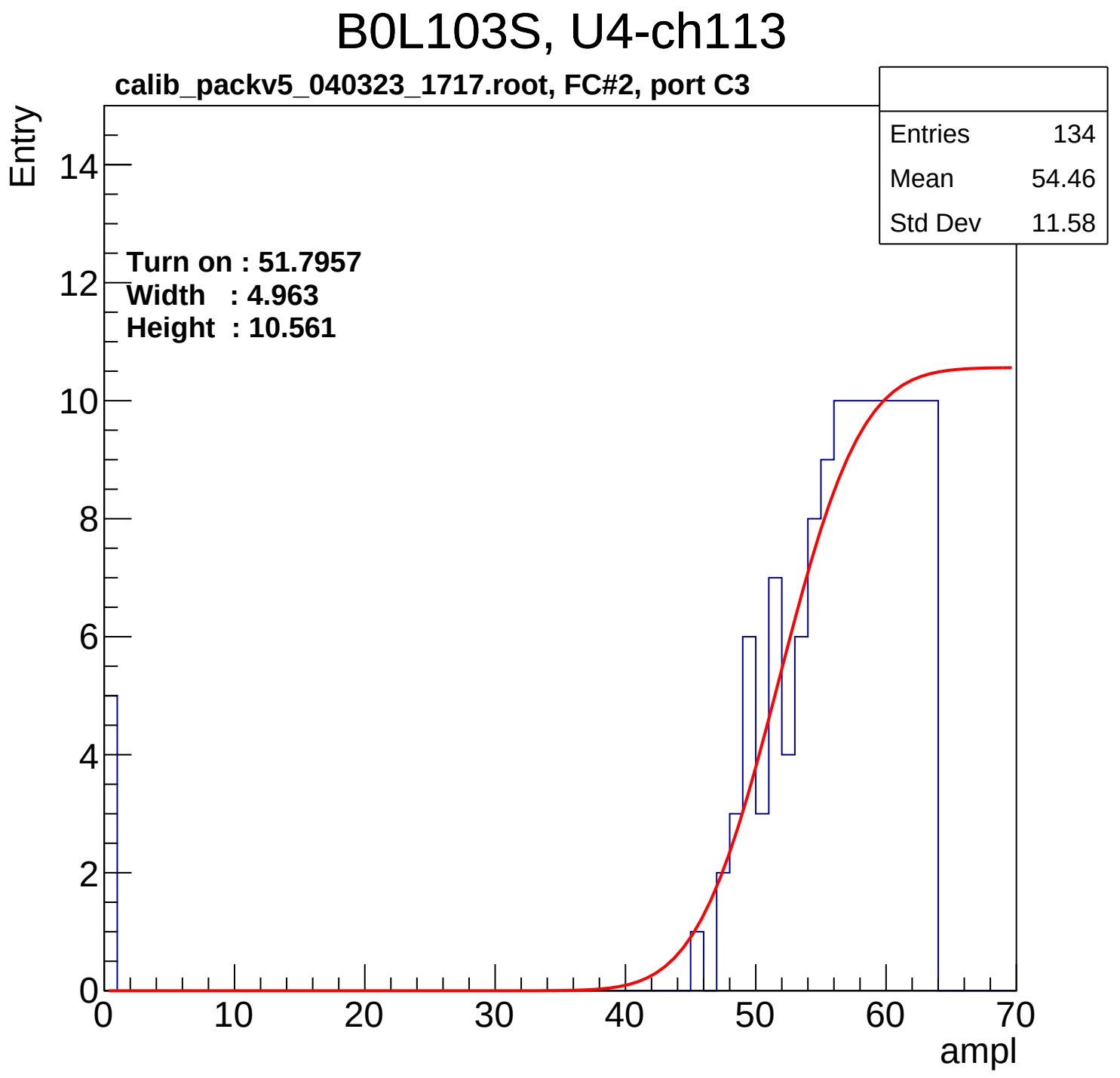
B0L103S, U4-ch113
calib_packv5_040323_1717.root, FC#2, port C3
Entries 134
Mean 54.46
Std Dev 11.58
Turn on : 51.7957
Width : 4.963
Height : 10.561
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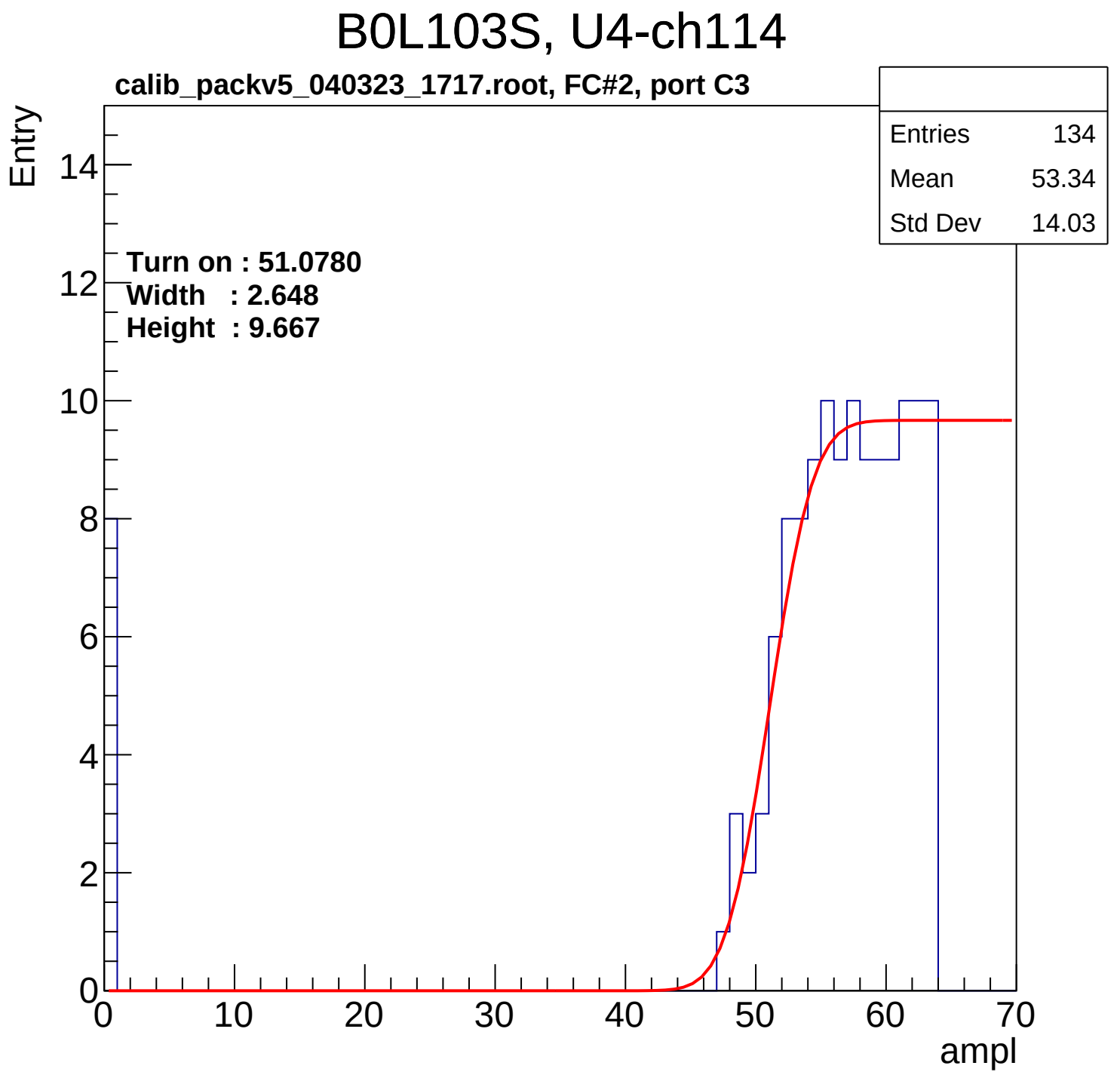
B0L103S, U4-ch114
calib_packv5_040323_1717.root, FC#2, port C3
Entries 134
Mean 53.34
Std Dev 14.03
Turn on : 51.0780
Width : 2.648
Height : 9.667
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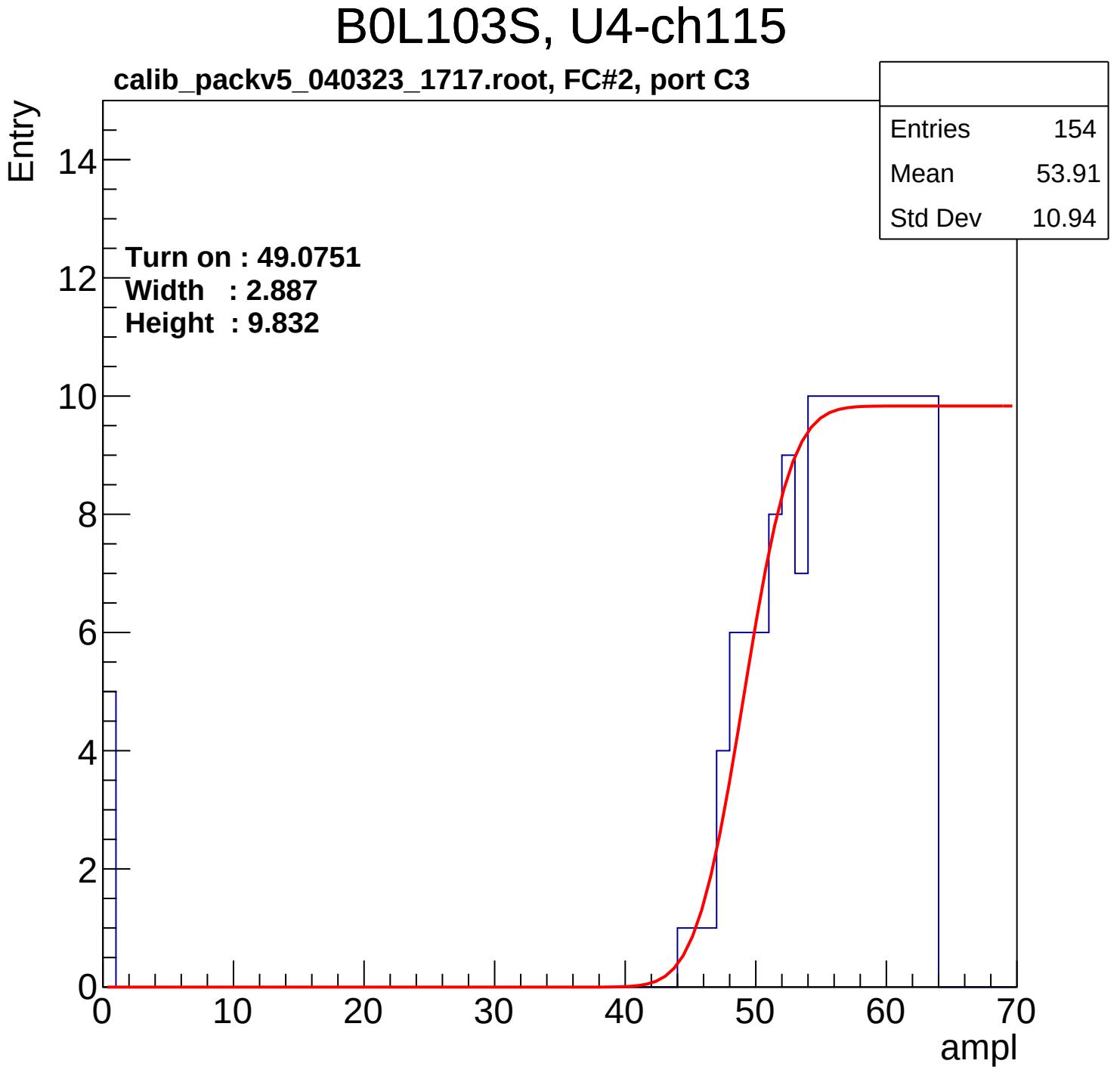
B0L103S, U4-ch115
calib_packv5_040323_1717.root, FC#2, port C3
Entries 154
Mean 53.91
Std Dev 10.94
Turn on : 49.0751
Width : 2.887
Height : 9.832
Entry
ampl
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6
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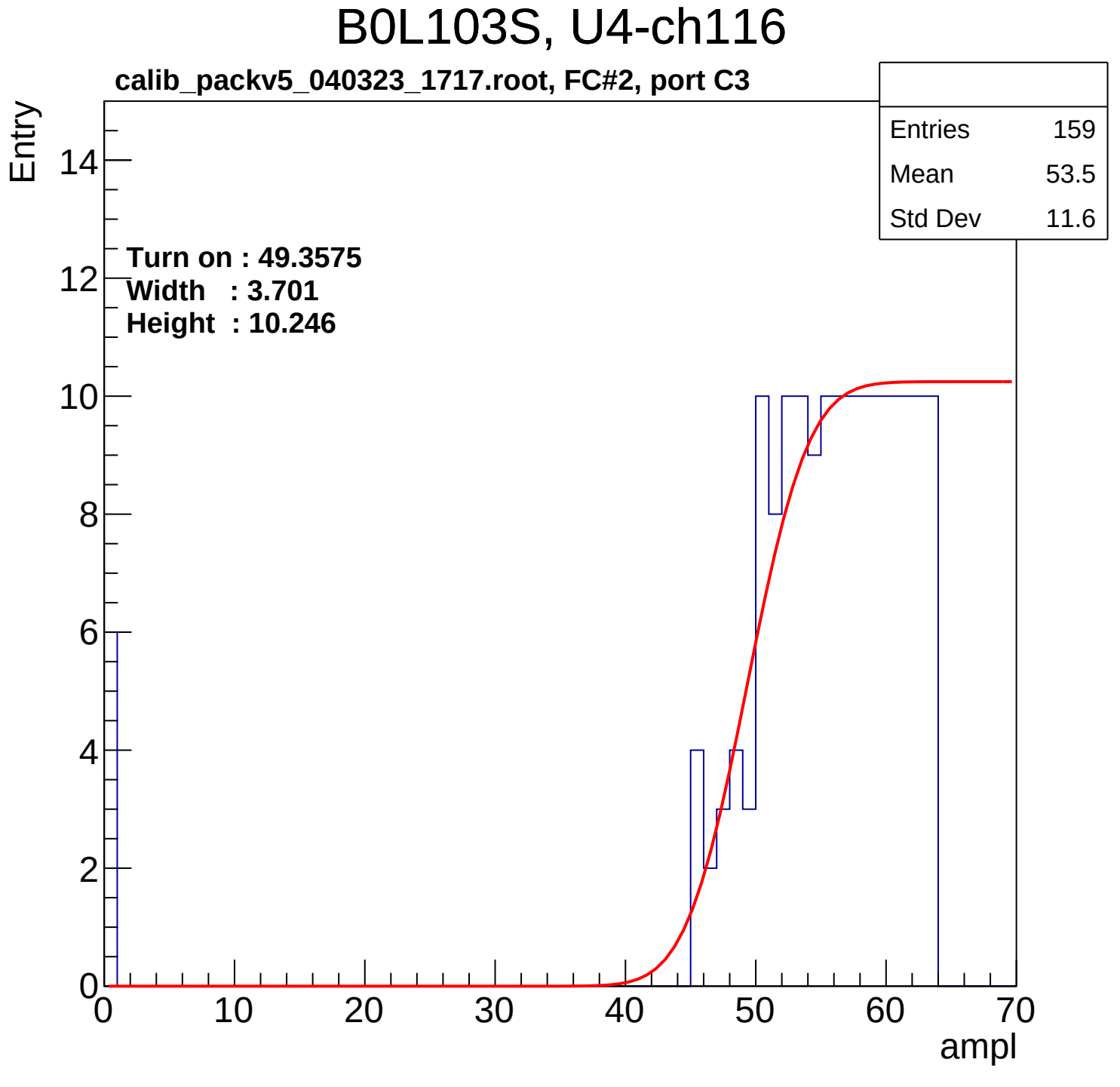
B0L103S, U4-ch116
calib_packv5_040323_1717.root, FC#2, port C3
Entries 159
Mean 53.5
Std Dev 11.6
Turn on : 49.3575
Width : 3.701
Height : 10.246
Entry
ampl
0
2
4
6
8
10
12
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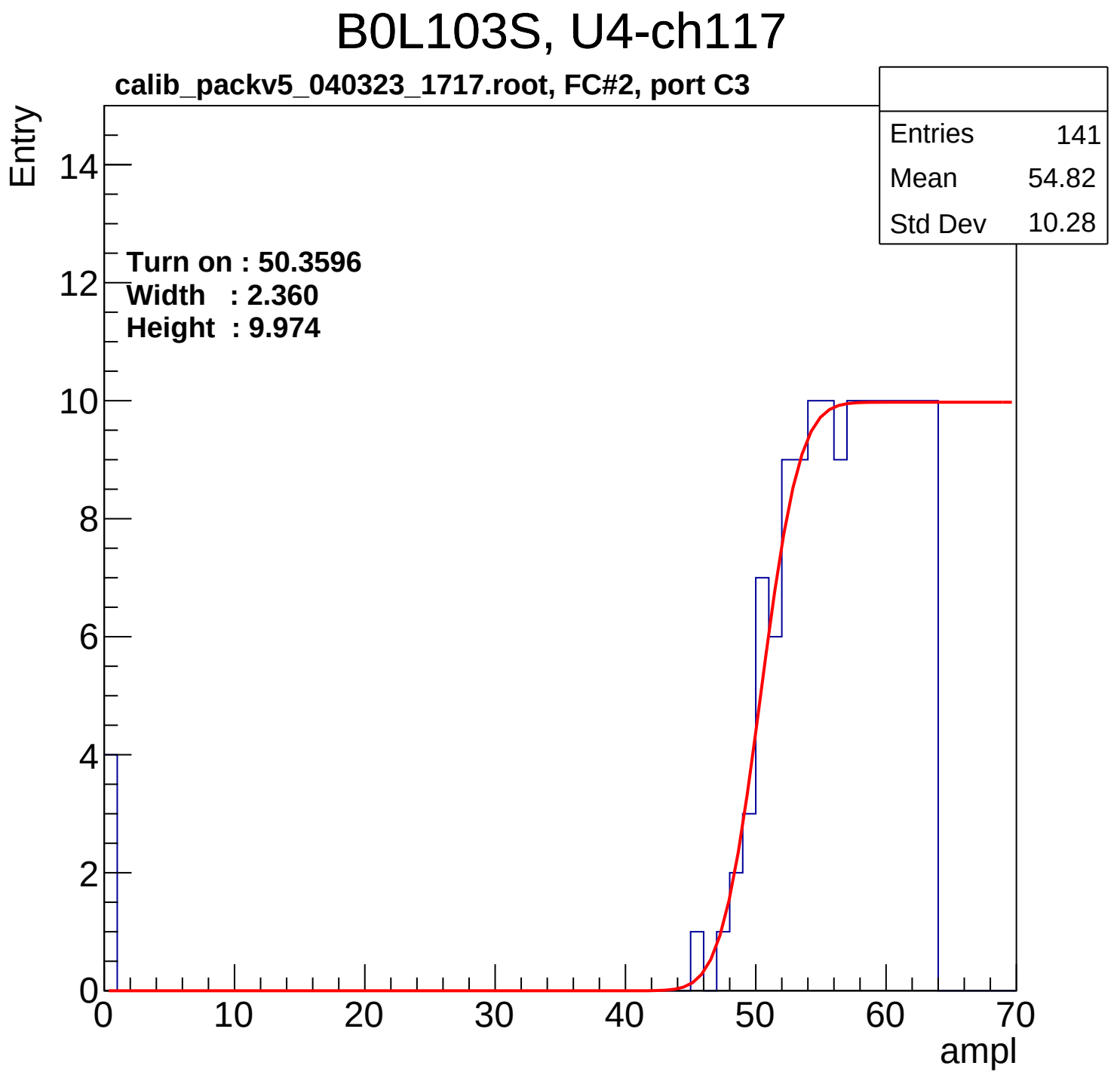
B0L103S, U4-ch117
calib_packv5_040323_1717.root, FC#2, port C3
Entries 141
Mean 54.82
Std Dev 10.28
Turn on : 50.3596
Width : 2.360
Height : 9.974
Entry
ampl
0
2
4
6
8
10
12
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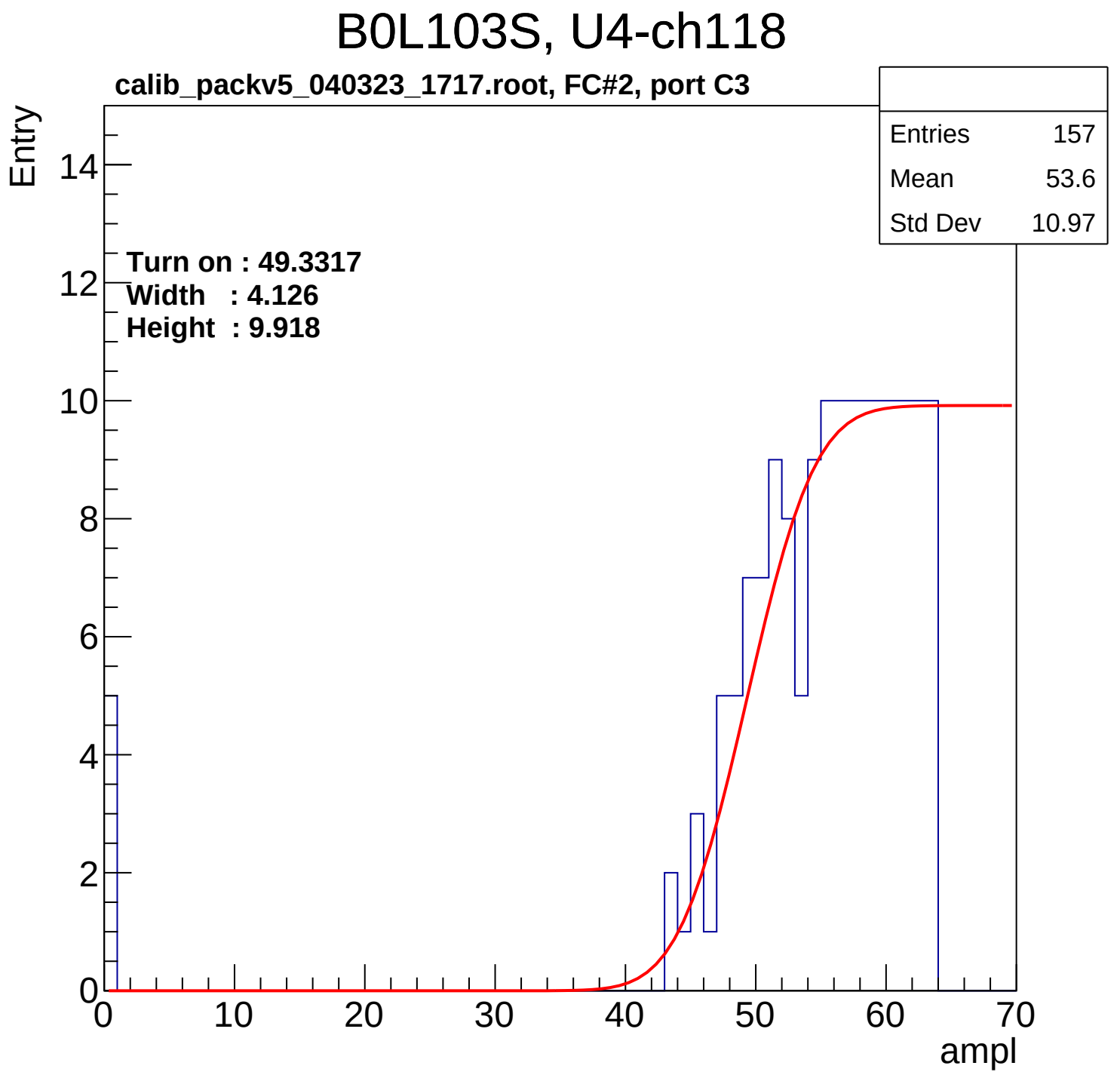
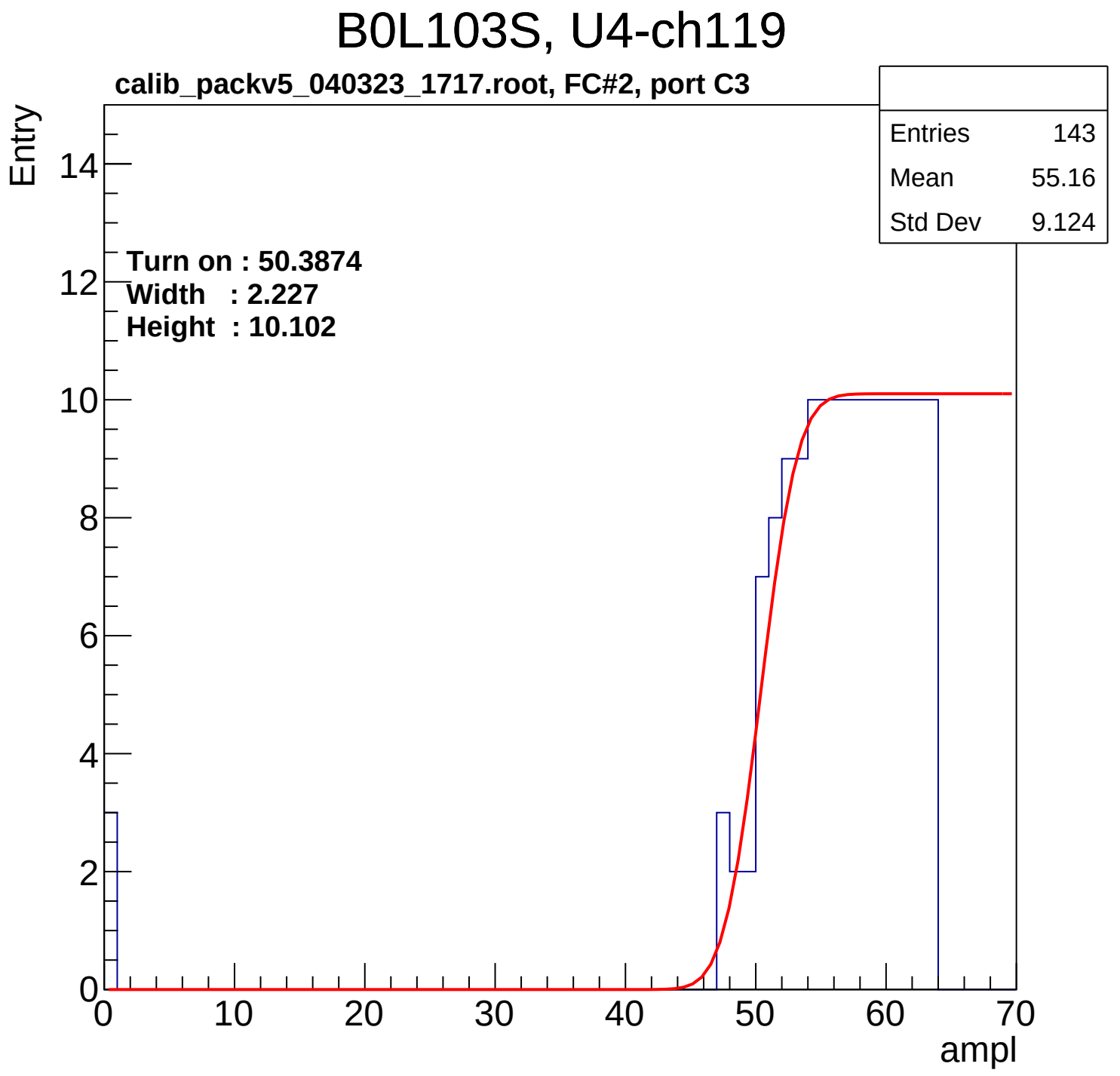
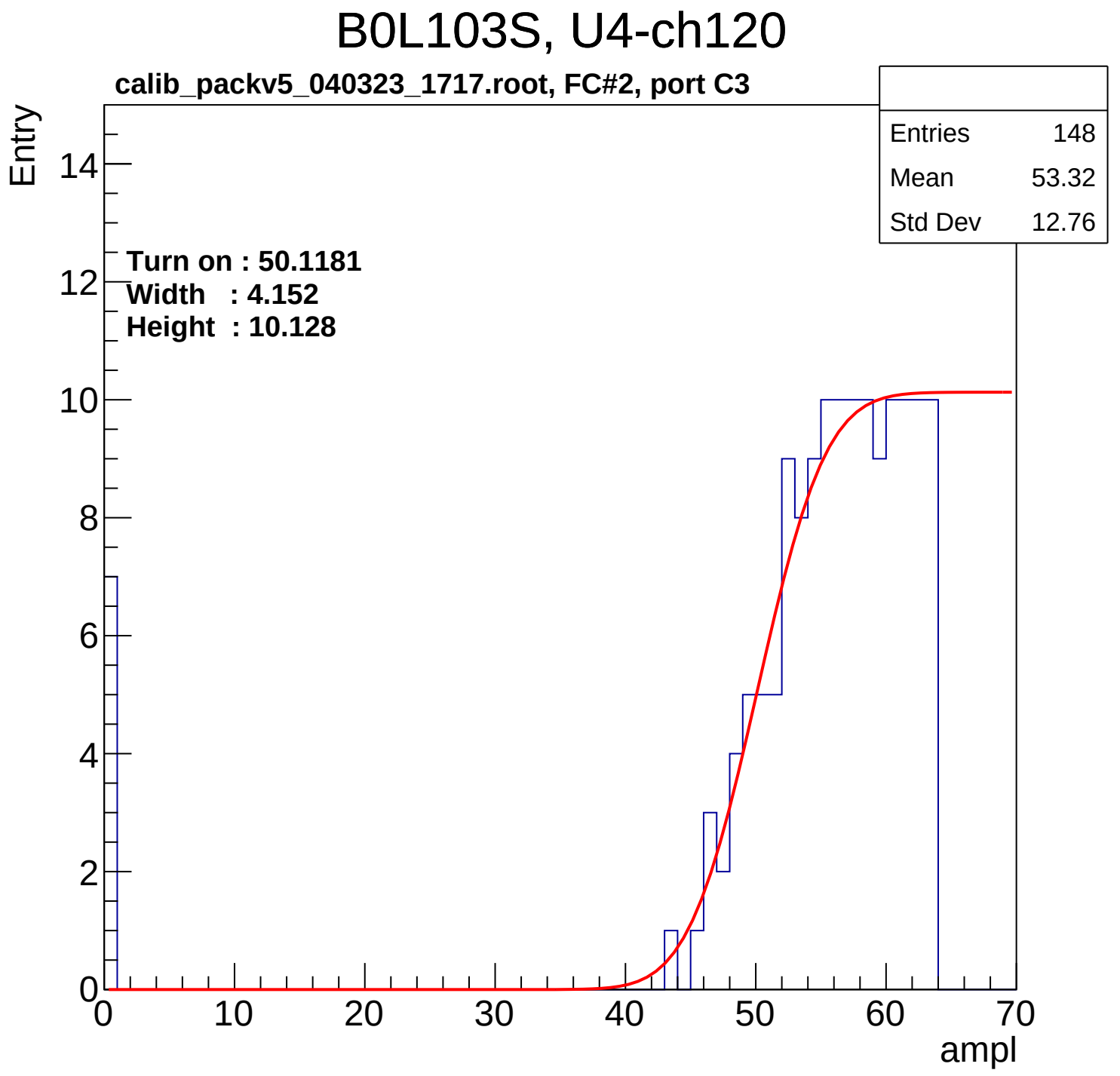
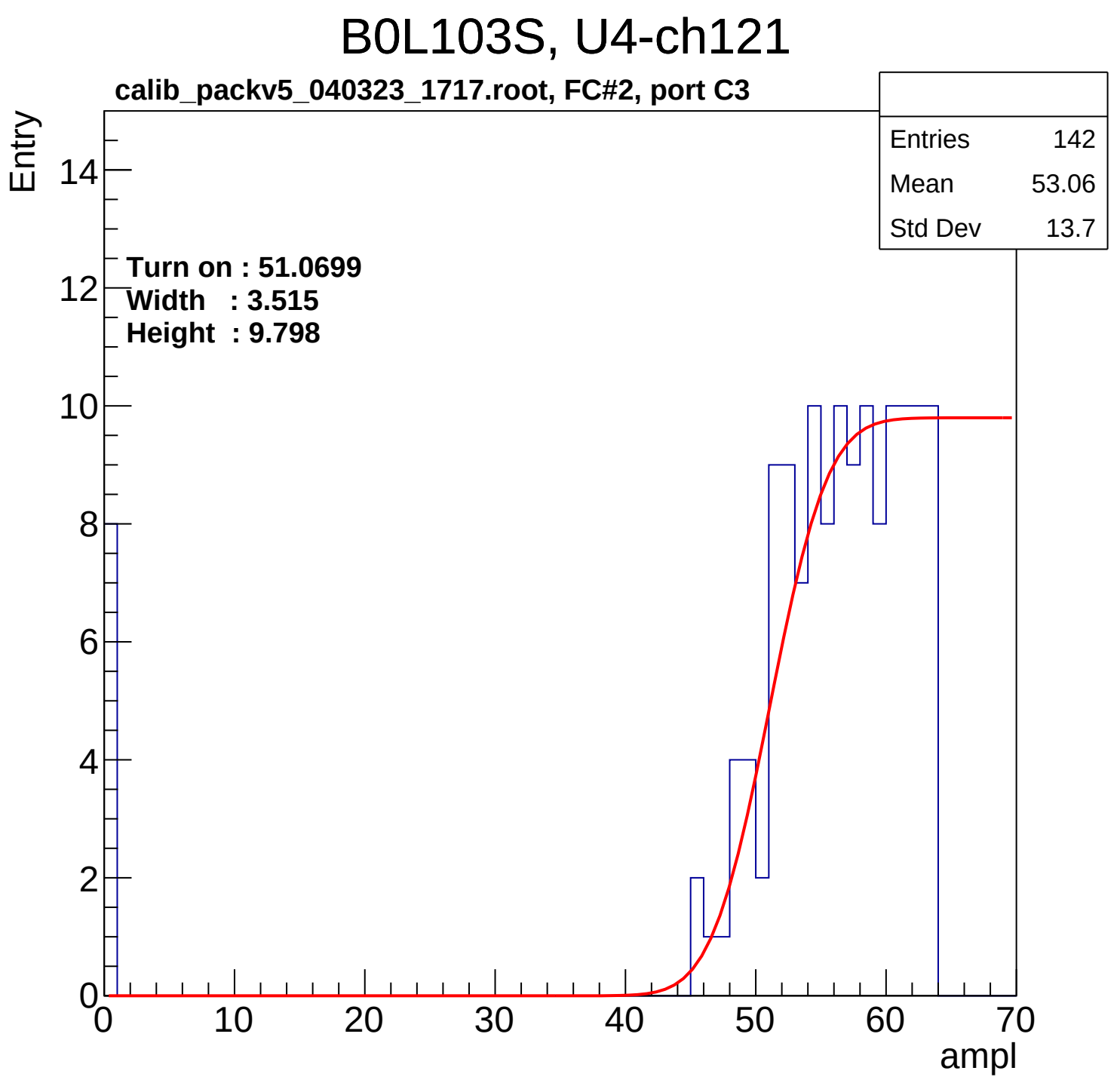
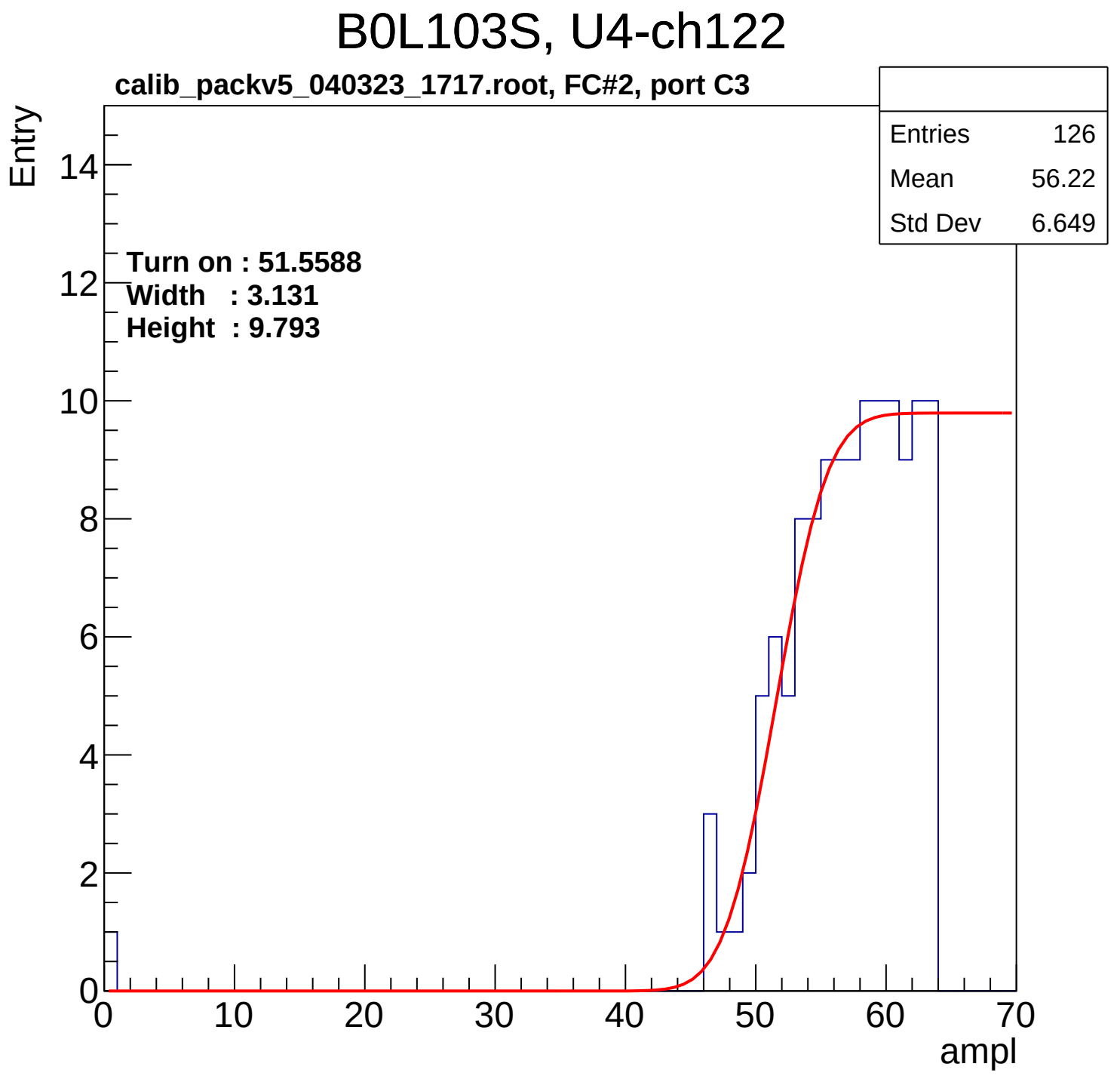

B0L103S, U4-ch118
calib_packv5_040323_1717.root, FC#2, port C3
Entries 157
Mean 53.6
Std Dev 10.97
Turn on : 49.3317
Width : 4.126
Height : 9.918
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L103S, U4-ch119
calib_packv5_040323_1717.root, FC#2, port C3
Entries 143
Mean 55.16
Std Dev 9.124
Turn on : 50.3874
Width : 2.227
Height : 10.102
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L103S, U4-ch120
calib_packv5_040323_1717.root, FC#2, port C3
Entries 148
Mean 53.32
Std Dev 12.76
Turn on : 50.1181
Width : 4.152
Height : 10.128
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L103S, U4-ch121
calib_packv5_040323_1717.root, FC#2, port C3
Entries 142
Mean 53.06
Std Dev 13.7
Turn on : 51.0699
Width : 3.515
Height : 9.798
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L103S, U4-ch122
calib_packv5_040323_1717.root, FC#2, port C3
Entries 126
Mean 56.22
Std Dev 6.649
Turn on : 51.5588
Width : 3.131
Height : 9.793
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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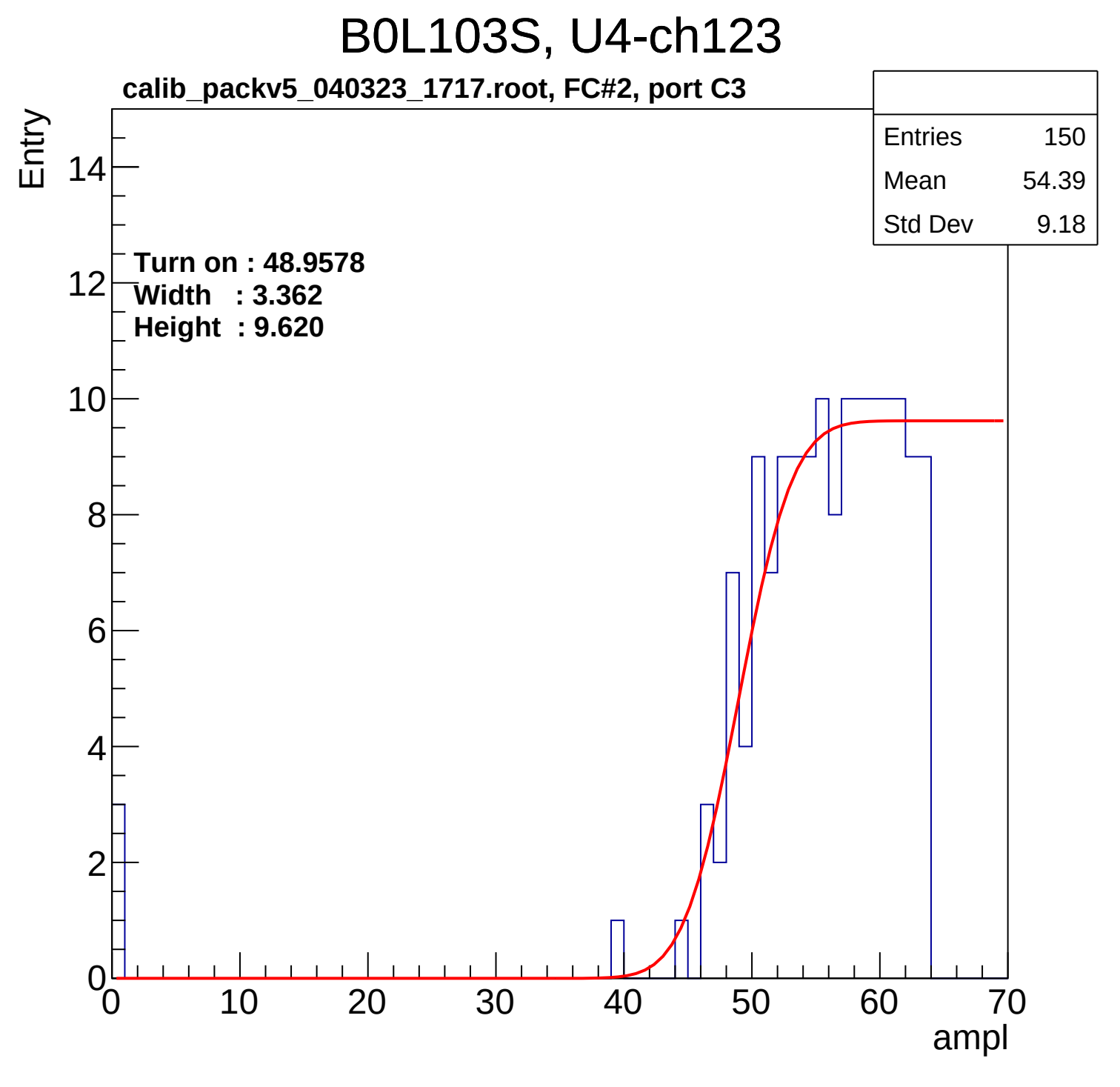
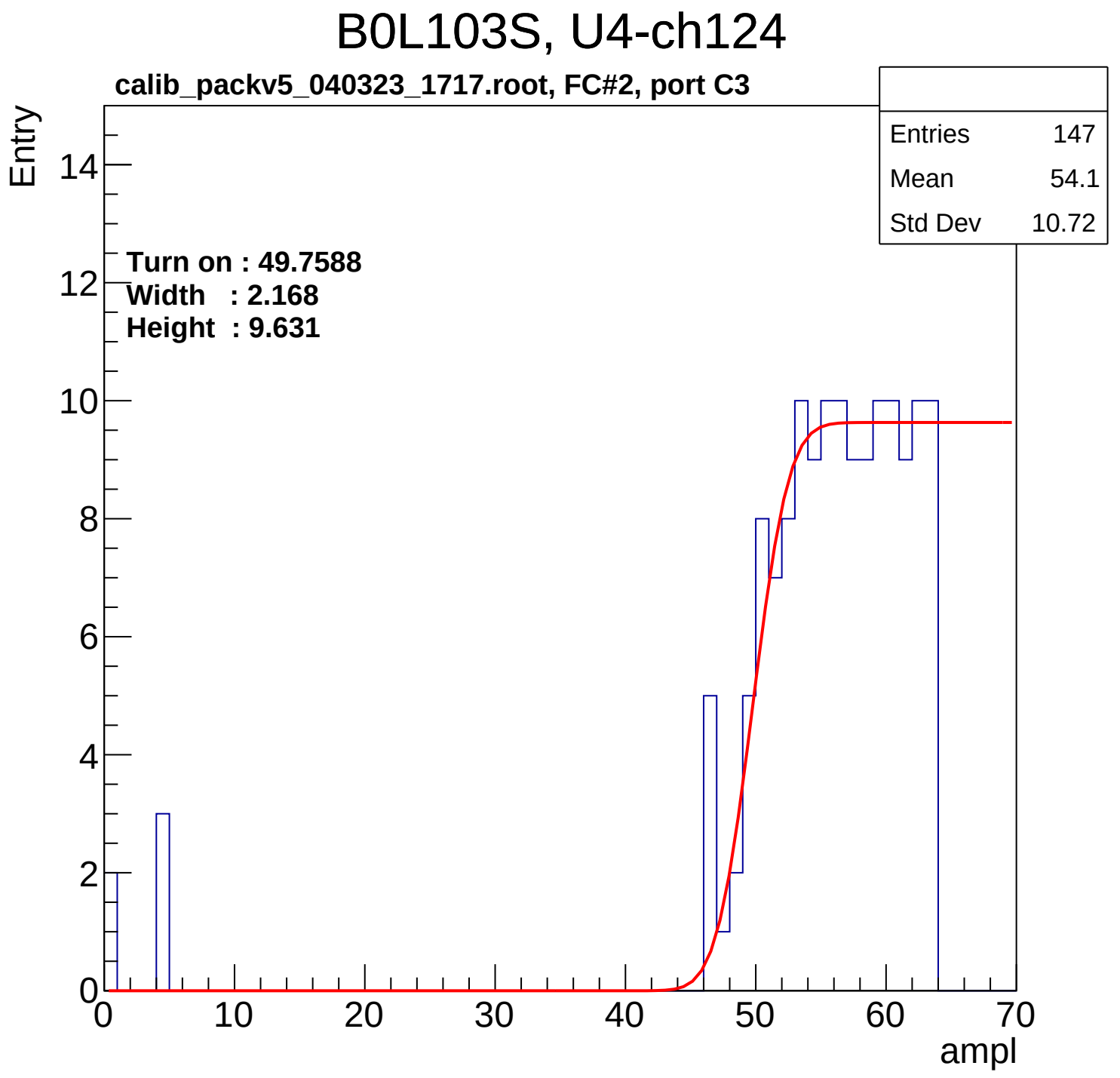
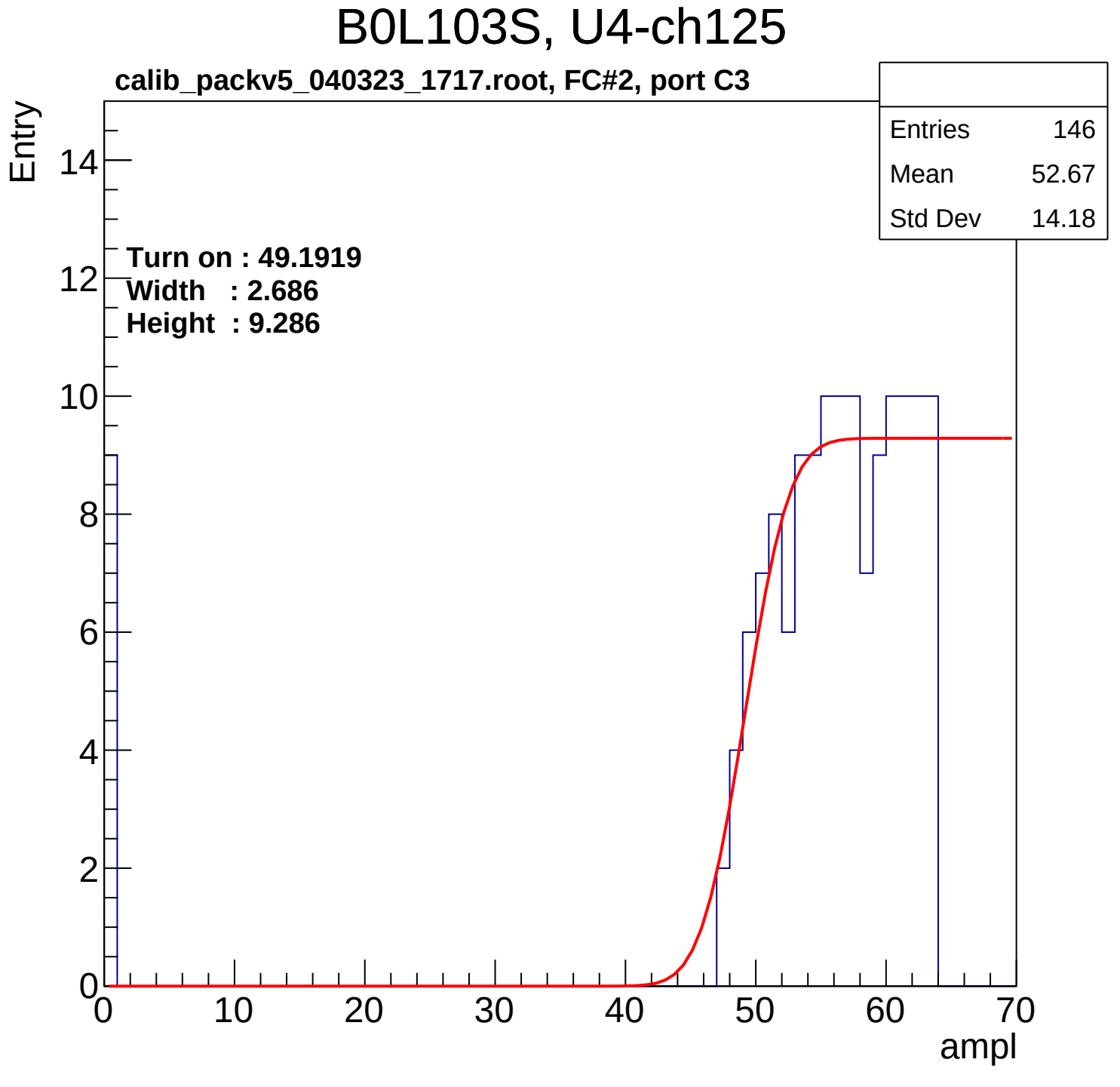
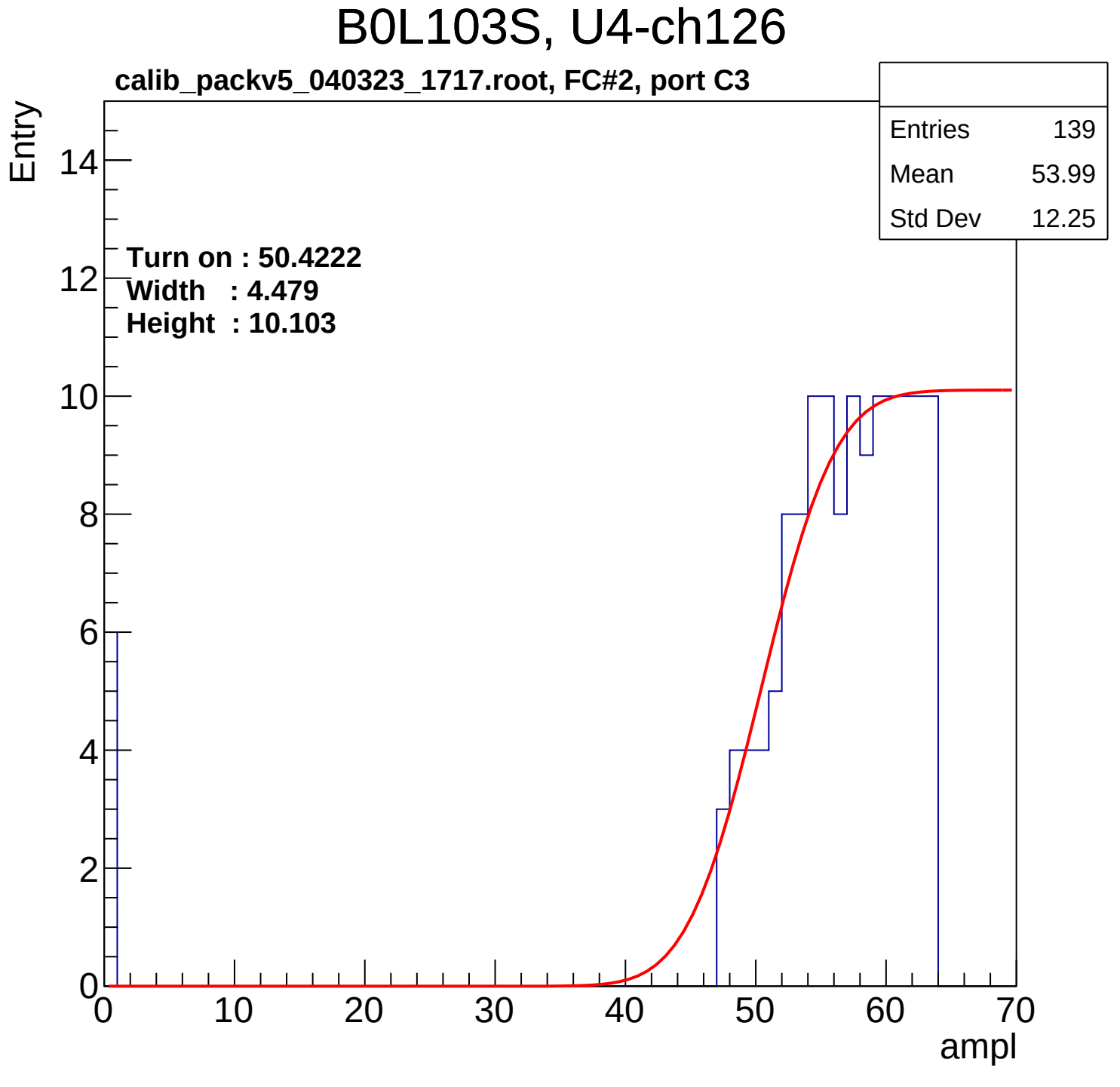

B0L103S, U4-ch123
calib_packv5_040323_1717.root, FC#2, port C3
Entries 150
Mean 54.39
Std Dev 9.18
Turn on : 48.9578
Width : 3.362
Height : 9.620
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L103S, U4-ch124
calib_packv5_040323_1717.root, FC#2, port C3
Entries 147
Mean 54.1
Std Dev 10.72
Turn on : 49.7588
Width : 2.168
Height : 9.631
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L103S, U4-ch125
calib_packv5_040323_1717.root, FC#2, port C3
Entries 146
Mean 52.67
Std Dev 14.18
Turn on : 49.1919
Width : 2.686
Height : 9.286
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L103S, U4-ch126
calib_packv5_040323_1717.root, FC#2, port C3
Entries 139
Mean 53.99
Std Dev 12.25
Turn on : 50.4222
Width : 4.479
Height : 10.103
Entry
ampl
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4
6
8
10
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14
0
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20
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60
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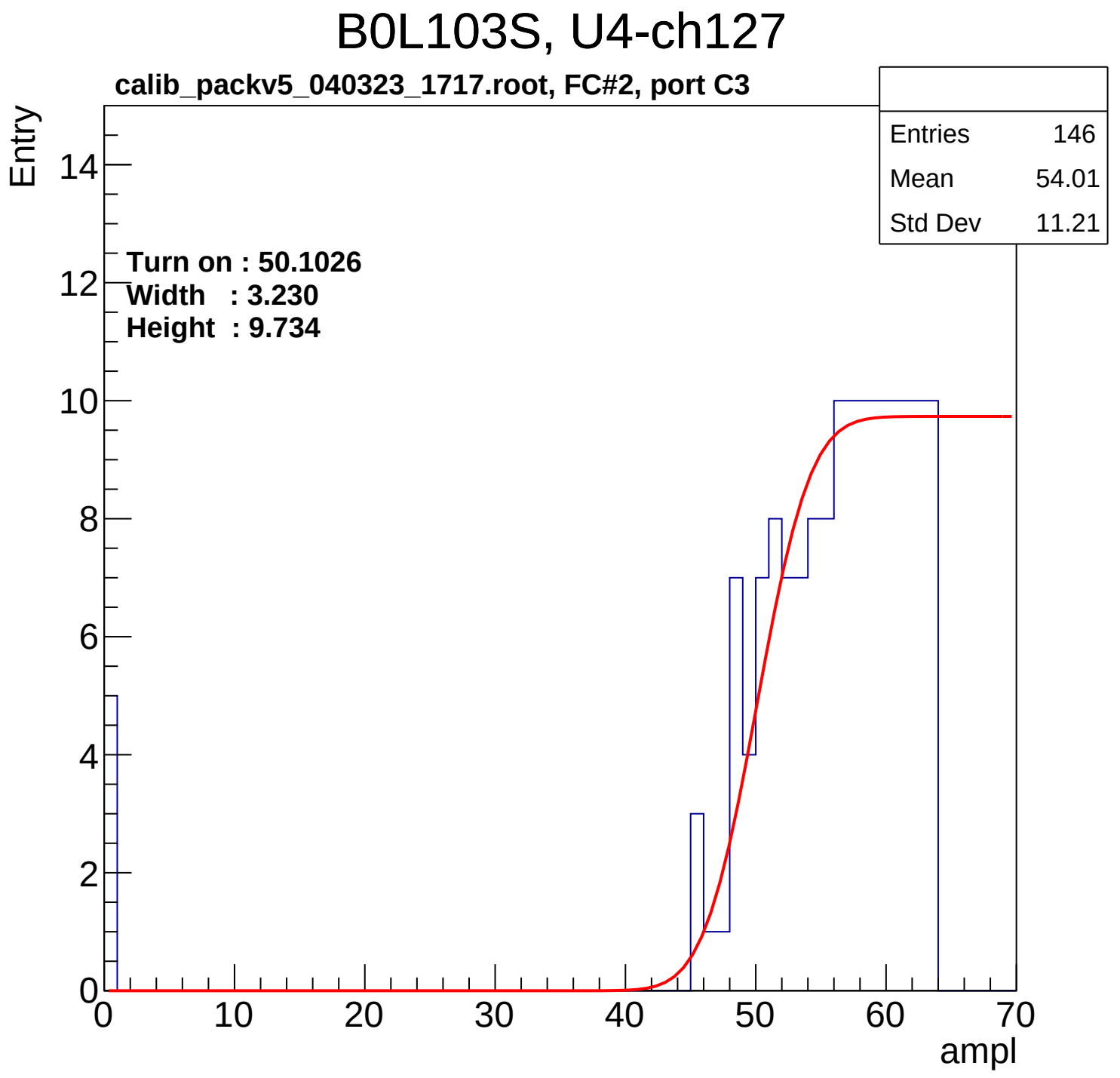
B0L103S, U4-ch127
calib_packv5_040323_1717.root, FC#2, port C3
Entries 146
Mean 54.01
Std Dev 11.21
Turn on : 50.1026
Width : 3.230
Height : 9.734
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
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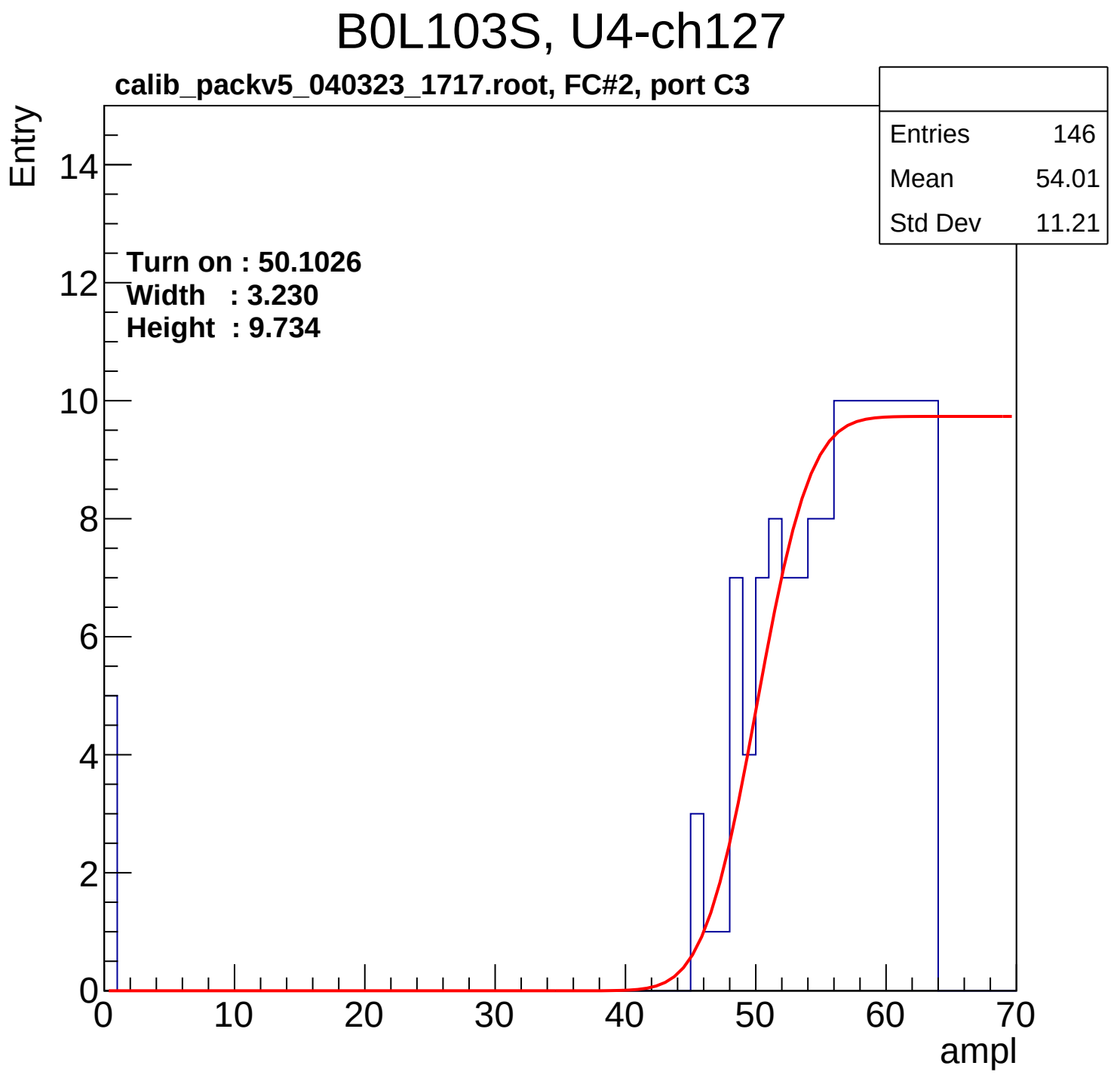
60
70


B0L103S, U4-ch127
calib_packv5_040323_1717.root, FC#2, port C3
Entries 146
Mean 54.01
Std Dev 11.21
Turn on : 50.1026
Width : 3.230
Height : 9.734
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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