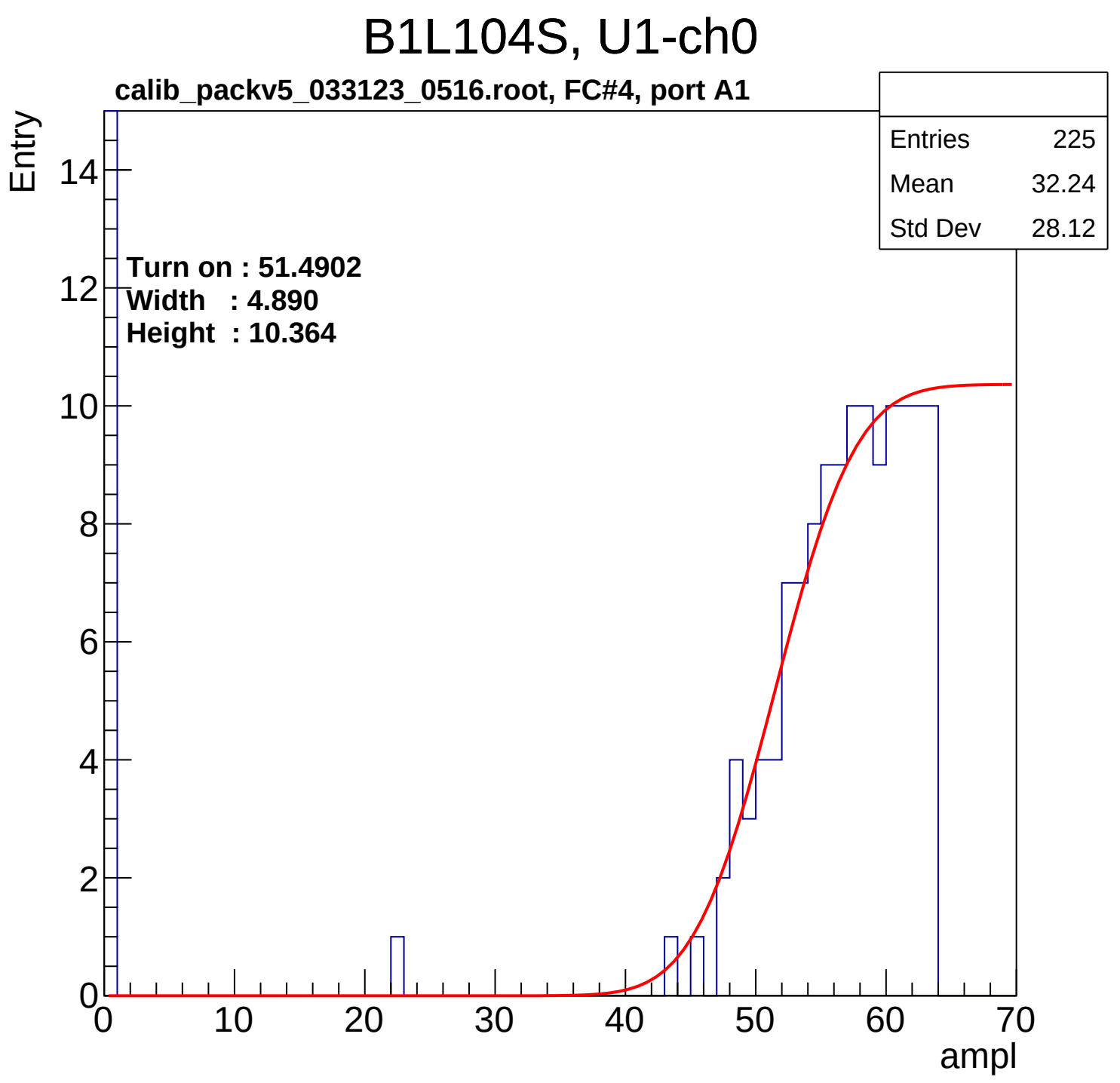
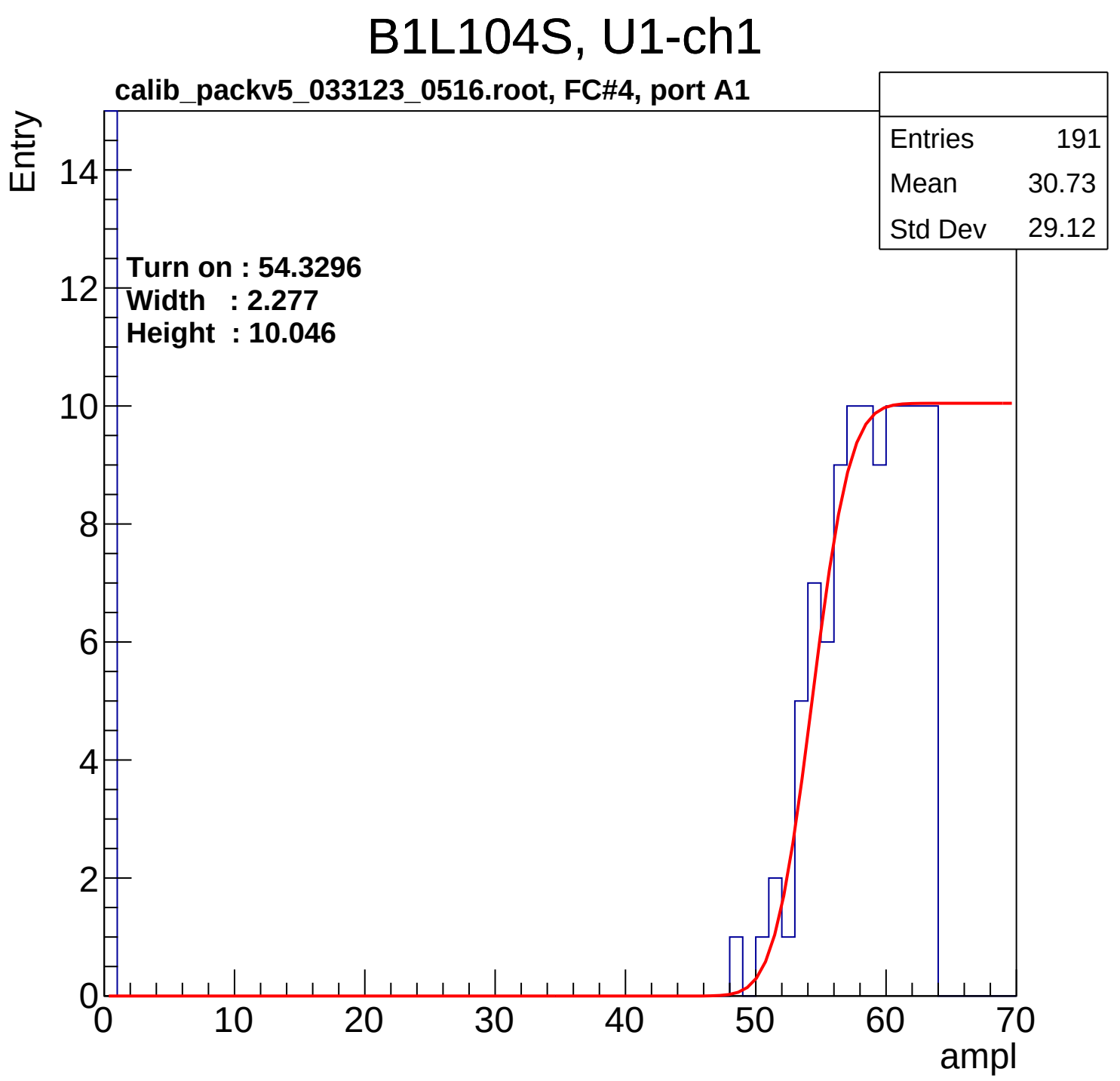
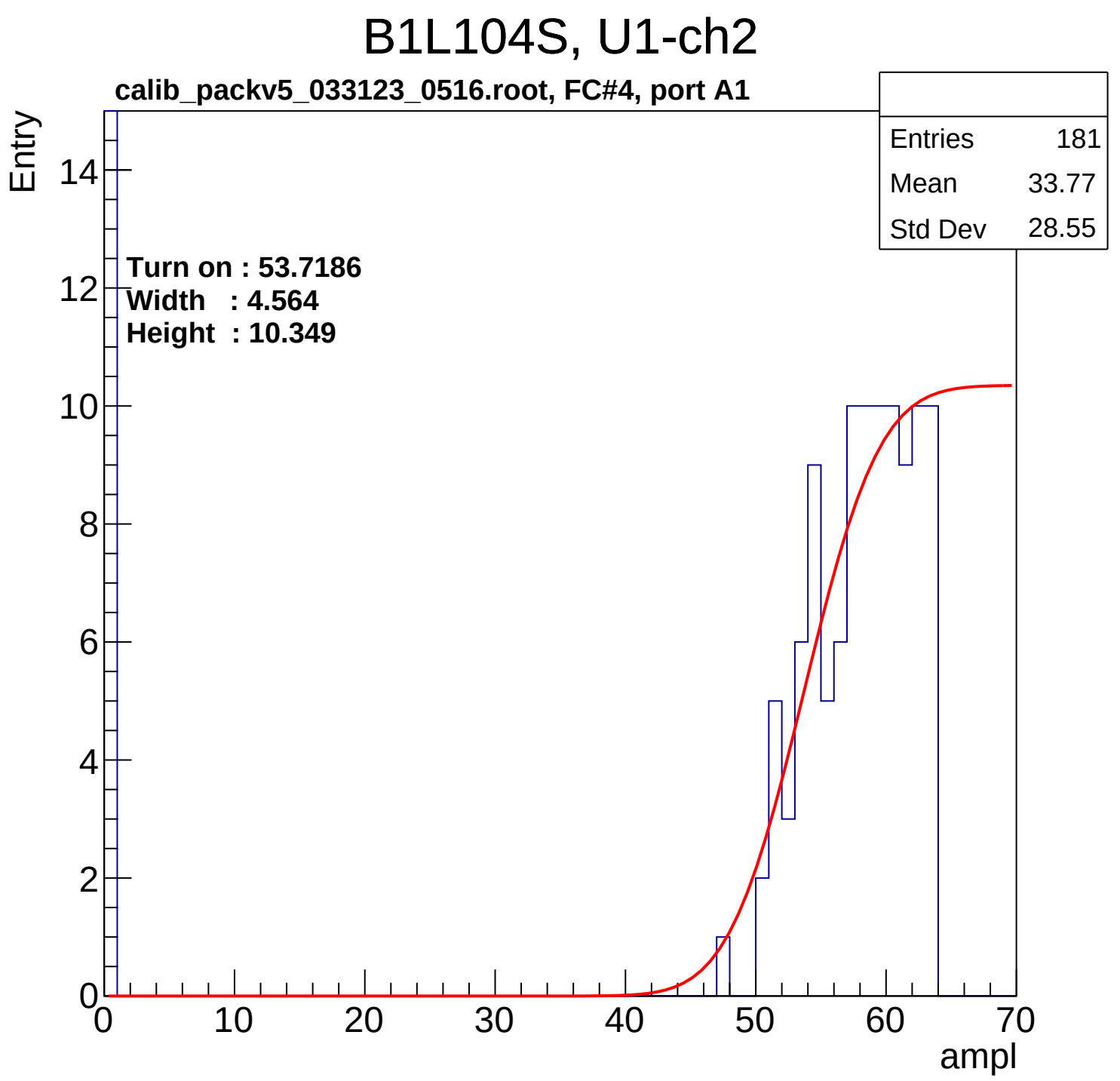
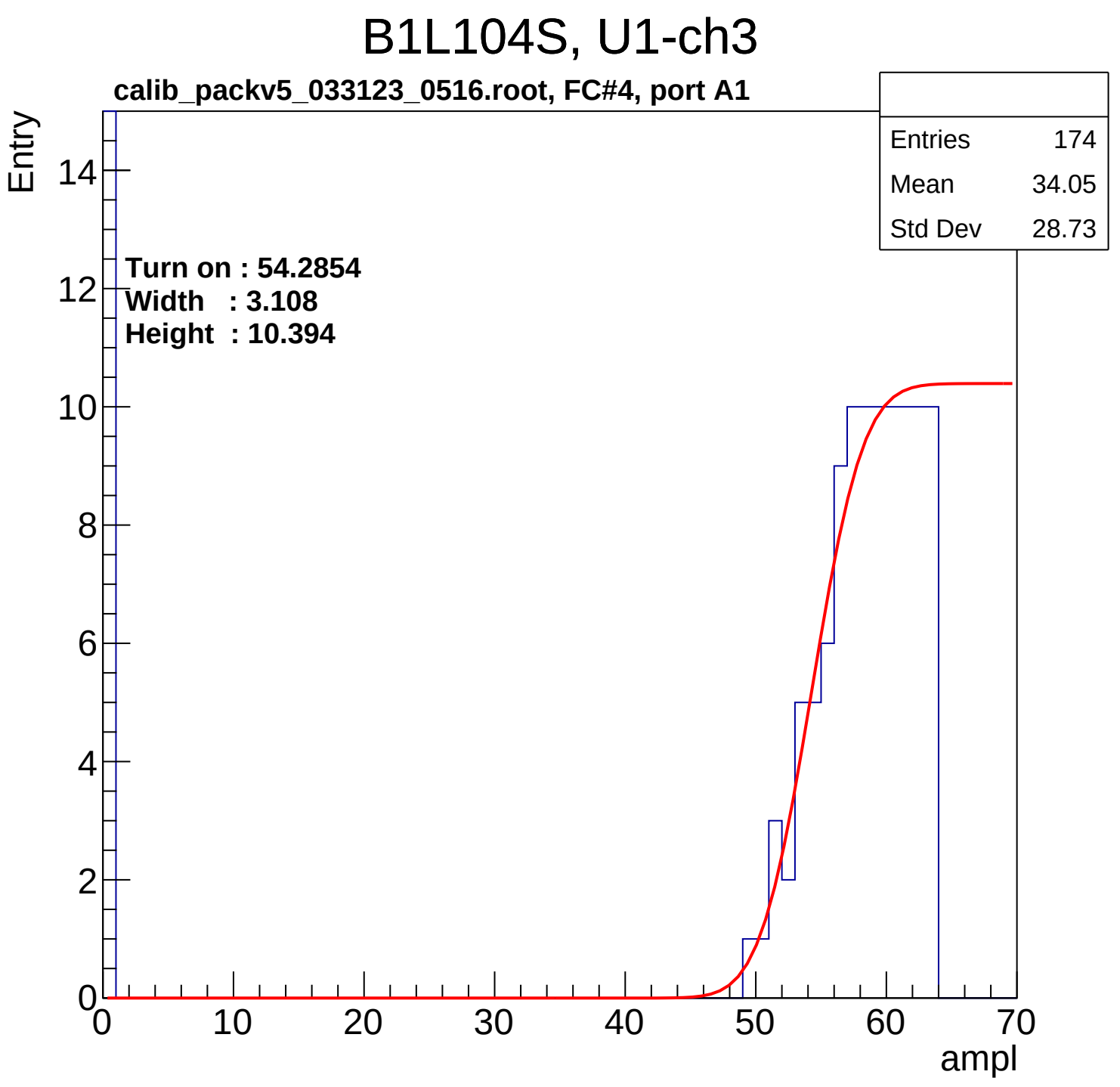
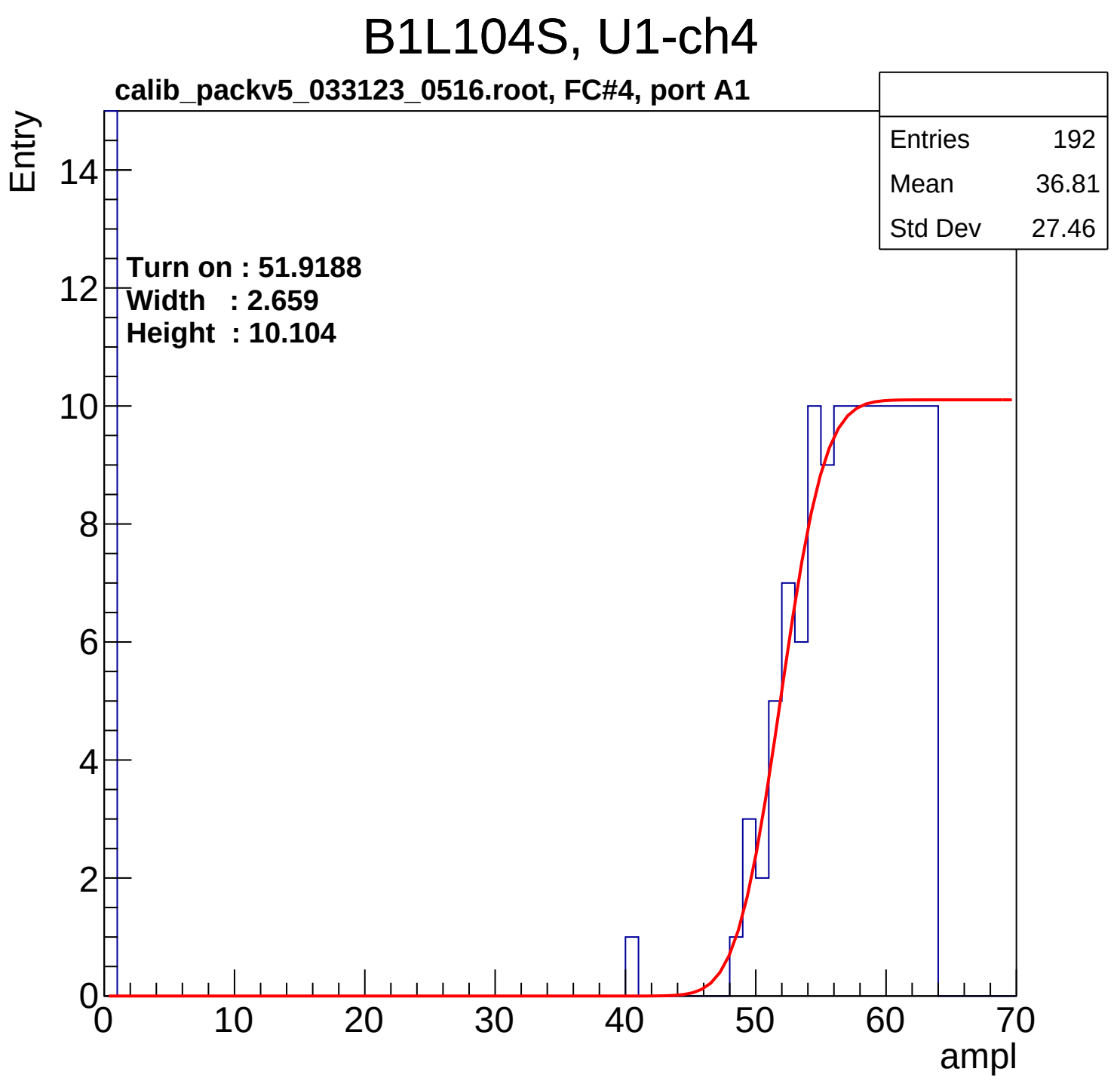
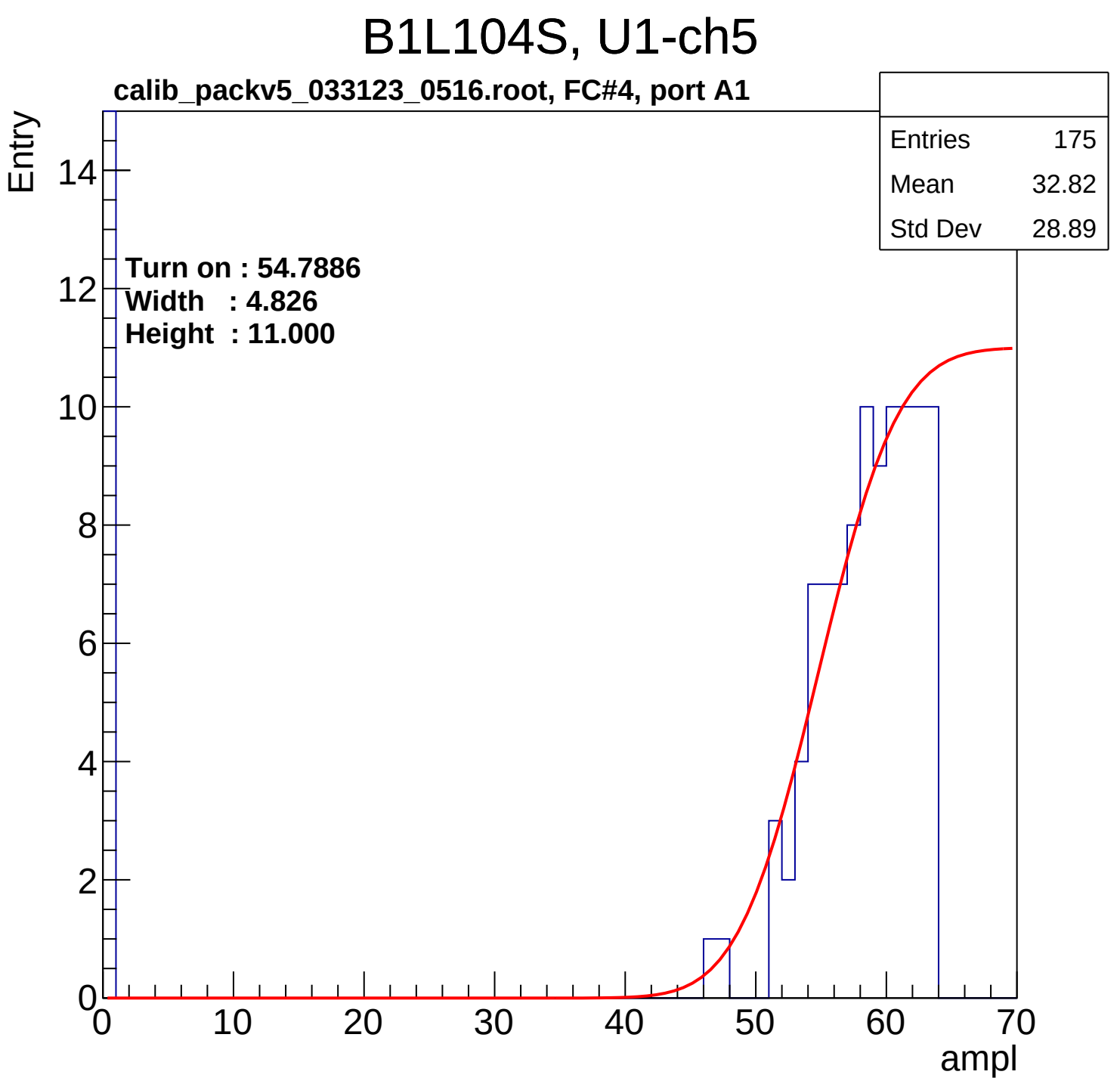

B1L104S, U1-ch0
calib_packv5_033123_0516.root, FC#4, port A1
Entries 225
Mean 32.24
Std Dev 28.12
Turn on : 51.4902
Width : 4.890
Height : 10.364
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

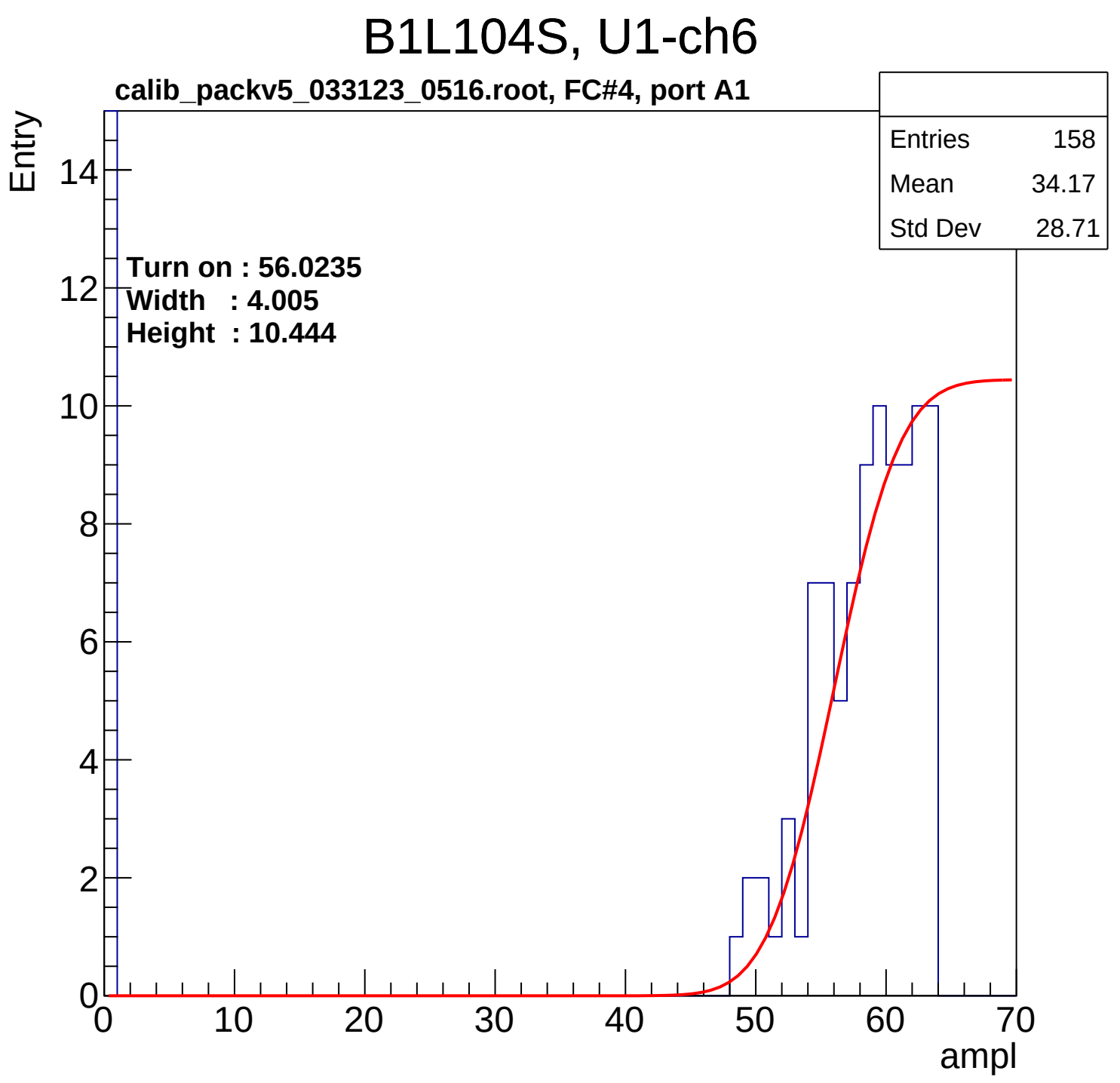

B1L104S, U1-ch1
calib_packv5_033123_0516.root, FC#4, port A1
Entries 191
Mean 30.73
Std Dev 29.12
Turn on : 54.3296
Width : 2.277
Height : 10.046
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

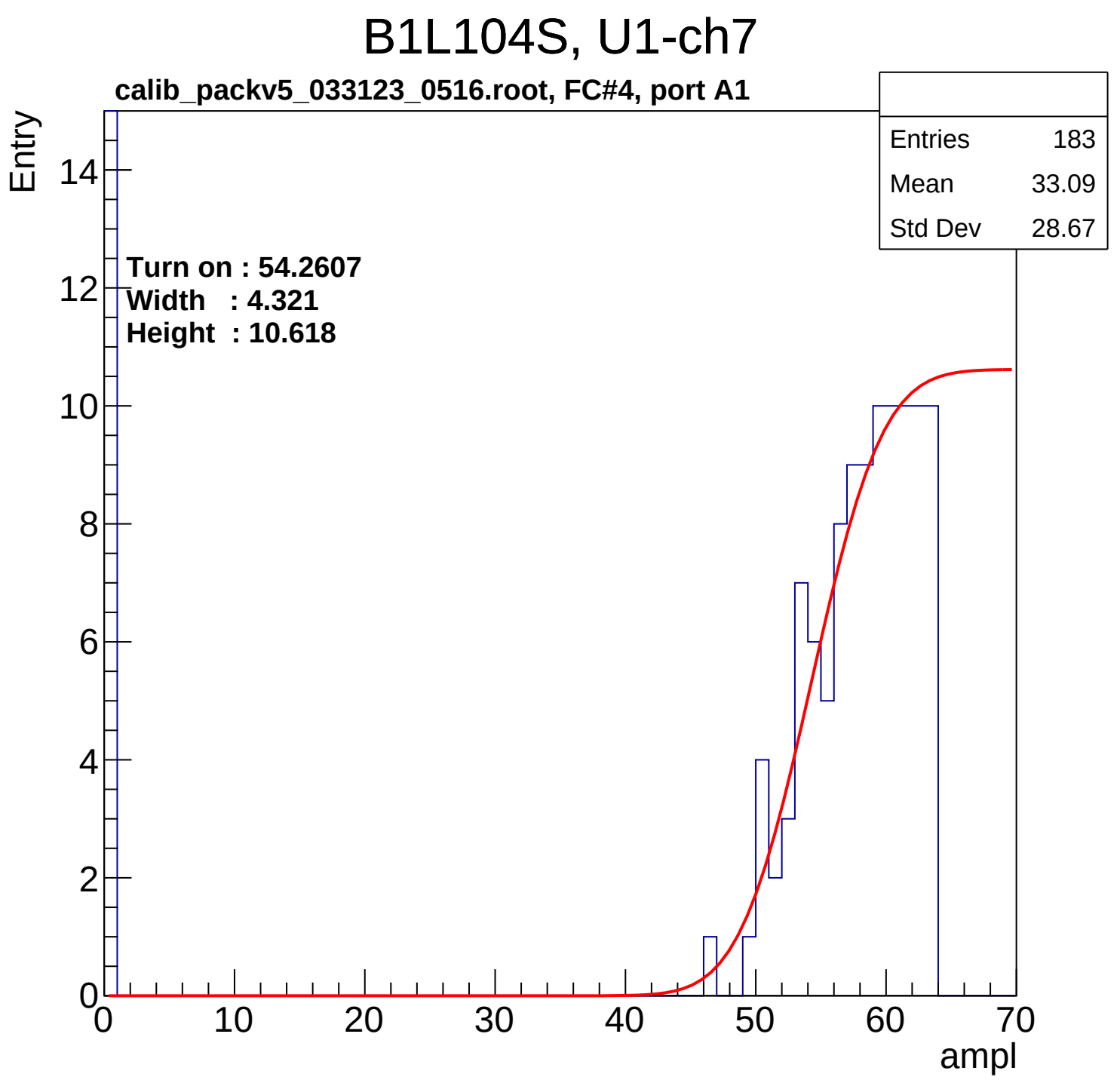

B1L104S, U1-ch2
calib_packv5_033123_0516.root, FC#4, port A1
Entries 181
Mean 33.77
Std Dev 28.55
Turn on : 53.7186
Width : 4.564
Height : 10.349
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

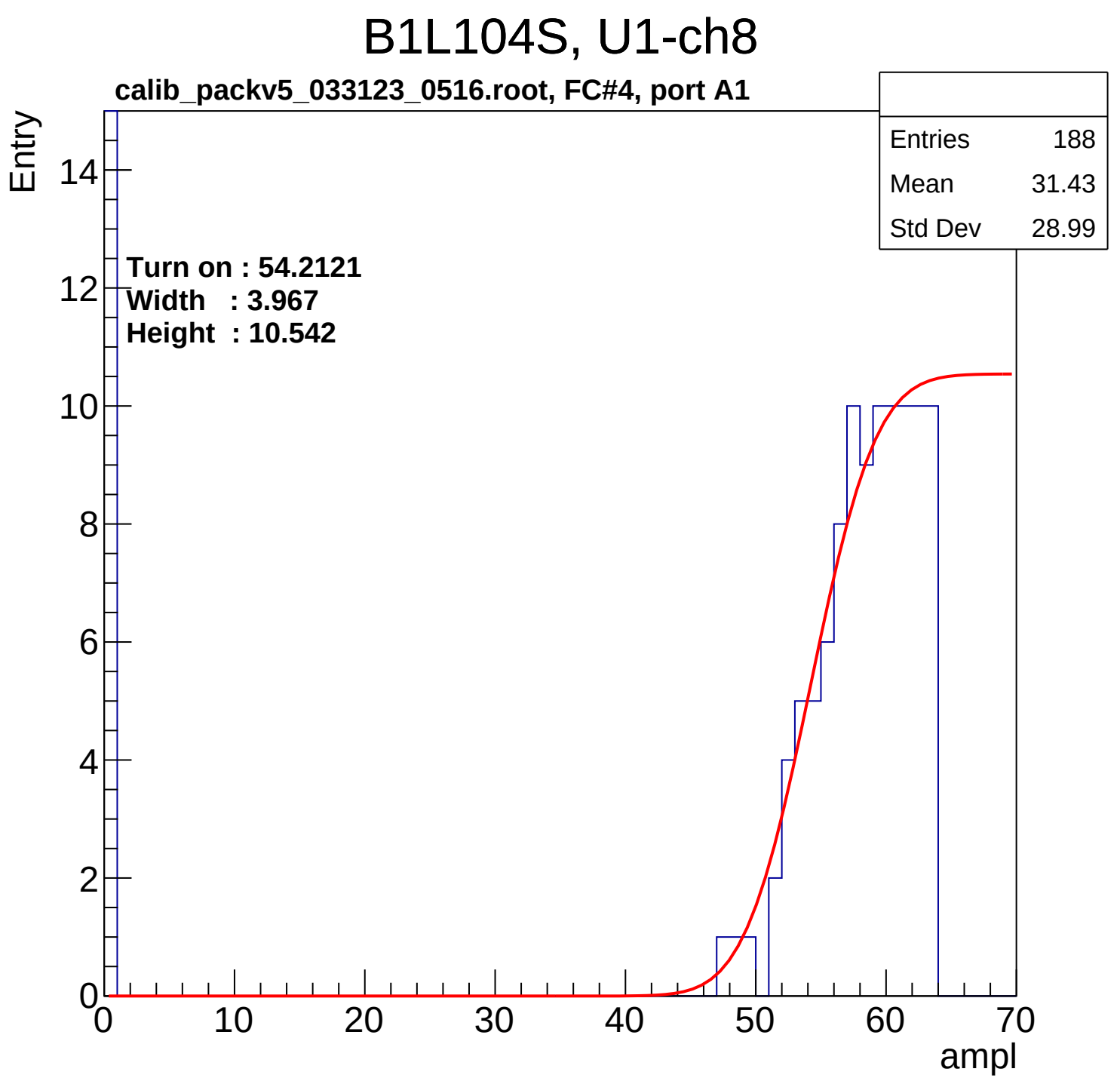

B1L104S, U1-ch3
calib_packv5_033123_0516.root, FC#4, port A1
Entries 174
Mean 34.05
Std Dev 28.73
Turn on : 54.2854
Width : 3.108
Height : 10.394
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

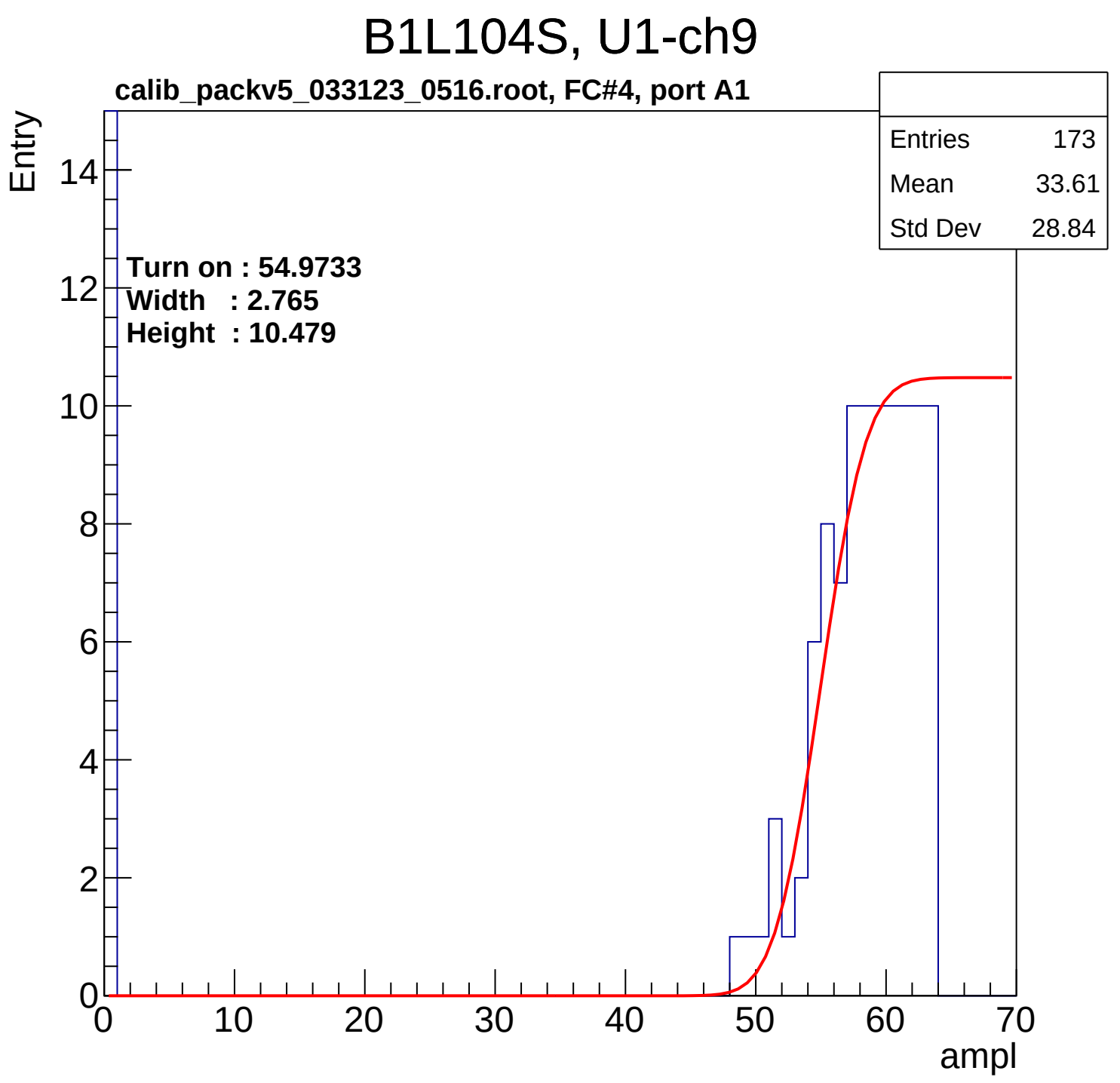

B1L104S, U1-ch4
calib_packv5_033123_0516.root, FC#4, port A1
Entries 192
Mean 36.81
Std Dev 27.46
Turn on : 51.9188
Width : 2.659
Height : 10.104
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

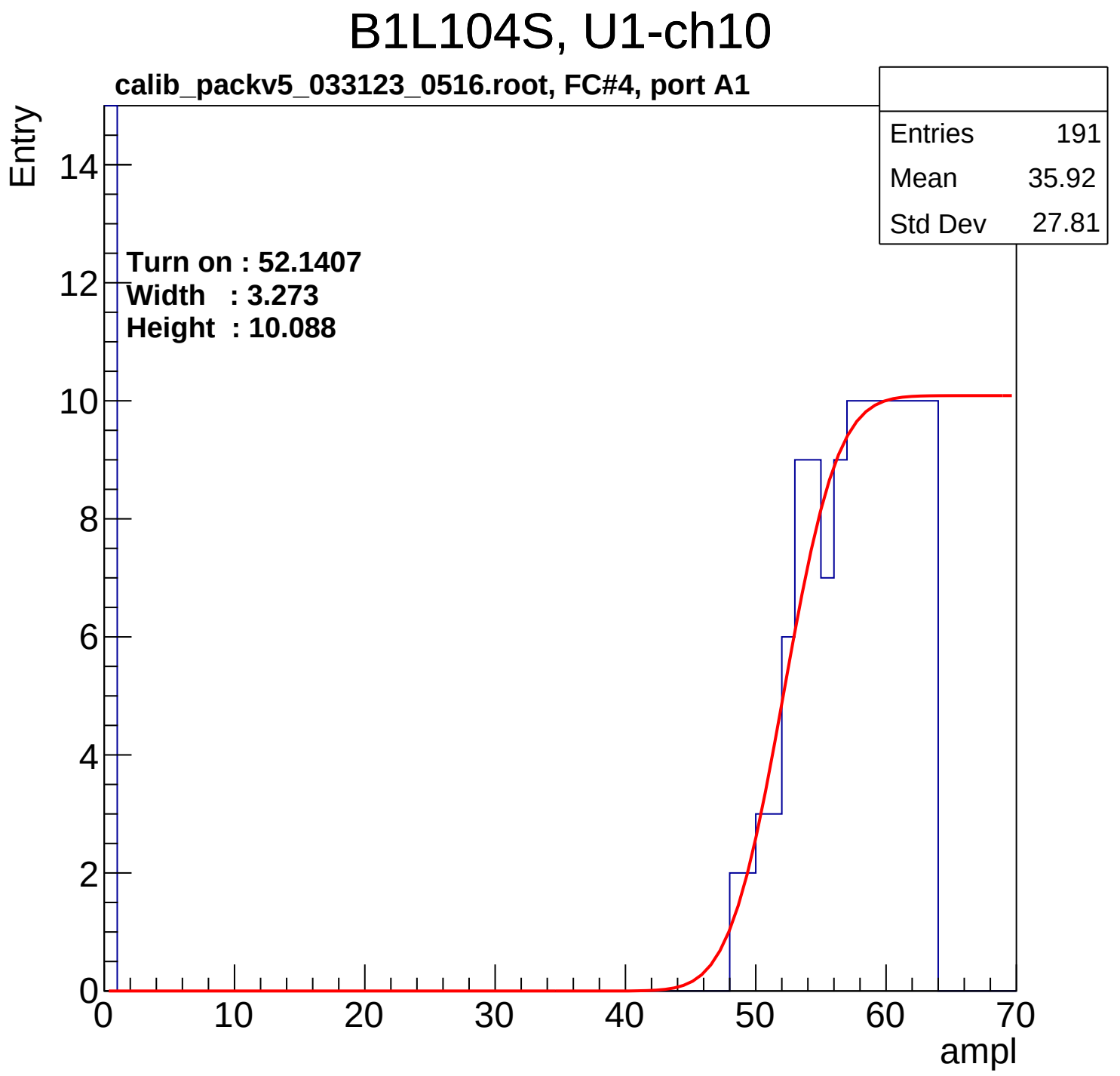

B1L104S, U1-ch5
calib_packv5_033123_0516.root, FC#4, port A1
Entries 175
Mean 32.82
Std Dev 28.89
Turn on : 54.7886
Width : 4.826
Height : 11.000
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

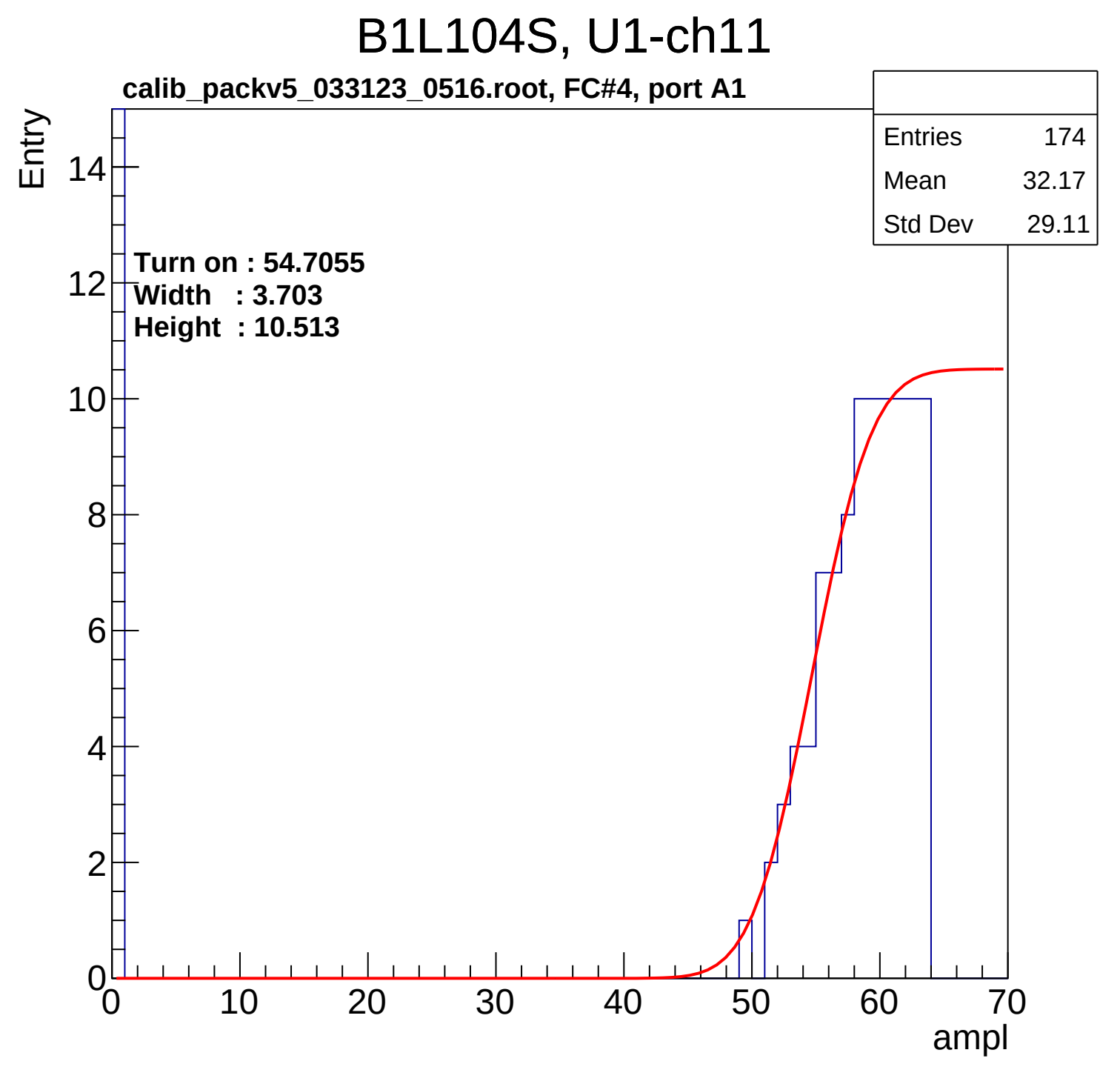

B1L104S, U1-ch6
calib_packv5_033123_0516.root, FC#4, port A1
Entries 158
Mean 34.17
Std Dev 28.71
Turn on : 56.0235
Width : 4.005
Height : 10.444
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

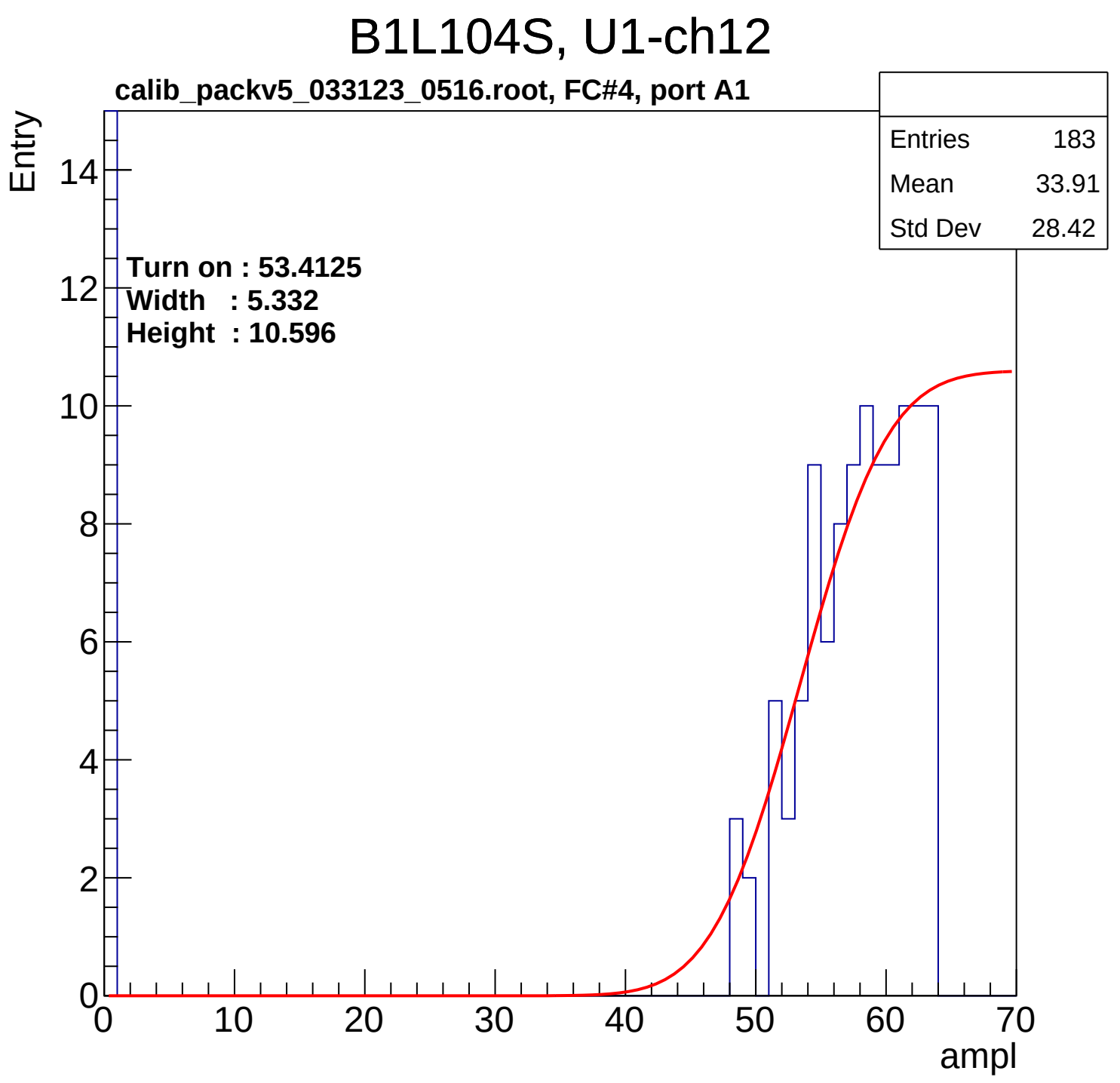

B1L104S, U1-ch7
calib_packv5_033123_0516.root, FC#4, port A1
Entries 183
Mean 33.09
Std Dev 28.67
Turn on : 54.2607
Width : 4.321
Height : 10.618
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

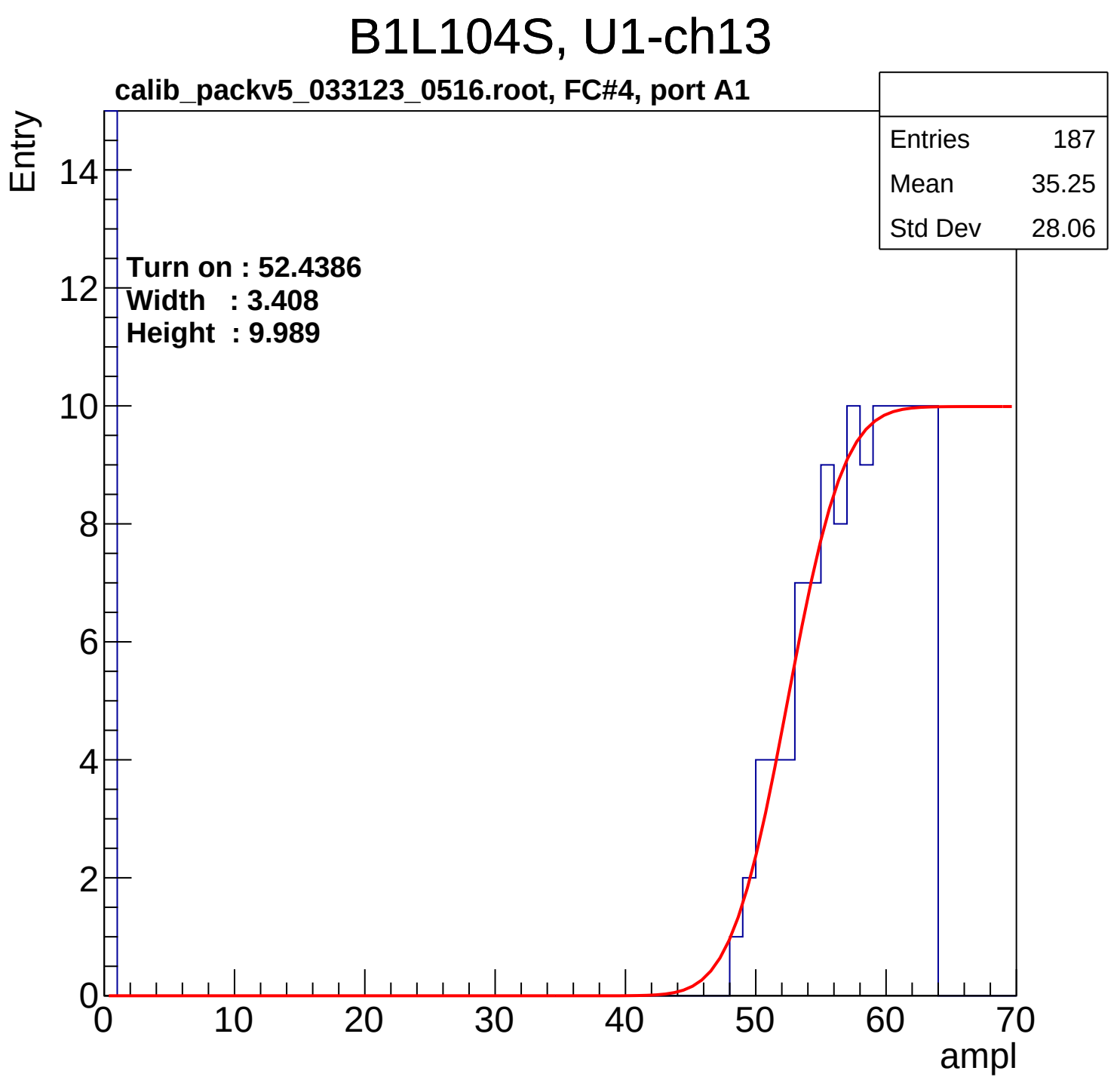

B1L104S, U1-ch8
calib_packv5_033123_0516.root, FC#4, port A1
Entries 188
Mean 31.43
Std Dev 28.99
Turn on : 54.2121
Width : 3.967
Height : 10.542
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

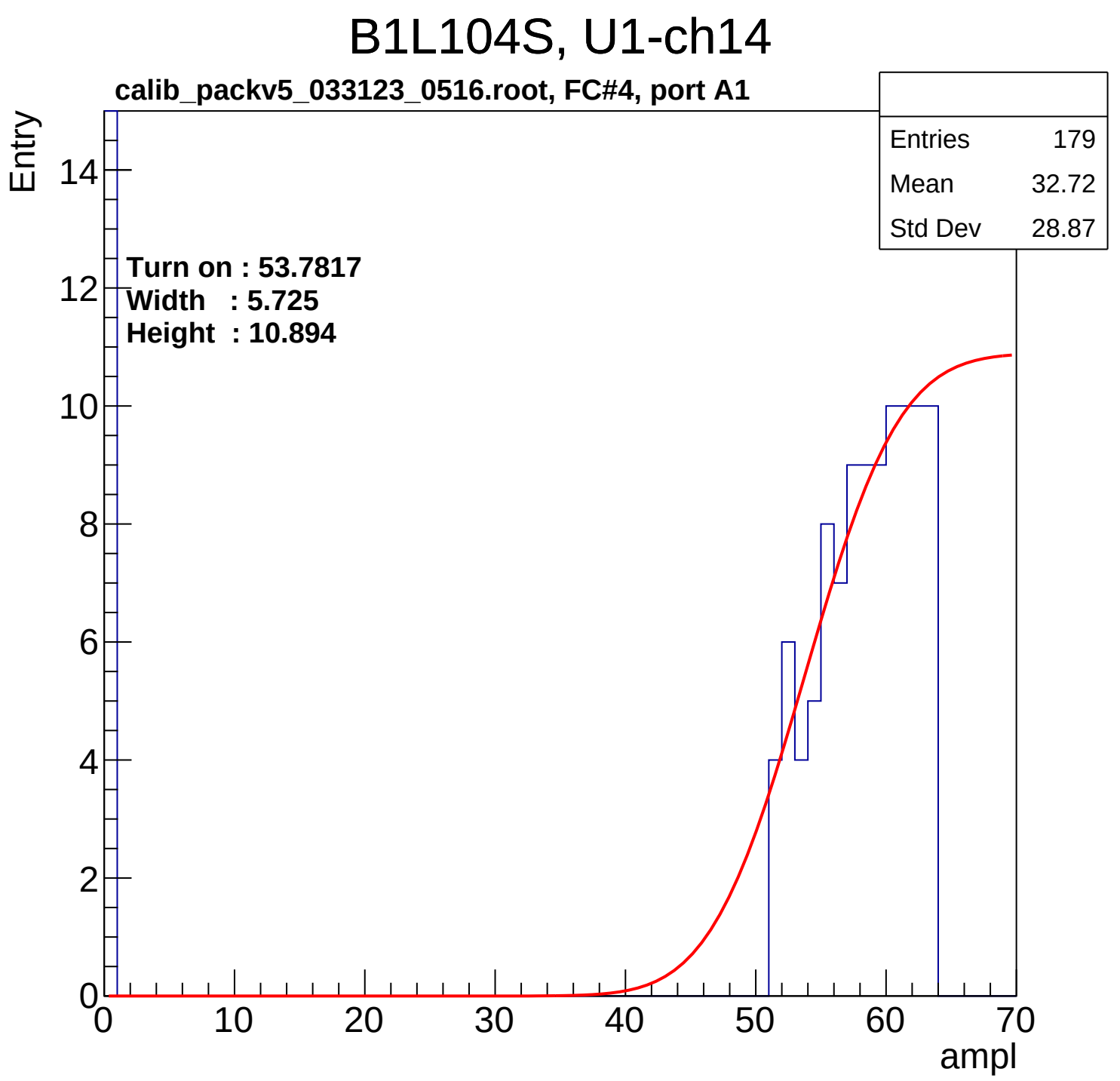

B1L104S, U1-ch9
calib_packv5_033123_0516.root, FC#4, port A1
Entries 173
Mean 33.61
Std Dev 28.84
Turn on : 54.9733
Width : 2.765
Height : 10.479
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

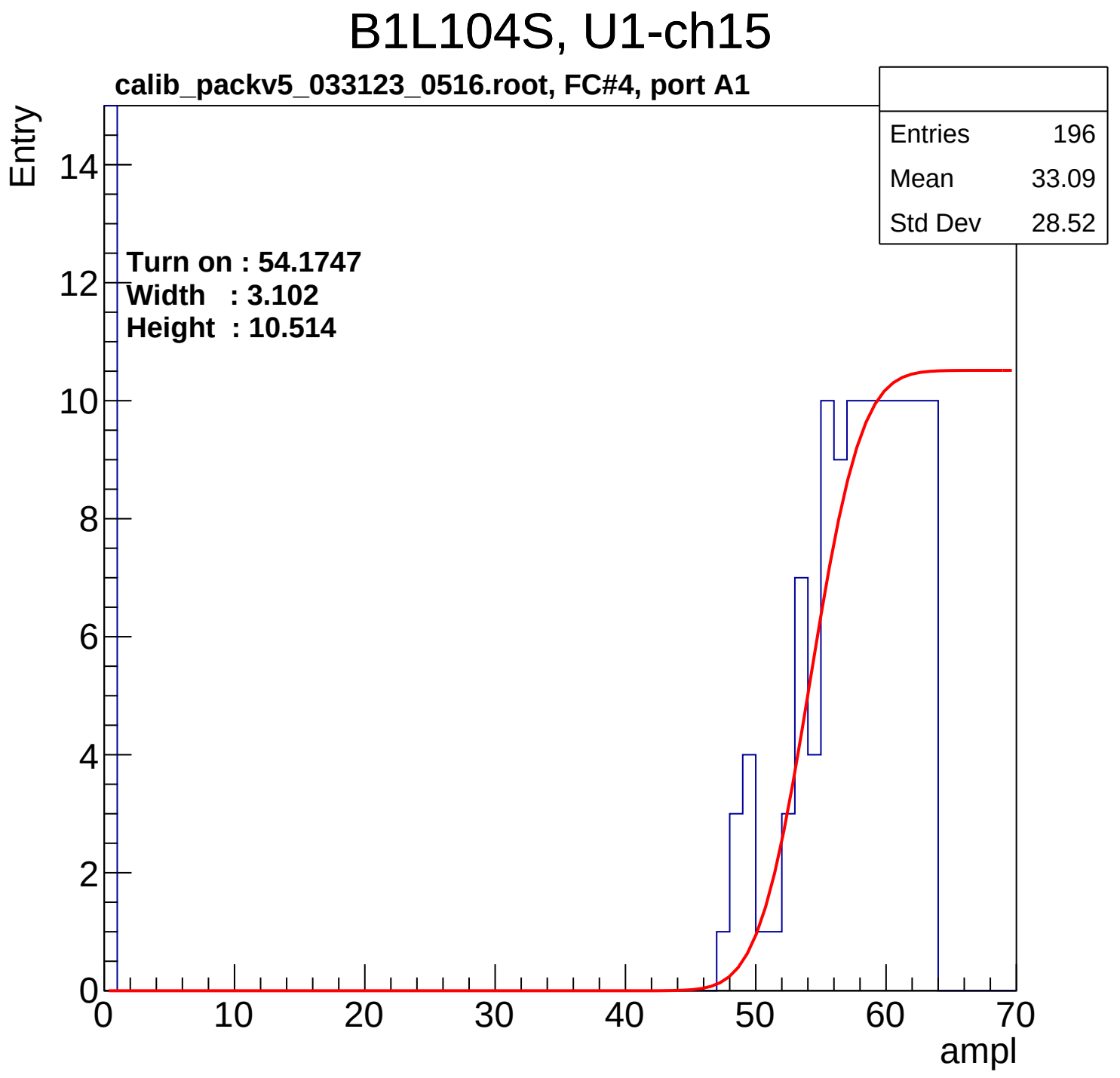

B1L104S, U1-ch10
calib_packv5_033123_0516.root, FC#4, port A1
Entries 191
Mean 35.92
Std Dev 27.81
Turn on : 52.1407
Width : 3.273
Height : 10.088
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

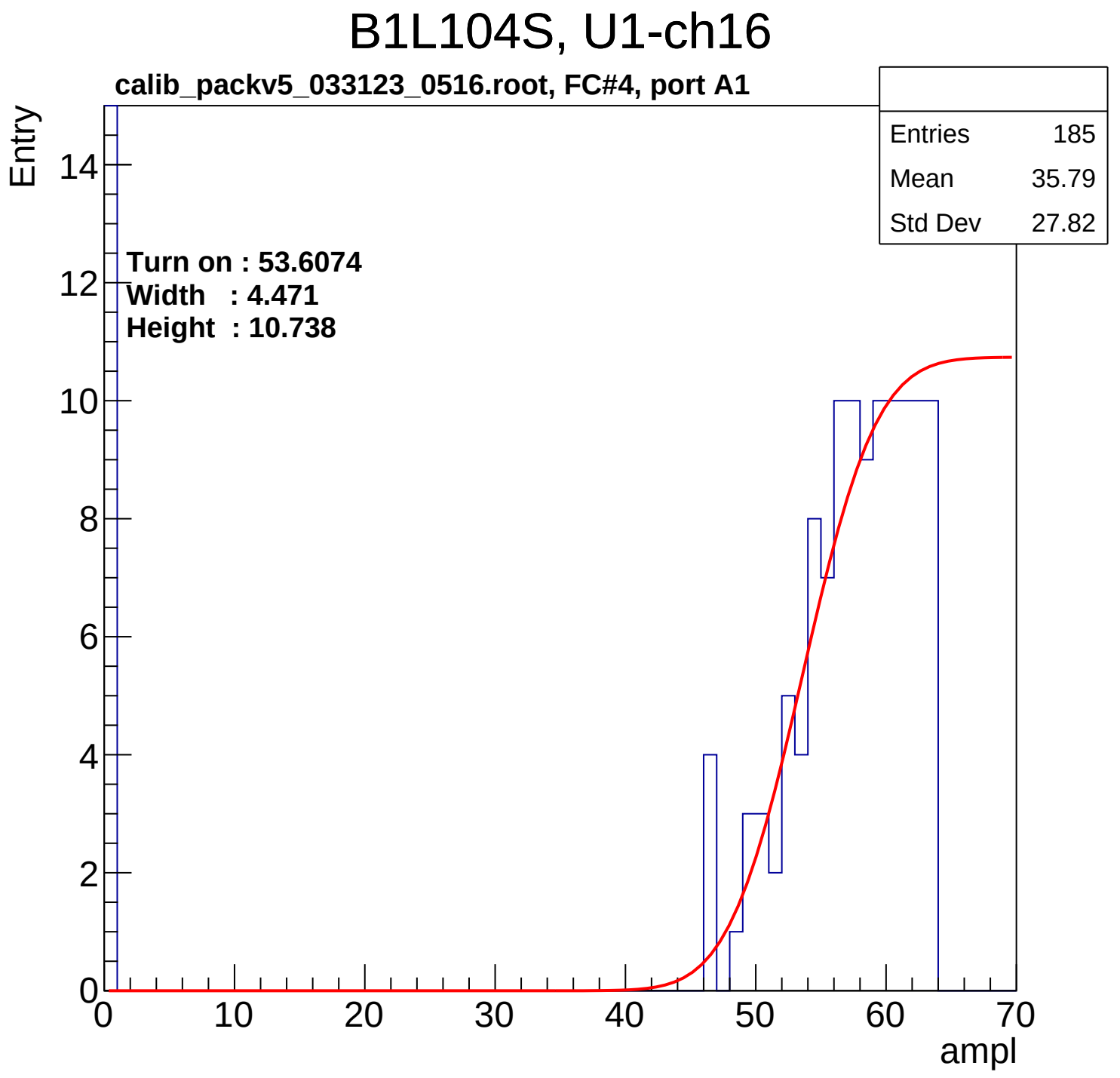

B1L104S, U1-ch11
calib_packv5_033123_0516.root, FC#4, port A1
Entries 174
Mean 32.17
Std Dev 29.11
Turn on : 54.7055
Width : 3.703
Height : 10.513
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

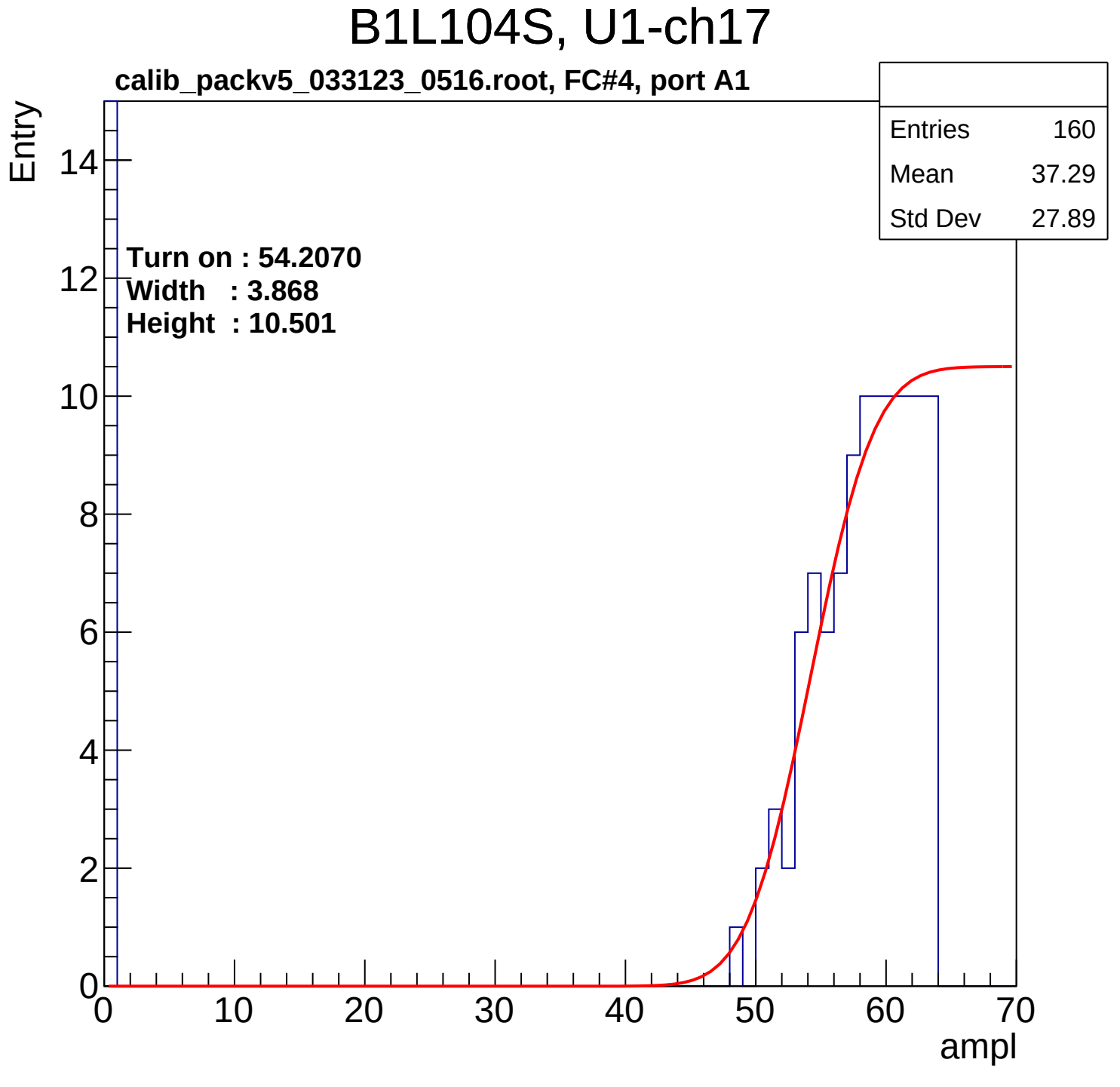

B1L104S, U1-ch12
calib_packv5_033123_0516.root, FC#4, port A1
Entries 183
Mean 33.91
Std Dev 28.42
Turn on : 53.4125
Width : 5.332
Height : 10.596
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

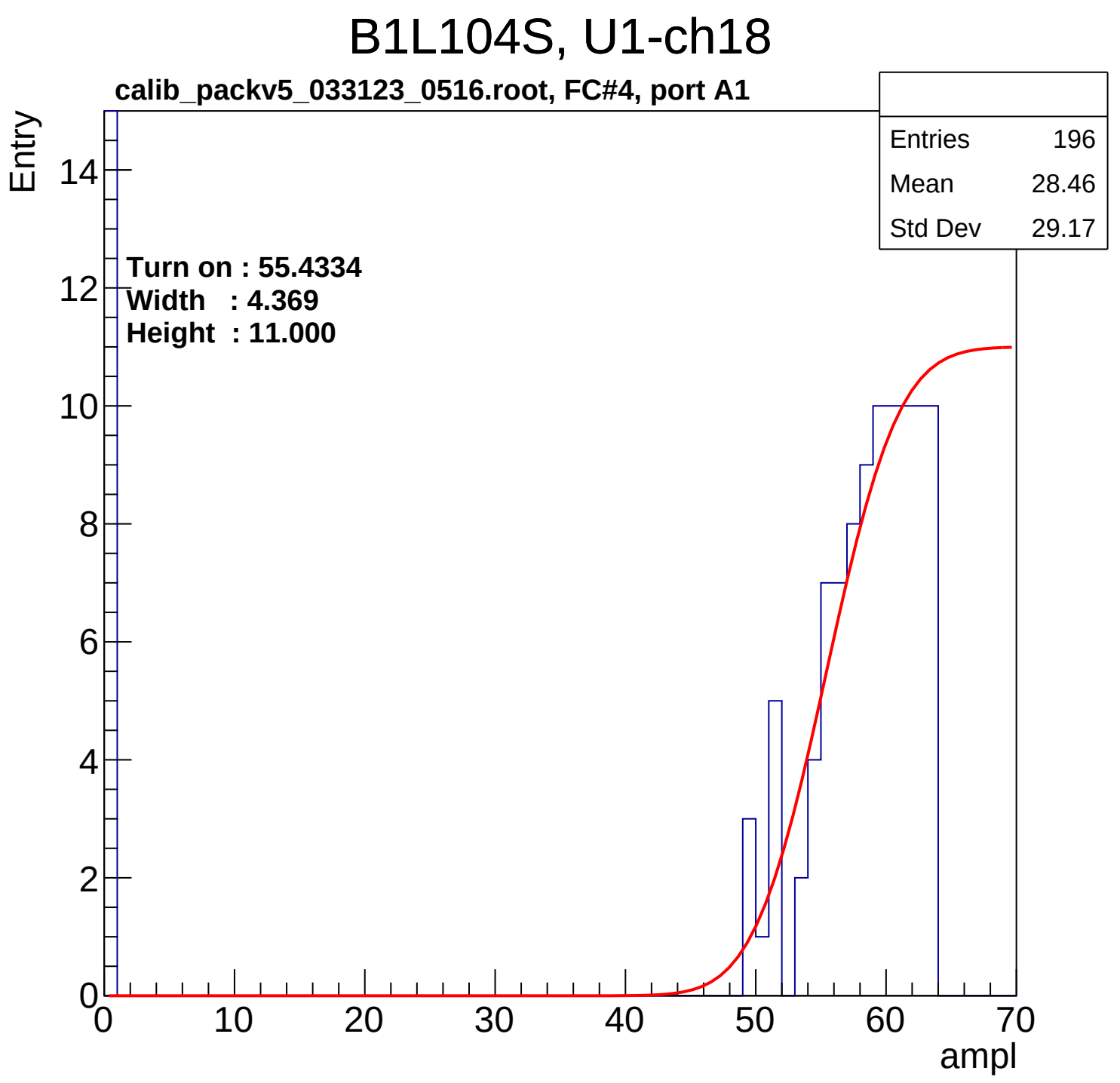

B1L104S, U1-ch13
calib_packv5_033123_0516.root, FC#4, port A1
Entries 187
Mean 35.25
Std Dev 28.06
Turn on : 52.4386
Width : 3.408
Height : 9.989
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

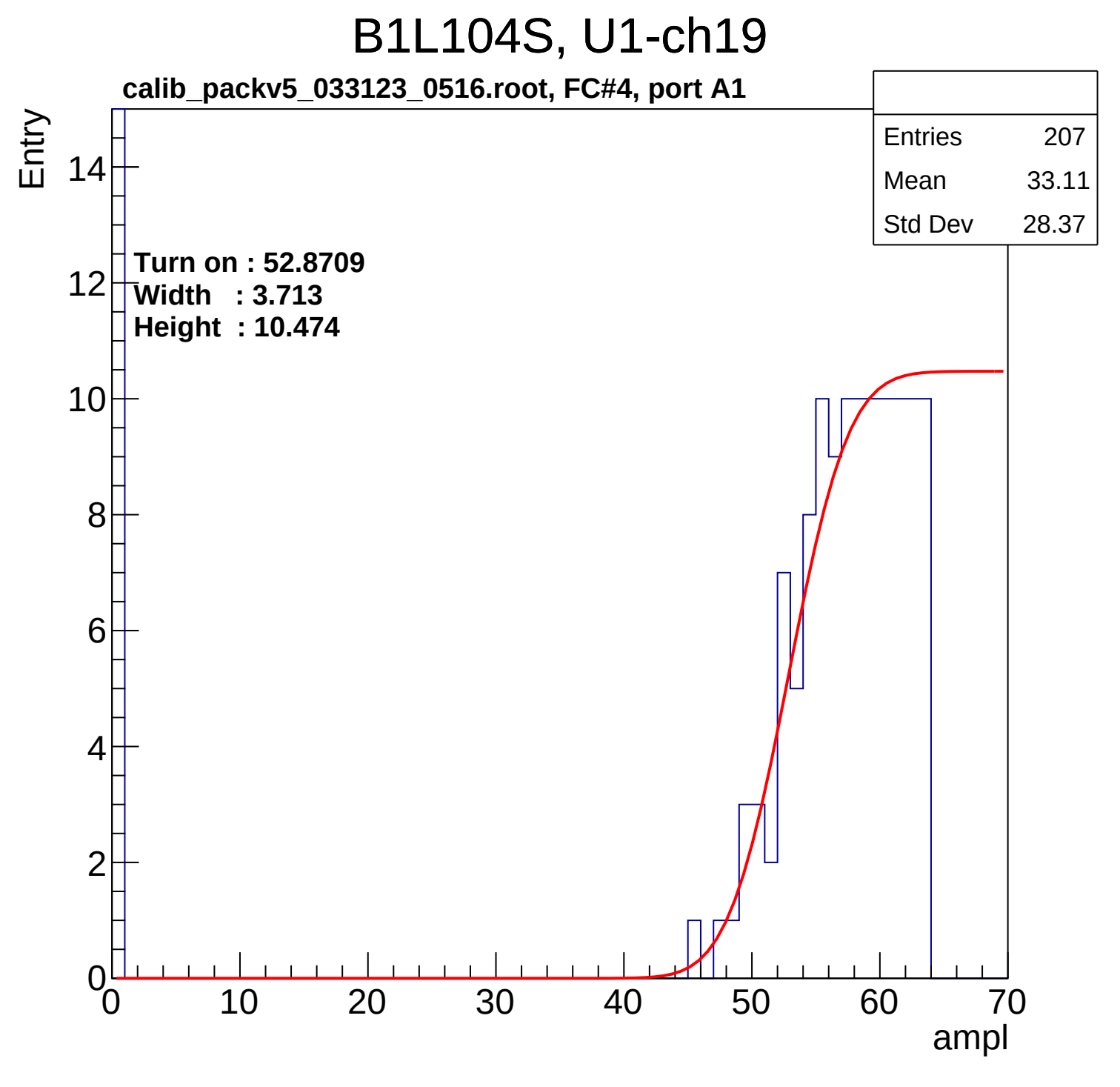

B1L104S, U1-ch14
calib_packv5_033123_0516.root, FC#4, port A1
Entries 179
Mean 32.72
Std Dev 28.87
Turn on : 53.7817
Width : 5.725
Height : 10.894
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

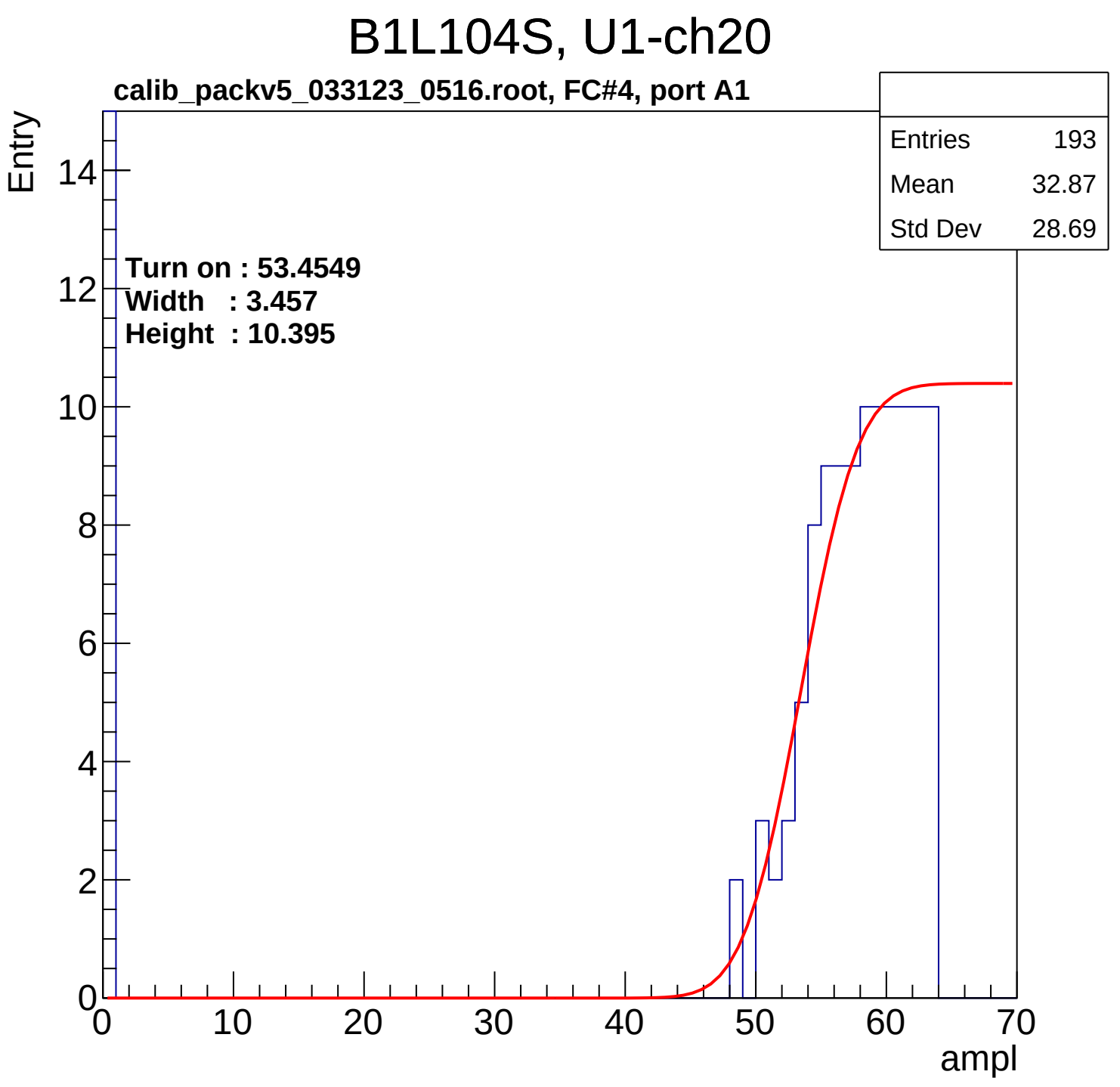

B1L104S, U1-ch15
calib_packv5_033123_0516.root, FC#4, port A1
Entries 196
Mean 33.09
Std Dev 28.52
Turn on : 54.1747
Width : 3.102
Height : 10.514
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

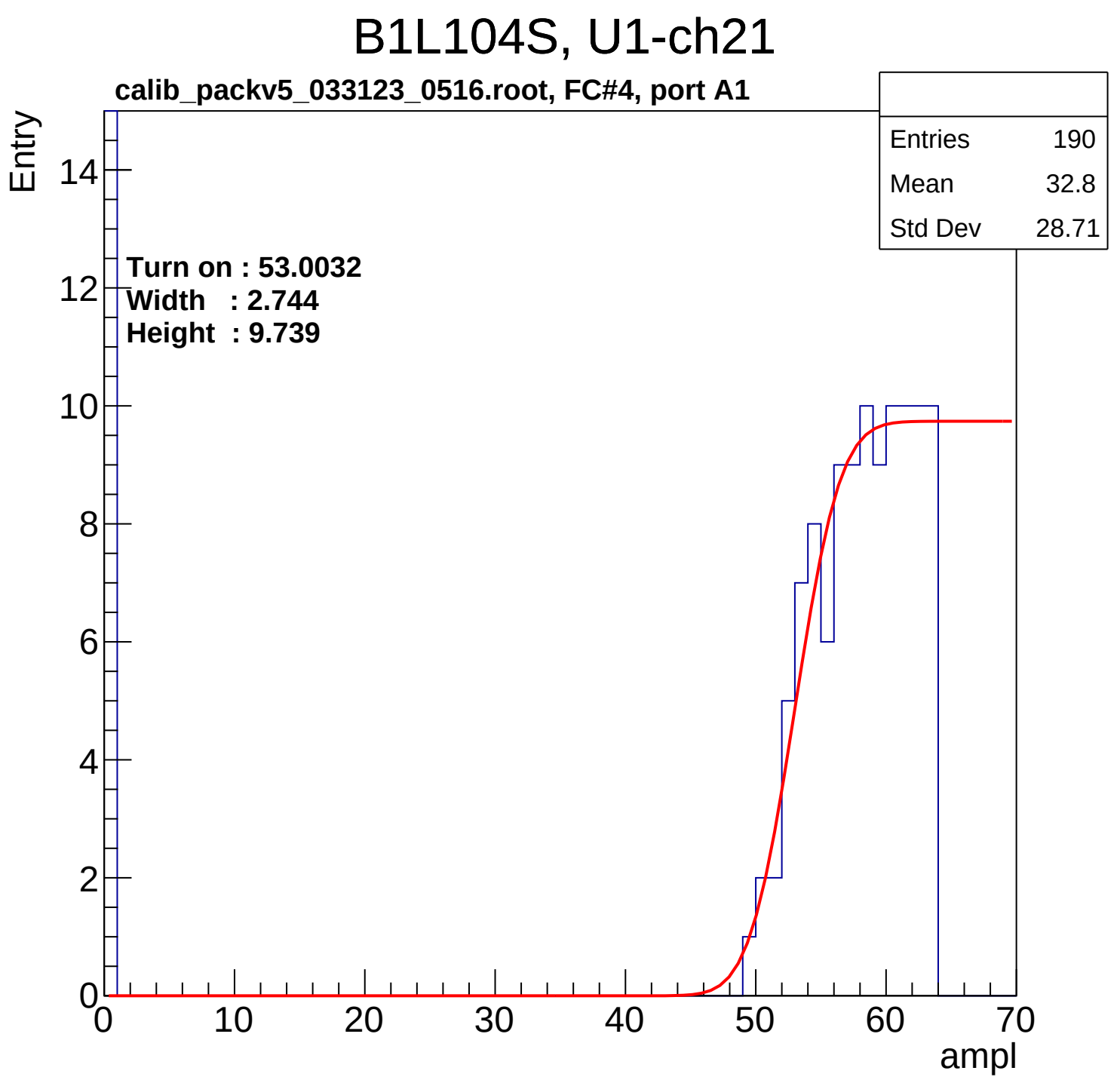

B1L104S, U1-ch16
calib_packv5_033123_0516.root, FC#4, port A1
Entries 185
Mean 35.79
Std Dev 27.82
Turn on : 53.6074
Width : 4.471
Height : 10.738
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

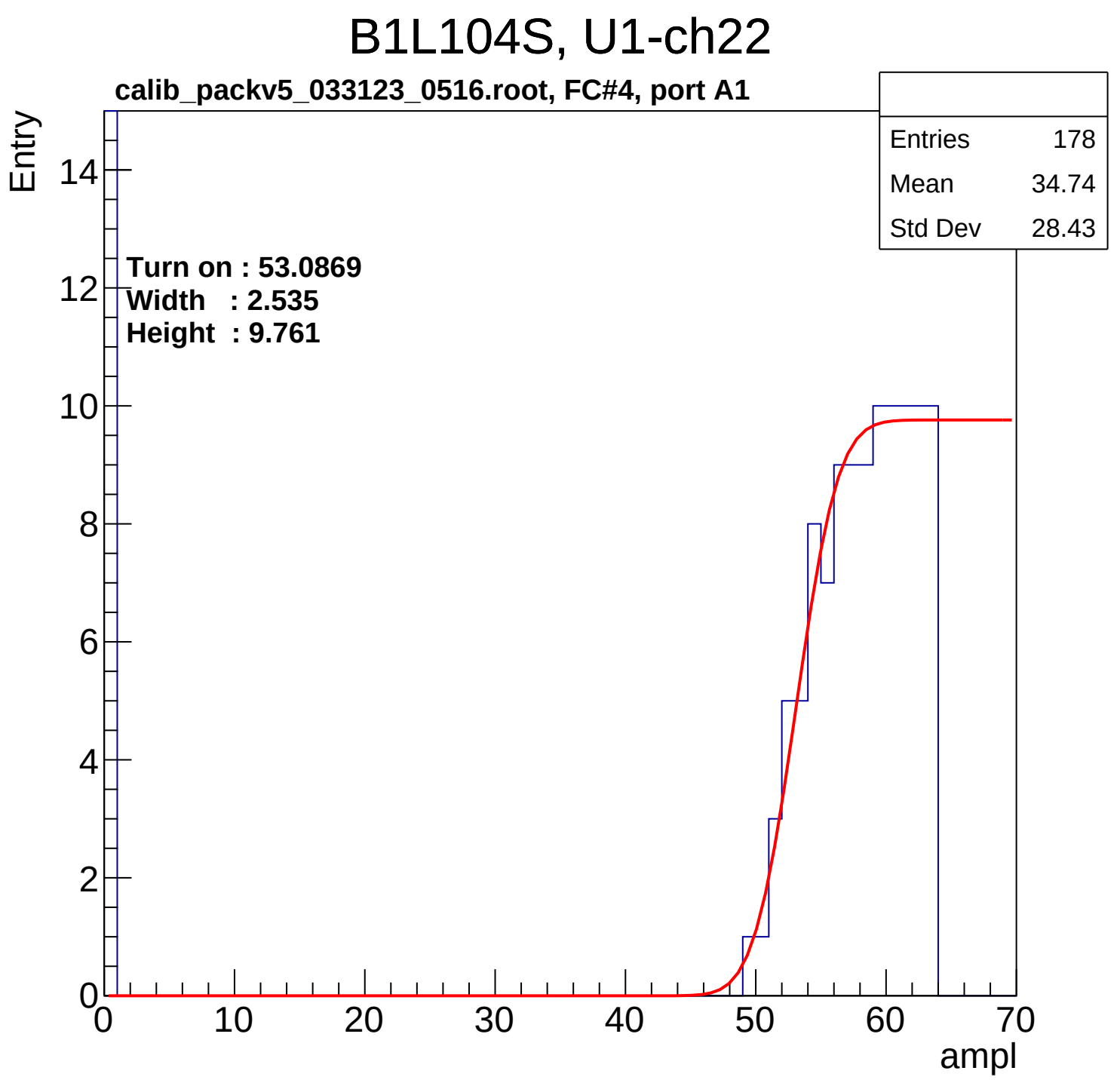

B1L104S, U1-ch17
calib_packv5_033123_0516.root, FC#4, port A1
Entries 160
Mean 37.29
Std Dev 27.89
Turn on : 54.2070
Width : 3.868
Height : 10.501
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

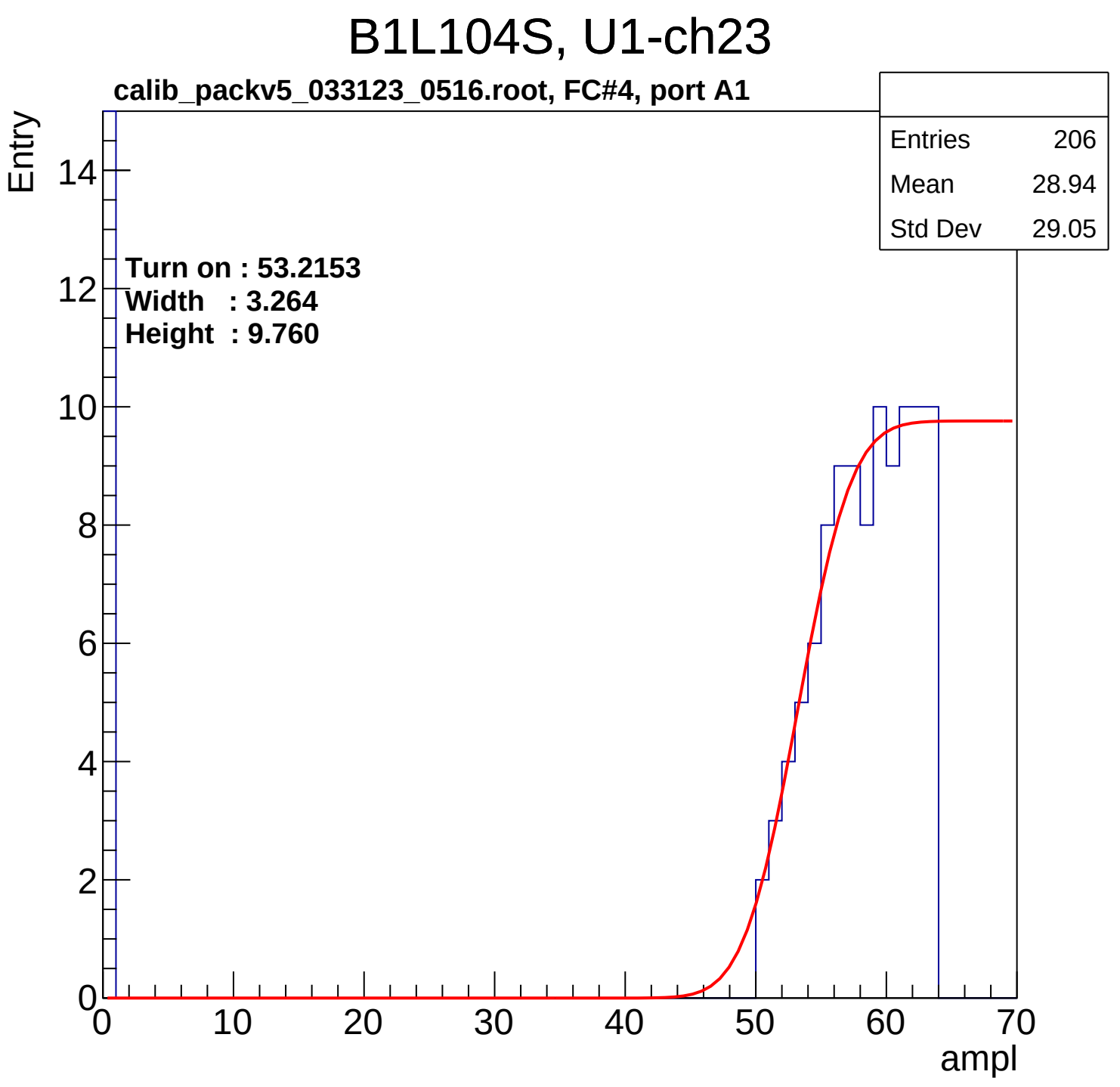

B1L104S, U1-ch18
calib_packv5_033123_0516.root, FC#4, port A1
Entries 196
Mean 28.46
Std Dev 29.17
Turn on : 55.4334
Width : 4.369
Height : 11.000
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

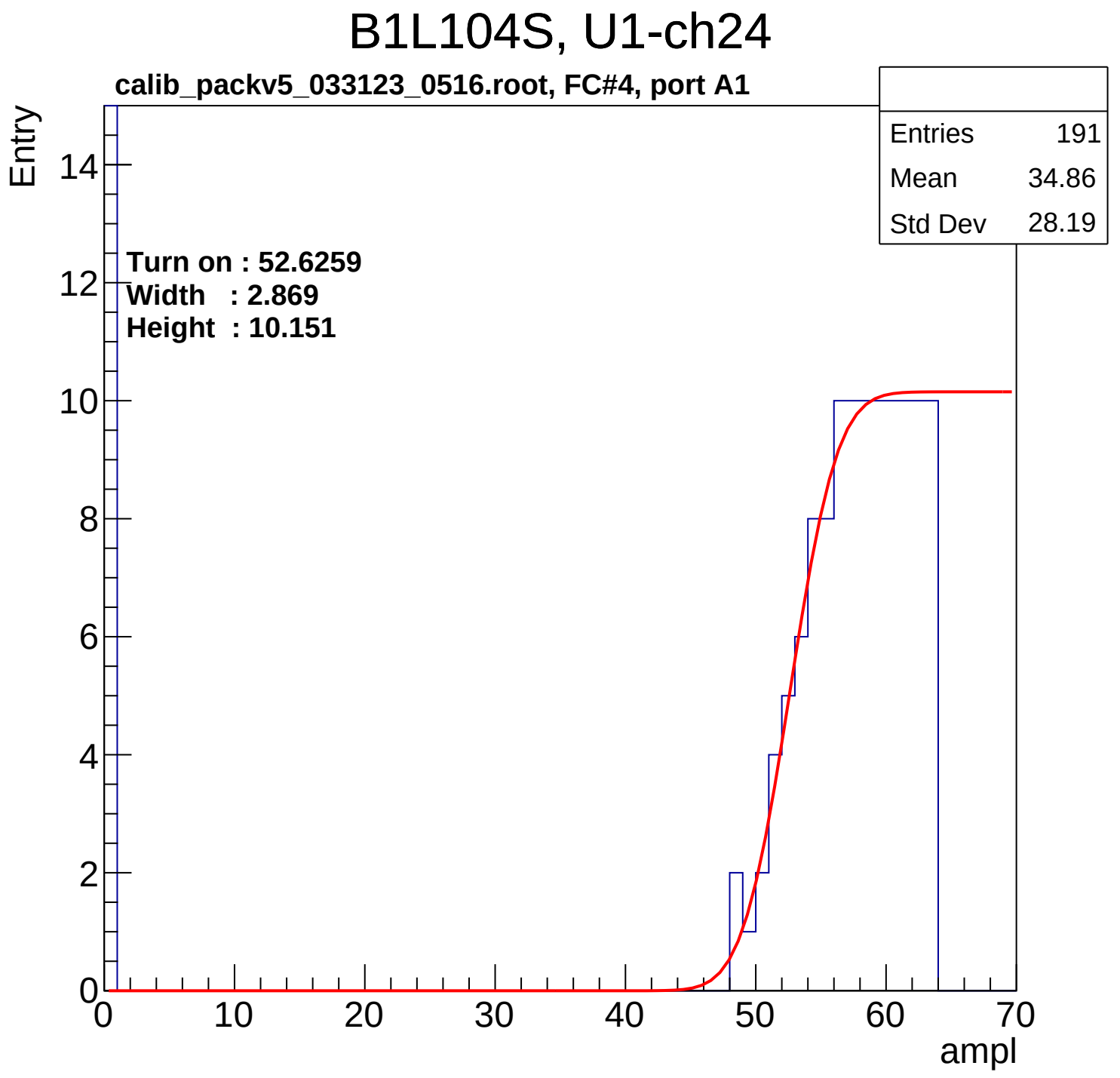

B1L104S, U1-ch19
calib_packv5_033123_0516.root, FC#4, port A1
Entries 207
Mean 33.11
Std Dev 28.37
Turn on : 52.8709
Width : 3.713
Height : 10.474
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

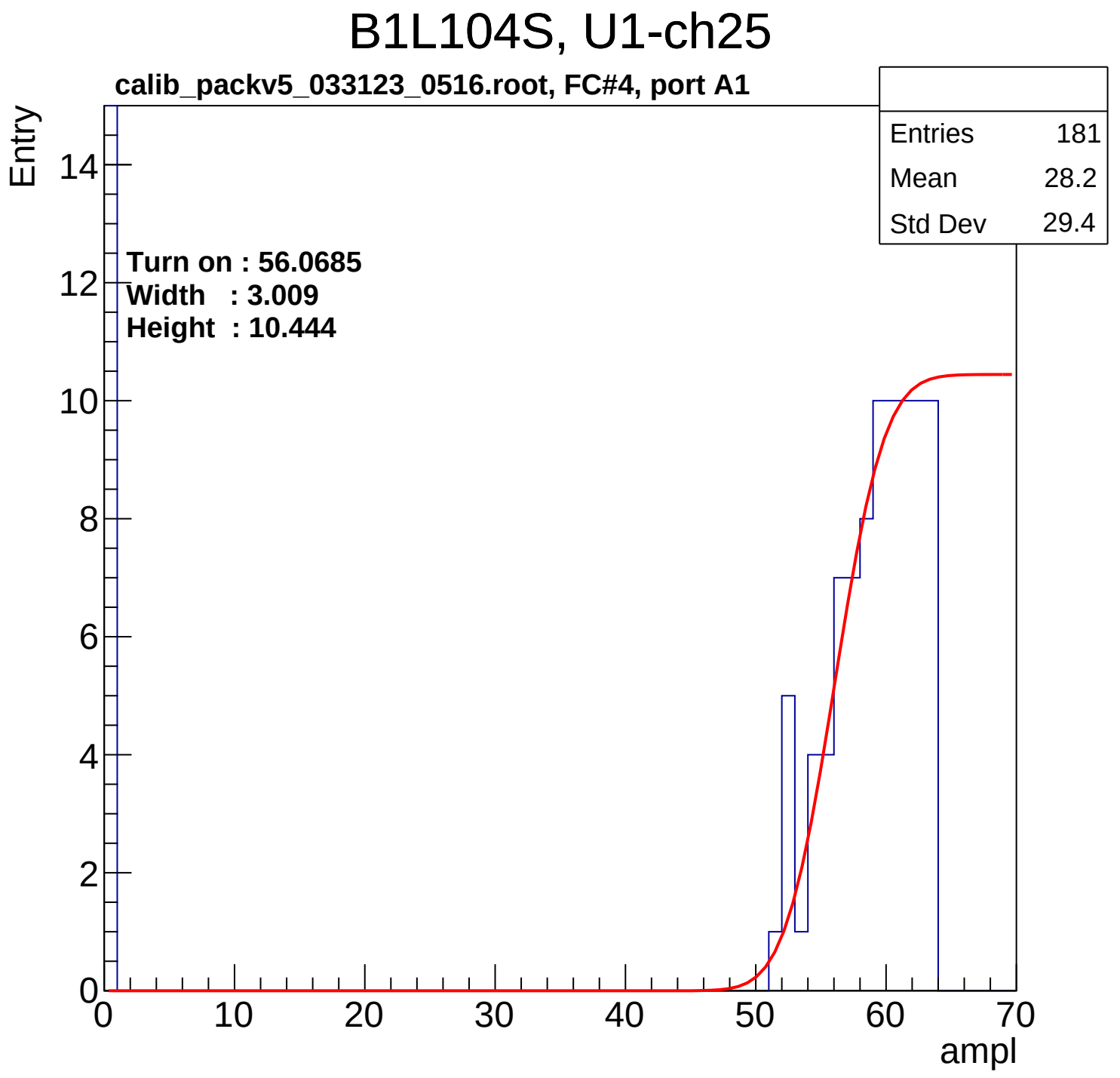

B1L104S, U1-ch20
calib_packv5_033123_0516.root, FC#4, port A1
Entries 193
Mean 32.87
Std Dev 28.69
Turn on : 53.4549
Width : 3.457
Height : 10.395
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

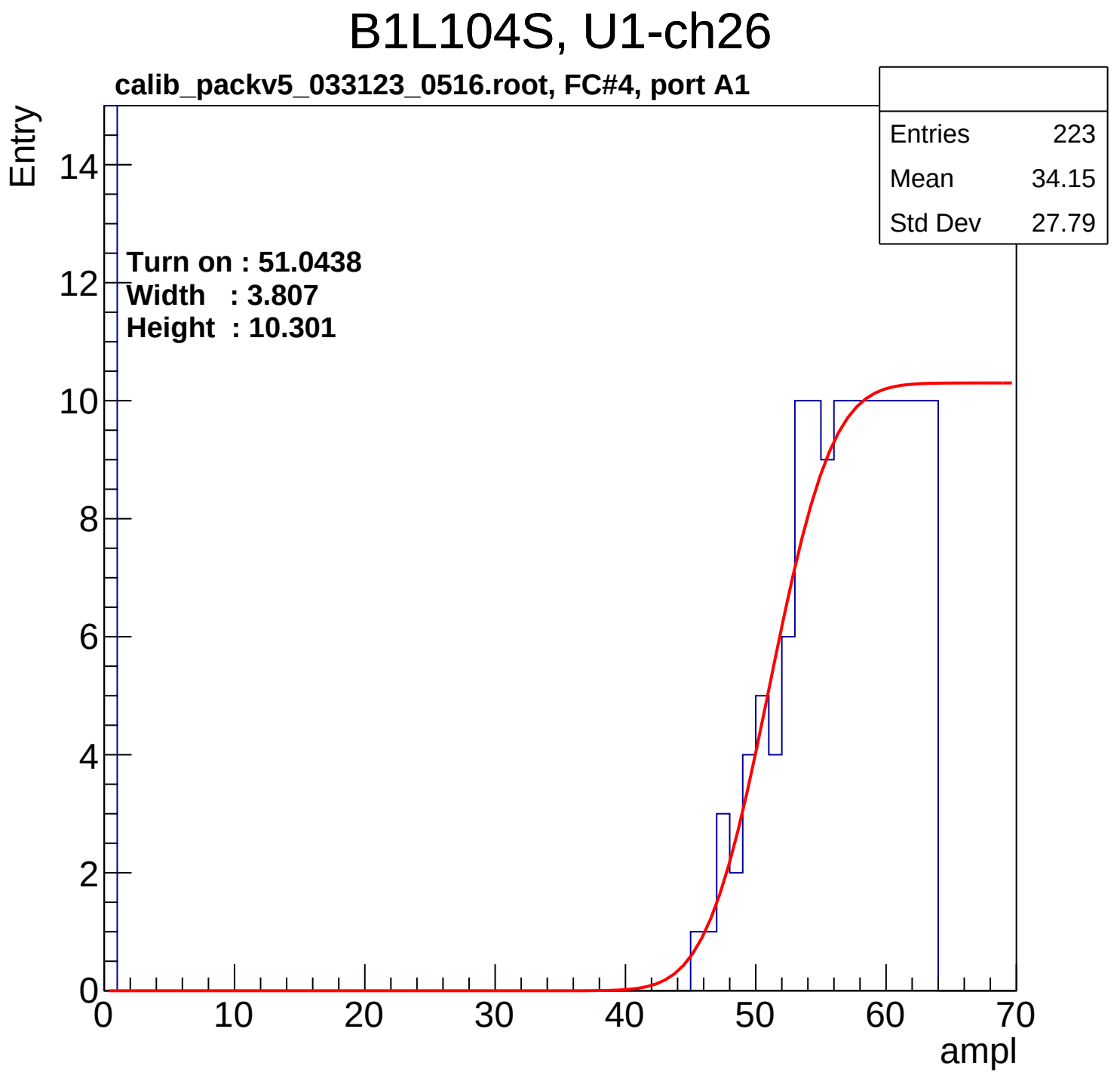

B1L104S, U1-ch21
calib_packv5_033123_0516.root, FC#4, port A1
Entries 190
Mean 32.8
Std Dev 28.71
Turn on : 53.0032
Width : 2.744
Height : 9.739
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

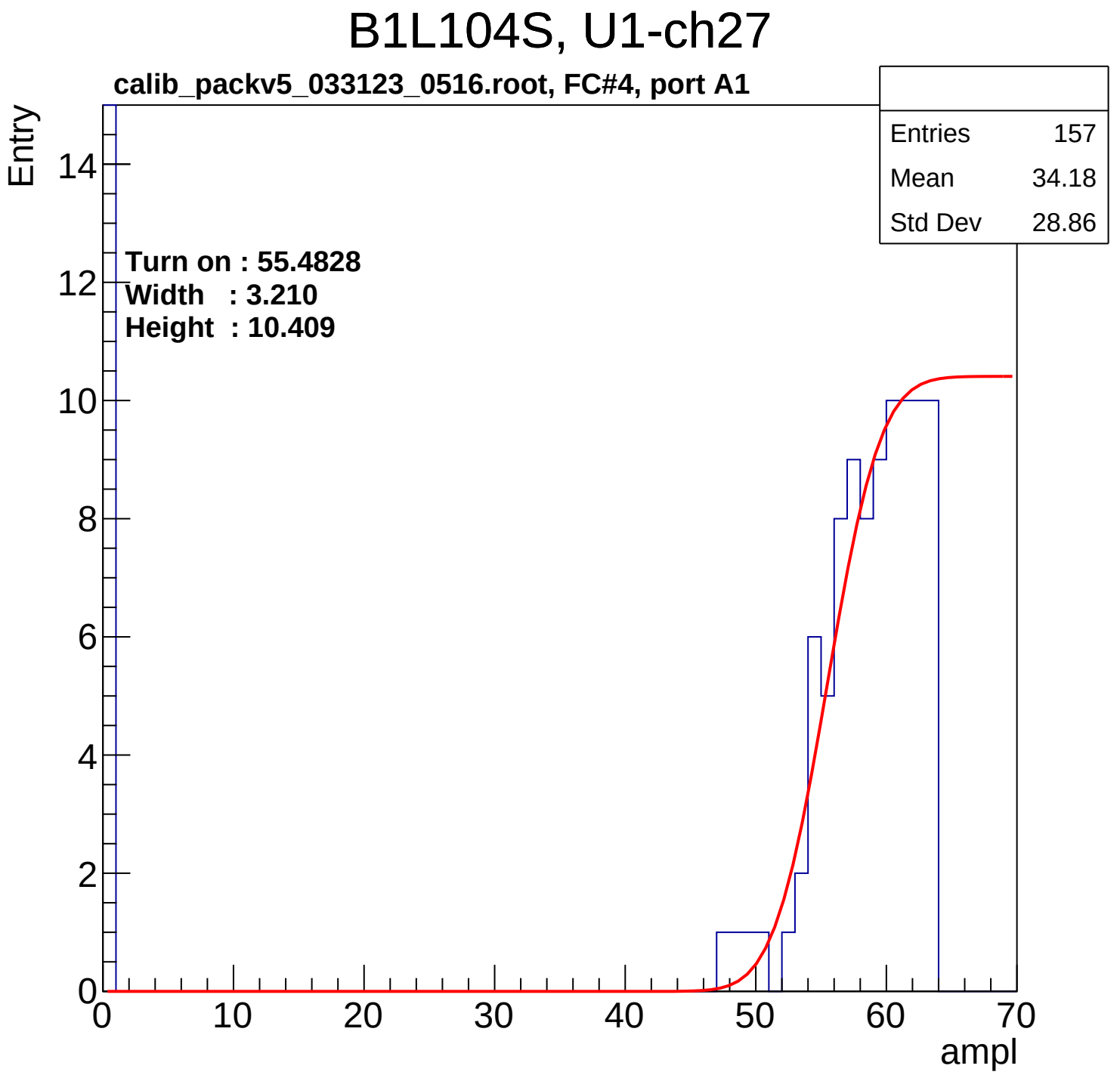

B1L104S, U1-ch22
calib_packv5_033123_0516.root, FC#4, port A1
Entries 178
Mean 34.74
Std Dev 28.43
Turn on : 53.0869
Width : 2.535
Height : 9.761
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

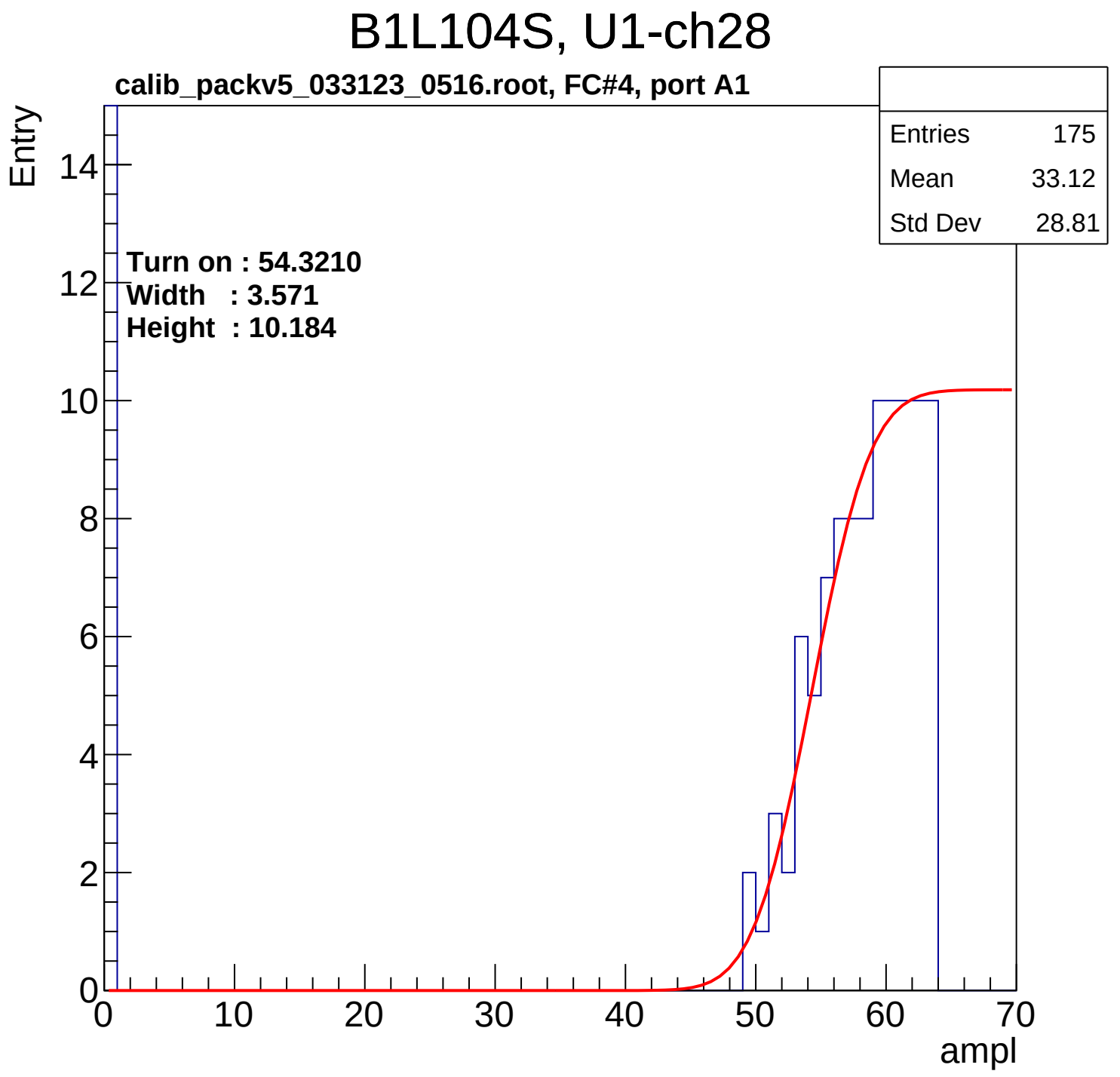

B1L104S, U1-ch23
calib_packv5_033123_0516.root, FC#4, port A1
Entries 206
Mean 28.94
Std Dev 29.05
Turn on : 53.2153
Width : 3.264
Height : 9.760
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

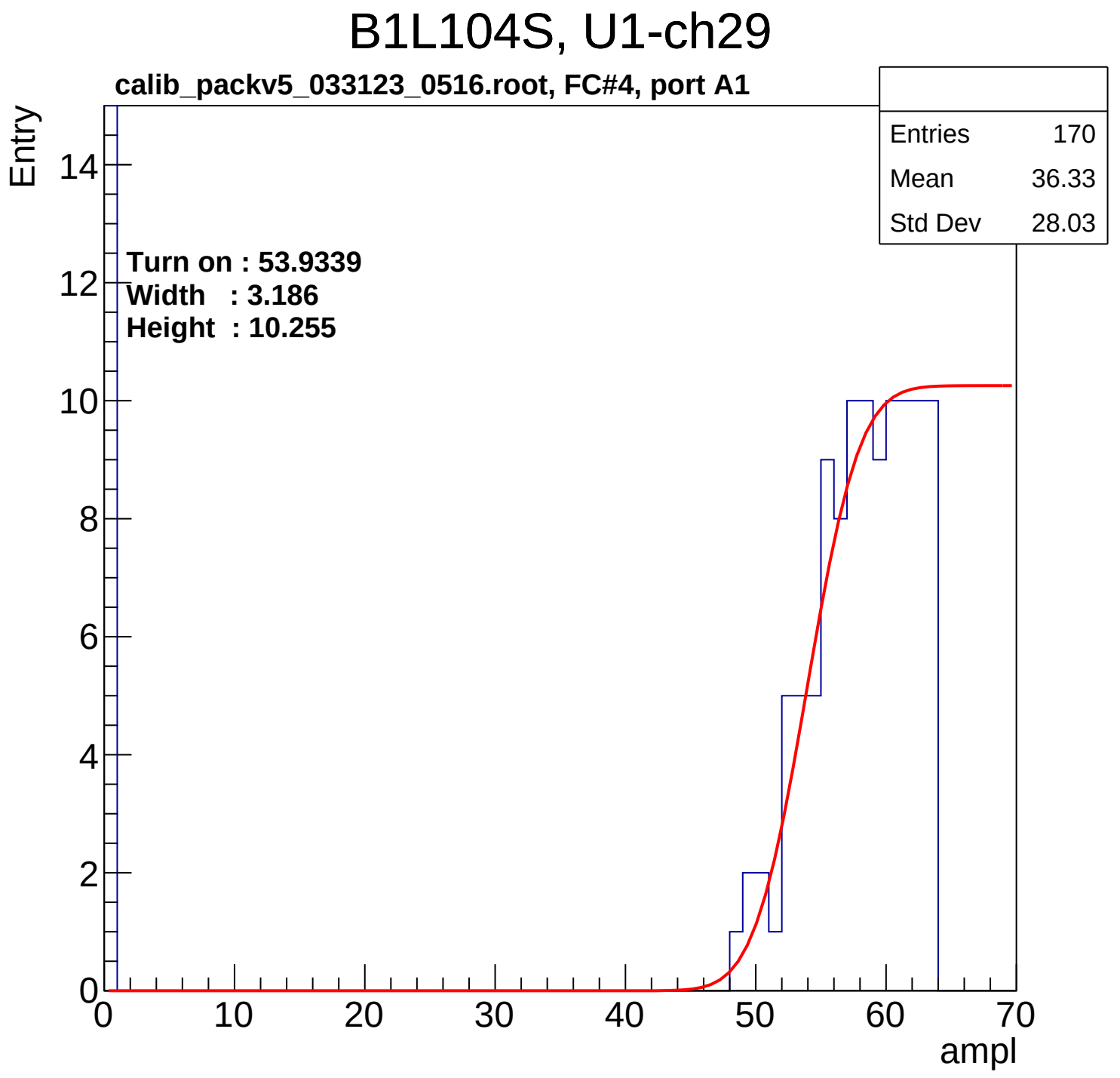

B1L104S, U1-ch24
calib_packv5_033123_0516.root, FC#4, port A1
Entries 191
Mean 34.86
Std Dev 28.19
Turn on : 52.6259
Width : 2.869
Height : 10.151
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

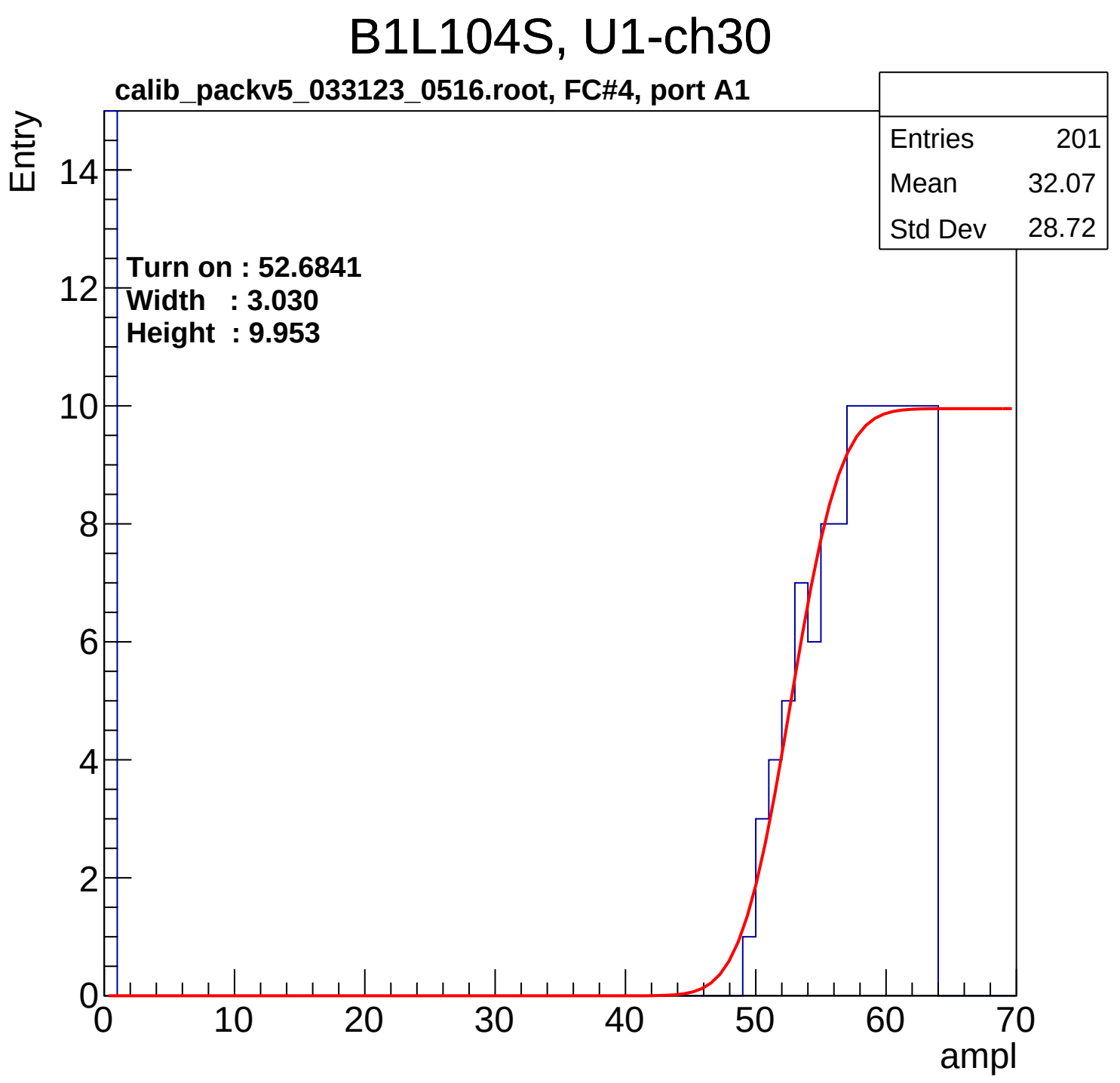

B1L104S, U1-ch25
calib_packv5_033123_0516.root, FC#4, port A1
Entries 181
Mean 28.2
Std Dev 29.4
Turn on : 56.0685
Width : 3.009
Height : 10.444
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

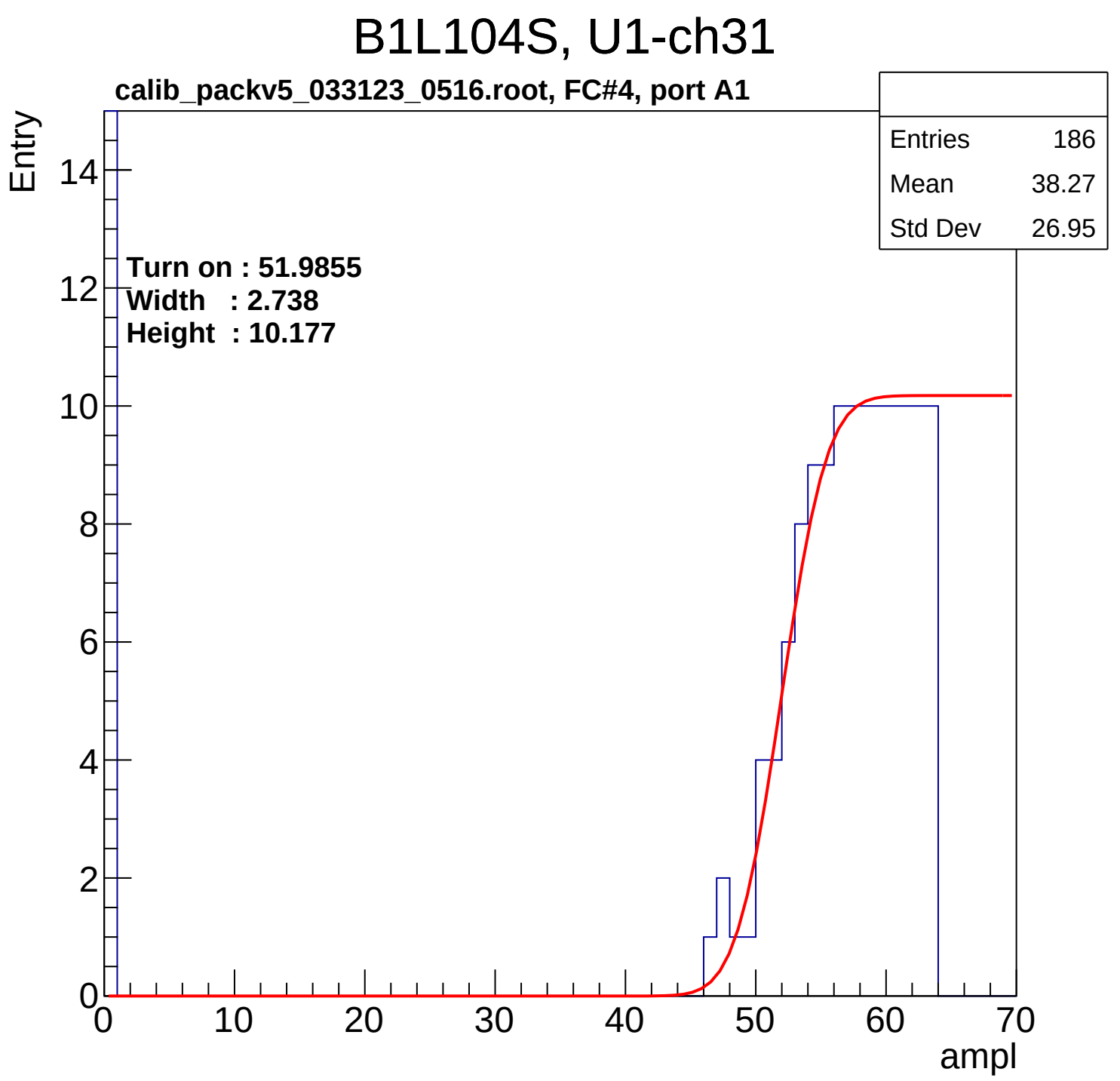

B1L104S, U1-ch26
calib_packv5_033123_0516.root, FC#4, port A1
Entries 223
Mean 34.15
Std Dev 27.79
Turn on : 51.0438
Width : 3.807
Height : 10.301
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

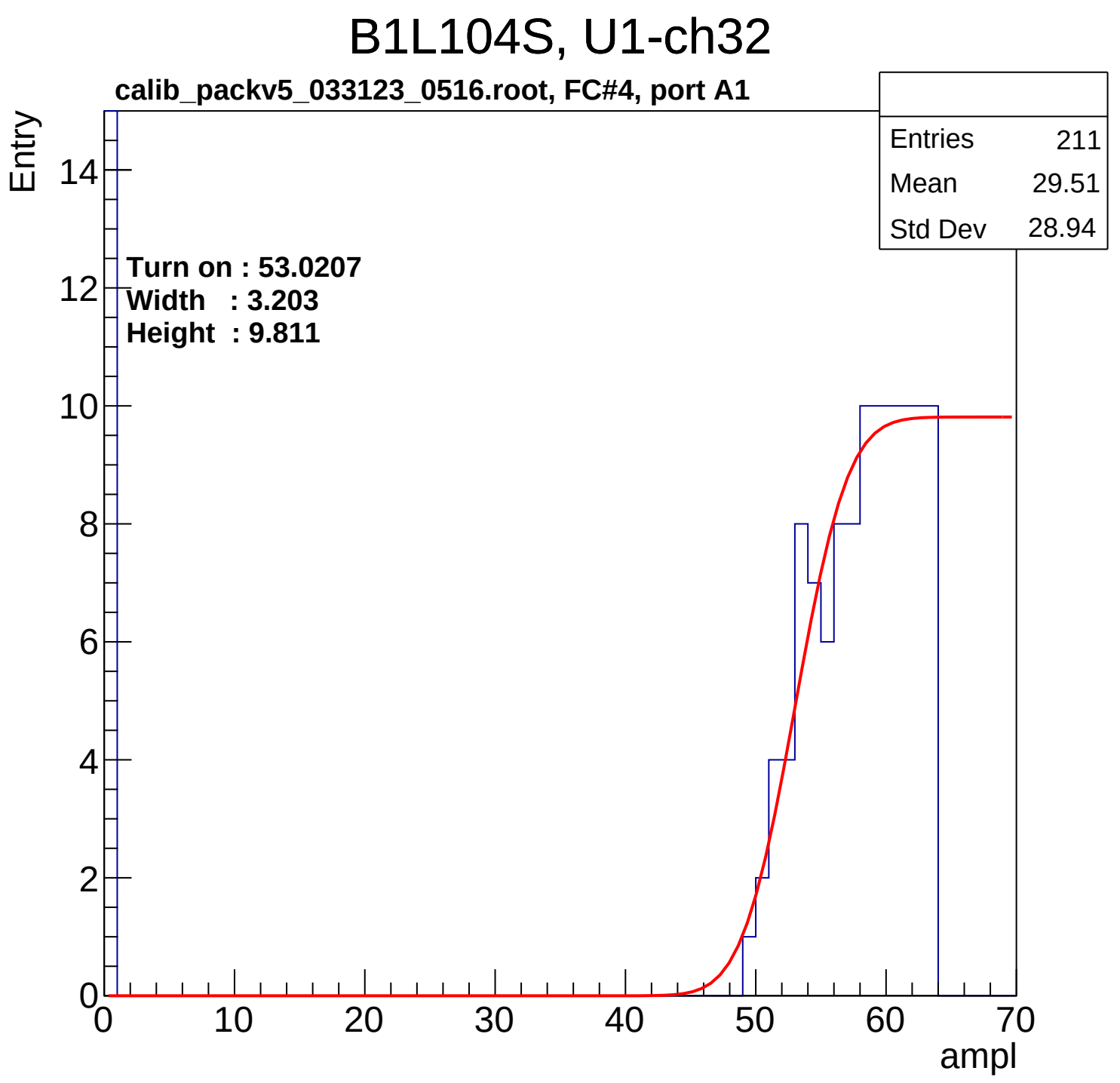

B1L104S, U1-ch27
calib_packv5_033123_0516.root, FC#4, port A1
Entries 157
Mean 34.18
Std Dev 28.86
Turn on : 55.4828
Width : 3.210
Height : 10.409
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

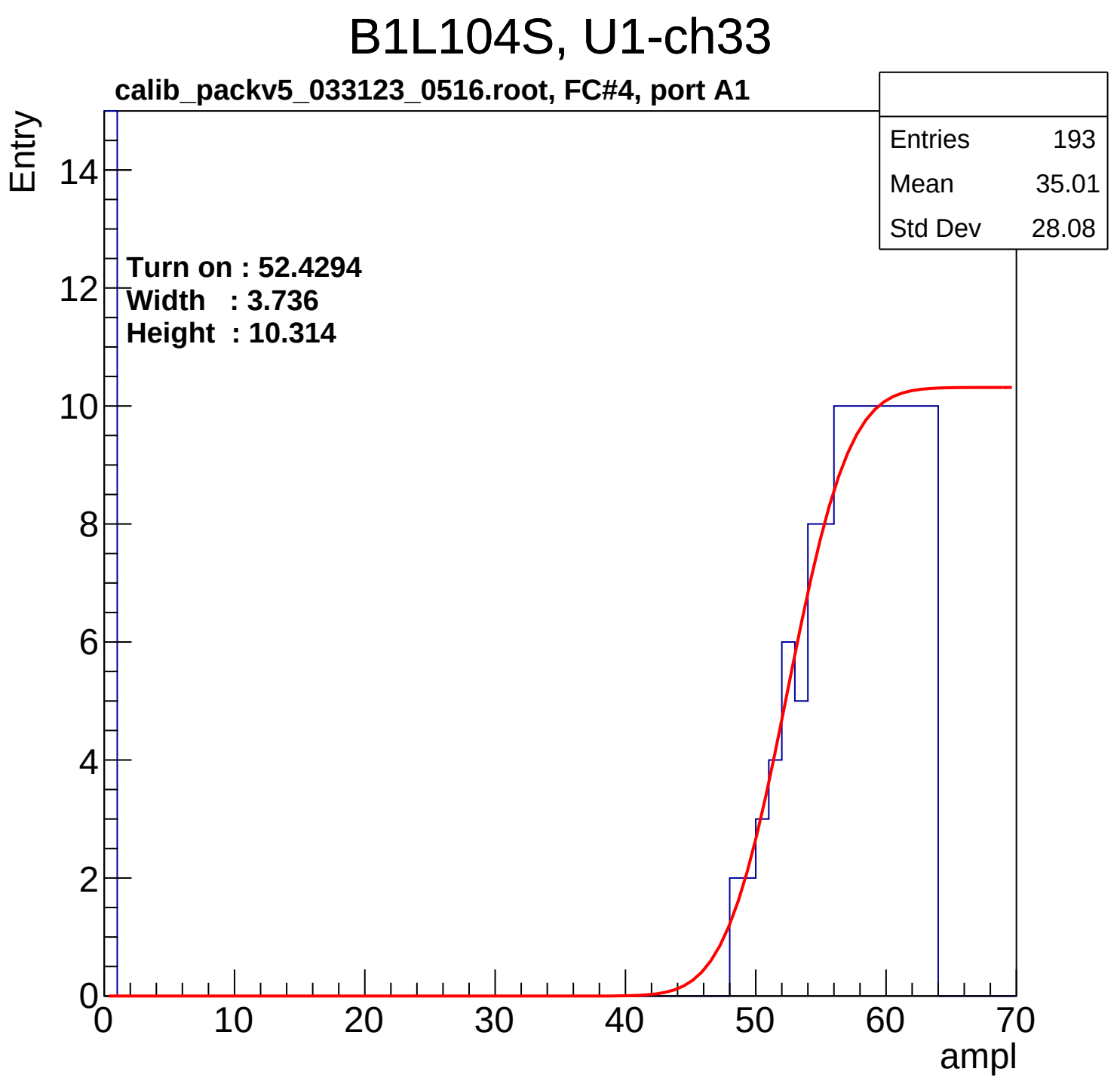

B1L104S, U1-ch28
calib_packv5_033123_0516.root, FC#4, port A1
Entries 175
Mean 33.12
Std Dev 28.81
Turn on : 54.3210
Width : 3.571
Height : 10.184
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

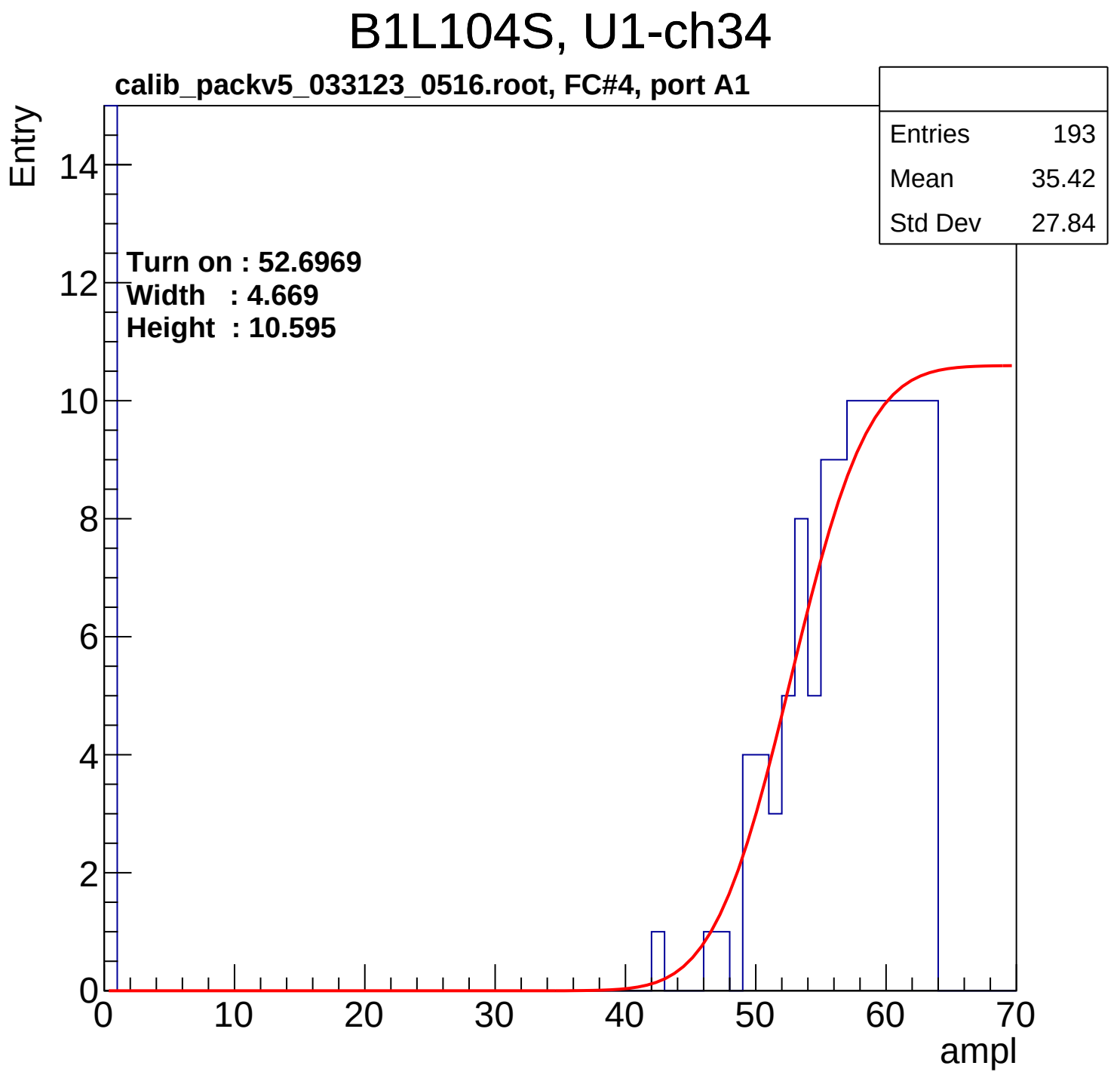

B1L104S, U1-ch29
calib_packv5_033123_0516.root, FC#4, port A1
Entries 170
Mean 36.33
Std Dev 28.03
Turn on : 53.9339
Width : 3.186
Height : 10.255
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

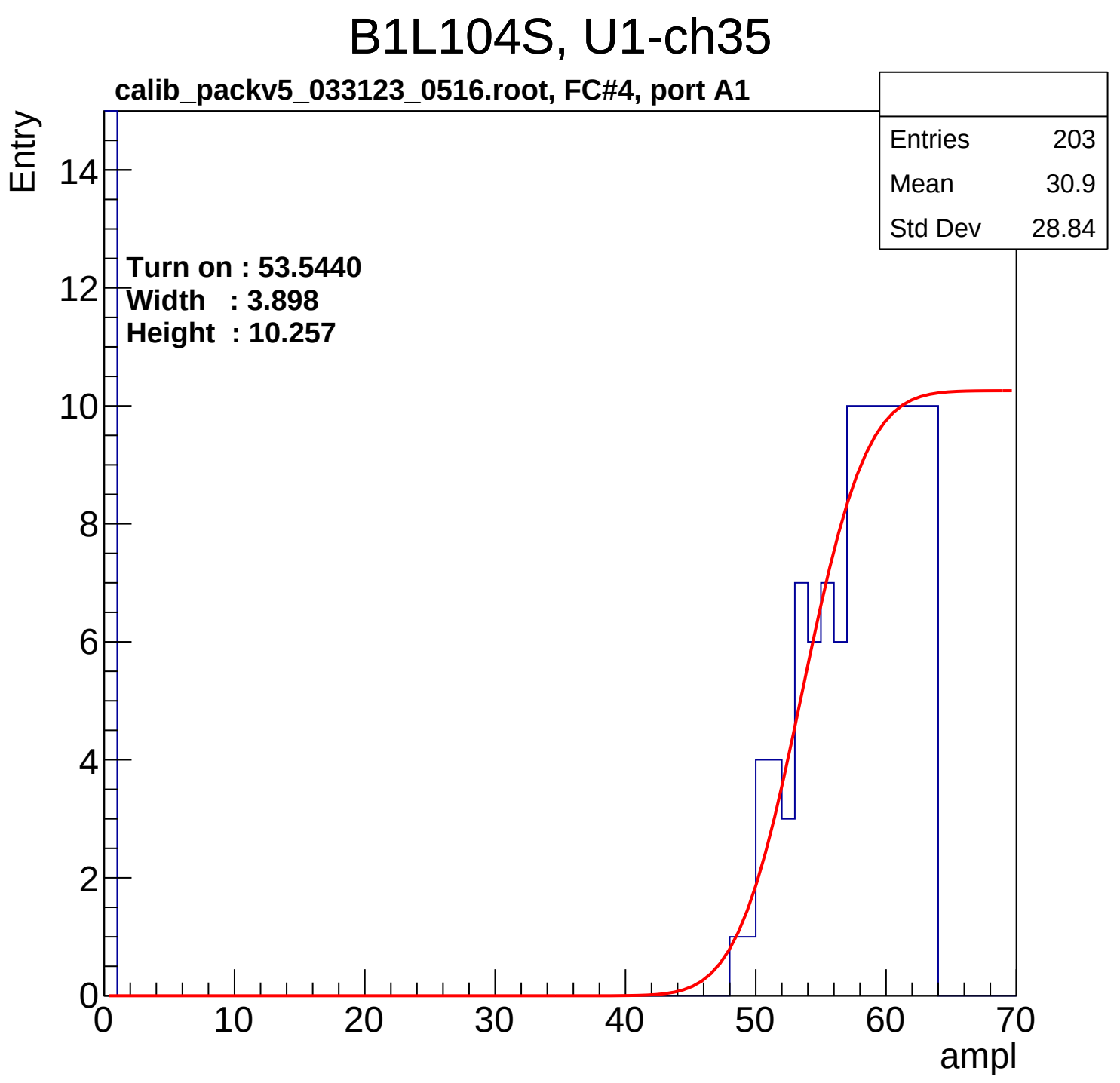

B1L104S, U1-ch30
calib_packv5_033123_0516.root, FC#4, port A1
Entries 201
Mean 32.07
Std Dev 28.72
Turn on : 52.6841
Width : 3.030
Height : 9.953
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

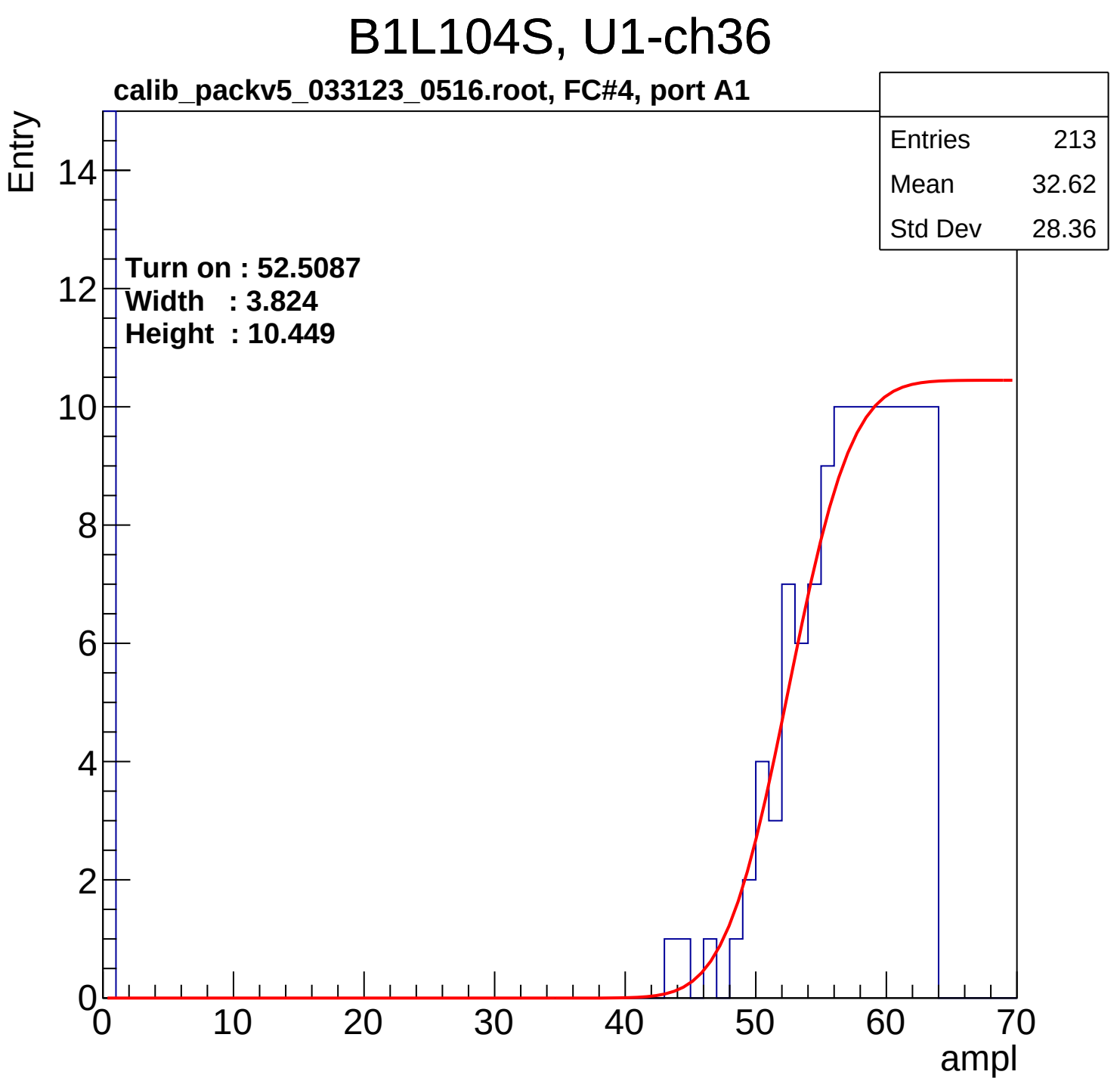

B1L104S, U1-ch31
calib_packv5_033123_0516.root, FC#4, port A1
Entries 186
Mean 38.27
Std Dev 26.95
Turn on : 51.9855
Width : 2.738
Height : 10.177
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

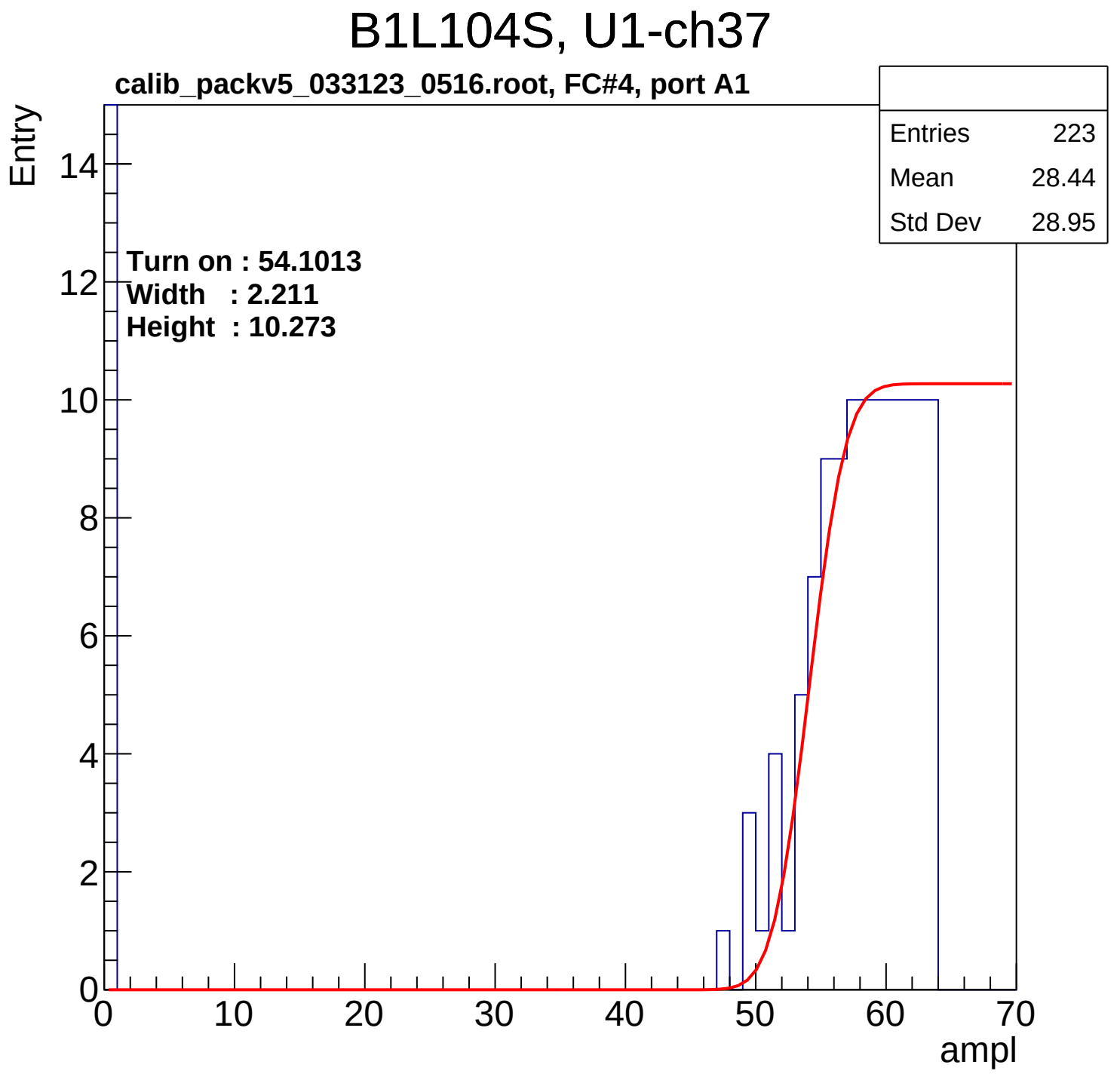

B1L104S, U1-ch32
calib_packv5_033123_0516.root, FC#4, port A1
Entries 211
Mean 29.51
Std Dev 28.94
Turn on : 53.0207
Width : 3.203
Height : 9.811
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

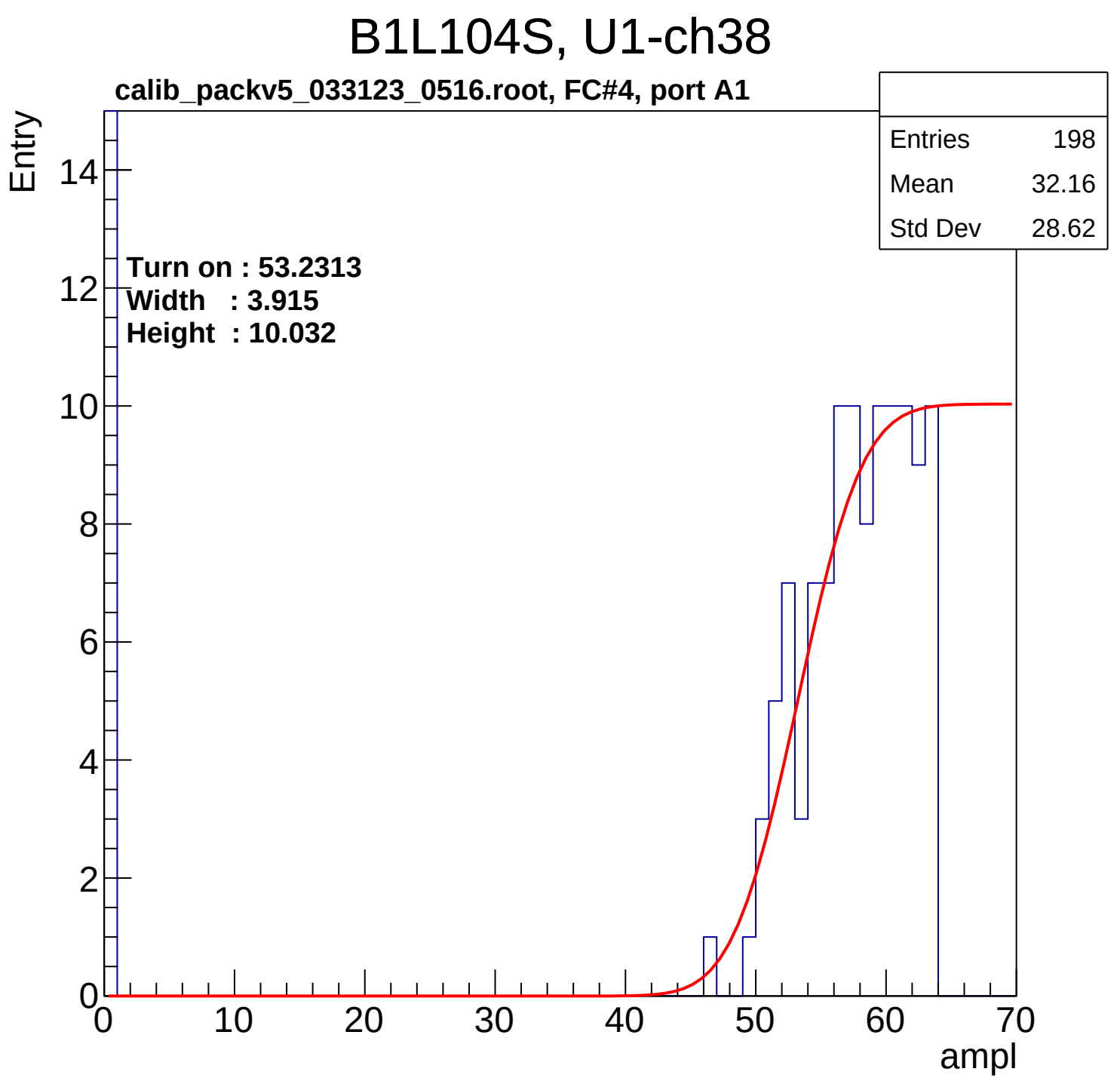

B1L104S, U1-ch33
calib_packv5_033123_0516.root, FC#4, port A1
Entries 193
Mean 35.01
Std Dev 28.08
Turn on : 52.4294
Width : 3.736
Height : 10.314
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

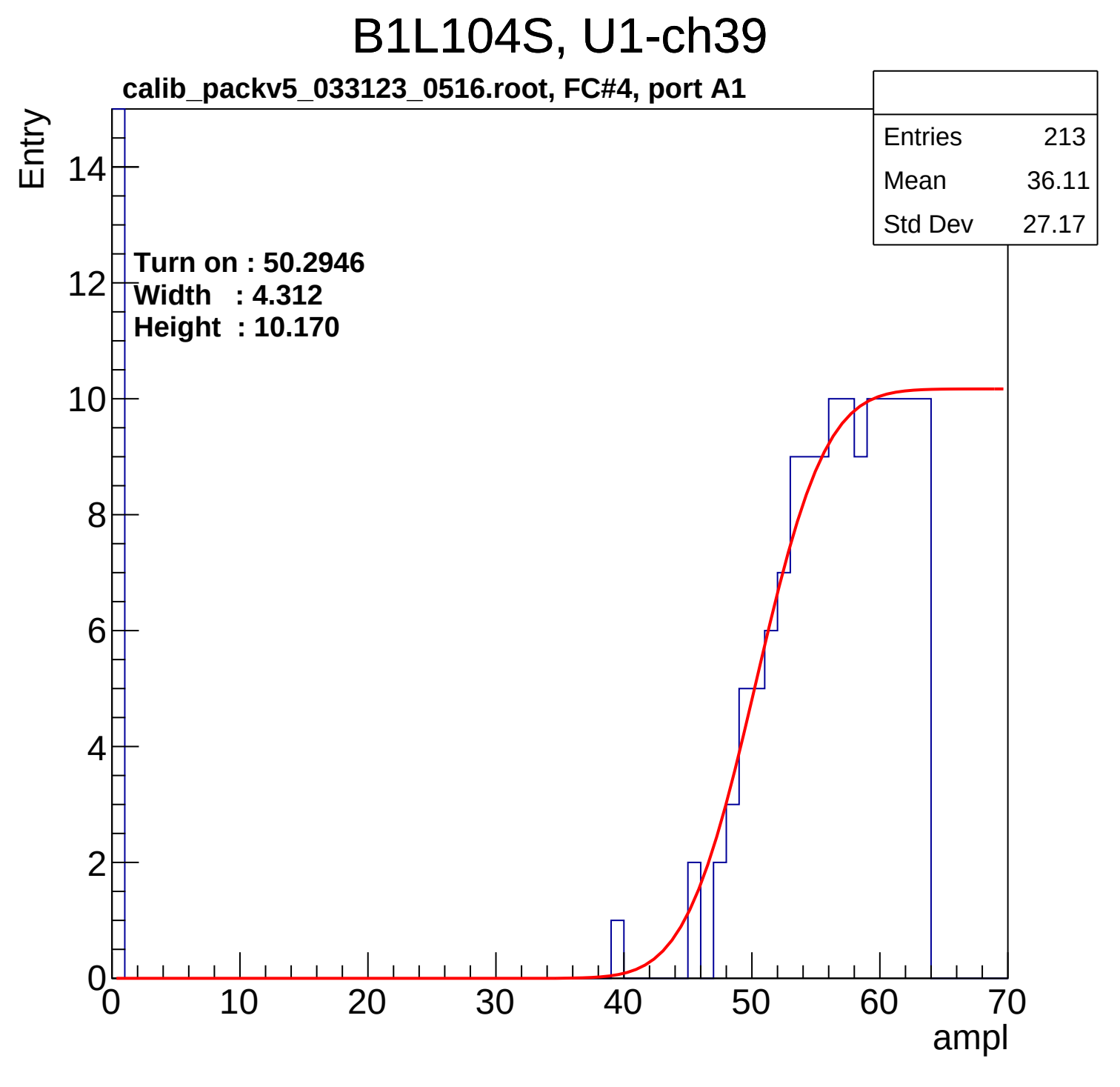

B1L104S, U1-ch34
calib_packv5_033123_0516.root, FC#4, port A1
Entries 193
Mean 35.42
Std Dev 27.84
Turn on : 52.6969
Width : 4.669
Height : 10.595
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

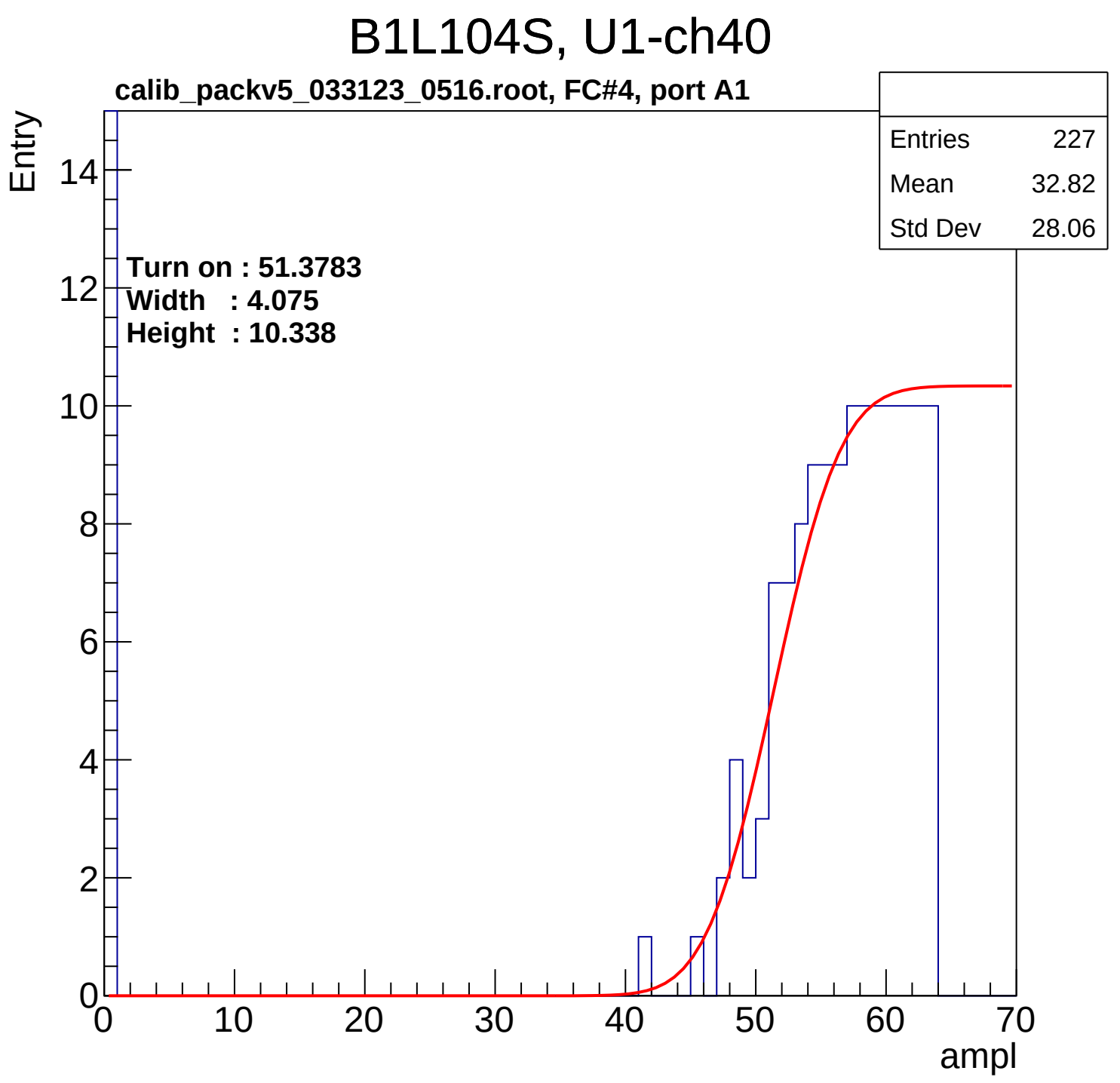

B1L104S, U1-ch35
calib_packv5_033123_0516.root, FC#4, port A1
Entries 203
Mean 30.9
Std Dev 28.84
Turn on : 53.5440
Width : 3.898
Height : 10.257
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

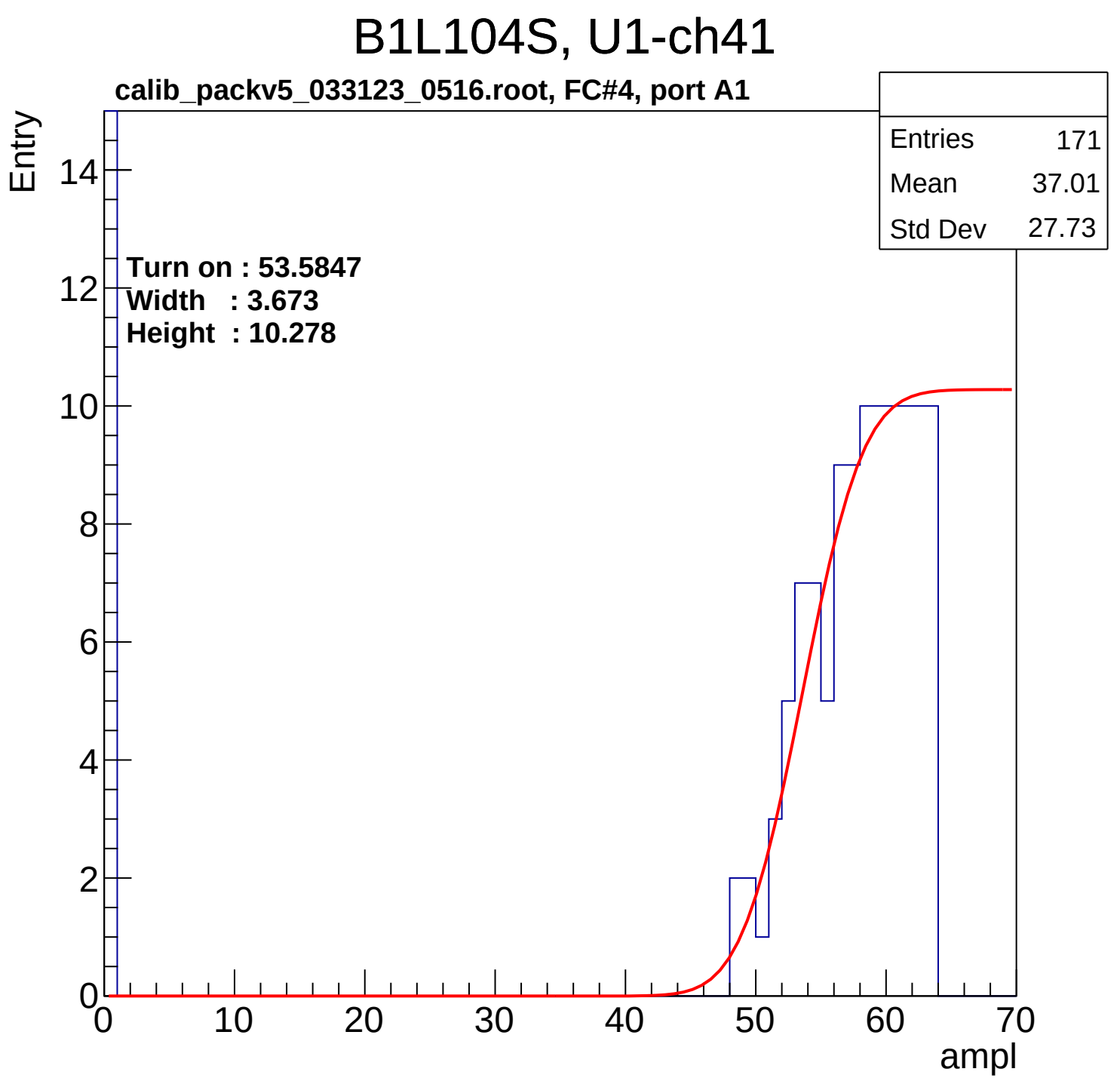

B1L104S, U1-ch36
calib_packv5_033123_0516.root, FC#4, port A1
Entries 213
Mean 32.62
Std Dev 28.36
Turn on : 52.5087
Width : 3.824
Height : 10.449
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

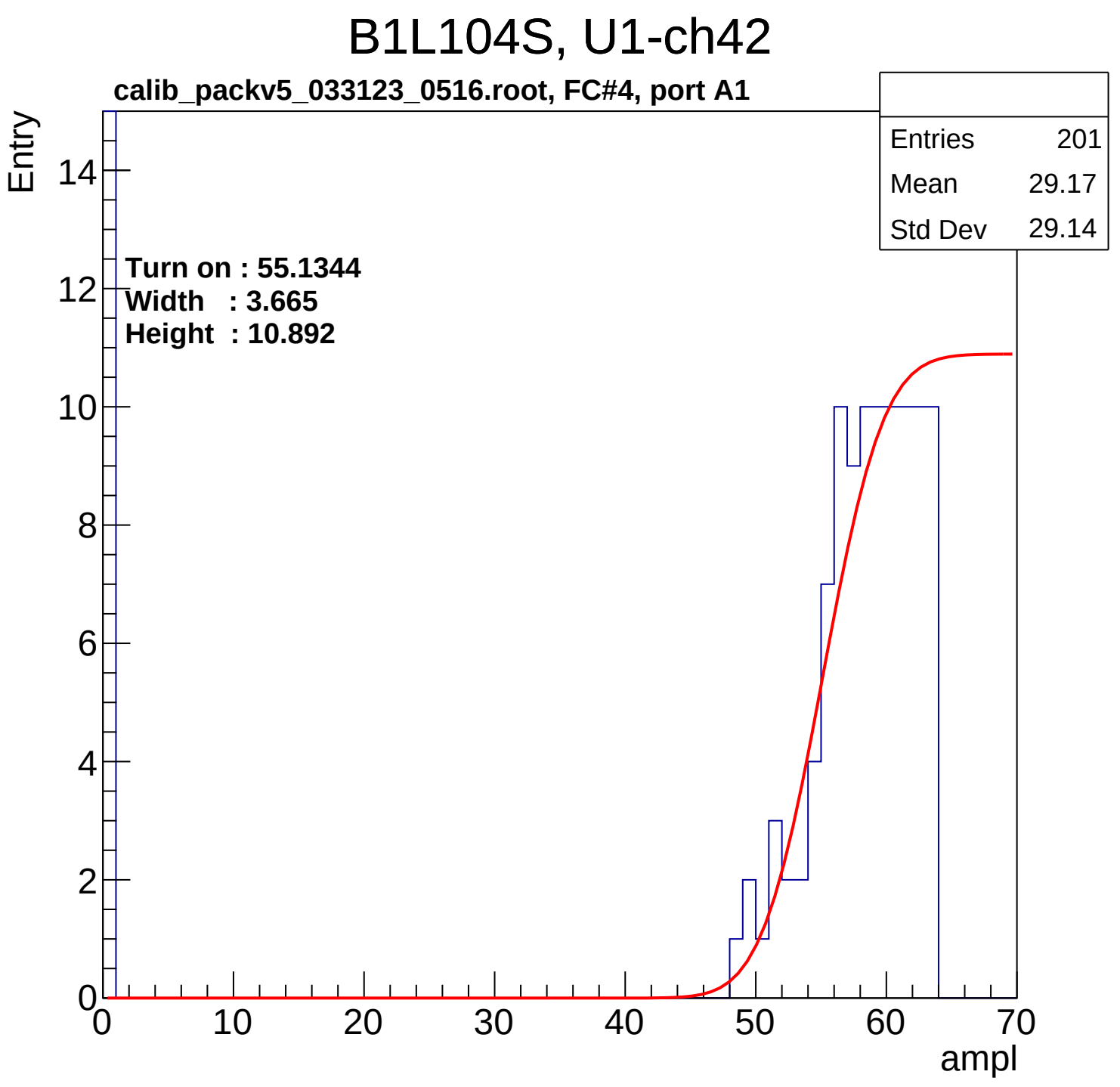

B1L104S, U1-ch37
calib_packv5_033123_0516.root, FC#4, port A1
Entries 223
Mean 28.44
Std Dev 28.95
Turn on : 54.1013
Width : 2.211
Height : 10.273
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

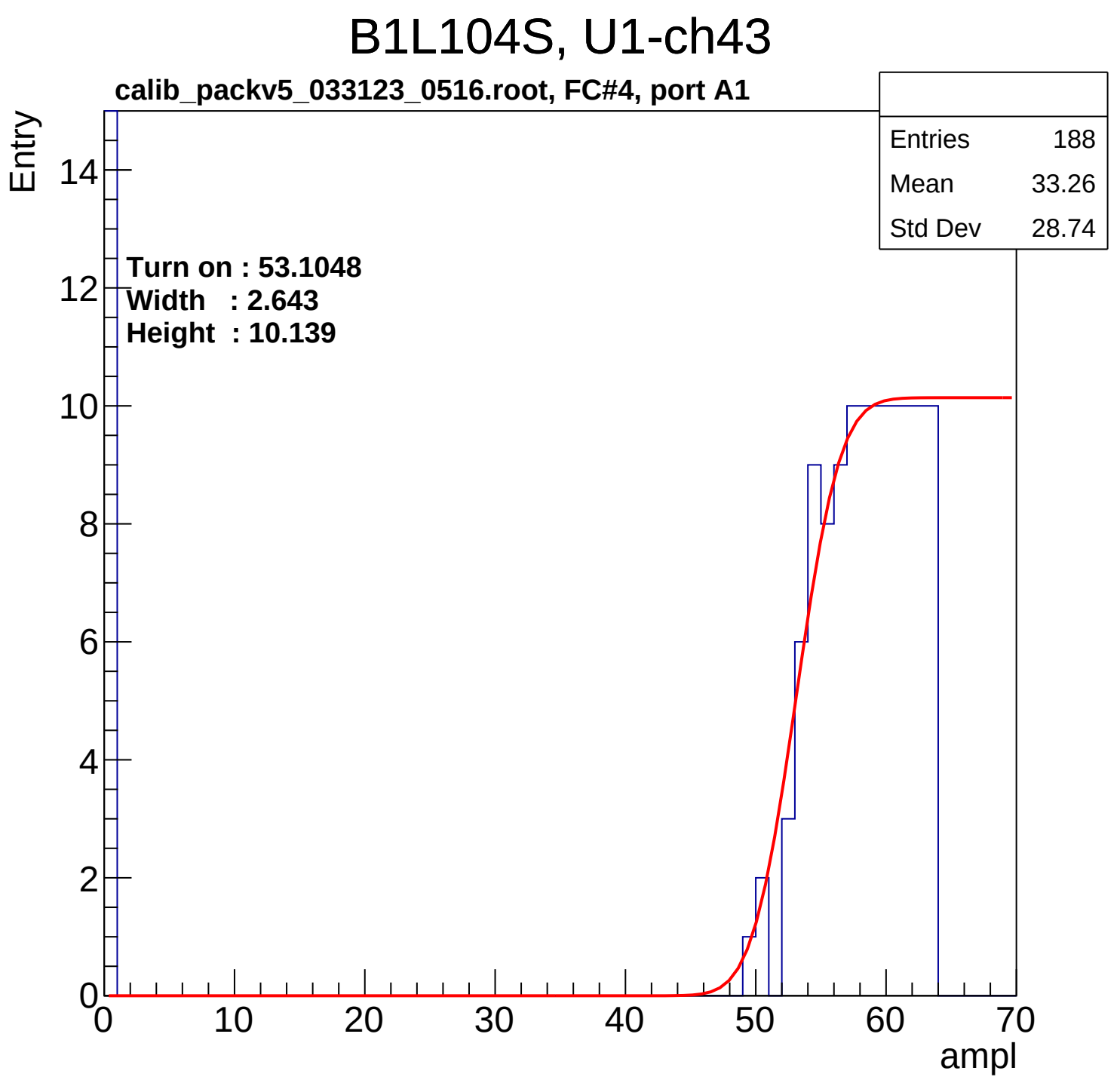

B1L104S, U1-ch38
calib_packv5_033123_0516.root, FC#4, port A1
Entries 198
Mean 32.16
Std Dev 28.62
Turn on : 53.2313
Width : 3.915
Height : 10.032
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

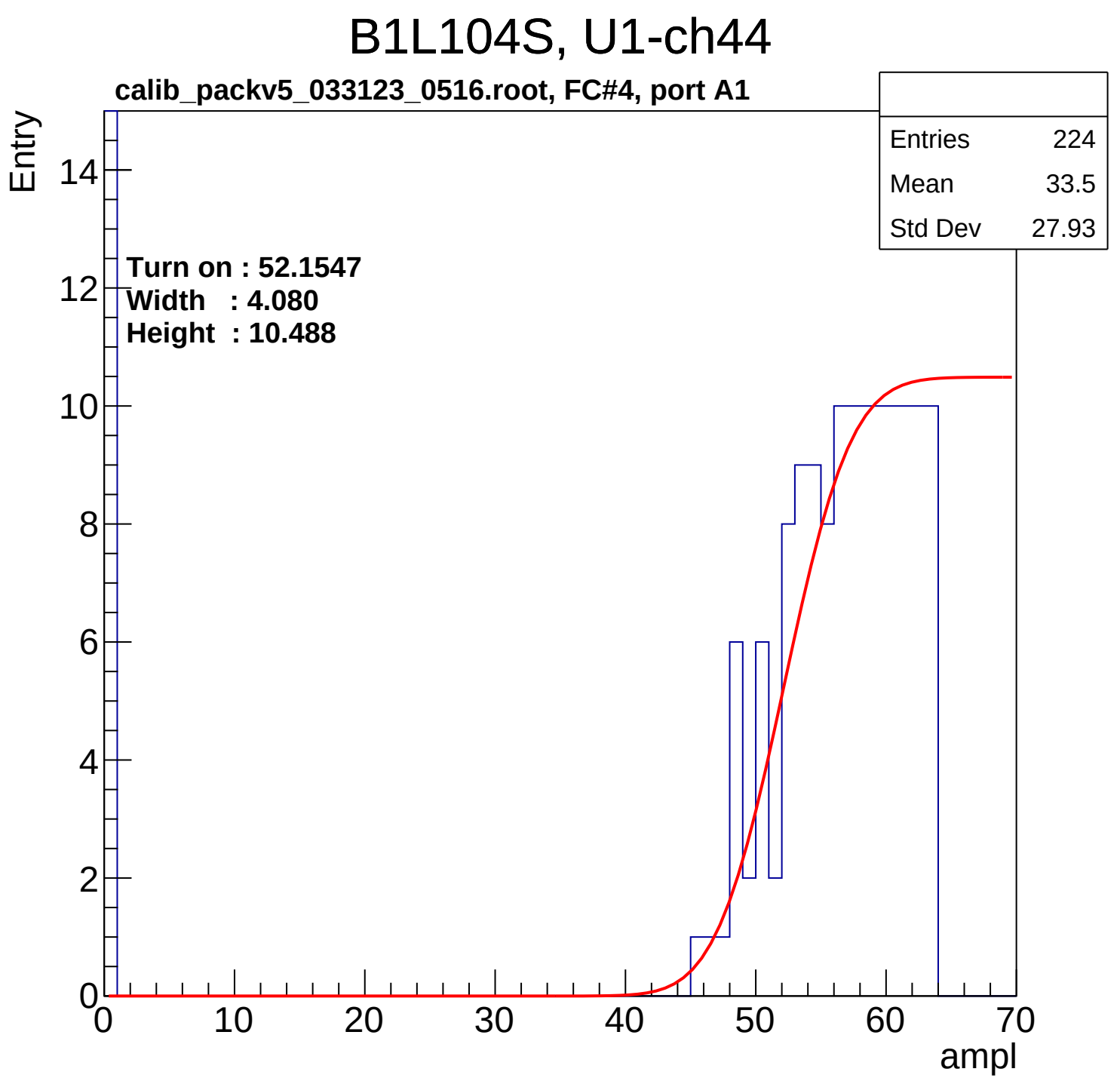

B1L104S, U1-ch39
calib_packv5_033123_0516.root, FC#4, port A1
Entries 213
Mean 36.11
Std Dev 27.17
Turn on : 50.2946
Width : 4.312
Height : 10.170
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

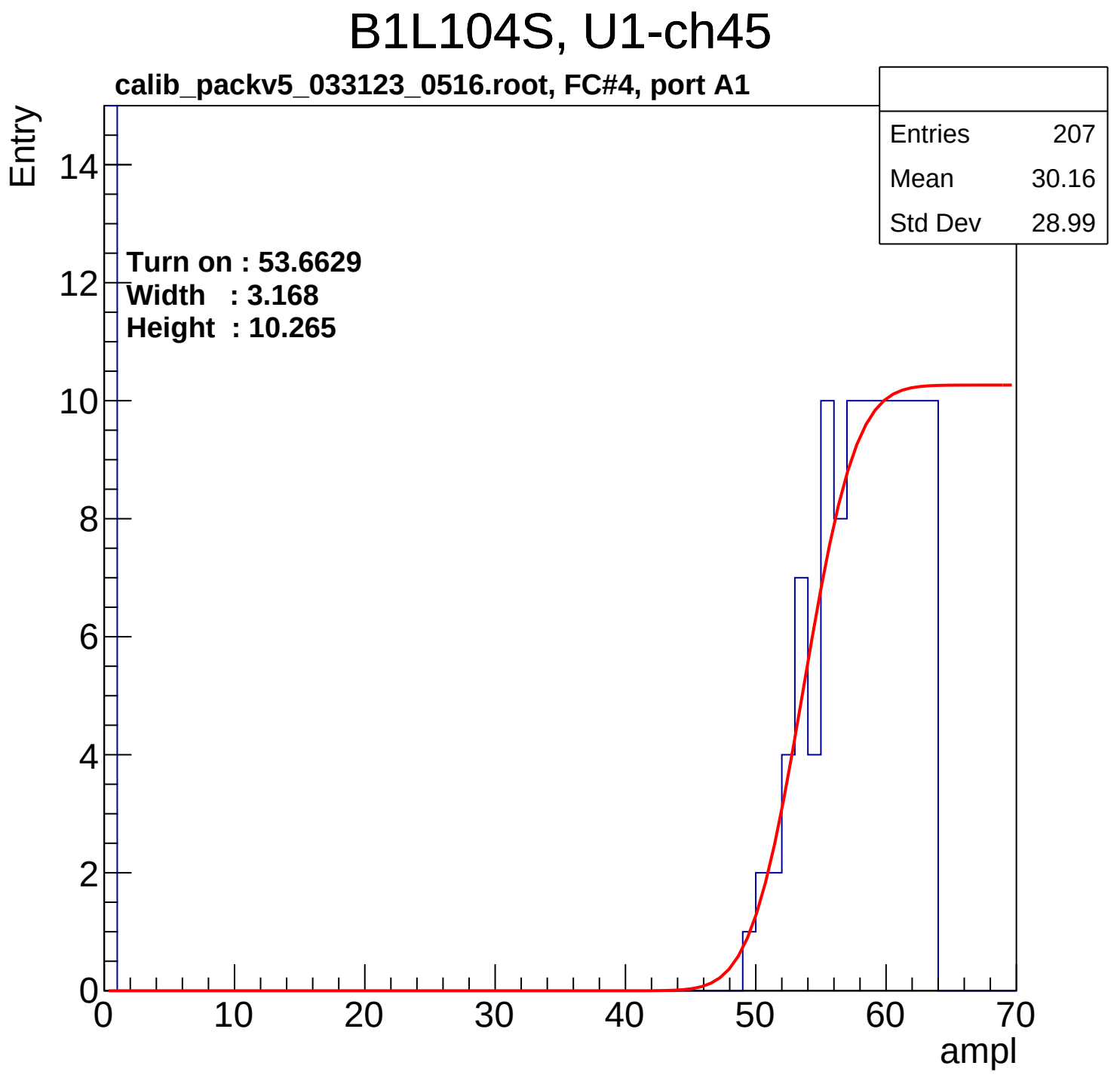

B1L104S, U1-ch40
calib_packv5_033123_0516.root, FC#4, port A1
Entries 227
Mean 32.82
Std Dev 28.06
Turn on : 51.3783
Width : 4.075
Height : 10.338
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

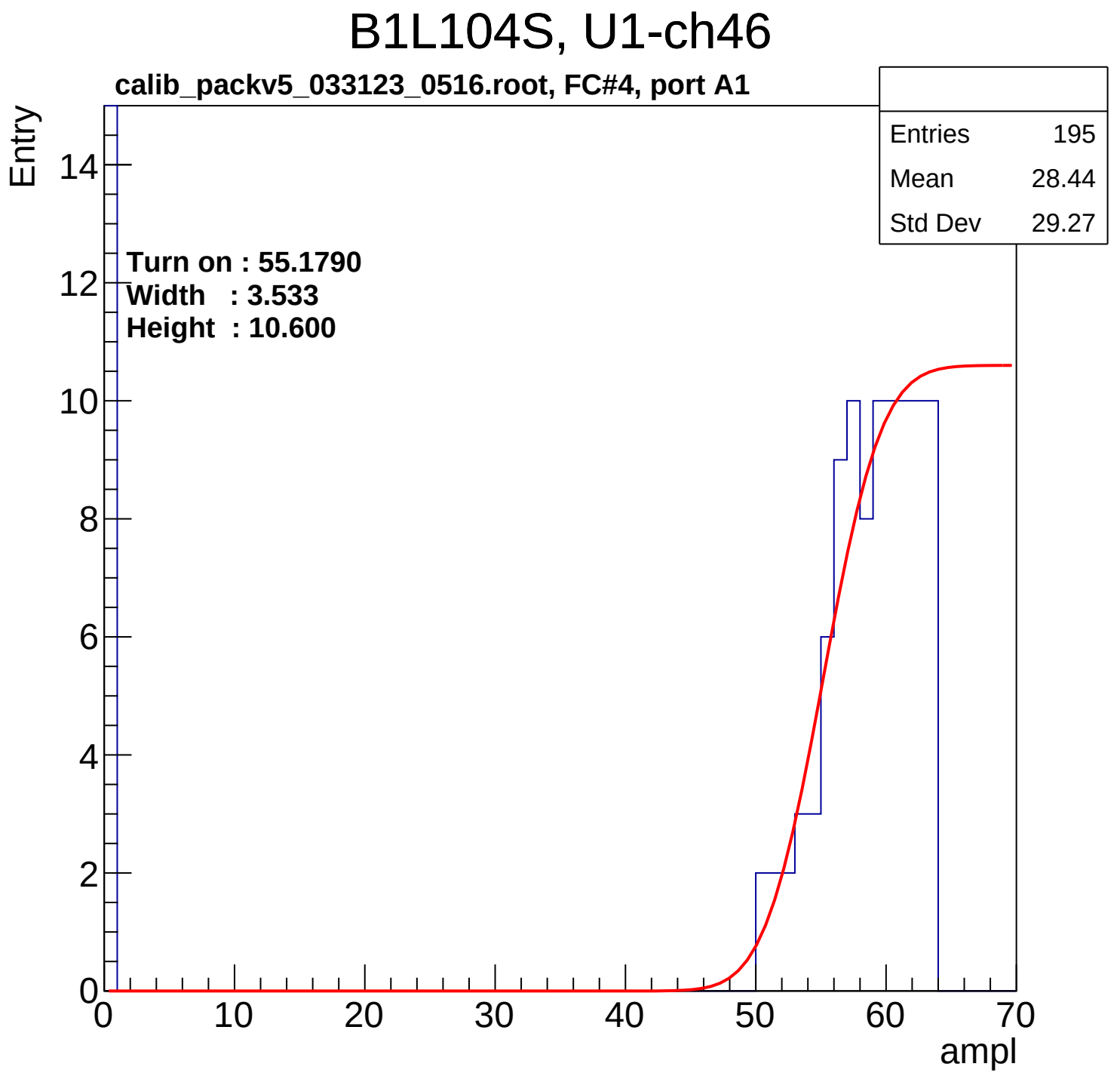

B1L104S, U1-ch41
calib_packv5_033123_0516.root, FC#4, port A1
Entries 171
Mean 37.01
Std Dev 27.73
Turn on : 53.5847
Width : 3.673
Height : 10.278
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

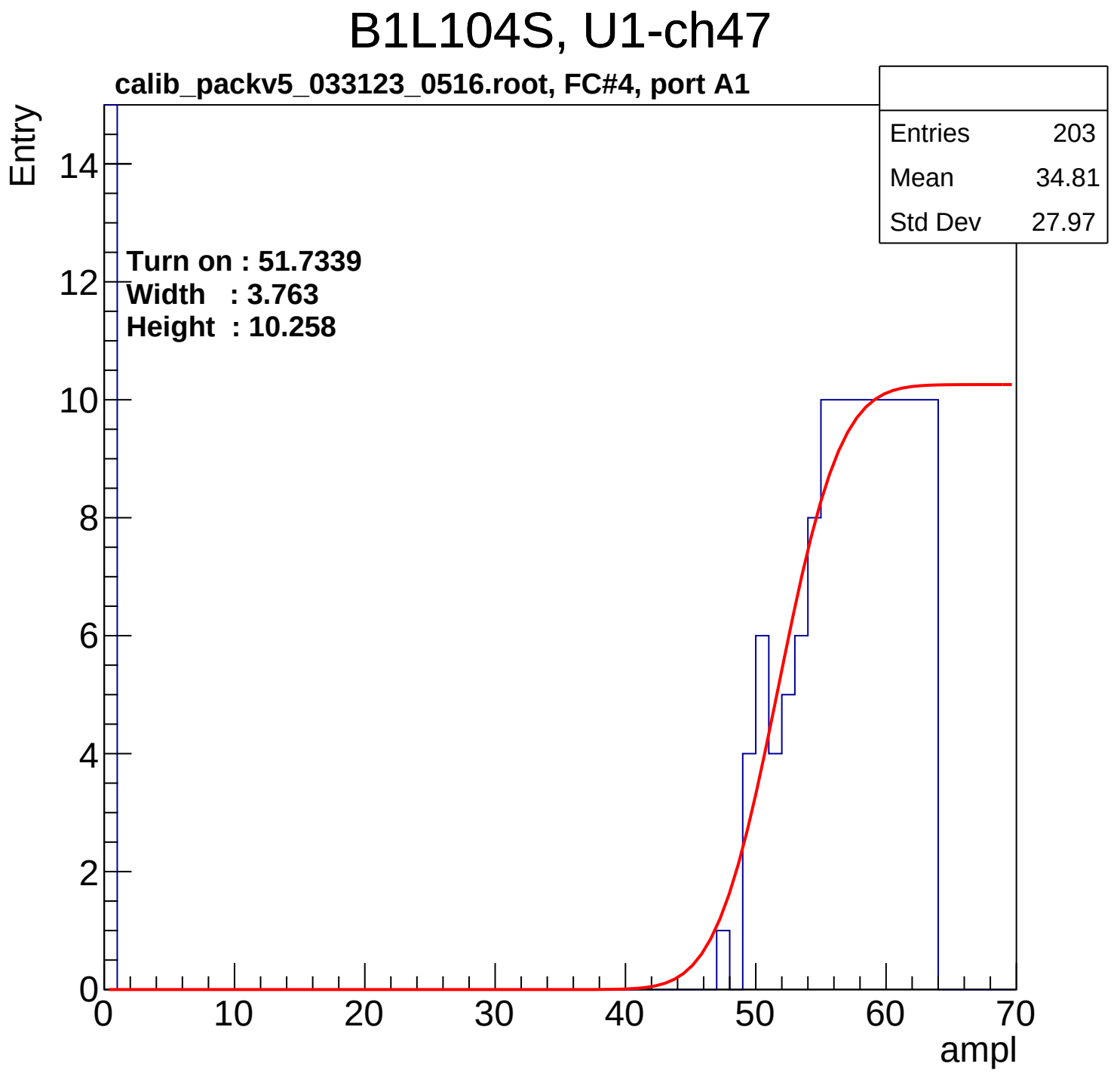

B1L104S, U1-ch42
calib_packv5_033123_0516.root, FC#4, port A1
Entries 201
Mean 29.17
Std Dev 29.14
Turn on : 55.1344
Width : 3.665
Height : 10.892
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

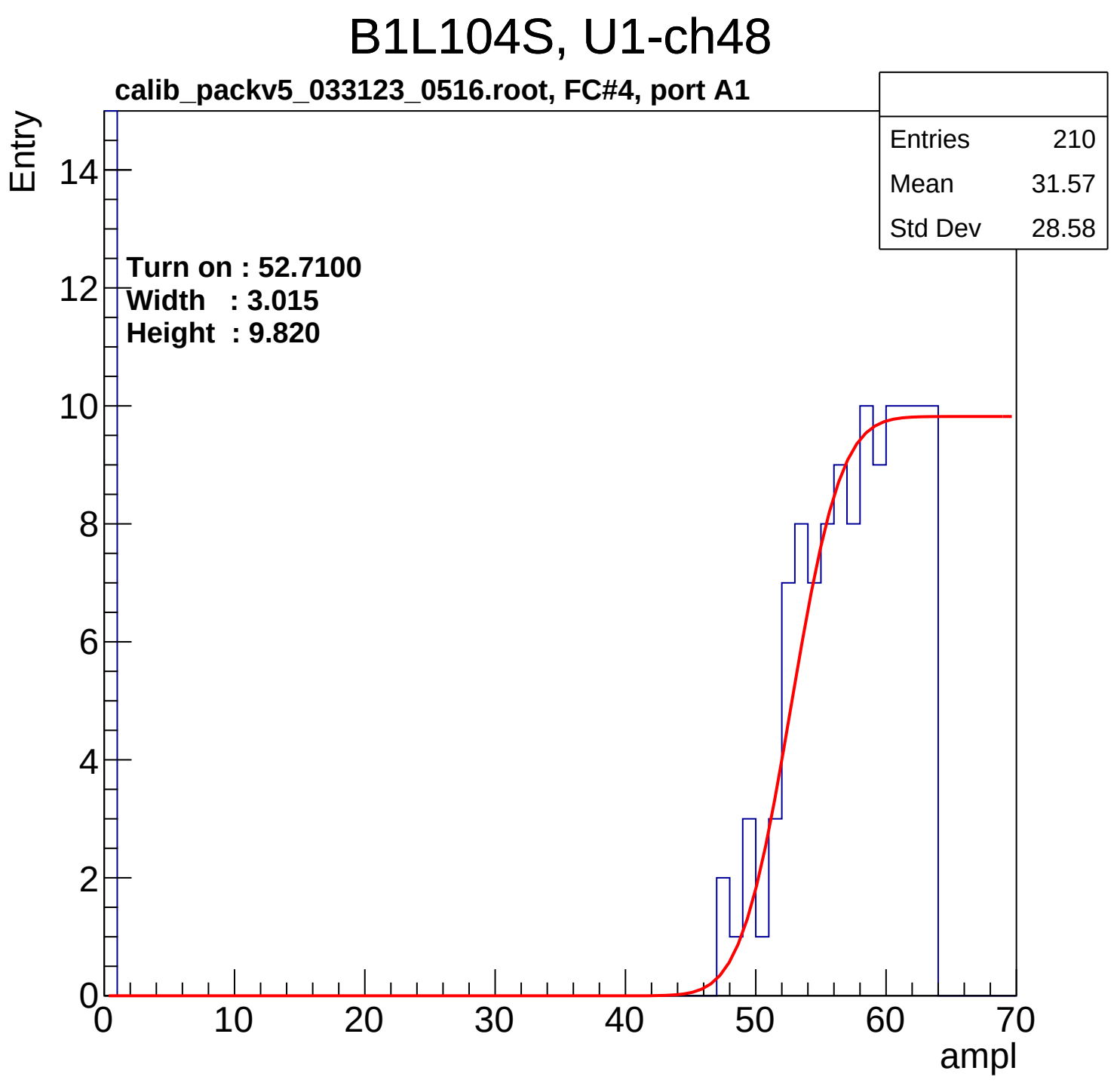

B1L104S, U1-ch43
calib_packv5_033123_0516.root, FC#4, port A1
Entries 188
Mean 33.26
Std Dev 28.74
Turn on : 53.1048
Width : 2.643
Height : 10.139
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

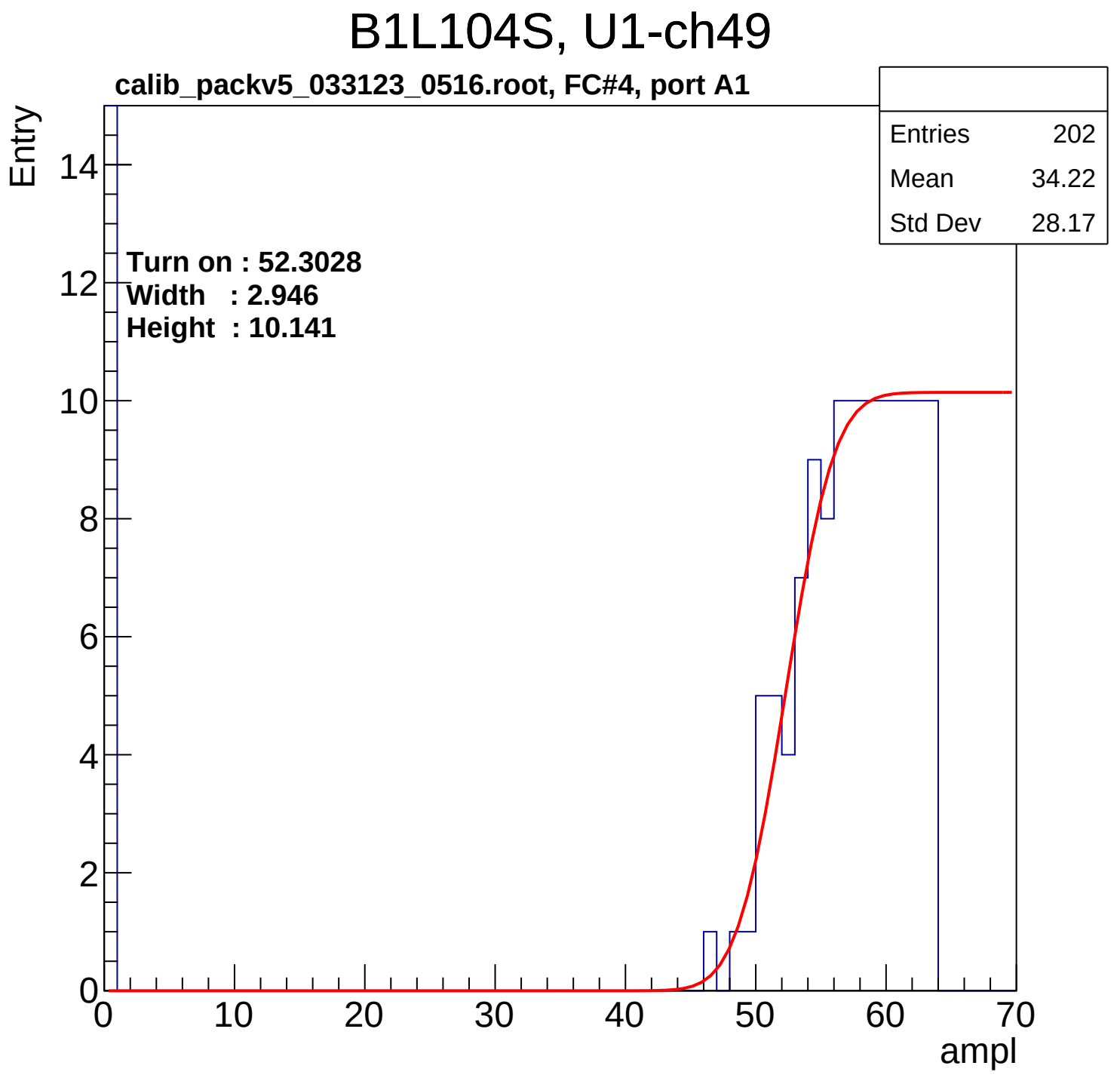

B1L104S, U1-ch44
calib_packv5_033123_0516.root, FC#4, port A1
Entries 224
Mean 33.5
Std Dev 27.93
Turn on : 52.1547
Width : 4.080
Height : 10.488
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

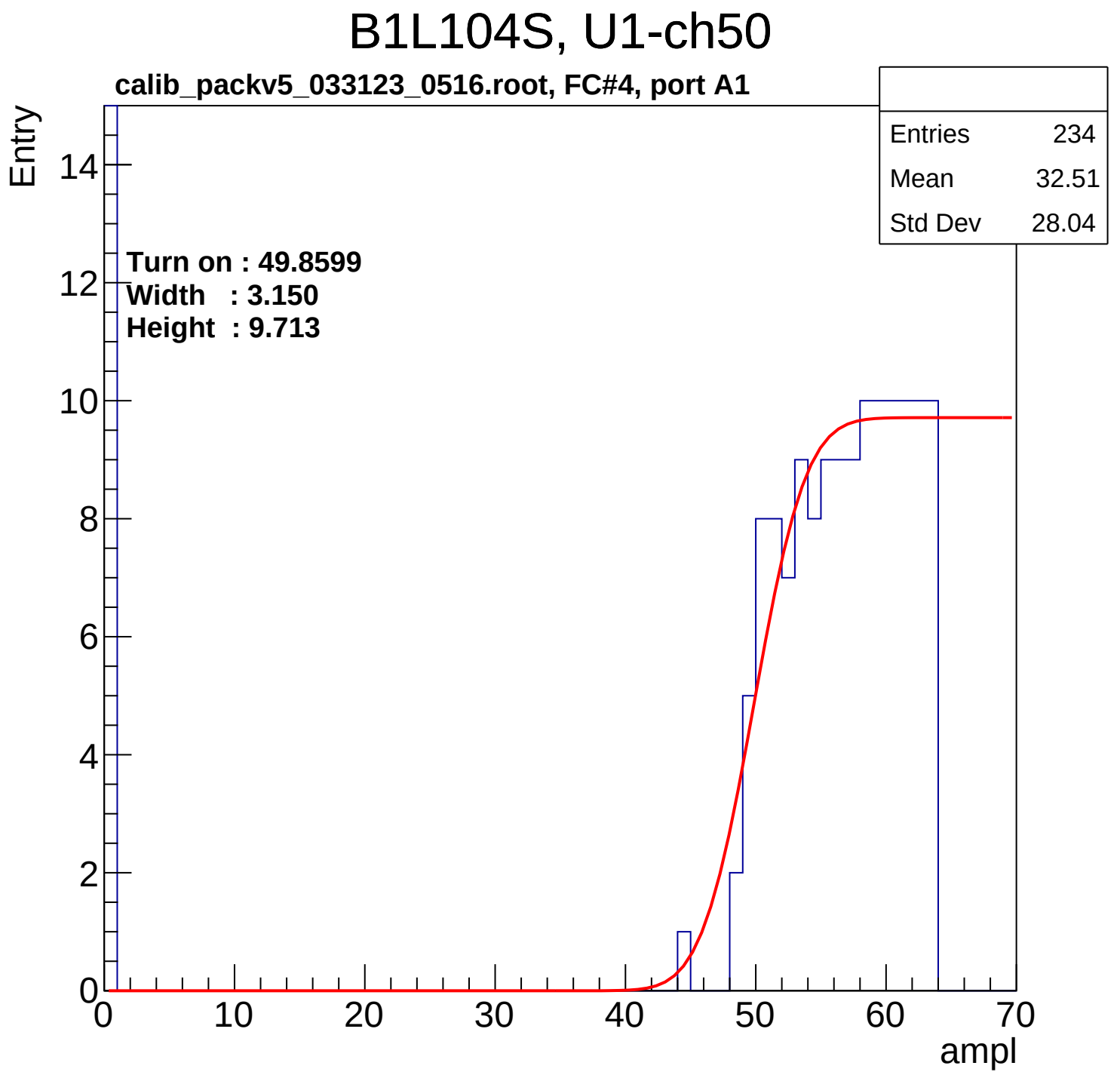

B1L104S, U1-ch45
calib_packv5_033123_0516.root, FC#4, port A1
Entries 207
Mean 30.16
Std Dev 28.99
Turn on : 53.6629
Width : 3.168
Height : 10.265
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

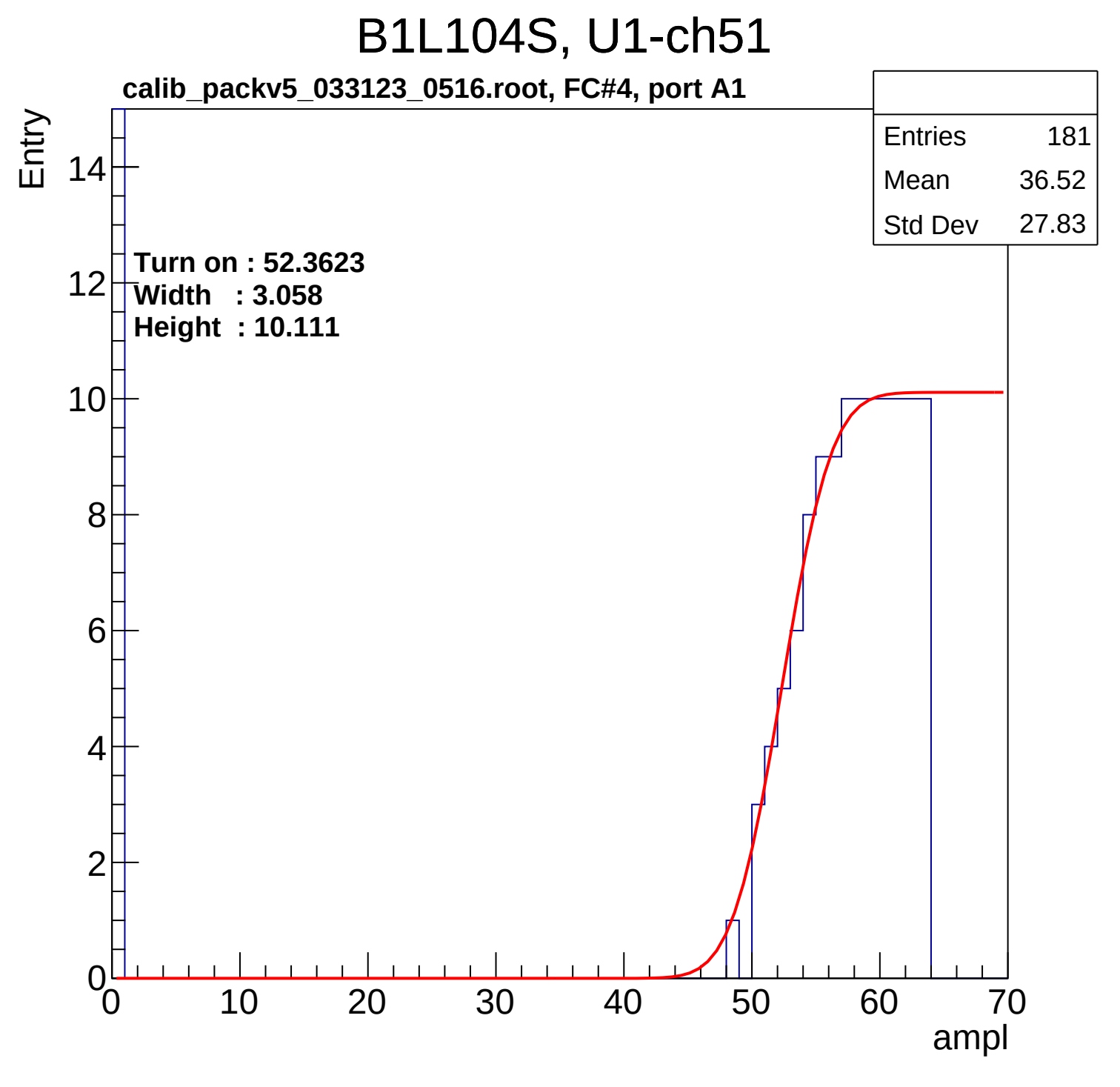

B1L104S, U1-ch46
calib_packv5_033123_0516.root, FC#4, port A1
Entries 195
Mean 28.44
Std Dev 29.27
Turn on : 55.1790
Width : 3.533
Height : 10.600
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

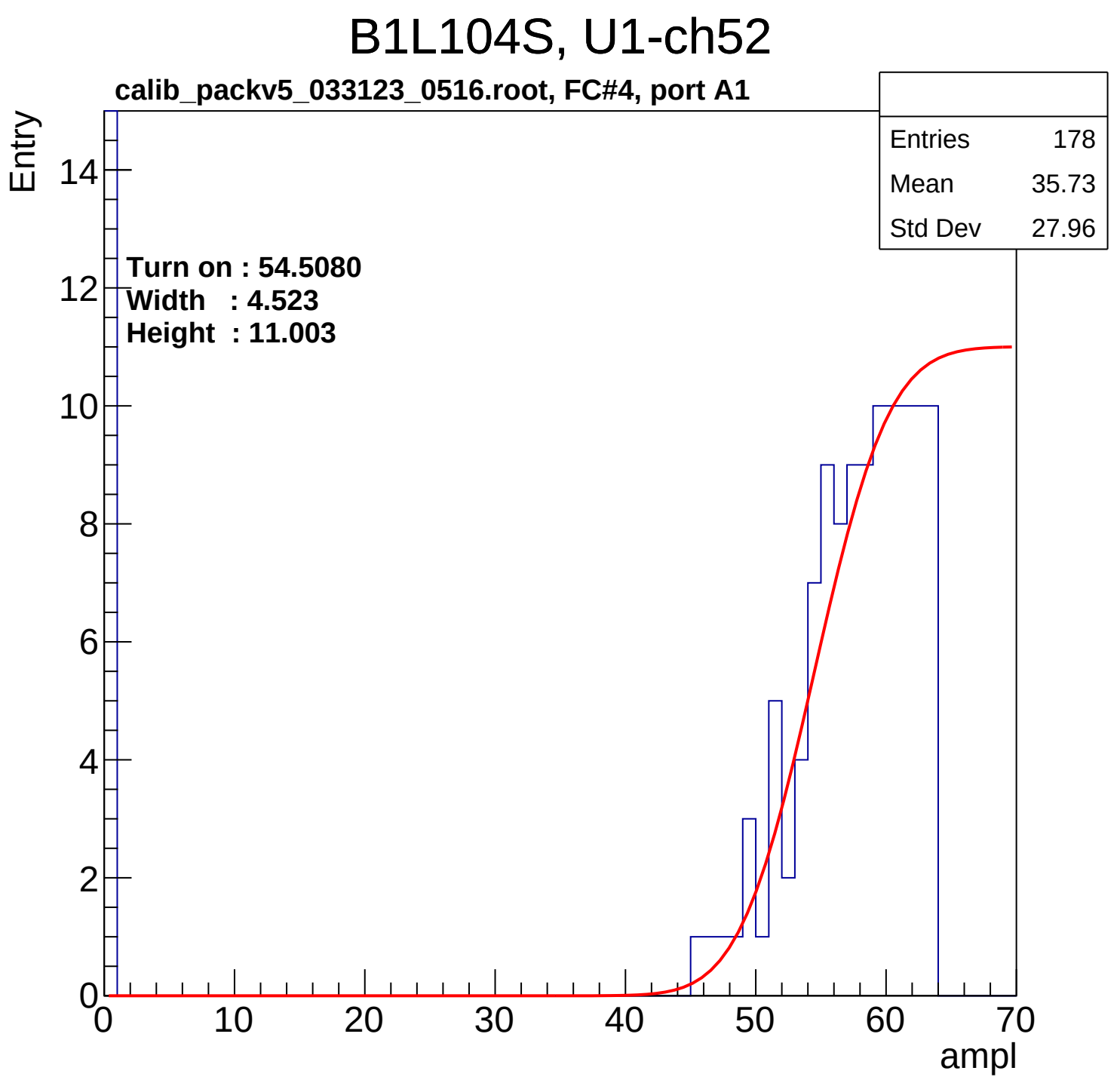

B1L104S, U1-ch47
calib_packv5_033123_0516.root, FC#4, port A1
Entries 203
Mean 34.81
Std Dev 27.97
Turn on : 51.7339
Width : 3.763
Height : 10.258
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

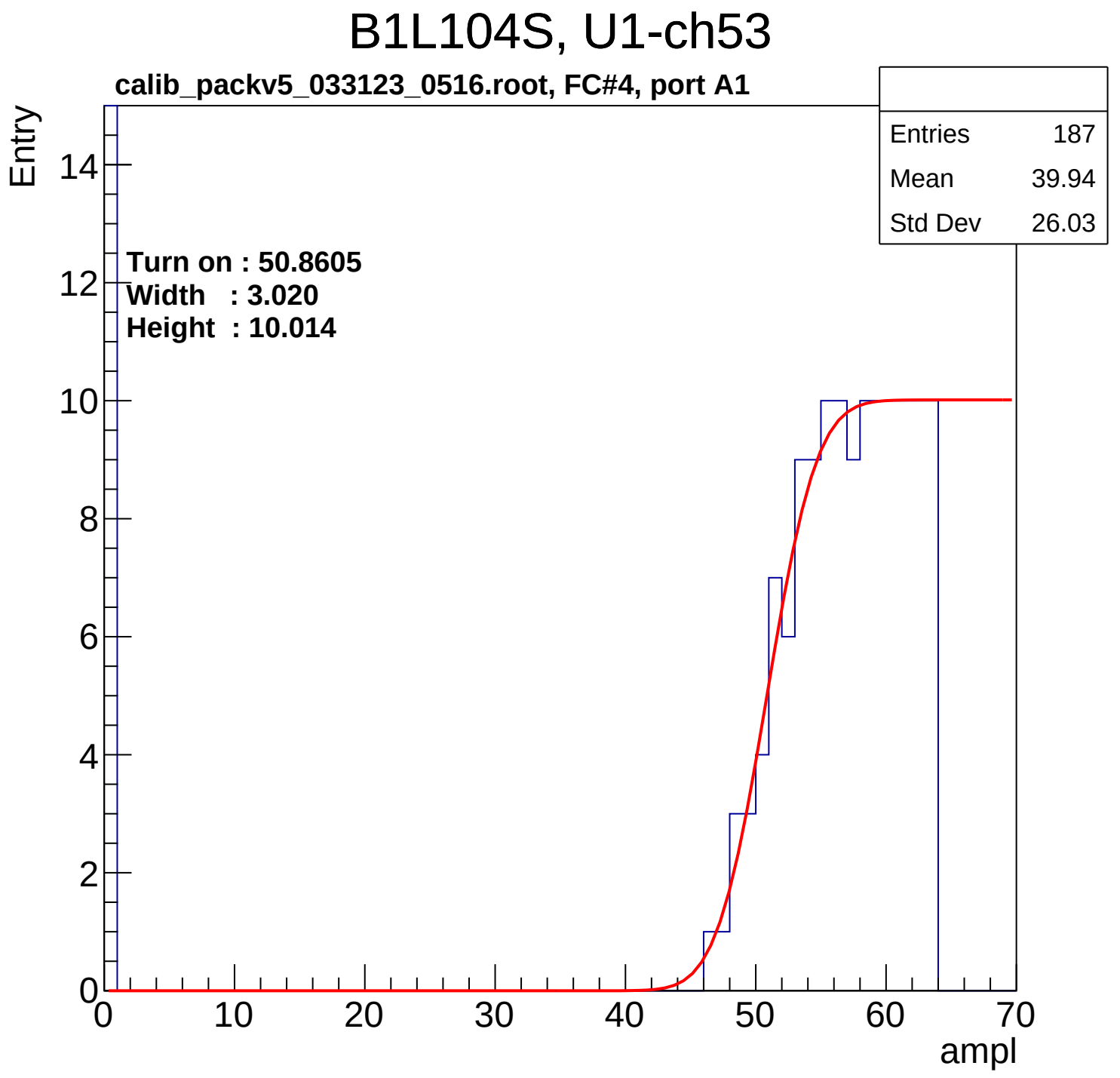

B1L104S, U1-ch48
calib_packv5_033123_0516.root, FC#4, port A1
Entries 210
Mean 31.57
Std Dev 28.58
Turn on : 52.7100
Width : 3.015
Height : 9.820
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

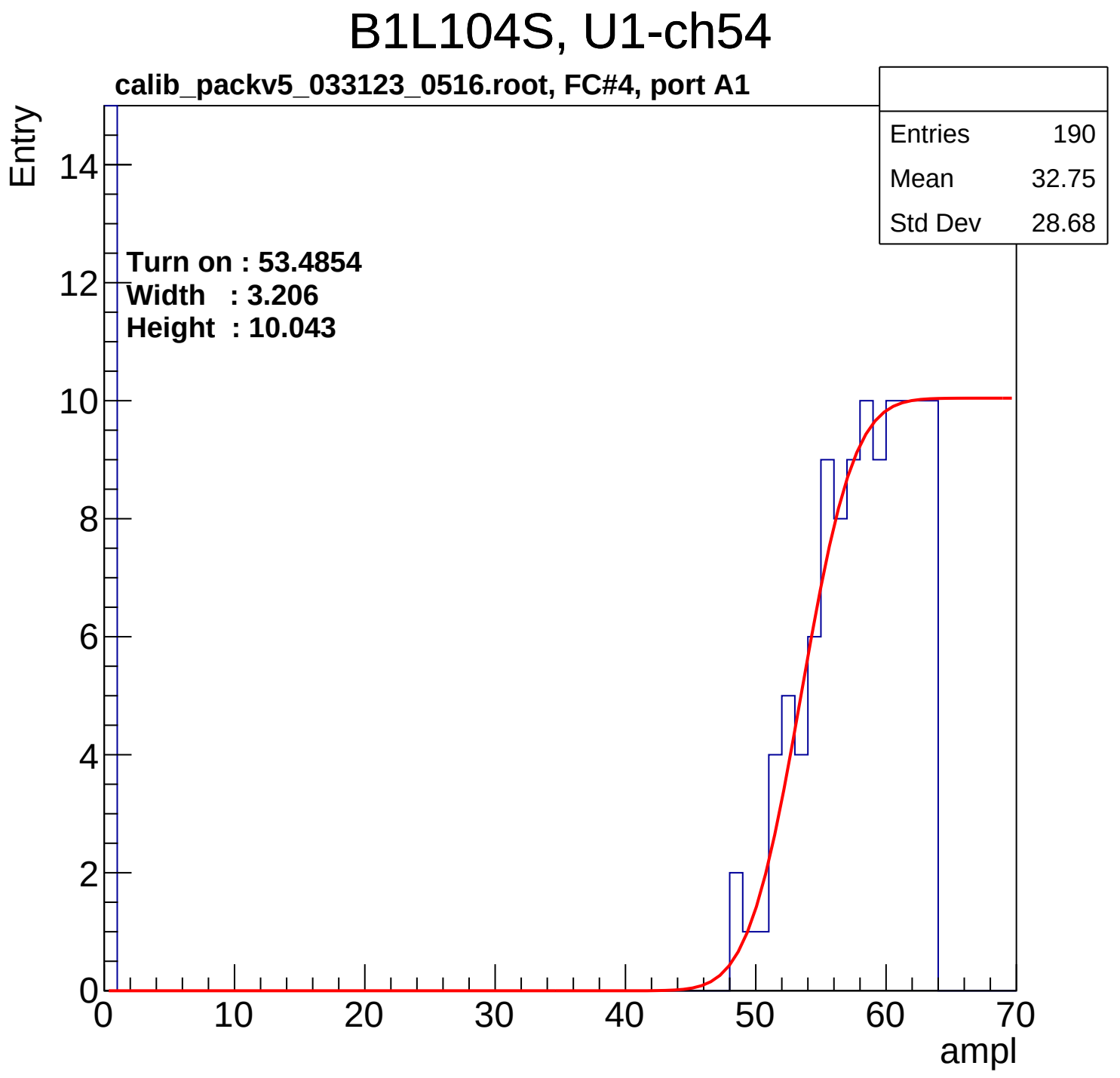

B1L104S, U1-ch49
calib_packv5_033123_0516.root, FC#4, port A1
Entries 202
Mean 34.22
Std Dev 28.17
Turn on : 52.3028
Width : 2.946
Height : 10.141
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

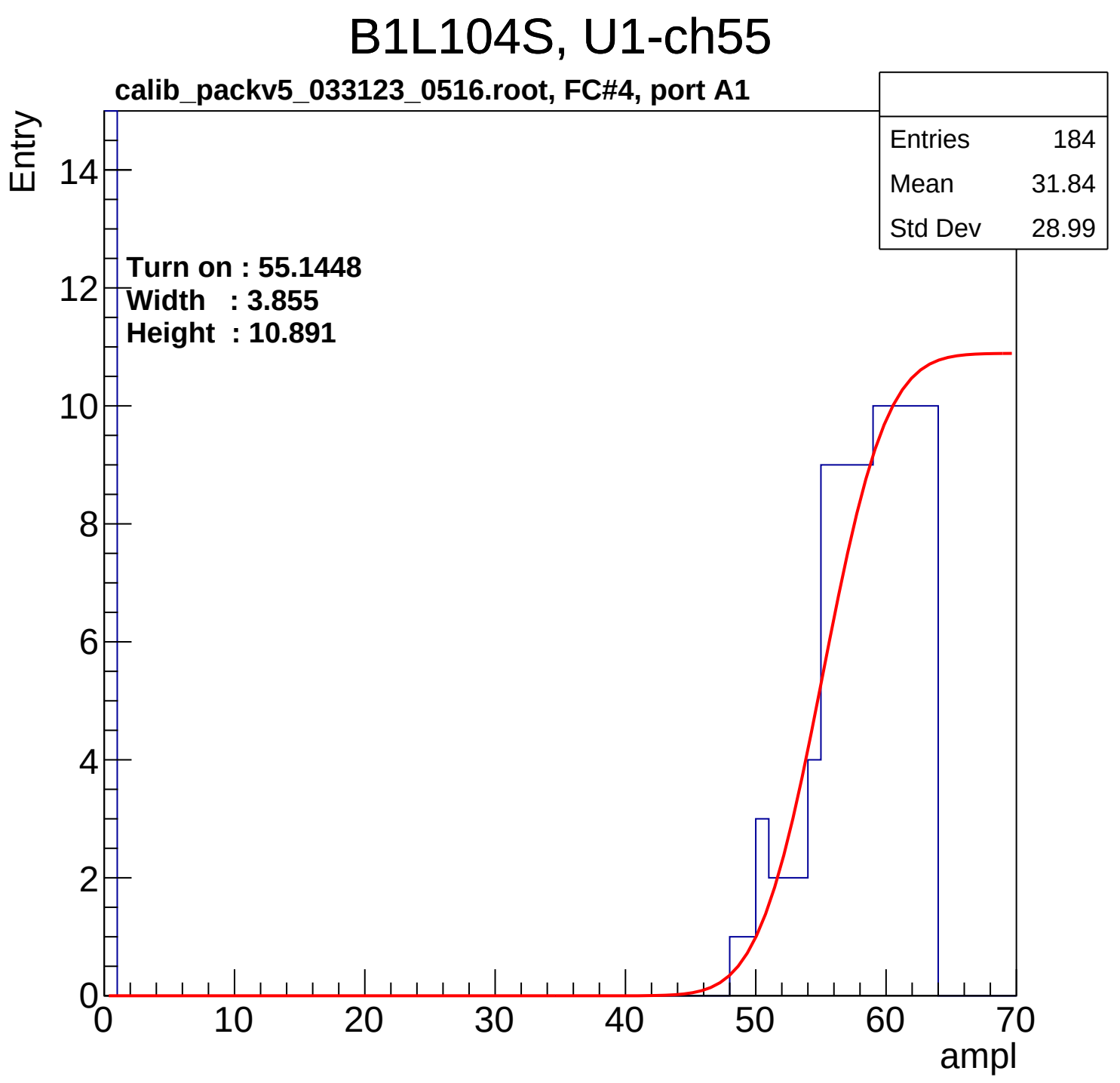

B1L104S, U1-ch50
calib_packv5_033123_0516.root, FC#4, port A1
Entries 234
Mean 32.51
Std Dev 28.04
Turn on : 49.8599
Width : 3.150
Height : 9.713
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

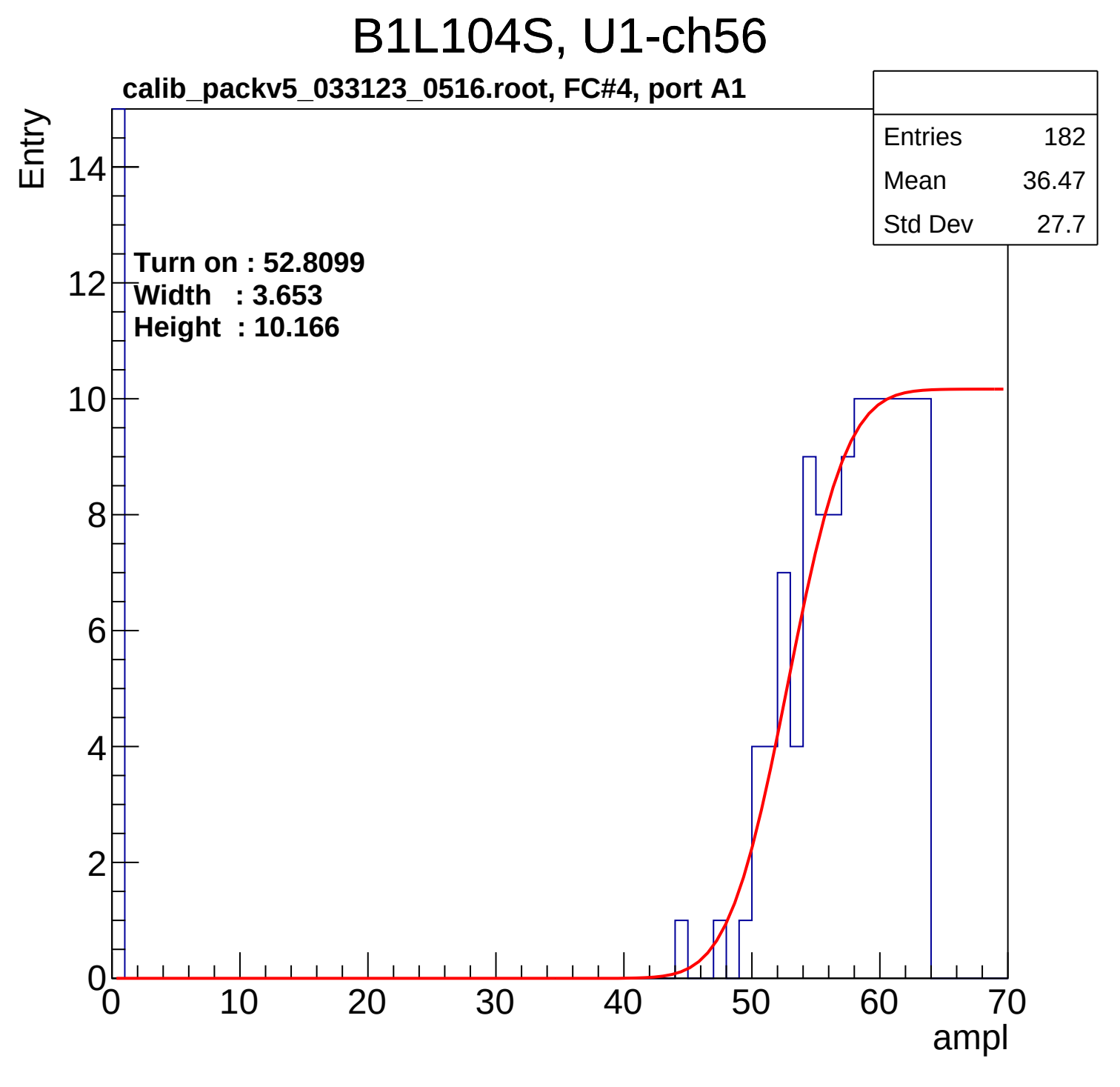

B1L104S, U1-ch51
calib_packv5_033123_0516.root, FC#4, port A1
Entries 181
Mean 36.52
Std Dev 27.83
Turn on : 52.3623
Width : 3.058
Height : 10.111
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

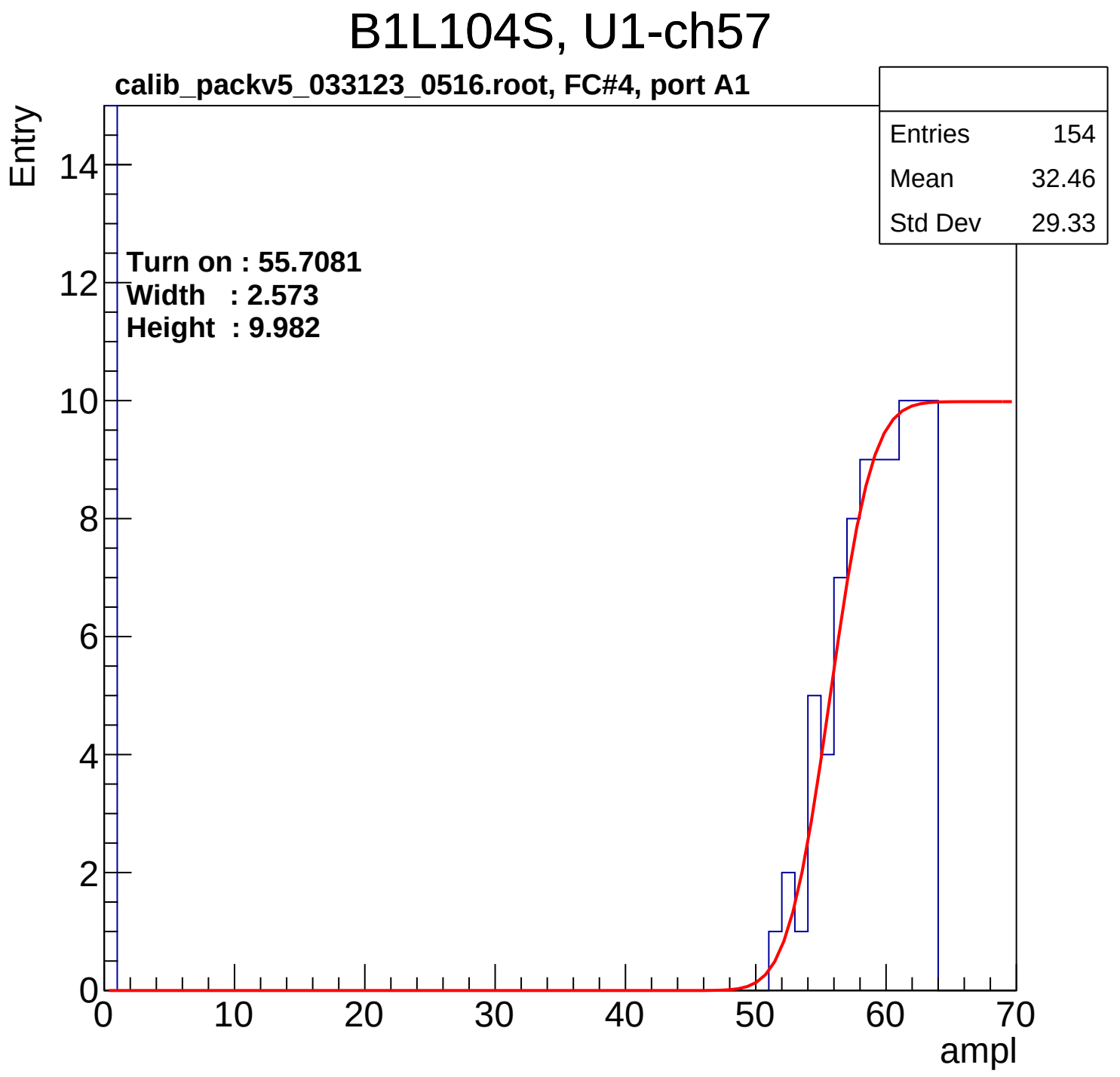

B1L104S, U1-ch52
calib_packv5_033123_0516.root, FC#4, port A1
Entries 178
Mean 35.73
Std Dev 27.96
Turn on : 54.5080
Width : 4.523
Height : 11.003
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

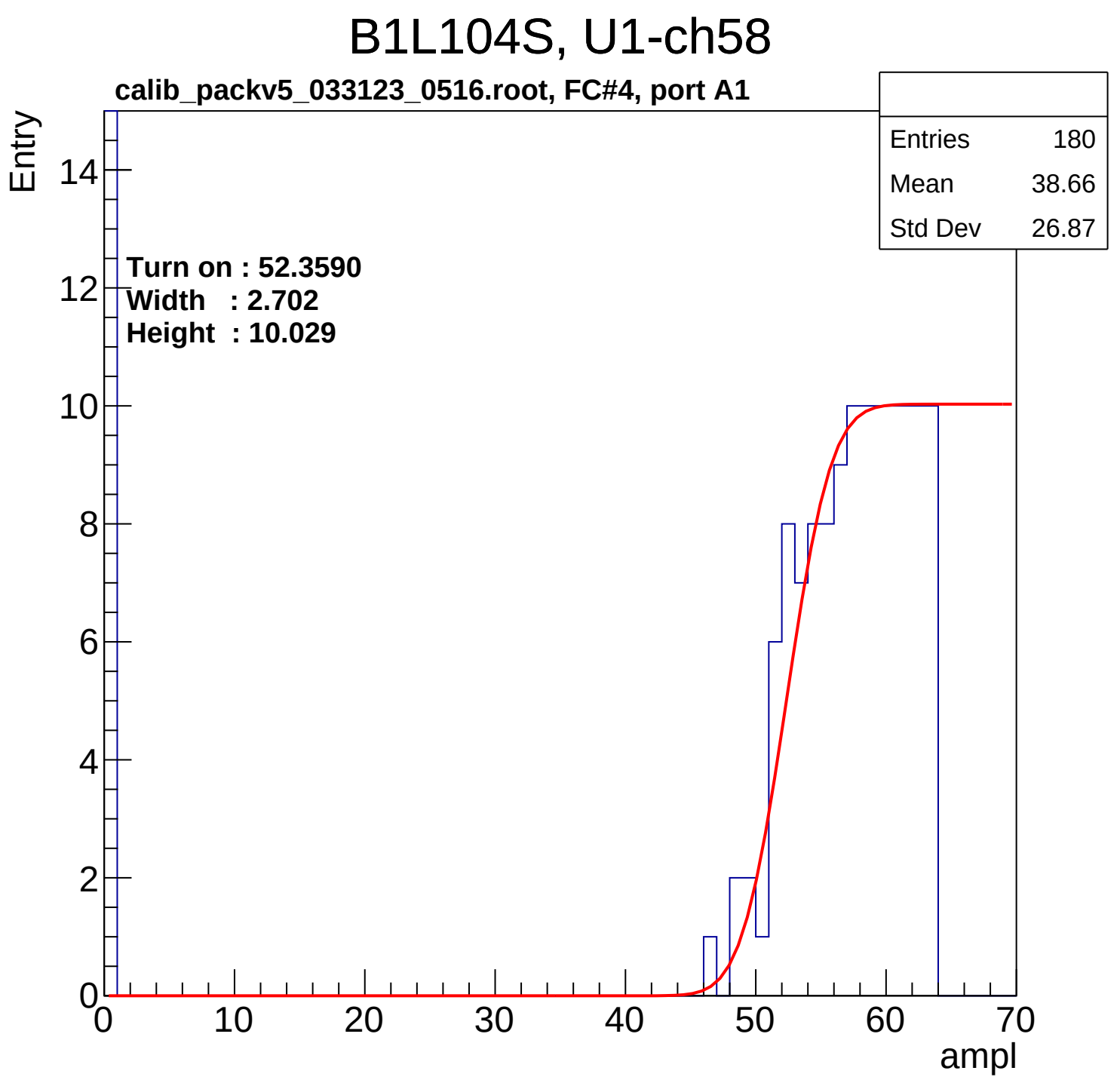

B1L104S, U1-ch53
calib_packv5_033123_0516.root, FC#4, port A1
Entries 187
Mean 39.94
Std Dev 26.03
Turn on : 50.8605
Width : 3.020
Height : 10.014
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

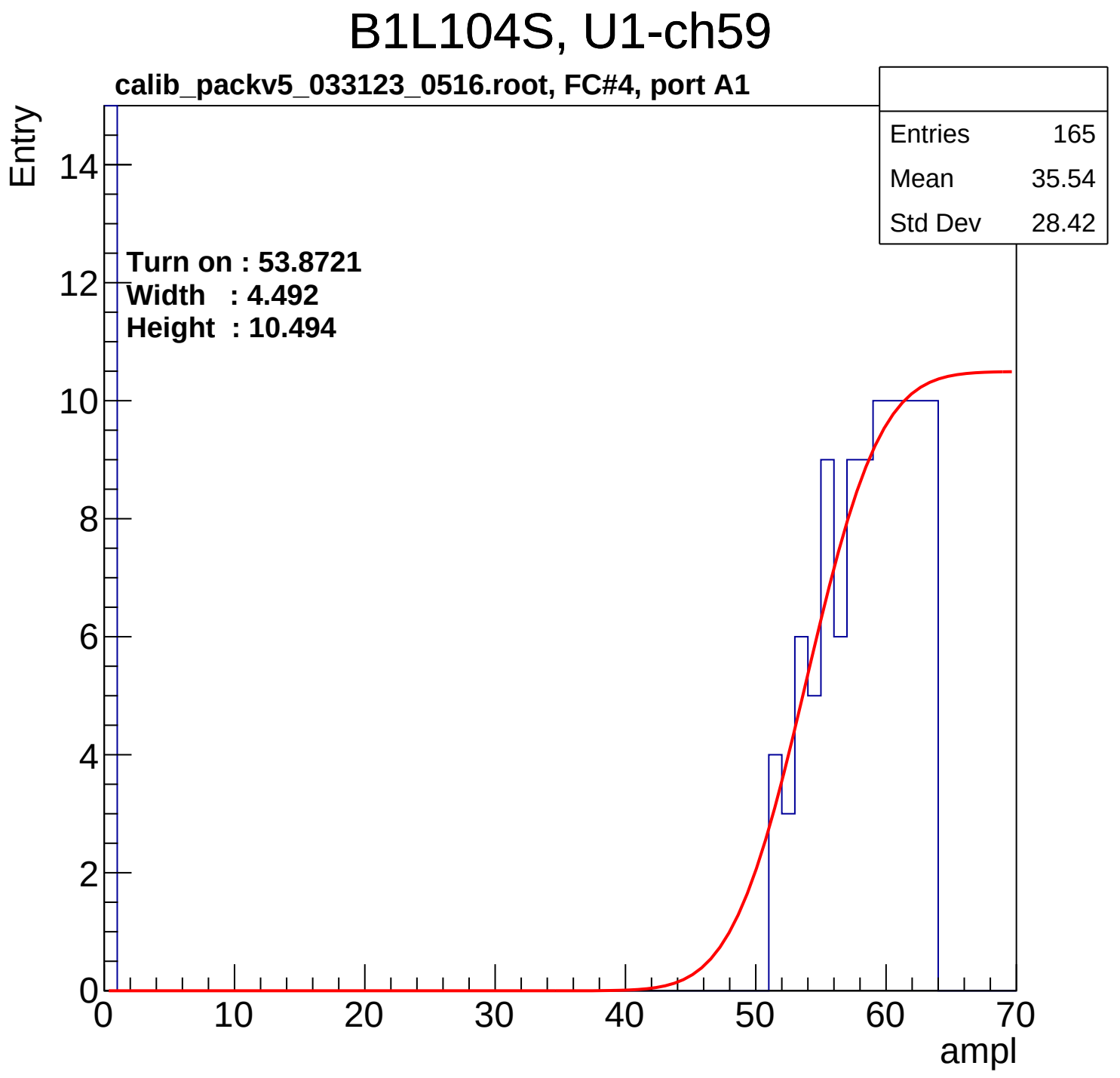

B1L104S, U1-ch54
calib_packv5_033123_0516.root, FC#4, port A1
Entries 190
Mean 32.75
Std Dev 28.68
Turn on : 53.4854
Width : 3.206
Height : 10.043
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

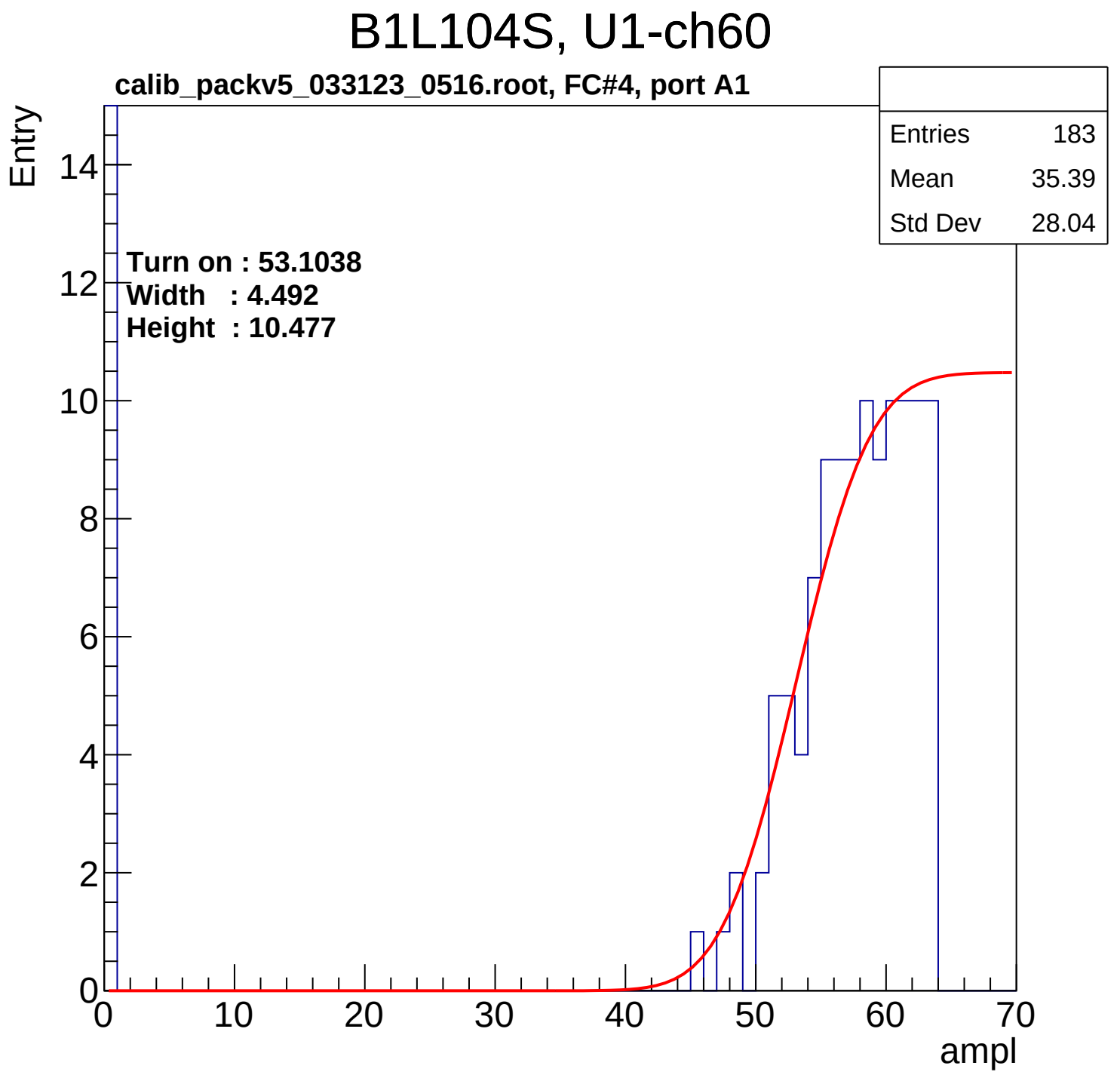

B1L104S, U1-ch55
calib_packv5_033123_0516.root, FC#4, port A1
Entries 184
Mean 31.84
Std Dev 28.99
Turn on : 55.1448
Width : 3.855
Height : 10.891
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

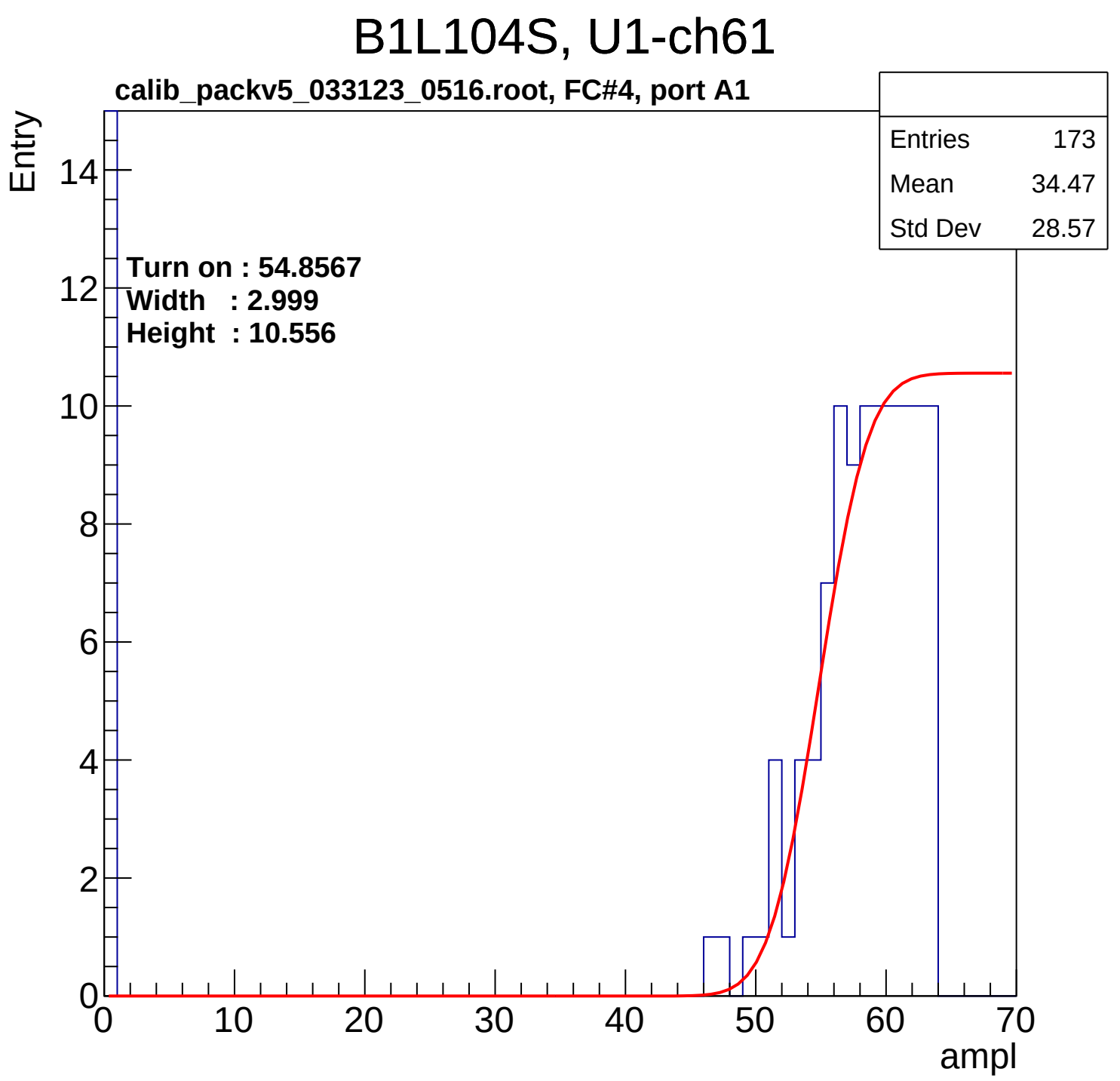

B1L104S, U1-ch56
calib_packv5_033123_0516.root, FC#4, port A1
Entries 182
Mean 36.47
Std Dev 27.7
Turn on : 52.8099
Width : 3.653
Height : 10.166
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

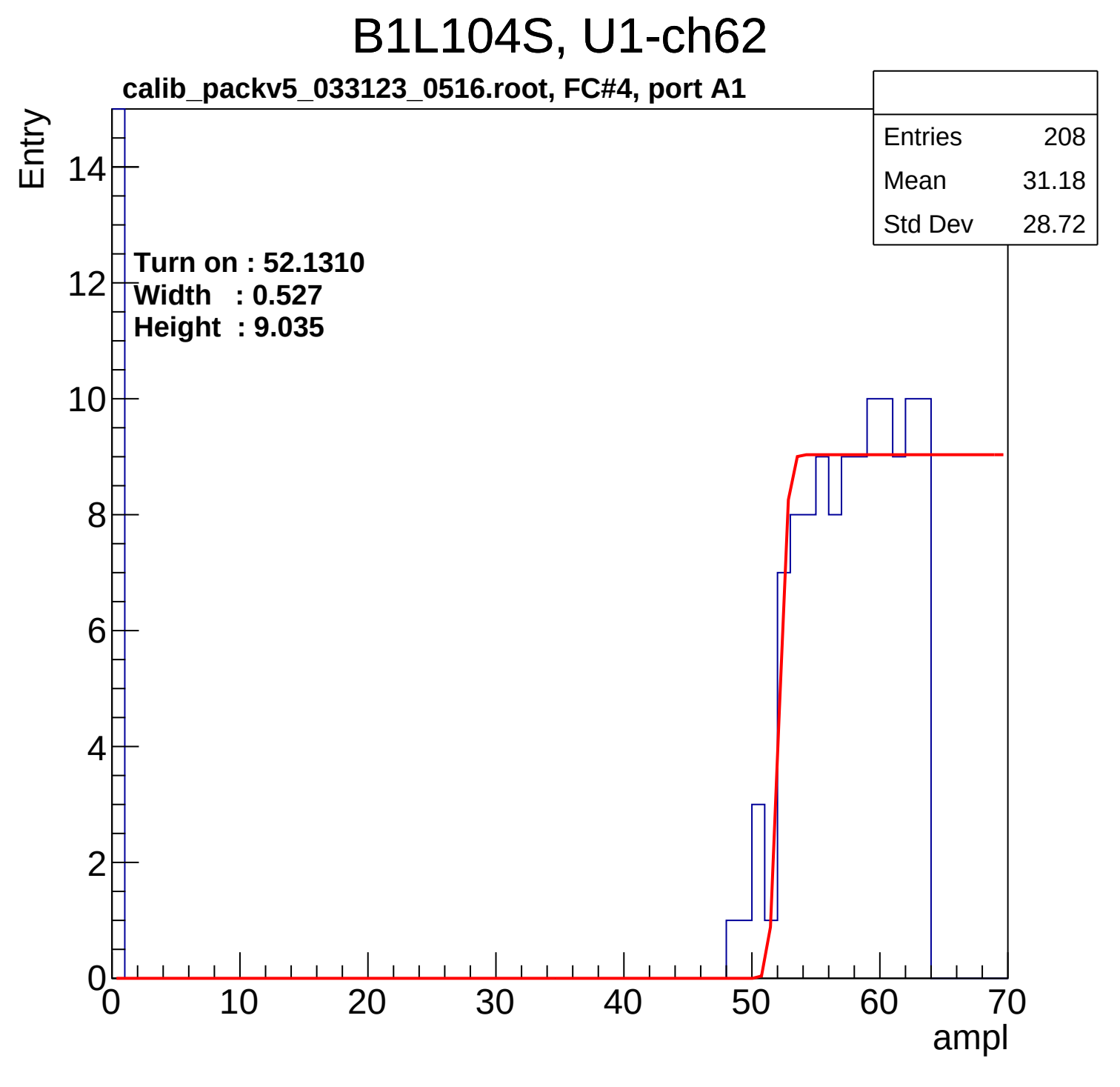

B1L104S, U1-ch57
calib_packv5_033123_0516.root, FC#4, port A1
Entries 154
Mean 32.46
Std Dev 29.33
Turn on : 55.7081
Width : 2.573
Height : 9.982
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

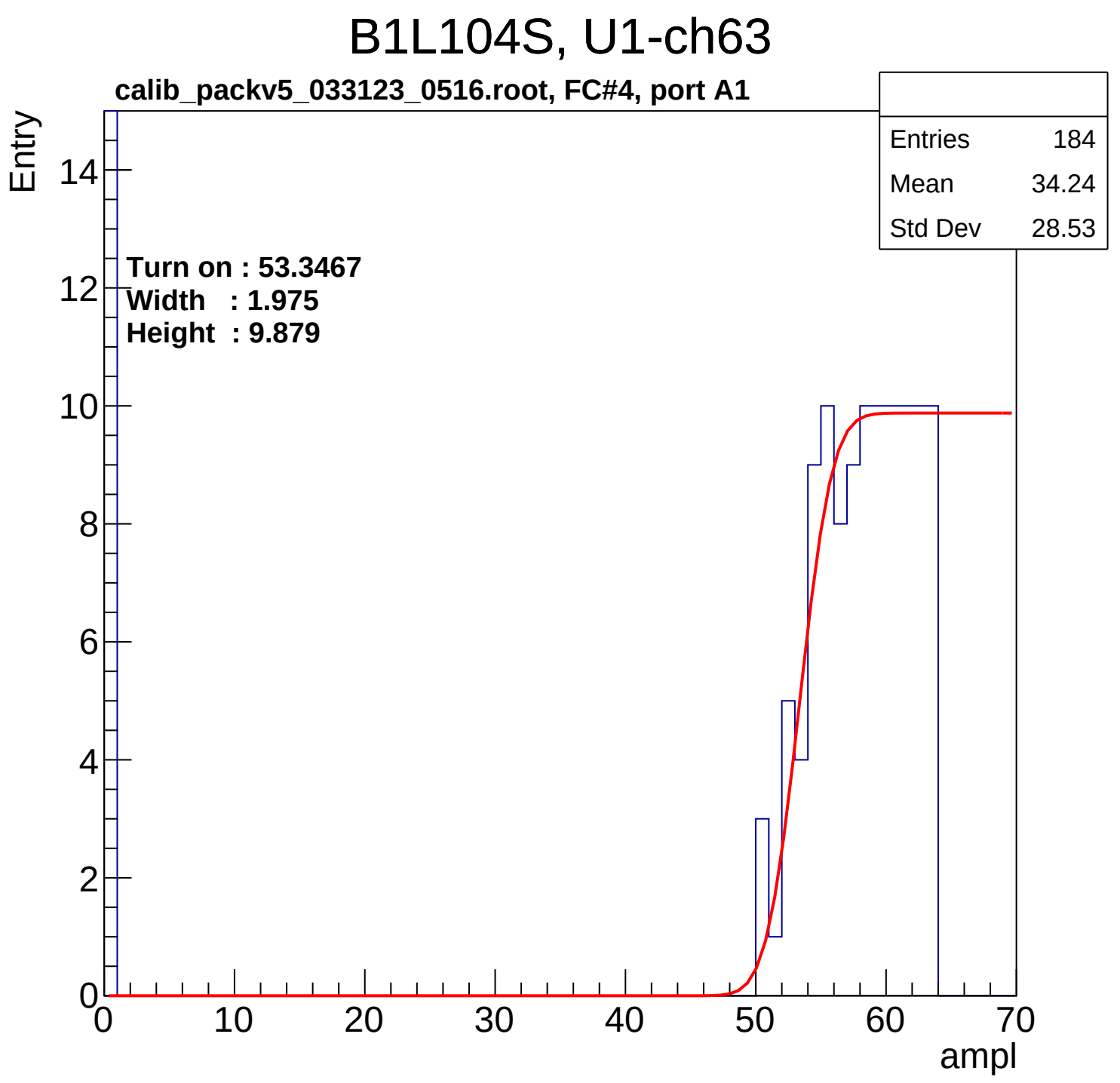

B1L104S, U1-ch58
calib_packv5_033123_0516.root, FC#4, port A1
Entries 180
Mean 38.66
Std Dev 26.87
Turn on : 52.3590
Width : 2.702
Height : 10.029
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

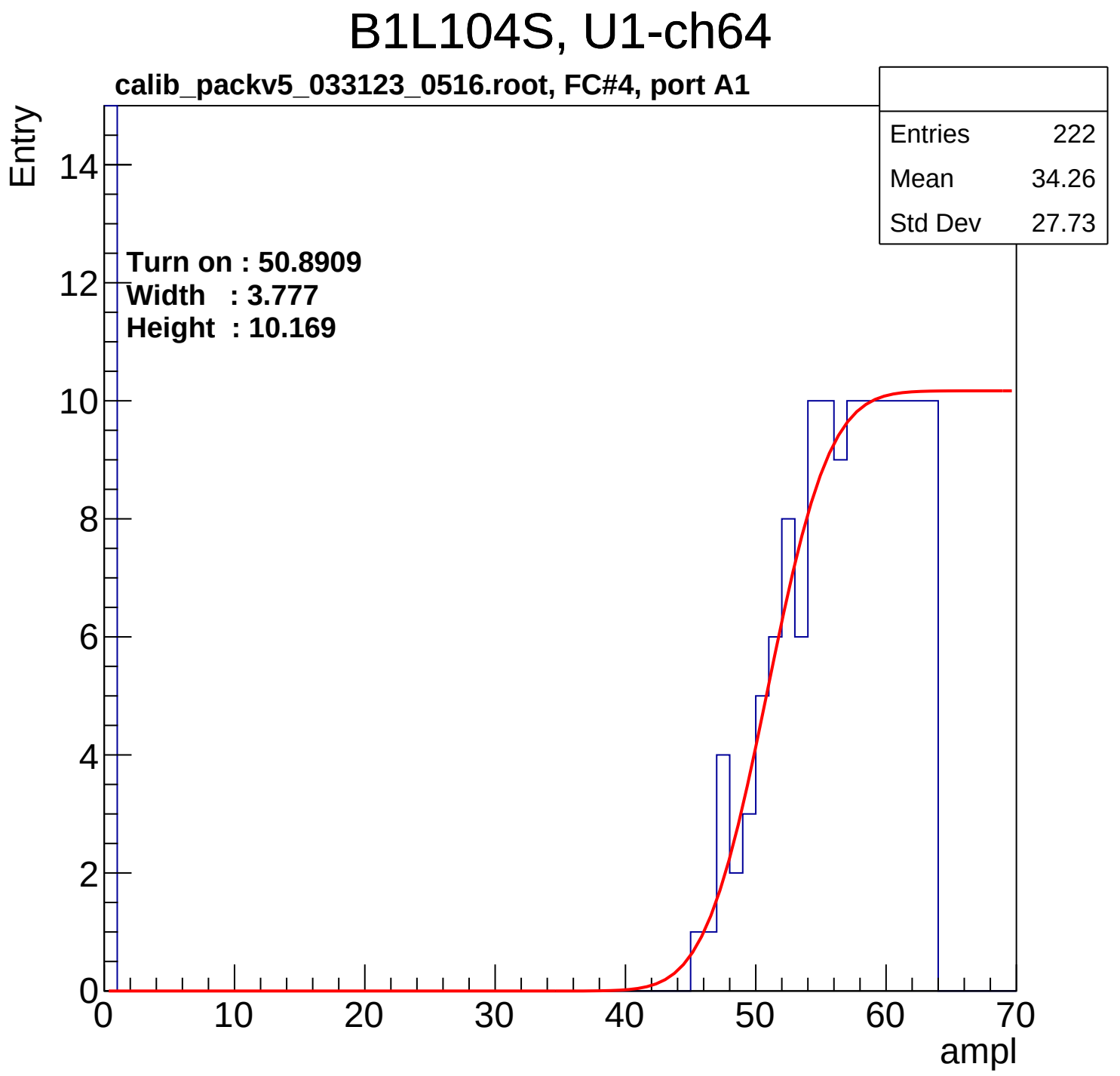

B1L104S, U1-ch59
calib_packv5_033123_0516.root, FC#4, port A1
Entries 165
Mean 35.54
Std Dev 28.42
Turn on : 53.8721
Width : 4.492
Height : 10.494
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

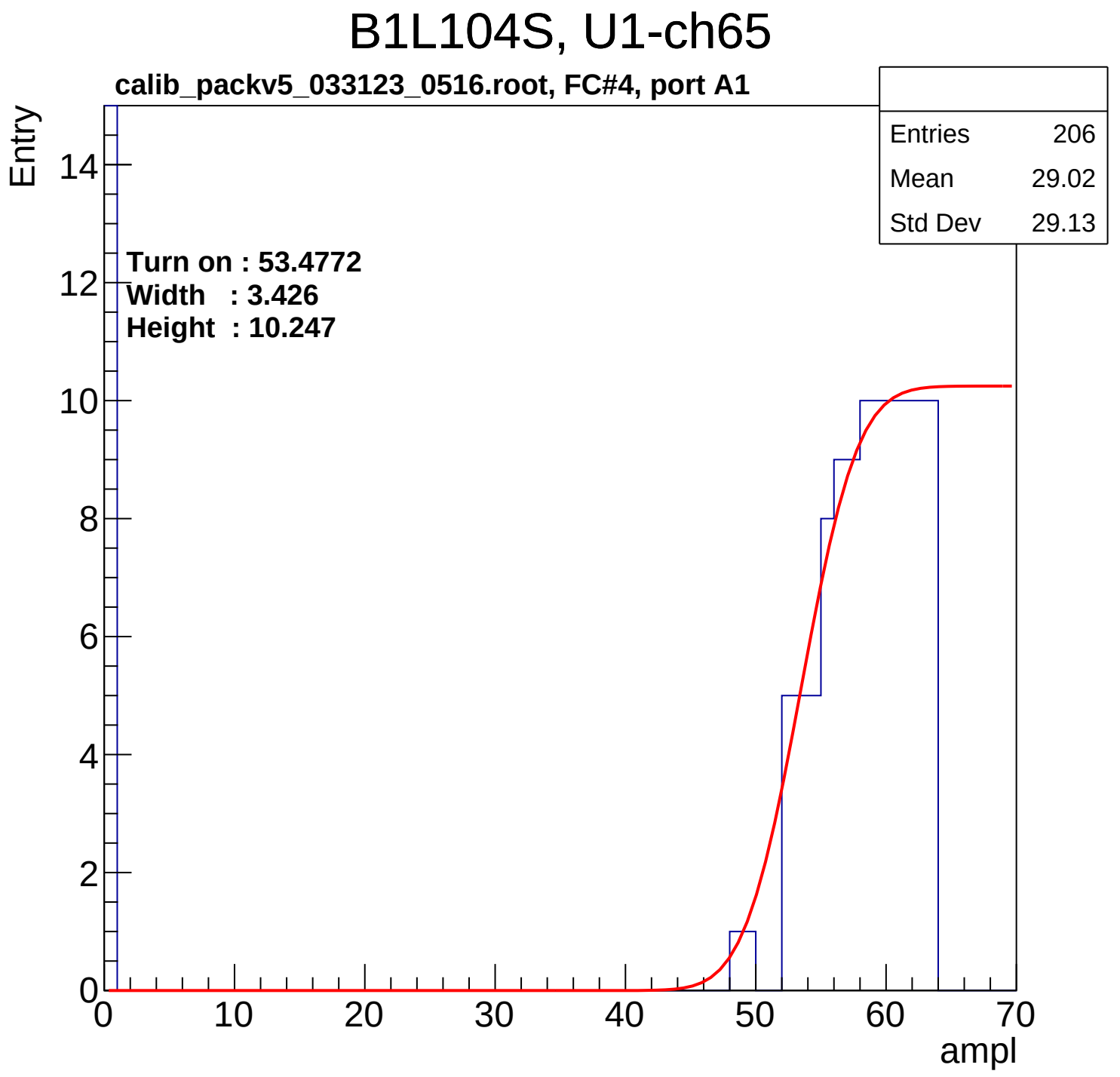

B1L104S, U1-ch60
calib_packv5_033123_0516.root, FC#4, port A1
Entries 183
Mean 35.39
Std Dev 28.04
Turn on : 53.1038
Width : 4.492
Height : 10.477
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

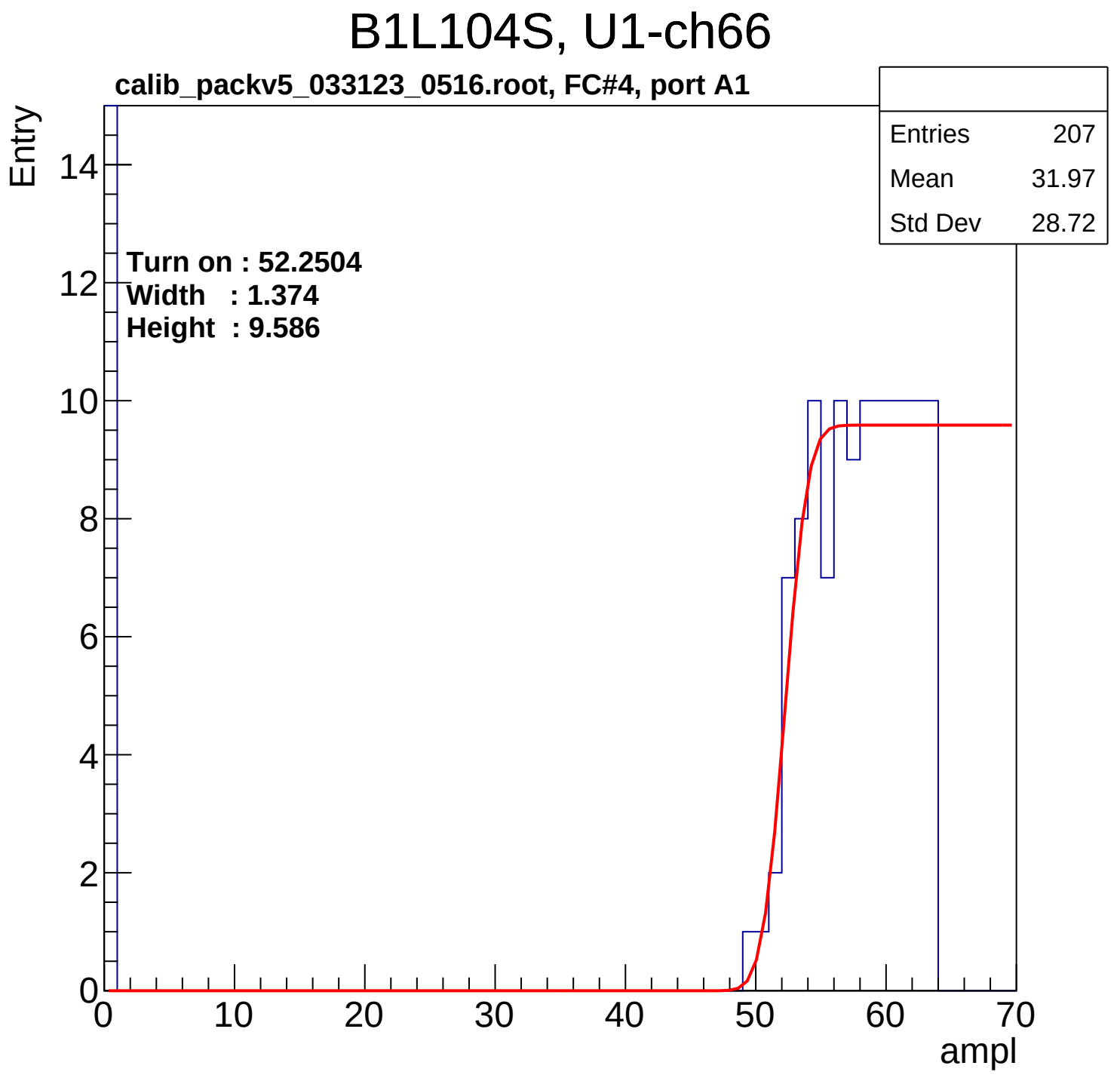

B1L104S, U1-ch61
calib_packv5_033123_0516.root, FC#4, port A1
Entries 173
Mean 34.47
Std Dev 28.57
Turn on : 54.8567
Width : 2.999
Height : 10.556
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

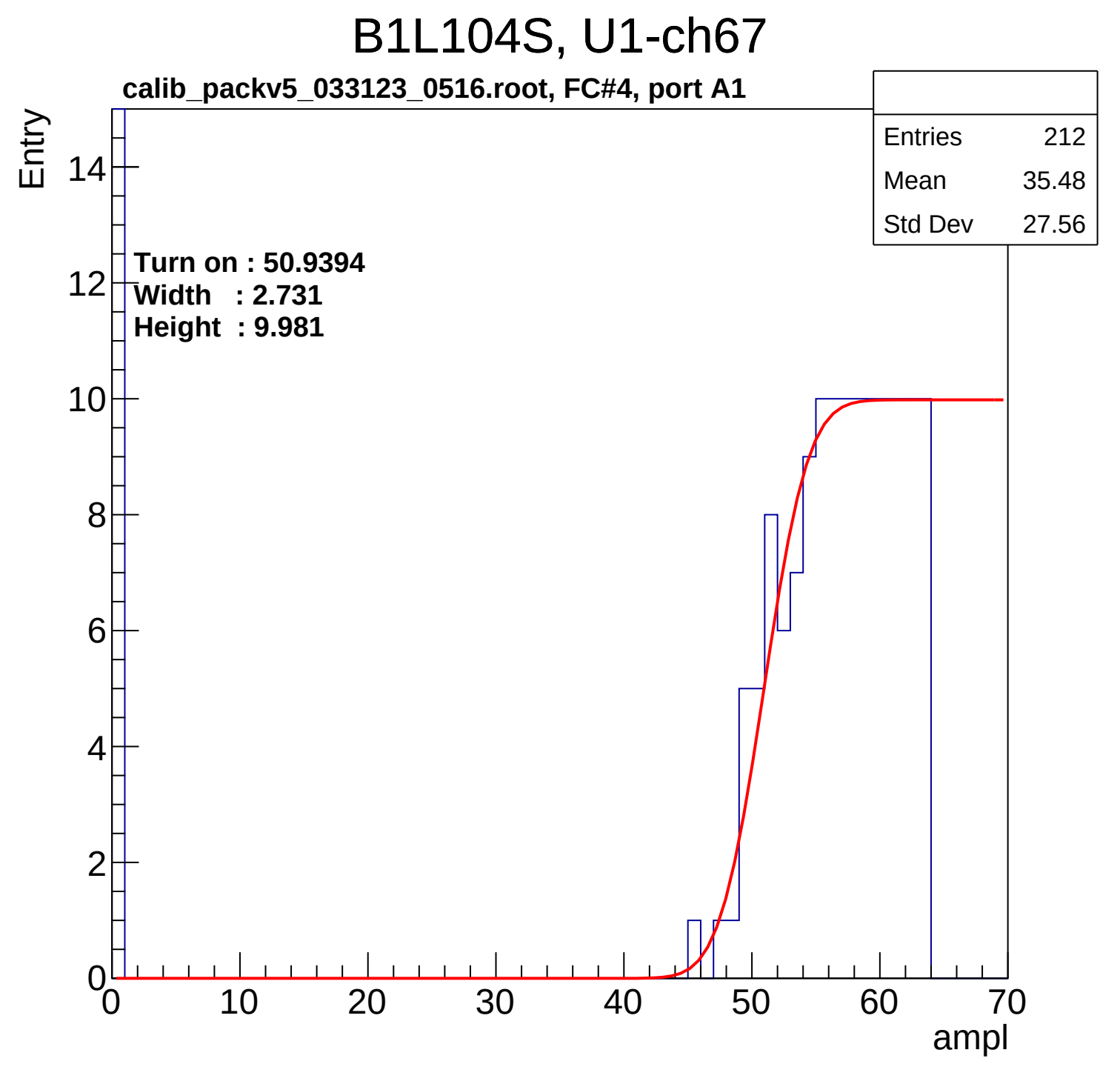

B1L104S, U1-ch62
calib_packv5_033123_0516.root, FC#4, port A1
Entries 208
Mean 31.18
Std Dev 28.72
Turn on : 52.1310
Width : 0.527
Height : 9.035
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

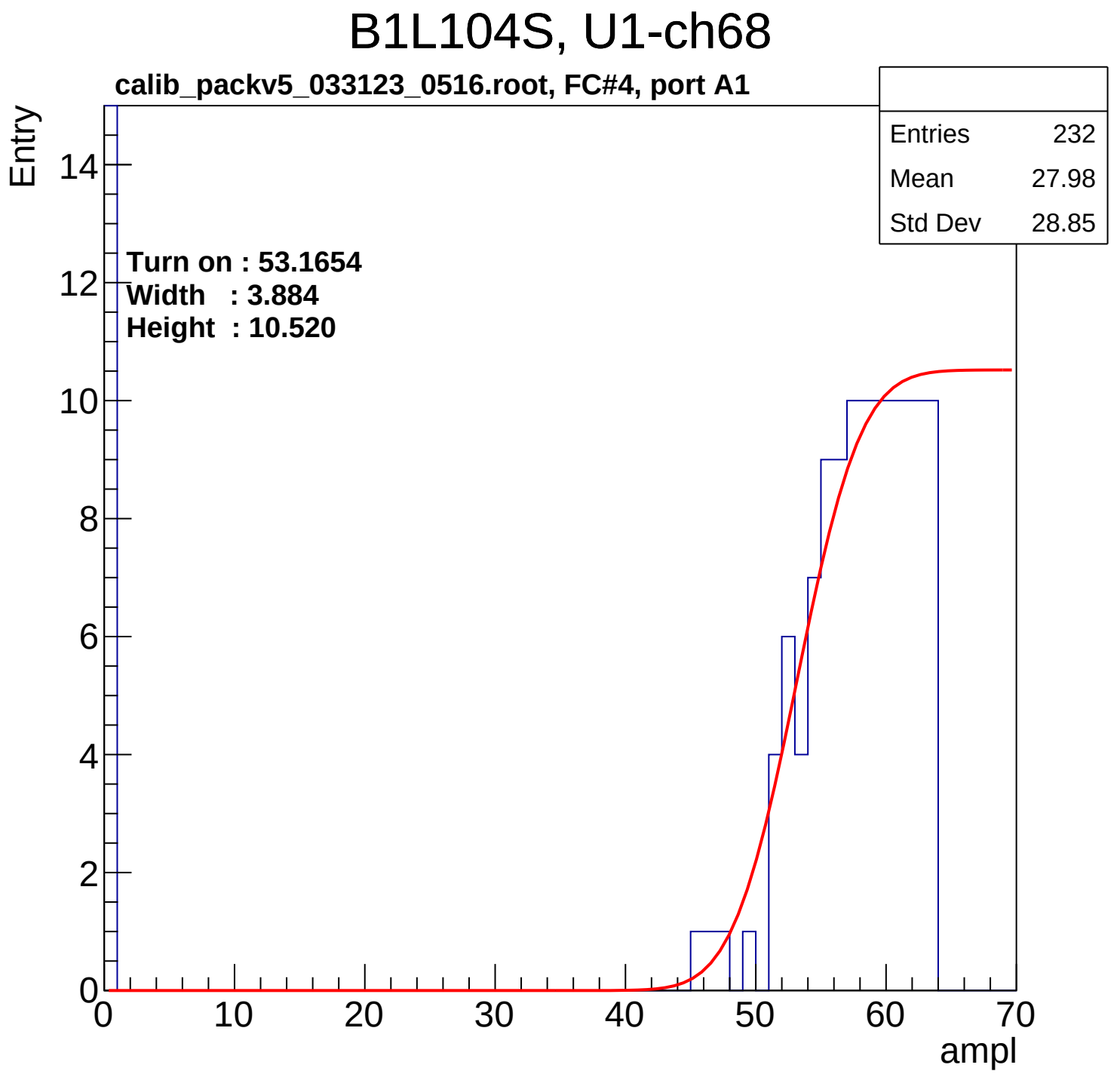

B1L104S, U1-ch63
calib_packv5_033123_0516.root, FC#4, port A1
Entries 184
Mean 34.24
Std Dev 28.53
Turn on : 53.3467
Width : 1.975
Height : 9.879
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

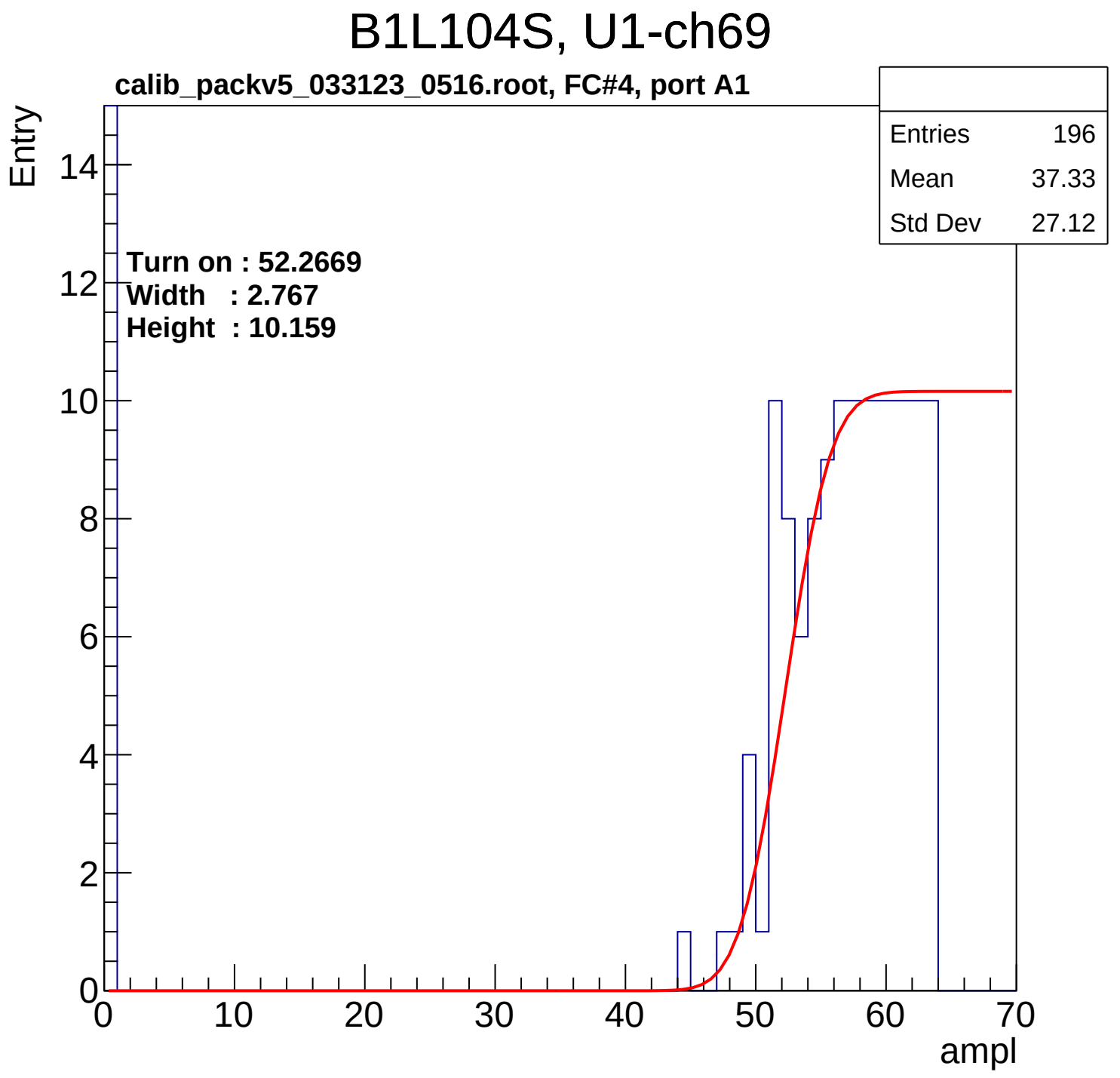

B1L104S, U1-ch64
calib_packv5_033123_0516.root, FC#4, port A1
Entries 222
Mean 34.26
Std Dev 27.73
Turn on : 50.8909
Width : 3.777
Height : 10.169
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

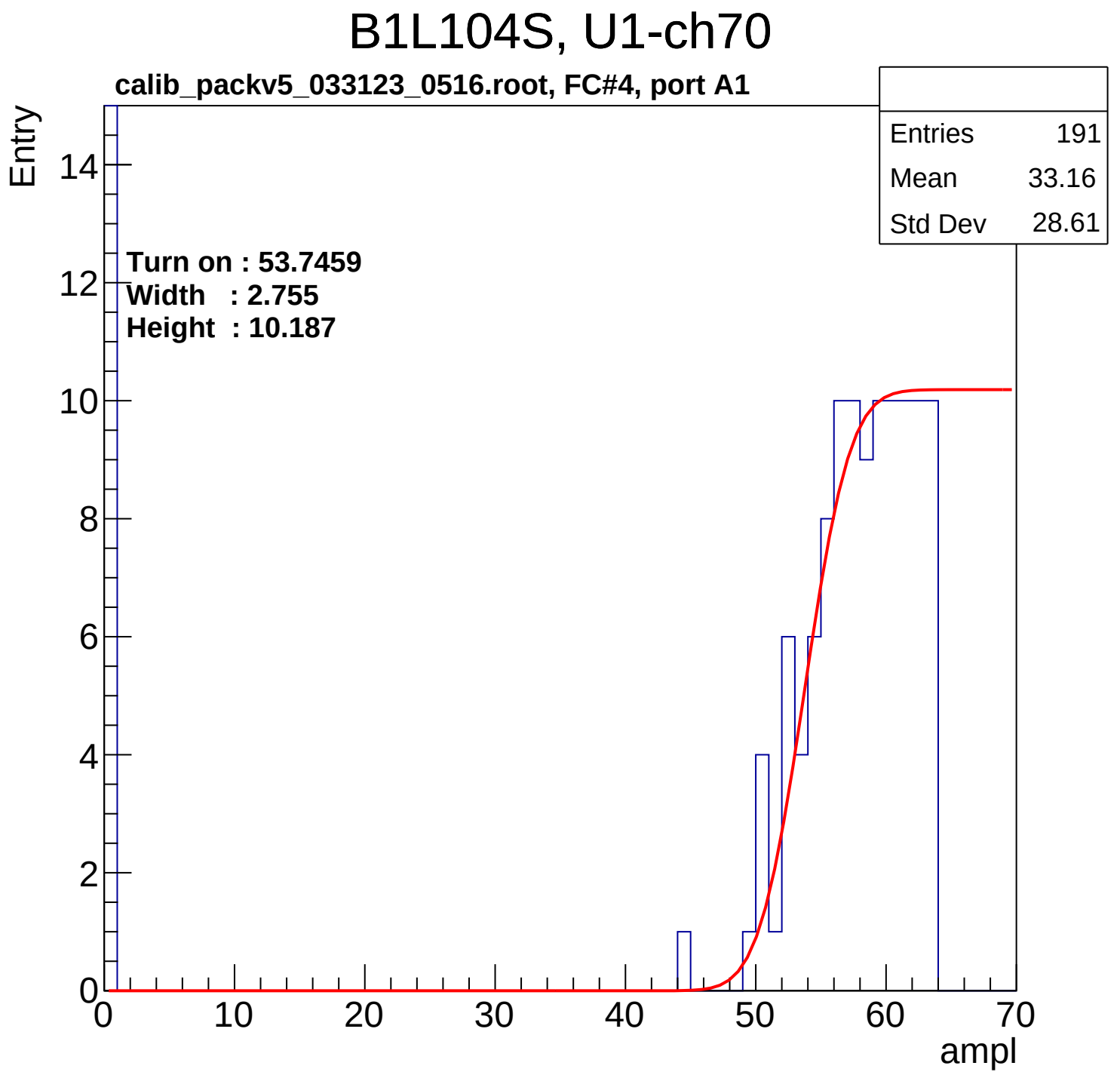

B1L104S, U1-ch65
calib_packv5_033123_0516.root, FC#4, port A1
Entries 206
Mean 29.02
Std Dev 29.13
Turn on : 53.4772
Width : 3.426
Height : 10.247
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

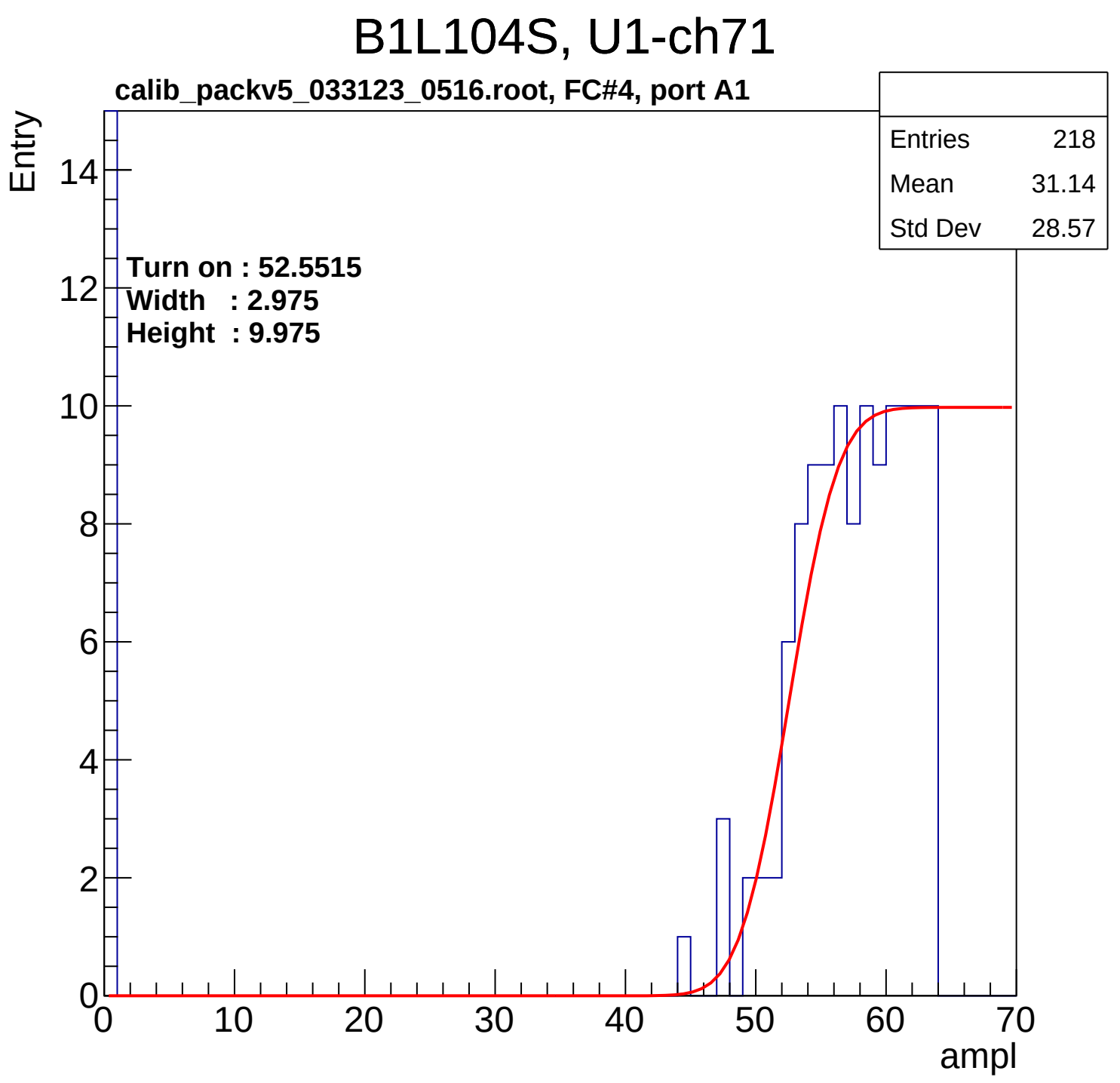

B1L104S, U1-ch66
calib_packv5_033123_0516.root, FC#4, port A1
Entries 207
Mean 31.97
Std Dev 28.72
Turn on : 52.2504
Width : 1.374
Height : 9.586
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

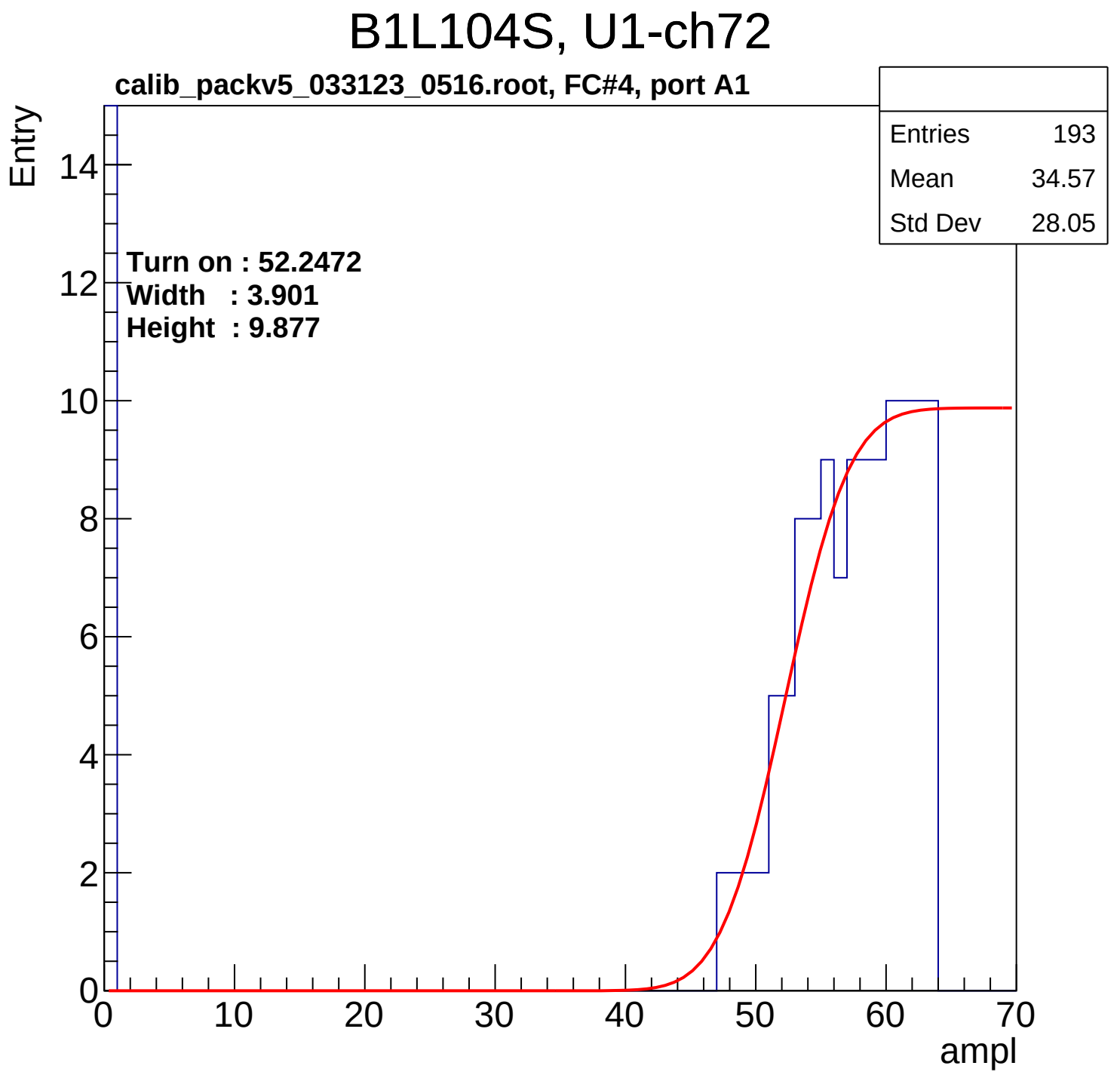

B1L104S, U1-ch67
calib_packv5_033123_0516.root, FC#4, port A1
Entries 212
Mean 35.48
Std Dev 27.56
Turn on : 50.9394
Width : 2.731
Height : 9.981
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

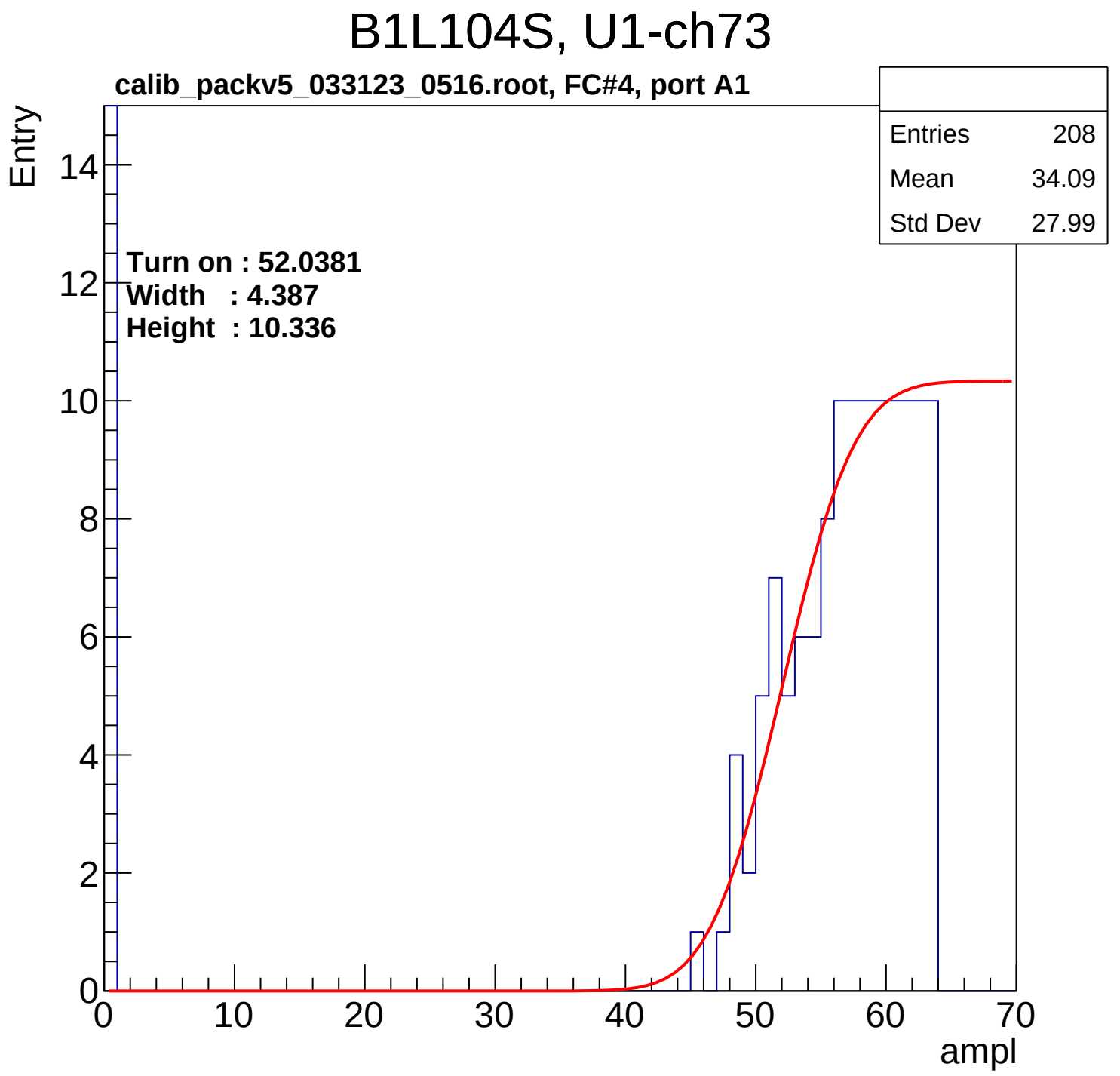

B1L104S, U1-ch68
calib_packv5_033123_0516.root, FC#4, port A1
Entries 232
Mean 27.98
Std Dev 28.85
Turn on : 53.1654
Width : 3.884
Height : 10.520
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

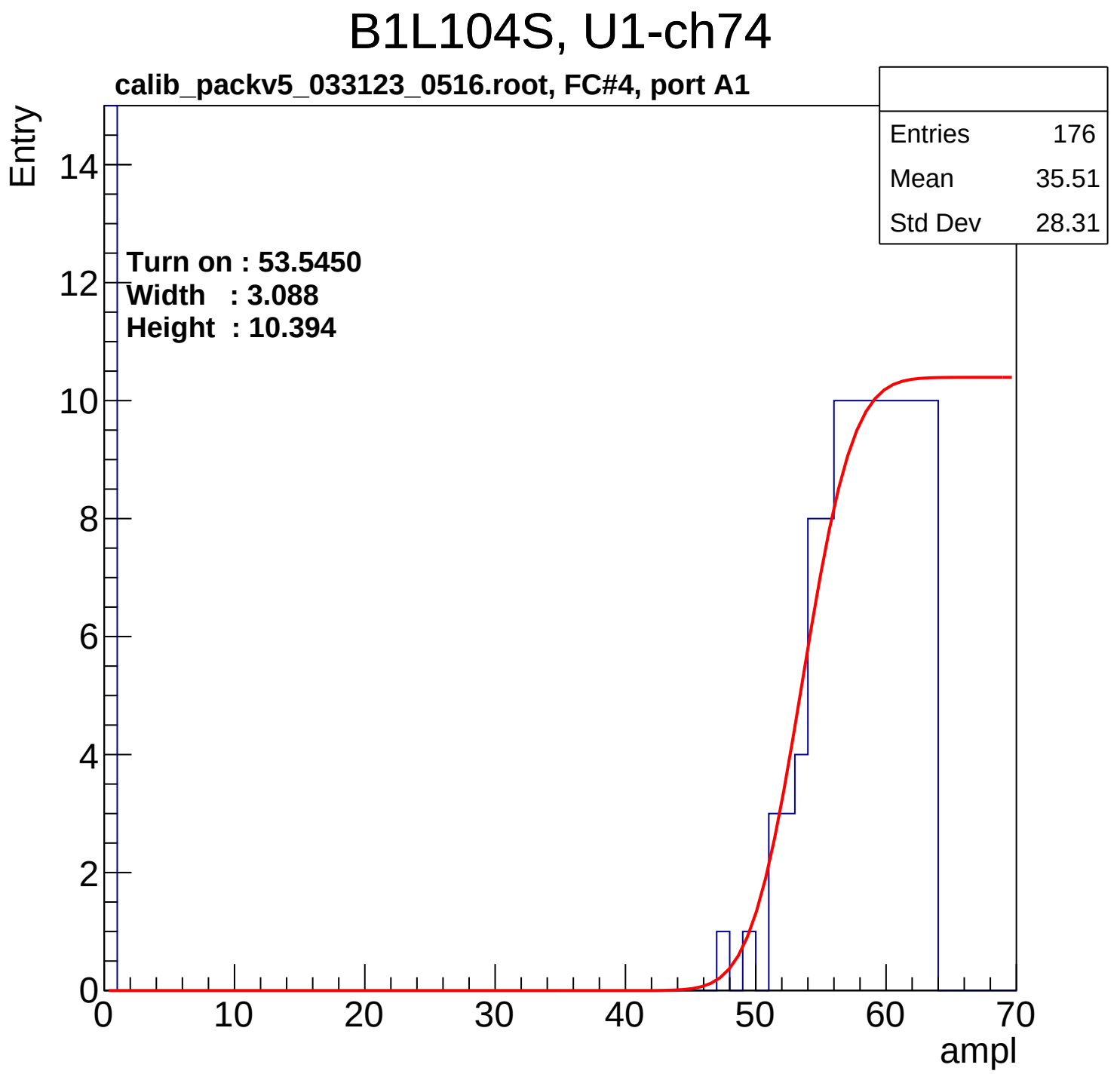

B1L104S, U1-ch69
calib_packv5_033123_0516.root, FC#4, port A1
Entries 196
Mean 37.33
Std Dev 27.12
Turn on : 52.2669
Width : 2.767
Height : 10.159
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

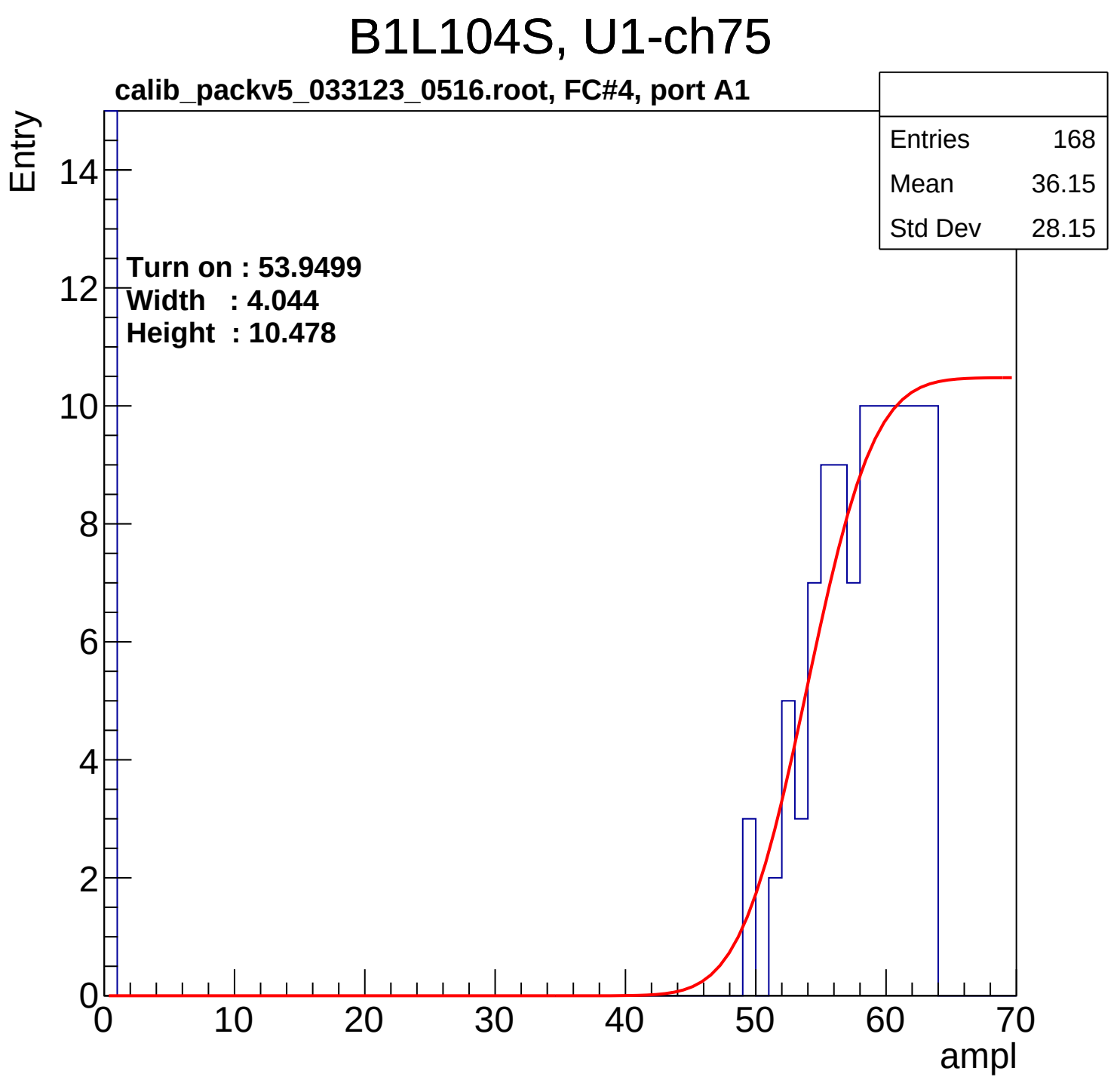

B1L104S, U1-ch70
calib_packv5_033123_0516.root, FC#4, port A1
Entries 191
Mean 33.16
Std Dev 28.61
Turn on : 53.7459
Width : 2.755
Height : 10.187
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

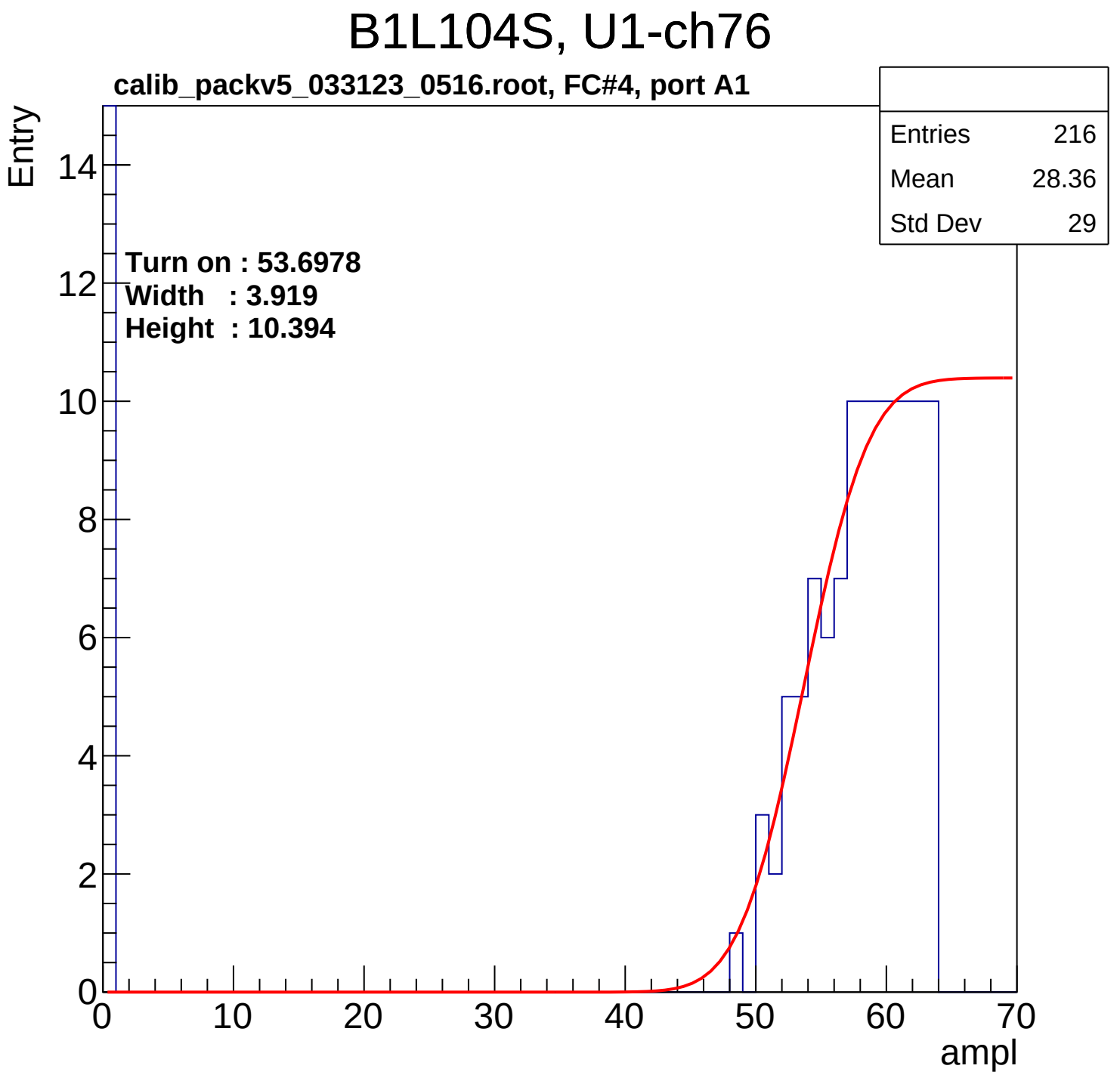

B1L104S, U1-ch71
calib_packv5_033123_0516.root, FC#4, port A1
Entries 218
Mean 31.14
Std Dev 28.57
Turn on : 52.5515
Width : 2.975
Height : 9.975
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

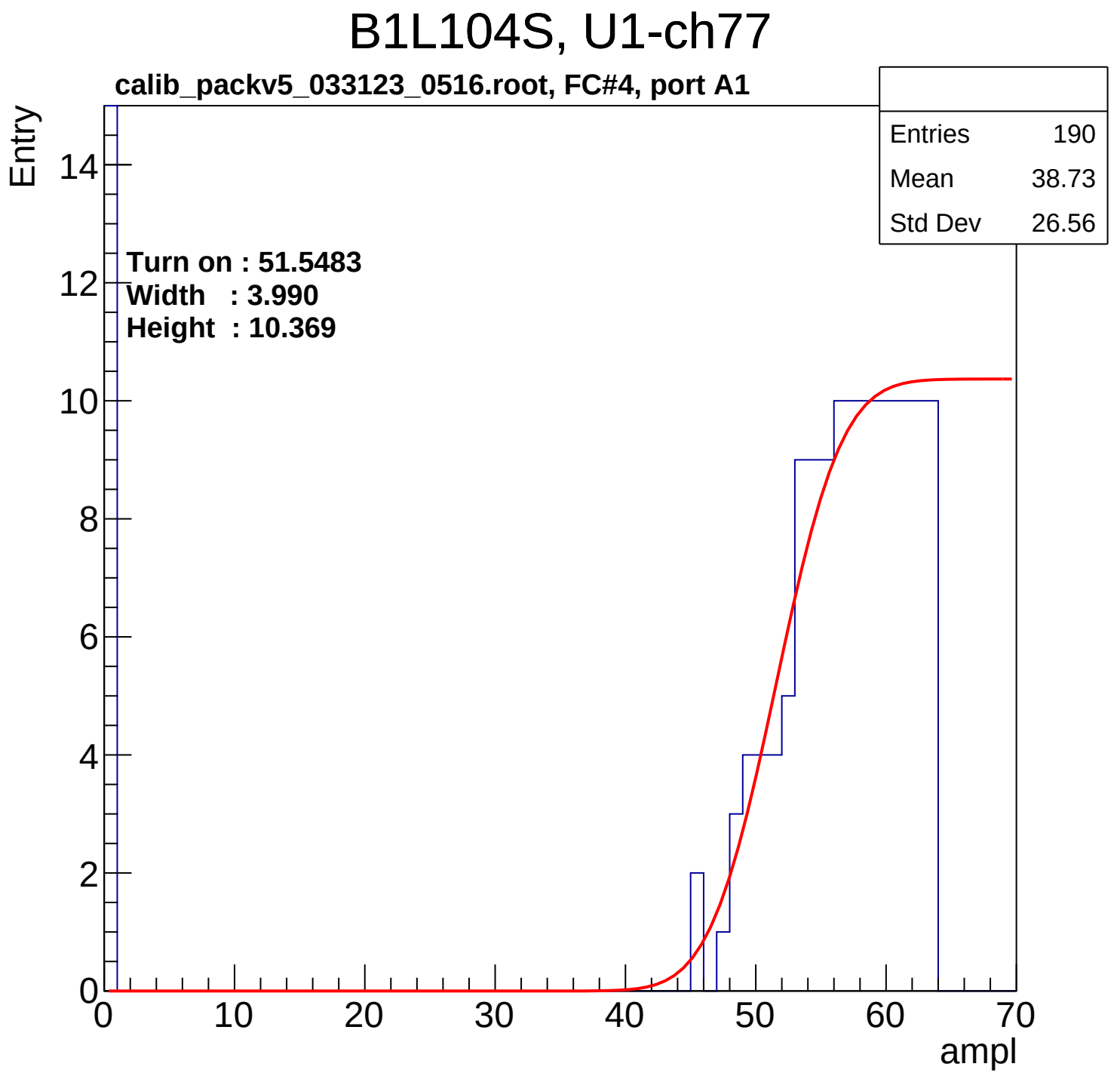

B1L104S, U1-ch72
calib_packv5_033123_0516.root, FC#4, port A1
Entries 193
Mean 34.57
Std Dev 28.05
Turn on : 52.2472
Width : 3.901
Height : 9.877
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

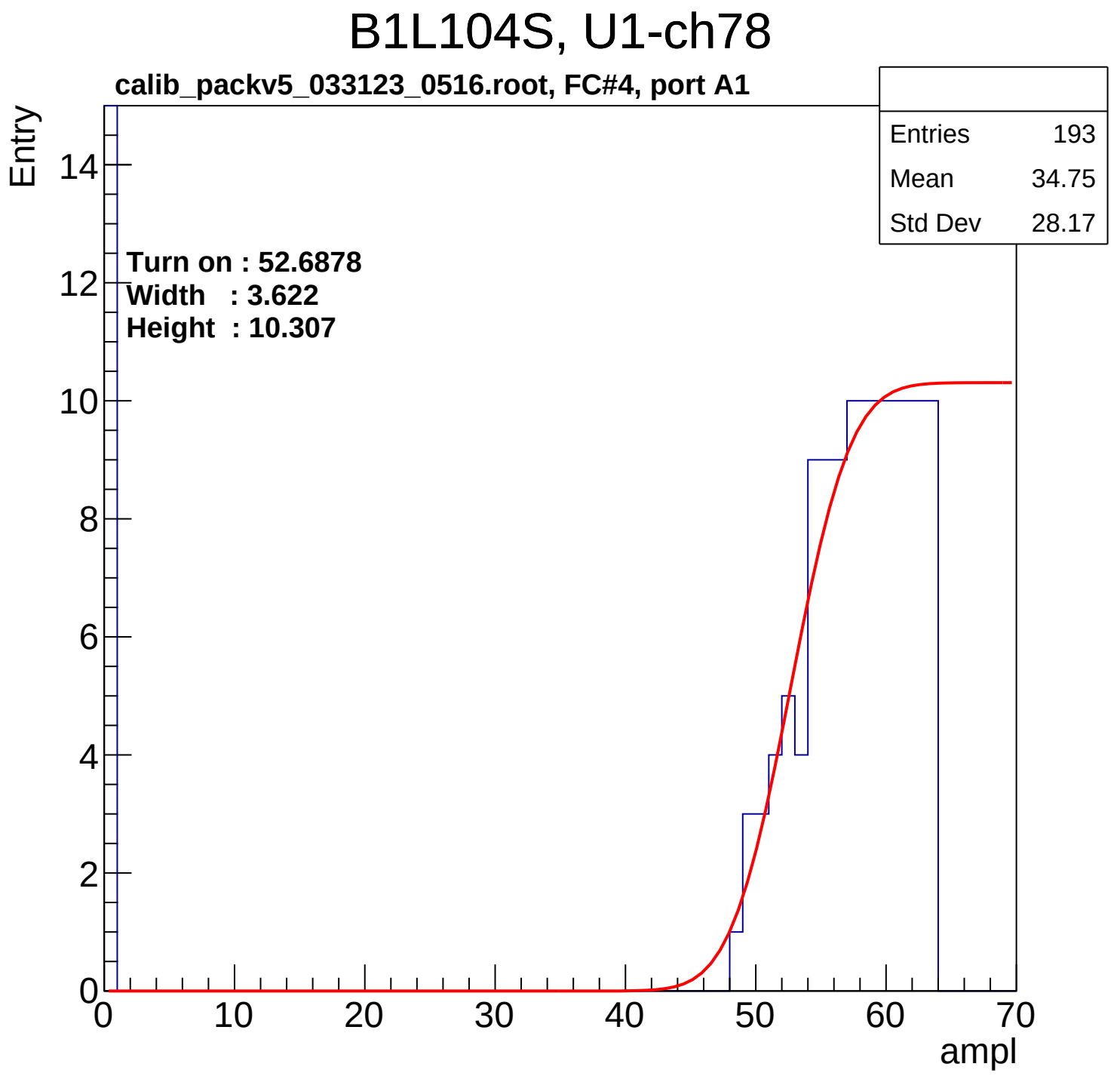

B1L104S, U1-ch73
calib_packv5_033123_0516.root, FC#4, port A1
Entries 208
Mean 34.09
Std Dev 27.99
Turn on : 52.0381
Width : 4.387
Height : 10.336
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

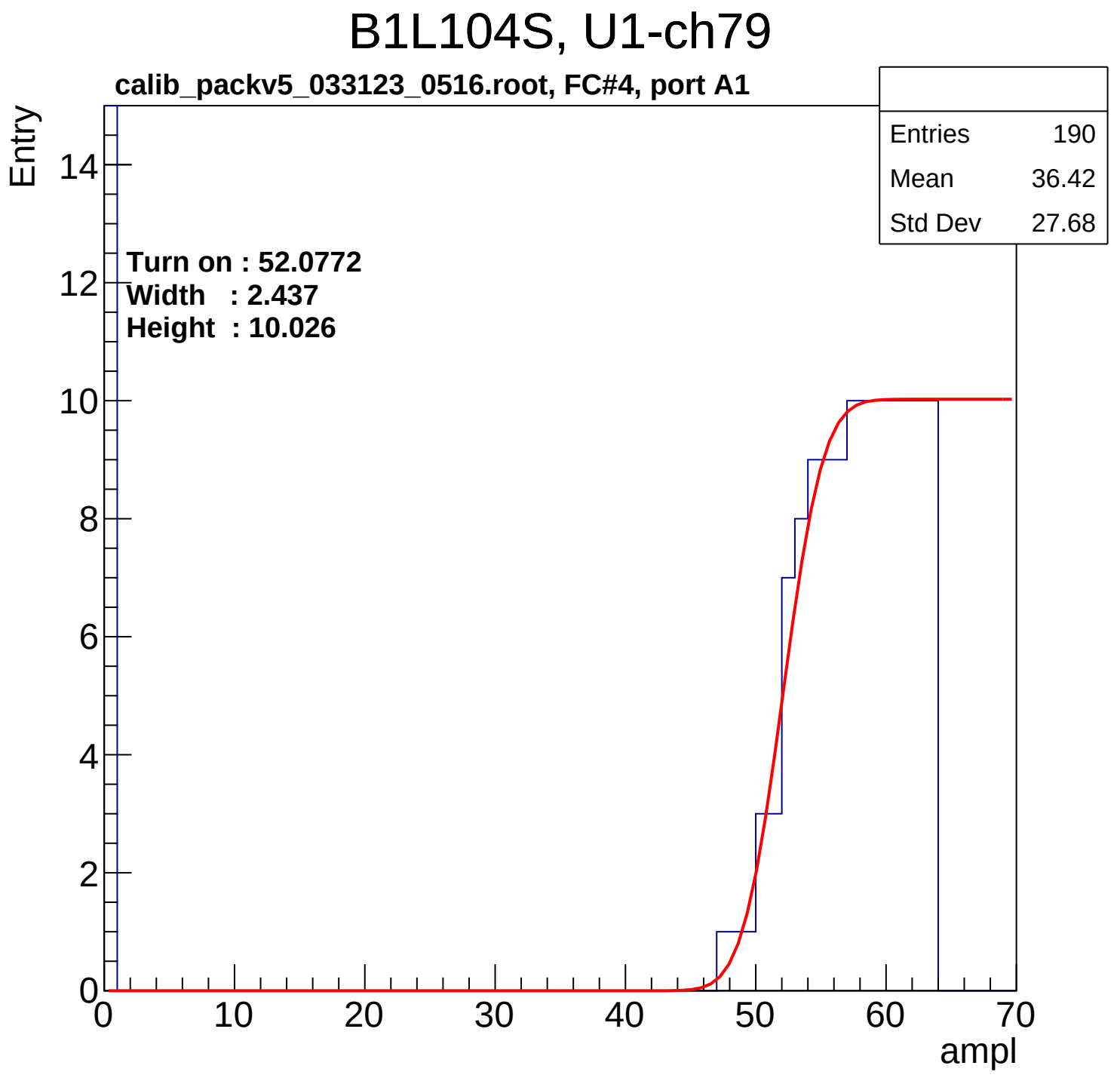

B1L104S, U1-ch74
calib_packv5_033123_0516.root, FC#4, port A1
Entries 176
Mean 35.51
Std Dev 28.31
Turn on : 53.5450
Width : 3.088
Height : 10.394
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

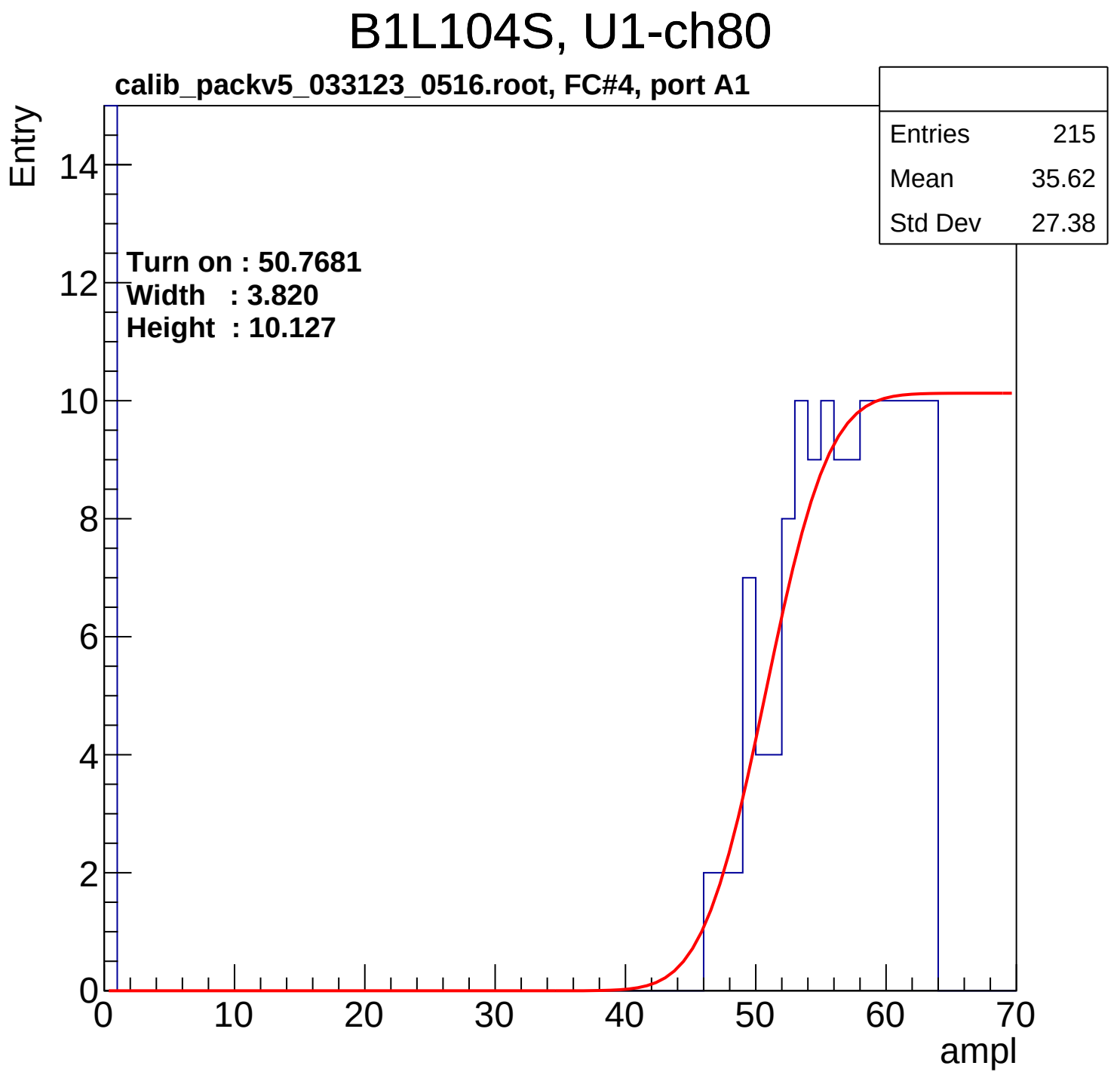

B1L104S, U1-ch75
calib_packv5_033123_0516.root, FC#4, port A1
Entries 168
Mean 36.15
Std Dev 28.15
Turn on : 53.9499
Width : 4.044
Height : 10.478
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

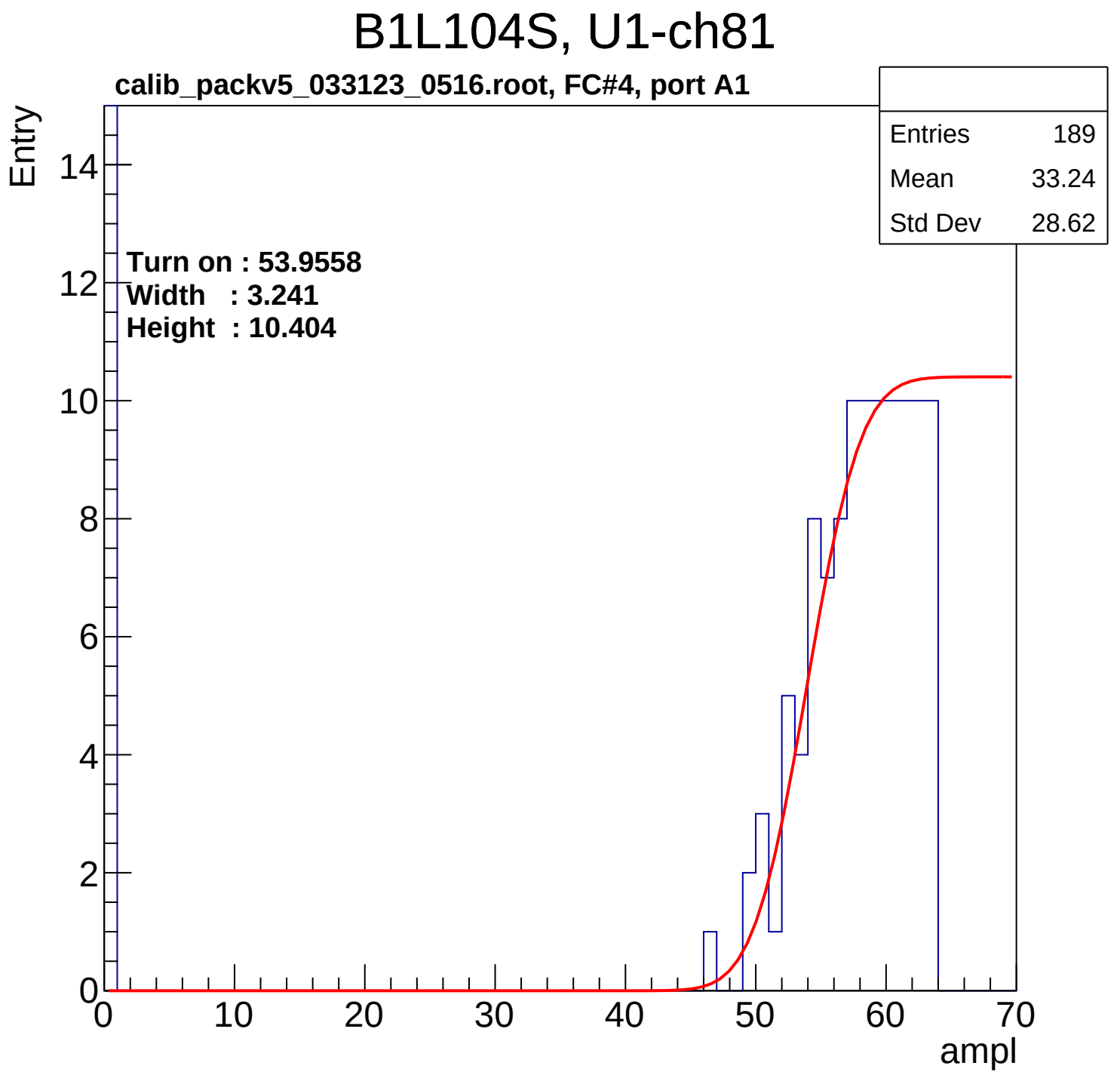

B1L104S, U1-ch76
calib_packv5_033123_0516.root, FC#4, port A1
Entries 216
Mean 28.36
Std Dev 29
Turn on : 53.6978
Width : 3.919
Height : 10.394
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

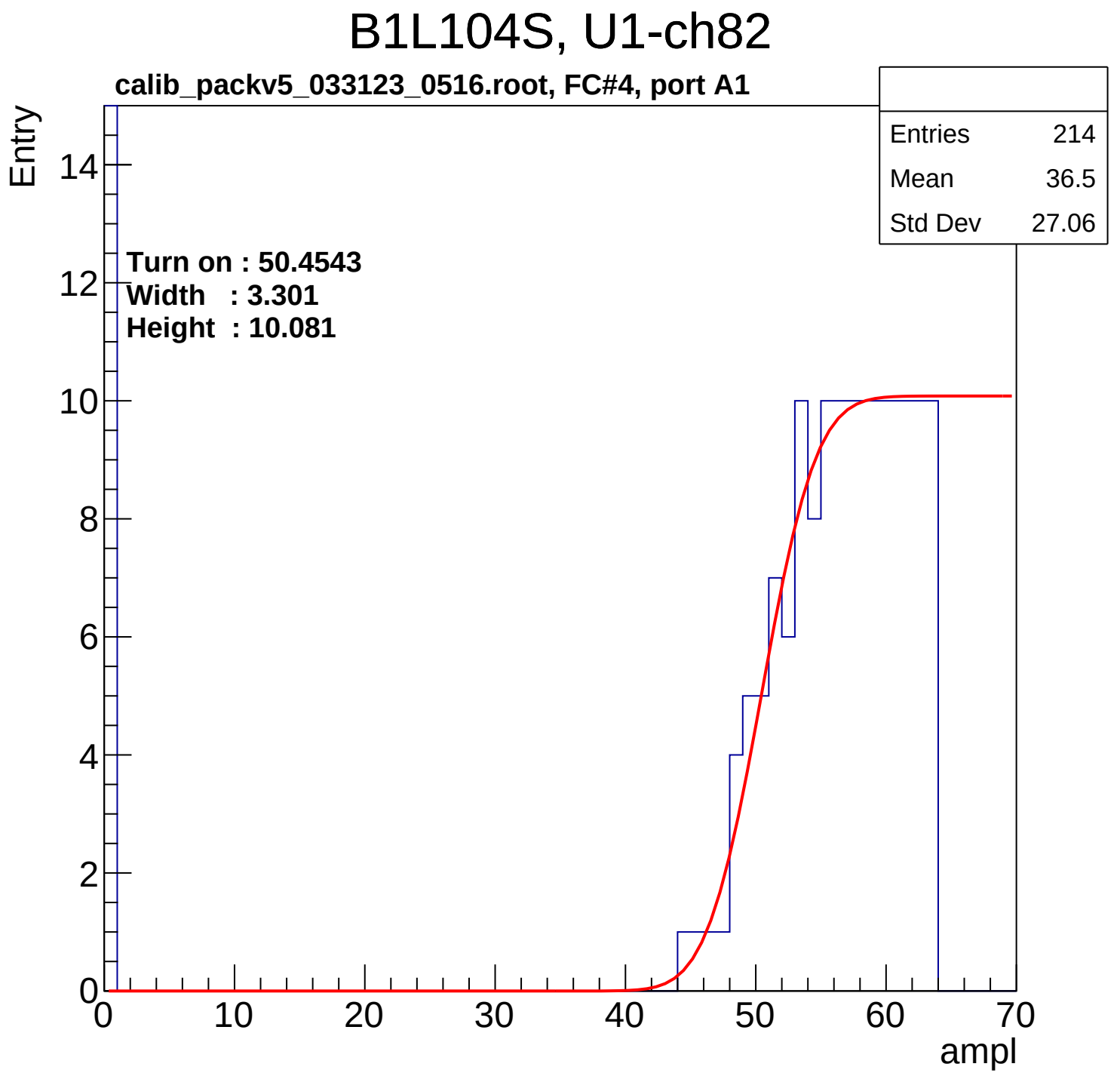

B1L104S, U1-ch77
calib_packv5_033123_0516.root, FC#4, port A1
Entries 190
Mean 38.73
Std Dev 26.56
Turn on : 51.5483
Width : 3.990
Height : 10.369
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

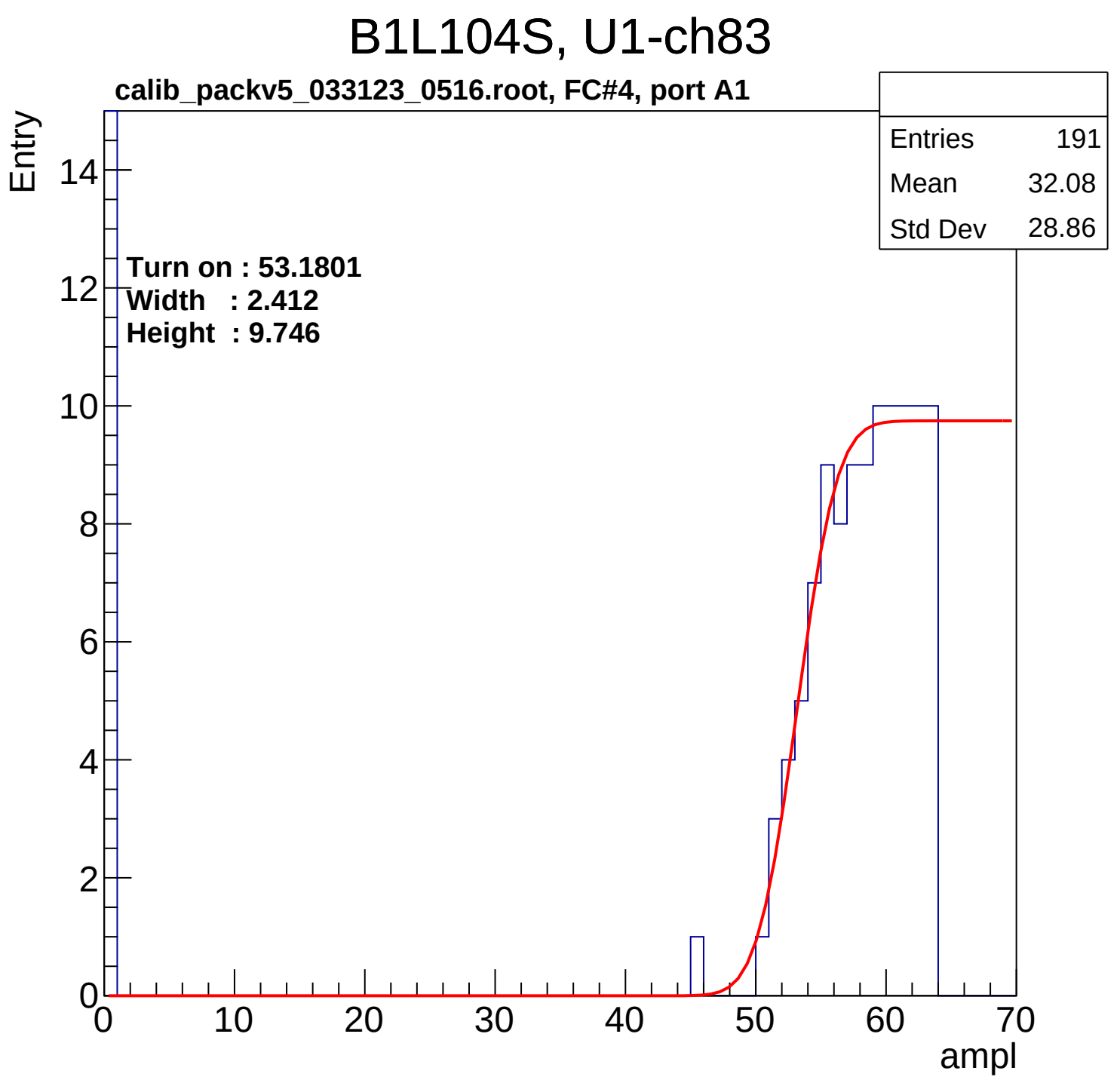

B1L104S, U1-ch78
calib_packv5_033123_0516.root, FC#4, port A1
Entries 193
Mean 34.75
Std Dev 28.17
Turn on : 52.6878
Width : 3.622
Height : 10.307
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

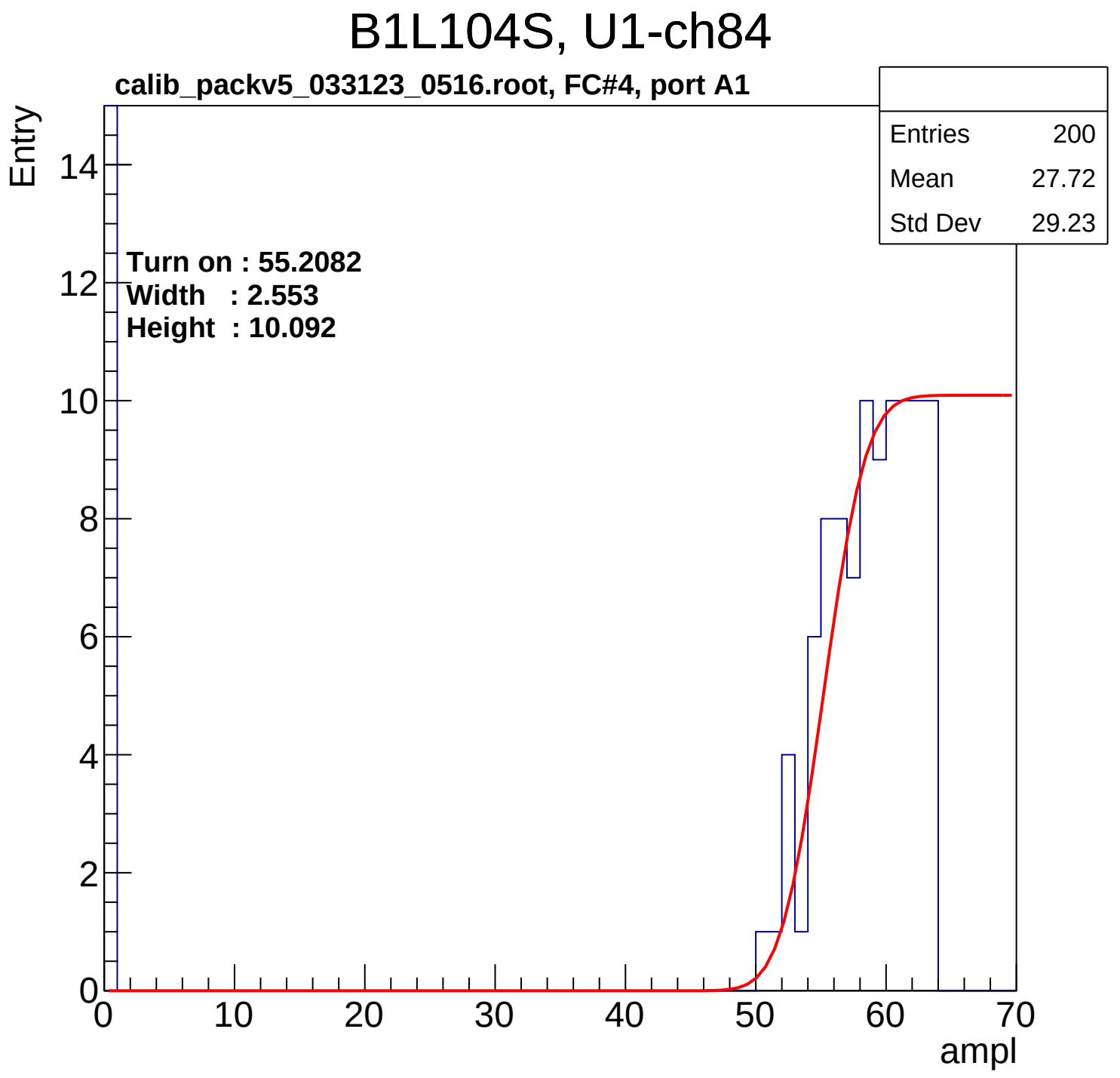

B1L104S, U1-ch79
calib_packv5_033123_0516.root, FC#4, port A1
Entries 190
Mean 36.42
Std Dev 27.68
Turn on : 52.0772
Width : 2.437
Height : 10.026
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

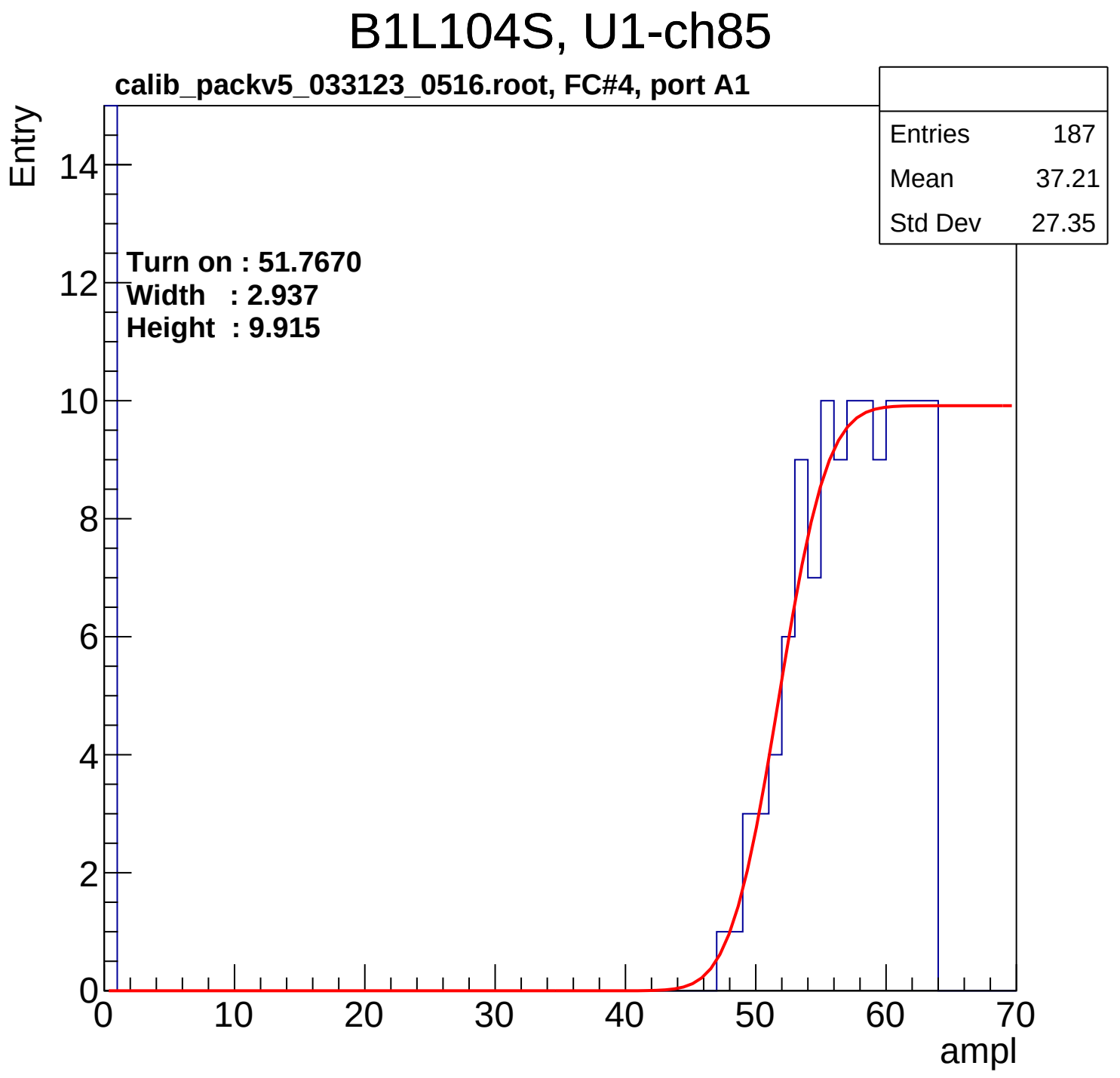

B1L104S, U1-ch80
calib_packv5_033123_0516.root, FC#4, port A1
Entries 215
Mean 35.62
Std Dev 27.38
Turn on : 50.7681
Width : 3.820
Height : 10.127
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

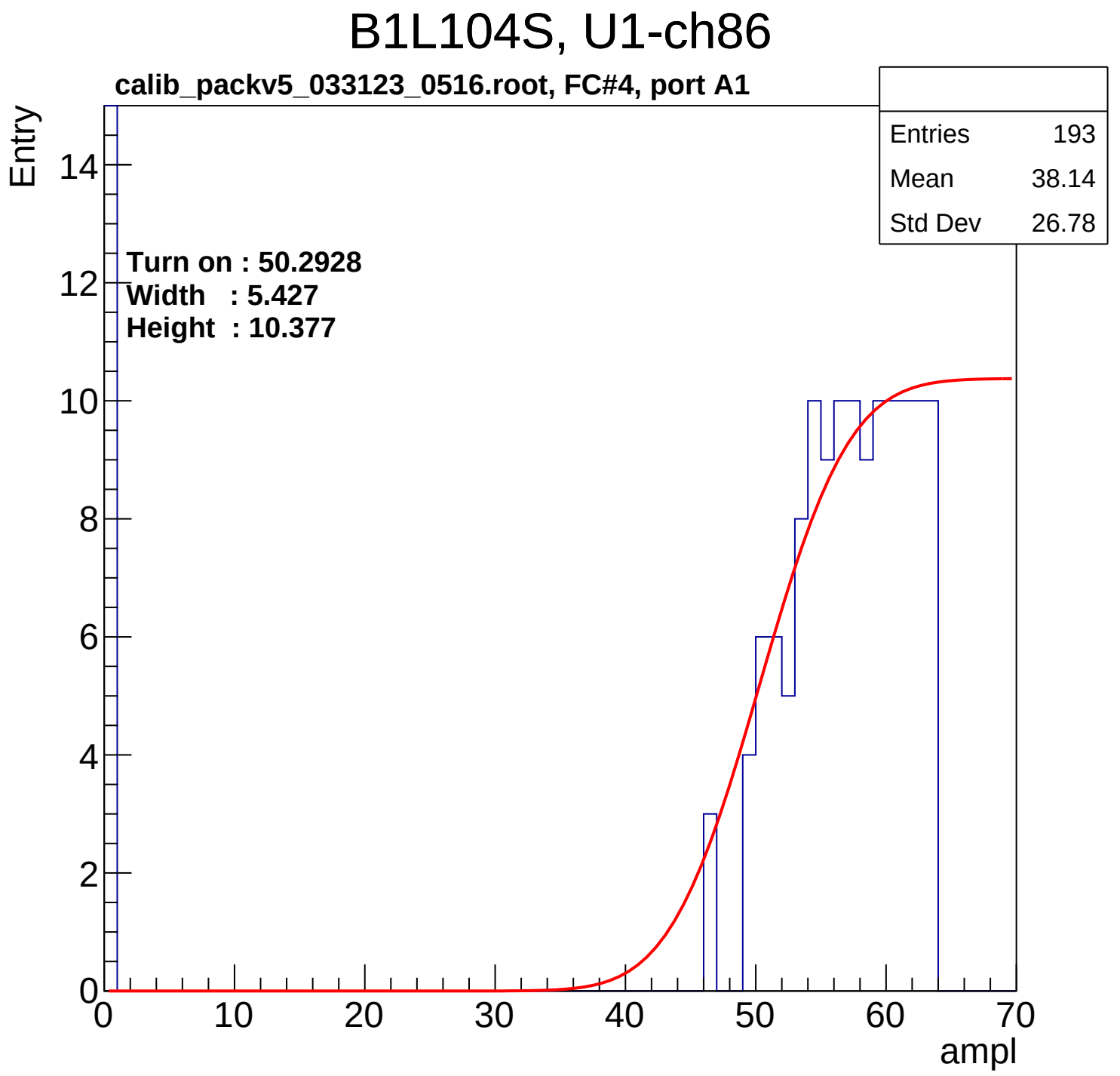

B1L104S, U1-ch81
calib_packv5_033123_0516.root, FC#4, port A1
Entries 189
Mean 33.24
Std Dev 28.62
Turn on : 53.9558
Width : 3.241
Height : 10.404
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

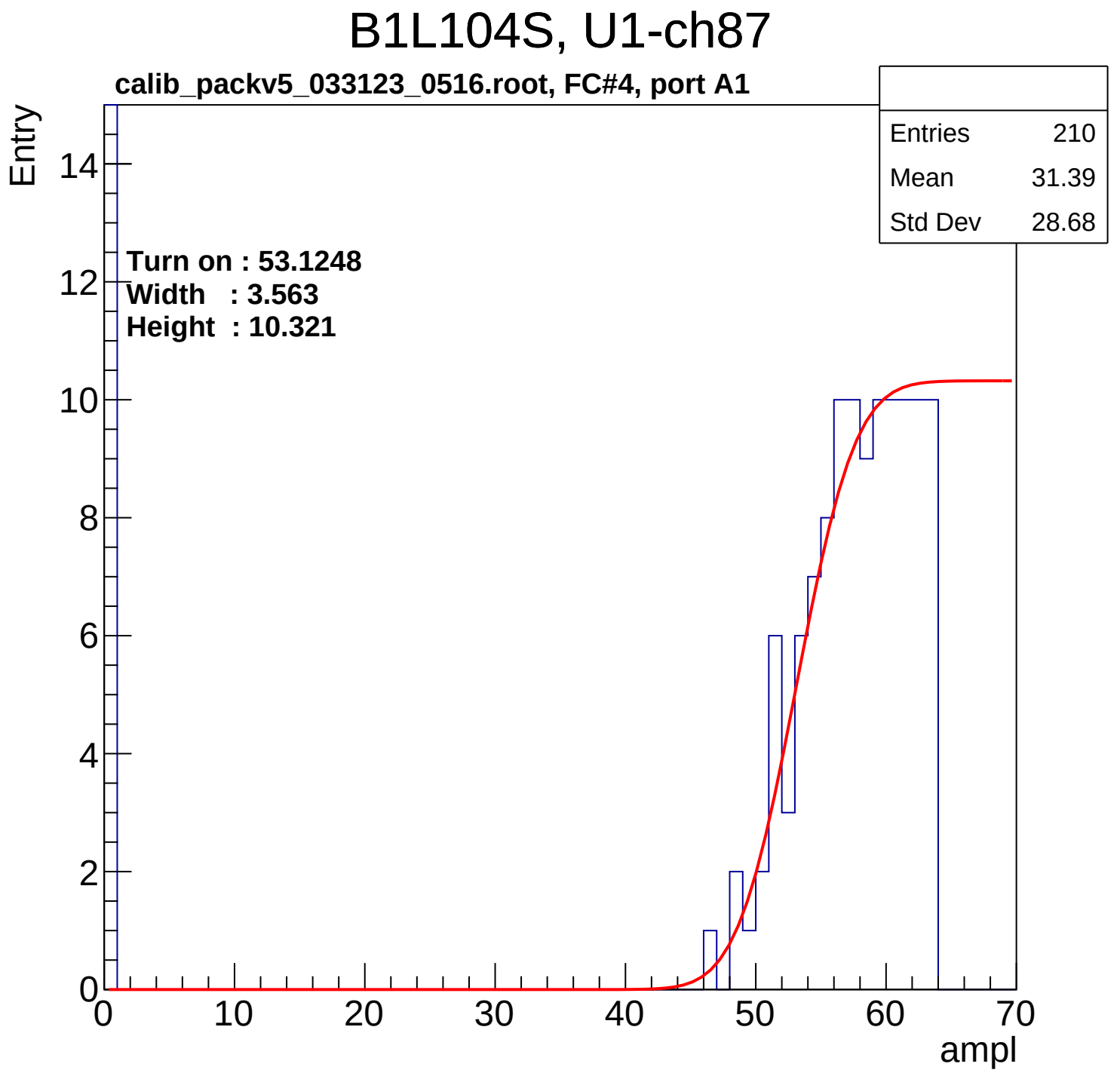

B1L104S, U1-ch82
calib_packv5_033123_0516.root, FC#4, port A1
Entries 214
Mean 36.5
Std Dev 27.06
Turn on : 50.4543
Width : 3.301
Height : 10.081
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

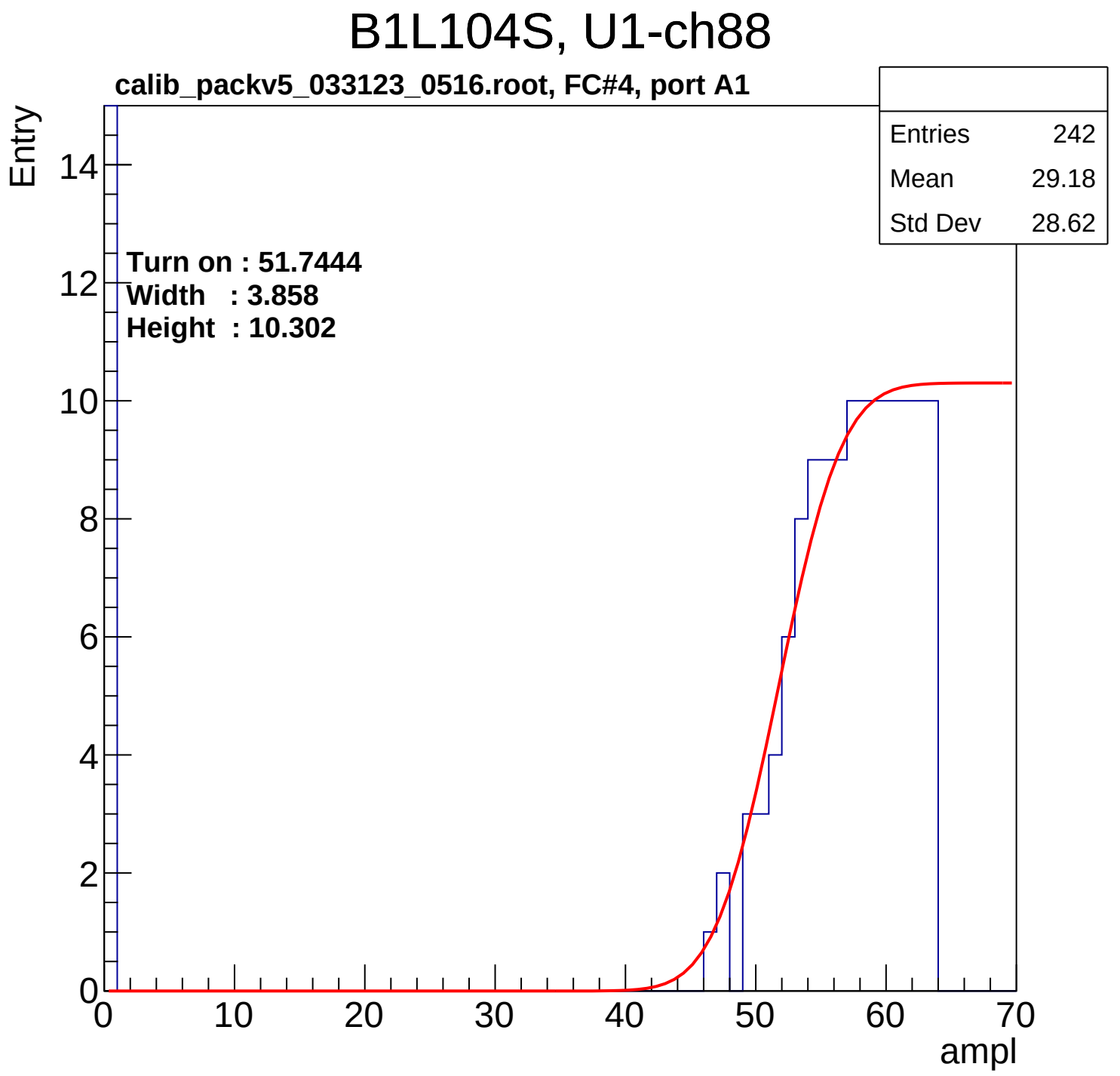

B1L104S, U1-ch83
calib_packv5_033123_0516.root, FC#4, port A1
Entries 191
Mean 32.08
Std Dev 28.86
Turn on : 53.1801
Width : 2.412
Height : 9.746
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

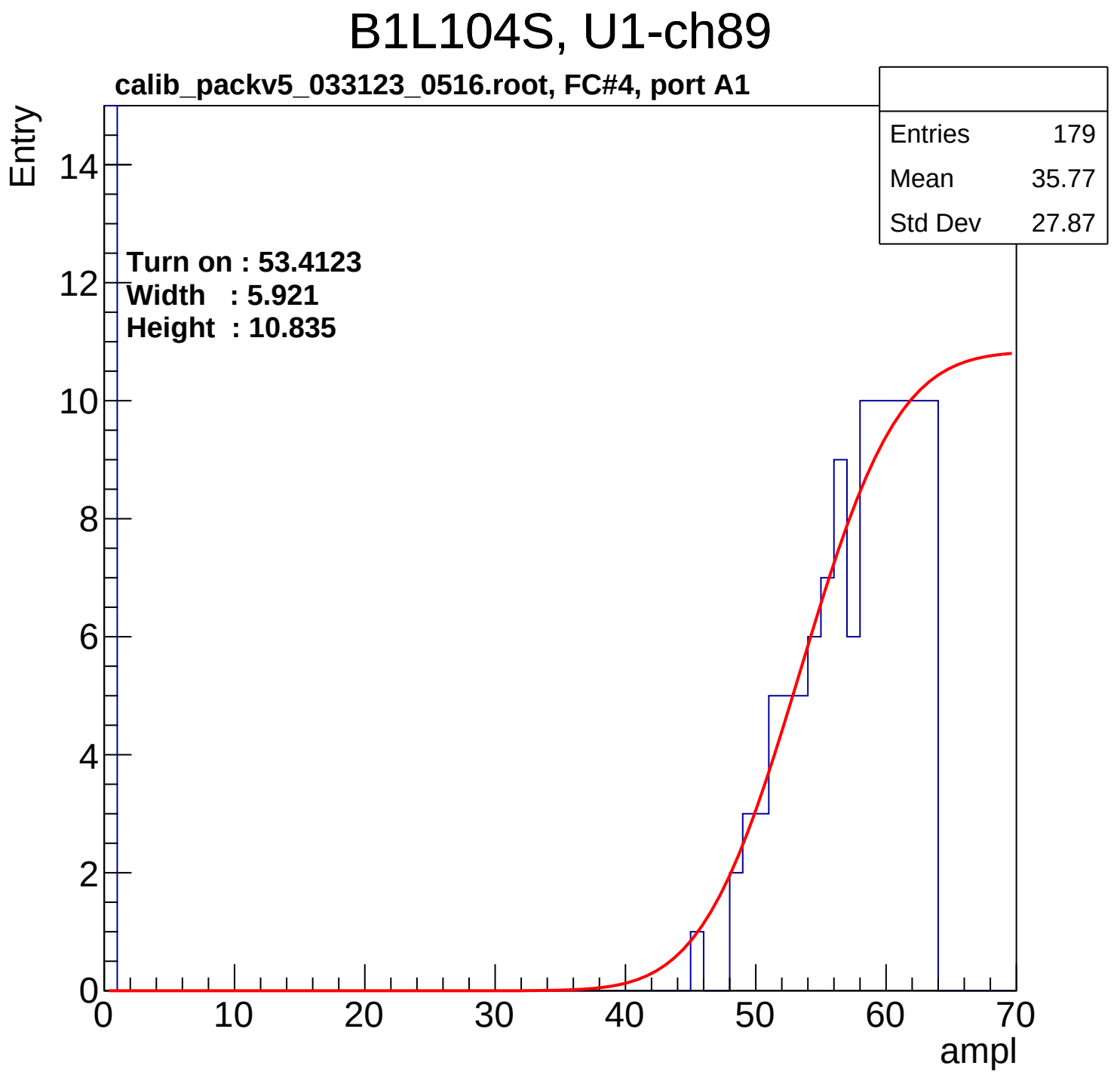

B1L104S, U1-ch84
calib_packv5_033123_0516.root, FC#4, port A1
Entries 200
Mean 27.72
Std Dev 29.23
Turn on : 55.2082
Width : 2.553
Height : 10.092
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

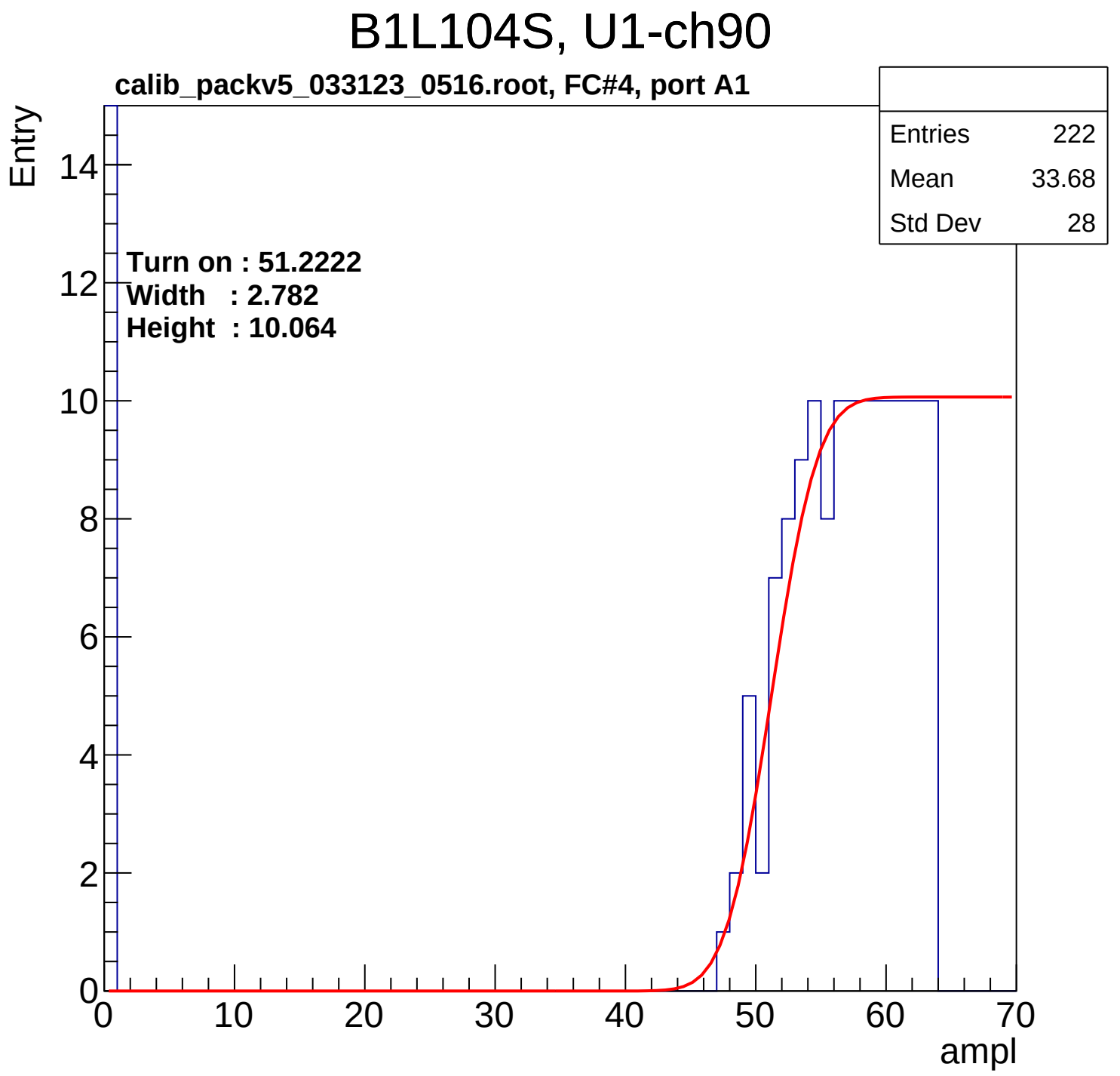

B1L104S, U1-ch85
calib_packv5_033123_0516.root, FC#4, port A1
Entries 187
Mean 37.21
Std Dev 27.35
Turn on : 51.7670
Width : 2.937
Height : 9.915
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

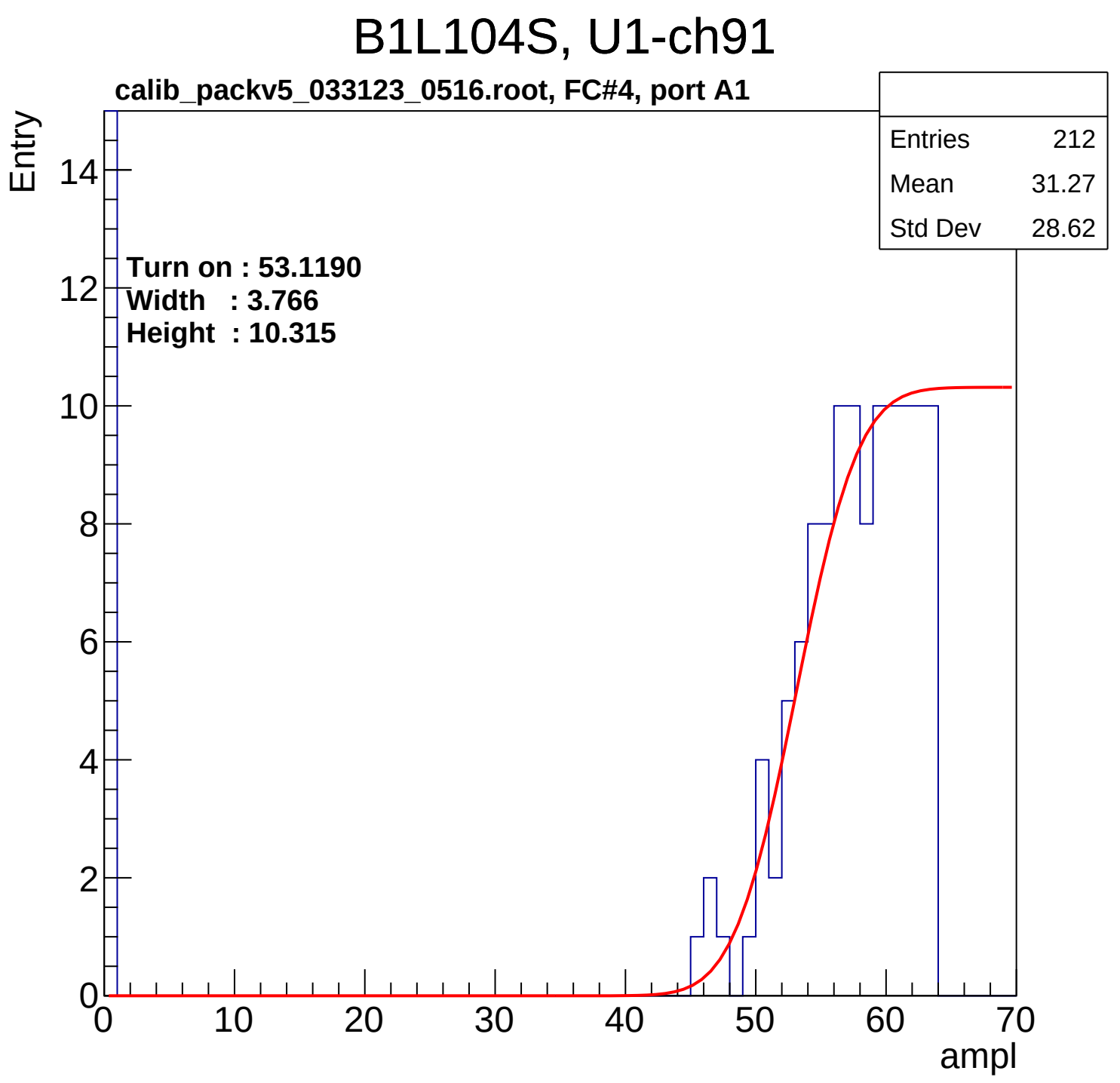

B1L104S, U1-ch86
calib_packv5_033123_0516.root, FC#4, port A1
Entries 193
Mean 38.14
Std Dev 26.78
Turn on : 50.2928
Width : 5.427
Height : 10.377
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

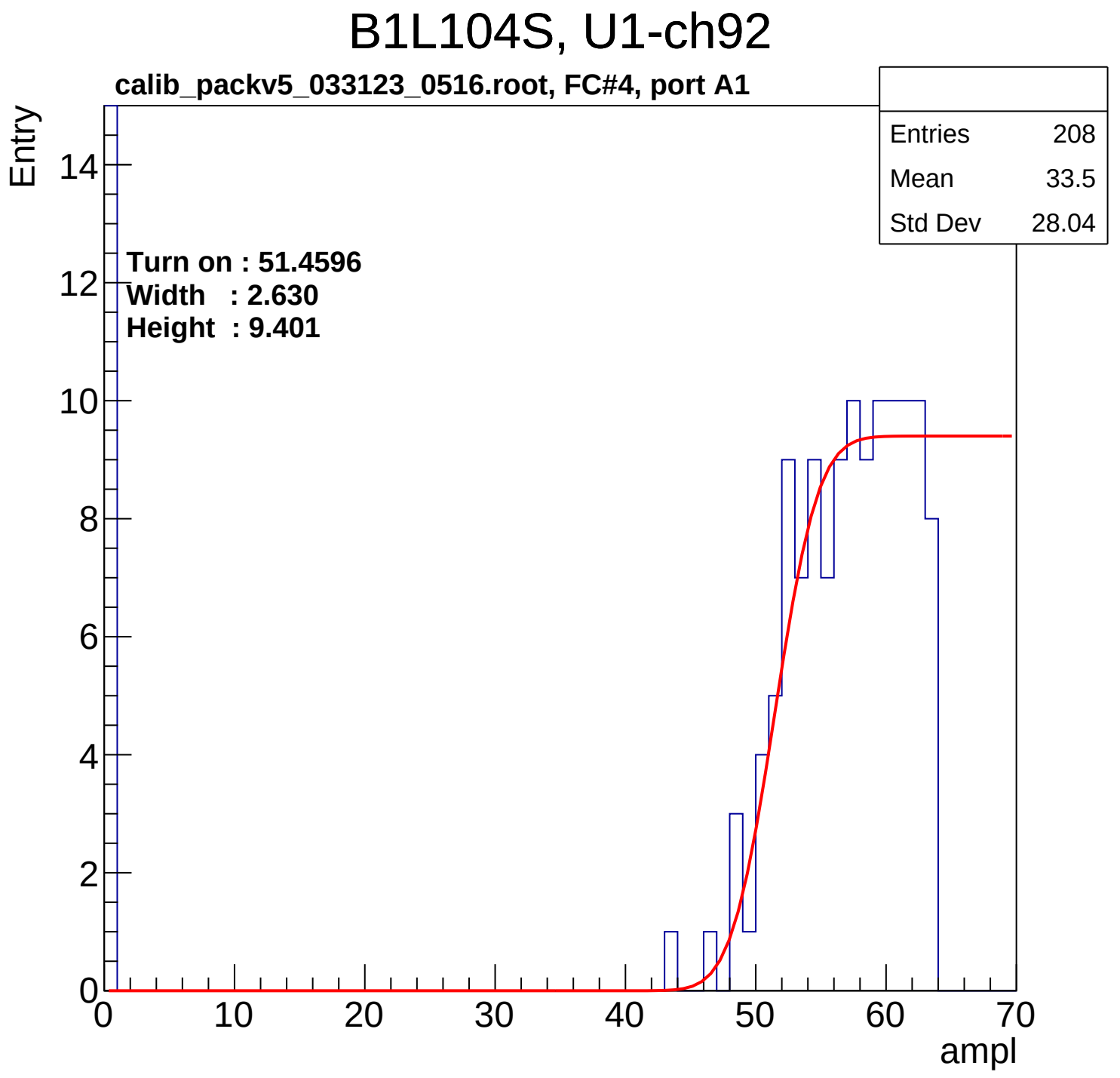

B1L104S, U1-ch87
calib_packv5_033123_0516.root, FC#4, port A1
Entries 210
Mean 31.39
Std Dev 28.68
Turn on : 53.1248
Width : 3.563
Height : 10.321
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

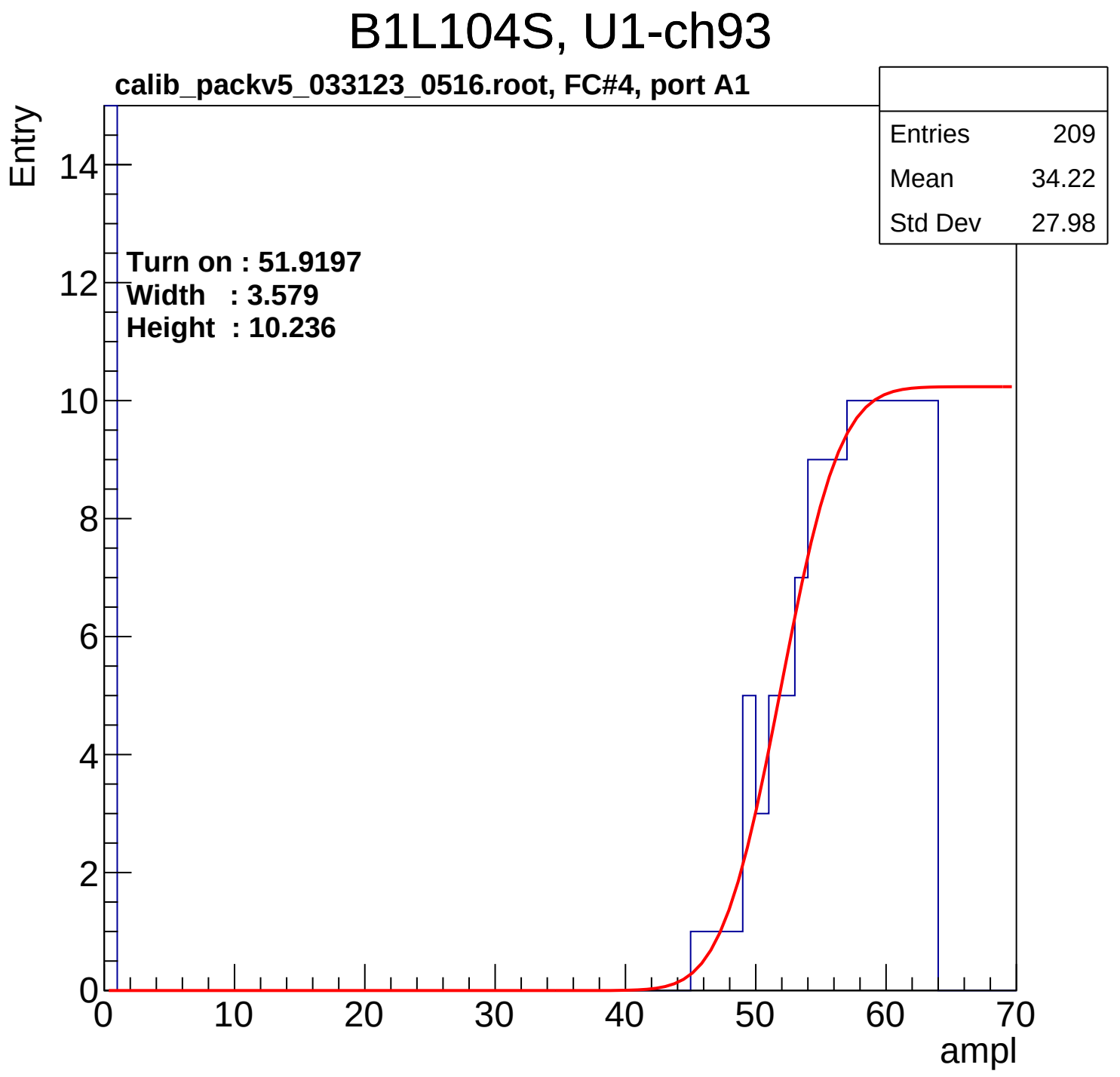

B1L104S, U1-ch88
calib_packv5_033123_0516.root, FC#4, port A1
Entries 242
Mean 29.18
Std Dev 28.62
Turn on : 51.7444
Width : 3.858
Height : 10.302
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

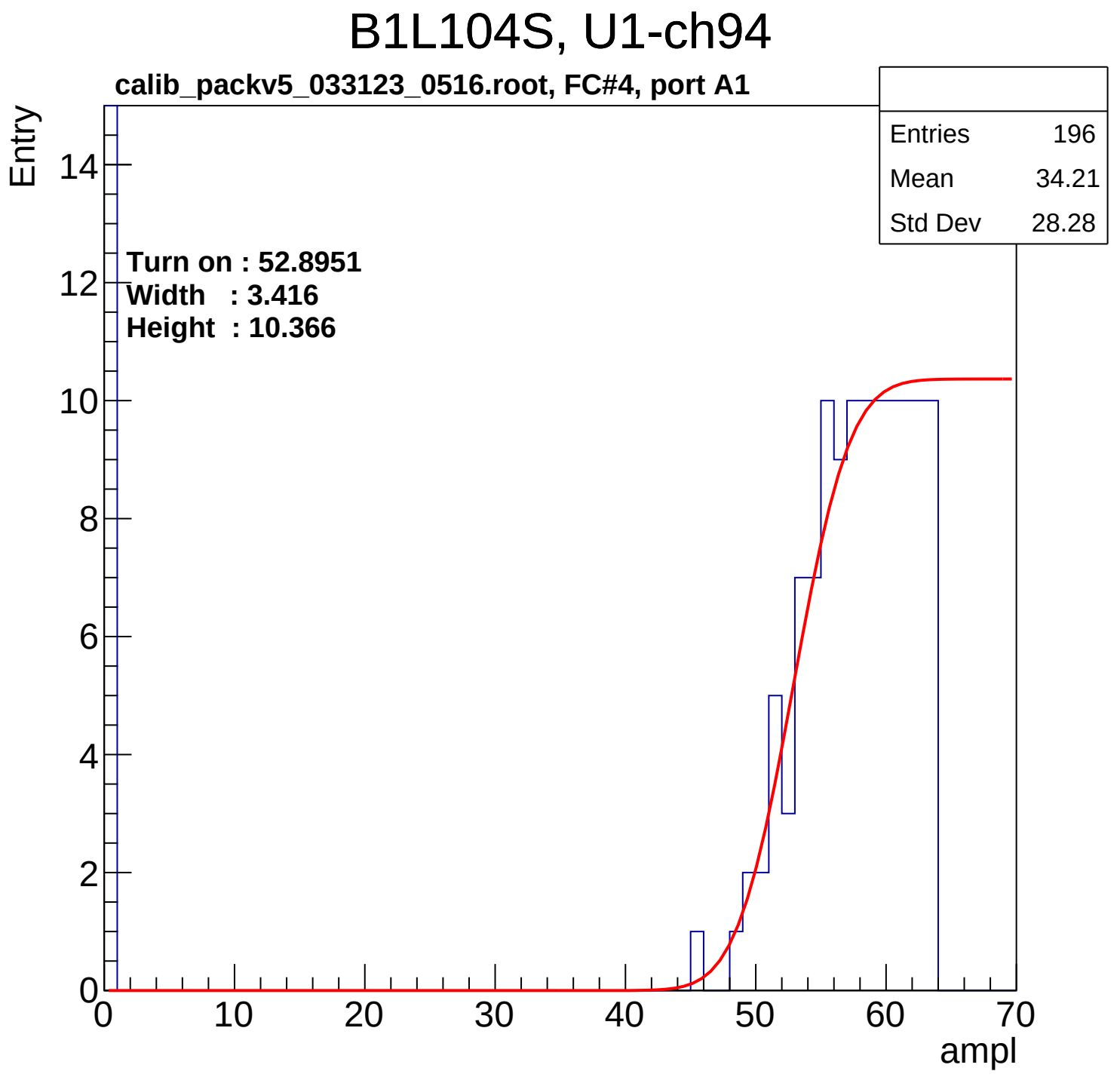

B1L104S, U1-ch89
calib_packv5_033123_0516.root, FC#4, port A1
Entries 179
Mean 35.77
Std Dev 27.87
Turn on : 53.4123
Width : 5.921
Height : 10.835
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

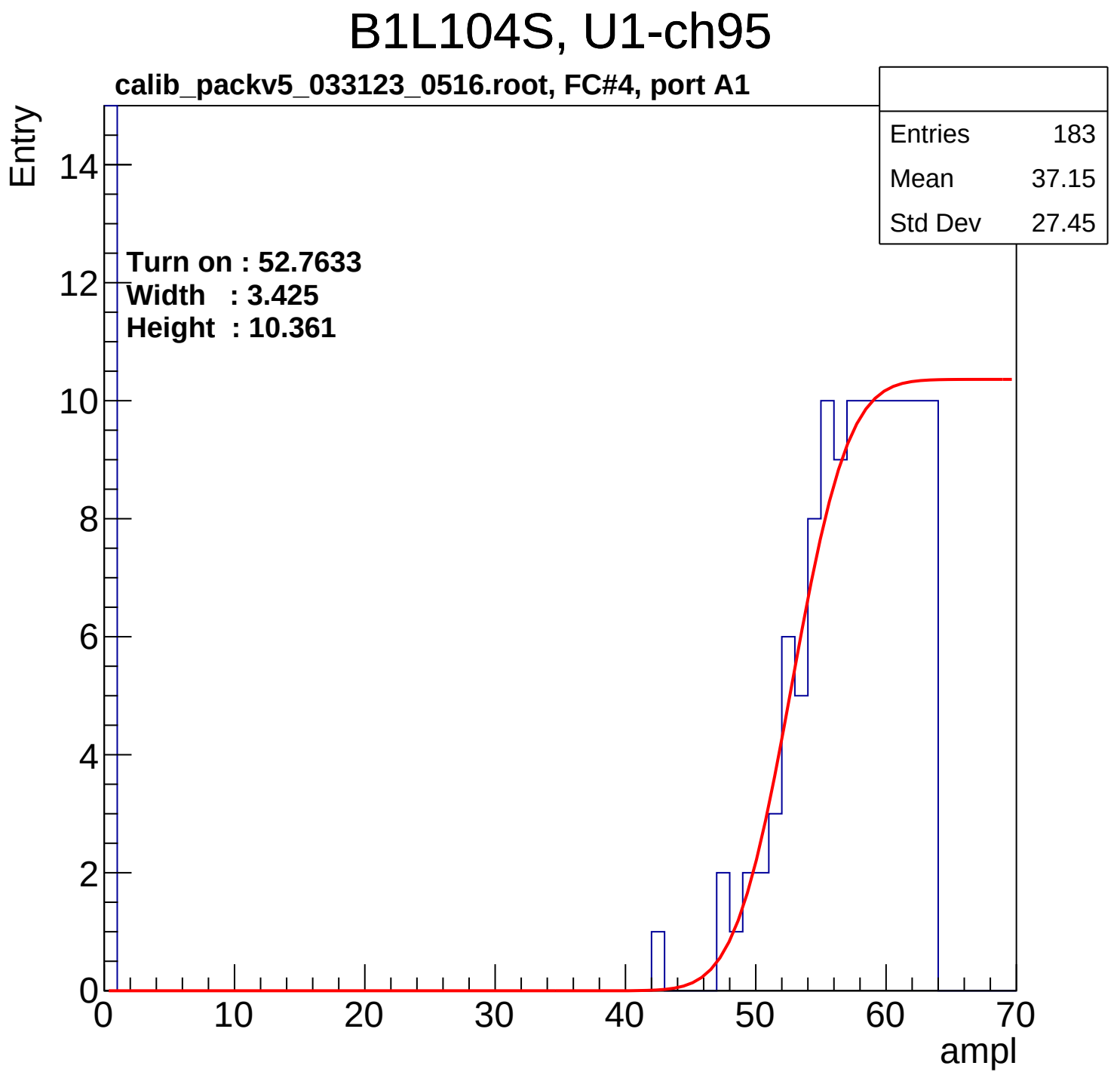

B1L104S, U1-ch90
calib_packv5_033123_0516.root, FC#4, port A1
Entries 222
Mean 33.68
Std Dev 28
Turn on : 51.2222
Width : 2.782
Height : 10.064
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

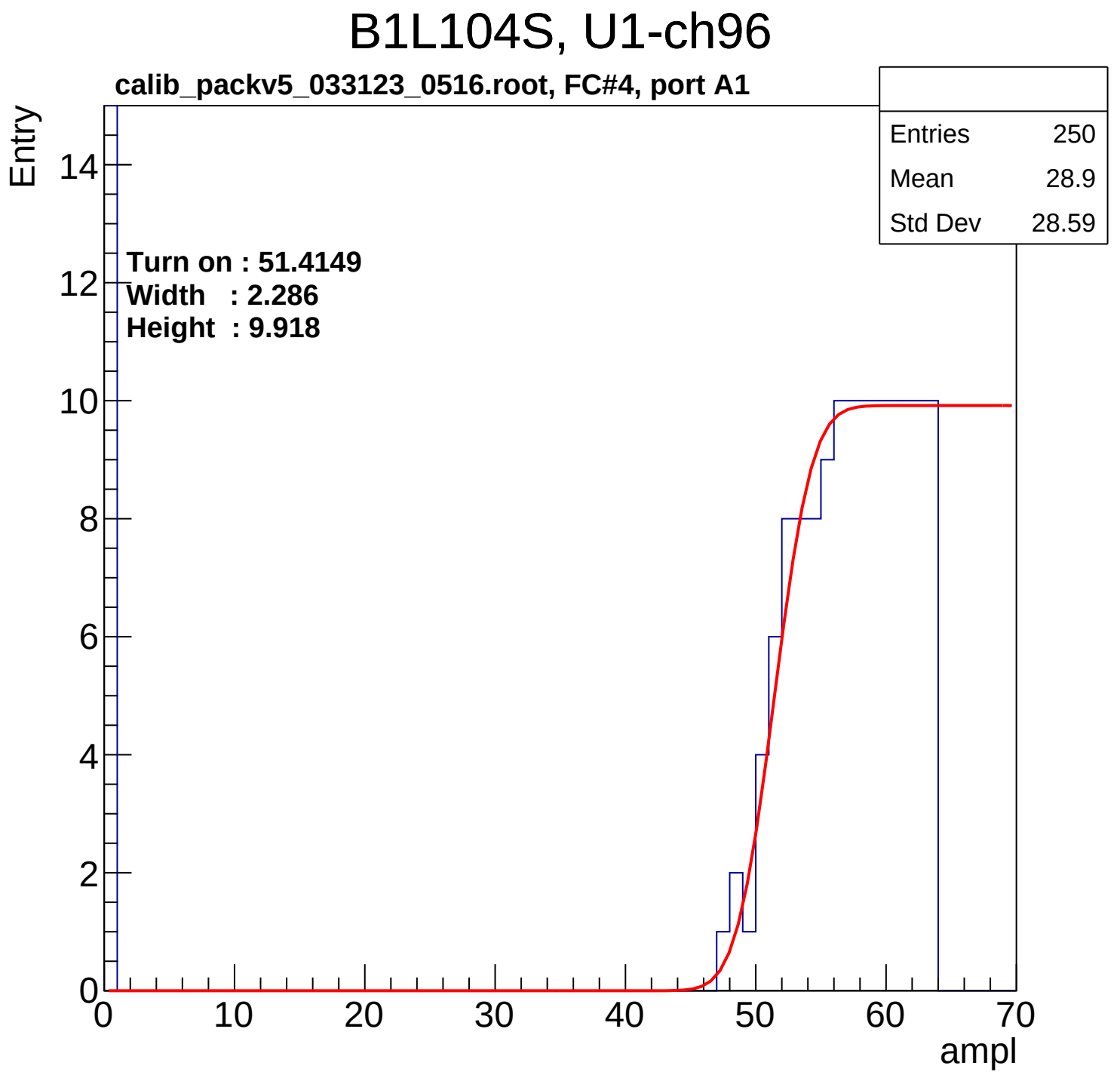

B1L104S, U1-ch91
calib_packv5_033123_0516.root, FC#4, port A1
Entries 212
Mean 31.27
Std Dev 28.62
Turn on : 53.1190
Width : 3.766
Height : 10.315
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

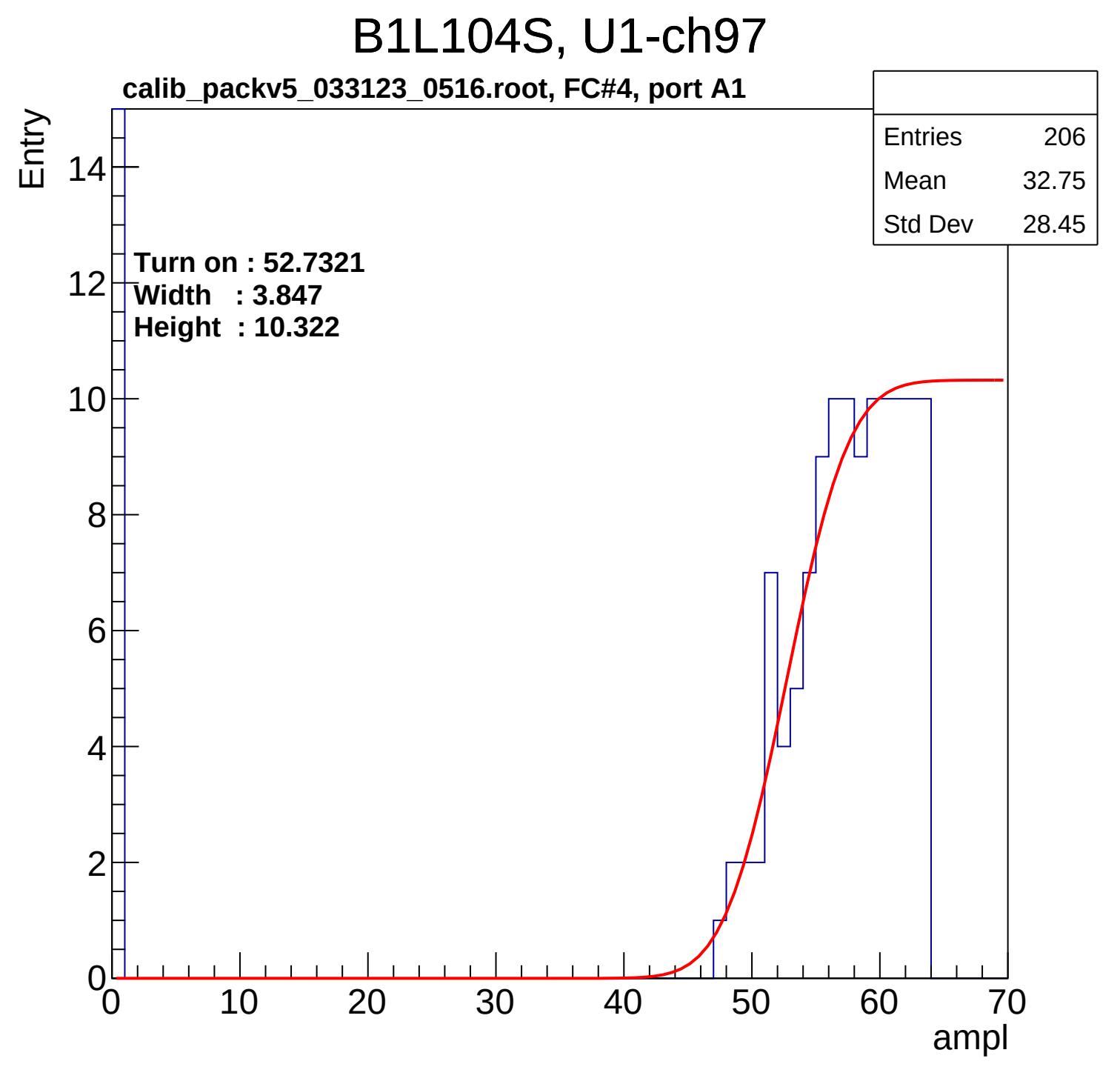

B1L104S, U1-ch92
calib_packv5_033123_0516.root, FC#4, port A1
Entries 208
Mean 33.5
Std Dev 28.04
Turn on : 51.4596
Width : 2.630
Height : 9.401
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

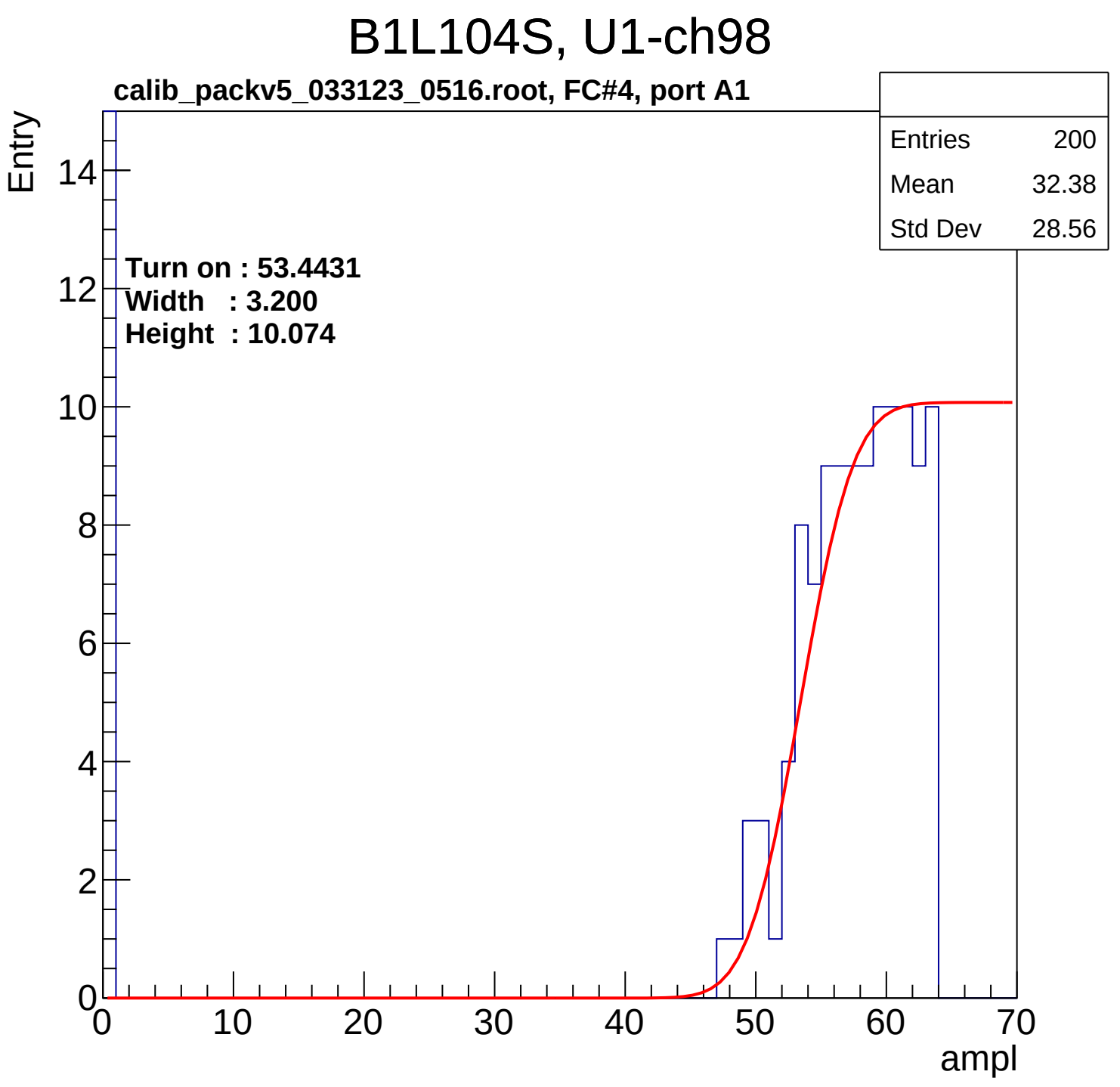

B1L104S, U1-ch93
calib_packv5_033123_0516.root, FC#4, port A1
Entries 209
Mean 34.22
Std Dev 27.98
Turn on : 51.9197
Width : 3.579
Height : 10.236
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

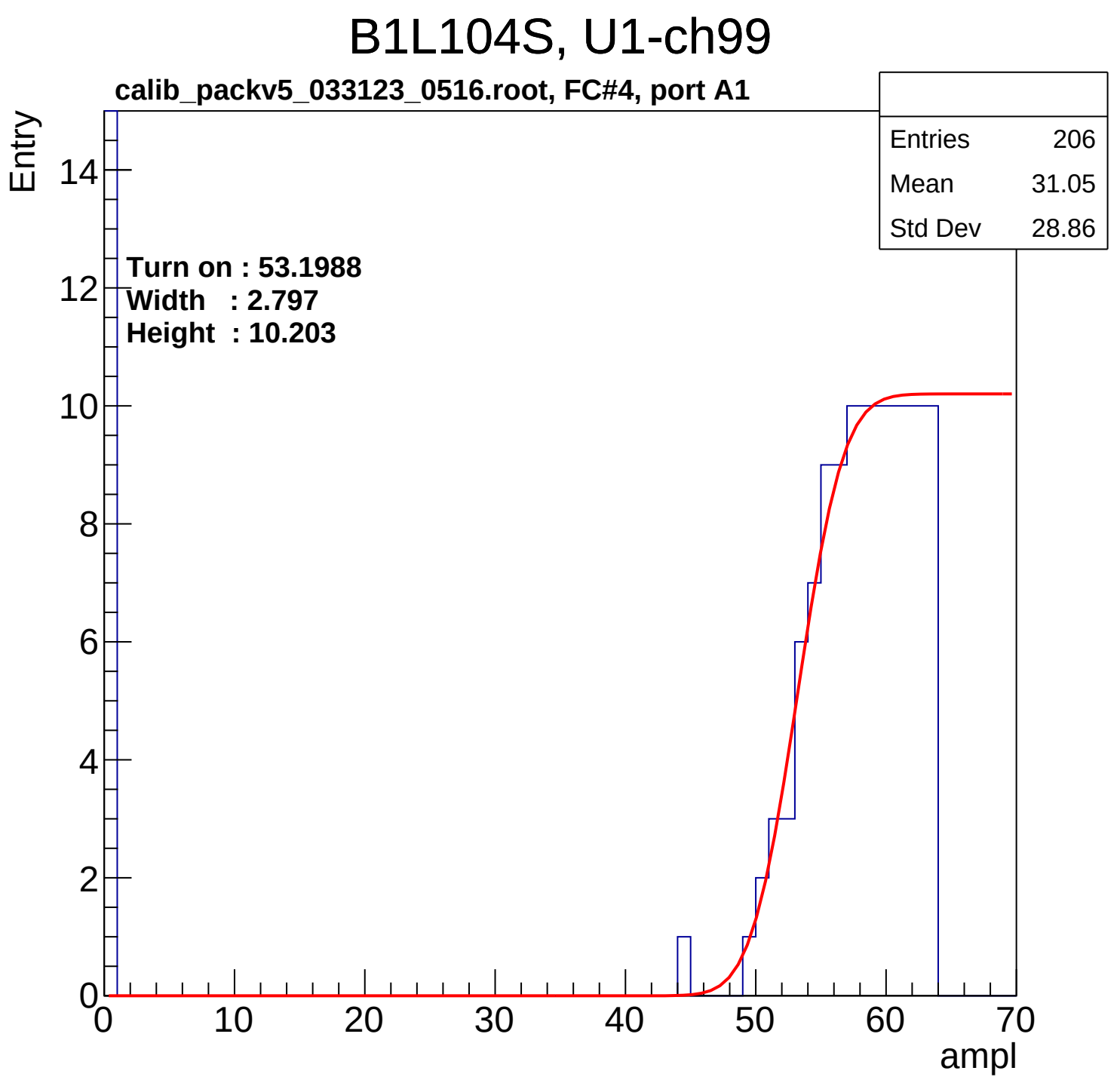

B1L104S, U1-ch94
calib_packv5_033123_0516.root, FC#4, port A1
Entries 196
Mean 34.21
Std Dev 28.28
Turn on : 52.8951
Width : 3.416
Height : 10.366
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

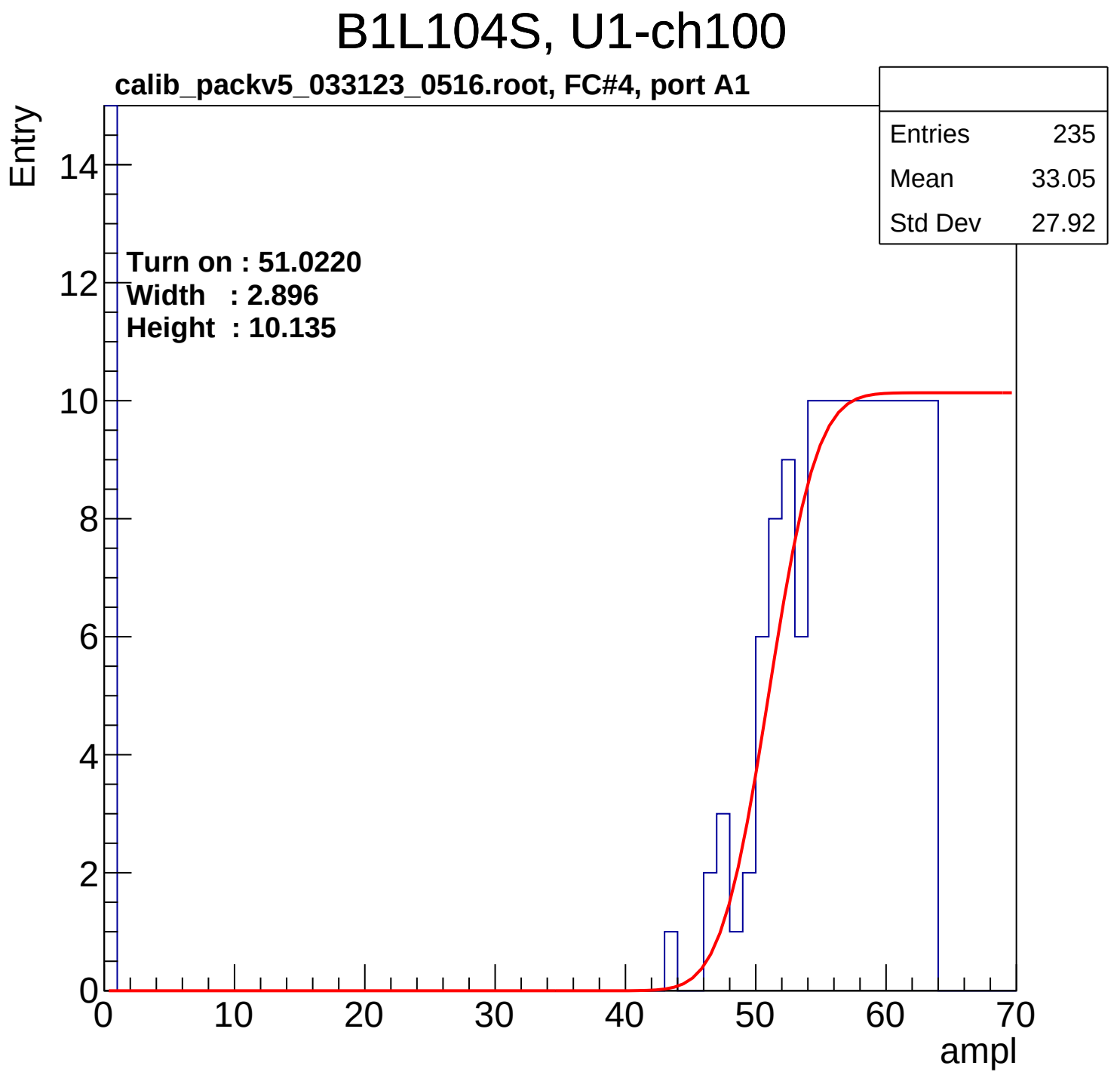

B1L104S, U1-ch95
calib_packv5_033123_0516.root, FC#4, port A1
Entries 183
Mean 37.15
Std Dev 27.45
Turn on : 52.7633
Width : 3.425
Height : 10.361
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

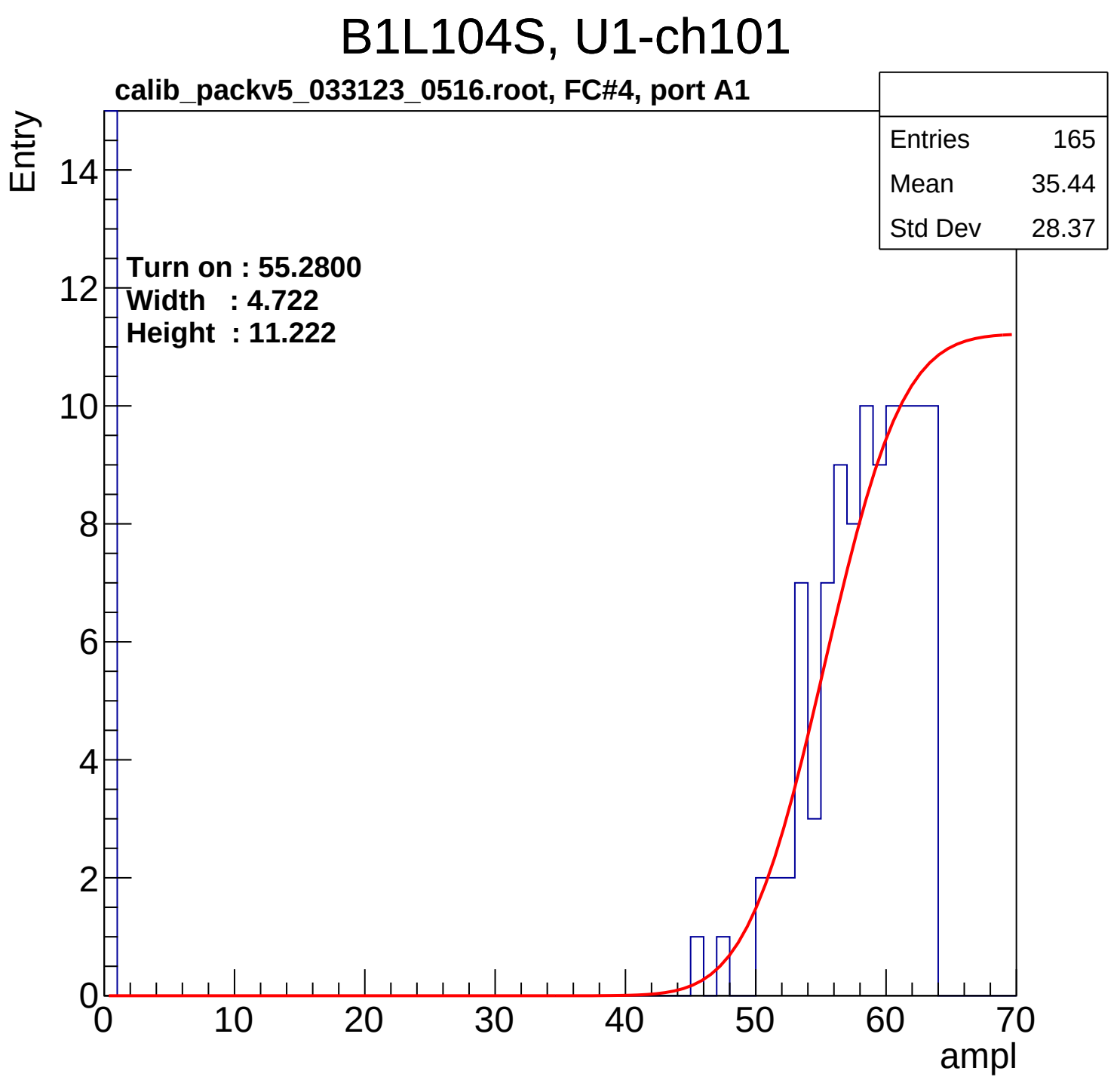

B1L104S, U1-ch96
calib_packv5_033123_0516.root, FC#4, port A1
Entries 250
Mean 28.9
Std Dev 28.59
Turn on : 51.4149
Width : 2.286
Height : 9.918
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

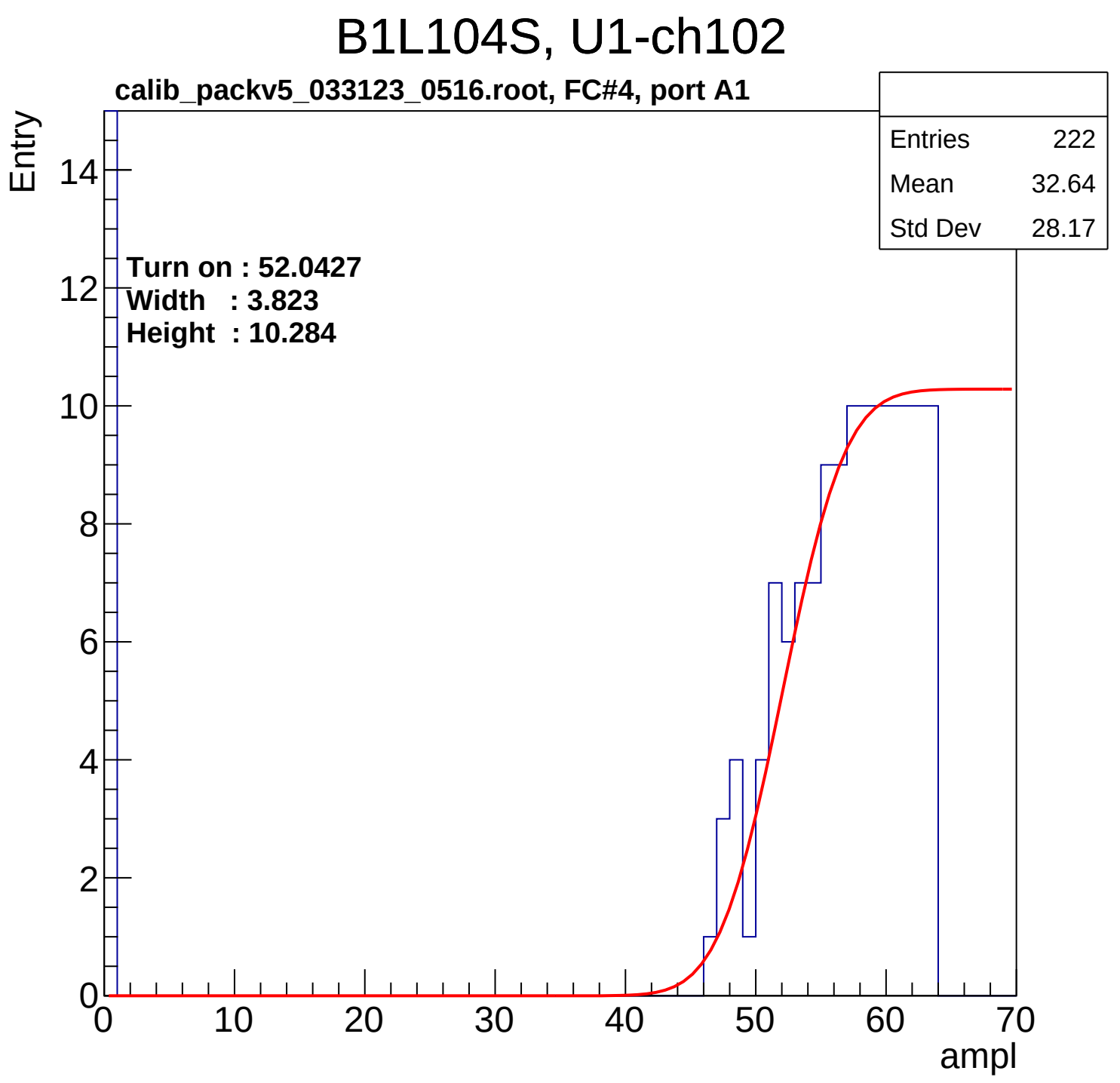

B1L104S, U1-ch97
calib_packv5_033123_0516.root, FC#4, port A1
Entries 206
Mean 32.75
Std Dev 28.45
Turn on : 52.7321
Width : 3.847
Height : 10.322
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

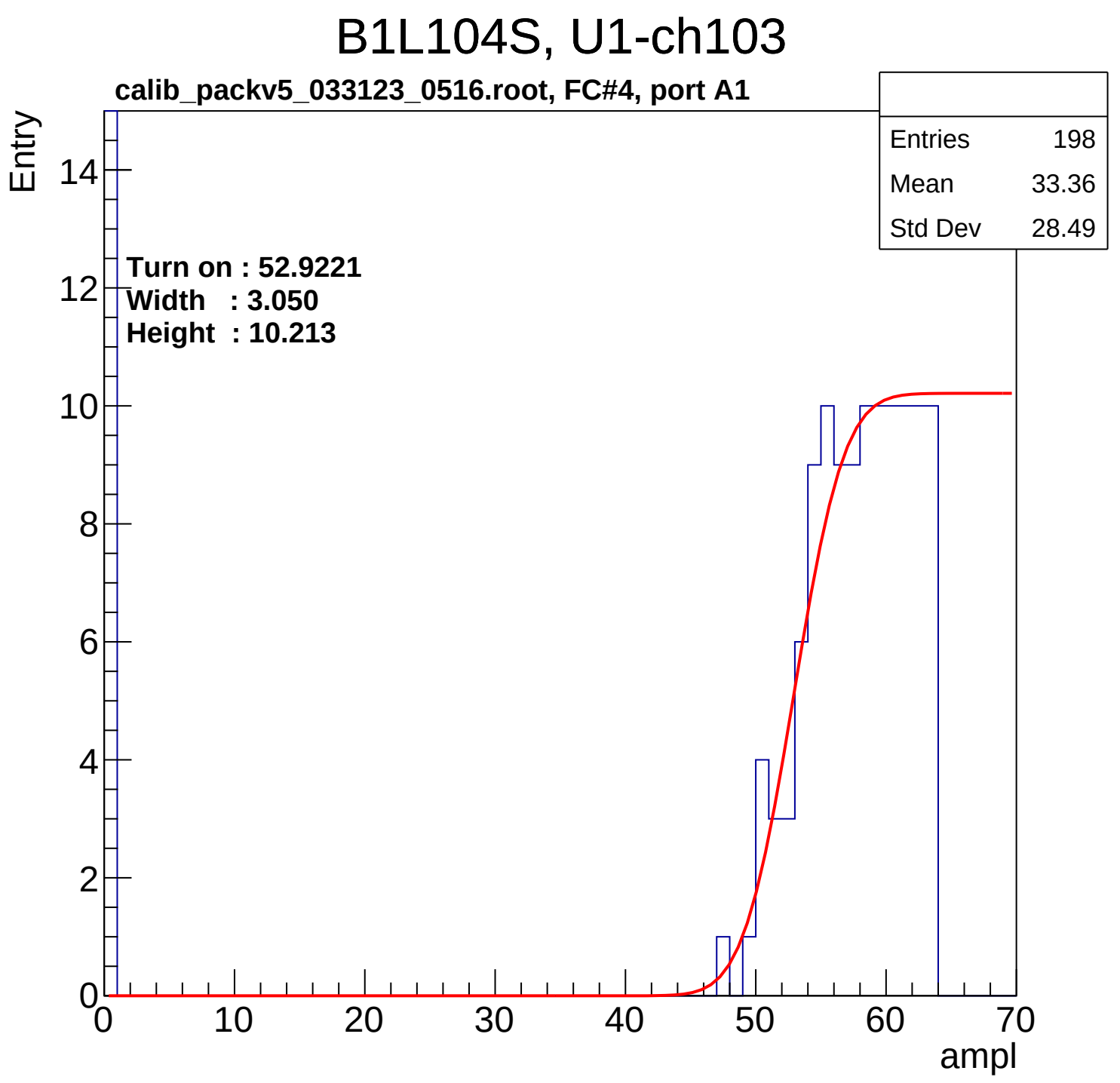

B1L104S, U1-ch98
calib_packv5_033123_0516.root, FC#4, port A1
Entries 200
Mean 32.38
Std Dev 28.56
Turn on : 53.4431
Width : 3.200
Height : 10.074
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

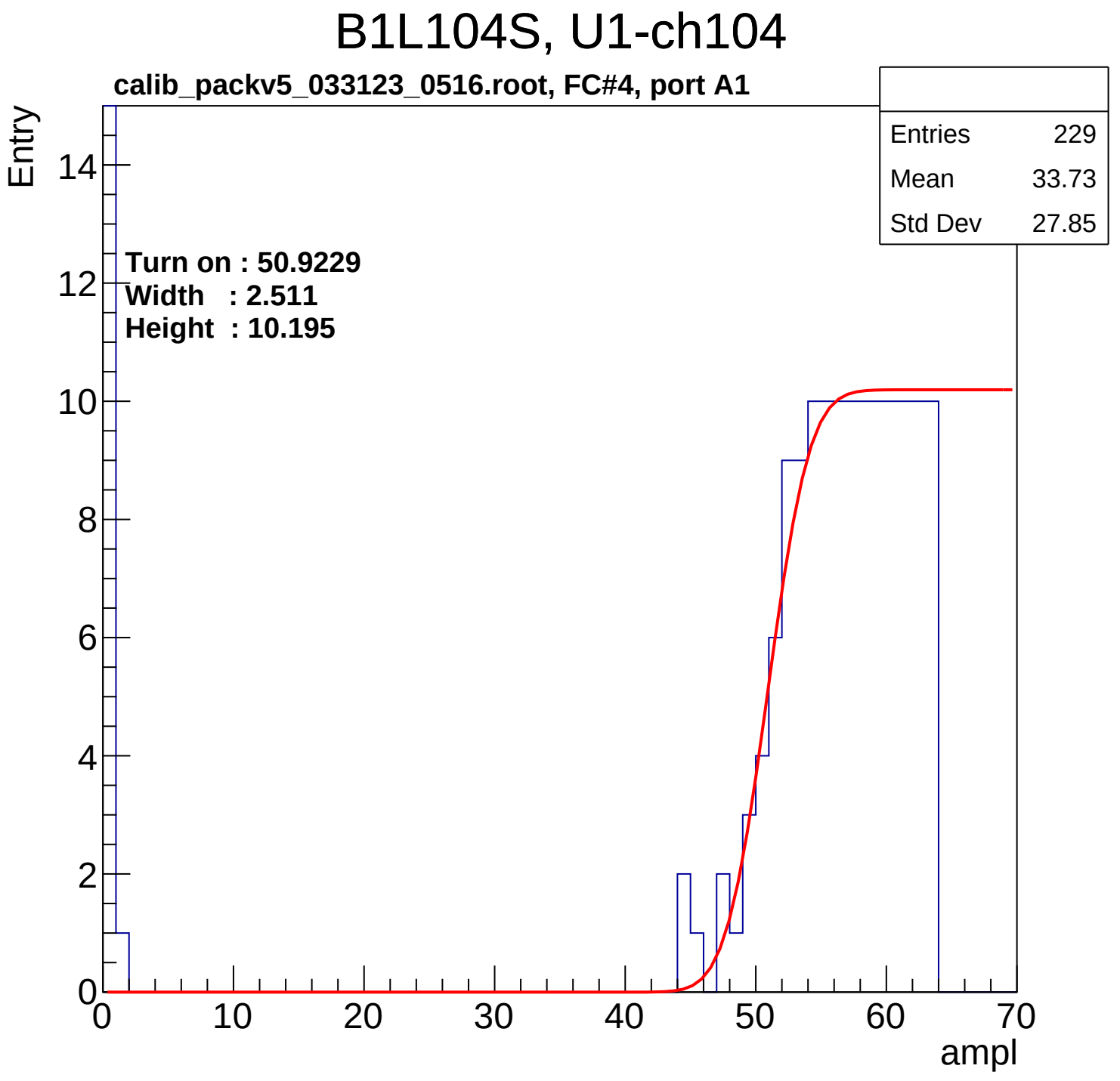

B1L104S, U1-ch99
calib_packv5_033123_0516.root, FC#4, port A1
Entries 206
Mean 31.05
Std Dev 28.86
Turn on : 53.1988
Width : 2.797
Height : 10.203
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

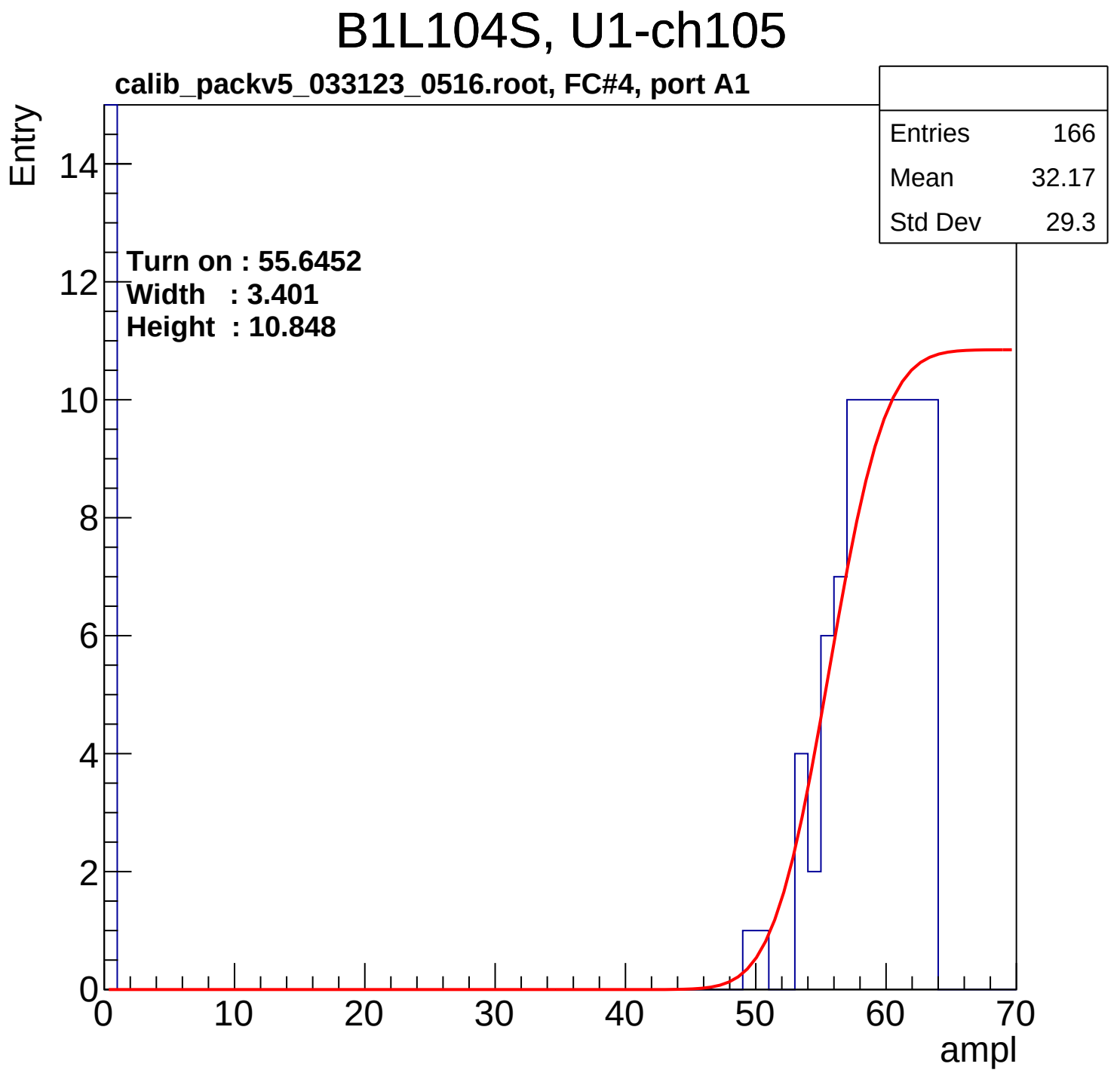

B1L104S, U1-ch100
calib_packv5_033123_0516.root, FC#4, port A1
Entries 235
Mean 33.05
Std Dev 27.92
Turn on : 51.0220
Width : 2.896
Height : 10.135
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

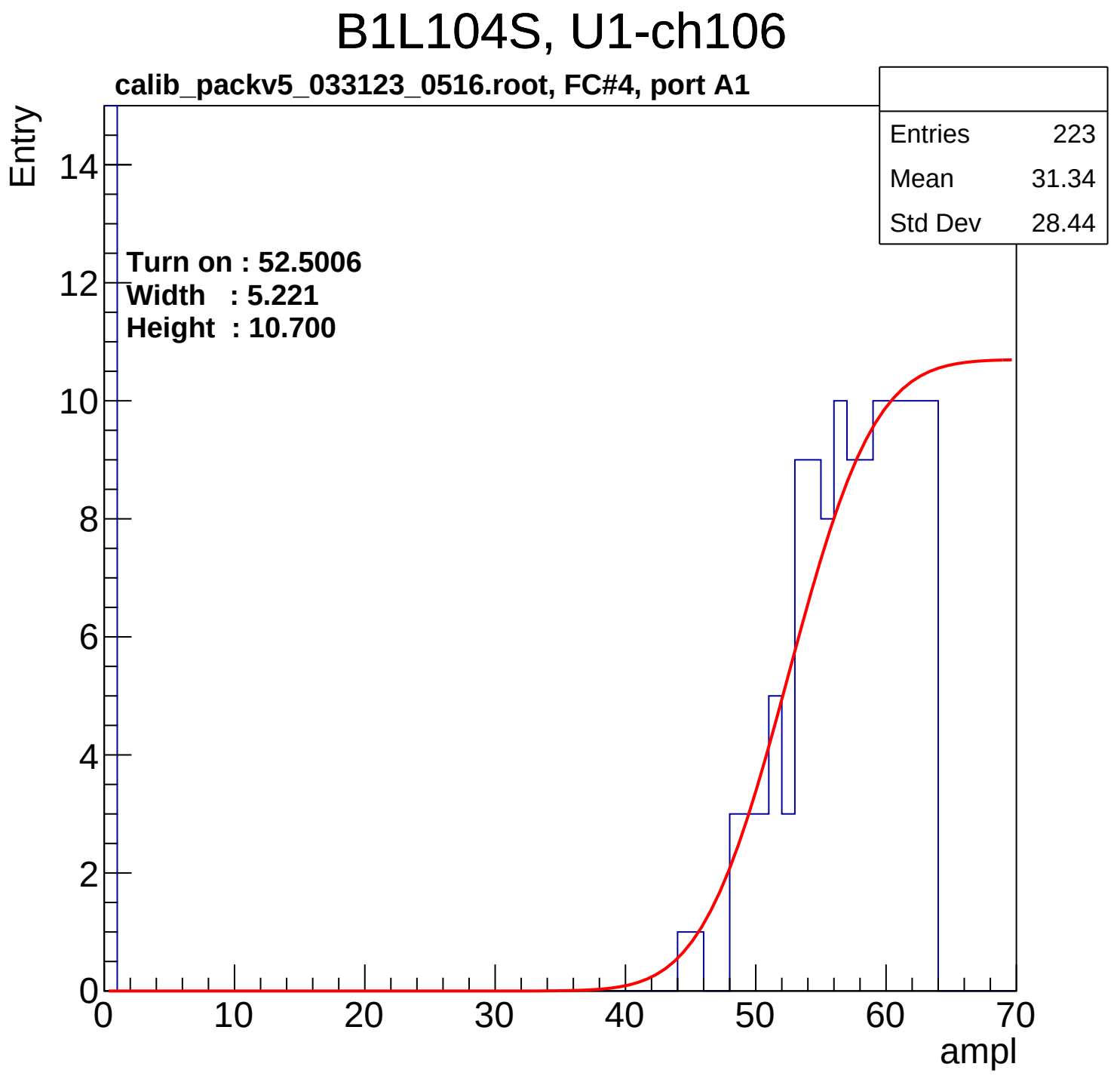

B1L104S, U1-ch101
calib_packv5_033123_0516.root, FC#4, port A1
Entries 165
Mean 35.44
Std Dev 28.37
Turn on : 55.2800
Width : 4.722
Height : 11.222
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

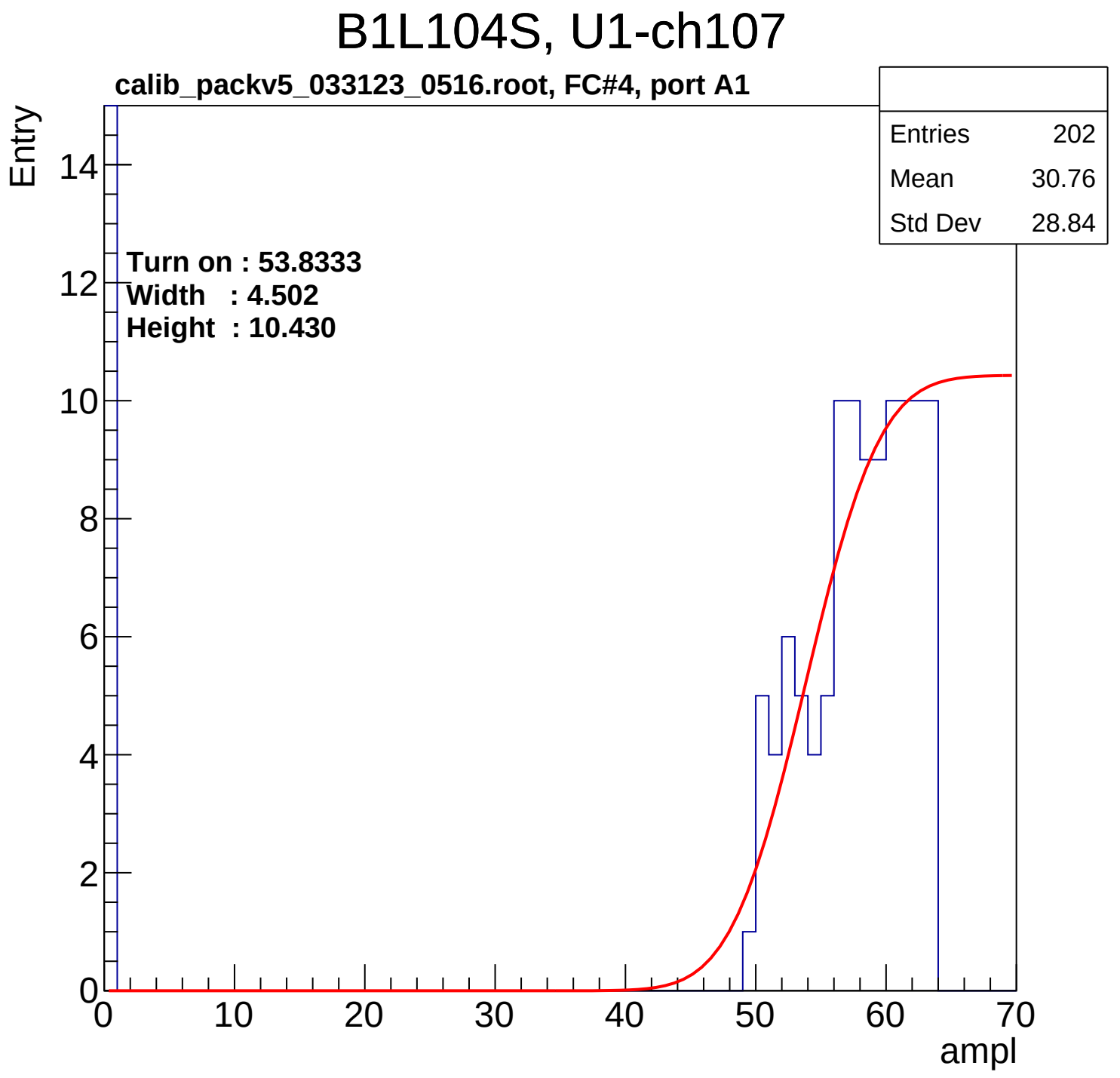

B1L104S, U1-ch102
calib_packv5_033123_0516.root, FC#4, port A1
Entries 222
Mean 32.64
Std Dev 28.17
Turn on : 52.0427
Width : 3.823
Height : 10.284
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

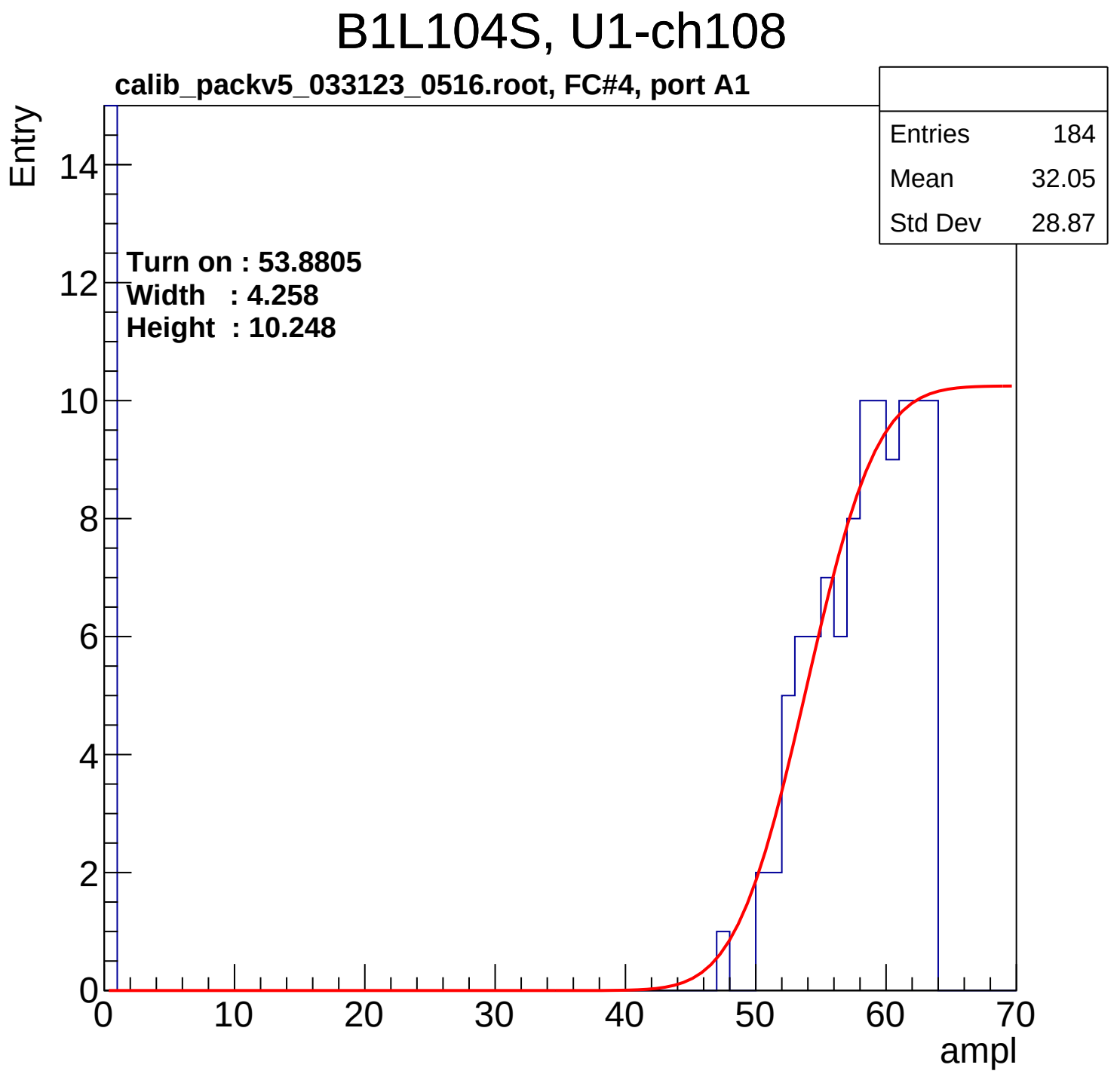

B1L104S, U1-ch103
calib_packv5_033123_0516.root, FC#4, port A1
Entries 198
Mean 33.36
Std Dev 28.49
Turn on : 52.9221
Width : 3.050
Height : 10.213
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

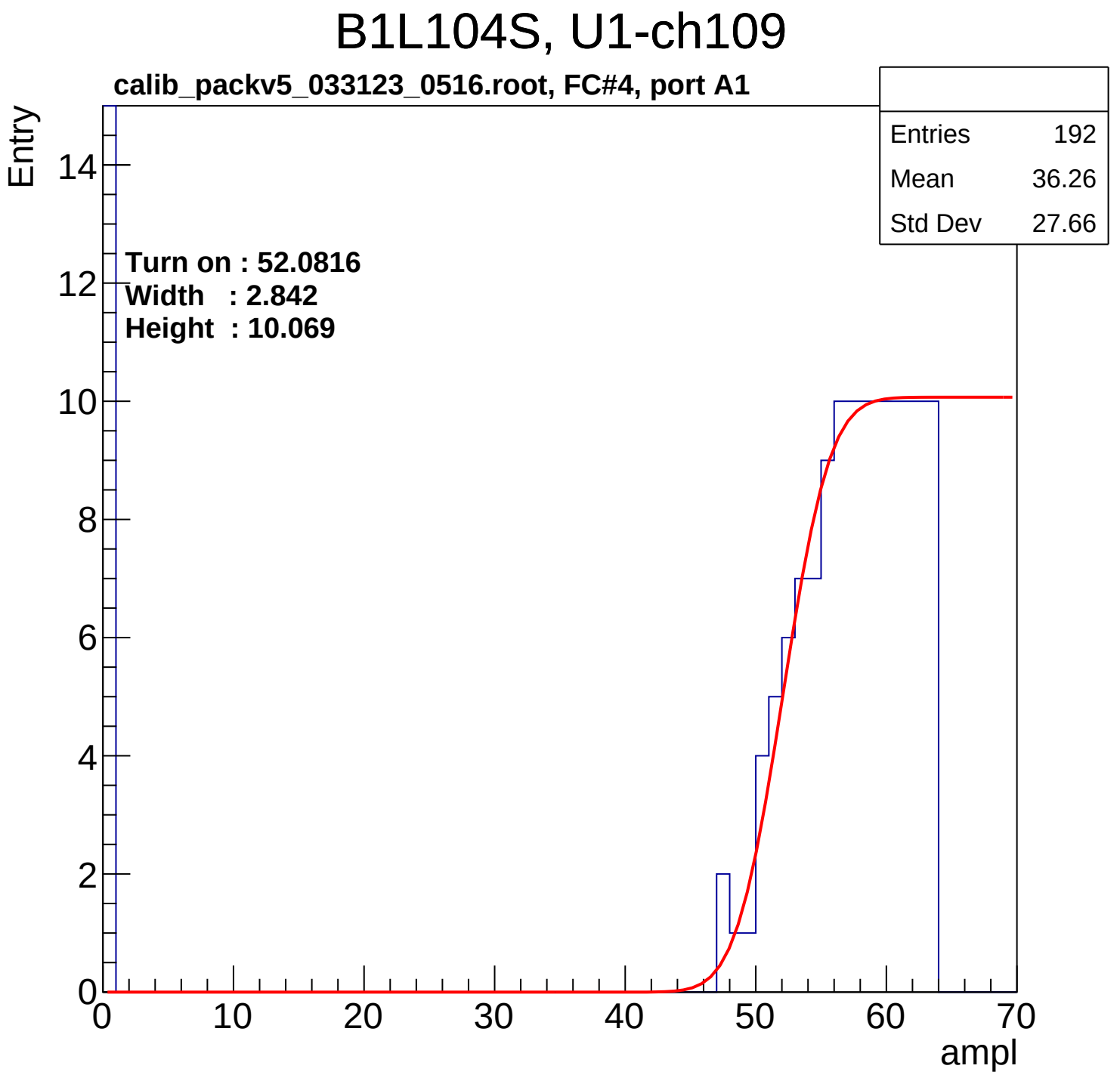

B1L104S, U1-ch104
calib_packv5_033123_0516.root, FC#4, port A1
Entries 229
Mean 33.73
Std Dev 27.85
Turn on : 50.9229
Width : 2.511
Height : 10.195
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

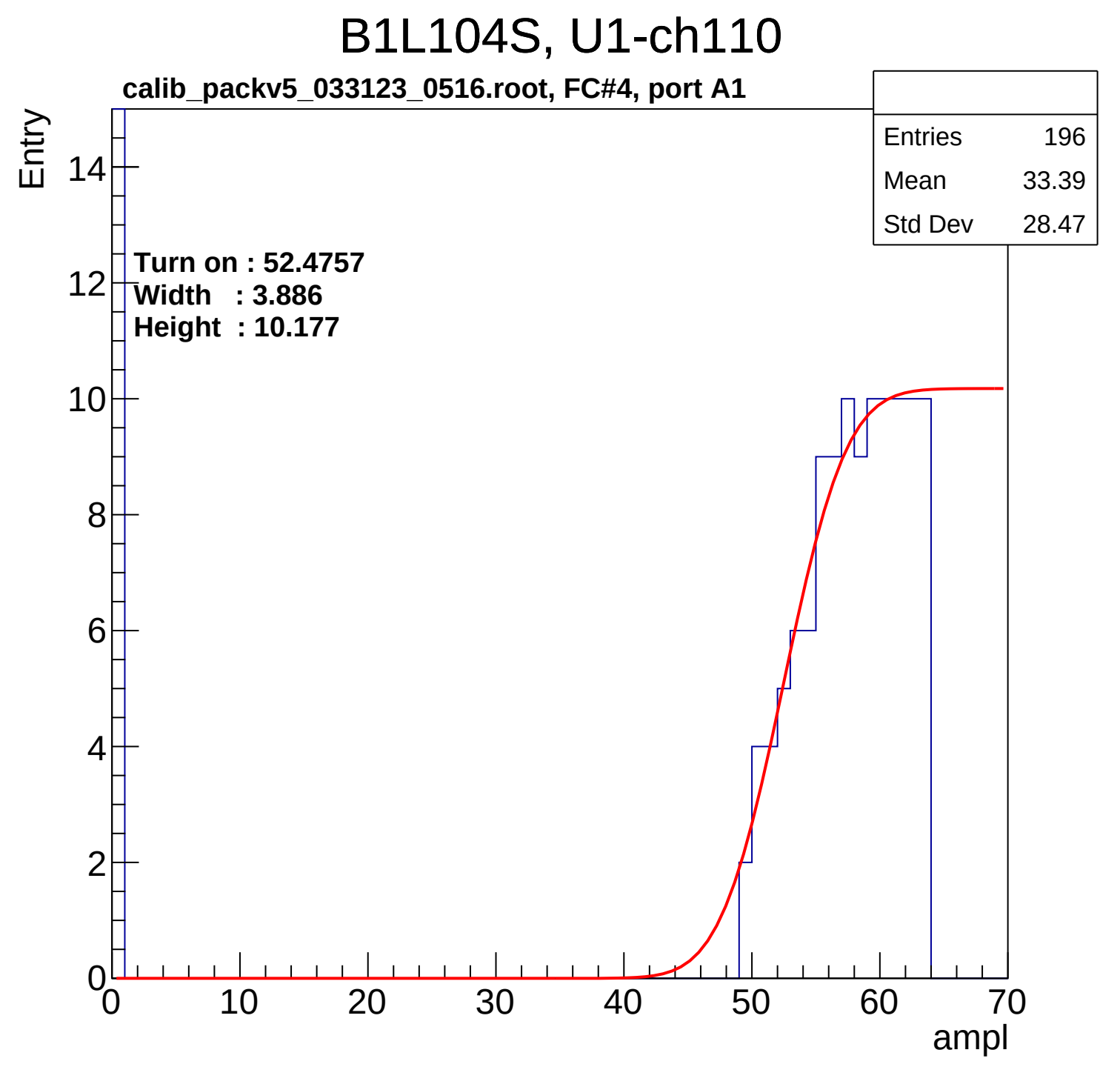

B1L104S, U1-ch105
calib_packv5_033123_0516.root, FC#4, port A1
Entries 166
Mean 32.17
Std Dev 29.3
Turn on : 55.6452
Width : 3.401
Height : 10.848
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

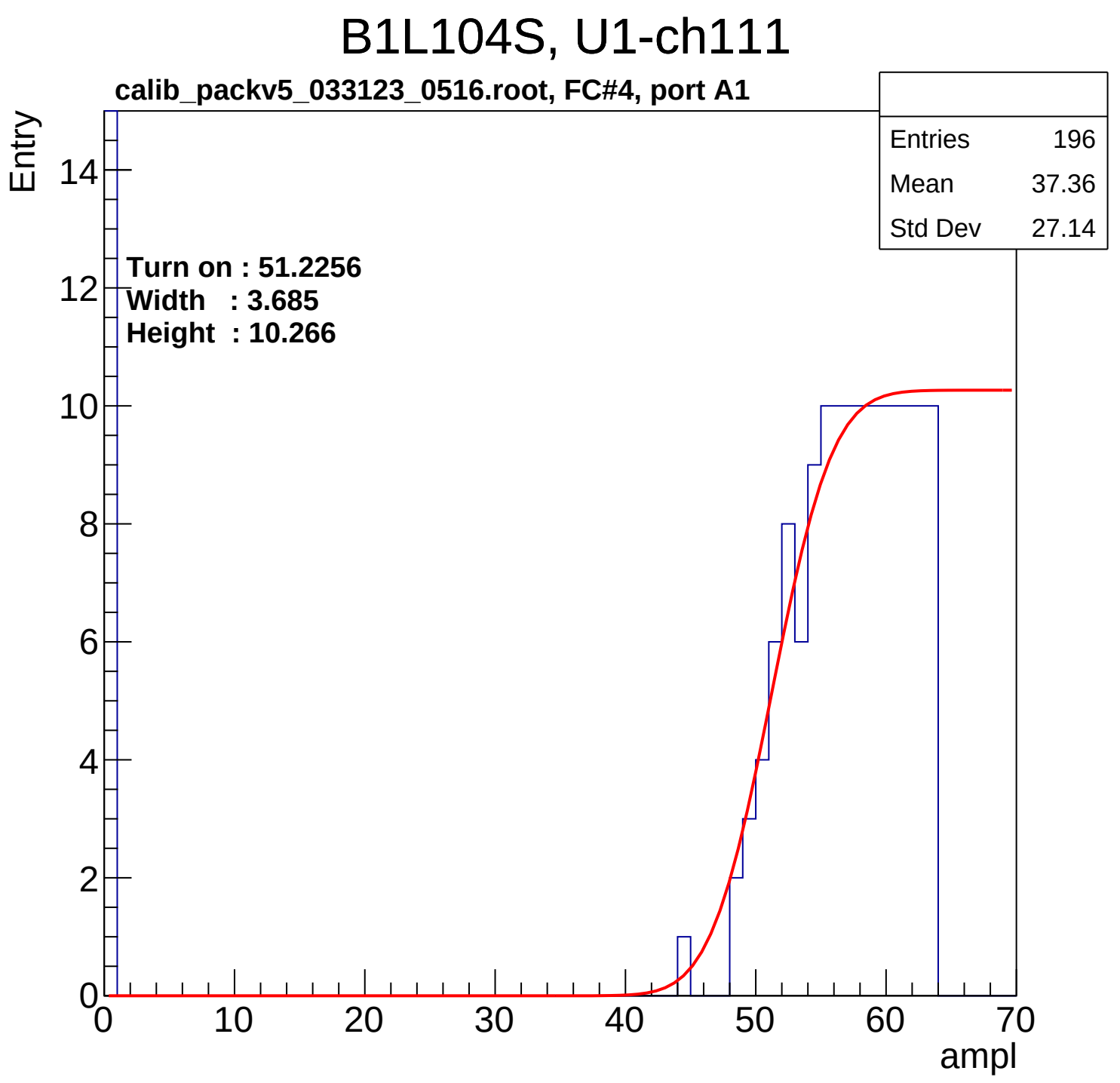

B1L104S, U1-ch106
calib_packv5_033123_0516.root, FC#4, port A1
Entries 223
Mean 31.34
Std Dev 28.44
Turn on : 52.5006
Width : 5.221
Height : 10.700
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

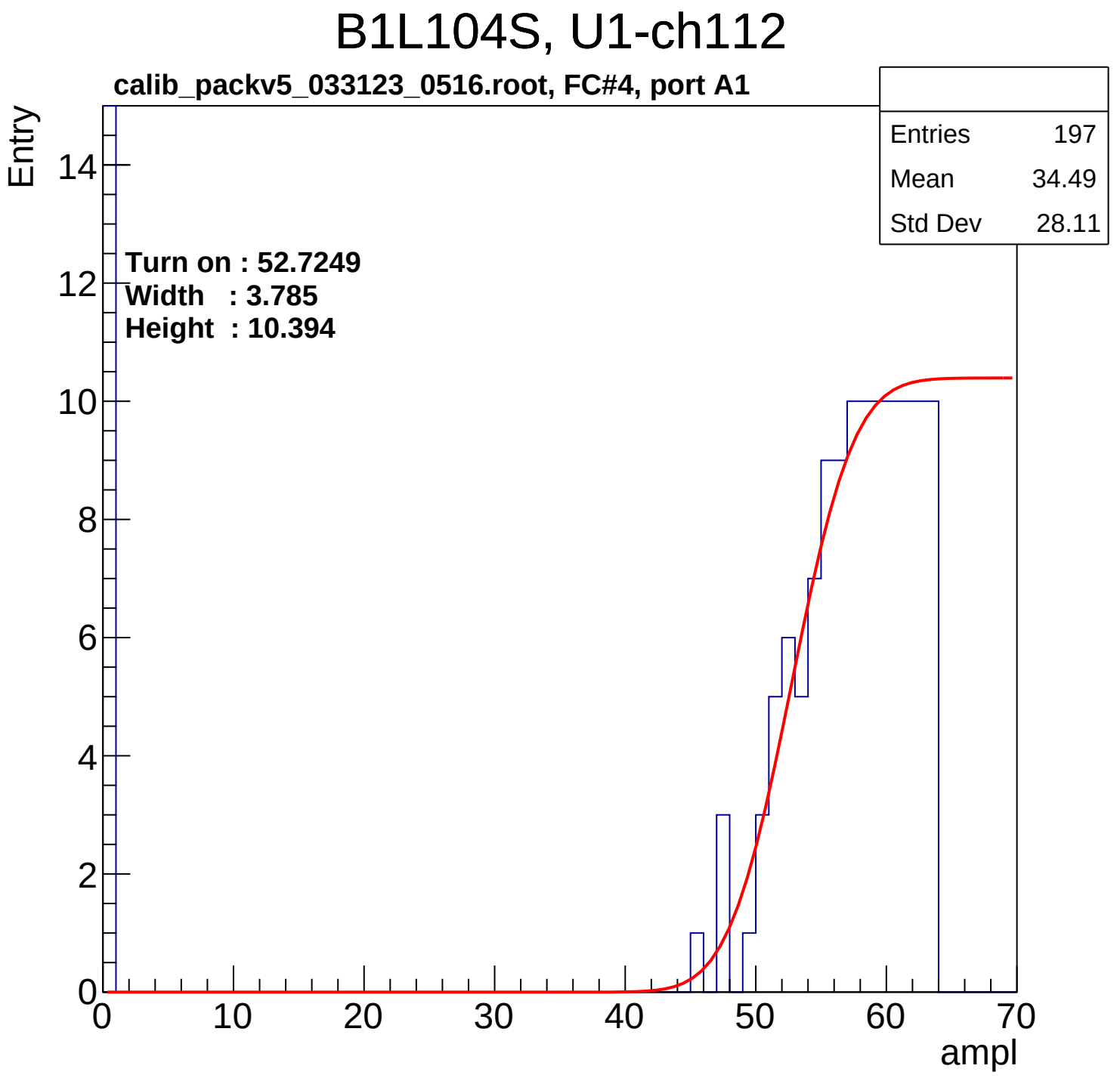

B1L104S, U1-ch107
calib_packv5_033123_0516.root, FC#4, port A1
Entries 202
Mean 30.76
Std Dev 28.84
Turn on : 53.8333
Width : 4.502
Height : 10.430
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

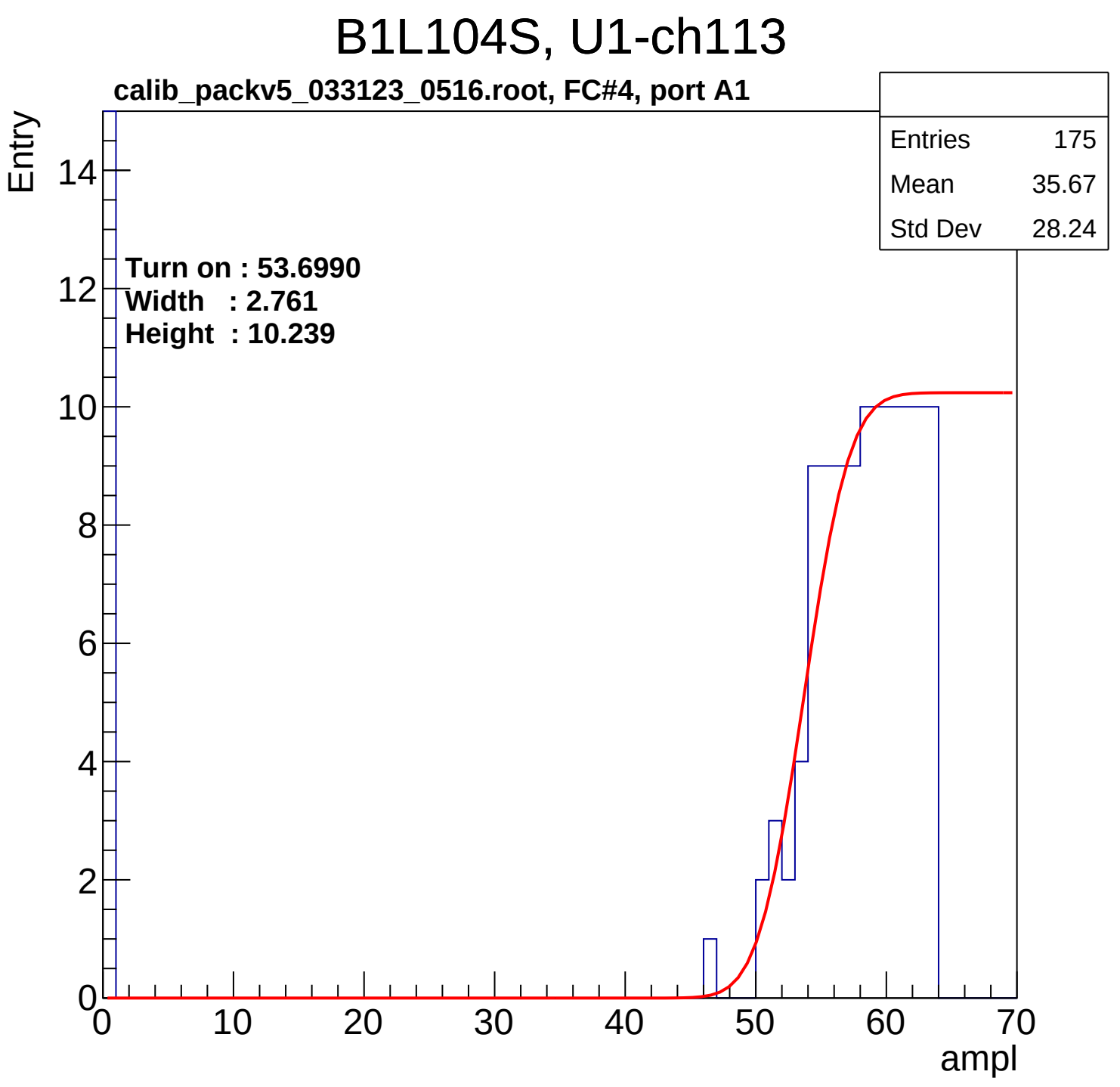

B1L104S, U1-ch108
calib_packv5_033123_0516.root, FC#4, port A1
Entries 184
Mean 32.05
Std Dev 28.87
Turn on : 53.8805
Width : 4.258
Height : 10.248
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

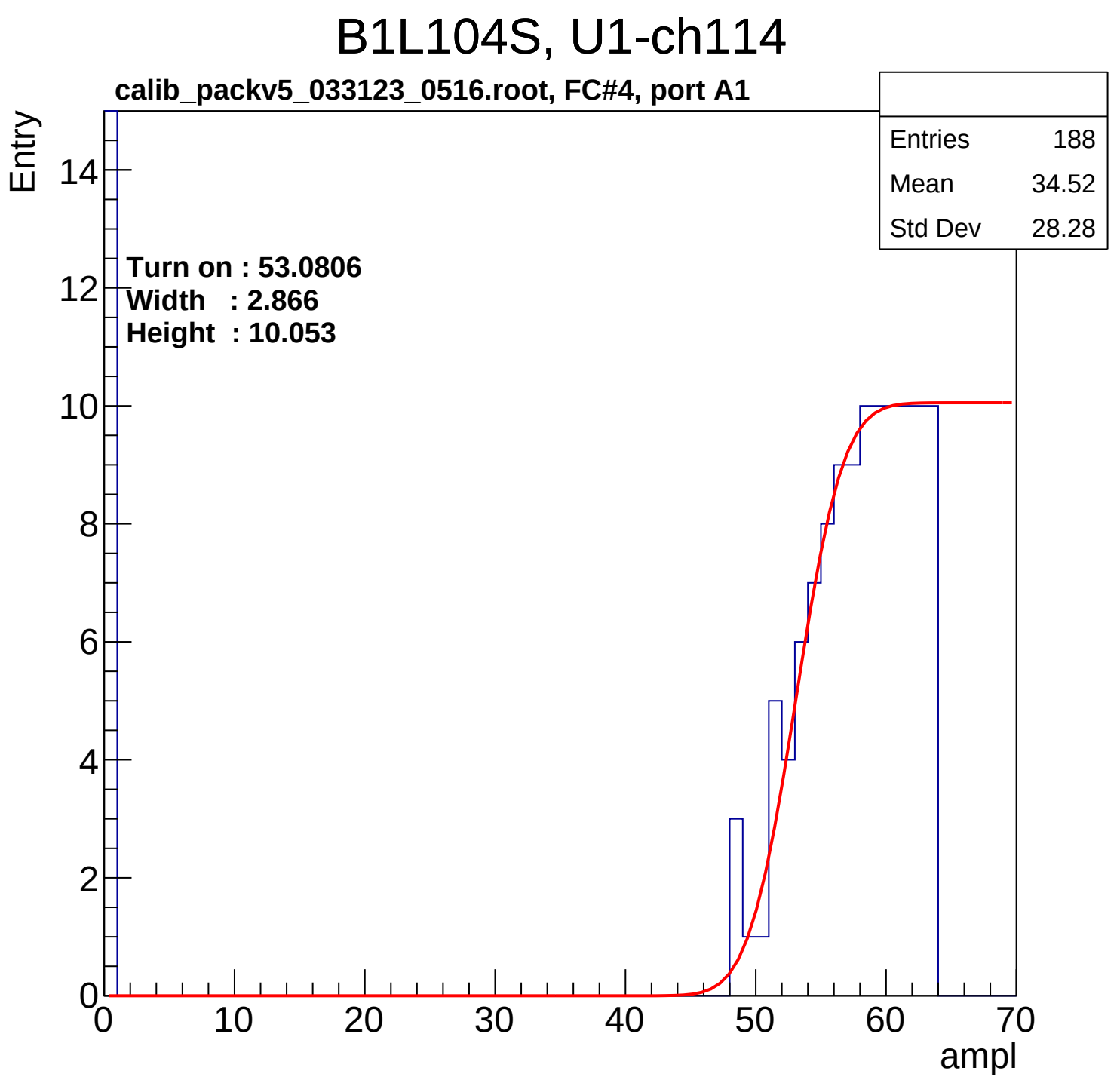

B1L104S, U1-ch109
calib_packv5_033123_0516.root, FC#4, port A1
Entries 192
Mean 36.26
Std Dev 27.66
Turn on : 52.0816
Width : 2.842
Height : 10.069
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

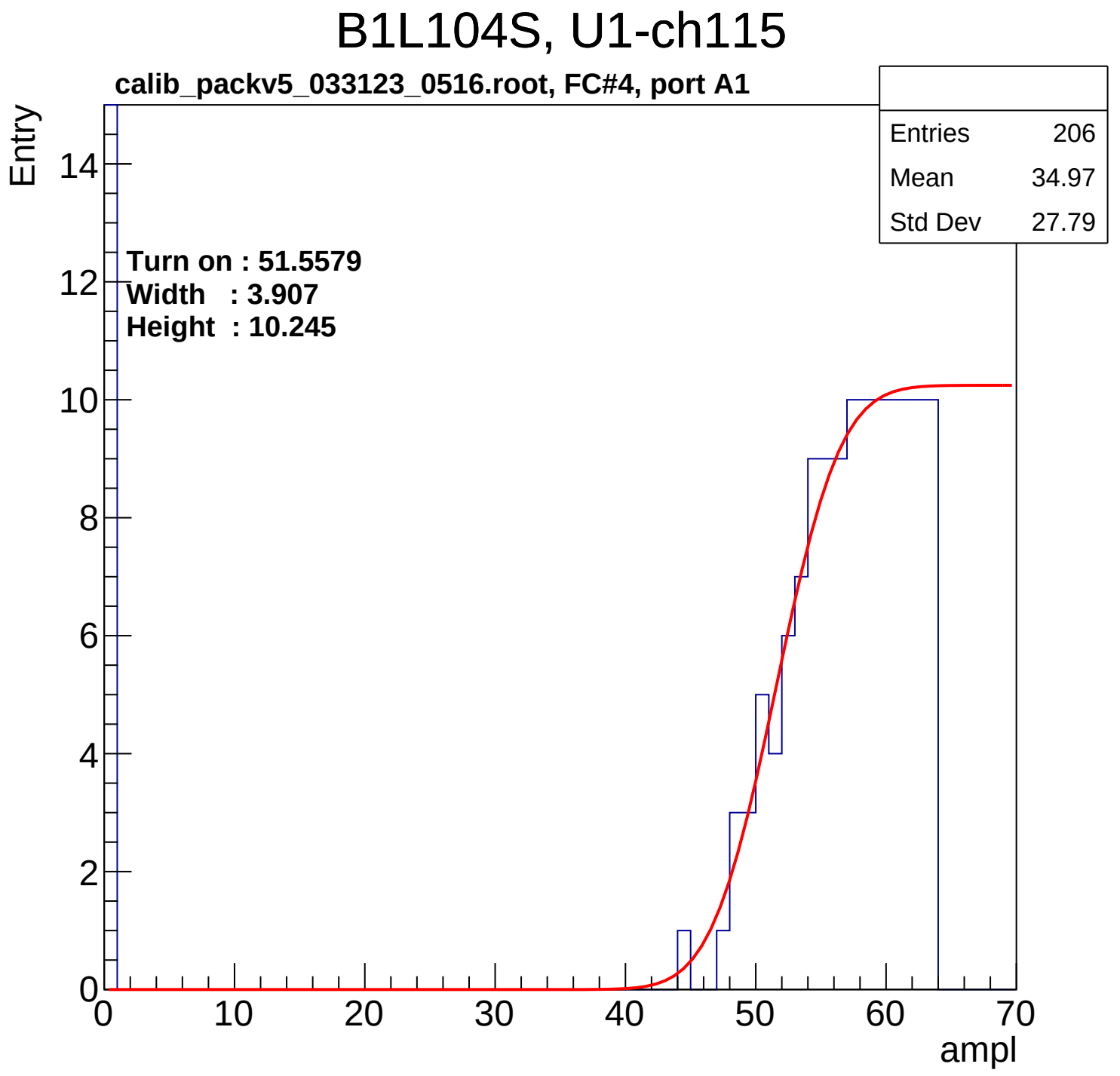

B1L104S, U1-ch110
calib_packv5_033123_0516.root, FC#4, port A1
Entries 196
Mean 33.39
Std Dev 28.47
Turn on : 52.4757
Width : 3.886
Height : 10.177
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

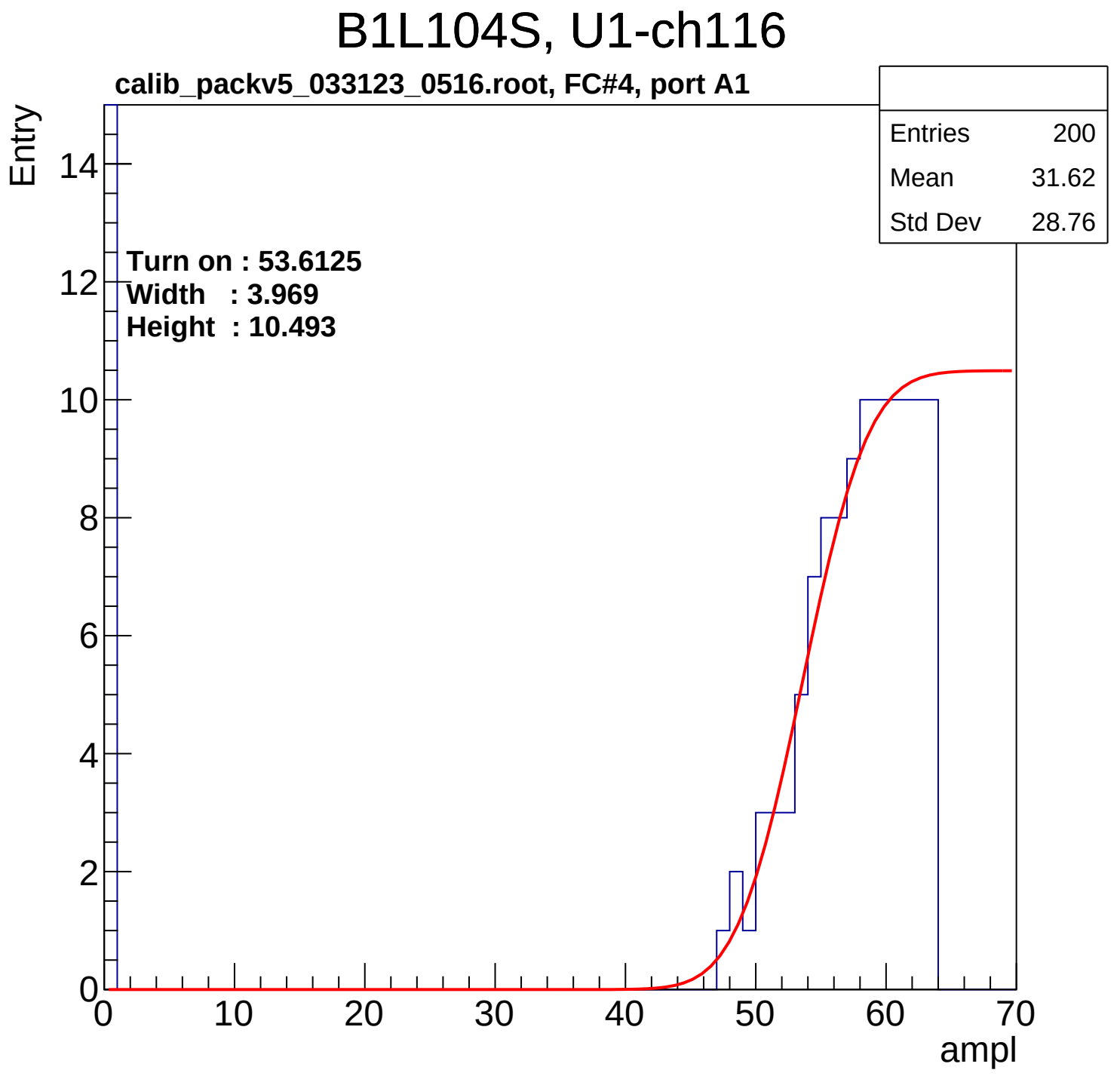

B1L104S, U1-ch111
calib_packv5_033123_0516.root, FC#4, port A1
Entries 196
Mean 37.36
Std Dev 27.14
Turn on : 51.2256
Width : 3.685
Height : 10.266
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

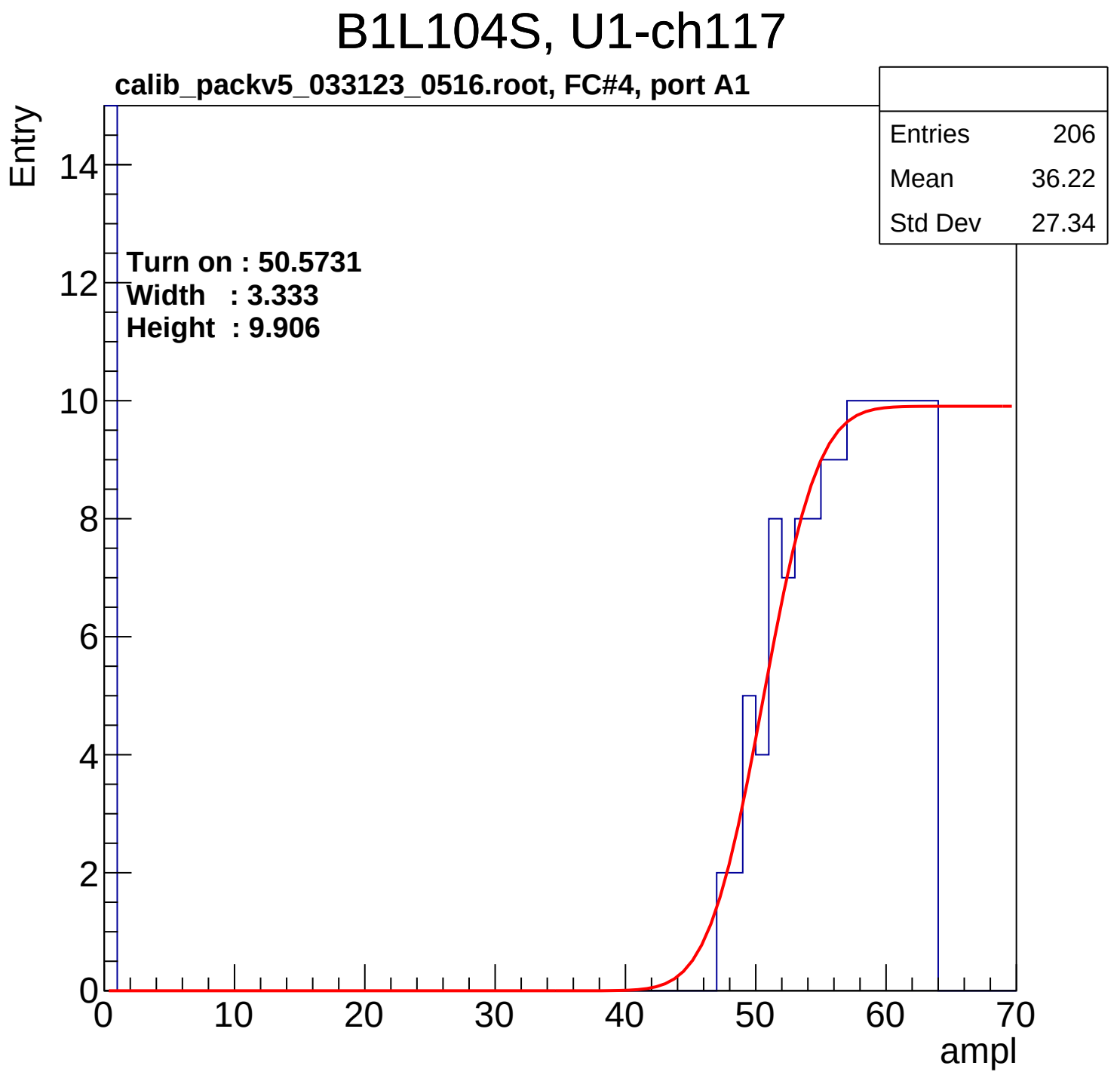

B1L104S, U1-ch112
calib_packv5_033123_0516.root, FC#4, port A1
Entries 197
Mean 34.49
Std Dev 28.11
Turn on : 52.7249
Width : 3.785
Height : 10.394
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

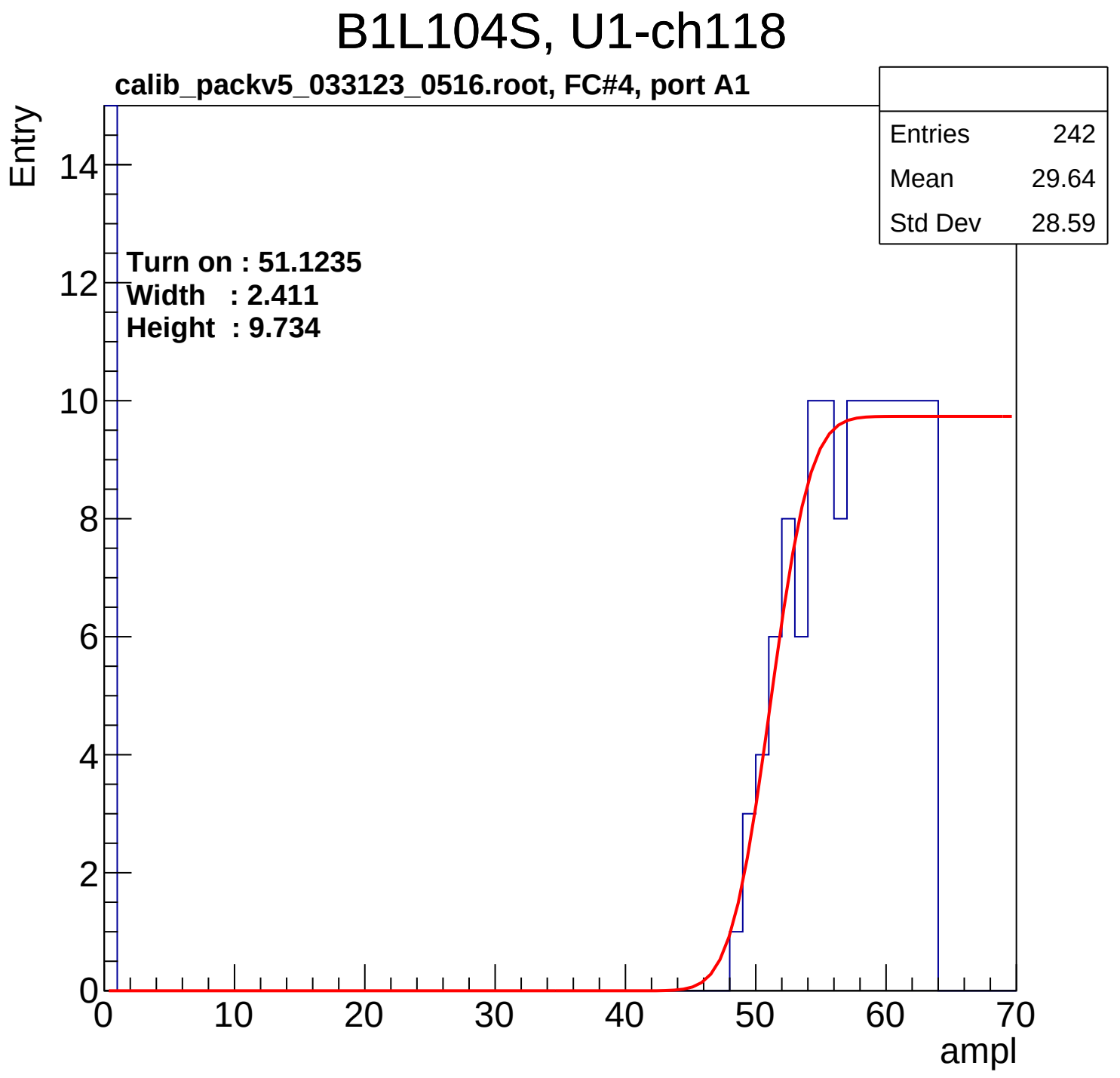

B1L104S, U1-ch113
calib_packv5_033123_0516.root, FC#4, port A1
Entries 175
Mean 35.67
Std Dev 28.24
Turn on : 53.6990
Width : 2.761
Height : 10.239
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

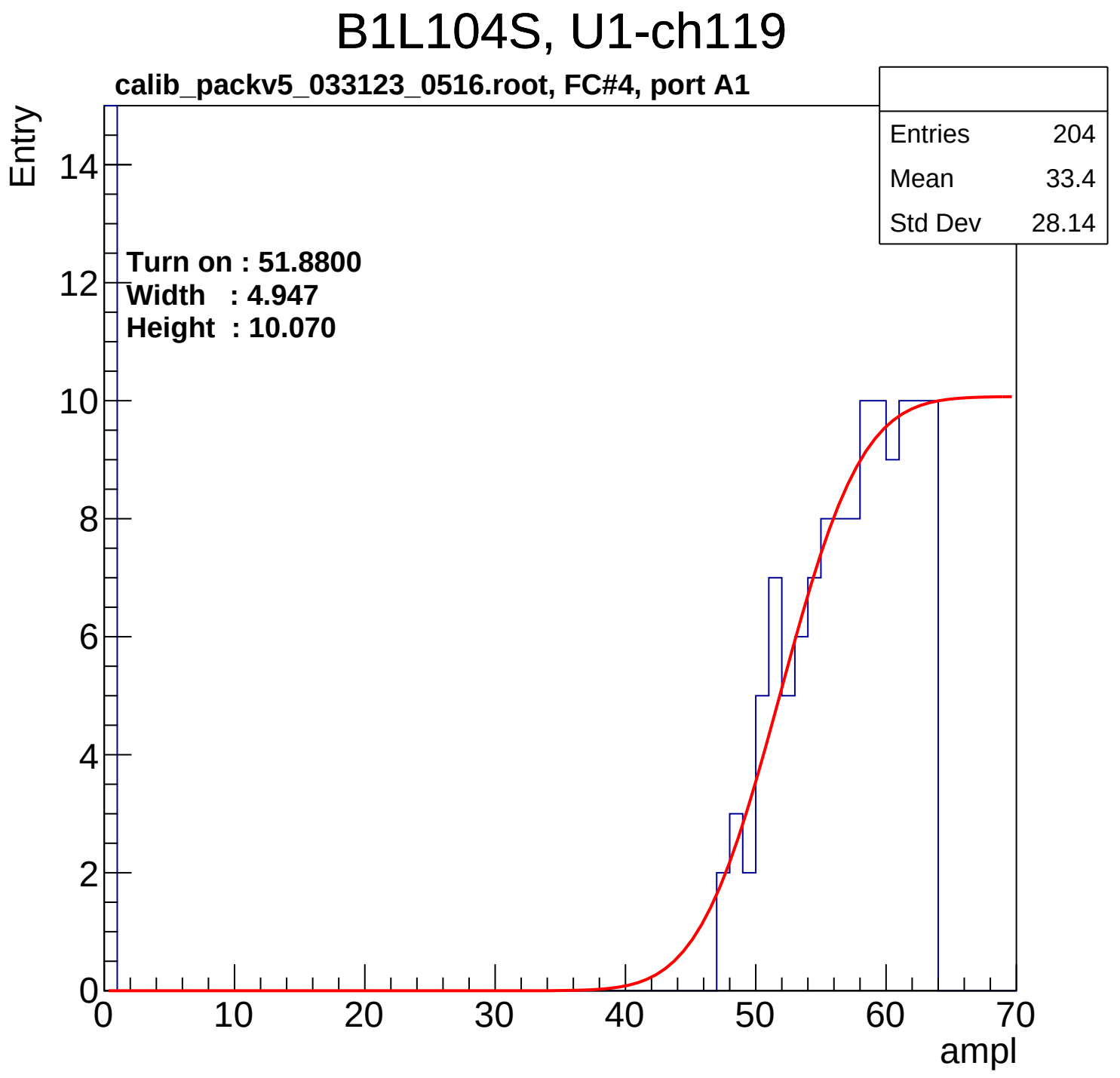

B1L104S, U1-ch114
calib_packv5_033123_0516.root, FC#4, port A1
Entries 188
Mean 34.52
Std Dev 28.28
Turn on : 53.0806
Width : 2.866
Height : 10.053
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

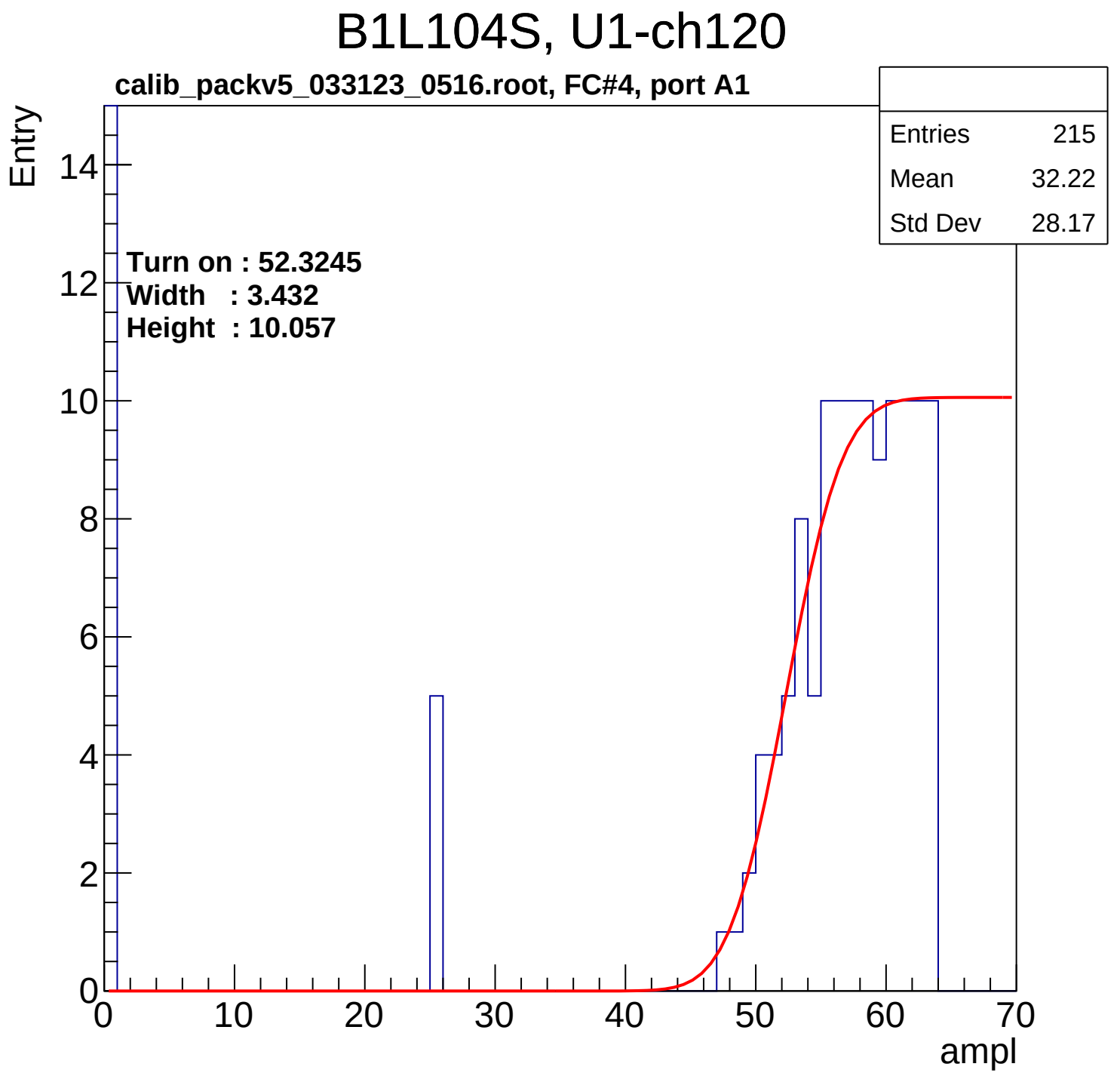

B1L104S, U1-ch115
calib_packv5_033123_0516.root, FC#4, port A1
Entries 206
Mean 34.97
Std Dev 27.79
Turn on : 51.5579
Width : 3.907
Height : 10.245
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

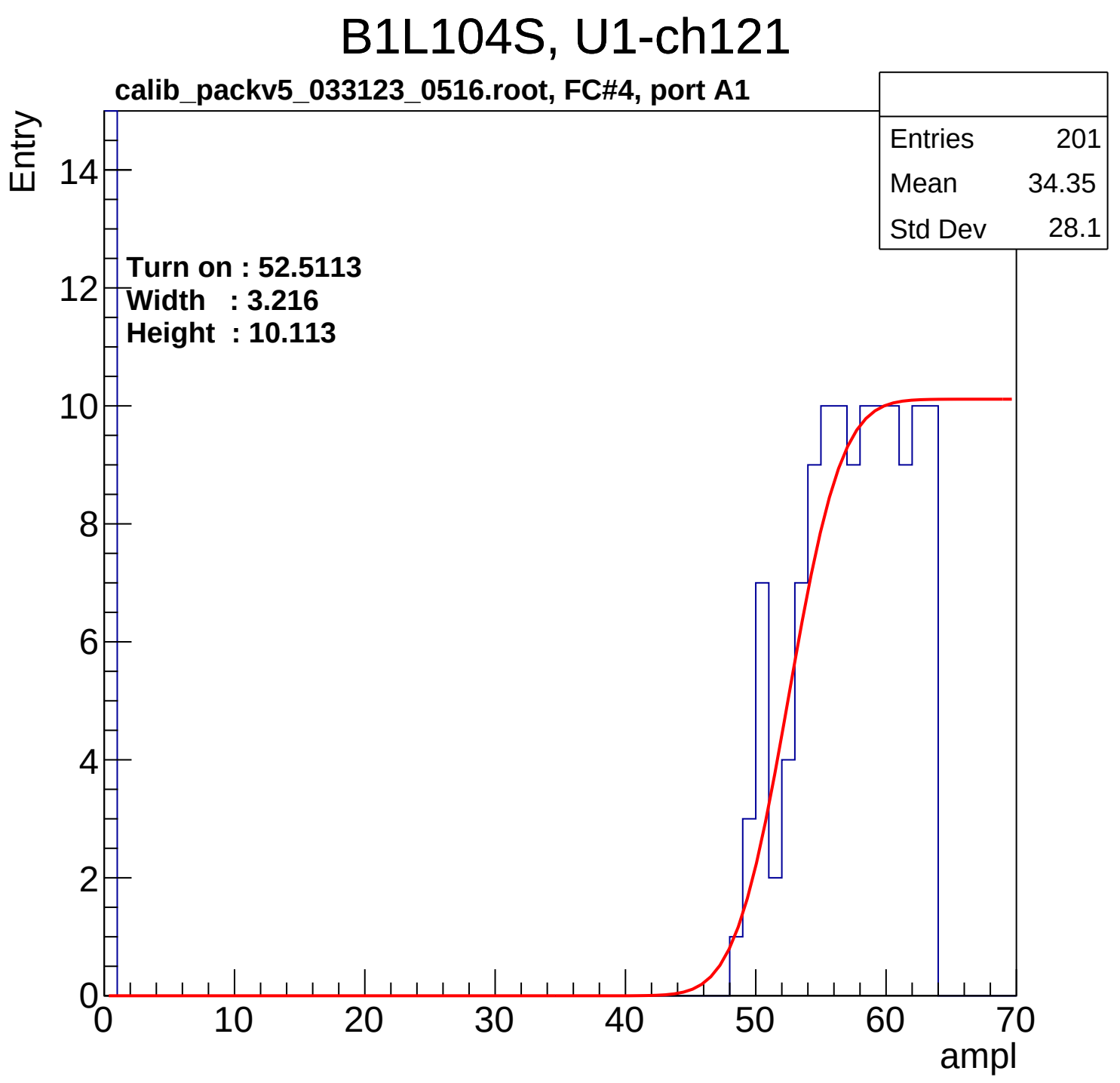

B1L104S, U1-ch116
calib_packv5_033123_0516.root, FC#4, port A1
Entries 200
Mean 31.62
Std Dev 28.76
Turn on : 53.6125
Width : 3.969
Height : 10.493
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

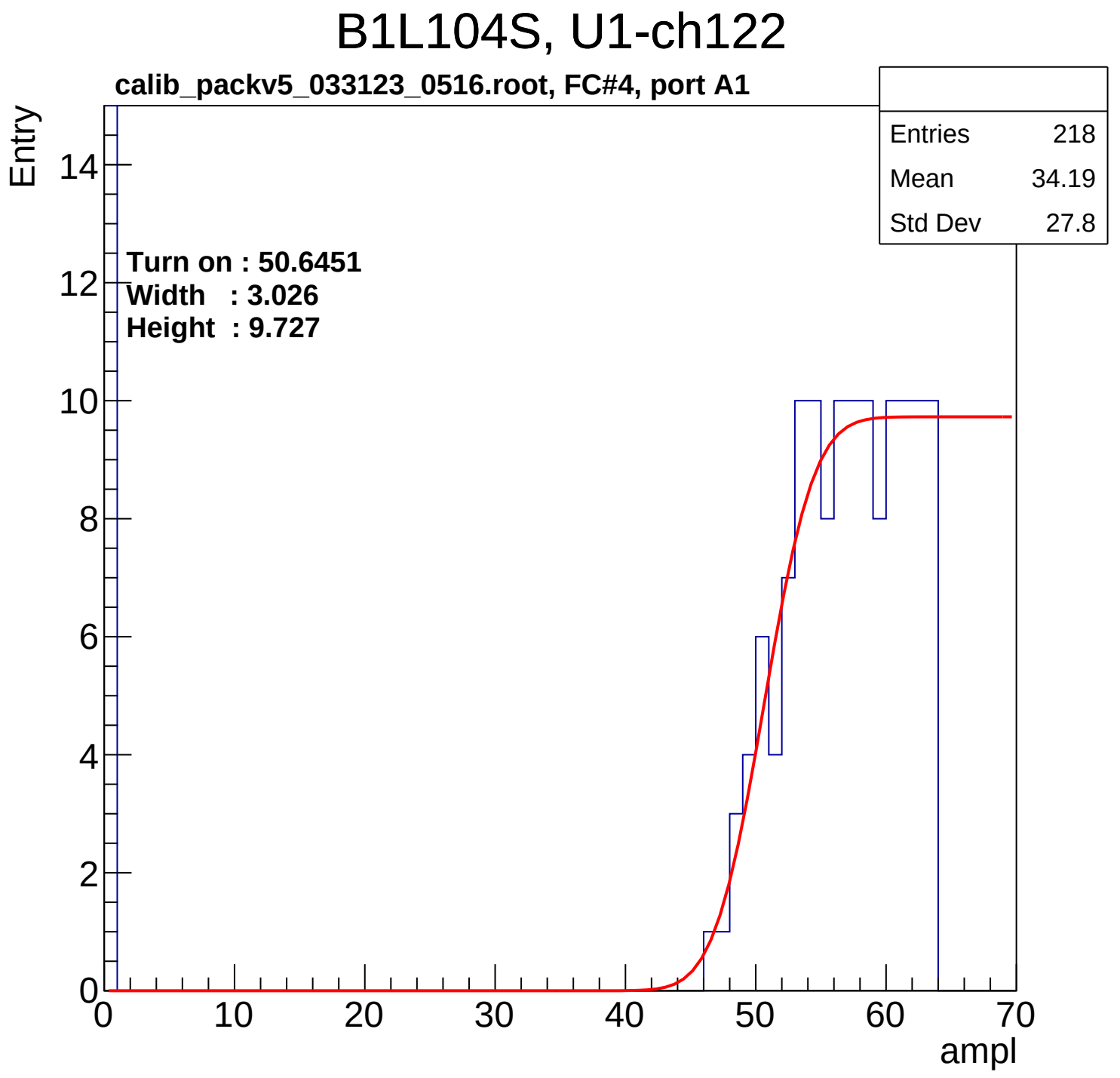

B1L104S, U1-ch117
calib_packv5_033123_0516.root, FC#4, port A1
Entries 206
Mean 36.22
Std Dev 27.34
Turn on : 50.5731
Width : 3.333
Height : 9.906
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

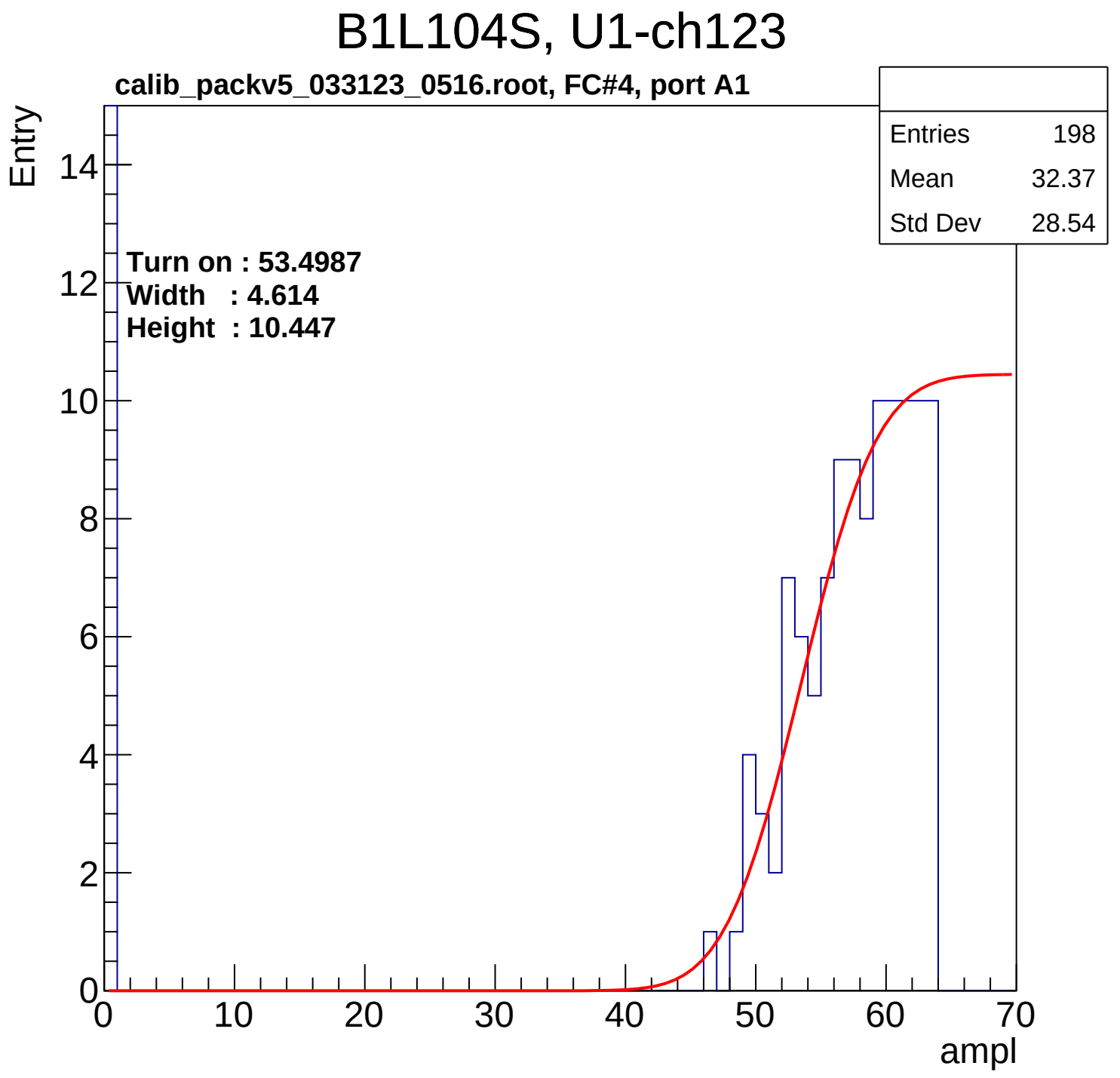

B1L104S, U1-ch118
calib_packv5_033123_0516.root, FC#4, port A1
Entries 242
Mean 29.64
Std Dev 28.59
Turn on : 51.1235
Width : 2.411
Height : 9.734
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

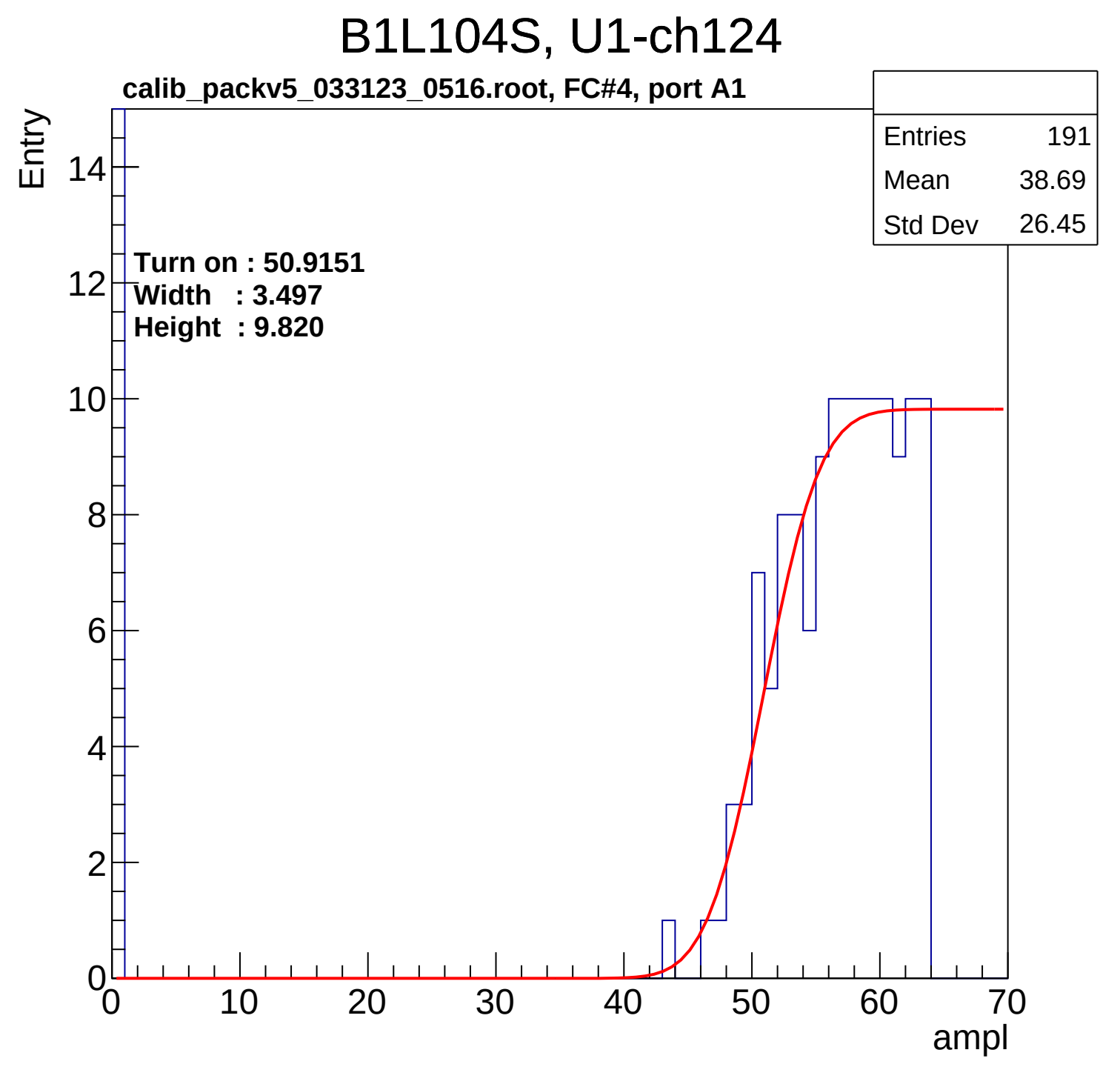

B1L104S, U1-ch119
calib_packv5_033123_0516.root, FC#4, port A1
Entries 204
Mean 33.4
Std Dev 28.14
Turn on : 51.8800
Width : 4.947
Height : 10.070
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

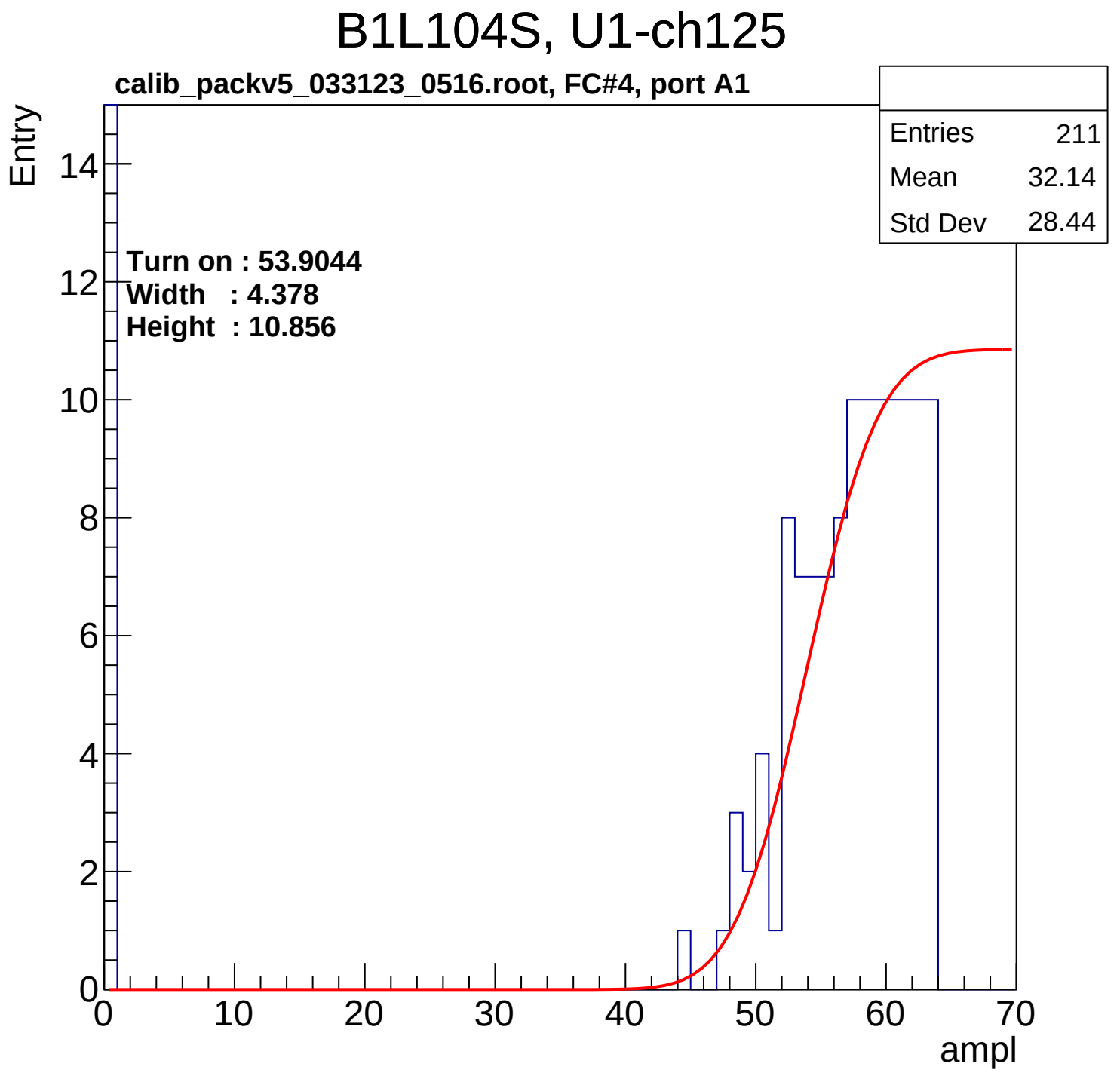

B1L104S, U1-ch120
calib_packv5_033123_0516.root, FC#4, port A1
Entries 215
Mean 32.22
Std Dev 28.17
Turn on : 52.3245
Width : 3.432
Height : 10.057
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

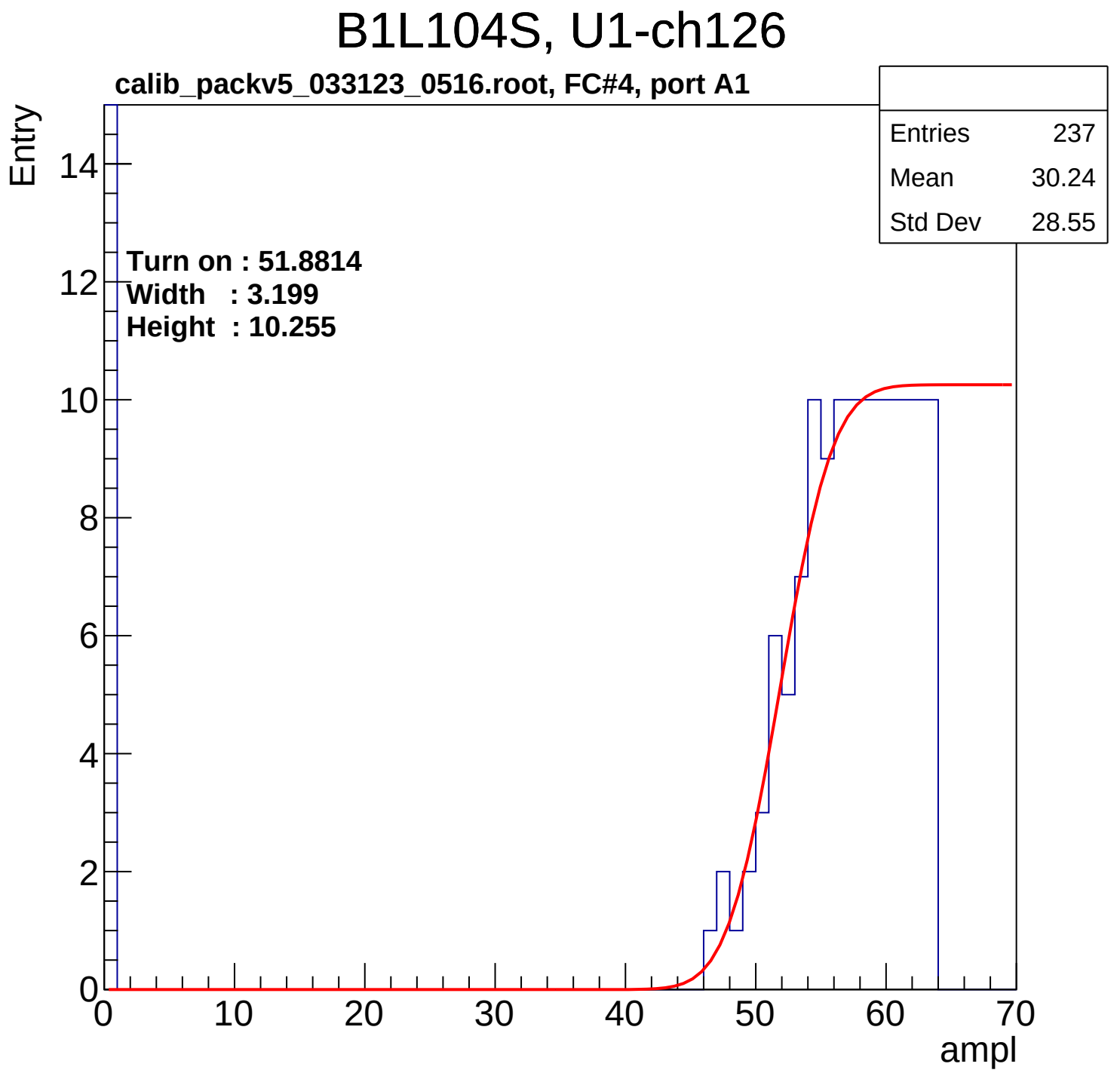

B1L104S, U1-ch121
calib_packv5_033123_0516.root, FC#4, port A1
Entries 201
Mean 34.35
Std Dev 28.1
Turn on : 52.5113
Width : 3.216
Height : 10.113
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

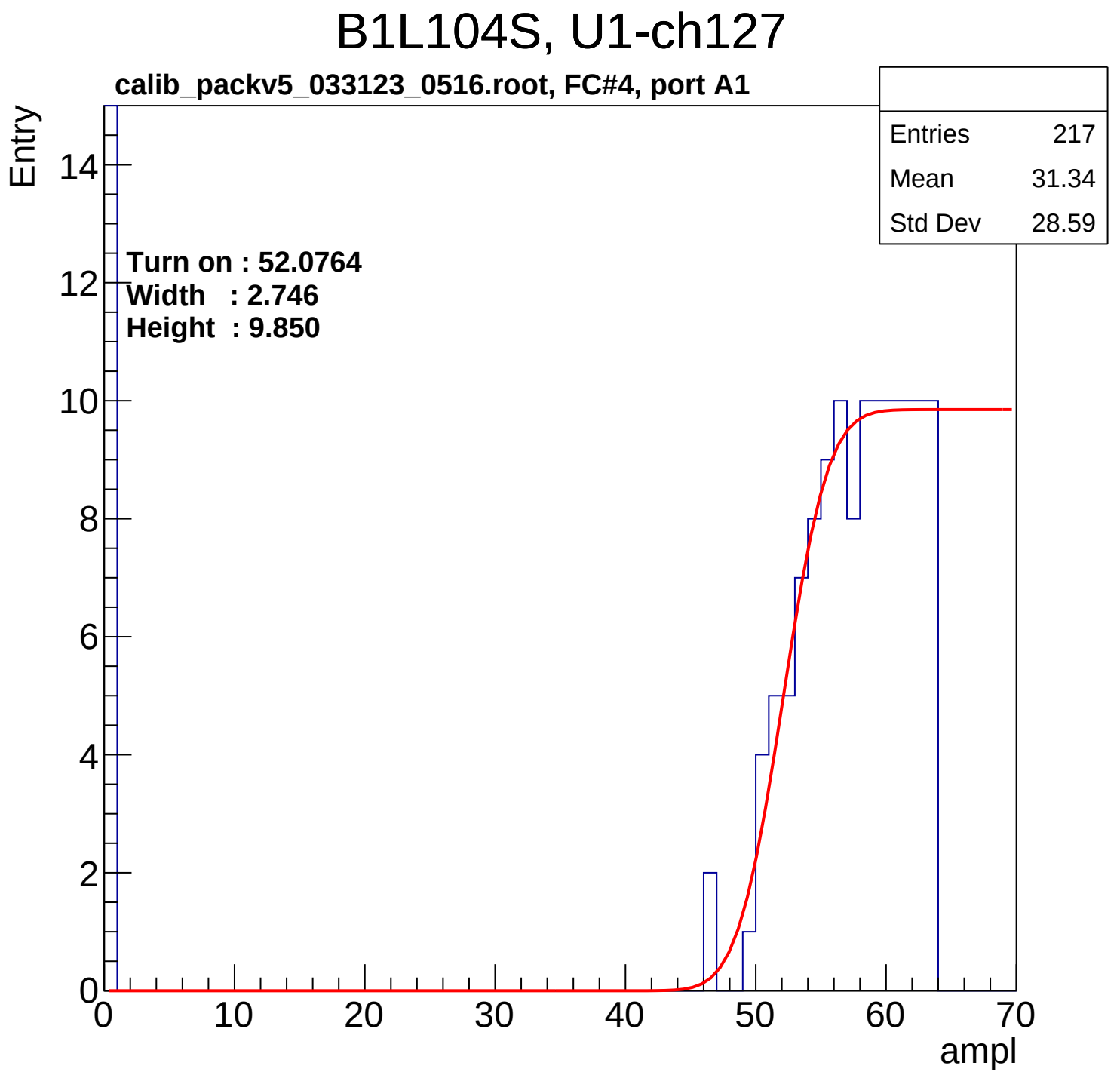

B1L104S, U1-ch122
calib_packv5_033123_0516.root, FC#4, port A1
Entries 218
Mean 34.19
Std Dev 27.8
Turn on : 50.6451
Width : 3.026
Height : 9.727
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

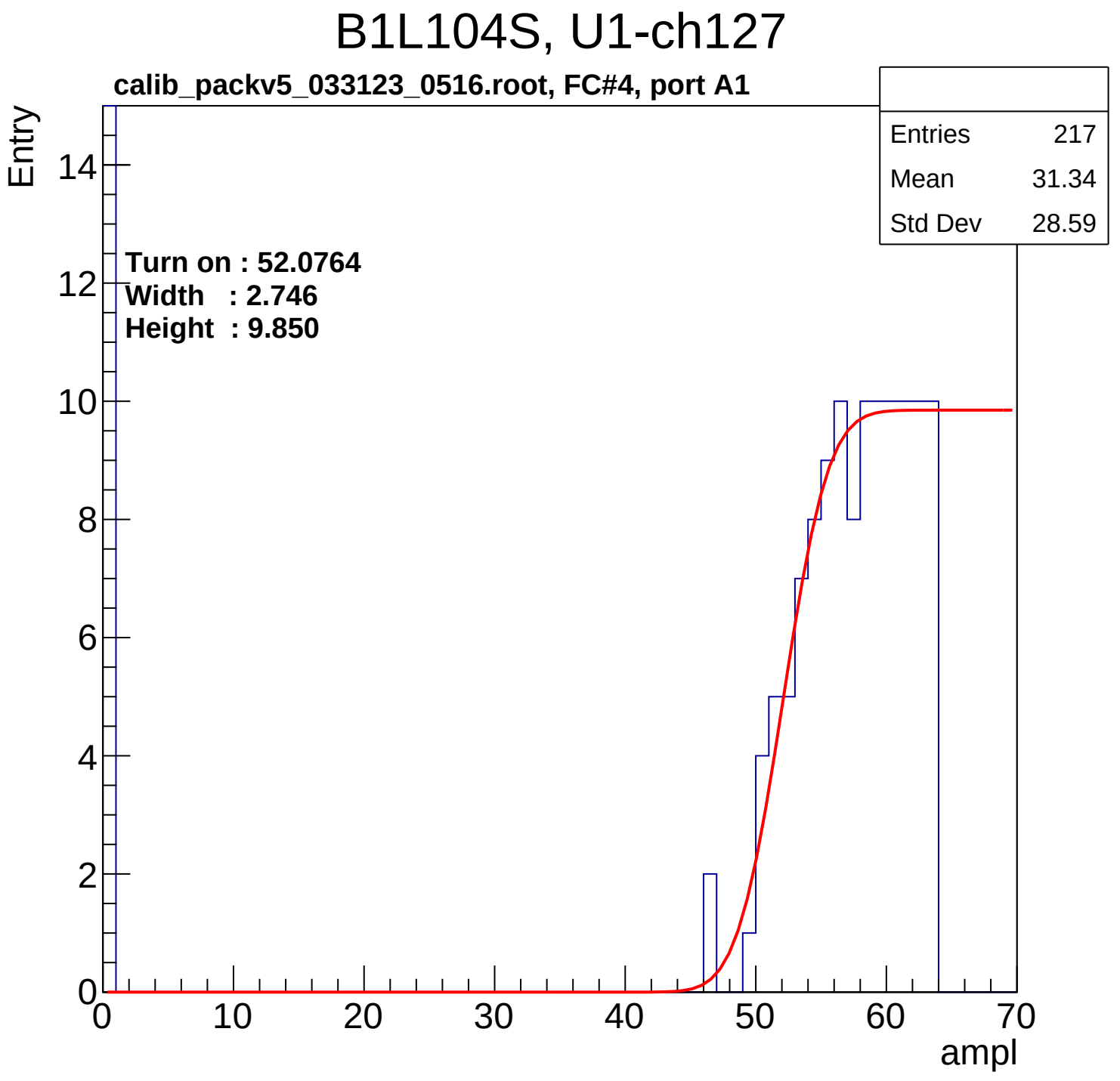

B1L104S, U1-ch123
calib_packv5_033123_0516.root, FC#4, port A1
Entries 198
Mean 32.37
Std Dev 28.54
Turn on : 53.4987
Width : 4.614
Height : 10.447
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L104S, U1-ch124
calib_packv5_033123_0516.root, FC#4, port A1
Entries 191
Mean 38.69
Std Dev 26.45
Turn on : 50.9151
Width : 3.497
Height : 9.820
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L104S, U1-ch125
calib_packv5_033123_0516.root, FC#4, port A1
Entries 211
Mean 32.14
Std Dev 28.44
Turn on : 53.9044
Width : 4.378
Height : 10.856
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L104S, U1-ch126
calib_packv5_033123_0516.root, FC#4, port A1
Entries 237
Mean 30.24
Std Dev 28.55
Turn on : 51.8814
Width : 3.199
Height : 10.255
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L104S, U1-ch127
calib_packv5_033123_0516.root, FC#4, port A1
Entries 217
Mean 31.34
Std Dev 28.59
Turn on : 52.0764
Width : 2.746
Height : 9.850
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L104S, U1-ch127
calib_packv5_033123_0516.root, FC#4, port A1
Entries 217
Mean 31.34
Std Dev 28.59
Turn on : 52.0764
Width : 2.746
Height : 9.850
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70