



# B1L103S, U11-ch0, adc0

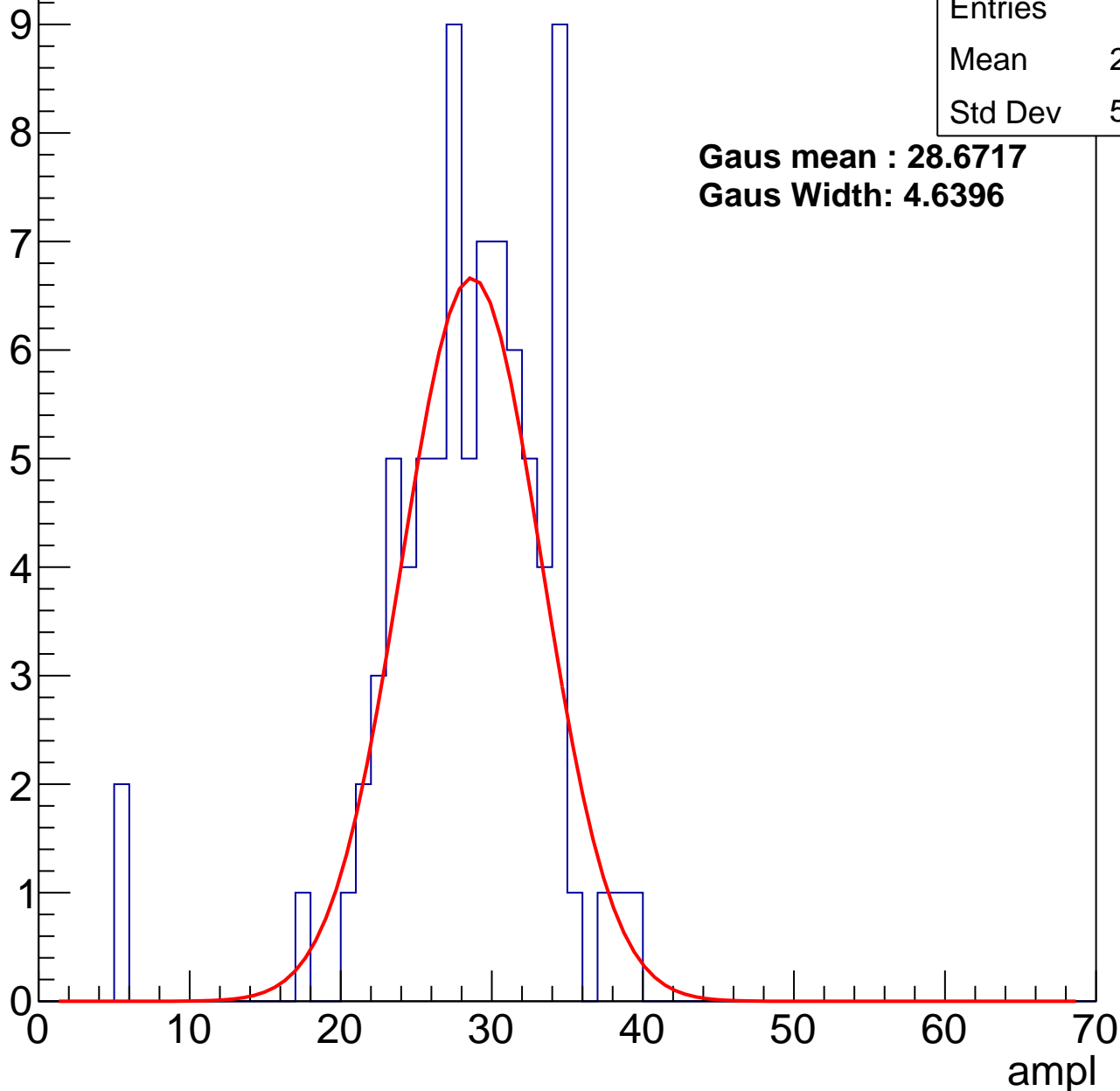
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	84
Mean	27.98
Std Dev	5.623

**Gaus mean : 28.6717**

**Gaus Width: 4.6396**



# B1L103S, U11-ch0, adc1

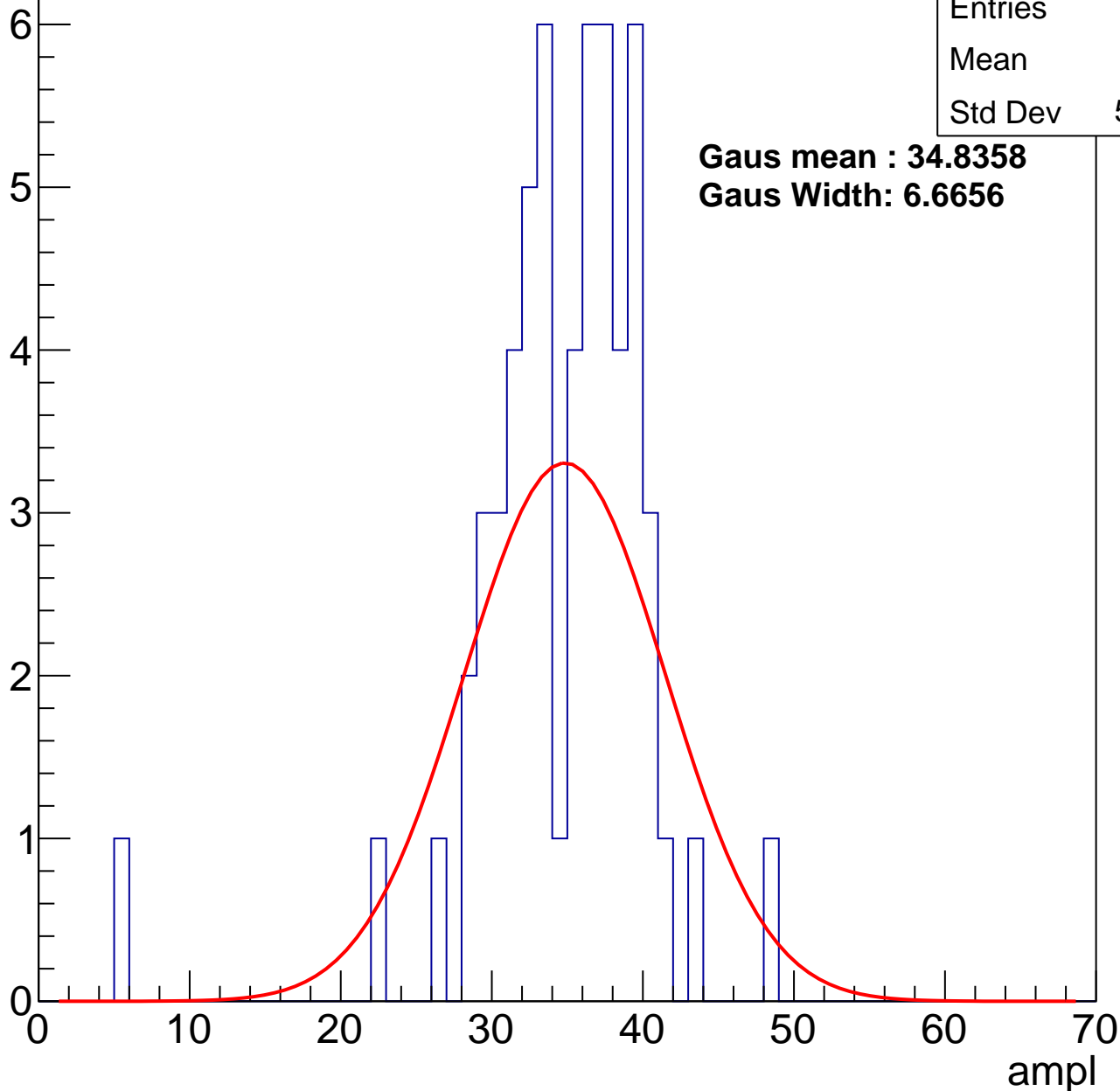
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	59
Mean	34.2
Std Dev	5.871

**Gaus mean : 34.8358**

**Gaus Width: 6.6656**



# B1L103S, U11-ch0, adc2

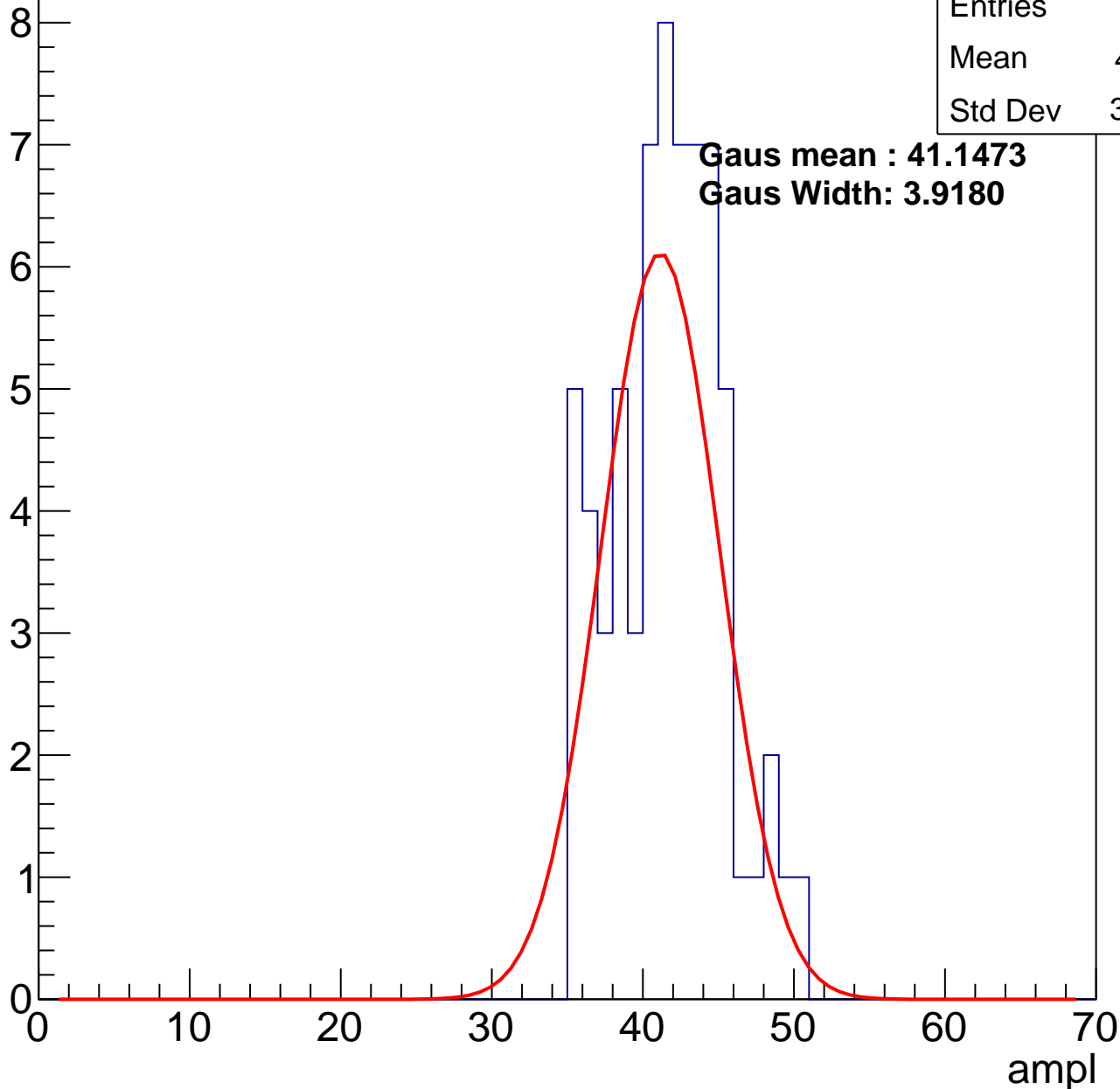
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	41.21
Std Dev	3.606

**Gaus mean : 41.1473**

**Gaus Width: 3.9180**

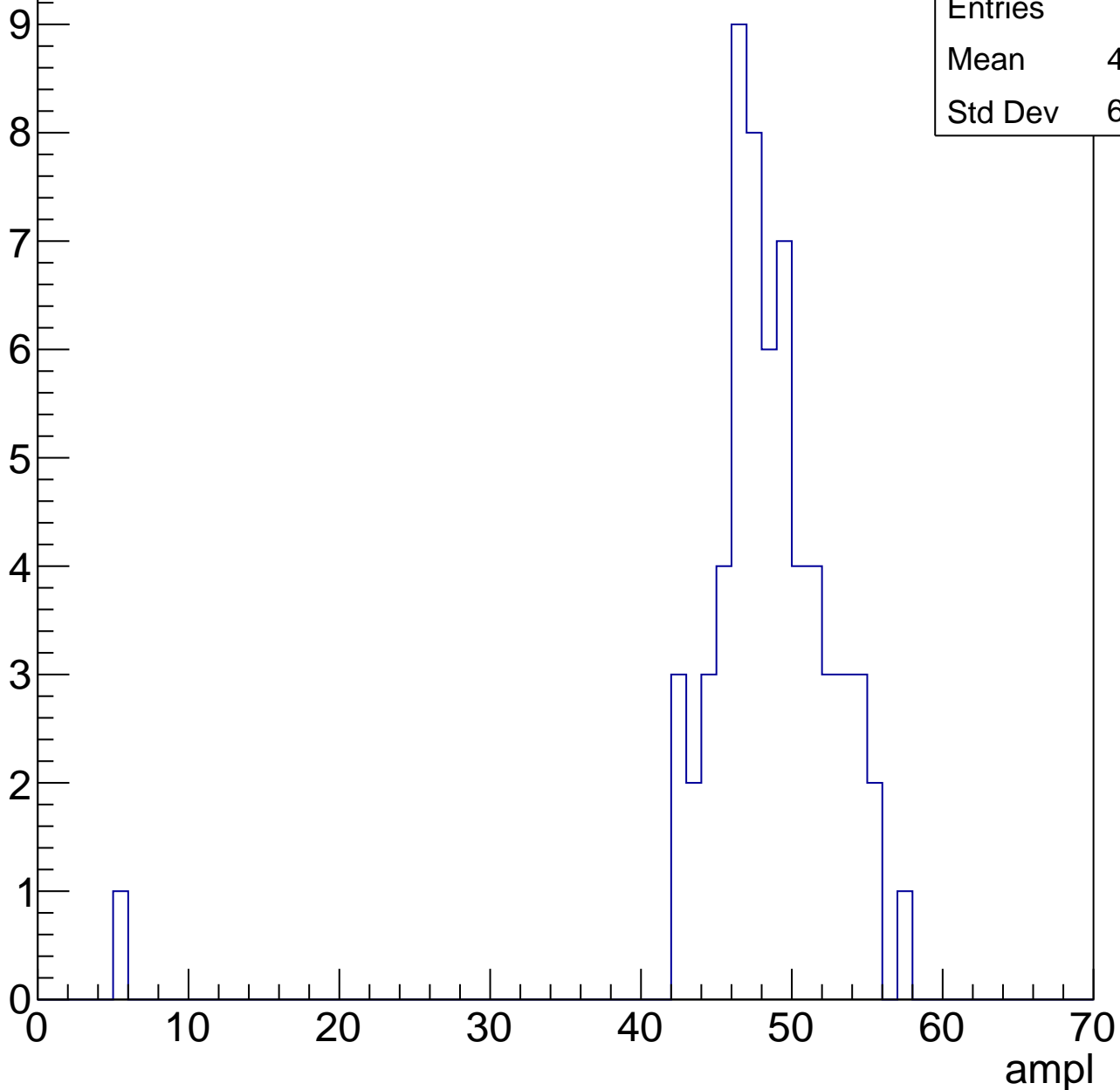


# B1L103S, U11-ch0, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	47.59
Std Dev	6.416

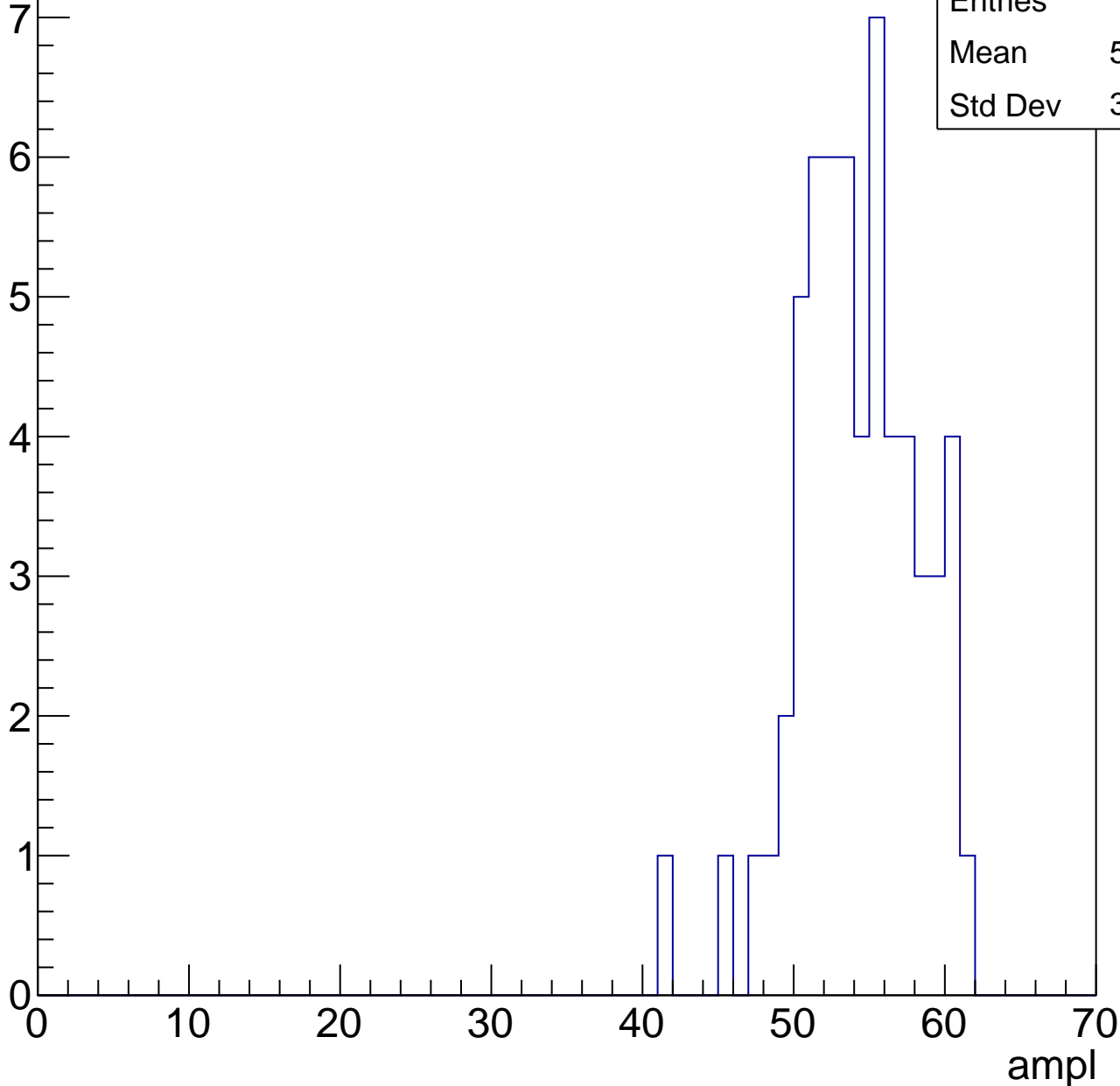


# B1L103S, U11-ch0, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	59
Mean	53.73
Std Dev	3.948

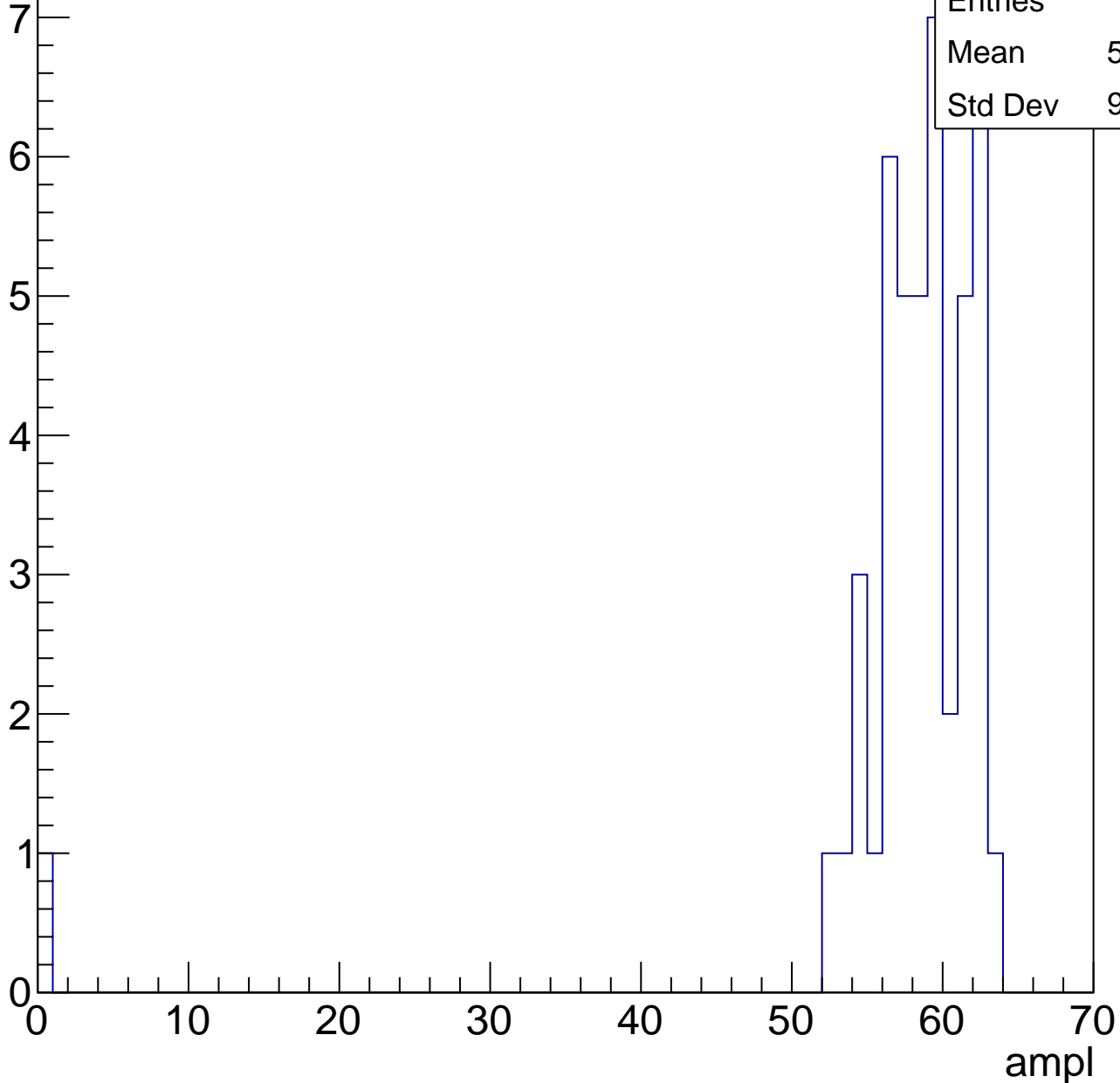


# B1L103S, U11-ch0, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	45
Mean	57.07
Std Dev	9.029

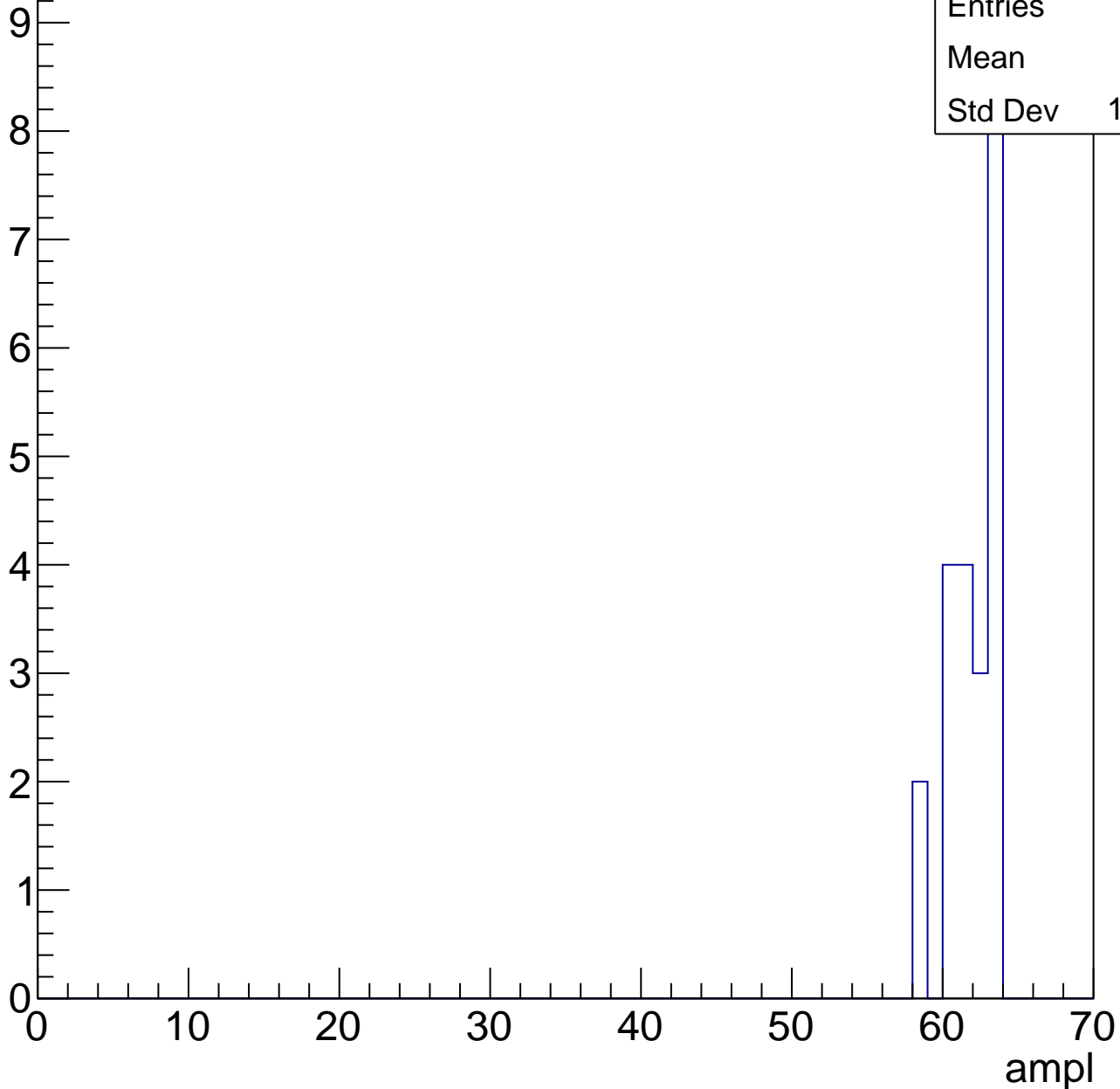


# B1L103S, U11-ch0, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	22
Mean	61.5
Std Dev	1.588

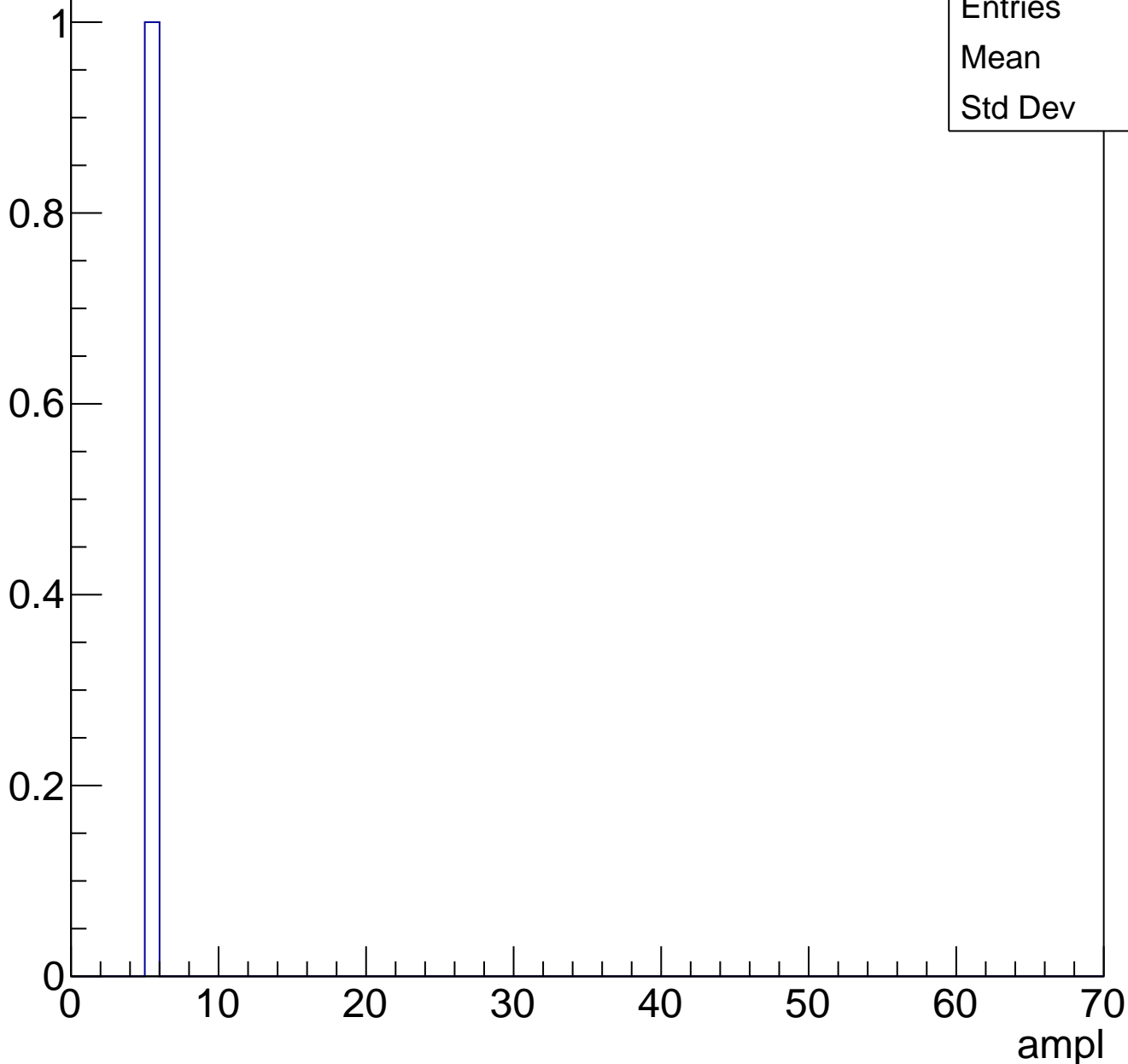




# B1L103S, U11-ch0, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U11-ch1, adc0

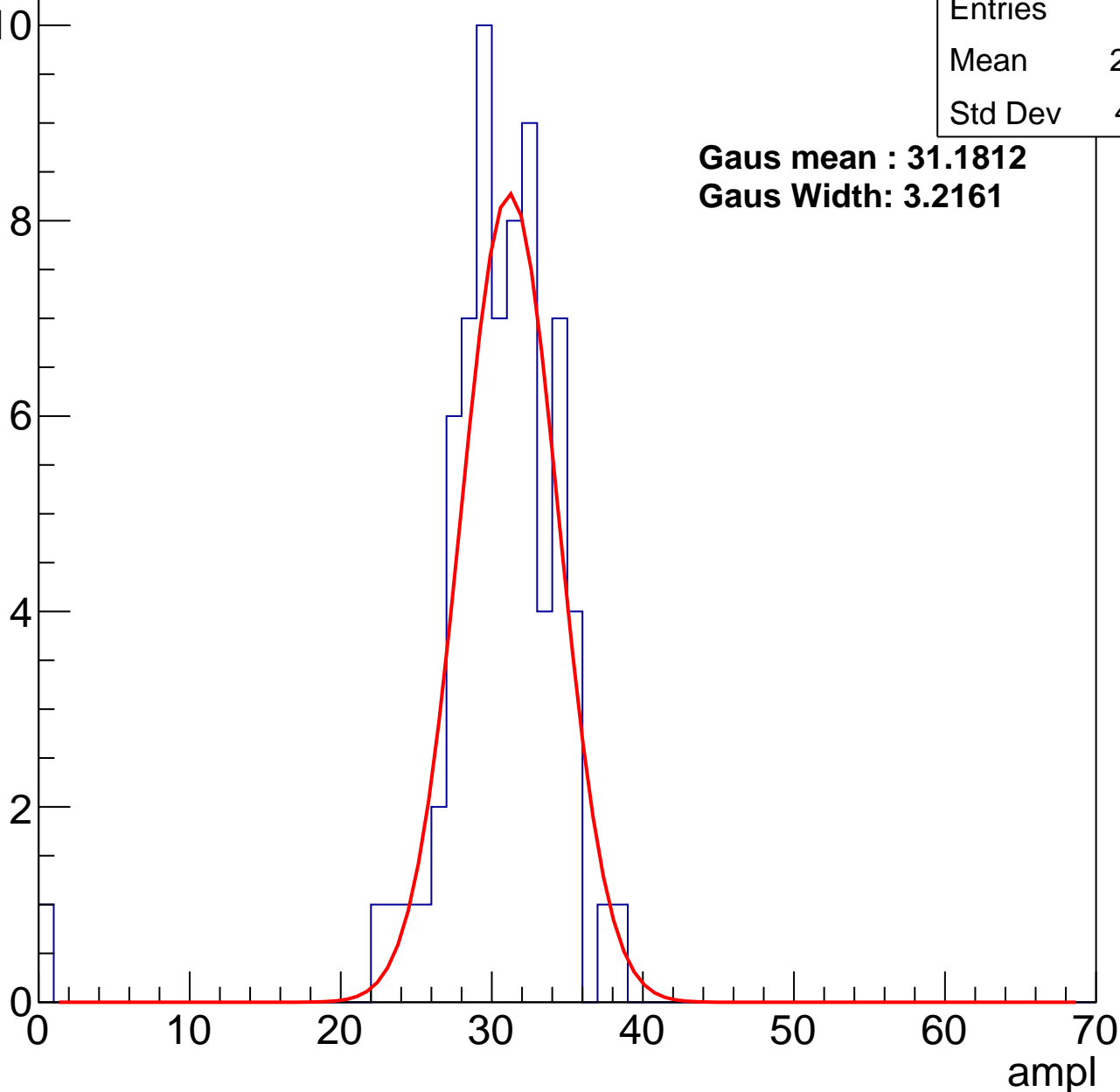
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	71
Mean	29.93
Std Dev	4.751

**Gaus mean : 31.1812**

**Gaus Width: 3.2161**



# B1L103S, U11-ch1, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	68
Mean	38.1
Std Dev	3.348

**Gaus mean : 38.2061**

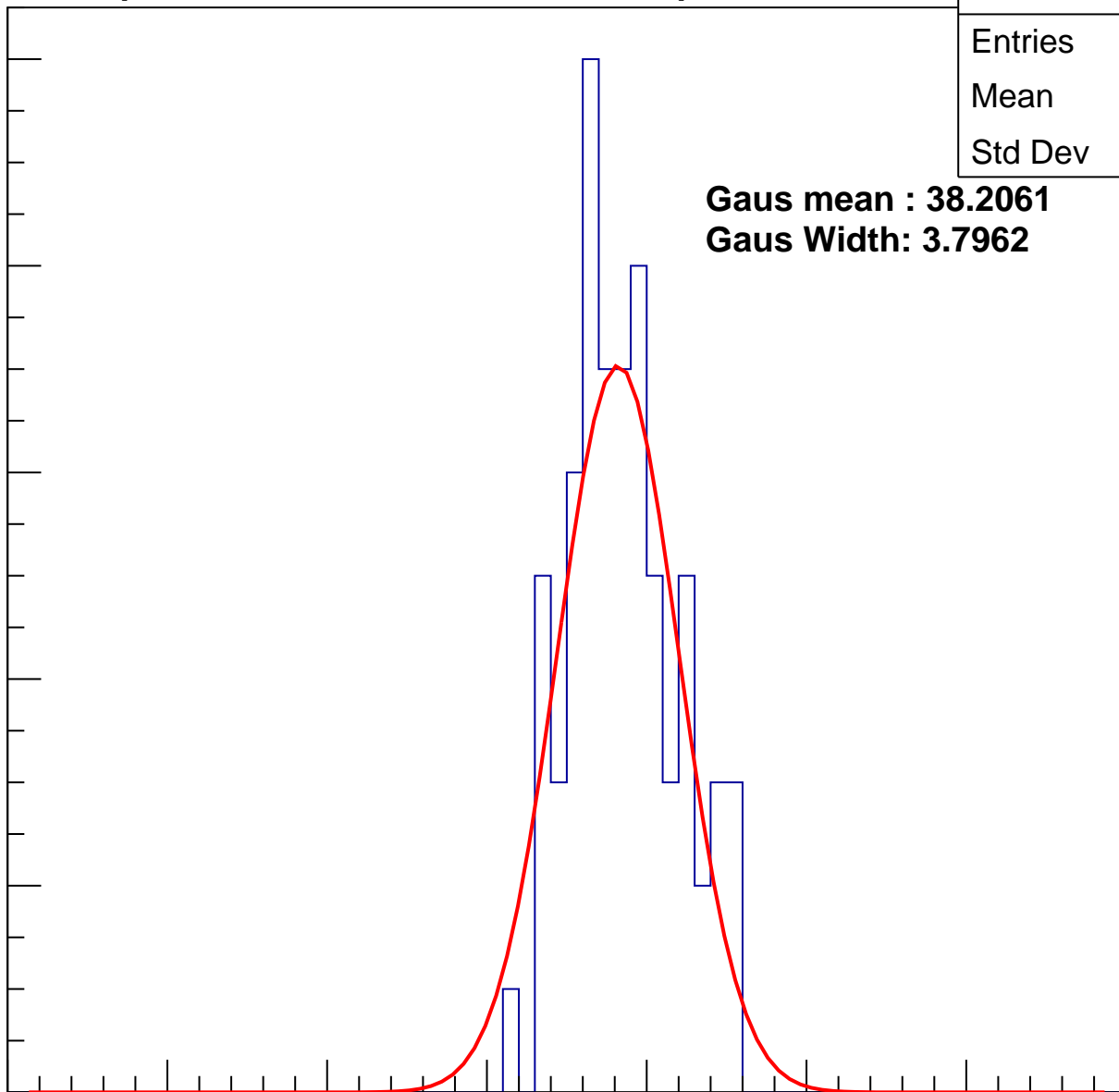
**Gaus Width: 3.7962**

Entry

10  
8  
6  
4  
2  
0

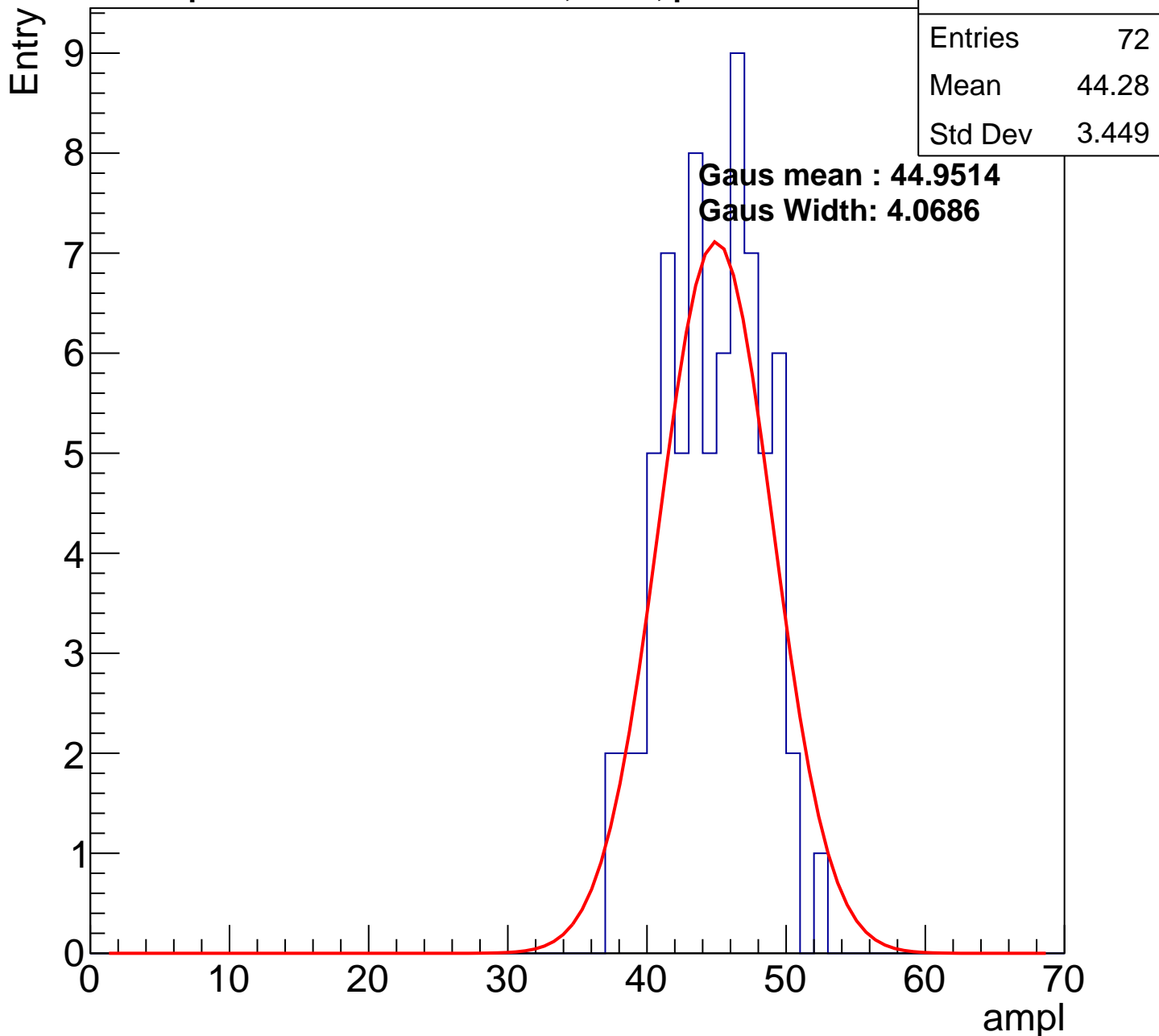
0 10 20 30 40 50 60 70

ampl



# B1L103S, U11-ch1, adc2

calib\_packv5\_042523\_0143.root, FC#7, port C2

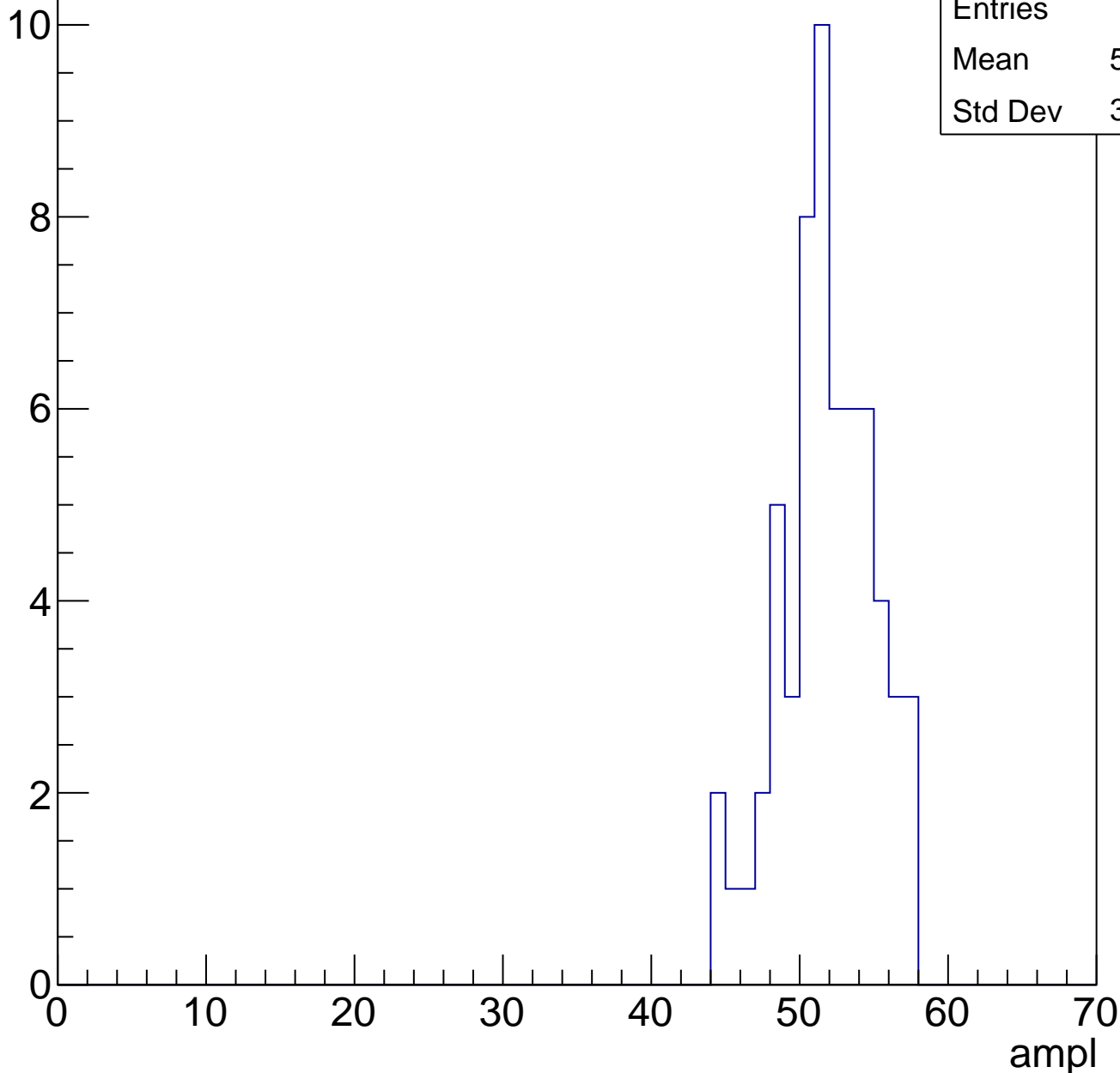


# B1L103S, U11-ch1, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	60
Mean	51.38
Std Dev	3.104

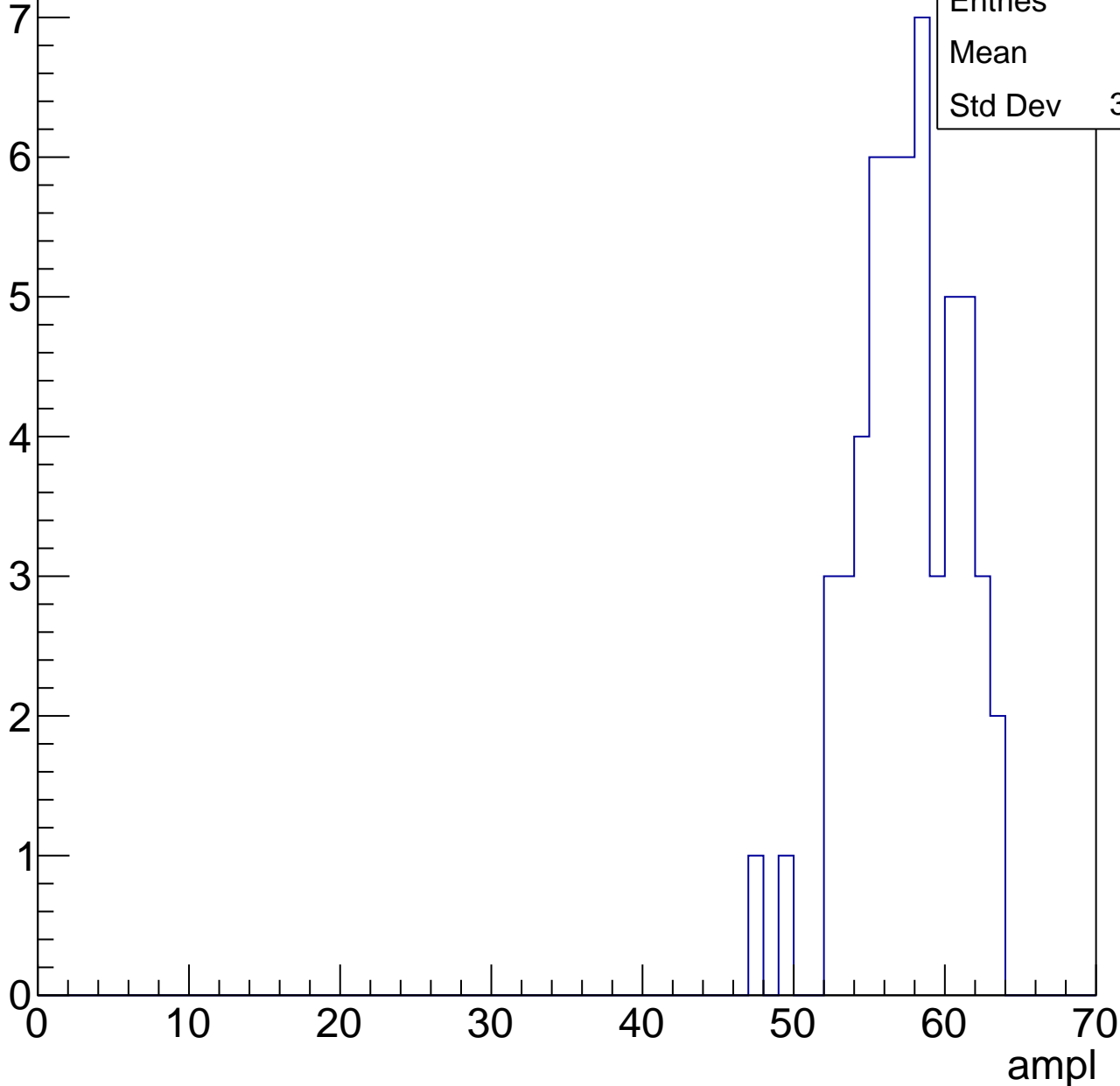


# B1L103S, U11-ch1, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

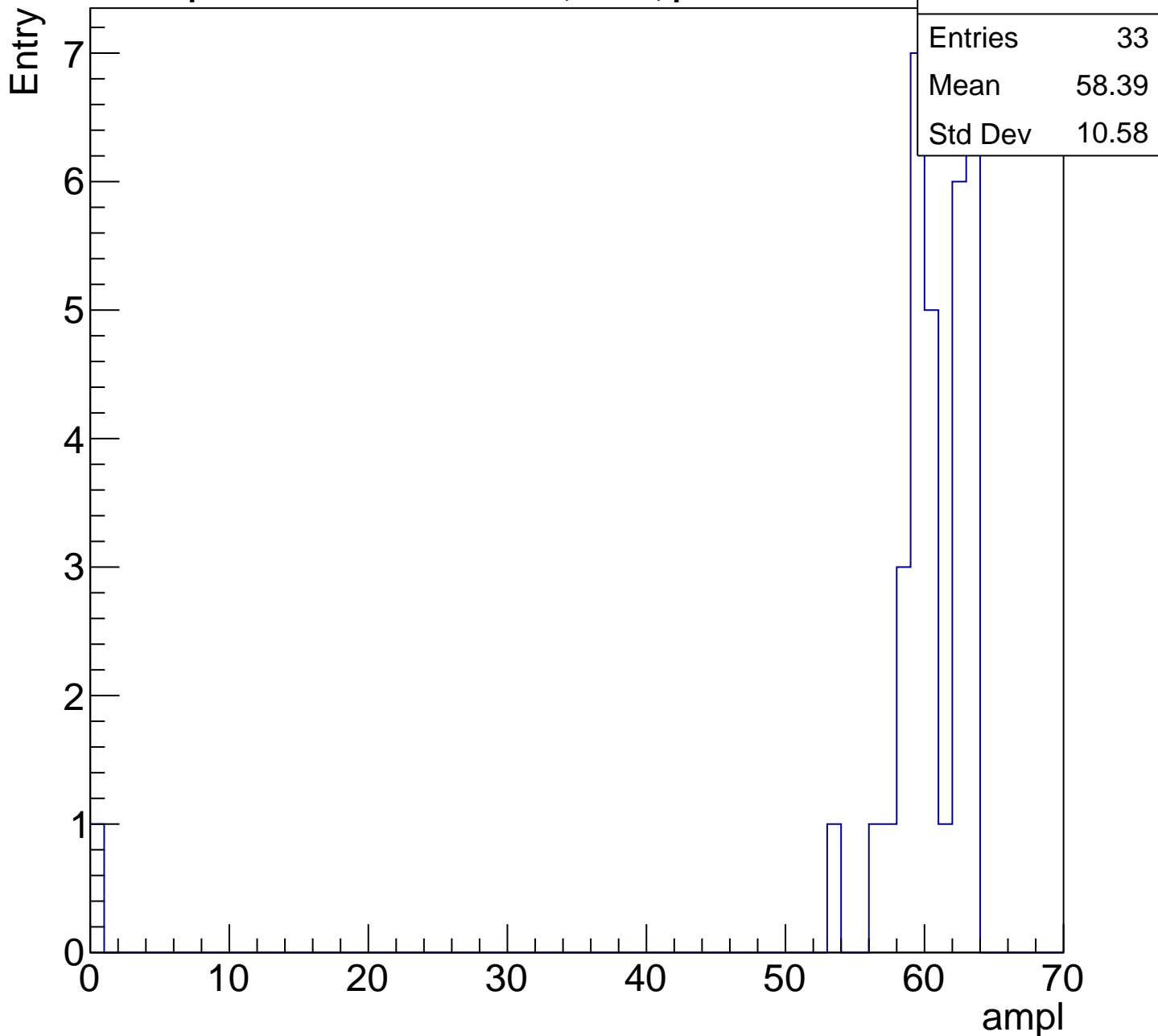
Entry

Entries	55
Mean	57
Std Dev	3.422



# B1L103S, U11-ch1, adc5

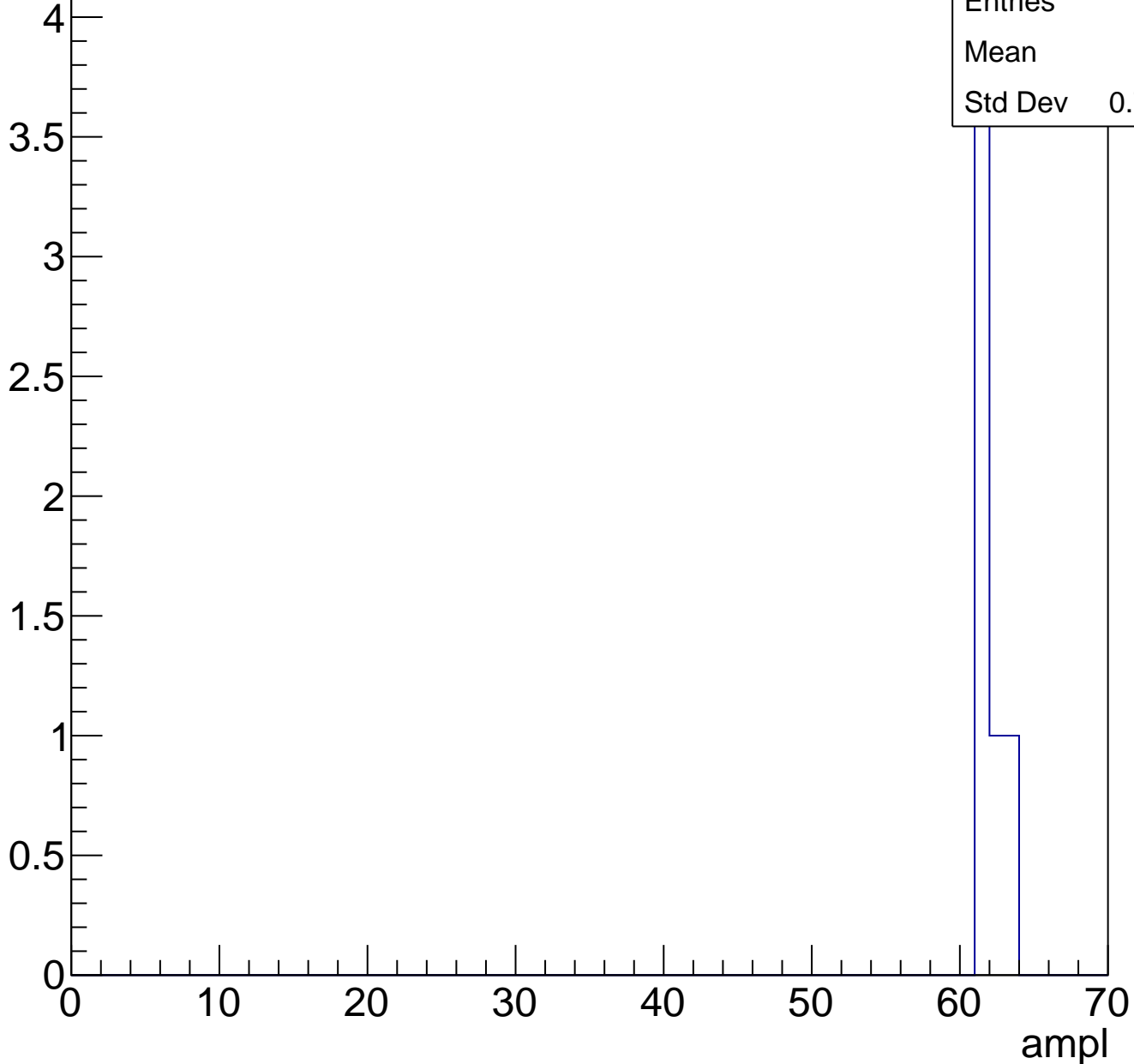
calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U11-ch1, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U11-ch1, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L103S, U11-ch2, adc0

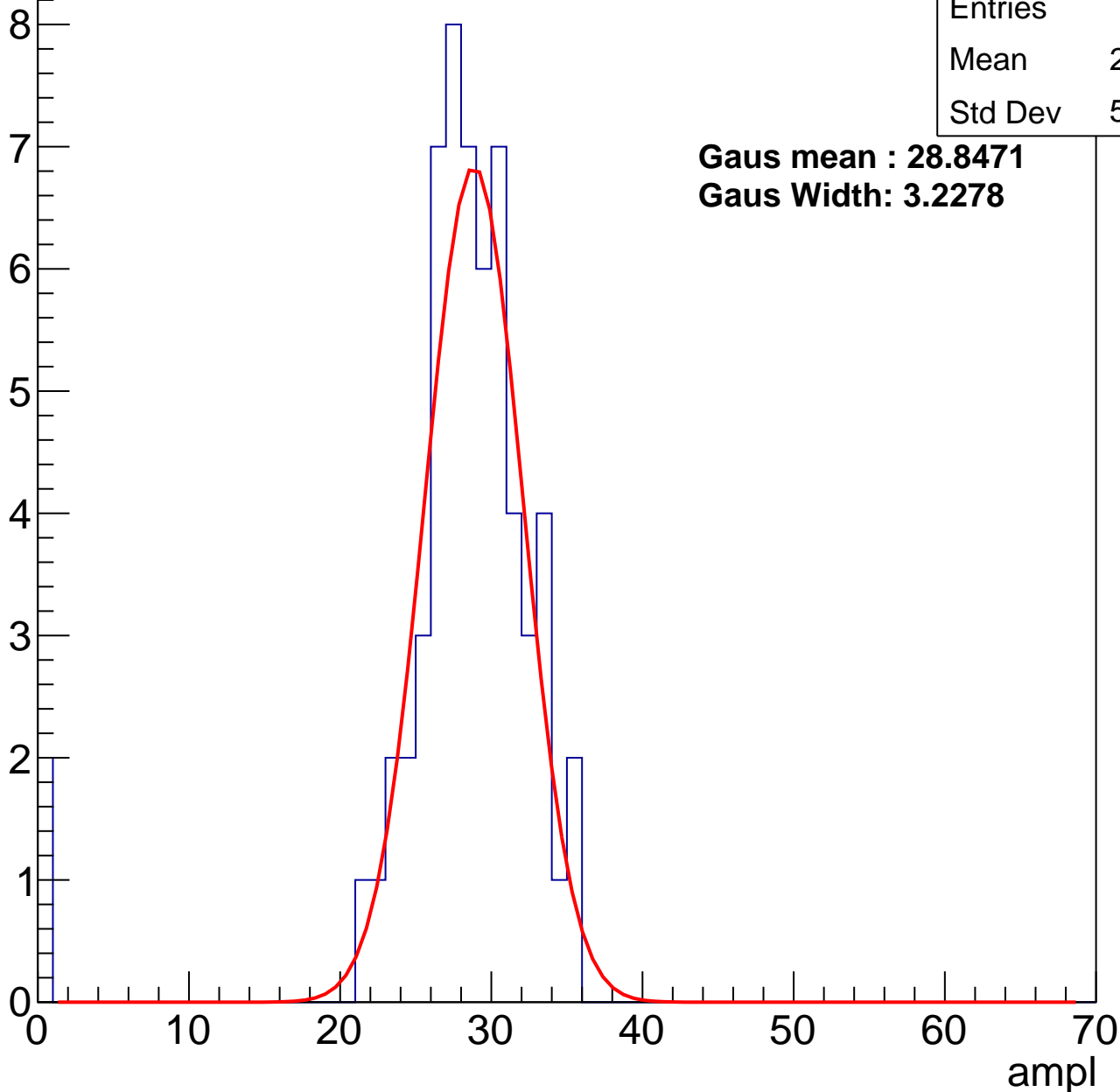
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	60
Mean	27.43
Std Dev	5.959

**Gaus mean : 28.8471**

**Gaus Width: 3.2278**



# B1L103S, U11-ch2, adc1

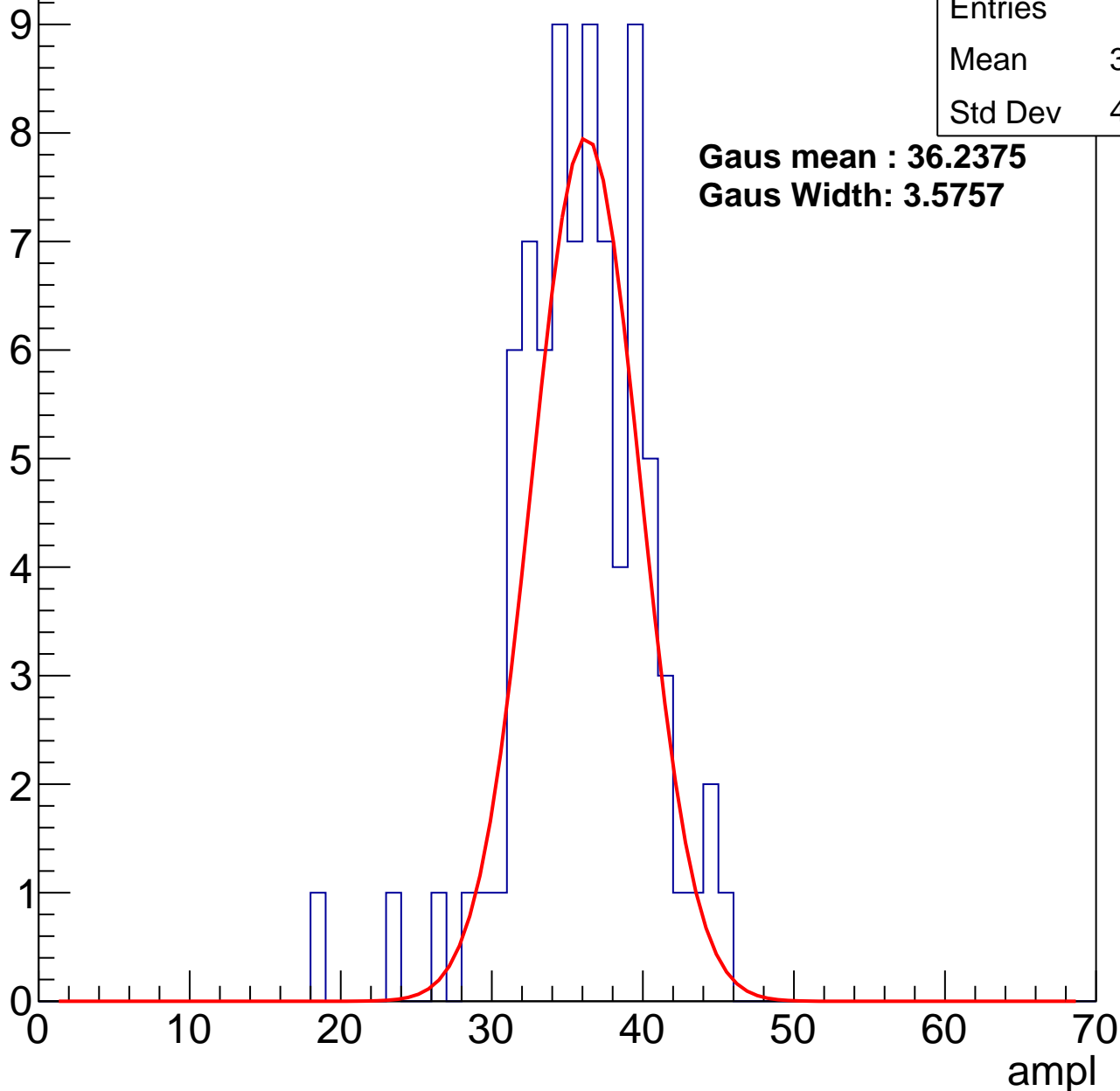
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	83
Mean	35.42
Std Dev	4.426

**Gaus mean : 36.2375**

**Gaus Width: 3.5757**



# B1L103S, U11-ch2, adc2

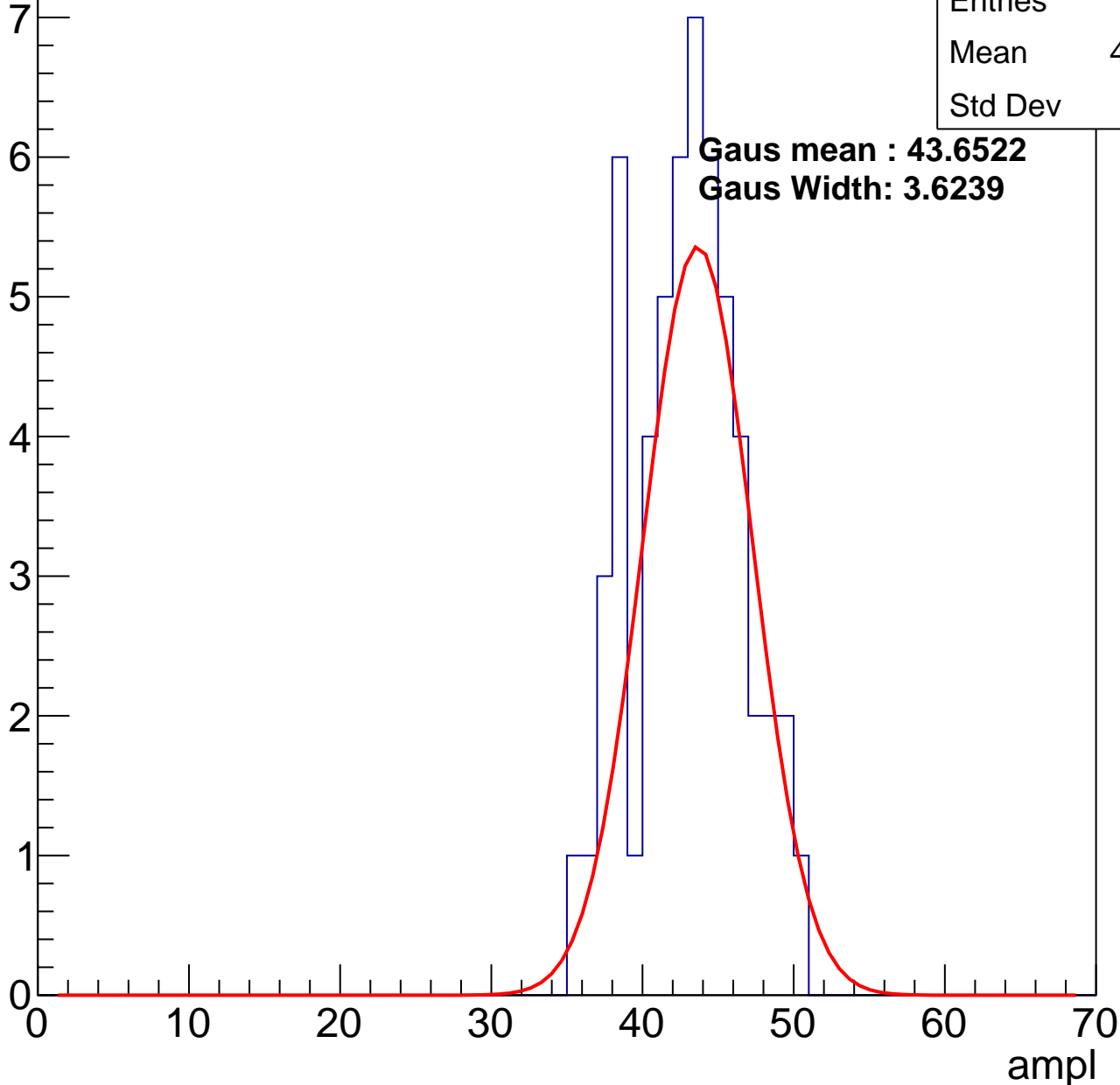
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	56
Mean	42.46
Std Dev	3.53

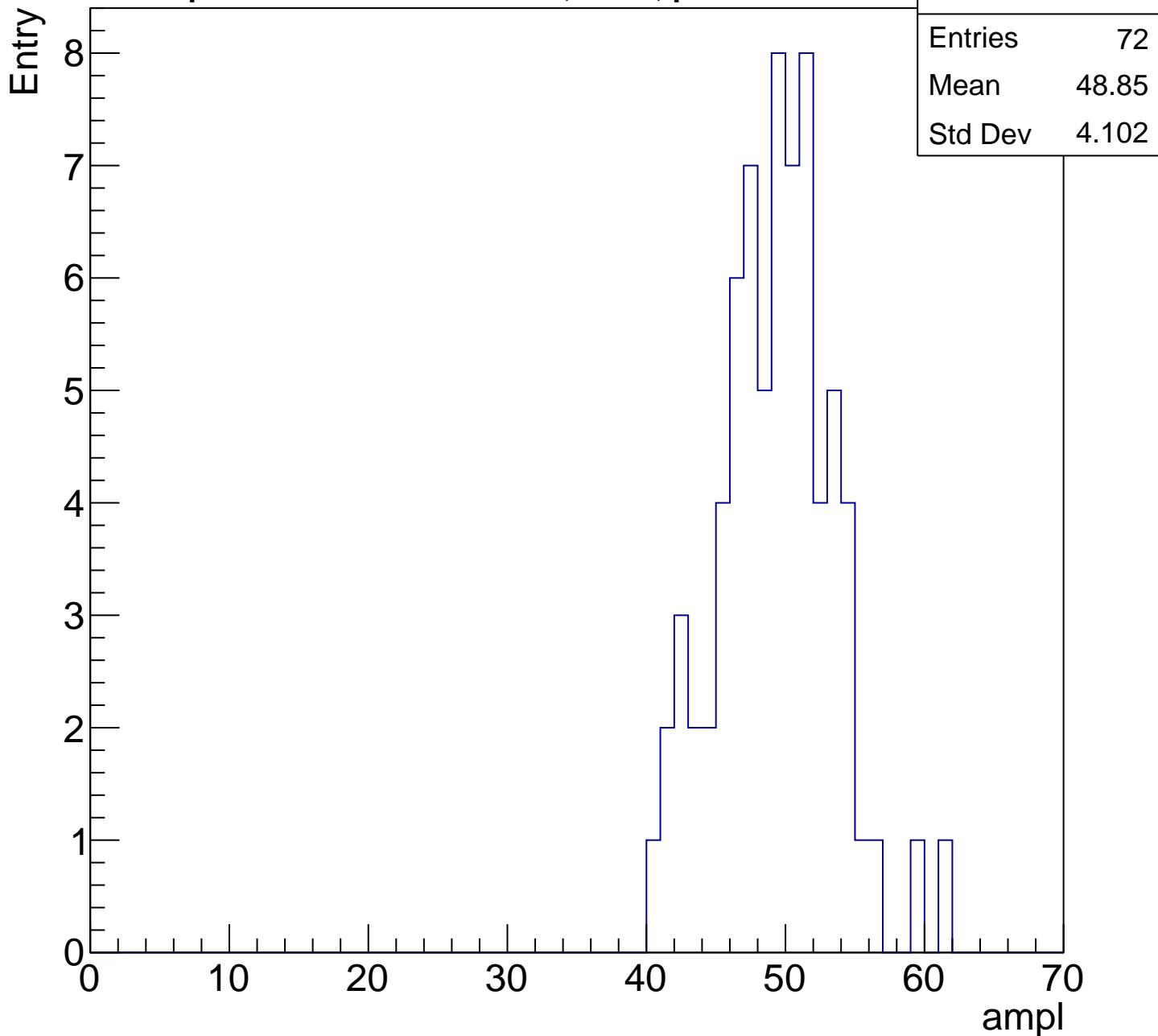
**Gaus mean : 43.6522**

**Gaus Width: 3.6239**



# B1L103S, U11-ch2, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

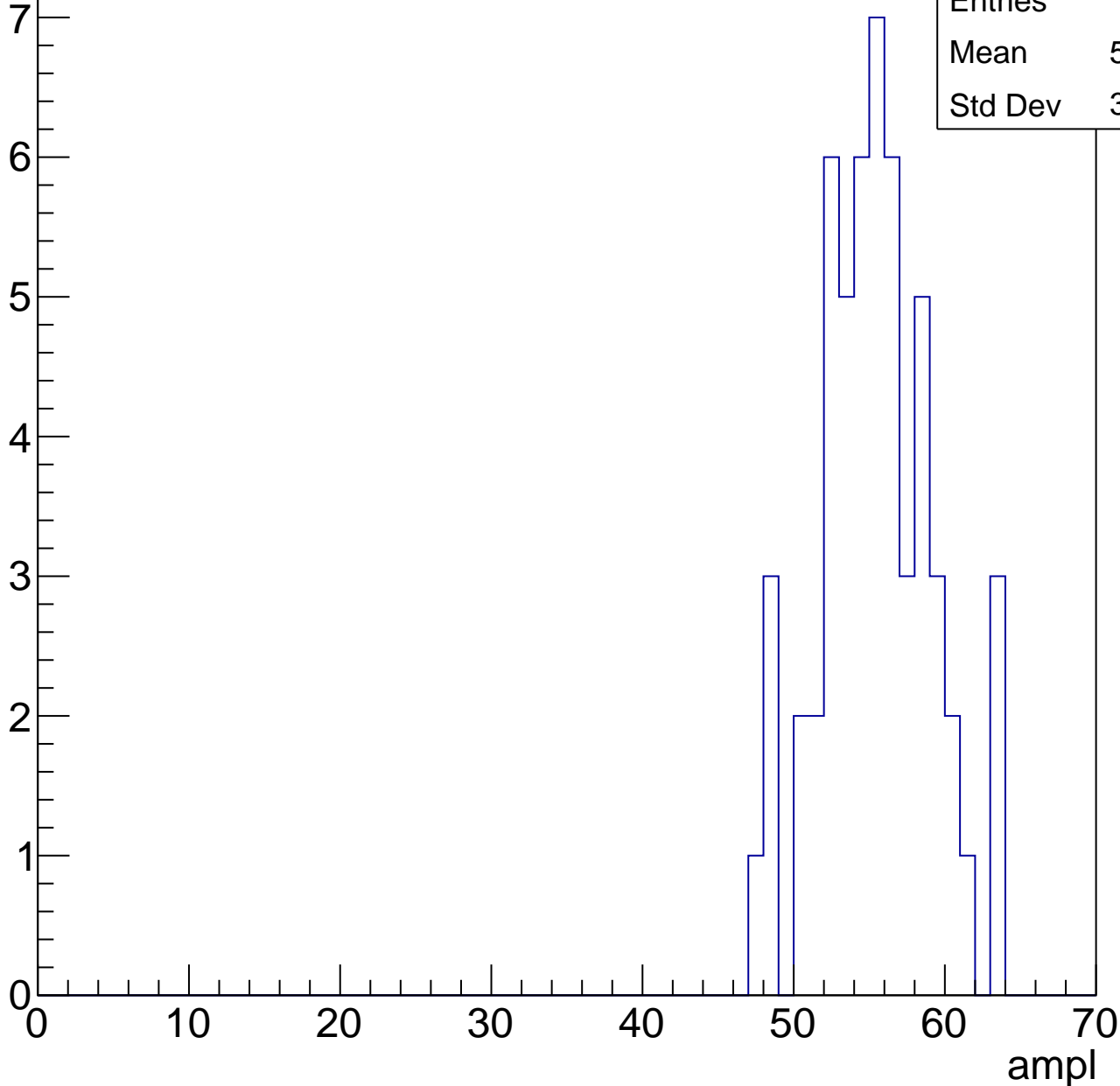


# B1L103S, U11-ch2, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	55
Mean	54.96
Std Dev	3.722

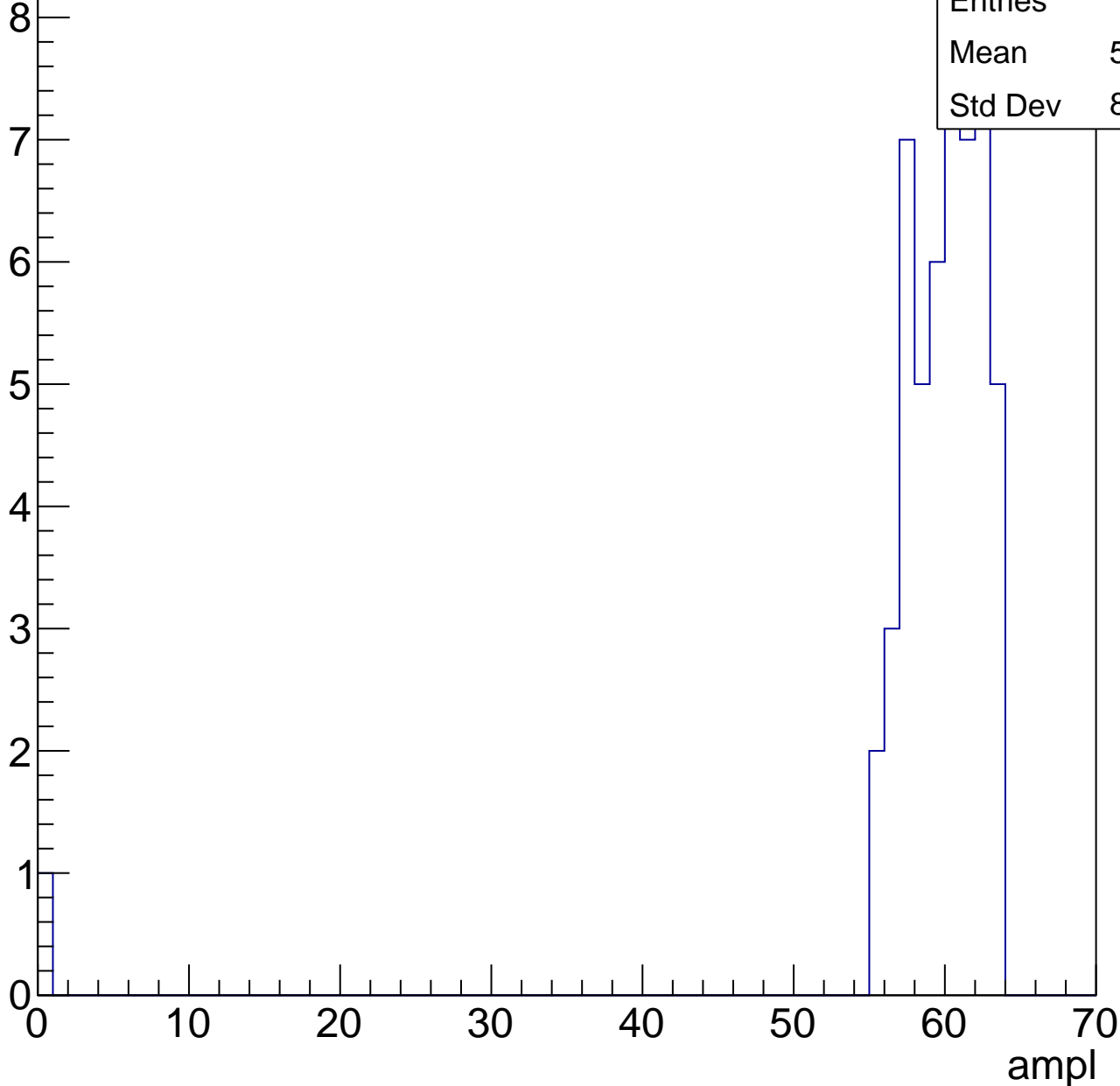


# B1L103S, U11-ch2, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	52
Mean	58.44
Std Dev	8.486



# B1L103S, U11-ch2, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	4
Mean	62
Std Dev	0.7071

ampl

0 10 20 30 40 50 60 70



# B1L103S, U11-ch2, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U11-ch3, adc0

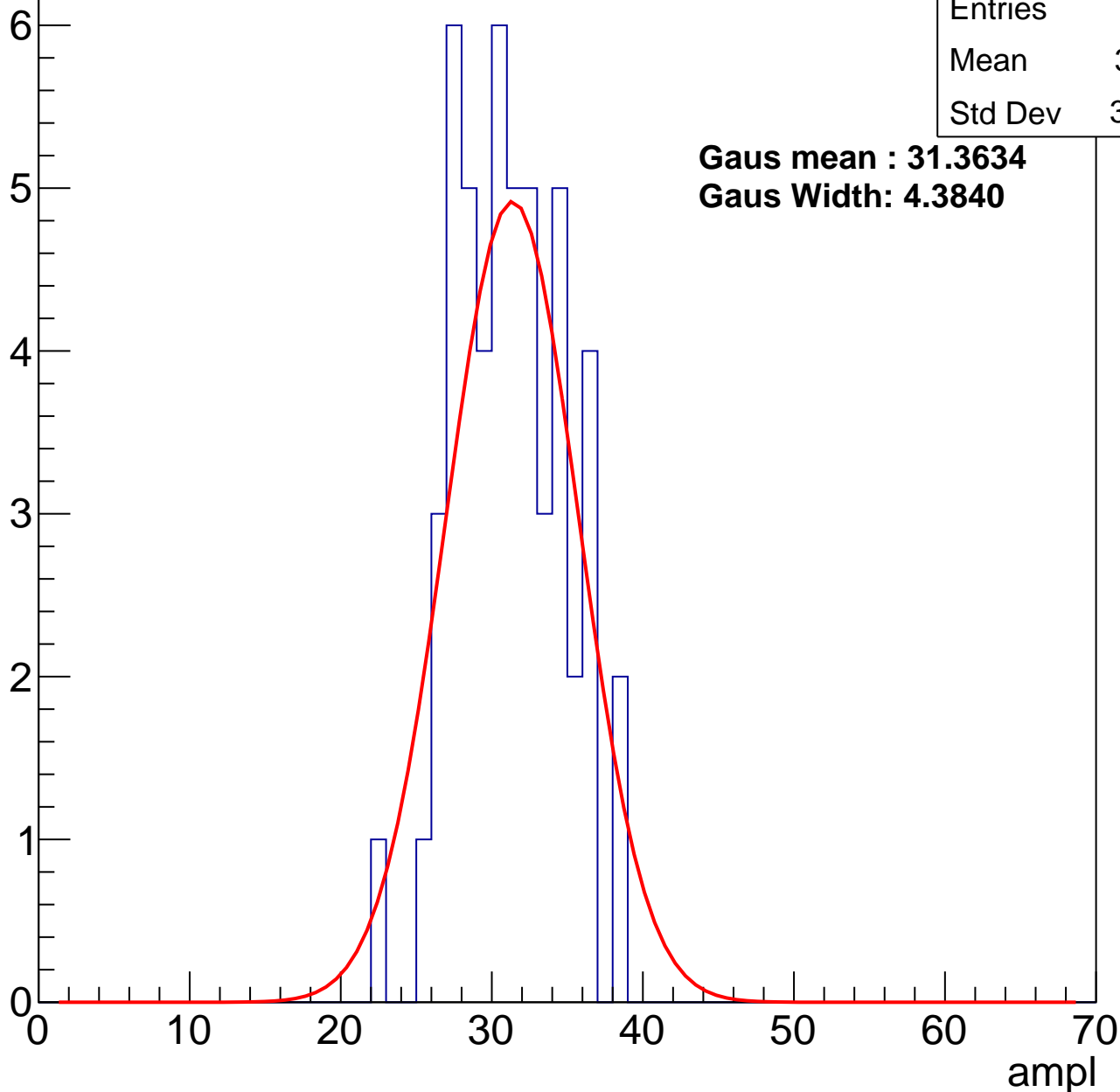
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	52
Mean	30.71
Std Dev	3.516

**Gaus mean : 31.3634**

**Gaus Width: 4.3840**



# B1L103S, U11-ch3, adc1

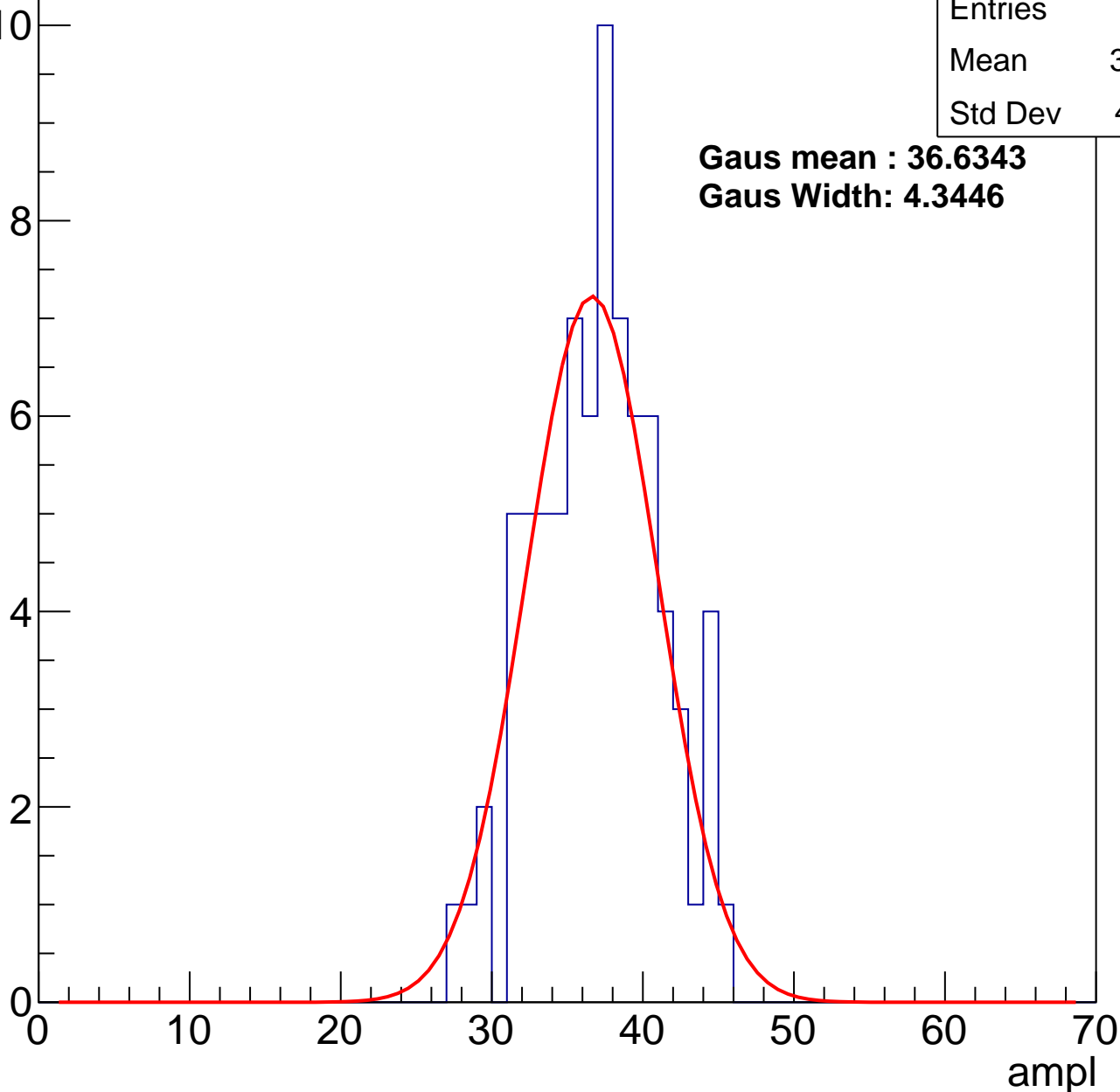
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	79
Mean	36.56
Std Dev	4.021

**Gaus mean : 36.6343**

**Gaus Width: 4.3446**



# B1L103S, U11-ch3, adc2

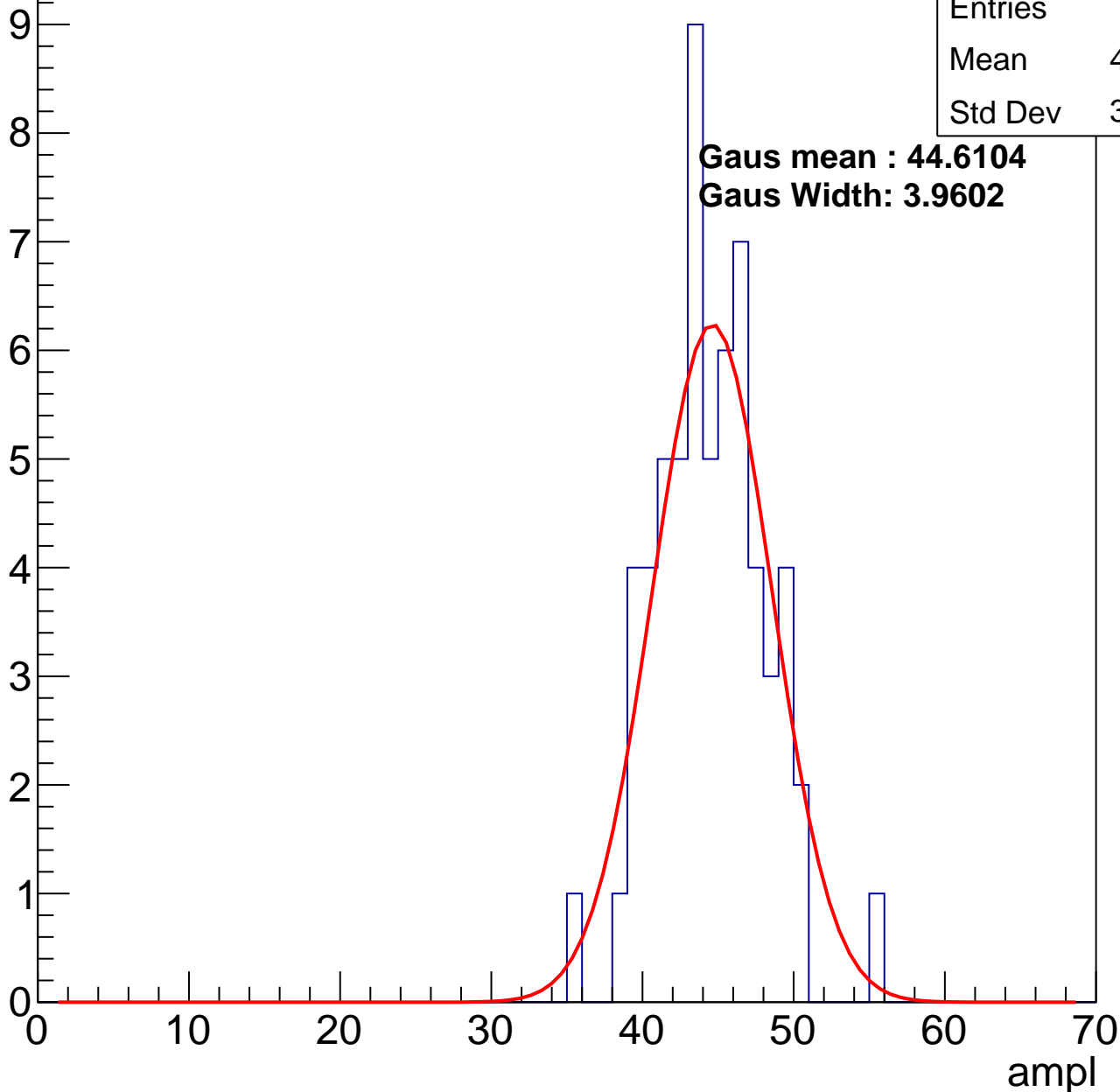
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	61
Mean	44.03
Std Dev	3.543

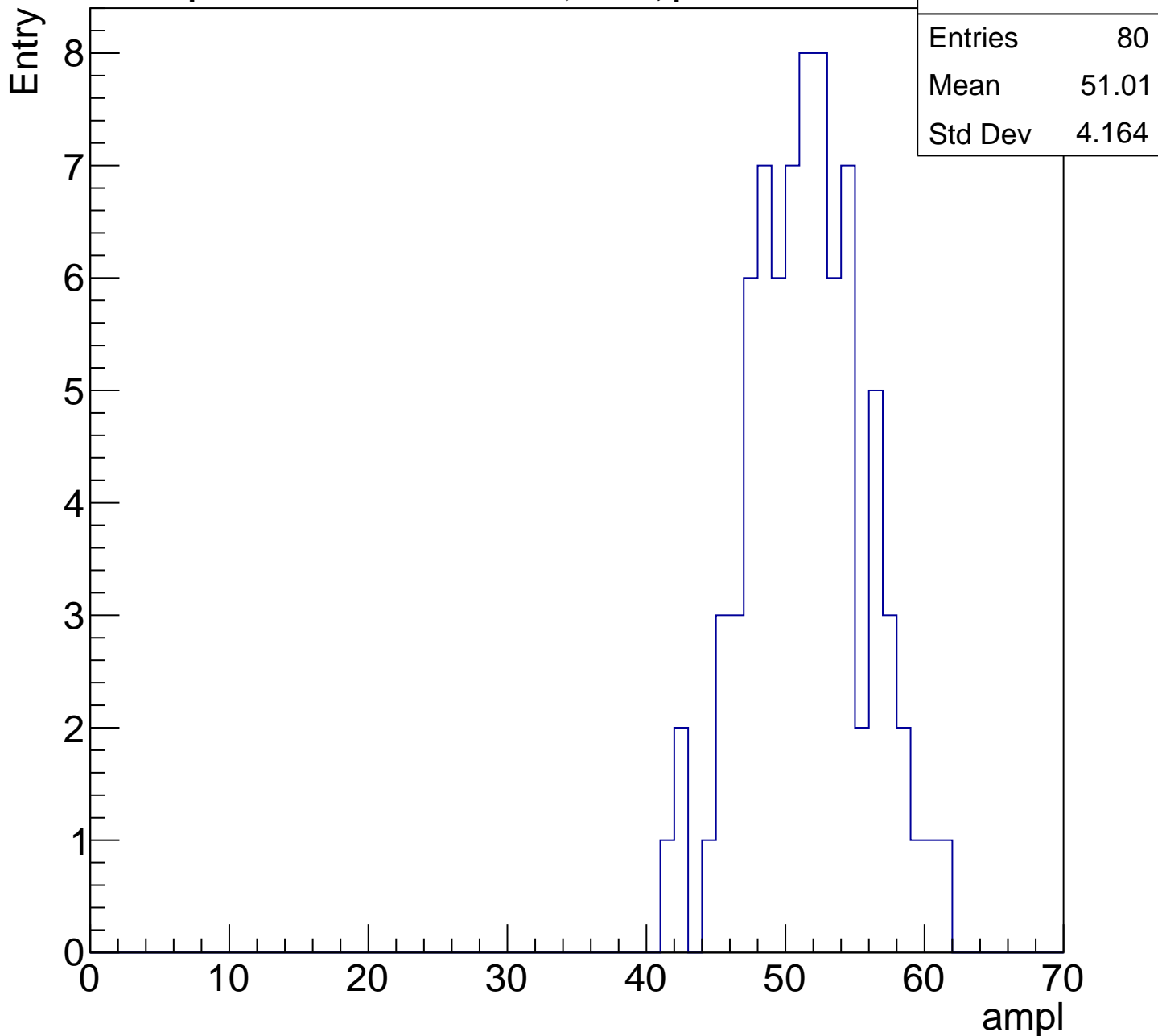
**Gaus mean : 44.6104**

**Gaus Width: 3.9602**



# B1L103S, U11-ch3, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

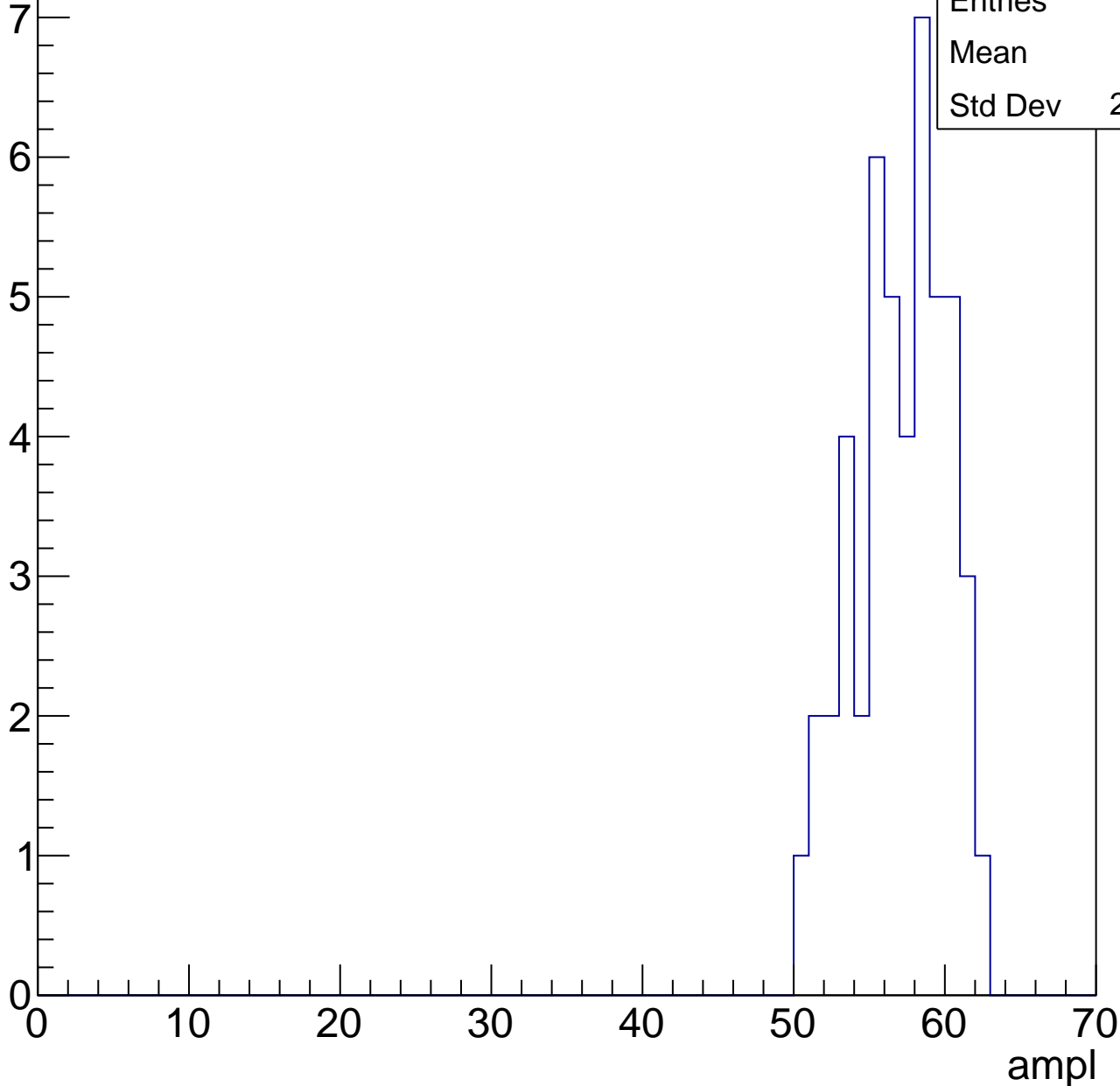


# B1L103S, U11-ch3, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	47
Mean	56.6
Std Dev	2.987

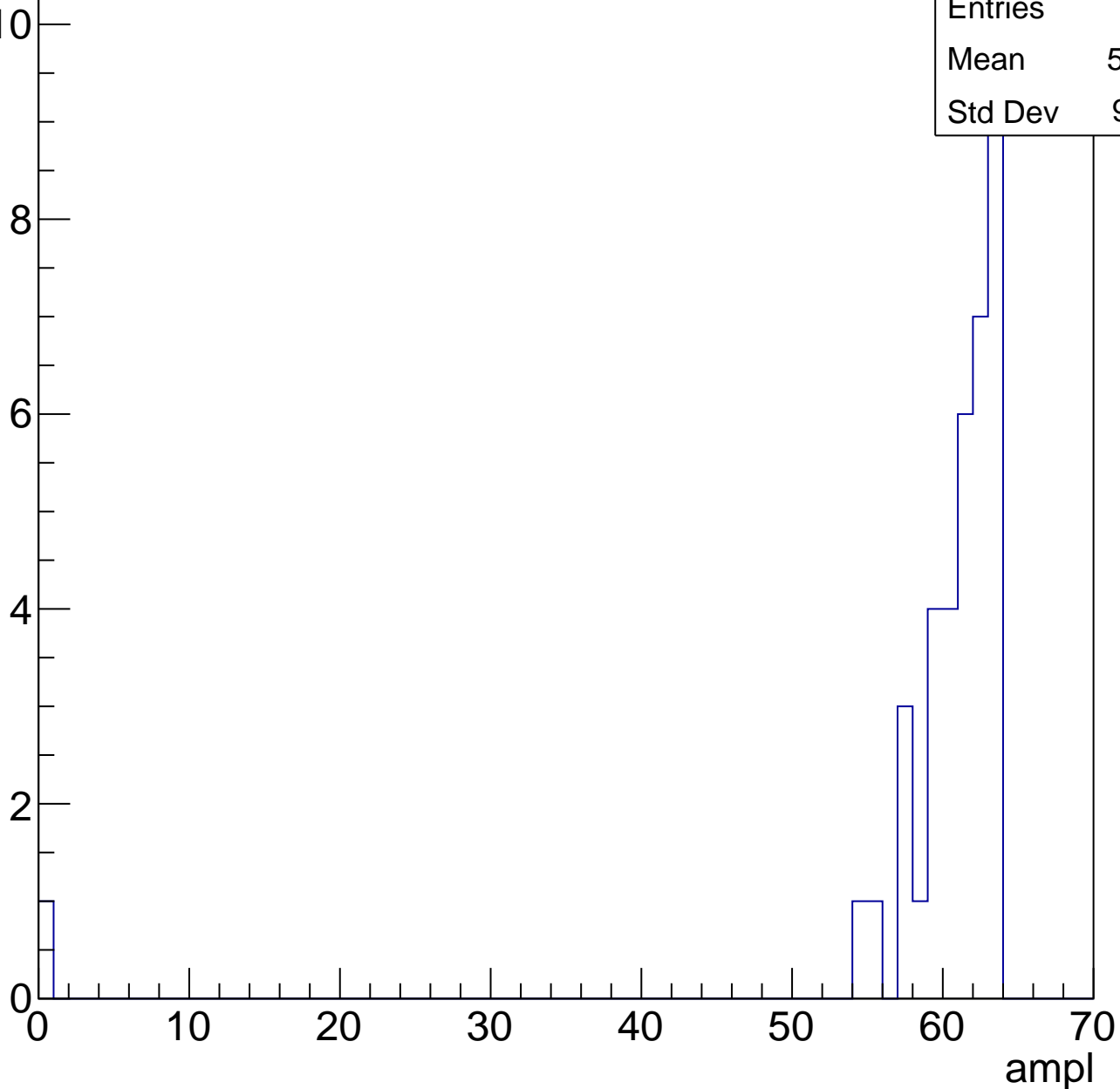


# B1L103S, U11-ch3, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	38
Mean	59.05
Std Dev	9.981



# B1L103S, U11-ch3, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	2
Mean	62
Std Dev	0

0 10 20 30 40 50 60 70

ampl



# B1L103S, U11-ch3, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U11-ch4, adc0

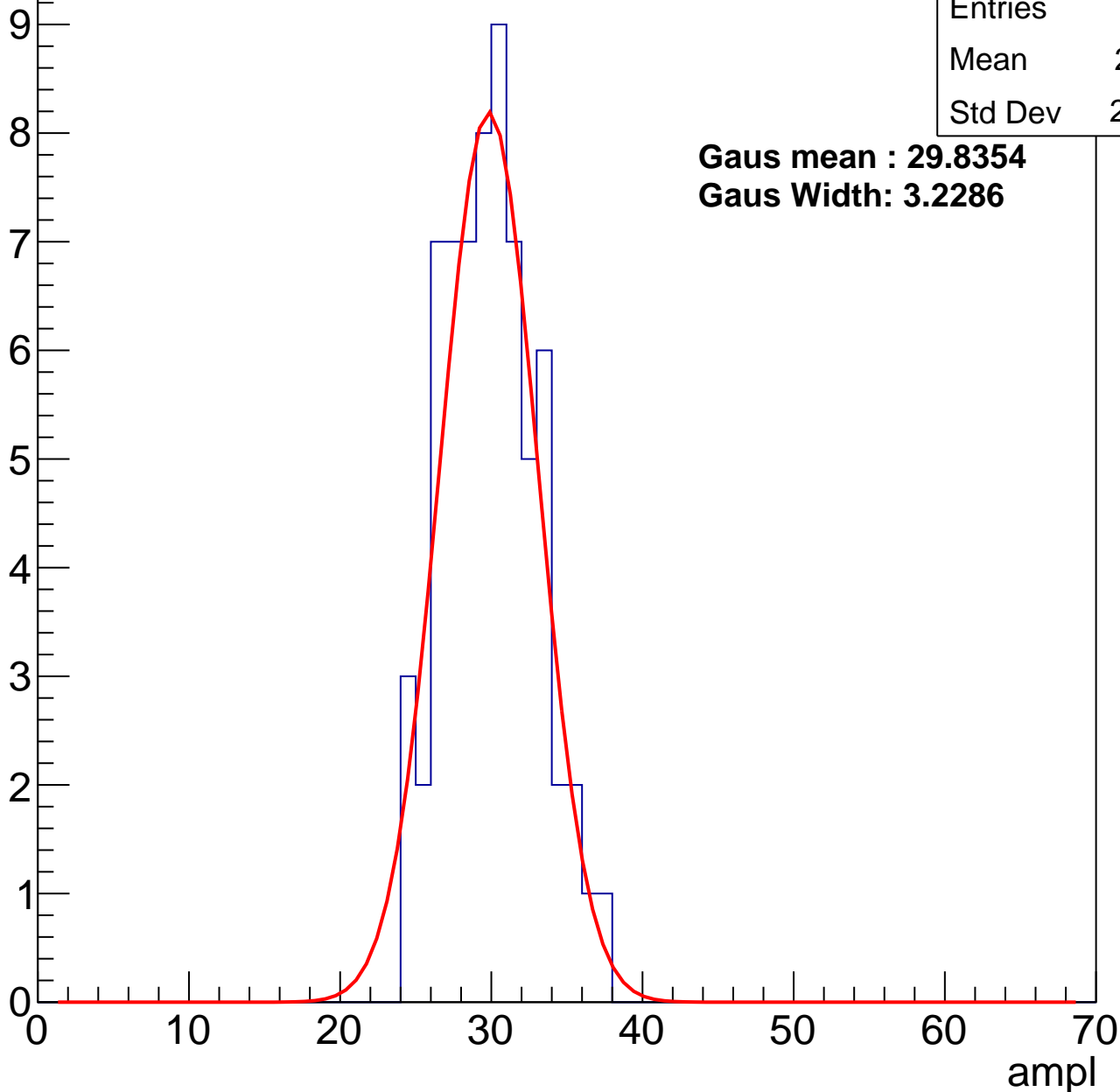
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	29.51
Std Dev	2.994

**Gaus mean : 29.8354**

**Gaus Width: 3.2286**



# B1L103S, U11-ch4, adc1

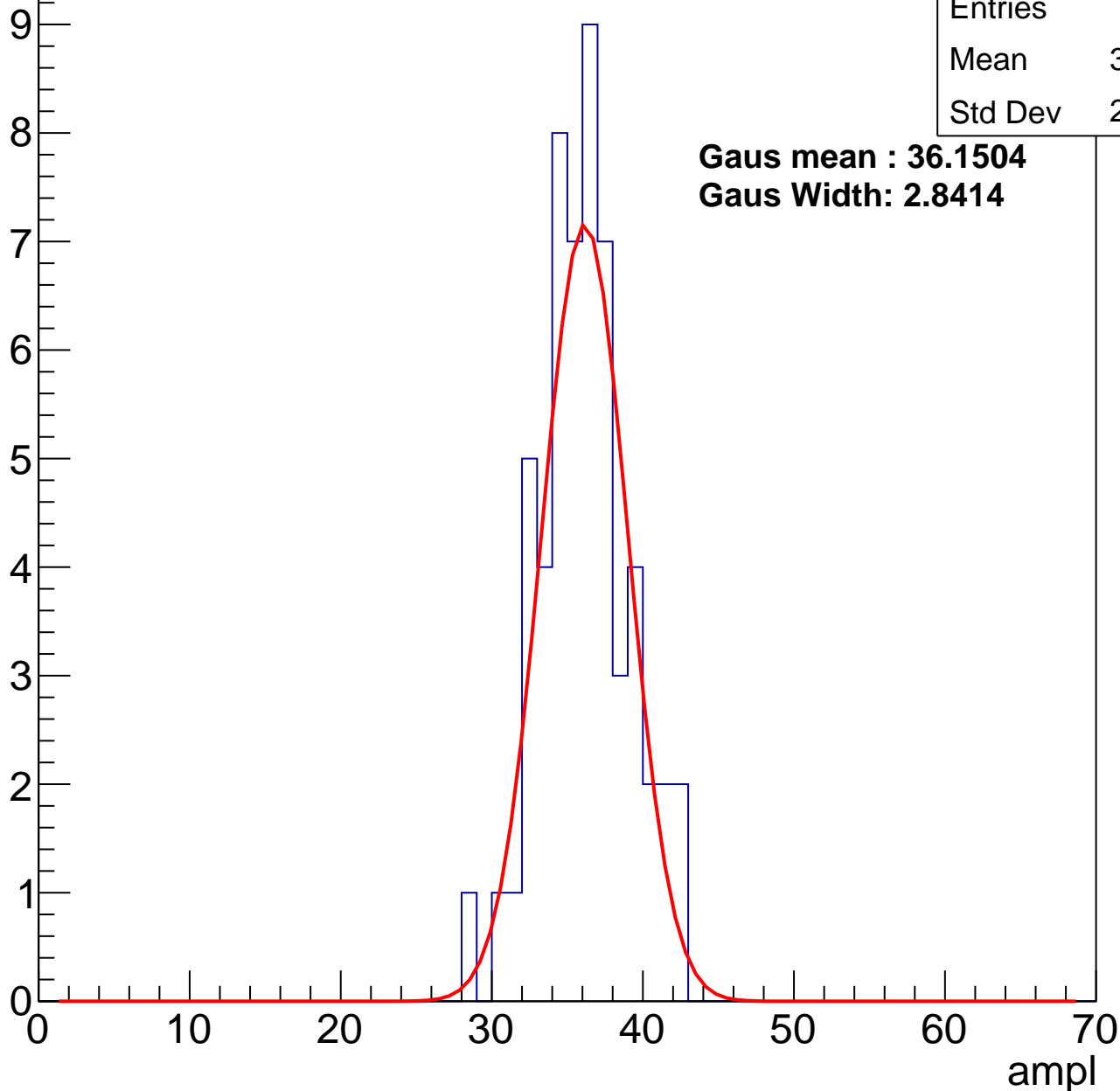
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	56
Mean	35.66
Std Dev	2.935

**Gaus mean : 36.1504**

**Gaus Width: 2.8414**



# B1L103S, U11-ch4, adc2

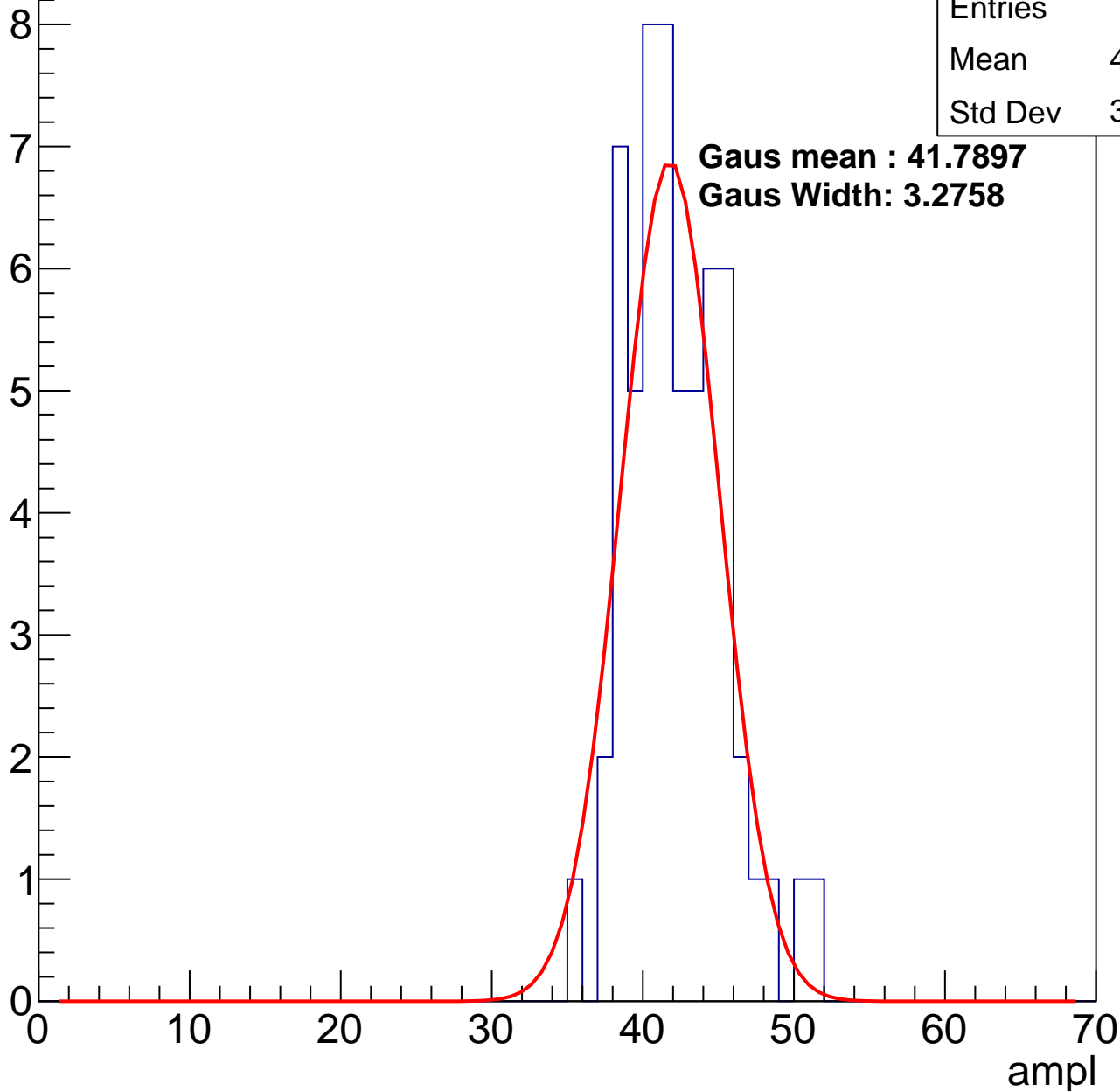
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	59
Mean	41.78
Std Dev	3.226

**Gaus mean : 41.7897**

**Gaus Width: 3.2758**

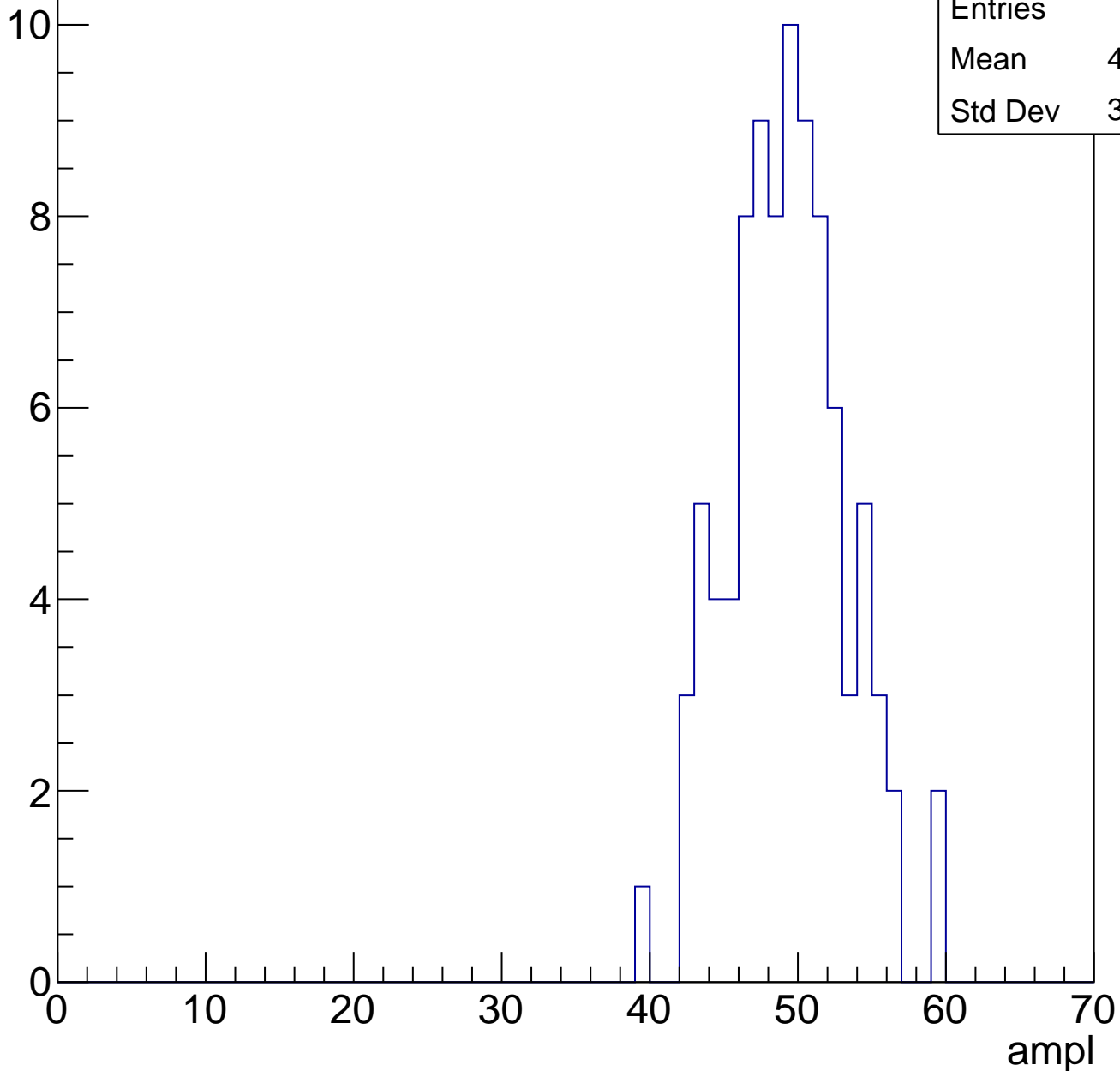


# B1L103S, U11-ch4, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	90
Mean	48.83
Std Dev	3.914

Entry

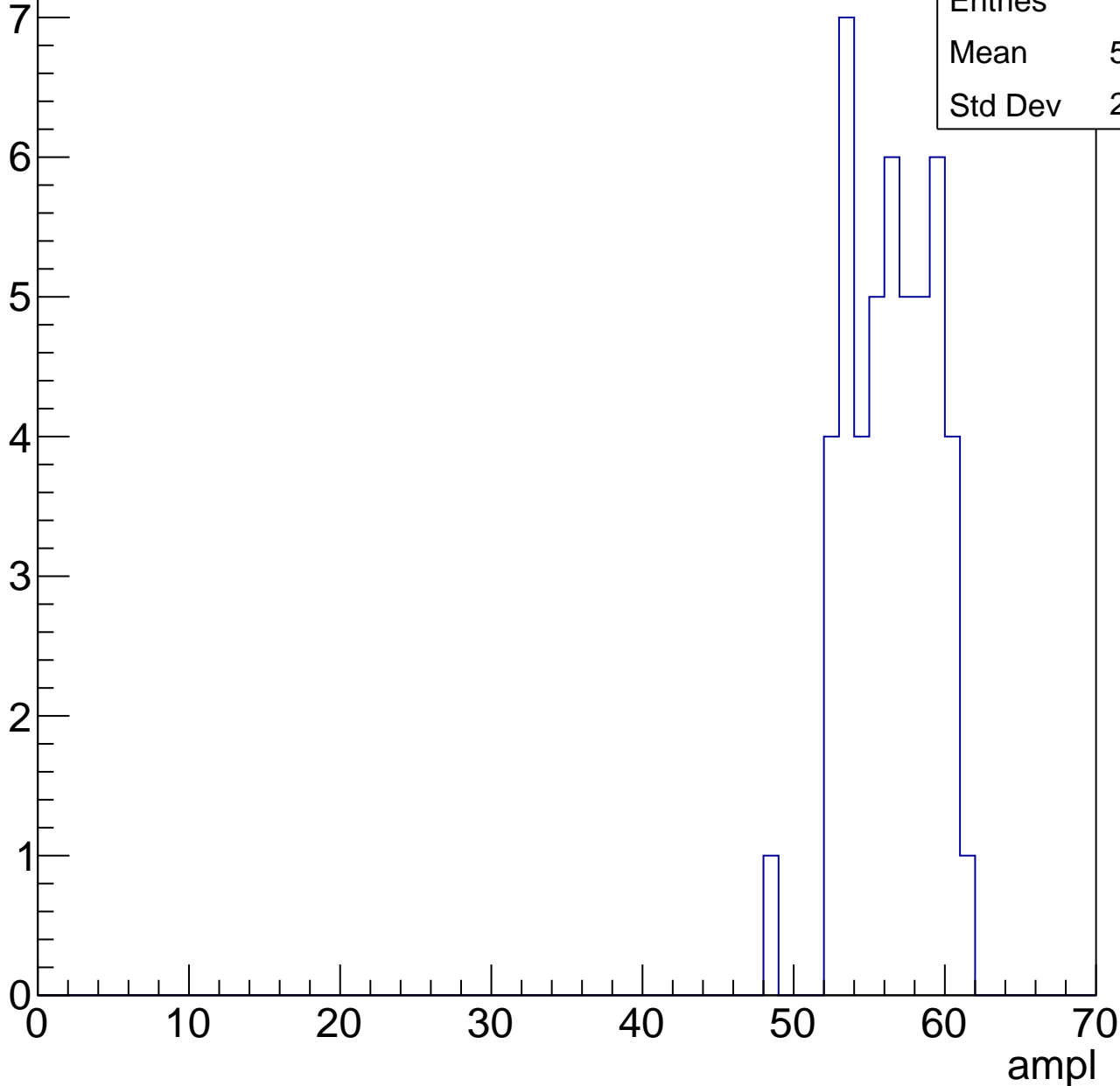


# B1L103S, U11-ch4, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	48
Mean	55.92
Std Dev	2.812

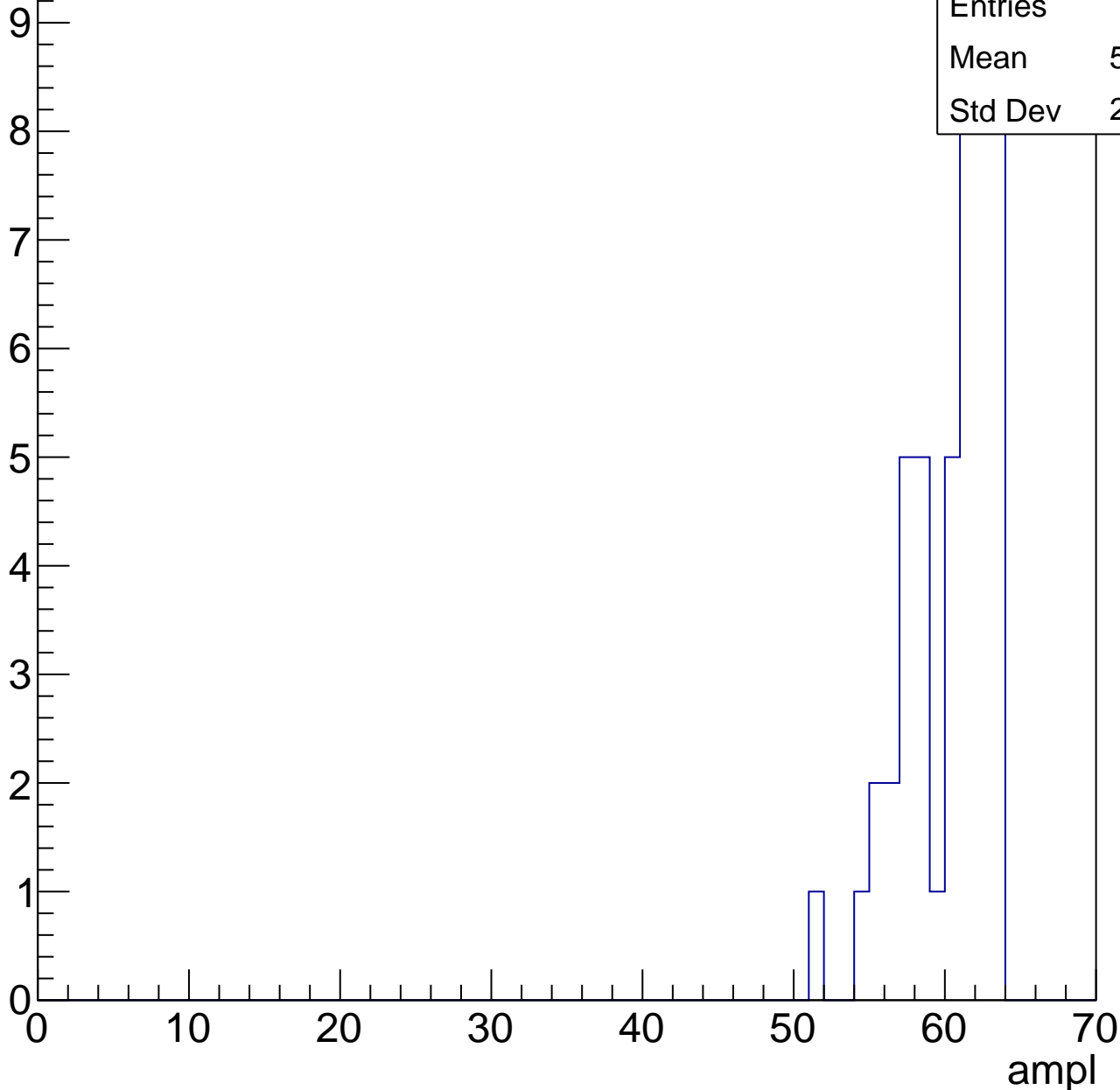


# B1L103S, U11-ch4, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

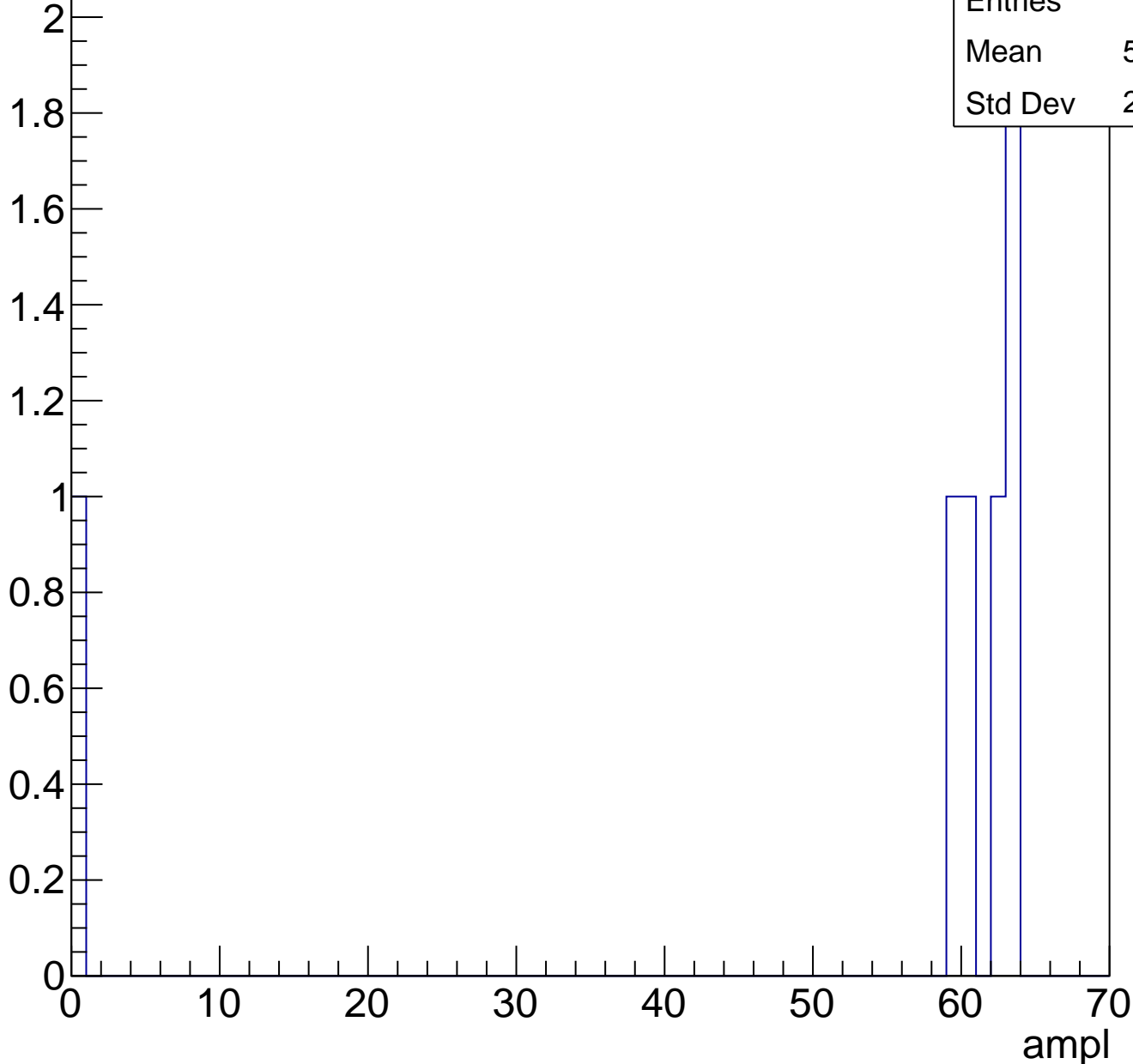
Entries	48
Mean	59.83
Std Dev	2.816



# B1L103S, U11-ch4, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U11-ch4, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	4
Mean	0
Std Dev	0

# B1L103S, U11-ch5, adc0

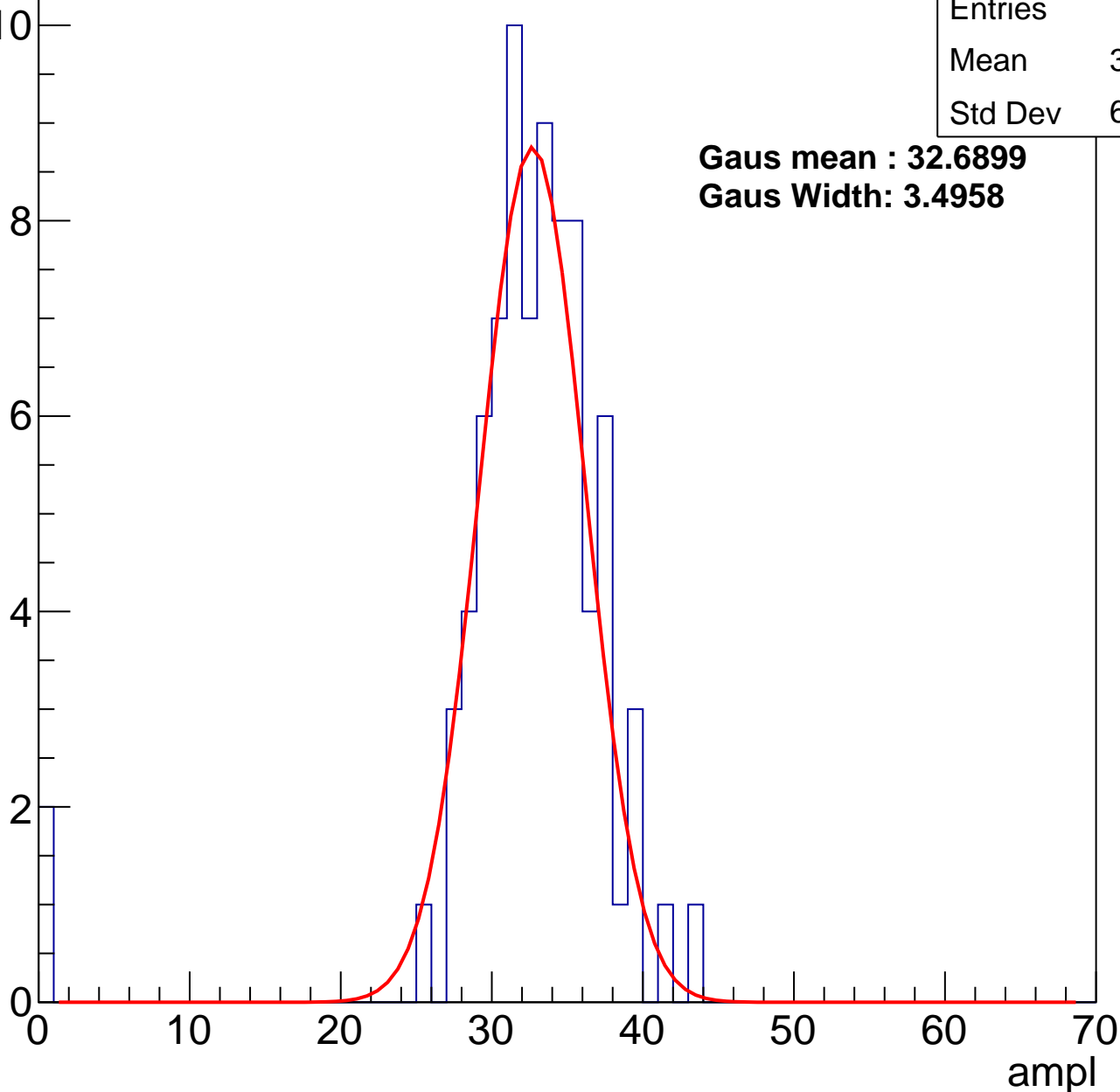
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	81
Mean	31.98
Std Dev	6.126

**Gaus mean : 32.6899**

**Gaus Width: 3.4958**



# B1L103S, U11-ch5, adc1

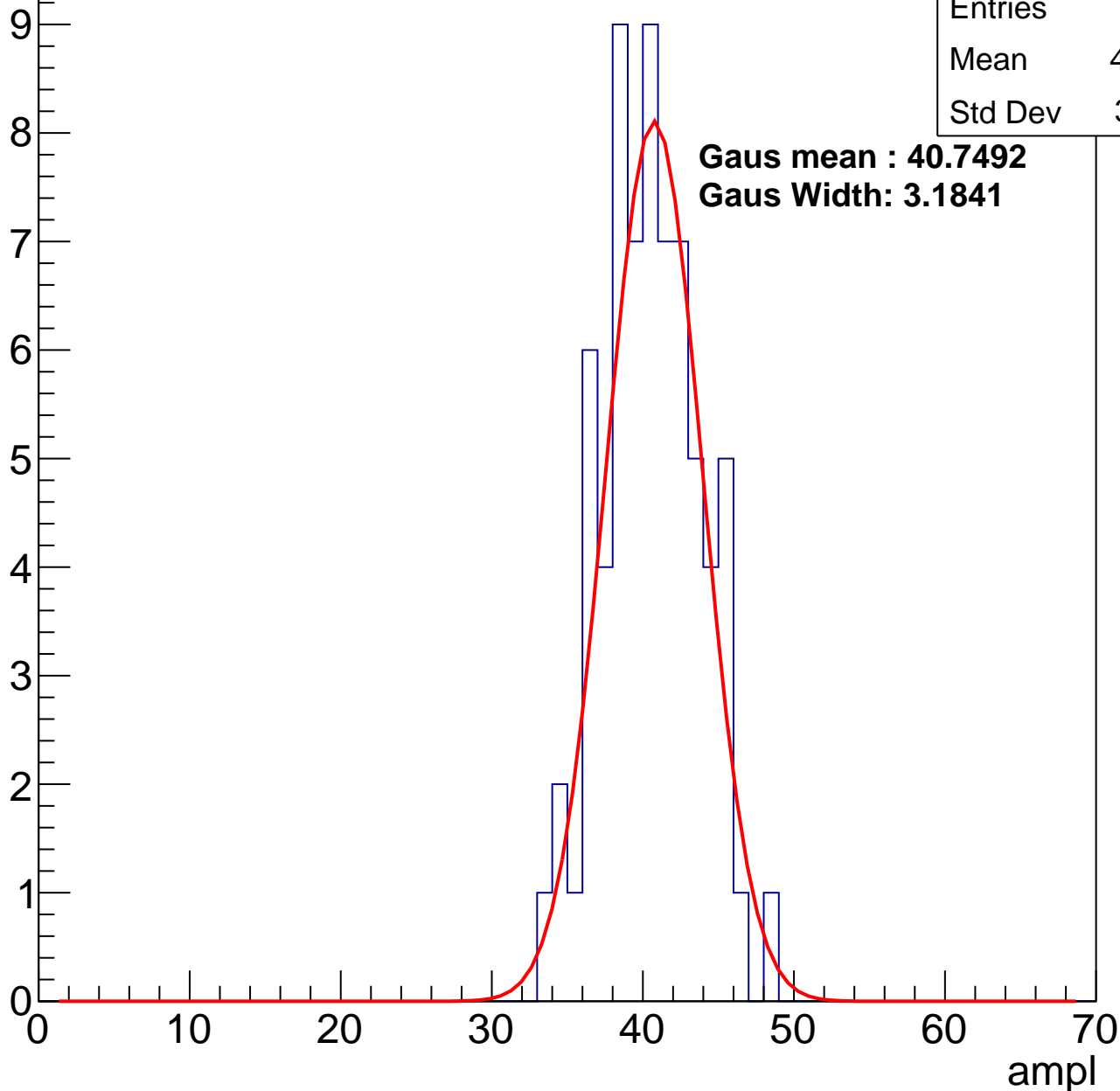
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	69
Mean	40.09
Std Dev	3.161

**Gaus mean : 40.7492**

**Gaus Width: 3.1841**



# B1L103S, U11-ch5, adc2

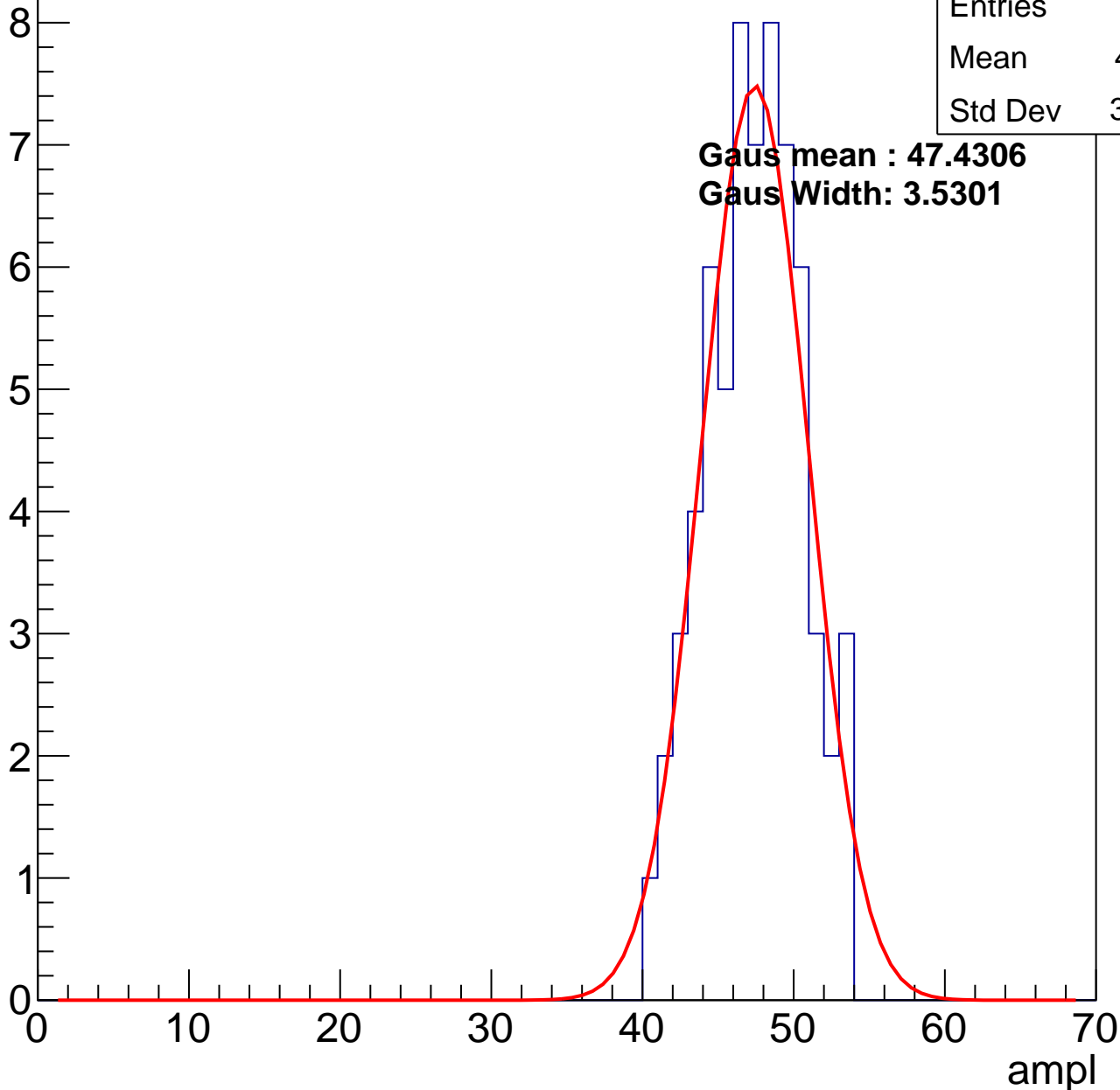
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	46.91
Std Dev	3.132

**Gaus mean : 47.4306**

**Gaus Width: 3.5301**

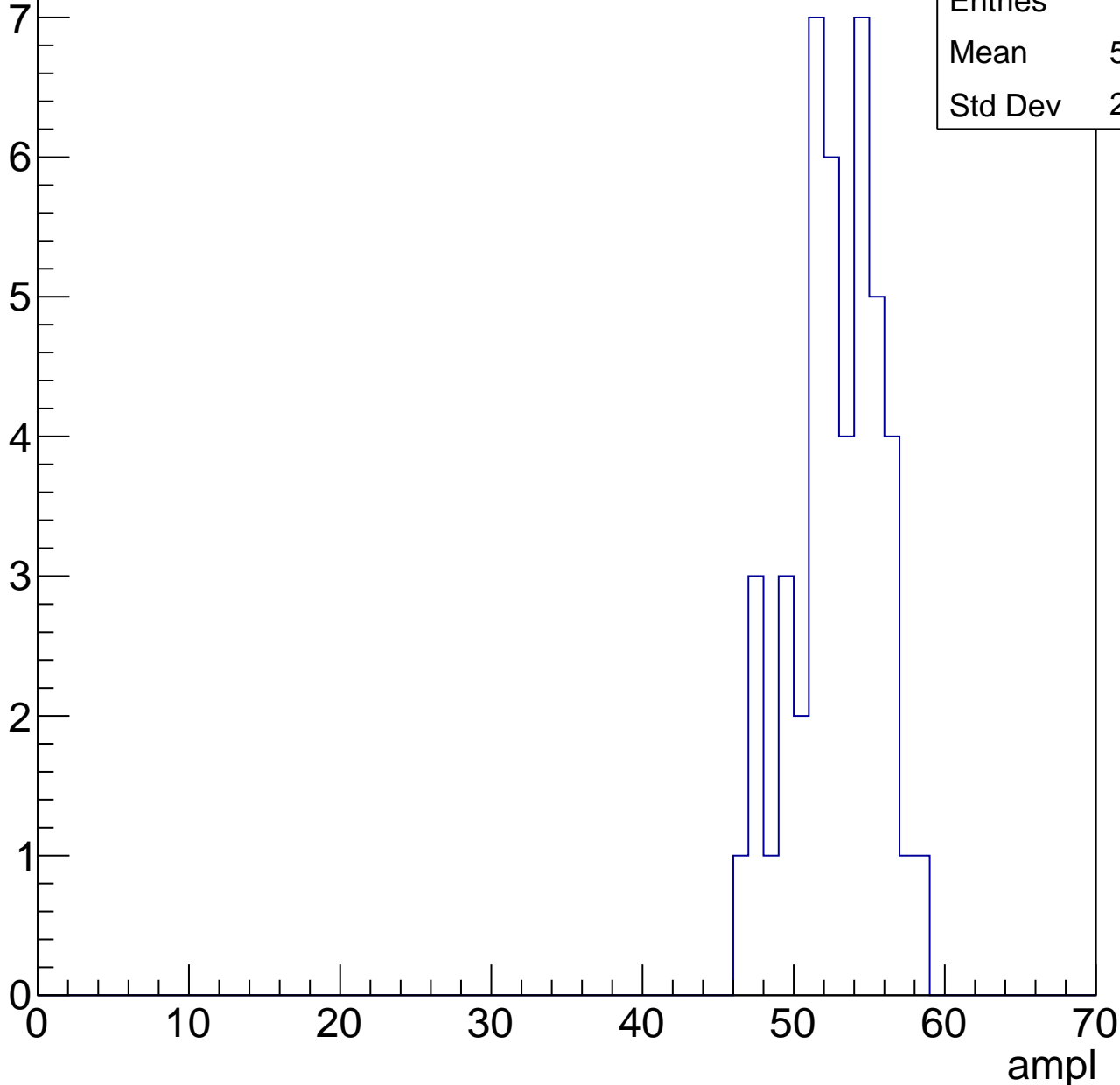


# B1L103S, U11-ch5, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	45
Mean	52.33
Std Dev	2.852

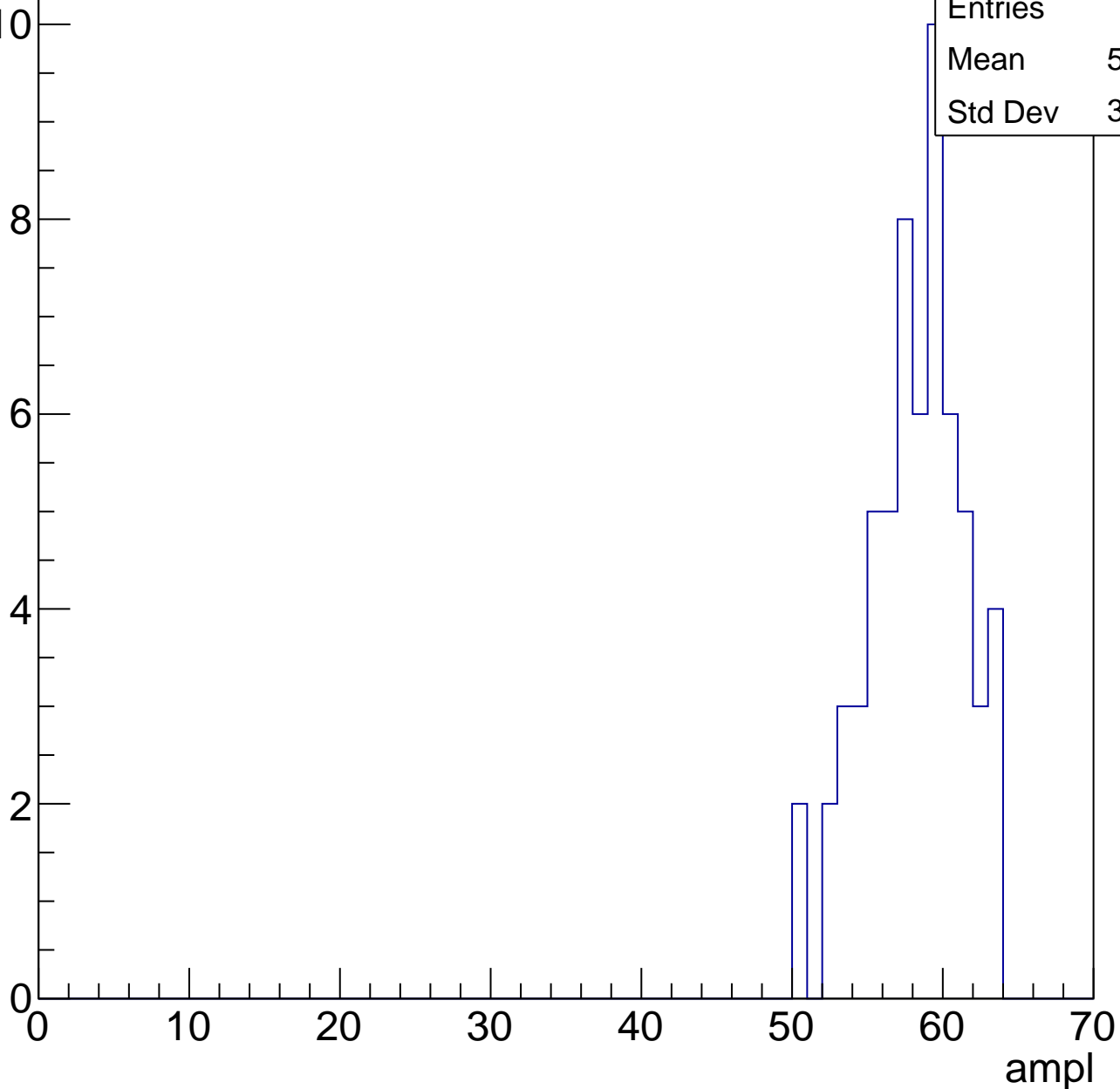


# B1L103S, U11-ch5, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	57.69
Std Dev	3.155

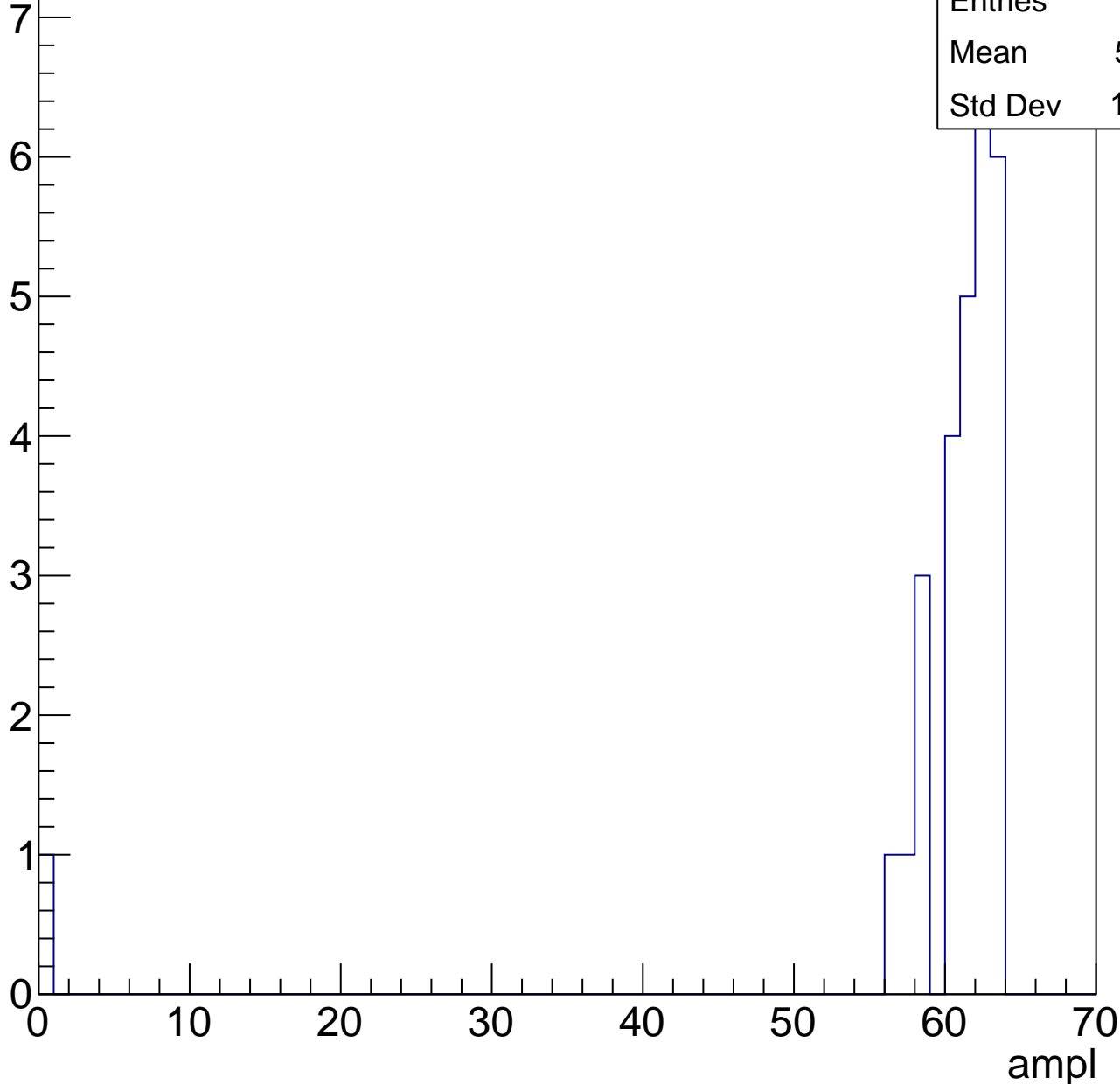


# B1L103S, U11-ch5, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	28
Mean	58.71
Std Dev	11.46



# B1L103S, U11-ch5, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0



# B1L103S, U11-ch5, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U11-ch6, adc0

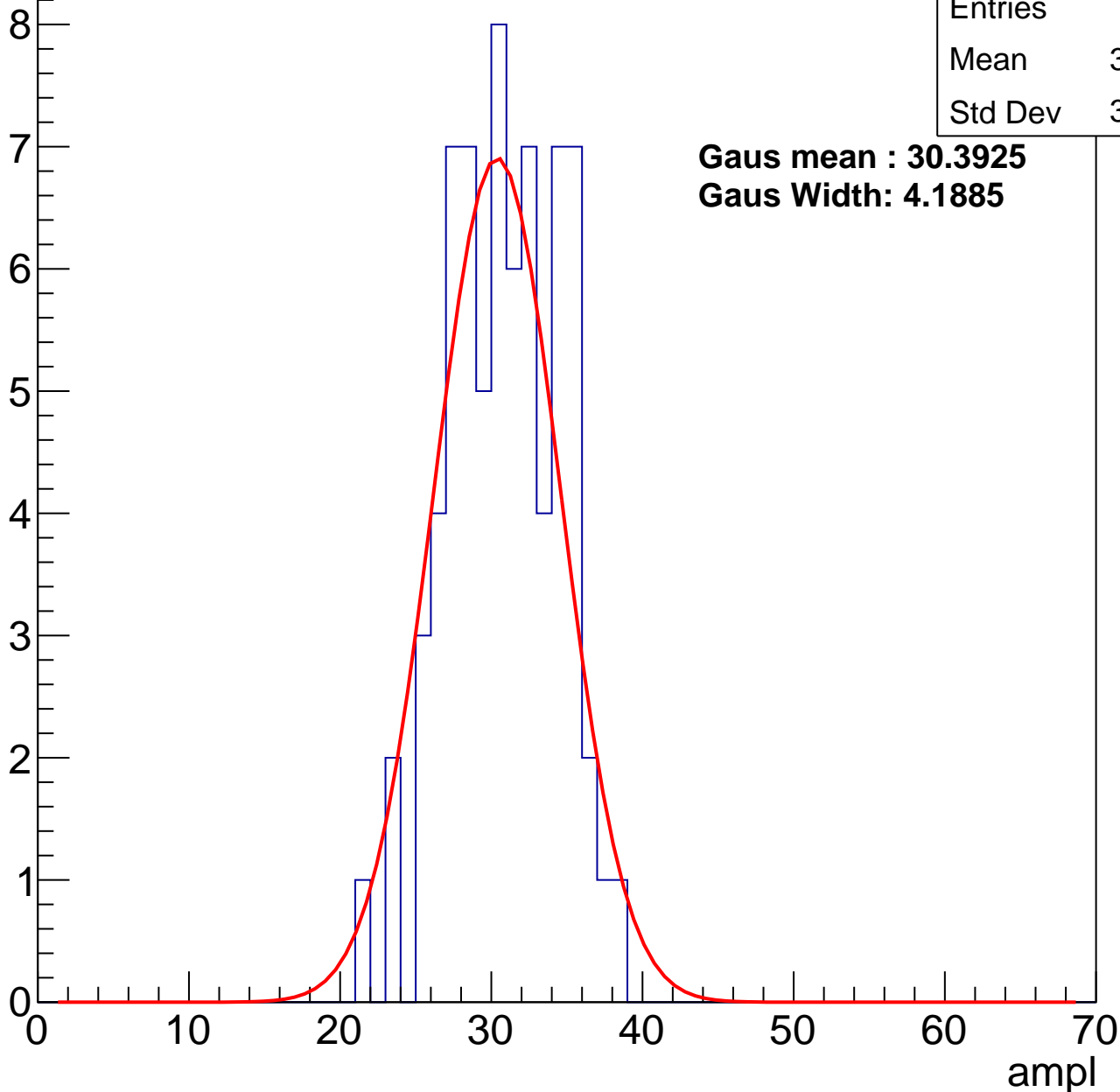
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	72
Mean	30.39
Std Dev	3.623

**Gaus mean : 30.3925**

**Gaus Width: 4.1885**



# B1L103S, U11-ch6, adc1

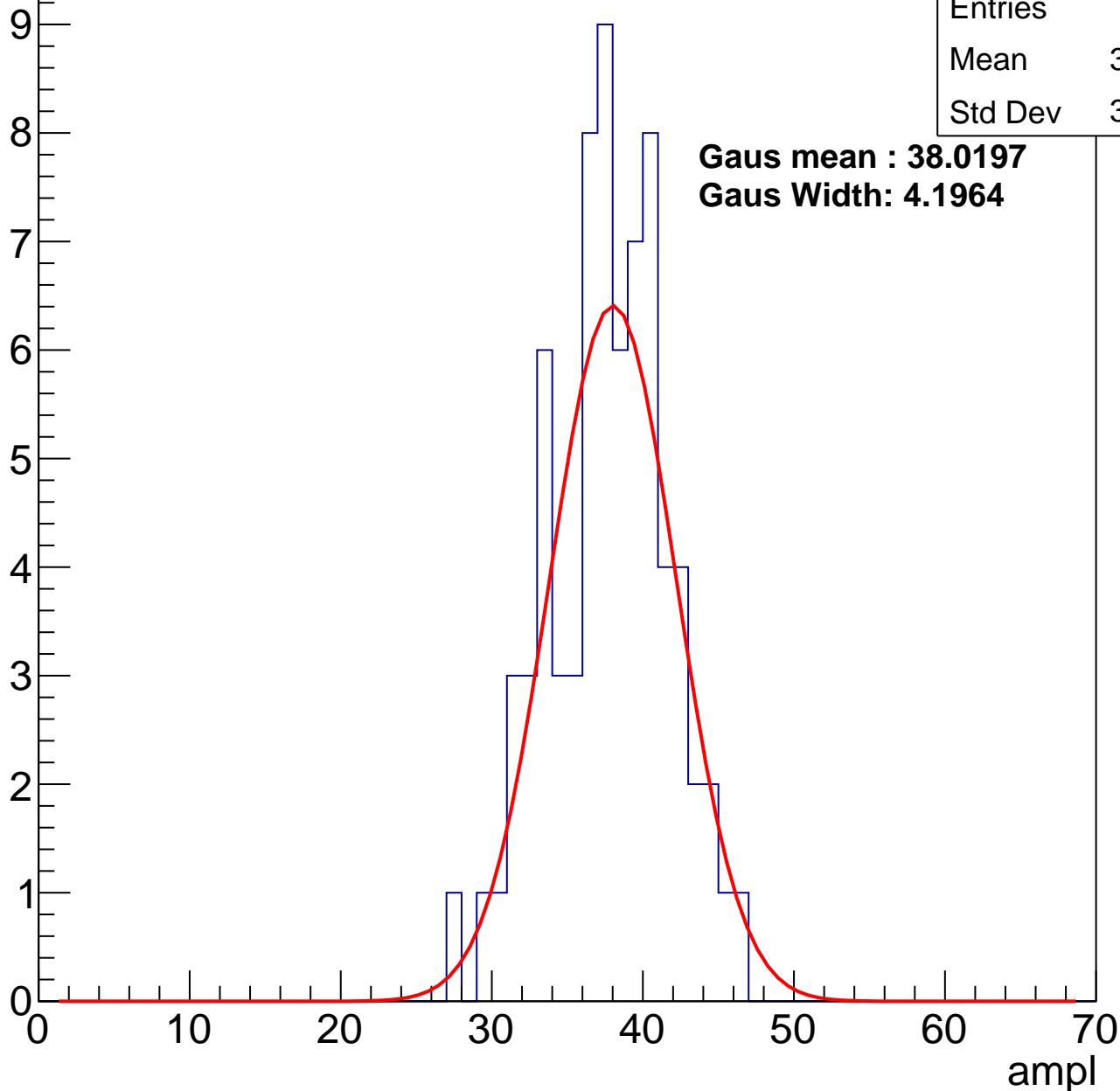
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	73
Mean	37.25
Std Dev	3.916

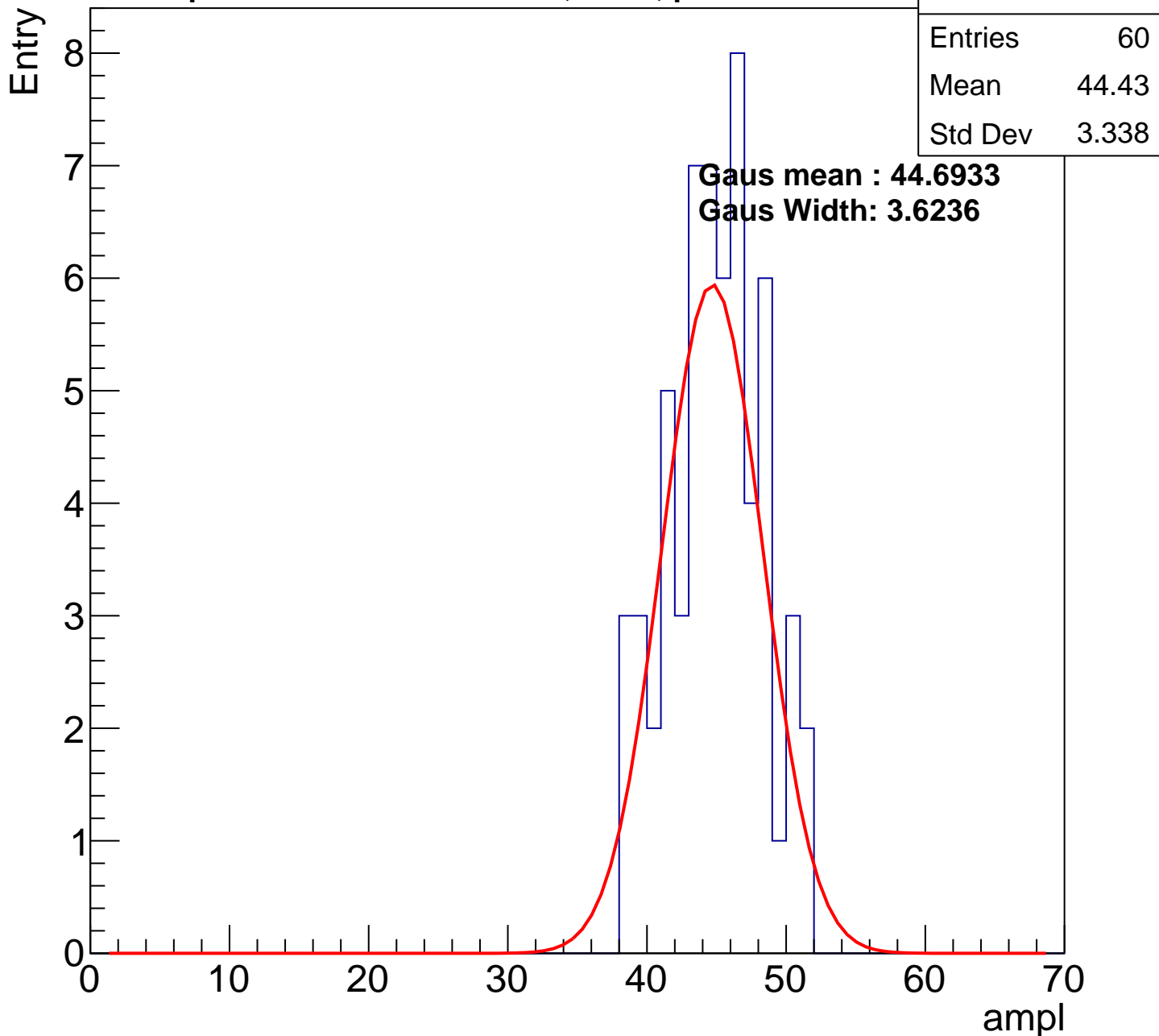
**Gaus mean : 38.0197**

**Gaus Width: 4.1964**



# B1L103S, U11-ch6, adc2

calib\_packv5\_042523\_0143.root, FC#7, port C2

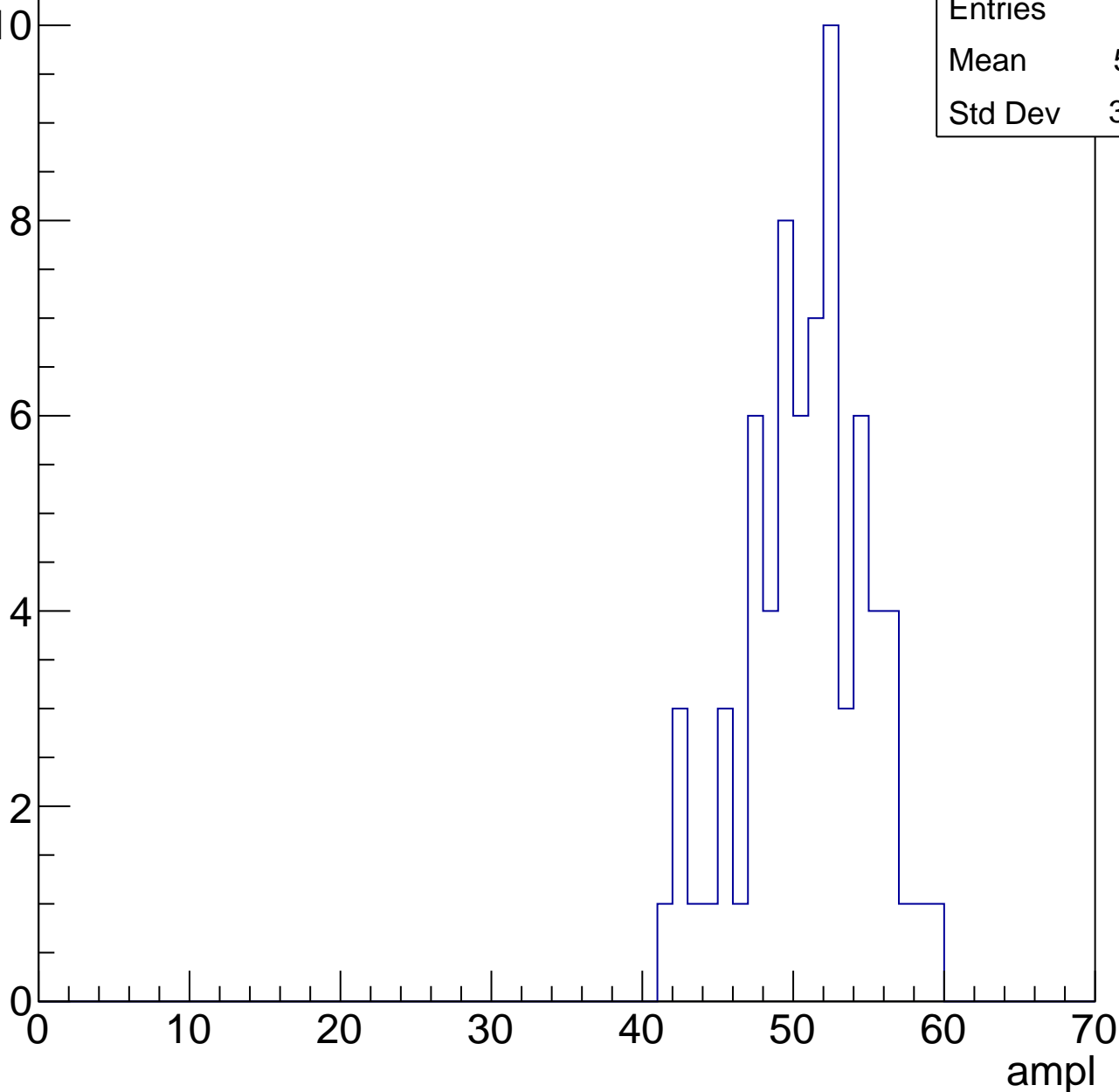


# B1L103S, U11-ch6, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	71
Mean	50.41
Std Dev	3.977

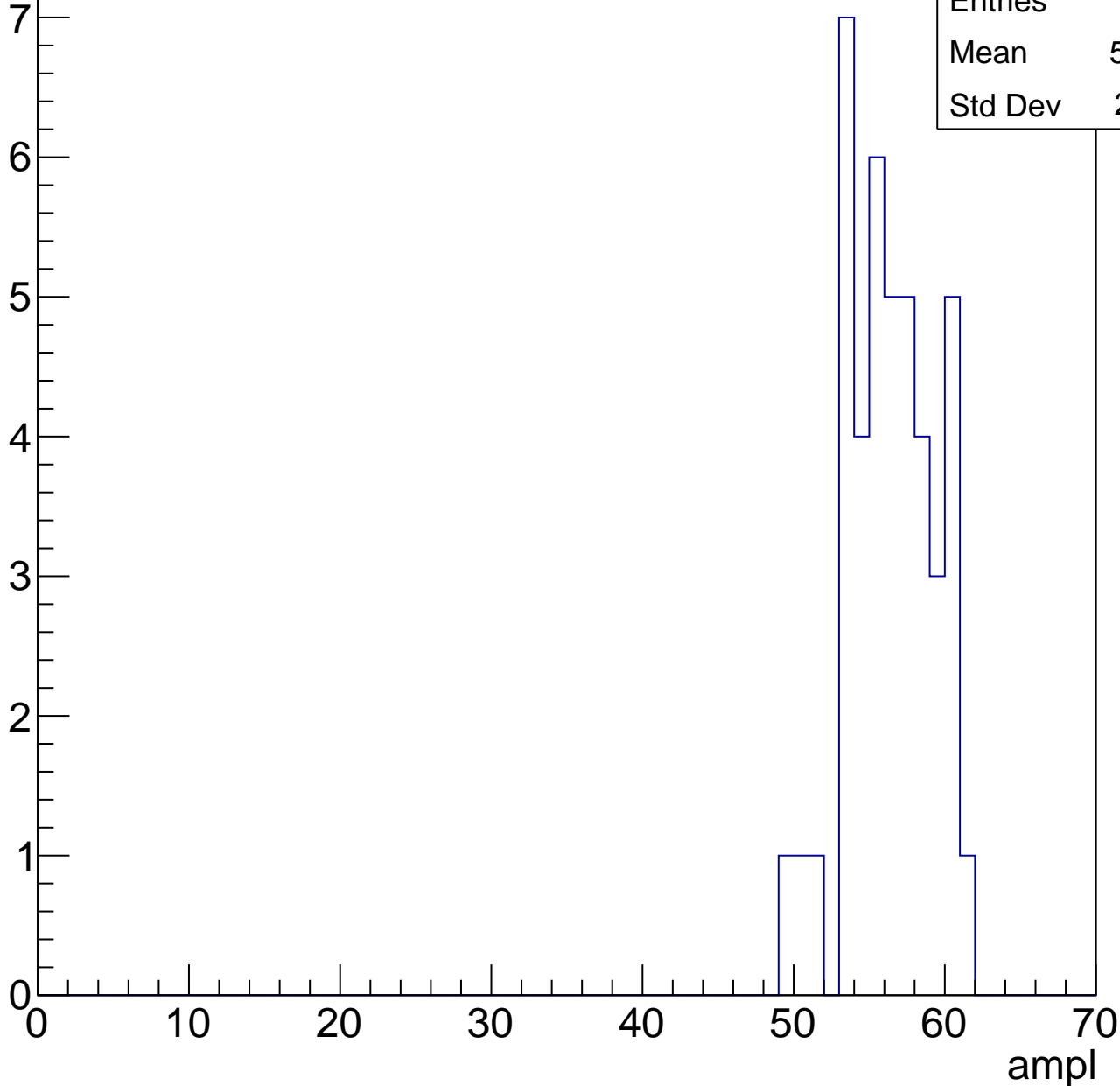


# B1L103S, U11-ch6, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	43
Mean	55.86
Std Dev	2.841

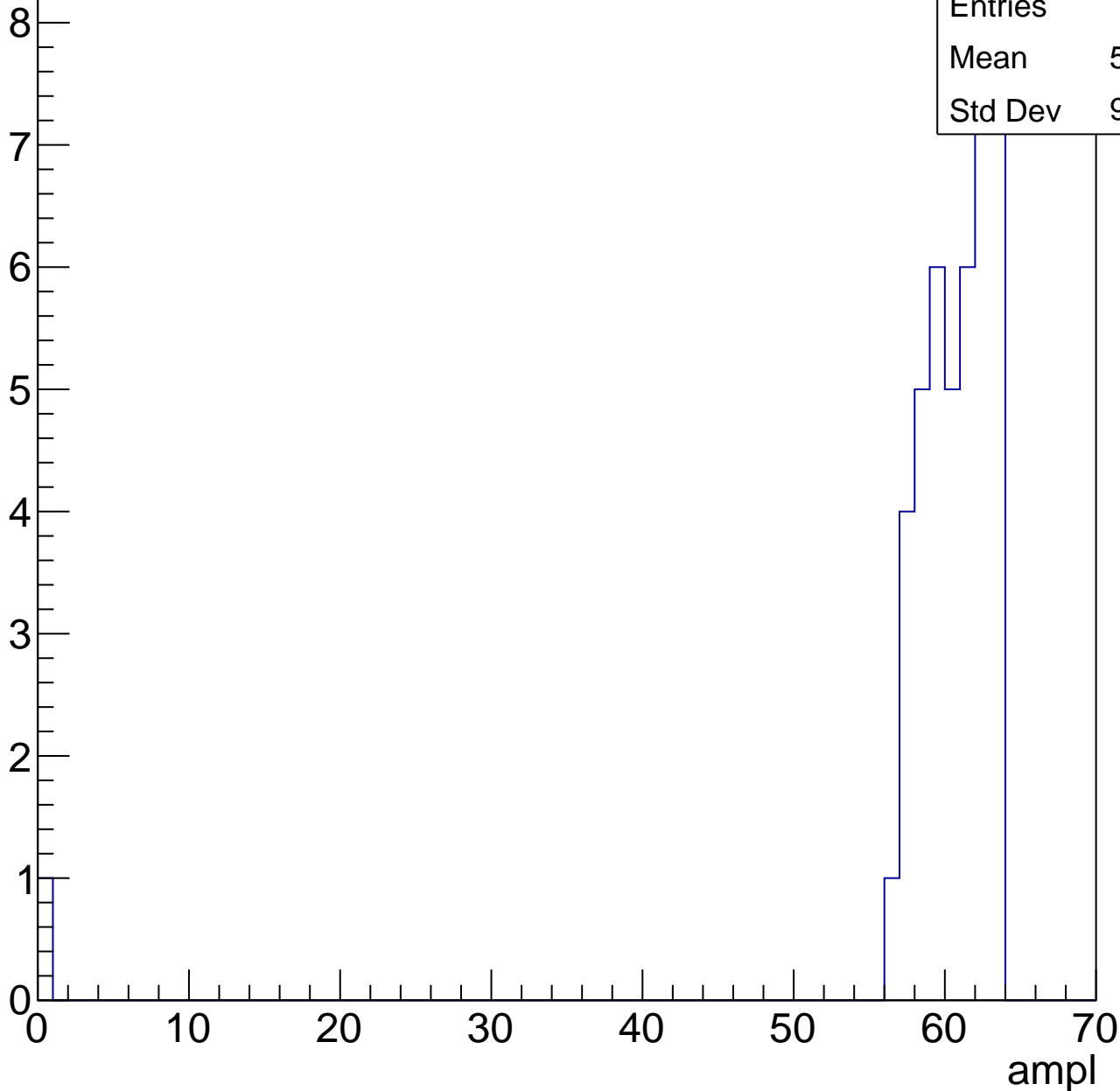


# B1L103S, U11-ch6, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

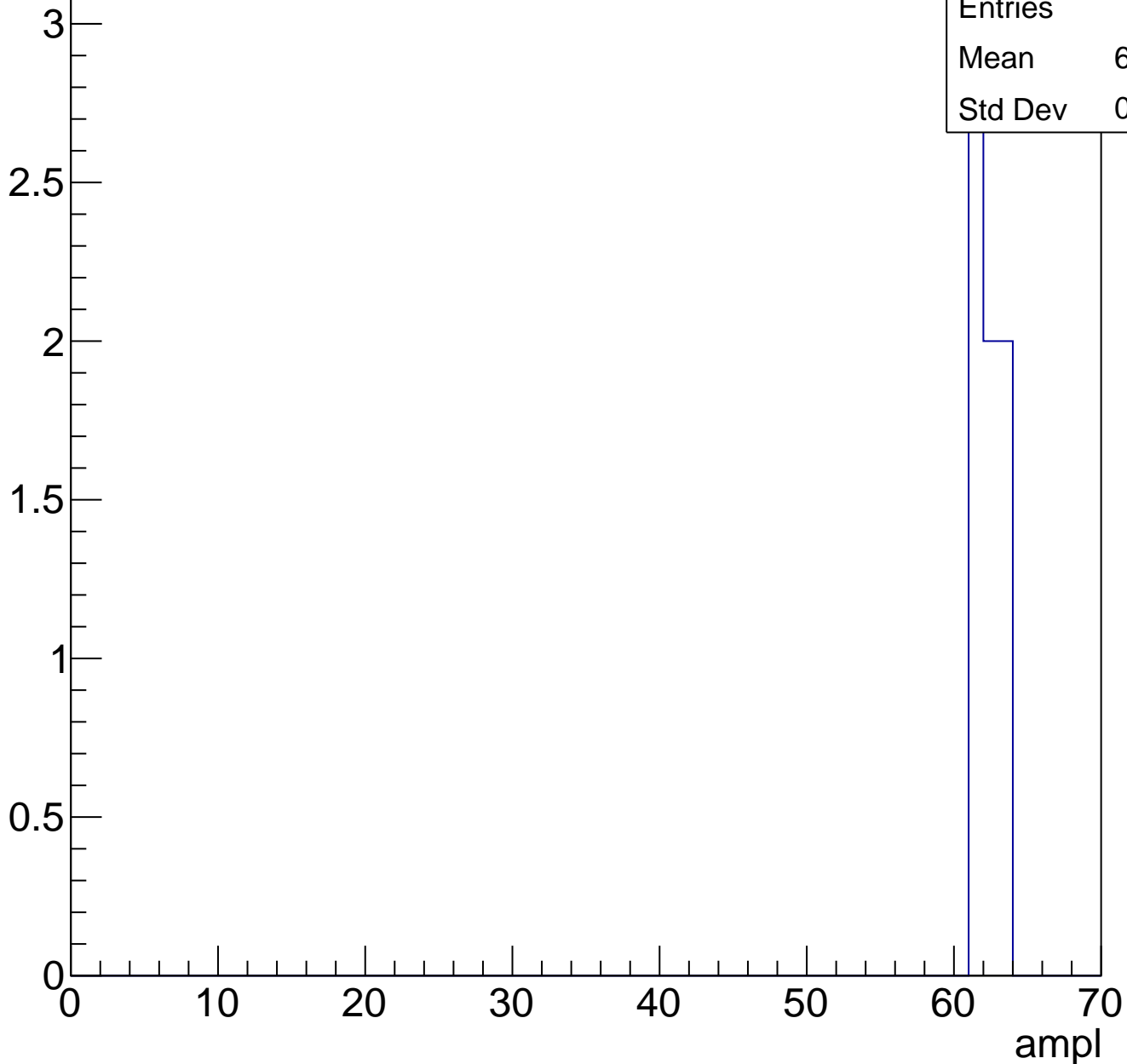
Entries	44
Mean	58.95
Std Dev	9.219



# B1L103S, U11-ch6, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U11-ch6, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U11-ch7, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	78
Mean	28.14
Std Dev	5.731

**Gaus mean : 29.1998**

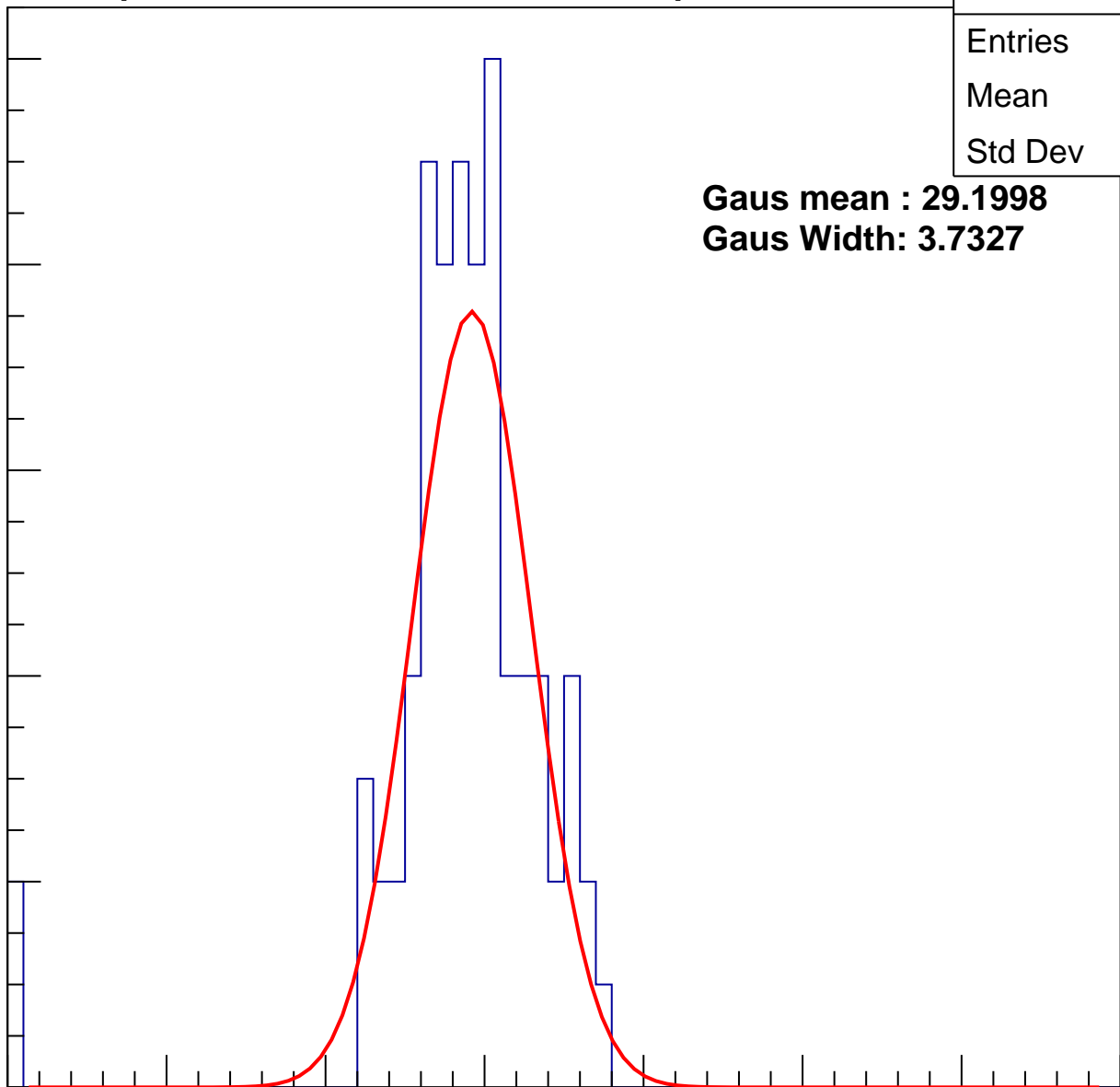
**Gaus Width: 3.7327**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U11-ch7, adc1

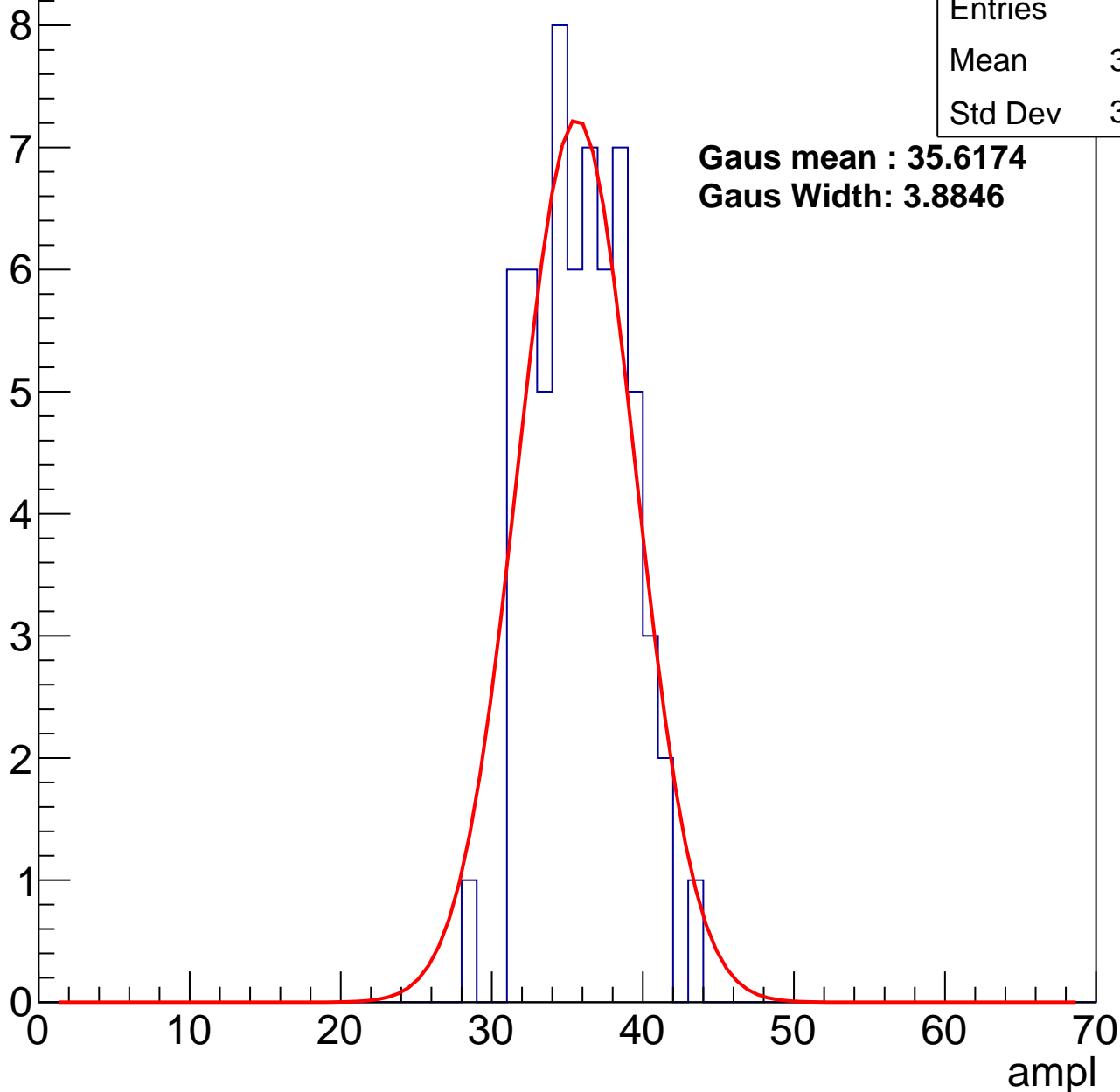
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	35.44
Std Dev	3.085

**Gaus mean : 35.6174**

**Gaus Width: 3.8846**



# B1L103S, U11-ch7, adc2

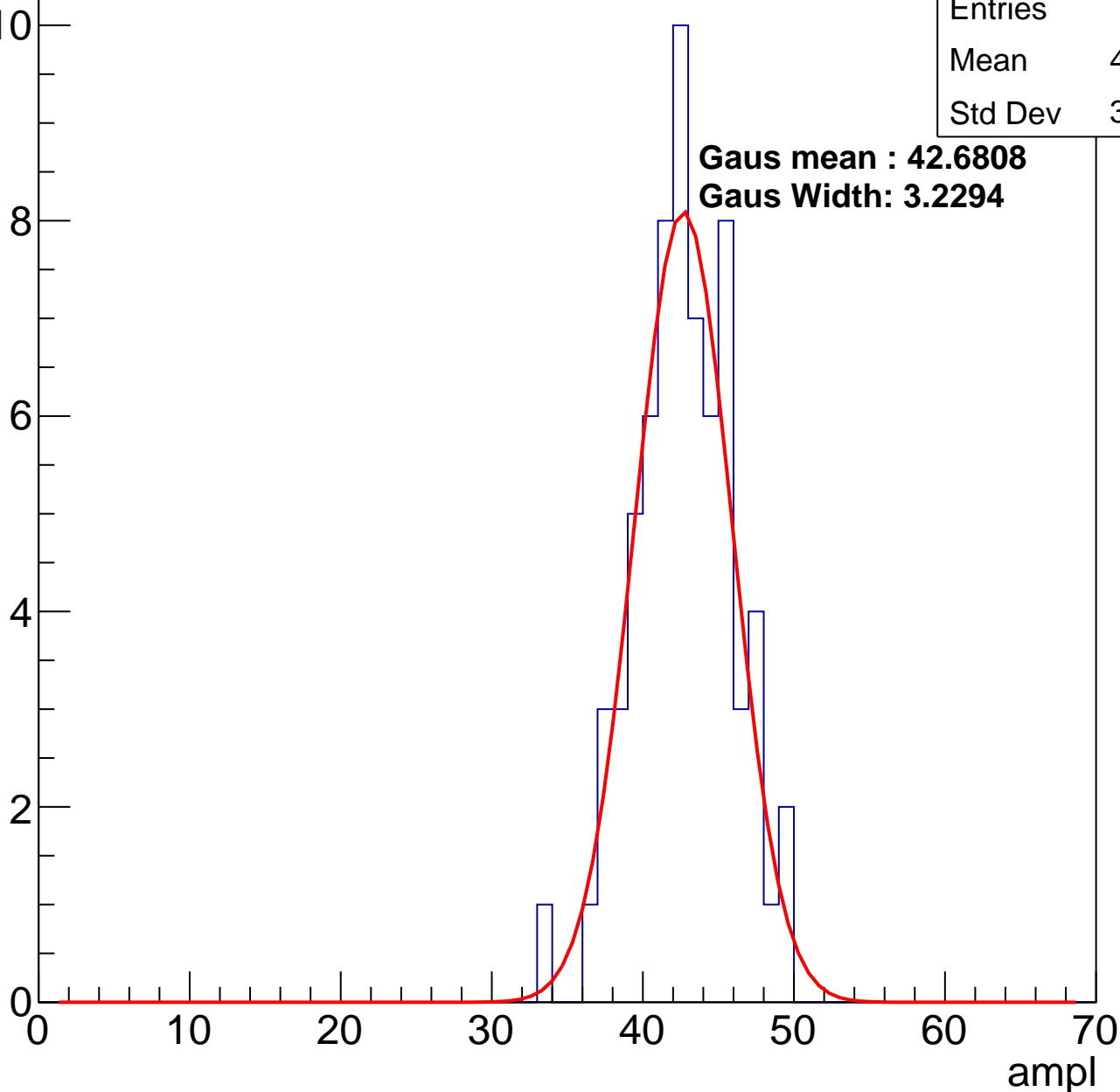
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	68
Mean	42.26
Std Dev	3.202

**Gaus mean : 42.6808**

**Gaus Width: 3.2294**

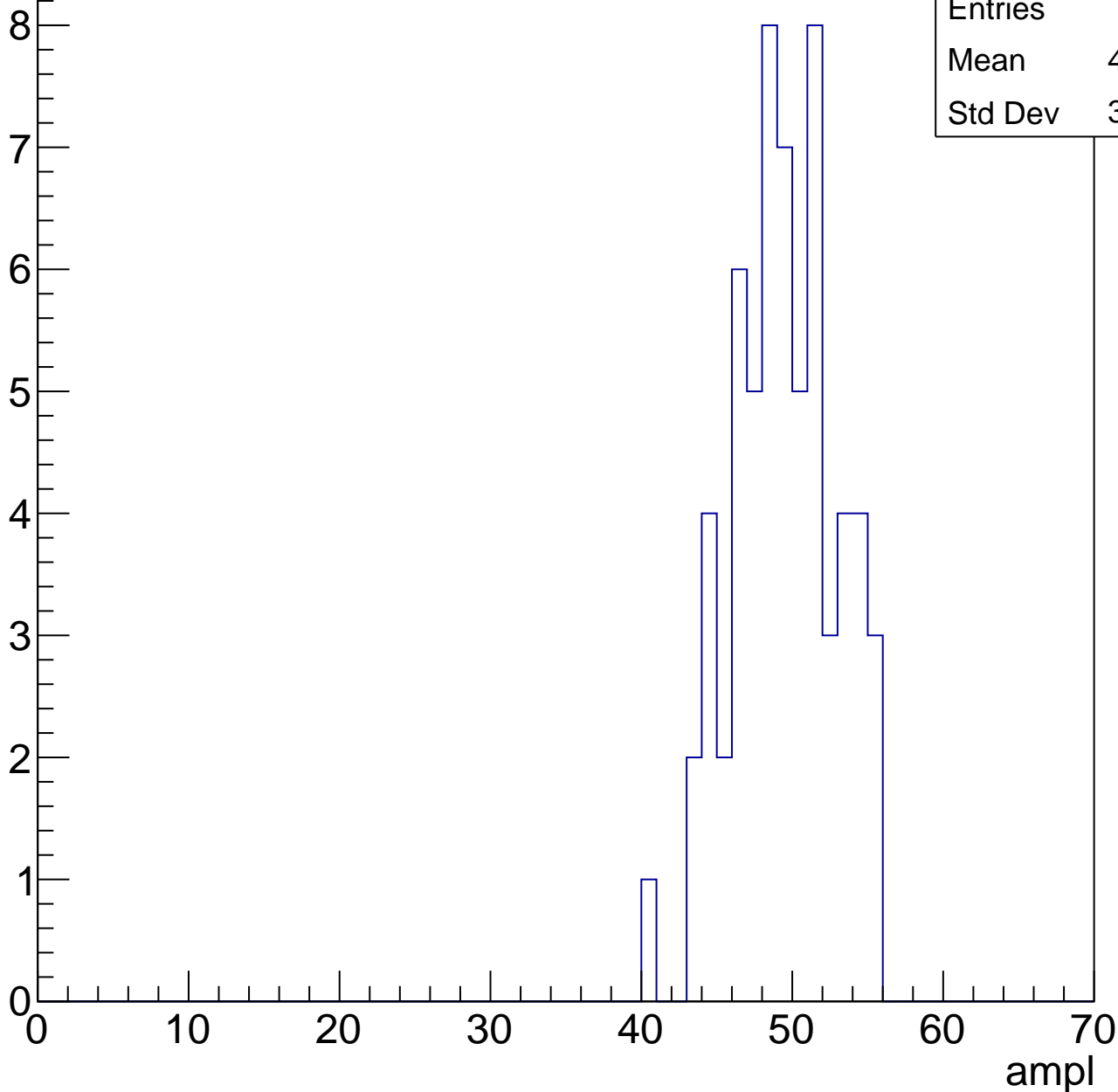


# B1L103S, U11-ch7, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

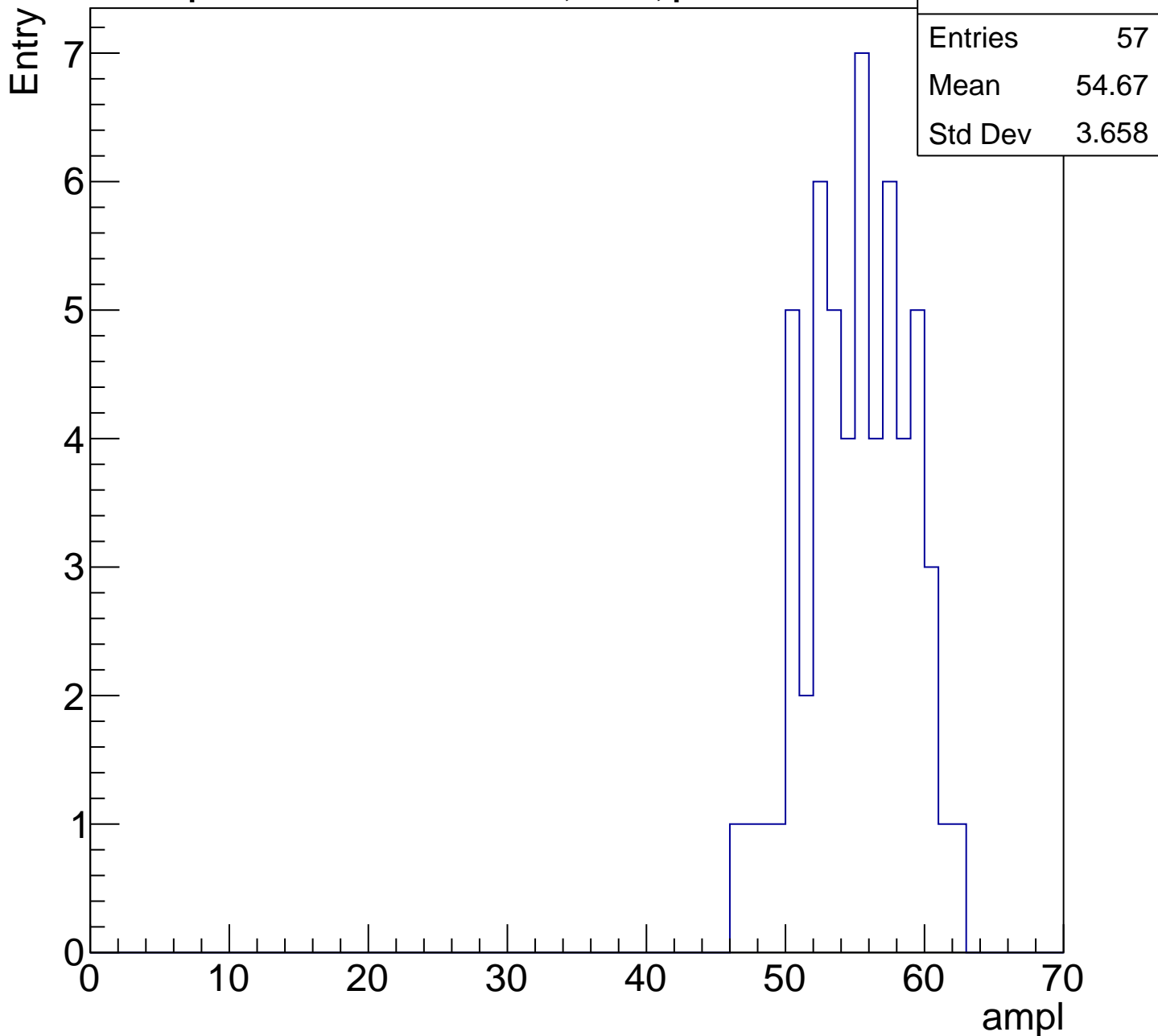
Entry

Entries	62
Mean	48.98
Std Dev	3.367



# B1L103S, U11-ch7, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

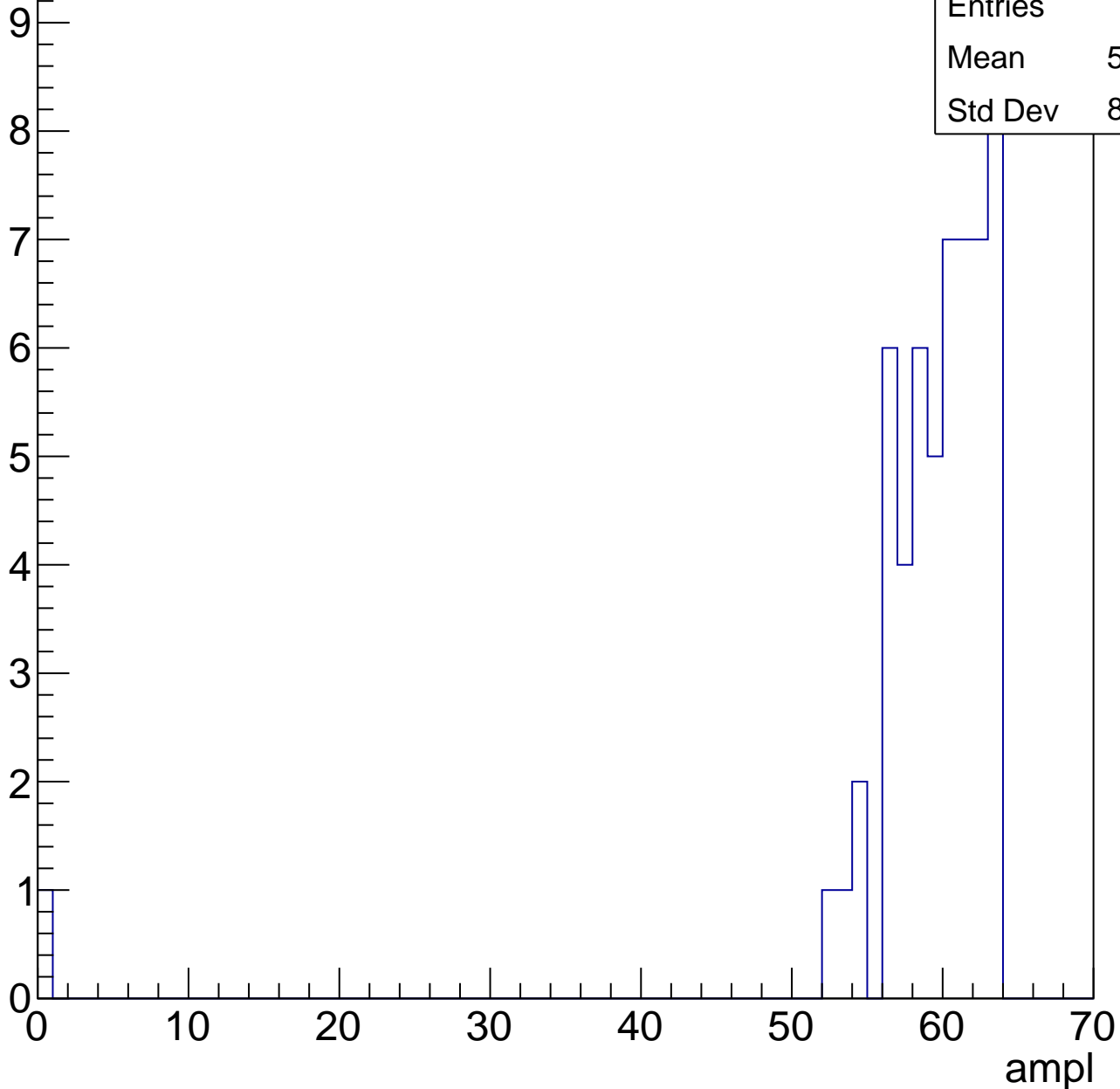


# B1L103S, U11-ch7, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	56
Mean	58.36
Std Dev	8.357



# B1L103S, U11-ch7, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	5
Mean	61.8
Std Dev	0.7483

ampl

0 10 20 30 40 50 60 70



# B1L103S, U11-ch7, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L103S, U11-ch8, adc0

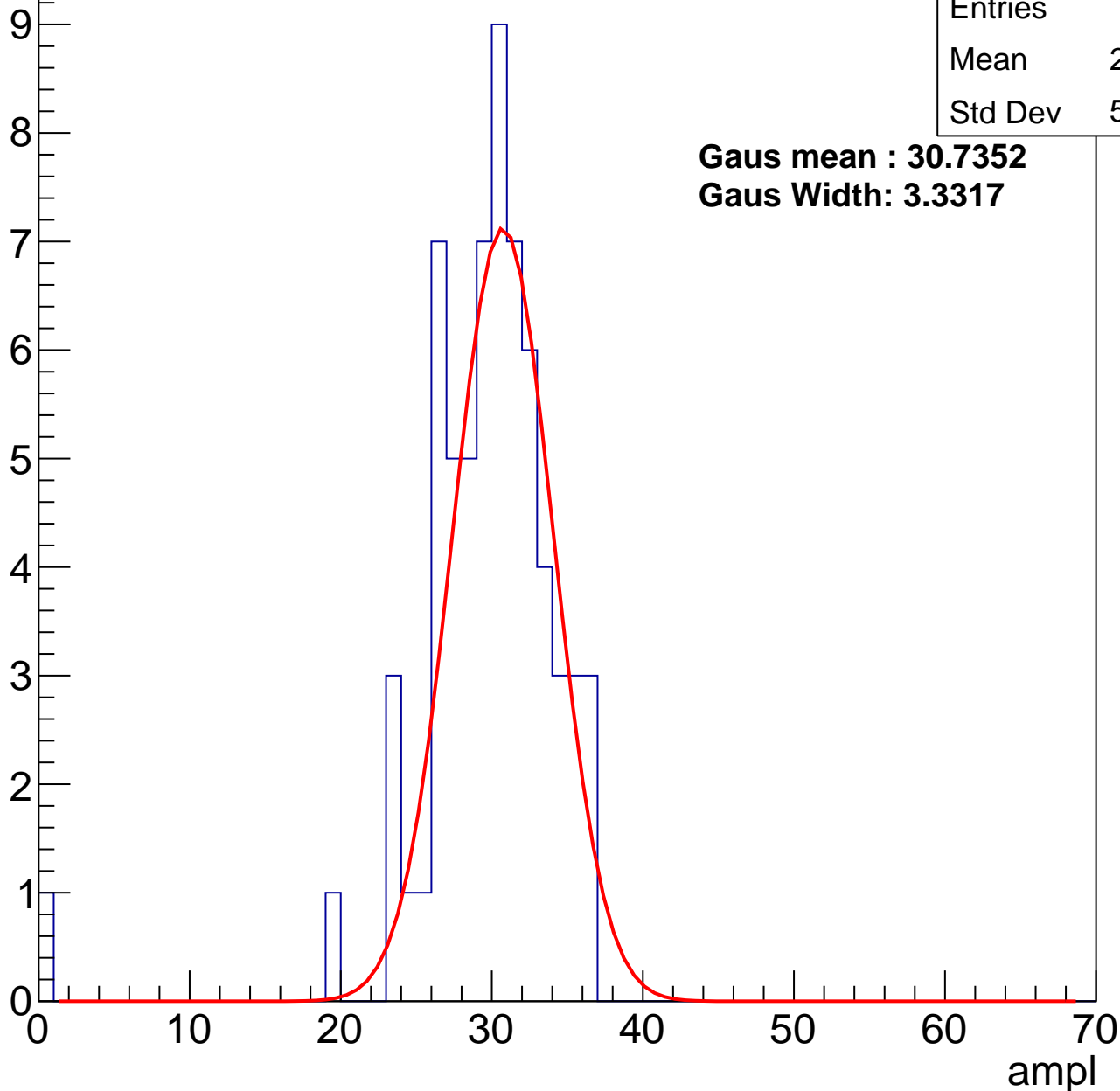
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	29.14
Std Dev	5.018

**Gaus mean : 30.7352**

**Gaus Width: 3.3317**



# B1L103S, U11-ch8, adc1

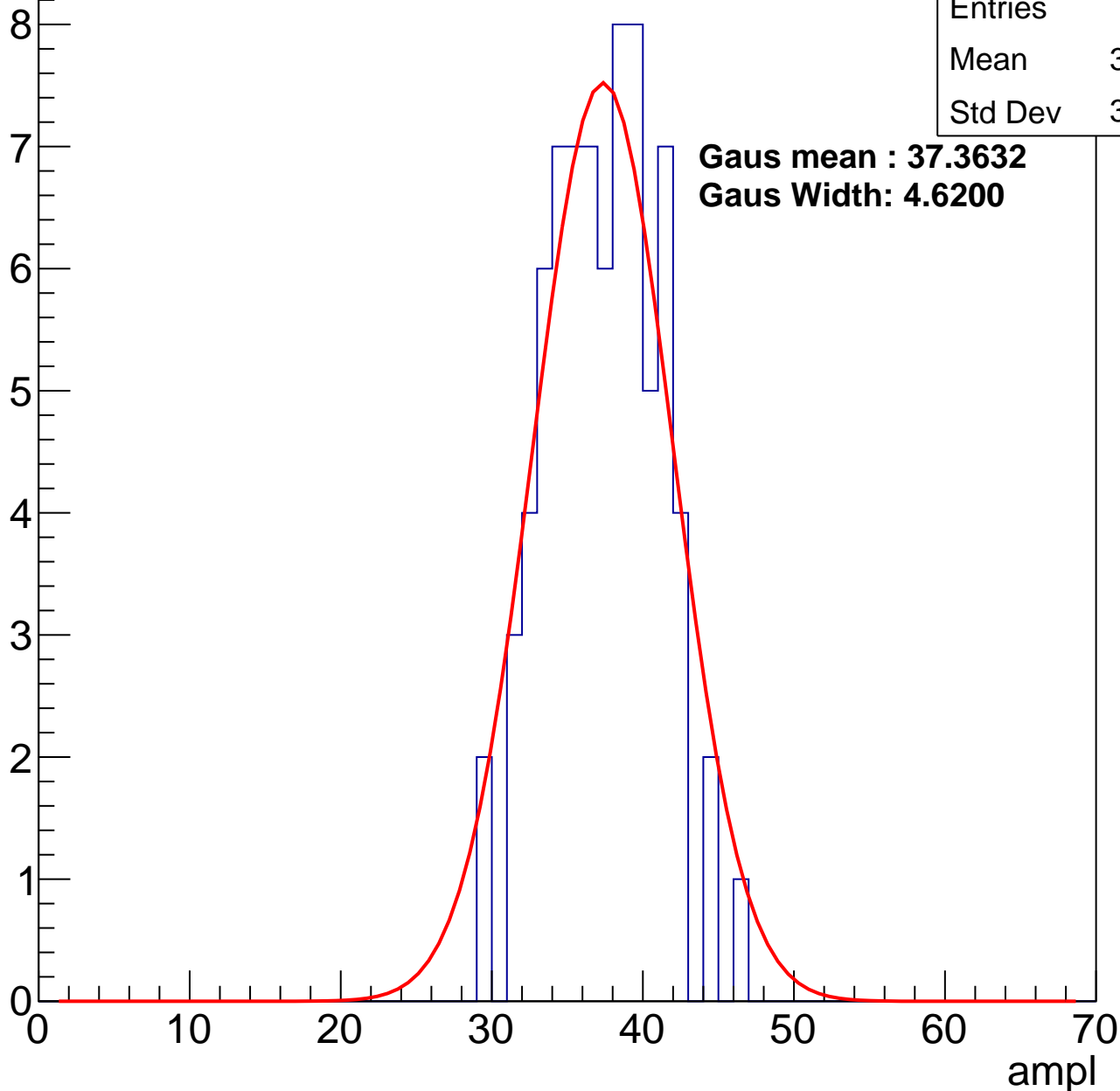
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	77
Mean	36.87
Std Dev	3.612

**Gaus mean : 37.3632**

**Gaus Width: 4.6200**



# B1L103S, U11-ch8, adc2

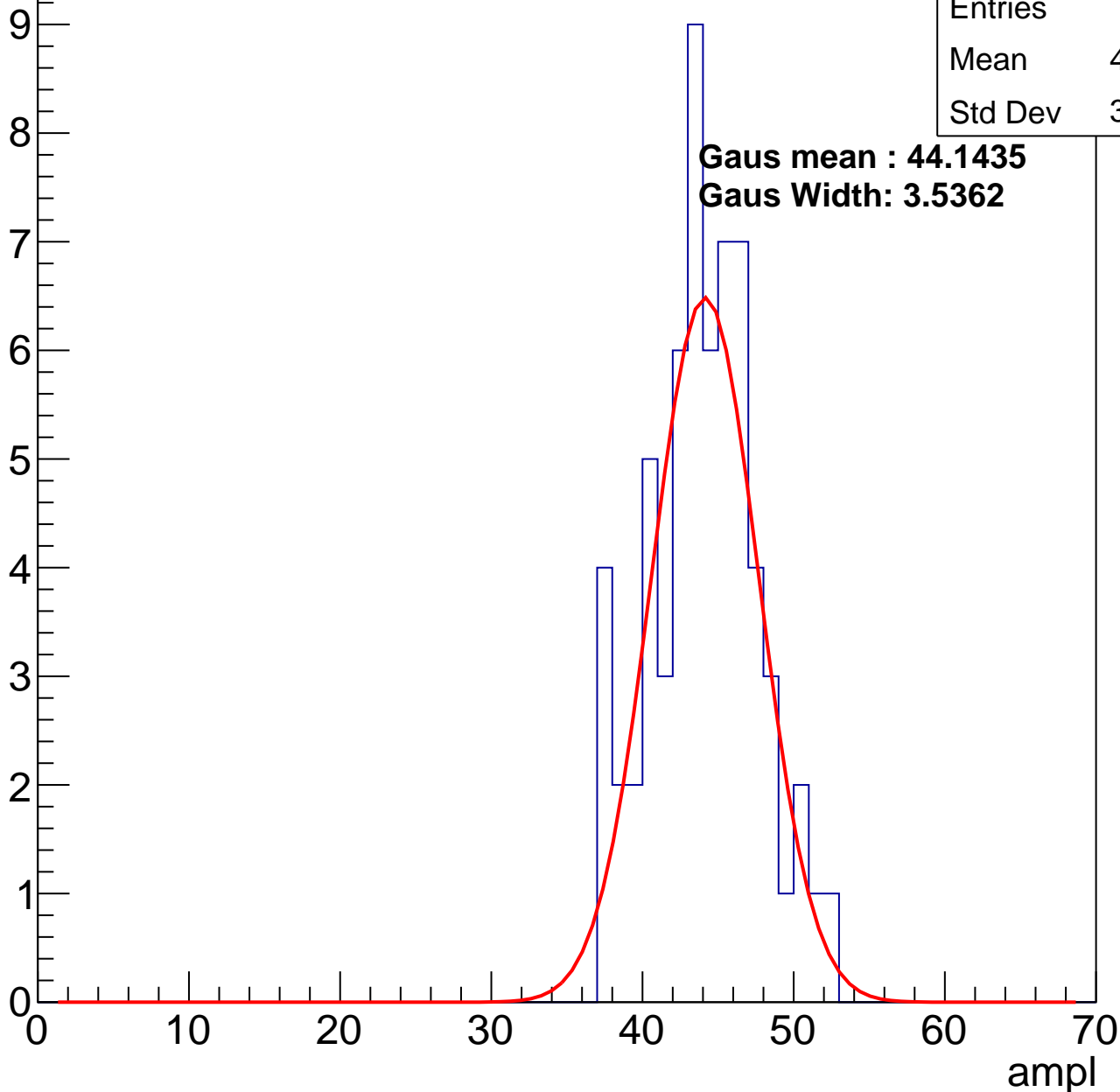
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	43.63
Std Dev	3.516

**Gaus mean : 44.1435**

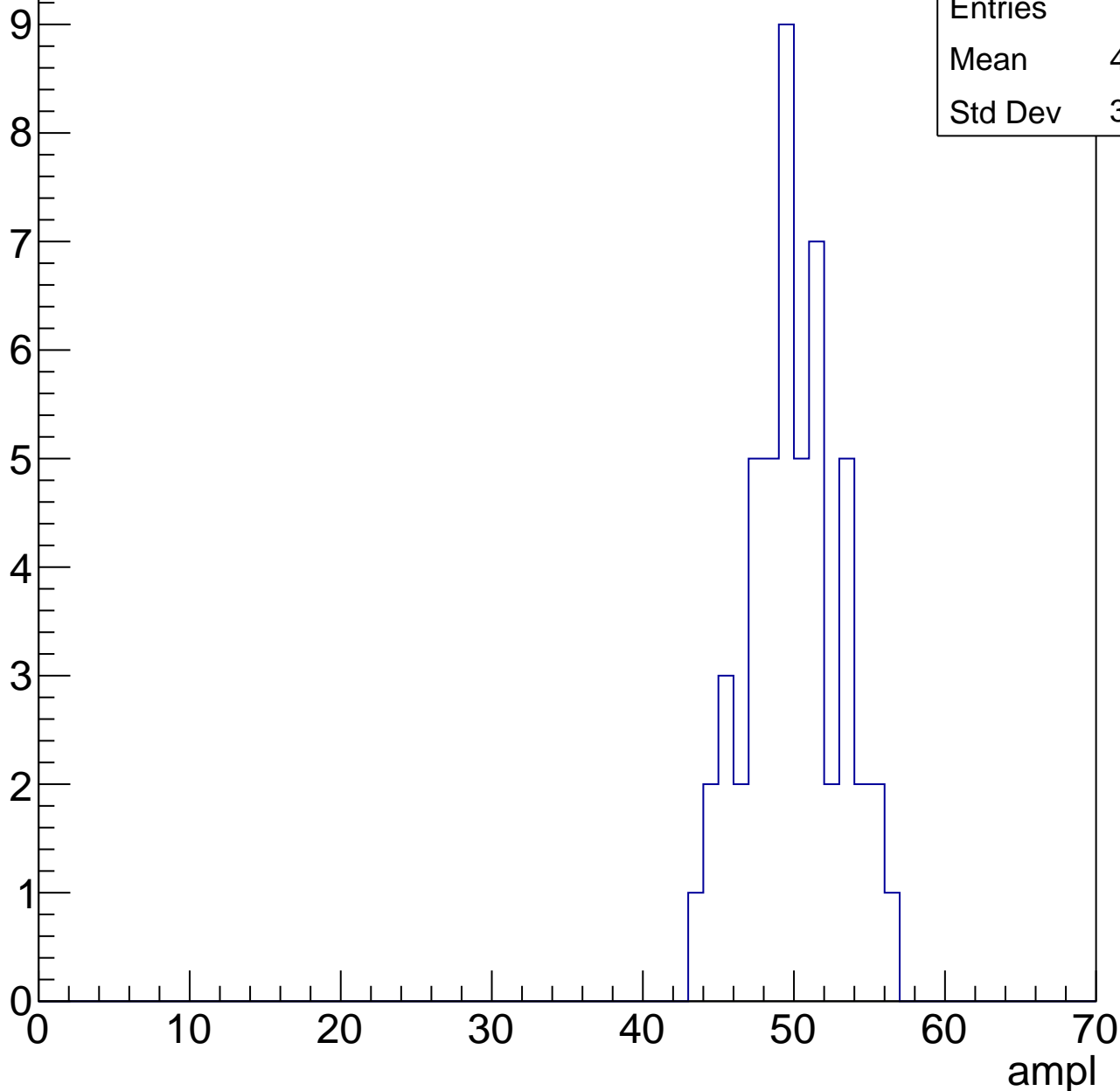
**Gaus Width: 3.5362**



# B1L103S, U11-ch8, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

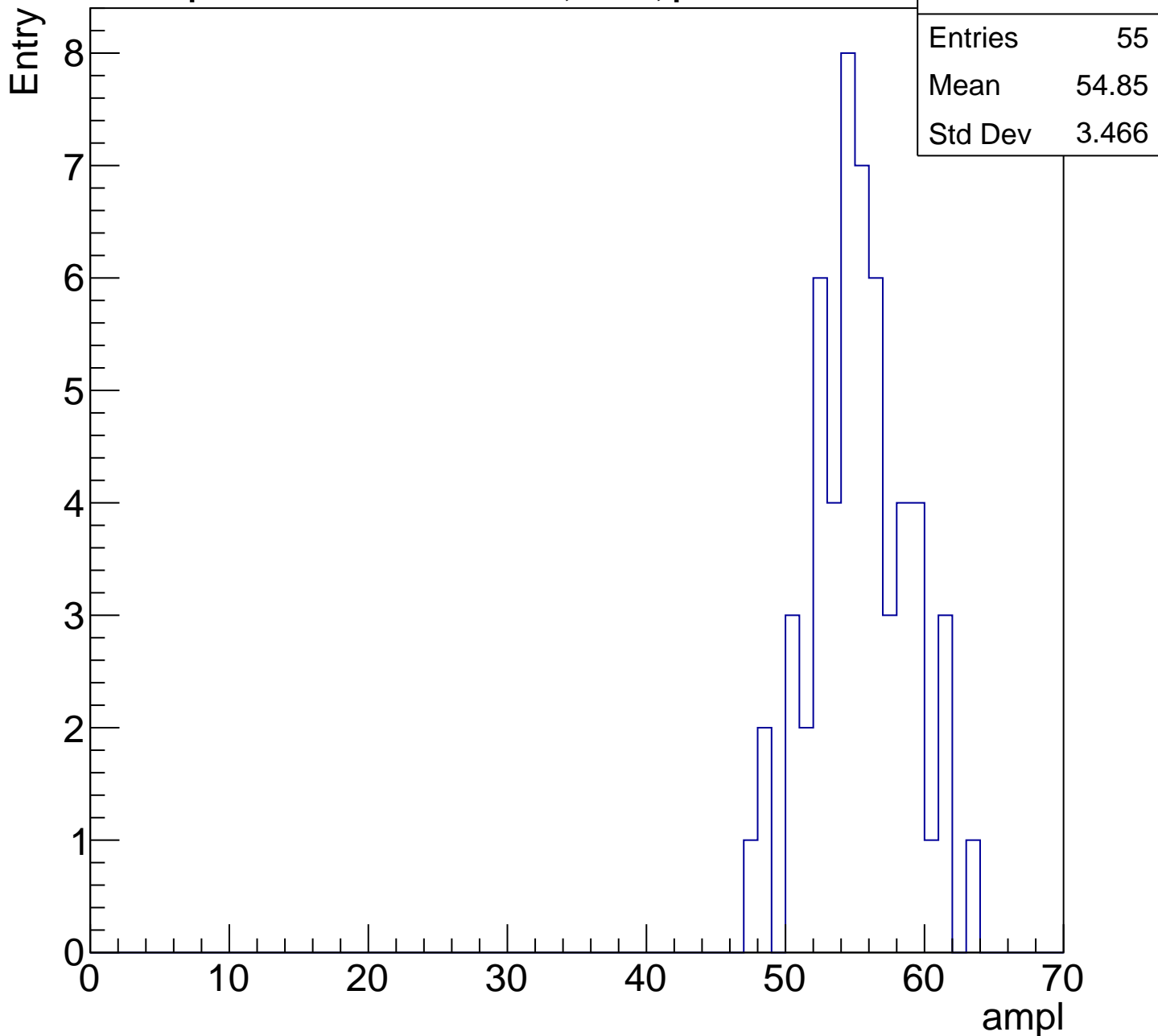
Entry



Entries	51
Mean	49.49
Std Dev	3.025

# B1L103S, U11-ch8, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U11-ch8, adc5

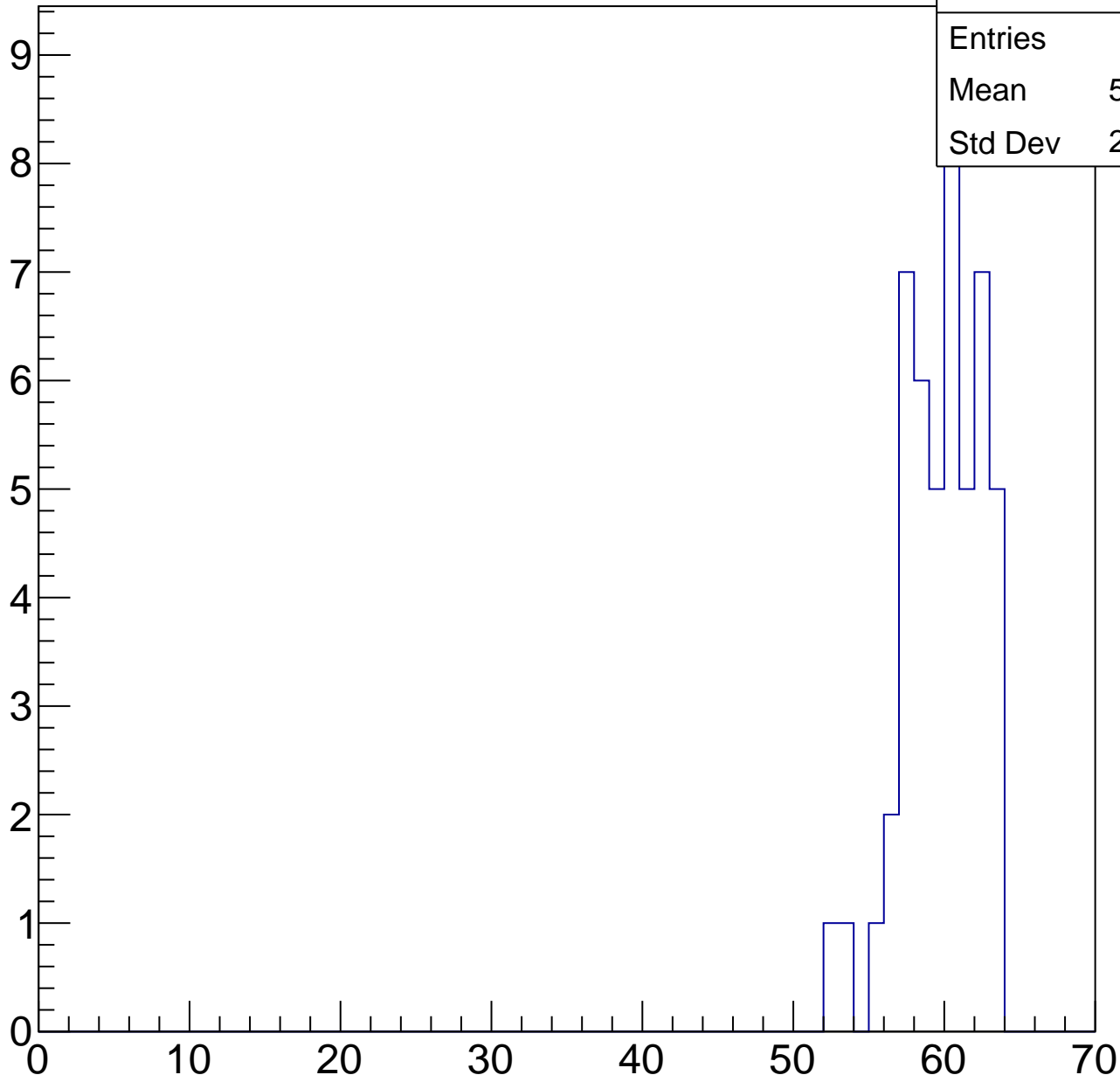
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	49
Mean	59.35
Std Dev	2.552

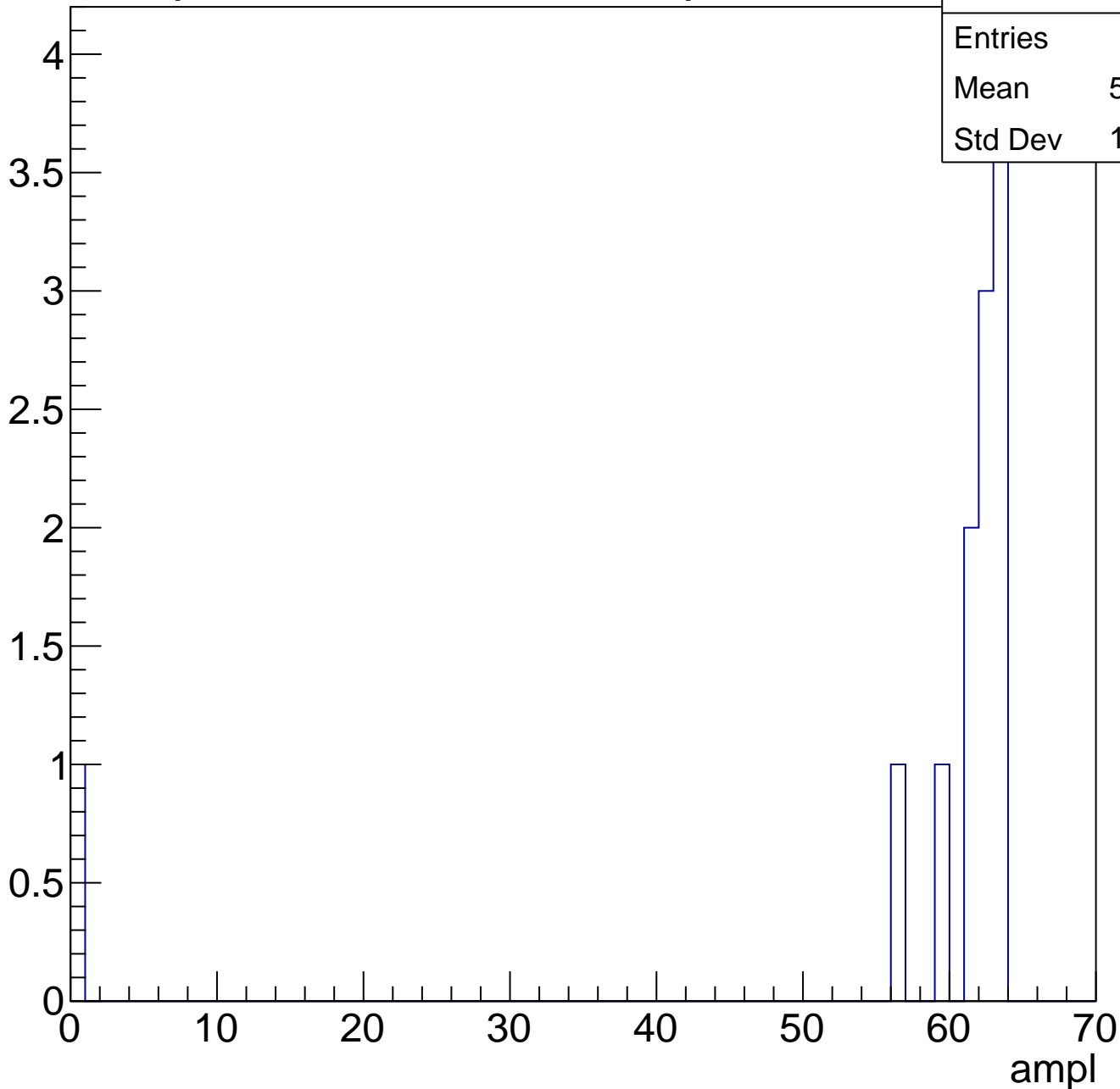
ampl



# B1L103S, U11-ch8, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

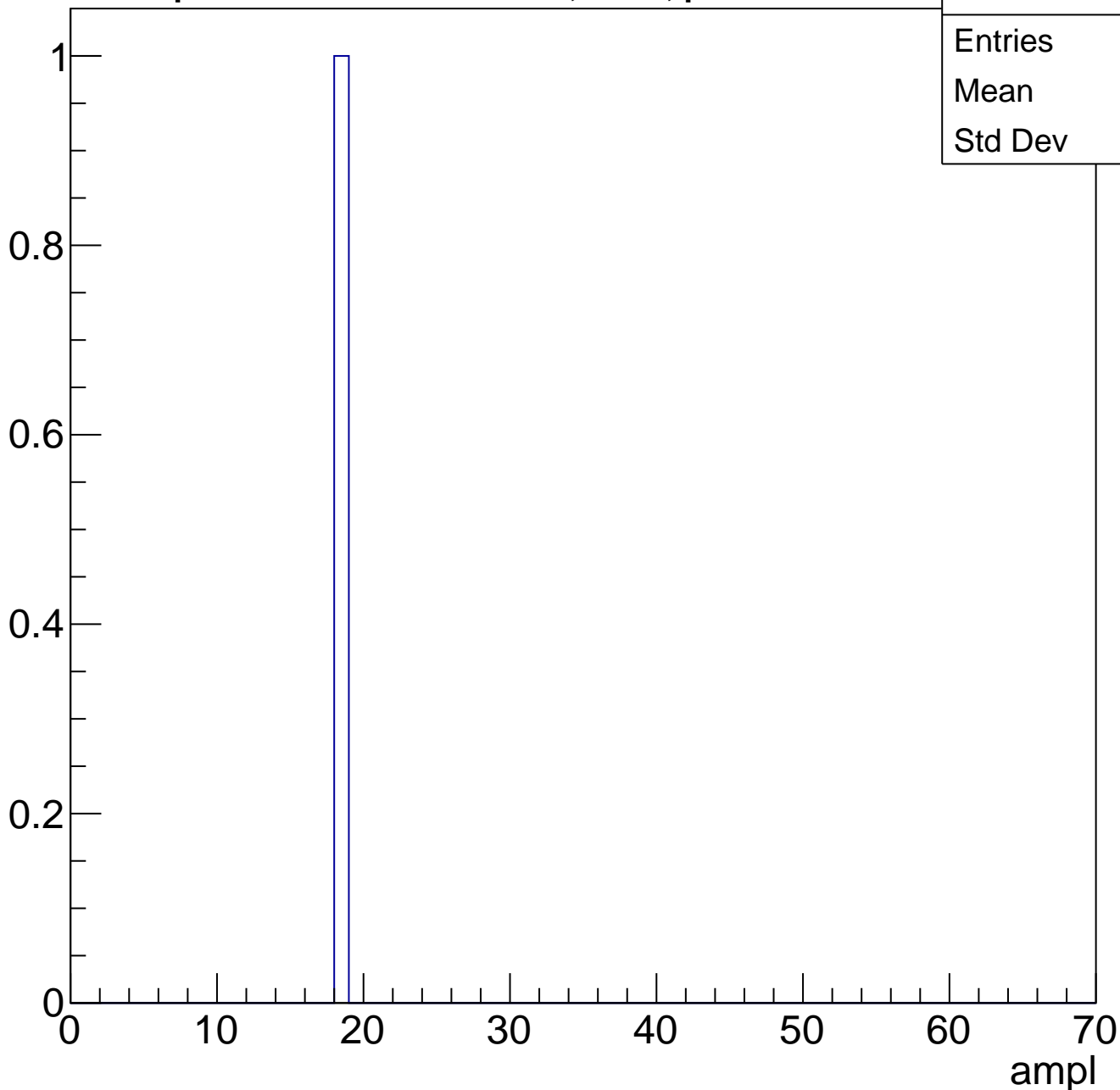




# B1L103S, U11-ch8, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	18
Std Dev	0

# B1L103S, U11-ch9, adc0

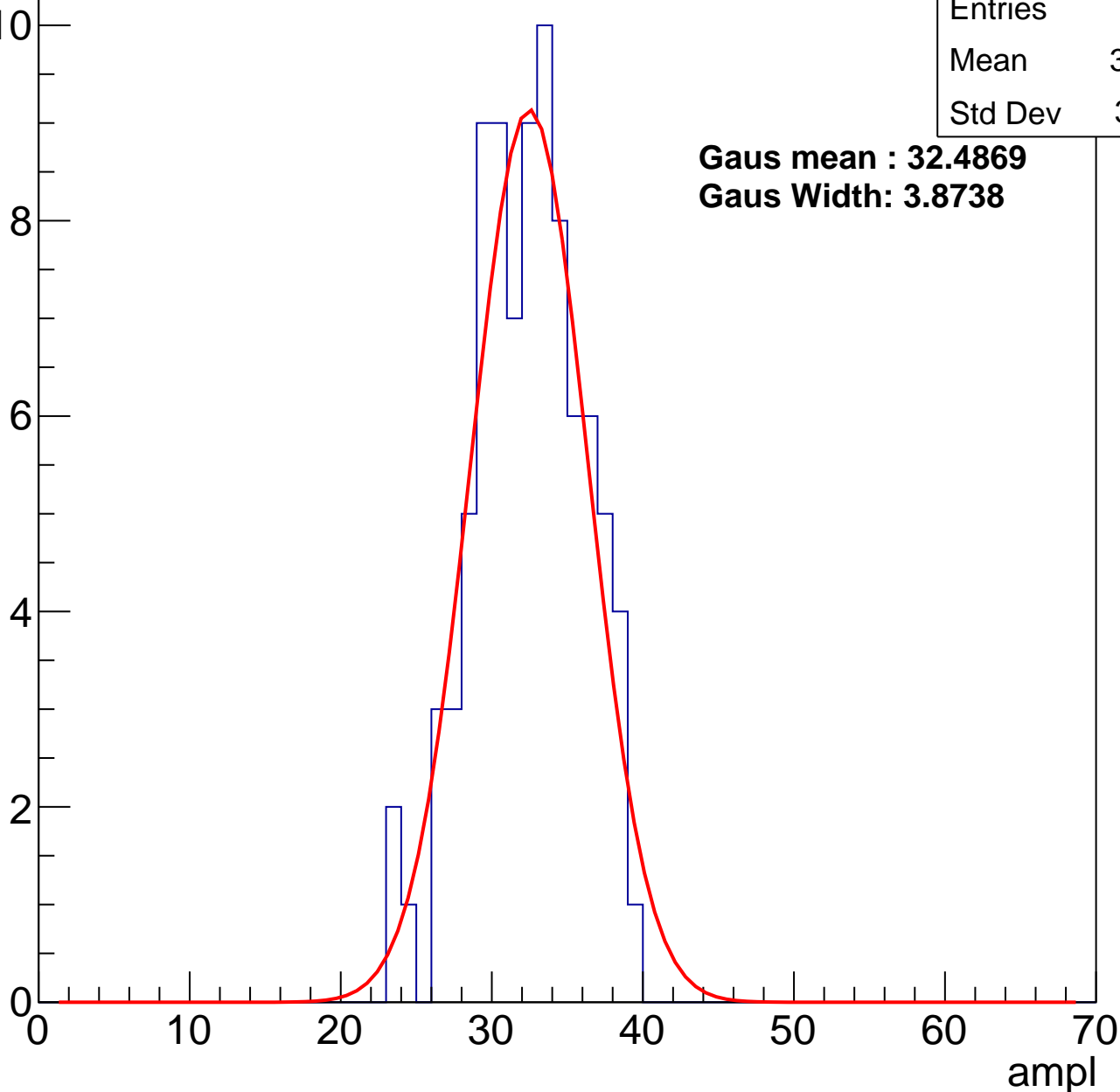
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	88
Mean	31.92
Std Dev	3.571

**Gaus mean : 32.4869**

**Gaus Width: 3.8738**



# B1L103S, U11-ch9, adc1

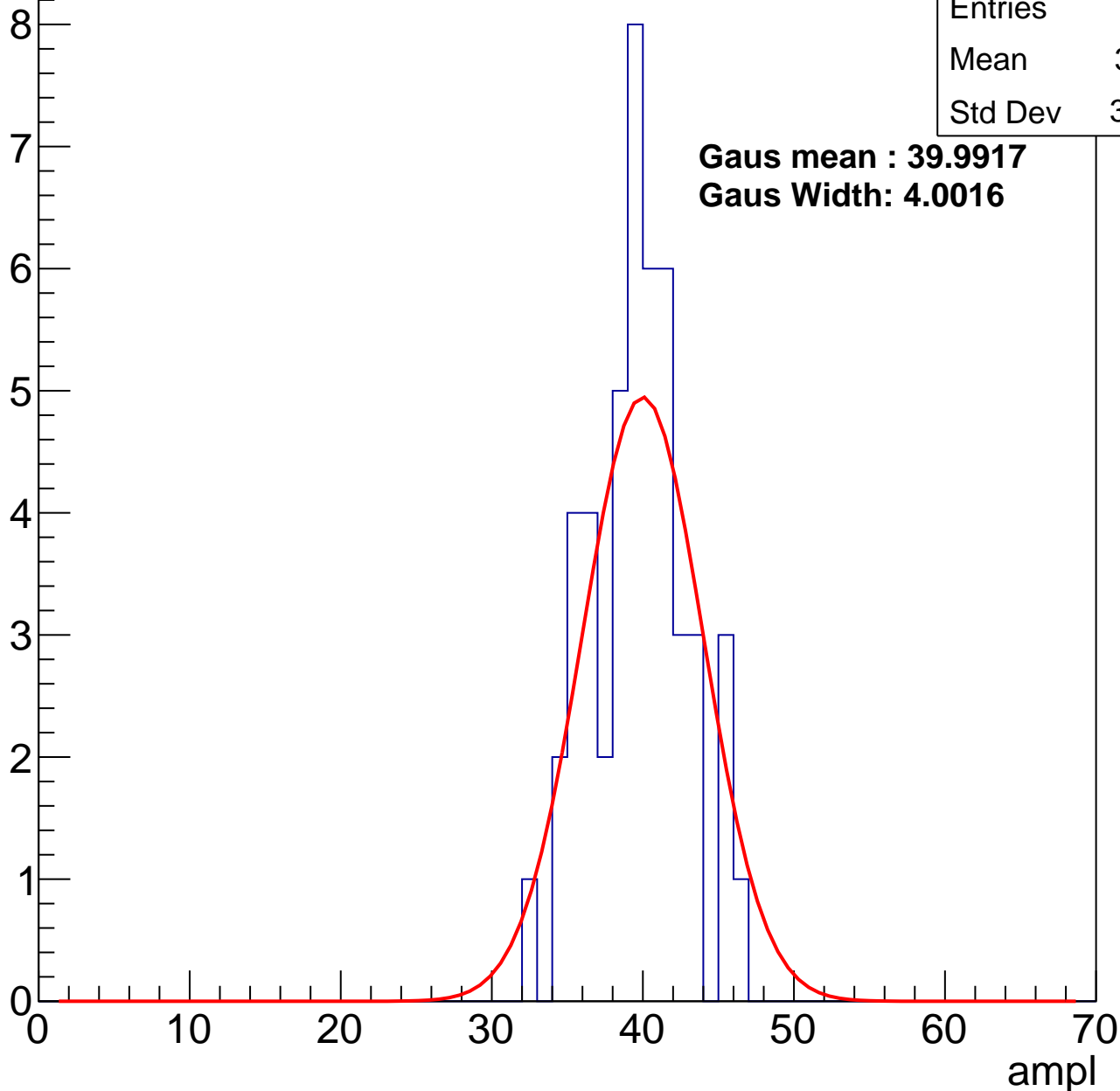
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	48
Mean	39.21
Std Dev	3.136

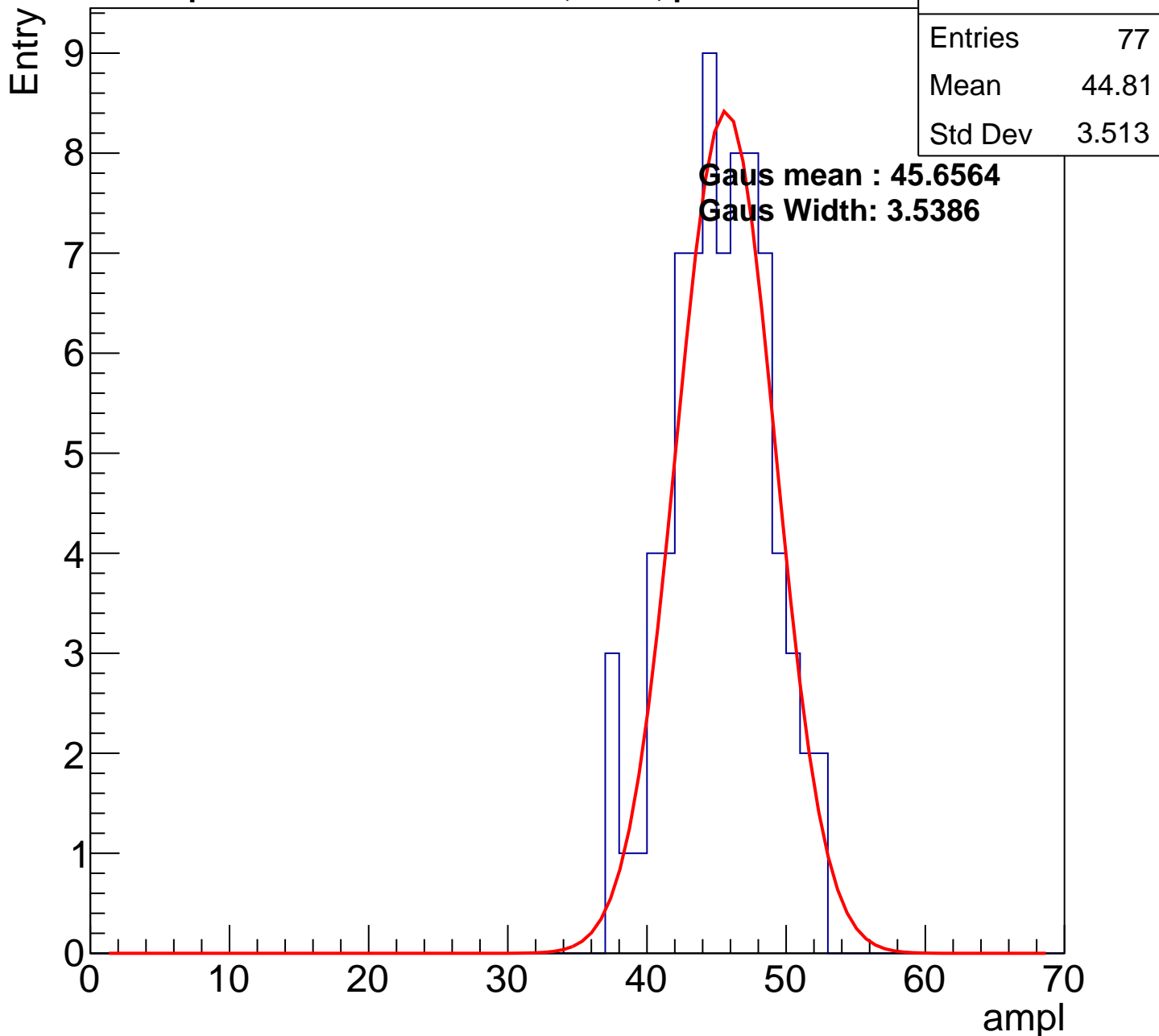
**Gaus mean : 39.9917**

**Gaus Width: 4.0016**



# B1L103S, U11-ch9, adc2

calib\_packv5\_042523\_0143.root, FC#7, port C2

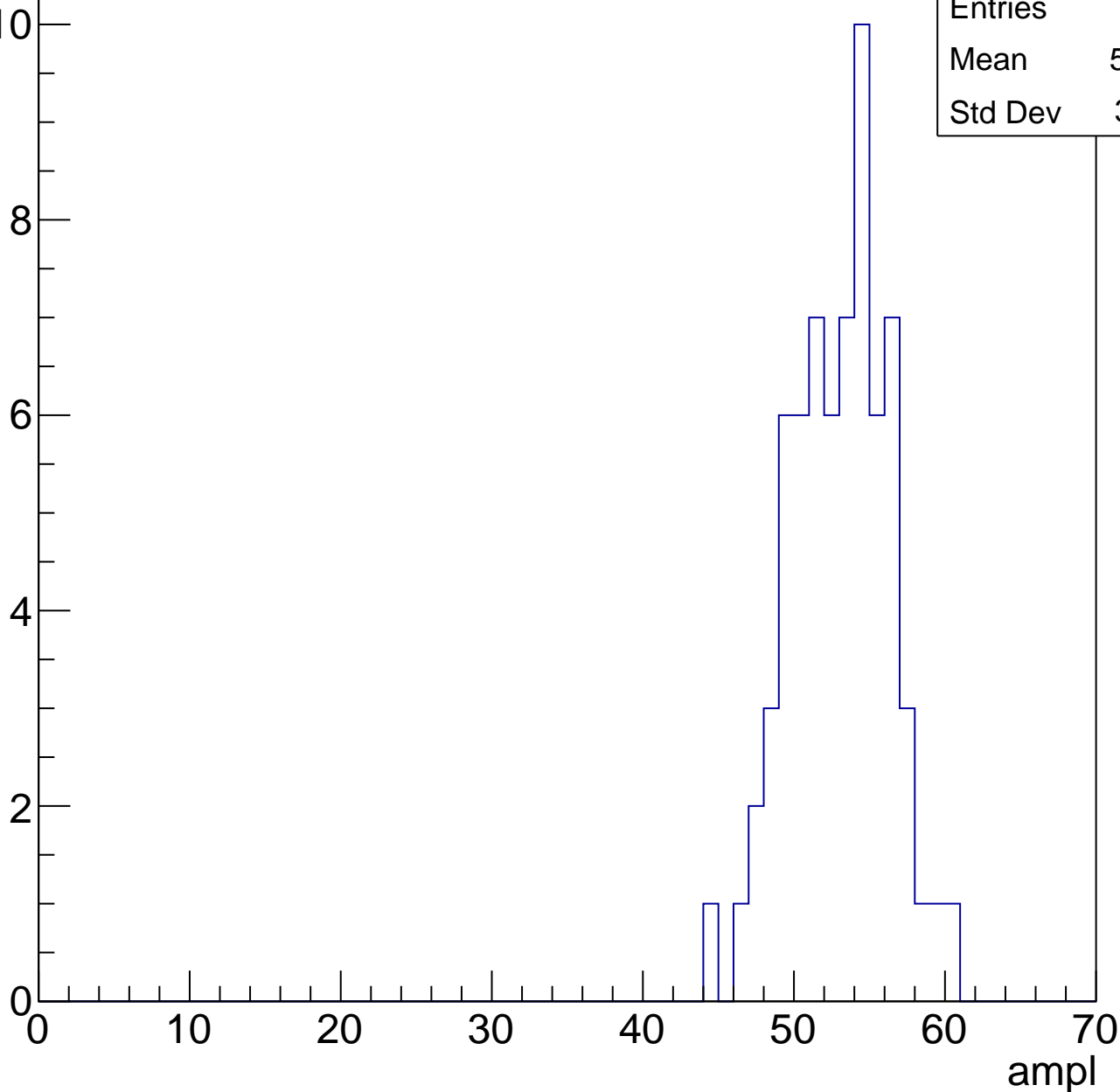


# B1L103S, U11-ch9, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

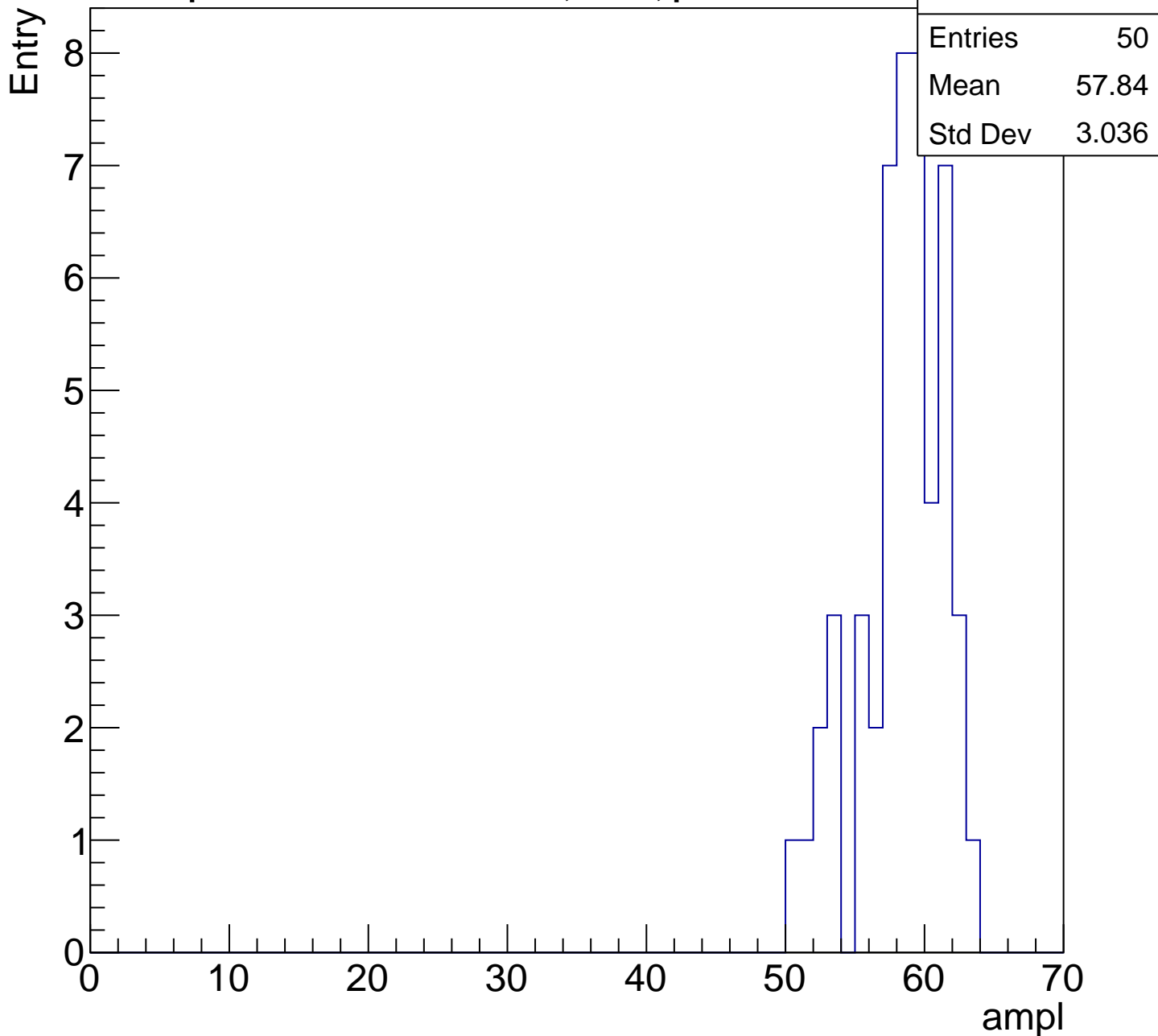
Entry

Entries	68
Mean	52.53
Std Dev	3.211



# B1L103S, U11-ch9, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

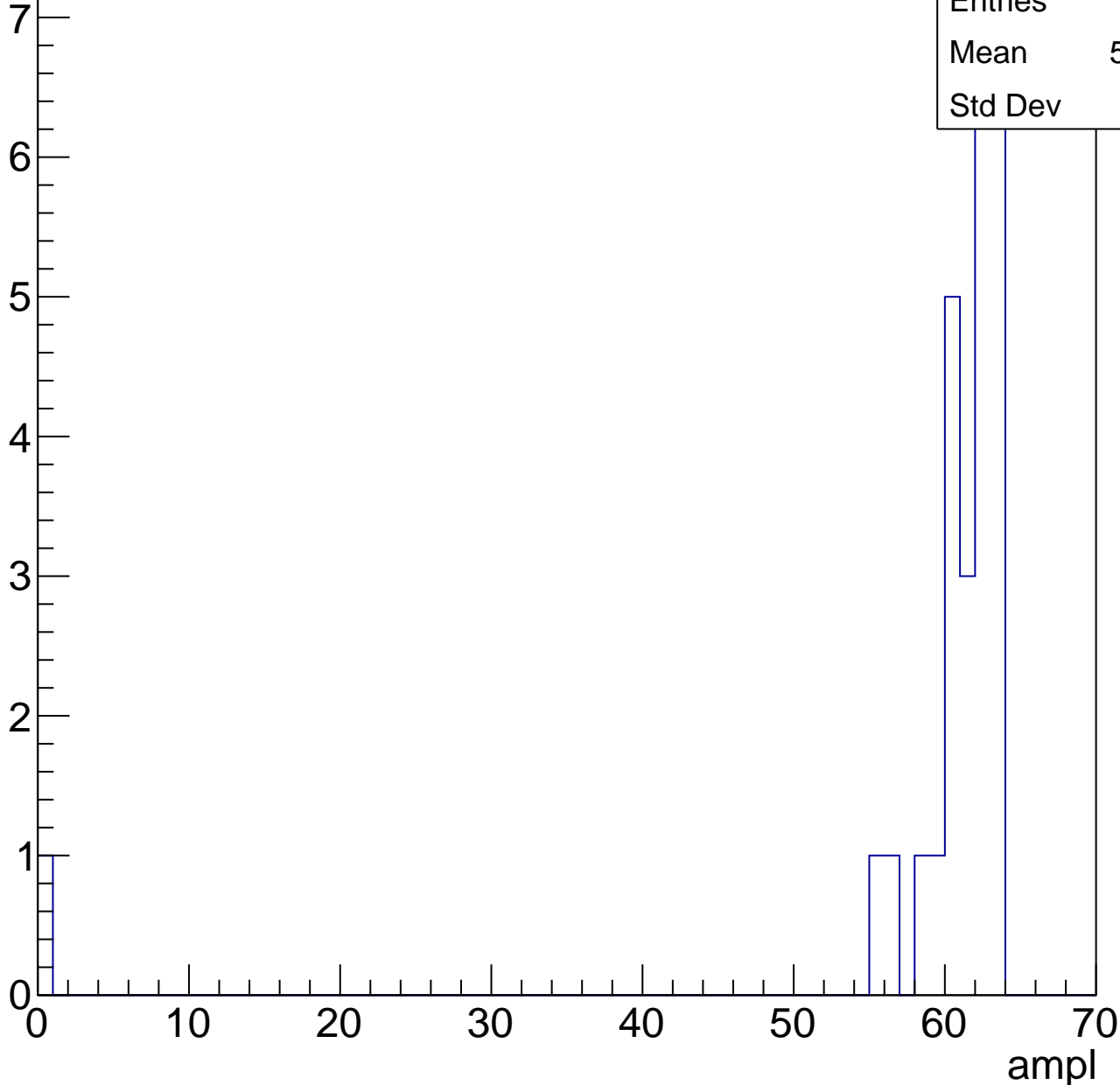


# B1L103S, U11-ch9, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	27
Mean	58.74
Std Dev	11.7



# B1L103S, U11-ch9, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	2
Mean	63
Std Dev	0

0 10 20 30 40 50 60 70

ampl



# B1L103S, U11-ch9, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U11-ch10, adc0

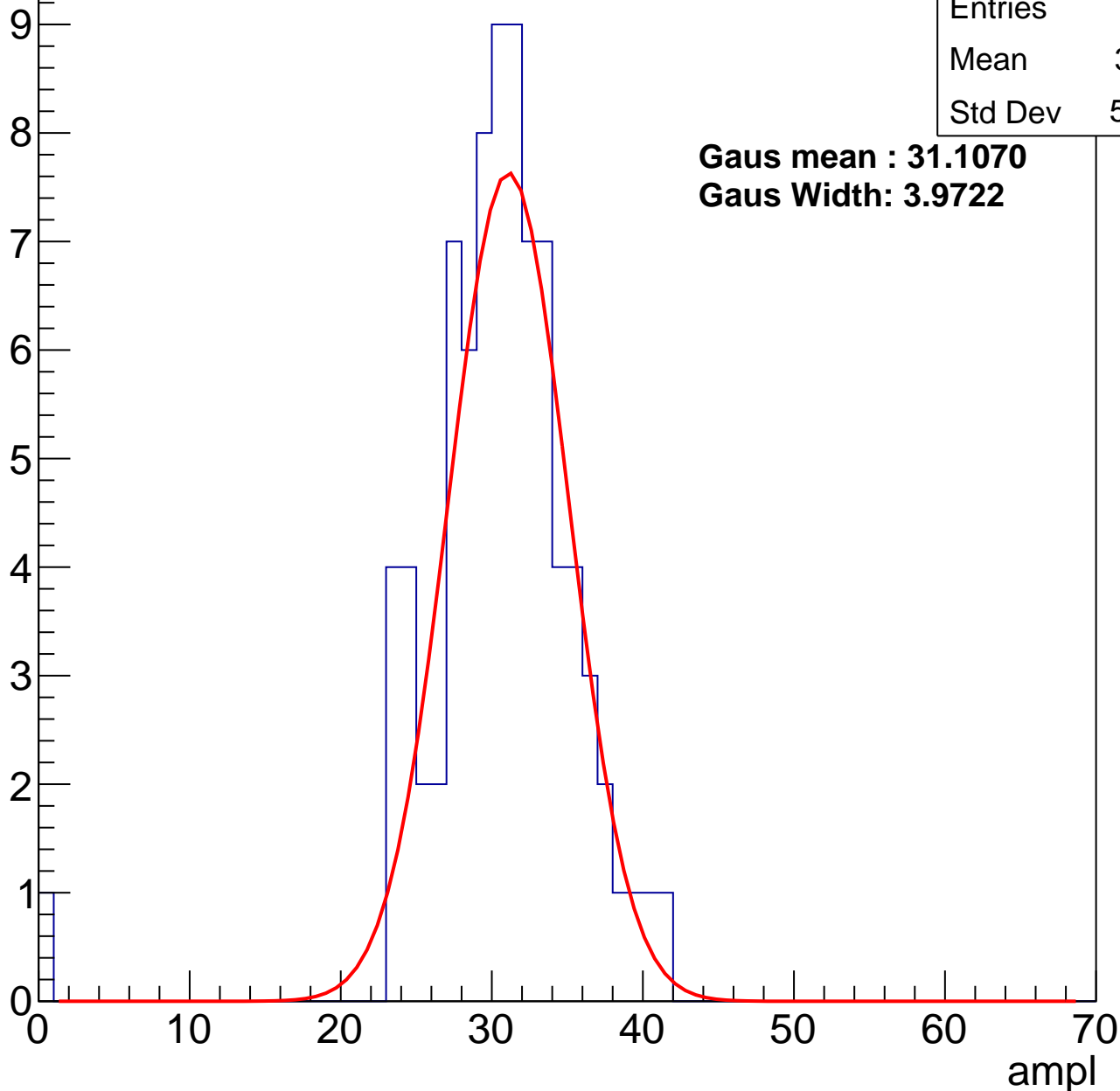
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	83
Mean	30.11
Std Dev	5.209

**Gaus mean : 31.1070**

**Gaus Width: 3.9722**



# B1L103S, U11-ch10, adc1

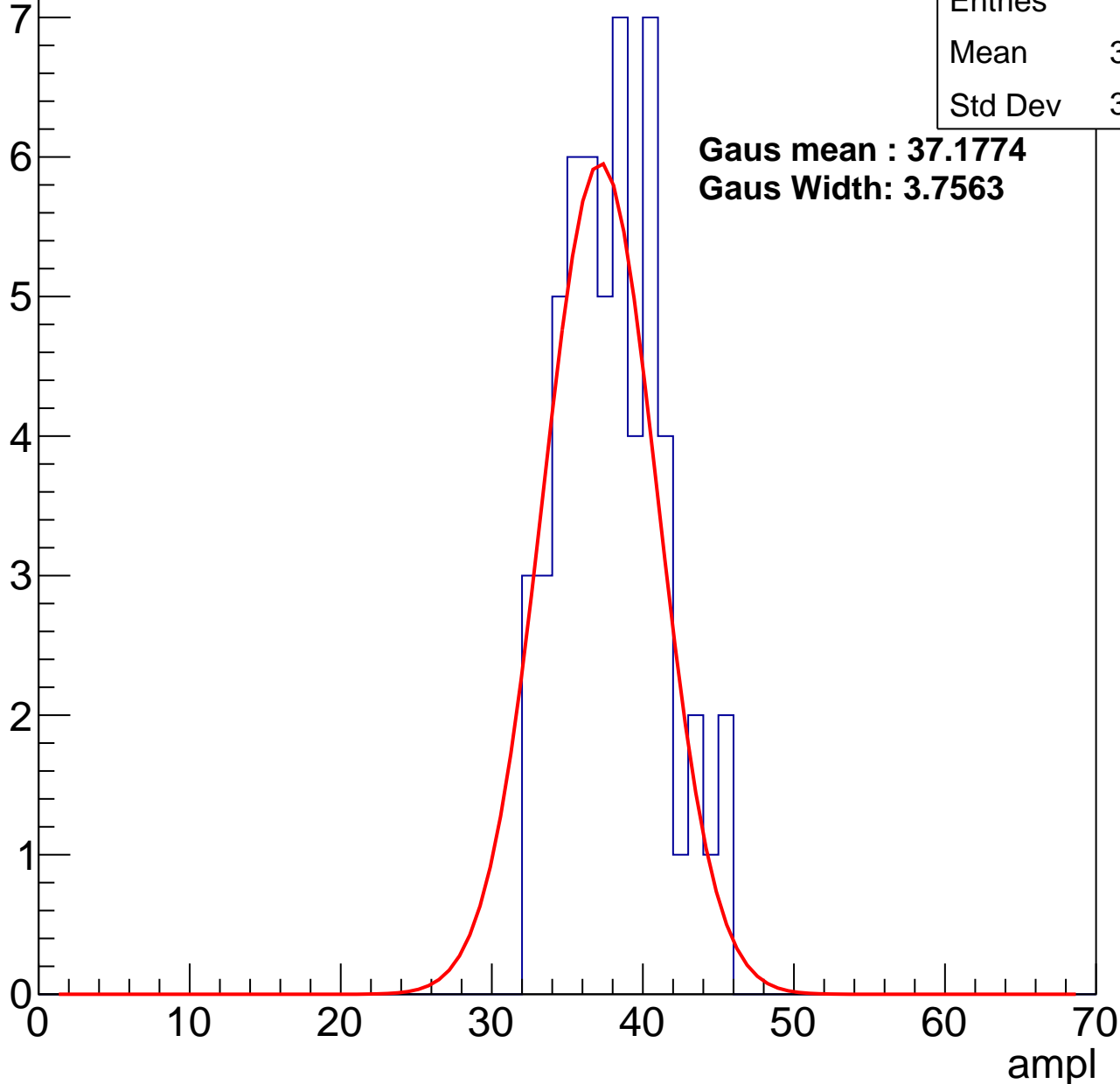
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	56
Mean	37.57
Std Dev	3.283

**Gaus mean : 37.1774**

**Gaus Width: 3.7563**



# B1L103S, U11-ch10, adc2

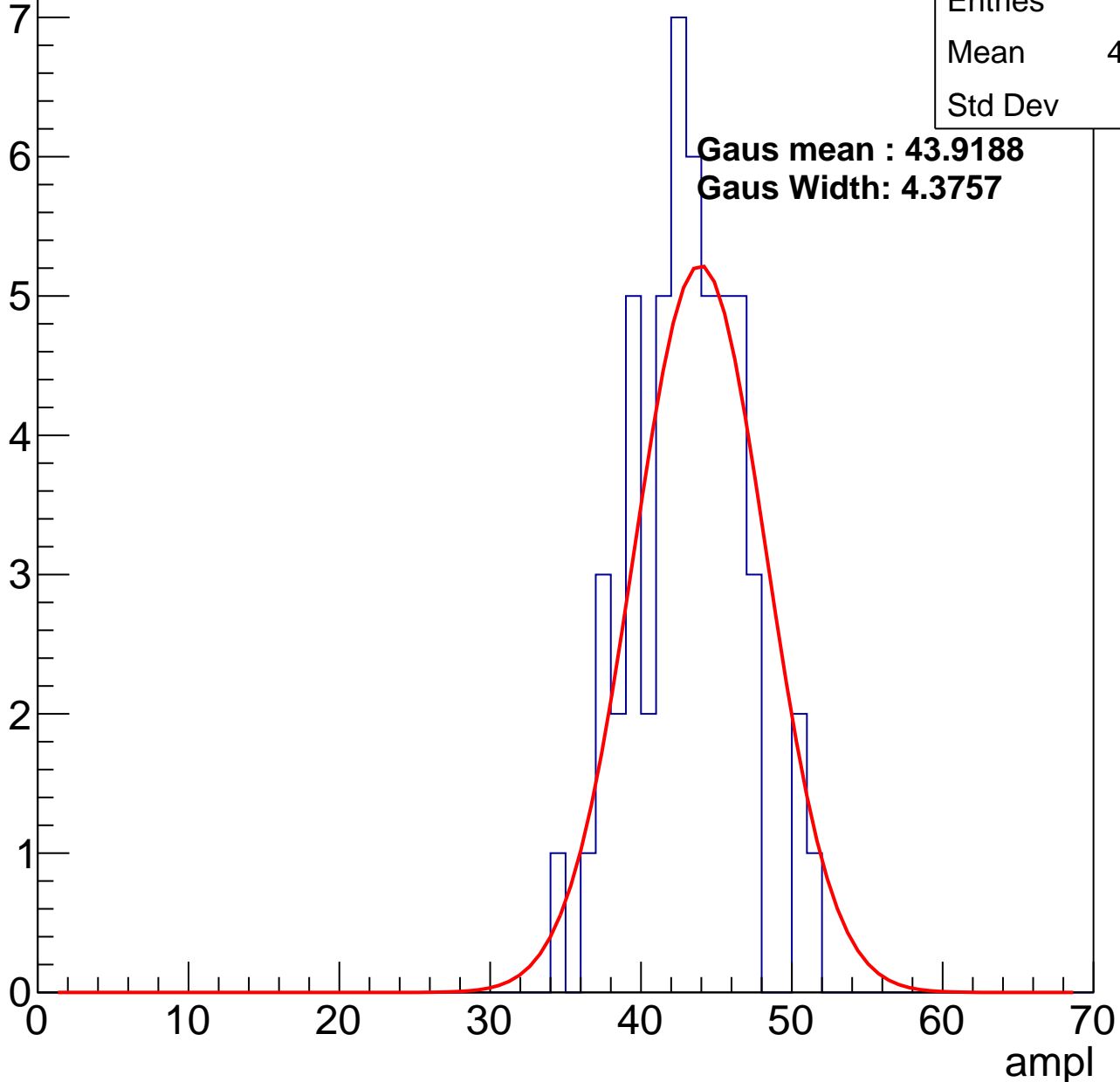
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	53
Mean	42.57
Std Dev	3.59

**Gaus mean : 43.9188**

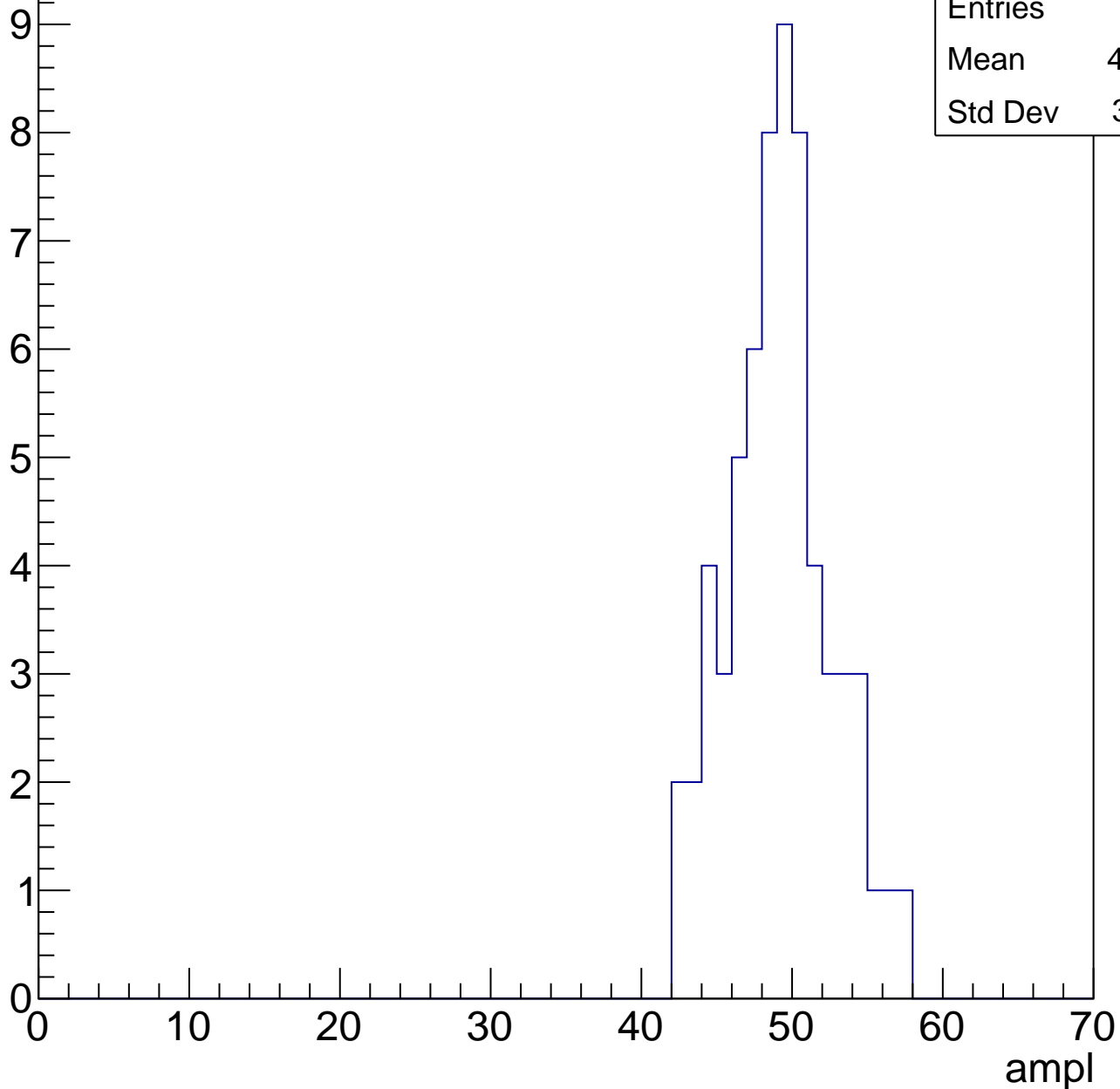
**Gaus Width: 4.3757**



# B1L103S, U11-ch10, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

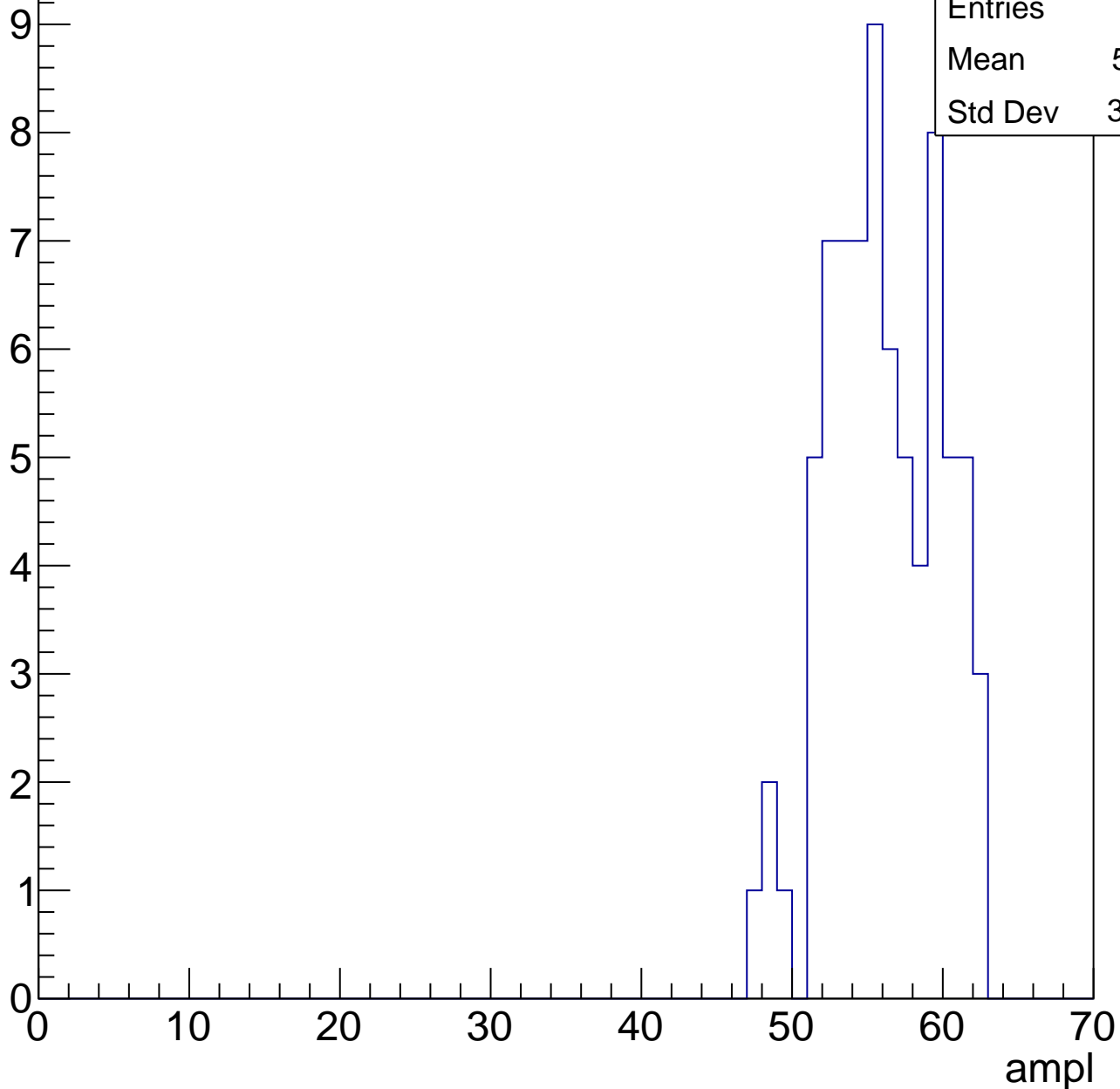


Entries	63
Mean	48.68
Std Dev	3.361

# B1L103S, U11-ch10, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



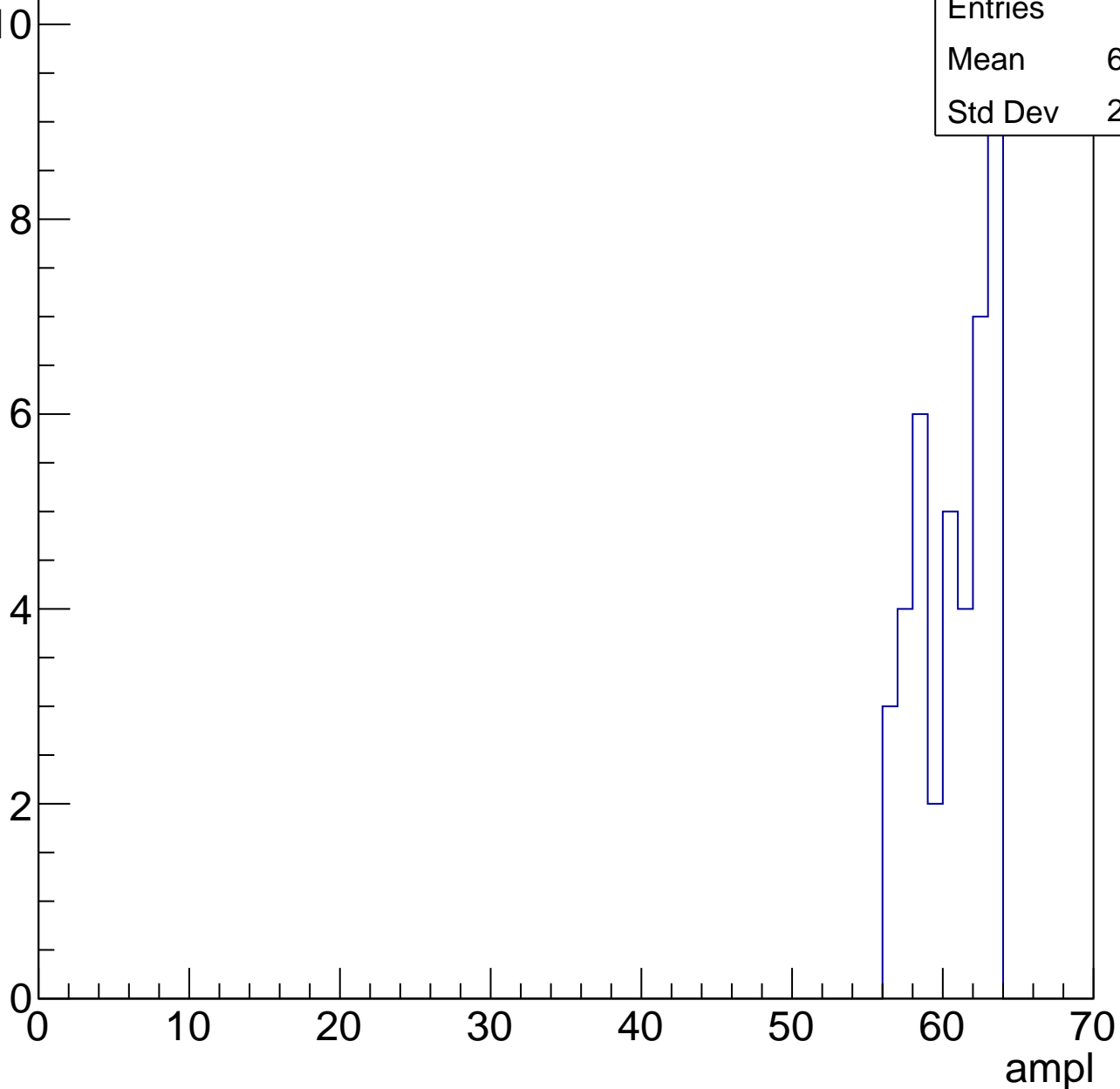
Entries	75
Mean	55.61
Std Dev	3.633

# B1L103S, U11-ch10, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

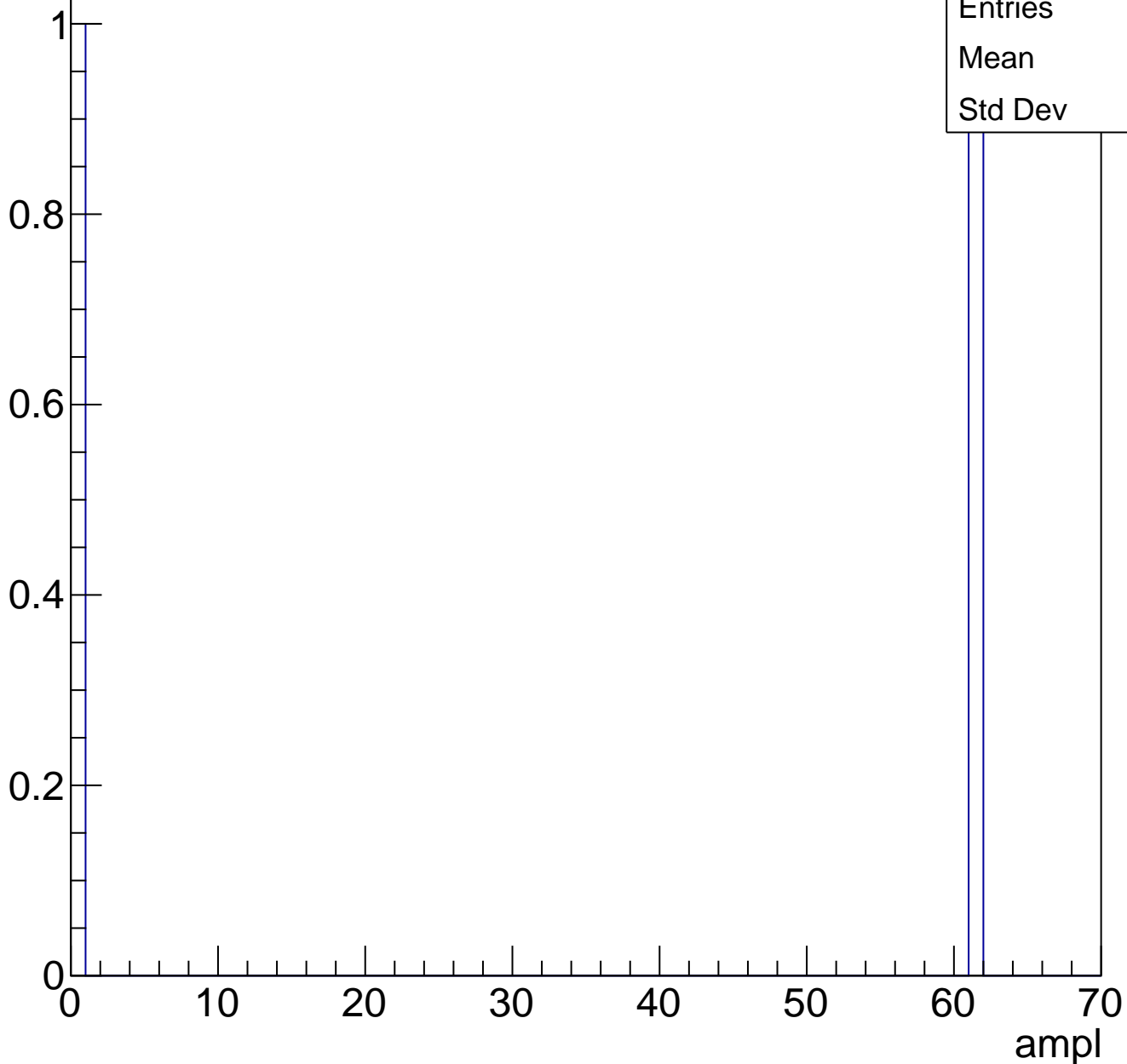
Entries	41
Mean	60.24
Std Dev	2.366



# B1L103S, U11-ch10, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U11-ch10, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U11-ch11, adc0

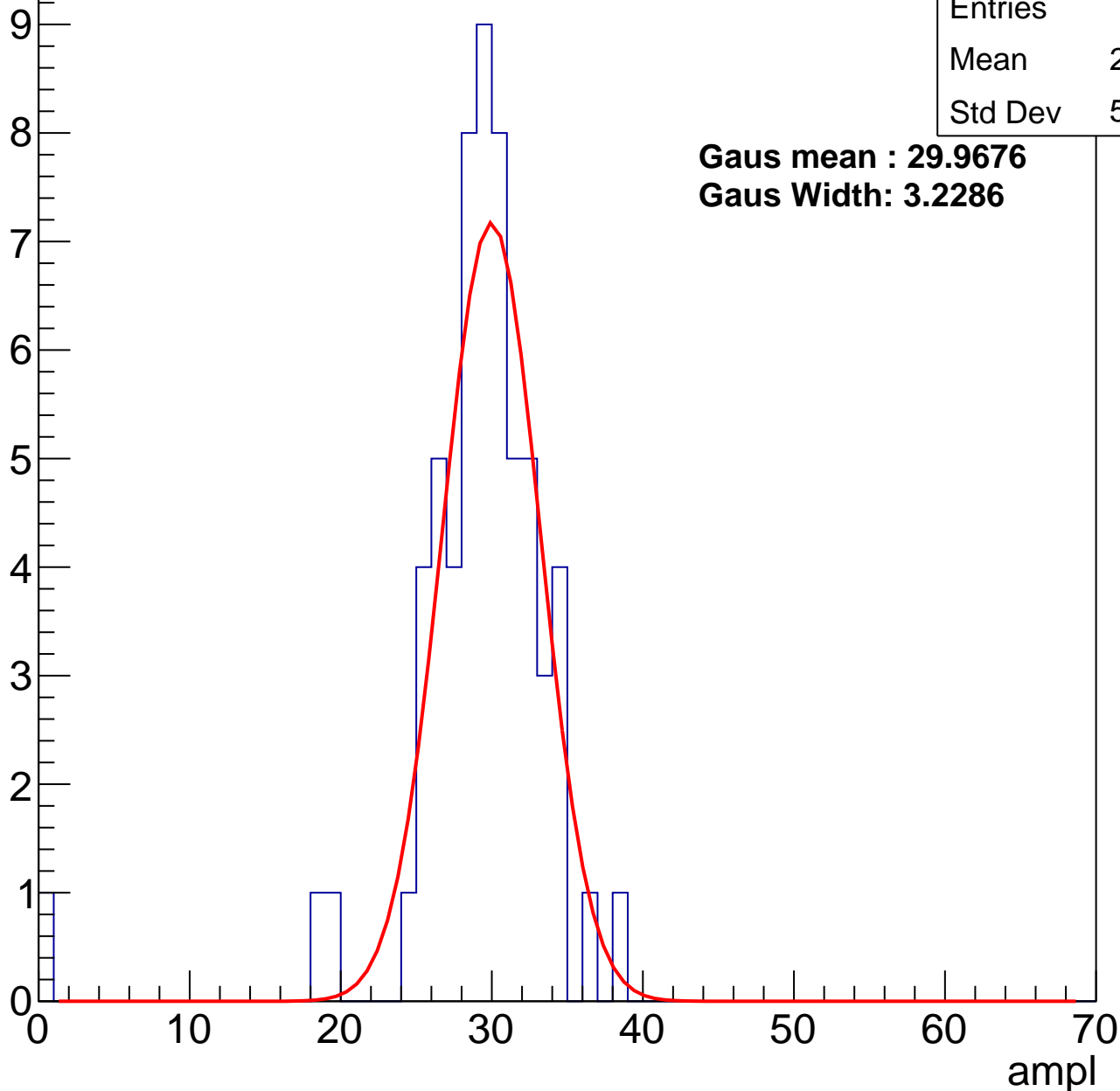
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	61
Mean	28.66
Std Dev	5.063

**Gaus mean : 29.9676**

**Gaus Width: 3.2286**



# B1L103S, U11-ch11, adc1

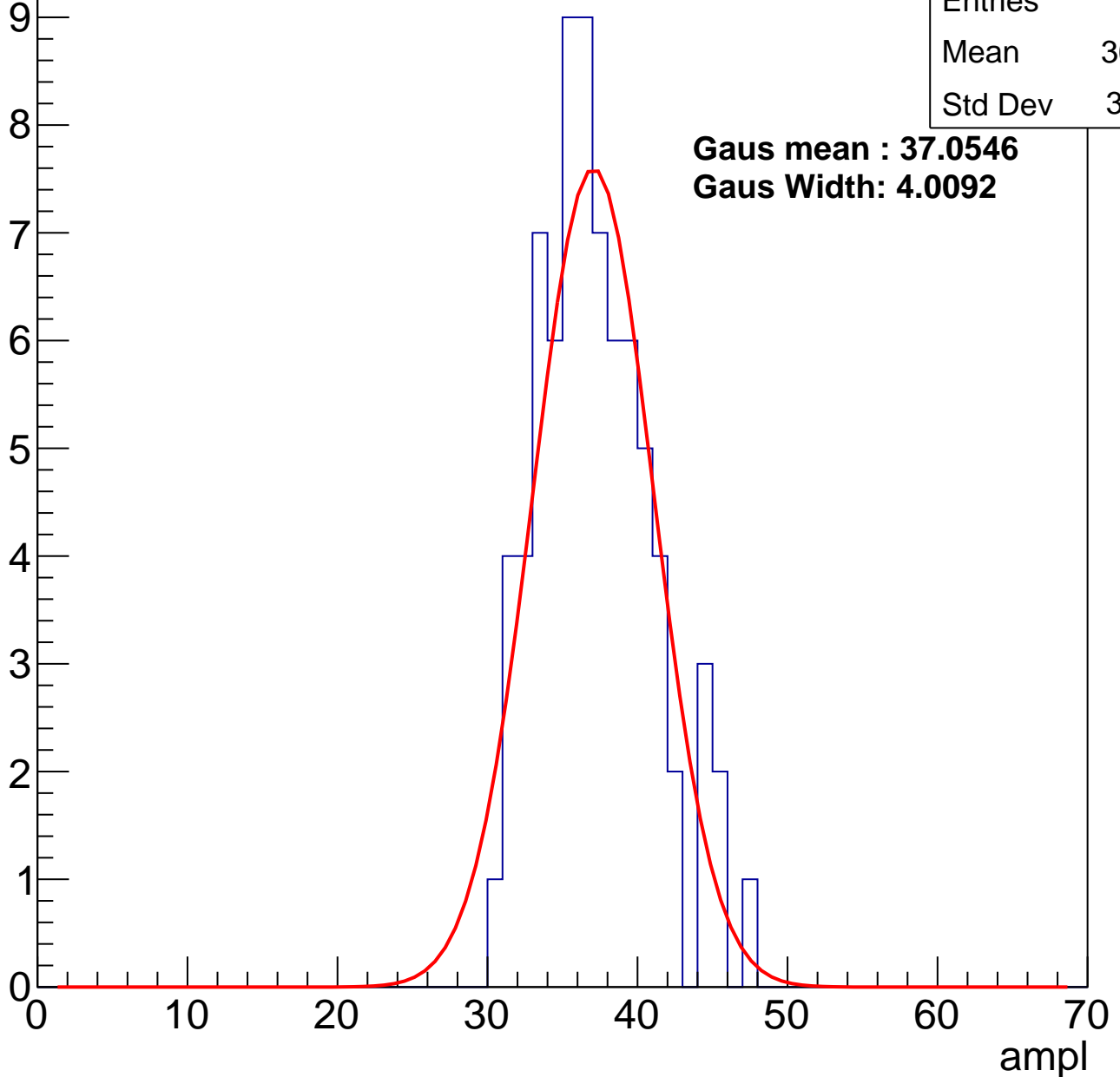
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	76
Mean	36.76
Std Dev	3.741

**Gaus mean : 37.0546**

**Gaus Width: 4.0092**



# B1L103S, U11-ch11, adc2

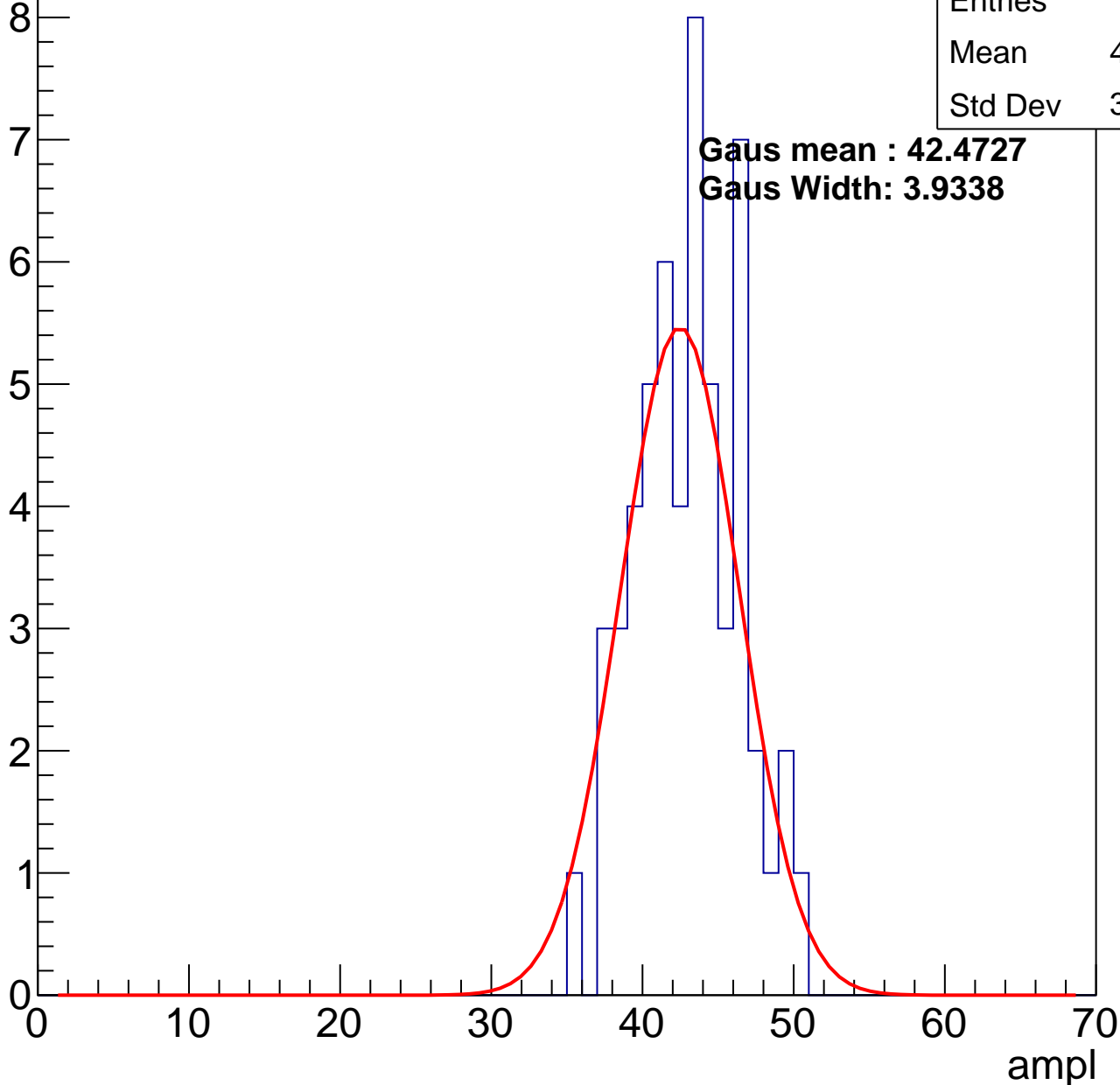
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	55
Mean	42.56
Std Dev	3.389

**Gaus mean : 42.4727**

**Gaus Width: 3.9338**

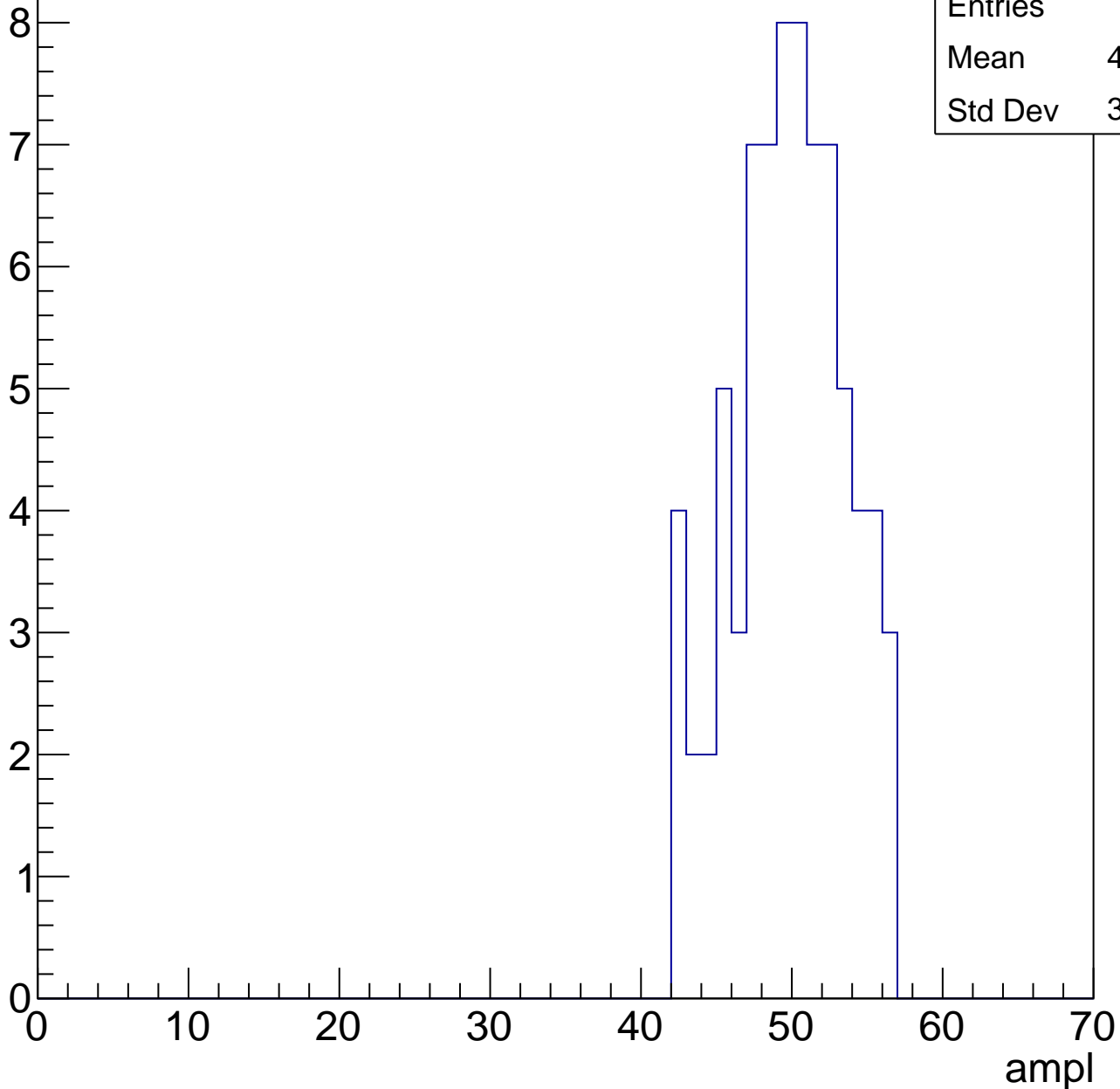


# B1L103S, U11-ch11, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	76
Mean	49.37
Std Dev	3.663

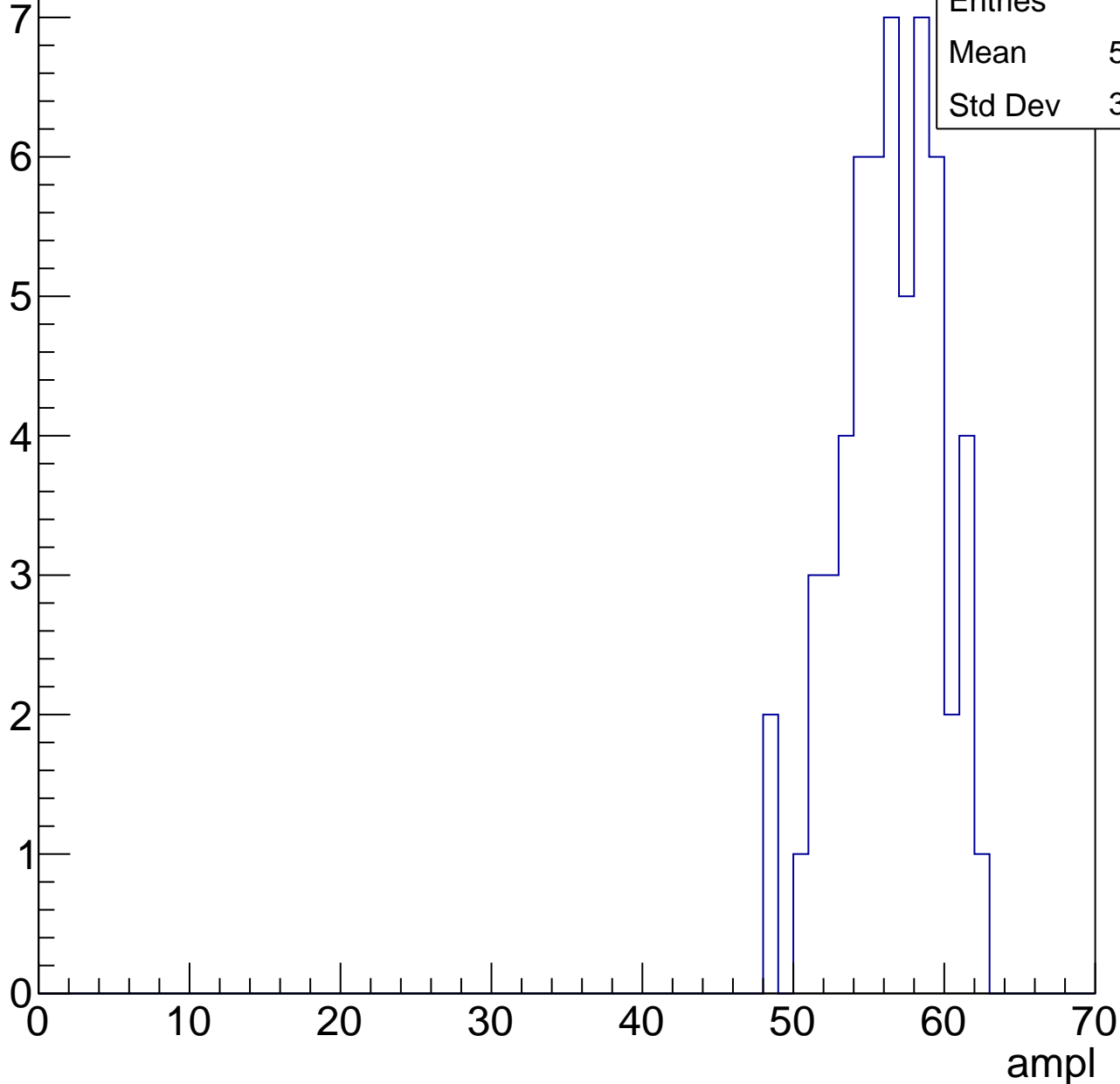


# B1L103S, U11-ch11, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	57
Mean	55.86
Std Dev	3.263

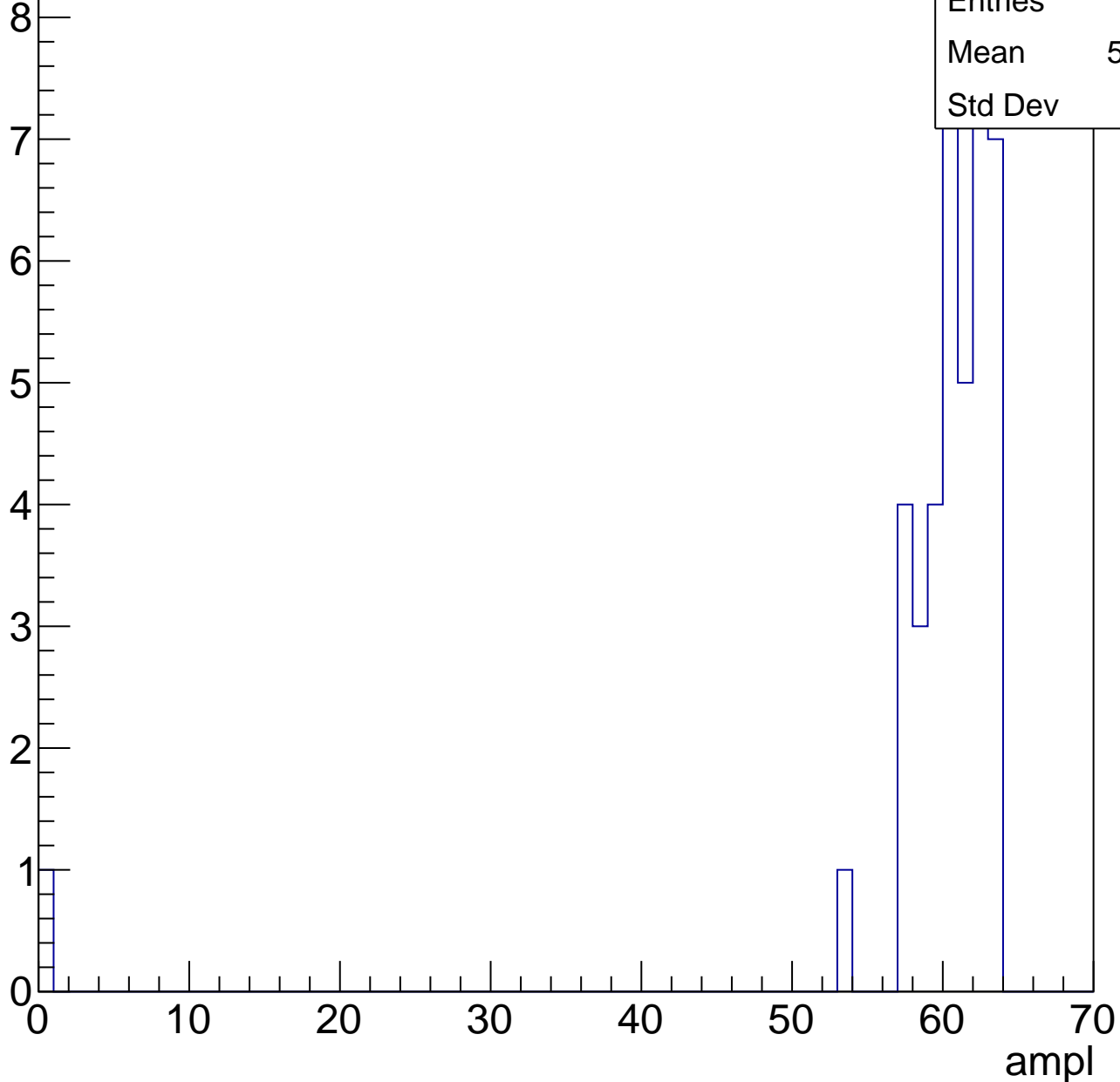


# B1L103S, U11-ch11, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

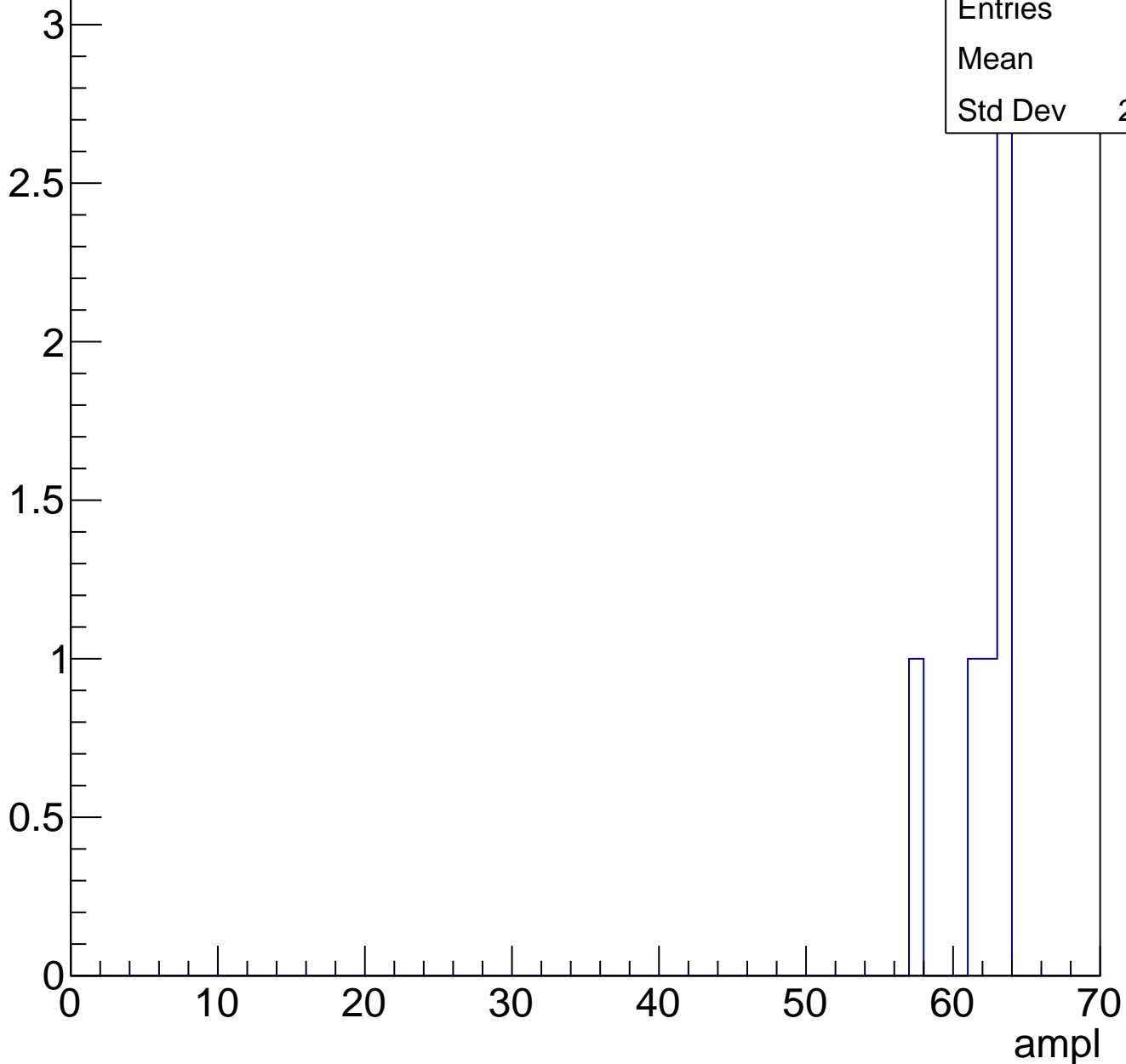
Entries	41
Mean	58.85
Std Dev	9.56



# B1L103S, U11-ch11, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U11-ch11, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L103S, U11-ch12, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	71
Mean	30.7
Std Dev	5.15

**Gaus mean : 31.7461**

**Gaus Width: 3.4664**

Entry

10  
8  
6  
4  
2  
0

ampl

0

10

20

30

40

50

60

70

# B1L103S, U11-ch12, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	70
Mean	38.23
Std Dev	3.921

**Gaus mean : 38.3741**

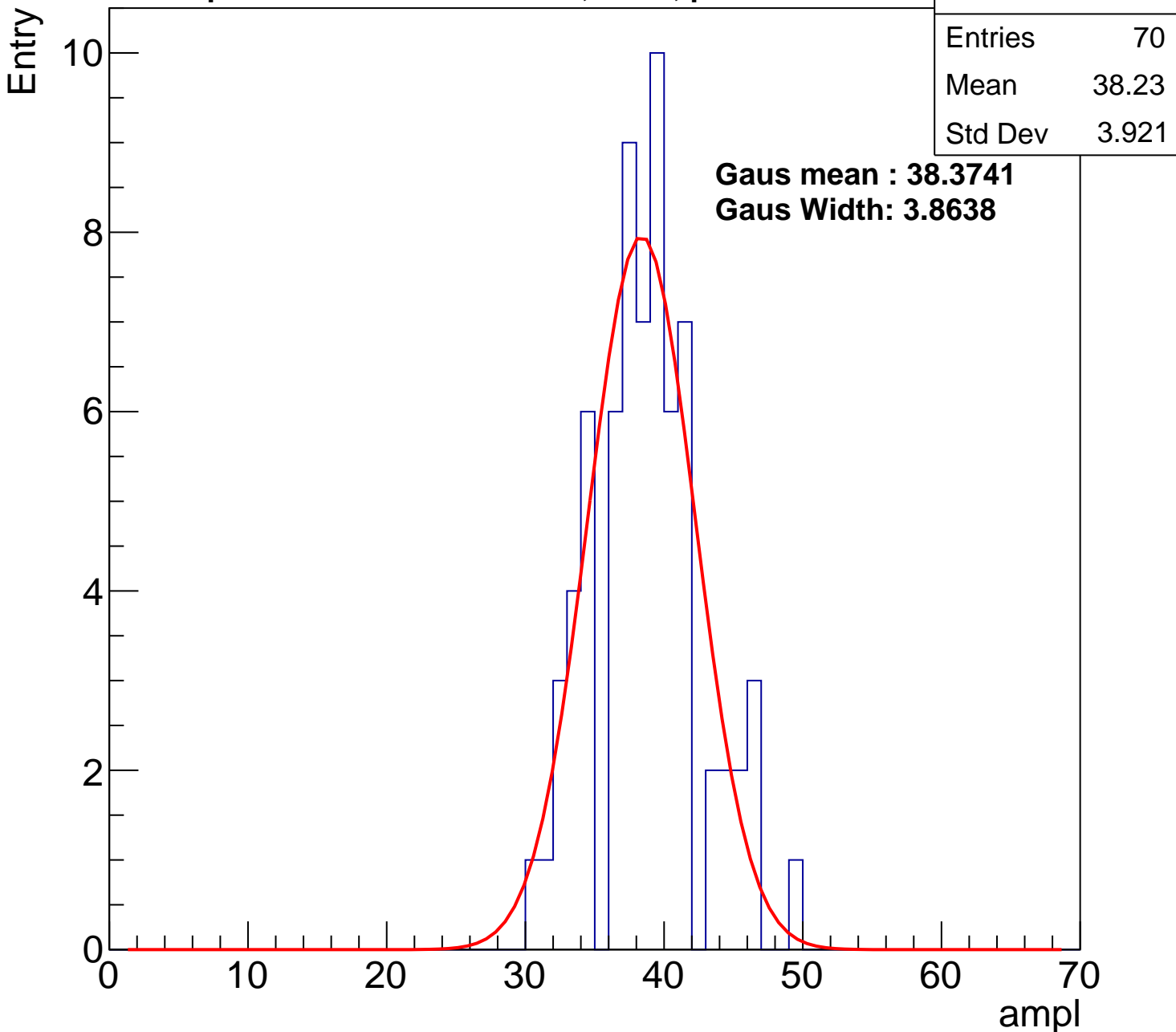
**Gaus Width: 3.8638**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U11-ch12, adc2

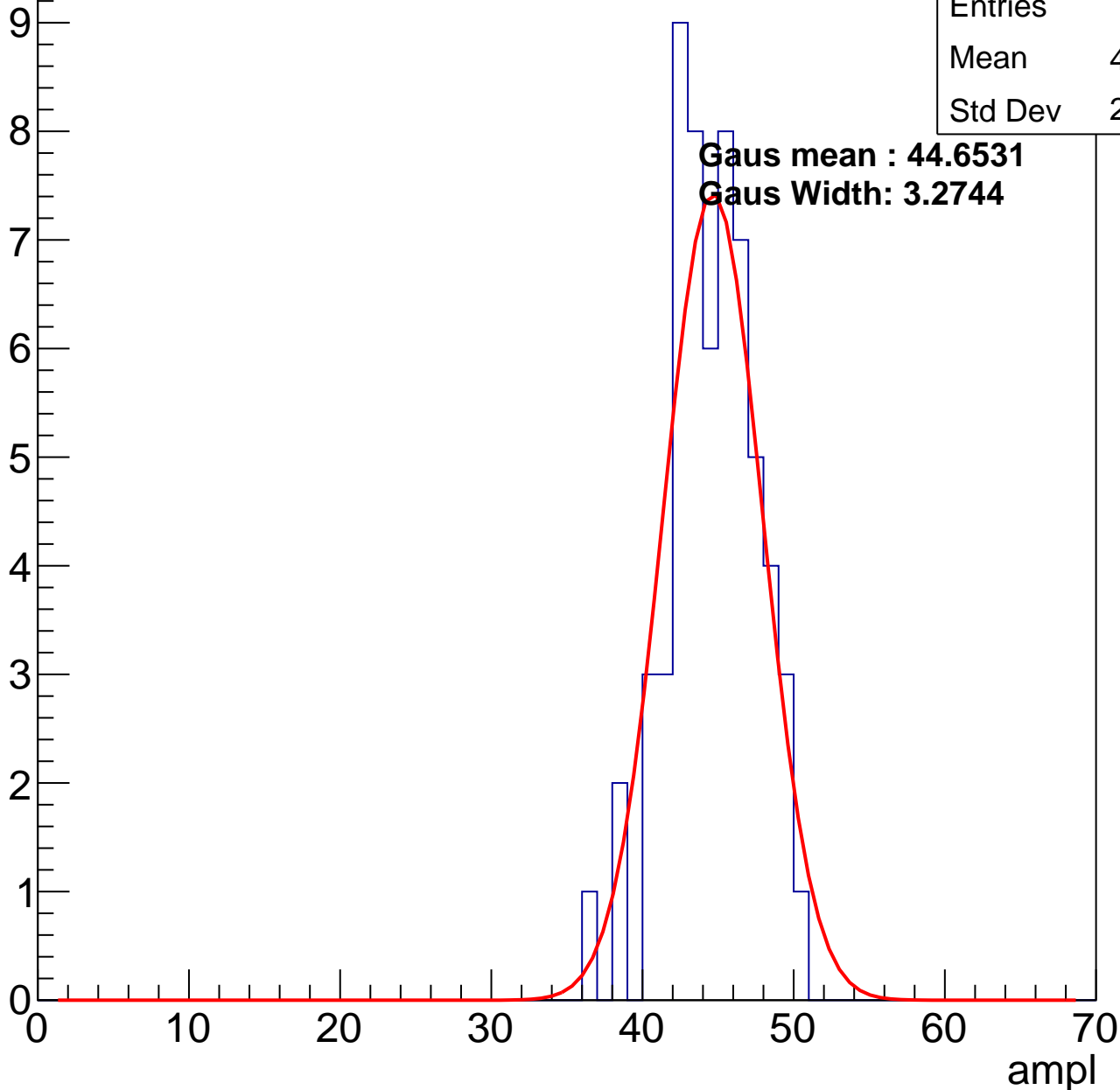
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	60
Mean	44.12
Std Dev	2.916

**Gaus mean : 44.6531**

**Gaus Width: 3.2744**

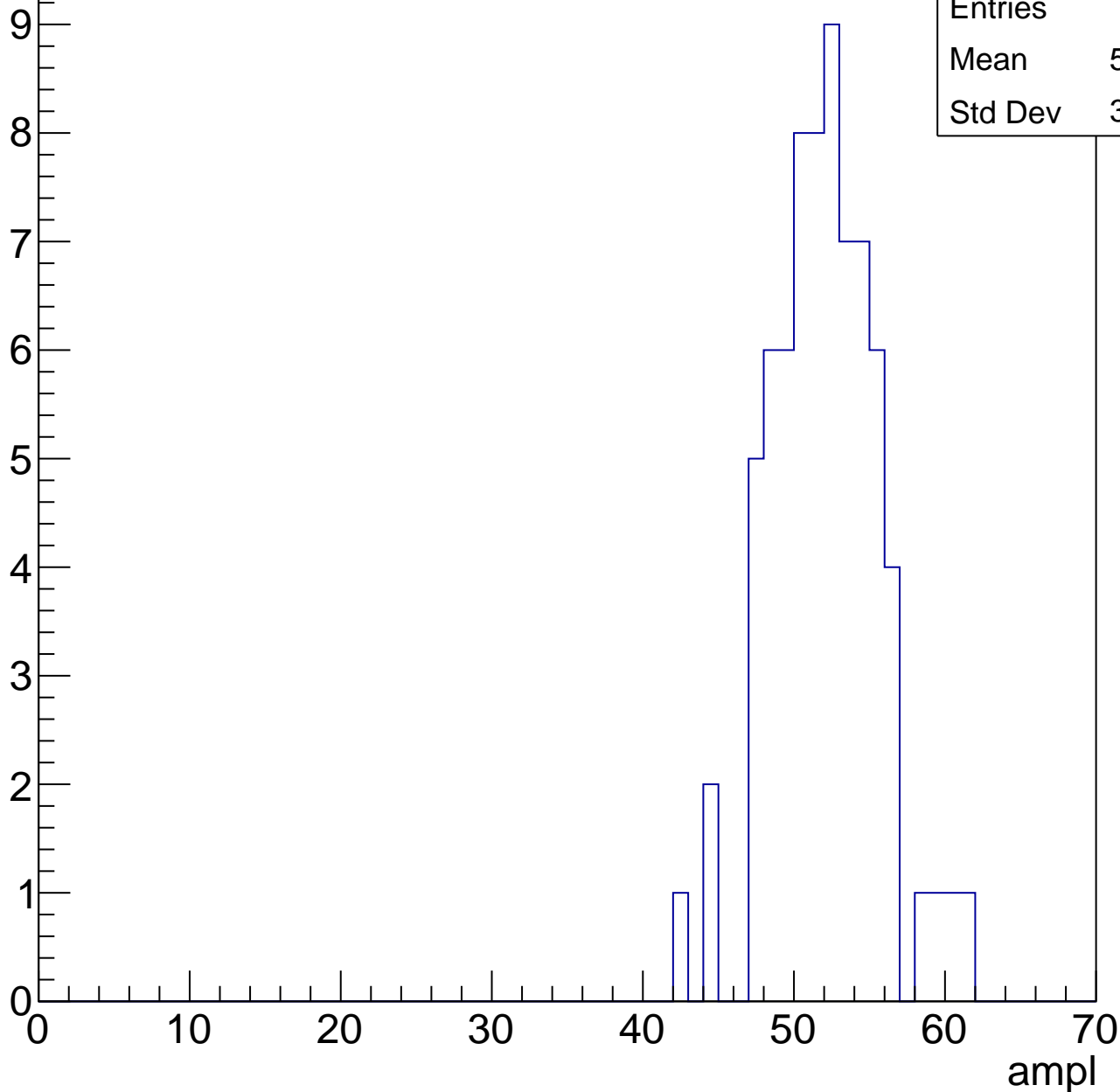


# B1L103S, U11-ch12, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	73
Mean	51.56
Std Dev	3.535

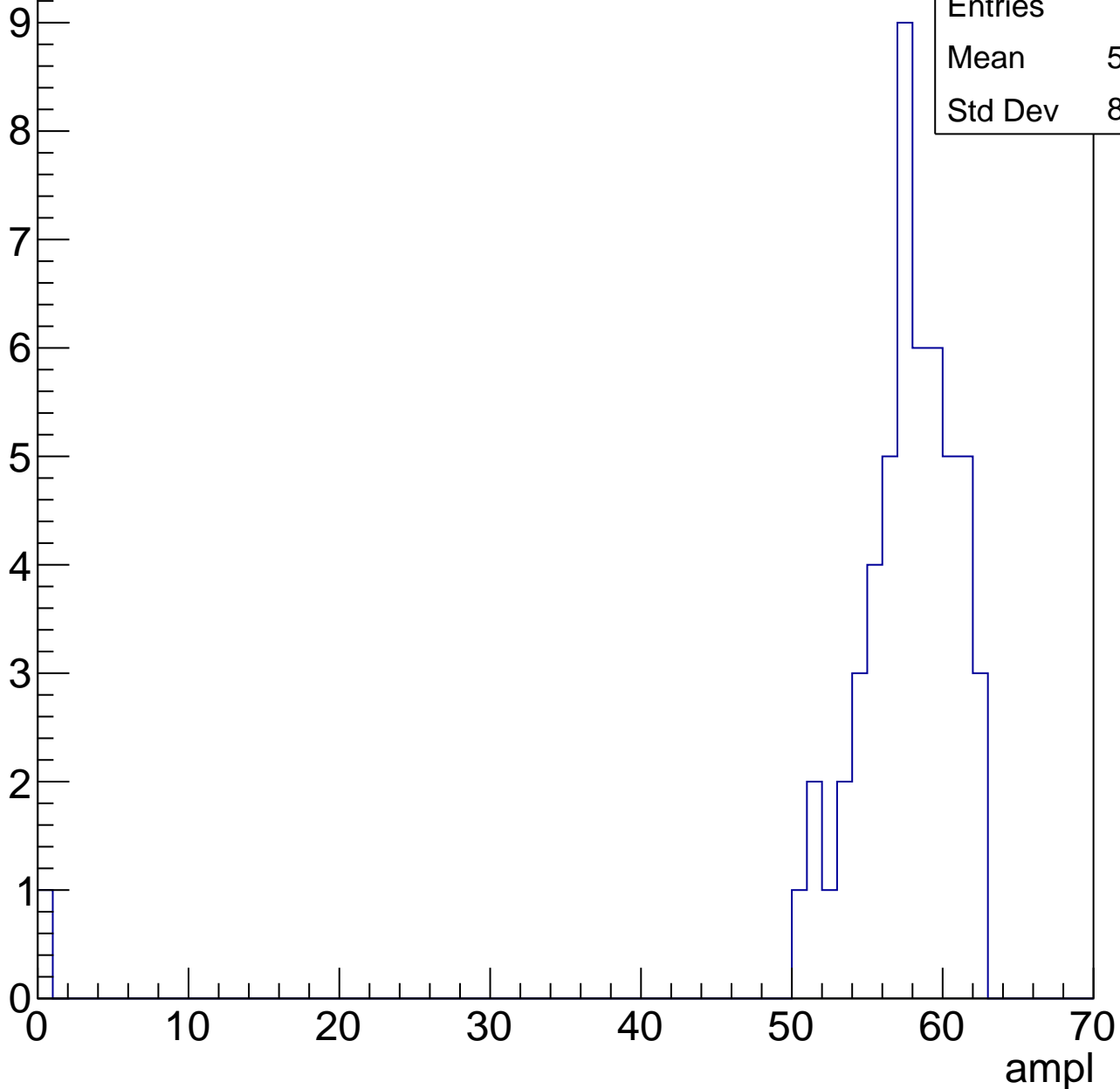


# B1L103S, U11-ch12, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	53
Mean	56.19
Std Dev	8.322

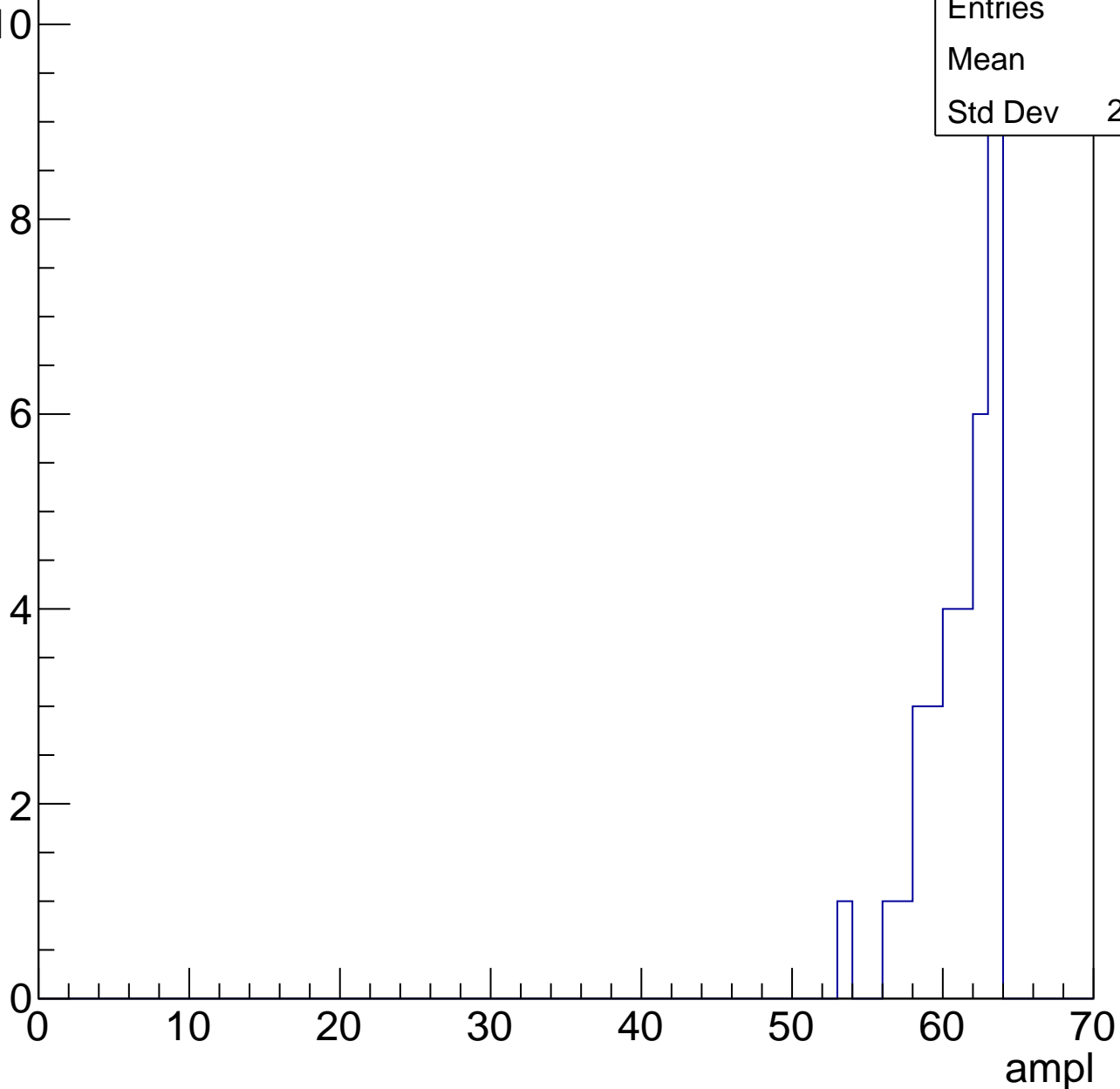


# B1L103S, U11-ch12, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	33
Mean	60.7
Std Dev	2.406



# B1L103S, U11-ch12, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	62
Std Dev	0



# B1L103S, U11-ch12, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U11-ch13, adc0

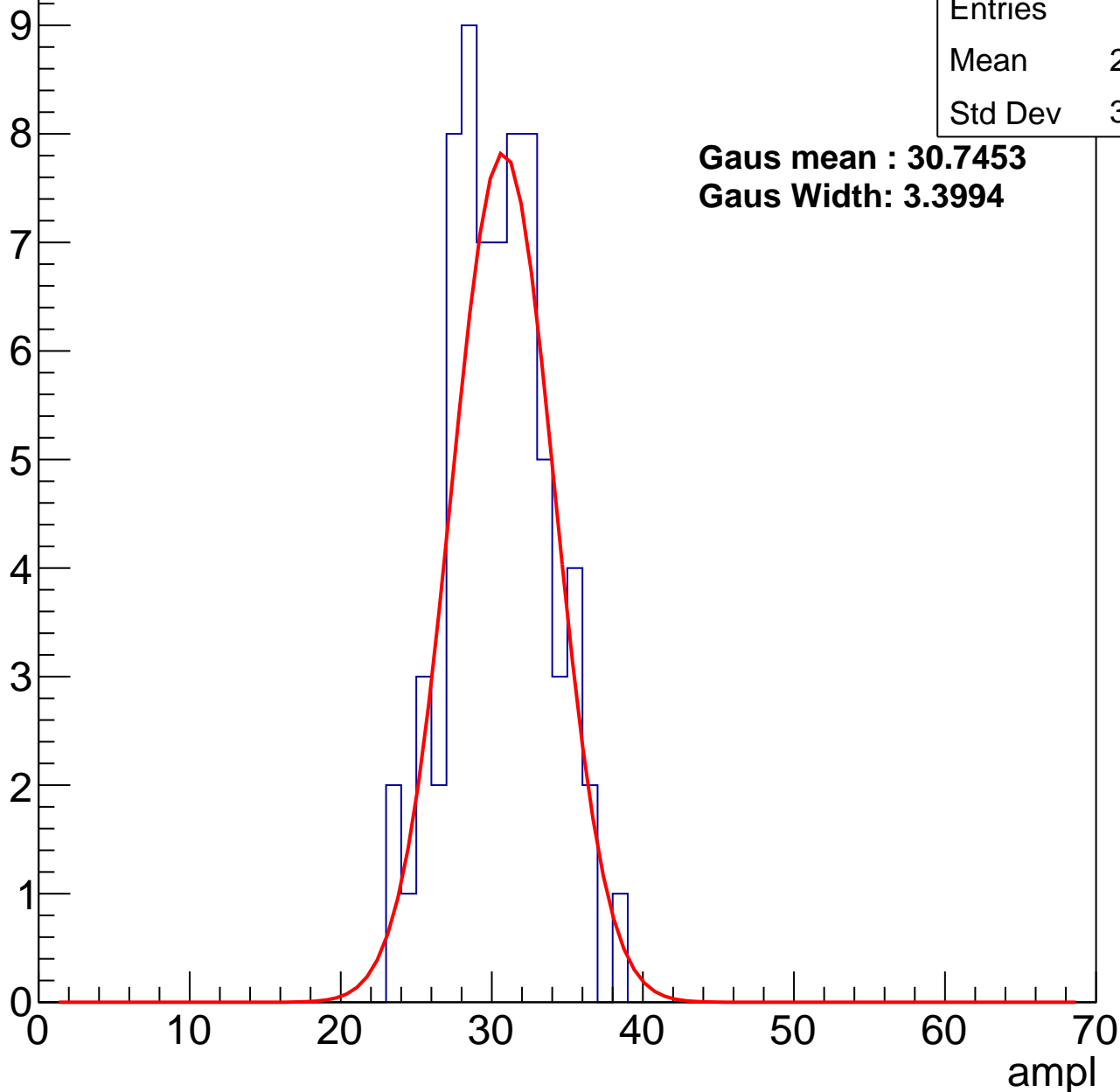
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	70
Mean	29.99
Std Dev	3.218

**Gaus mean : 30.7453**

**Gaus Width: 3.3994**



# B1L103S, U11-ch13, adc1

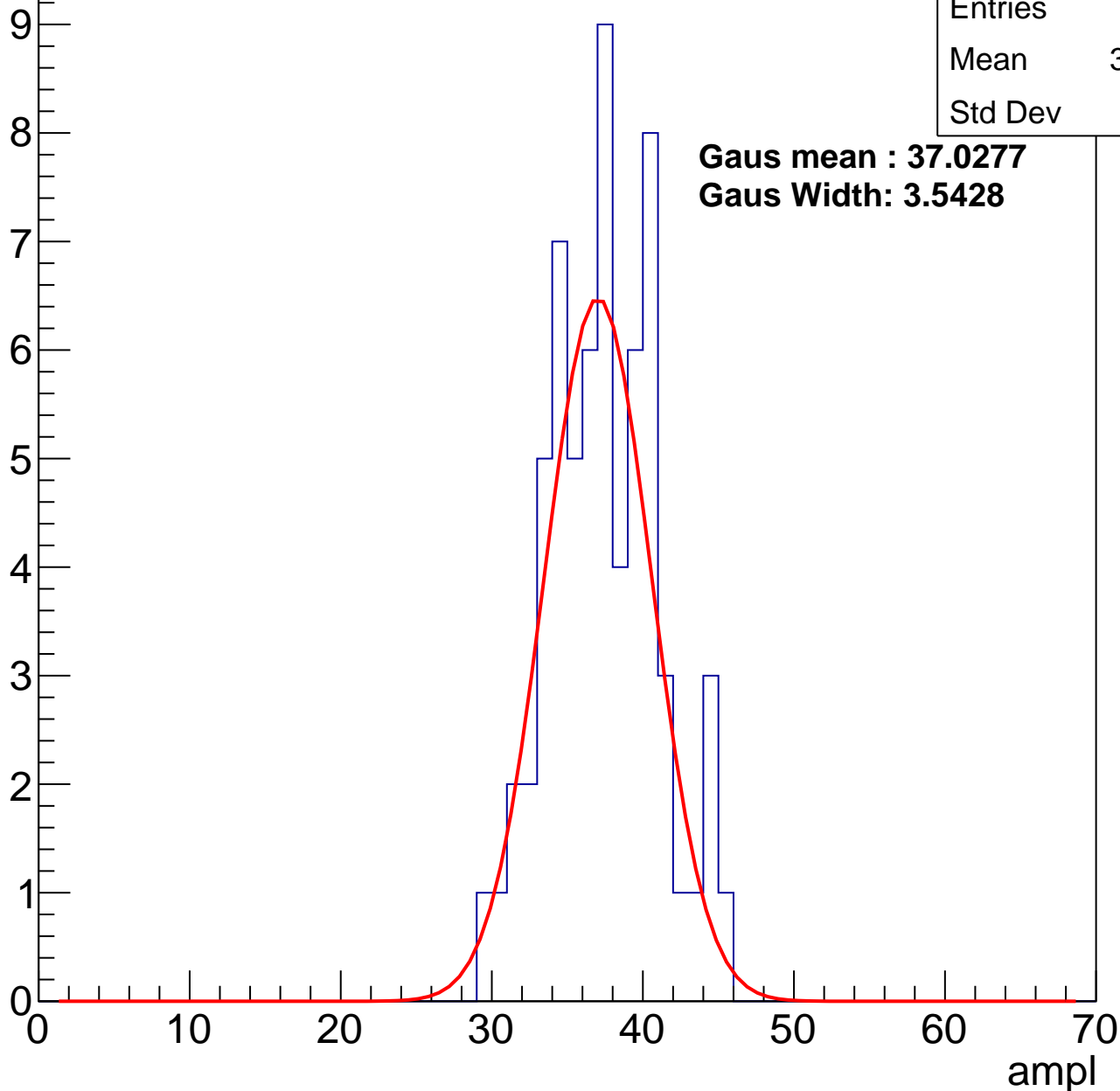
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	36.97
Std Dev	3.56

**Gaus mean : 37.0277**

**Gaus Width: 3.5428**



# B1L103S, U11-ch13, adc2

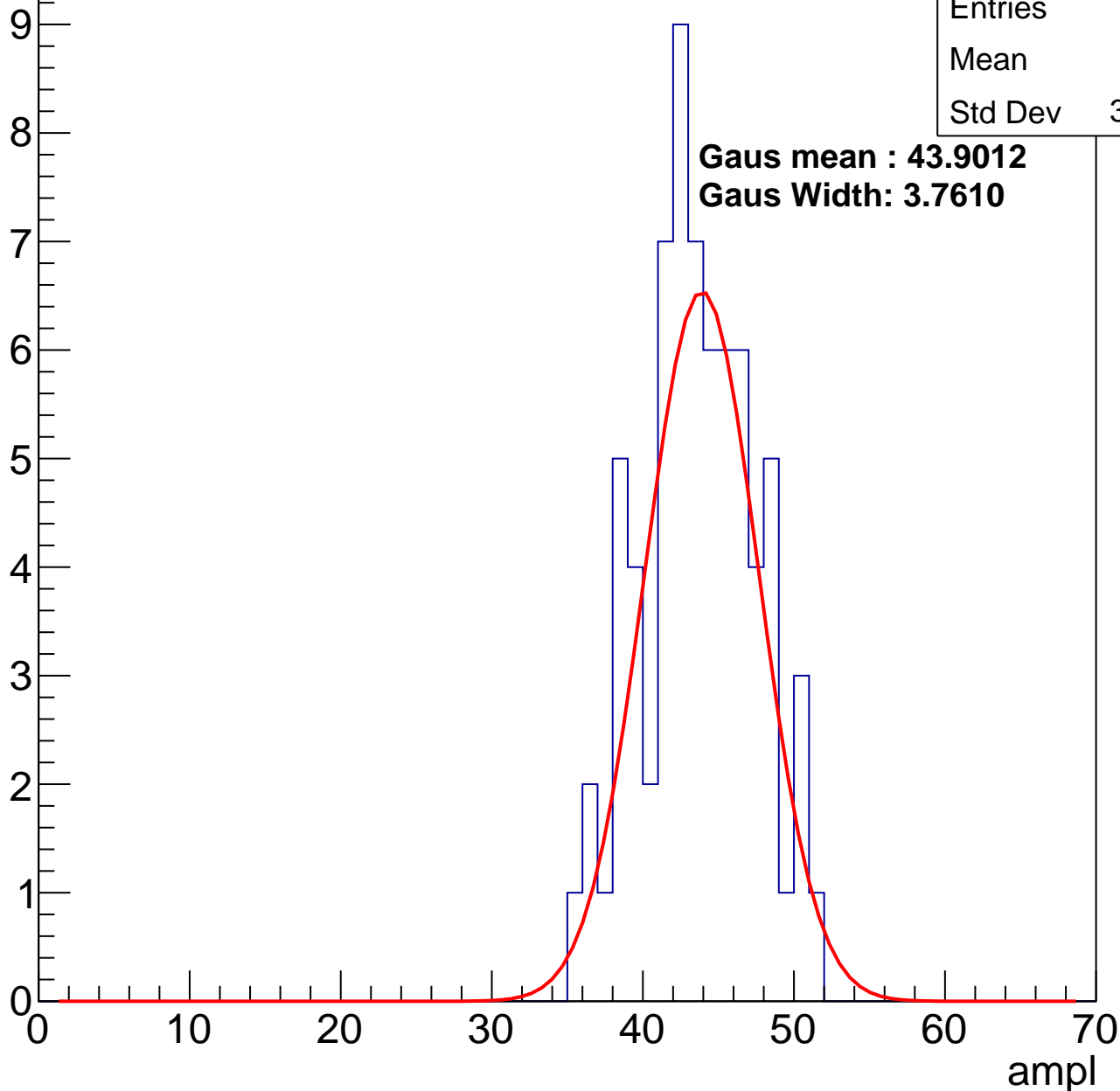
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	70
Mean	43.2
Std Dev	3.702

**Gaus mean : 43.9012**

**Gaus Width: 3.7610**

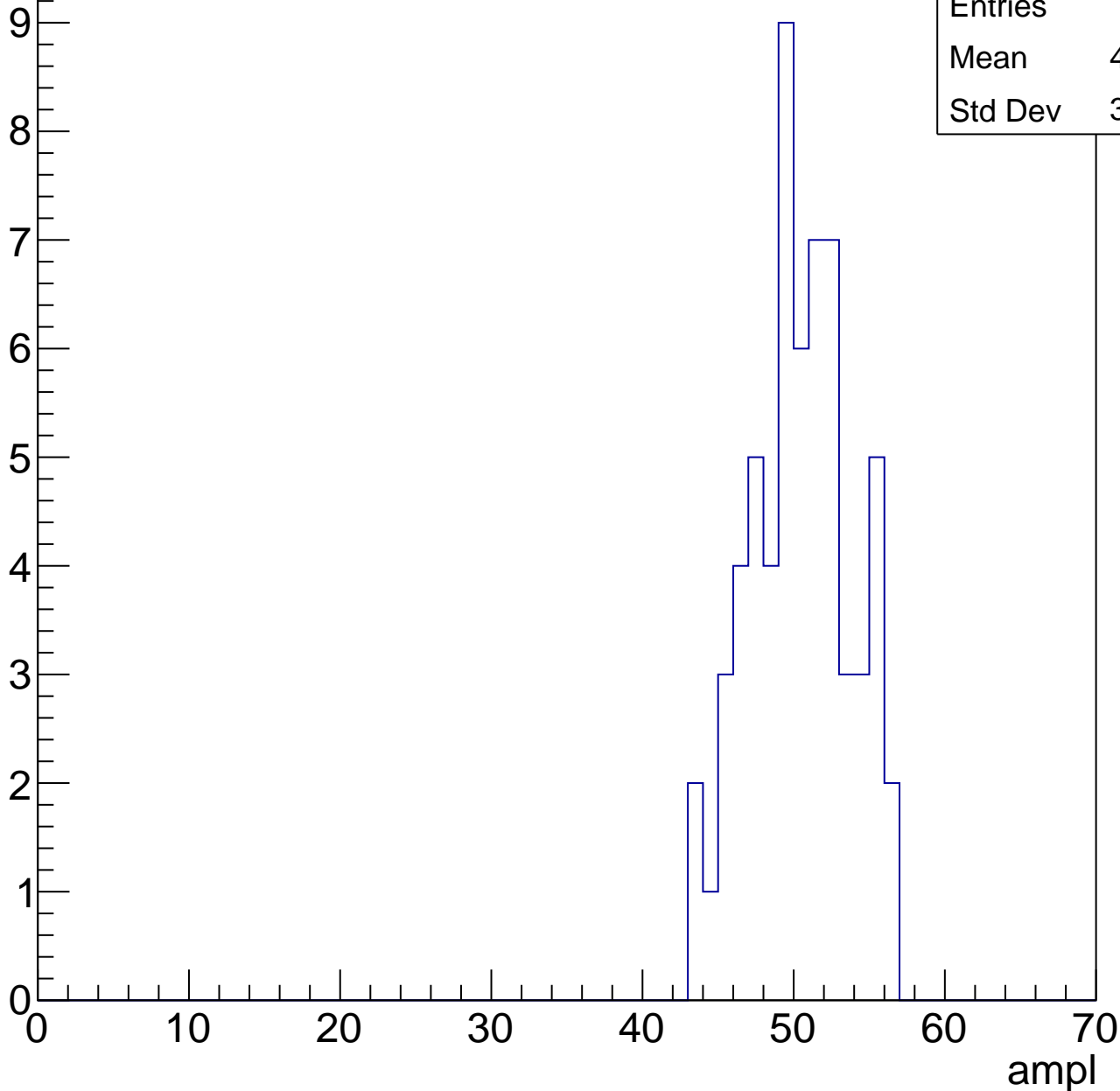


# B1L103S, U11-ch13, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	61
Mean	49.93
Std Dev	3.264

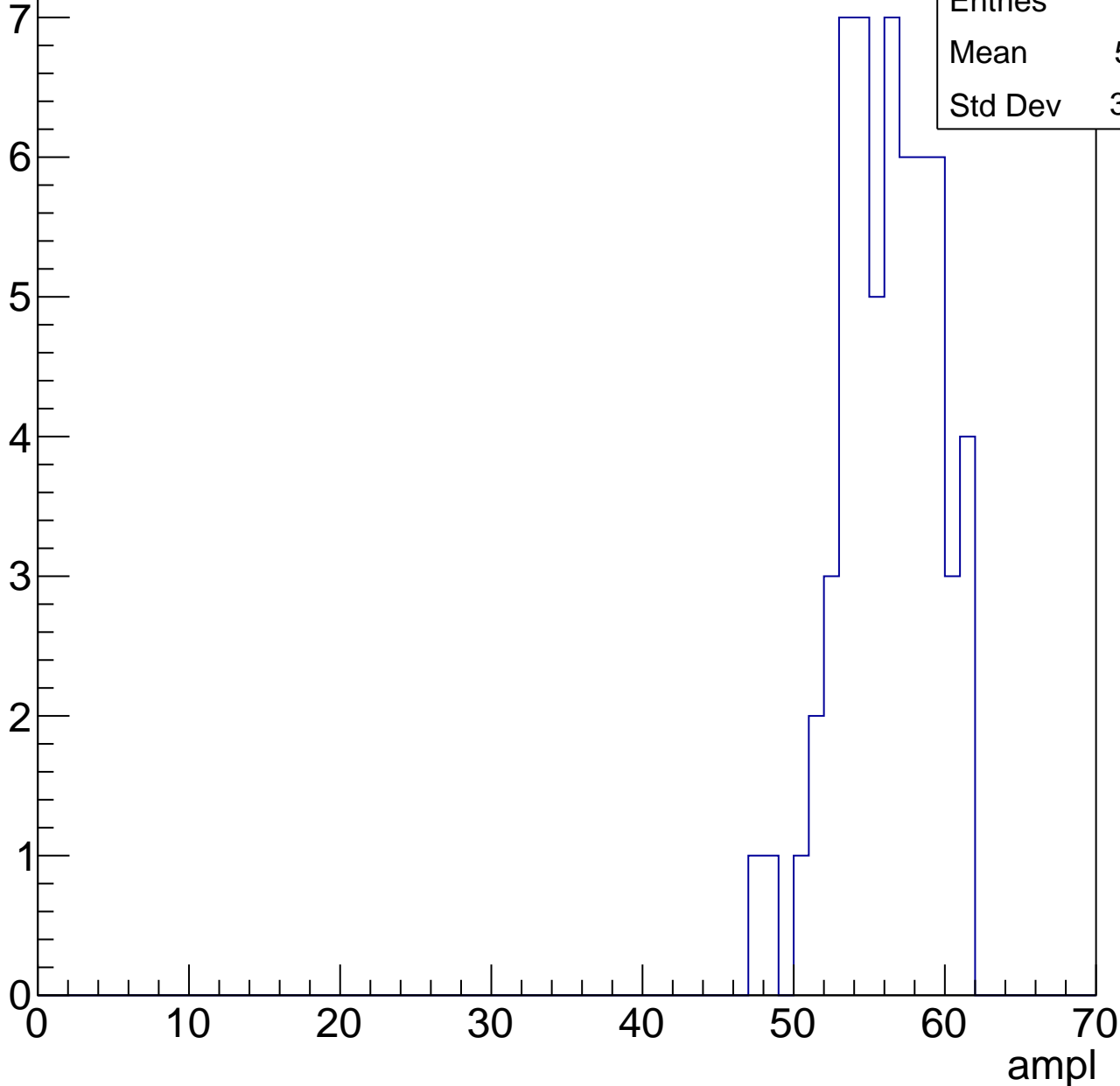


# B1L103S, U11-ch13, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	59
Mean	55.71
Std Dev	3.195

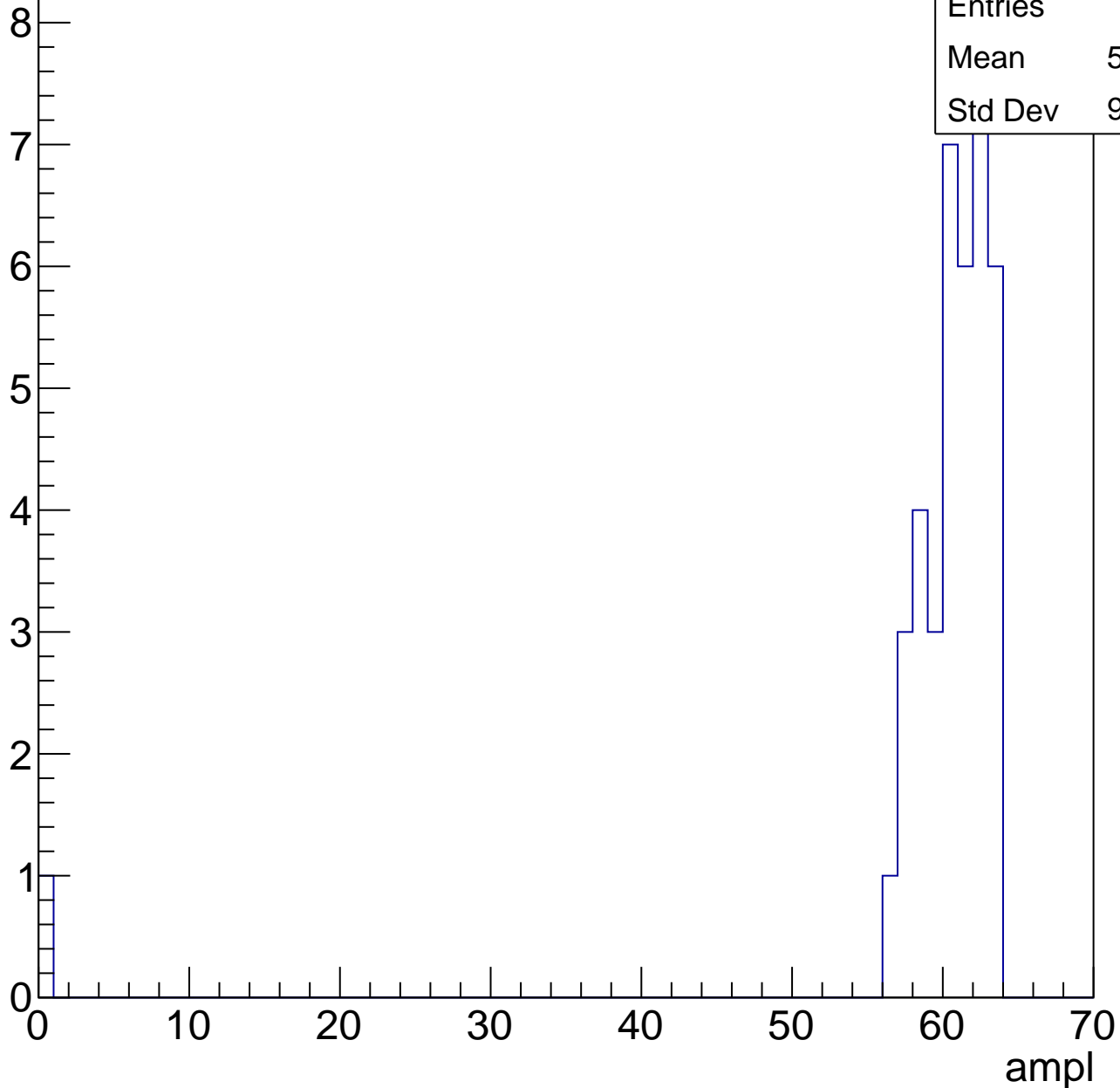


# B1L103S, U11-ch13, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

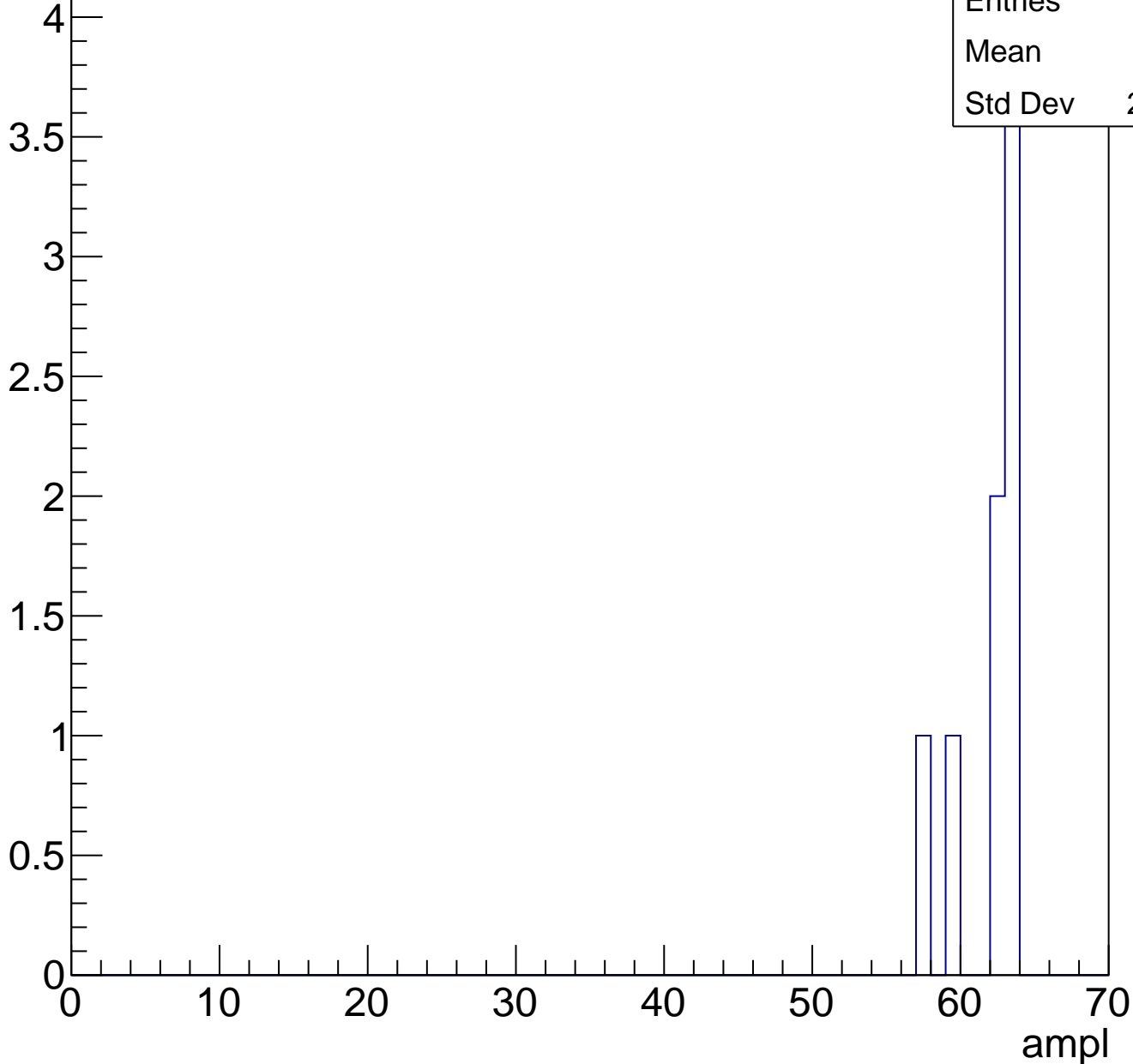
Entries	39
Mean	58.87
Std Dev	9.746



# B1L103S, U11-ch13, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U11-ch13, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L103S, U11-ch14, adc0

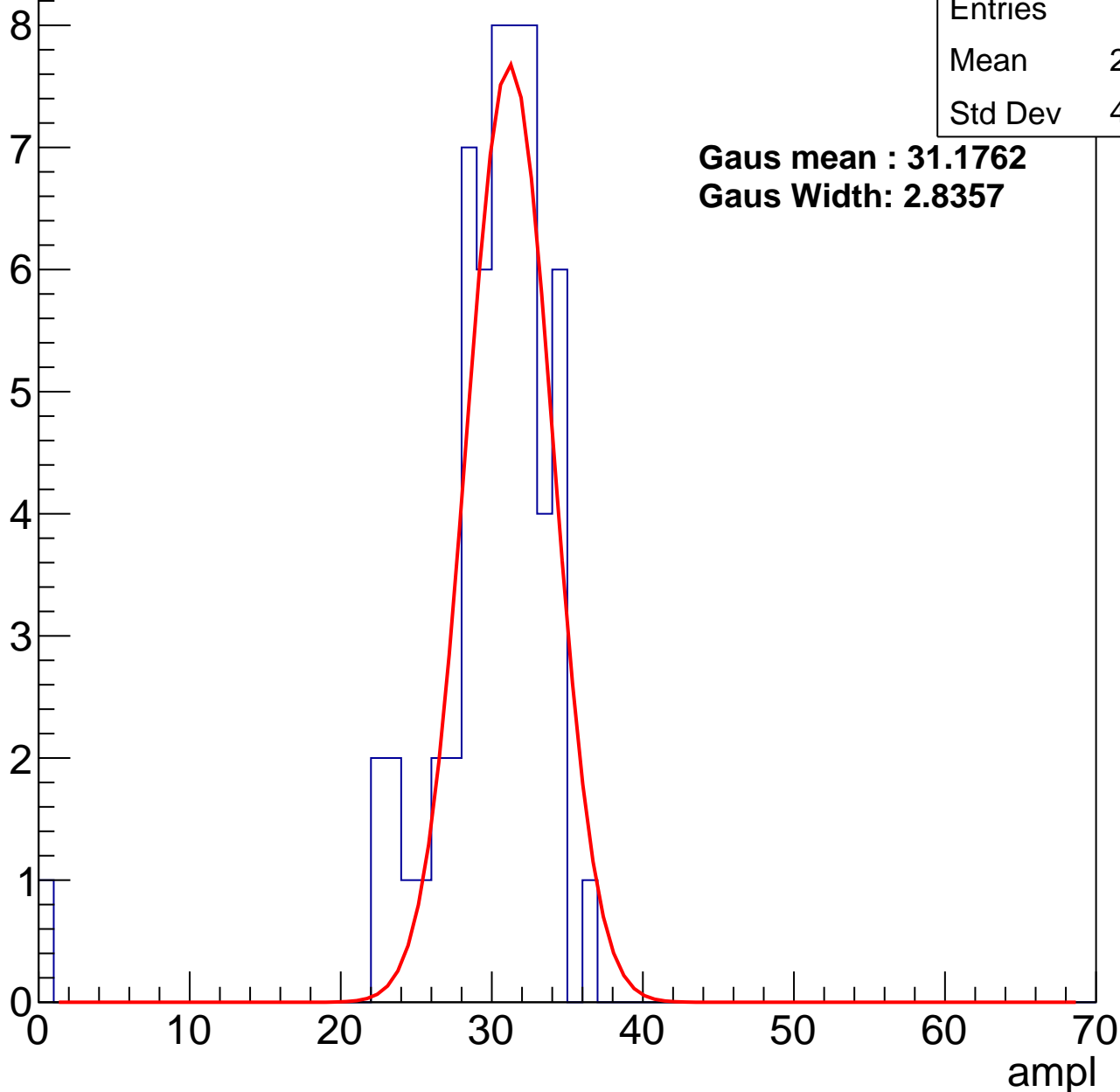
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	59
Mean	29.34
Std Dev	4.963

**Gaus mean : 31.1762**

**Gaus Width: 2.8357**



# B1L103S, U11-ch14, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	62
Mean	36.32
Std Dev	3.509

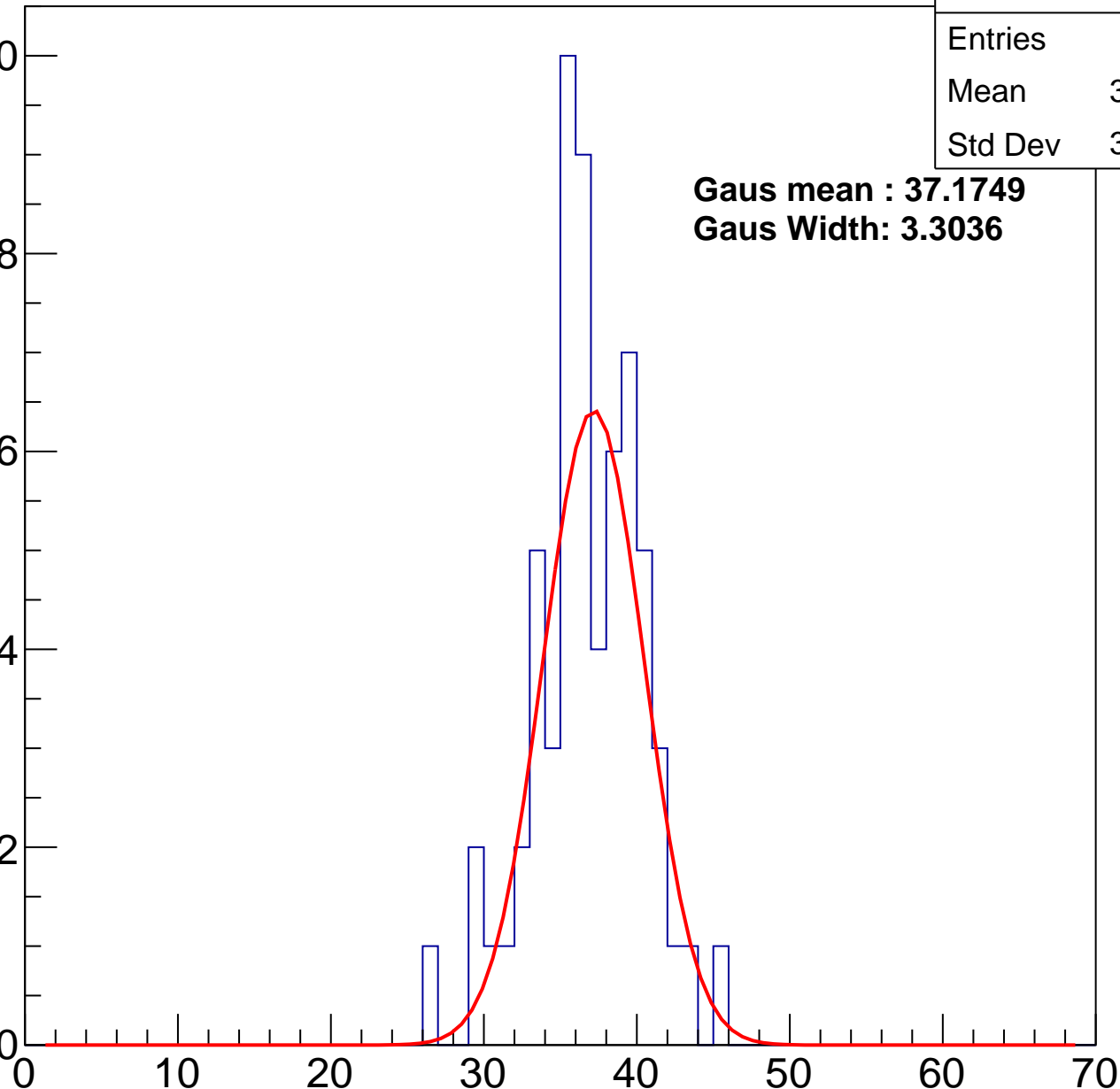
**Gaus mean : 37.1749**

**Gaus Width: 3.3036**

Entry

10  
8  
6  
4  
2  
0

ampl



# B1L103S, U11-ch14, adc2

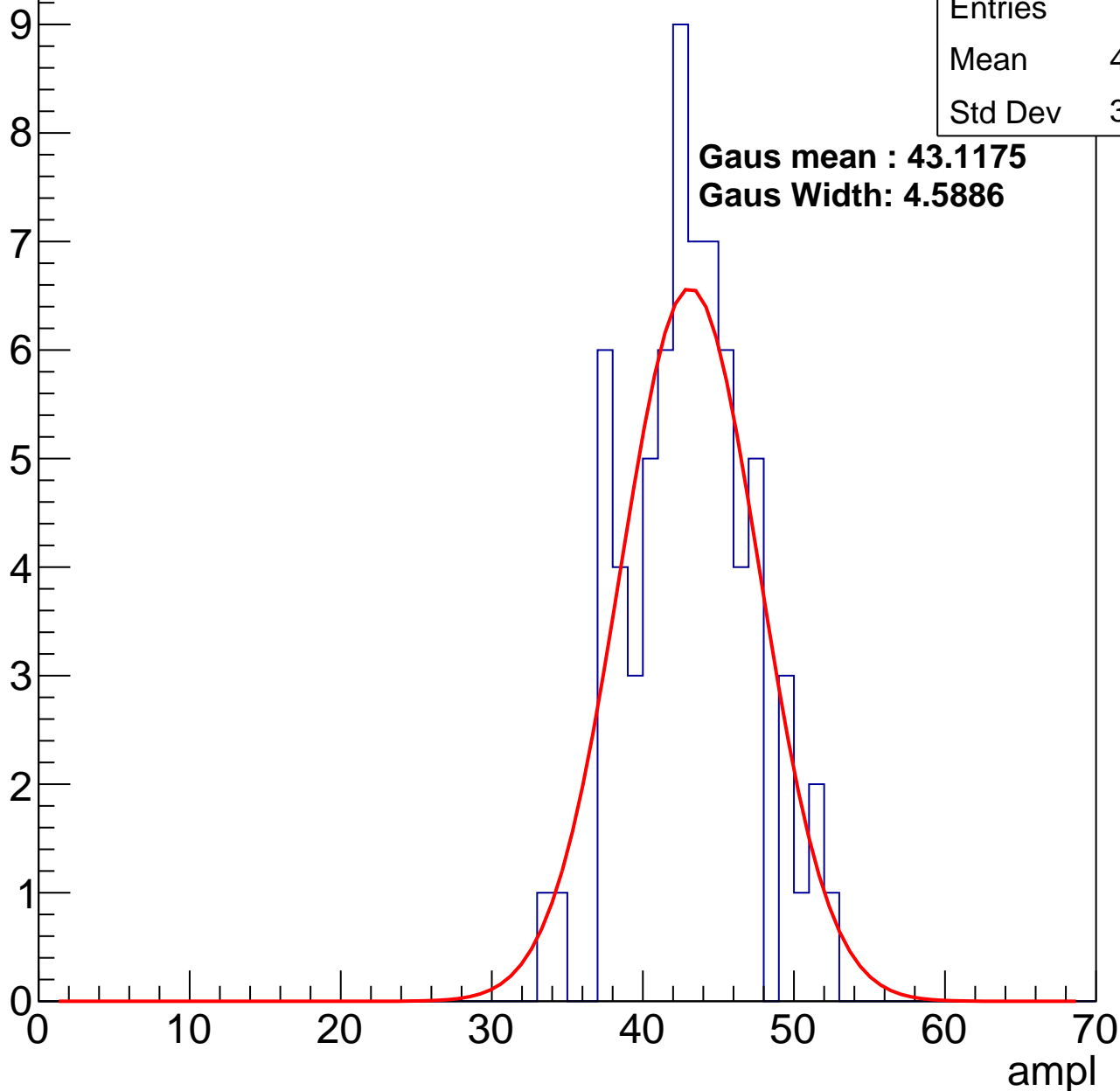
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	71
Mean	42.69
Std Dev	3.988

**Gaus mean : 43.1175**

**Gaus Width: 4.5886**

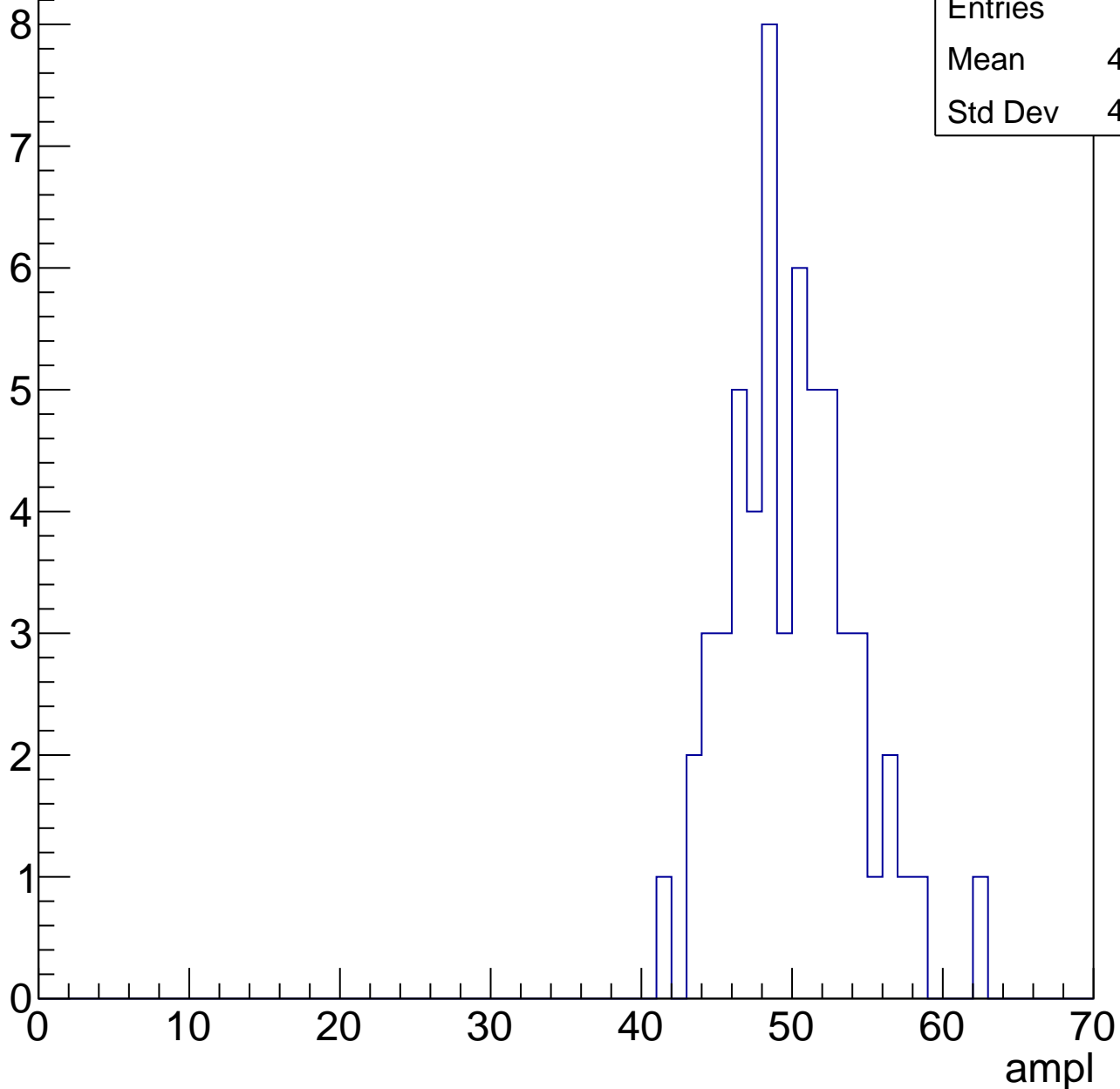


# B1L103S, U11-ch14, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	57
Mean	49.53
Std Dev	4.092

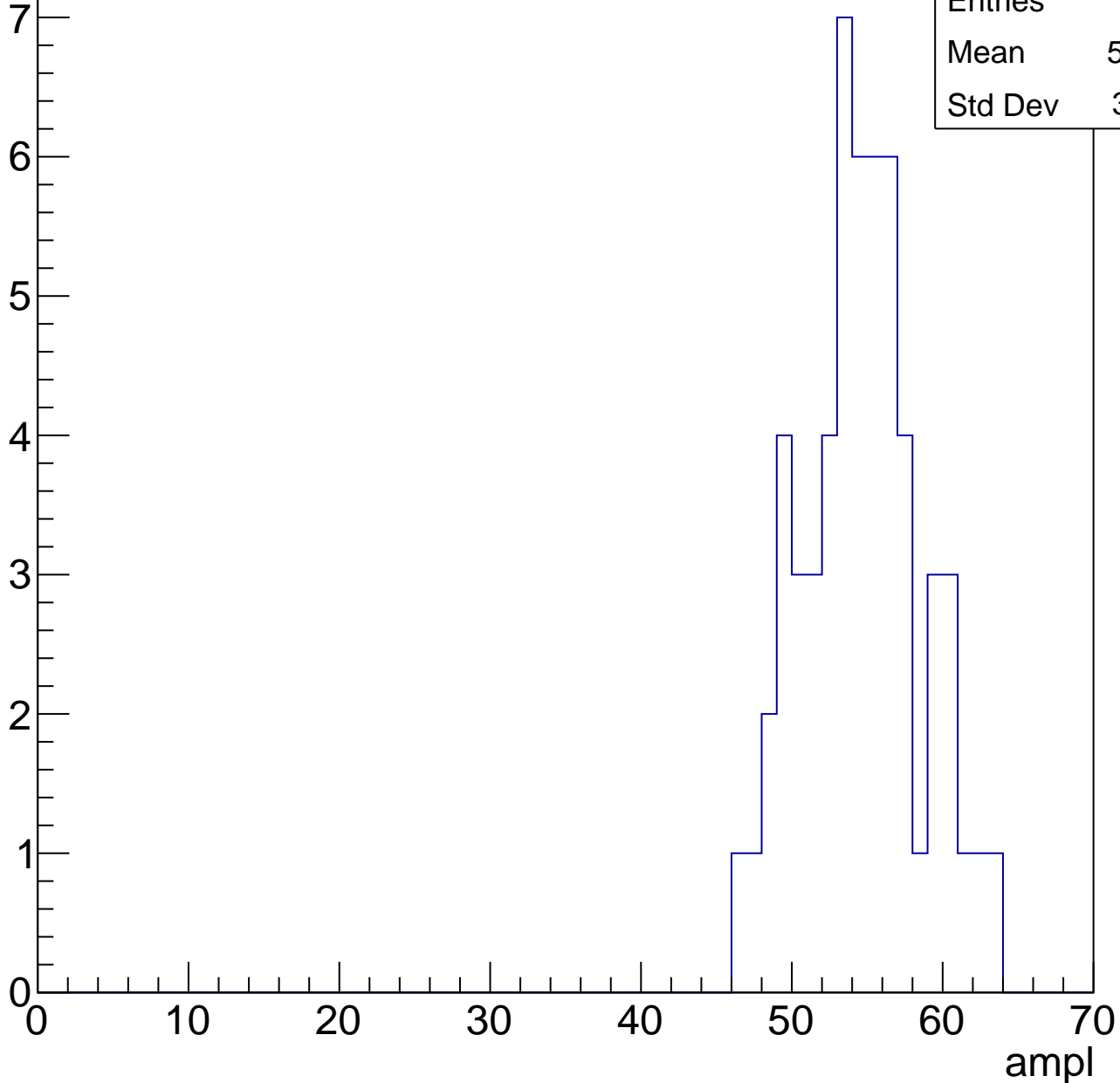


# B1L103S, U11-ch14, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

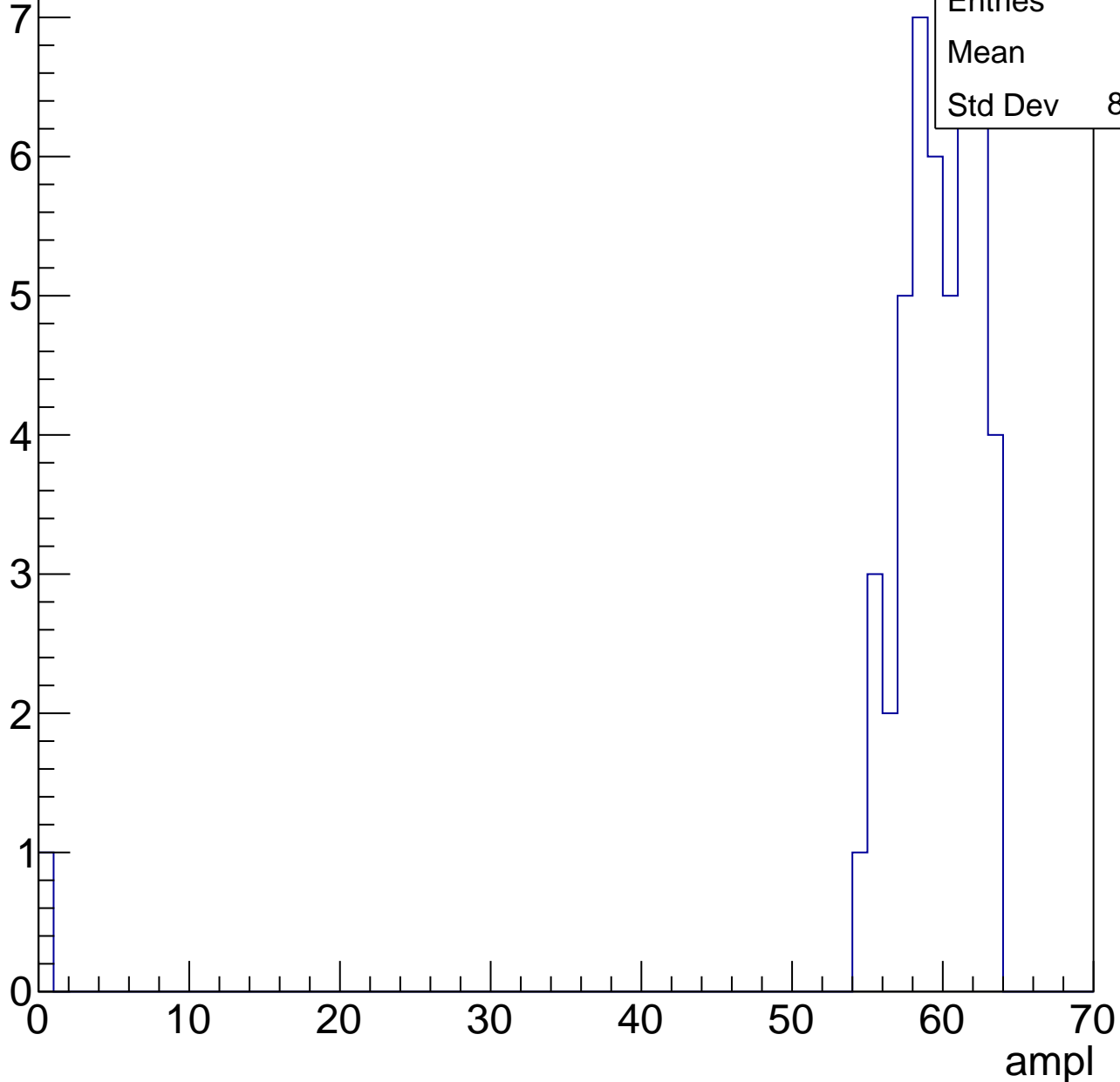
Entries	57
Mean	54.14
Std Dev	3.841



# B1L103S, U11-ch14, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

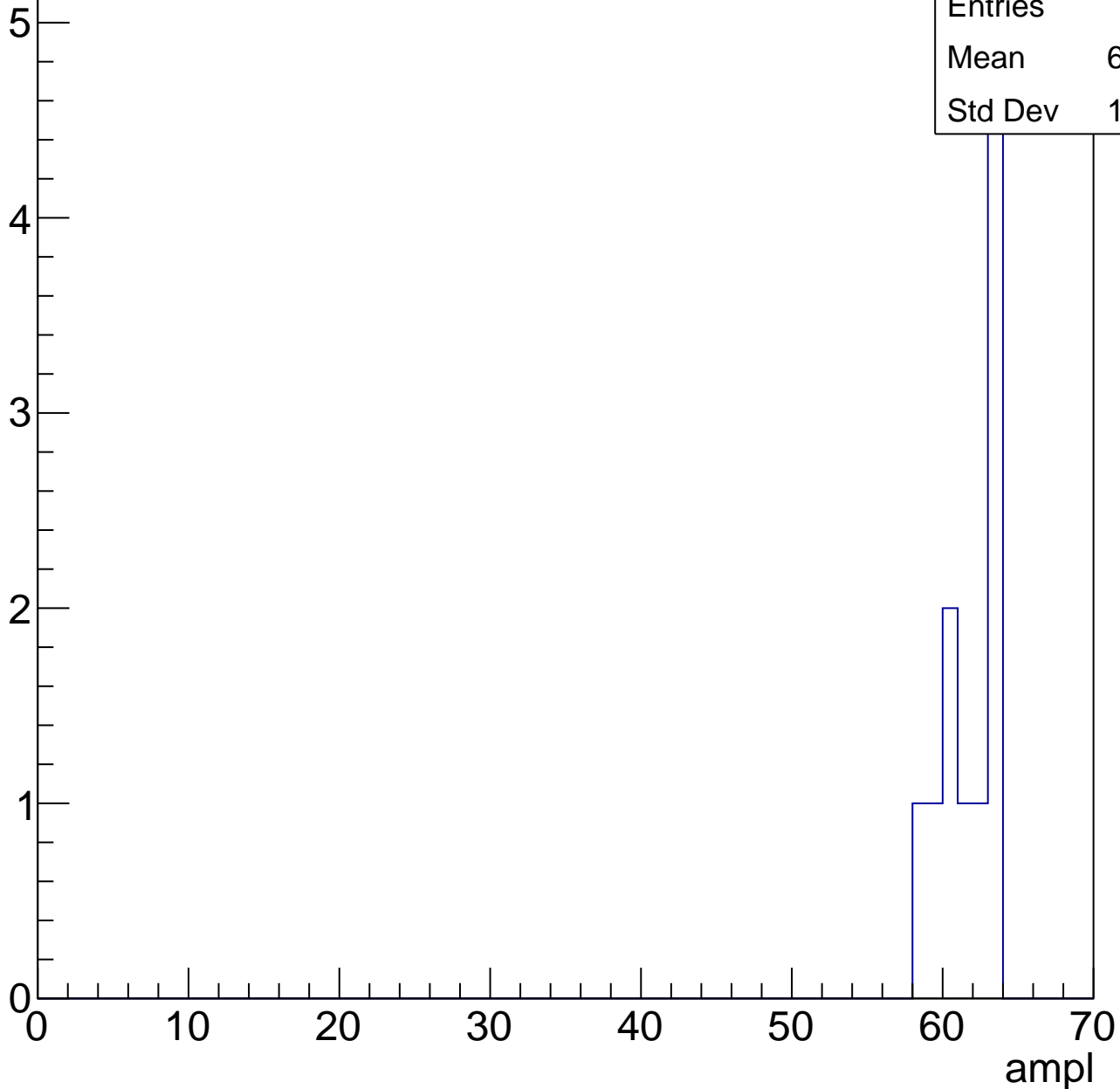


# B1L103S, U11-ch14, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	11
Mean	61.36
Std Dev	1.772





# B1L103S, U11-ch14, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U11-ch15, adc0

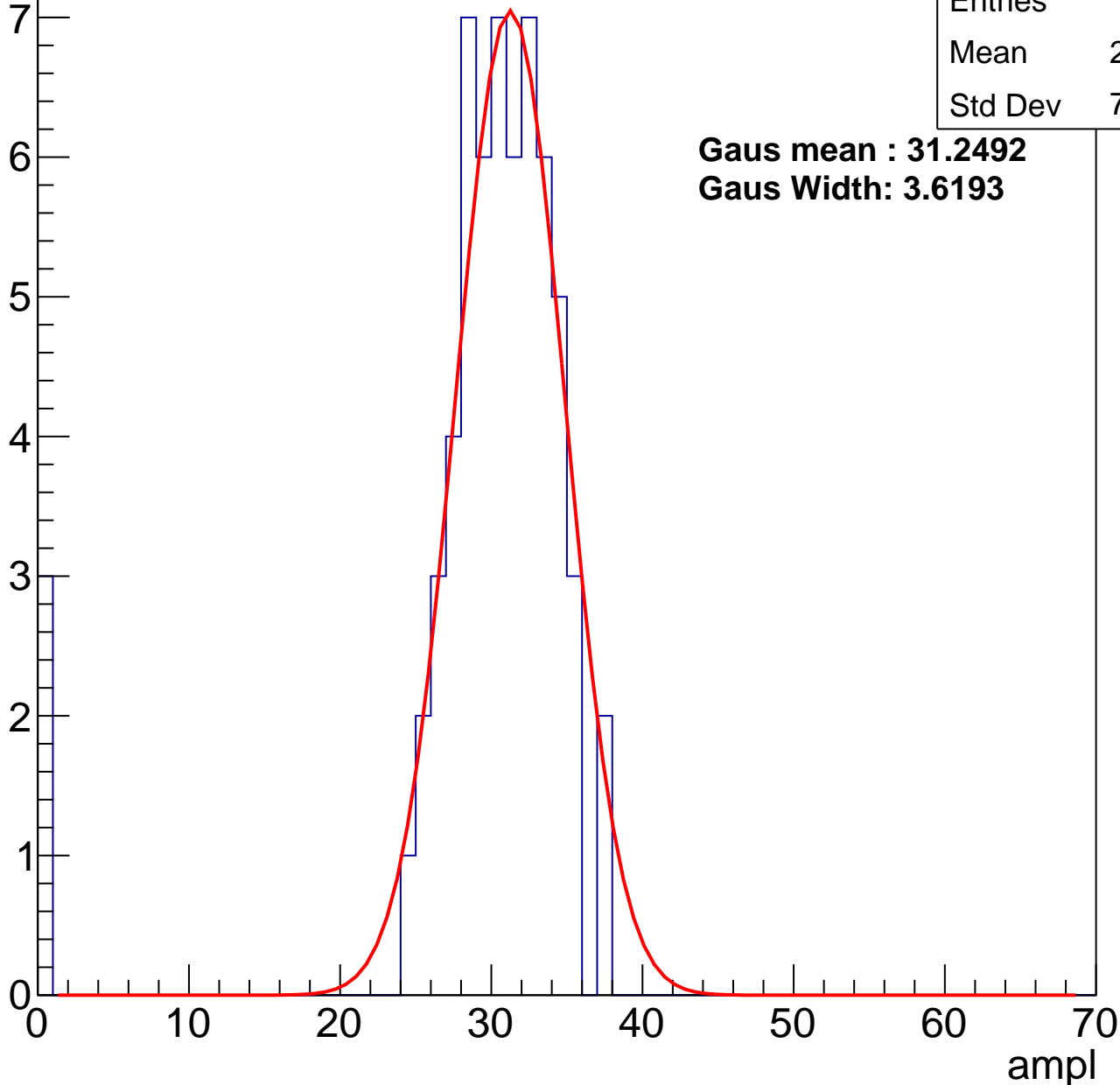
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	28.98
Std Dev	7.163

**Gaus mean : 31.2492**

**Gaus Width: 3.6193**



# B1L103S, U11-ch15, adc1

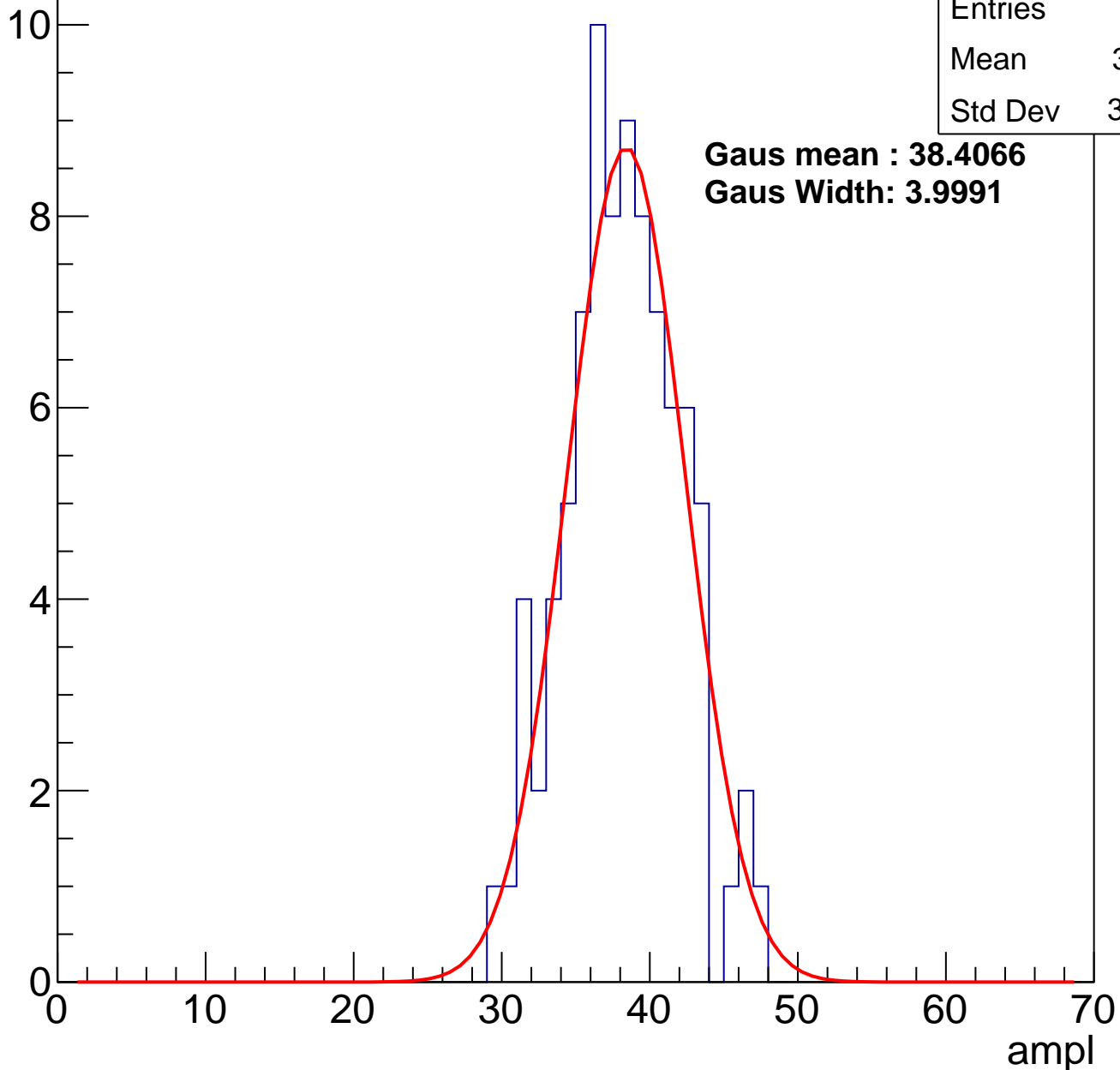
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	87
Mean	37.71
Std Dev	3.814

**Gaus mean : 38.4066**

**Gaus Width: 3.9991**

Entry



# B1L103S, U11-ch15, adc2

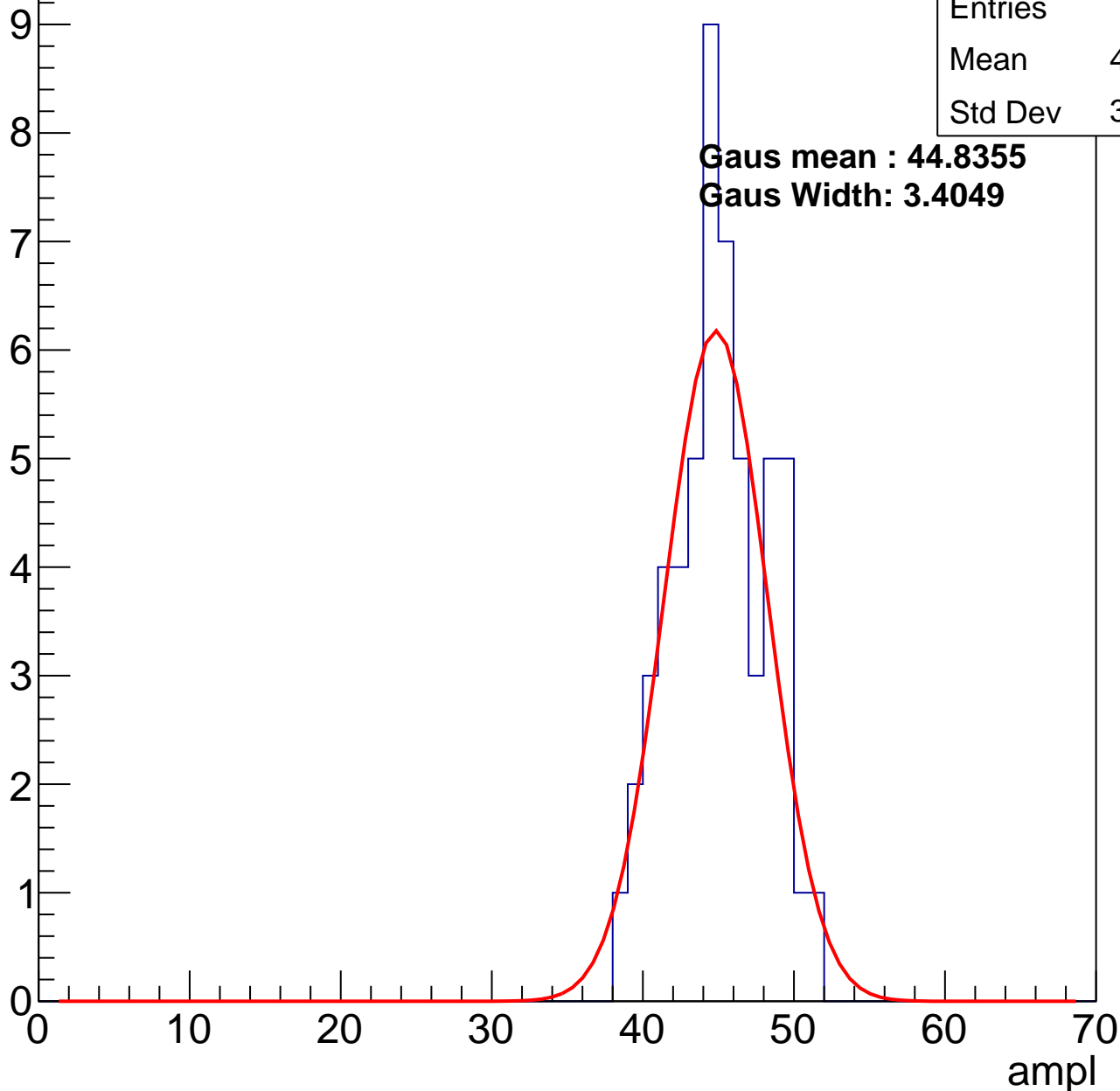
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	55
Mean	44.56
Std Dev	3.068

**Gaus mean : 44.8355**

**Gaus Width: 3.4049**

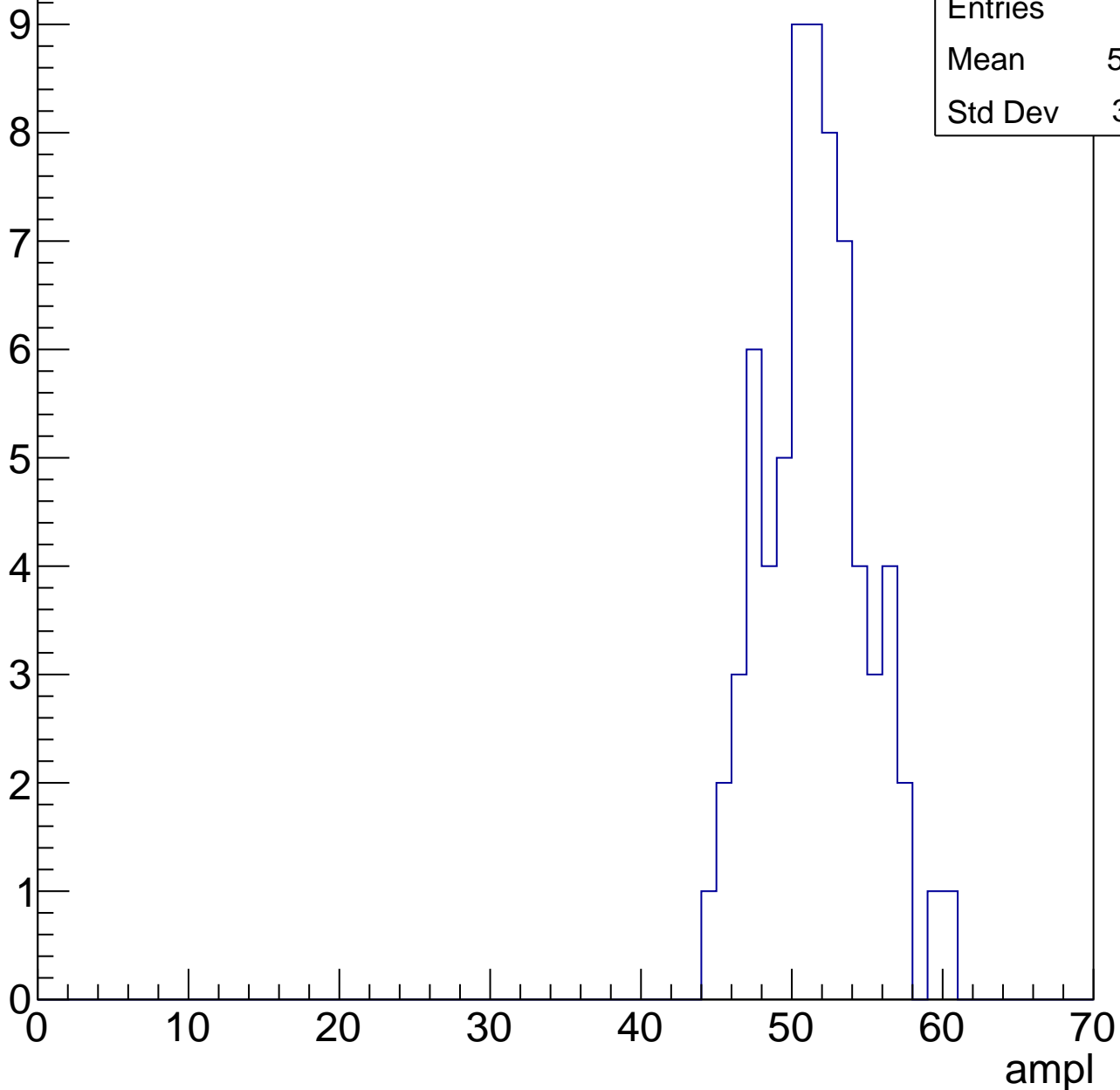


# B1L103S, U11-ch15, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	69
Mean	51.09
Std Dev	3.391

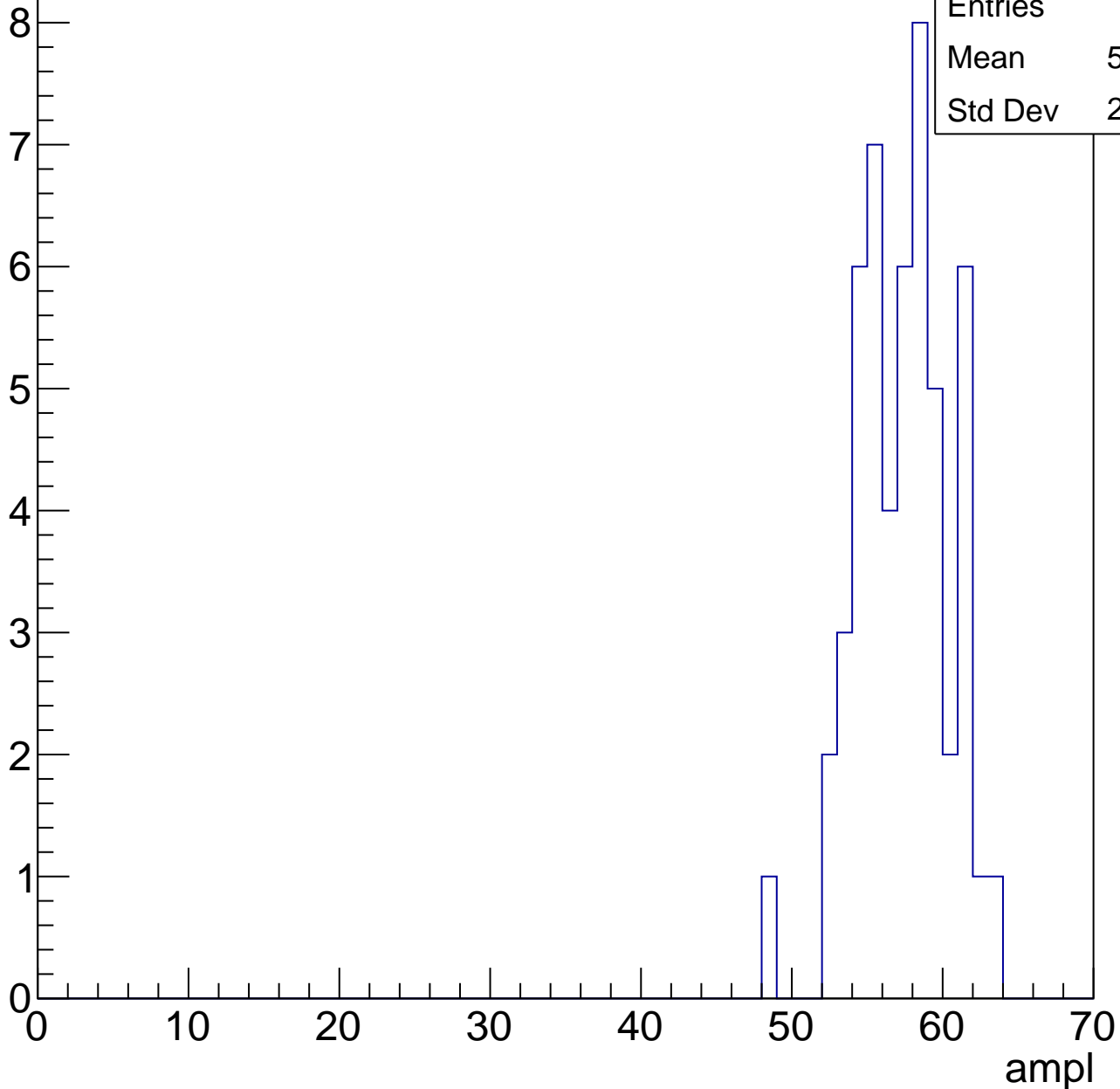


# B1L103S, U11-ch15, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

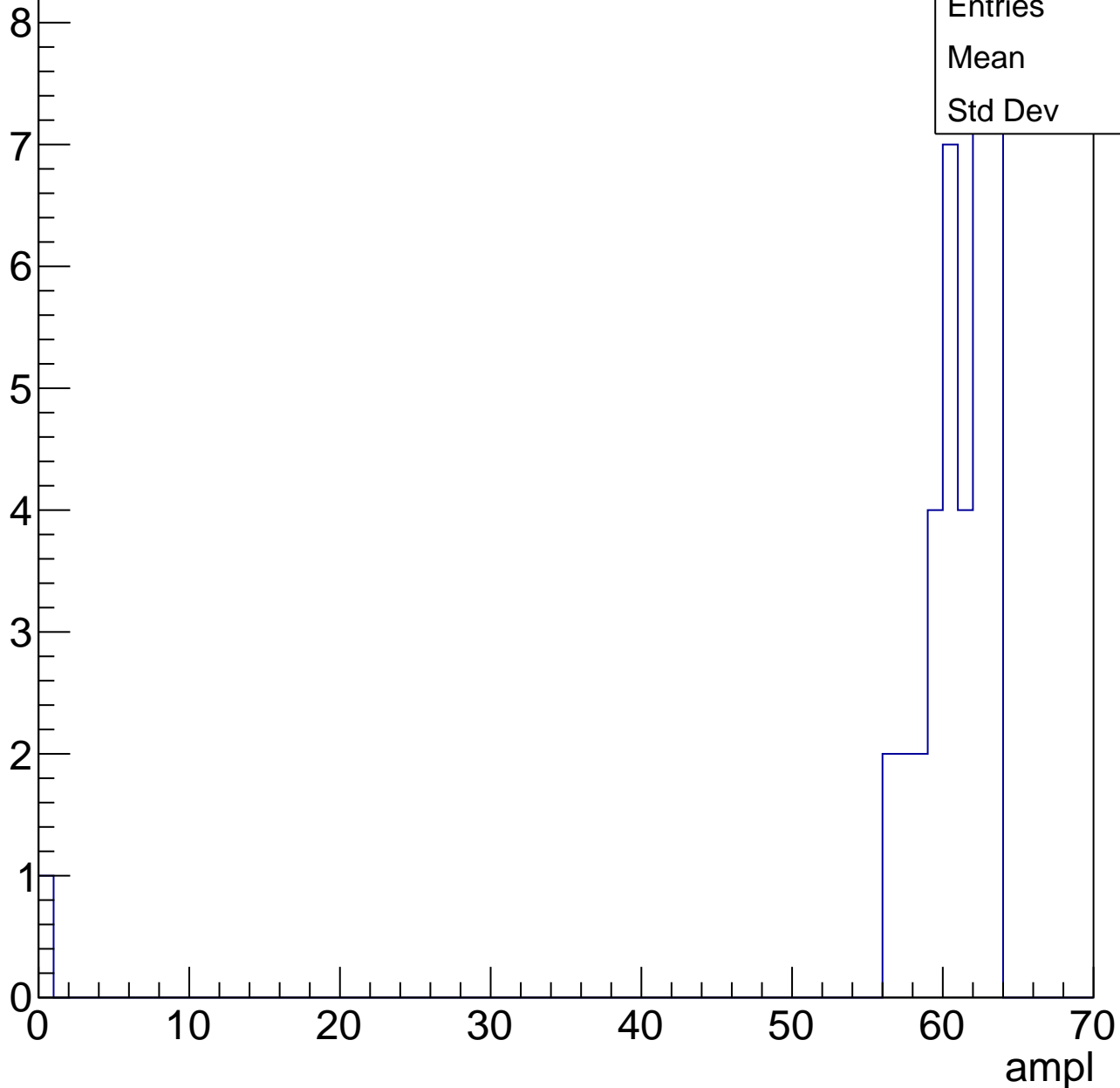
Entries	52
Mean	56.85
Std Dev	2.996



# B1L103S, U11-ch15, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U11-ch15, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U11-ch15, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

1  
0.8  
0.6  
0.4  
0.2  
0

Entries	1
Mean	24
Std Dev	0

ampl

0 10 20 30 40 50 60 70

# B1L103S, U11-ch16, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	83
Mean	28.55
Std Dev	4.757

**Gaus mean : 28.8645**

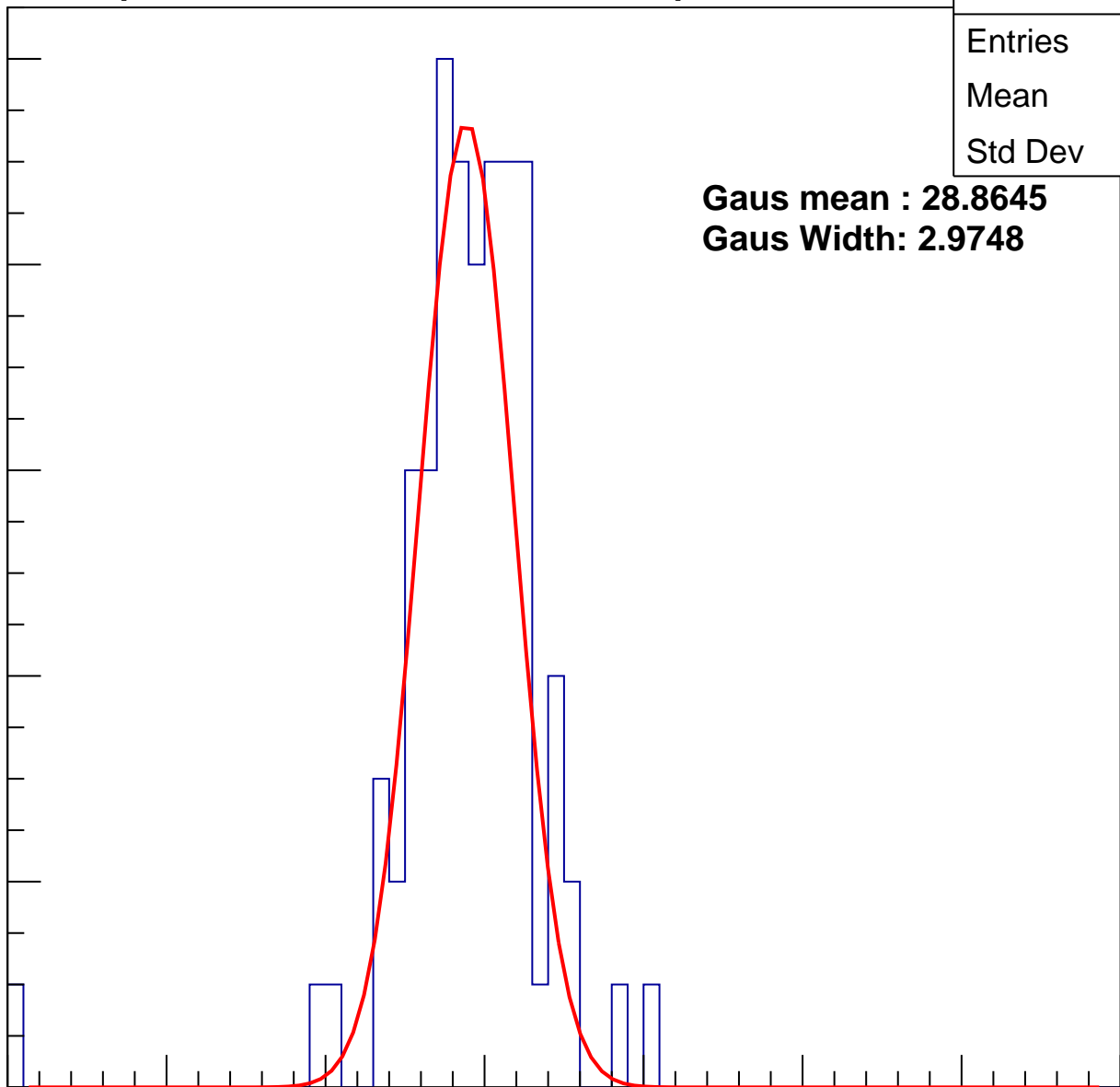
**Gaus Width: 2.9748**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U11-ch16, adc1

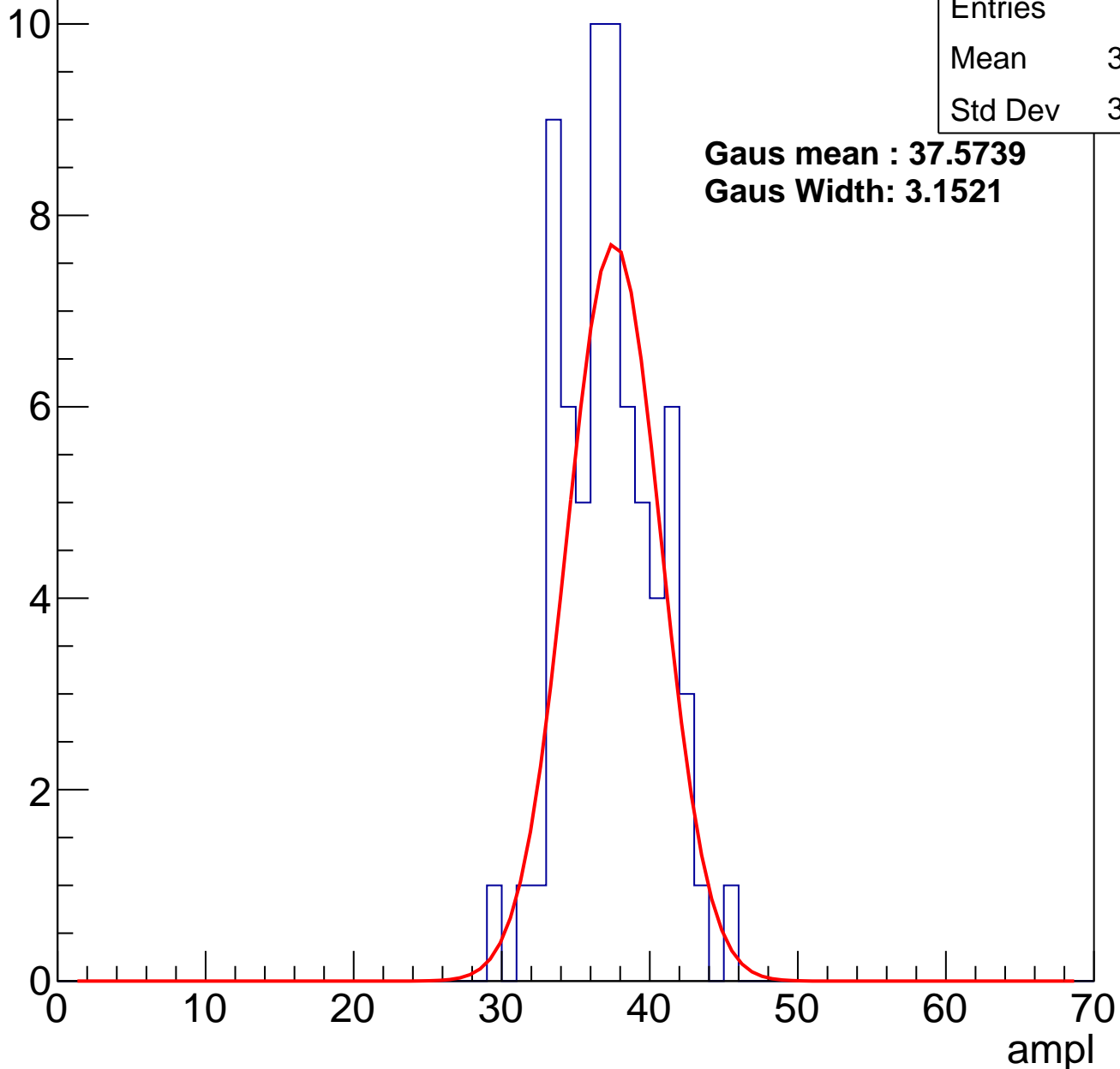
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	69
Mean	36.83
Std Dev	3.148

**Gaus mean : 37.5739**

**Gaus Width: 3.1521**

Entry



# B1L103S, U11-ch16, adc2

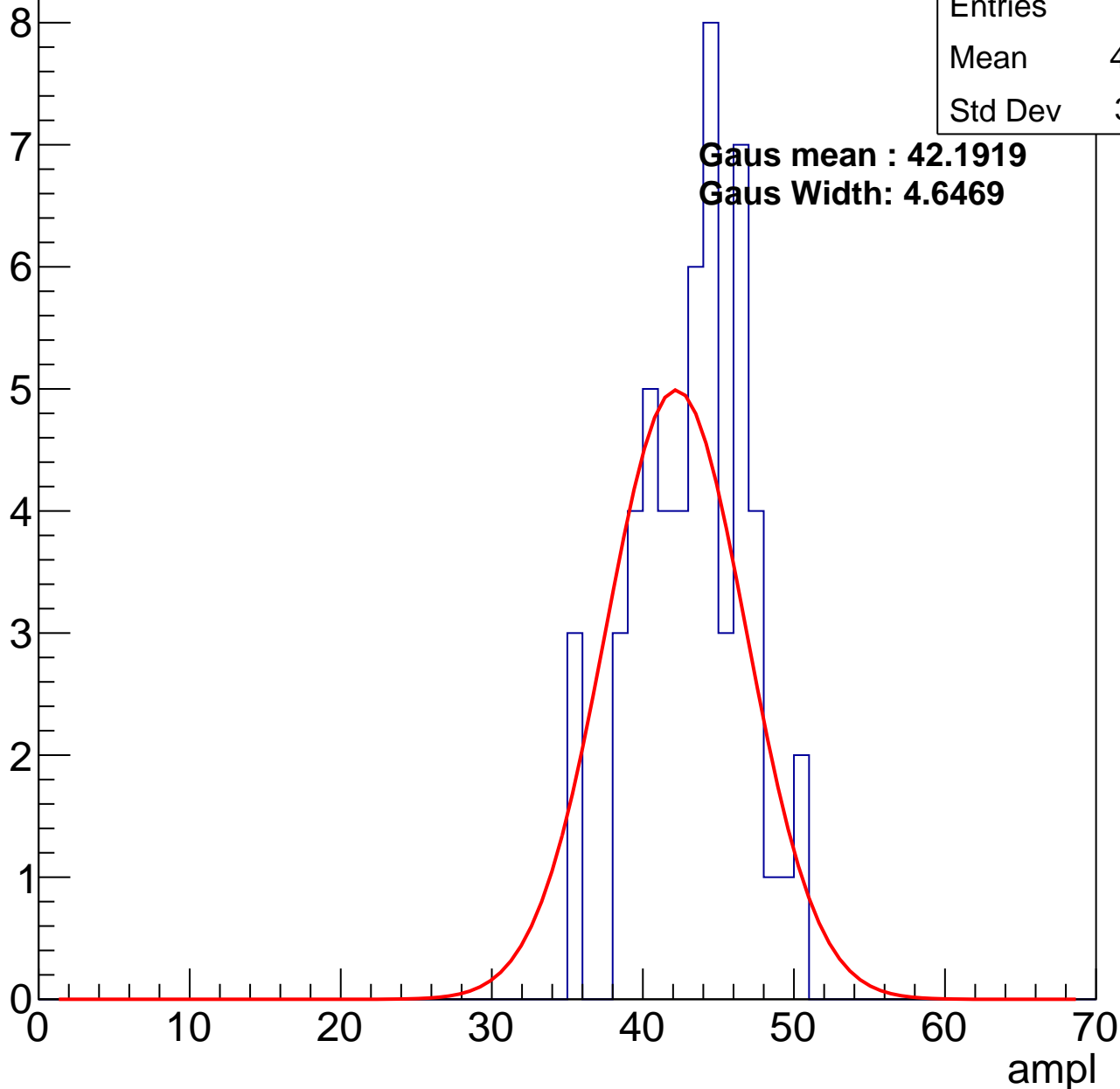
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	55
Mean	42.89
Std Dev	3.571

**Gaus mean : 42.1919**

**Gaus Width: 4.6469**

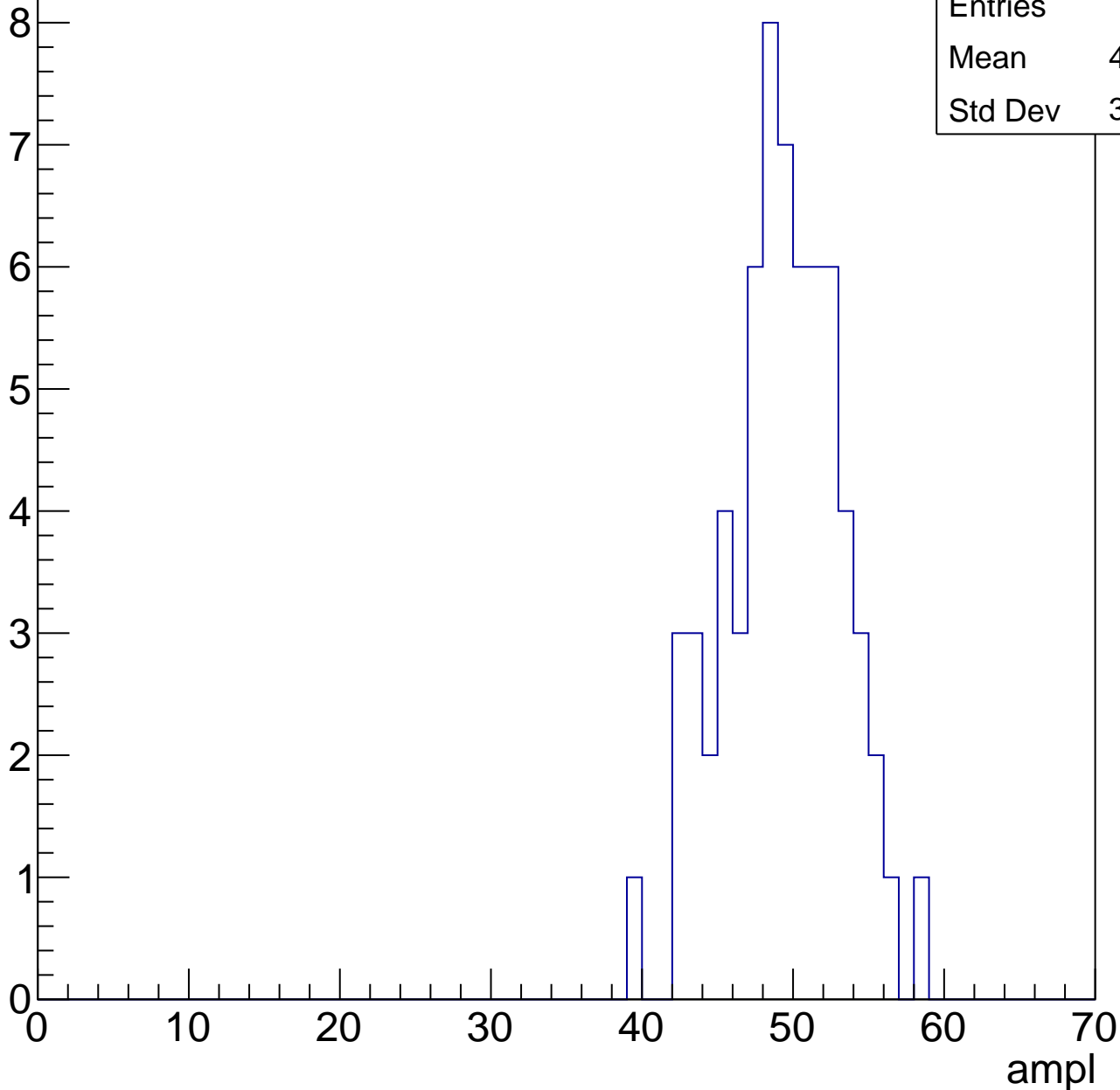


# B1L103S, U11-ch16, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	48.86
Std Dev	3.797

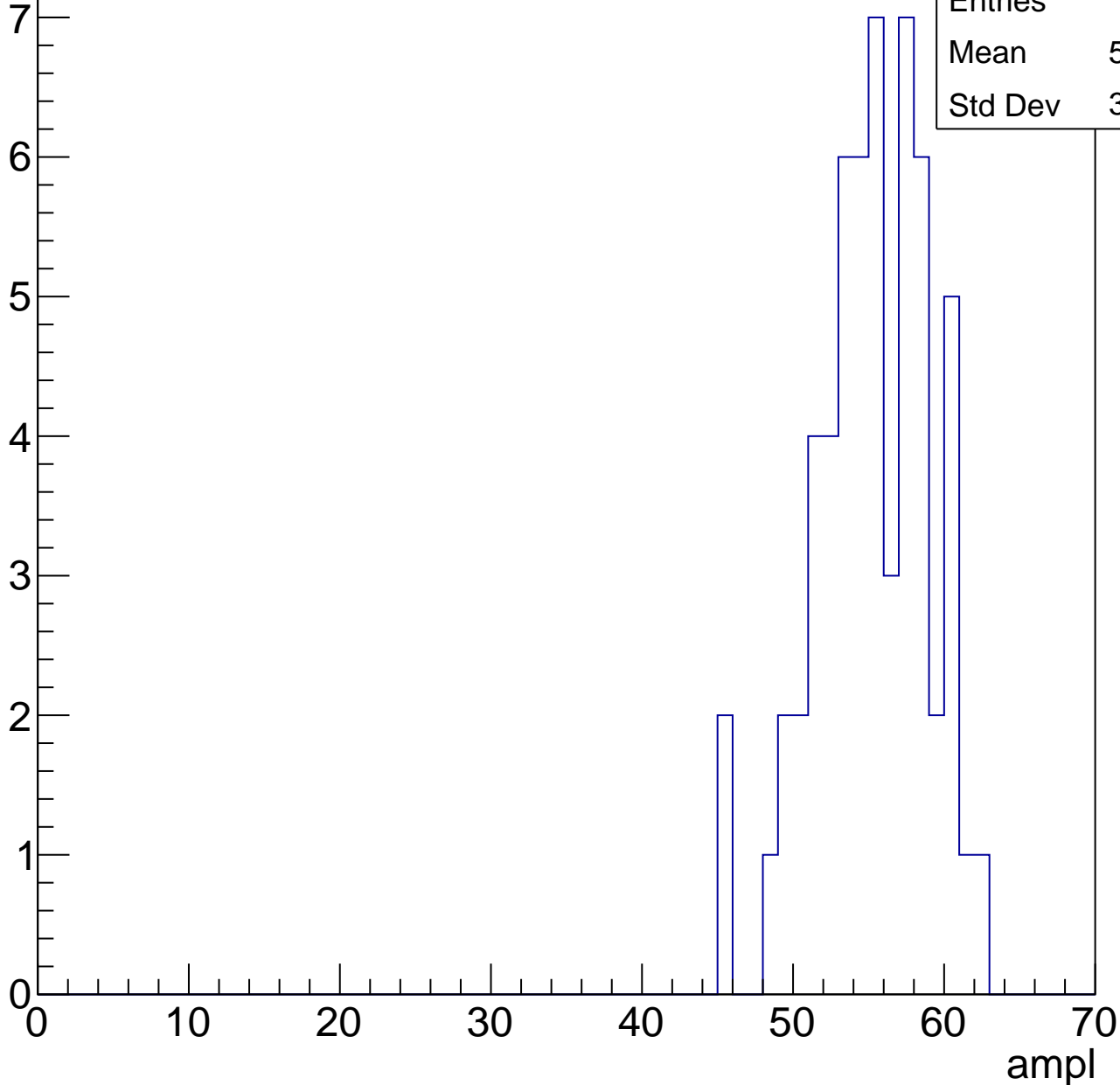


# B1L103S, U11-ch16, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	59
Mean	54.76
Std Dev	3.739



# B1L103S, U11-ch16, adc5

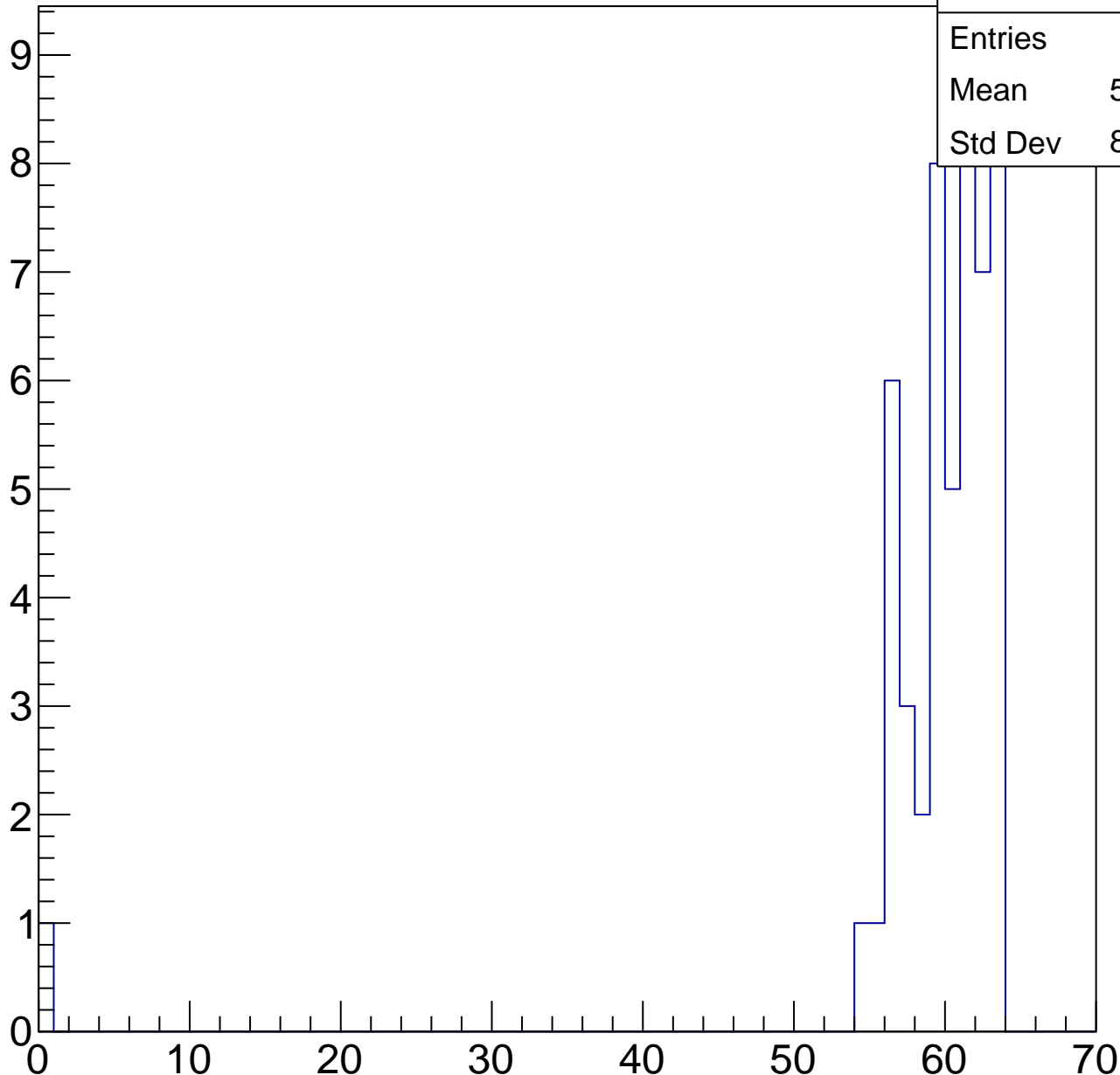
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	51
Mean	58.69
Std Dev	8.665

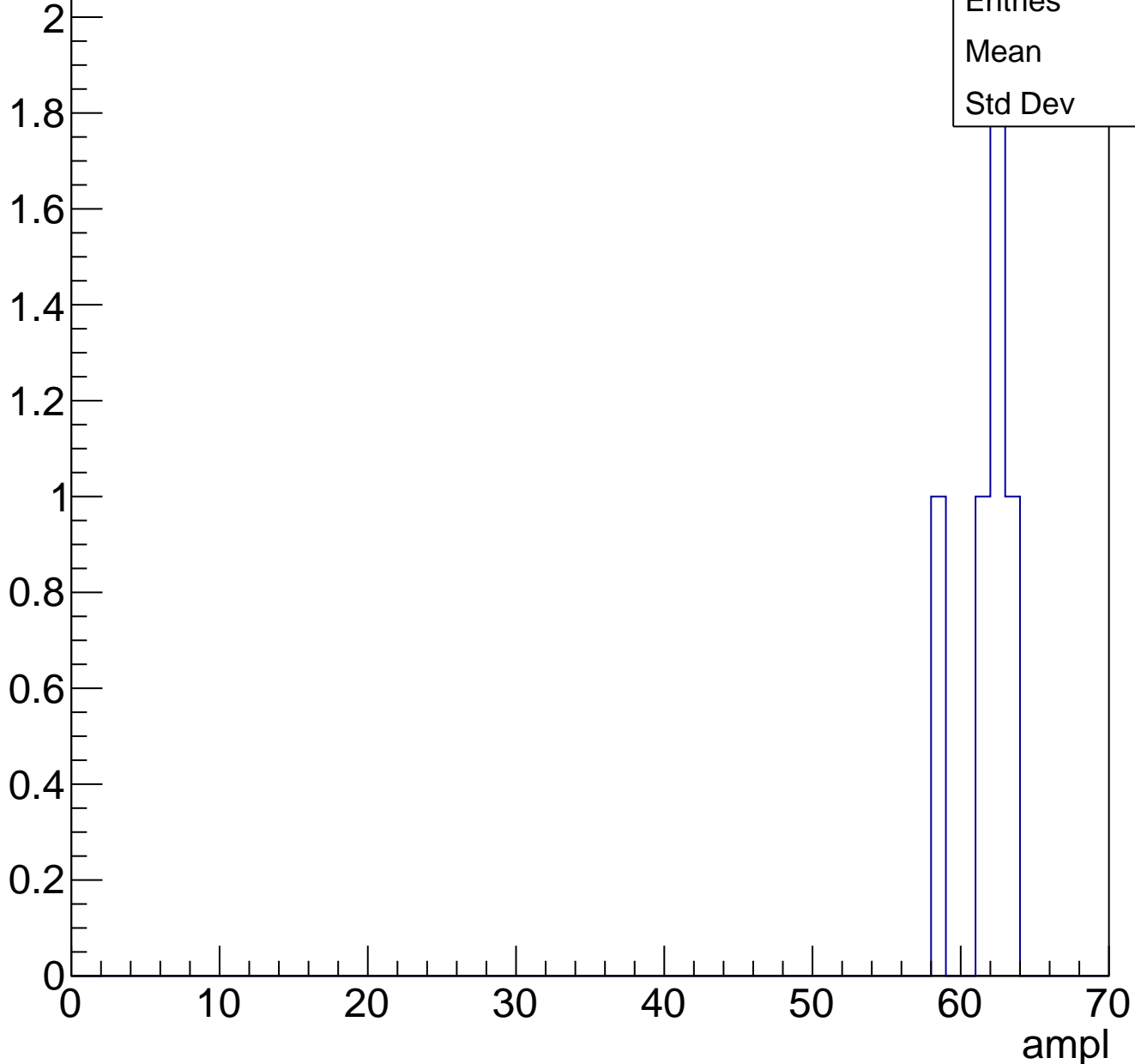
ampl



# B1L103S, U11-ch16, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U11-ch16, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U11-ch17, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	71
Mean	29.69
Std Dev	4.598

**Gaus mean : 30.5315**

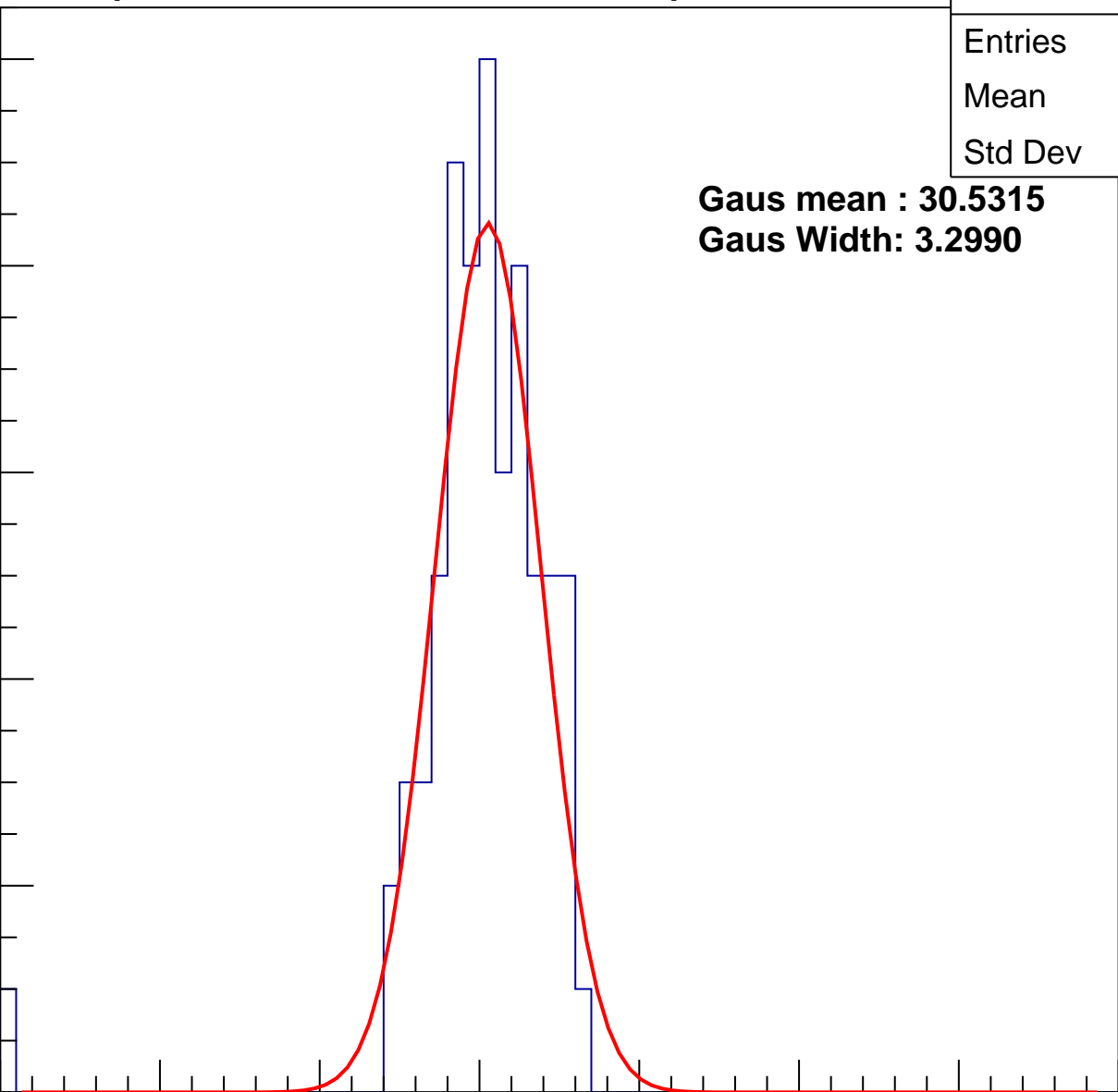
**Gaus Width: 3.2990**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U11-ch17, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	85
Mean	38.07
Std Dev	4.035

**Gaus mean : 38.7301**

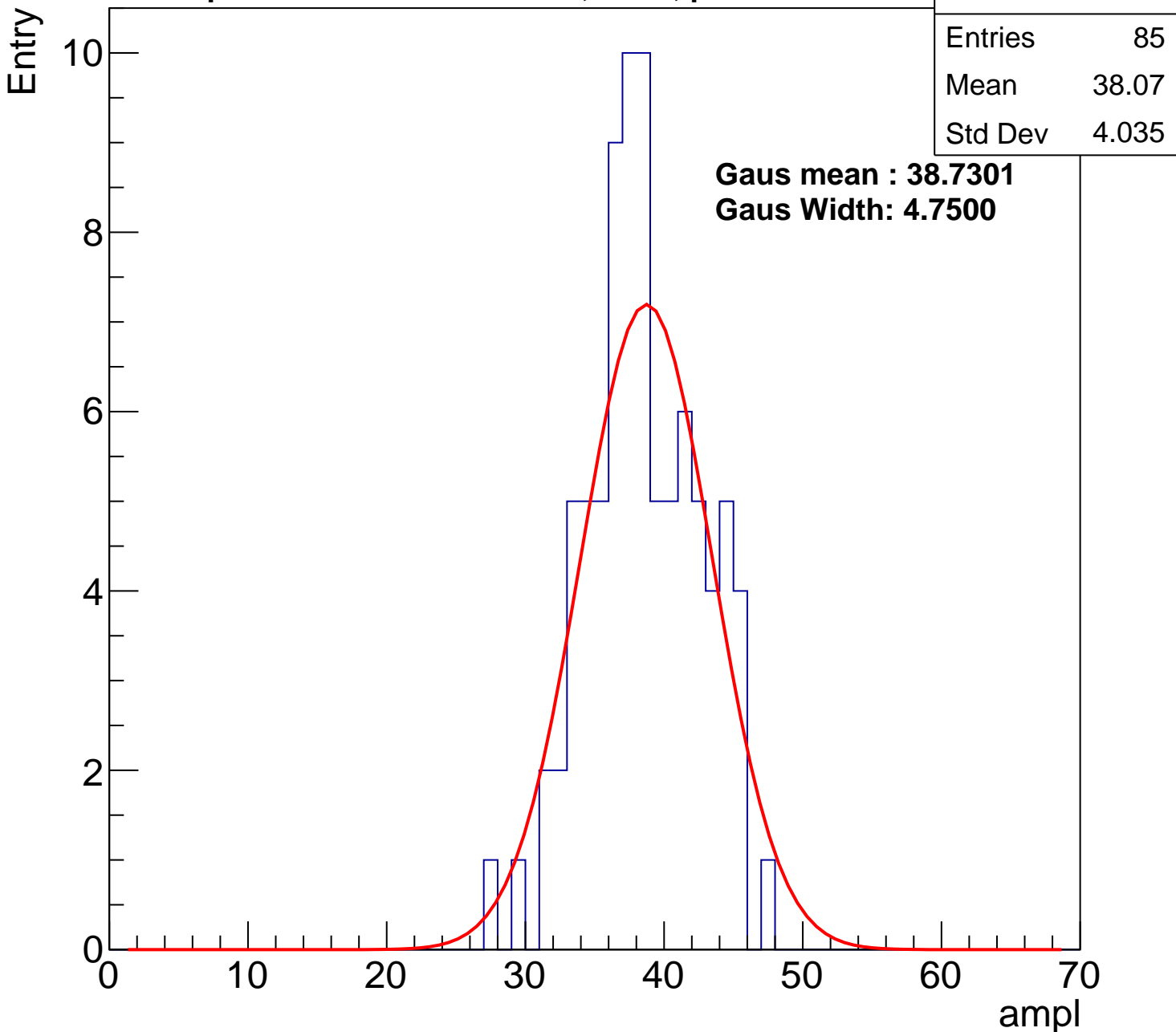
**Gaus Width: 4.7500**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B1L103S, U11-ch17, adc2

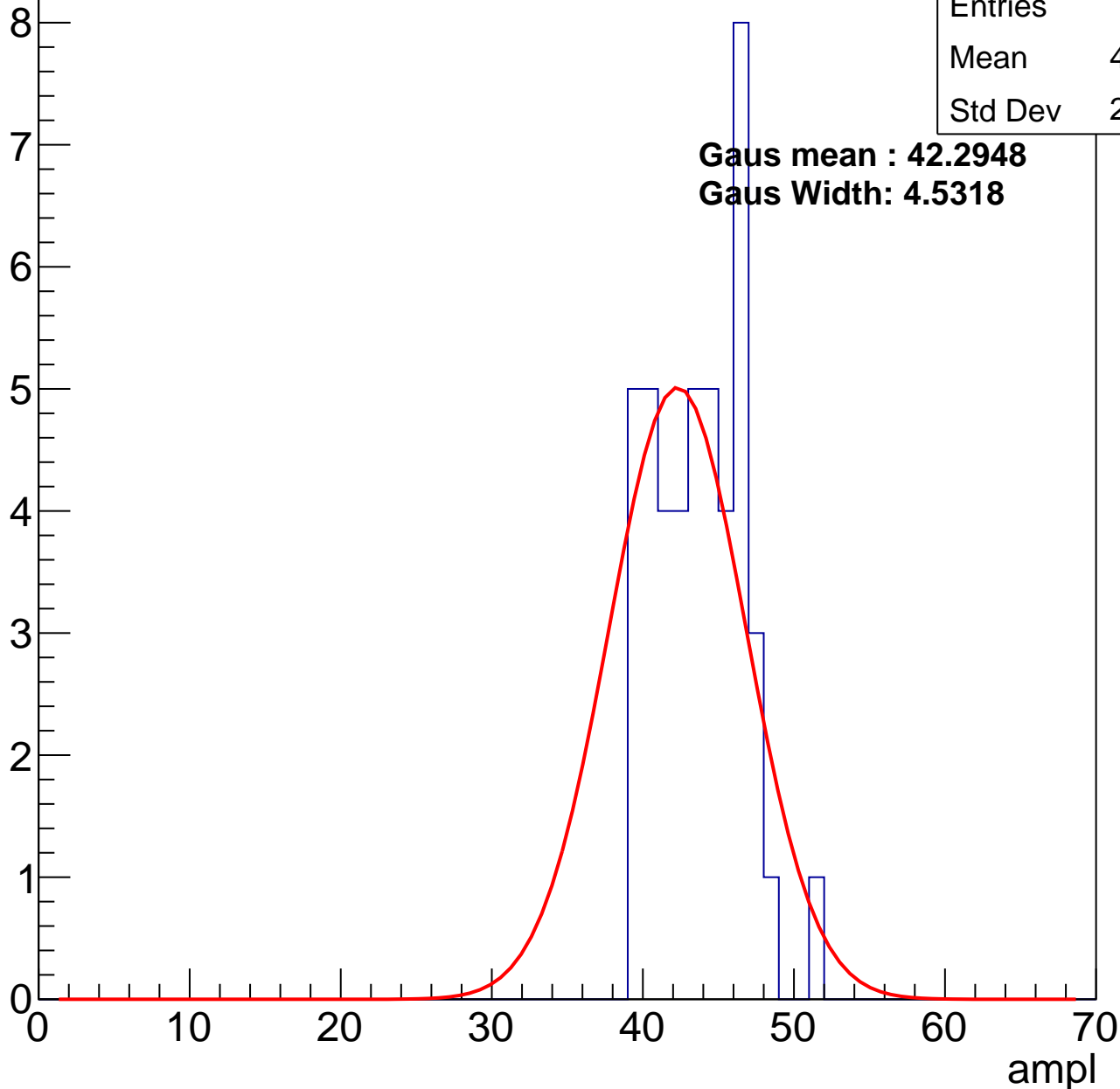
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	45
Mean	43.33
Std Dev	2.867

**Gaus mean : 42.2948**

**Gaus Width: 4.5318**



# B1L103S, U11-ch17, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

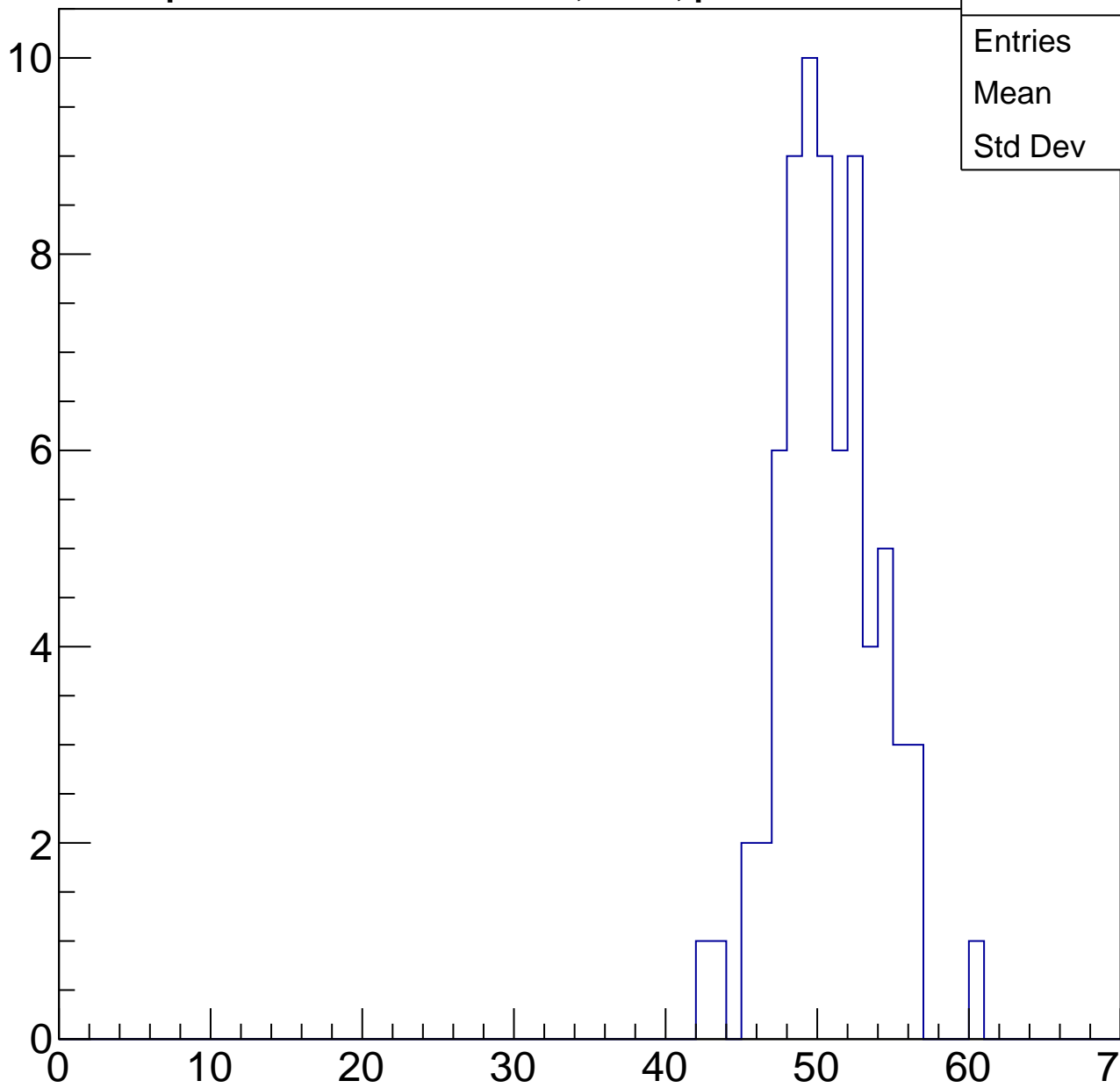
Entries	71
Mean	50.28
Std Dev	3.207

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B1L103S, U11-ch17, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

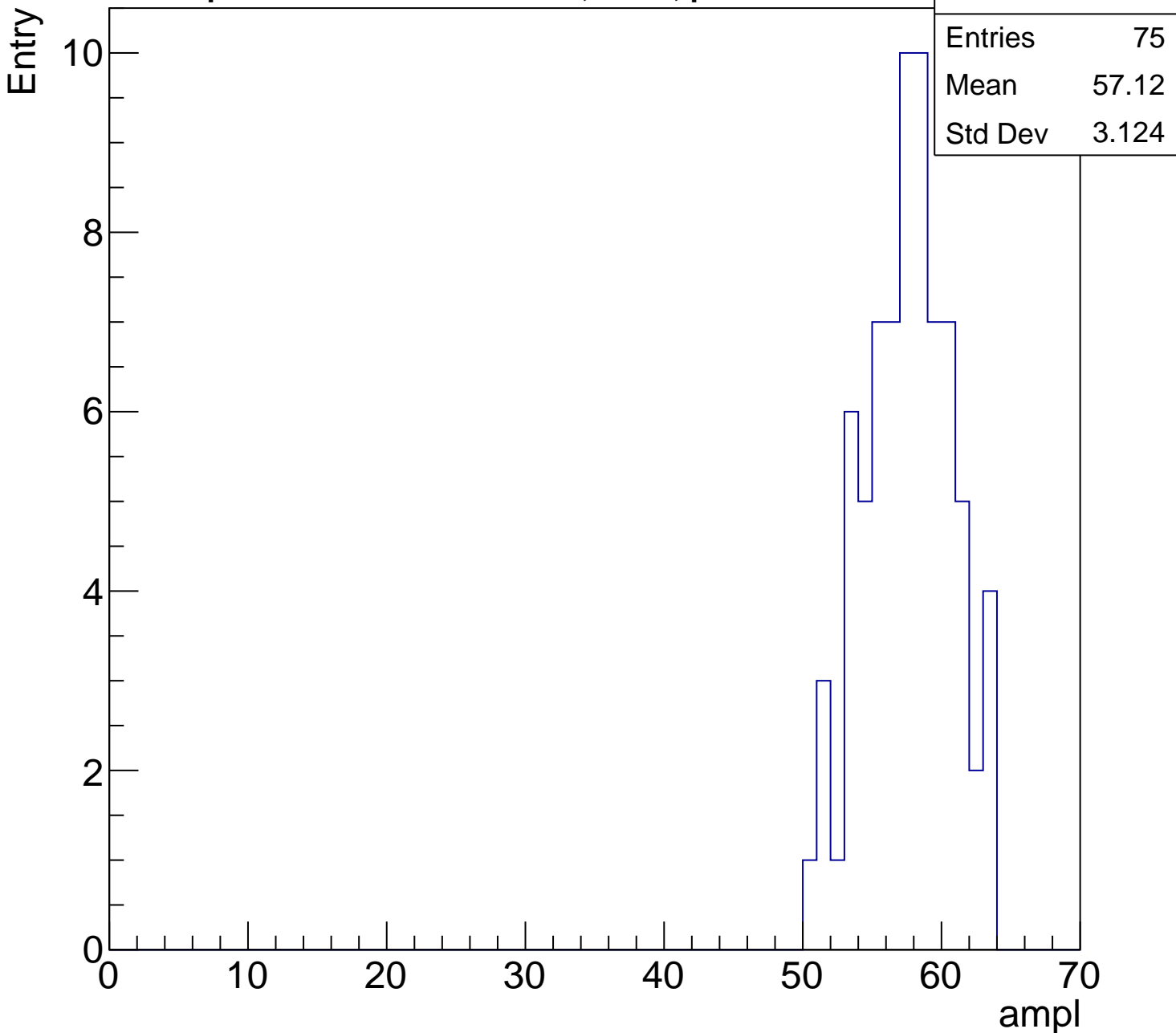
Entries	75
Mean	57.12
Std Dev	3.124

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

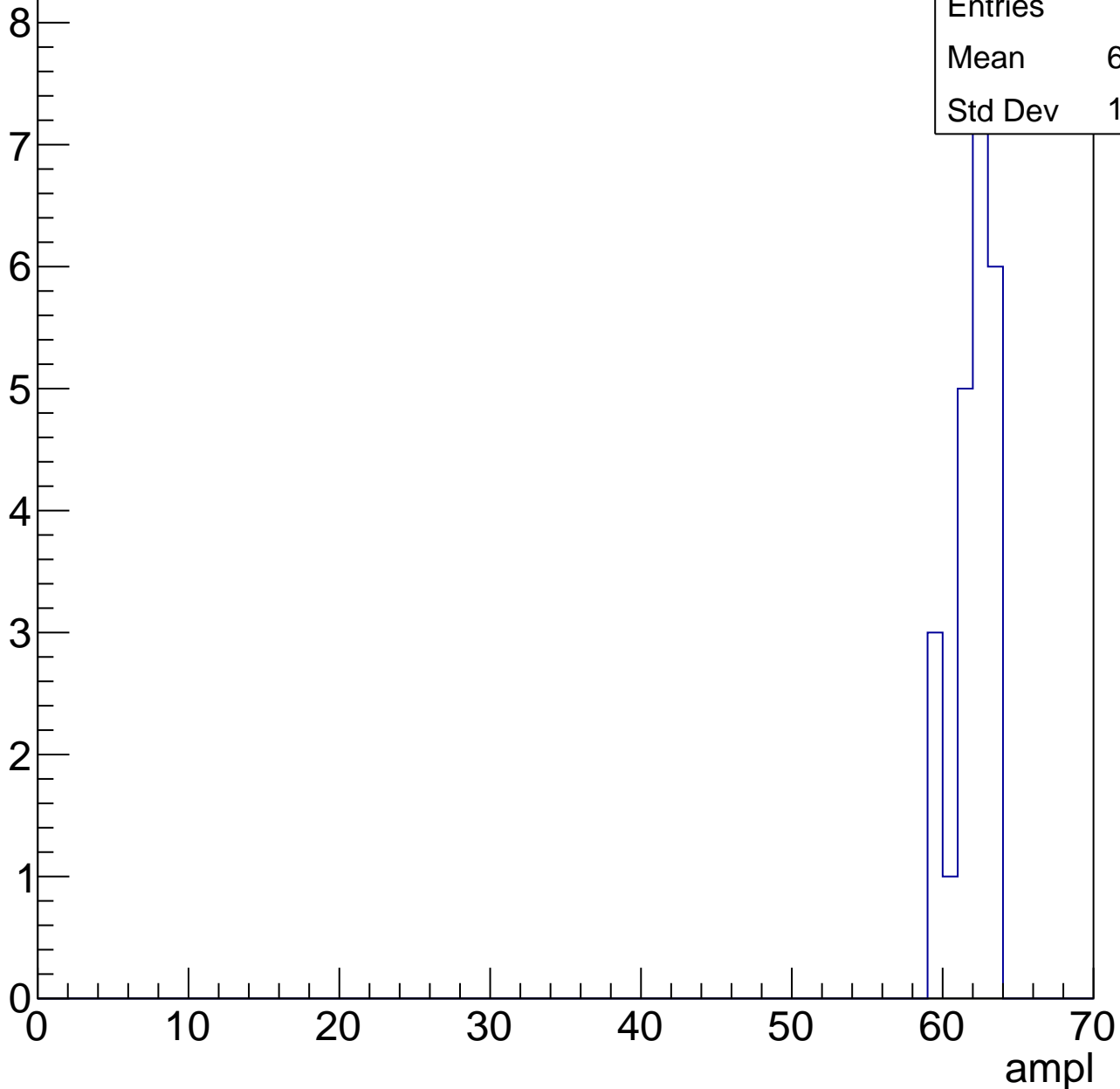


# B1L103S, U11-ch17, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

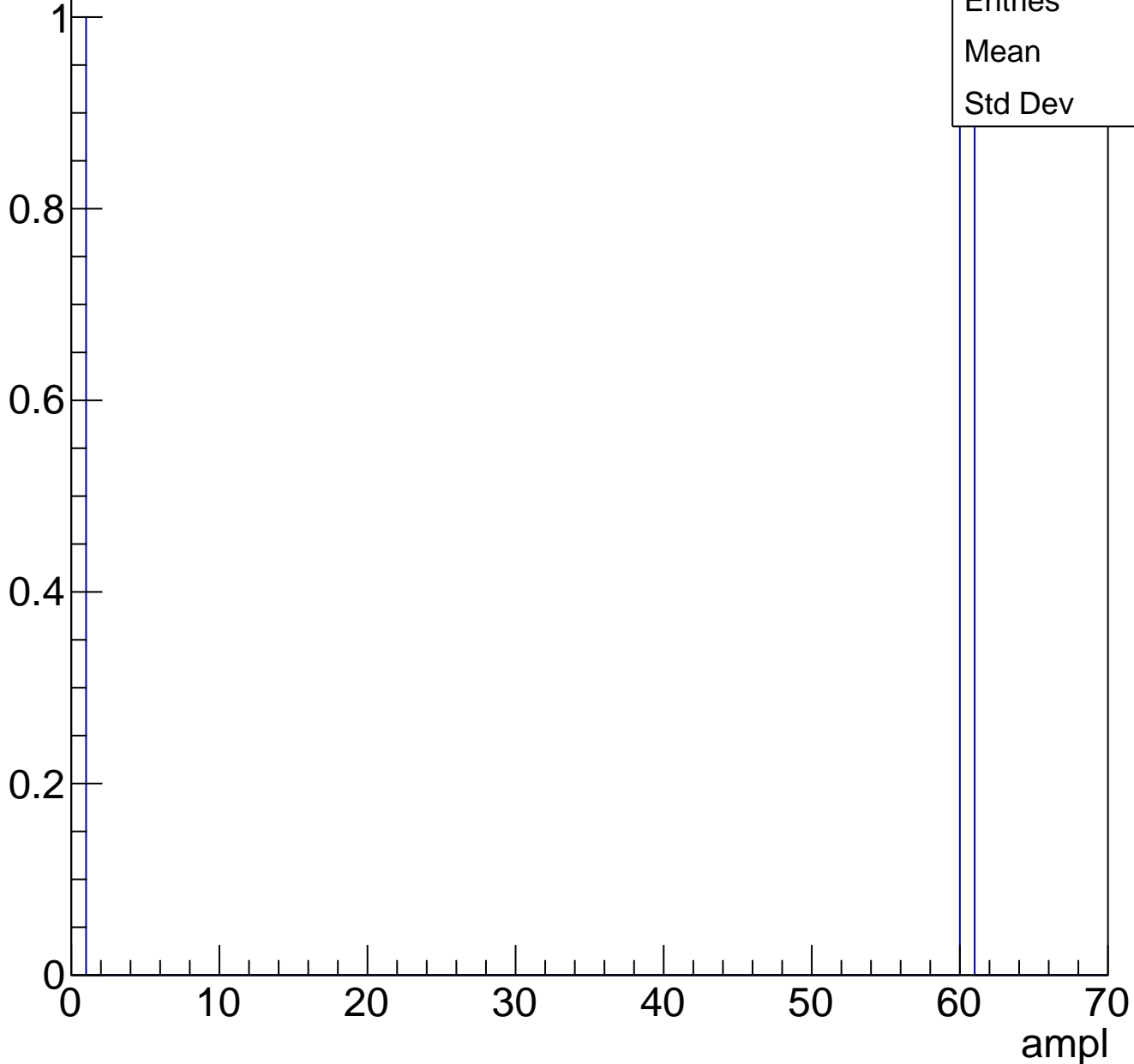
Entries	23
Mean	61.57
Std Dev	1.279



# B1L103S, U11-ch17, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U11-ch17, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	23
Std Dev	0

# B1L103S, U11-ch18, adc0

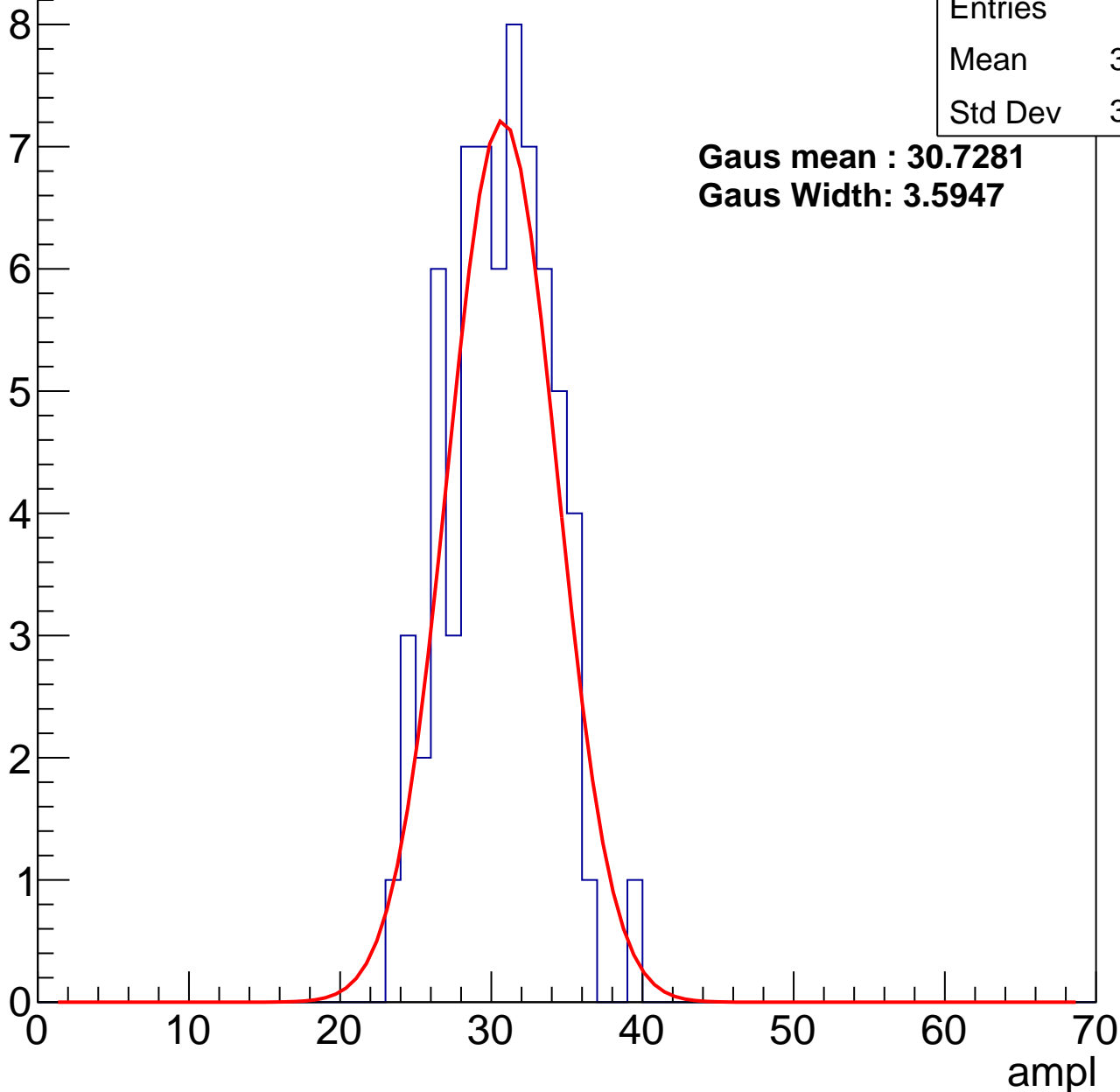
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	30.09
Std Dev	3.349

**Gaus mean : 30.7281**

**Gaus Width: 3.5947**



# B1L103S, U11-ch18, adc1

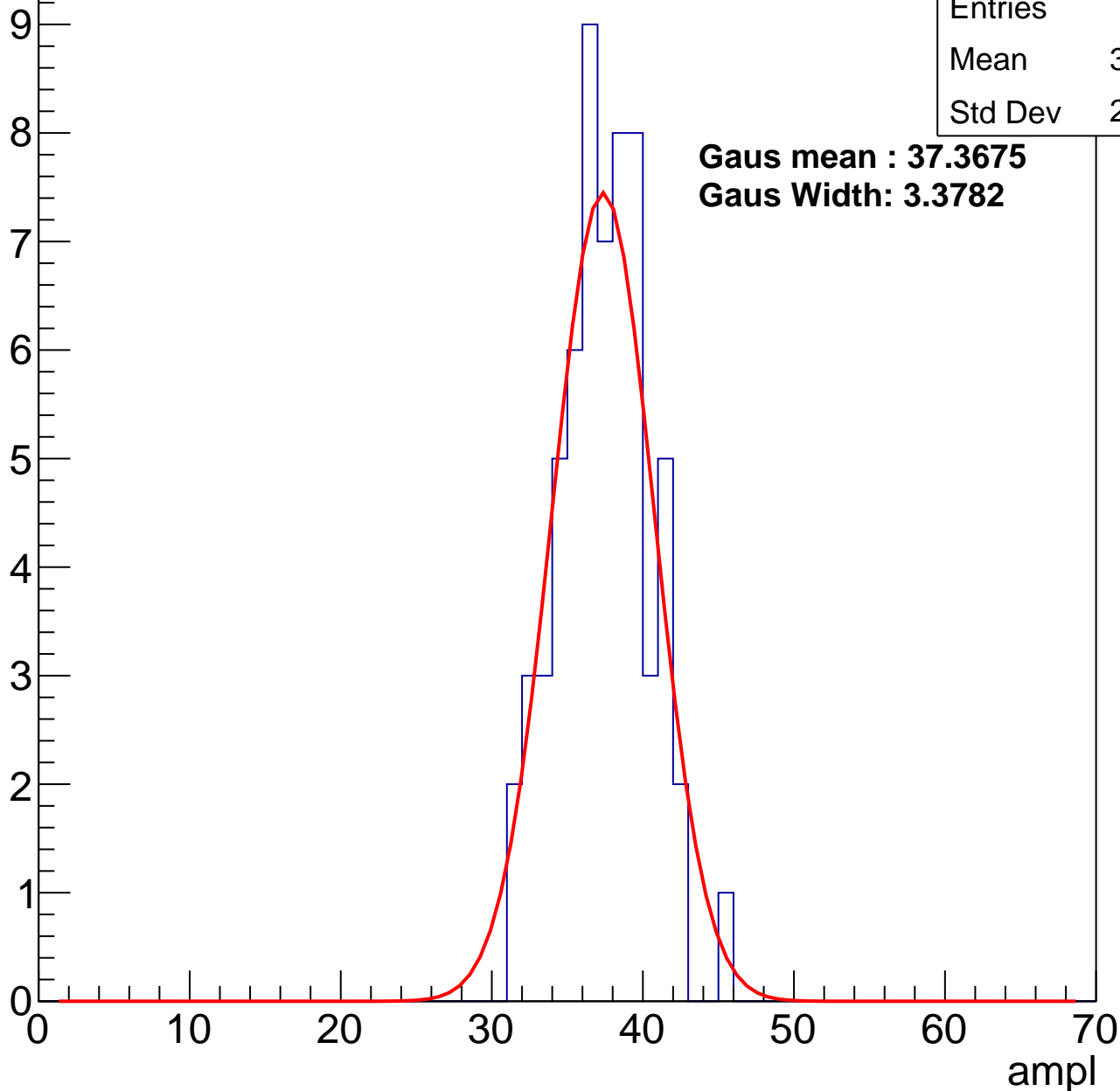
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	36.94
Std Dev	2.934

**Gaus mean : 37.3675**

**Gaus Width: 3.3782**



# B1L103S, U11-ch18, adc2

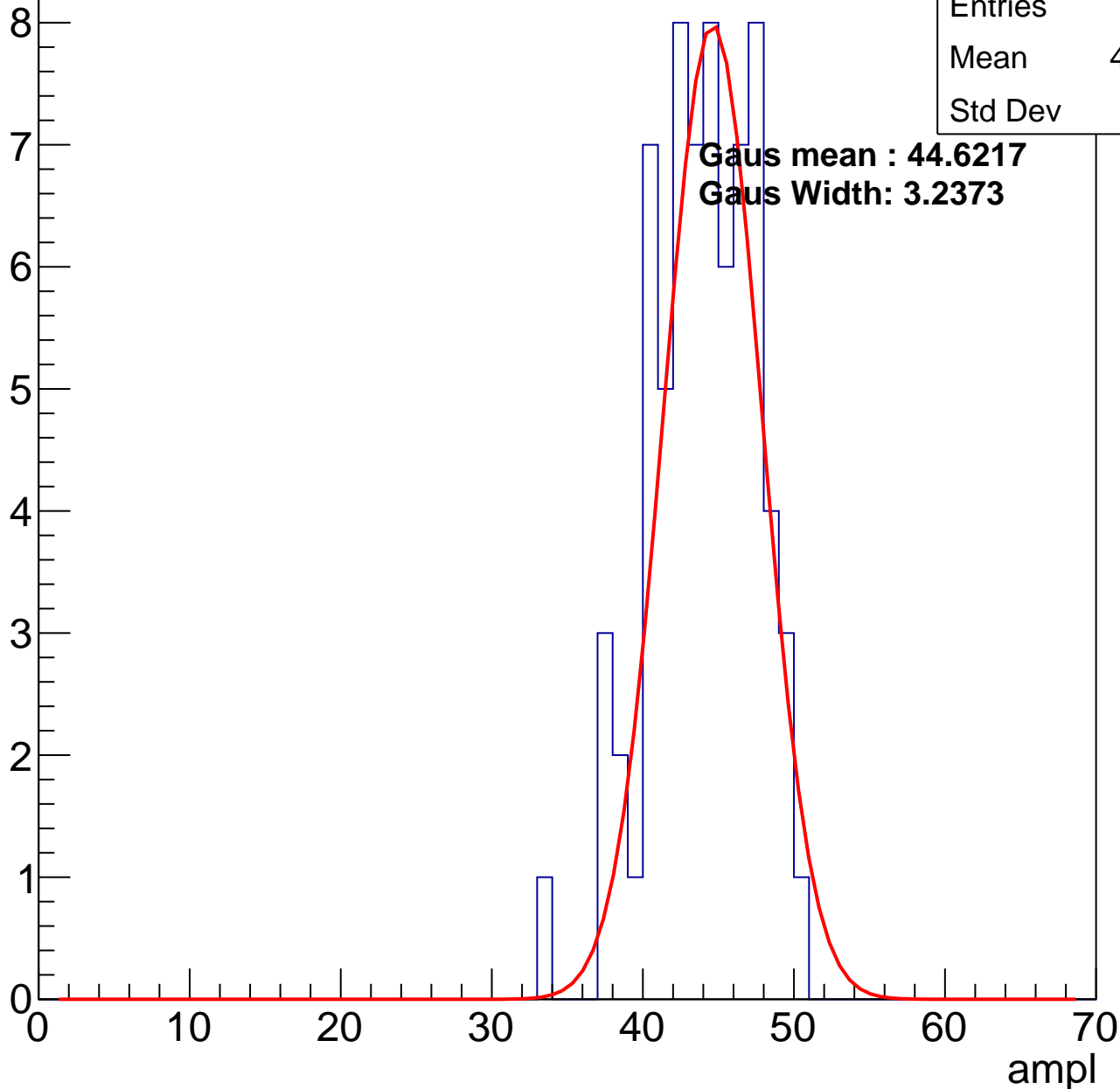
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	71
Mean	43.52
Std Dev	3.41

**Gaus mean : 44.6217**

**Gaus Width: 3.2373**

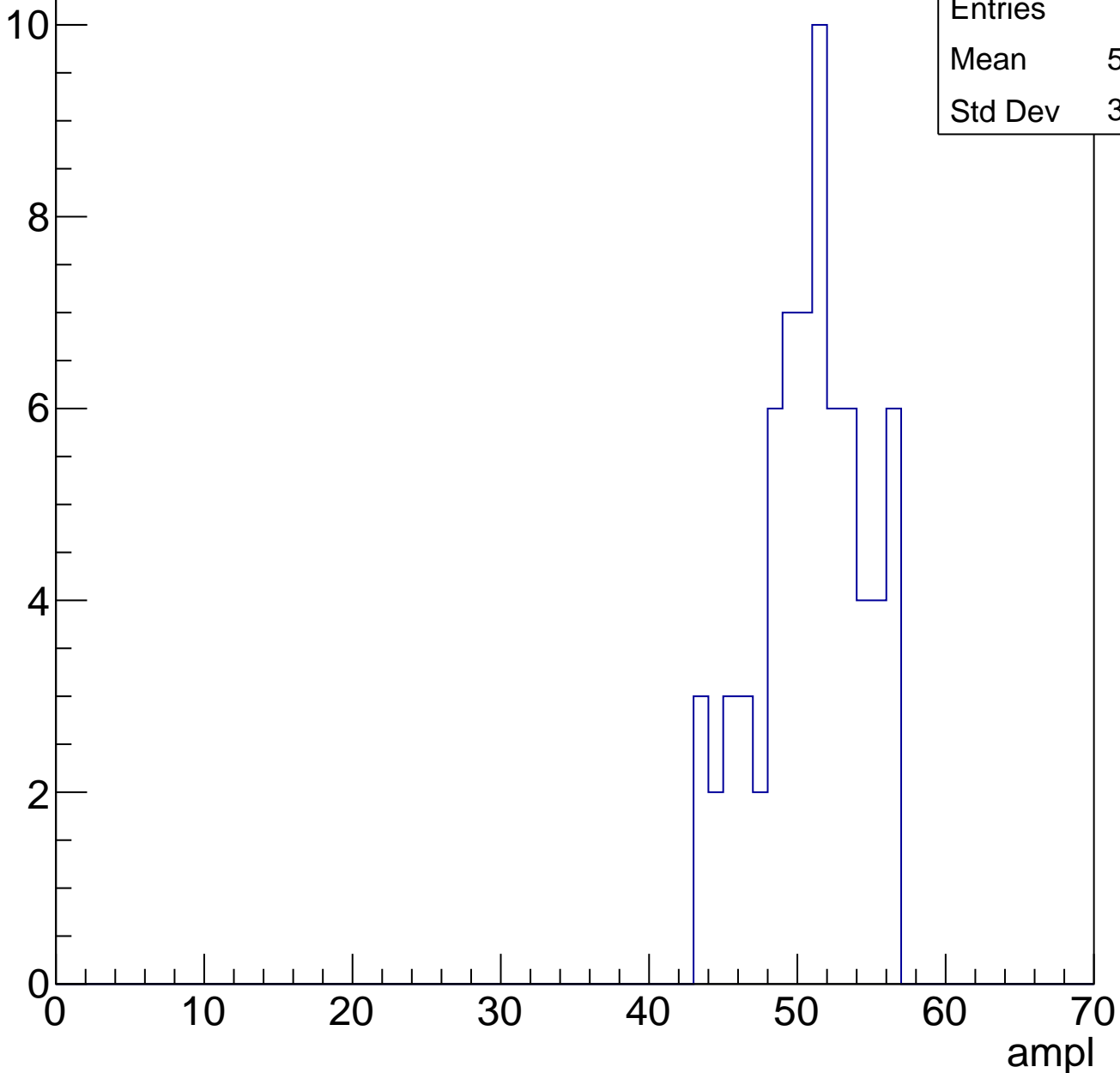


# B1L103S, U11-ch18, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

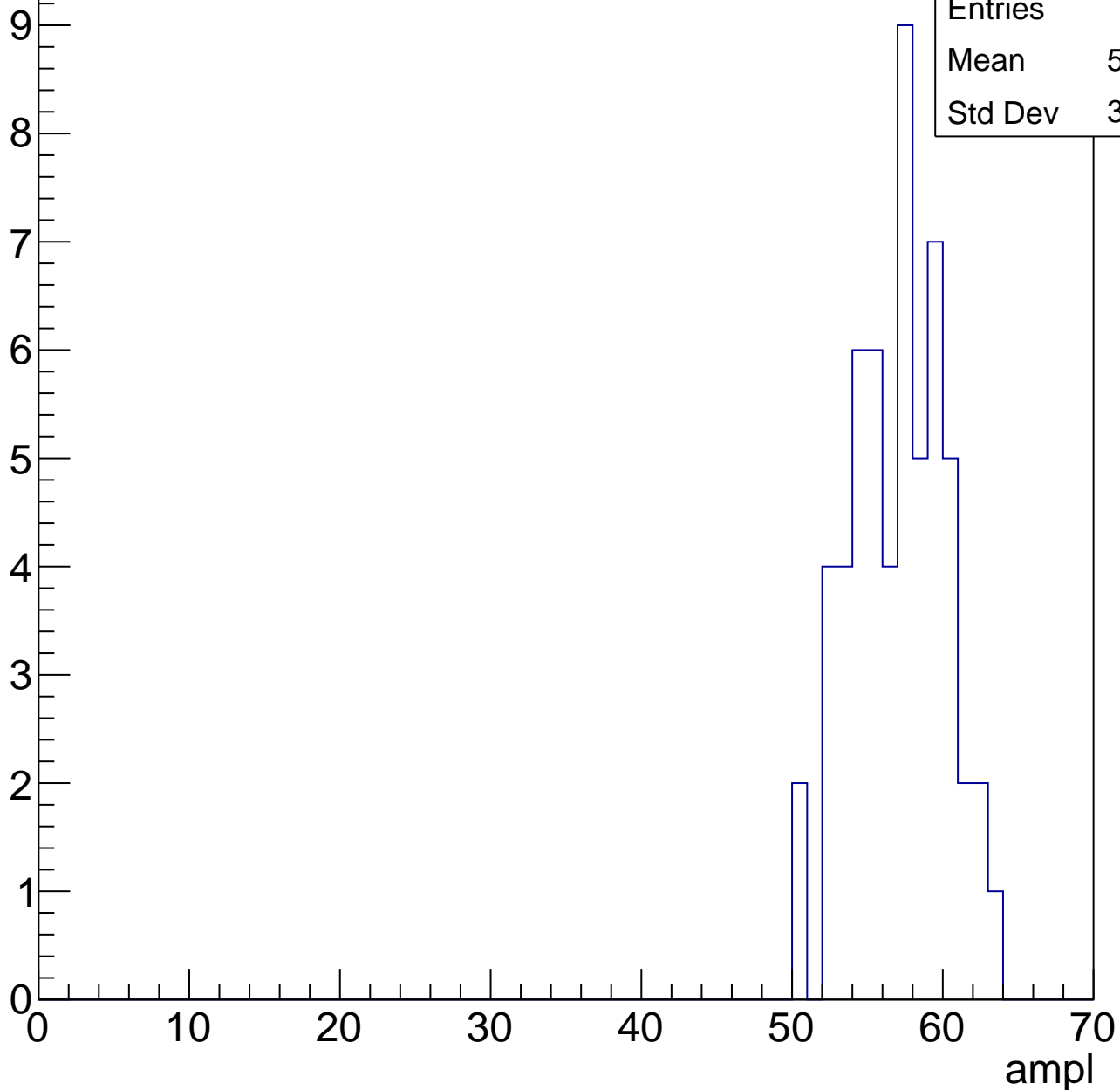
Entries	69
Mean	50.39
Std Dev	3.507



# B1L103S, U11-ch18, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

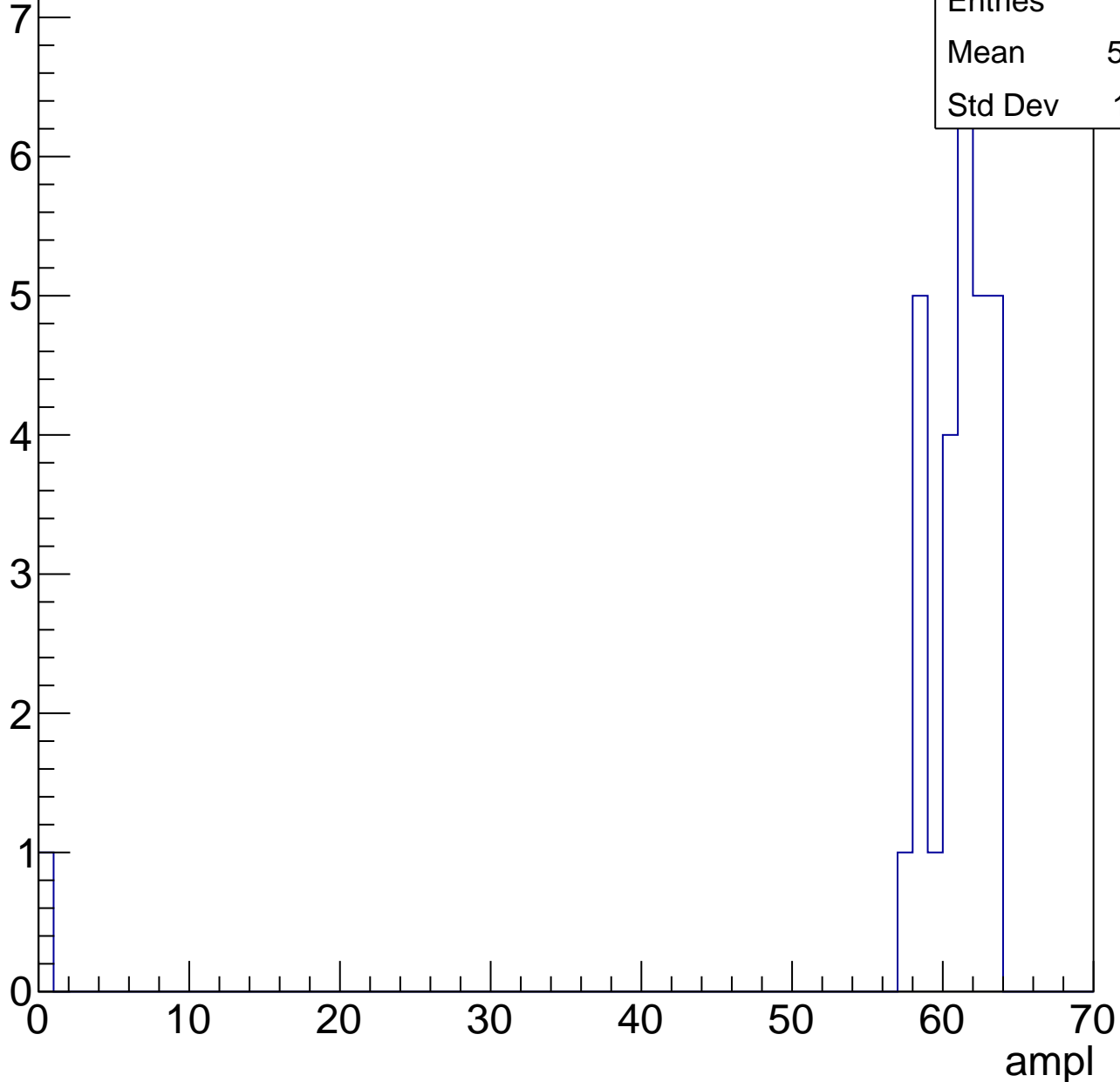


# B1L103S, U11-ch18, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

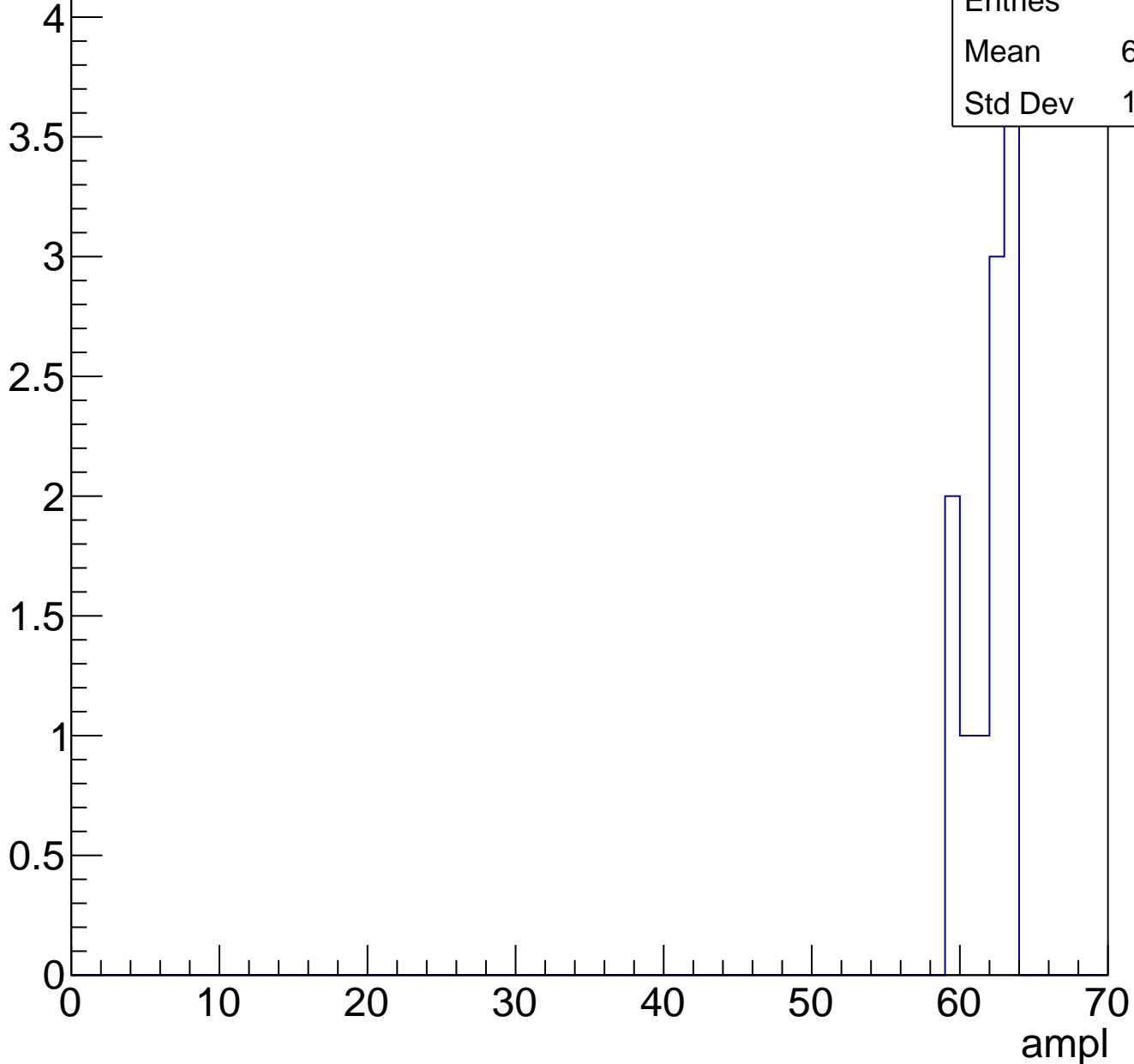
Entries	29
Mean	58.55
Std Dev	11.21



# B1L103S, U11-ch18, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U11-ch18, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U11-ch19, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	74
Mean	29.11
Std Dev	4.755

**Gaus mean : 29.8565**

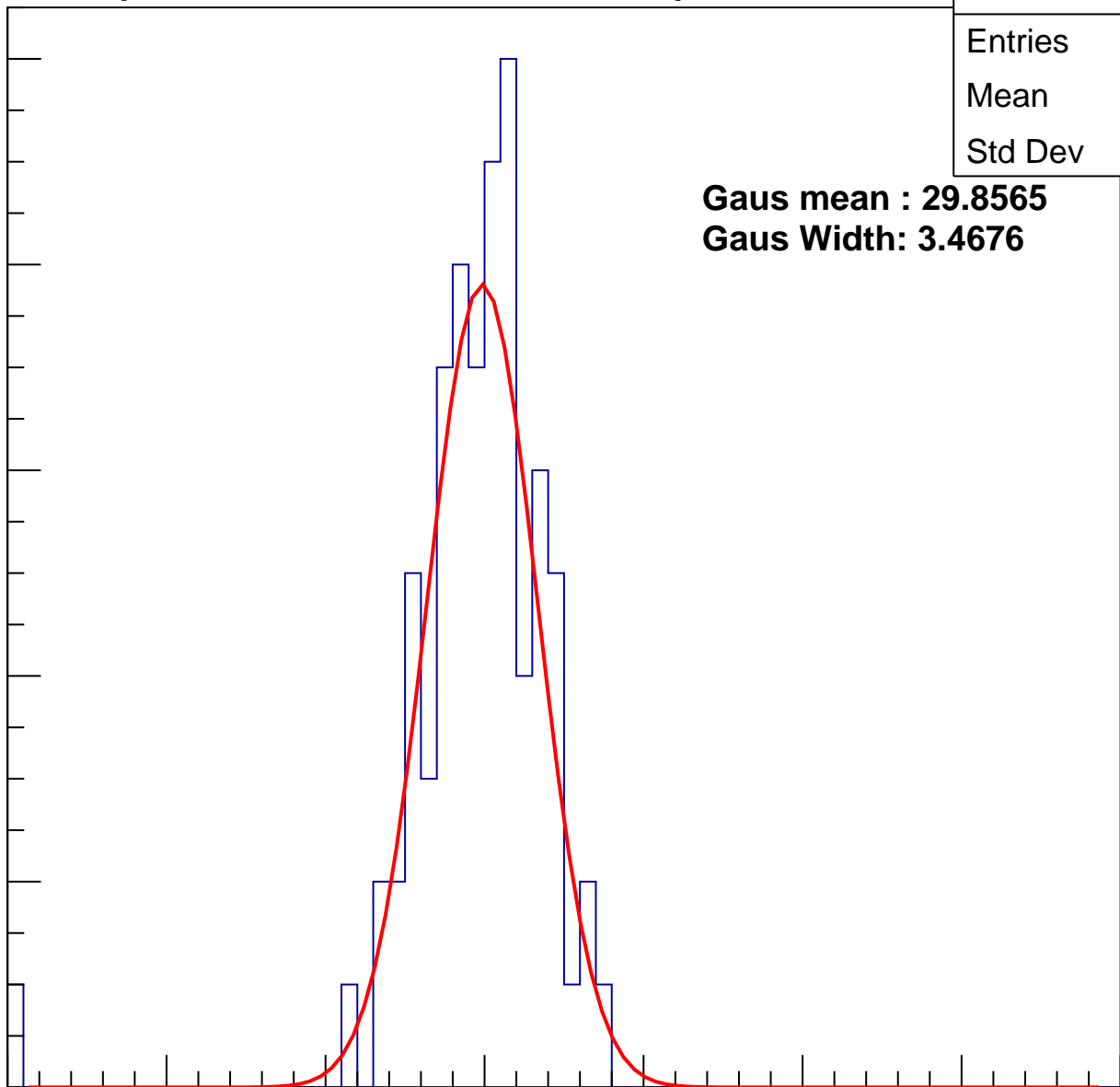
**Gaus Width: 3.4676**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B1L103S, U11-ch19, adc1

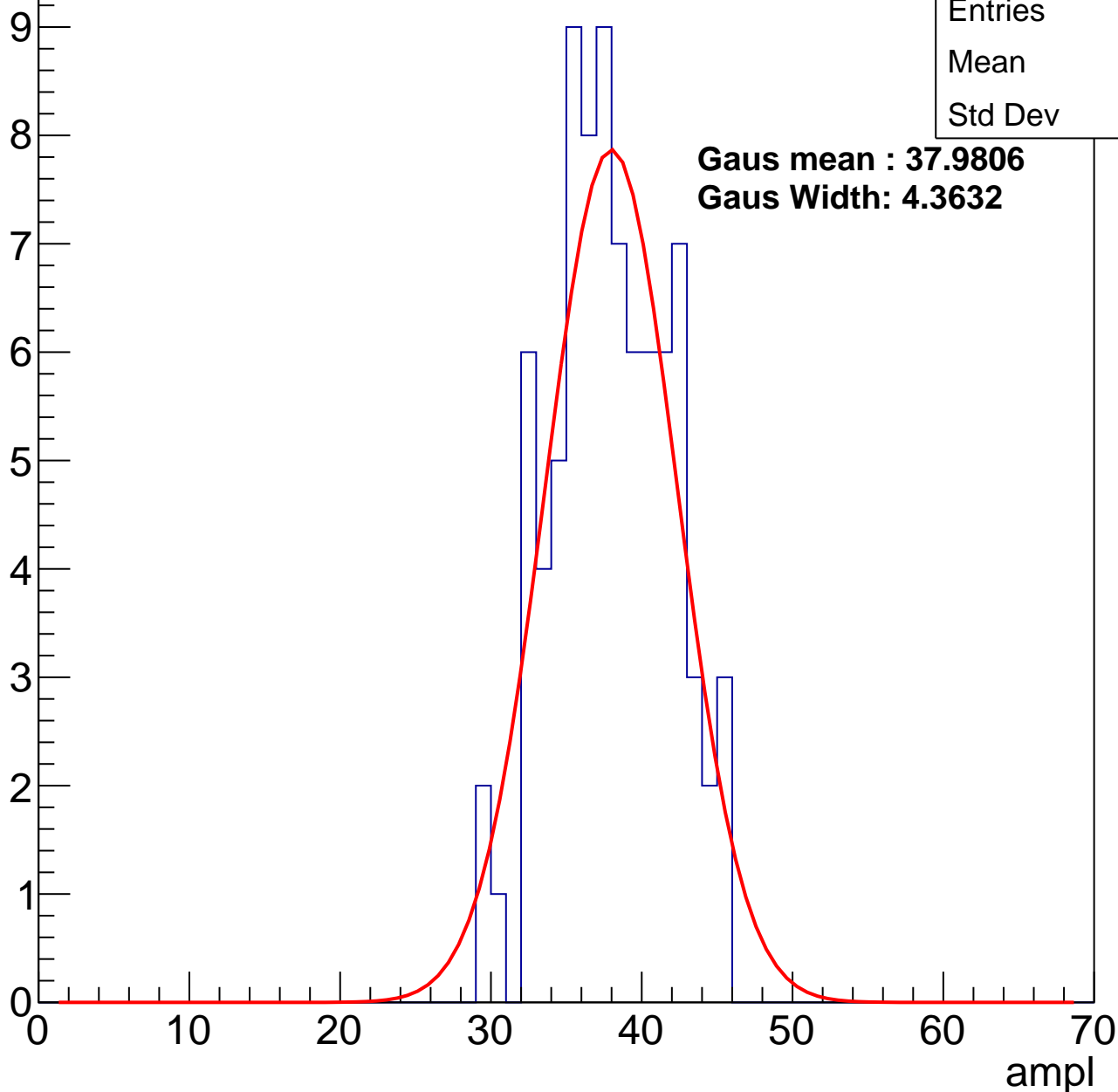
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	84
Mean	37.5
Std Dev	3.8

**Gaus mean : 37.9806**

**Gaus Width: 4.3632**



# B1L103S, U11-ch19, adc2

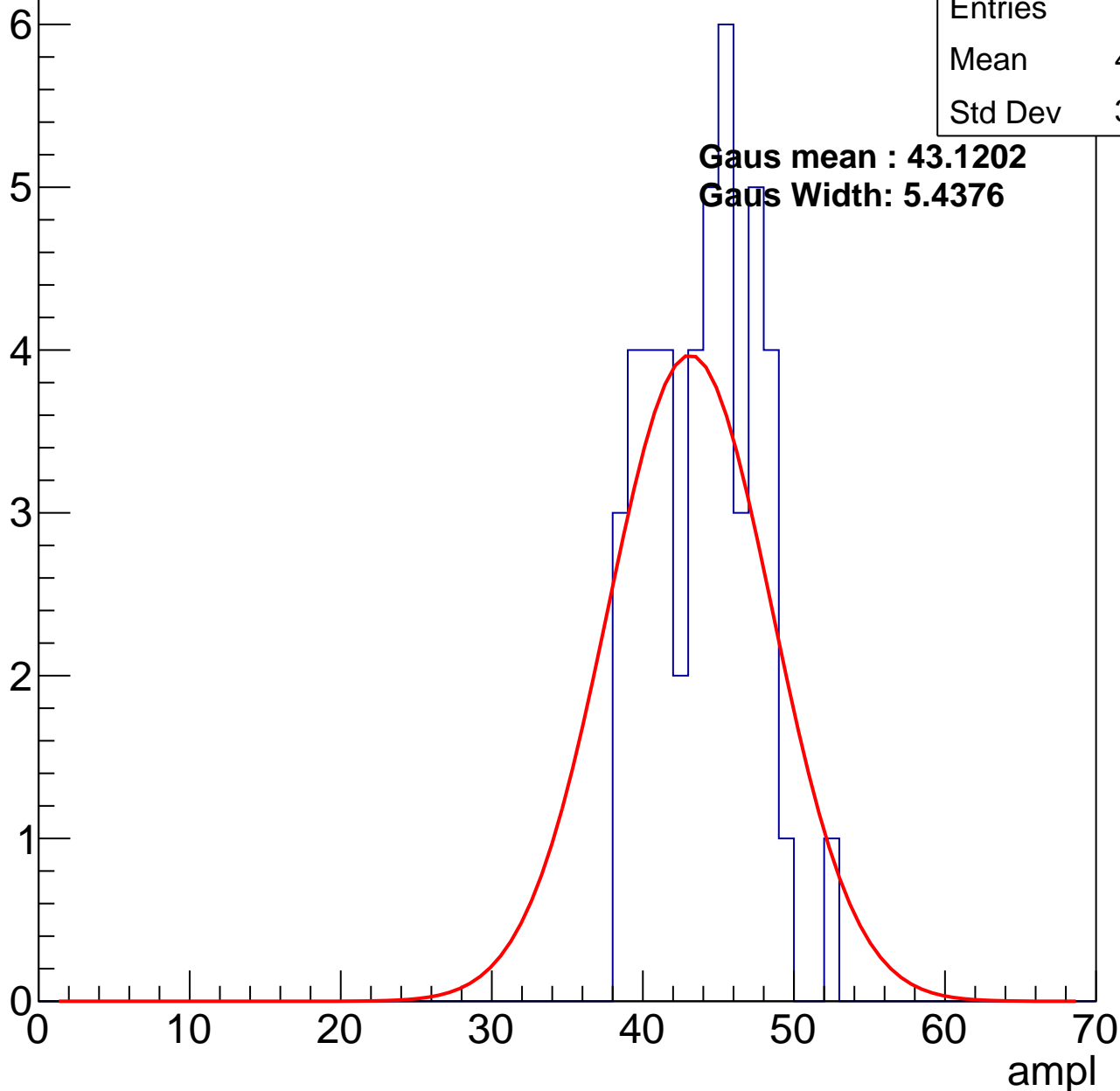
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	46
Mean	43.61
Std Dev	3.391

**Gaus mean : 43.1202**

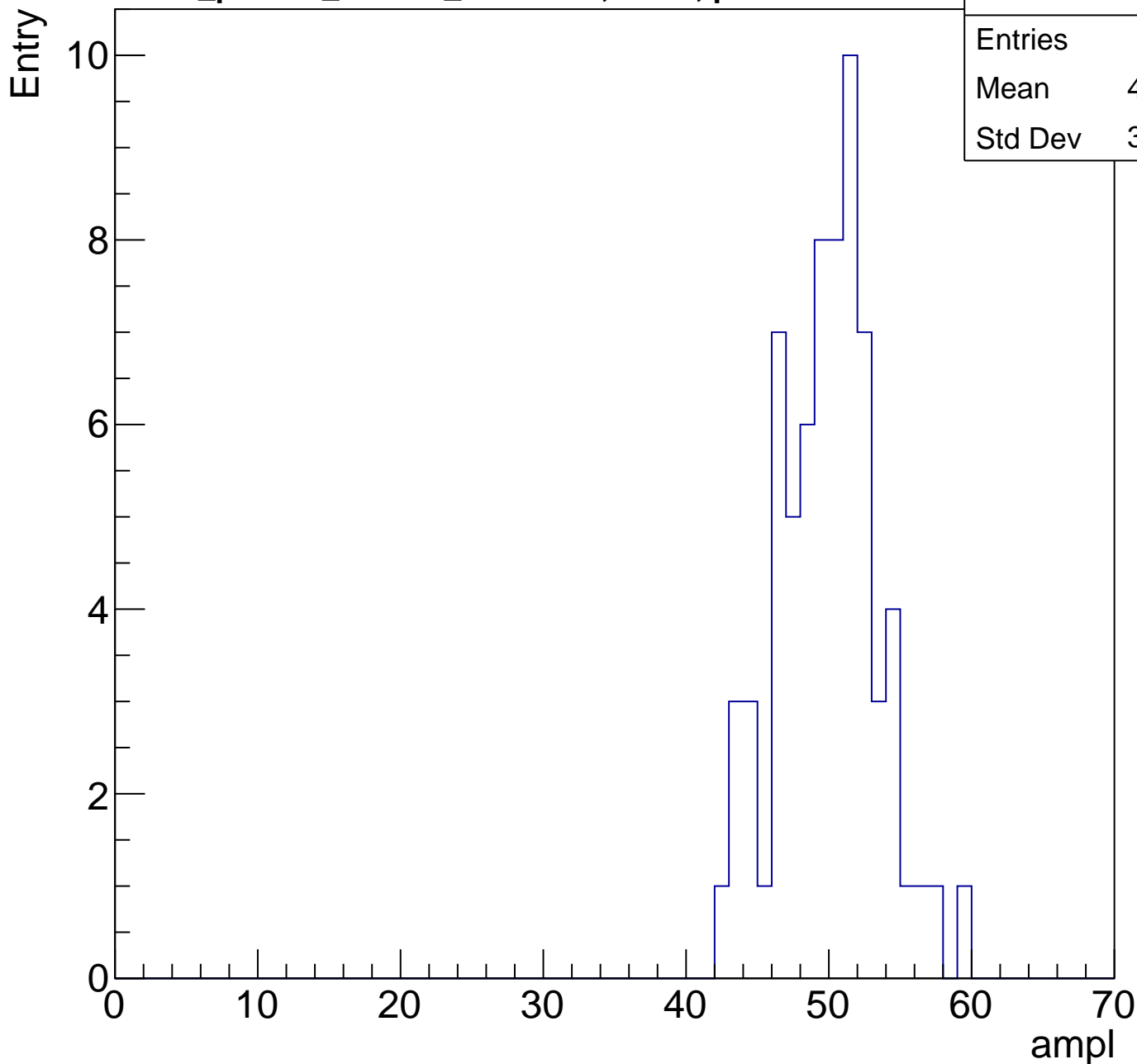
**Gaus Width: 5.4376**



# B1L103S, U11-ch19, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	70
Mean	49.44
Std Dev	3.446

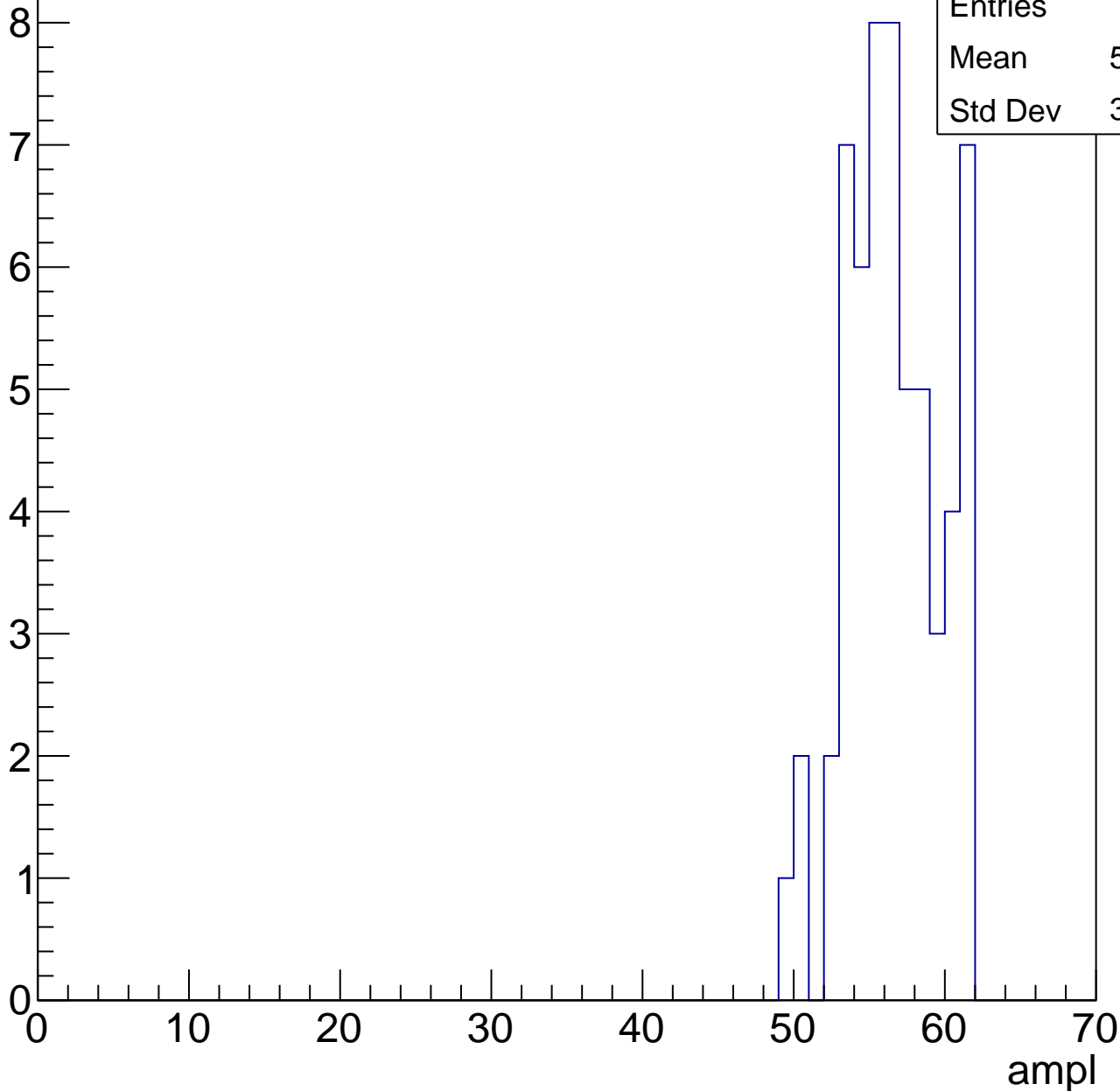


# B1L103S, U11-ch19, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	58
Mean	56.12
Std Dev	3.046

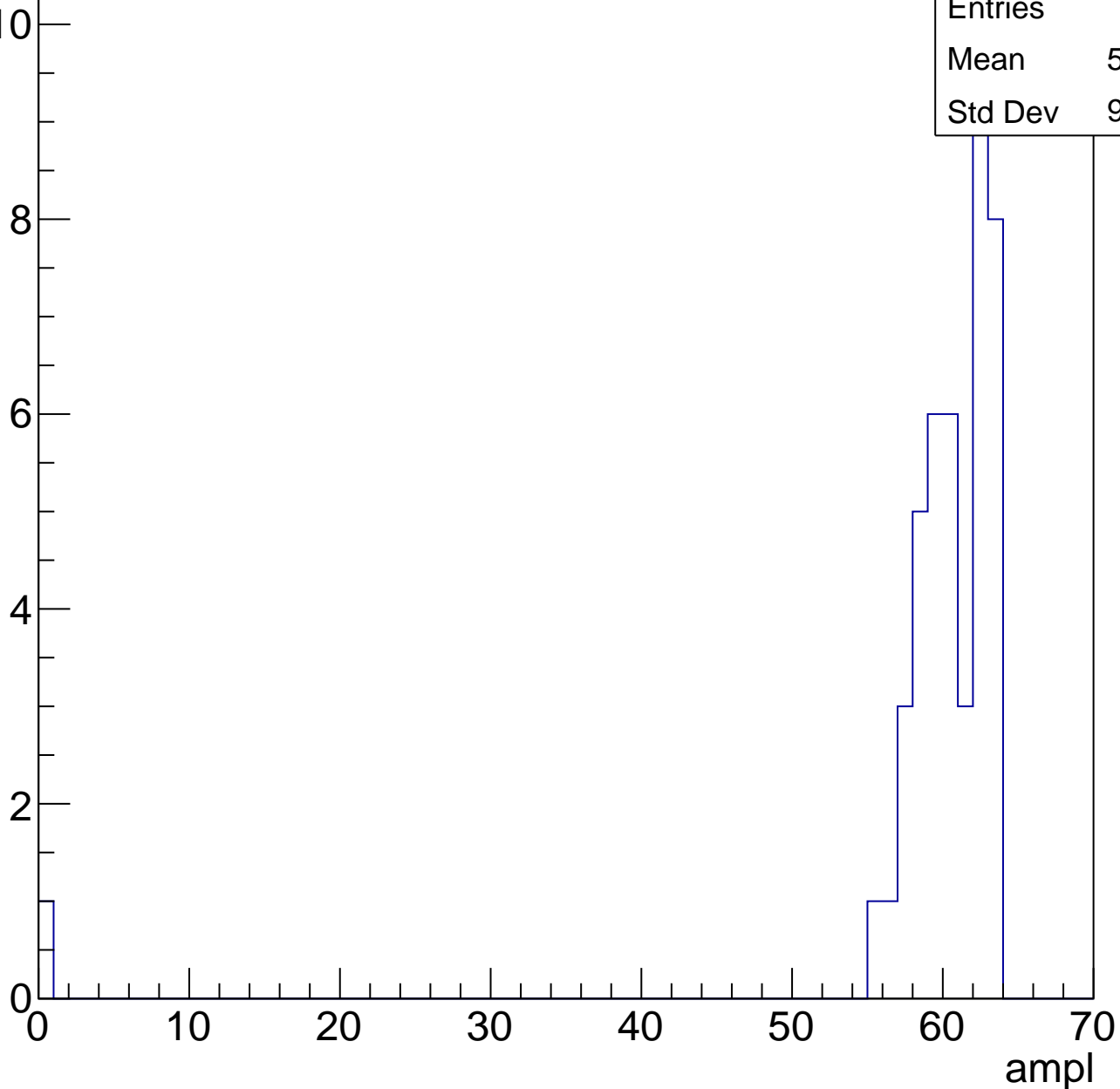


# B1L103S, U11-ch19, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

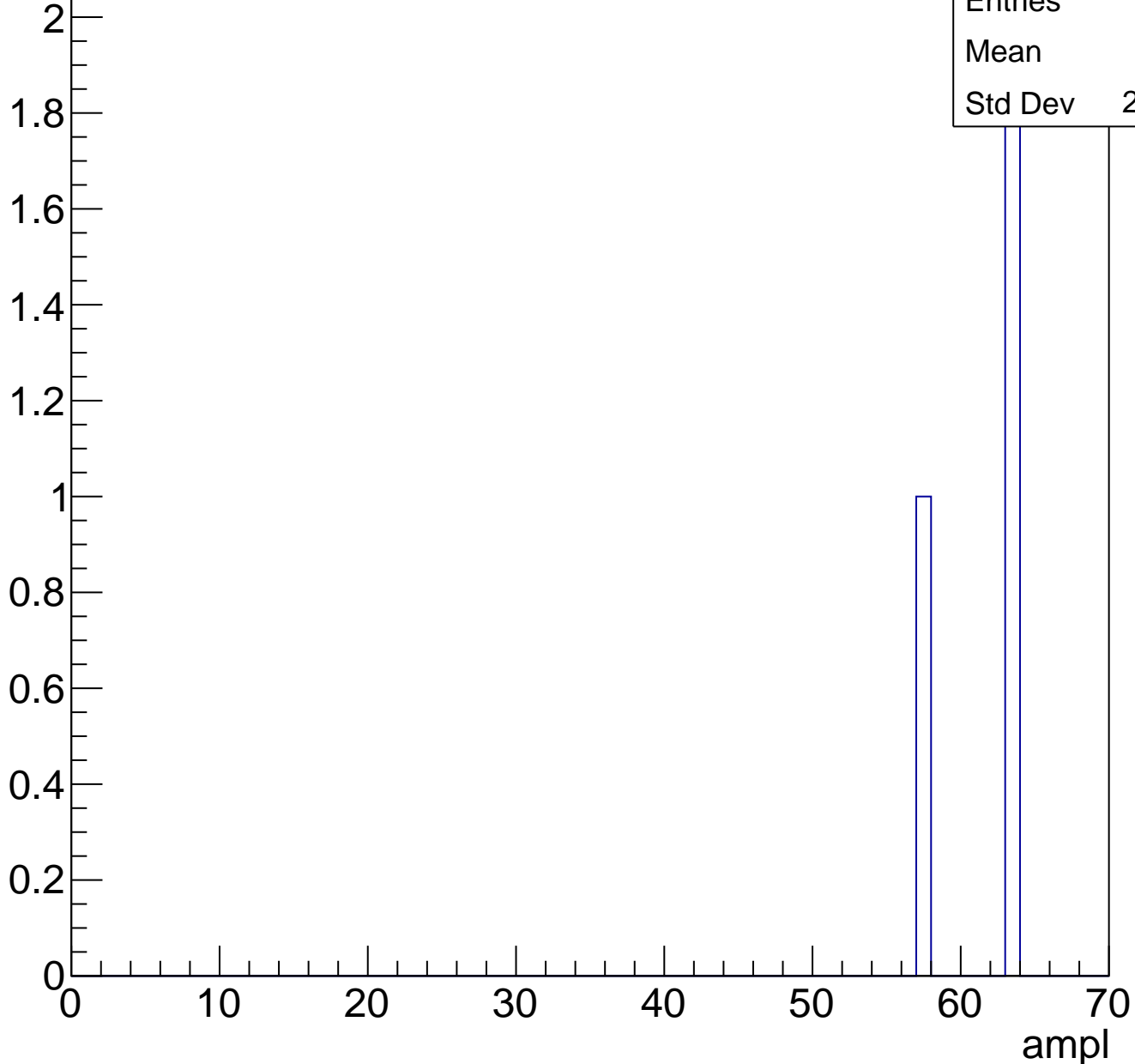
Entries	44
Mean	58.93
Std Dev	9.243



# B1L103S, U11-ch19, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U11-ch19, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U11-ch20, adc0

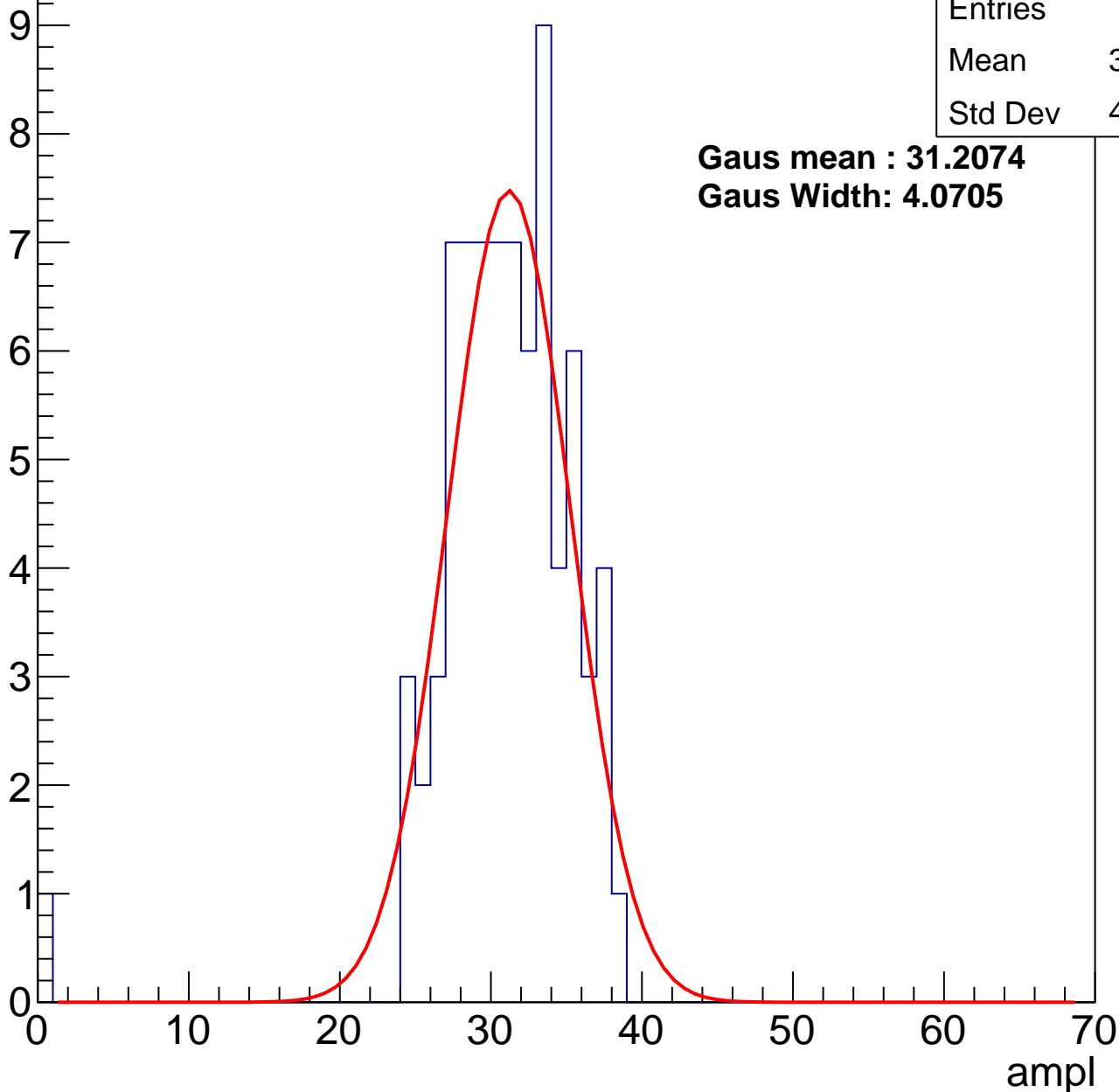
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	77
Mean	30.44
Std Dev	4.945

**Gaus mean : 31.2074**

**Gaus Width: 4.0705**



# B1L103S, U11-ch20, adc1

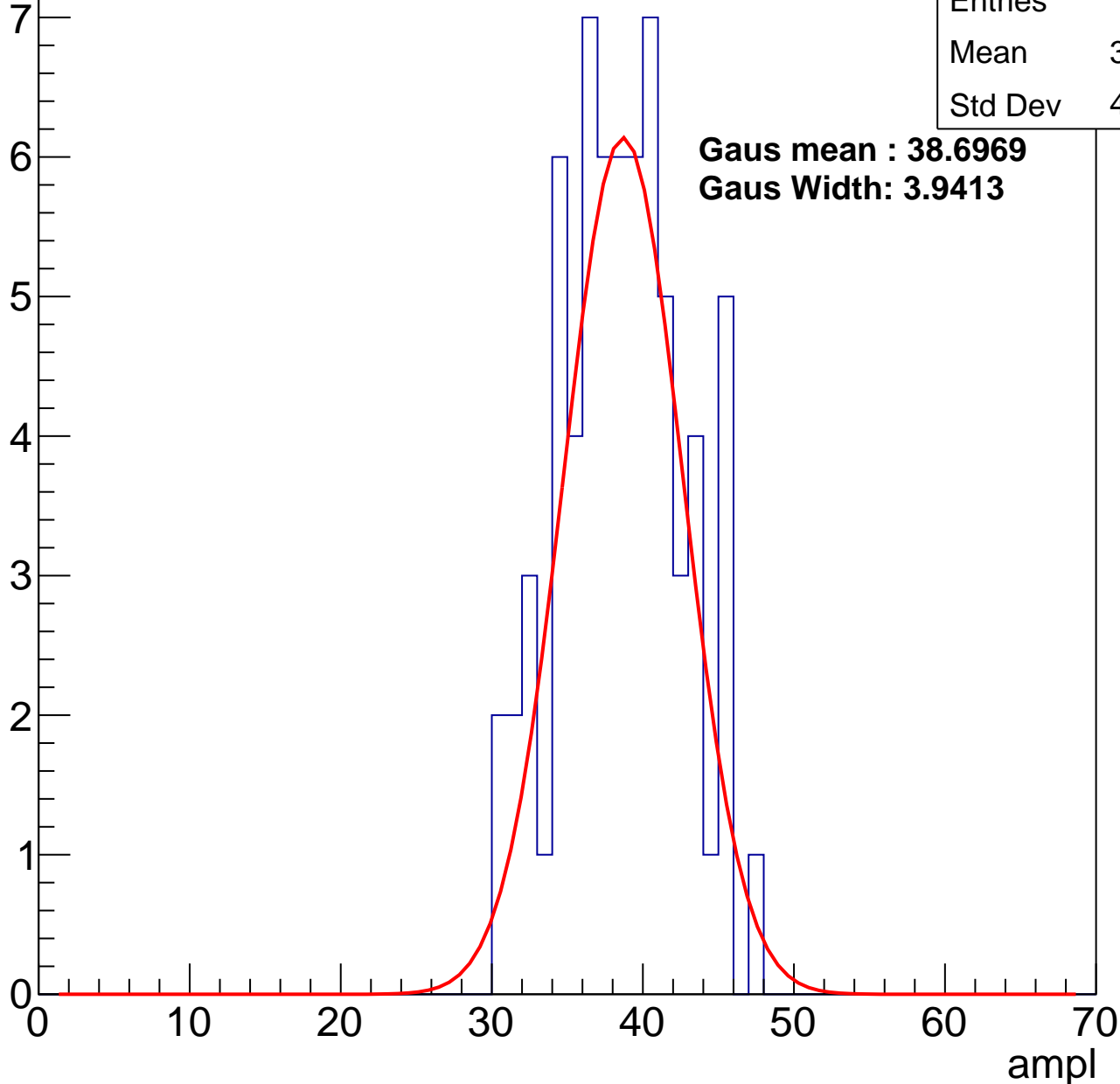
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	69
Mean	38.12
Std Dev	4.016

**Gaus mean : 38.6969**

**Gaus Width: 3.9413**



# B1L103S, U11-ch20, adc2

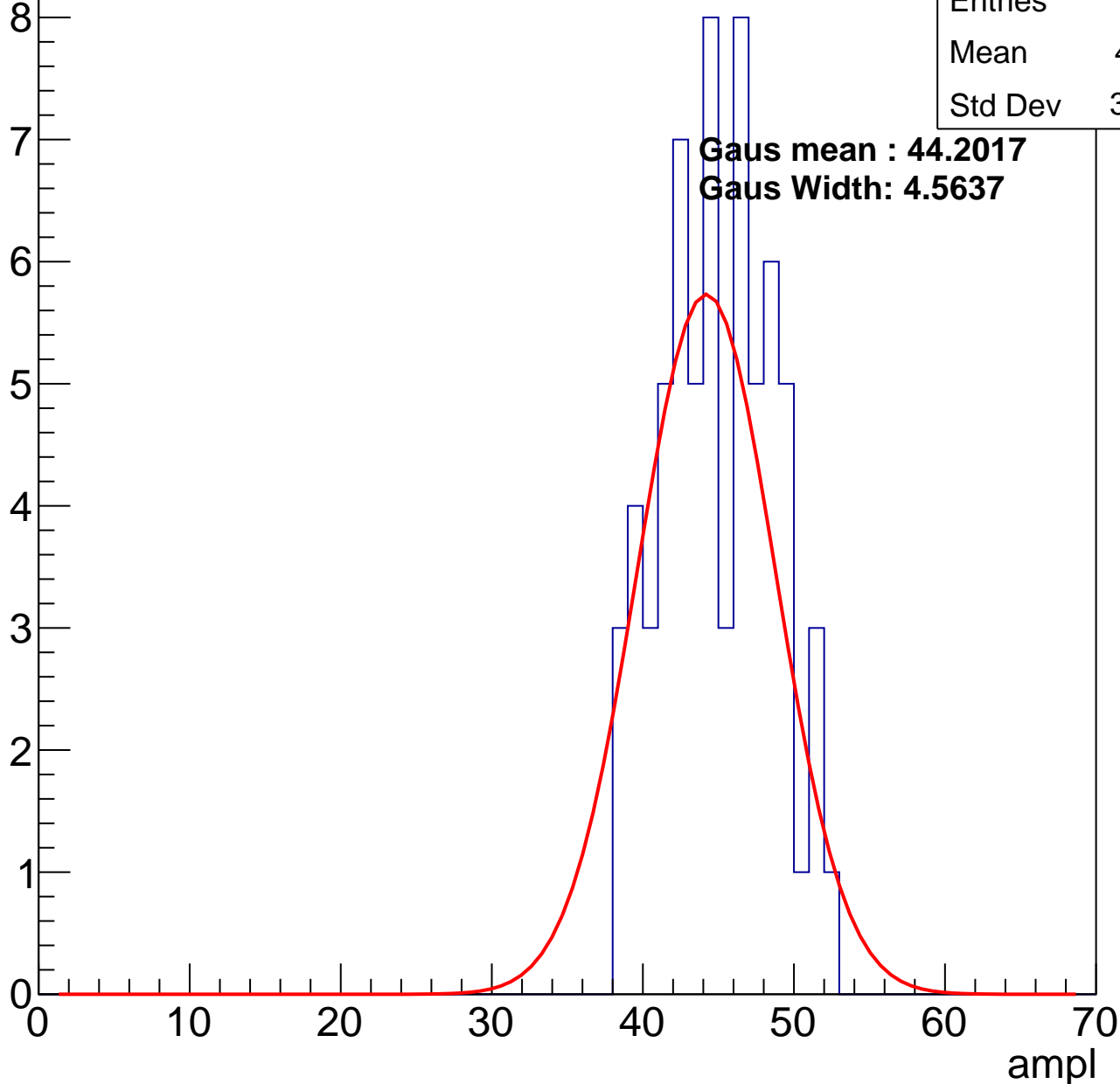
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	44.51
Std Dev	3.593

**Gaus mean : 44.2017**

**Gaus Width: 4.5637**

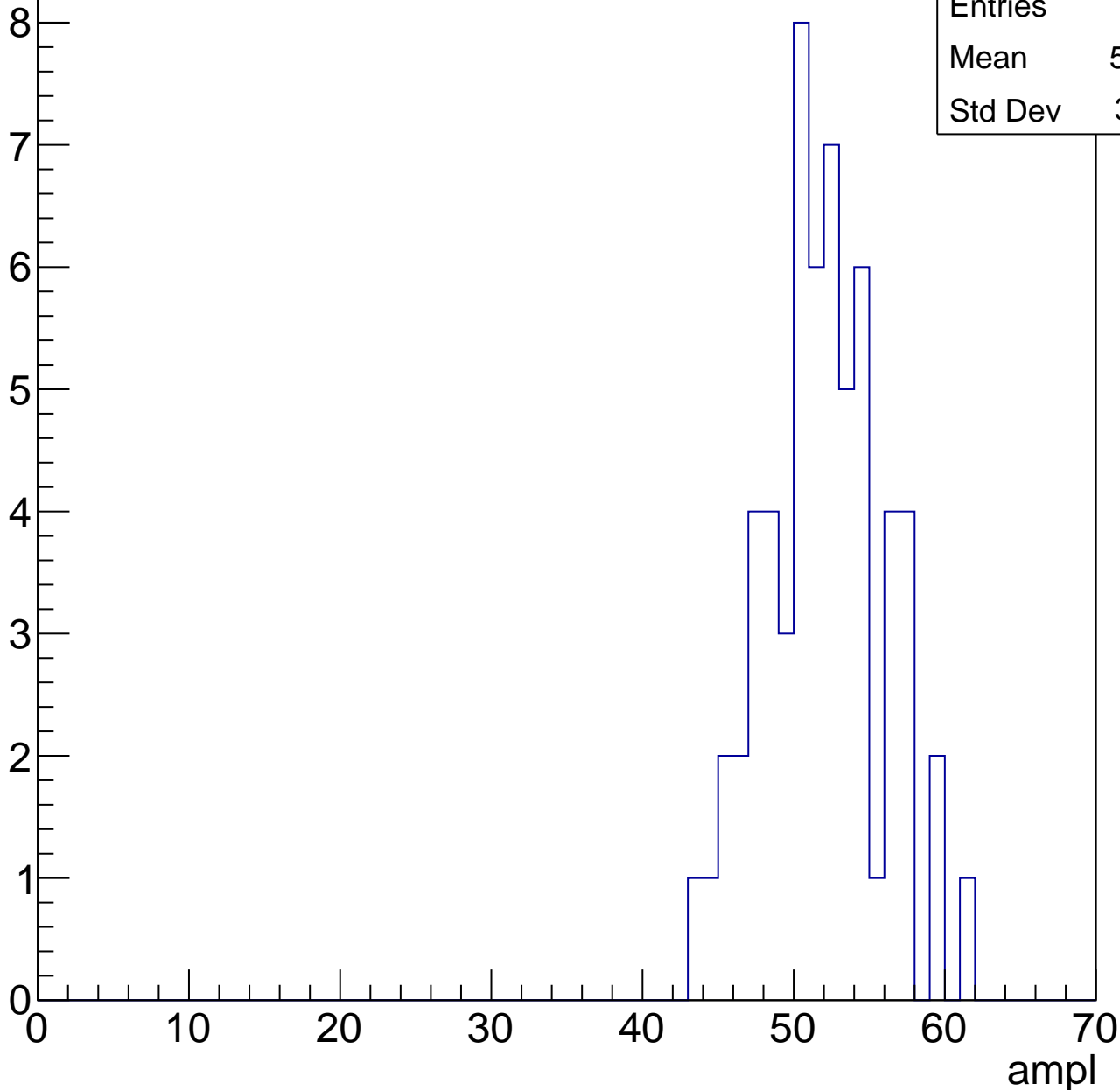


# B1L103S, U11-ch20, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	61
Mean	51.49
Std Dev	3.861

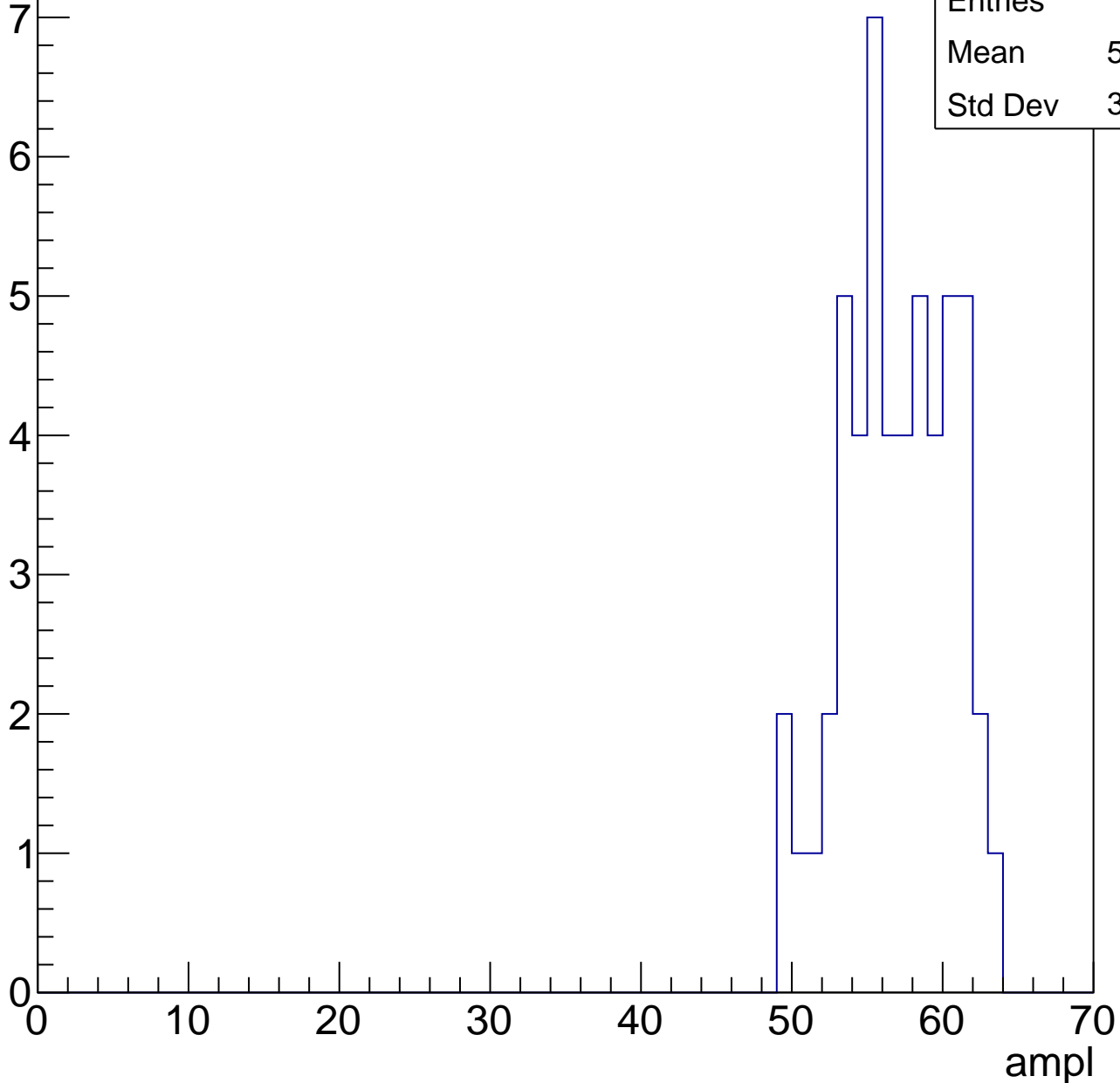


# B1L103S, U11-ch20, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	52
Mean	56.52
Std Dev	3.483

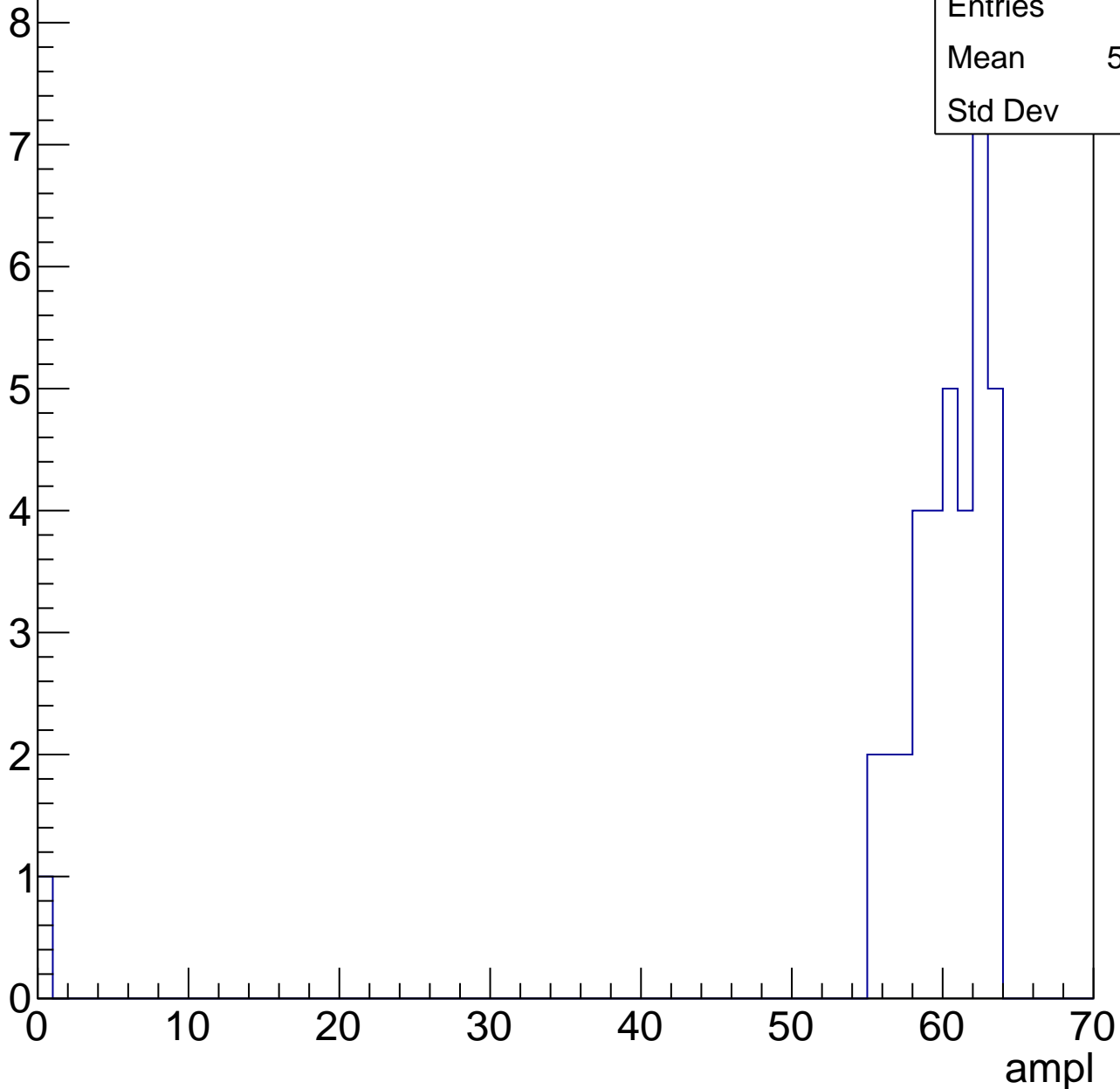


# B1L103S, U11-ch20, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

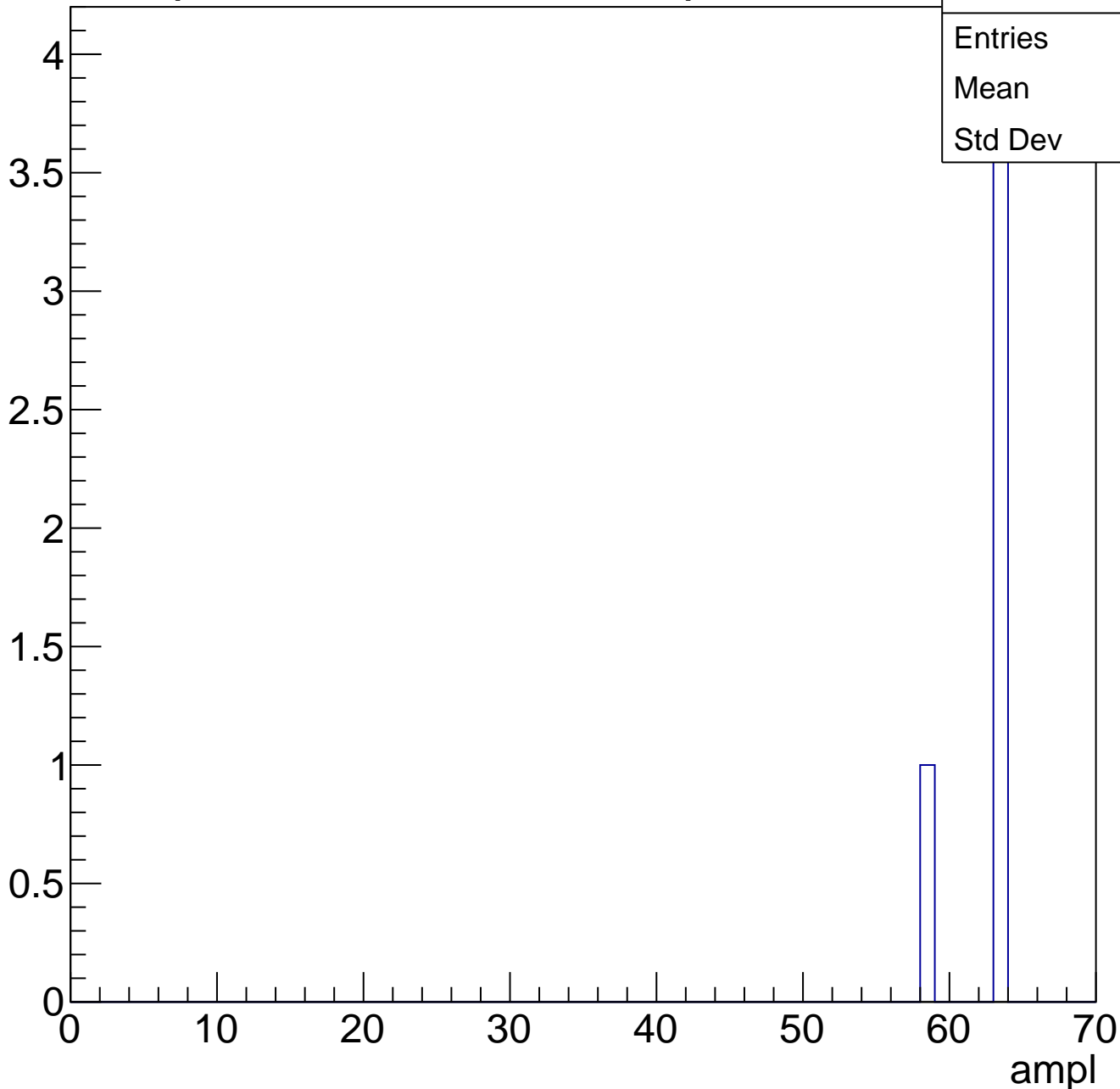
Entries	37
Mean	58.35
Std Dev	10



# B1L103S, U11-ch20, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U11-ch20, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U11-ch21, adc0

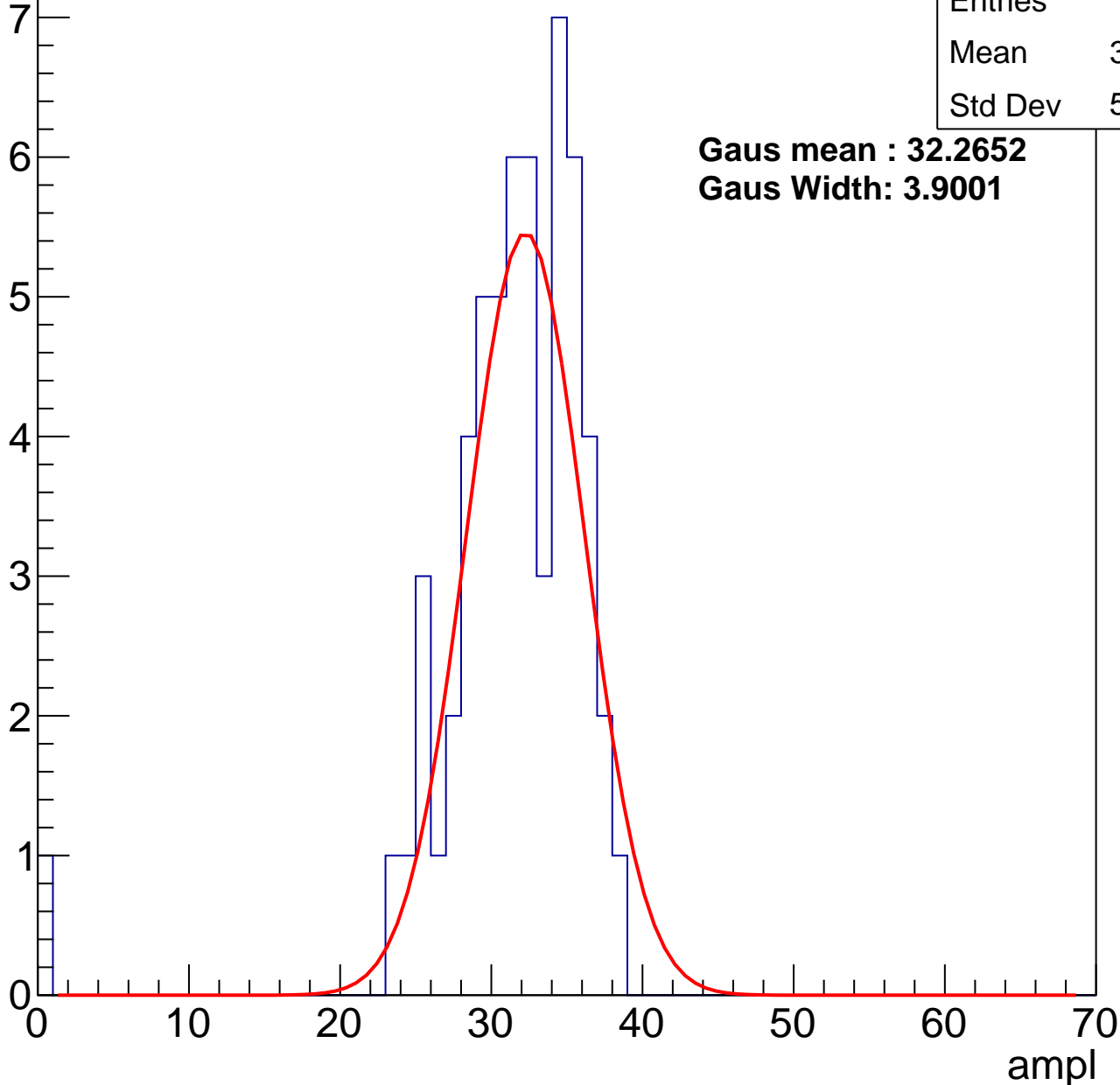
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	58
Mean	30.86
Std Dev	5.409

**Gaus mean : 32.2652**

**Gaus Width: 3.9001**



# B1L103S, U11-ch21, adc1

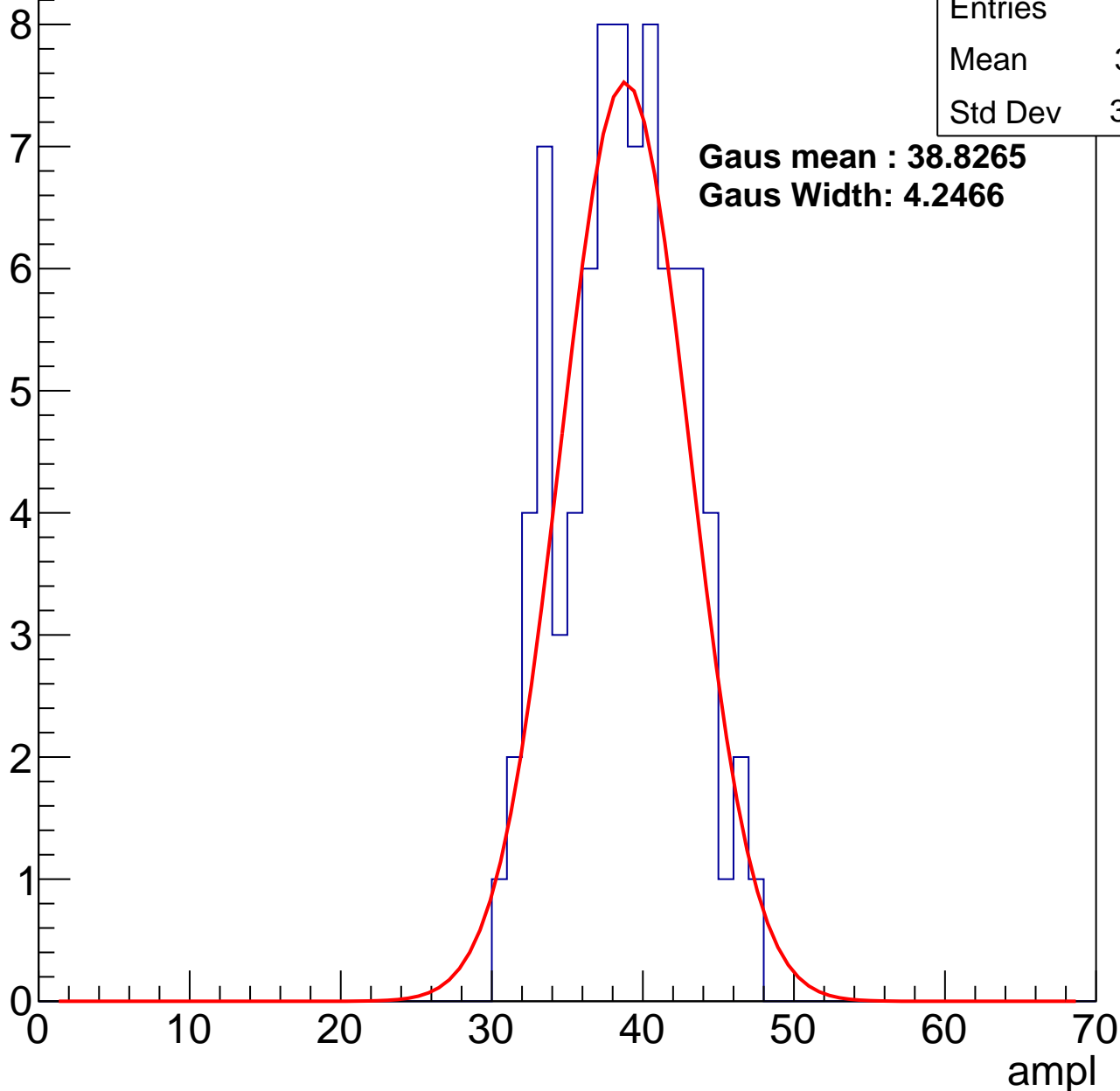
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	84
Mean	38.31
Std Dev	3.979

**Gaus mean : 38.8265**

**Gaus Width: 4.2466**



# B1L103S, U11-ch21, adc2

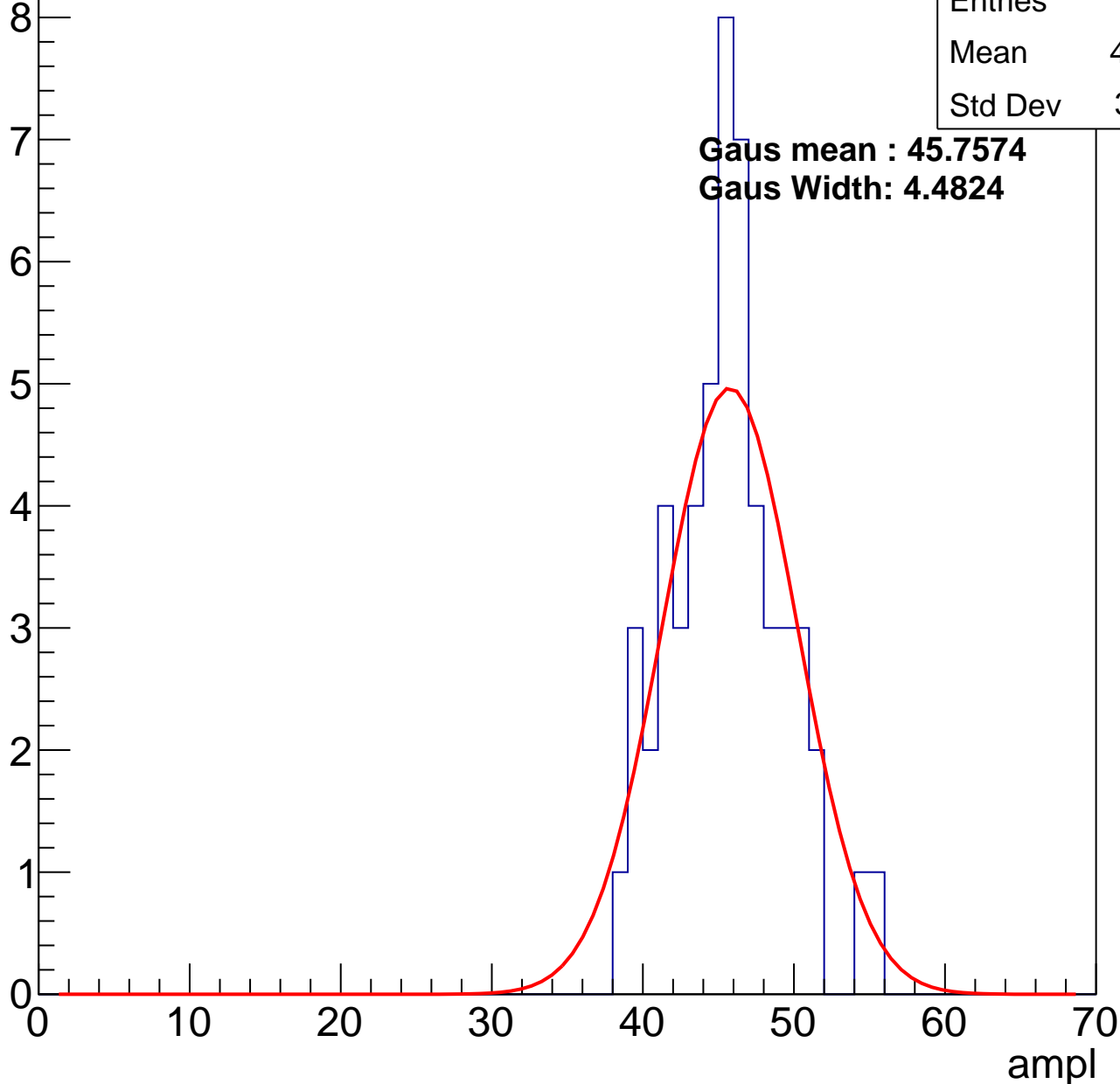
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	54
Mean	45.17
Std Dev	3.711

**Gaus mean : 45.7574**

**Gaus Width: 4.4824**

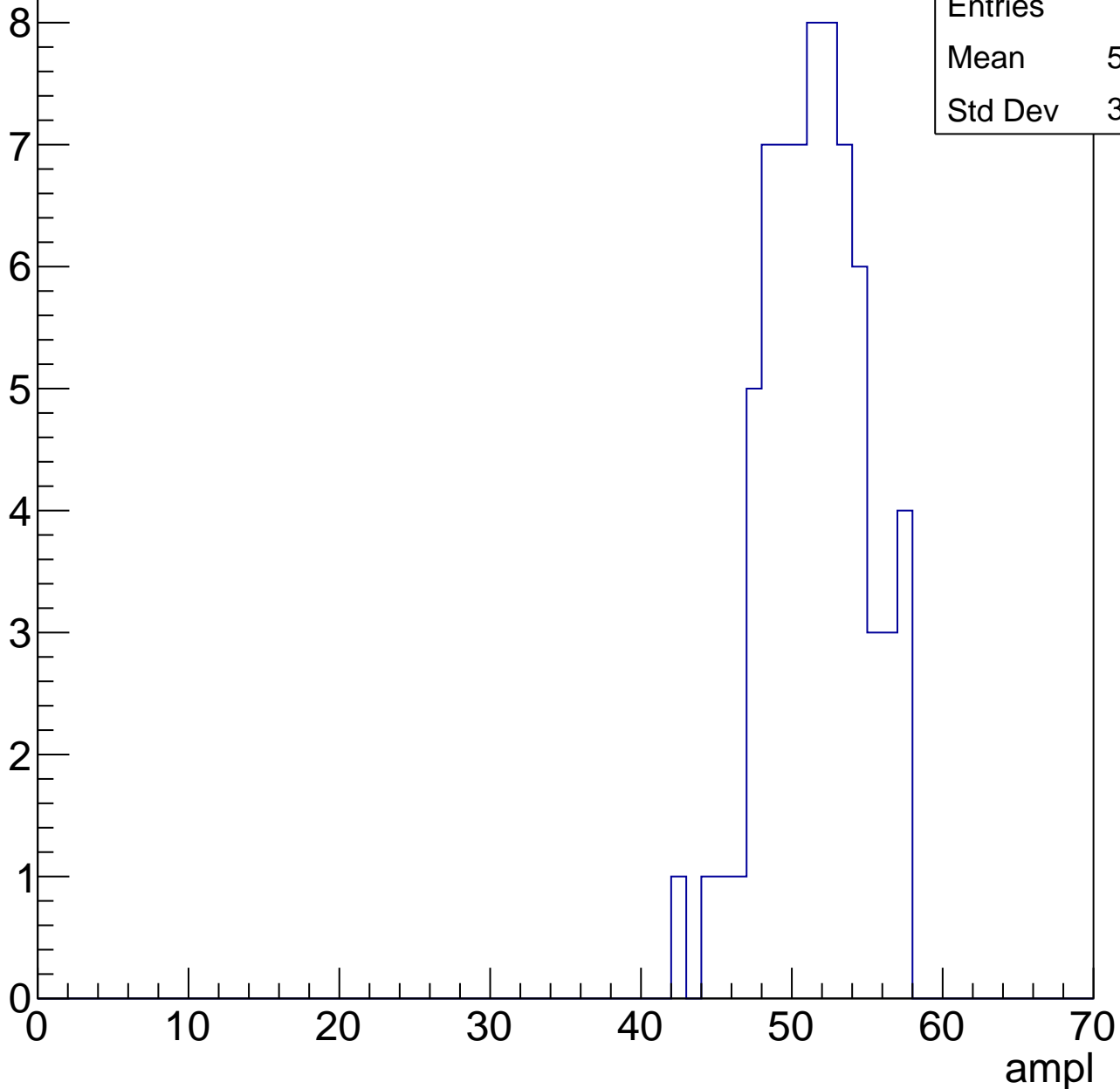


# B1L103S, U11-ch21, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	69
Mean	51.03
Std Dev	3.244

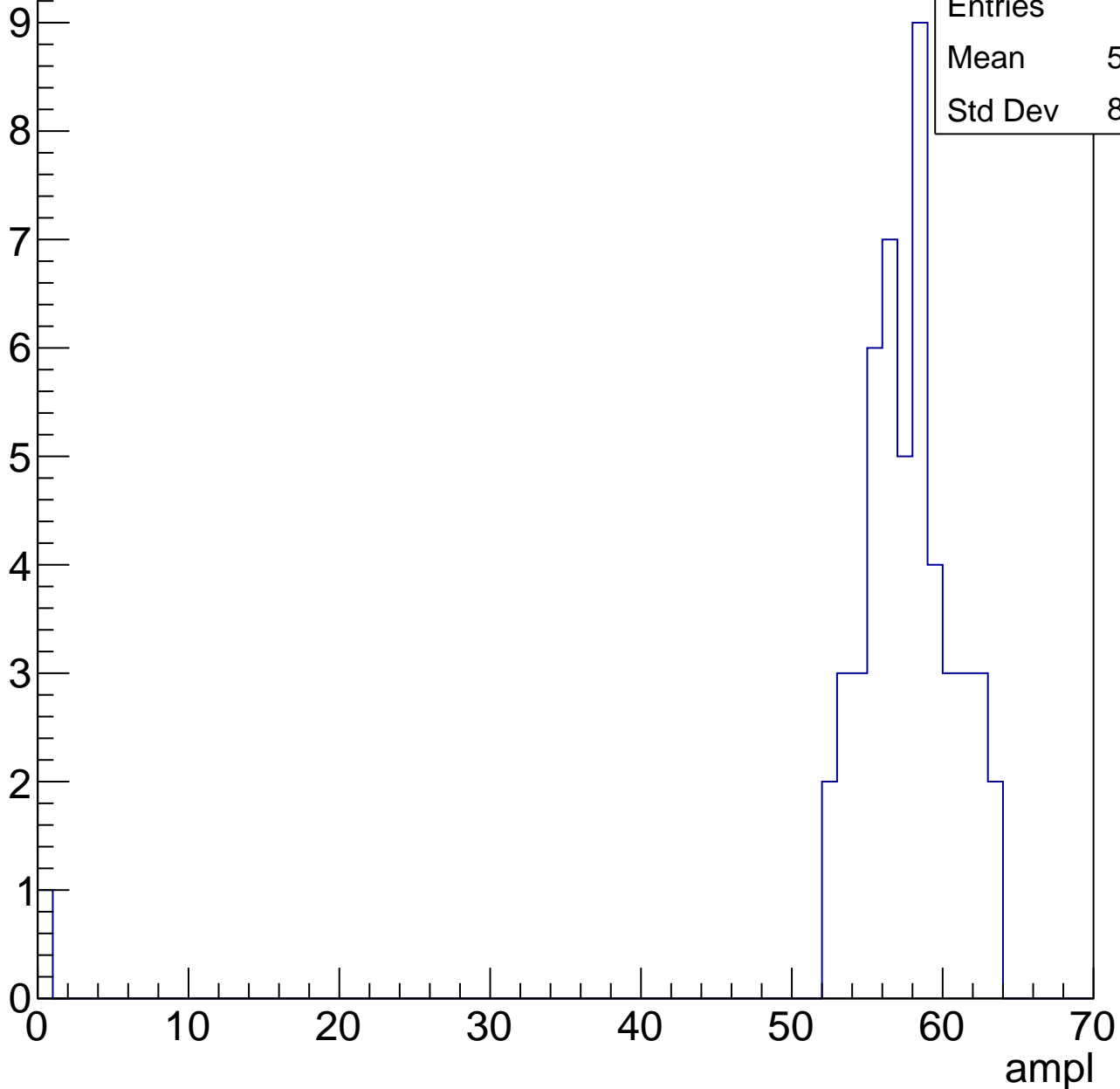


# B1L103S, U11-ch21, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

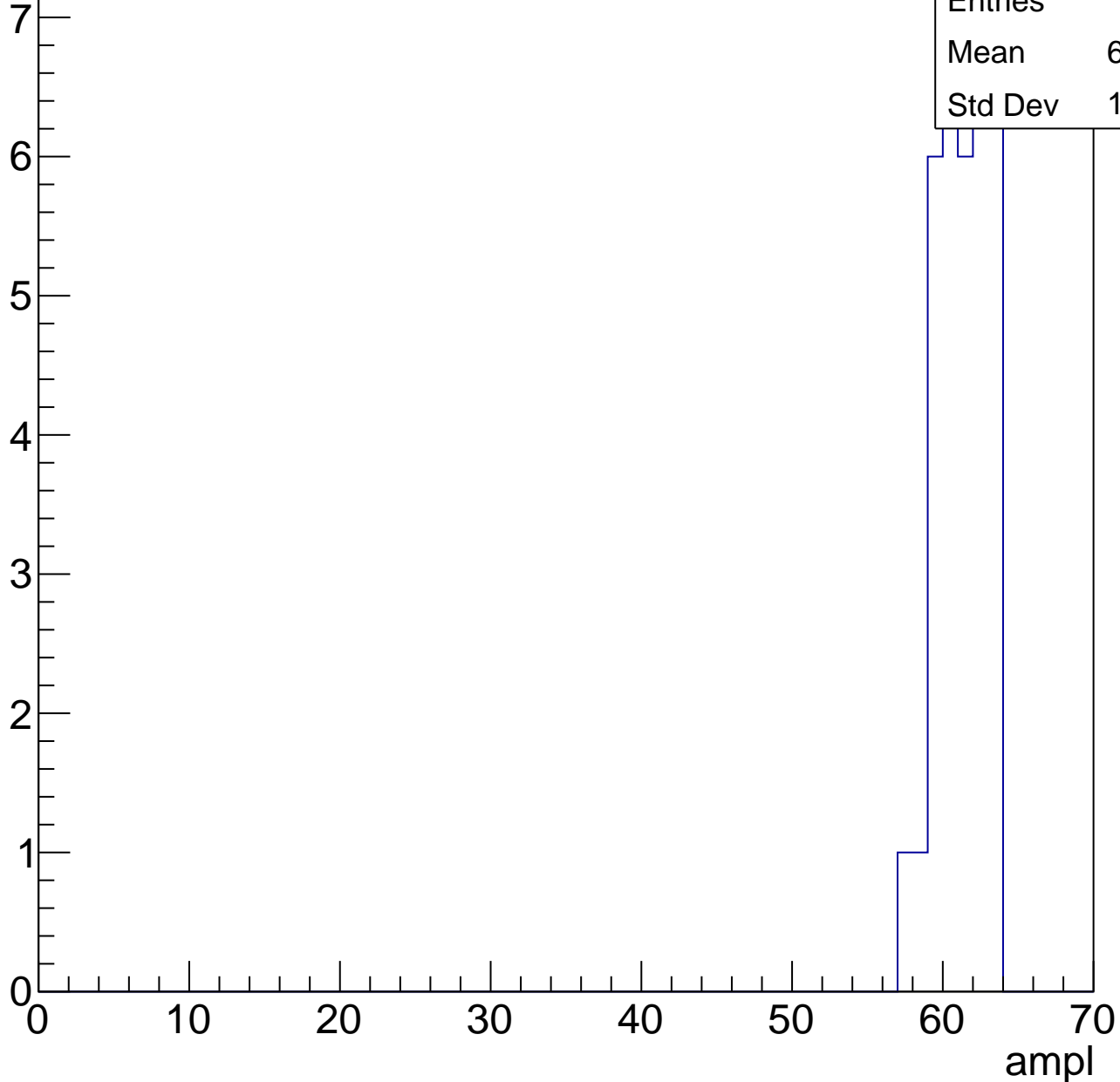
Entries	51
Mean	56.18
Std Dev	8.422



# B1L103S, U11-ch21, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

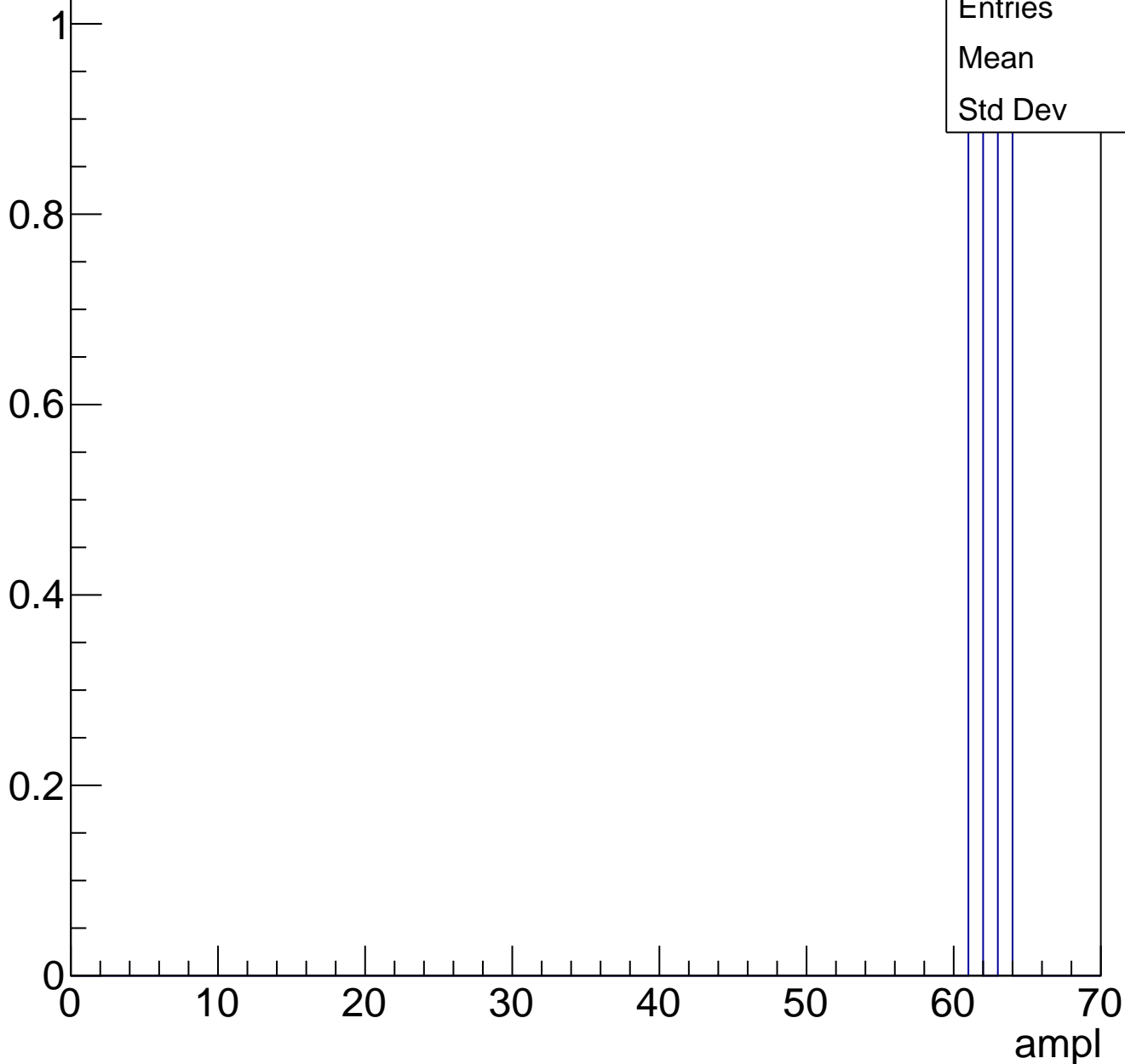
Entry



# B1L103S, U11-ch21, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U11-ch21, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U11-ch22, adc0

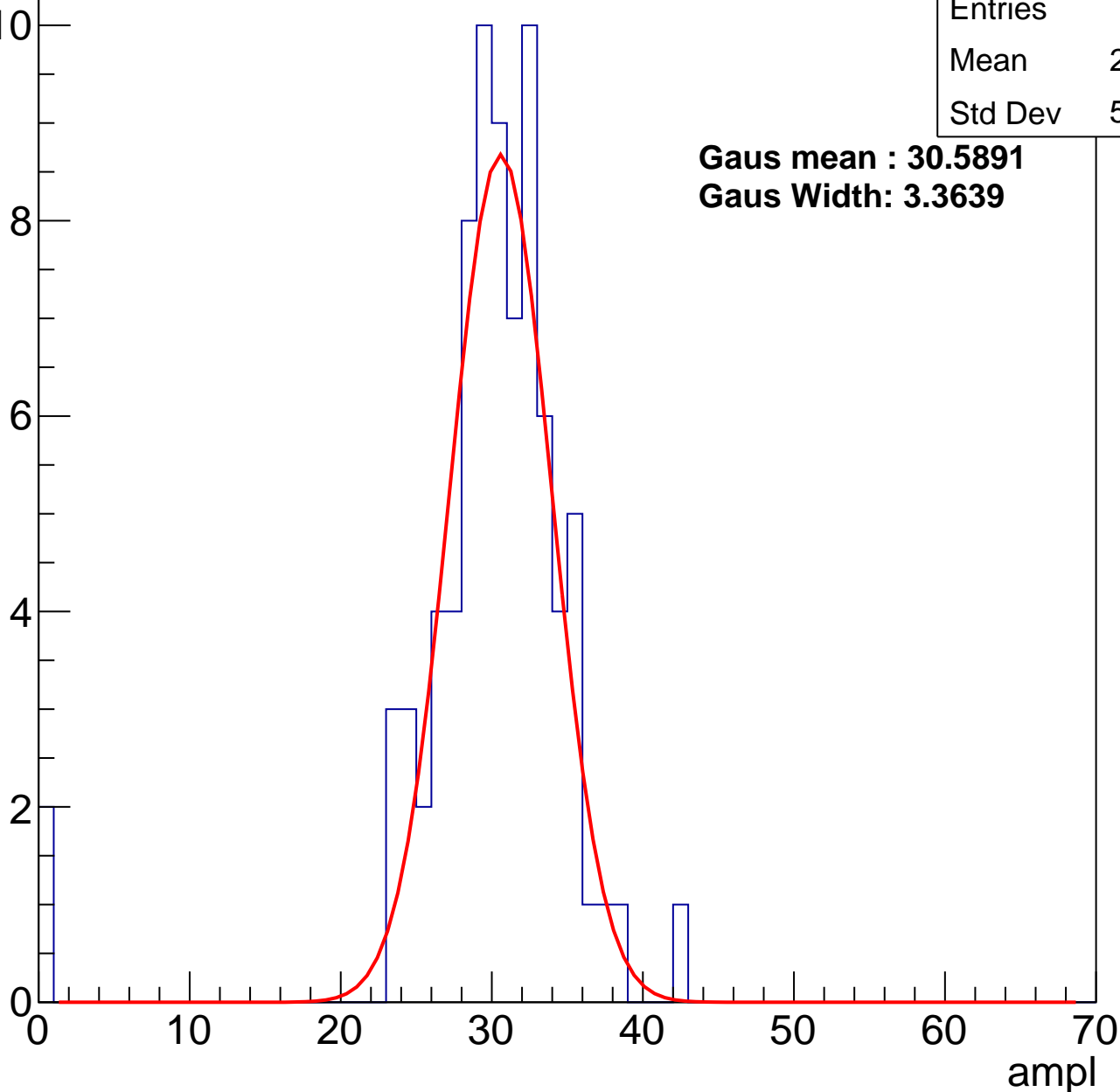
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	81
Mean	29.46
Std Dev	5.886

**Gaus mean : 30.5891**

**Gaus Width: 3.3639**



# B1L103S, U11-ch22, adc1

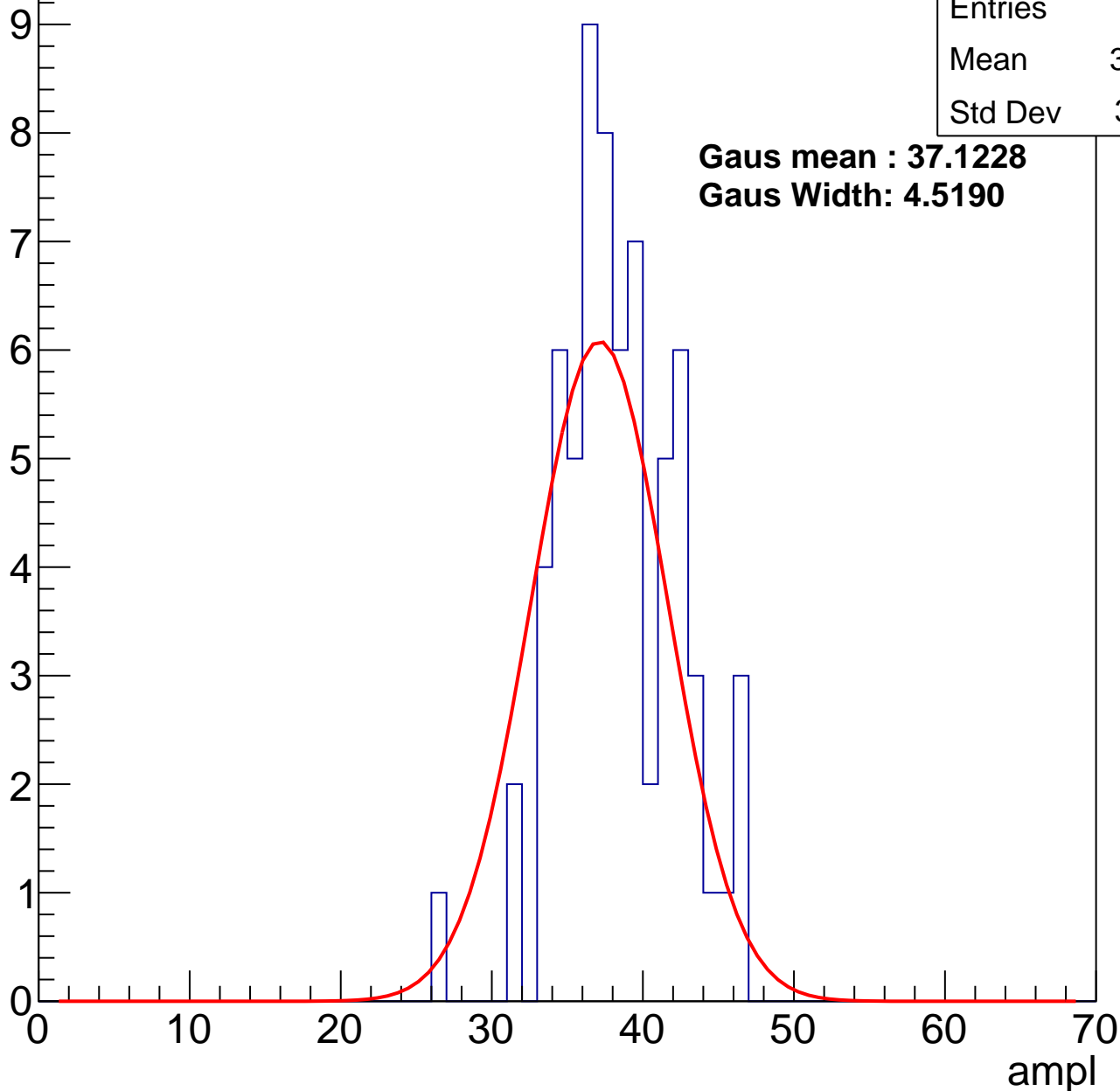
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	69
Mean	37.87
Std Dev	3.871

**Gaus mean : 37.1228**

**Gaus Width: 4.5190**



# B1L103S, U11-ch22, adc2

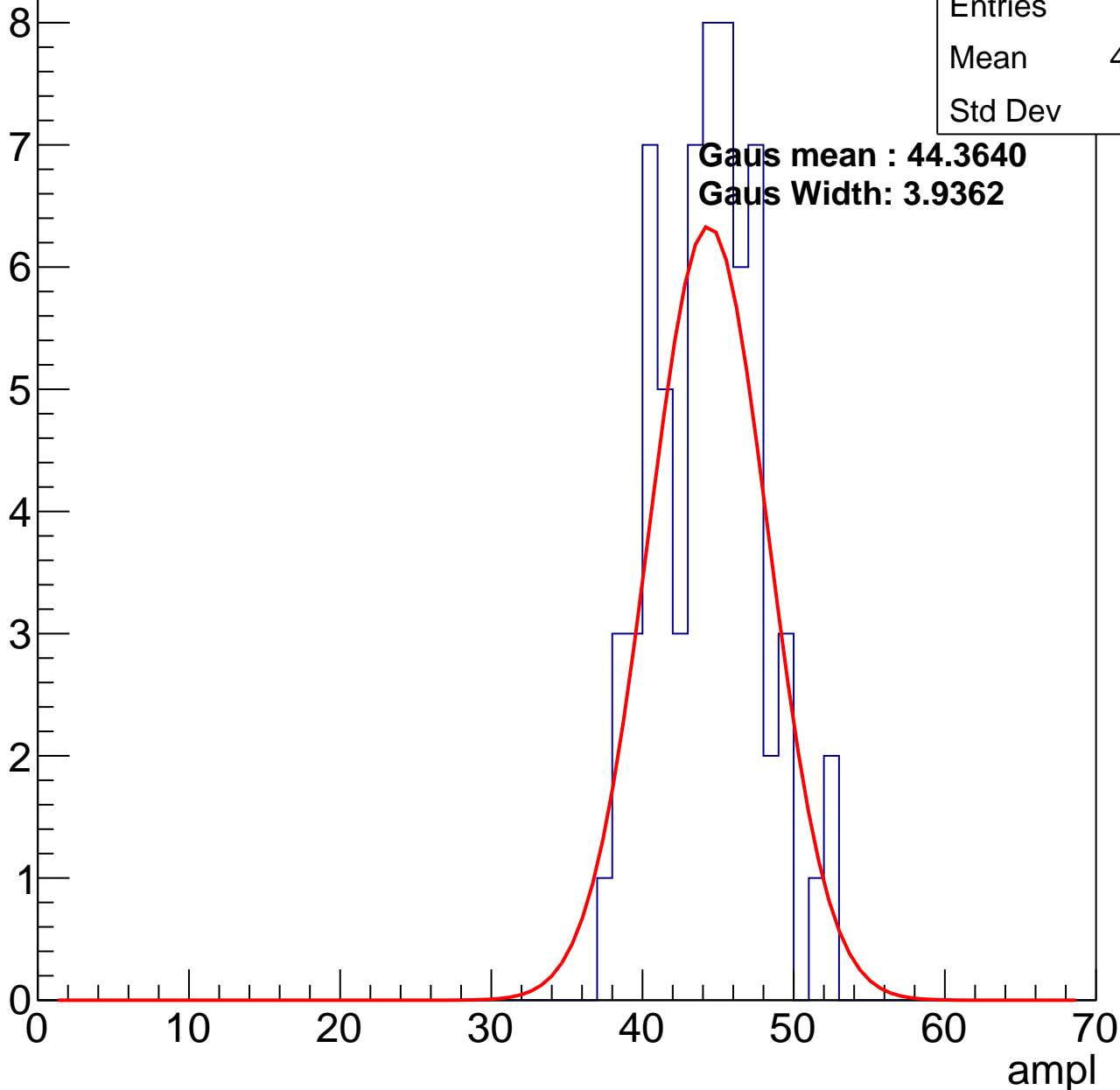
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	43.86
Std Dev	3.45

**Gaus mean : 44.3640**

**Gaus Width: 3.9362**

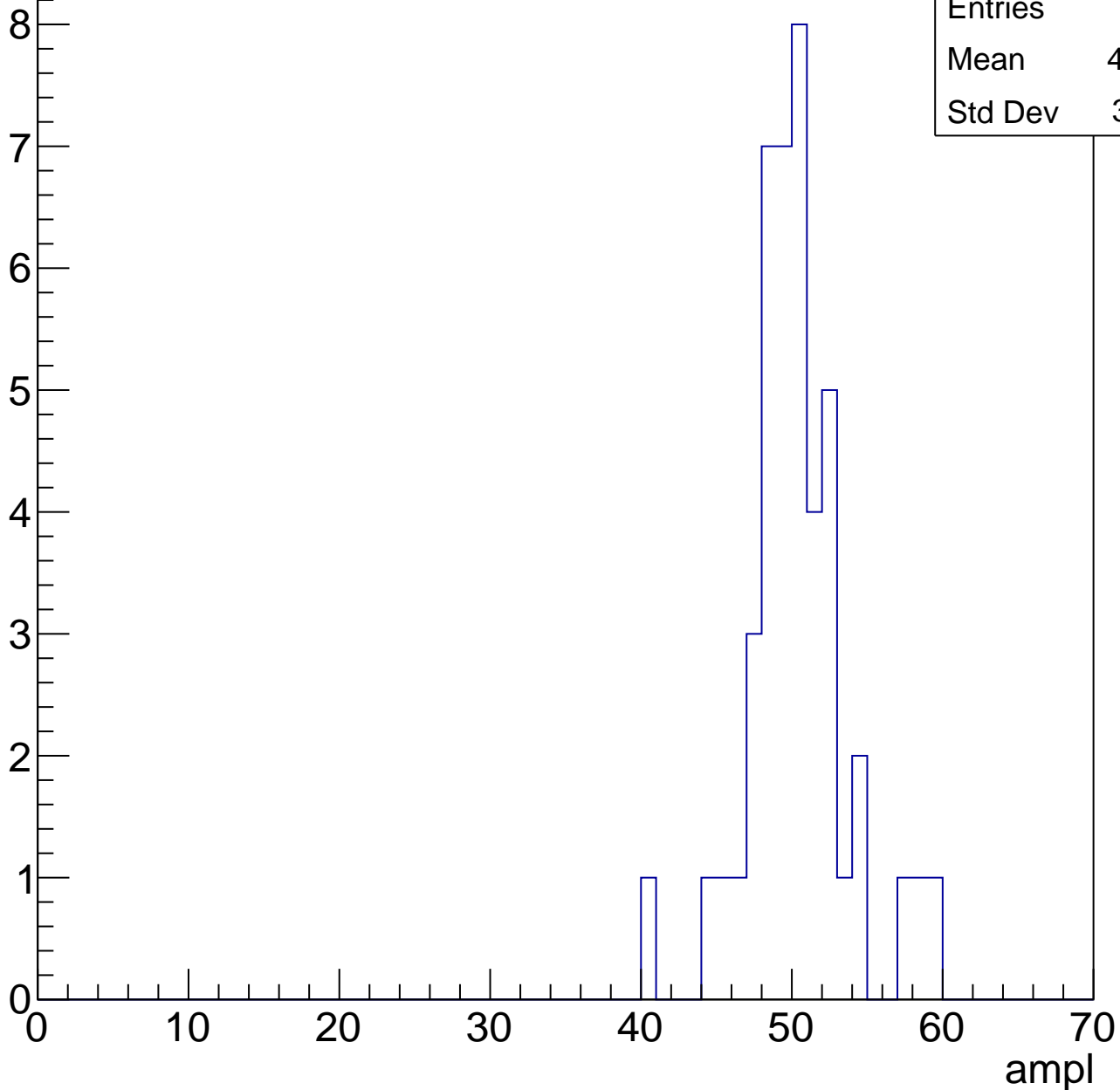


# B1L103S, U11-ch22, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	44
Mean	49.86
Std Dev	3.361

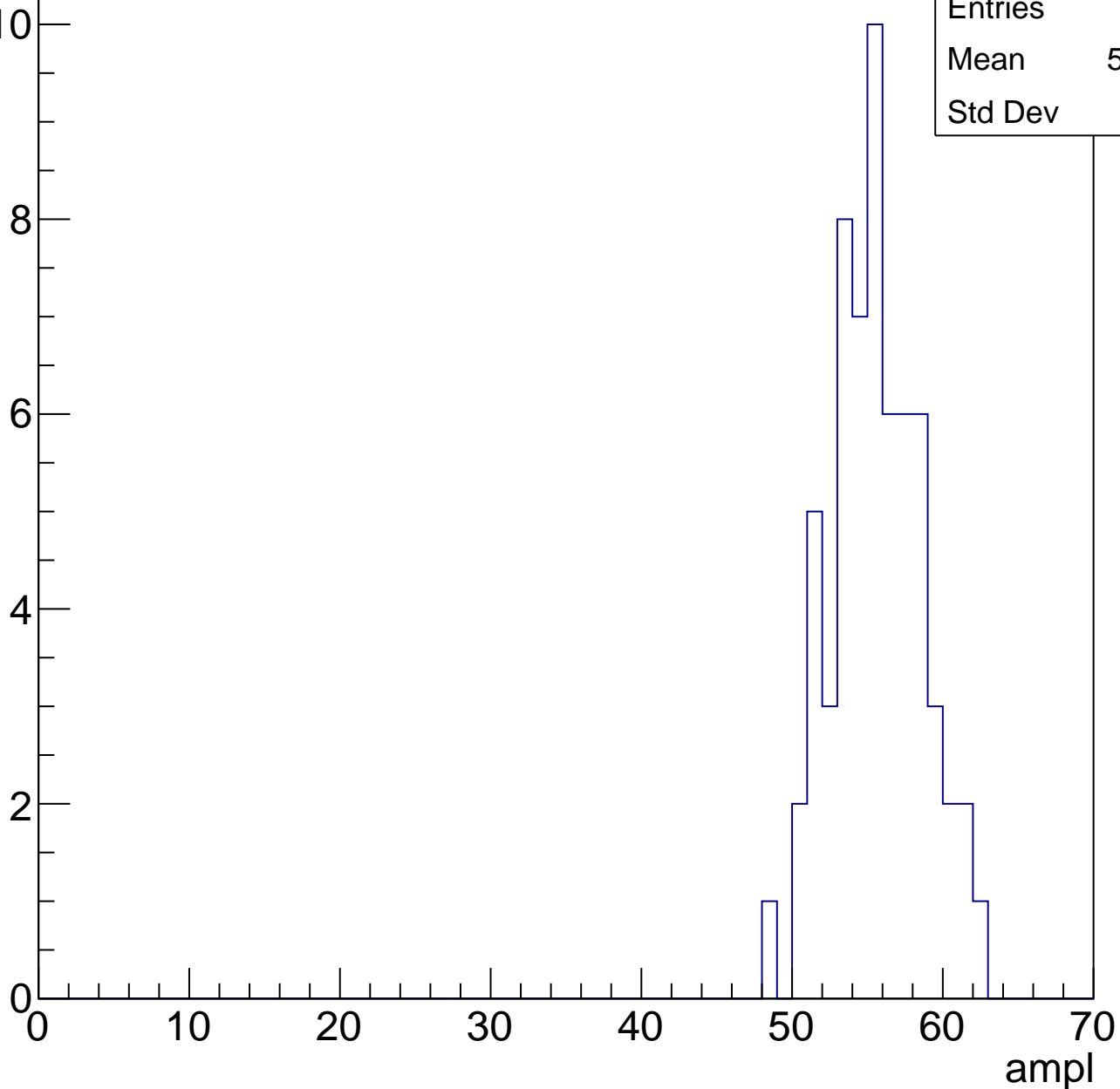


# B1L103S, U11-ch22, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	55.13
Std Dev	2.97

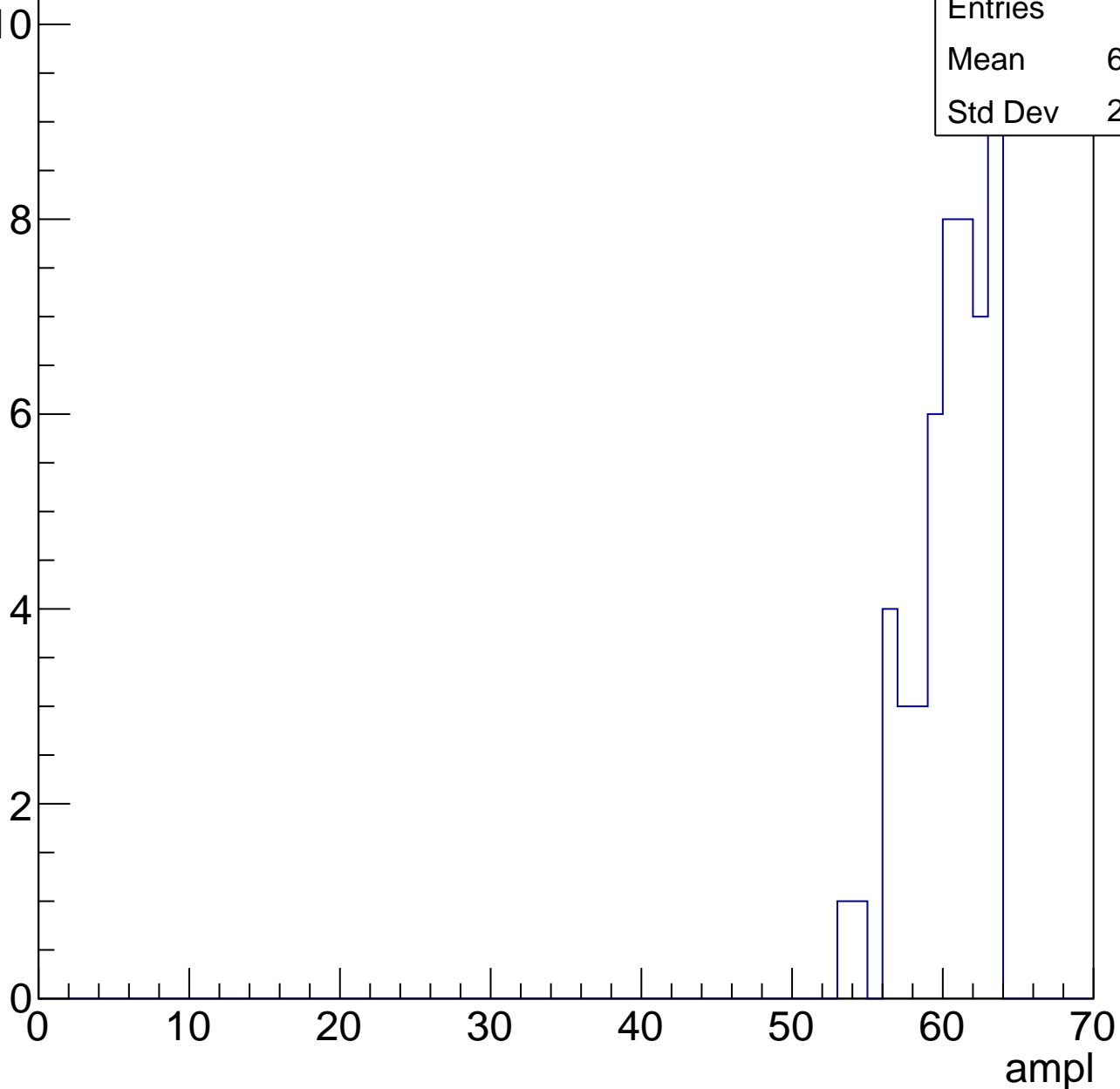


# B1L103S, U11-ch22, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	51
Mean	60.04
Std Dev	2.505



# B1L103S, U11-ch22, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U11-ch22, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U11-ch23, adc0

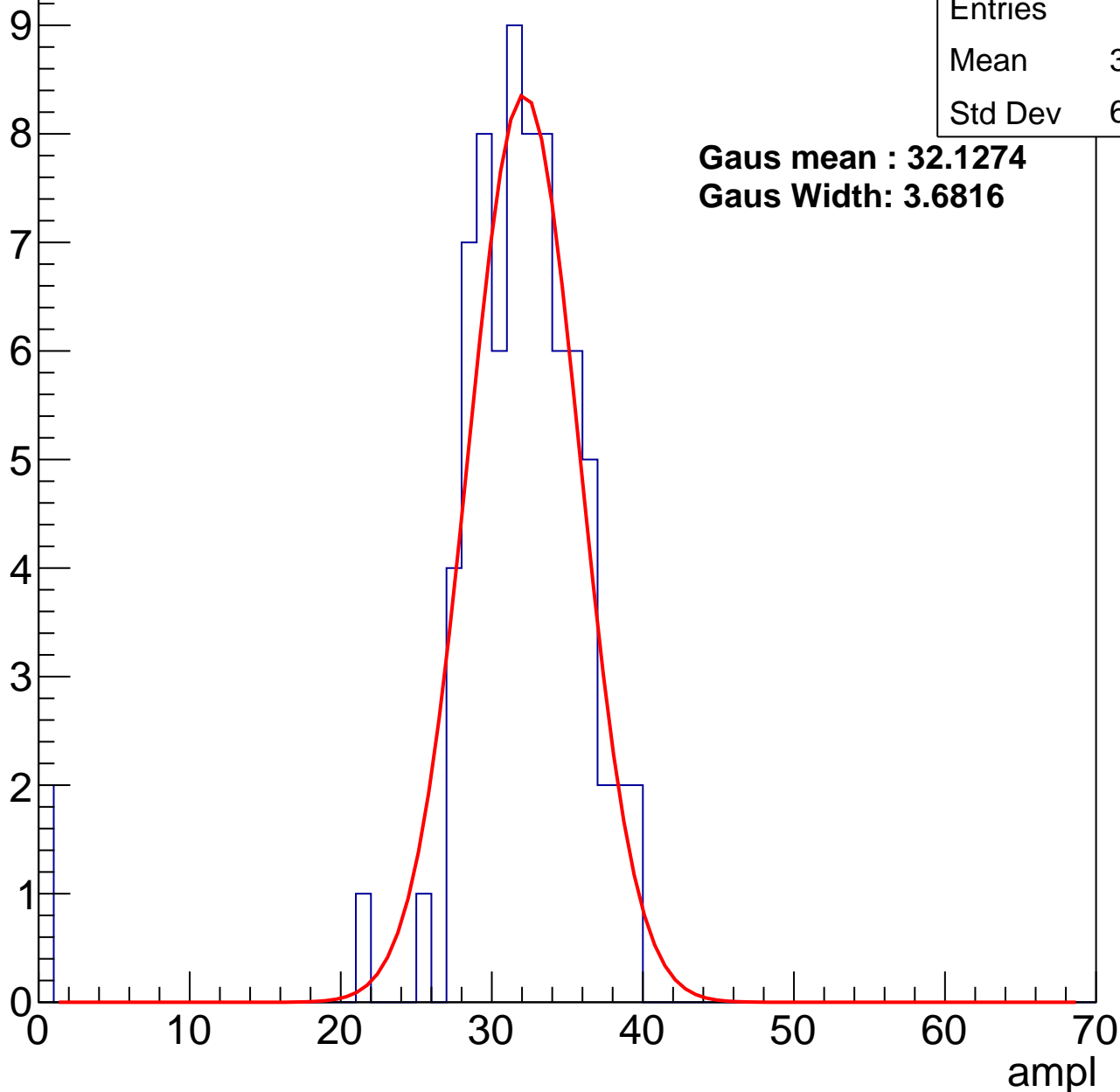
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	77
Mean	30.95
Std Dev	6.069

**Gaus mean : 32.1274**

**Gaus Width: 3.6816**



# B1L103S, U11-ch23, adc1

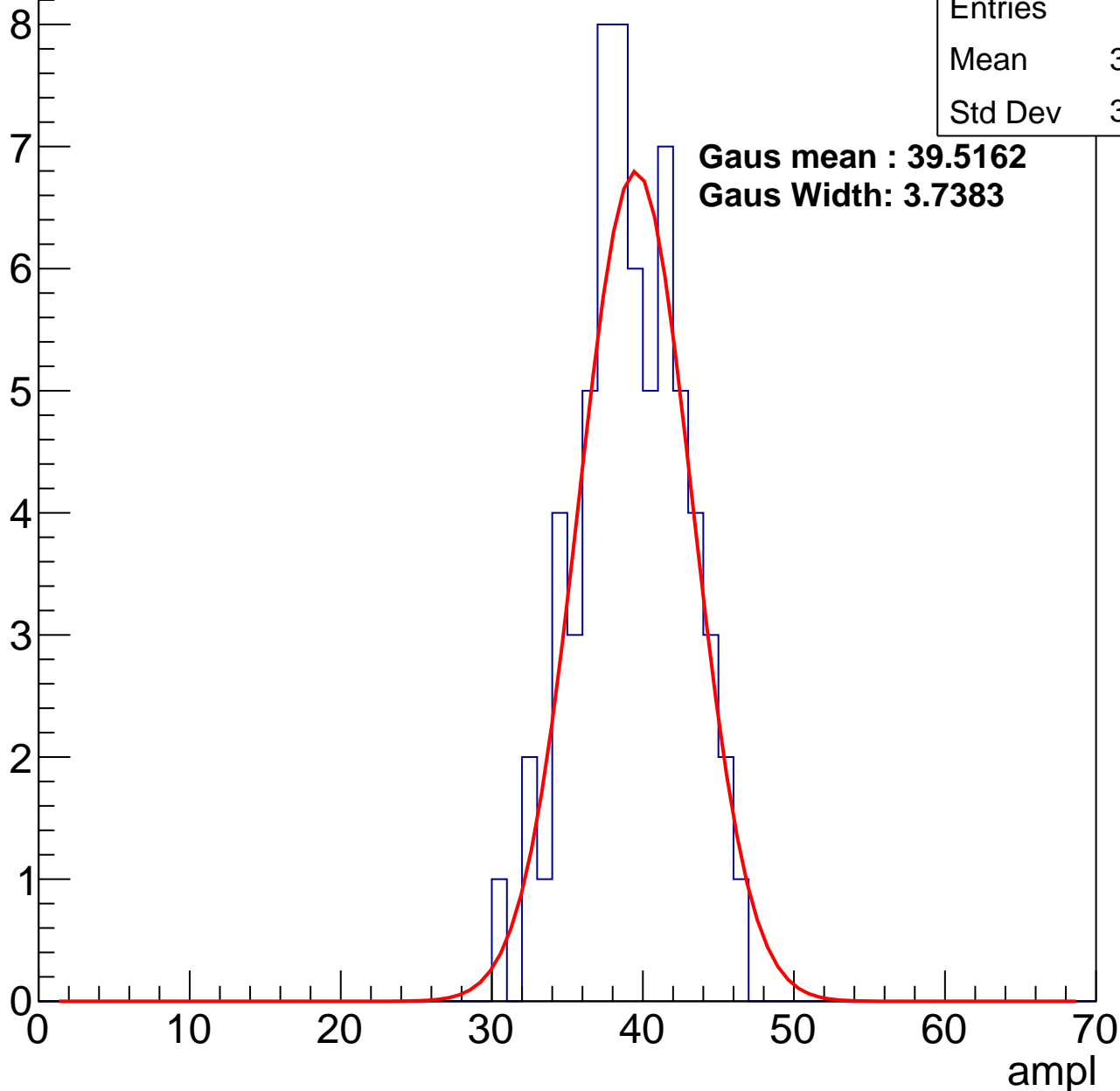
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	38.75
Std Dev	3.469

**Gaus mean : 39.5162**

**Gaus Width: 3.7383**



# B1L103S, U11-ch23, adc2

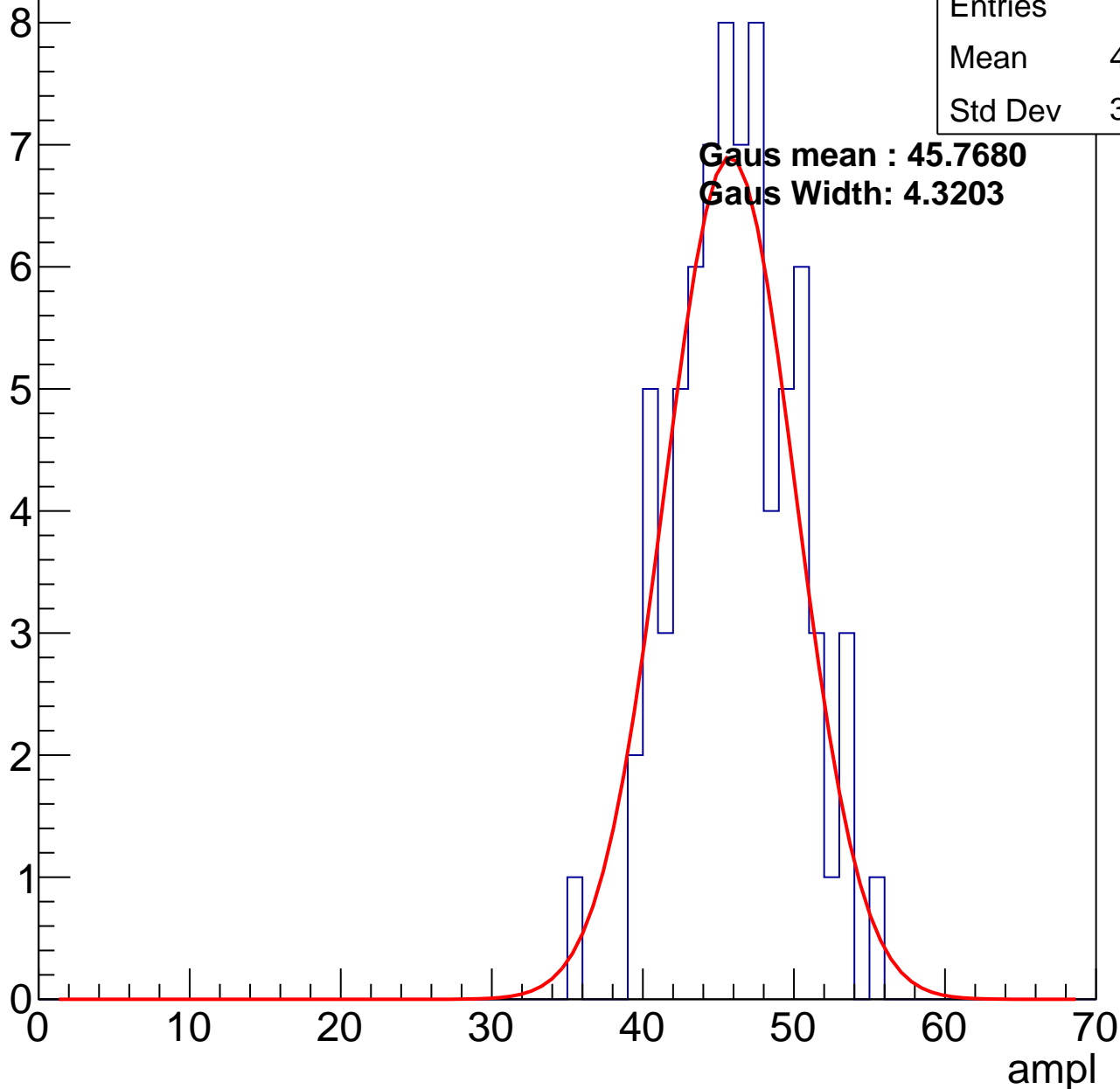
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	75
Mean	45.68
Std Dev	3.899

**Gaus mean : 45.7680**

**Gaus Width: 4.3203**

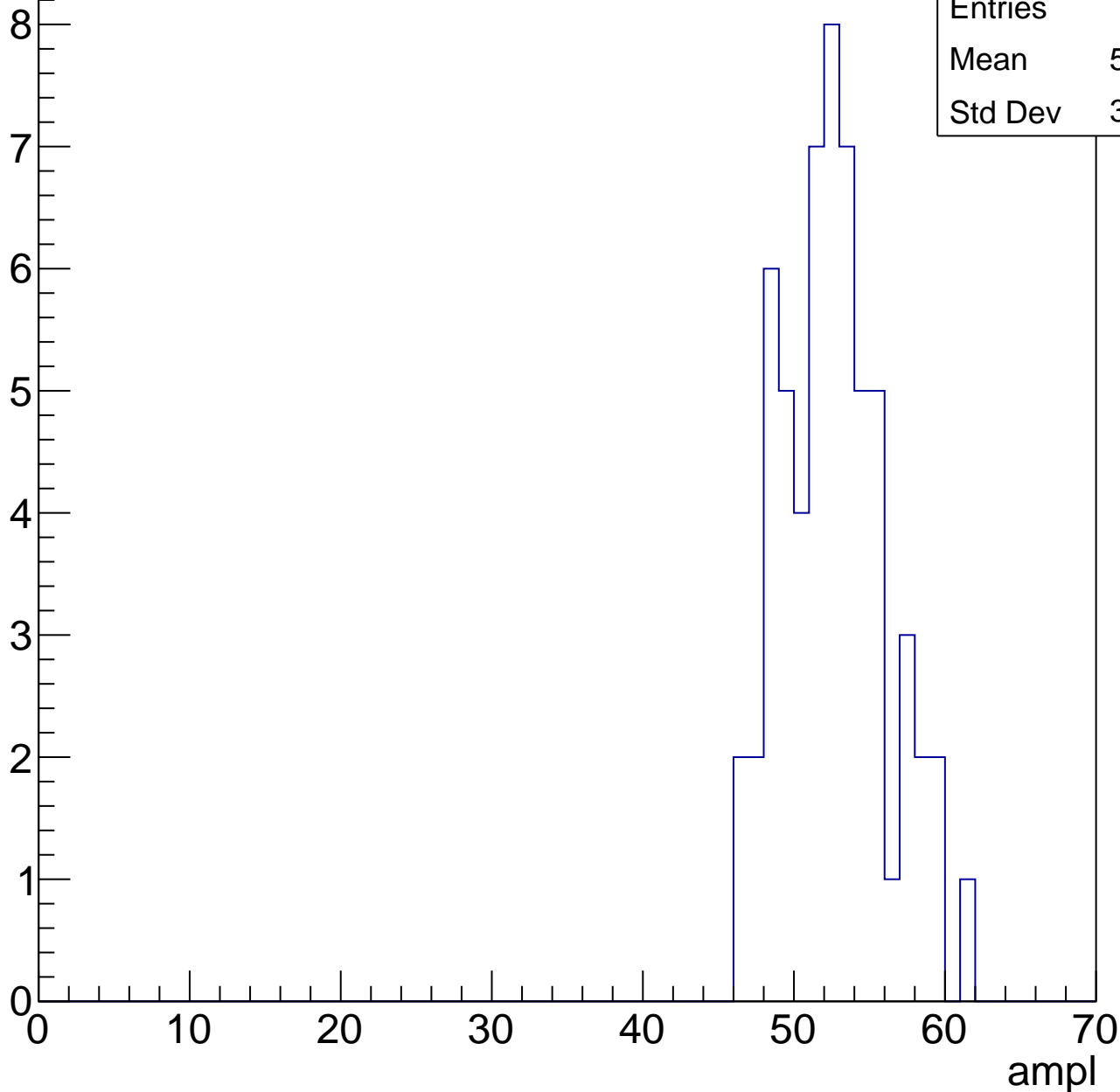


# B1L103S, U11-ch23, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

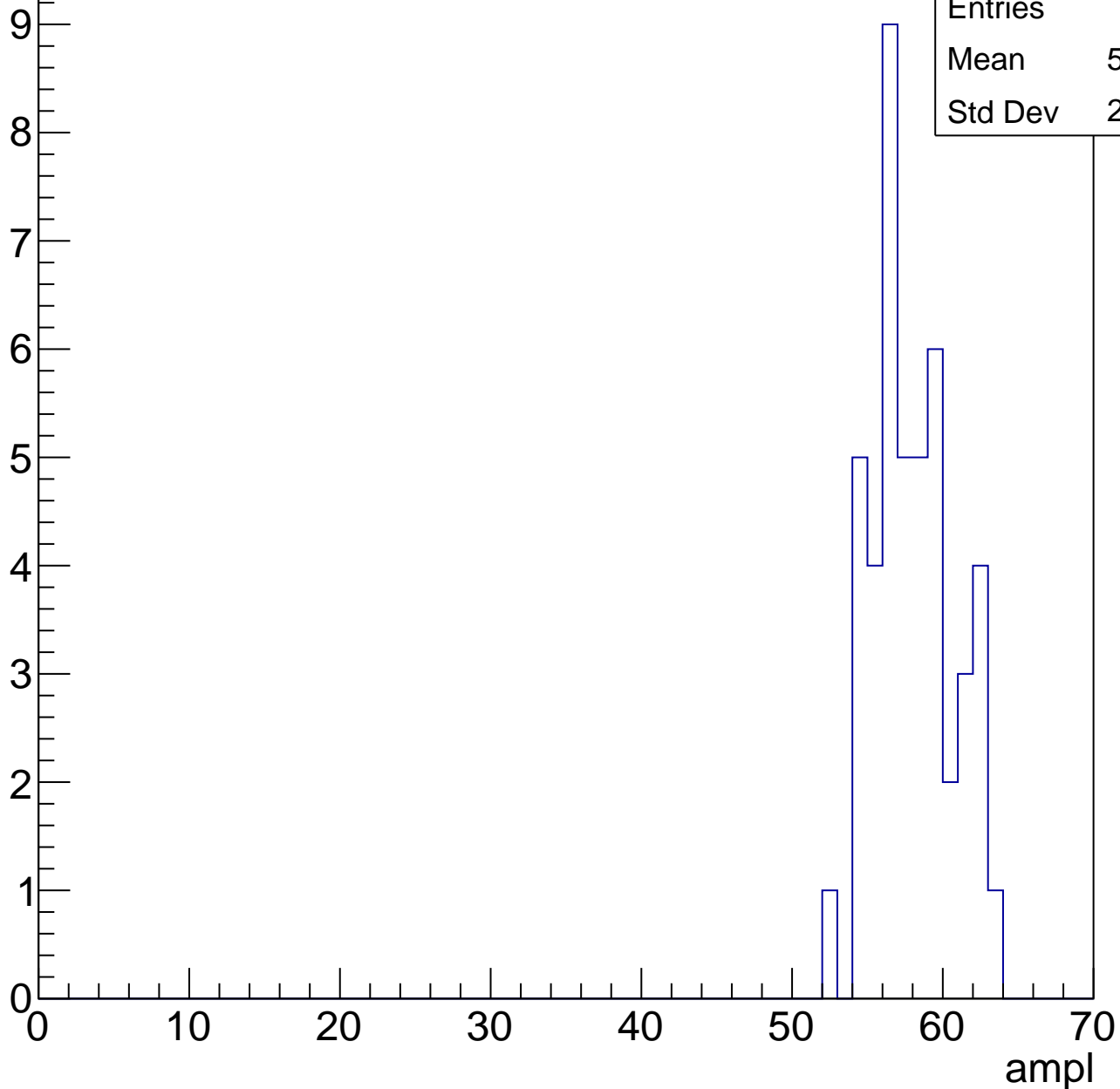
Entries	60
Mean	52.17
Std Dev	3.412



# B1L103S, U11-ch23, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	45
Mean	57.53
Std Dev	2.638

# B1L103S, U11-ch23, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

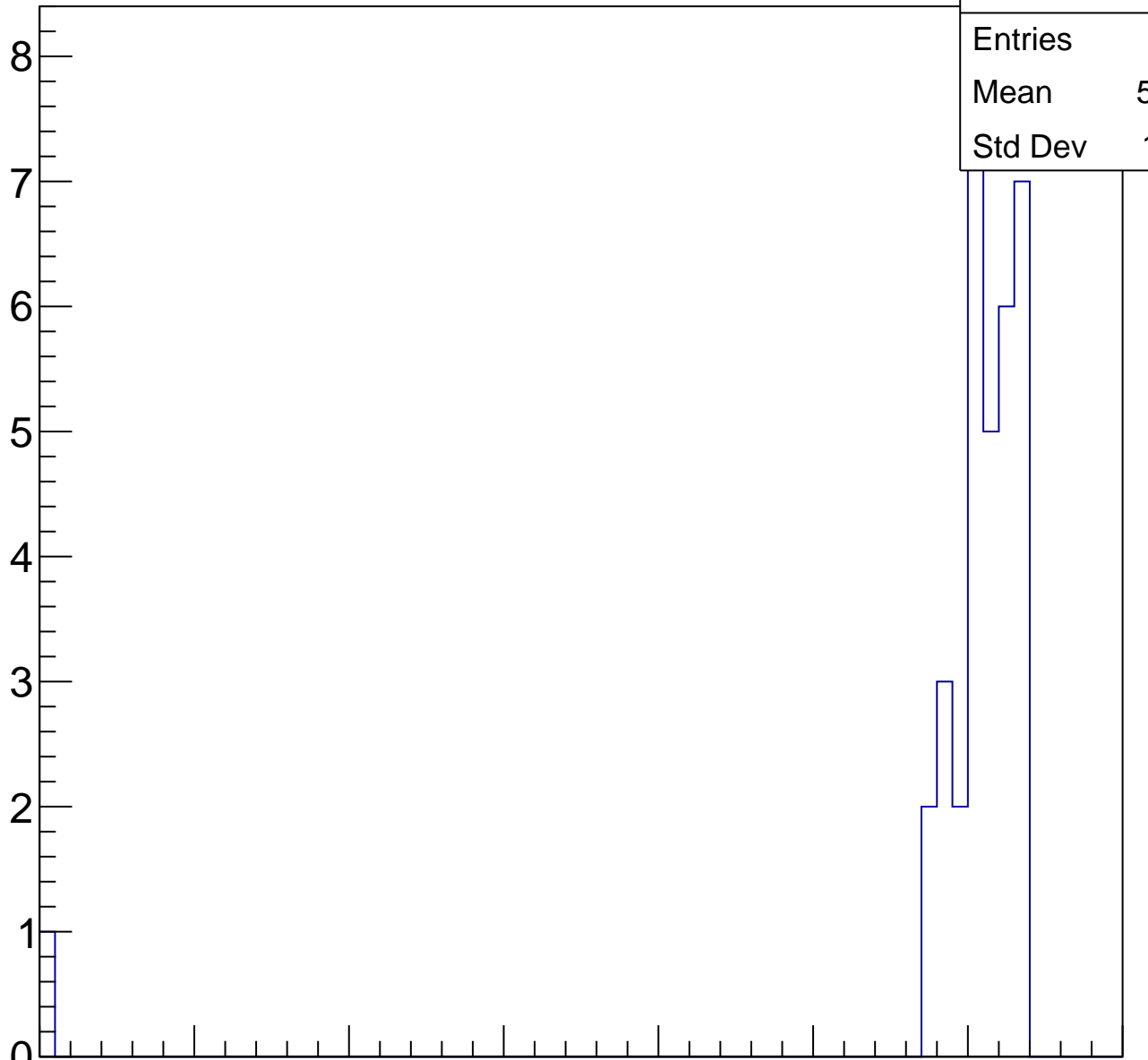
Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	34
Mean	58.94
Std Dev	10.41

ampl

0 10 20 30 40 50 60 70



# B1L103S, U11-ch23, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U11-ch23, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U11-ch24, adc0

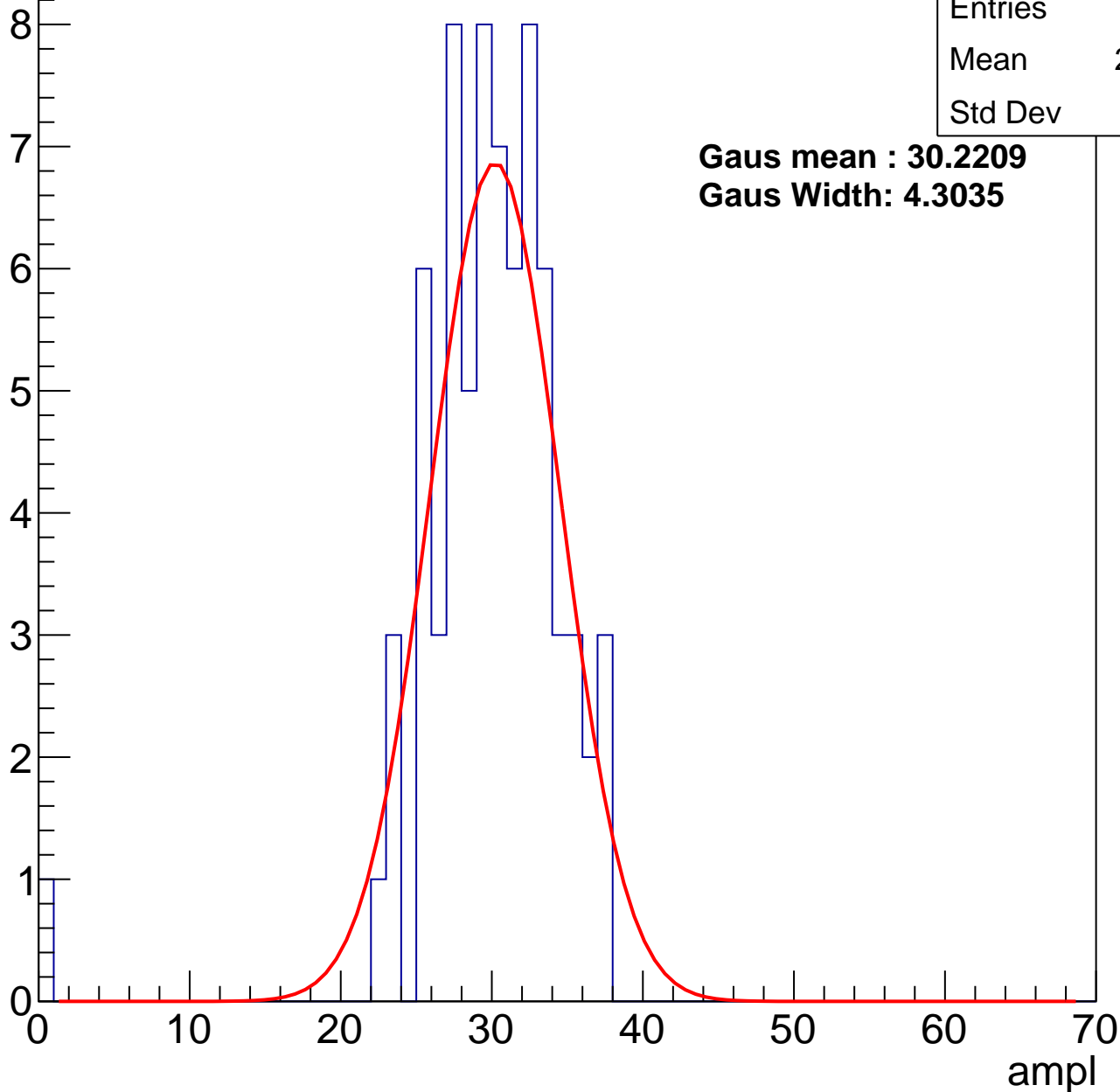
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	73
Mean	29.41
Std Dev	4.99

**Gaus mean : 30.2209**

**Gaus Width: 4.3035**



# B1L103S, U11-ch24, adc1

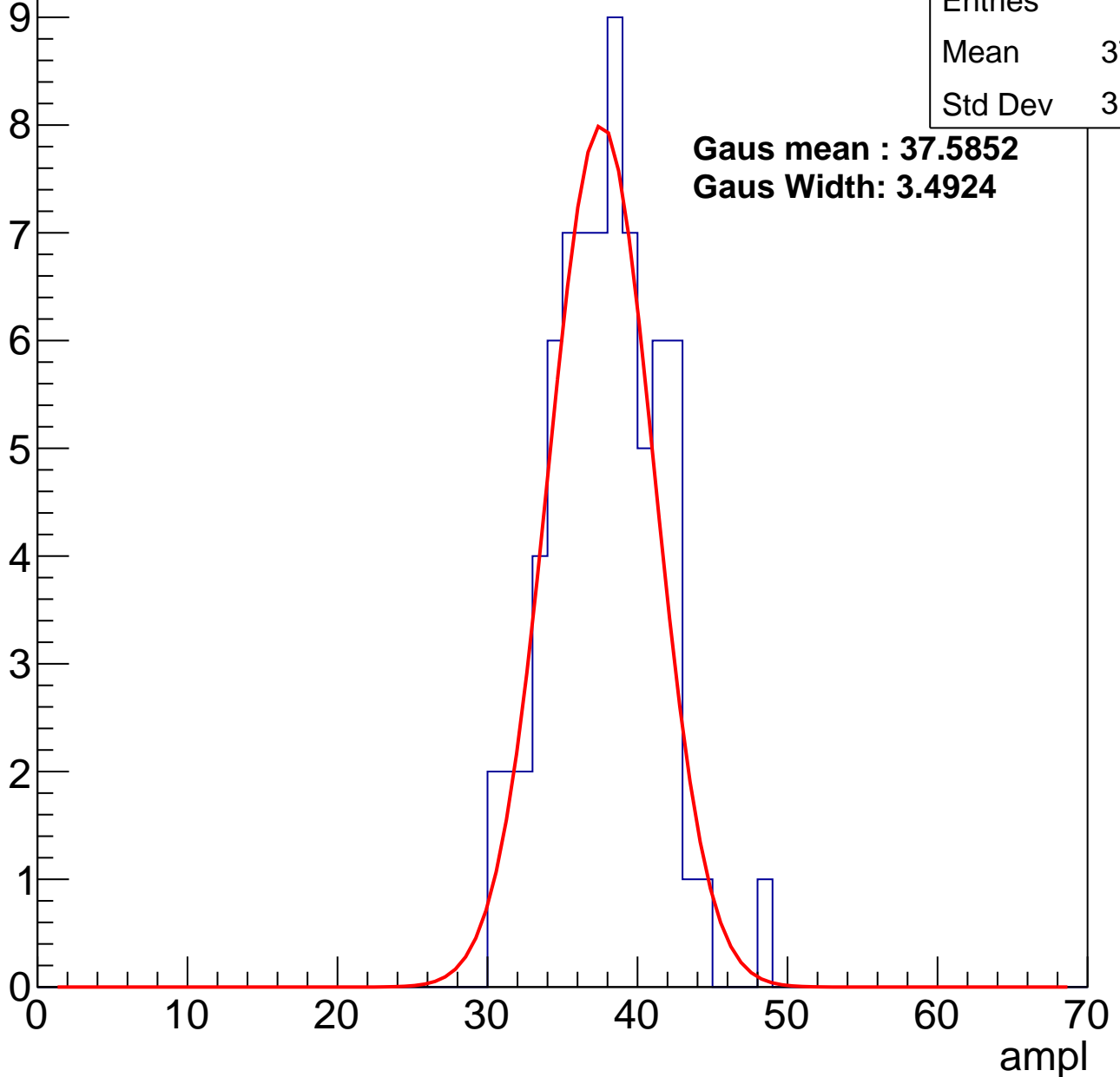
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	73
Mean	37.34
Std Dev	3.508

**Gaus mean : 37.5852**

**Gaus Width: 3.4924**



# B1L103S, U11-ch24, adc2

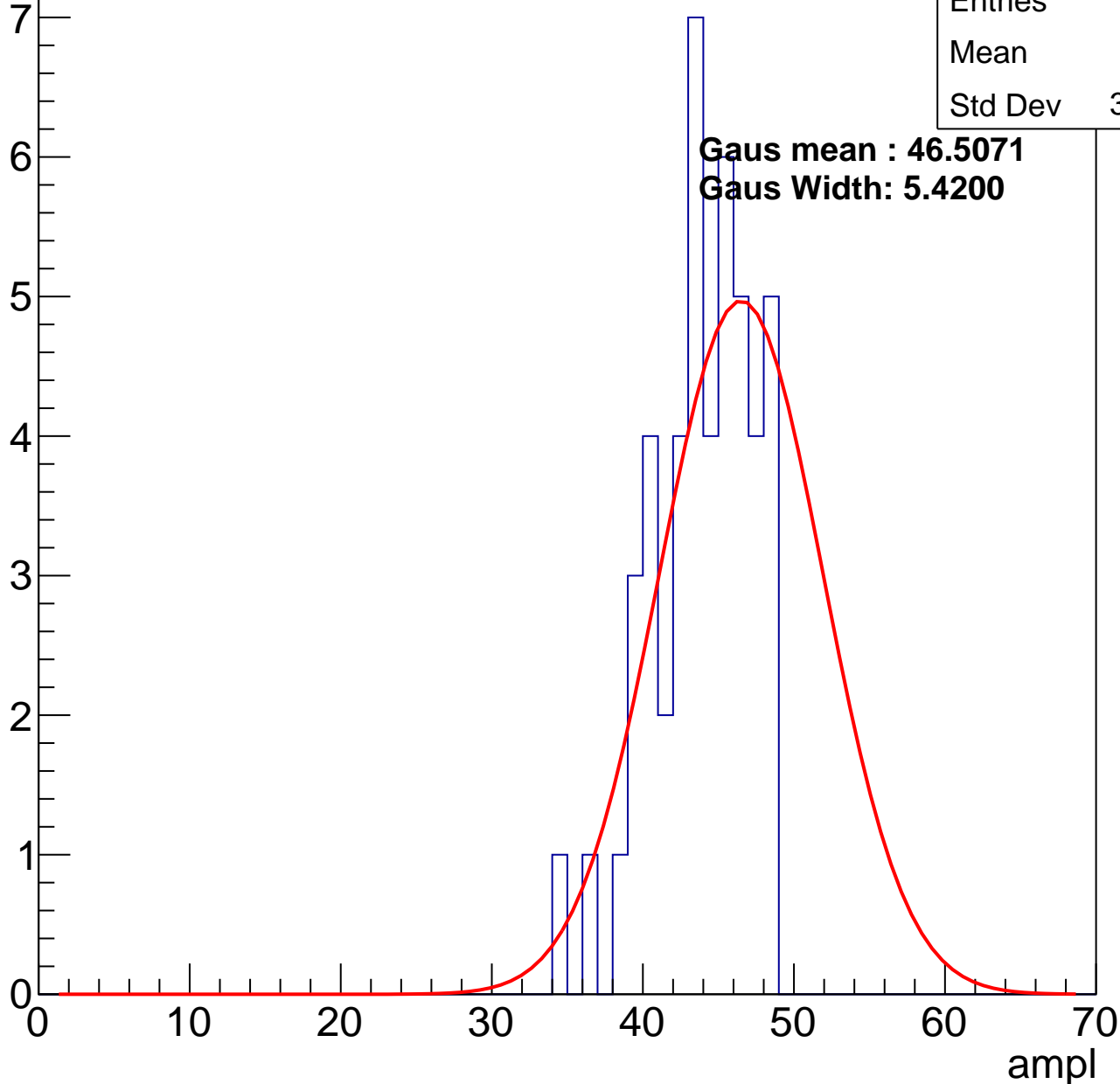
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	47
Mean	43.4
Std Dev	3.279

**Gaus mean : 46.5071**

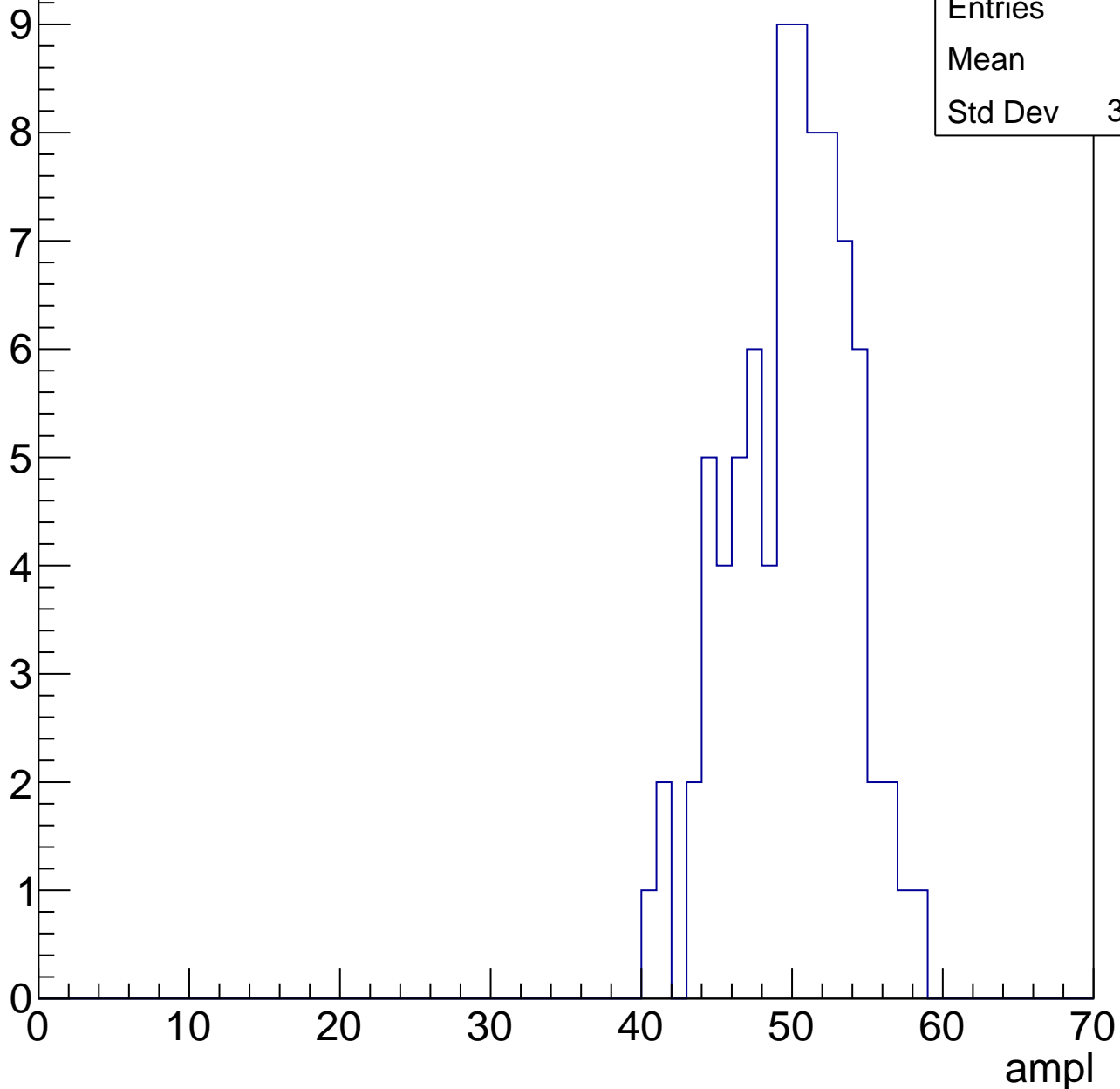
**Gaus Width: 5.4200**



# B1L103S, U11-ch24, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

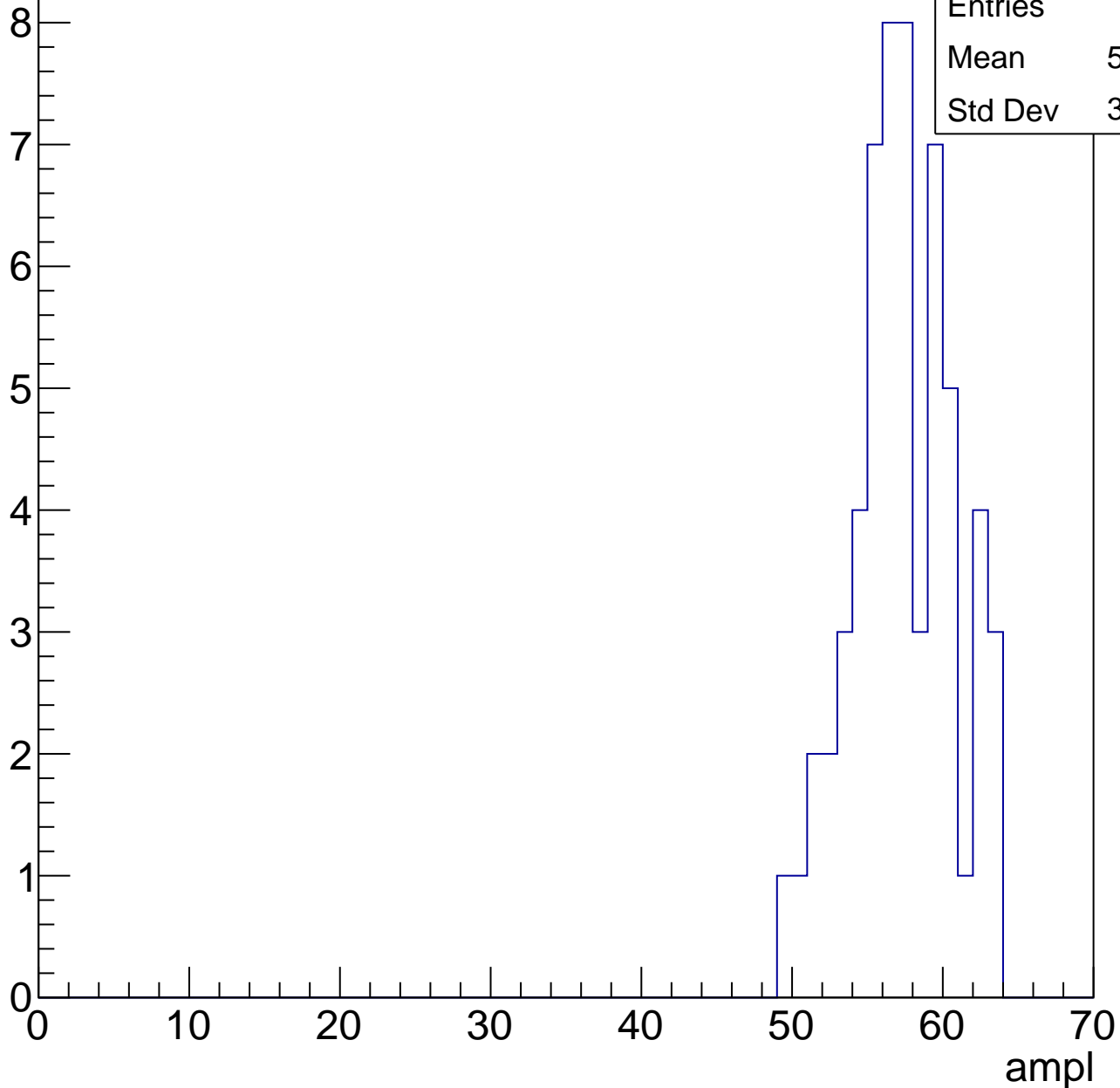
Entry



# B1L103S, U11-ch24, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



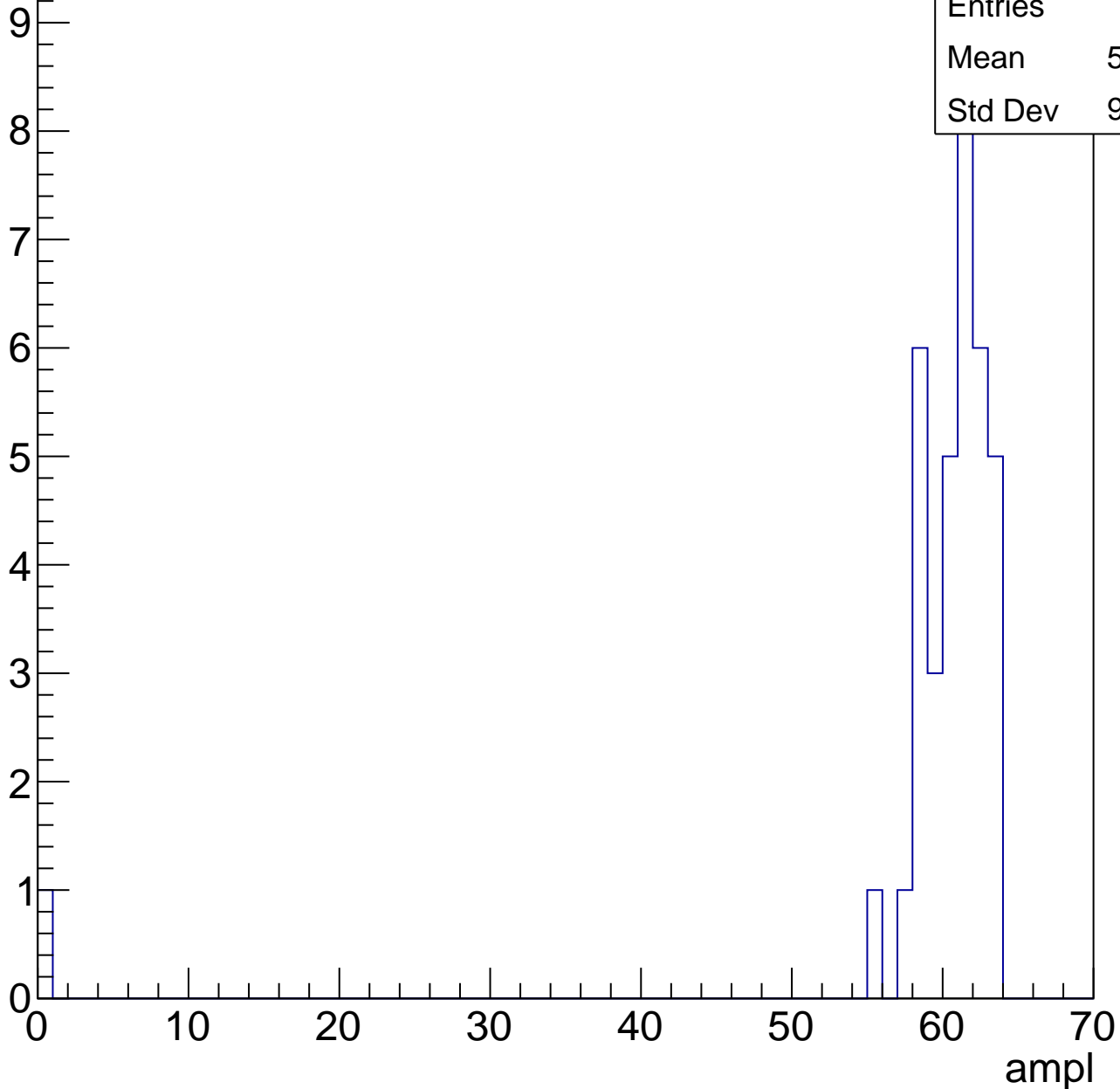
Entries	59
Mean	56.85
Std Dev	3.328

# B1L103S, U11-ch24, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	37
Mean	58.73
Std Dev	9.972



# B1L103S, U11-ch24, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U11-ch24, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U11-ch25, adc0

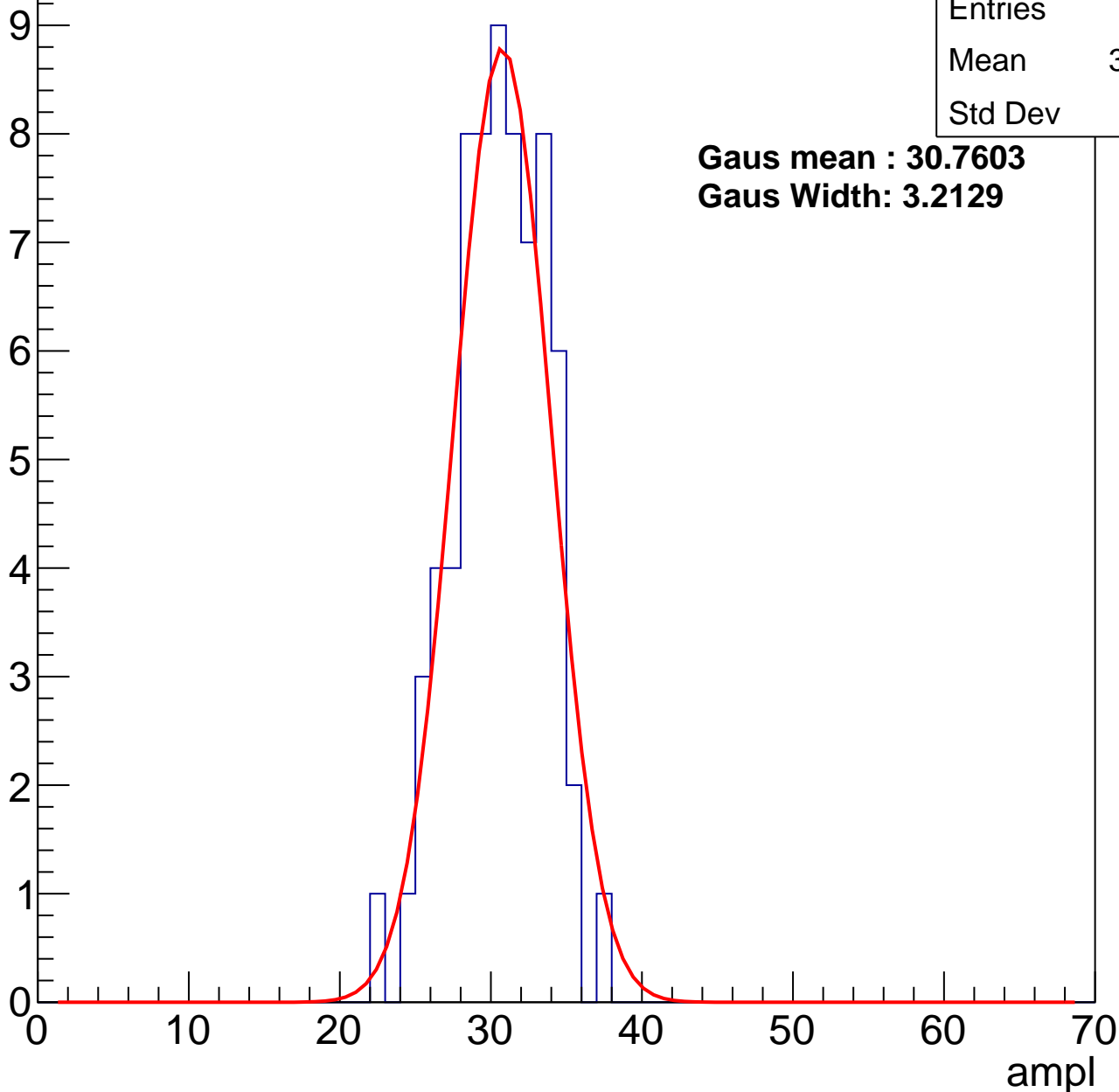
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	70
Mean	30.09
Std Dev	2.97

**Gaus mean : 30.7603**

**Gaus Width: 3.2129**



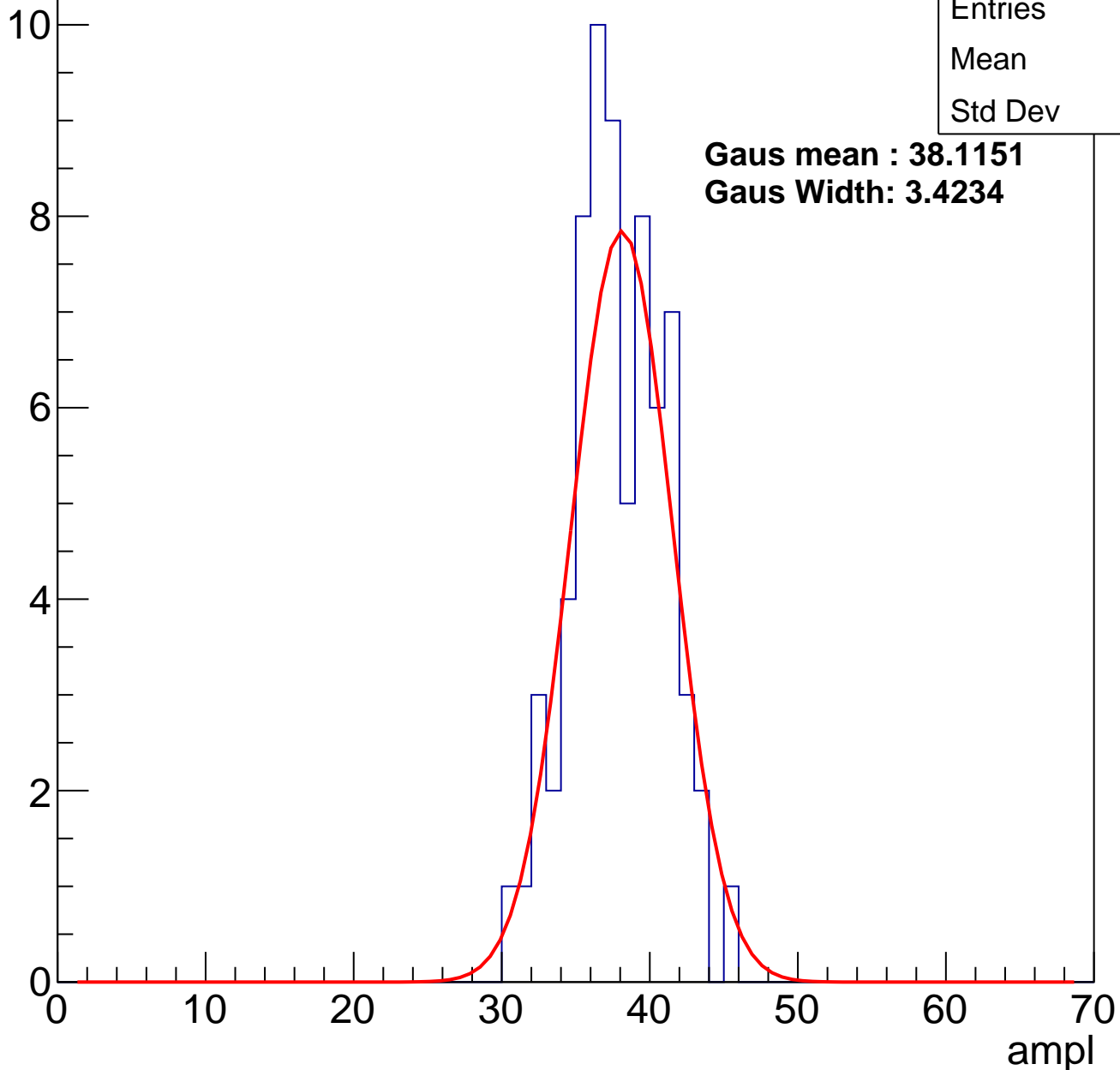
# B1L103S, U11-ch25, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	70
Mean	37.4
Std Dev	3.1

**Gaus mean : 38.1151**  
**Gaus Width: 3.4234**

Entry



# B1L103S, U11-ch25, adc2

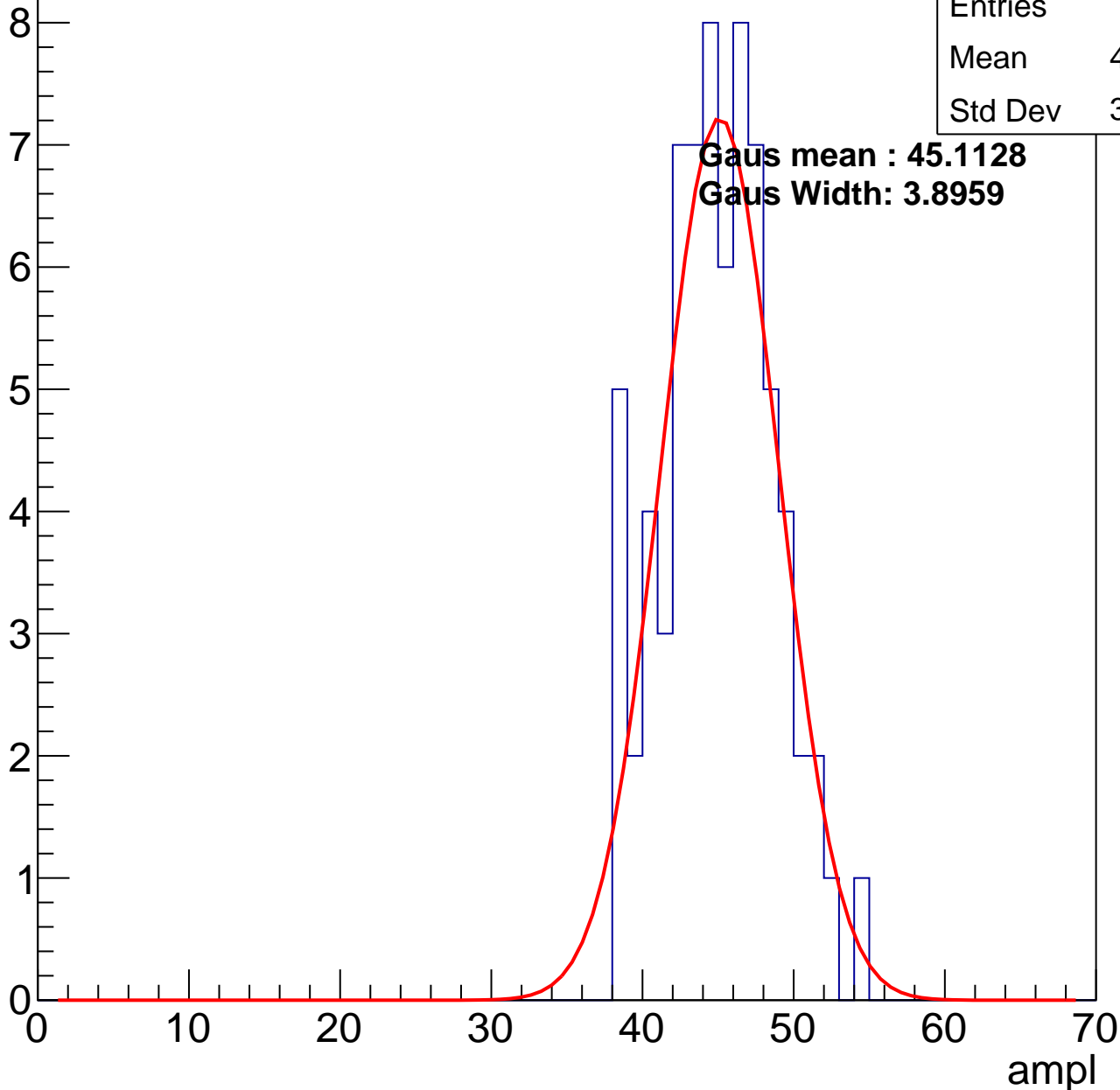
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	72
Mean	44.57
Std Dev	3.628

**Gaus mean : 45.1128**

**Gaus Width: 3.8959**

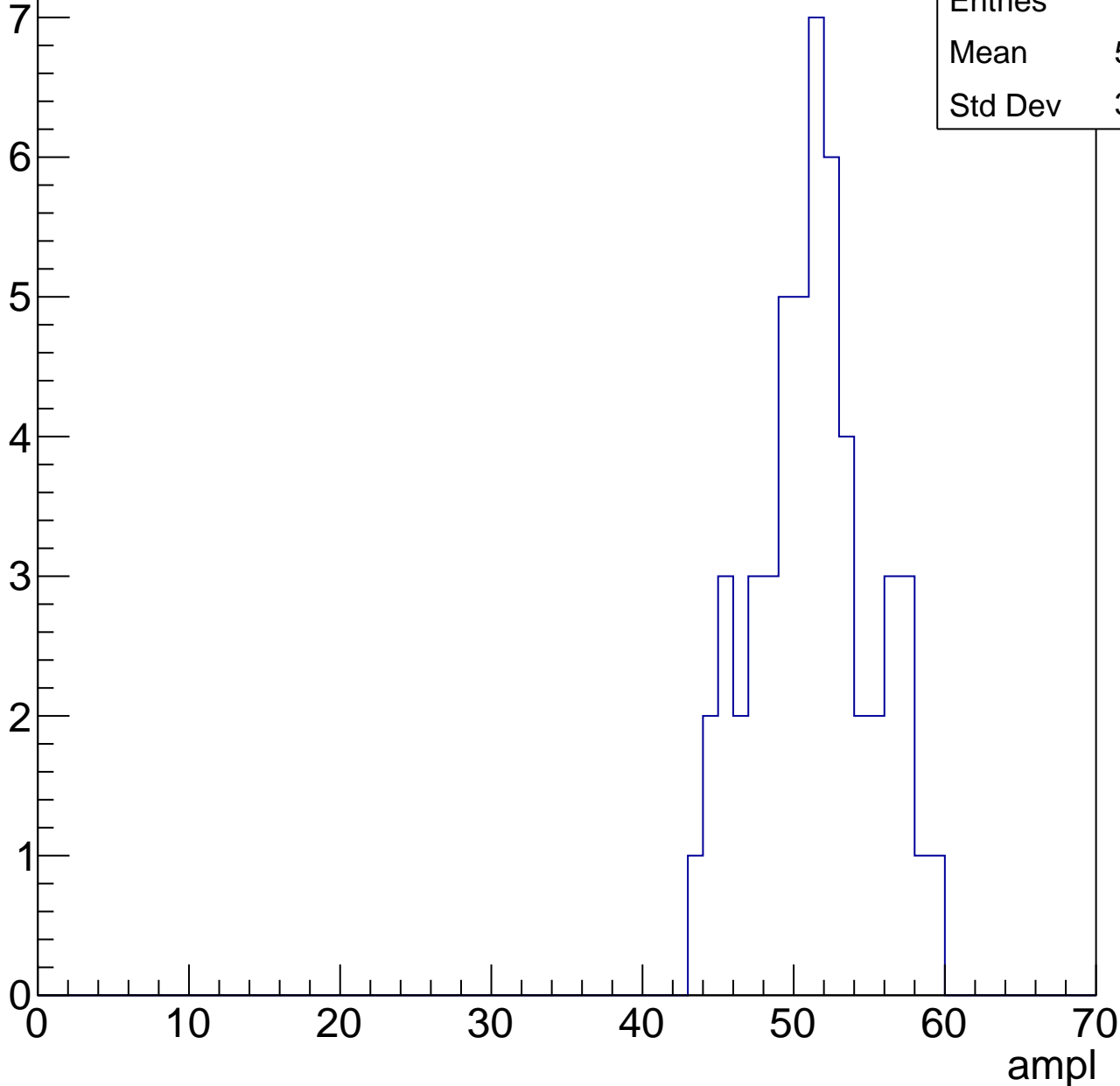


# B1L103S, U11-ch25, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

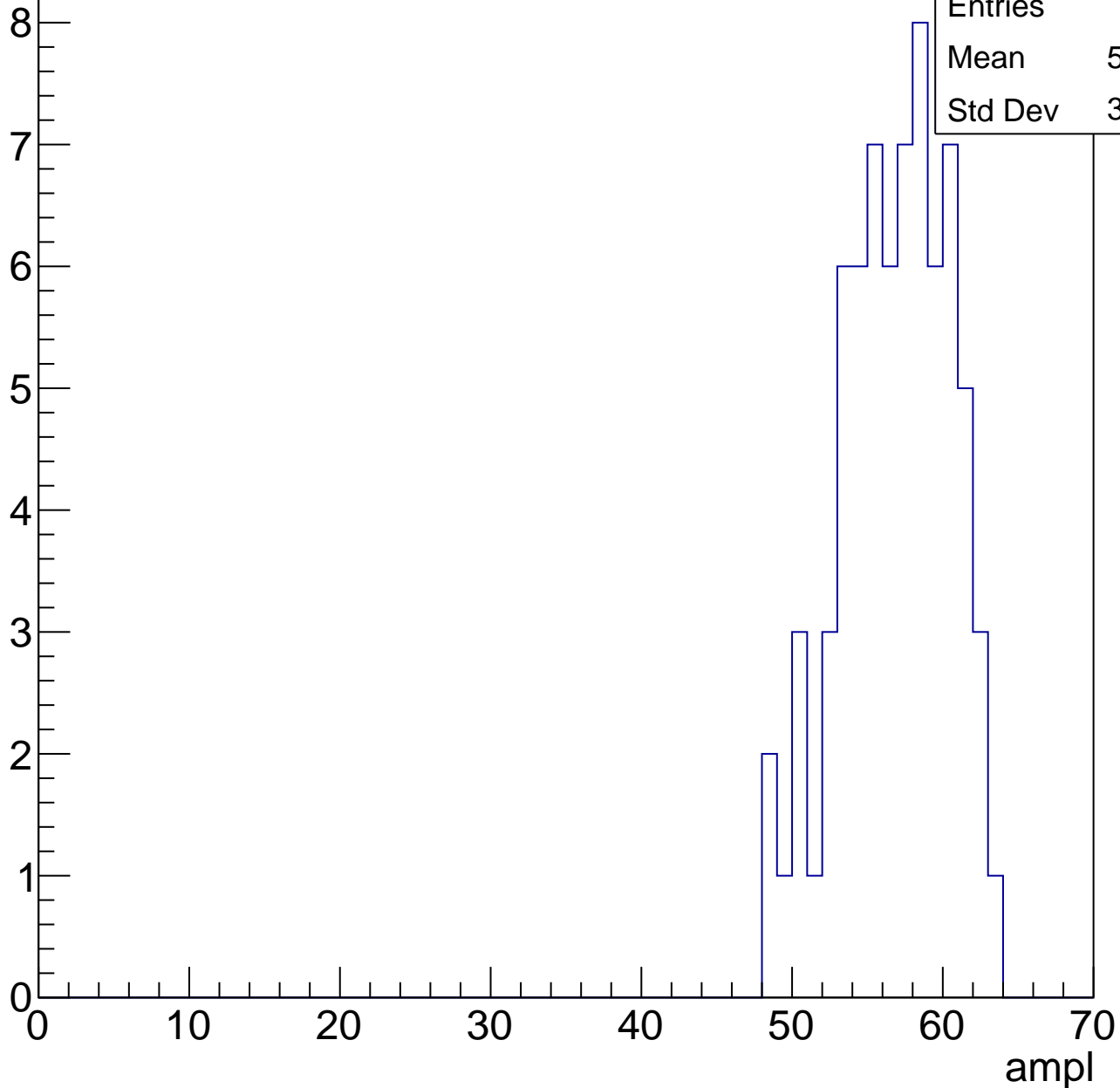
Entries	53
Mean	50.81
Std Dev	3.851



# B1L103S, U11-ch25, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



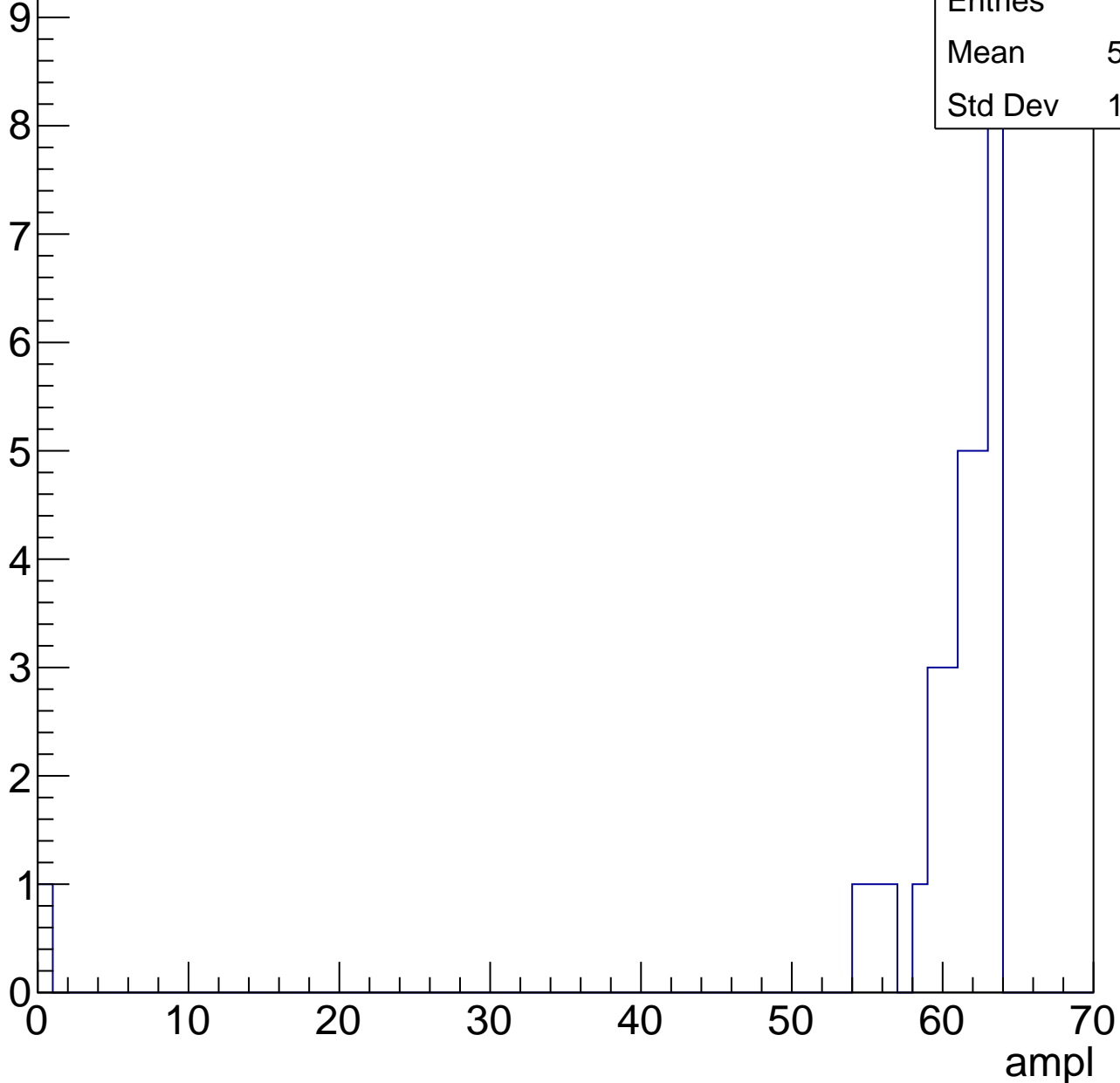
Entries	72
Mean	56.33
Std Dev	3.578

# B1L103S, U11-ch25, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	30
Mean	58.73
Std Dev	11.17



# B1L103S, U11-ch25, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U11-ch25, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L103S, U11-ch26, adc0

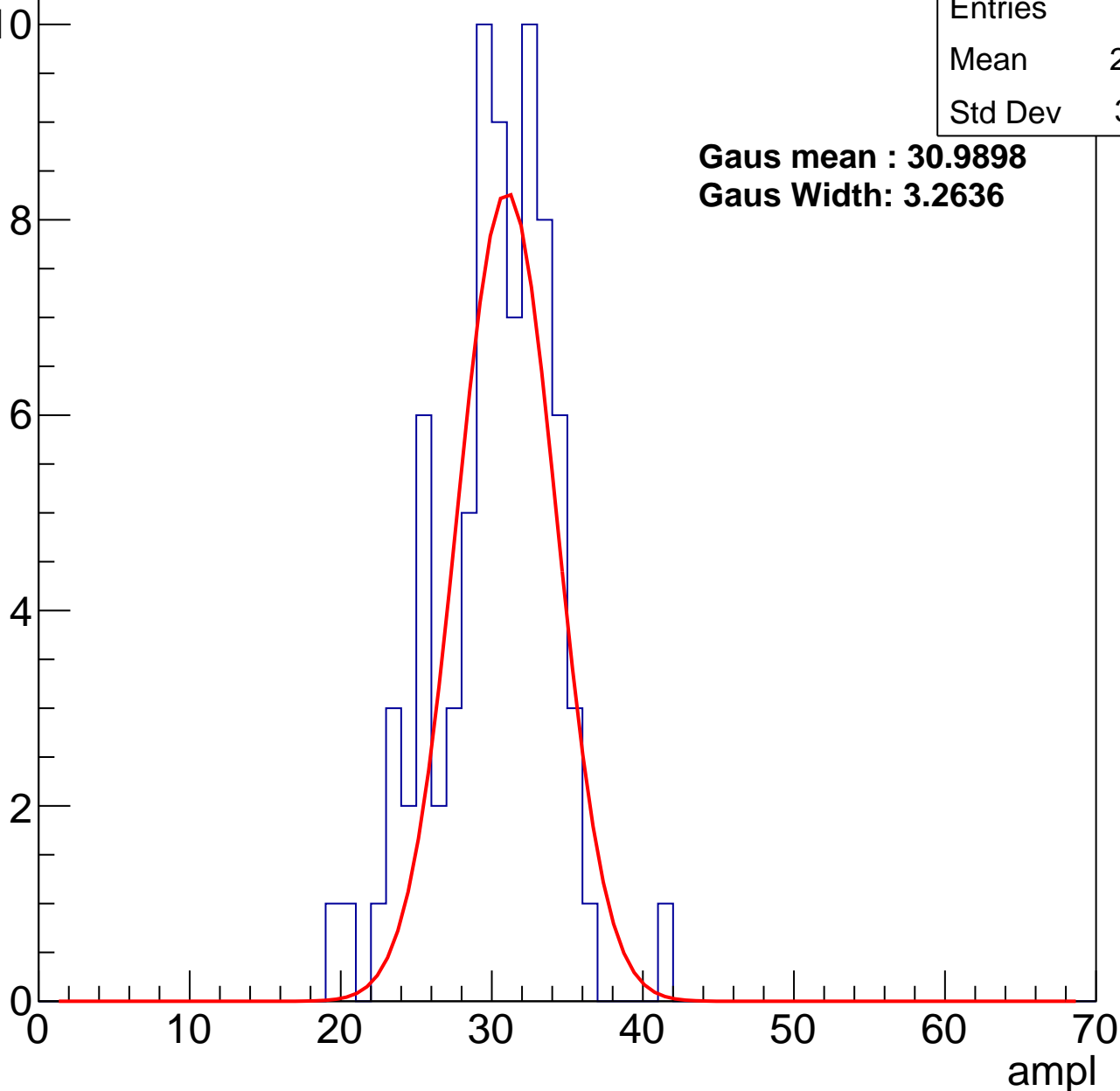
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	79
Mean	29.72
Std Dev	3.871

**Gaus mean : 30.9898**

**Gaus Width: 3.2636**



# B1L103S, U11-ch26, adc1

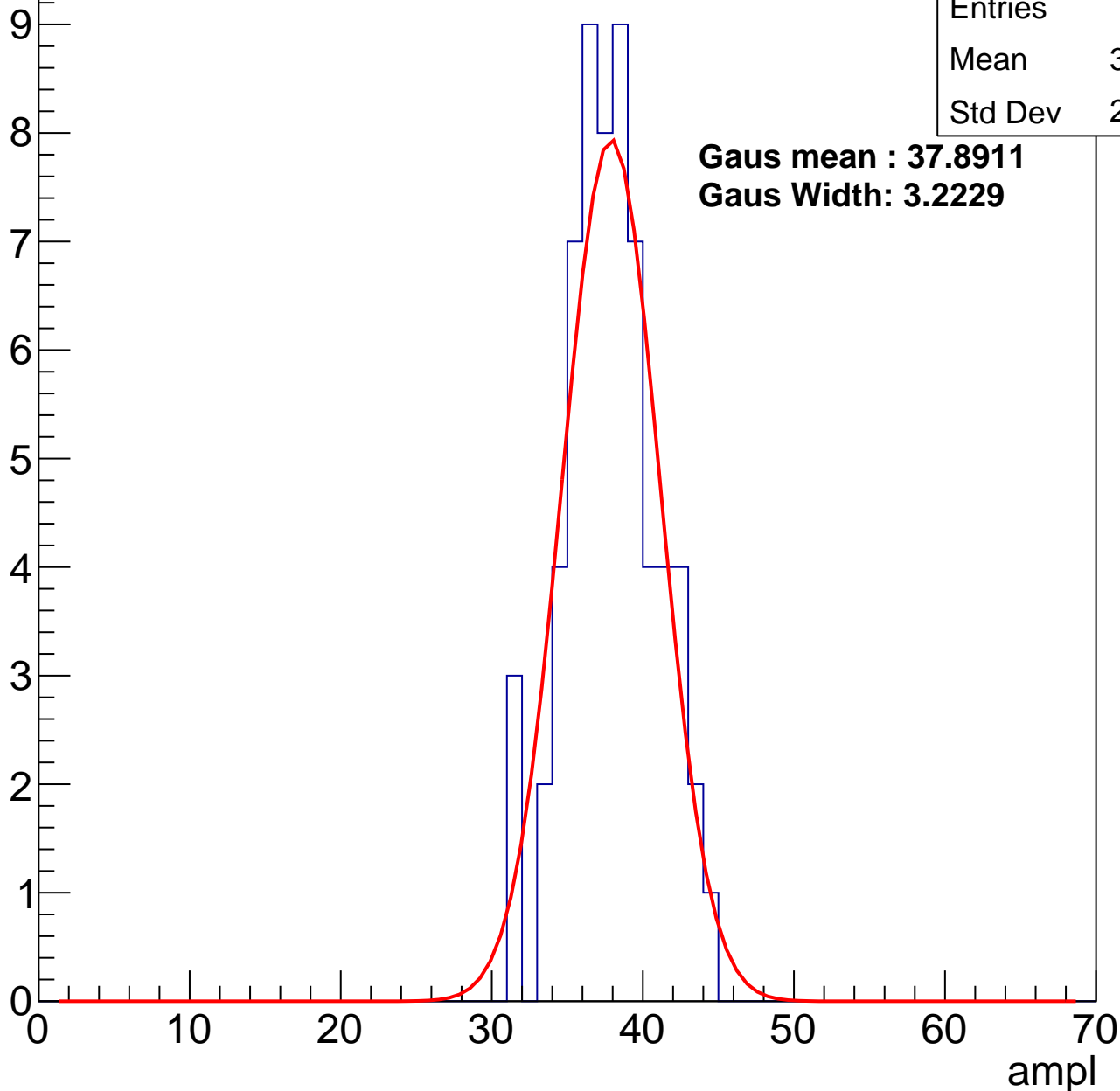
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	37.45
Std Dev	2.952

**Gaus mean : 37.8911**

**Gaus Width: 3.2229**



# B1L103S, U11-ch26, adc2

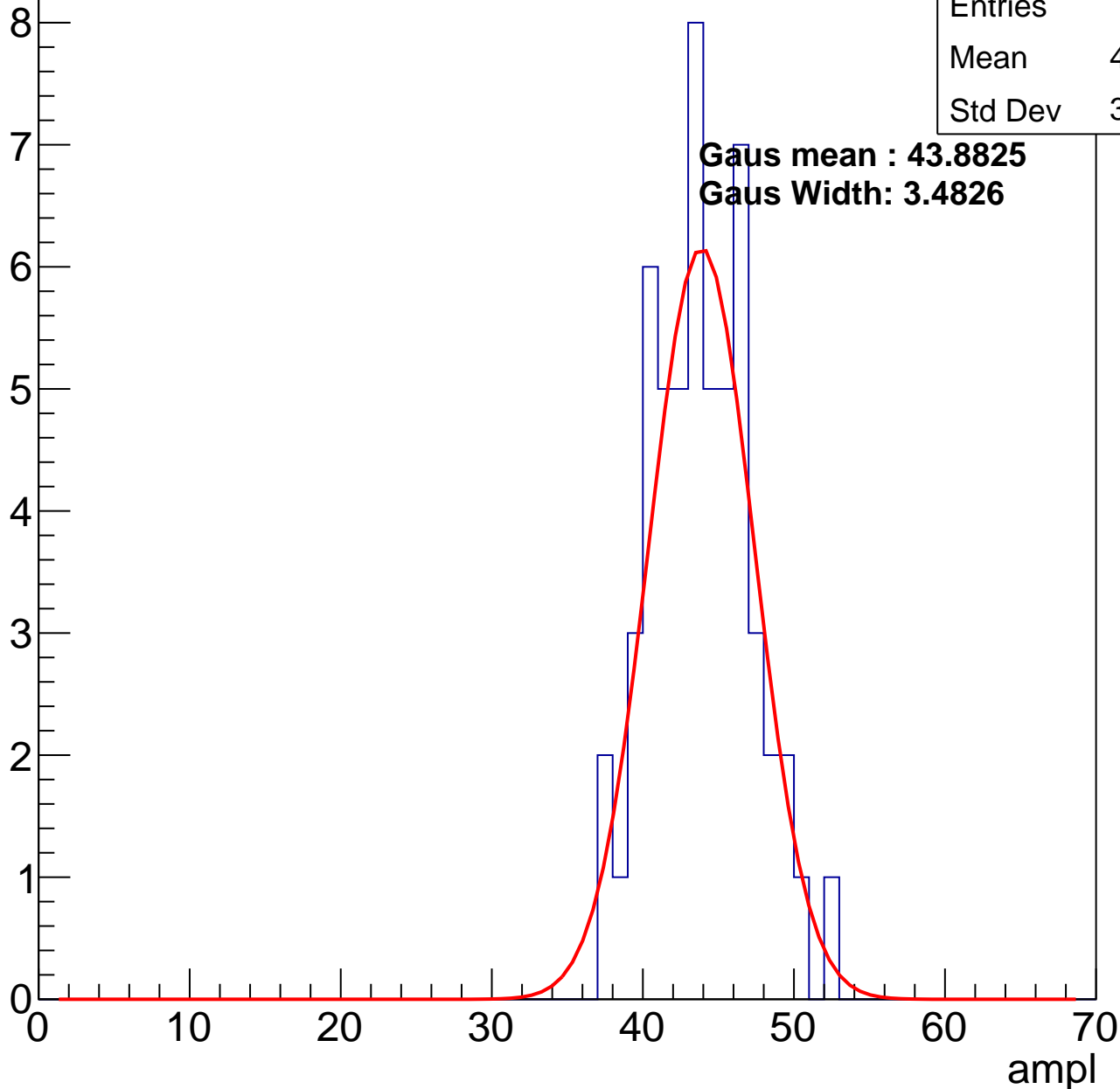
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	56
Mean	43.43
Std Dev	3.278

**Gaus mean : 43.8825**

**Gaus Width: 3.4826**

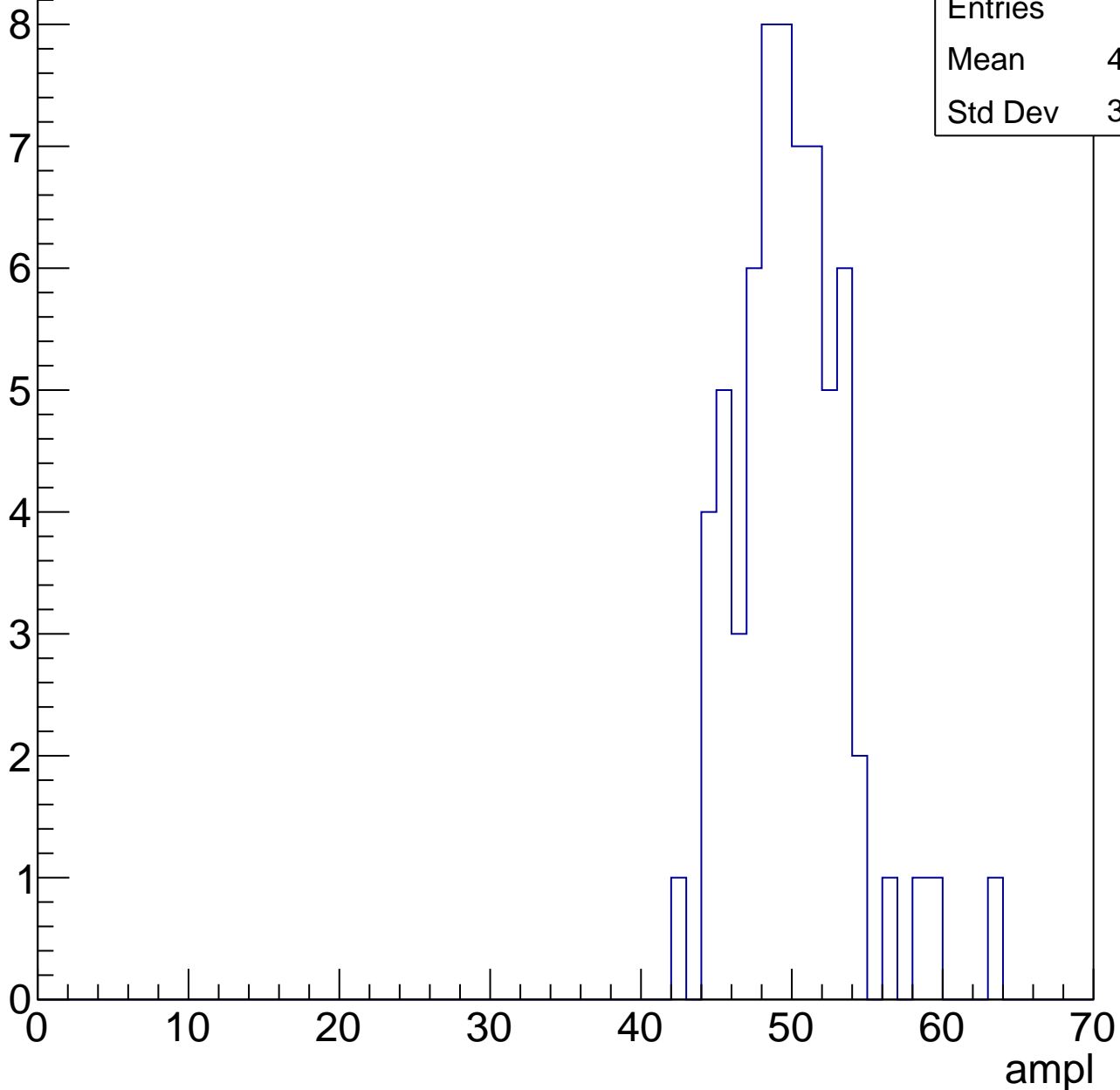


# B1L103S, U11-ch26, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

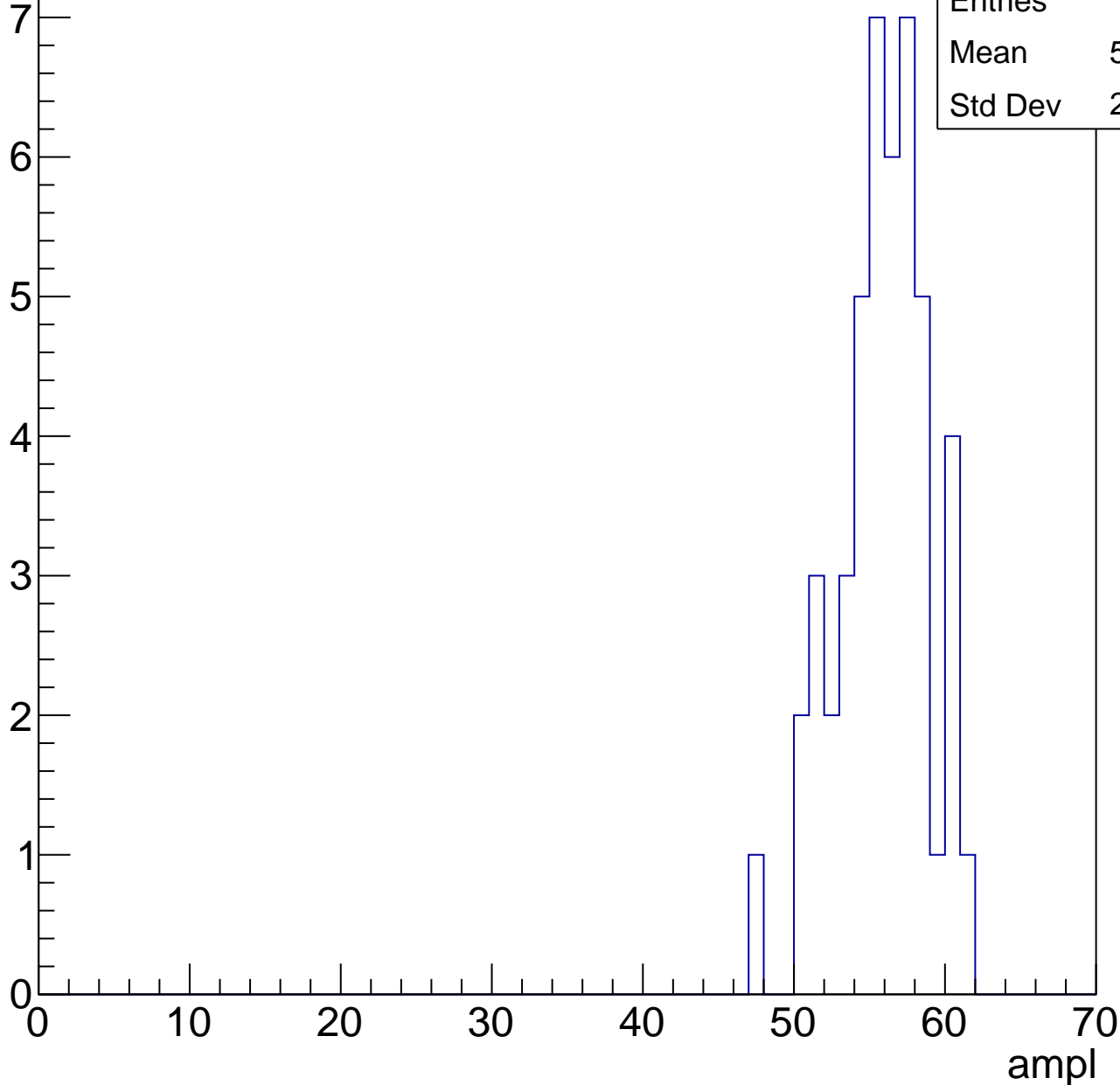
Entries	66
Mean	49.52
Std Dev	3.739



# B1L103S, U11-ch26, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

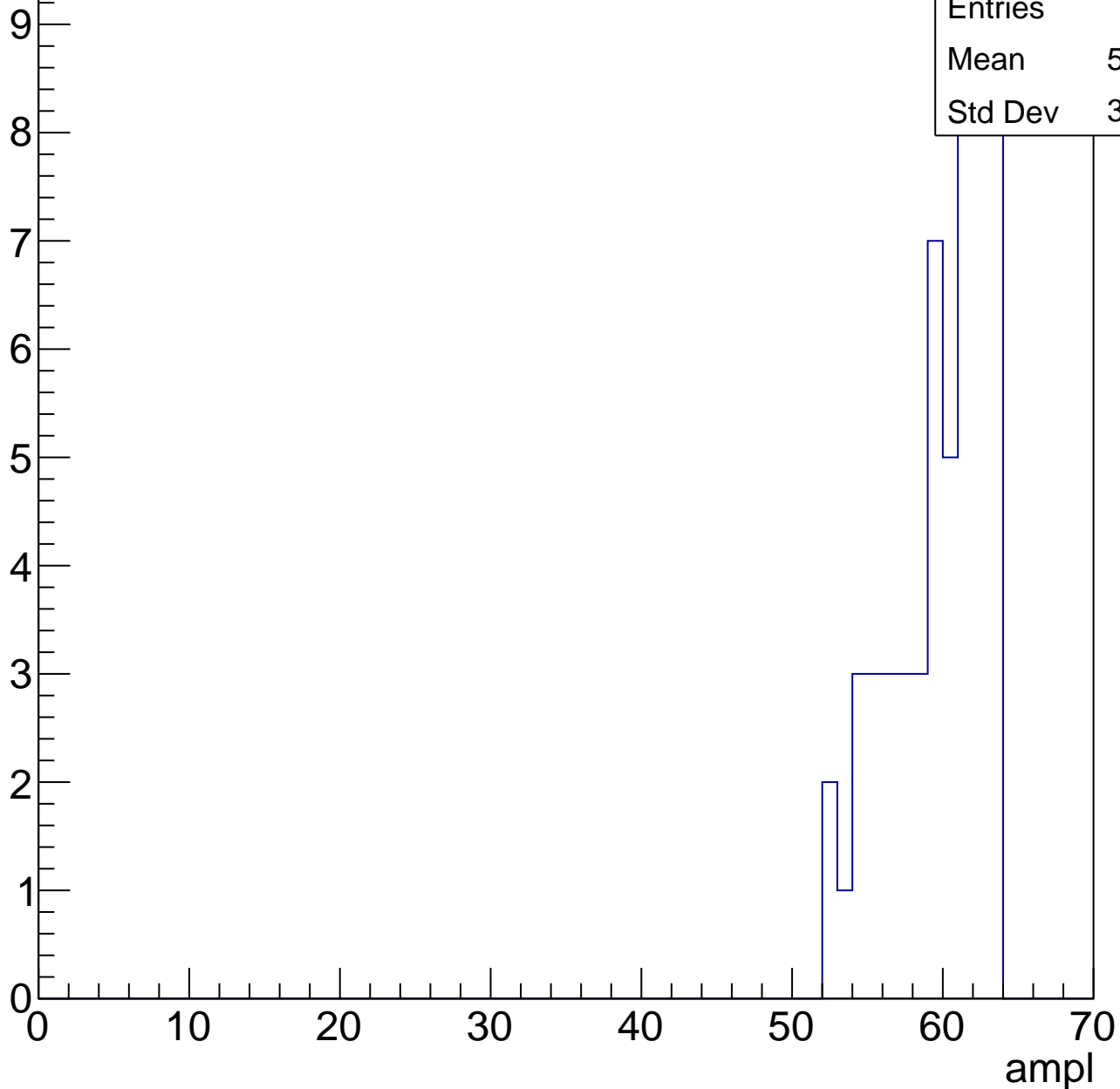


Entries	47
Mean	55.38
Std Dev	2.993

# B1L103S, U11-ch26, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

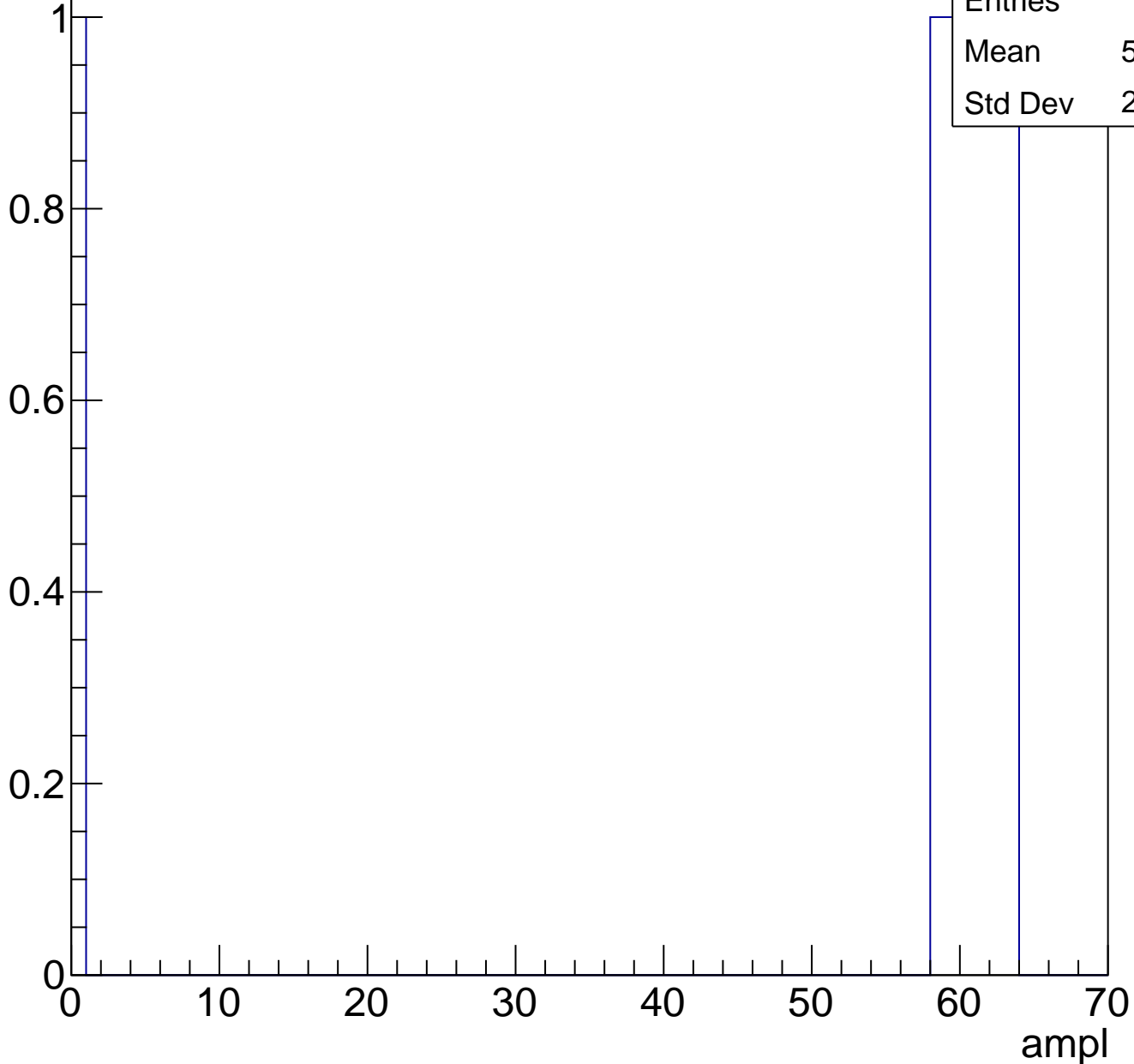
Entry



# B1L103S, U11-ch26, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U11-ch26, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L103S, U11-ch27, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	75
Mean	30.72
Std Dev	3.235

**Gaus mean : 30.9665**

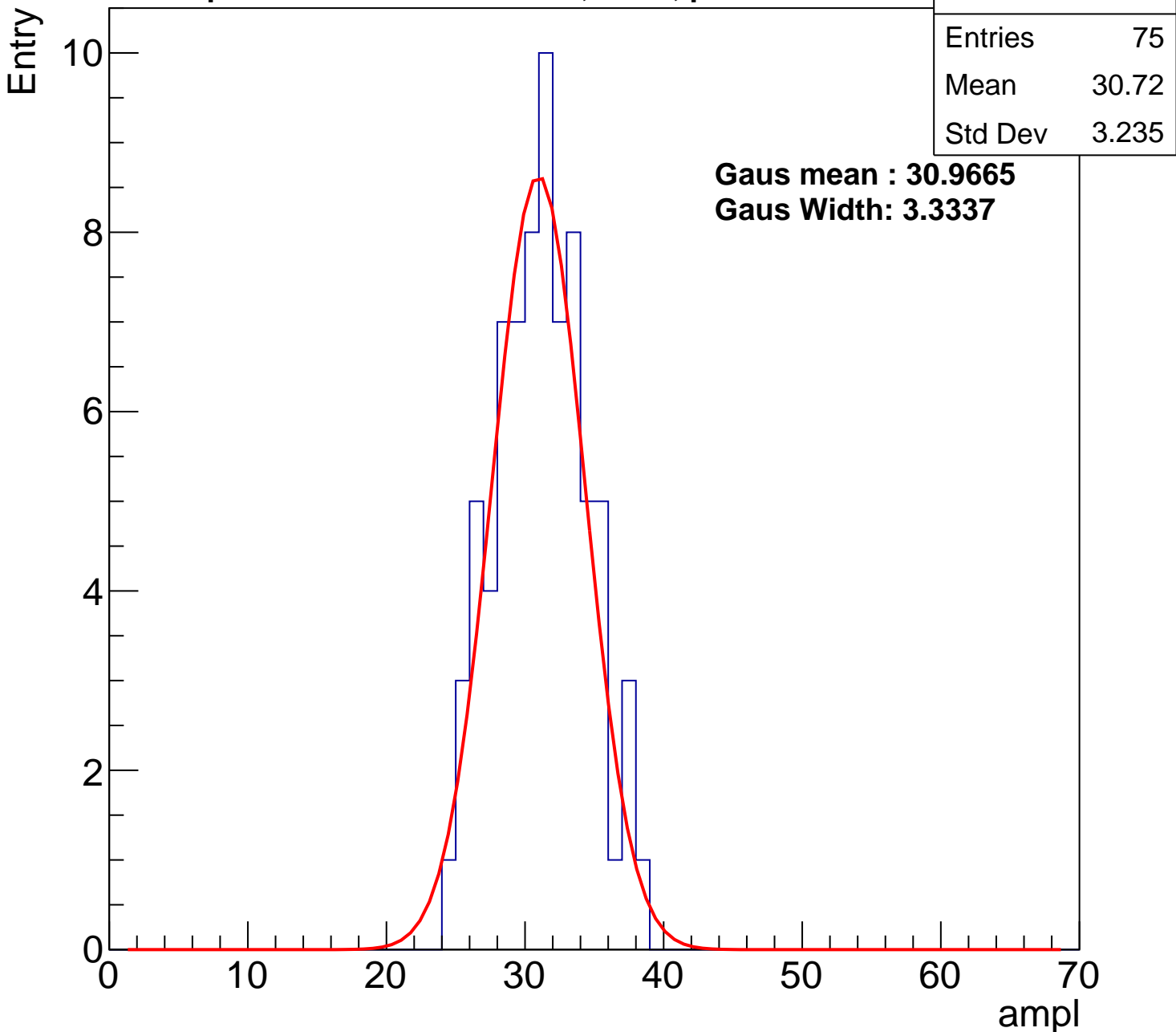
**Gaus Width: 3.3337**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U11-ch27, adc1

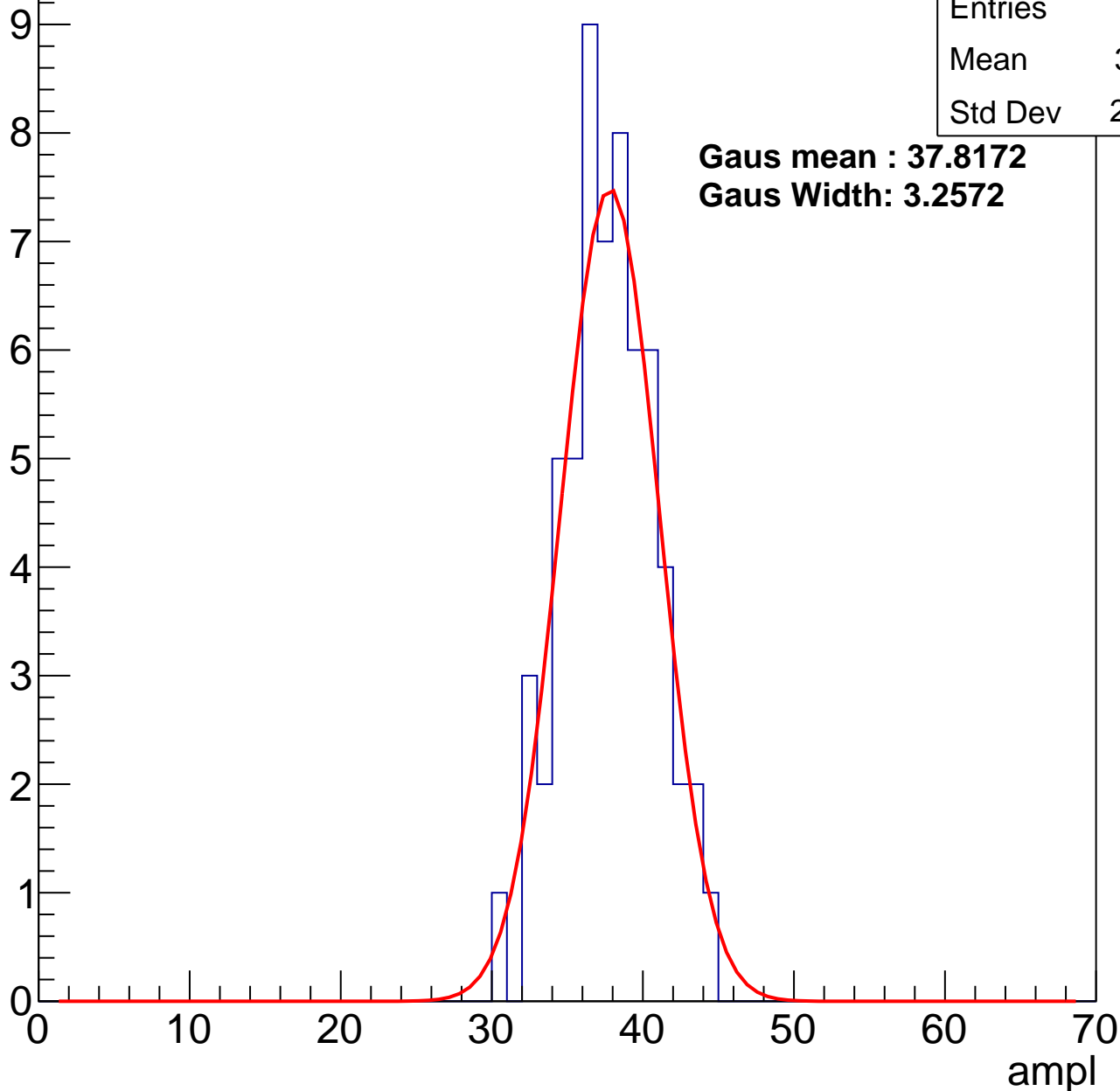
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	61
Mean	37.31
Std Dev	2.989

**Gaus mean : 37.8172**

**Gaus Width: 3.2572**



# B1L103S, U11-ch27, adc2

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	80
Mean	44.74
Std Dev	3.353

**Gaus mean : 45.0843**

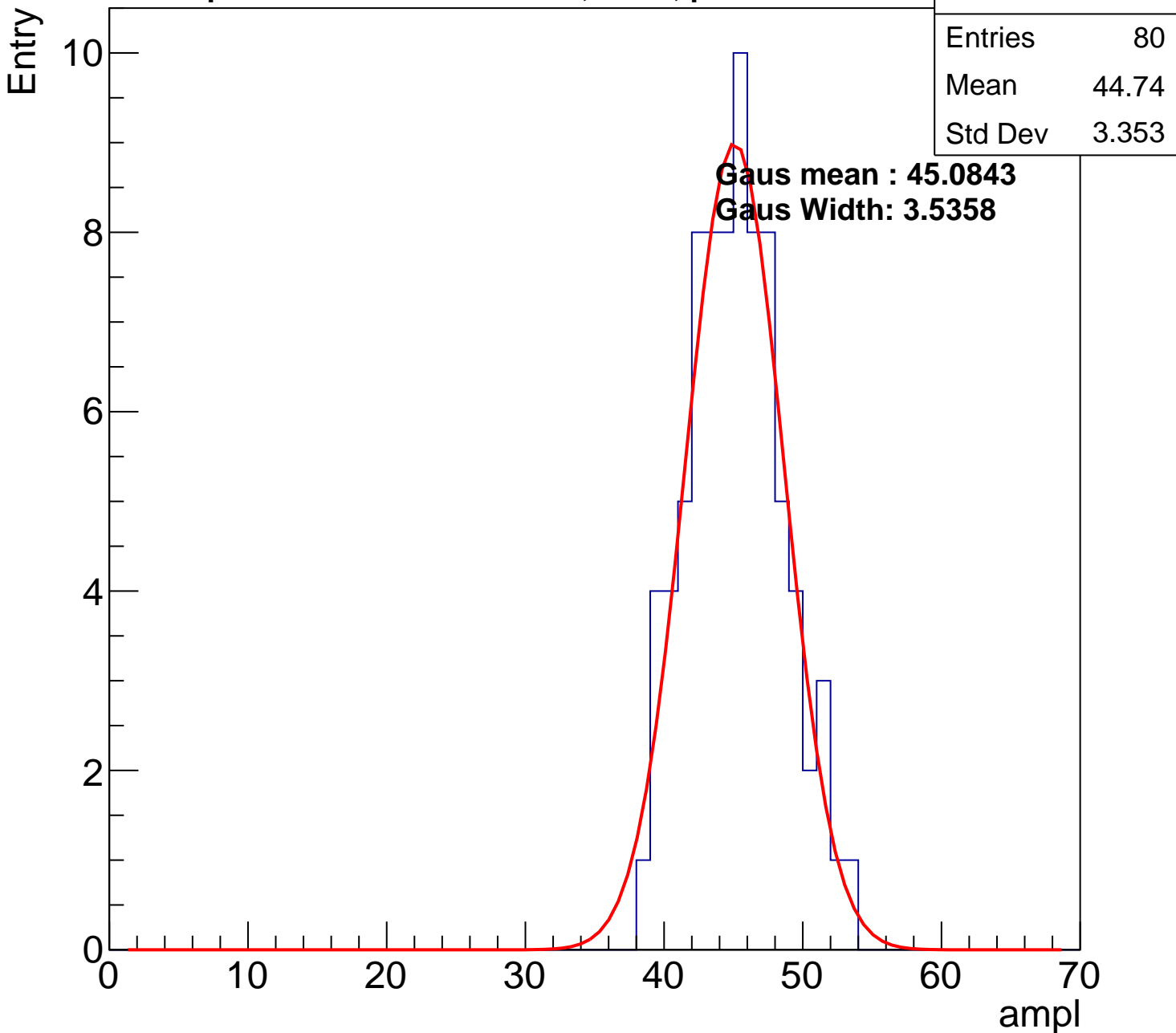
**Gaus Width: 3.5358**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

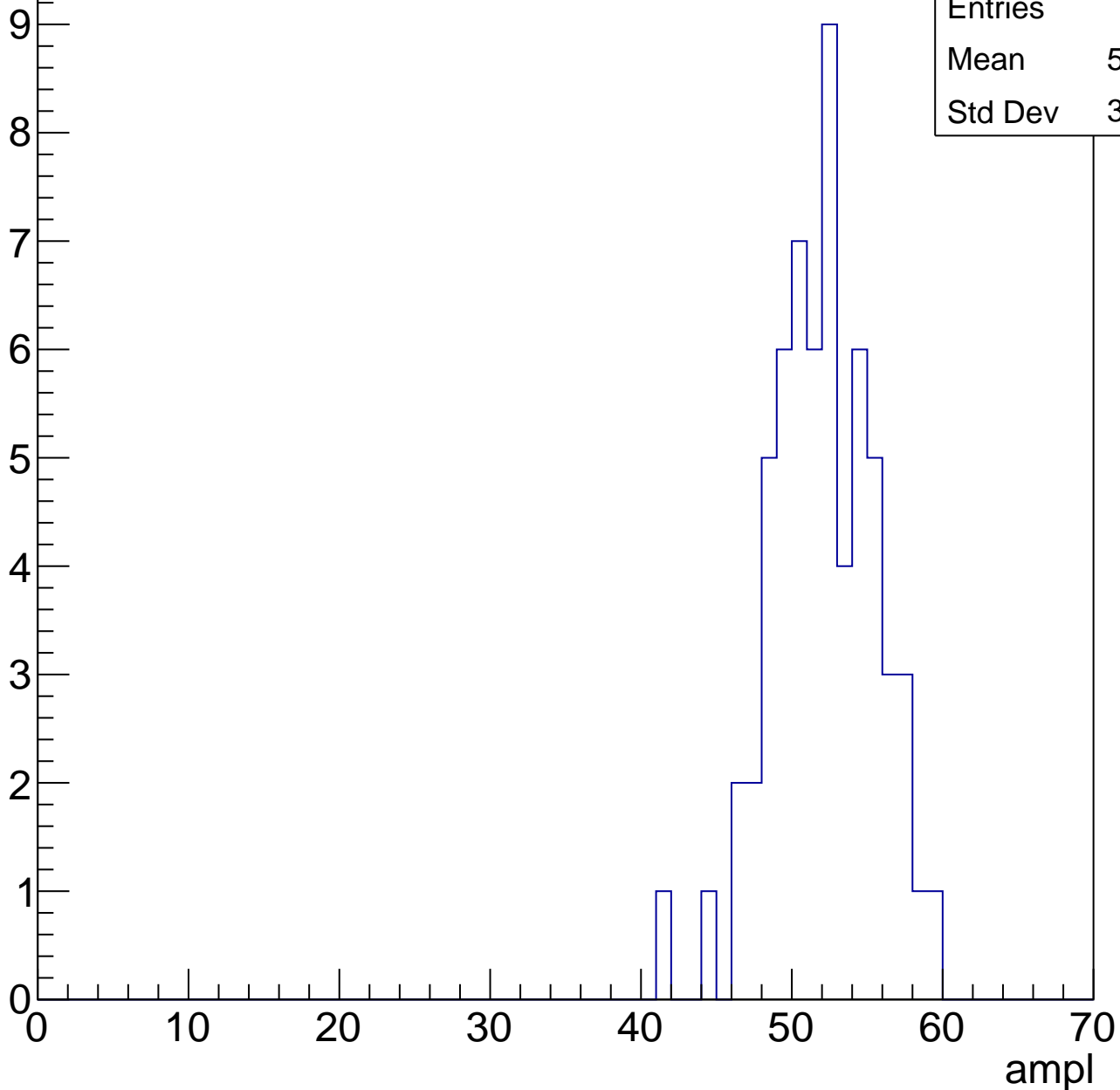


# B1L103S, U11-ch27, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	51.55
Std Dev	3.463

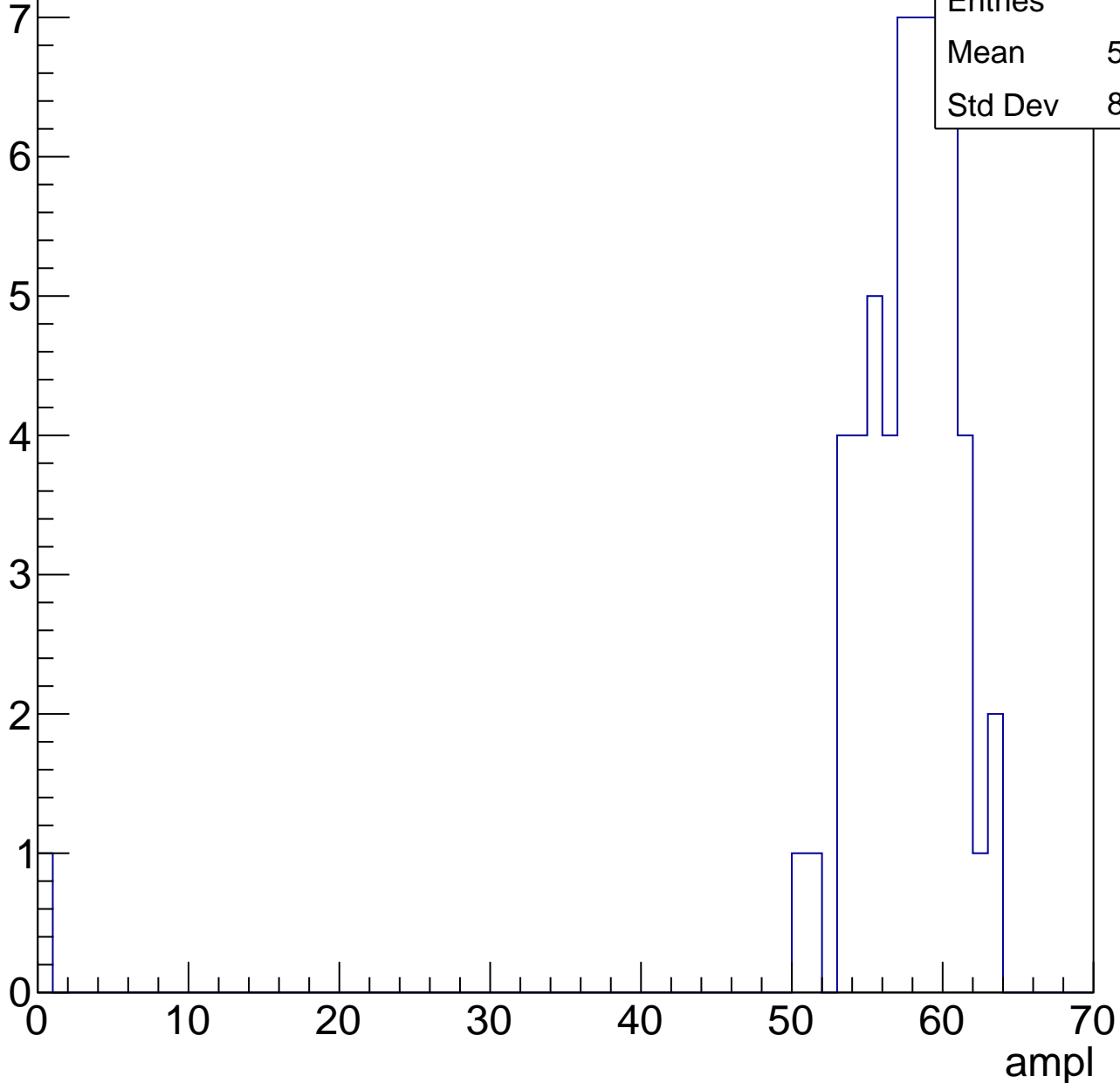


# B1L103S, U11-ch27, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	55
Mean	56.33
Std Dev	8.193

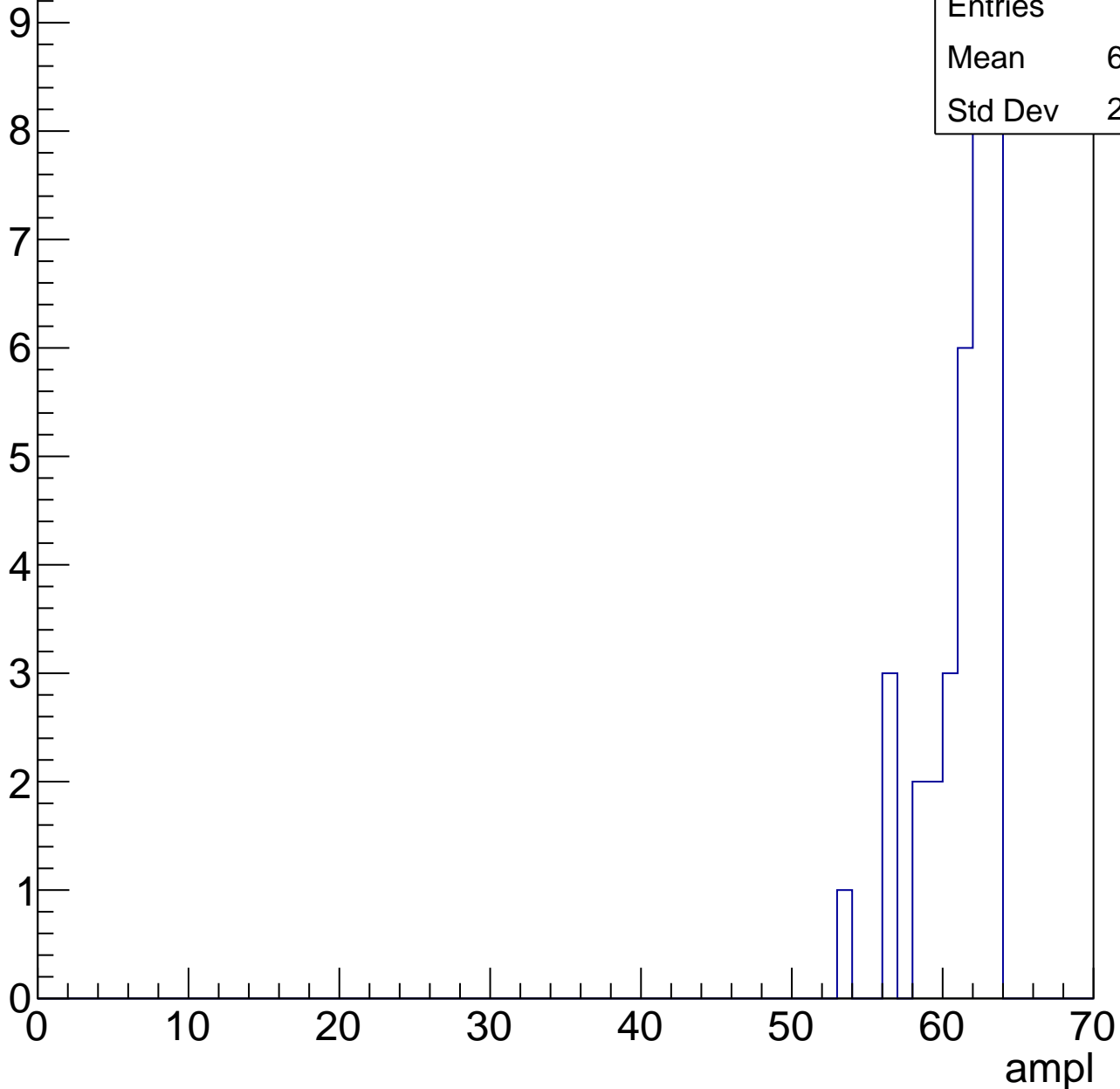


# B1L103S, U11-ch27, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	34
Mean	60.68
Std Dev	2.458



# B1L103S, U11-ch27, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0



# B1L103S, U11-ch27, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U11-ch28, adc0

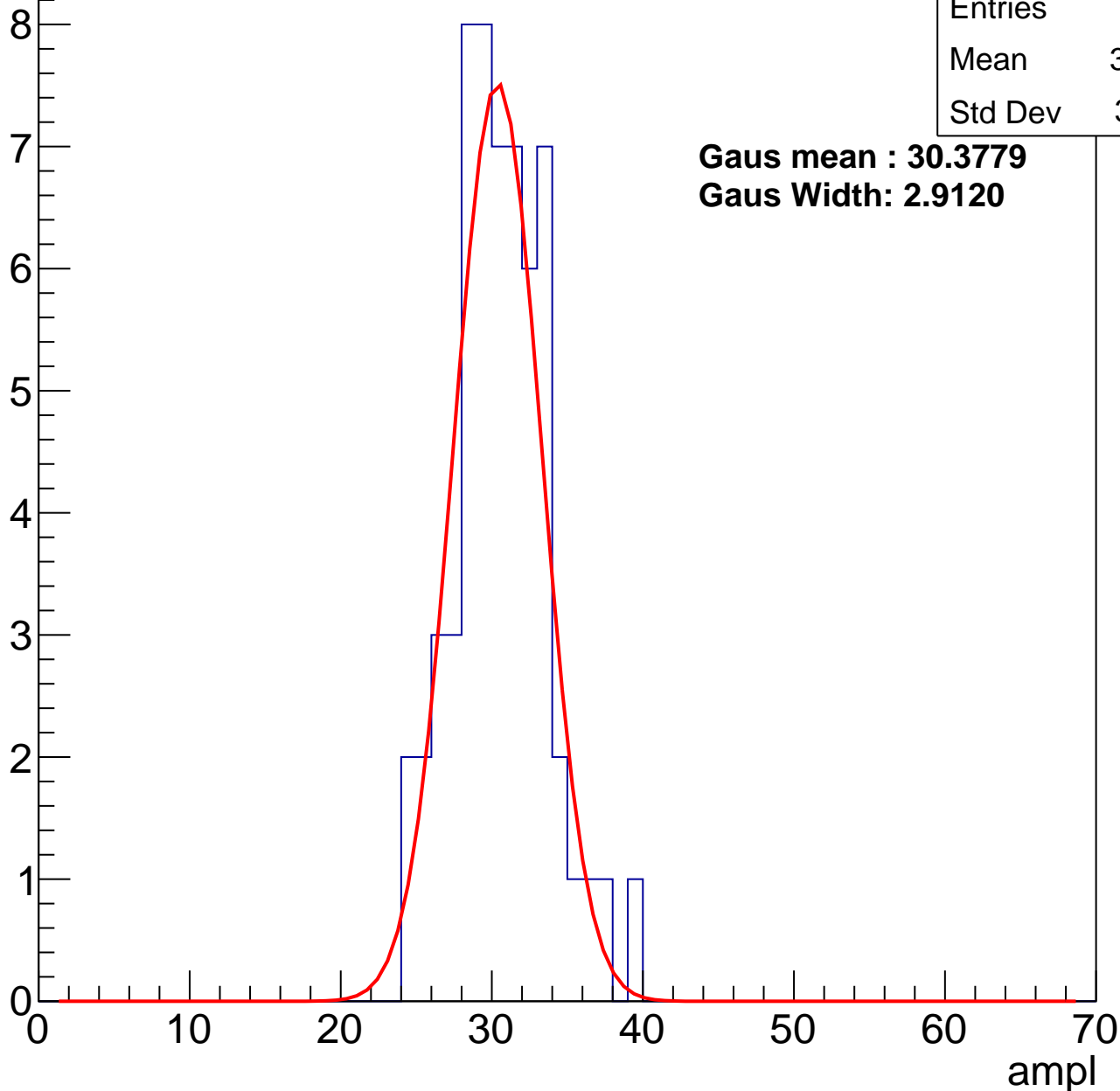
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	59
Mean	30.14
Std Dev	3.061

**Gaus mean : 30.3779**

**Gaus Width: 2.9120**



# B1L103S, U11-ch28, adc1

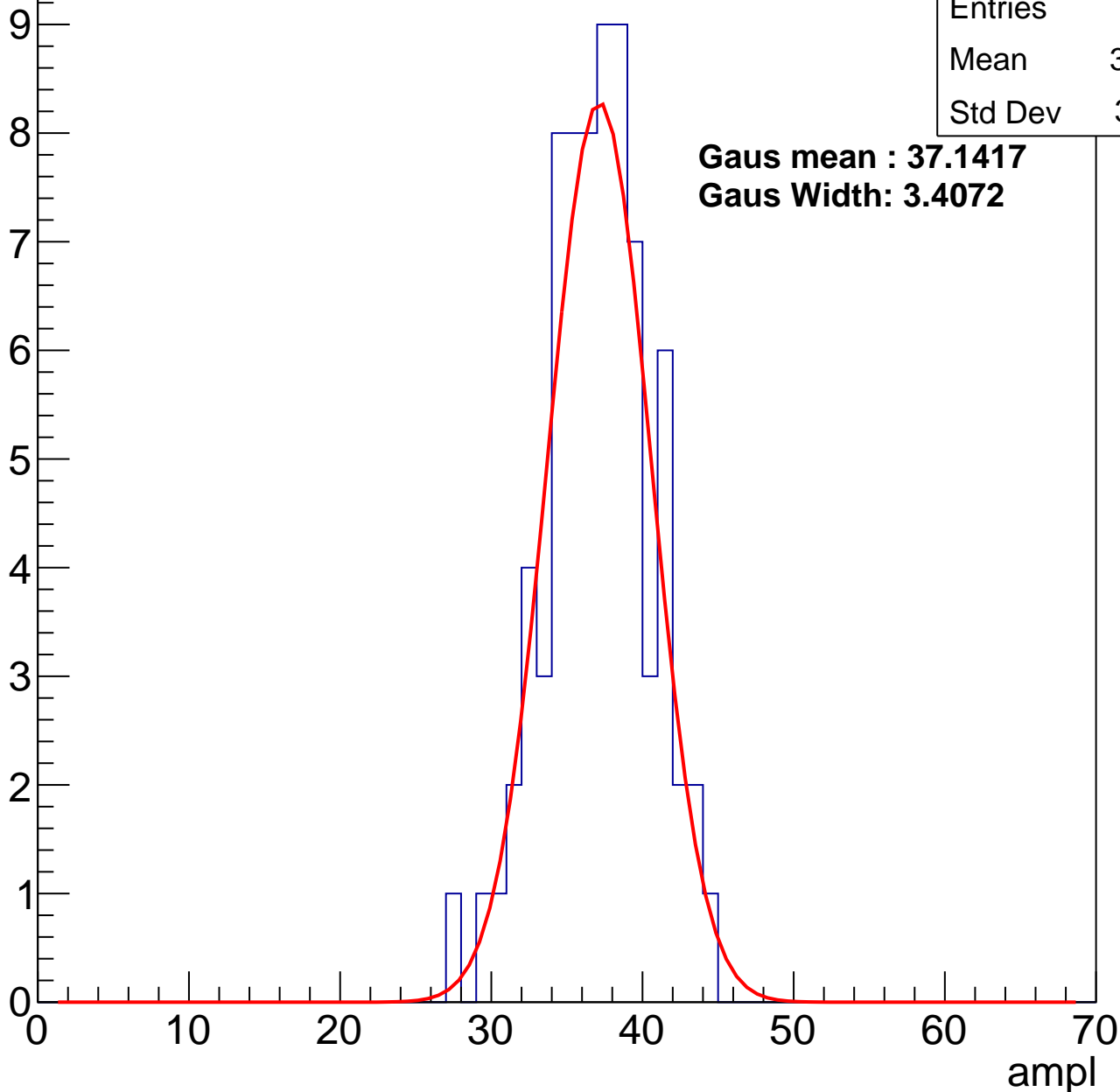
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	75
Mean	36.57
Std Dev	3.391

**Gaus mean : 37.1417**

**Gaus Width: 3.4072**



# B1L103S, U11-ch28, adc2

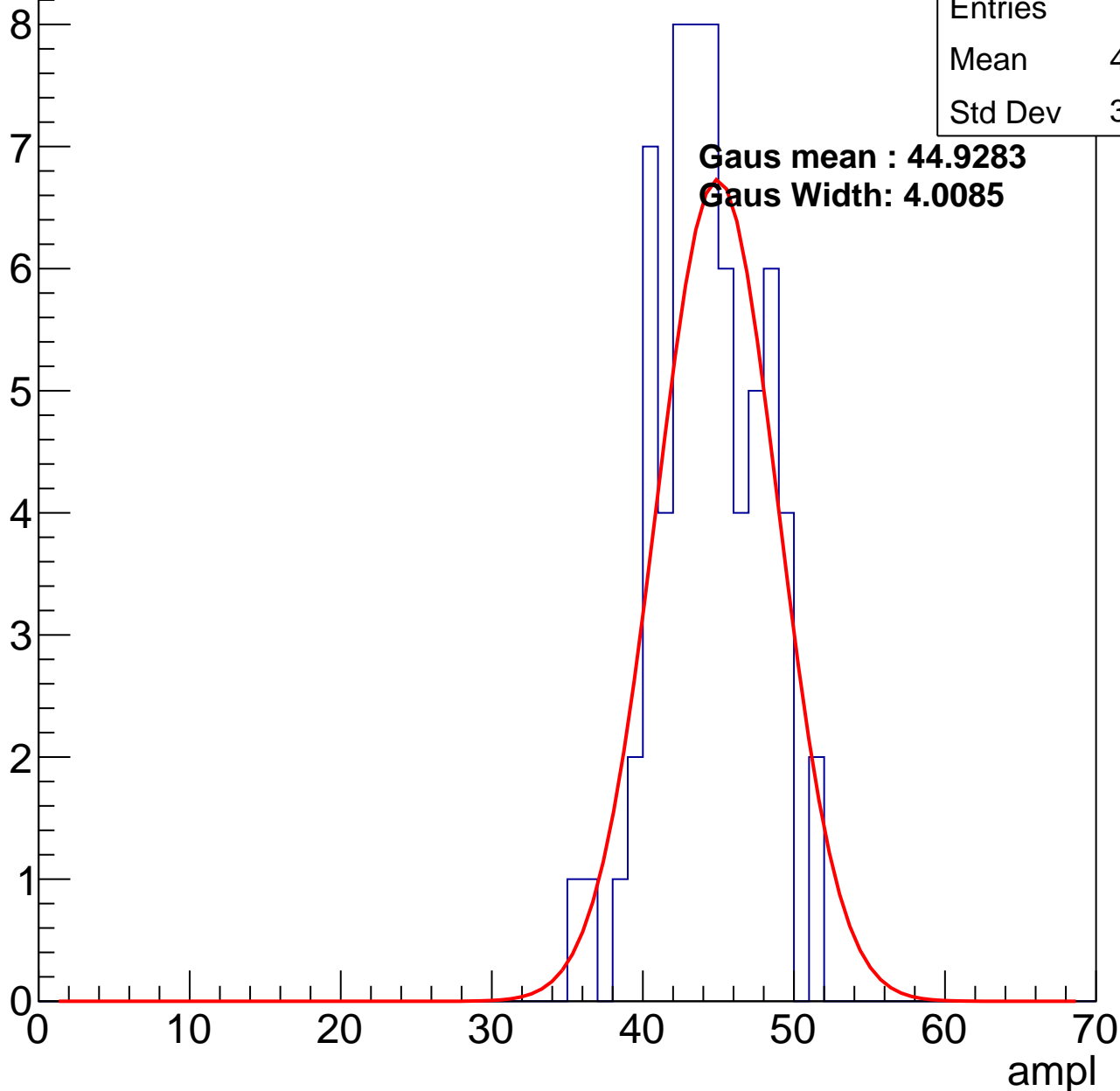
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	43.85
Std Dev	3.409

**Gaus mean : 44.9283**

**Gaus Width: 4.0085**

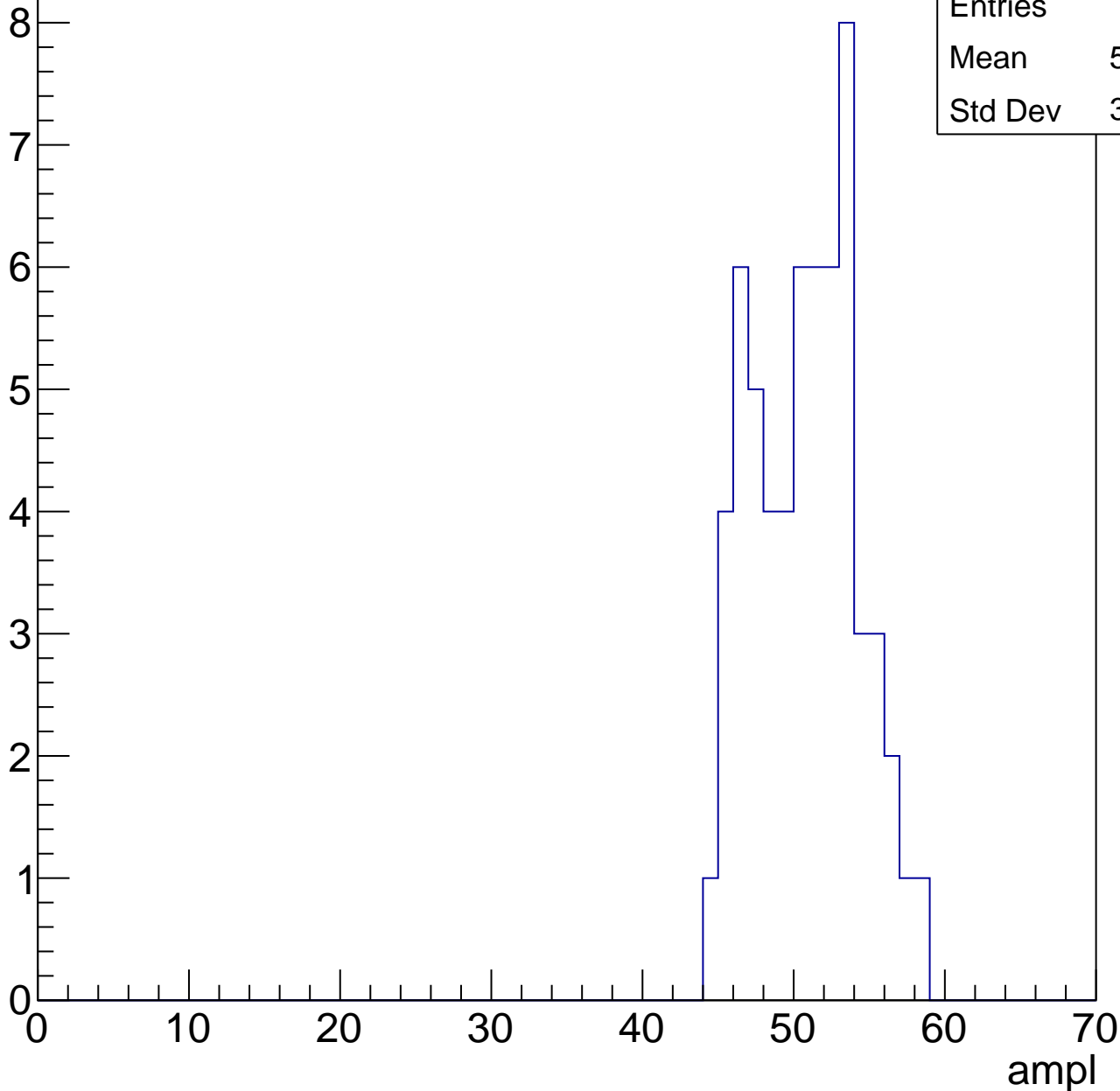


# B1L103S, U11-ch28, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	60
Mean	50.32
Std Dev	3.418

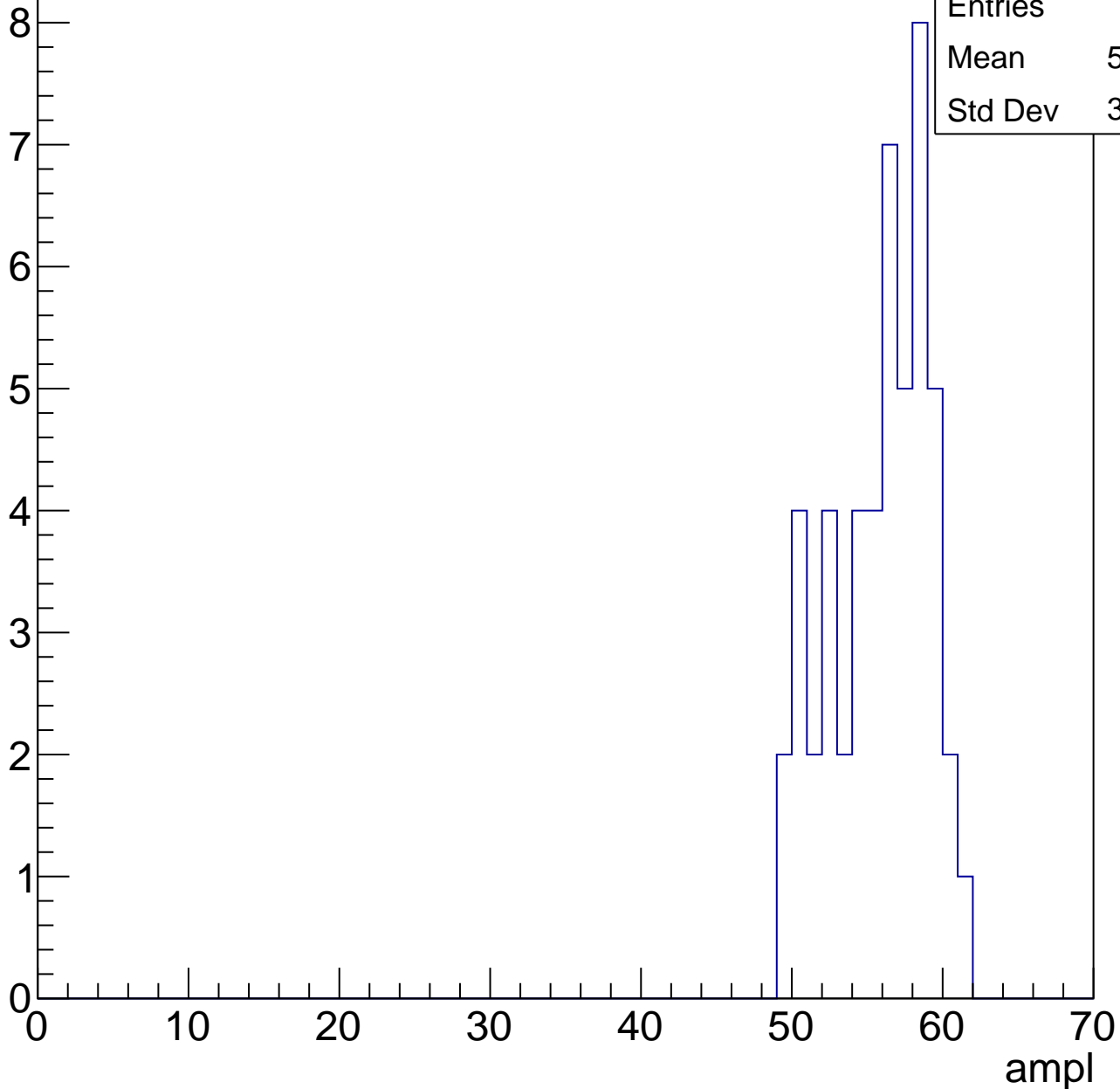


# B1L103S, U11-ch28, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

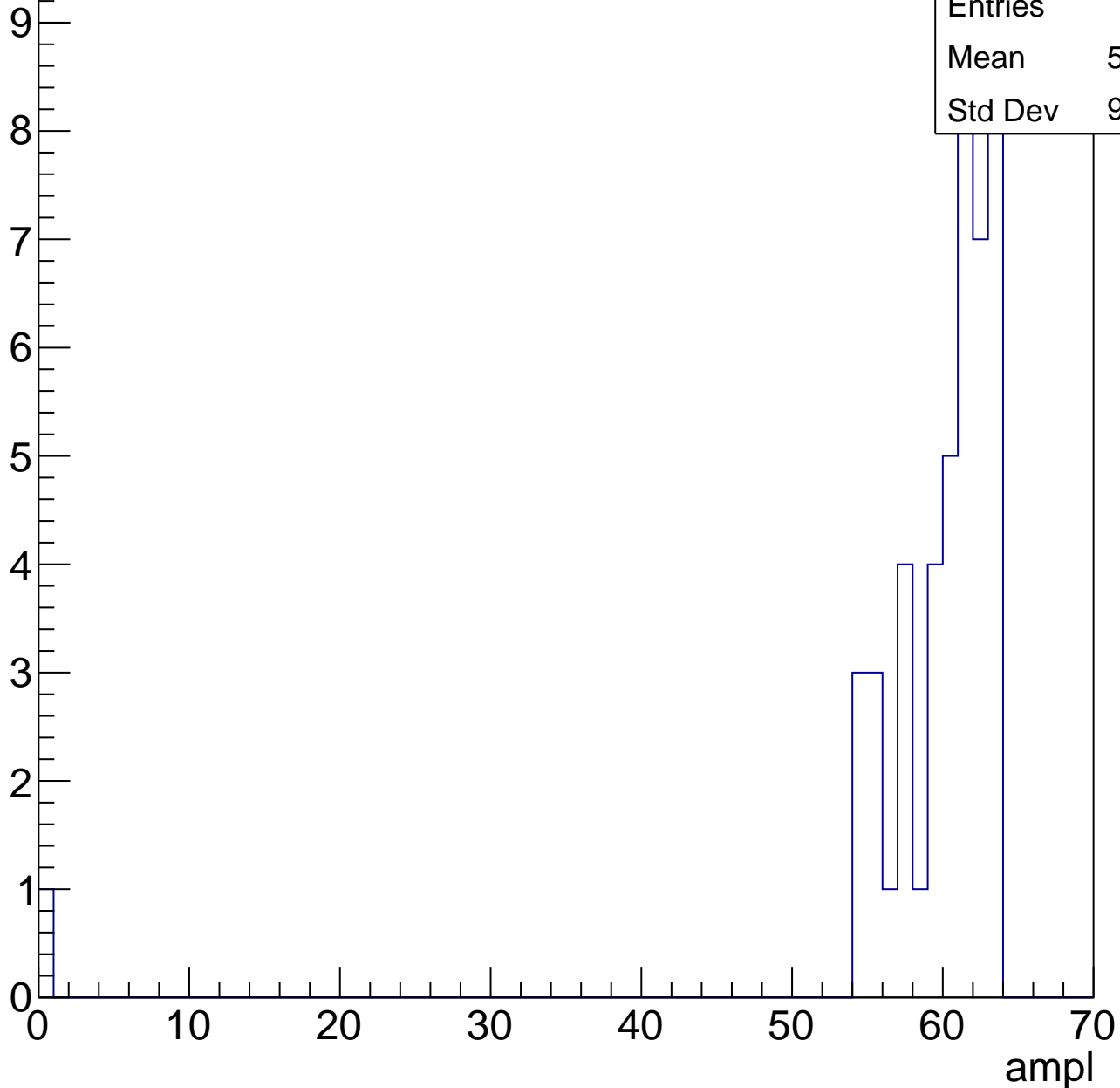
Entries	50
Mean	55.34
Std Dev	3.198



# B1L103S, U11-ch28, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

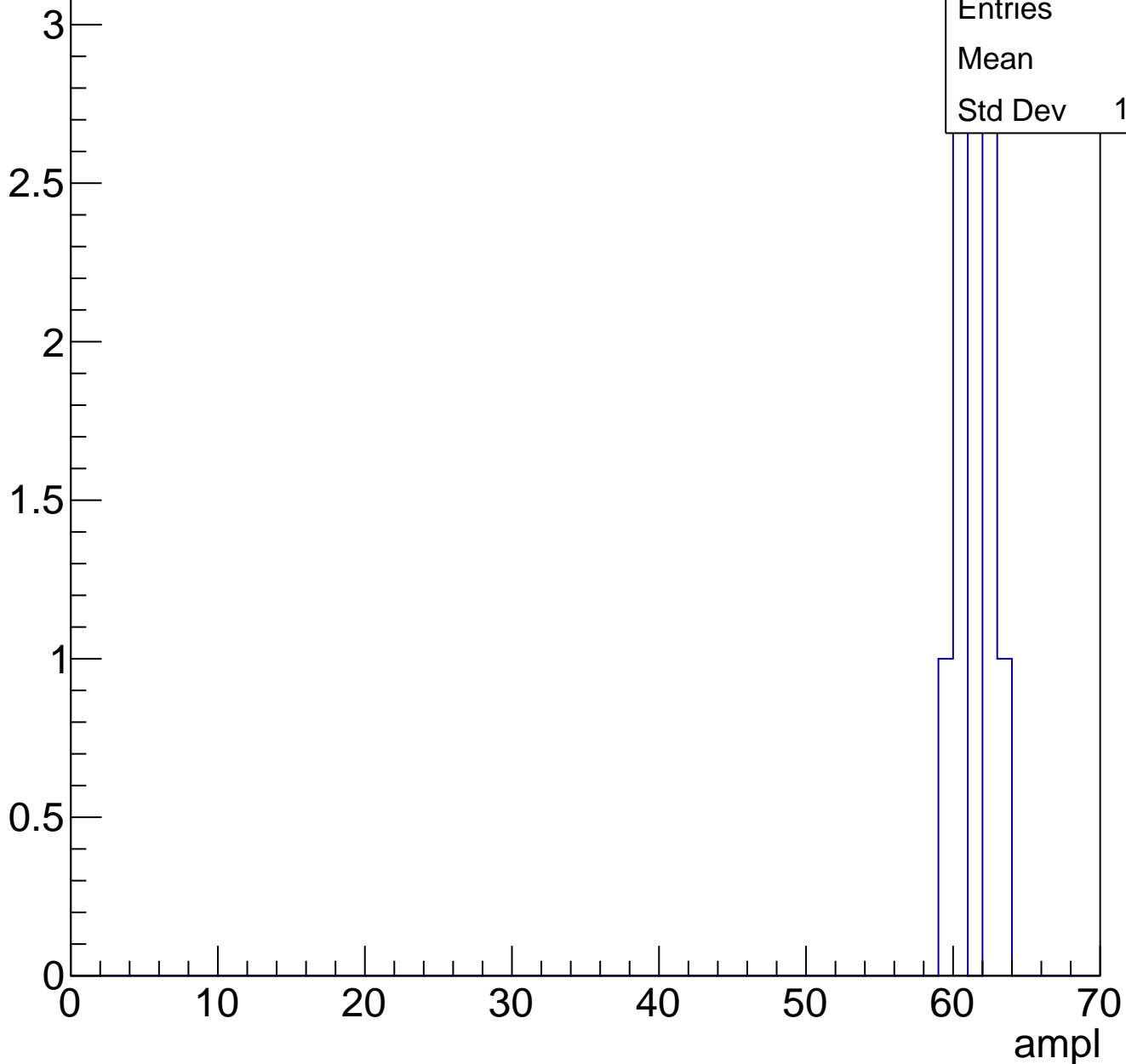
Entry



# B1L103S, U11-ch28, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U11-ch28, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U11-ch29, adc0

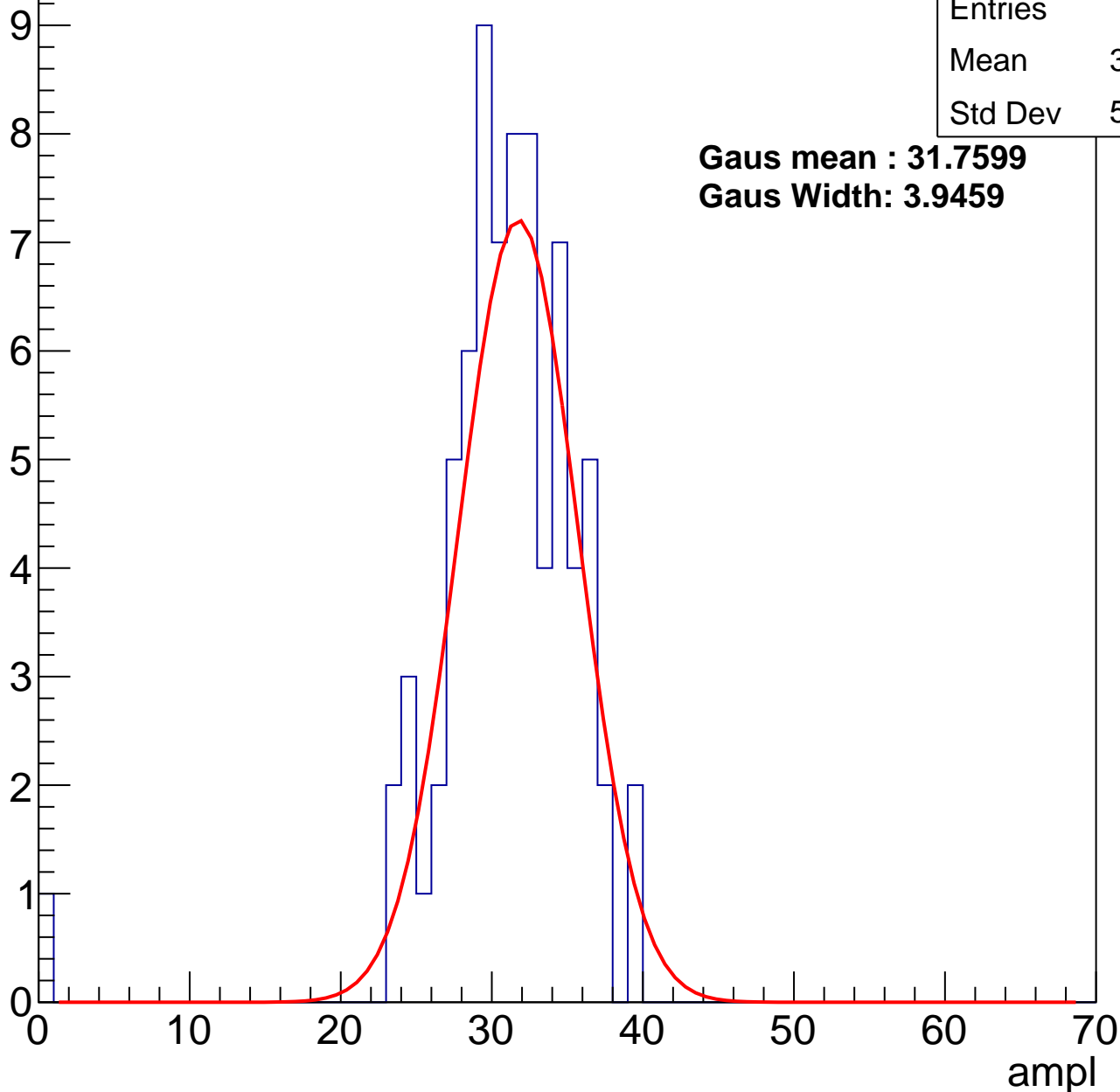
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	76
Mean	30.46
Std Dev	5.069

**Gaus mean : 31.7599**

**Gaus Width: 3.9459**



# B1L103S, U11-ch29, adc1

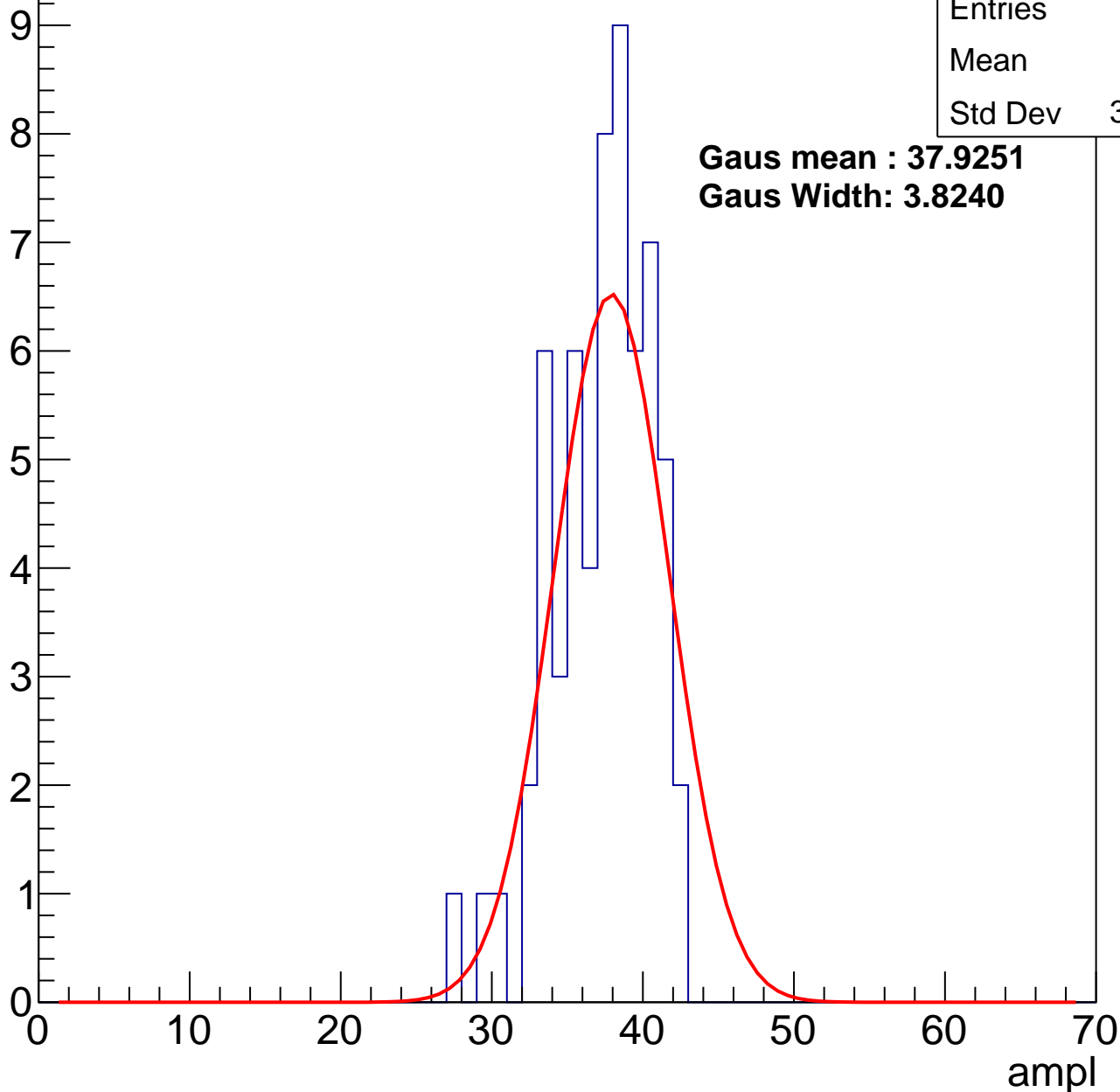
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	61
Mean	36.8
Std Dev	3.233

**Gaus mean : 37.9251**

**Gaus Width: 3.8240**



# B1L103S, U11-ch29, adc2

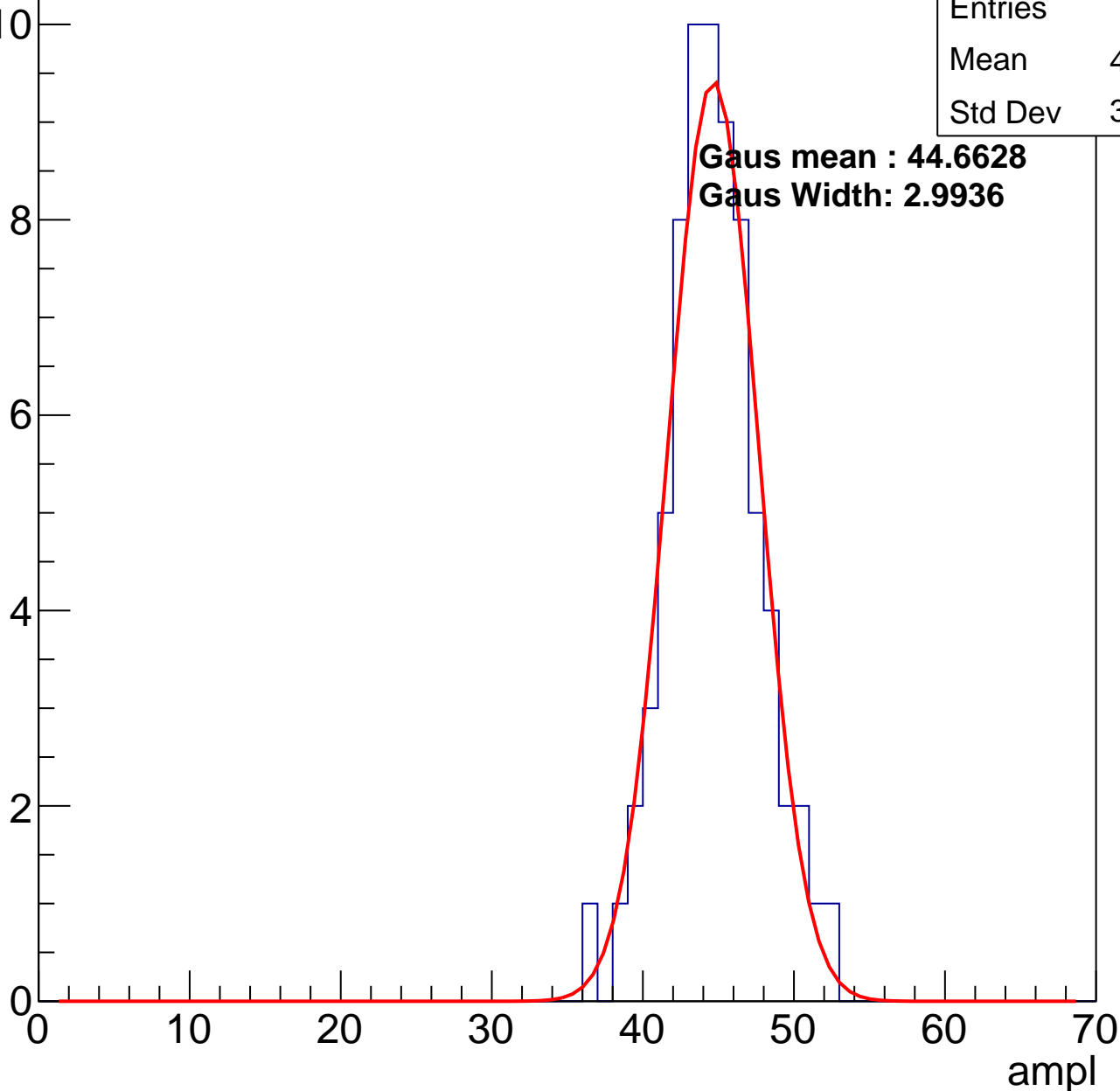
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	72
Mean	44.22
Std Dev	3.042

**Gaus mean : 44.6628**

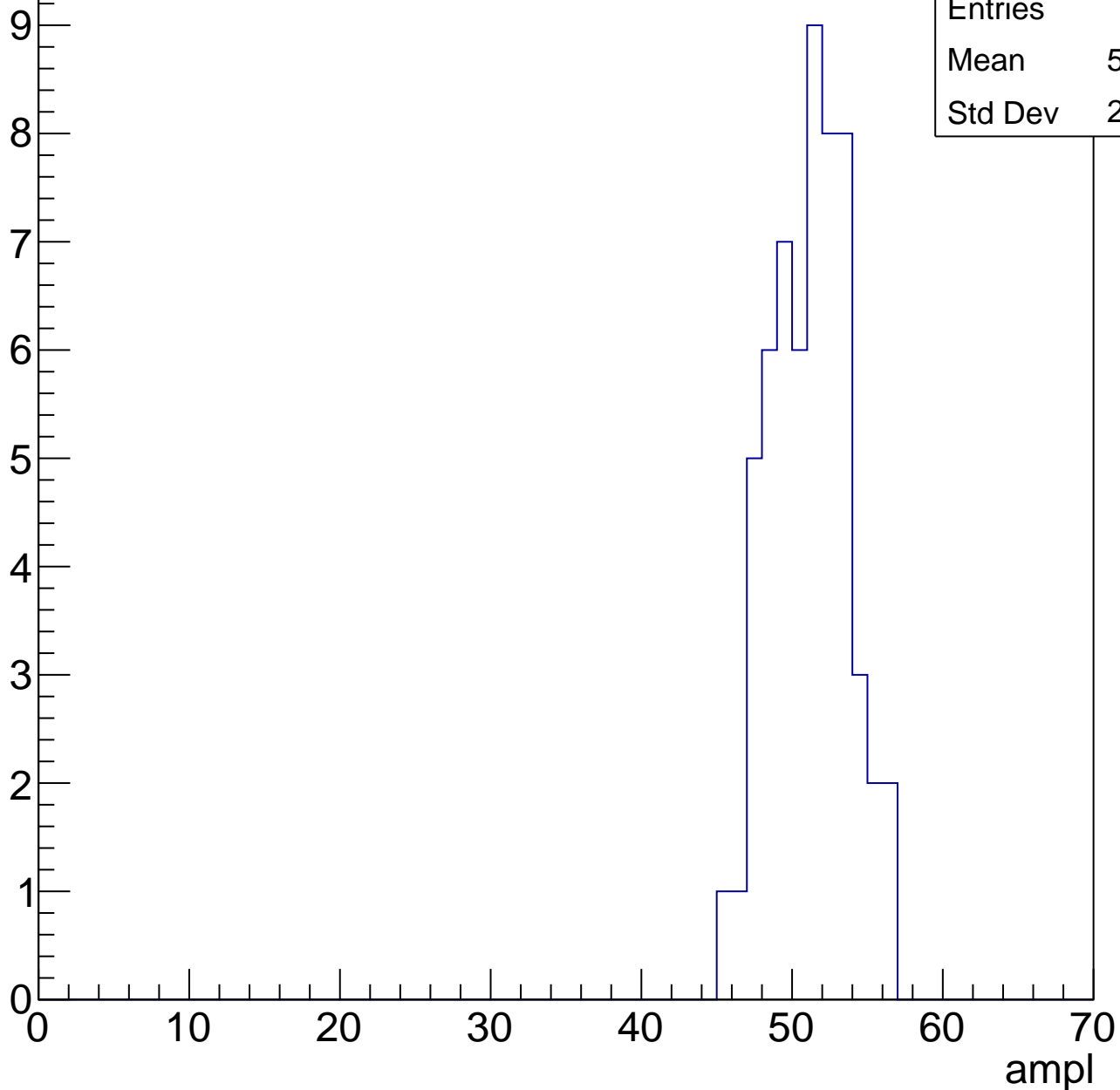
**Gaus Width: 2.9936**



# B1L103S, U11-ch29, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



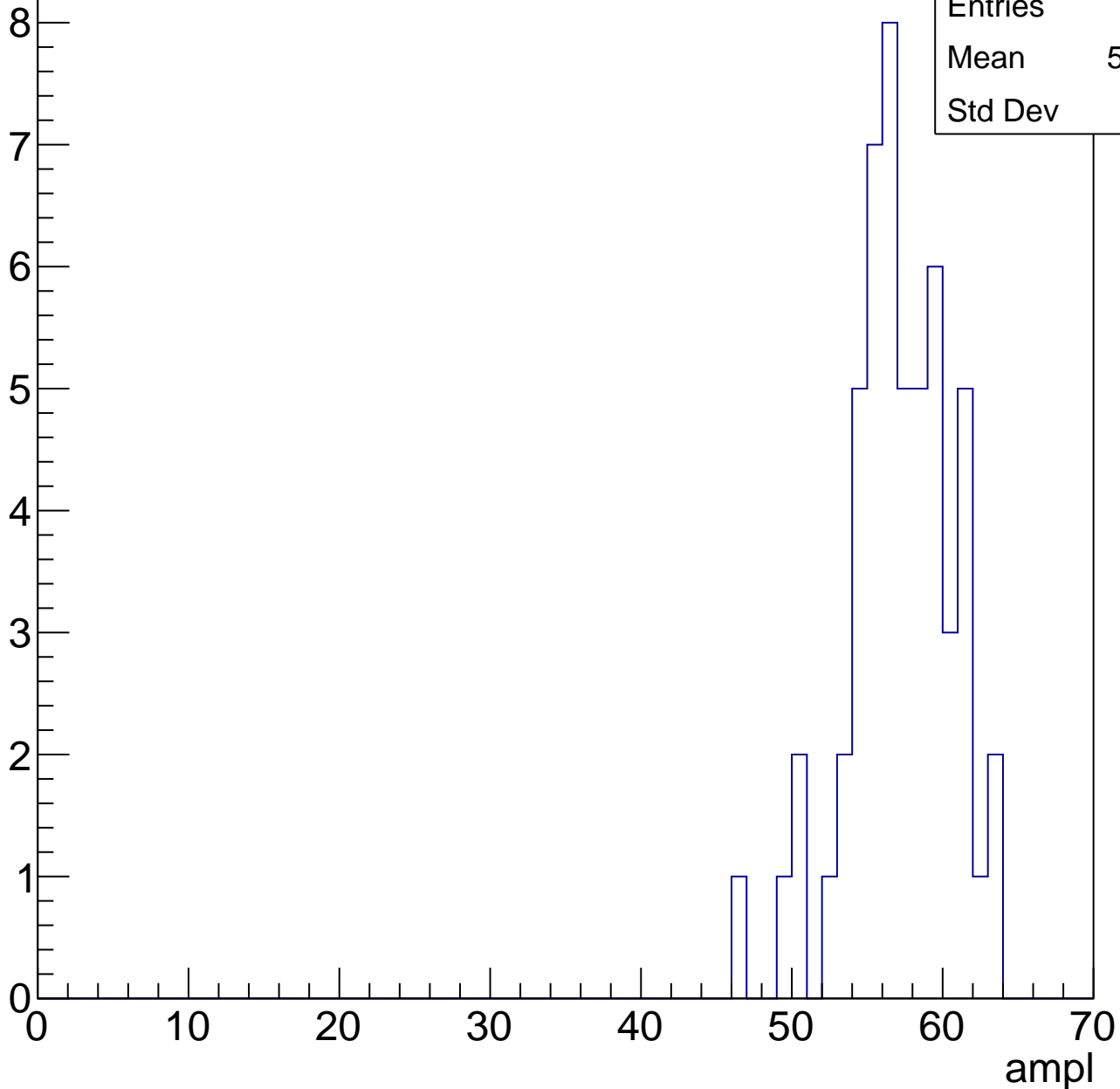
Entries	58
Mean	50.69
Std Dev	2.534

# B1L103S, U11-ch29, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	54
Mean	56.63
Std Dev	3.46

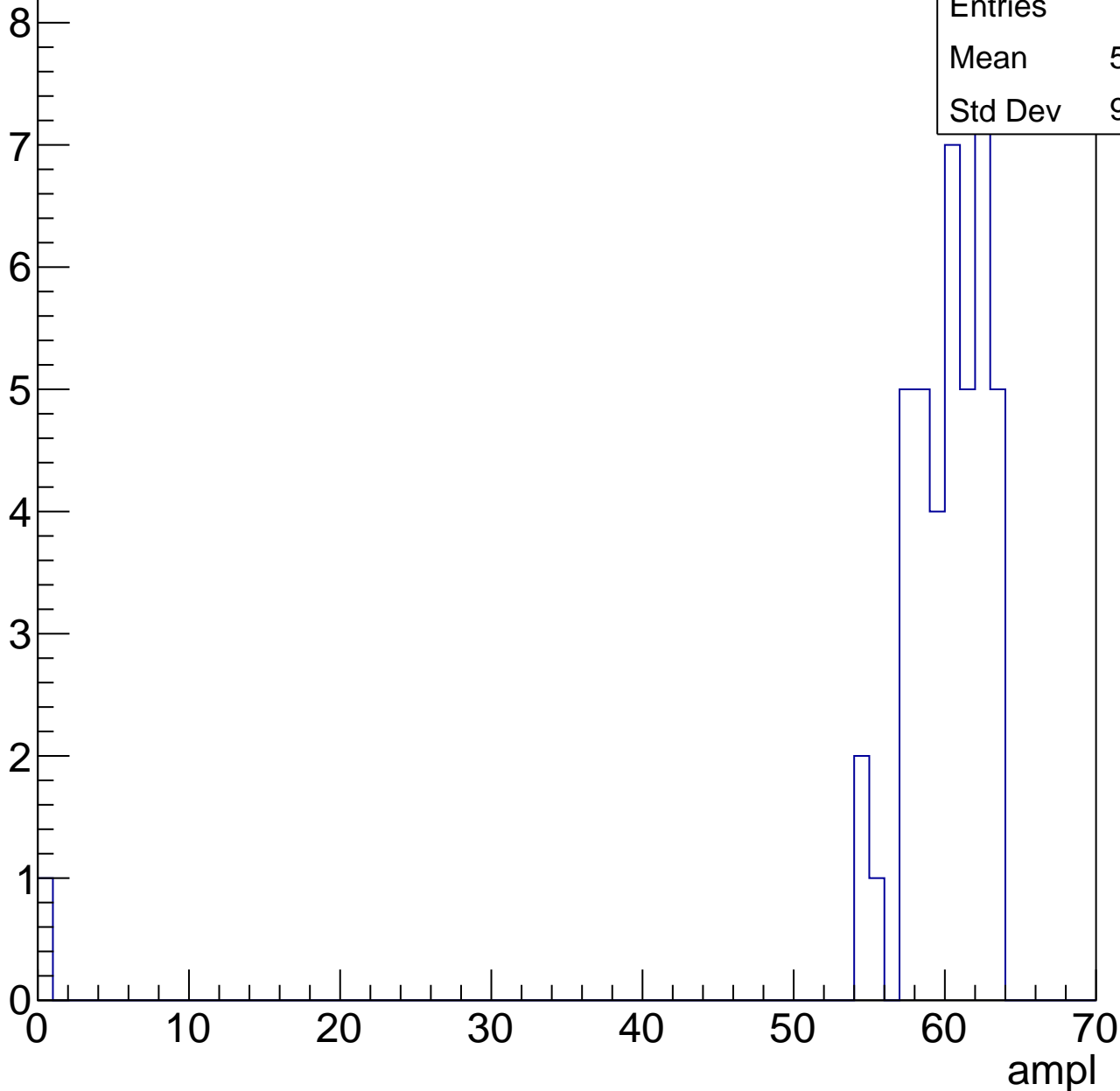


# B1L103S, U11-ch29, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	43
Mean	58.37
Std Dev	9.319



# B1L103S, U11-ch29, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U11-ch29, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U11-ch30, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	84
Mean	30.73
Std Dev	3.708

**Gaus mean : 30.7625**

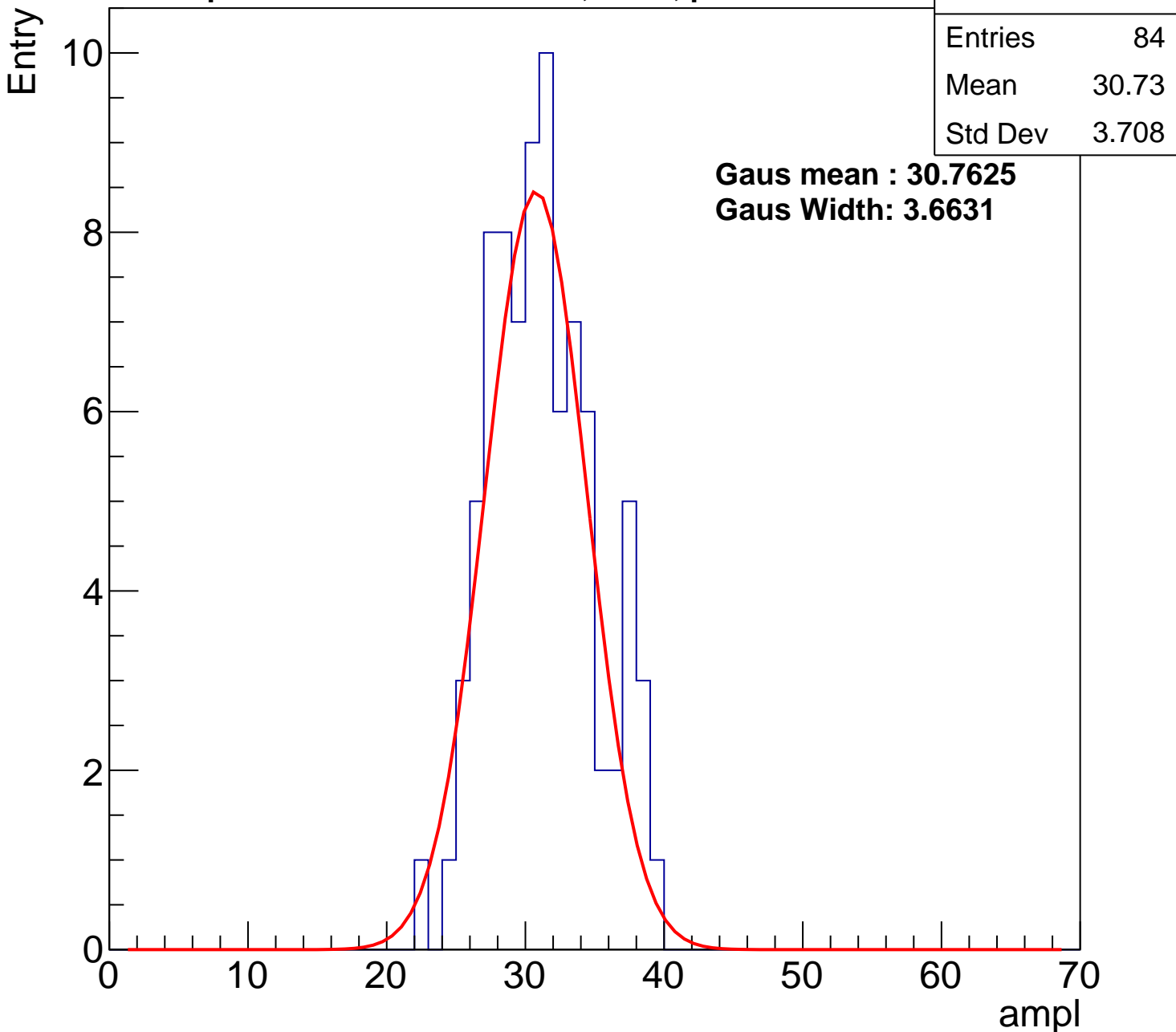
**Gaus Width: 3.6631**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U11-ch30, adc1

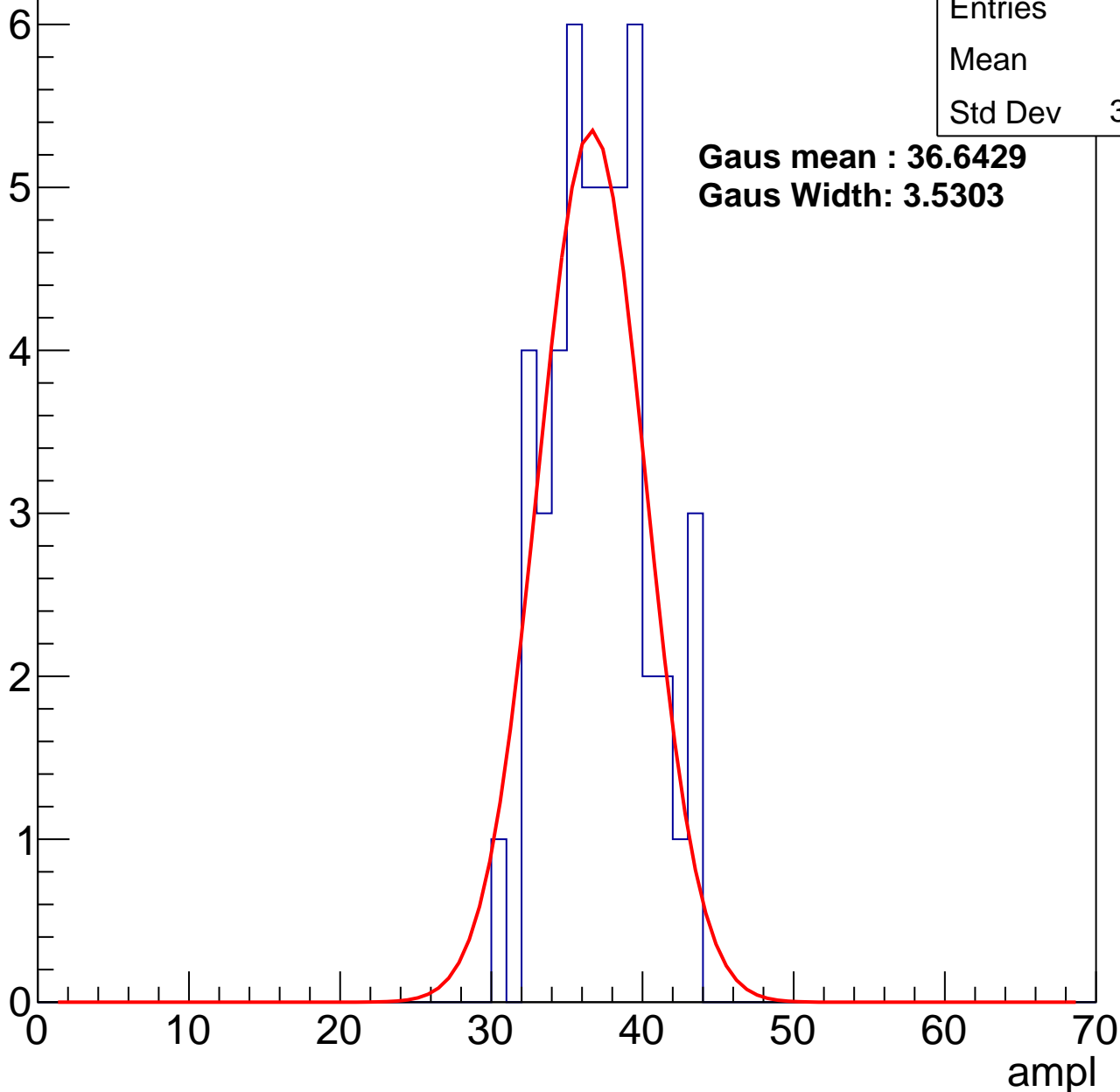
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	47
Mean	36.7
Std Dev	3.162

**Gaus mean : 36.6429**

**Gaus Width: 3.5303**



# B1L103S, U11-ch30, adc2

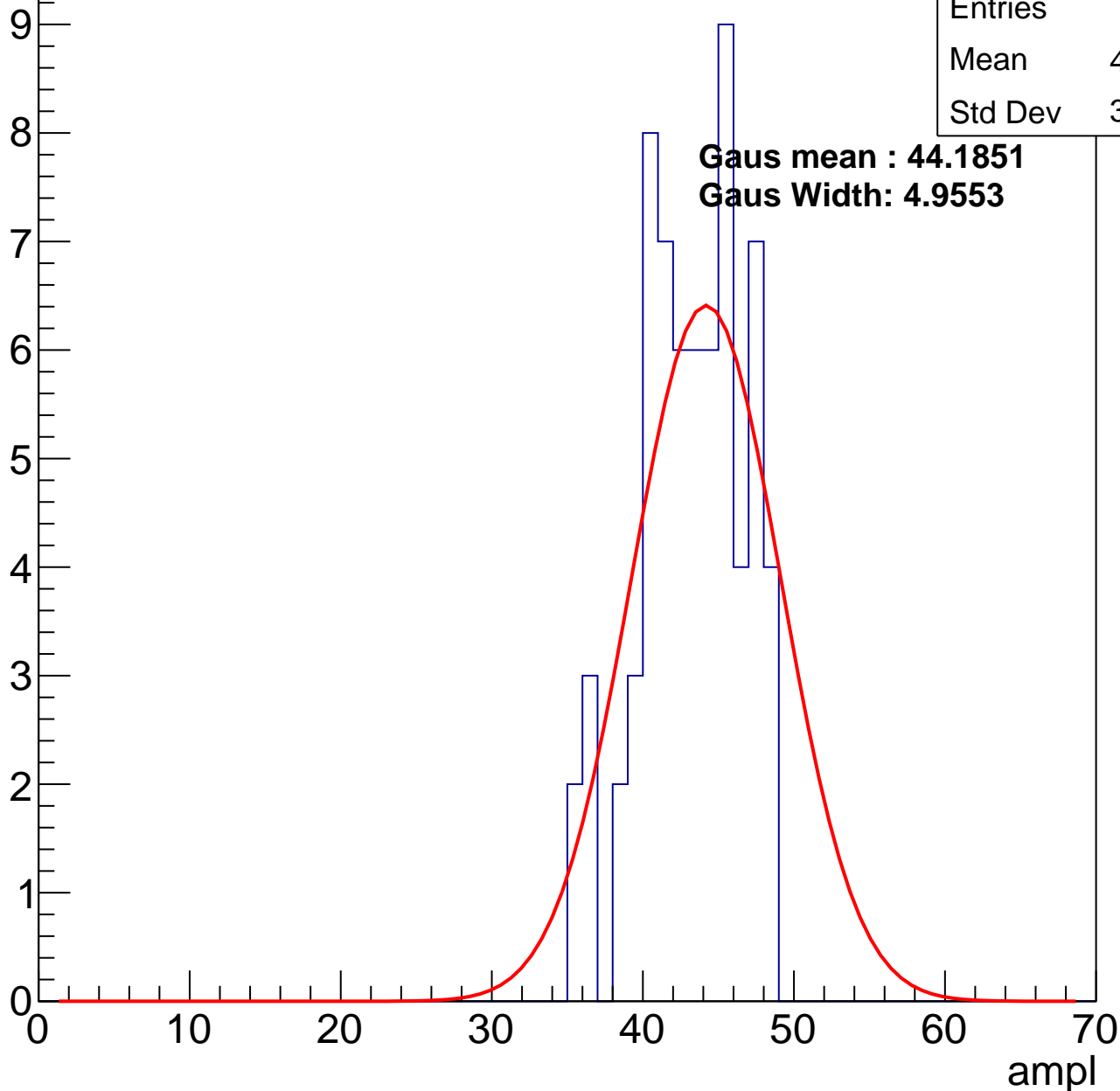
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	42.72
Std Dev	3.376

**Gaus mean : 44.1851**

**Gaus Width: 4.9553**

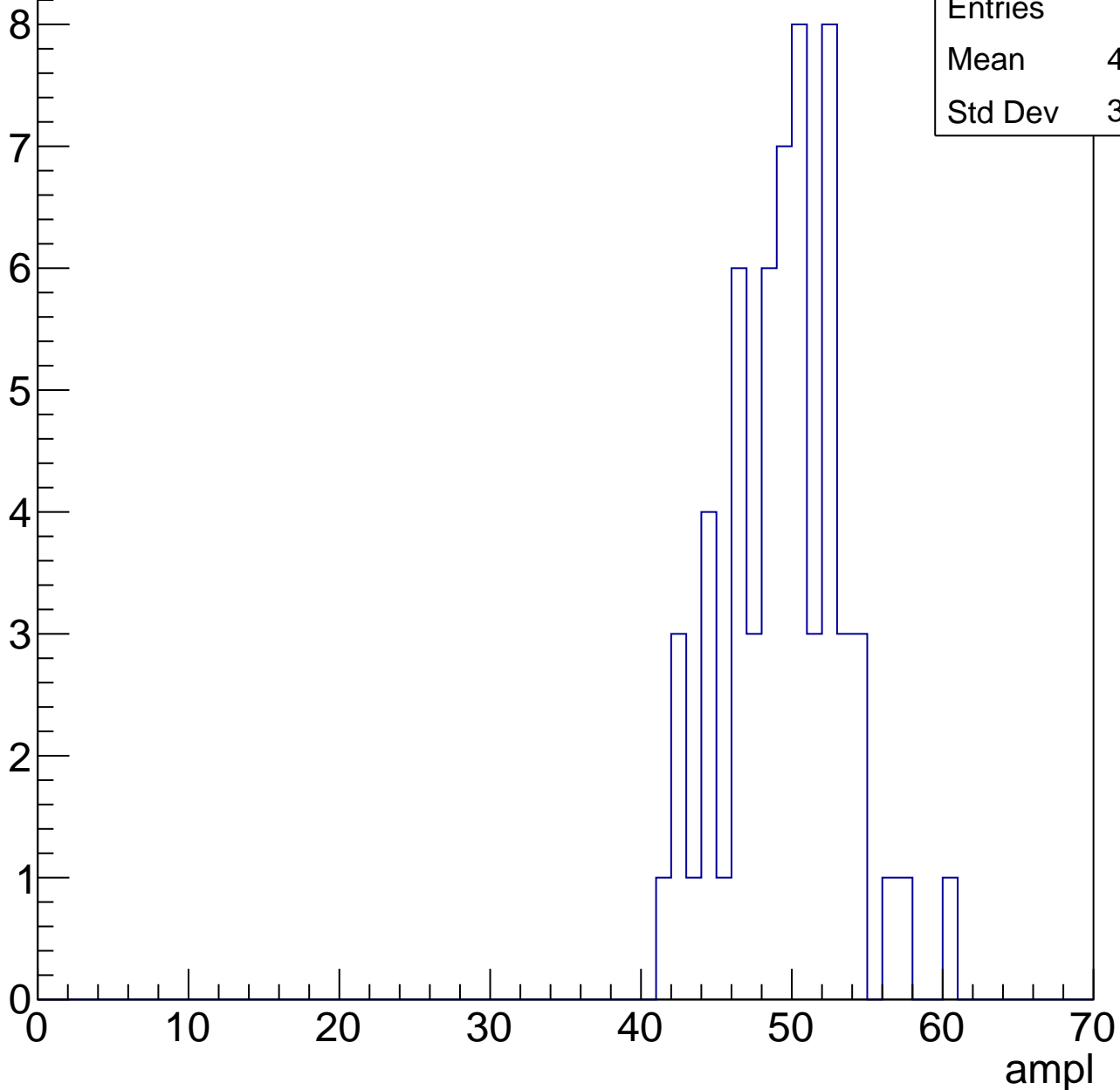


# B1L103S, U11-ch30, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

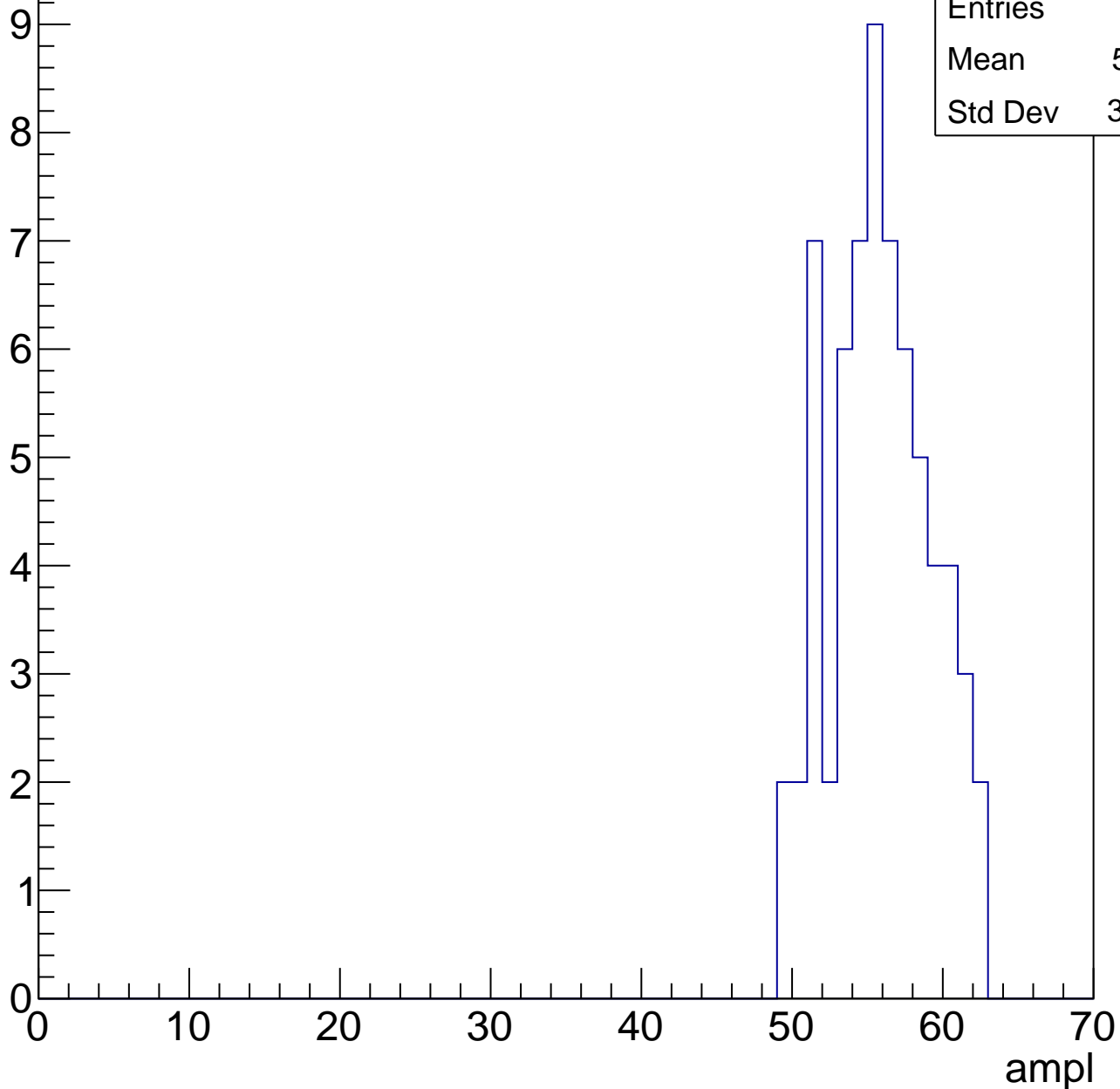
Entries	60
Mean	49.03
Std Dev	3.838



# B1L103S, U11-ch30, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

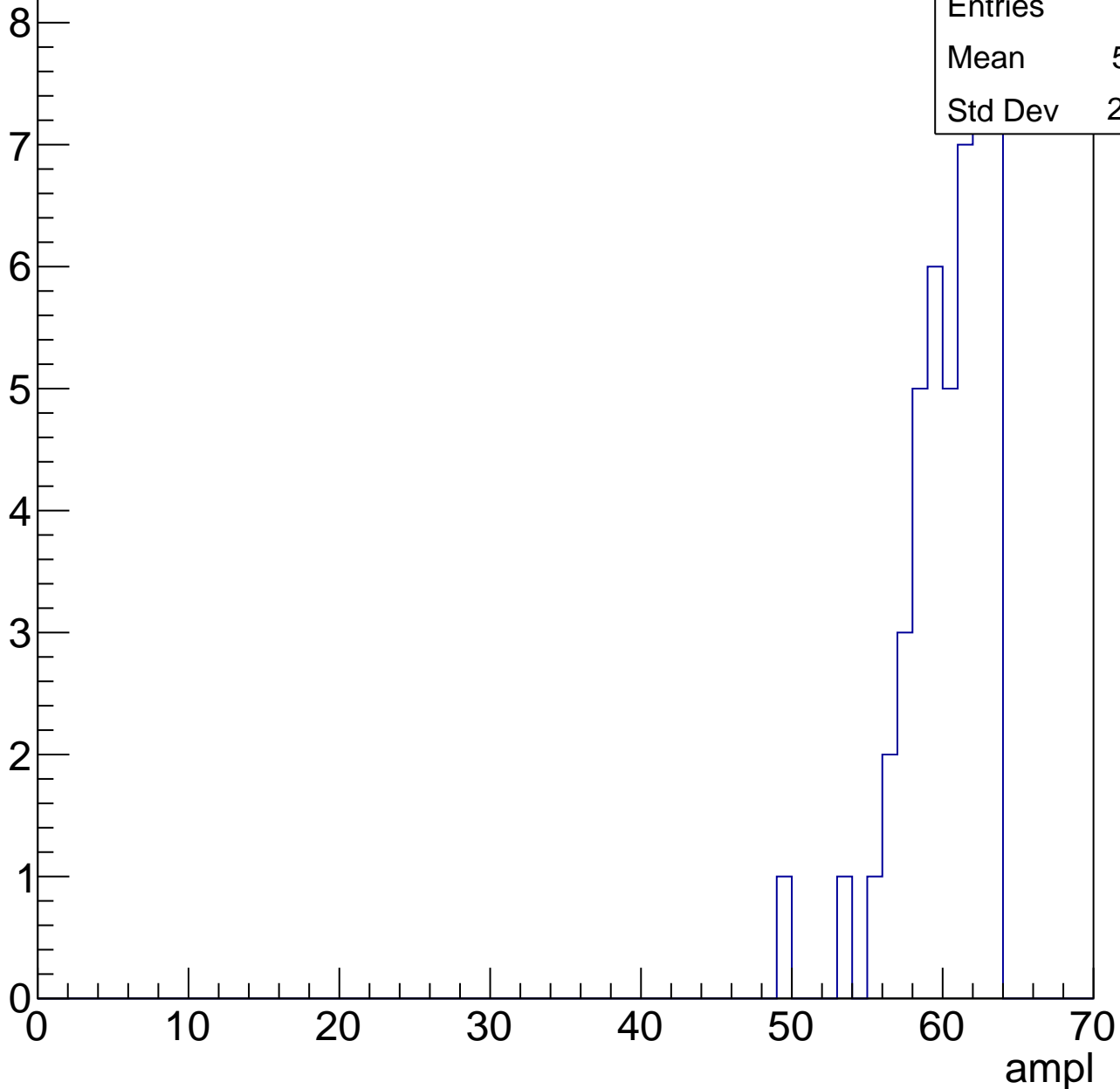


# B1L103S, U11-ch30, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	47
Mean	59.81
Std Dev	2.878



# B1L103S, U11-ch30, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U11-ch30, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U11-ch31, adc0

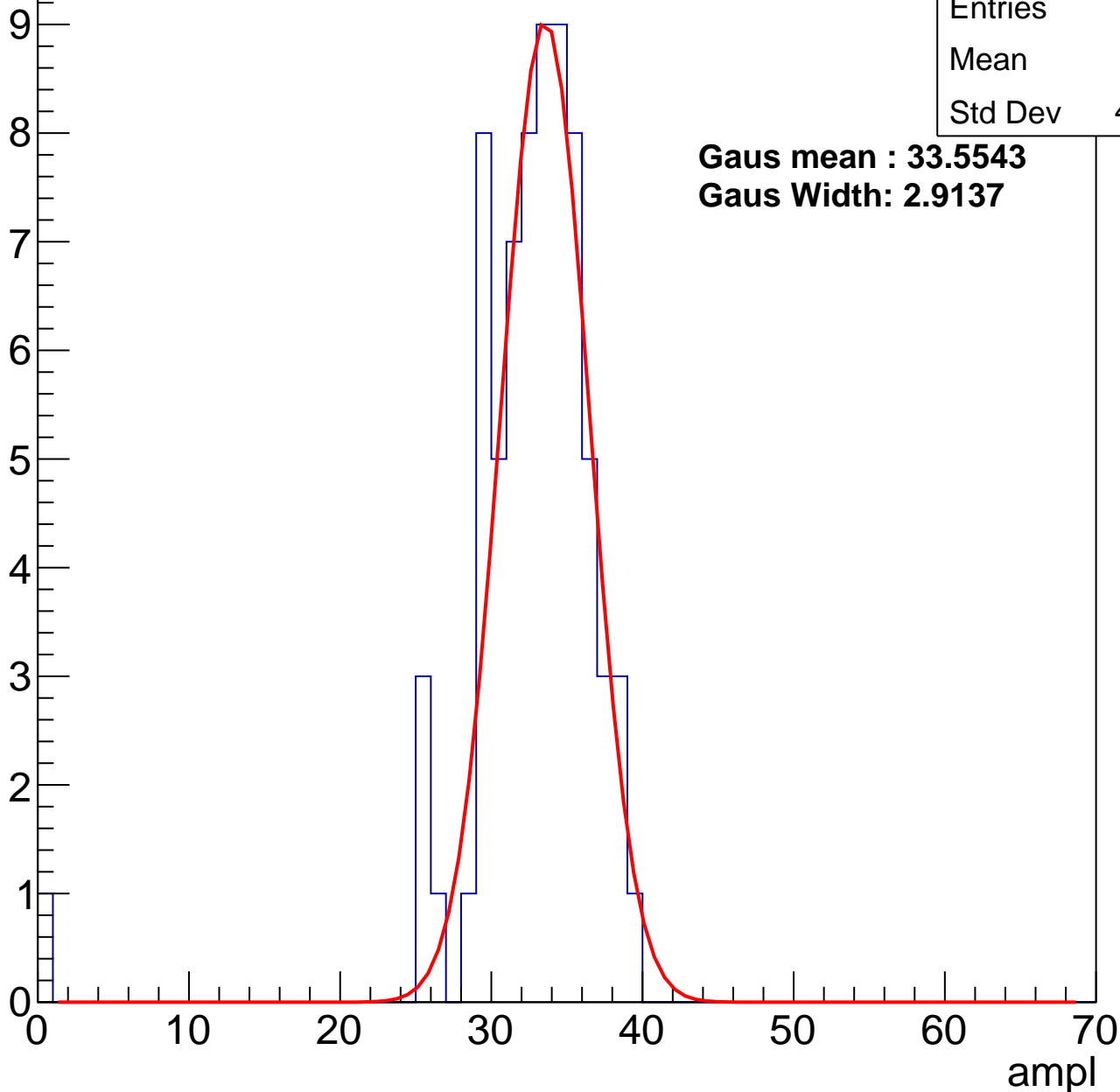
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	72
Mean	32.1
Std Dev	4.931

**Gaus mean : 33.5543**

**Gaus Width: 2.9137**



# B1L103S, U11-ch31, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	60
Mean	39.87
Std Dev	3.09

**Gaus mean : 40.1166**

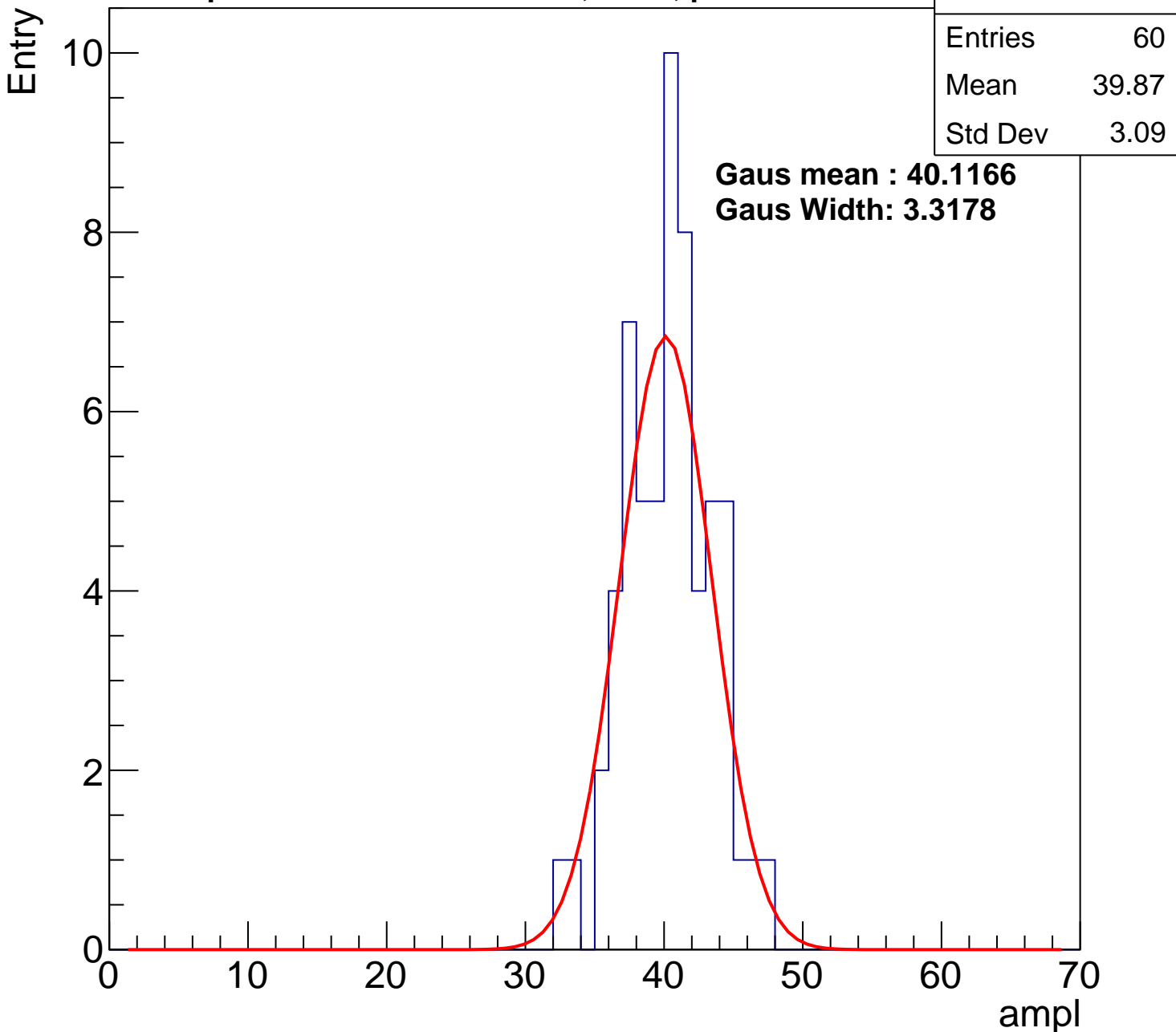
**Gaus Width: 3.3178**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U11-ch31, adc2

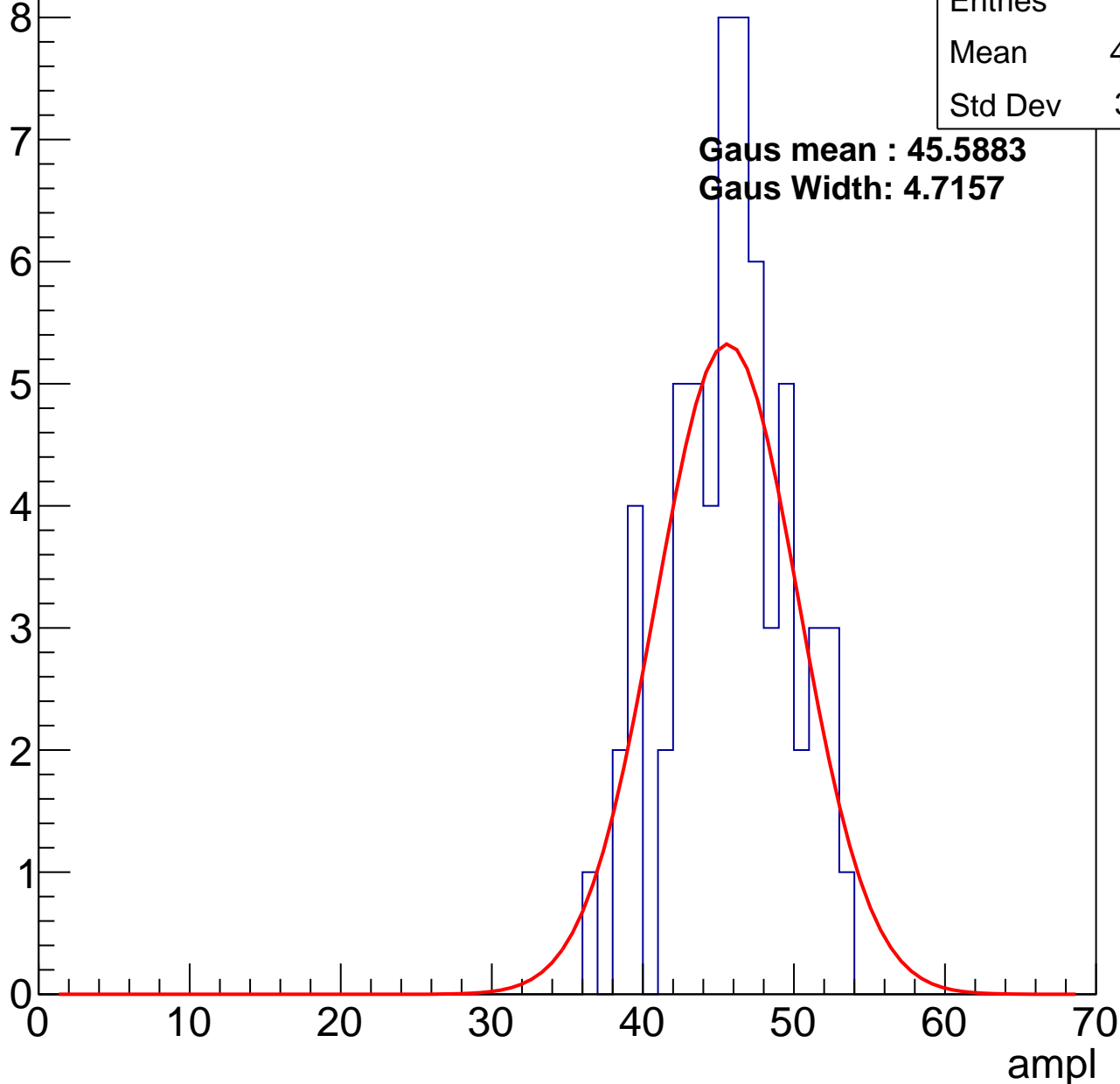
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	45.35
Std Dev	3.861

**Gaus mean : 45.5883**

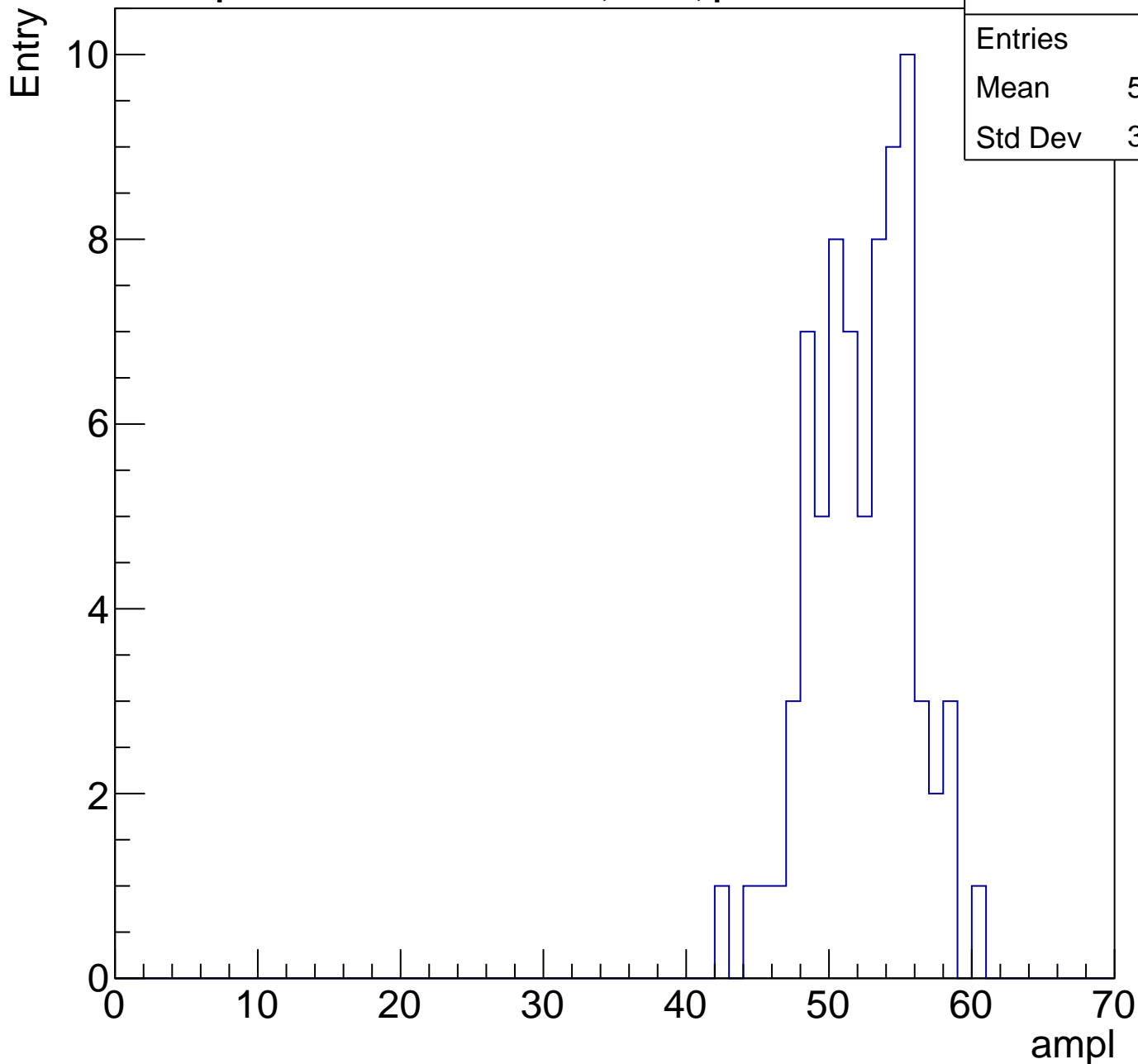
**Gaus Width: 4.7157**



# B1L103S, U11-ch31, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

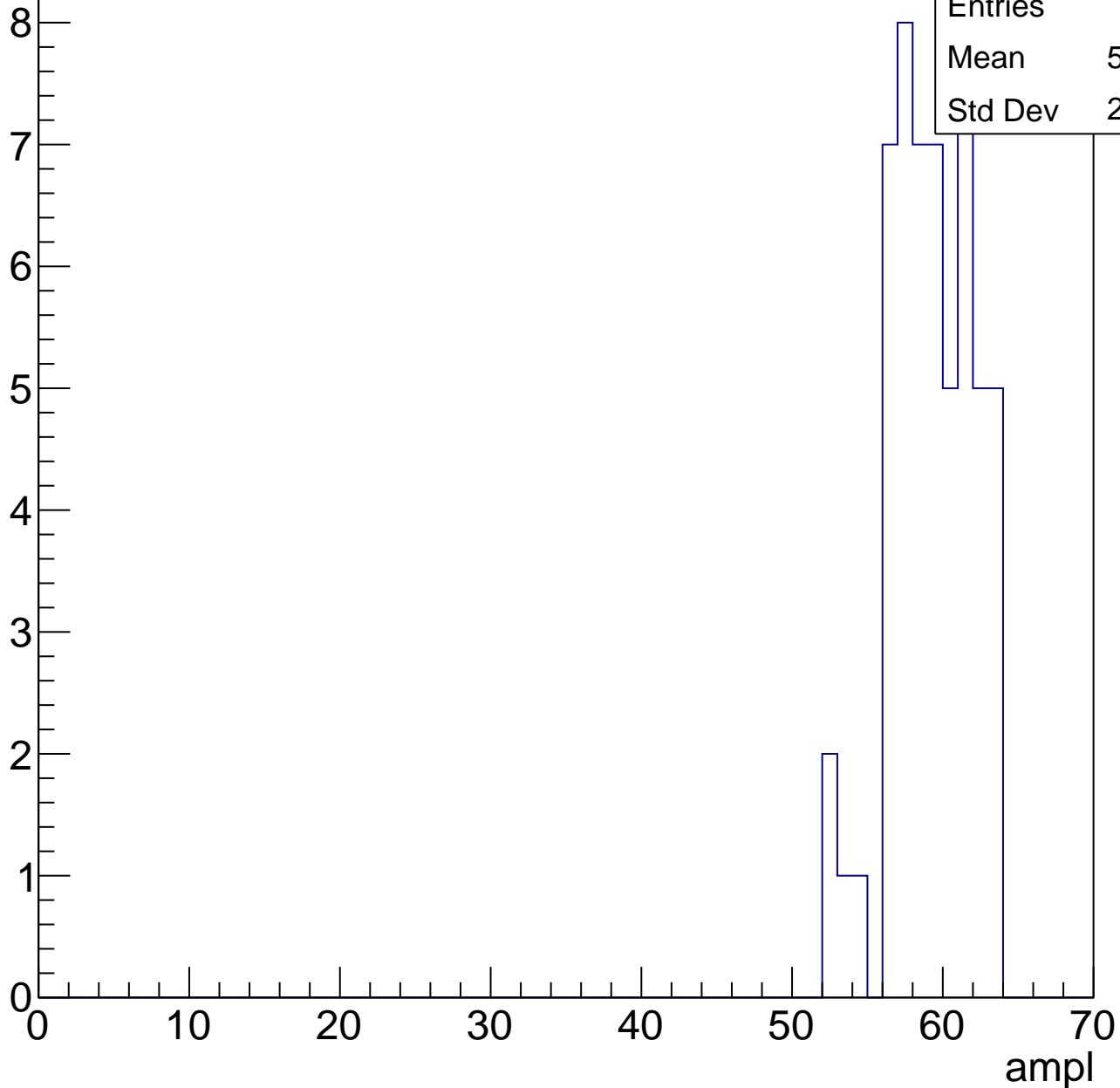
Entries	75
Mean	51.89
Std Dev	3.508



# B1L103S, U11-ch31, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

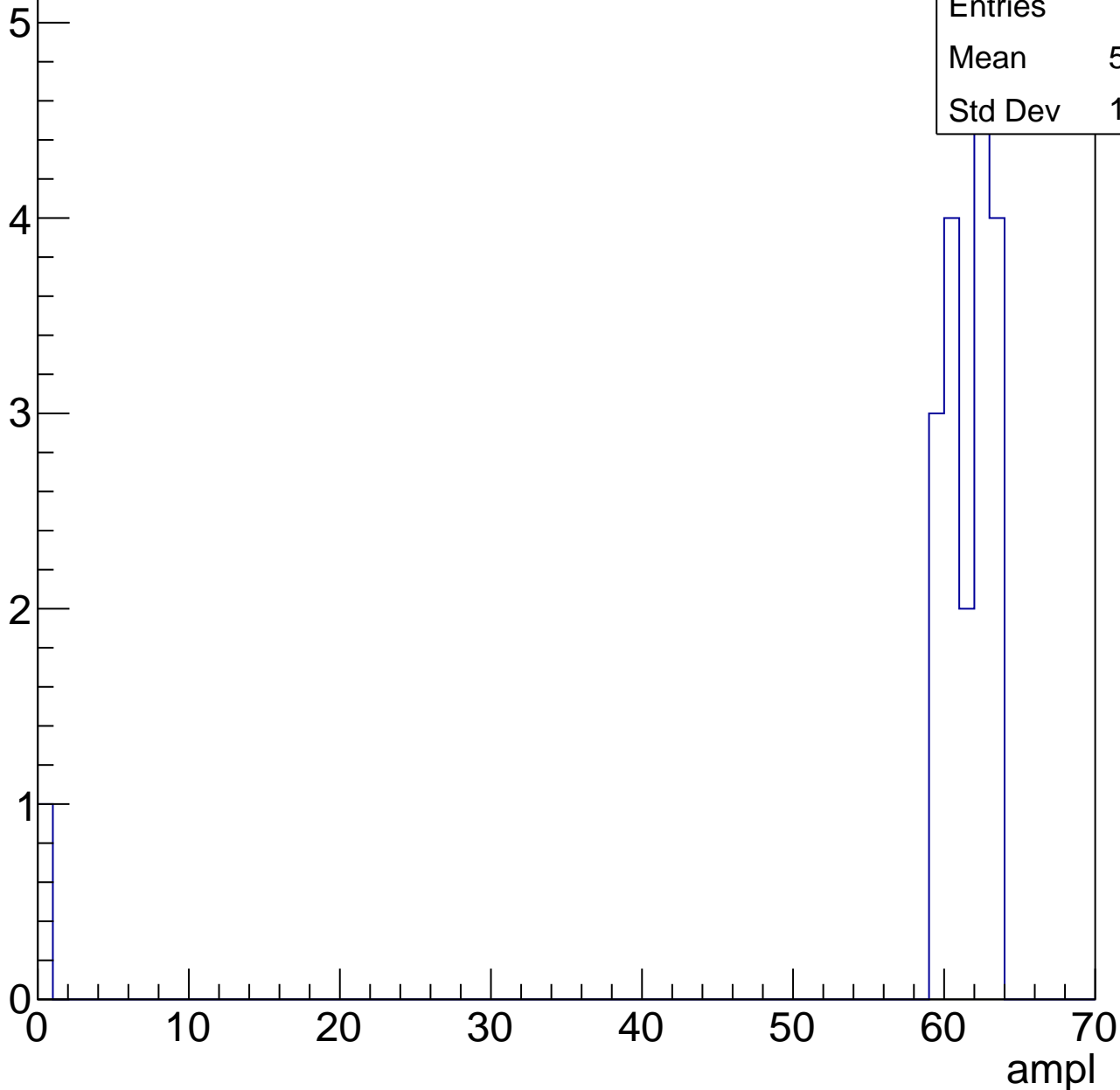


# B1L103S, U11-ch31, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	19
Mean	57.95
Std Dev	13.73



# B1L103S, U11-ch31, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	63
Std Dev	0



# B1L103S, U11-ch31, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U11-ch32, adc0

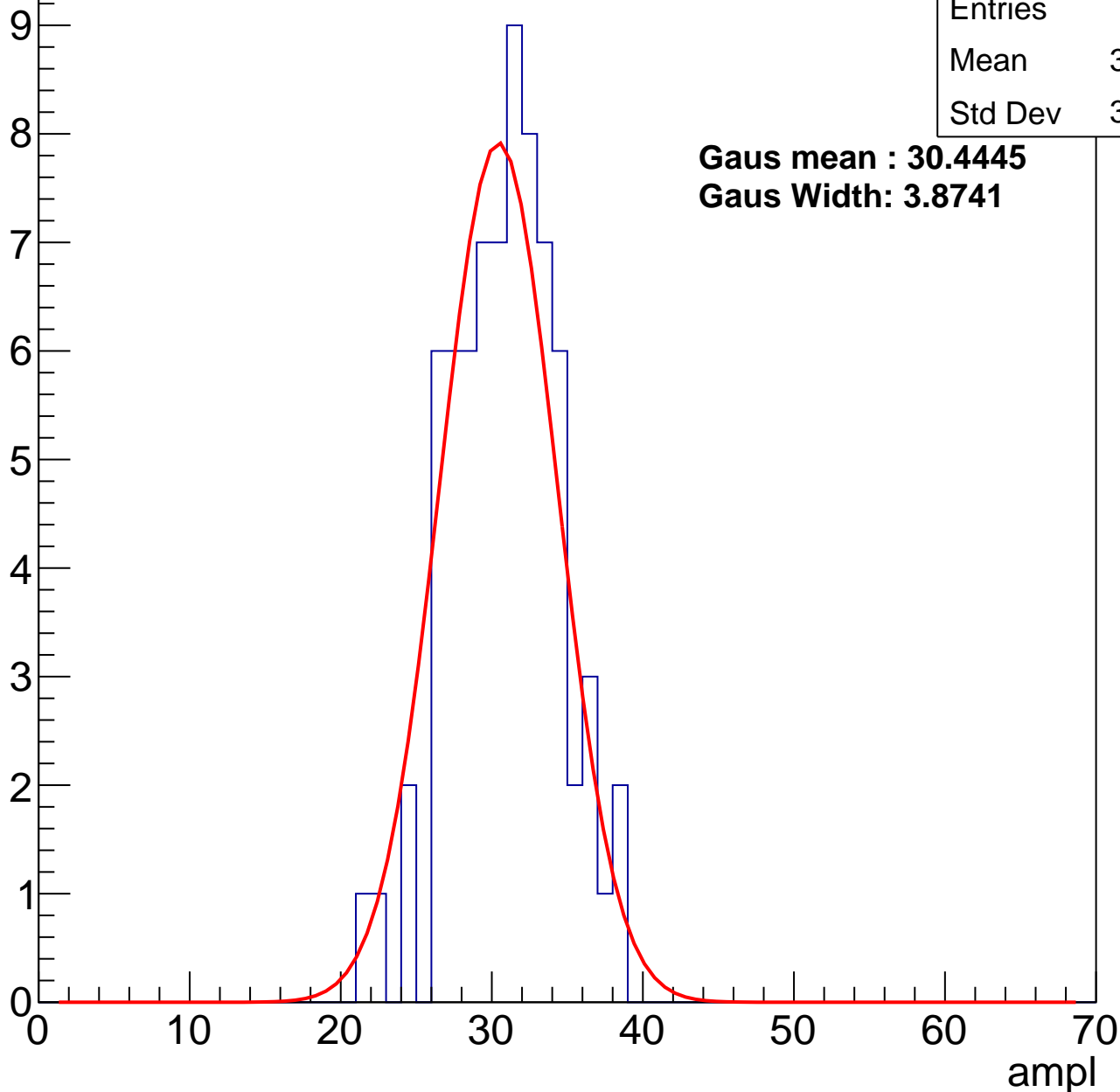
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	74
Mean	30.42
Std Dev	3.526

**Gaus mean : 30.4445**

**Gaus Width: 3.8741**



# B1L103S, U11-ch32, adc1

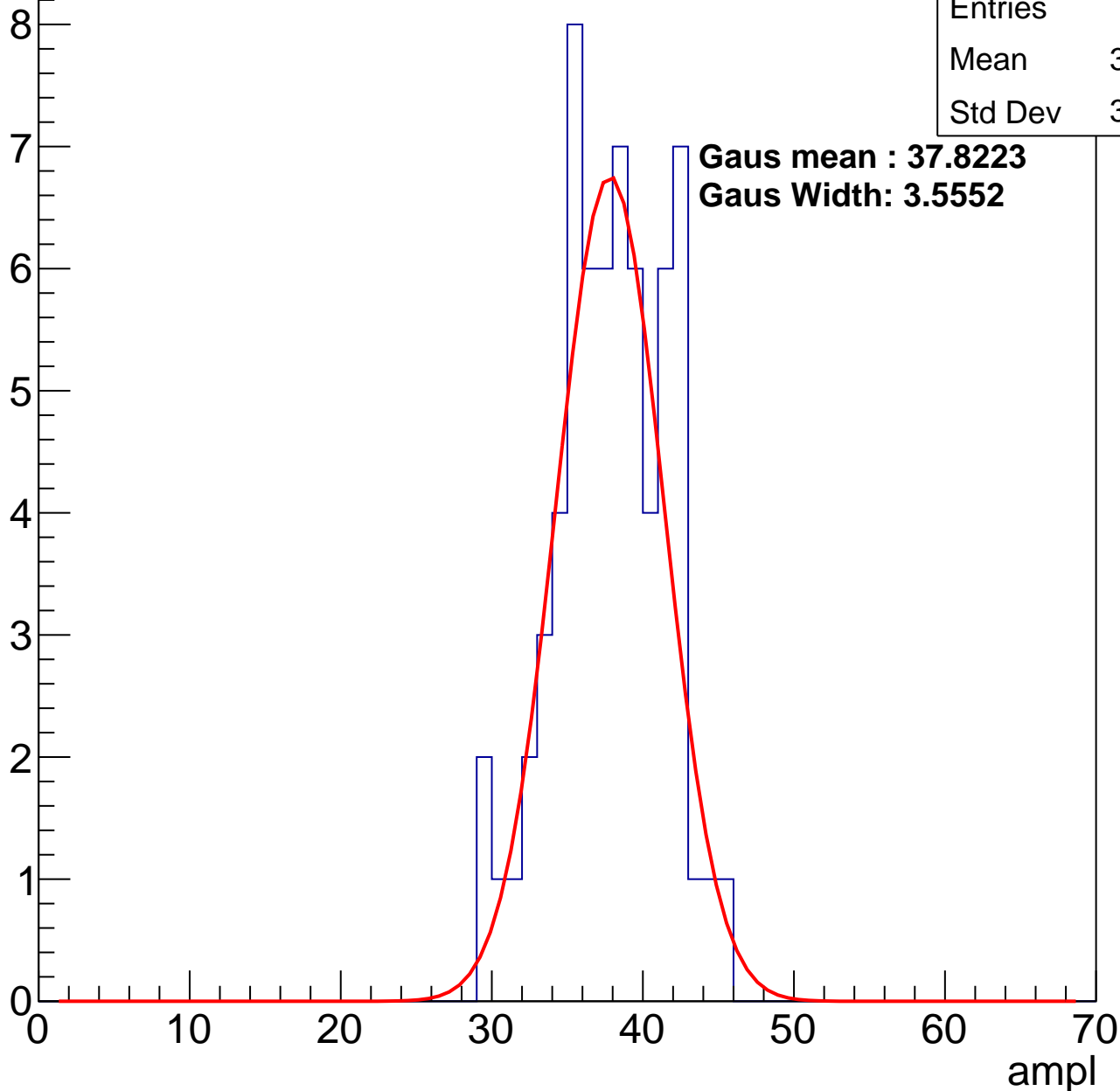
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	37.39
Std Dev	3.613

**Gaus mean : 37.8223**

**Gaus Width: 3.5552**



# B1L103S, U11-ch32, adc2

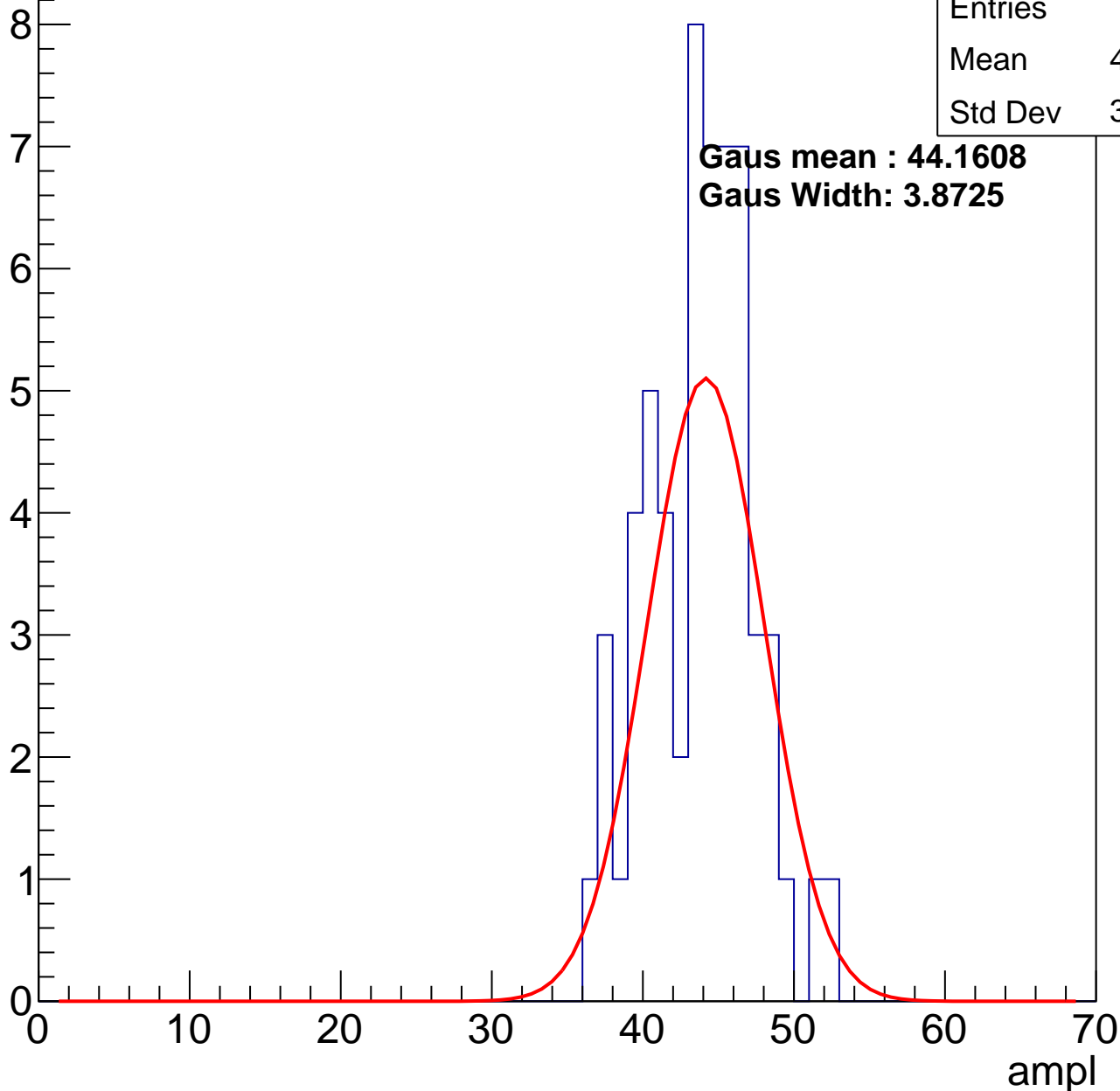
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	58
Mean	43.36
Std Dev	3.482

**Gaus mean : 44.1608**

**Gaus Width: 3.8725**

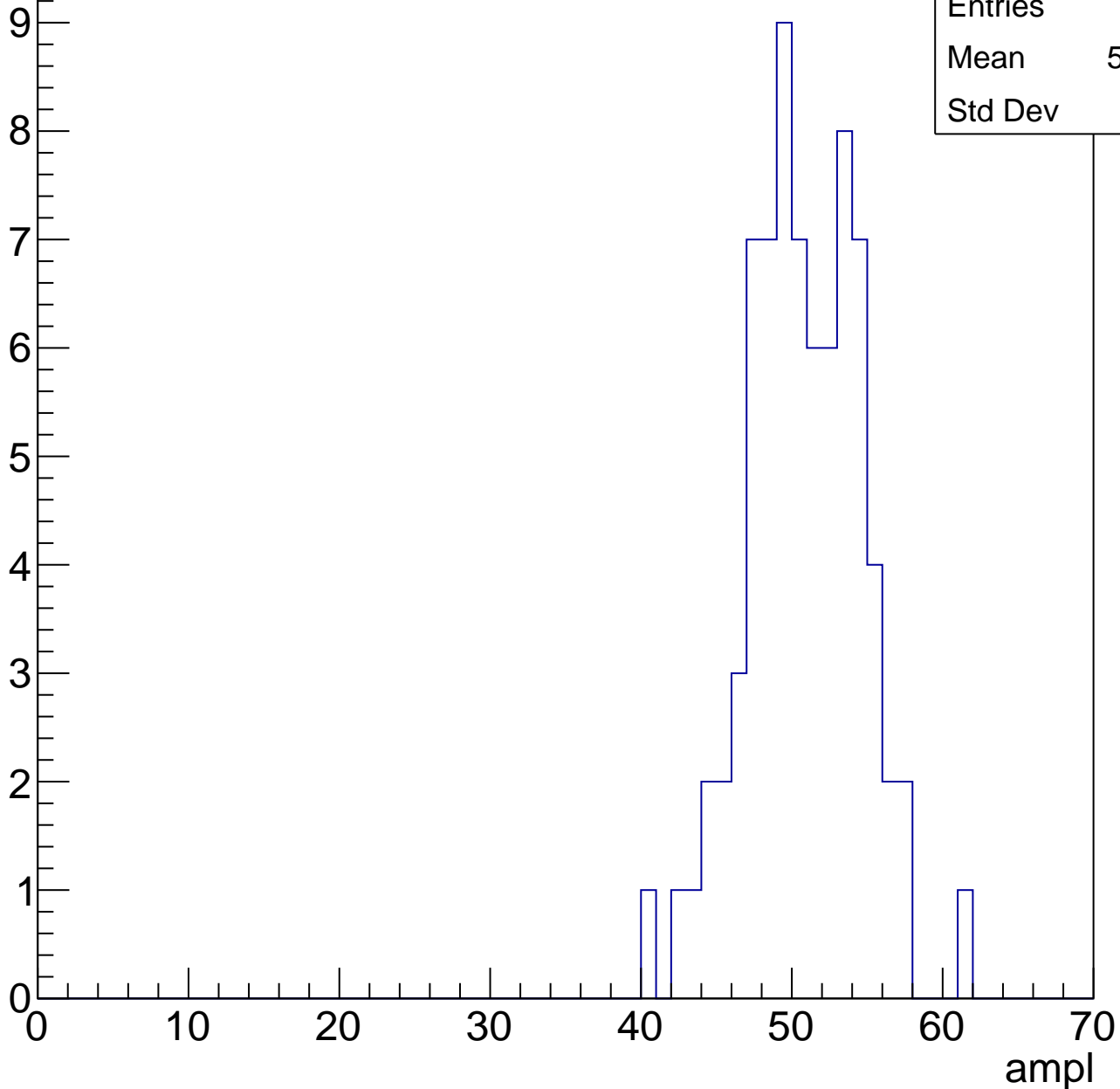


# B1L103S, U11-ch32, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	76
Mean	50.32
Std Dev	3.77

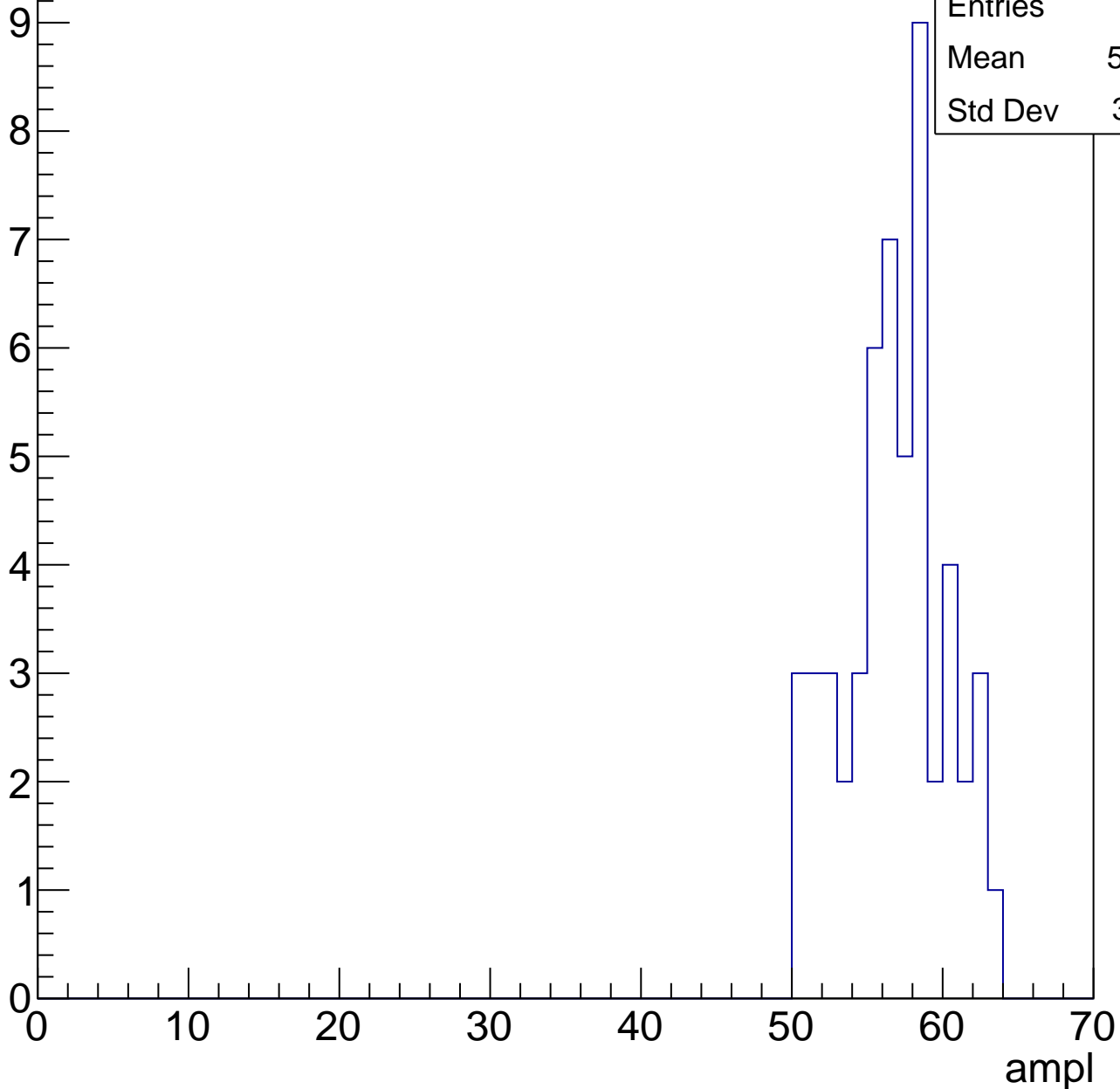


# B1L103S, U11-ch32, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	53
Mean	56.32
Std Dev	3.341

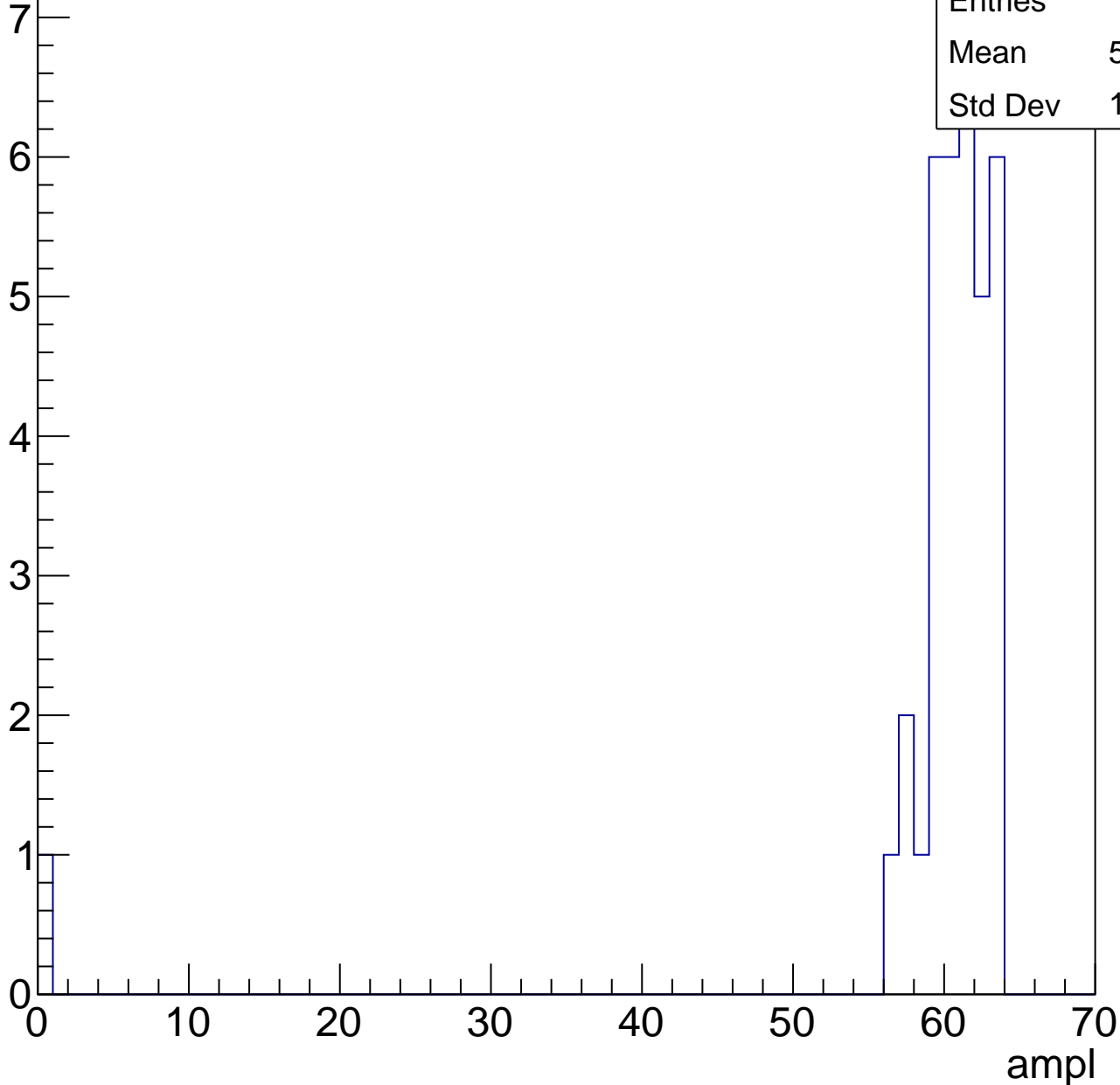


# B1L103S, U11-ch32, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

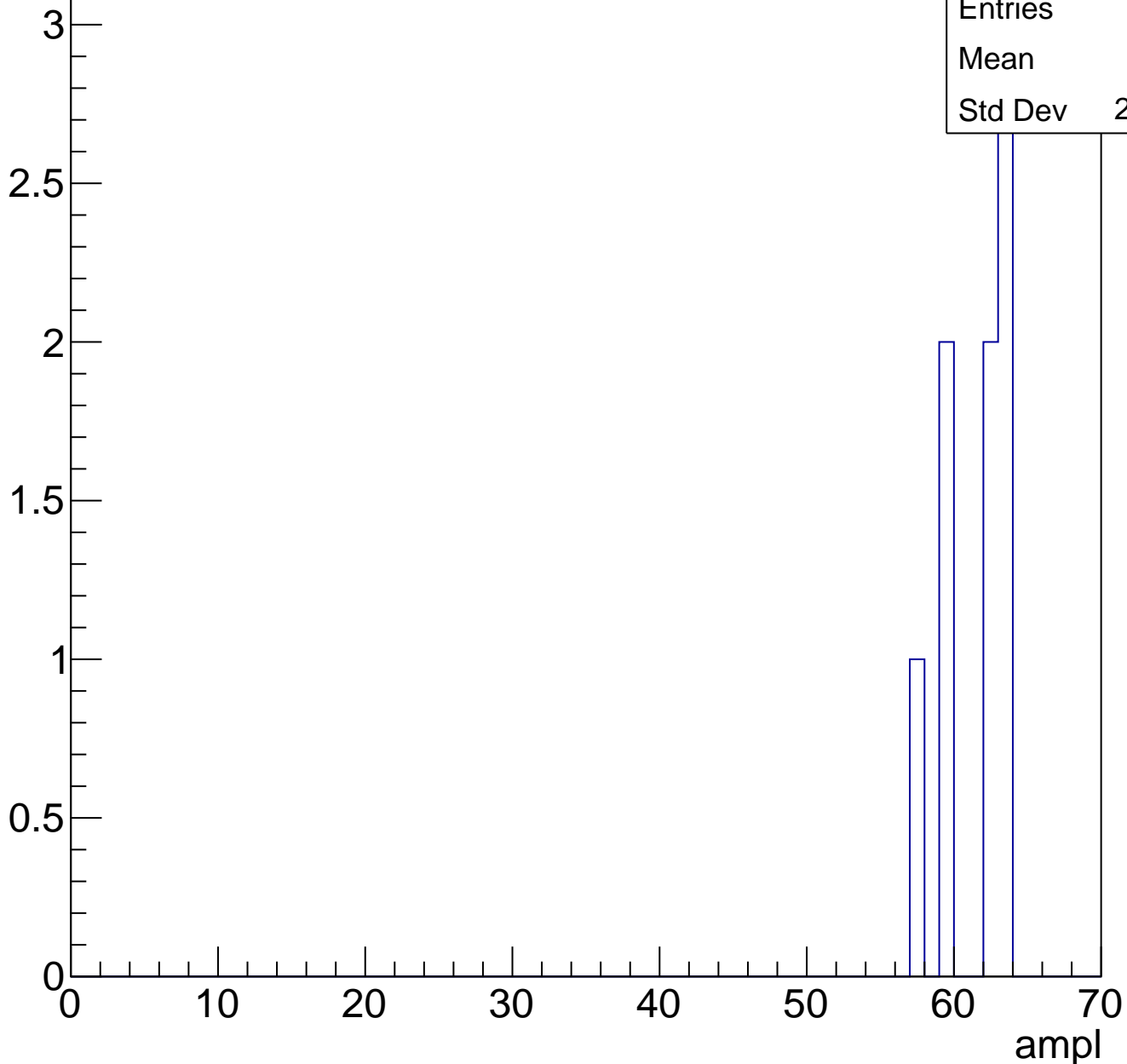
Entries	35
Mean	58.77
Std Dev	10.24



# B1L103S, U11-ch32, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U11-ch32, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L103S, U11-ch33, adc0

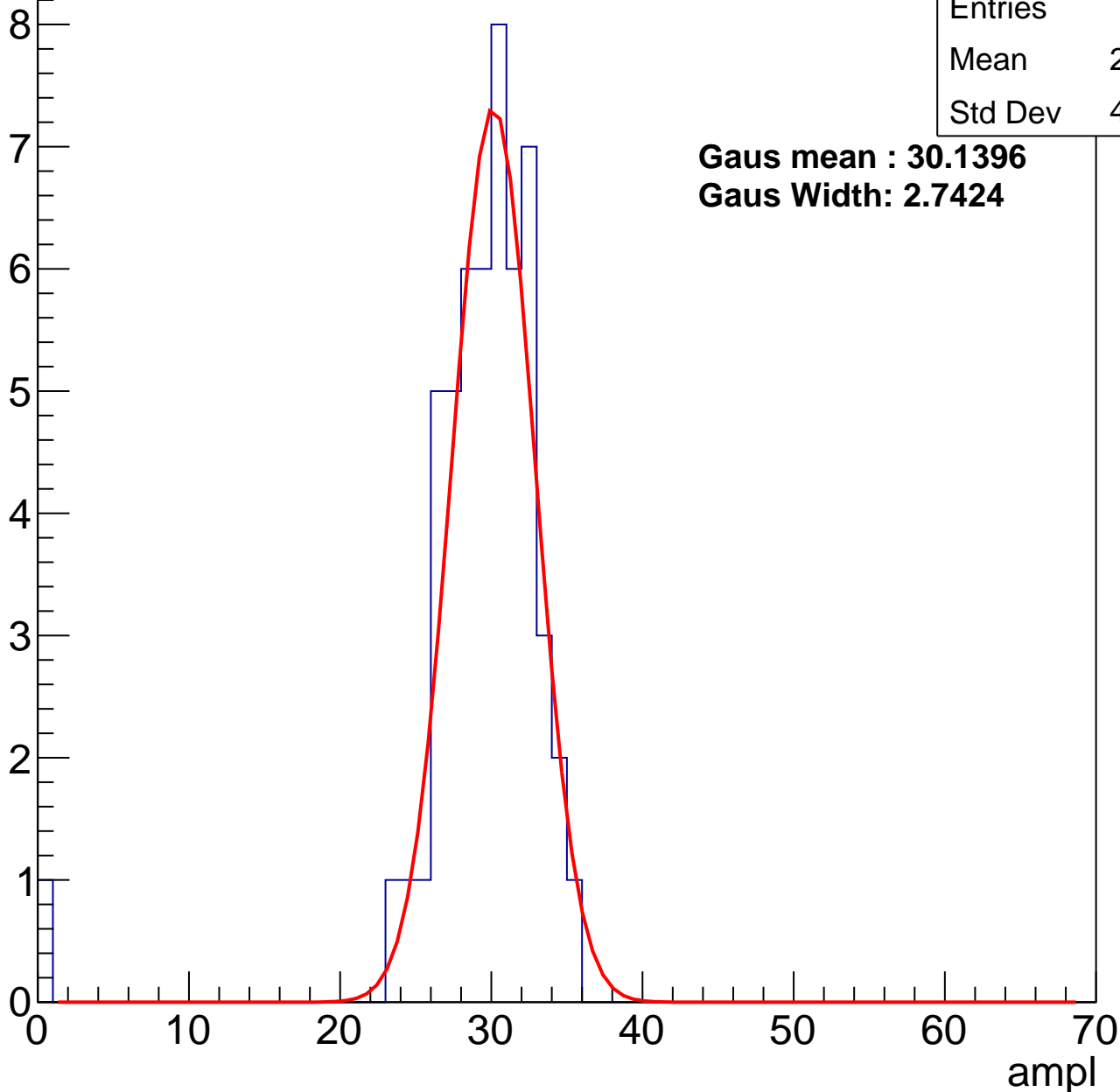
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	53
Mean	28.89
Std Dev	4.793

**Gaus mean : 30.1396**

**Gaus Width: 2.7424**



# B1L103S, U11-ch33, adc1

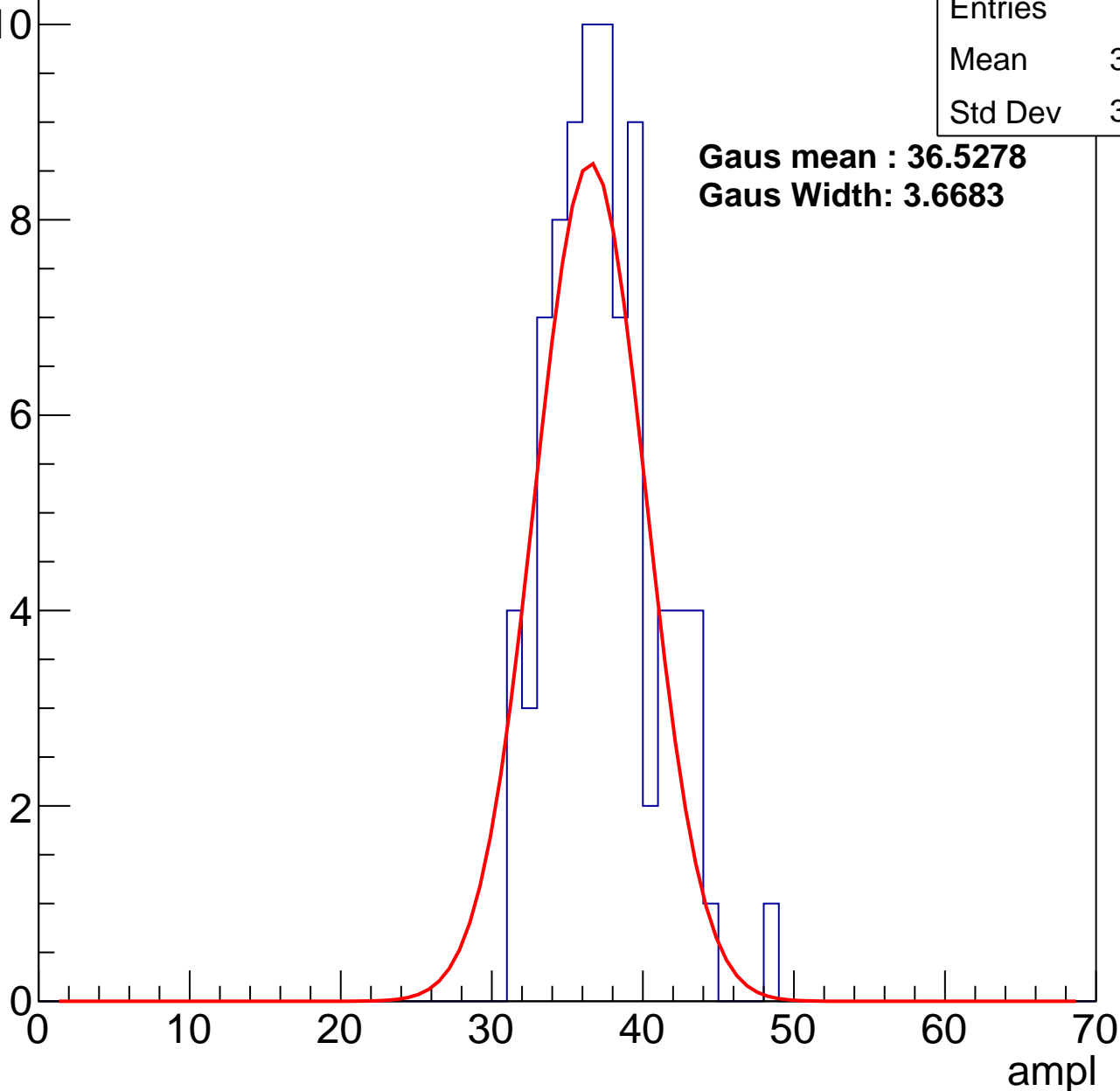
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	83
Mean	36.88
Std Dev	3.448

**Gaus mean : 36.5278**

**Gaus Width: 3.6683**



# B1L103S, U11-ch33, adc2

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	69
Mean	44.09
Std Dev	3.087

**Gaus mean : 44.7618**

**Gaus Width: 3.1555**

10

8

6

4

2

0

ampl

0

10

20

30

40

50

60

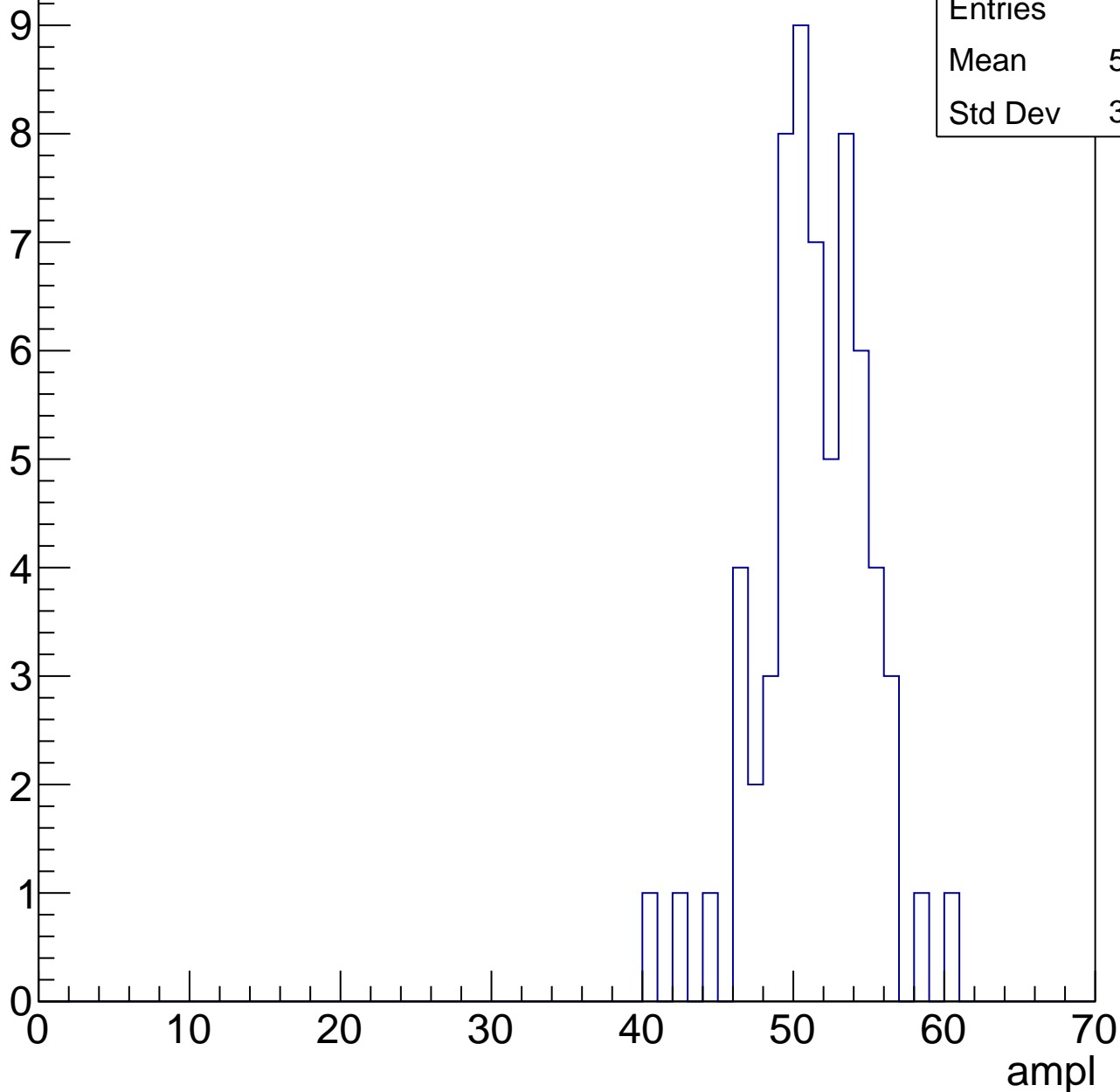
70

# B1L103S, U11-ch33, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	50.95
Std Dev	3.559

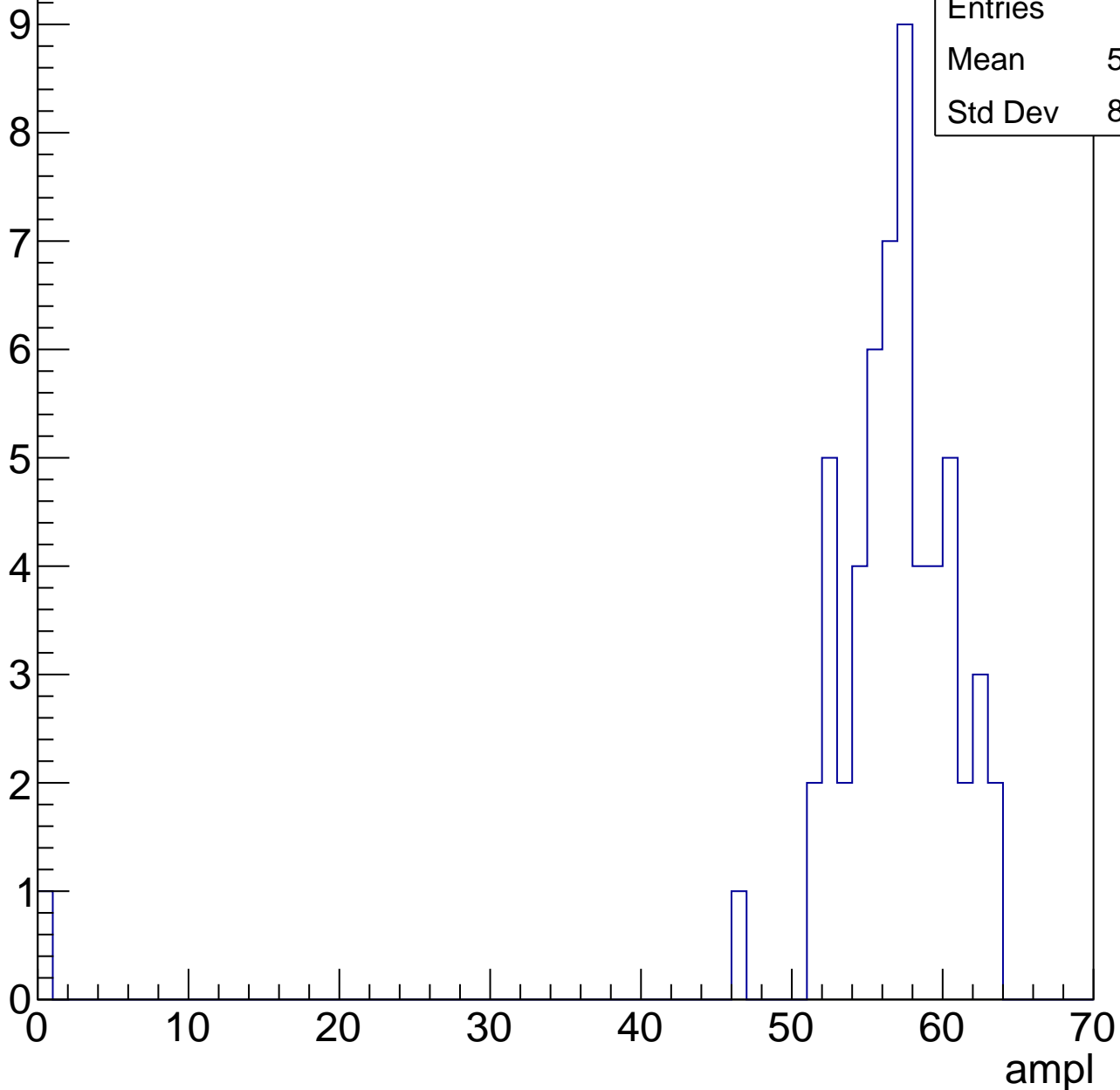


# B1L103S, U11-ch33, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	57
Mean	55.56
Std Dev	8.156

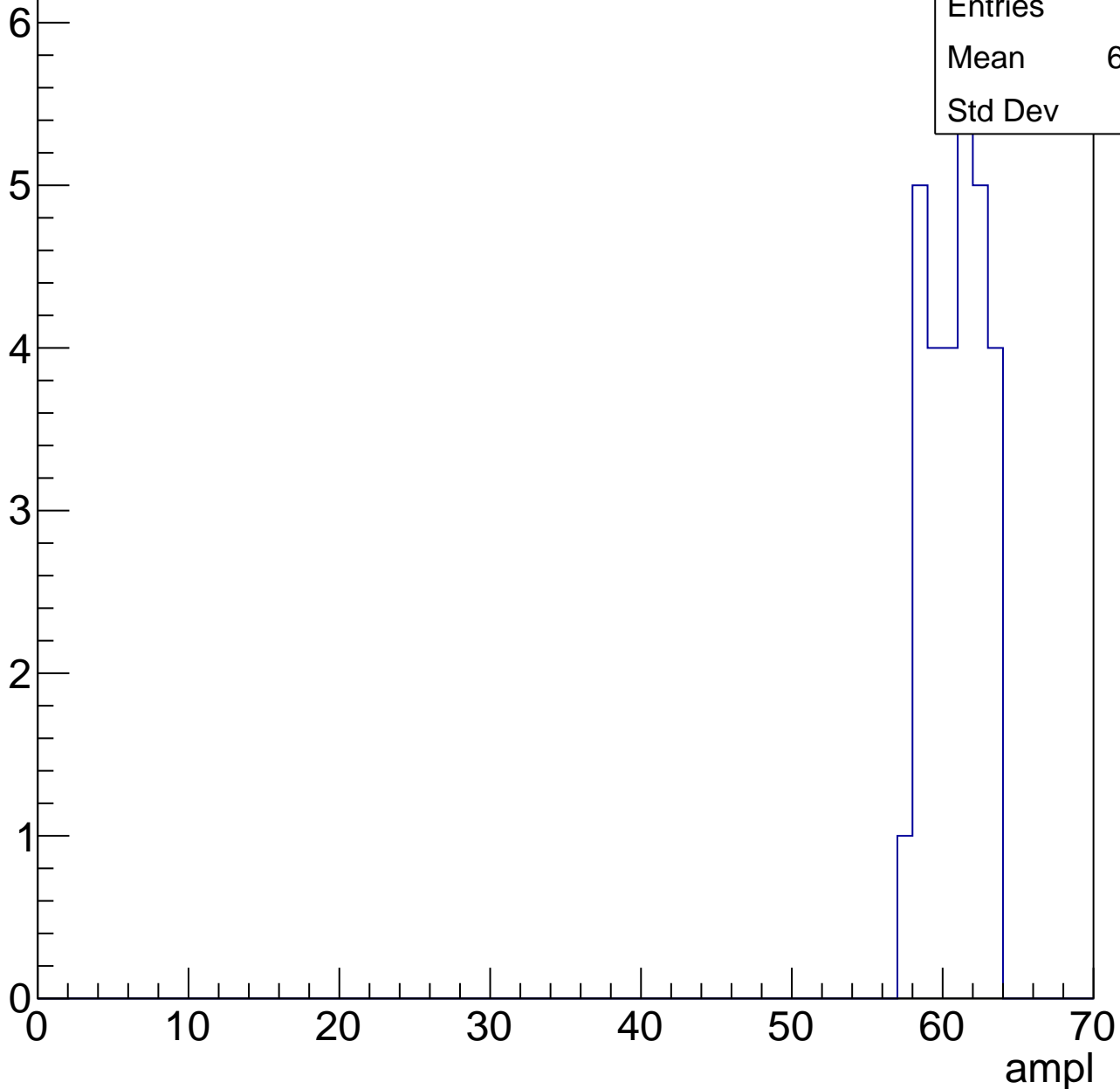


# B1L103S, U11-ch33, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

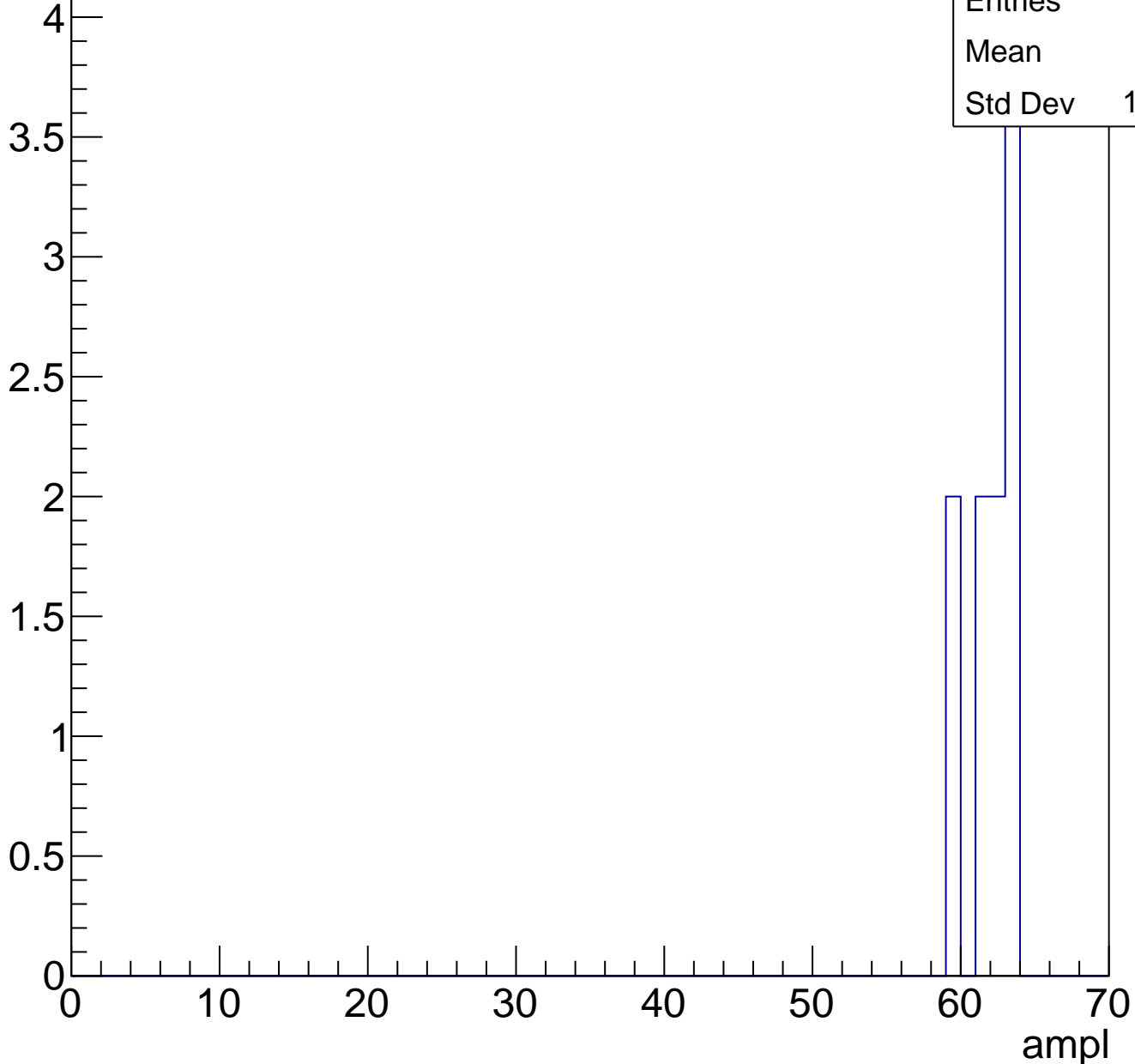
Entries	29
Mean	60.38
Std Dev	1.77



# B1L103S, U11-ch33, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	10
Mean	61.6
Std Dev	1.497



# B1L103S, U11-ch33, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L103S, U11-ch34, adc0

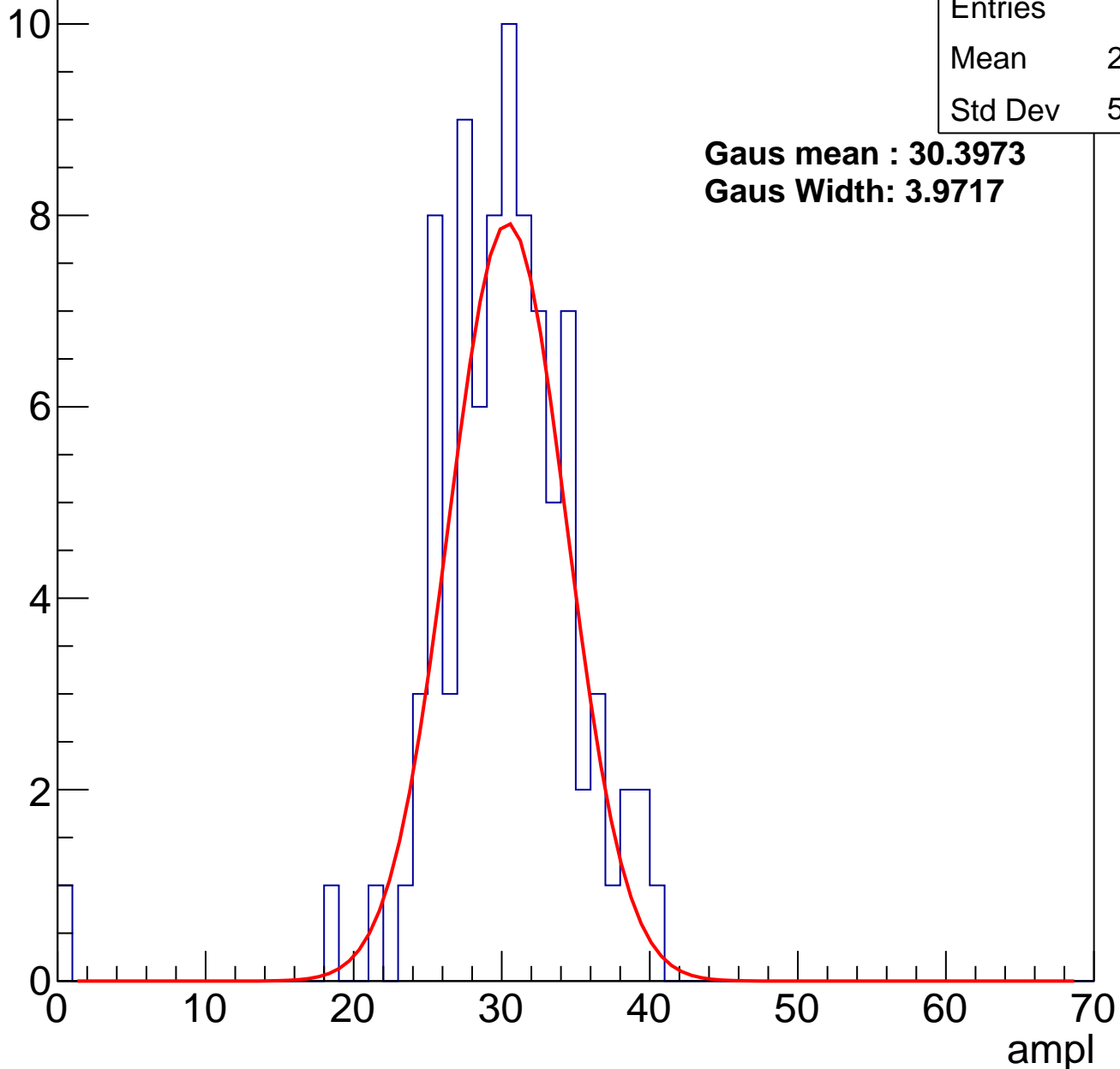
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	89
Mean	29.65
Std Dev	5.217

**Gaus mean : 30.3973**

**Gaus Width: 3.9717**

Entry



# B1L103S, U11-ch34, adc1

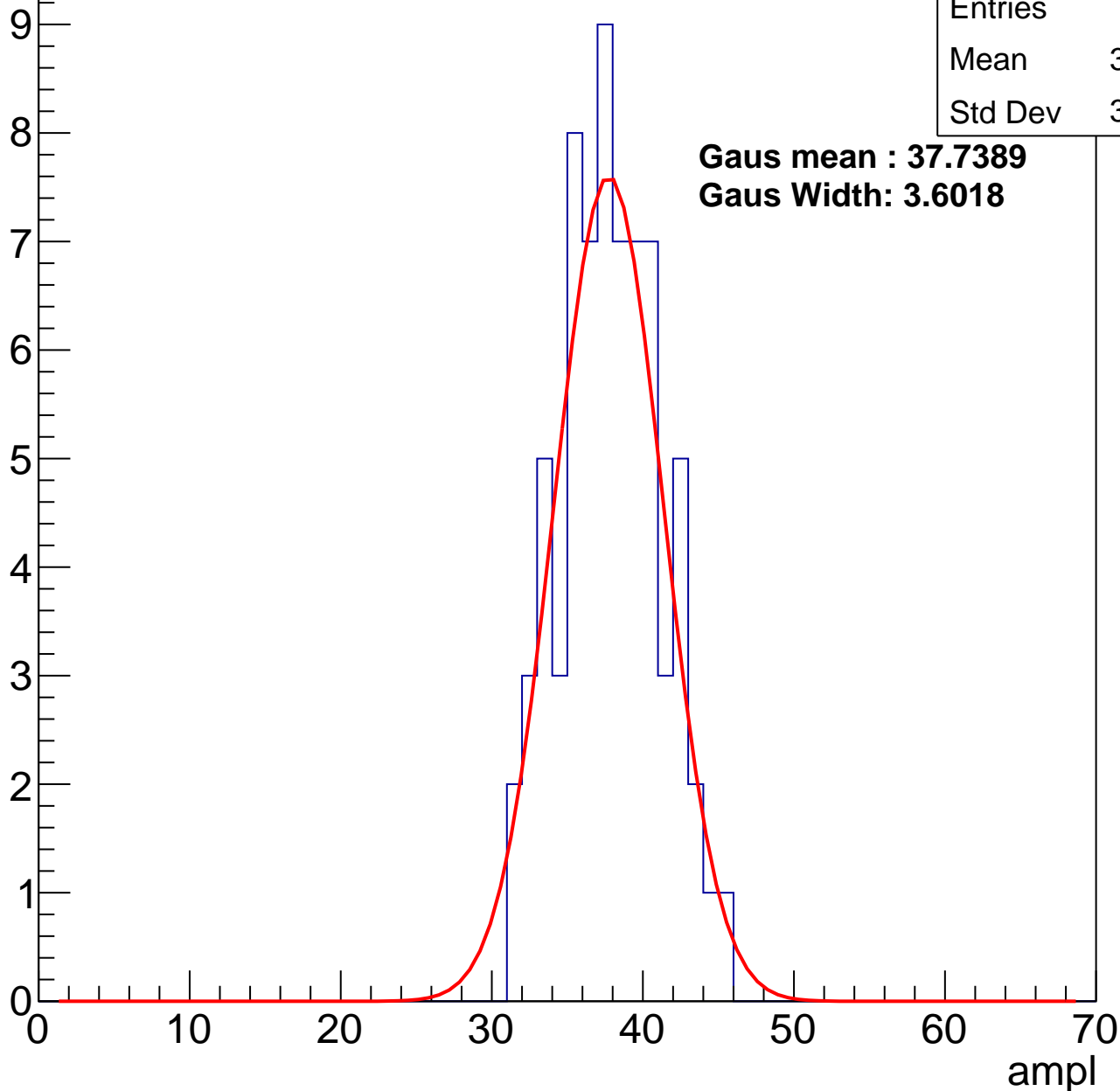
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	70
Mean	37.39
Std Dev	3.248

**Gaus mean : 37.7389**

**Gaus Width: 3.6018**



# B1L103S, U11-ch34, adc2

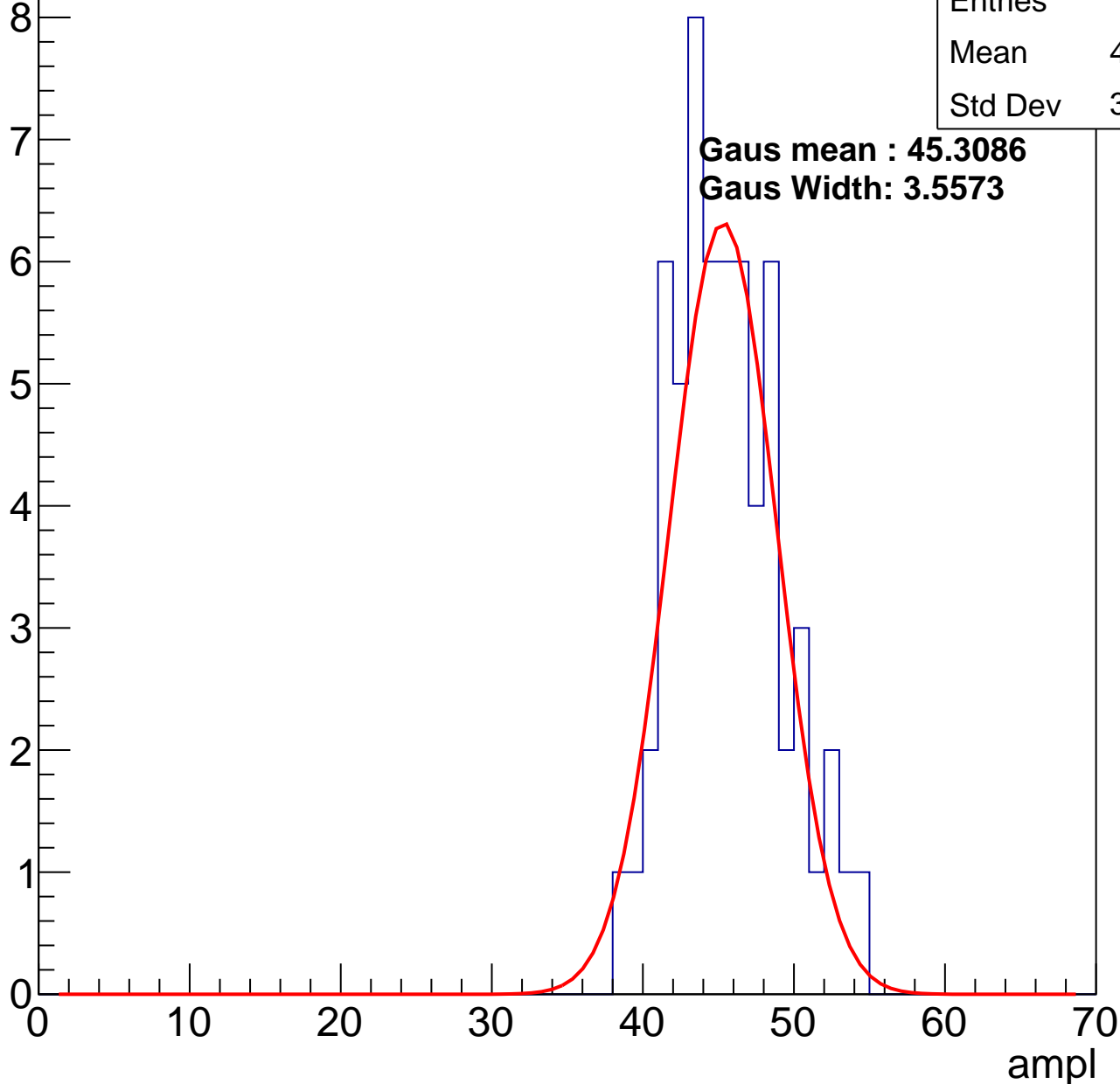
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	61
Mean	45.13
Std Dev	3.564

**Gaus mean : 45.3086**

**Gaus Width: 3.5573**

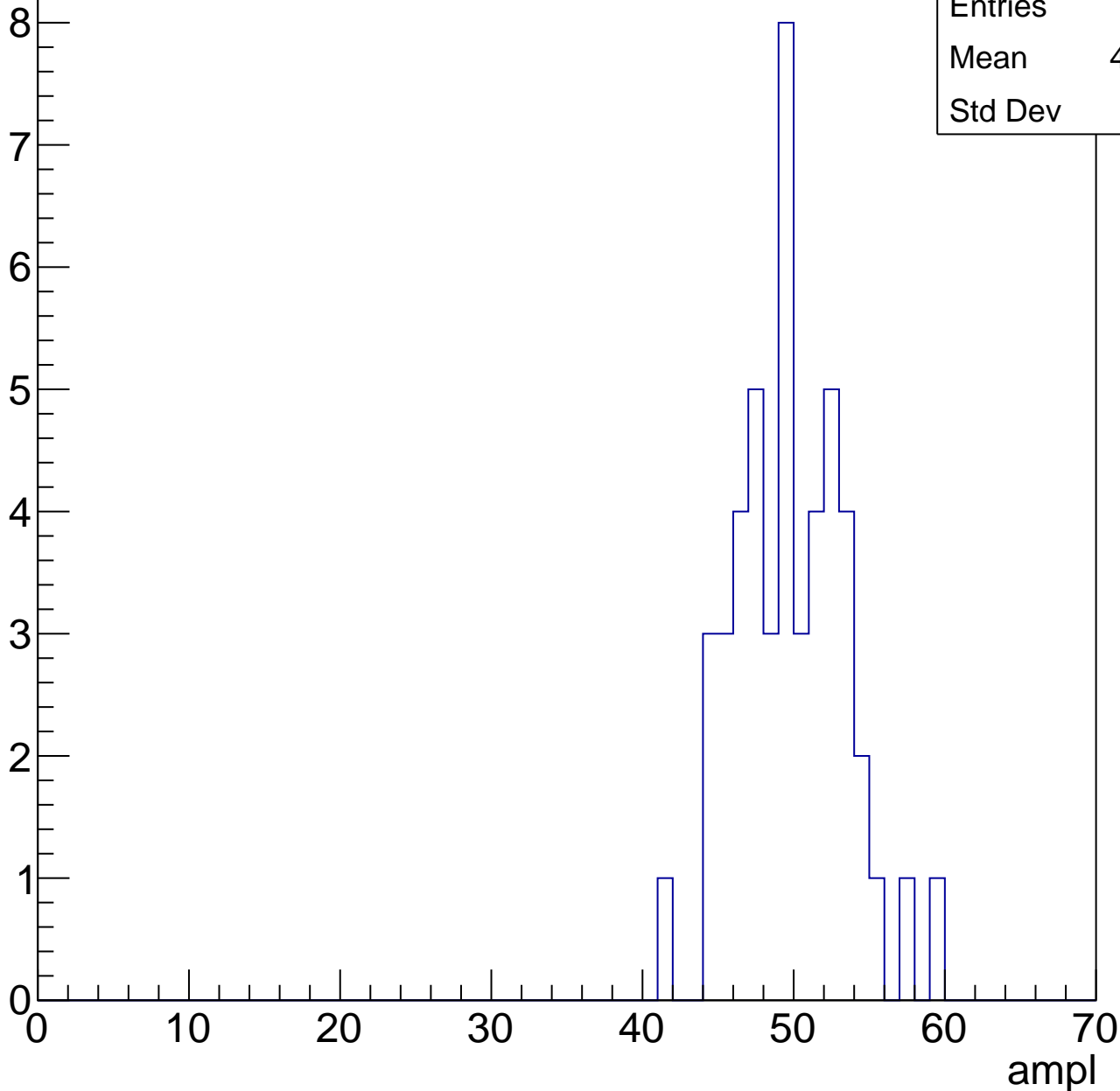


# B1L103S, U11-ch34, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	48
Mean	49.33
Std Dev	3.59

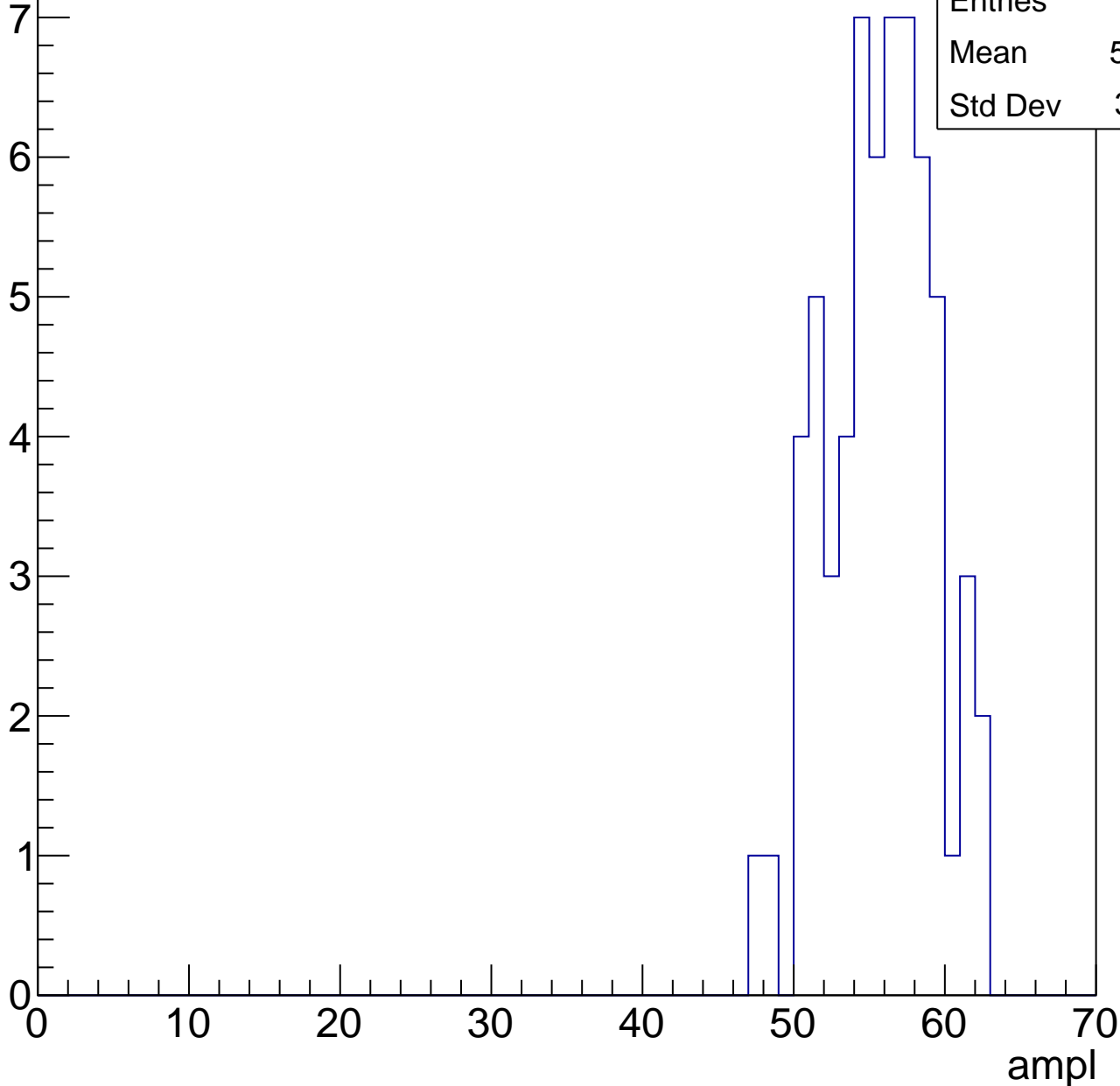


# B1L103S, U11-ch34, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	55.27
Std Dev	3.451

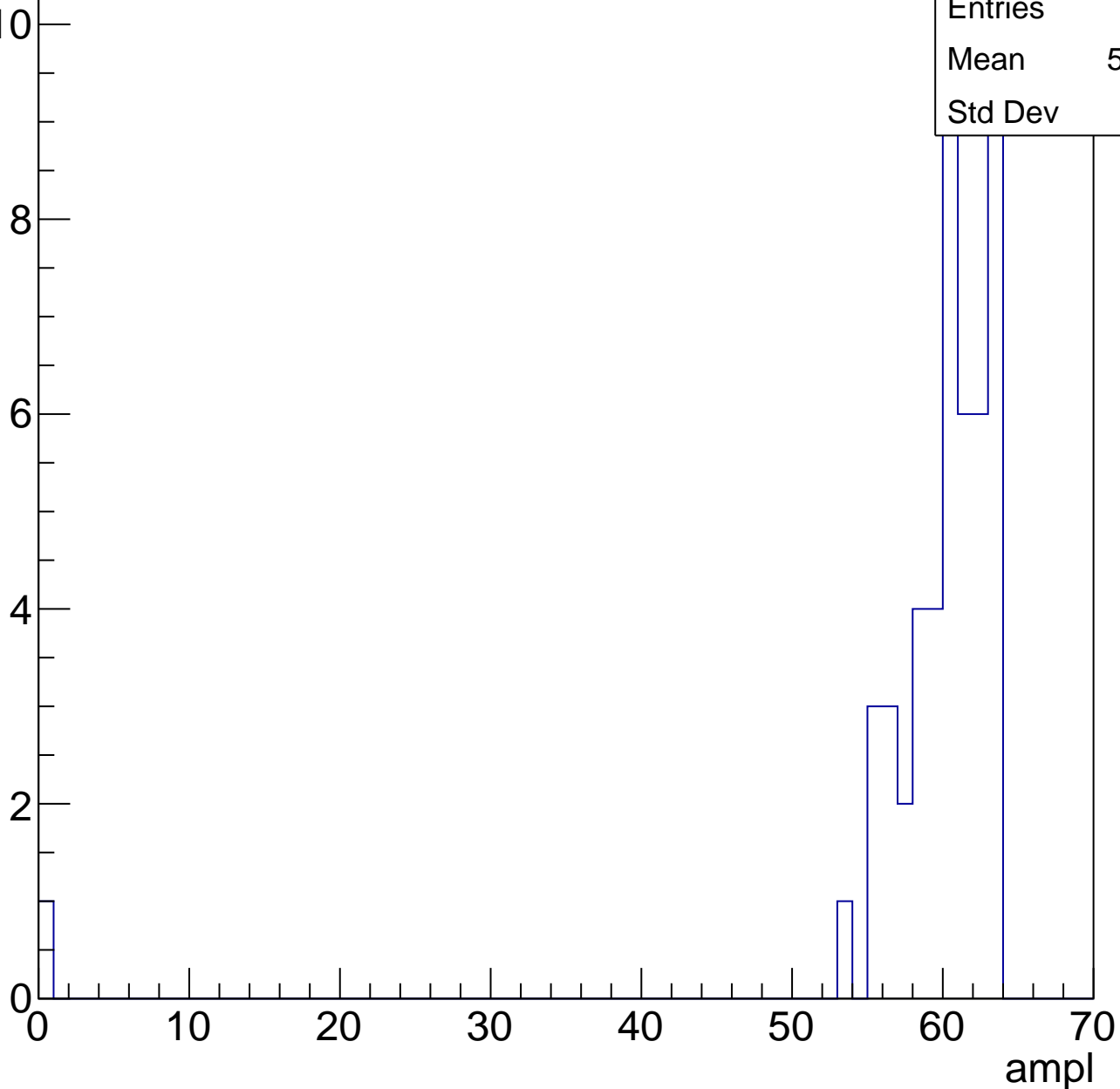


# B1L103S, U11-ch34, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	49
Mean	58.69
Std Dev	8.86



# B1L103S, U11-ch34, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	3
Mean	61.67
Std Dev	0.4714

ampl

0 10 20 30 40 50 60 70



# B1L103S, U11-ch34, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U11-ch35, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	70
Mean	30.67
Std Dev	3.294

**Gaus mean : 31.3304**

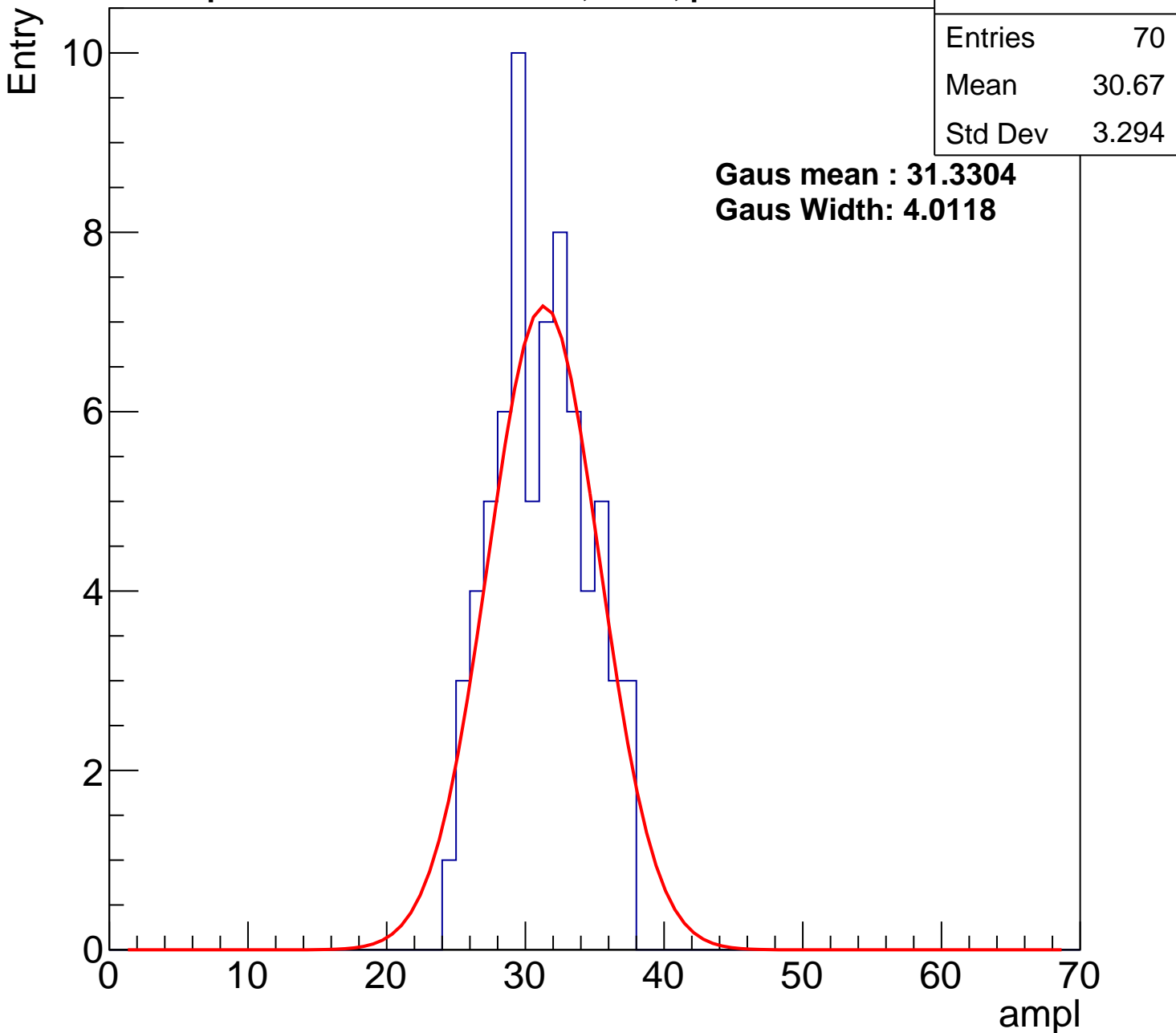
**Gaus Width: 4.0118**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U11-ch35, adc1

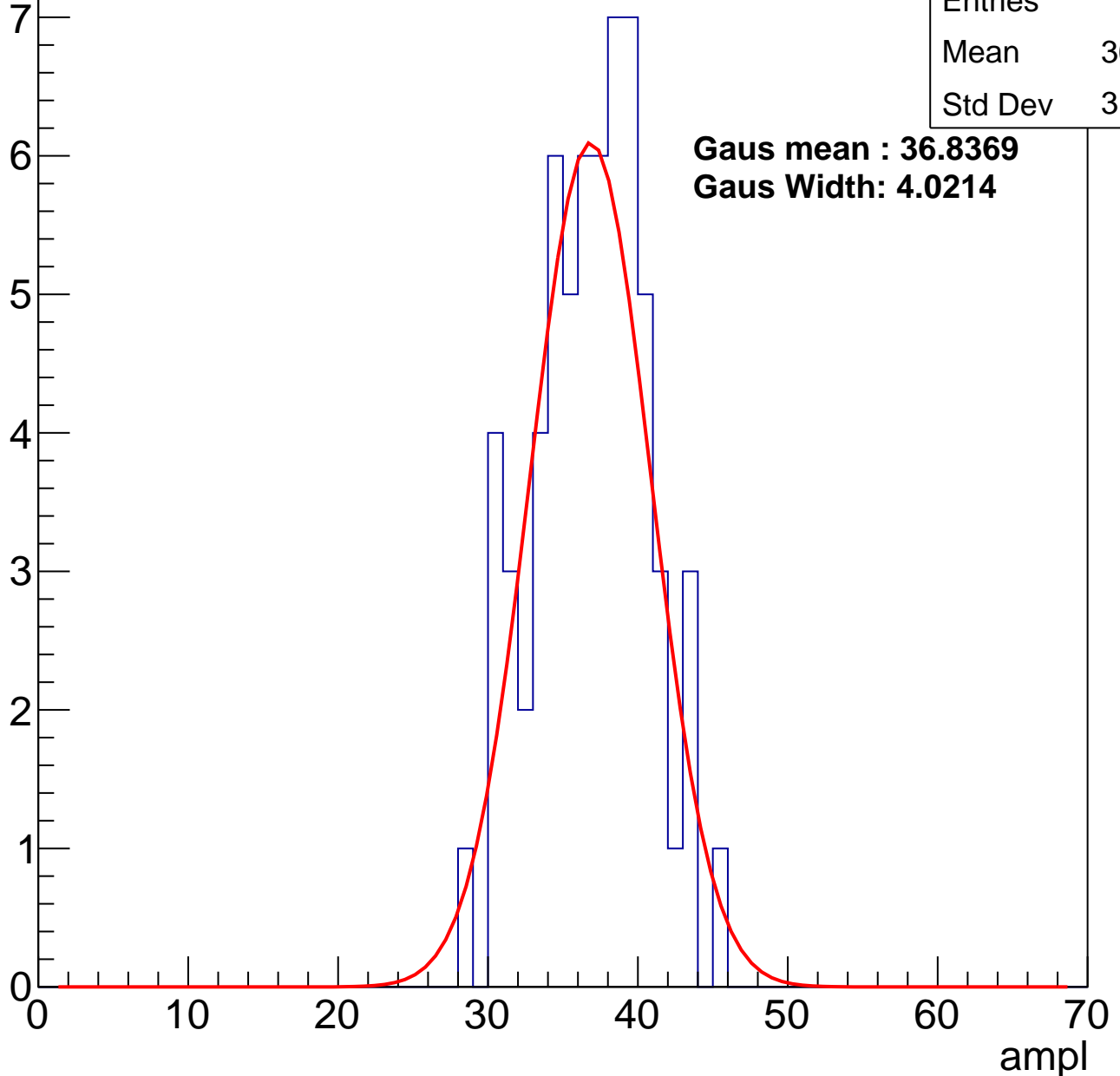
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	36.44
Std Dev	3.716

**Gaus mean : 36.8369**

**Gaus Width: 4.0214**



# B1L103S, U11-ch35, adc2

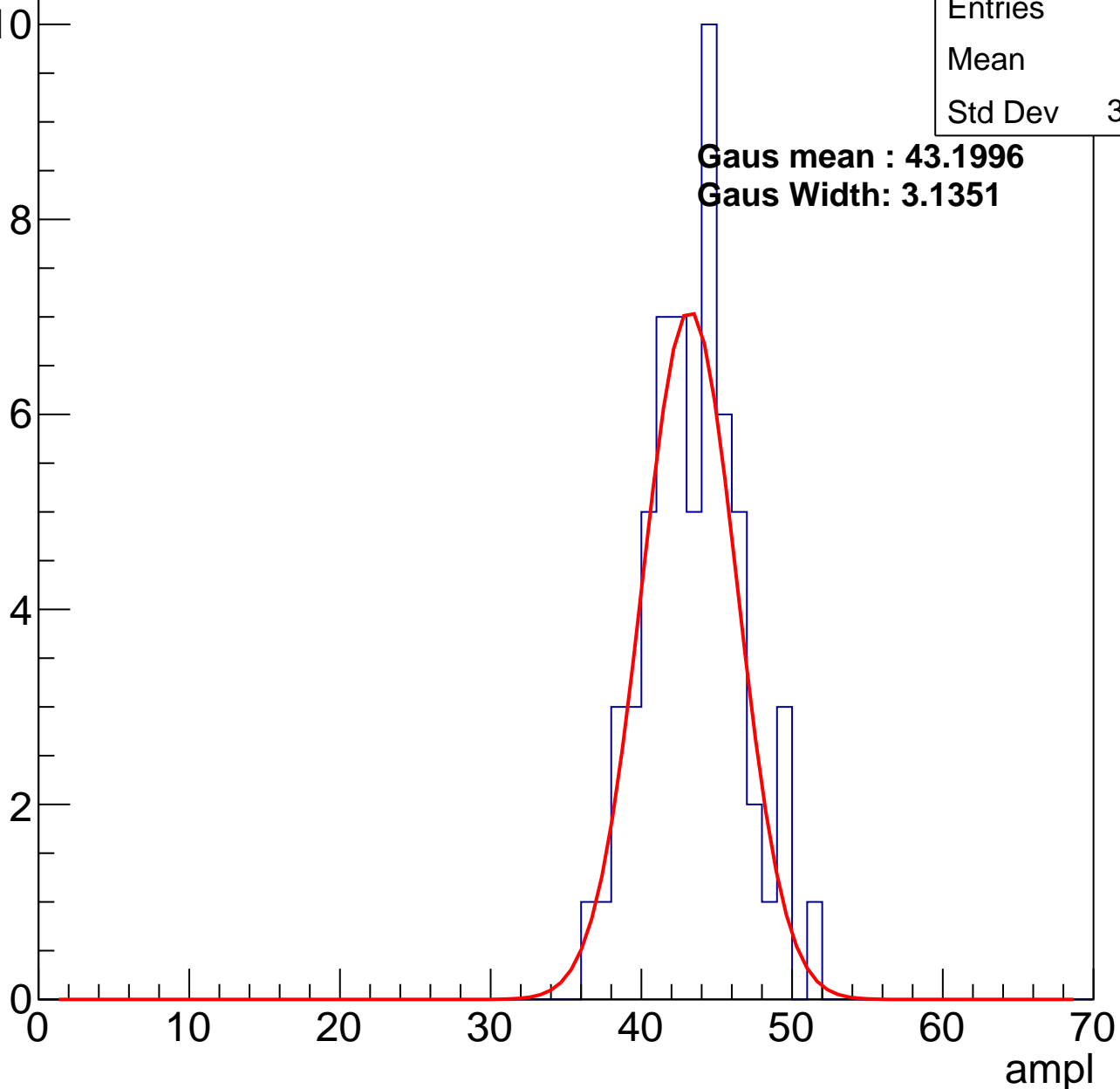
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	60
Mean	43
Std Dev	3.152

**Gaus mean : 43.1996**

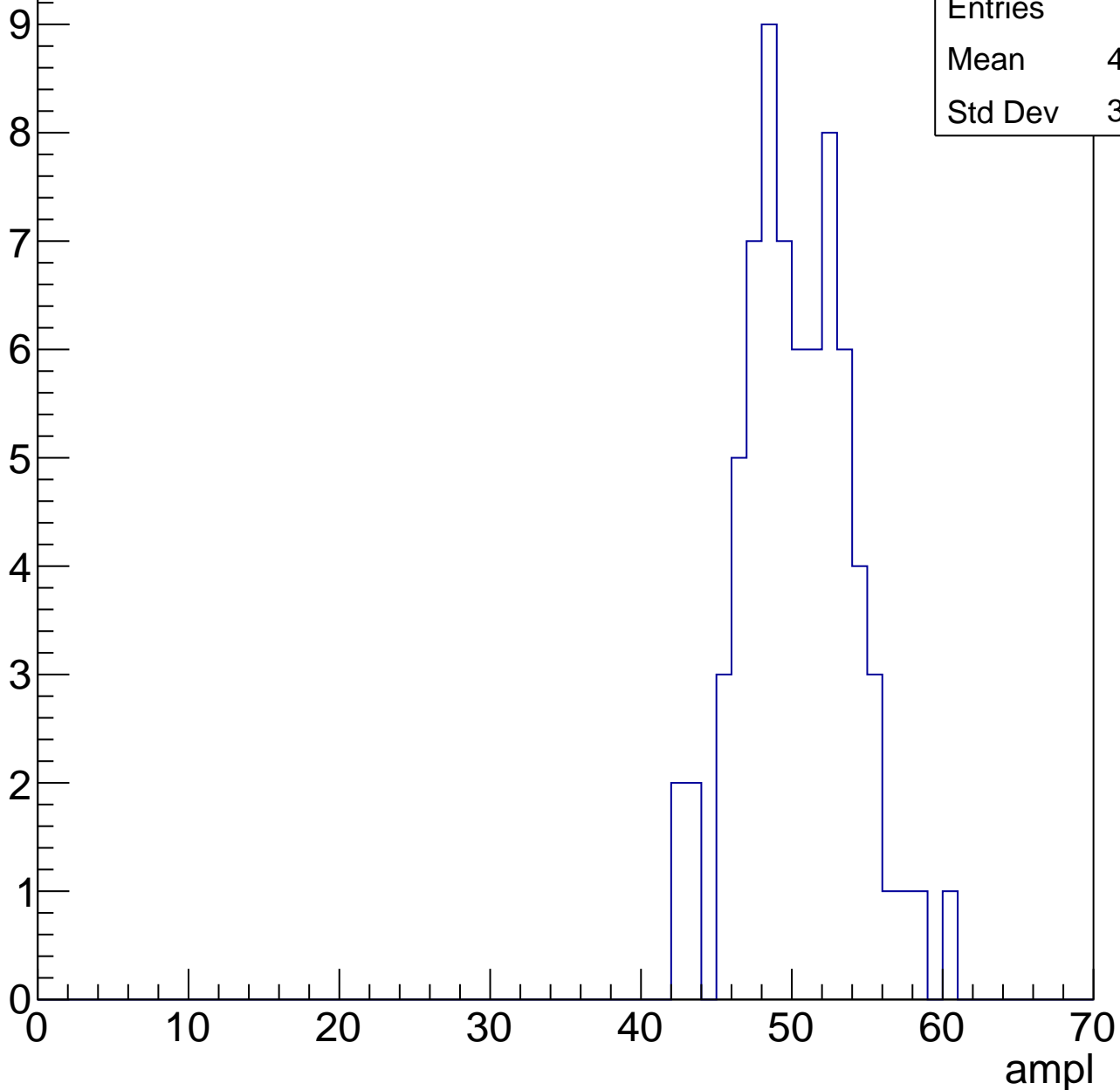
**Gaus Width: 3.1351**



# B1L103S, U11-ch35, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



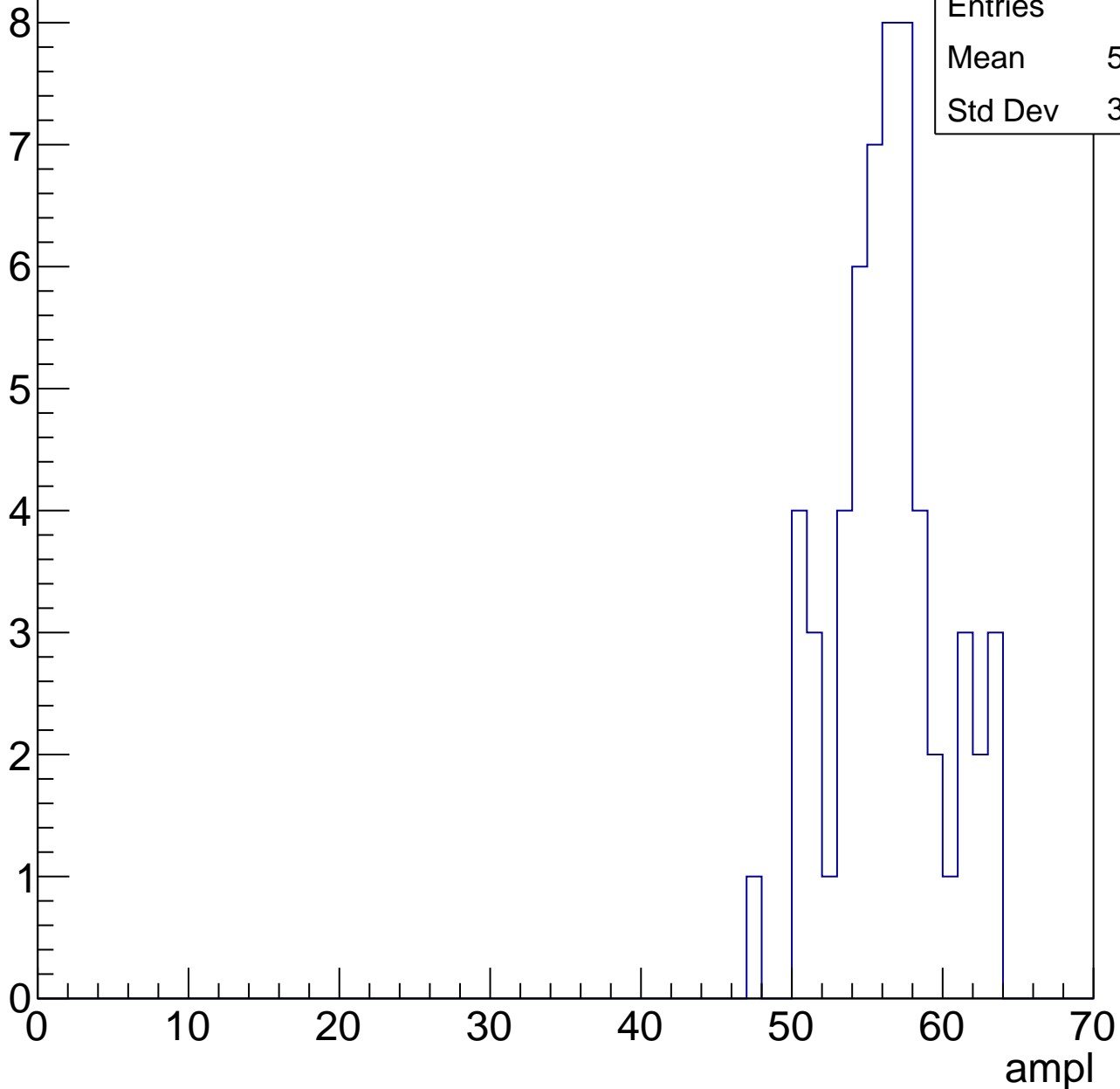
Entries	72
Mean	49.88
Std Dev	3.663

# B1L103S, U11-ch35, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

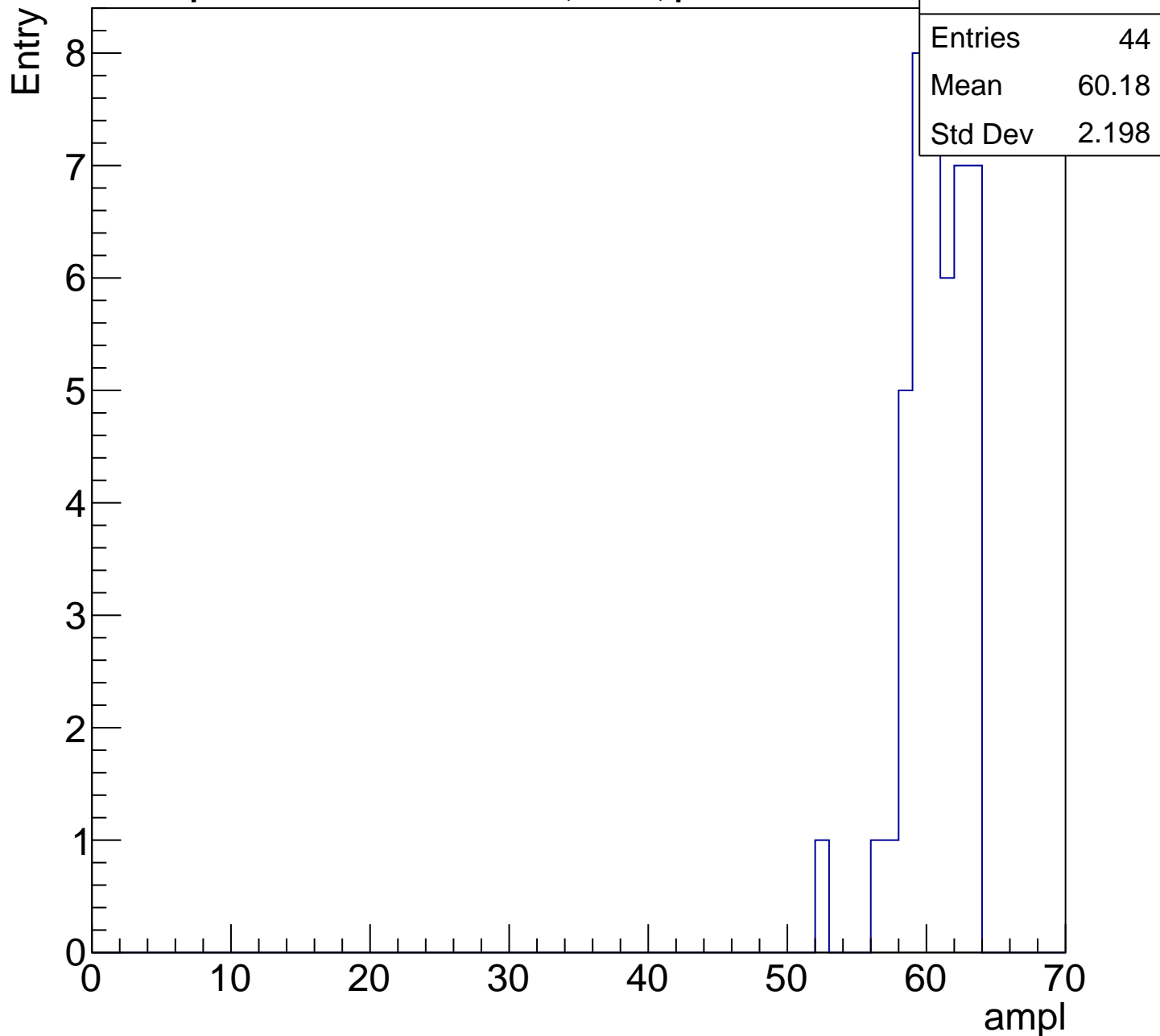
Entry

Entries	57
Mean	55.84
Std Dev	3.587



# B1L103S, U11-ch35, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U11-ch35, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U11-ch35, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	23
Std Dev	0

# B1L103S, U11-ch36, adc0

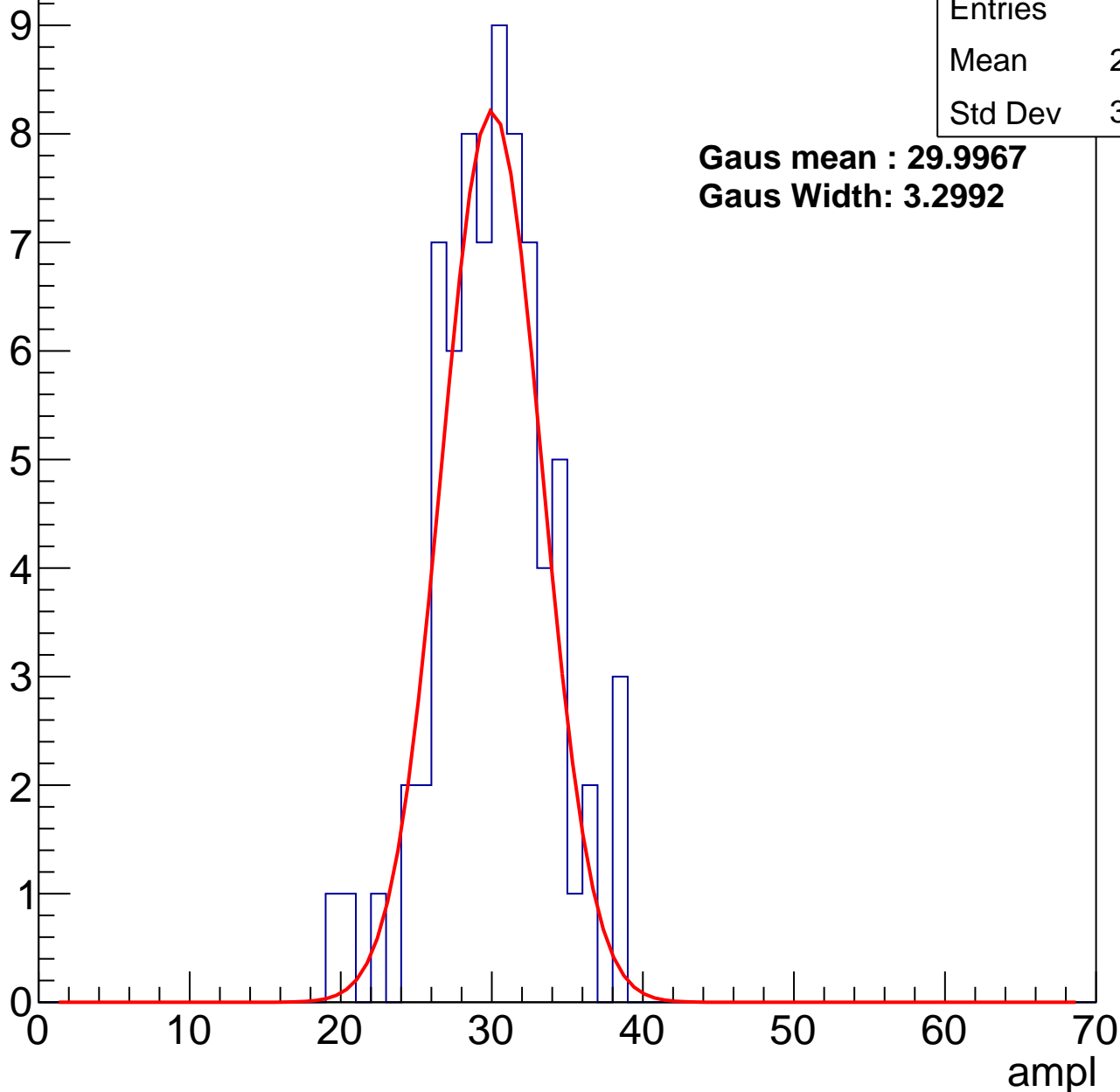
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	74
Mean	29.66
Std Dev	3.757

**Gaus mean : 29.9967**

**Gaus Width: 3.2992**



# B1L103S, U11-ch36, adc1

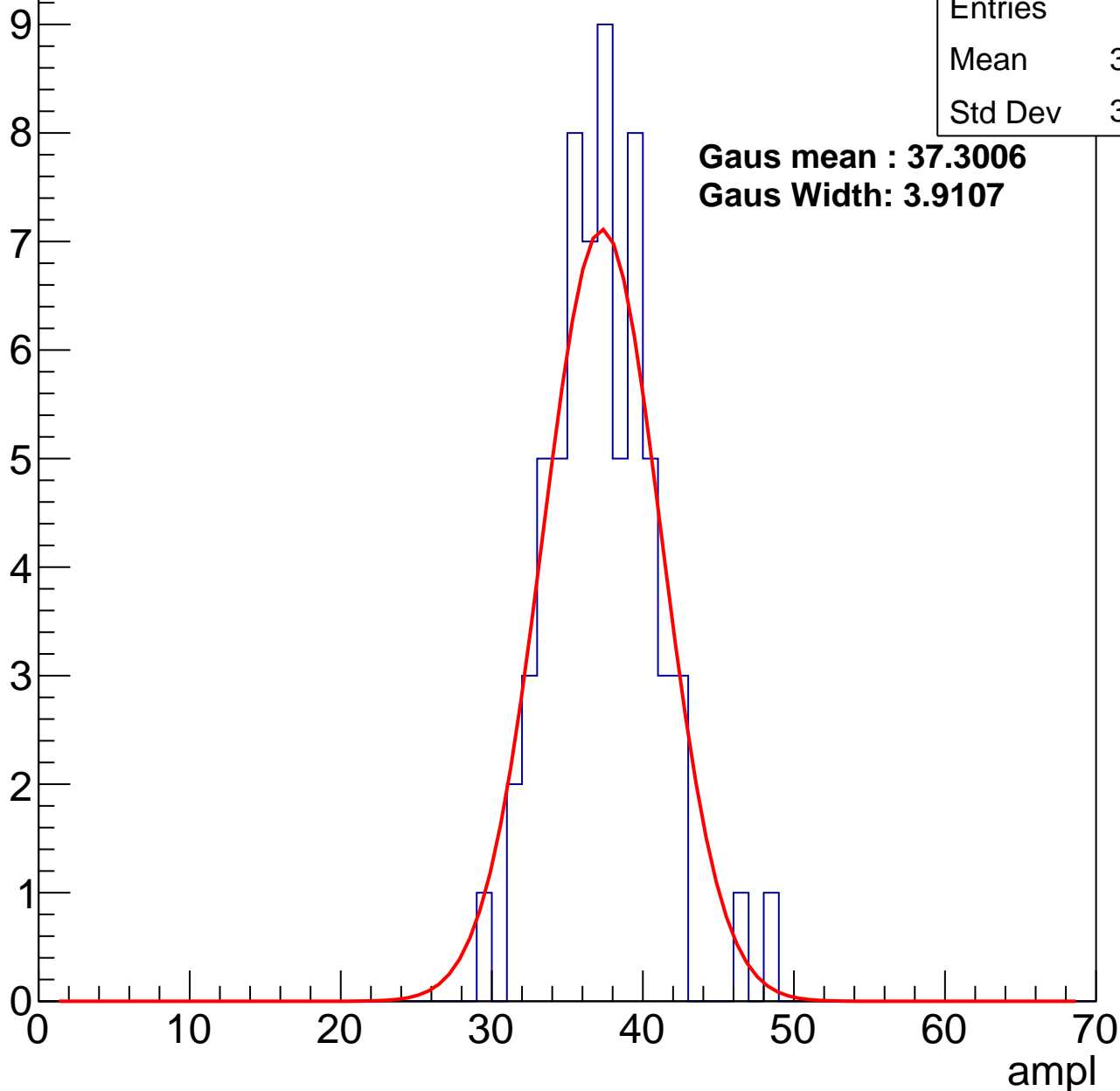
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	36.85
Std Dev	3.439

**Gaus mean : 37.3006**

**Gaus Width: 3.9107**



# B1L103S, U11-ch36, adc2

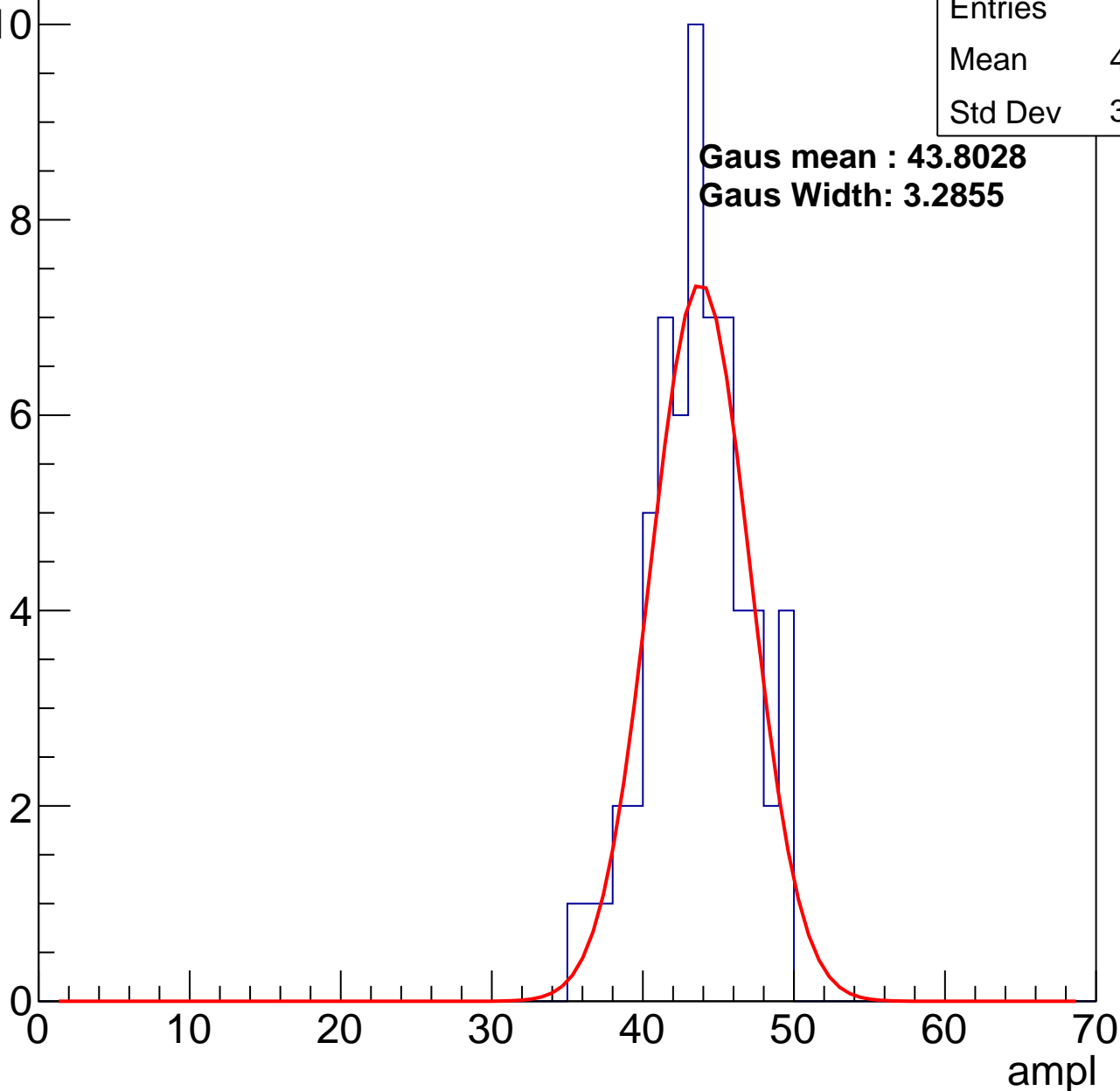
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	43.14
Std Dev	3.182

**Gaus mean : 43.8028**

**Gaus Width: 3.2855**

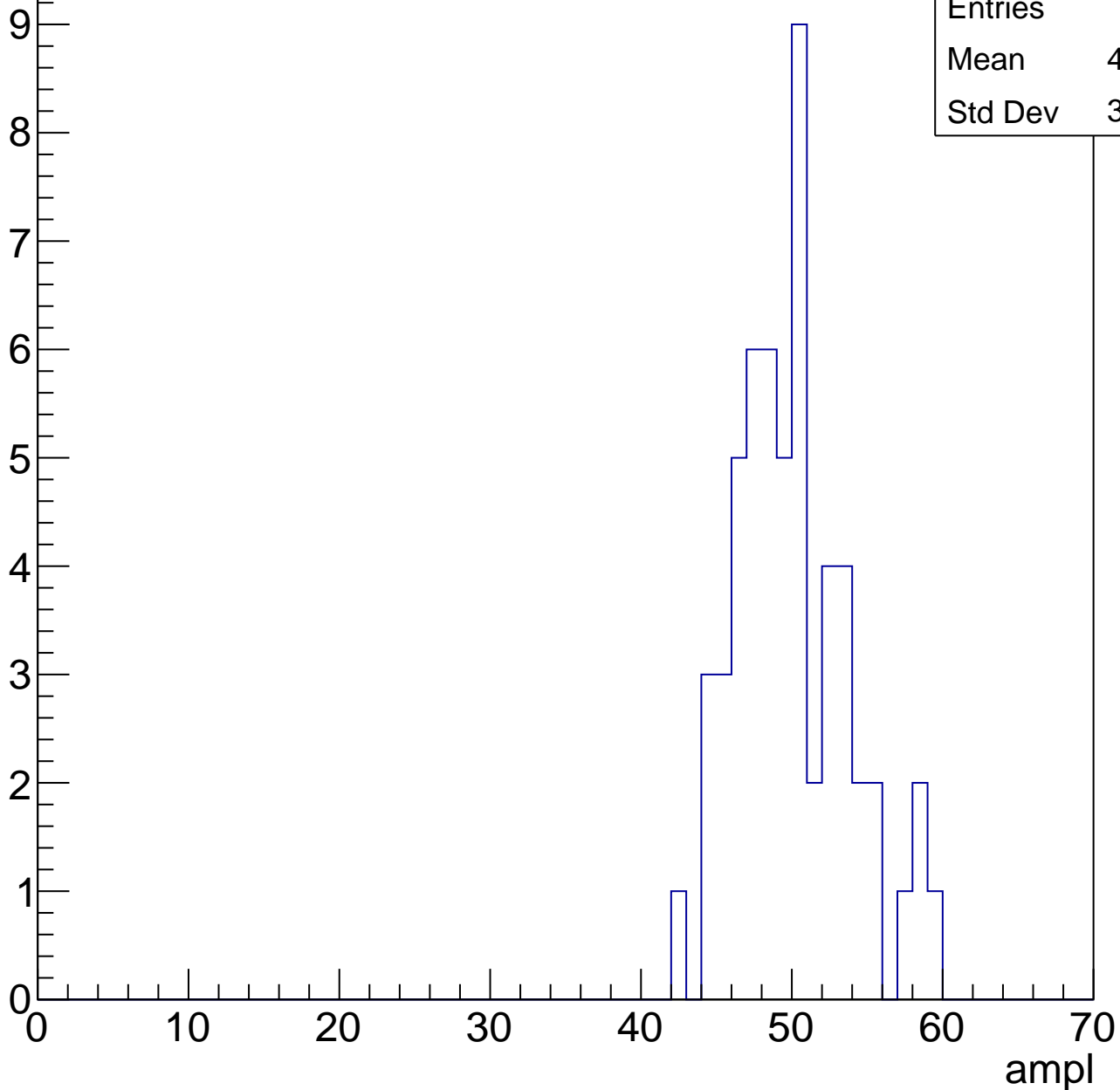


# B1L103S, U11-ch36, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	56
Mean	49.57
Std Dev	3.765

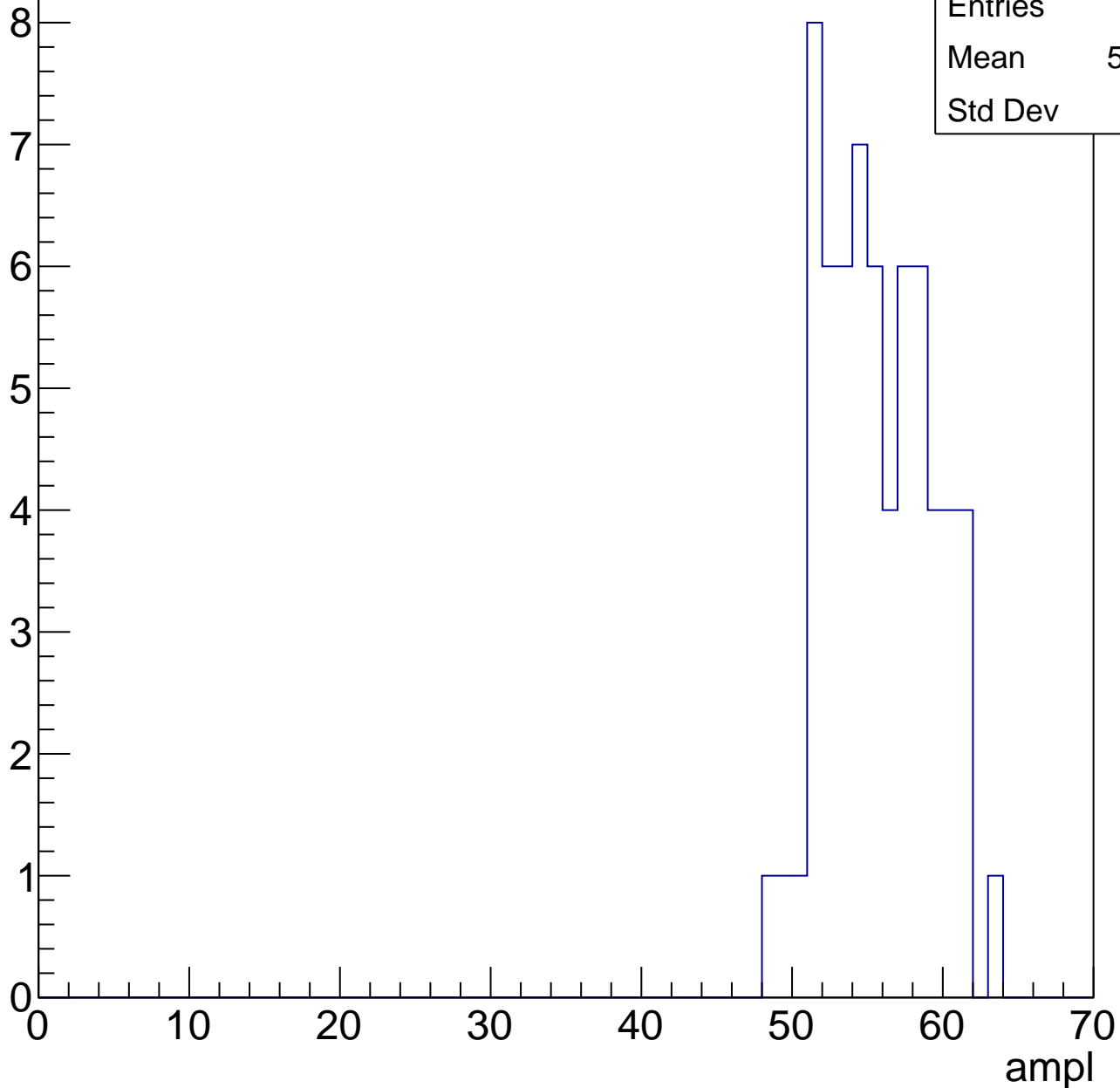


# B1L103S, U11-ch36, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	55.23
Std Dev	3.45

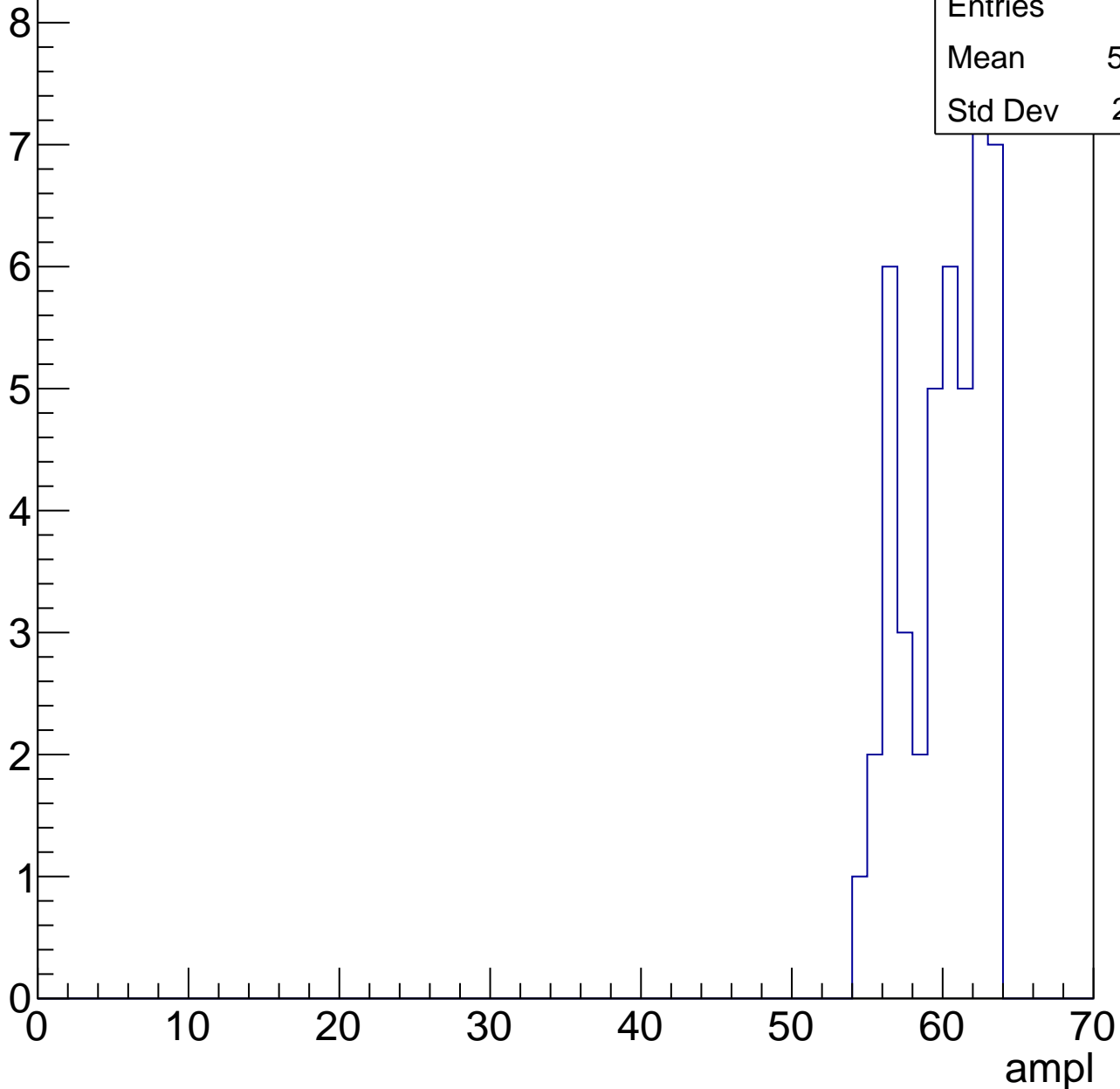


# B1L103S, U11-ch36, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	45
Mean	59.64
Std Dev	2.651



# B1L103S, U11-ch36, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

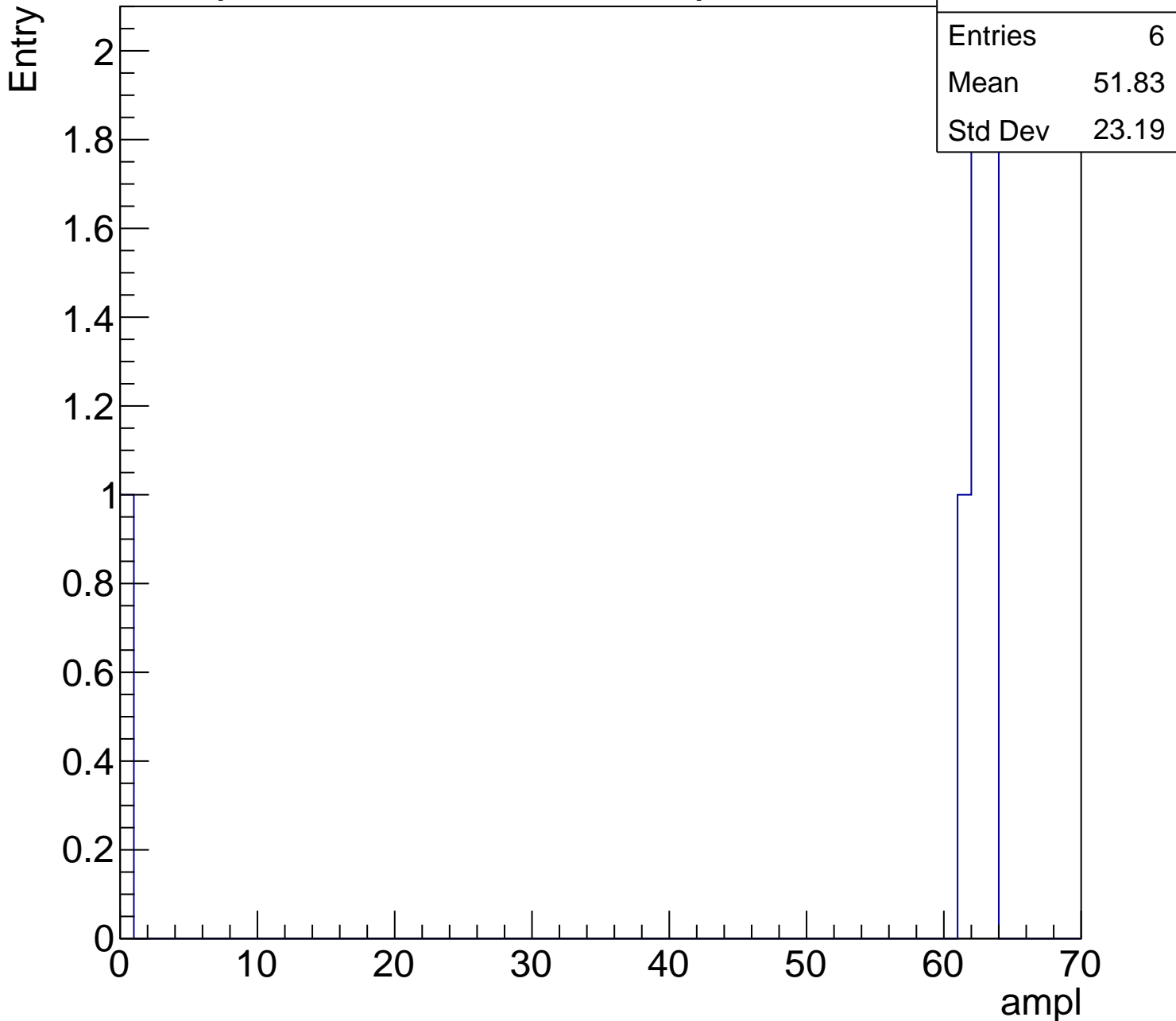
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	6
Mean	51.83
Std Dev	23.19

0 10 20 30 40 50 60 70

ampl





# B1L103S, U11-ch36, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L103S, U11-ch37, adc0

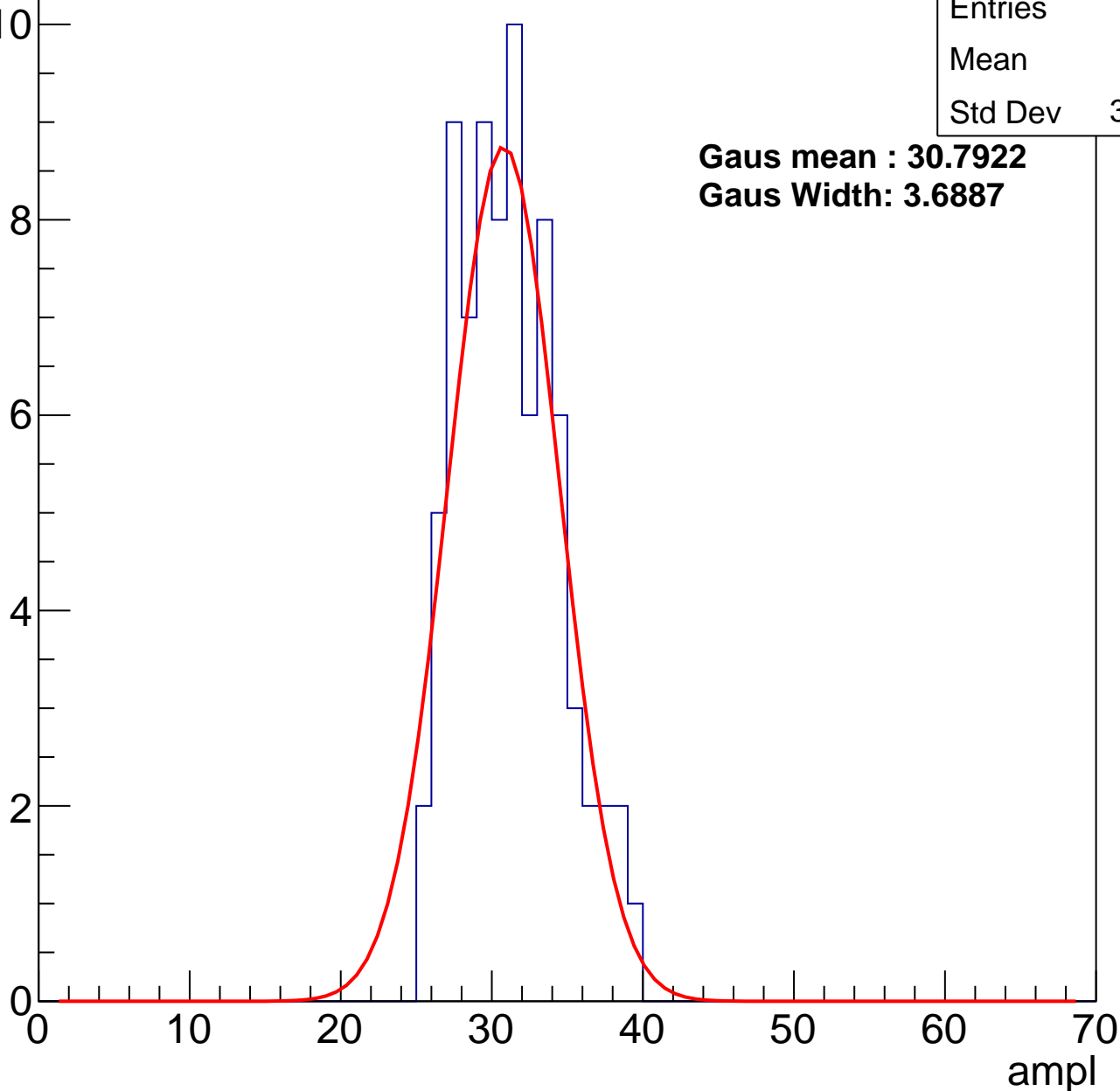
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	80
Mean	30.7
Std Dev	3.288

**Gaus mean : 30.7922**

**Gaus Width: 3.6887**



# B1L103S, U11-ch37, adc1

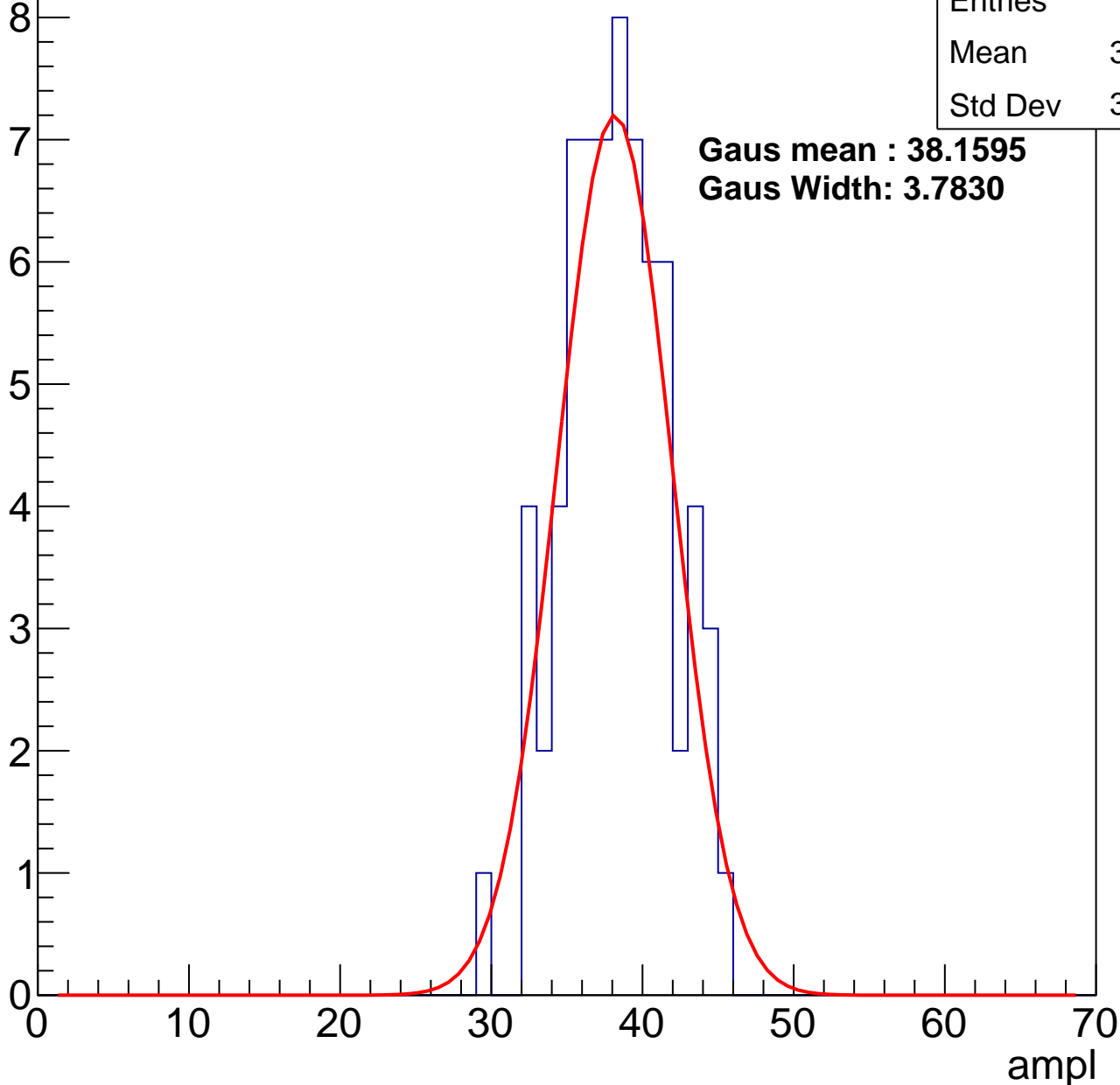
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	69
Mean	37.84
Std Dev	3.425

**Gaus mean : 38.1595**

**Gaus Width: 3.7830**



# B1L103S, U11-ch37, adc2

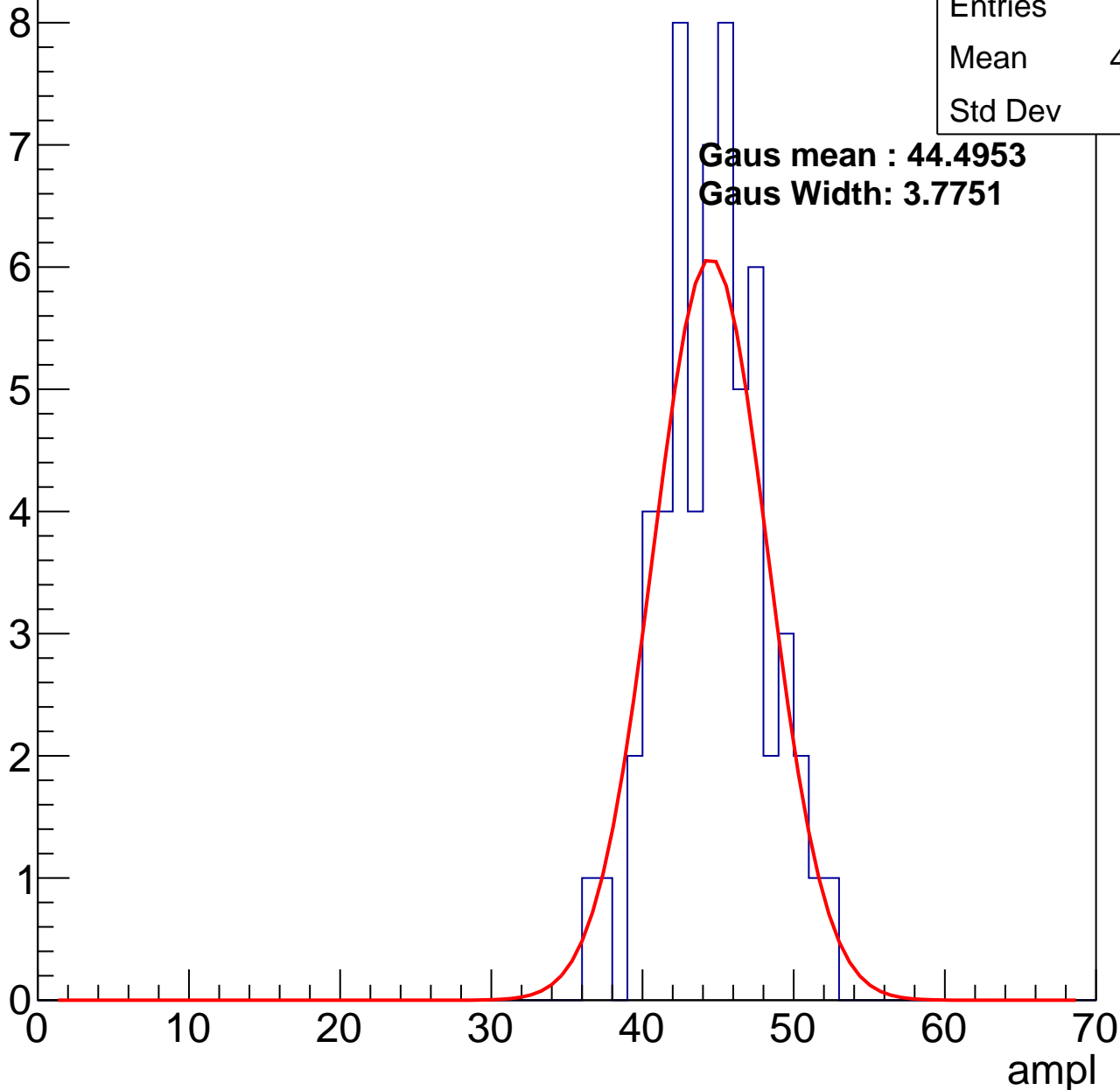
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	59
Mean	44.22
Std Dev	3.37

**Gaus mean : 44.4953**

**Gaus Width: 3.7751**

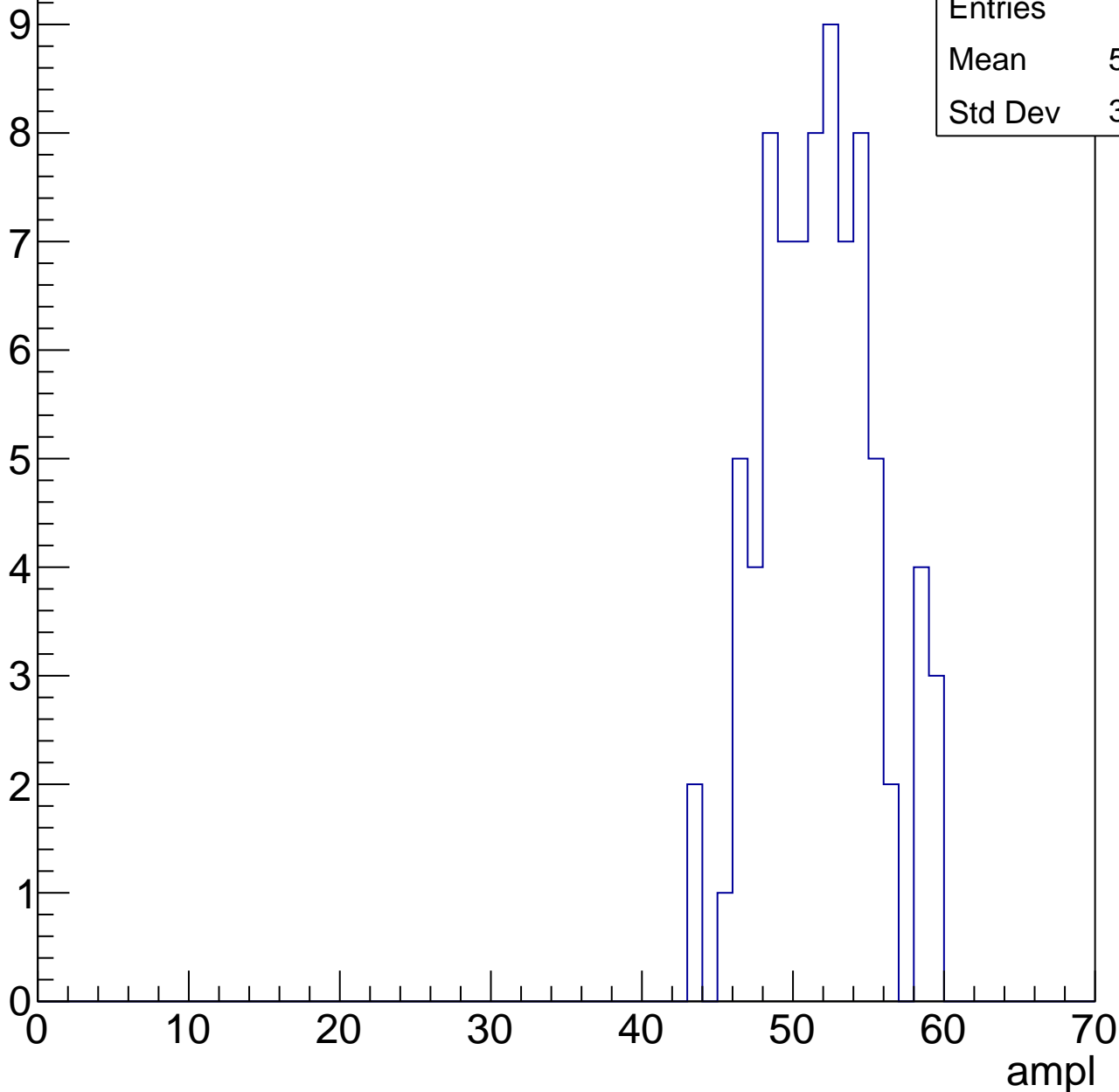


# B1L103S, U11-ch37, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	80
Mean	51.26
Std Dev	3.677

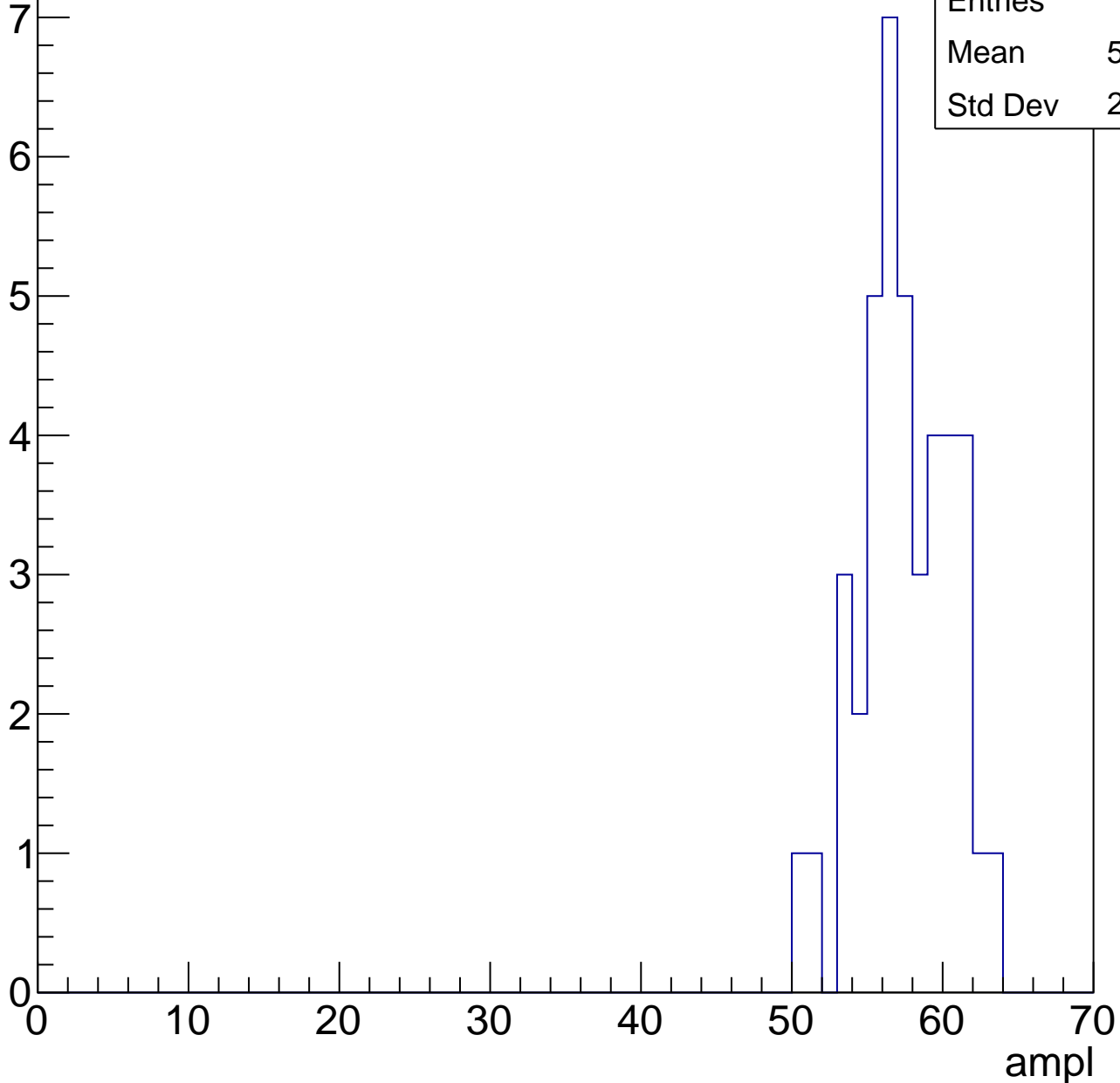


# B1L103S, U11-ch37, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	41
Mean	57.05
Std Dev	2.955

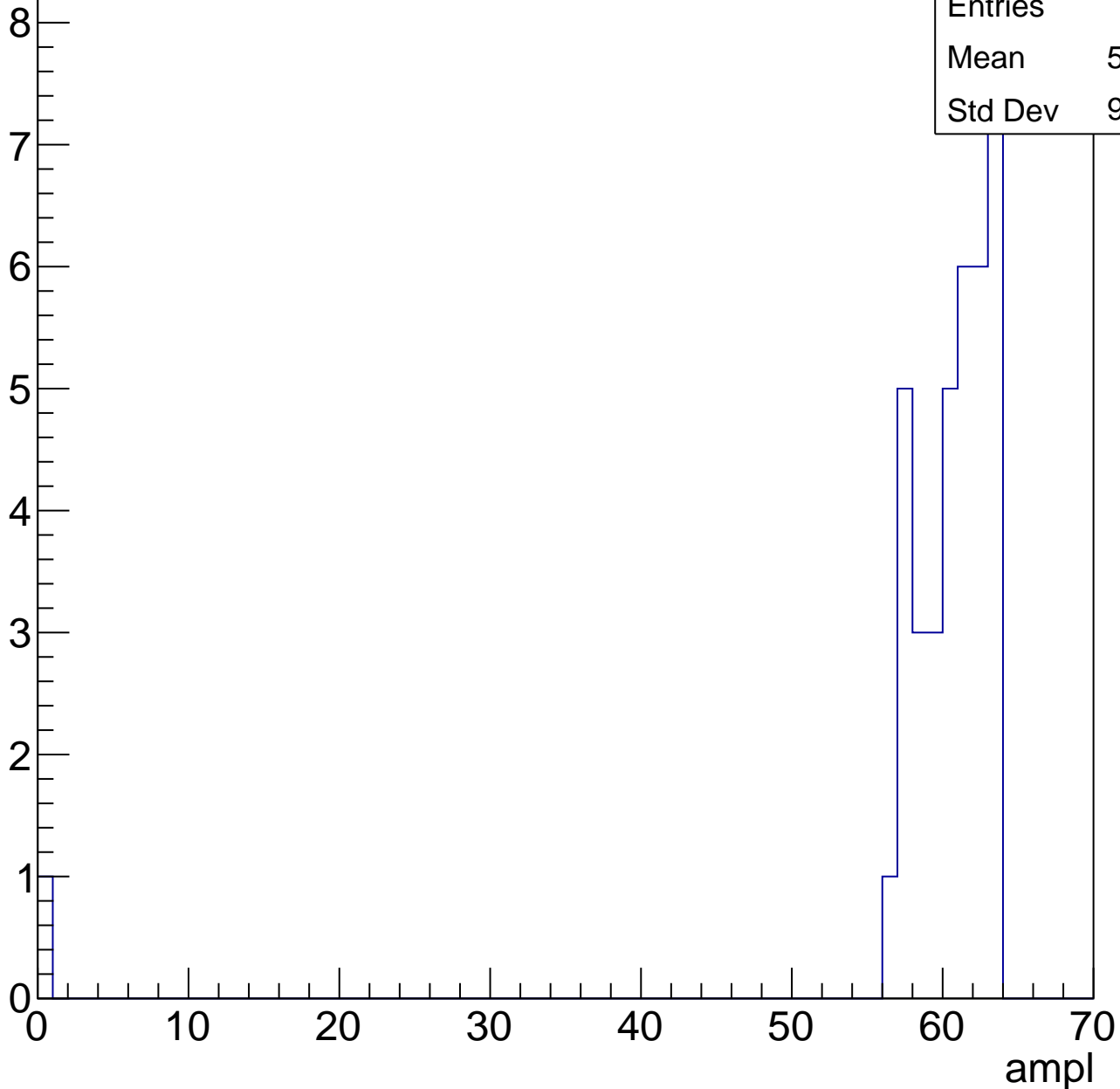


# B1L103S, U11-ch37, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

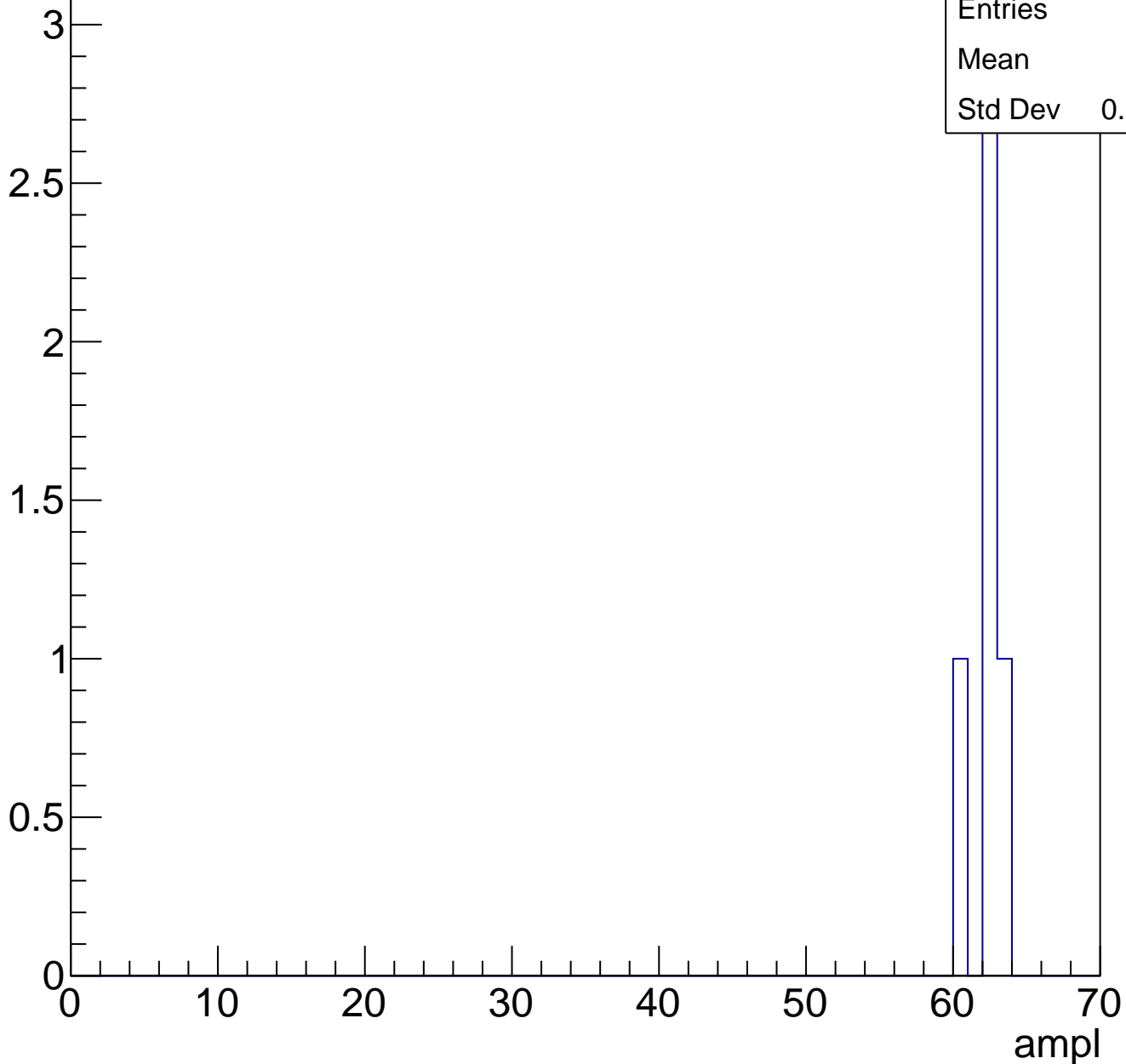
Entries	38
Mean	58.79
Std Dev	9.897



# B1L103S, U11-ch37, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U11-ch37, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U11-ch38, adc0

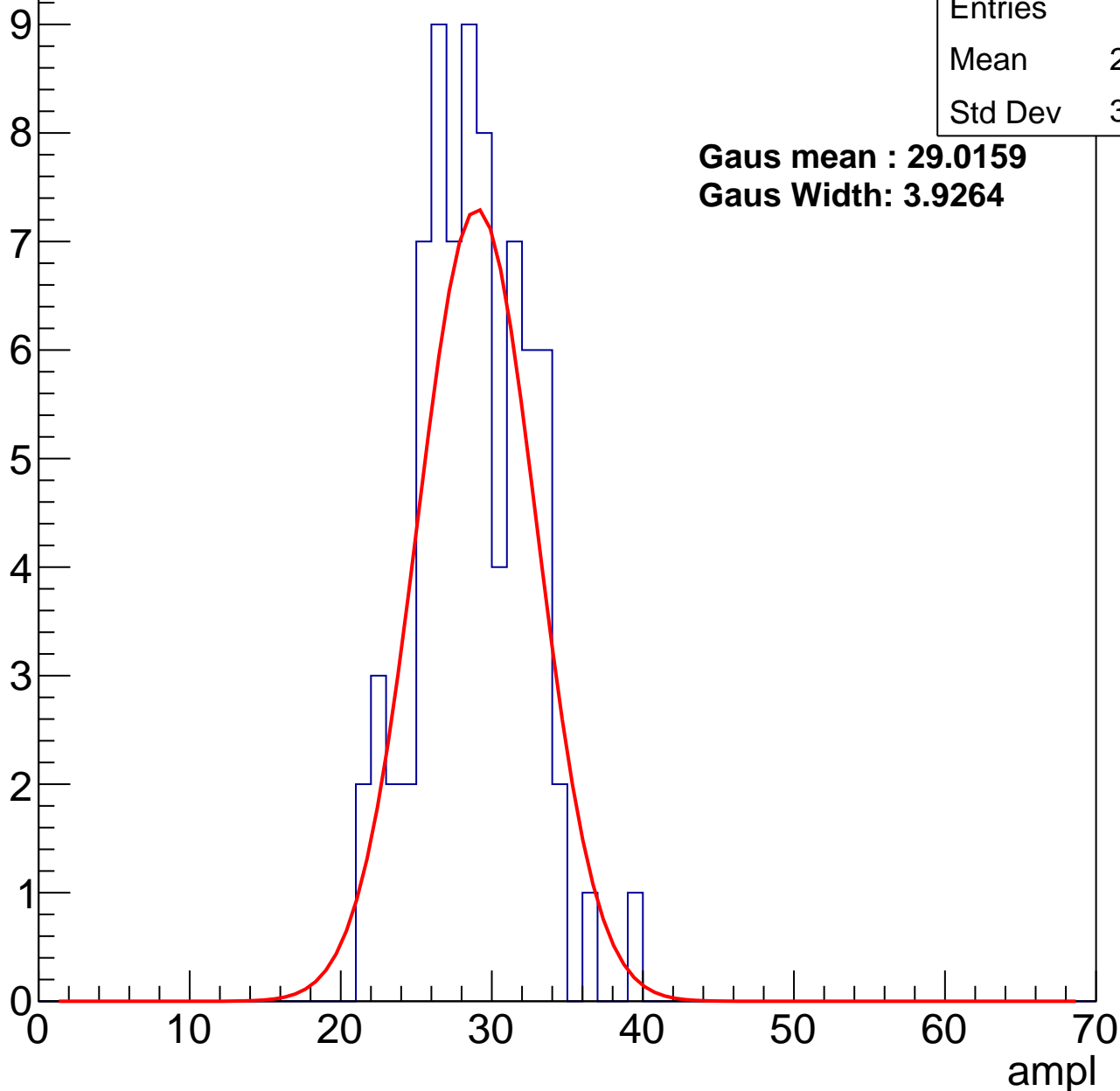
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	76
Mean	28.34
Std Dev	3.582

**Gaus mean : 29.0159**

**Gaus Width: 3.9264**



# B1L103S, U11-ch38, adc1

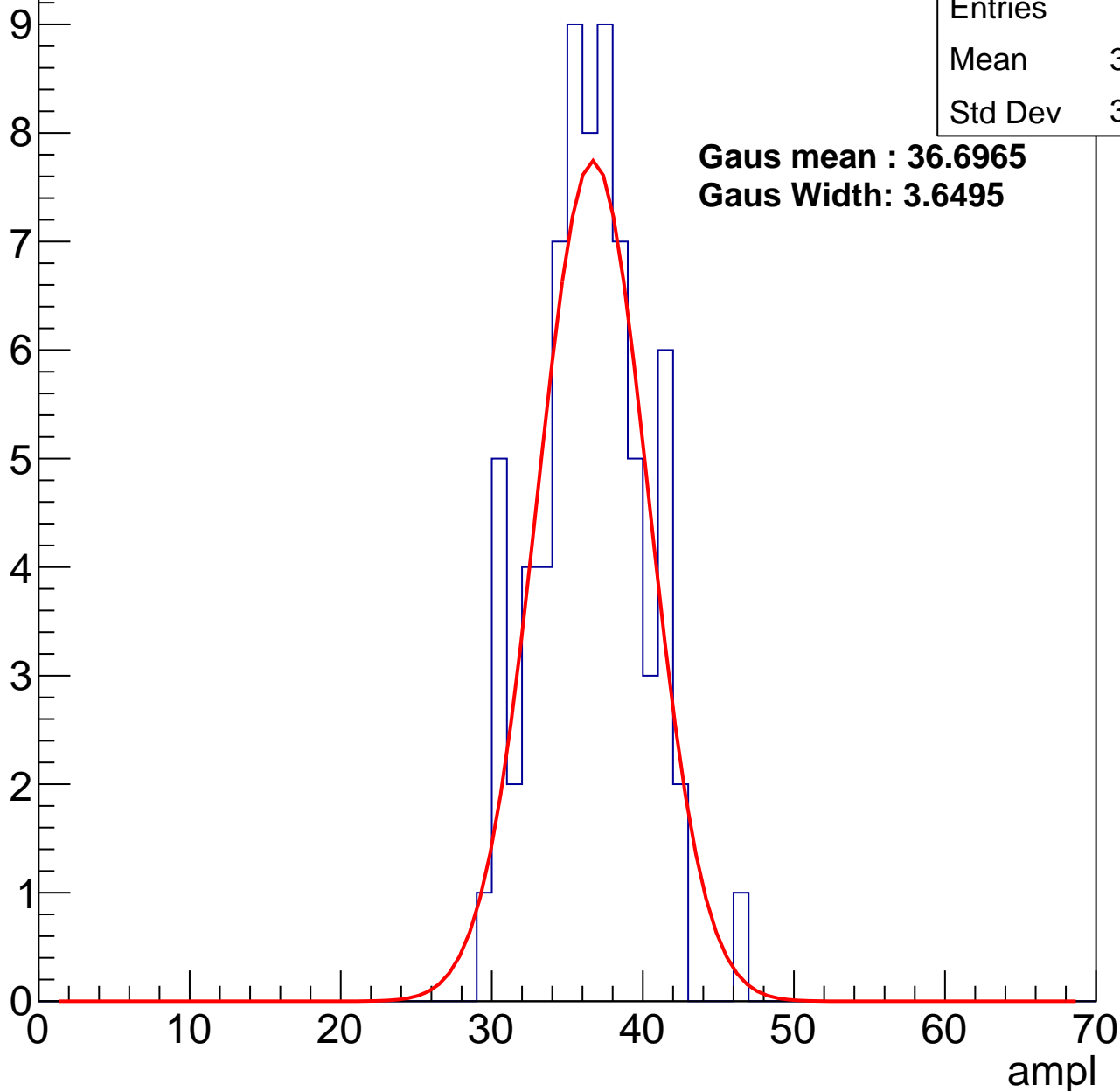
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	73
Mean	36.05
Std Dev	3.448

**Gaus mean : 36.6965**

**Gaus Width: 3.6495**



# B1L103S, U11-ch38, adc2

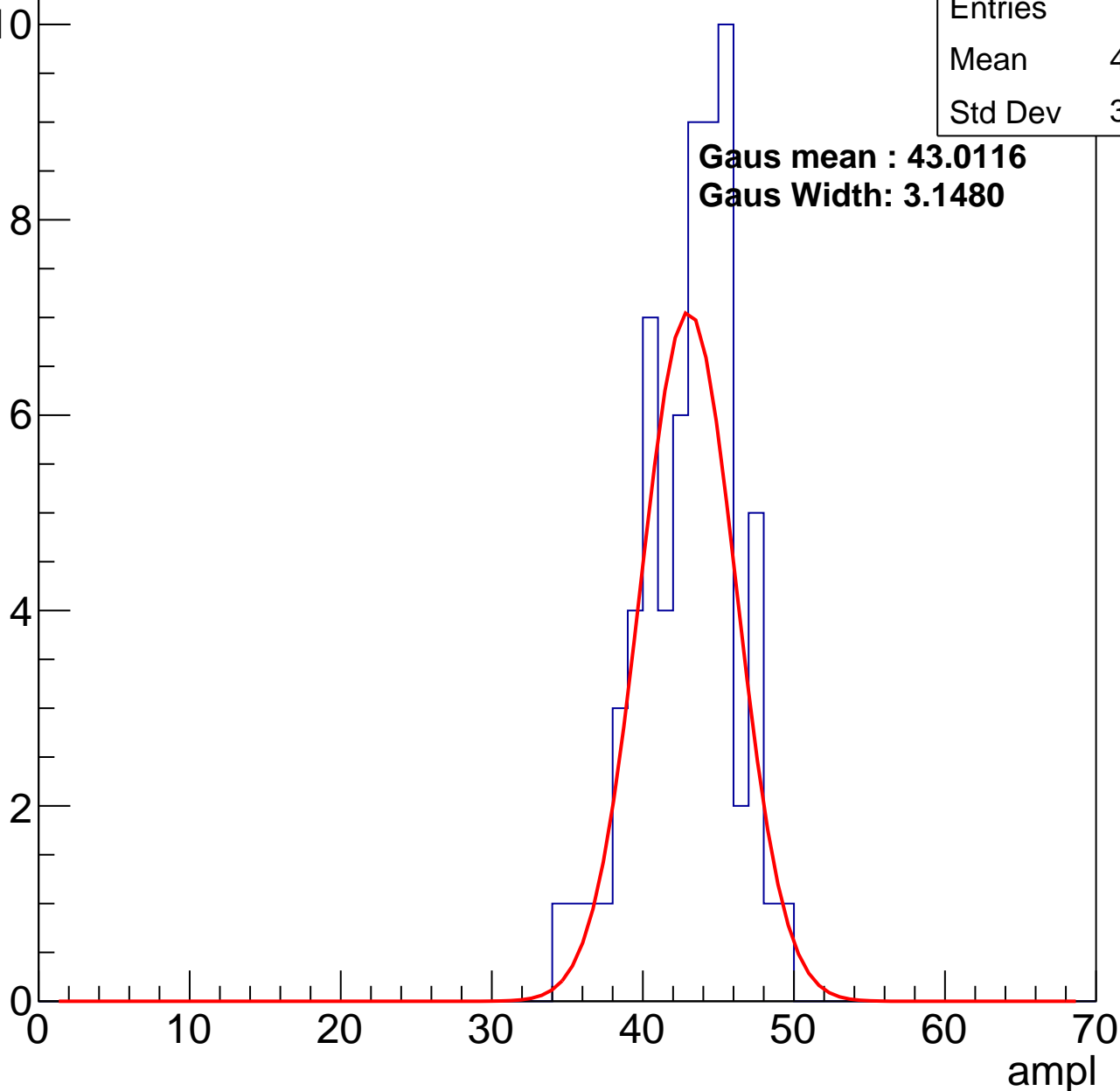
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	42.54
Std Dev	3.158

**Gaus mean : 43.0116**

**Gaus Width: 3.1480**

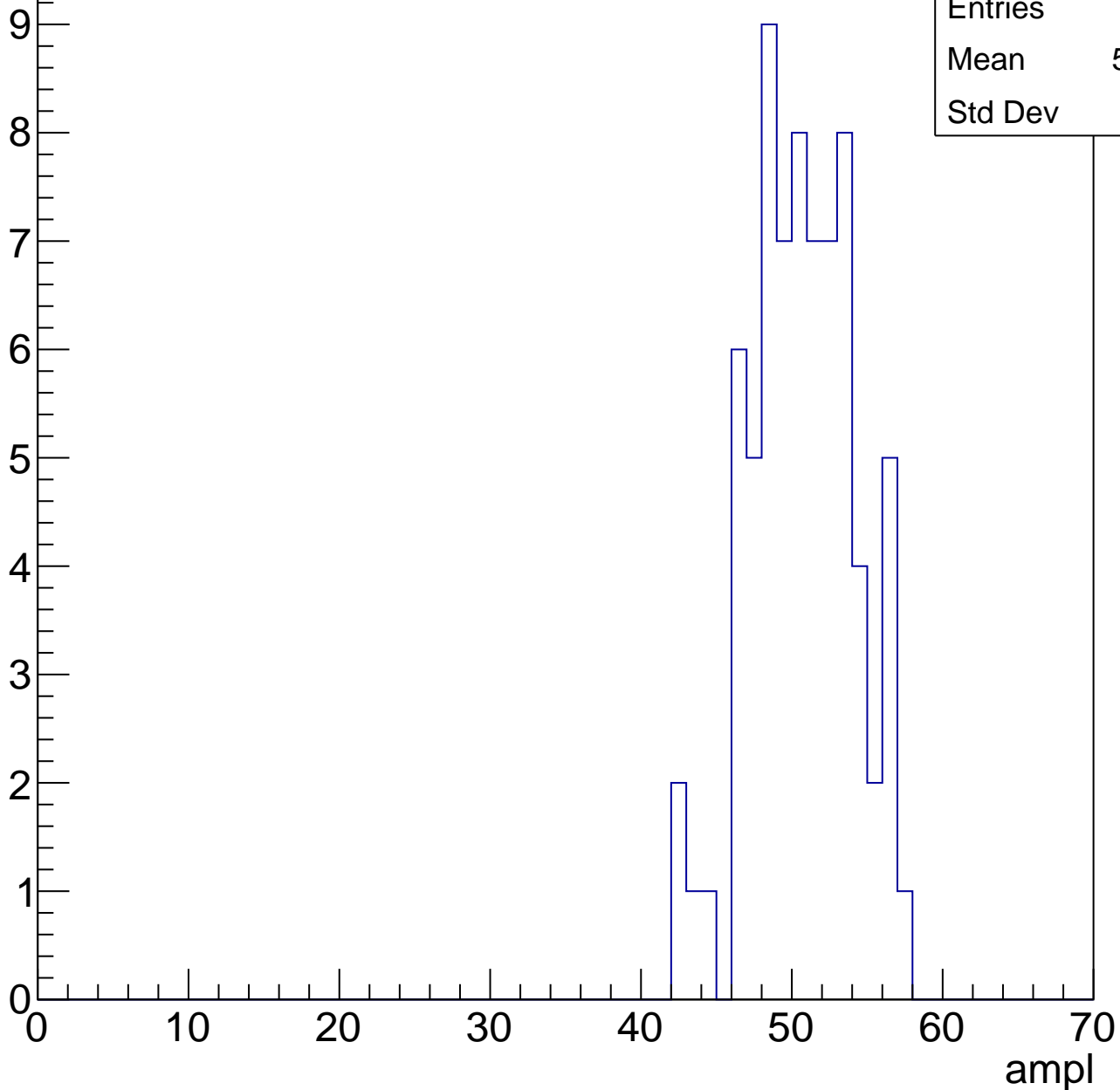


# B1L103S, U11-ch38, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	73
Mean	50.21
Std Dev	3.4

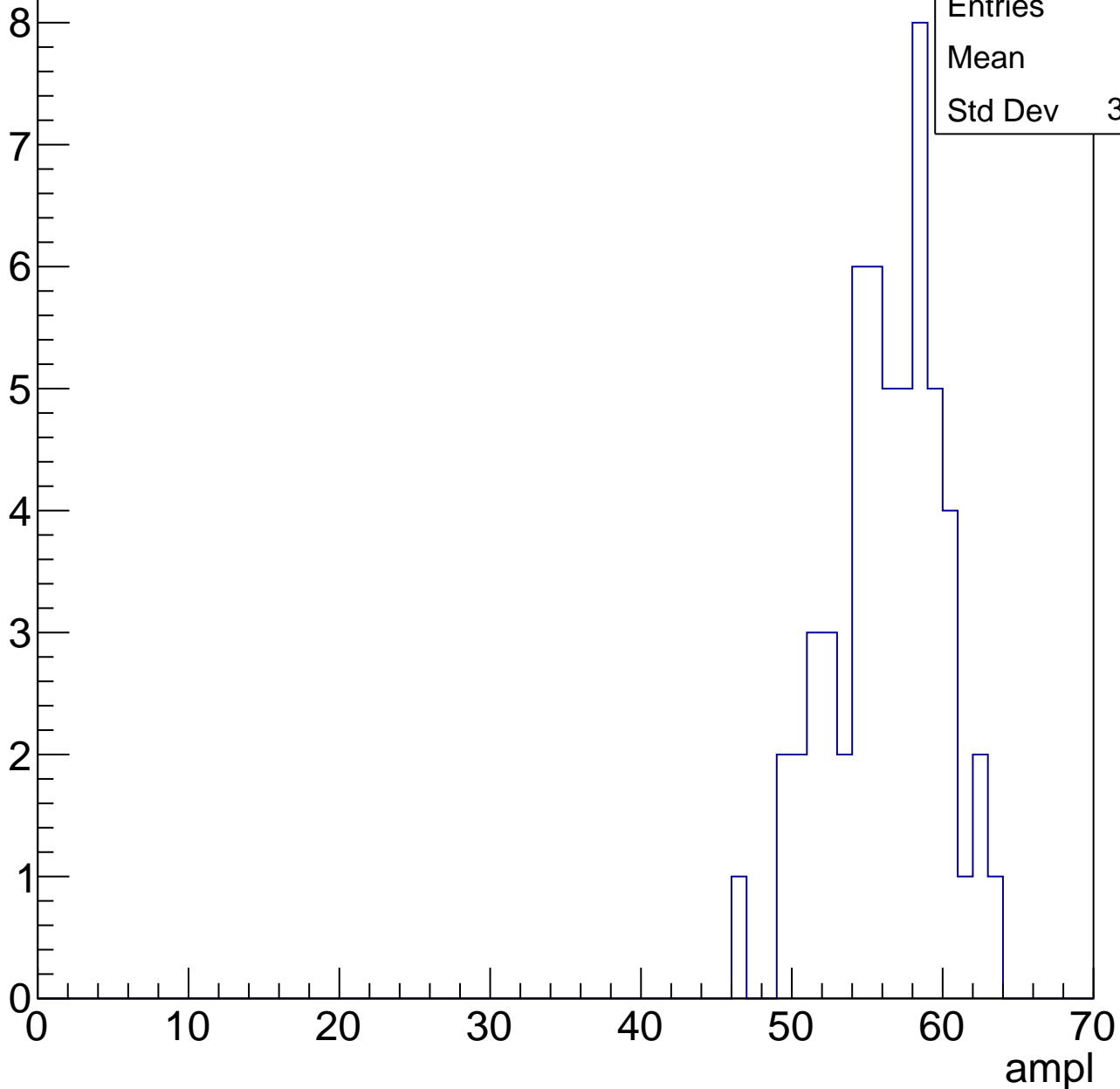


# B1L103S, U11-ch38, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	56
Mean	55.8
Std Dev	3.613

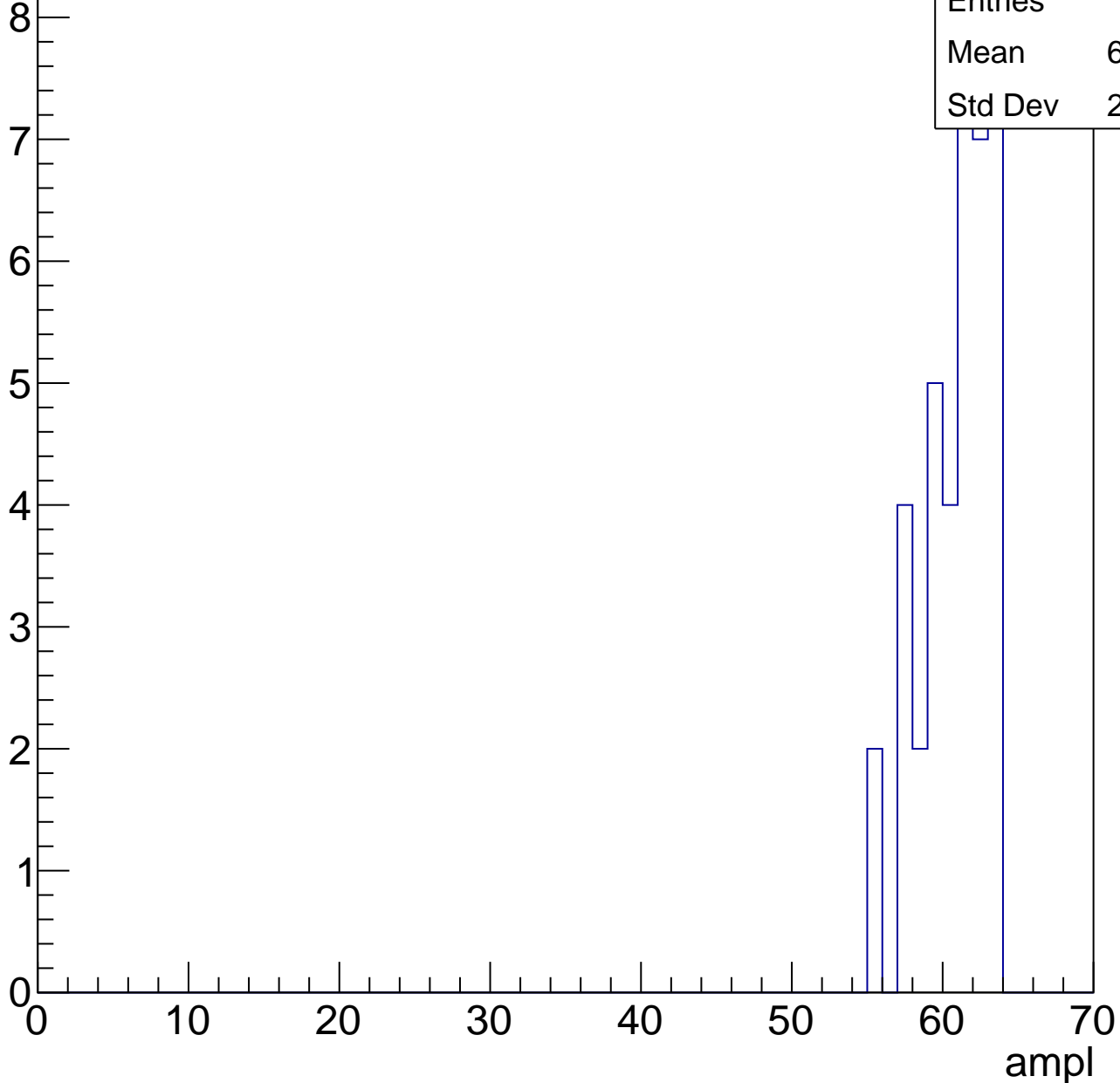


# B1L103S, U11-ch38, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	40
Mean	60.38
Std Dev	2.244



# B1L103S, U11-ch38, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	6
Mean	51
Std Dev	22.83

ampl

0 10 20 30 40 50 60 70



# B1L103S, U11-ch38, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L103S, U11-ch39, adc0

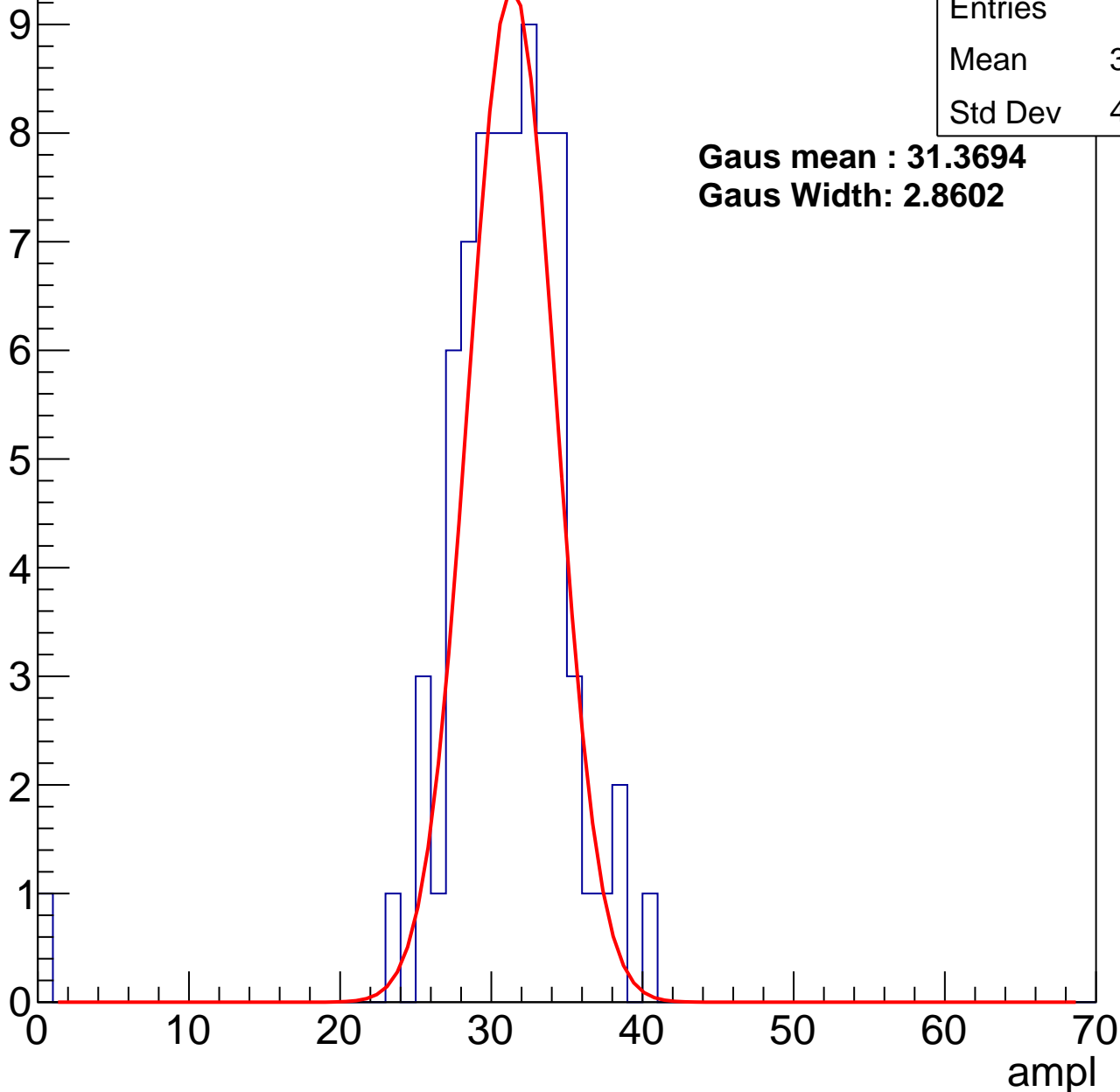
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	76
Mean	30.53
Std Dev	4.786

**Gaus mean : 31.3694**

**Gaus Width: 2.8602**



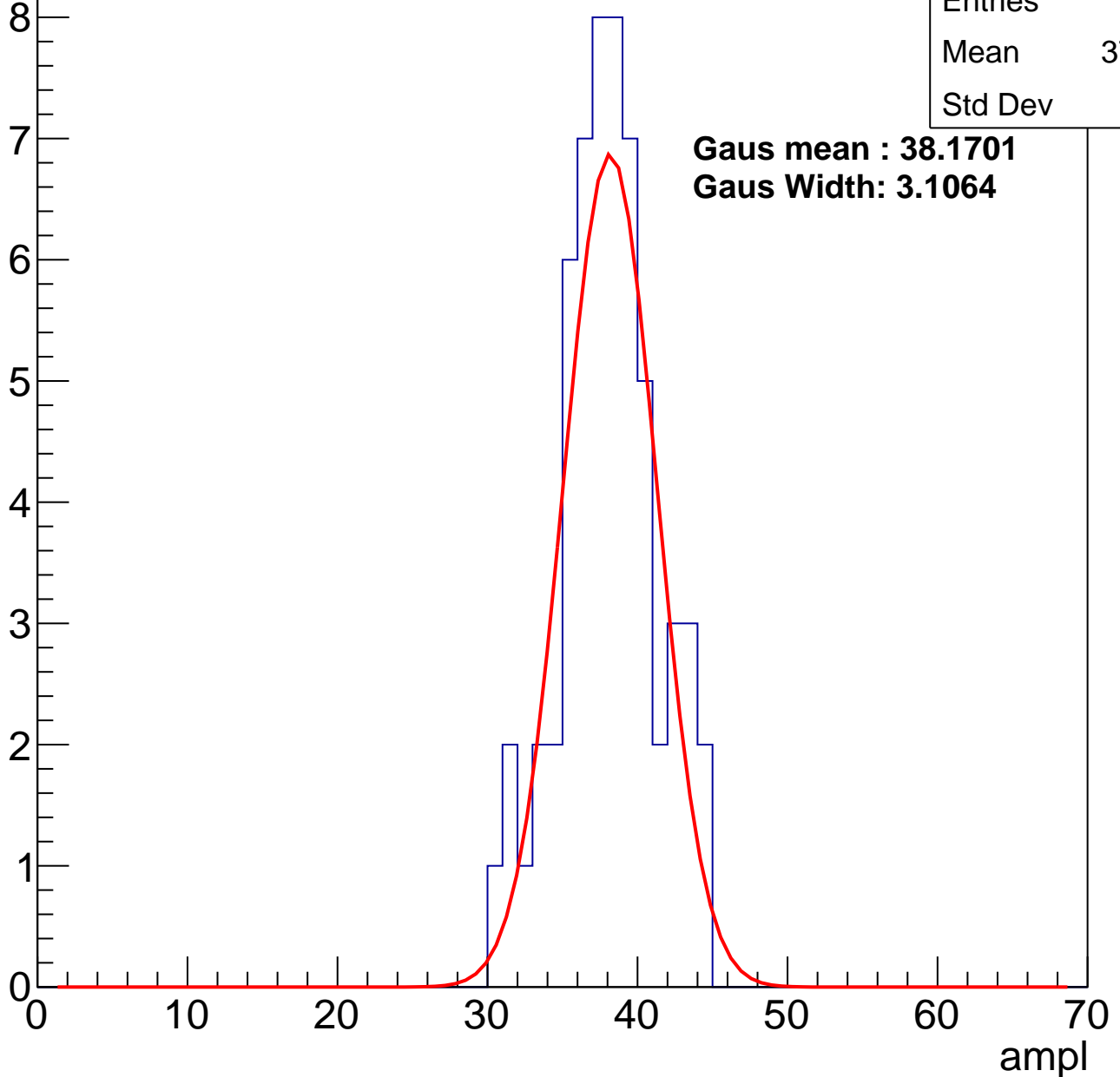
# B1L103S, U11-ch39, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	59
Mean	37.59
Std Dev	3.19

**Gaus mean : 38.1701**  
**Gaus Width: 3.1064**



# B1L103S, U11-ch39, adc2

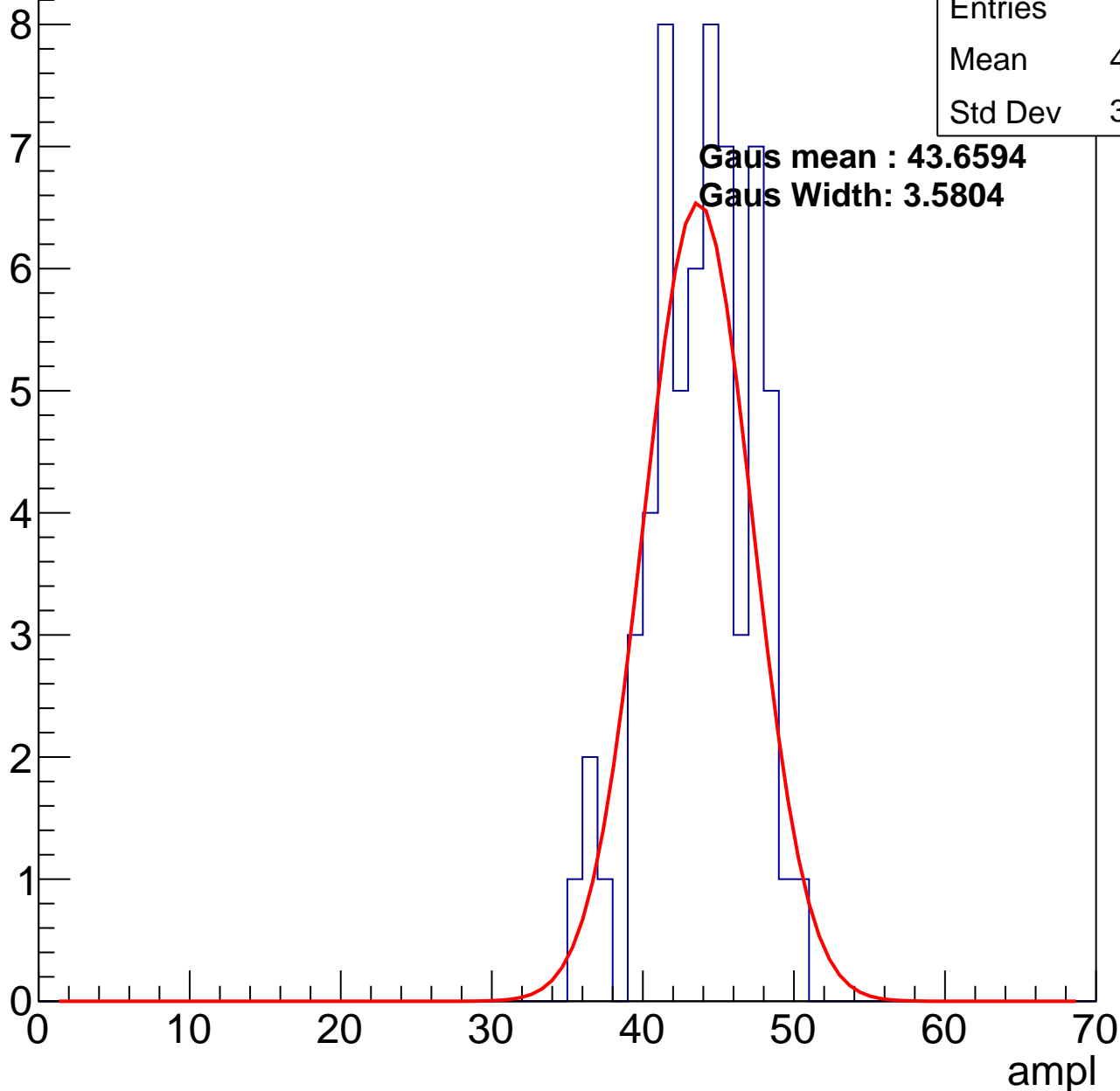
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	43.39
Std Dev	3.347

**Gaus mean : 43.6594**

**Gaus Width: 3.5804**

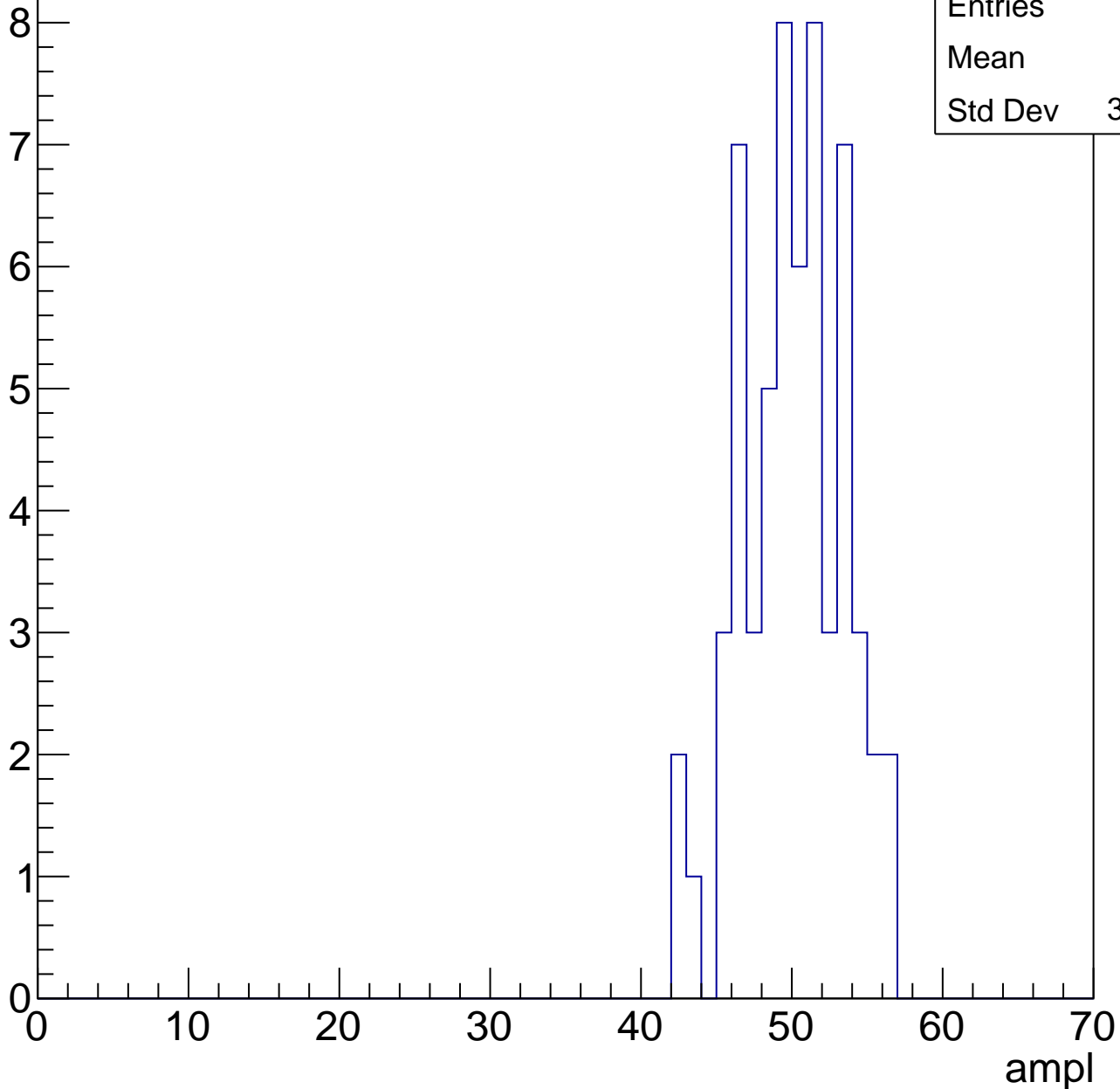


# B1L103S, U11-ch39, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	60
Mean	49.6
Std Dev	3.323

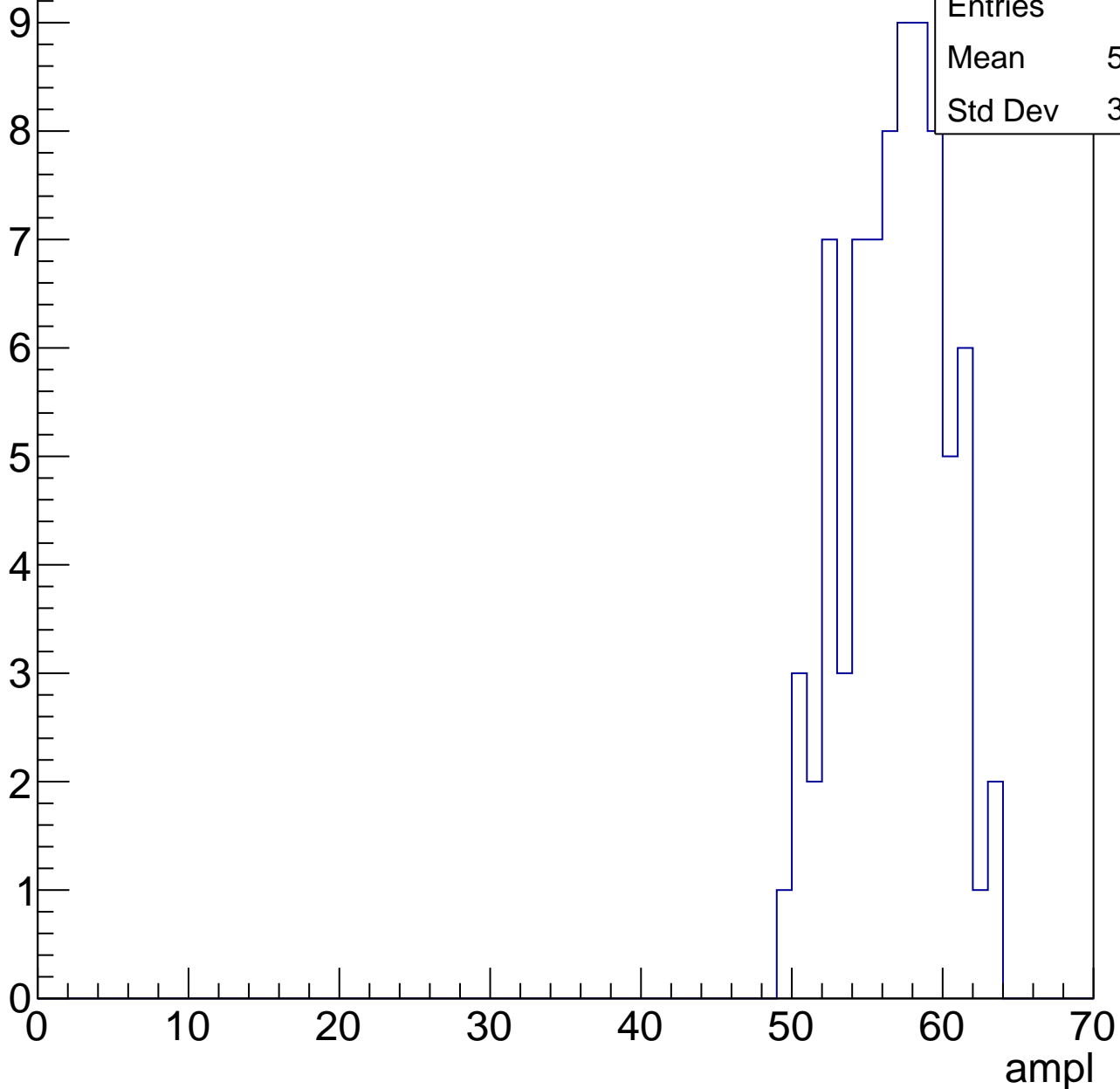


# B1L103S, U11-ch39, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	78
Mean	56.36
Std Dev	3.305

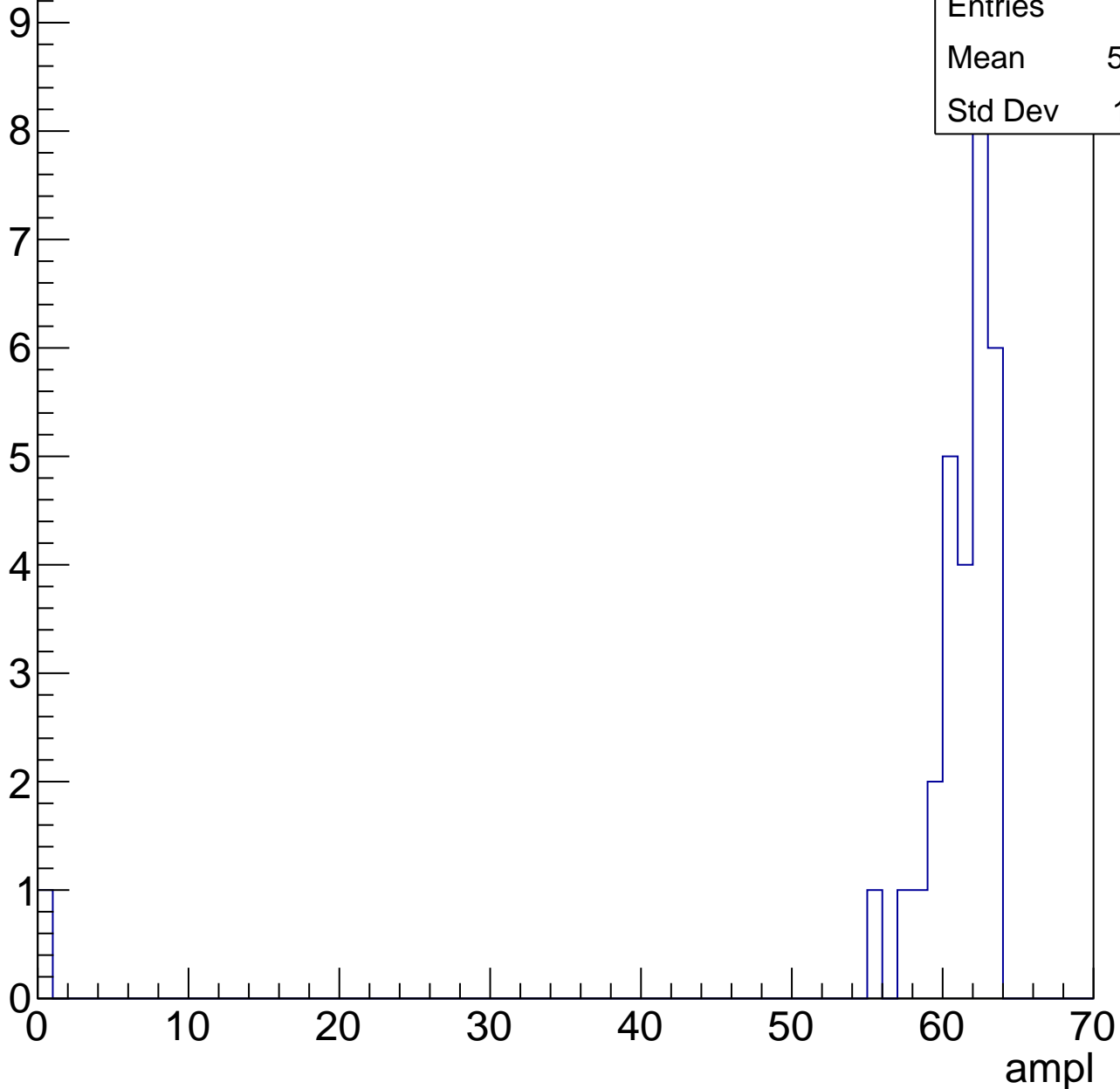


# B1L103S, U11-ch39, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	30
Mean	58.93
Std Dev	11.11



# B1L103S, U11-ch39, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U11-ch39, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U11-ch40, adc0

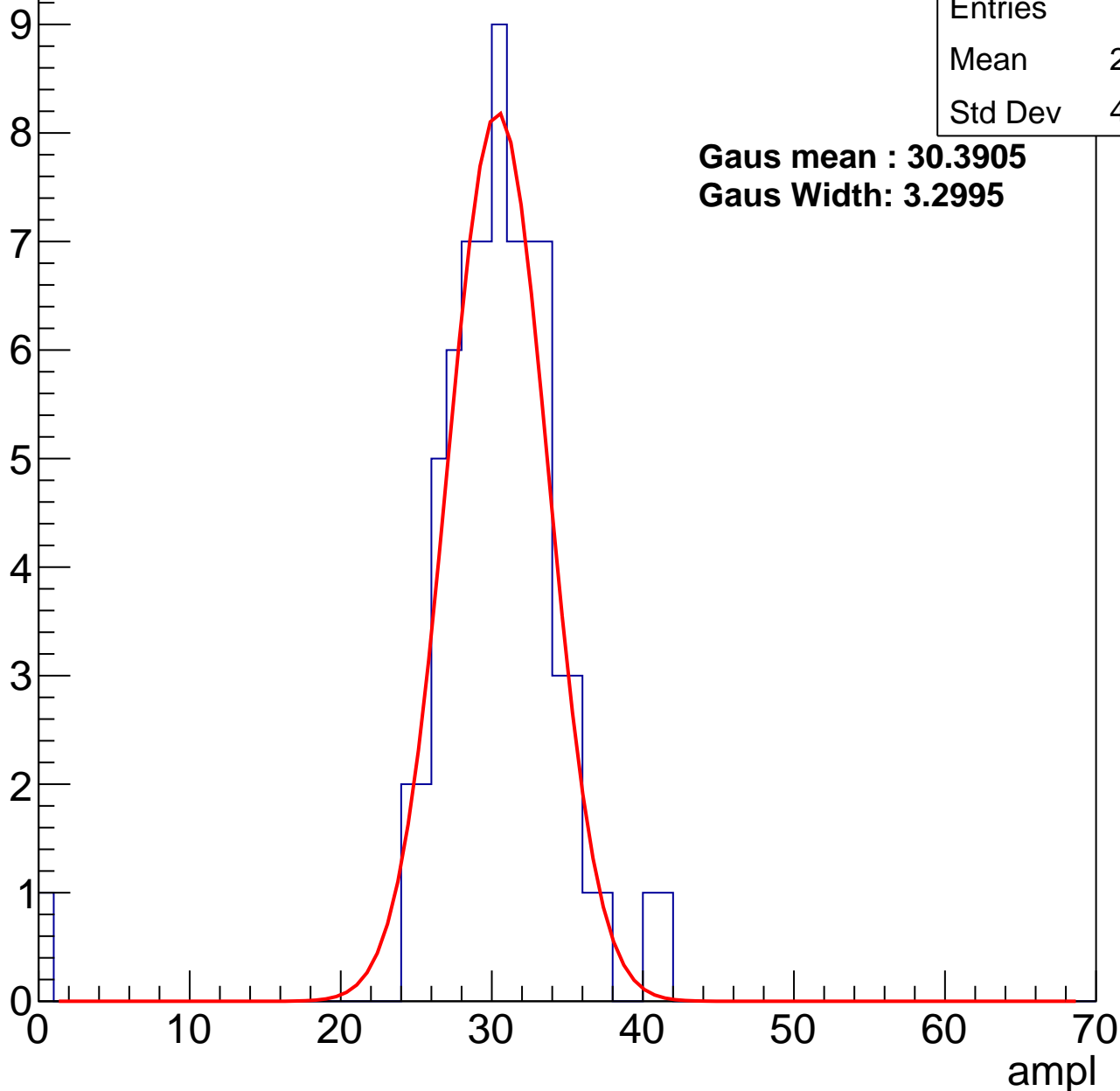
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	70
Mean	29.89
Std Dev	4.953

**Gaus mean : 30.3905**

**Gaus Width: 3.2995**



# B1L103S, U11-ch40, adc1

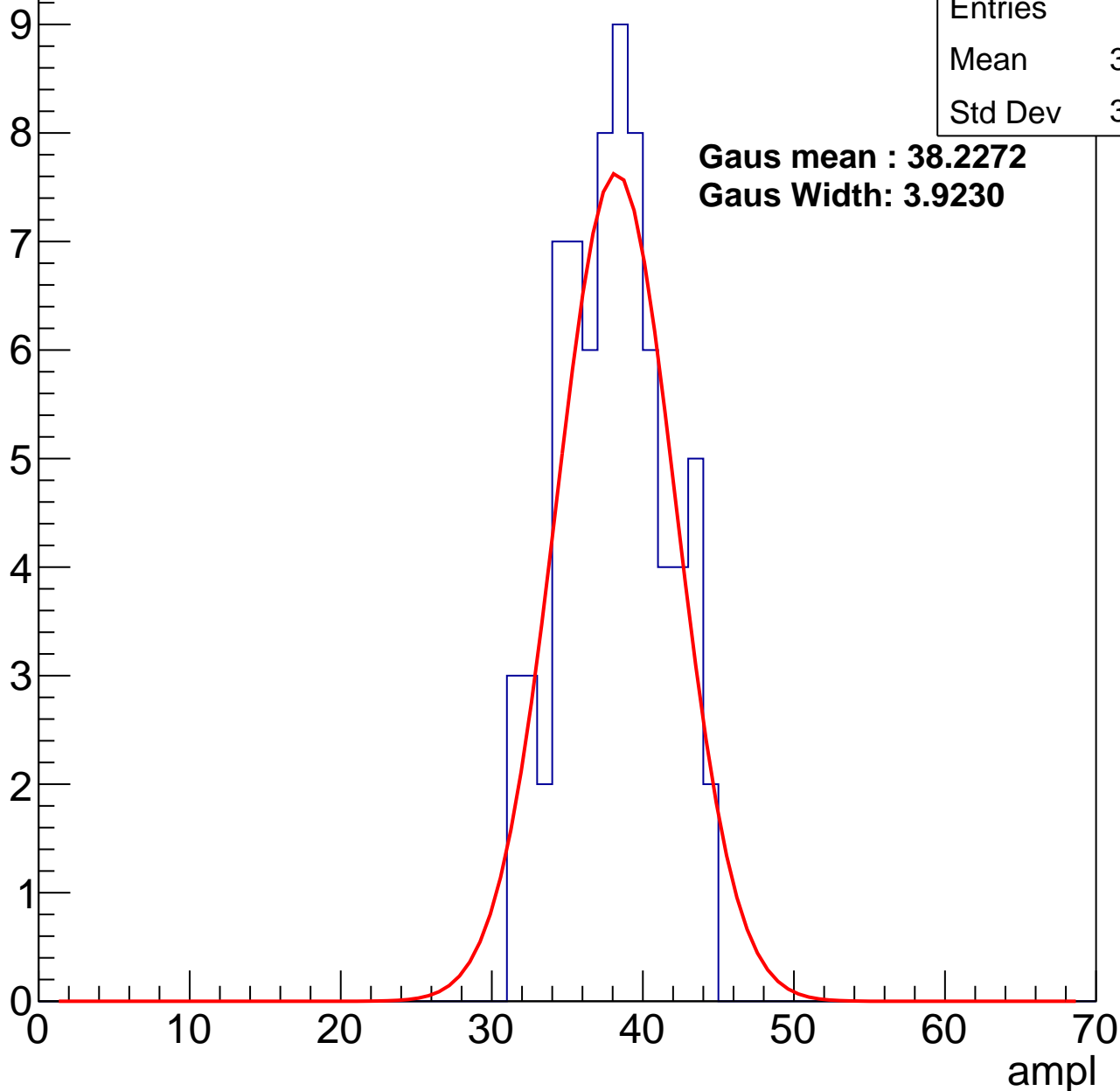
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	74
Mean	37.55
Std Dev	3.342

**Gaus mean : 38.2272**

**Gaus Width: 3.9230**



# B1L103S, U11-ch40, adc2

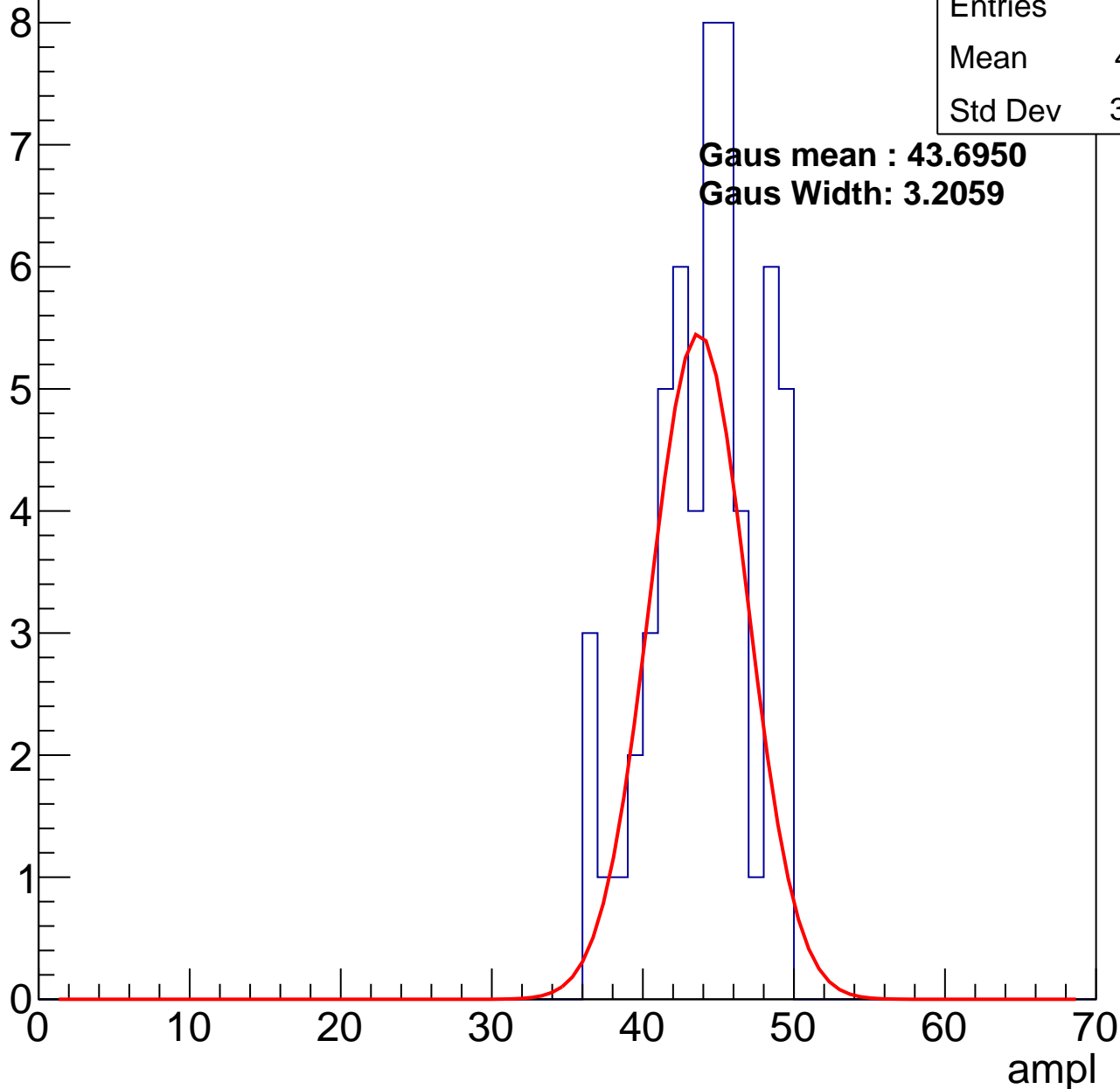
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	57
Mean	43.61
Std Dev	3.488

**Gaus mean : 43.6950**

**Gaus Width: 3.2059**

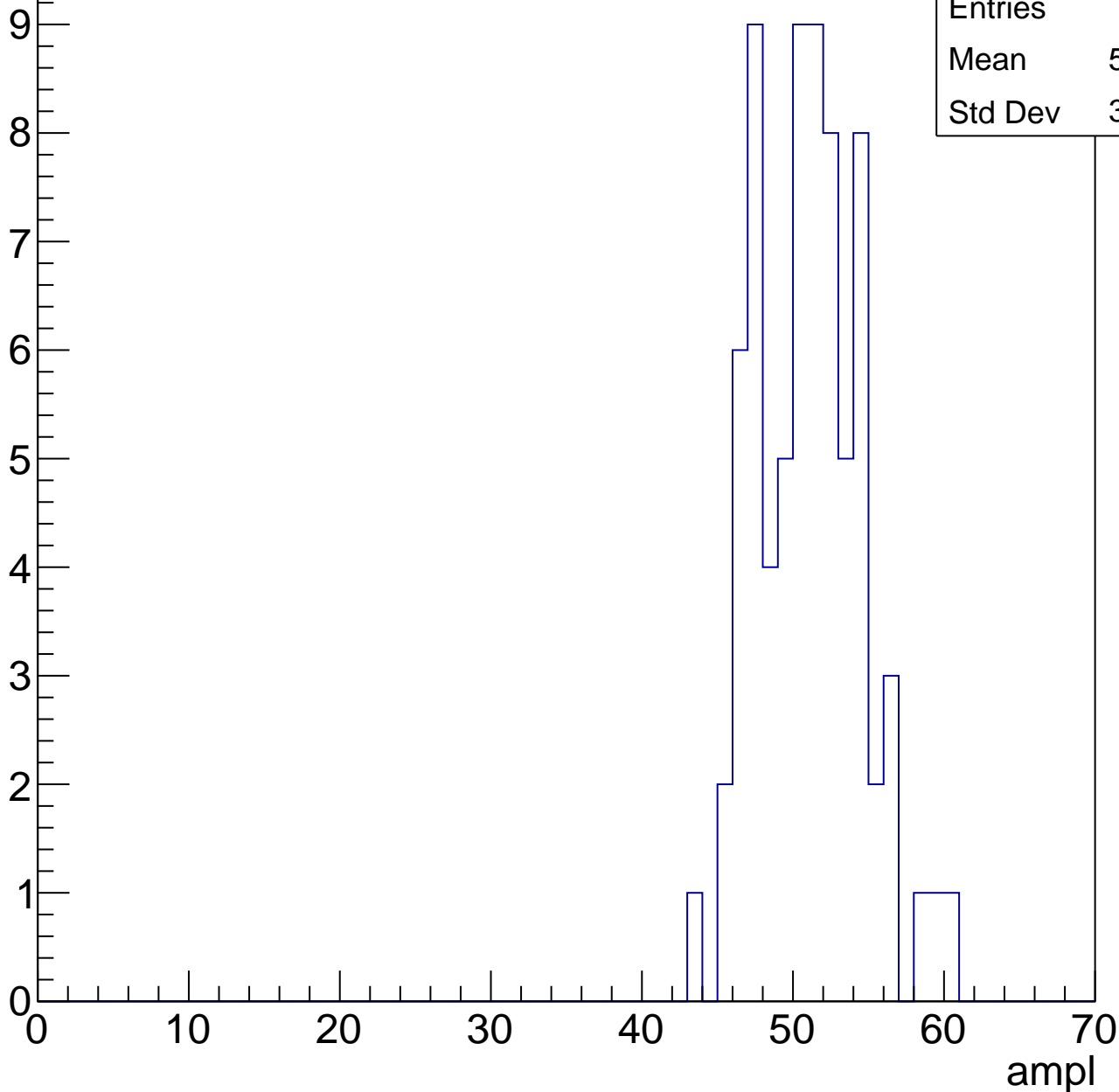


# B1L103S, U11-ch40, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

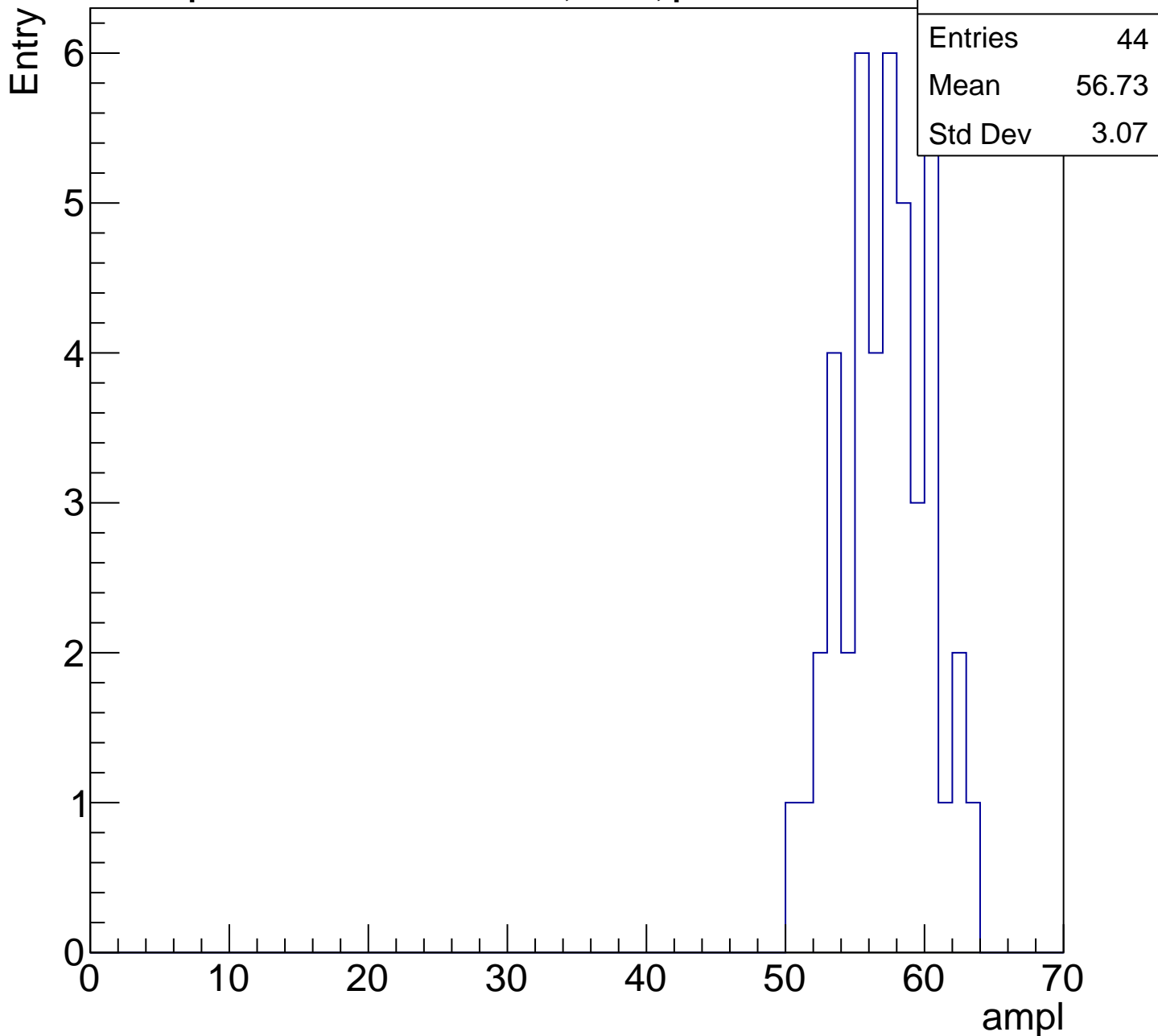
Entry

Entries	74
Mean	50.62
Std Dev	3.459



# B1L103S, U11-ch40, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

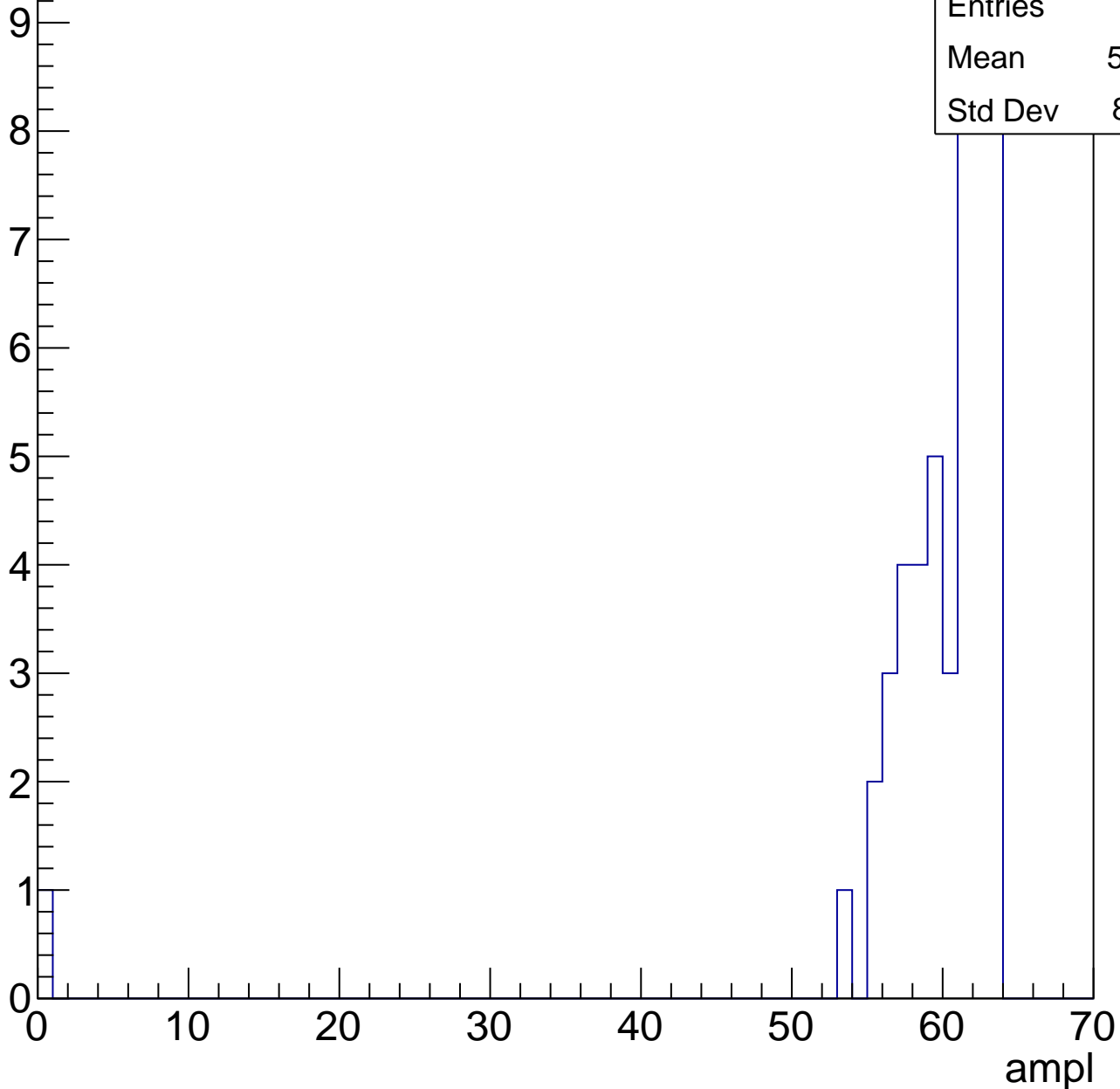


# B1L103S, U11-ch40, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

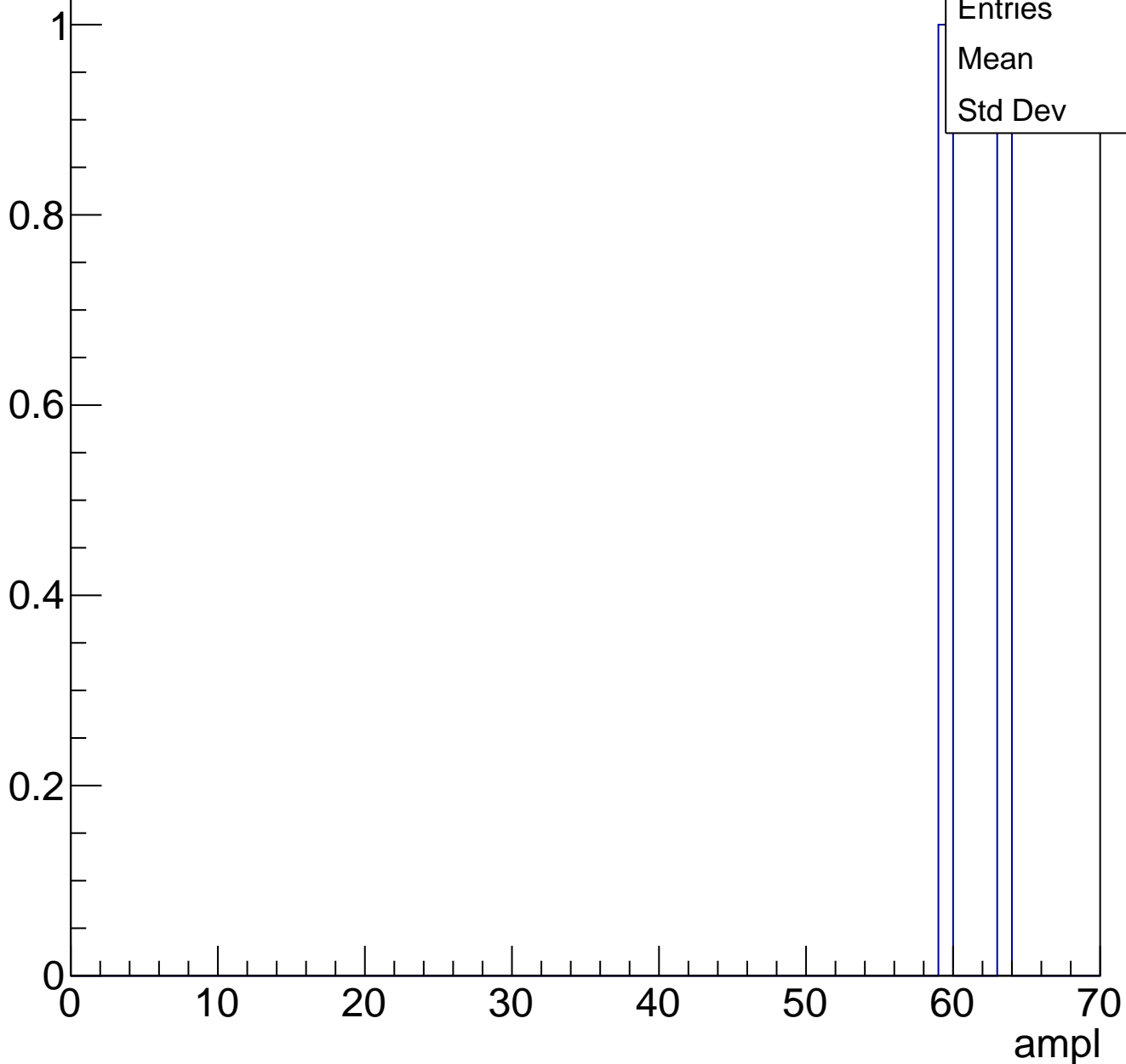
Entries	48
Mean	58.65
Std Dev	8.931



# B1L103S, U11-ch40, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U11-ch40, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L103S, U11-ch41, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	73
Mean	29.32
Std Dev	4.857

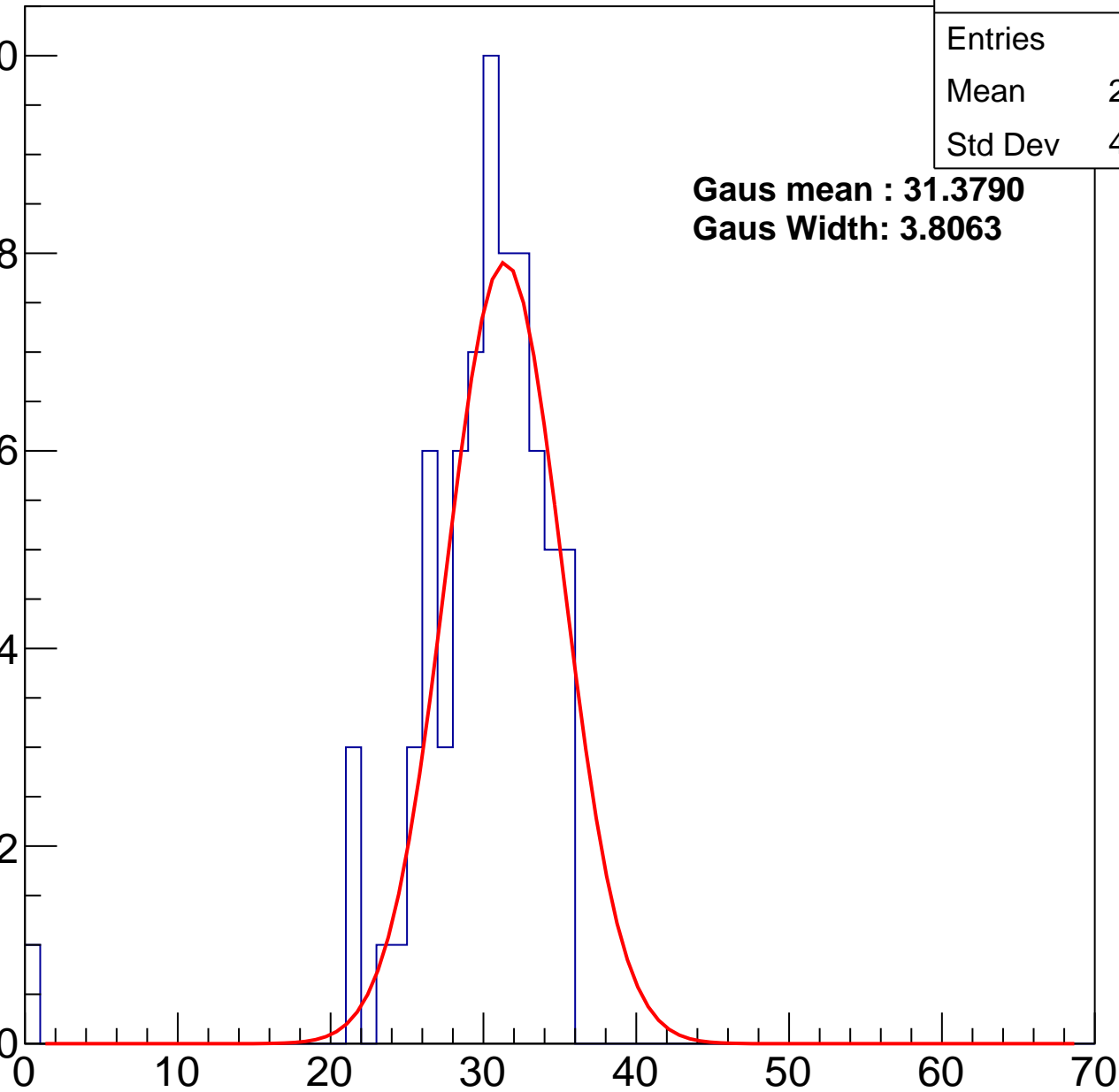
**Gaus mean : 31.3790**

**Gaus Width: 3.8063**

Entry

10  
8  
6  
4  
2  
0

ampl



# B1L103S, U11-ch41, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	68
Mean	37.32
Std Dev	3.187

**Gaus mean : 37.7338**

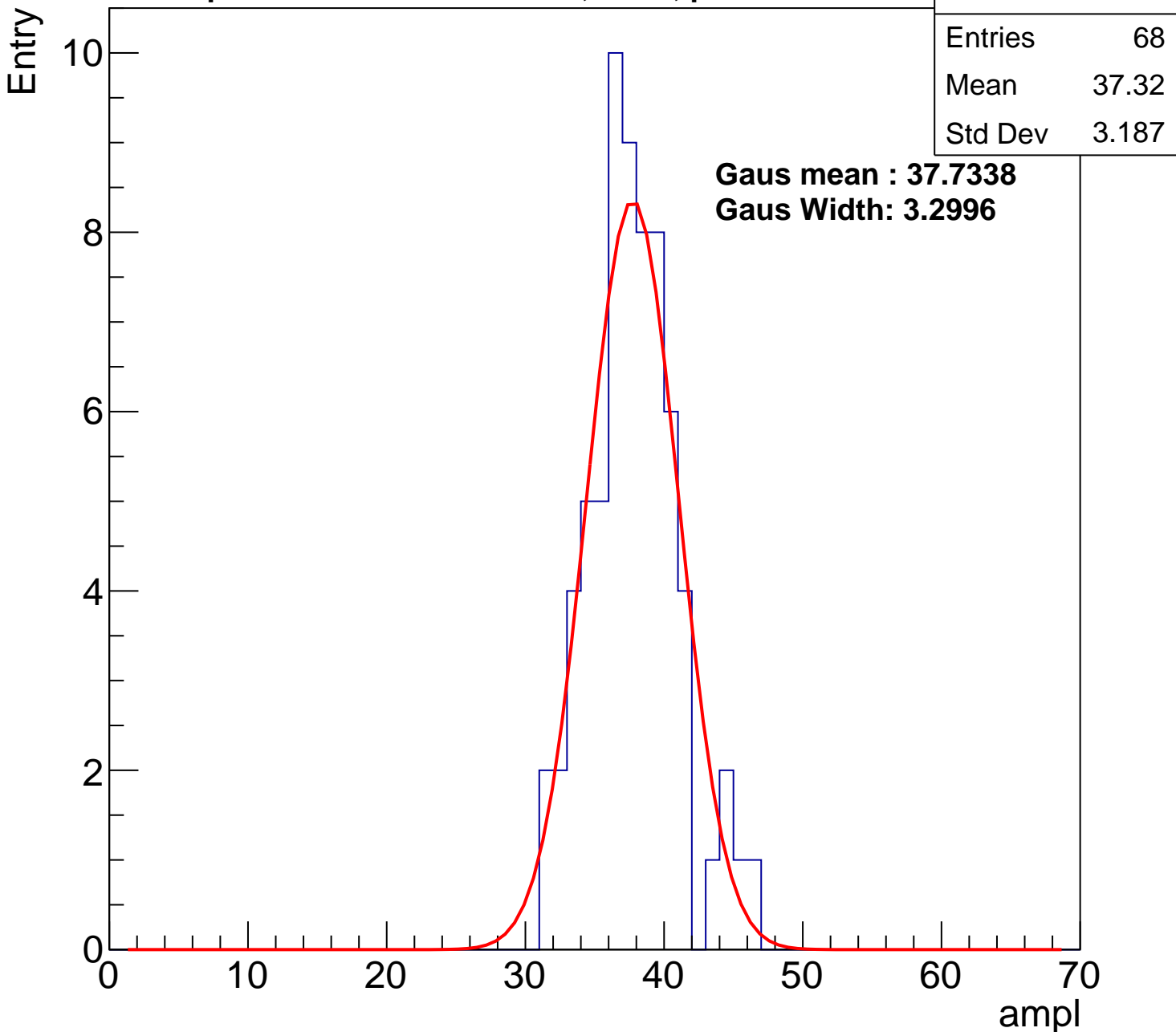
**Gaus Width: 3.2996**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B1L103S, U11-ch41, adc2

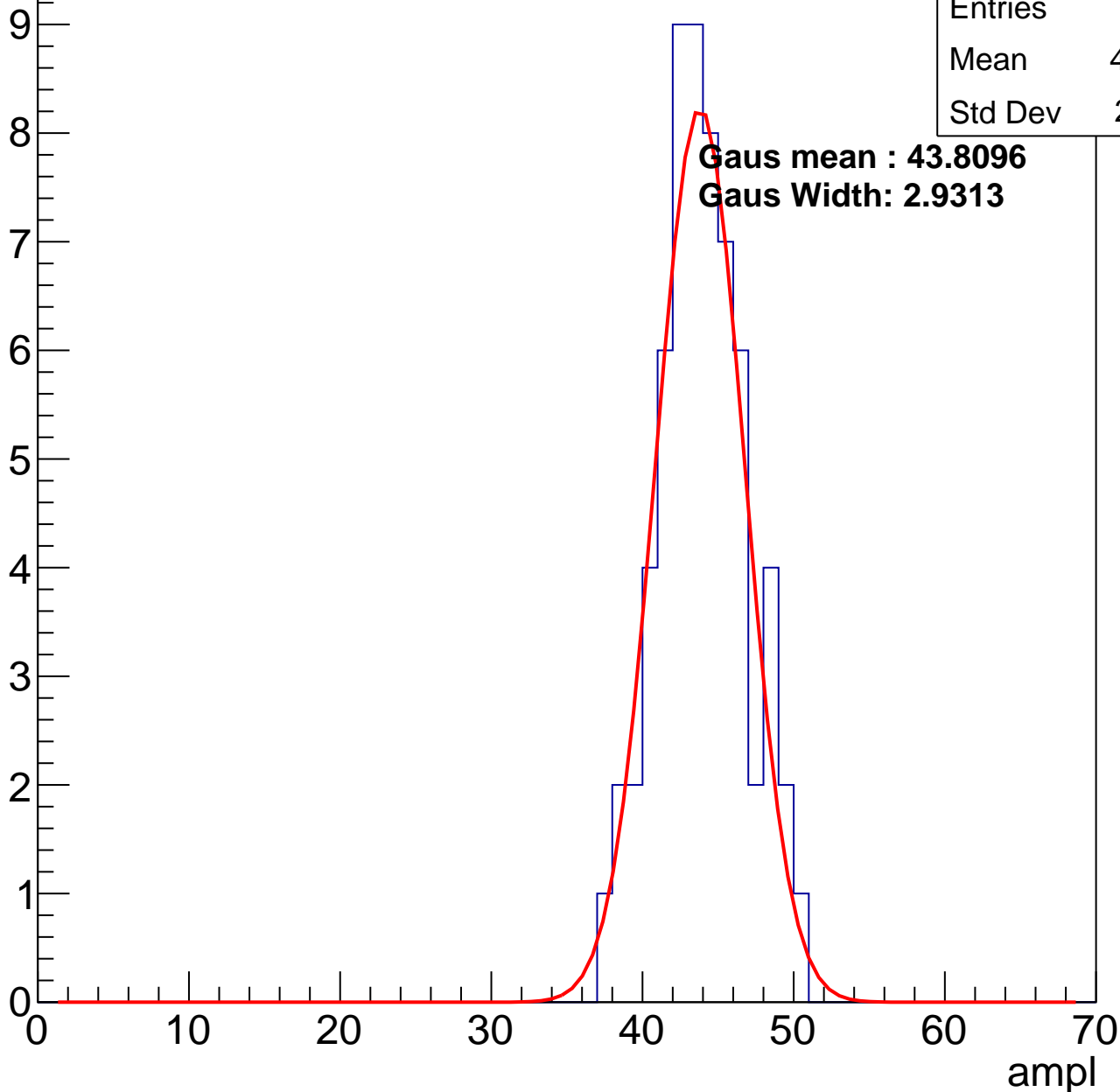
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	43.48
Std Dev	2.861

**Gaus mean : 43.8096**

**Gaus Width: 2.9313**

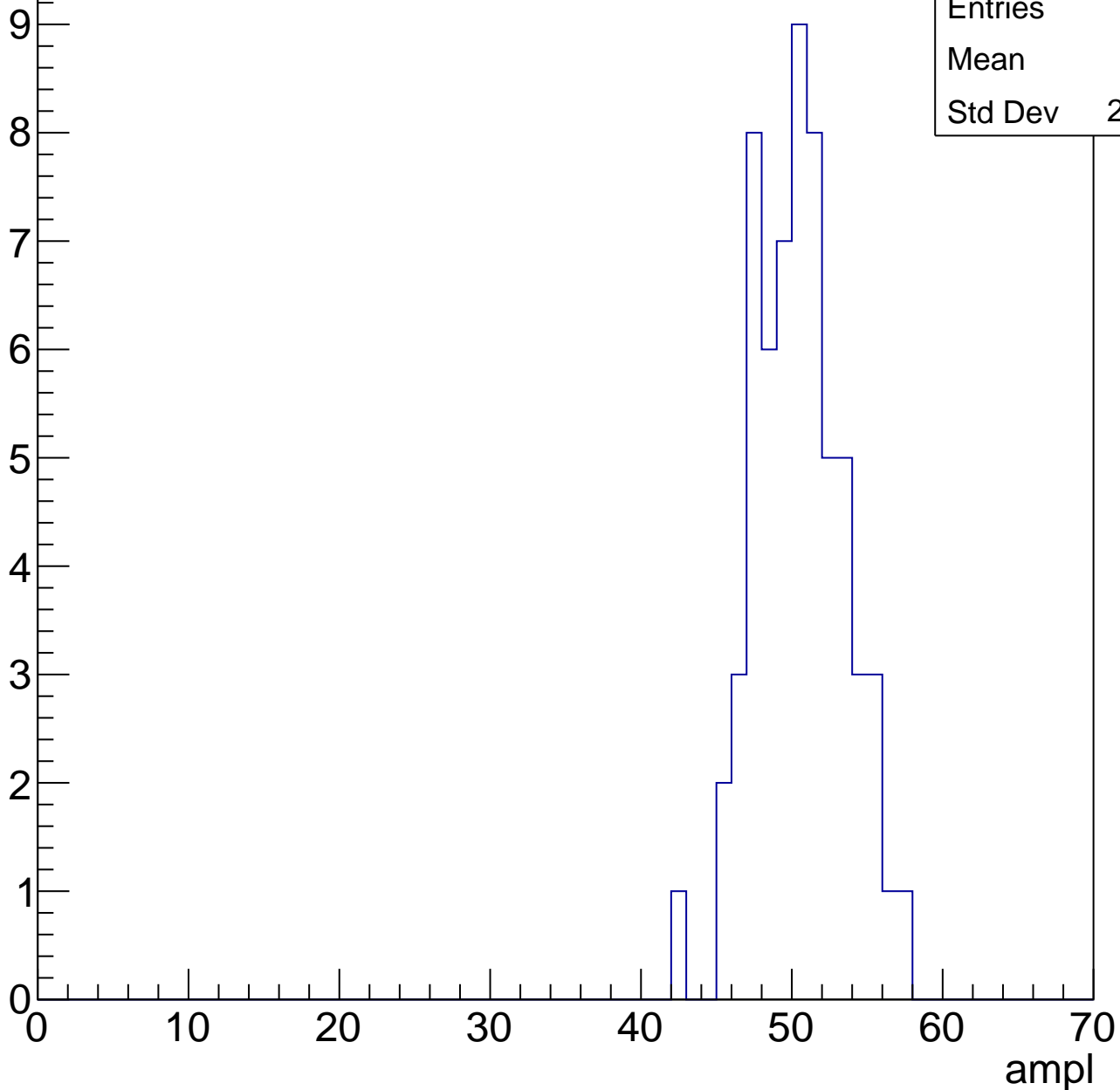


# B1L103S, U11-ch41, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	50
Std Dev	2.968

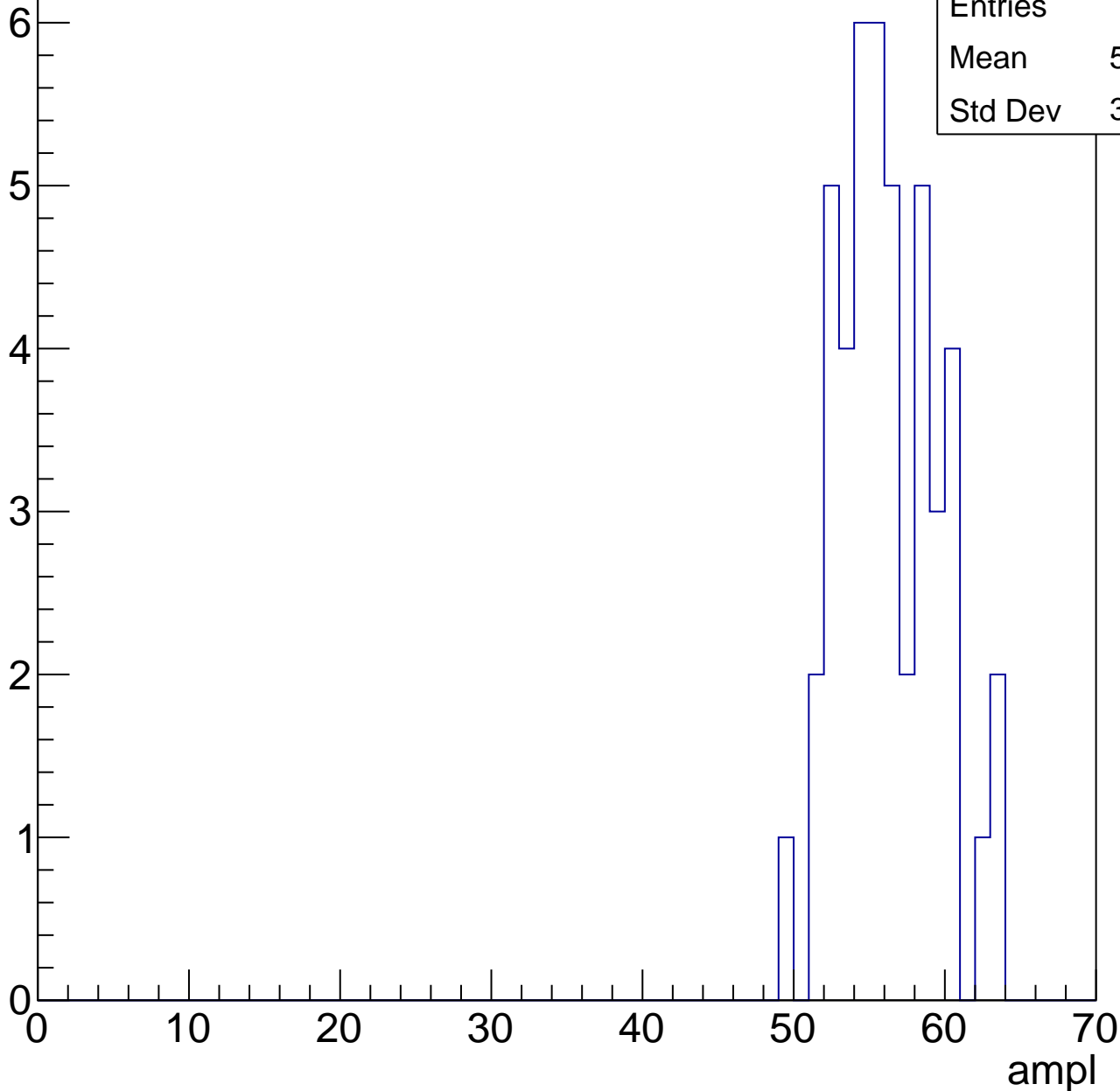


# B1L103S, U11-ch41, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	46
Mean	55.78
Std Dev	3.263

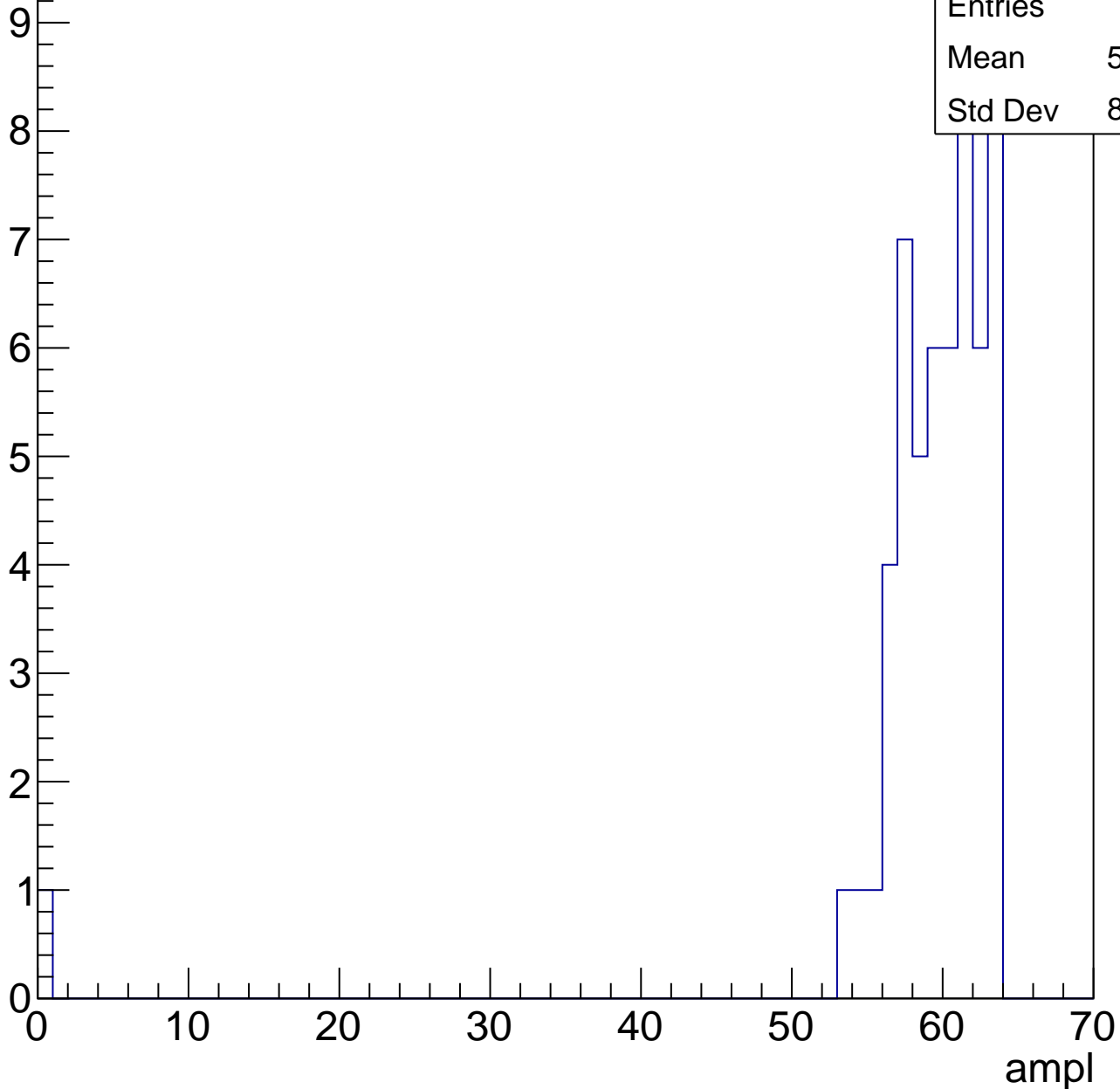


# B1L103S, U11-ch41, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

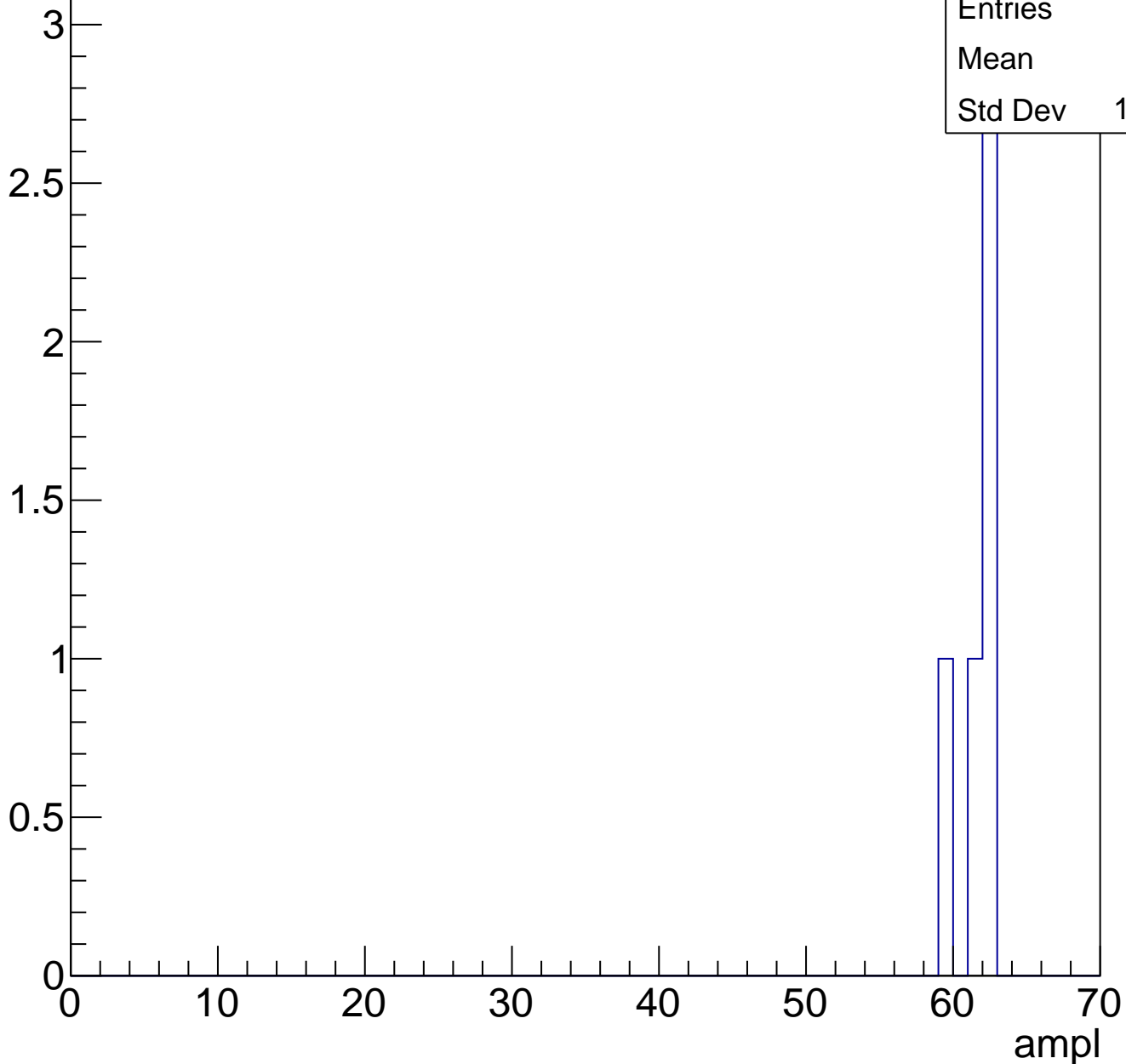
Entries	55
Mean	58.44
Std Dev	8.349



# B1L103S, U11-ch41, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U11-ch41, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L103S, U11-ch42, adc0

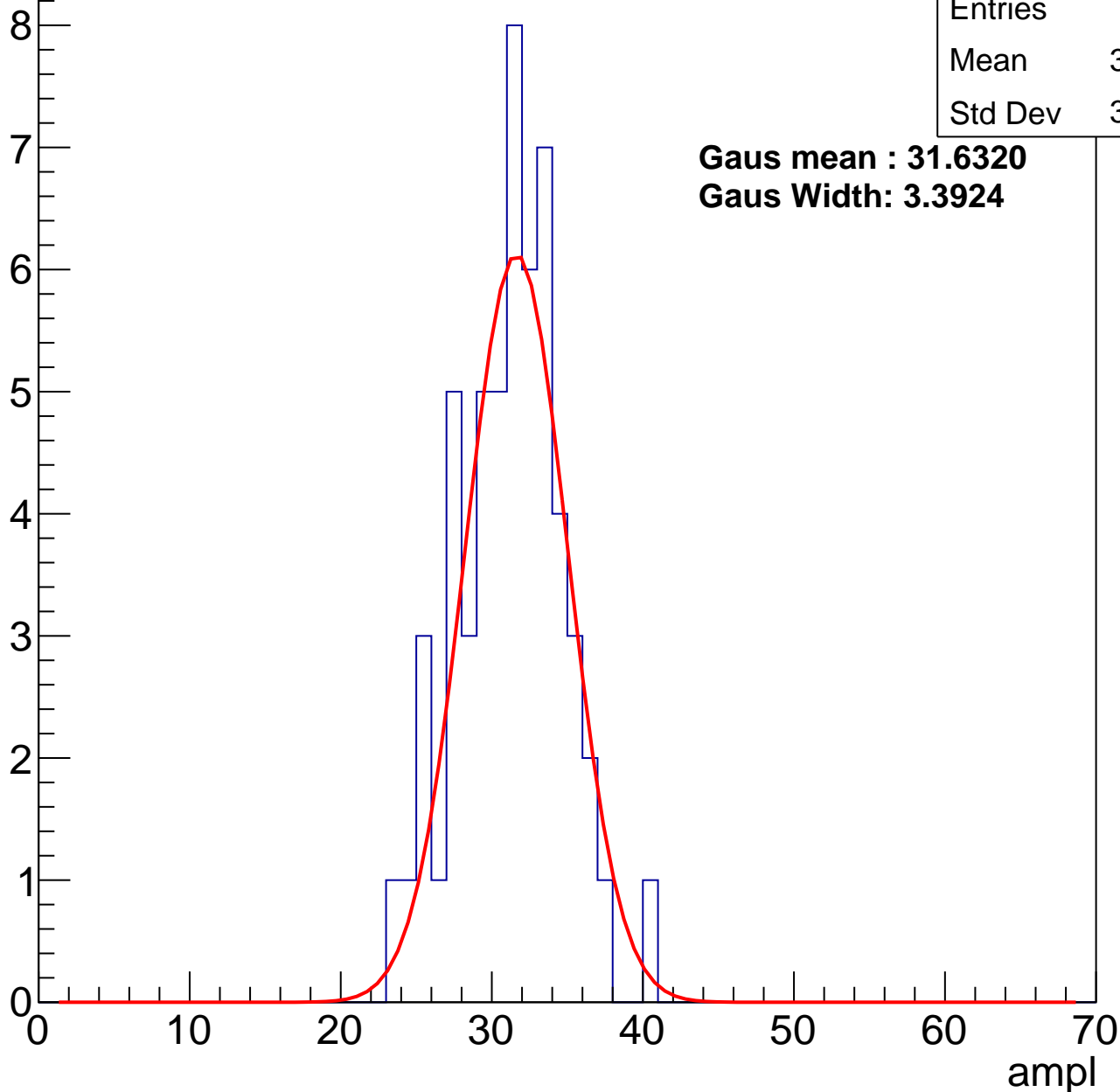
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	56
Mean	30.77
Std Dev	3.433

**Gaus mean : 31.6320**

**Gaus Width: 3.3924**



# B1L103S, U11-ch42, adc1

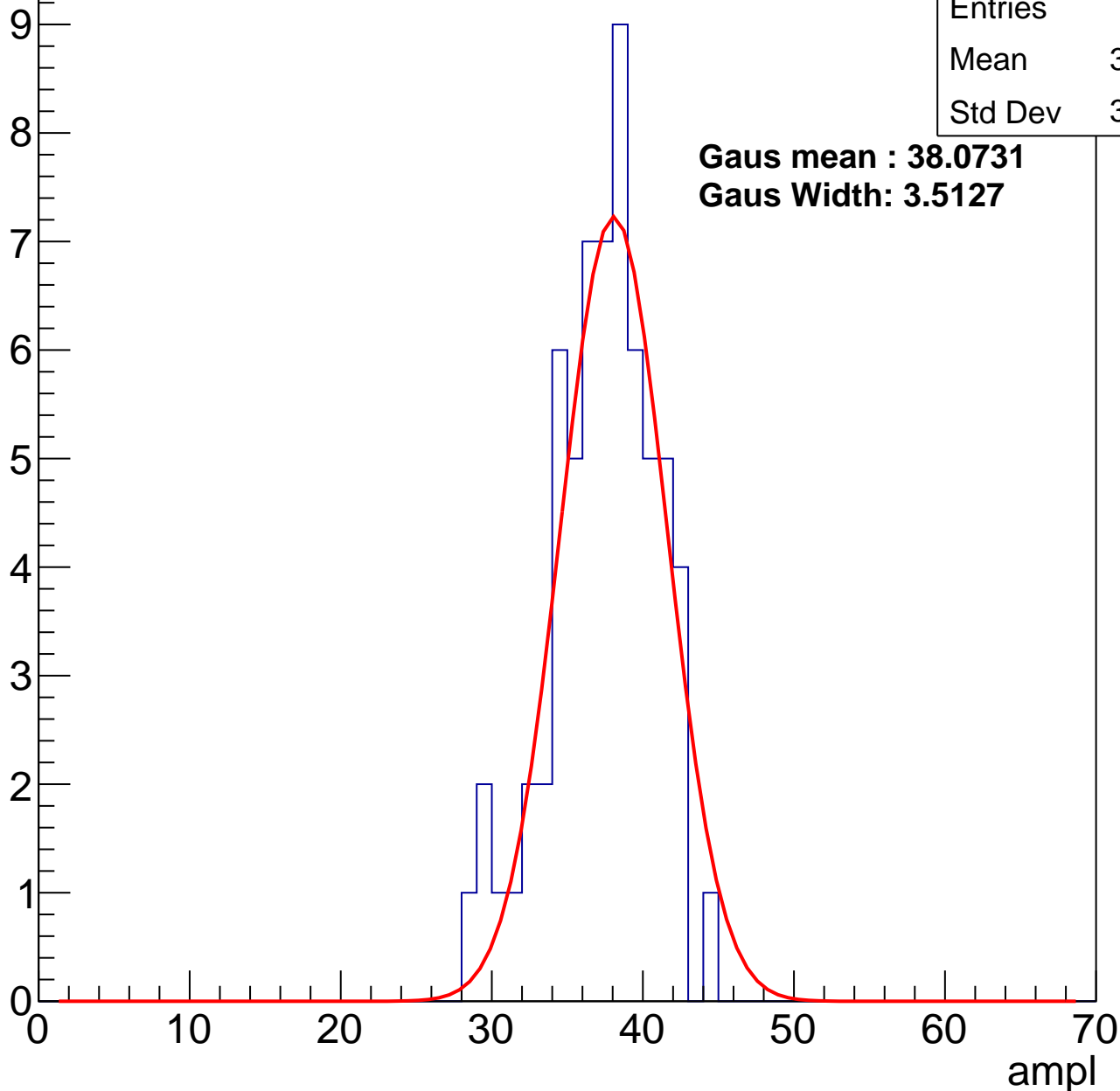
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	36.88
Std Dev	3.453

**Gaus mean : 38.0731**

**Gaus Width: 3.5127**



# B1L103S, U11-ch42, adc2

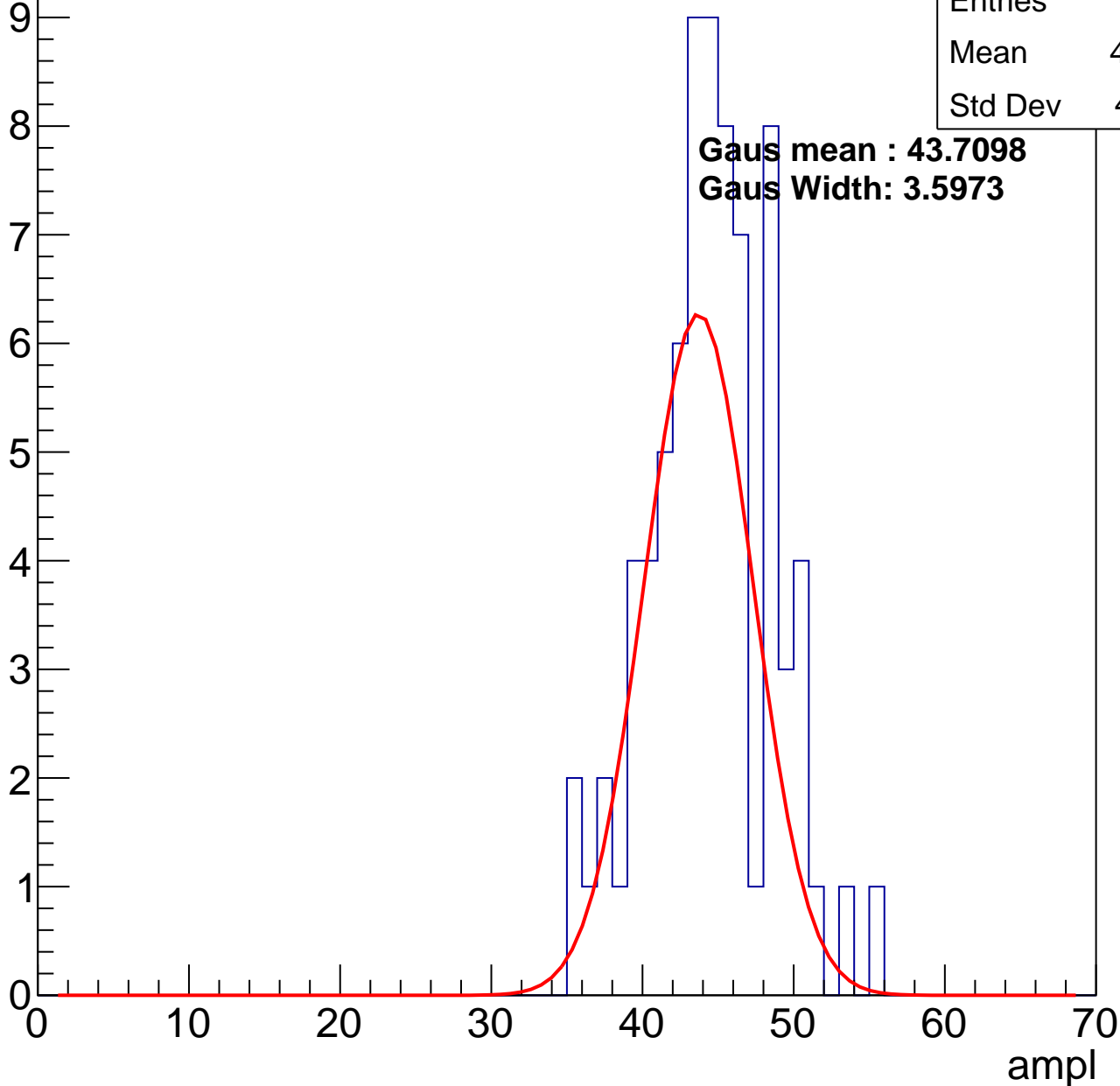
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	77
Mean	44.06
Std Dev	4.021

**Gaus mean : 43.7098**

**Gaus Width: 3.5973**

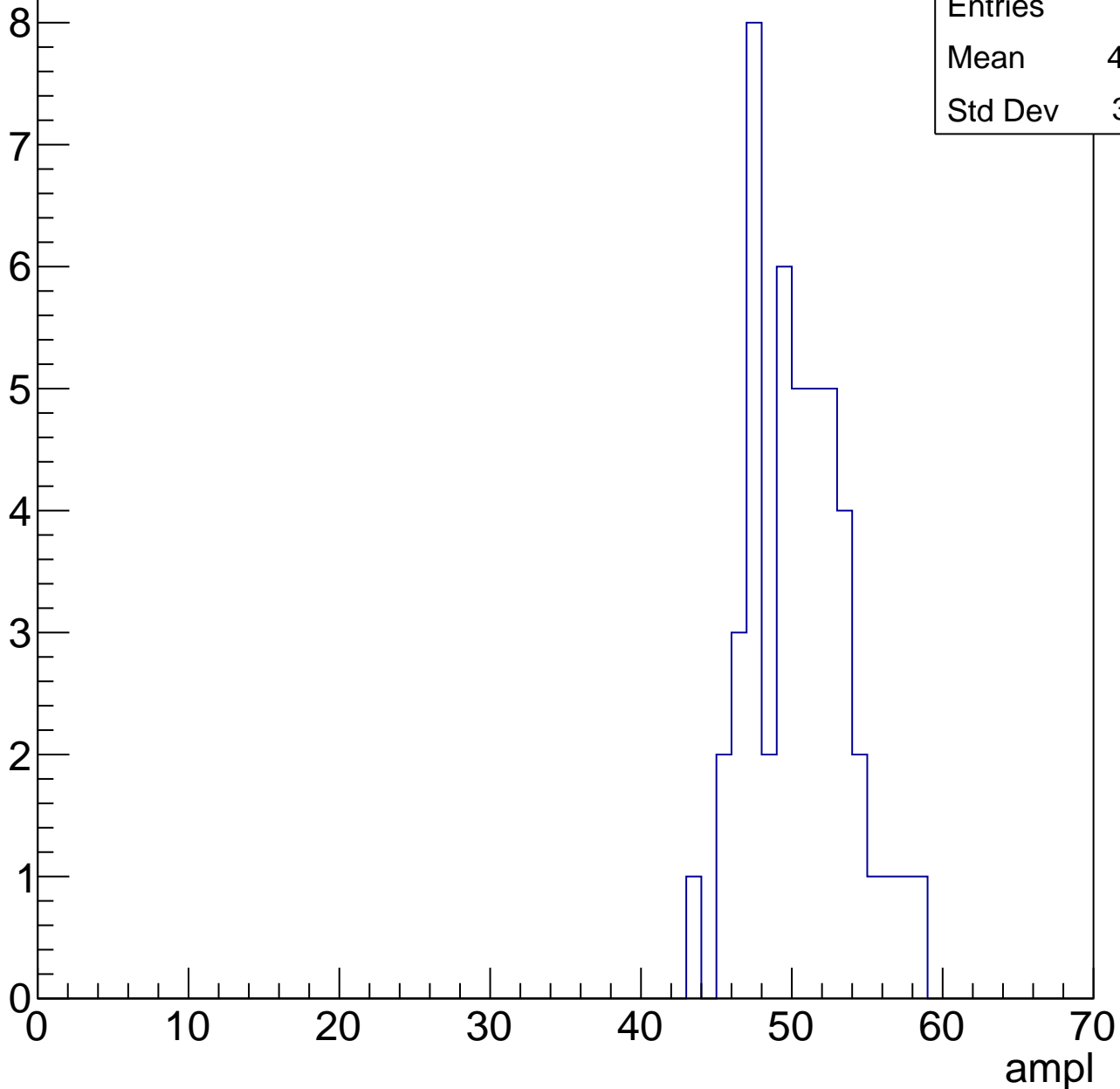


# B1L103S, U11-ch42, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	47
Mean	49.96
Std Dev	3.261

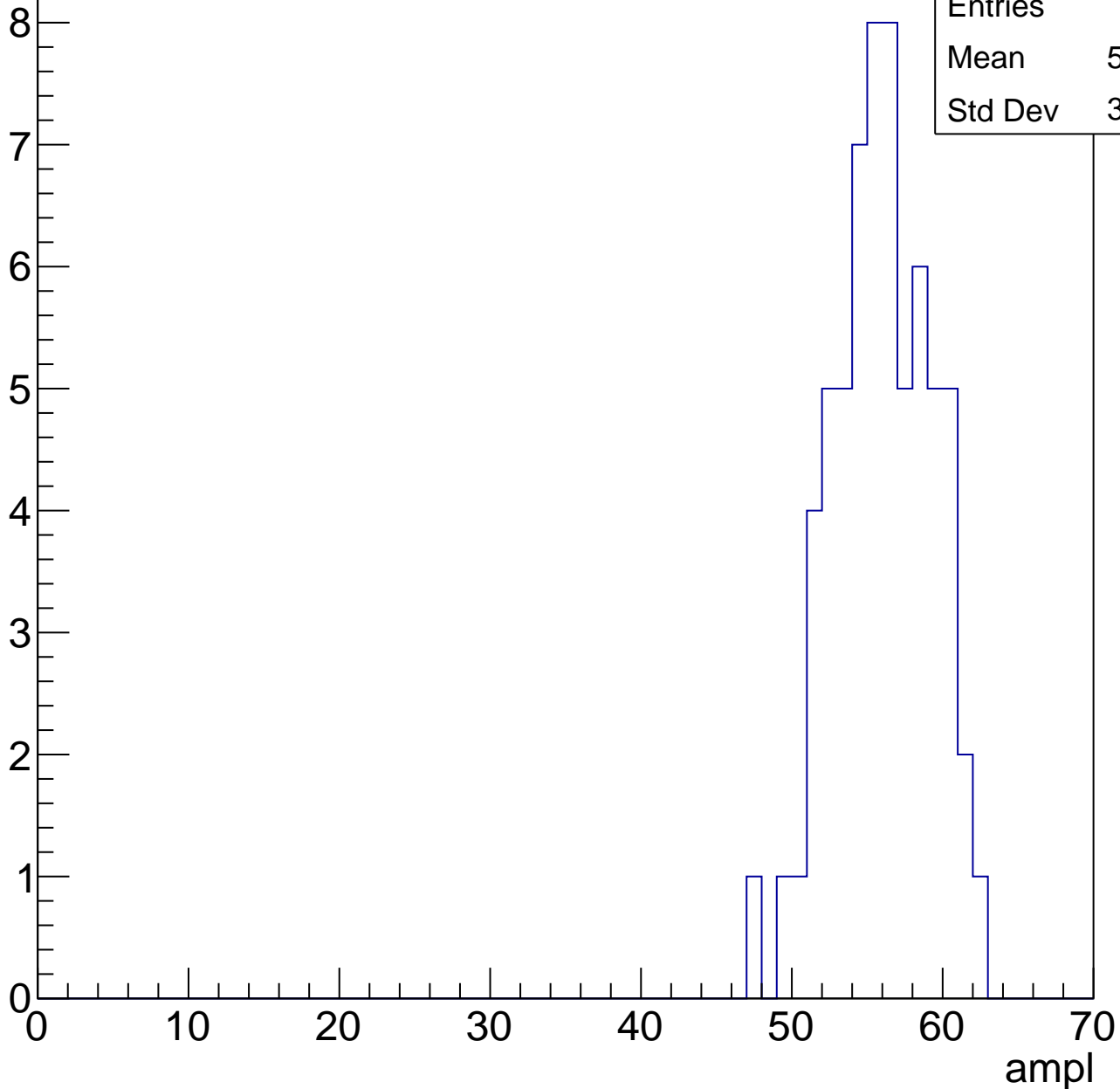


# B1L103S, U11-ch42, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	55.52
Std Dev	3.192

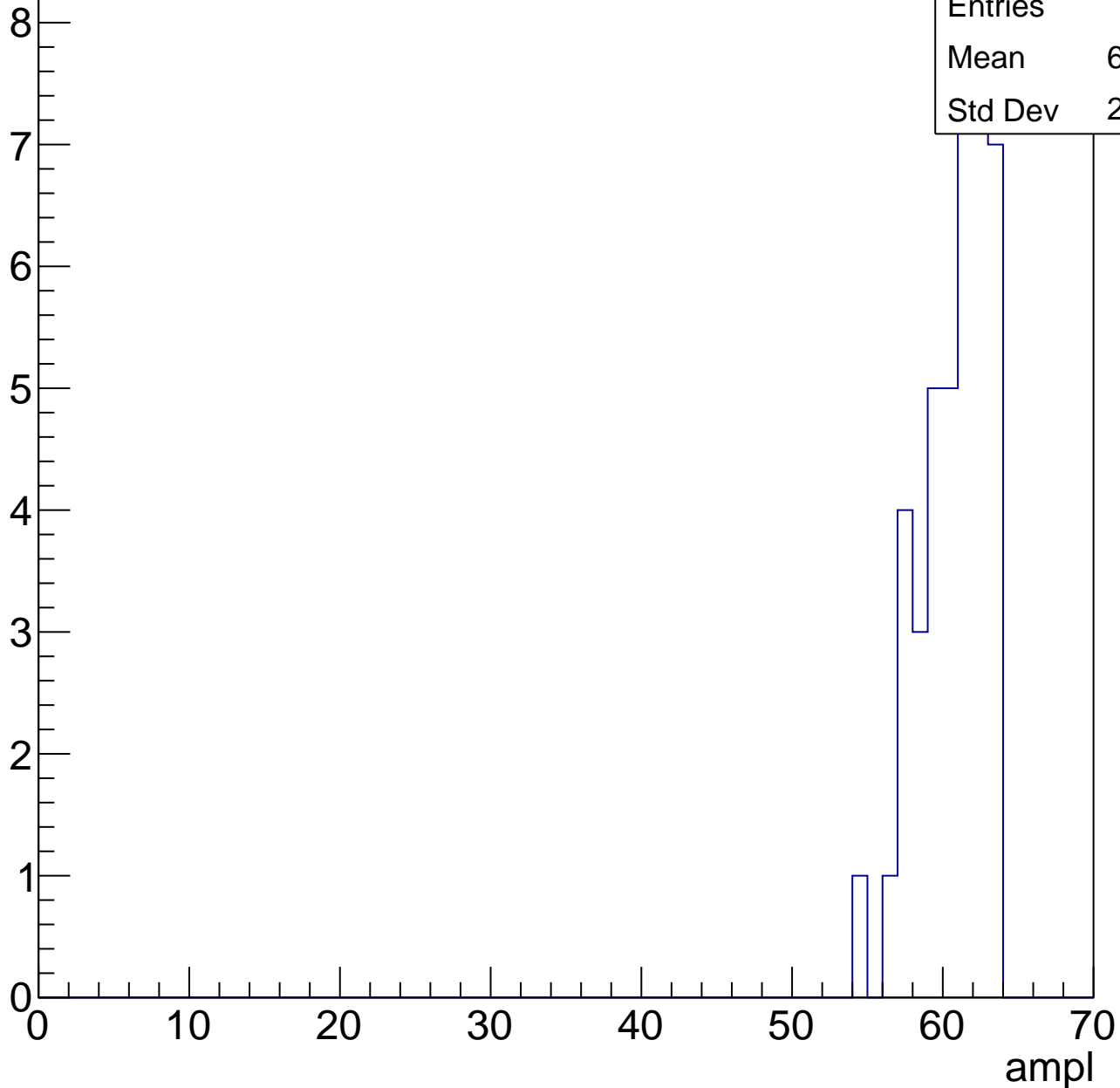


# B1L103S, U11-ch42, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	42
Mean	60.29
Std Dev	2.207



# B1L103S, U11-ch42, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U11-ch42, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U11-ch43, adc0

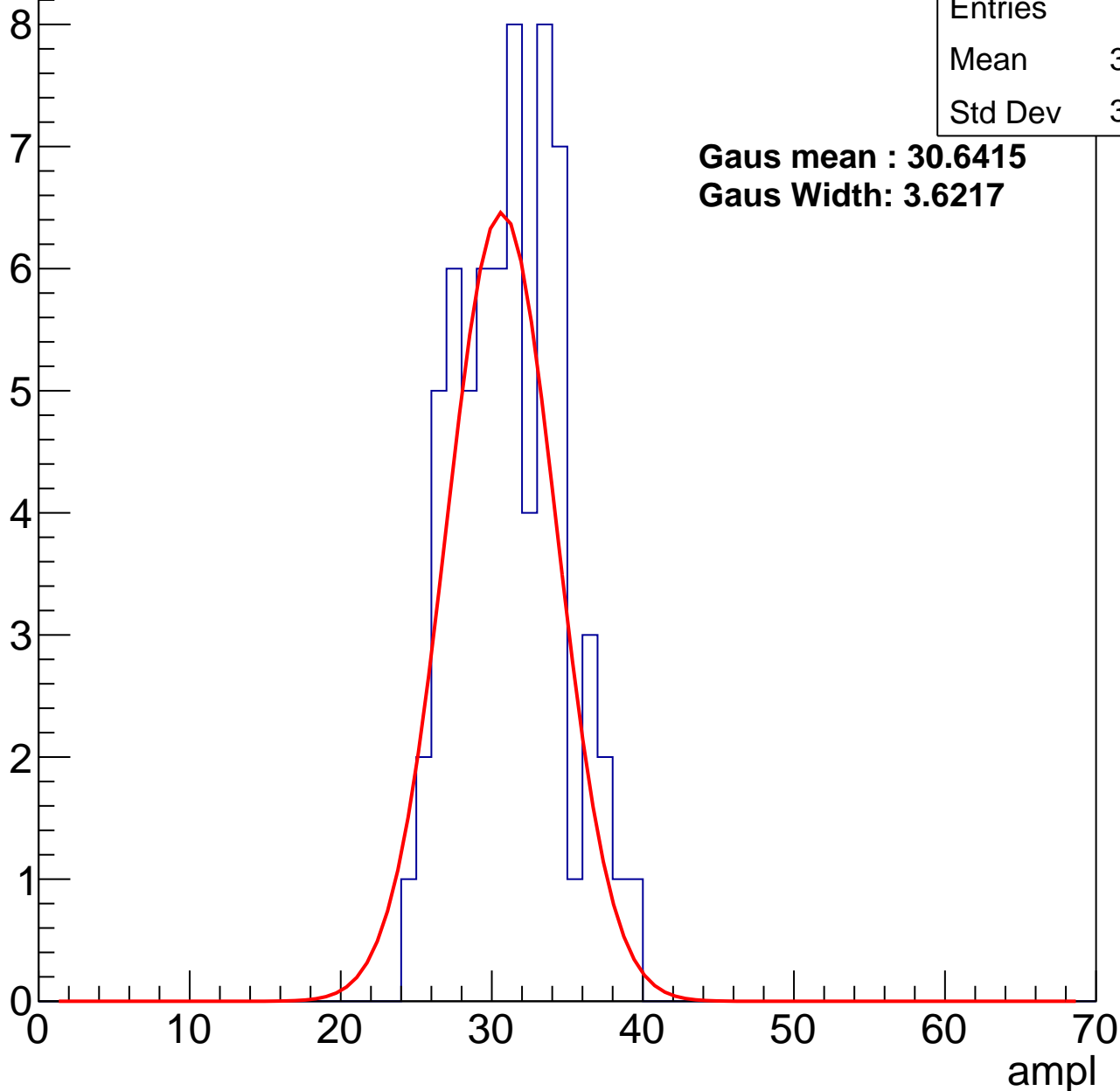
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	30.79
Std Dev	3.458

**Gaus mean : 30.6415**

**Gaus Width: 3.6217**



# B1L103S, U11-ch43, adc1

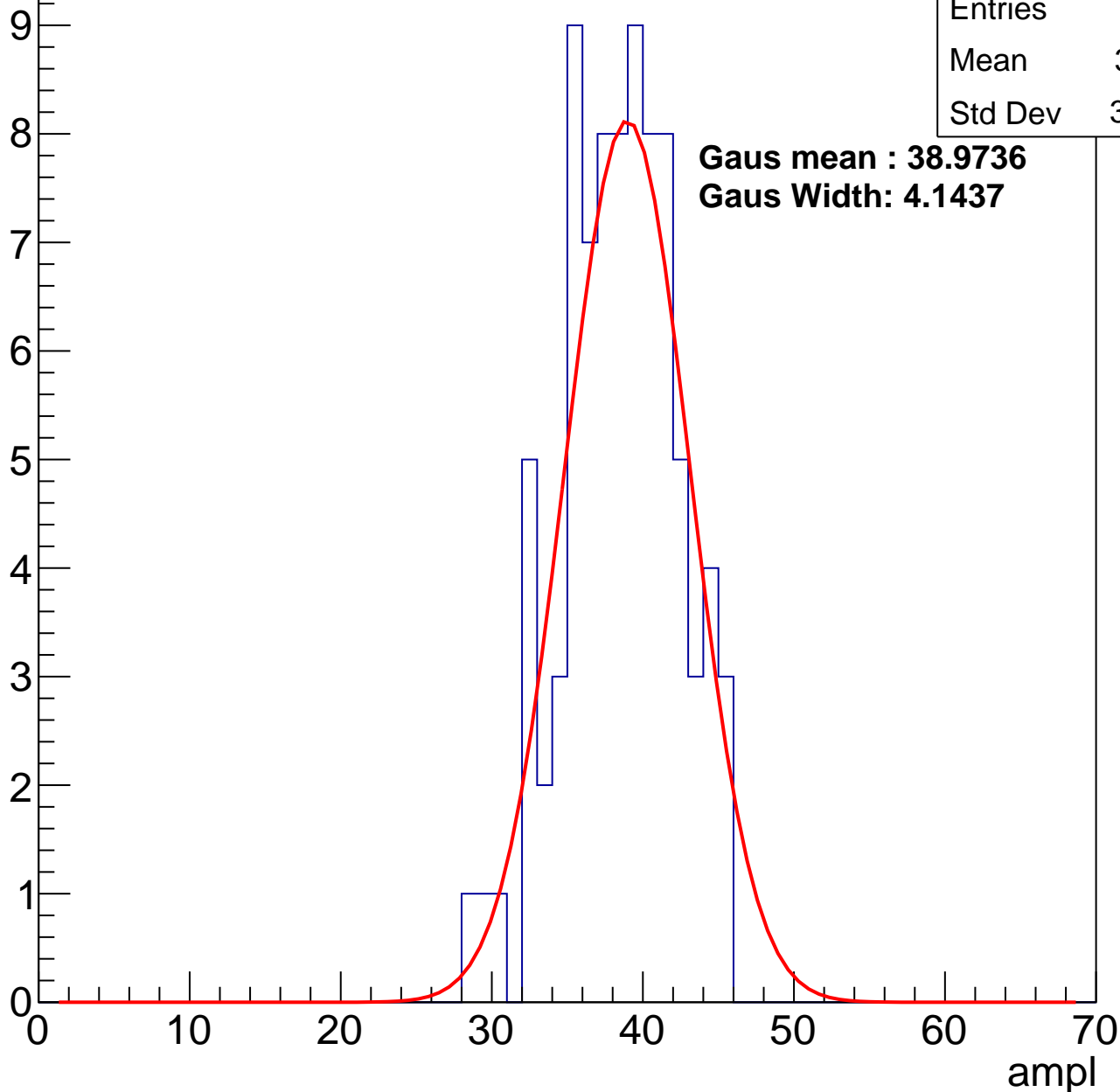
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	85
Mean	38.01
Std Dev	3.756

**Gaus mean : 38.9736**

**Gaus Width: 4.1437**



# B1L103S, U11-ch43, adc2

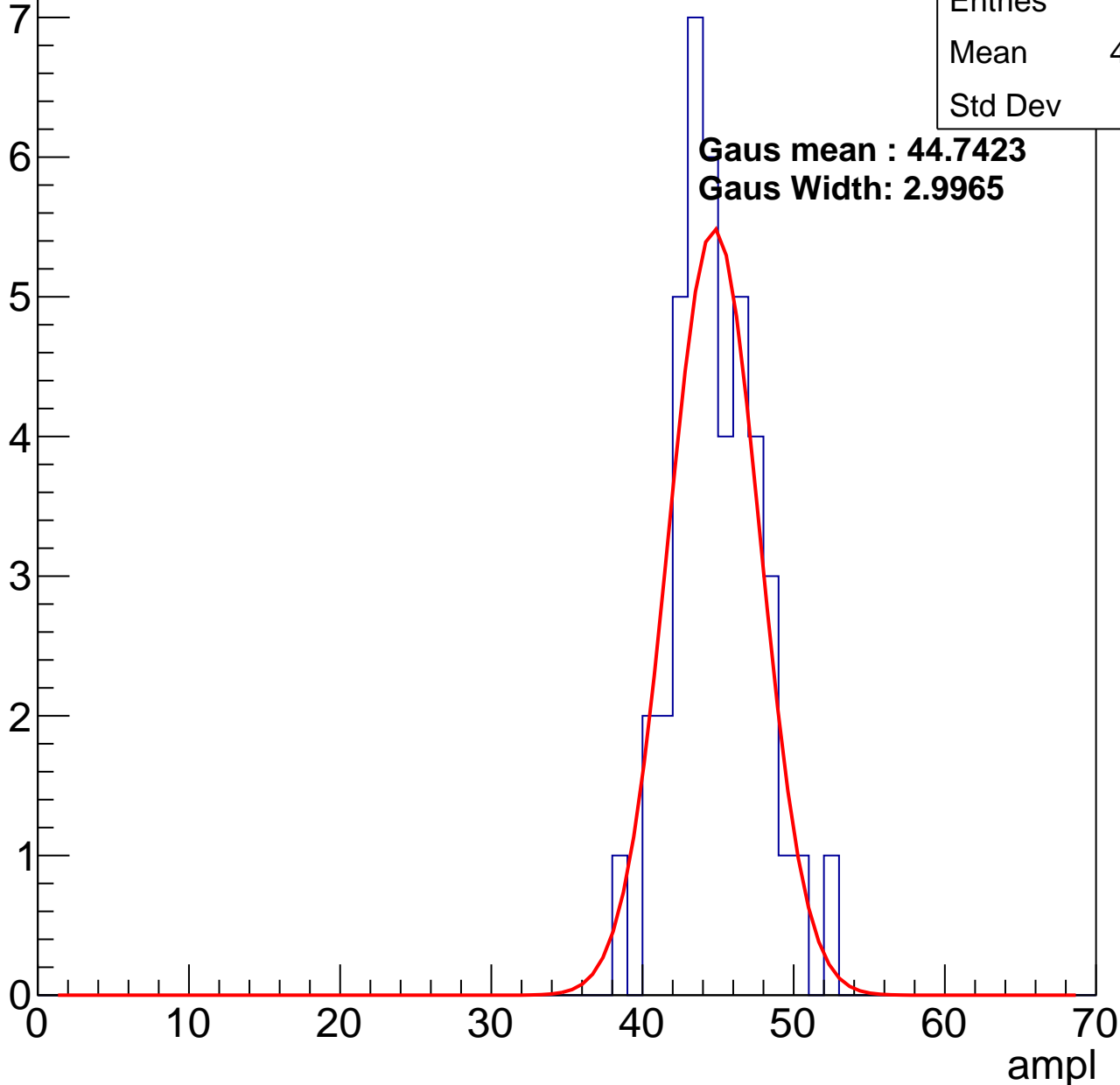
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	42
Mean	44.48
Std Dev	2.83

**Gaus mean : 44.7423**

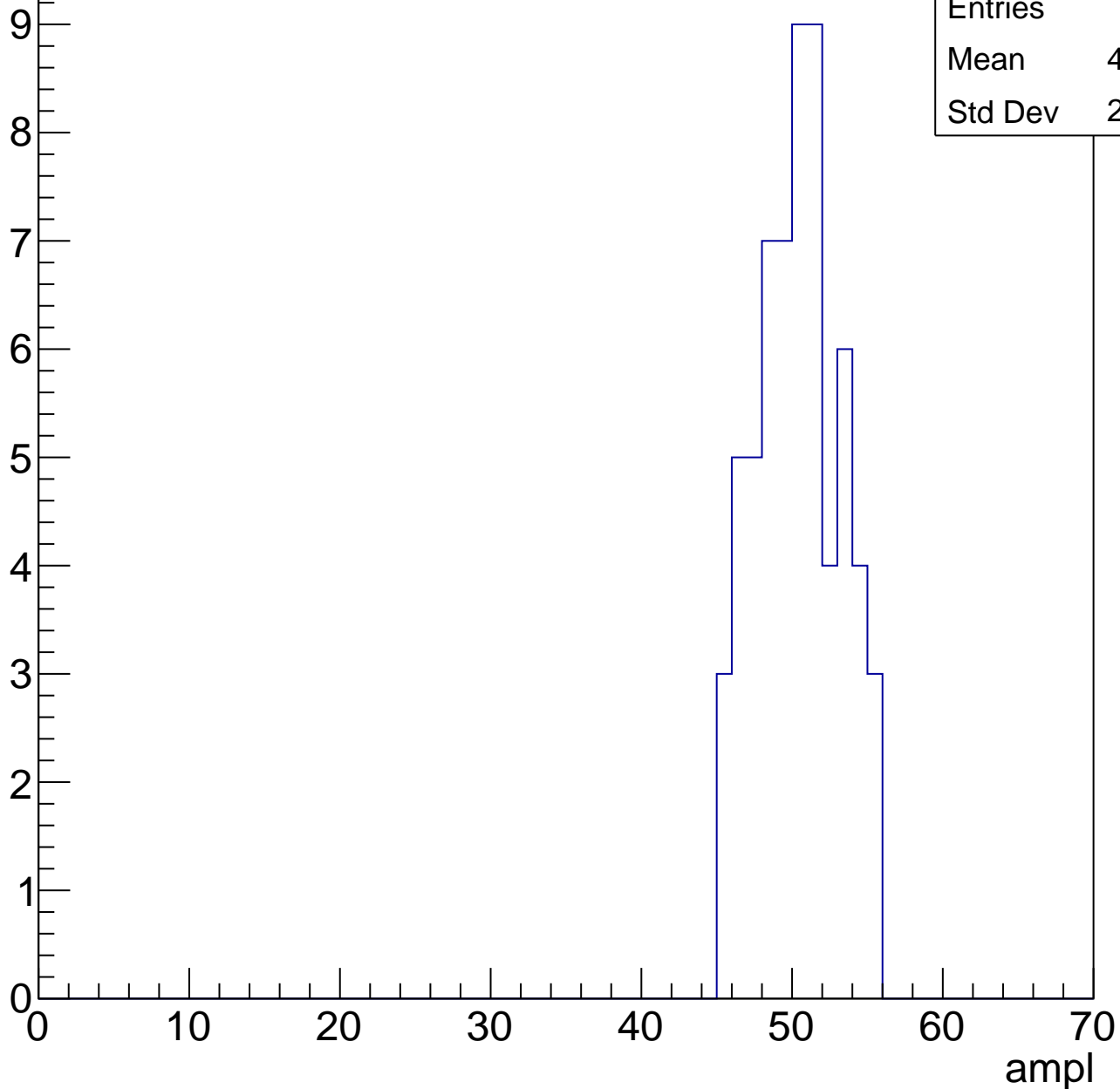
**Gaus Width: 2.9965**



# B1L103S, U11-ch43, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

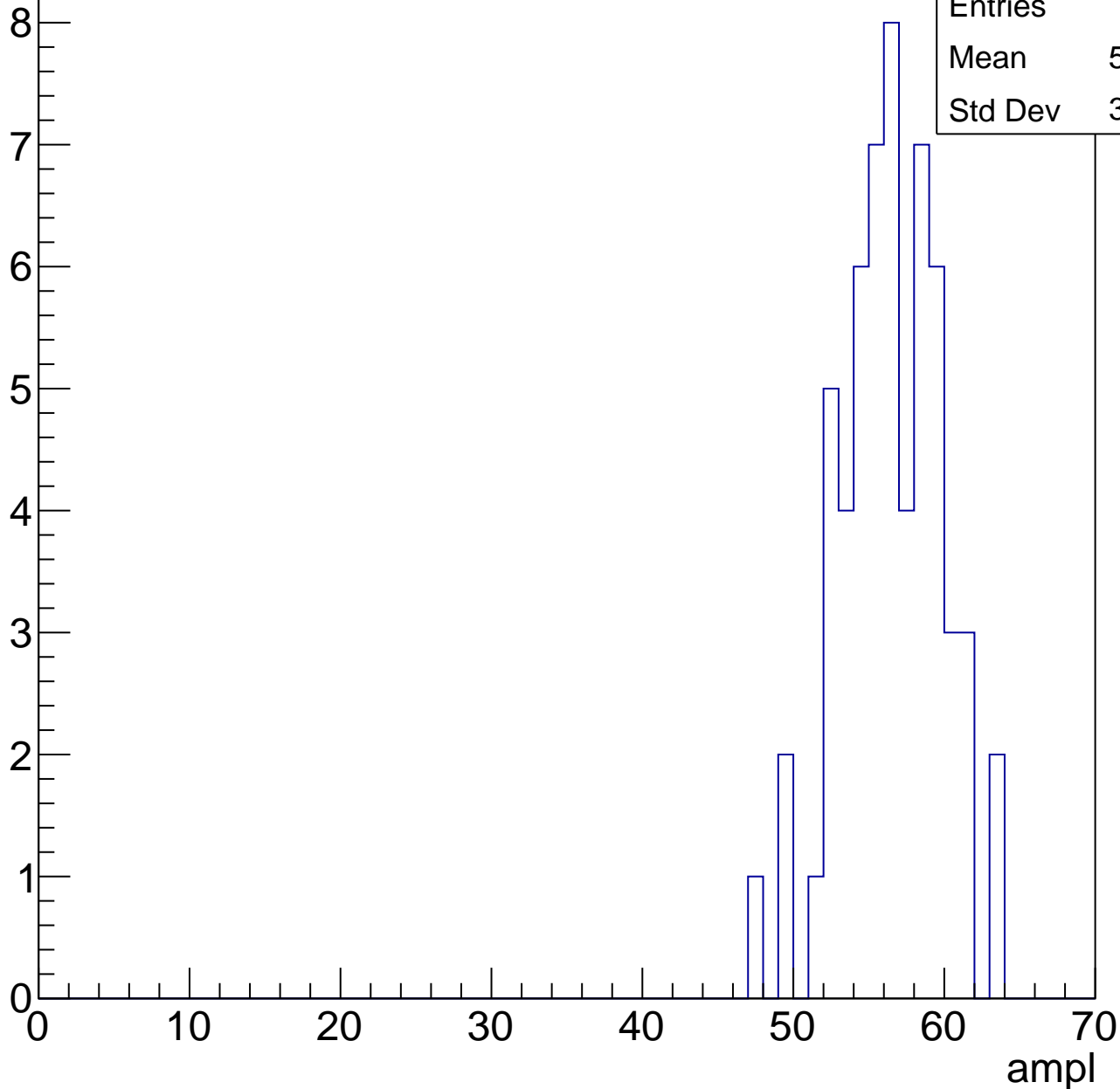


# B1L103S, U11-ch43, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	59
Mean	55.97
Std Dev	3.339

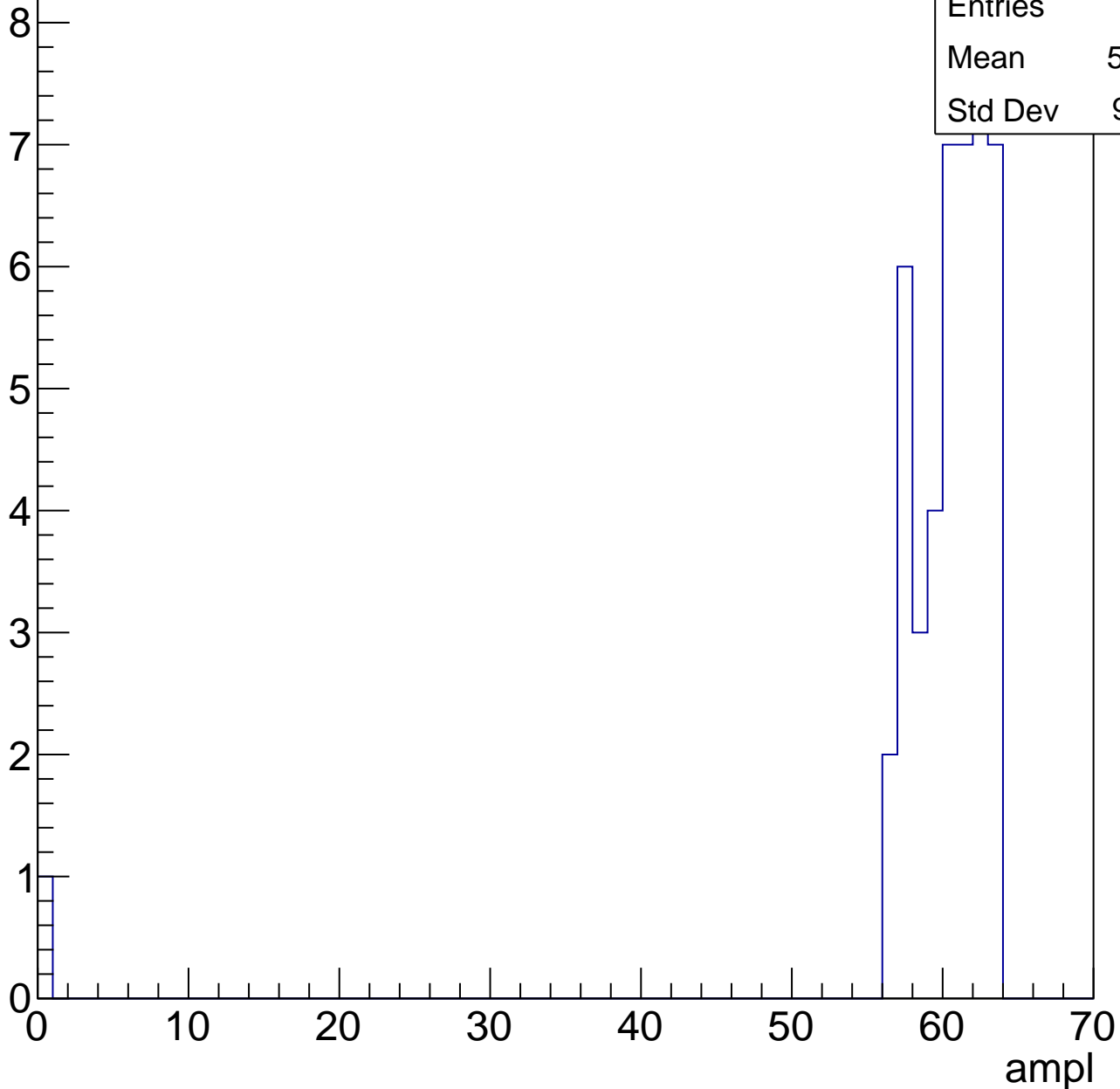


# B1L103S, U11-ch43, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	45
Mean	58.84
Std Dev	9.121



# B1L103S, U11-ch43, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	3
Mean	62.33
Std Dev	0.4714

ampl





# B1L103S, U11-ch43, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



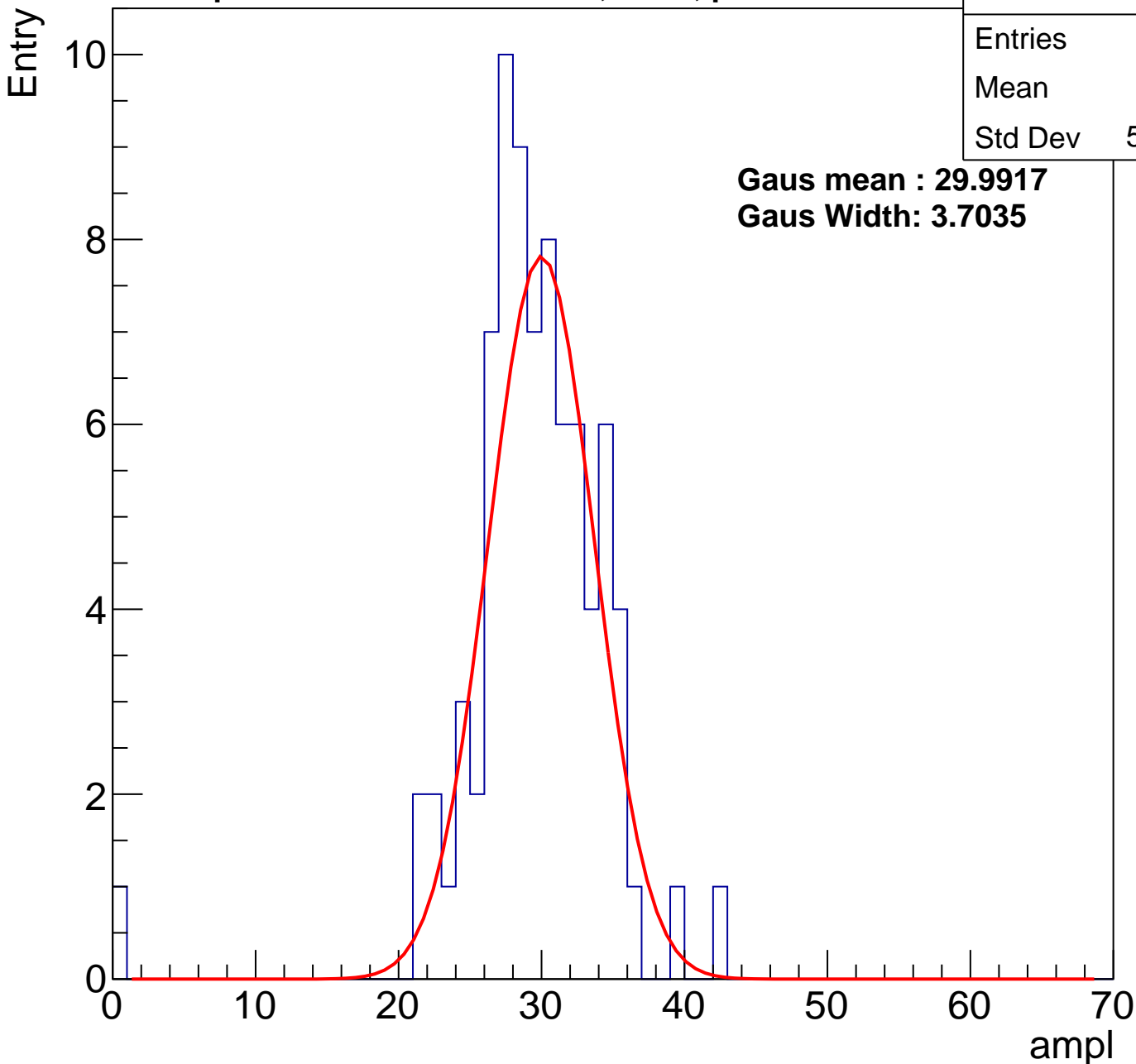
Entries	1
Mean	0
Std Dev	0

# B1L103S, U11-ch44, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	81
Mean	29
Std Dev	5.072

**Gaus mean : 29.9917**  
**Gaus Width: 3.7035**



# B1L103S, U11-ch44, adc1

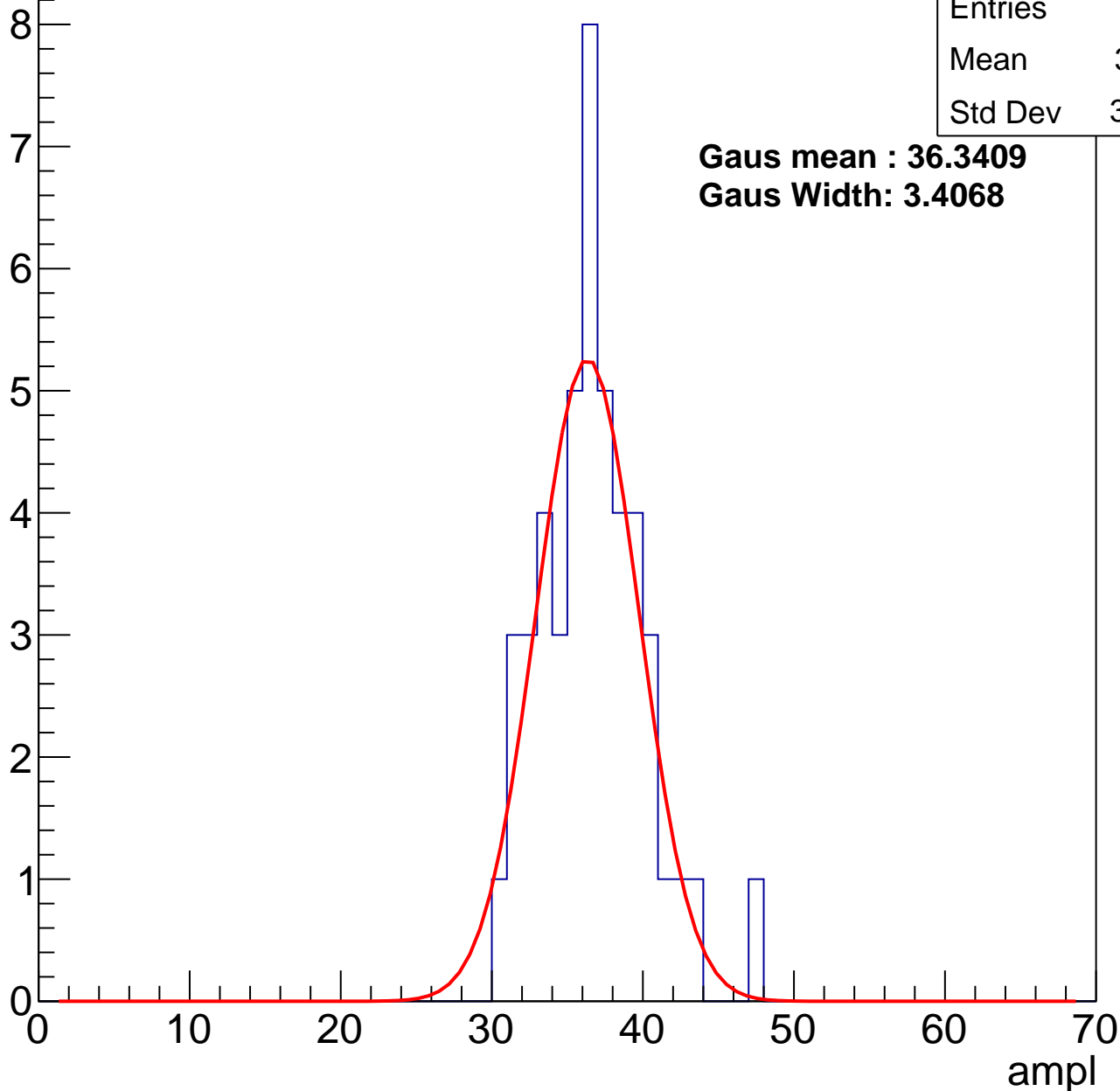
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	47
Mean	36.21
Std Dev	3.408

**Gaus mean : 36.3409**

**Gaus Width: 3.4068**



# B1L103S, U11-ch44, adc2

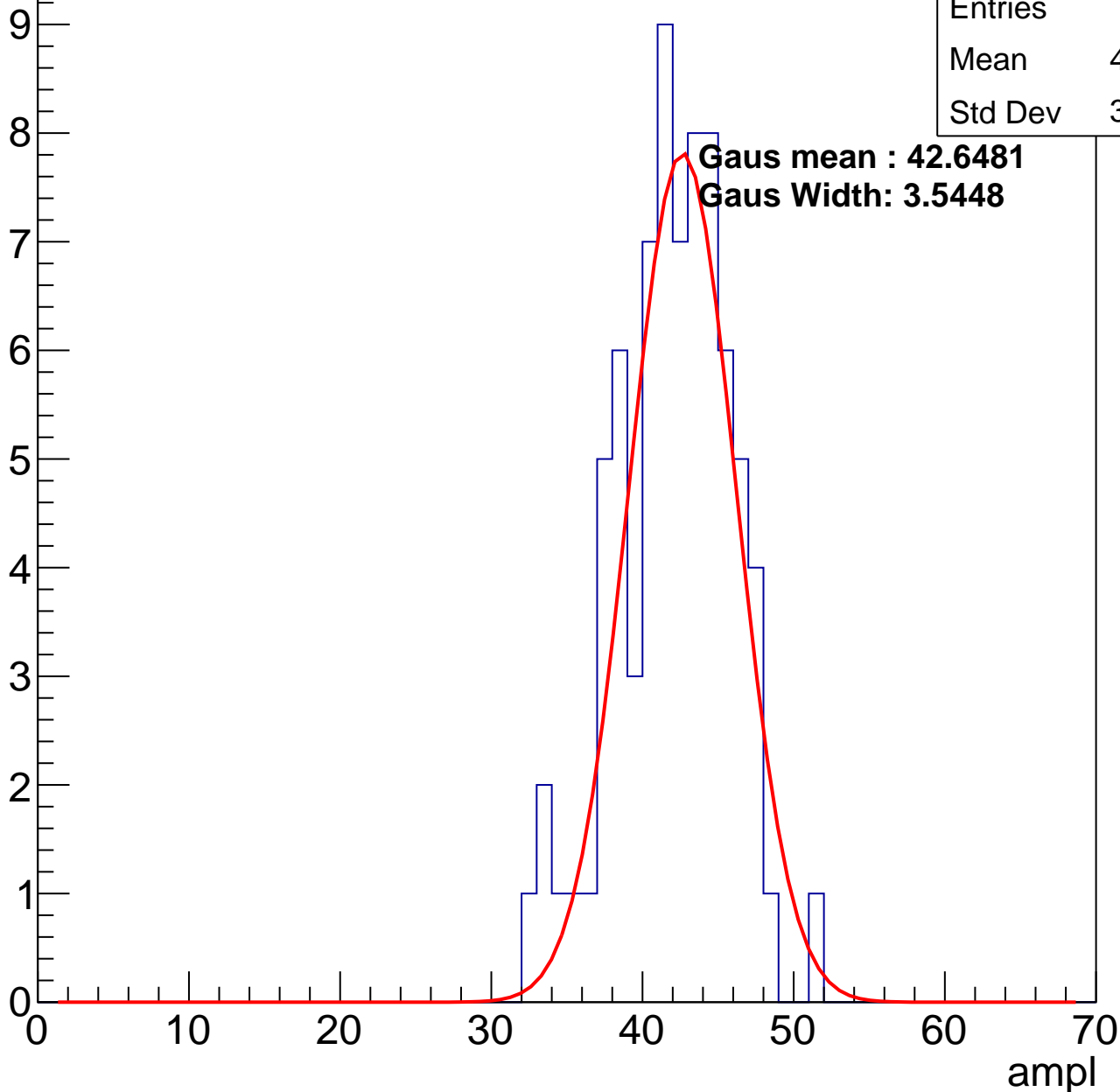
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	76
Mean	41.57
Std Dev	3.757

**Gaus mean : 42.6481**

**Gaus Width: 3.5448**

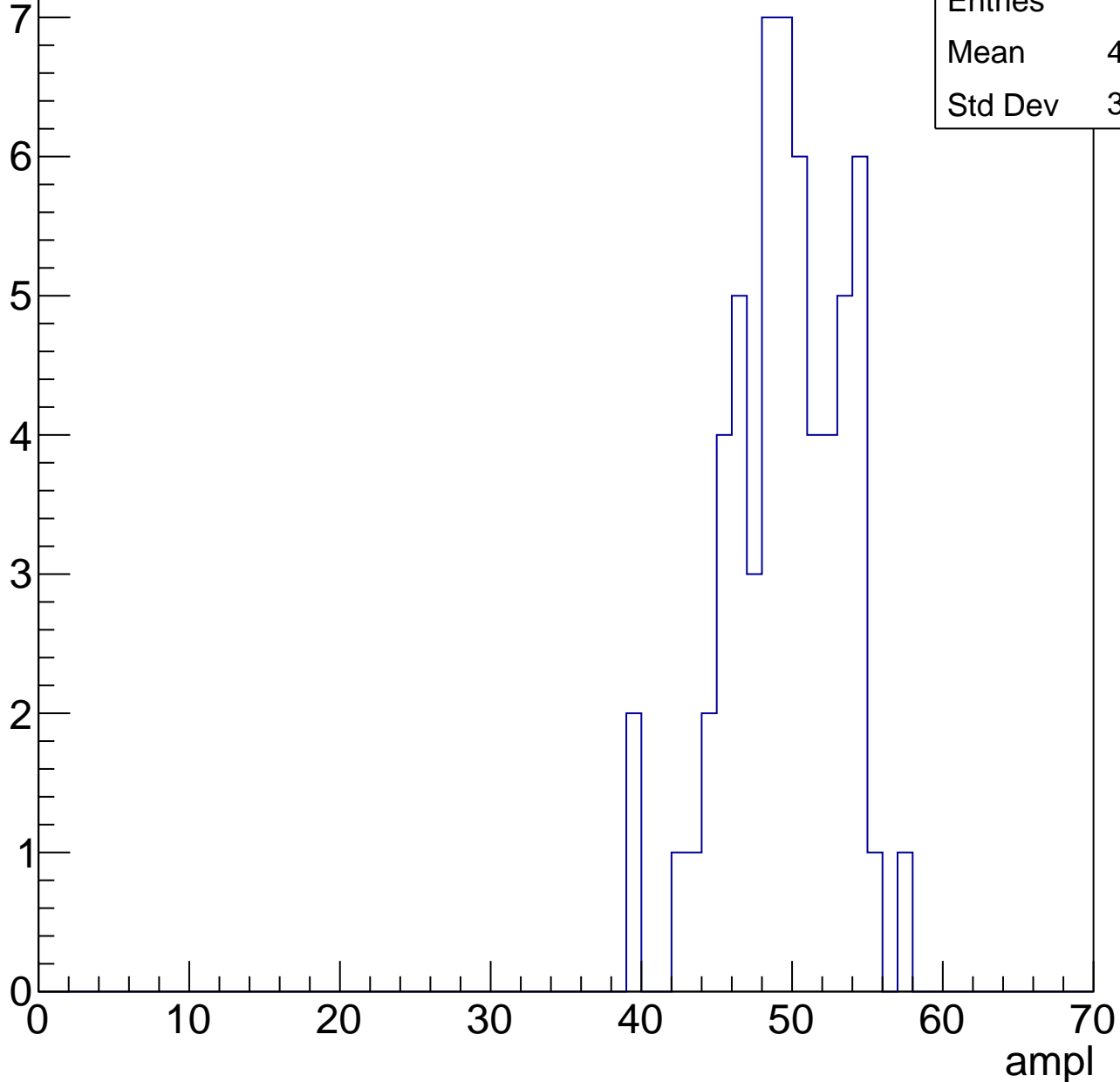


# B1L103S, U11-ch44, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	59
Mean	49.05
Std Dev	3.798

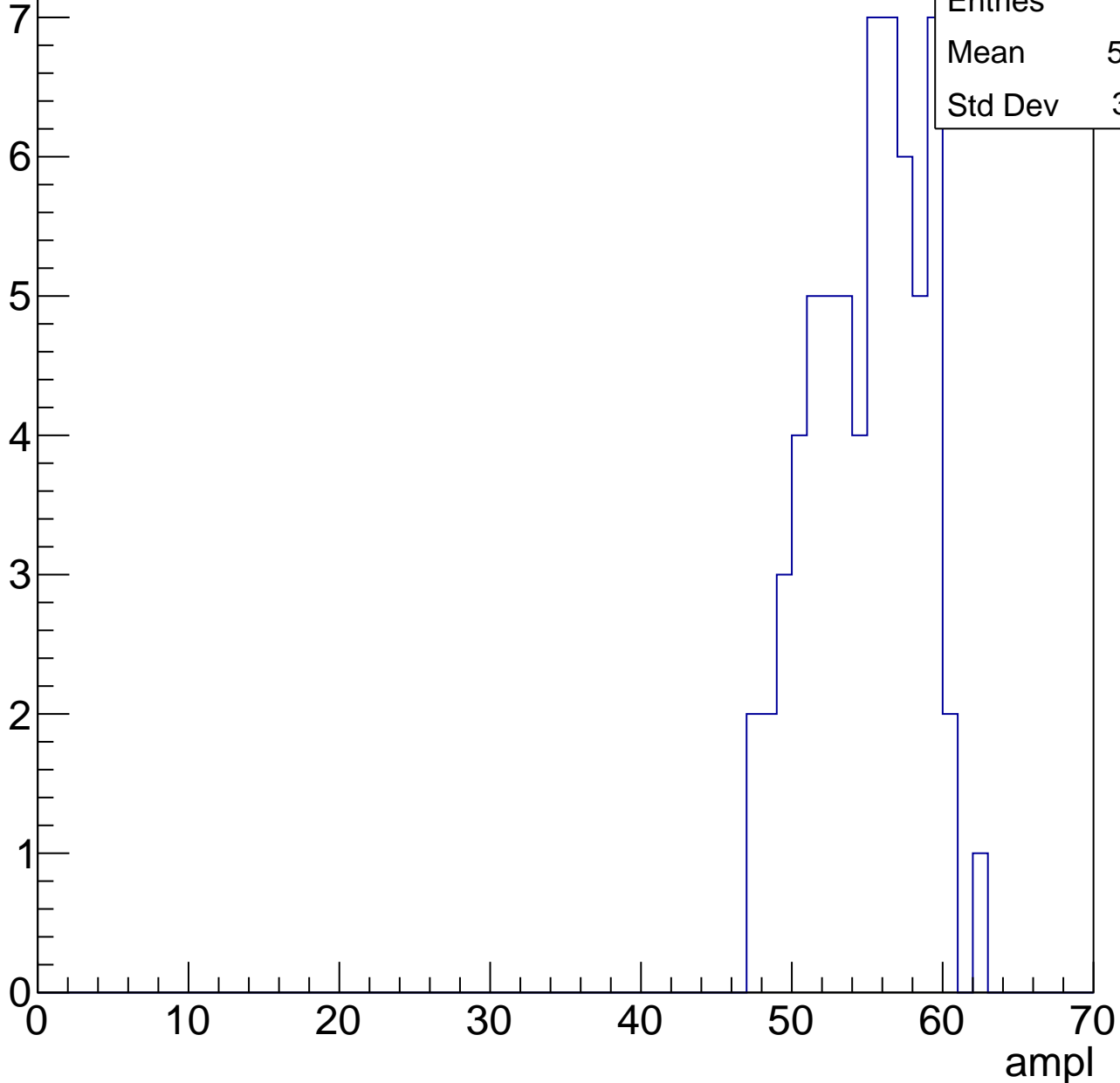


# B1L103S, U11-ch44, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	54.42
Std Dev	3.611

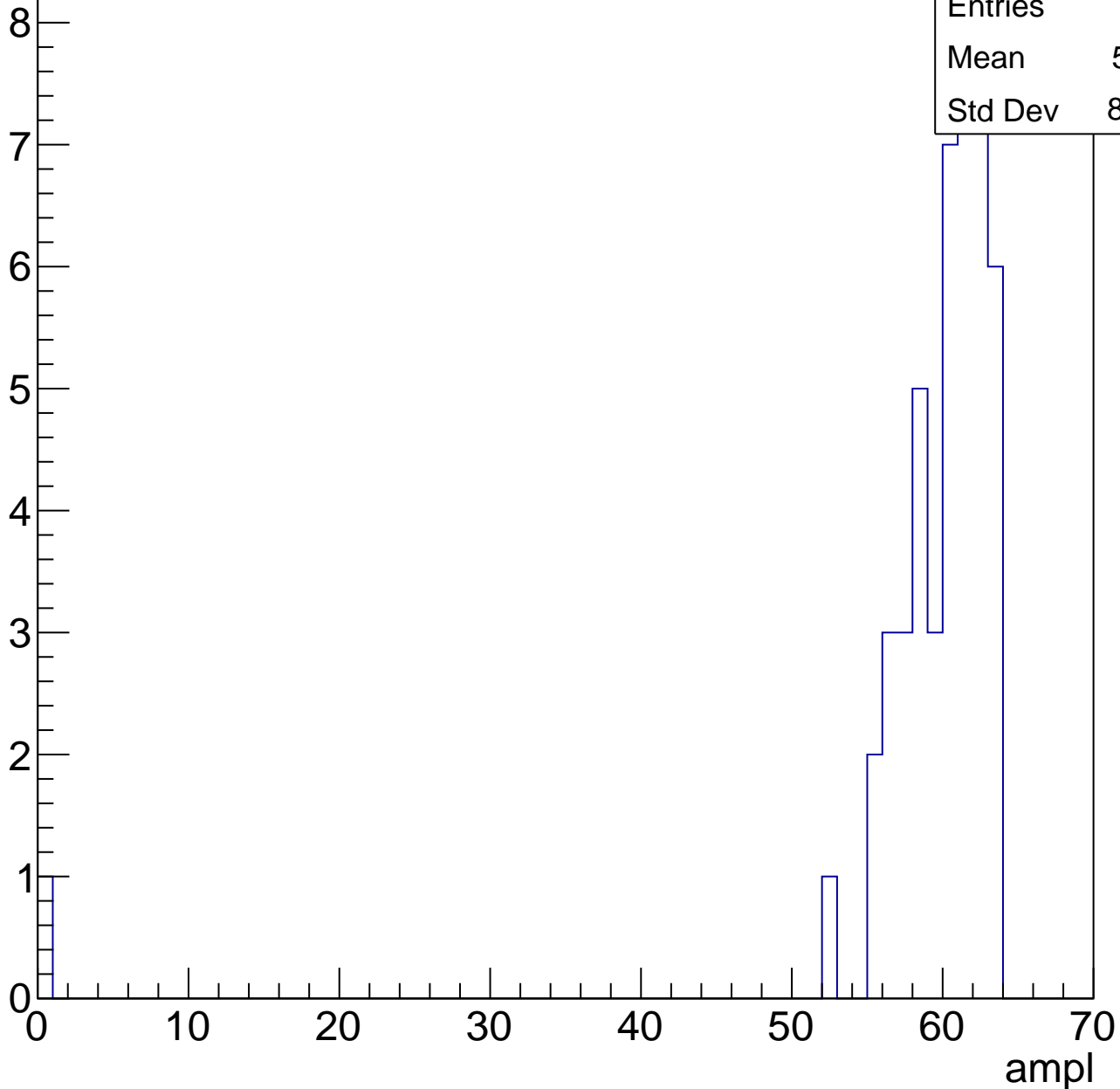


# B1L103S, U11-ch44, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

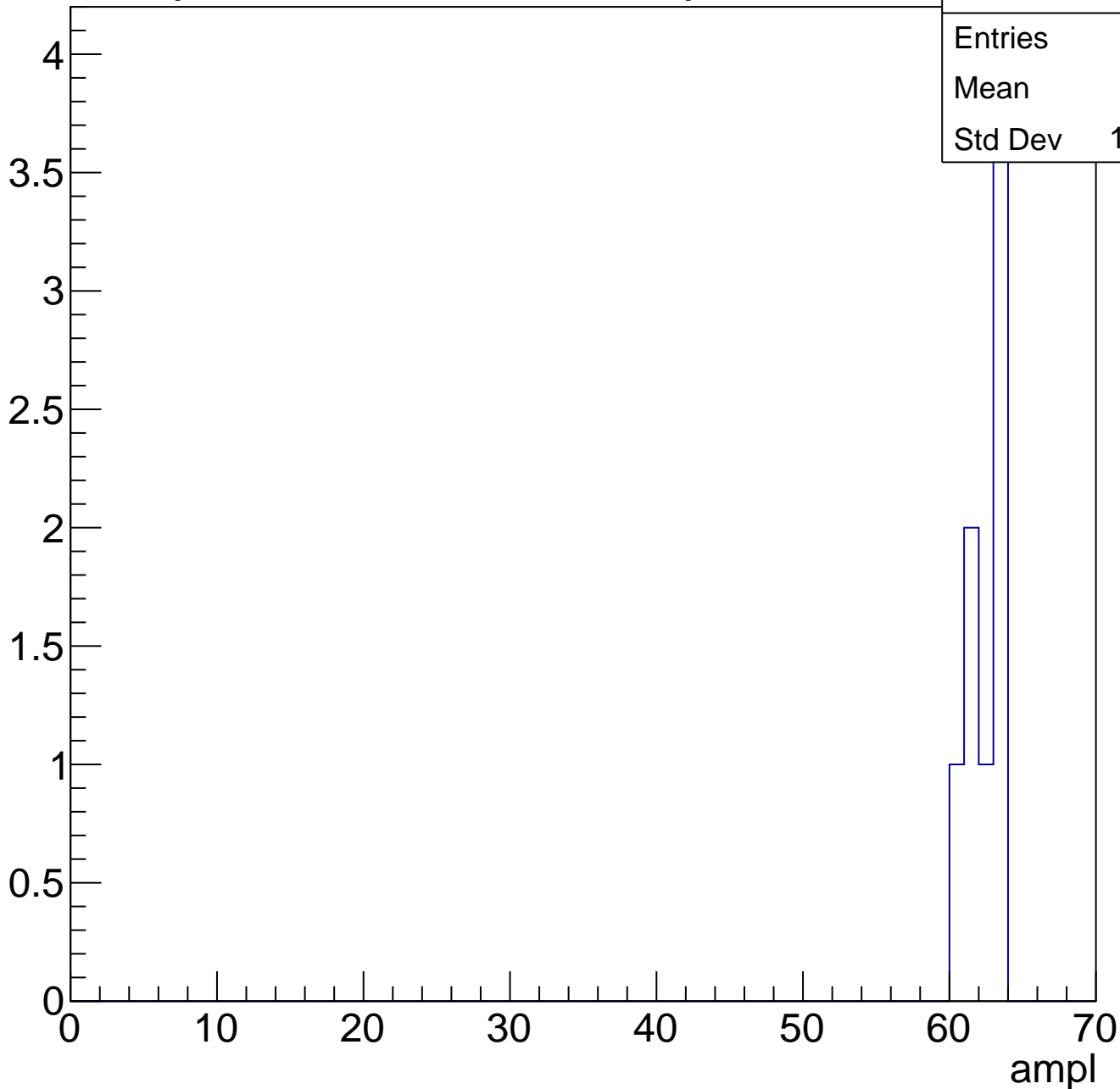
Entries	47
Mean	58.51
Std Dev	8.994



# B1L103S, U11-ch44, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U11-ch44, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L103S, U11-ch45, adc0

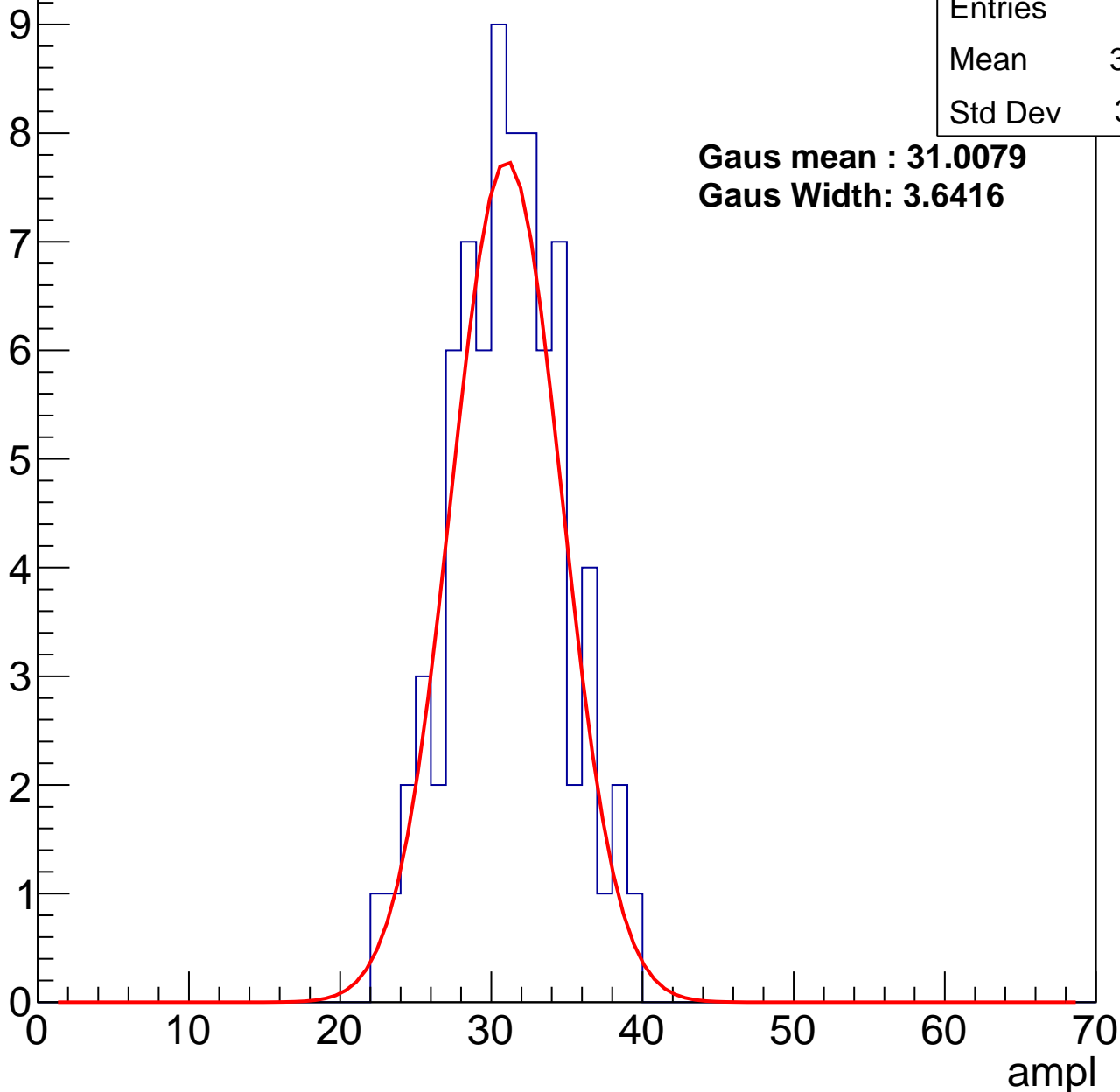
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	76
Mean	30.63
Std Dev	3.641

**Gaus mean : 31.0079**

**Gaus Width: 3.6416**



# B1L103S, U11-ch45, adc1

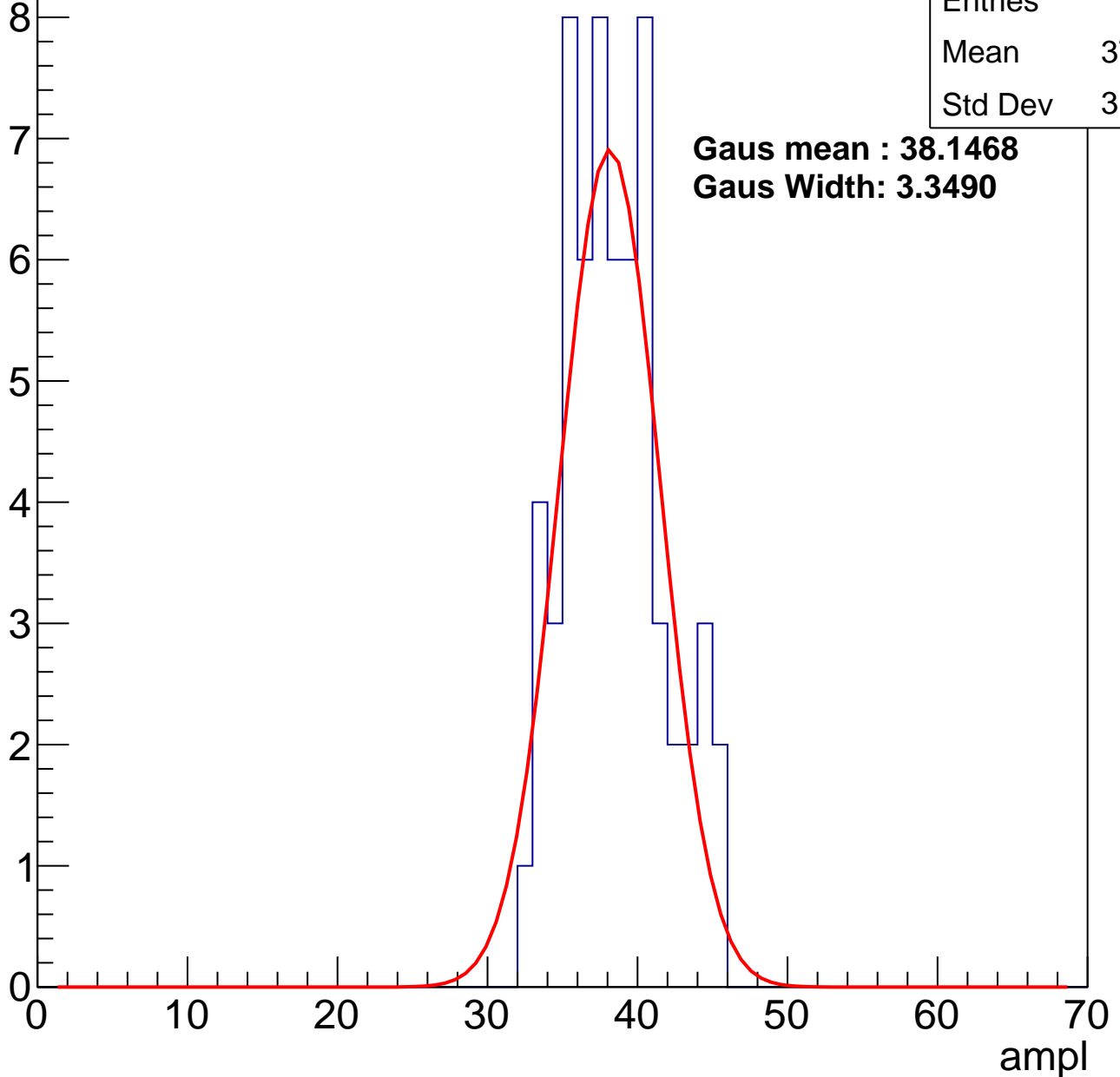
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	37.98
Std Dev	3.215

**Gaus mean : 38.1468**

**Gaus Width: 3.3490**



# B1L103S, U11-ch45, adc2

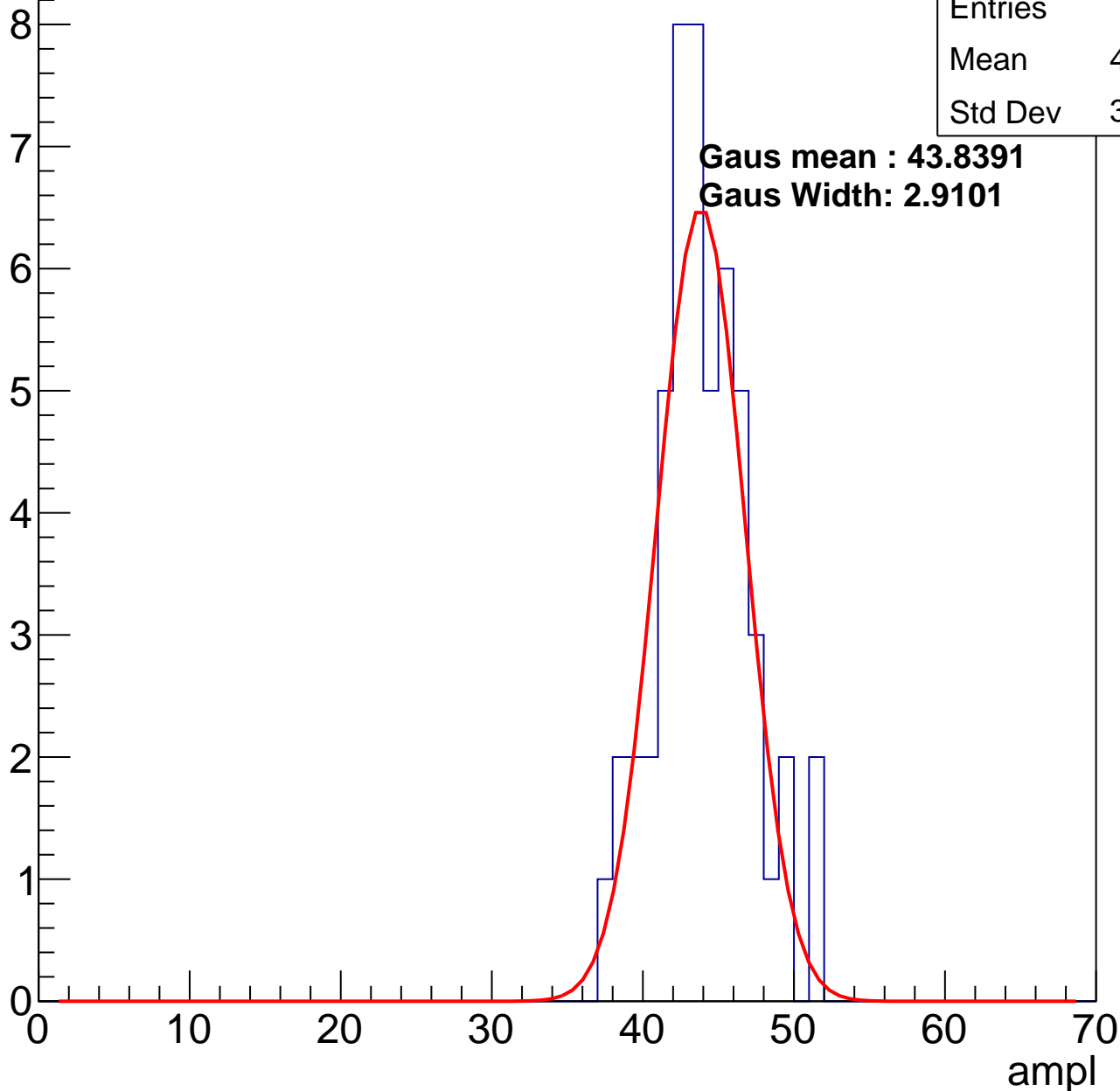
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	52
Mean	43.56
Std Dev	3.085

**Gaus mean : 43.8391**

**Gaus Width: 2.9101**



# B1L103S, U11-ch45, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

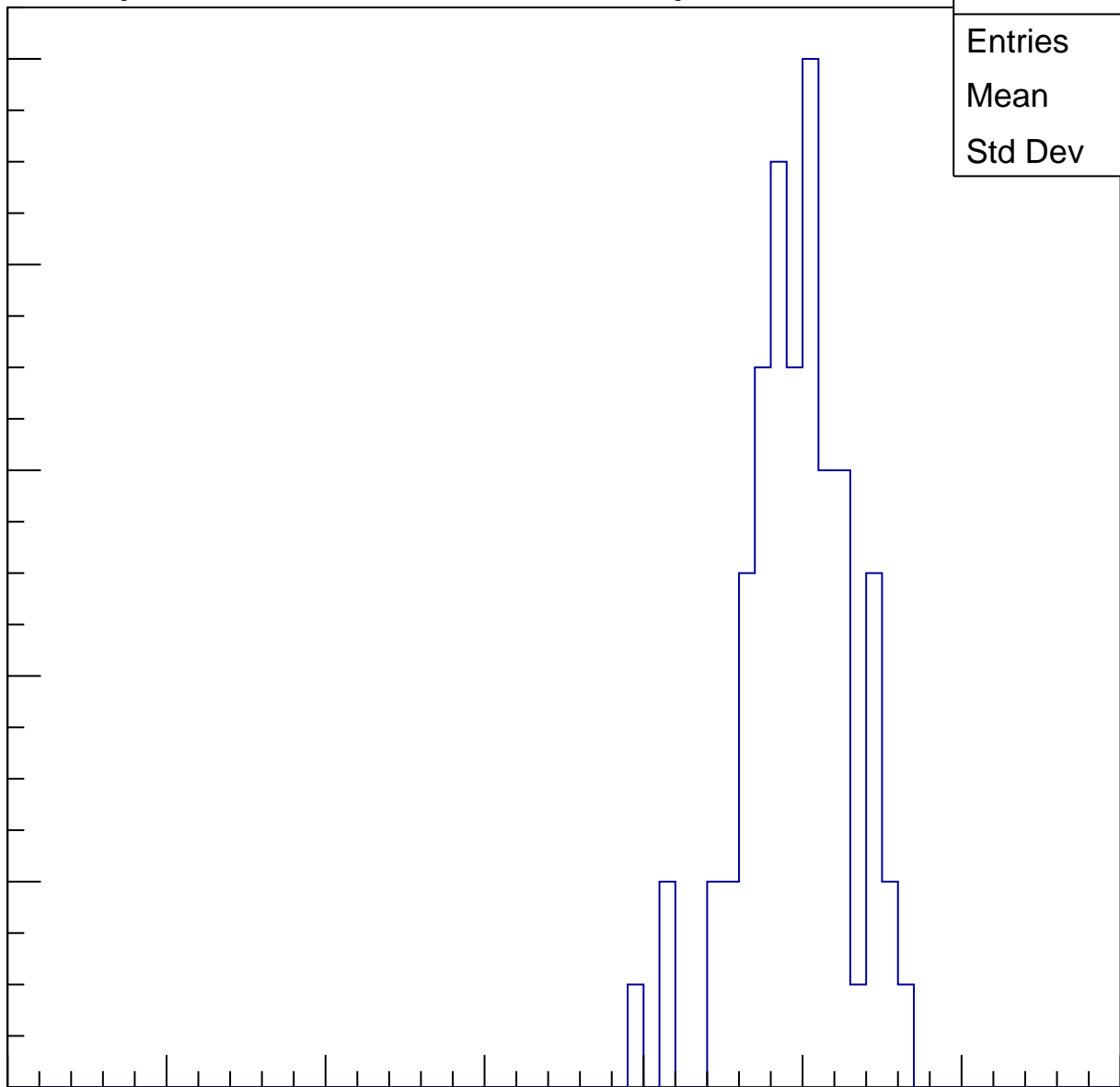
Entries	66
Mean	49.09
Std Dev	3.352

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

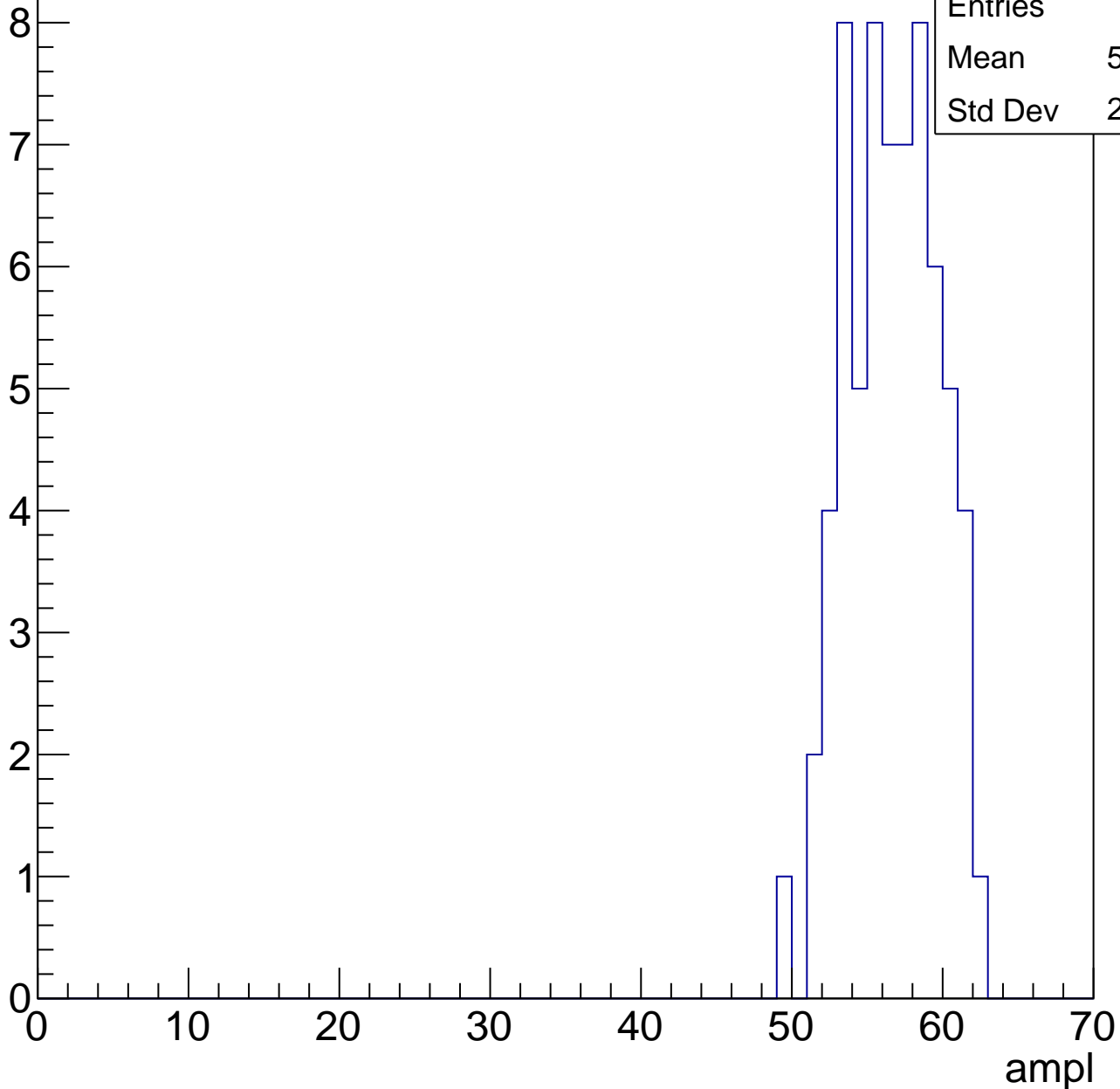


# B1L103S, U11-ch45, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	56.18
Std Dev	2.938

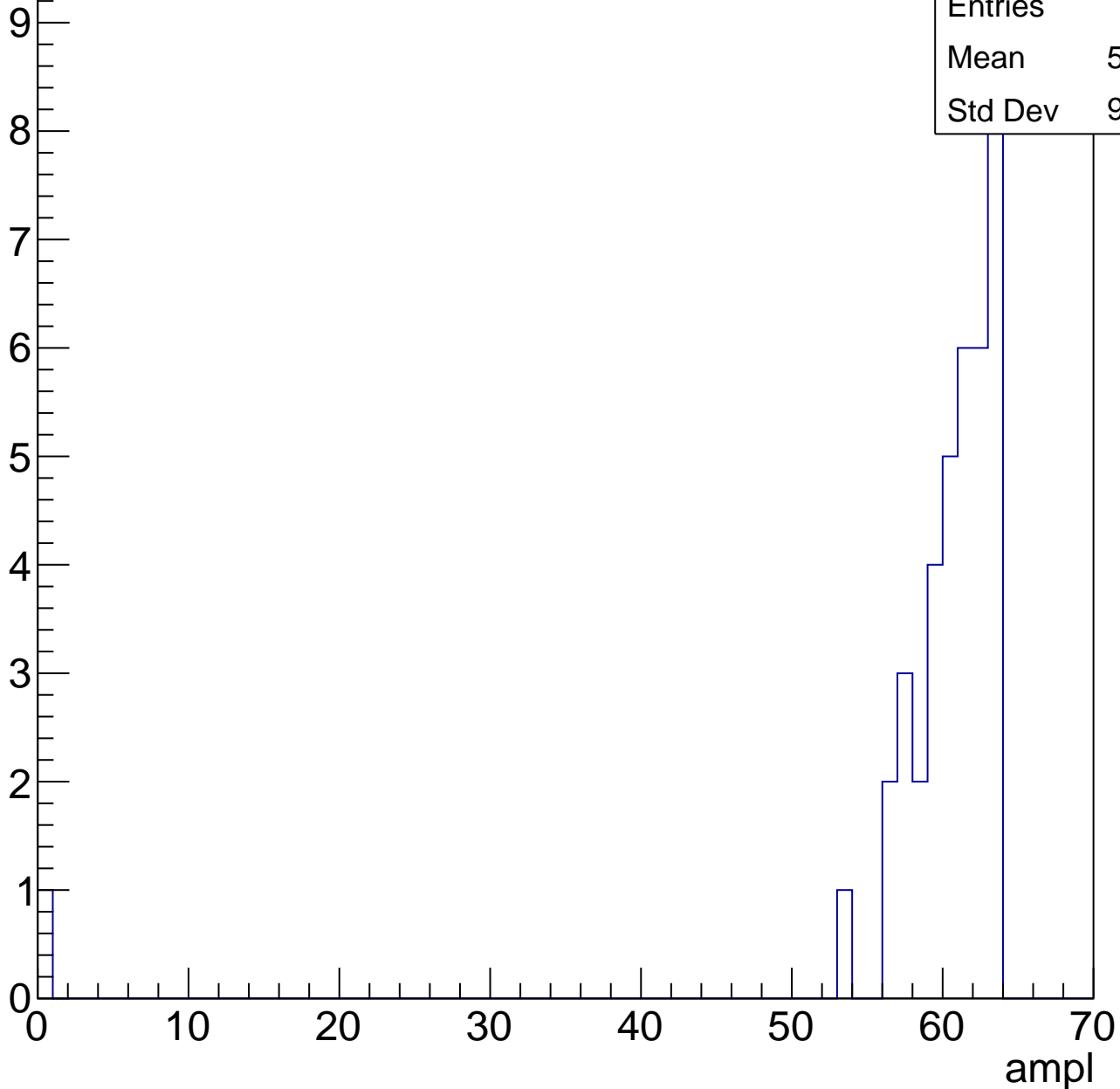


# B1L103S, U11-ch45, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	39
Mean	58.79
Std Dev	9.838



# B1L103S, U11-ch45, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U11-ch45, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U11-ch46, adc0

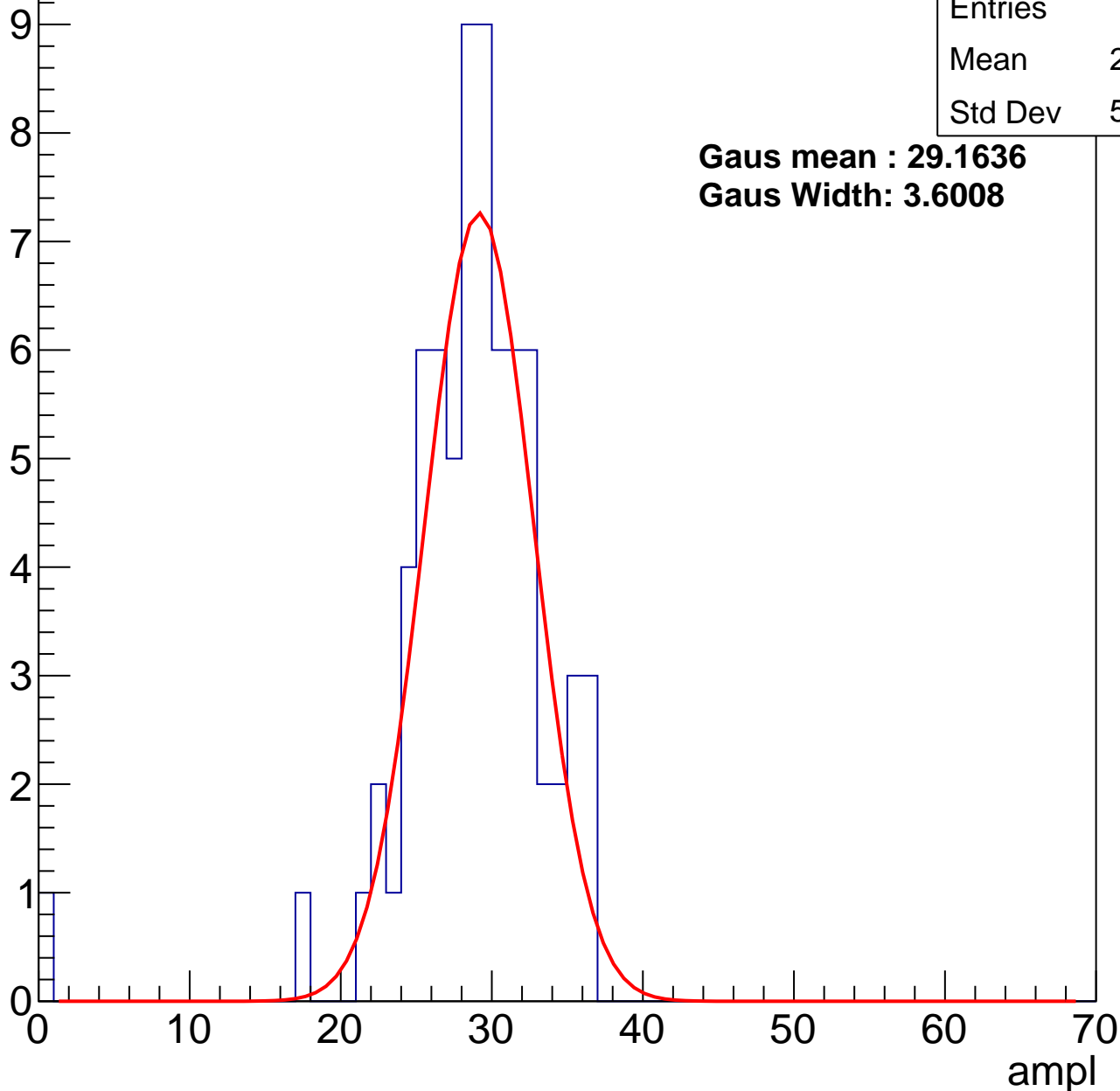
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	73
Mean	28.22
Std Dev	5.018

**Gaus mean : 29.1636**

**Gaus Width: 3.6008**



# B1L103S, U11-ch46, adc1

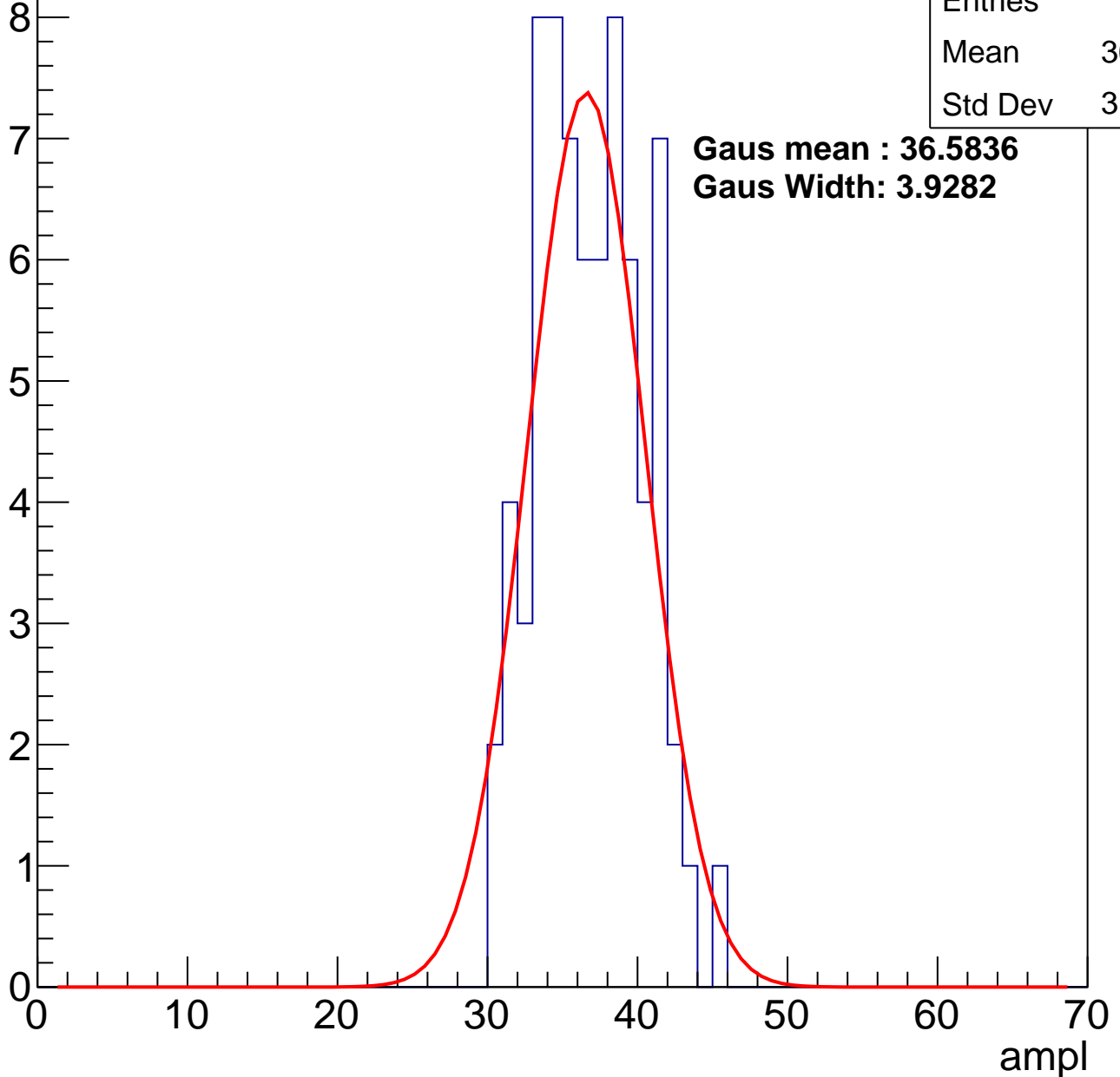
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	73
Mean	36.38
Std Dev	3.419

**Gaus mean : 36.5836**

**Gaus Width: 3.9282**



# B1L103S, U11-ch46, adc2

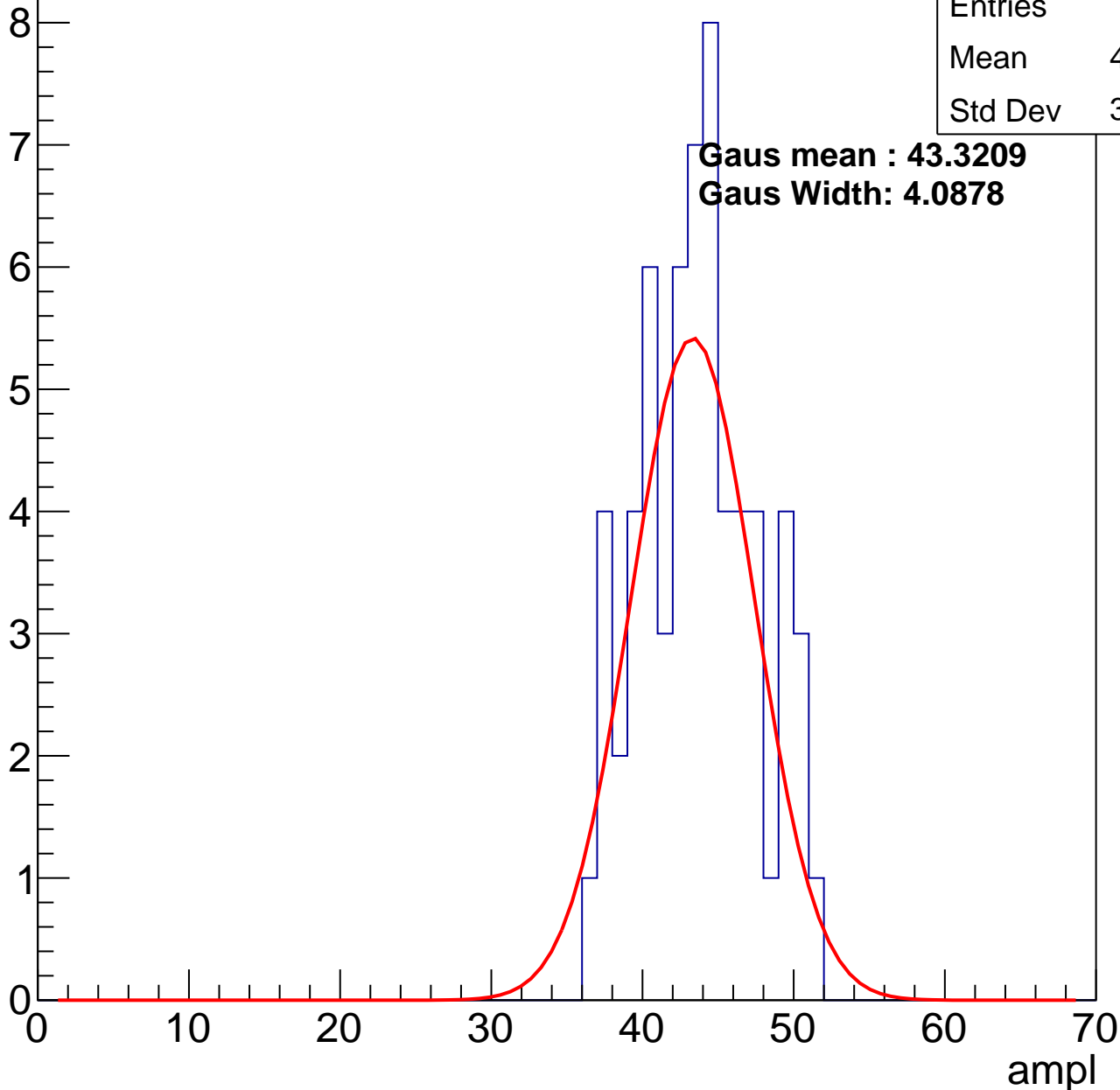
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	43.24
Std Dev	3.766

**Gaus mean : 43.3209**

**Gaus Width: 4.0878**

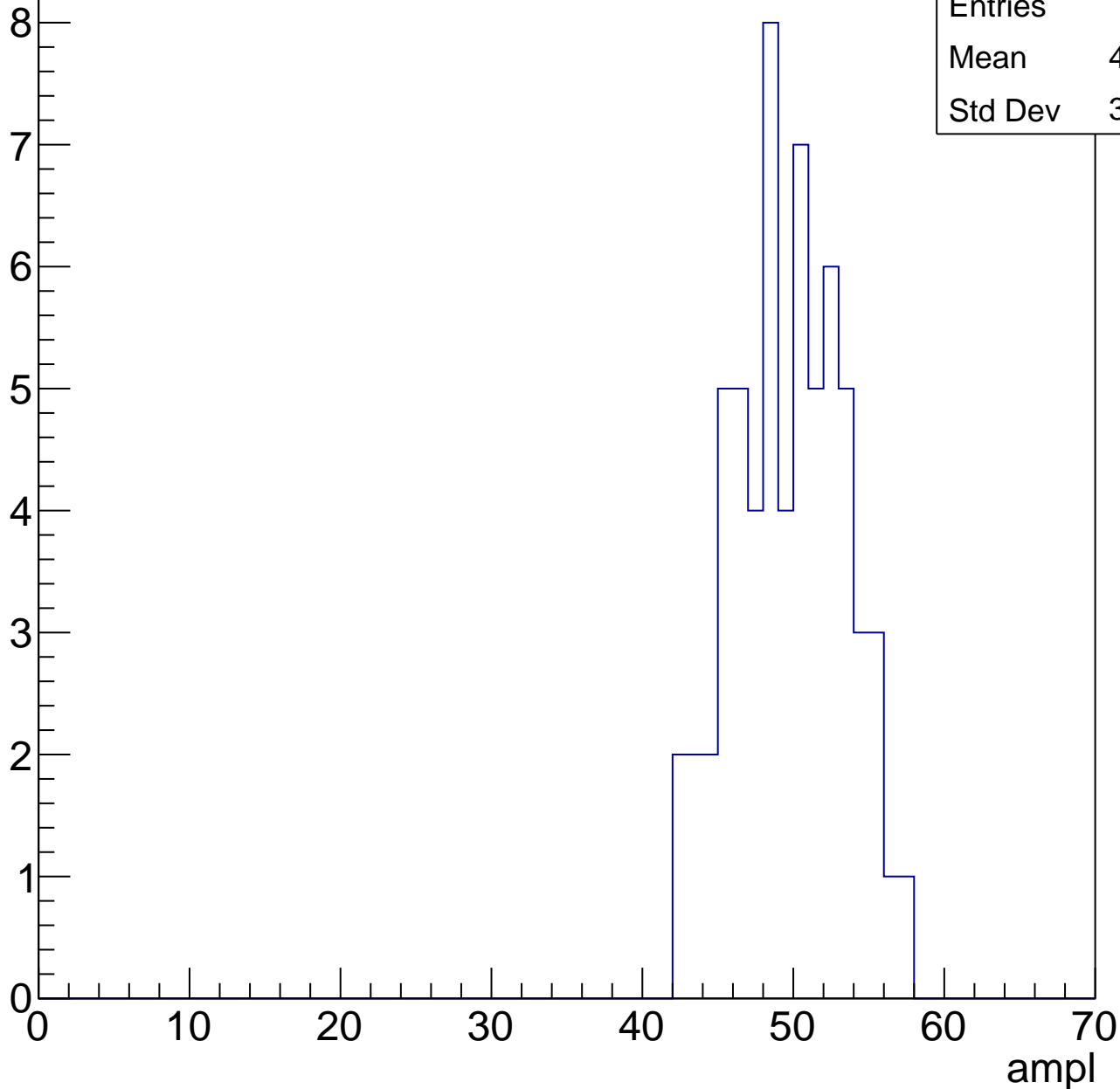


# B1L103S, U11-ch46, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	49.25
Std Dev	3.612

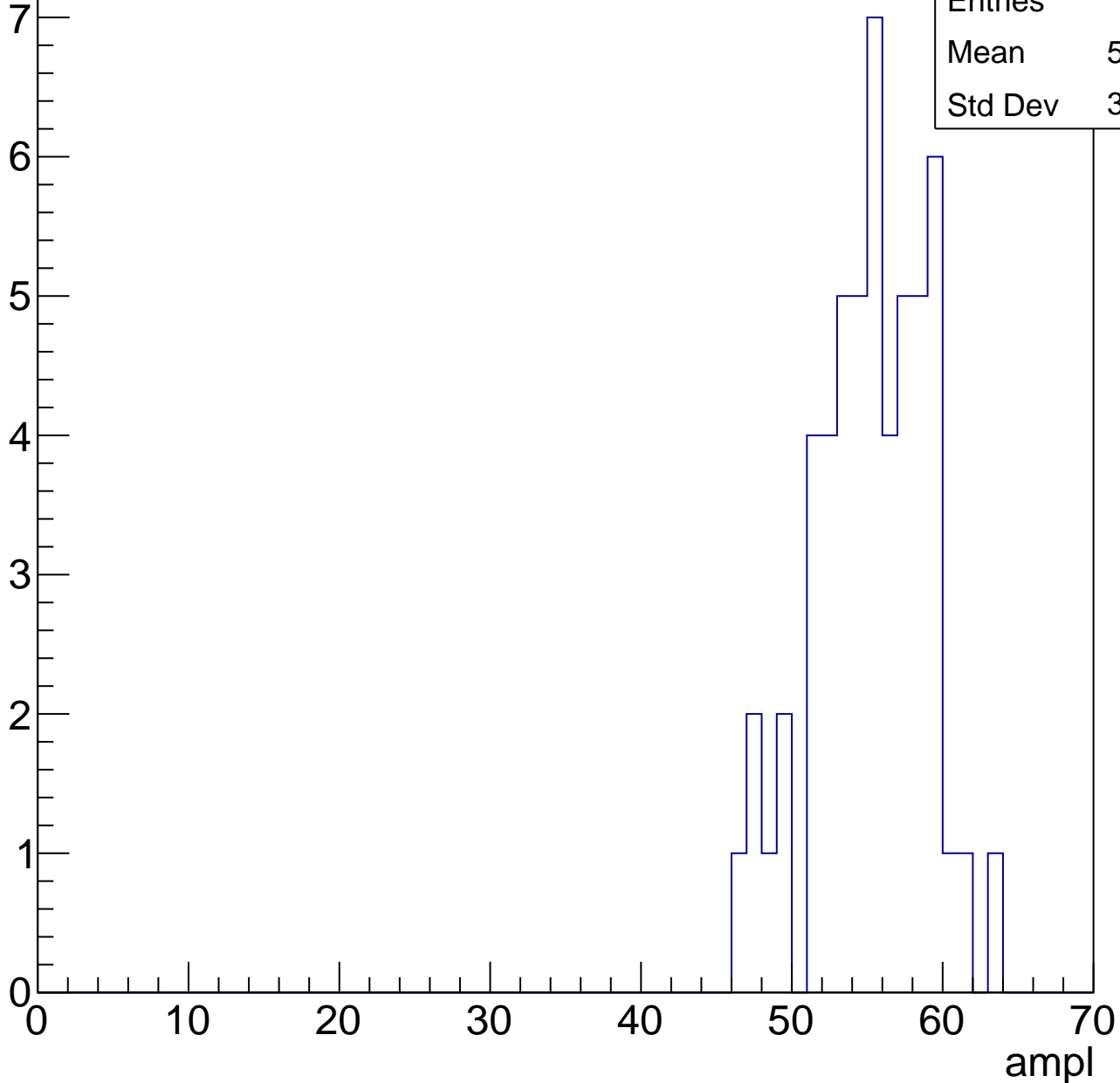


# B1L103S, U11-ch46, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

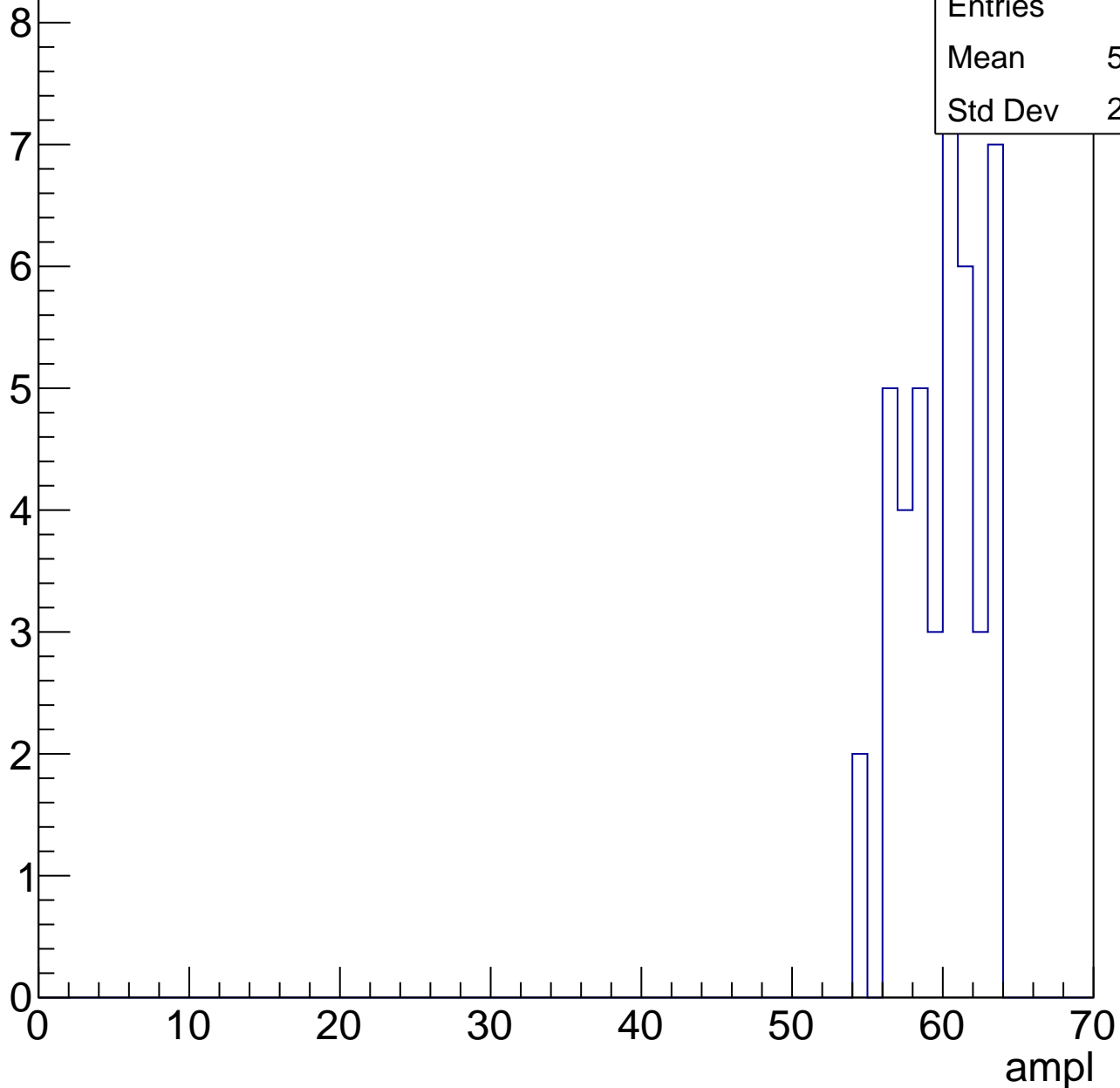
Entries	54
Mean	54.72
Std Dev	3.704



# B1L103S, U11-ch46, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

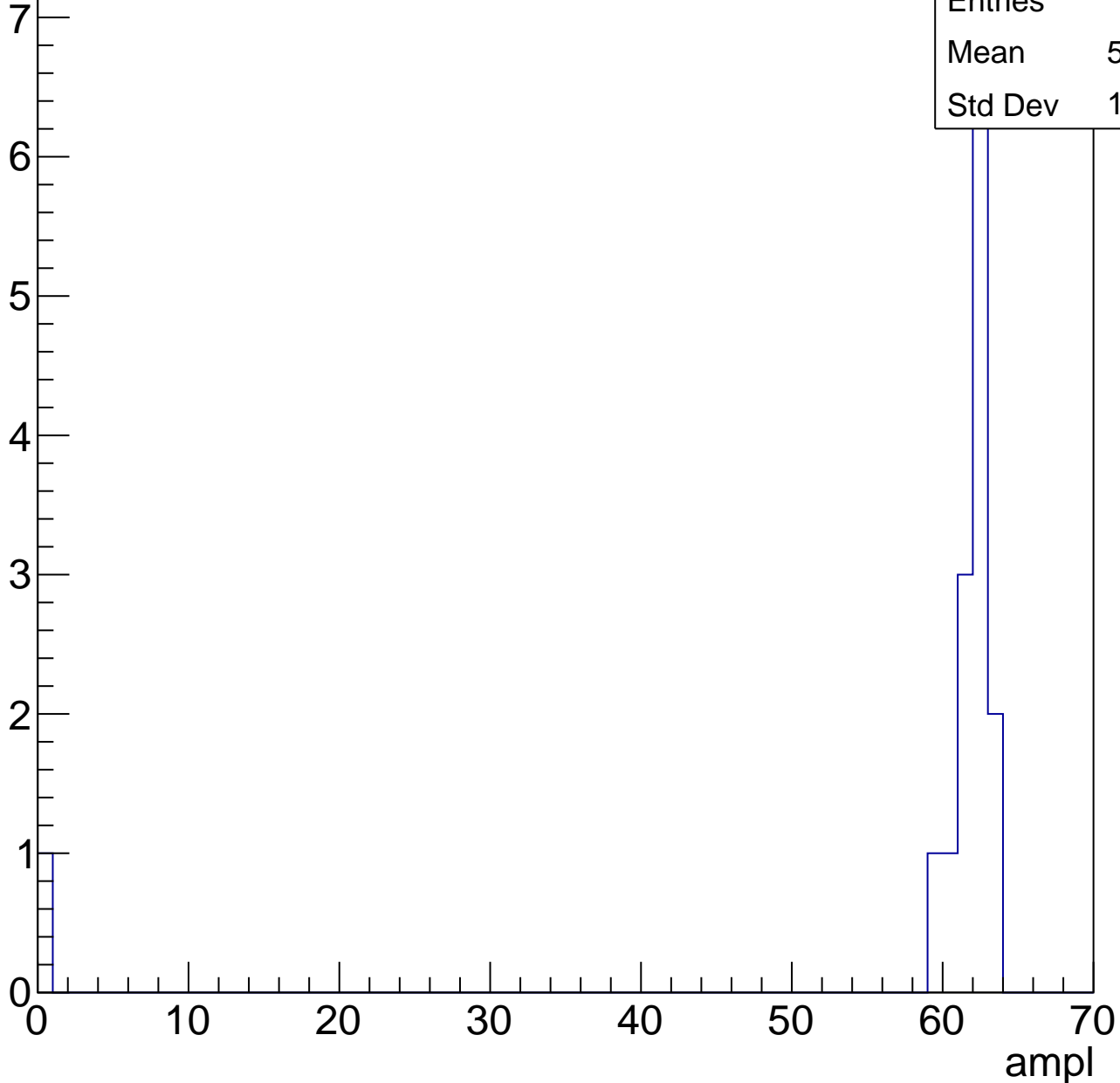


# B1L103S, U11-ch46, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	15
Mean	57.47
Std Dev	15.39





# B1L103S, U11-ch46, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L103S, U11-ch47, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	64
Mean	31.05
Std Dev	3.164

**Gaus mean : 32.0794**

**Gaus Width: 2.9726**

Entry

10  
8  
6  
4  
2  
0

ampl

0

10

20

30

40

50

60

70

# B1L103S, U11-ch47, adc1

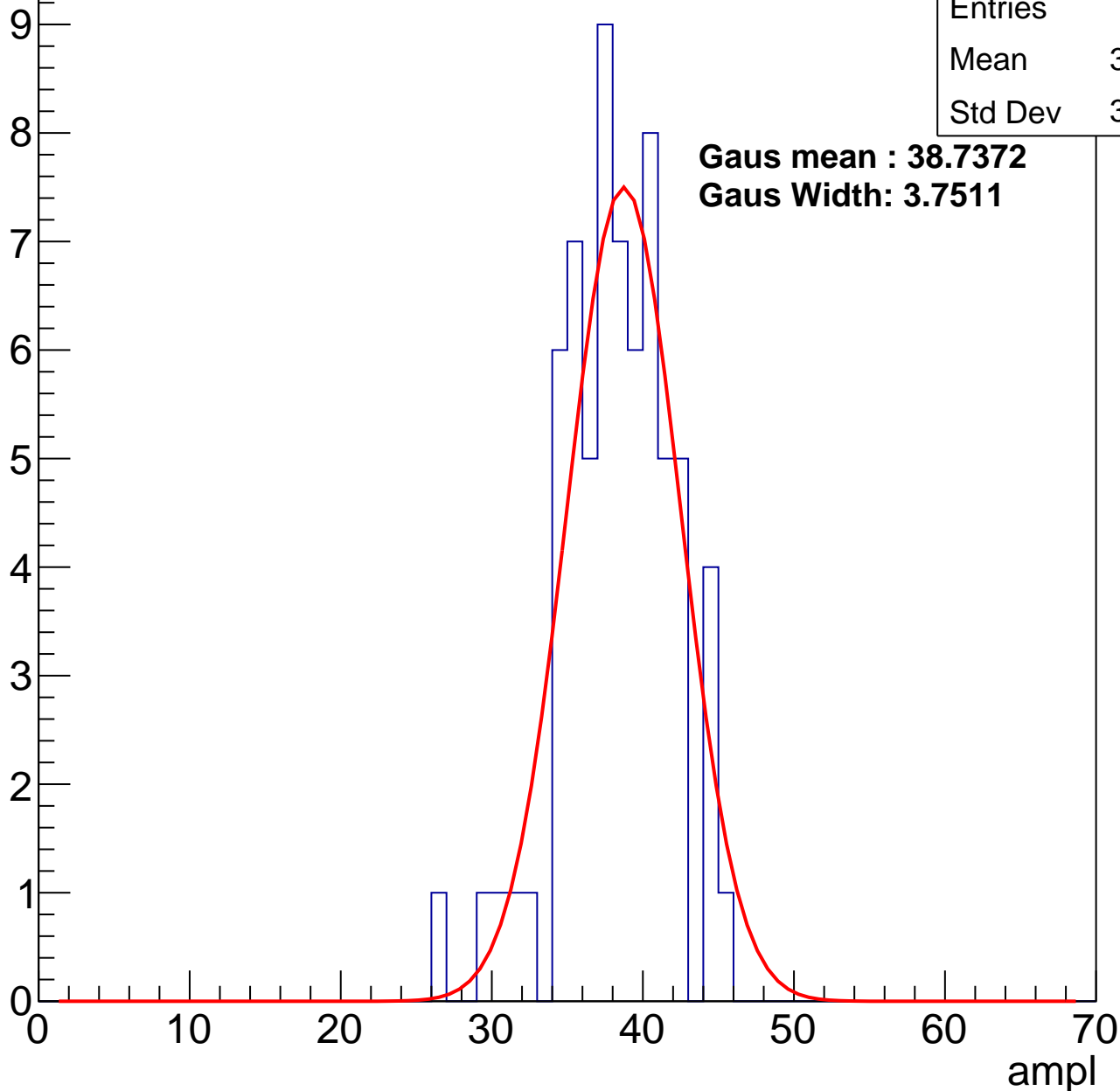
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	68
Mean	37.74
Std Dev	3.665

**Gaus mean : 38.7372**

**Gaus Width: 3.7511**



# B1L103S, U11-ch47, adc2

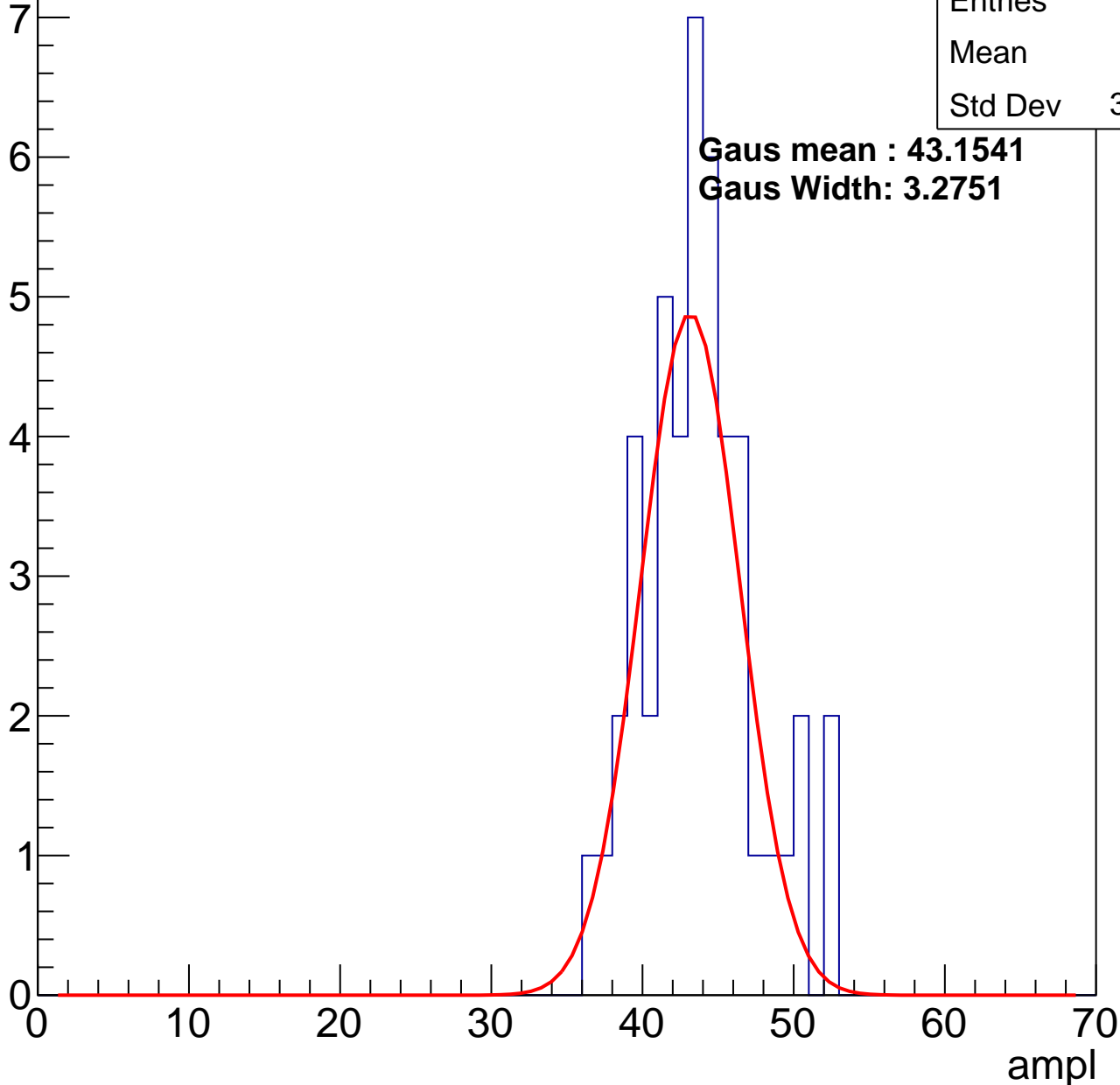
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	47
Mean	43.3
Std Dev	3.666

**Gaus mean : 43.1541**

**Gaus Width: 3.2751**

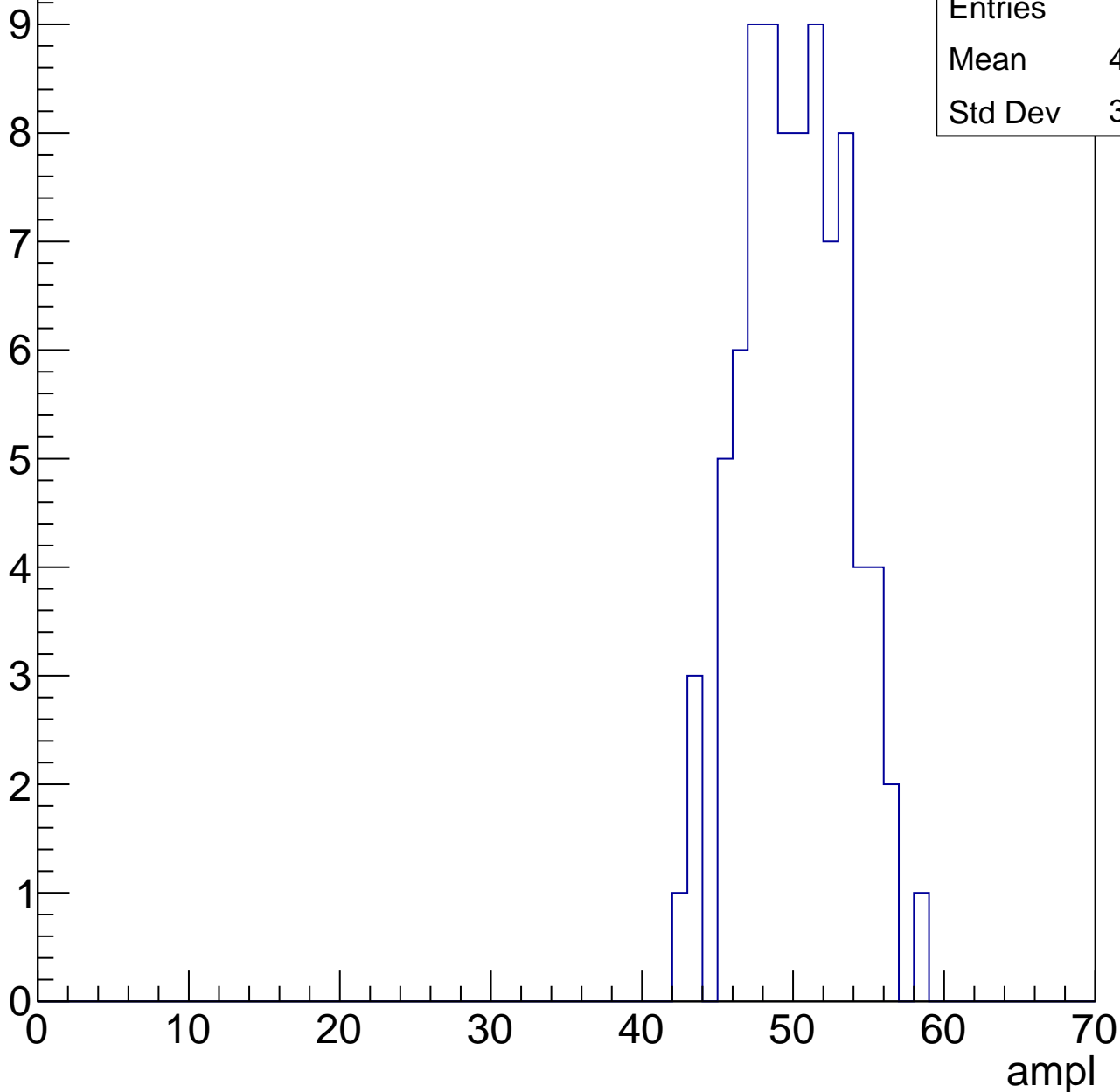


# B1L103S, U11-ch47, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

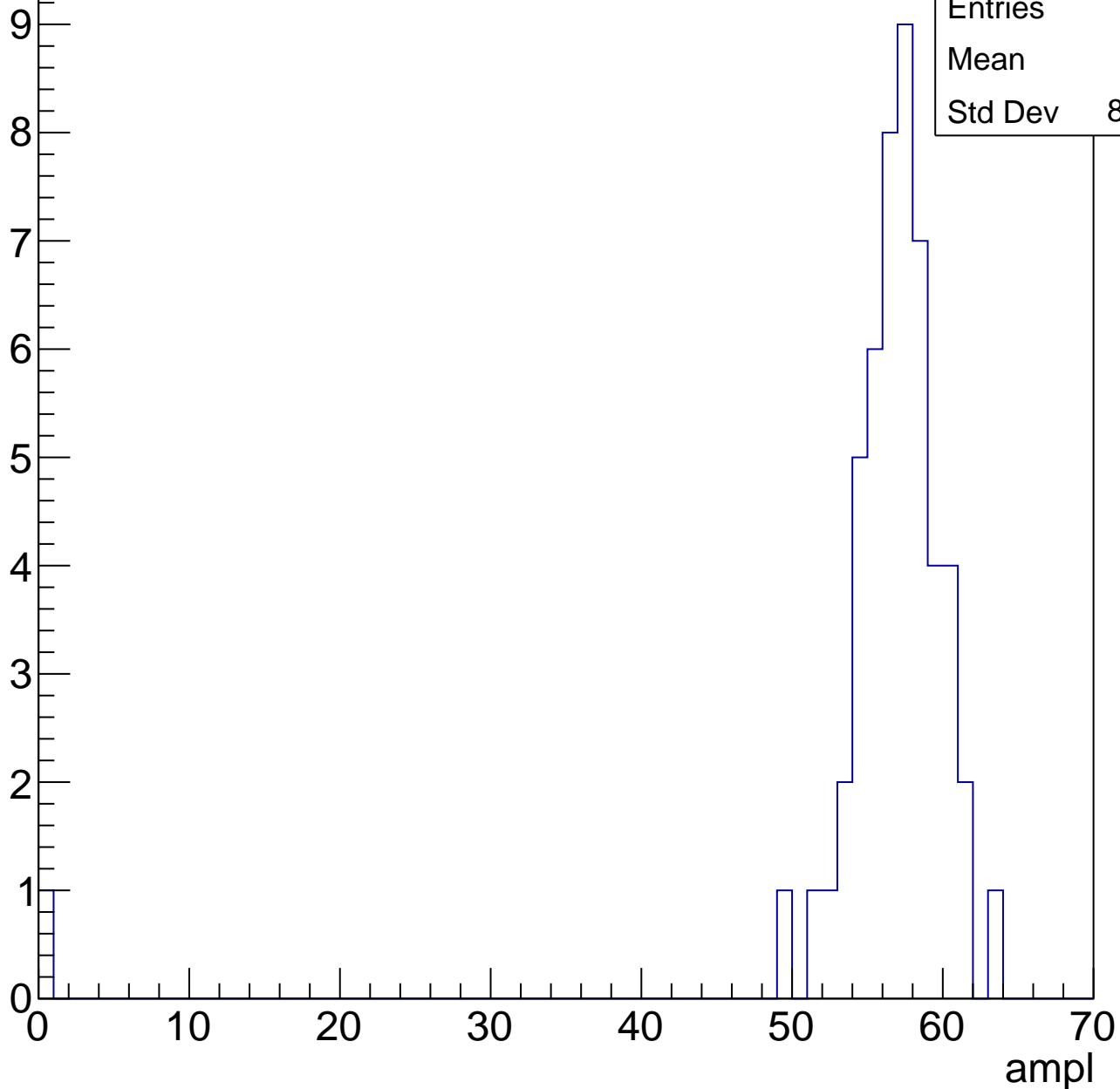
Entries	84
Mean	49.67
Std Dev	3.375



# B1L103S, U11-ch47, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

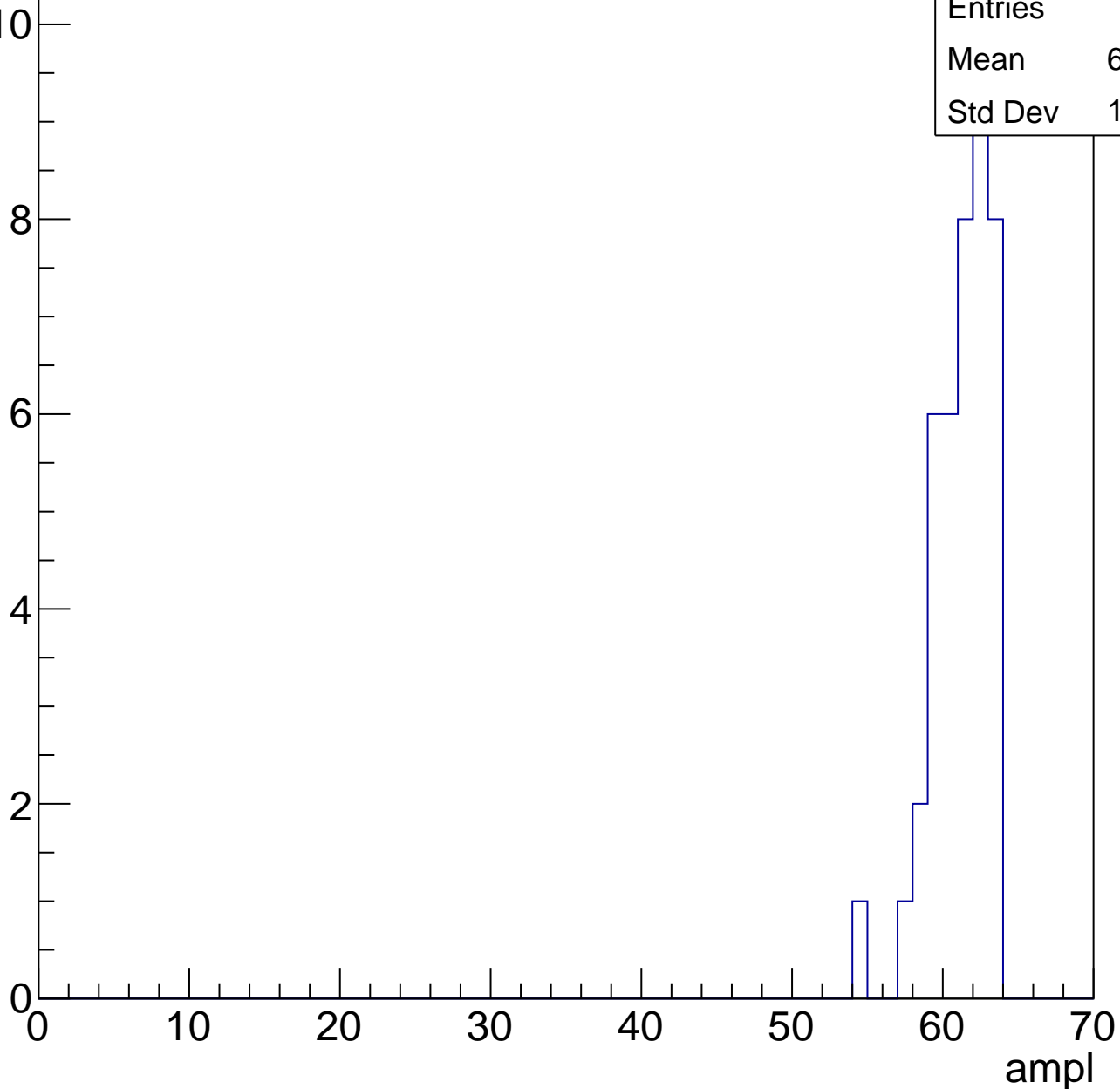


# B1L103S, U11-ch47, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	42
Mean	60.79
Std Dev	1.909



# B1L103S, U11-ch47, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



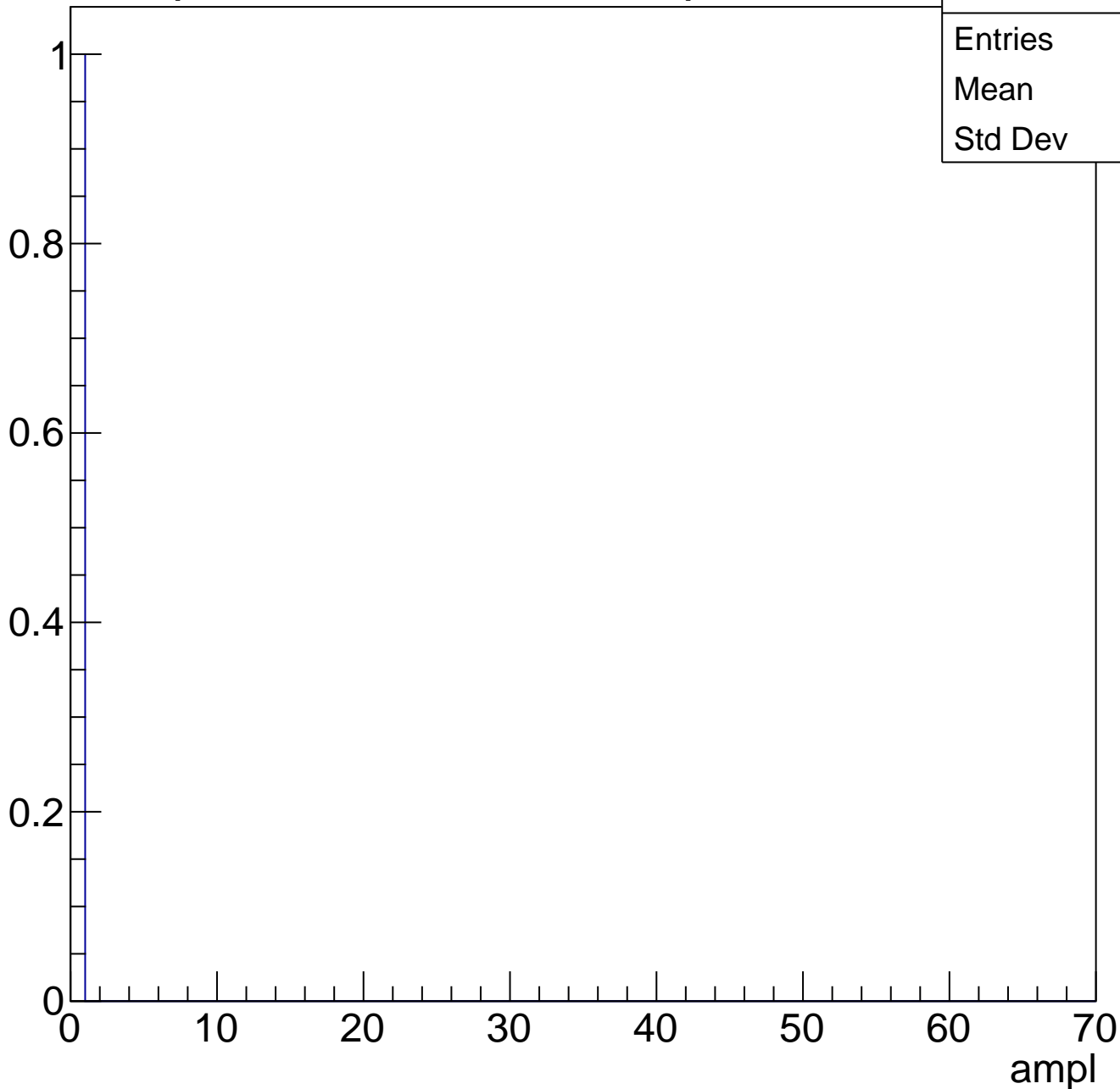
Entries	1
Mean	63
Std Dev	0



# B1L103S, U11-ch47, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U11-ch48, adc0

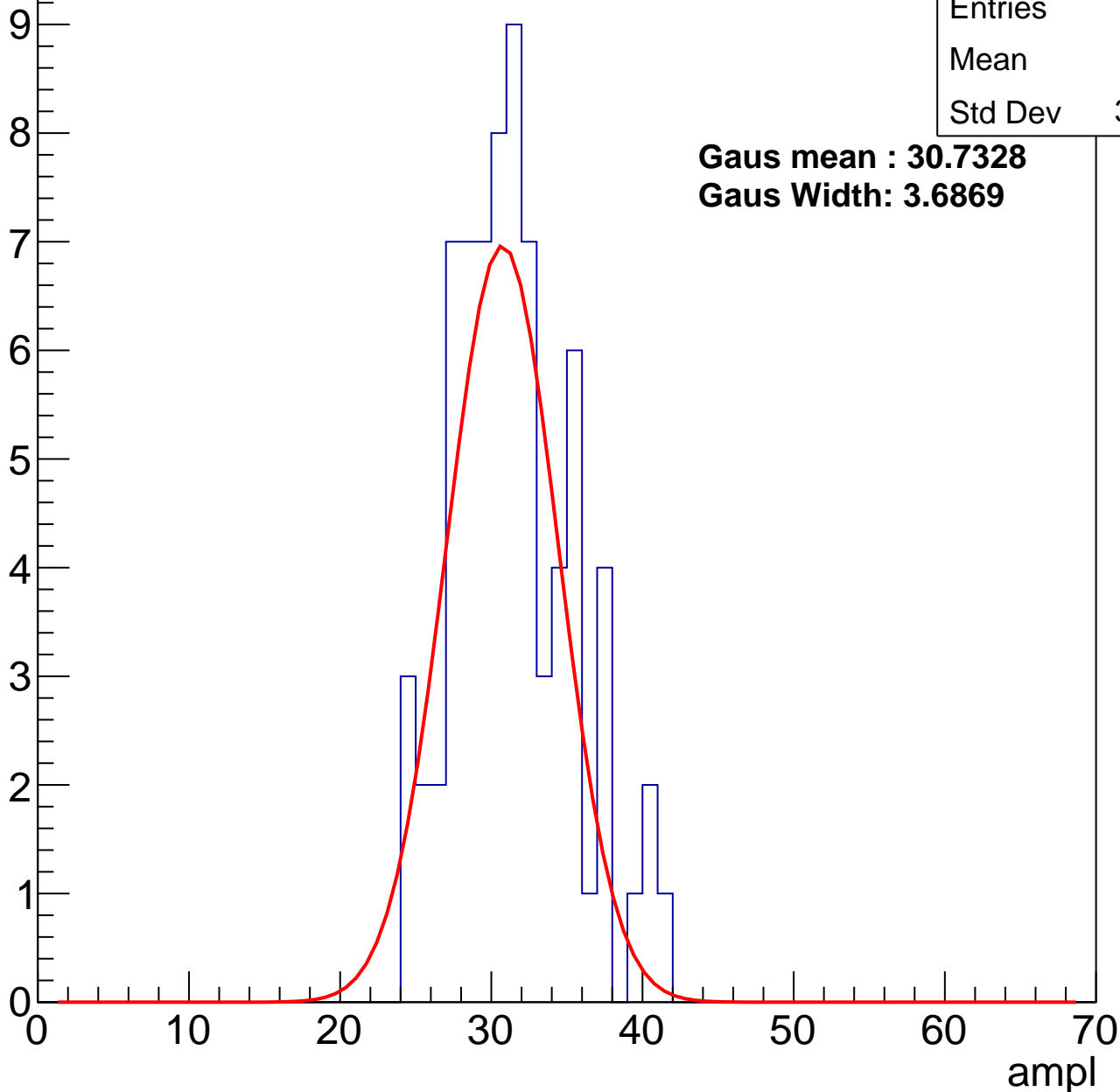
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	74
Mean	31
Std Dev	3.901

**Gaus mean : 30.7328**

**Gaus Width: 3.6869**



# B1L103S, U11-ch48, adc1

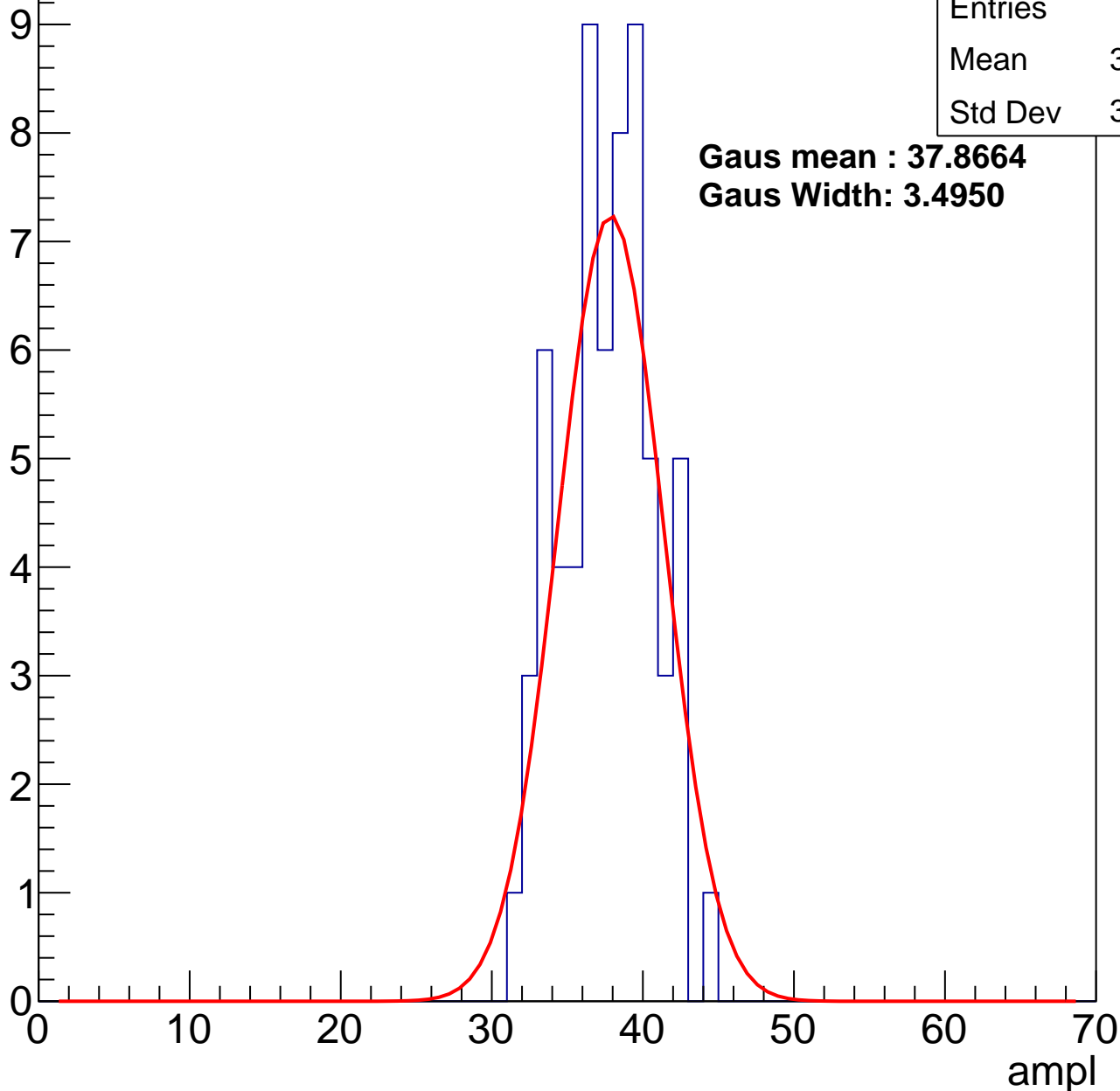
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	37.17
Std Dev	3.003

**Gaus mean : 37.8664**

**Gaus Width: 3.4950**



# B1L103S, U11-ch48, adc2

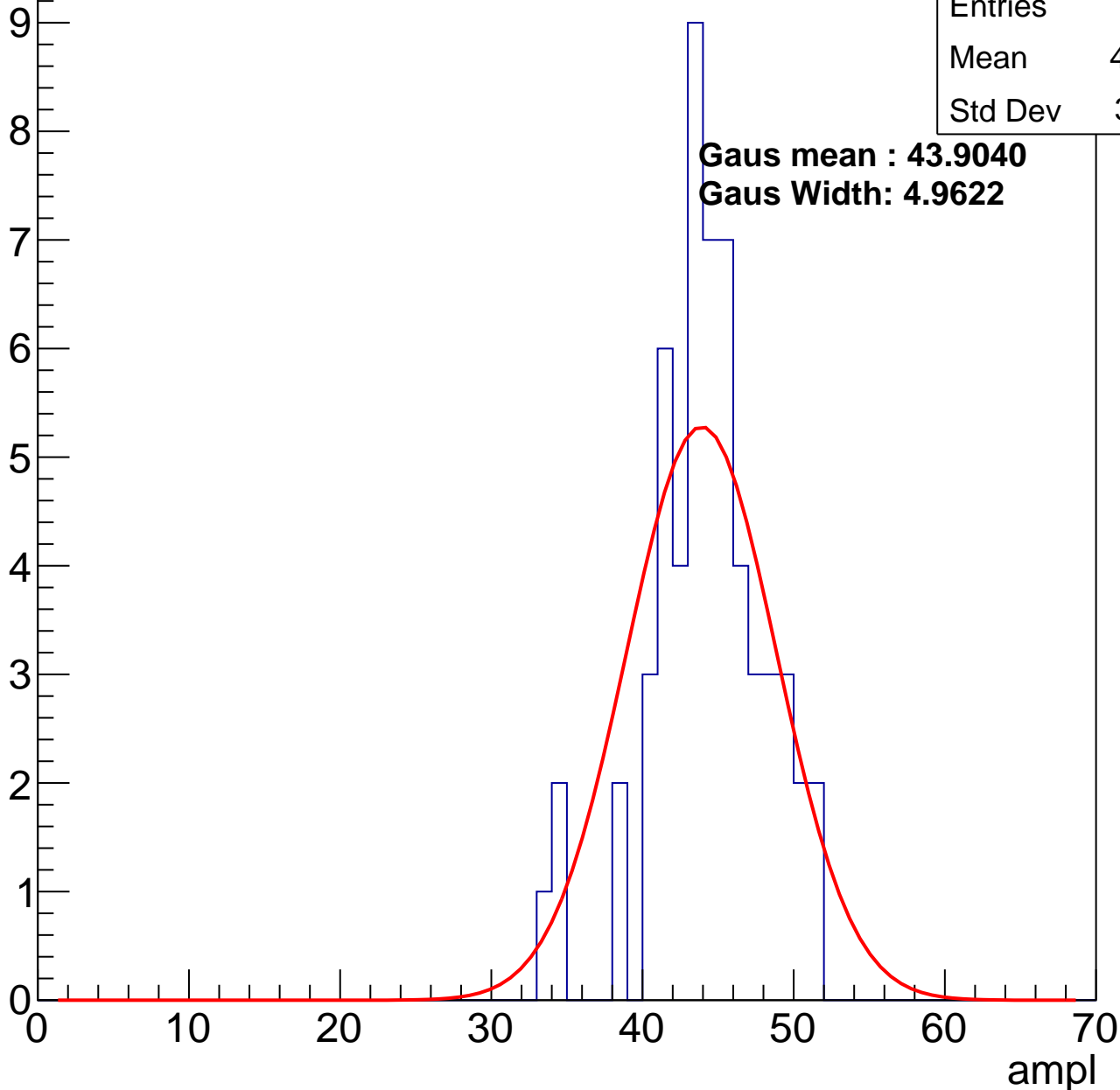
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	58
Mean	43.78
Std Dev	3.851

**Gaus mean : 43.9040**

**Gaus Width: 4.9622**

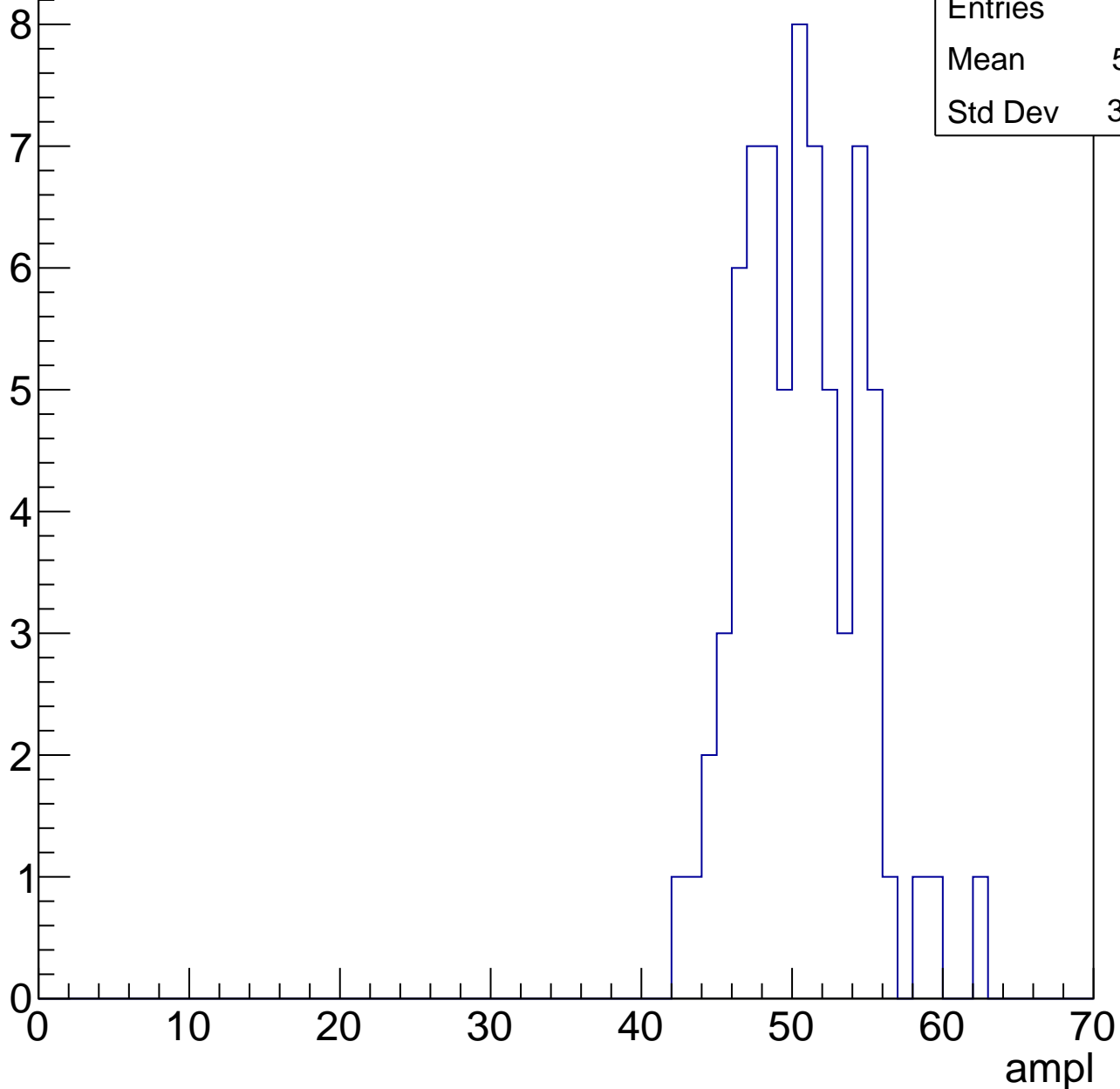


# B1L103S, U11-ch48, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	71
Mean	50.11
Std Dev	3.877

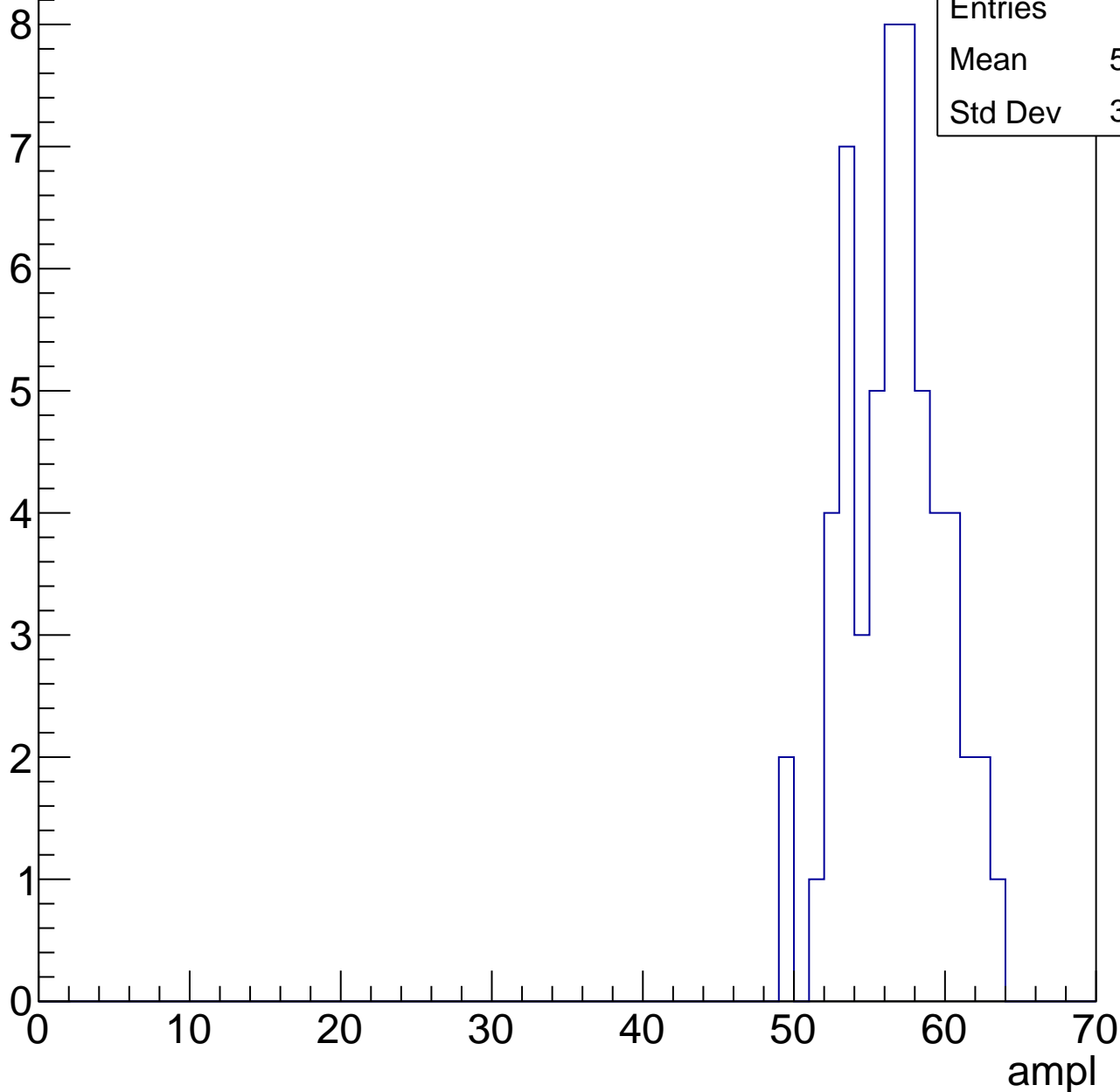


# B1L103S, U11-ch48, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	56
Mean	56.14
Std Dev	3.176

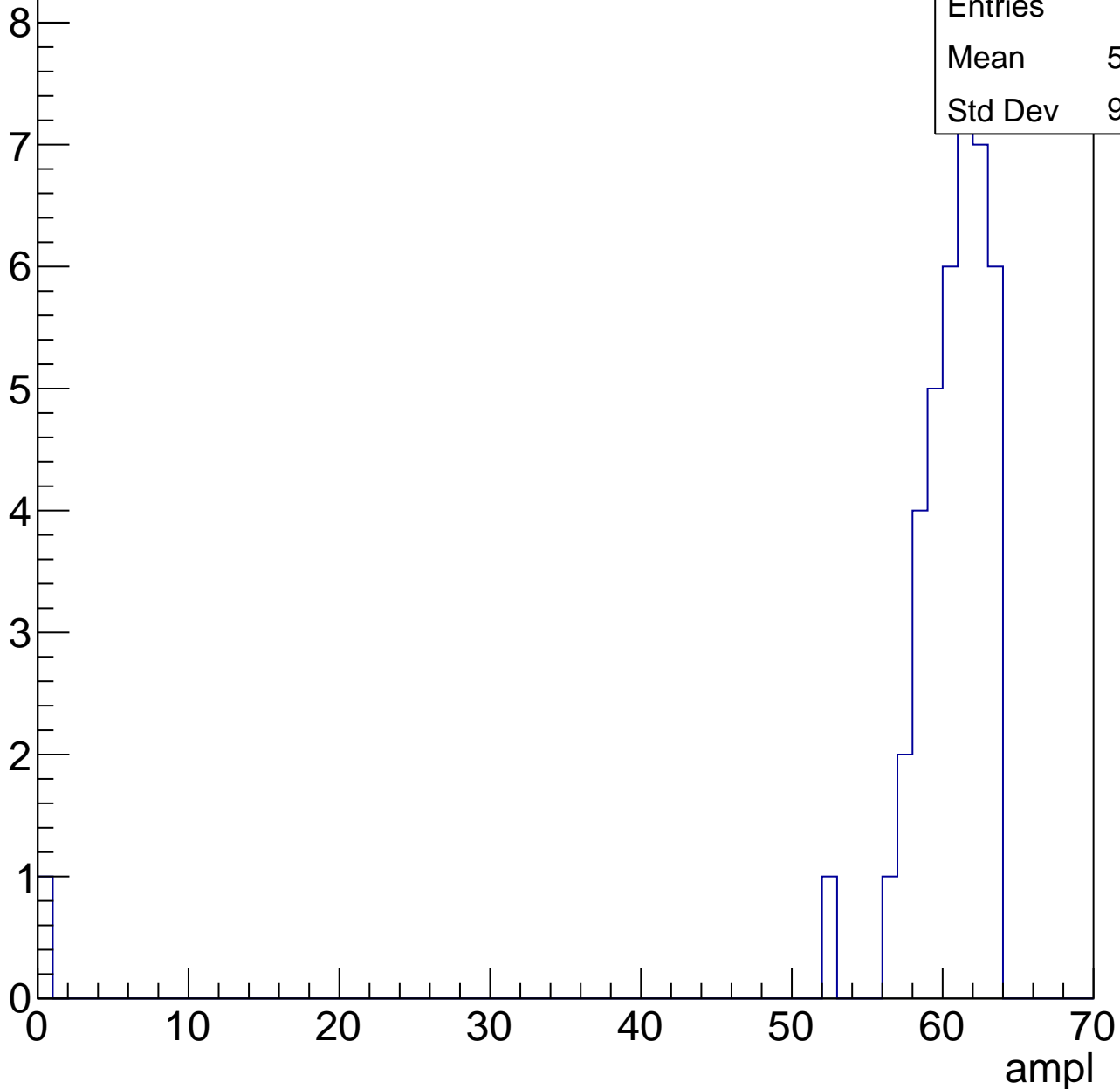


# B1L103S, U11-ch48, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	41
Mean	58.76
Std Dev	9.558



# B1L103S, U11-ch48, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U11-ch48, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	2
Mean	11
Std Dev	11

# B1L103S, U11-ch49, adc0

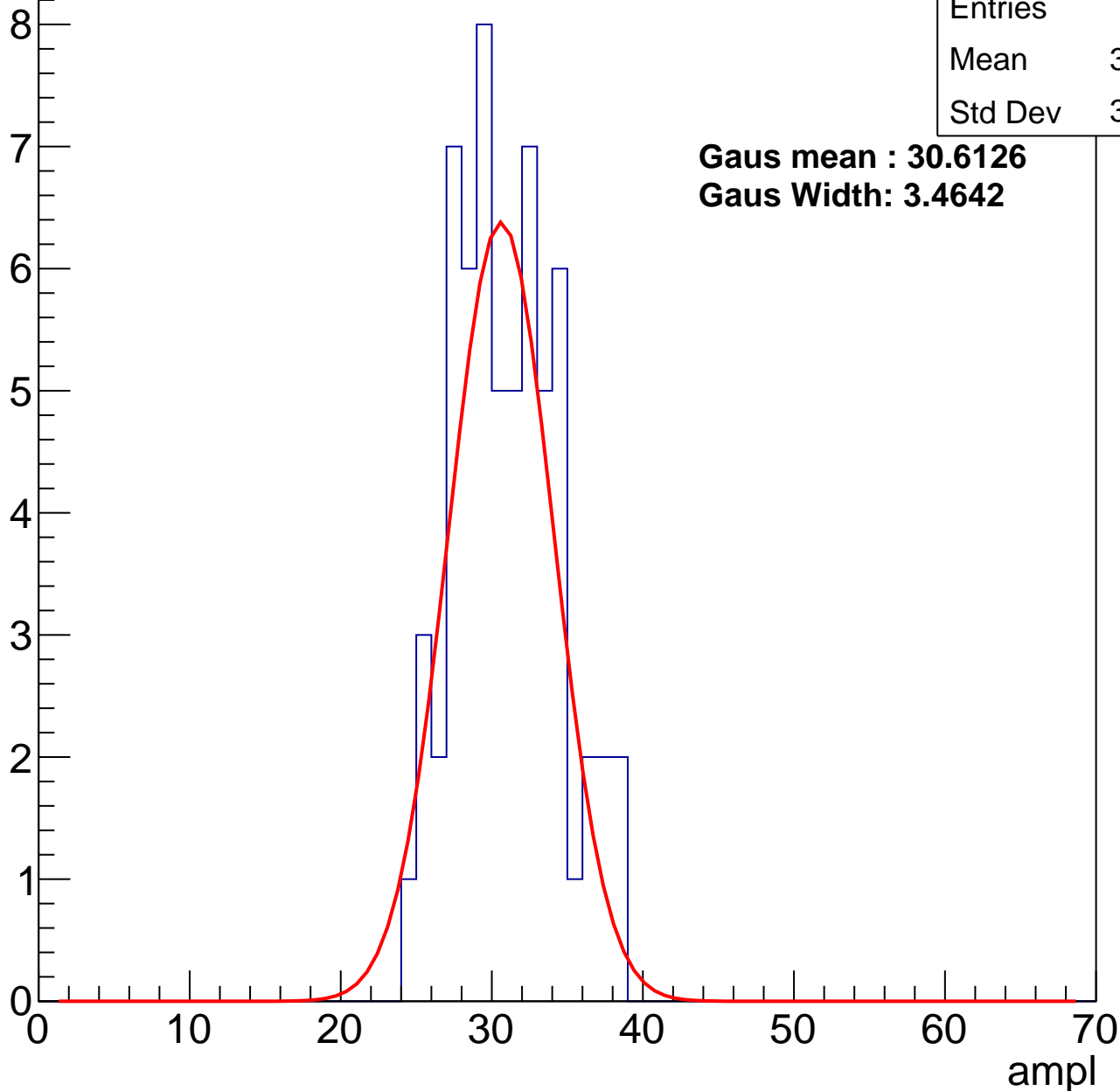
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	30.56
Std Dev	3.396

**Gaus mean : 30.6126**

**Gaus Width: 3.4642**



# B1L103S, U11-ch49, adc1

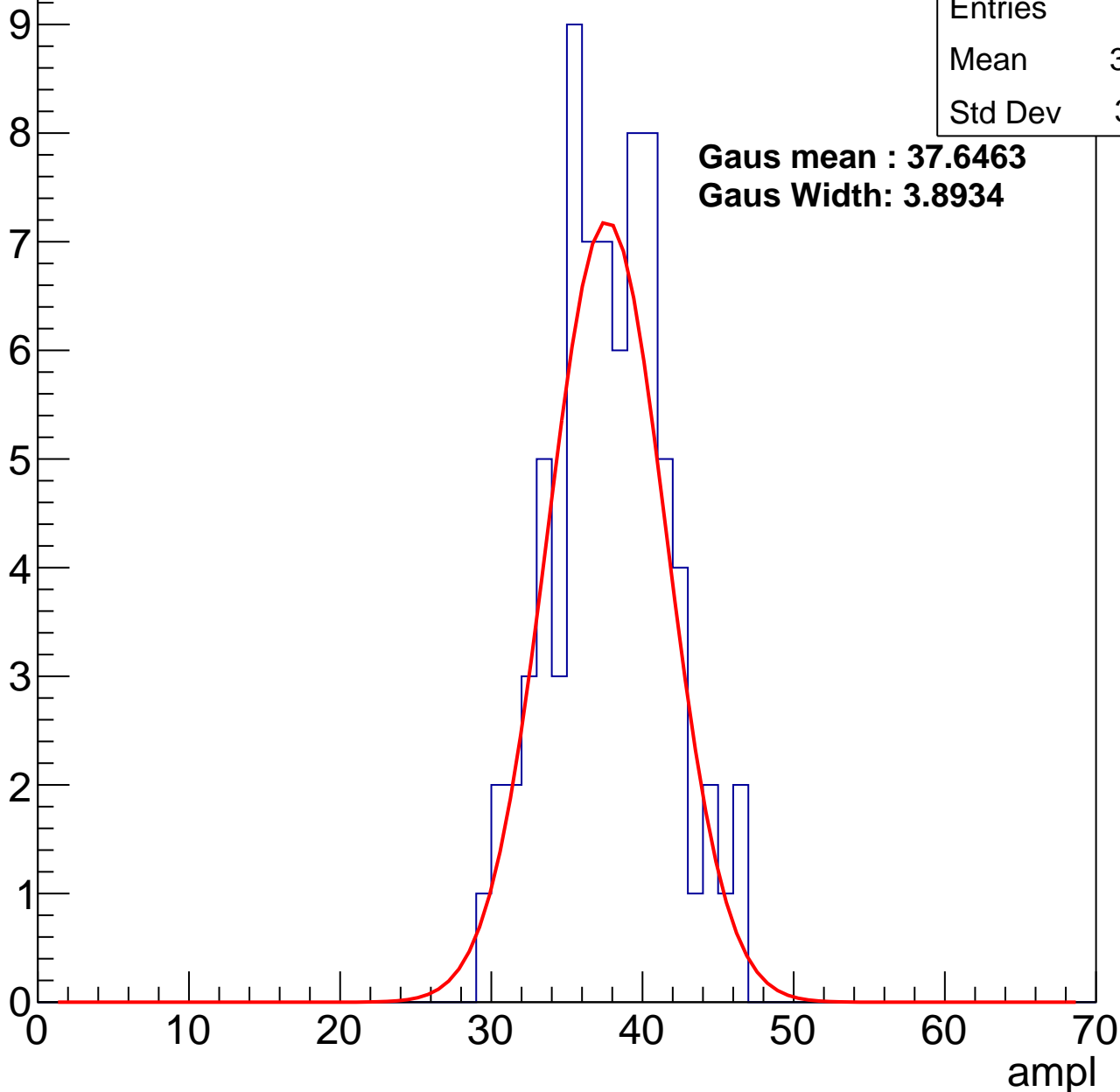
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	76
Mean	37.38
Std Dev	3.801

**Gaus mean : 37.6463**

**Gaus Width: 3.8934**



# B1L103S, U11-ch49, adc2

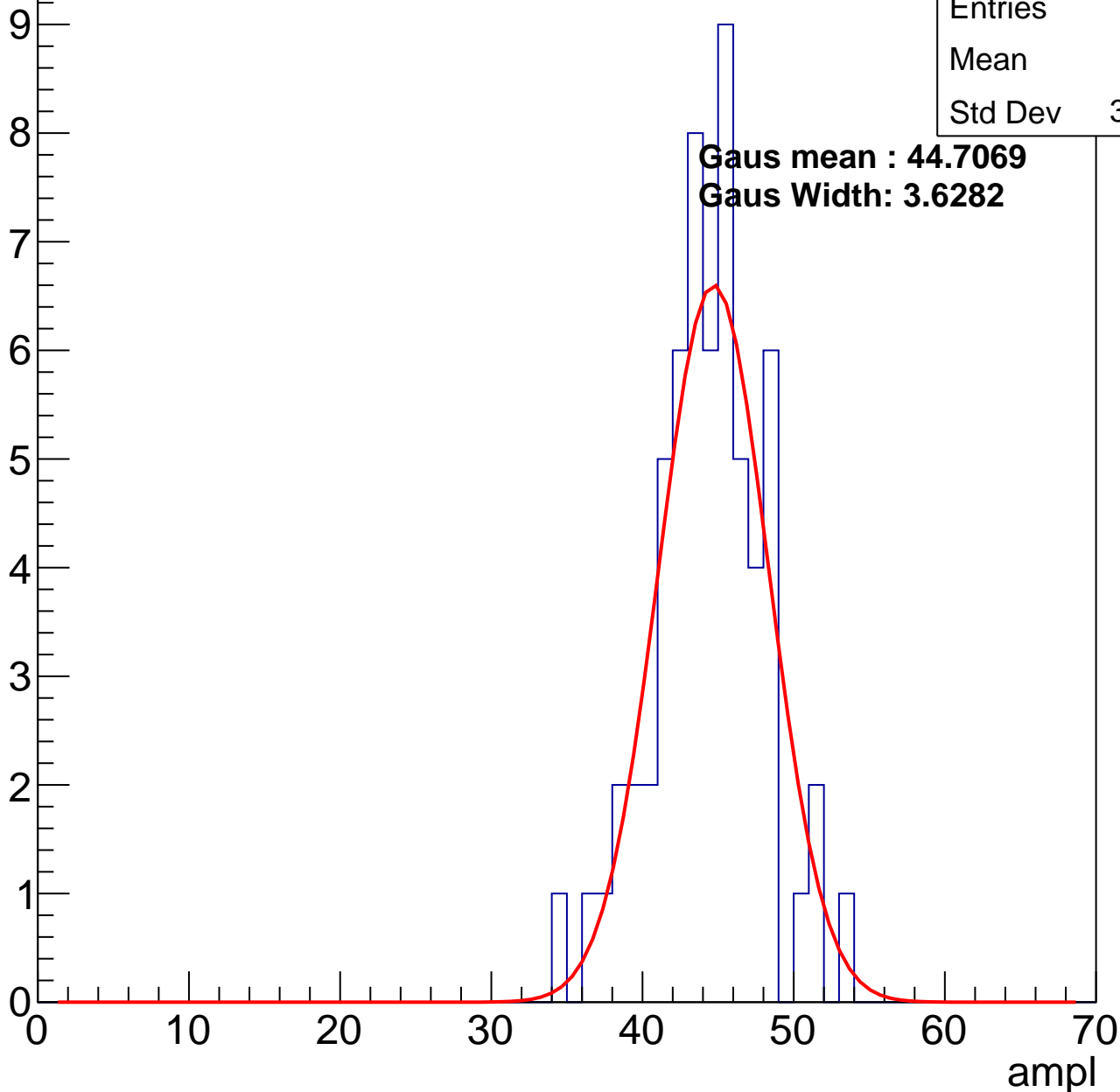
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	43.9
Std Dev	3.635

**Gaus mean : 44.7069**

**Gaus Width: 3.6282**



# B1L103S, U11-ch49, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	72
Mean	50.93
Std Dev	3.477

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

1

2

3

4

5

6

7

8

9

10

11

12

13

14

15

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17

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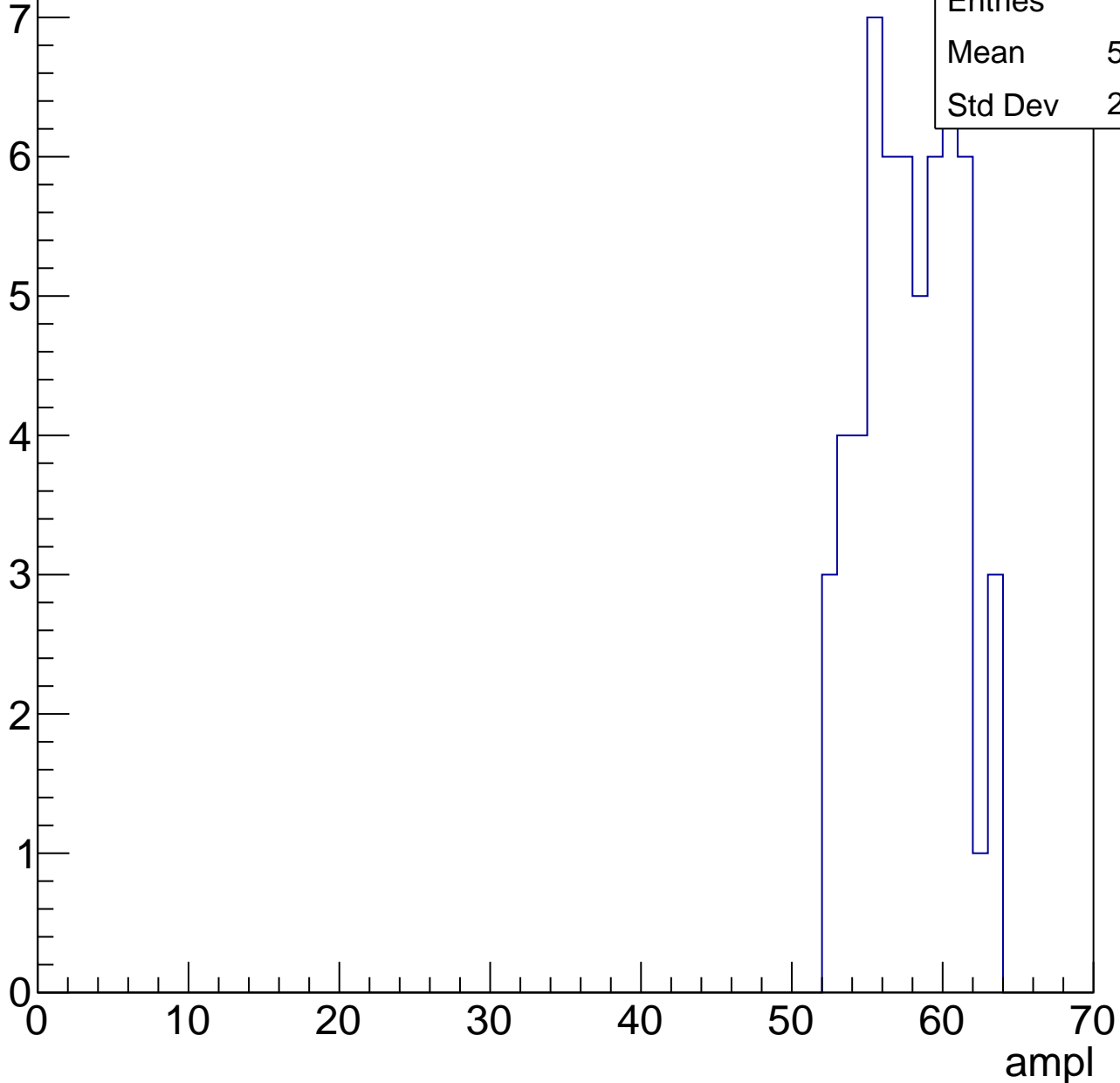
320

# B1L103S, U11-ch49, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	58
Mean	57.38
Std Dev	2.999

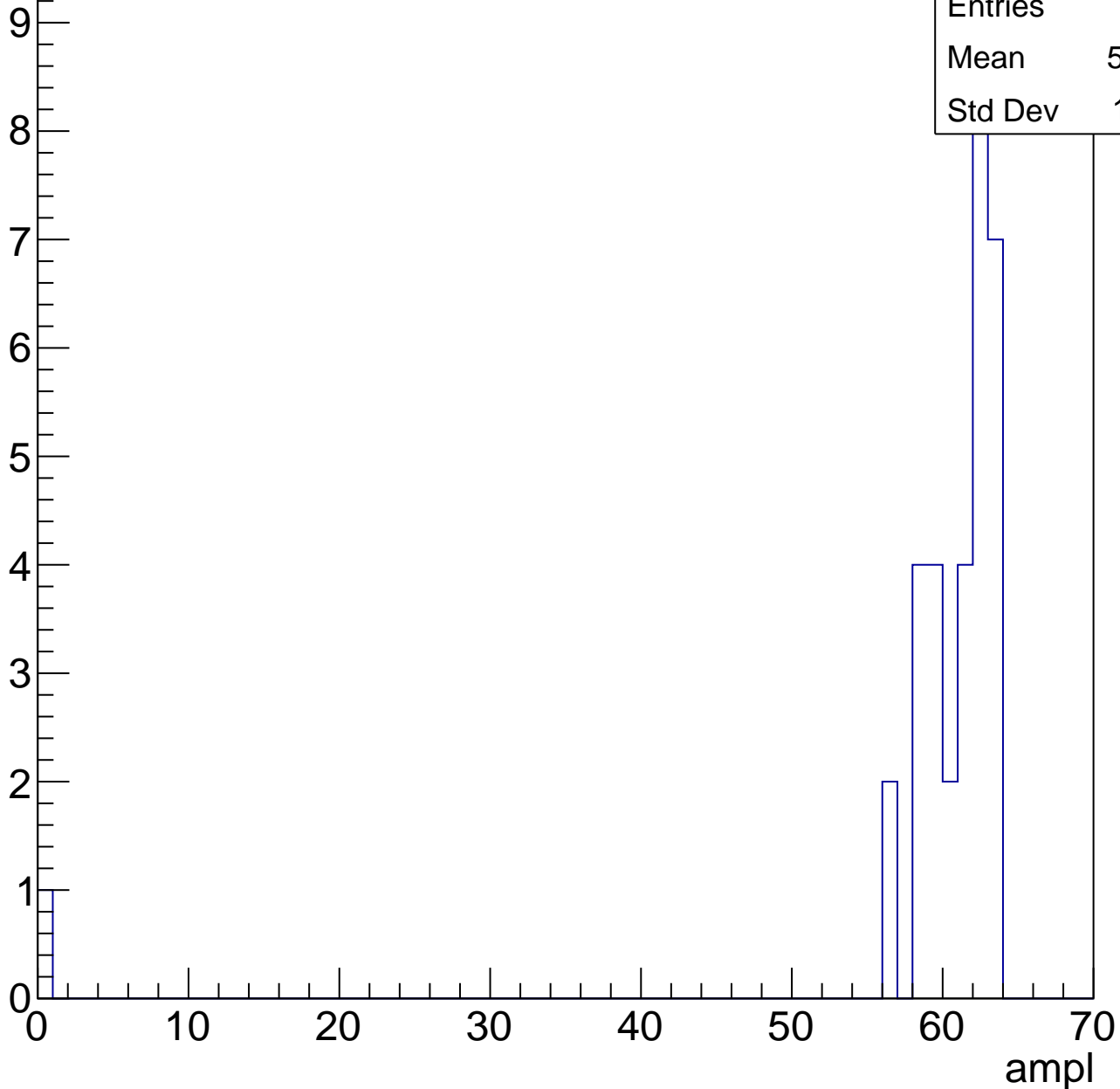


# B1L103S, U11-ch49, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	33
Mean	58.88
Std Dev	10.61



# B1L103S, U11-ch49, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0



# B1L103S, U11-ch49, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	3
Mean	7.667
Std Dev	10.84

# B1L103S, U11-ch50, adc0

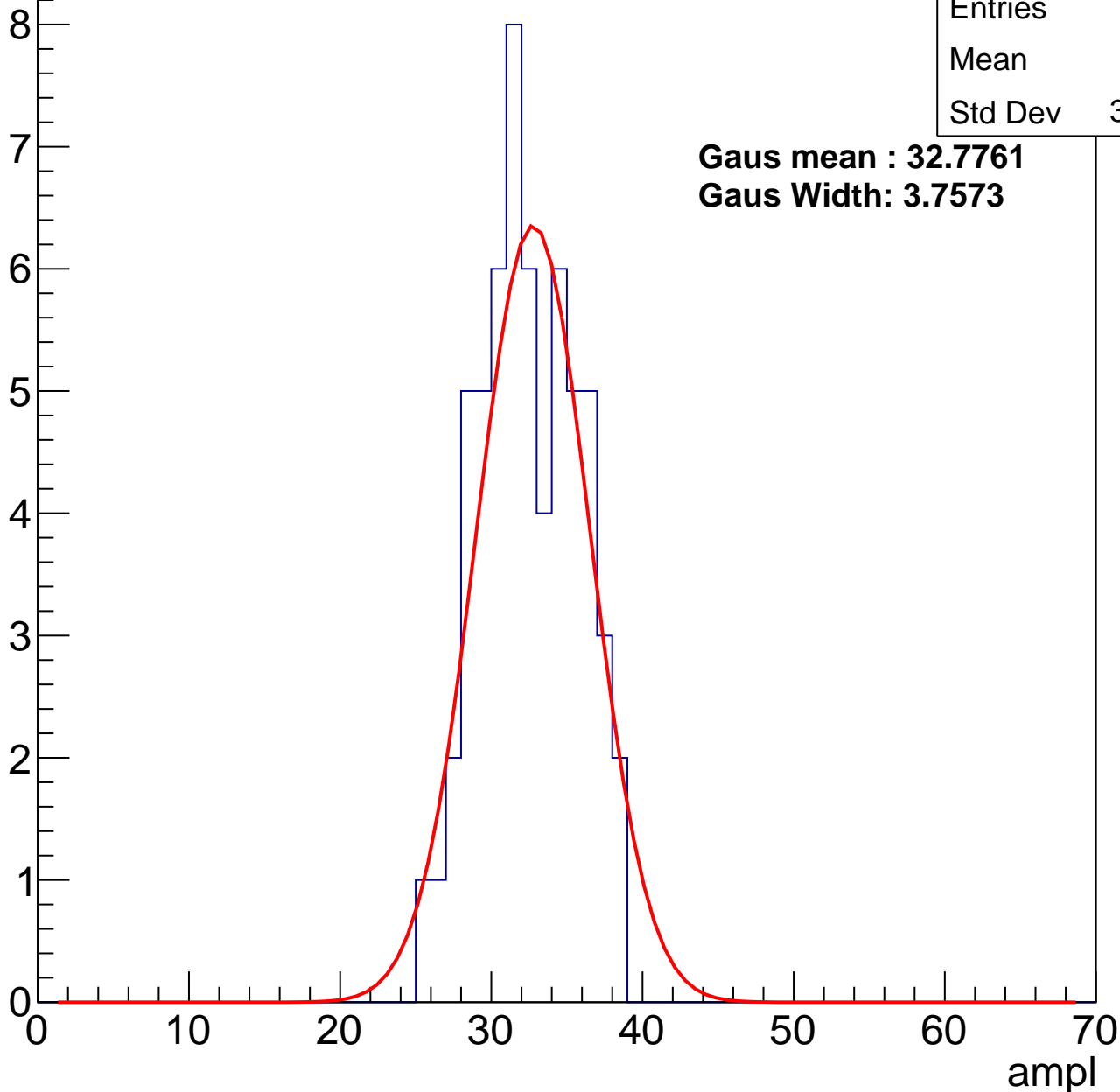
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	59
Mean	32
Std Dev	3.168

**Gaus mean : 32.7761**

**Gaus Width: 3.7573**



# B1L103S, U11-ch50, adc1

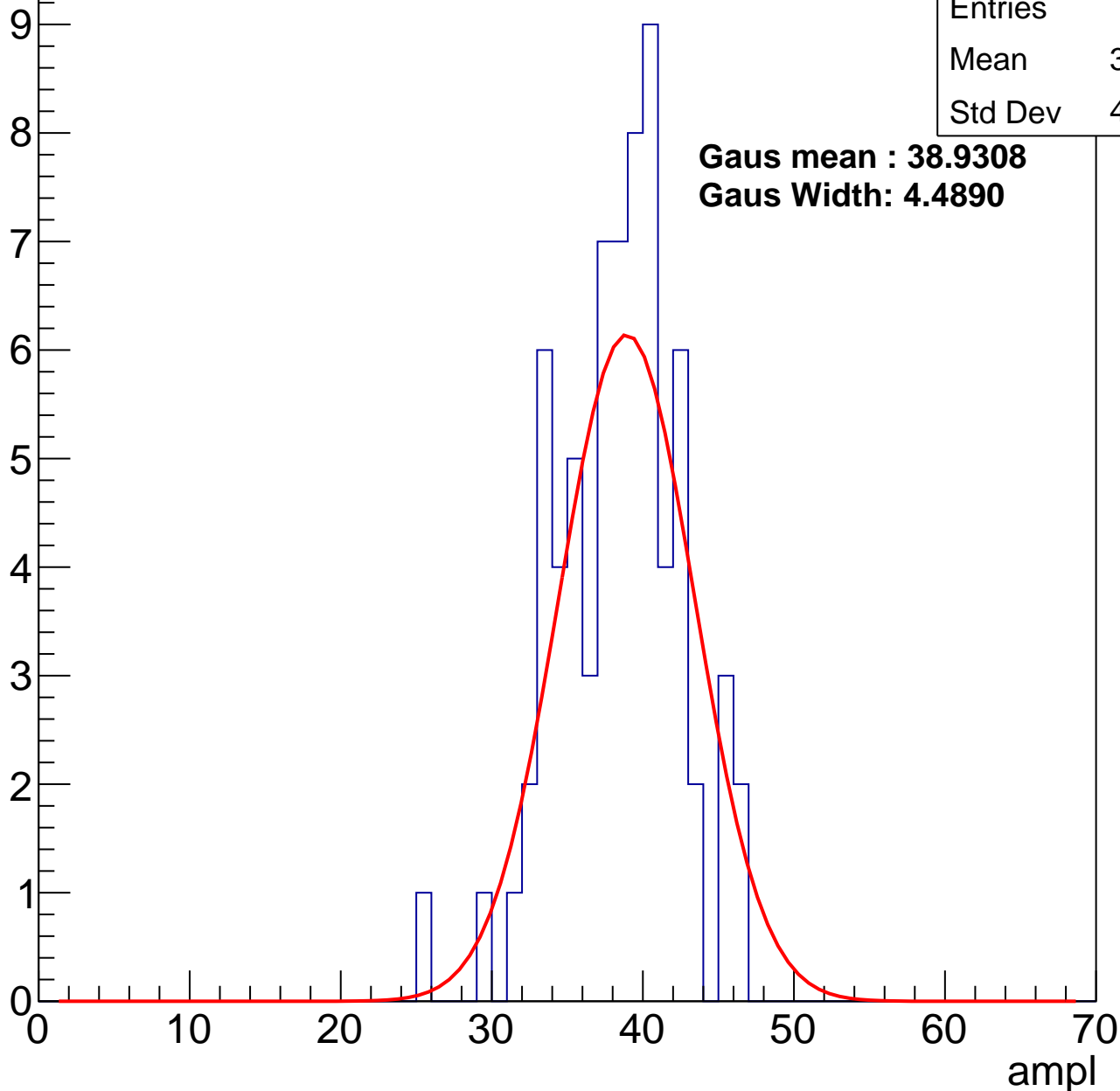
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	71
Mean	37.92
Std Dev	4.024

**Gaus mean : 38.9308**

**Gaus Width: 4.4890**



# B1L103S, U11-ch50, adc2

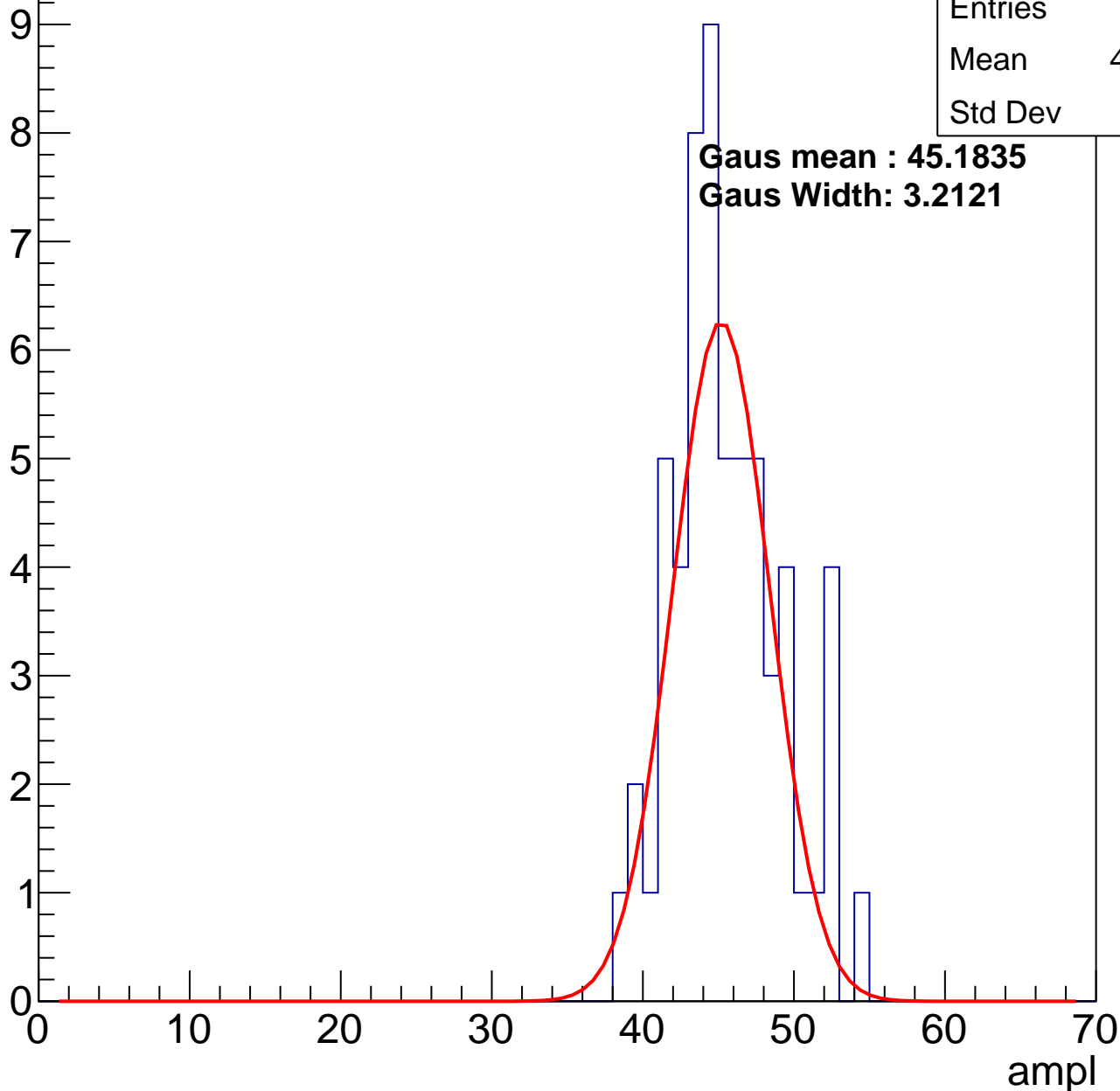
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	59
Mean	45.12
Std Dev	3.58

**Gaus mean : 45.1835**

**Gaus Width: 3.2121**

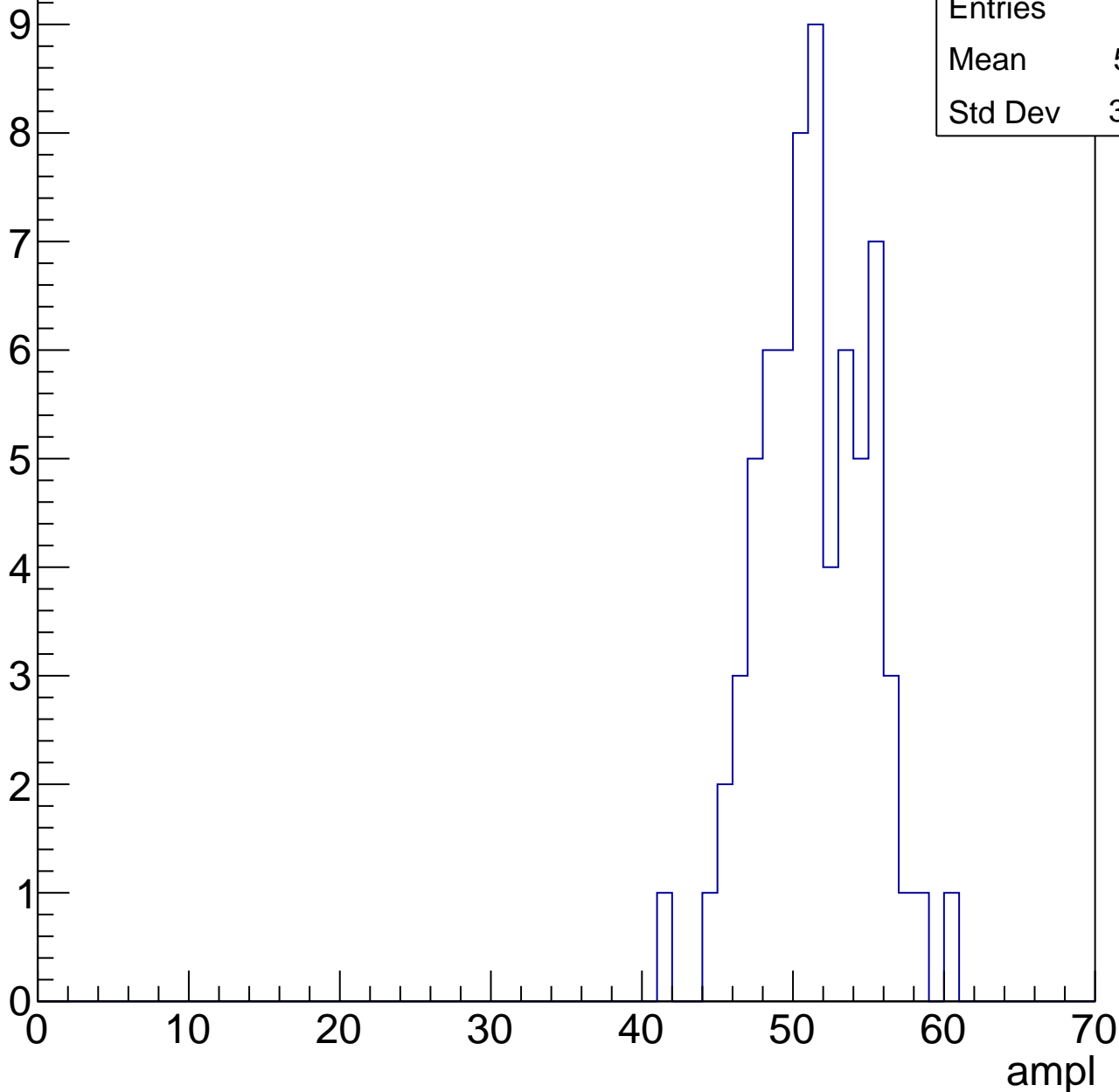


# B1L103S, U11-ch50, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

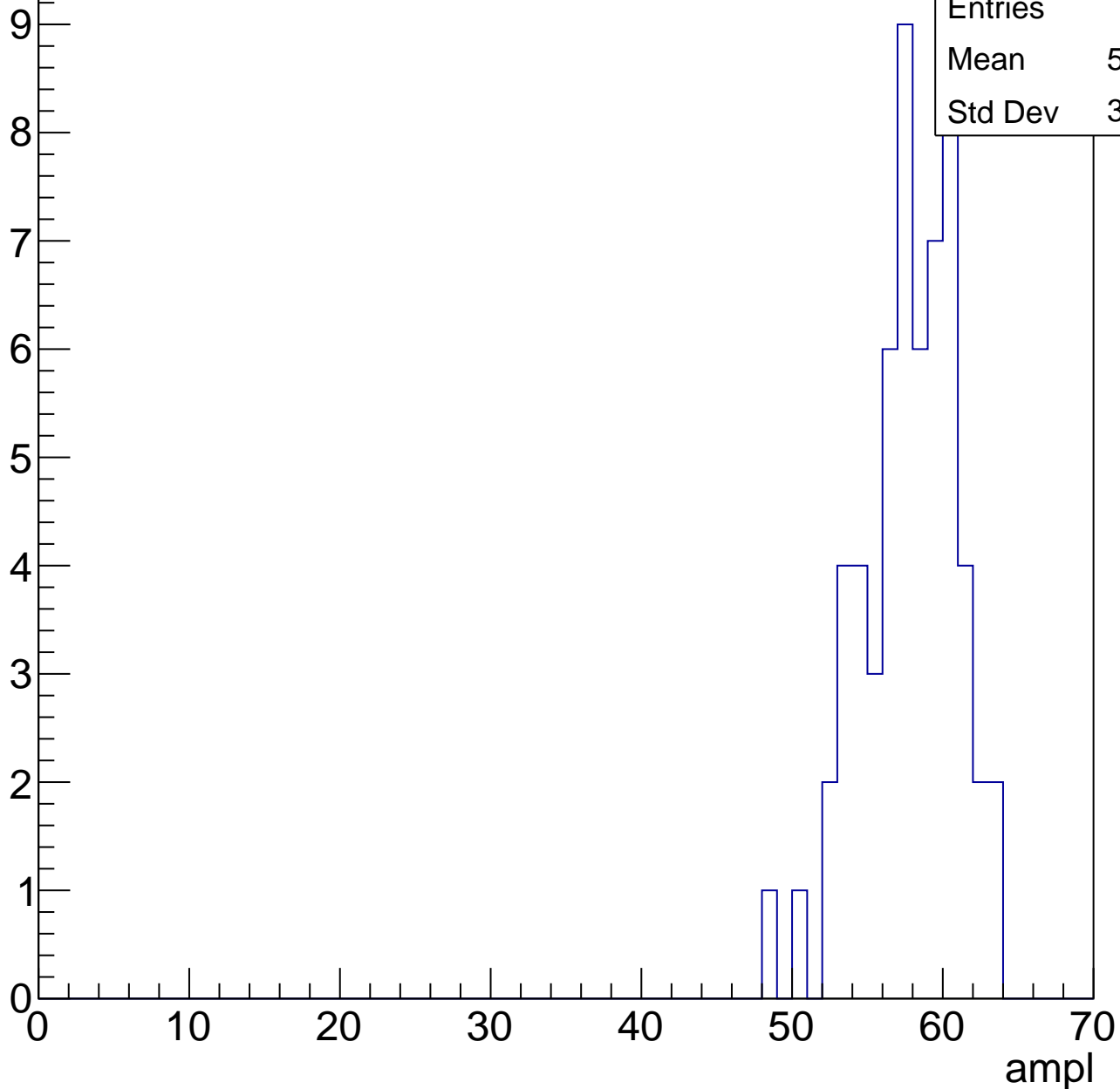
Entries	69
Mean	50.91
Std Dev	3.586



# B1L103S, U11-ch50, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

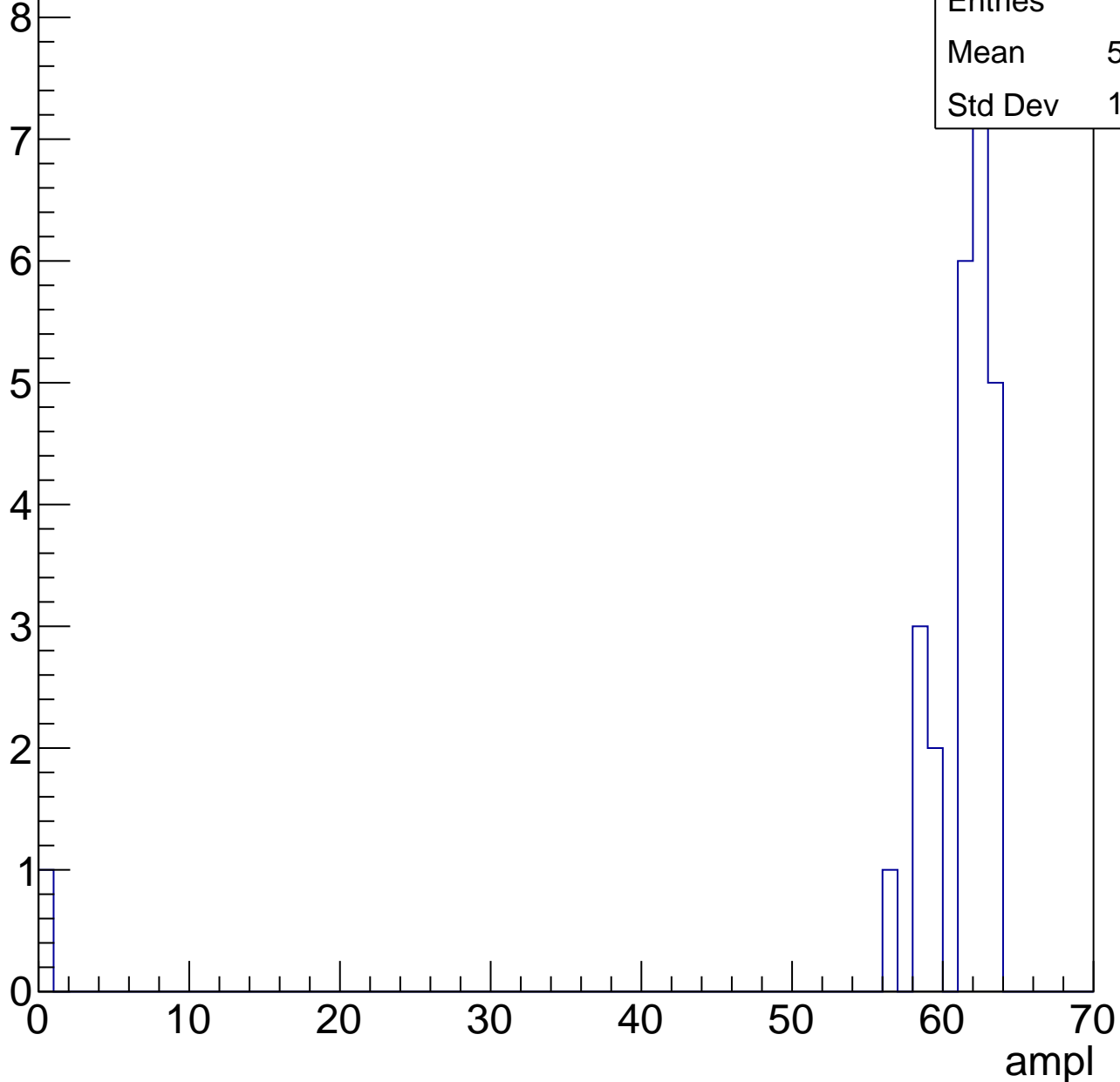


# B1L103S, U11-ch50, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

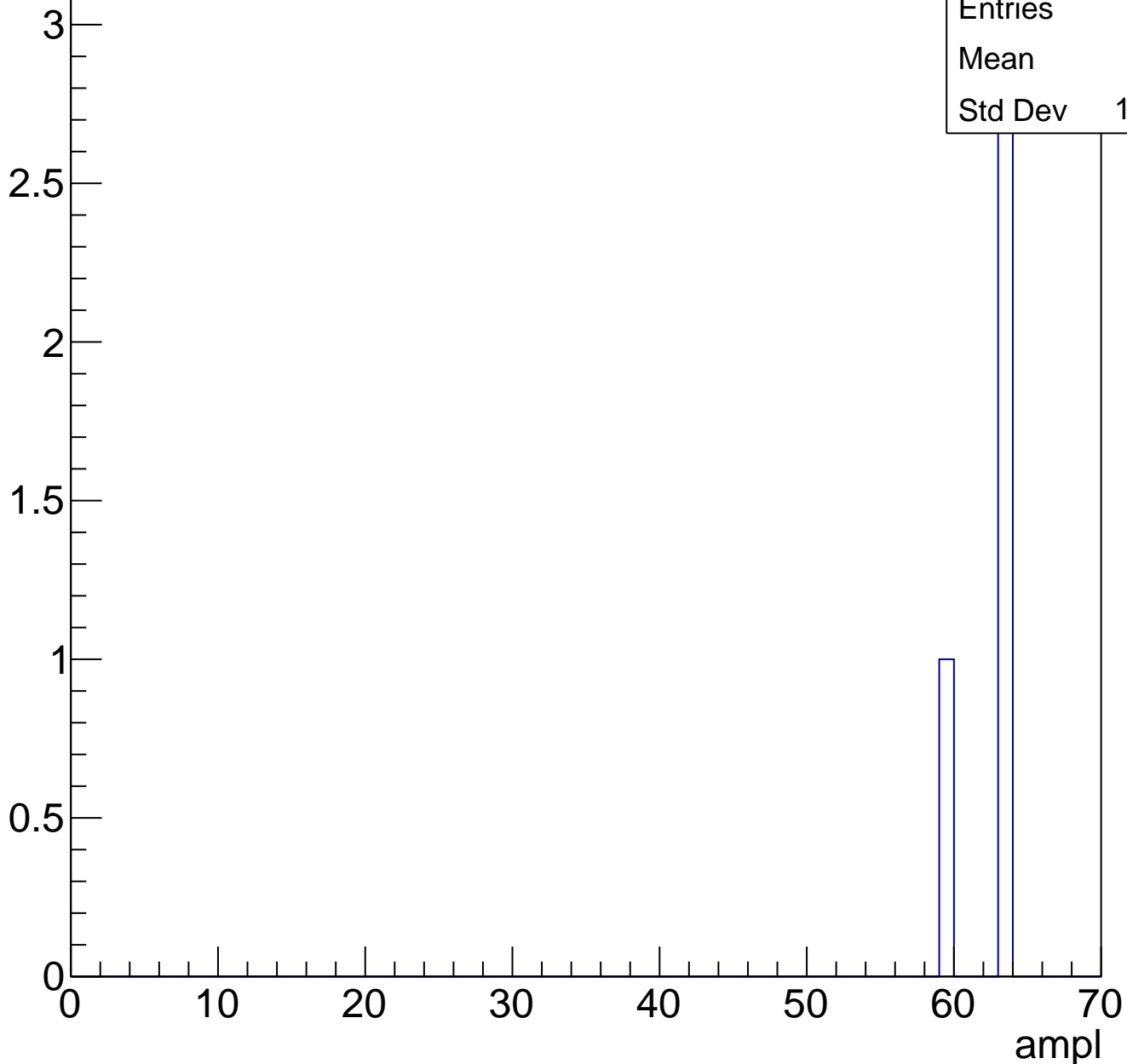
Entries	26
Mean	58.65
Std Dev	11.87



# B1L103S, U11-ch50, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U11-ch50, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U11-ch51, adc0

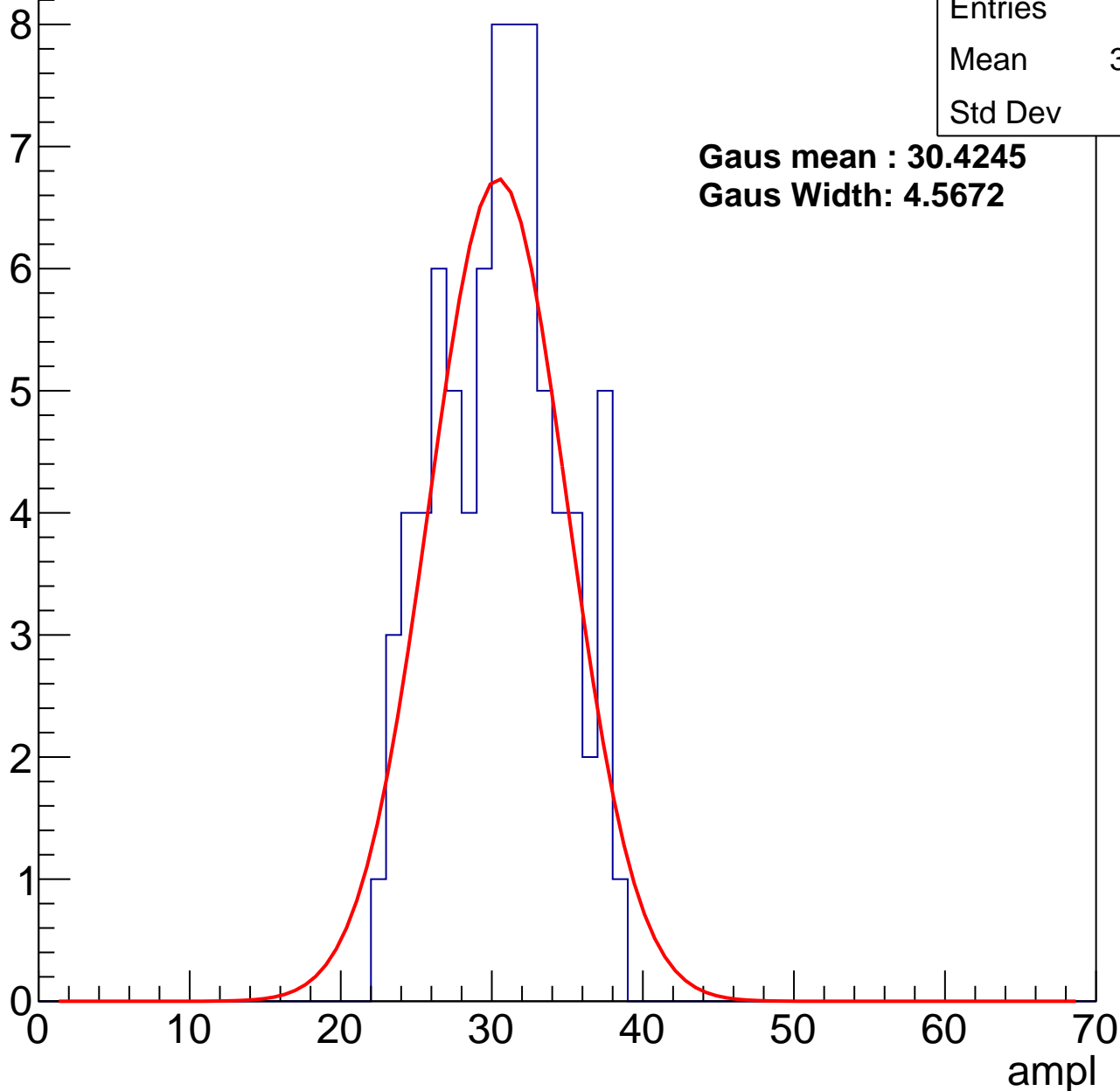
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	78
Mean	30.05
Std Dev	4

**Gaus mean : 30.4245**

**Gaus Width: 4.5672**



# B1L103S, U11-ch51, adc1

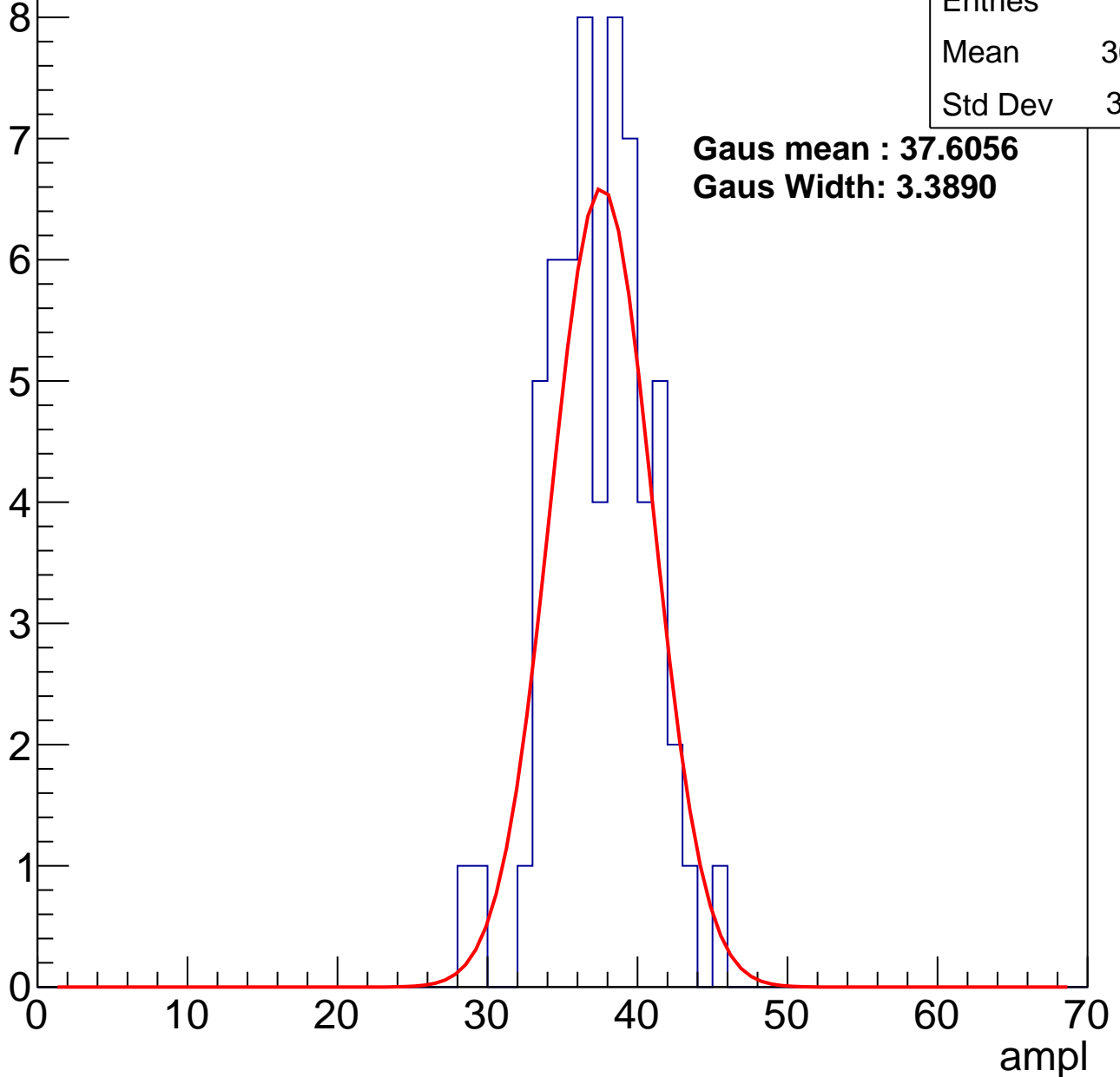
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	60
Mean	36.97
Std Dev	3.261

**Gaus mean : 37.6056**

**Gaus Width: 3.3890**



# B1L103S, U11-ch51, adc2

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	77
Mean	44.22
Std Dev	3.606

**Gaus mean : 44.7536**

**Gaus Width: 3.5170**

10

8

6

4

2

0

0

2

4

6

8

10

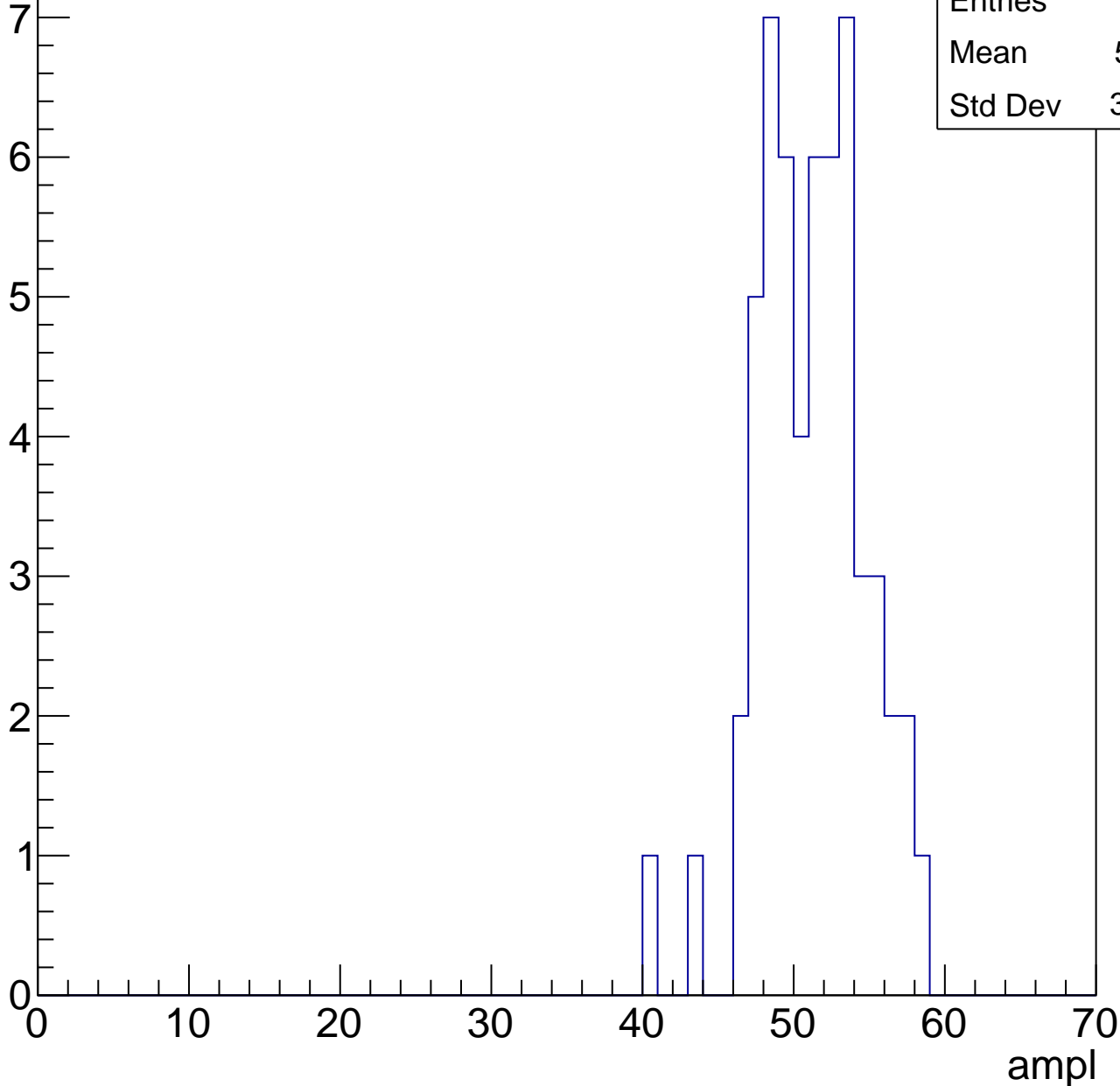
ampl

# B1L103S, U11-ch51, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	56
Mean	50.71
Std Dev	3.488

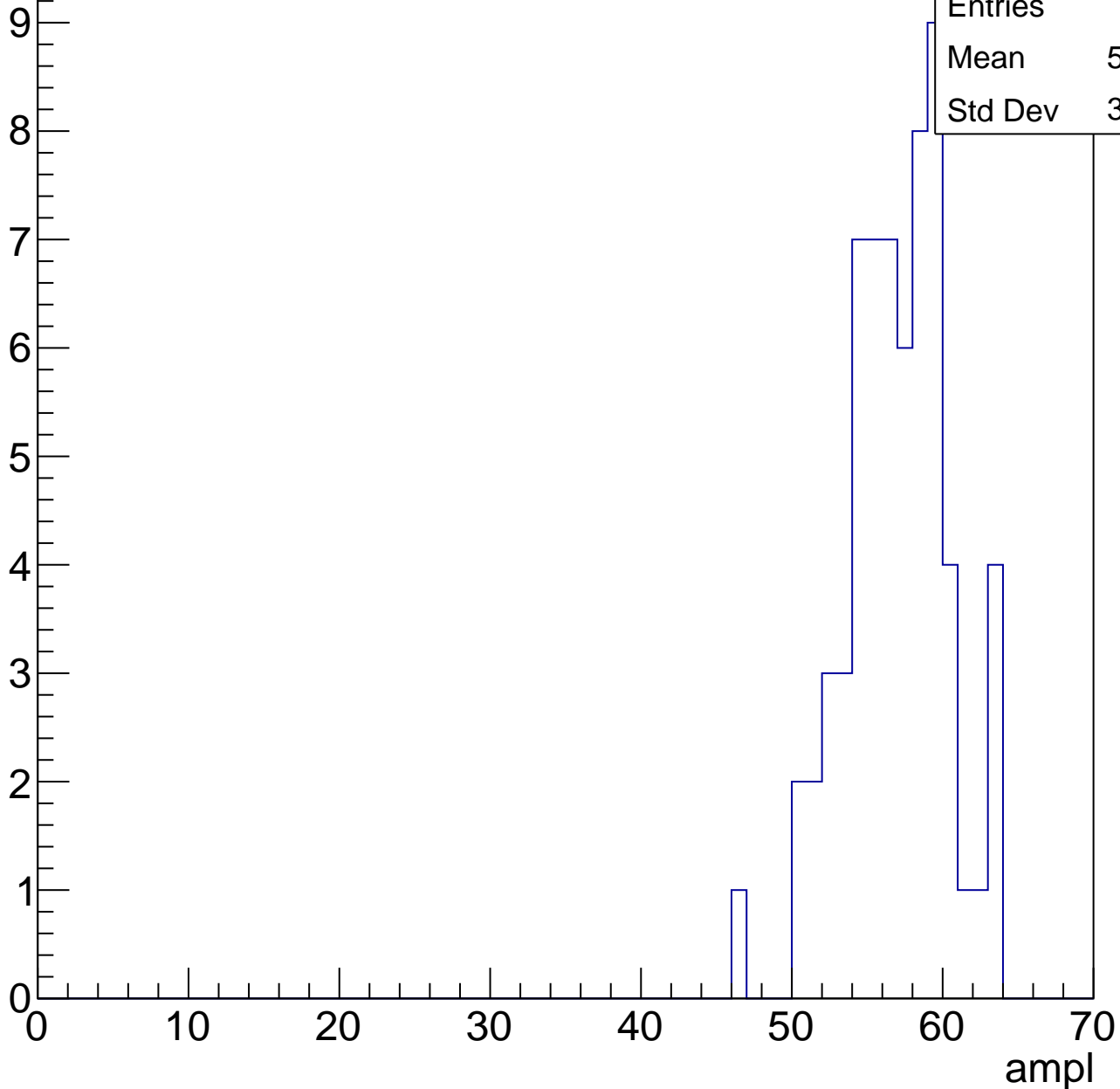


# B1L103S, U11-ch51, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	56.46
Std Dev	3.415

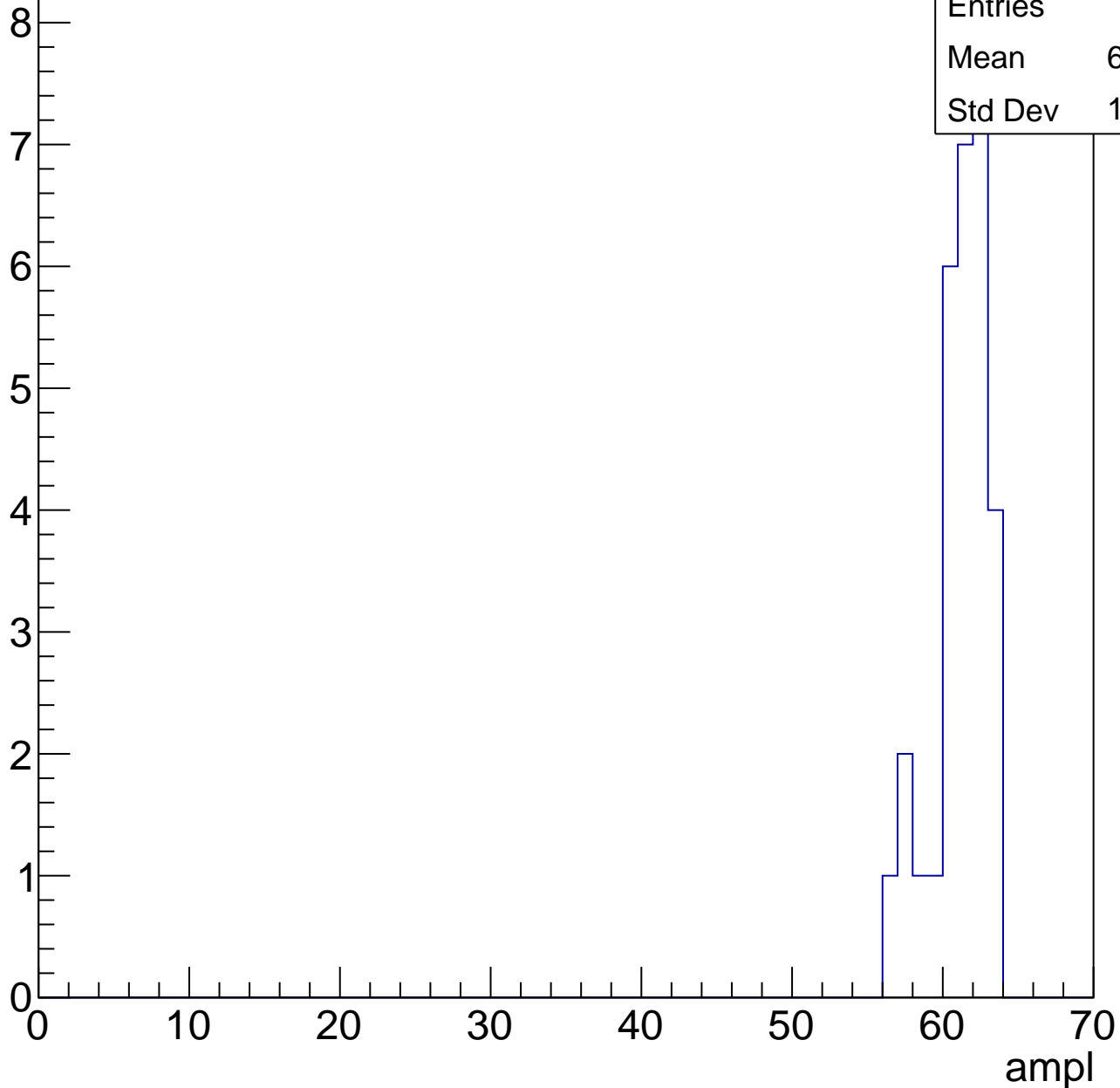


# B1L103S, U11-ch51, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

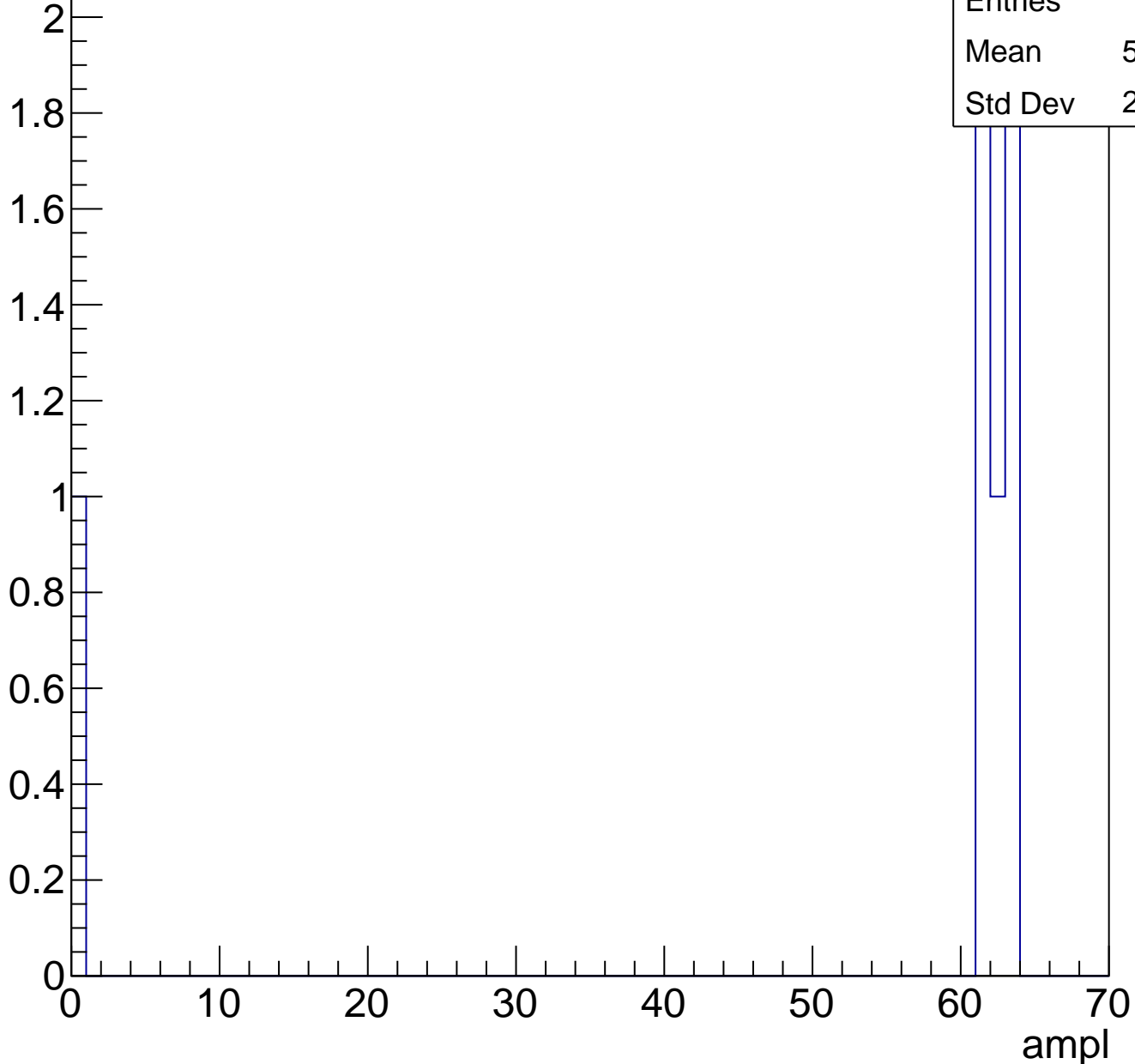
Entries	30
Mean	60.73
Std Dev	1.806



# B1L103S, U11-ch51, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U11-ch51, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L103S, U11-ch52, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	83
Mean	29.78
Std Dev	4.914

**Gaus mean : 30.5944**

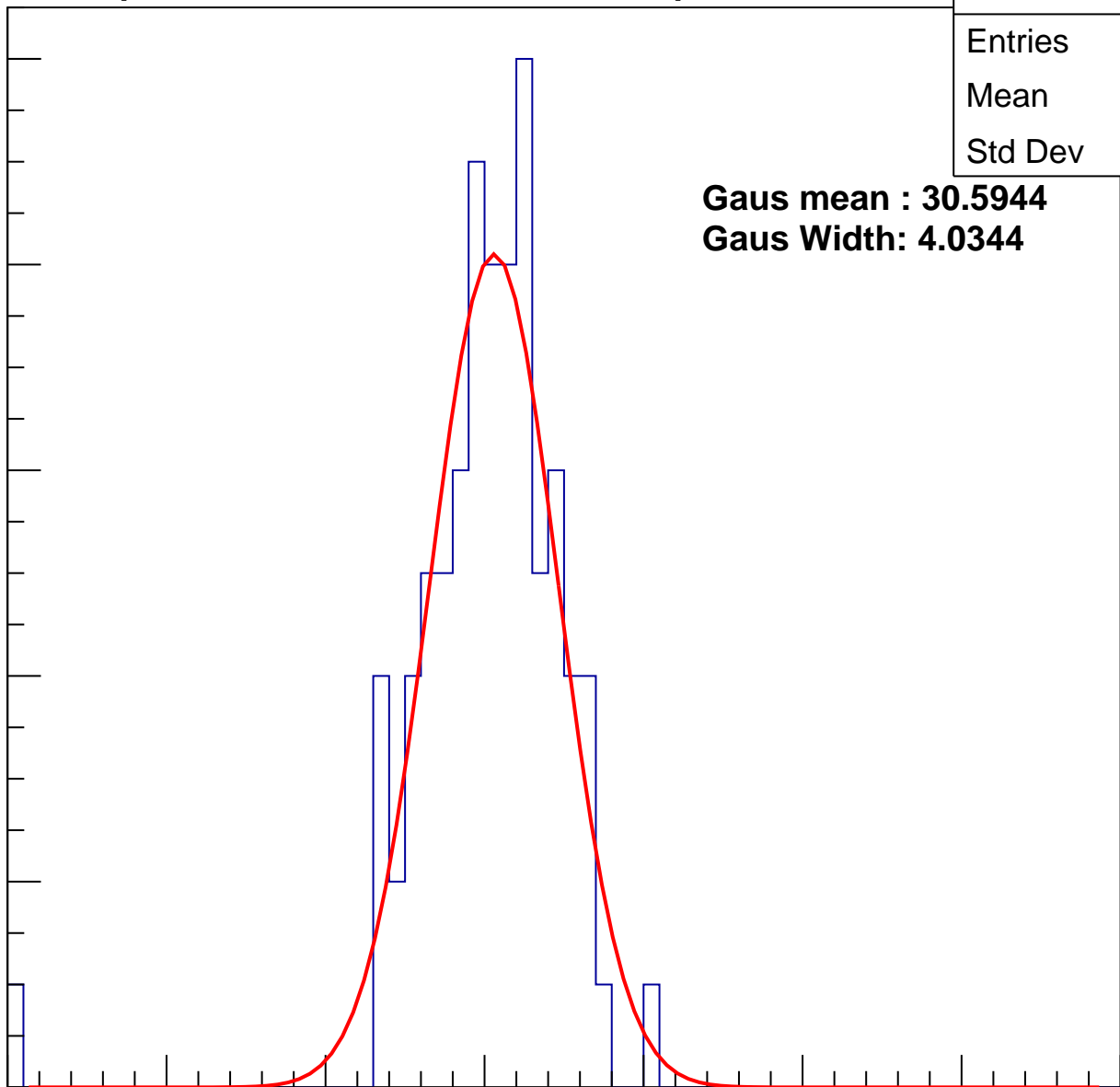
**Gaus Width: 4.0344**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



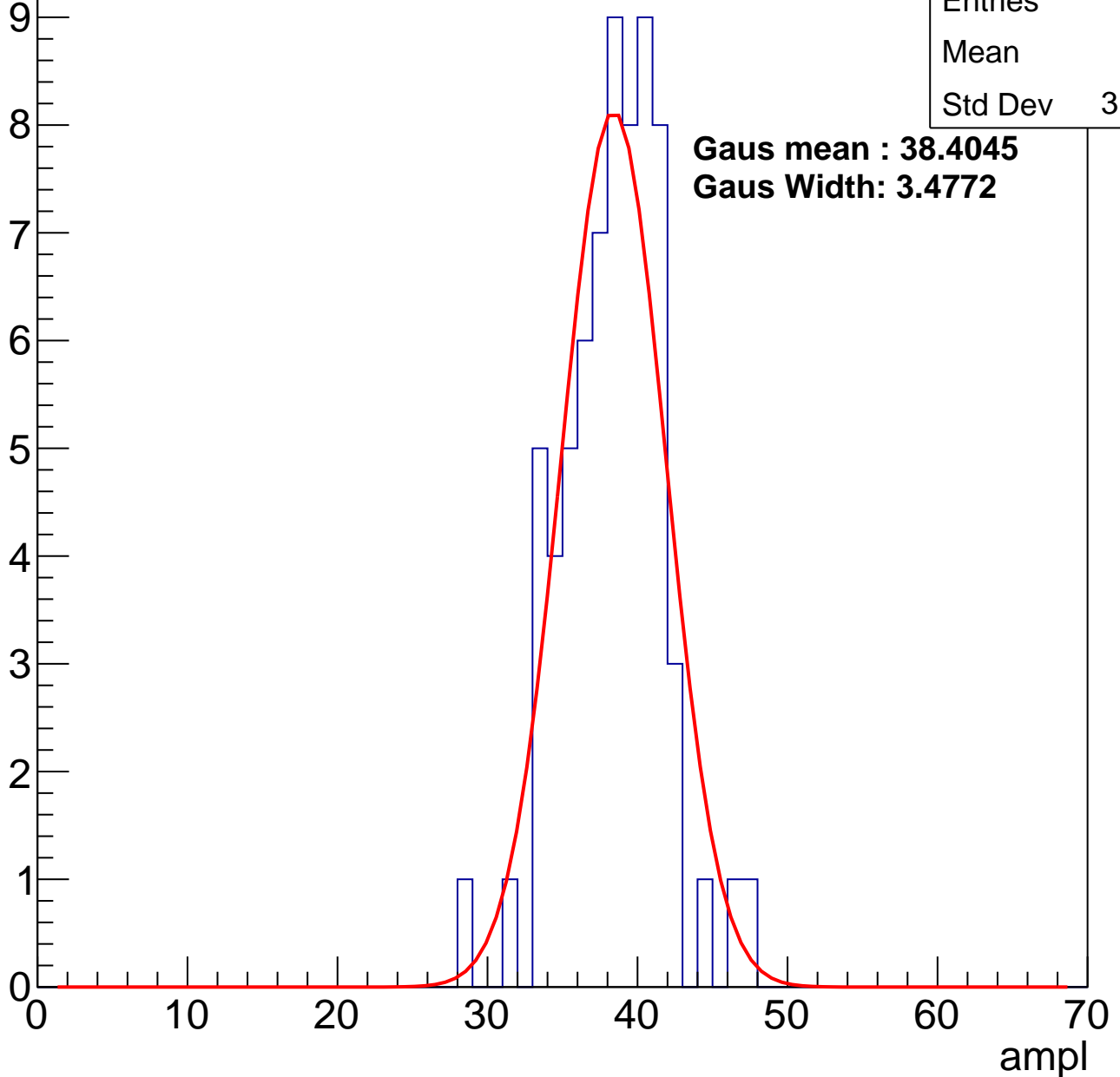
# B1L103S, U11-ch52, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	69
Mean	37.9
Std Dev	3.315

**Gaus mean : 38.4045**  
**Gaus Width: 3.4772**



# B1L103S, U11-ch52, adc2

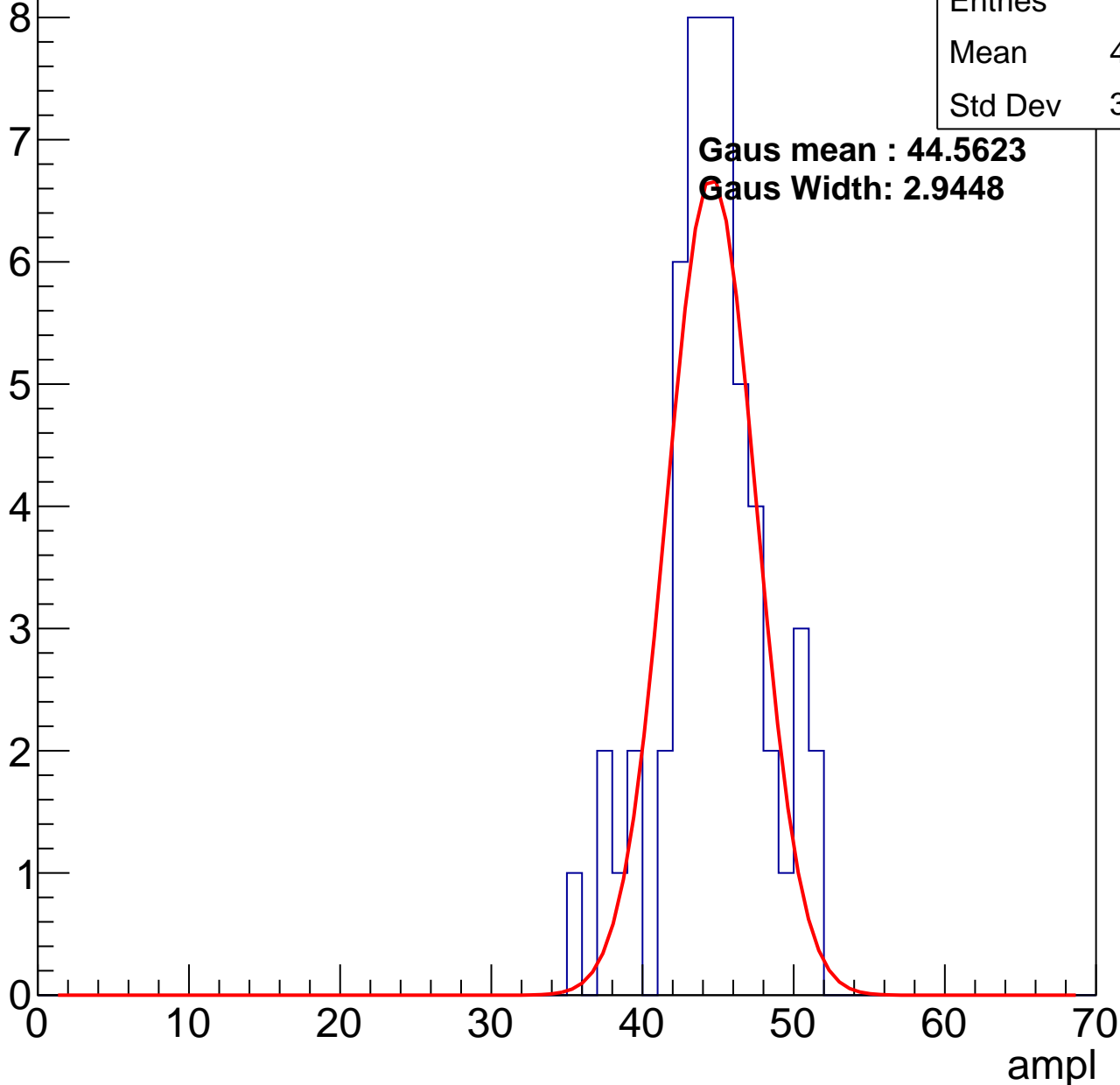
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	55
Mean	44.18
Std Dev	3.412

Gaus mean : 44.5623

Gaus Width: 2.9448

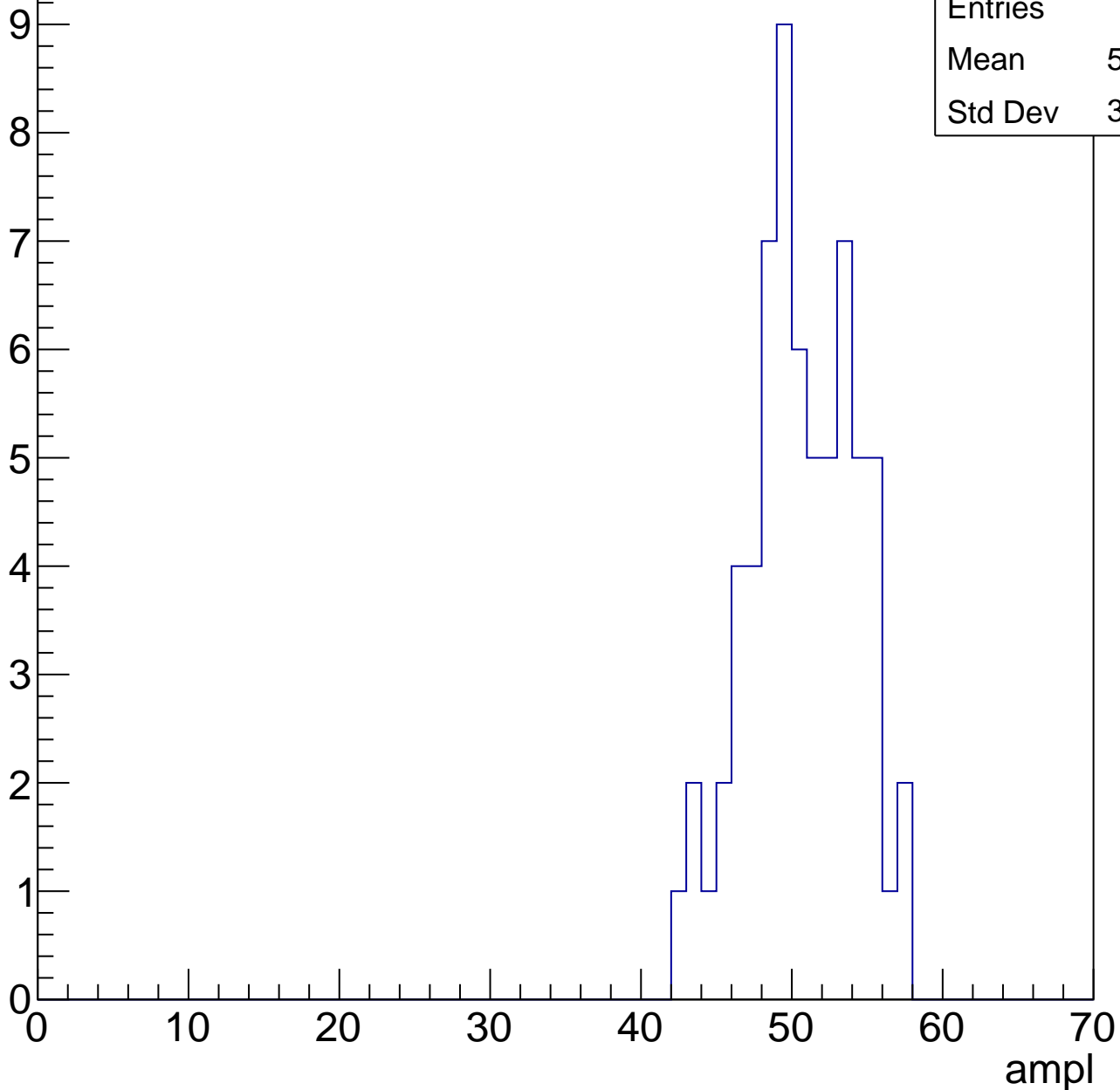


# B1L103S, U11-ch52, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	50.18
Std Dev	3.503

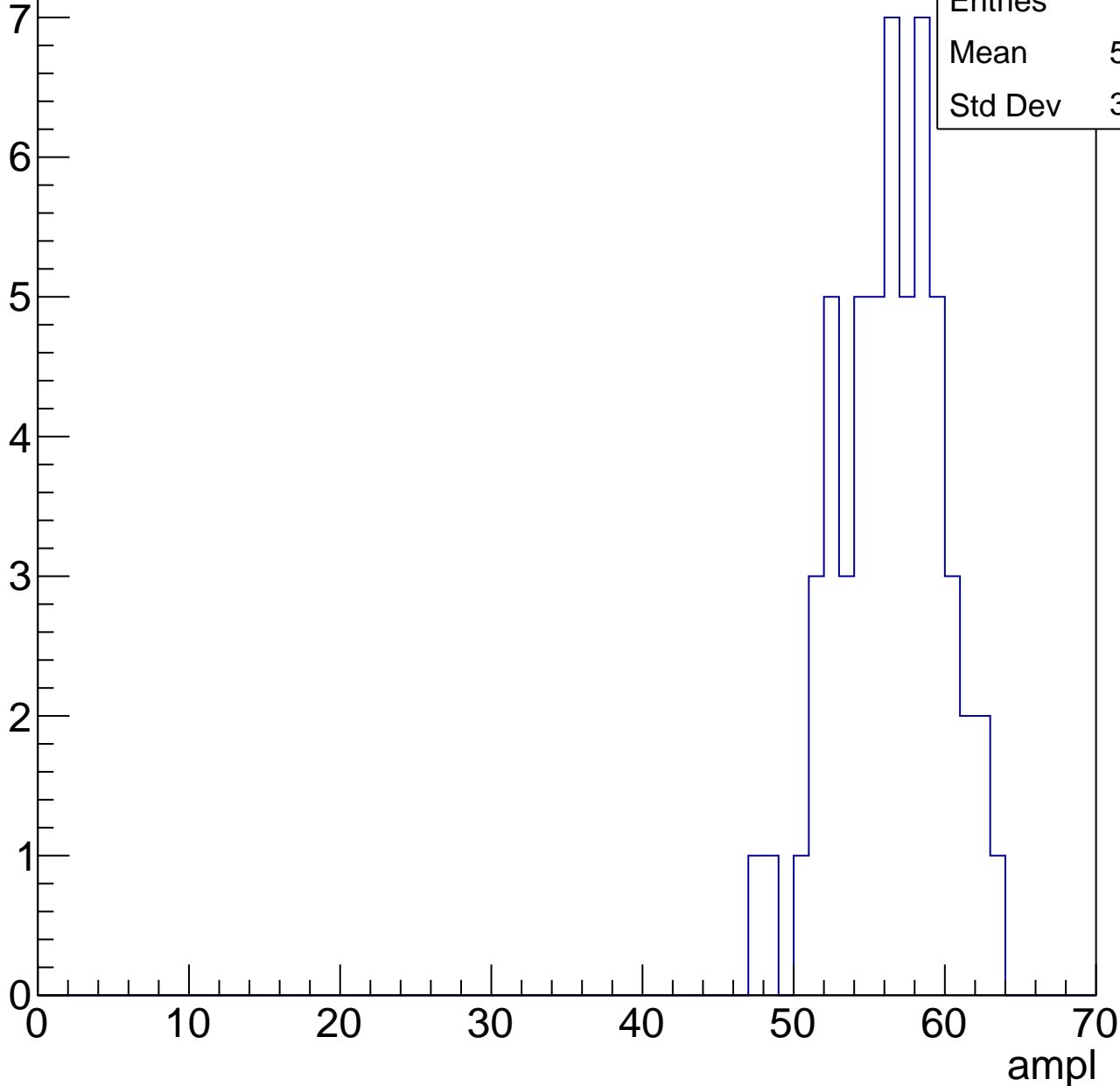


# B1L103S, U11-ch52, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	56
Mean	55.88
Std Dev	3.495

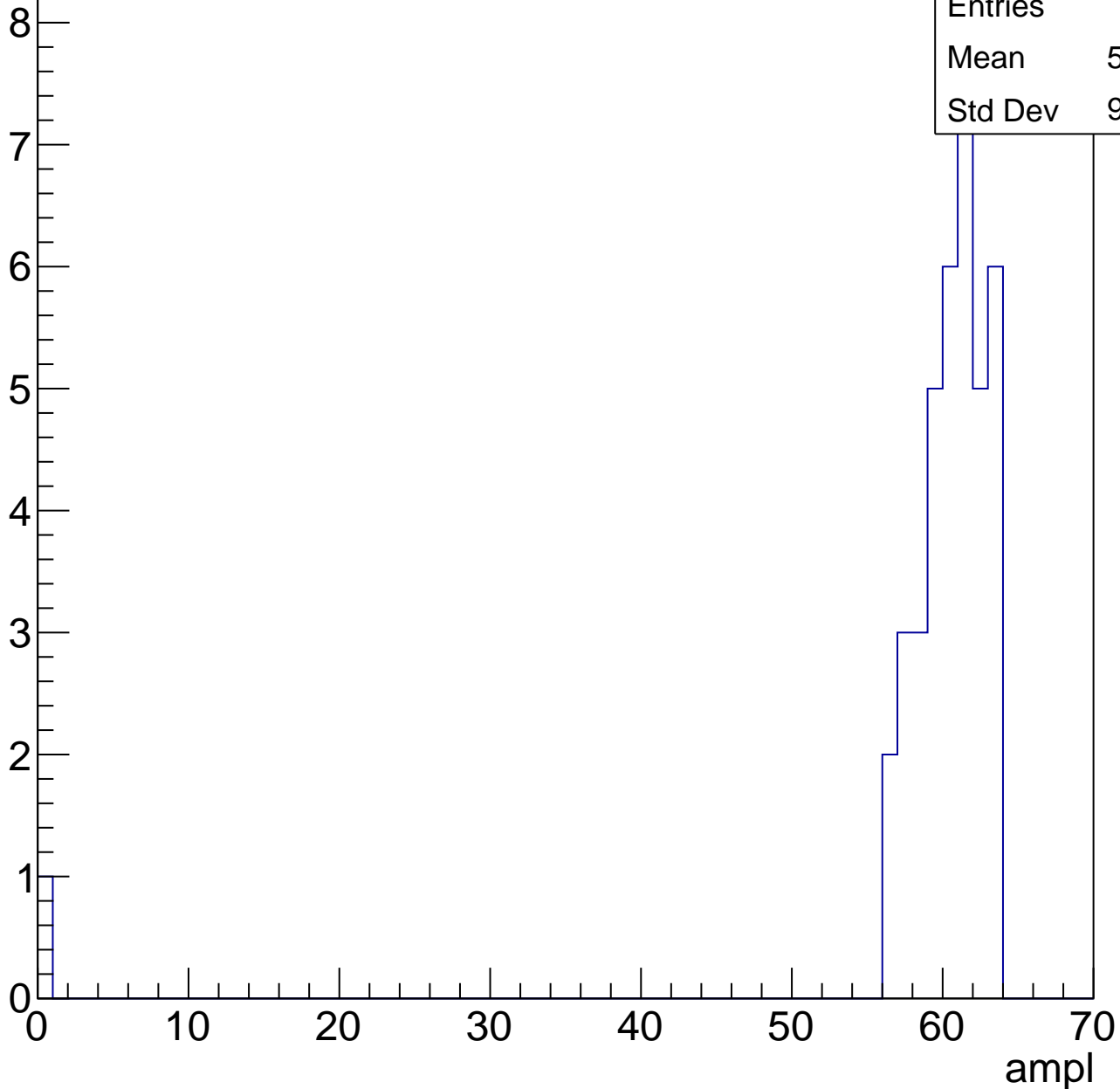


# B1L103S, U11-ch52, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	39
Mean	58.67
Std Dev	9.725



# B1L103S, U11-ch52, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U11-ch52, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L103S, U11-ch53, adc0

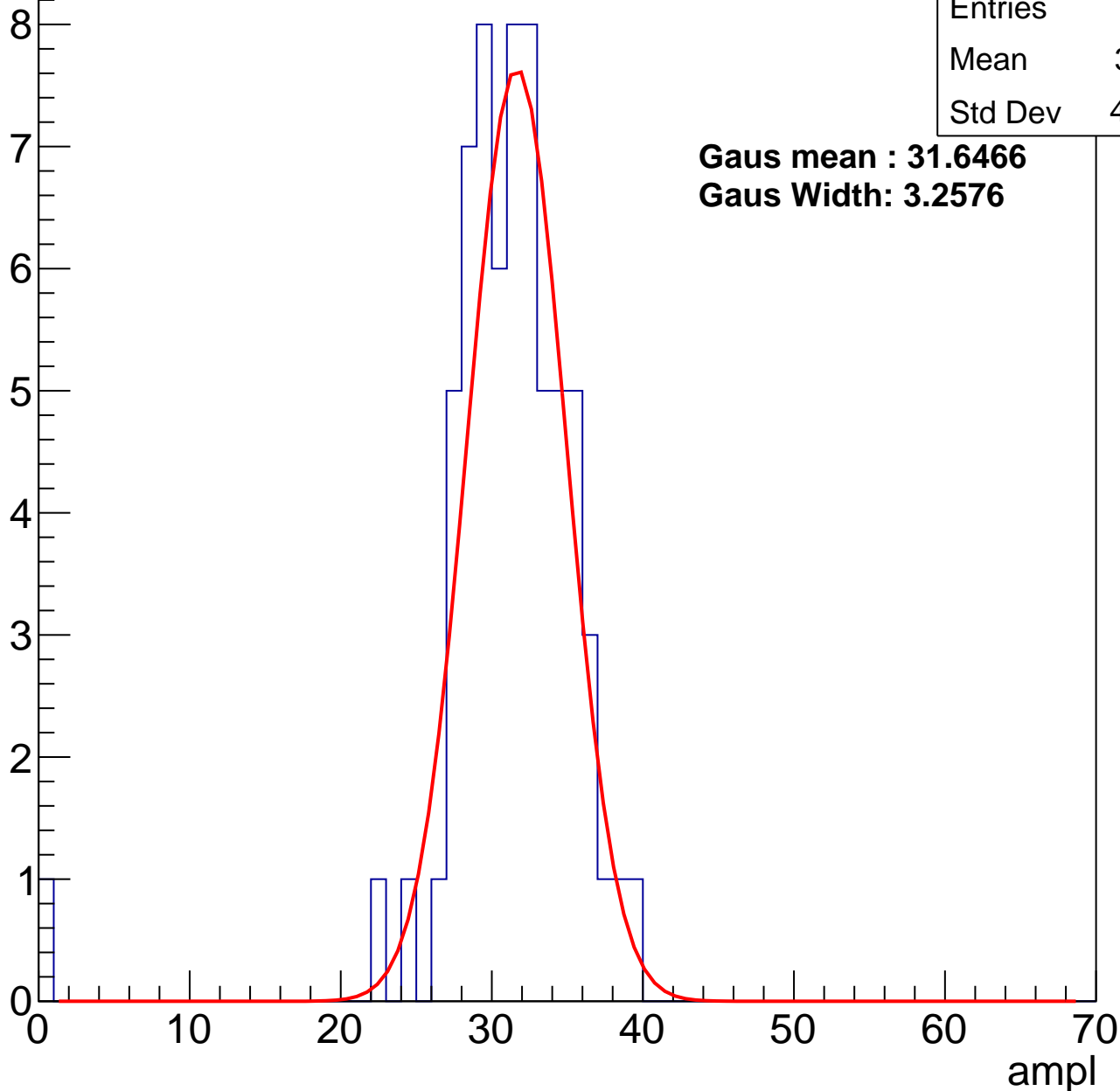
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	30.61
Std Dev	4.983

**Gaus mean : 31.6466**

**Gaus Width: 3.2576**



# B1L103S, U11-ch53, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	85
Mean	38.71
Std Dev	3.862

**Gaus mean : 38.7455**

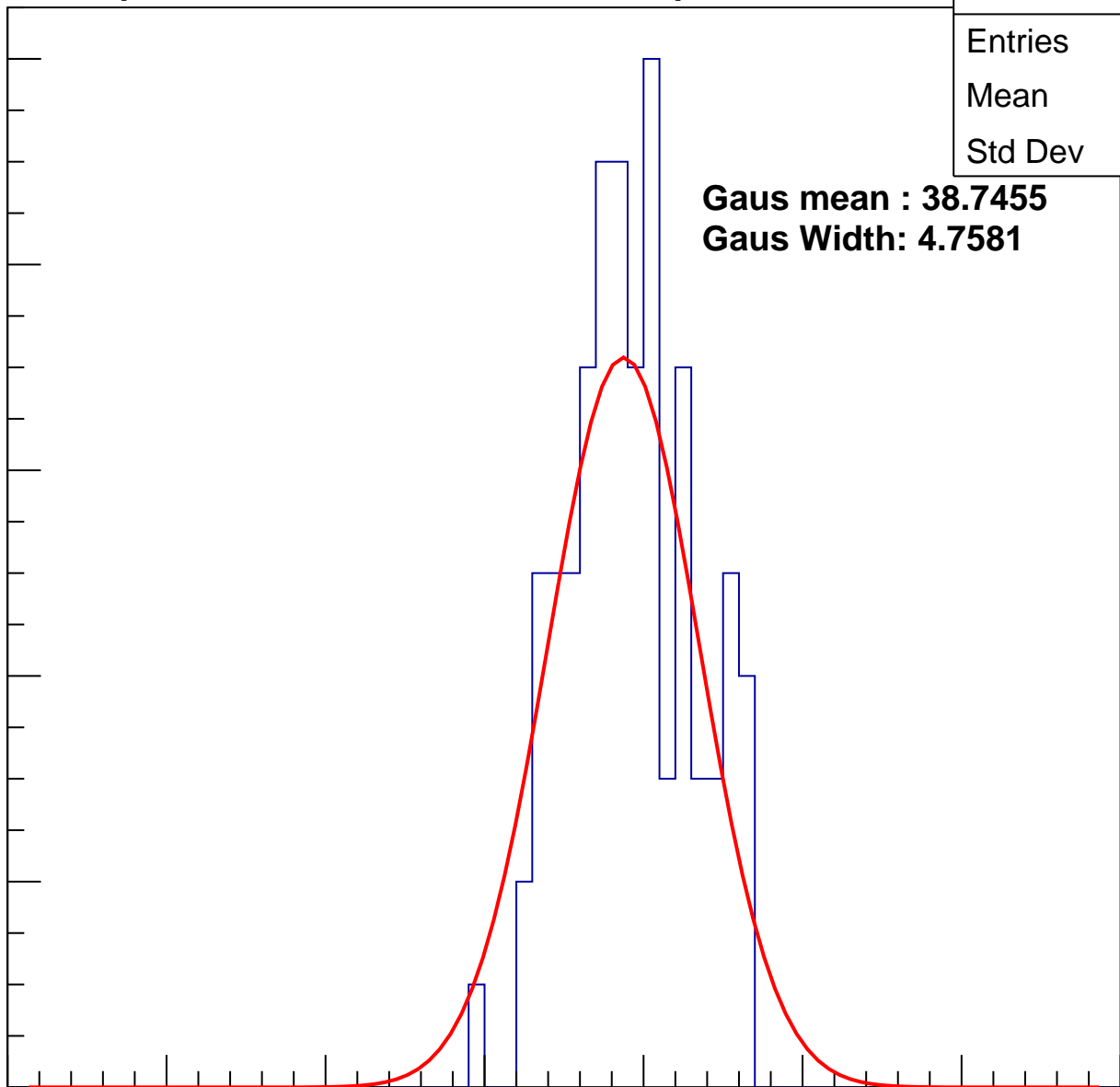
**Gaus Width: 4.7581**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U11-ch53, adc2

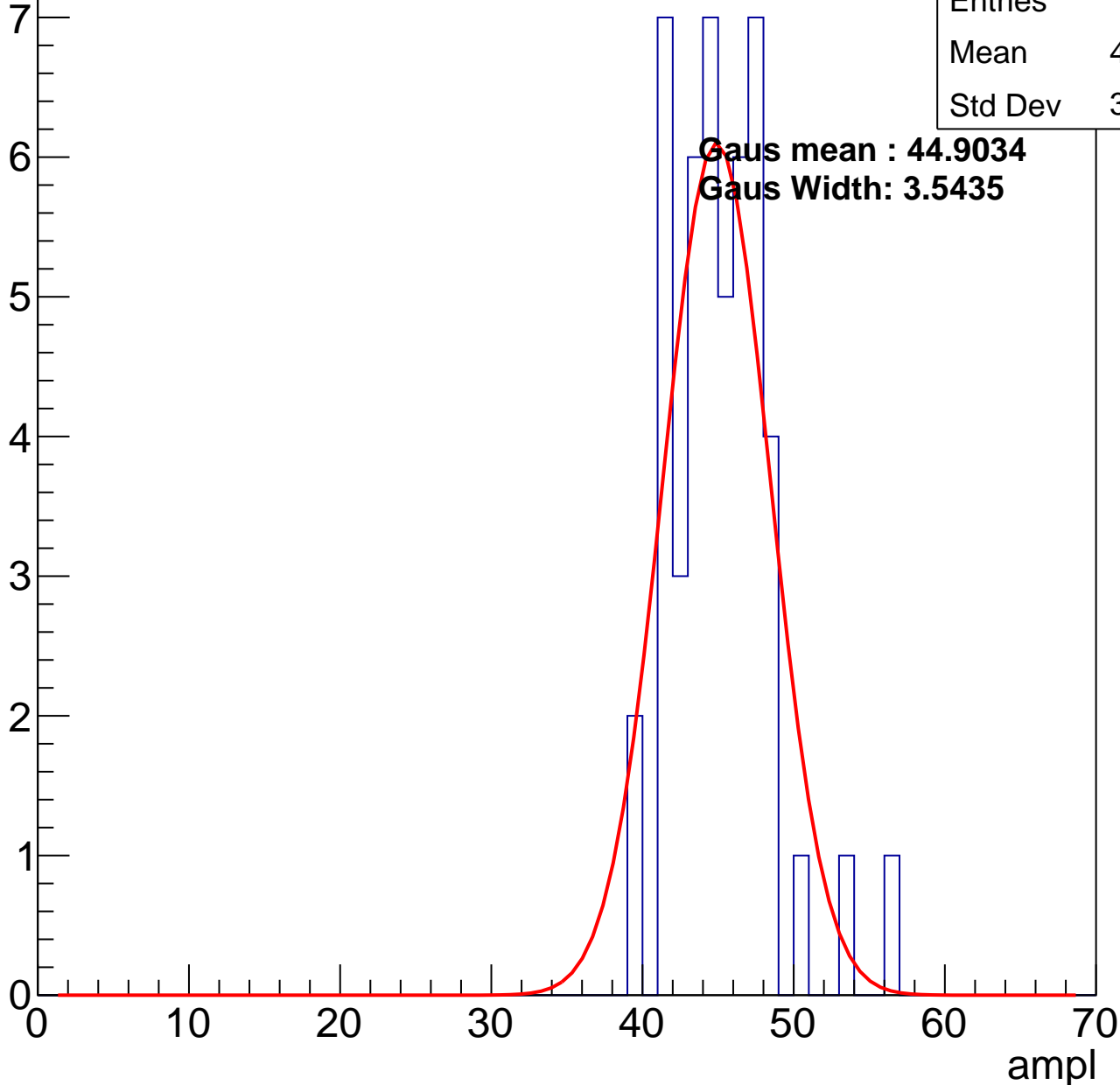
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	50
Mean	44.76
Std Dev	3.222

**Gaus mean : 44.9034**

**Gaus Width: 3.5435**

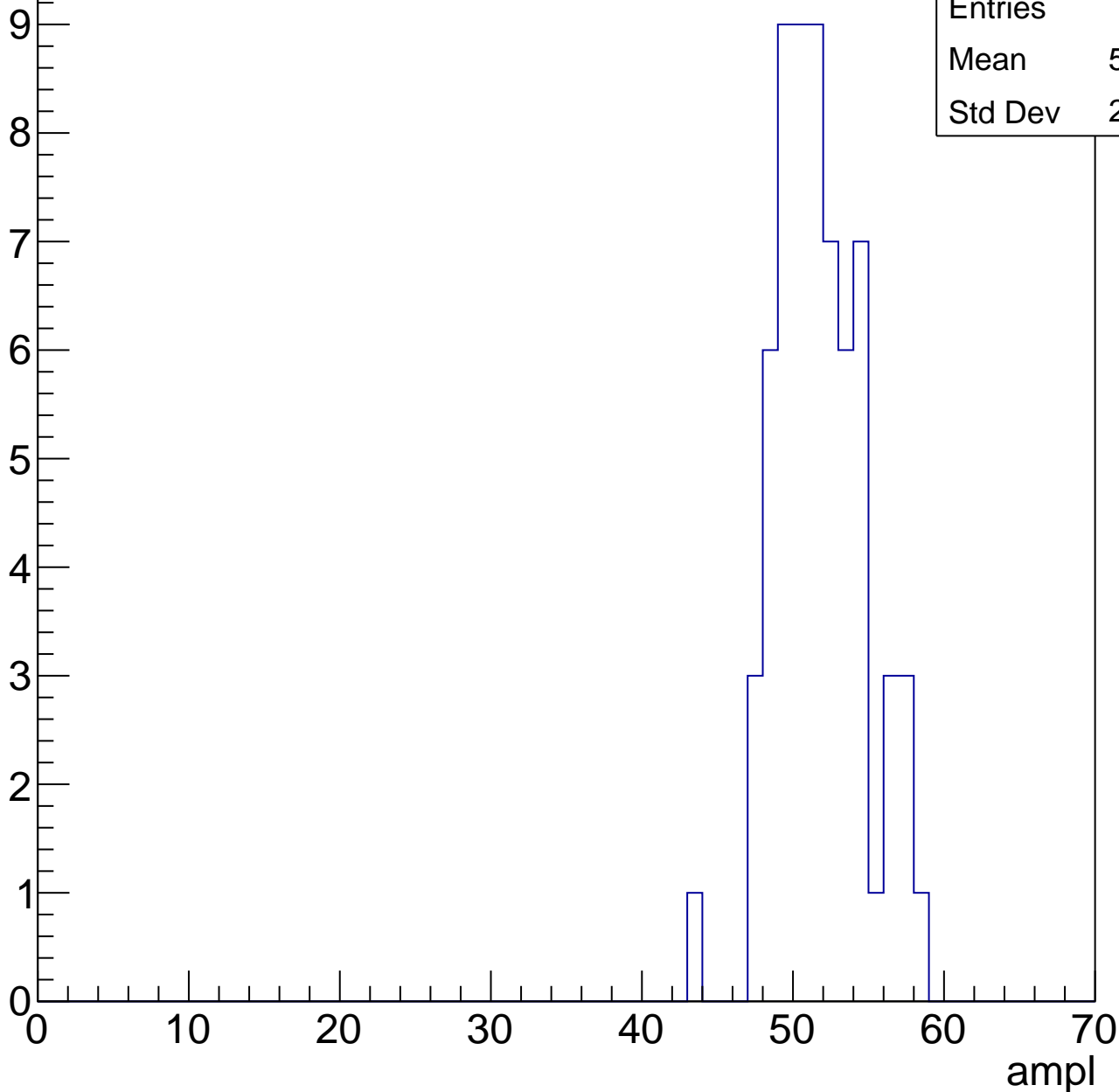


# B1L103S, U11-ch53, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	51.29
Std Dev	2.902

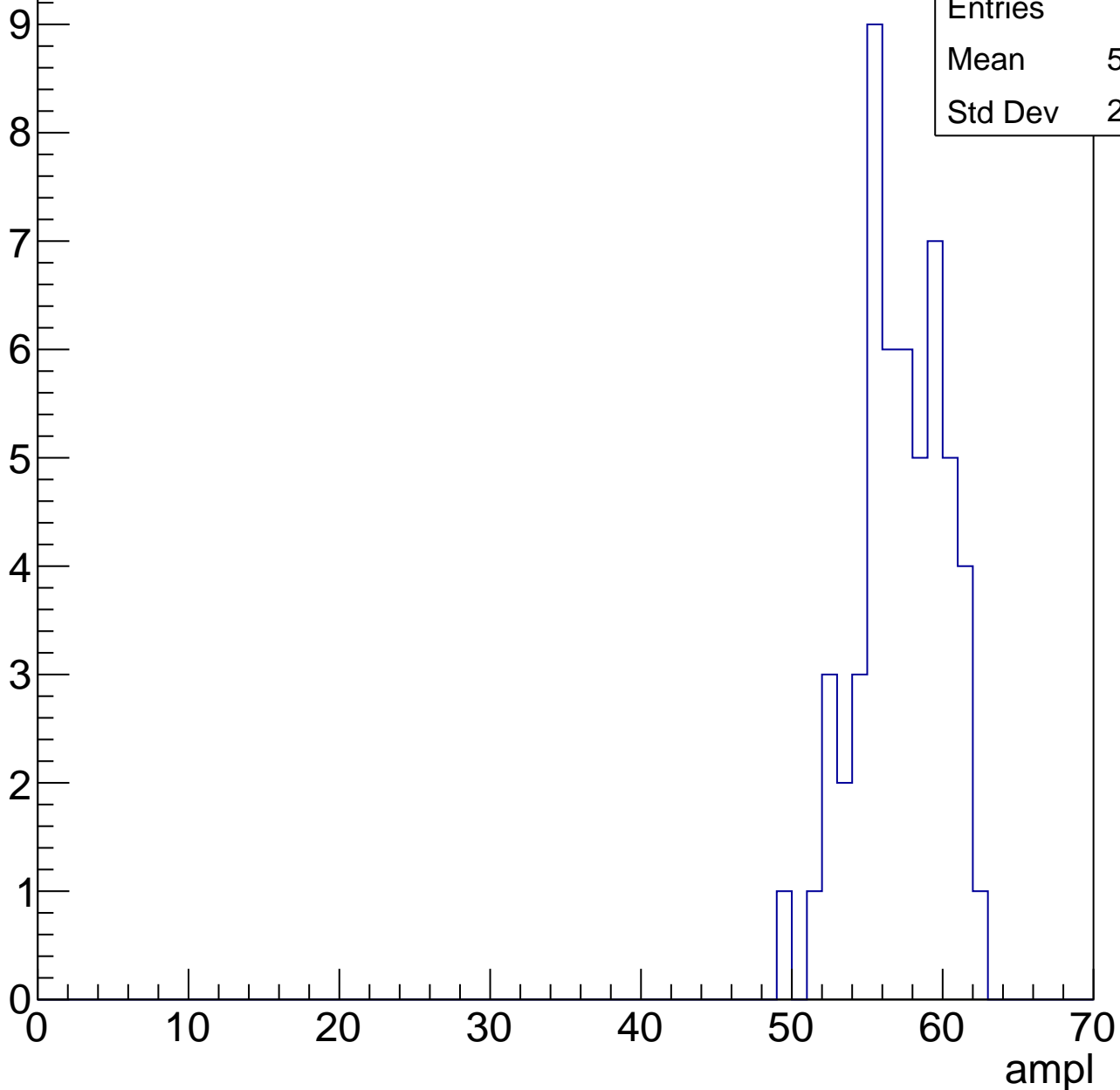


# B1L103S, U11-ch53, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	53
Mean	56.72
Std Dev	2.877

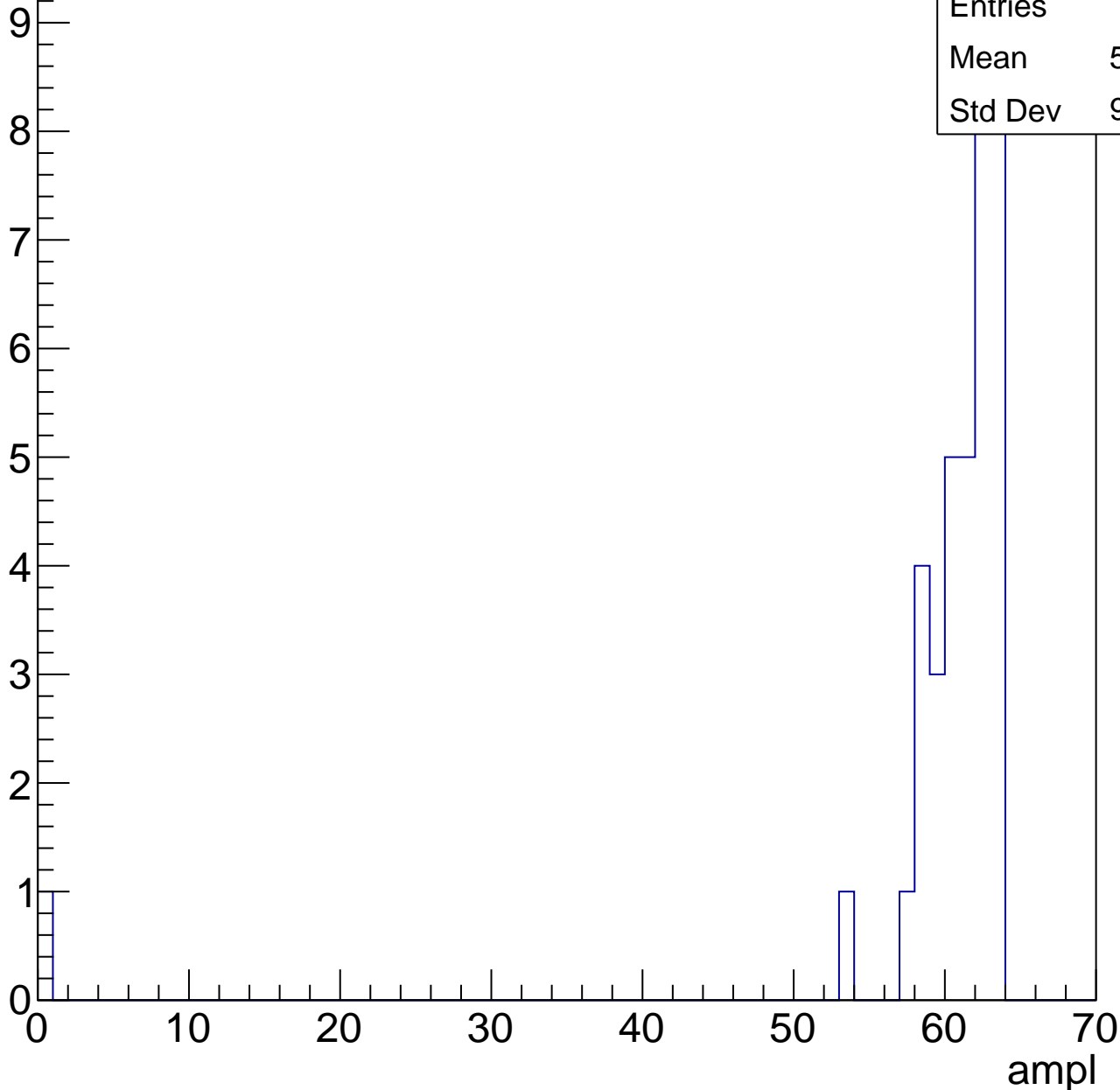


# B1L103S, U11-ch53, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	38
Mean	59.18
Std Dev	9.965



# B1L103S, U11-ch53, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U11-ch53, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U11-ch54, adc0

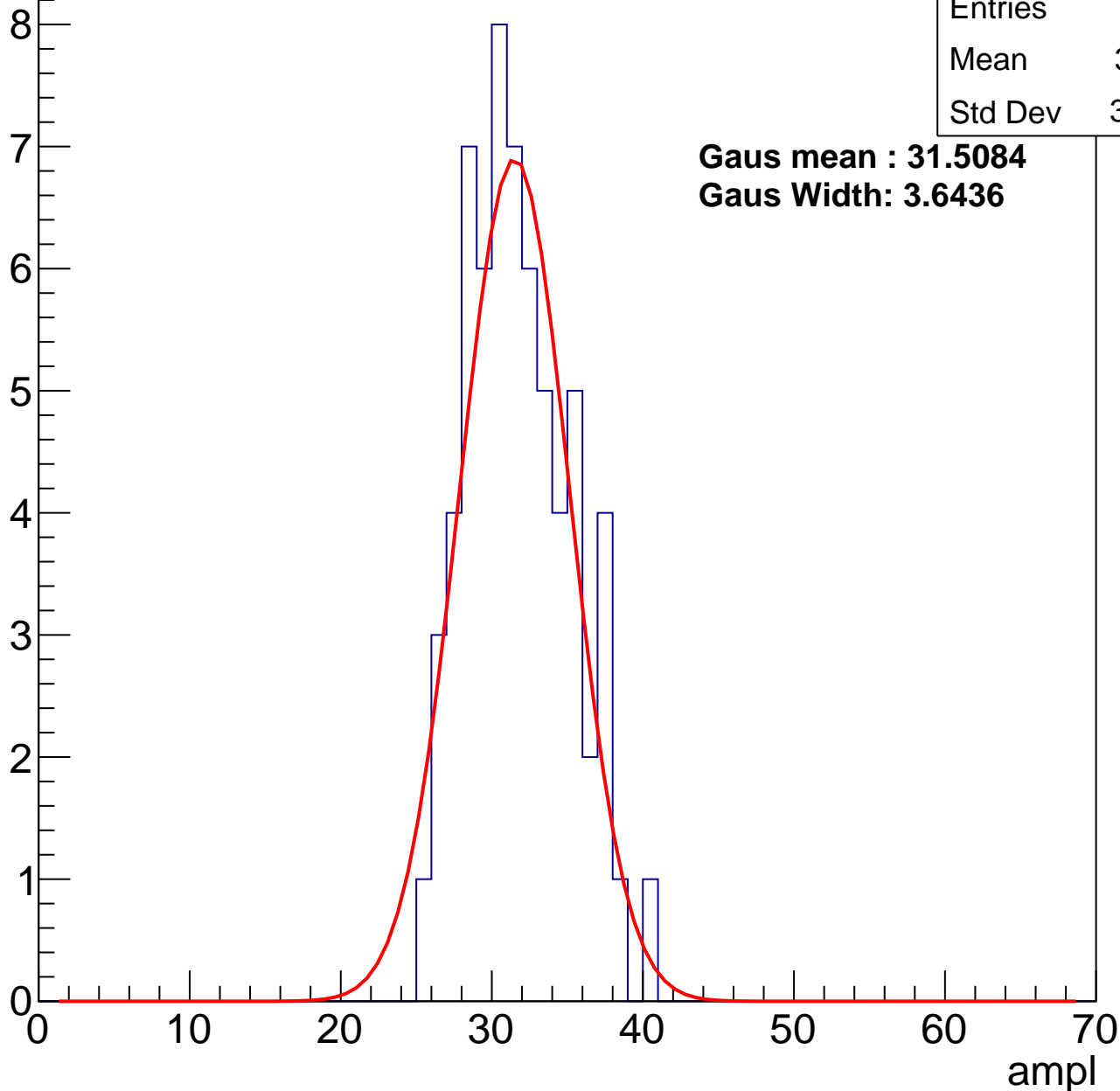
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	31.31
Std Dev	3.377

**Gaus mean : 31.5084**

**Gaus Width: 3.6436**



# B1L103S, U11-ch54, adc1

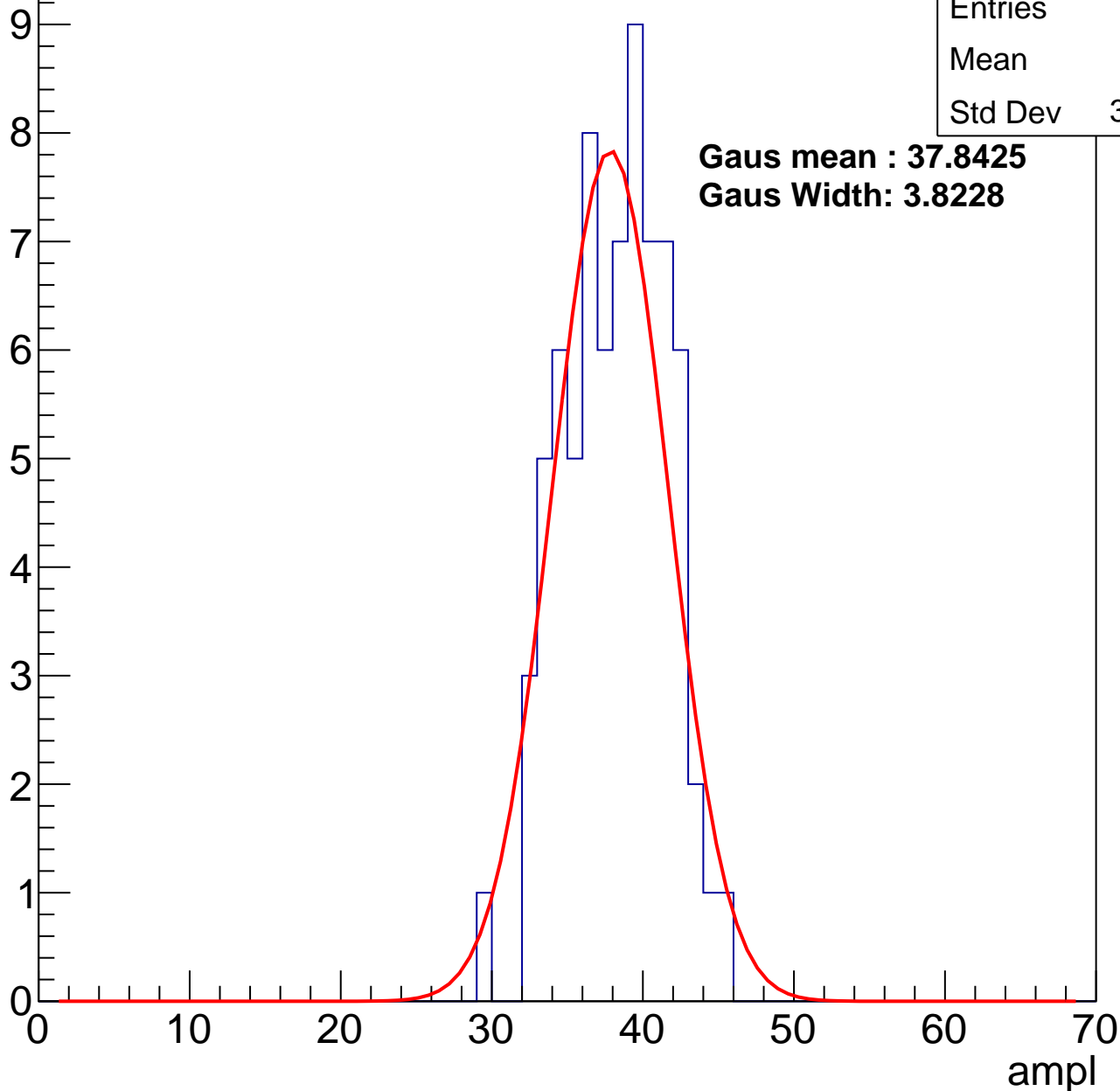
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	74
Mean	37.7
Std Dev	3.324

**Gaus mean : 37.8425**

**Gaus Width: 3.8228**



# B1L103S, U11-ch54, adc2

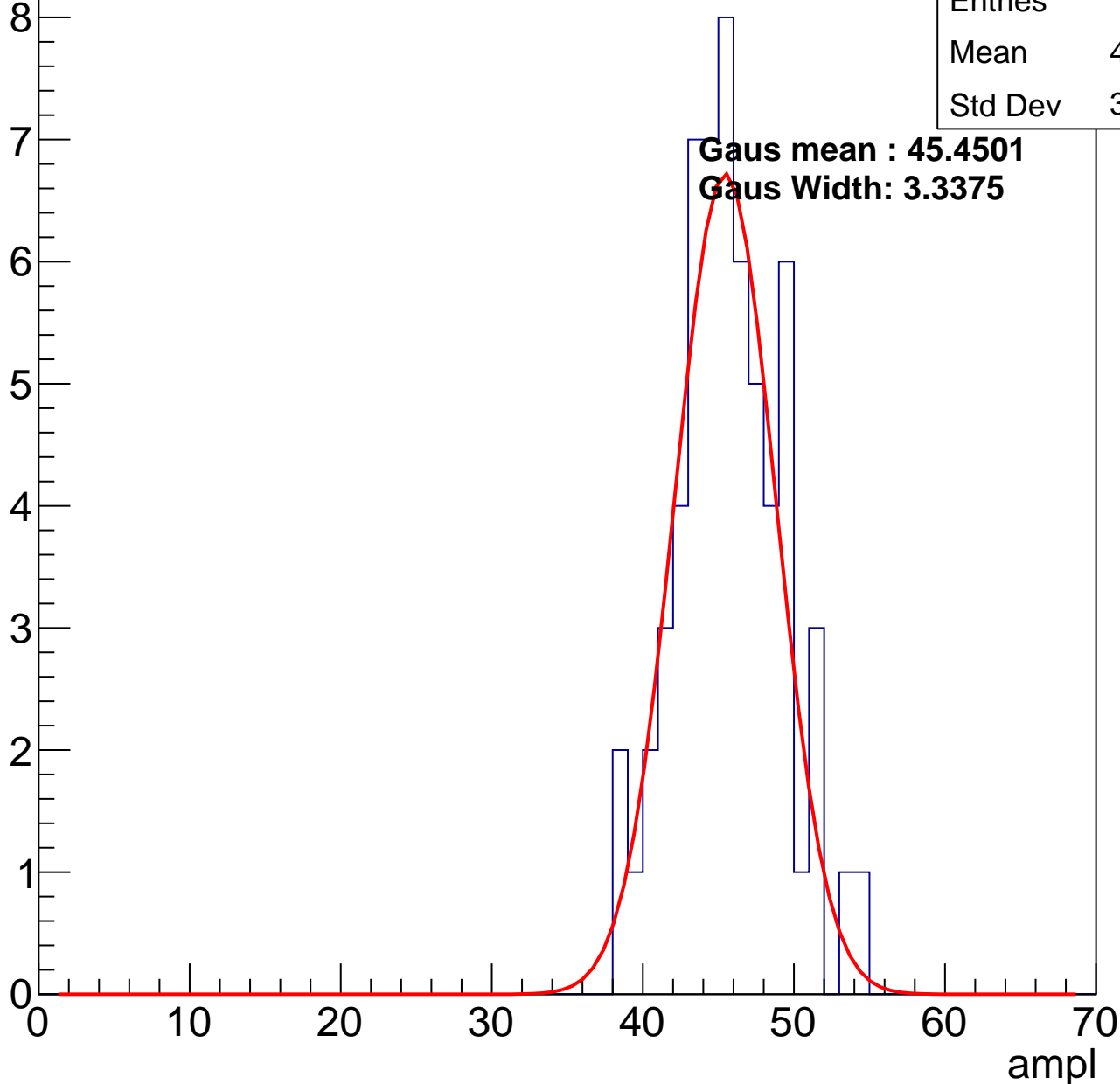
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	61
Mean	45.28
Std Dev	3.469

**Gaus mean : 45.4501**

**Gaus Width: 3.3375**

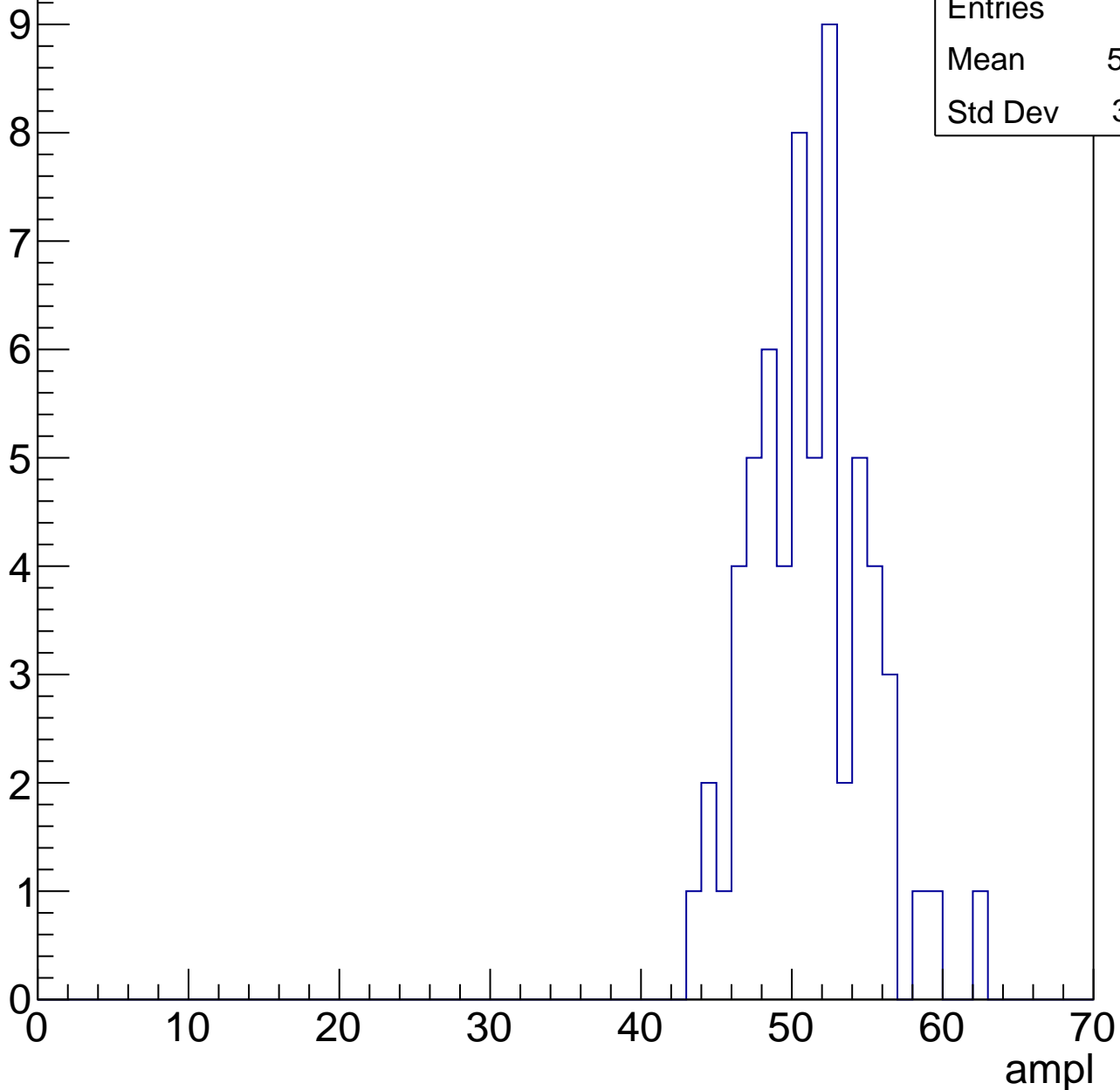


# B1L103S, U11-ch54, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	50.73
Std Dev	3.781

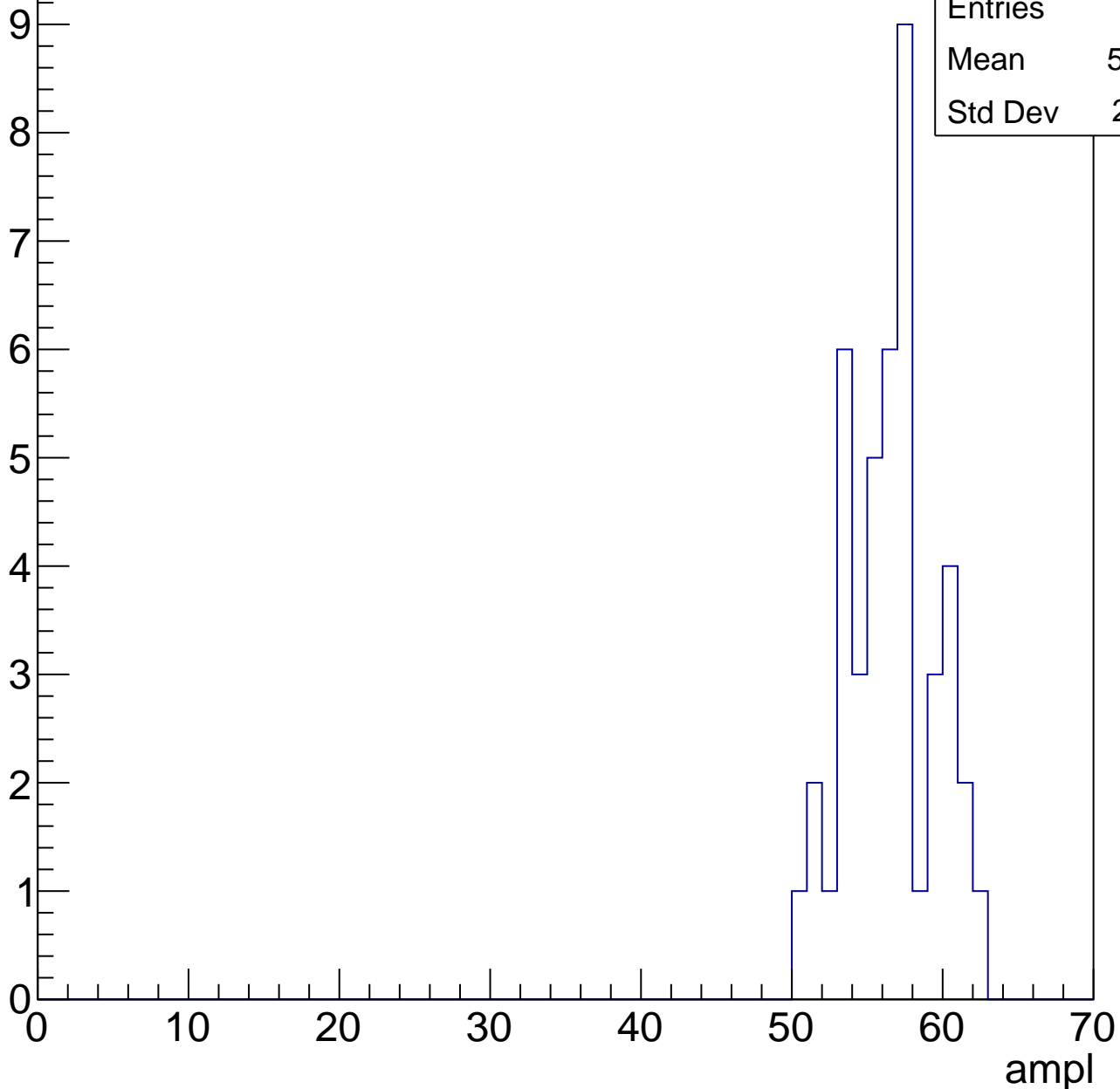


# B1L103S, U11-ch54, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

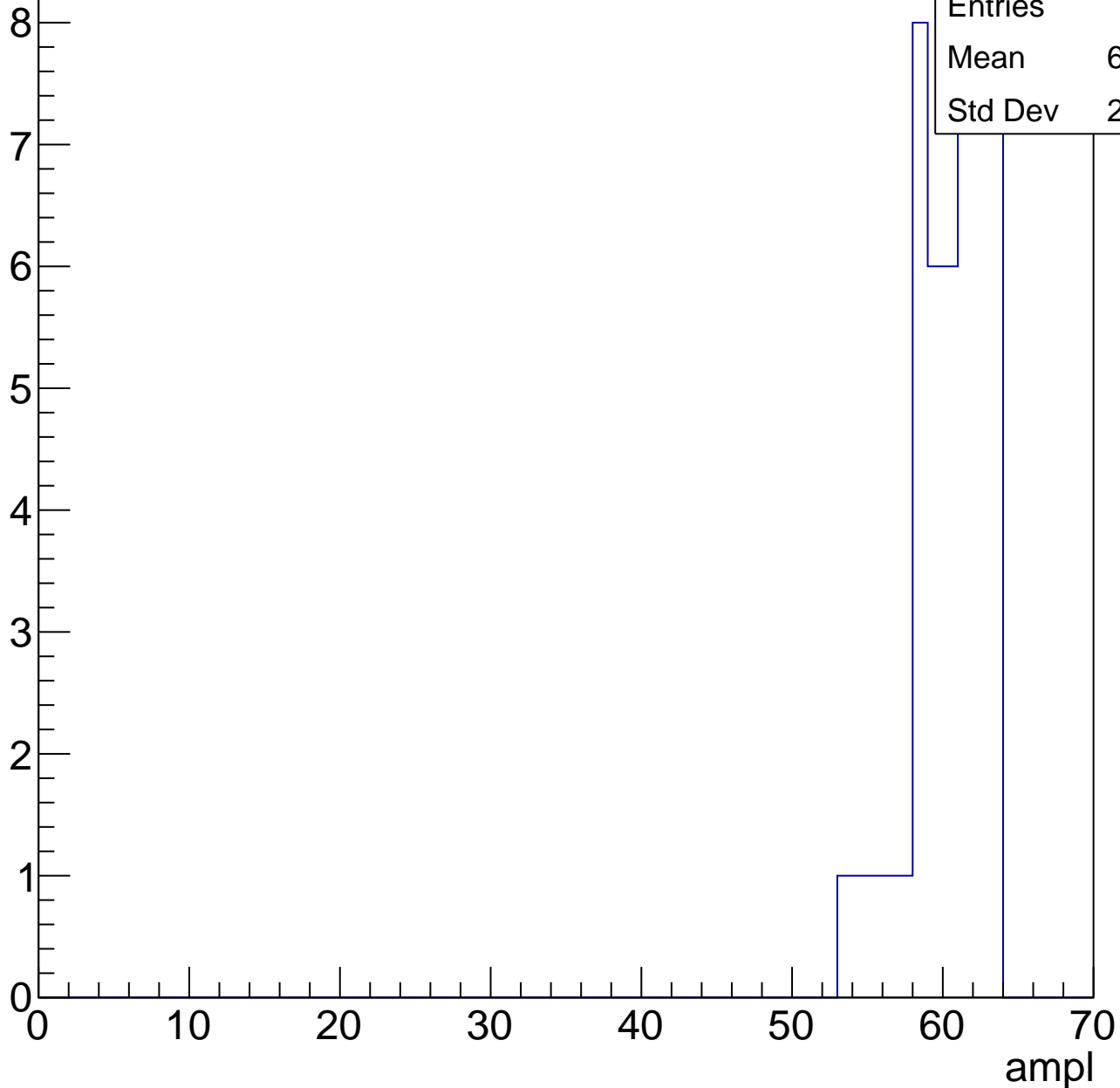
Entries	44
Mean	56.07
Std Dev	2.871



# B1L103S, U11-ch54, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U11-ch54, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U11-ch54, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U11-ch55, adc0

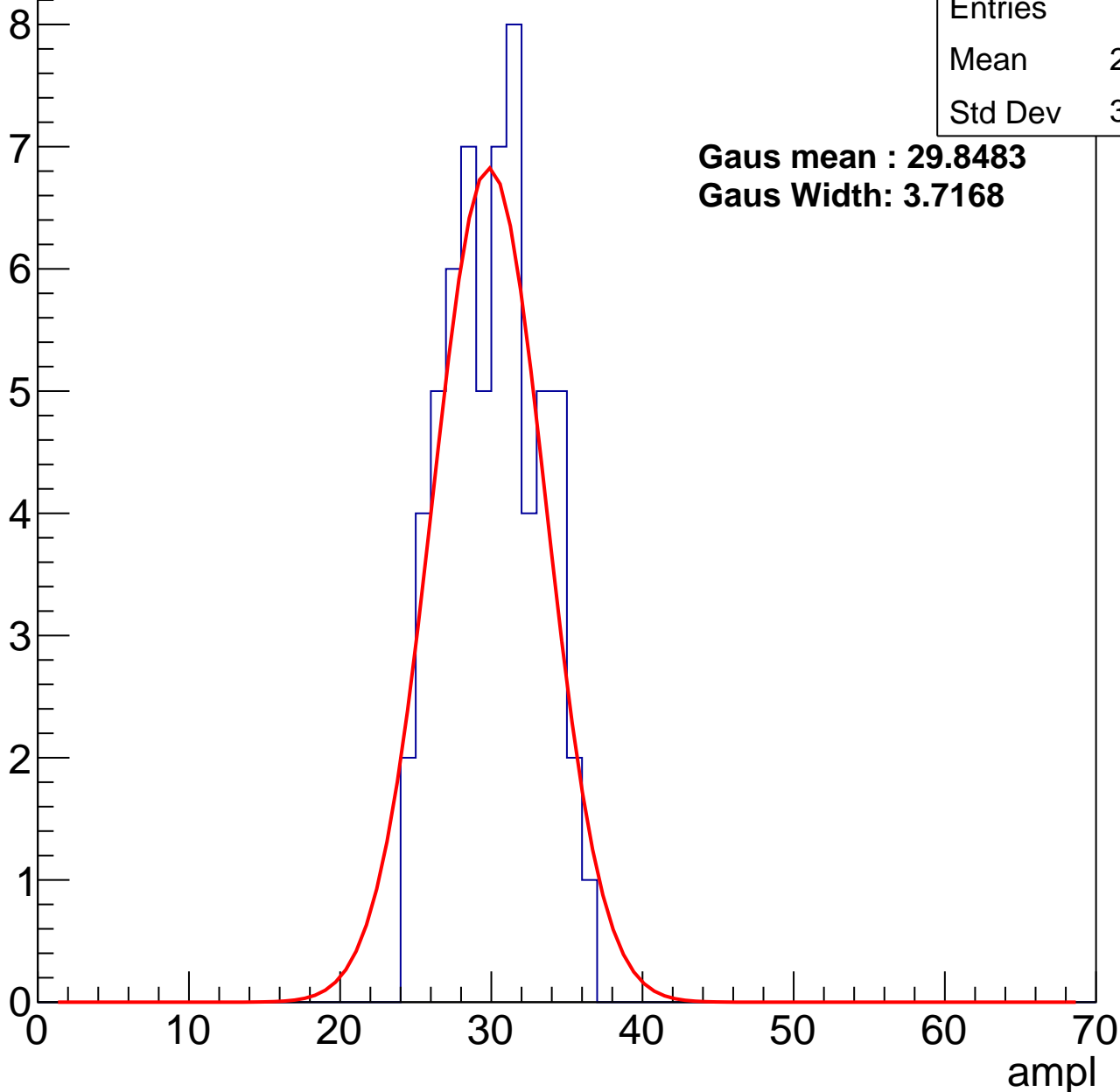
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	61
Mean	29.64
Std Dev	3.046

**Gaus mean : 29.8483**

**Gaus Width: 3.7168**

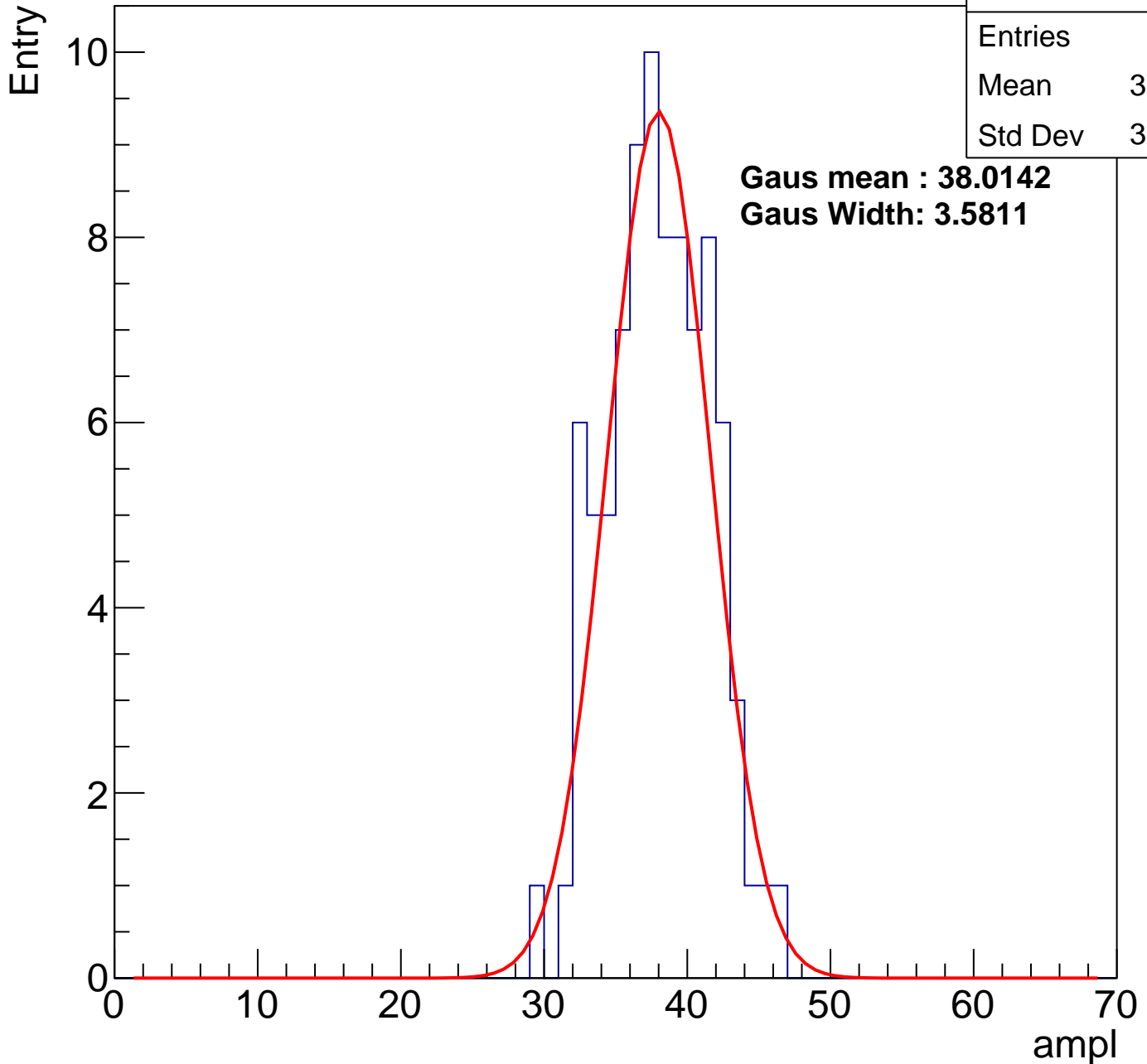


# B1L103S, U11-ch55, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	87
Mean	37.54
Std Dev	3.506

**Gaus mean : 38.0142**  
**Gaus Width: 3.5811**



# B1L103S, U11-ch55, adc2

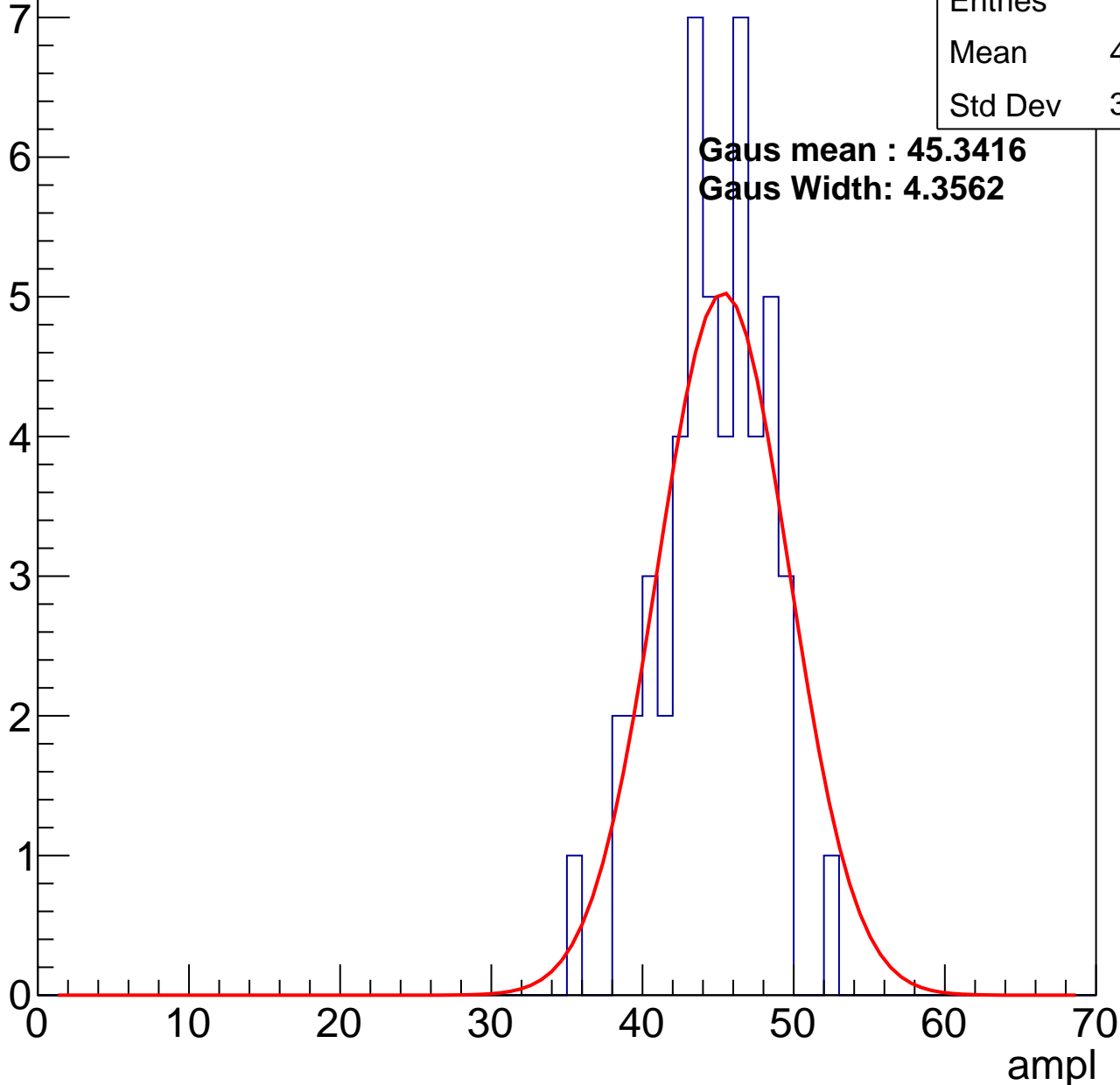
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	50
Mean	44.18
Std Dev	3.398

**Gaus mean : 45.3416**

**Gaus Width: 4.3562**



# B1L103S, U11-ch55, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

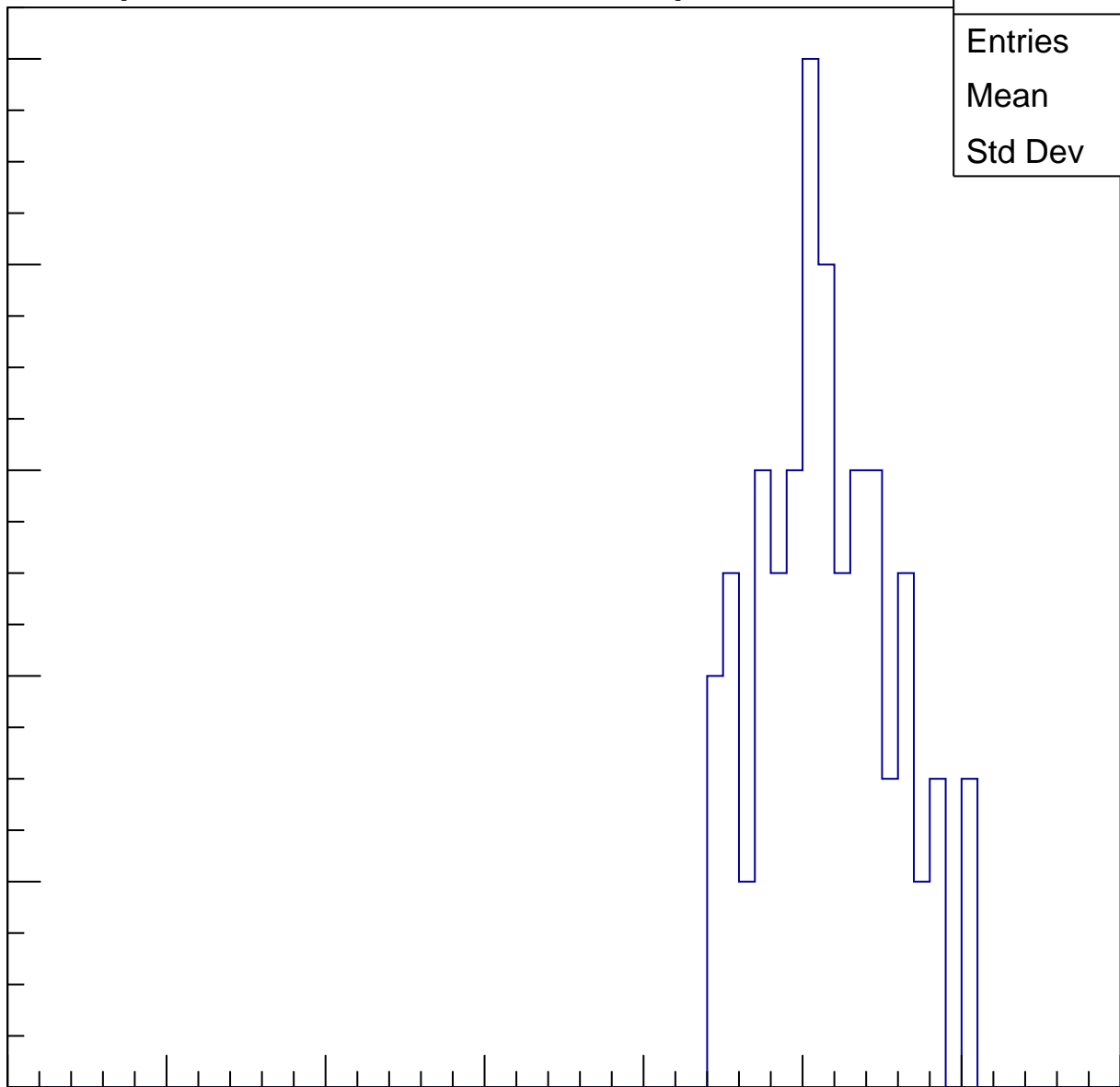
Entries	79
Mean	51.04
Std Dev	4.086

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

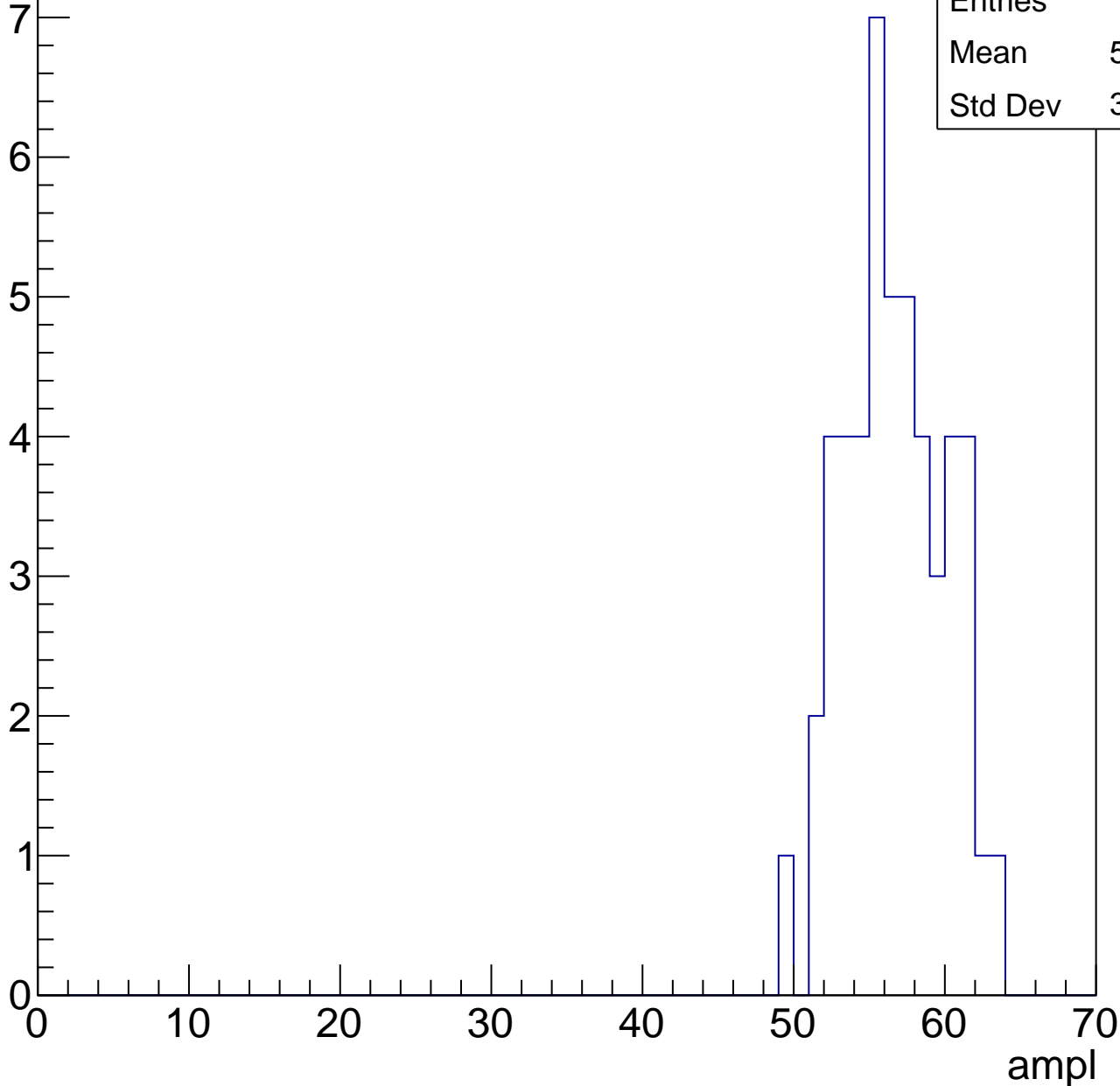


# B1L103S, U11-ch55, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	49
Mean	56.22
Std Dev	3.247

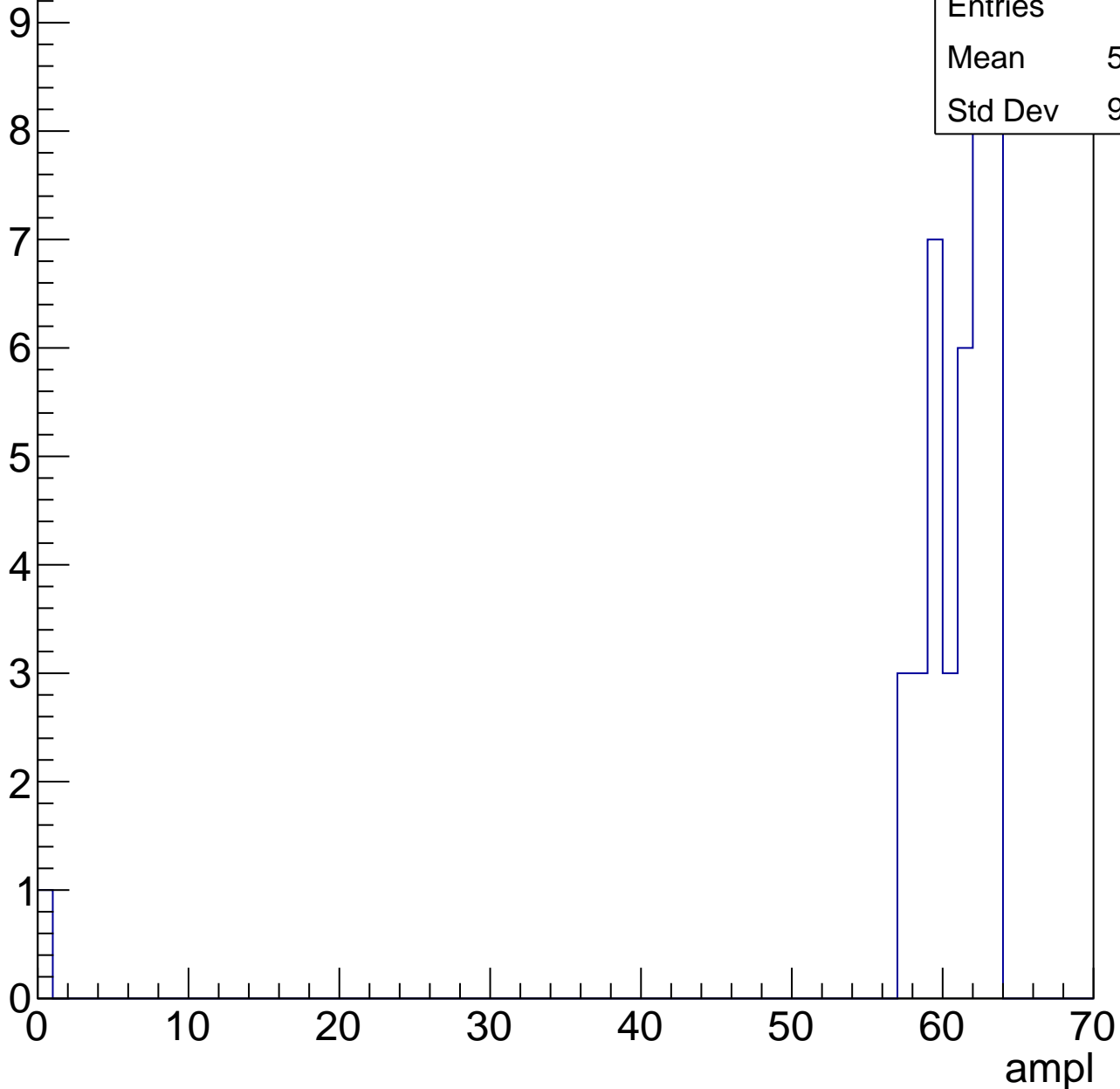


# B1L103S, U11-ch55, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	40
Mean	59.15
Std Dev	9.658



# B1L103S, U11-ch55, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U11-ch55, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U11-ch56, adc0

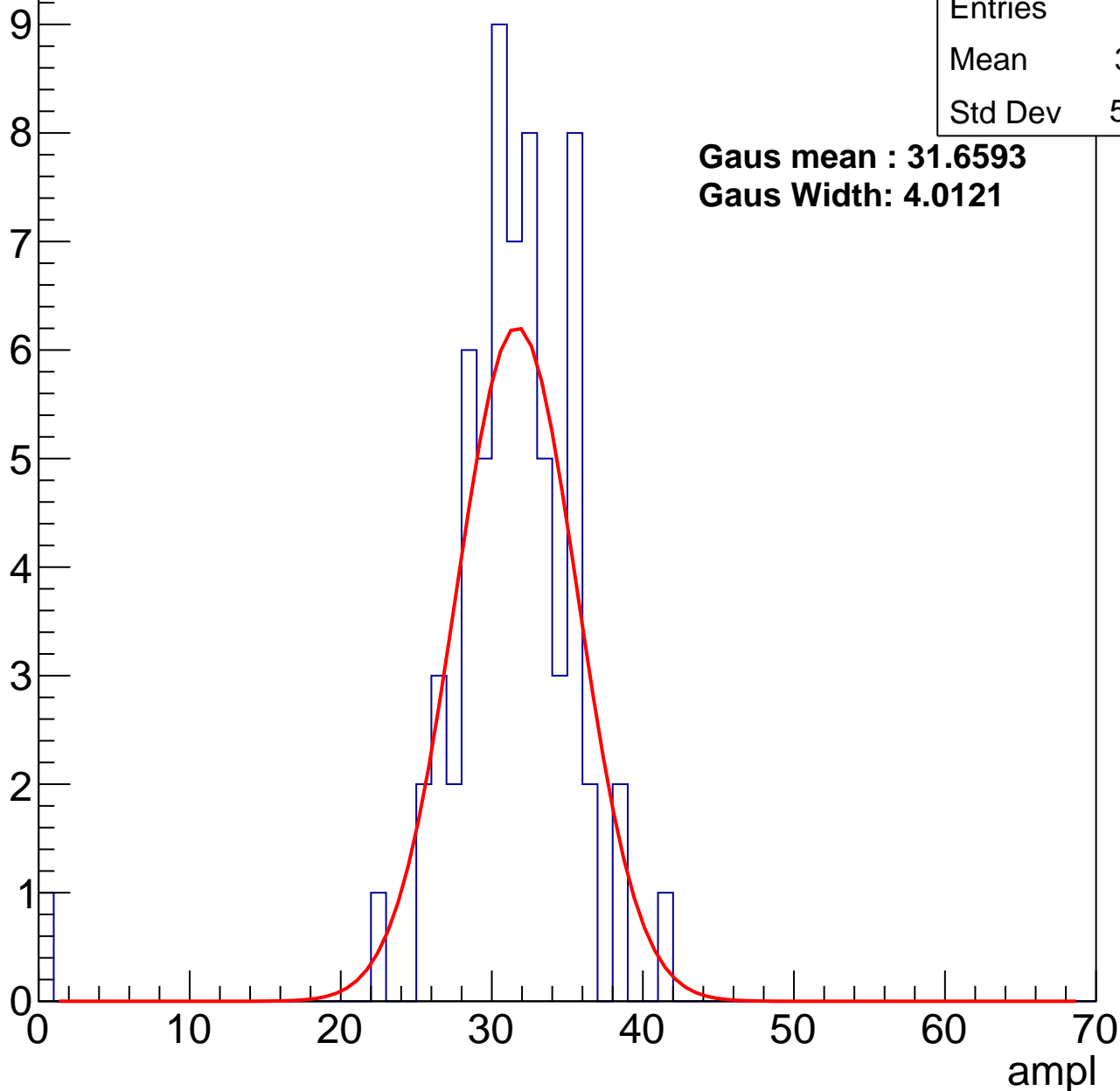
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	30.71
Std Dev	5.158

**Gaus mean : 31.6593**

**Gaus Width: 4.0121**



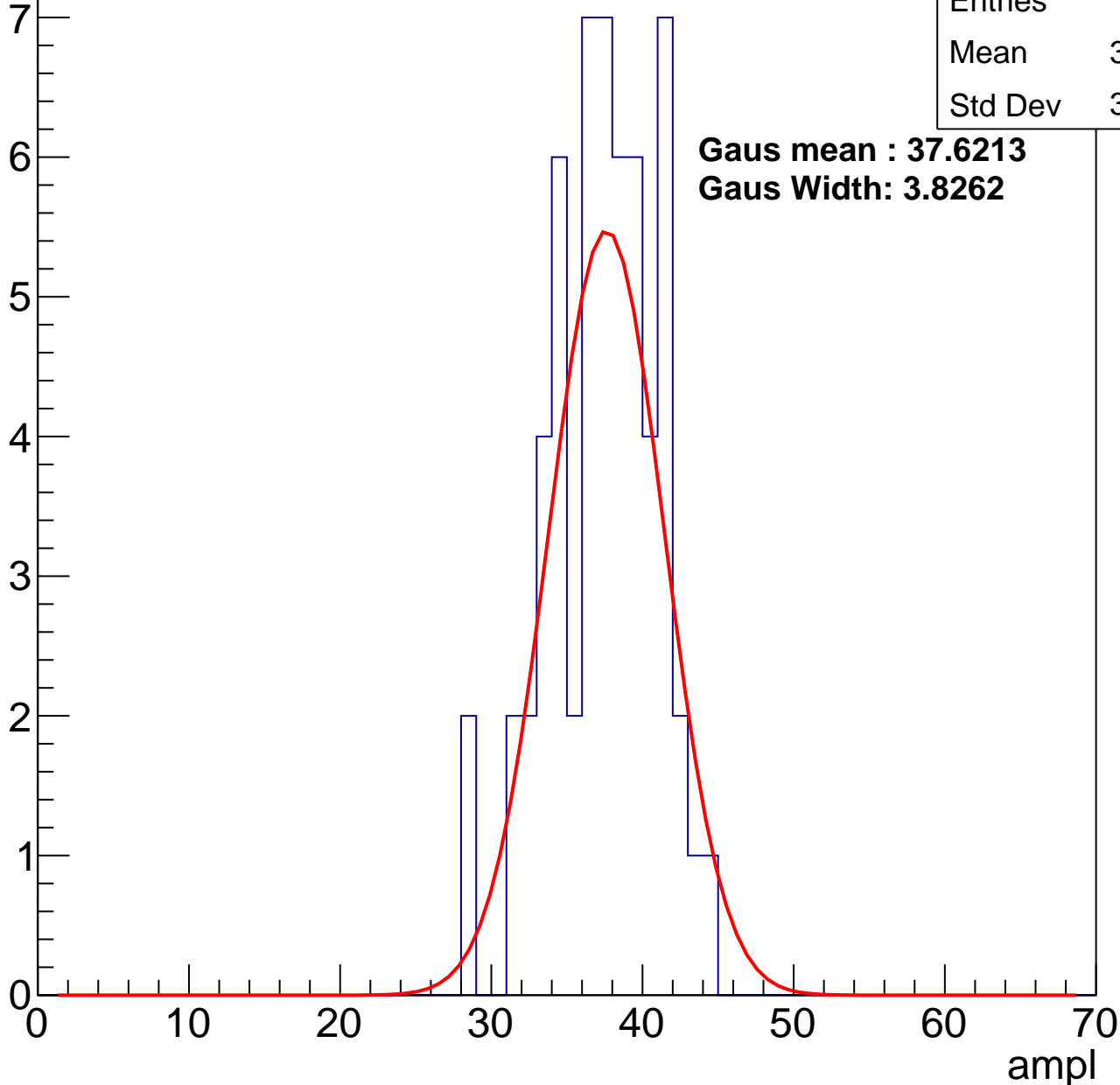
# B1L103S, U11-ch56, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	59
Mean	36.93
Std Dev	3.517

**Gaus mean : 37.6213**  
**Gaus Width: 3.8262**



# B1L103S, U11-ch56, adc2

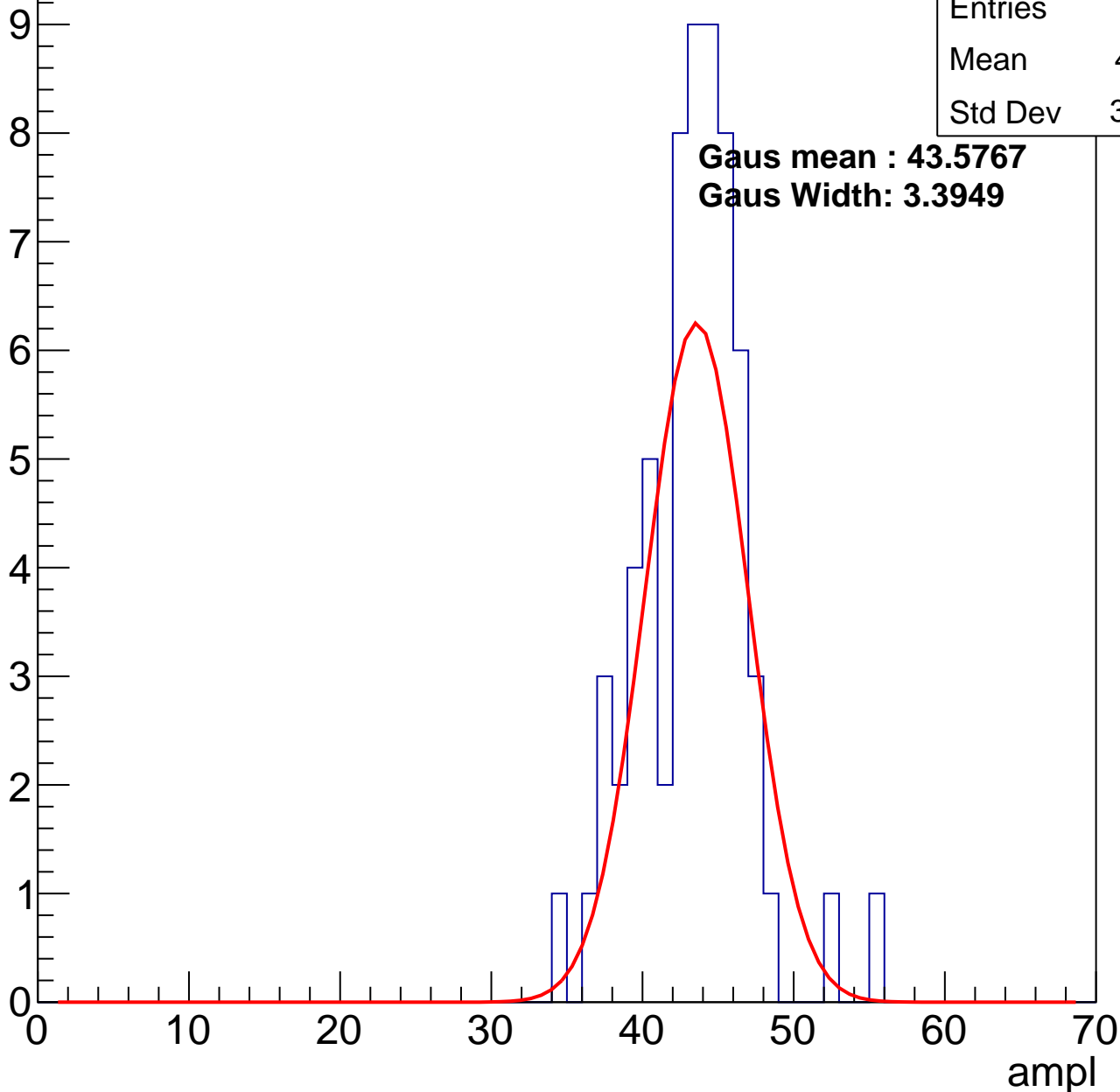
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	42.91
Std Dev	3.548

**Gaus mean : 43.5767**

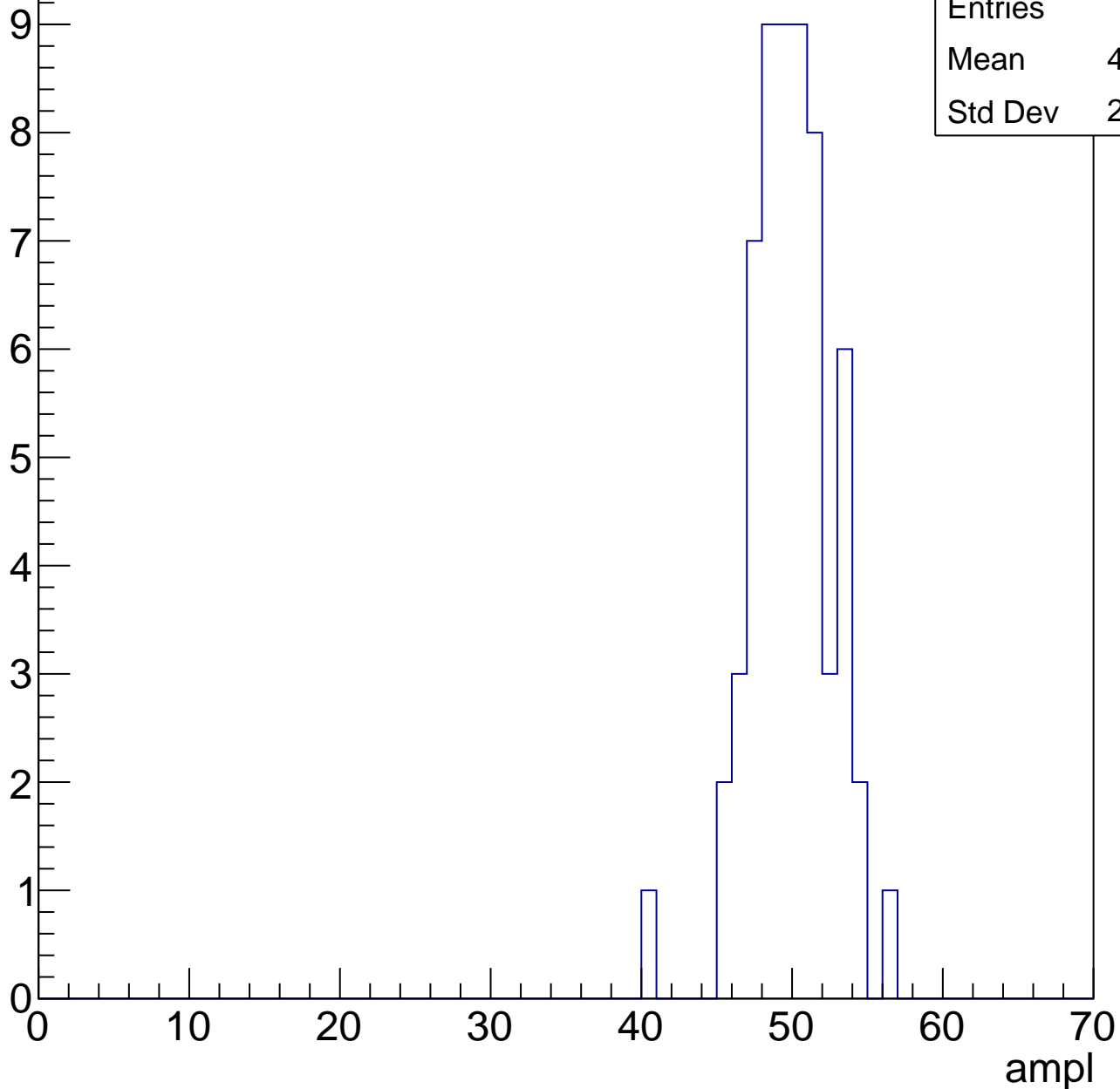
**Gaus Width: 3.3949**



# B1L103S, U11-ch56, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



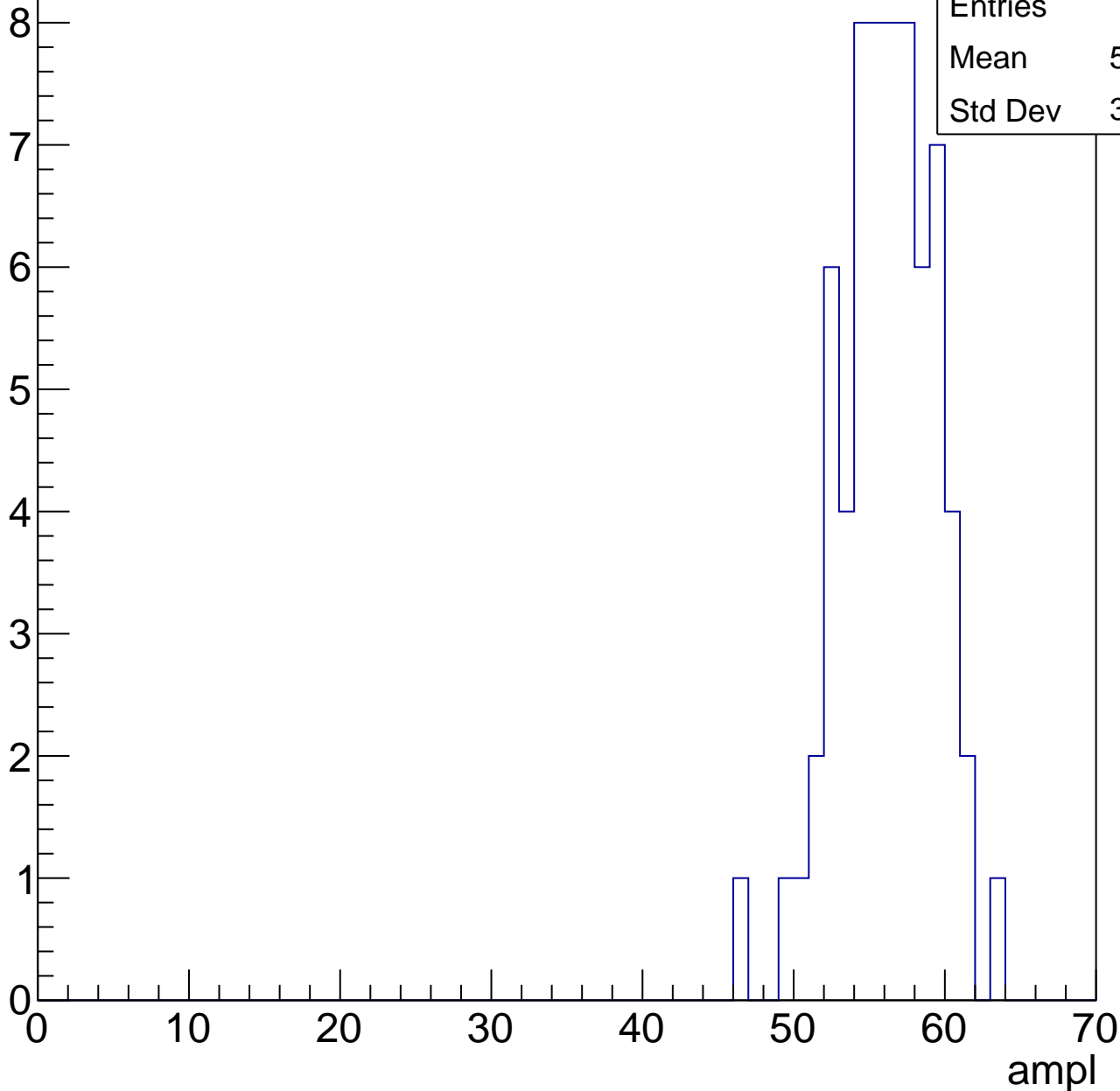
Entries	60
Mean	49.43
Std Dev	2.673

# B1L103S, U11-ch56, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	55.72
Std Dev	3.138

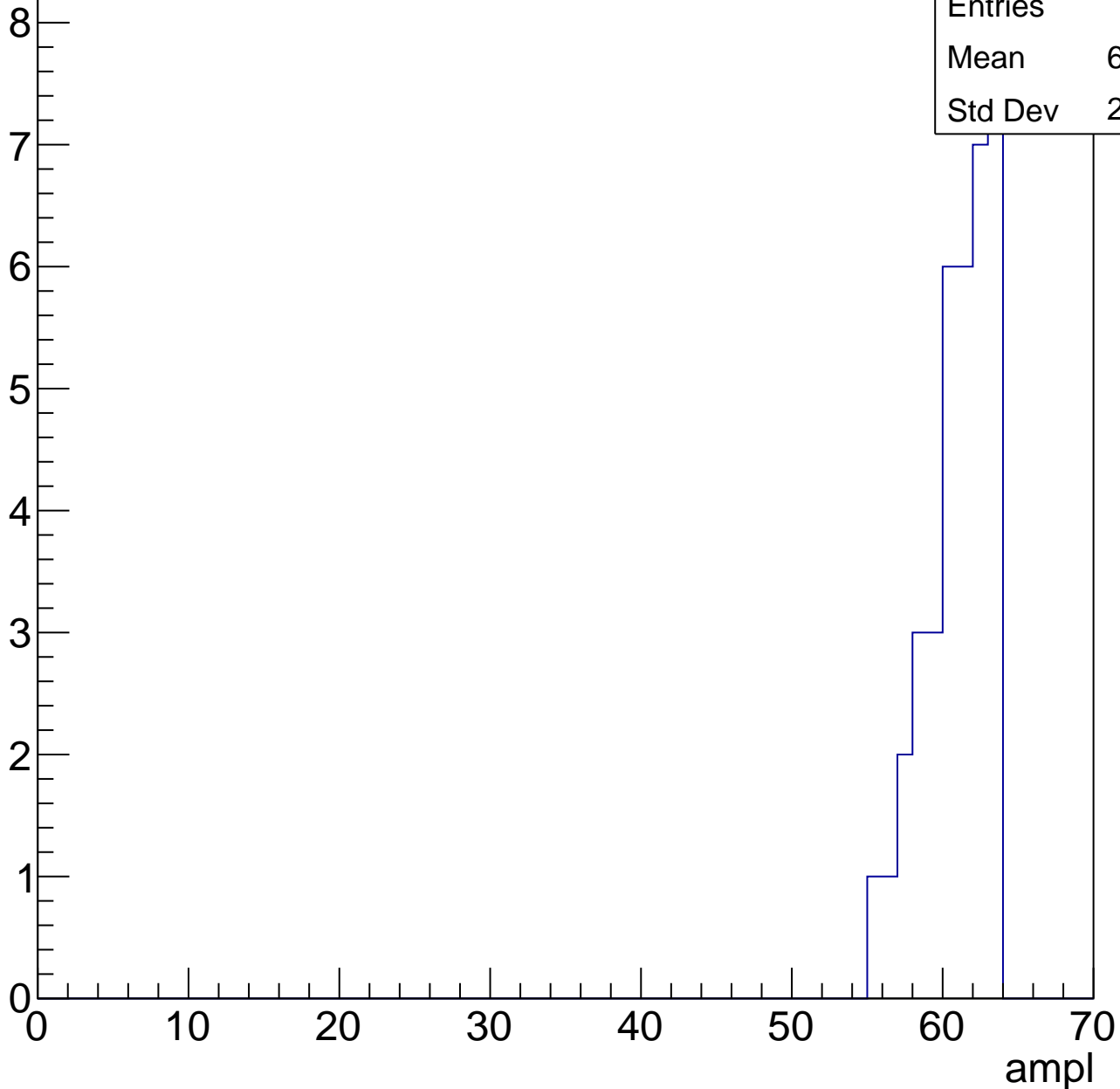


# B1L103S, U11-ch56, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

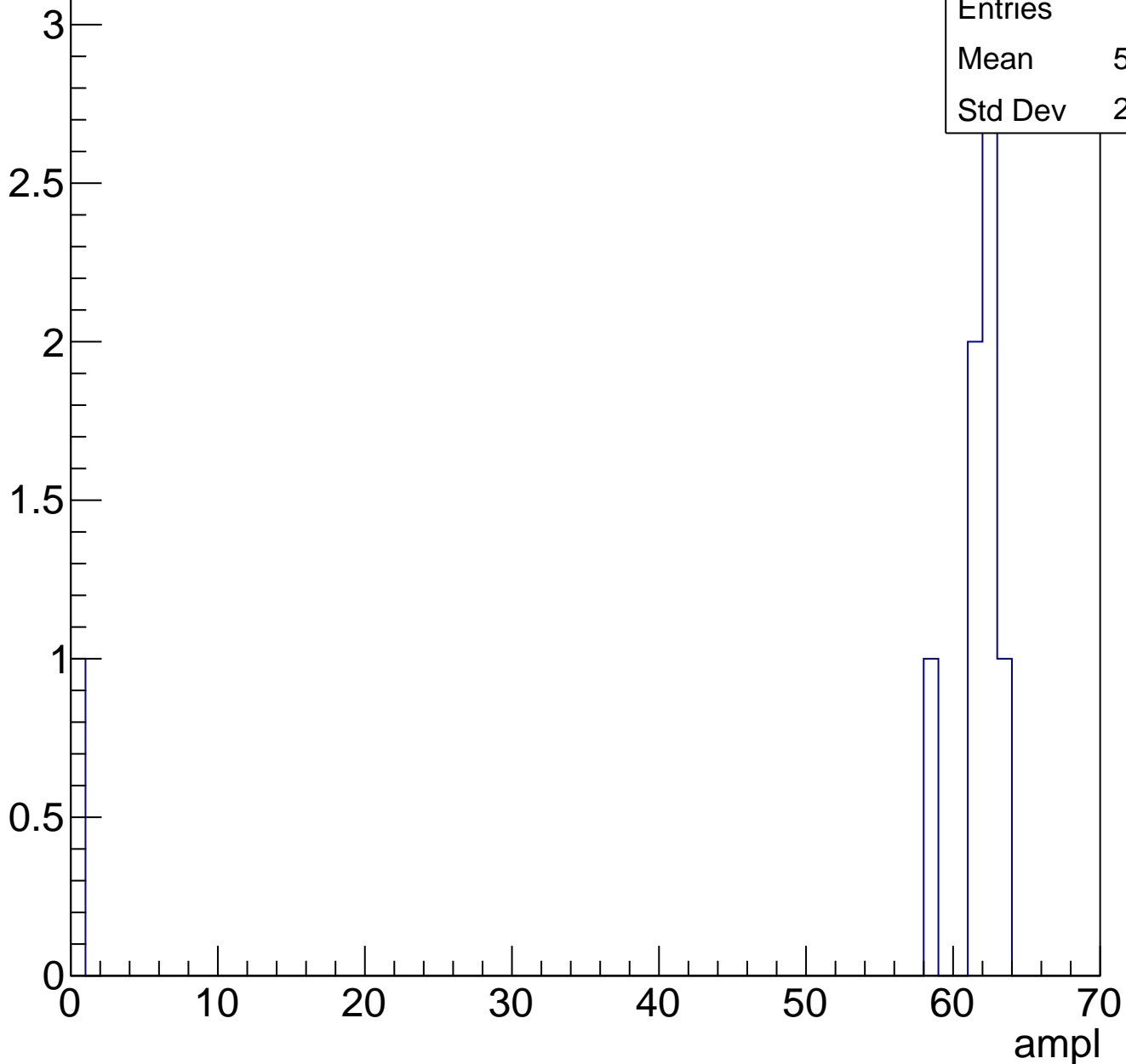
Entries	37
Mean	60.54
Std Dev	2.138



# B1L103S, U11-ch56, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U11-ch56, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U11-ch57, adc0

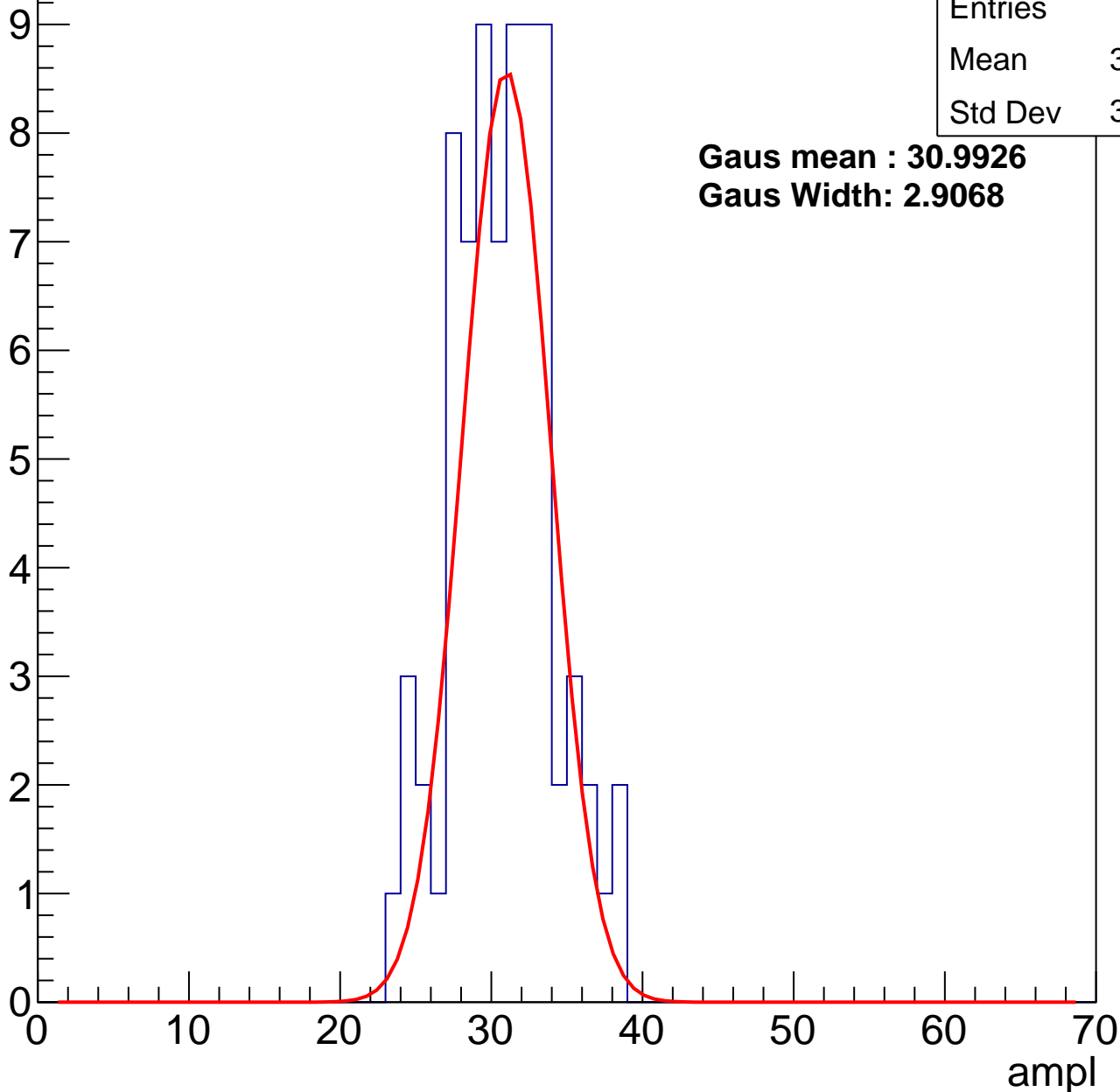
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	75
Mean	30.35
Std Dev	3.276

**Gaus mean : 30.9926**

**Gaus Width: 2.9068**



# B1L103S, U11-ch57, adc1

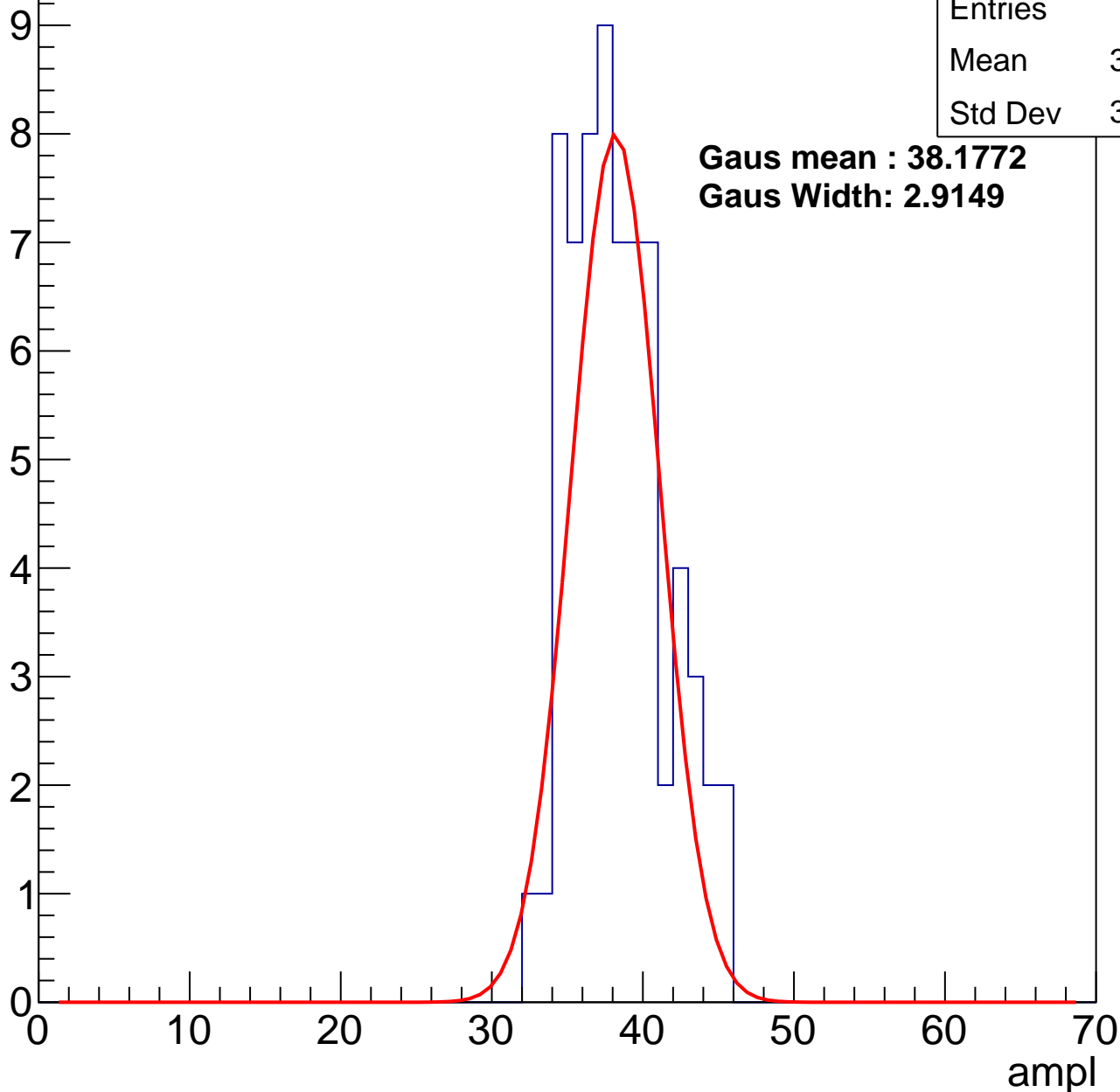
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	68
Mean	37.93
Std Dev	3.103

**Gaus mean : 38.1772**

**Gaus Width: 2.9149**



# B1L103S, U11-ch57, adc2

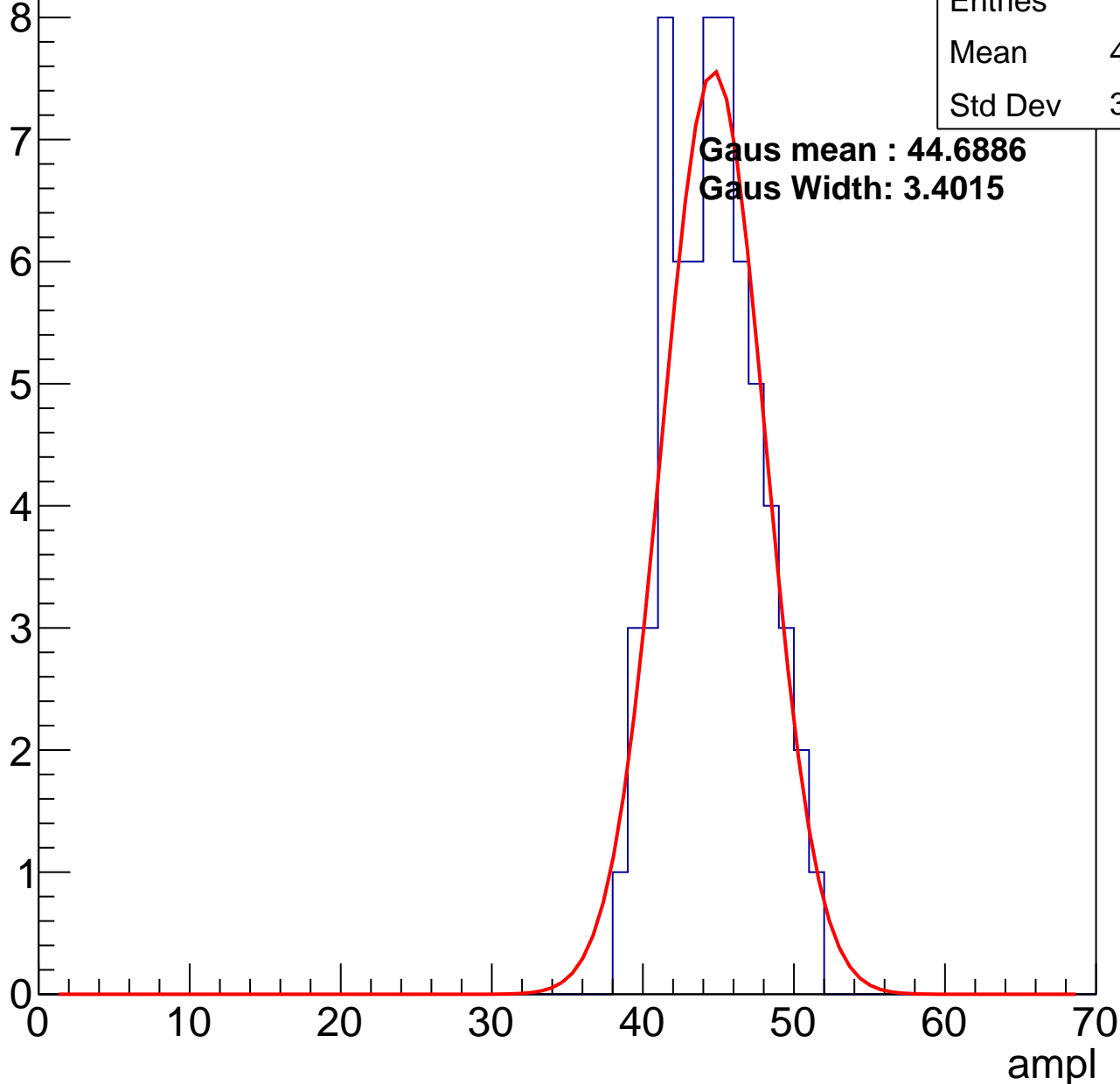
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	44.16
Std Dev	3.053

**Gaus mean : 44.6886**

**Gaus Width: 3.4015**

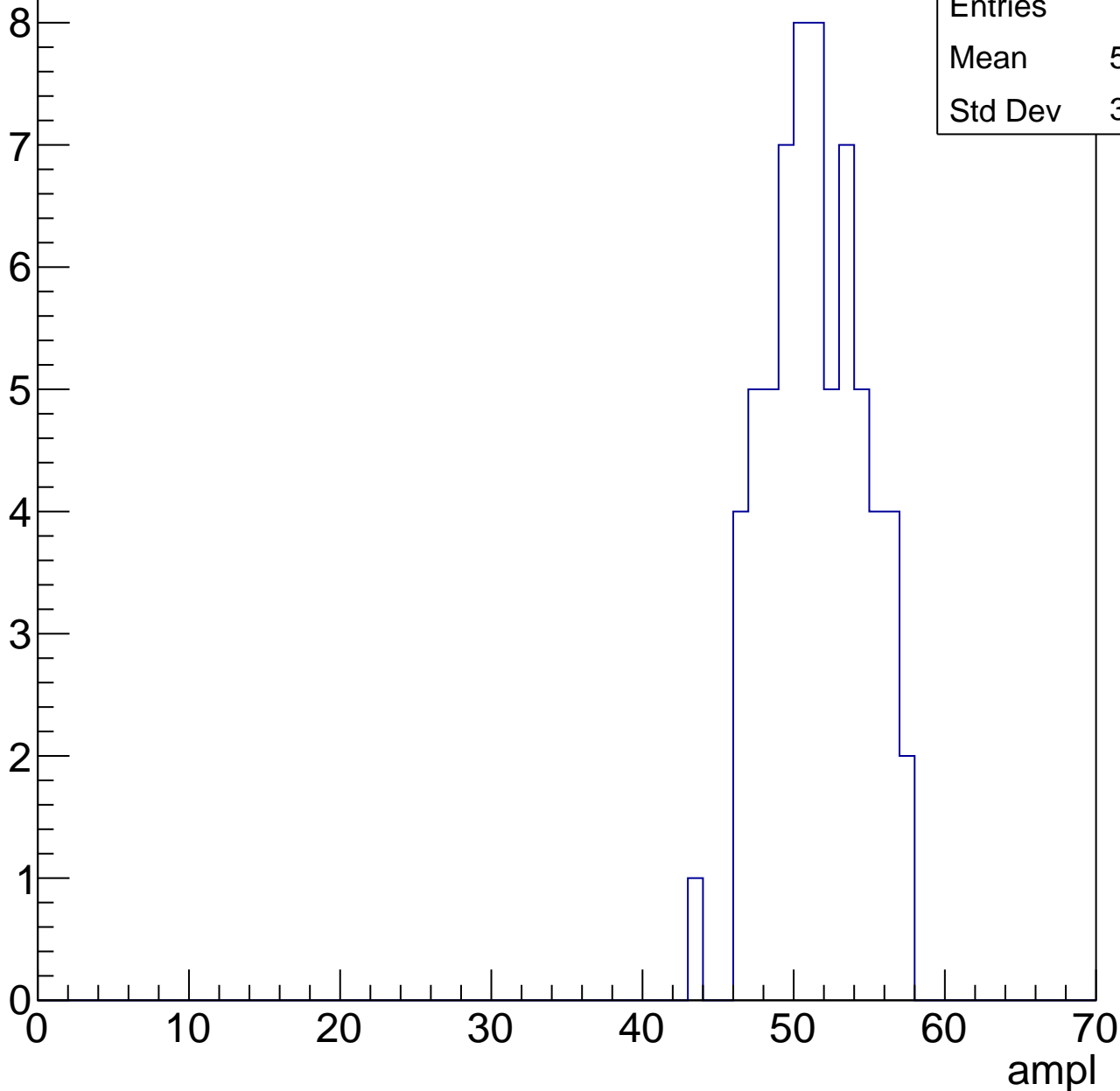


# B1L103S, U11-ch57, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	50.95
Std Dev	3.135

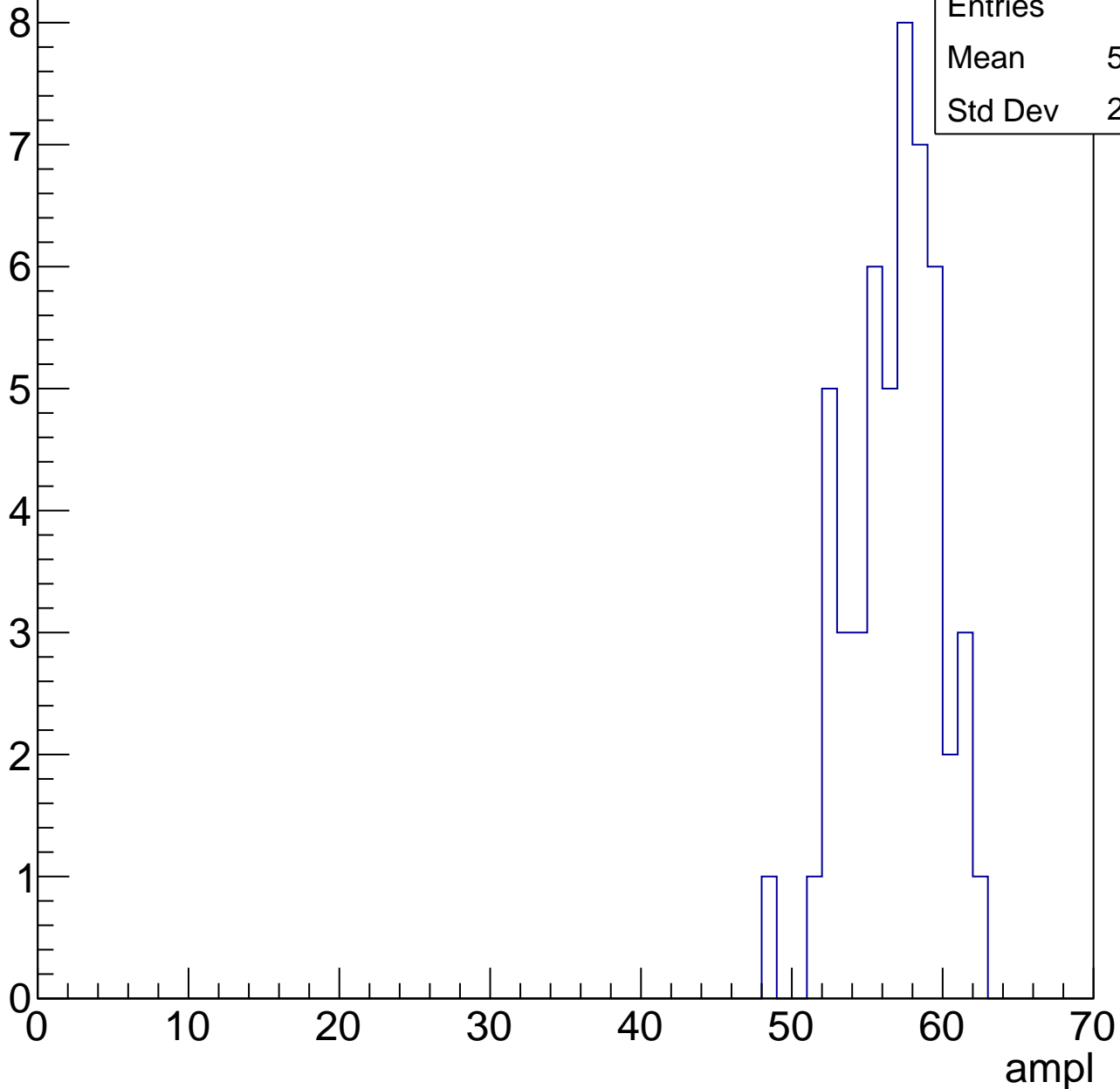


# B1L103S, U11-ch57, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	51
Mean	56.29
Std Dev	2.946

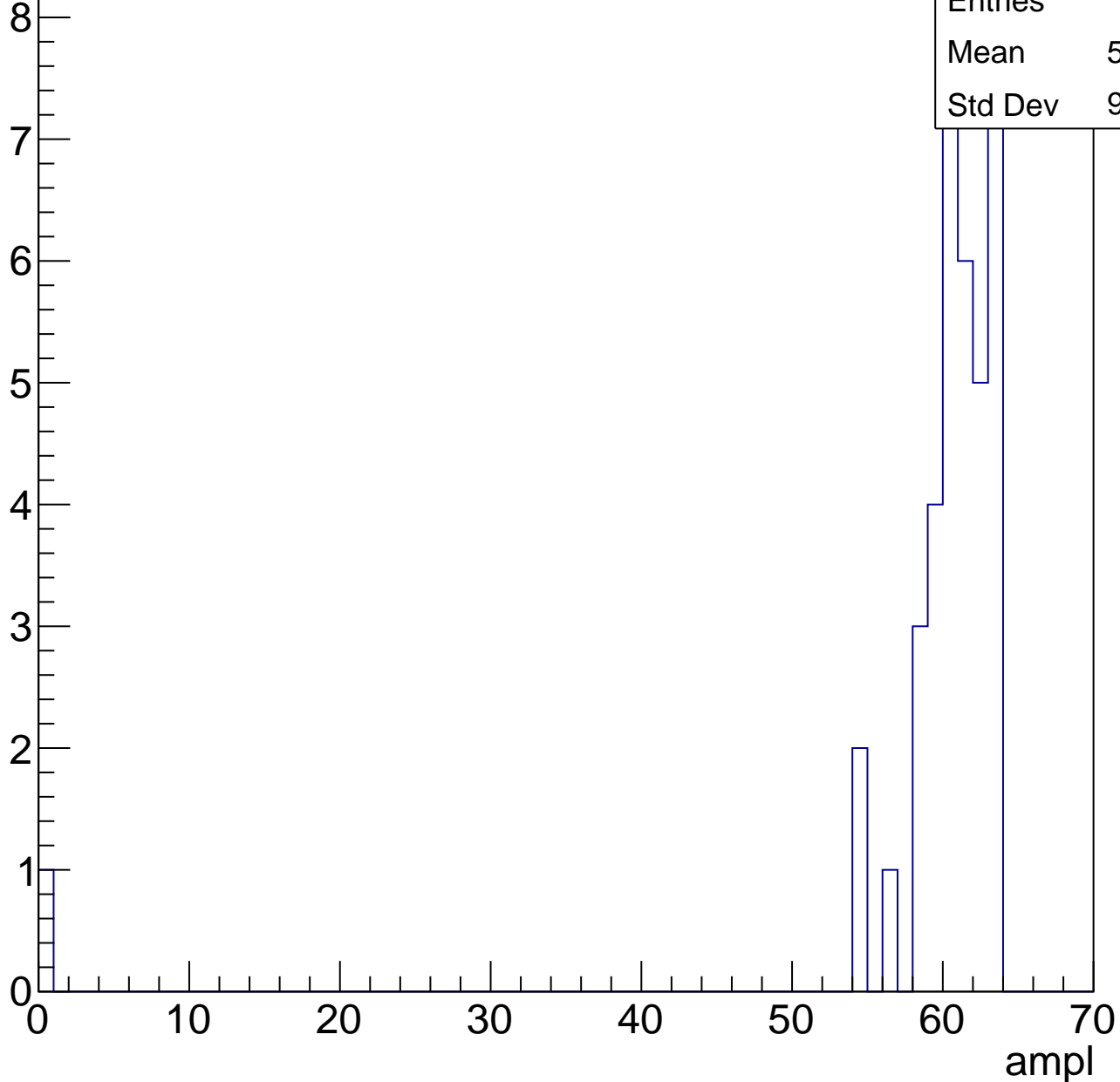


# B1L103S, U11-ch57, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	38
Mean	58.79
Std Dev	9.929



# B1L103S, U11-ch57, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U11-ch57, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L103S, U11-ch58, adc0

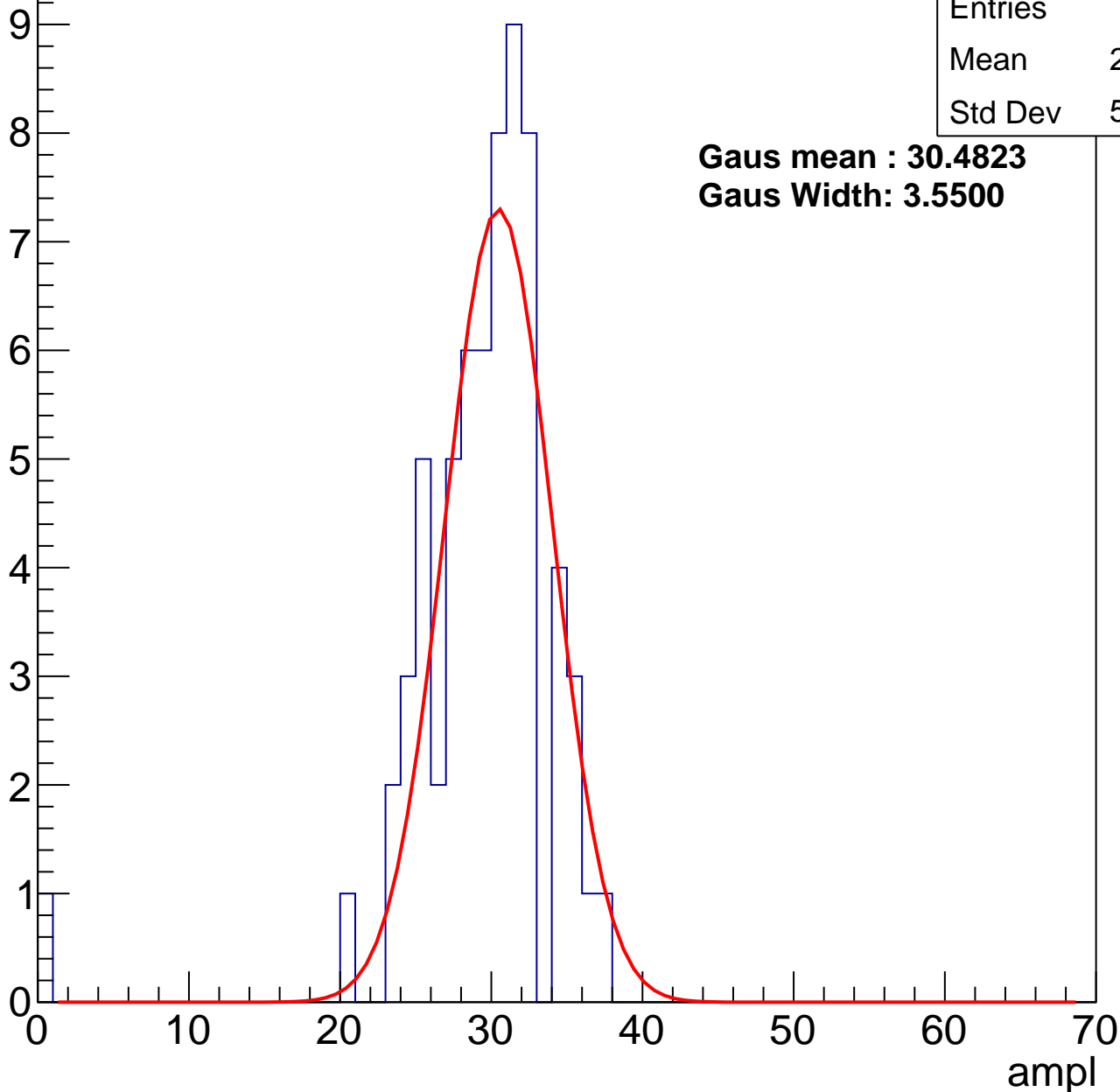
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	28.94
Std Dev	5.007

**Gaus mean : 30.4823**

**Gaus Width: 3.5500**



# B1L103S, U11-ch58, adc1

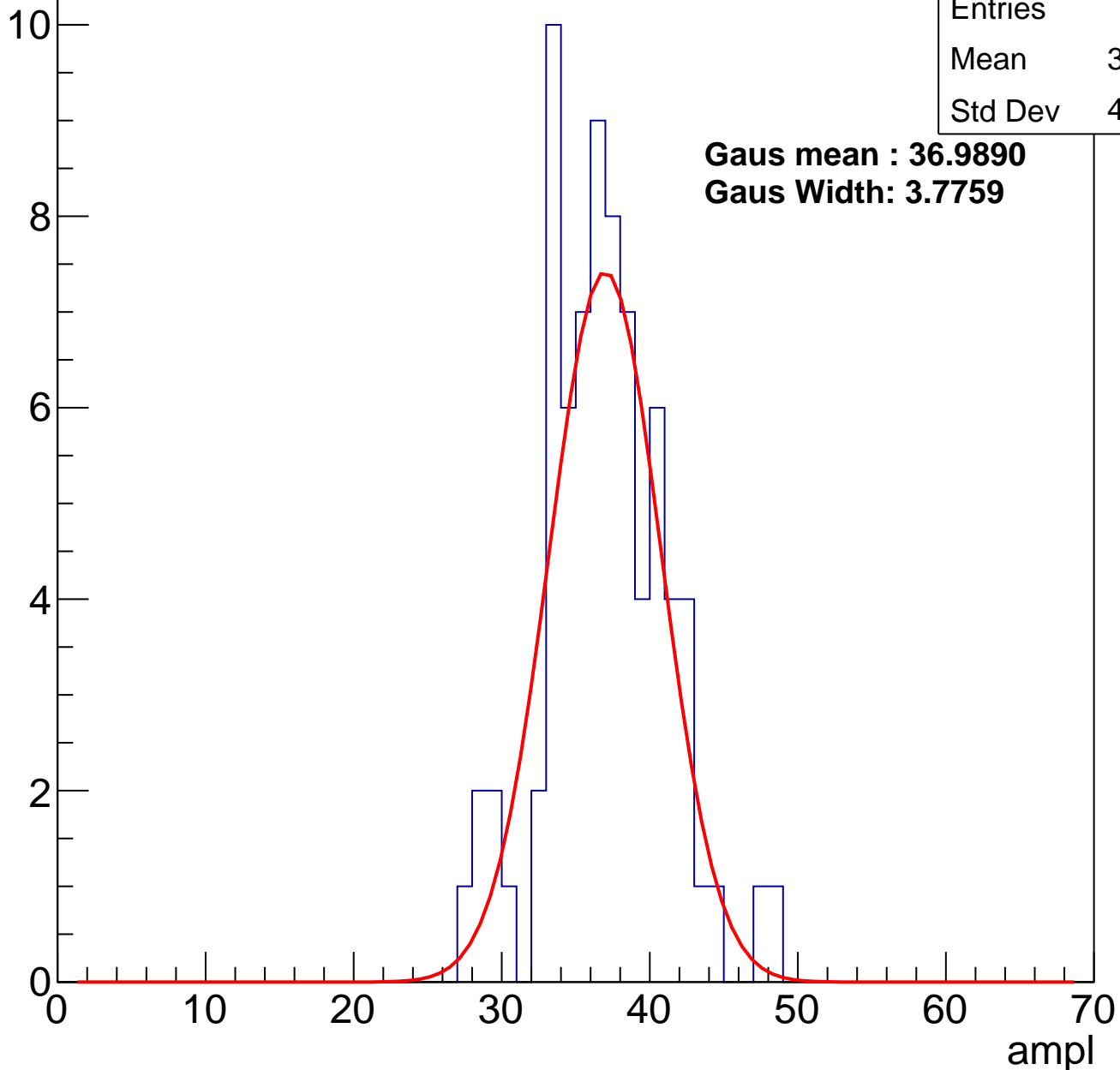
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	77
Mean	36.49
Std Dev	4.057

**Gaus mean : 36.9890**

**Gaus Width: 3.7759**

Entry



# B1L103S, U11-ch58, adc2

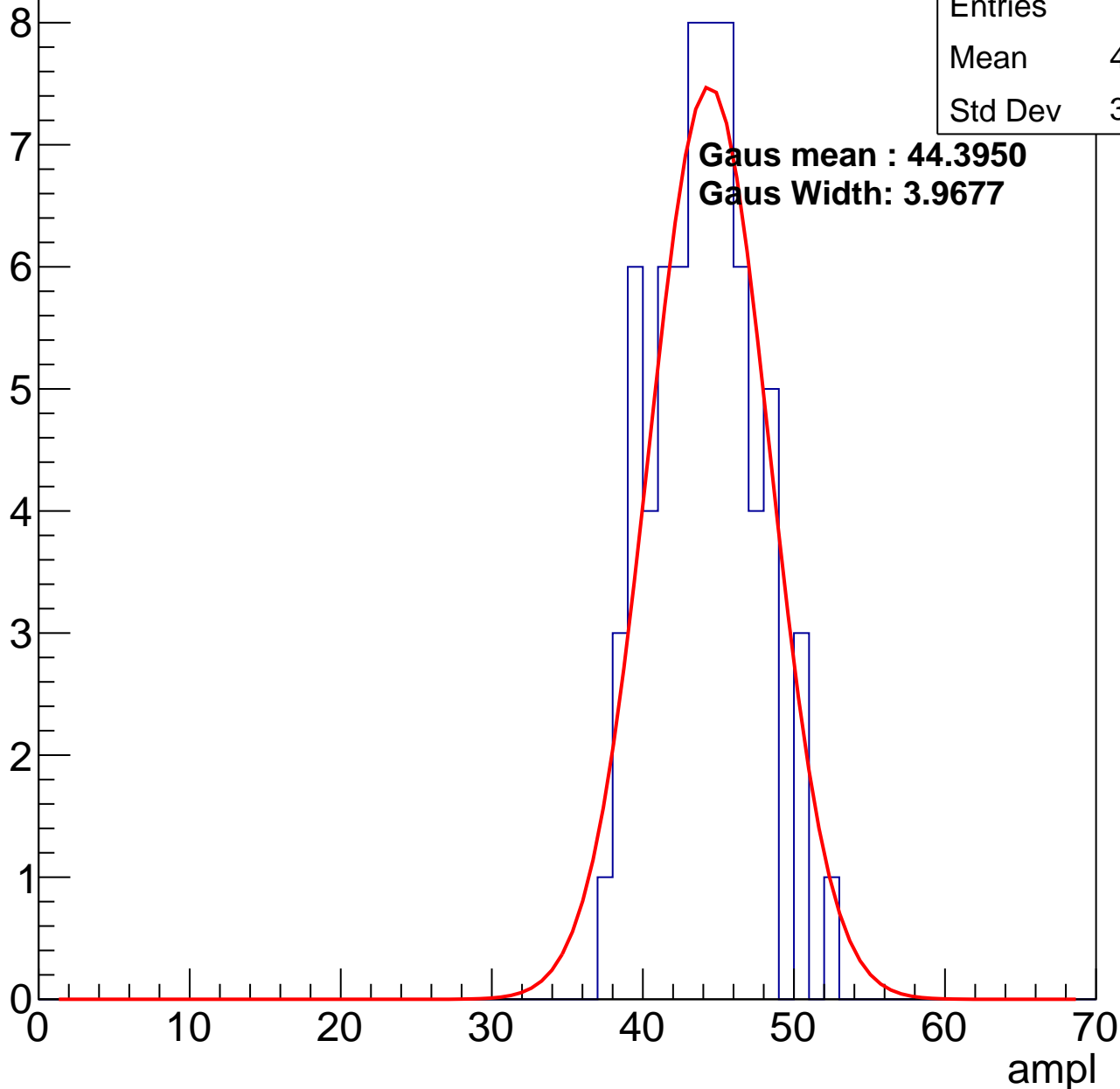
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	69
Mean	43.55
Std Dev	3.326

**Gaus mean : 44.3950**

**Gaus Width: 3.9677**

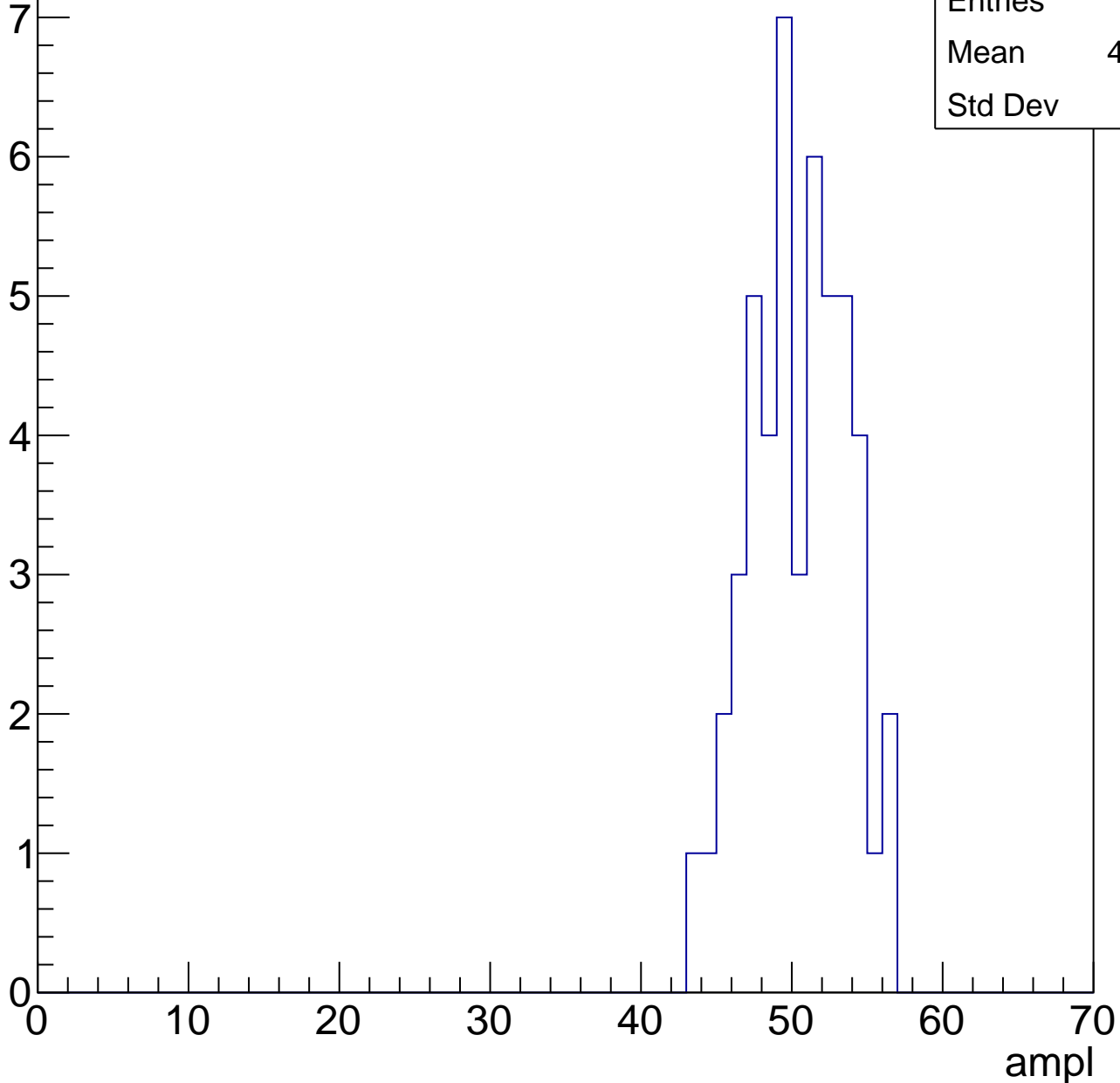


# B1L103S, U11-ch58, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	49
Mean	49.98
Std Dev	3.14

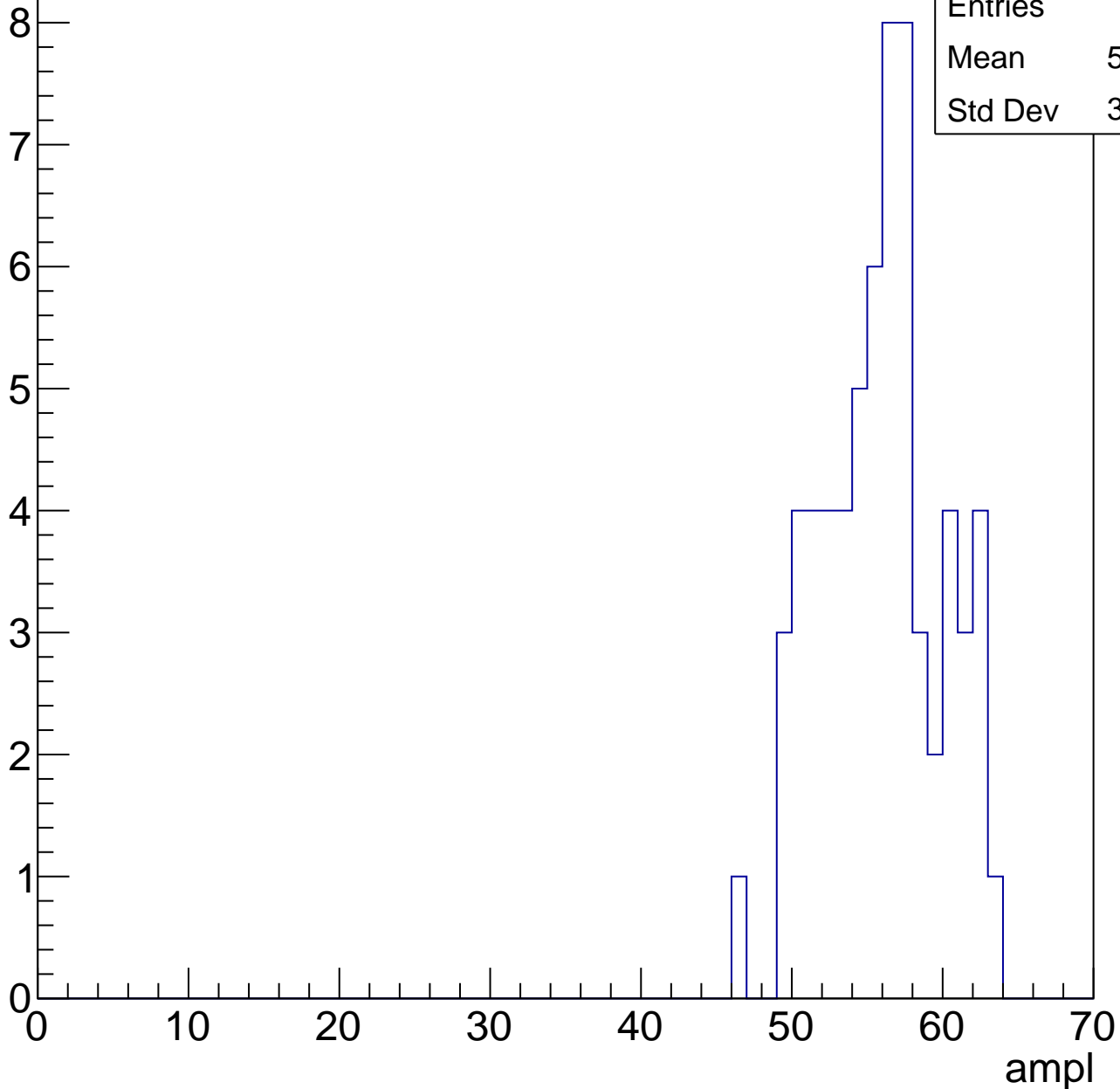


# B1L103S, U11-ch58, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

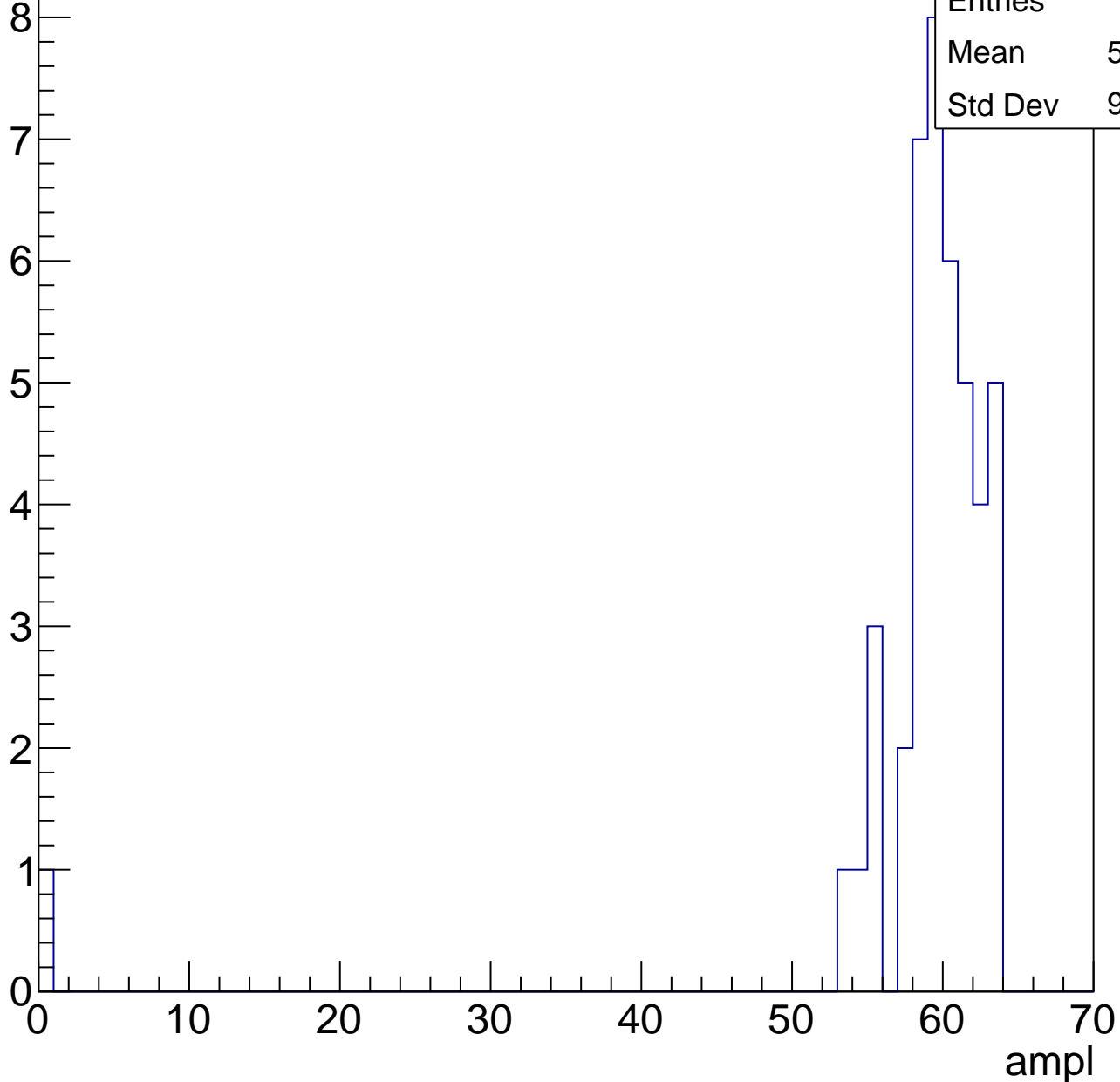
Entries	64
Mean	55.42
Std Dev	3.884



# B1L103S, U11-ch58, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U11-ch58, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U11-ch58, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U11-ch59, adc0

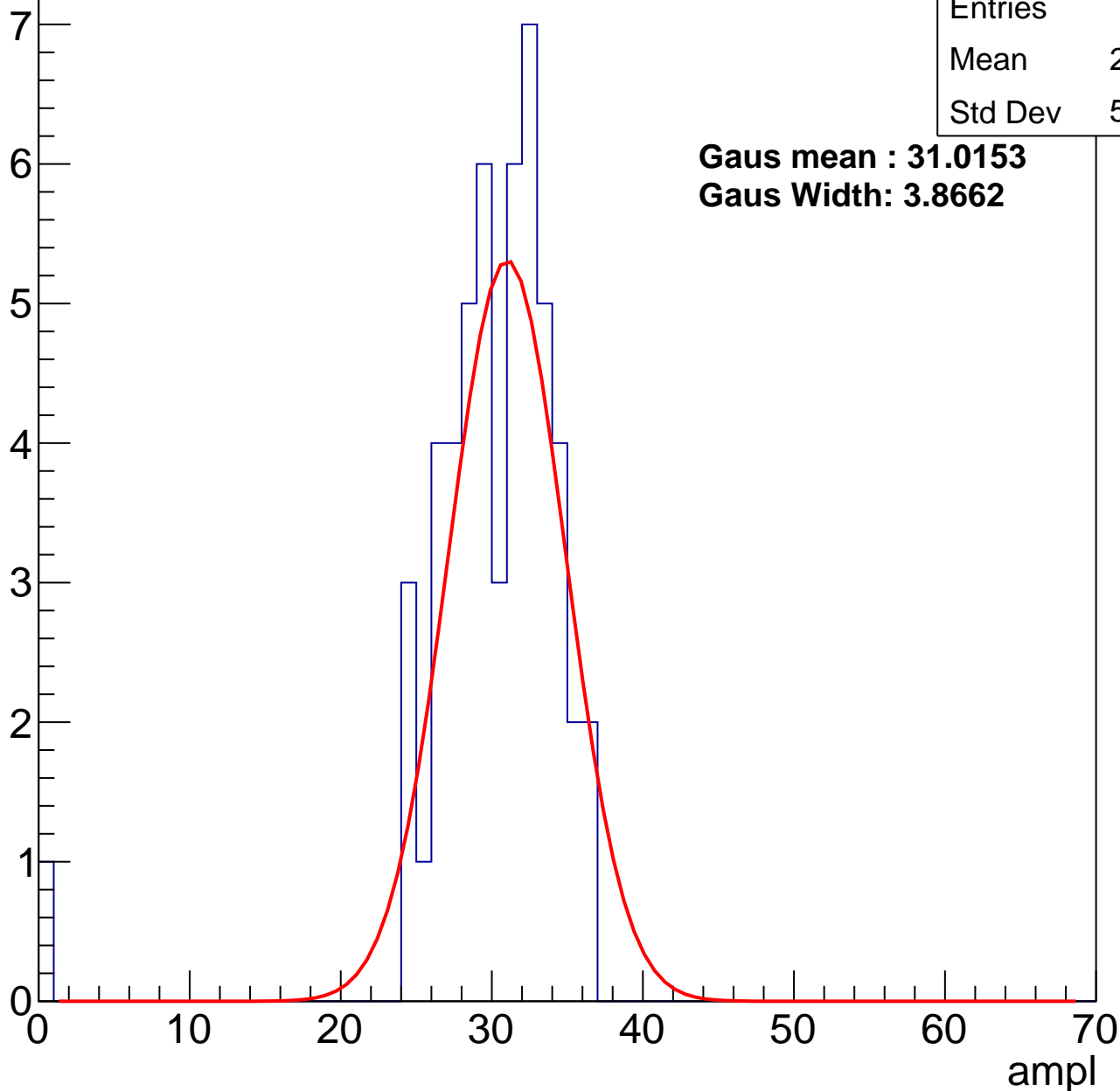
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	53
Mean	29.55
Std Dev	5.164

**Gaus mean : 31.0153**

**Gaus Width: 3.8662**



# B1L103S, U11-ch59, adc1

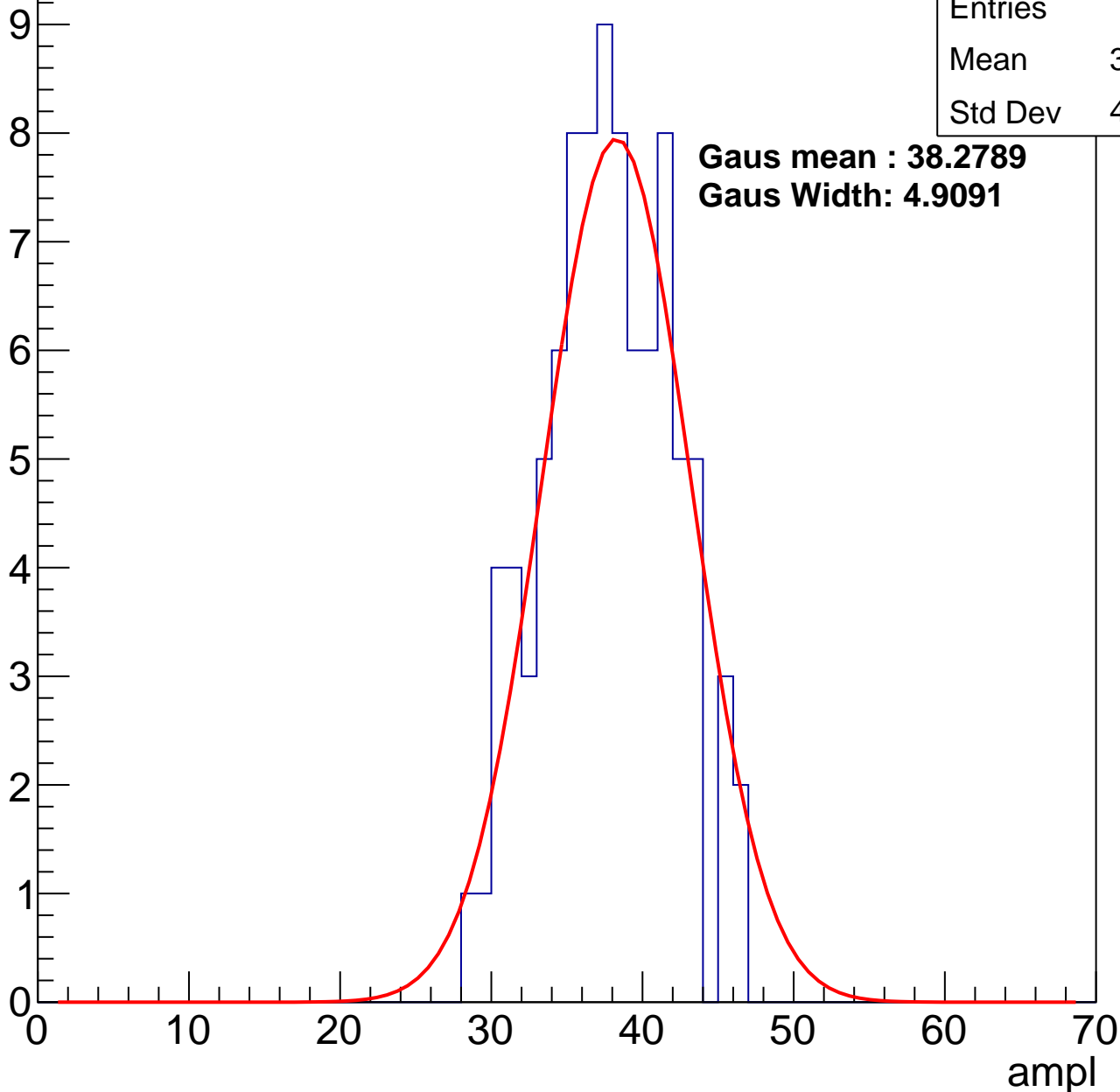
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	92
Mean	37.23
Std Dev	4.173

**Gaus mean : 38.2789**

**Gaus Width: 4.9091**



# B1L103S, U11-ch59, adc2

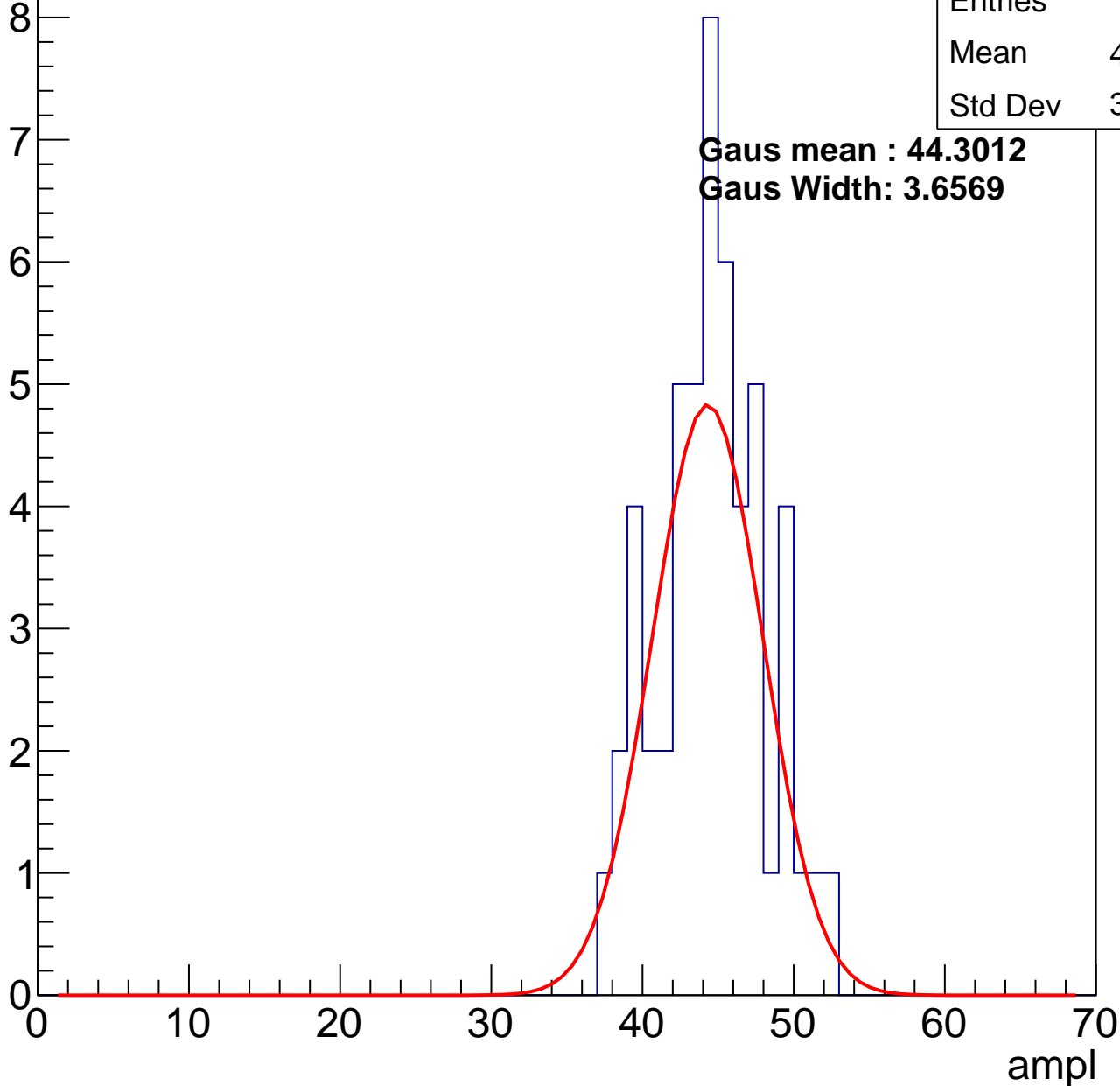
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	52
Mean	44.12
Std Dev	3.473

**Gaus mean : 44.3012**

**Gaus Width: 3.6569**

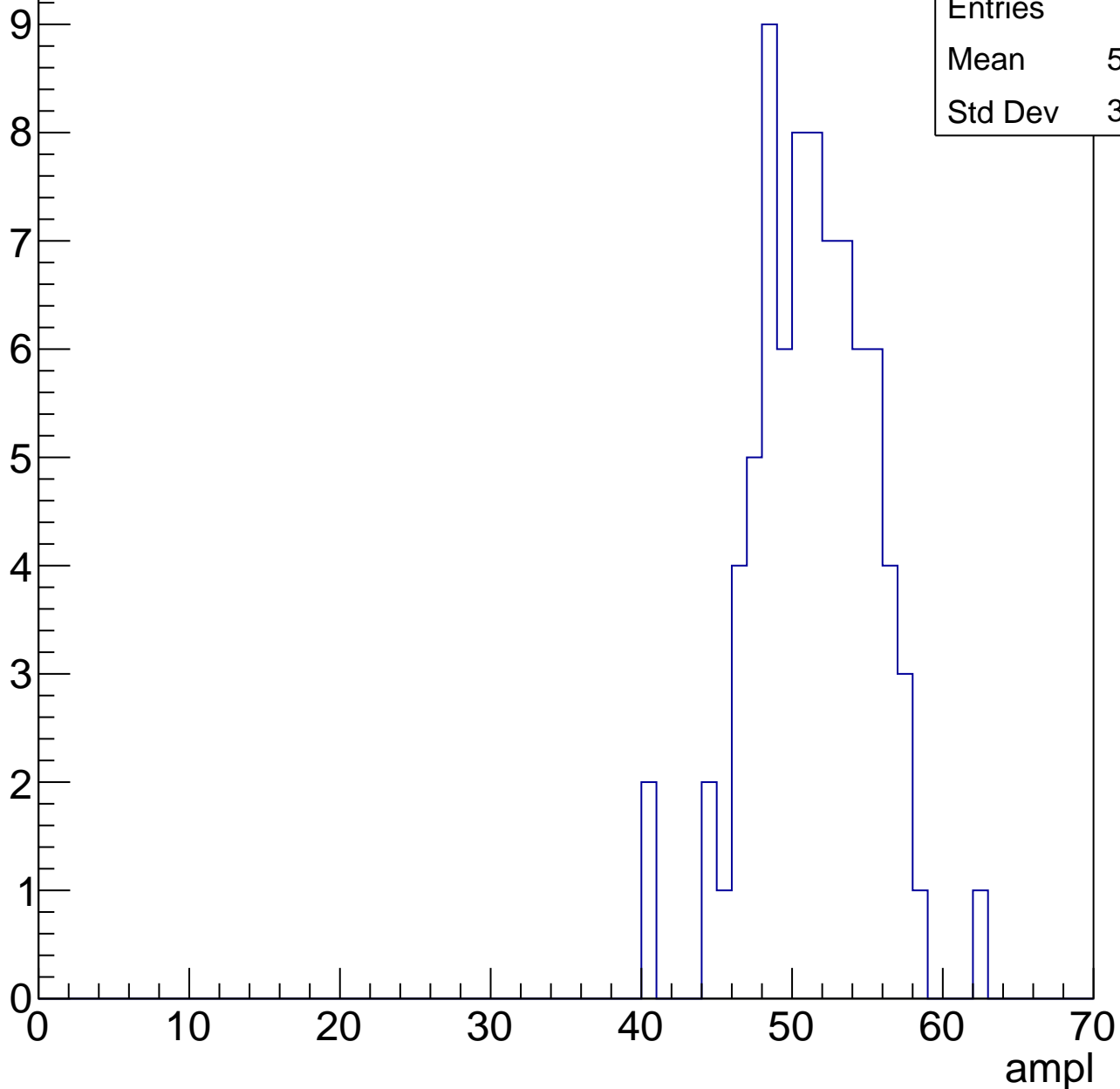


# B1L103S, U11-ch59, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	80
Mean	50.88
Std Dev	3.922

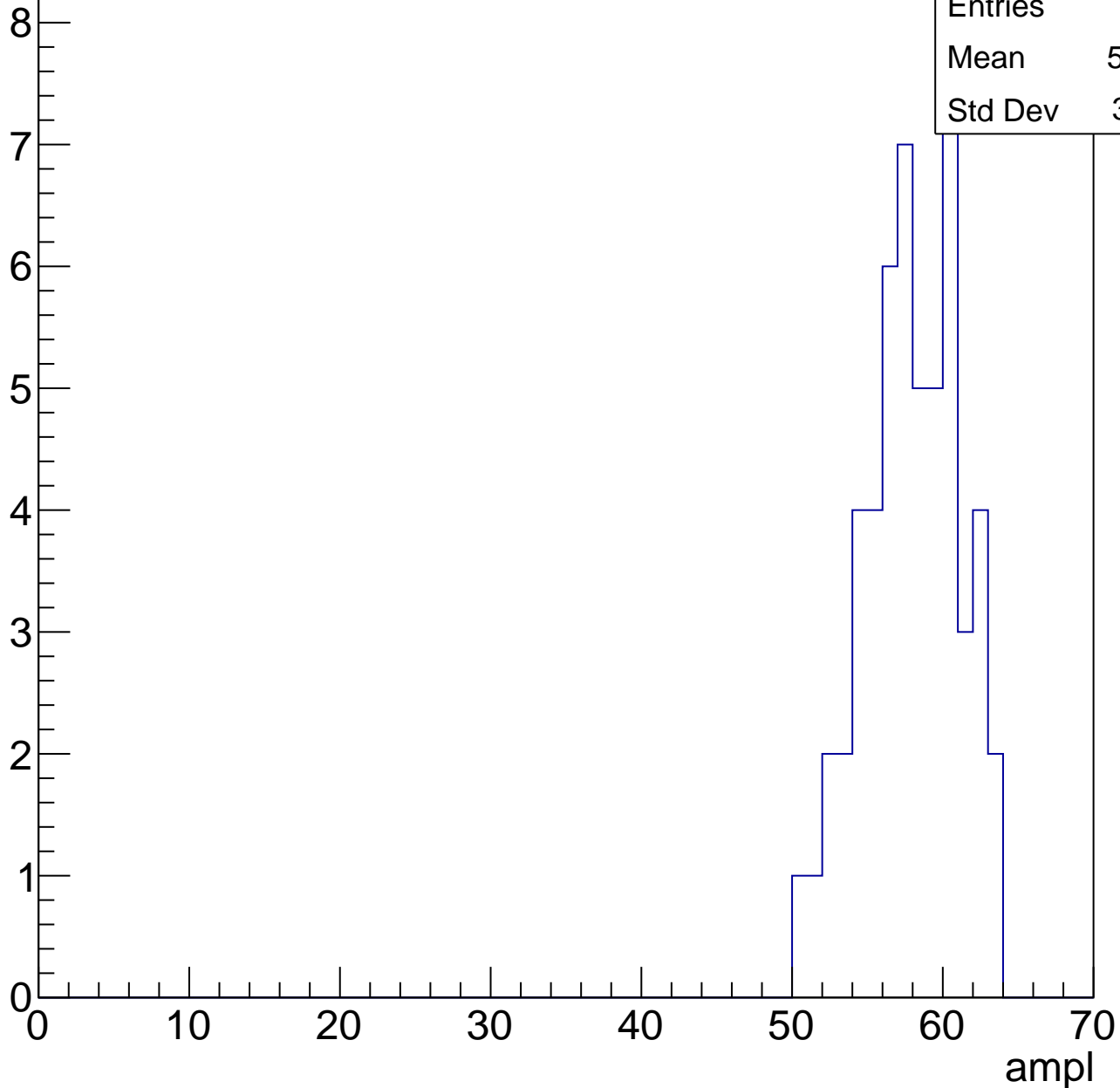


# B1L103S, U11-ch59, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	54
Mean	57.48
Std Dev	3.131

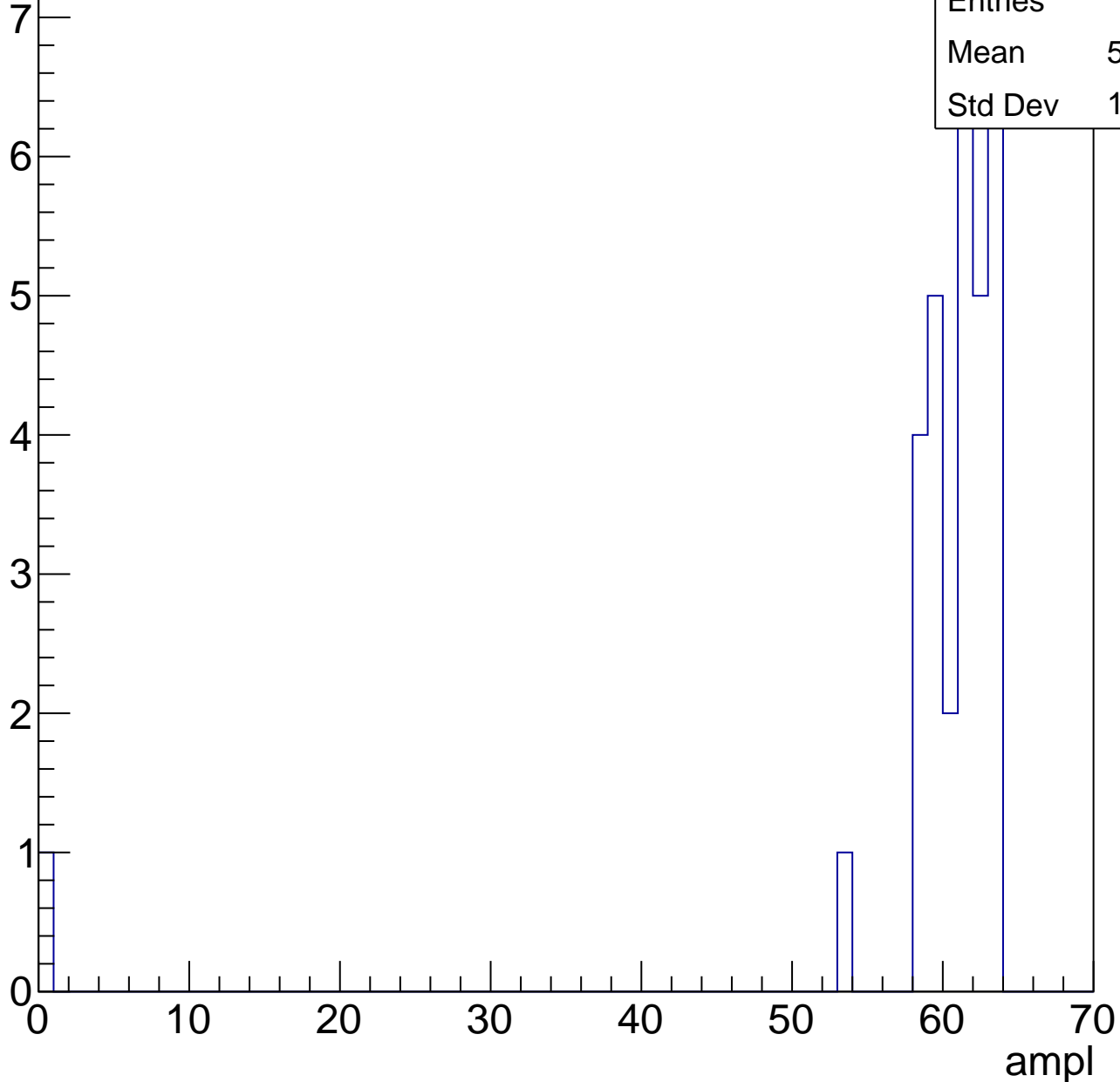


# B1L103S, U11-ch59, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	32
Mean	58.69
Std Dev	10.76



# B1L103S, U11-ch59, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	63
Std Dev	0



# B1L103S, U11-ch59, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U11-ch60, adc0

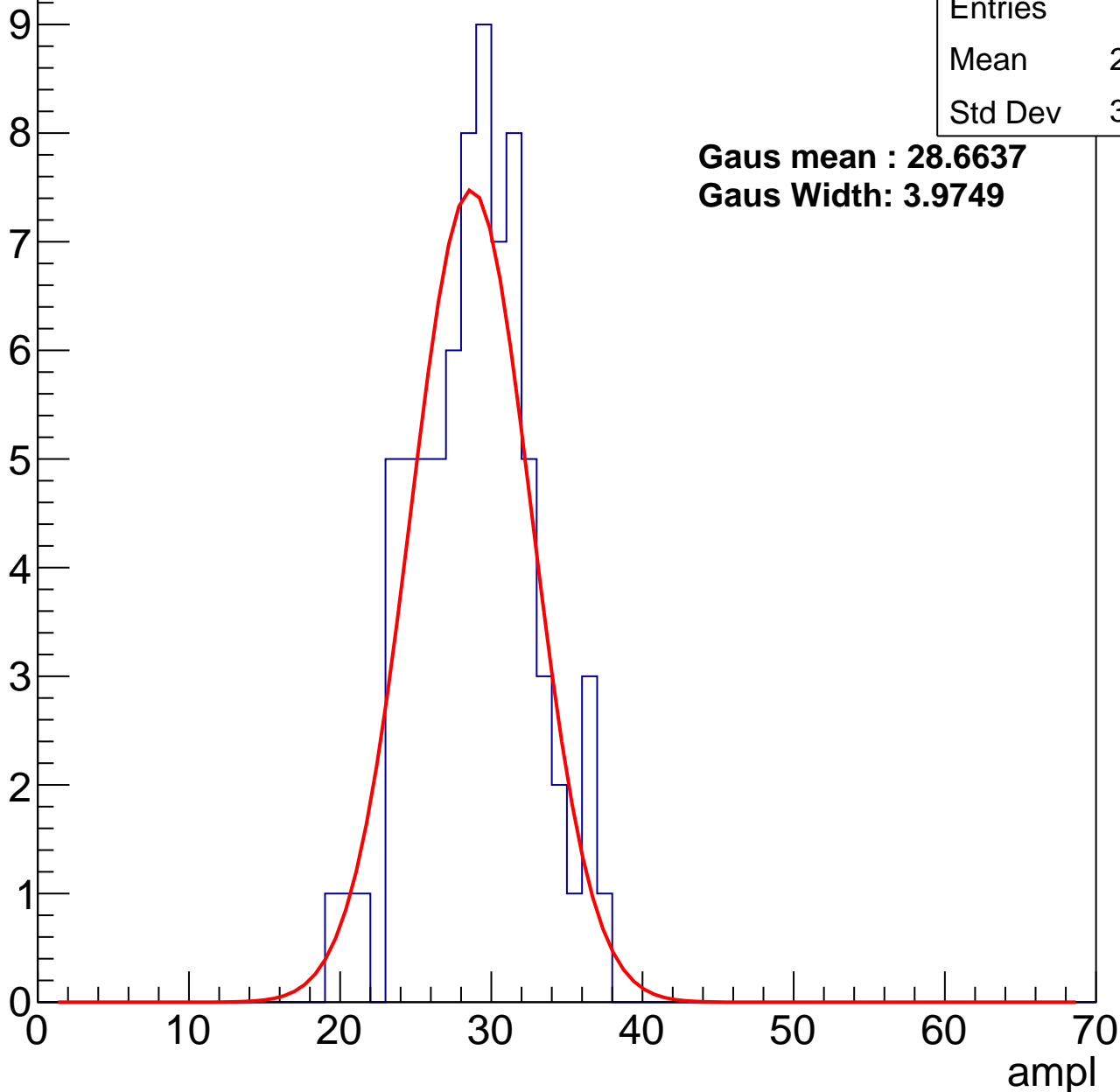
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	76
Mean	28.45
Std Dev	3.826

**Gaus mean : 28.6637**

**Gaus Width: 3.9749**



# B1L103S, U11-ch60, adc1

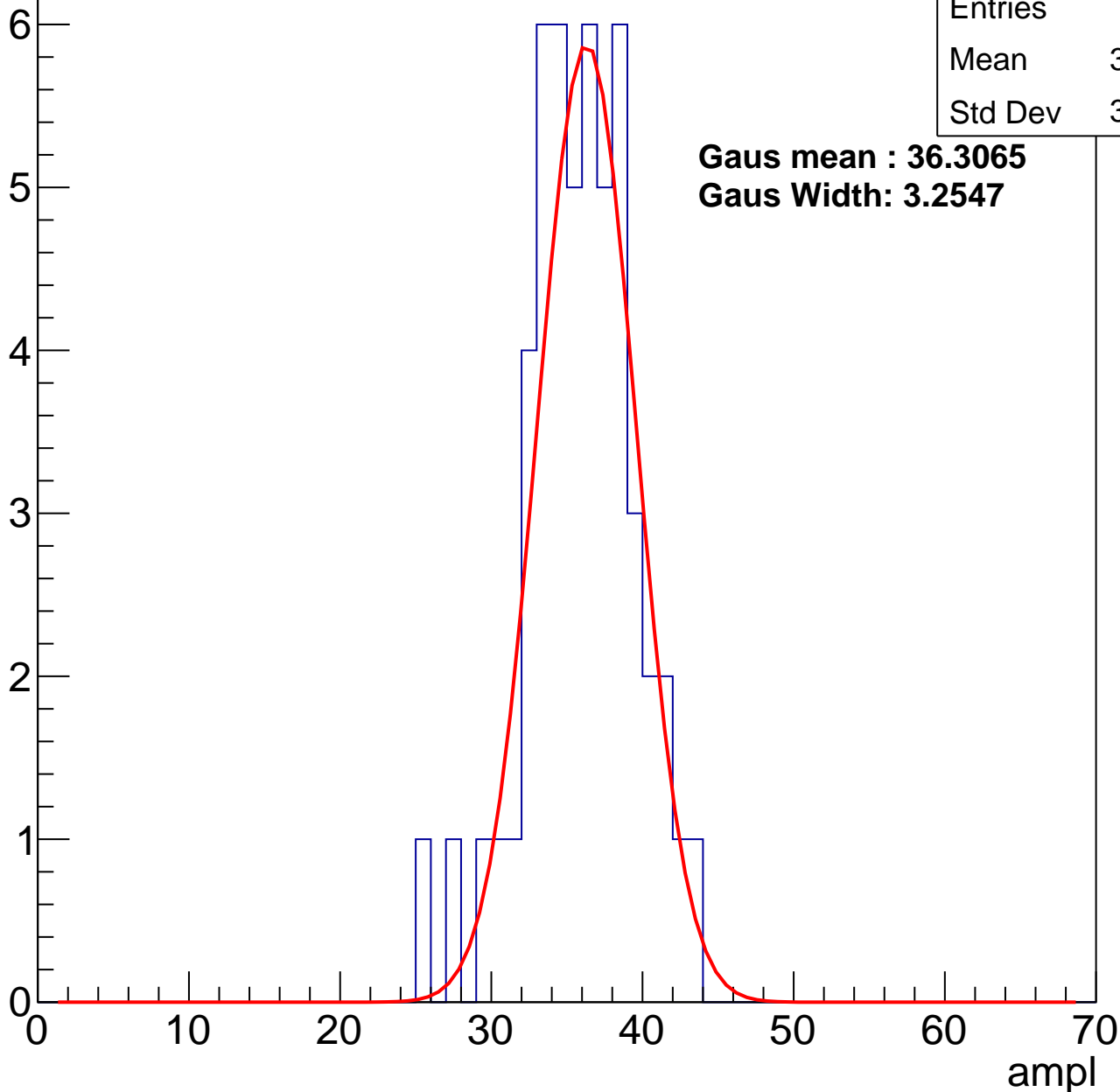
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	52
Mean	35.38
Std Dev	3.569

**Gaus mean : 36.3065**

**Gaus Width: 3.2547**



# B1L103S, U11-ch60, adc2

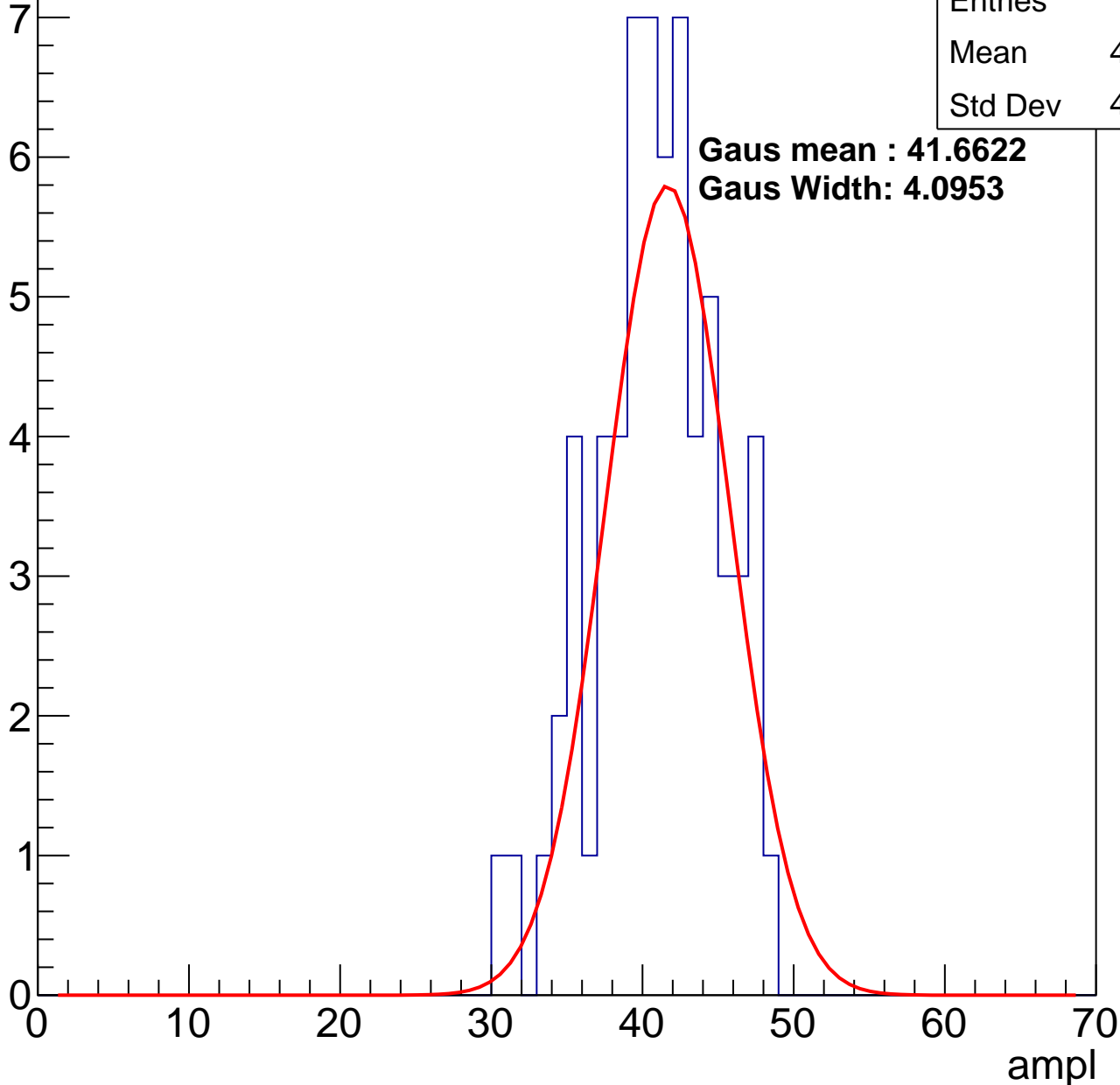
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	40.49
Std Dev	4.027

**Gaus mean : 41.6622**

**Gaus Width: 4.0953**

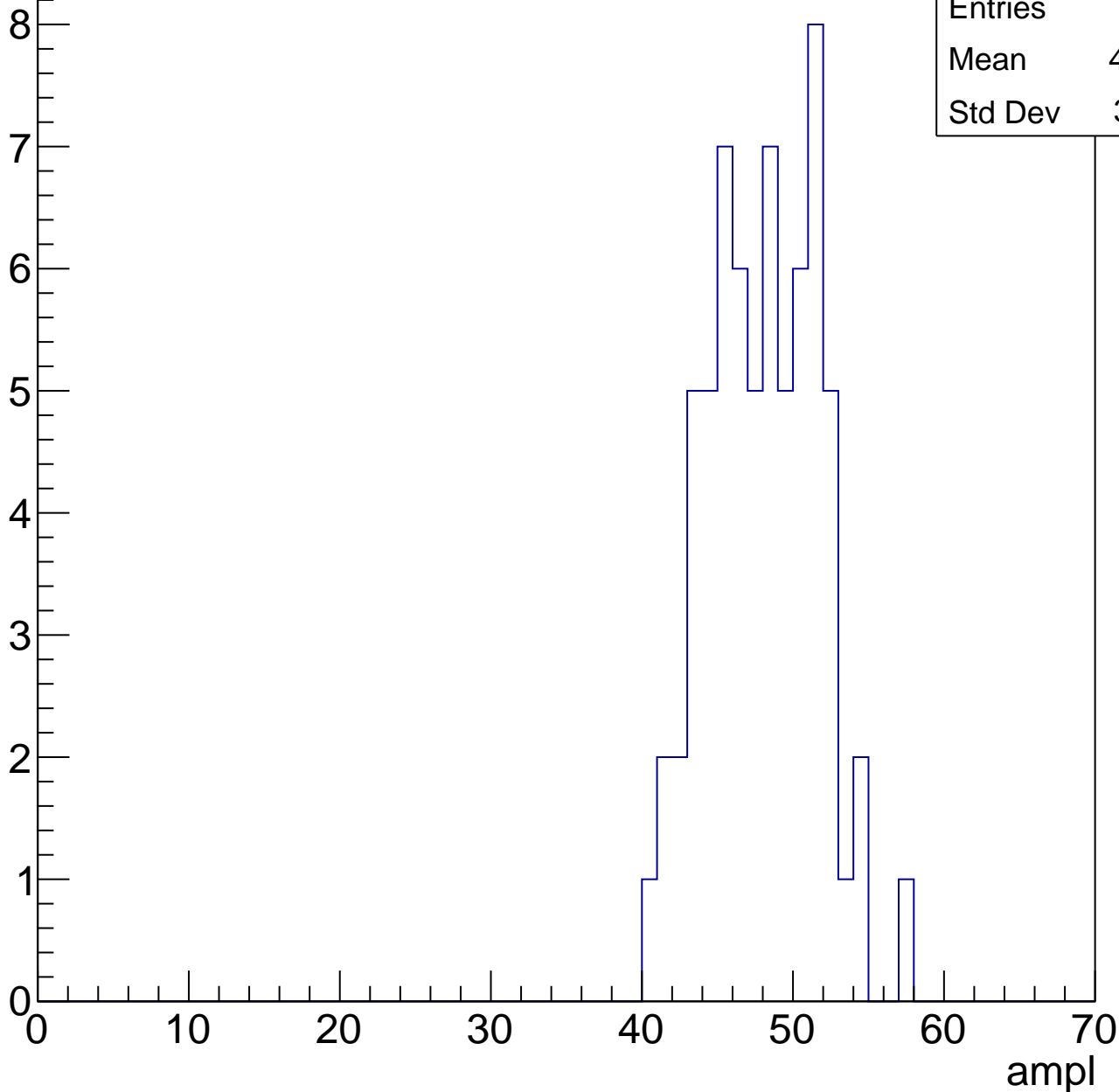


# B1L103S, U11-ch60, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	68
Mean	47.56
Std Dev	3.591

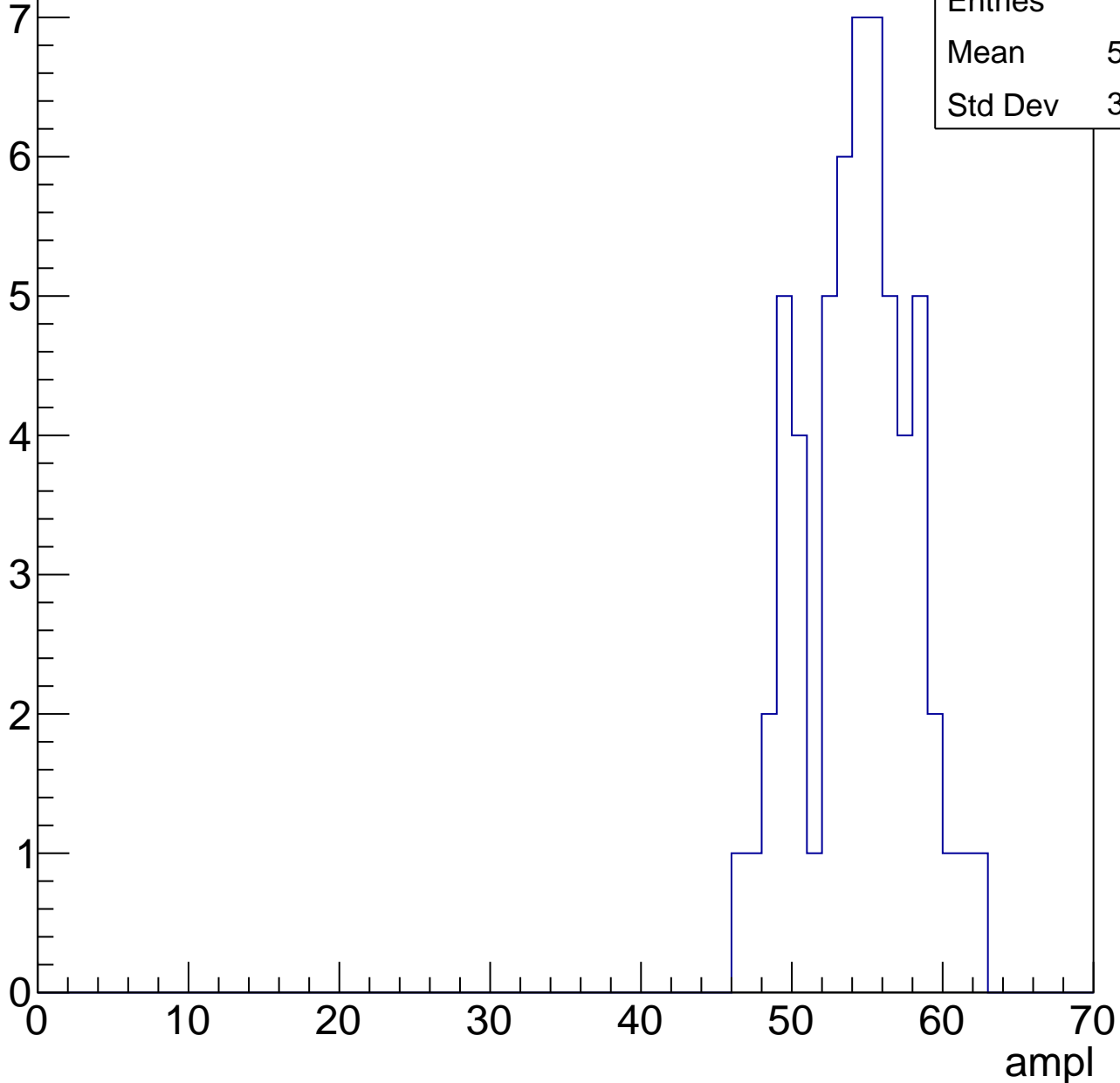


# B1L103S, U11-ch60, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	58
Mean	53.88
Std Dev	3.596

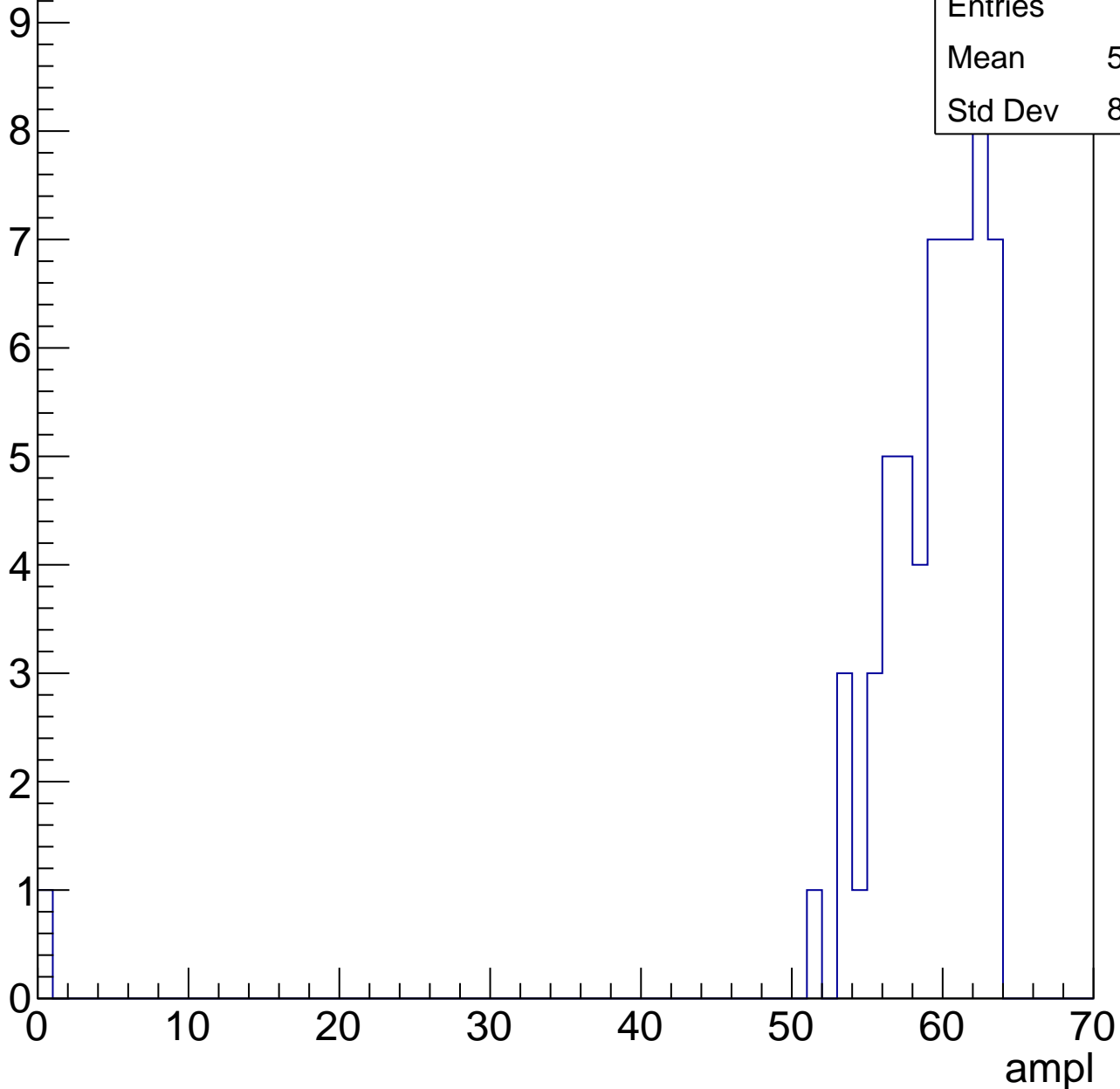


# B1L103S, U11-ch60, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	60
Mean	58.08
Std Dev	8.137



# B1L103S, U11-ch60, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

3

2.5

2

1.5

1

0.5

0

0

10

20

30

40

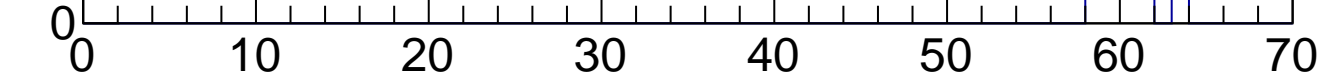
50

60

70

ampl

Entries	9
Mean	60.89
Std Dev	1.728





# B1L103S, U11-ch60, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U11-ch61, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	73
Mean	28.1
Std Dev	5.805

**Gaus mean : 29.0577**

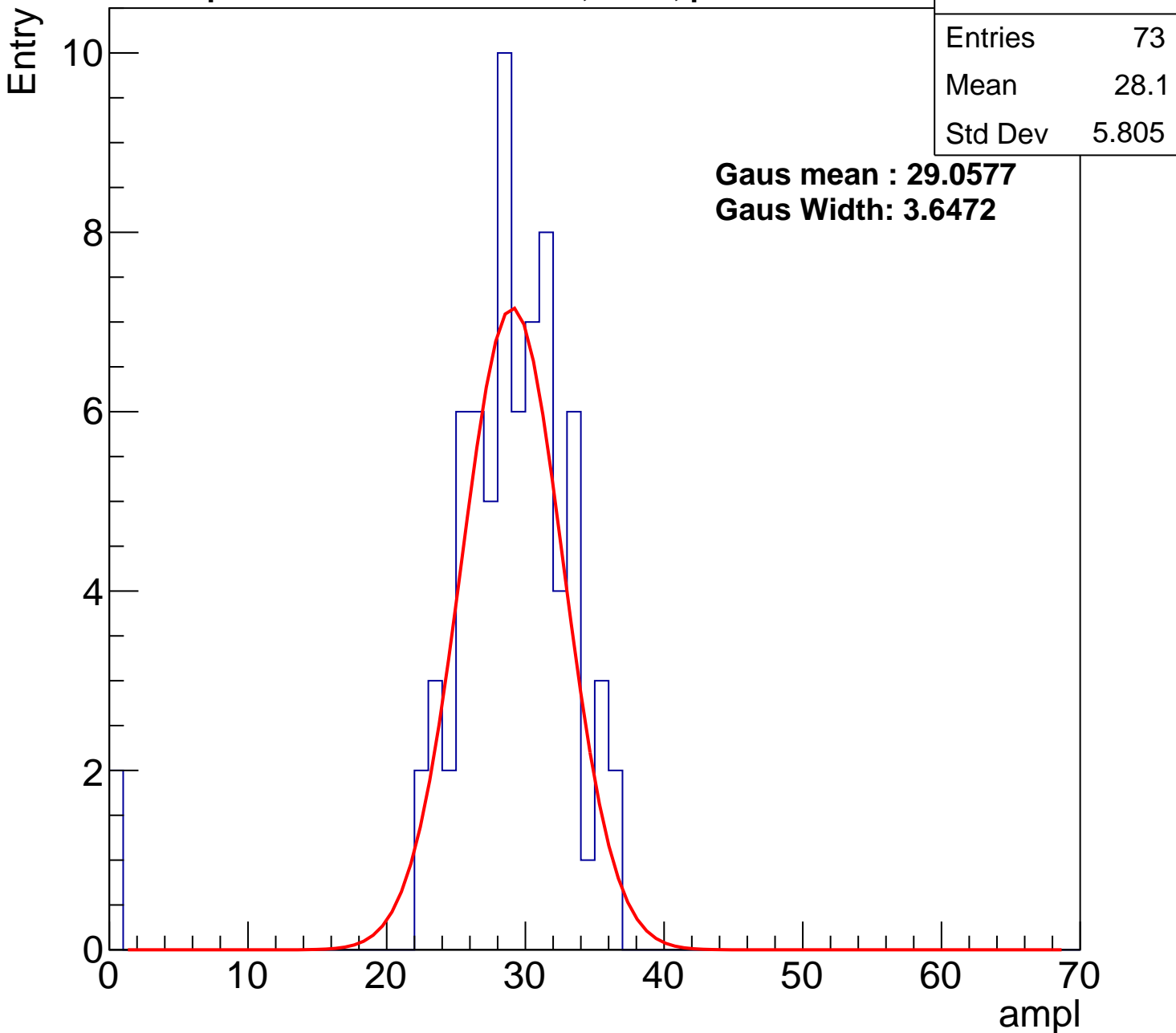
**Gaus Width: 3.6472**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U11-ch61, adc1

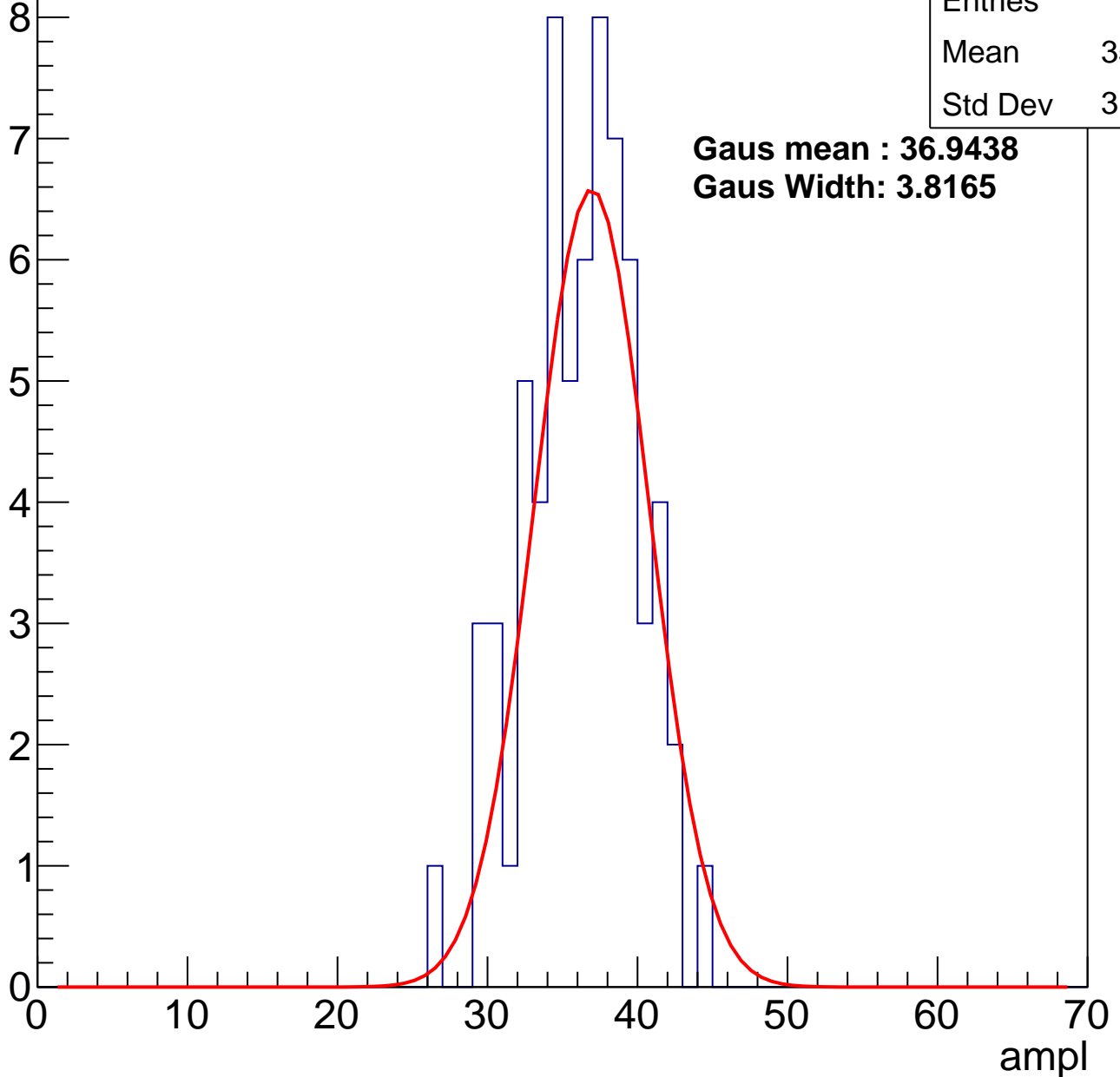
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	35.78
Std Dev	3.672

**Gaus mean : 36.9438**

**Gaus Width: 3.8165**



# B1L103S, U11-ch61, adc2

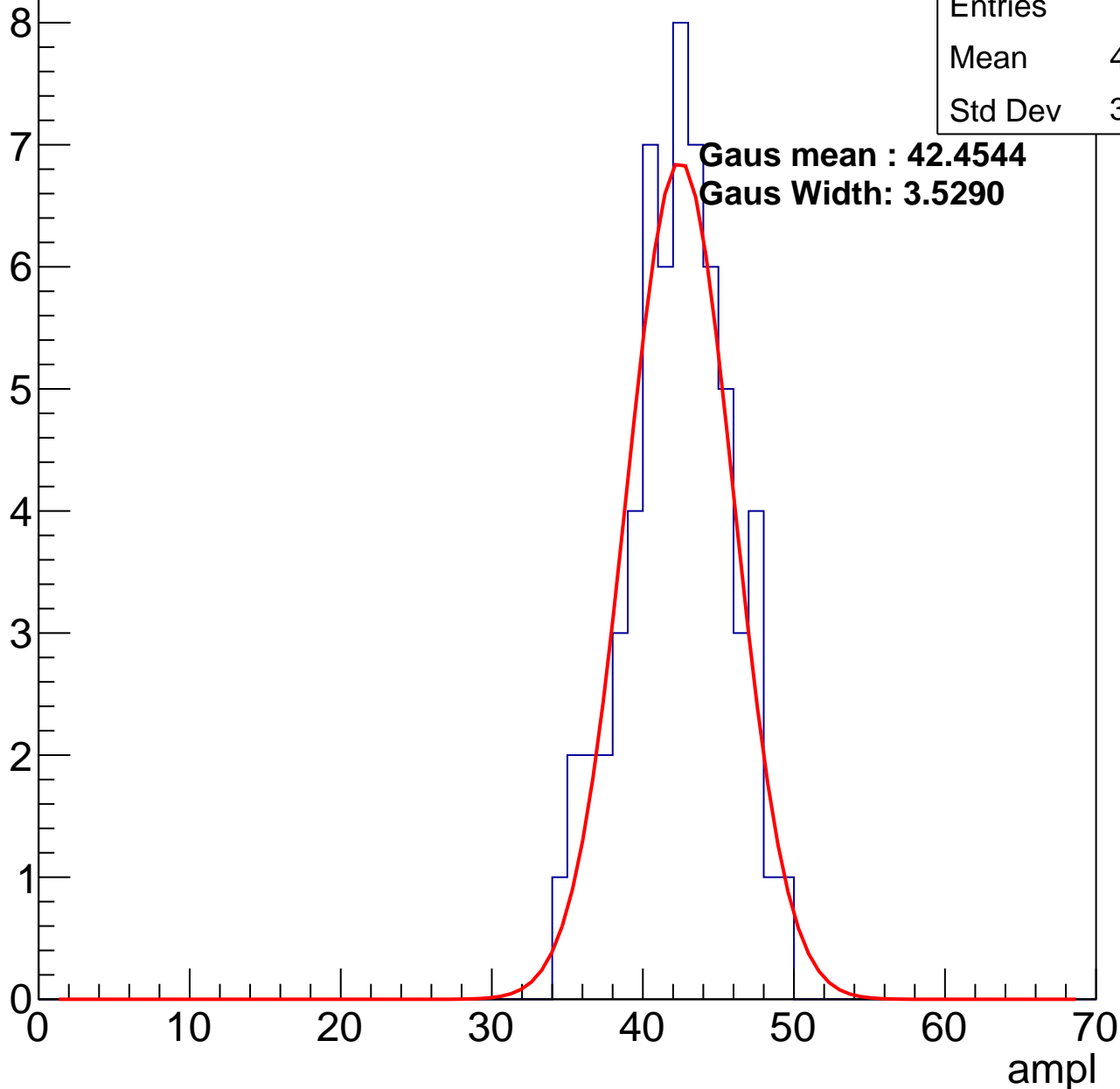
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	41.85
Std Dev	3.383

**Gaus mean : 42.4544**

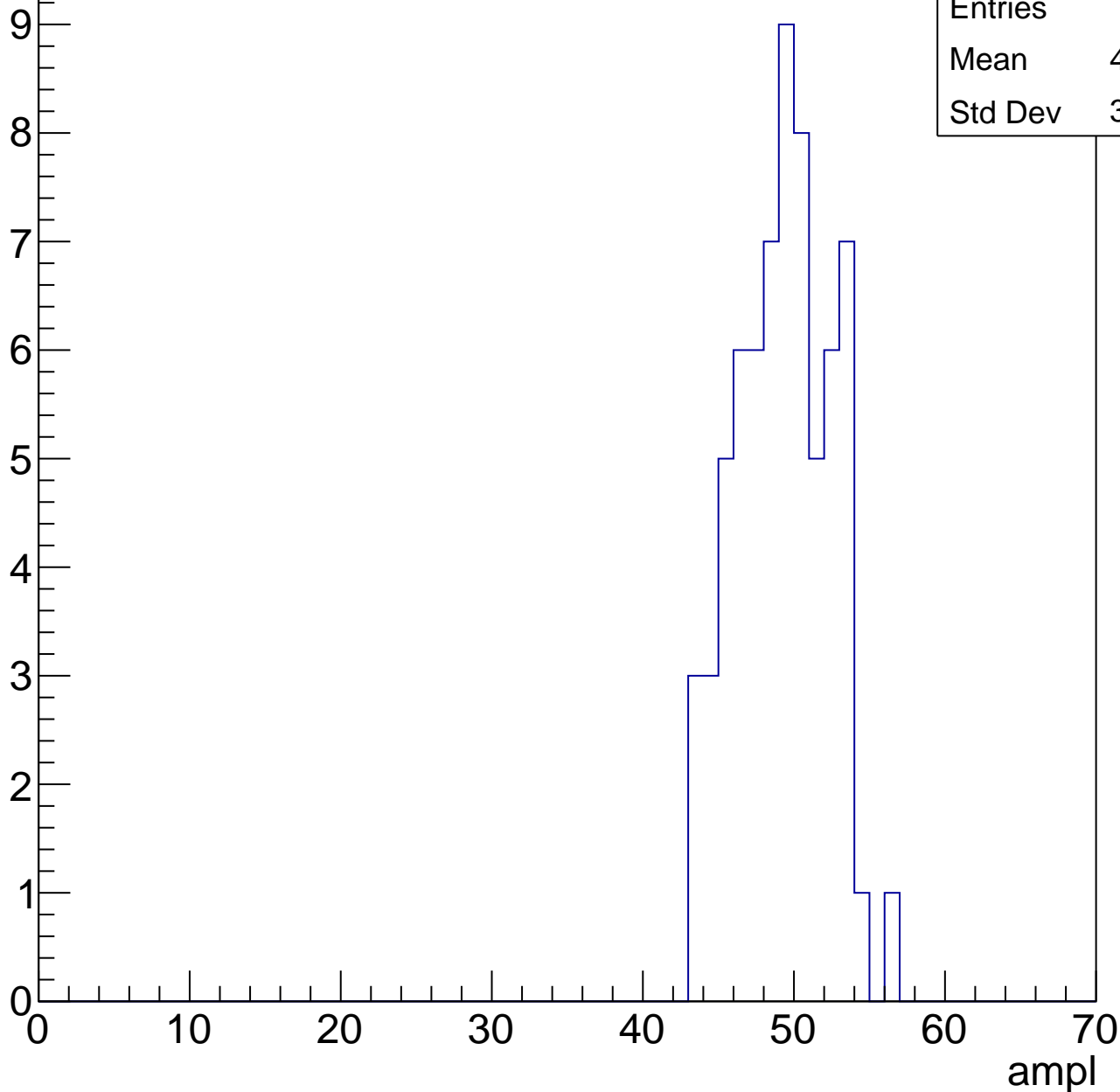
**Gaus Width: 3.5290**



# B1L103S, U11-ch61, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

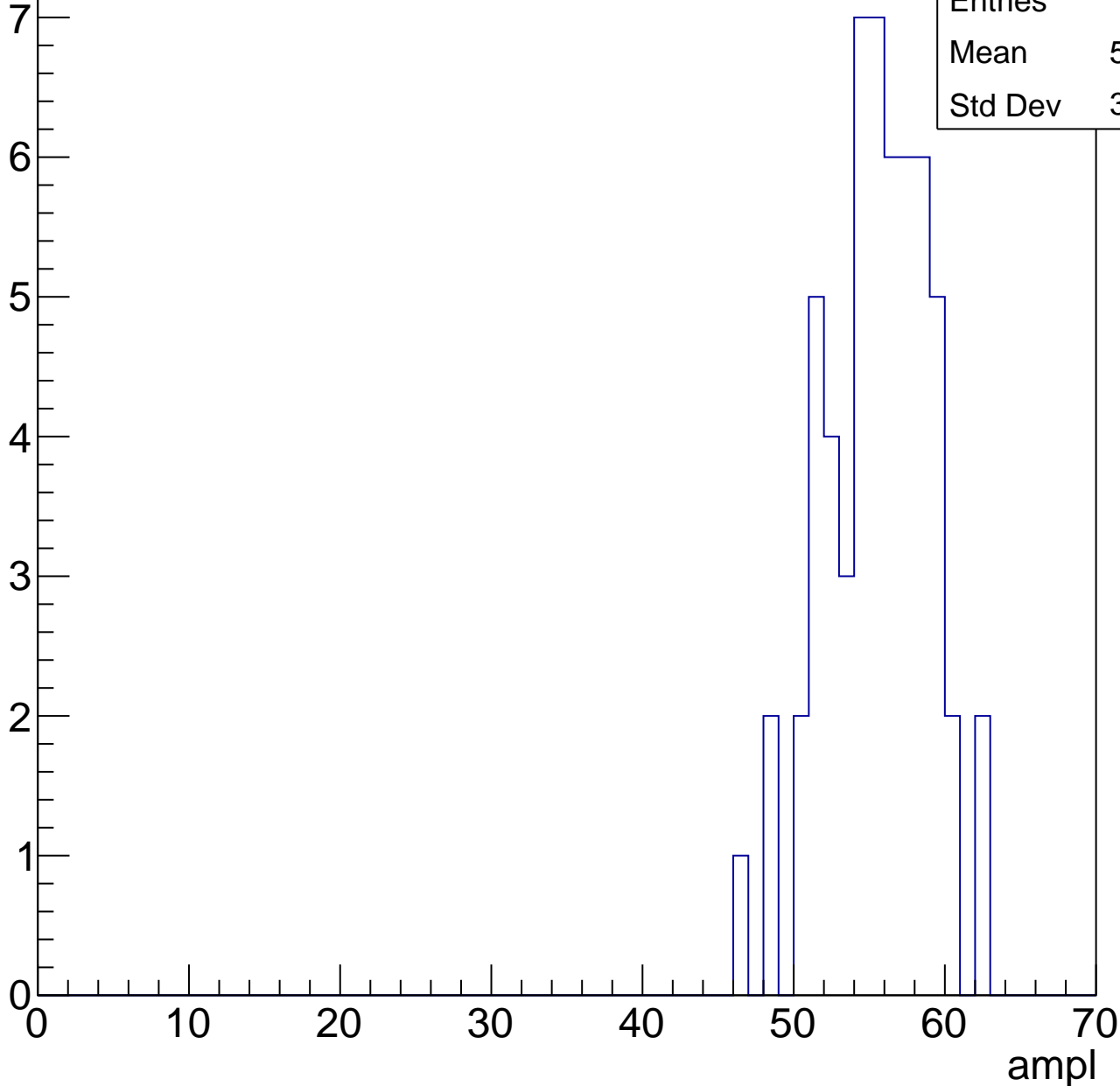


# B1L103S, U11-ch61, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	58
Mean	55.03
Std Dev	3.414

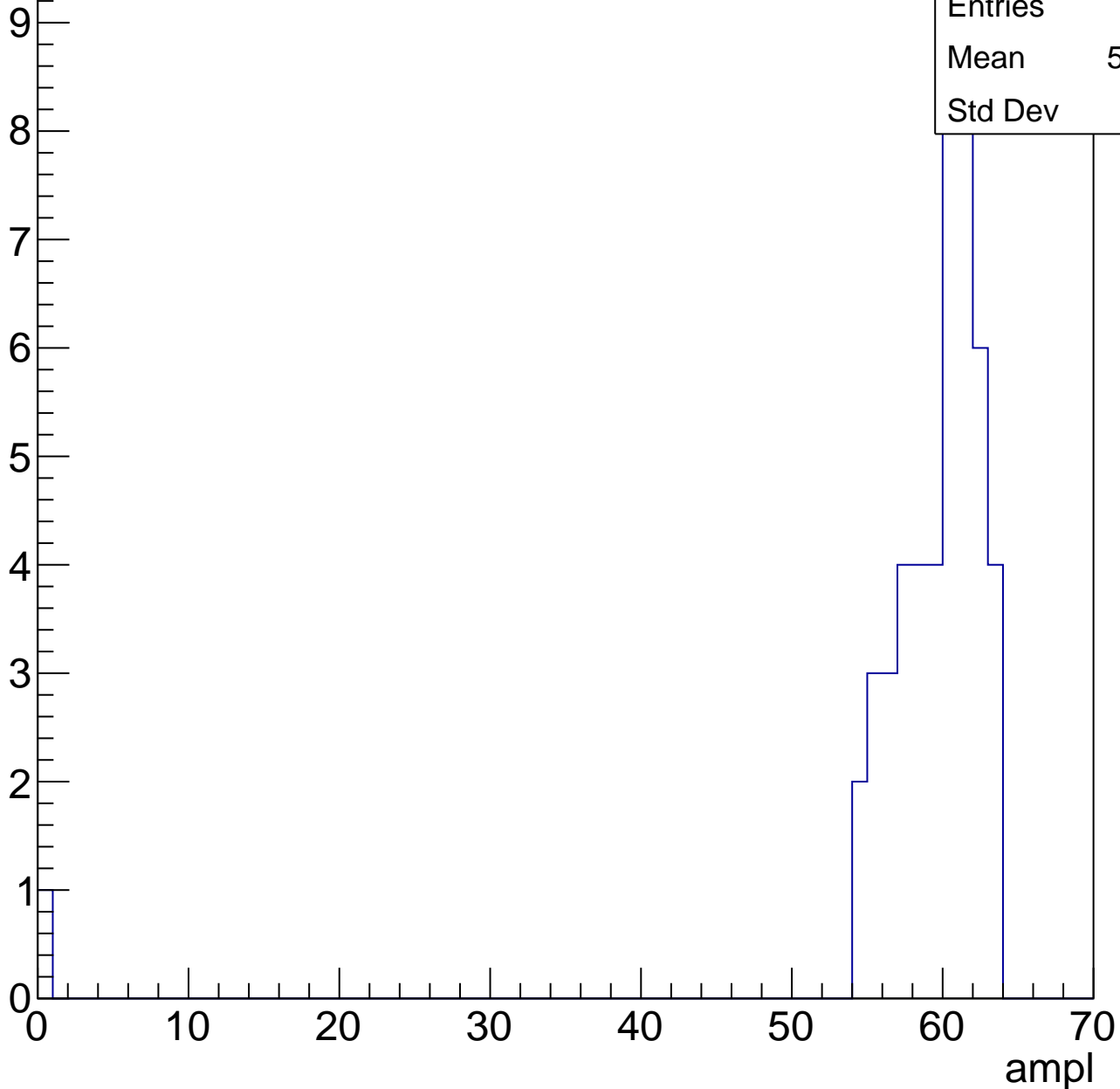


# B1L103S, U11-ch61, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	48
Mean	58.12
Std Dev	8.84

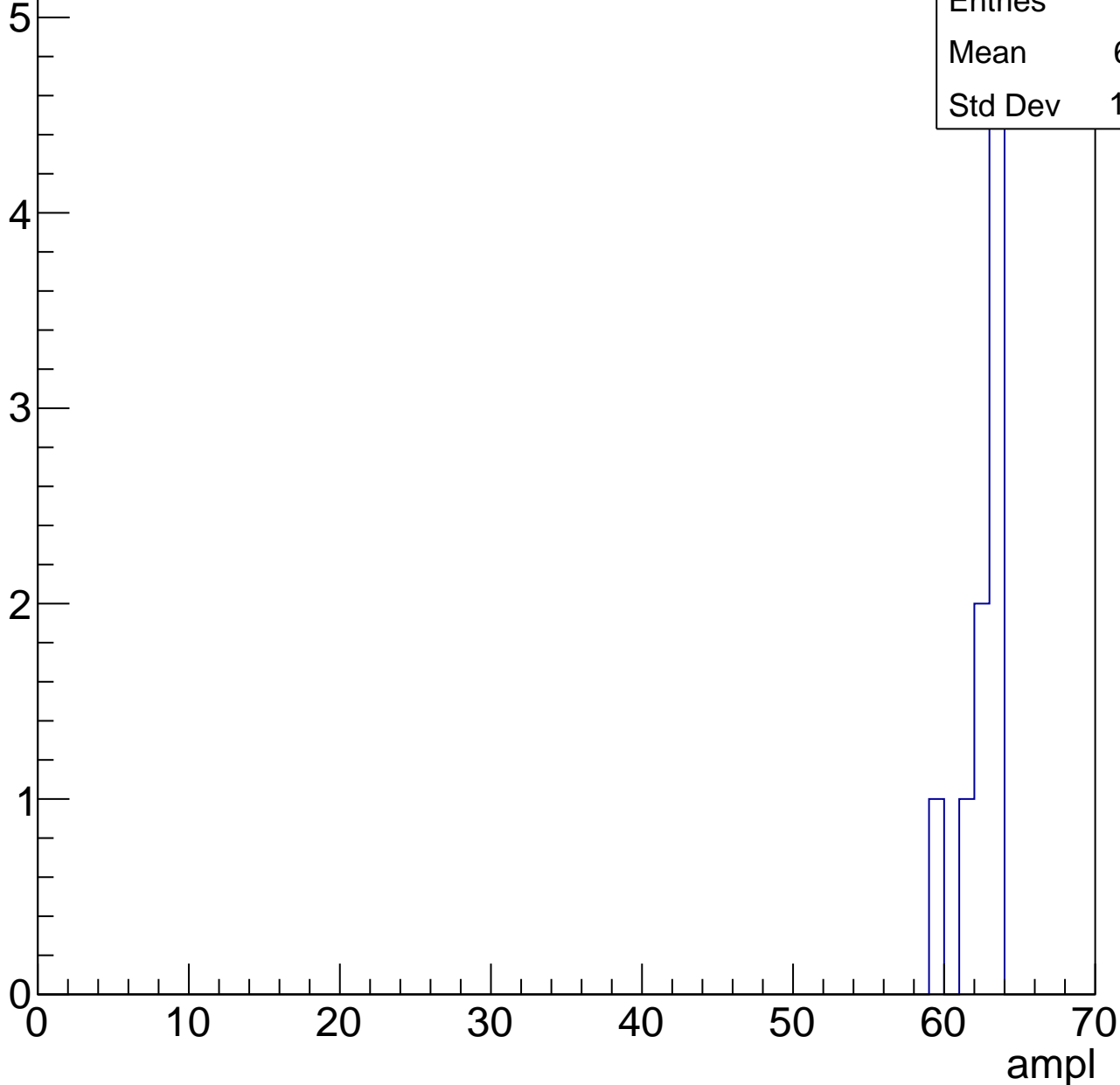


# B1L103S, U11-ch61, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	9
Mean	62.11
Std Dev	1.286





# B1L103S, U11-ch61, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U11-ch62, adc0

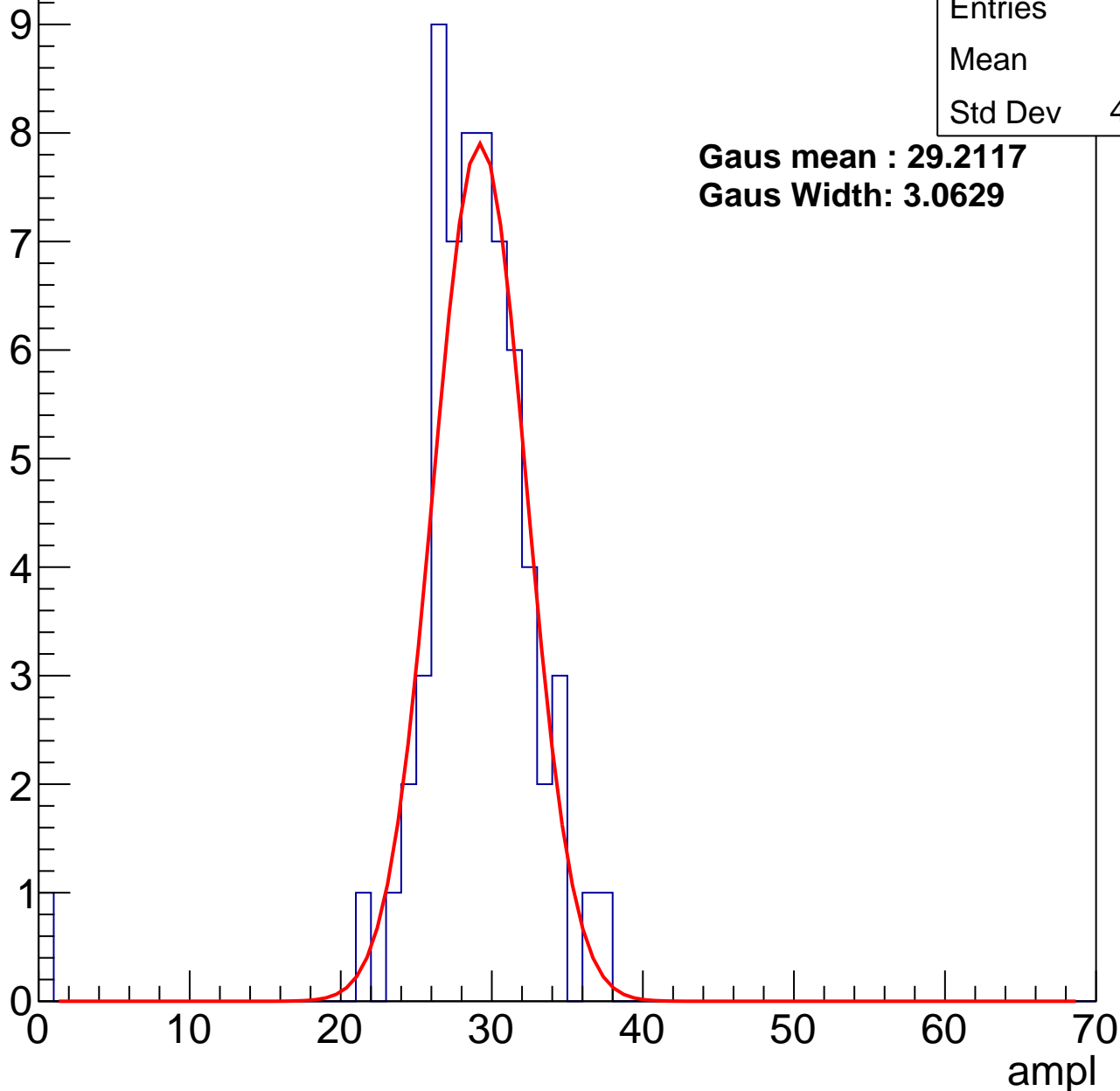
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	28.3
Std Dev	4.696

**Gaus mean : 29.2117**

**Gaus Width: 3.0629**



# B1L103S, U11-ch62, adc1

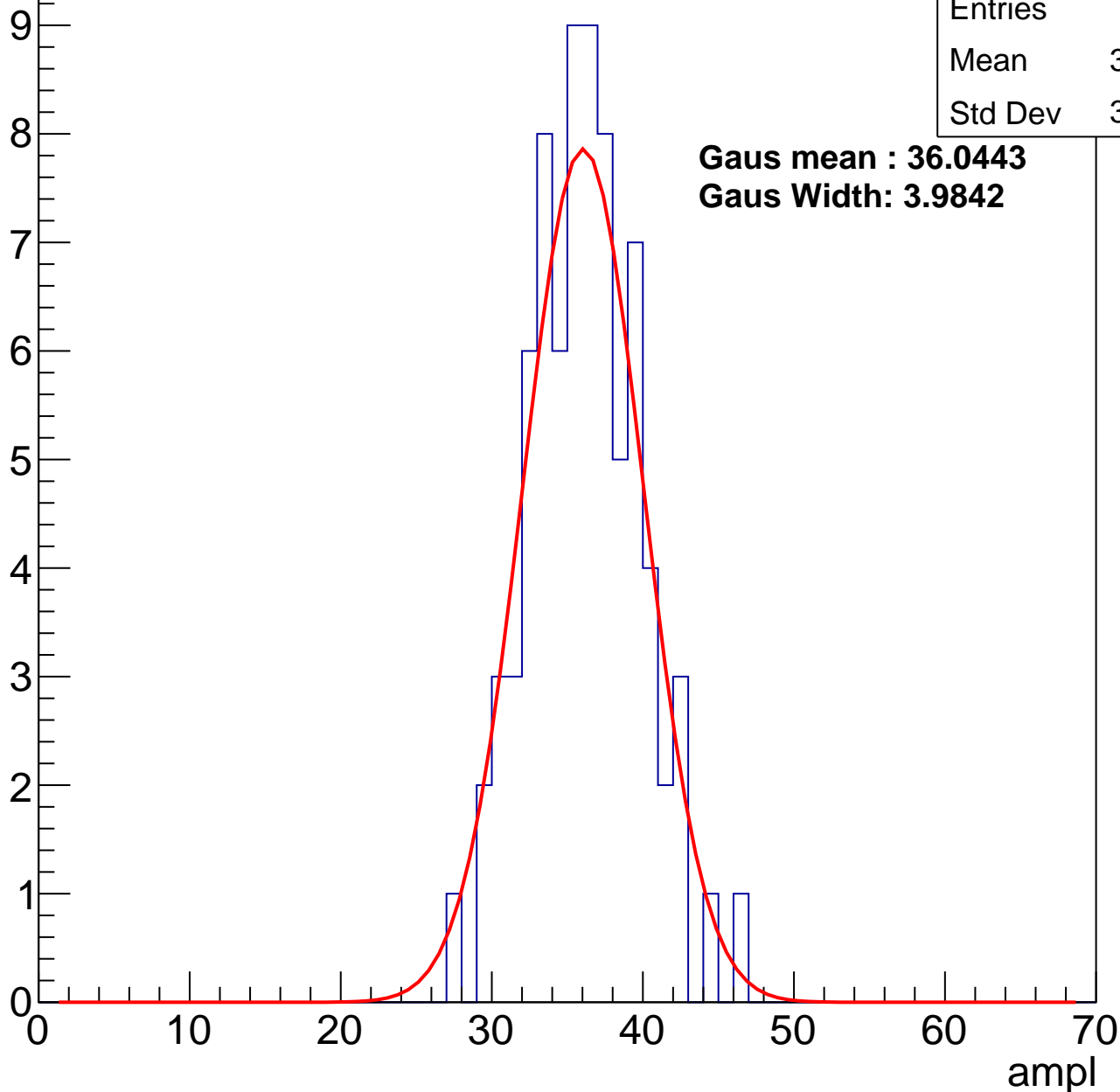
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	78
Mean	35.69
Std Dev	3.638

**Gaus mean : 36.0443**

**Gaus Width: 3.9842**



# B1L103S, U11-ch62, adc2

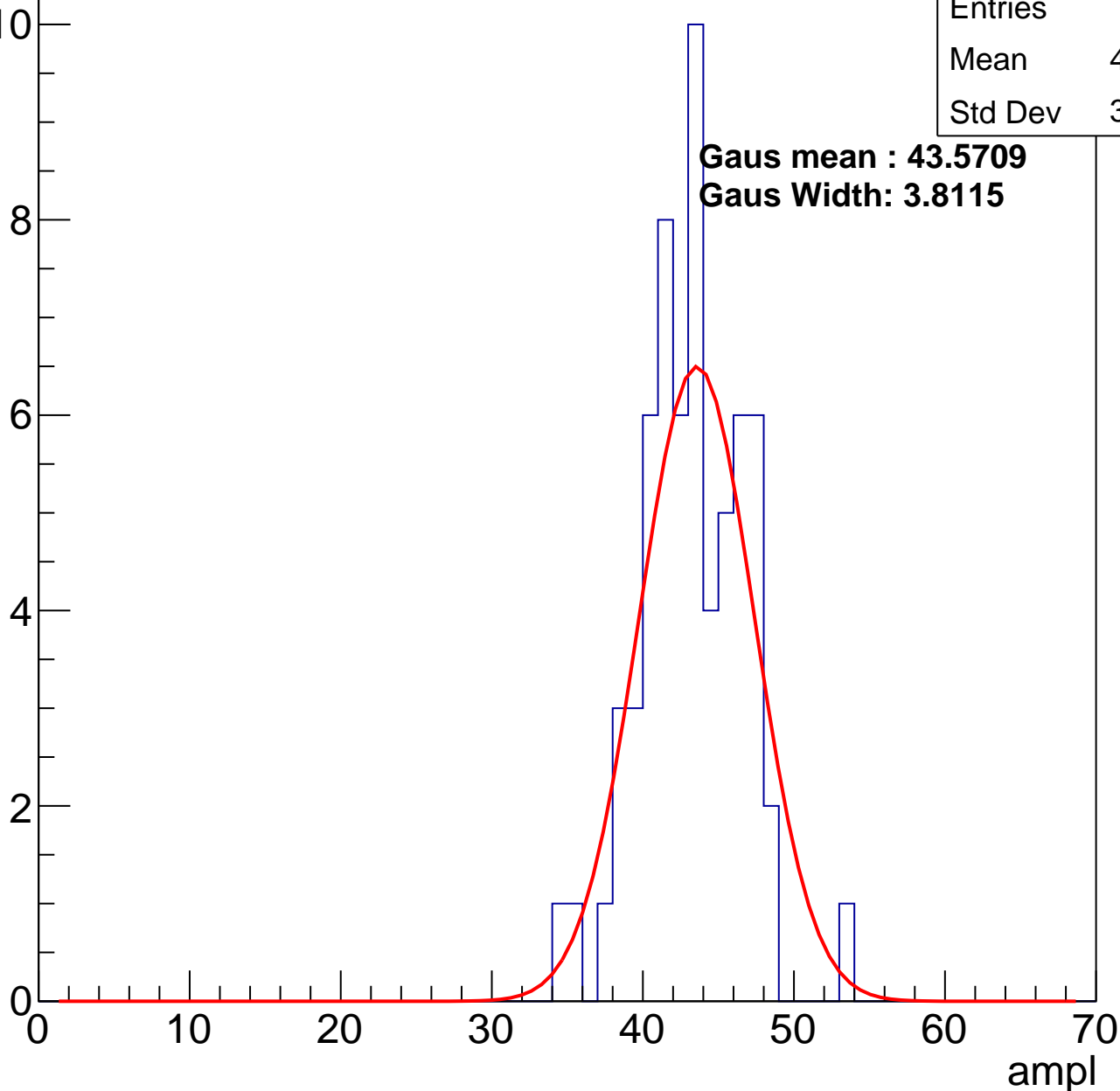
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	42.78
Std Dev	3.373

**Gaus mean : 43.5709**

**Gaus Width: 3.8115**

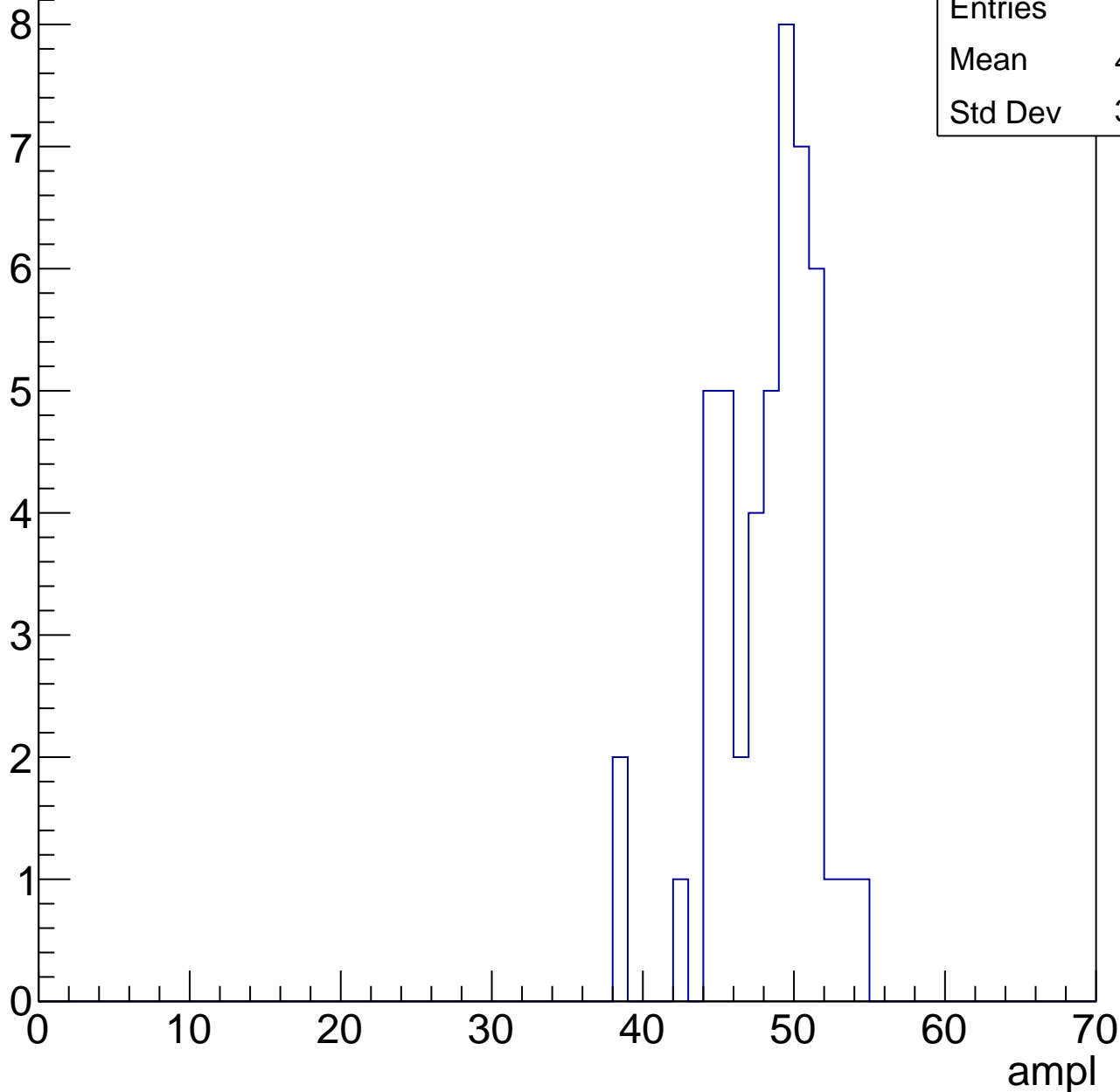


# B1L103S, U11-ch62, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

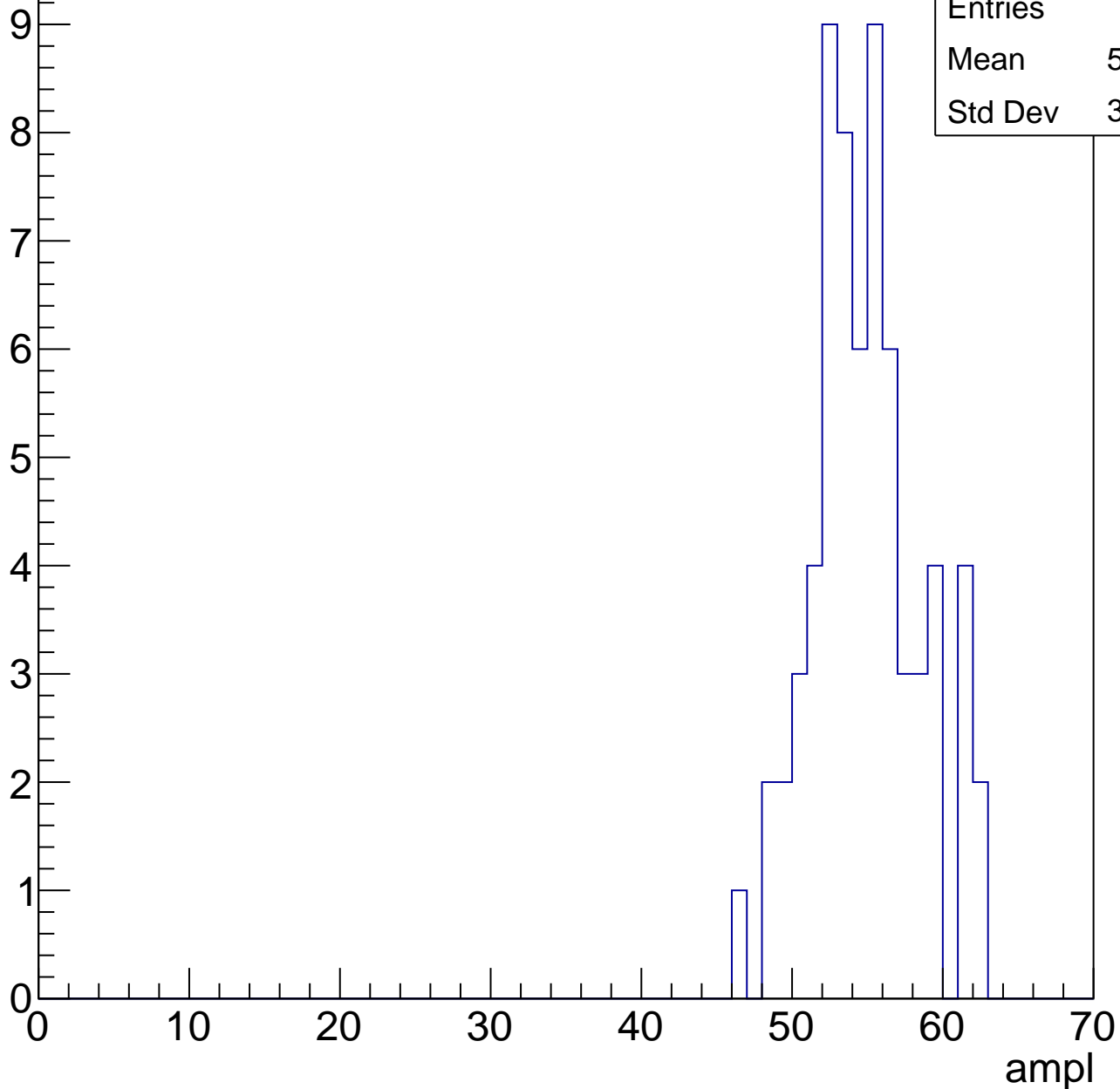
Entries	48
Mean	47.71
Std Dev	3.341



# B1L103S, U11-ch62, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



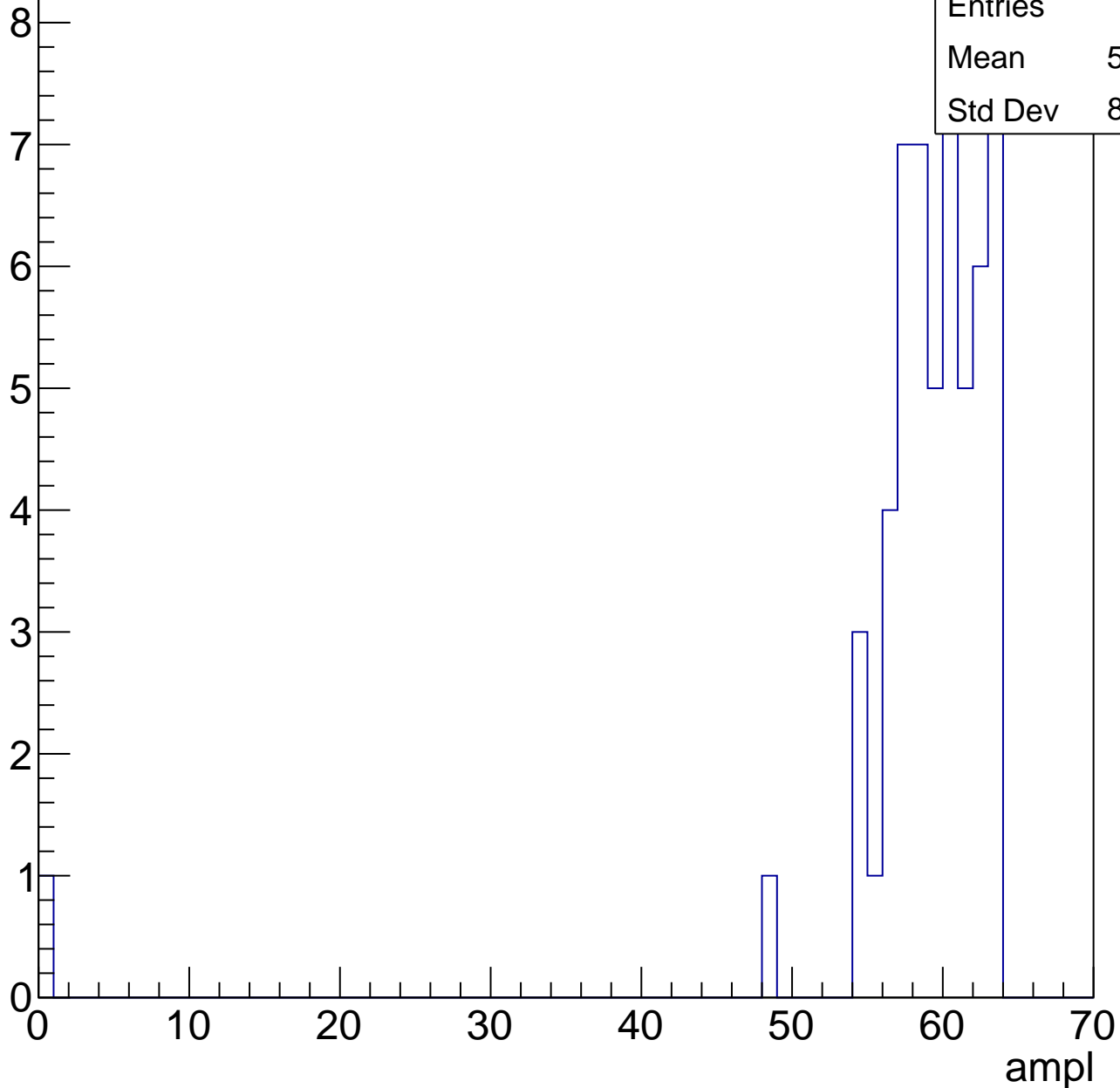
Entries	66
Mean	54.39
Std Dev	3.559

# B1L103S, U11-ch62, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	56
Mean	58.04
Std Dev	8.369



# B1L103S, U11-ch62, adc6

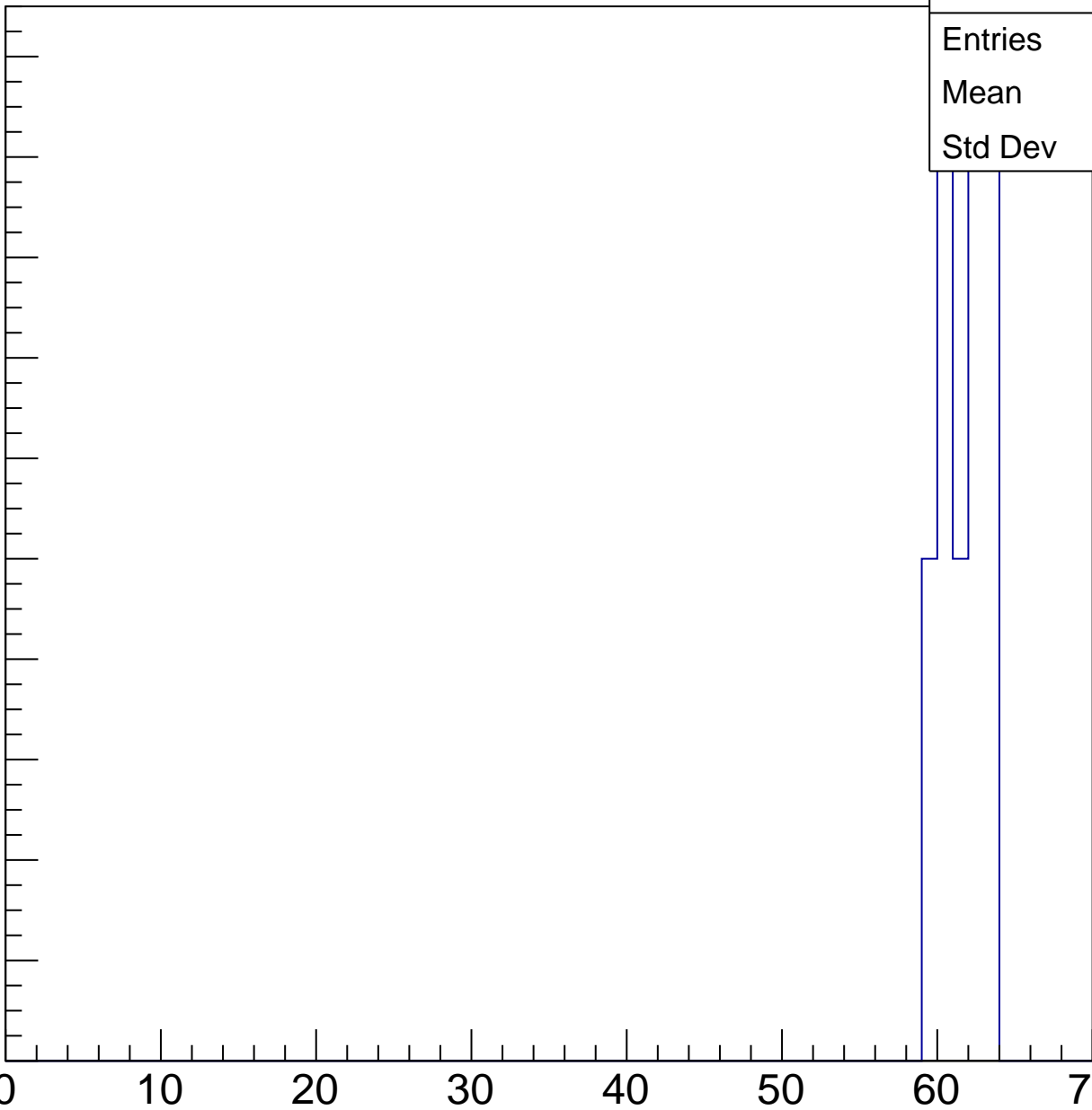
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	8
Mean	61.25
Std Dev	1.392

ampl





# B1L103S, U11-ch62, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U11-ch63, adc0

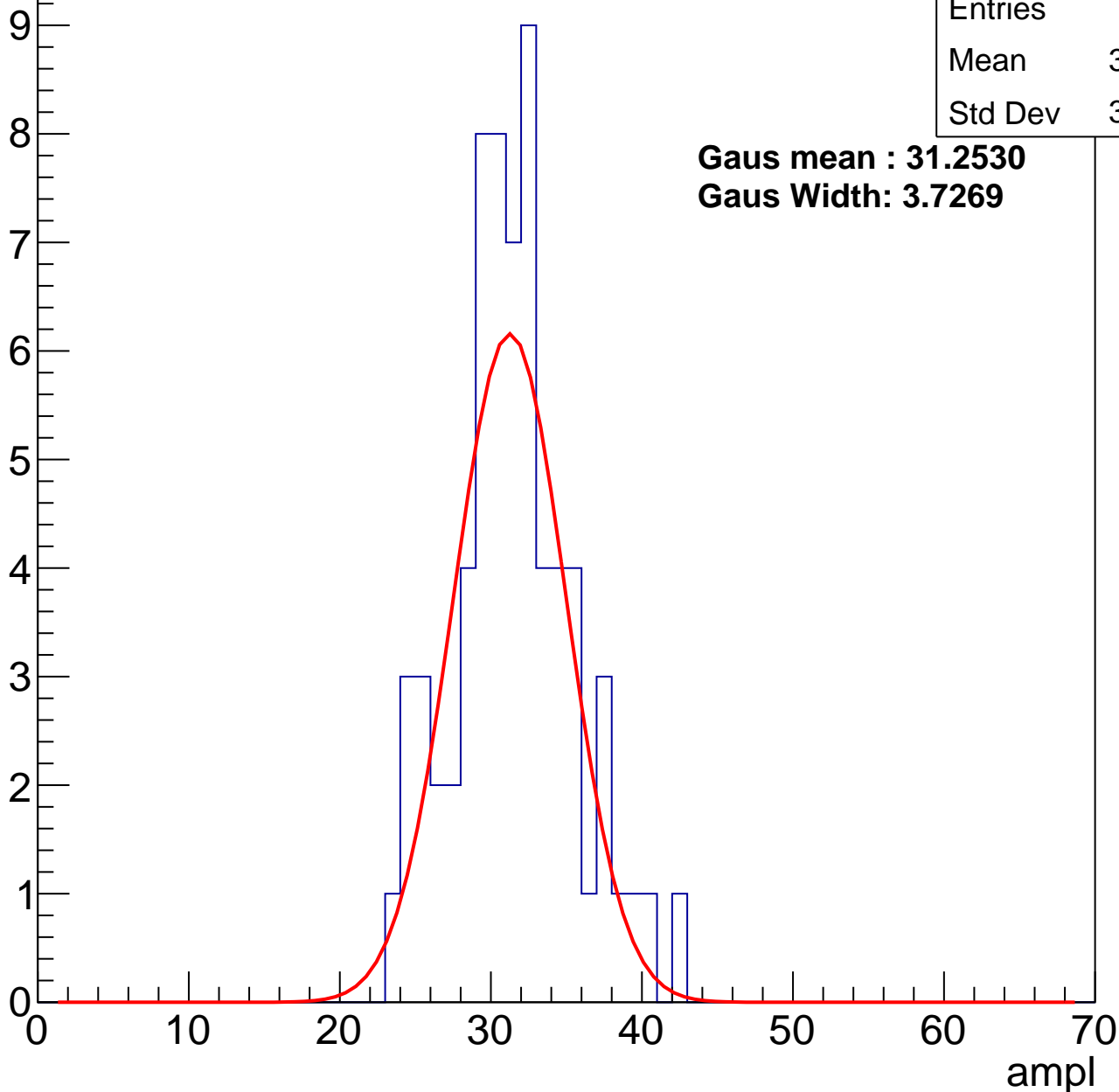
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	31.03
Std Dev	3.959

**Gaus mean : 31.2530**

**Gaus Width: 3.7269**



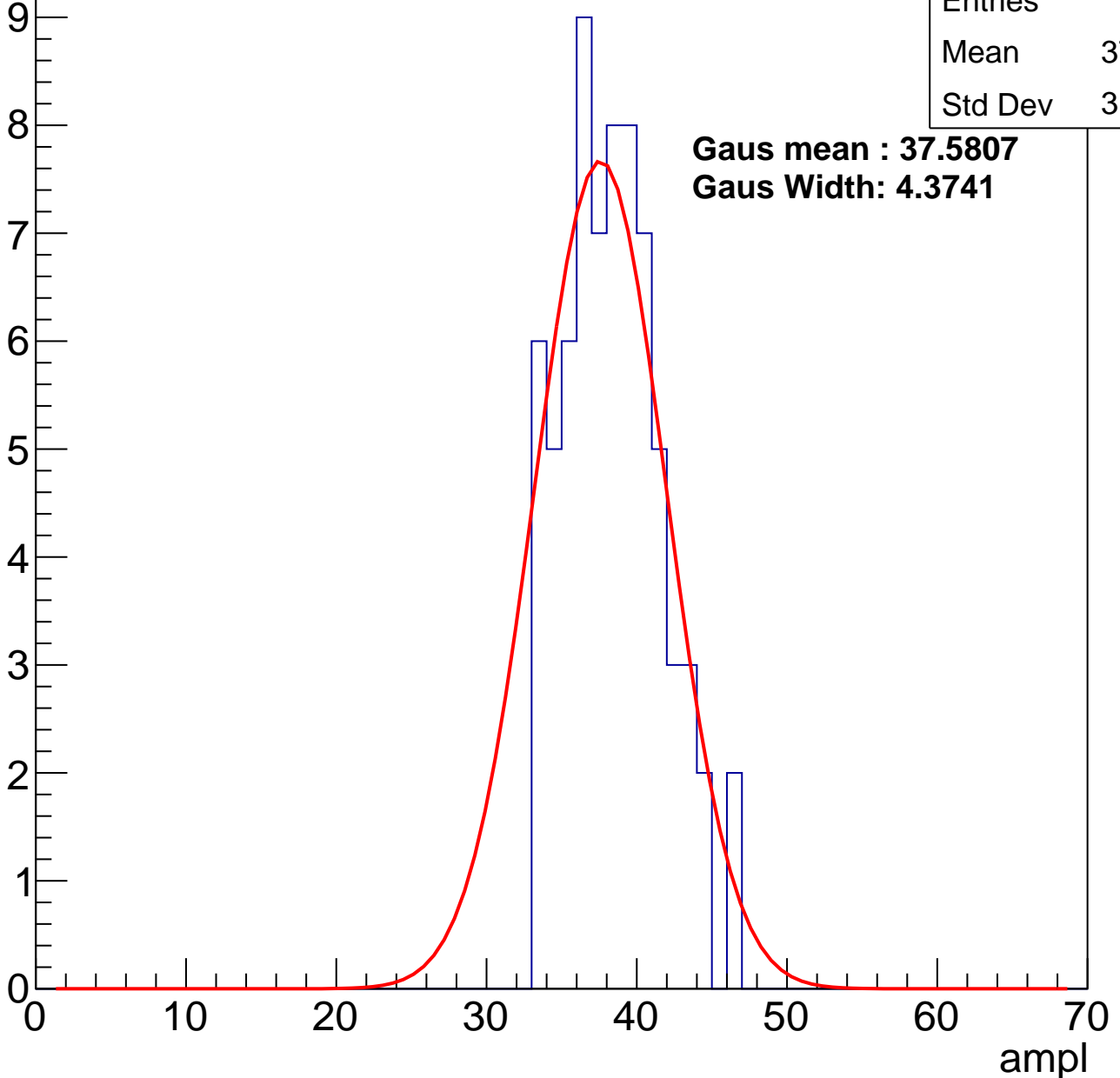
# B1L103S, U11-ch63, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	71
Mean	37.99
Std Dev	3.209

**Gaus mean : 37.5807**  
**Gaus Width: 4.3741**



# B1L103S, U11-ch63, adc2

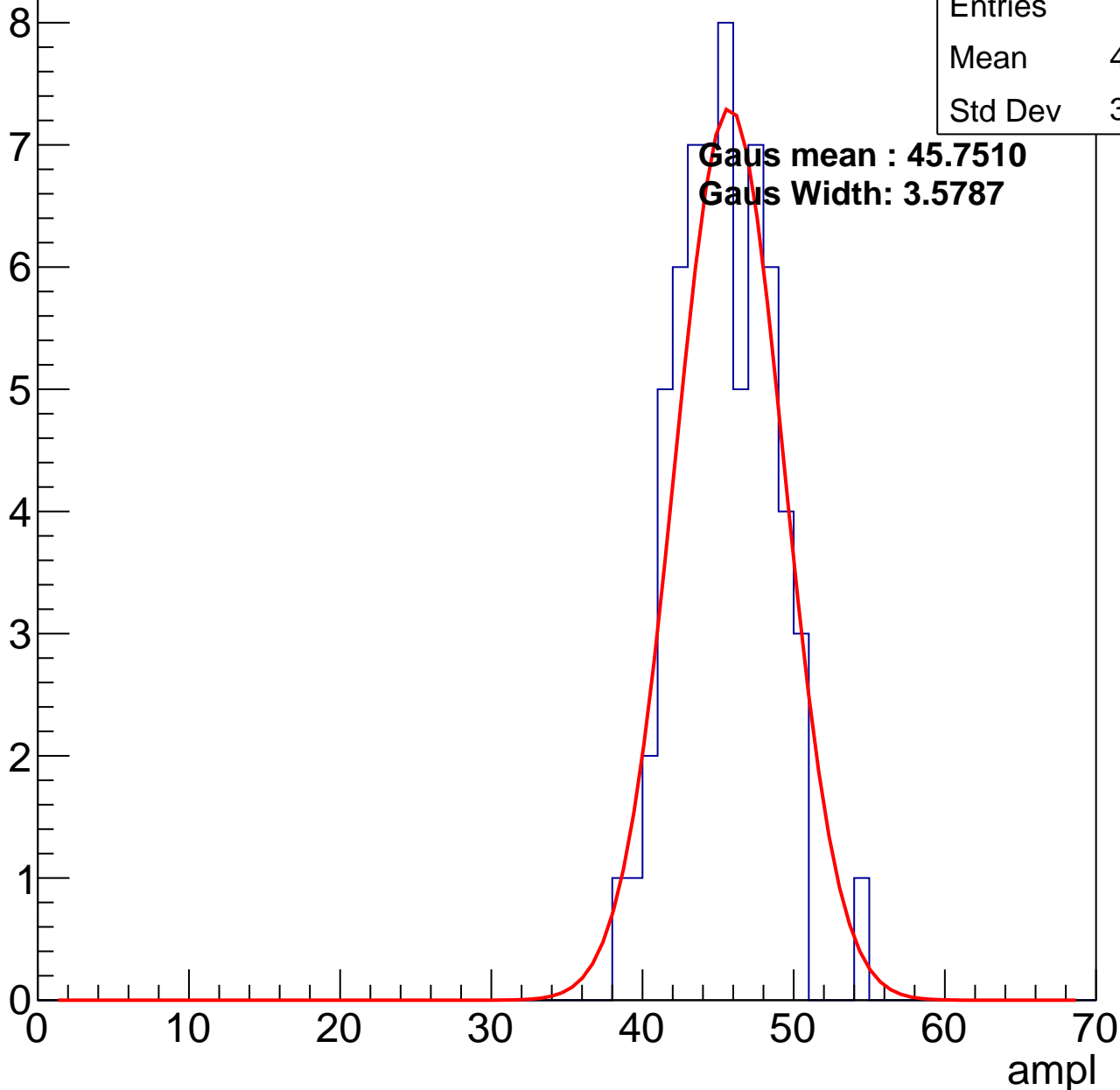
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	44.92
Std Dev	3.113

**Gaus mean : 45.7510**

**Gaus Width: 3.5787**

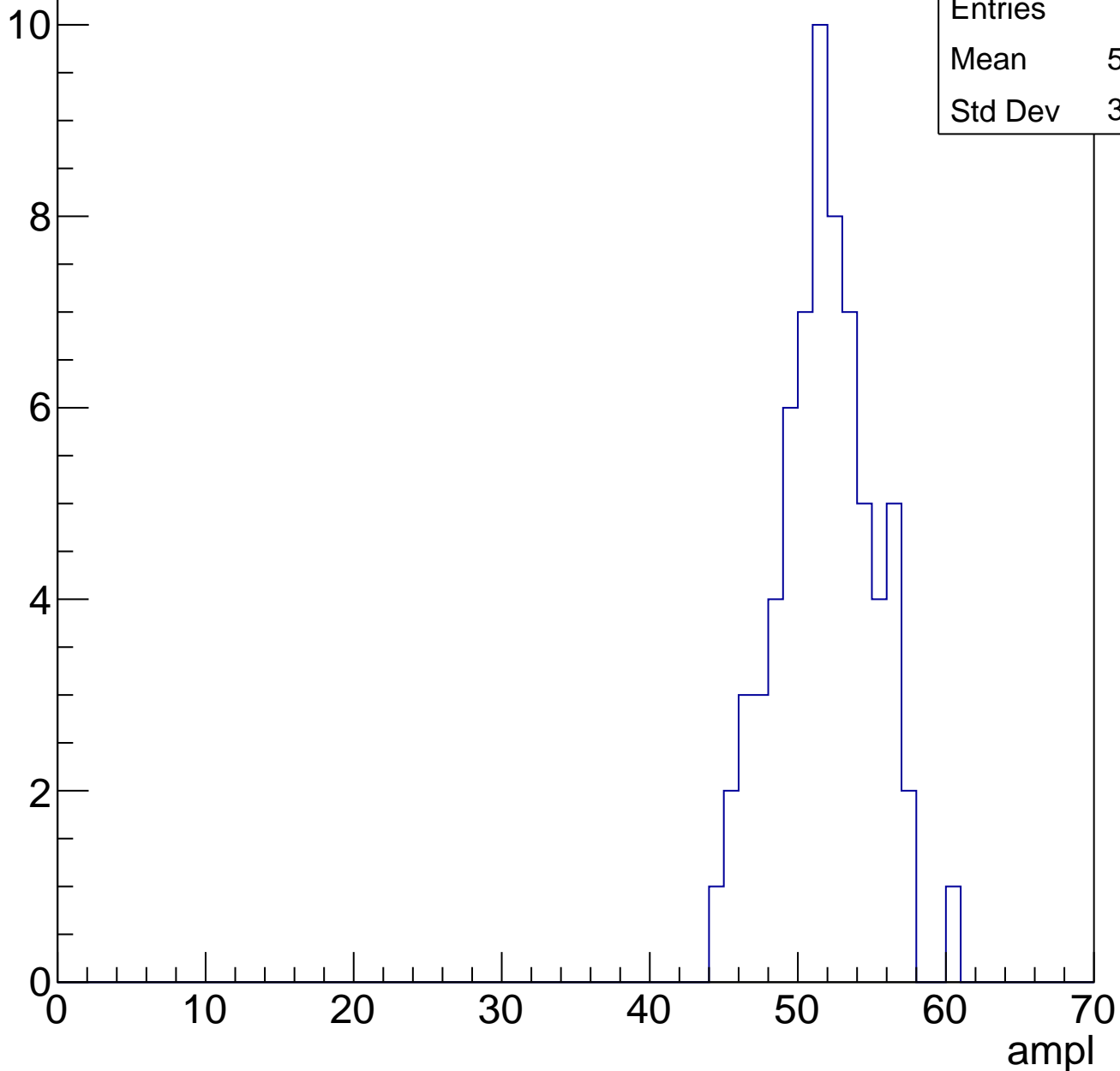


# B1L103S, U11-ch63, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	68
Mean	51.32
Std Dev	3.269

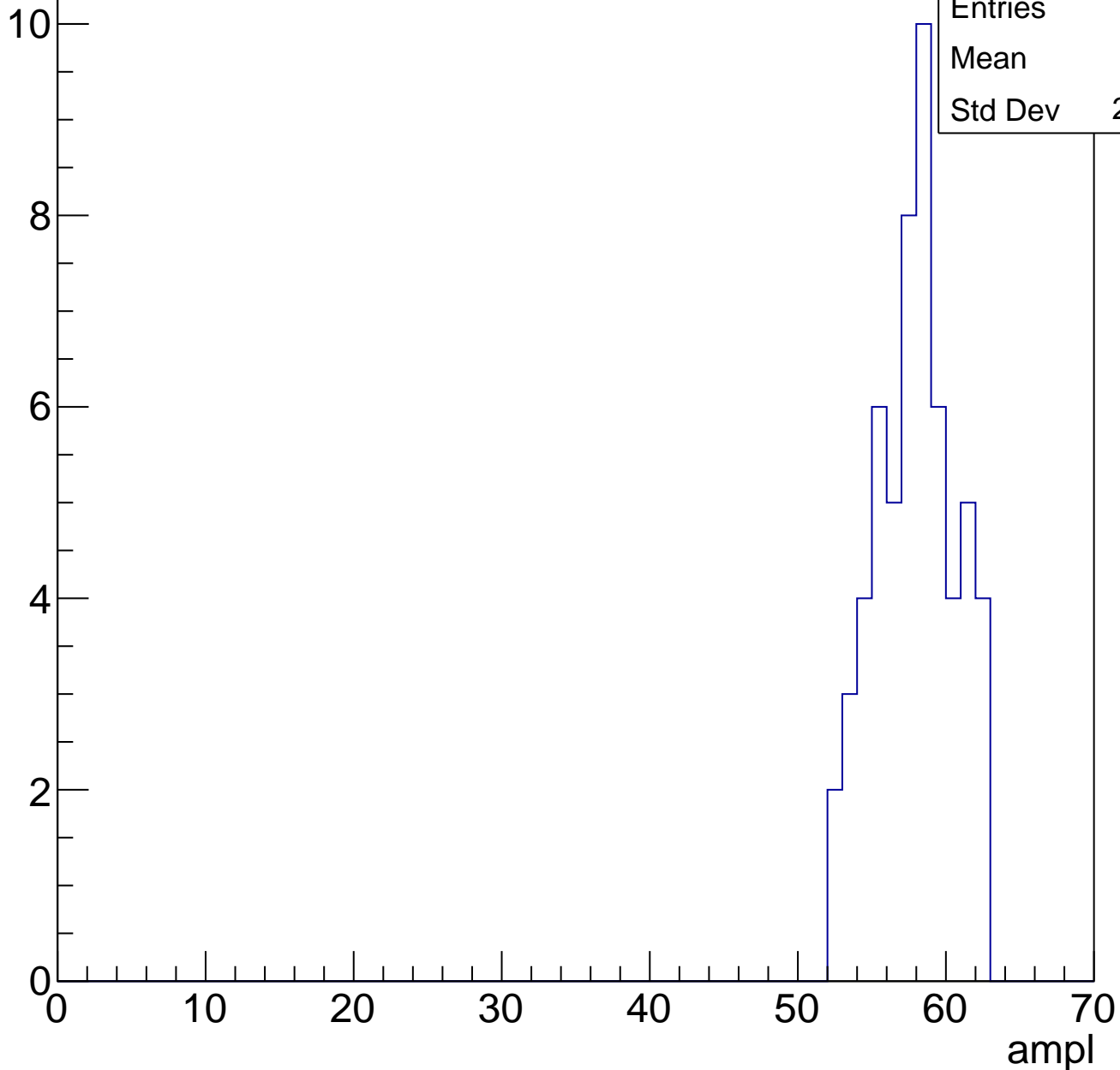


# B1L103S, U11-ch63, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	57
Mean	57.4
Std Dev	2.661

Entry



# B1L103S, U11-ch63, adc5

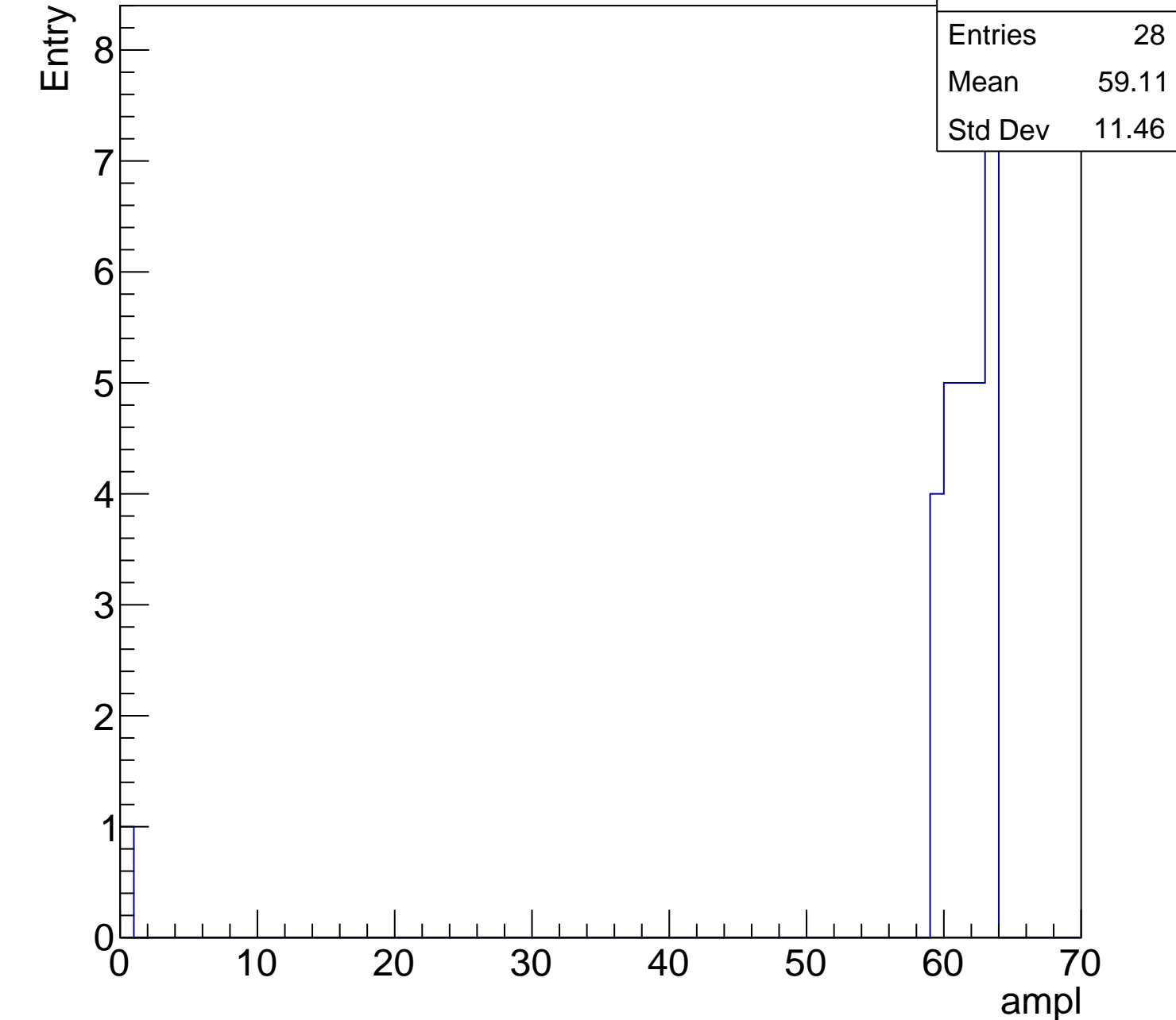
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	28
Mean	59.11
Std Dev	11.46

ampl



# B1L103S, U11-ch63, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	3
Mean	62.67
Std Dev	0.4714

ampl

0 10 20 30 40 50 60 70



# B1L103S, U11-ch63, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L103S, U11-ch64, adc0

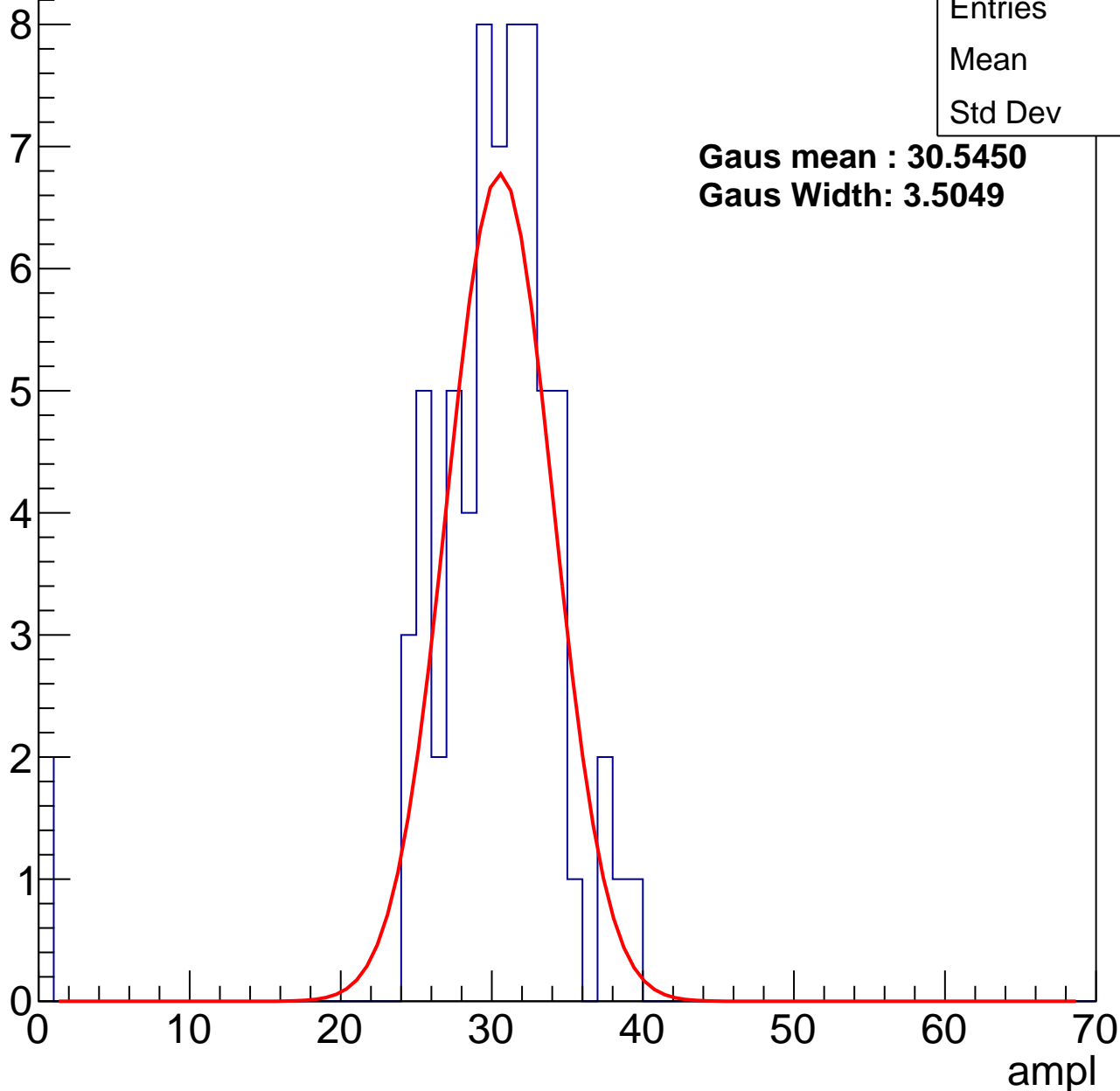
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	29.3
Std Dev	6.15

**Gaus mean : 30.5450**

**Gaus Width: 3.5049**



# B1L103S, U11-ch64, adc1

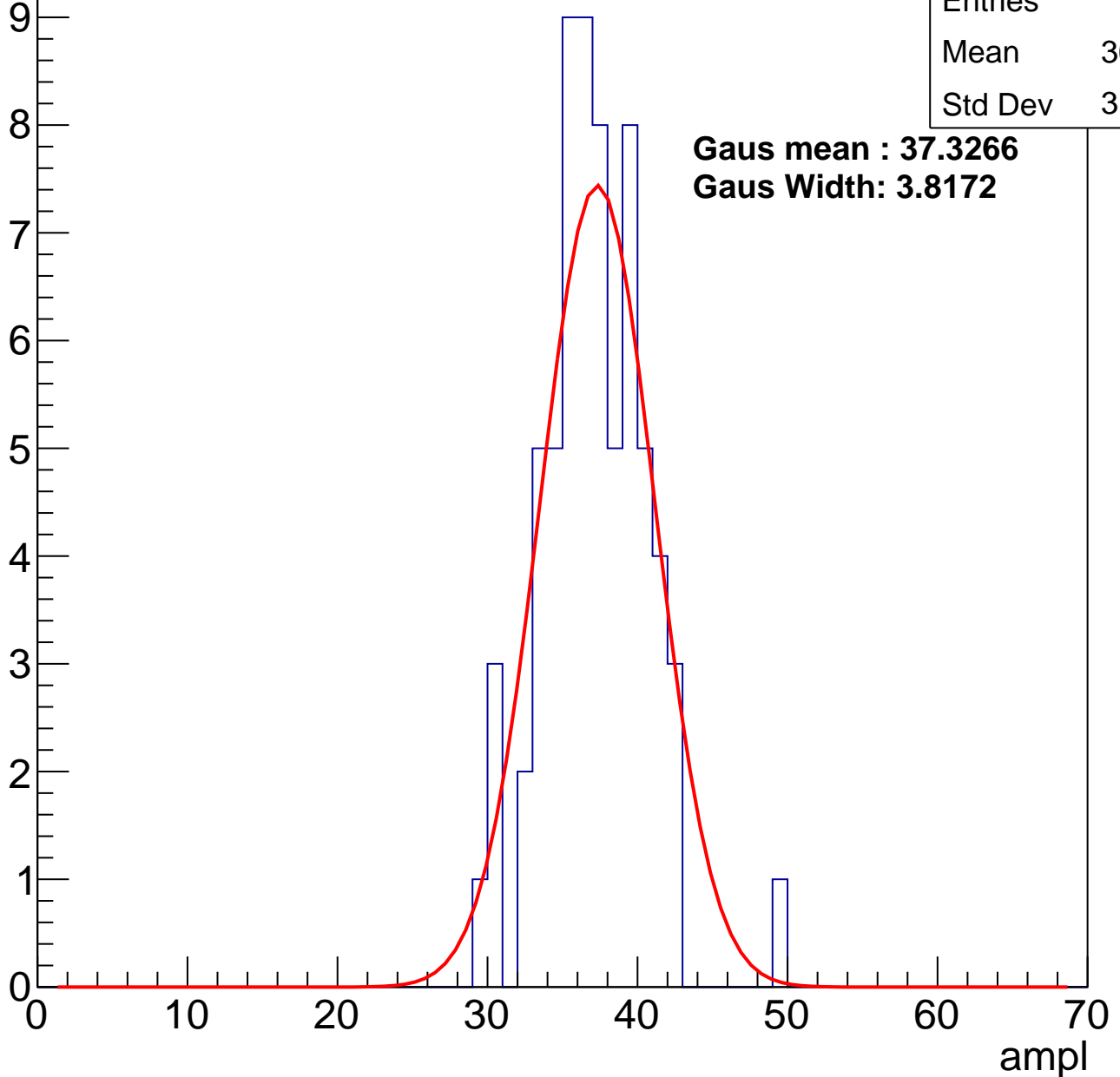
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	68
Mean	36.68
Std Dev	3.406

**Gaus mean : 37.3266**

**Gaus Width: 3.8172**



# B1L103S, U11-ch64, adc2

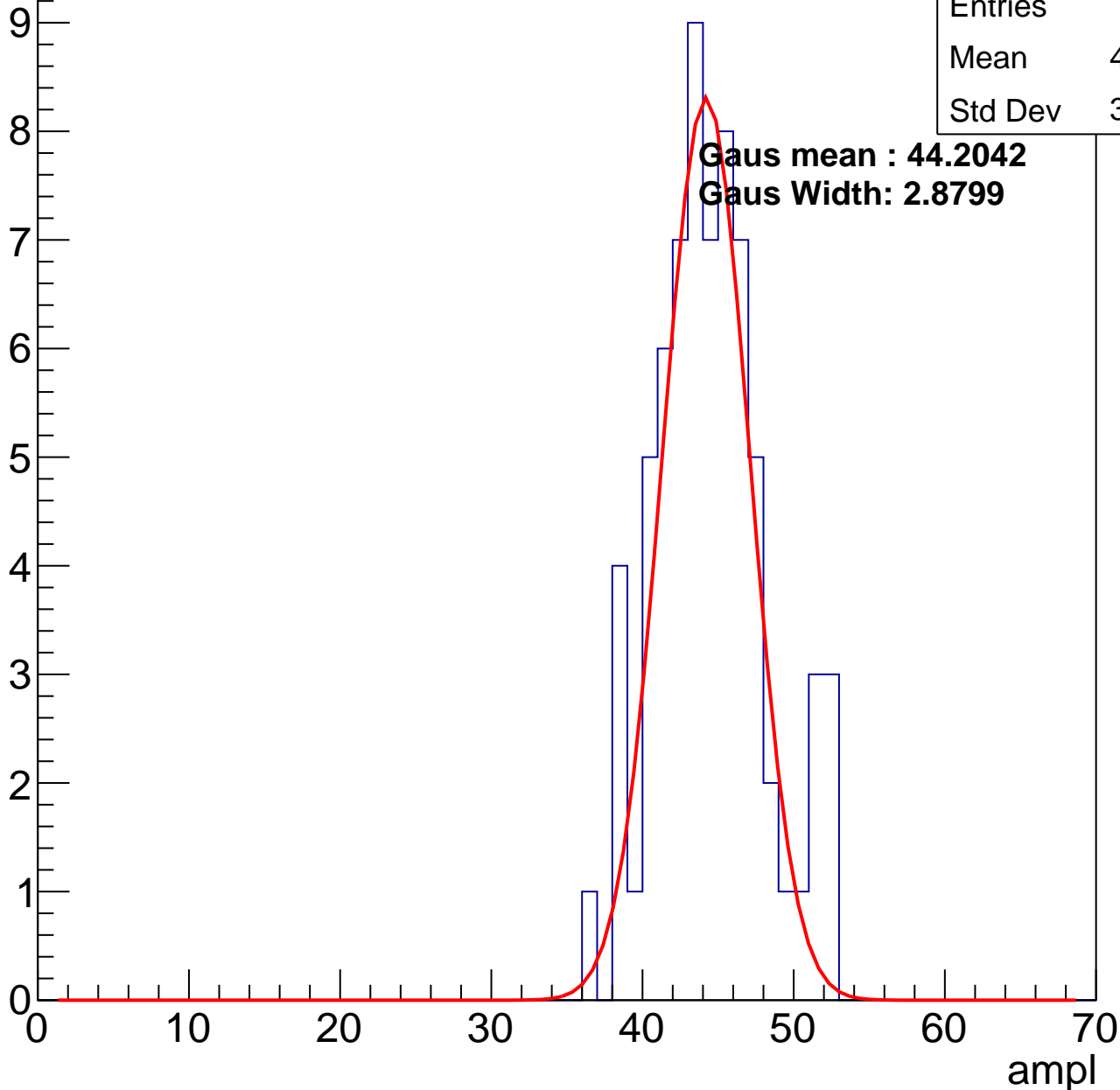
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	70
Mean	44.04
Std Dev	3.619

**Gaus mean : 44.2042**

**Gaus Width: 2.8799**

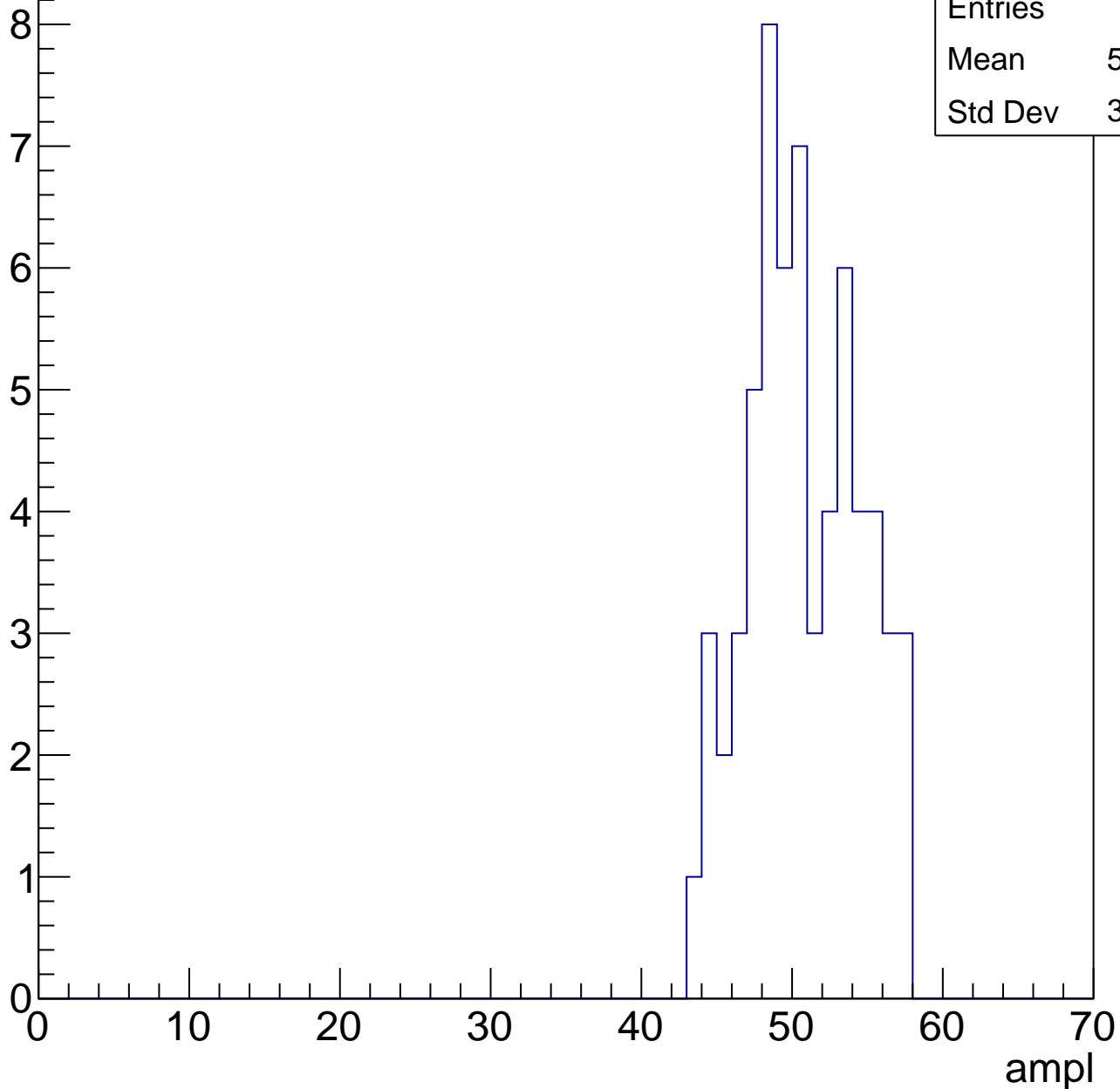


# B1L103S, U11-ch64, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	50.32
Std Dev	3.645

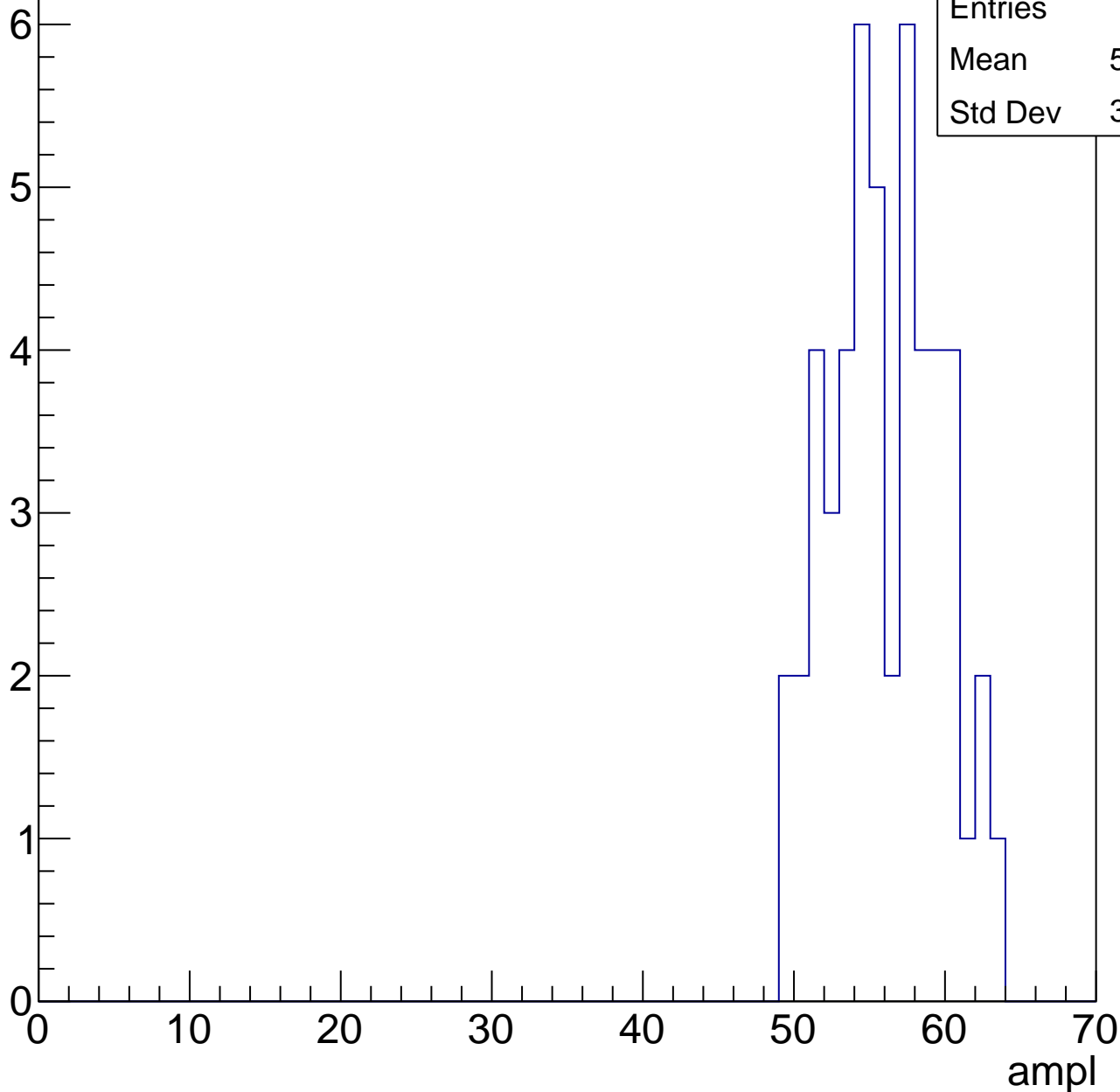


# B1L103S, U11-ch64, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	50
Mean	55.58
Std Dev	3.584

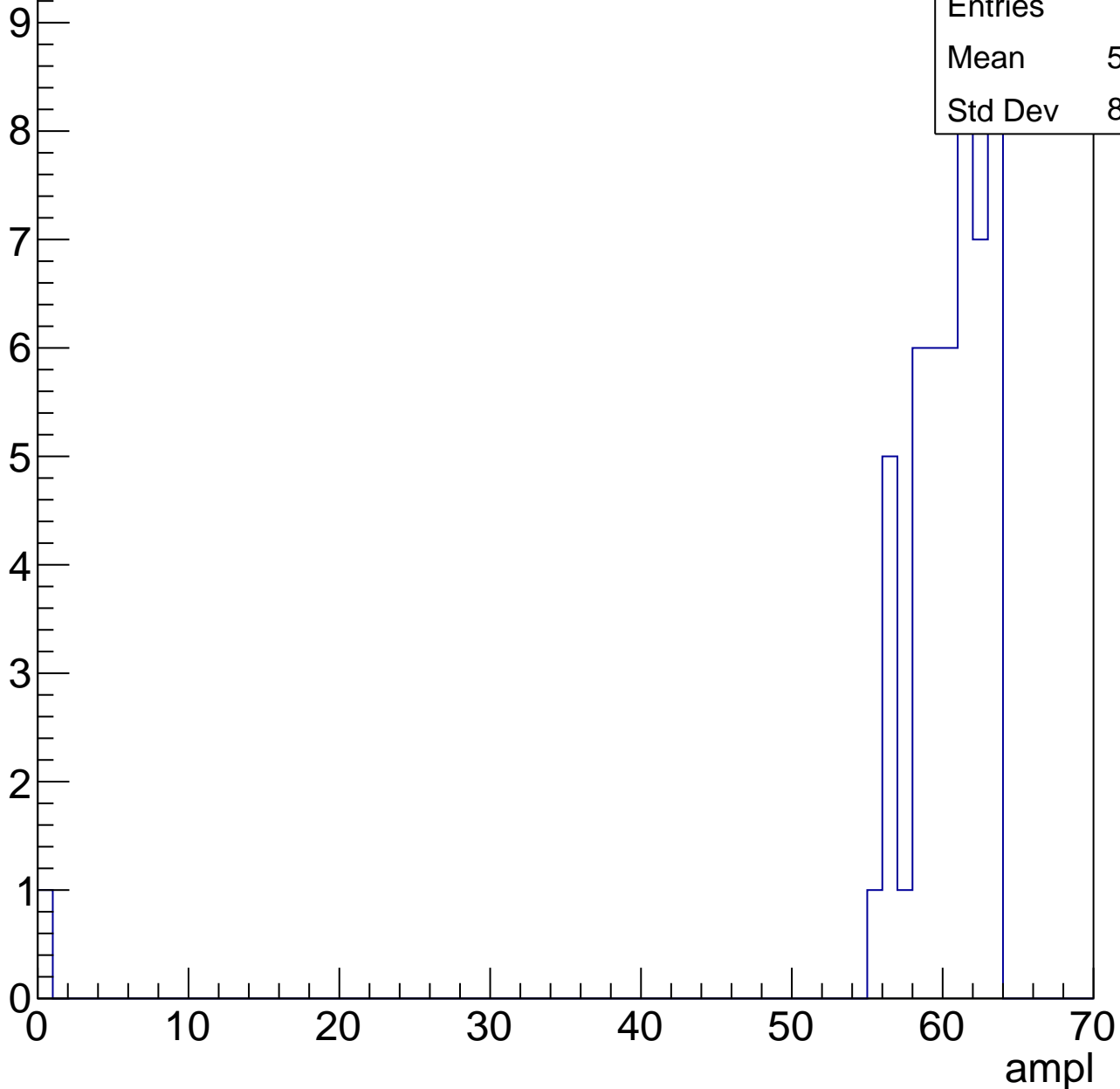


# B1L103S, U11-ch64, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	50
Mean	58.82
Std Dev	8.699



# B1L103S, U11-ch64, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U11-ch64, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	2
Mean	11
Std Dev	11

# B1L103S, U11-ch65, adc0

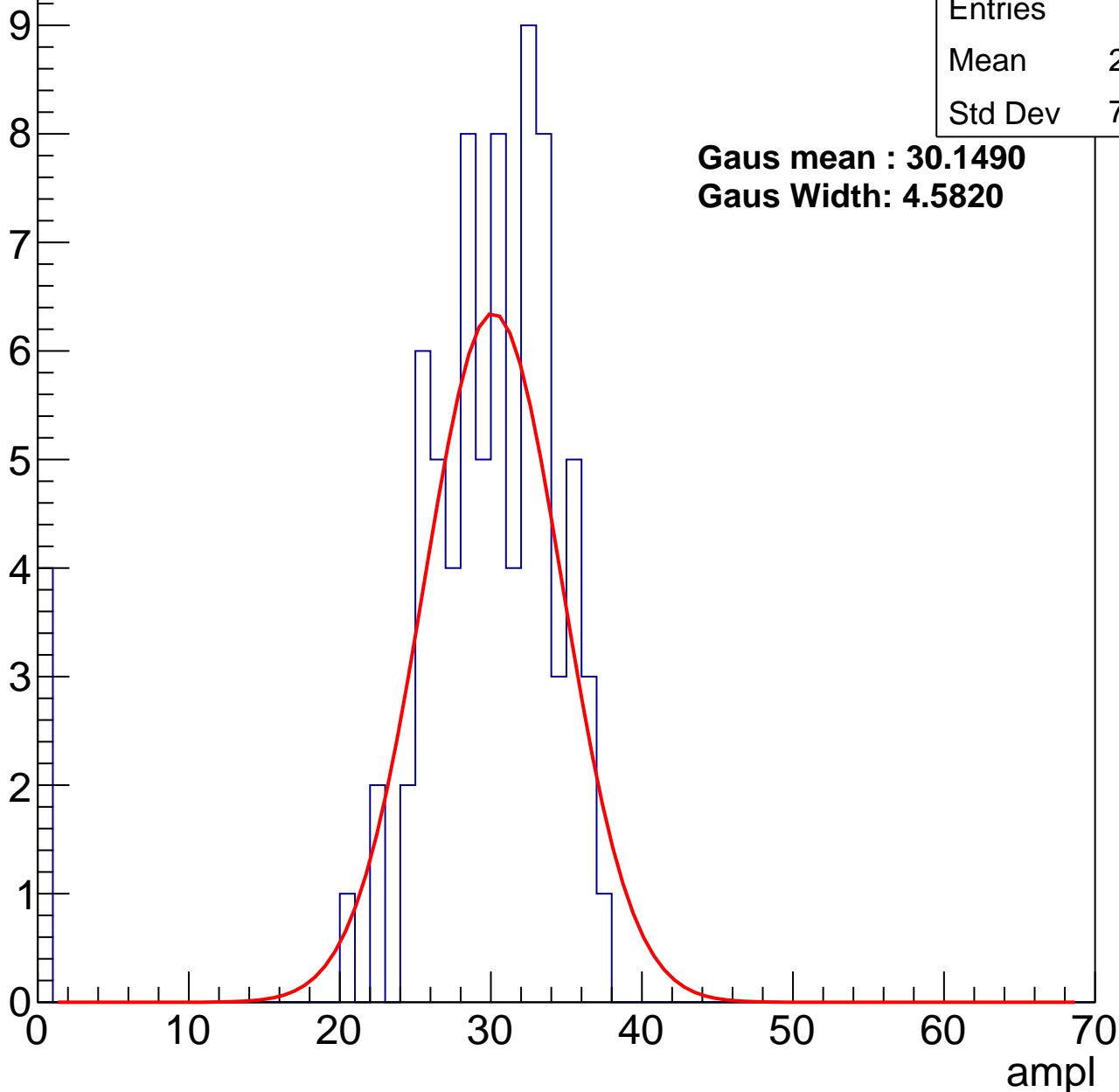
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	78
Mean	28.29
Std Dev	7.526

**Gaus mean : 30.1490**

**Gaus Width: 4.5820**



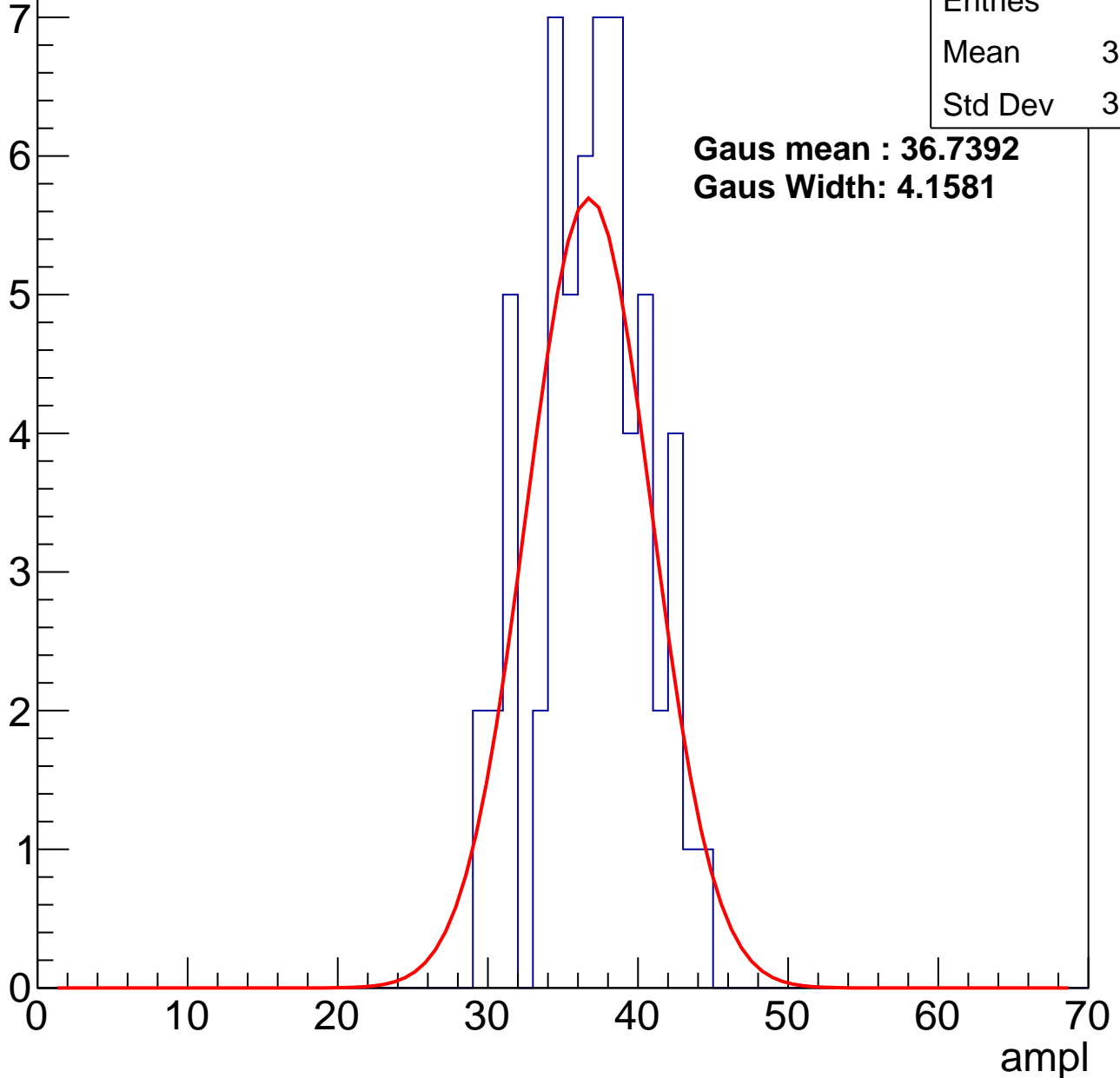
# B1L103S, U11-ch65, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	60
Mean	36.43
Std Dev	3.635

**Gaus mean : 36.7392**  
**Gaus Width: 4.1581**



# B1L103S, U11-ch65, adc2

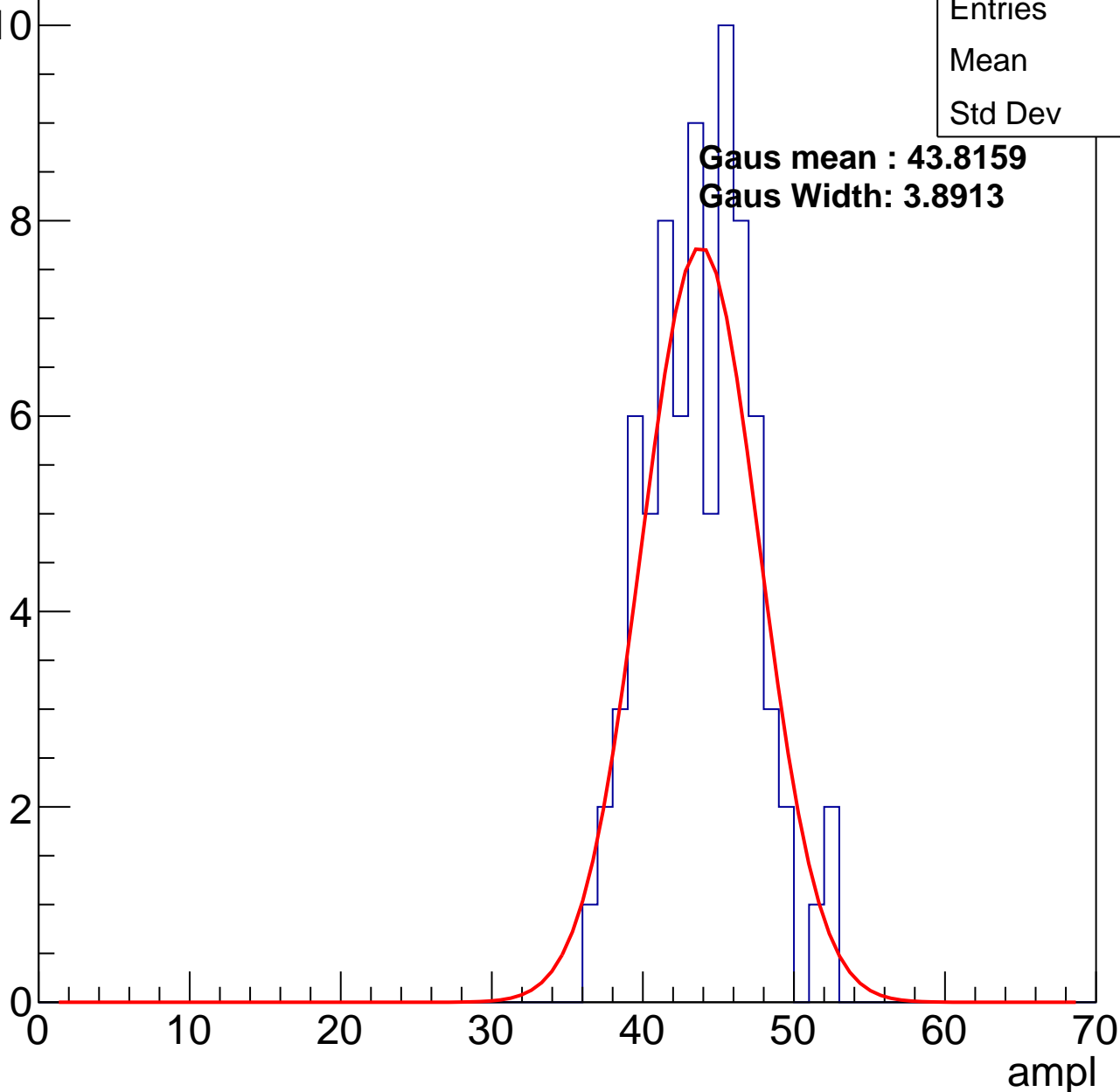
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	77
Mean	43.4
Std Dev	3.51

**Gaus mean : 43.8159**

**Gaus Width: 3.8913**

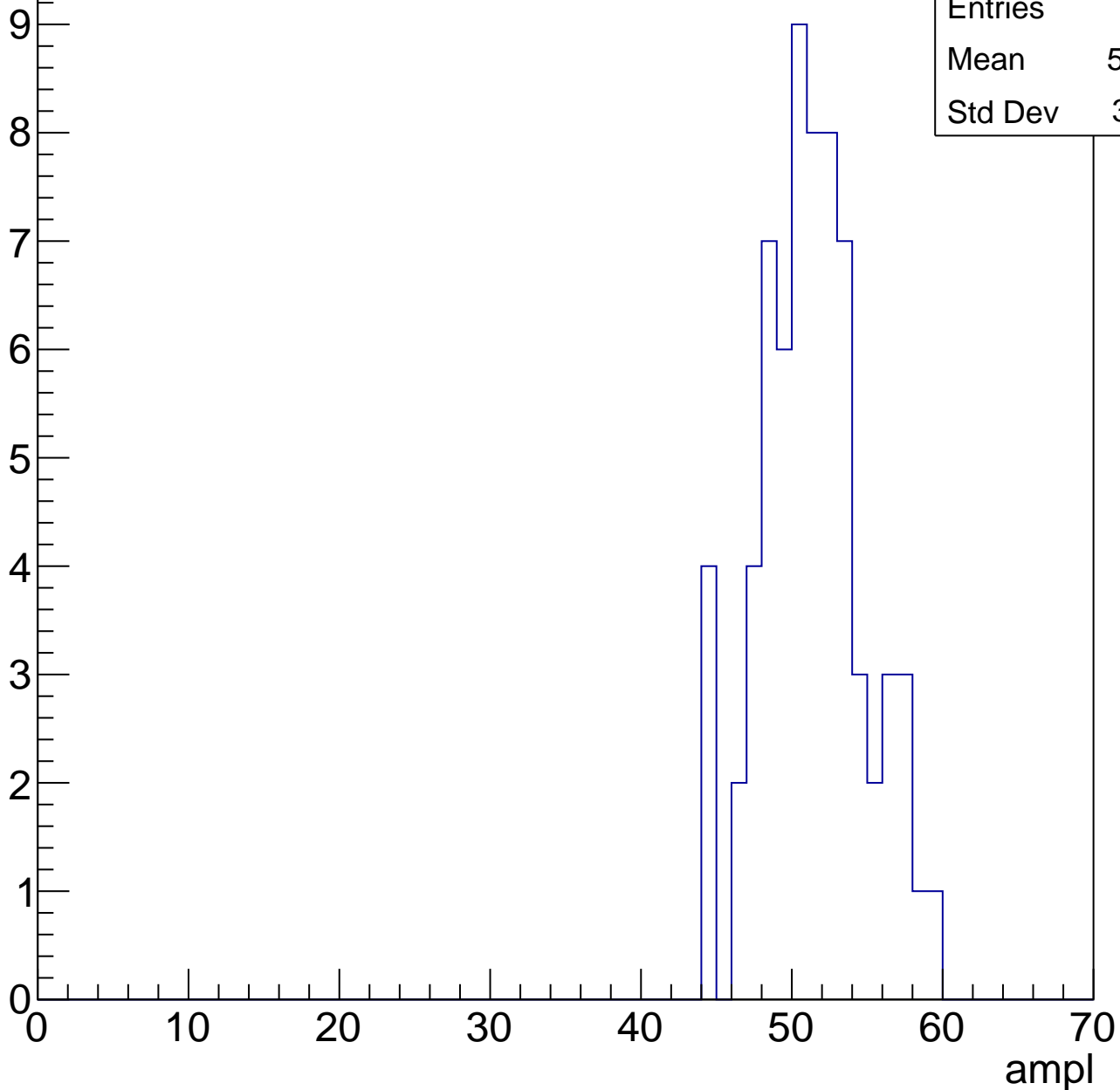


# B1L103S, U11-ch65, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	68
Mean	50.87
Std Dev	3.421

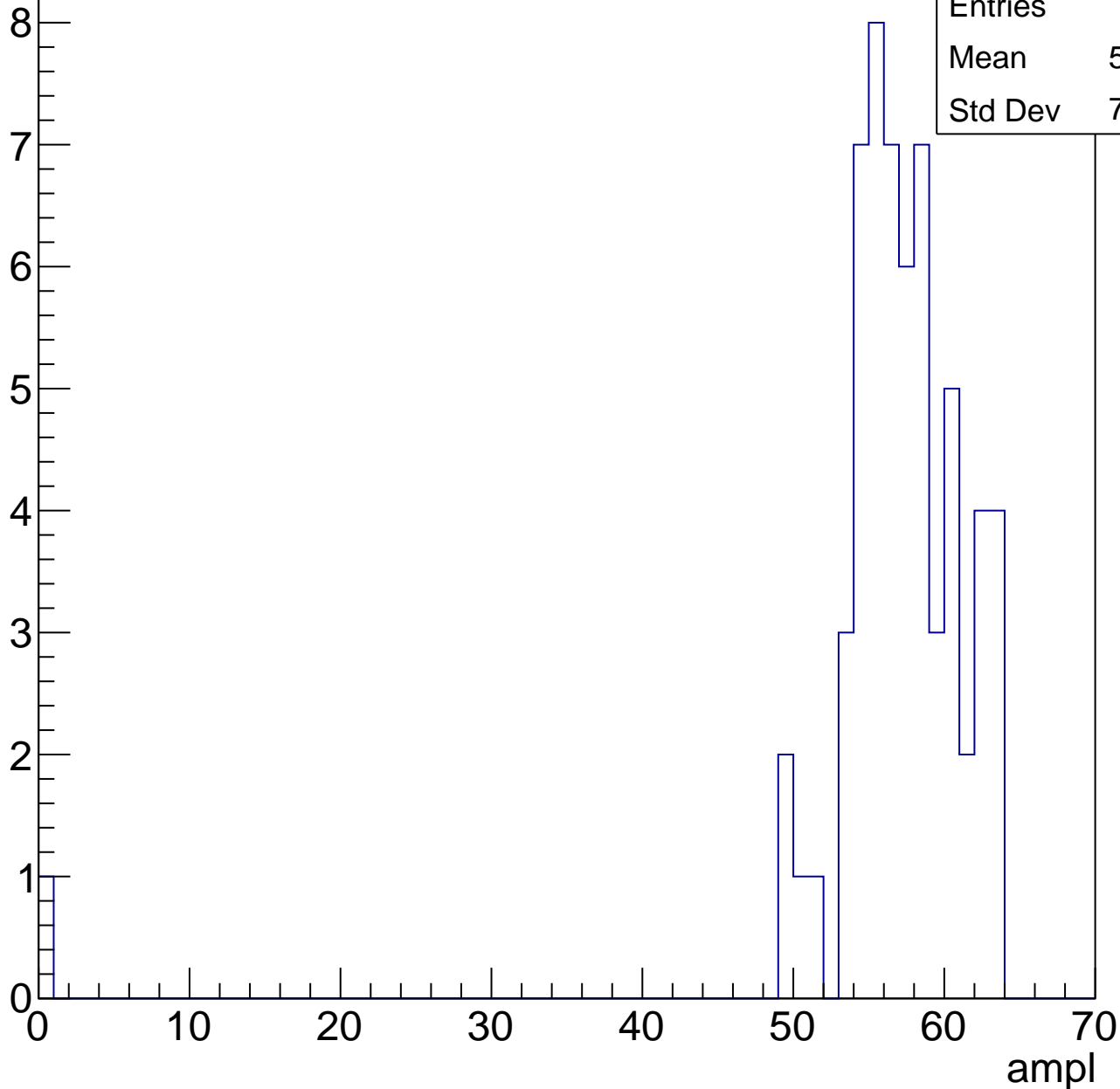


# B1L103S, U11-ch65, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	61
Mean	55.98
Std Dev	7.985

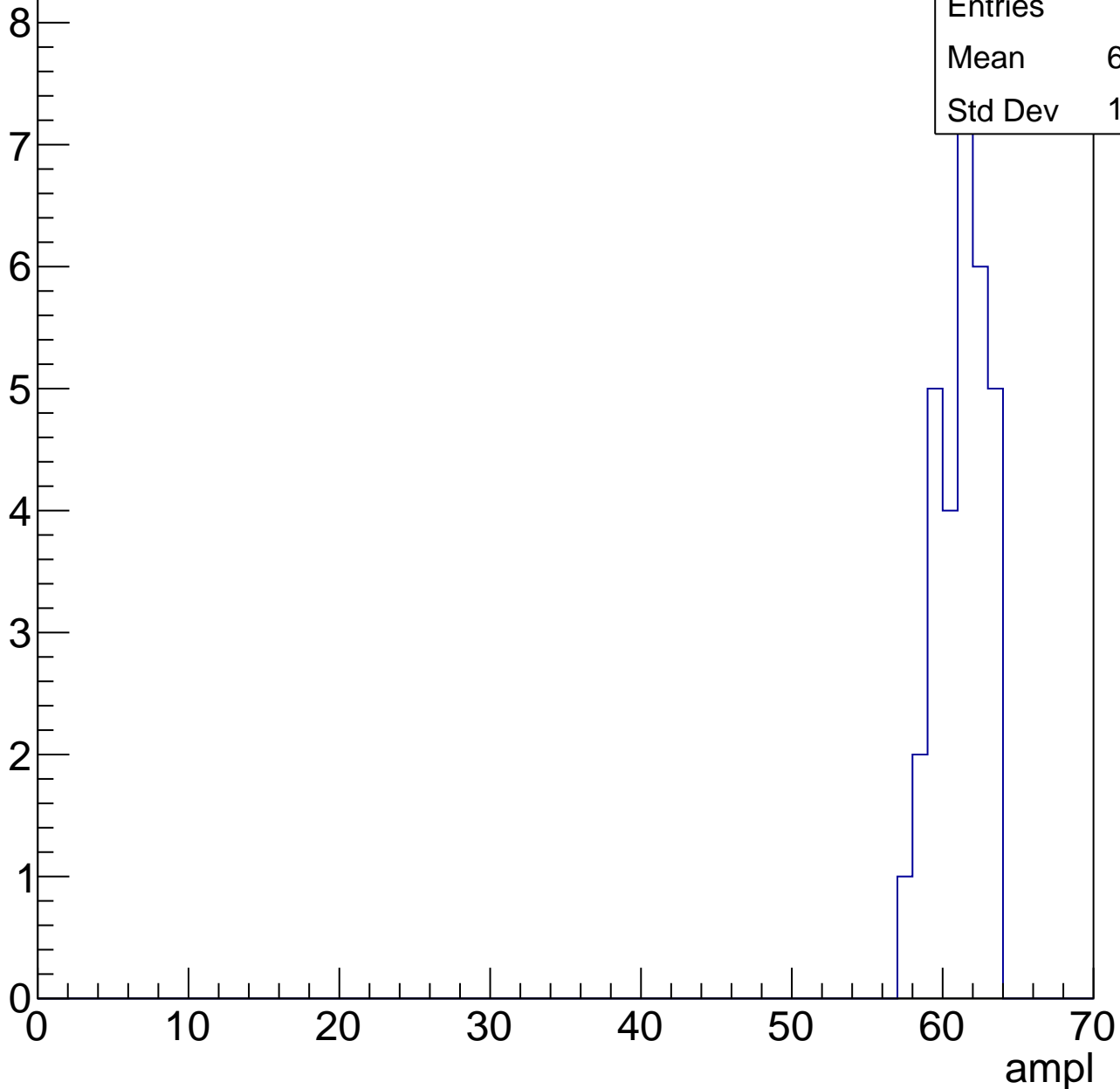


# B1L103S, U11-ch65, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

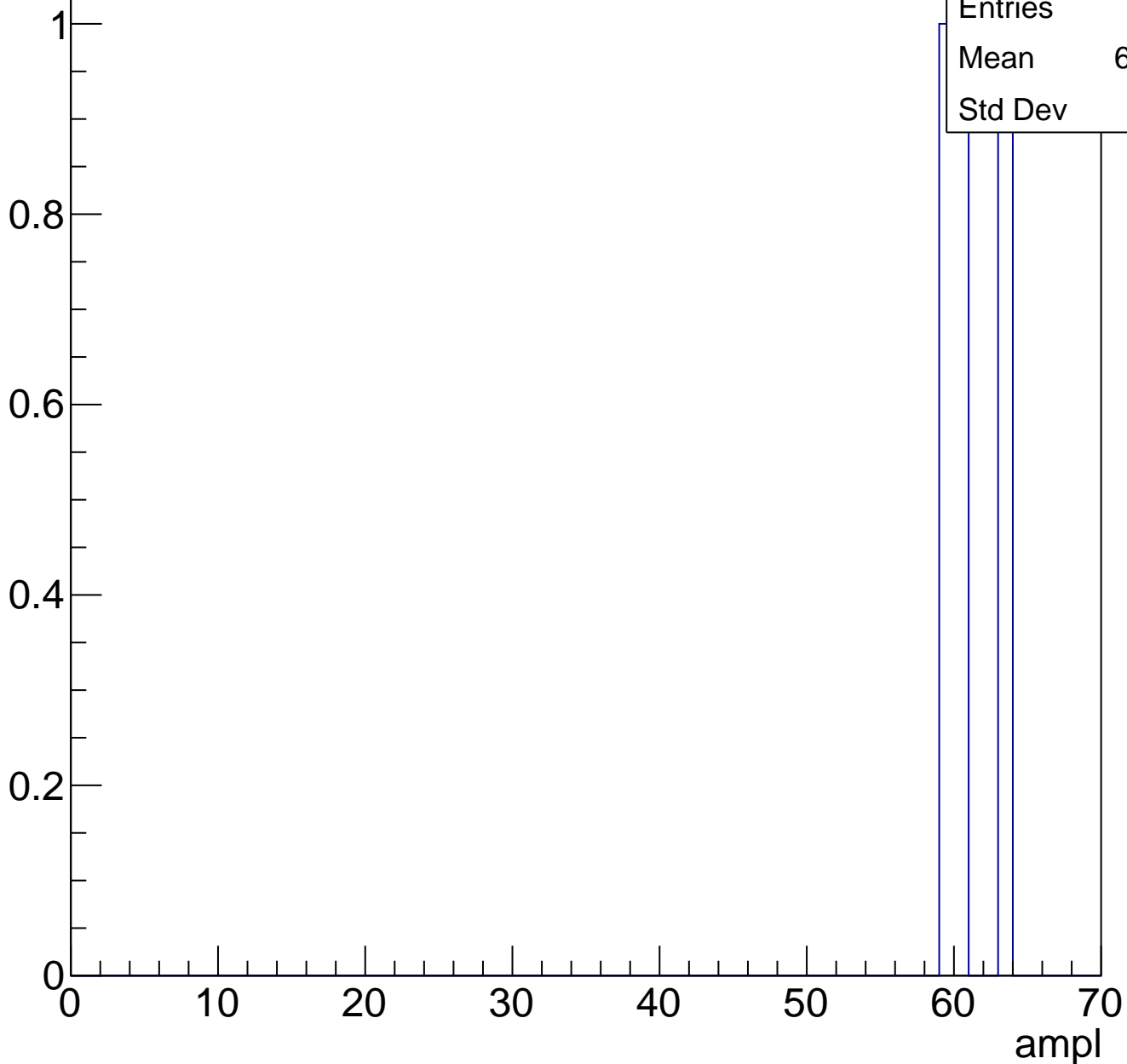
Entries	31
Mean	60.74
Std Dev	1.626



# B1L103S, U11-ch65, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U11-ch65, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L103S, U11-ch66, adc0

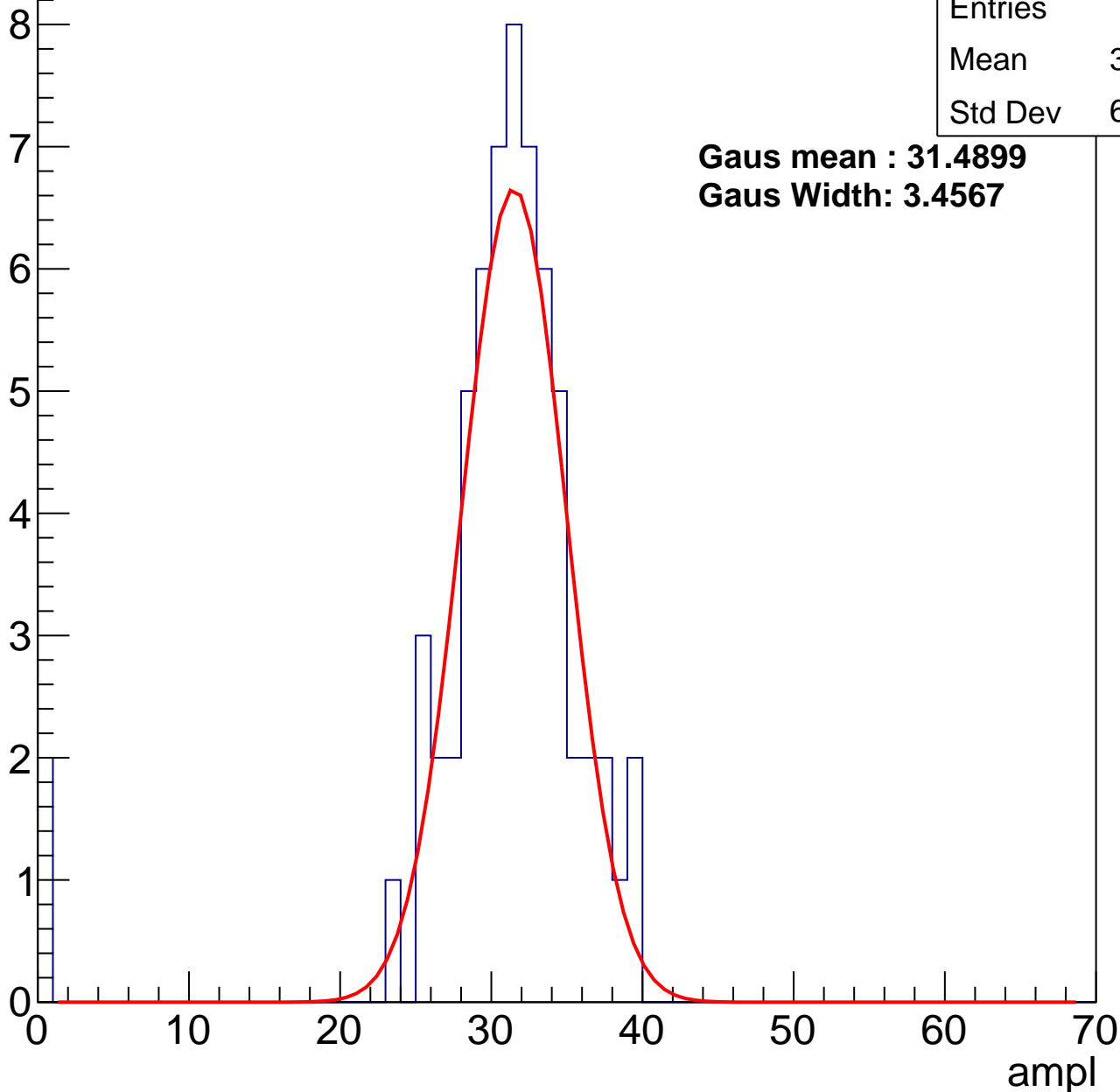
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	30.16
Std Dev	6.442

**Gaus mean : 31.4899**

**Gaus Width: 3.4567**



# B1L103S, U11-ch66, adc1

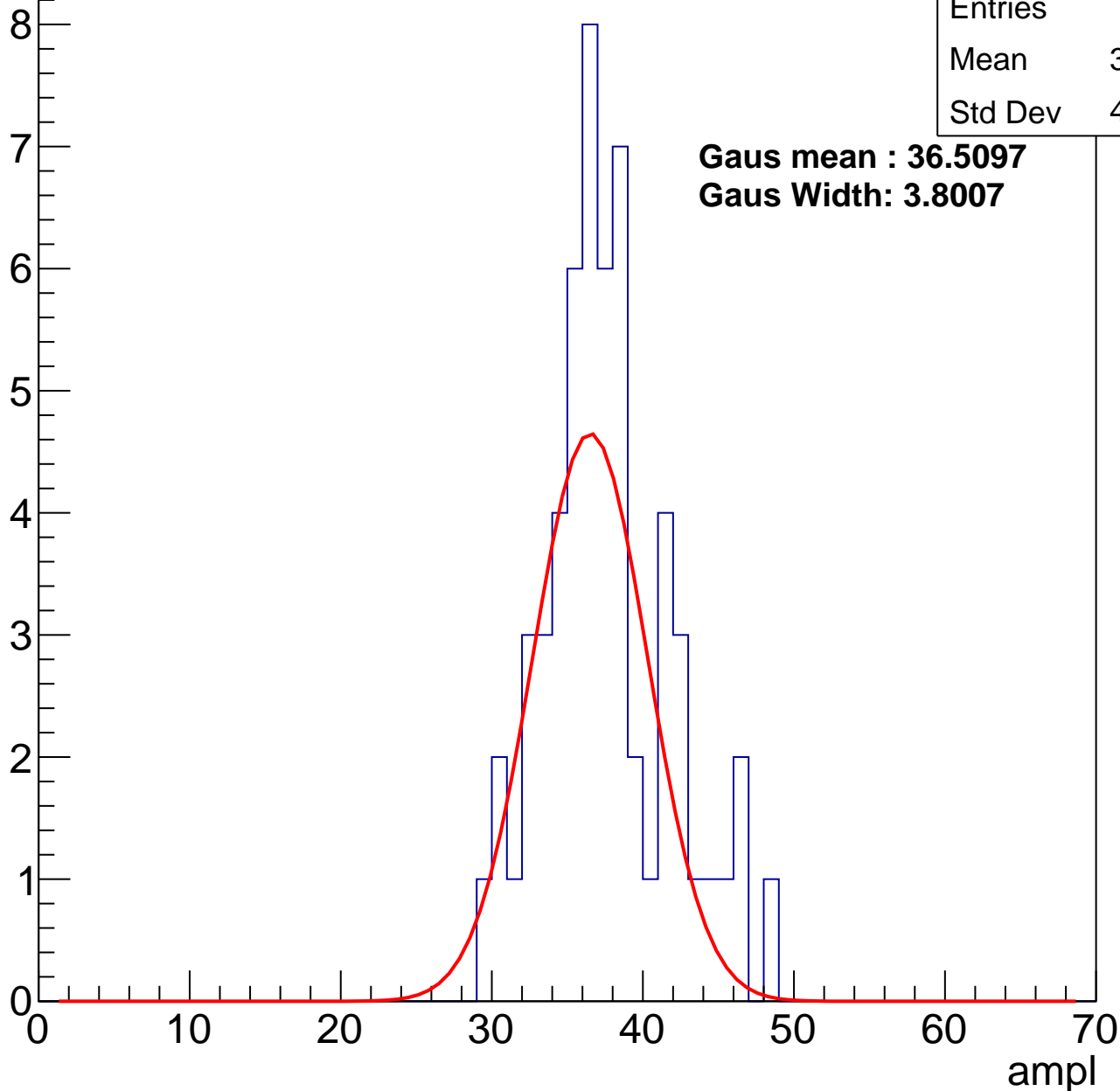
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	57
Mean	37.14
Std Dev	4.153

**Gaus mean : 36.5097**

**Gaus Width: 3.8007**



# B1L103S, U11-ch66, adc2

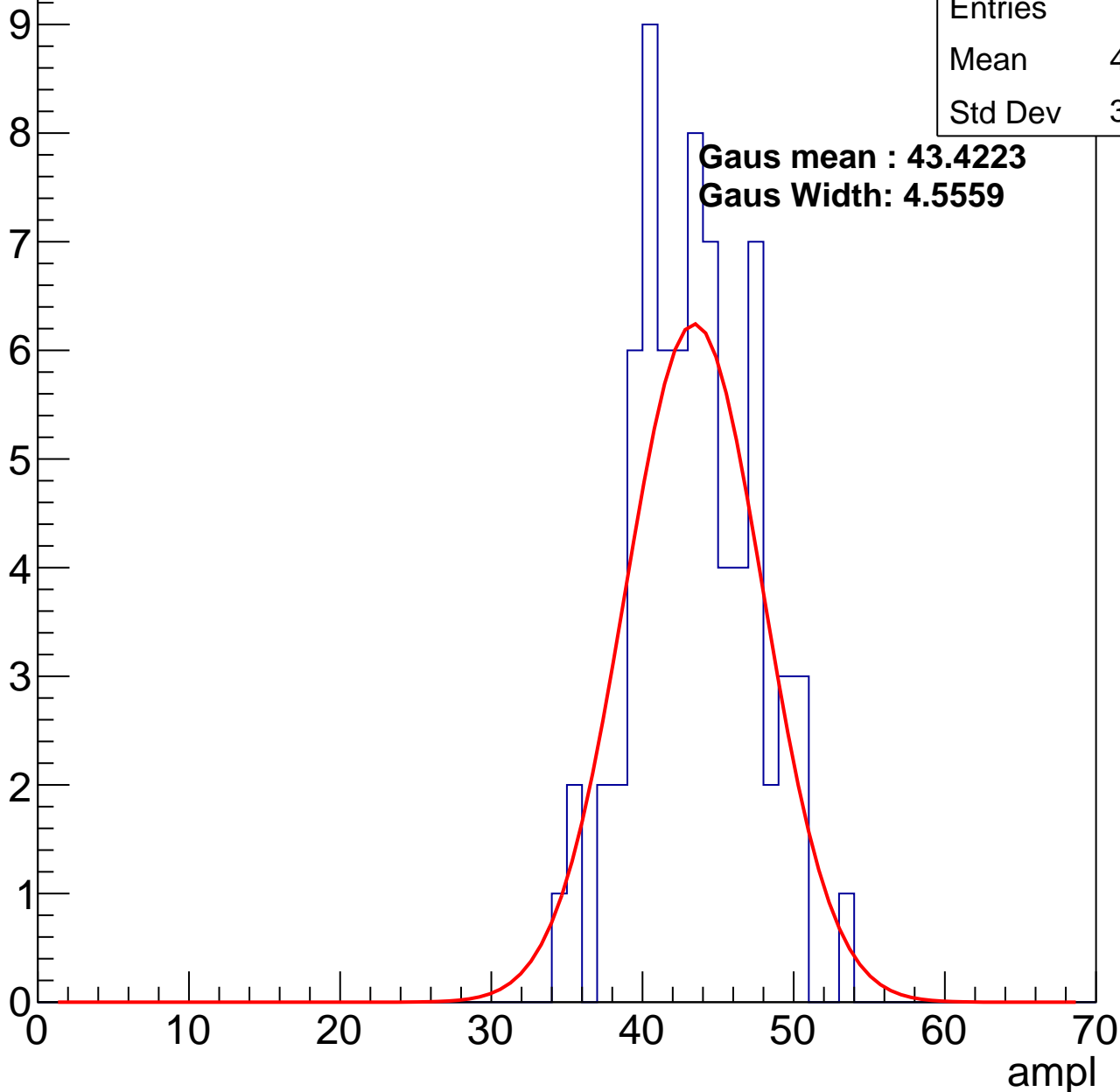
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	73
Mean	42.97
Std Dev	3.906

**Gaus mean : 43.4223**

**Gaus Width: 4.5559**



# B1L103S, U11-ch66, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

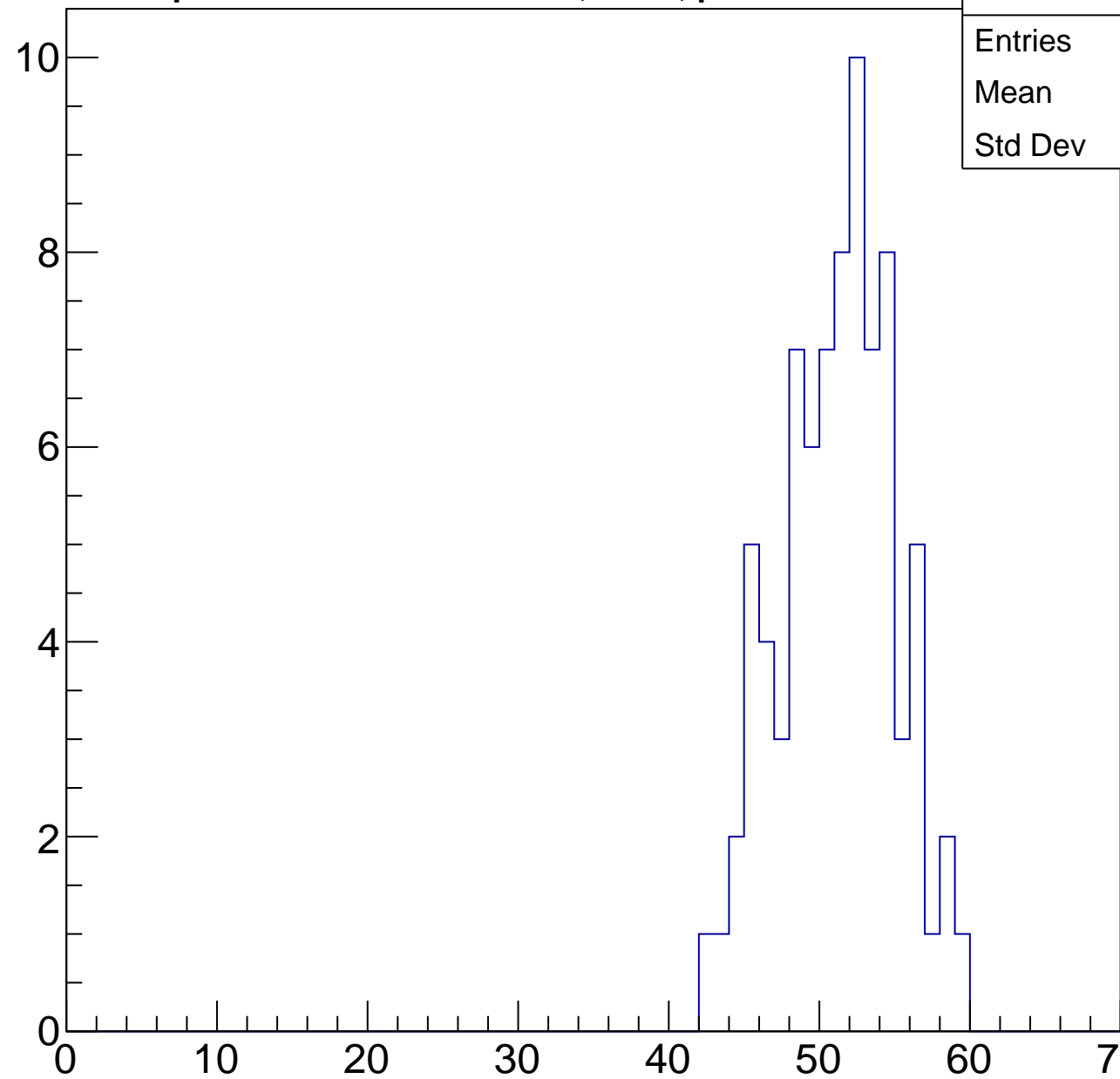
Entries	81
Mean	50.75
Std Dev	3.753

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

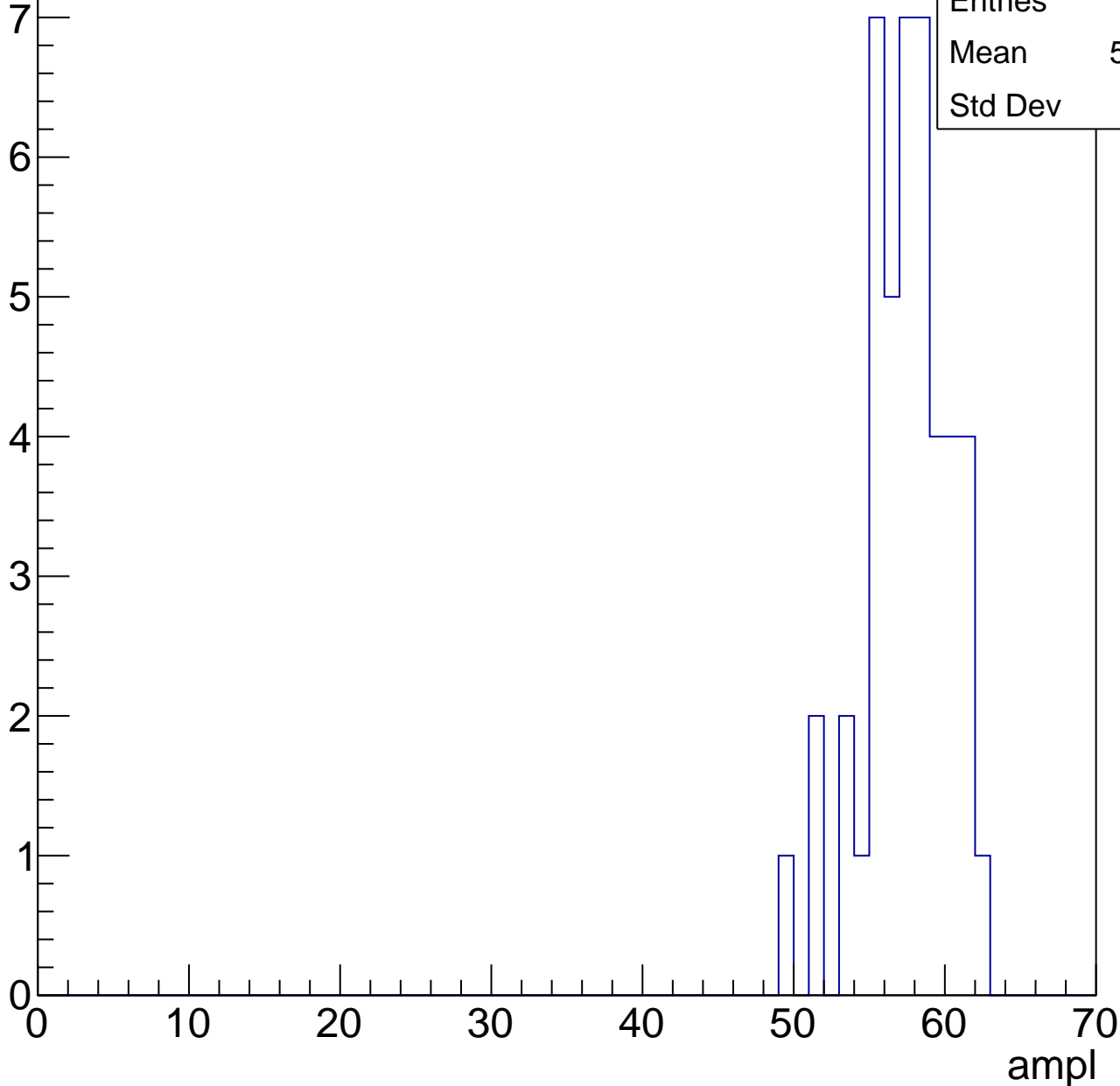


# B1L103S, U11-ch66, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	45
Mean	56.96
Std Dev	2.82

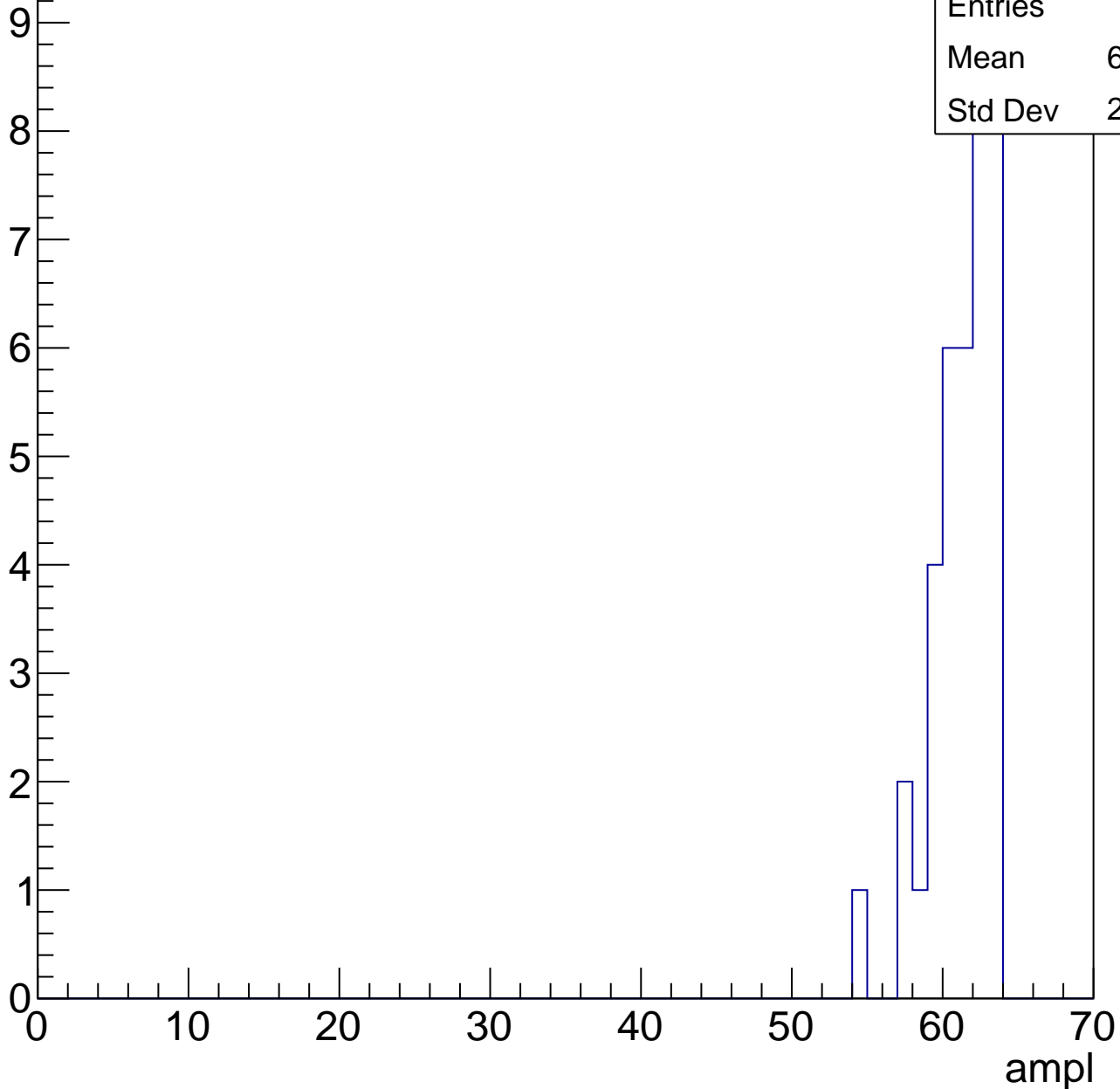


# B1L103S, U11-ch66, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

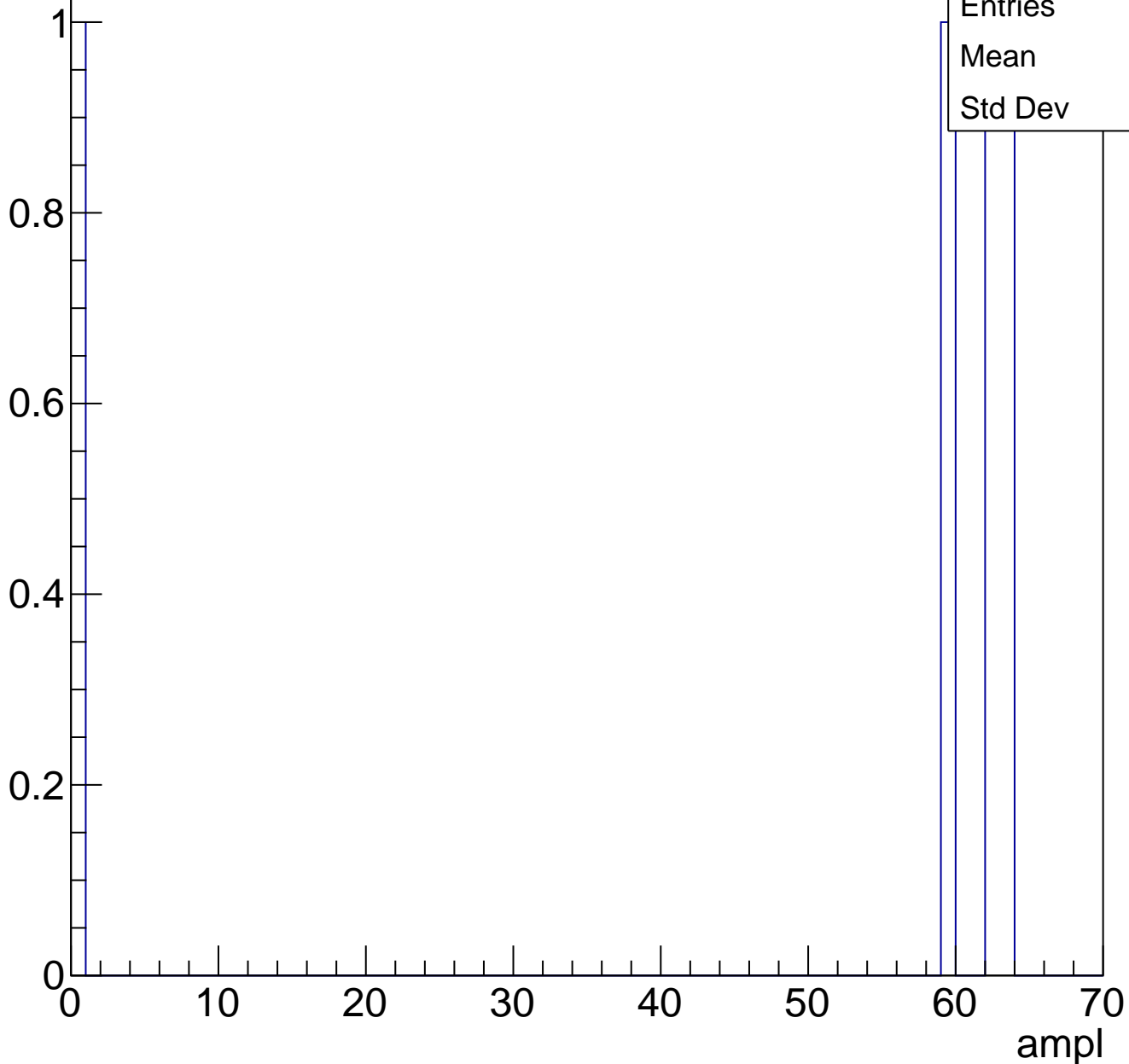
Entries	37
Mean	60.84
Std Dev	2.047



# B1L103S, U11-ch66, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U11-ch66, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U11-ch67, adc0

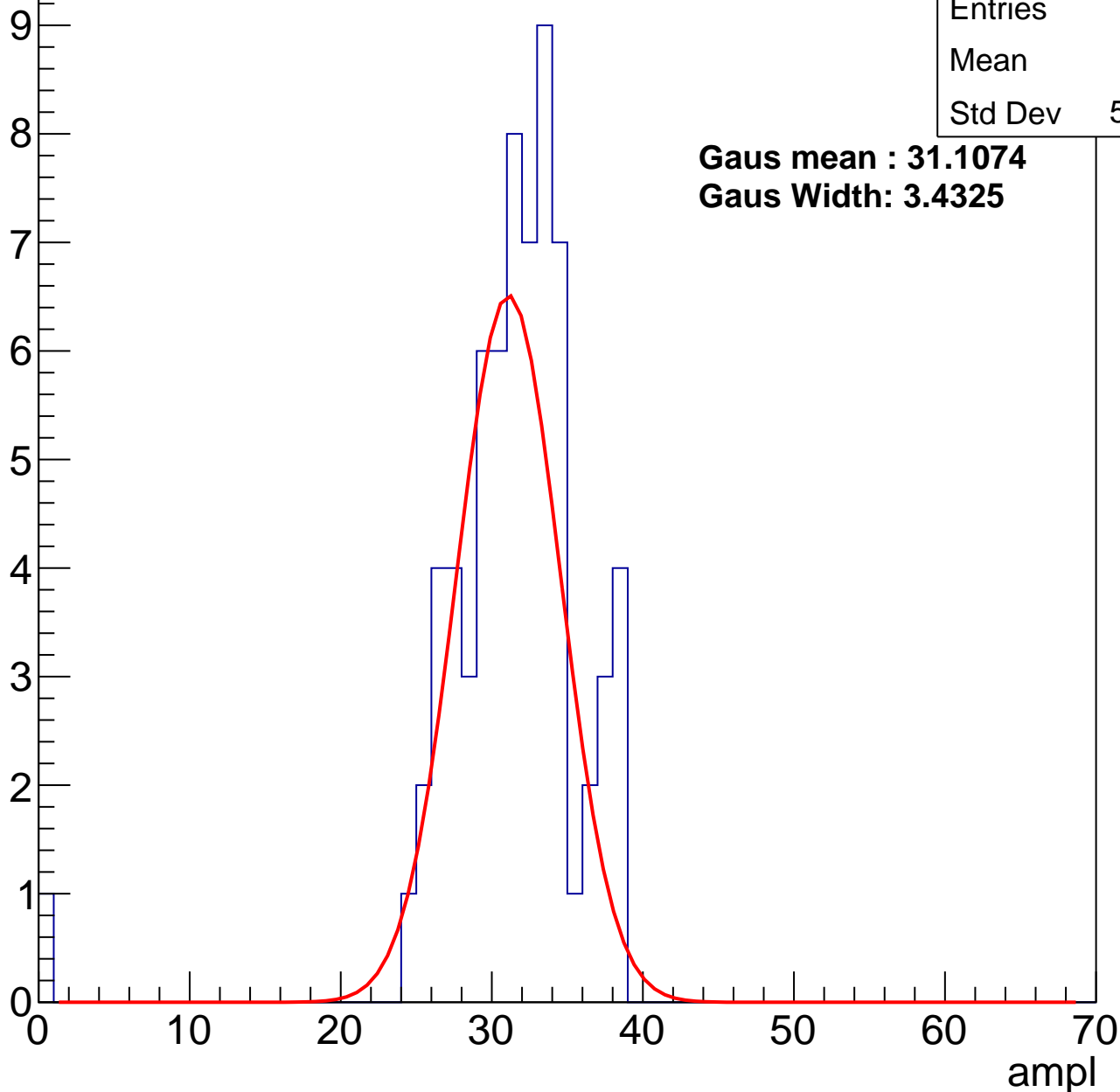
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	68
Mean	30.9
Std Dev	5.114

**Gaus mean : 31.1074**

**Gaus Width: 3.4325**



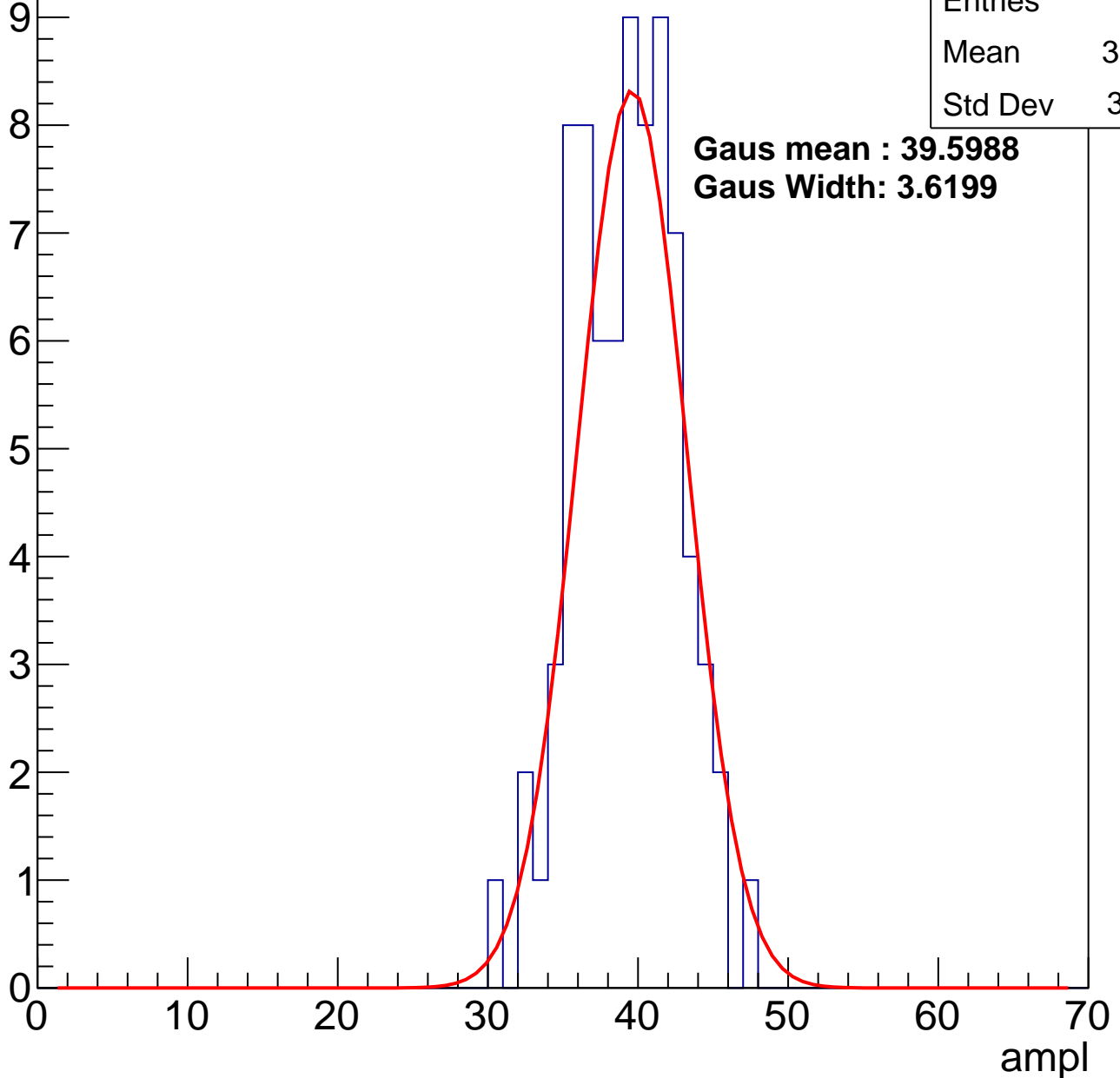
# B1L103S, U11-ch67, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	78
Mean	38.74
Std Dev	3.391

**Gaus mean : 39.5988**  
**Gaus Width: 3.6199**



# B1L103S, U11-ch67, adc2

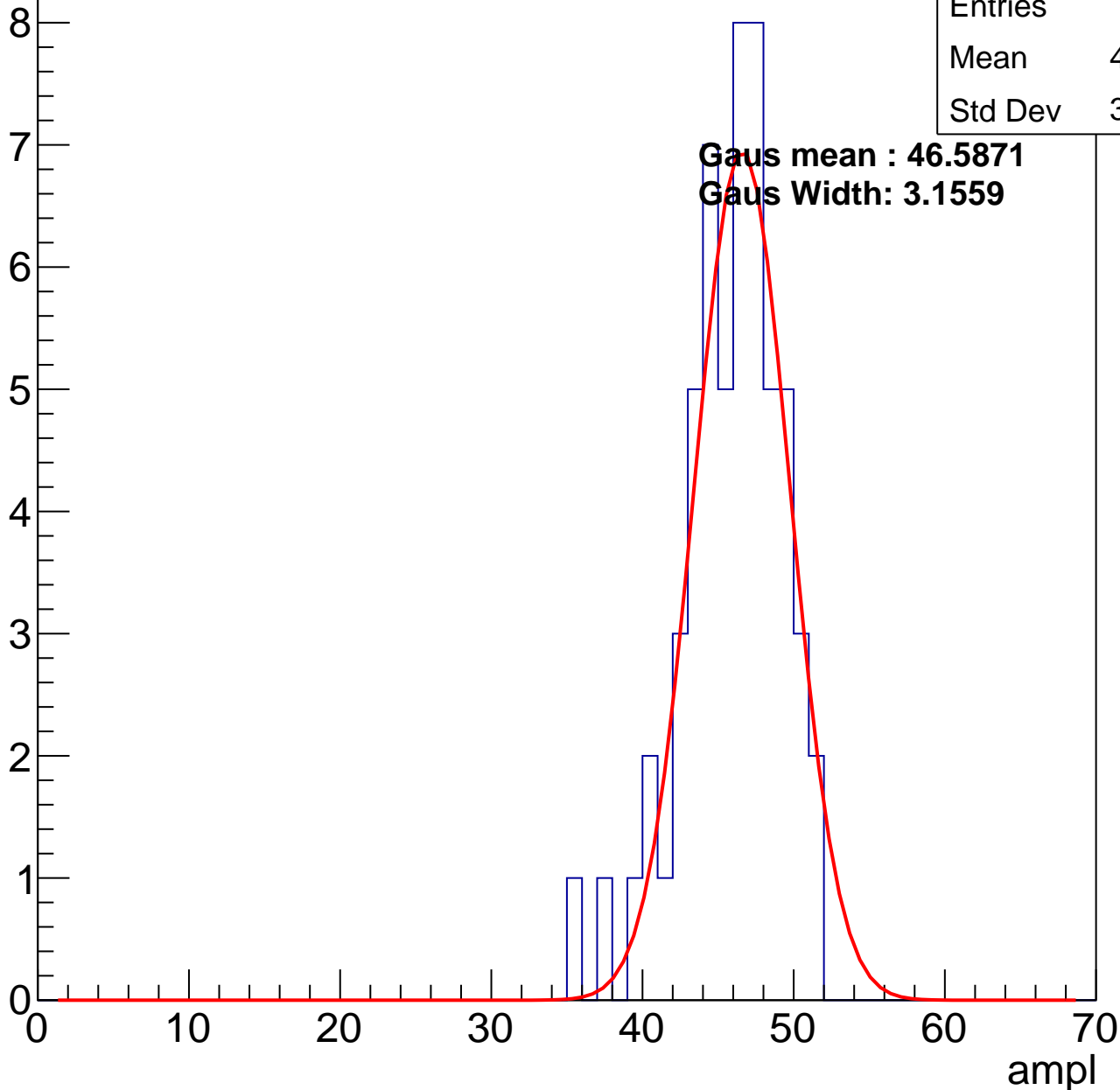
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	57
Mean	45.39
Std Dev	3.307

**Gaus mean : 46.5871**

**Gaus Width: 3.1559**

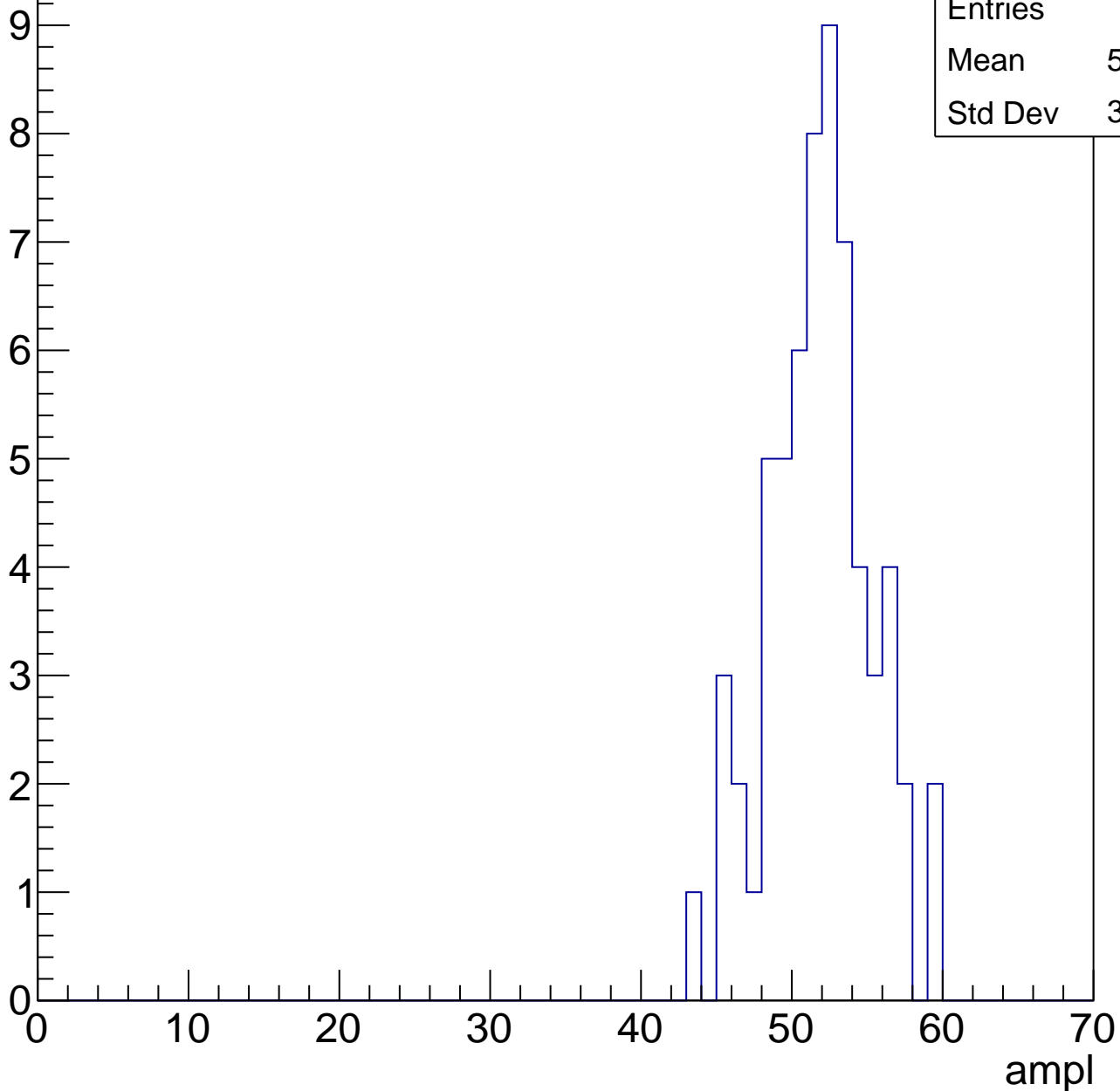


# B1L103S, U11-ch67, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	51.39
Std Dev	3.409

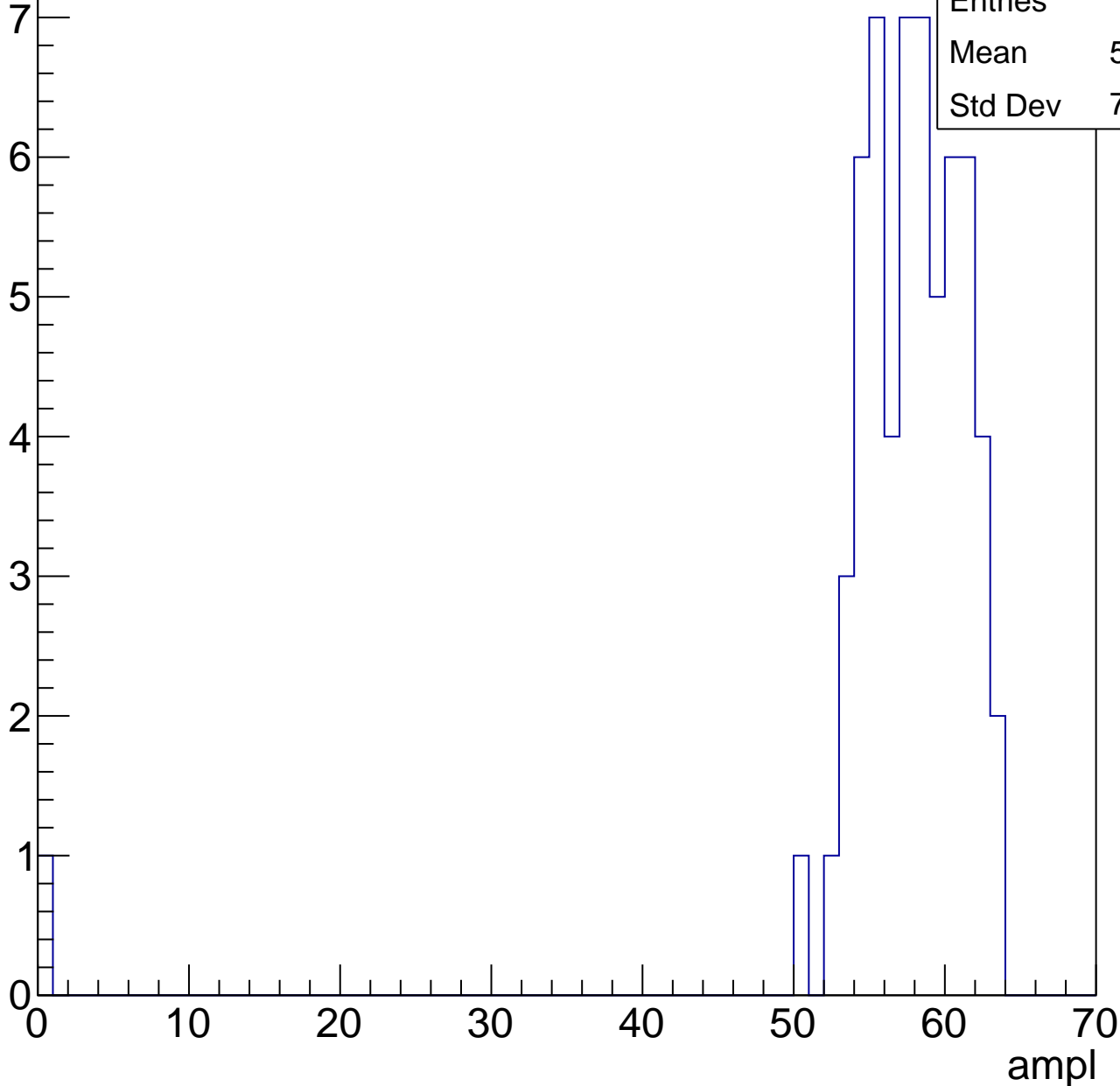


# B1L103S, U11-ch67, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

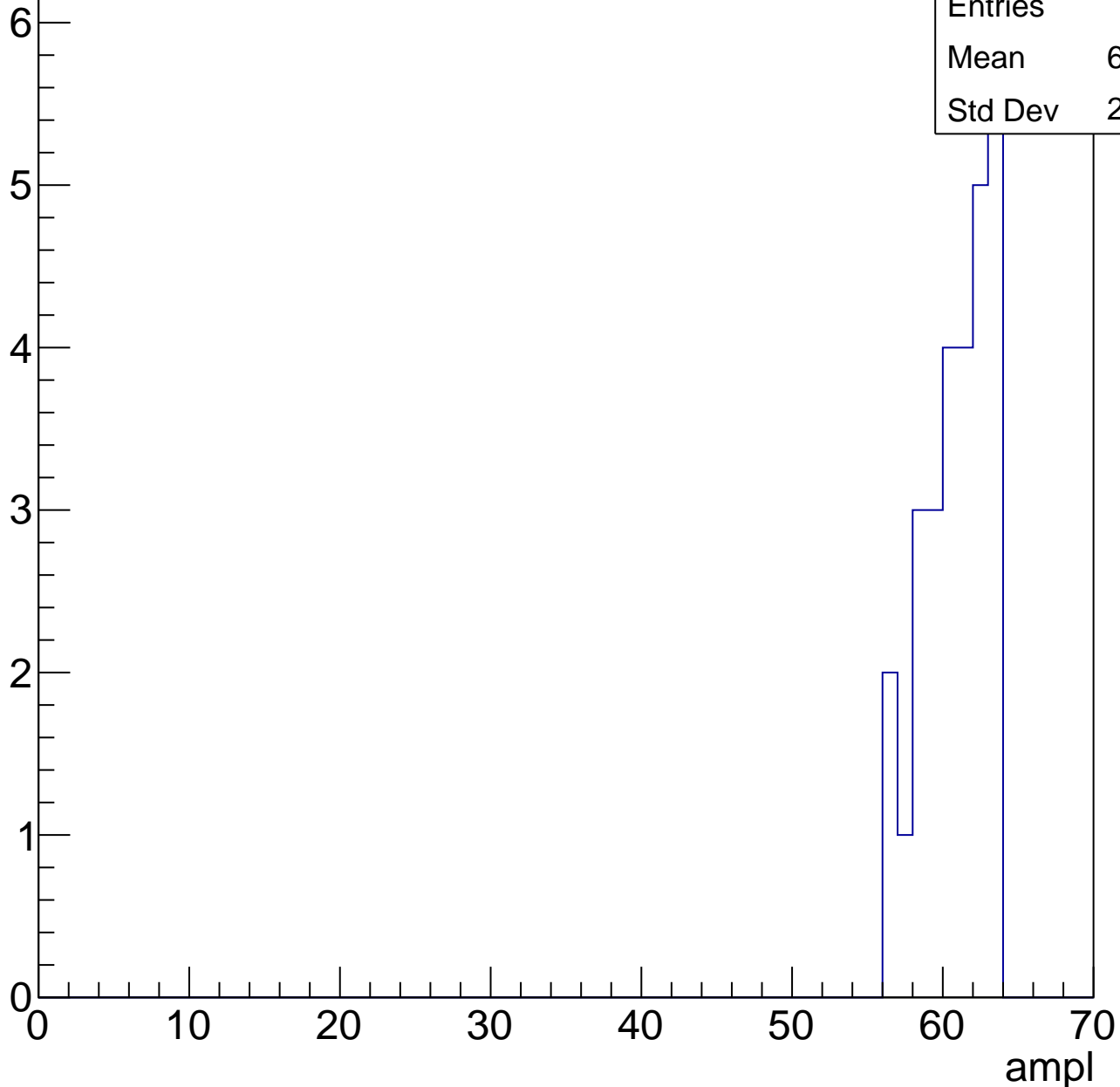
Entries	60
Mean	56.57
Std Dev	7.953



# B1L103S, U11-ch67, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U11-ch67, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	3
Mean	62.67
Std Dev	0.4714

ampl

0 10 20 30 40 50 60 70



# B1L103S, U11-ch67, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U11-ch68, adc0

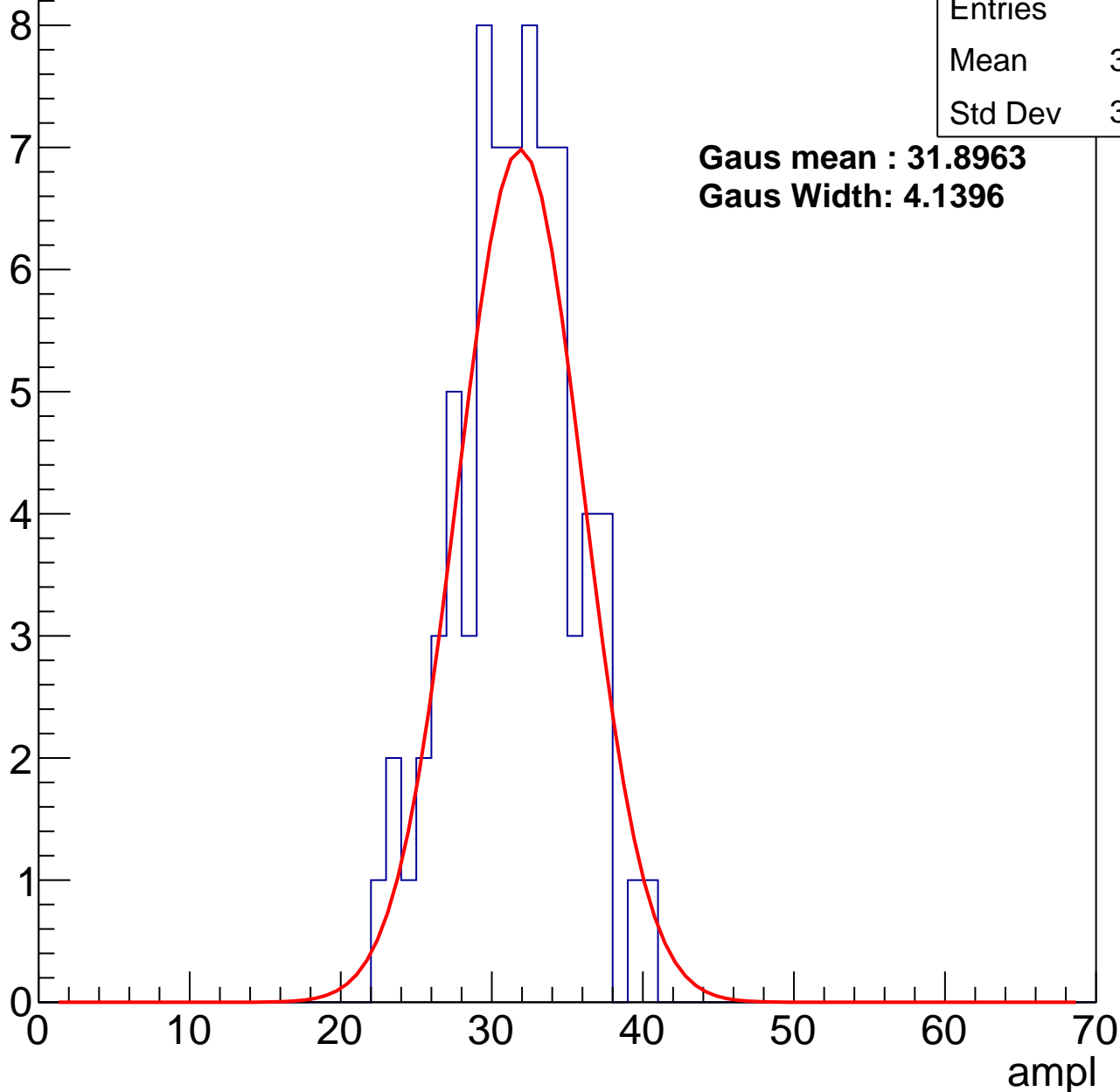
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	74
Mean	31.07
Std Dev	3.832

**Gaus mean : 31.8963**

**Gaus Width: 4.1396**



# B1L103S, U11-ch68, adc1

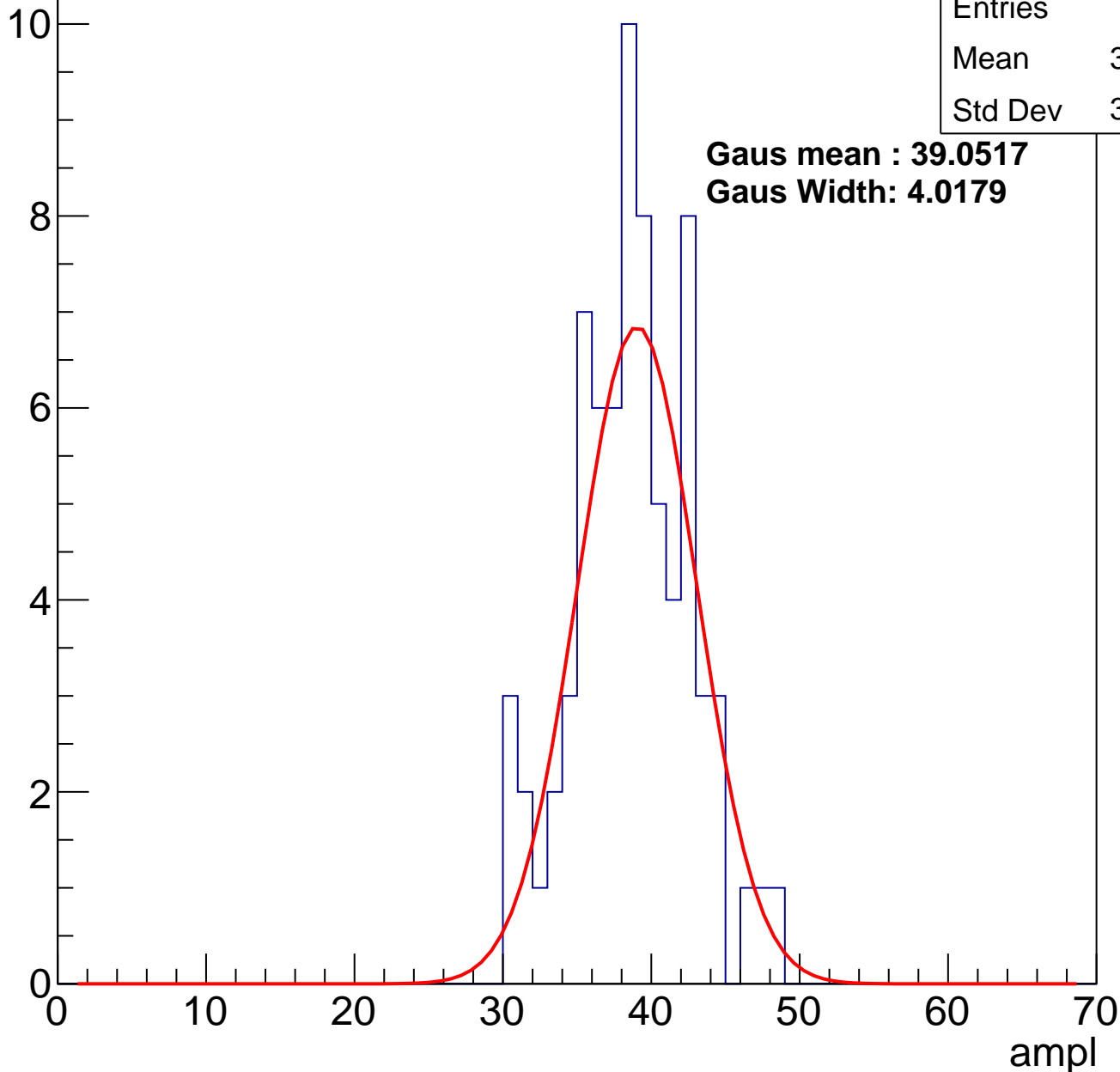
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	74
Mean	38.23
Std Dev	3.913

**Gaus mean : 39.0517**

**Gaus Width: 4.0179**

Entry



# B1L103S, U11-ch68, adc2

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	61
Mean	45.61
Std Dev	3.645

**Gaus mean : 45.9761**

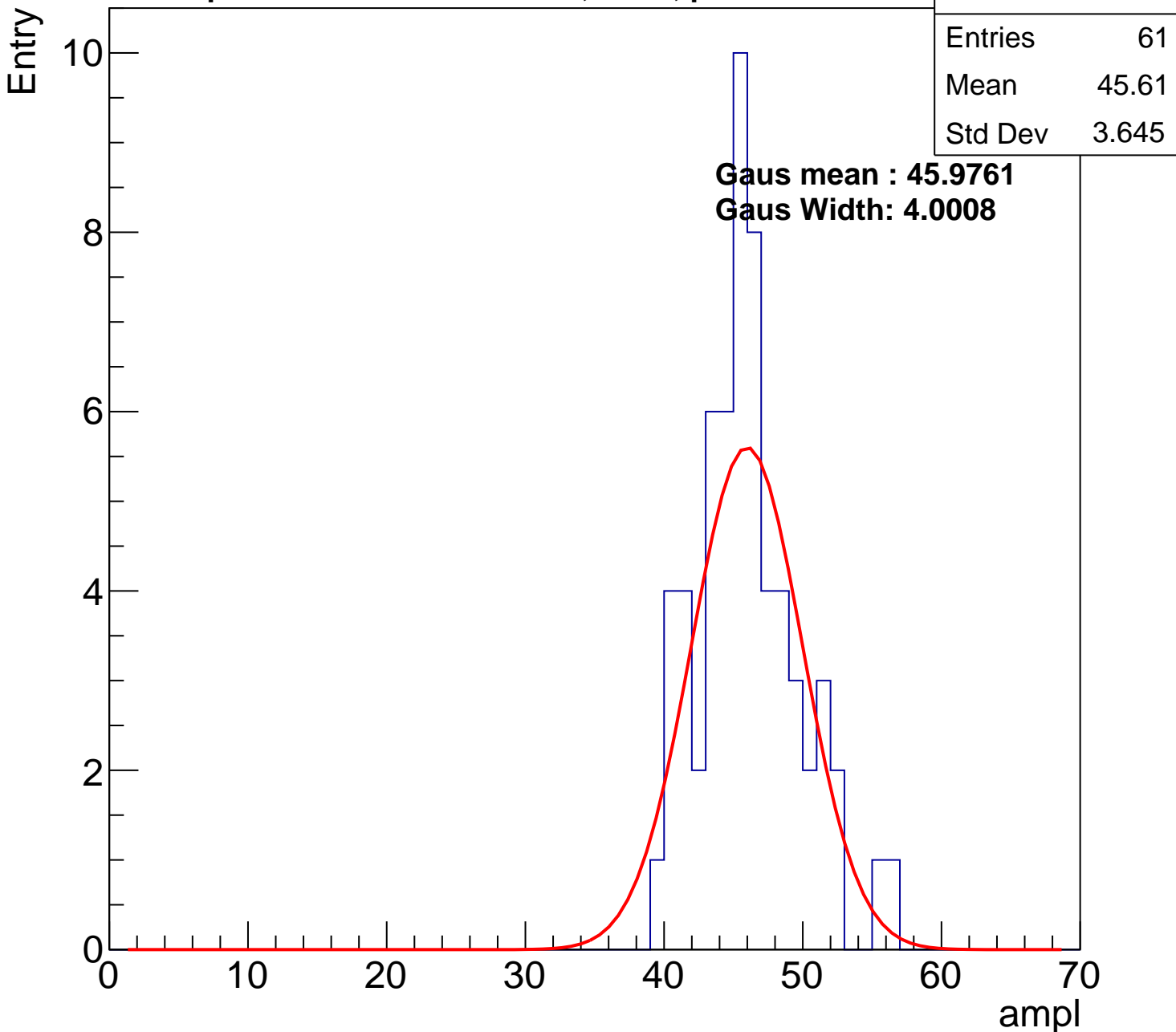
**Gaus Width: 4.0008**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

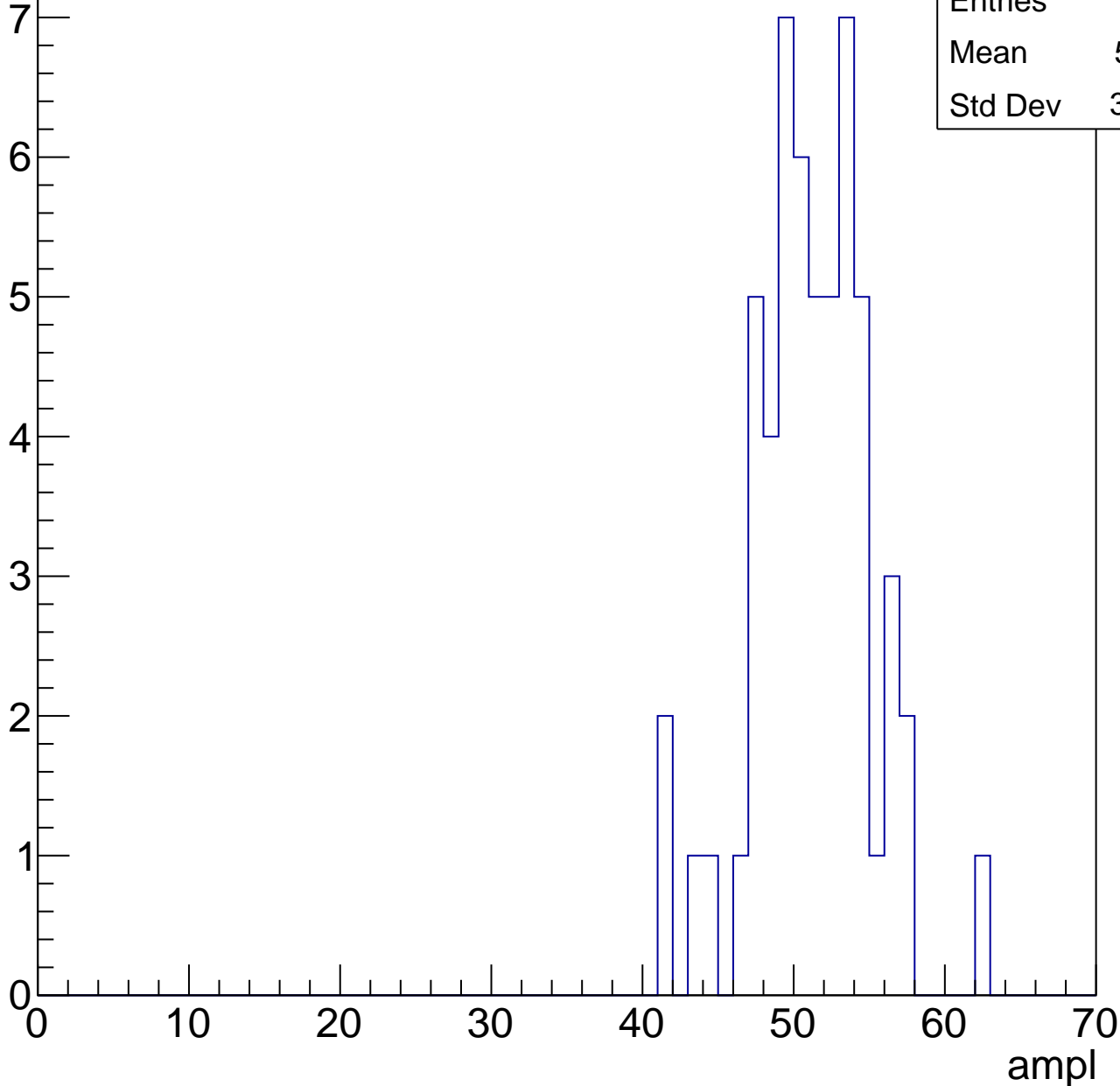


# B1L103S, U11-ch68, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	56
Mean	50.71
Std Dev	3.885

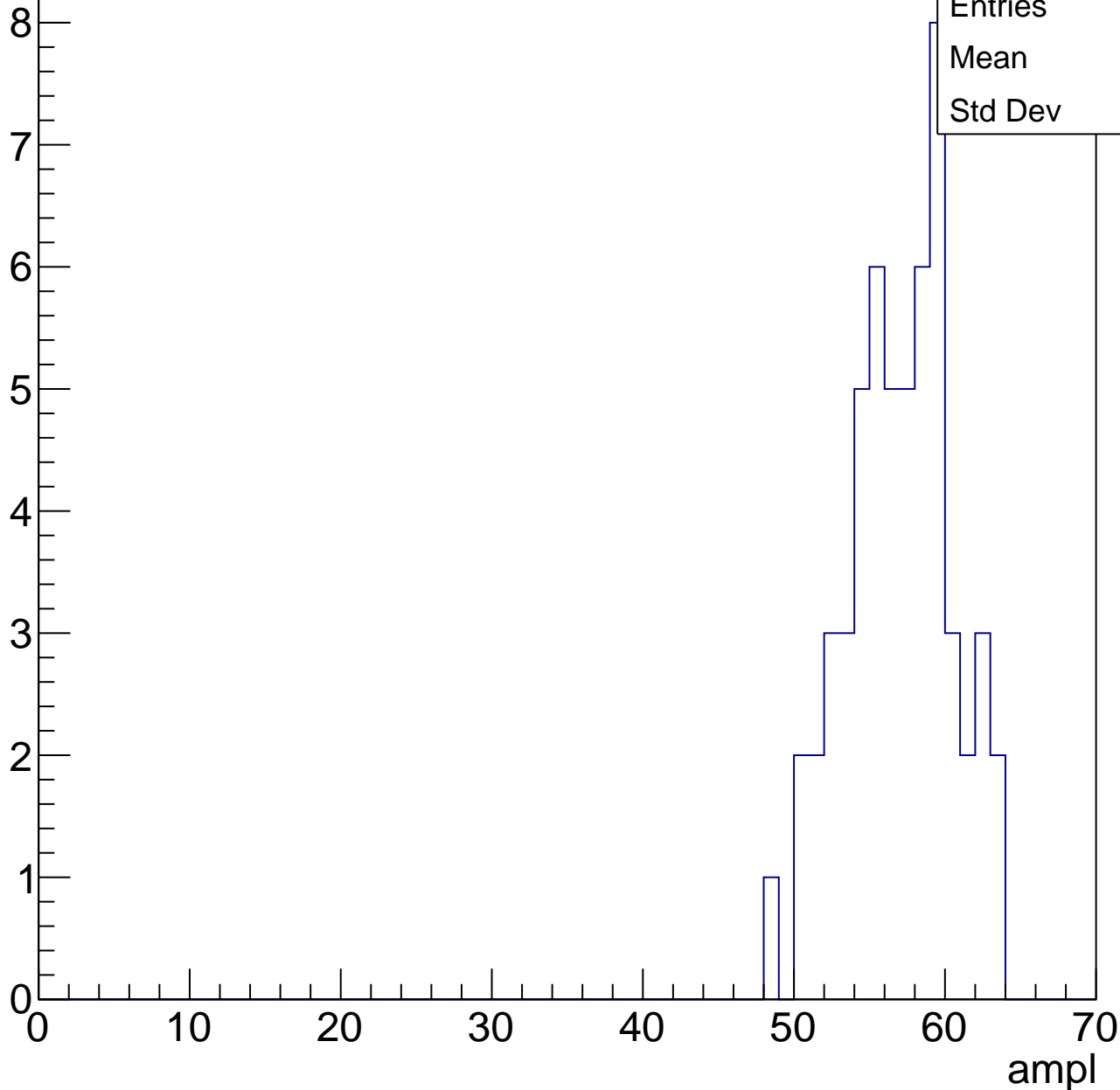


# B1L103S, U11-ch68, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

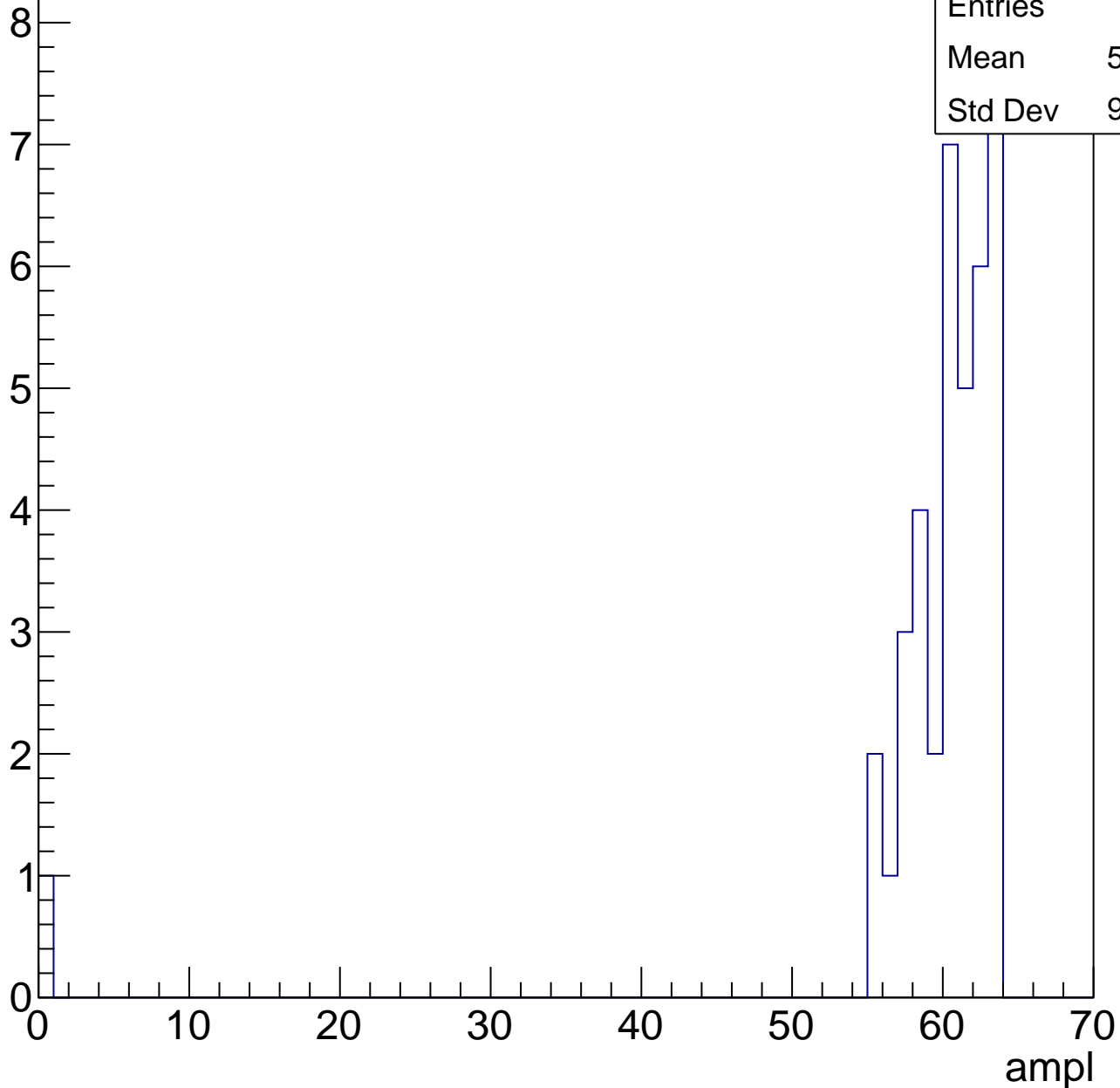
Entries	56
Mean	56.5
Std Dev	3.48



# B1L103S, U11-ch68, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

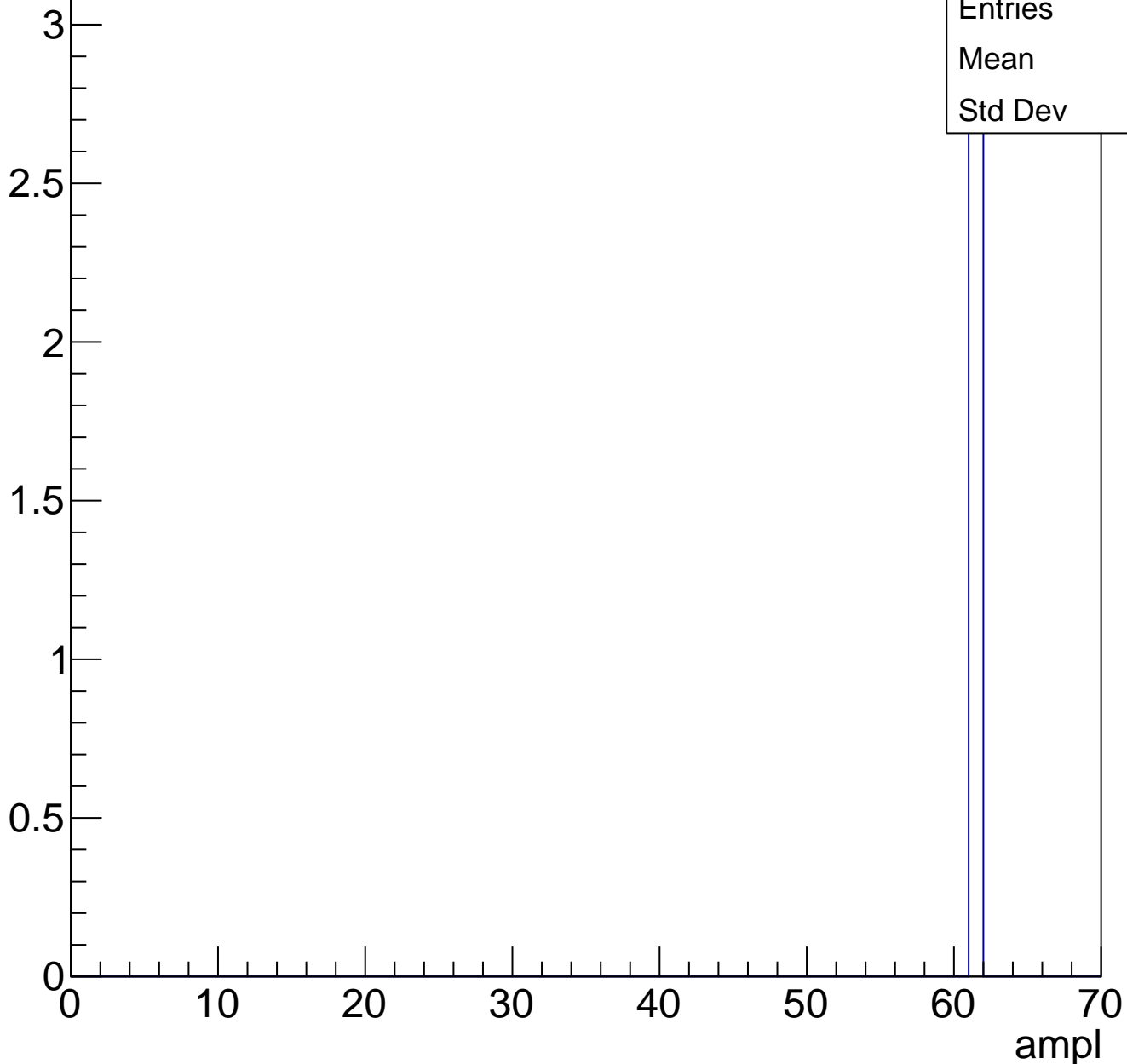
Entry



# B1L103S, U11-ch68, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U11-ch68, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U11-ch69, adc0

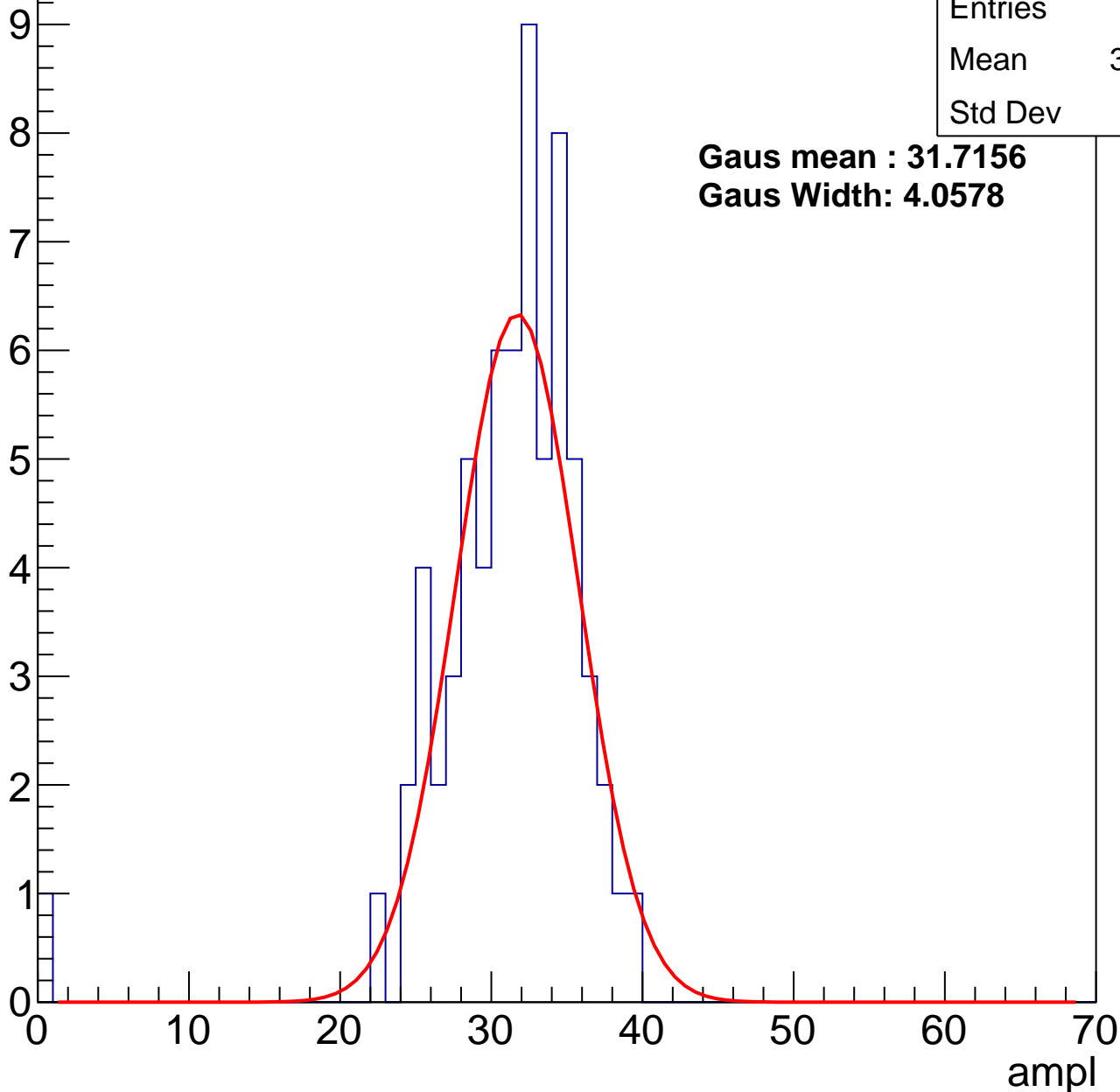
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	68
Mean	30.65
Std Dev	5.26

**Gaus mean : 31.7156**

**Gaus Width: 4.0578**



# B1L103S, U11-ch69, adc1

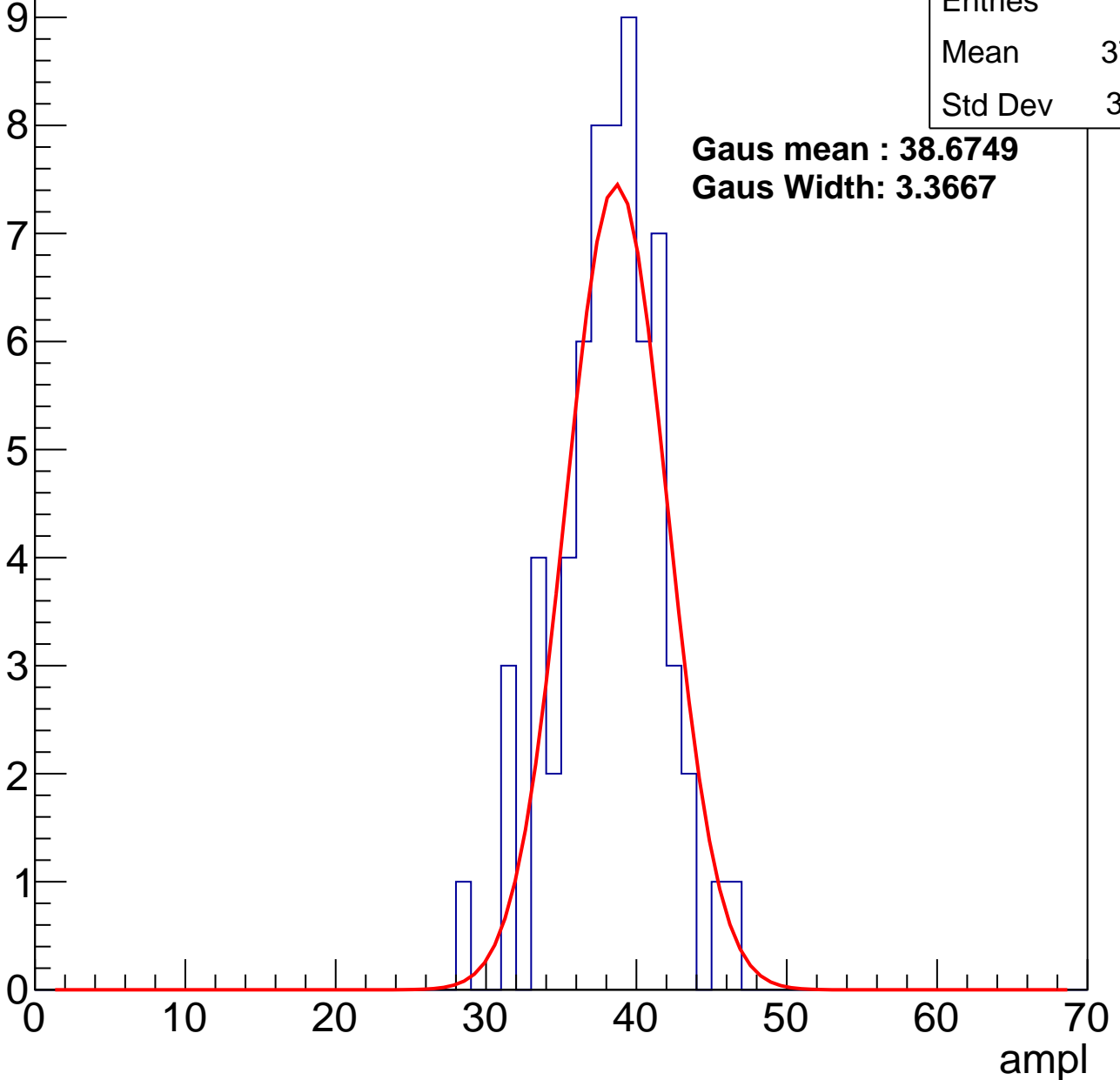
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	37.82
Std Dev	3.401

**Gaus mean : 38.6749**

**Gaus Width: 3.3667**



# B1L103S, U11-ch69, adc2

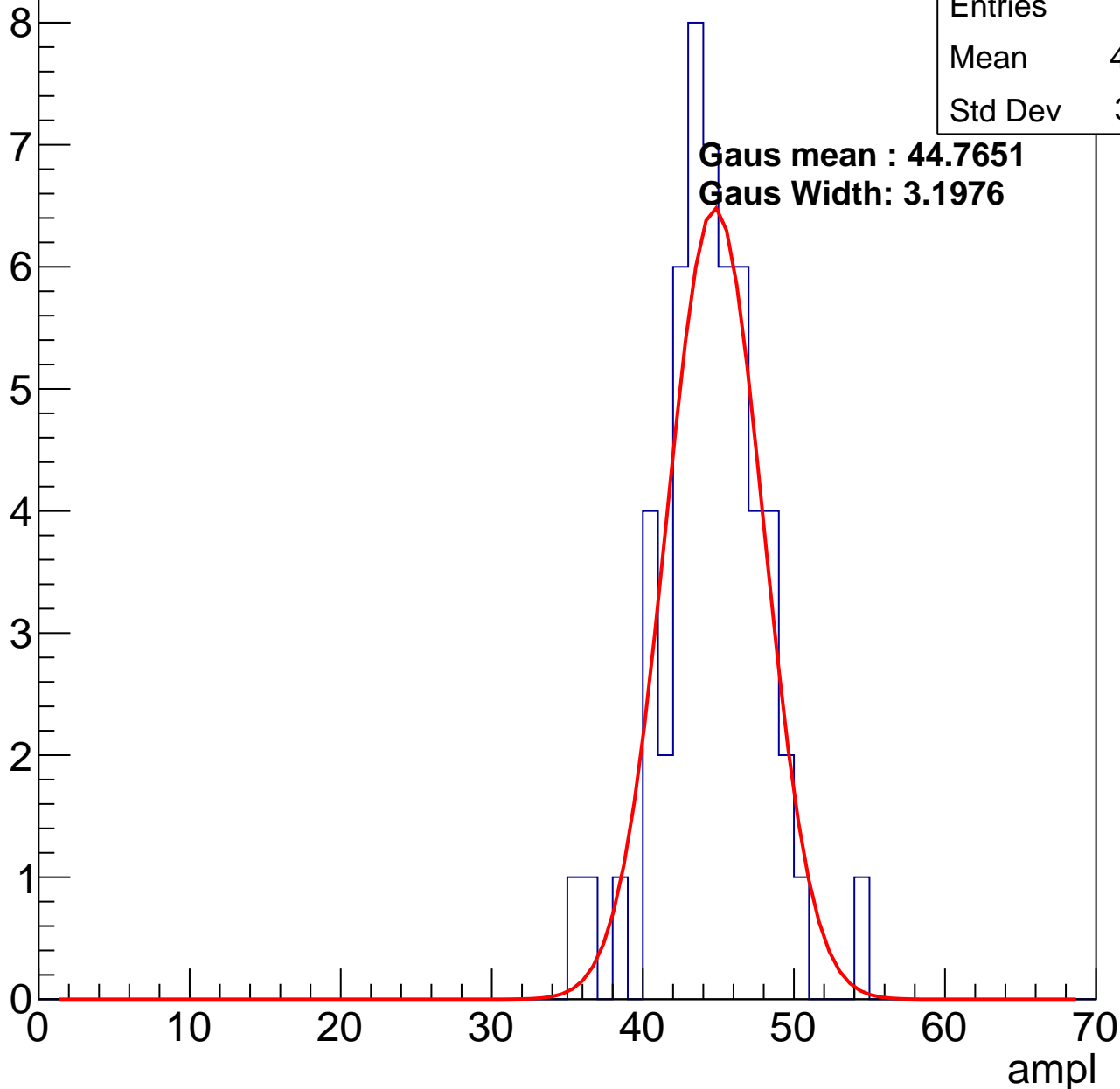
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	54
Mean	44.13
Std Dev	3.361

**Gaus mean : 44.7651**

**Gaus Width: 3.1976**

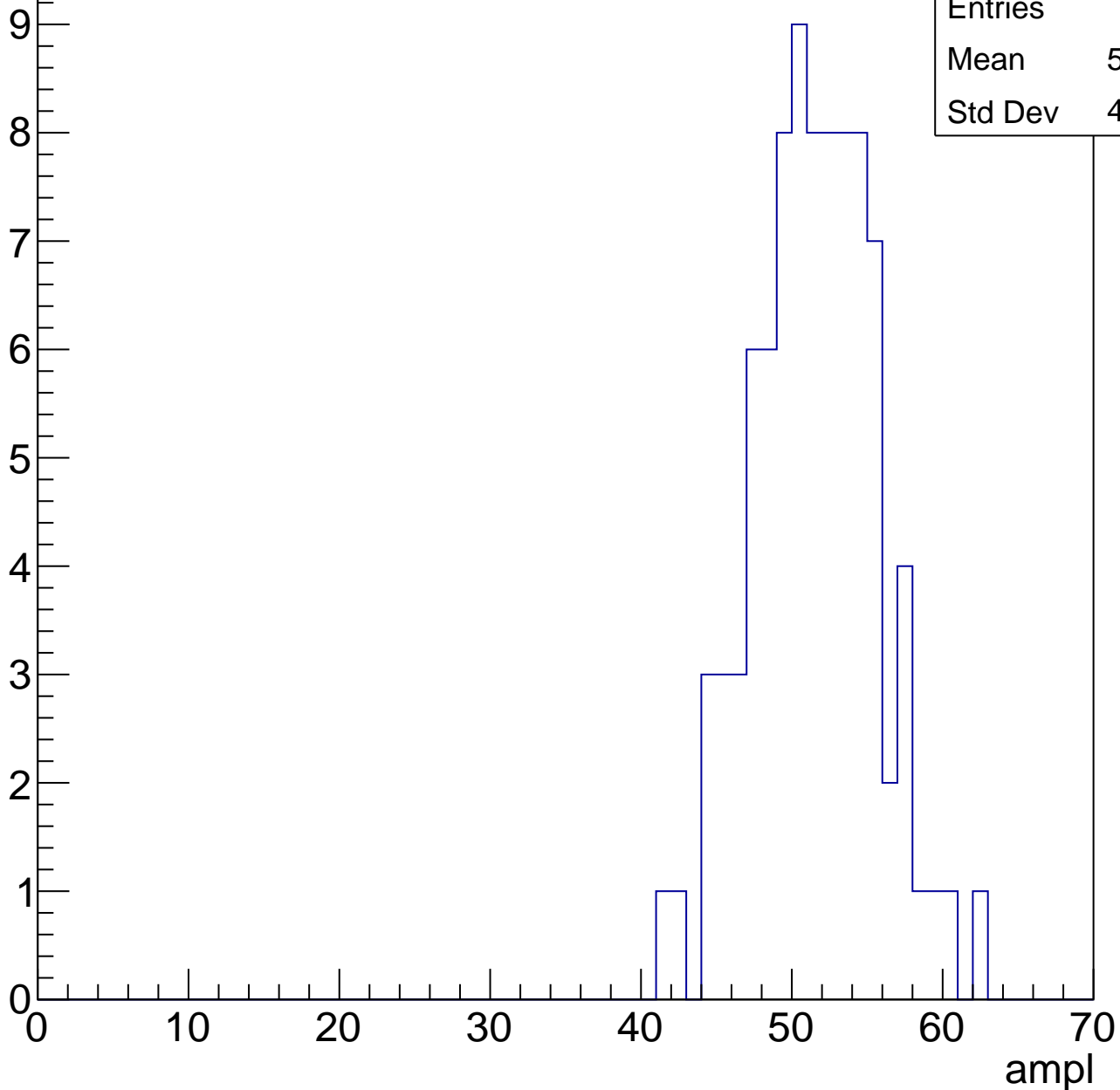


# B1L103S, U11-ch69, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	89
Mean	51.06
Std Dev	4.015

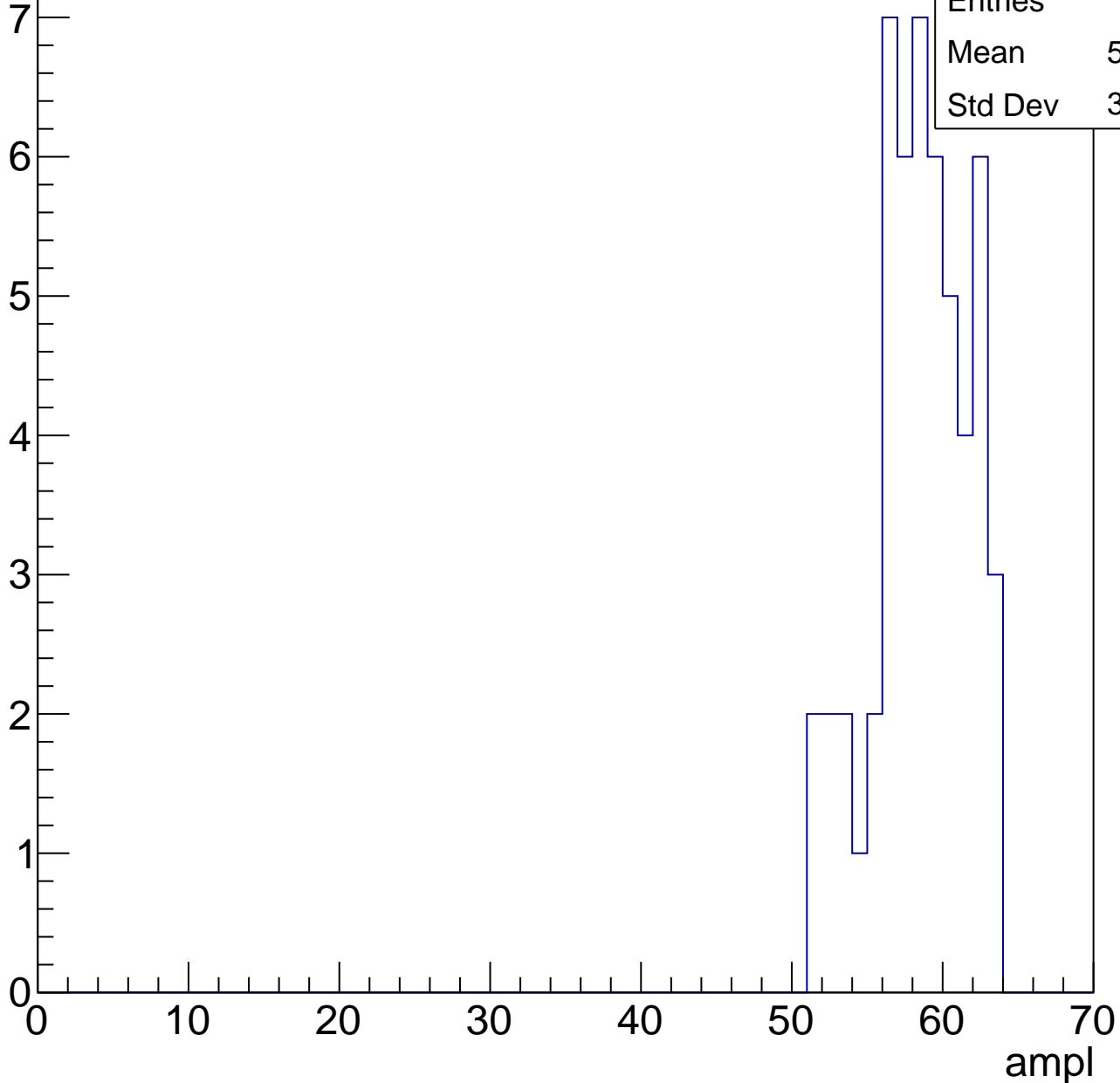


# B1L103S, U11-ch69, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	53
Mean	58.02
Std Dev	3.135

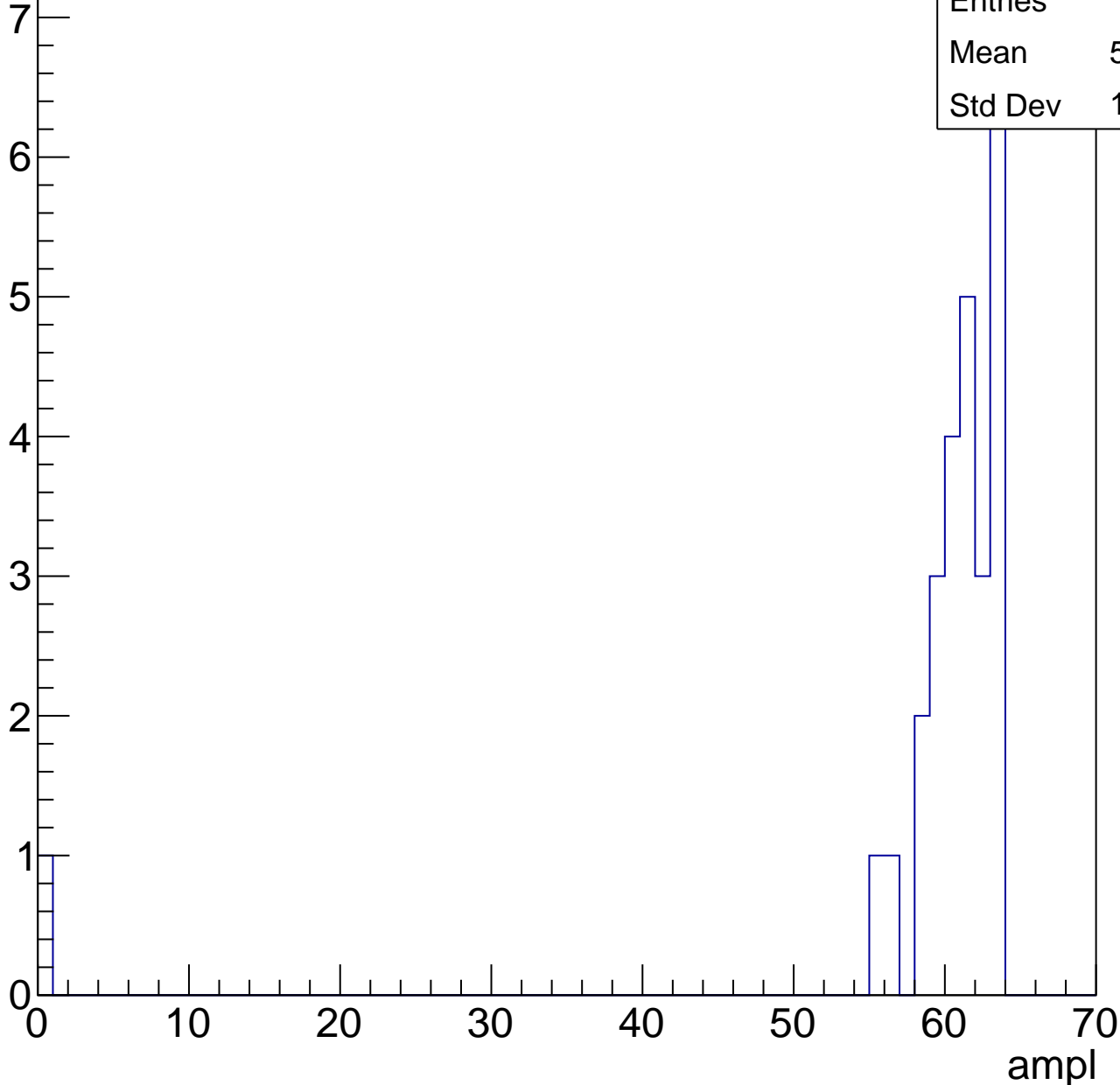


# B1L103S, U11-ch69, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	27
Mean	58.37
Std Dev	11.64



# B1L103S, U11-ch69, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U11-ch69, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L103S, U11-ch70, adc0

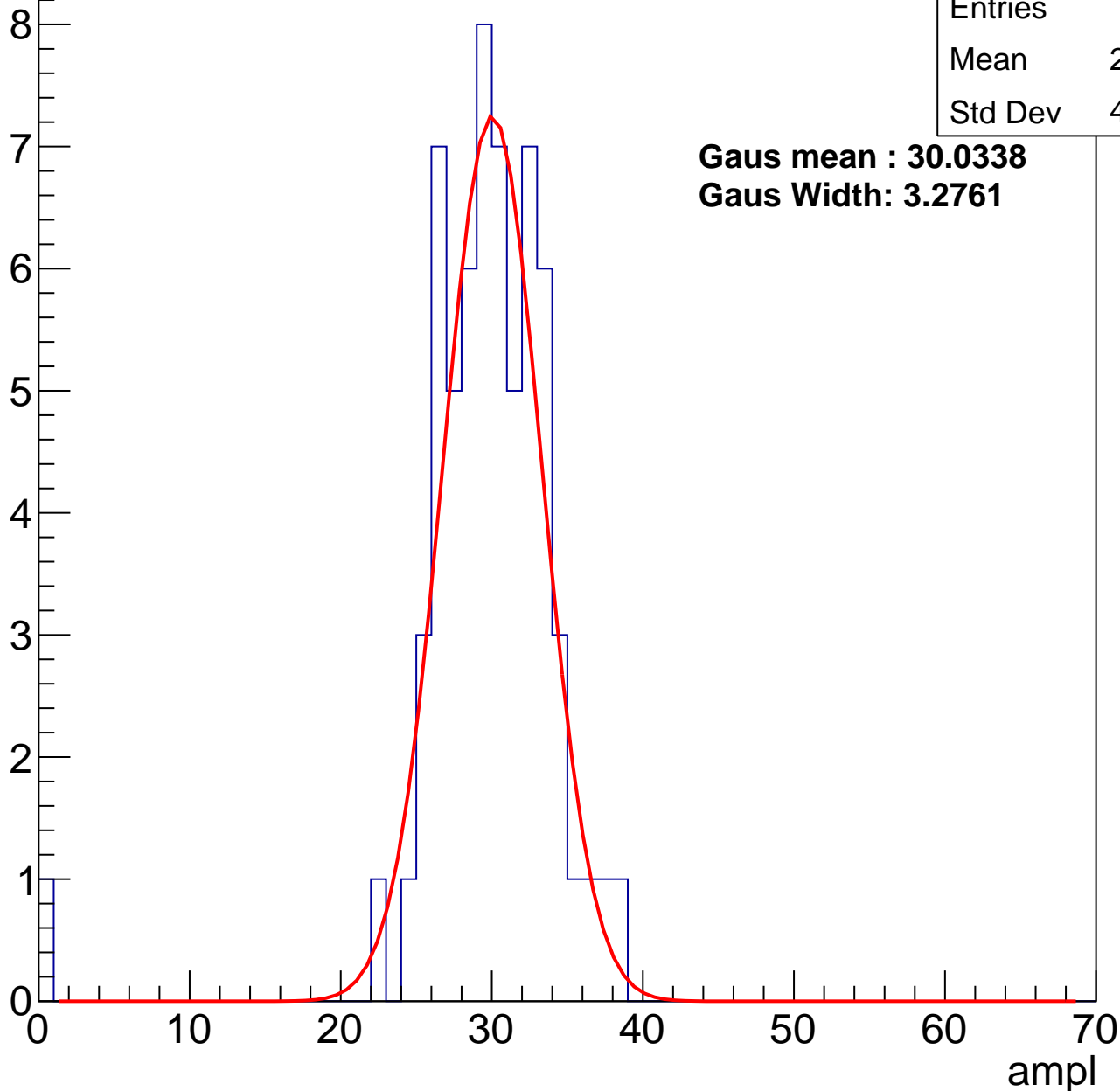
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	29.27
Std Dev	4.903

**Gaus mean : 30.0338**

**Gaus Width: 3.2761**



# B1L103S, U11-ch70, adc1

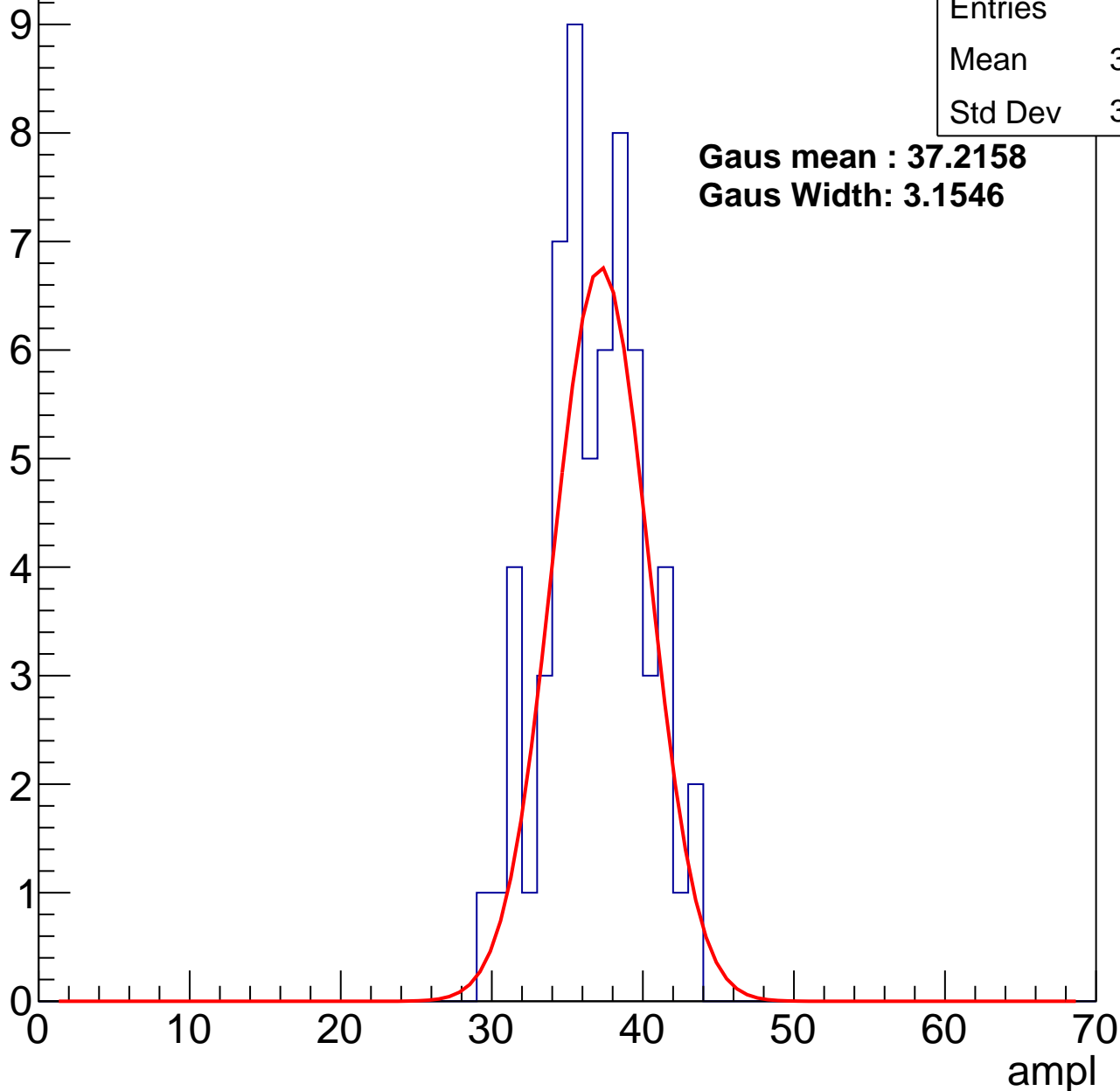
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	61
Mean	36.38
Std Dev	3.215

**Gaus mean : 37.2158**

**Gaus Width: 3.1546**



# B1L103S, U11-ch70, adc2

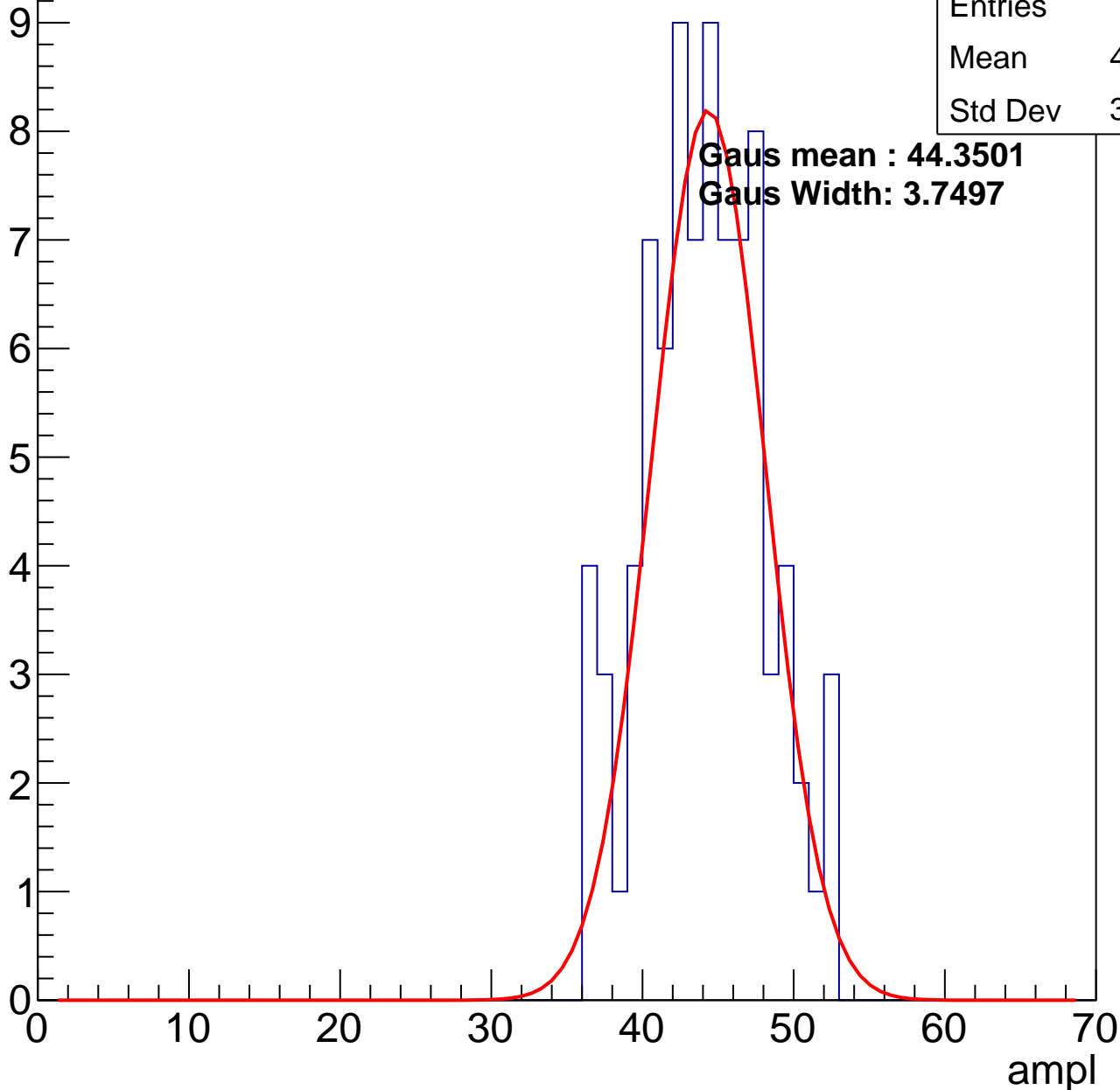
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	85
Mean	43.65
Std Dev	3.919

**Gaus mean : 44.3501**

**Gaus Width: 3.7497**

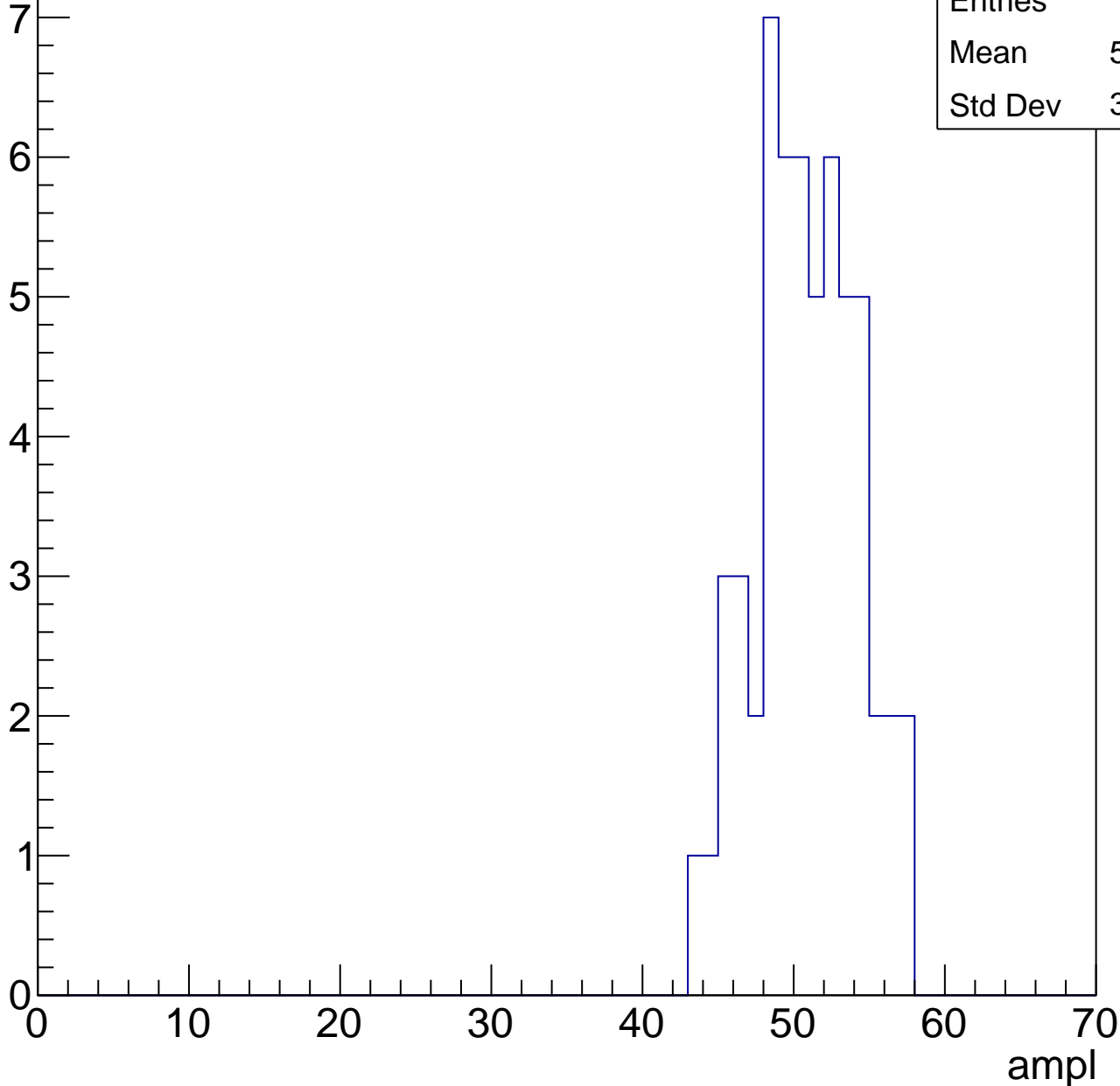


# B1L103S, U11-ch70, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

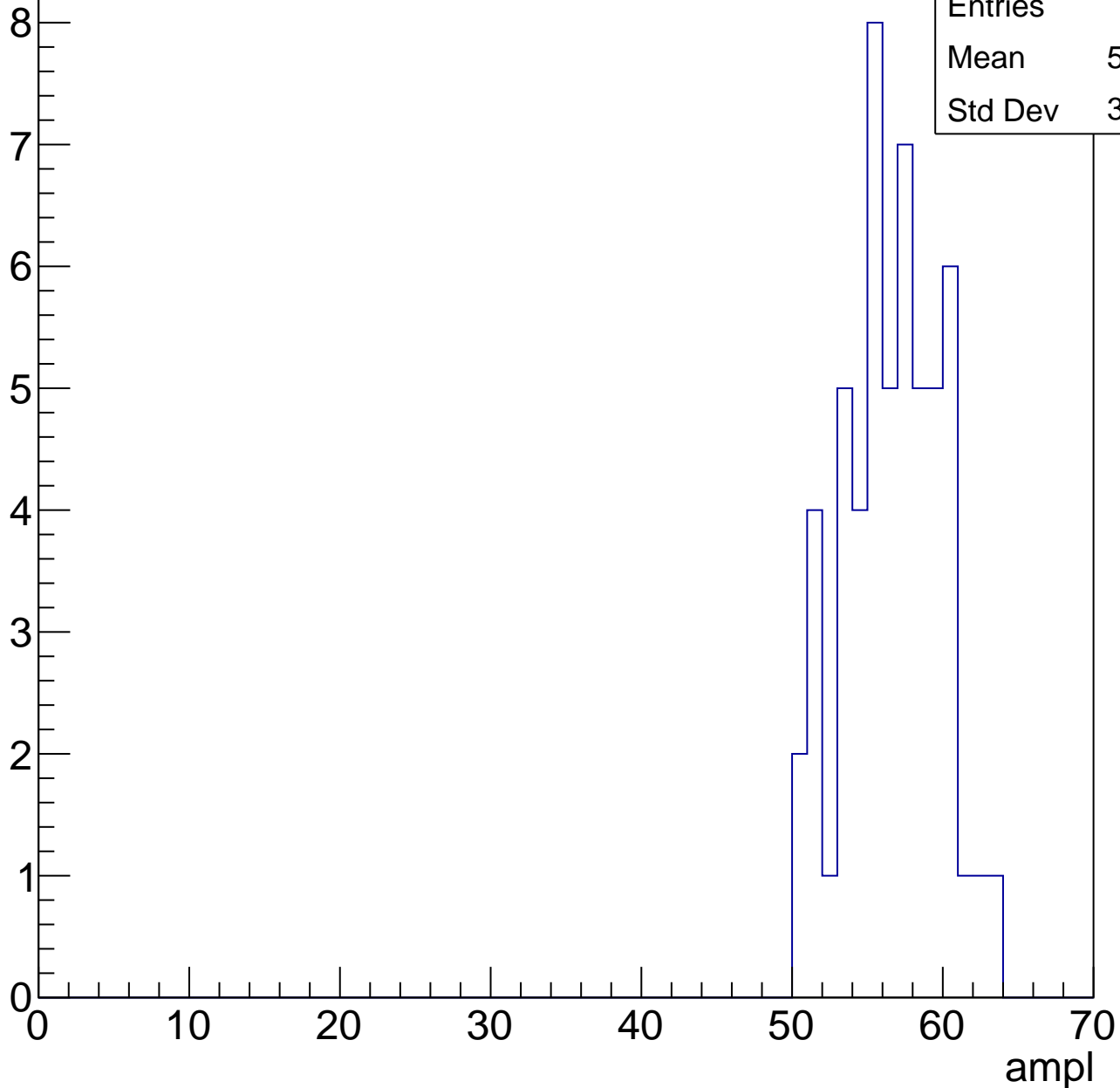
Entries	56
Mean	50.39
Std Dev	3.342



# B1L103S, U11-ch70, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



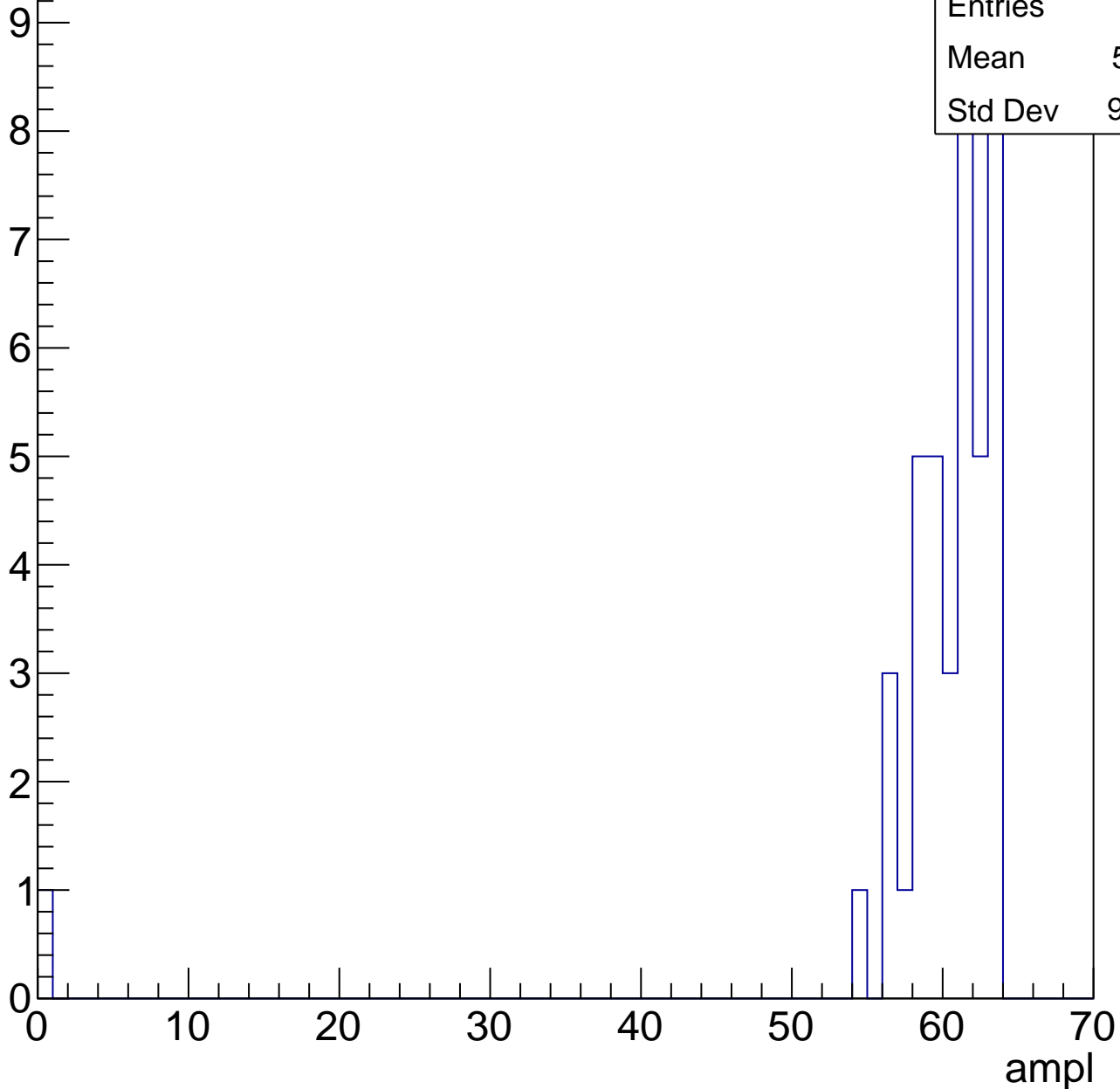
Entries	55
Mean	56.13
Std Dev	3.116

# B1L103S, U11-ch70, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

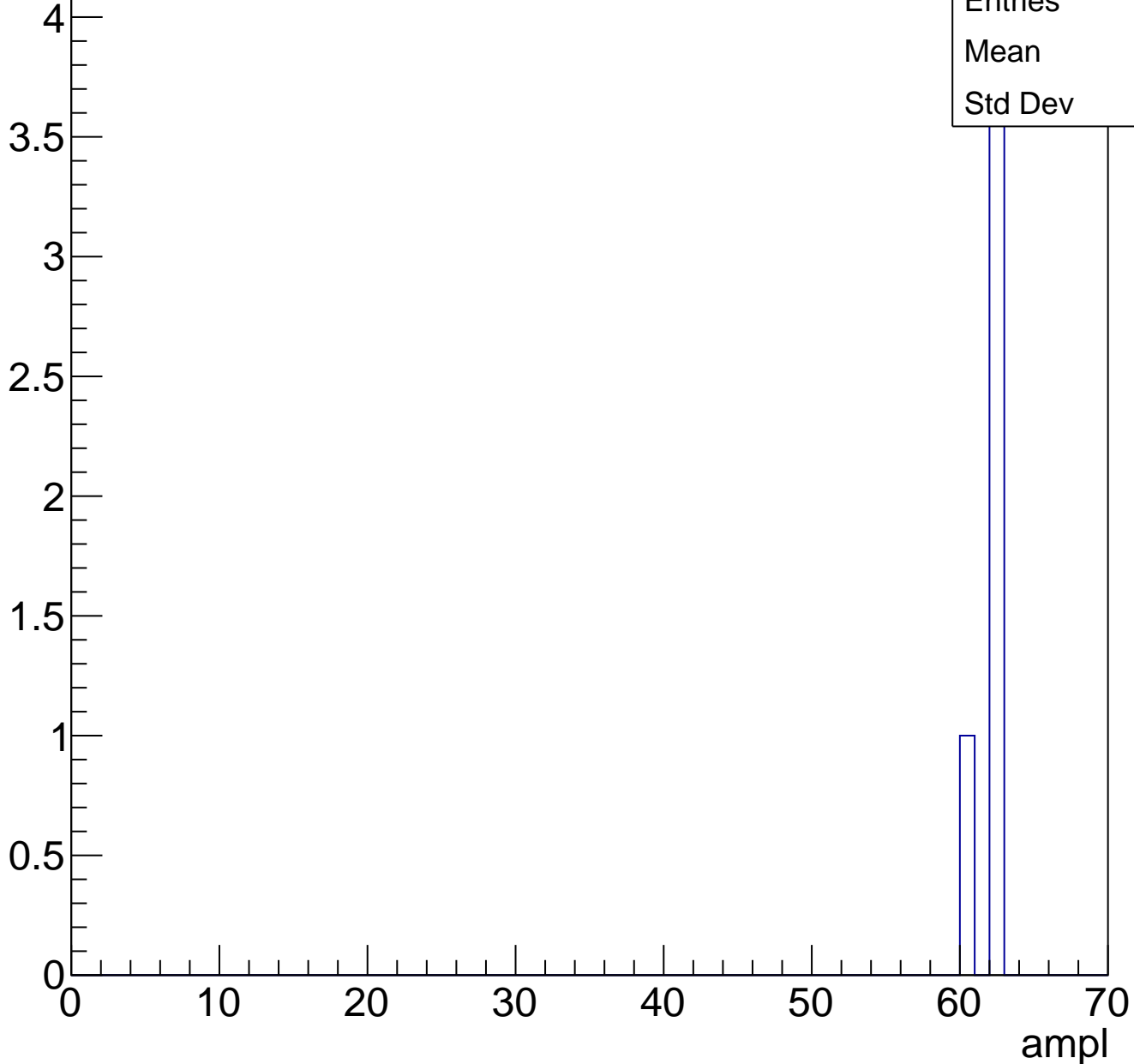
Entries	42
Mean	58.81
Std Dev	9.472



# B1L103S, U11-ch70, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U11-ch70, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U11-ch71, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	81
Mean	31.37
Std Dev	3.666

**Gaus mean : 31.5519**

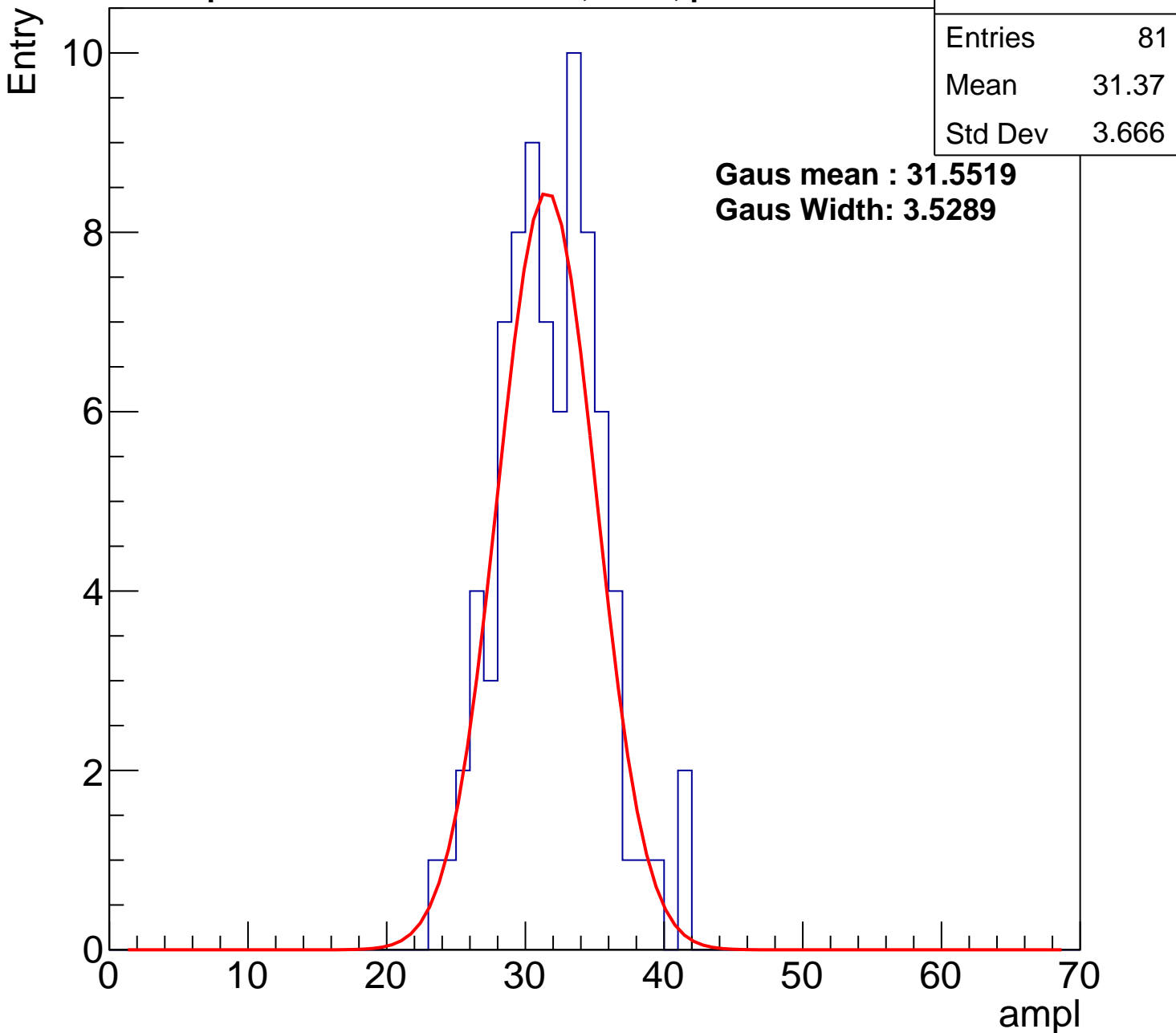
**Gaus Width: 3.5289**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U11-ch71, adc1

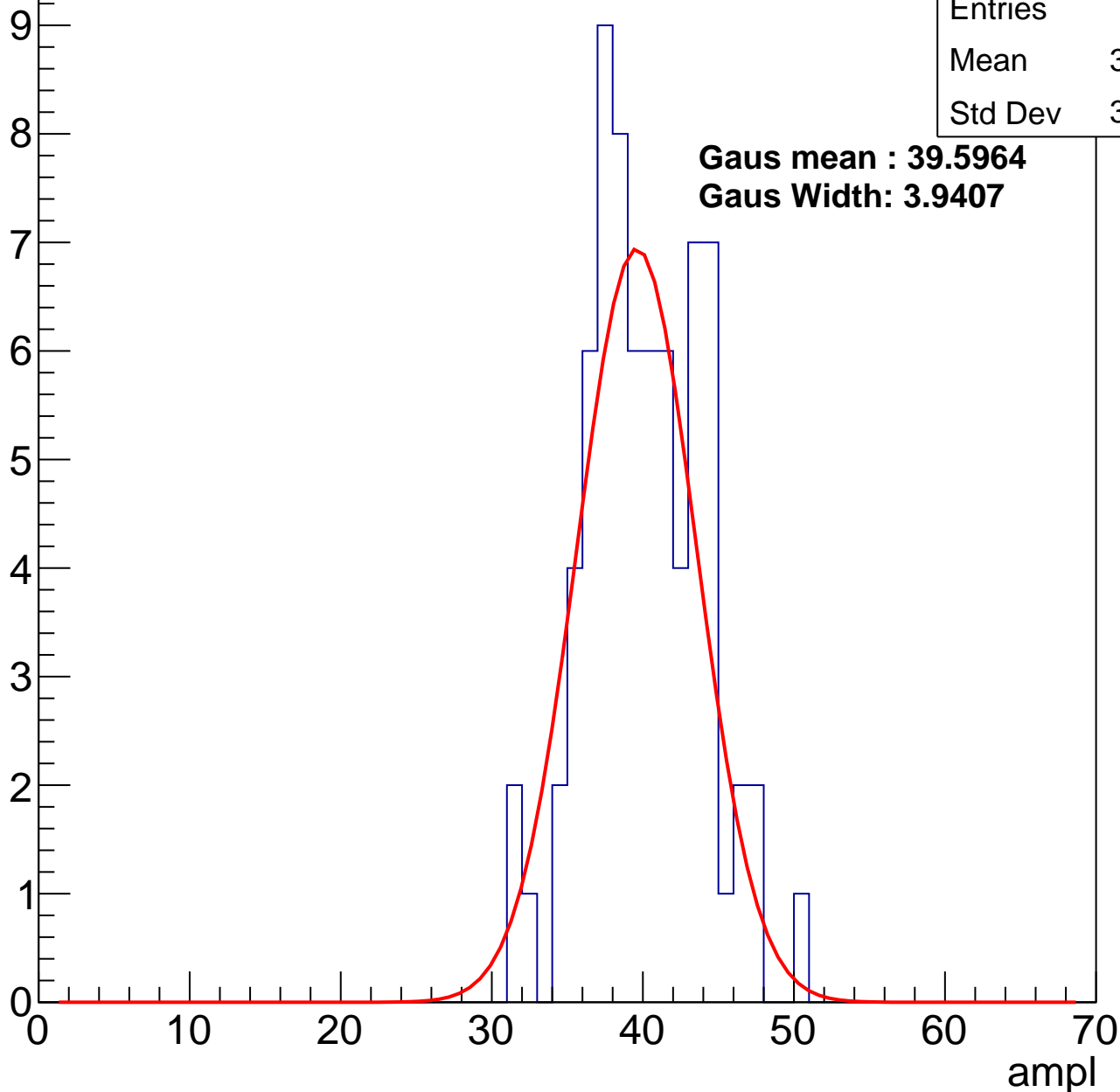
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	74
Mean	39.64
Std Dev	3.847

**Gaus mean : 39.5964**

**Gaus Width: 3.9407**



# B1L103S, U11-ch71, adc2

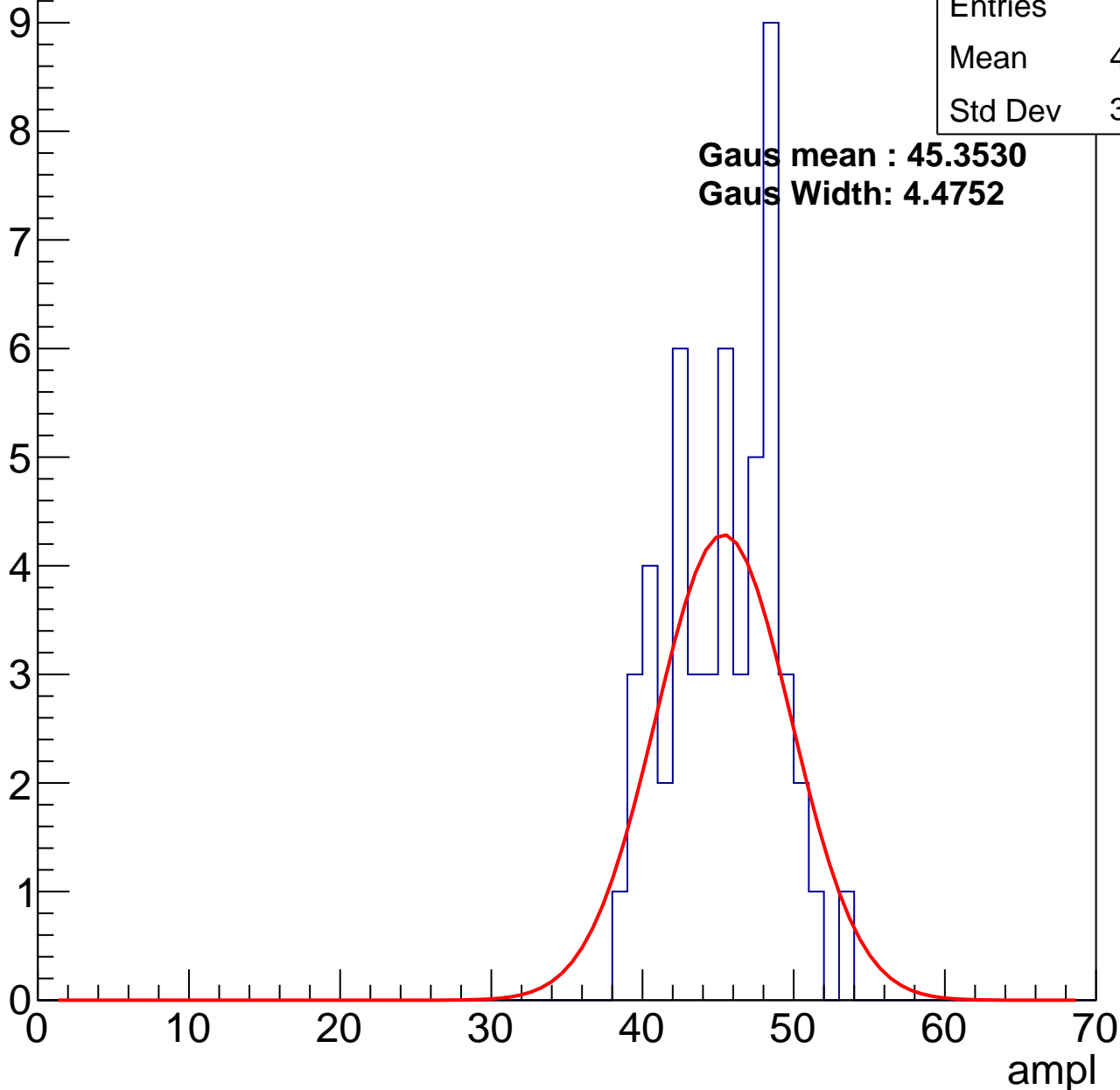
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	52
Mean	44.92
Std Dev	3.562

**Gaus mean : 45.3530**

**Gaus Width: 4.4752**



# B1L103S, U11-ch71, adc3

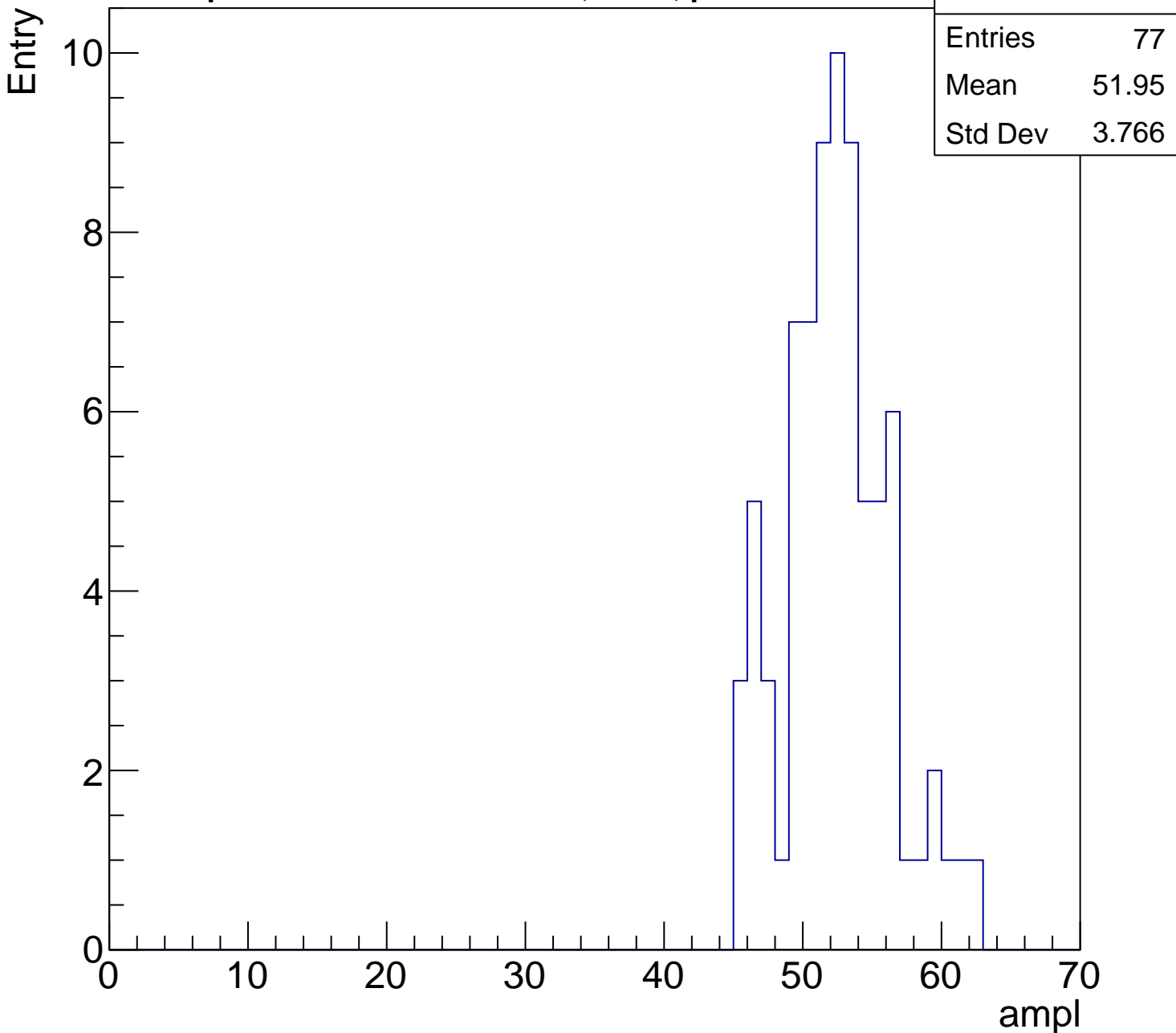
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	77
Mean	51.95
Std Dev	3.766

Entry

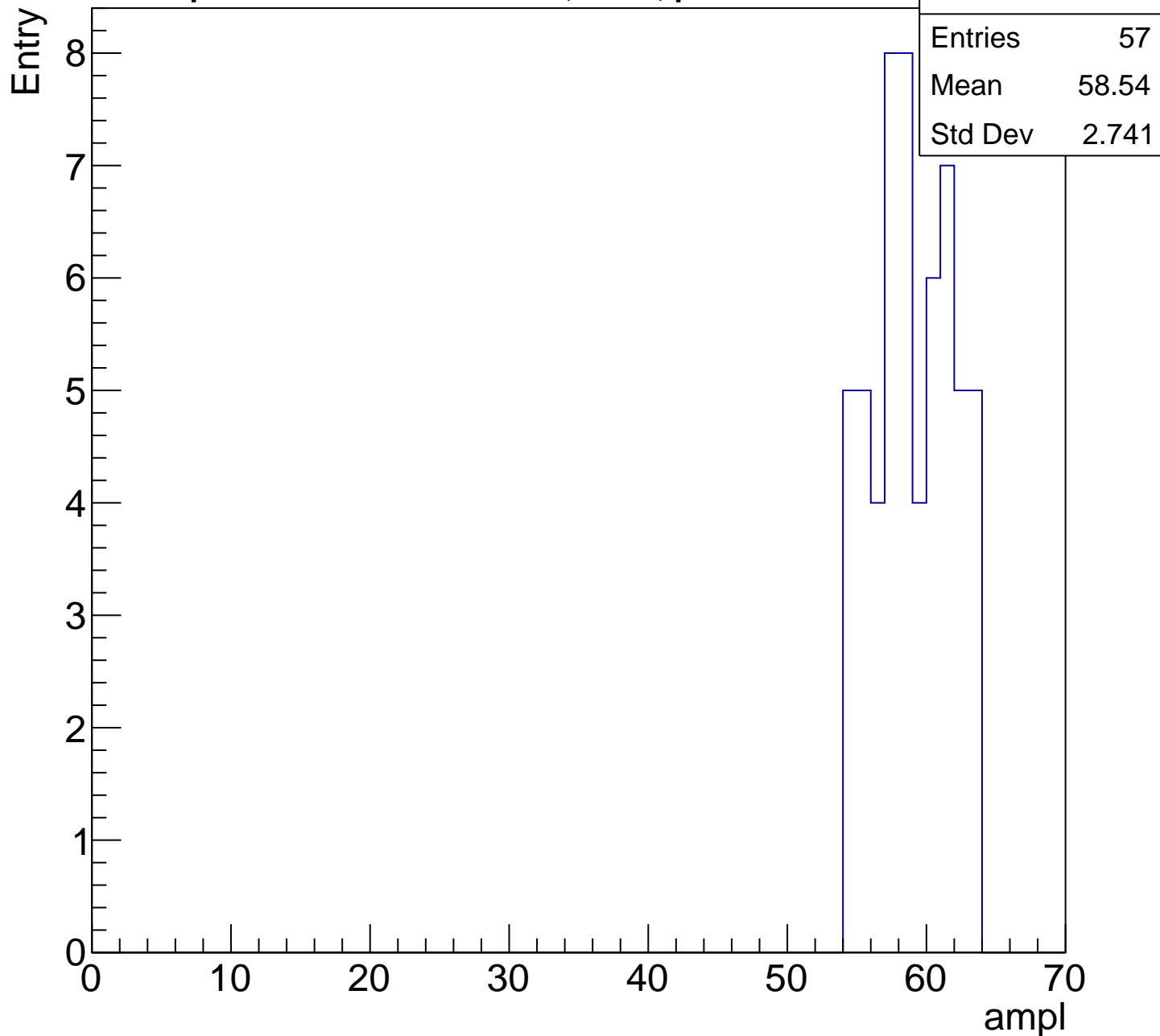
10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70  
ampl



# B1L103S, U11-ch71, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

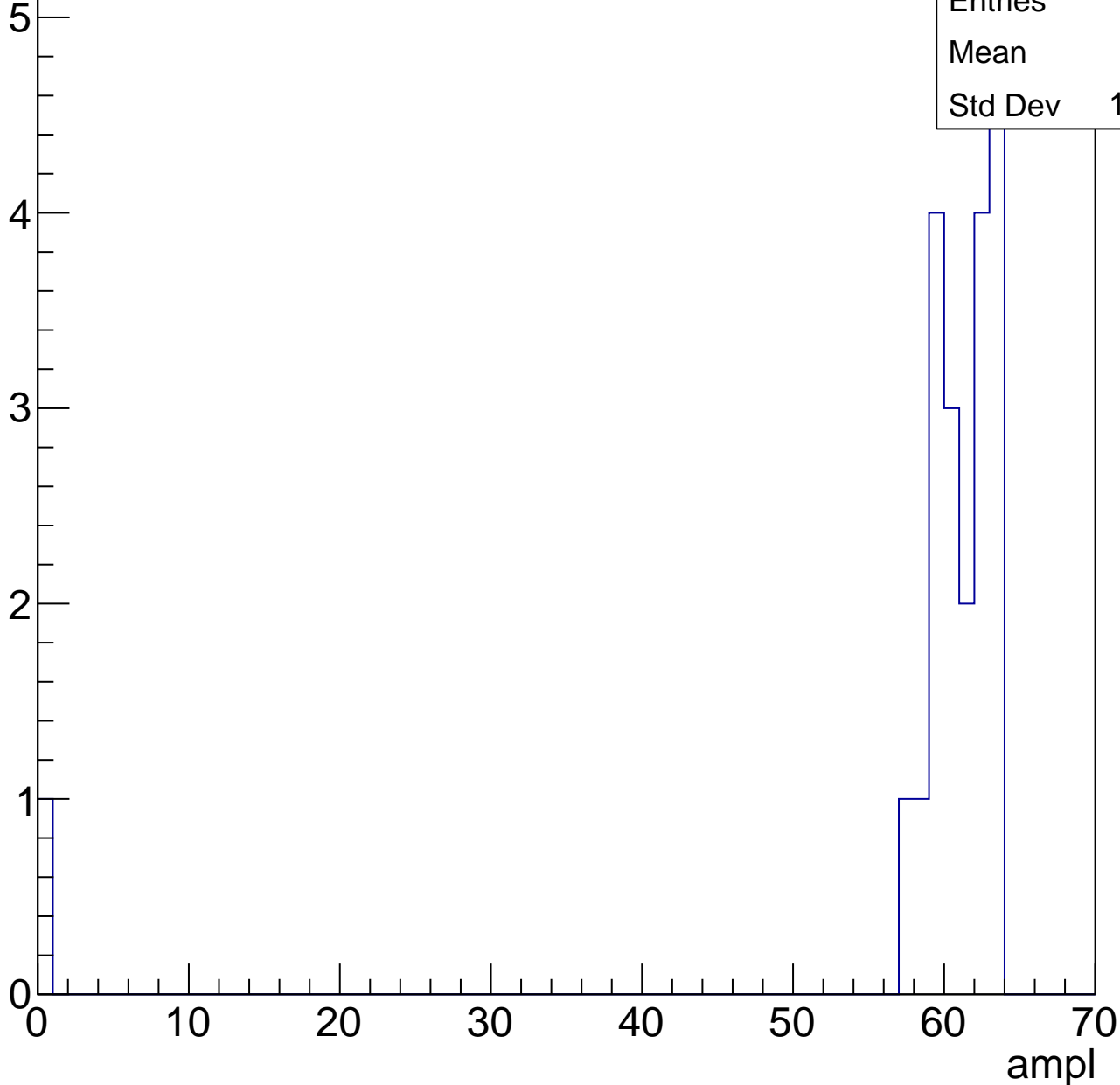


# B1L103S, U11-ch71, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	21
Mean	57.9
Std Dev	13.07



# B1L103S, U11-ch71, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0



# B1L103S, U11-ch71, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U11-ch72, adc0

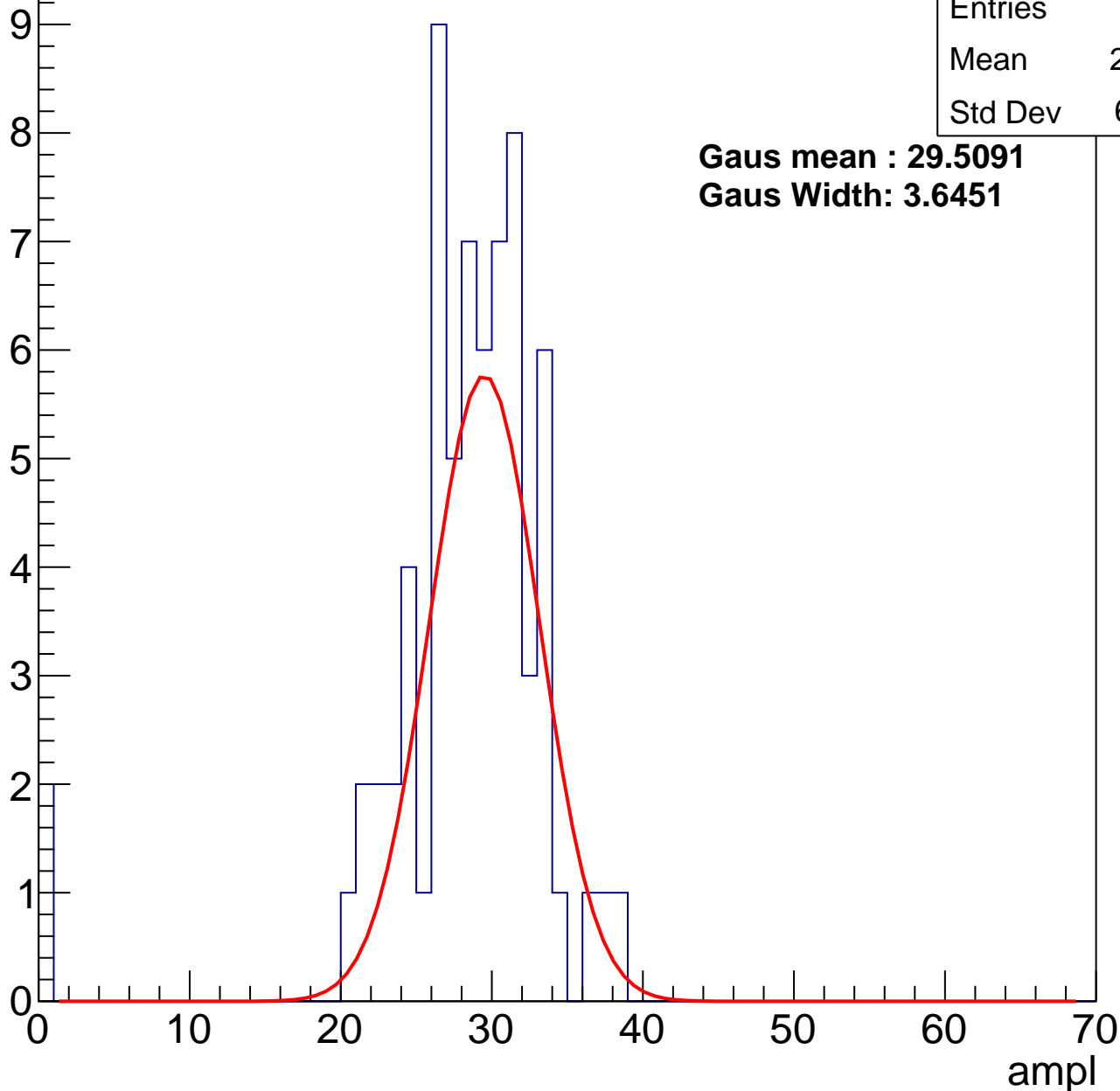
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	69
Mean	27.67
Std Dev	6.071

**Gaus mean : 29.5091**

**Gaus Width: 3.6451**



# B1L103S, U11-ch72, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	79
Mean	35.87
Std Dev	3.661

**Gaus mean : 36.3685**

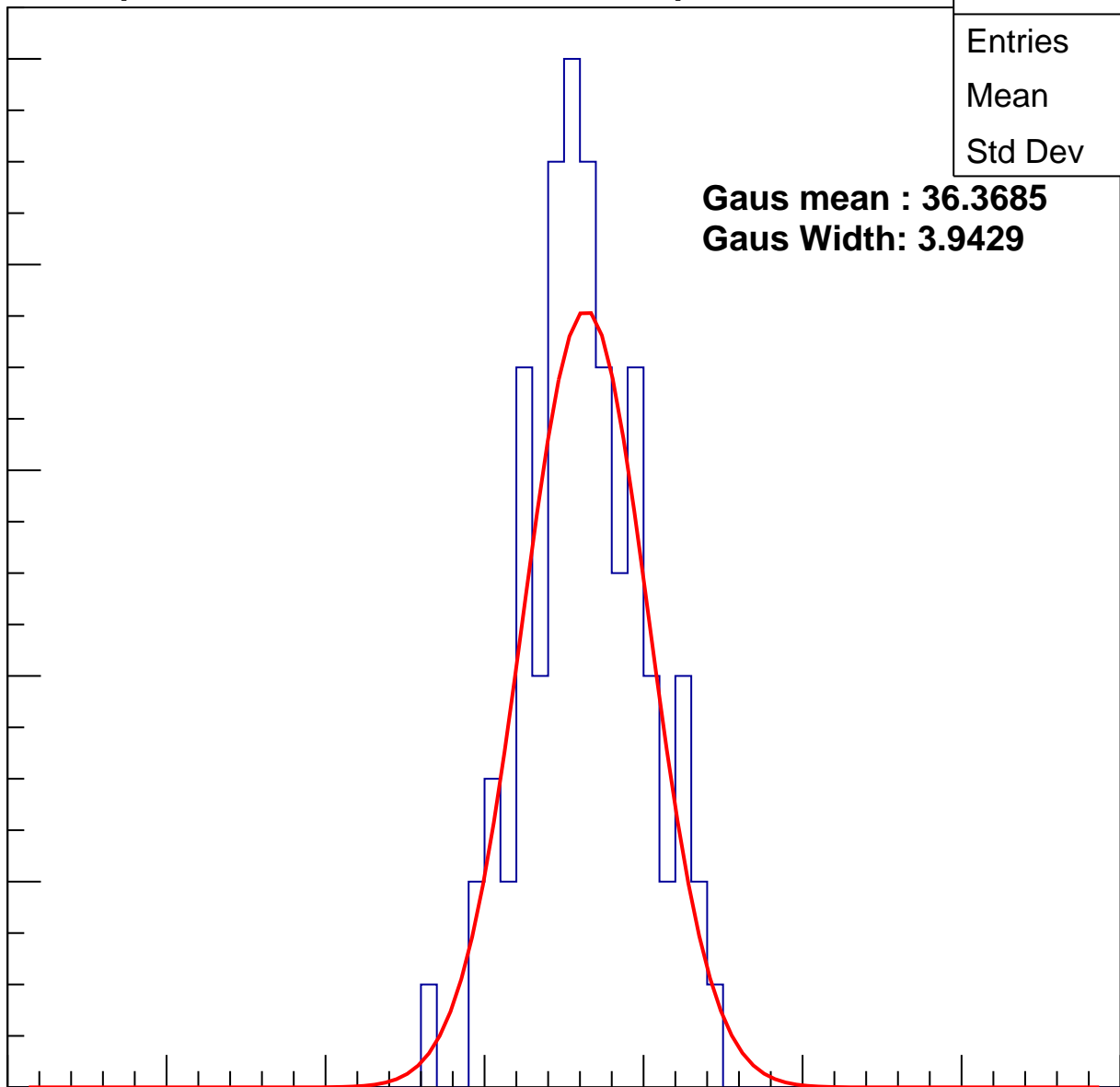
**Gaus Width: 3.9429**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B1L103S, U11-ch72, adc2

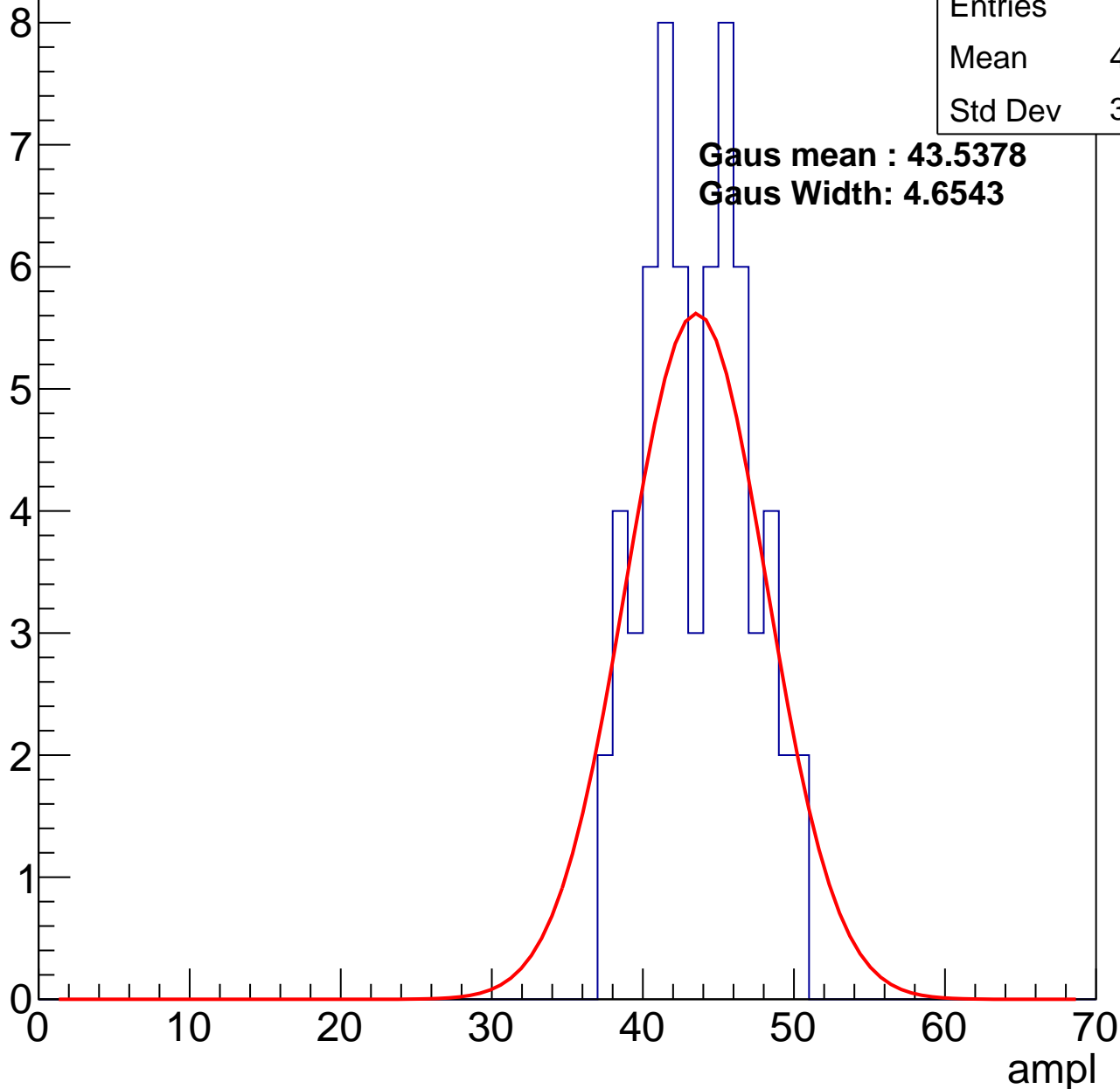
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	43.22
Std Dev	3.378

**Gaus mean : 43.5378**

**Gaus Width: 4.6543**

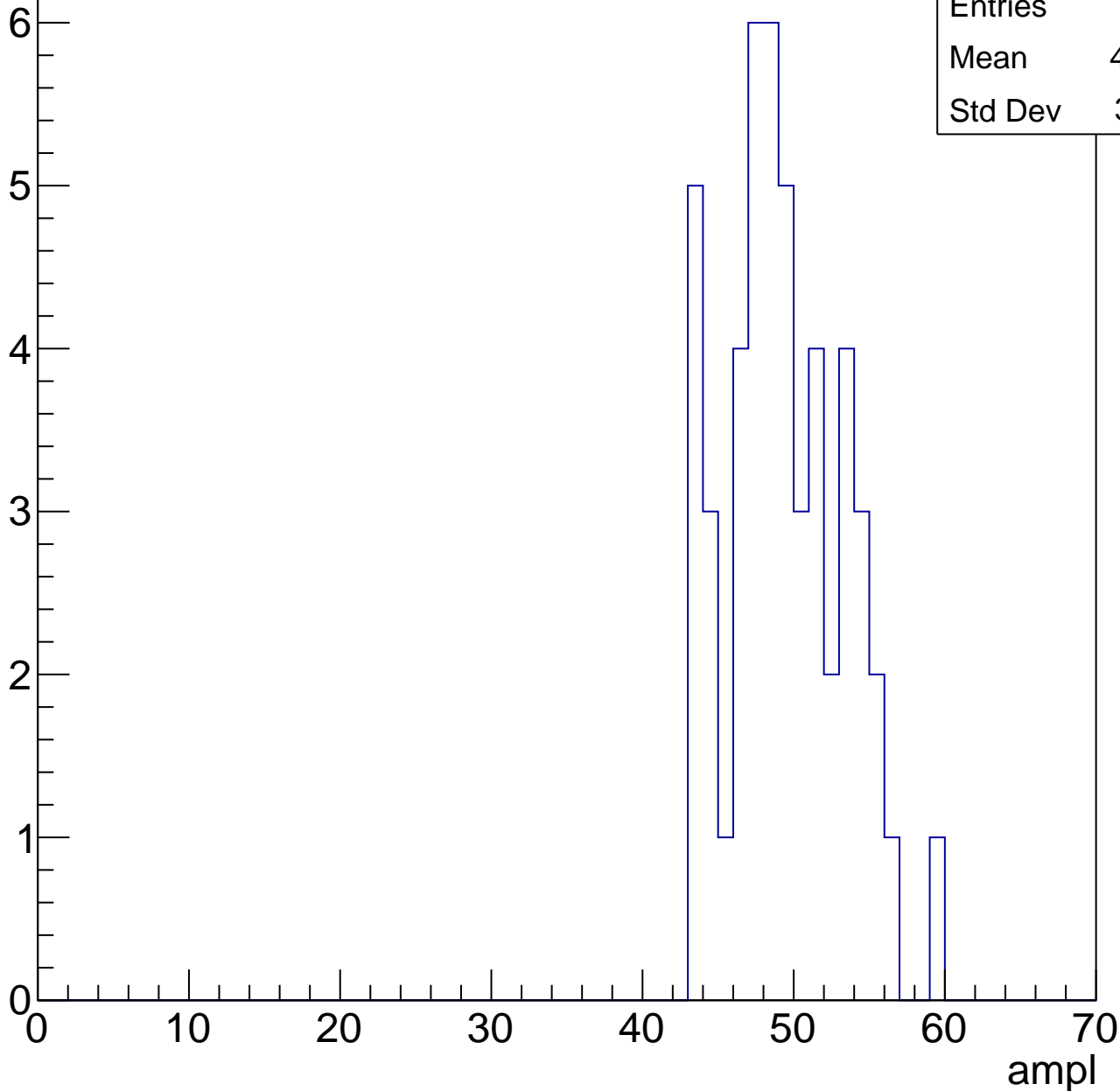


# B1L103S, U11-ch72, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	50
Mean	48.96
Std Dev	3.831

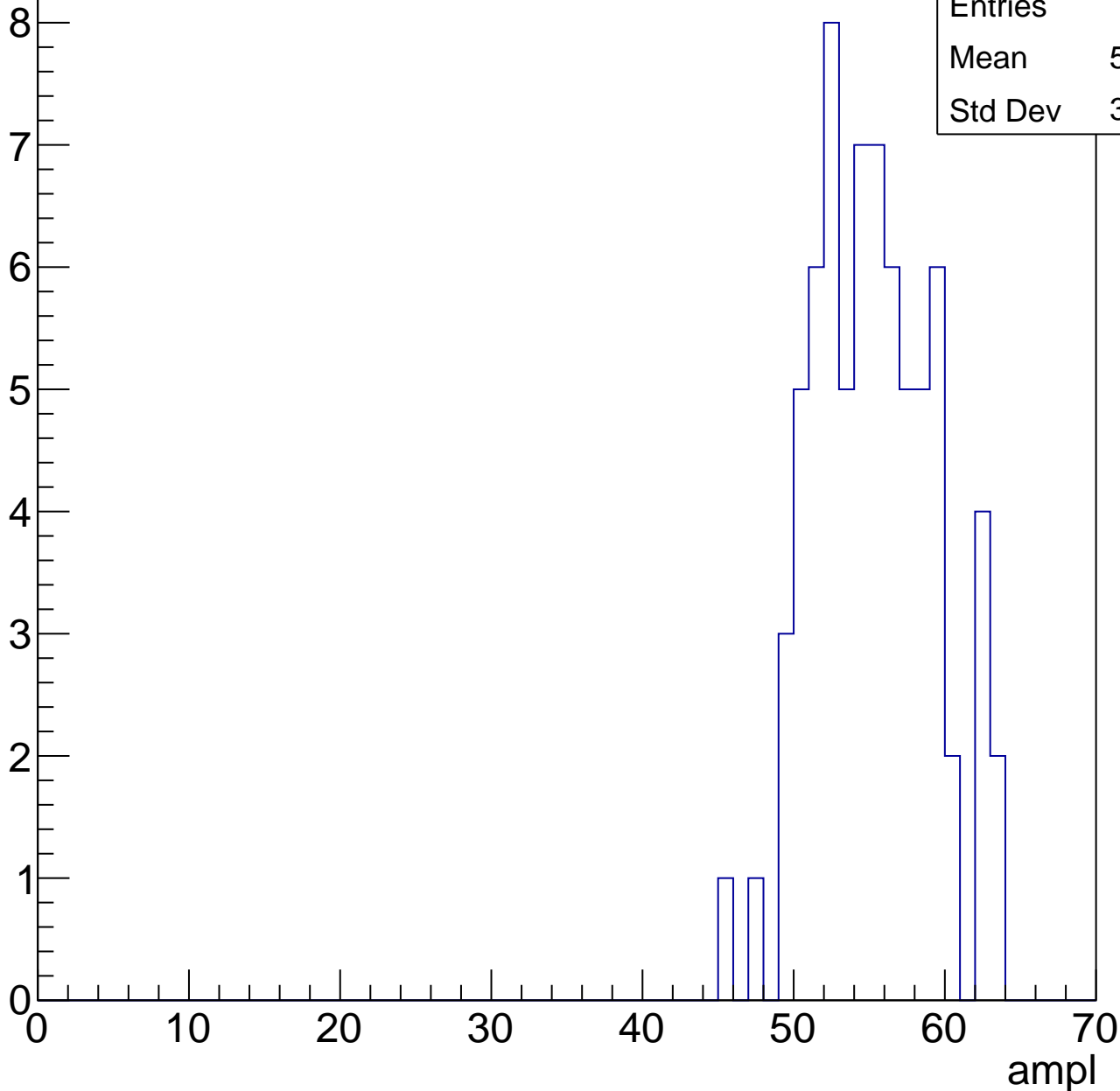


# B1L103S, U11-ch72, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	73
Mean	54.77
Std Dev	3.933

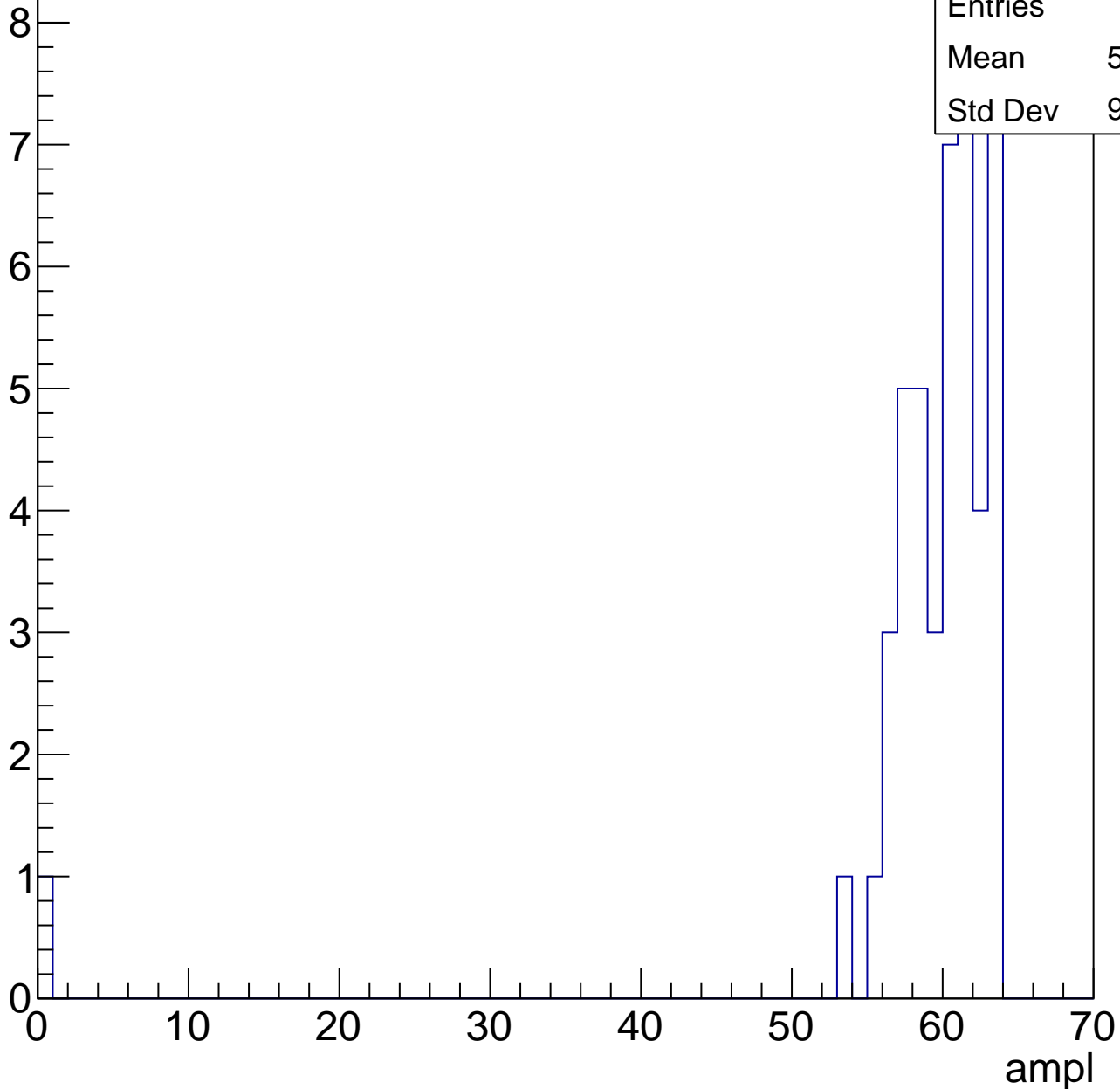


# B1L103S, U11-ch72, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	46
Mean	58.43
Std Dev	9.057



# B1L103S, U11-ch72, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	5
Mean	61.2
Std Dev	0.7483

ampl

0 10 20 30 40 50 60 70



# B1L103S, U11-ch72, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U11-ch73, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	87
Mean	30.1
Std Dev	4.883

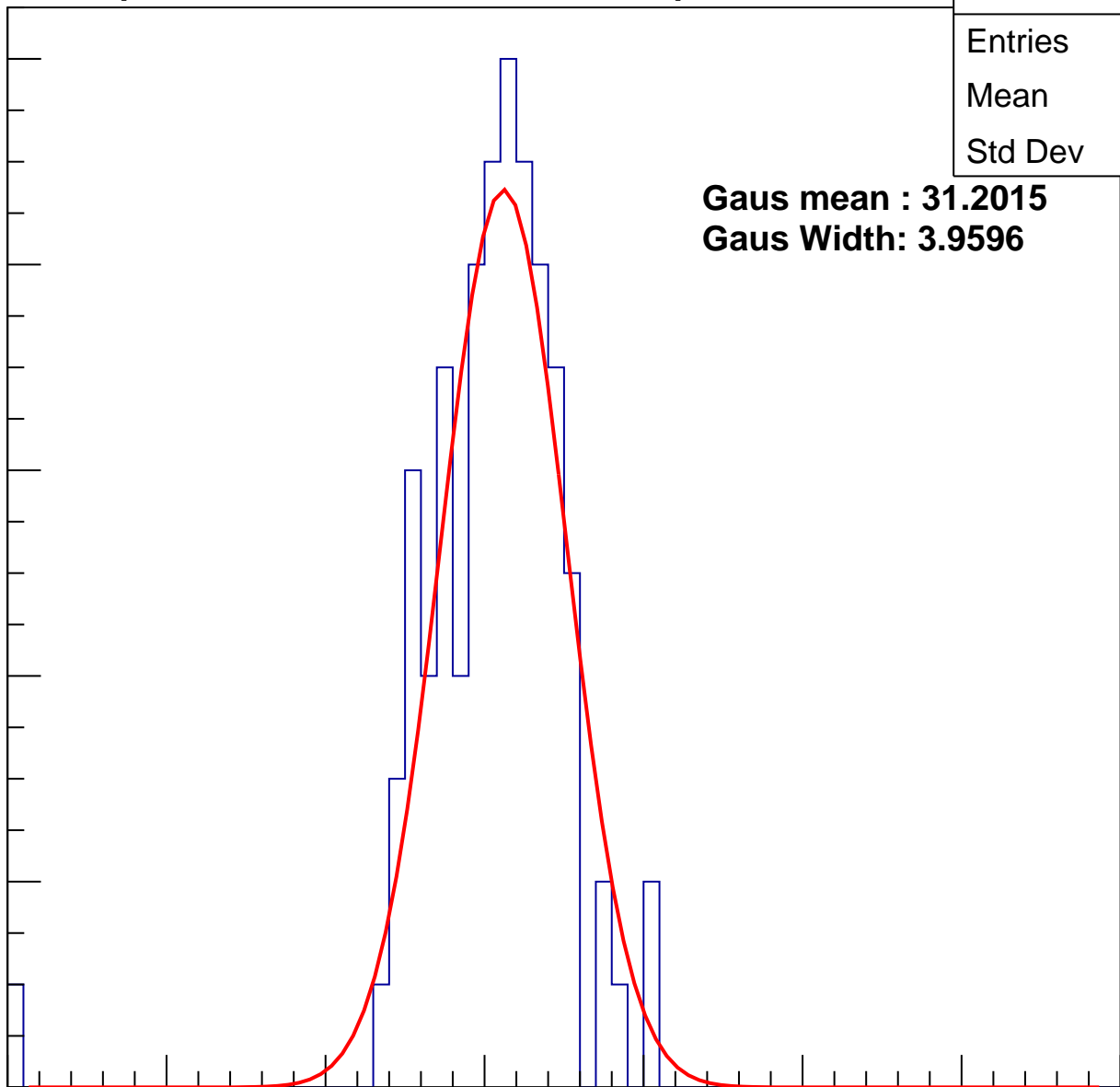
**Gaus mean : 31.2015**  
**Gaus Width: 3.9596**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U11-ch73, adc1

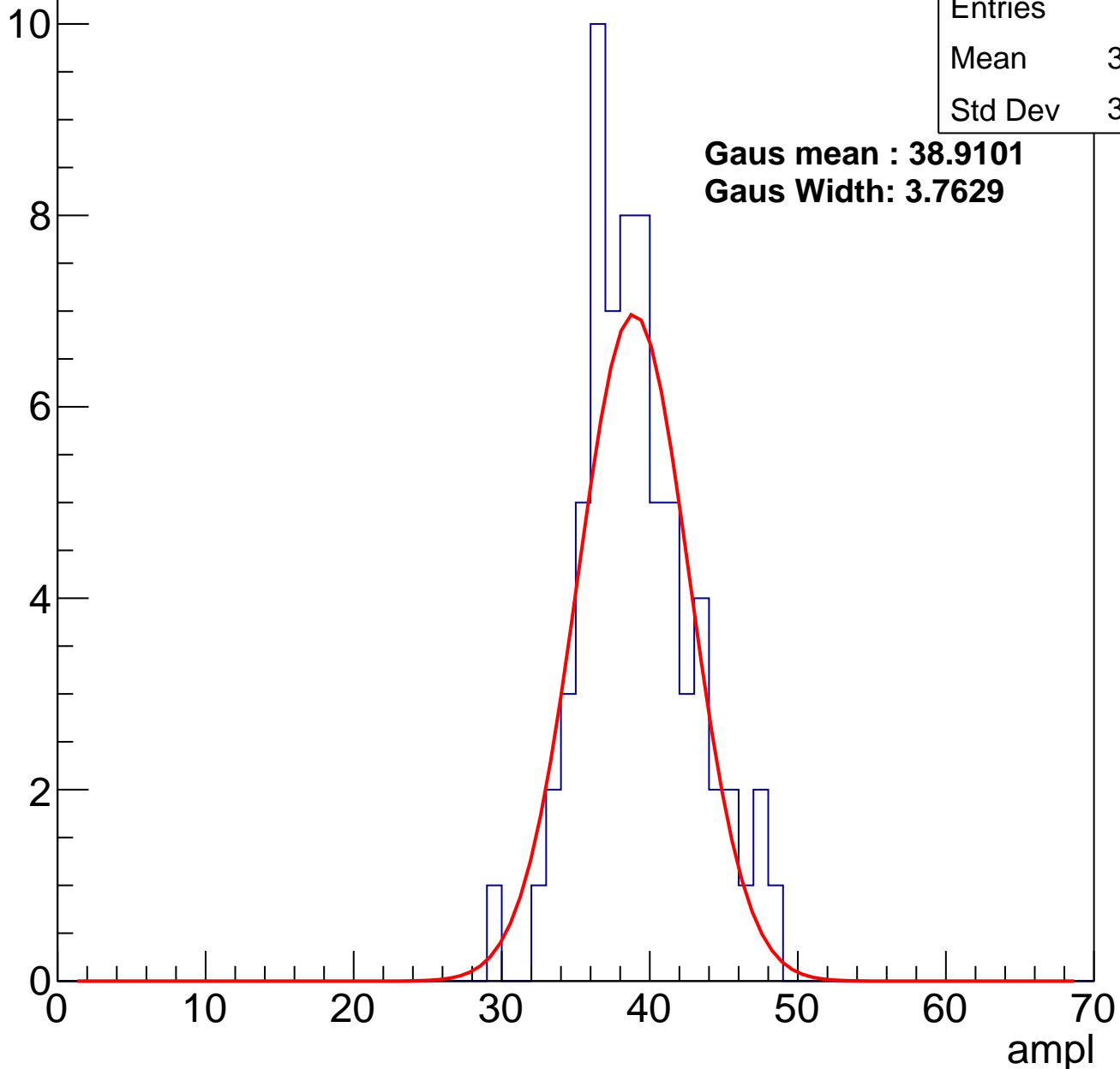
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	70
Mean	38.69
Std Dev	3.763

**Gaus mean : 38.9101**

**Gaus Width: 3.7629**

Entry



# B1L103S, U11-ch73, adc2

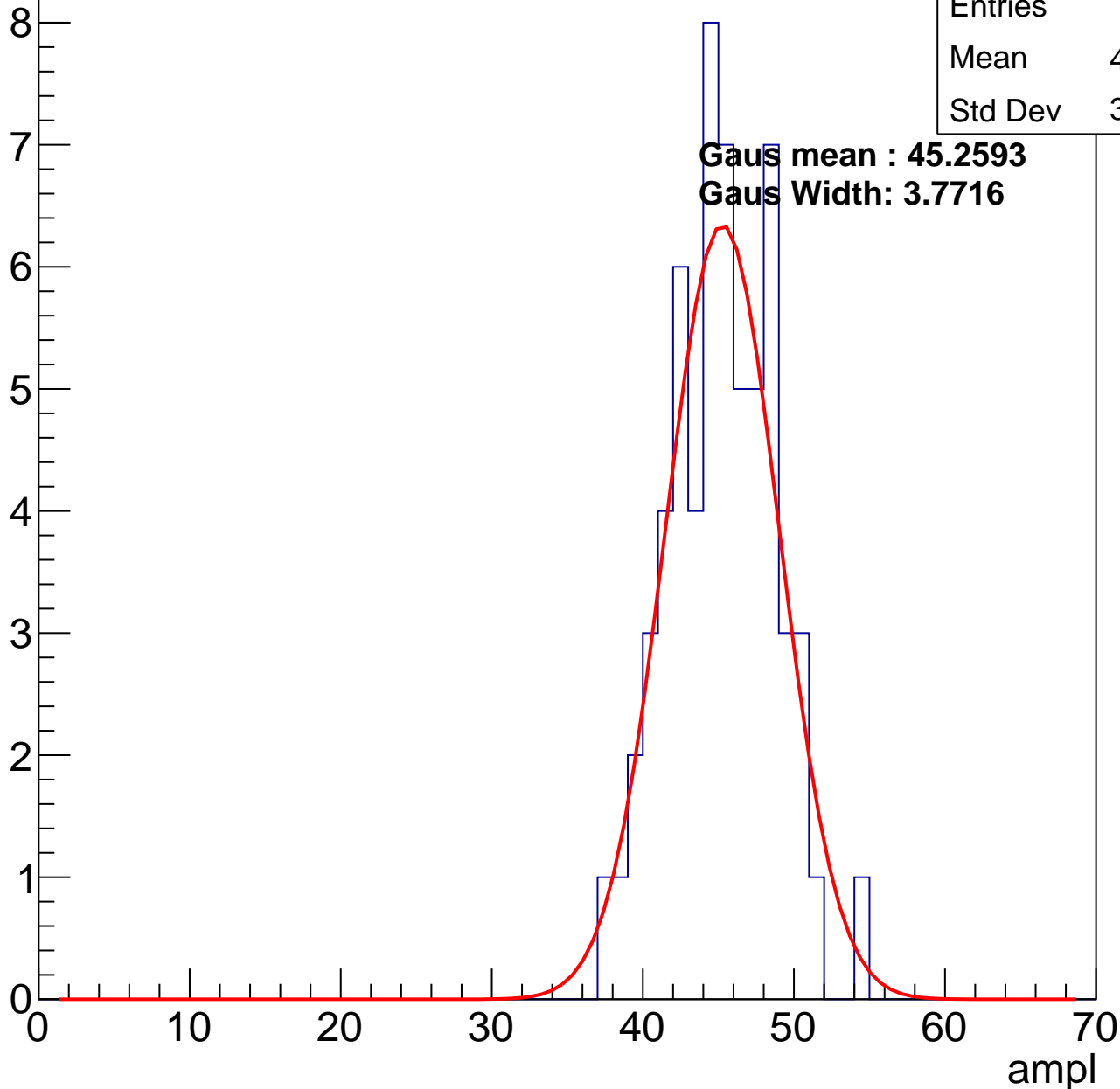
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	61
Mean	44.77
Std Dev	3.452

Gaus mean : 45.2593

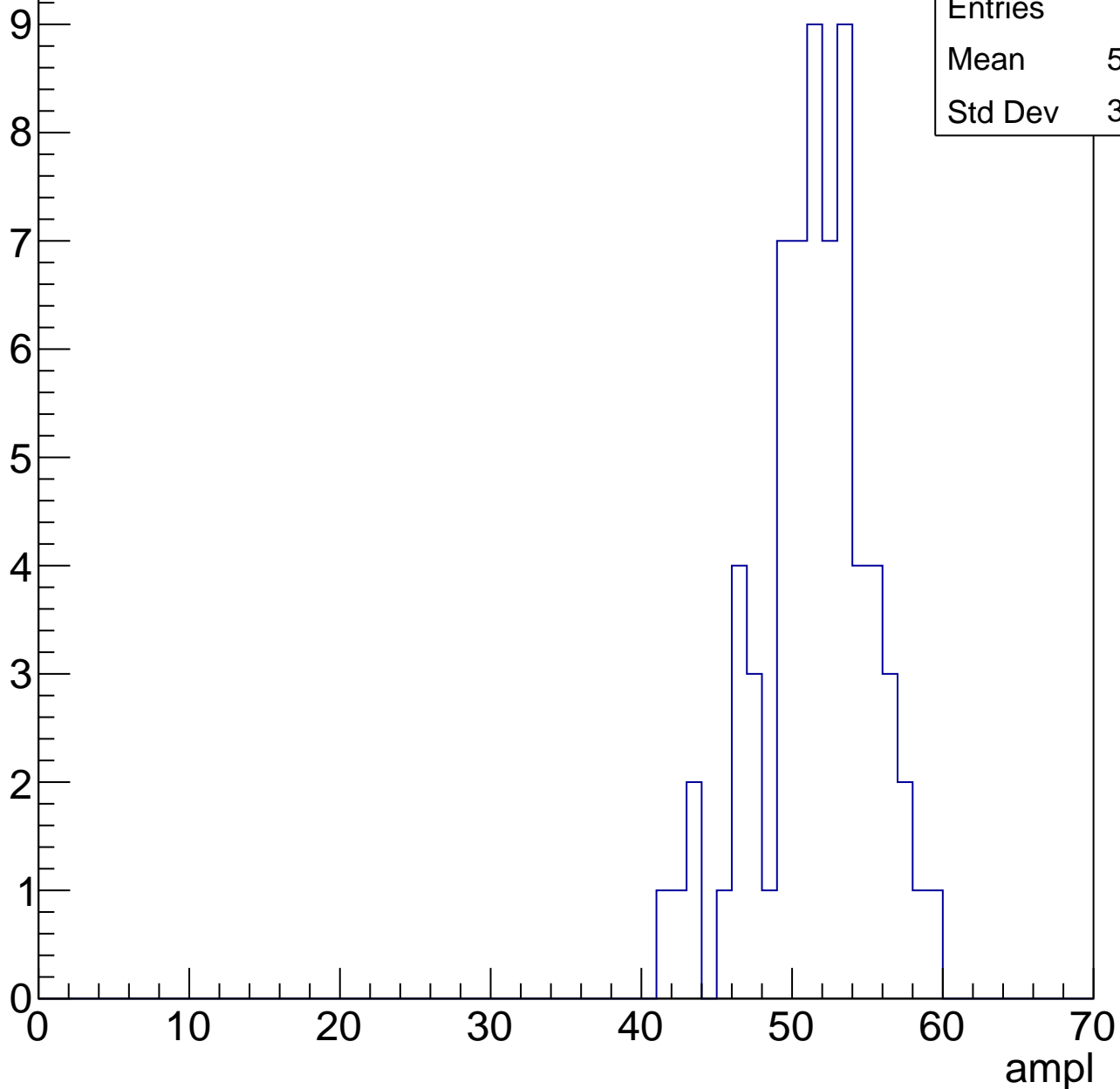
Gaus Width: 3.7716



# B1L103S, U11-ch73, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

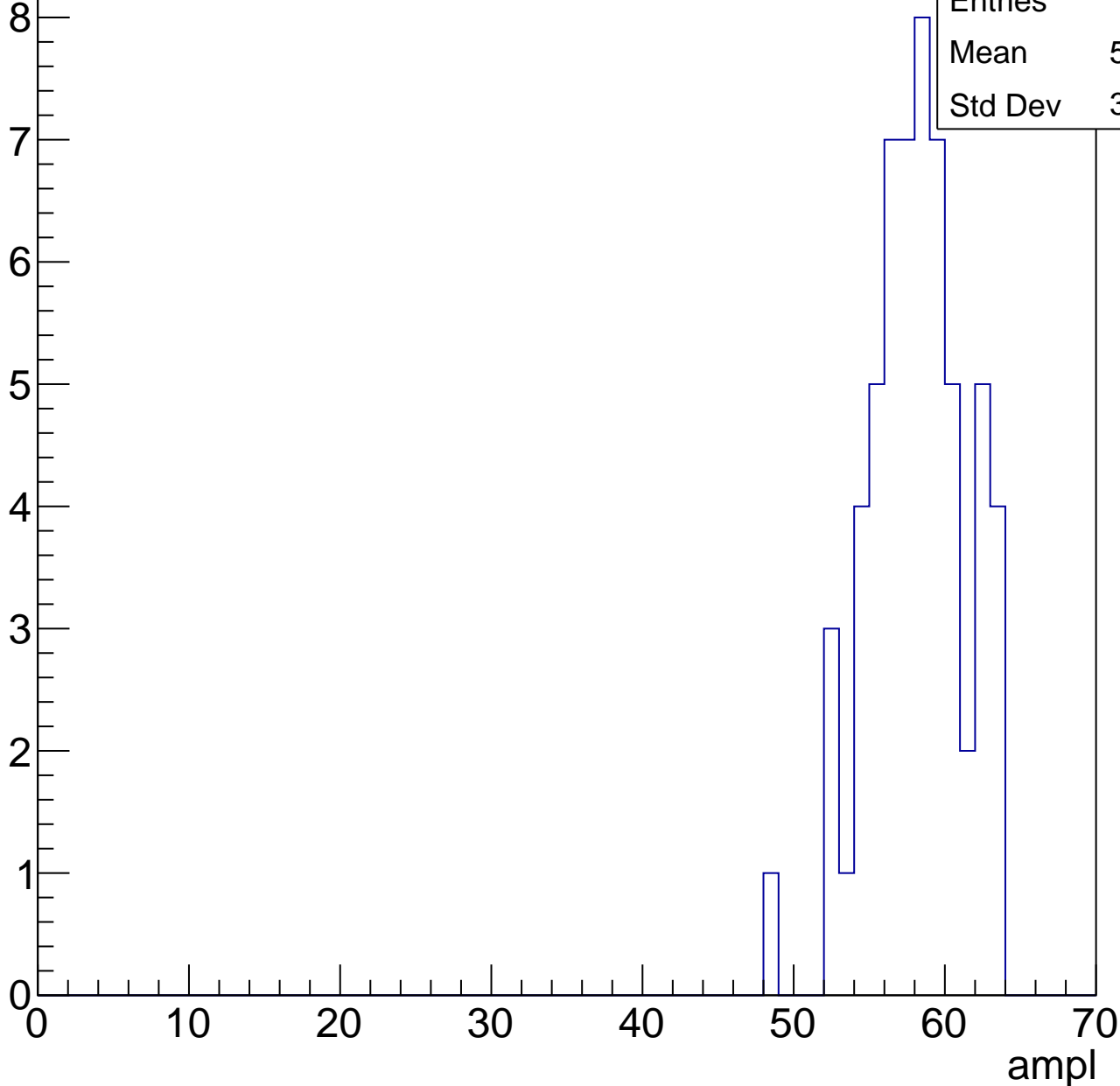


# B1L103S, U11-ch73, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	59
Mean	57.63
Std Dev	3.172

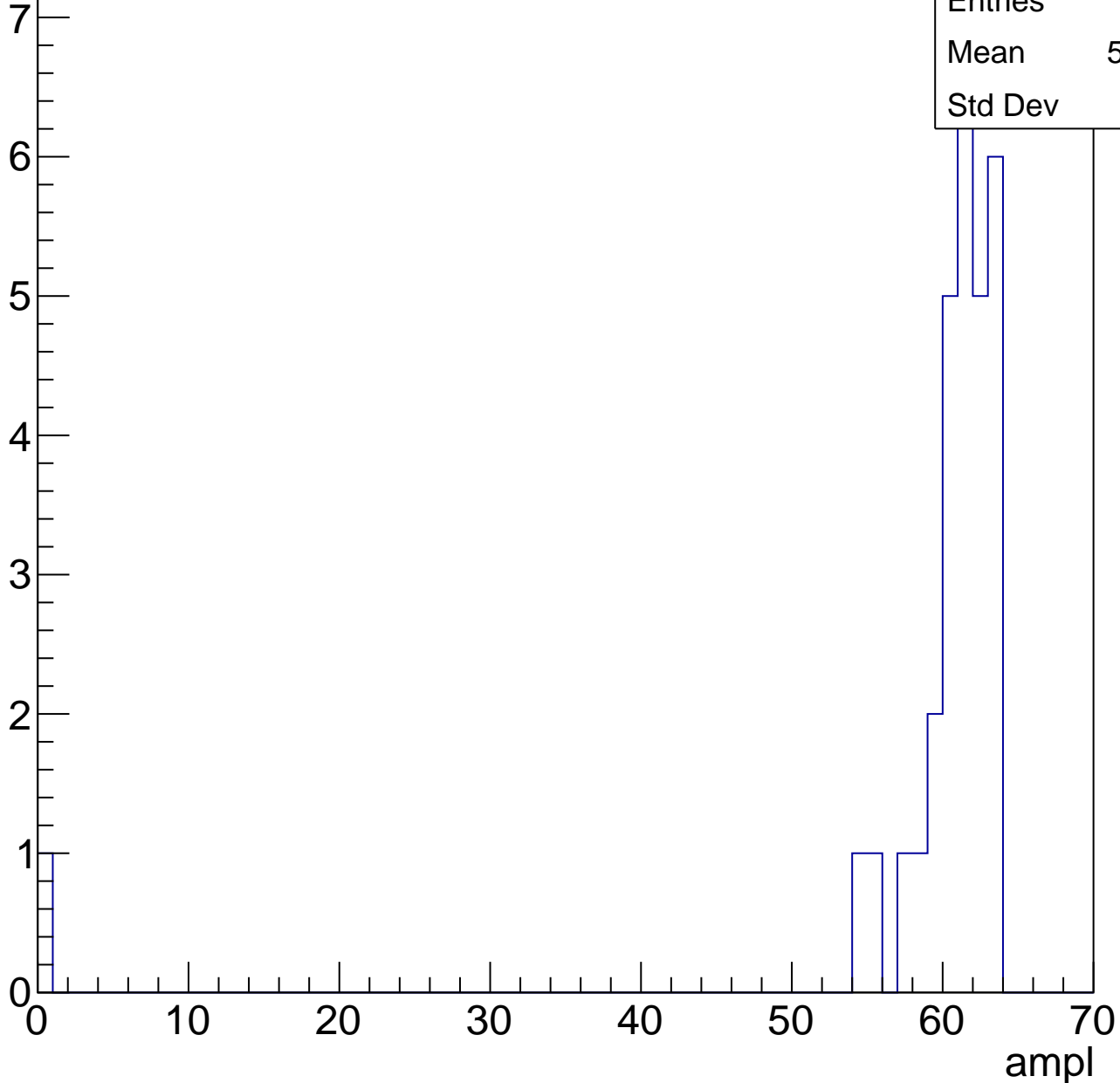


# B1L103S, U11-ch73, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	30
Mean	58.57
Std Dev	11.1



# B1L103S, U11-ch73, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U11-ch73, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U11-ch74, adc0

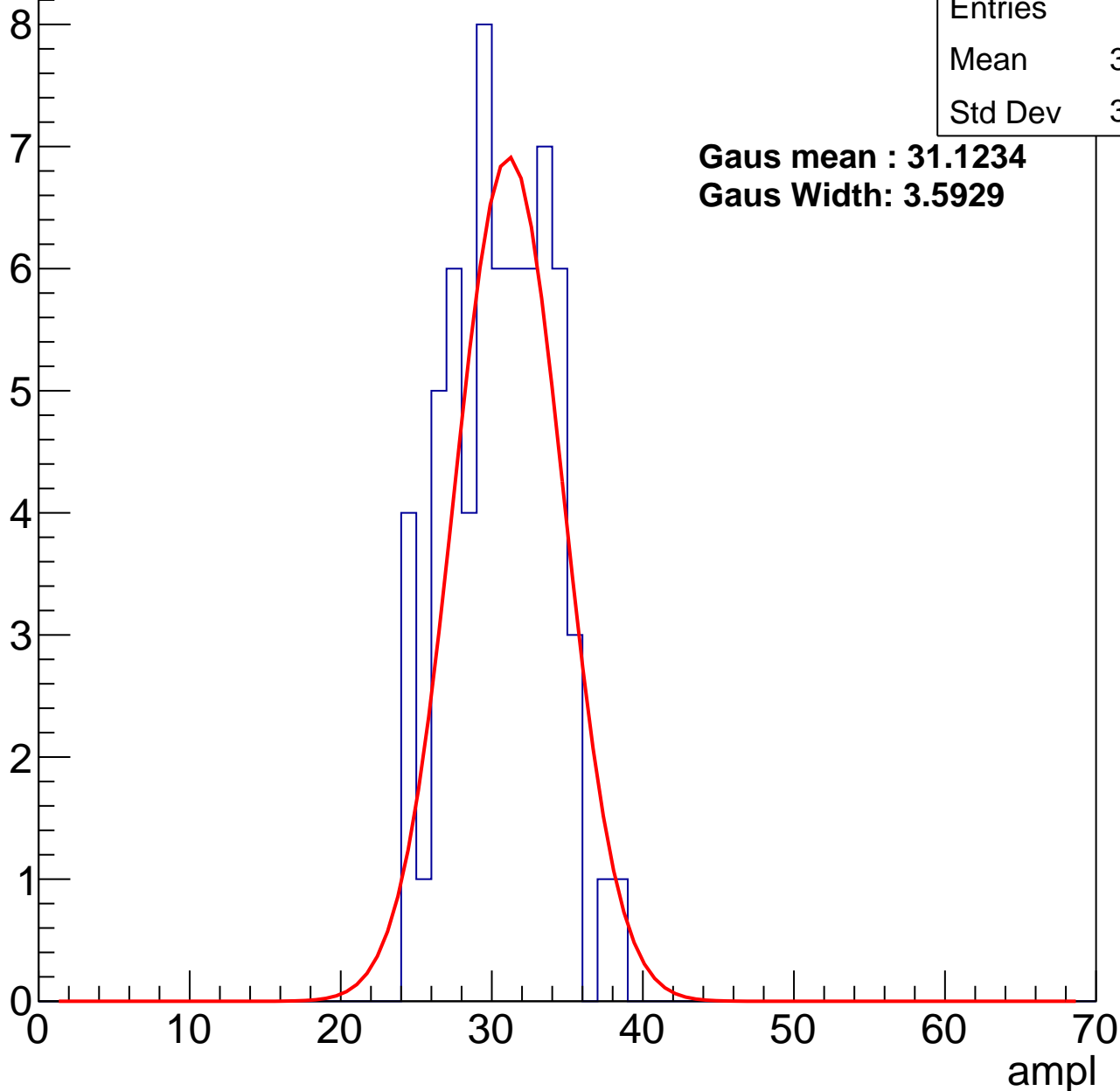
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	30.16
Std Dev	3.313

**Gaus mean : 31.1234**

**Gaus Width: 3.5929**



# B1L103S, U11-ch74, adc1

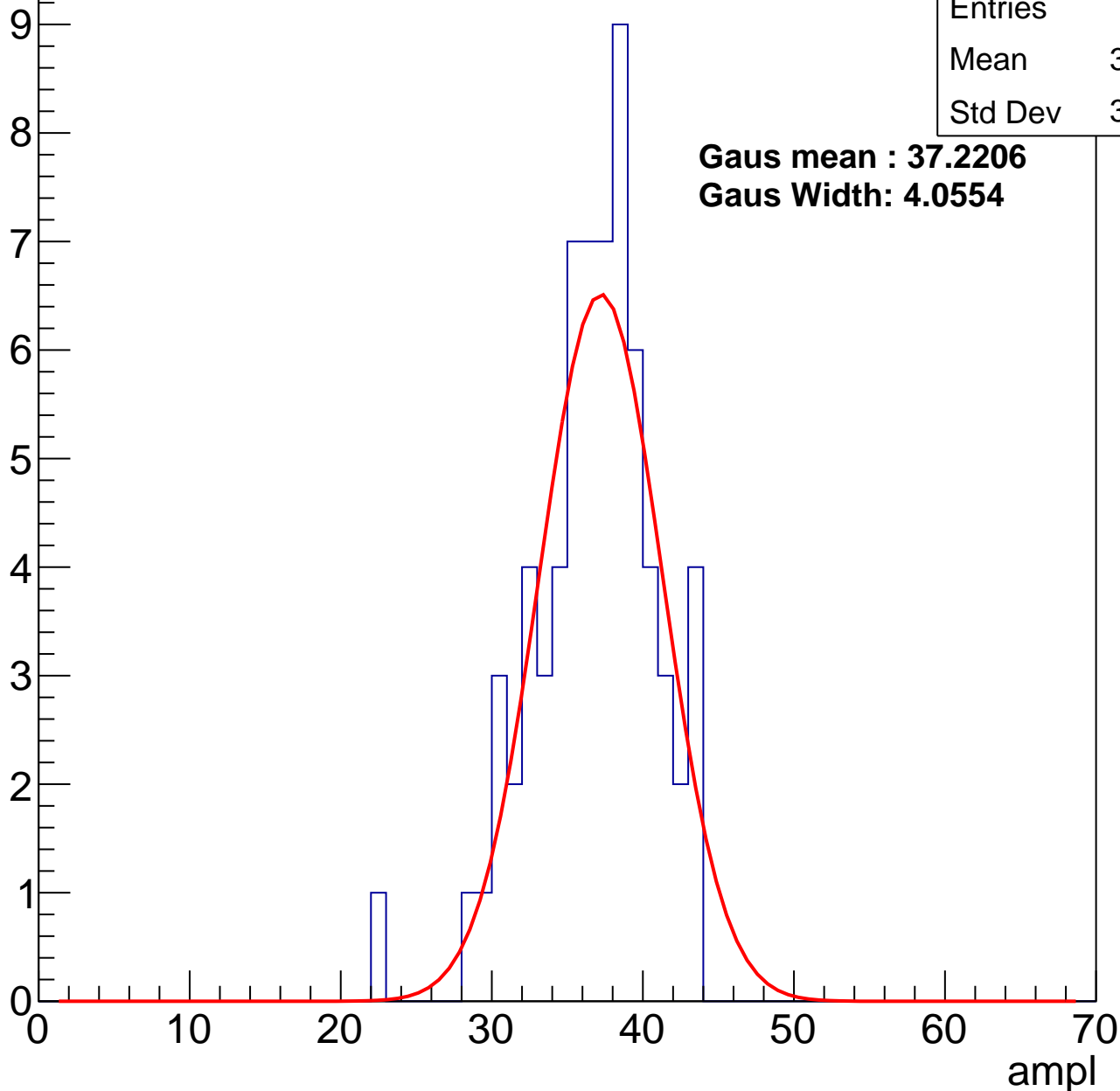
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	68
Mean	36.25
Std Dev	3.987

**Gaus mean : 37.2206**

**Gaus Width: 4.0554**



# B1L103S, U11-ch74, adc2

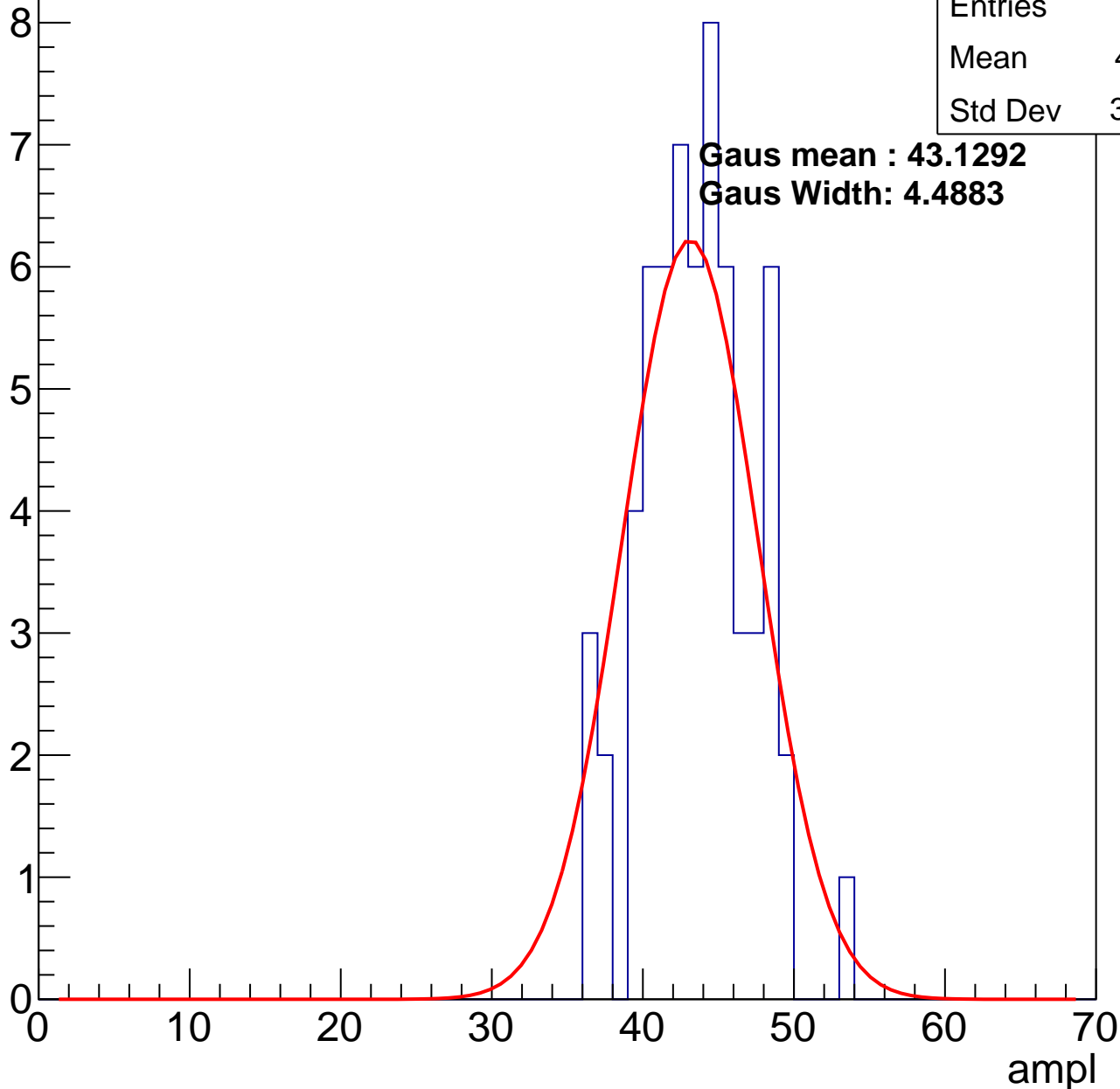
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	43.11
Std Dev	3.555

**Gaus mean : 43.1292**

**Gaus Width: 4.4883**

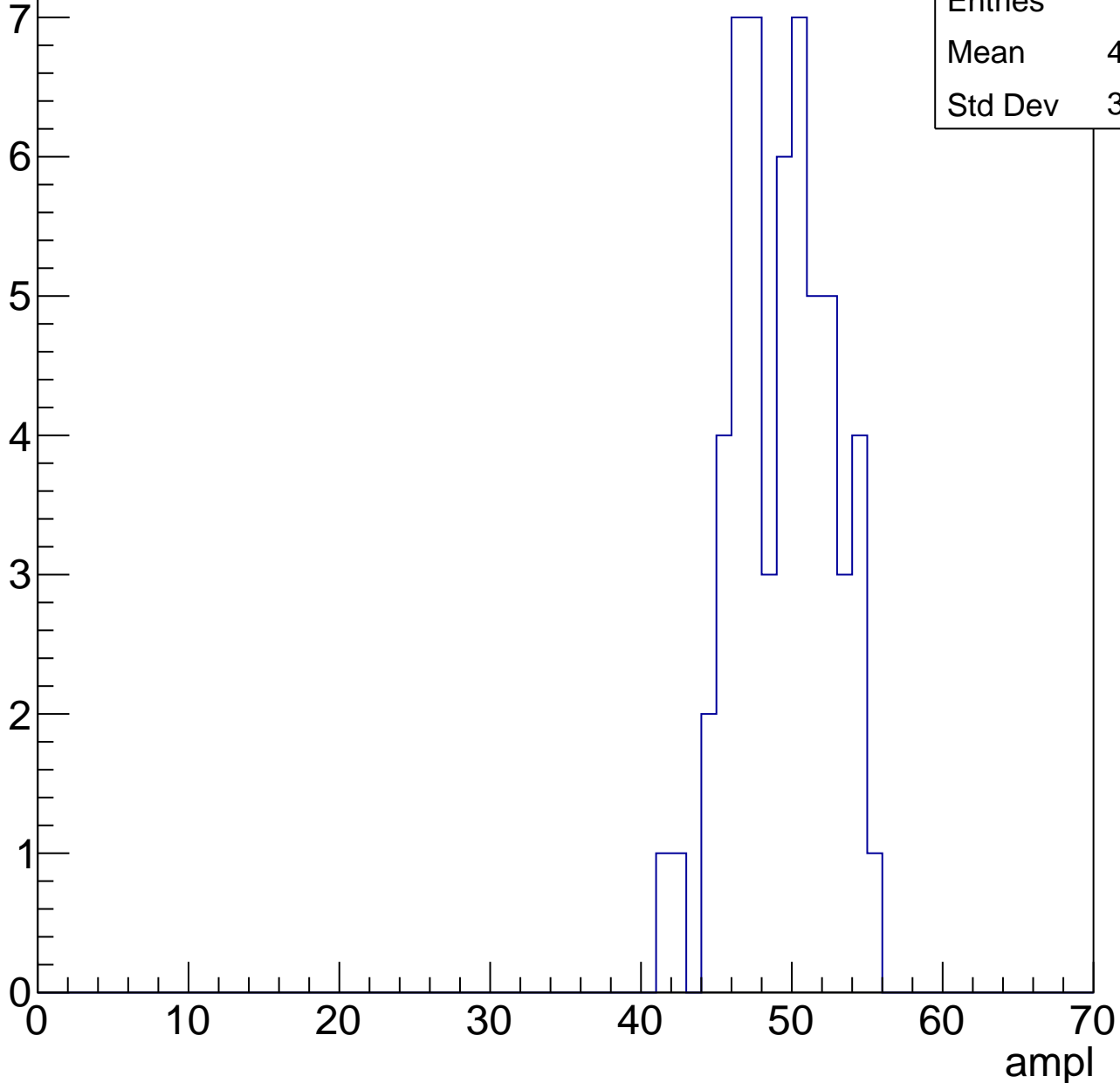


# B1L103S, U11-ch74, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

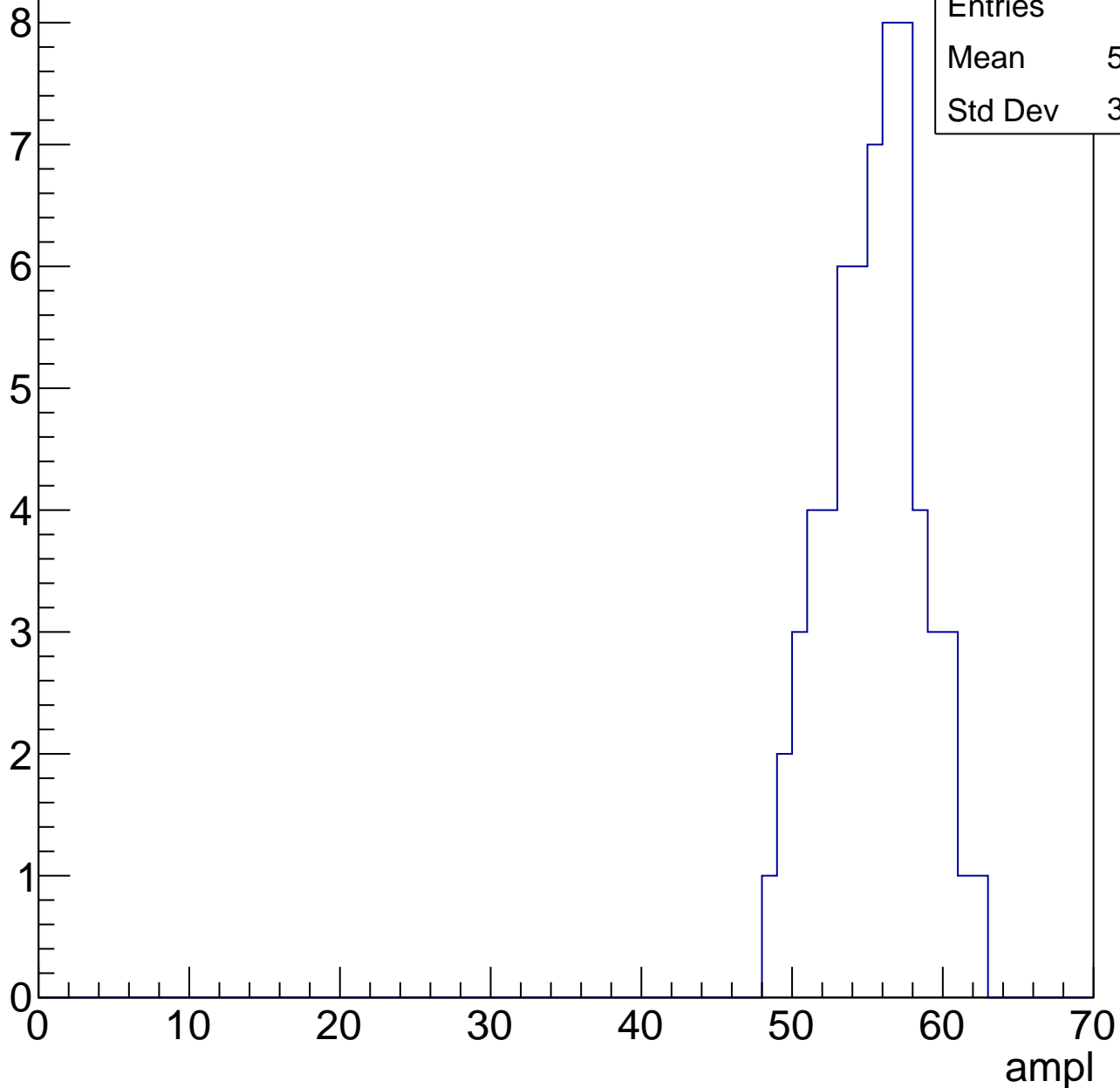
Entries	56
Mean	48.84
Std Dev	3.206



# B1L103S, U11-ch74, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



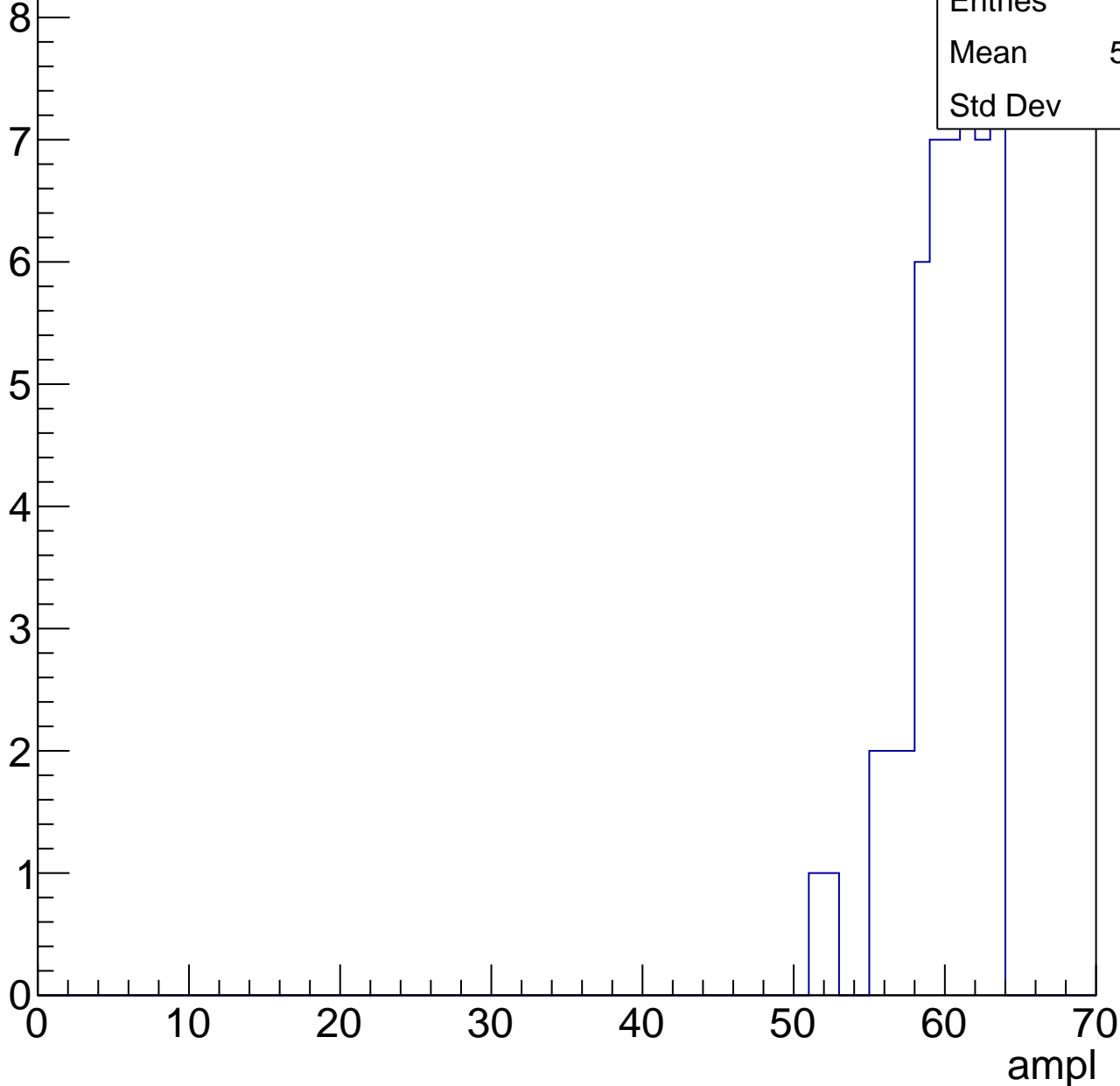
Entries	61
Mean	54.93
Std Dev	3.162

# B1L103S, U11-ch74, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	51
Mean	59.73
Std Dev	2.73



# B1L103S, U11-ch74, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	6
Mean	51.83
Std Dev	23.19



# B1L103S, U11-ch74, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U11-ch75, adc0

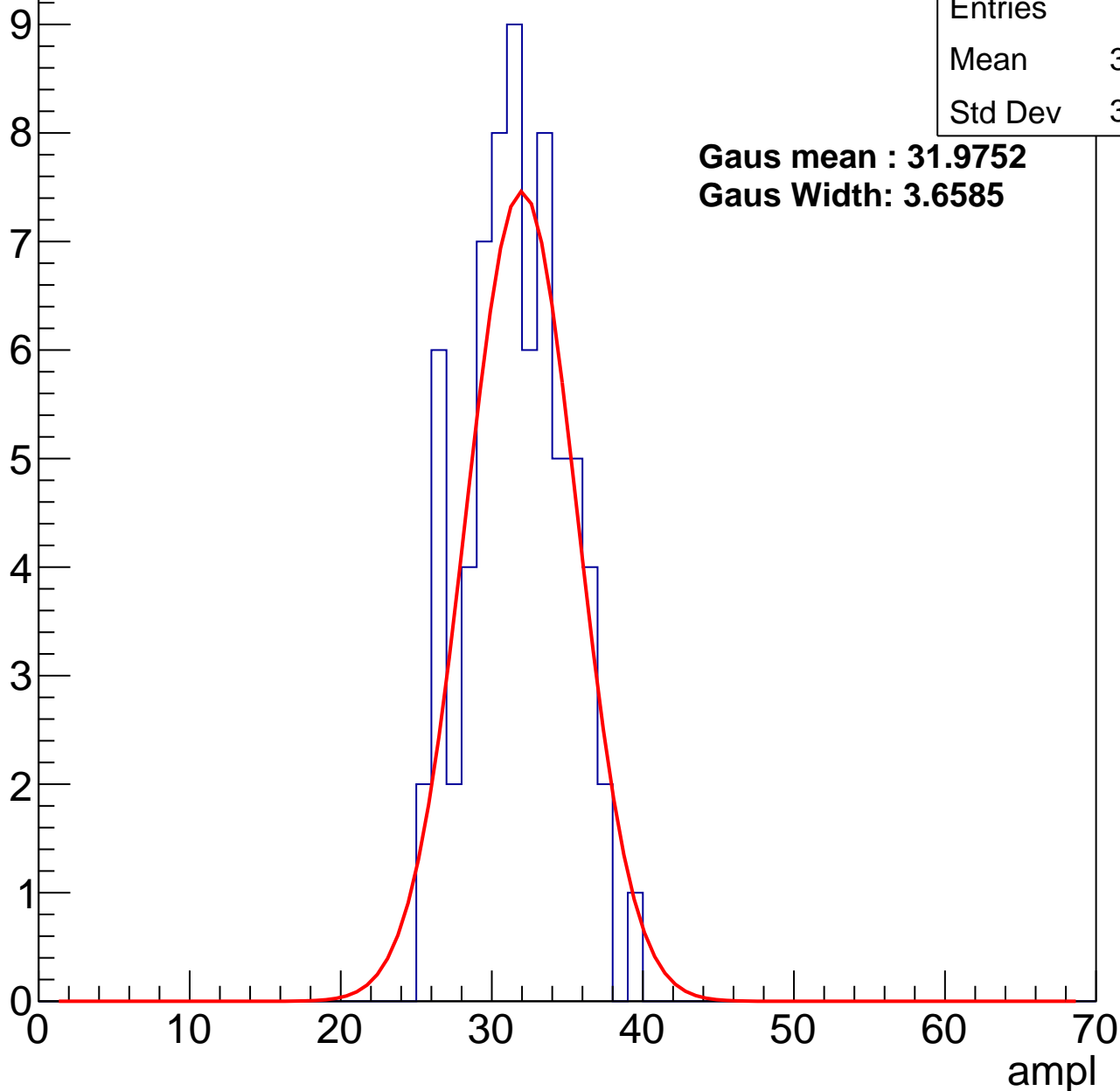
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	69
Mean	31.19
Std Dev	3.236

**Gaus mean : 31.9752**

**Gaus Width: 3.6585**



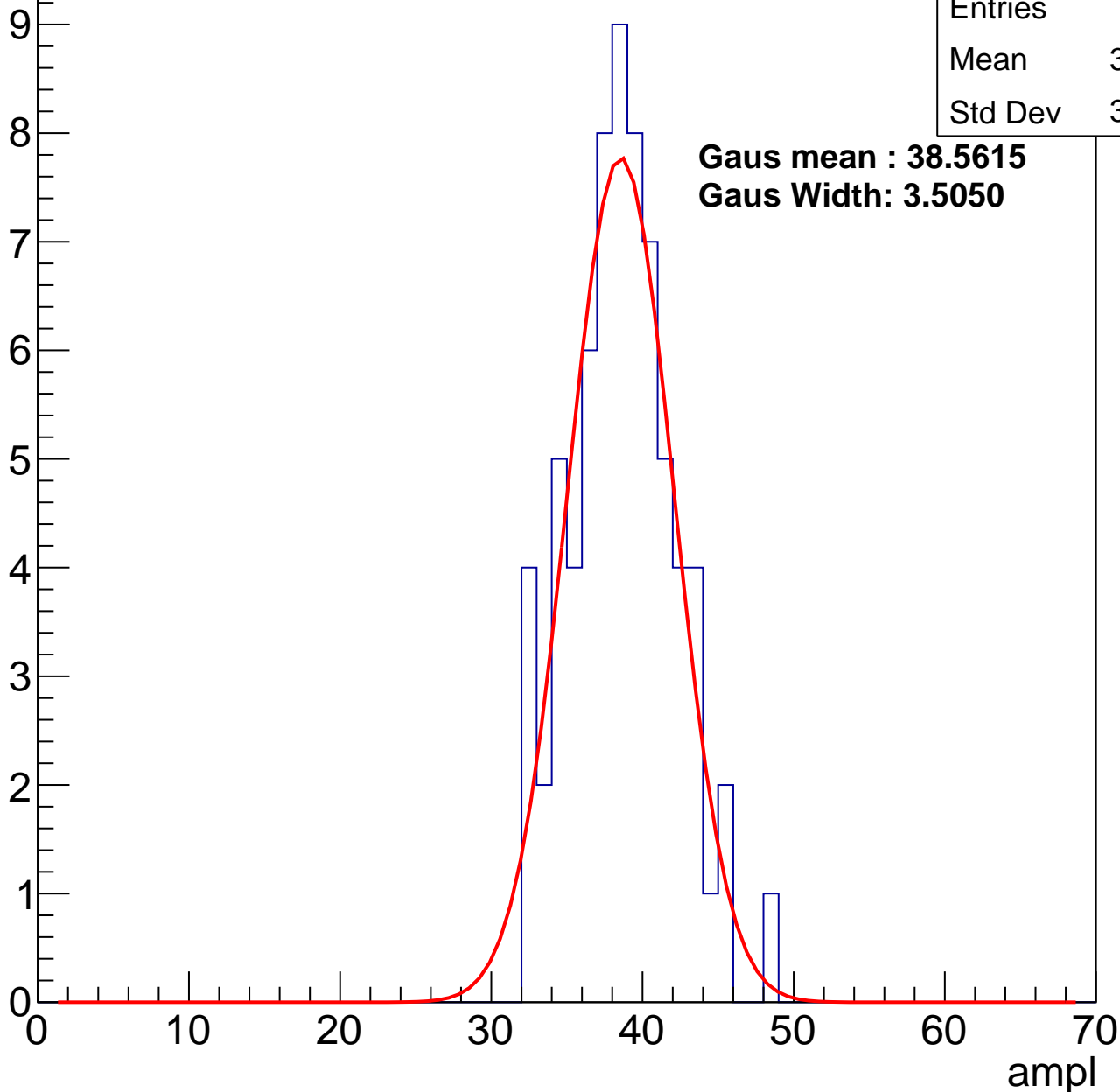
# B1L103S, U11-ch75, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	70
Mean	38.24
Std Dev	3.416

**Gaus mean : 38.5615**  
**Gaus Width: 3.5050**



# B1L103S, U11-ch75, adc2

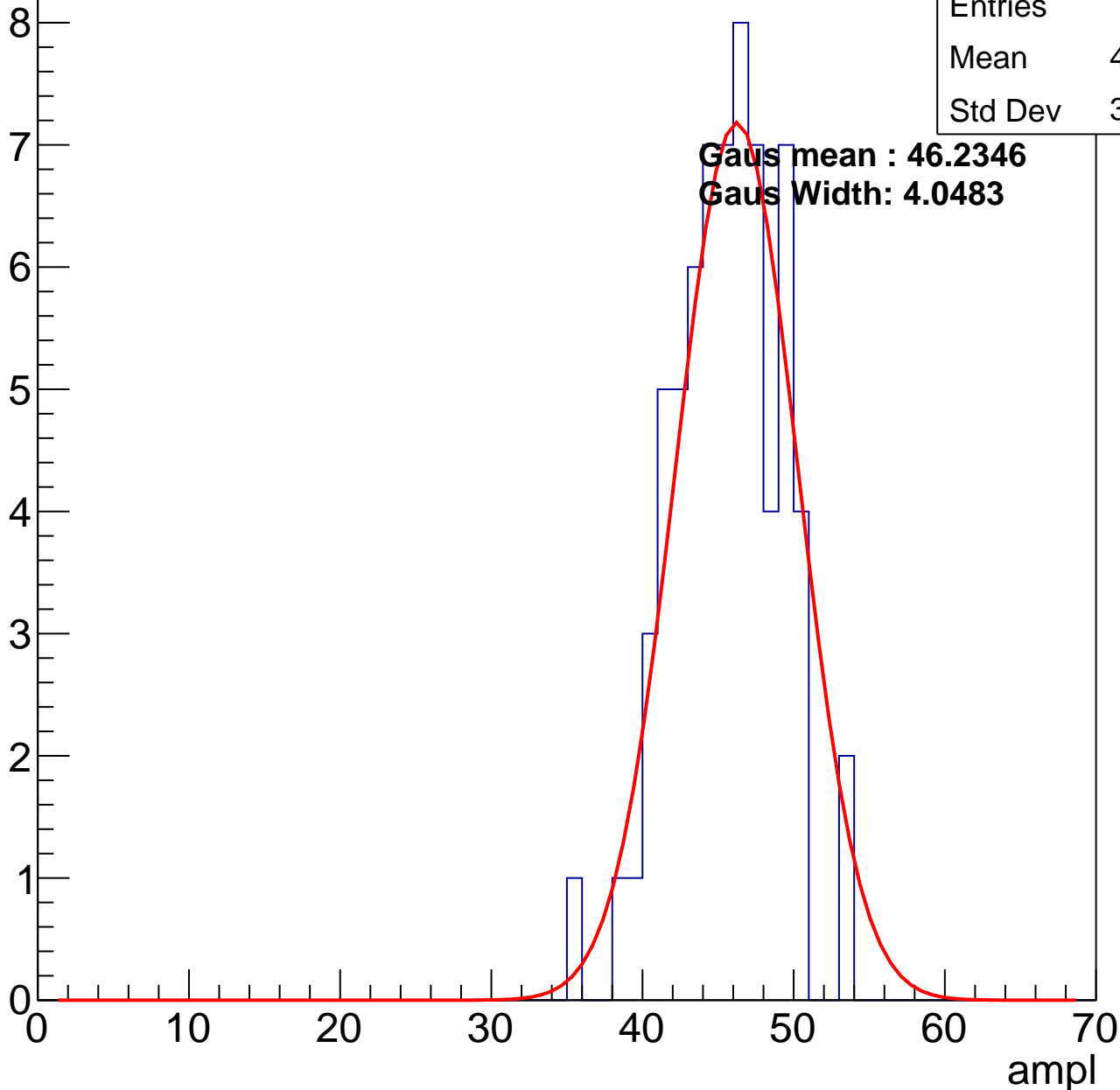
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	68
Mean	45.09
Std Dev	3.488

Gaus mean : 46.2346

Gaus Width: 4.0483

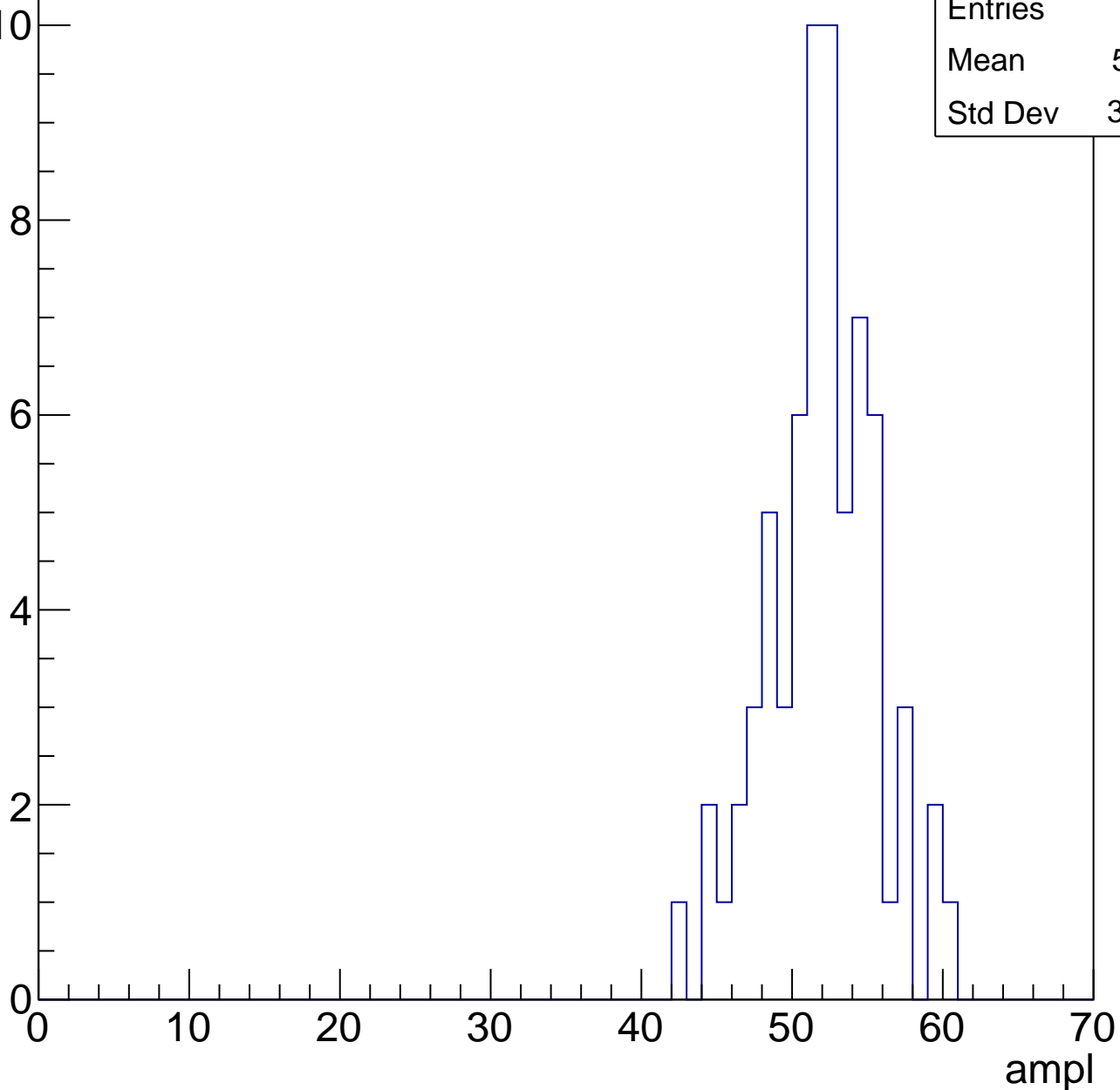


# B1L103S, U11-ch75, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	68
Mean	51.51
Std Dev	3.616

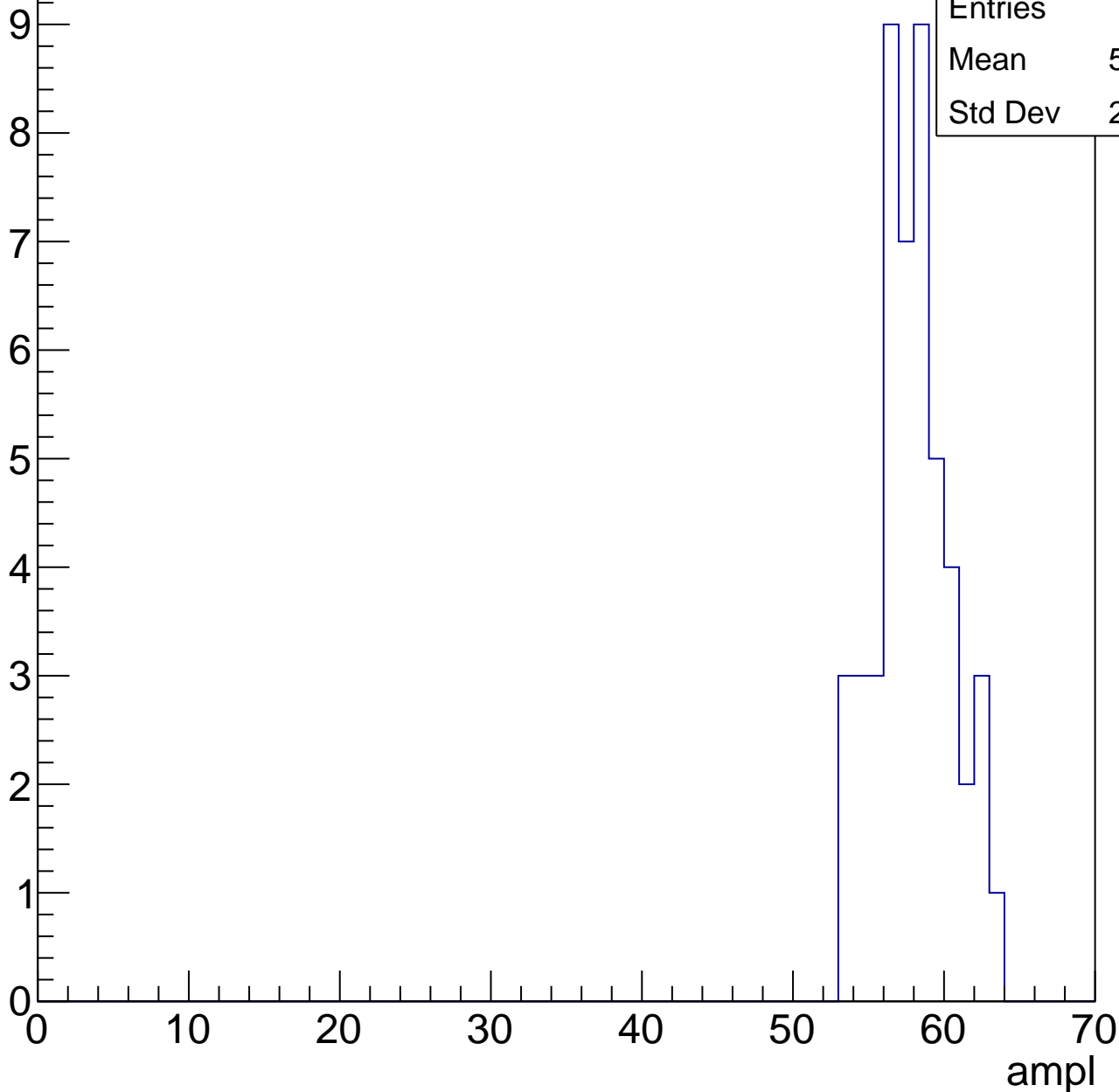


# B1L103S, U11-ch75, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	49
Mean	57.49
Std Dev	2.442

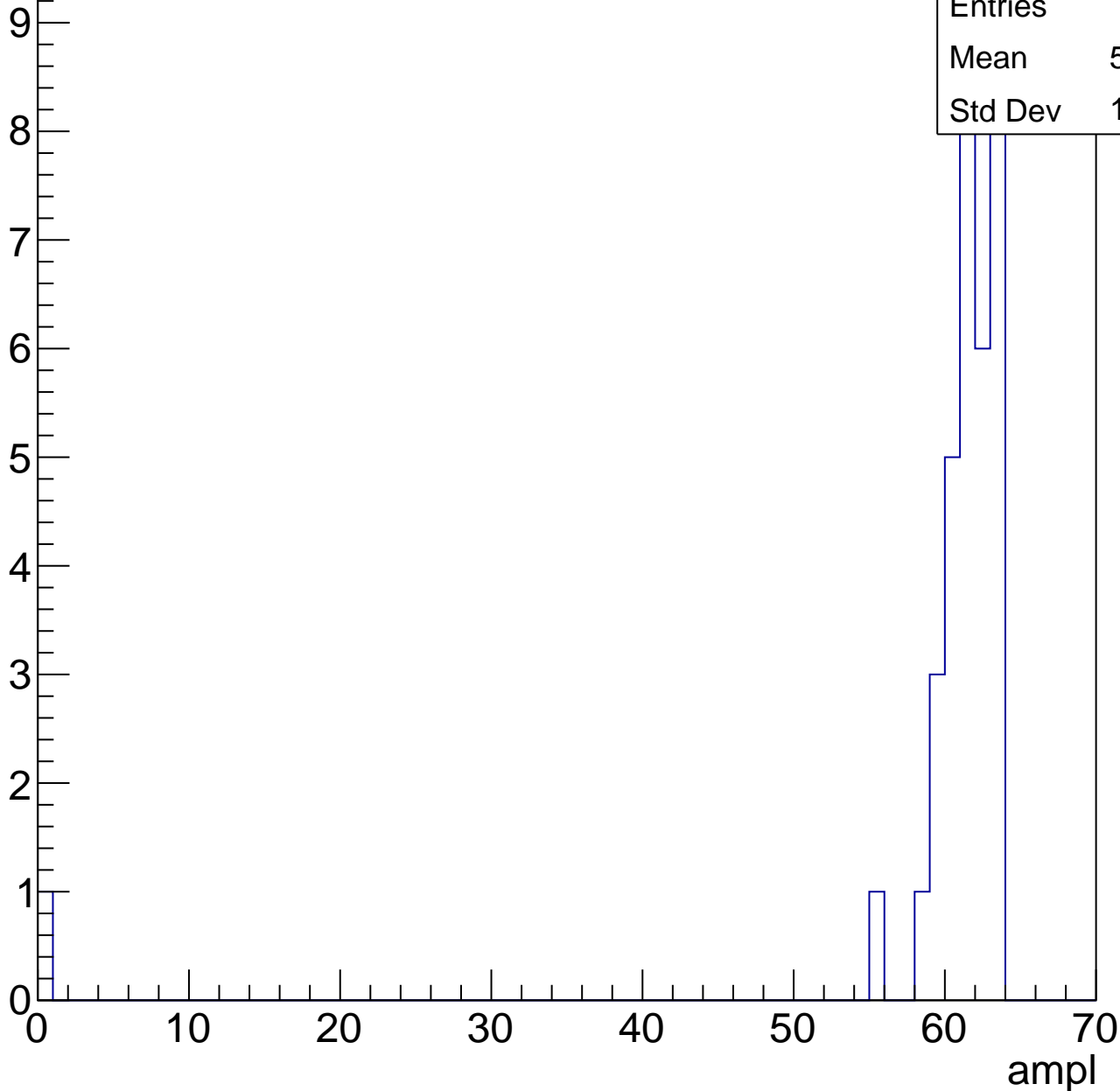


# B1L103S, U11-ch75, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	34
Mean	59.32
Std Dev	10.47



# B1L103S, U11-ch75, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	62
Std Dev	0



# B1L103S, U11-ch75, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U11-ch76, adc0

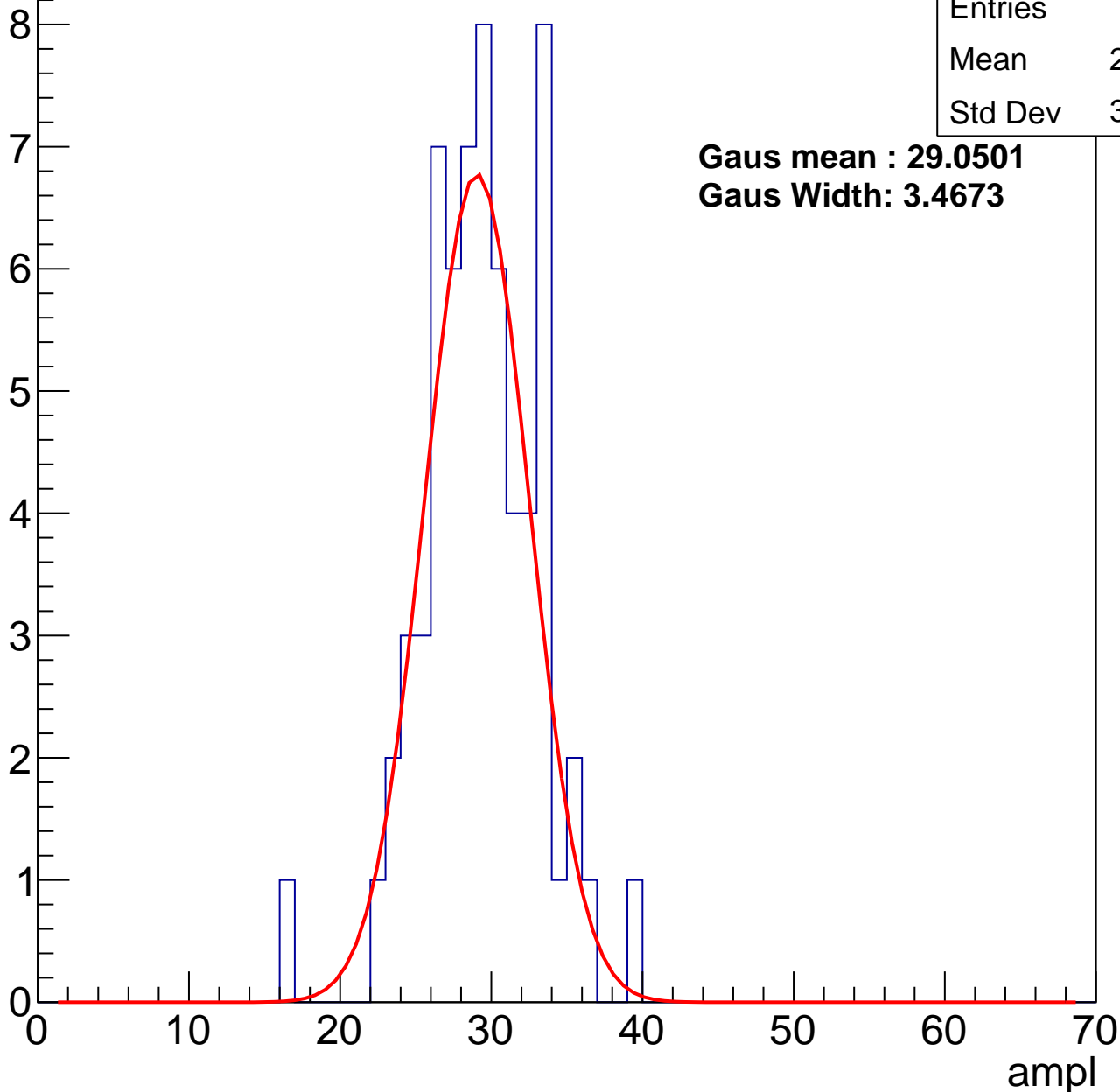
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	28.89
Std Dev	3.799

**Gaus mean : 29.0501**

**Gaus Width: 3.4673**



# B1L103S, U11-ch76, adc1

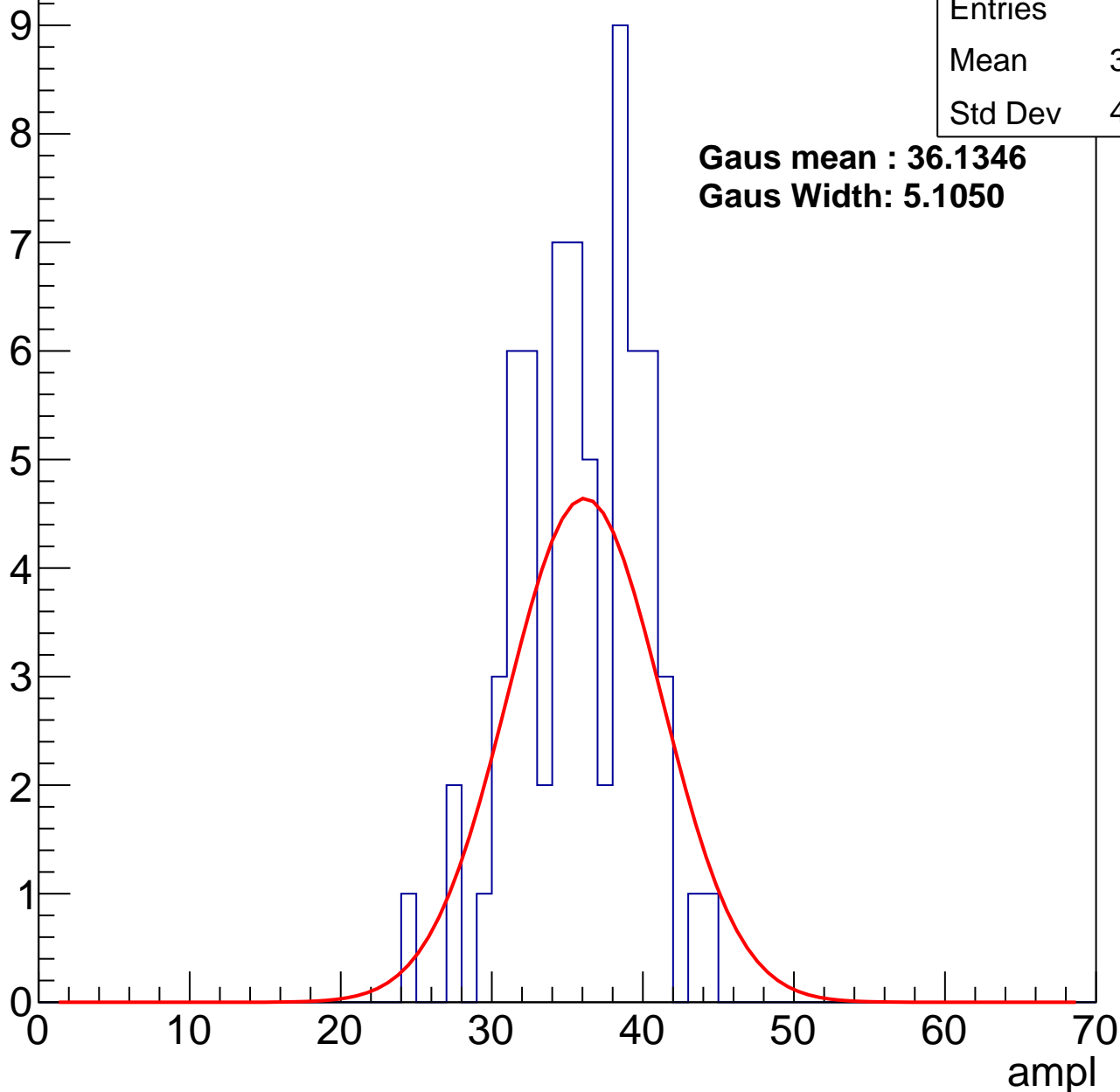
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	68
Mean	35.35
Std Dev	4.039

**Gaus mean : 36.1346**

**Gaus Width: 5.1050**



# B1L103S, U11-ch76, adc2

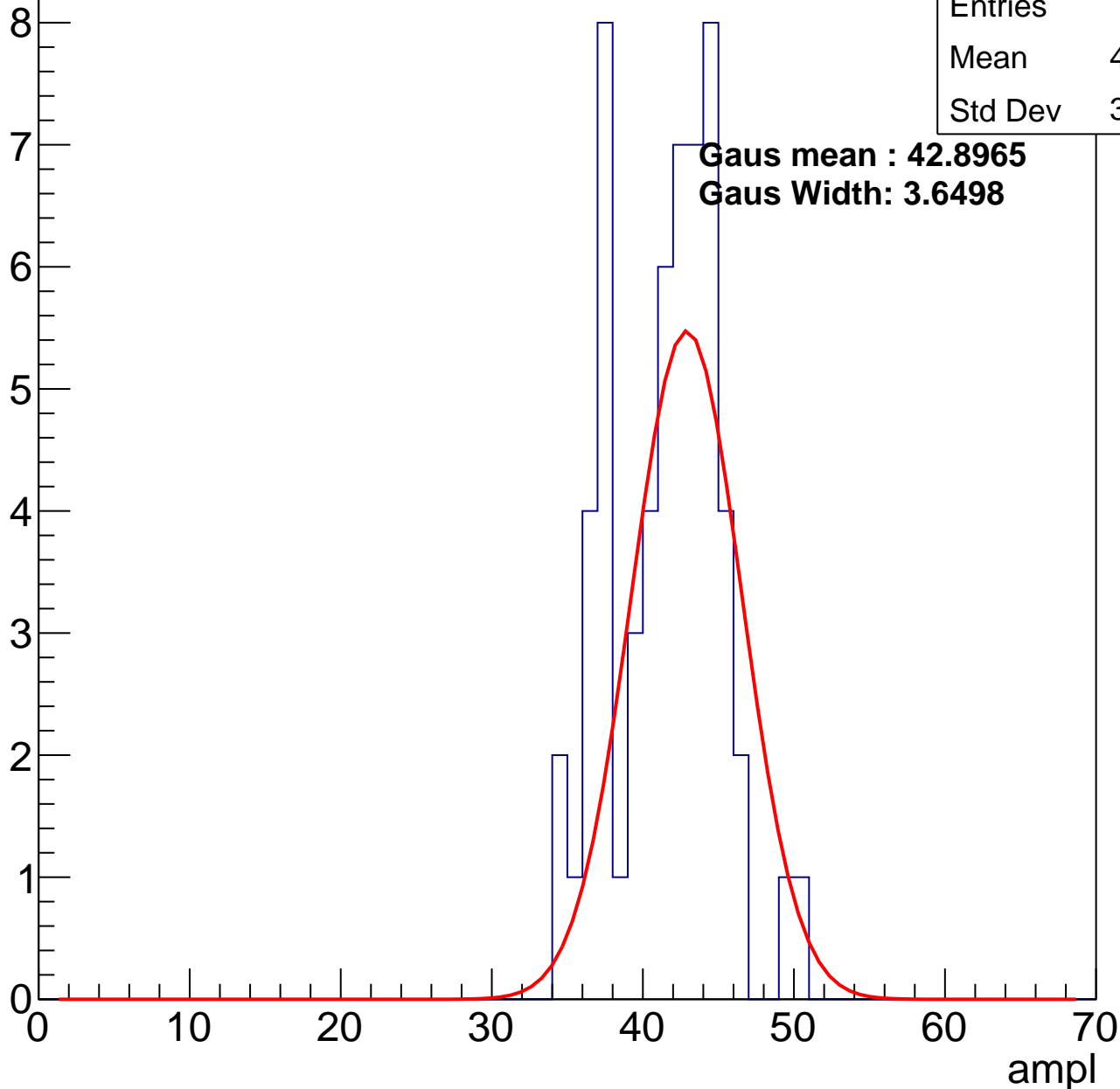
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	59
Mean	41.05
Std Dev	3.572

**Gaus mean : 42.8965**

**Gaus Width: 3.6498**



# B1L103S, U11-ch76, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

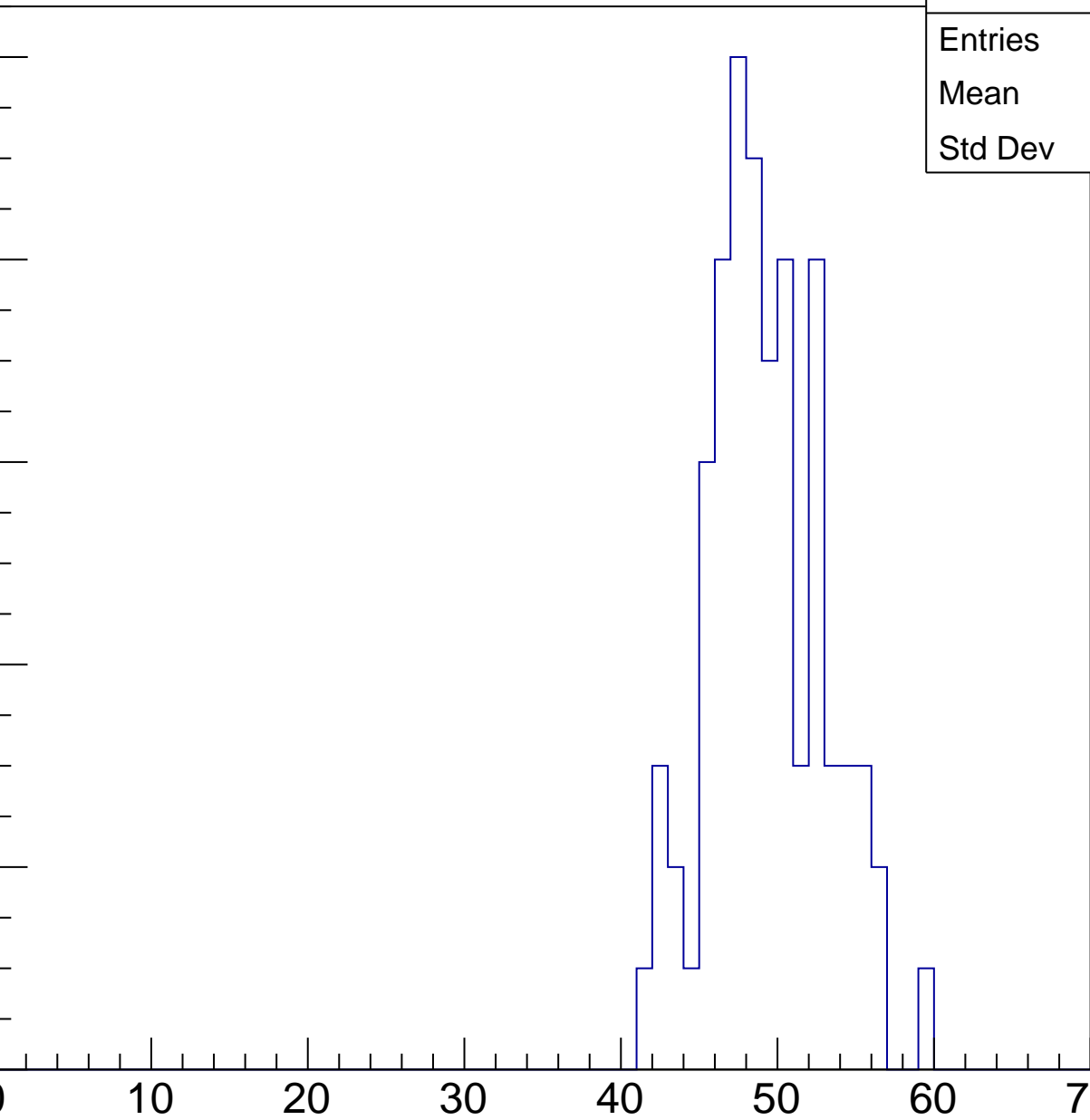
Entries	78
Mean	48.79
Std Dev	3.656

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

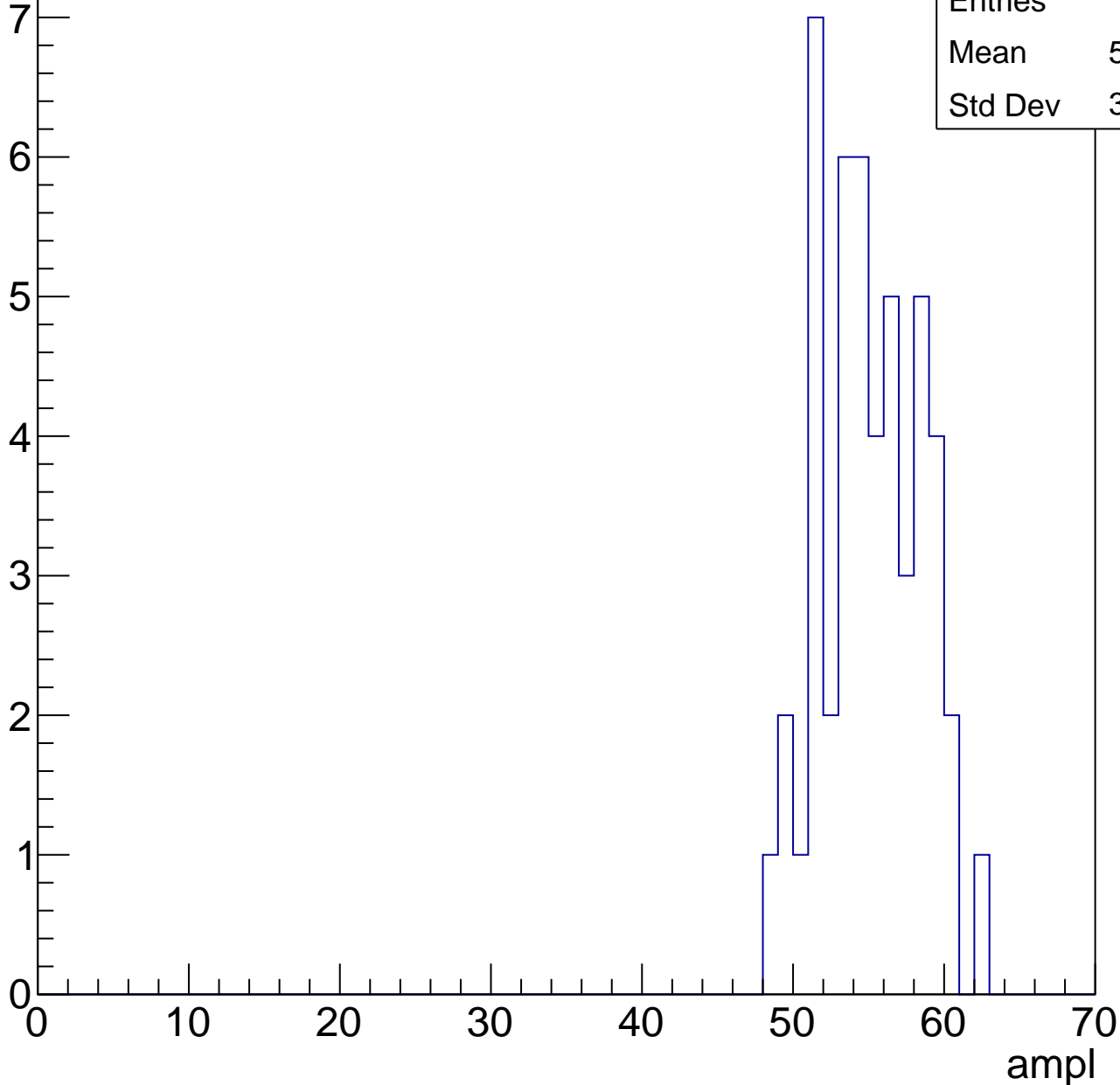


# B1L103S, U11-ch76, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	49
Mean	54.65
Std Dev	3.274

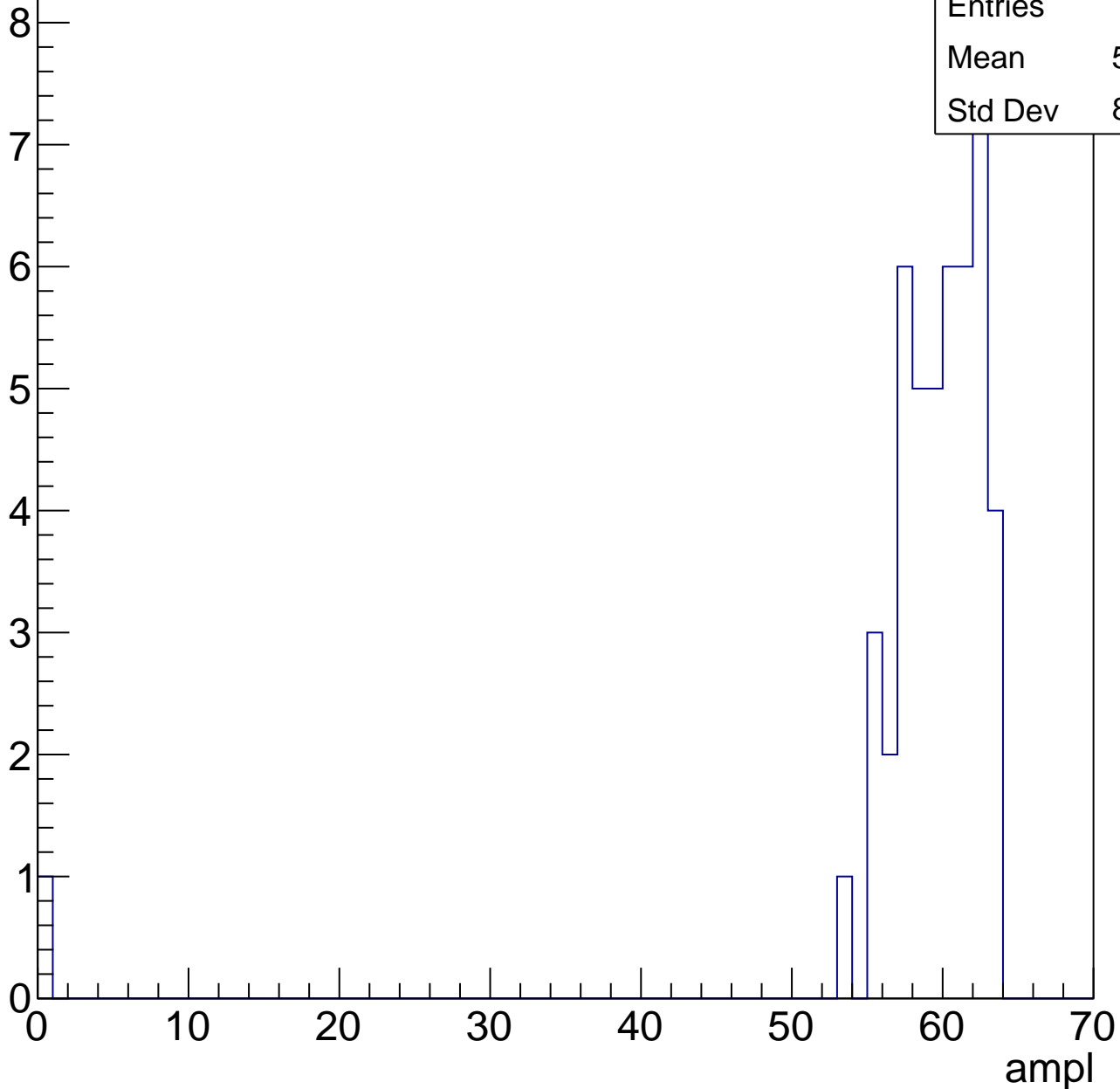


# B1L103S, U11-ch76, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	47
Mean	58.11
Std Dev	8.921

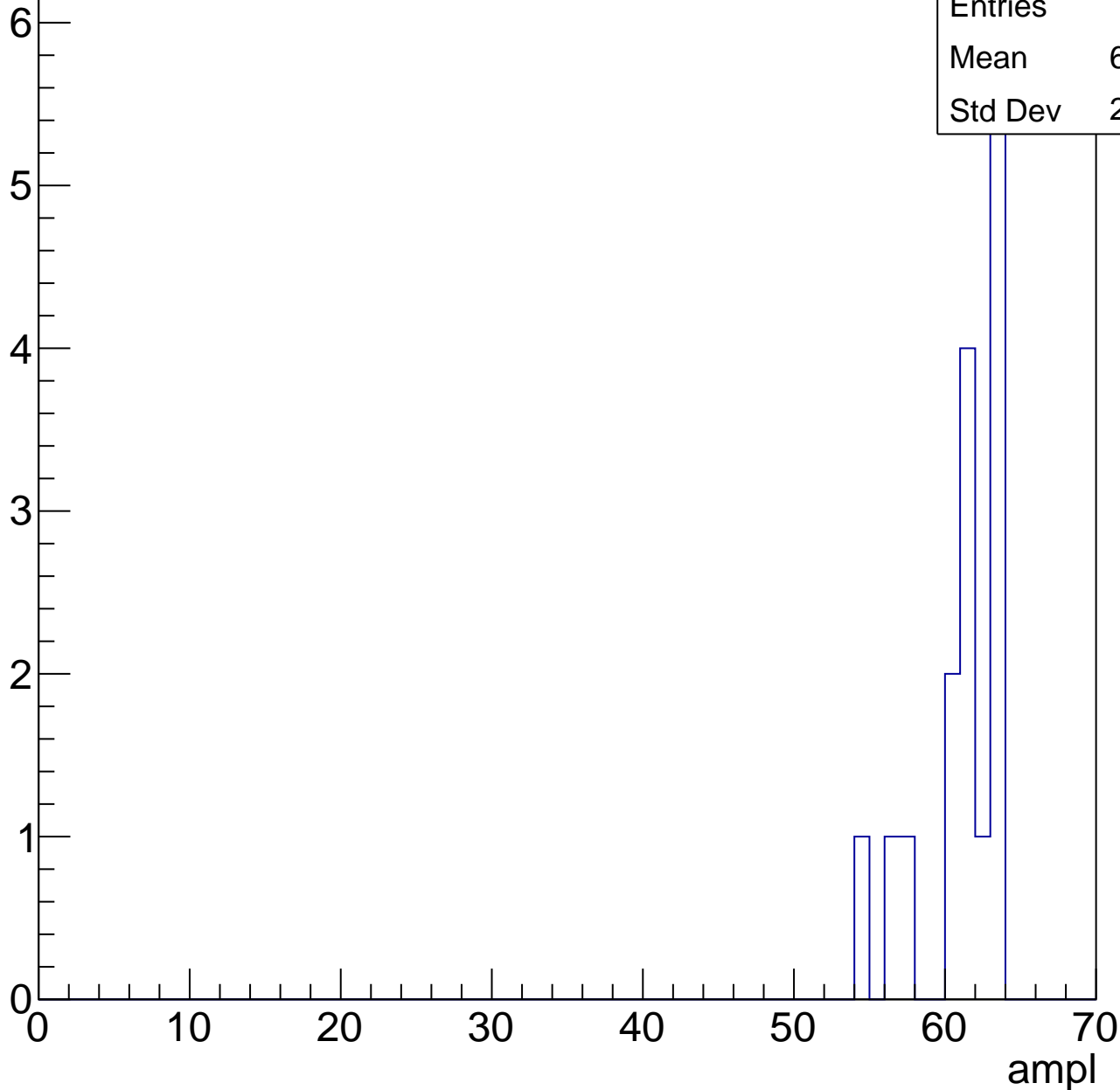


# B1L103S, U11-ch76, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	16
Mean	60.69
Std Dev	2.686





# B1L103S, U11-ch76, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L103S, U11-ch77, adc0

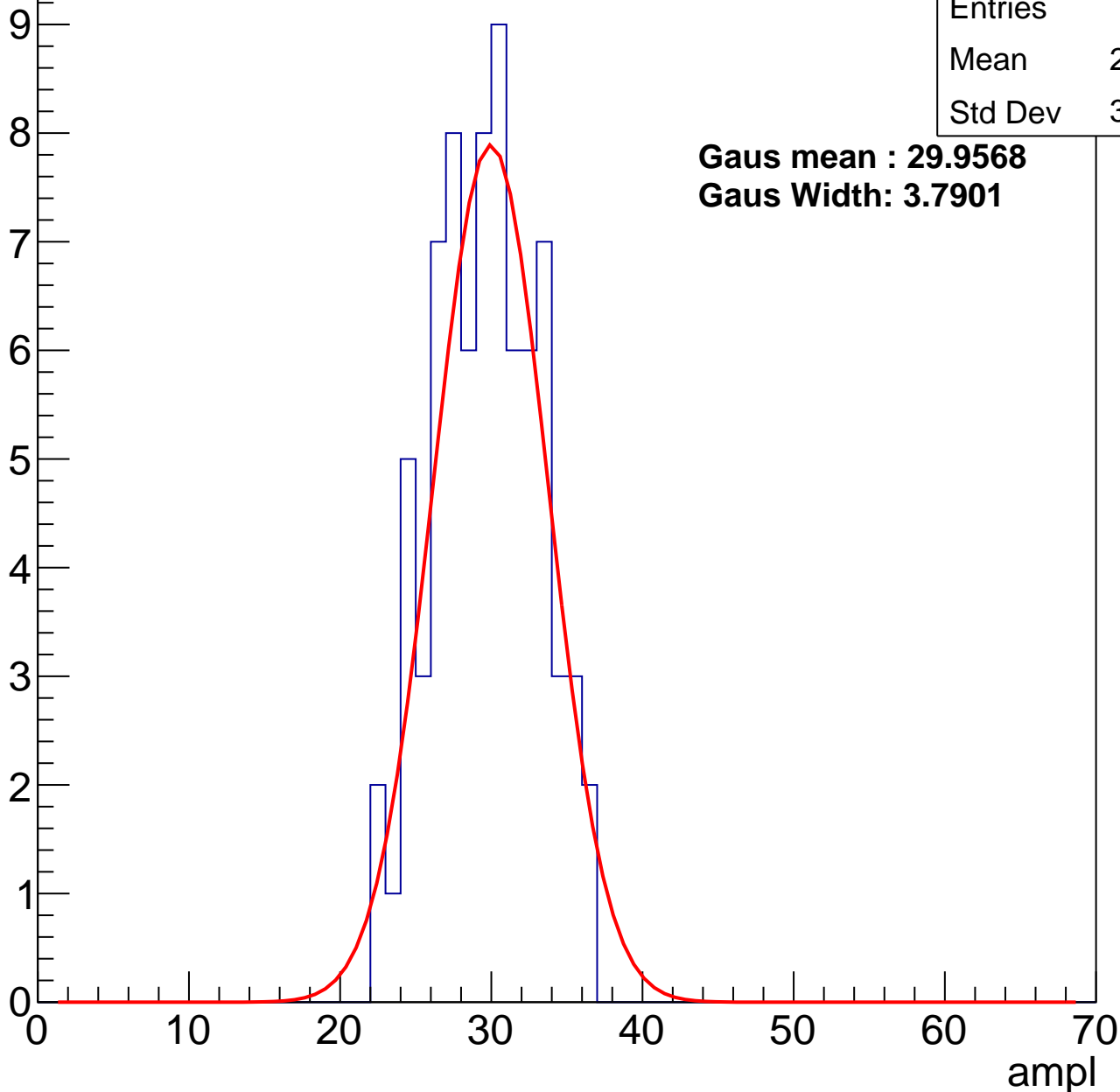
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	76
Mean	29.18
Std Dev	3.413

**Gaus mean : 29.9568**

**Gaus Width: 3.7901**



# B1L103S, U11-ch77, adc1

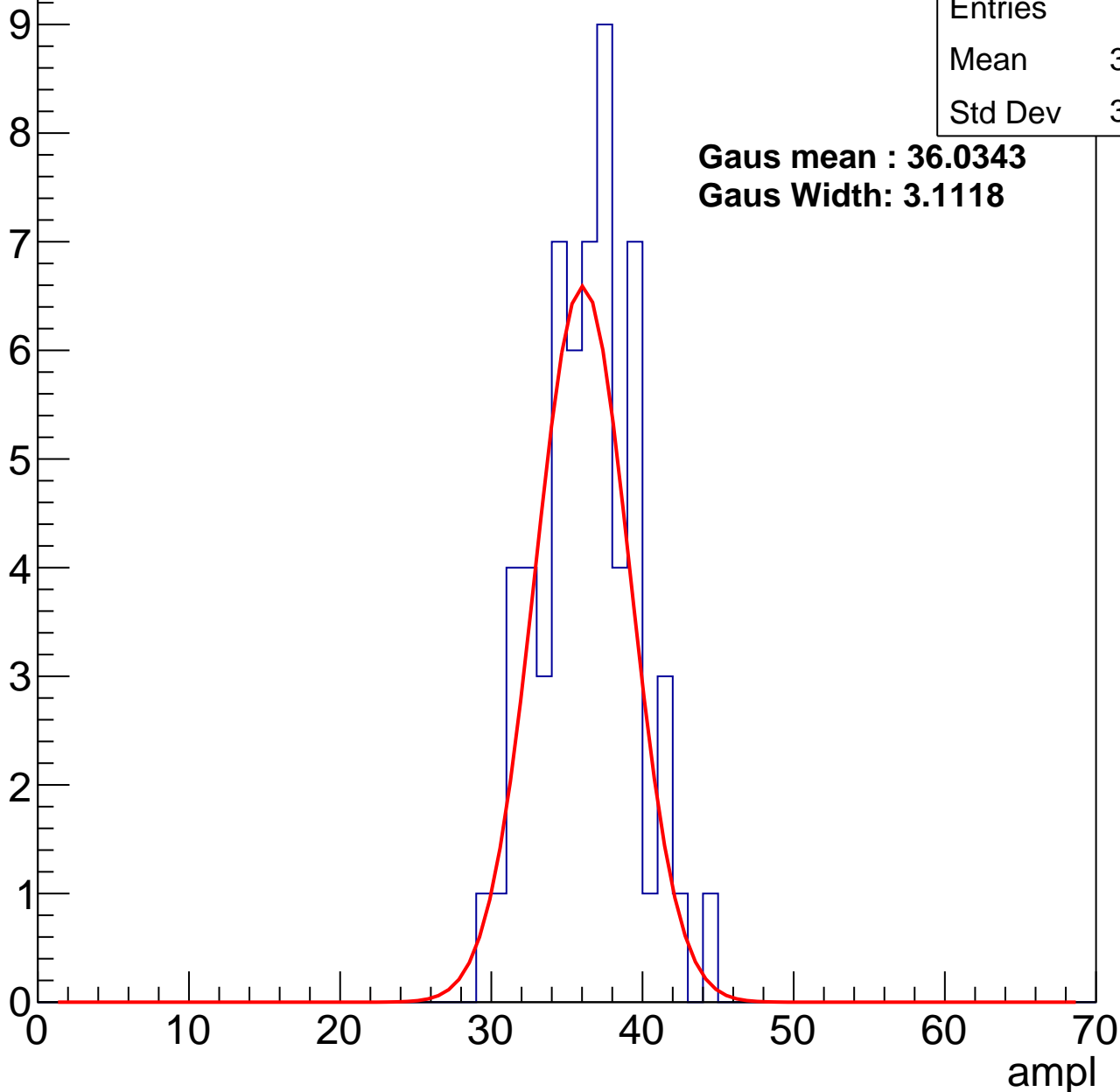
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	59
Mean	35.88
Std Dev	3.157

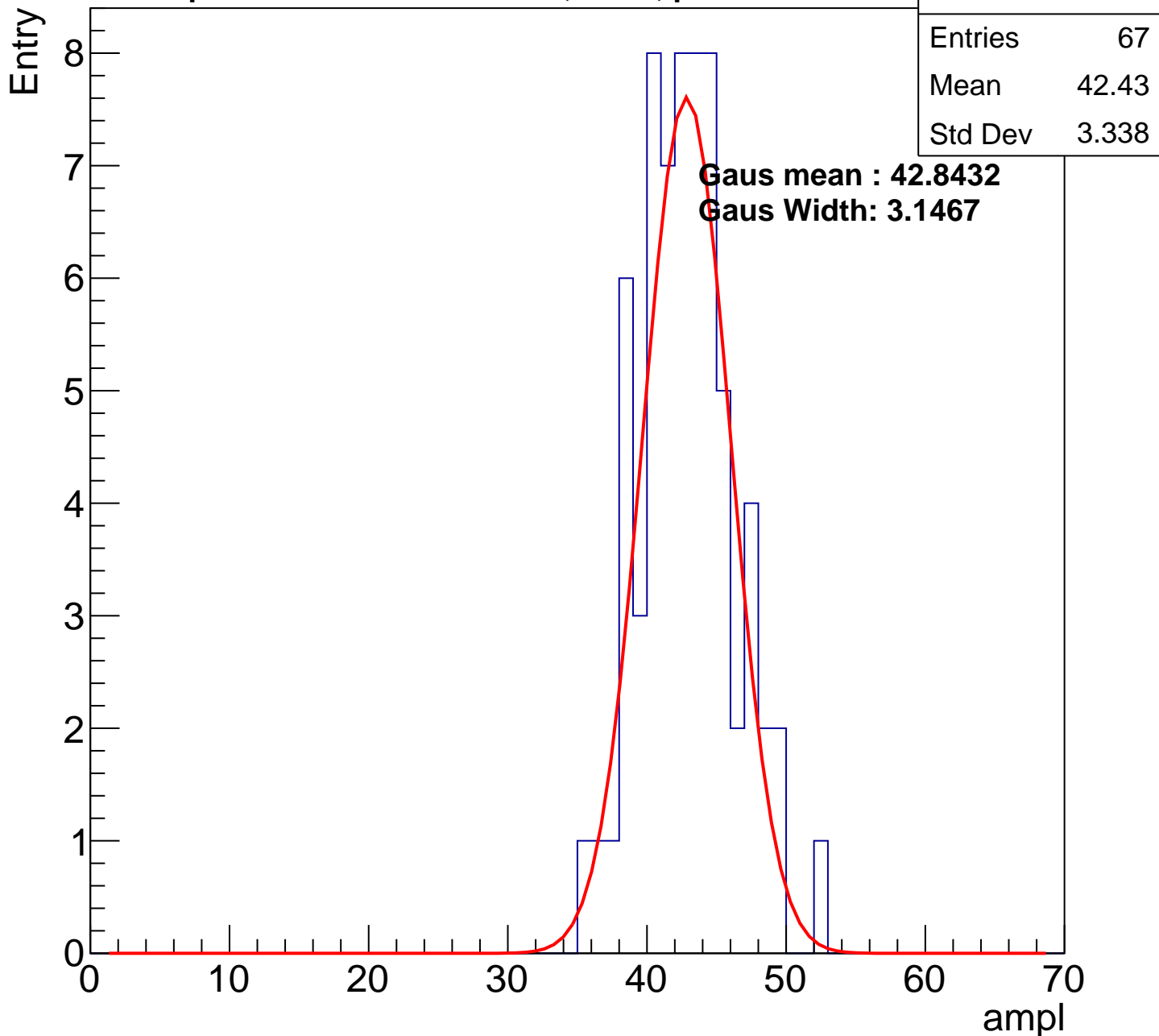
**Gaus mean : 36.0343**

**Gaus Width: 3.1118**



# B1L103S, U11-ch77, adc2

calib\_packv5\_042523\_0143.root, FC#7, port C2

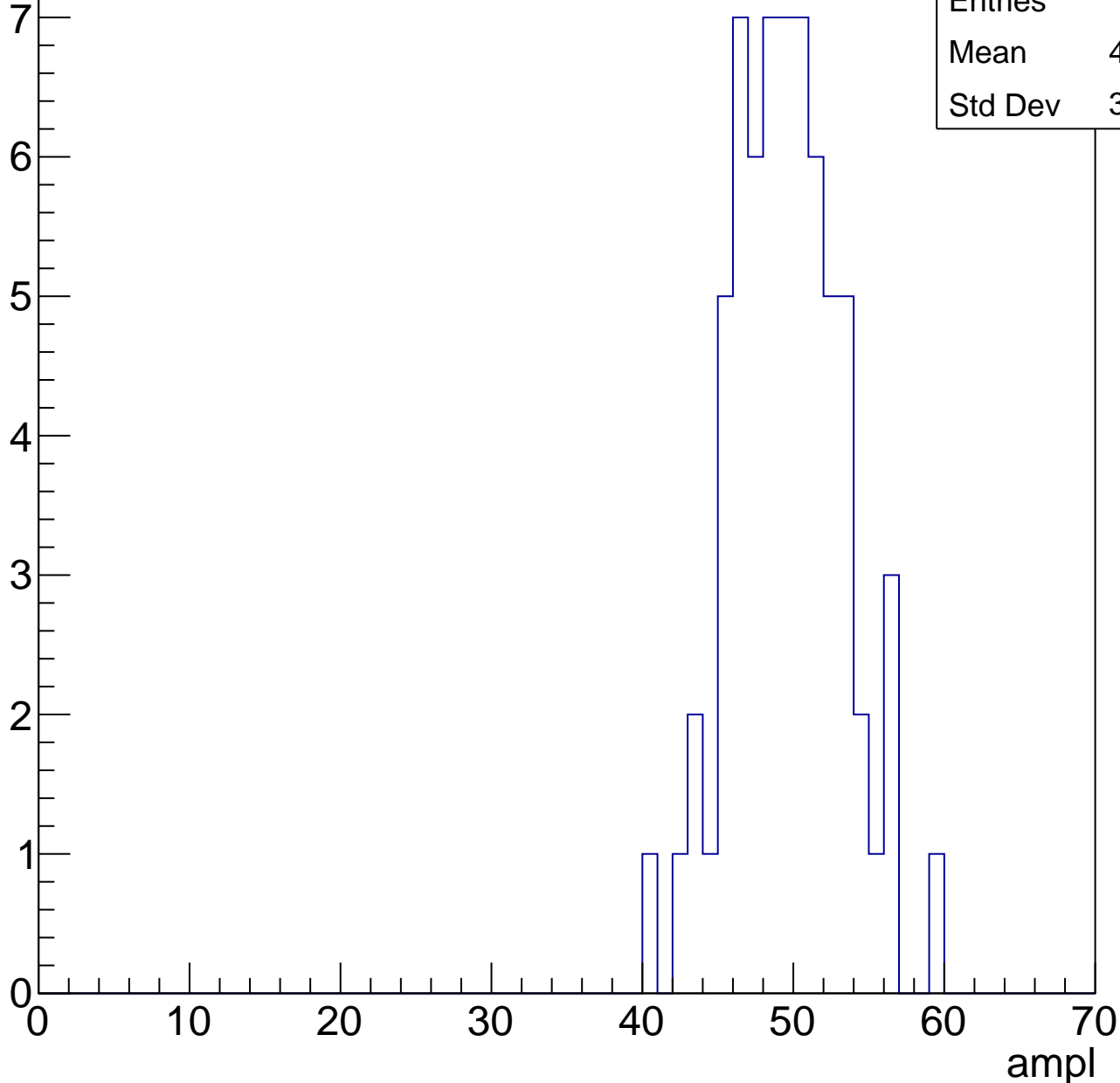


# B1L103S, U11-ch77, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	49.12
Std Dev	3.643

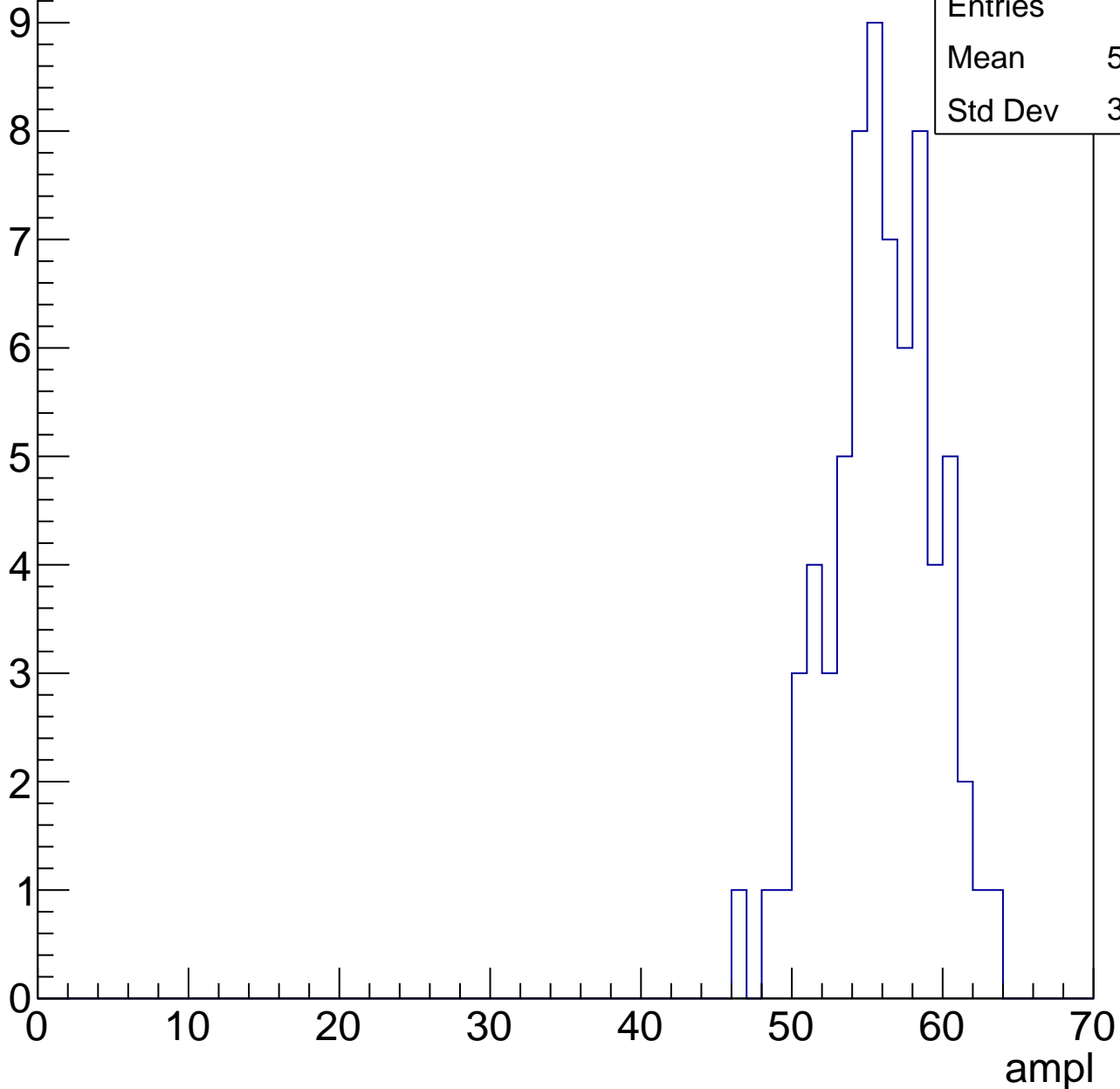


# B1L103S, U11-ch77, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	69
Mean	55.45
Std Dev	3.454

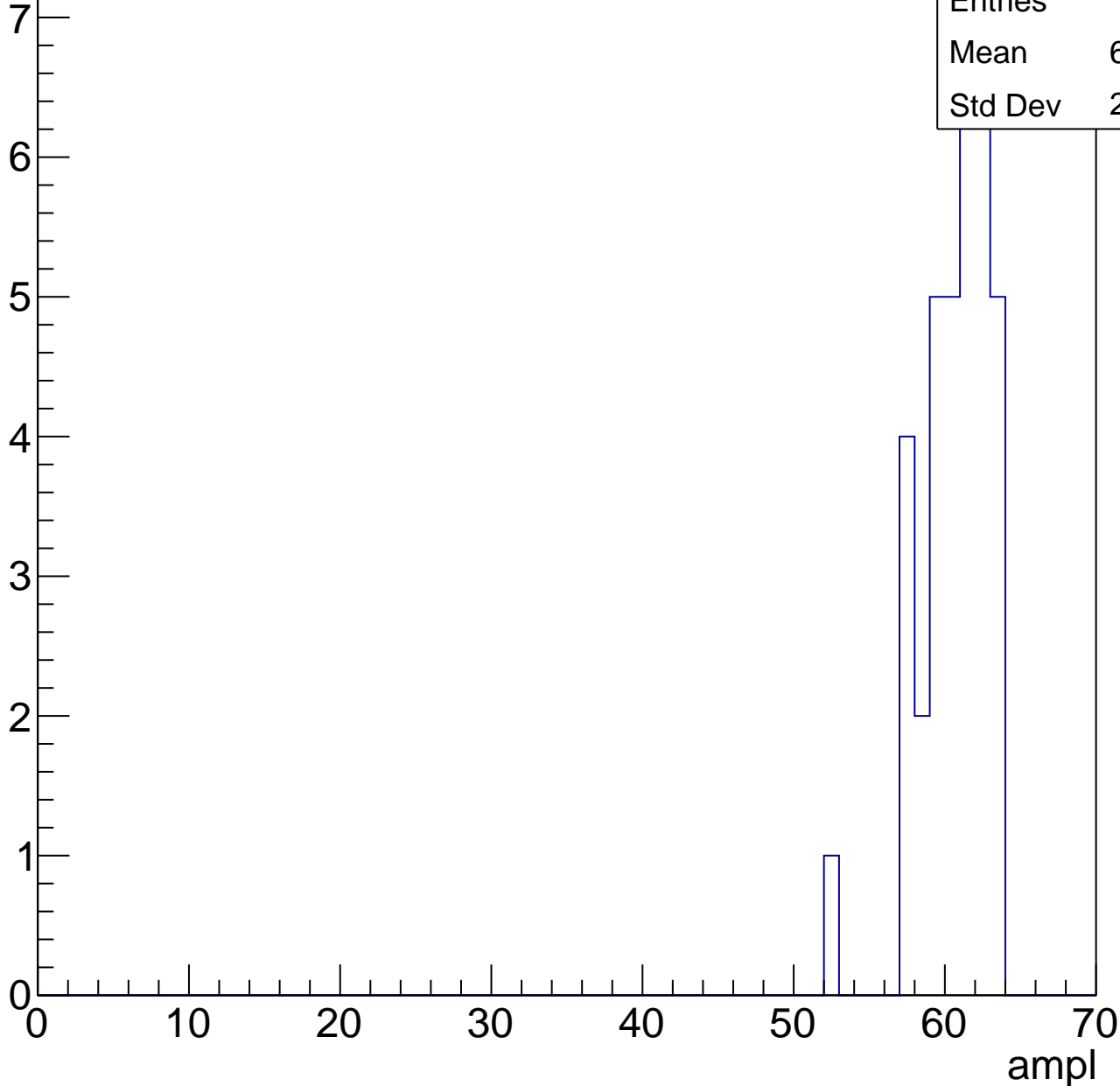


# B1L103S, U11-ch77, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	36
Mean	60.19
Std Dev	2.307



# B1L103S, U11-ch77, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U11-ch77, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U11-ch78, adc0

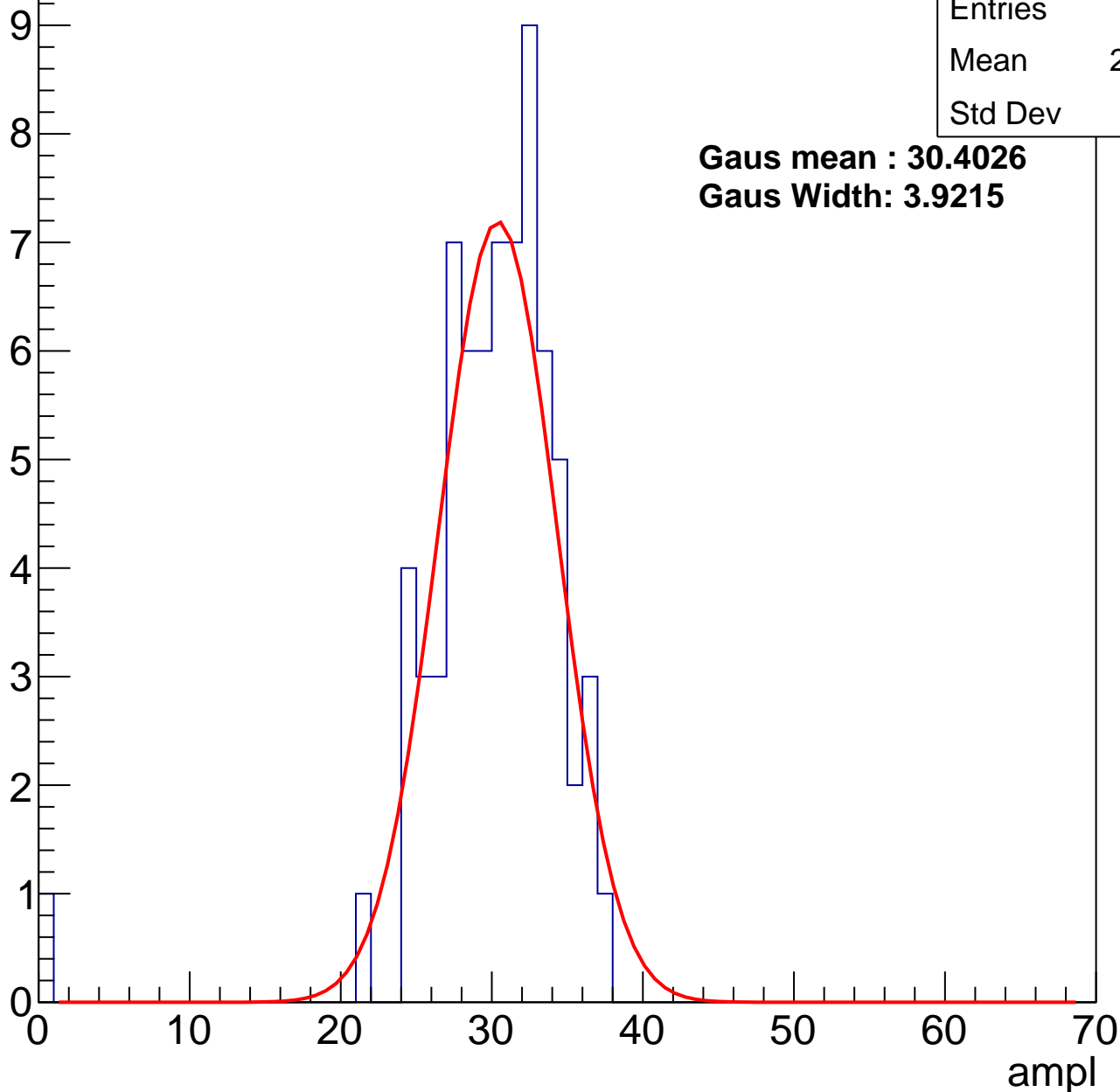
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	71
Mean	29.56
Std Dev	4.91

**Gaus mean : 30.4026**

**Gaus Width: 3.9215**



# B1L103S, U11-ch78, adc1

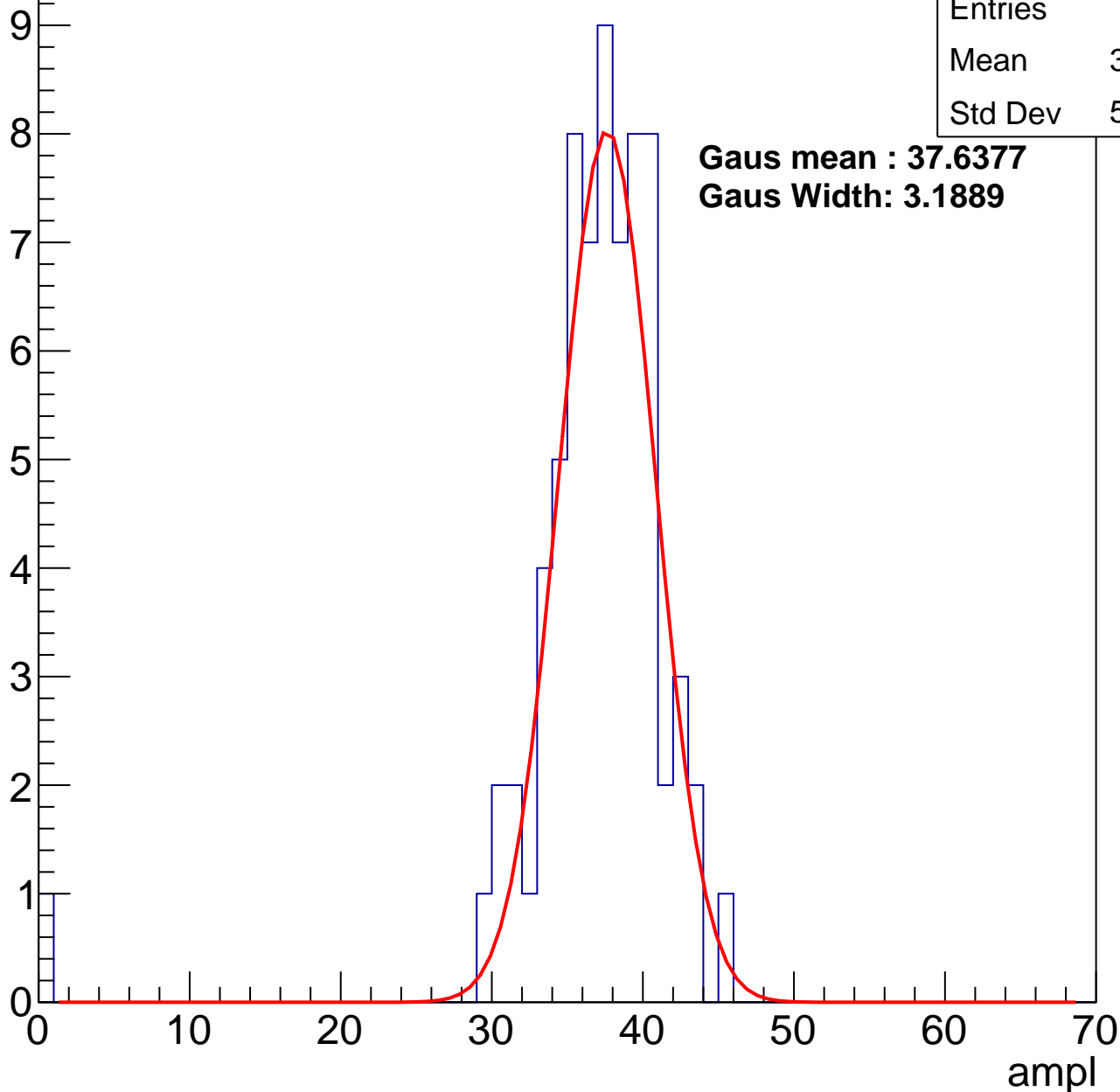
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	71
Mean	36.44
Std Dev	5.448

**Gaus mean : 37.6377**

**Gaus Width: 3.1889**



# B1L103S, U11-ch78, adc2

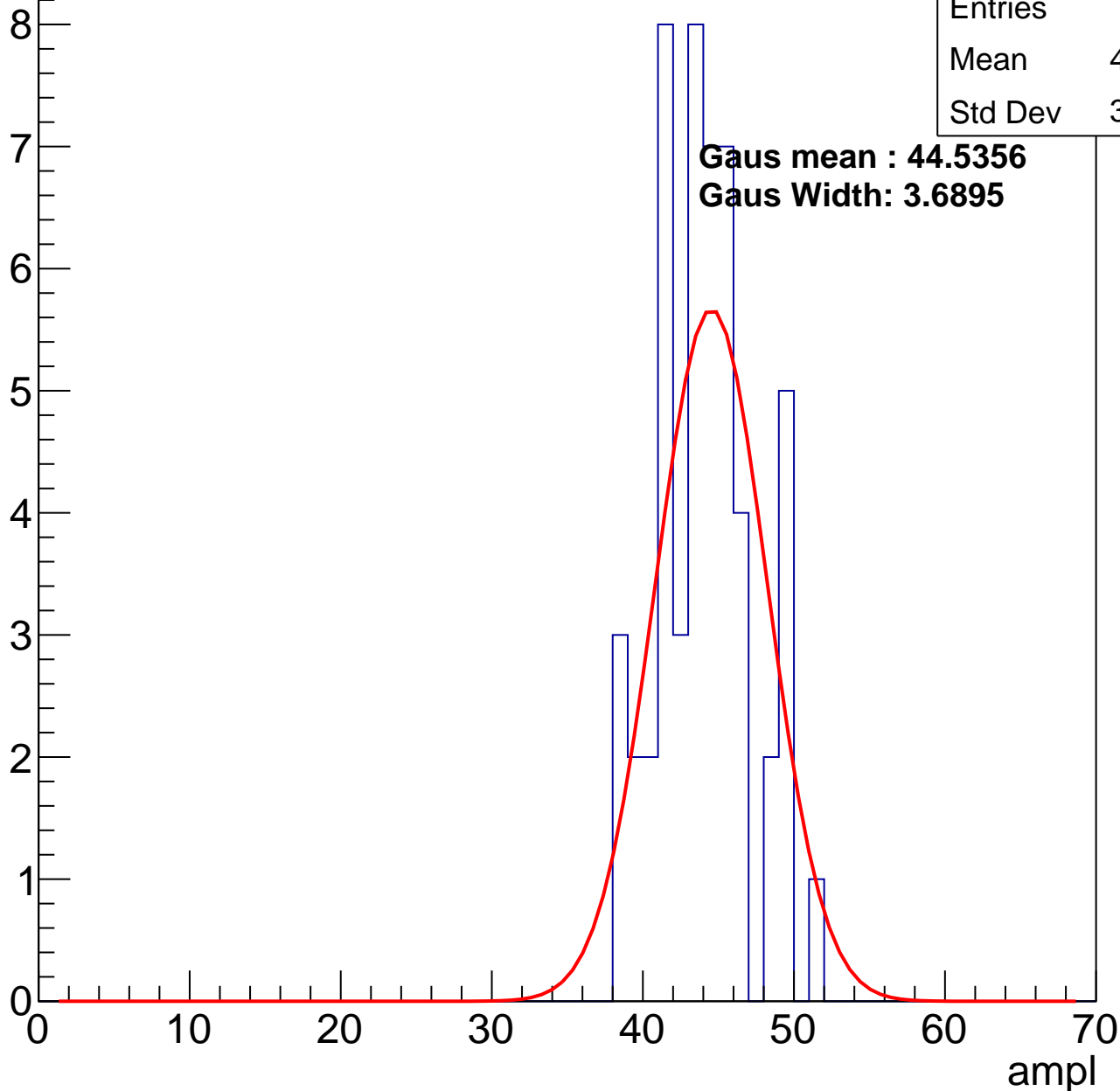
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	52
Mean	43.63
Std Dev	3.113

**Gaus mean : 44.5356**

**Gaus Width: 3.6895**

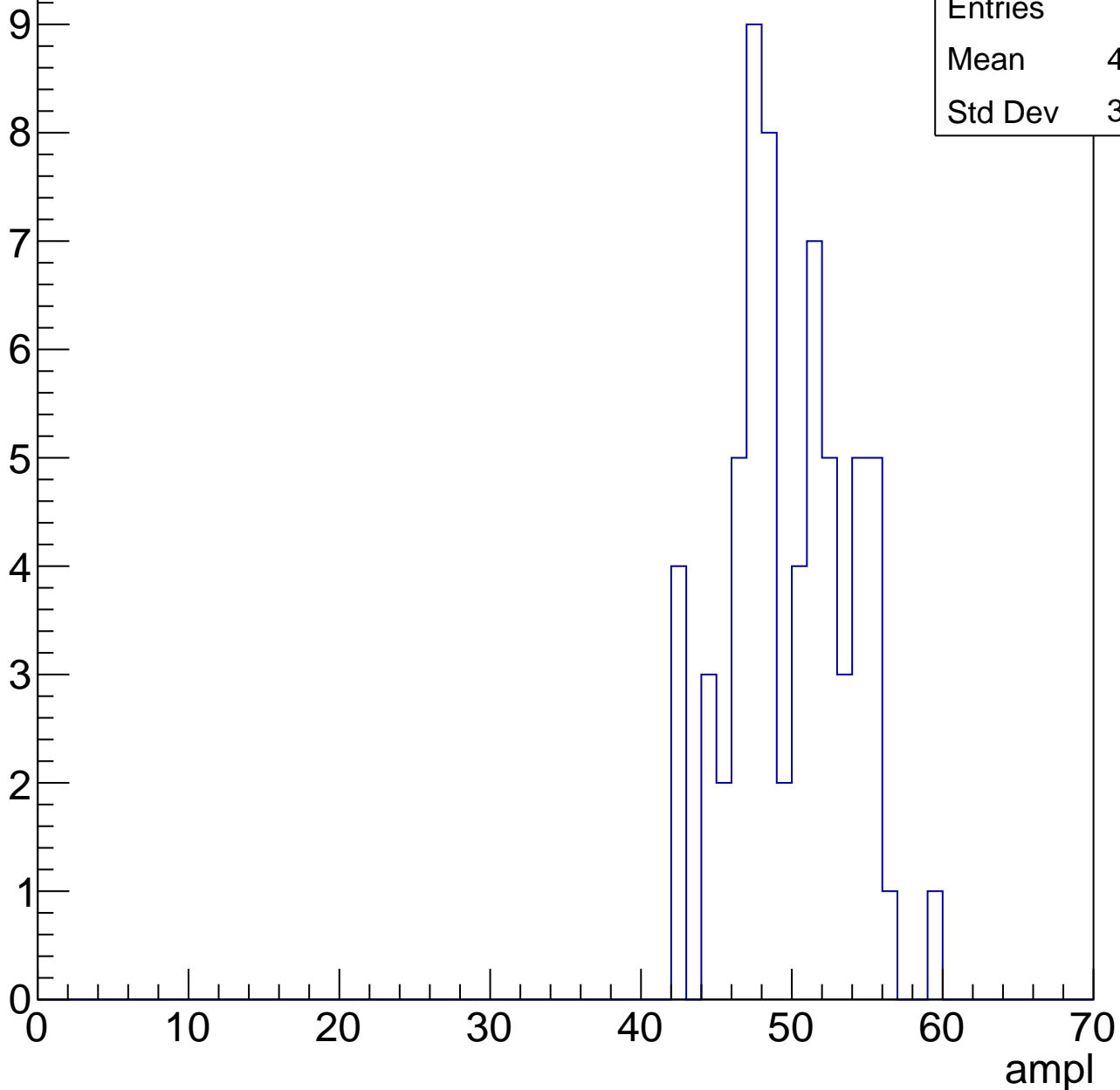


# B1L103S, U11-ch78, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

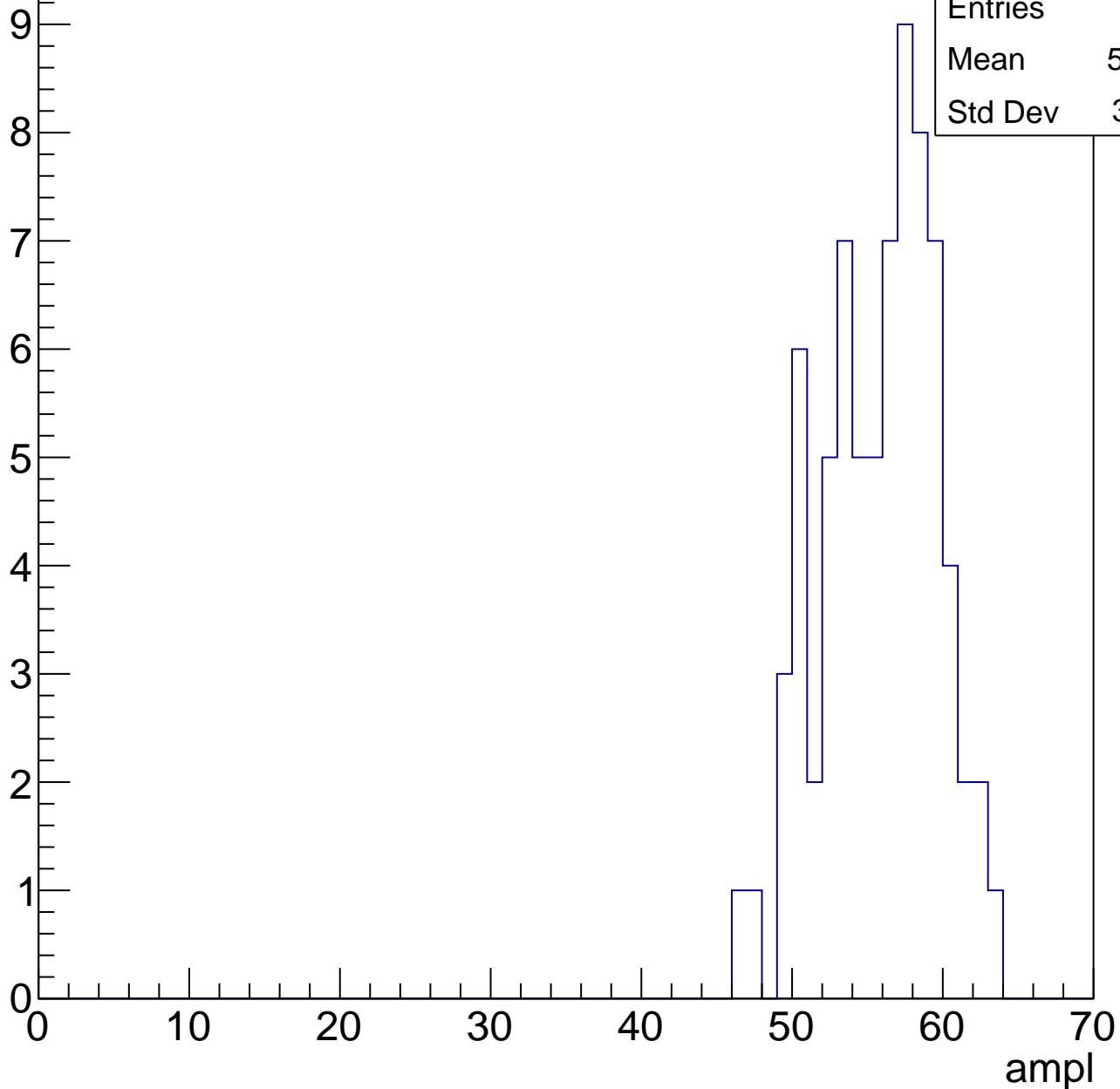
Entries	64
Mean	49.39
Std Dev	3.875



# B1L103S, U11-ch78, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



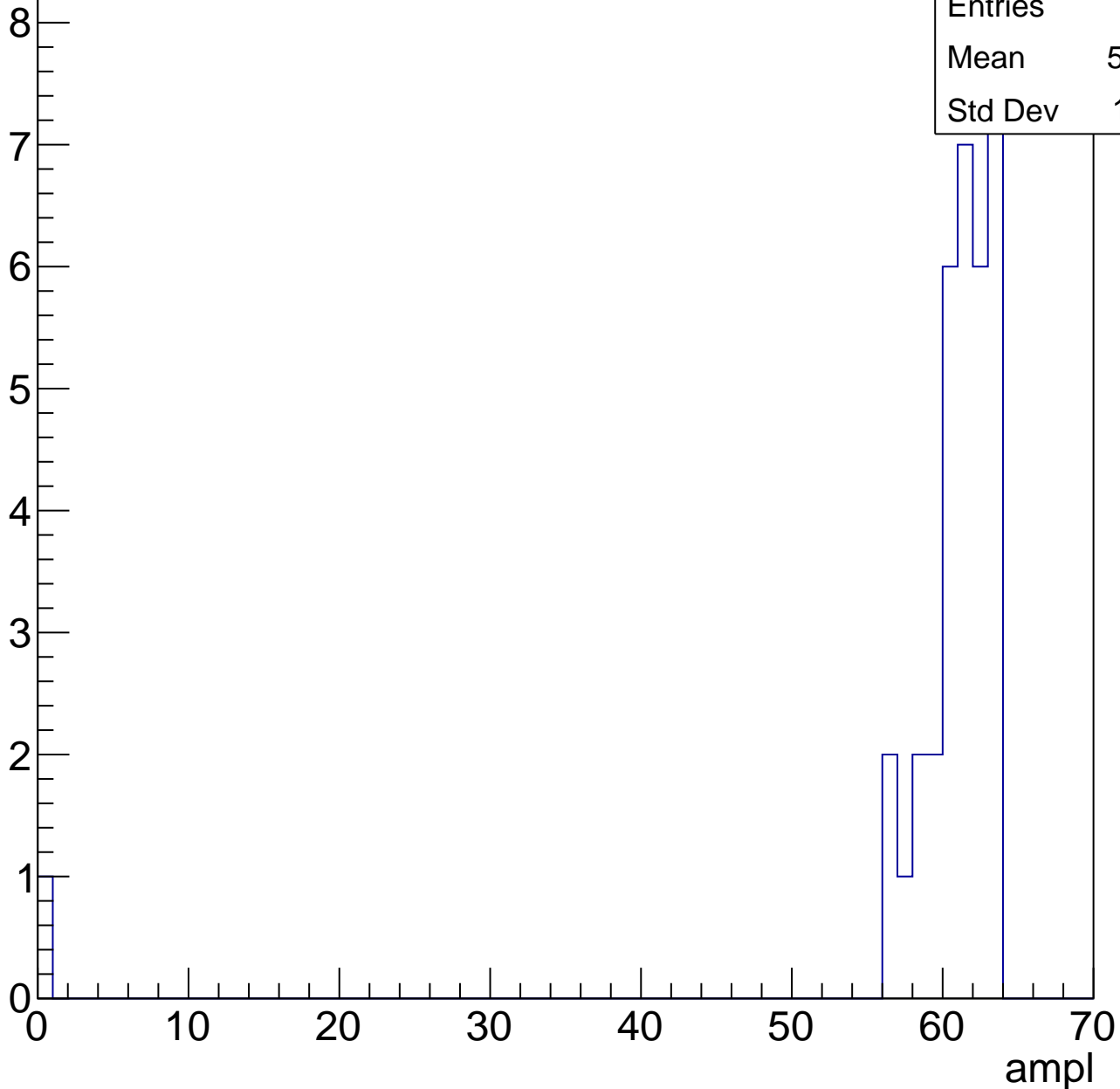
Entries	75
Mean	55.32
Std Dev	3.771

# B1L103S, U11-ch78, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	35
Mean	59.03
Std Dev	10.31



# B1L103S, U11-ch78, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U11-ch78, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U11-ch79, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	67
Mean	30.27
Std Dev	5.077

**Gaus mean : 30.3120**

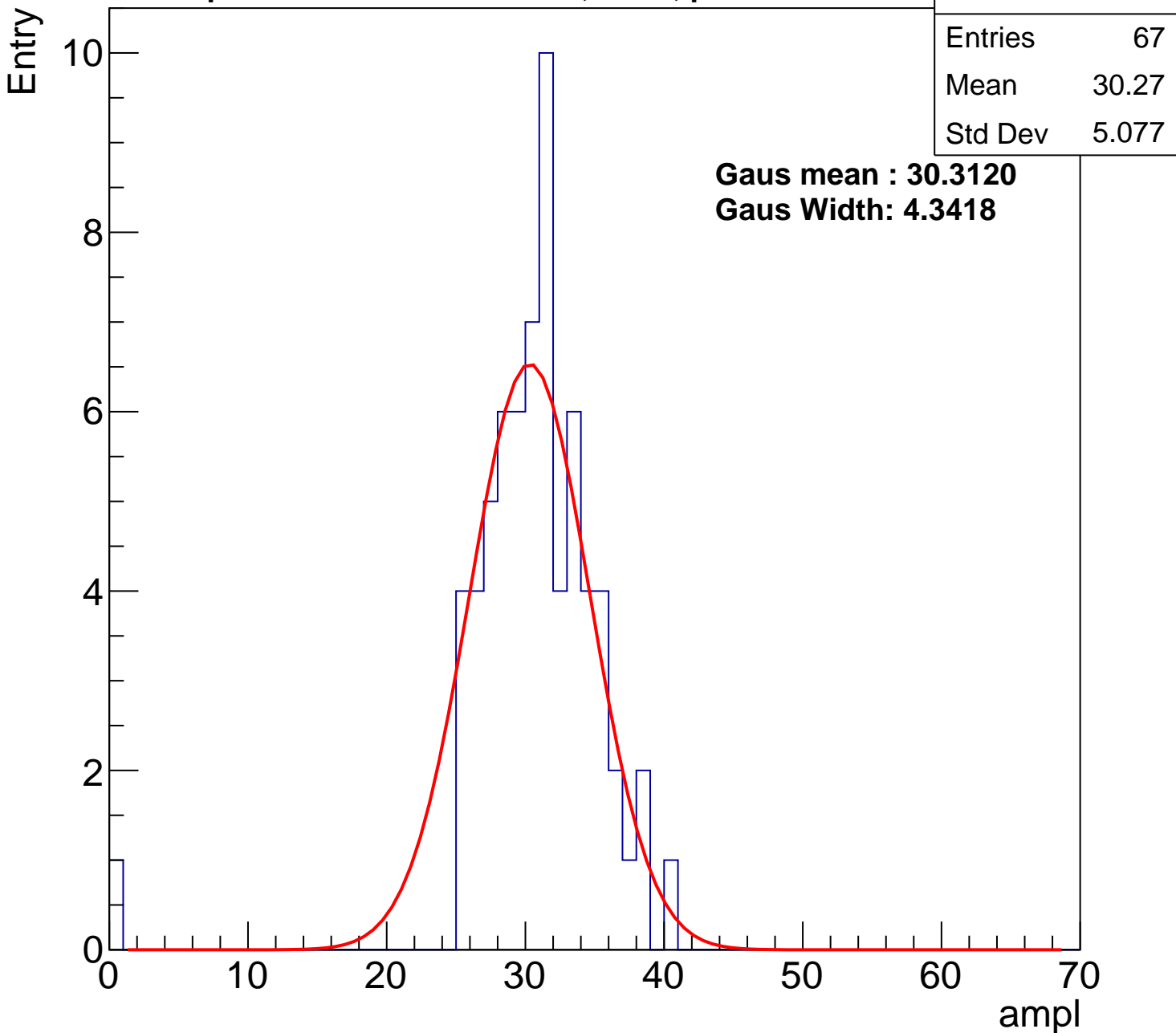
**Gaus Width: 4.3418**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U11-ch79, adc1

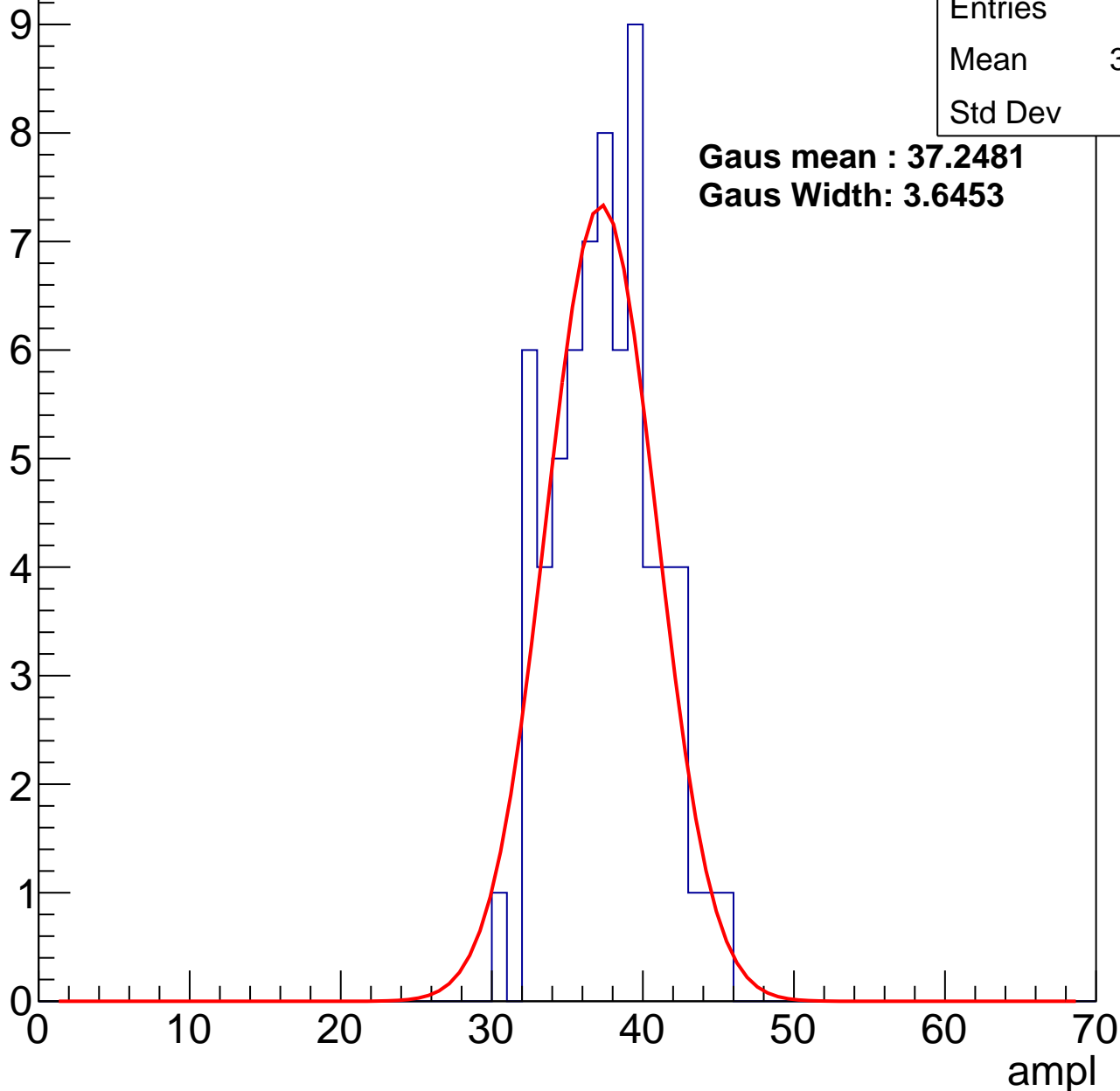
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	37.09
Std Dev	3.3

**Gaus mean : 37.2481**

**Gaus Width: 3.6453**



# B1L103S, U11-ch79, adc2

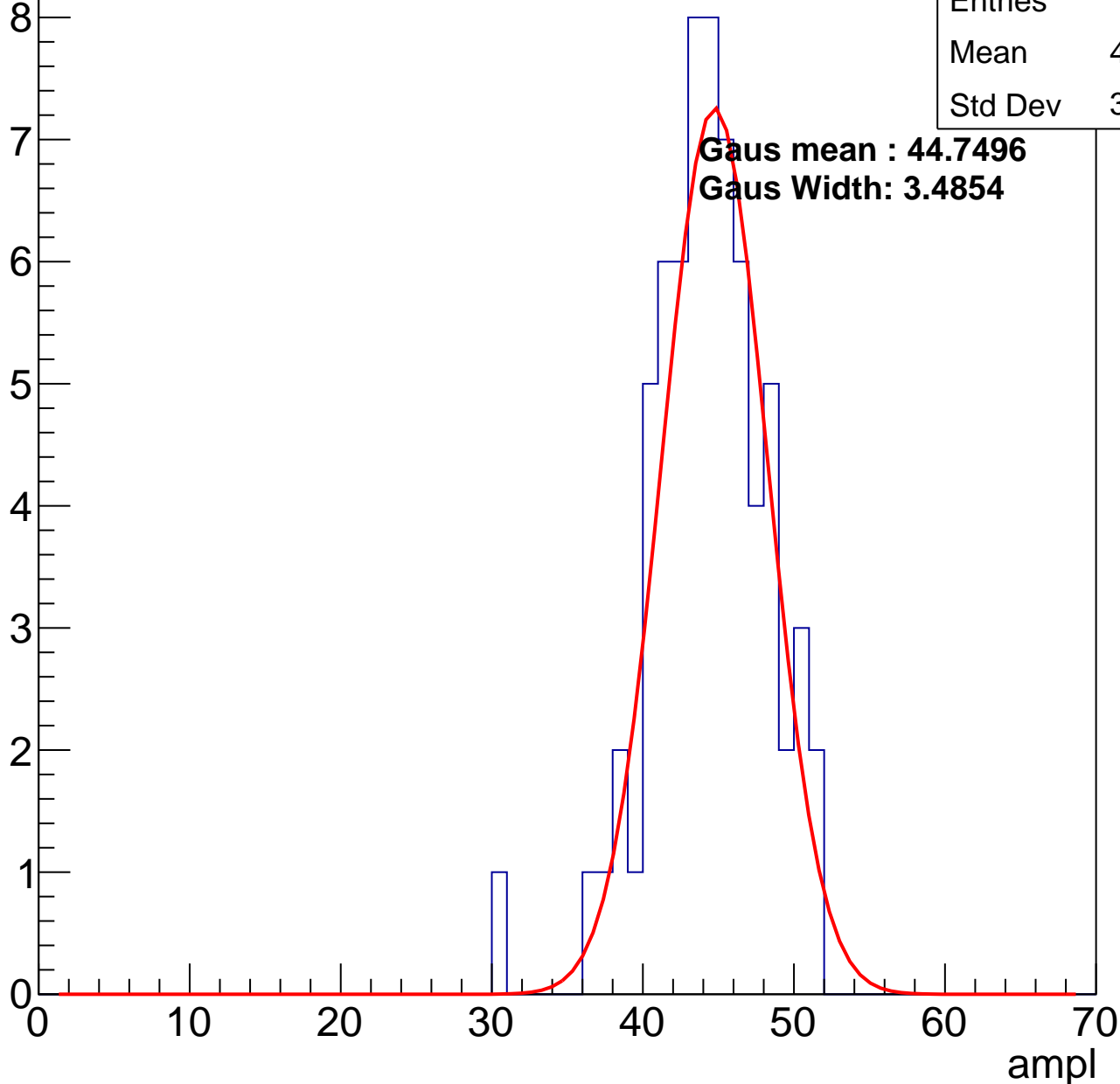
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	68
Mean	43.84
Std Dev	3.783

**Gaus mean : 44.7496**

**Gaus Width: 3.4854**

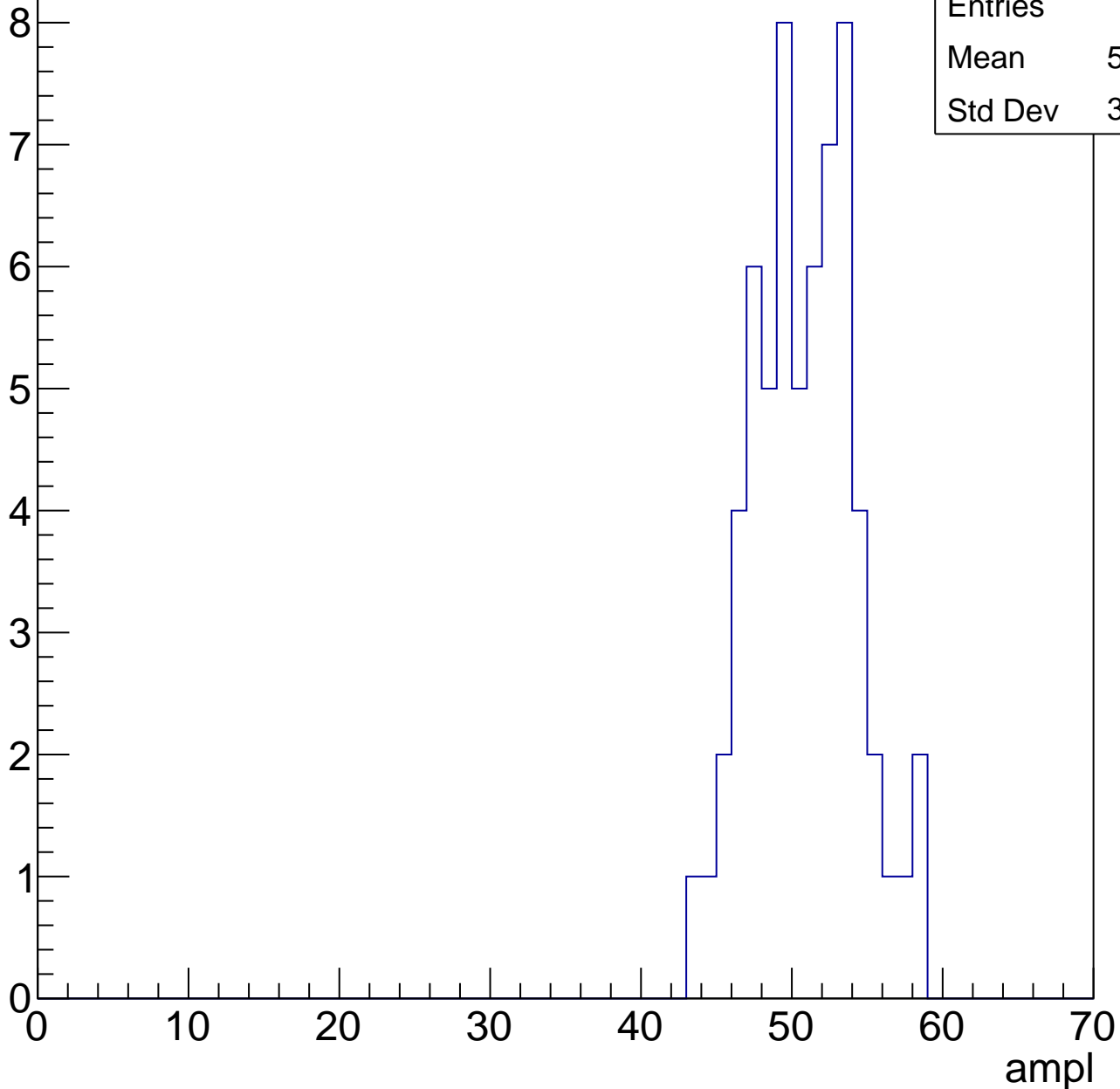


# B1L103S, U11-ch79, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	50.38
Std Dev	3.345

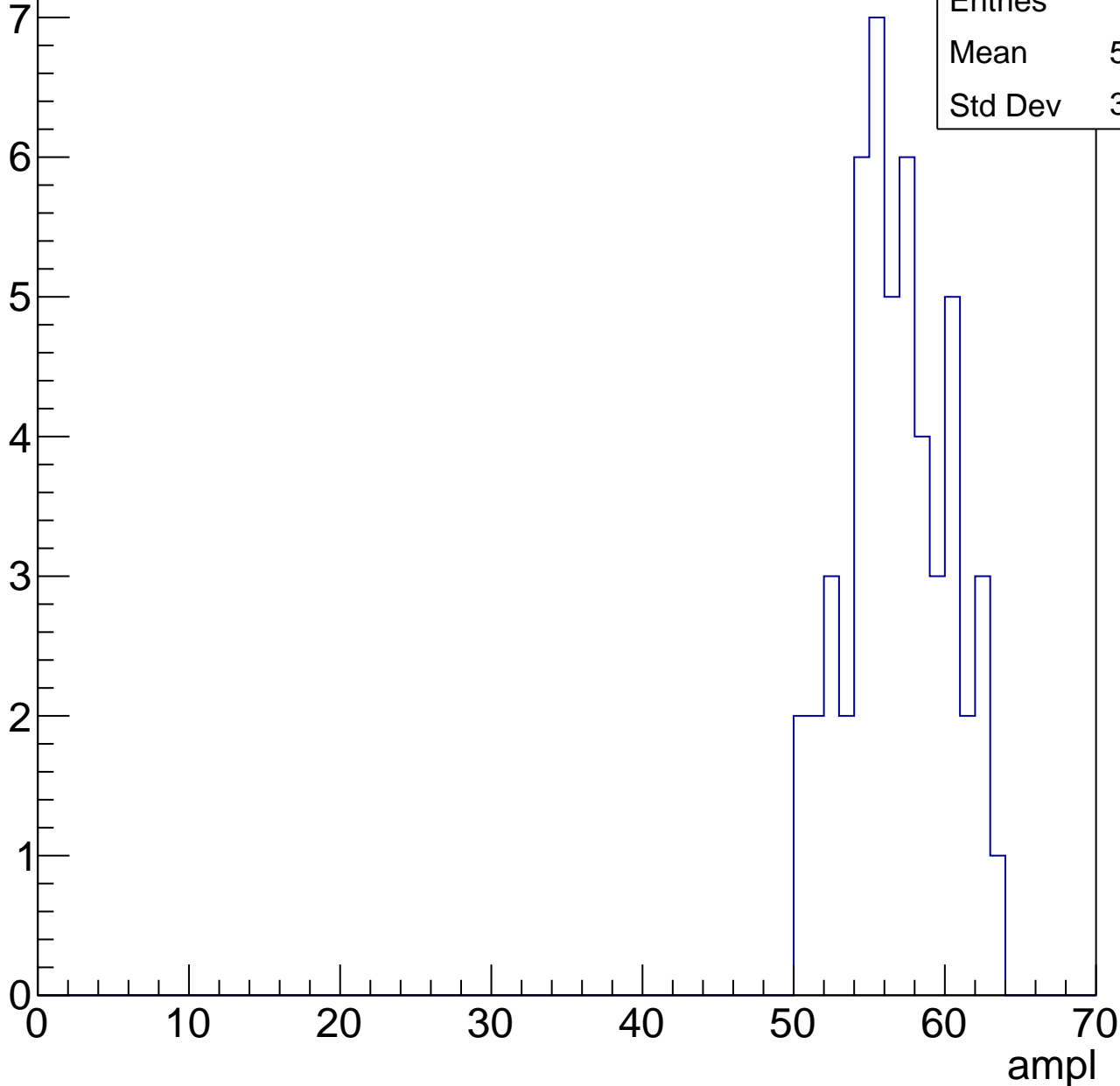


# B1L103S, U11-ch79, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	51
Mean	56.37
Std Dev	3.278

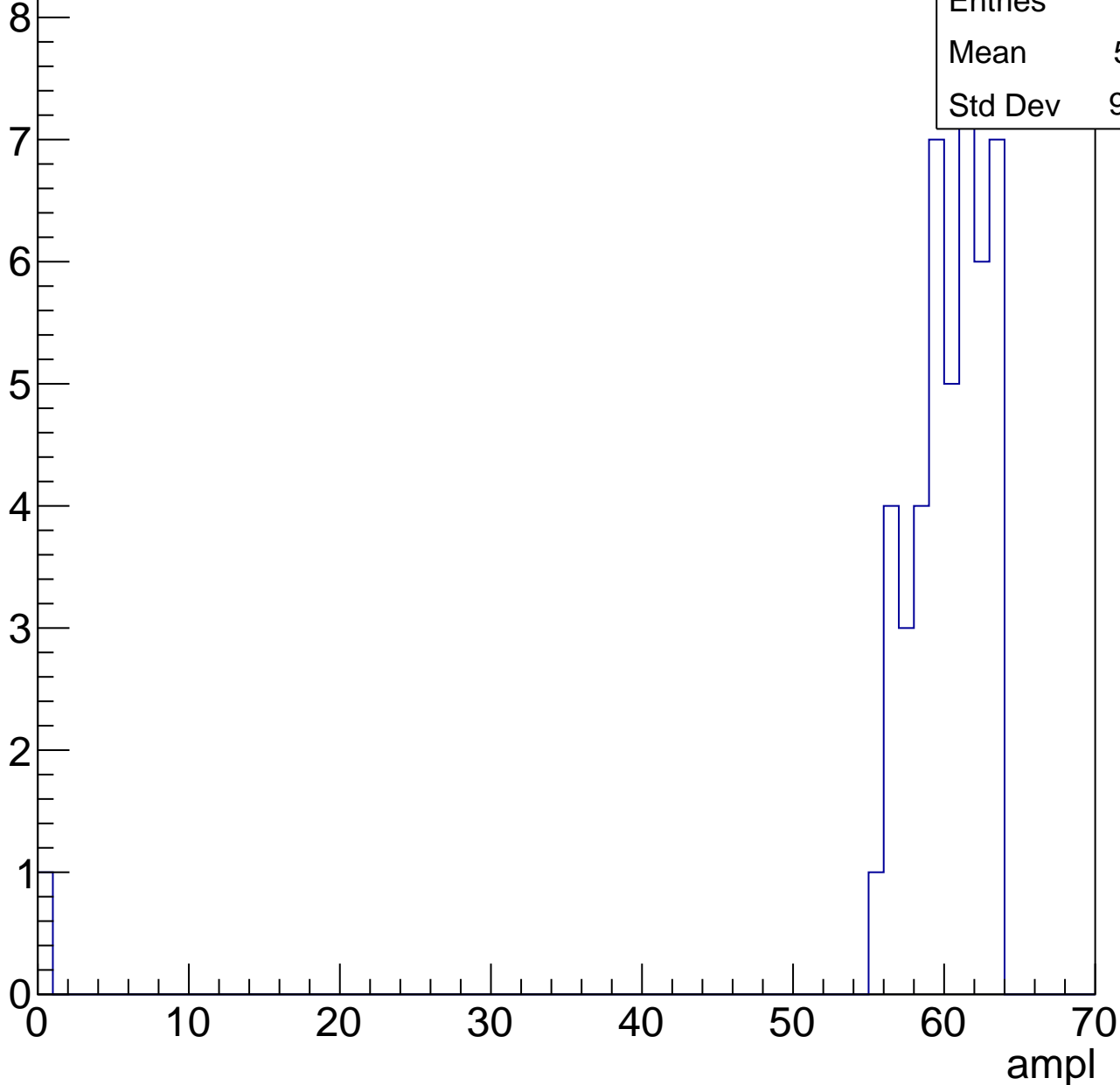


# B1L103S, U11-ch79, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	46
Mean	58.61
Std Dev	9.023



# B1L103S, U11-ch79, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	3
Mean	62.67
Std Dev	0.4714

ampl

0 10 20 30 40 50 60 70



# B1L103S, U11-ch79, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	3
Mean	0
Std Dev	0

# B1L103S, U11-ch80, adc0

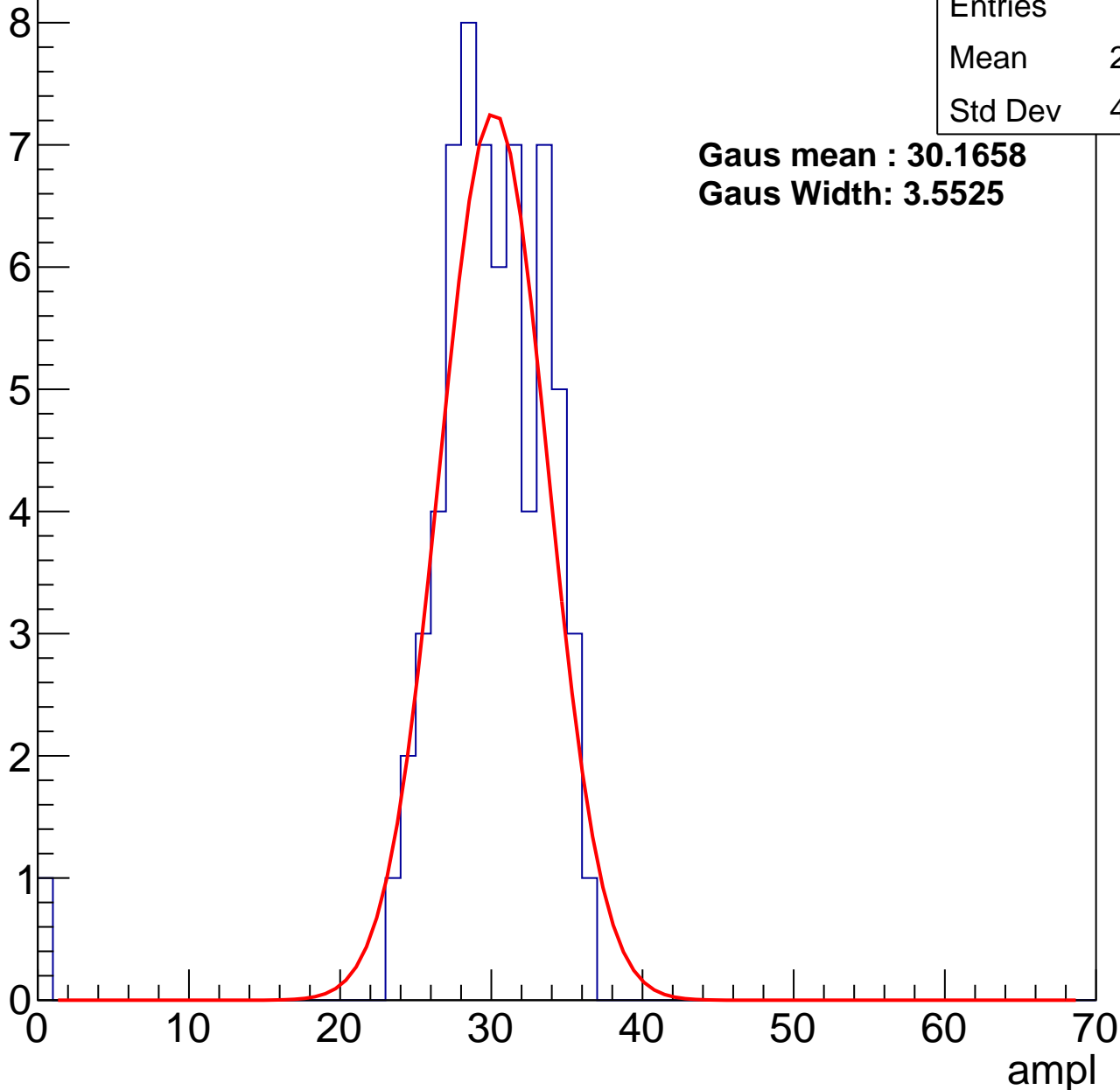
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	29.29
Std Dev	4.776

**Gaus mean : 30.1658**

**Gaus Width: 3.5525**



# B1L103S, U11-ch80, adc1

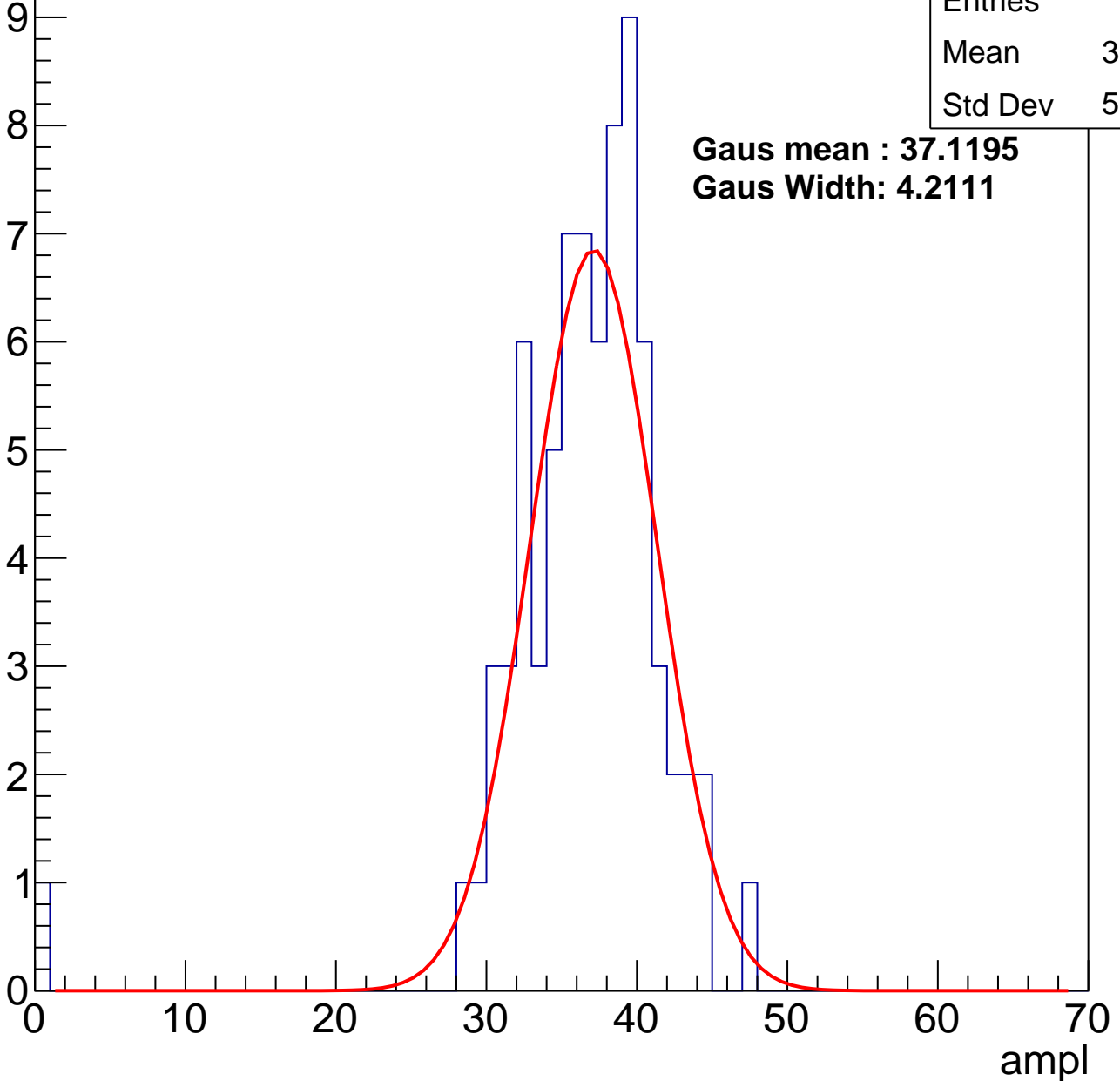
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	76
Mean	36.09
Std Dev	5.678

**Gaus mean : 37.1195**

**Gaus Width: 4.2111**



# B1L103S, U11-ch80, adc2

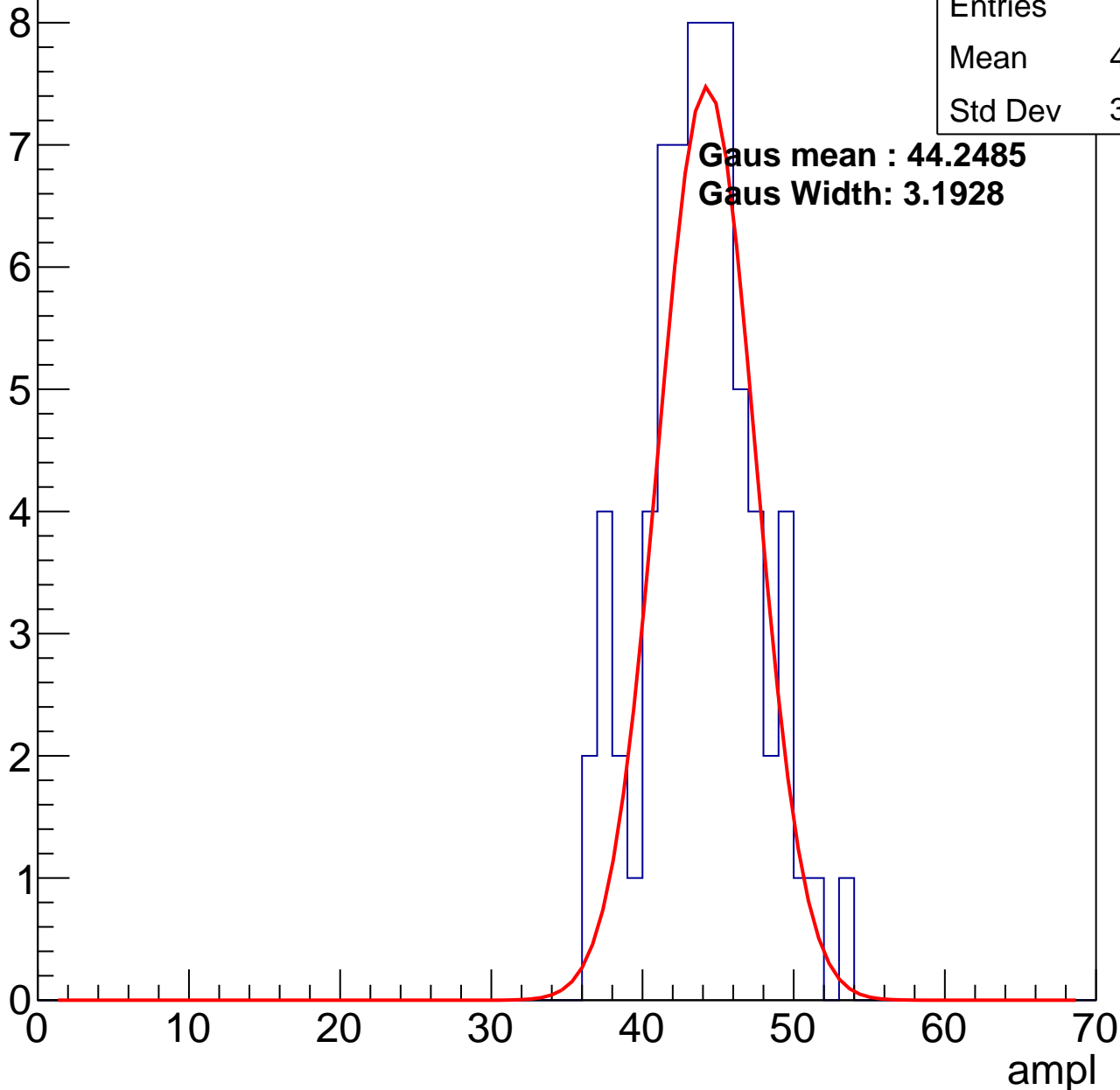
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	69
Mean	43.42
Std Dev	3.657

**Gaus mean : 44.2485**

**Gaus Width: 3.1928**

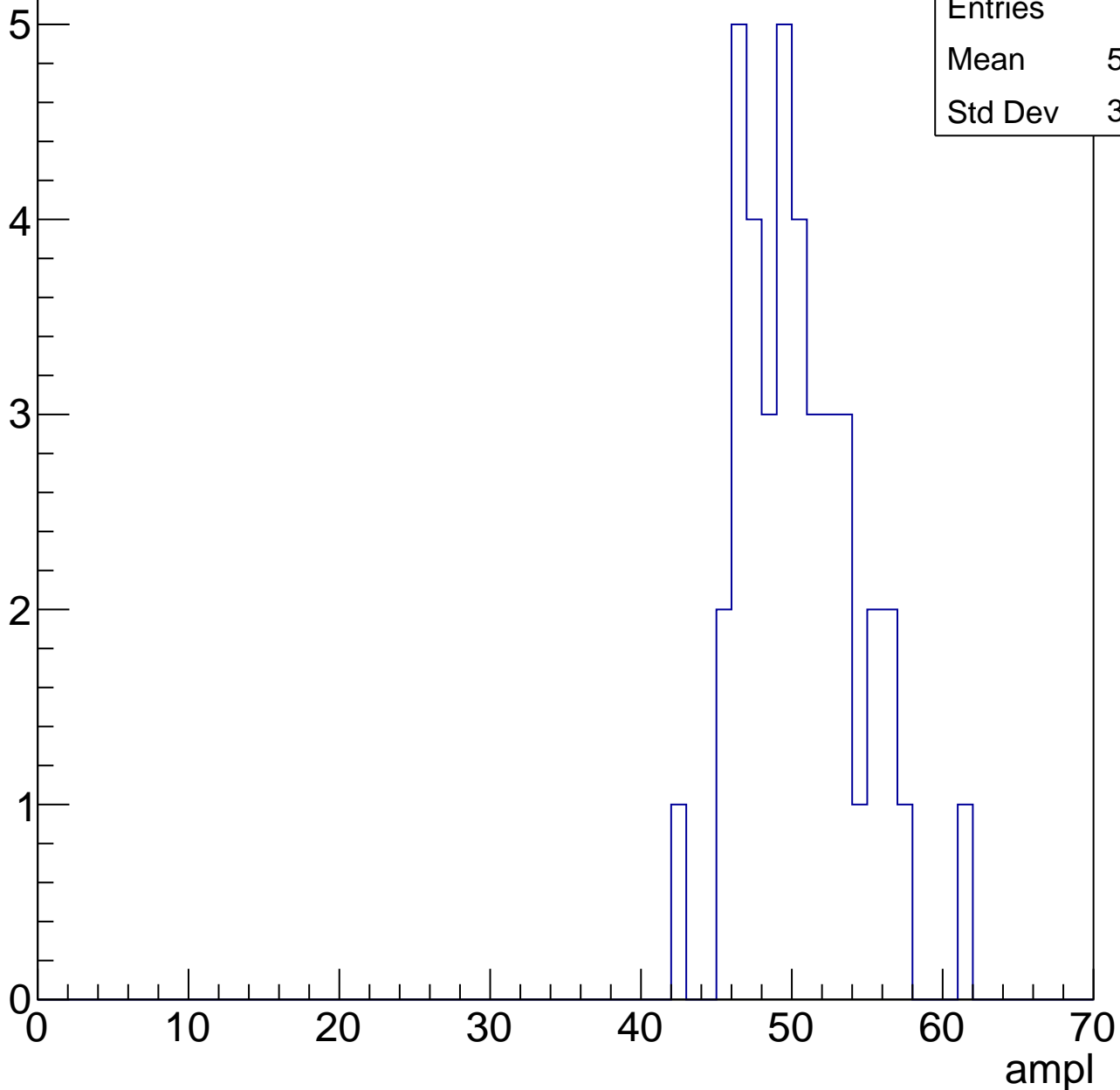


# B1L103S, U11-ch80, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	40
Mean	50.02
Std Dev	3.863

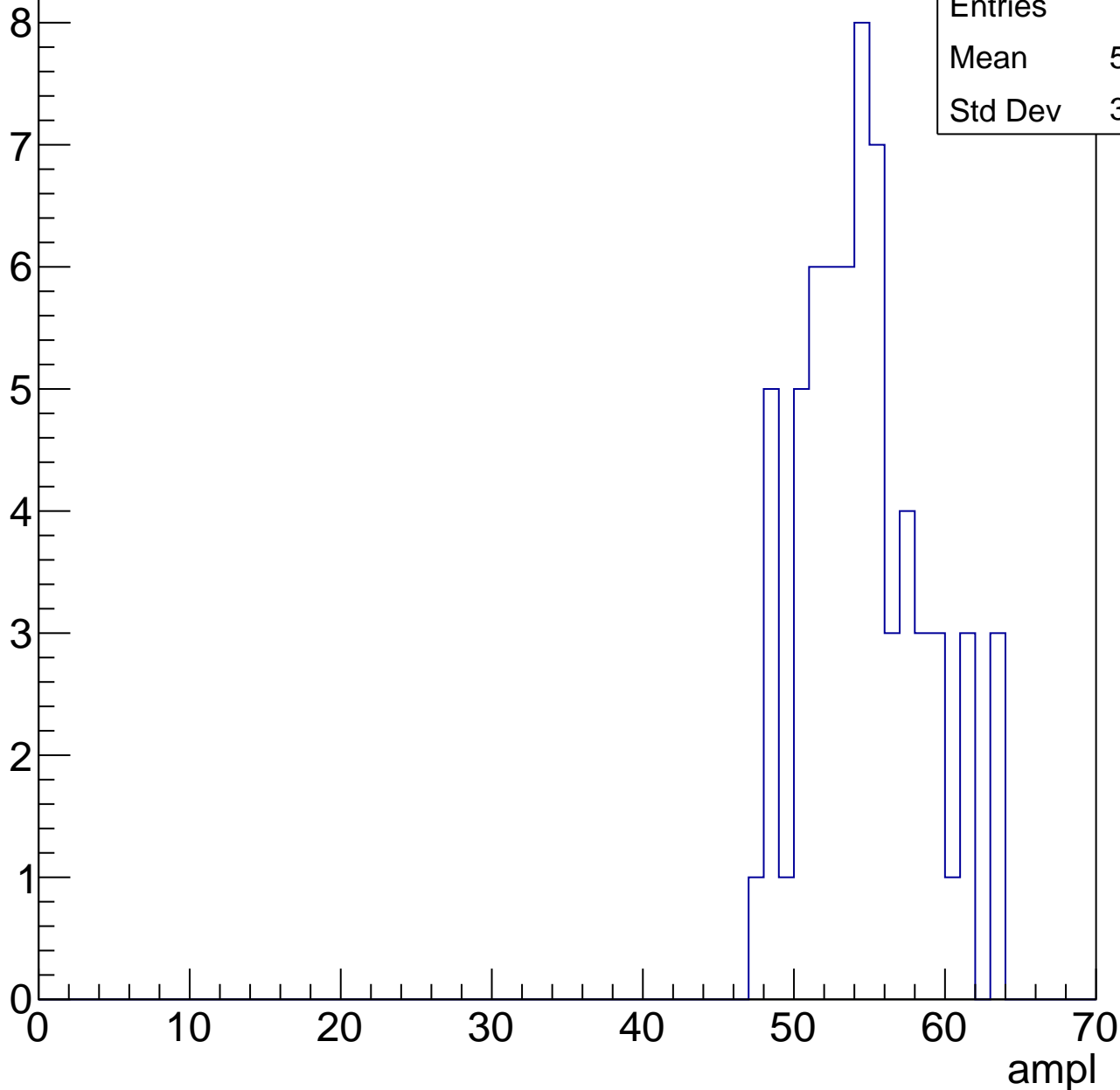


# B1L103S, U11-ch80, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

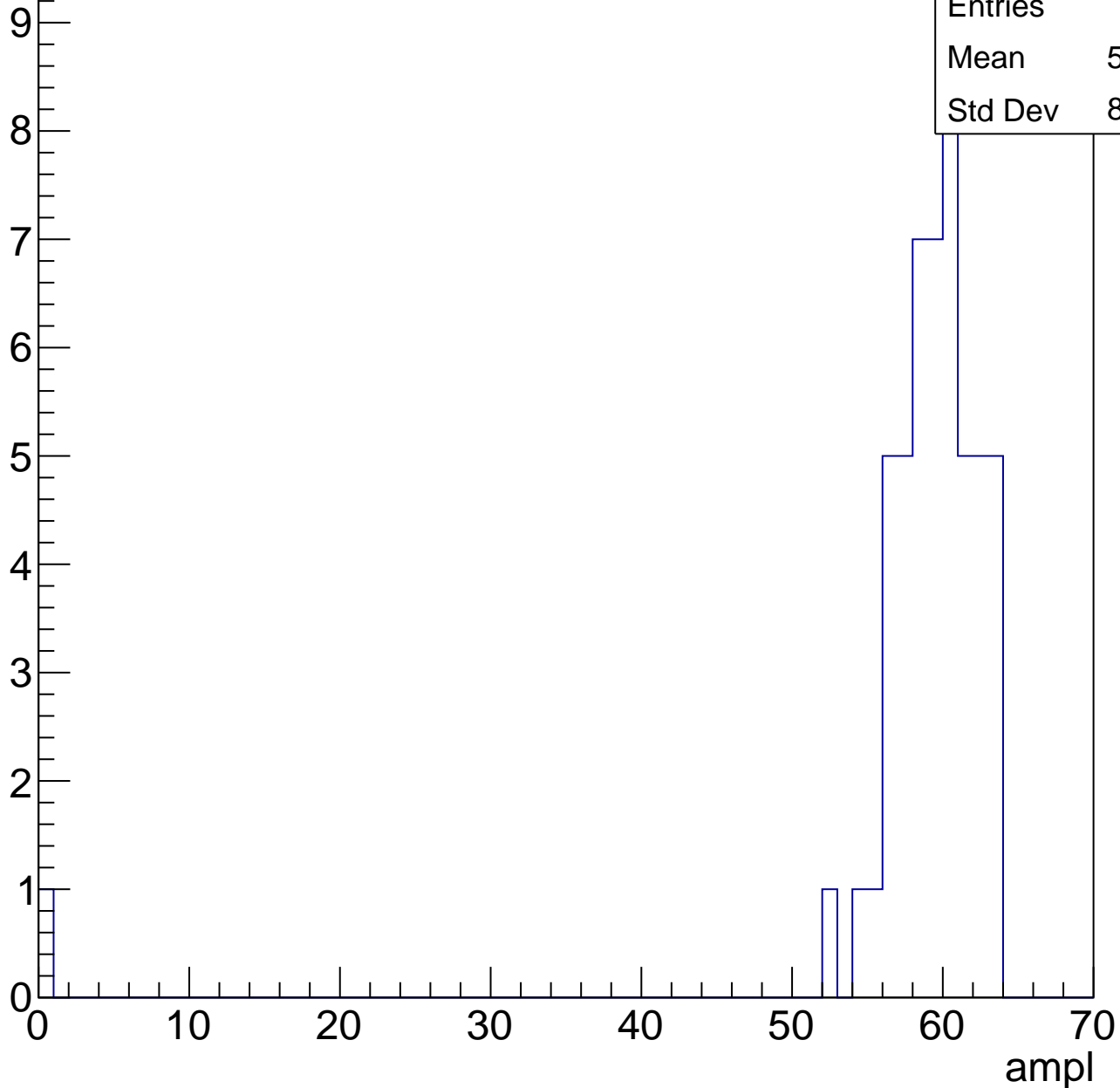
Entries	65
Mean	54.12
Std Dev	3.963



# B1L103S, U11-ch80, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

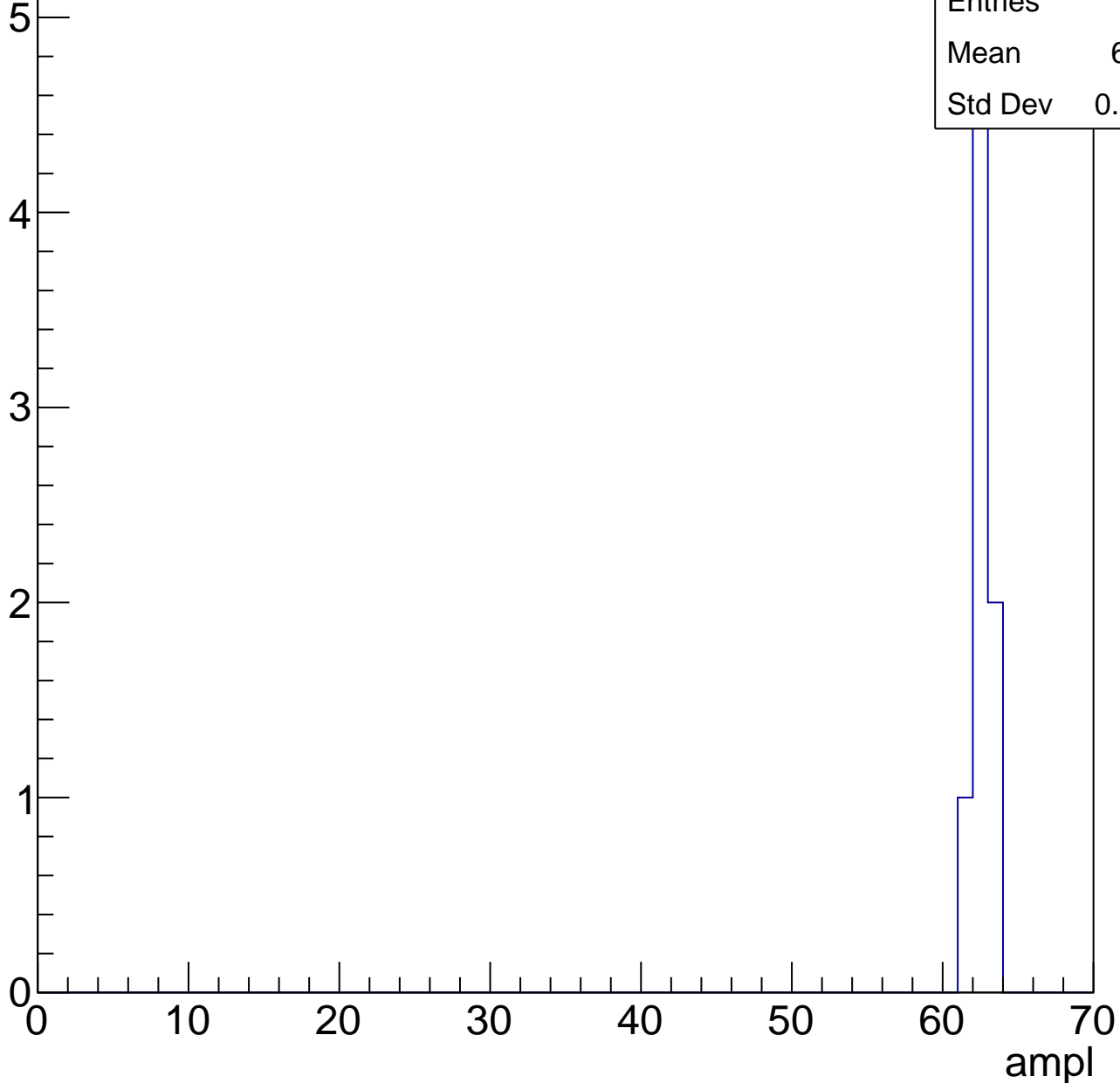


# B1L103S, U11-ch80, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	8
Mean	62.12
Std Dev	0.5995





# B1L103S, U11-ch80, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U11-ch81, adc0

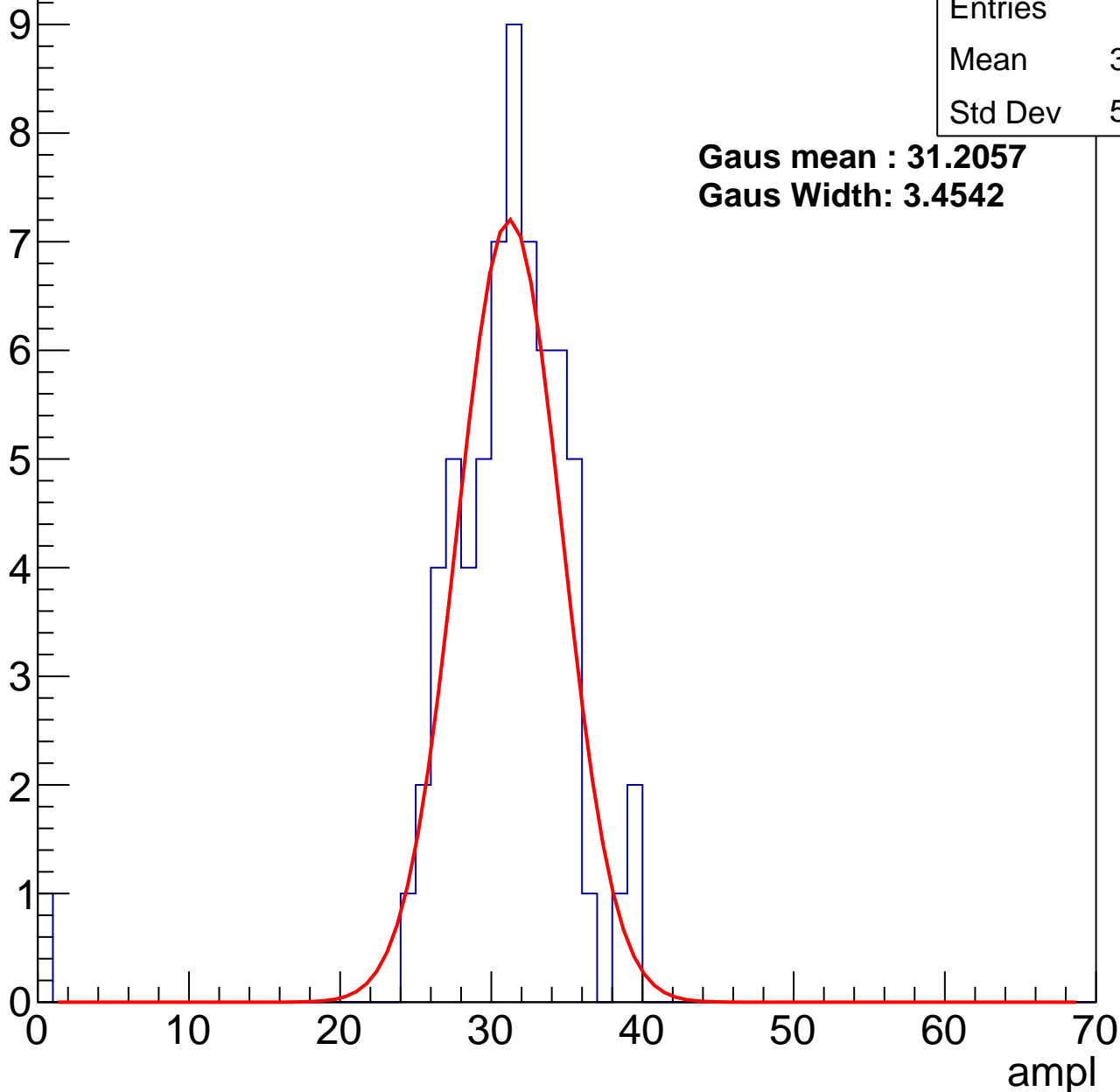
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	30.48
Std Dev	5.037

**Gaus mean : 31.2057**

**Gaus Width: 3.4542**



# B1L103S, U11-ch81, adc1

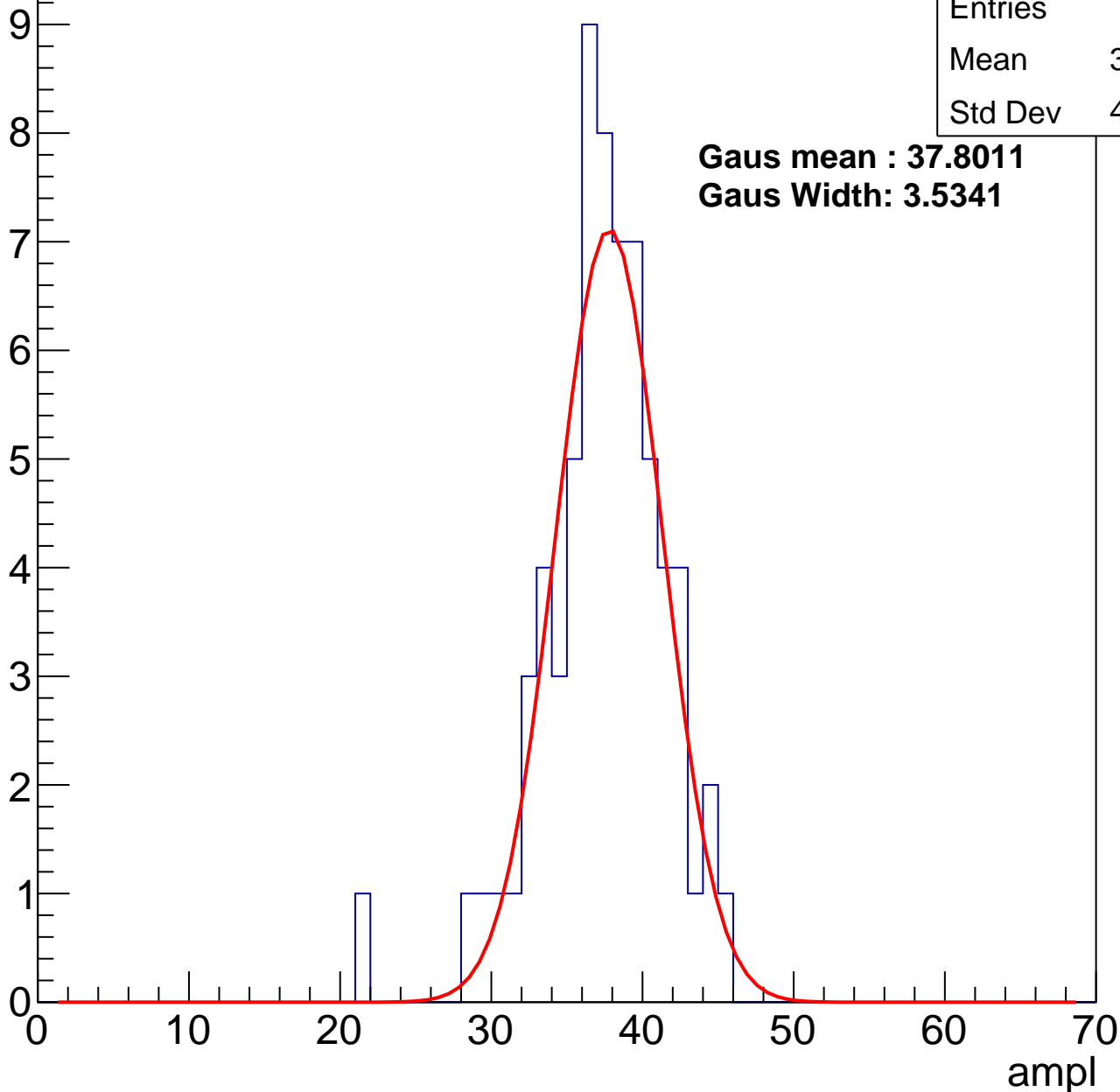
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	68
Mean	36.93
Std Dev	4.063

**Gaus mean : 37.8011**

**Gaus Width: 3.5341**



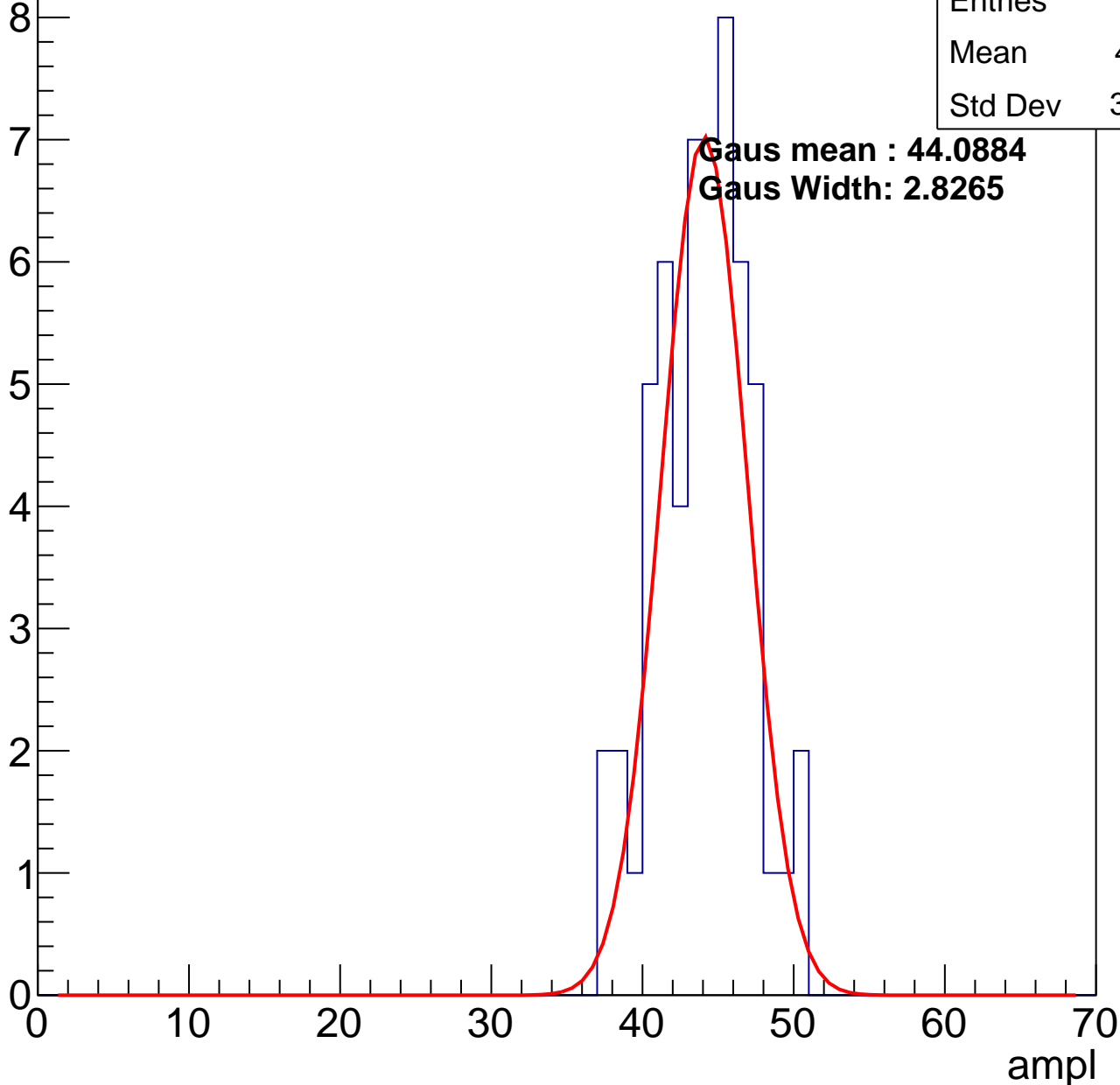
# B1L103S, U11-ch81, adc2

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	57
Mean	43.51
Std Dev	3.044

**Gaus mean : 44.0884**  
**Gaus Width: 2.8265**

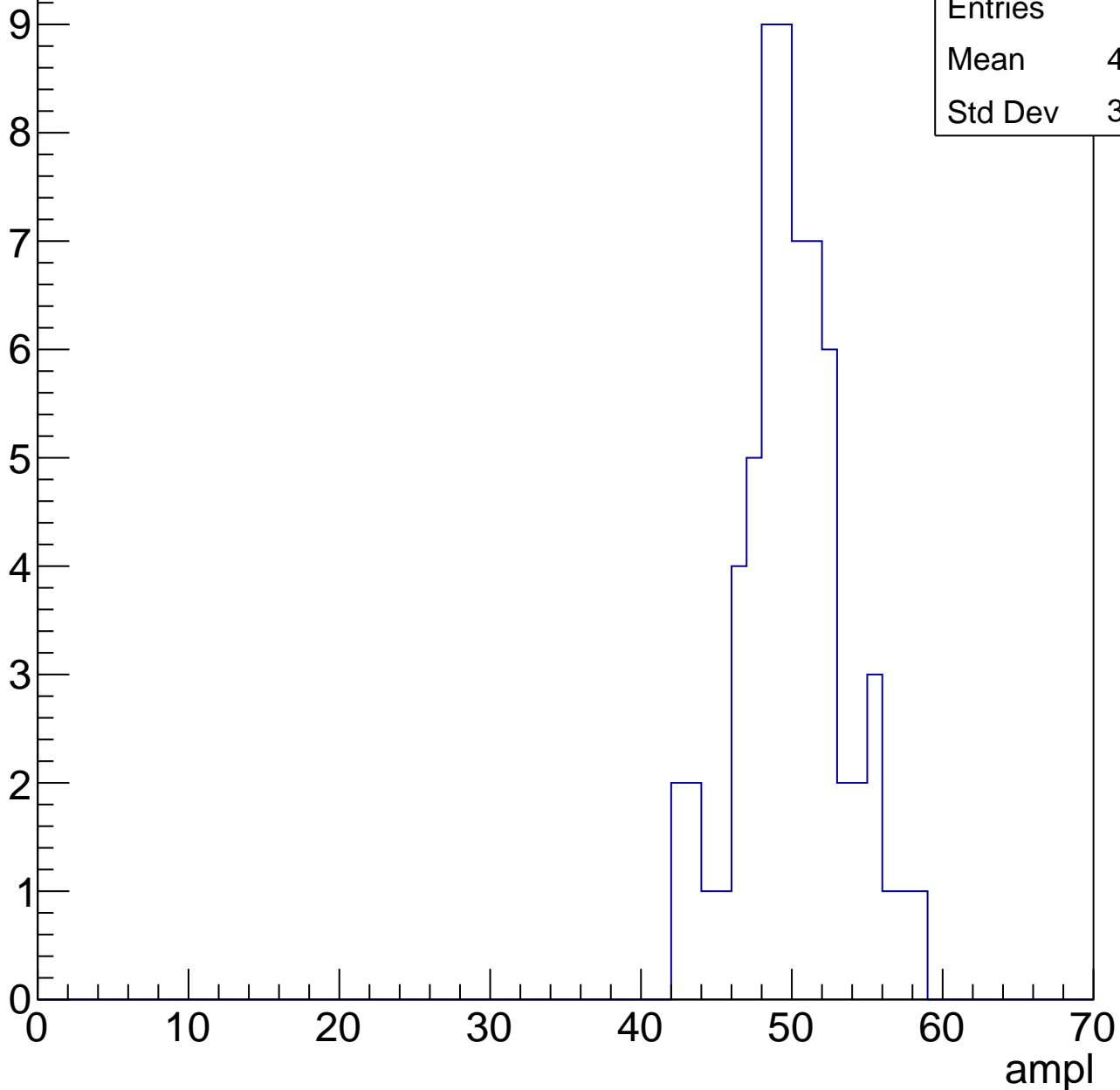


# B1L103S, U11-ch81, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

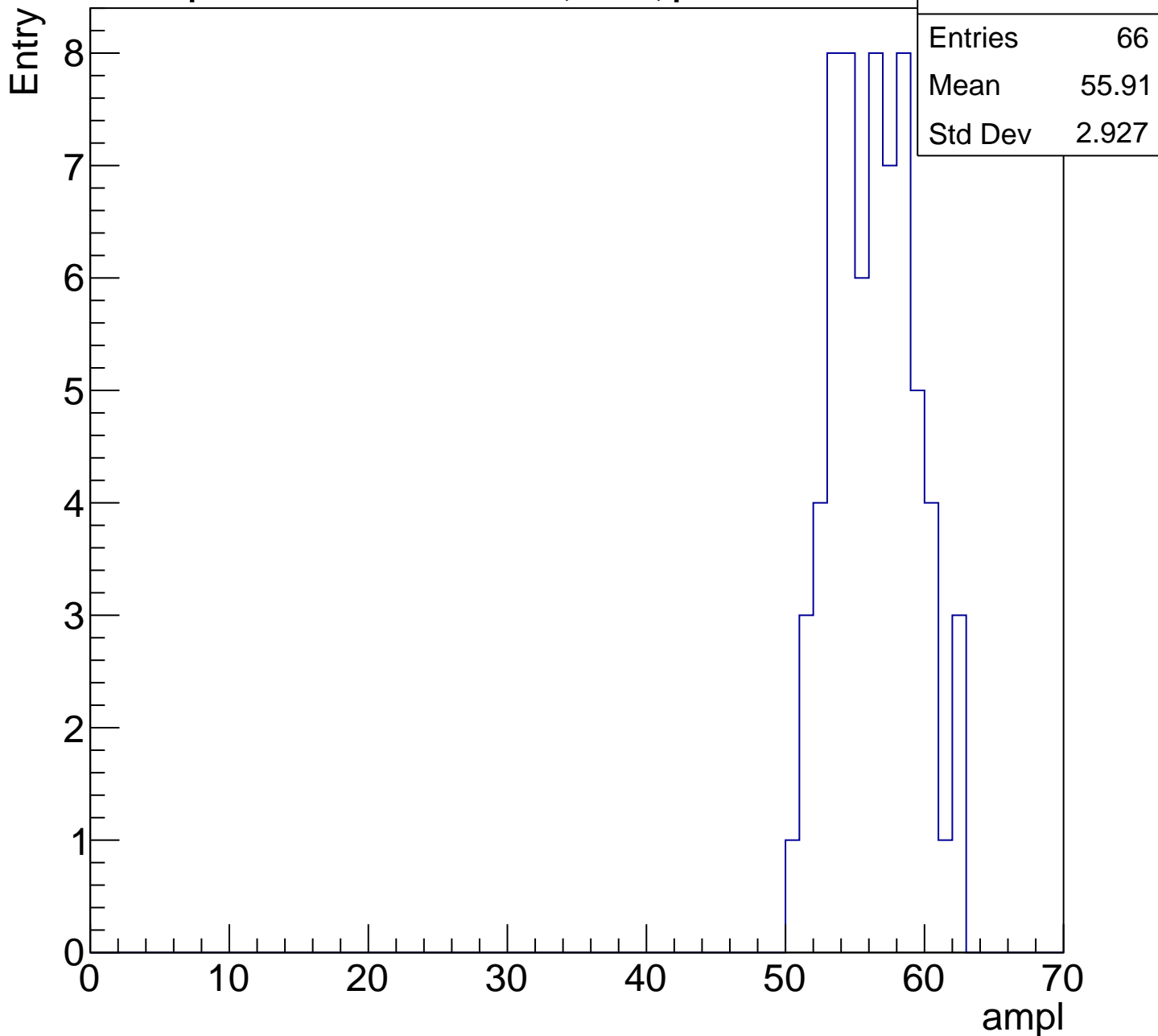
Entry

Entries	63
Mean	49.52
Std Dev	3.408



# B1L103S, U11-ch81, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

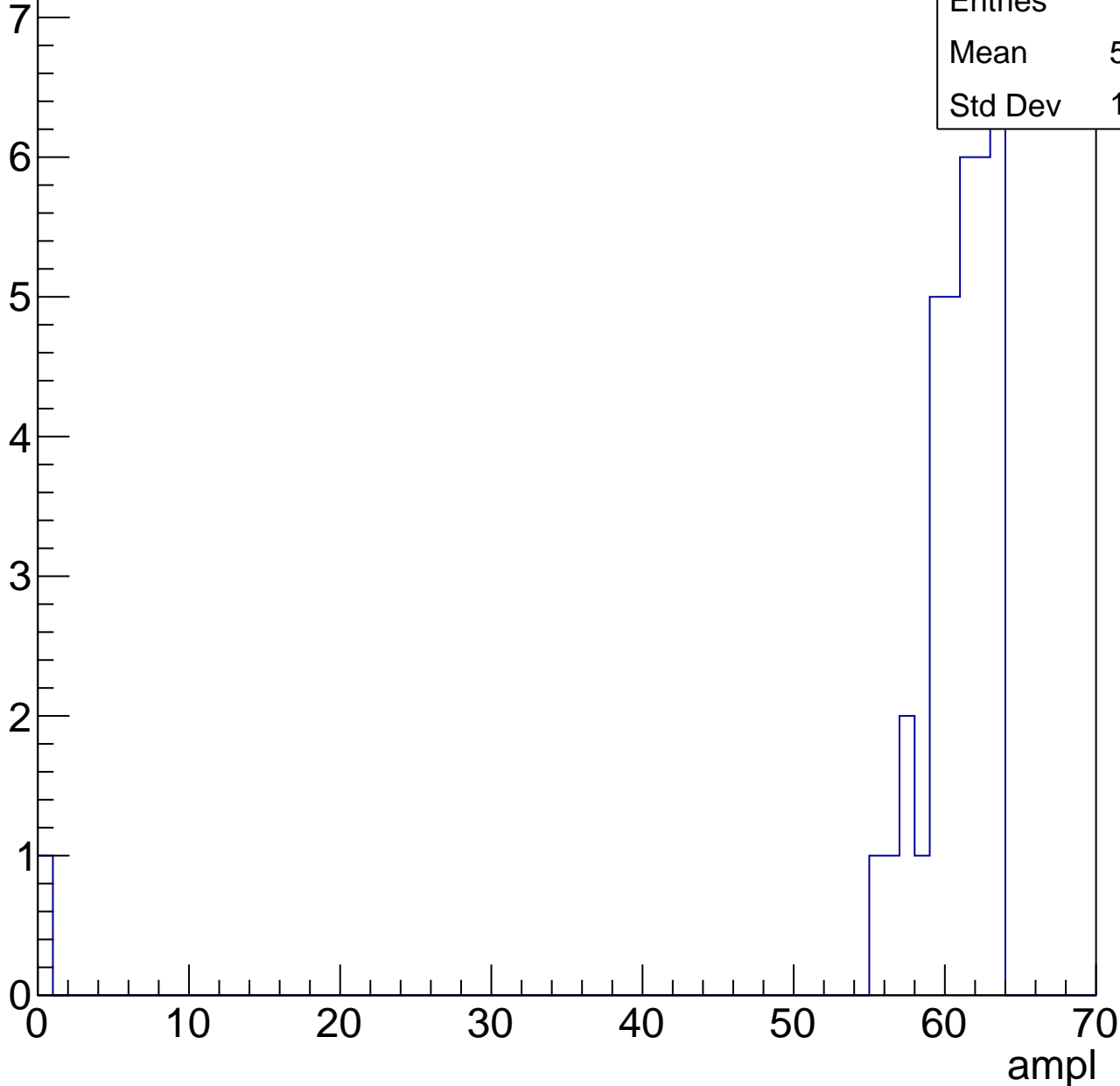


# B1L103S, U11-ch81, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

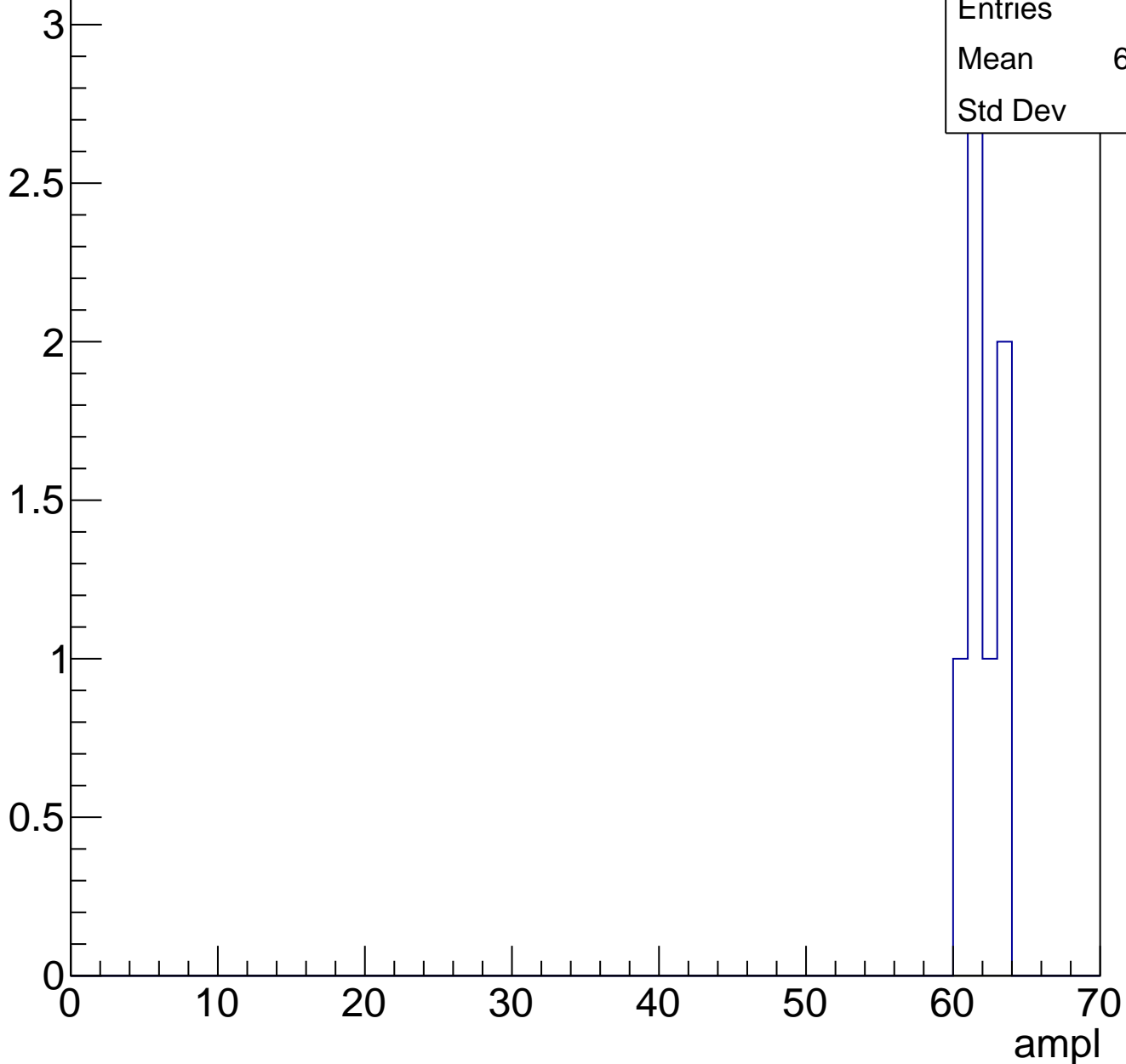
Entries	35
Mean	58.77
Std Dev	10.29



# B1L103S, U11-ch81, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U11-ch81, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U11-ch82, adc0

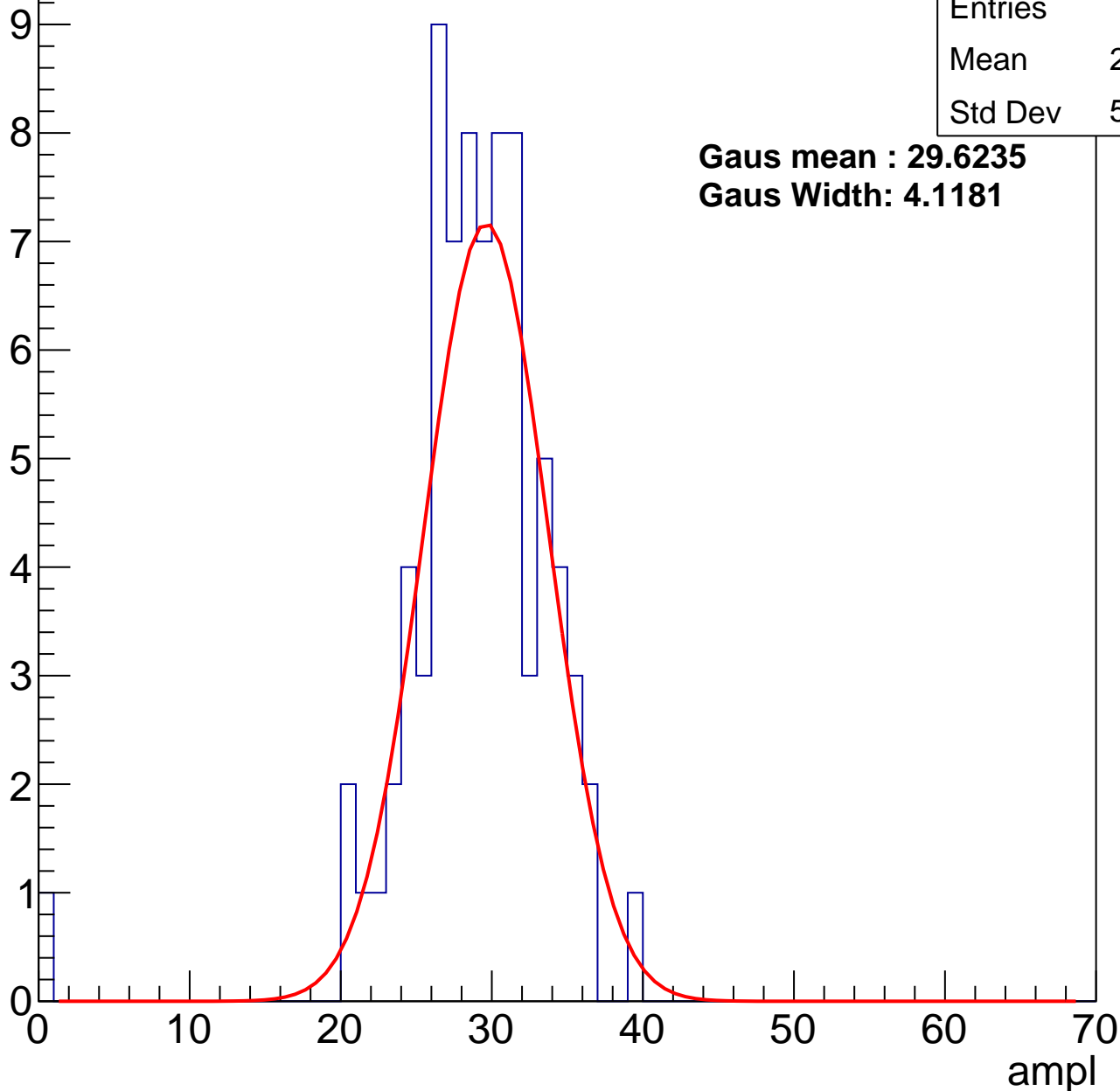
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	79
Mean	28.49
Std Dev	5.014

**Gaus mean : 29.6235**

**Gaus Width: 4.1181**



# B1L103S, U11-ch82, adc1

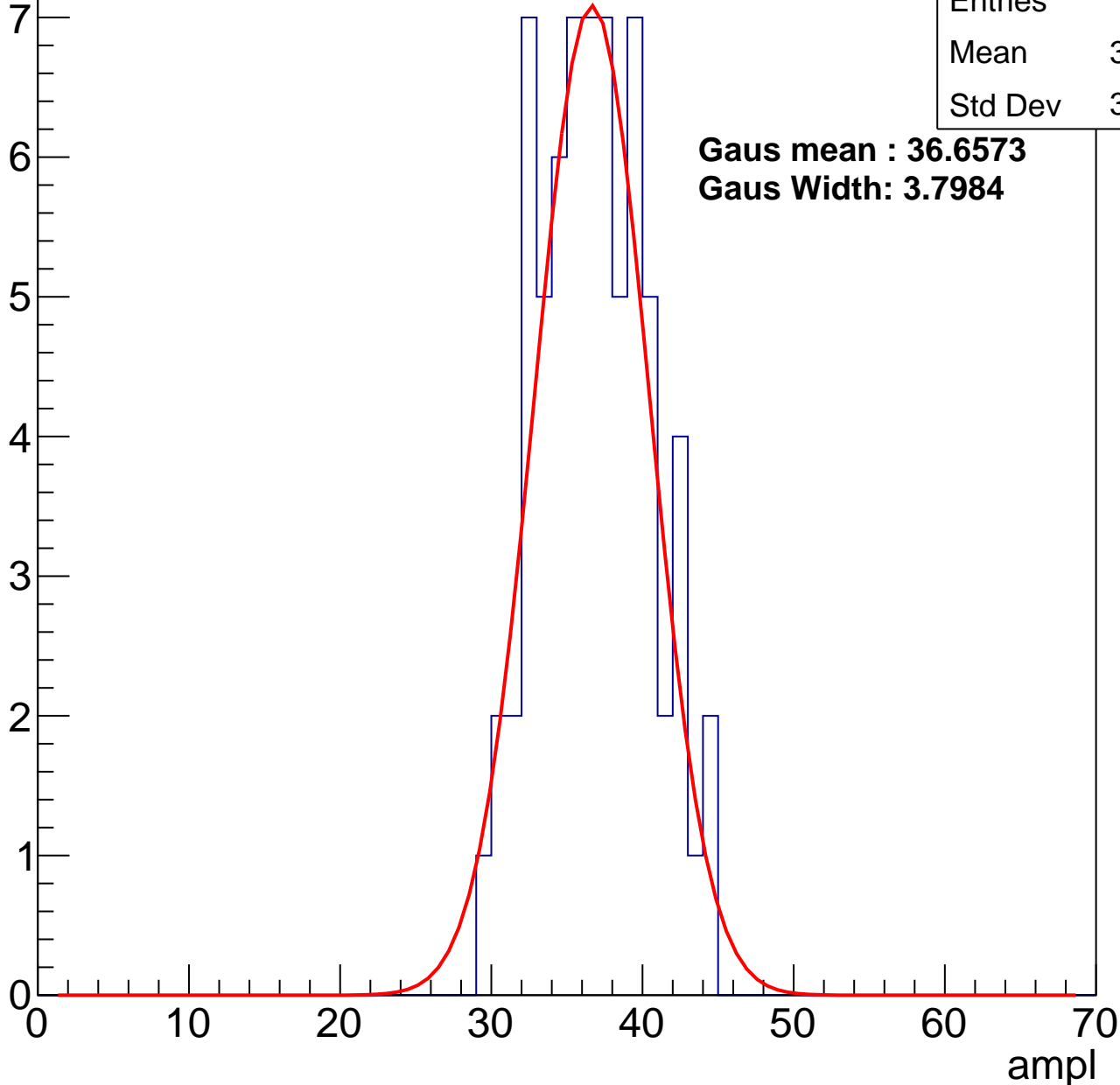
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	70
Mean	36.34
Std Dev	3.569

**Gaus mean : 36.6573**

**Gaus Width: 3.7984**



# B1L103S, U11-ch82, adc2

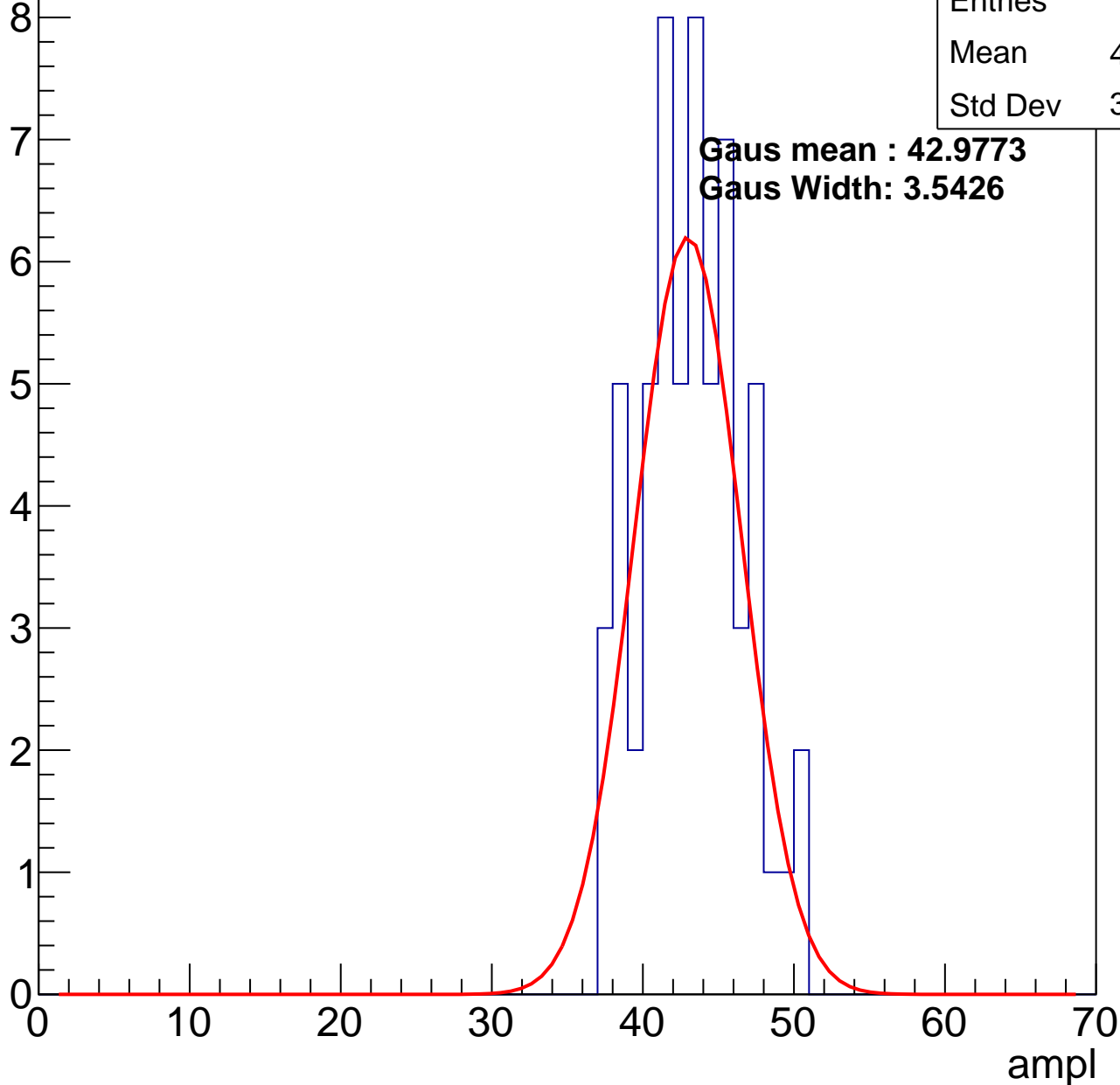
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	60
Mean	42.77
Std Dev	3.273

**Gaus mean : 42.9773**

**Gaus Width: 3.5426**

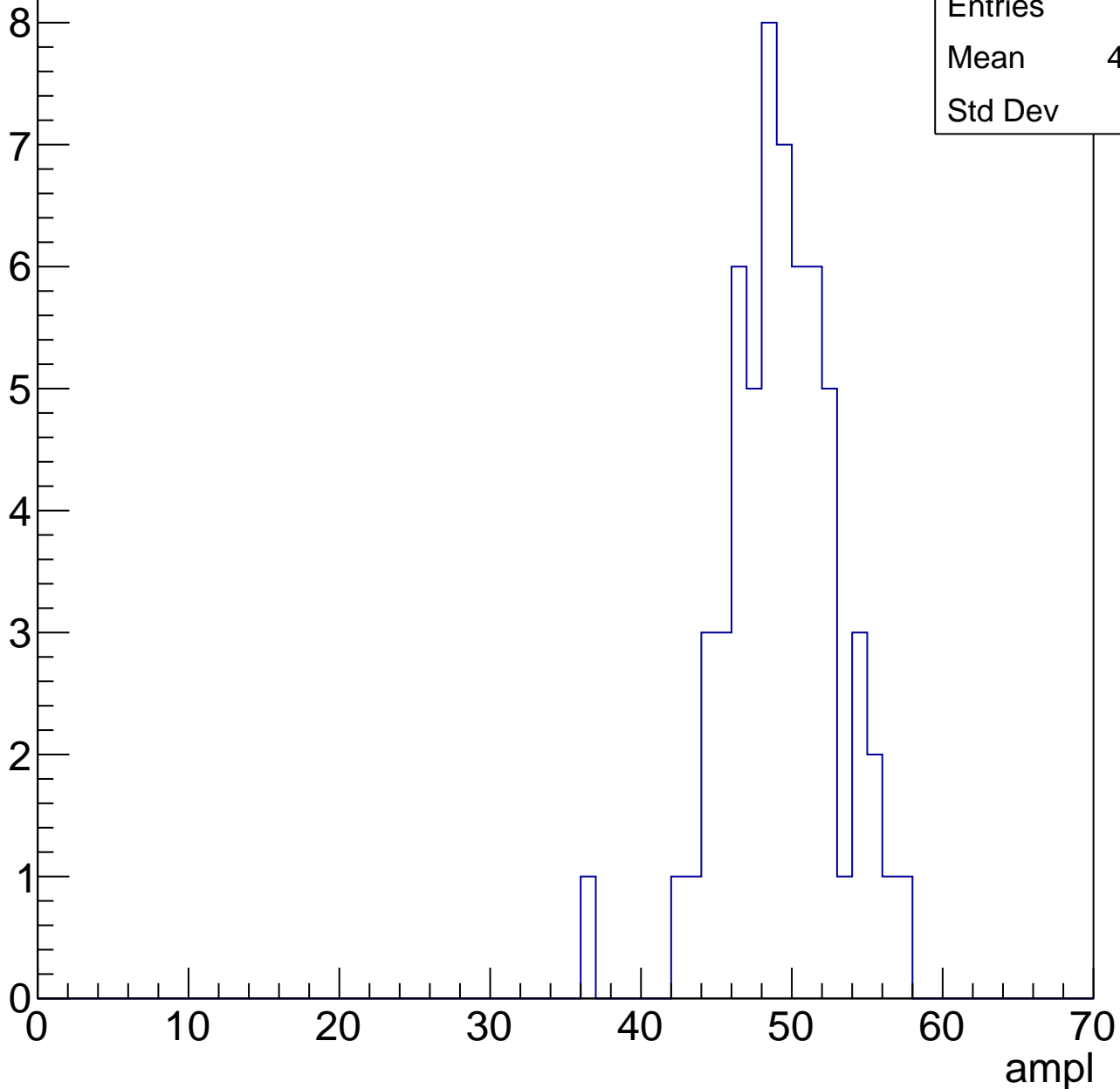


# B1L103S, U11-ch82, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

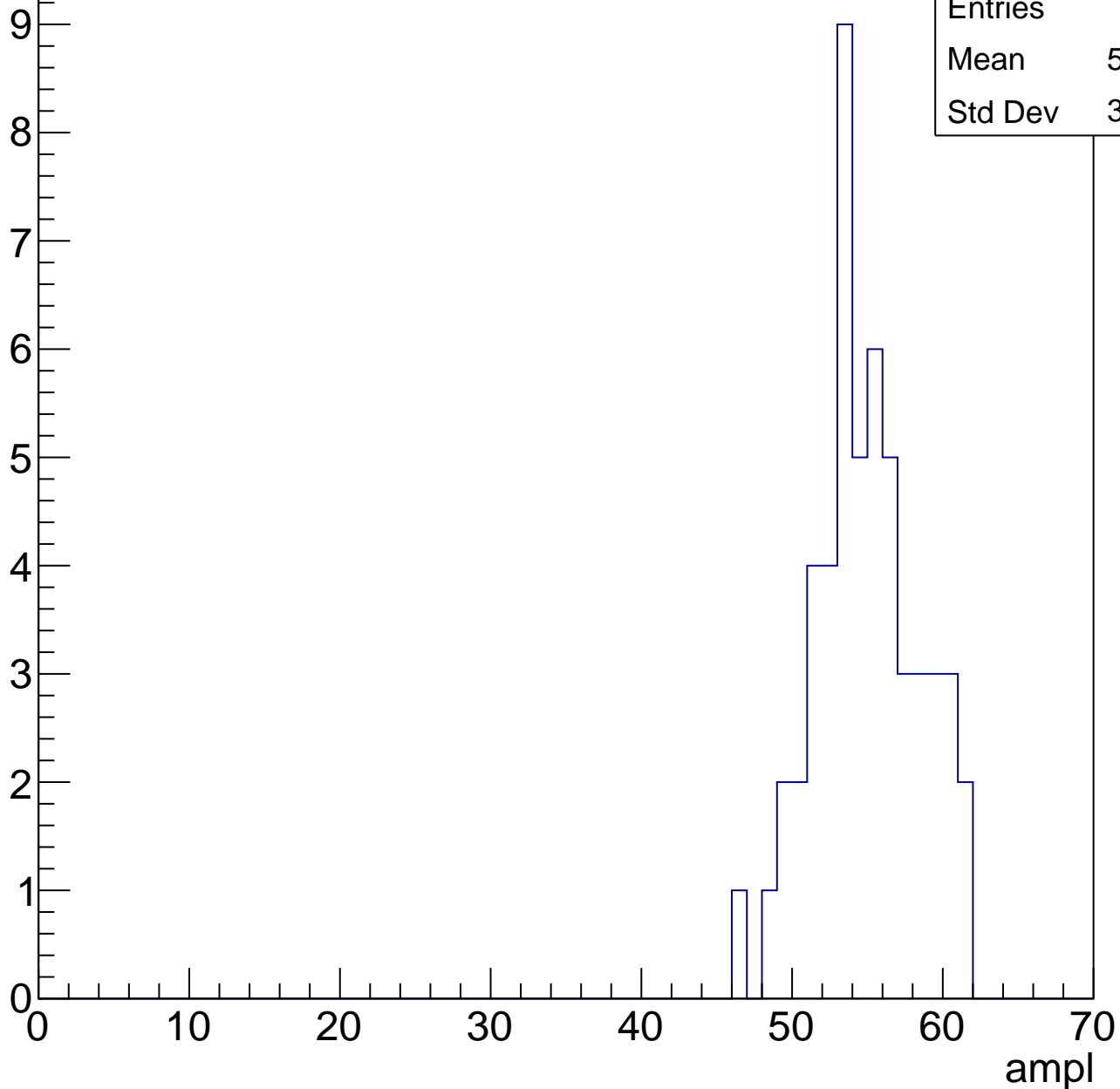
Entries	60
Mean	48.83
Std Dev	3.67



# B1L103S, U11-ch82, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	53
Mean	54.43
Std Dev	3.406

# B1L103S, U11-ch82, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

7

6

5

4

3

2

1

0

Entries	51
Mean	58.92
Std Dev	2.619

ampl

0

10

20

30

40

50

60

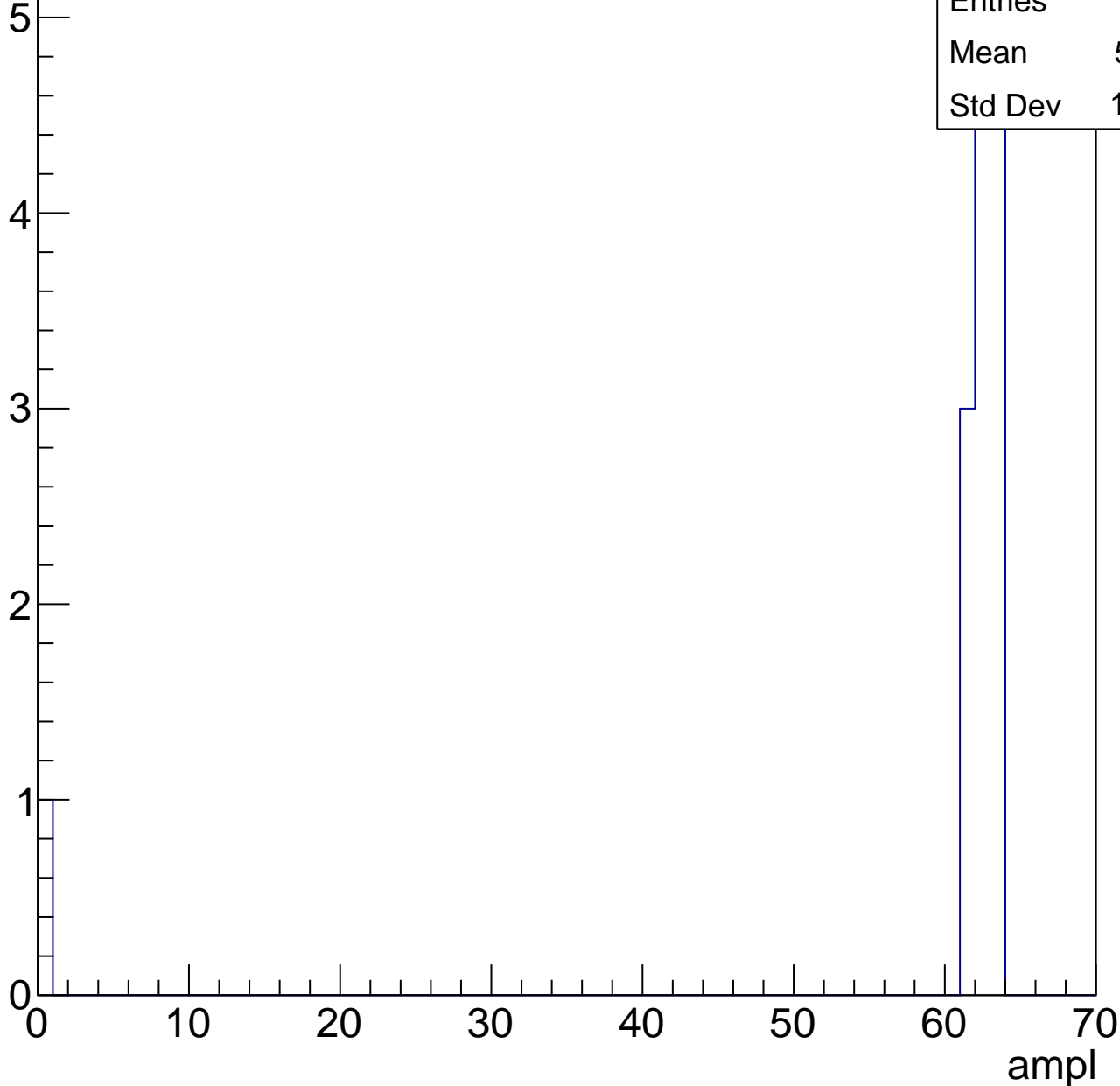
70

# B1L103S, U11-ch82, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	14
Mean	57.71
Std Dev	16.02





# B1L103S, U11-ch82, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L103S, U11-ch83, adc0

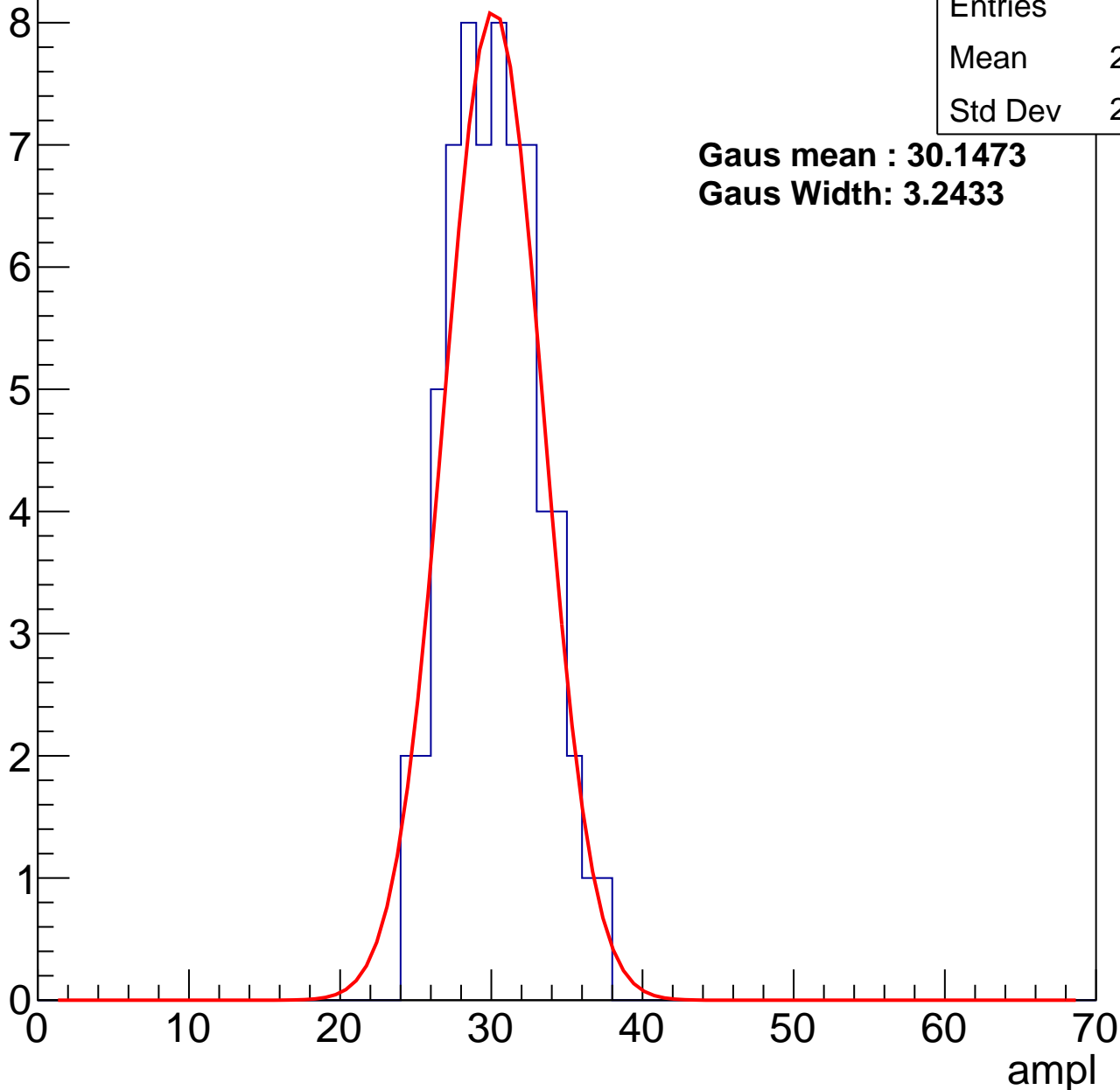
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	29.78
Std Dev	2.964

**Gaus mean : 30.1473**

**Gaus Width: 3.2433**



# B1L103S, U11-ch83, adc1

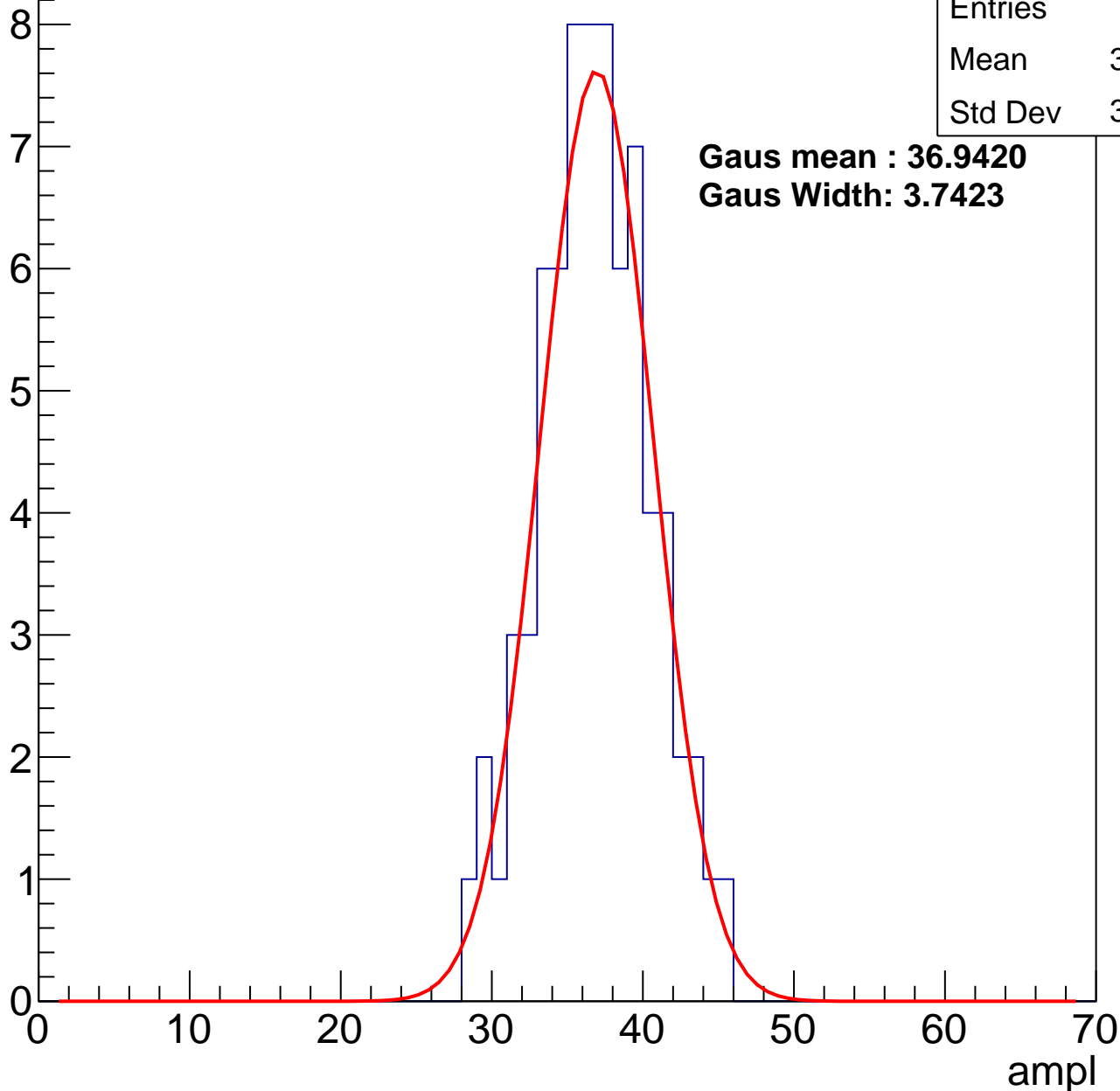
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	73
Mean	36.37
Std Dev	3.647

**Gaus mean : 36.9420**

**Gaus Width: 3.7423**



# B1L103S, U11-ch83, adc2

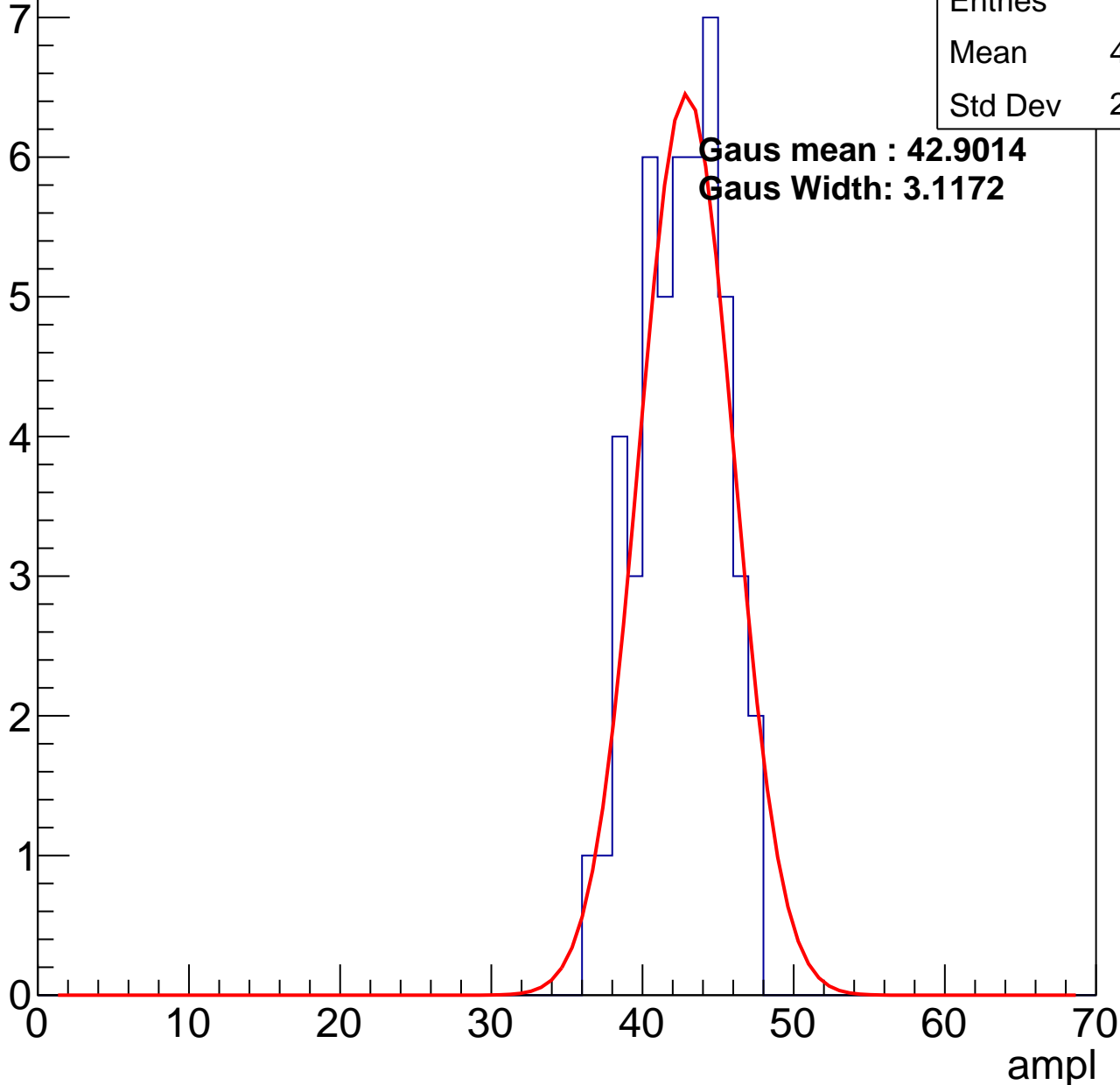
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	49
Mean	42.08
Std Dev	2.702

**Gaus mean : 42.9014**

**Gaus Width: 3.1172**



# B1L103S, U11-ch83, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	83
Mean	49.2
Std Dev	3.456

Entry

10

8

6

4

2

0

0

10

20

30

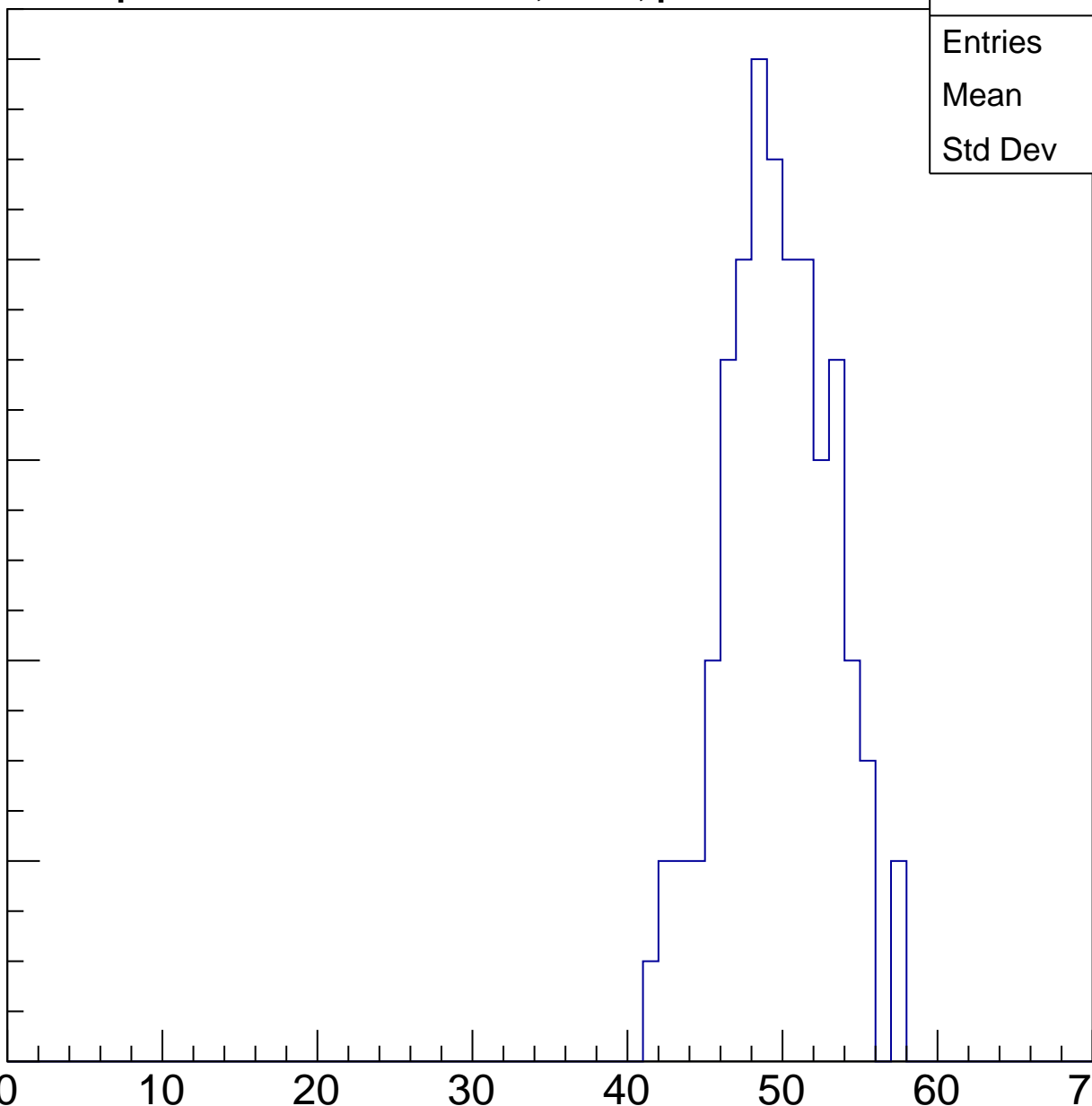
40

50

60

70

ampl



# B1L103S, U11-ch83, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

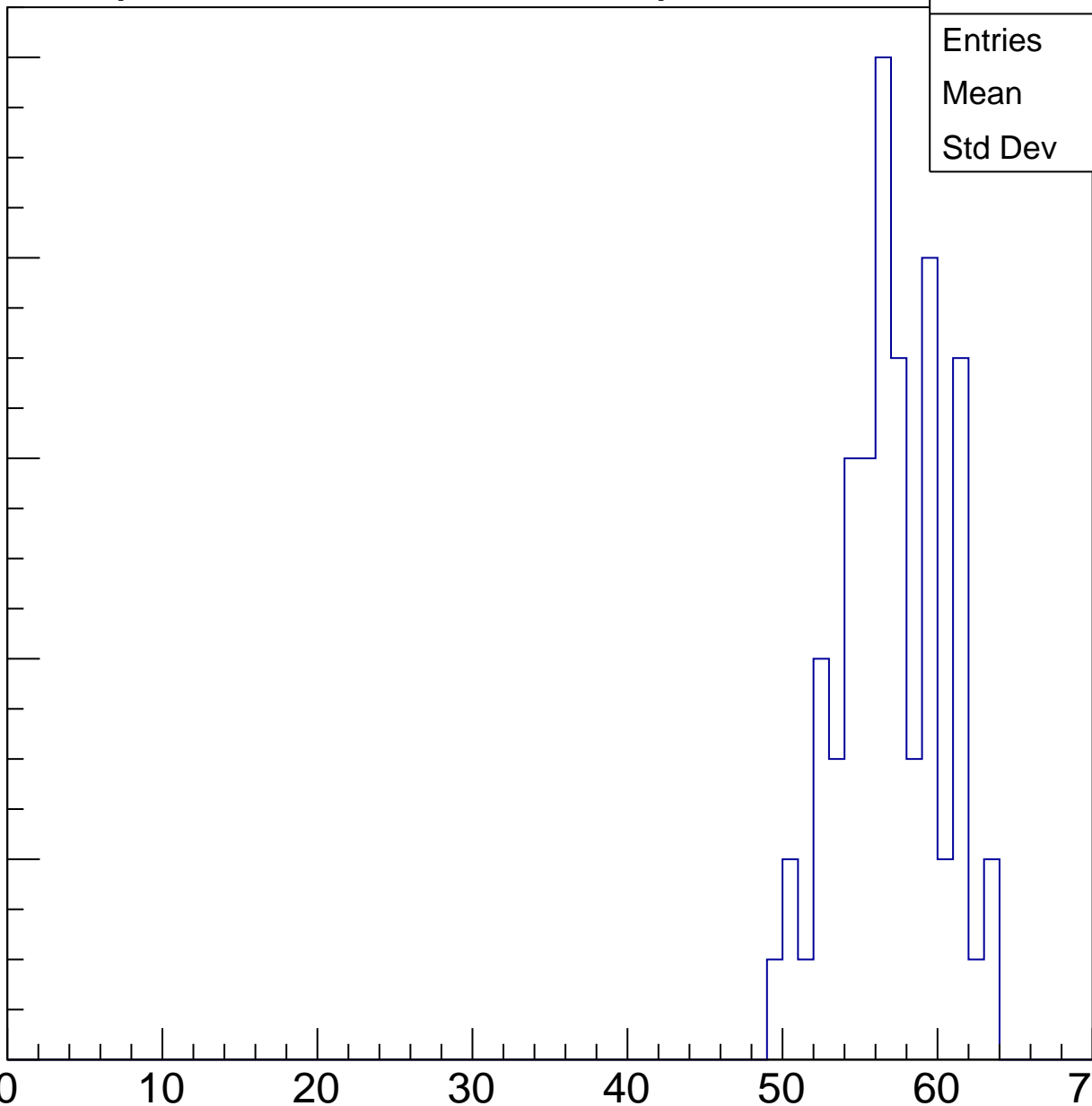
Entries	63
Mean	56.52
Std Dev	3.29

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

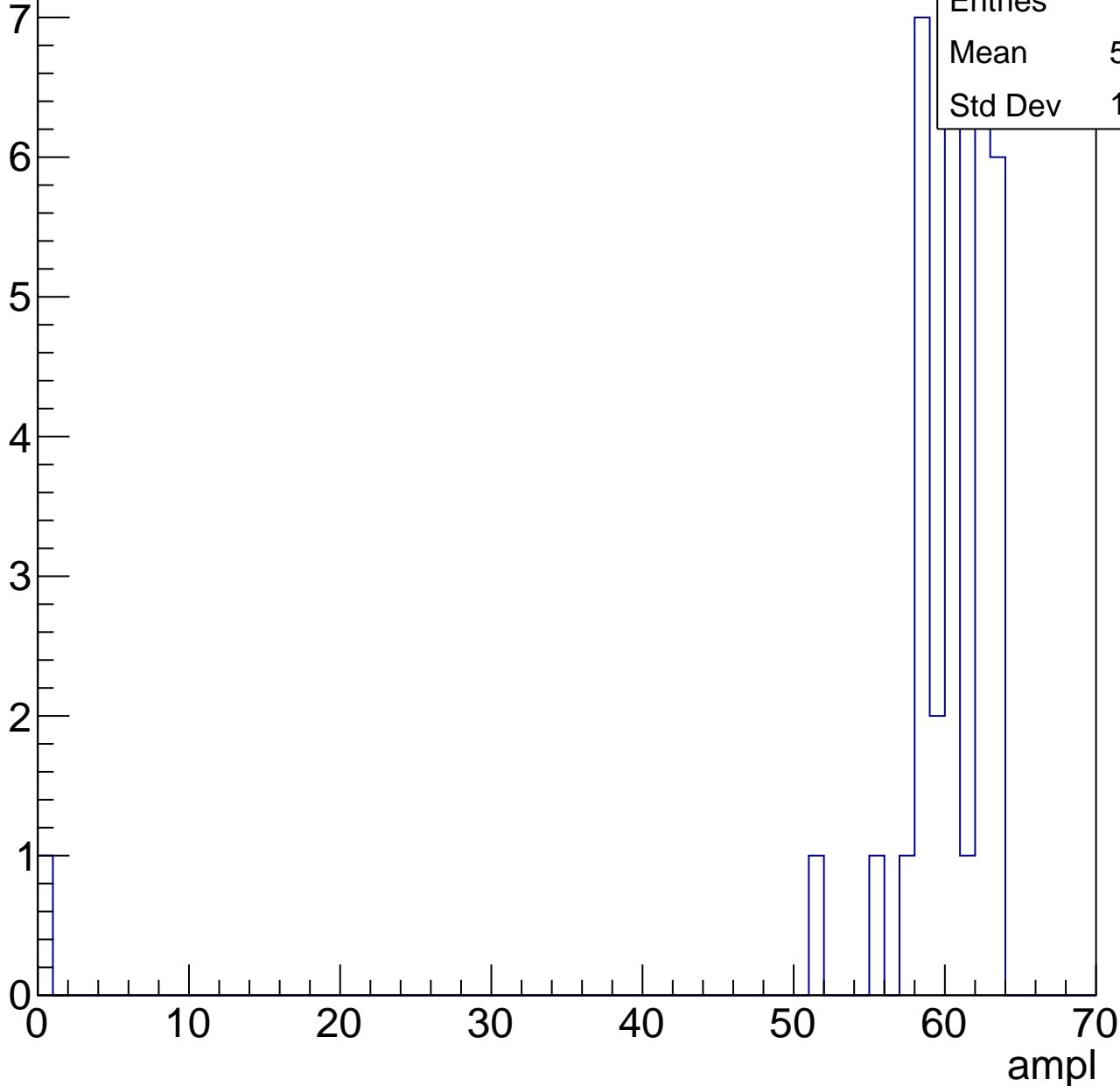


# B1L103S, U11-ch83, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	34
Mean	58.24
Std Dev	10.46



# B1L103S, U11-ch83, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	7
Mean	61.71
Std Dev	1.03

ampl

0 10 20 30 40 50 60 70



# B1L103S, U11-ch83, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U11-ch84, adc0

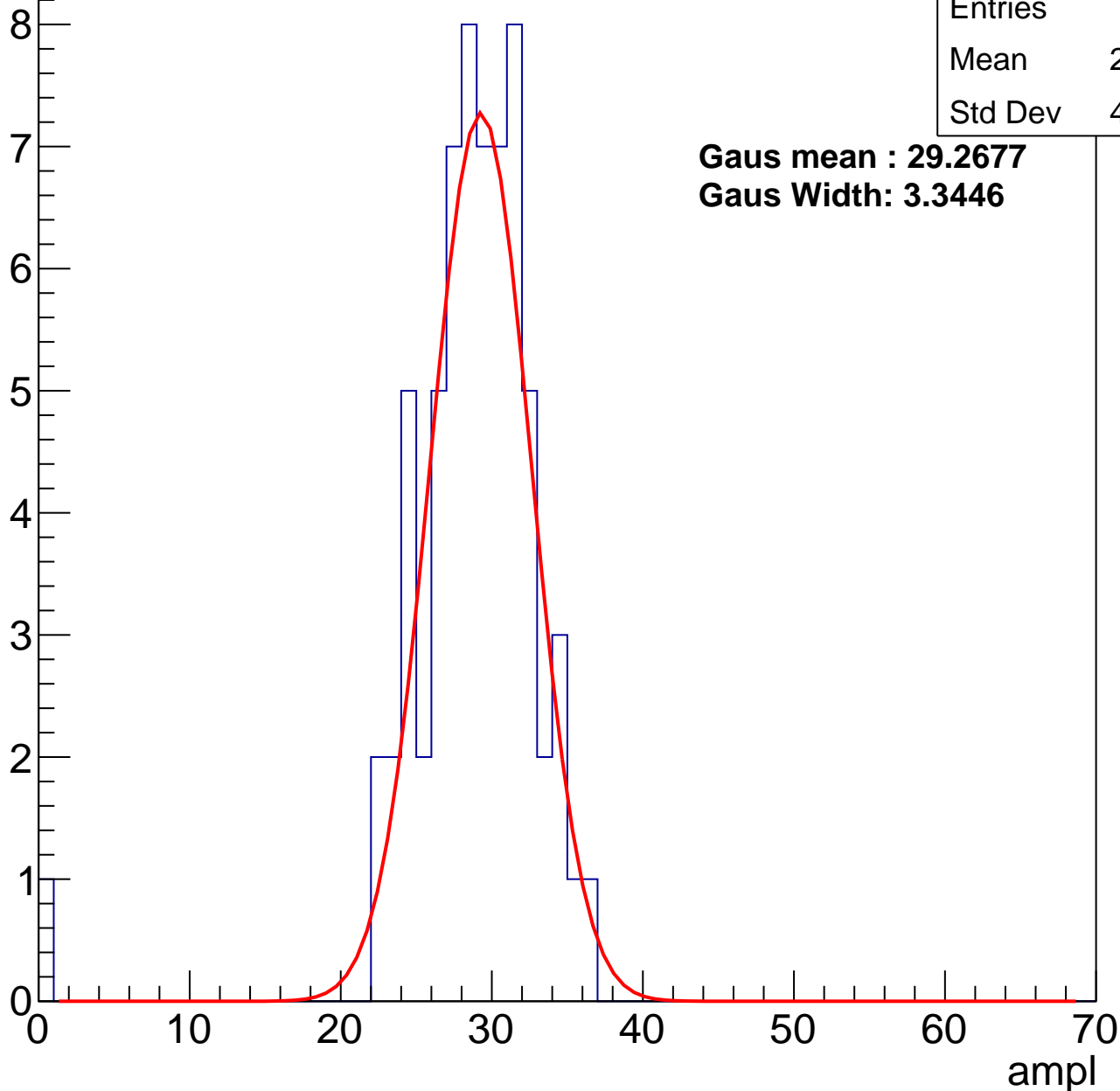
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	28.23
Std Dev	4.744

**Gaus mean : 29.2677**

**Gaus Width: 3.3446**



# B1L103S, U11-ch84, adc1

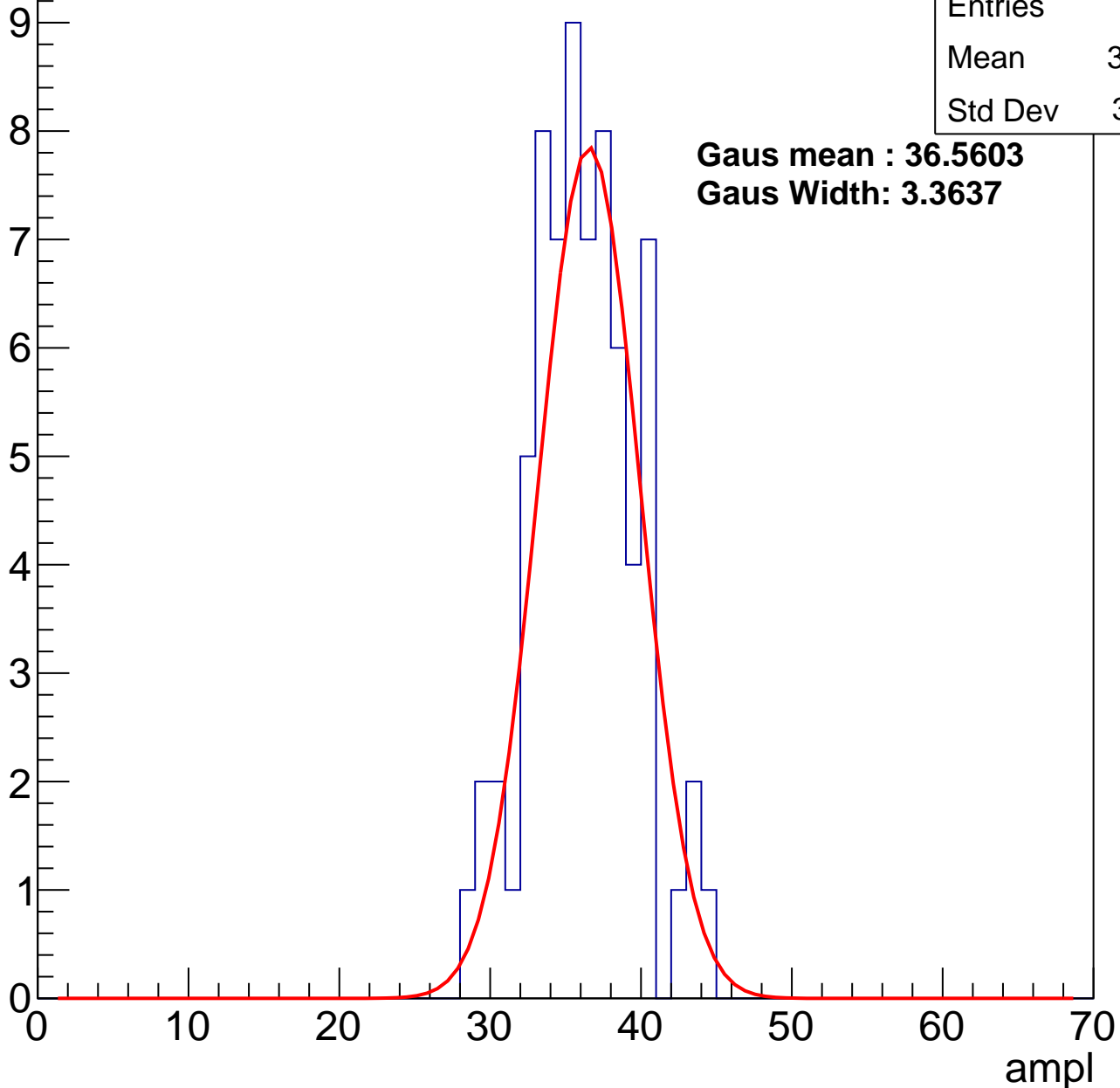
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	71
Mean	35.75
Std Dev	3.401

**Gaus mean : 36.5603**

**Gaus Width: 3.3637**



# B1L103S, U11-ch84, adc2

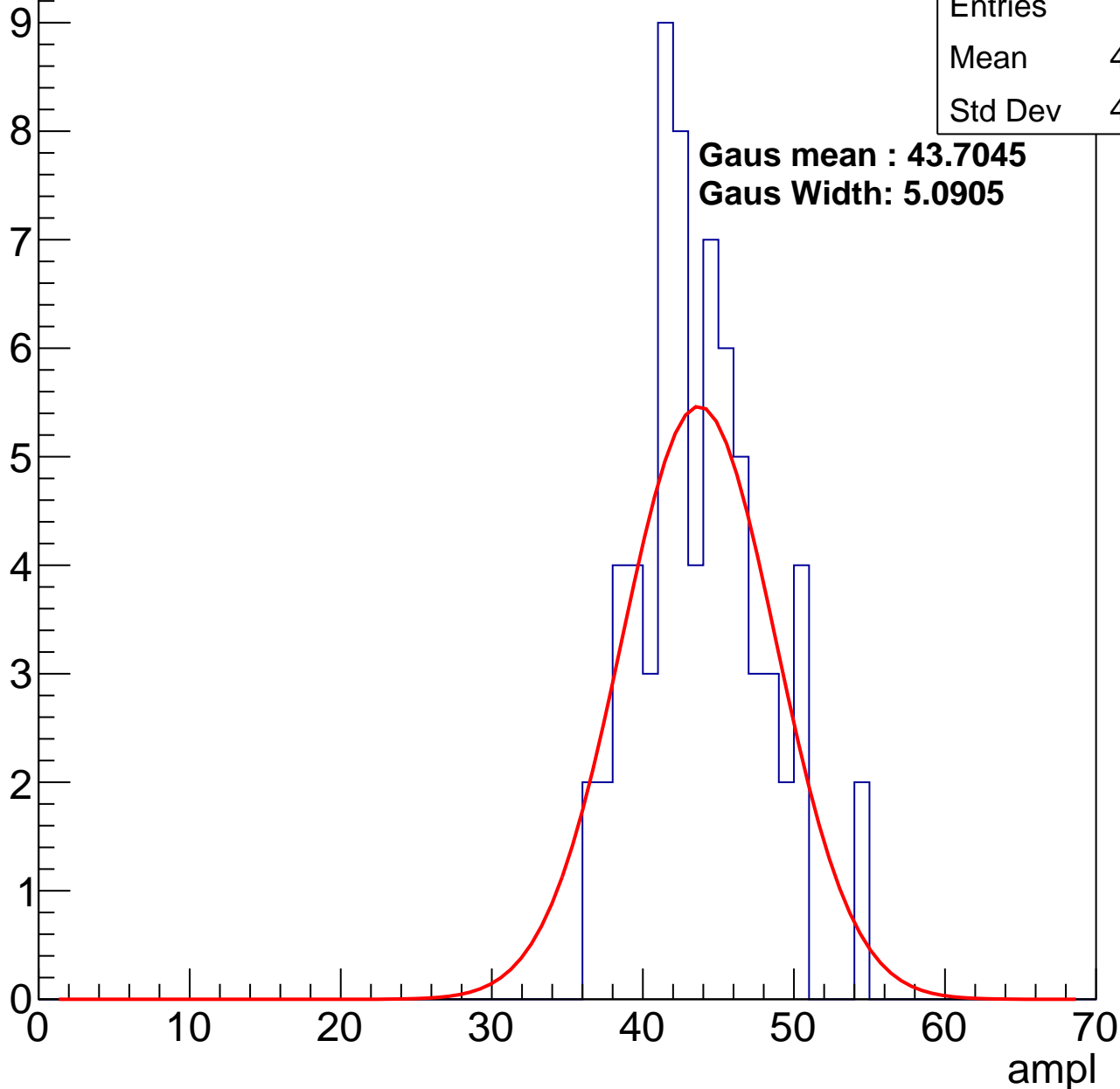
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	68
Mean	43.38
Std Dev	4.029

**Gaus mean : 43.7045**

**Gaus Width: 5.0905**



# B1L103S, U11-ch84, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	69
Mean	48.65
Std Dev	3.814

Entry

10

8

6

4

2

0

0

10

20

30

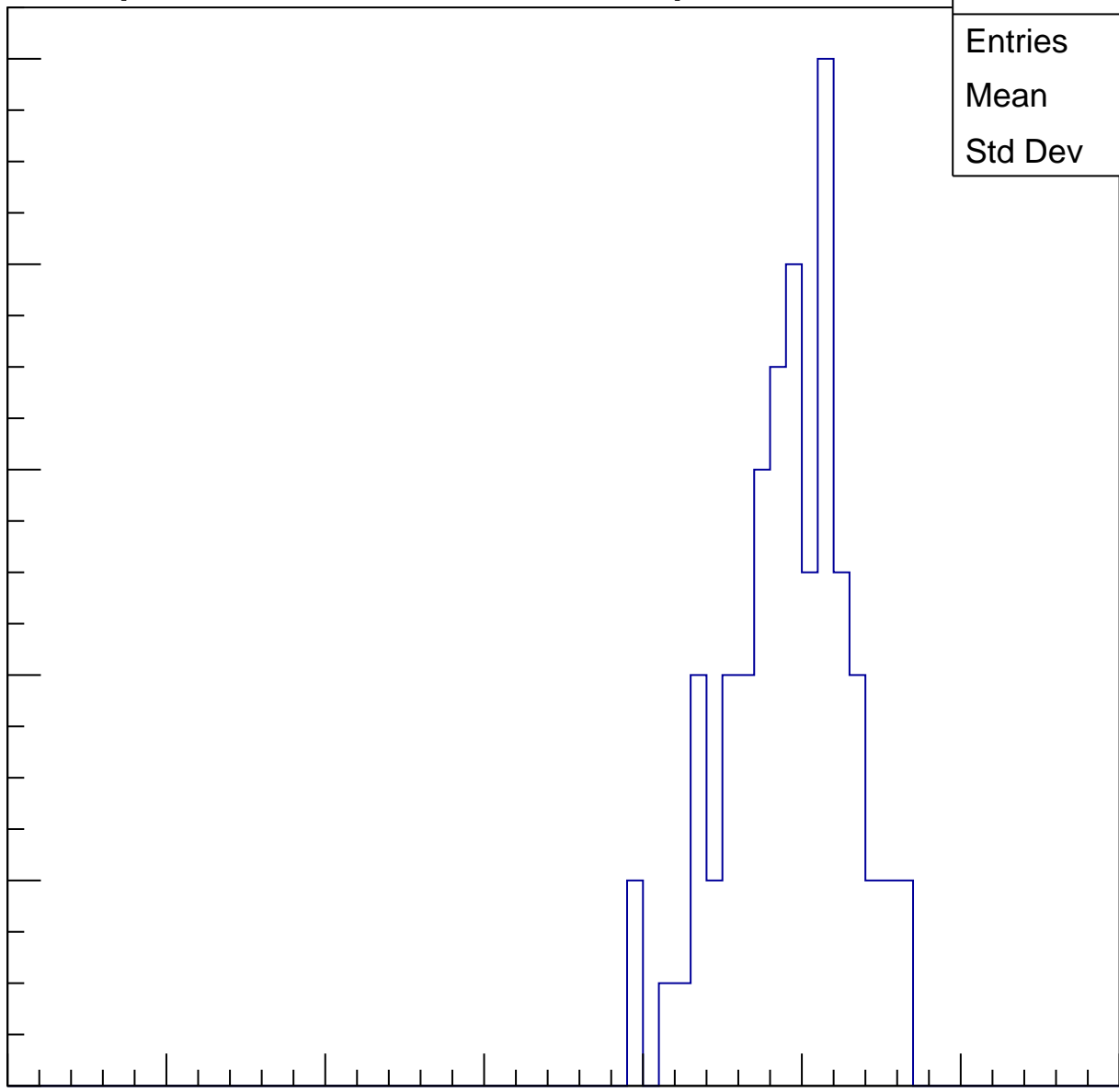
40

50

60

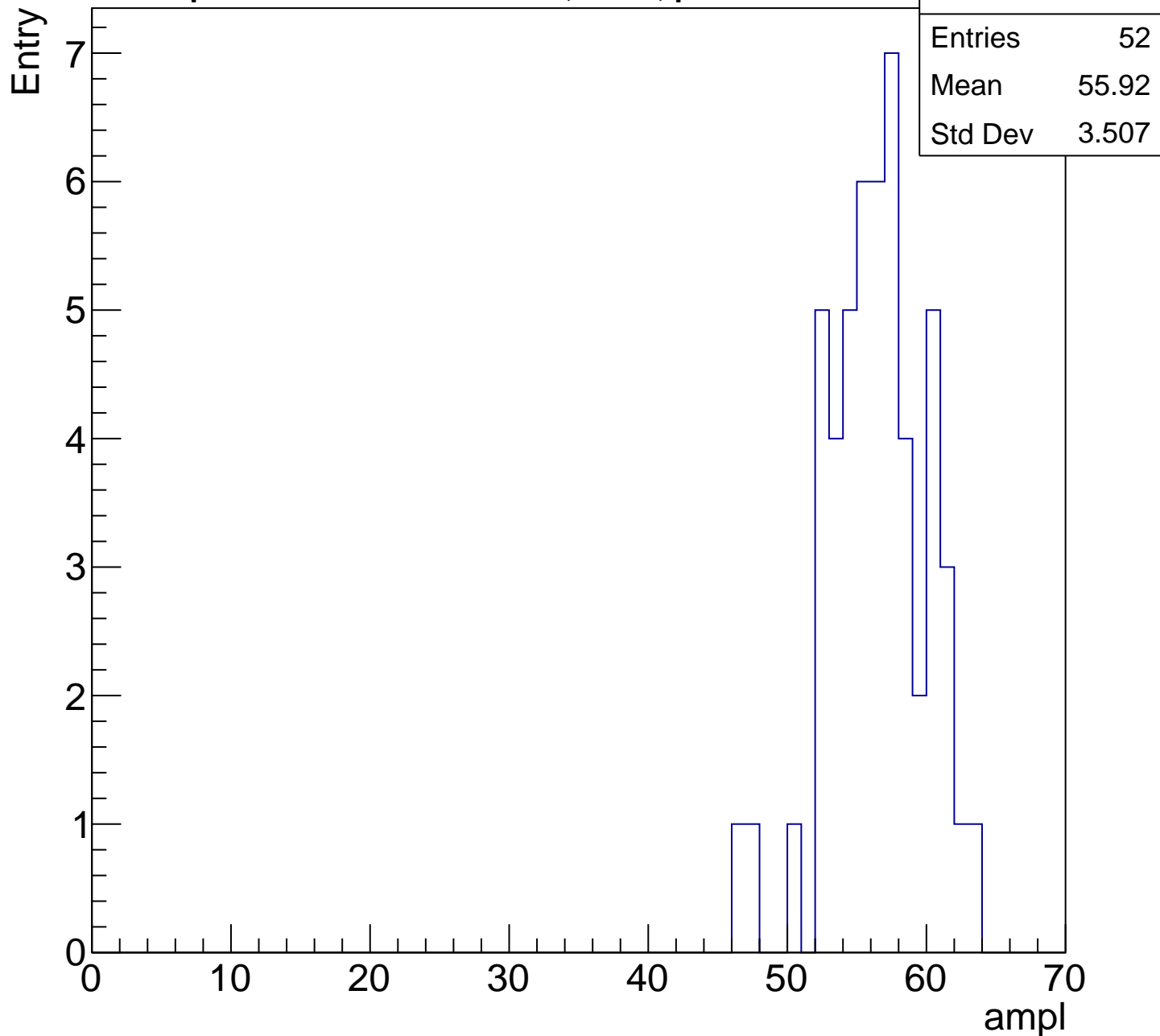
70

ampl



# B1L103S, U11-ch84, adc4

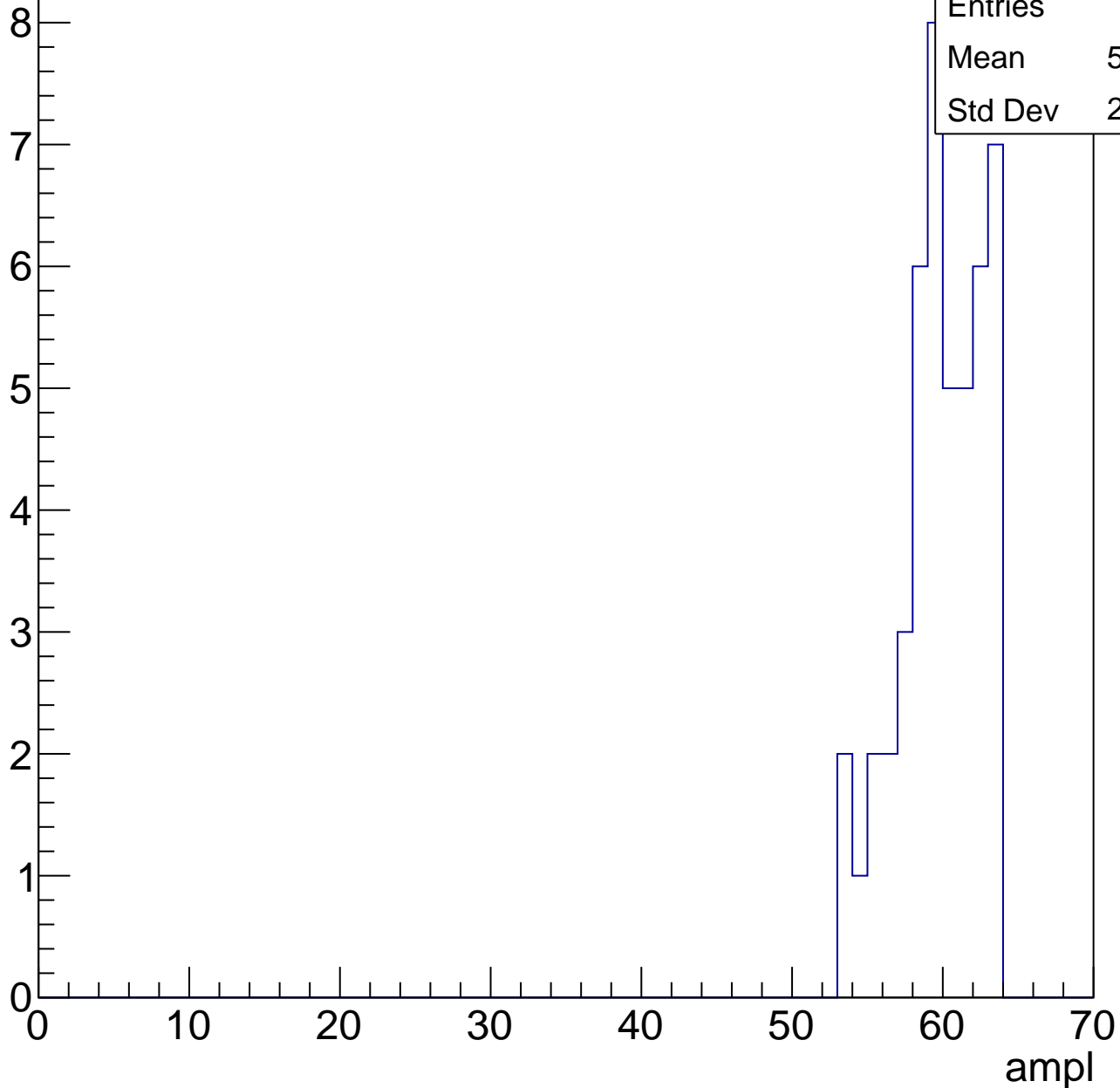
calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U11-ch84, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

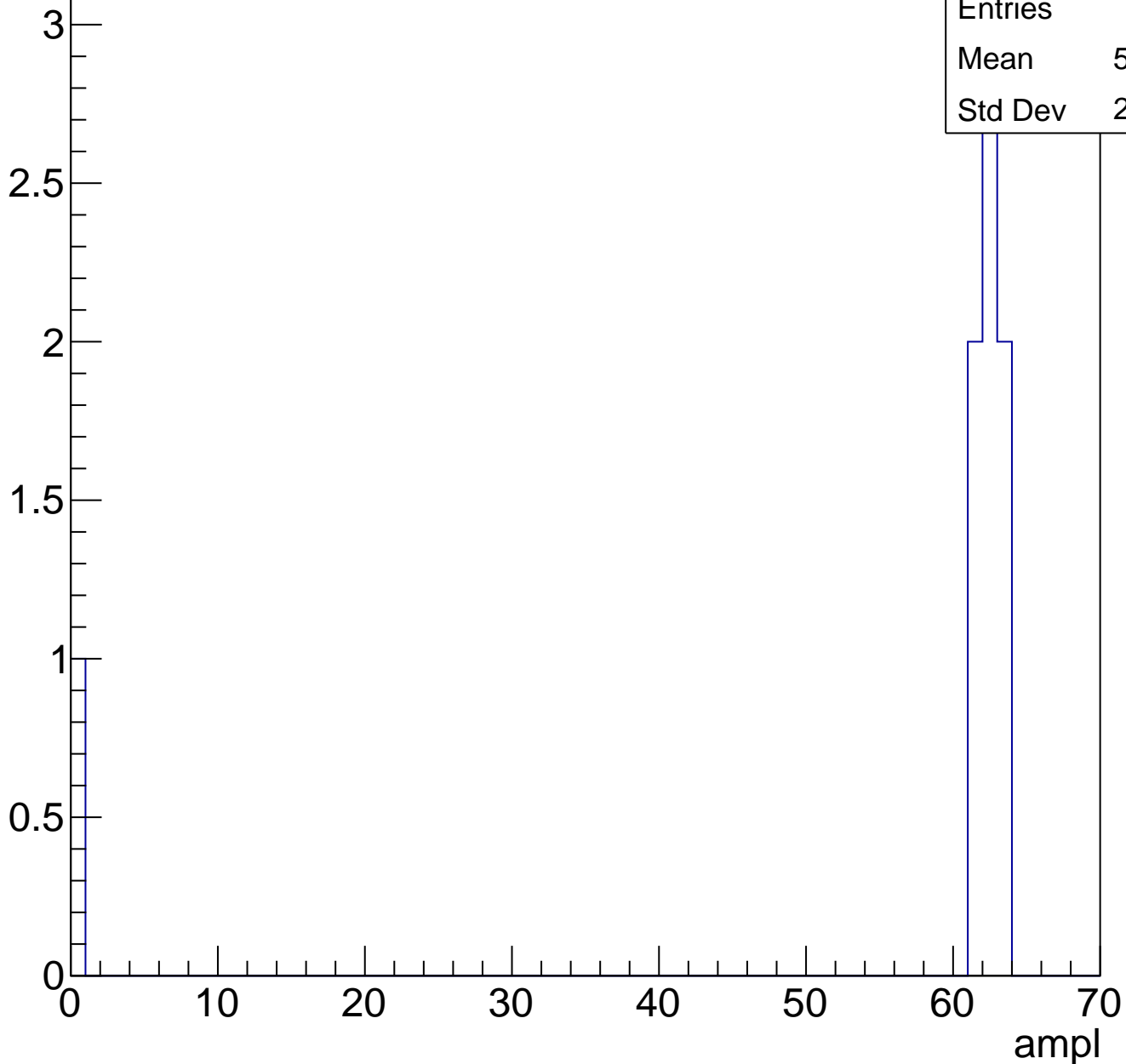


Entries	47
Mean	59.38
Std Dev	2.725

# B1L103S, U11-ch84, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U11-ch84, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	3
Mean	7.333
Std Dev	10.37

# B1L103S, U11-ch85, adc0

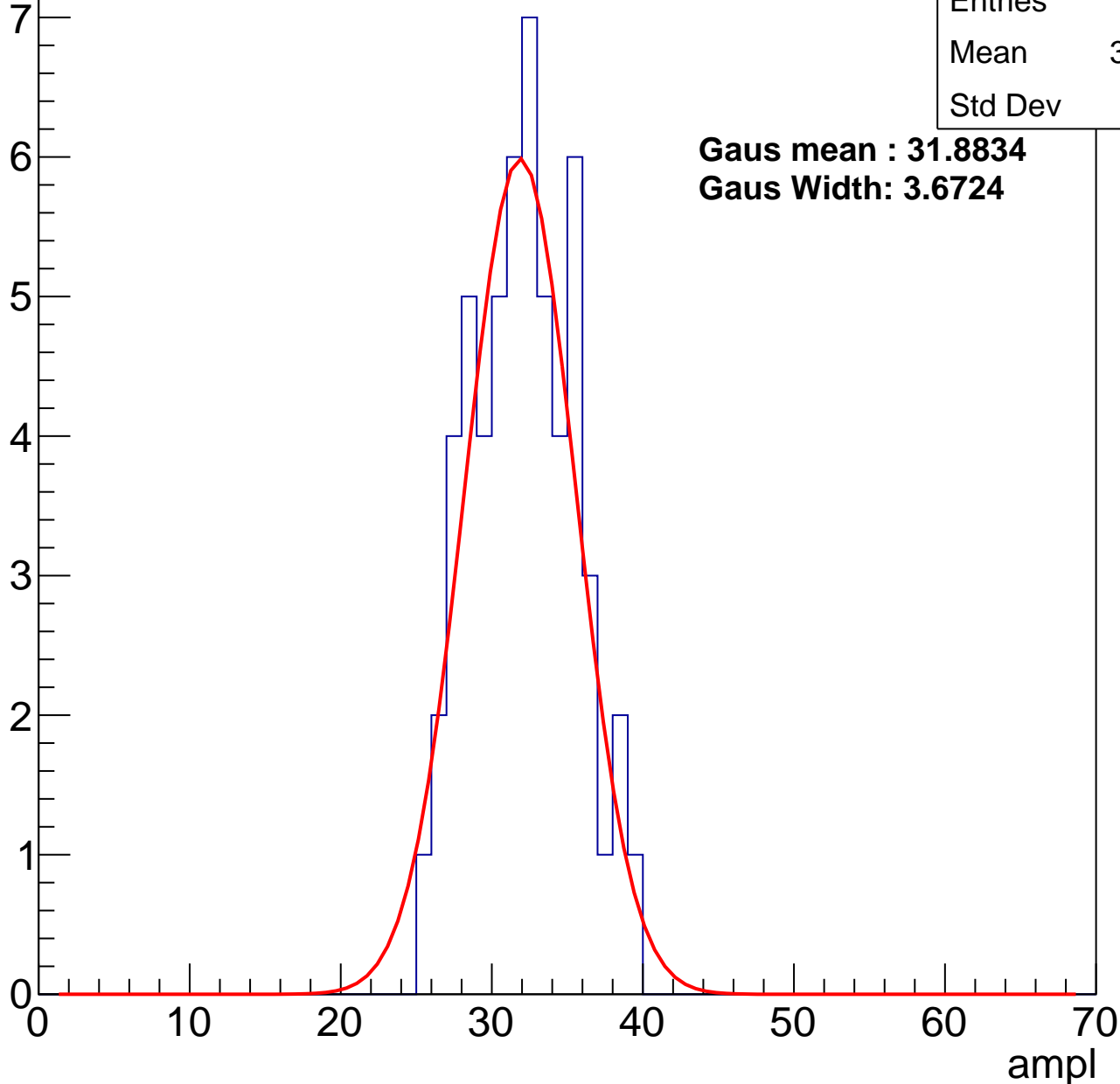
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	56
Mean	31.64
Std Dev	3.34

**Gaus mean : 31.8834**

**Gaus Width: 3.6724**



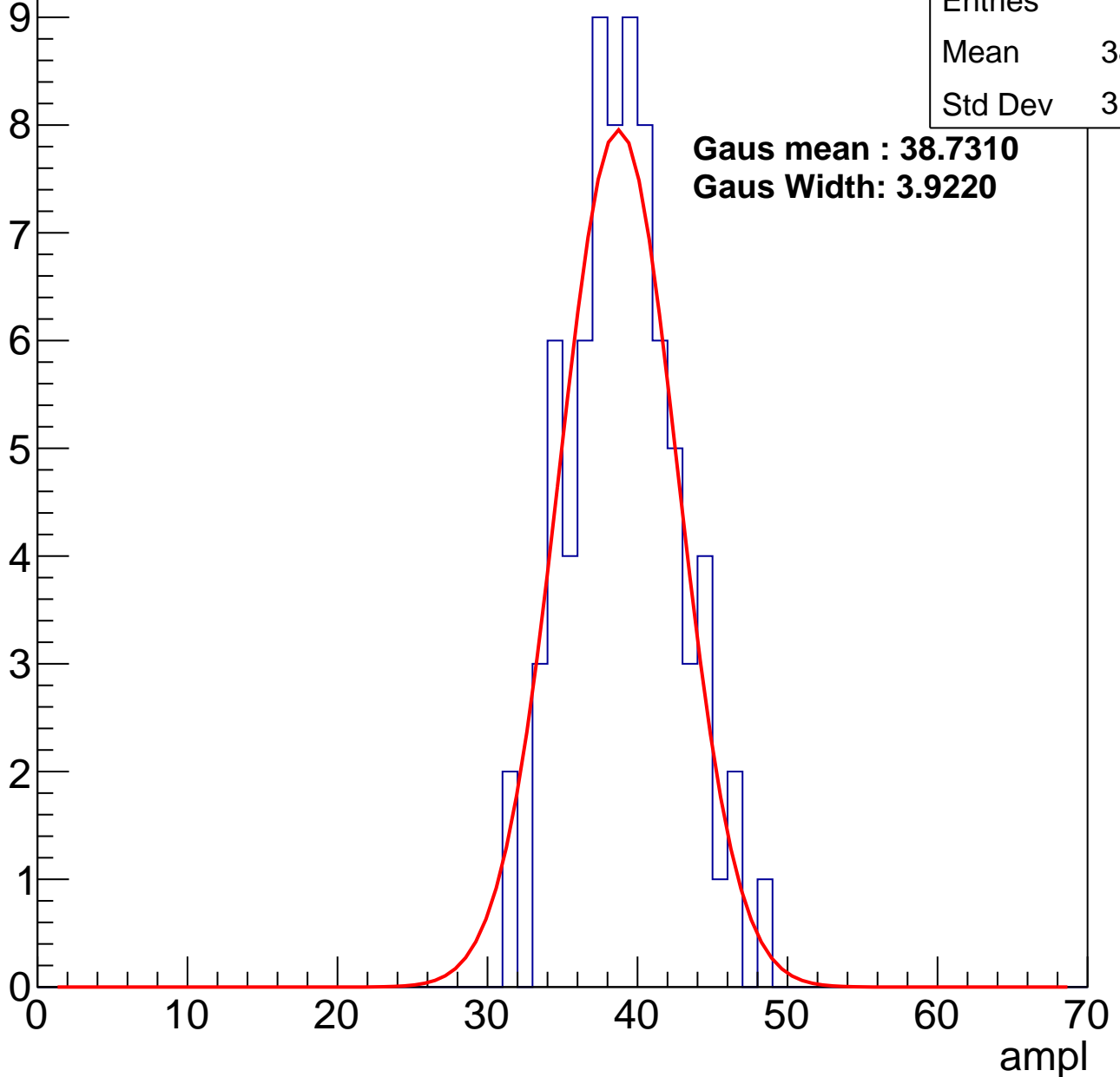
# B1L103S, U11-ch85, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	77
Mean	38.64
Std Dev	3.564

**Gaus mean : 38.7310**  
**Gaus Width: 3.9220**



# B1L103S, U11-ch85, adc2

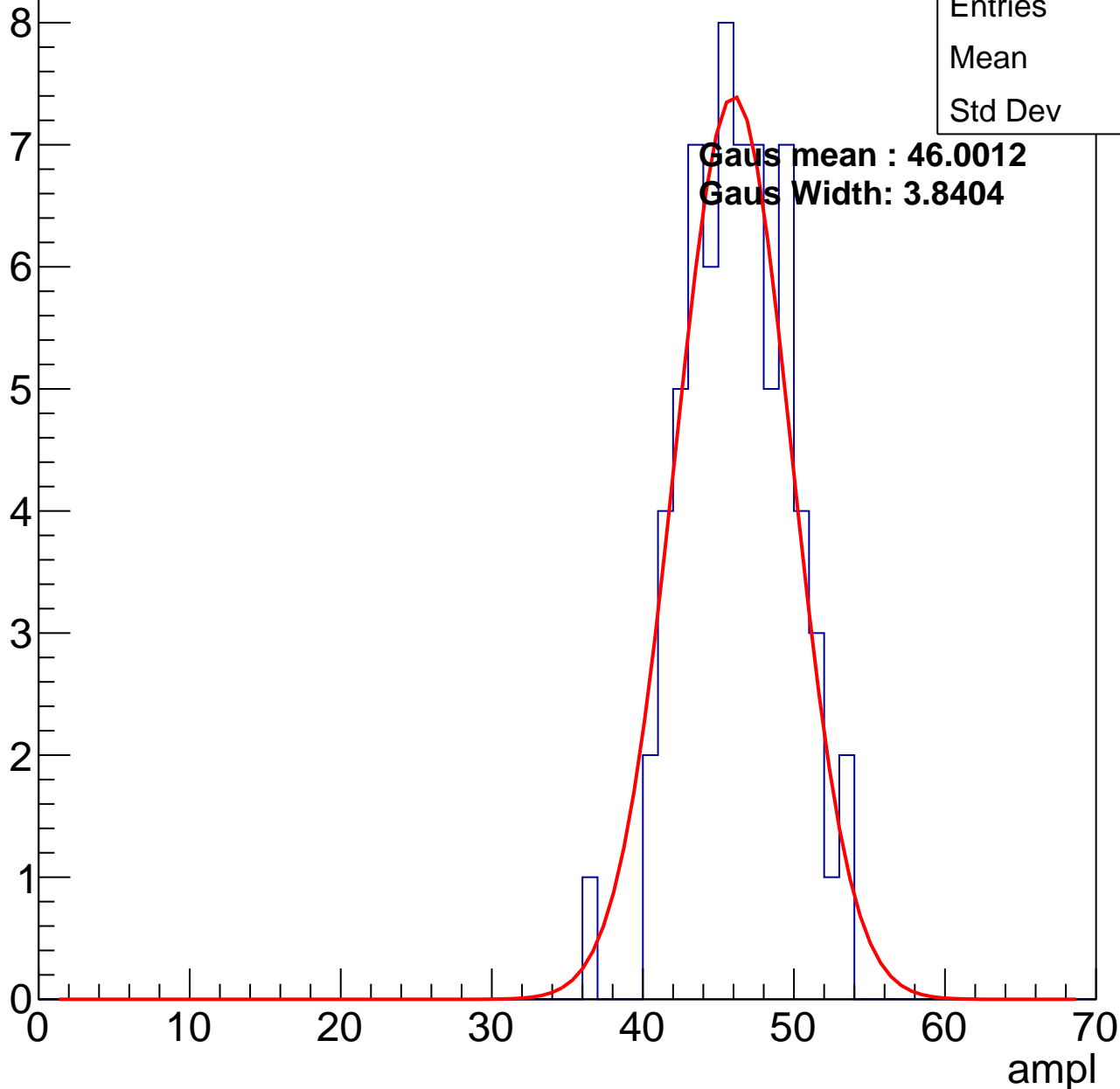
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	69
Mean	45.8
Std Dev	3.42

Gaus mean : 46.0012

Gaus Width: 3.8404

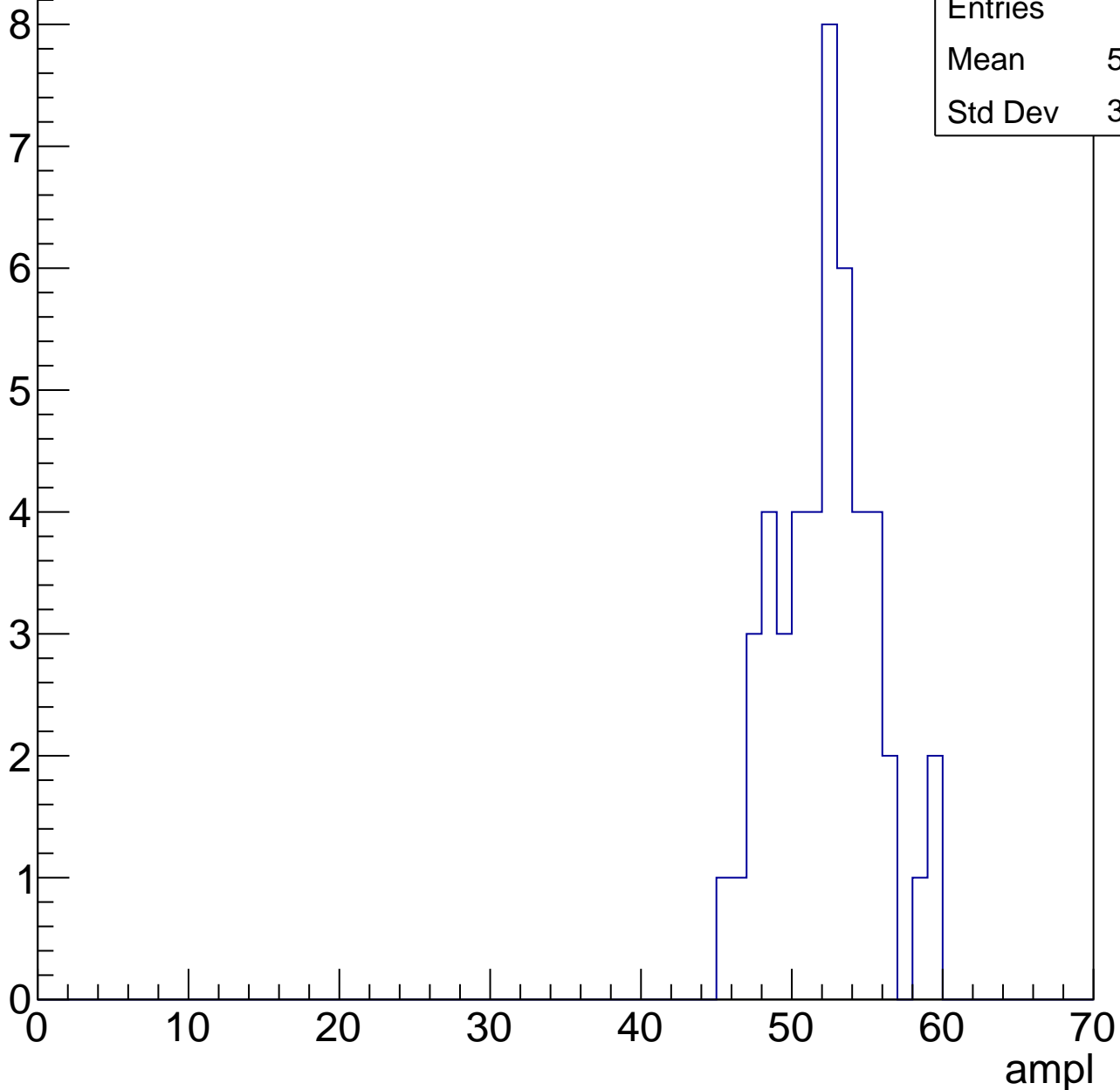


# B1L103S, U11-ch85, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	47
Mean	51.77
Std Dev	3.237



# B1L103S, U11-ch85, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	60
Mean	55.95
Std Dev	7.938

Entry

10

8

6

4

2

0

0

10

20

30

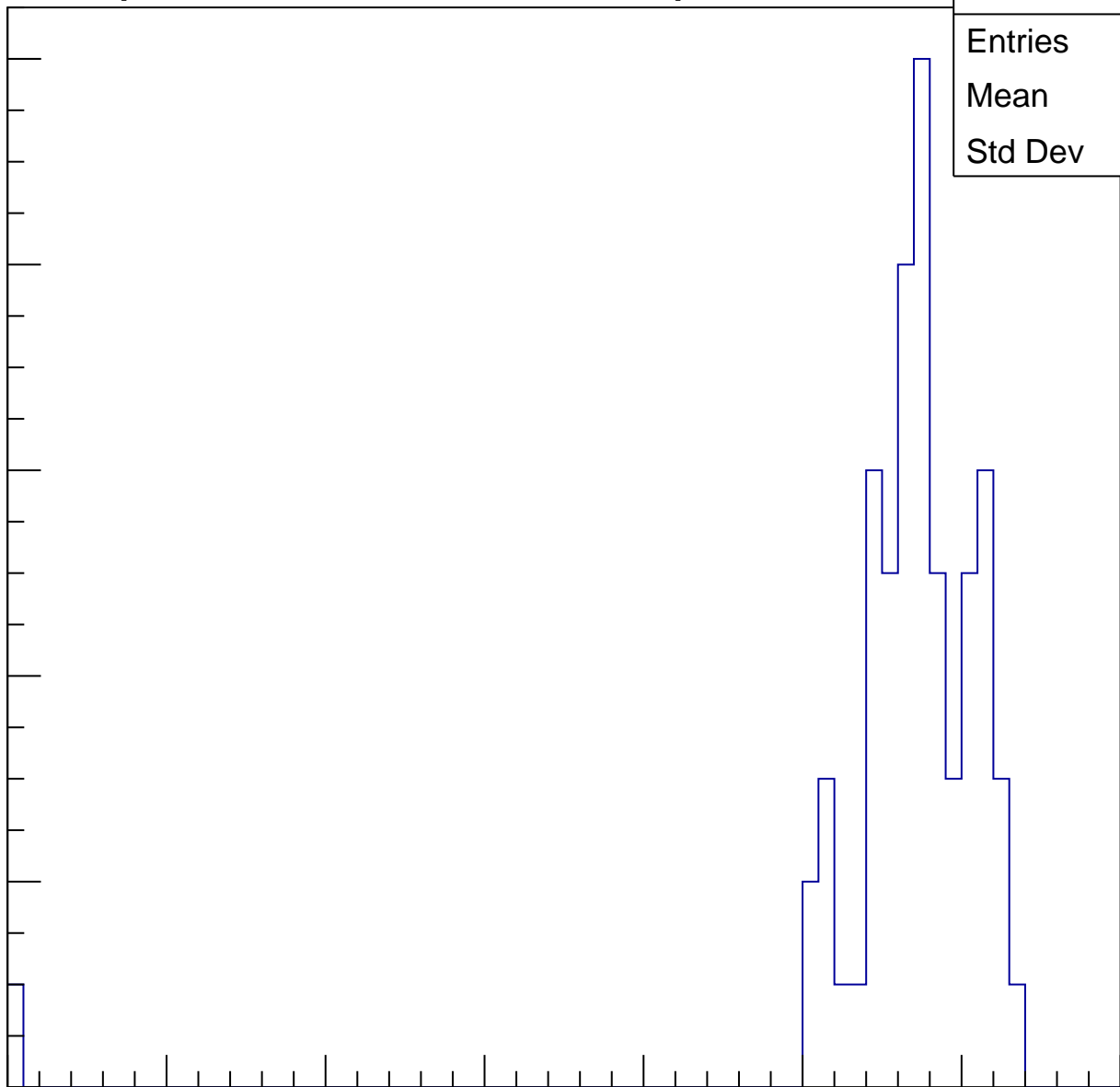
40

50

60

70

ampl

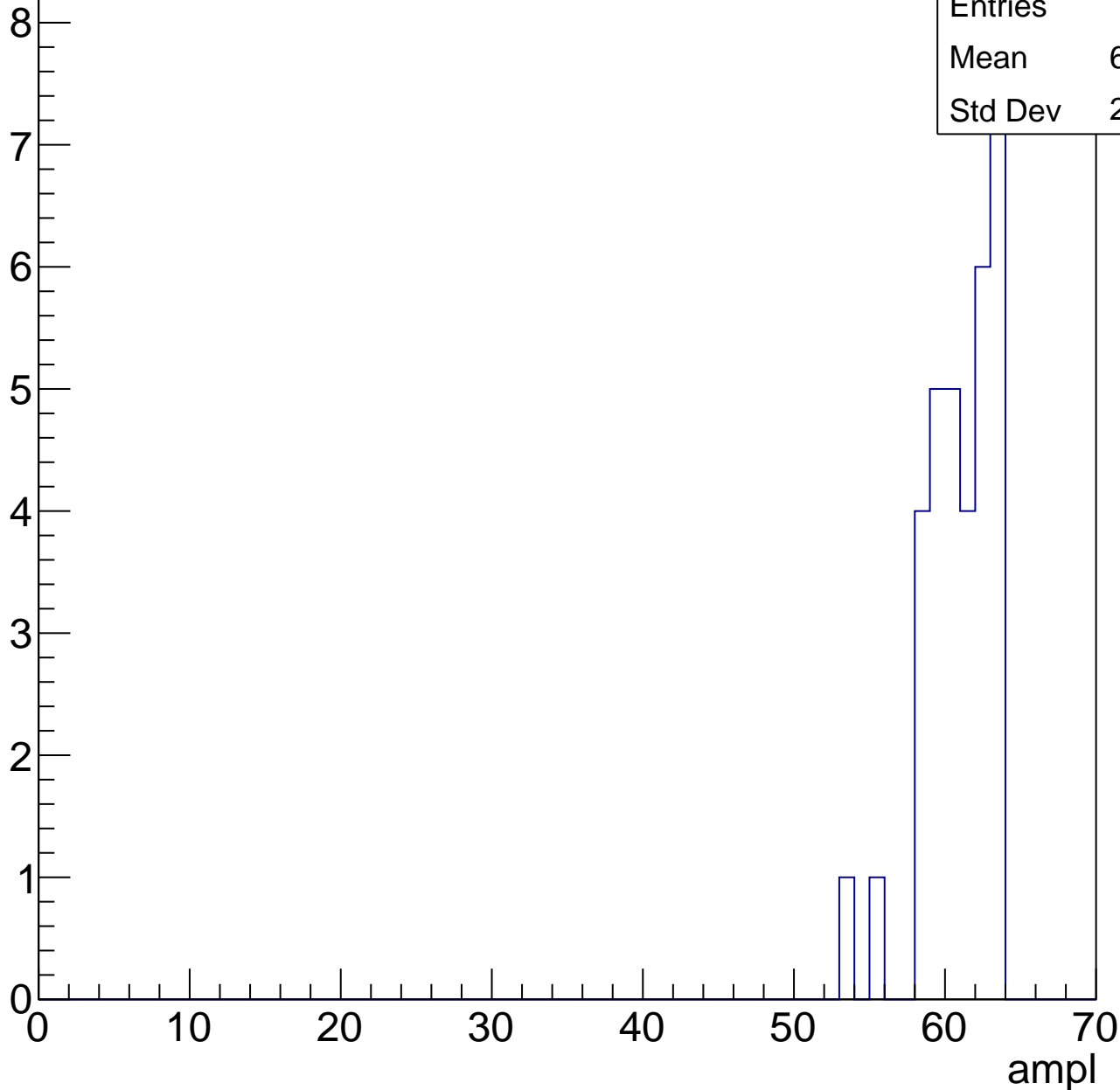


# B1L103S, U11-ch85, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	34
Mean	60.44
Std Dev	2.354



# B1L103S, U11-ch85, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U11-ch85, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

1  
0.8  
0.6  
0.4  
0.2  
0

Entries	1
Mean	24
Std Dev	0

ampl

# B1L103S, U11-ch86, adc0

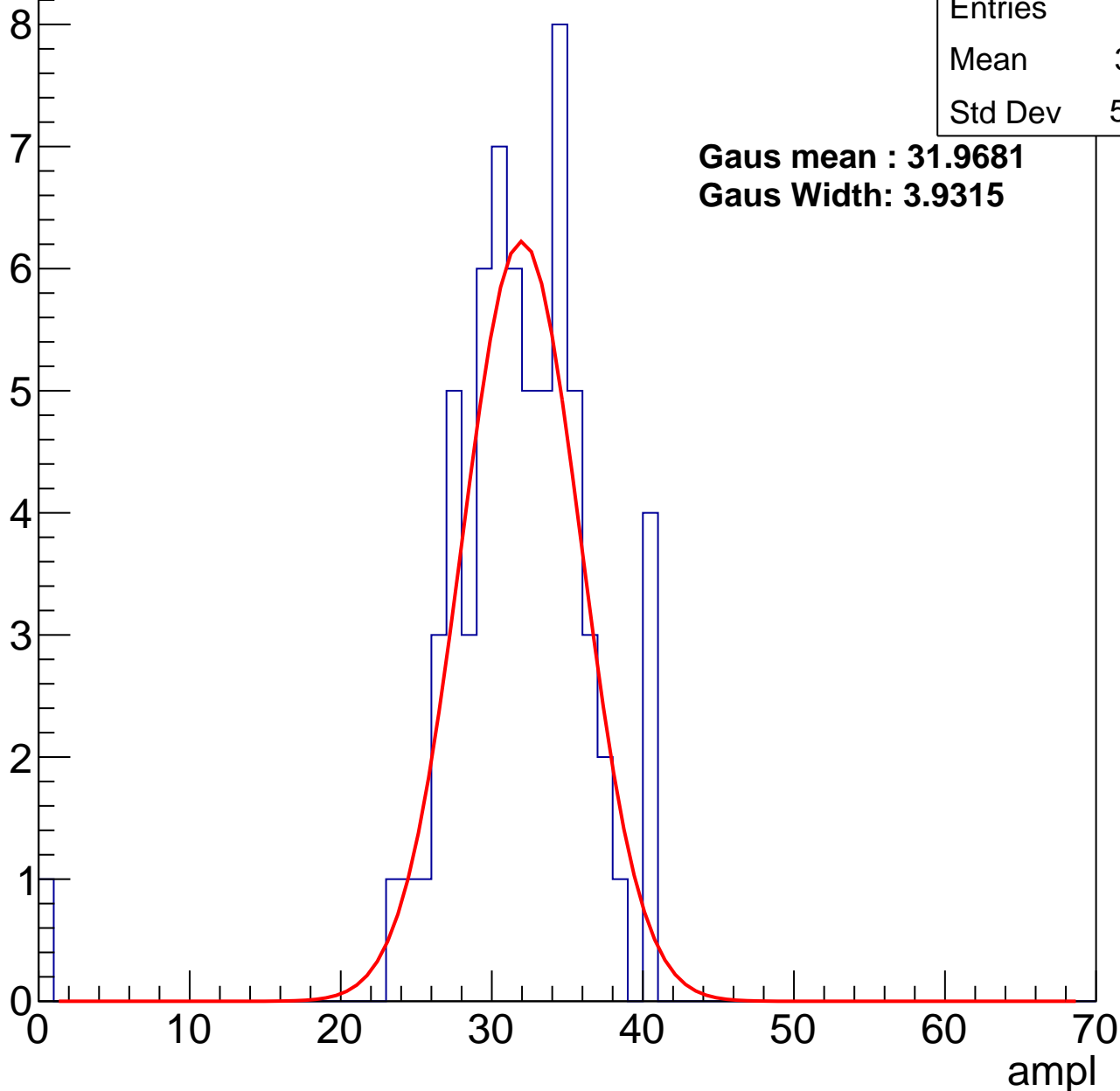
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	31.21
Std Dev	5.487

**Gaus mean : 31.9681**

**Gaus Width: 3.9315**



# B1L103S, U11-ch86, adc1

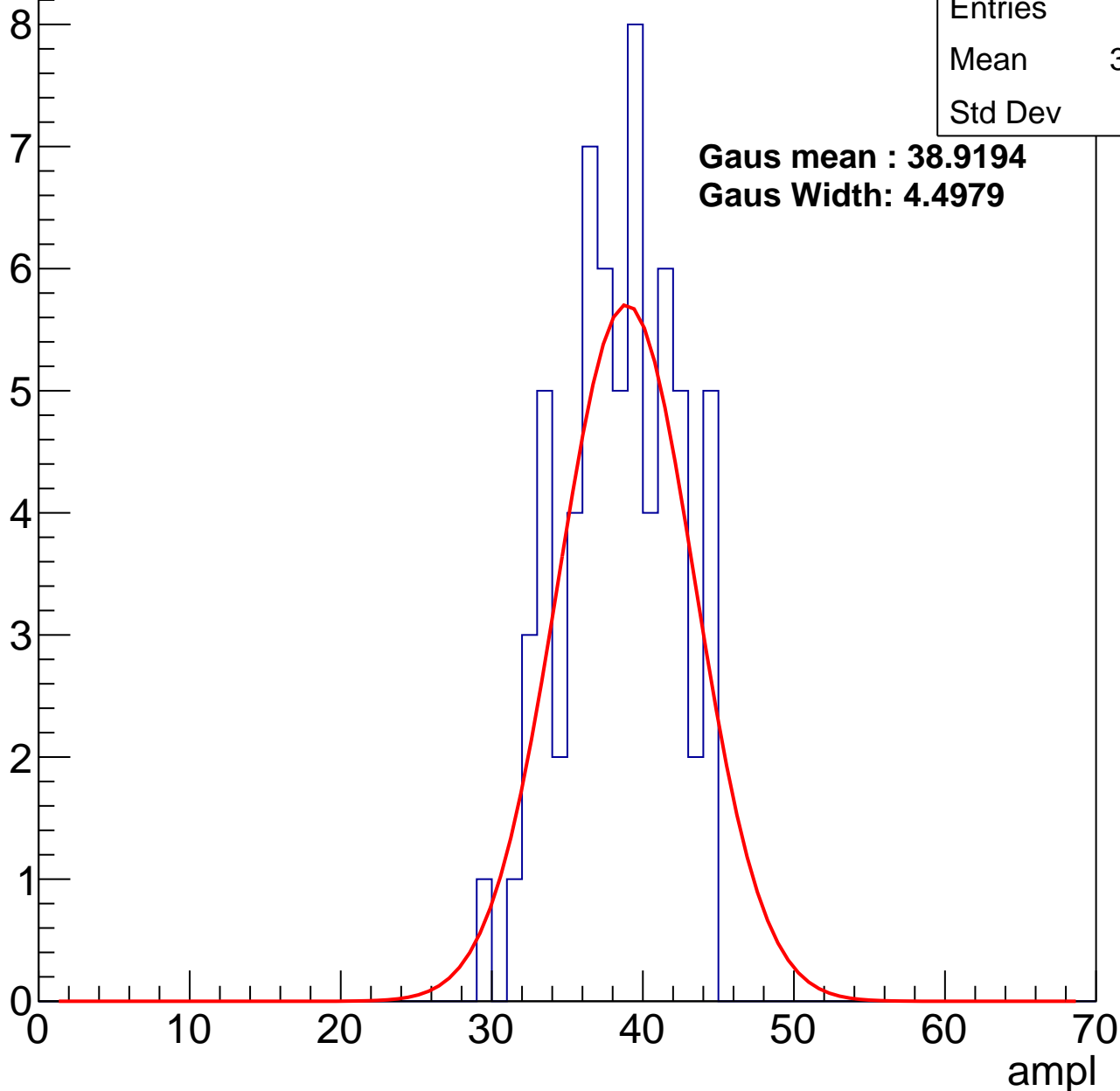
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	37.92
Std Dev	3.65

**Gaus mean : 38.9194**

**Gaus Width: 4.4979**



# B1L103S, U11-ch86, adc2

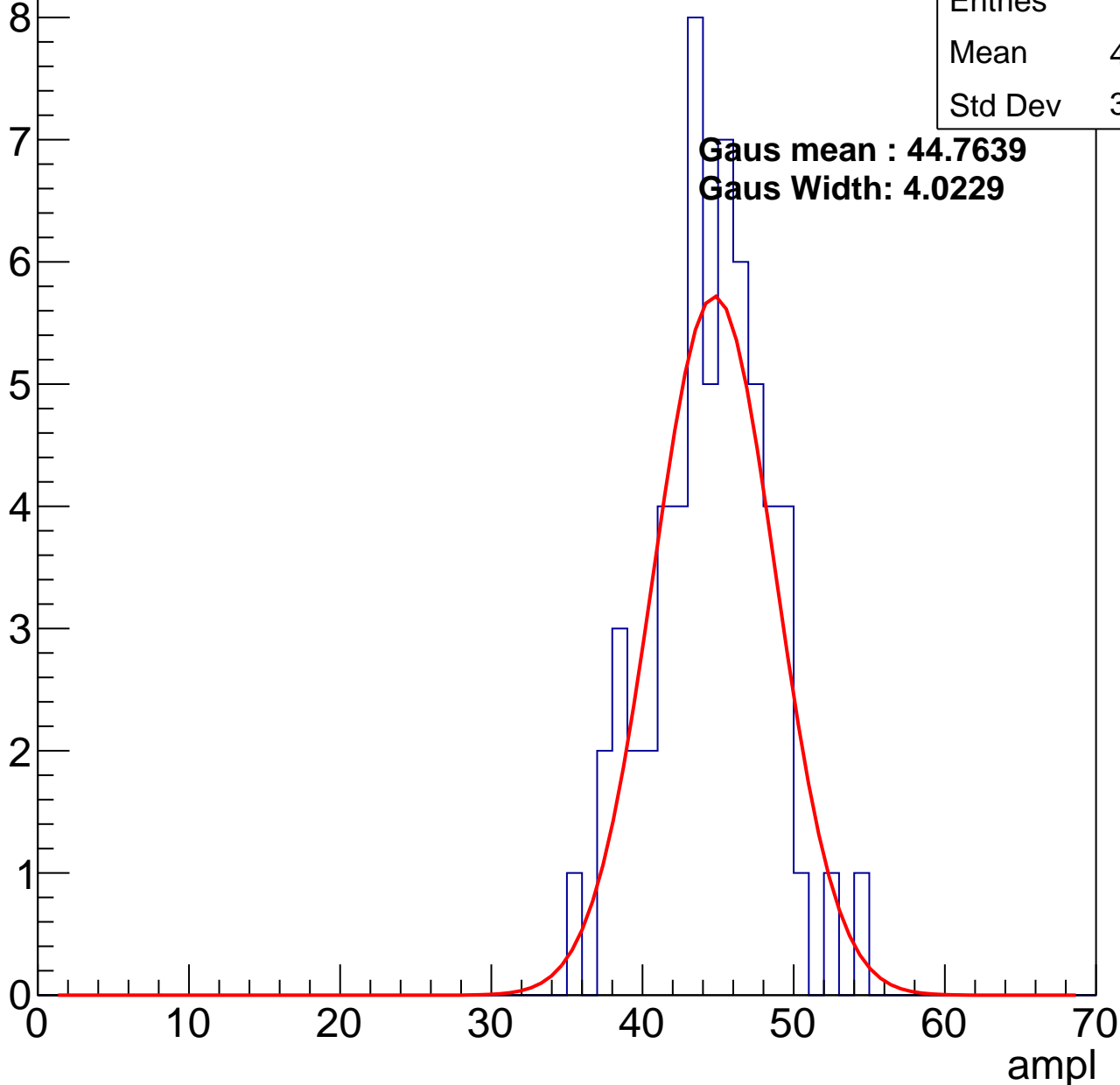
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	60
Mean	44.12
Std Dev	3.804

**Gaus mean : 44.7639**

**Gaus Width: 4.0229**

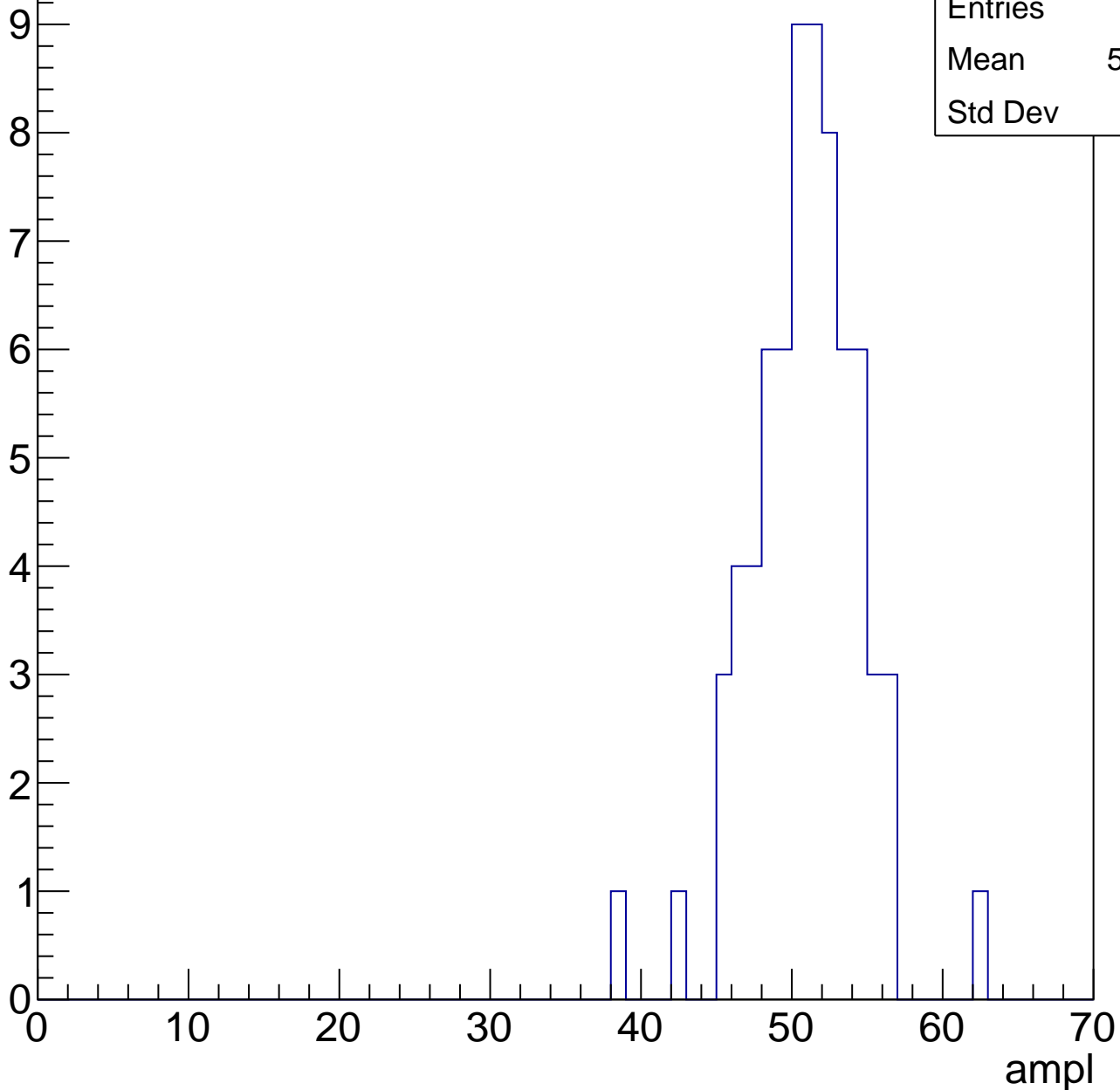


# B1L103S, U11-ch86, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	70
Mean	50.44
Std Dev	3.62

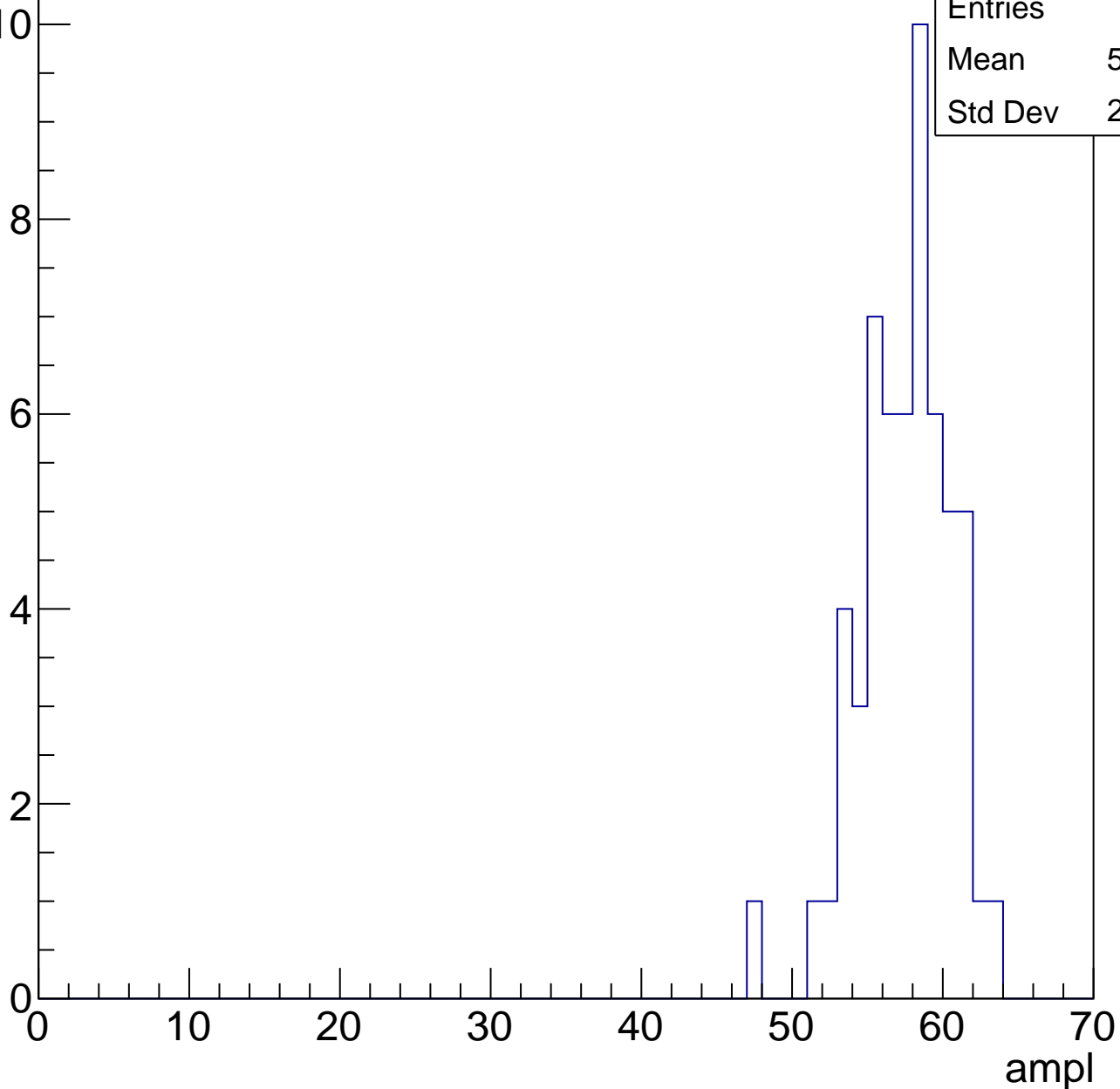


# B1L103S, U11-ch86, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	57
Mean	57.04
Std Dev	2.979

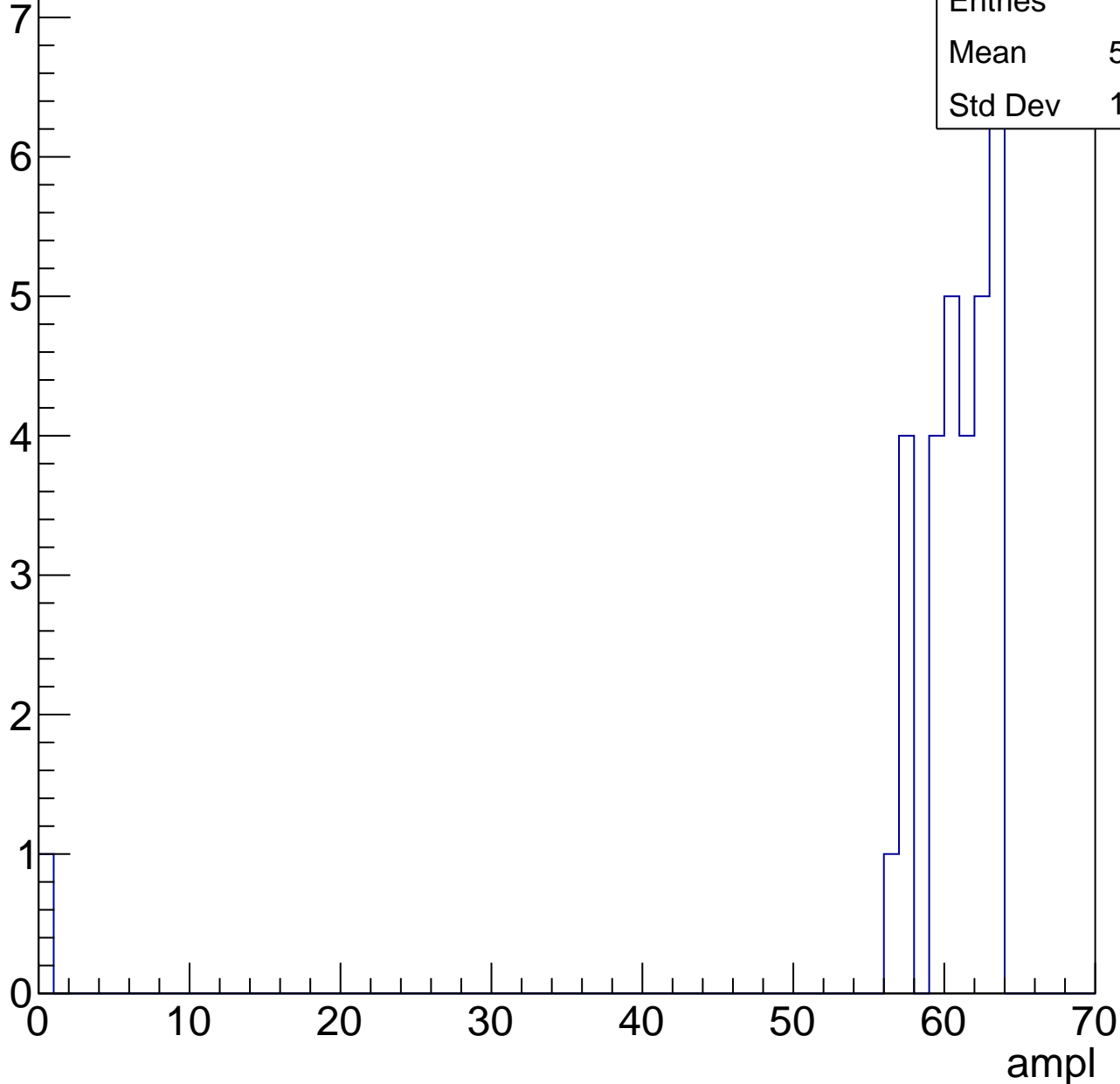


# B1L103S, U11-ch86, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	31
Mean	58.55
Std Dev	10.89



# B1L103S, U11-ch86, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

3

2.5

2

1.5

1

0.5

0

0

10

20

30

40

50

60

70

ampl

Entries

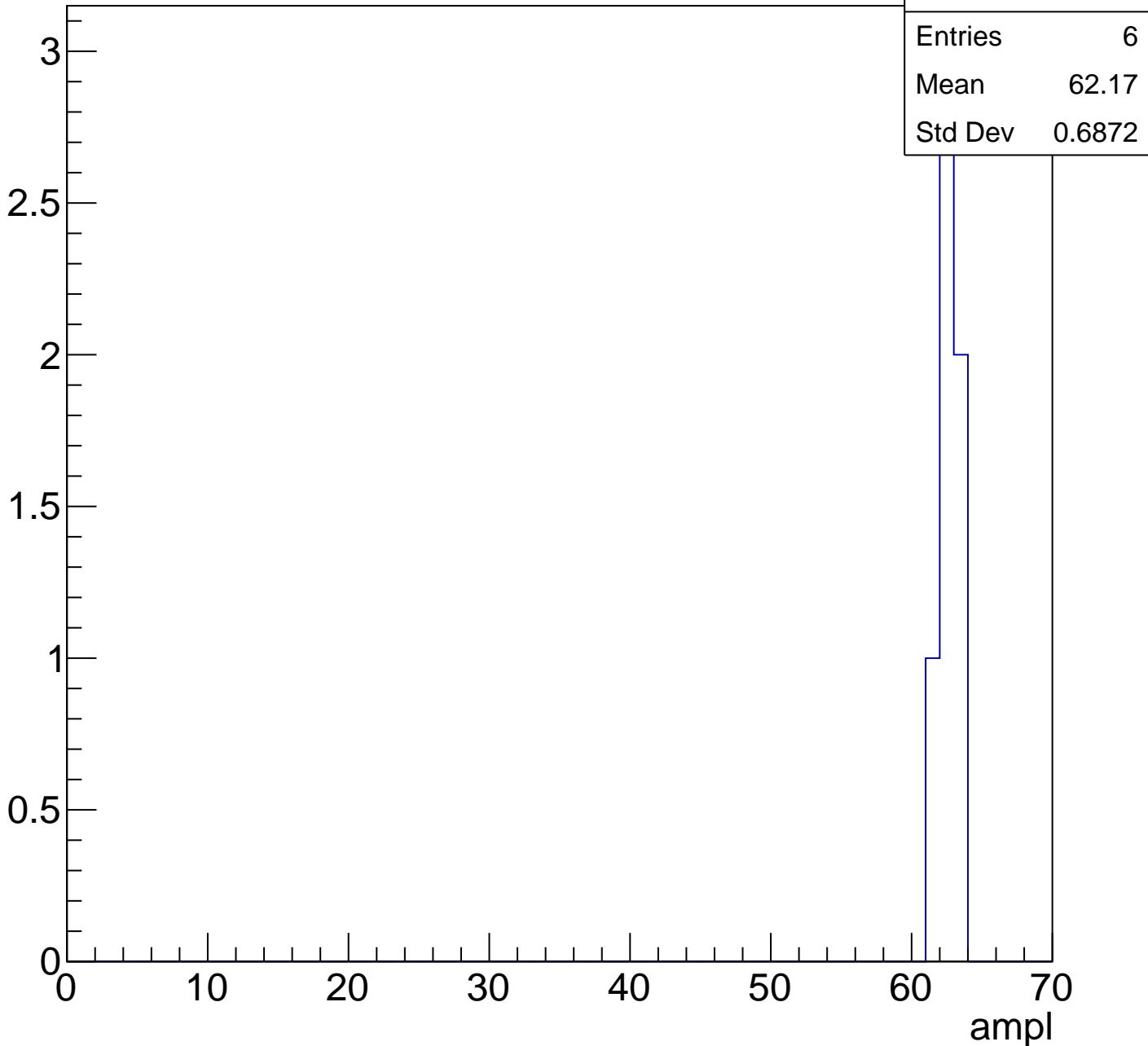
6

Mean

62.17

Std Dev

0.6872





# B1L103S, U11-ch86, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	2
Mean	11.5
Std Dev	11.5

# B1L103S, U11-ch87, adc0

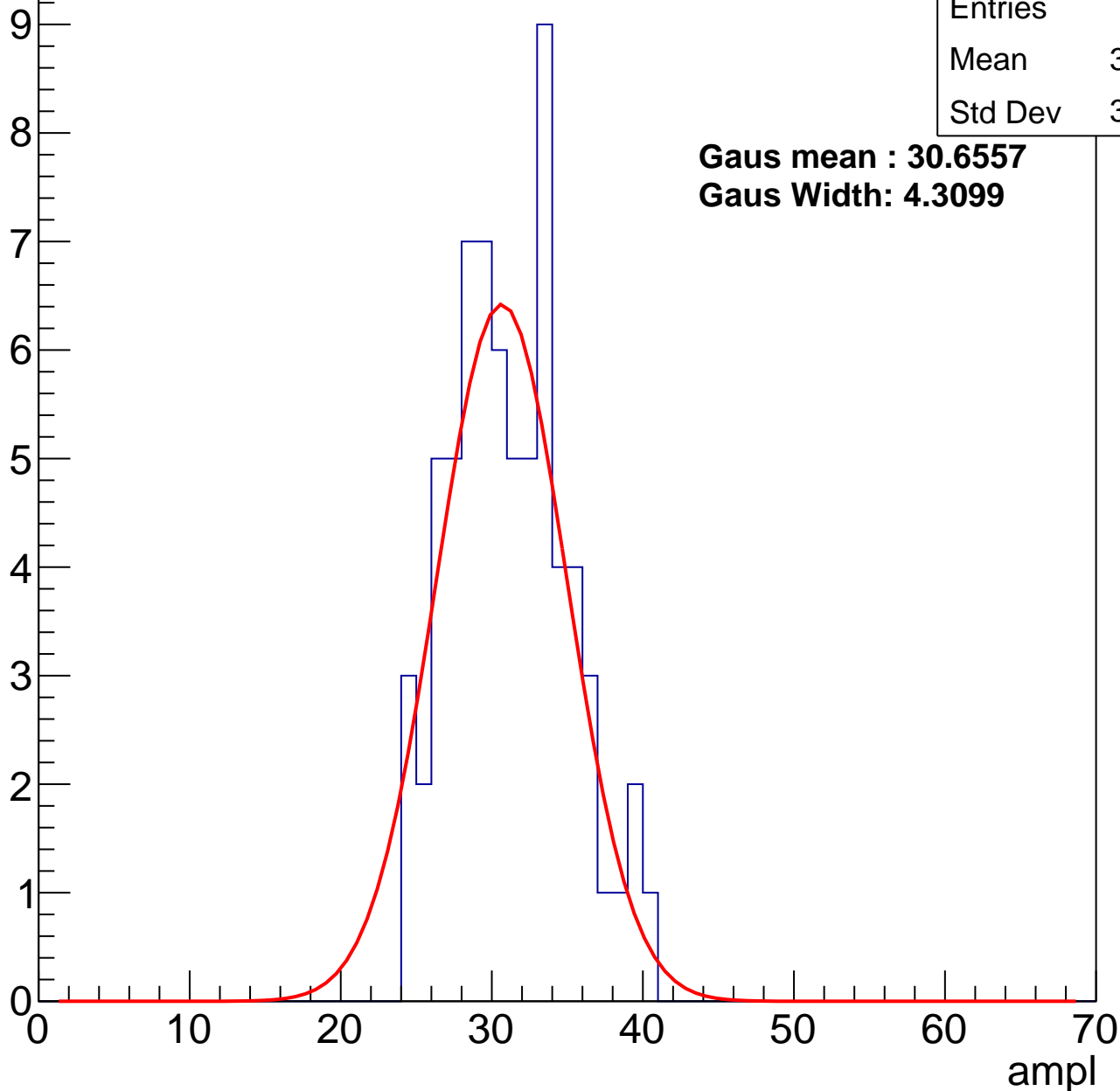
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	70
Mean	30.79
Std Dev	3.832

**Gaus mean : 30.6557**

**Gaus Width: 4.3099**



# B1L103S, U11-ch87, adc1

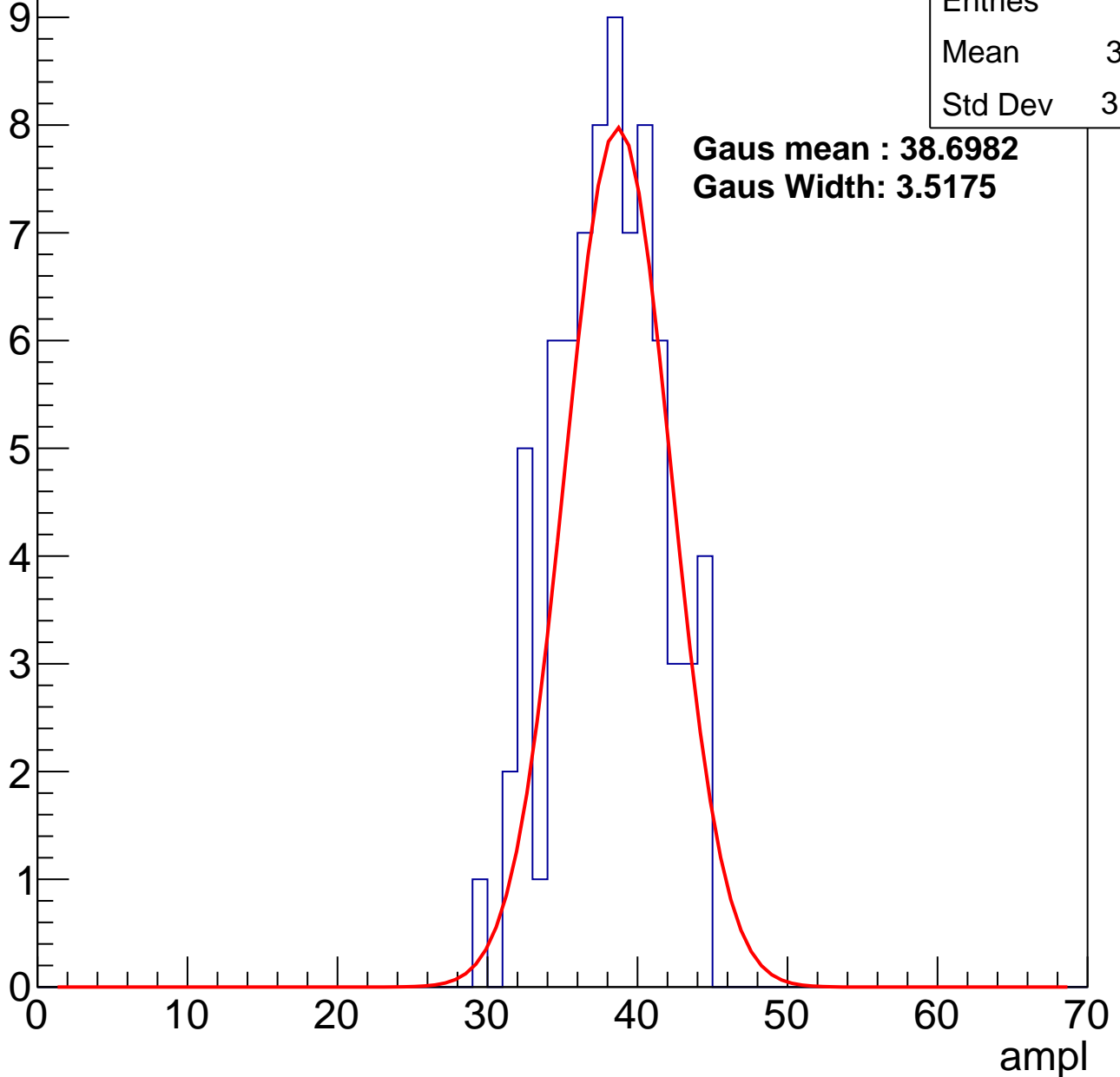
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	76
Mean	37.61
Std Dev	3.476

**Gaus mean : 38.6982**

**Gaus Width: 3.5175**



# B1L103S, U11-ch87, adc2

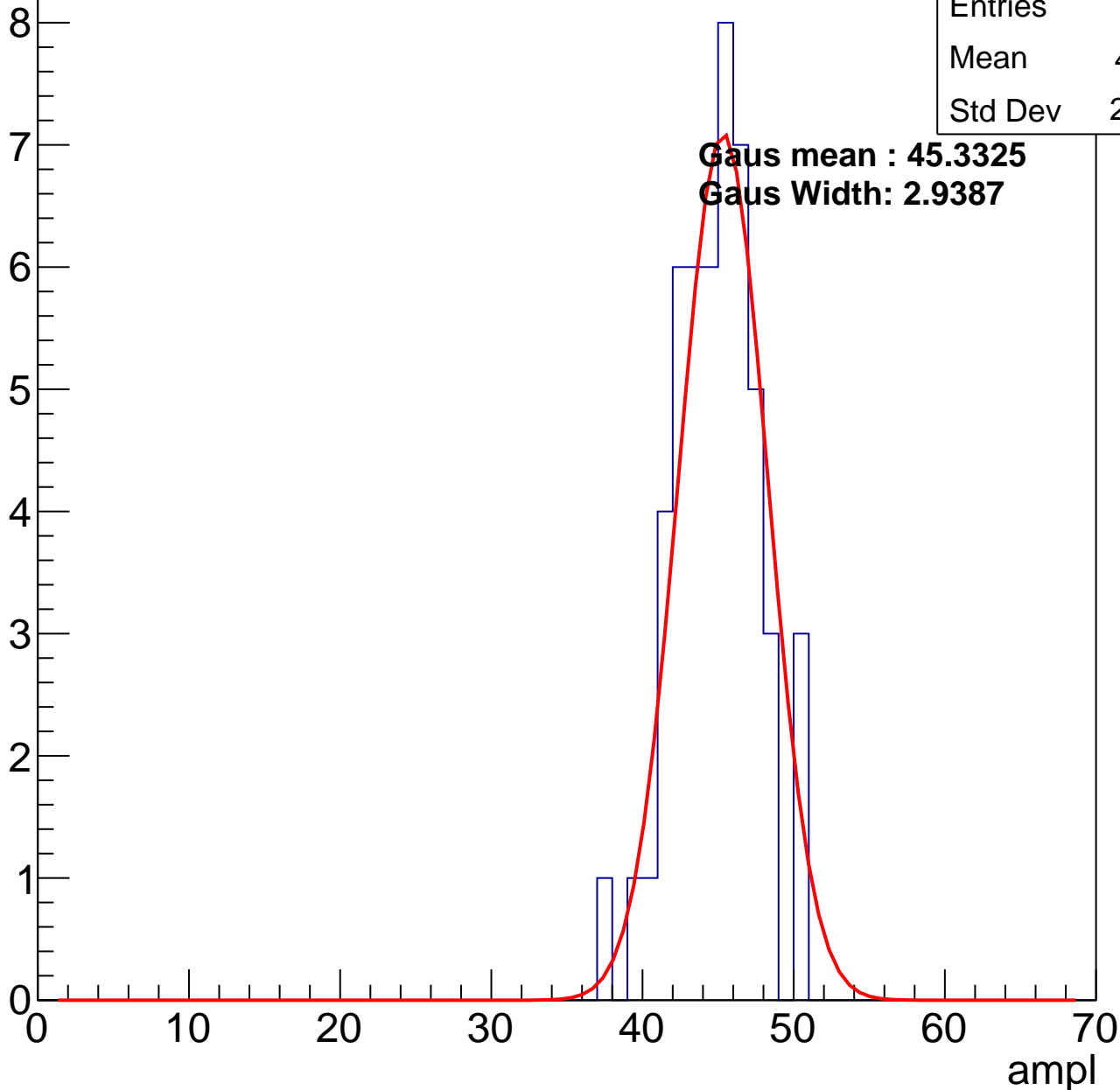
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	51
Mean	44.41
Std Dev	2.745

**Gaus mean : 45.3325**

**Gaus Width: 2.9387**

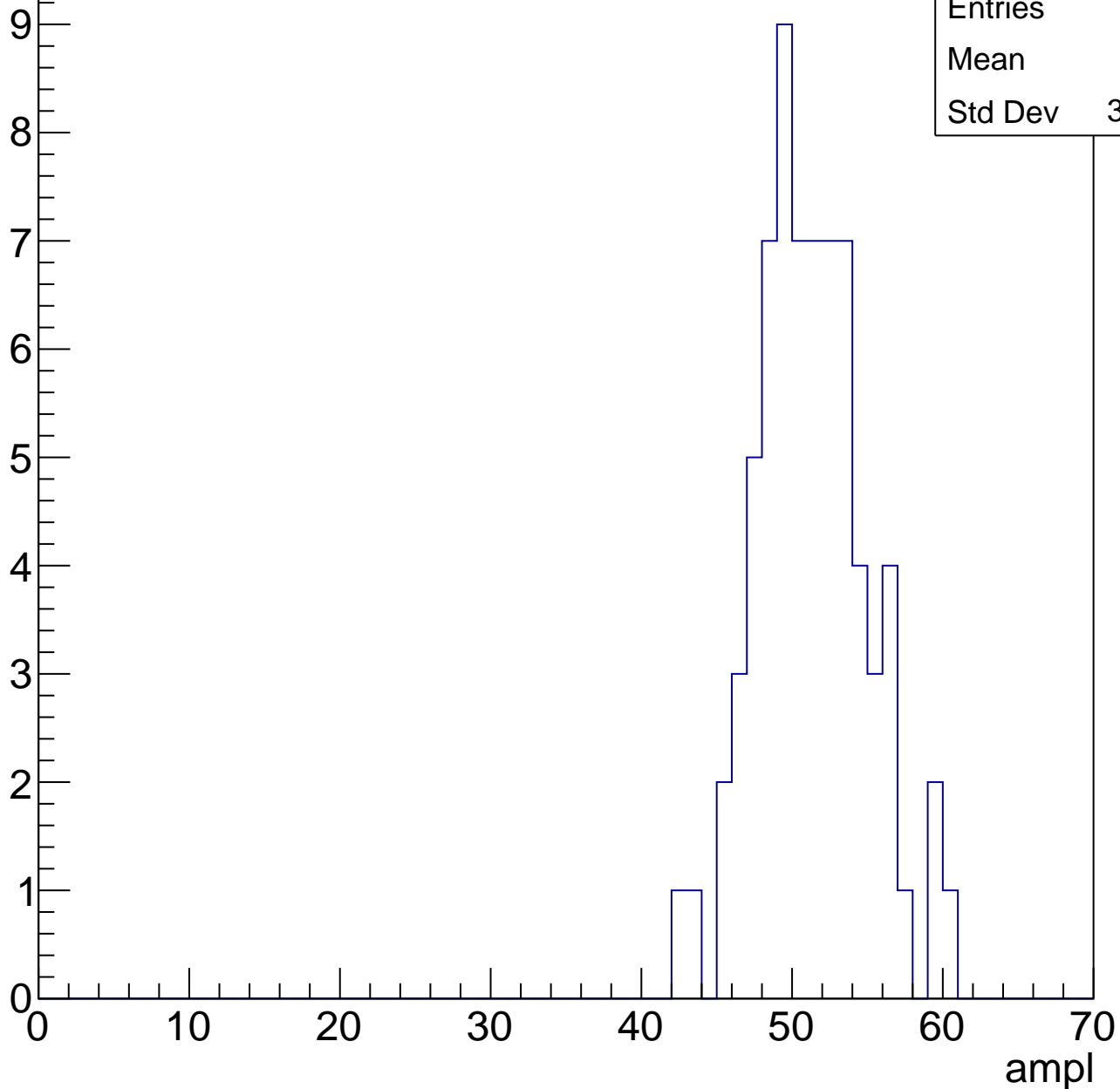


# B1L103S, U11-ch87, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	71
Mean	50.8
Std Dev	3.637

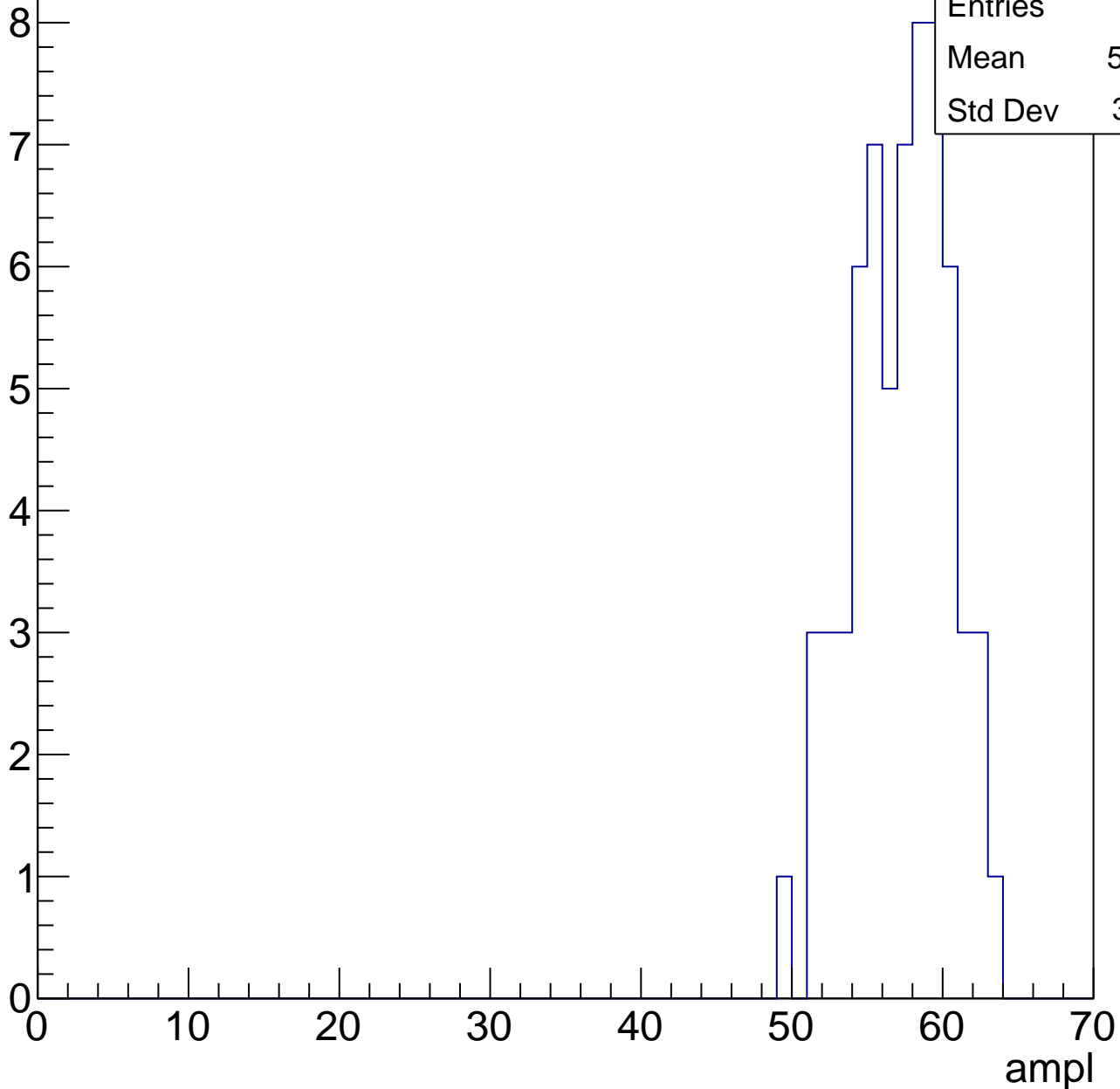


# B1L103S, U11-ch87, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	56.77
Std Dev	3.141

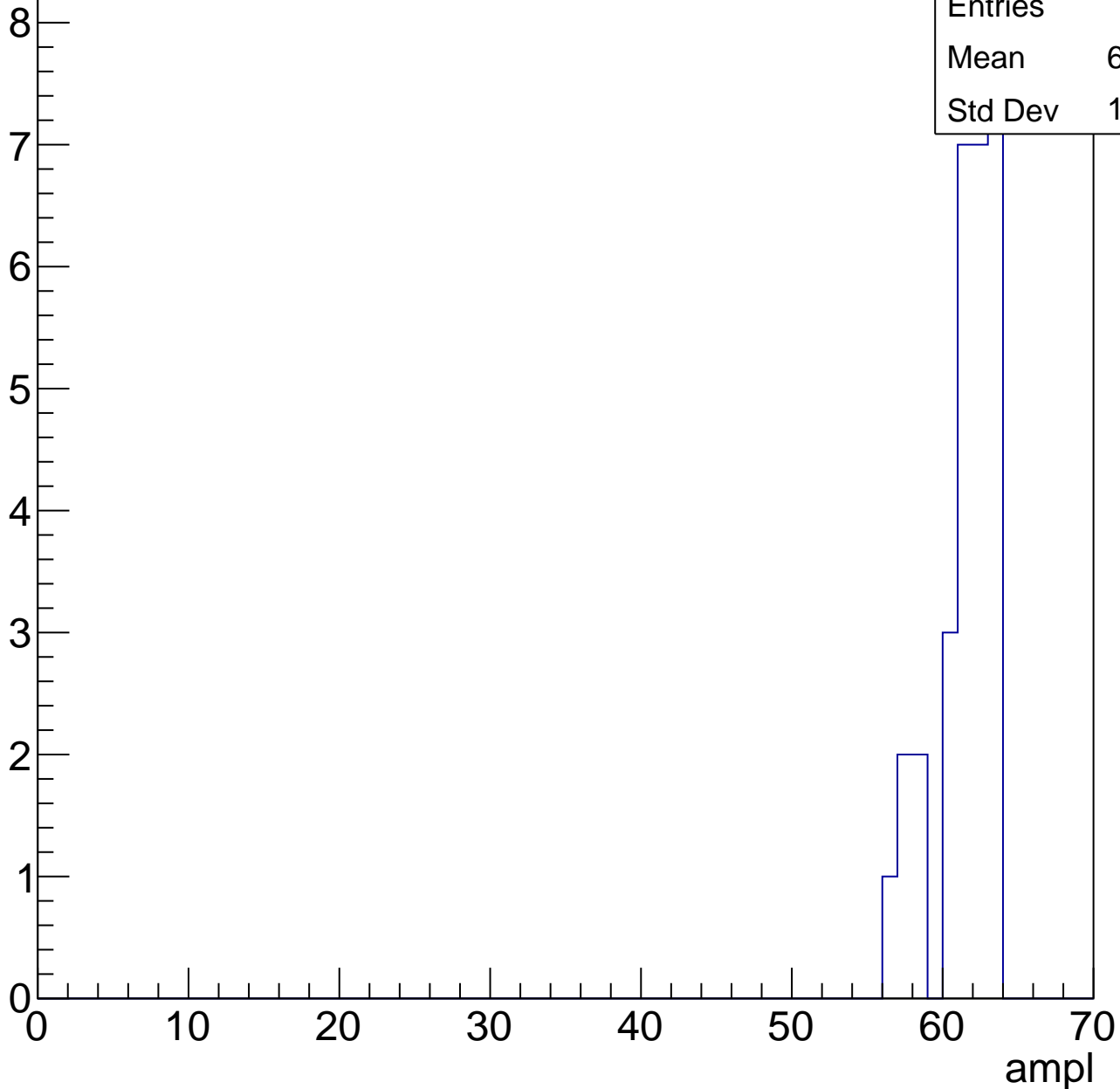


# B1L103S, U11-ch87, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	30
Mean	61.03
Std Dev	1.975



# B1L103S, U11-ch87, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



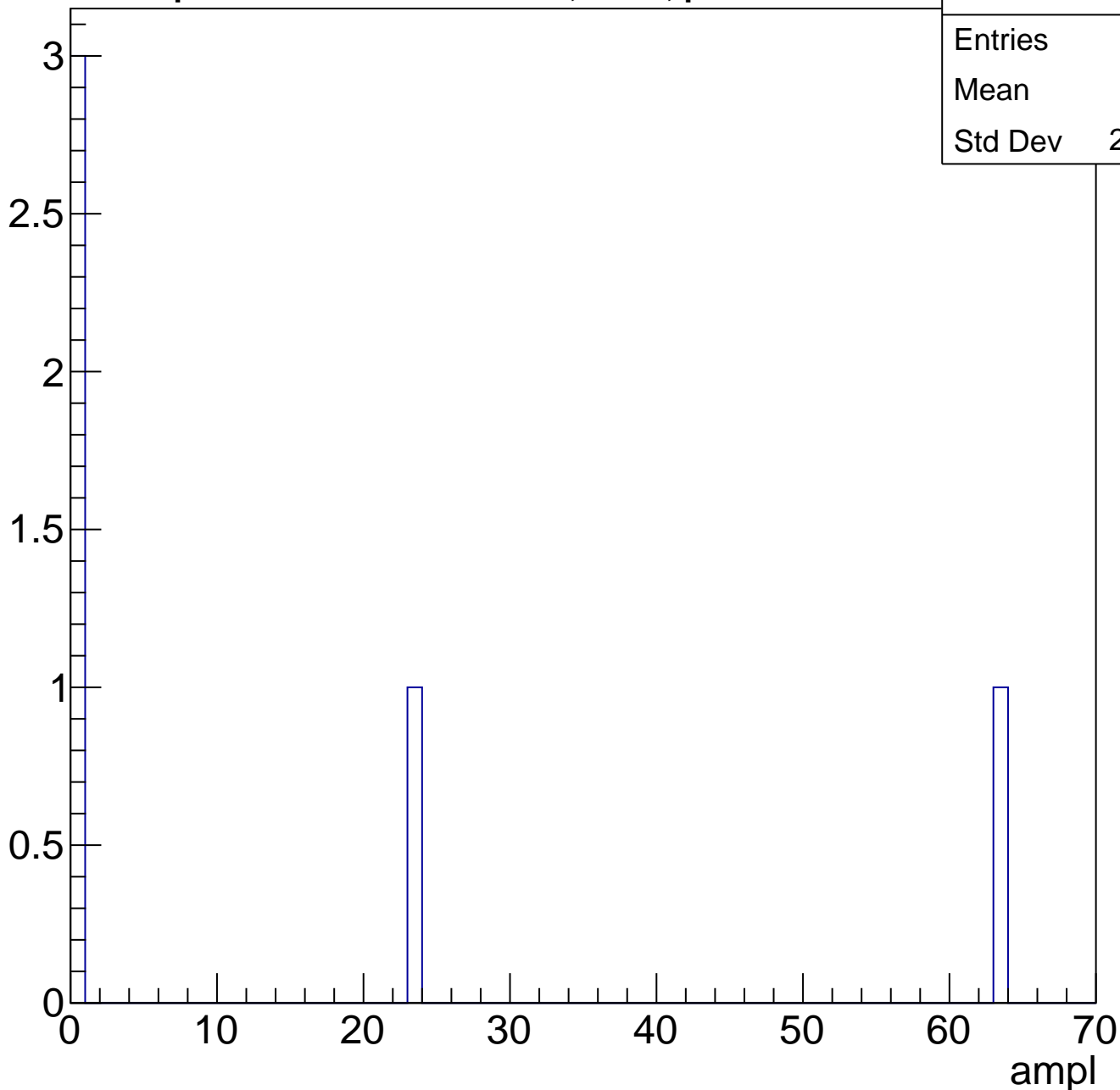
Entries	1
Mean	0
Std Dev	0



# B1L103S, U11-ch87, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	5
Mean	17.2
Std Dev	24.57

# B1L103S, U11-ch88, adc0

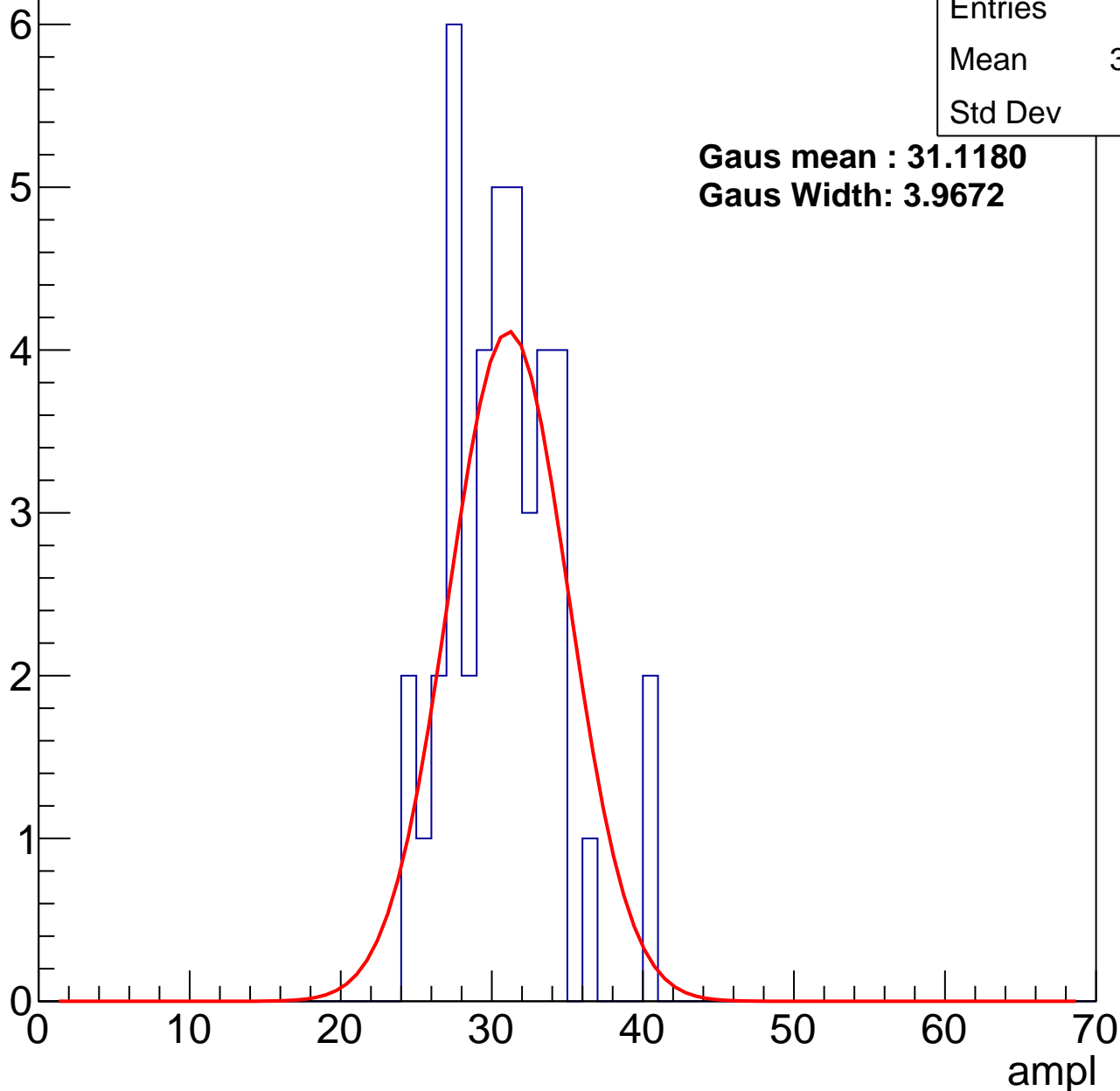
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	41
Mean	30.34
Std Dev	3.64

**Gaus mean : 31.1180**

**Gaus Width: 3.9672**



# B1L103S, U11-ch88, adc1

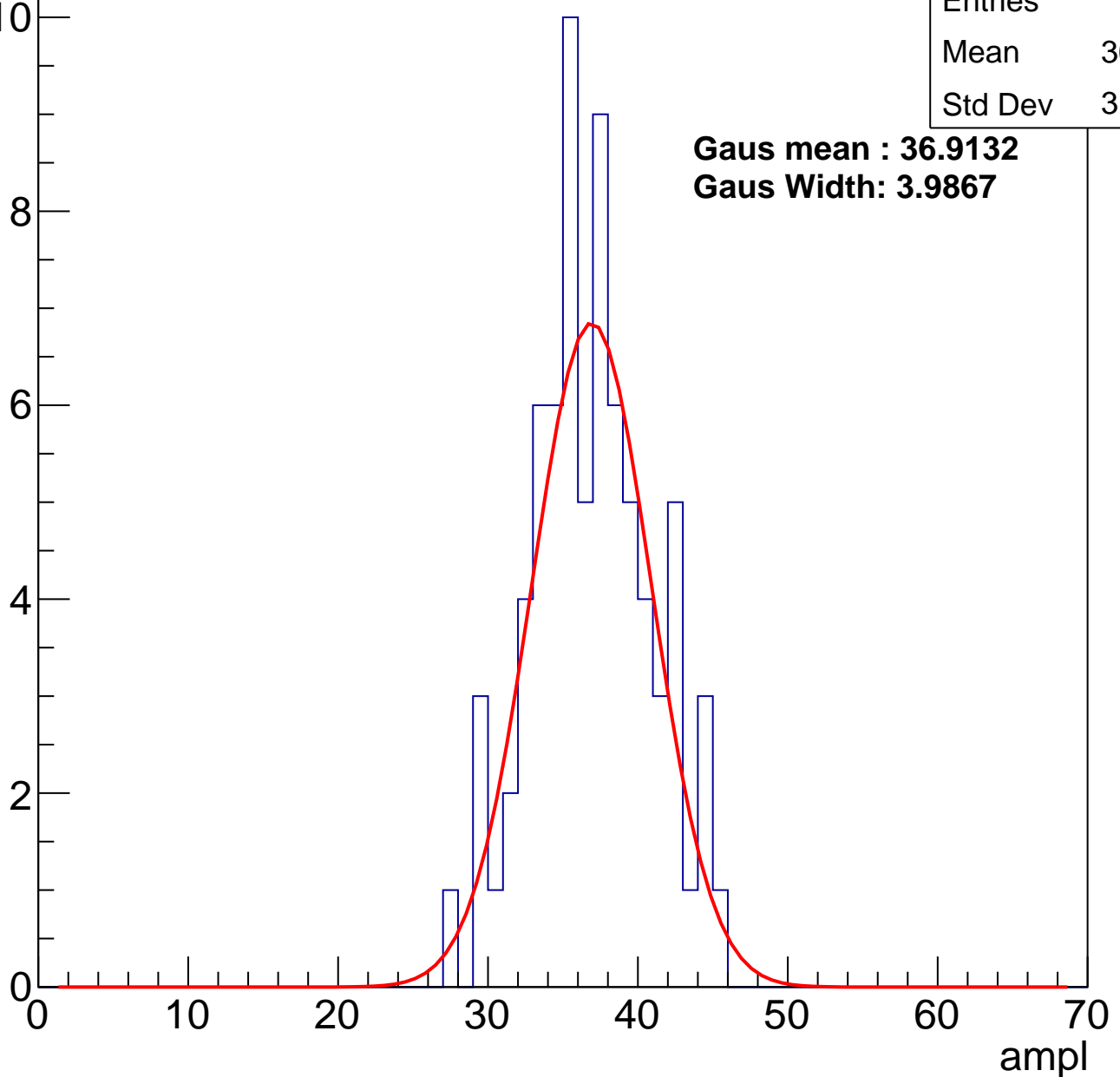
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	75
Mean	36.47
Std Dev	3.947

**Gaus mean : 36.9132**

**Gaus Width: 3.9867**



# B1L103S, U11-ch88, adc2

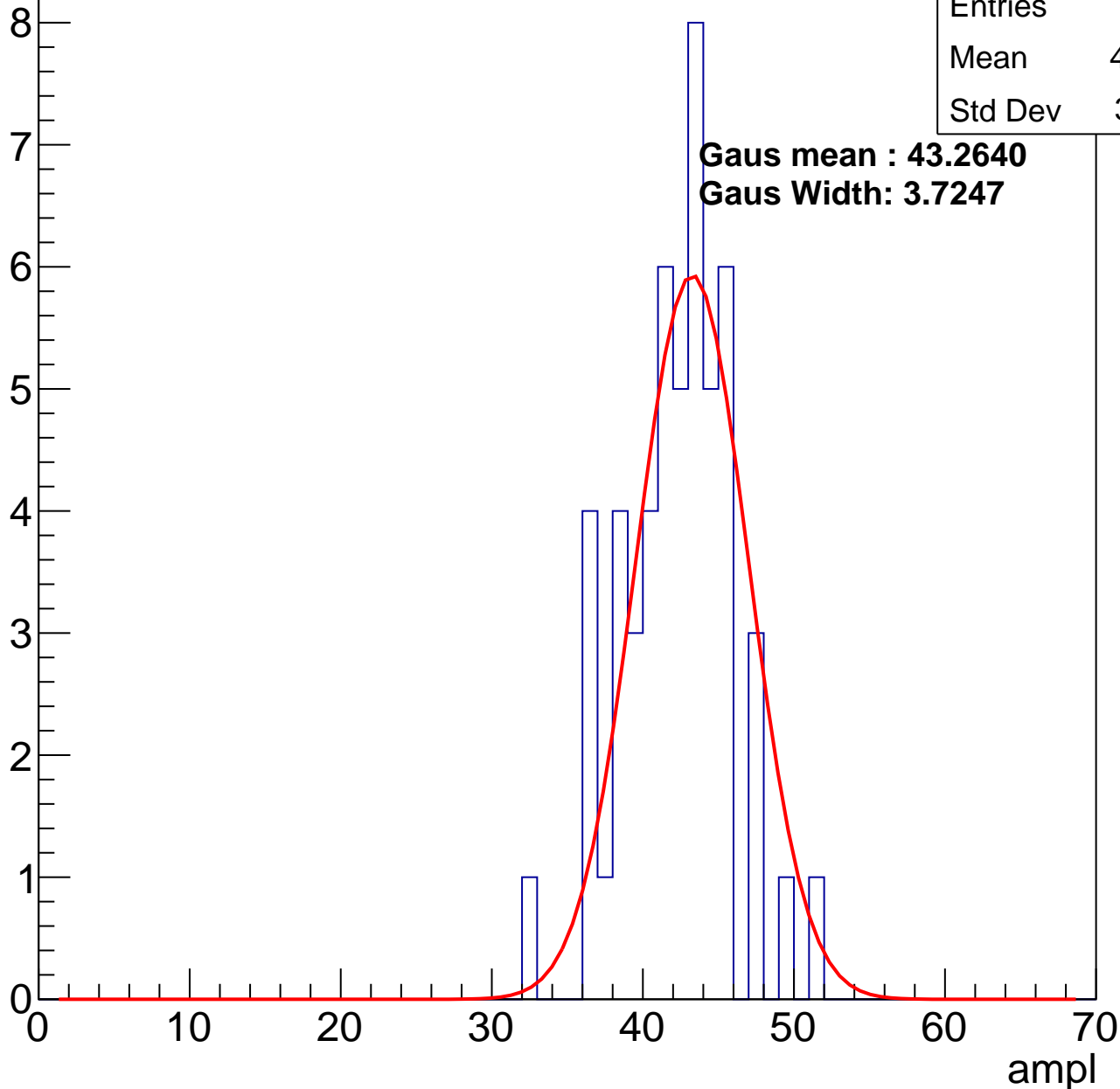
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	52
Mean	41.79
Std Dev	3.581

**Gaus mean : 43.2640**

**Gaus Width: 3.7247**



# B1L103S, U11-ch88, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	86
Mean	49.84
Std Dev	4.148

Entry

10

8

6

4

2

0

0

10

20

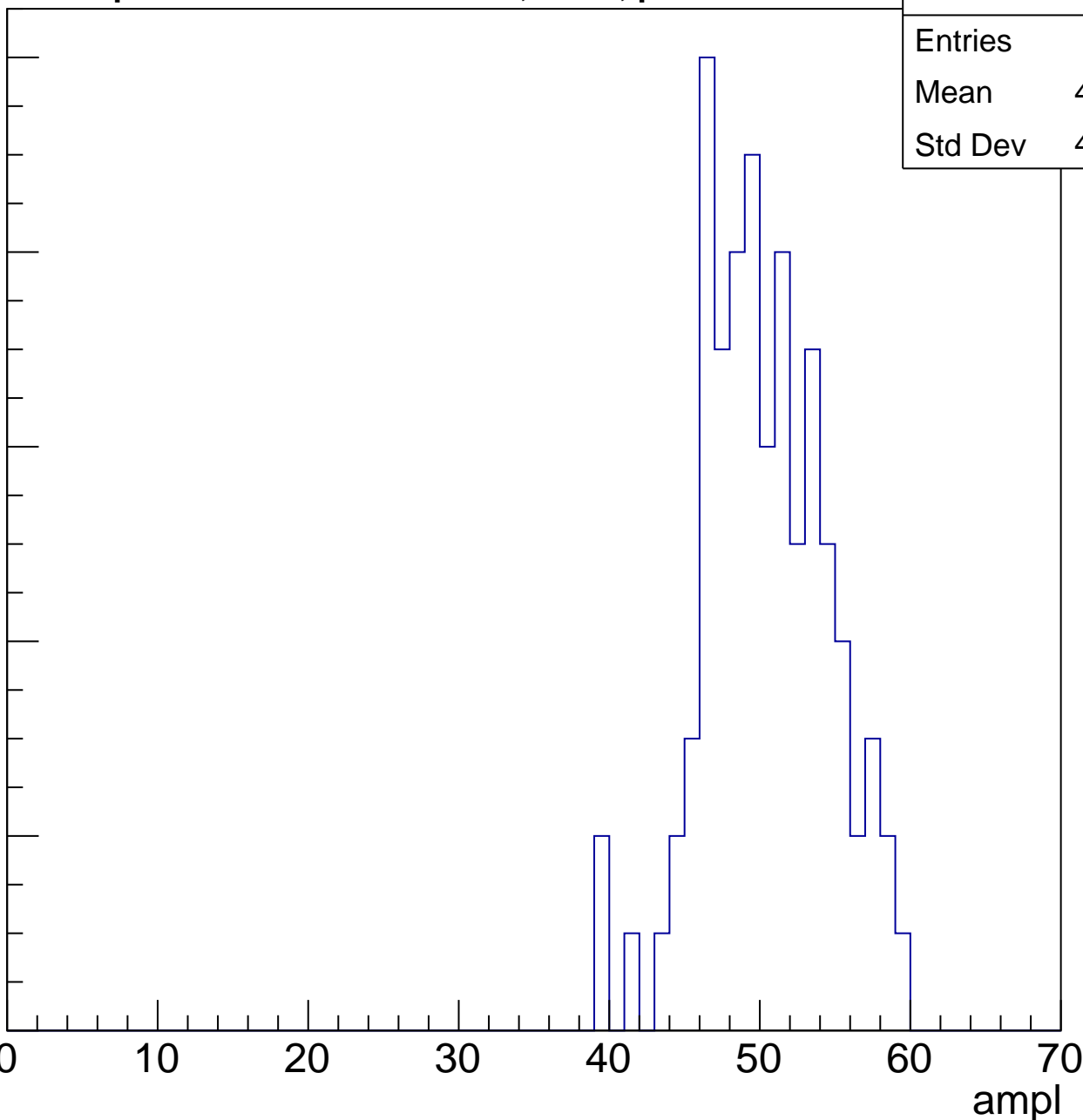
30

40

50

60

ampl

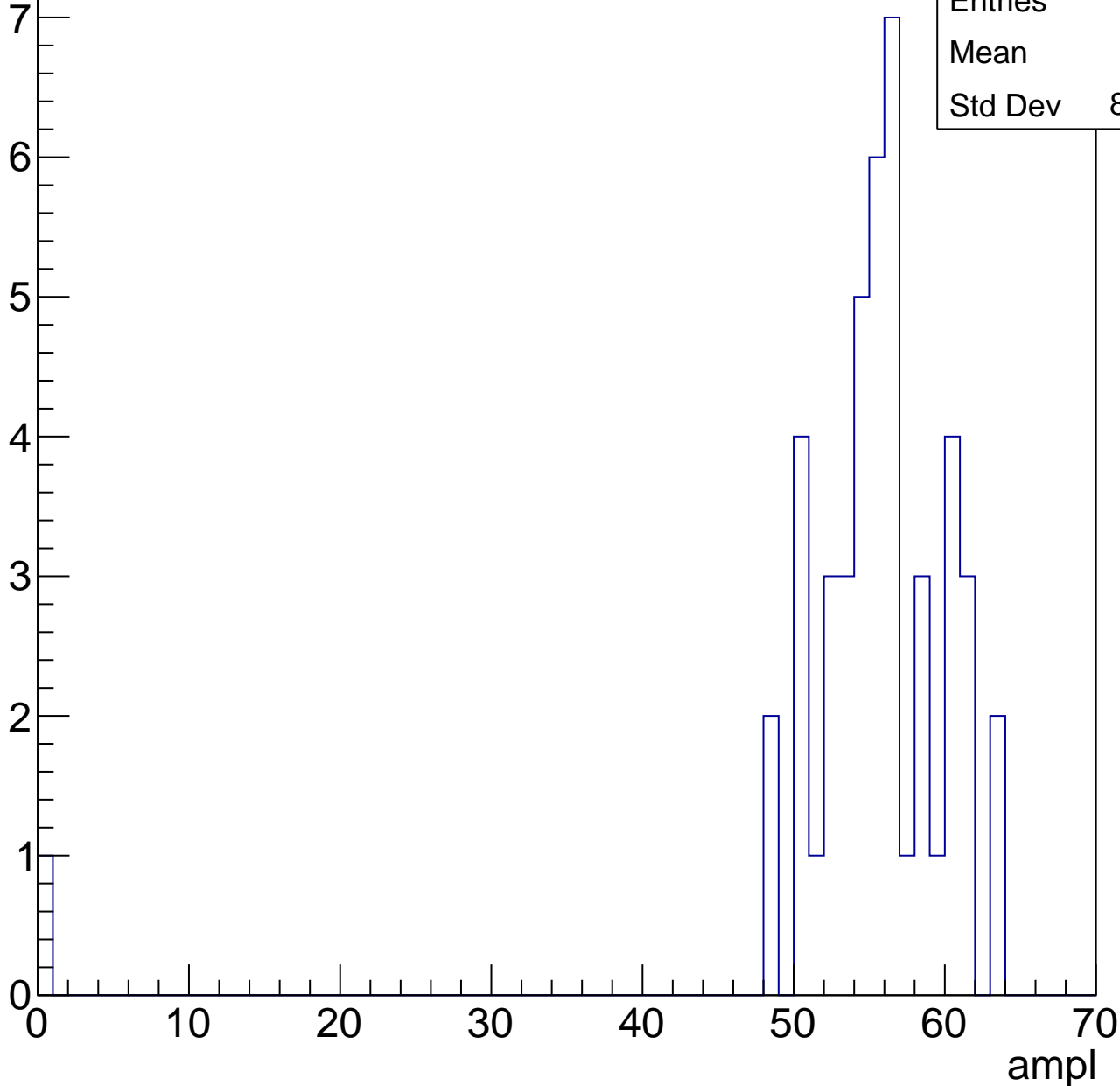


# B1L103S, U11-ch88, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	46
Mean	54.2
Std Dev	8.899



# B1L103S, U11-ch88, adc5

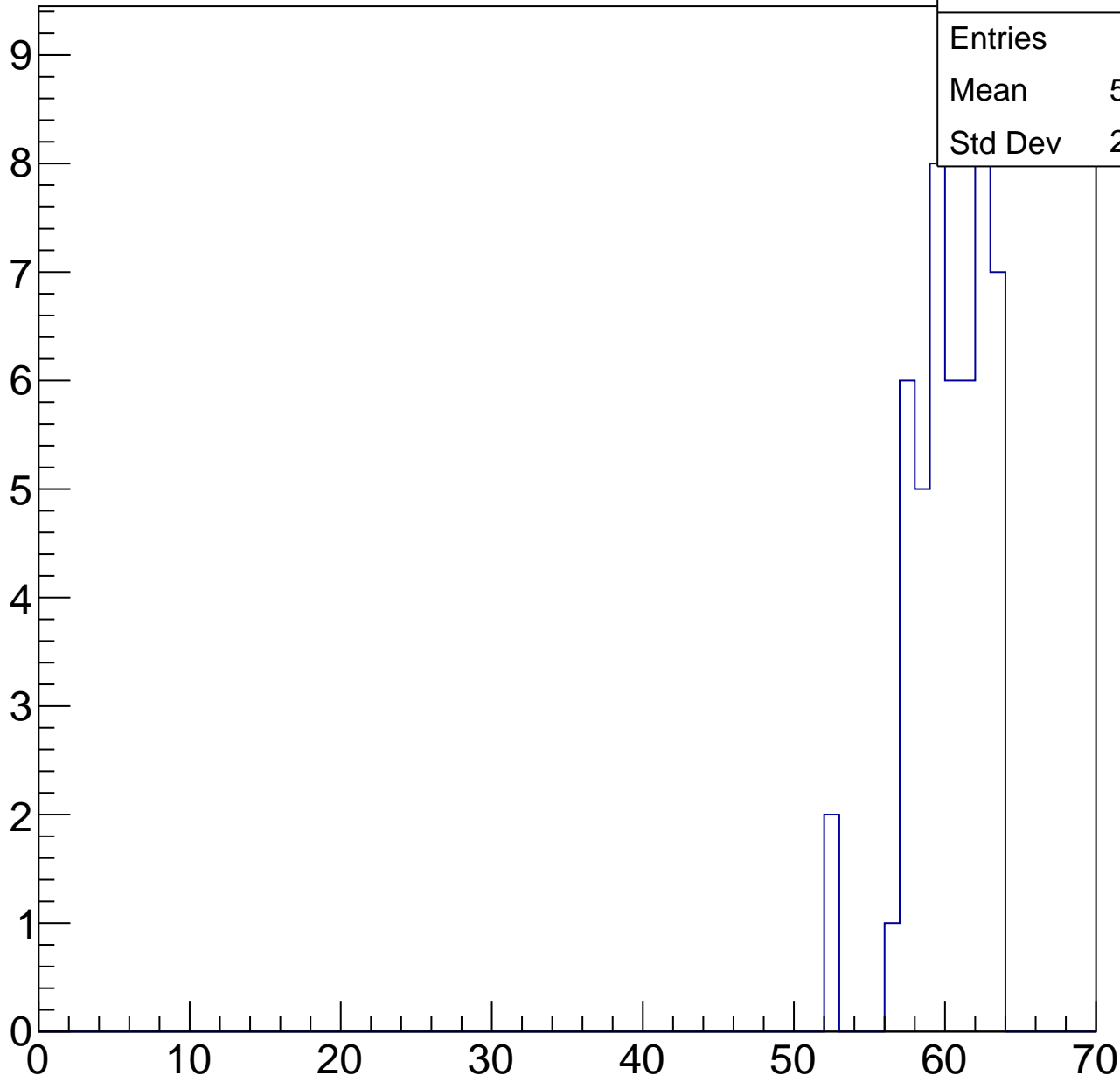
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	50
Mean	59.78
Std Dev	2.564

ampl



# B1L103S, U11-ch88, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U11-ch88, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U11-ch89, adc0

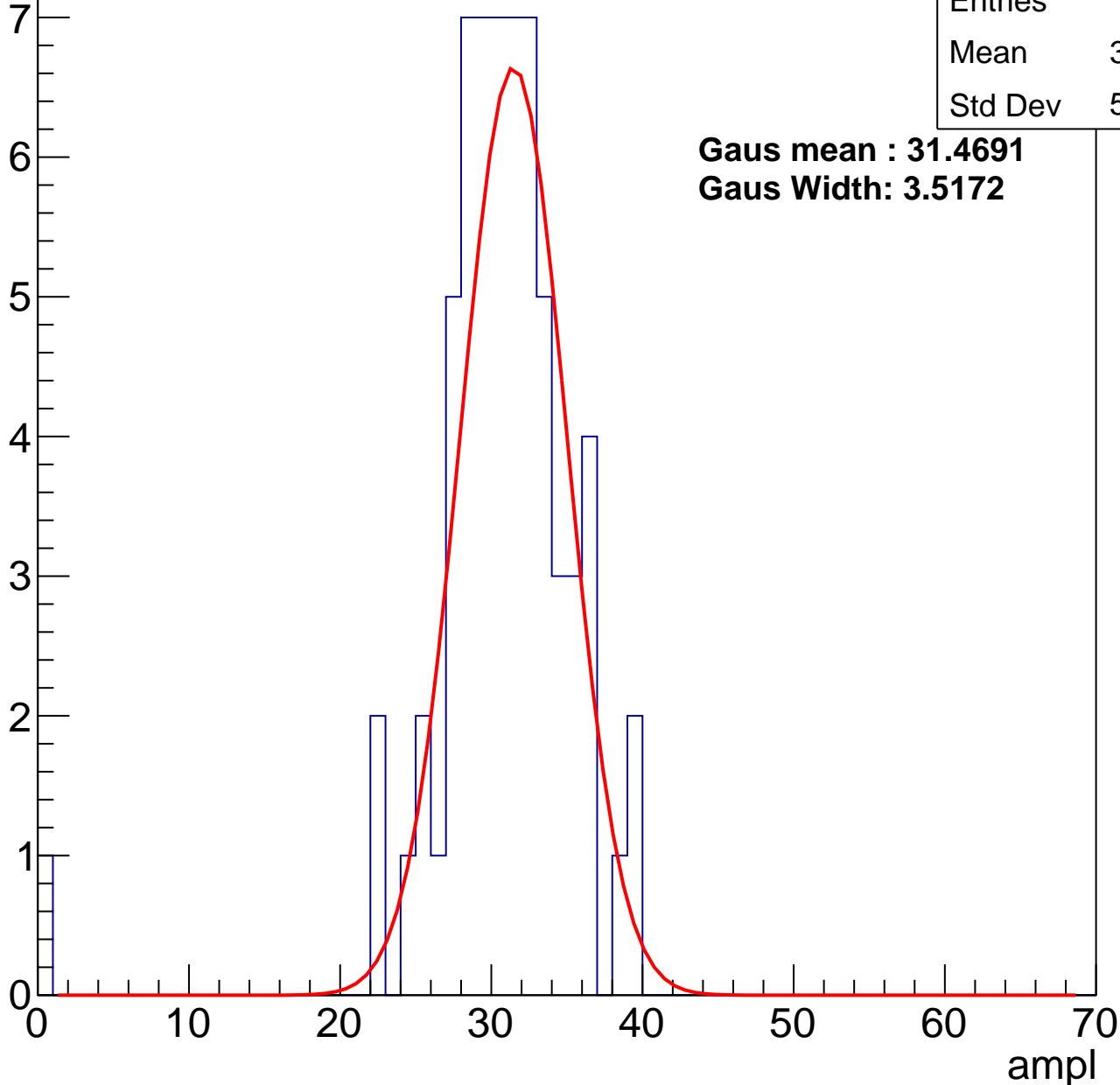
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	30.17
Std Dev	5.235

**Gaus mean : 31.4691**

**Gaus Width: 3.5172**



# B1L103S, U11-ch89, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	91
Mean	38.37
Std Dev	4.078

**Gaus mean : 39.0993**

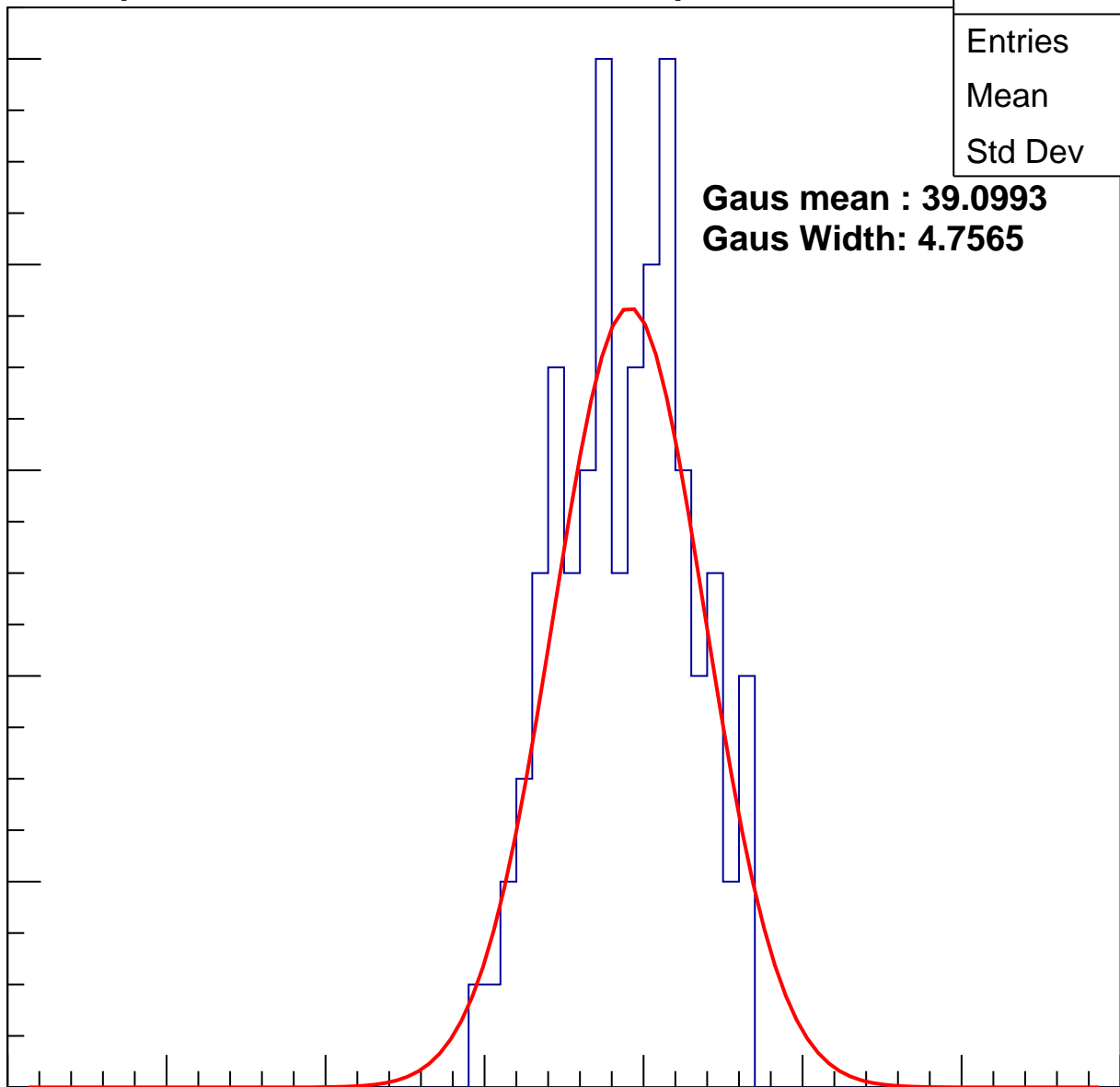
**Gaus Width: 4.7565**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U11-ch89, adc2

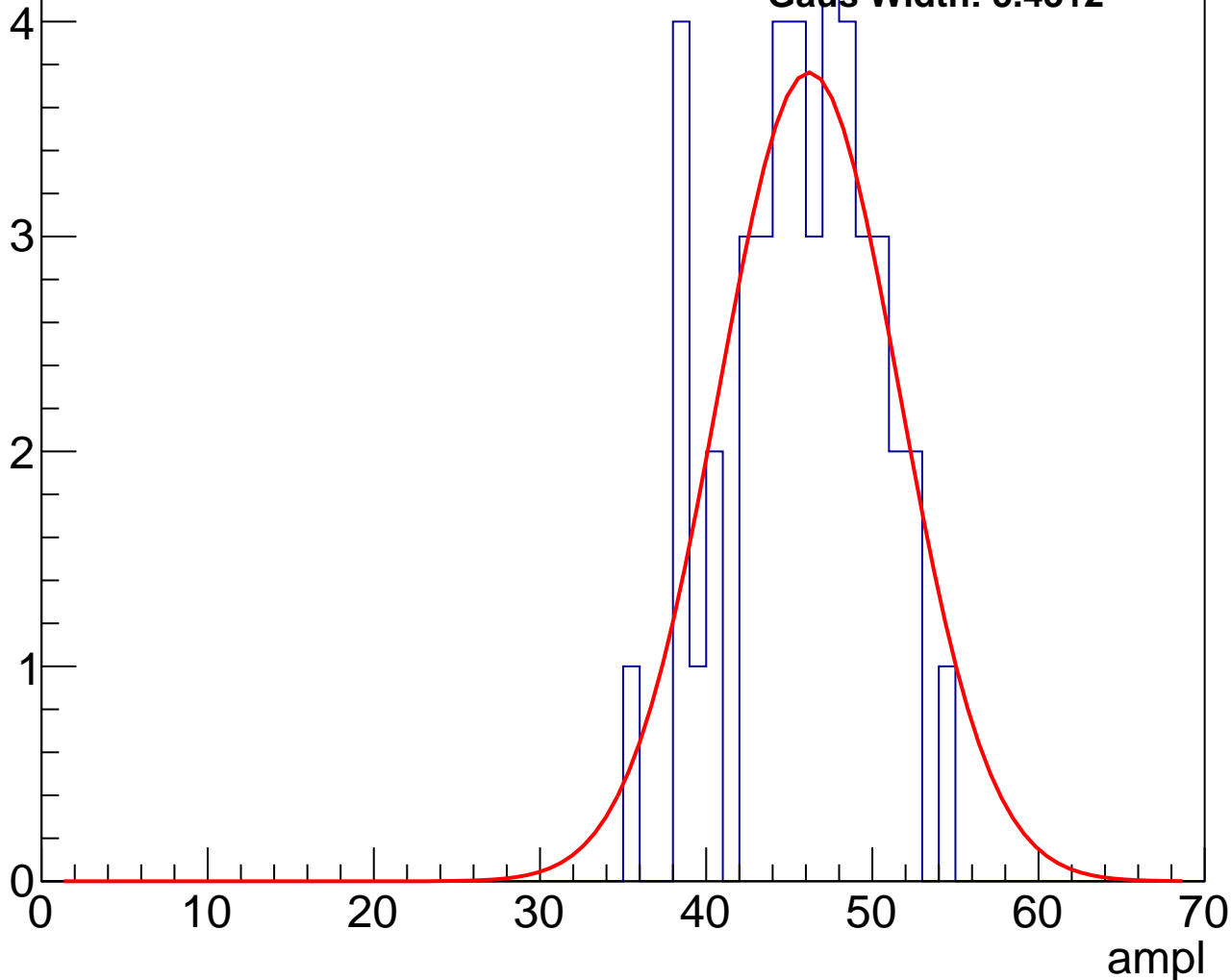
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	45
Mean	45.31
Std Dev	4.355

**Gaus mean : 46.1936**

**Gaus Width: 5.4312**

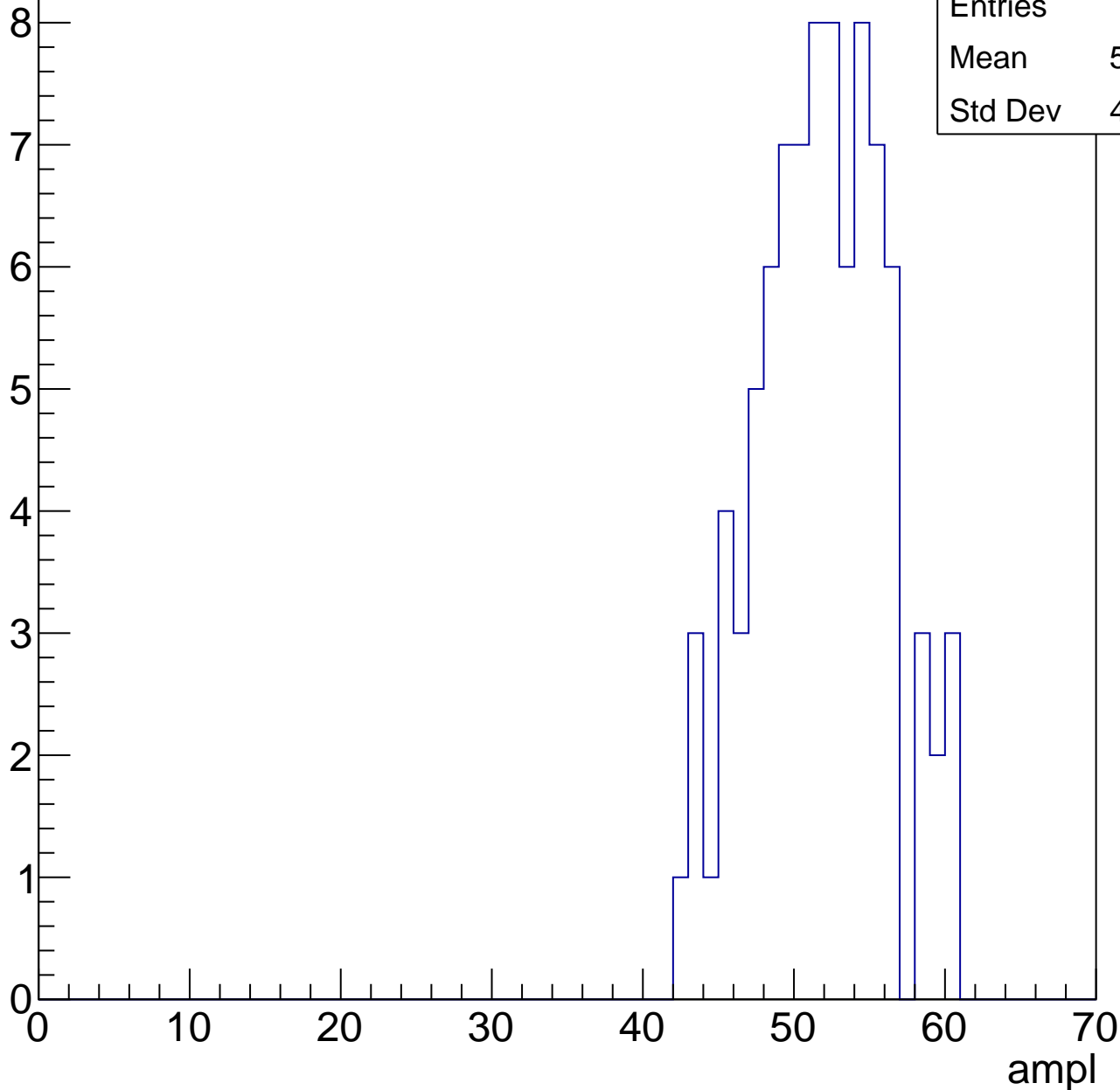


# B1L103S, U11-ch89, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

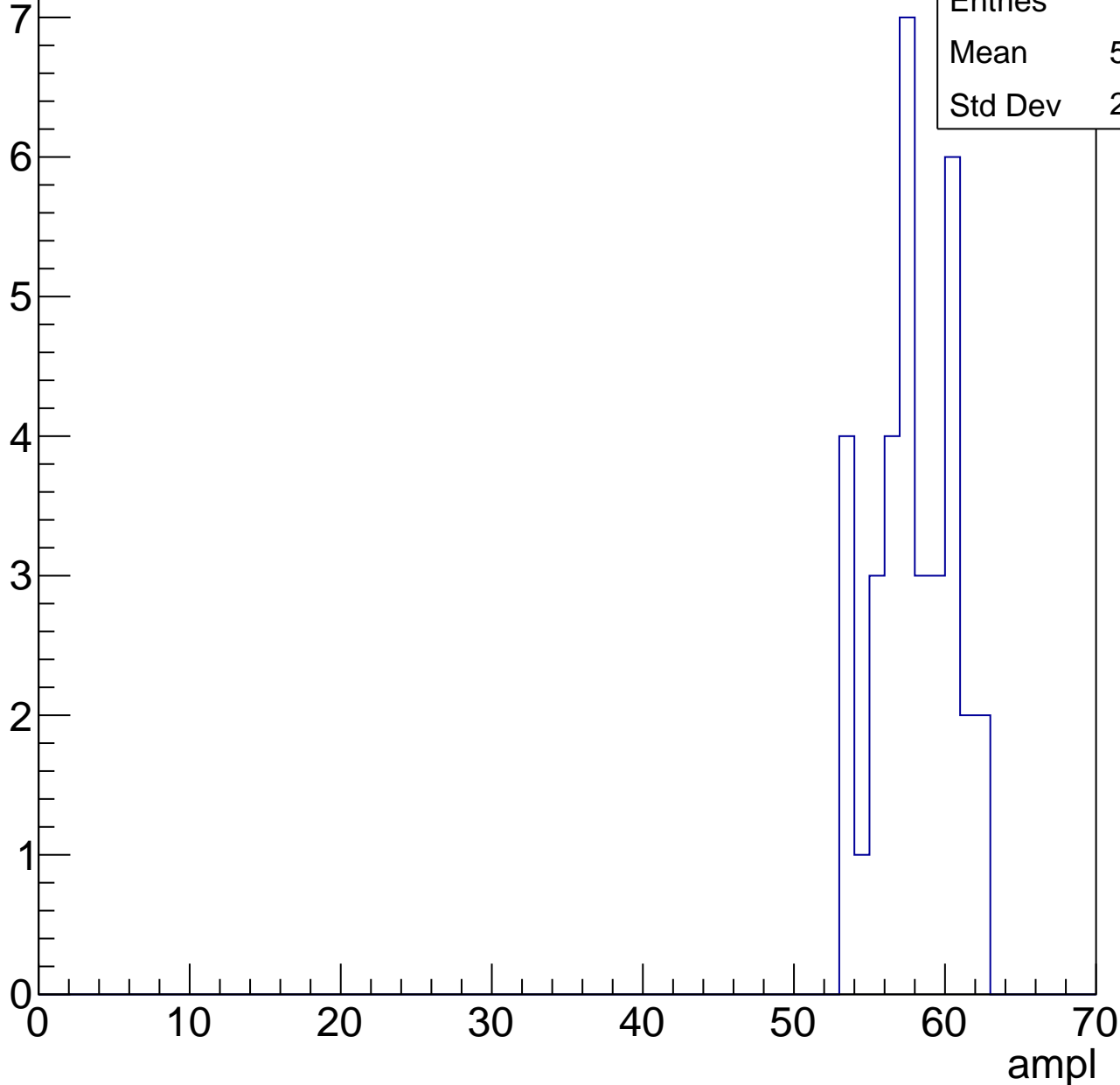
Entries	88
Mean	51.32
Std Dev	4.244



# B1L103S, U11-ch89, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

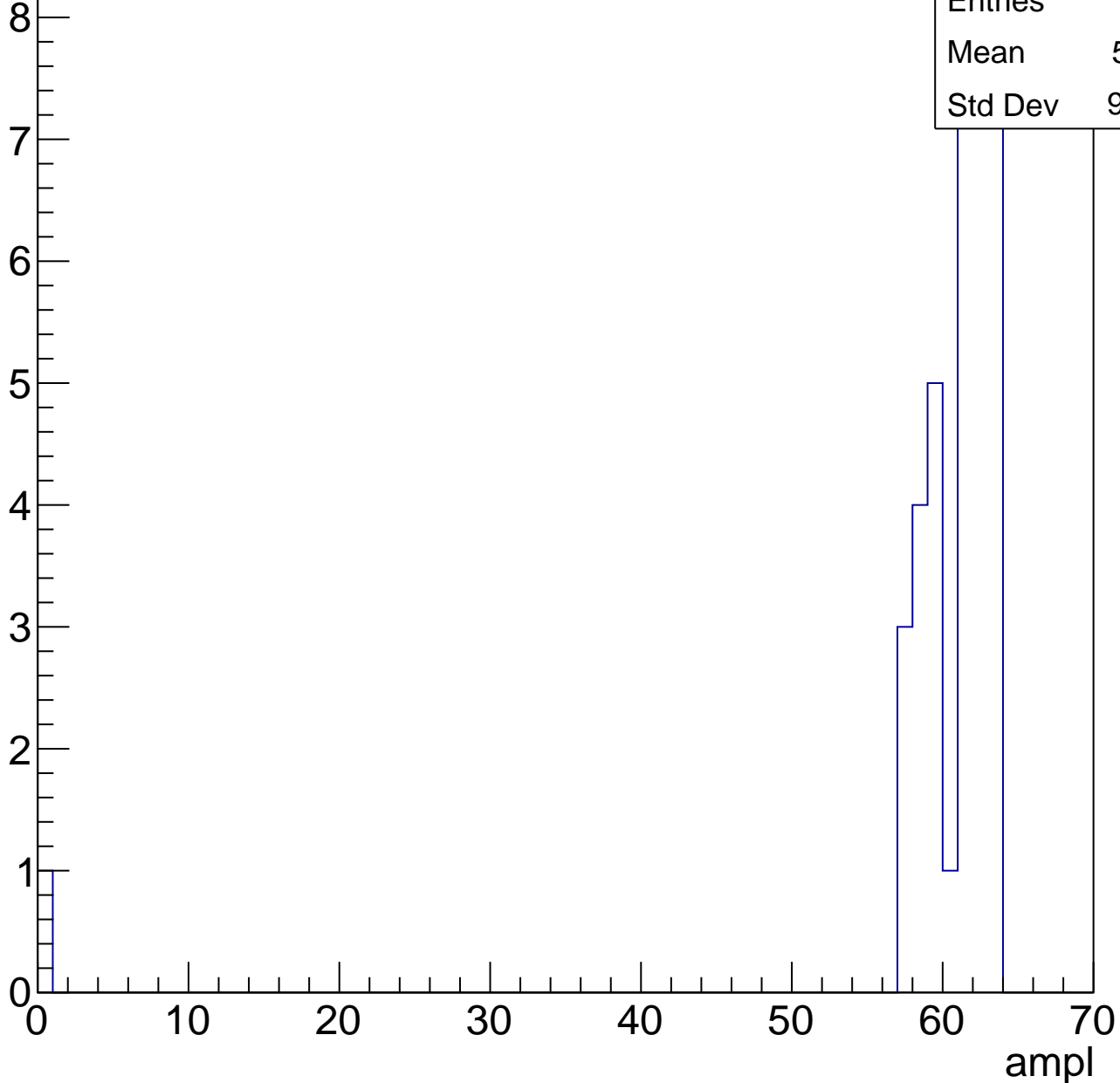


# B1L103S, U11-ch89, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	38
Mean	59.11
Std Dev	9.907



# B1L103S, U11-ch89, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U11-ch89, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L103S, U11-ch90, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	81
Mean	29.25
Std Dev	3.717

**Gaus mean : 29.6877**

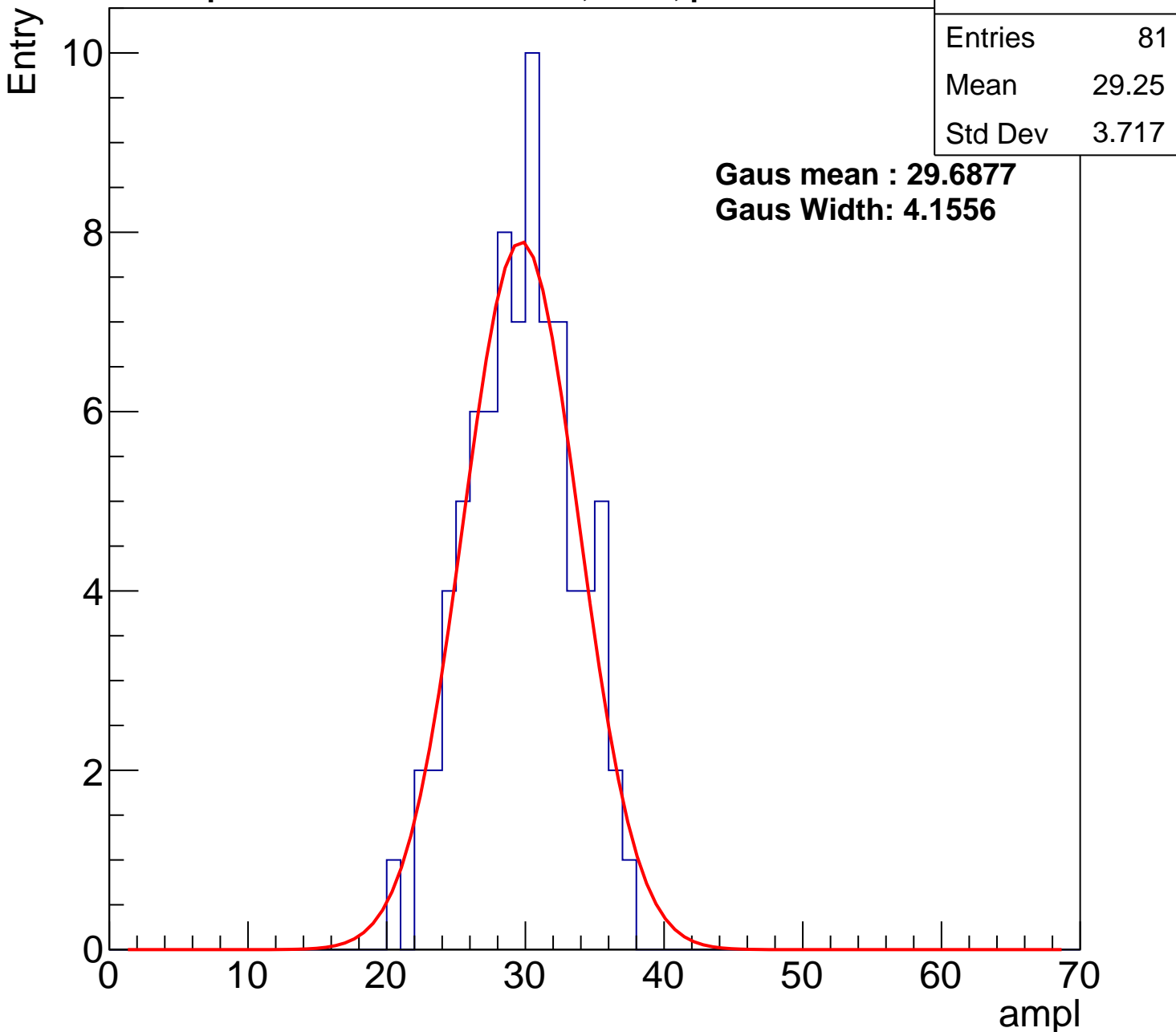
**Gaus Width: 4.1556**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U11-ch90, adc1

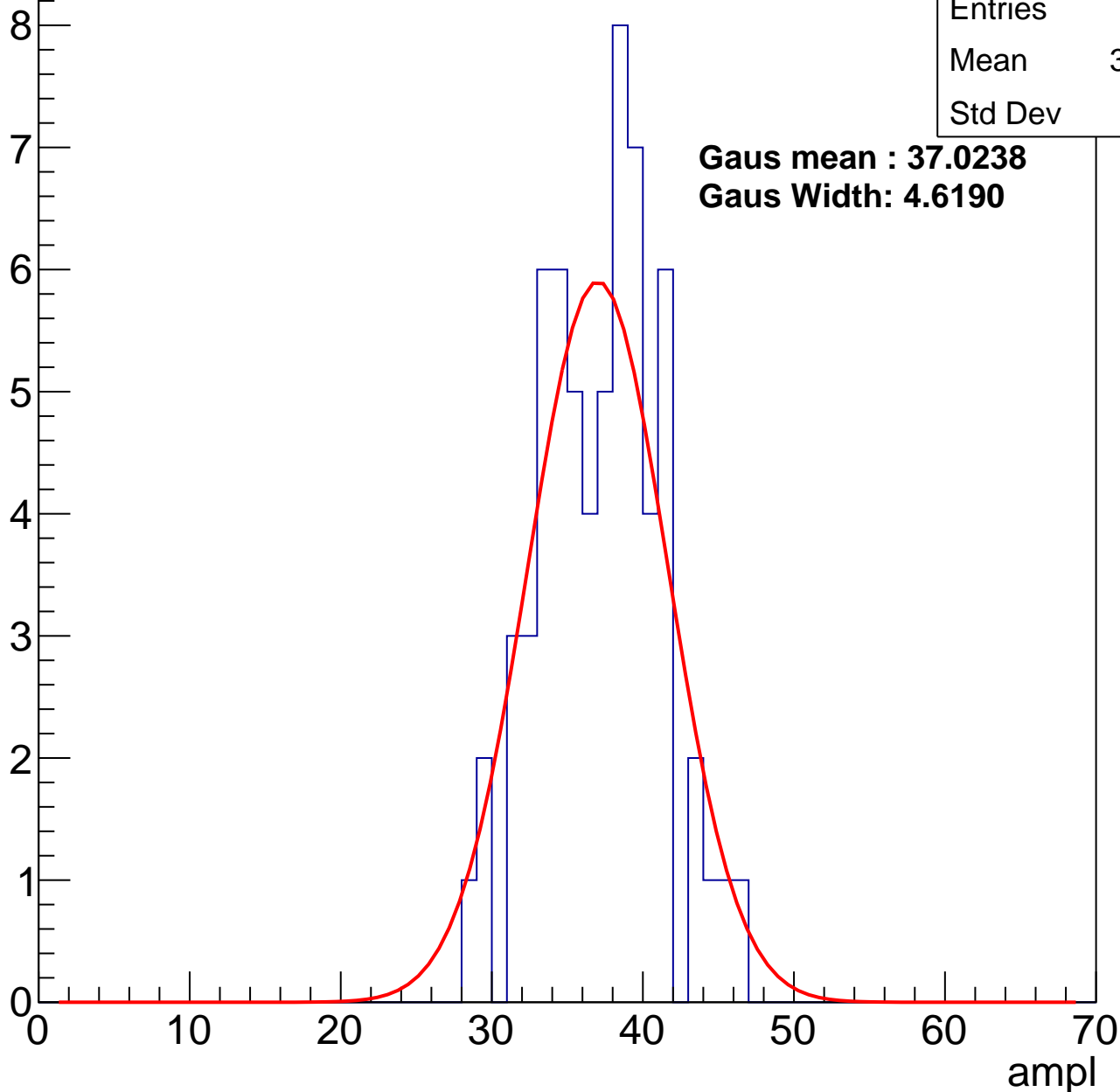
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	36.69
Std Dev	3.91

**Gaus mean : 37.0238**

**Gaus Width: 4.6190**



# B1L103S, U11-ch90, adc2

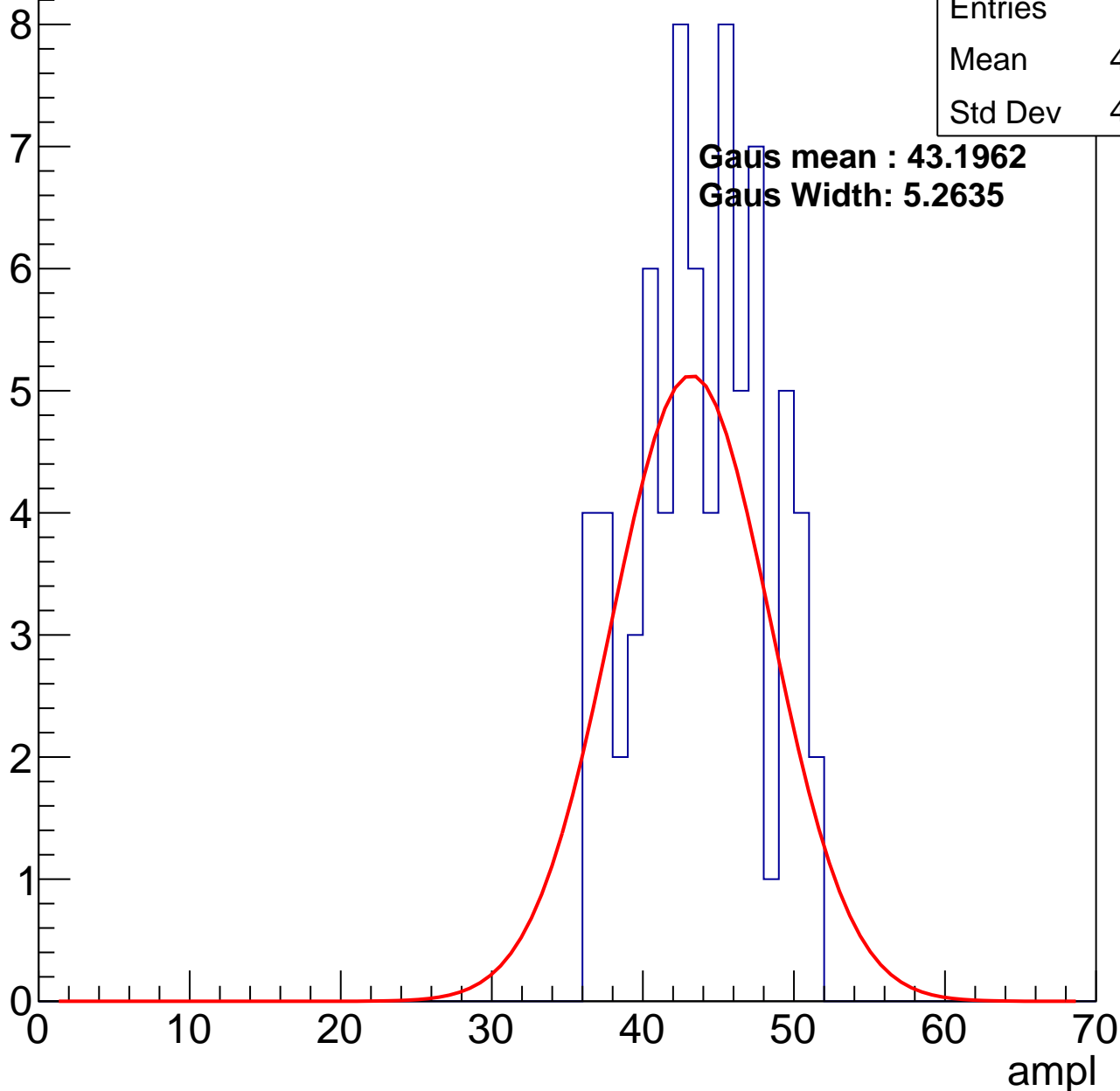
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	73
Mean	43.47
Std Dev	4.092

**Gaus mean : 43.1962**

**Gaus Width: 5.2635**

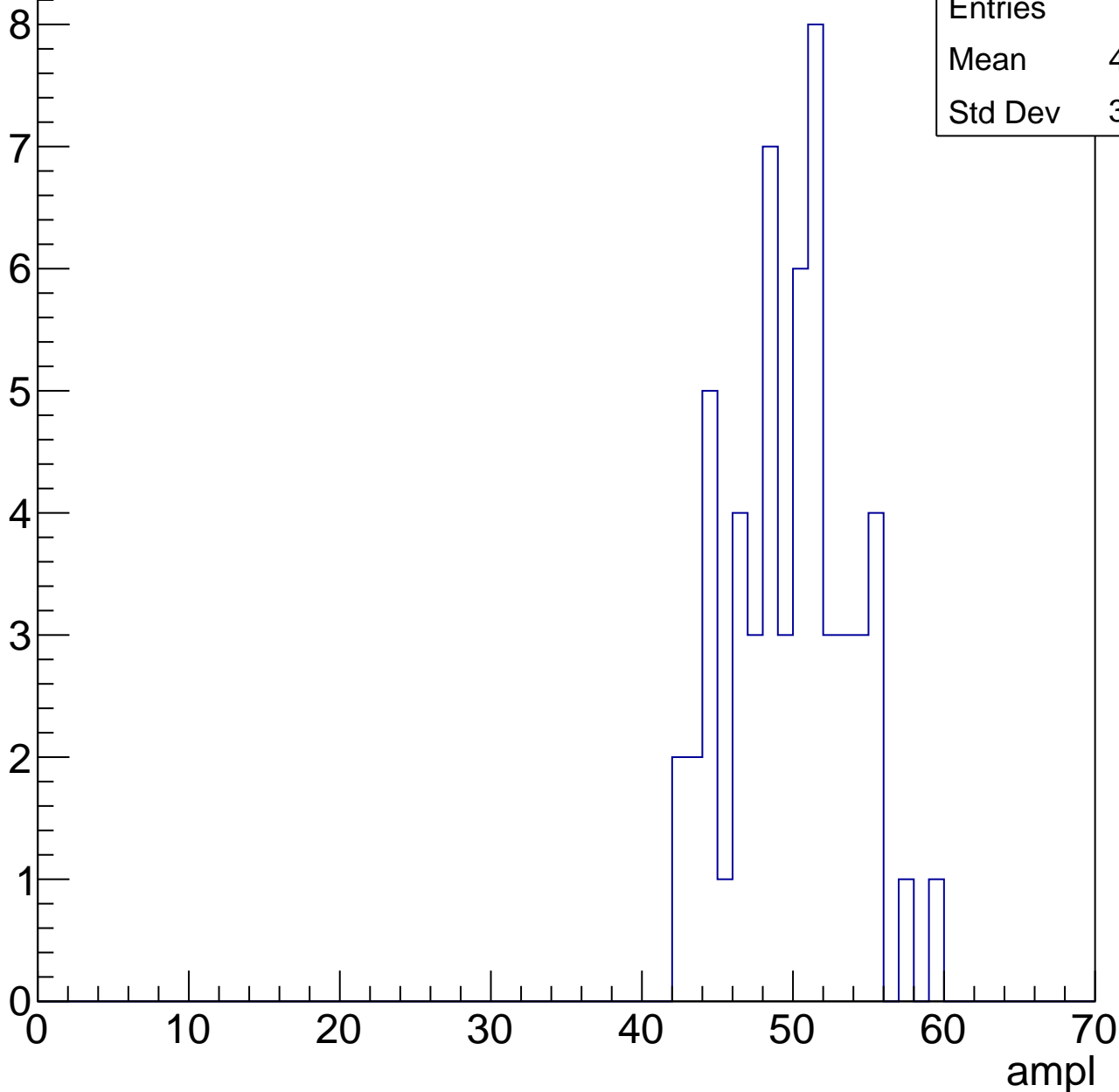


# B1L103S, U11-ch90, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

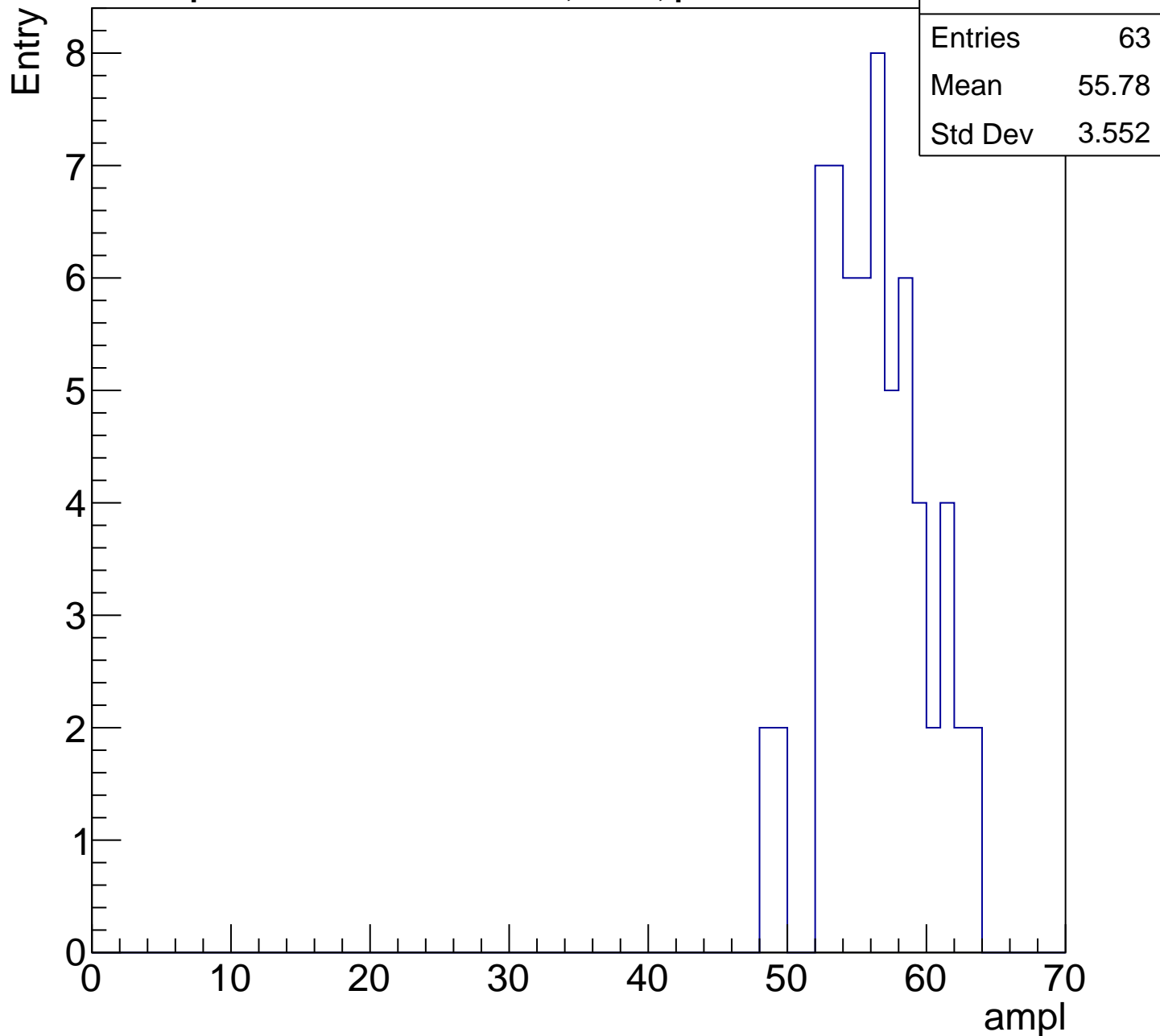
Entry

Entries	56
Mean	49.36
Std Dev	3.907



# B1L103S, U11-ch90, adc4

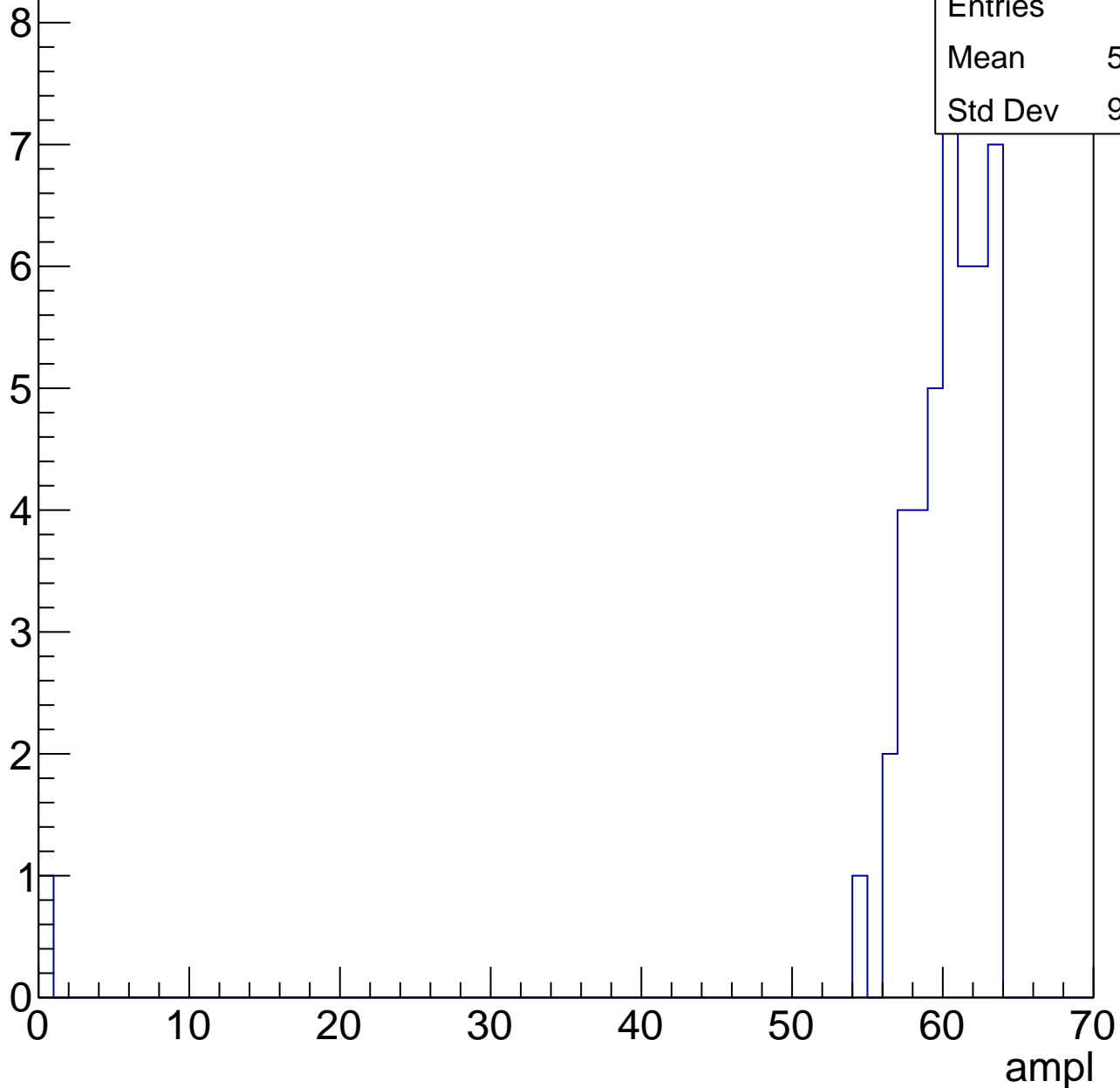
calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U11-ch90, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U11-ch90, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U11-ch90, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L103S, U11-ch91, adc0

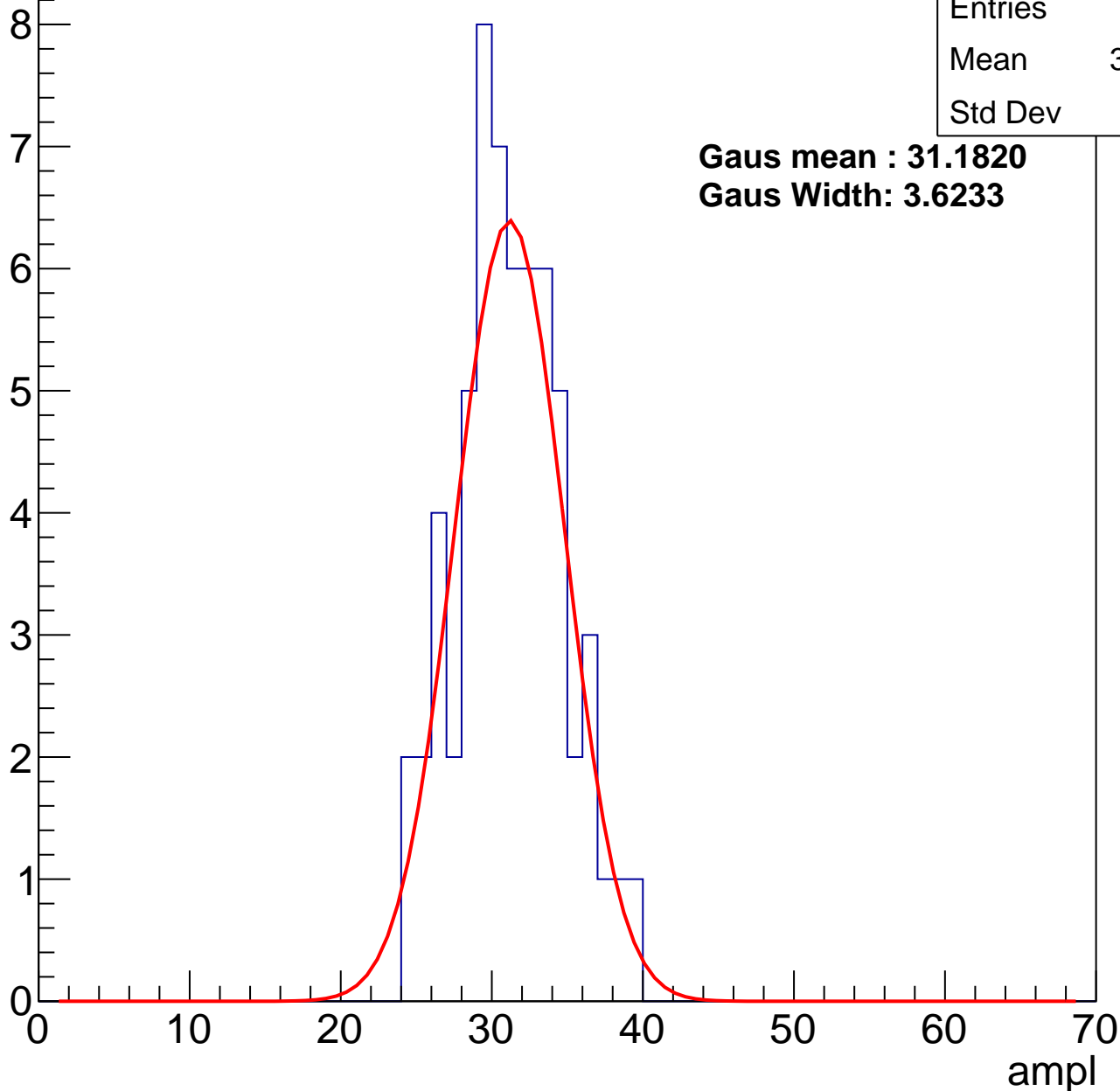
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	61
Mean	30.75
Std Dev	3.42

**Gaus mean : 31.1820**

**Gaus Width: 3.6233**



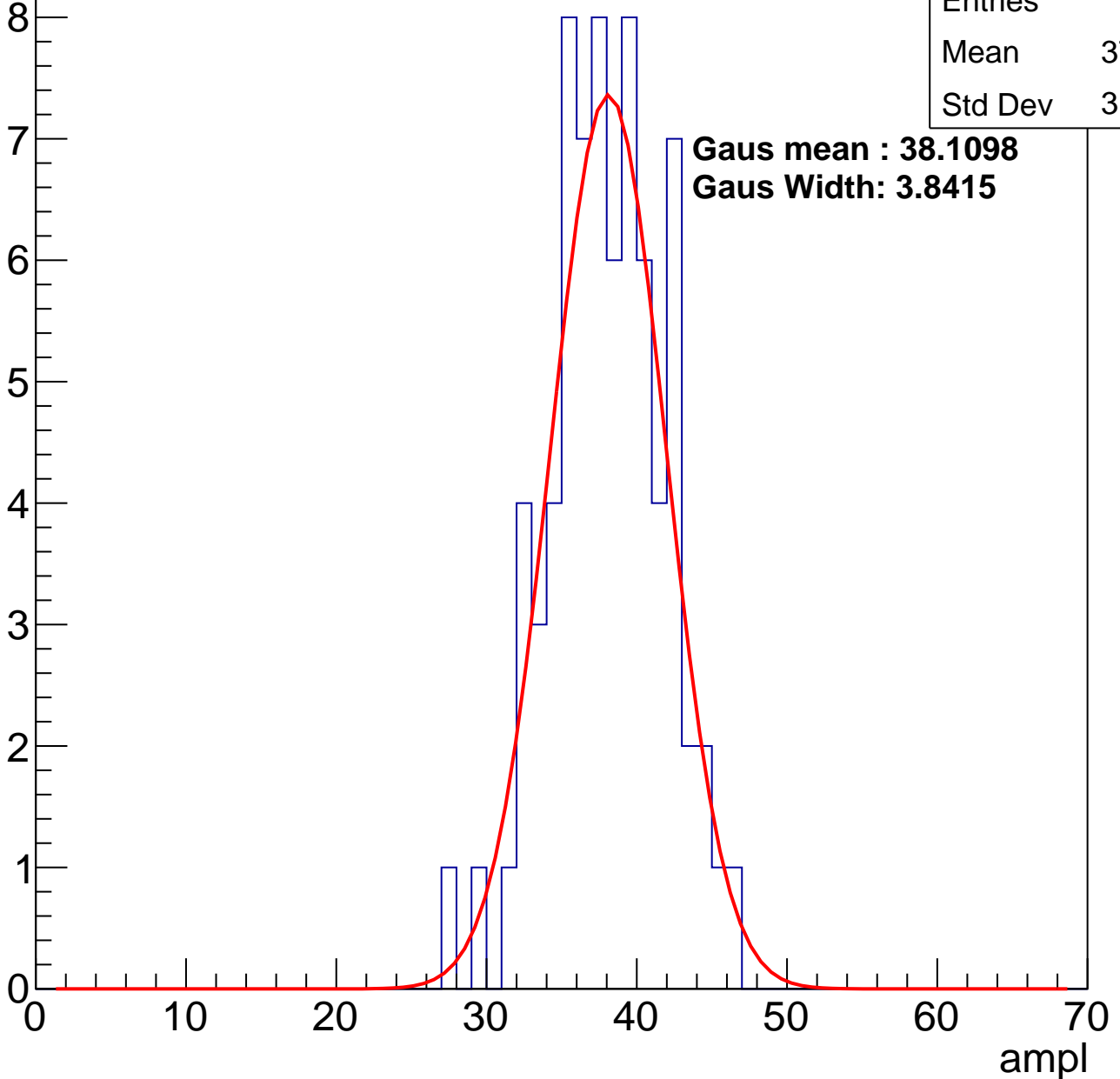
# B1L103S, U11-ch91, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	74
Mean	37.58
Std Dev	3.756

**Gaus mean : 38.1098**  
**Gaus Width: 3.8415**



# B1L103S, U11-ch91, adc2

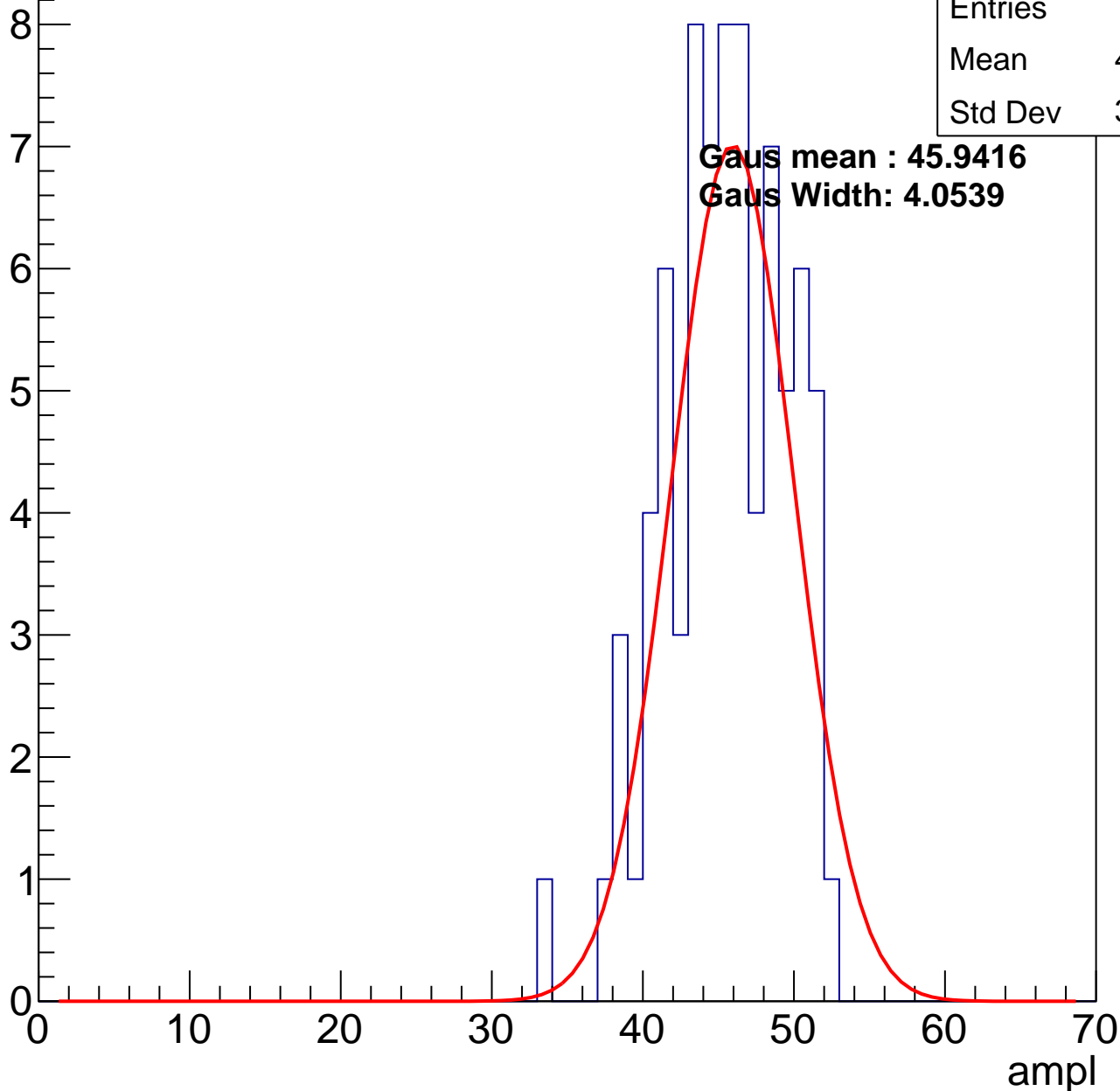
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	78
Mean	45.01
Std Dev	3.921

**Gaus mean : 45.9416**

**Gaus Width: 4.0539**

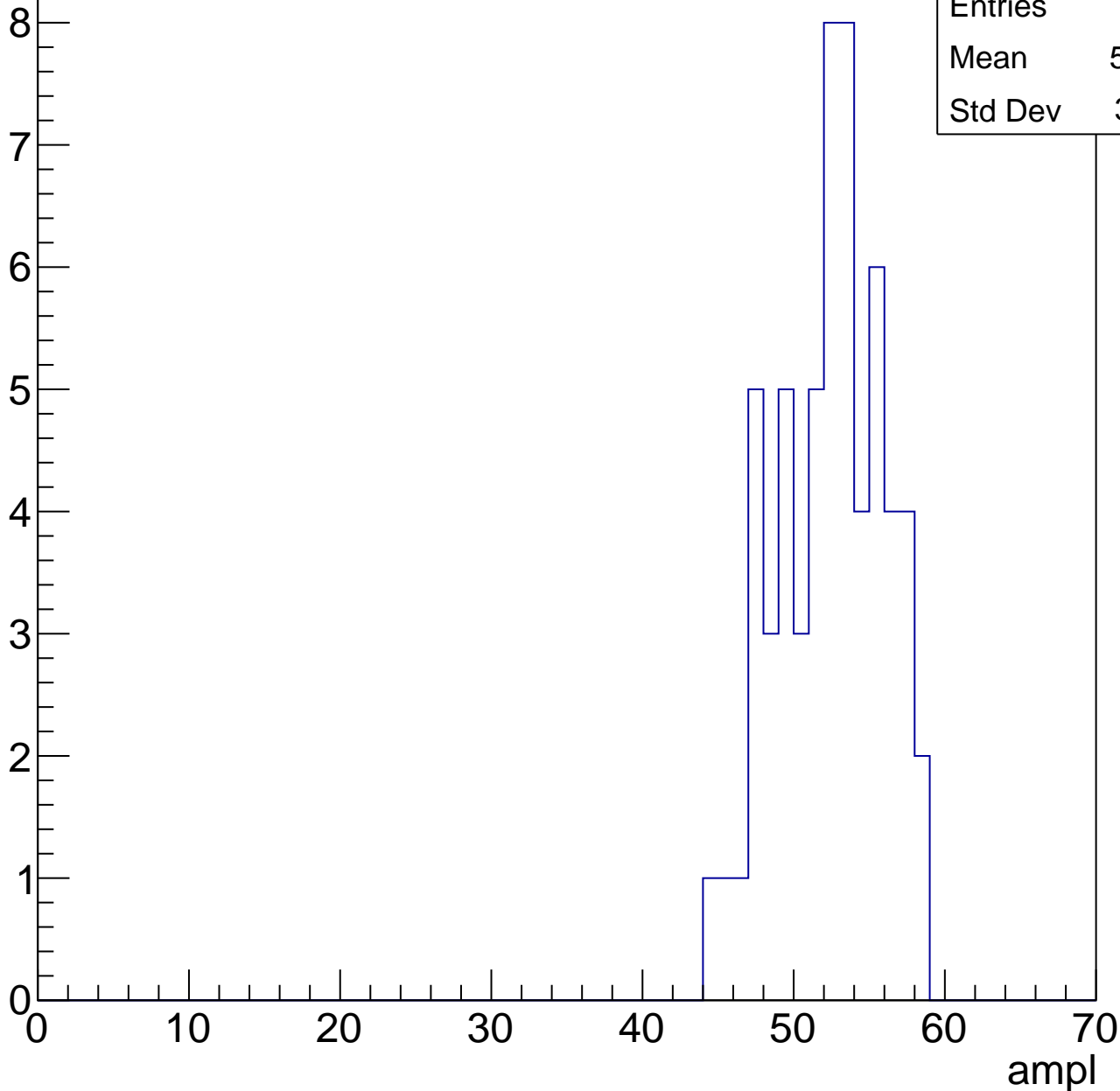


# B1L103S, U11-ch91, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	60
Mean	51.97
Std Dev	3.411

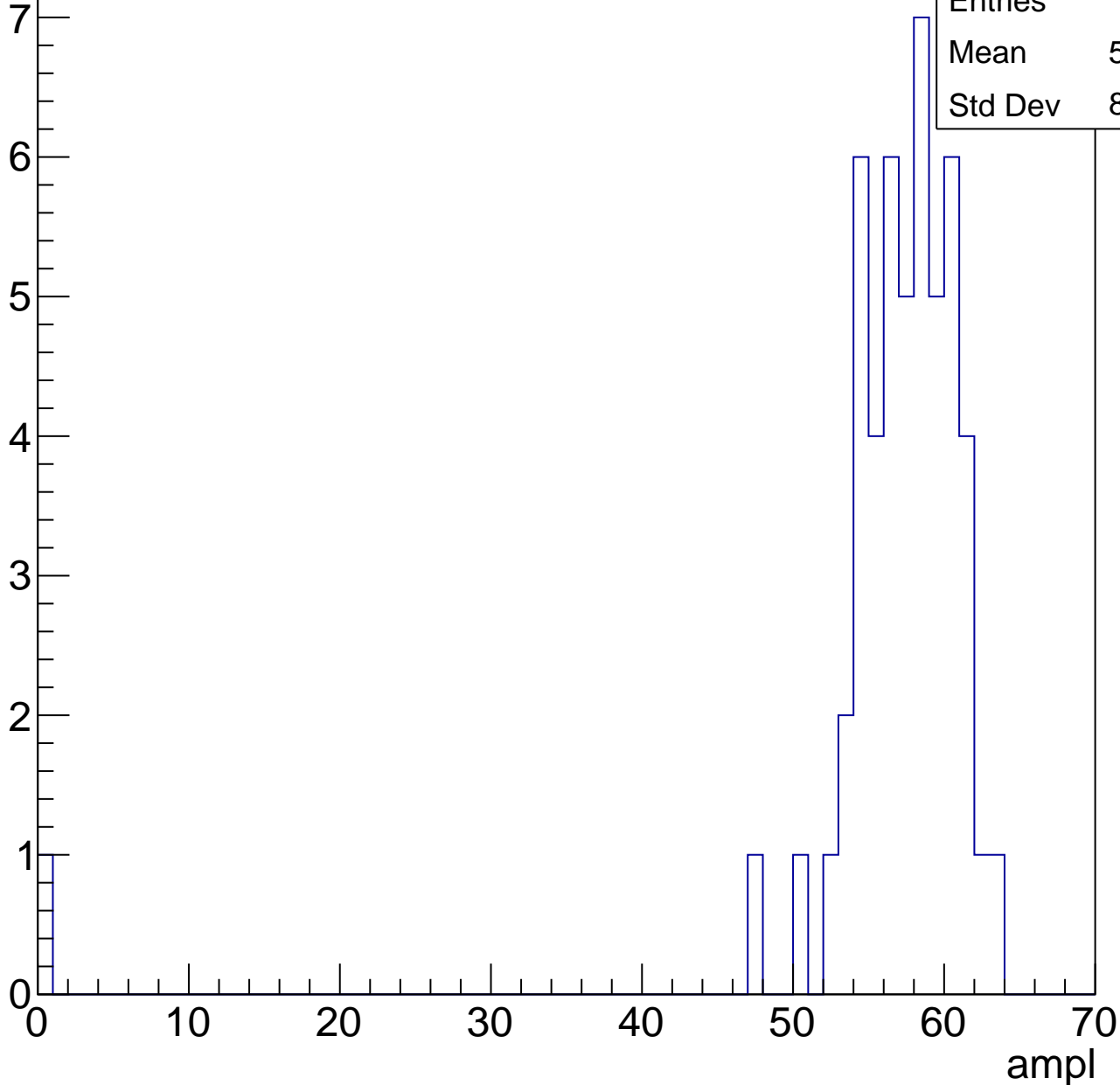


# B1L103S, U11-ch91, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	51
Mean	55.88
Std Dev	8.487

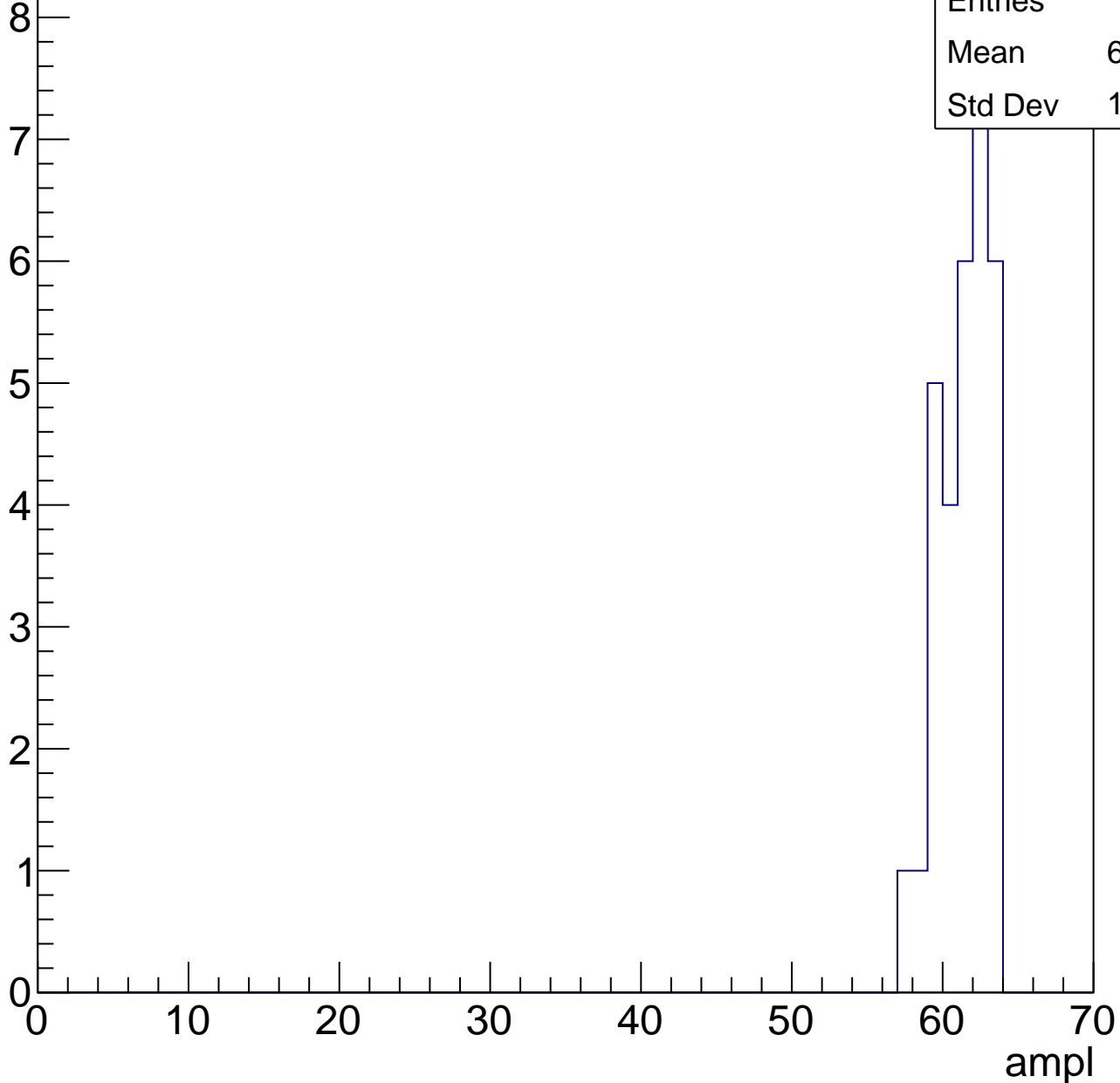


# B1L103S, U11-ch91, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	31
Mean	60.97
Std Dev	1.616



# B1L103S, U11-ch91, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U11-ch91, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	23
Std Dev	0

# B1L103S, U11-ch92, adc0

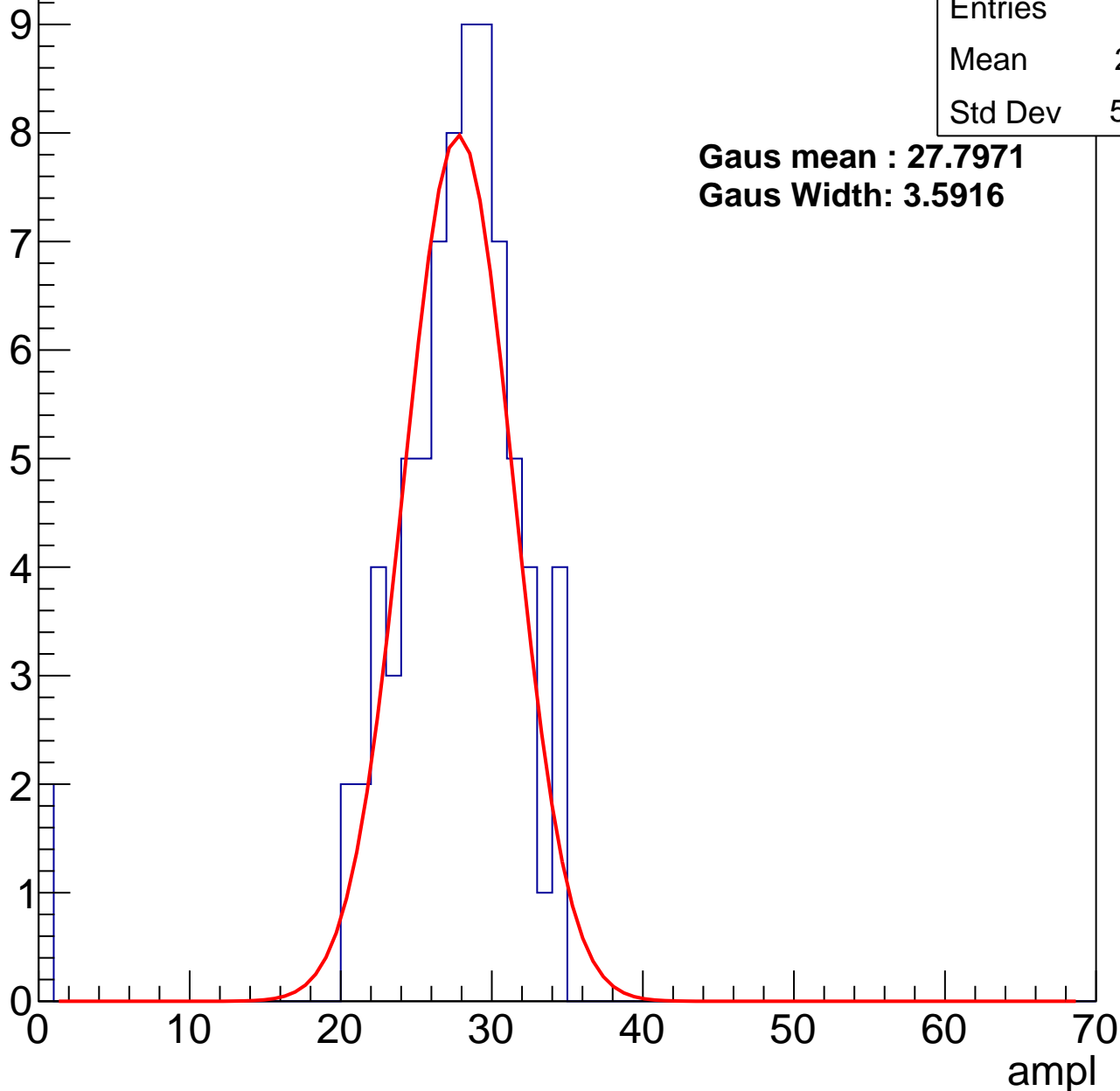
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	77
Mean	26.71
Std Dev	5.538

**Gaus mean : 27.7971**

**Gaus Width: 3.5916**



# B1L103S, U11-ch92, adc1

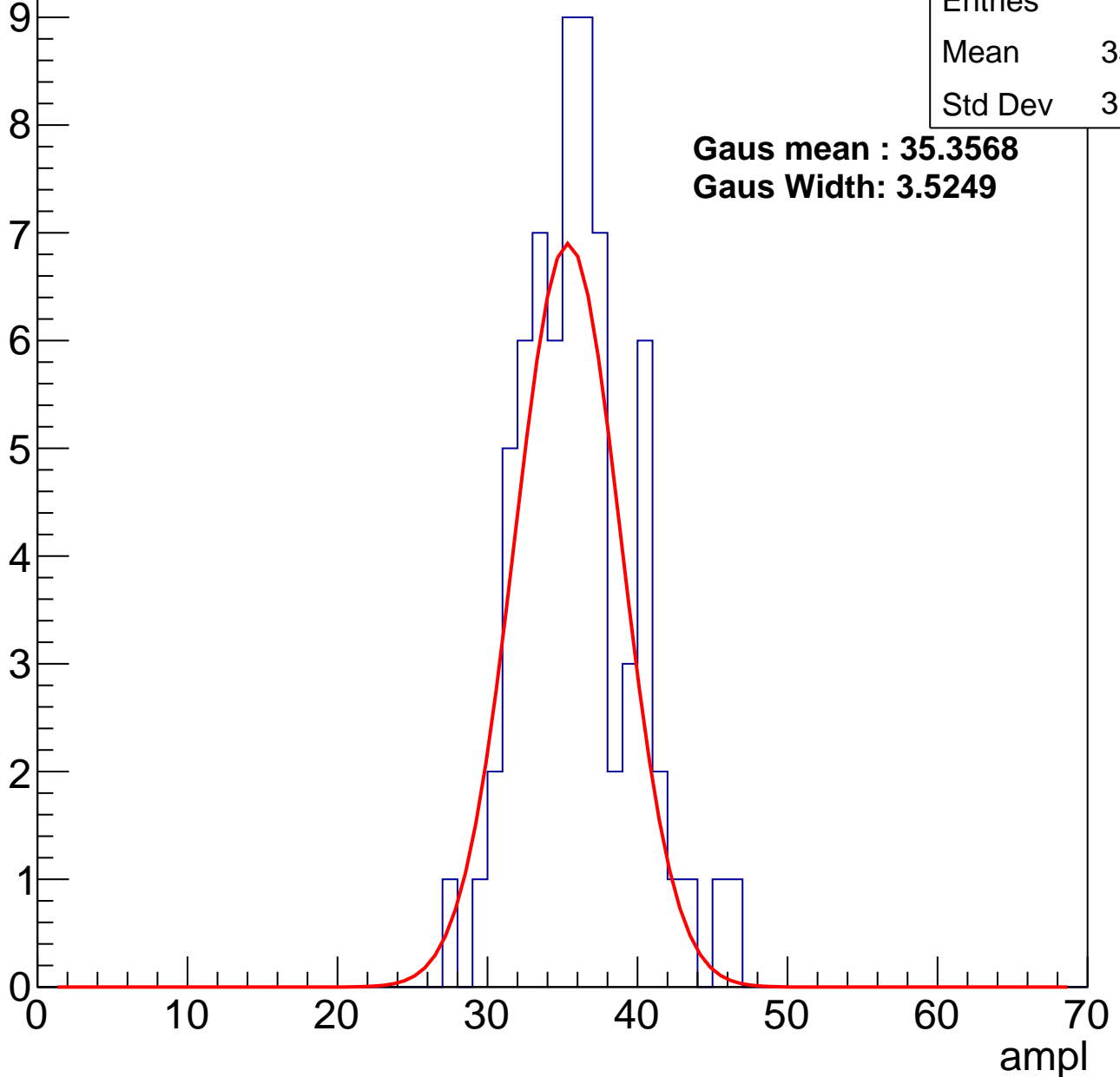
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	70
Mean	35.53
Std Dev	3.698

**Gaus mean : 35.3568**

**Gaus Width: 3.5249**



# B1L103S, U11-ch92, adc2

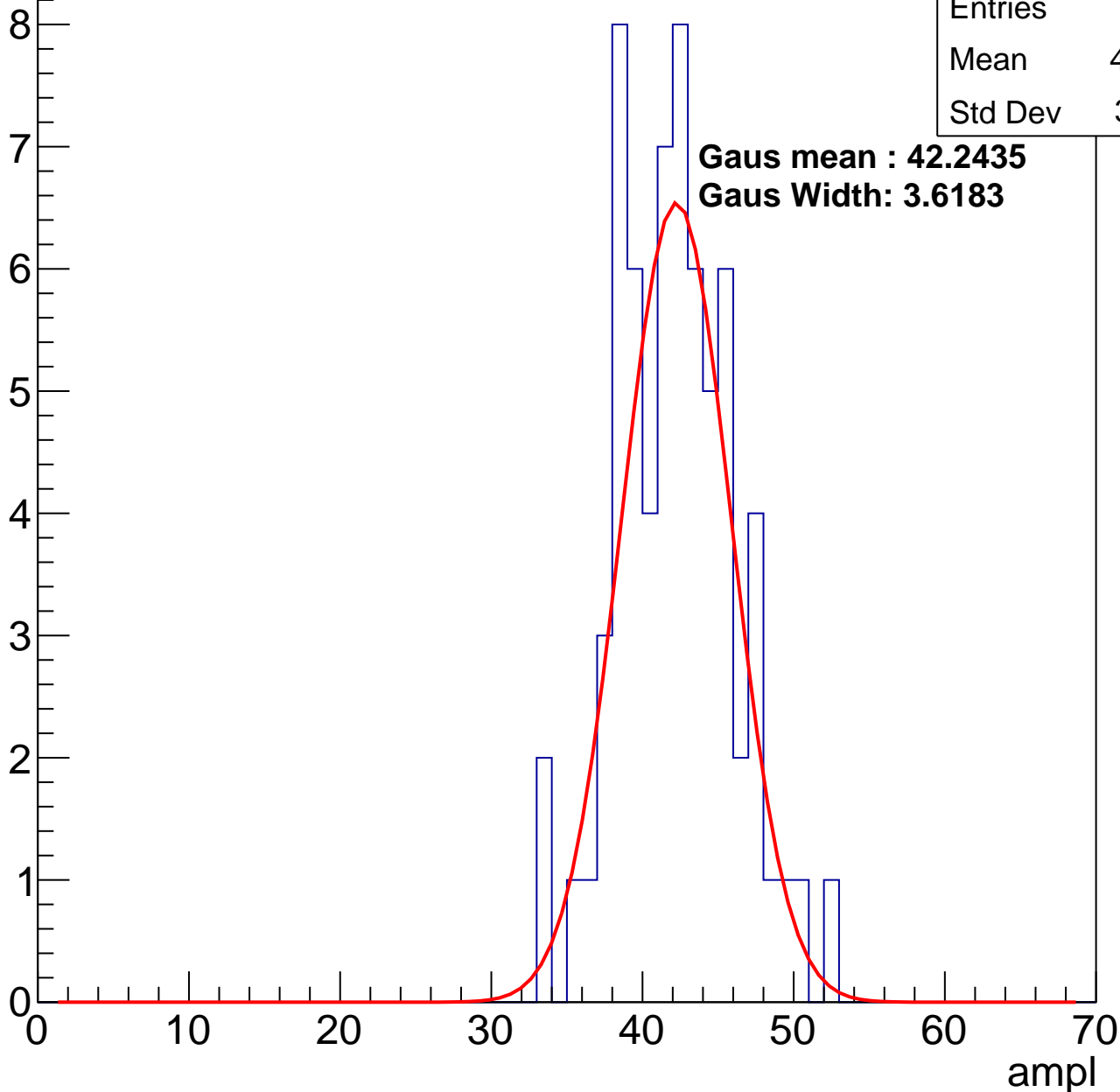
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	41.73
Std Dev	3.831

**Gaus mean : 42.2435**

**Gaus Width: 3.6183**

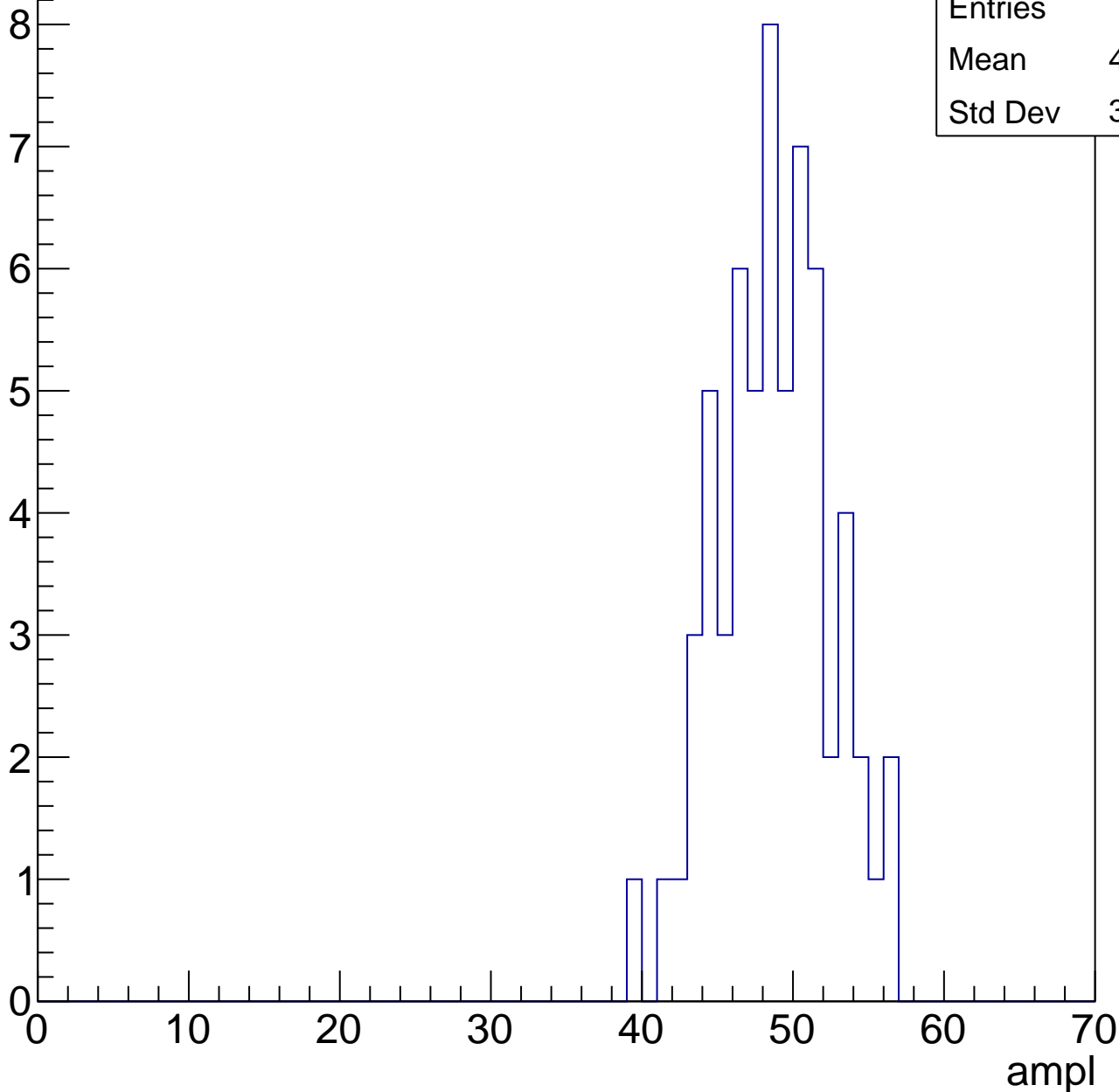


# B1L103S, U11-ch92, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	48.27
Std Dev	3.682

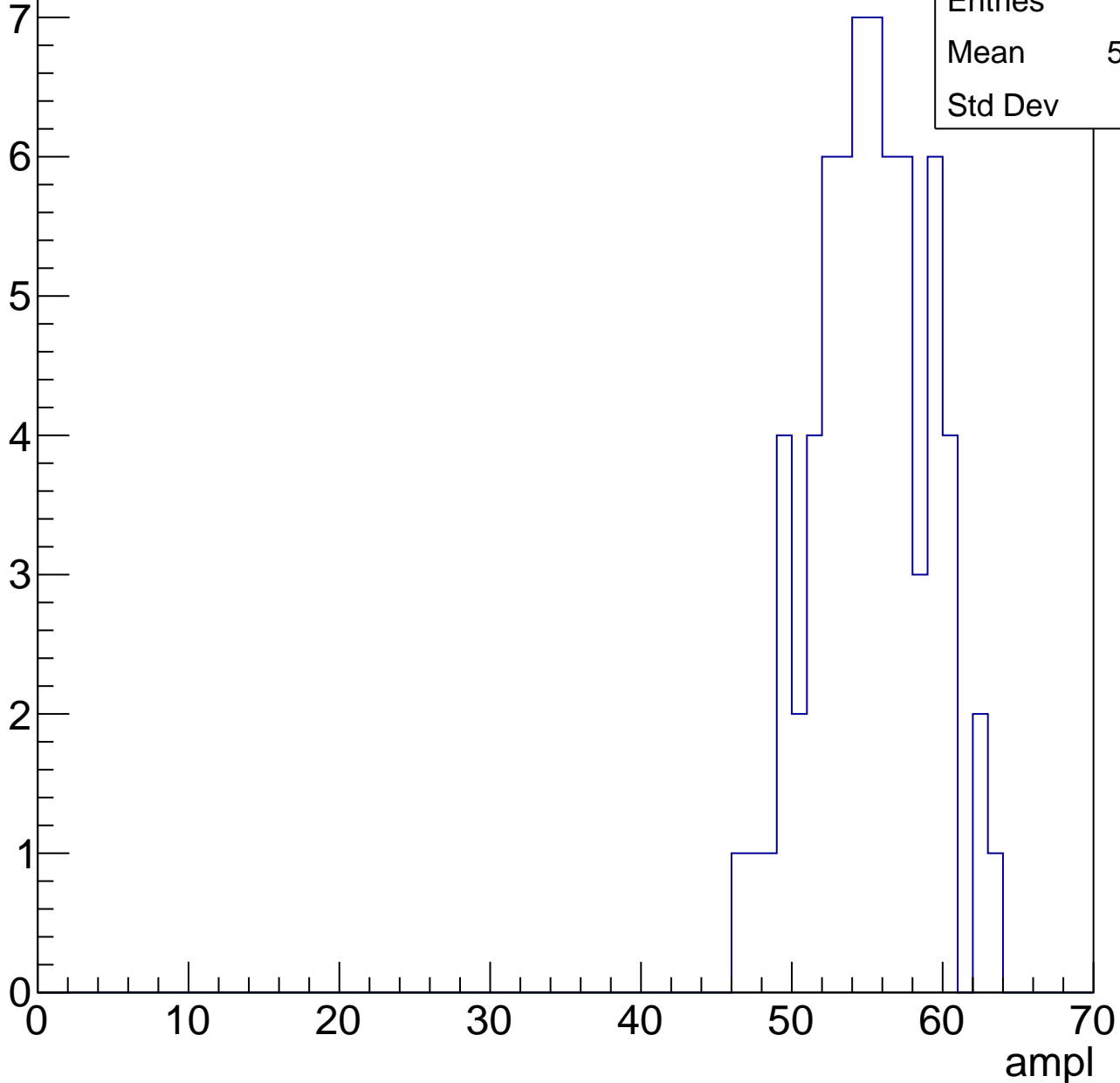


# B1L103S, U11-ch92, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

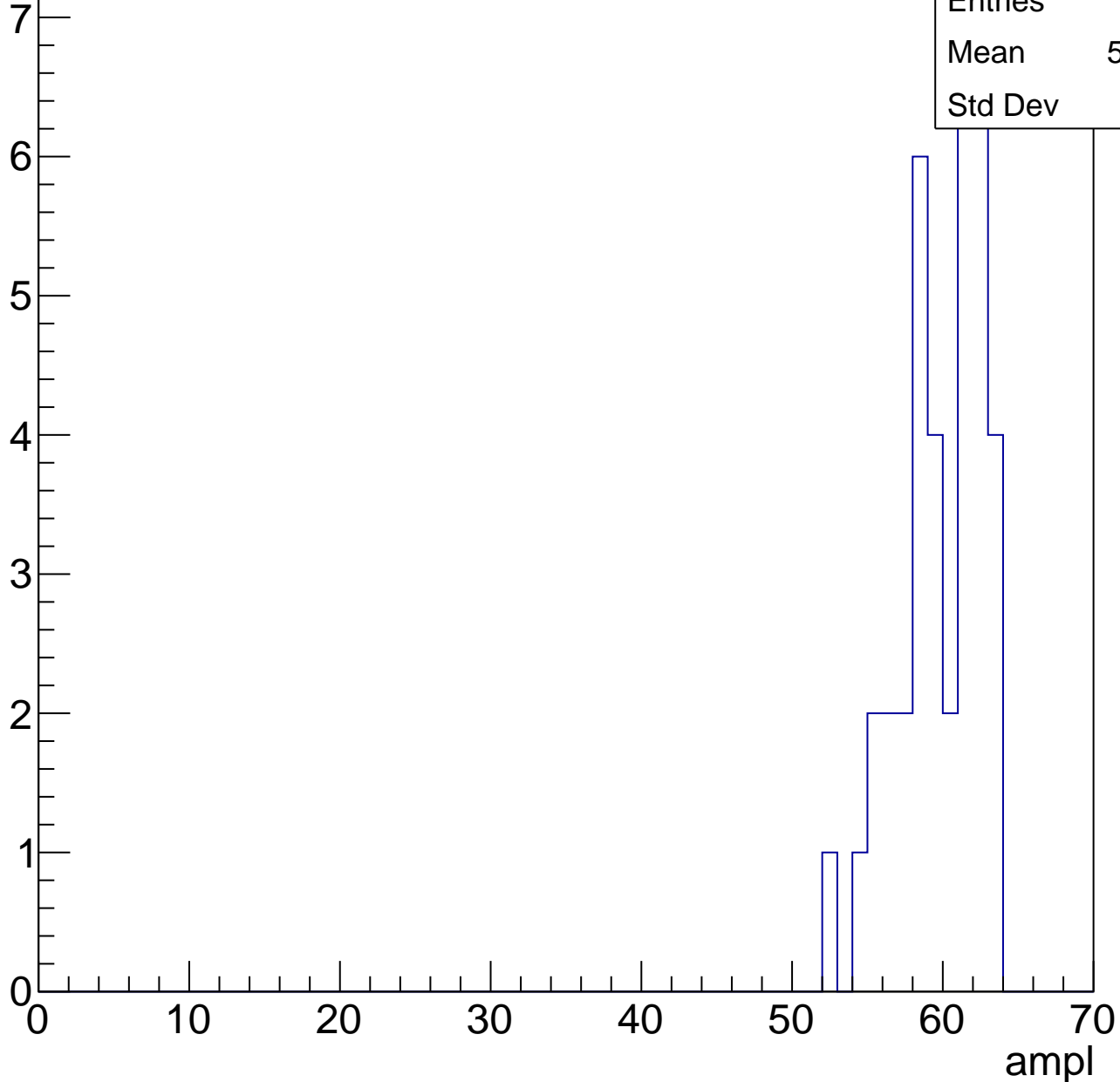
Entries	67
Mean	54.73
Std Dev	3.76



# B1L103S, U11-ch92, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

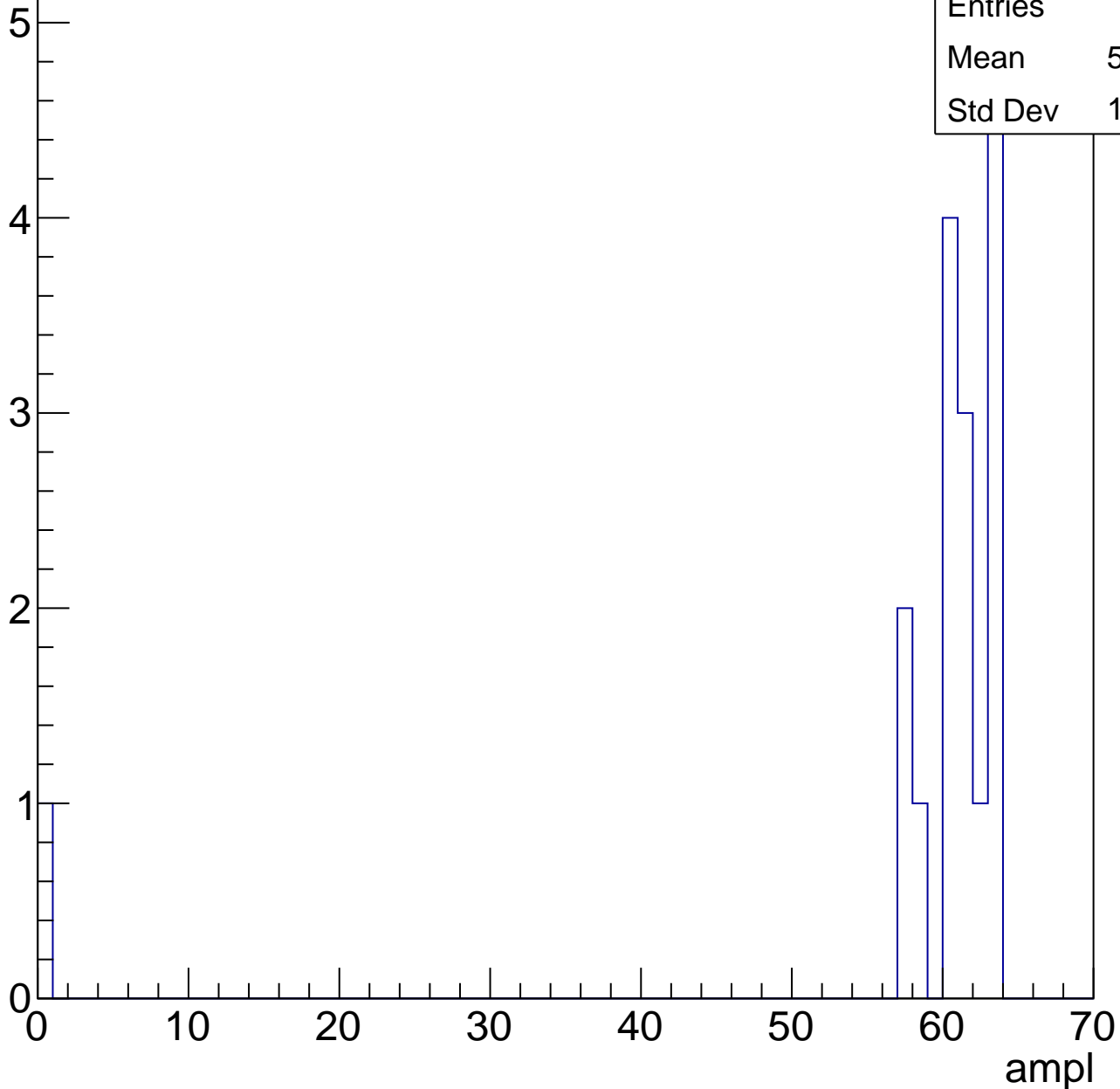


# B1L103S, U11-ch92, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	17
Mean	57.18
Std Dev	14.43





# B1L103S, U11-ch92, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L103S, U11-ch93, adc0

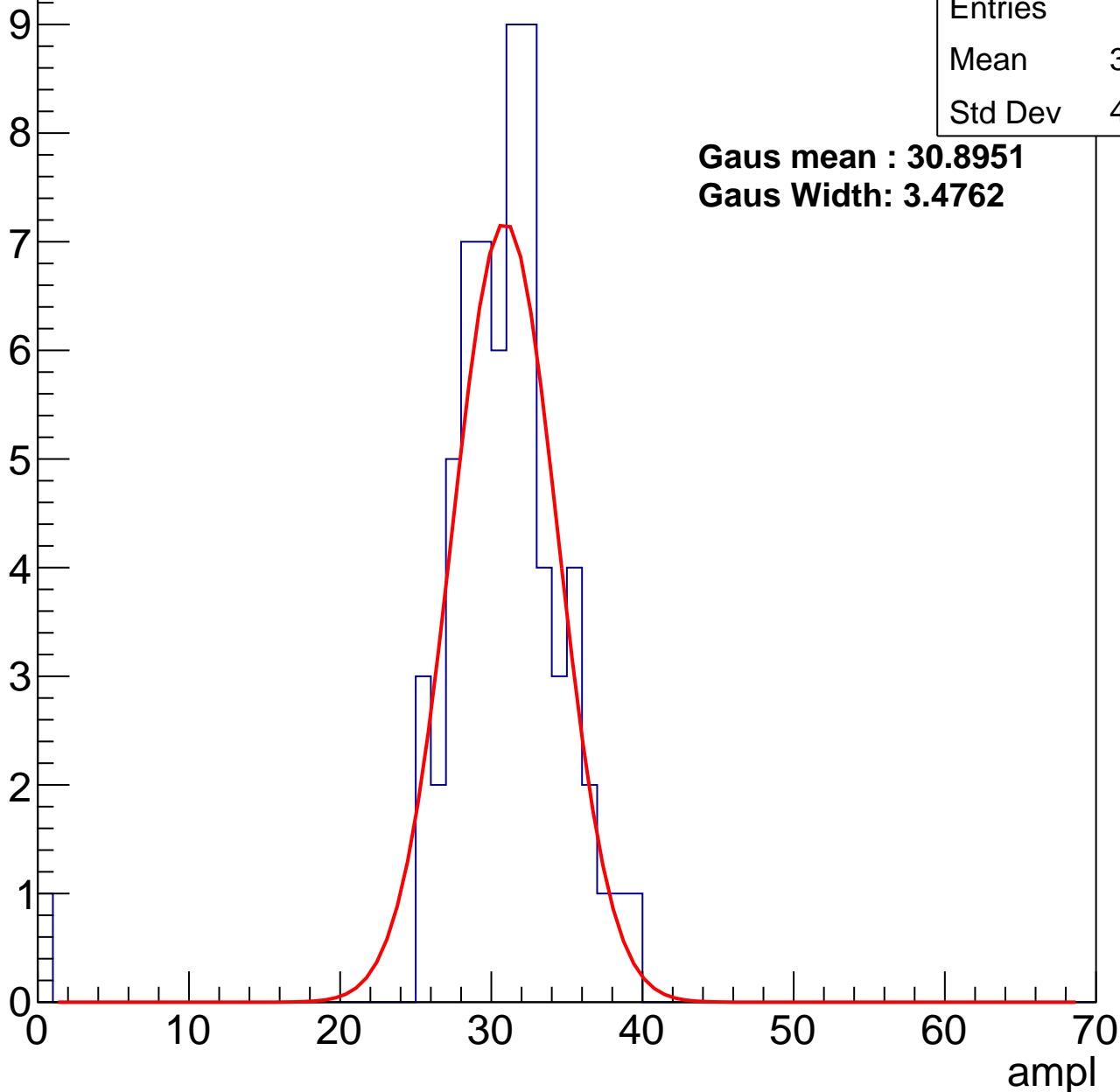
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	30.28
Std Dev	4.926

**Gaus mean : 30.8951**

**Gaus Width: 3.4762**



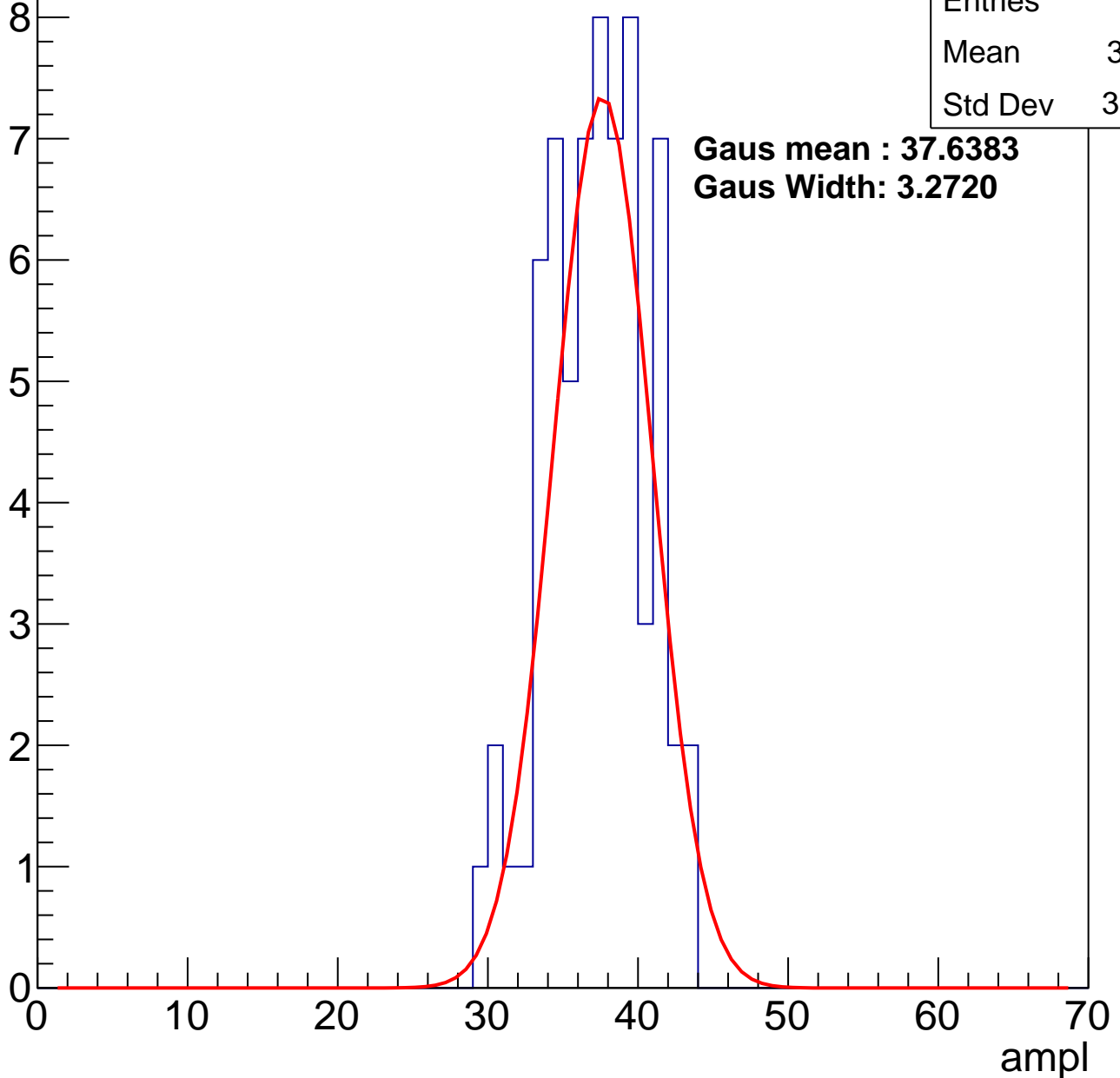
# B1L103S, U11-ch93, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	36.81
Std Dev	3.247

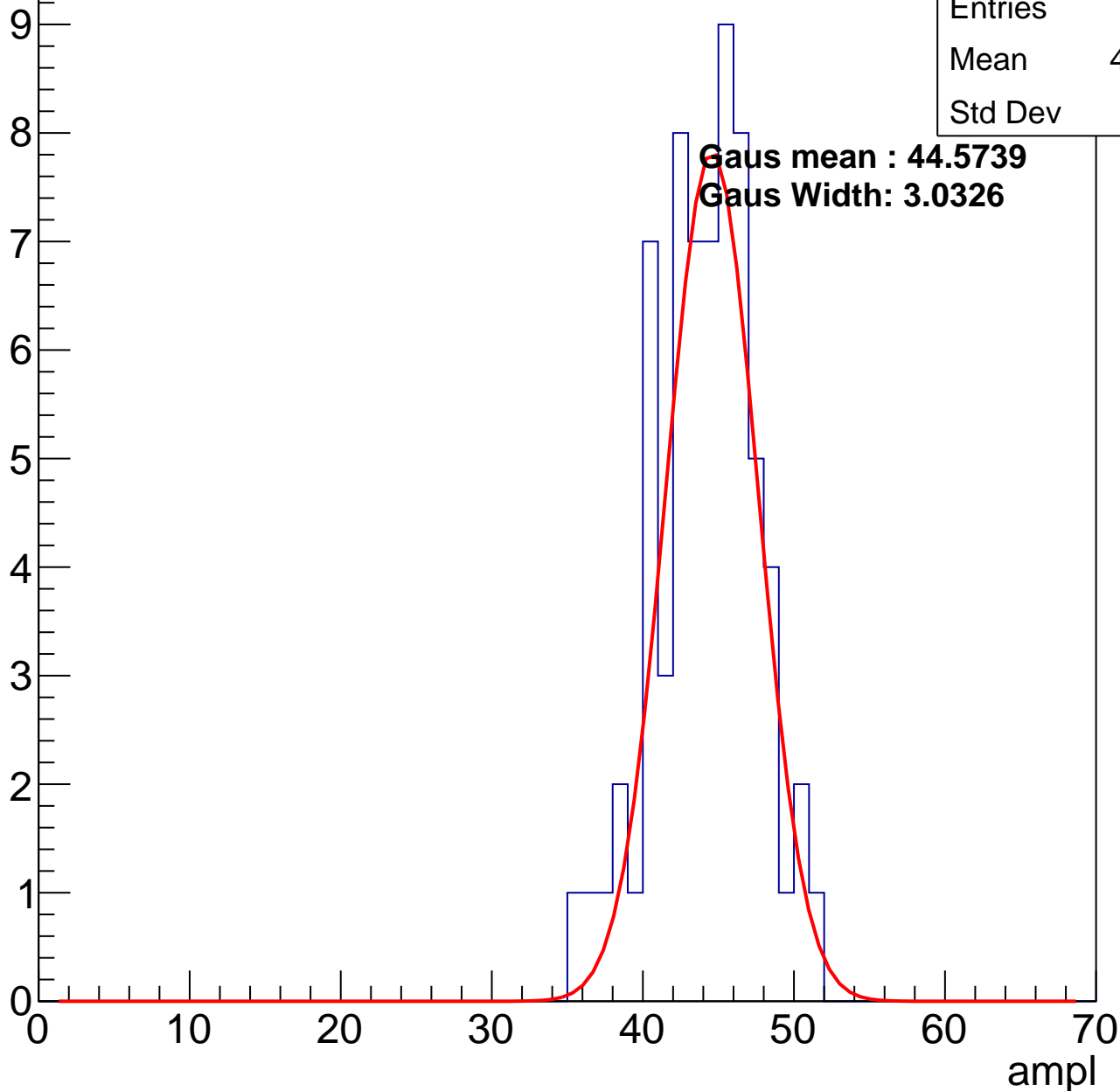
**Gaus mean : 37.6383**  
**Gaus Width: 3.2720**



# B1L103S, U11-ch93, adc2

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

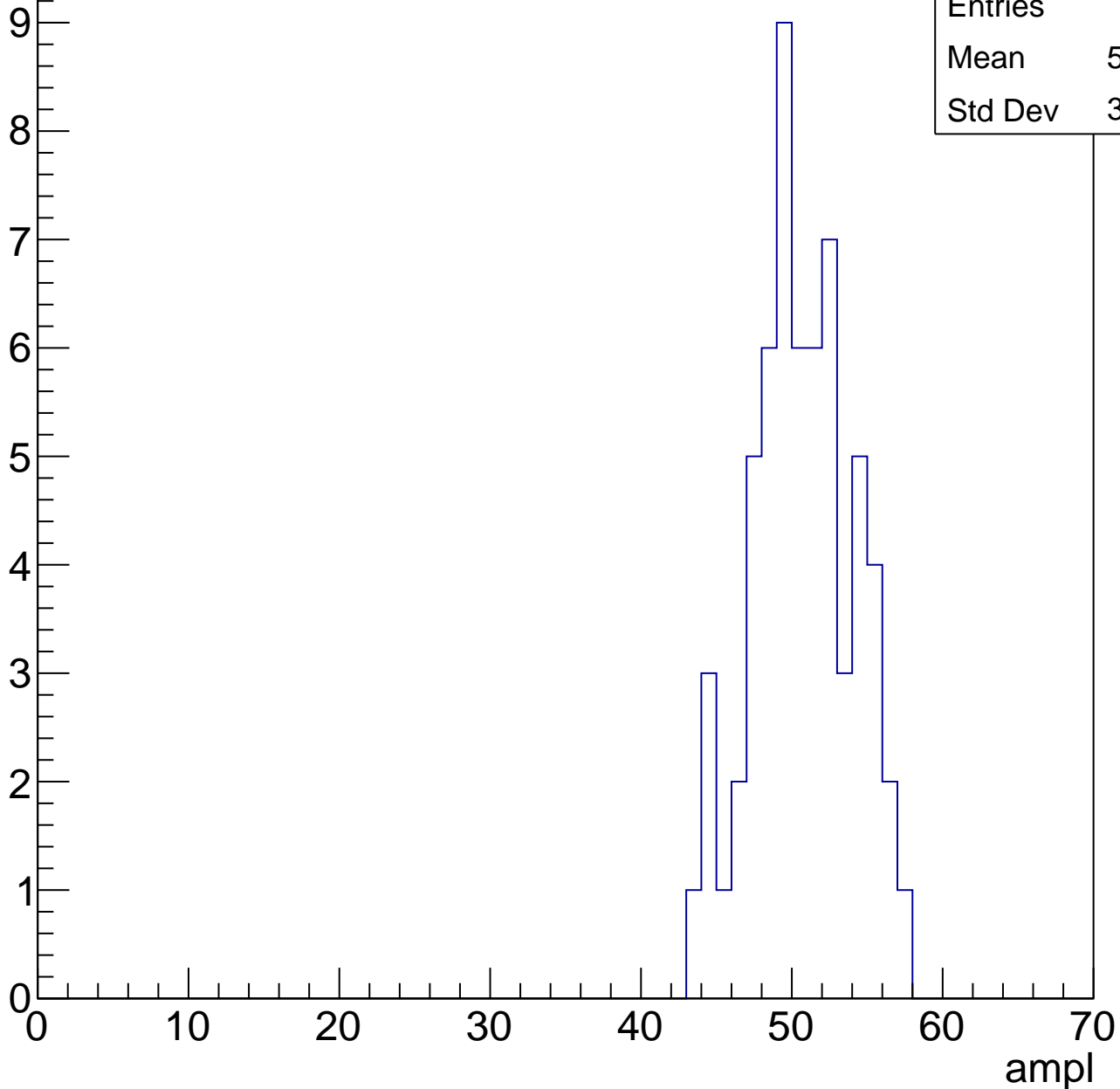


# B1L103S, U11-ch93, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	61
Mean	50.23
Std Dev	3.266

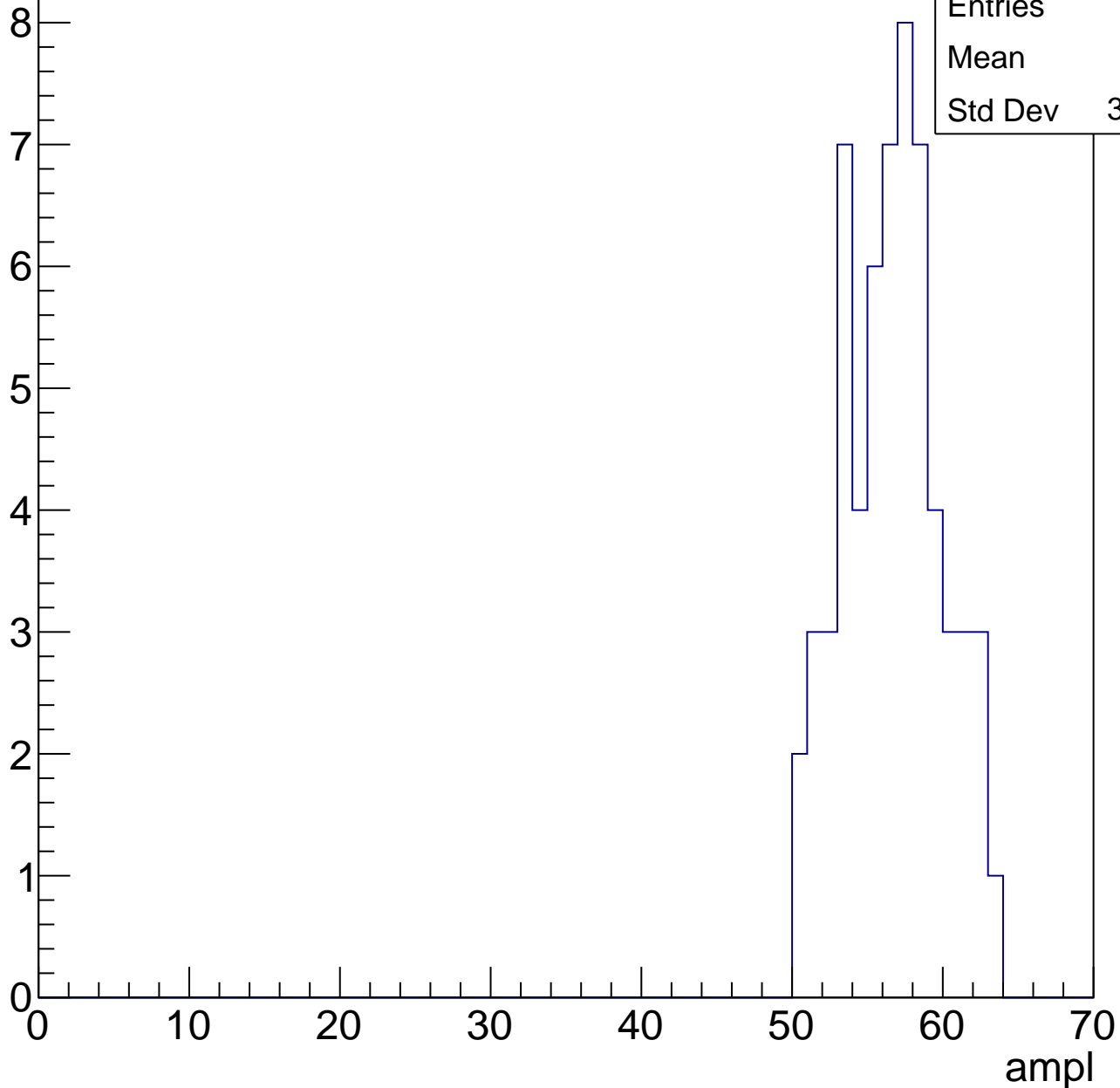


# B1L103S, U11-ch93, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	61
Mean	56.2
Std Dev	3.213



# B1L103S, U11-ch93, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

7

6

5

4

3

2

1

0

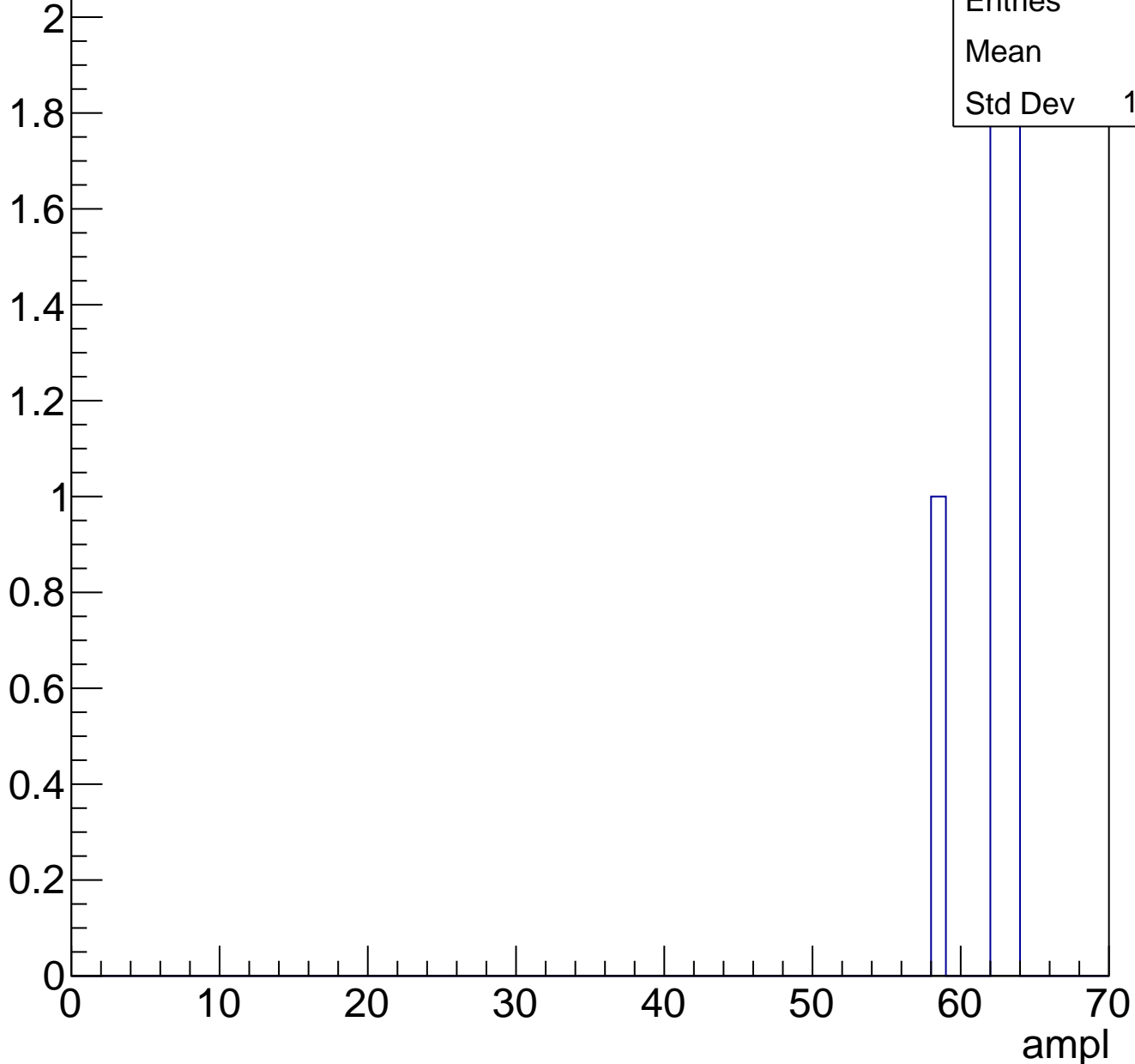
Entries	38
Mean	58.82
Std Dev	9.883

ampl

# B1L103S, U11-ch93, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U11-ch93, adc7

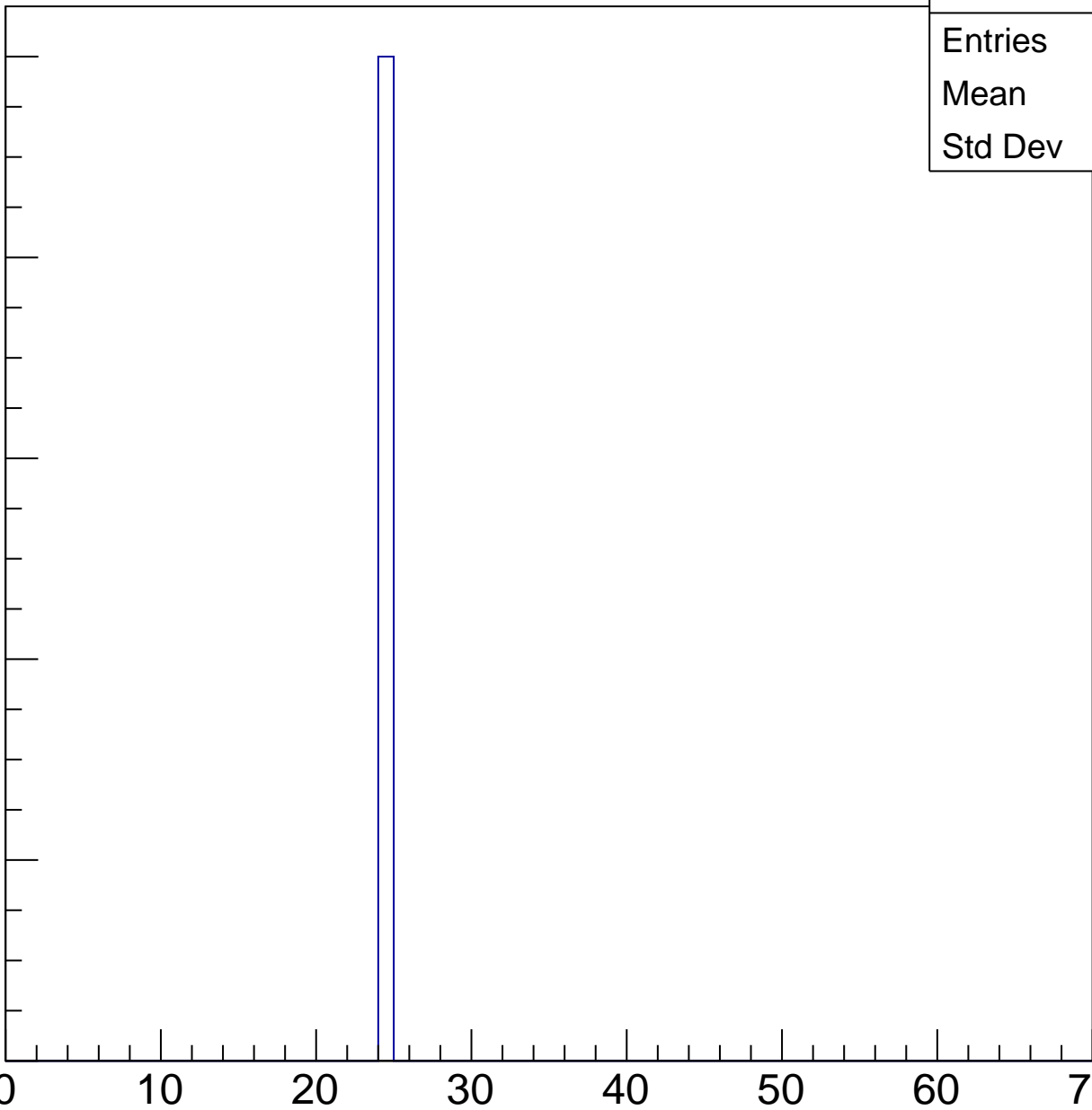
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

1  
0.8  
0.6  
0.4  
0.2  
0

Entries	1
Mean	24
Std Dev	0

ampl



# B1L103S, U11-ch94, adc0

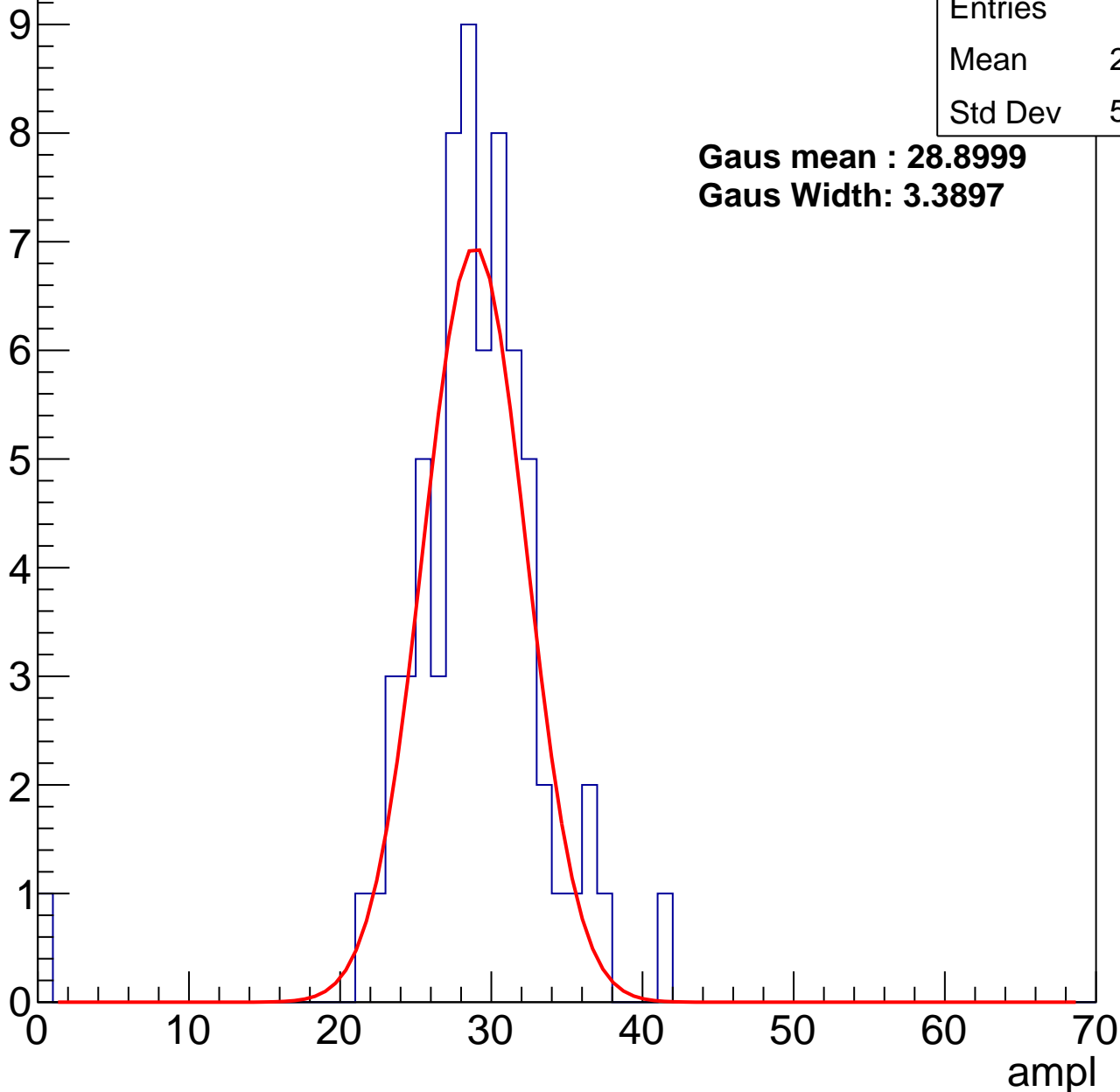
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	28.36
Std Dev	5.086

**Gaus mean : 28.8999**

**Gaus Width: 3.3897**



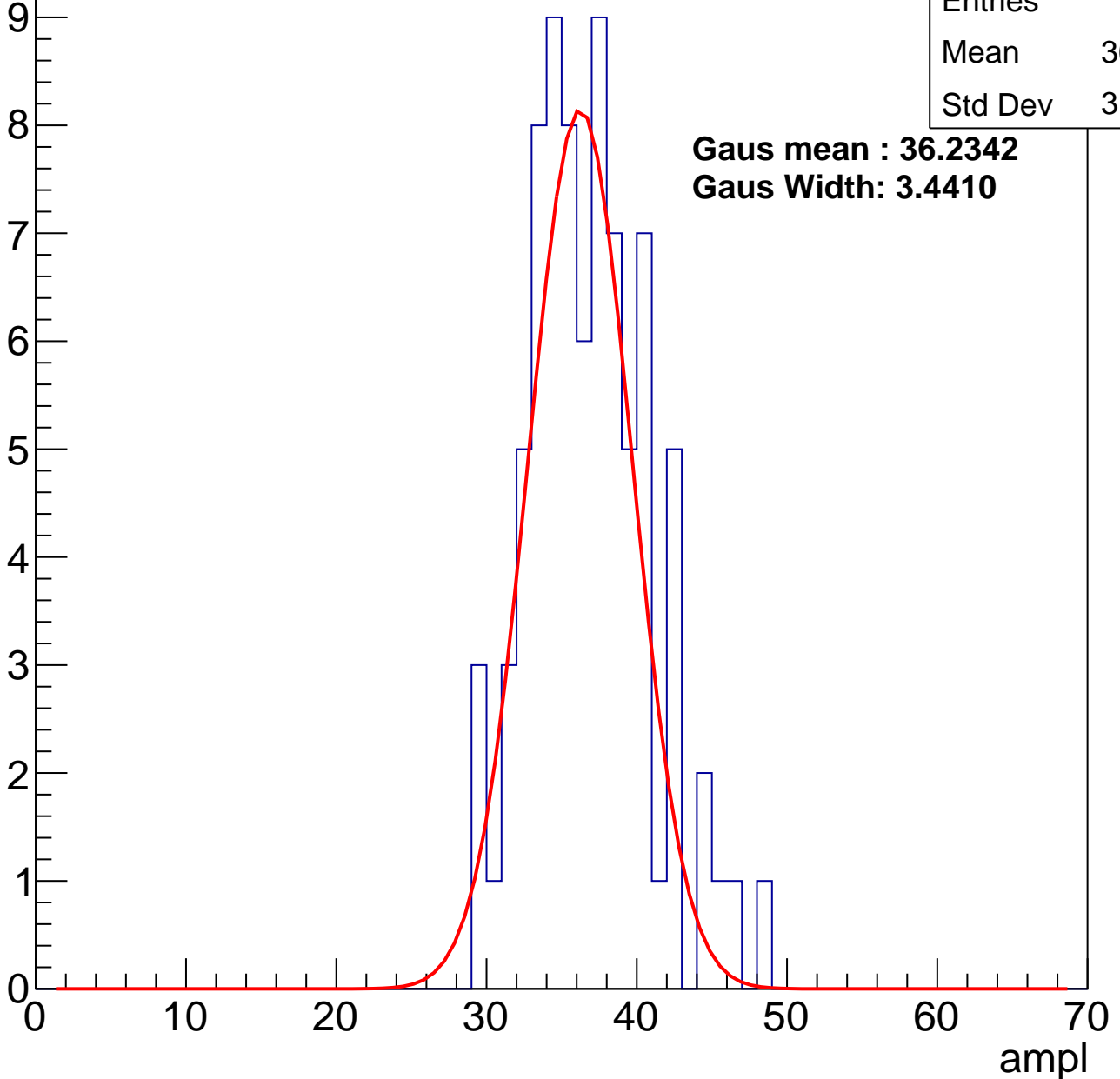
# B1L103S, U11-ch94, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	82
Mean	36.44
Std Dev	3.967

**Gaus mean : 36.2342**  
**Gaus Width: 3.4410**



# B1L103S, U11-ch94, adc2

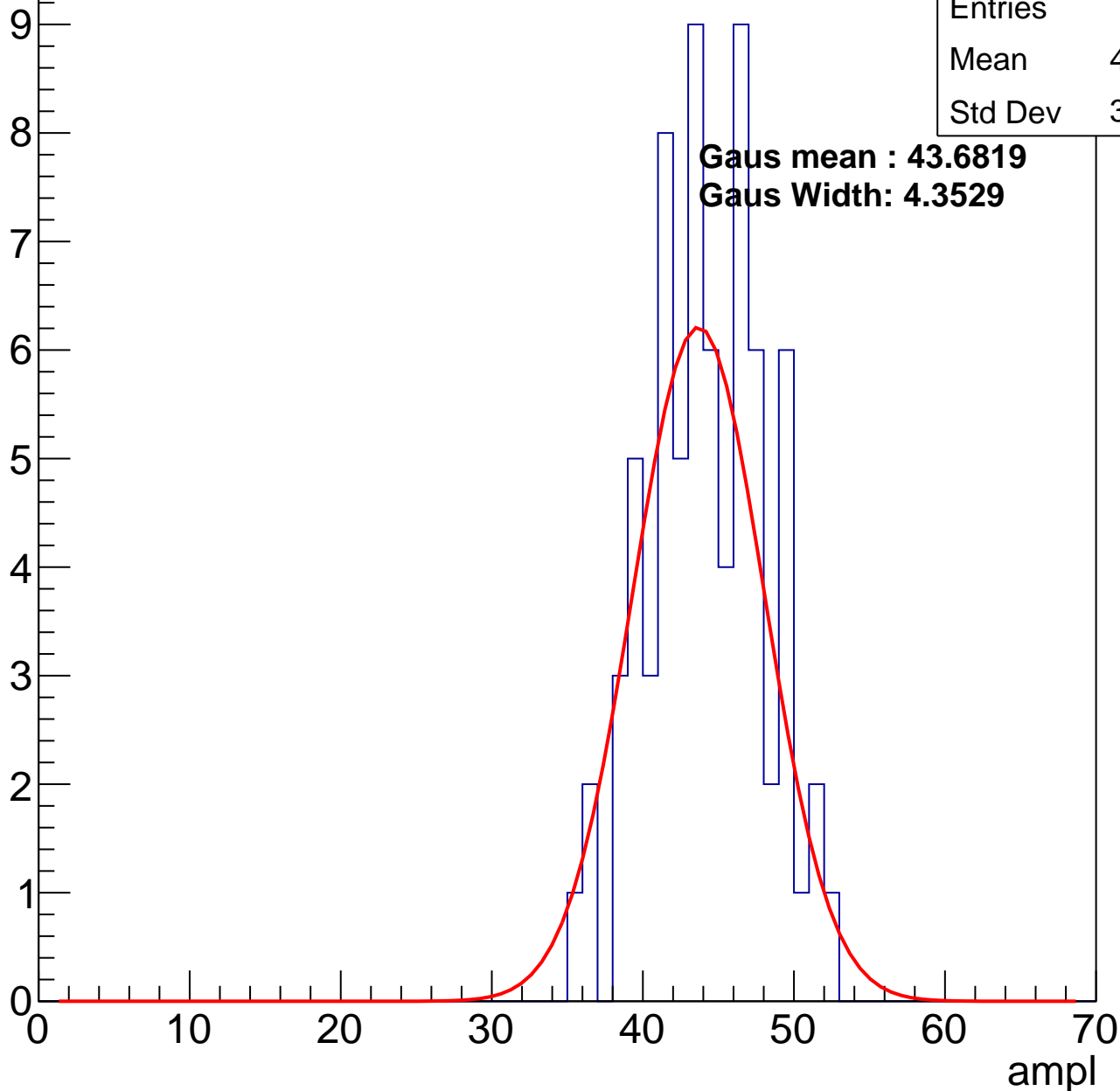
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	73
Mean	43.77
Std Dev	3.812

**Gaus mean : 43.6819**

**Gaus Width: 4.3529**

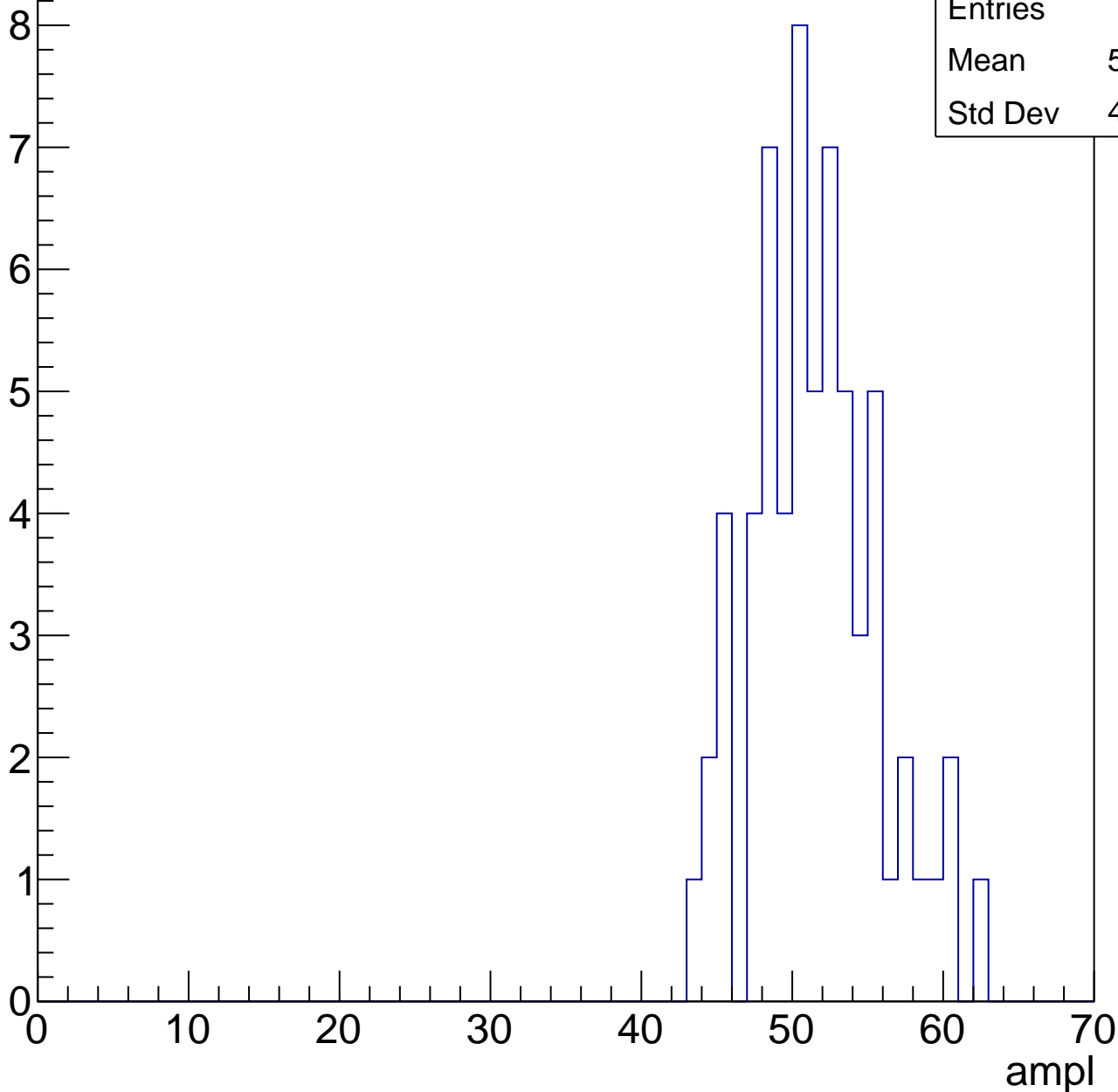


# B1L103S, U11-ch94, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	51.13
Std Dev	4.146

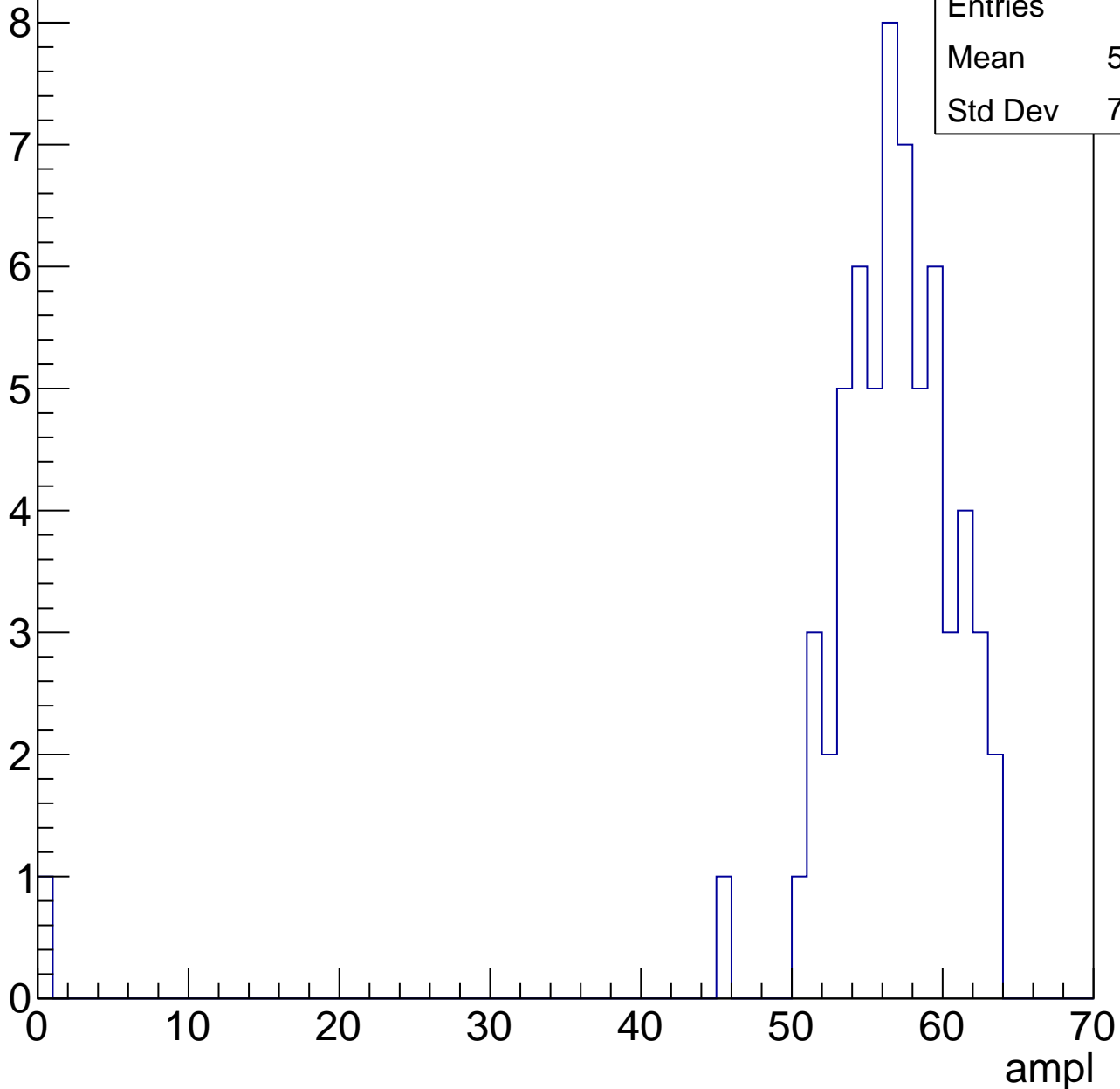


# B1L103S, U11-ch94, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	55.53
Std Dev	7.927

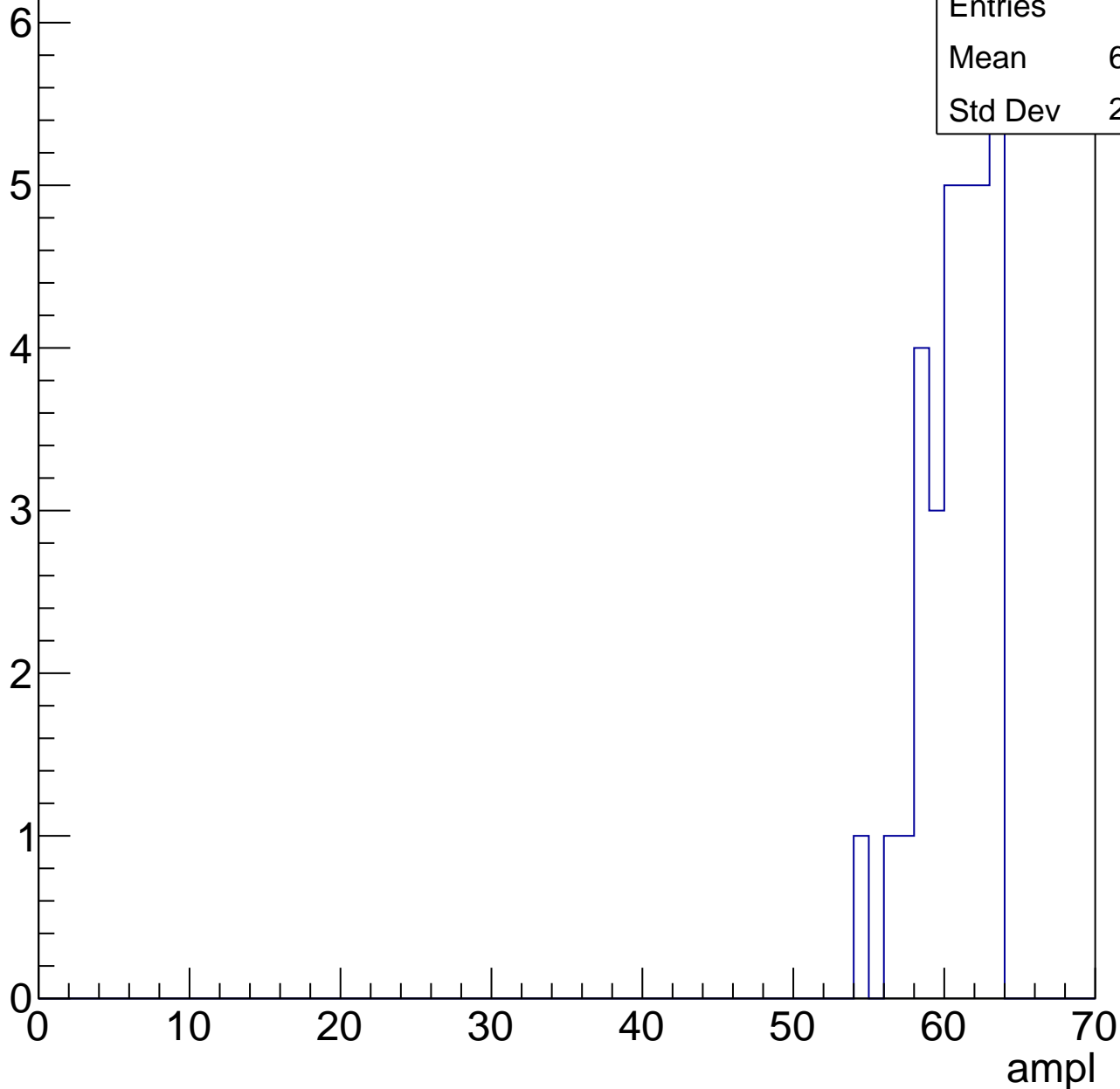


# B1L103S, U11-ch94, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	31
Mean	60.29
Std Dev	2.246



# B1L103S, U11-ch94, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

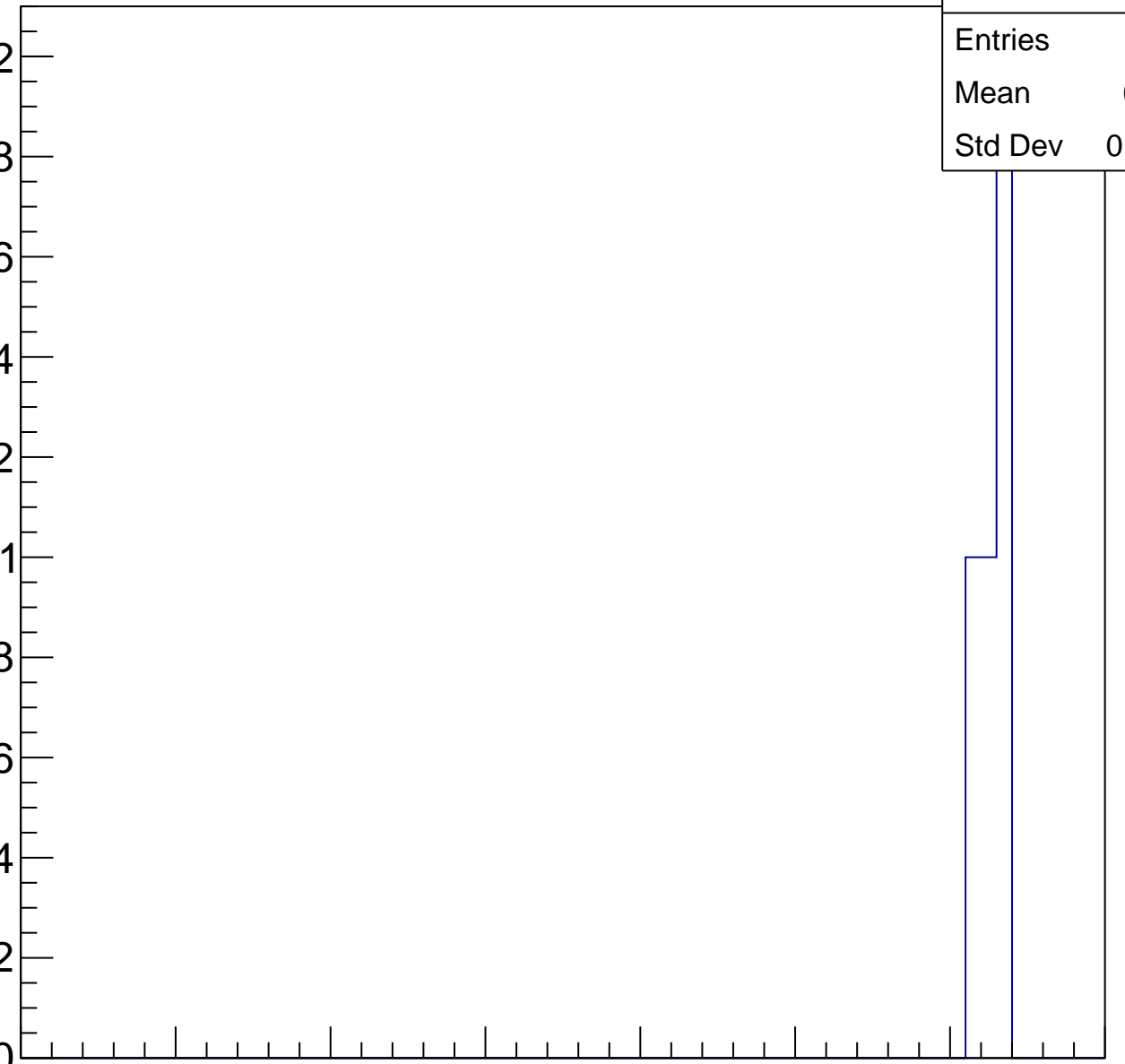
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	4
Mean	62.25
Std Dev	0.8292

ampl

0 10 20 30 40 50 60 70





# B1L103S, U11-ch94, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U11-ch95, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	65
Mean	27.43
Std Dev	6.827

**Gaus mean : 29.4984**

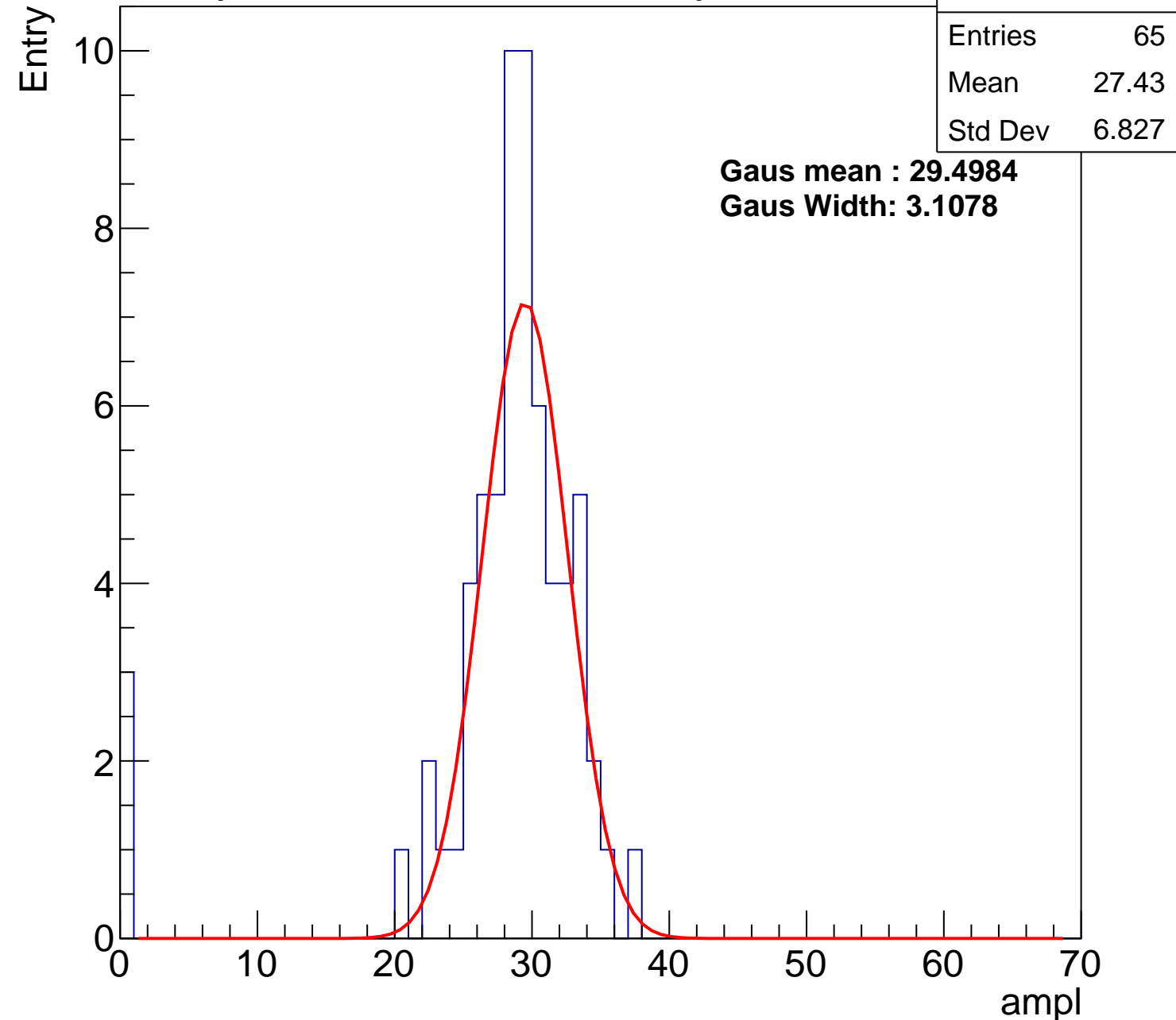
**Gaus Width: 3.1078**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



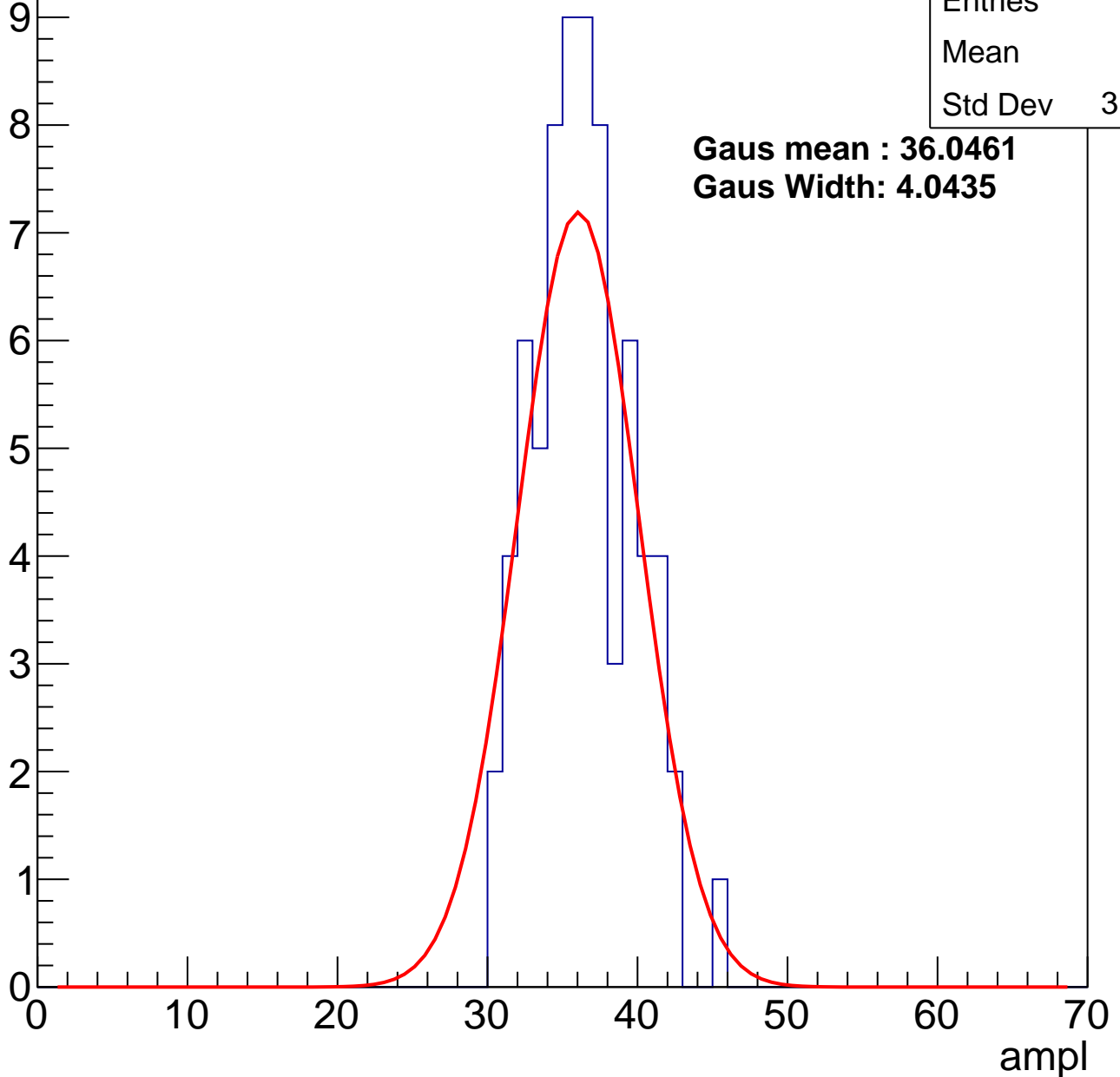
# B1L103S, U11-ch95, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	71
Mean	35.9
Std Dev	3.238

**Gaus mean : 36.0461**  
**Gaus Width: 4.0435**



# B1L103S, U11-ch95, adc2

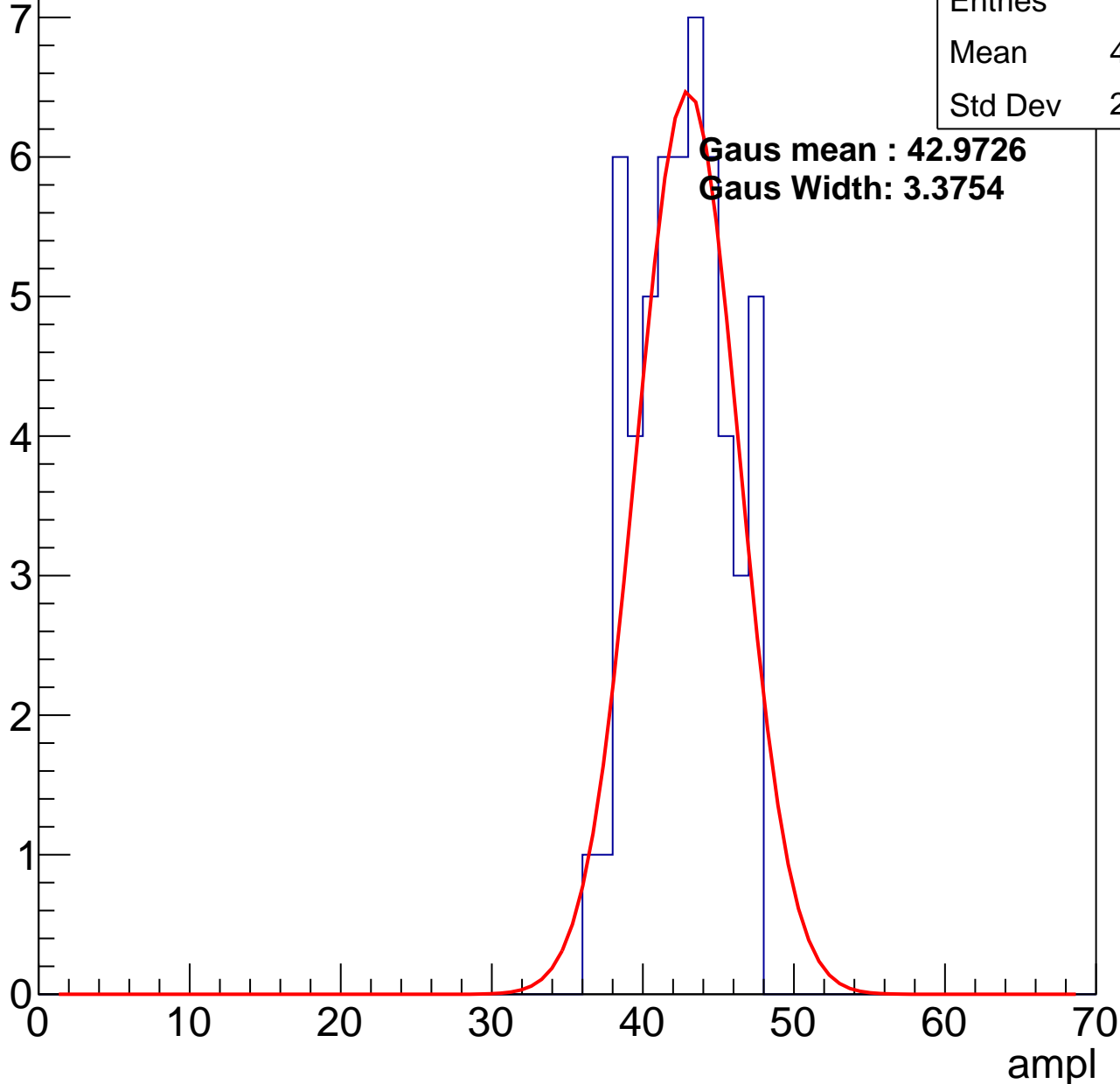
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	54
Mean	42.09
Std Dev	2.914

**Gaus mean : 42.9726**

**Gaus Width: 3.3754**

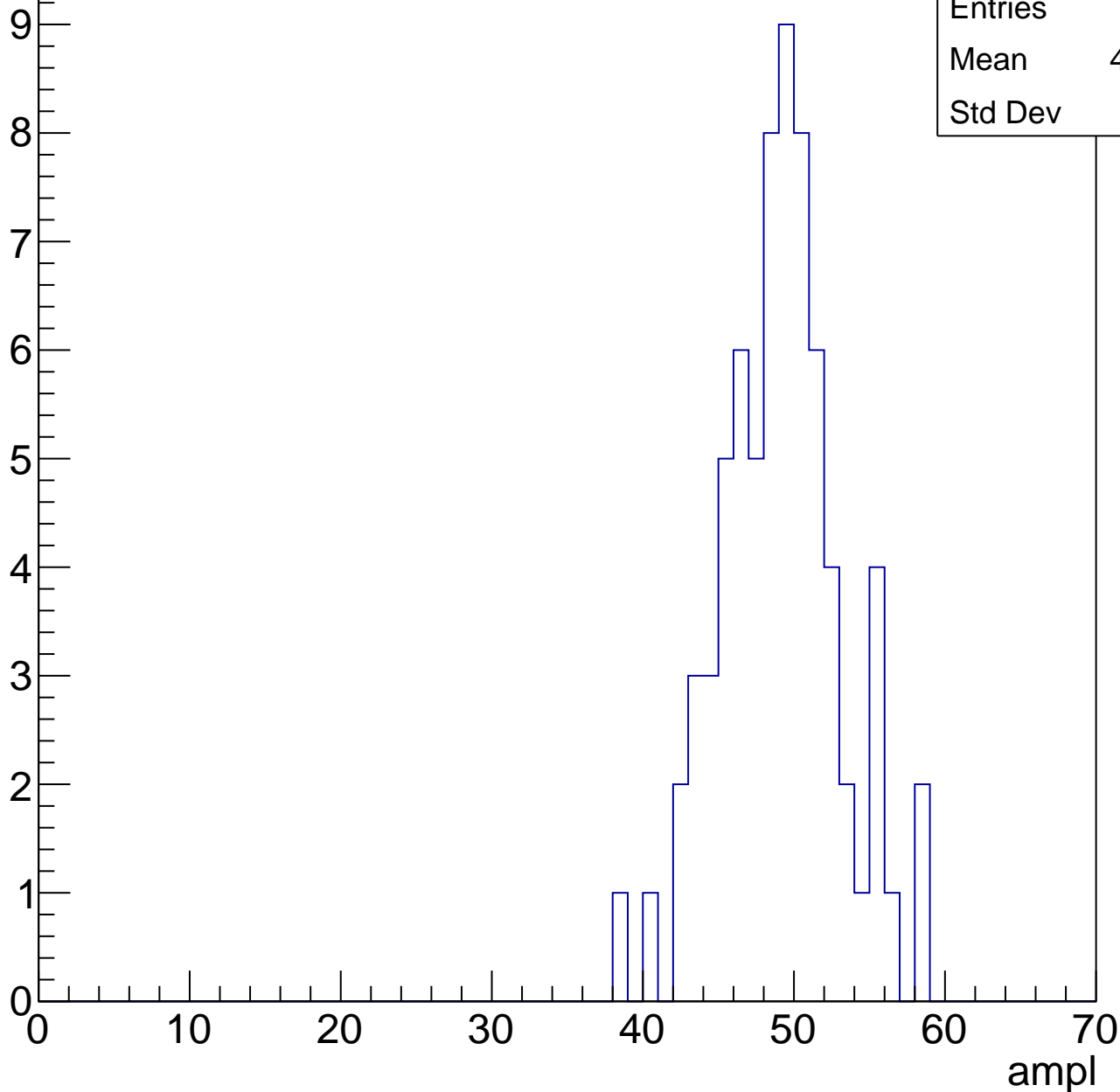


# B1L103S, U11-ch95, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	71
Mean	48.59
Std Dev	3.96

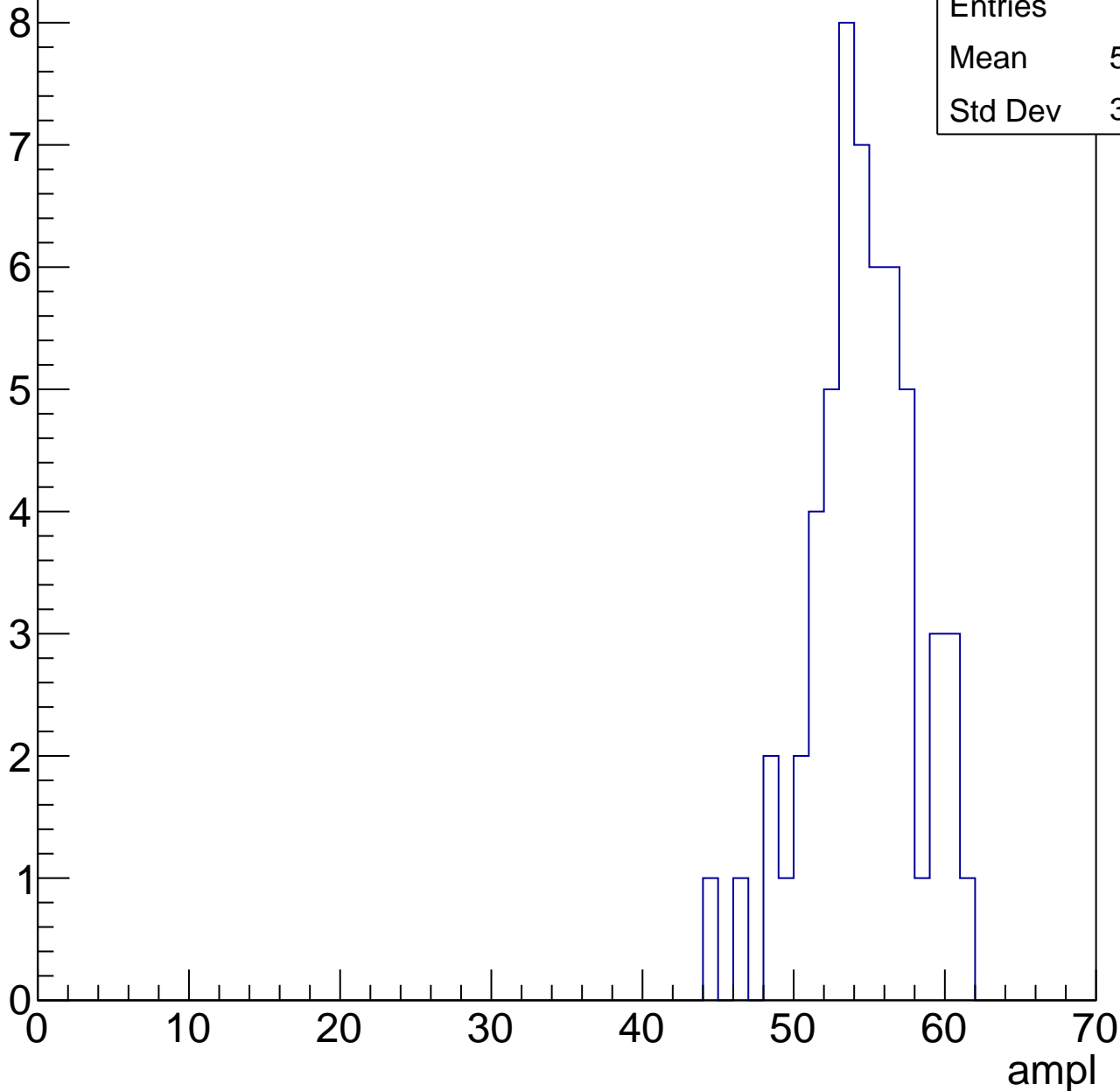


# B1L103S, U11-ch95, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	56
Mean	54.07
Std Dev	3.484

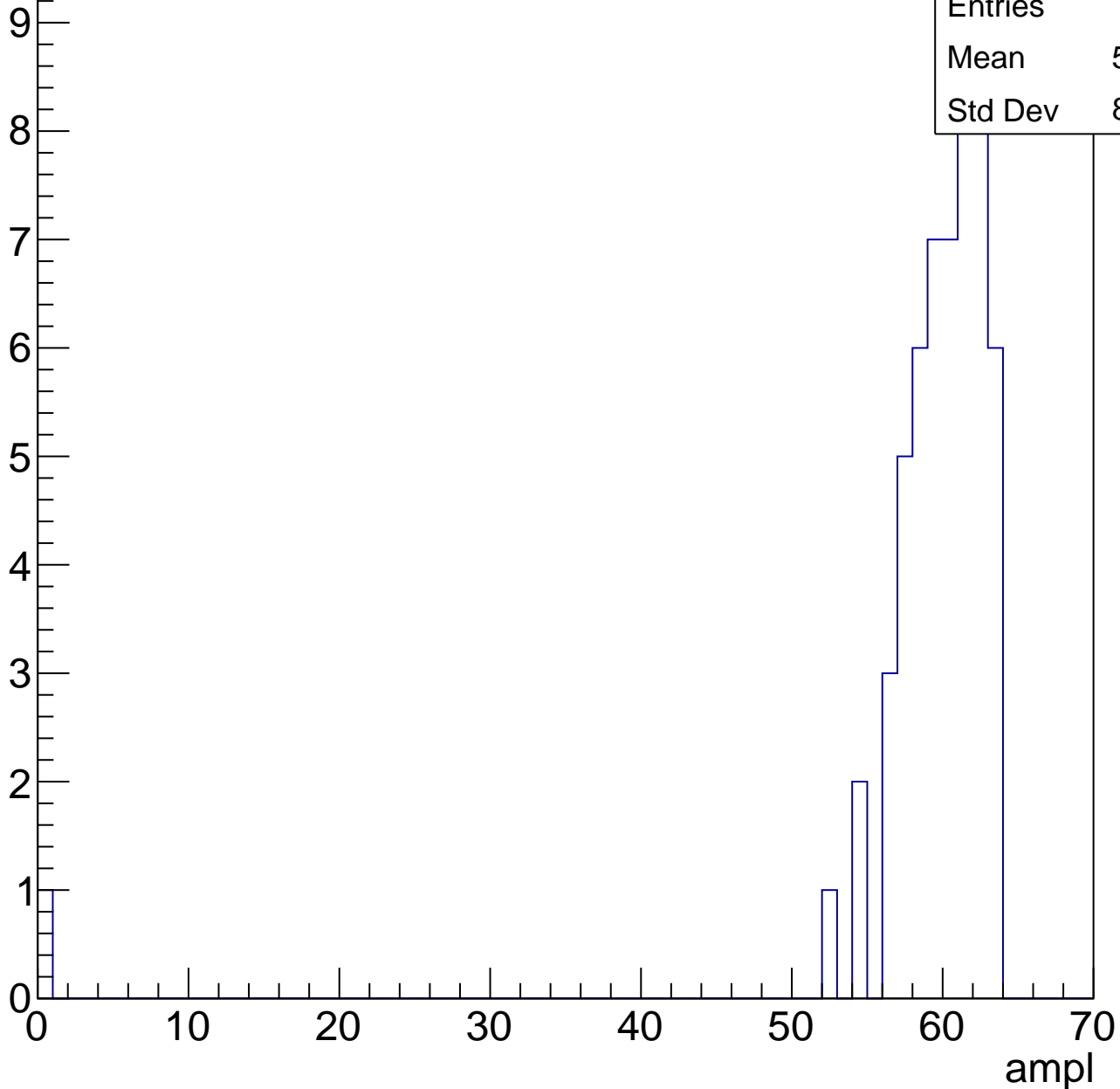


# B1L103S, U11-ch95, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

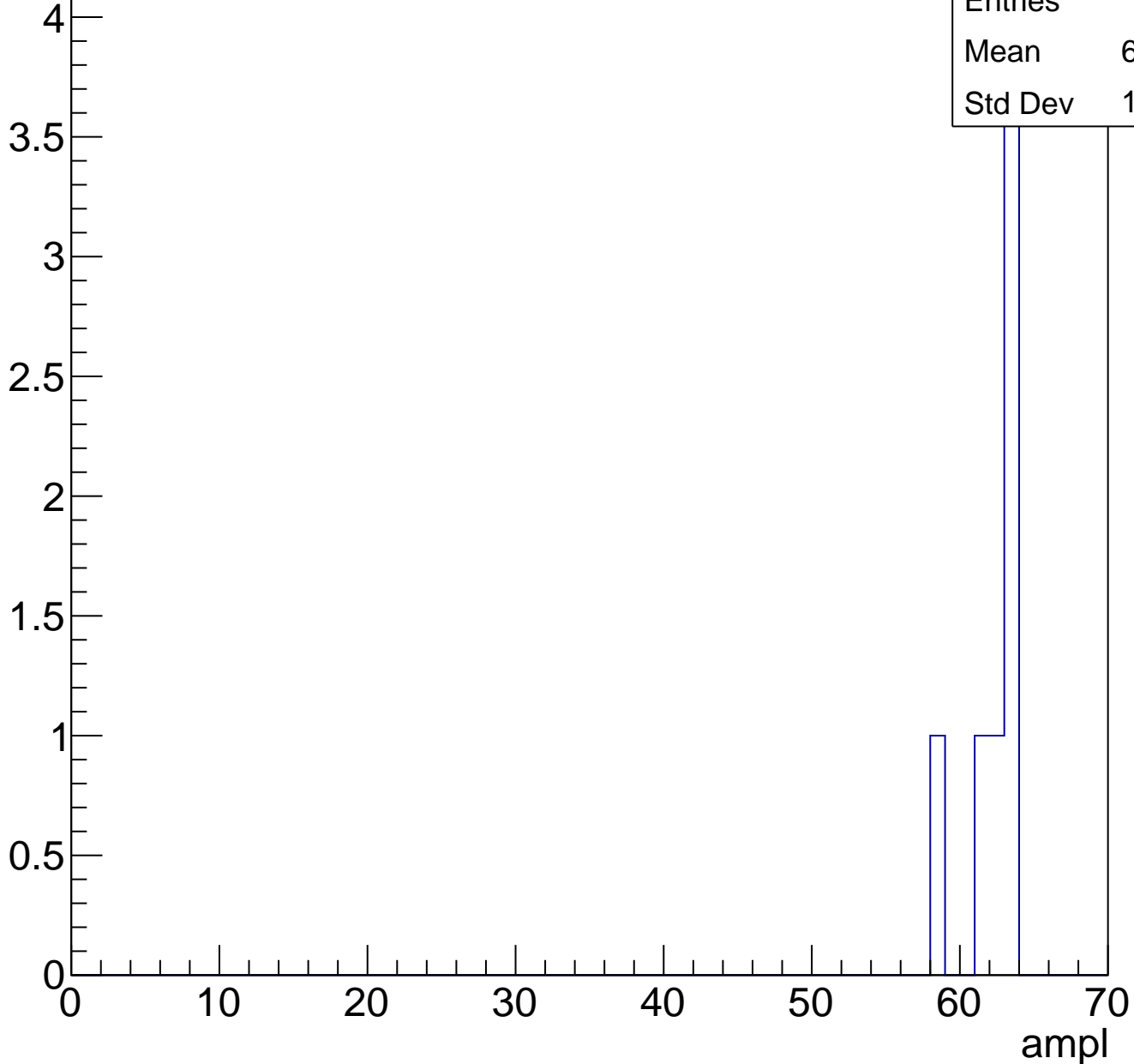
Entries	55
Mean	58.51
Std Dev	8.351



# B1L103S, U11-ch95, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U11-ch95, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L103S, U11-ch96, adc0

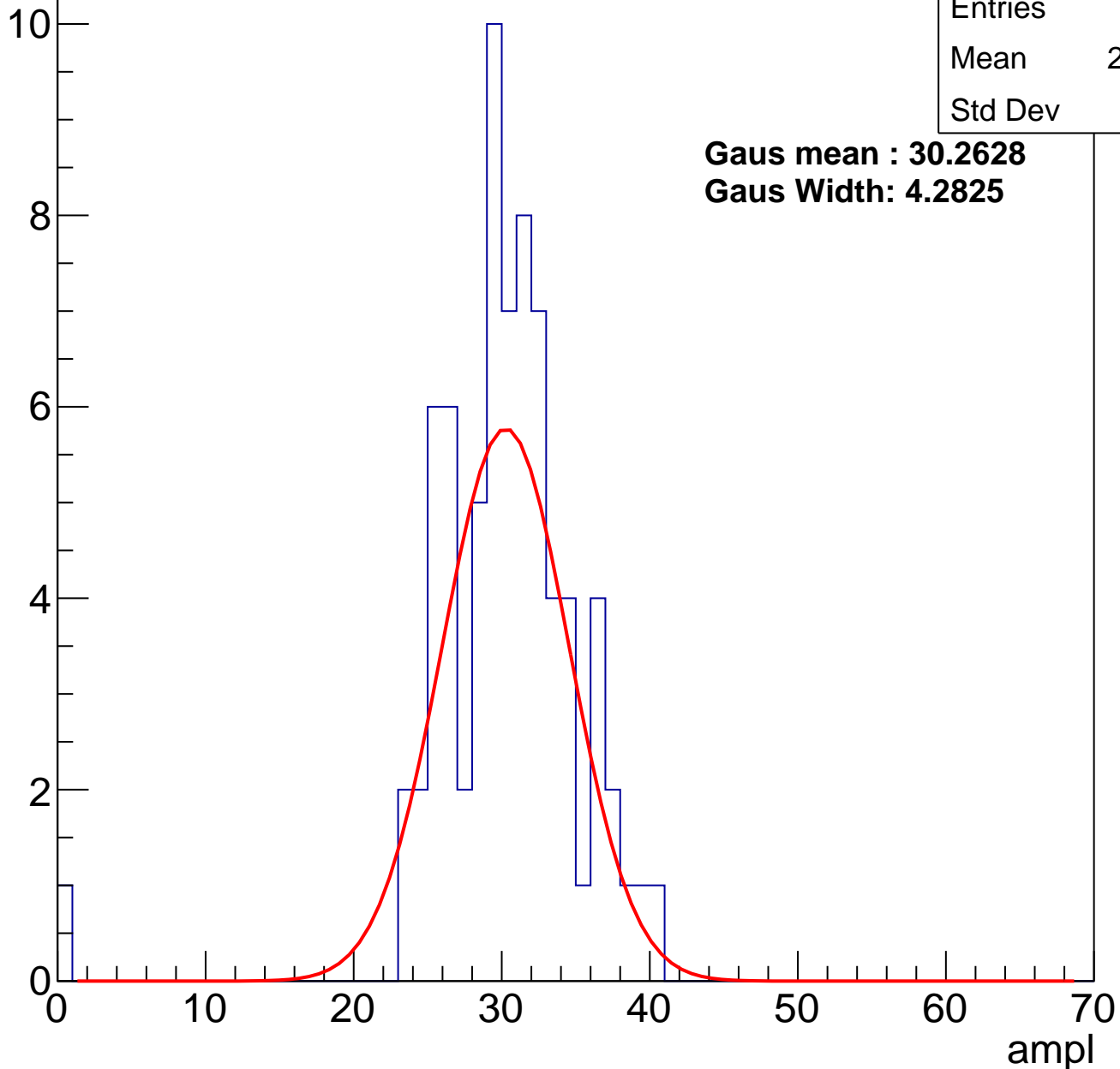
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	74
Mean	29.78
Std Dev	5.21

**Gaus mean : 30.2628**

**Gaus Width: 4.2825**

Entry



# B1L103S, U11-ch96, adc1

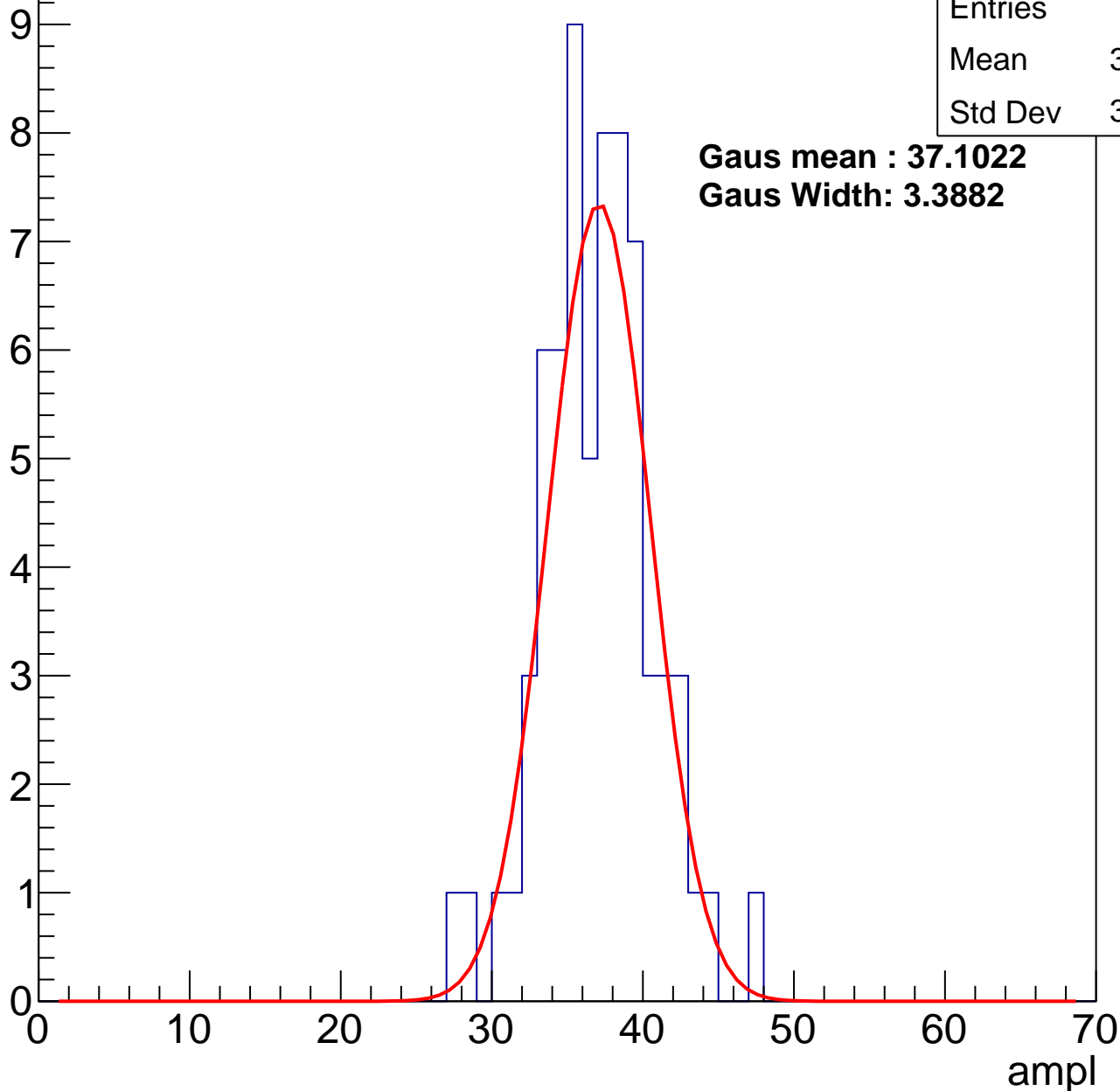
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	68
Mean	36.54
Std Dev	3.615

**Gaus mean : 37.1022**

**Gaus Width: 3.3882**

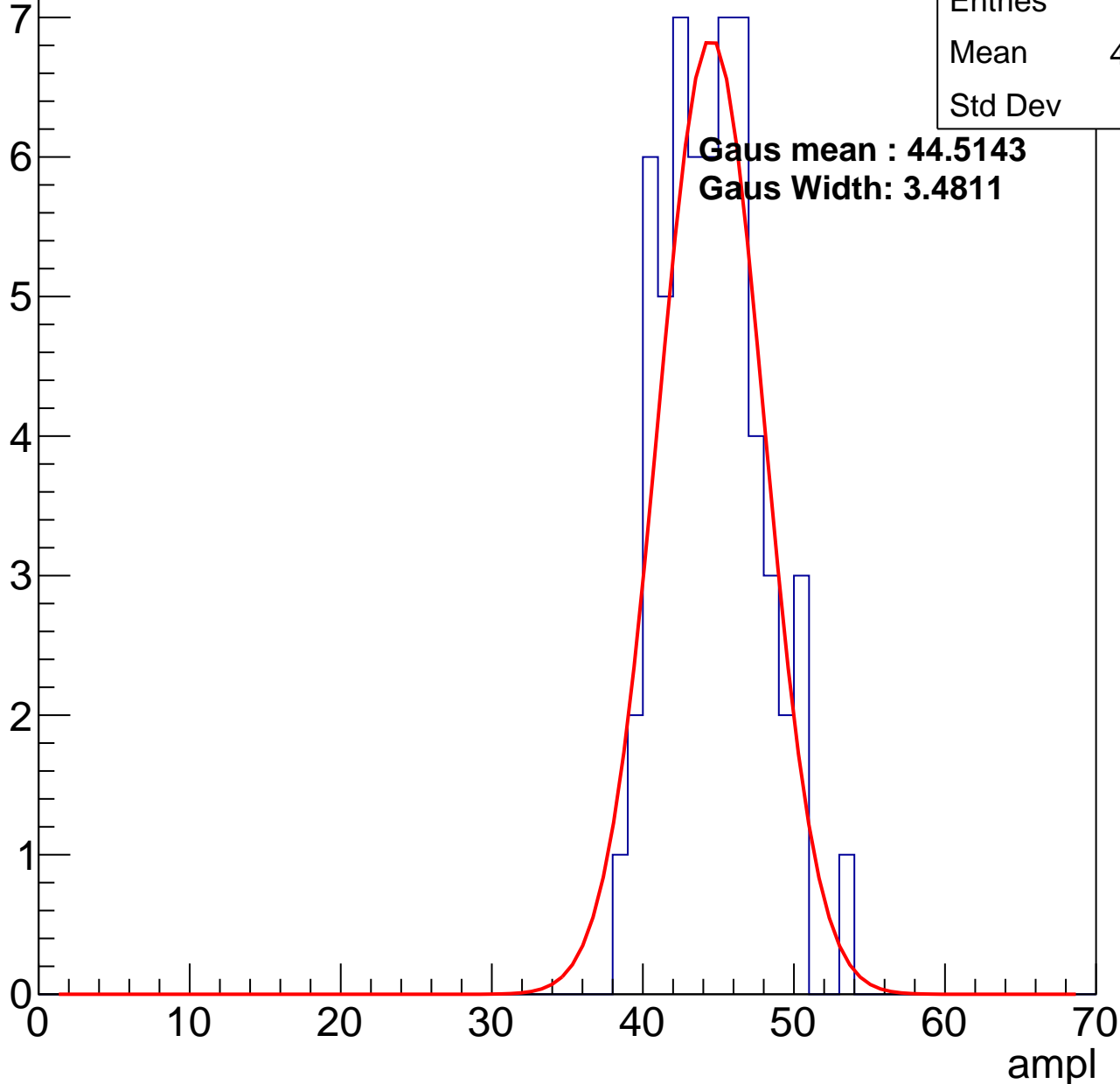


# B1L103S, U11-ch96, adc2

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	60
Mean	44.12
Std Dev	3.21

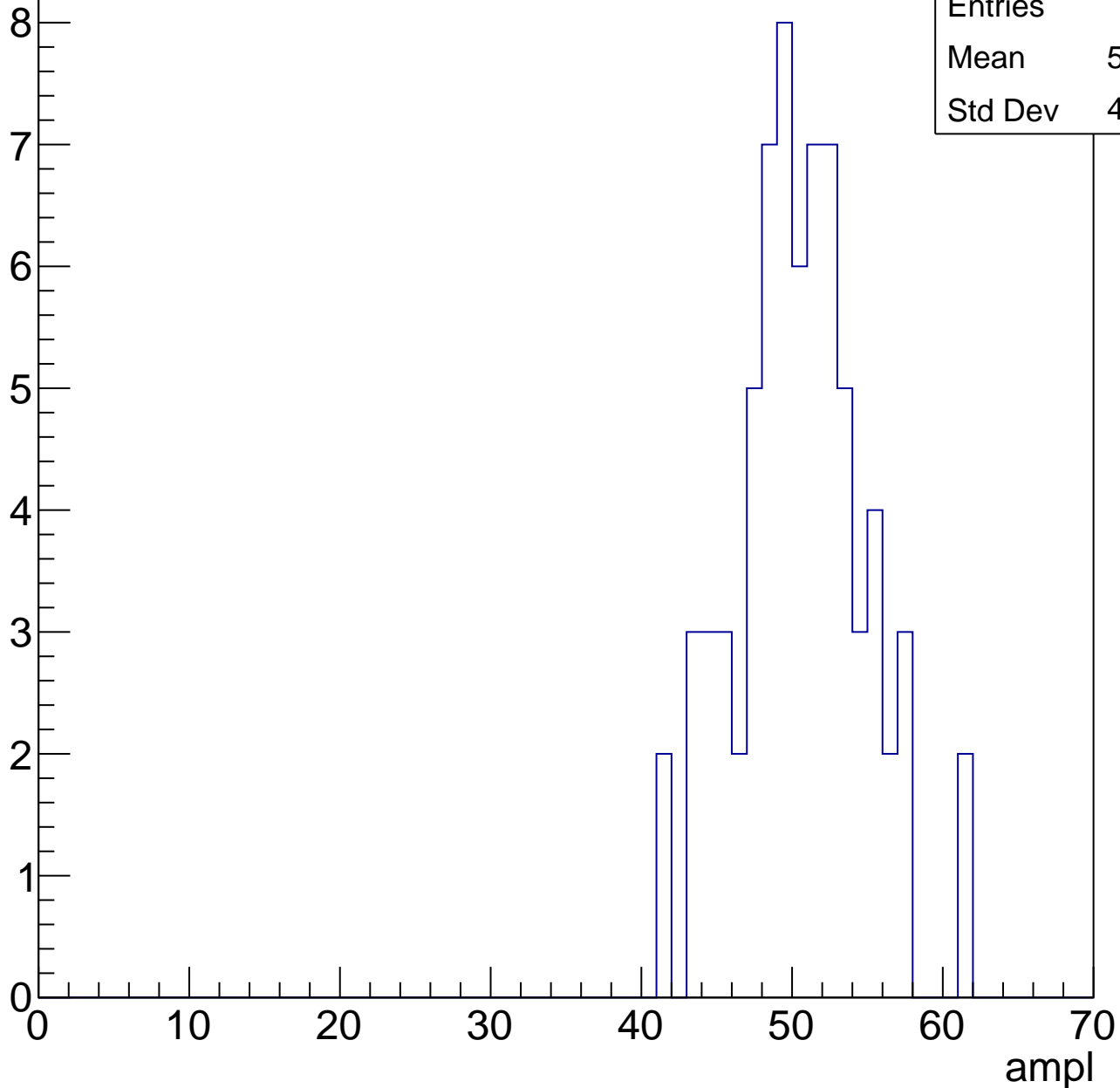


# B1L103S, U11-ch96, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	72
Mean	50.08
Std Dev	4.239

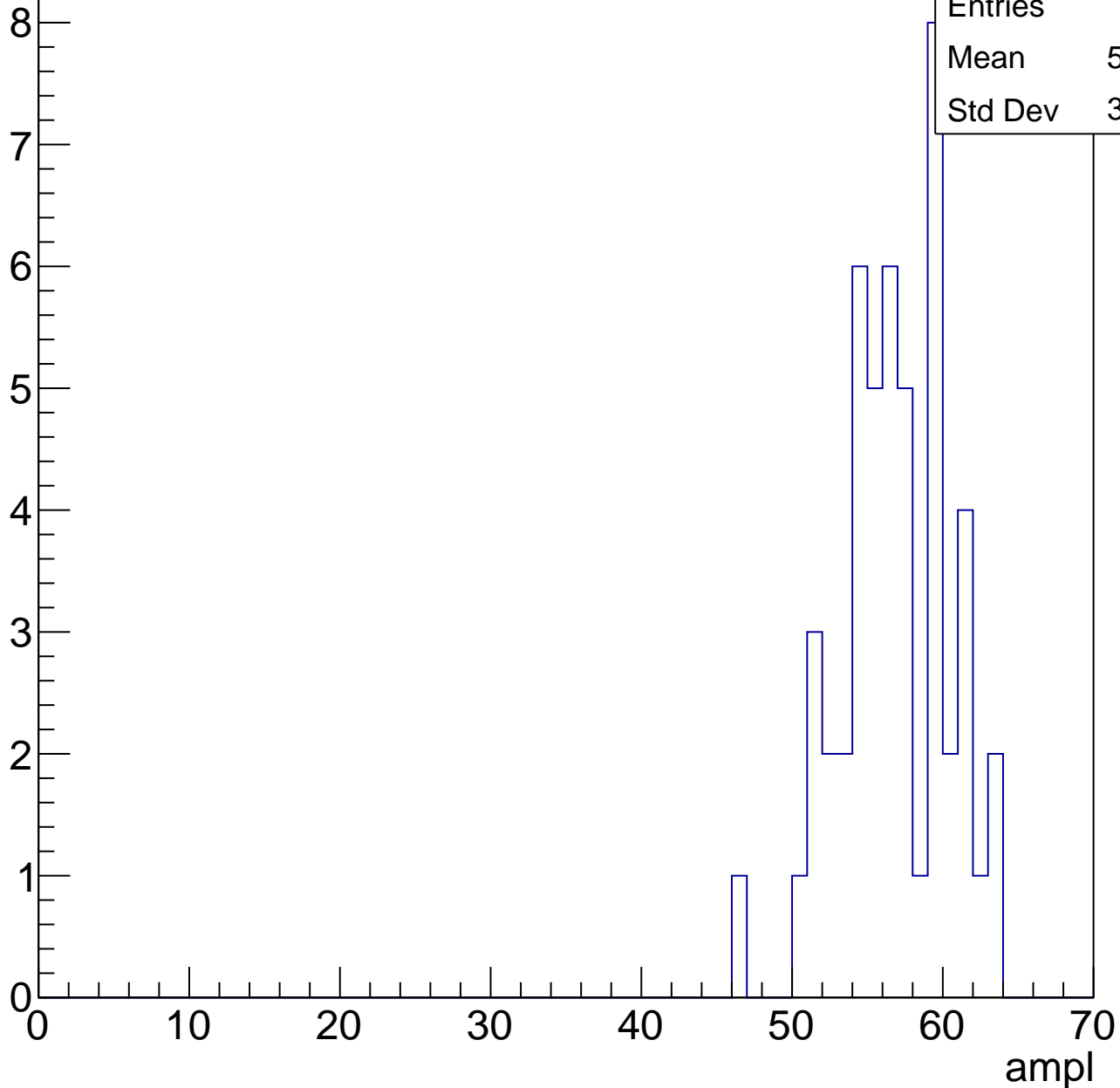


# B1L103S, U11-ch96, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

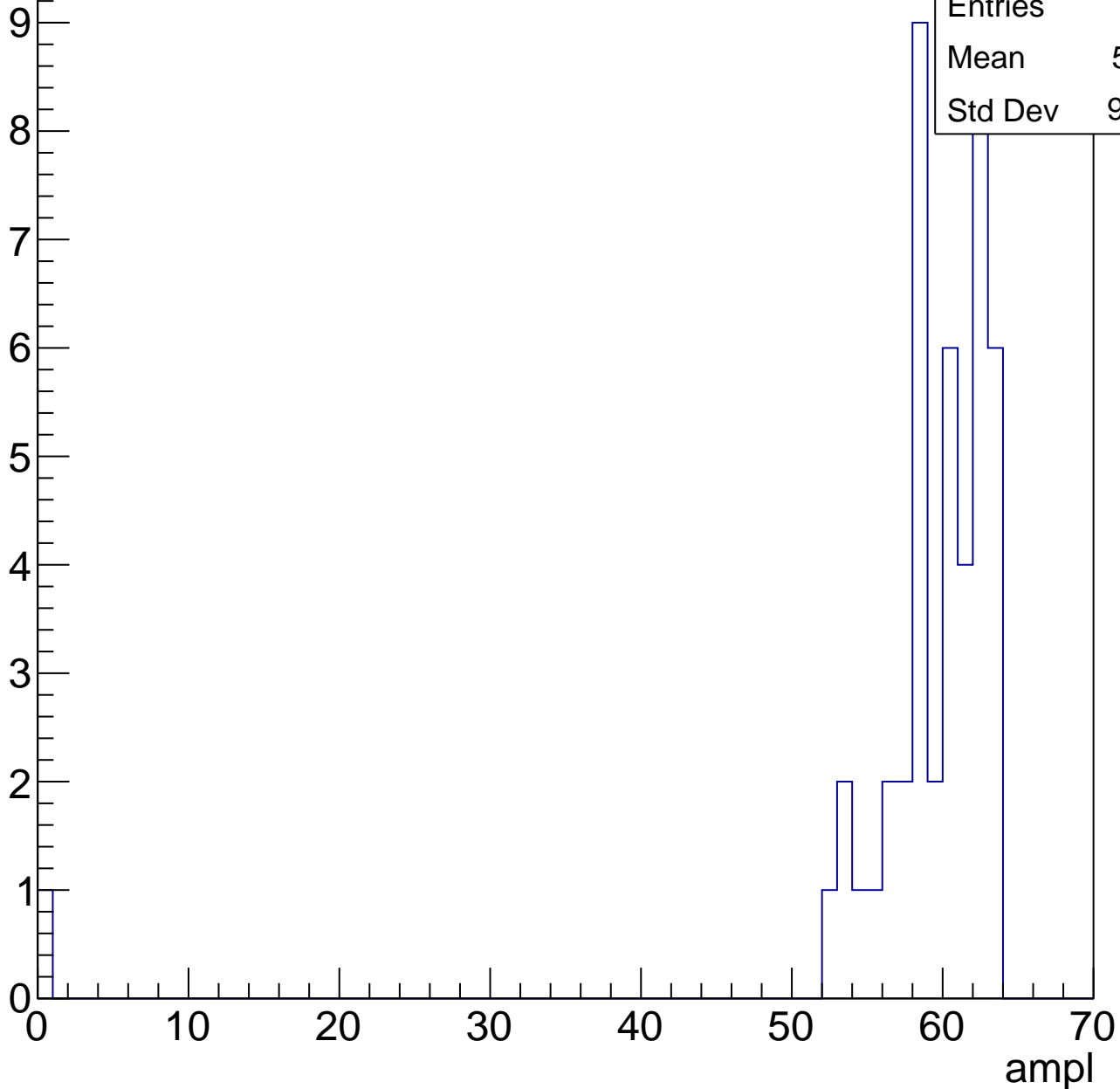
Entries	49
Mean	56.35
Std Dev	3.589



# B1L103S, U11-ch96, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U11-ch96, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

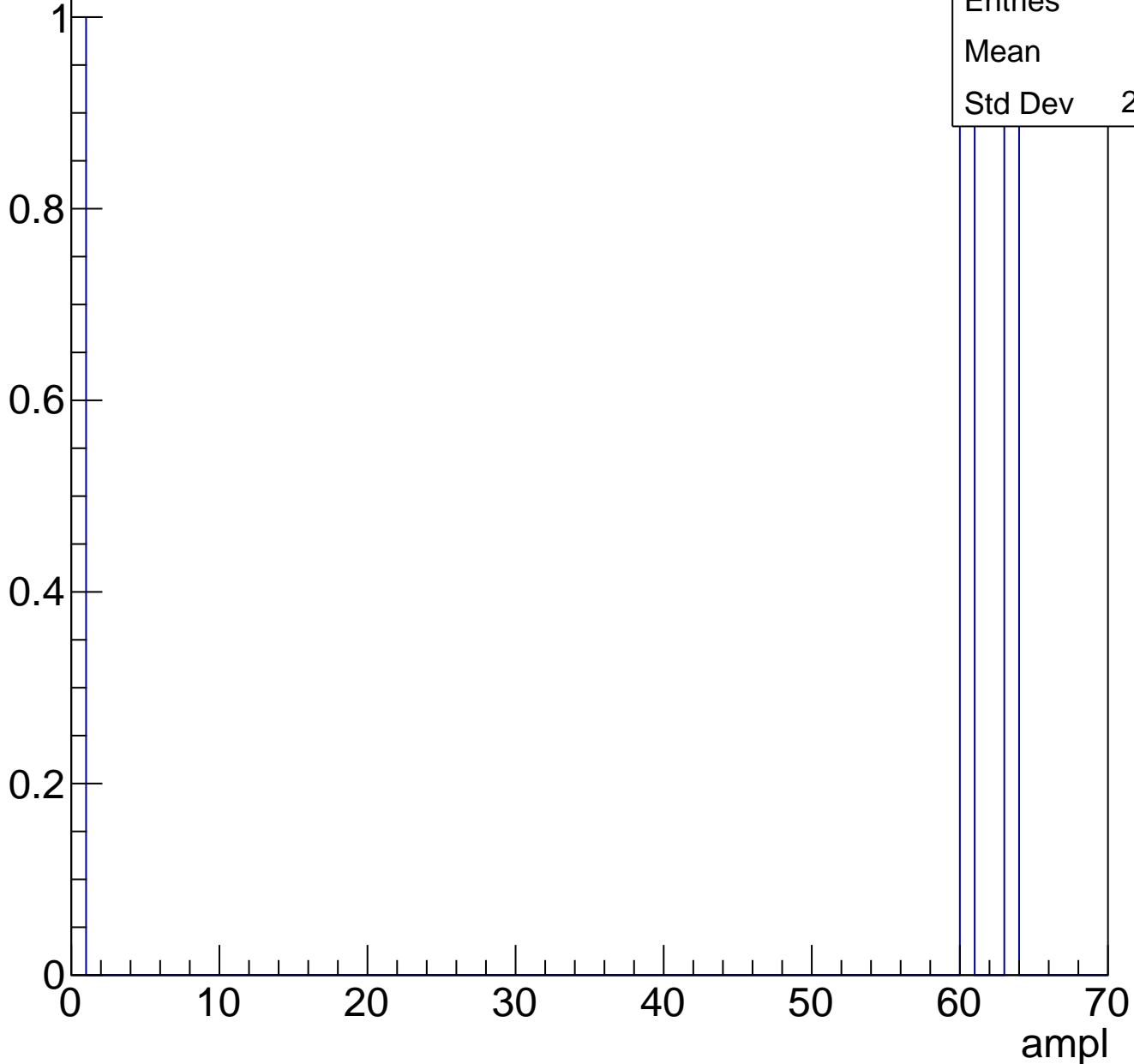




# B1L103S, U11-ch96, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U11-ch97, adc0

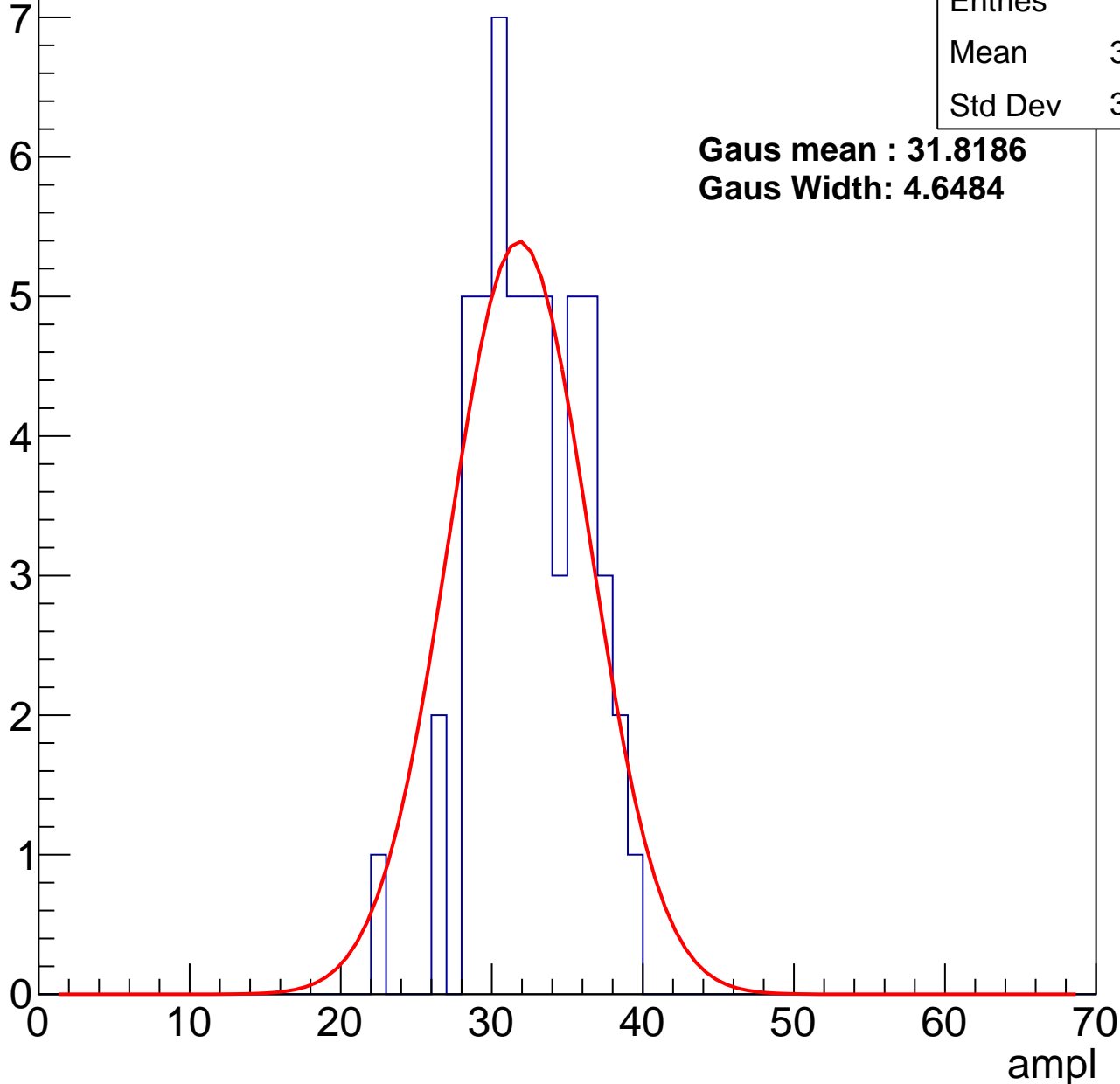
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	54
Mean	32.07
Std Dev	3.516

**Gaus mean : 31.8186**

**Gaus Width: 4.6484**



# B1L103S, U11-ch97, adc1

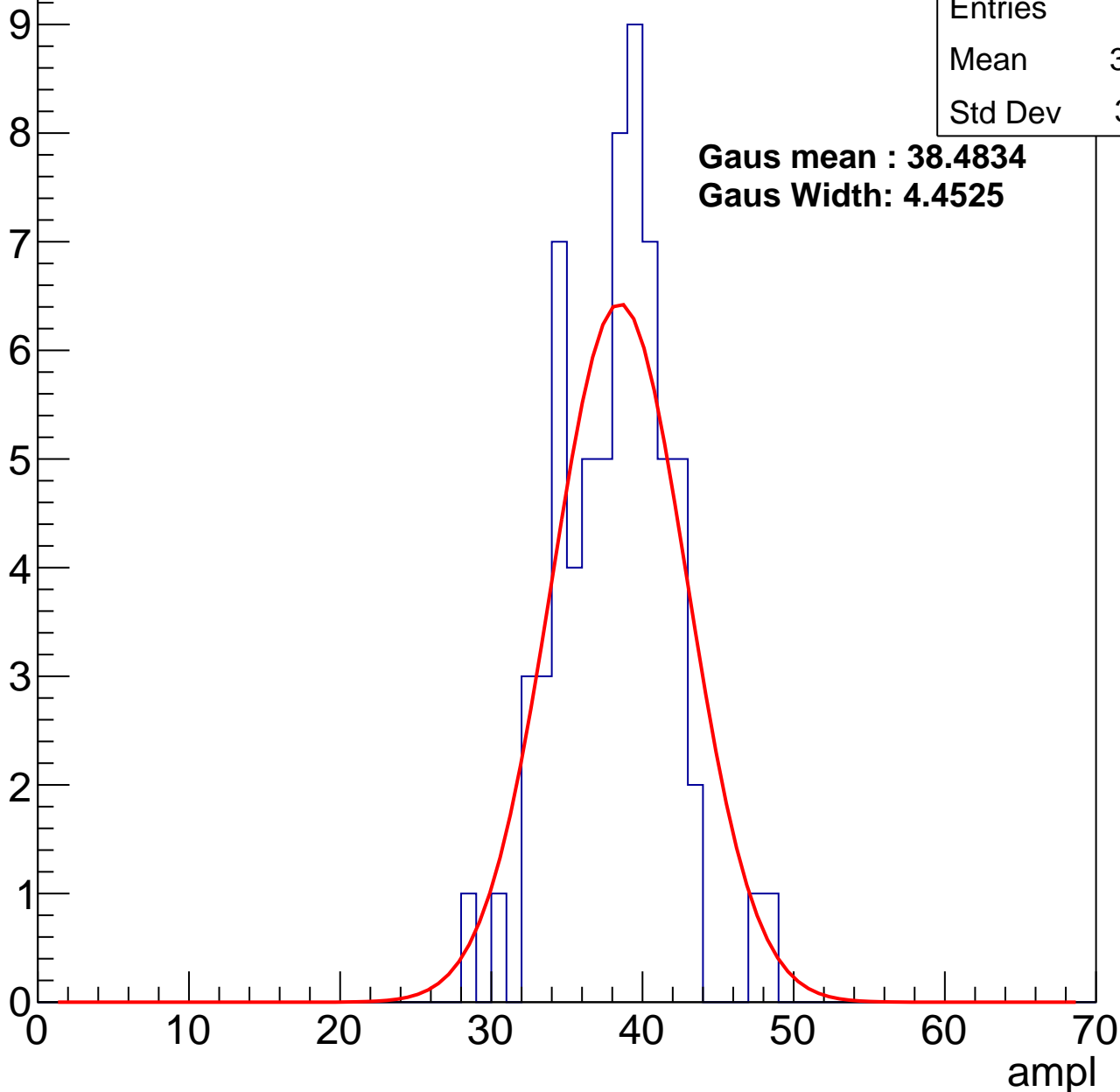
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	37.72
Std Dev	3.681

**Gaus mean : 38.4834**

**Gaus Width: 4.4525**



# B1L103S, U11-ch97, adc2

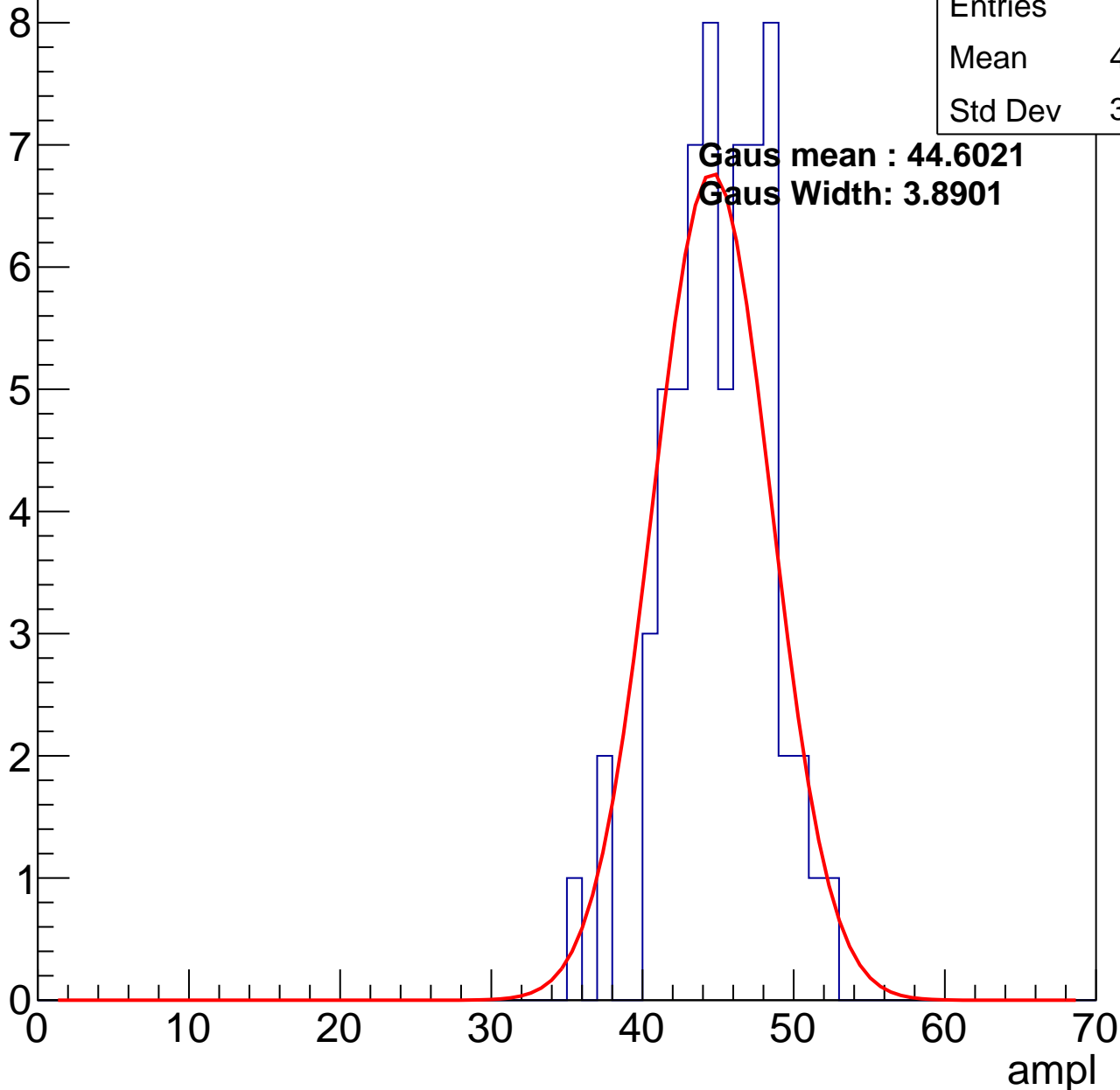
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	44.66
Std Dev	3.378

Gaus mean : 44.6021

Gaus Width: 3.8901

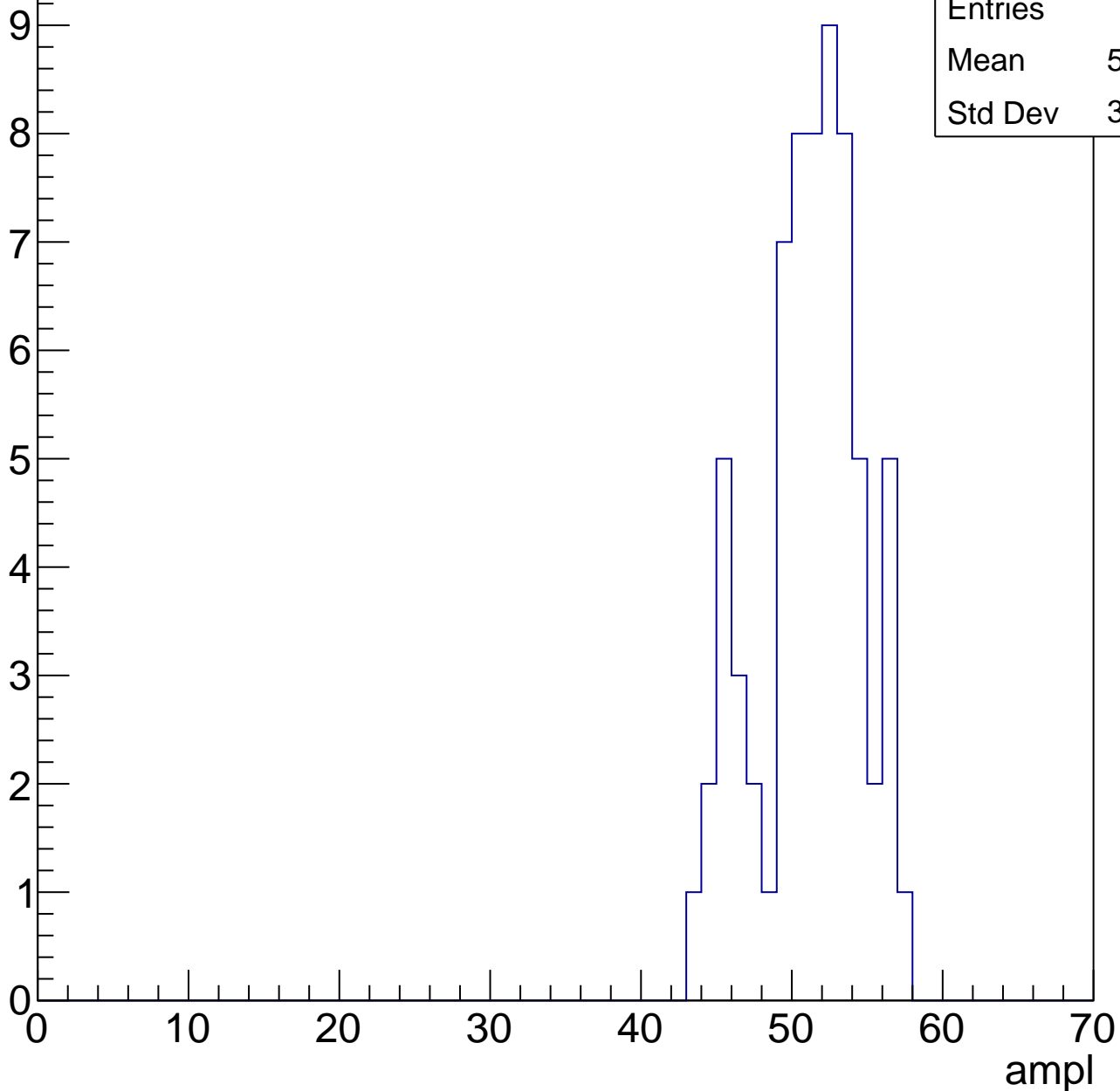


# B1L103S, U11-ch97, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

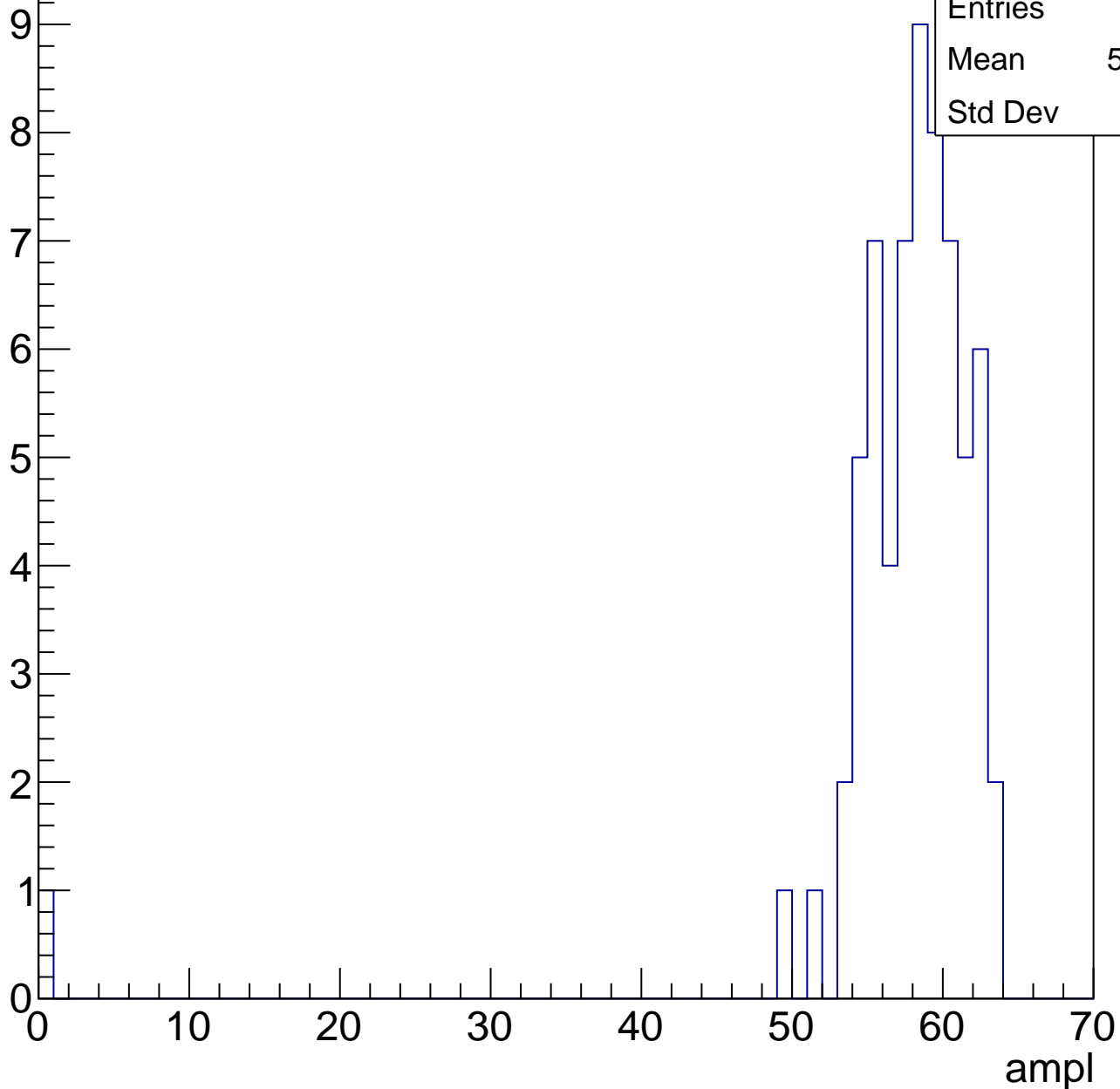
Entries	67
Mean	50.69
Std Dev	3.382



# B1L103S, U11-ch97, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

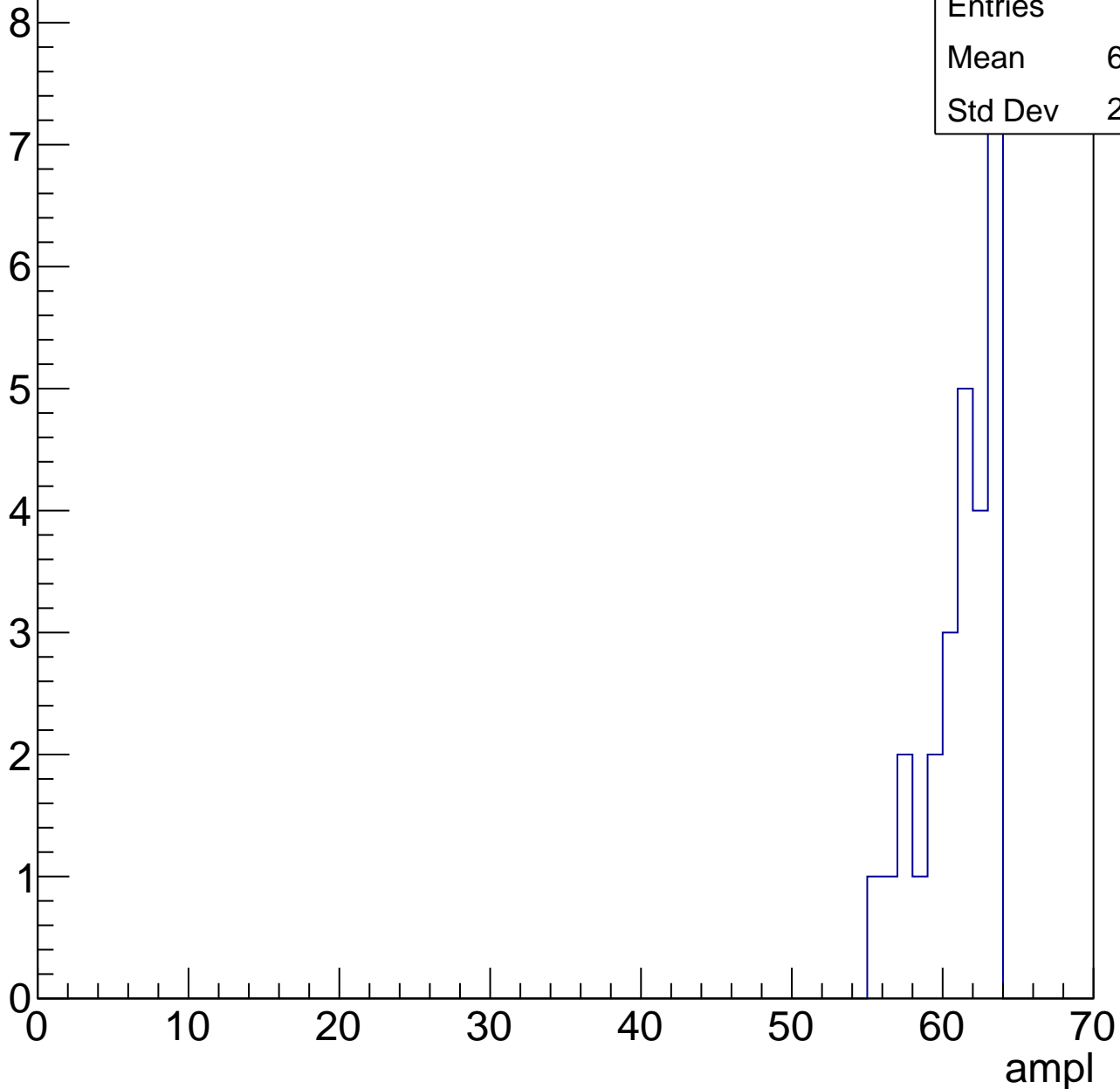


# B1L103S, U11-ch97, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	27
Mean	60.67
Std Dev	2.325



# B1L103S, U11-ch97, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0



# B1L103S, U11-ch97, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U11-ch98, adc0

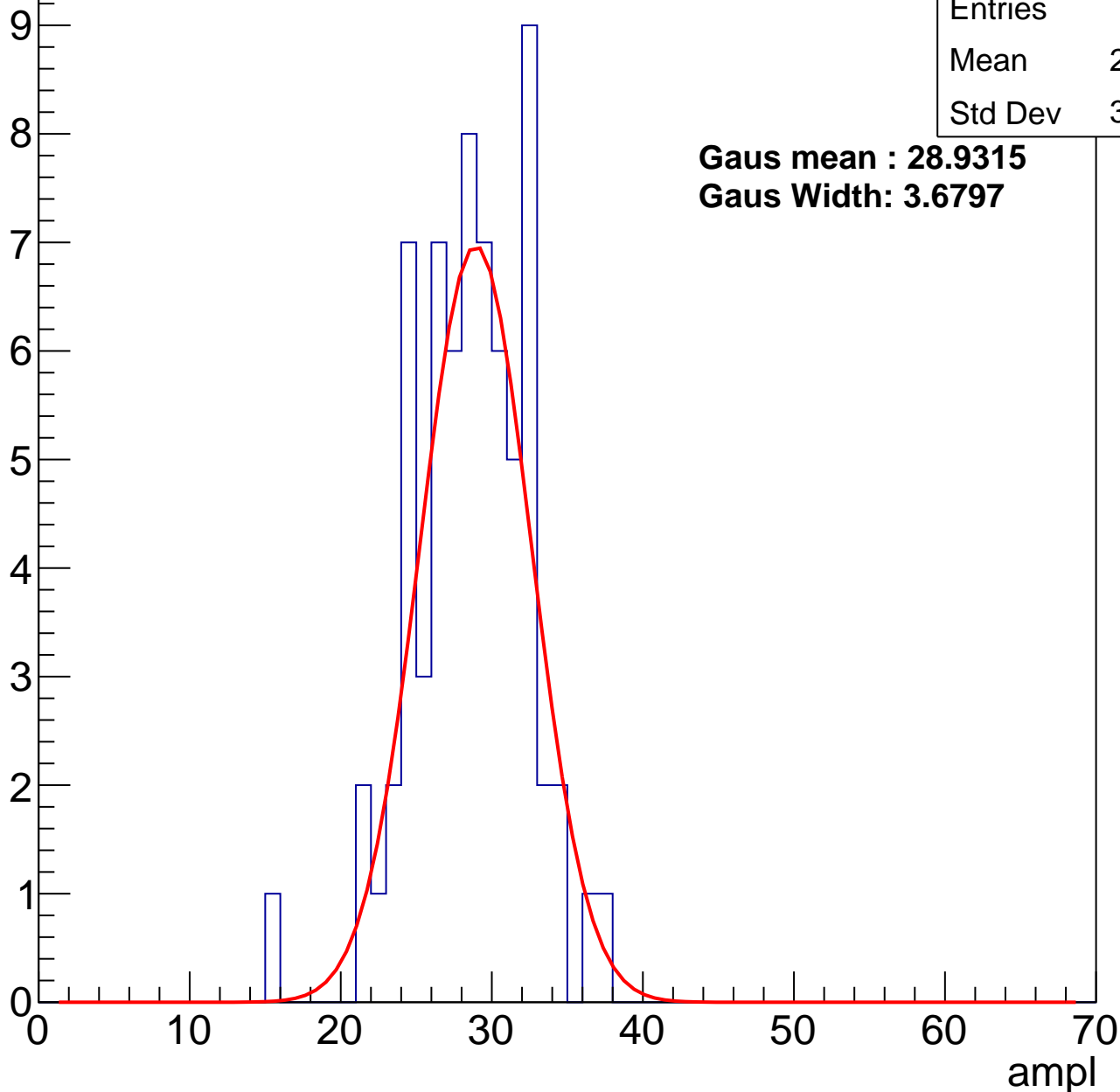
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	70
Mean	28.13
Std Dev	3.802

**Gaus mean : 28.9315**

**Gaus Width: 3.6797**



# B1L103S, U11-ch98, adc1

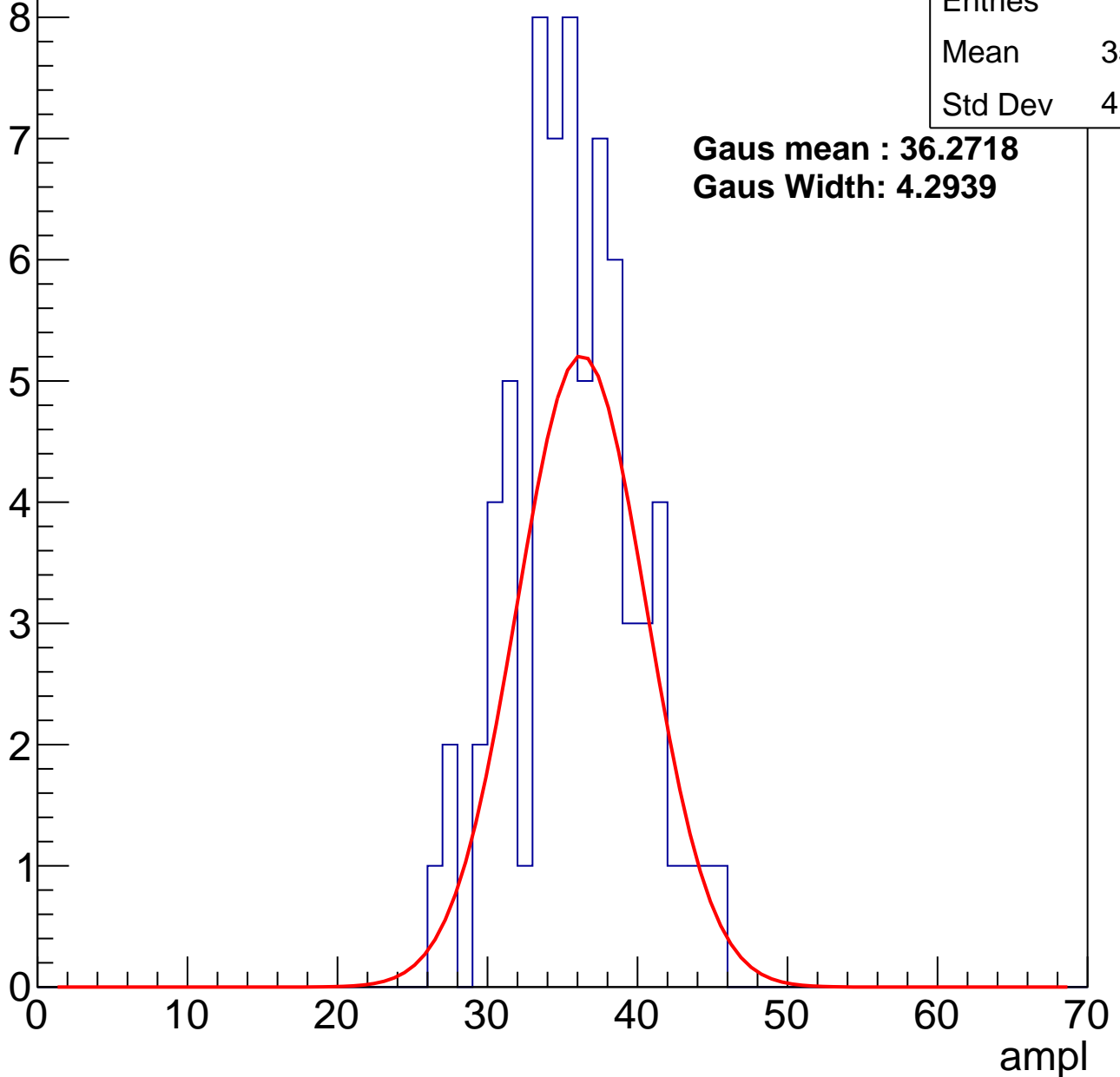
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	70
Mean	35.27
Std Dev	4.056

**Gaus mean : 36.2718**

**Gaus Width: 4.2939**



# B1L103S, U11-ch98, adc2

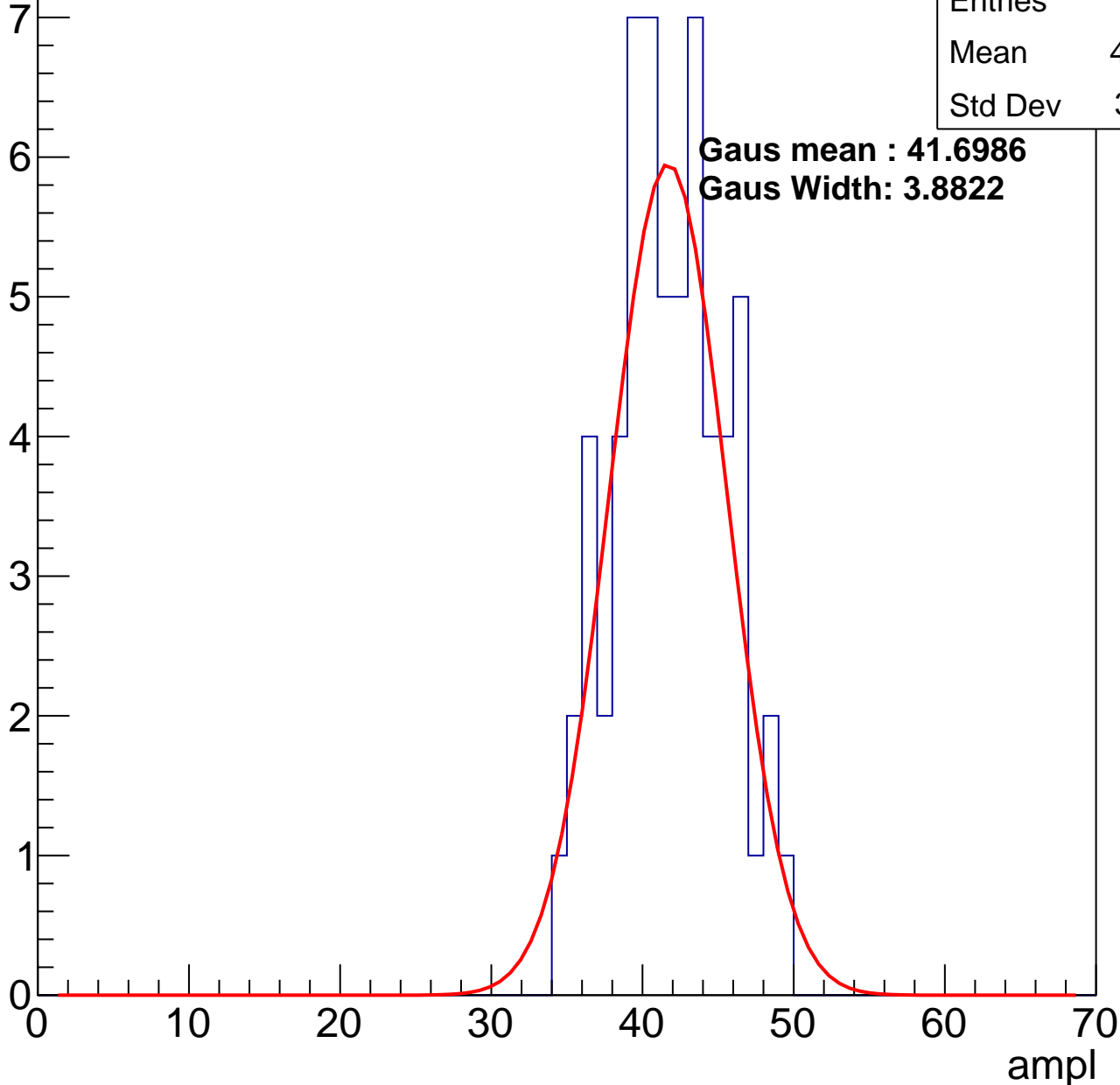
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	61
Mean	41.33
Std Dev	3.561

**Gaus mean : 41.6986**

**Gaus Width: 3.8822**

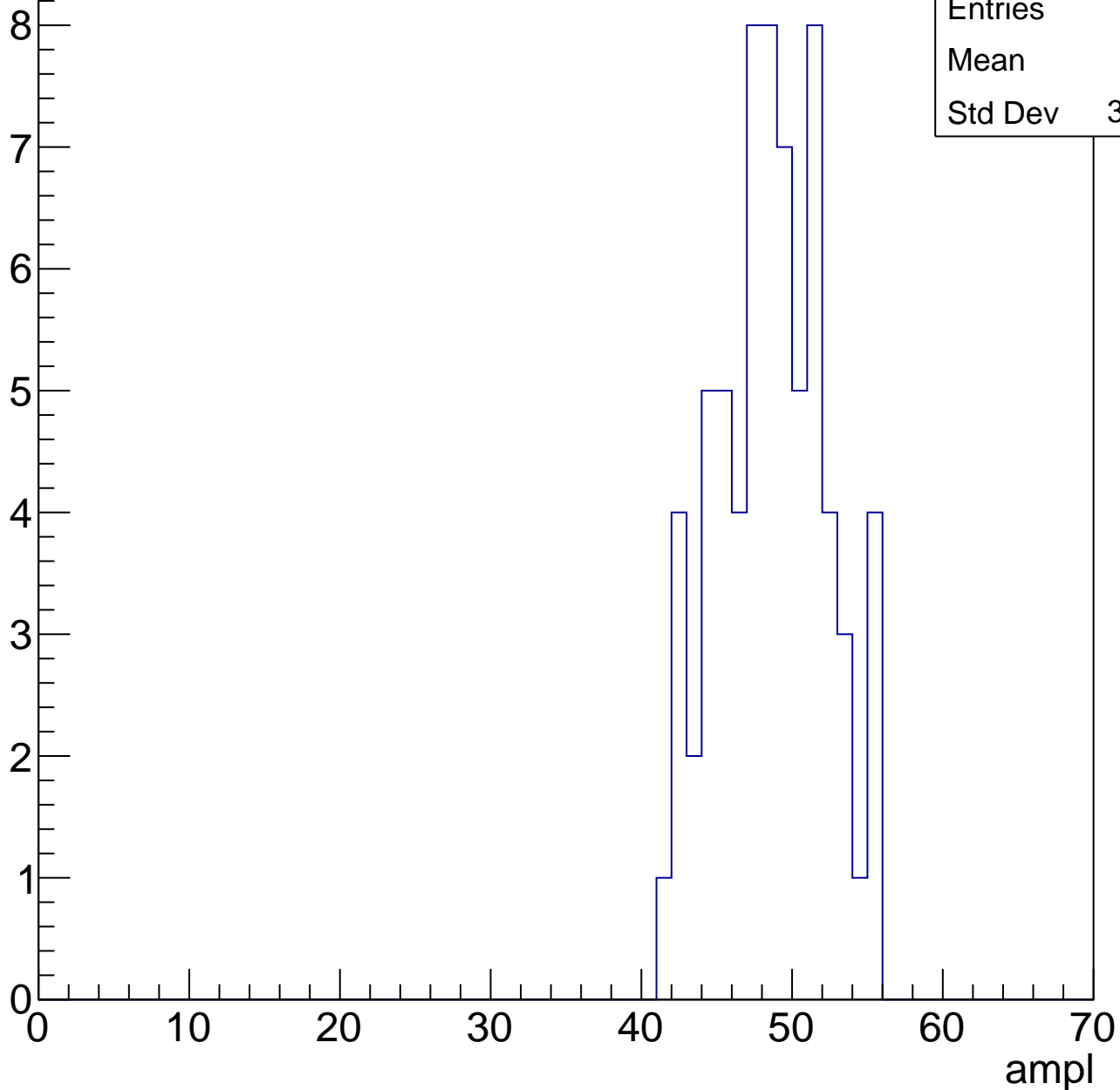


# B1L103S, U11-ch98, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	69
Mean	48.2
Std Dev	3.529

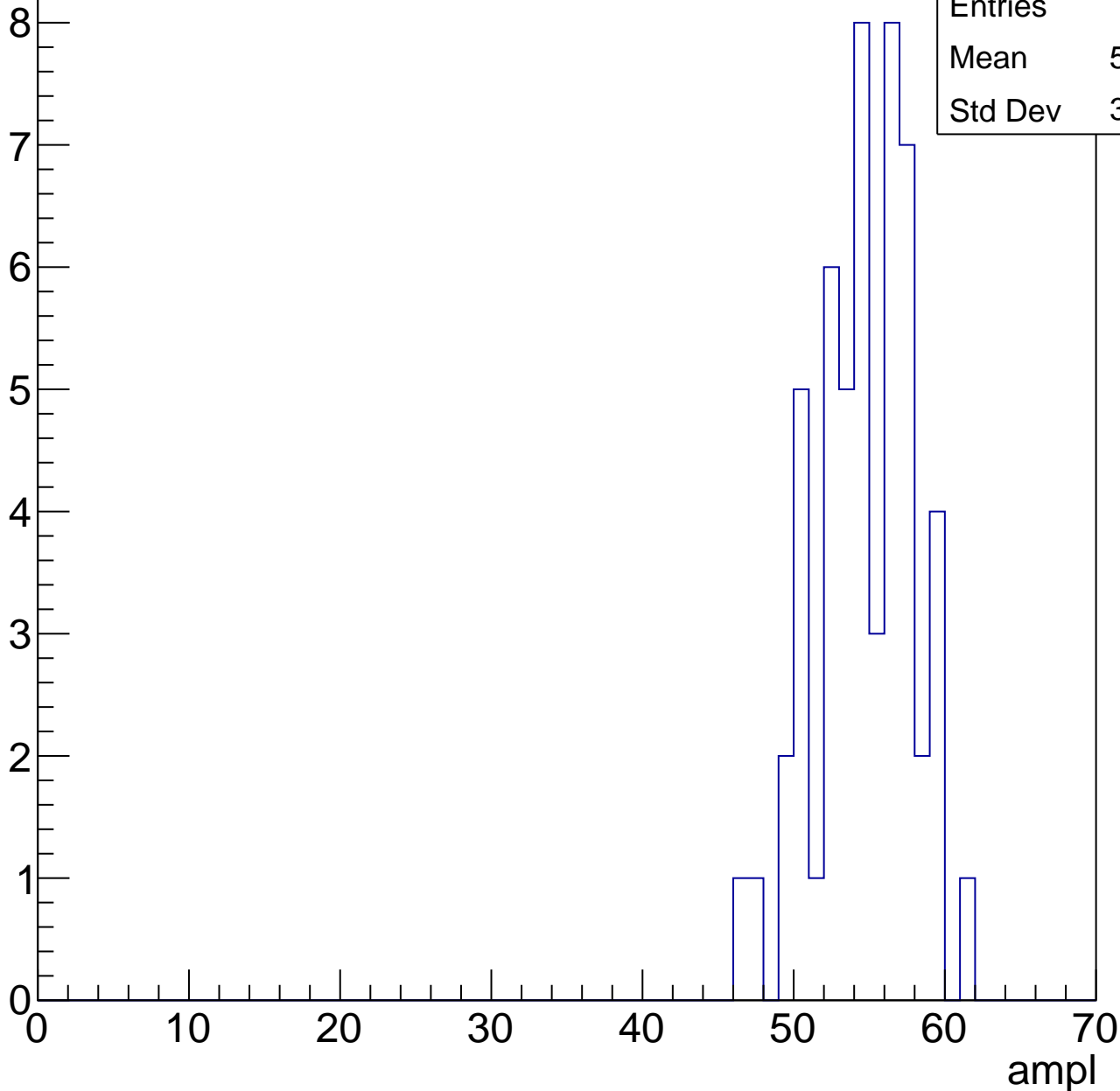


# B1L103S, U11-ch98, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	54
Mean	54.19
Std Dev	3.215



# B1L103S, U11-ch98, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	55
Mean	59.07
Std Dev	2.709

Entry

10

8

6

4

2

0

0

10

20

30

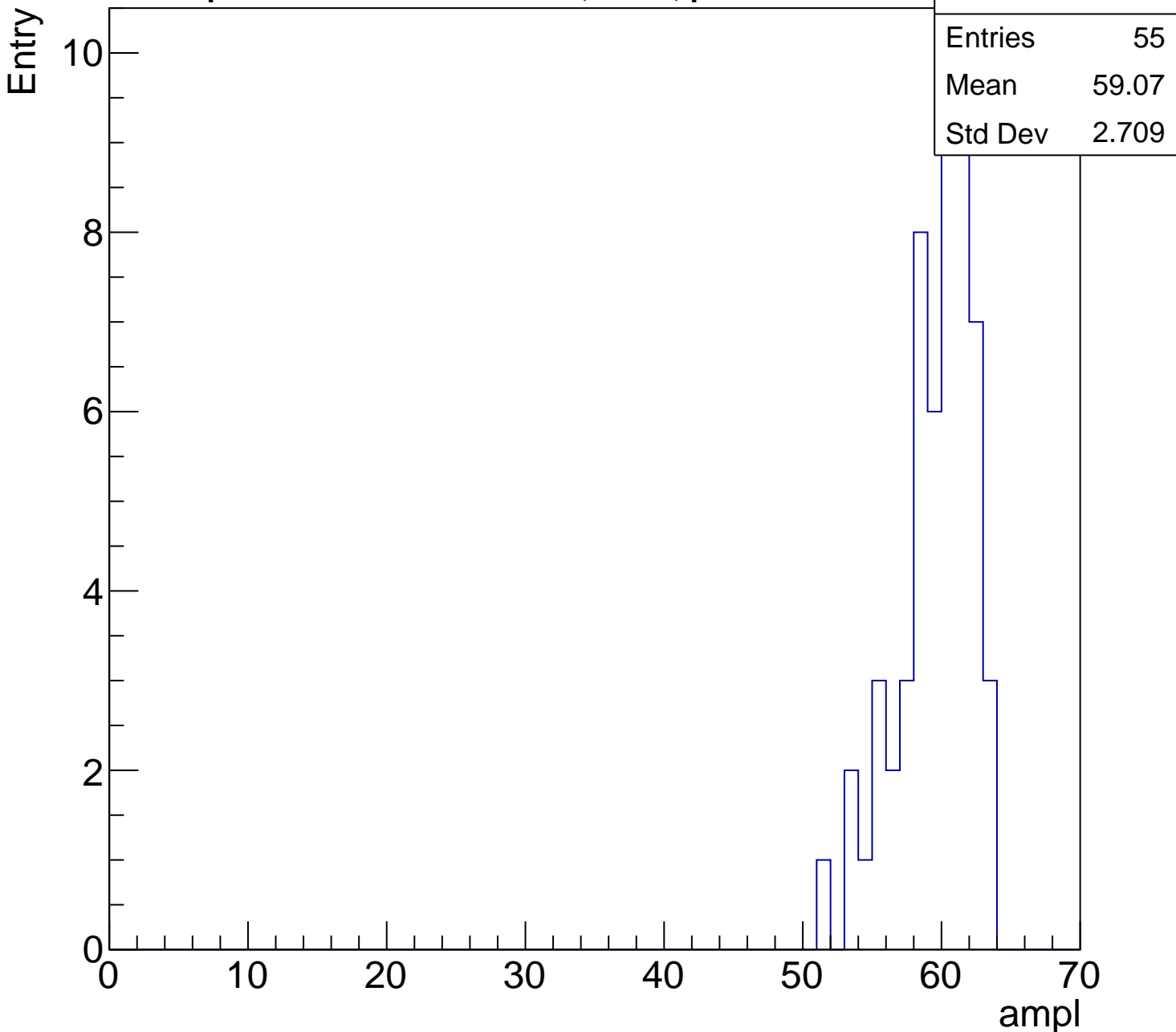
40

50

60

ampl

70

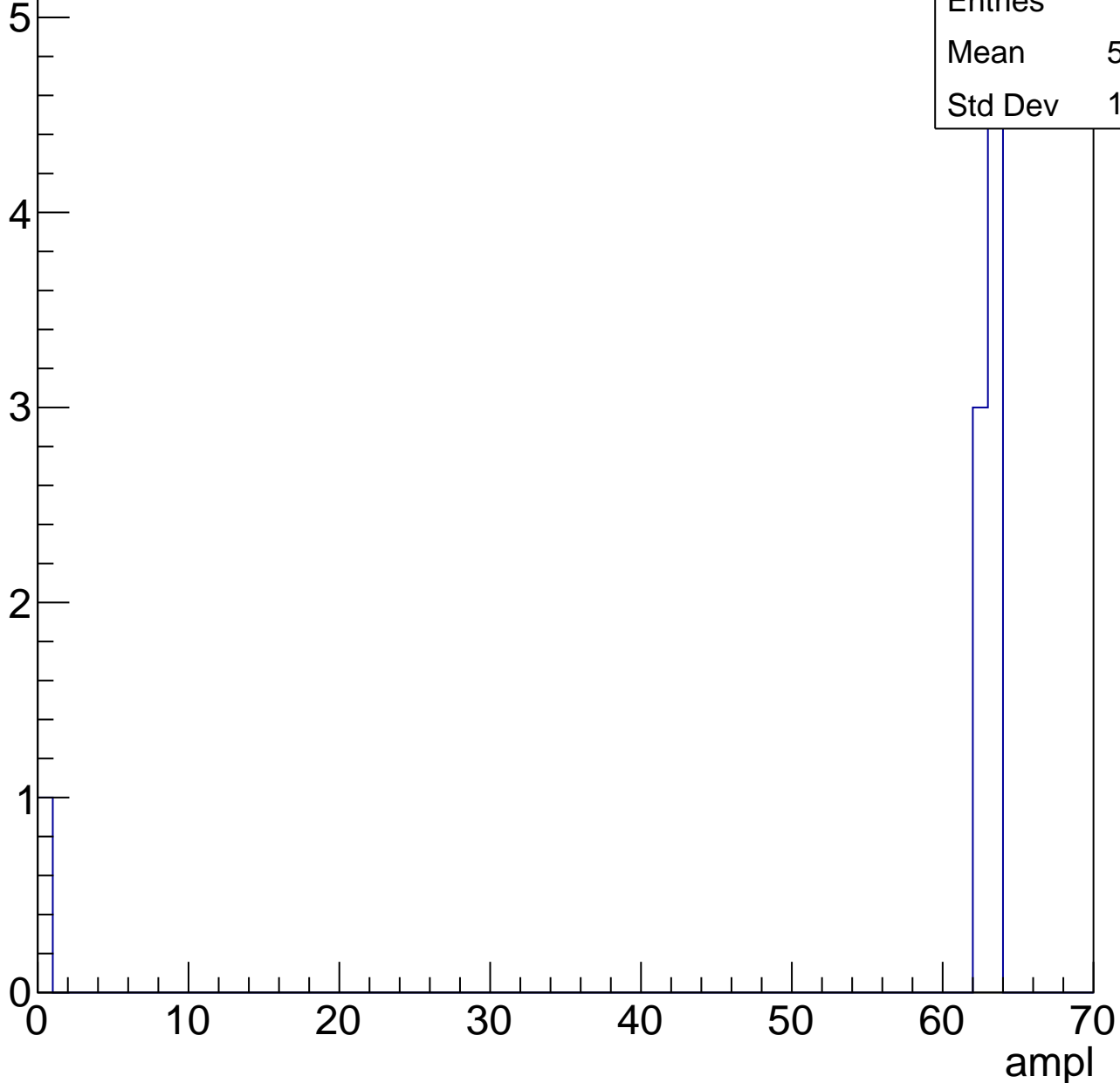


# B1L103S, U11-ch98, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	9
Mean	55.67
Std Dev	19.69





# B1L103S, U11-ch98, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U11-ch99, adc0

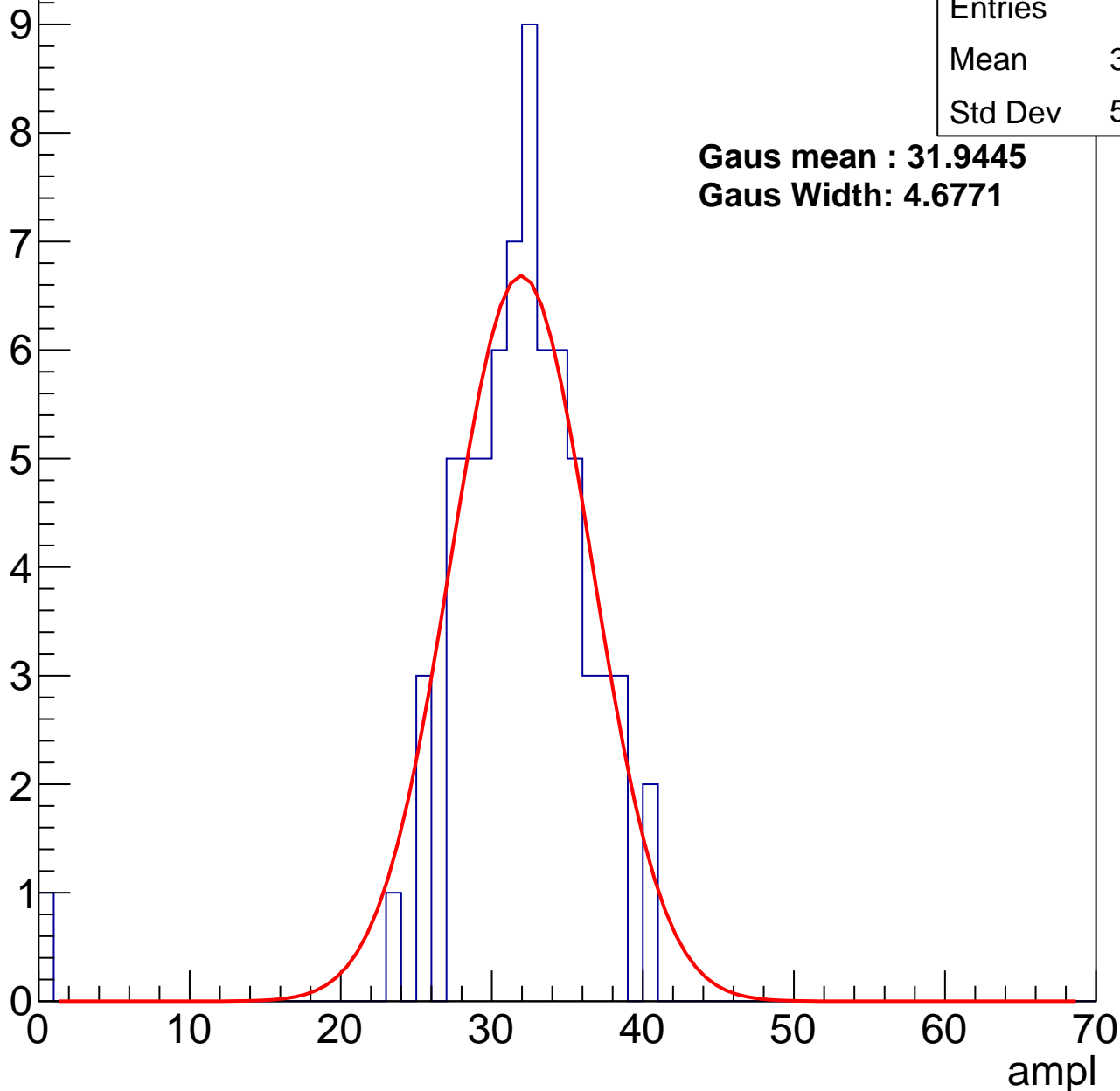
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	70
Mean	31.33
Std Dev	5.258

**Gaus mean : 31.9445**

**Gaus Width: 4.6771**



# B1L103S, U11-ch99, adc1

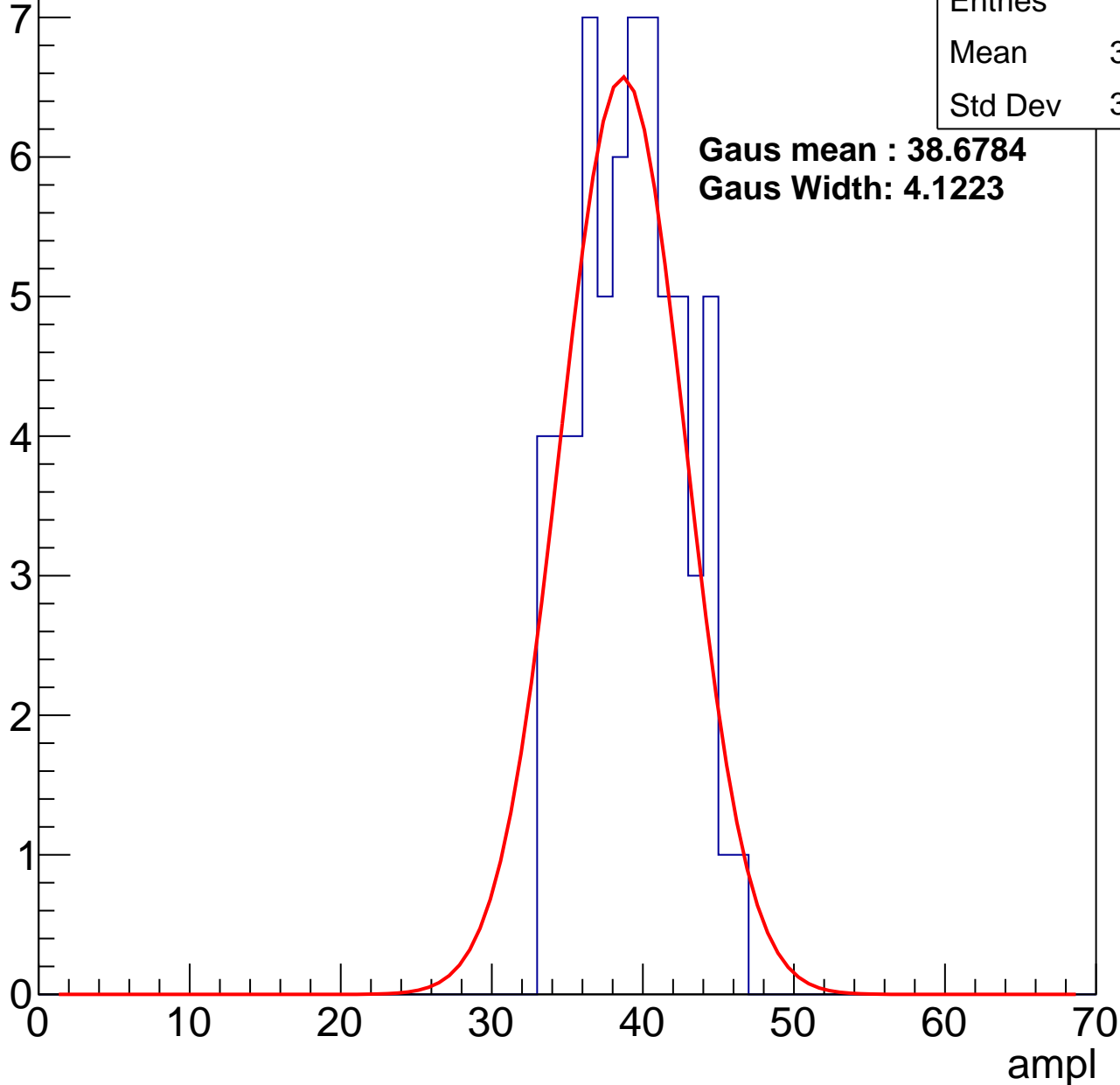
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	38.77
Std Dev	3.362

**Gaus mean : 38.6784**

**Gaus Width: 4.1223**



# B1L103S, U11-ch99, adc2

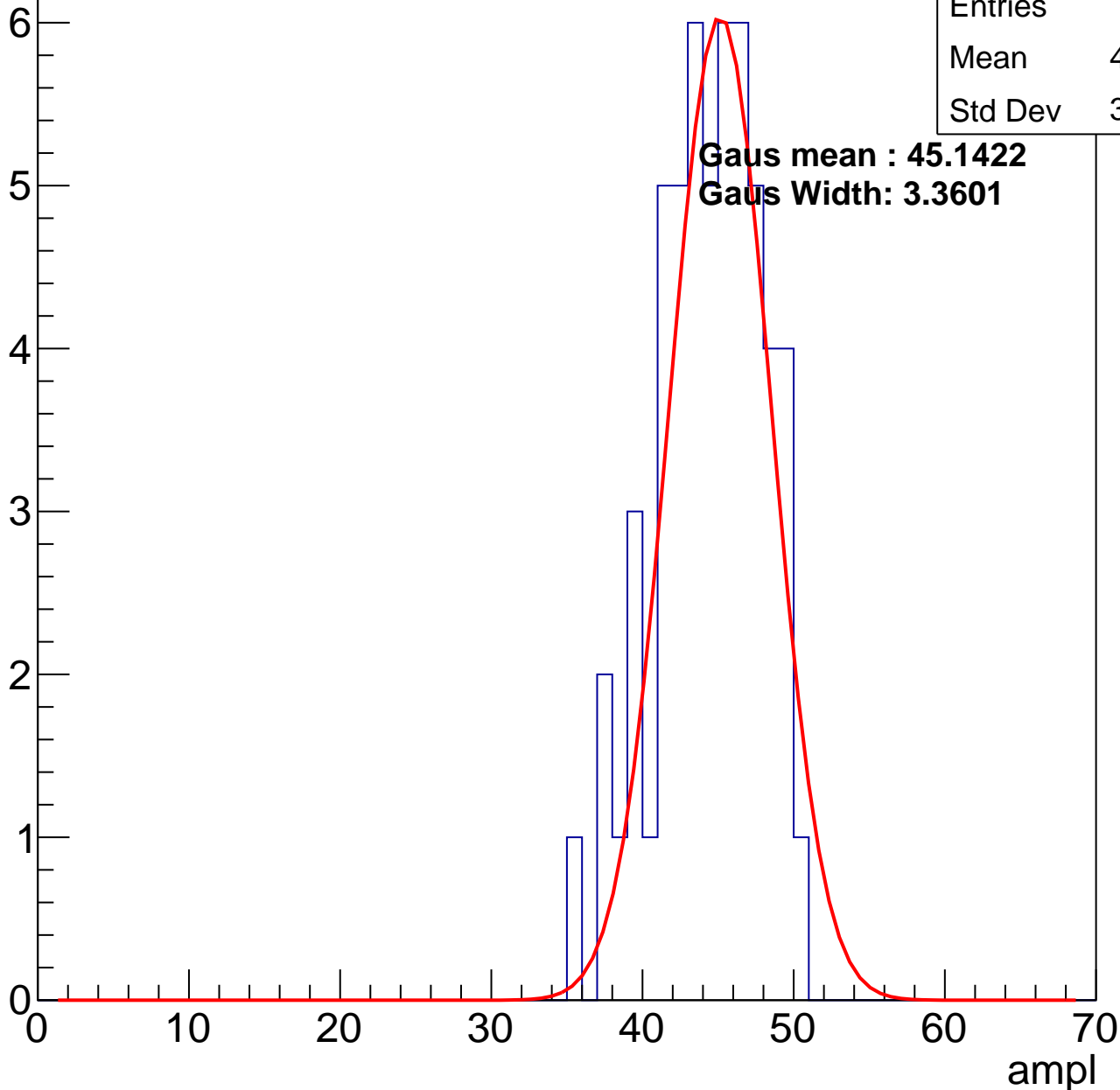
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	55
Mean	43.93
Std Dev	3.442

**Gaus mean : 45.1422**

**Gaus Width: 3.3601**

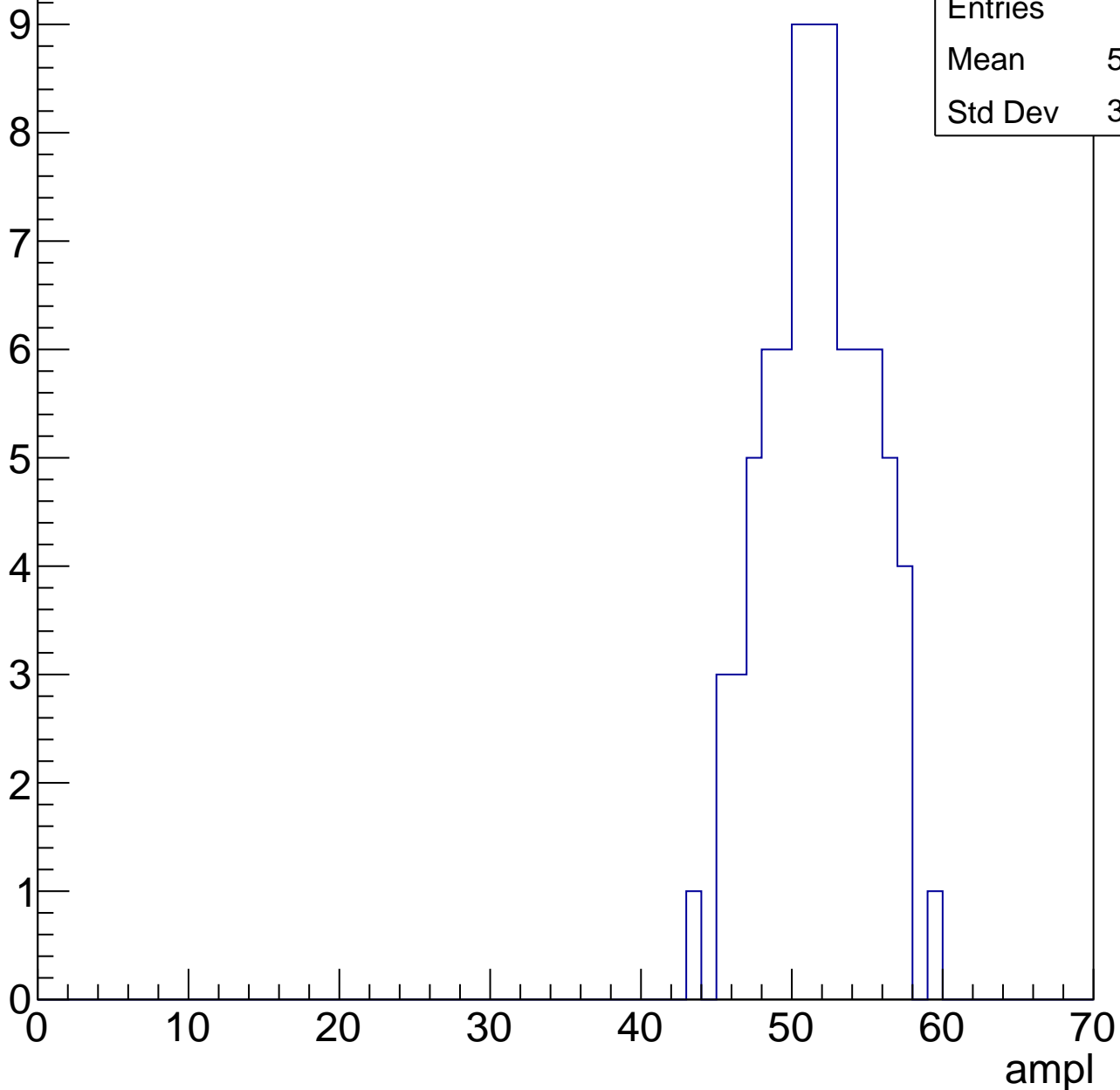


# B1L103S, U11-ch99, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	79
Mean	51.25
Std Dev	3.422



# B1L103S, U11-ch99, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	59
Mean	57.97
Std Dev	3.003

Entry

10

8

6

4

2

0

0

10

20

30

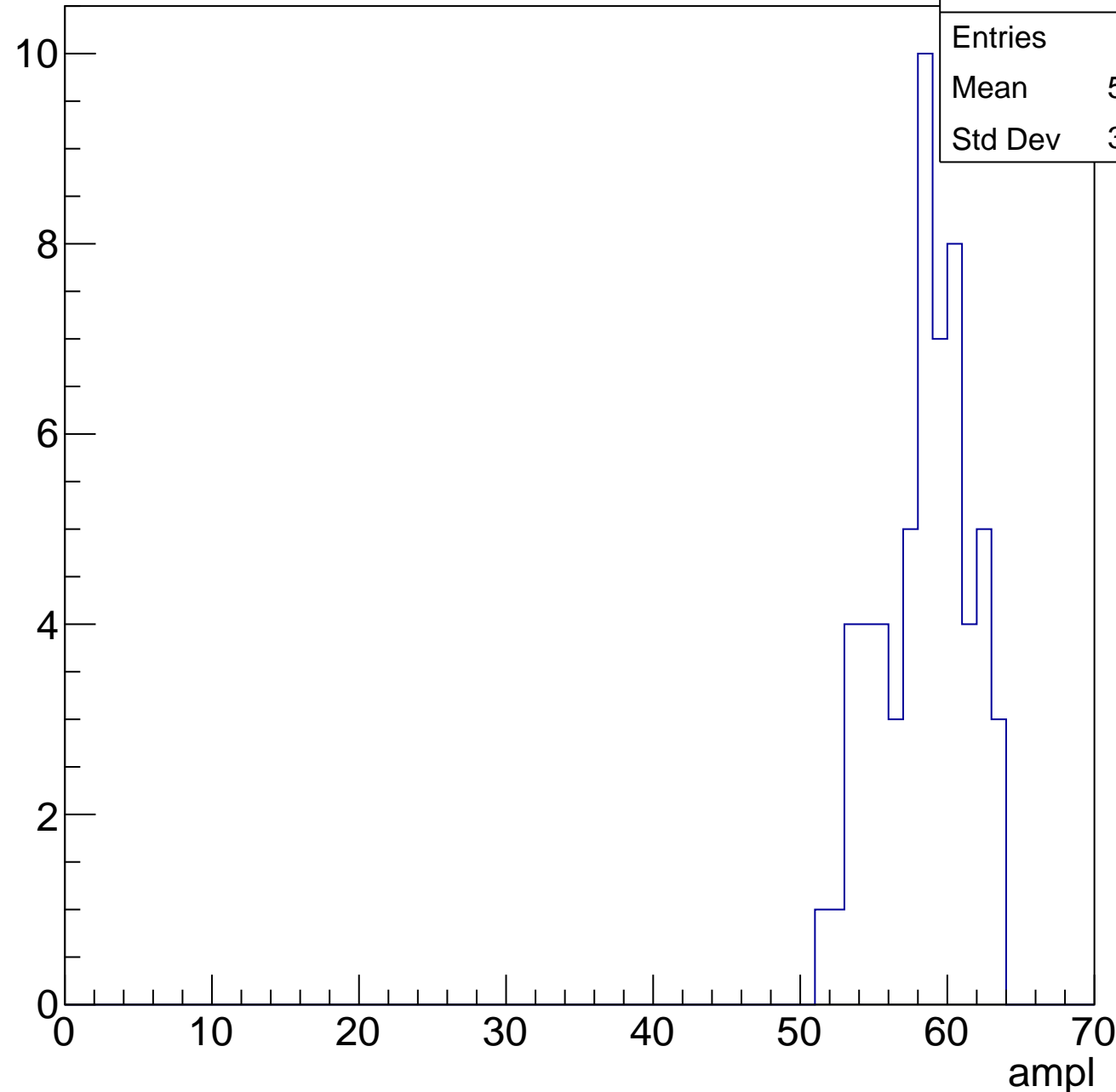
40

50

60

ampl

70

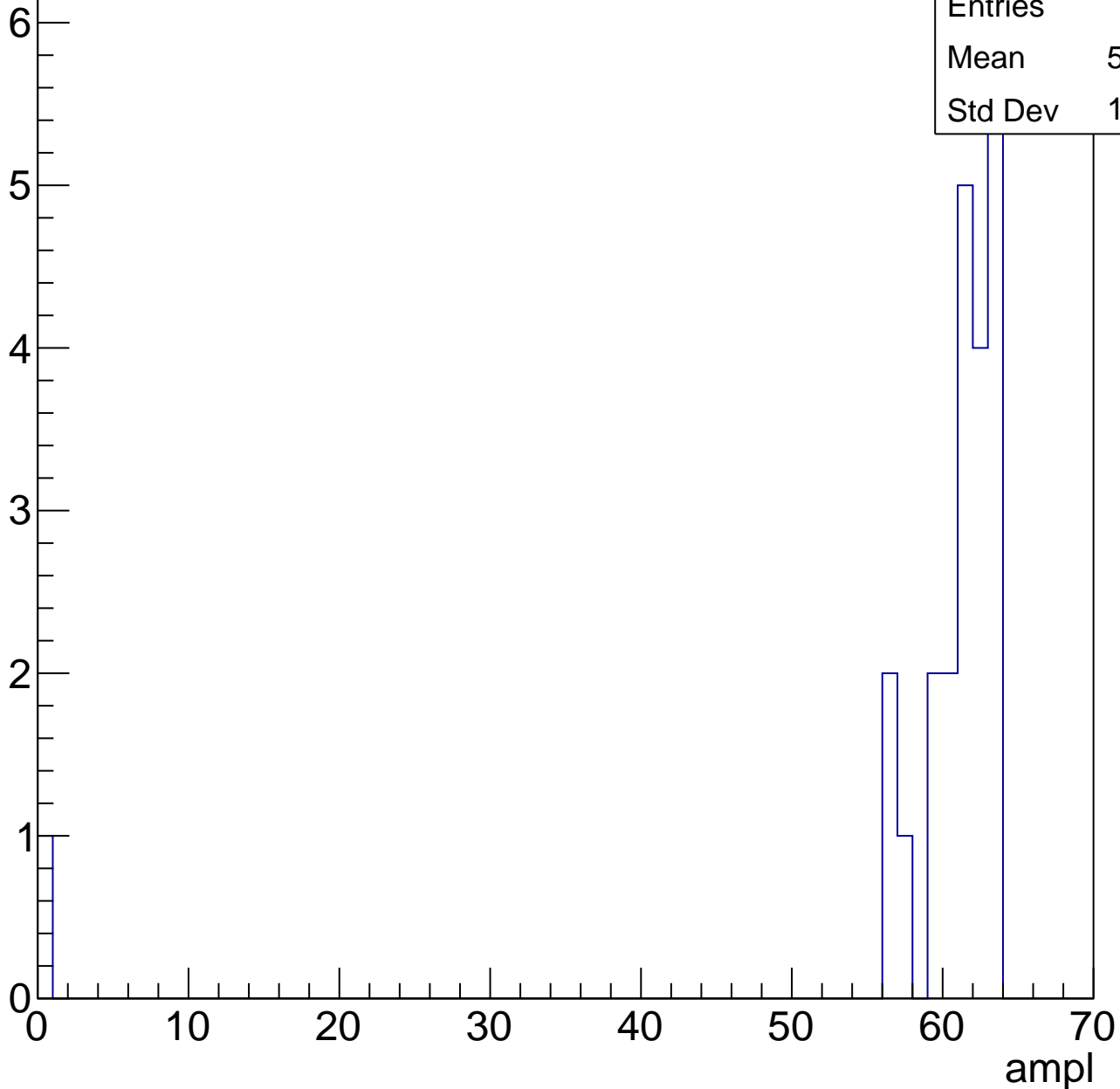


# B1L103S, U11-ch99, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	23
Mean	58.17
Std Dev	12.58



# B1L103S, U11-ch99, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U11-ch99, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U11-ch100, adc0

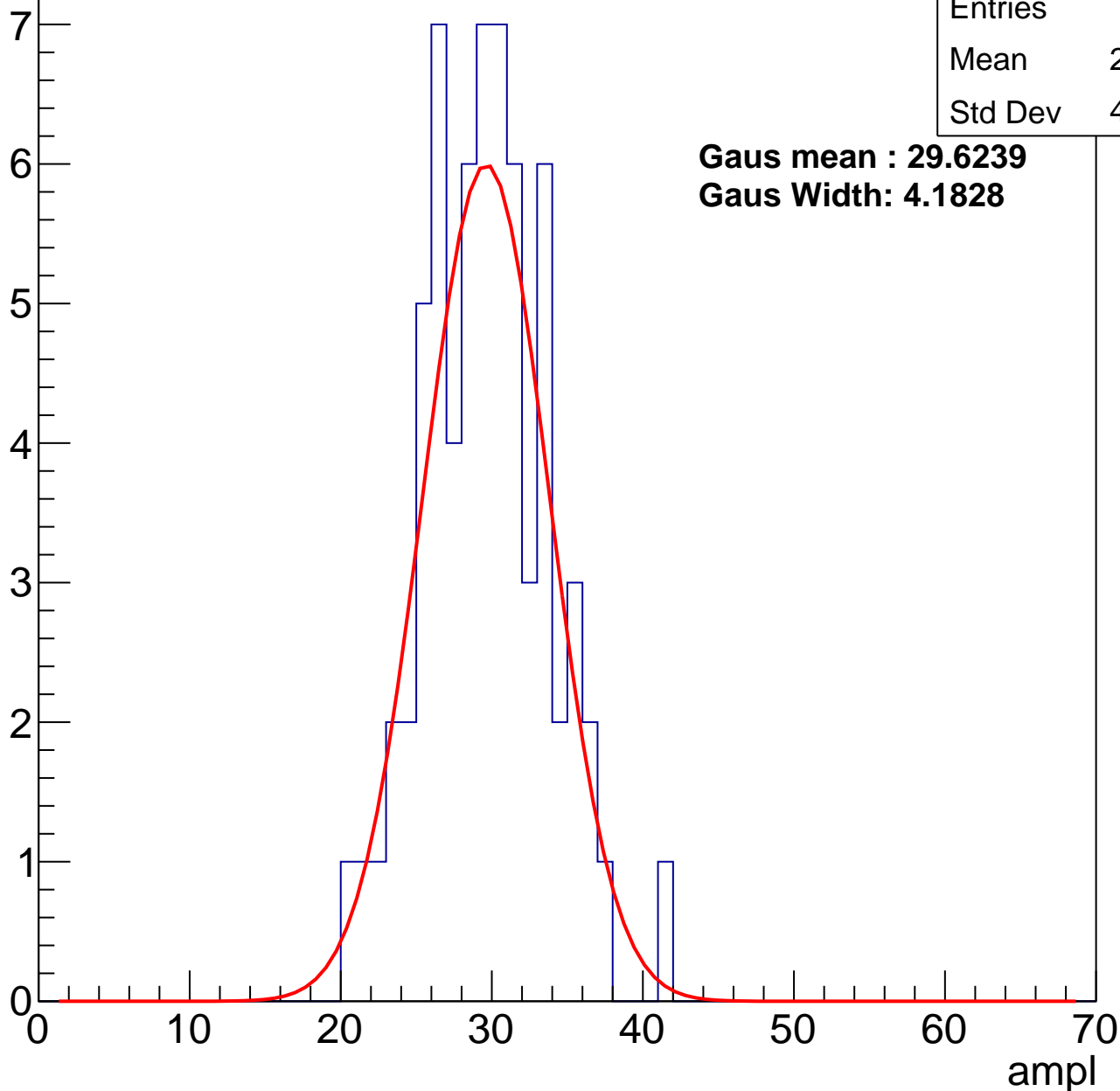
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	29.19
Std Dev	4.045

**Gaus mean : 29.6239**

**Gaus Width: 4.1828**



# B1L103S, U11-ch100, adc1

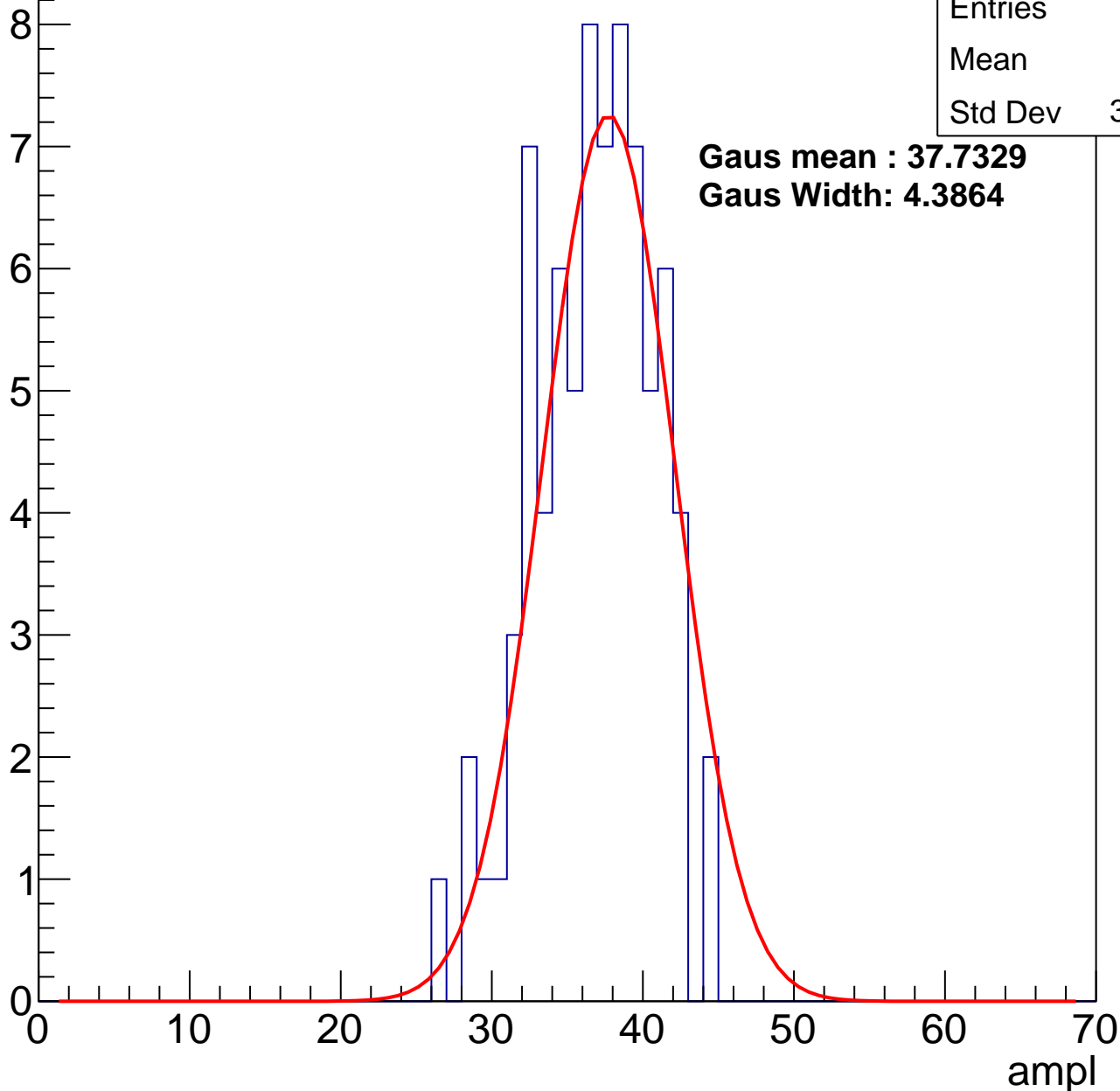
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	77
Mean	36.3
Std Dev	3.885

**Gaus mean : 37.7329**

**Gaus Width: 4.3864**



# B1L103S, U11-ch100, adc2

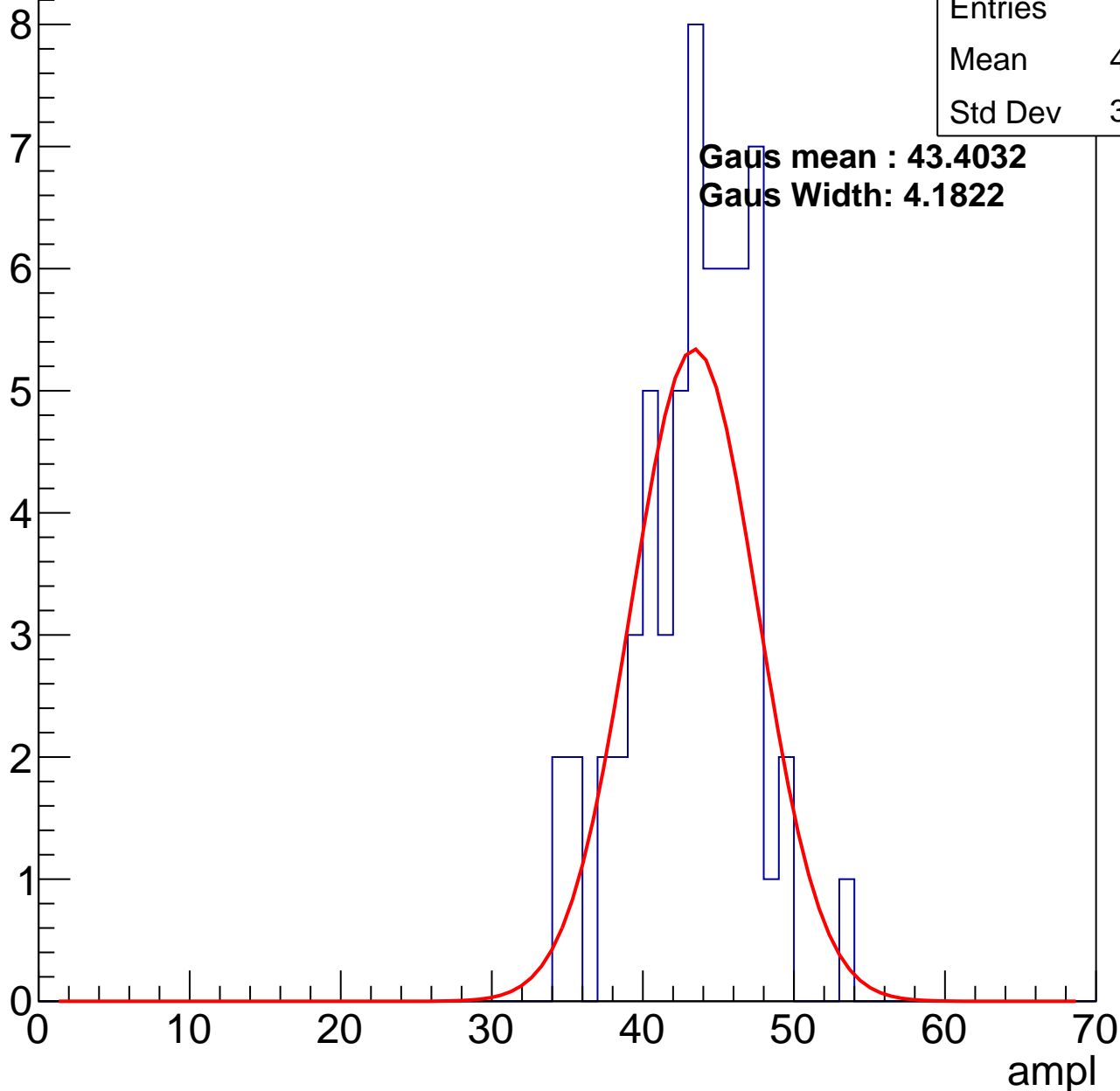
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	61
Mean	42.95
Std Dev	3.873

**Gaus mean : 43.4032**

**Gaus Width: 4.1822**

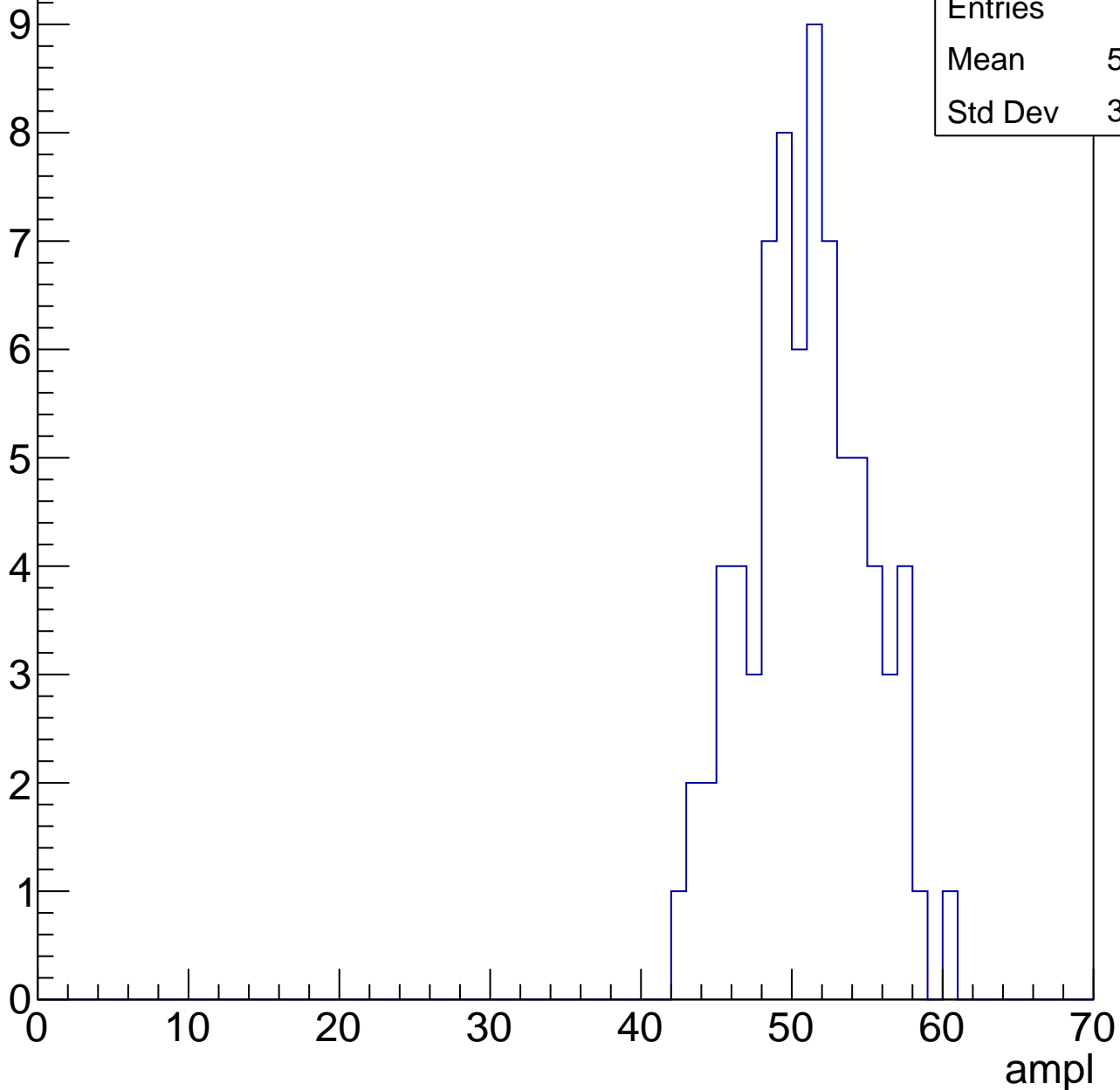


# B1L103S, U11-ch100, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	76
Mean	50.54
Std Dev	3.922

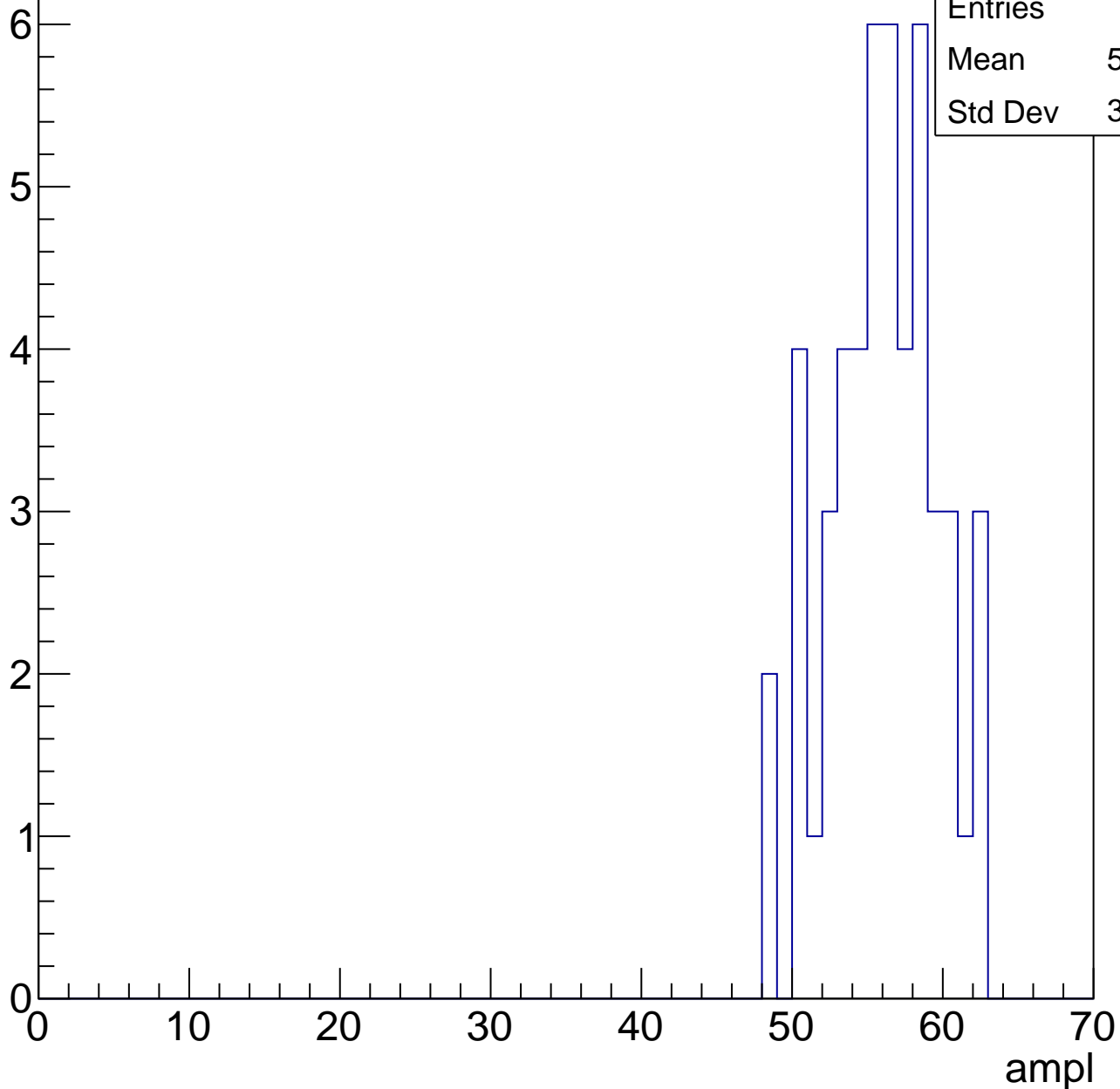


# B1L103S, U11-ch100, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	50
Mean	55.54
Std Dev	3.545

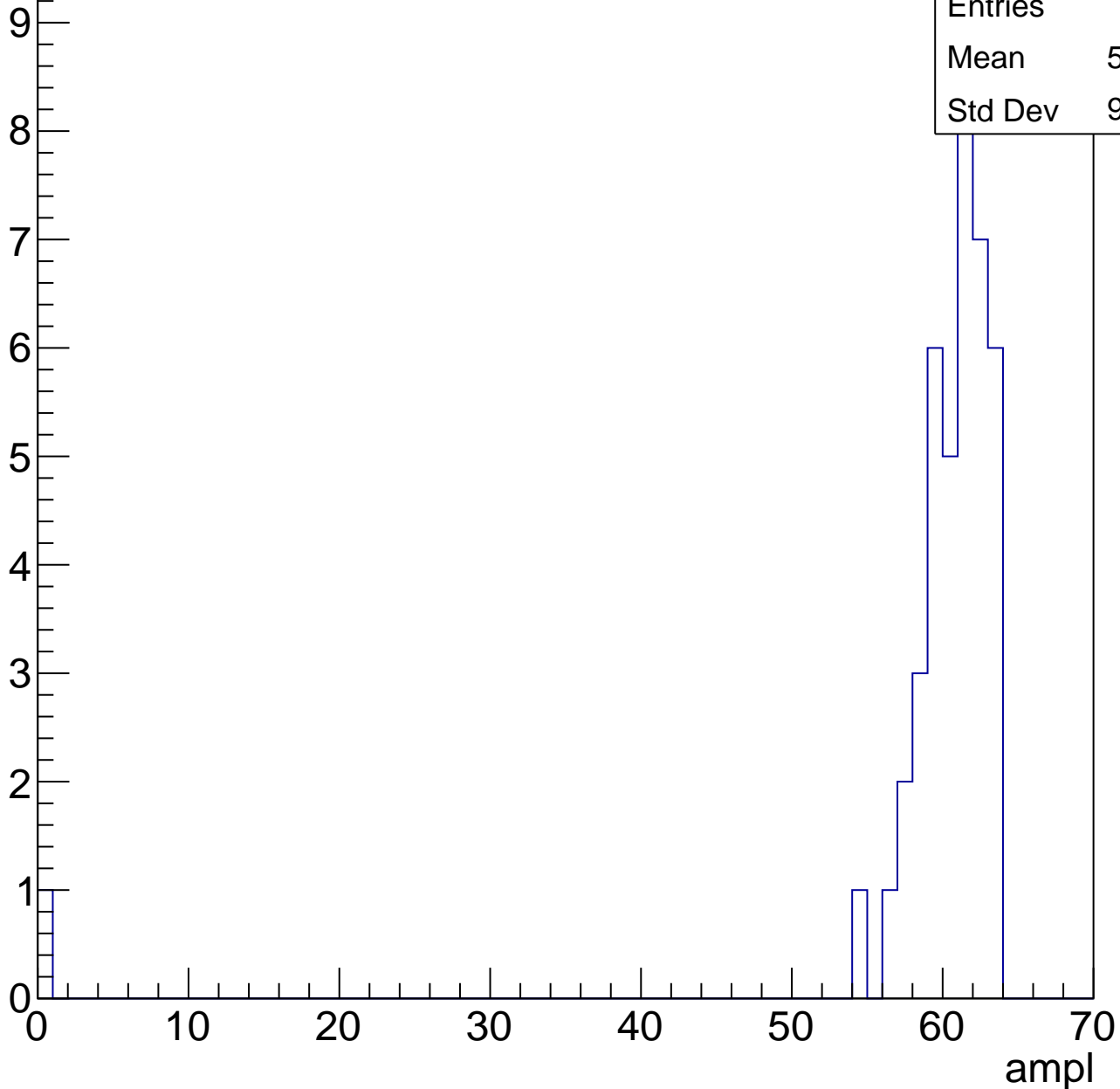


# B1L103S, U11-ch100, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

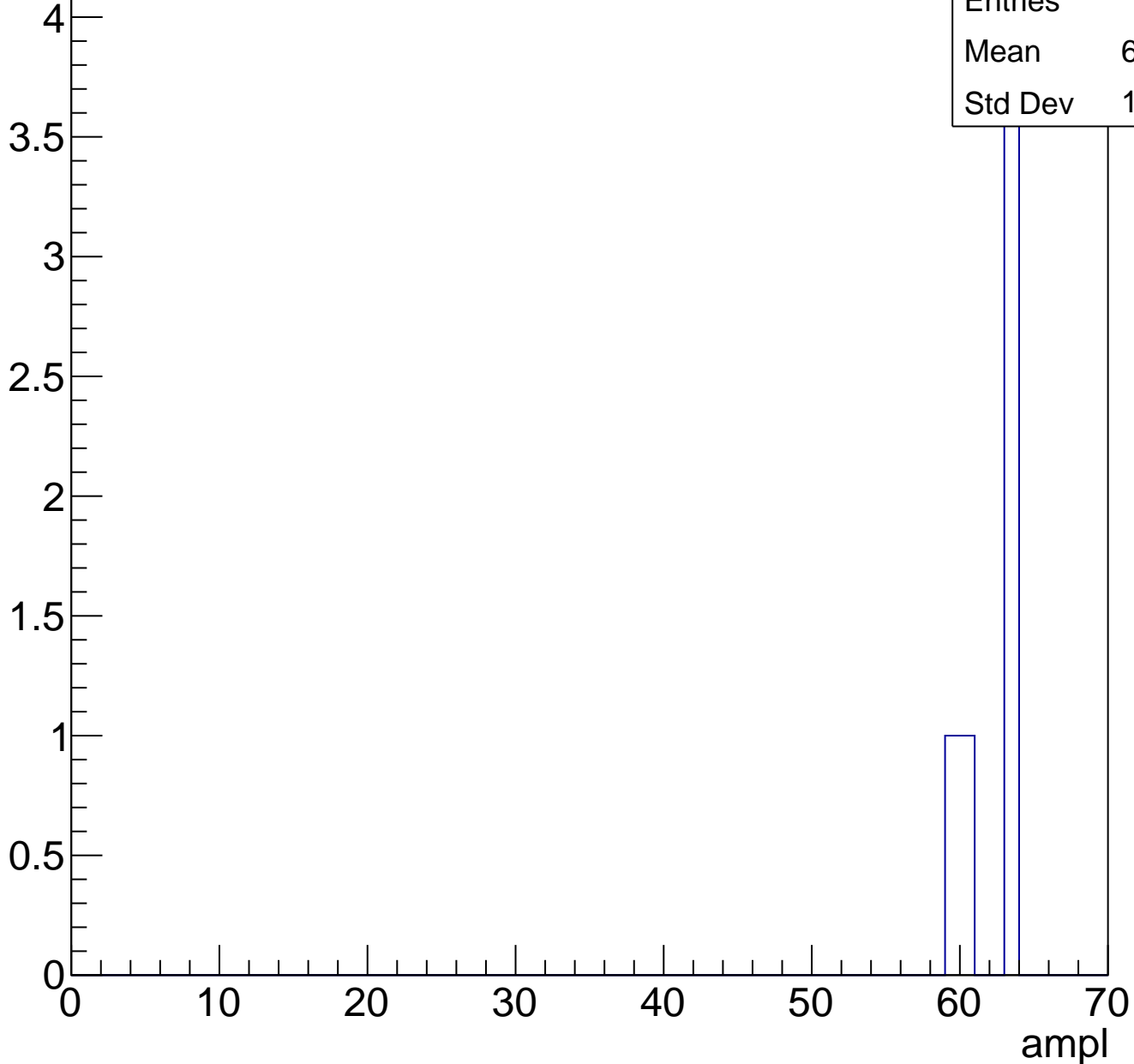
Entries	41
Mean	58.85
Std Dev	9.532



# B1L103S, U11-ch100, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U11-ch100, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U11-ch101, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	93
Mean	31.49
Std Dev	4.876

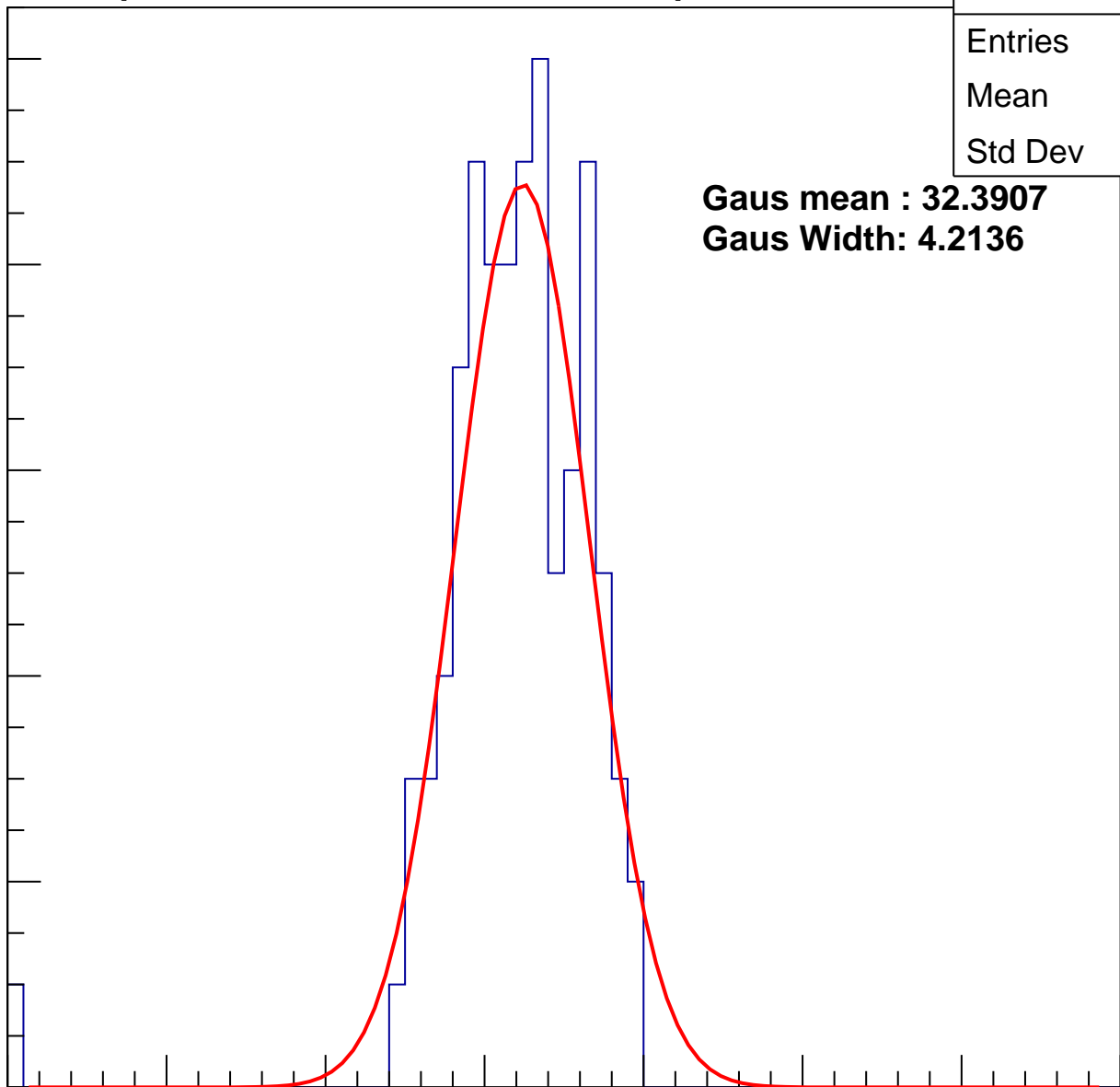
**Gaus mean : 32.3907**  
**Gaus Width: 4.2136**

Entry

10  
8  
6  
4  
2  
0

ampl

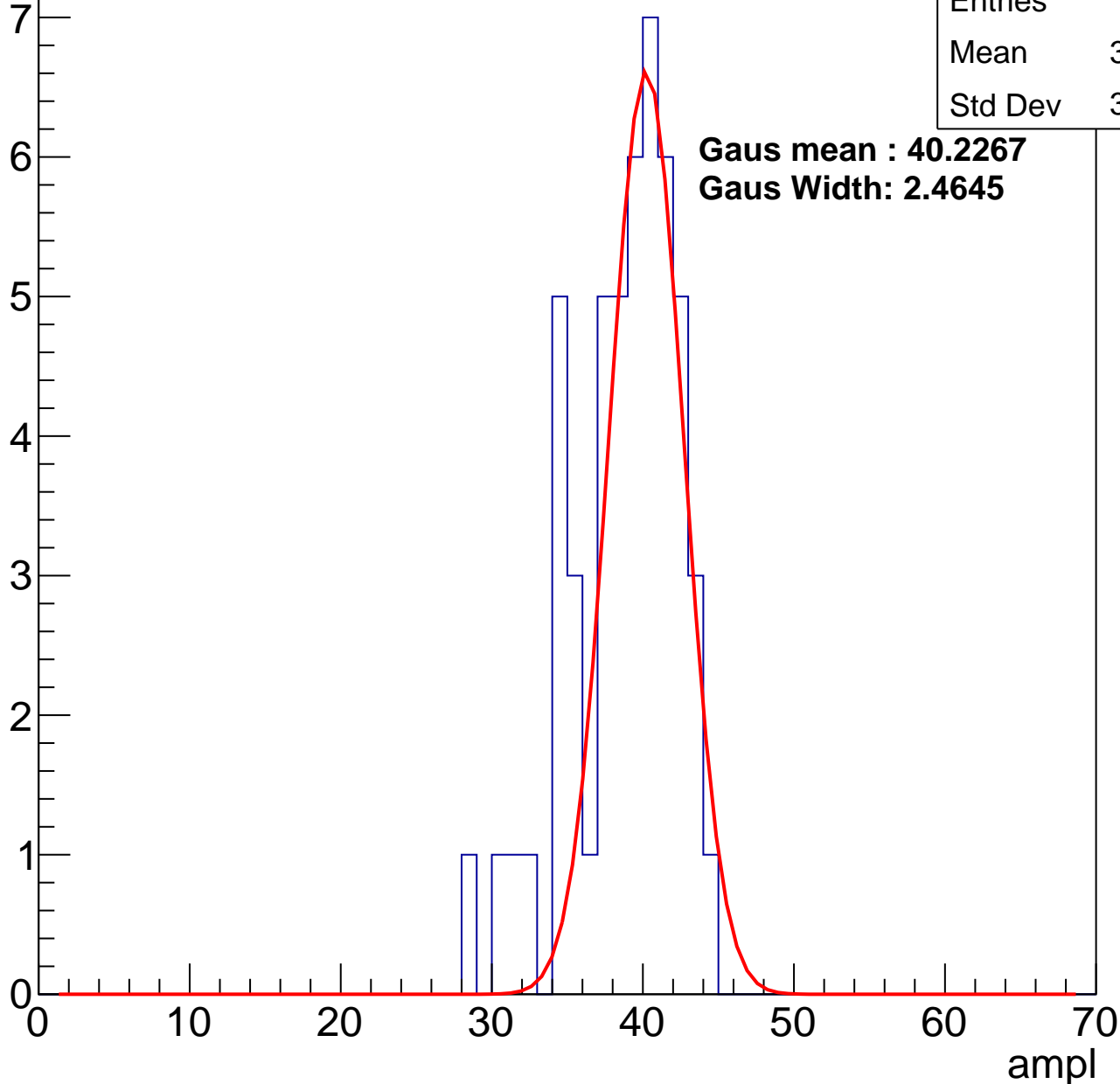
0 10 20 30 40 50 60 70



# B1L103S, U11-ch101, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U11-ch101, adc2

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	71
Mean	44.96
Std Dev	3.582

**Gaus mean : 45.4724**

**Gaus Width: 3.6524**

10

8

6

4

2

0

ampl

0

10

20

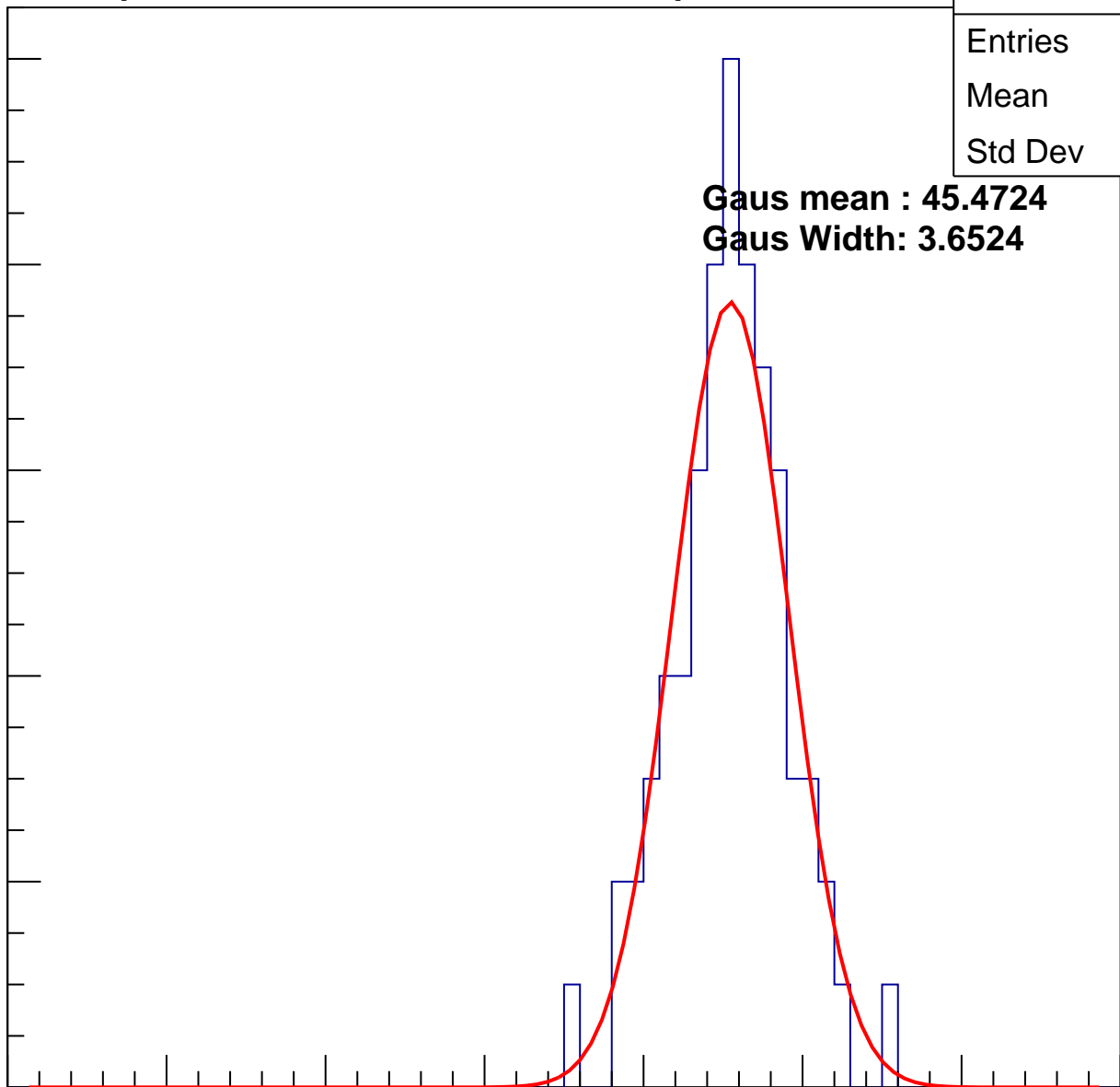
30

40

50

60

70

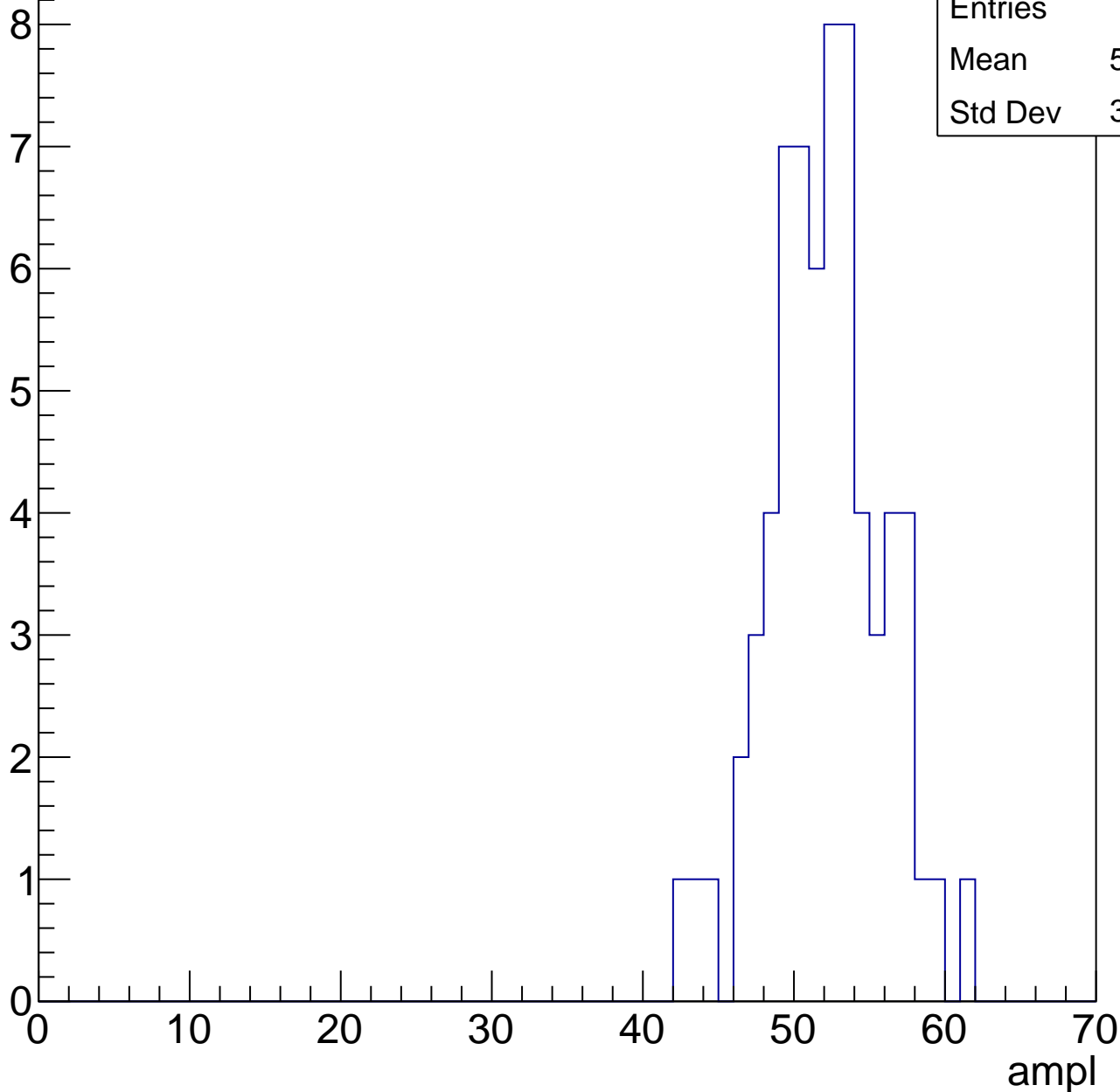


# B1L103S, U11-ch101, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	51.58
Std Dev	3.738

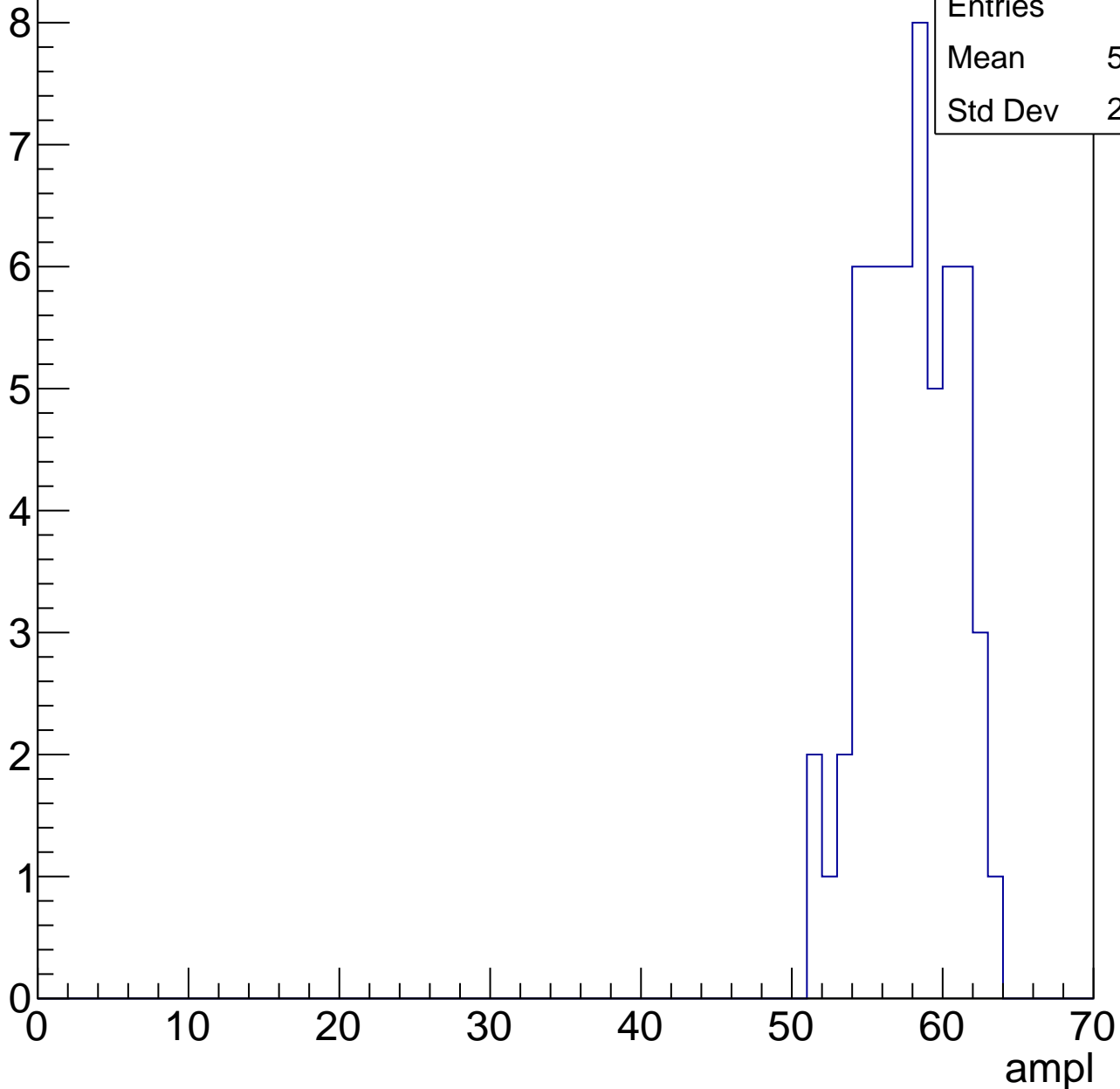


# B1L103S, U11-ch101, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	58
Mean	57.34
Std Dev	2.922

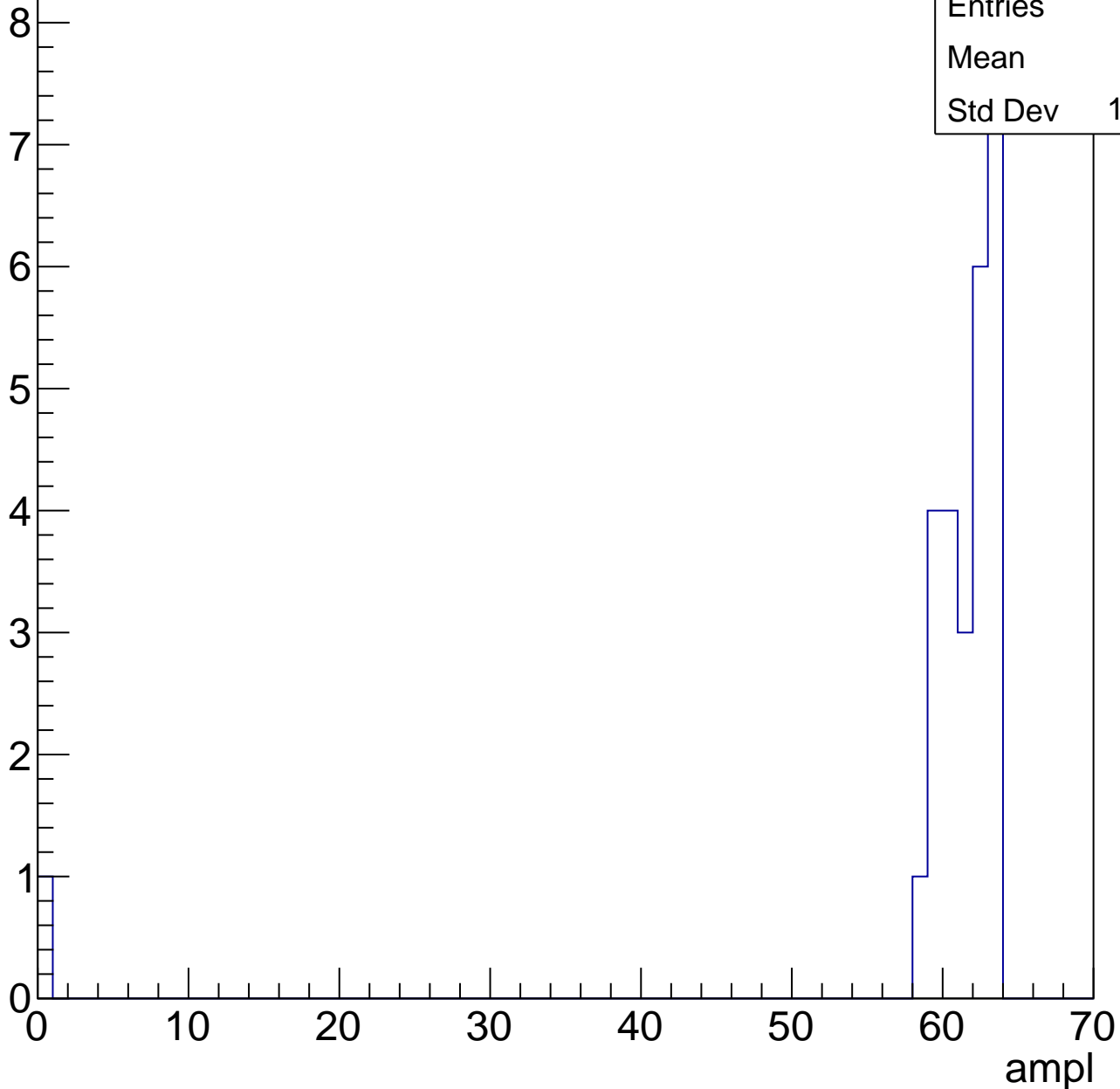


# B1L103S, U11-ch101, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	27
Mean	59
Std Dev	11.67



# B1L103S, U11-ch101, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U11-ch101, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U11-ch102, adc0

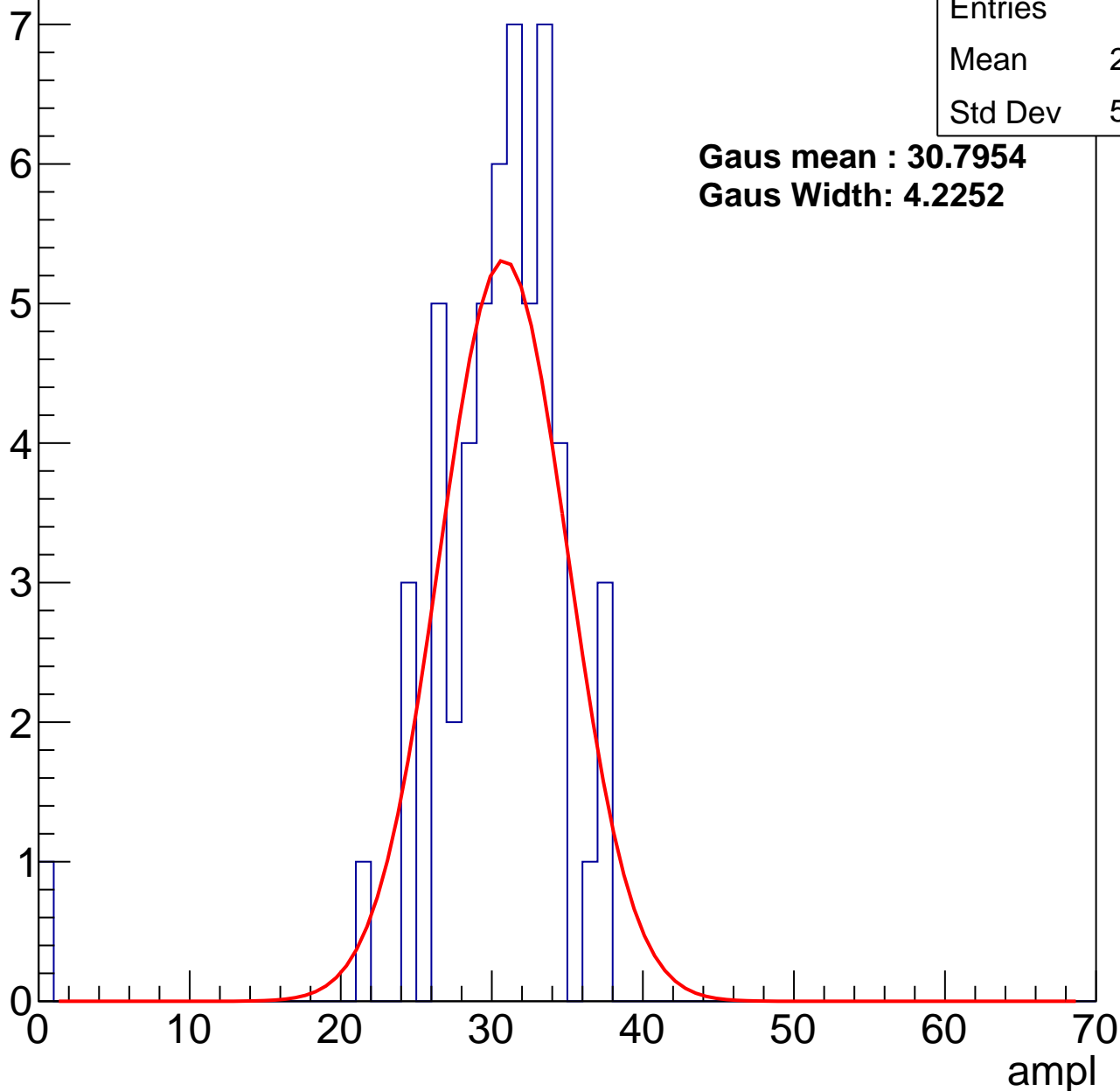
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	54
Mean	29.72
Std Dev	5.342

**Gaus mean : 30.7954**

**Gaus Width: 4.2252**



# B1L103S, U11-ch102, adc1

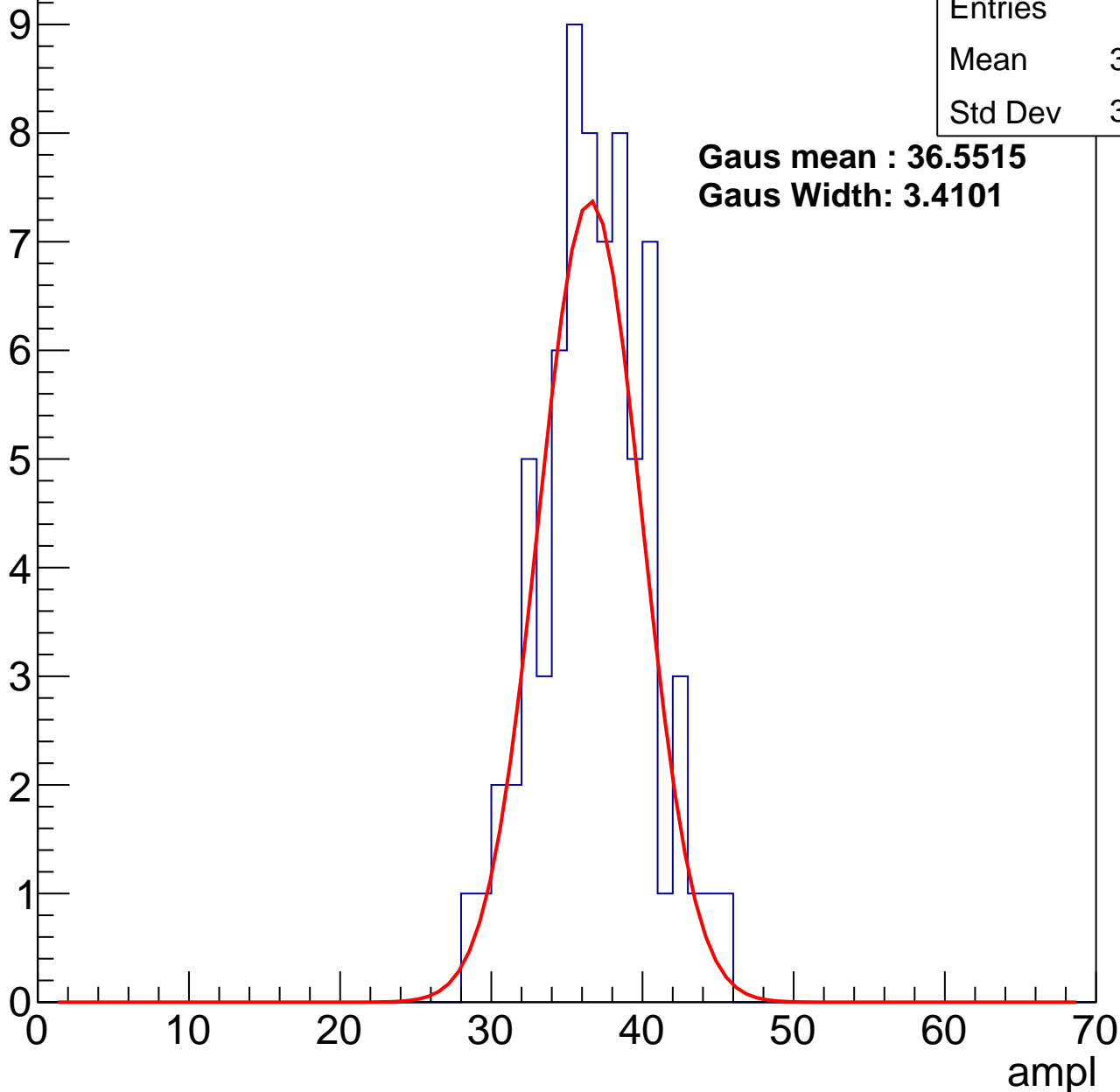
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	71
Mean	36.37
Std Dev	3.537

**Gaus mean : 36.5515**

**Gaus Width: 3.4101**



# B1L103S, U11-ch102, adc2

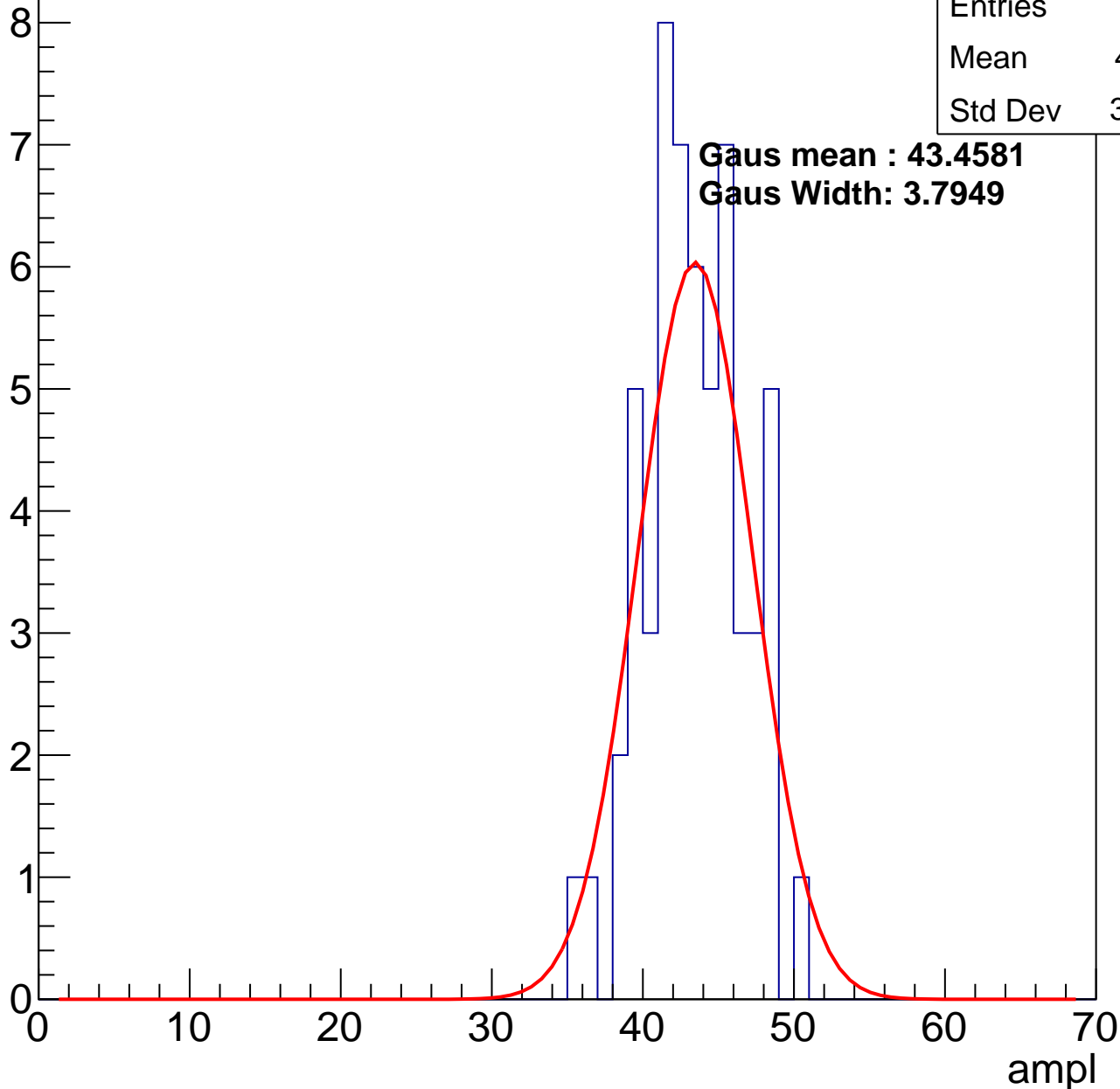
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	57
Mean	42.91
Std Dev	3.219

**Gaus mean : 43.4581**

**Gaus Width: 3.7949**

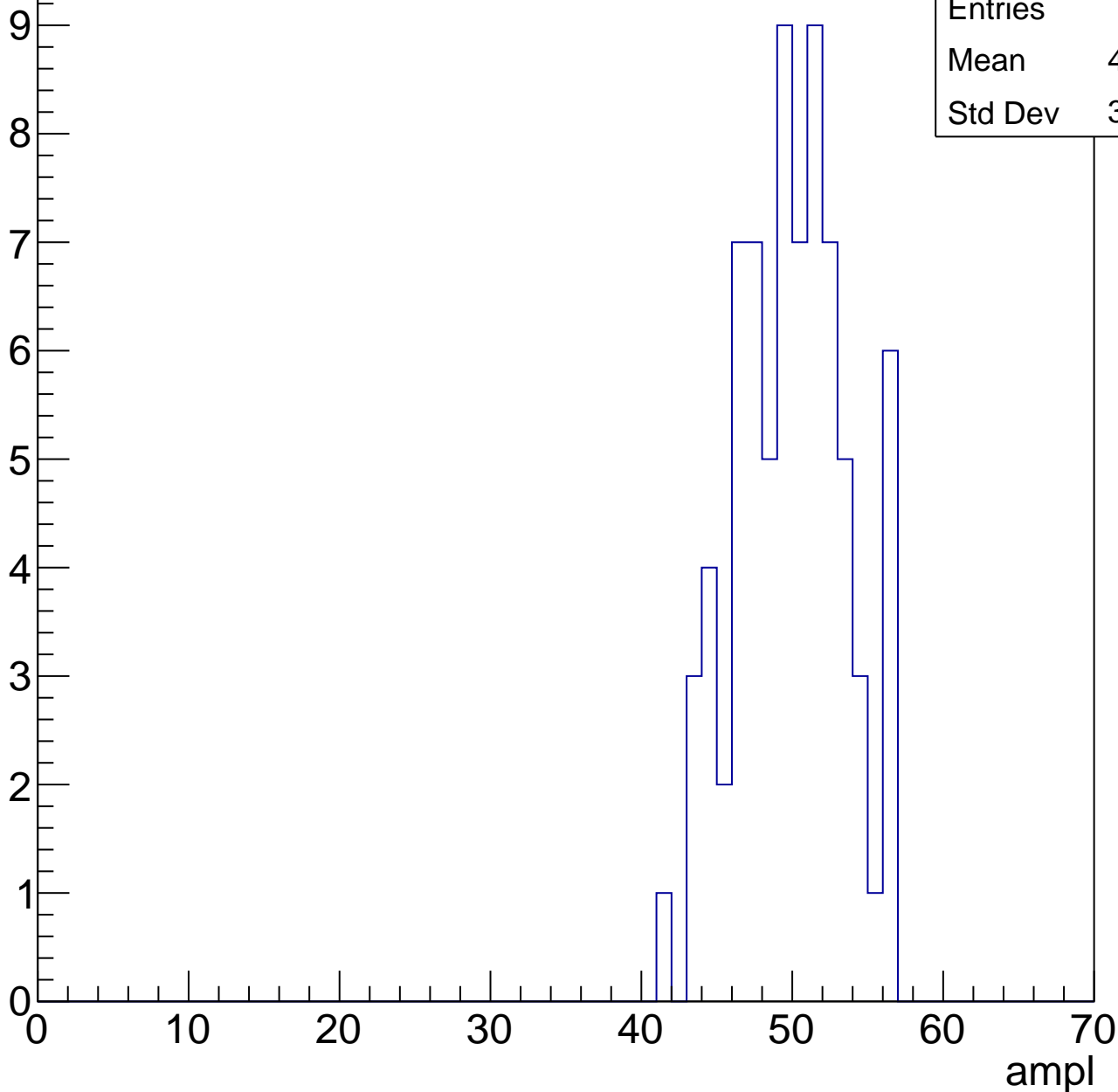


# B1L103S, U11-ch102, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	76
Mean	49.46
Std Dev	3.582

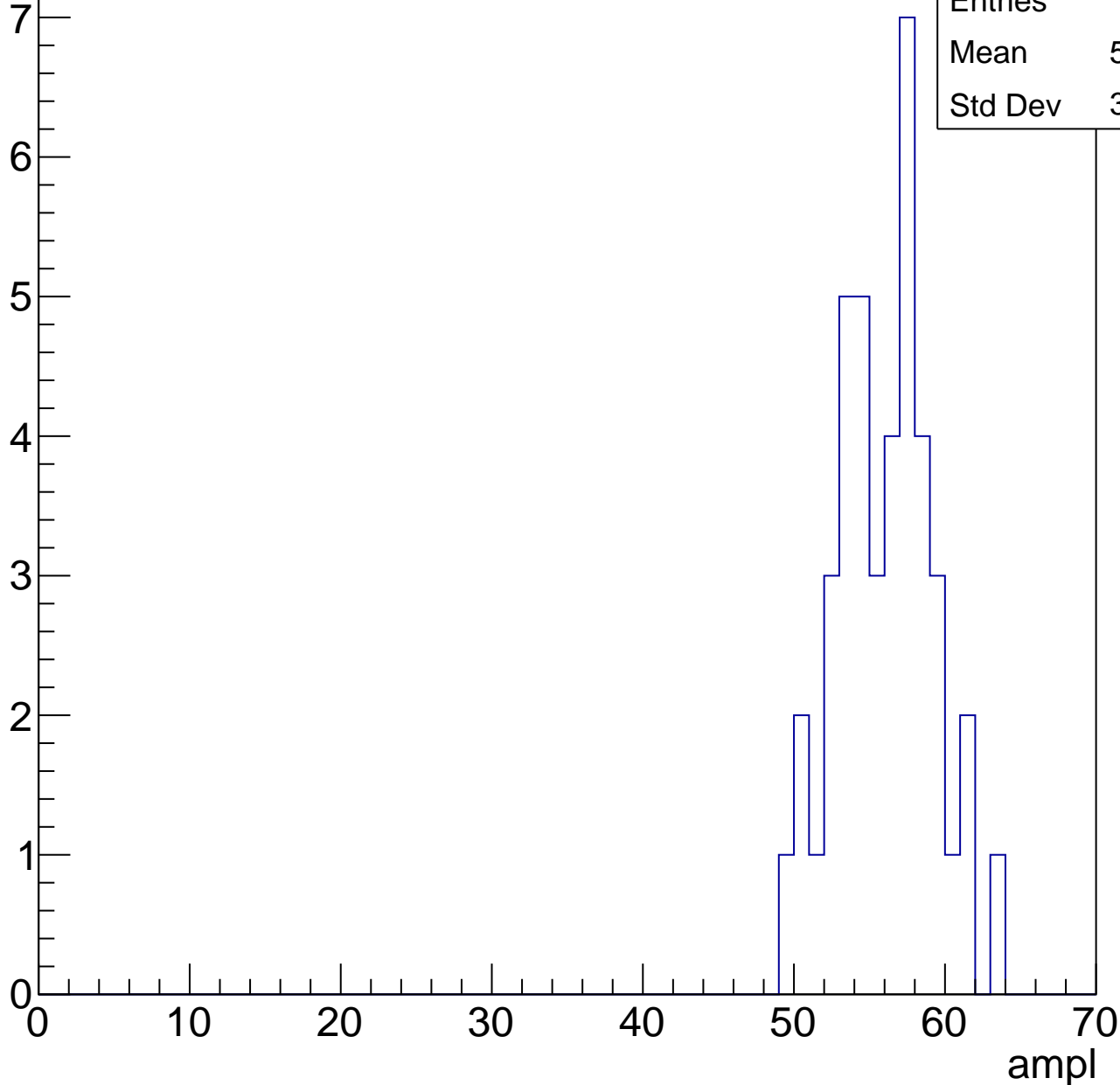


# B1L103S, U11-ch102, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

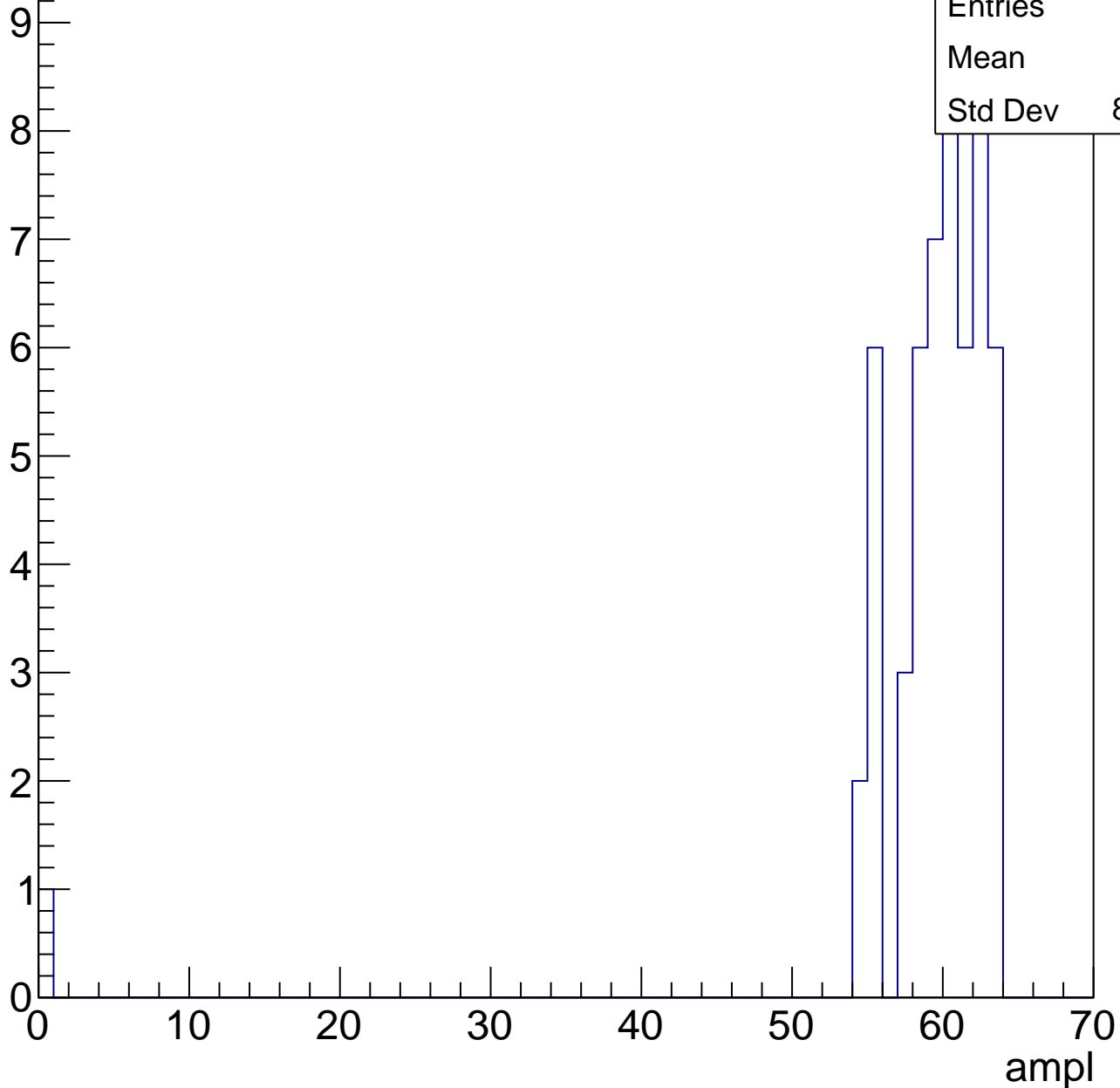
Entries	42
Mean	55.55
Std Dev	3.156



# B1L103S, U11-ch102, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

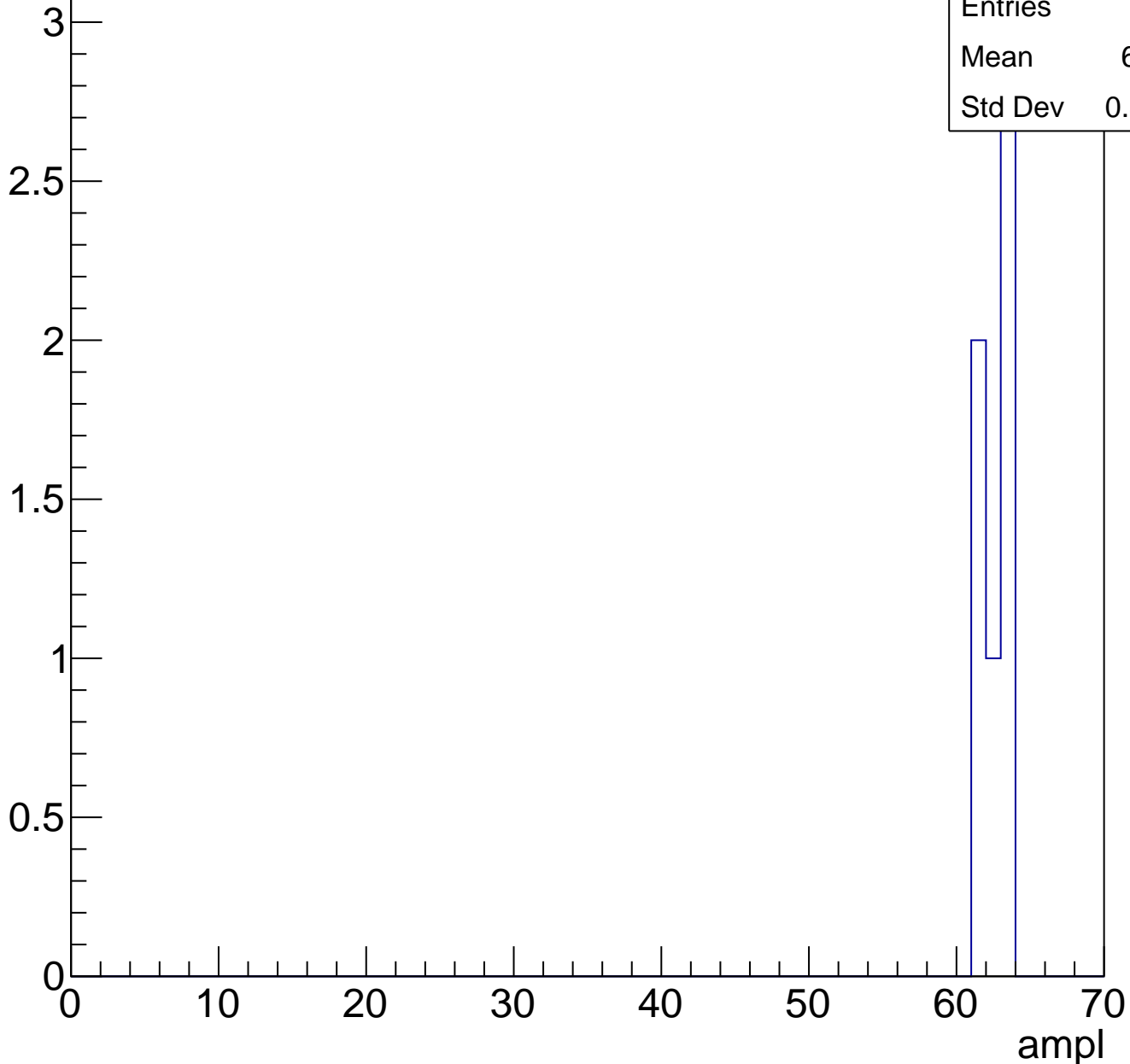
Entry



# B1L103S, U11-ch102, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U11-ch102, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U11-ch103, adc0

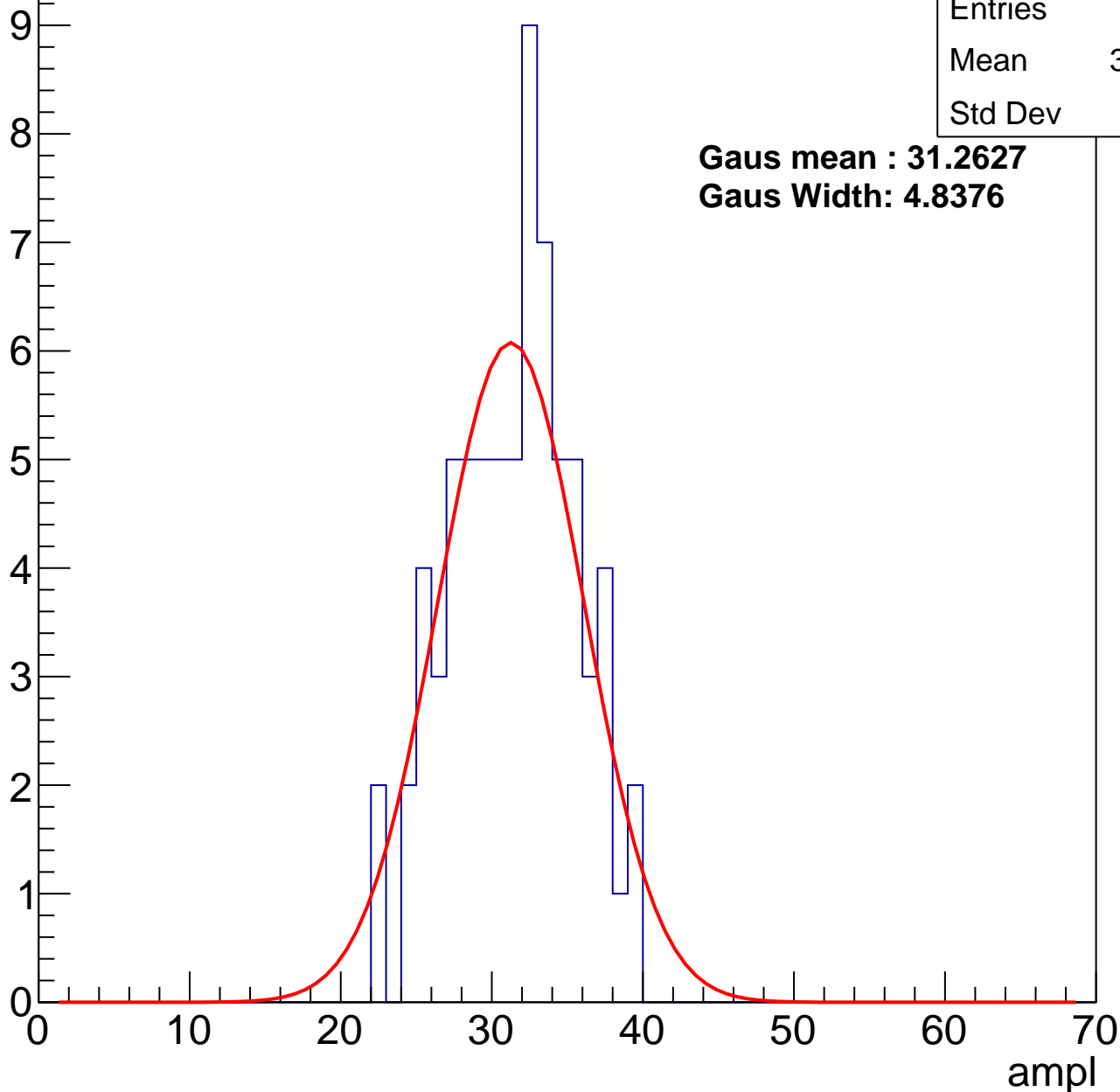
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	72
Mean	30.99
Std Dev	4.06

**Gaus mean : 31.2627**

**Gaus Width: 4.8376**



# B1L103S, U11-ch103, adc1

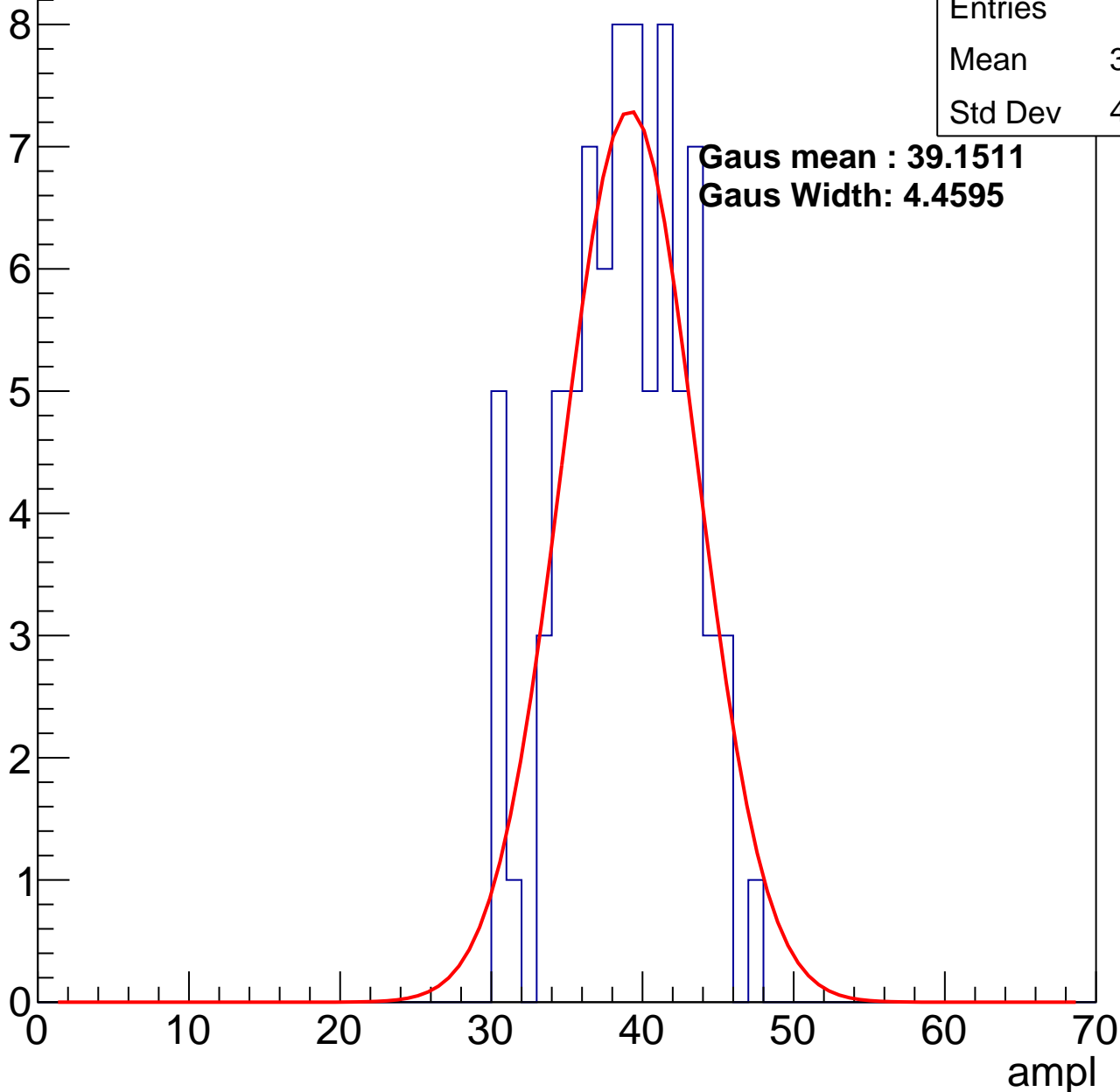
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	80
Mean	38.35
Std Dev	4.007

**Gaus mean : 39.1511**

**Gaus Width: 4.4595**



# B1L103S, U11-ch103, adc2

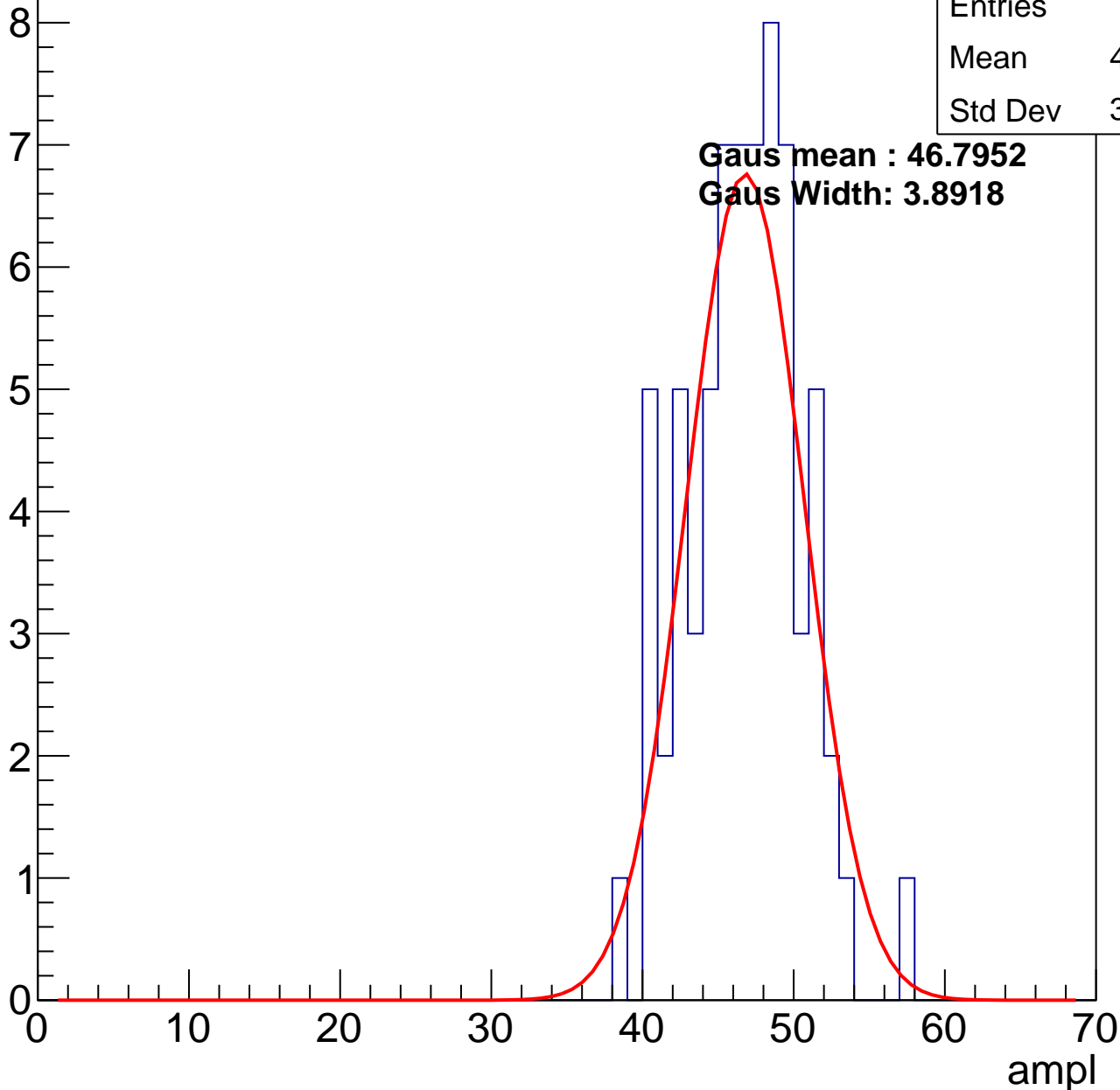
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	69
Mean	46.25
Std Dev	3.693

Gaus mean : 46.7952

Gaus Width: 3.8918

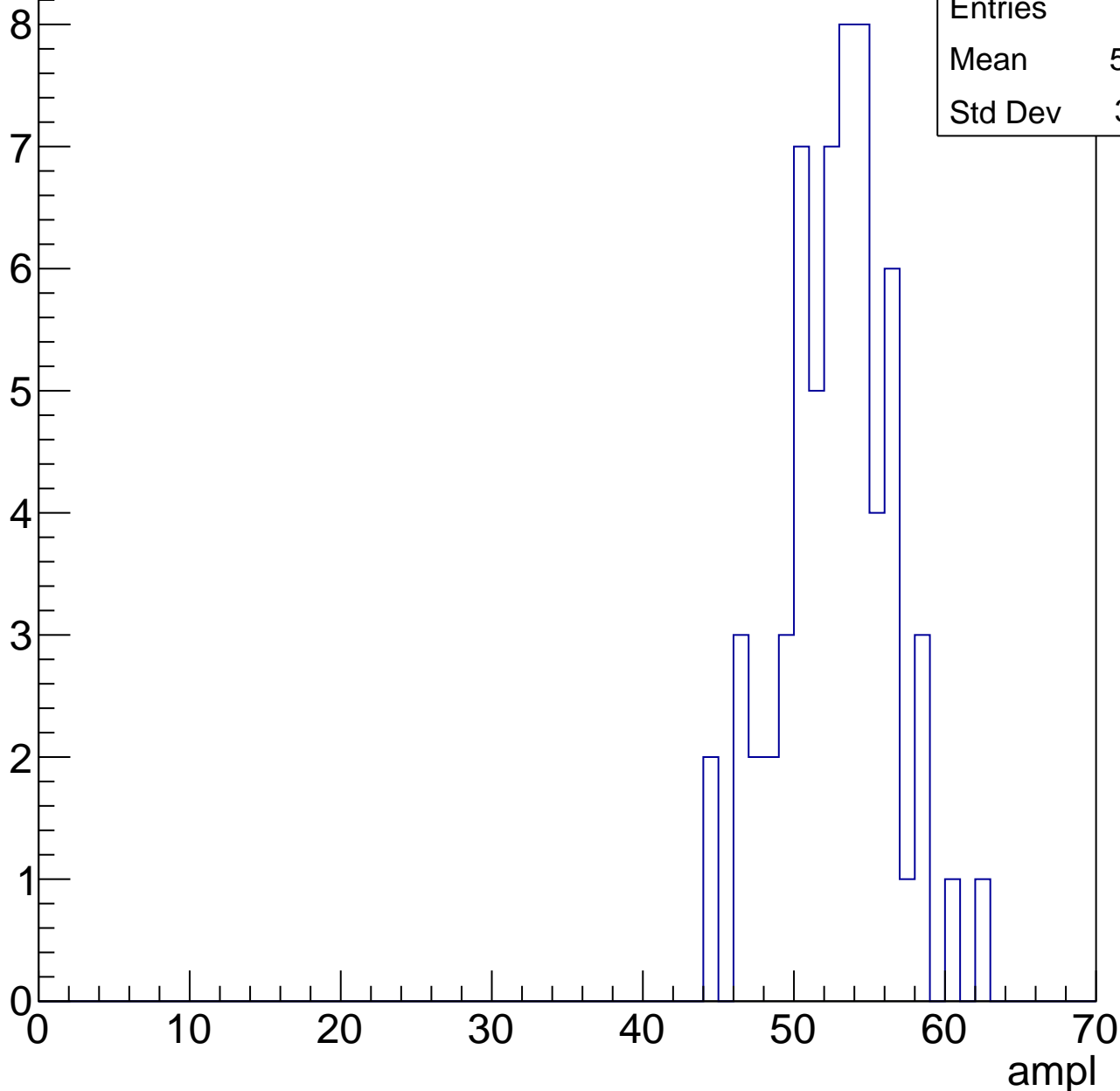


# B1L103S, U11-ch103, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	52.33
Std Dev	3.651

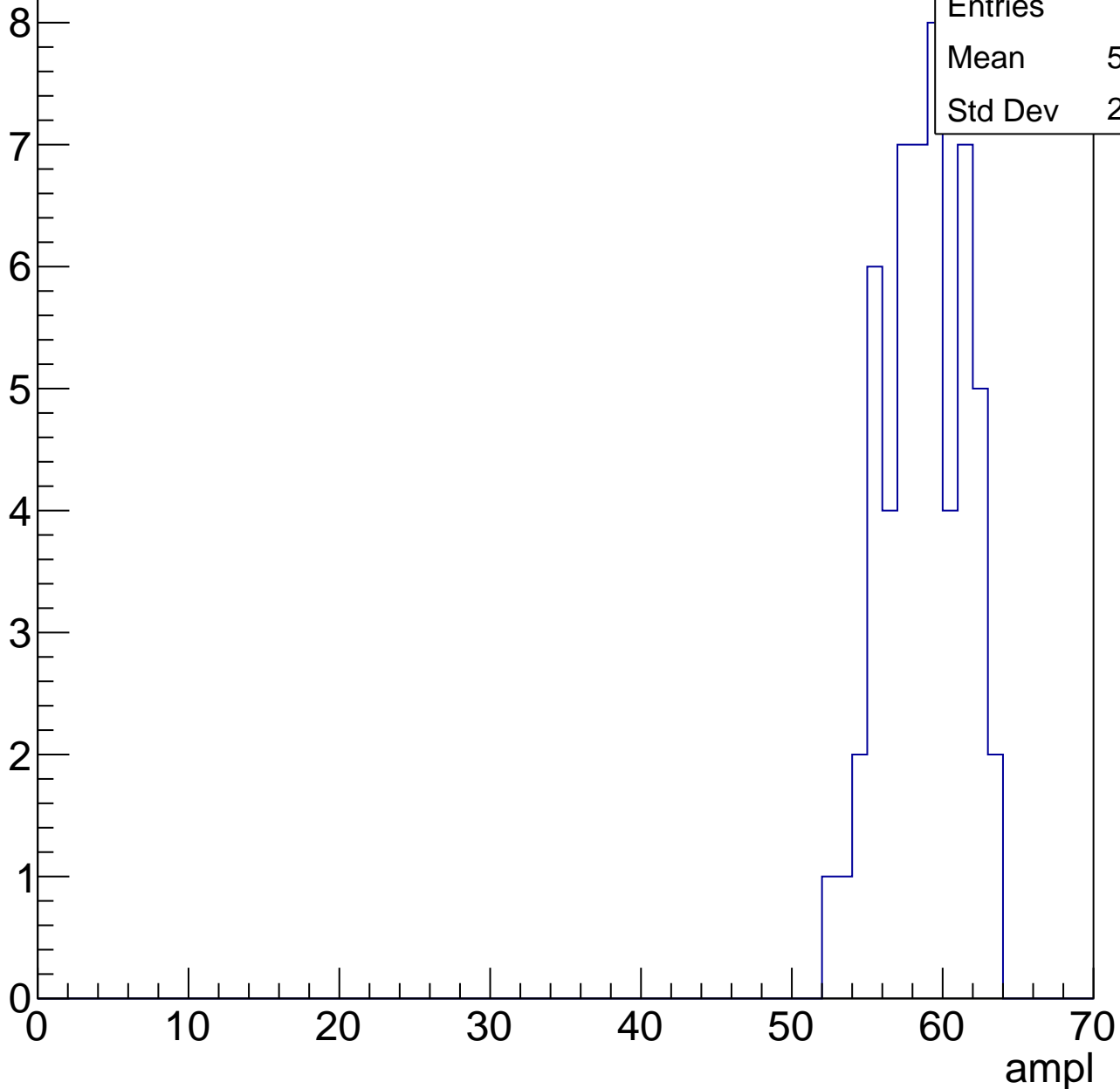


# B1L103S, U11-ch103, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	54
Mean	58.28
Std Dev	2.663

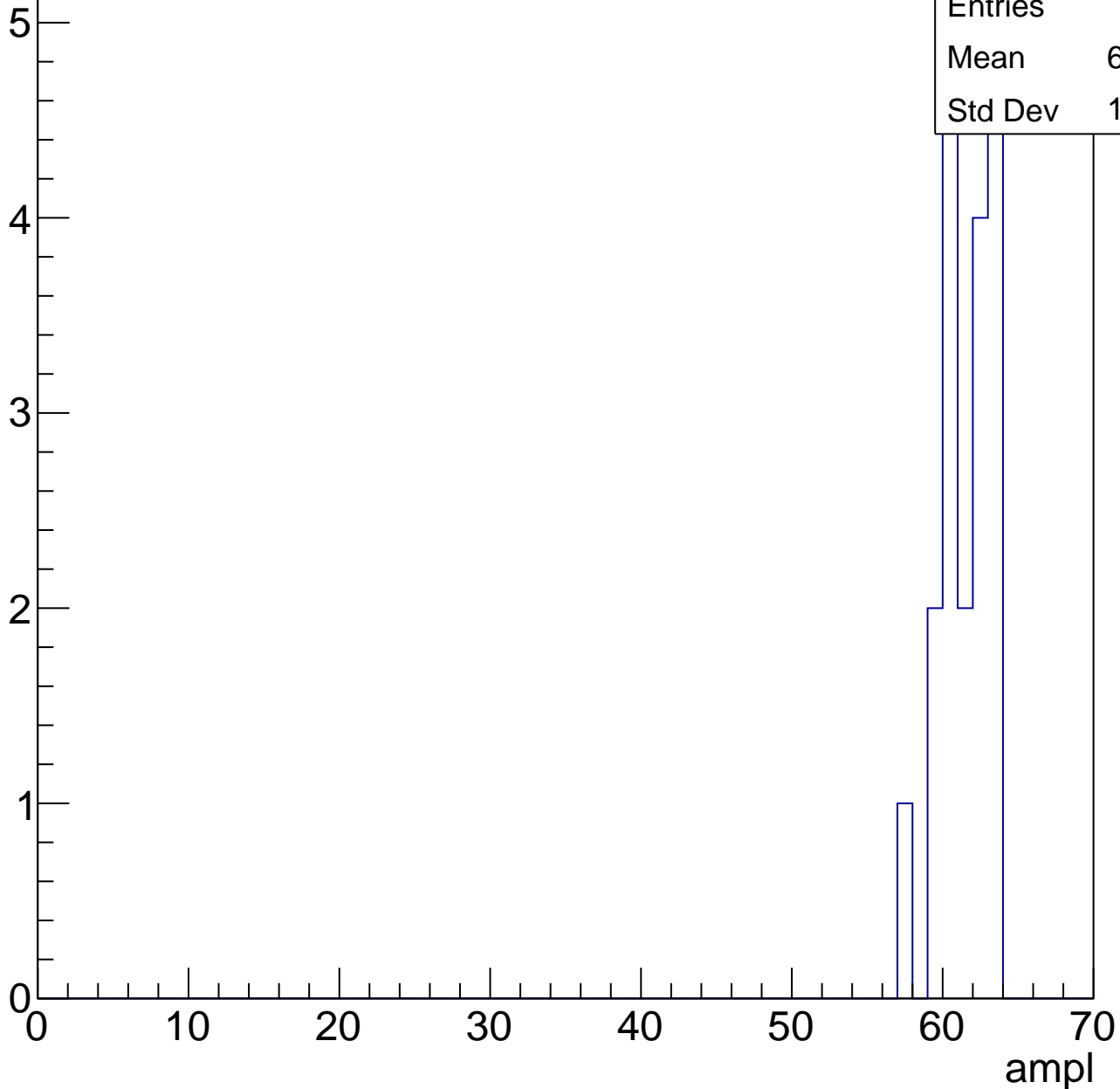


# B1L103S, U11-ch103, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

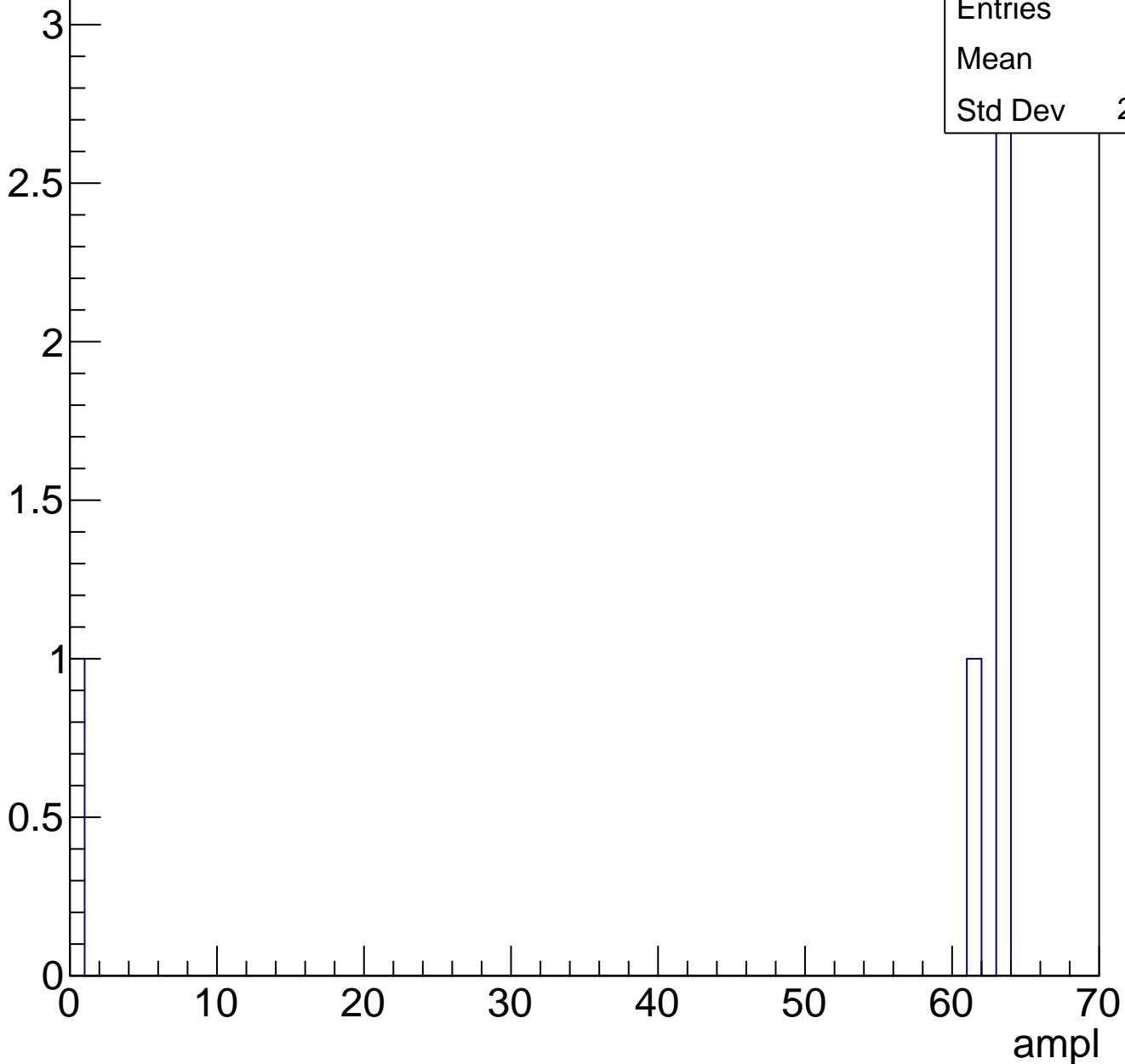
Entries	19
Mean	61.05
Std Dev	1.669



# B1L103S, U11-ch103, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U11-ch103, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L103S, U11-ch104, adc0

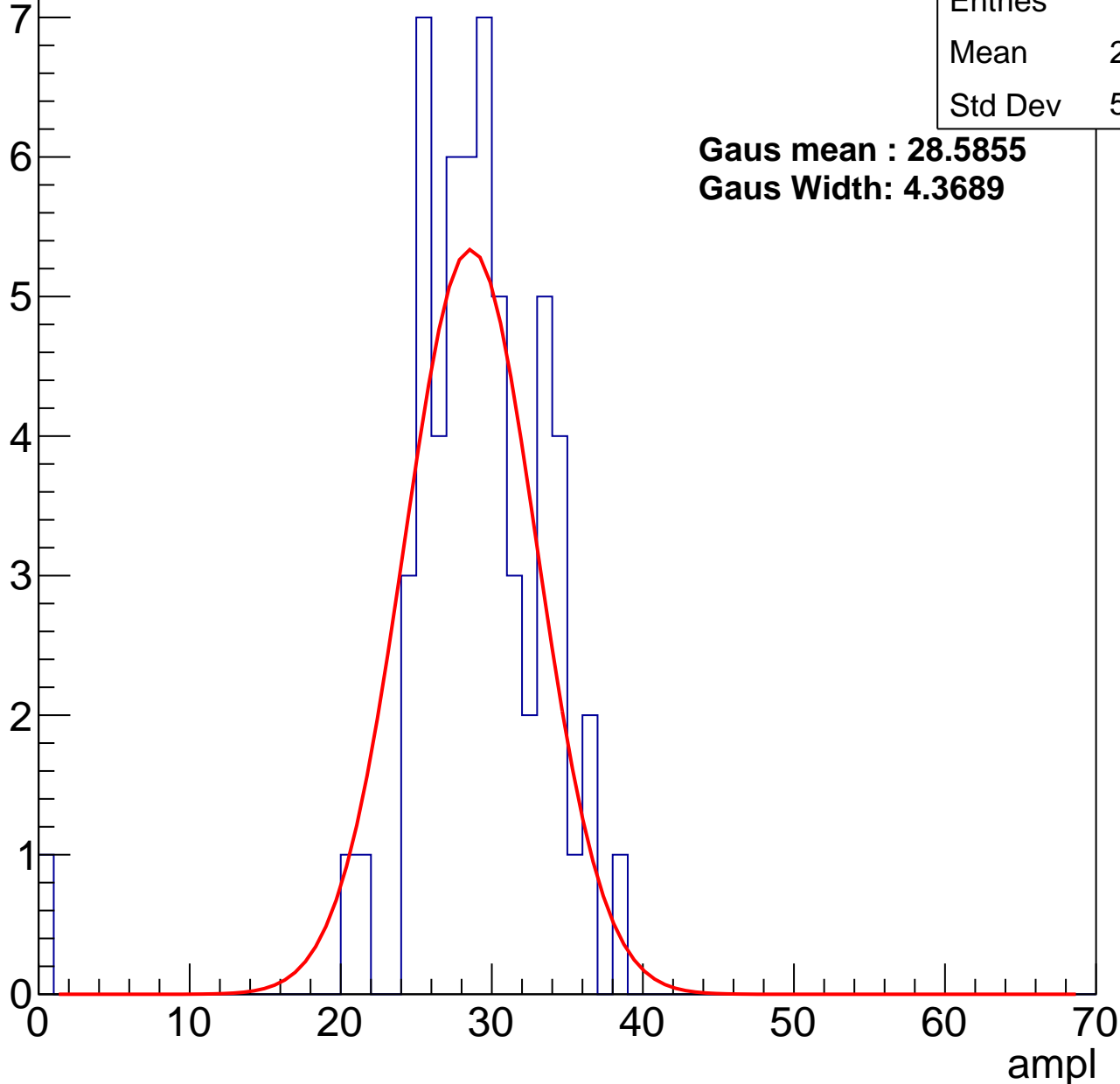
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	59
Mean	28.44
Std Dev	5.289

**Gaus mean : 28.5855**

**Gaus Width: 4.3689**



# B1L103S, U11-ch104, adc1

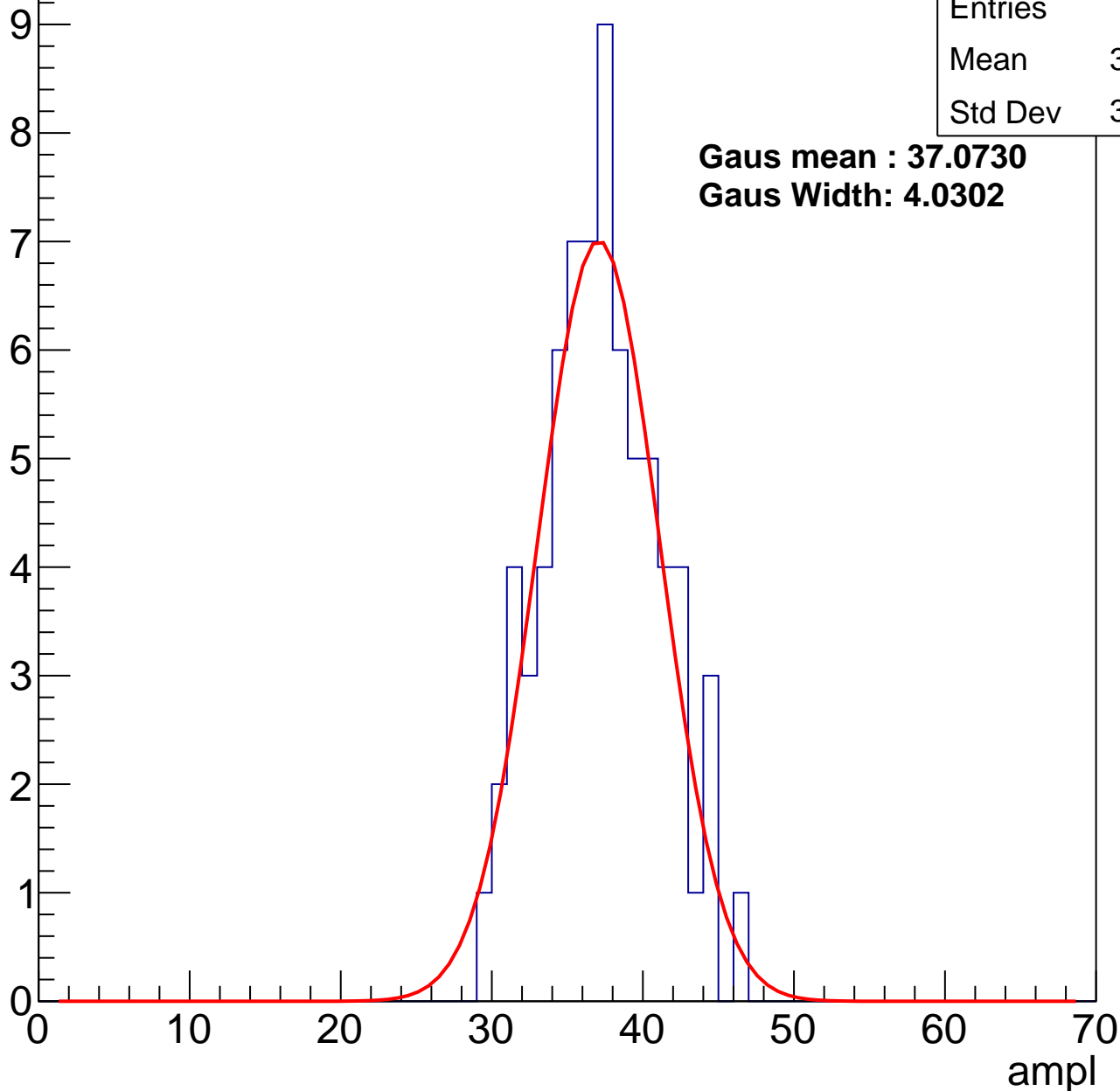
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	72
Mean	36.82
Std Dev	3.783

**Gaus mean : 37.0730**

**Gaus Width: 4.0302**

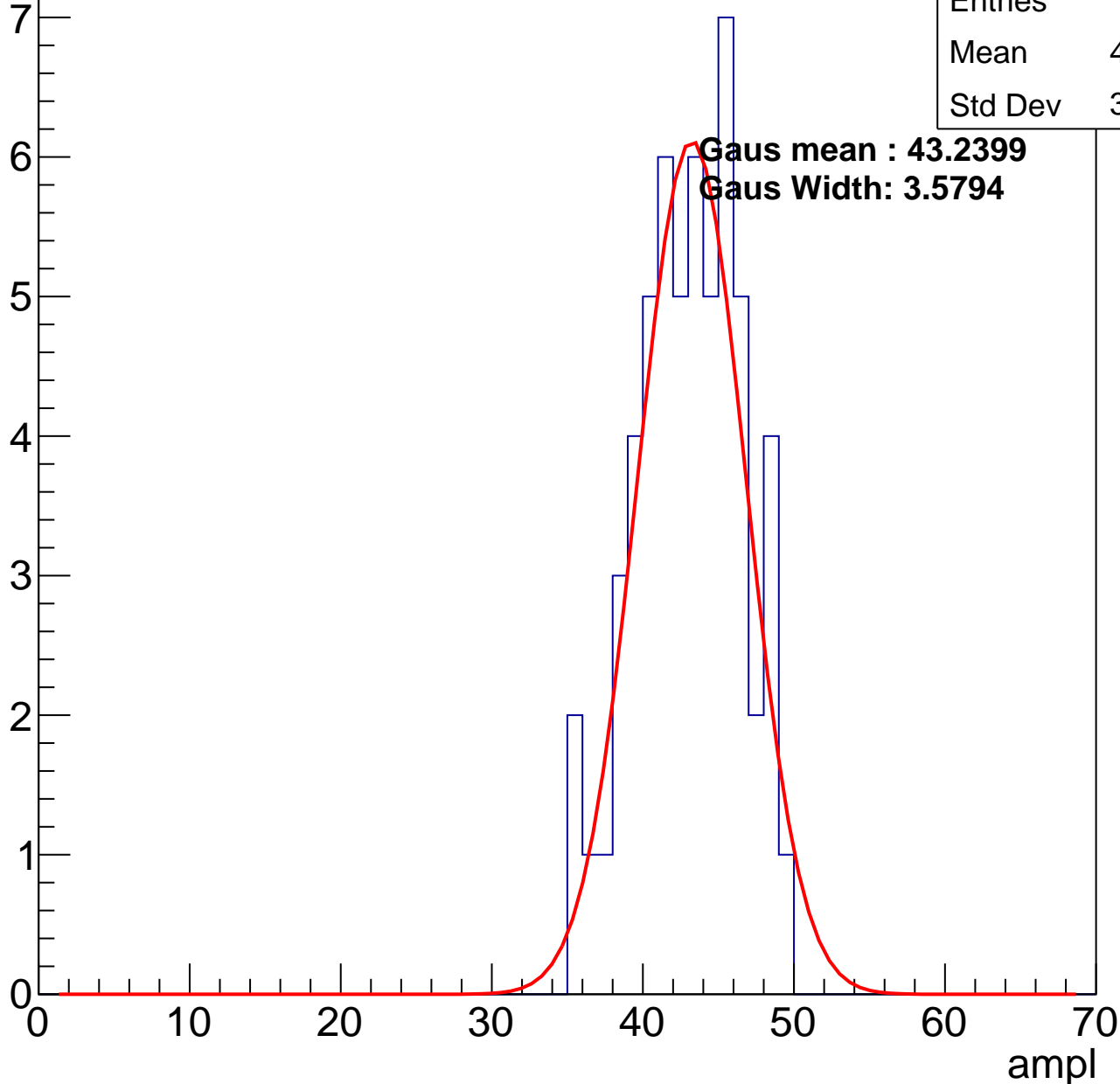


# B1L103S, U11-ch104, adc2

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	57
Mean	42.58
Std Dev	3.408

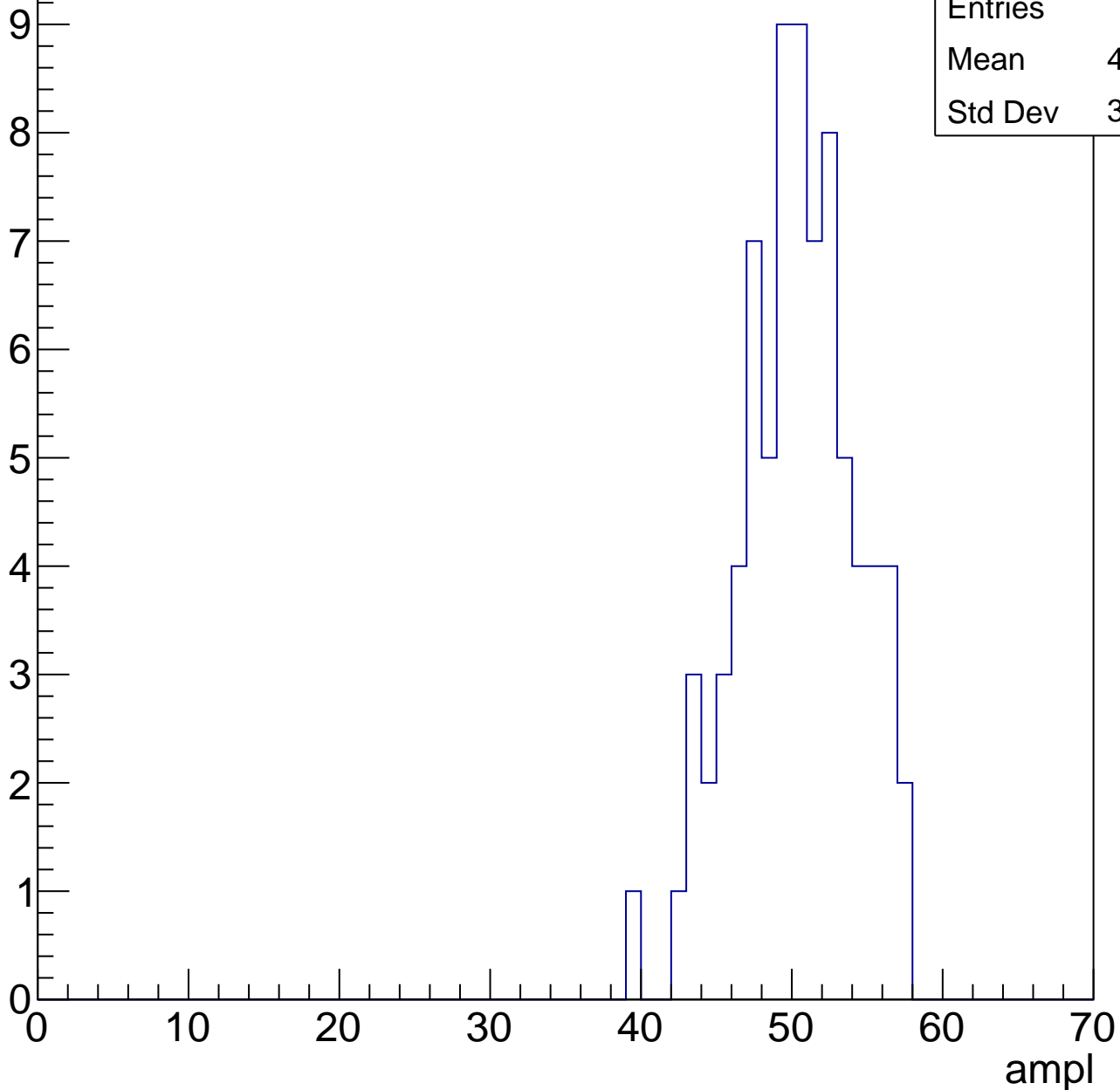


# B1L103S, U11-ch104, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	78
Mean	49.86
Std Dev	3.795

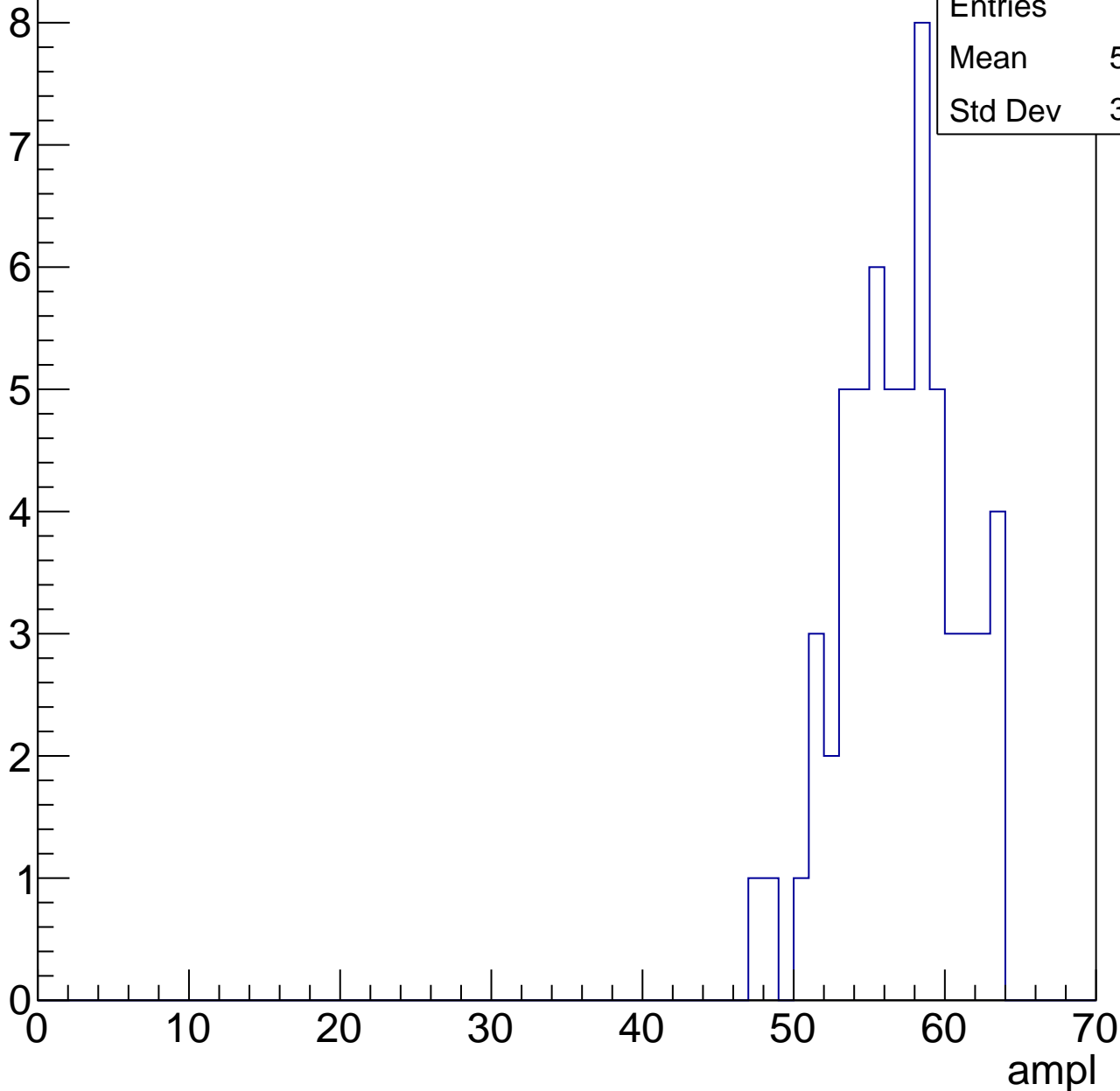


# B1L103S, U11-ch104, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	60
Mean	56.53
Std Dev	3.766

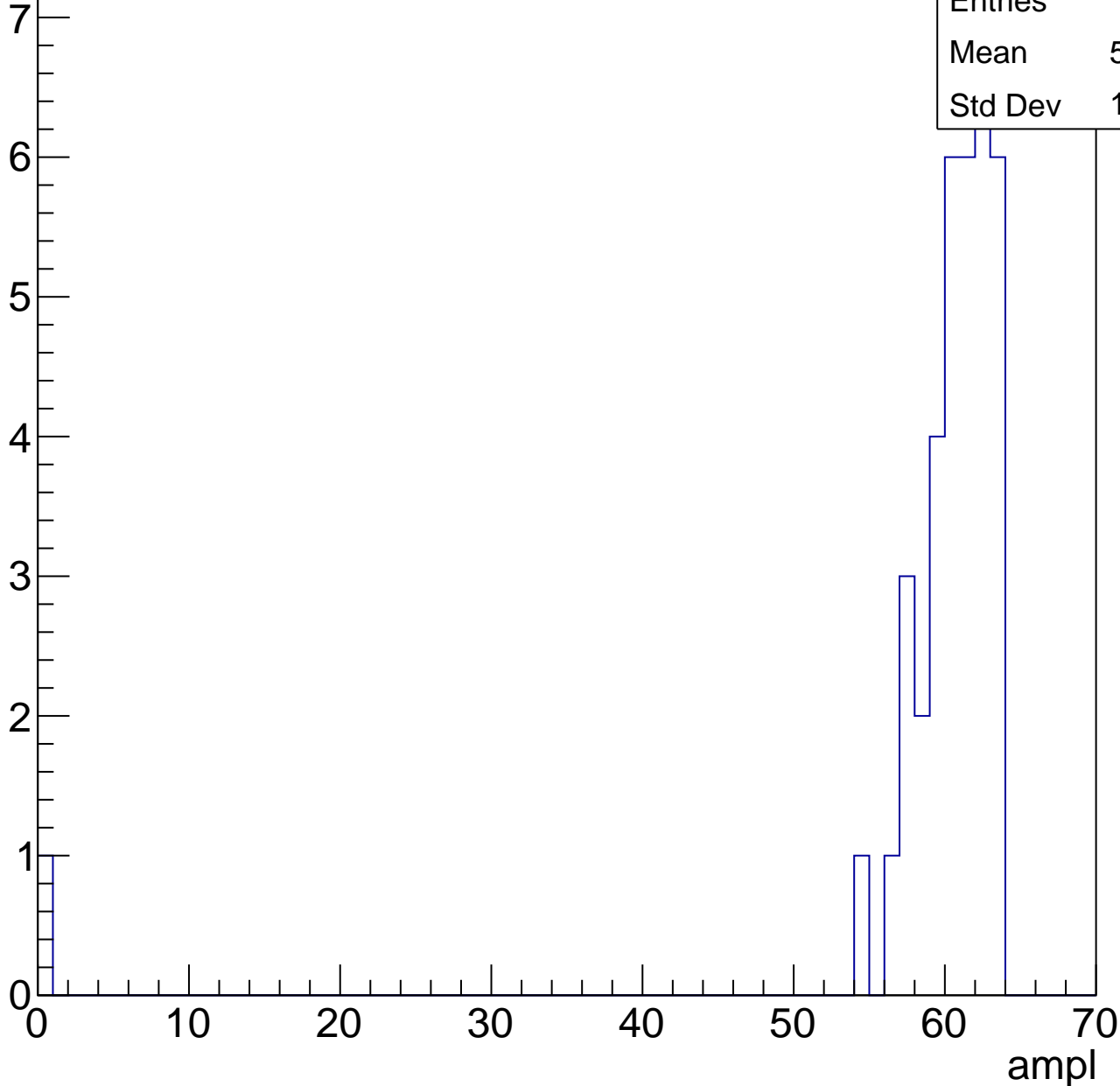


# B1L103S, U11-ch104, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

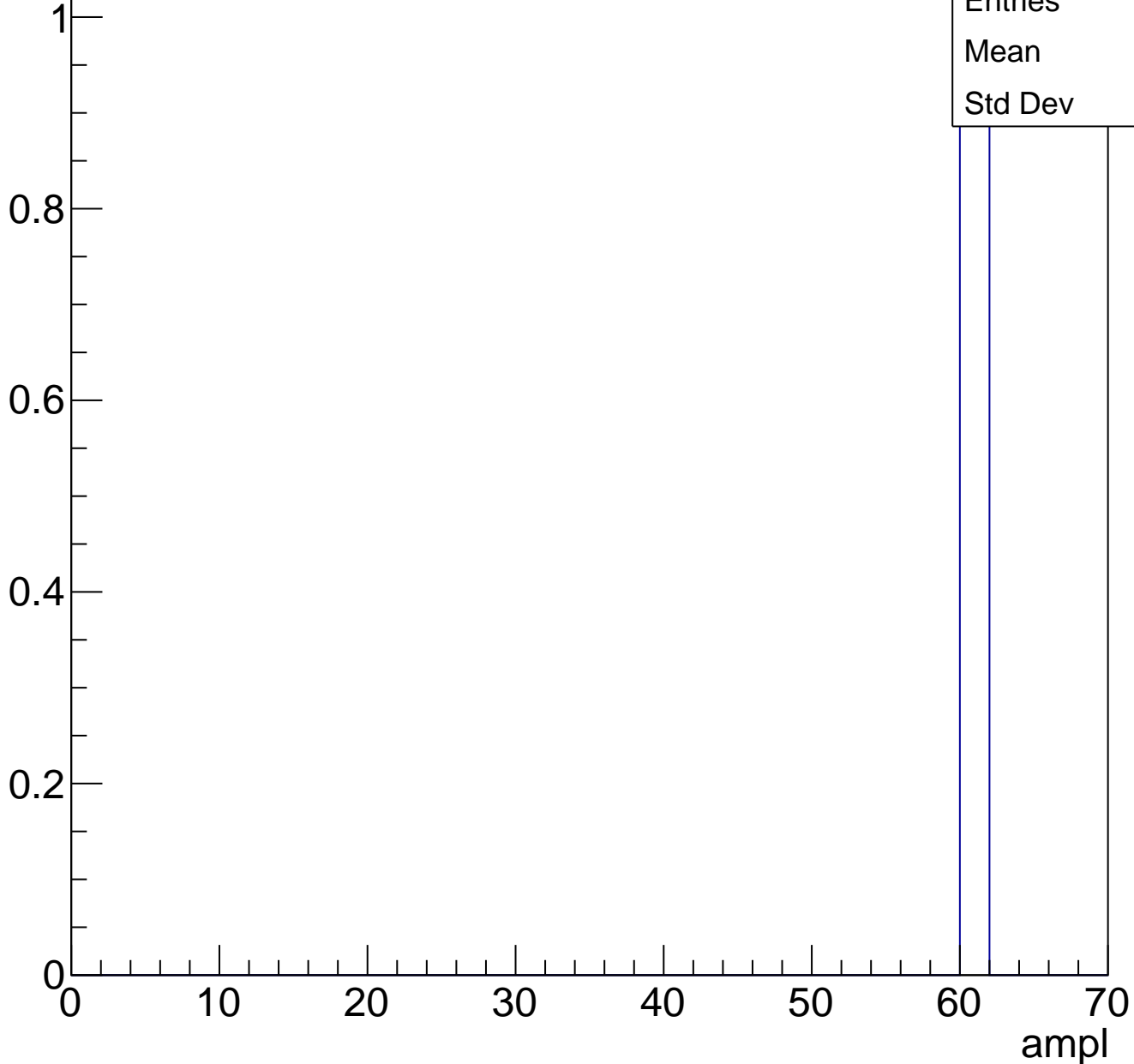
Entries	37
Mean	58.68
Std Dev	10.02



# B1L103S, U11-ch104, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

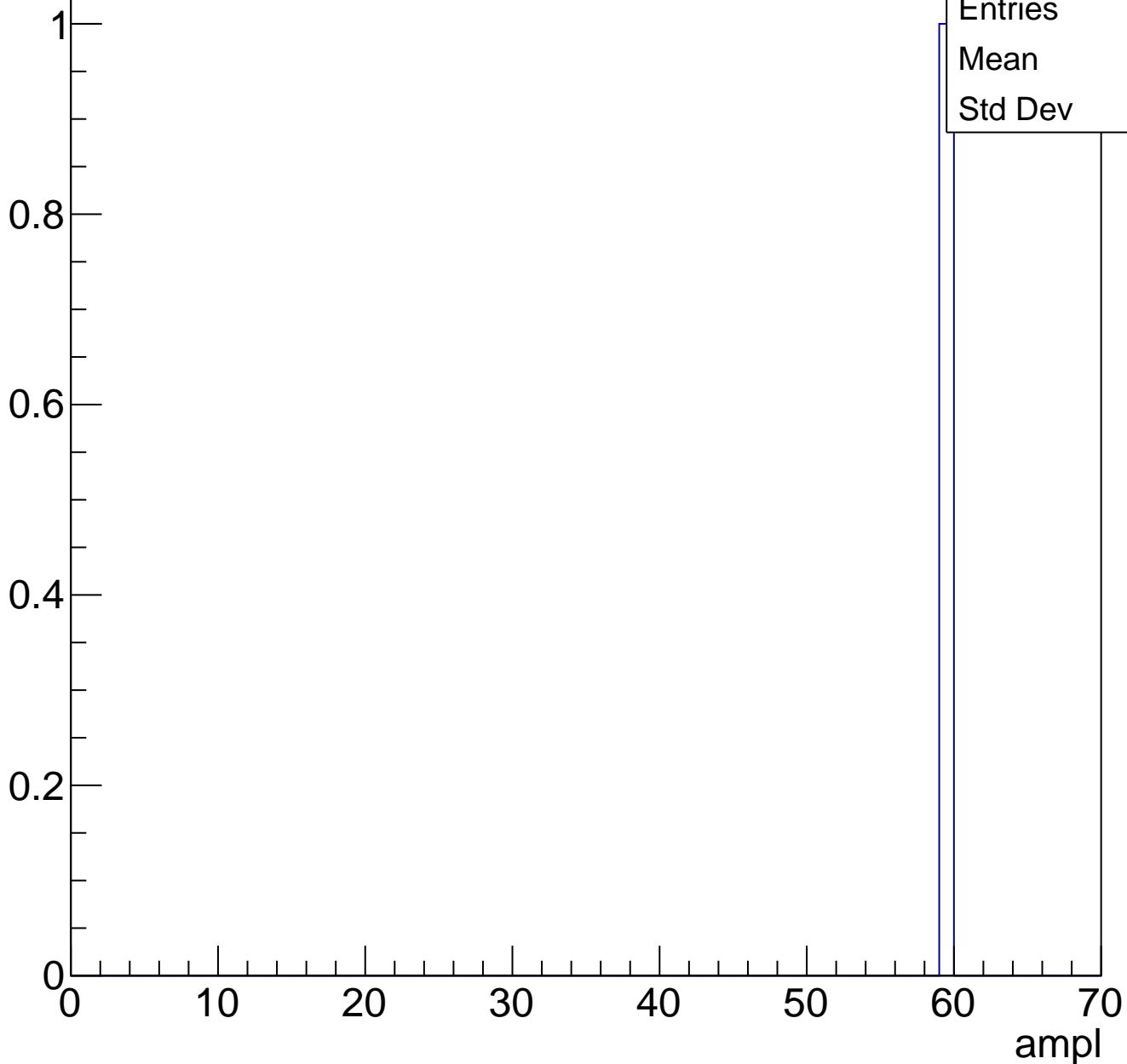




# B1L103S, U11-ch104, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U11-ch105, adc0

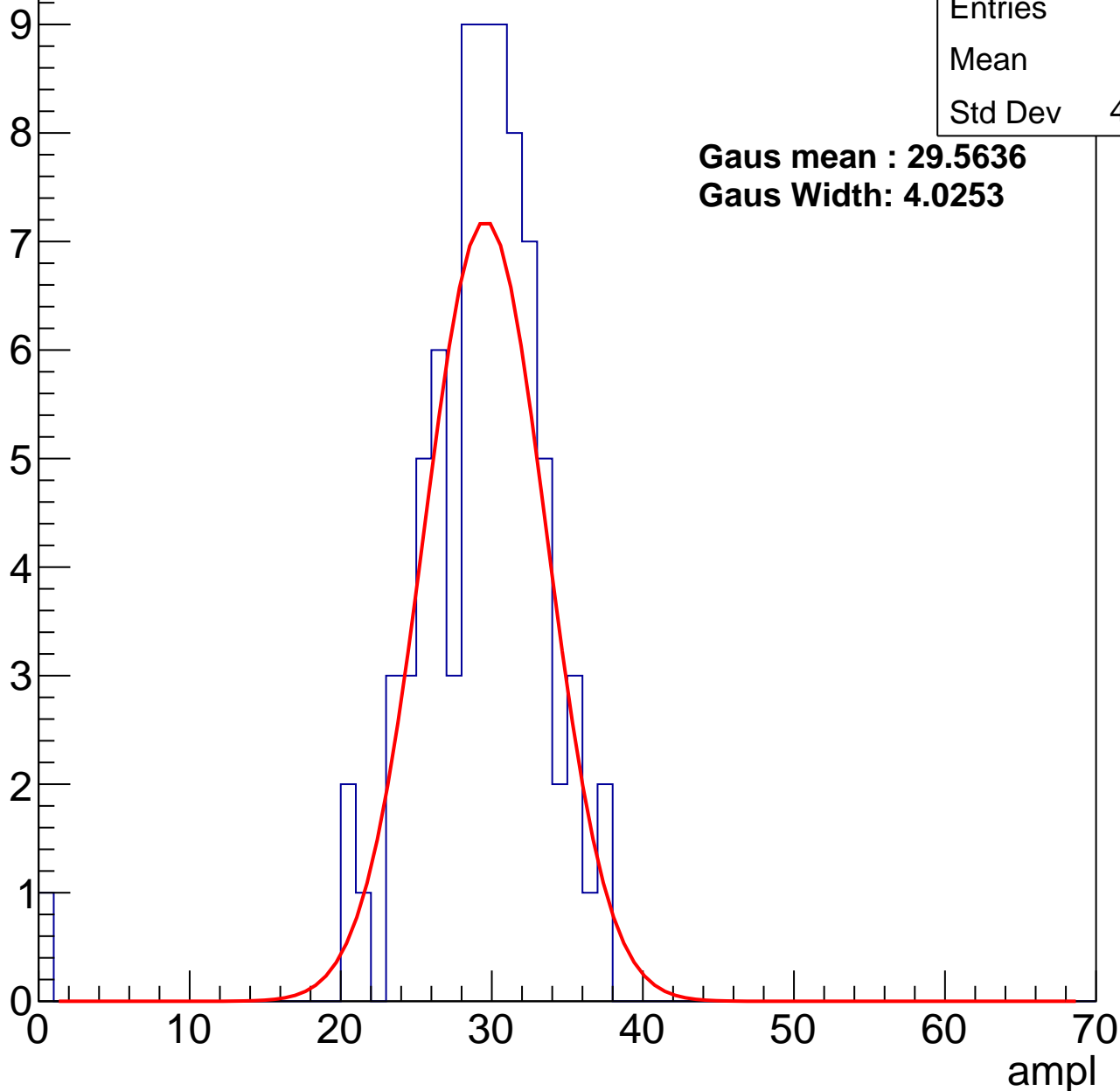
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	79
Mean	28.7
Std Dev	4.926

**Gaus mean : 29.5636**

**Gaus Width: 4.0253**



# B1L103S, U11-ch105, adc1

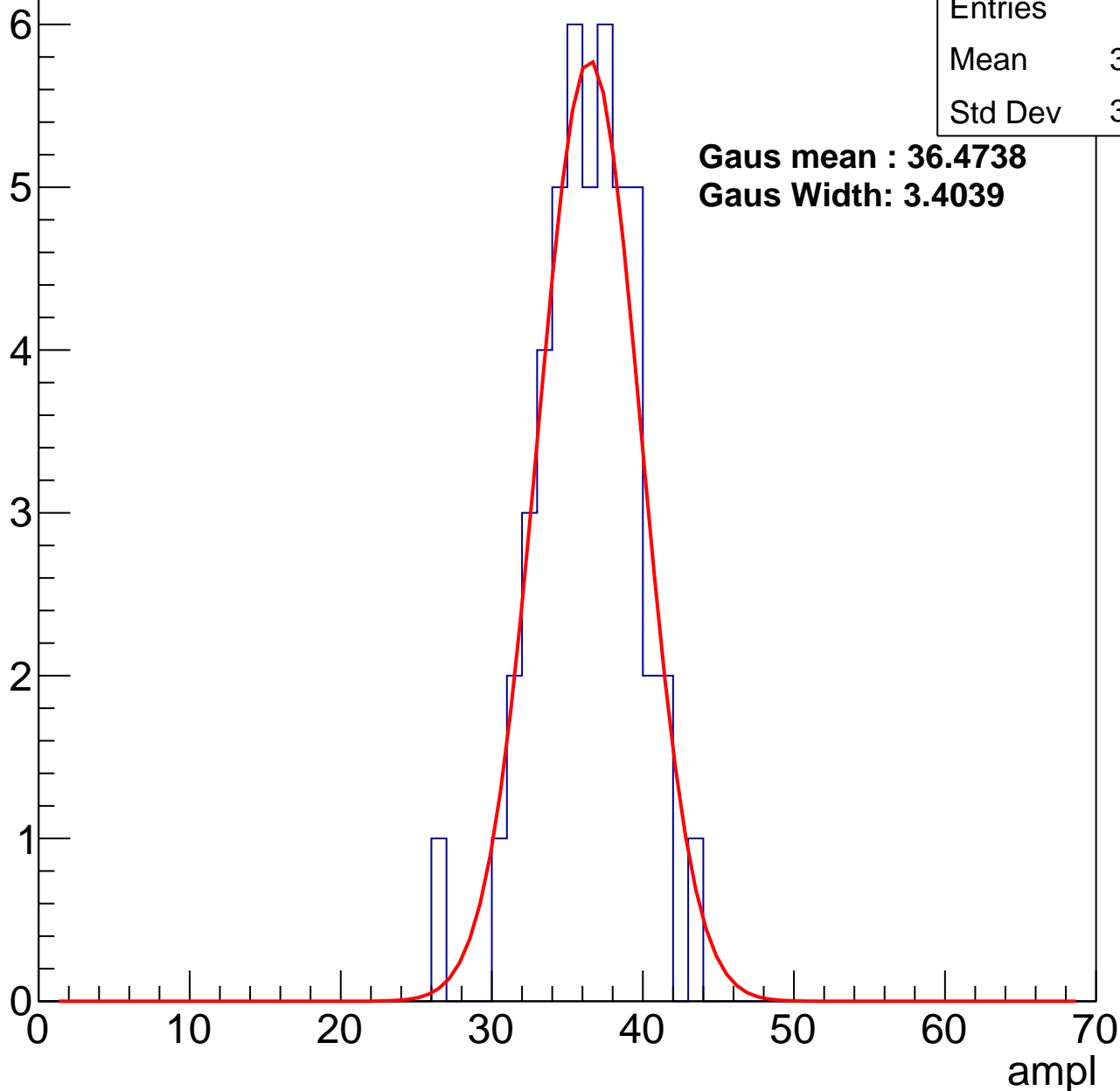
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	48
Mean	35.79
Std Dev	3.214

**Gaus mean : 36.4738**

**Gaus Width: 3.4039**



# B1L103S, U11-ch105, adc2

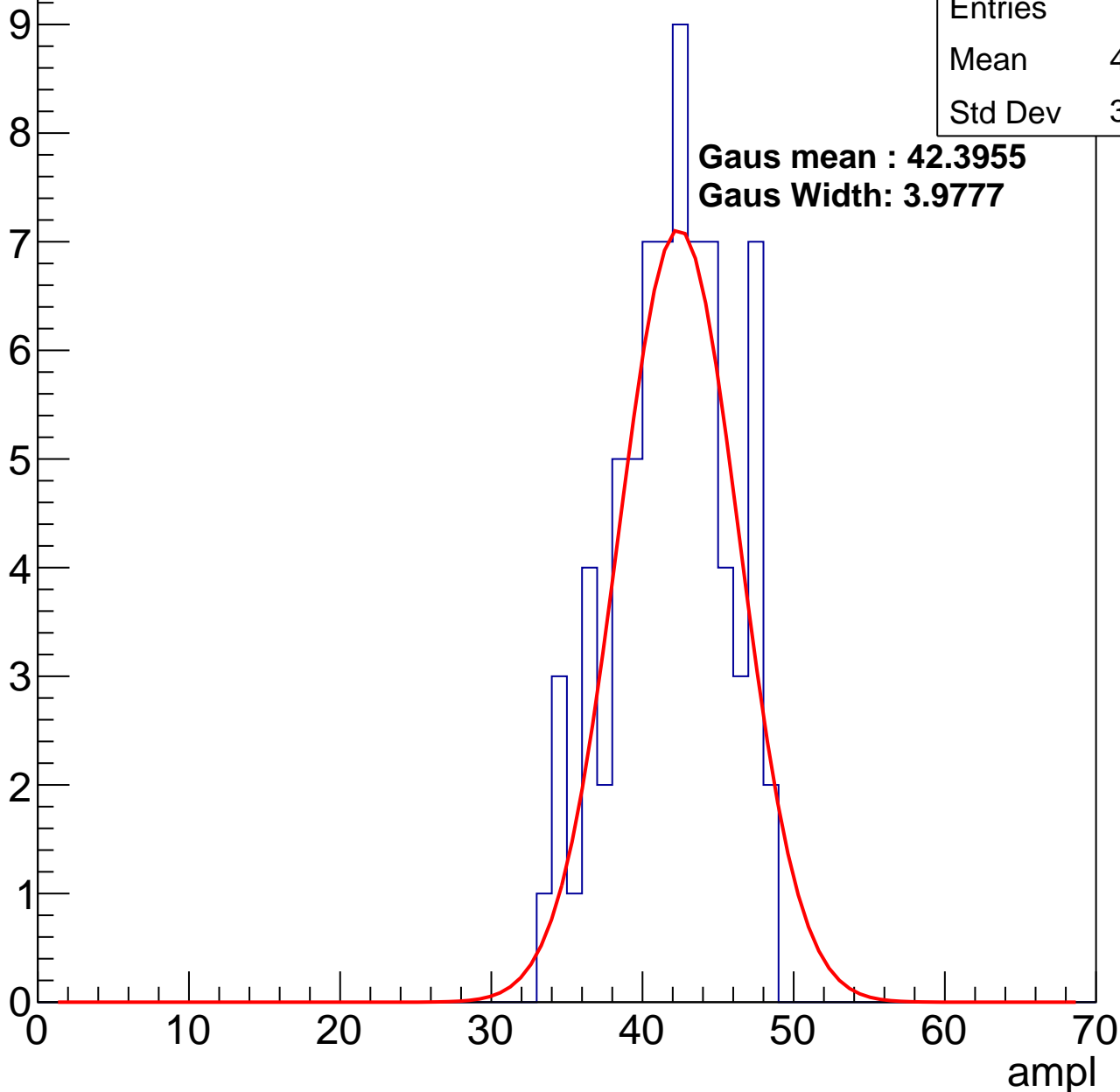
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	74
Mean	41.49
Std Dev	3.717

**Gaus mean : 42.3955**

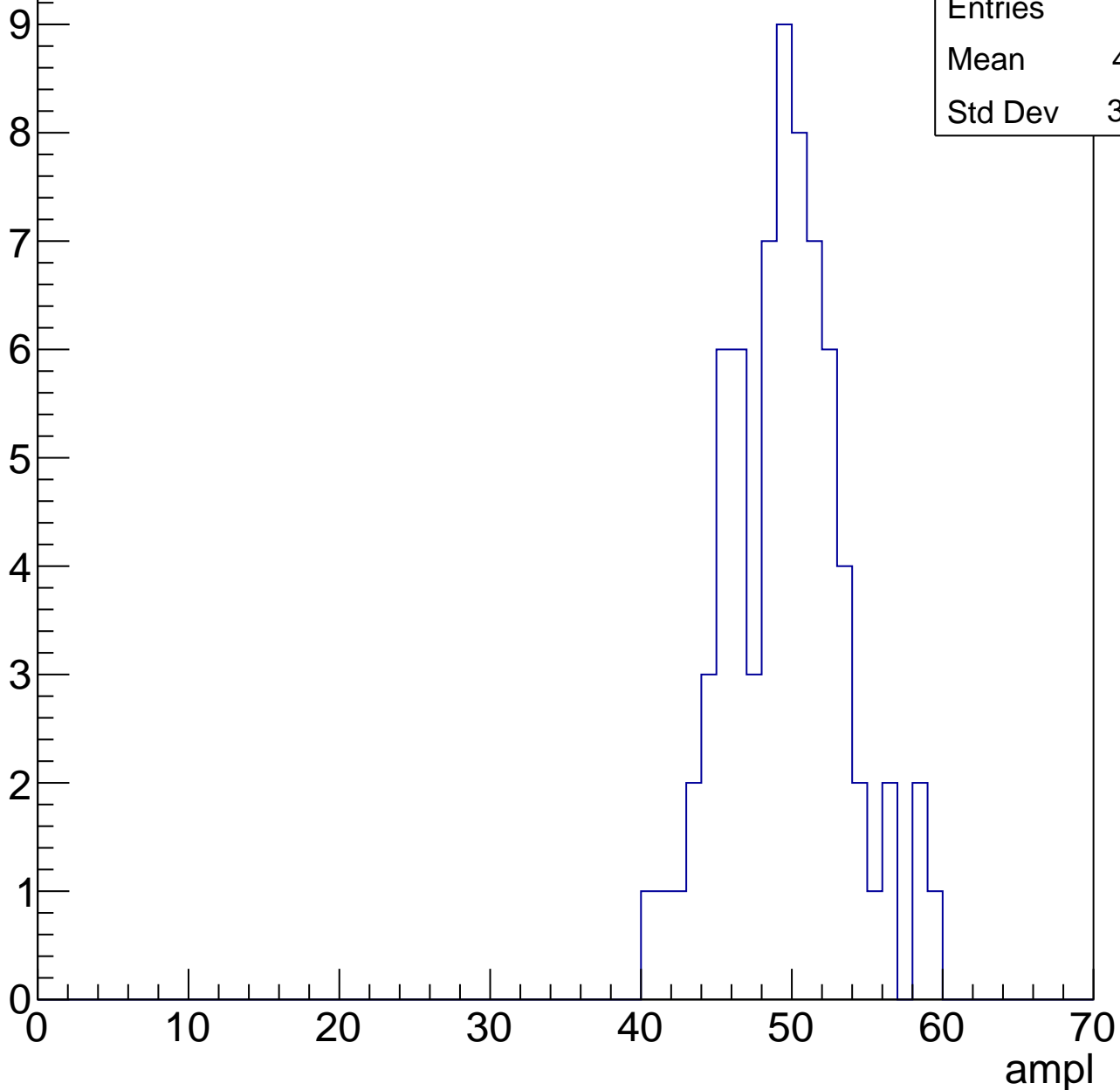
**Gaus Width: 3.9777**



# B1L103S, U11-ch105, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

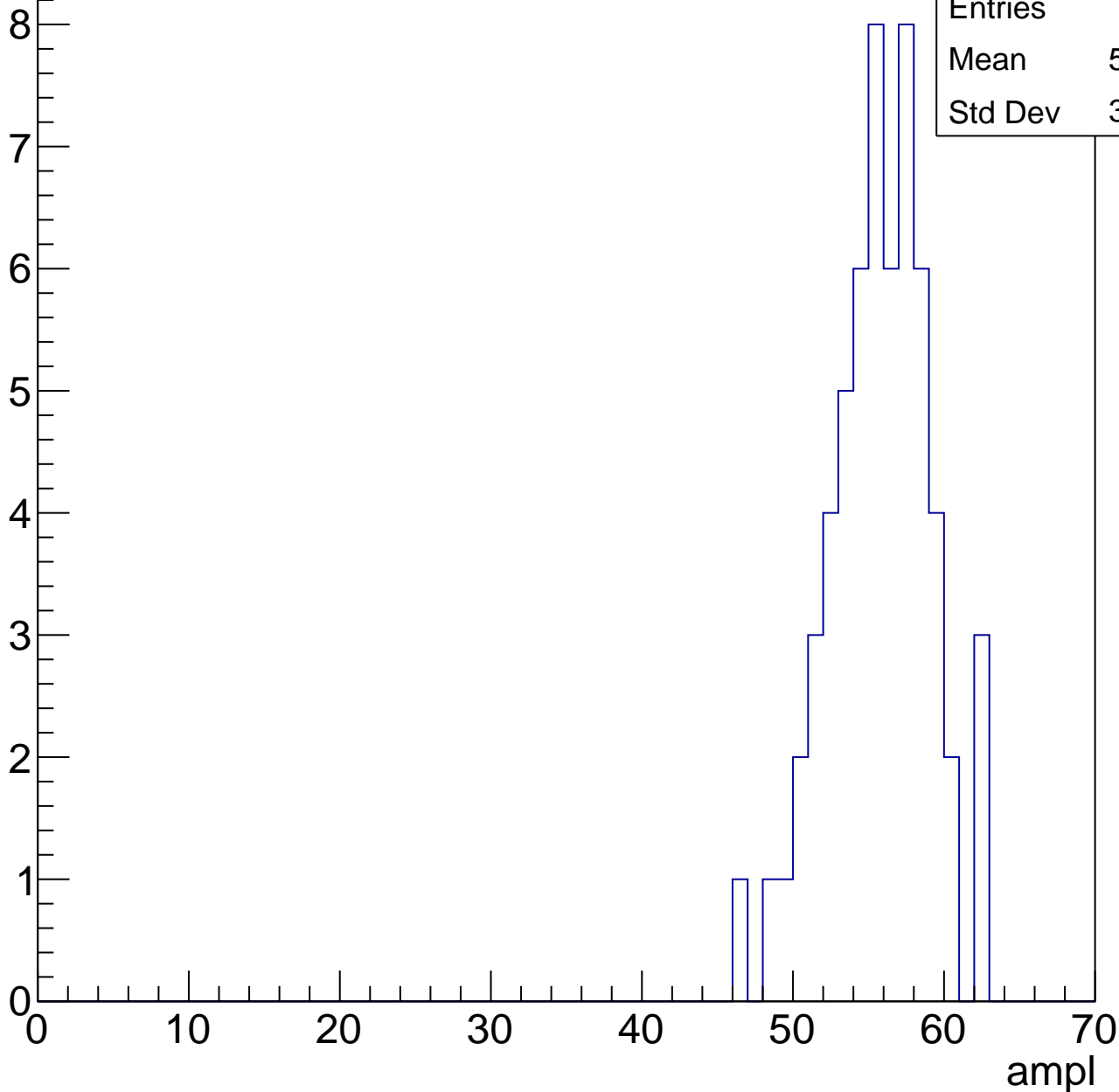


# B1L103S, U11-ch105, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

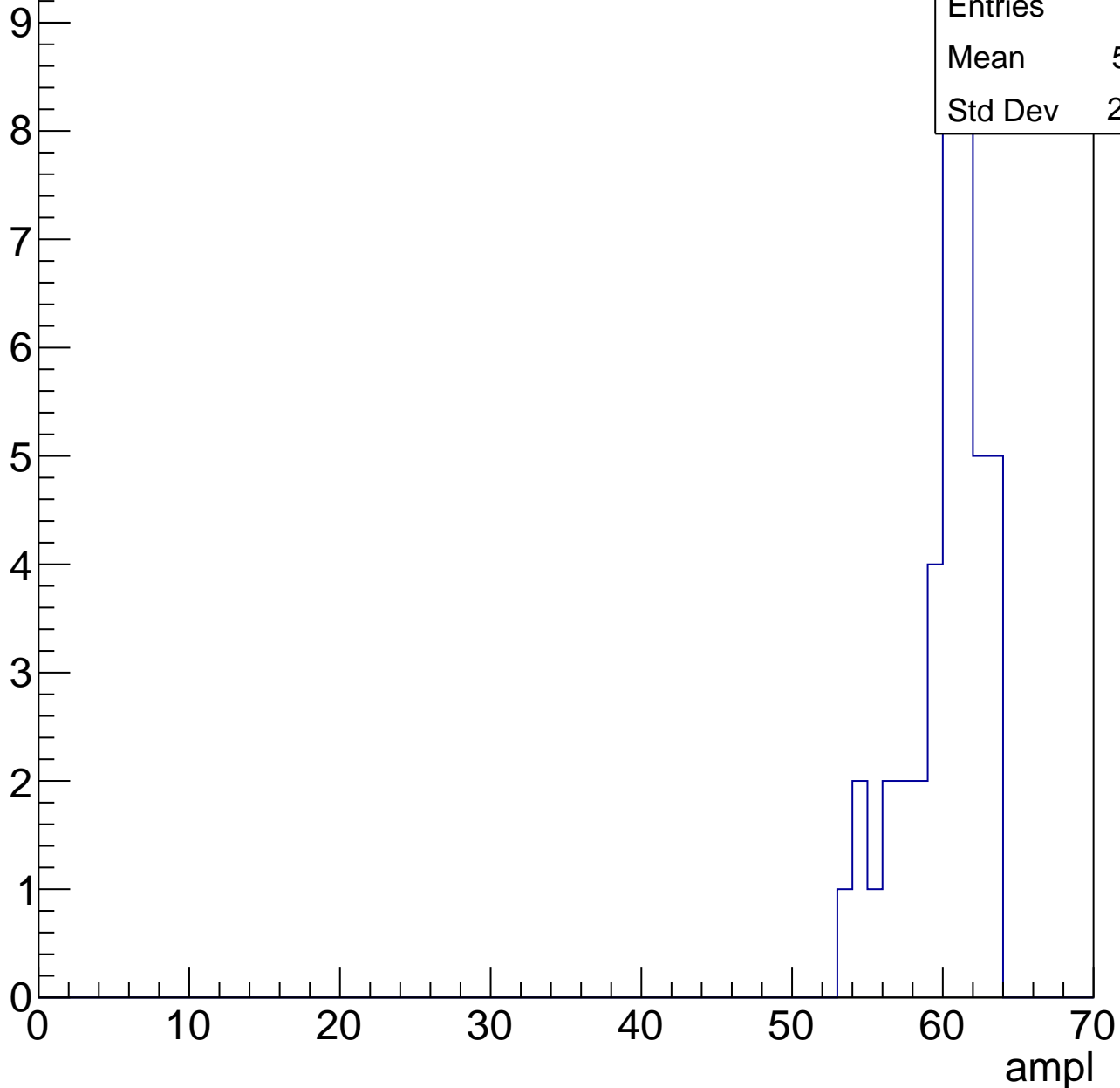
Entries	60
Mean	55.25
Std Dev	3.355



# B1L103S, U11-ch105, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



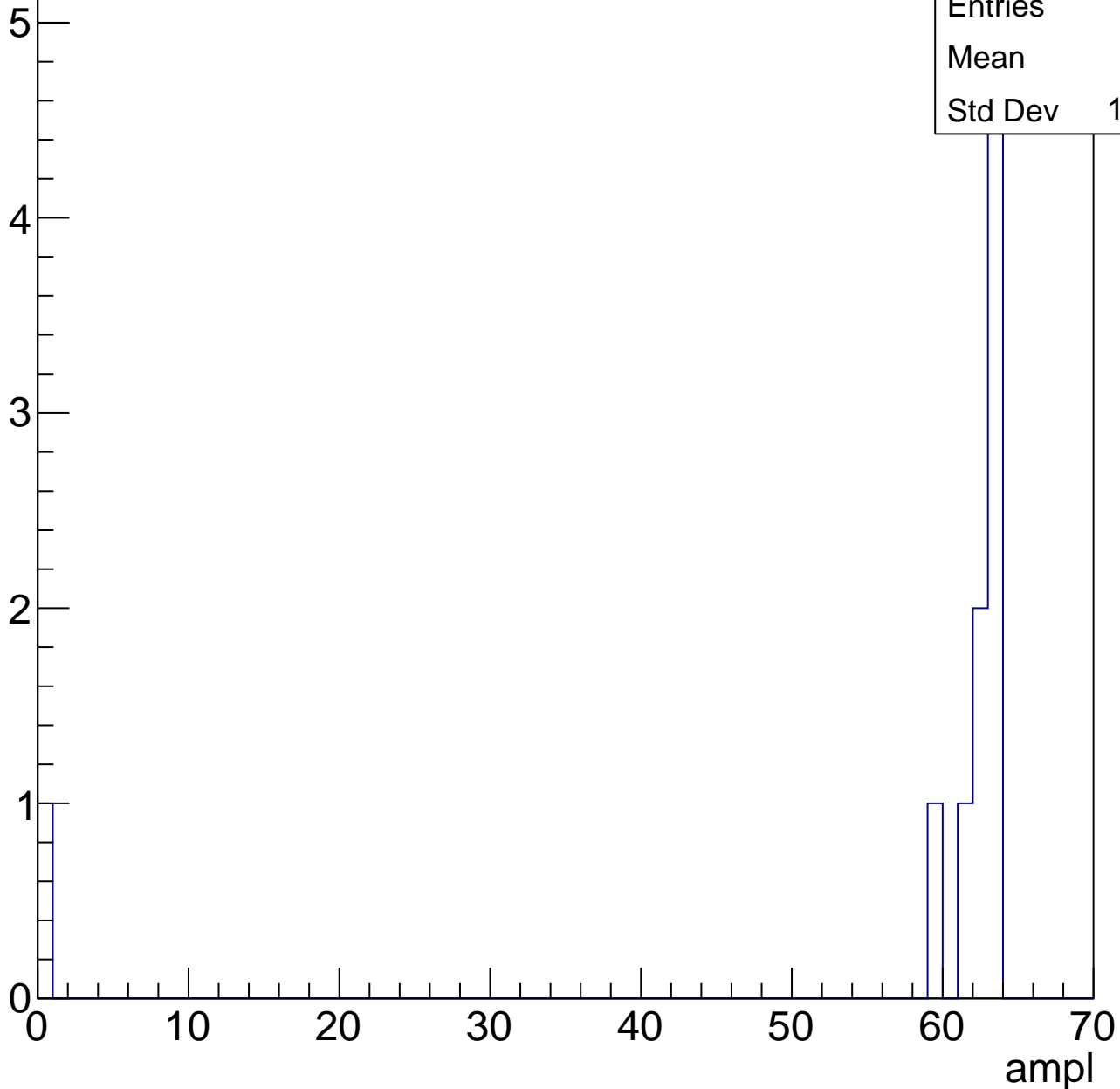
Entries	41
Mean	59.71
Std Dev	2.606

# B1L103S, U11-ch105, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	10
Mean	55.9
Std Dev	18.67



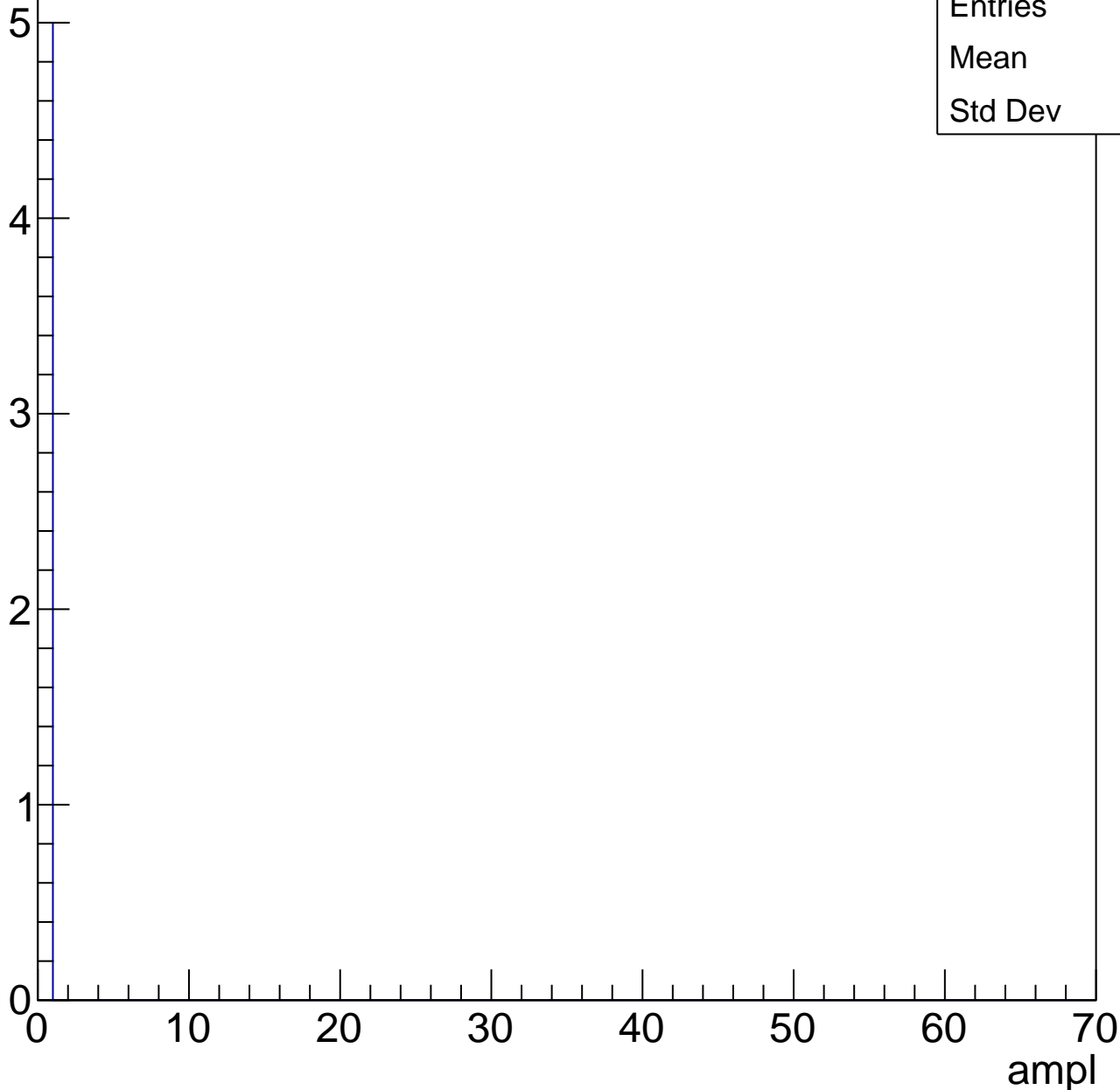


# B1L103S, U11-ch105, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	5
Mean	0
Std Dev	0



# B1L103S, U11-ch106, adc0

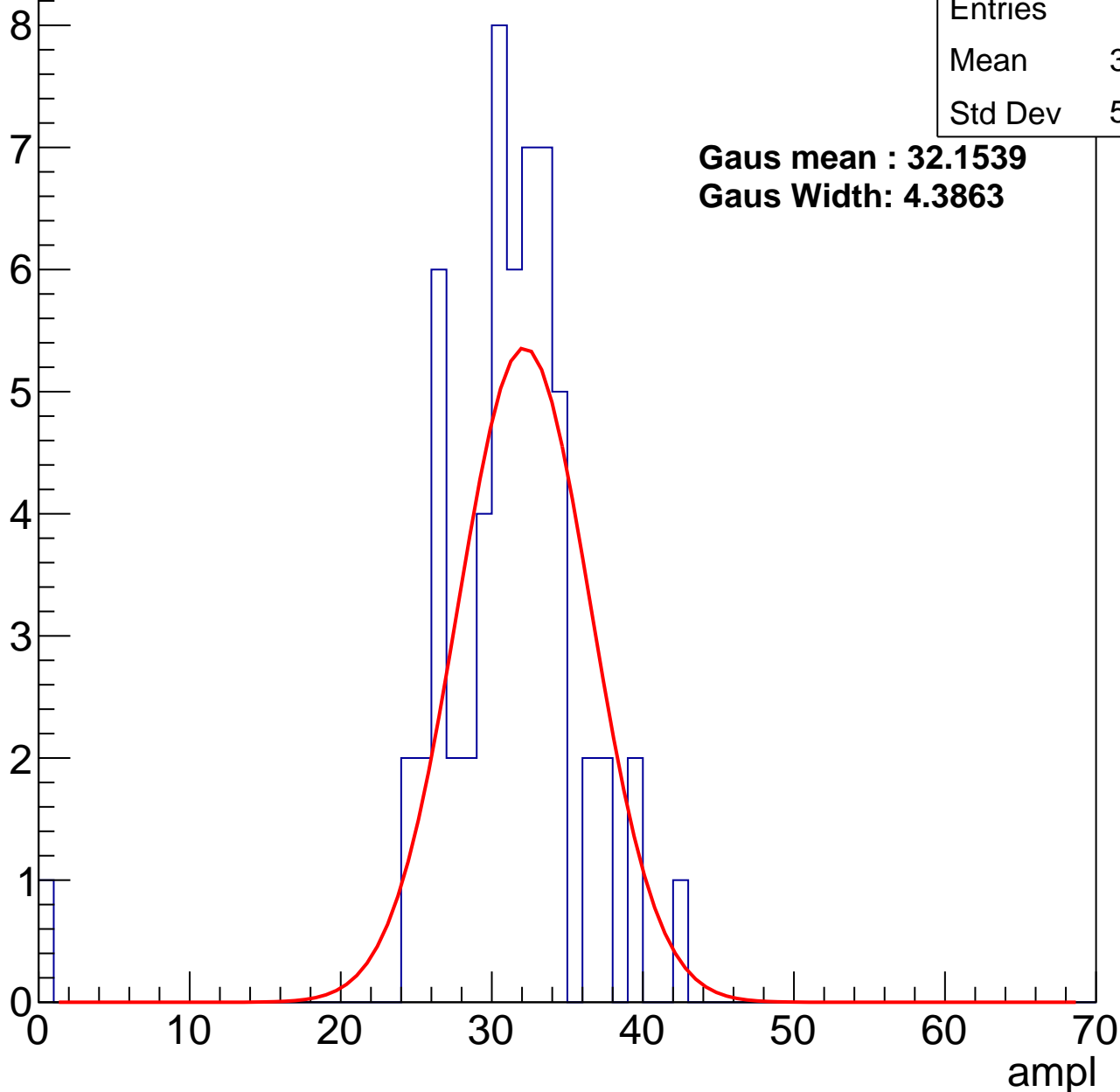
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	59
Mean	30.46
Std Dev	5.506

**Gaus mean : 32.1539**

**Gaus Width: 4.3863**



# B1L103S, U11-ch106, adc1

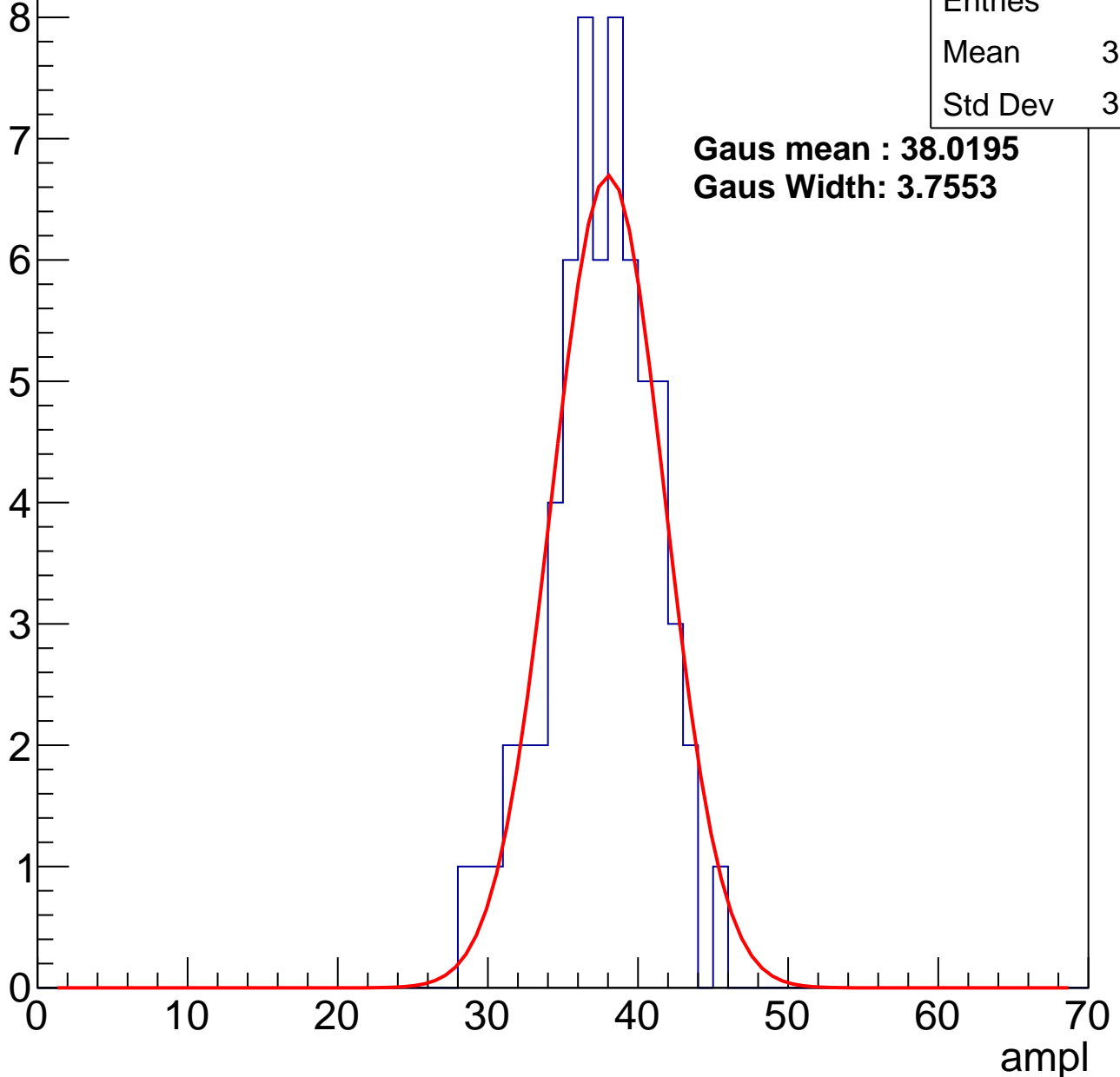
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	37.06
Std Dev	3.527

**Gaus mean : 38.0195**

**Gaus Width: 3.7553**



# B1L103S, U11-ch106, adc2

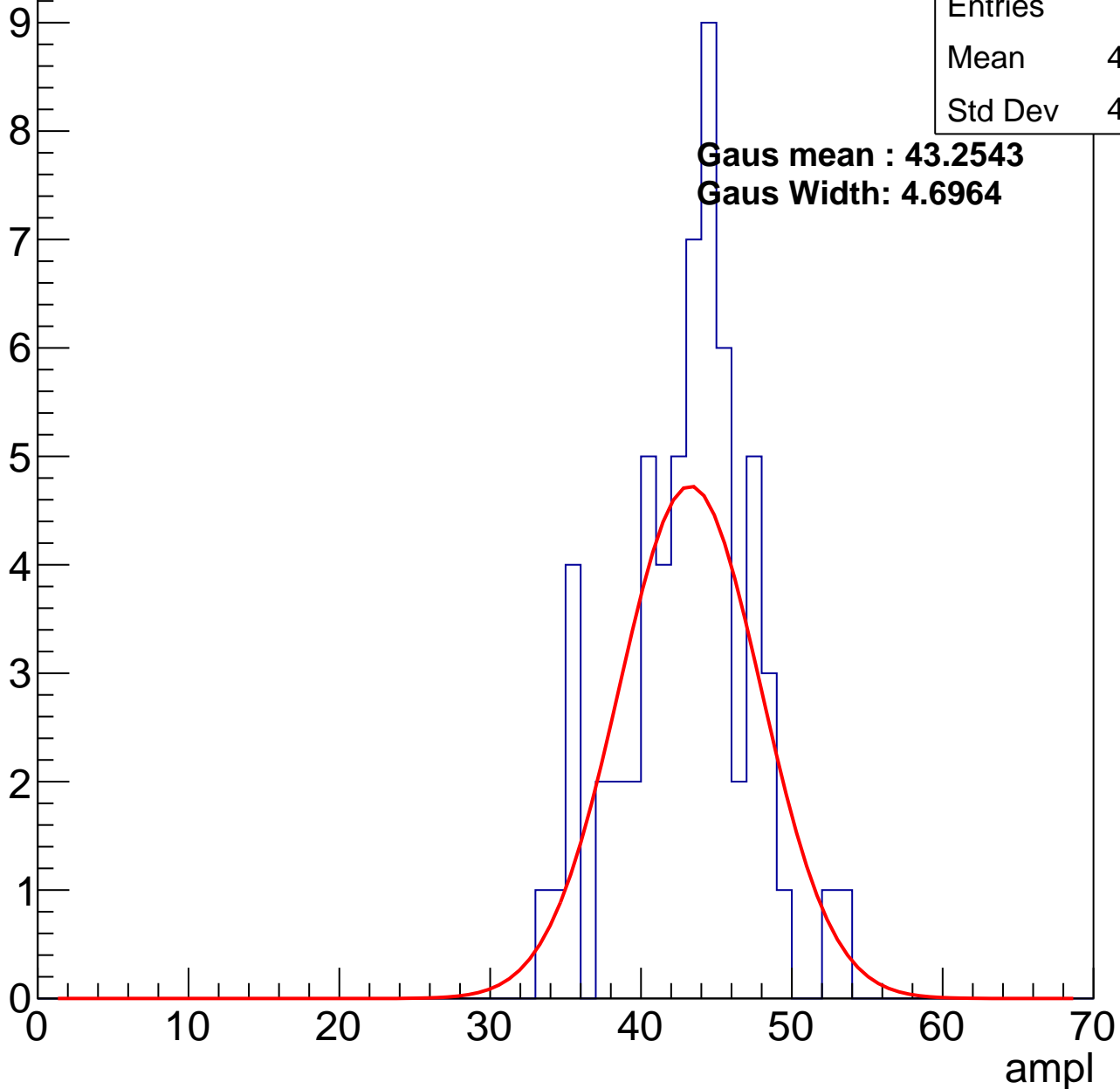
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	61
Mean	42.64
Std Dev	4.192

**Gaus mean : 43.2543**

**Gaus Width: 4.6964**

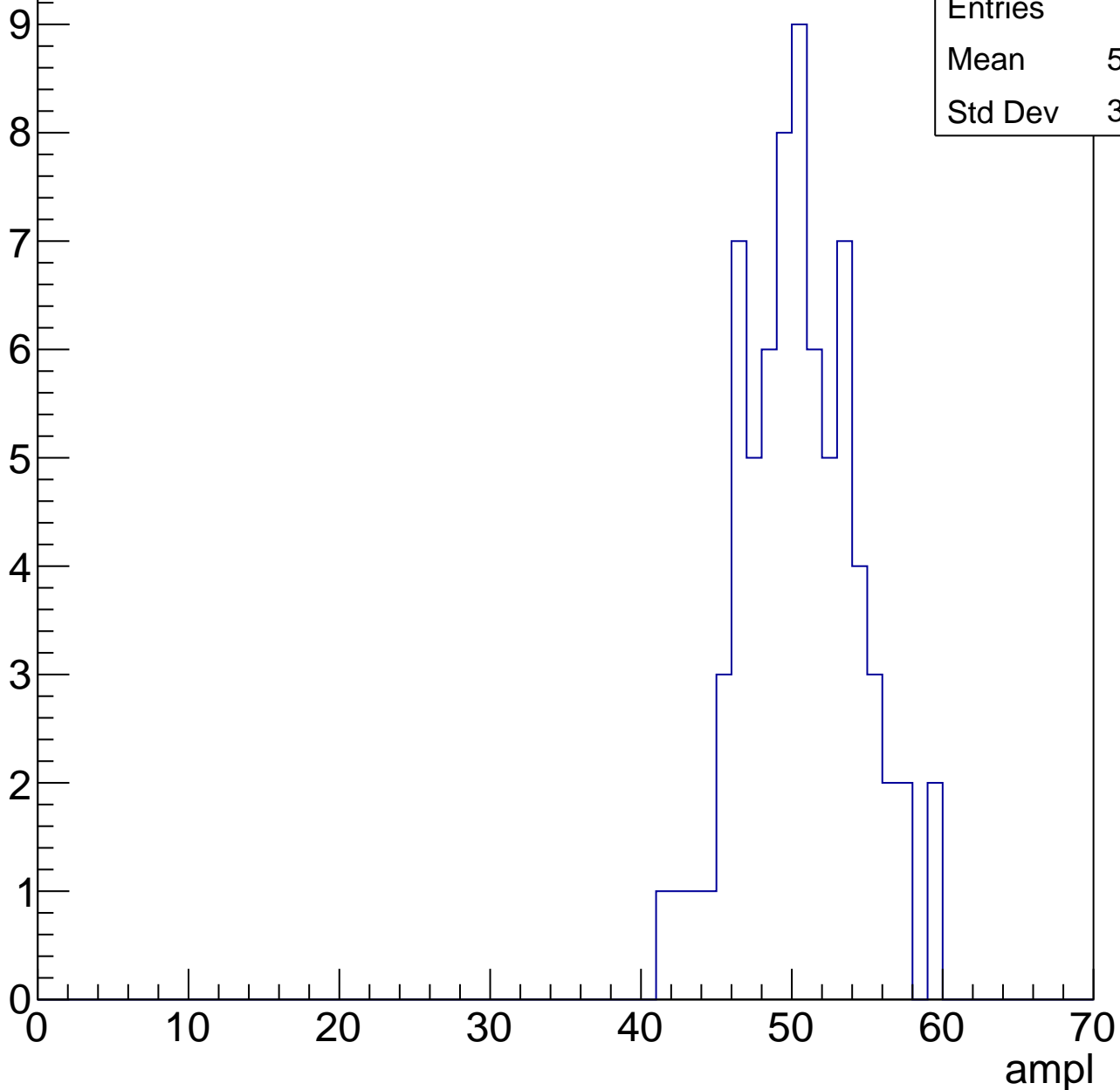


# B1L103S, U11-ch106, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	73
Mean	50.05
Std Dev	3.799

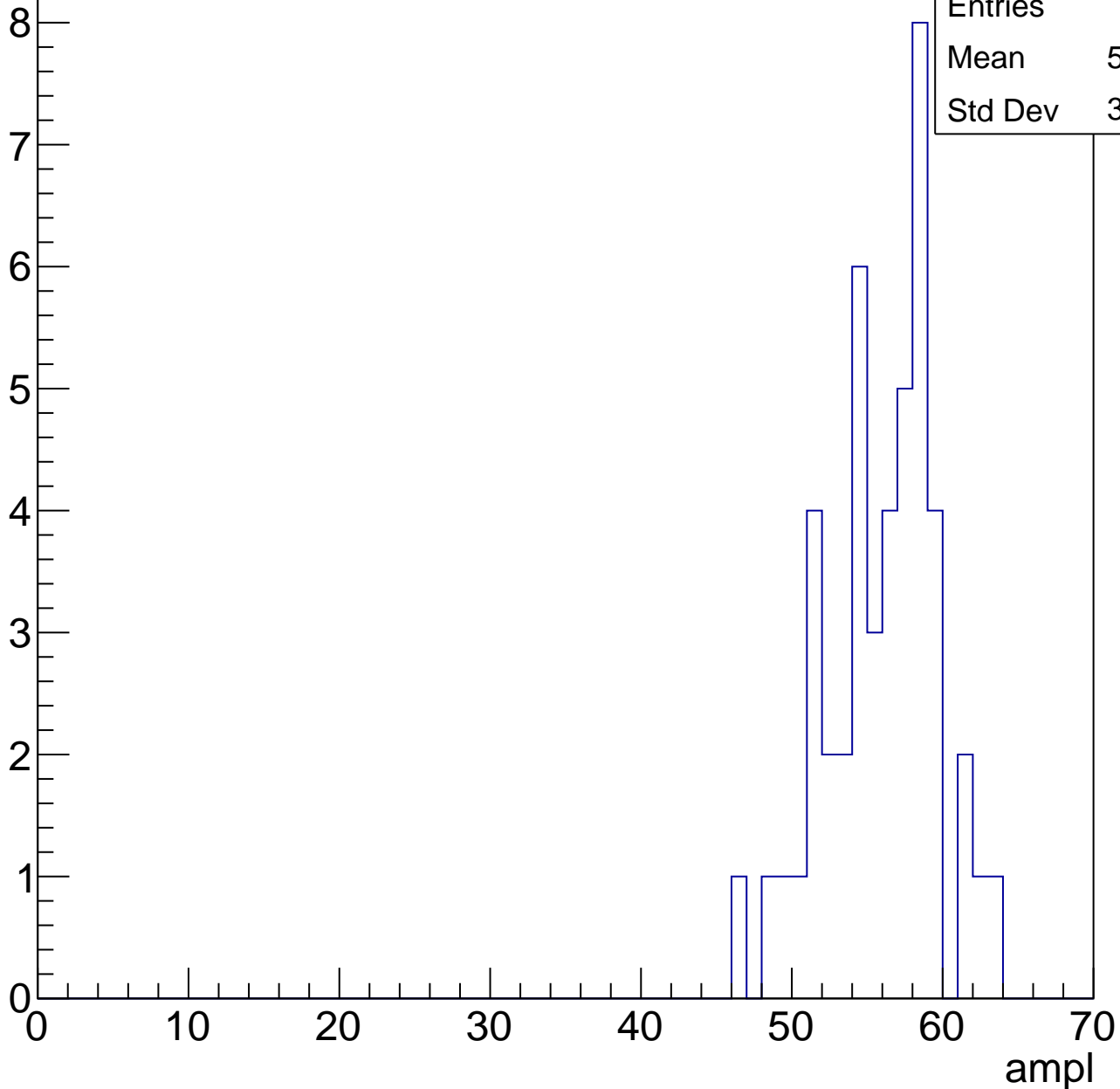


# B1L103S, U11-ch106, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	46
Mean	55.48
Std Dev	3.676

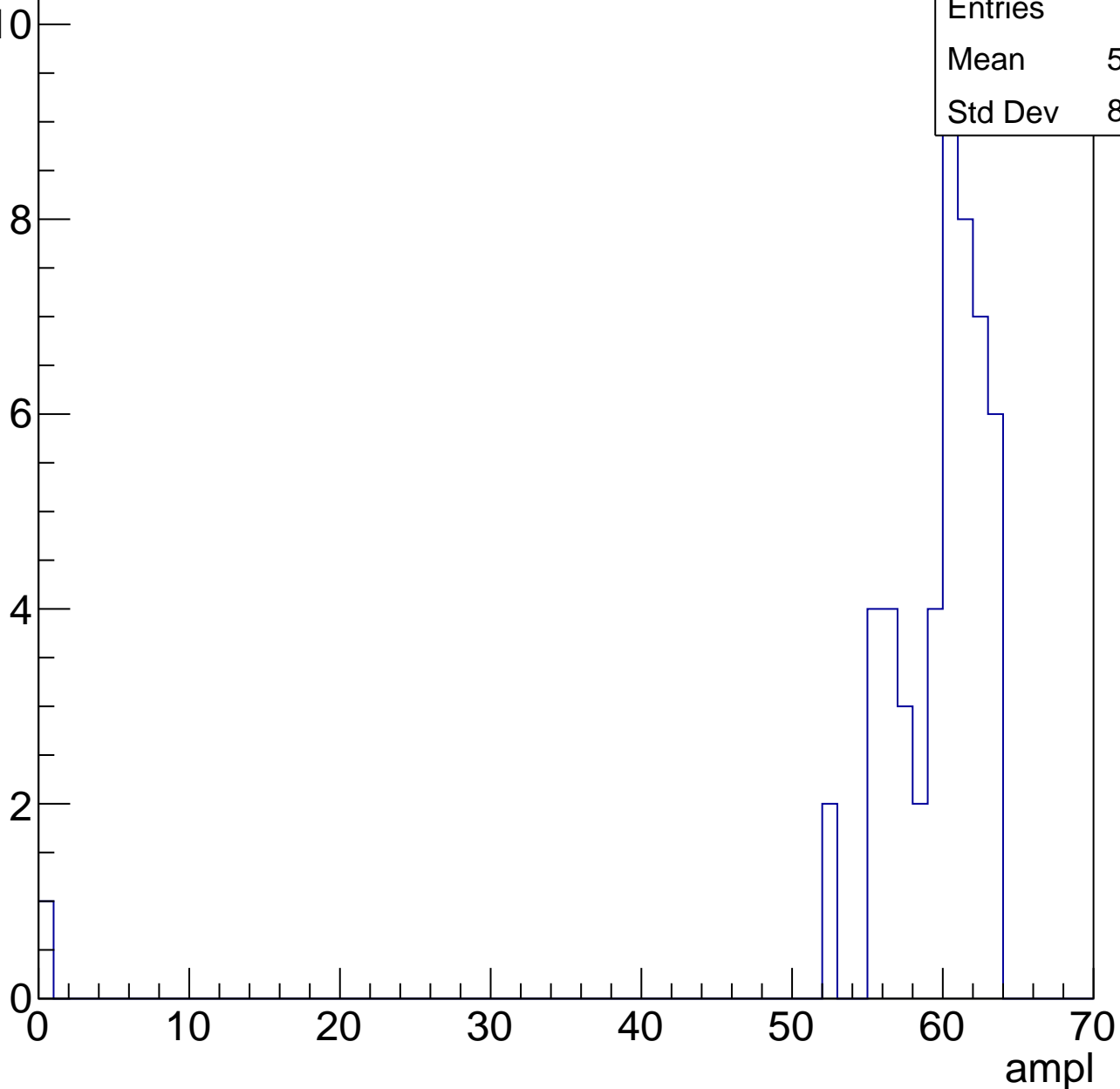


# B1L103S, U11-ch106, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	51
Mean	58.25
Std Dev	8.706



# B1L103S, U11-ch106, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U11-ch106, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U11-ch107, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	94
Mean	29.26
Std Dev	5.789

**Gaus mean : 30.8756**

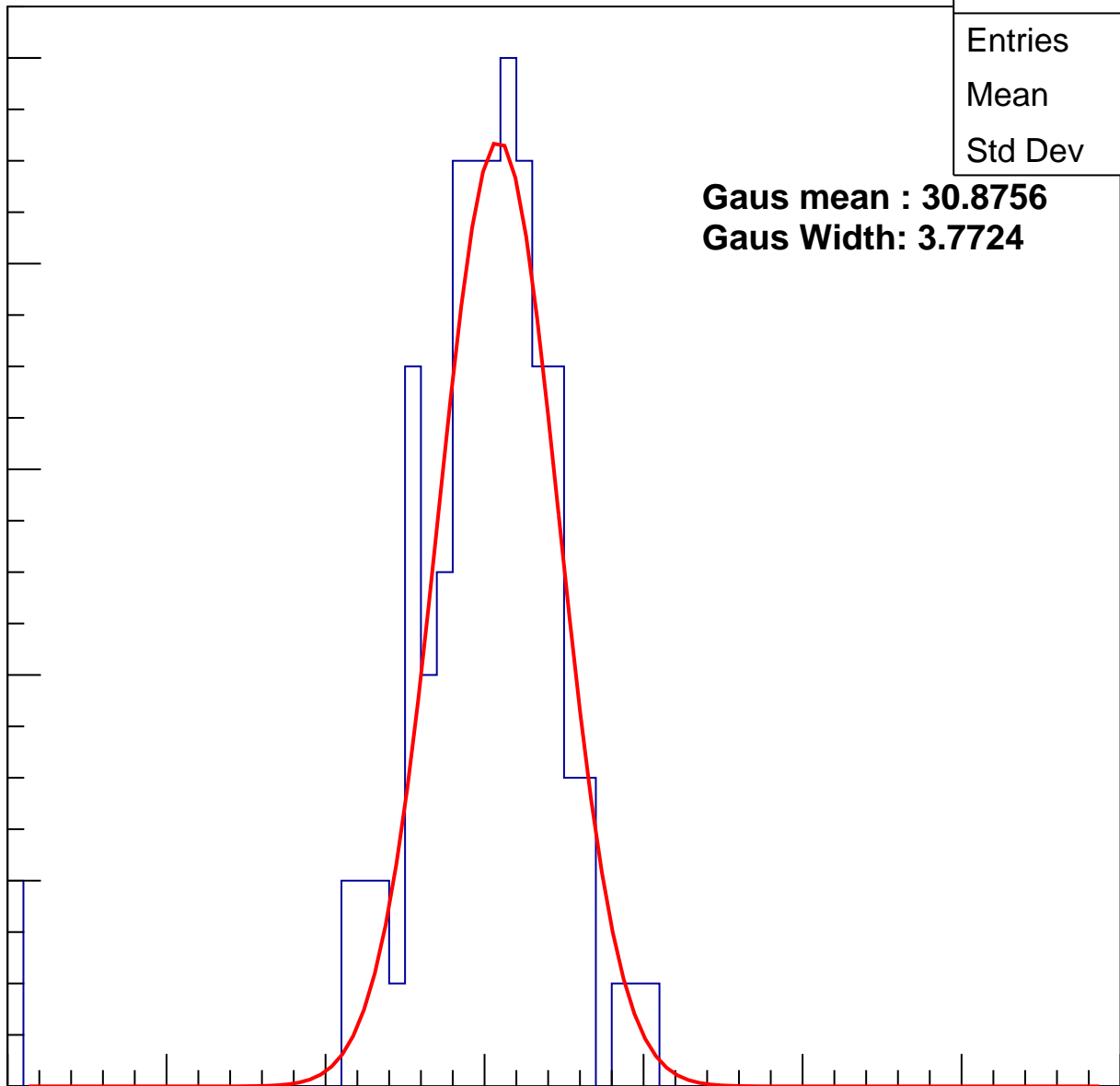
**Gaus Width: 3.7724**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U11-ch107, adc1

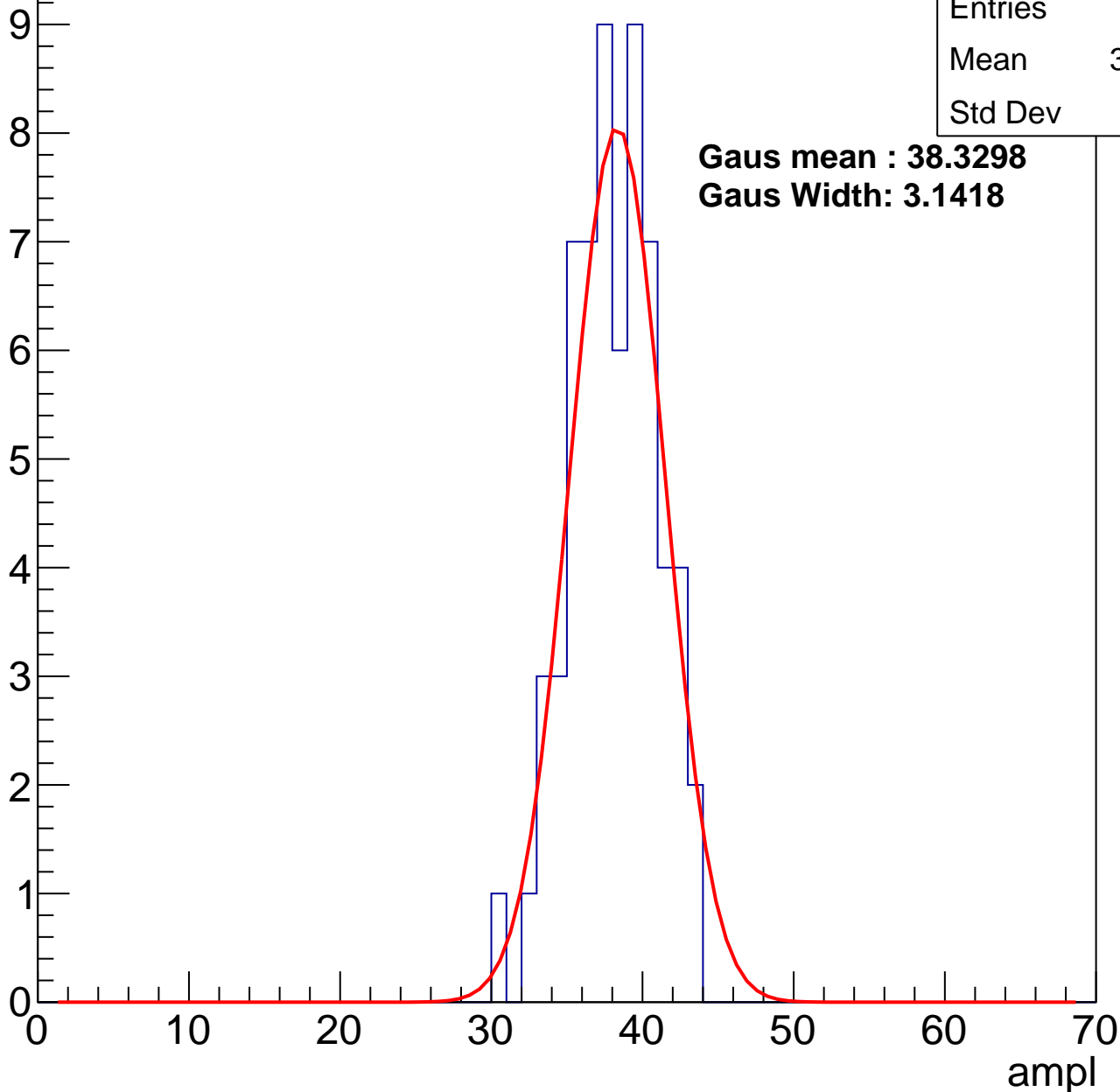
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	37.62
Std Dev	2.82

**Gaus mean : 38.3298**

**Gaus Width: 3.1418**



# B1L103S, U11-ch107, adc2

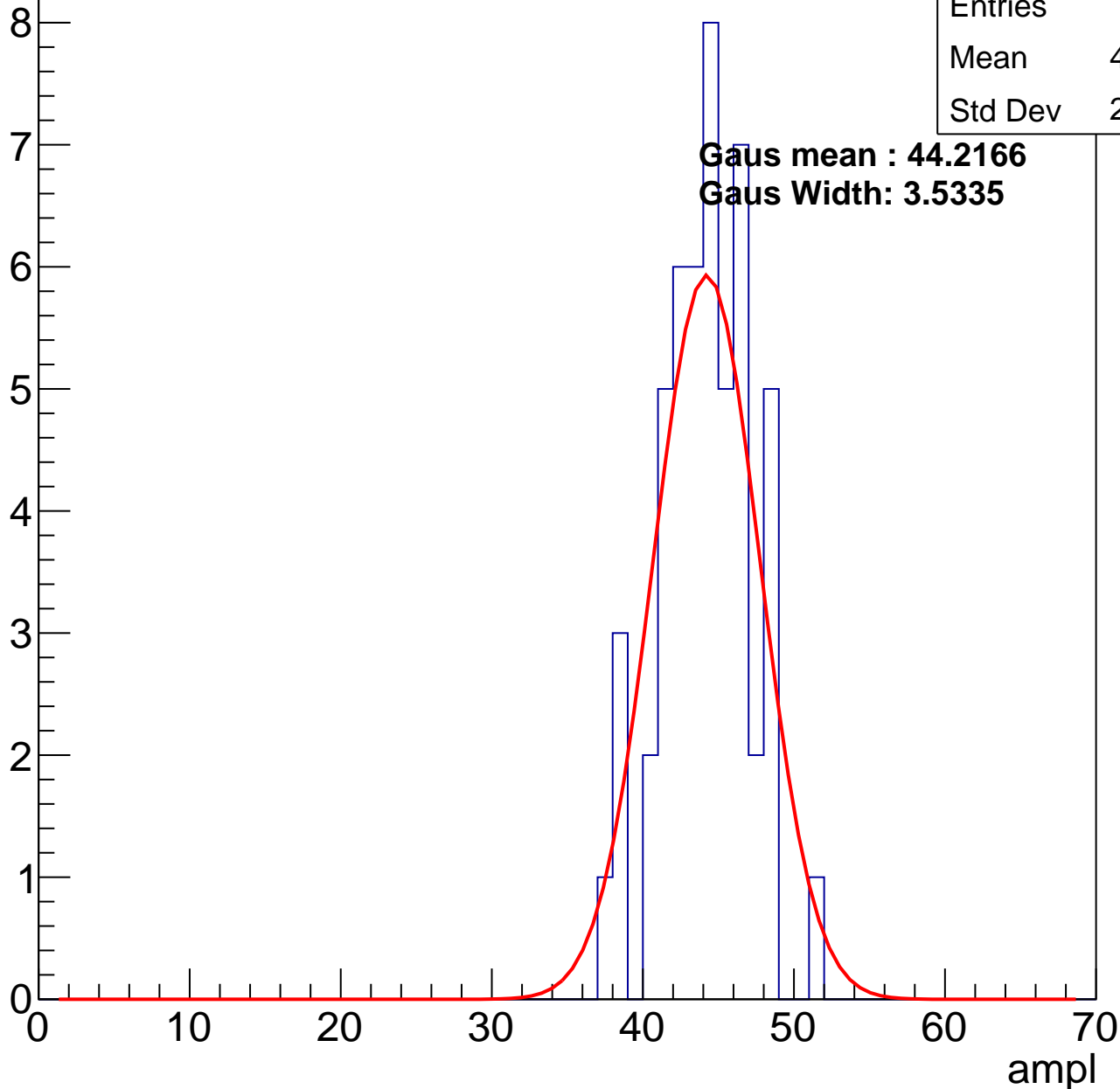
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	51
Mean	43.73
Std Dev	2.938

**Gaus mean : 44.2166**

**Gaus Width: 3.5335**

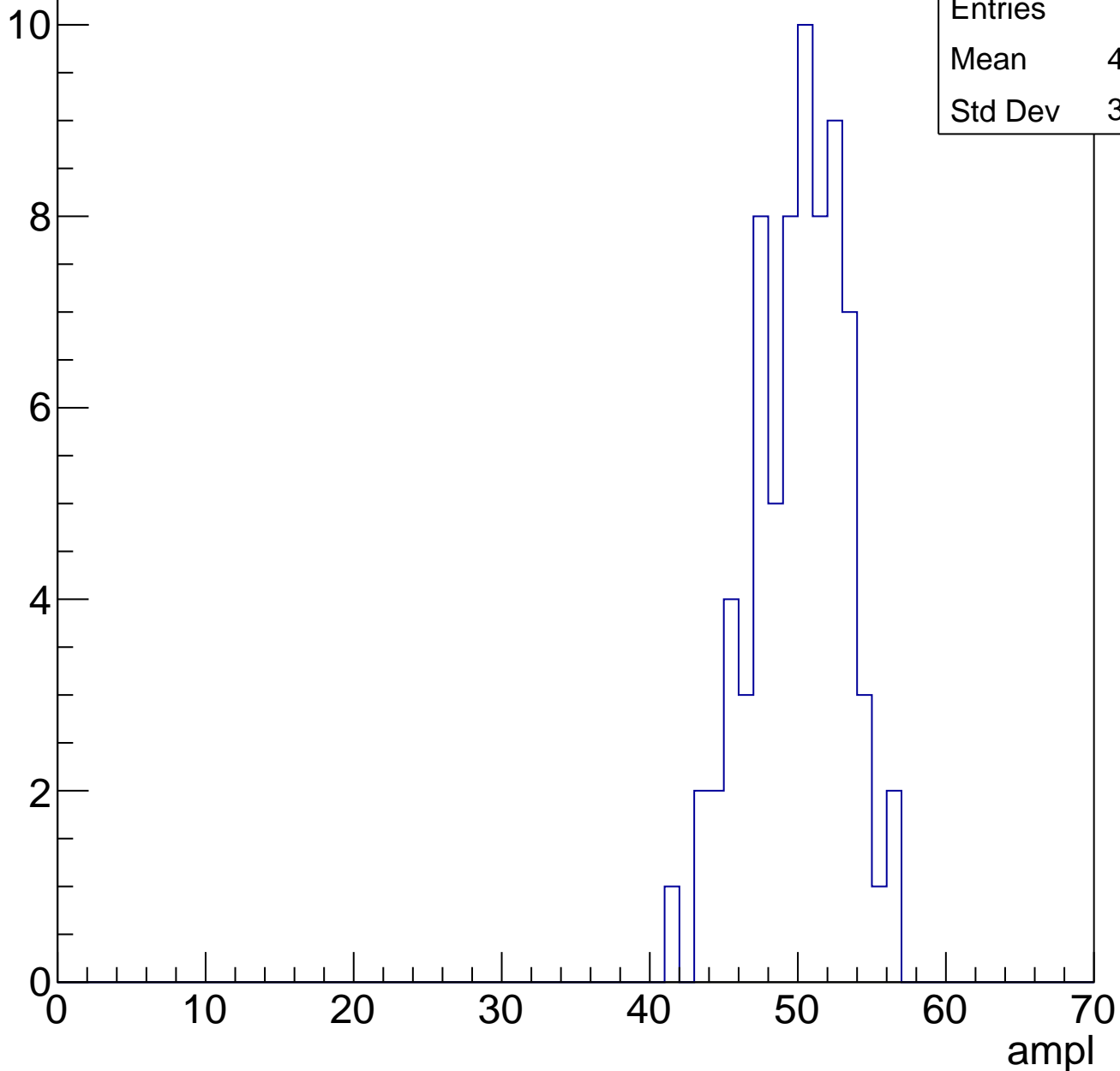


# B1L103S, U11-ch107, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	73
Mean	49.55
Std Dev	3.175

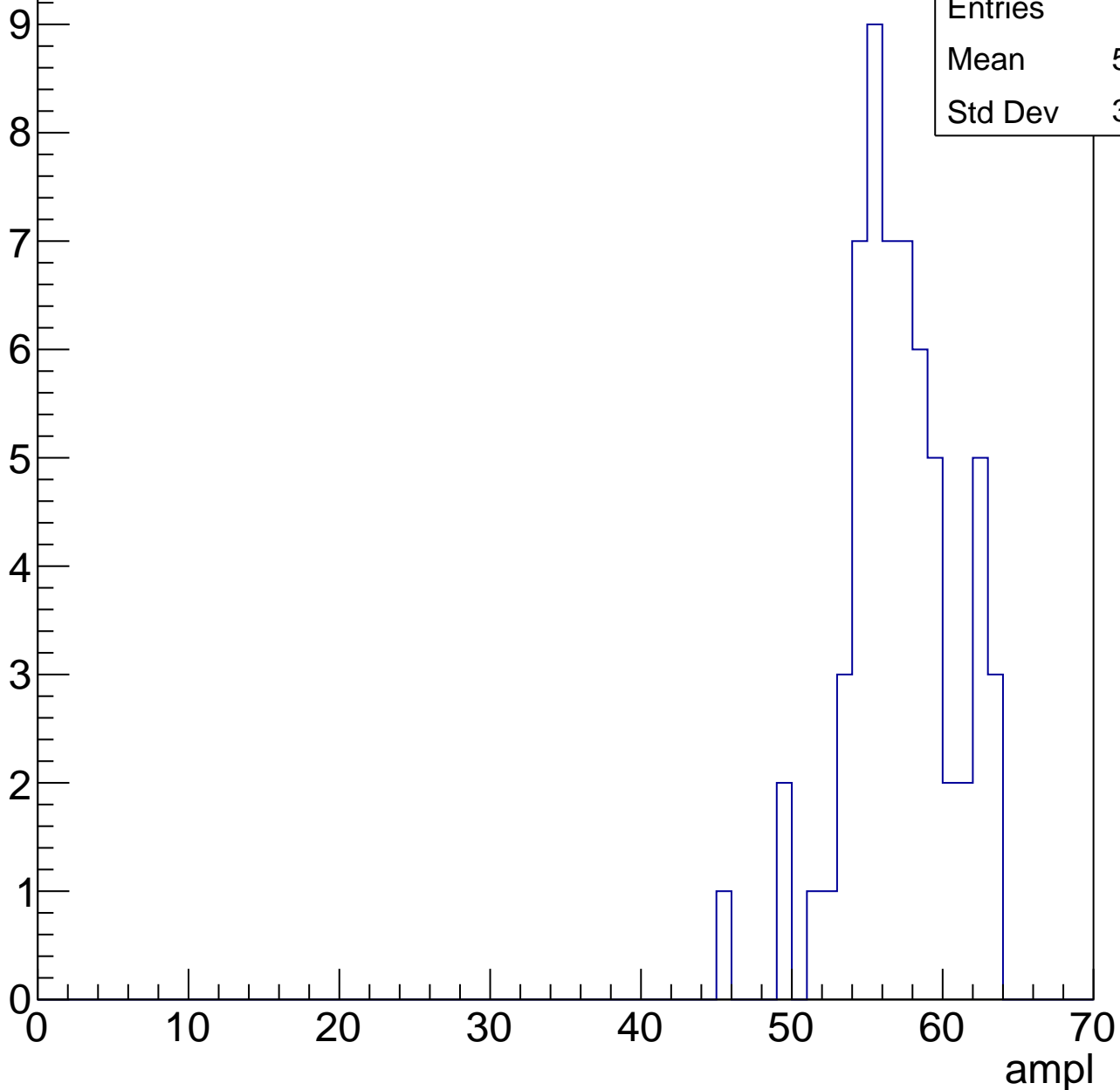


# B1L103S, U11-ch107, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	61
Mean	56.61
Std Dev	3.591

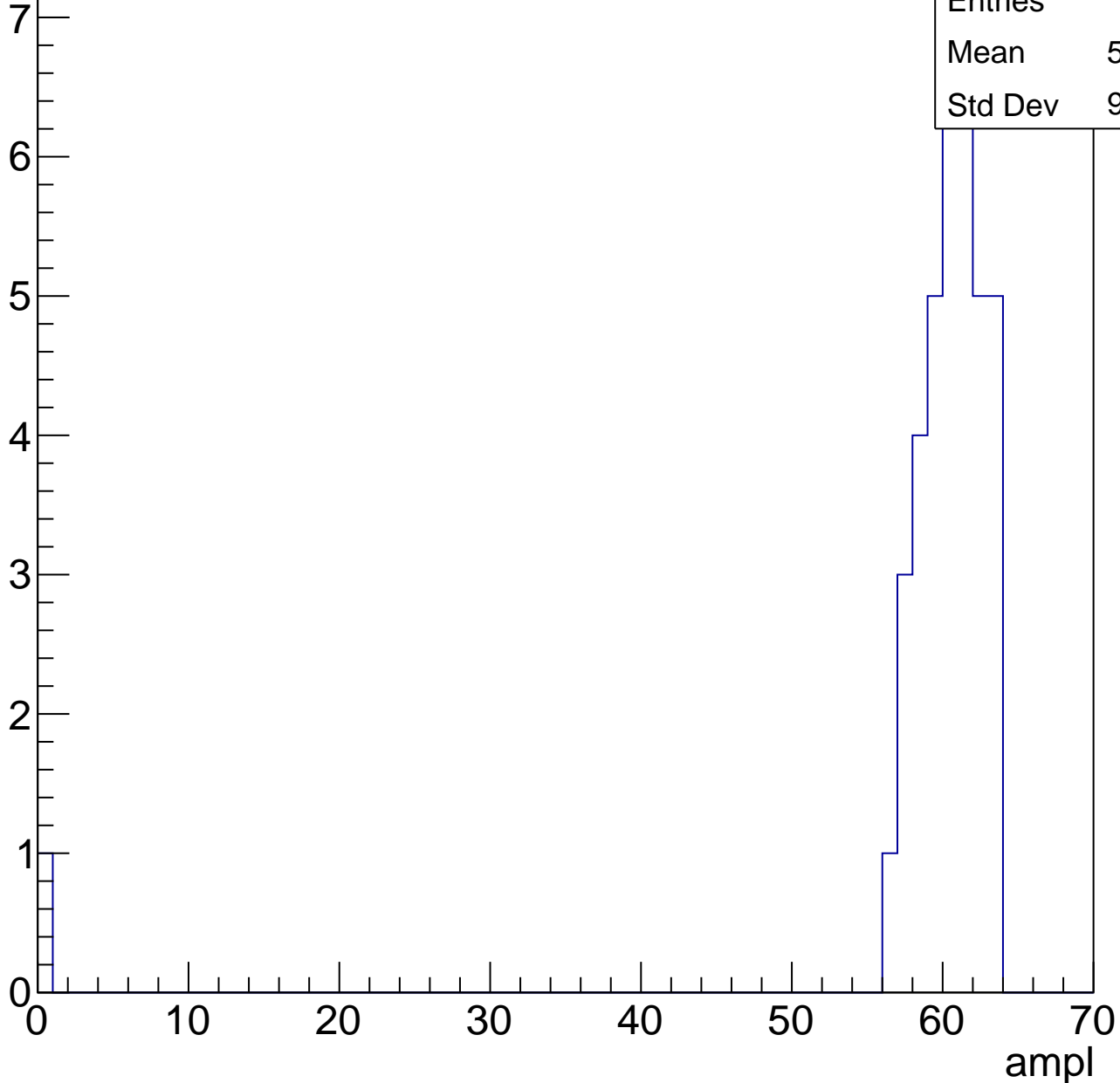


# B1L103S, U11-ch107, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	38
Mean	58.58
Std Dev	9.813



# B1L103S, U11-ch107, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U11-ch107, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U11-ch108, adc0

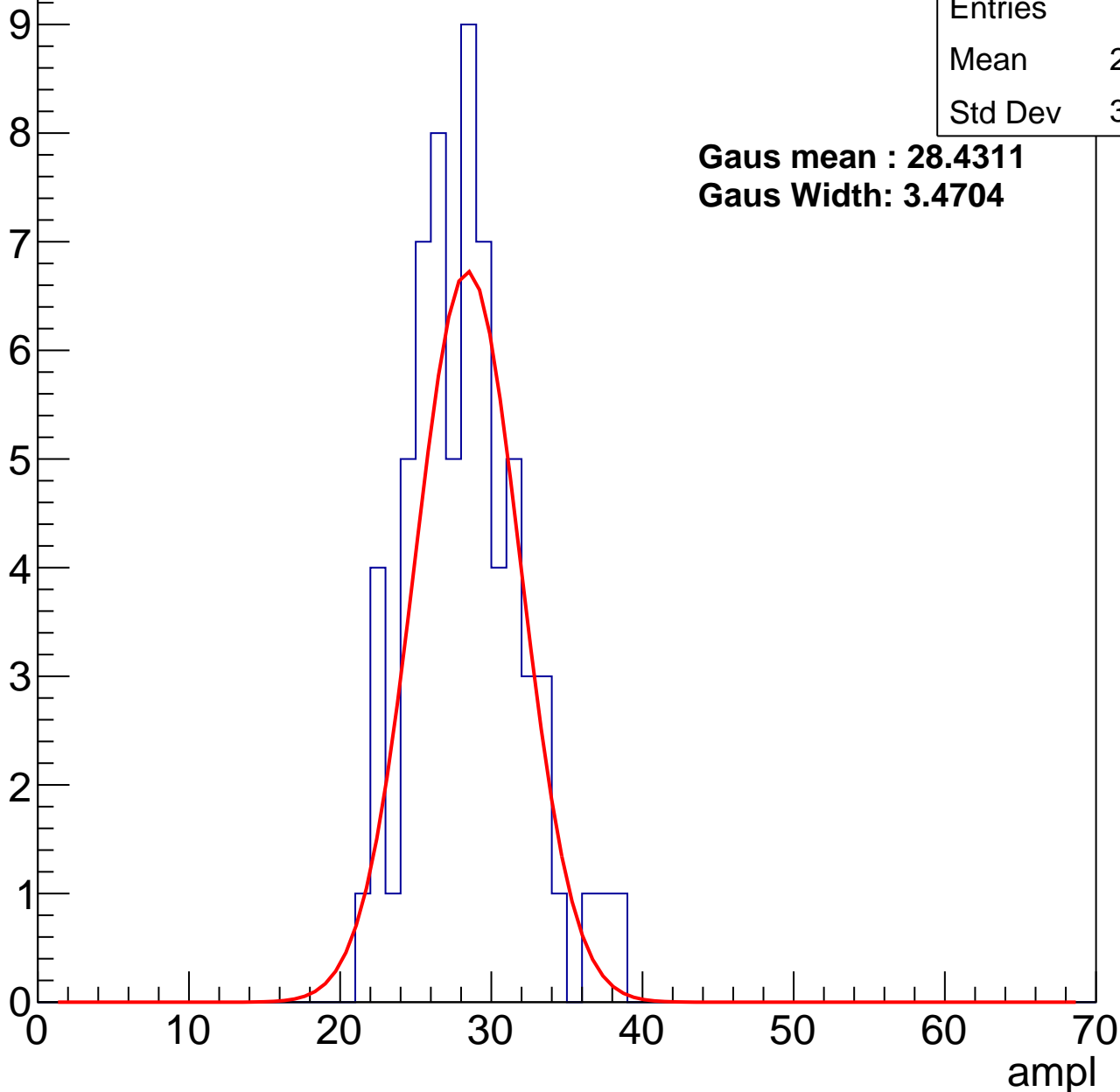
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	27.88
Std Dev	3.629

**Gaus mean : 28.4311**

**Gaus Width: 3.4704**



# B1L103S, U11-ch108, adc1

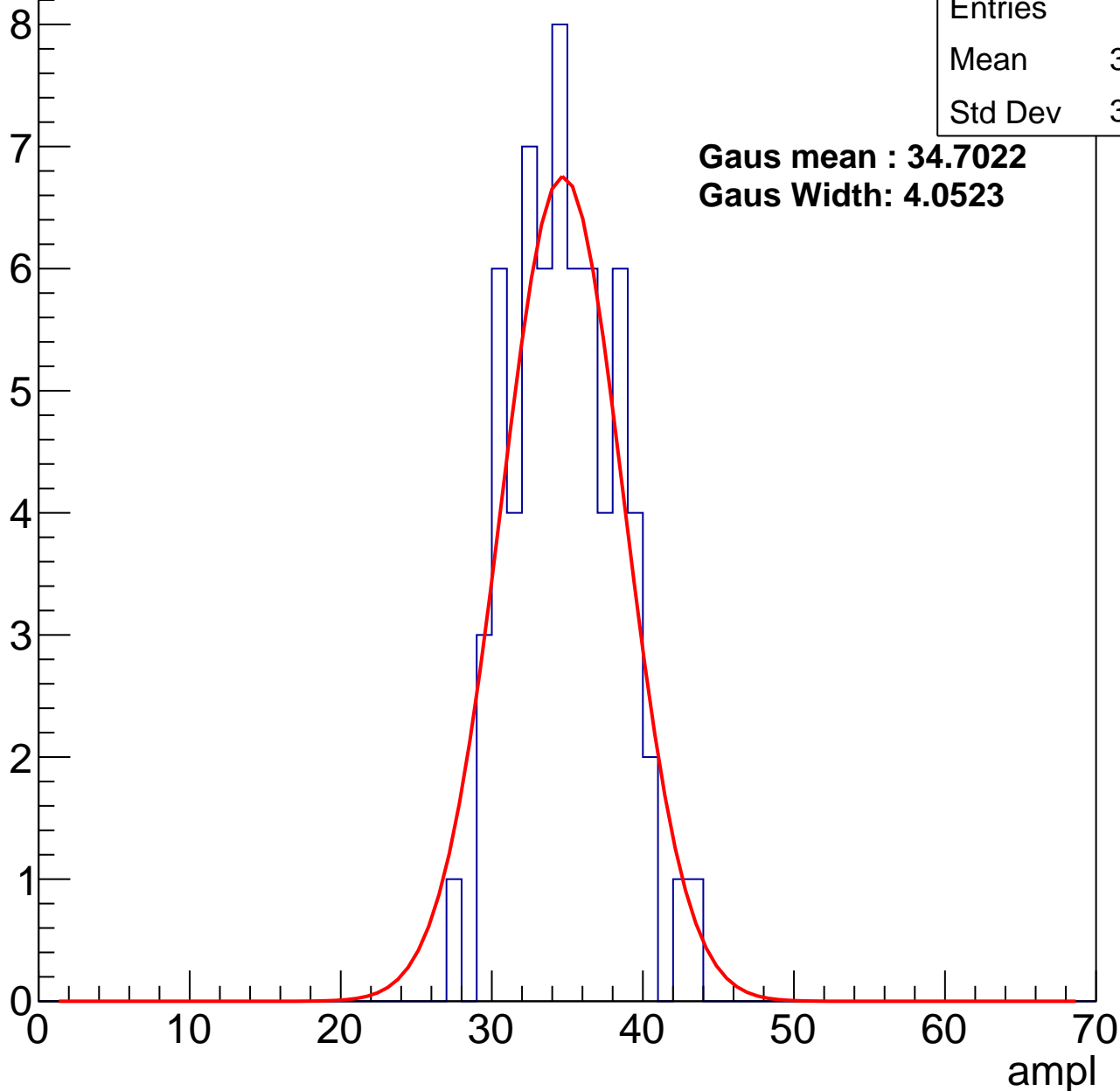
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	34.38
Std Dev	3.418

**Gaus mean : 34.7022**

**Gaus Width: 4.0523**



# B1L103S, U11-ch108, adc2

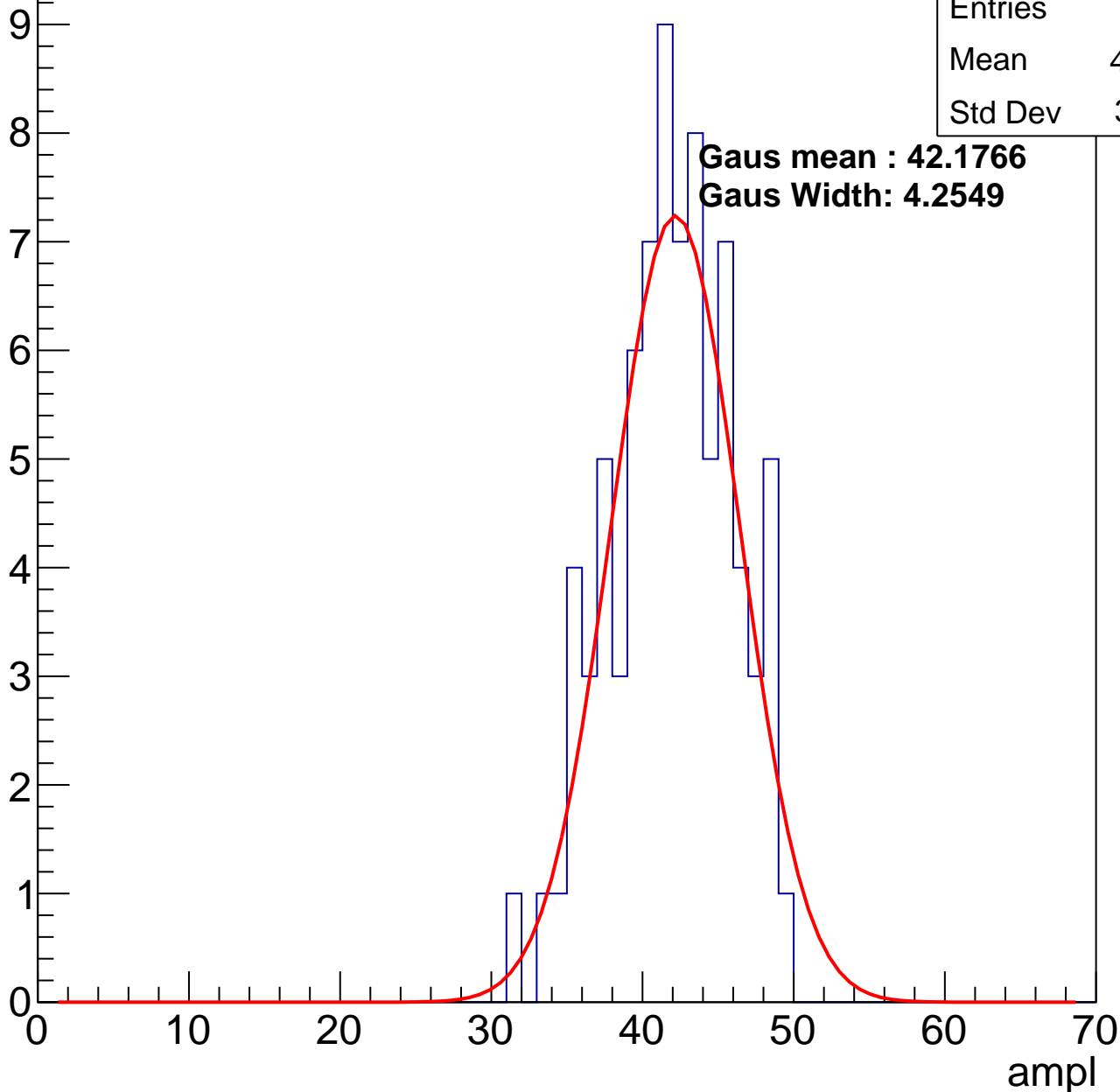
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	80
Mean	41.44
Std Dev	3.981

**Gaus mean : 42.1766**

**Gaus Width: 4.2549**

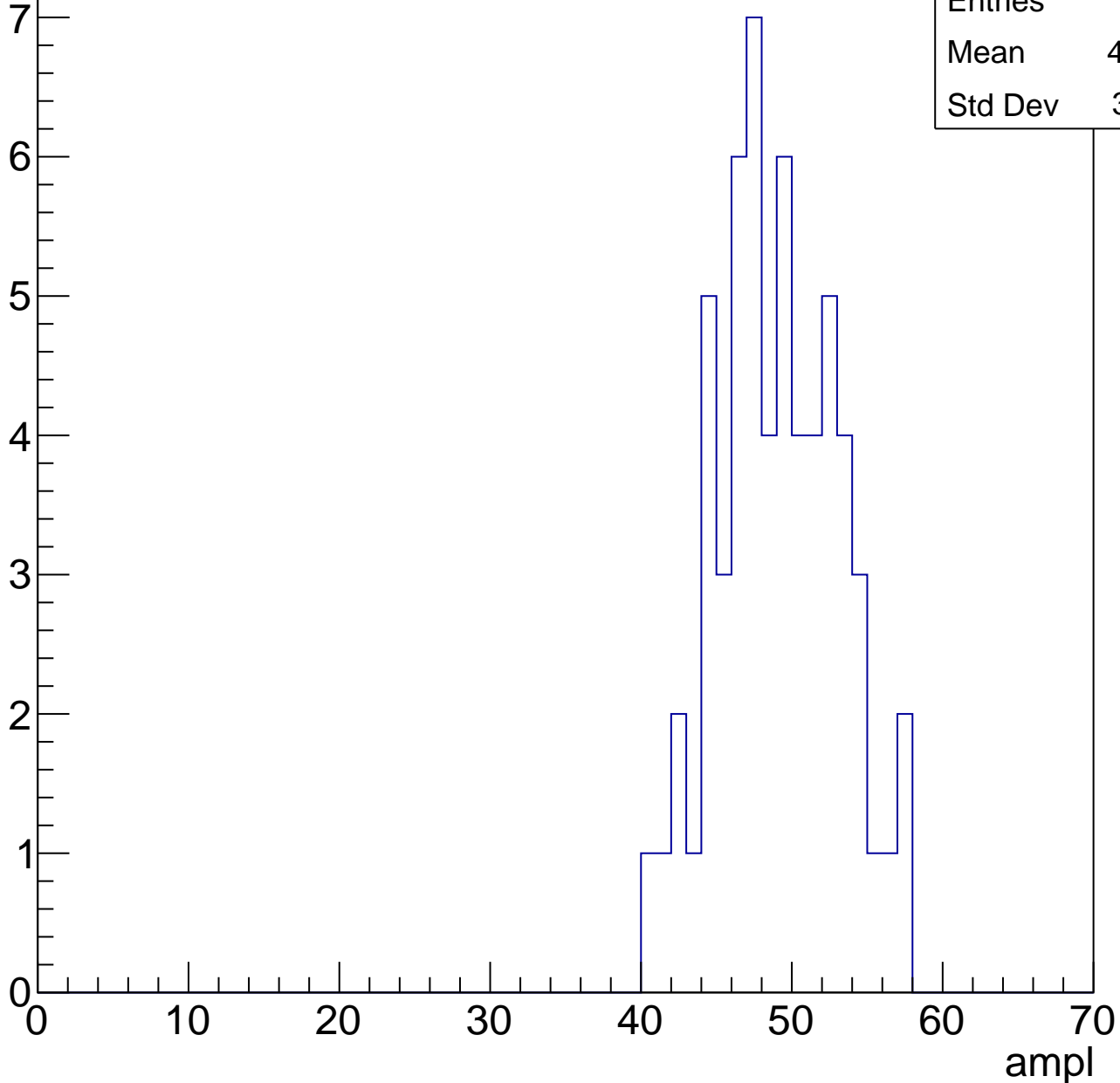


# B1L103S, U11-ch108, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	60
Mean	48.62
Std Dev	3.971

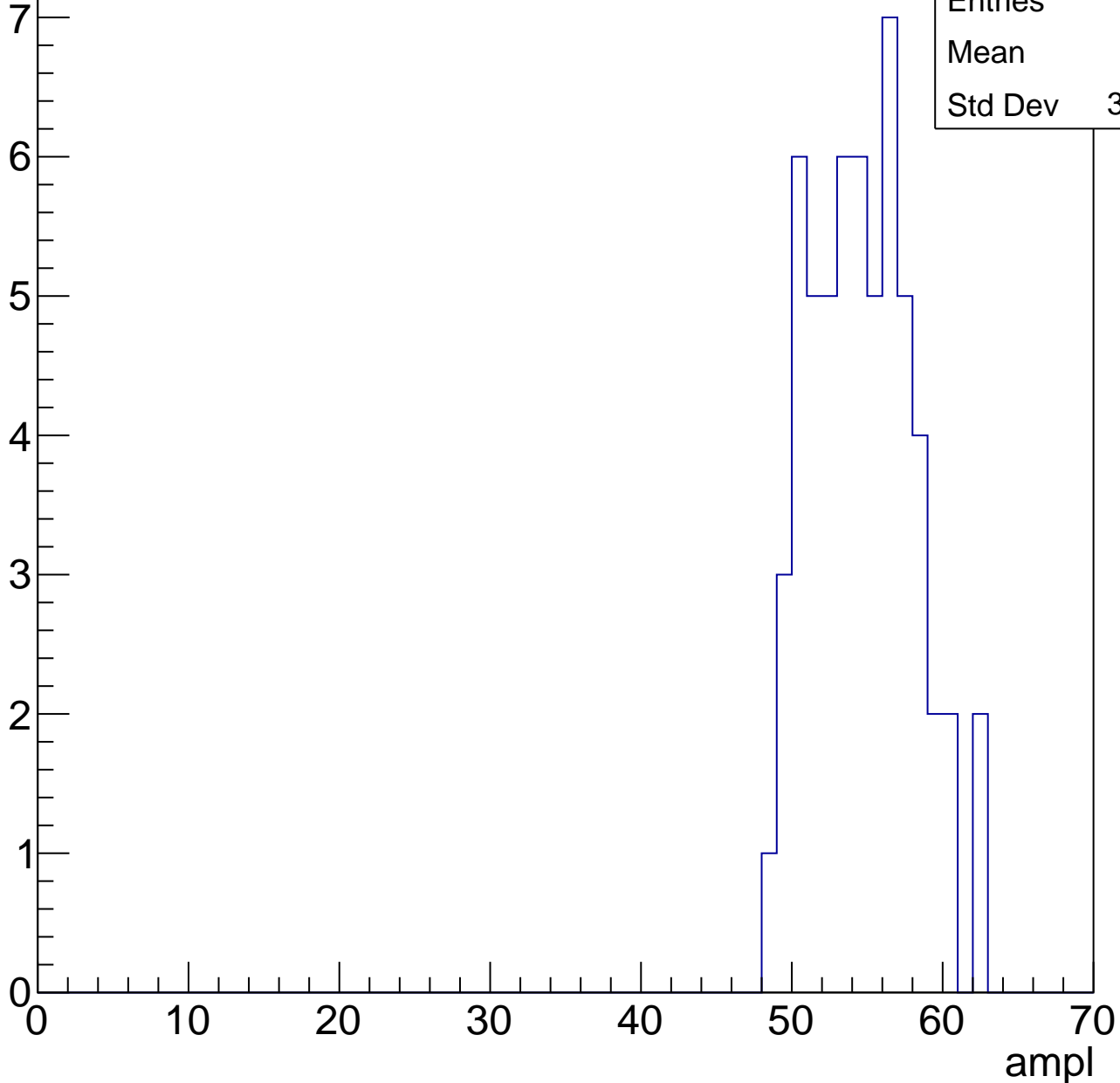


# B1L103S, U11-ch108, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	59
Mean	54.2
Std Dev	3.364

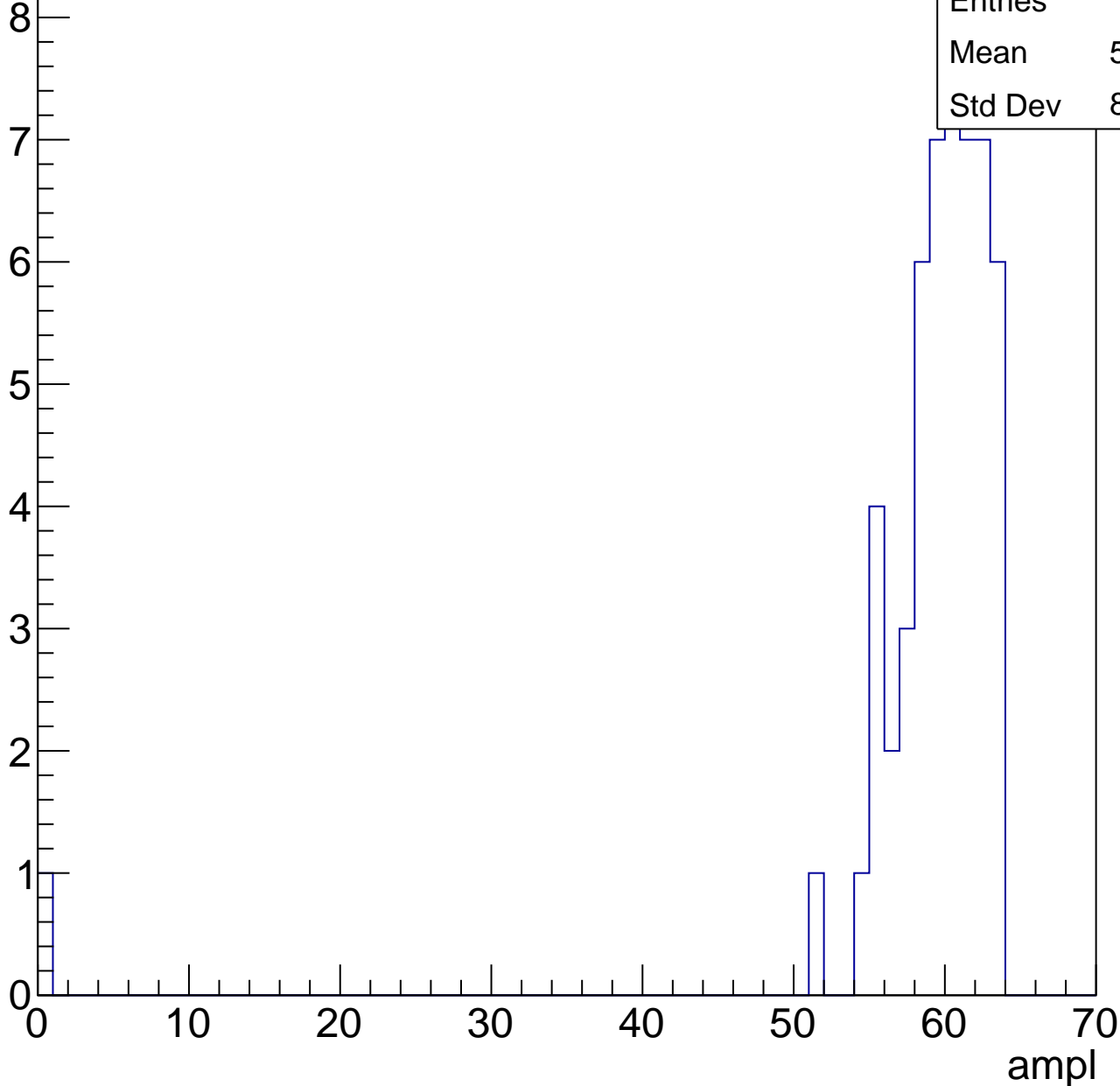


# B1L103S, U11-ch108, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

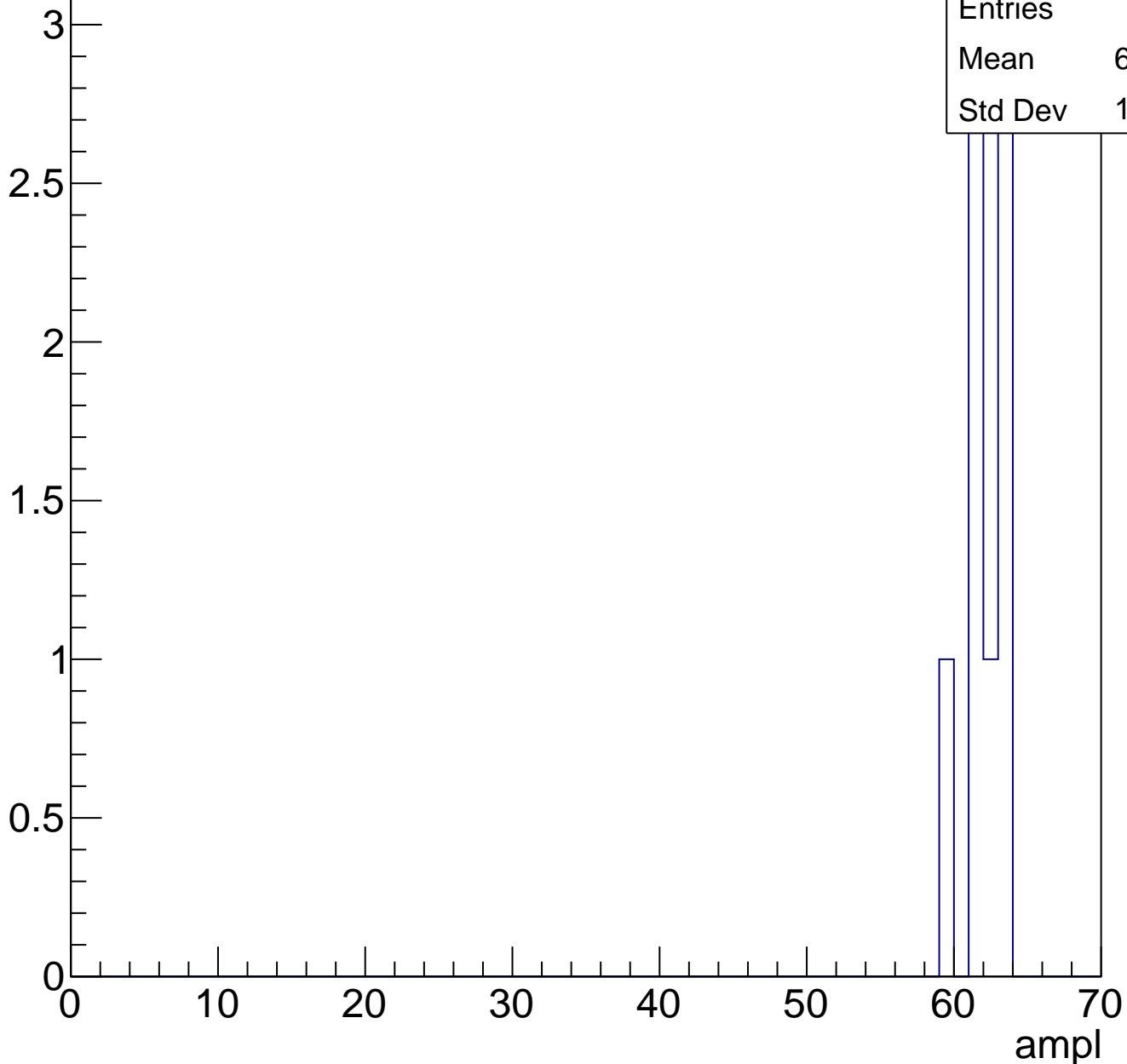
Entries	53
Mean	58.26
Std Dev	8.508



# B1L103S, U11-ch108, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

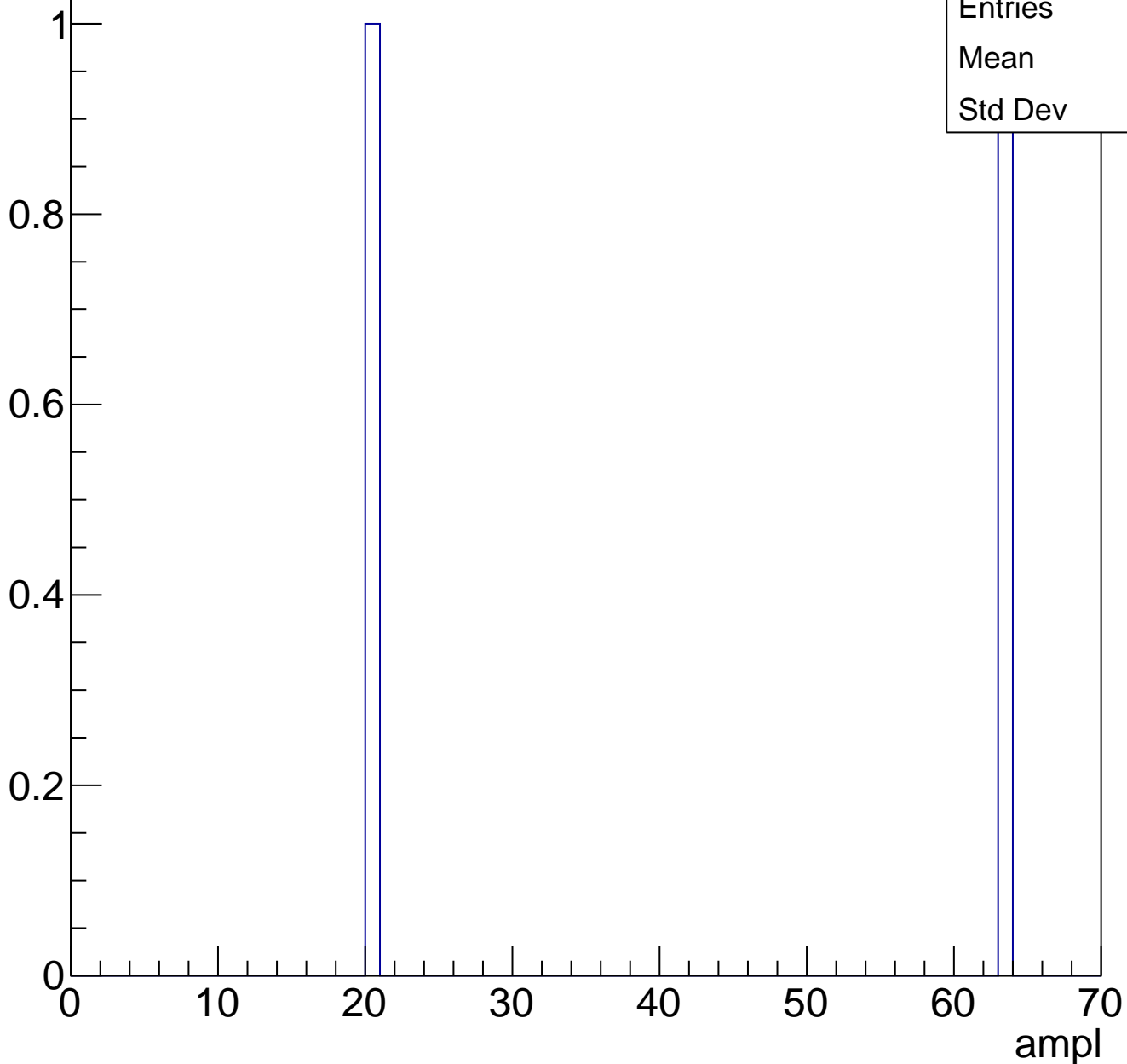




# B1L103S, U11-ch108, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	2
Mean	41.5
Std Dev	21.5

# B1L103S, U11-ch109, adc0

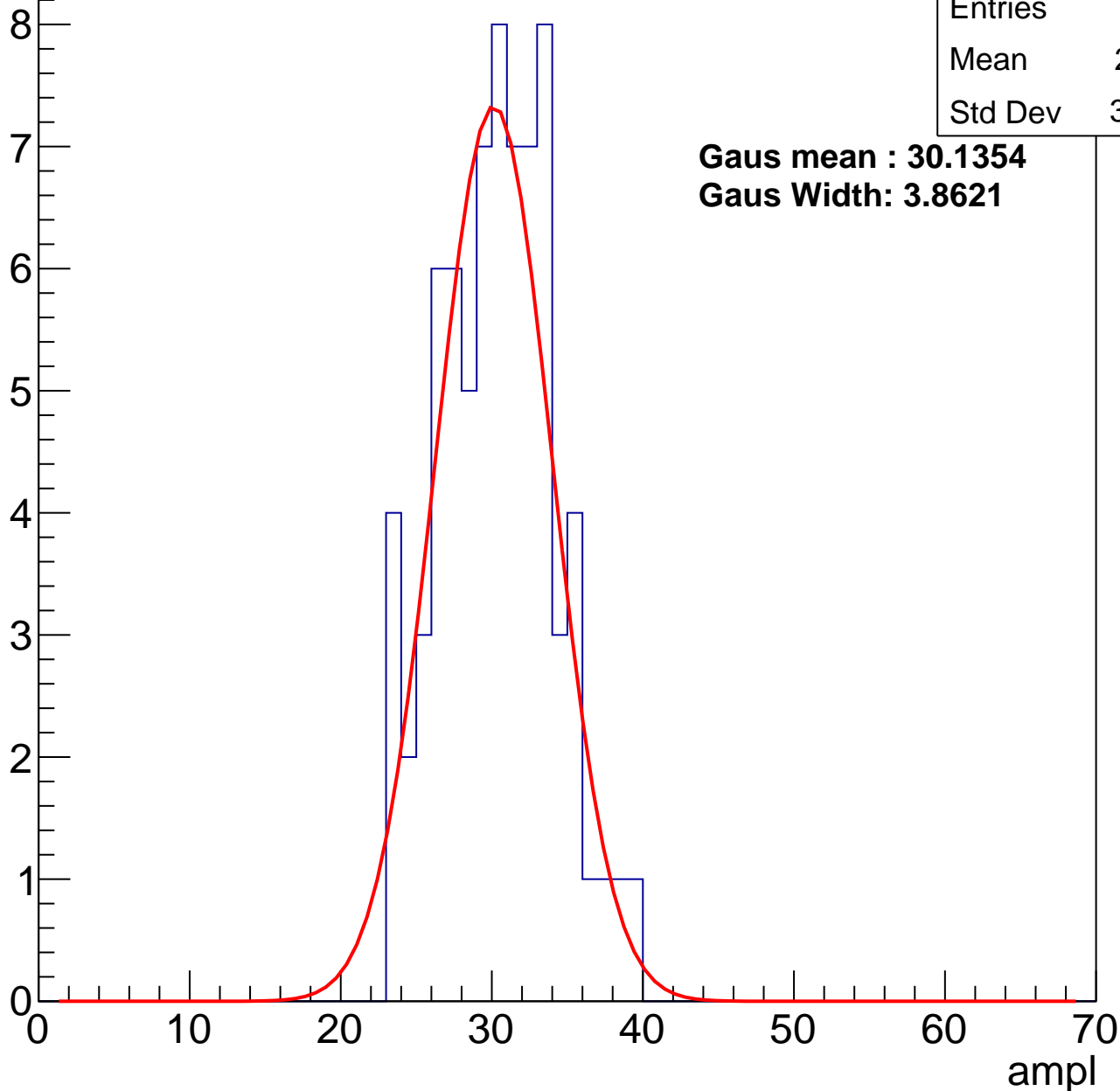
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	74
Mean	29.91
Std Dev	3.684

**Gaus mean : 30.1354**

**Gaus Width: 3.8621**



# B1L103S, U11-ch109, adc1

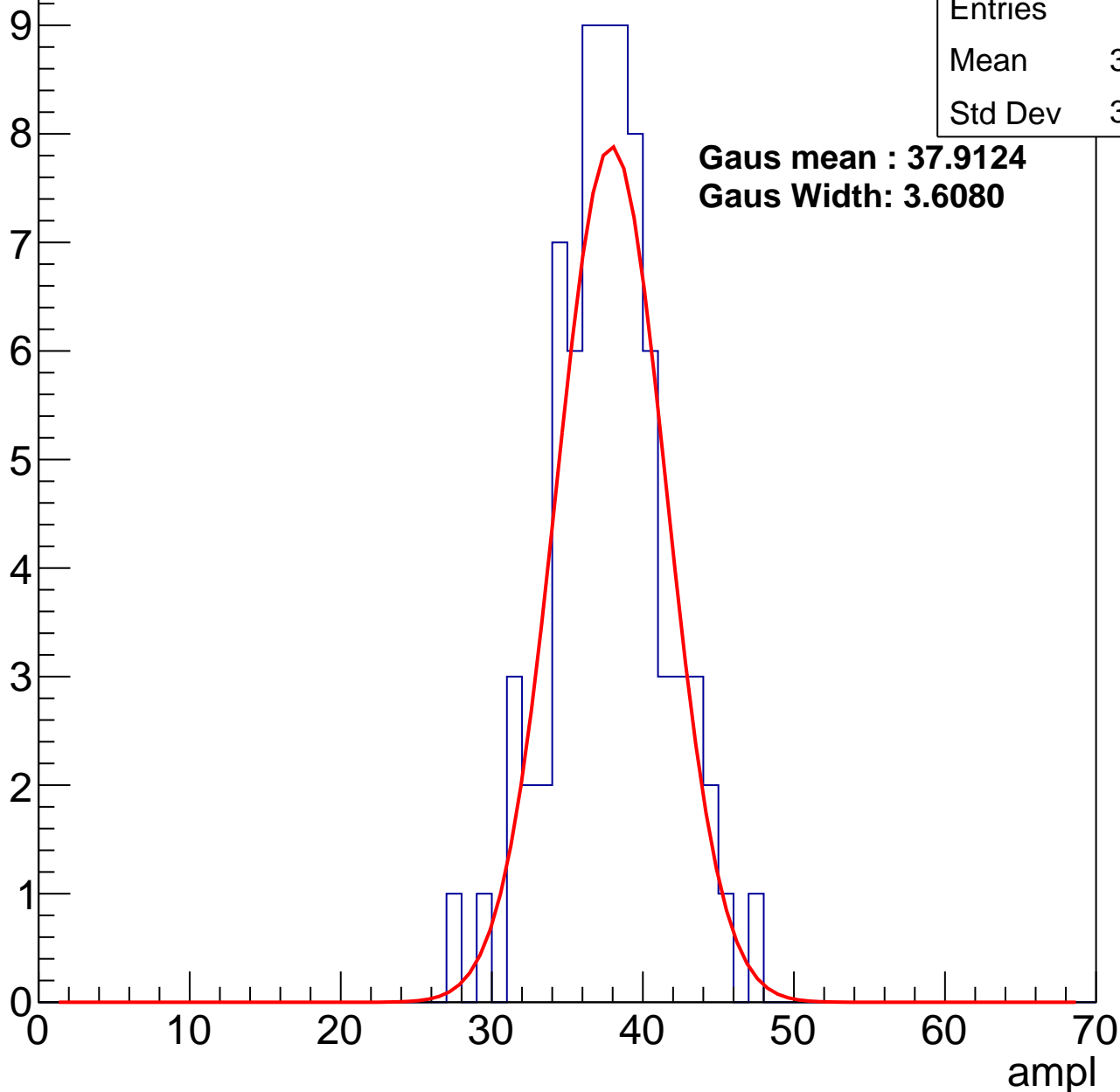
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	76
Mean	37.32
Std Dev	3.682

**Gaus mean : 37.9124**

**Gaus Width: 3.6080**



# B1L103S, U11-ch109, adc2

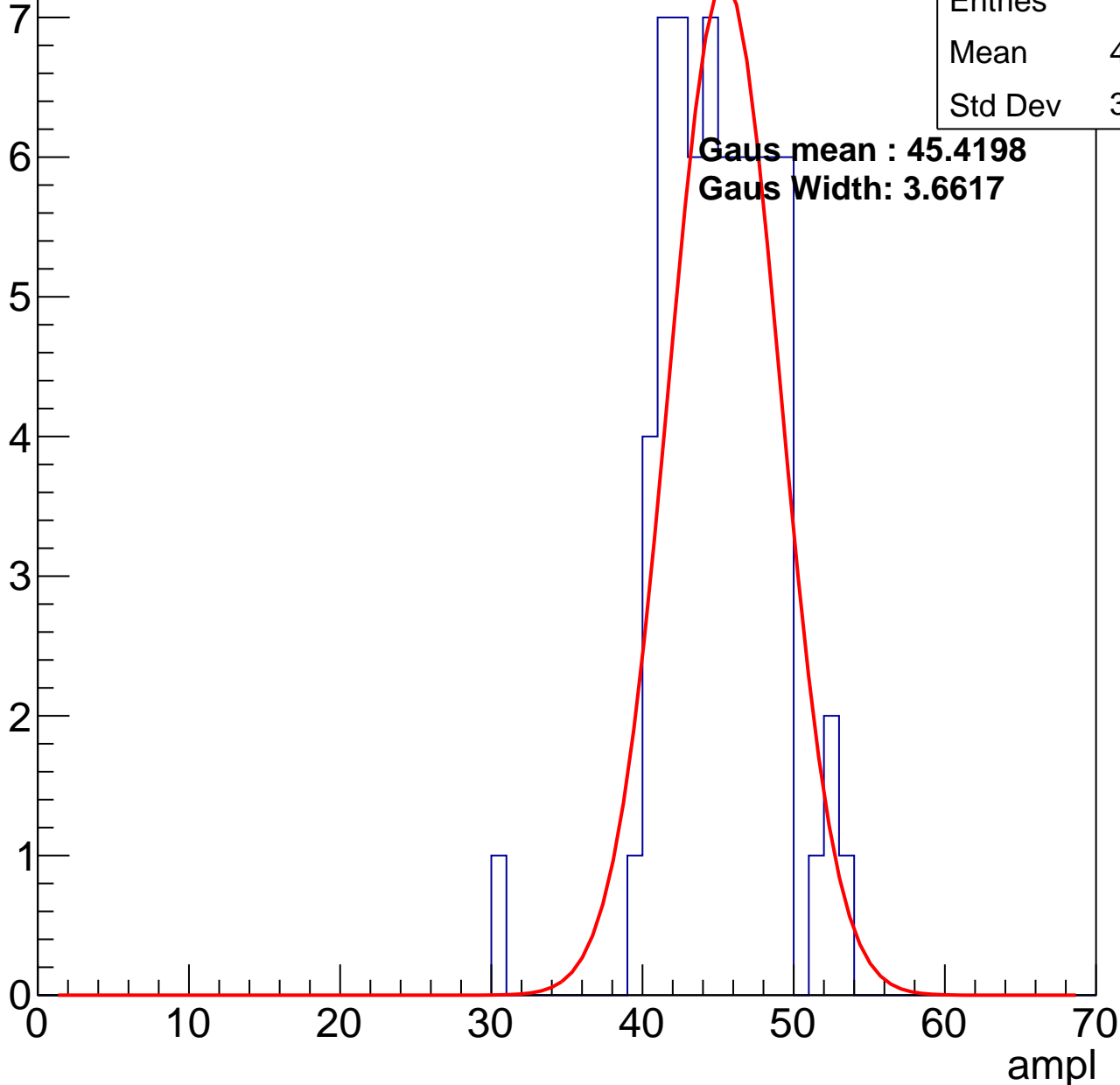
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	44.69
Std Dev	3.742

Gaus mean : 45.4198

Gaus Width: 3.6617

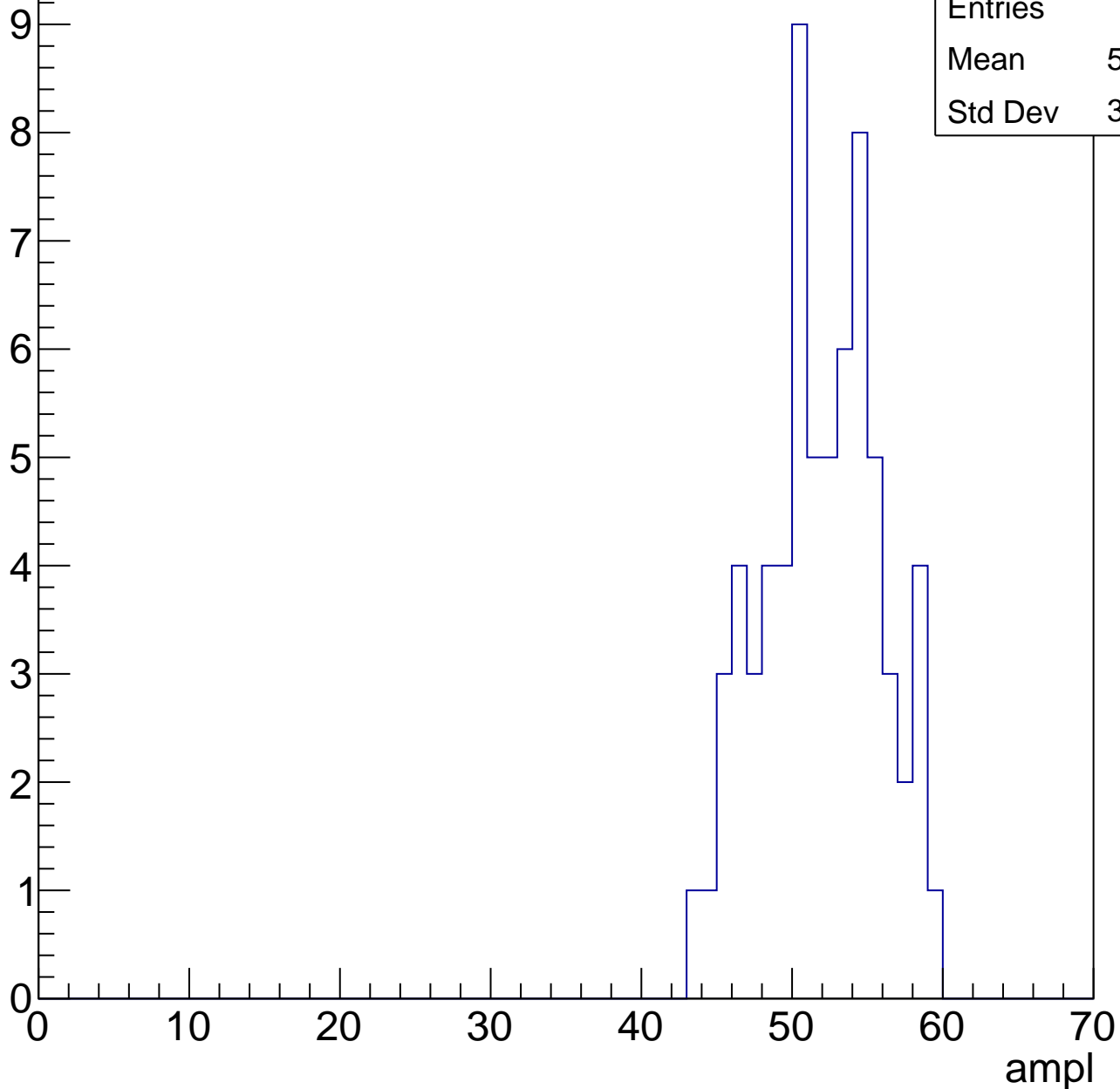


# B1L103S, U11-ch109, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	68
Mean	51.44
Std Dev	3.844

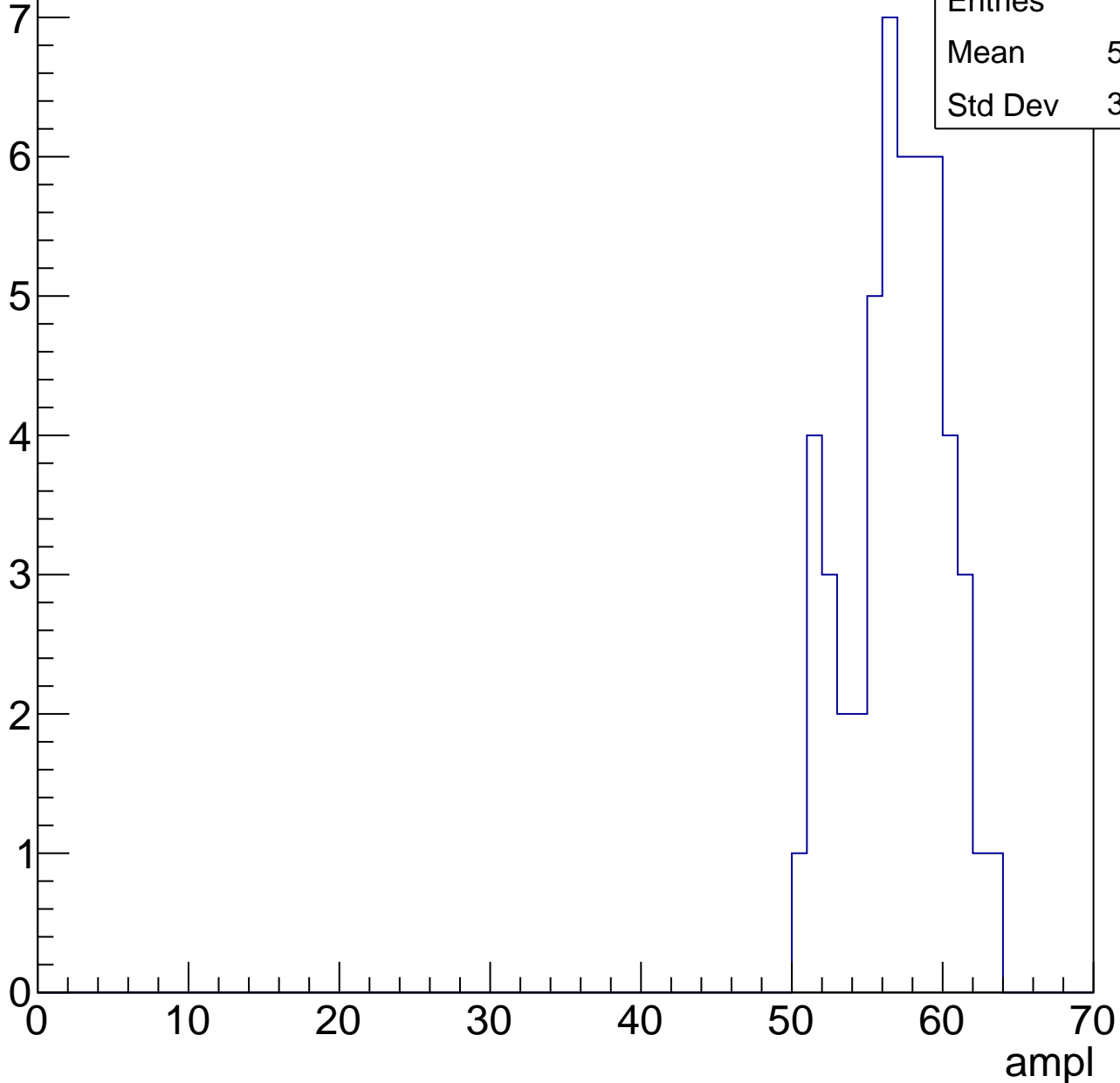


# B1L103S, U11-ch109, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	51
Mean	56.53
Std Dev	3.158

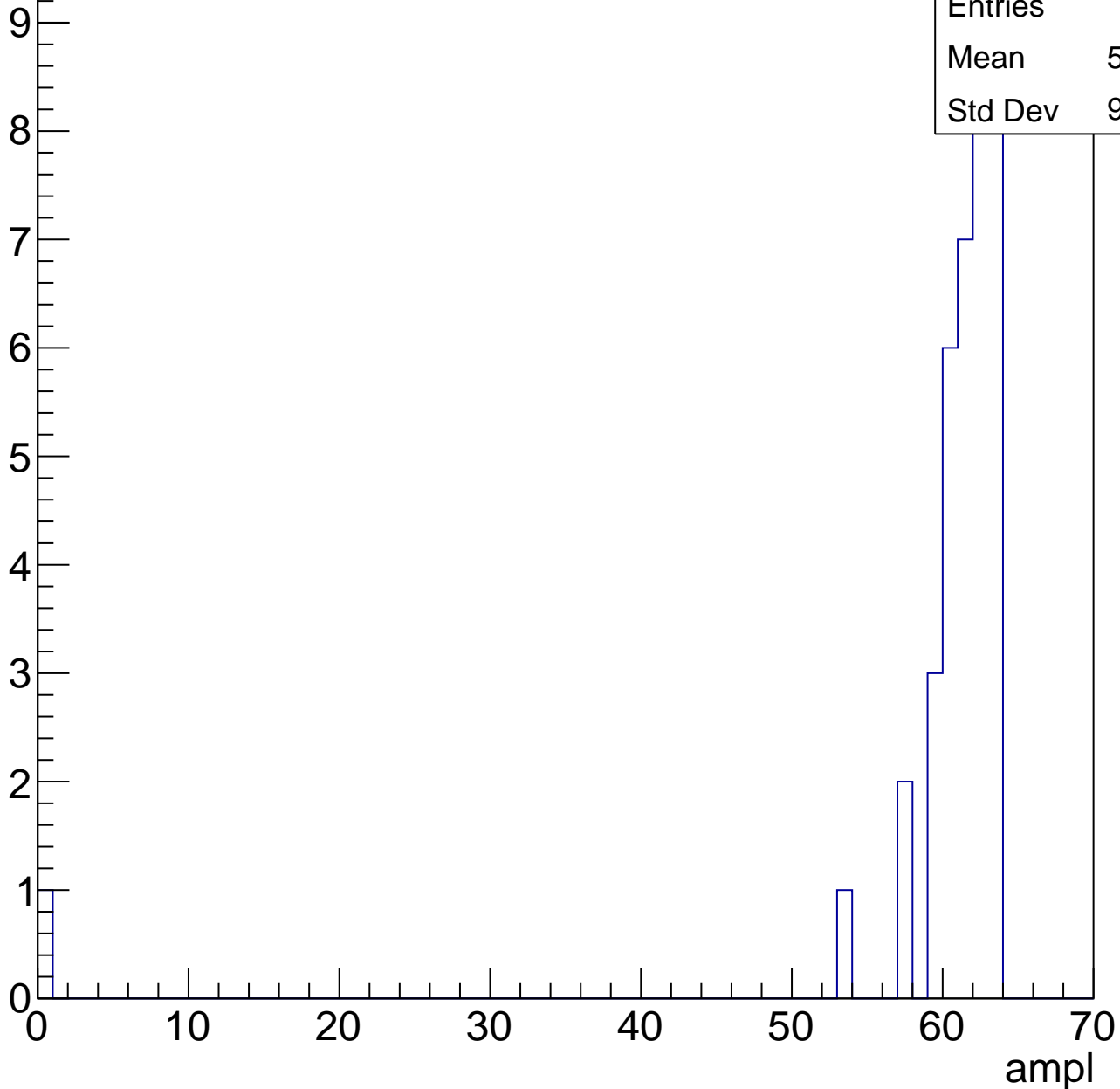


# B1L103S, U11-ch109, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	38
Mean	59.37
Std Dev	9.972



# B1L103S, U11-ch109, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0



# B1L103S, U11-ch109, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L103S, U11-ch110, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	89
Mean	30.38
Std Dev	5.46

**Gaus mean : 31.6586**

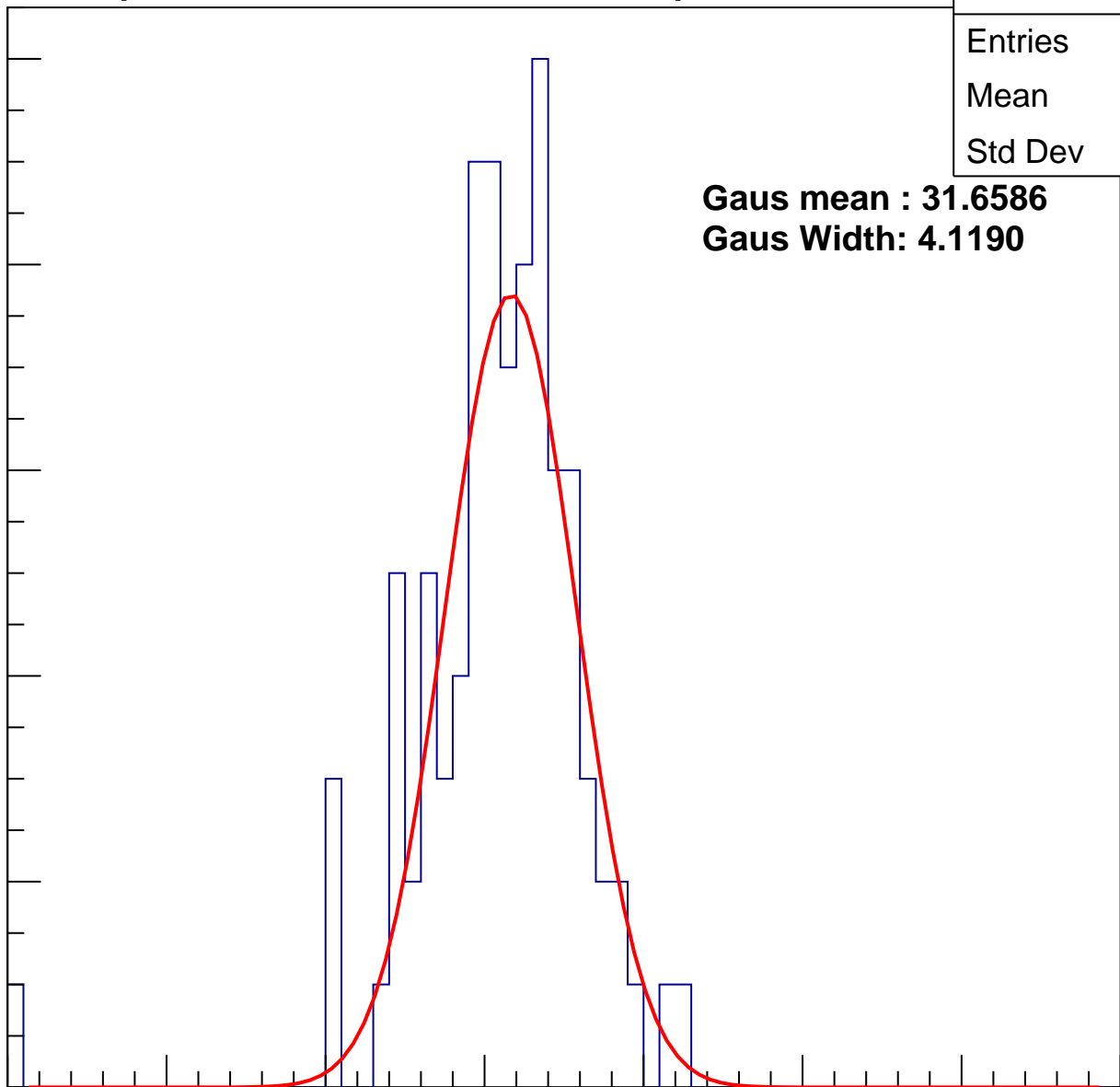
**Gaus Width: 4.1190**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U11-ch110, adc1

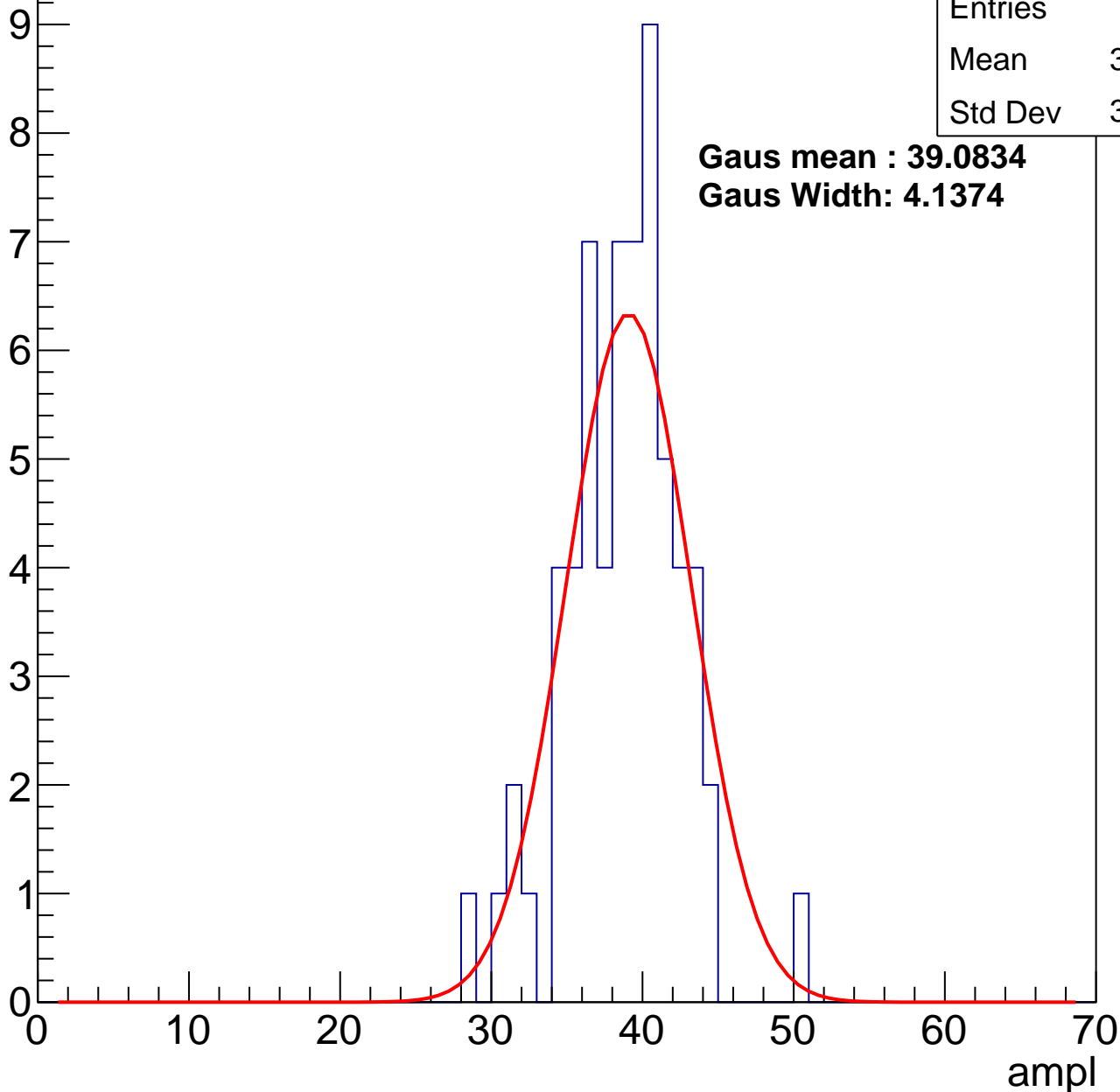
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	38.25
Std Dev	3.767

**Gaus mean : 39.0834**

**Gaus Width: 4.1374**



# B1L103S, U11-ch110, adc2

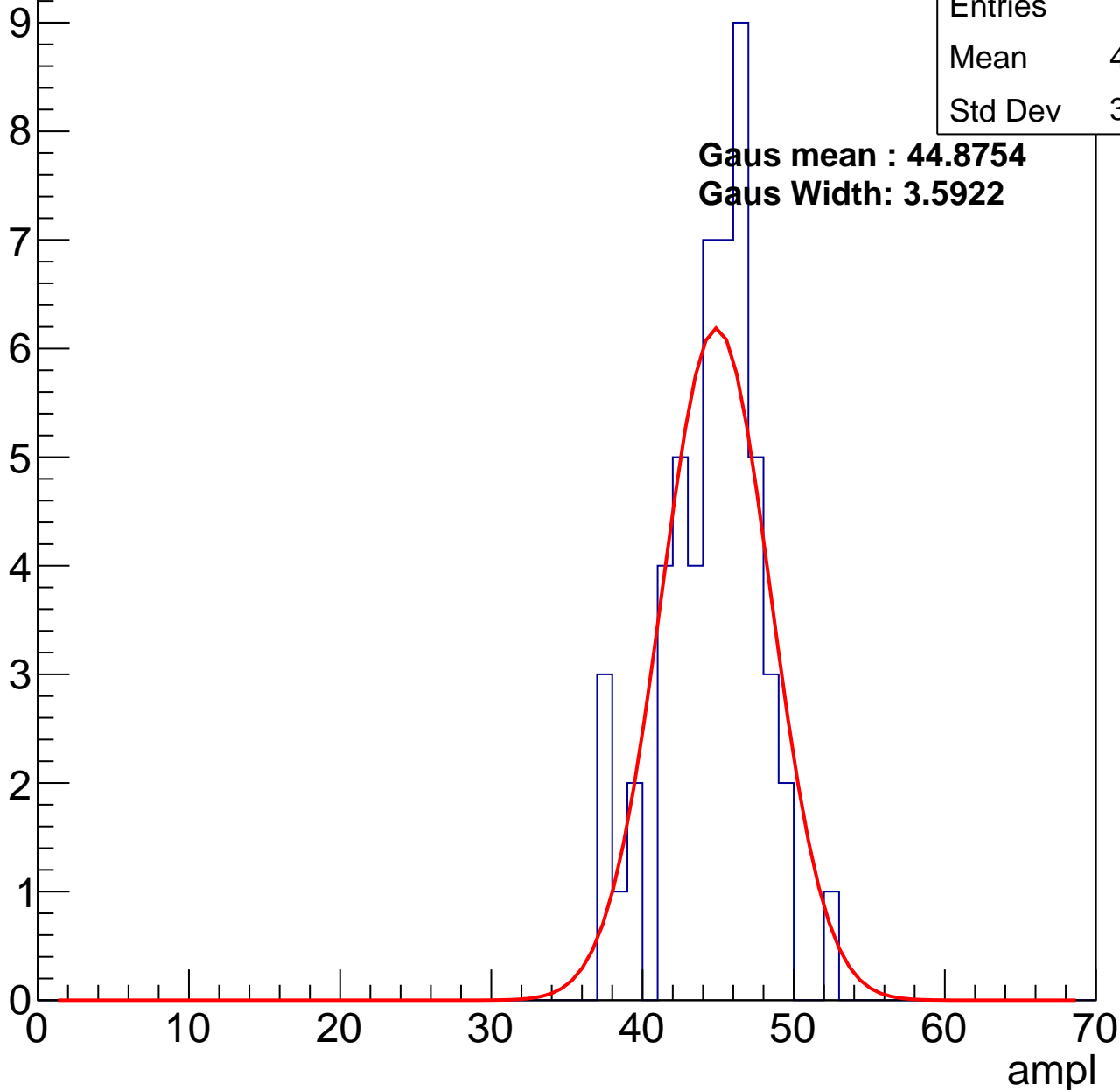
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	53
Mean	44.13
Std Dev	3.198

**Gaus mean : 44.8754**

**Gaus Width: 3.5922**

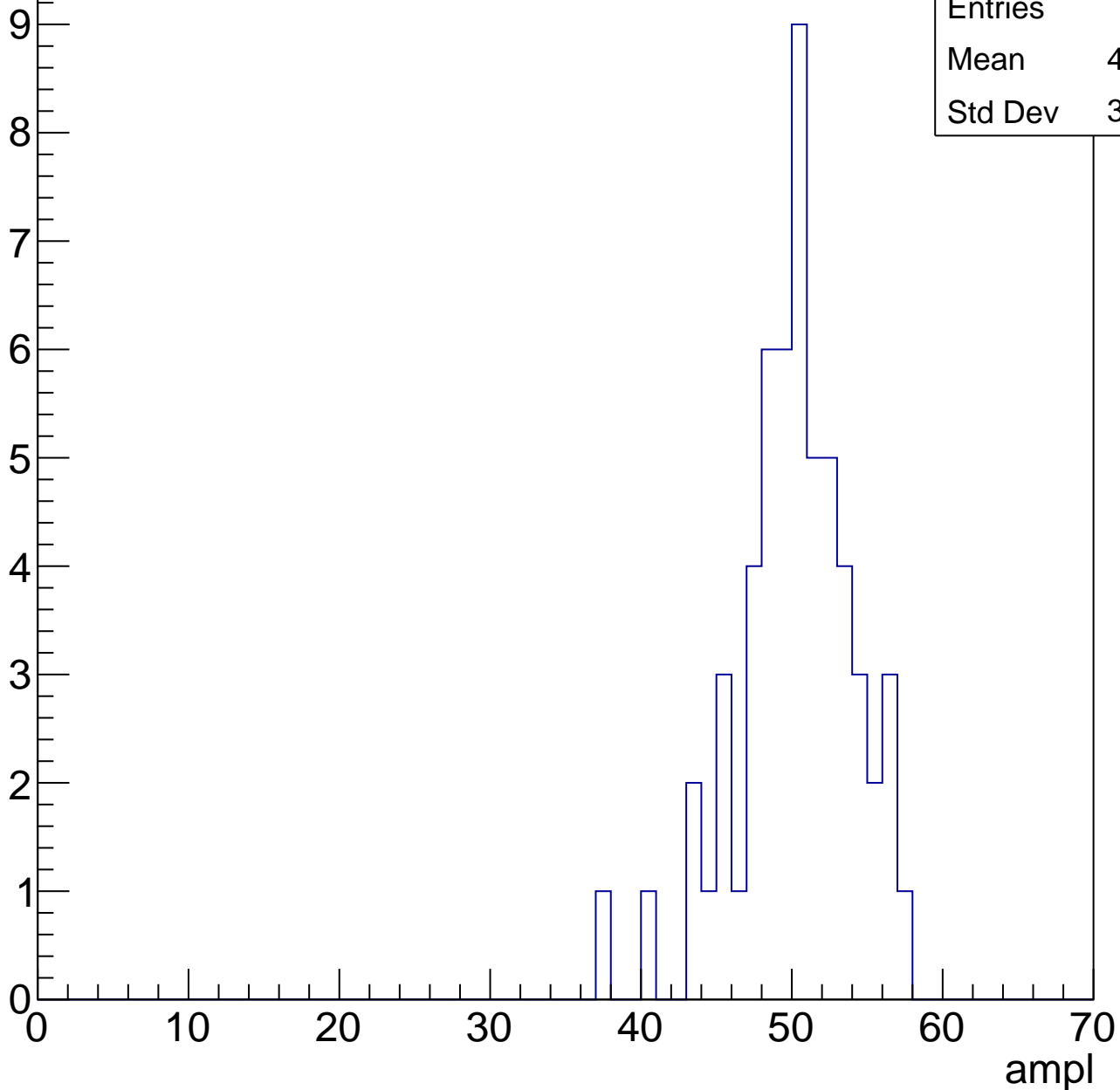


# B1L103S, U11-ch110, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	57
Mean	49.68
Std Dev	3.908

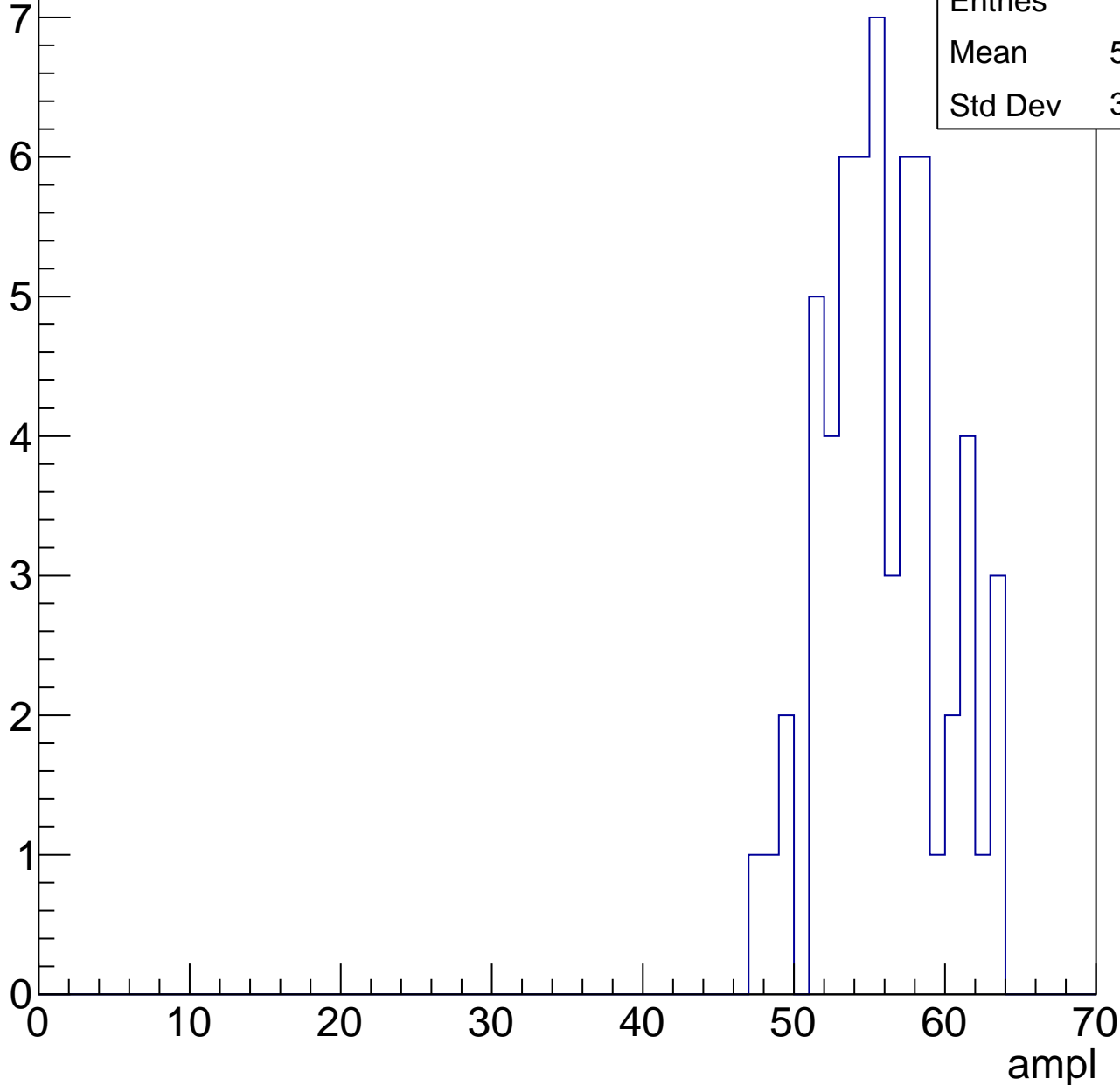


# B1L103S, U11-ch110, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	58
Mean	55.43
Std Dev	3.833

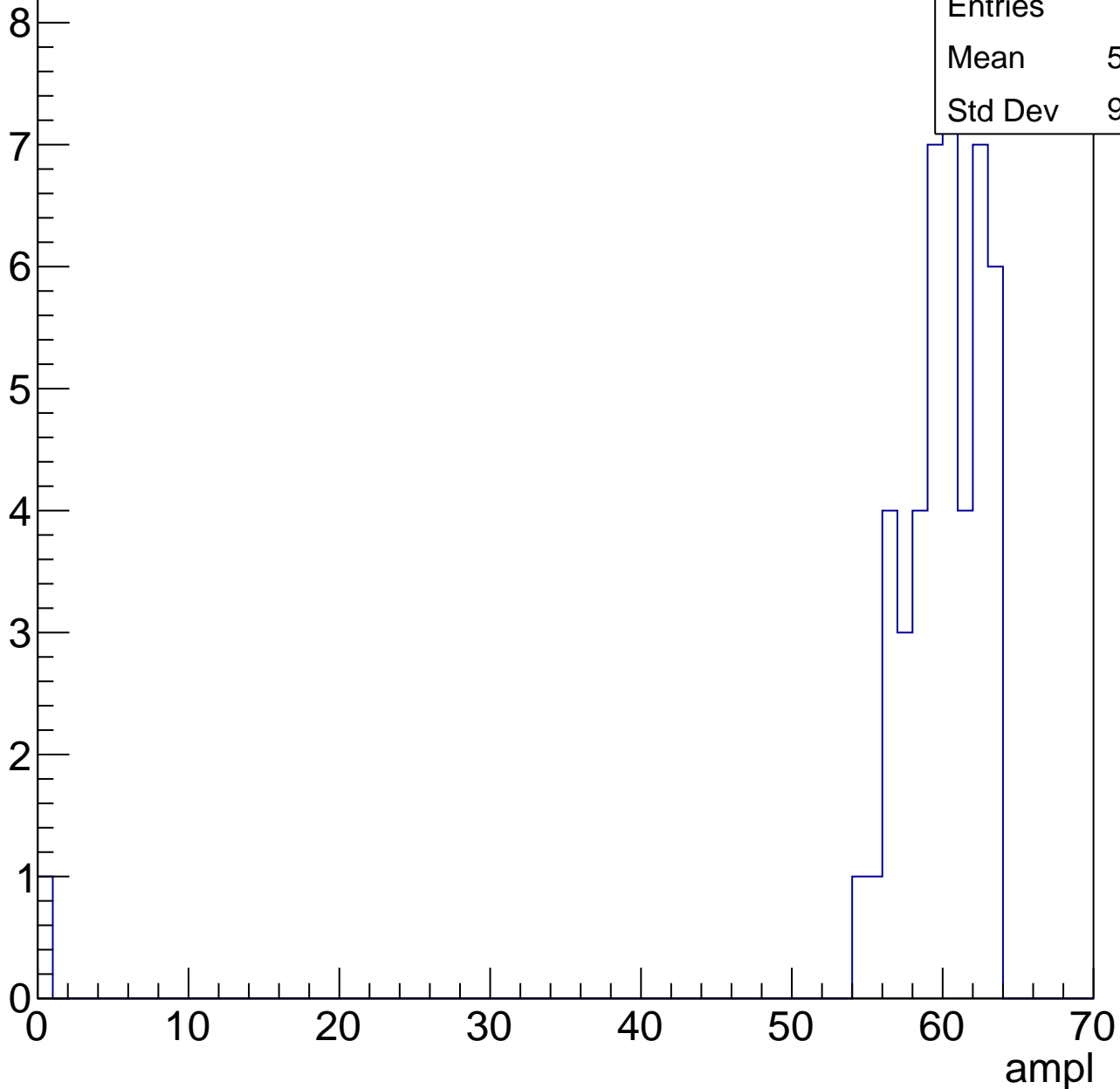


# B1L103S, U11-ch110, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	46
Mean	58.37
Std Dev	9.015



# B1L103S, U11-ch110, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

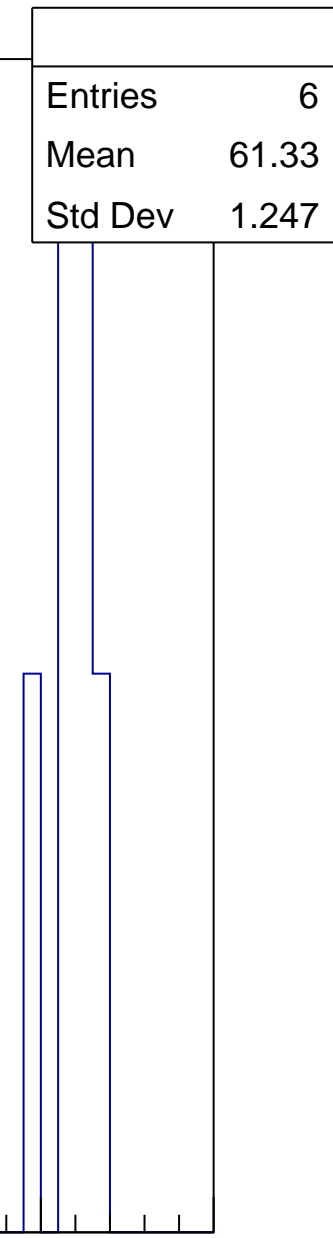
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	6
Mean	61.33
Std Dev	1.247

0 10 20 30 40 50 60 70

ampl

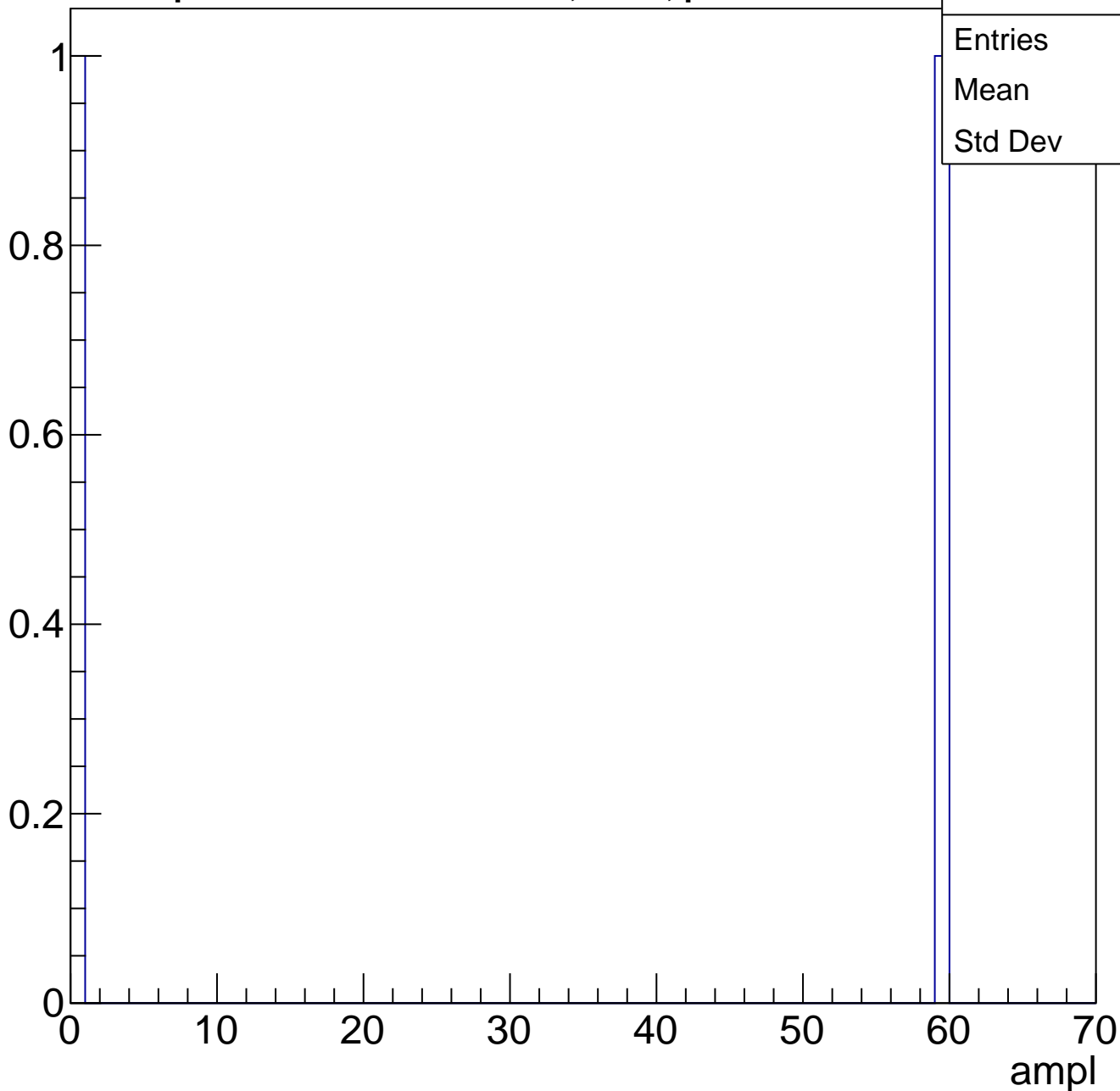




# B1L103S, U11-ch110, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U11-ch111, adc0

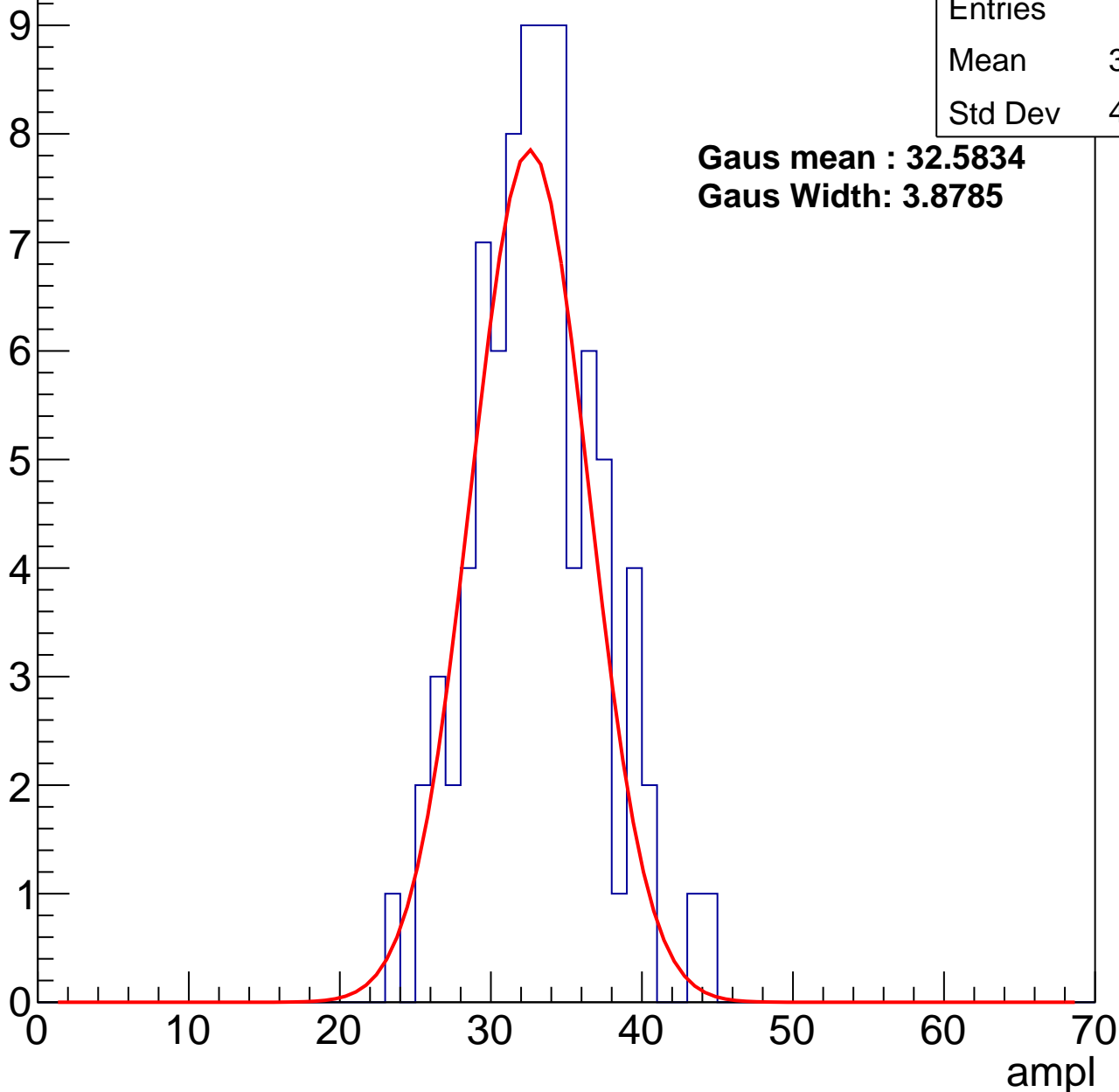
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	84
Mean	32.63
Std Dev	4.067

**Gaus mean : 32.5834**

**Gaus Width: 3.8785**



# B1L103S, U11-ch111, adc1

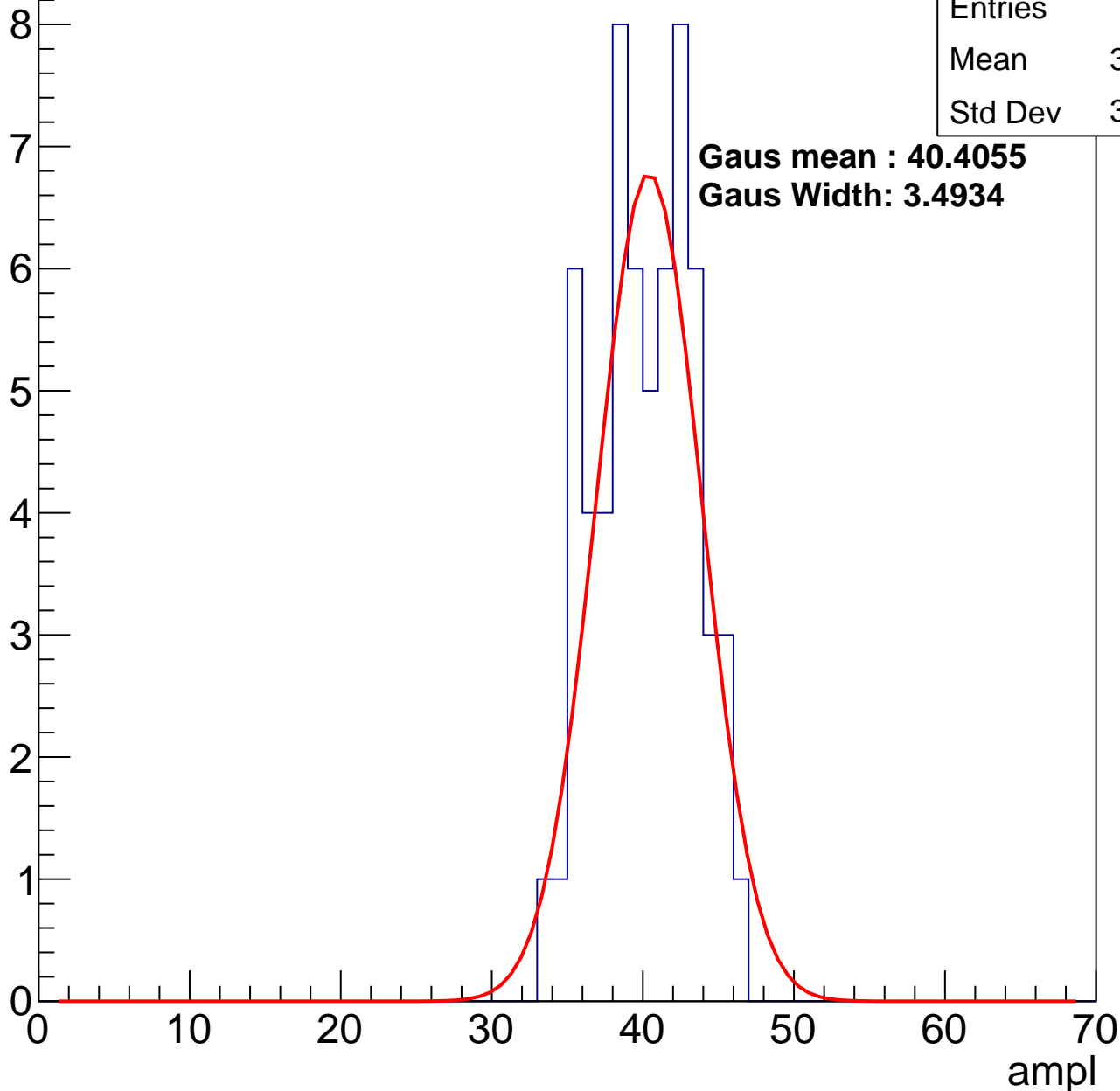
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	39.68
Std Dev	3.156

**Gaus mean : 40.4055**

**Gaus Width: 3.4934**



# B1L103S, U11-ch111, adc2

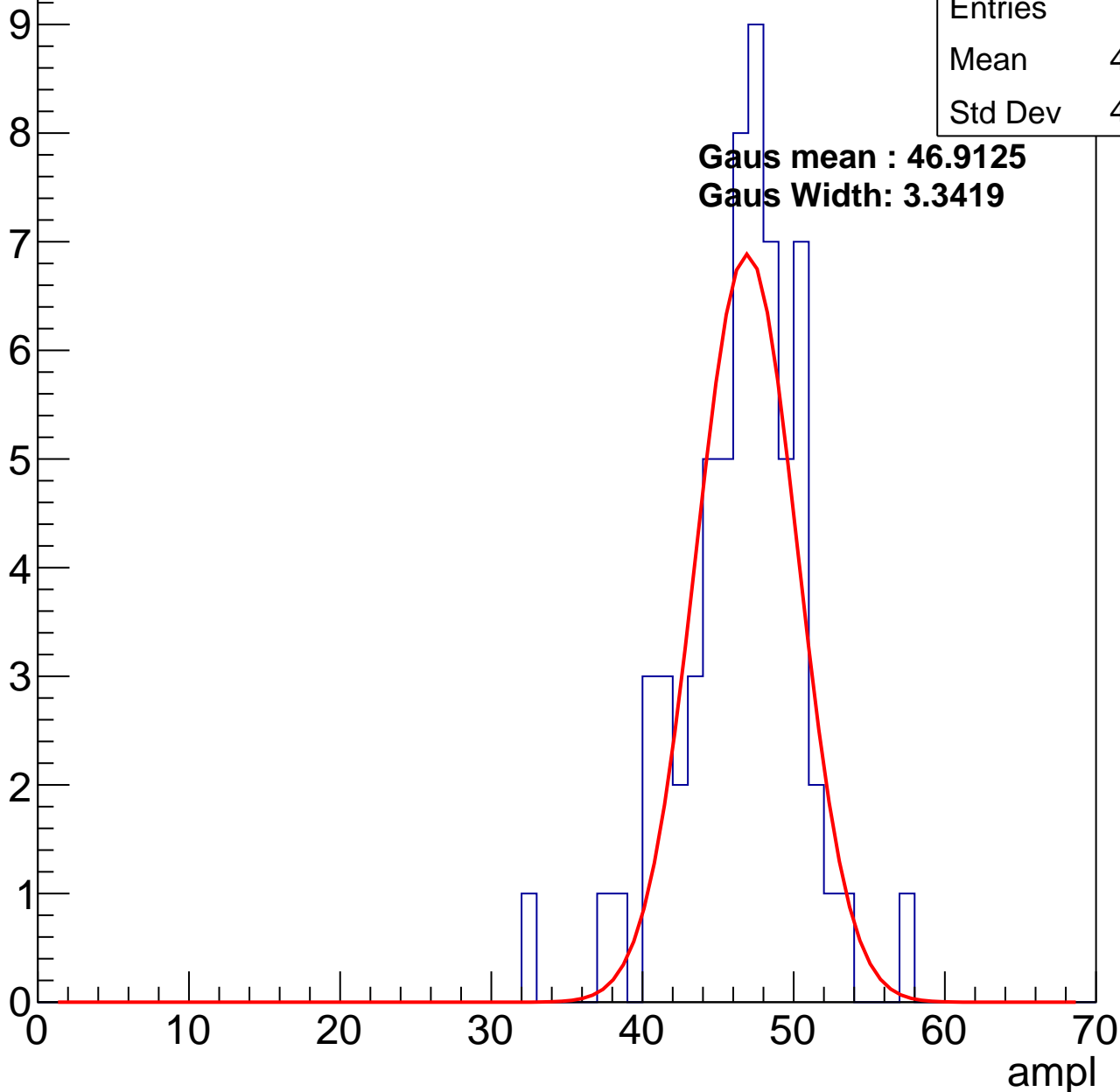
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	46.06
Std Dev	4.034

**Gaus mean : 46.9125**

**Gaus Width: 3.3419**

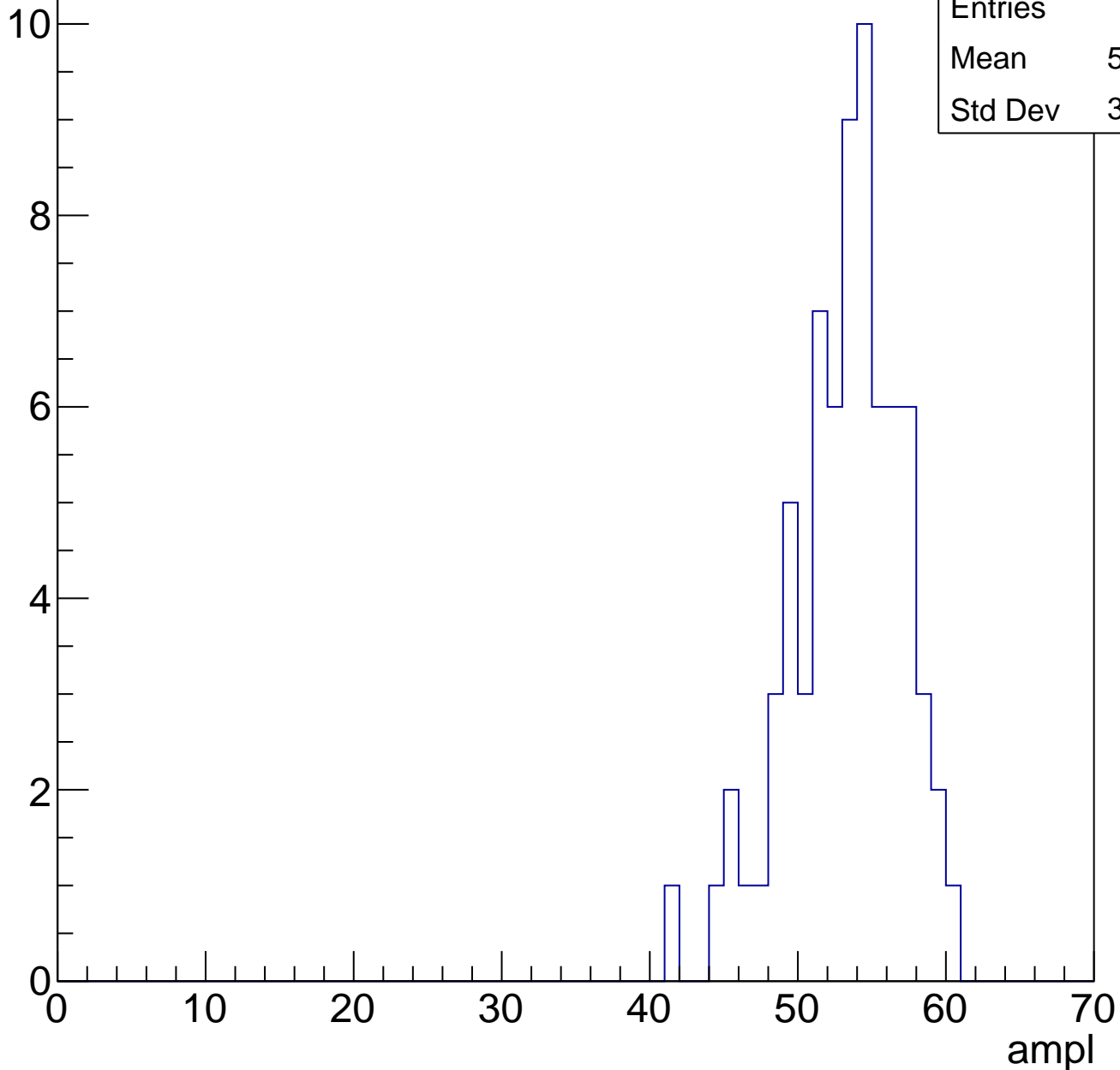


# B1L103S, U11-ch111, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	73
Mean	52.78
Std Dev	3.757

Entry

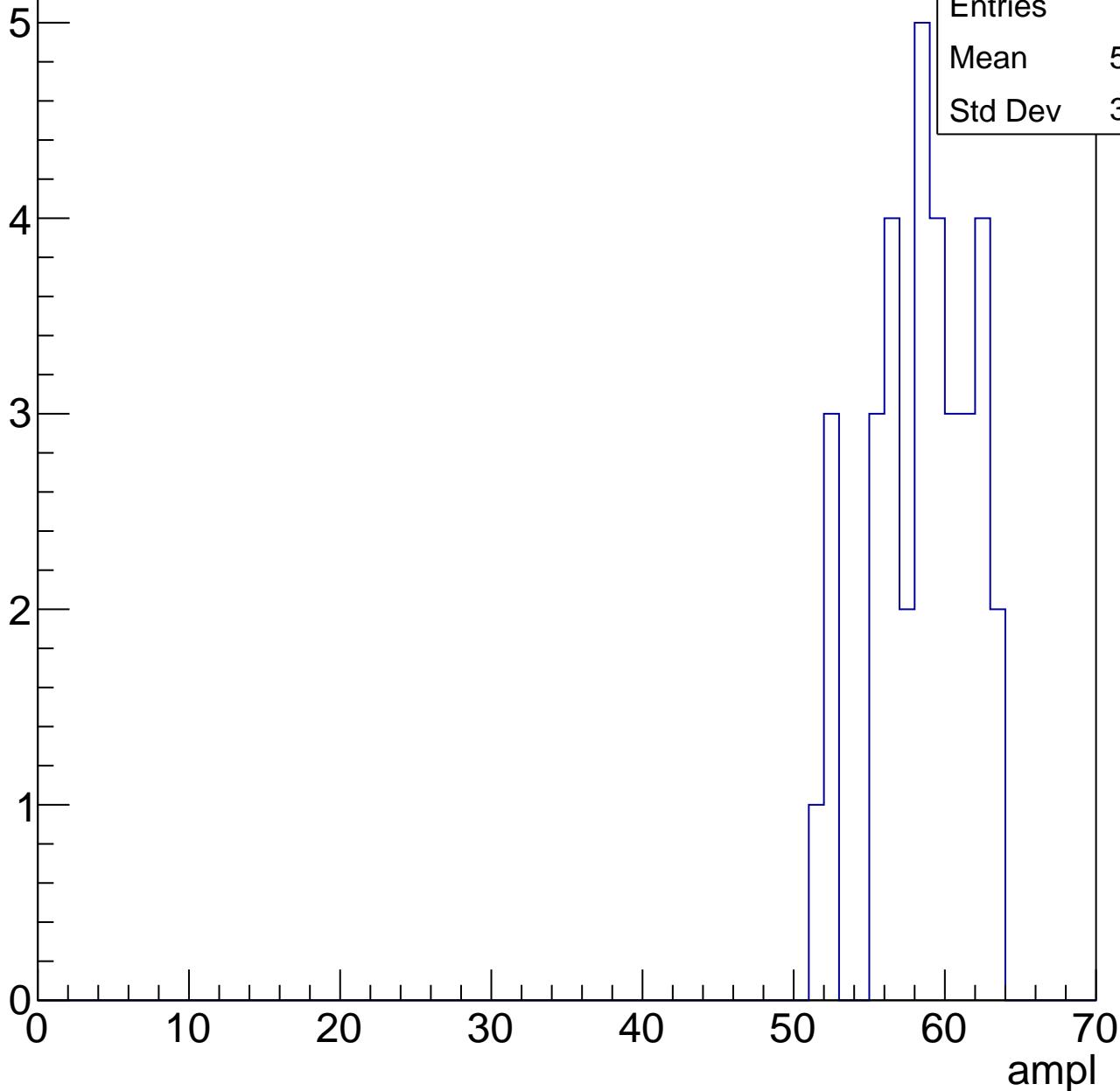


# B1L103S, U11-ch111, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	34
Mean	58.03
Std Dev	3.249

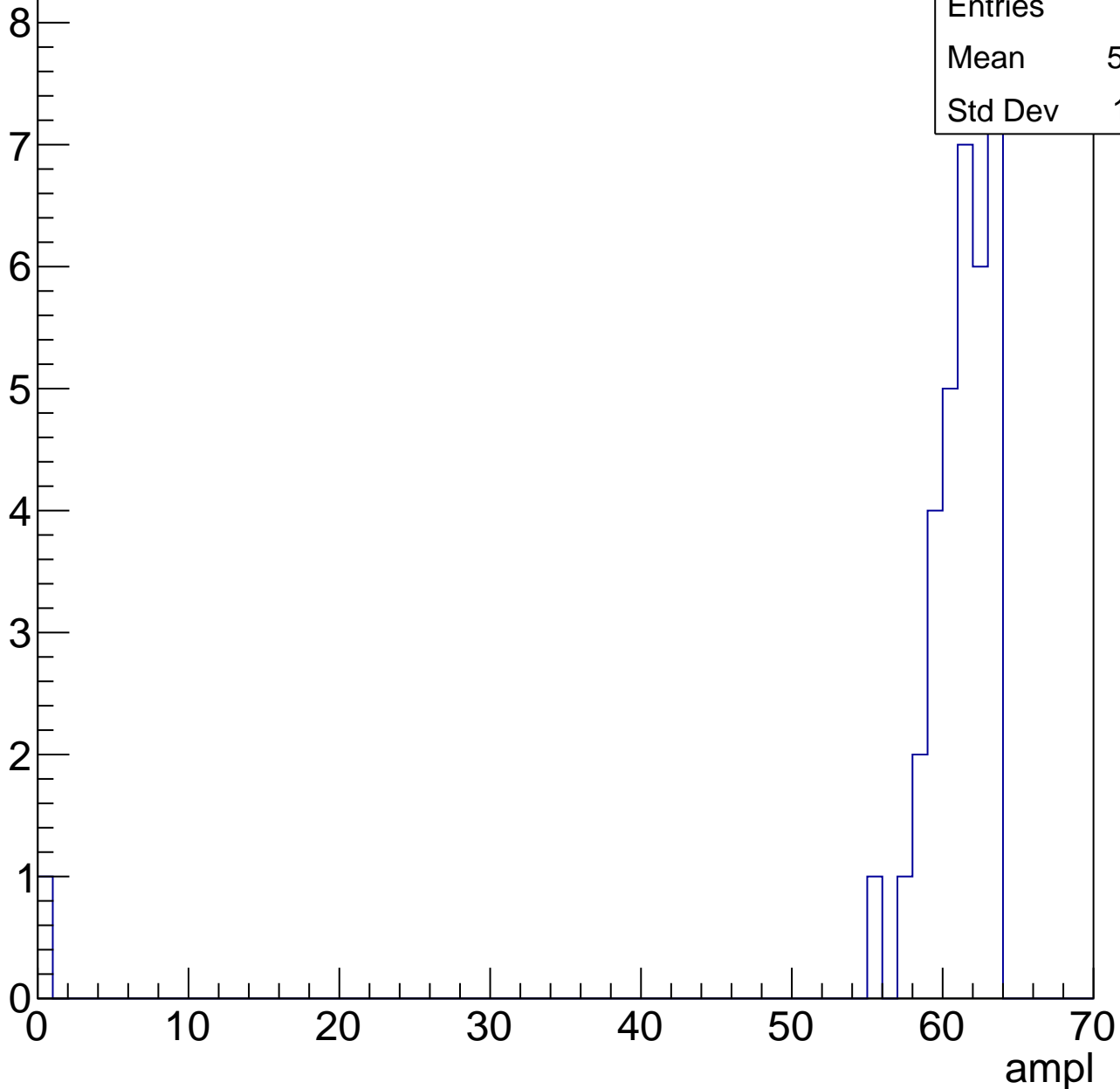


# B1L103S, U11-ch111, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

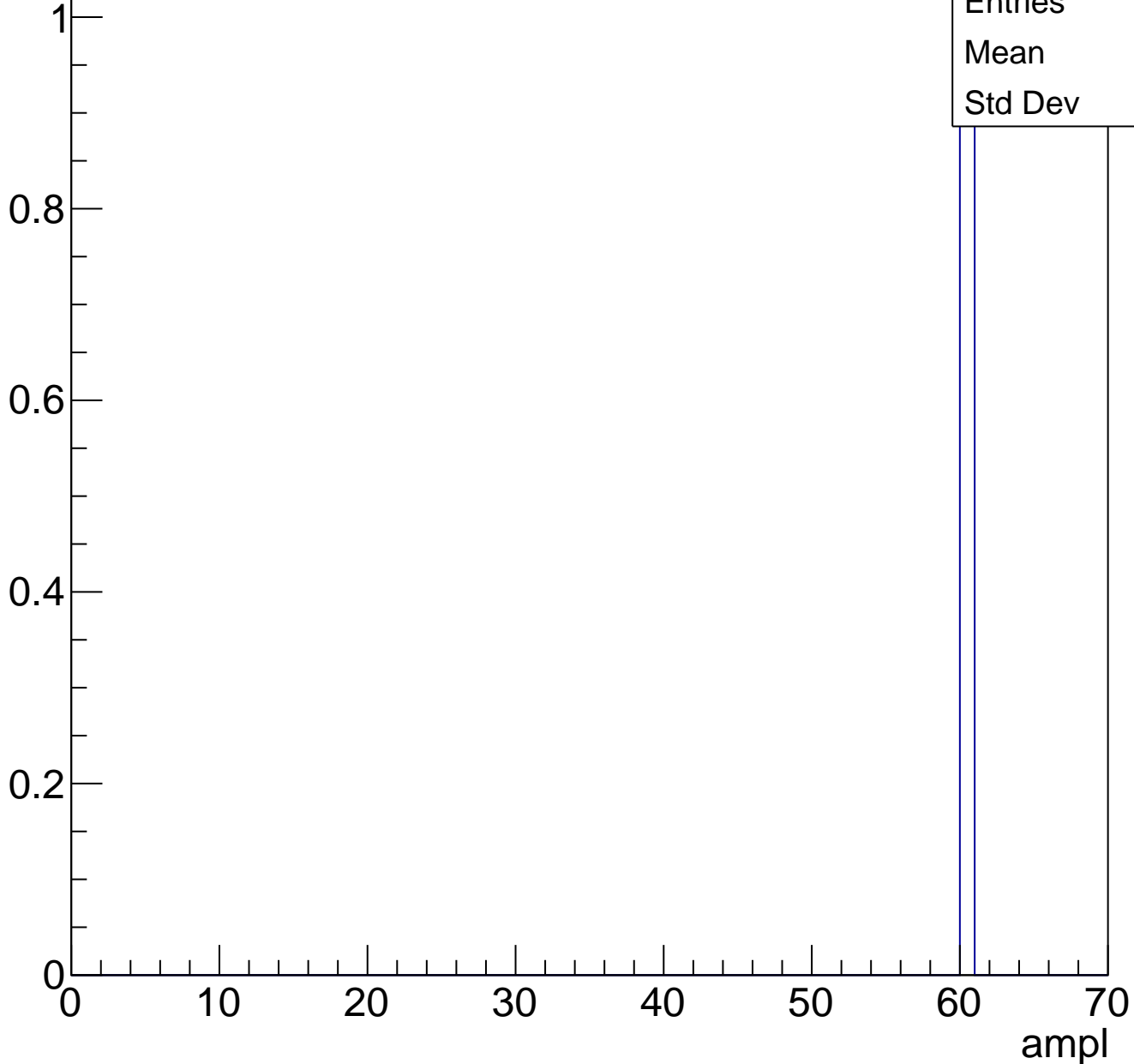
Entries	35
Mean	59.06
Std Dev	10.31



# B1L103S, U11-ch111, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

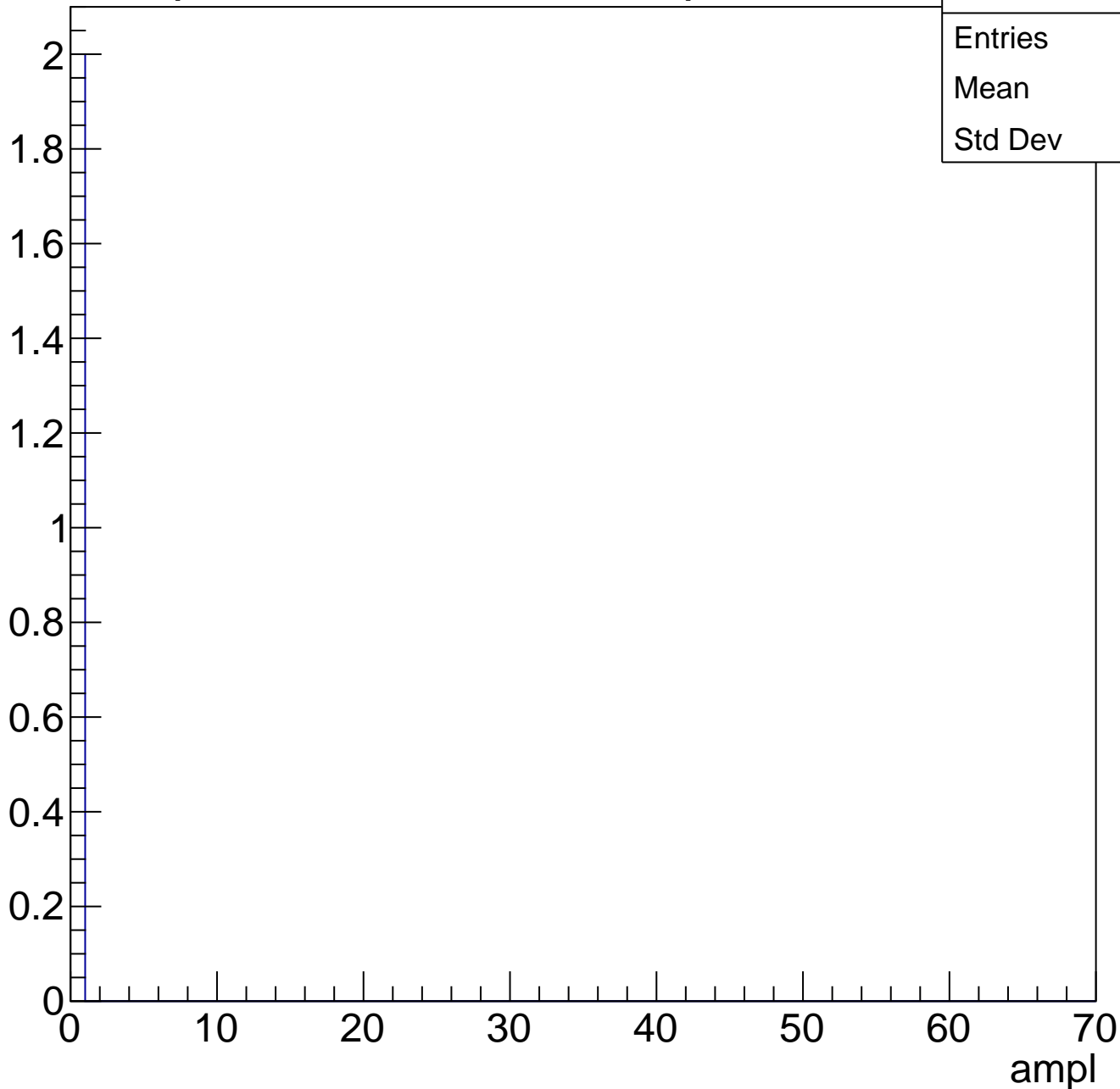




# B1L103S, U11-ch111, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U11-ch112, adc0

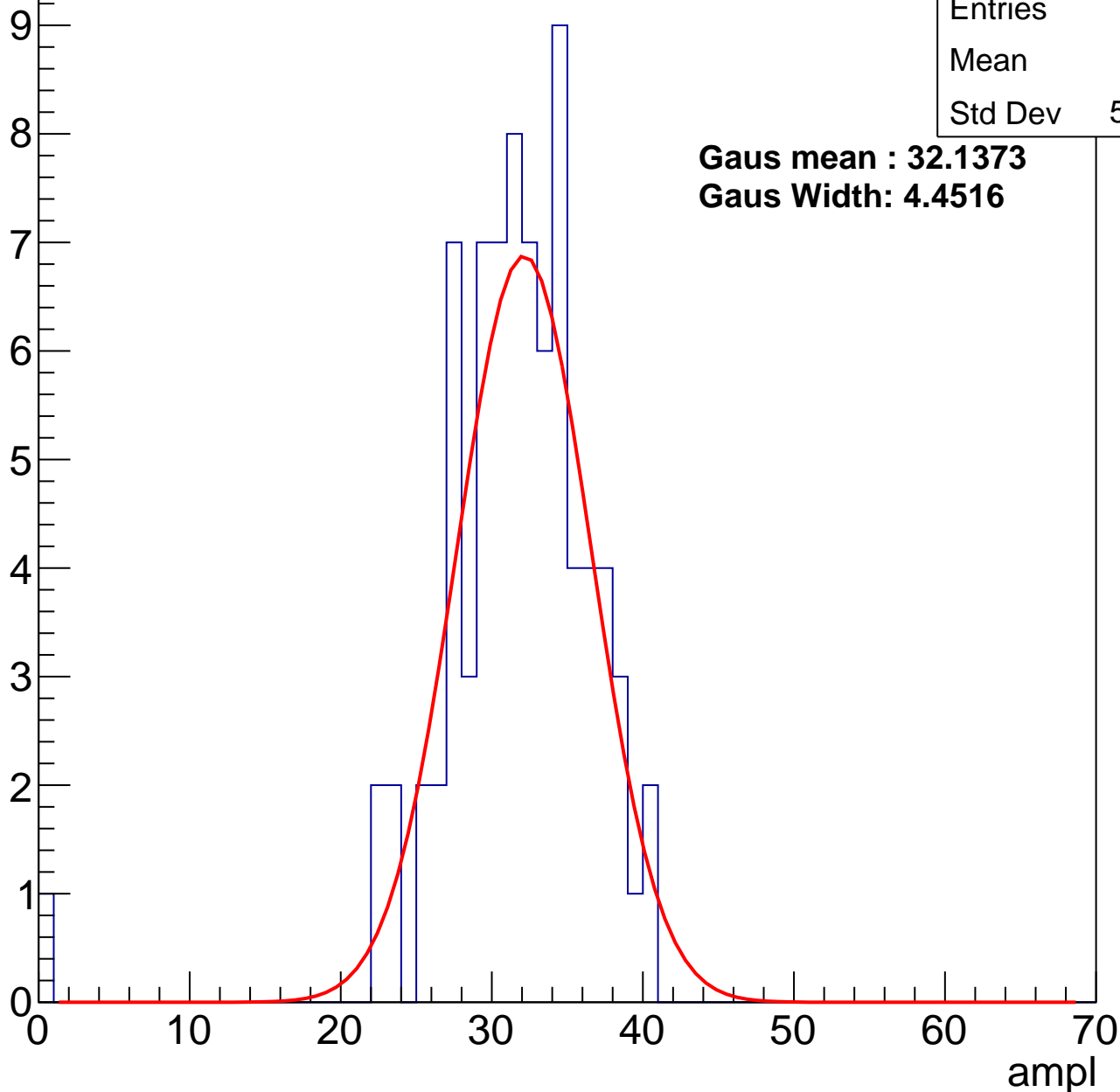
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	81
Mean	31.1
Std Dev	5.374

**Gaus mean : 32.1373**

**Gaus Width: 4.4516**



# B1L103S, U11-ch112, adc1

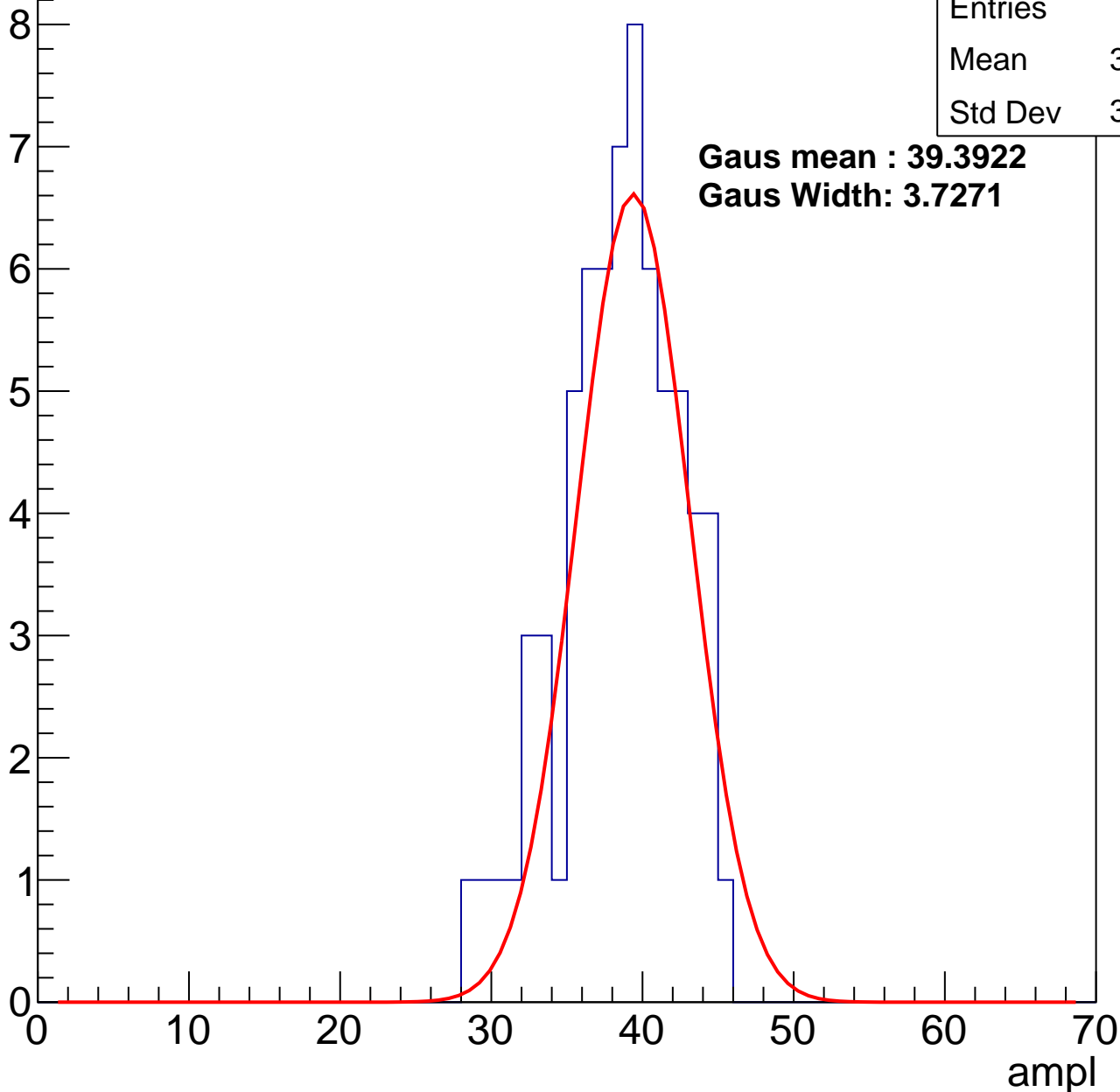
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	68
Mean	38.03
Std Dev	3.869

**Gaus mean : 39.3922**

**Gaus Width: 3.7271**



# B1L103S, U11-ch112, adc2

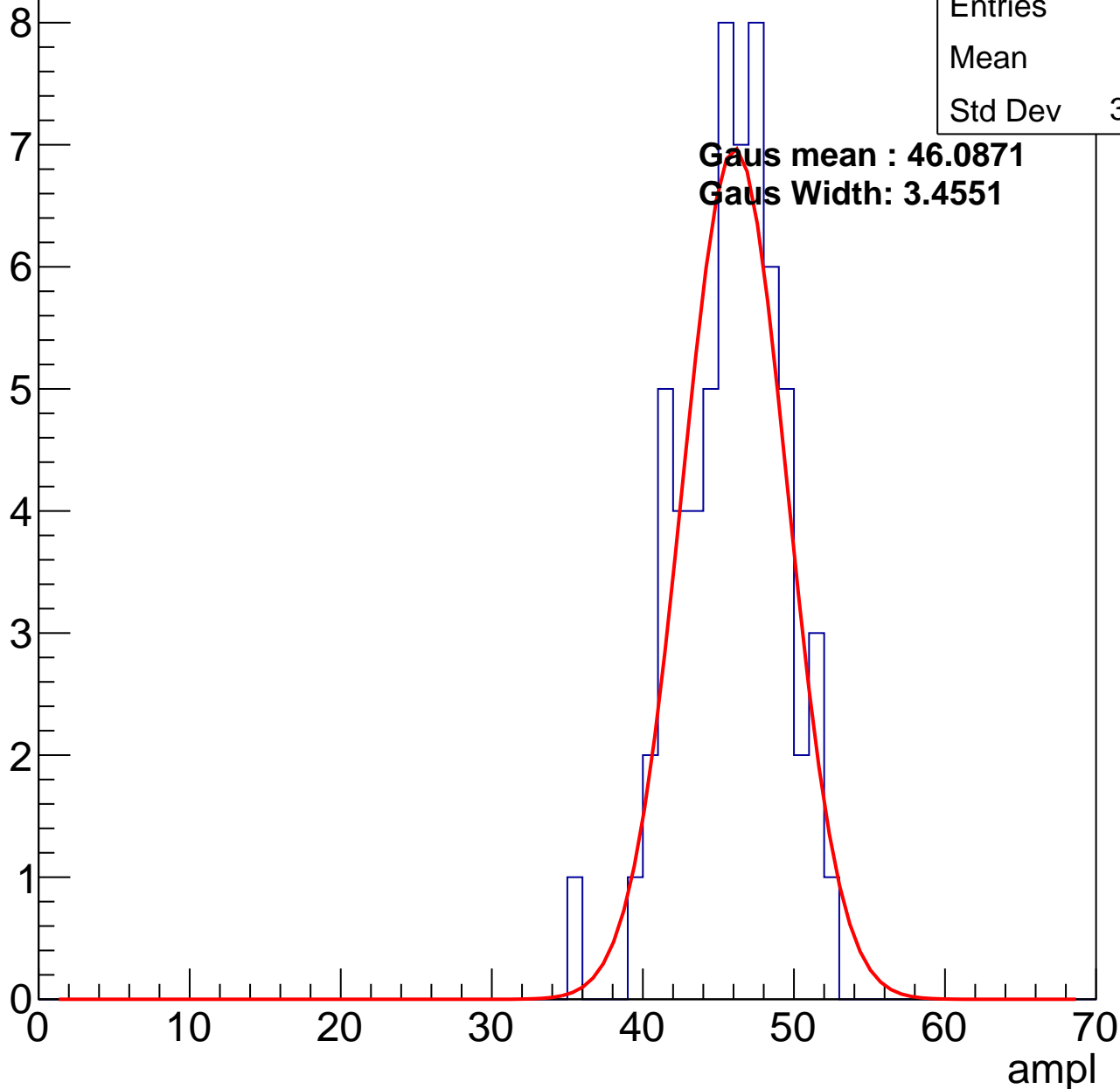
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	45.4
Std Dev	3.343

**Gaus mean : 46.0871**

**Gaus Width: 3.4551**

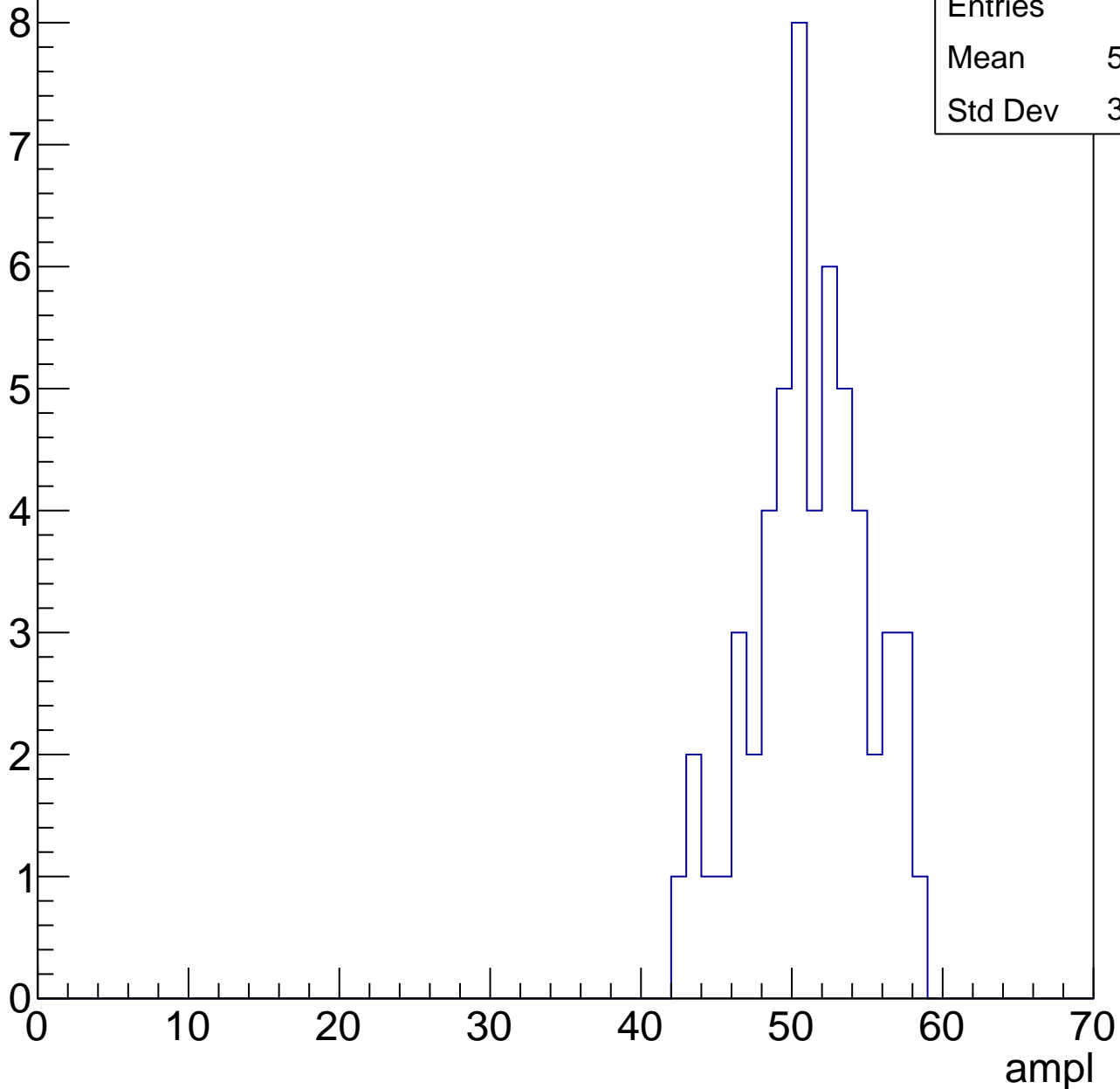


# B1L103S, U11-ch112, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	55
Mean	50.73
Std Dev	3.783

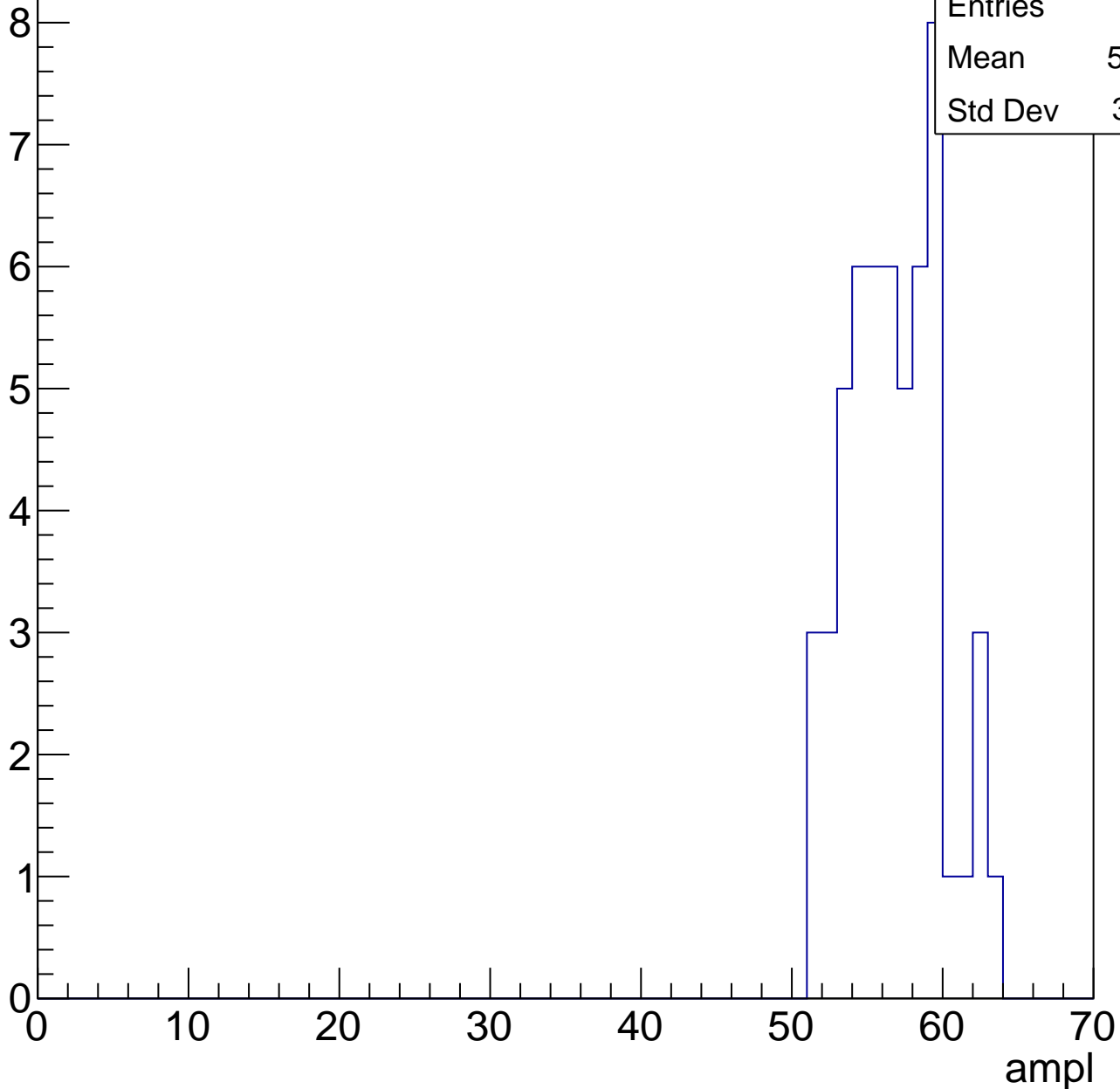


# B1L103S, U11-ch112, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

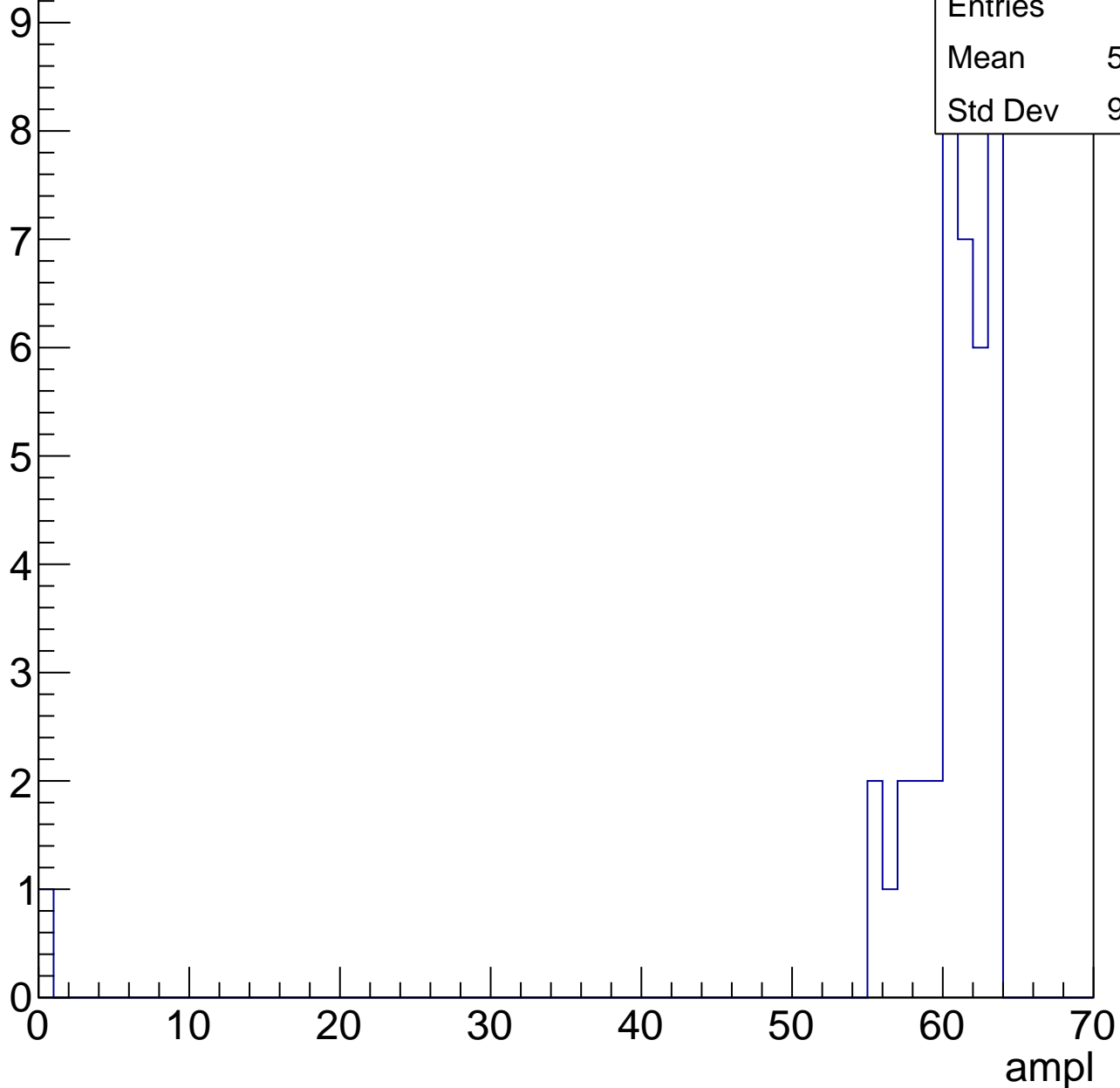
Entries	54
Mean	56.28
Std Dev	3.021



# B1L103S, U11-ch112, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

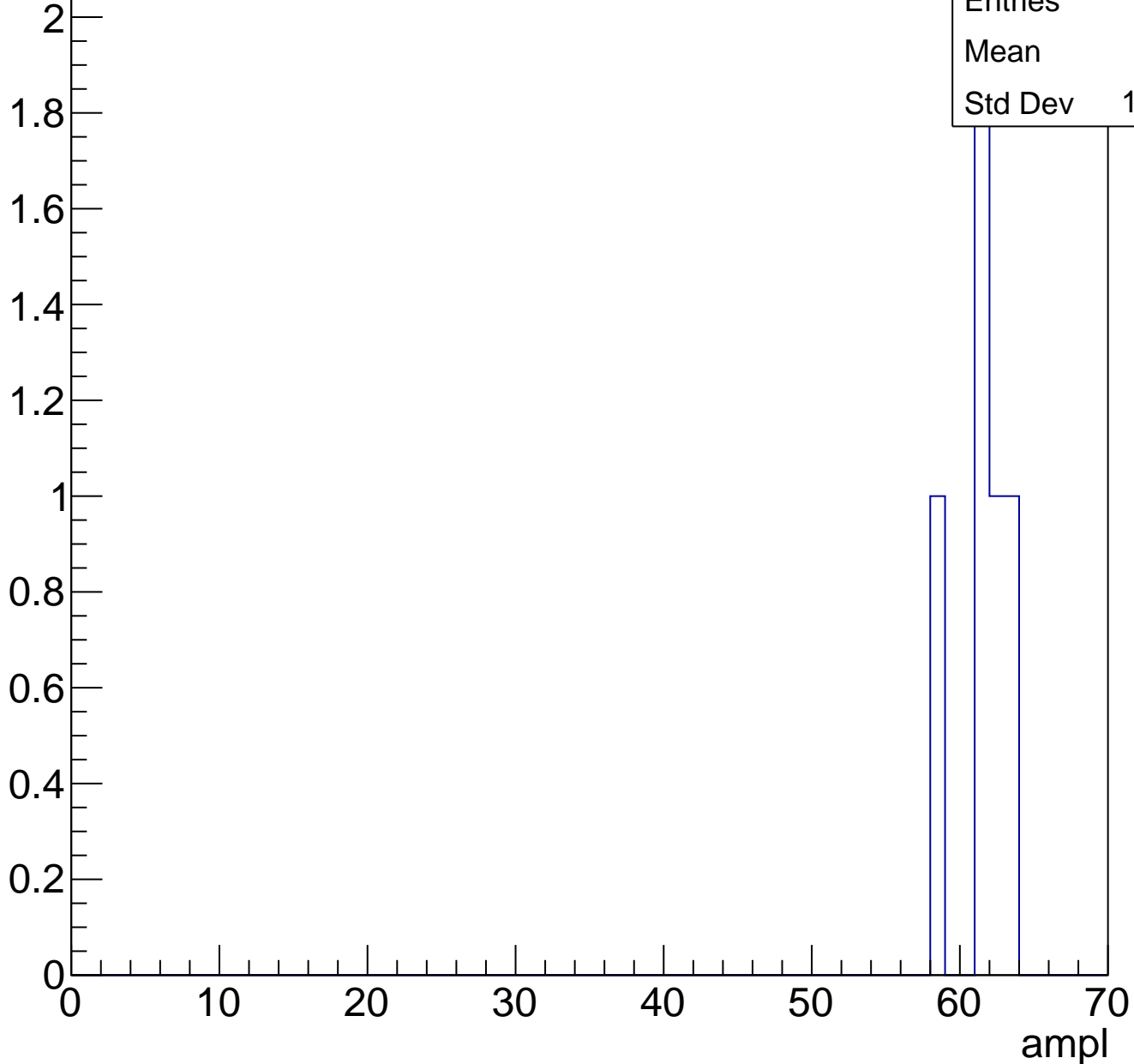
Entry



# B1L103S, U11-ch112, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U11-ch112, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

1  
0.8  
0.6  
0.4  
0.2  
0

Entries	1
Mean	22
Std Dev	0

ampl

# B1L103S, U11-ch113, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	86
Mean	28.07
Std Dev	3.54

**Gaus mean : 28.4820**

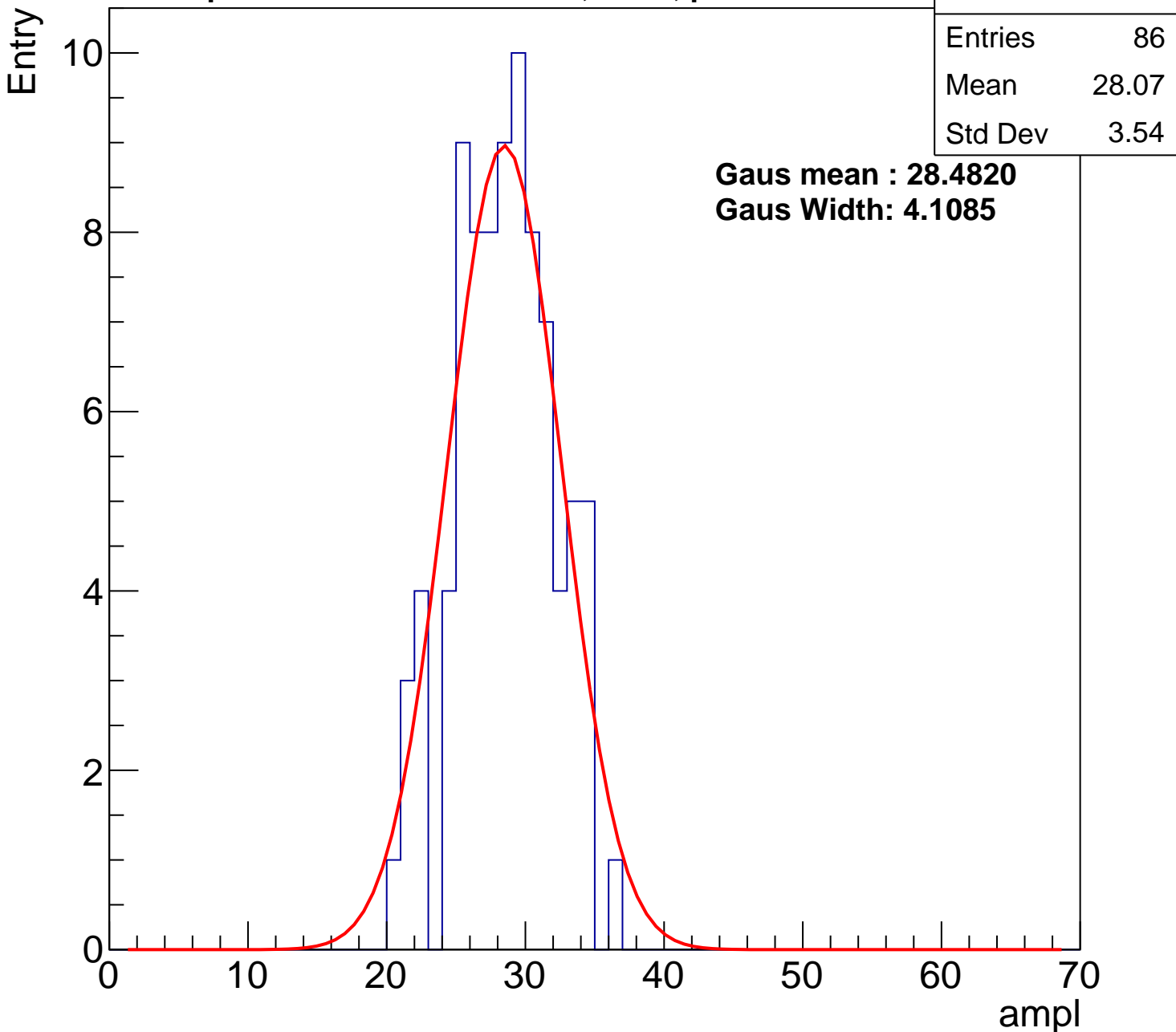
**Gaus Width: 4.1085**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U11-ch113, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	76
Mean	35.89
Std Dev	3.932

**Gaus mean : 36.4131**

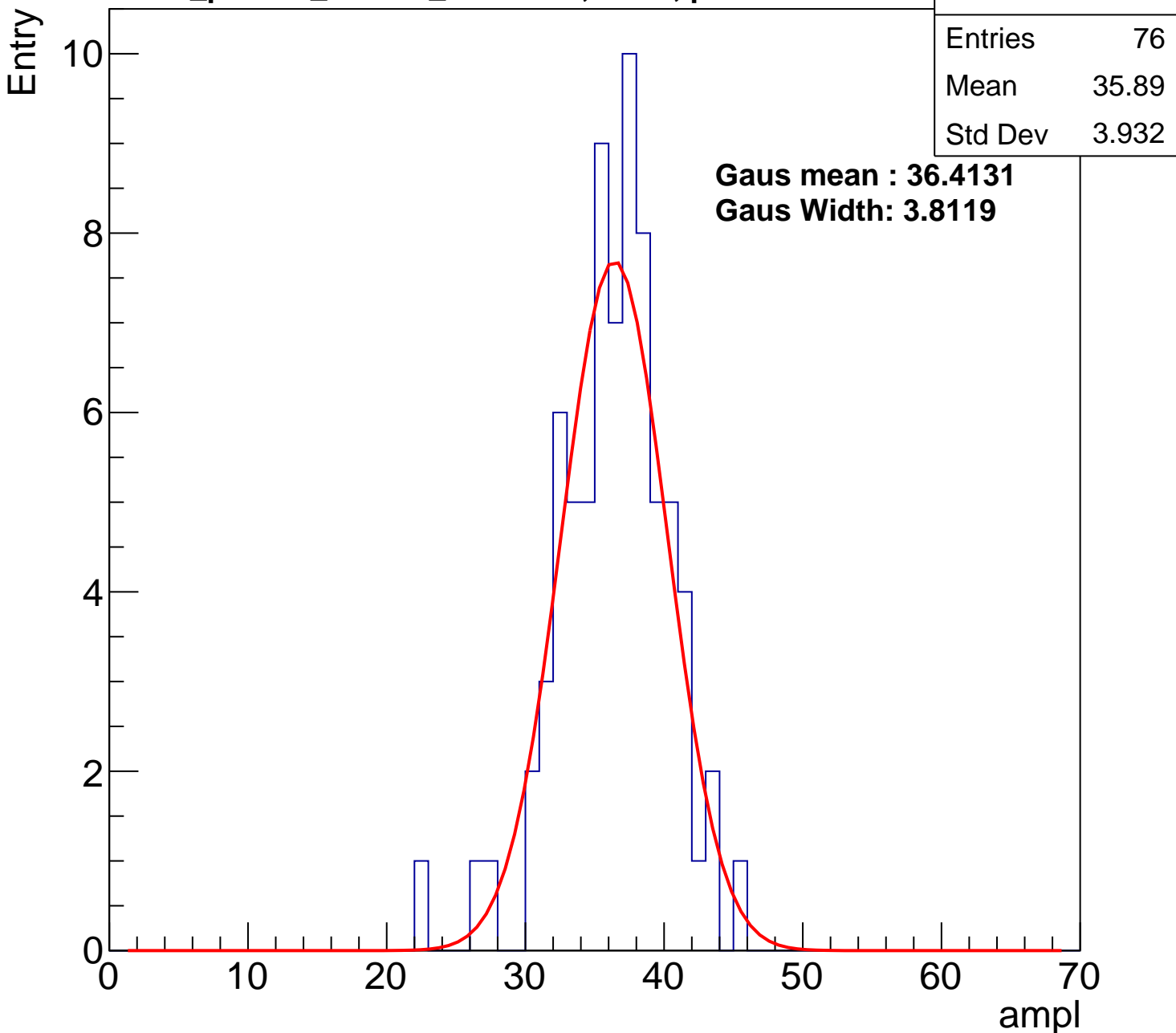
**Gaus Width: 3.8119**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B1L103S, U11-ch113, adc2

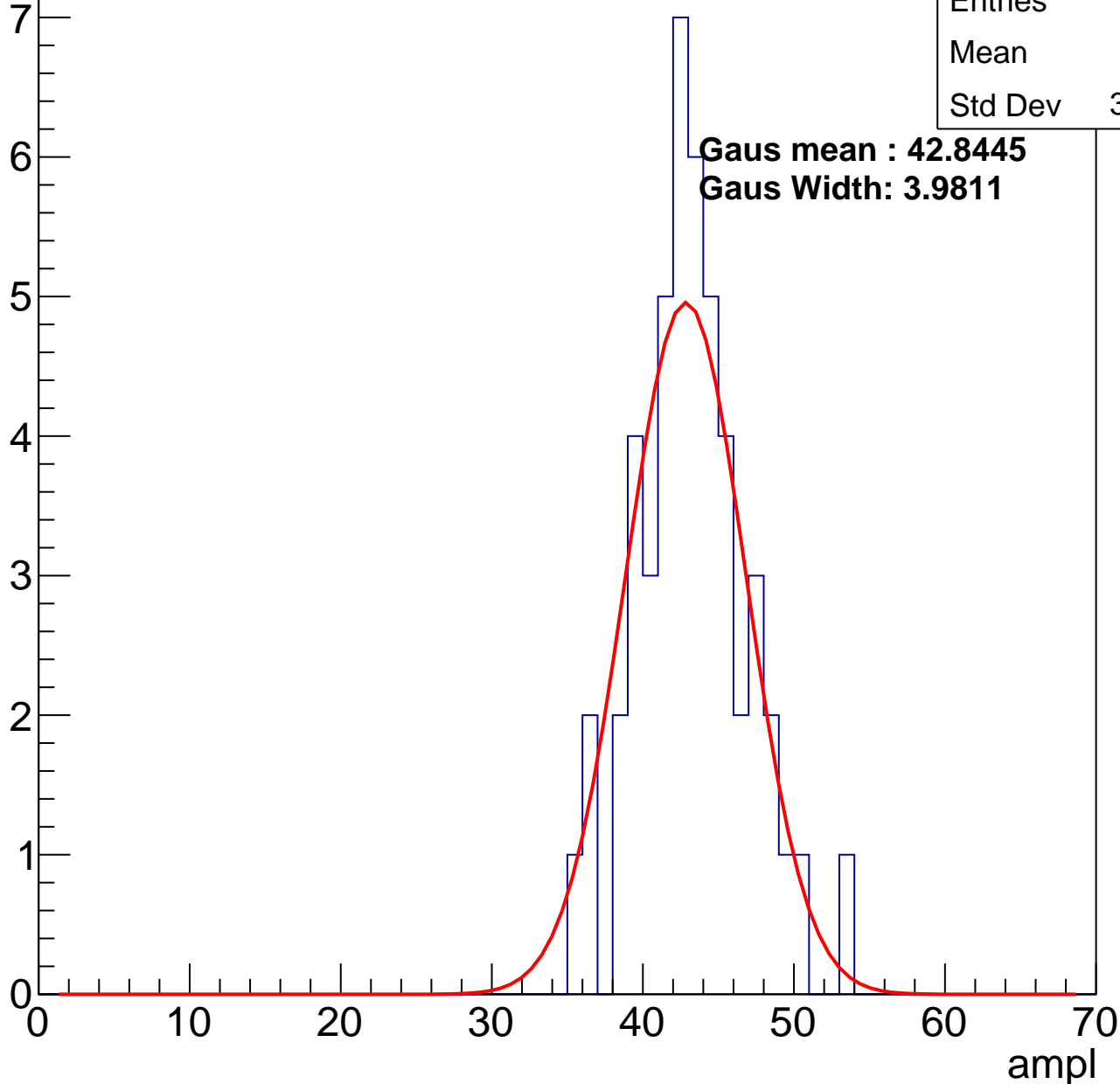
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	49
Mean	42.8
Std Dev	3.642

**Gaus mean : 42.8445**

**Gaus Width: 3.9811**

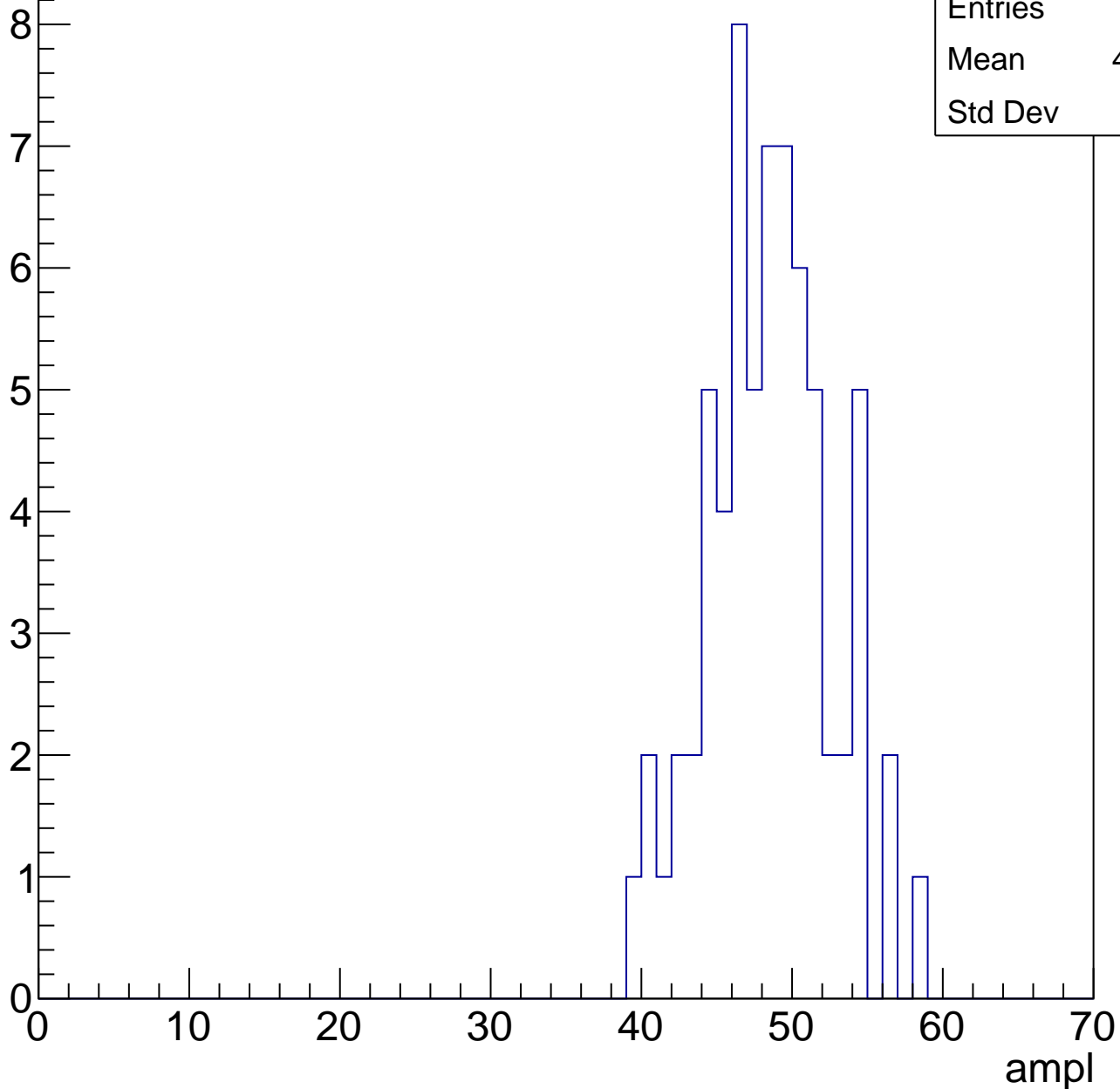


# B1L103S, U11-ch113, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	48.01
Std Dev	4.05

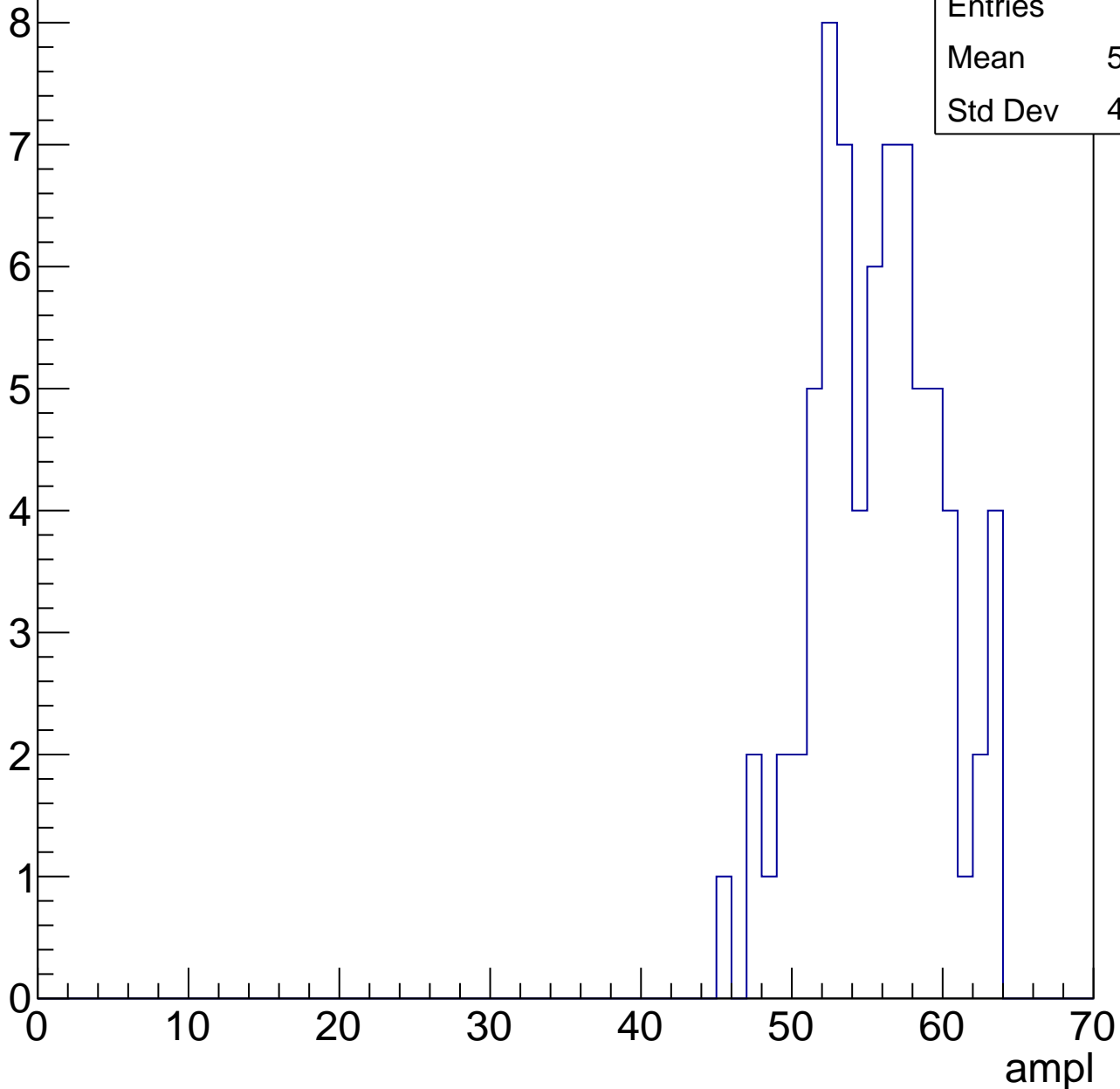


# B1L103S, U11-ch113, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	73
Mean	55.15
Std Dev	4.107

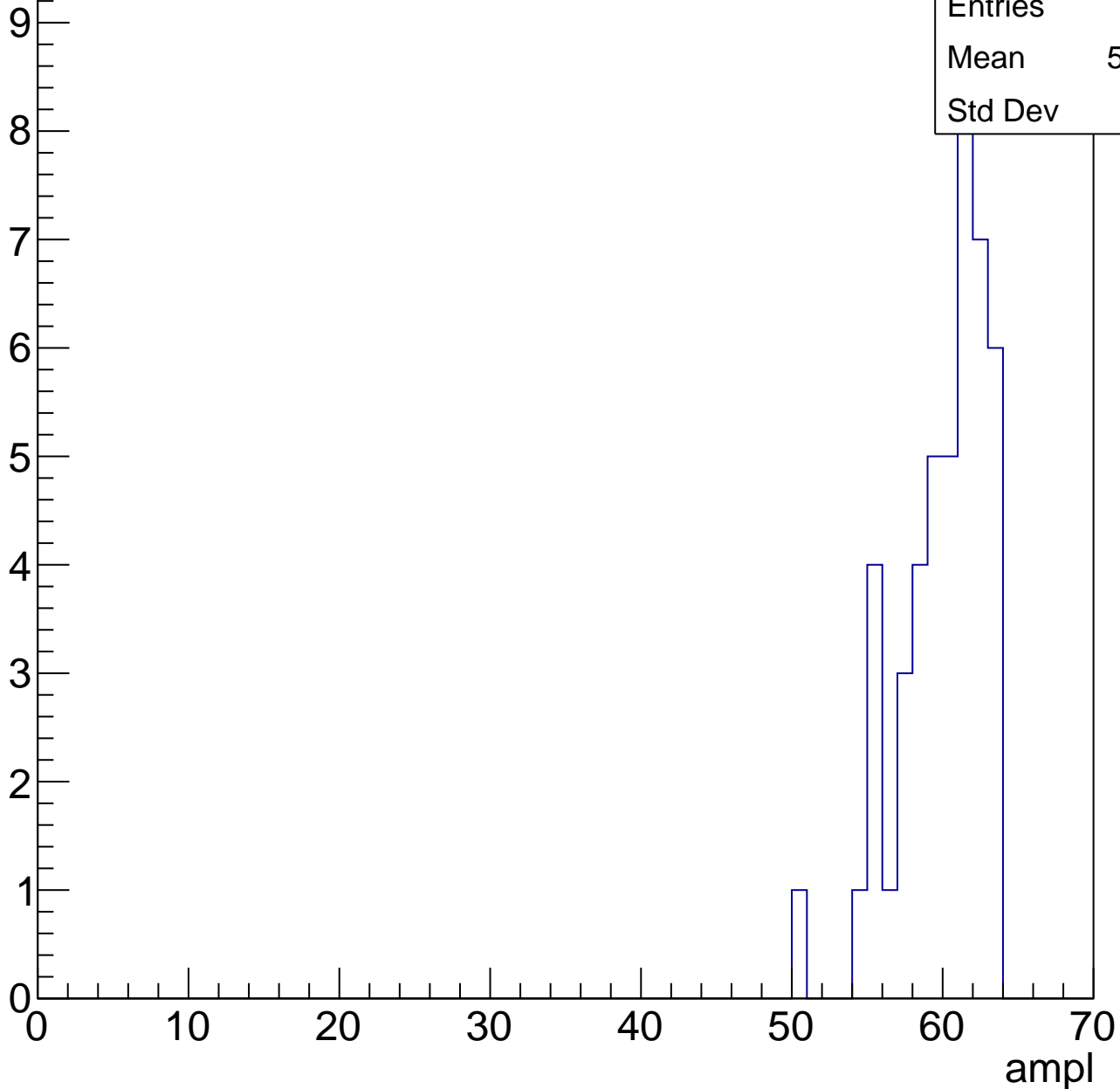


# B1L103S, U11-ch113, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

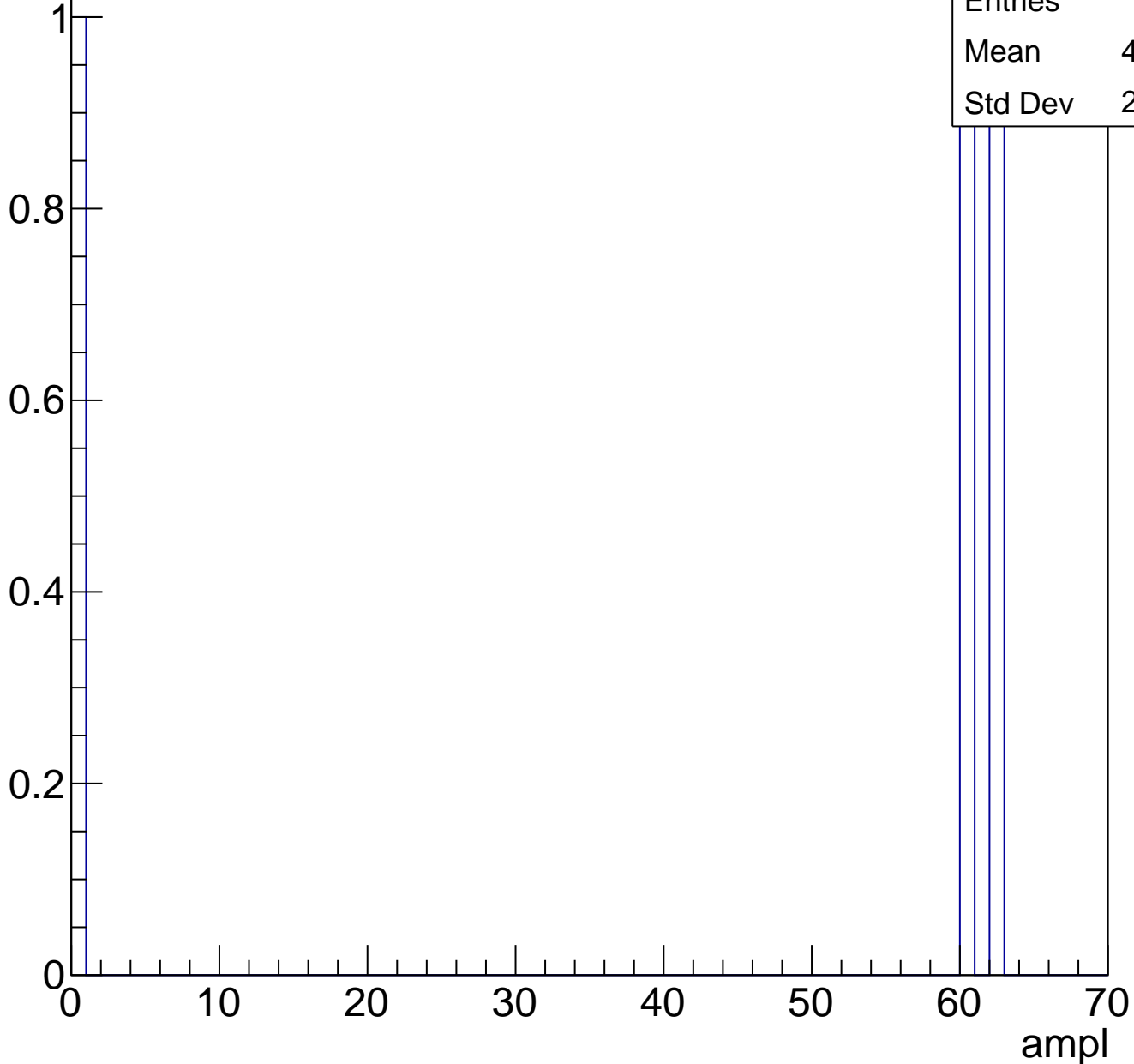
Entries	46
Mean	59.54
Std Dev	2.88



# B1L103S, U11-ch113, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U11-ch113, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U11-ch114, adc0

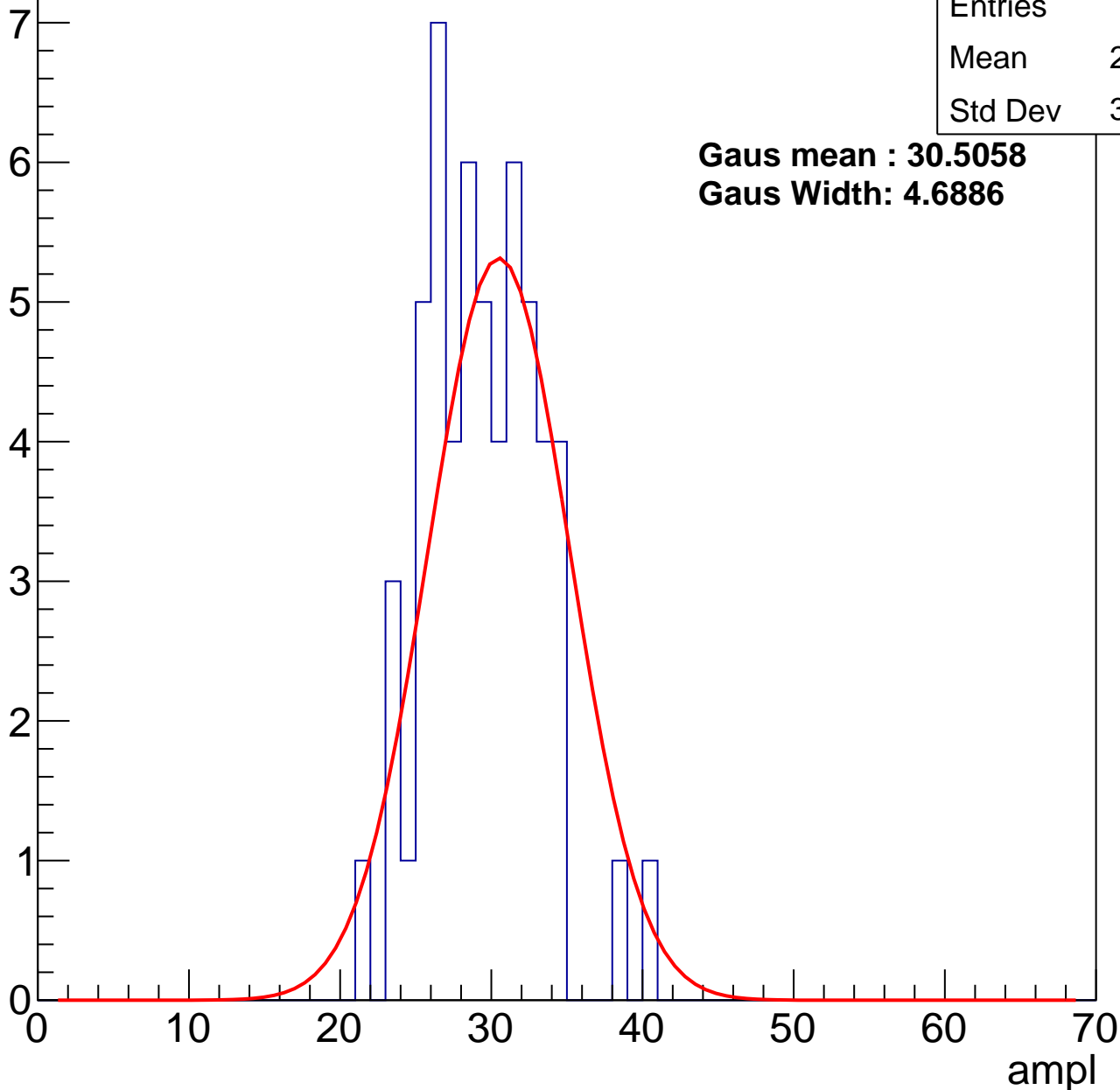
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	57
Mean	29.02
Std Dev	3.749

**Gaus mean : 30.5058**

**Gaus Width: 4.6886**



# B1L103S, U11-ch114, adc1

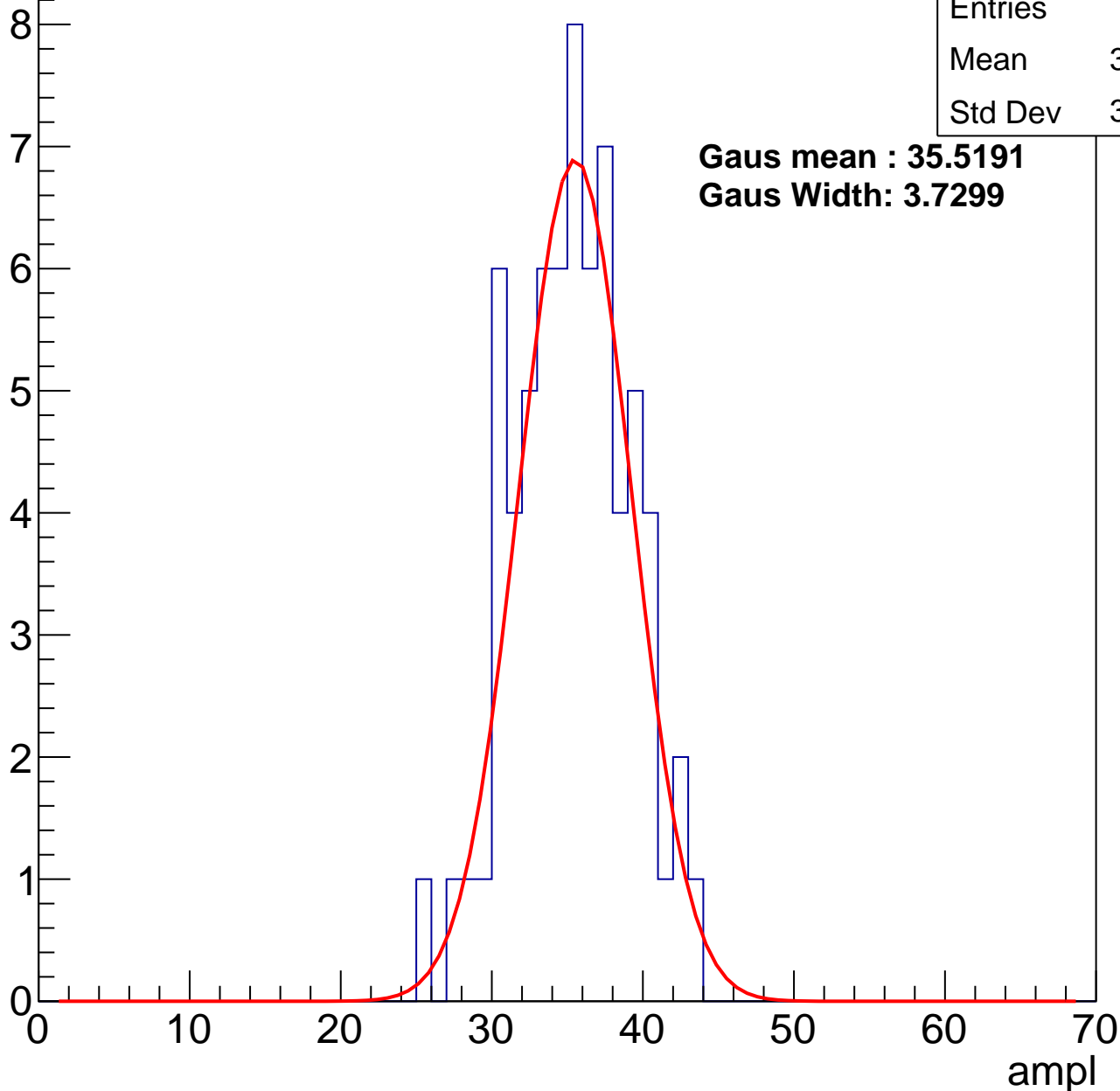
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	69
Mean	34.86
Std Dev	3.777

**Gaus mean : 35.5191**

**Gaus Width: 3.7299**



# B1L103S, U11-ch114, adc2

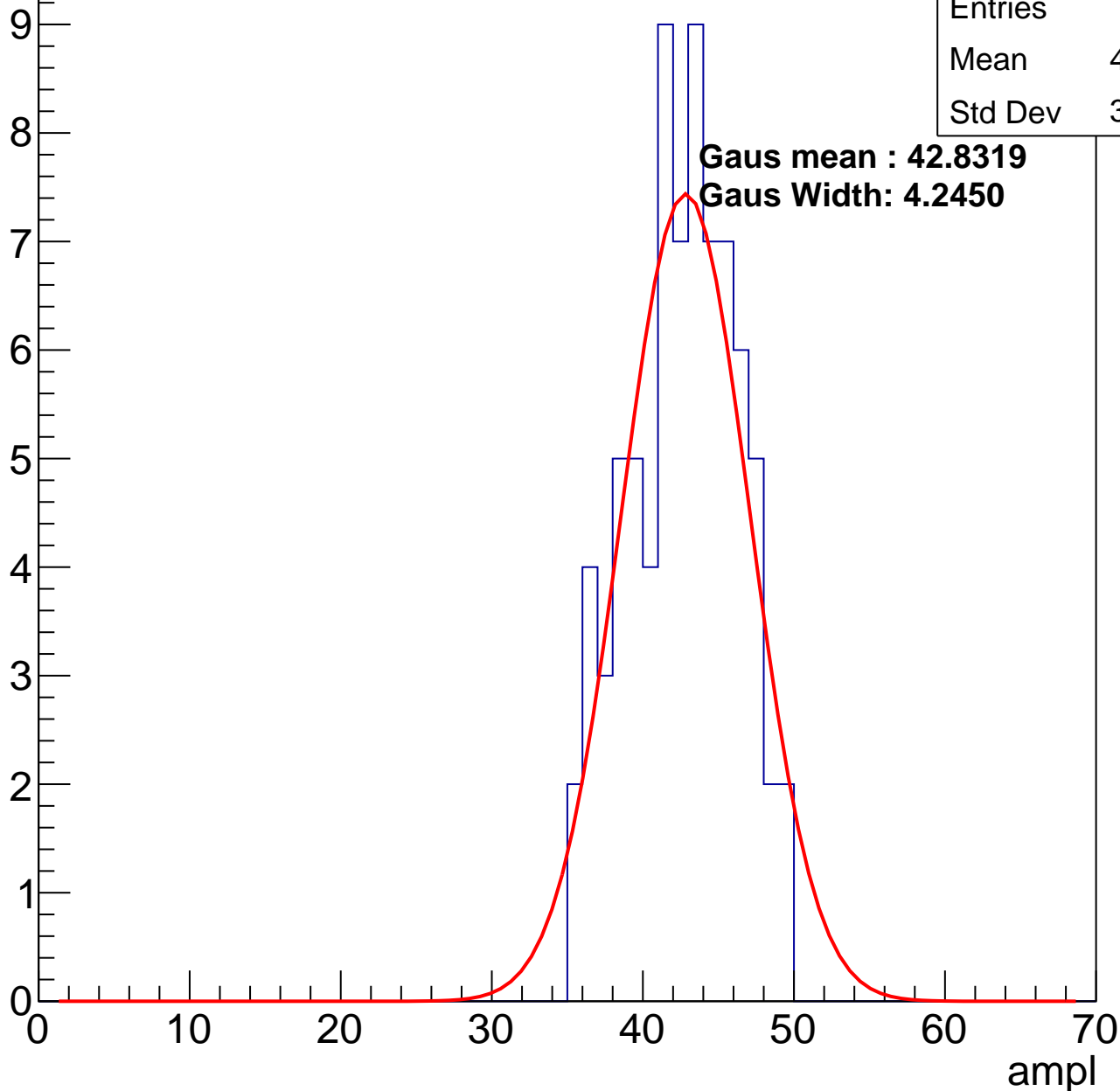
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	77
Mean	42.18
Std Dev	3.523

**Gaus mean : 42.8319**

**Gaus Width: 4.2450**

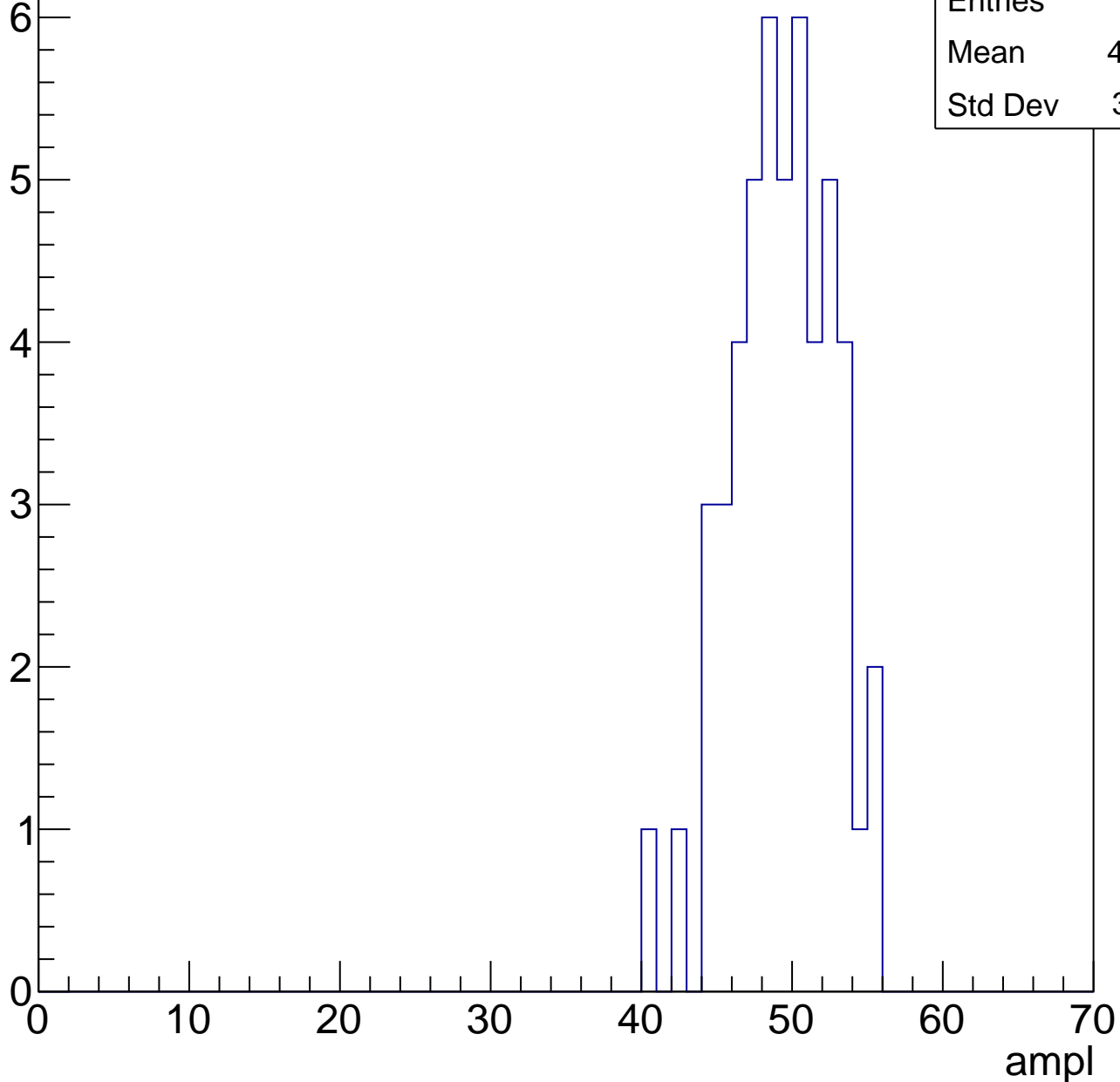


# B1L103S, U11-ch114, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	50
Mean	48.82
Std Dev	3.291

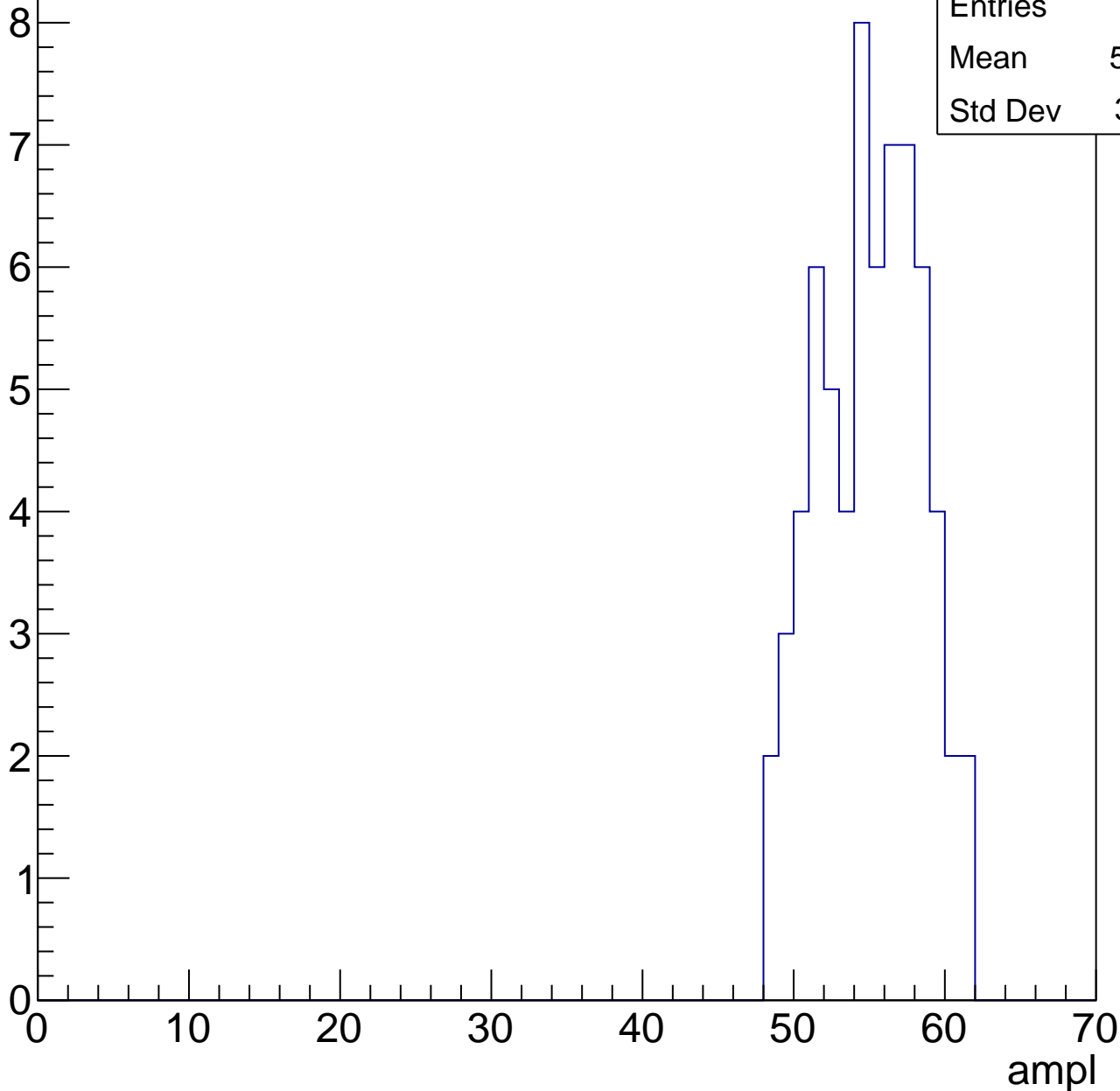


# B1L103S, U11-ch114, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	54.55
Std Dev	3.331

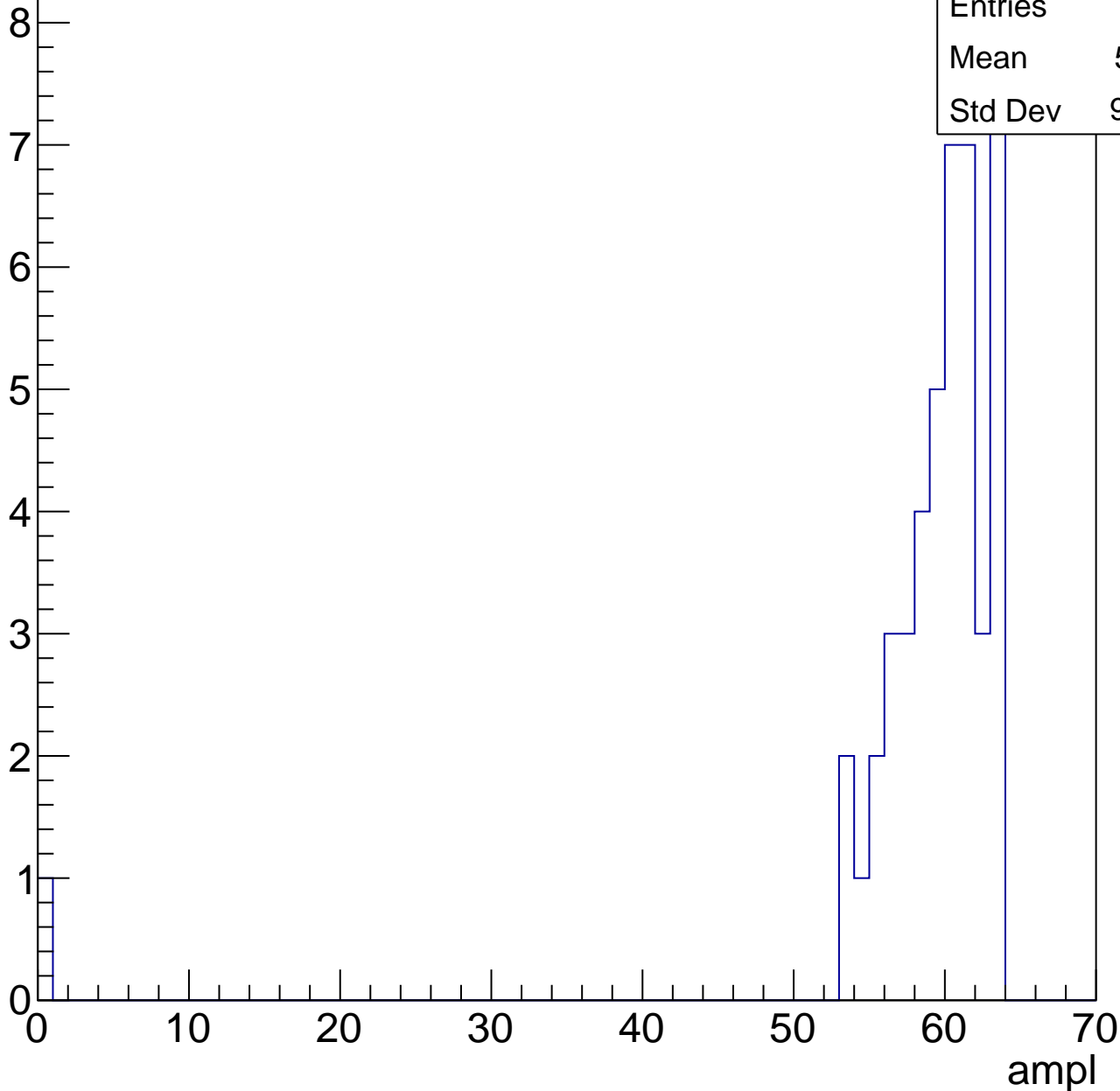


# B1L103S, U11-ch114, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	46
Mean	58.11
Std Dev	9.097

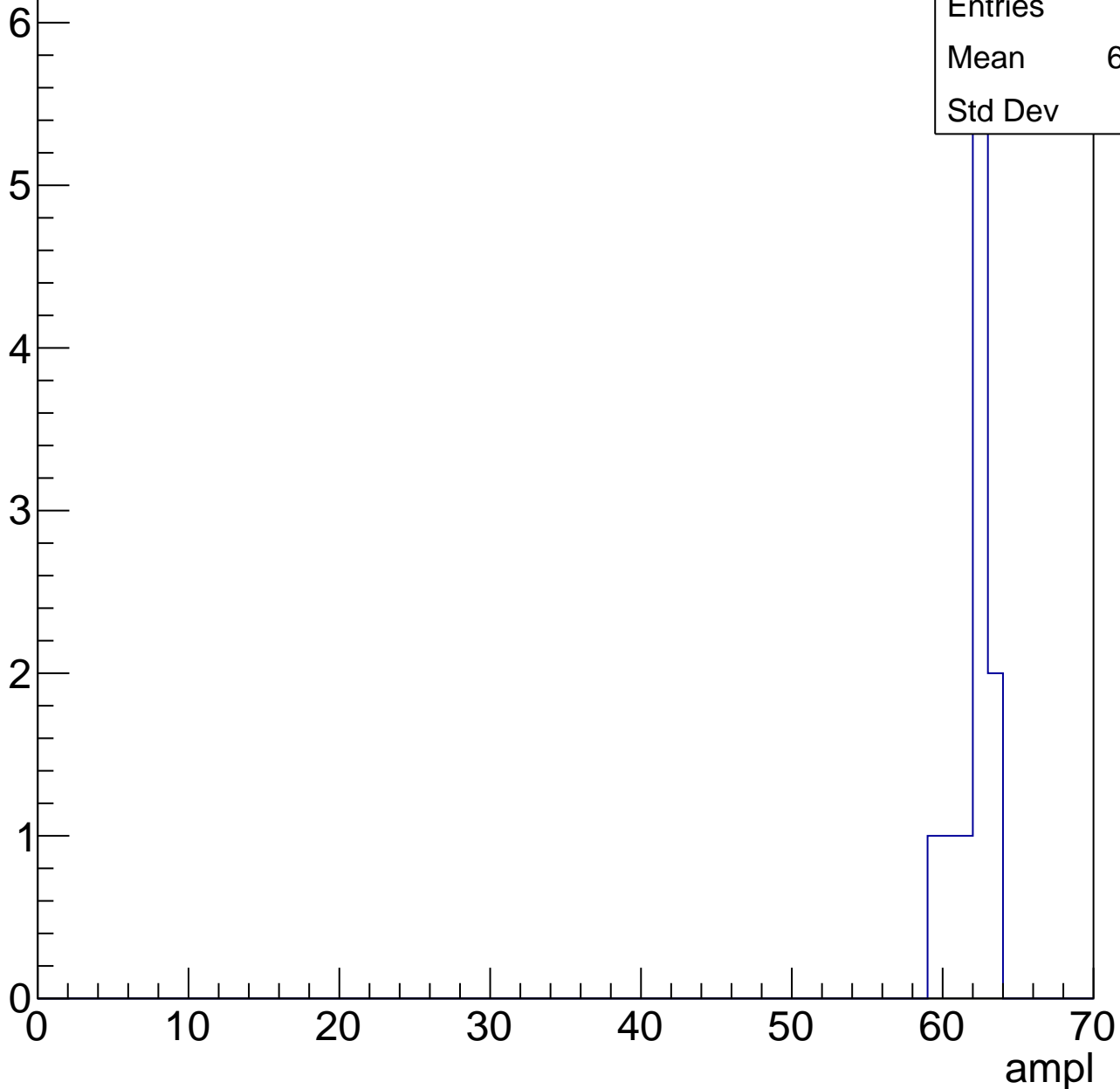


# B1L103S, U11-ch114, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	11
Mean	61.64
Std Dev	1.15





# B1L103S, U11-ch114, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U11-ch115, adc0

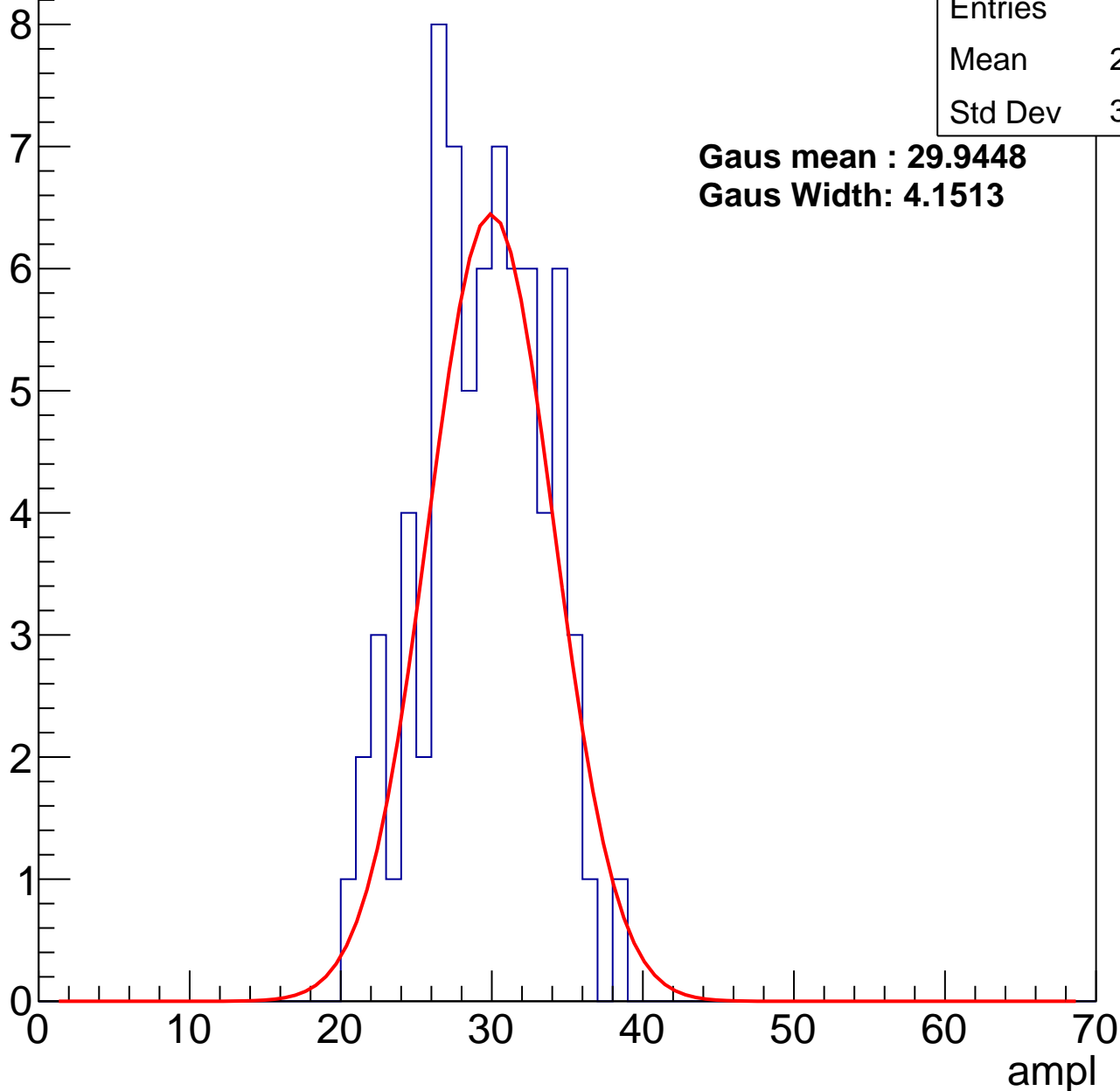
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	73
Mean	28.92
Std Dev	3.996

**Gaus mean : 29.9448**

**Gaus Width: 4.1513**



# B1L103S, U11-ch115, adc1

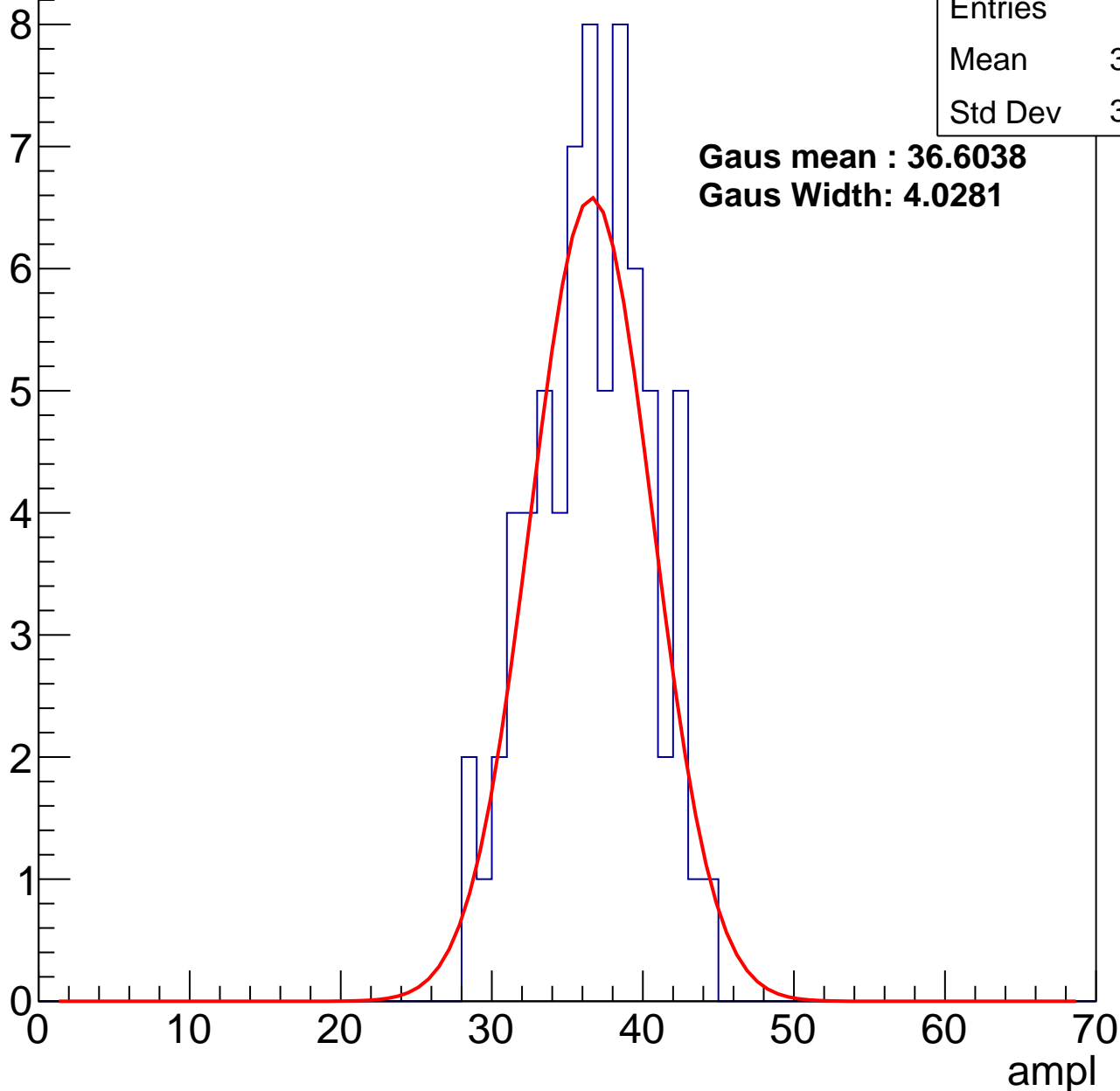
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	70
Mean	36.19
Std Dev	3.766

**Gaus mean : 36.6038**

**Gaus Width: 4.0281**



# B1L103S, U11-ch115, adc2

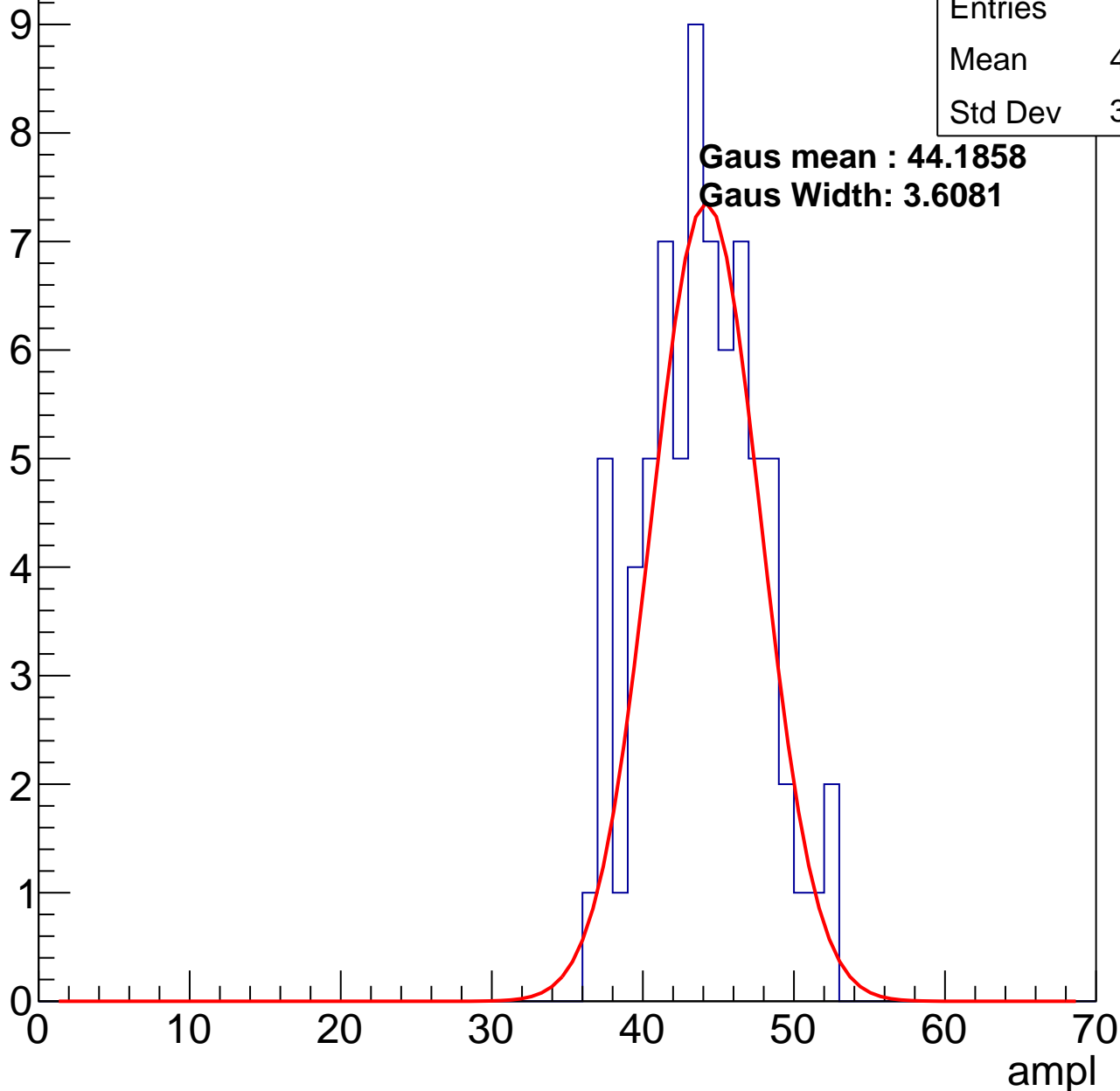
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	73
Mean	43.52
Std Dev	3.742

**Gaus mean : 44.1858**

**Gaus Width: 3.6081**

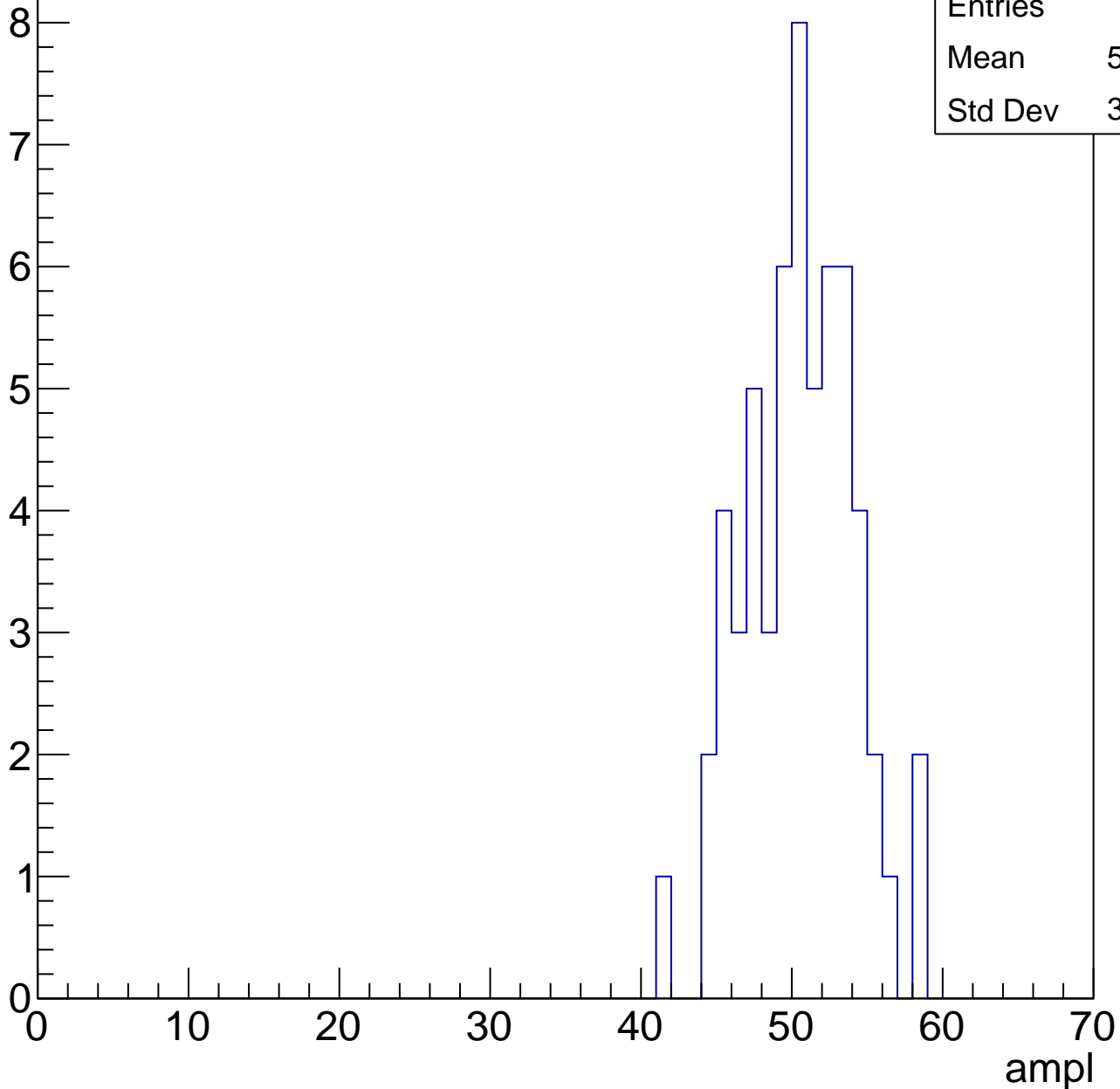


# B1L103S, U11-ch115, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	58
Mean	50.05
Std Dev	3.535

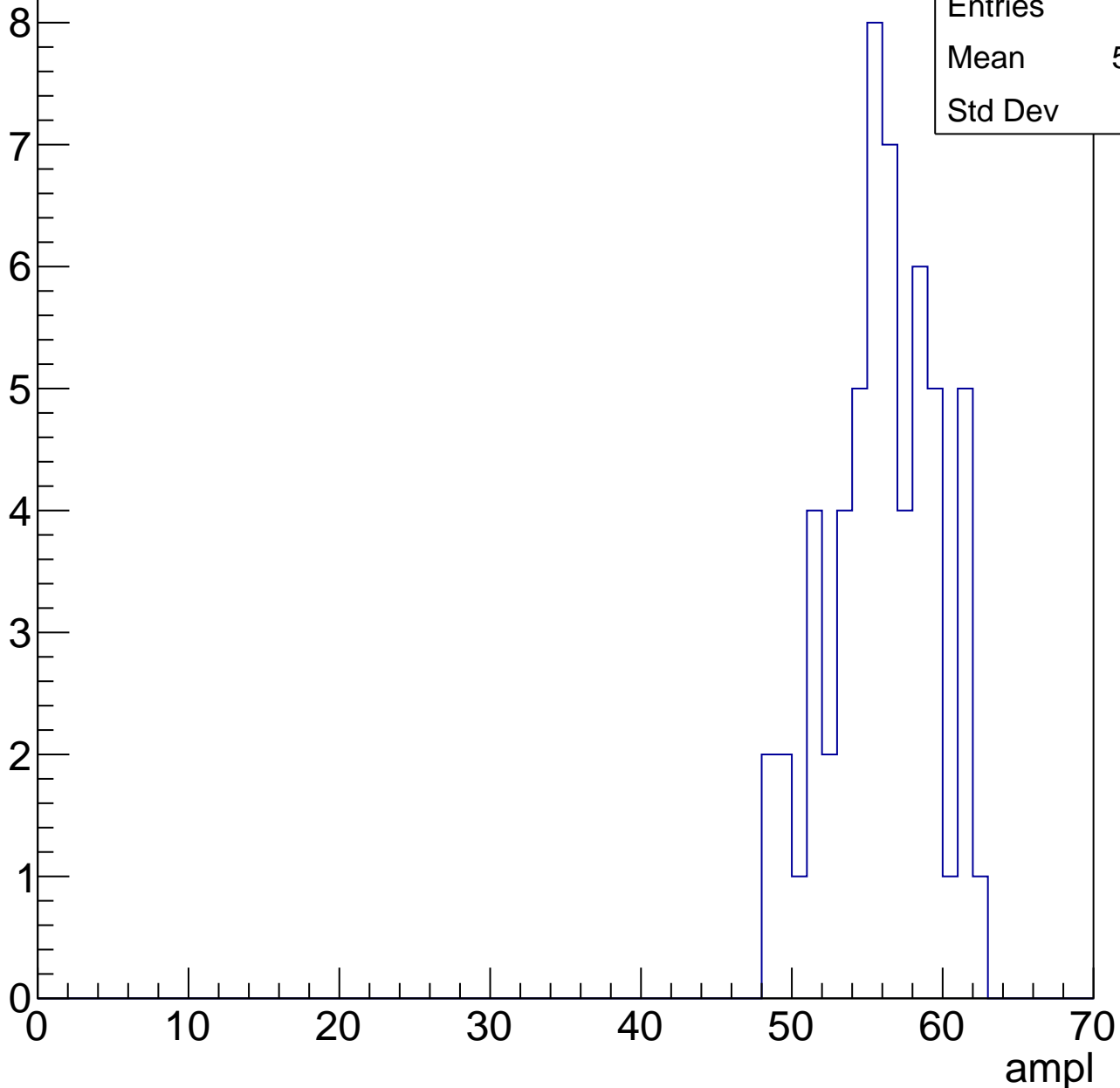


# B1L103S, U11-ch115, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	57
Mean	55.51
Std Dev	3.49

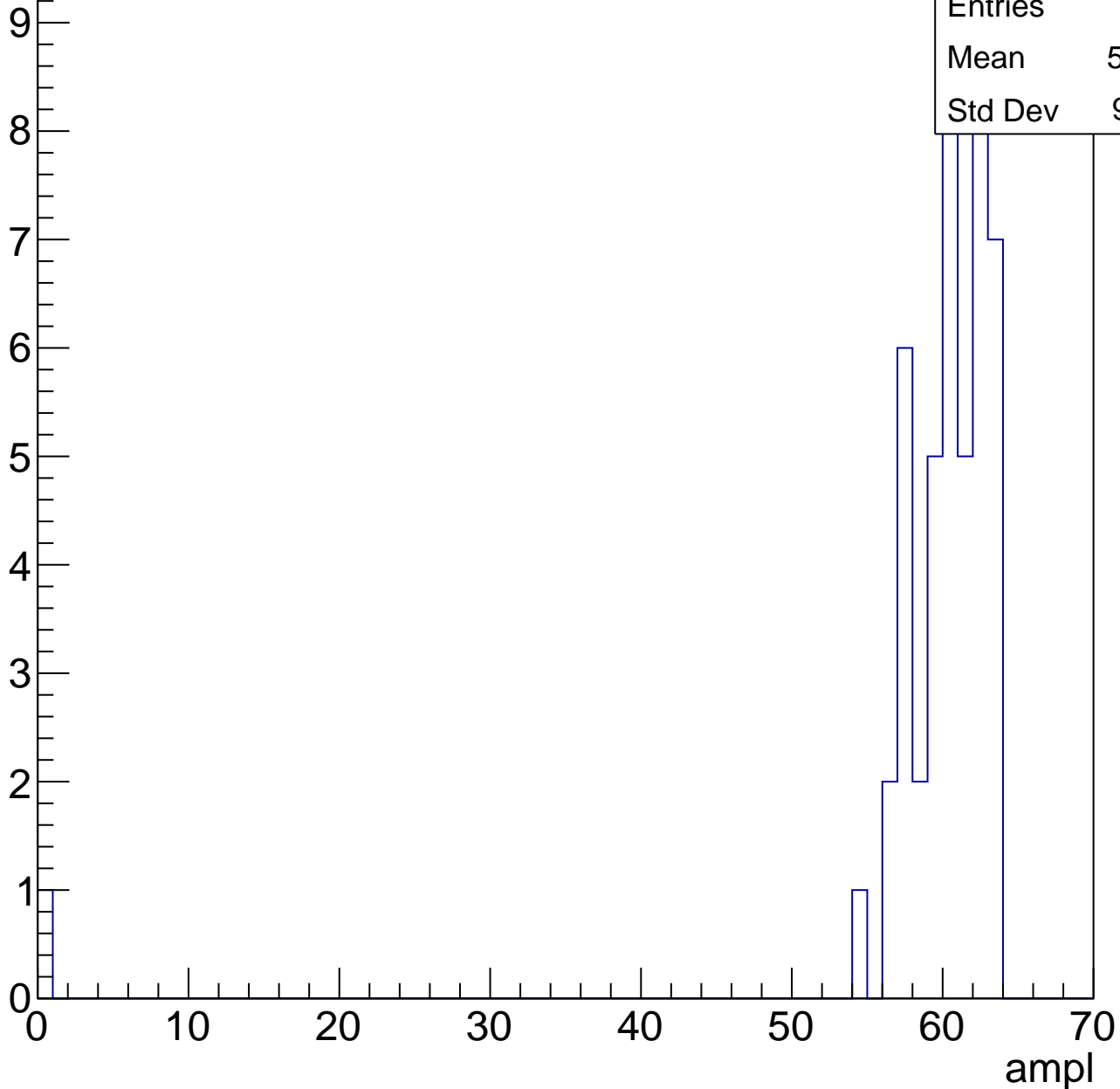


# B1L103S, U11-ch115, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	46
Mean	58.76
Std Dev	9.051



# B1L103S, U11-ch115, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	2
Mean	63
Std Dev	0

0 10 20 30 40 50 60 70

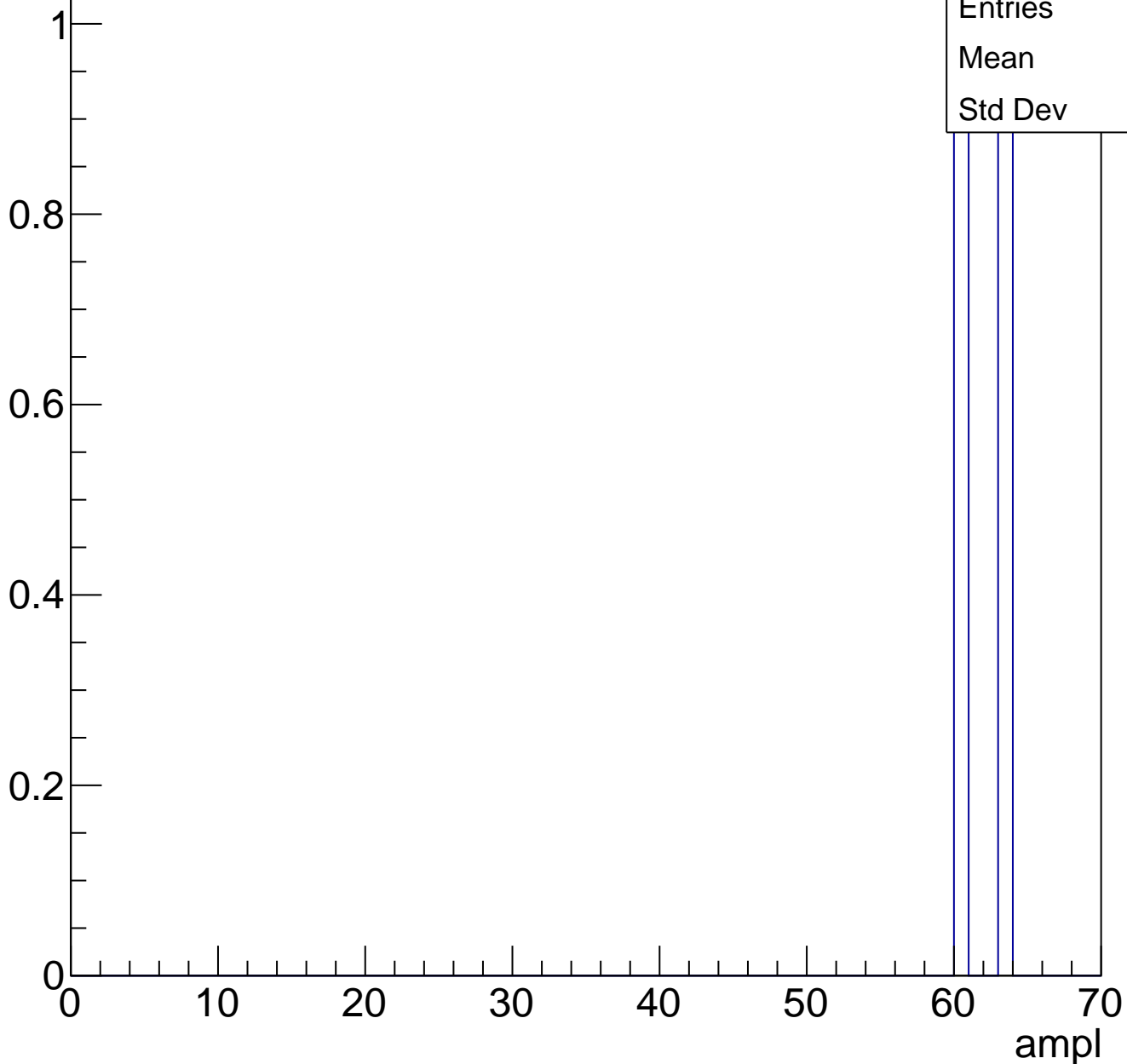
ampl



# B1L103S, U11-ch115, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U11-ch116, adc0

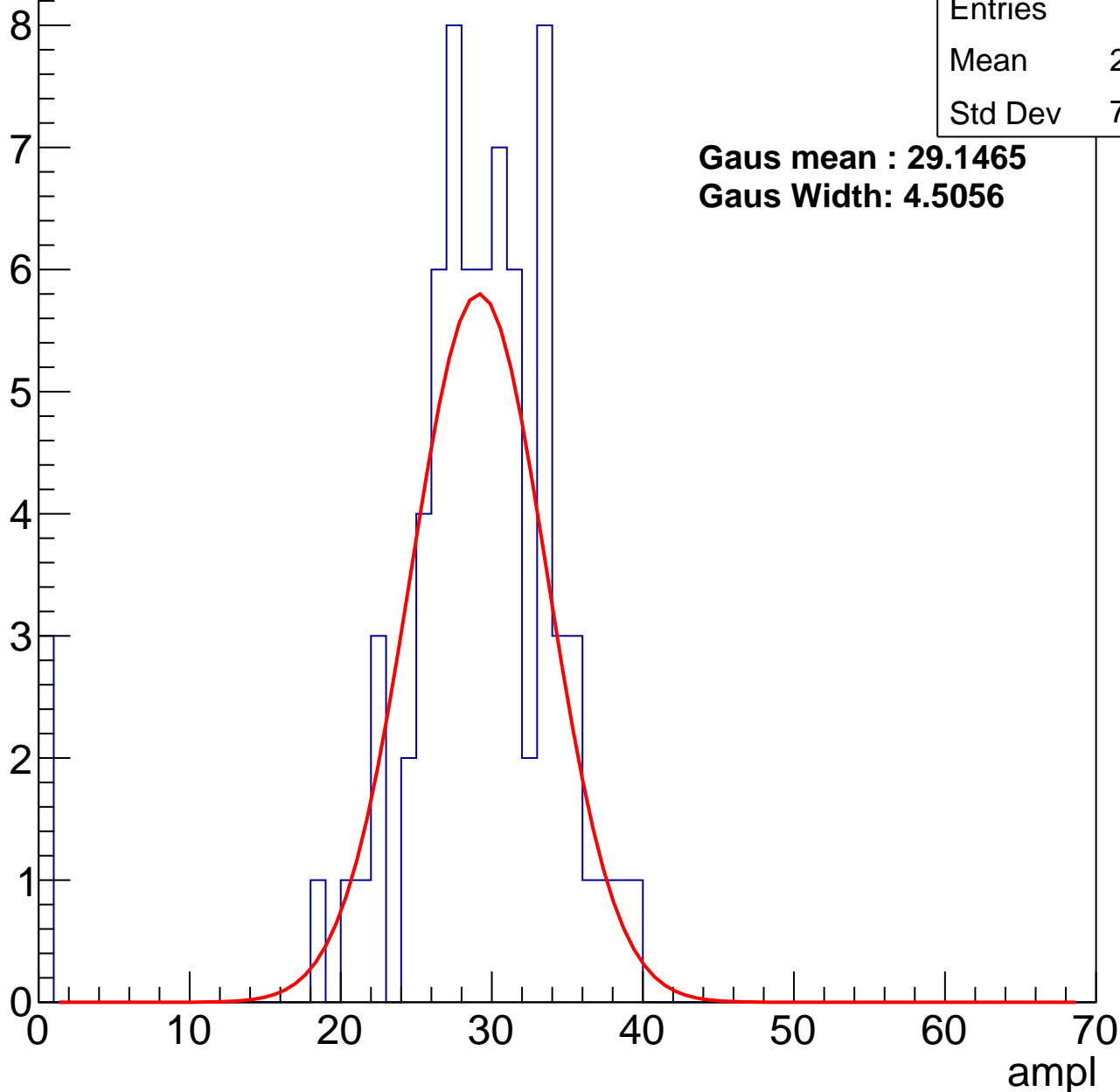
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	74
Mean	27.95
Std Dev	7.084

**Gaus mean : 29.1465**

**Gaus Width: 4.5056**



# B1L103S, U11-ch116, adc1

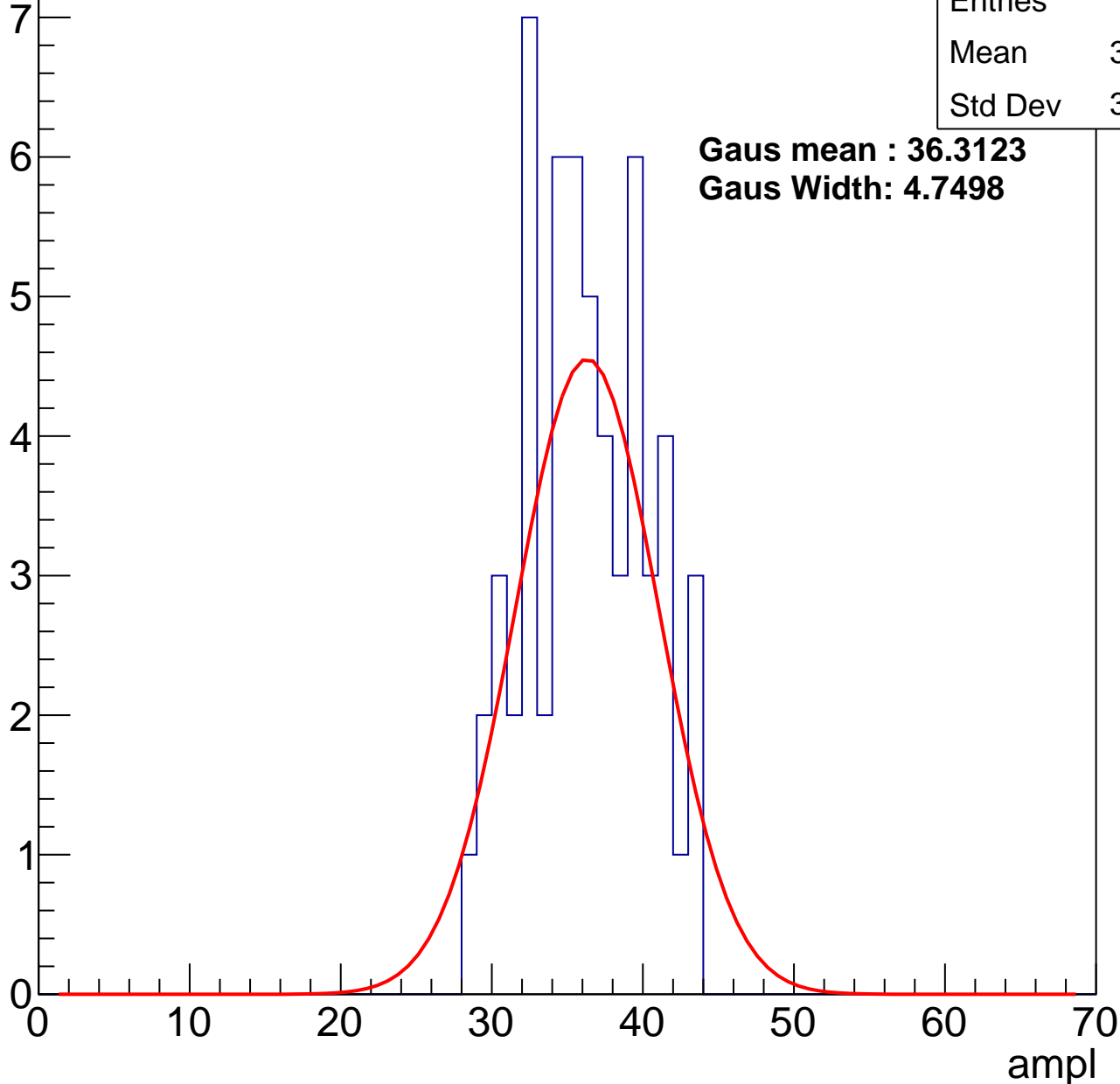
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	58
Mean	35.74
Std Dev	3.889

**Gaus mean : 36.3123**

**Gaus Width: 4.7498**



# B1L103S, U11-ch116, adc2

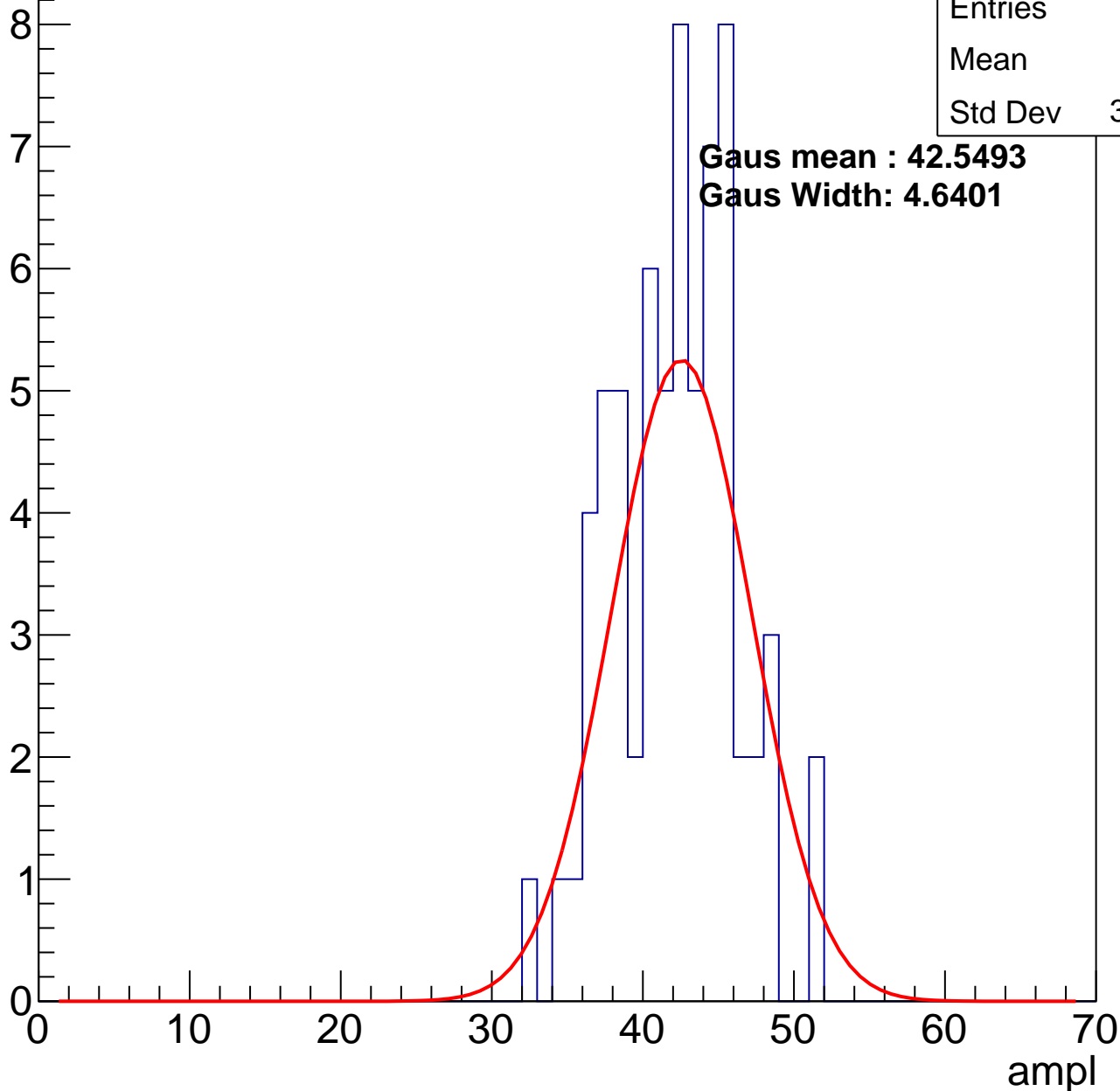
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	41.7
Std Dev	3.978

**Gaus mean : 42.5493**

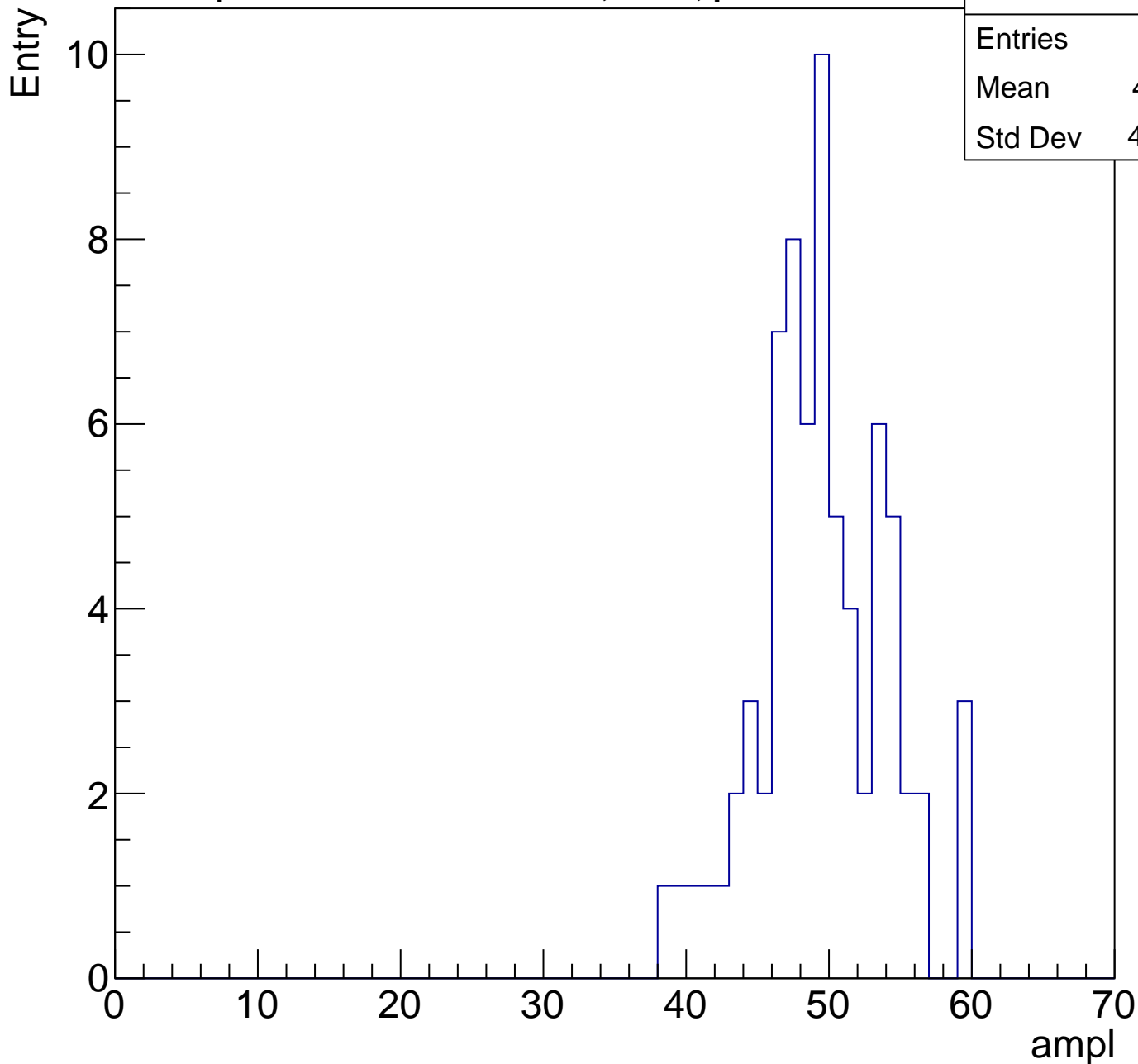
**Gaus Width: 4.6401**



# B1L103S, U11-ch116, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	72
Mean	49.01
Std Dev	4.449

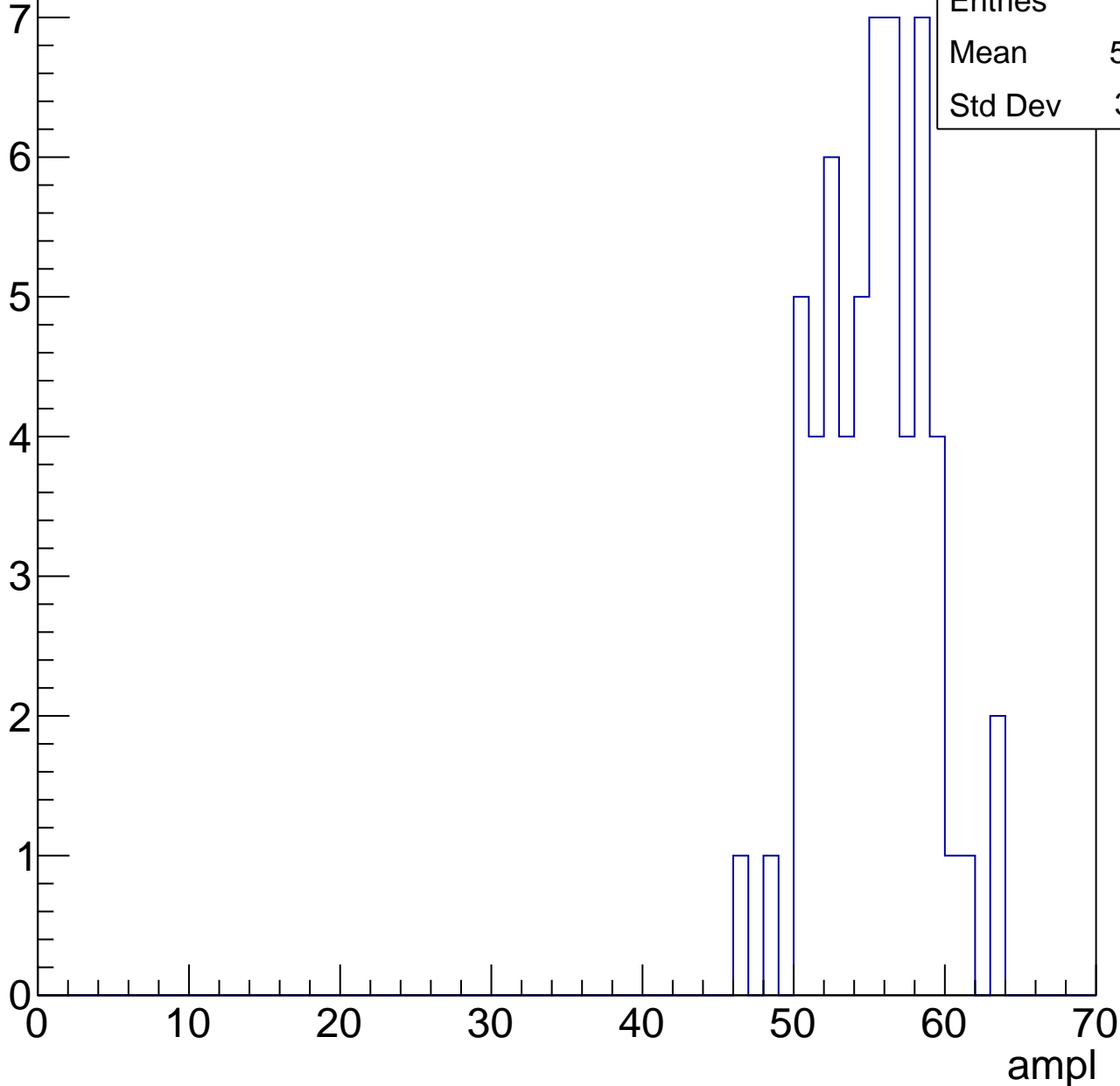


# B1L103S, U11-ch116, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	59
Mean	54.85
Std Dev	3.521

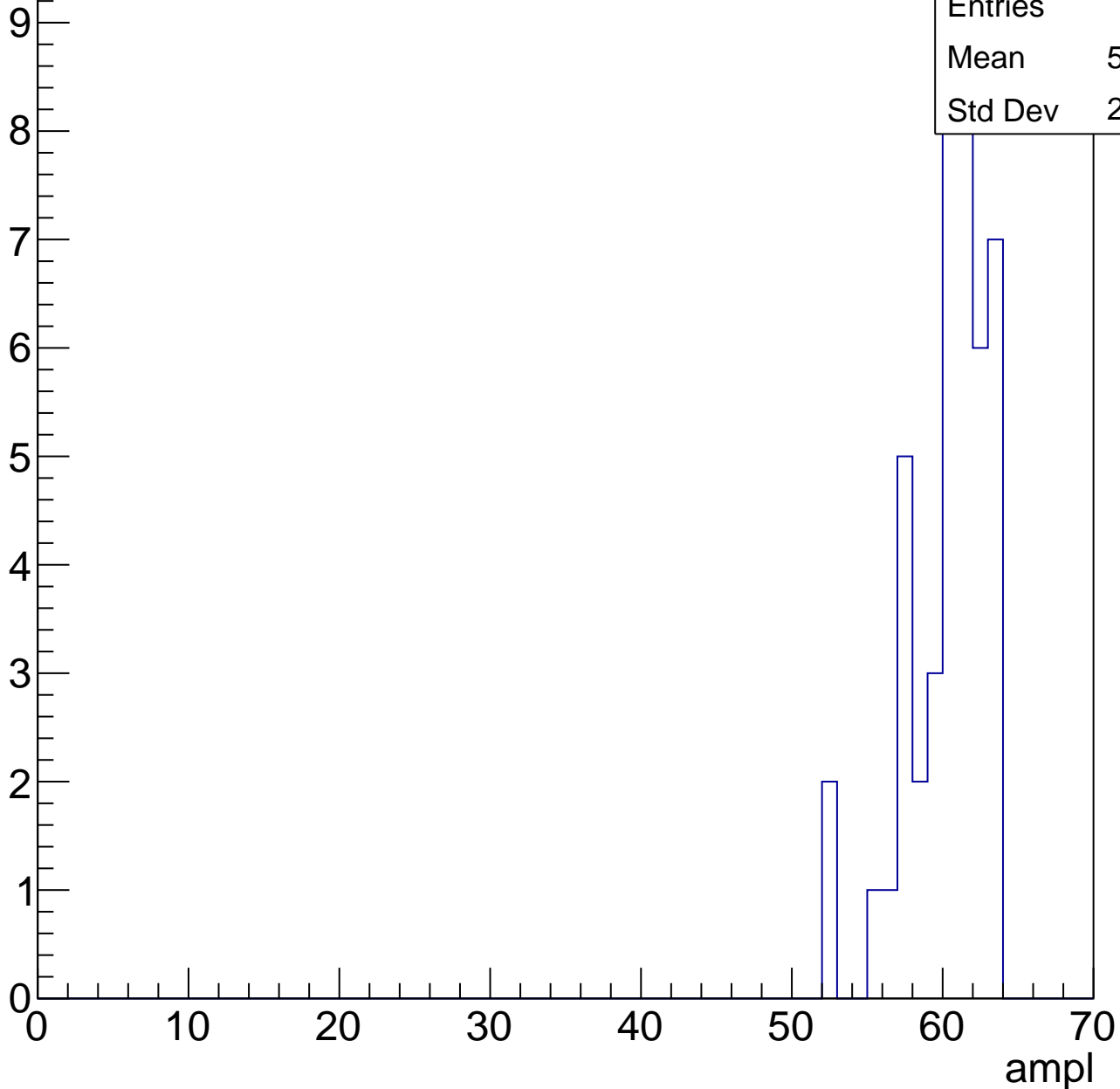


# B1L103S, U11-ch116, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

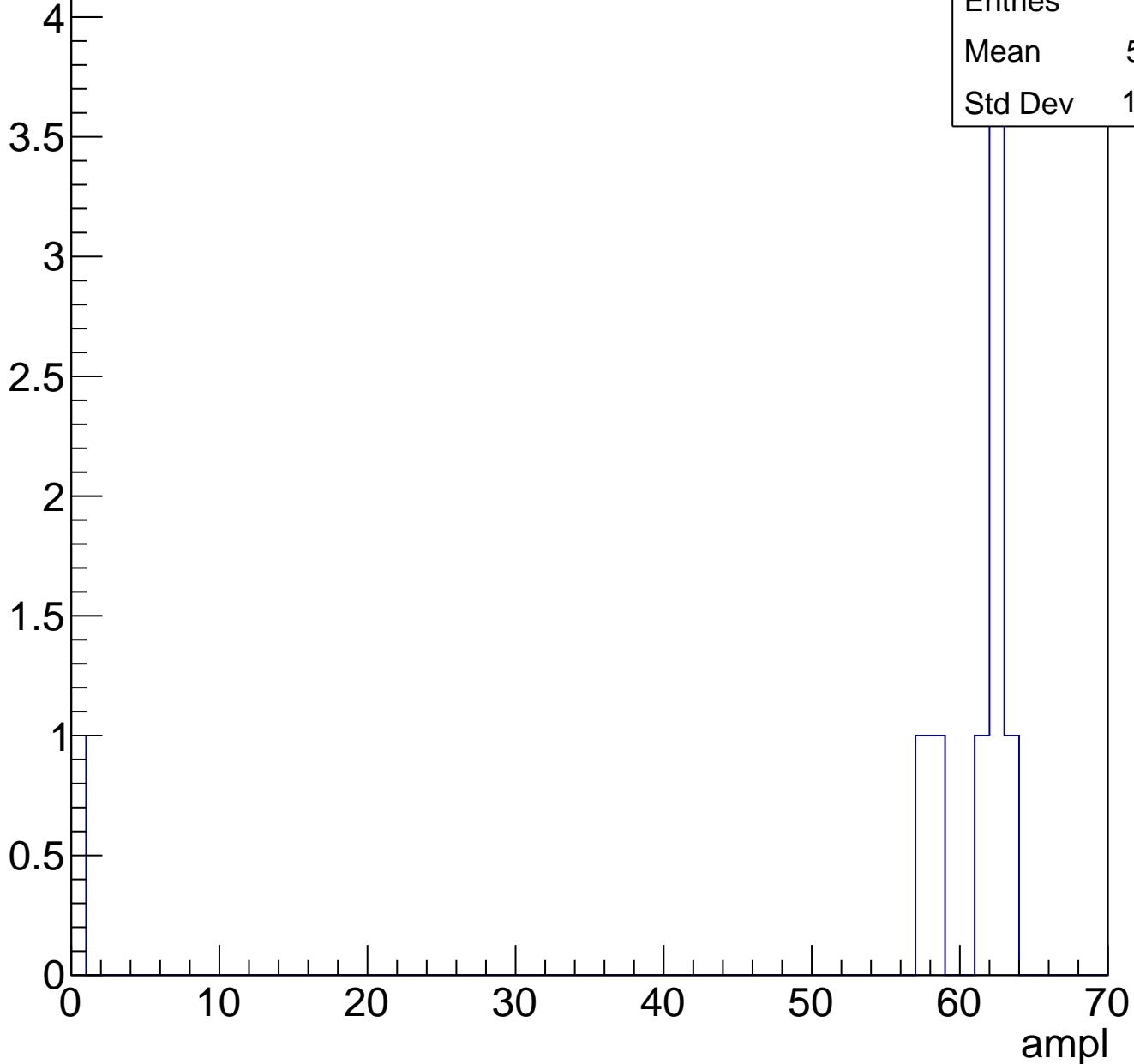
Entries	44
Mean	59.86
Std Dev	2.693



# B1L103S, U11-ch116, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U11-ch116, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U11-ch117, adc0

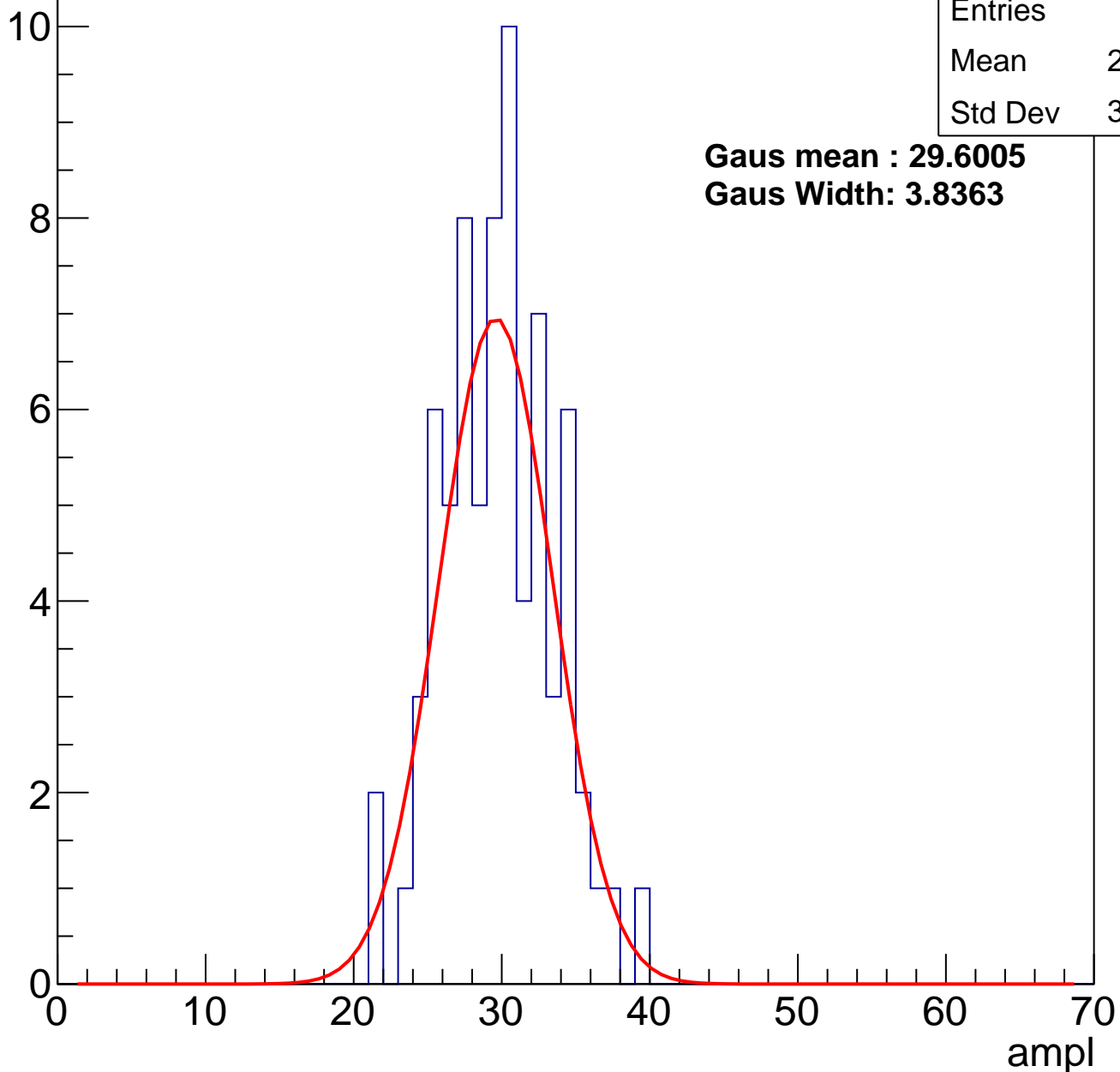
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	73
Mean	29.29
Std Dev	3.669

**Gaus mean : 29.6005**

**Gaus Width: 3.8363**

Entry



# B1L103S, U11-ch117, adc1

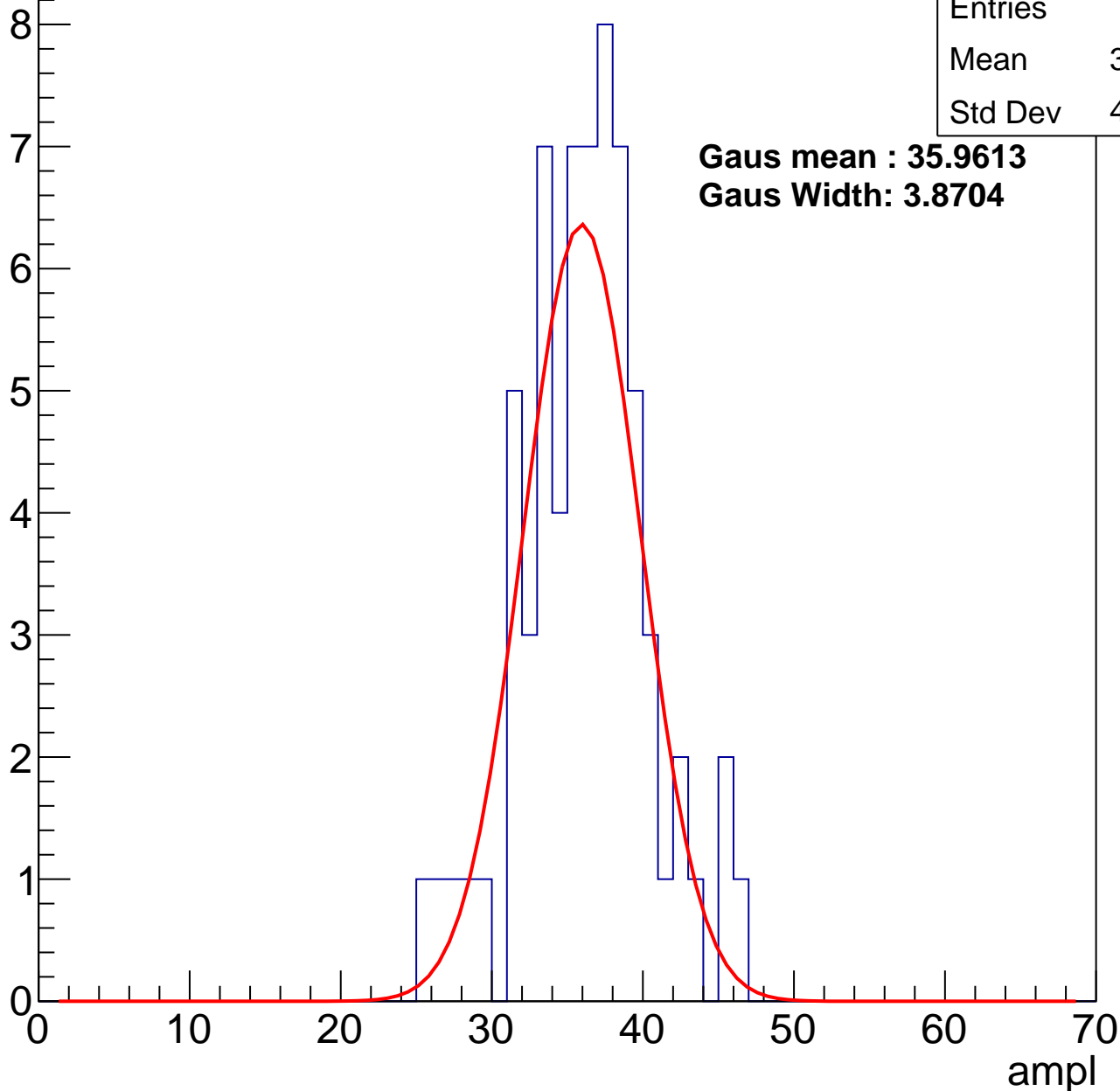
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	68
Mean	35.75
Std Dev	4.213

**Gaus mean : 35.9613**

**Gaus Width: 3.8704**



# B1L103S, U11-ch117, adc2

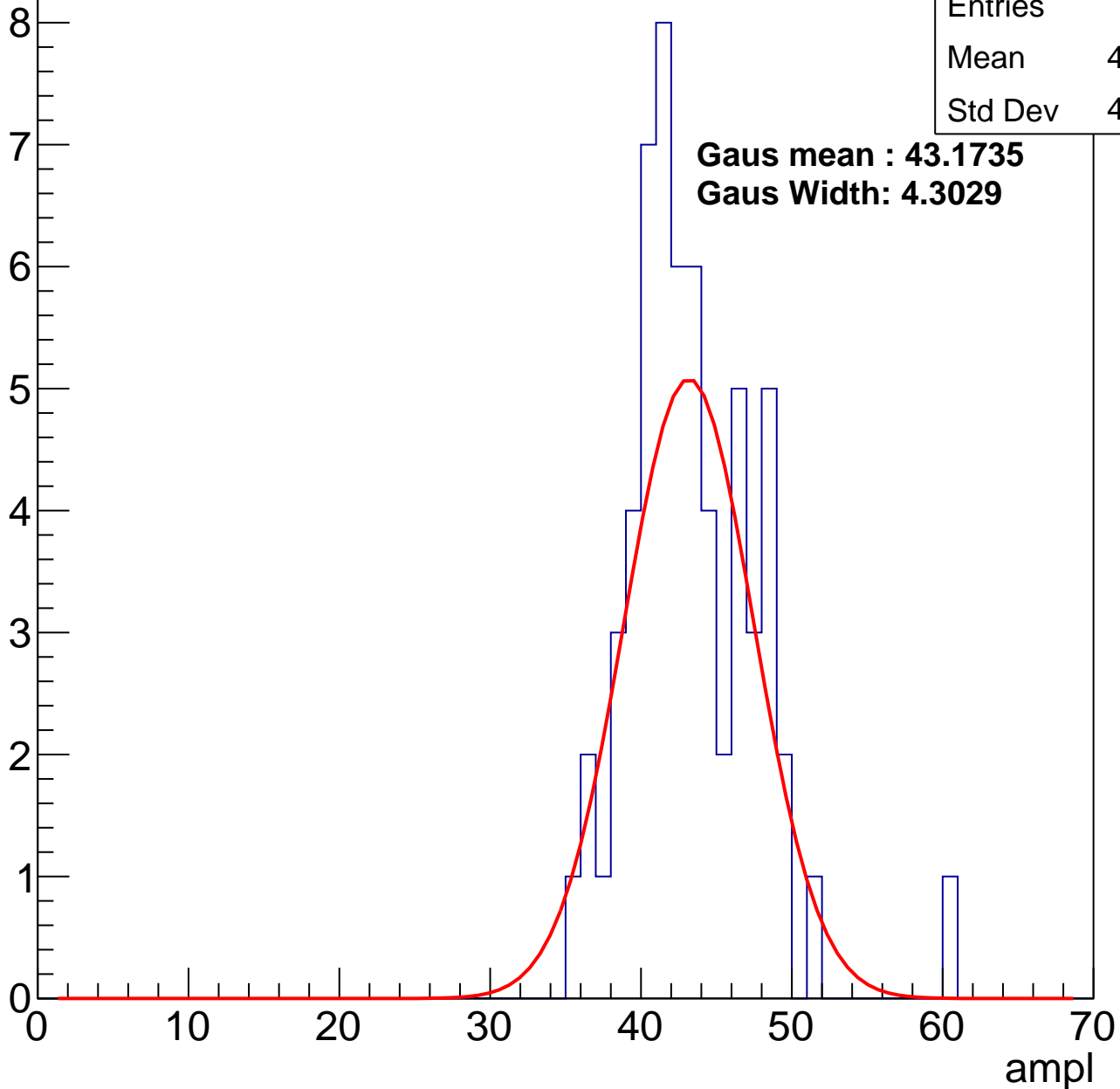
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	61
Mean	42.92
Std Dev	4.232

**Gaus mean : 43.1735**

**Gaus Width: 4.3029**

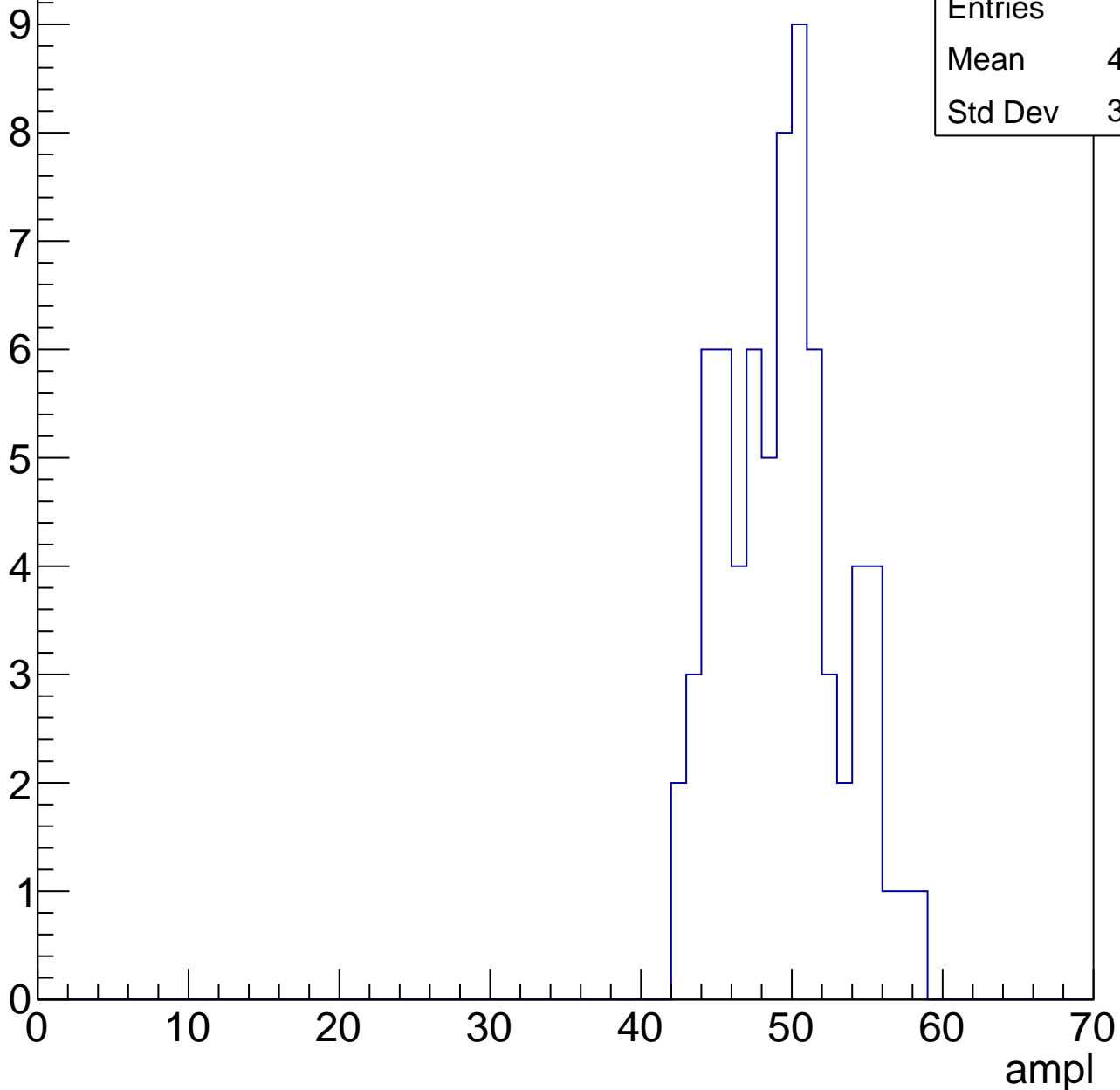


# B1L103S, U11-ch117, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	71
Mean	48.87
Std Dev	3.838

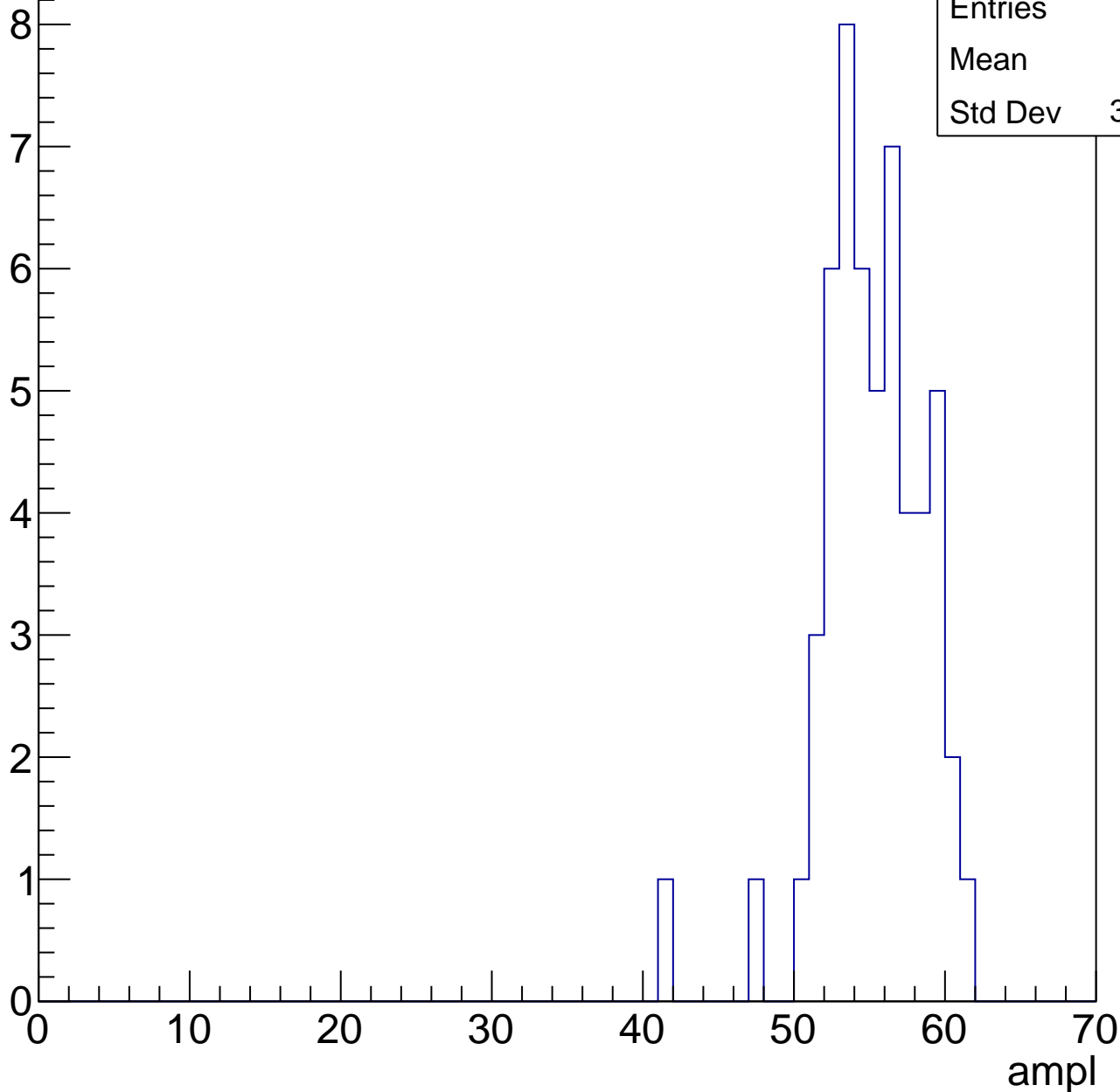


# B1L103S, U11-ch117, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	54
Mean	54.7
Std Dev	3.457

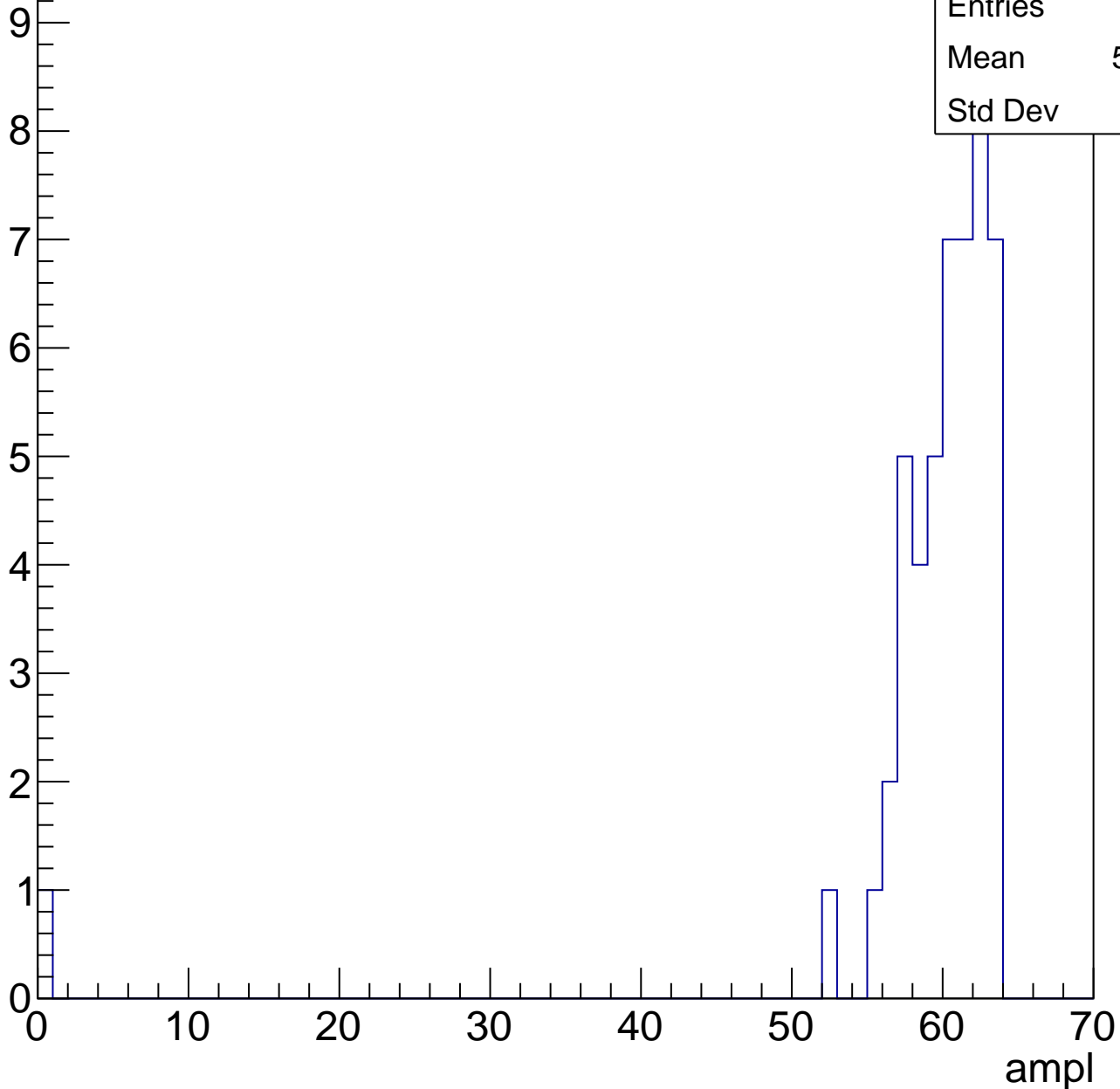


# B1L103S, U11-ch117, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

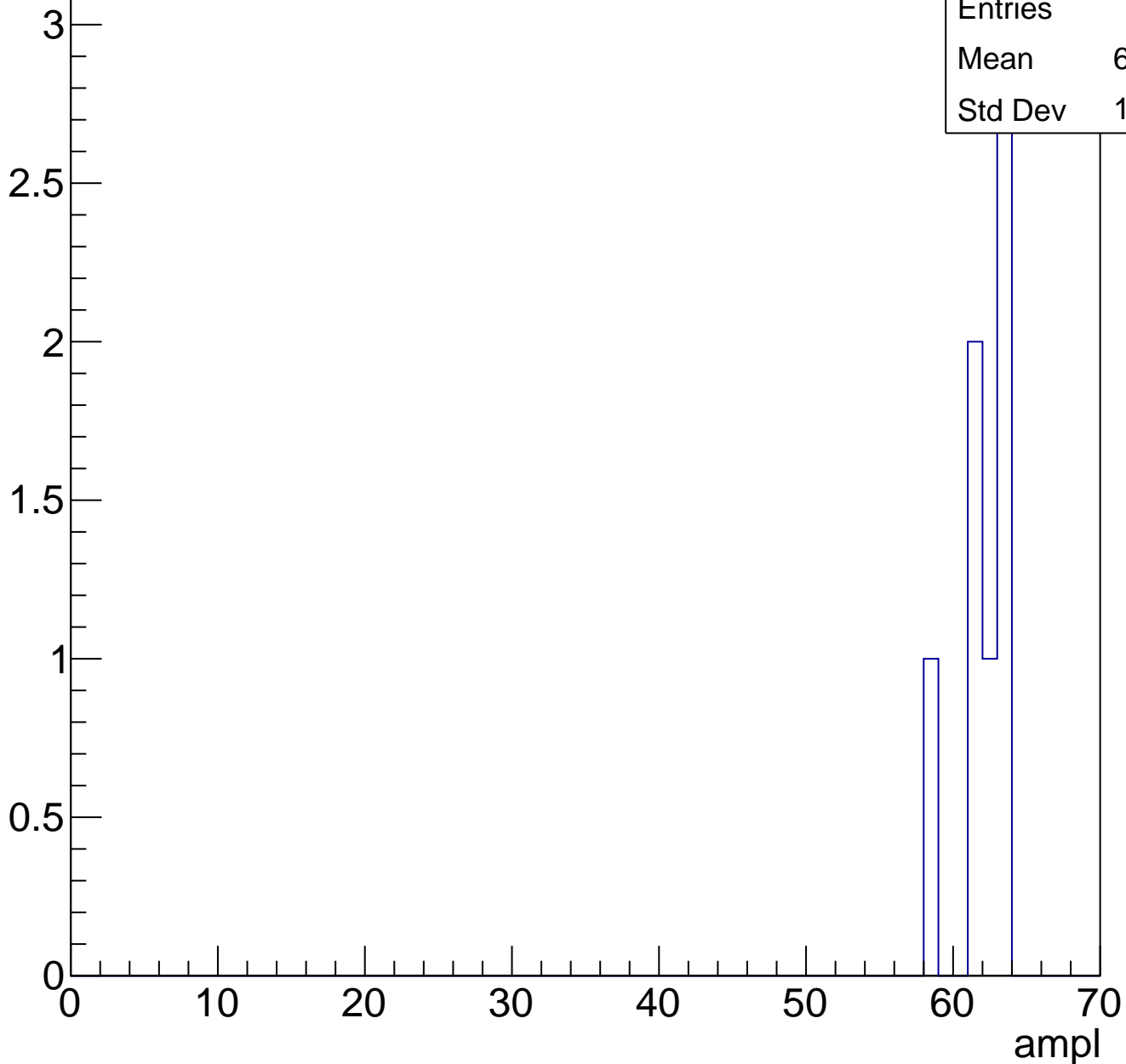
Entries	49
Mean	58.71
Std Dev	8.82



# B1L103S, U11-ch117, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U11-ch117, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U11-ch118, adc0

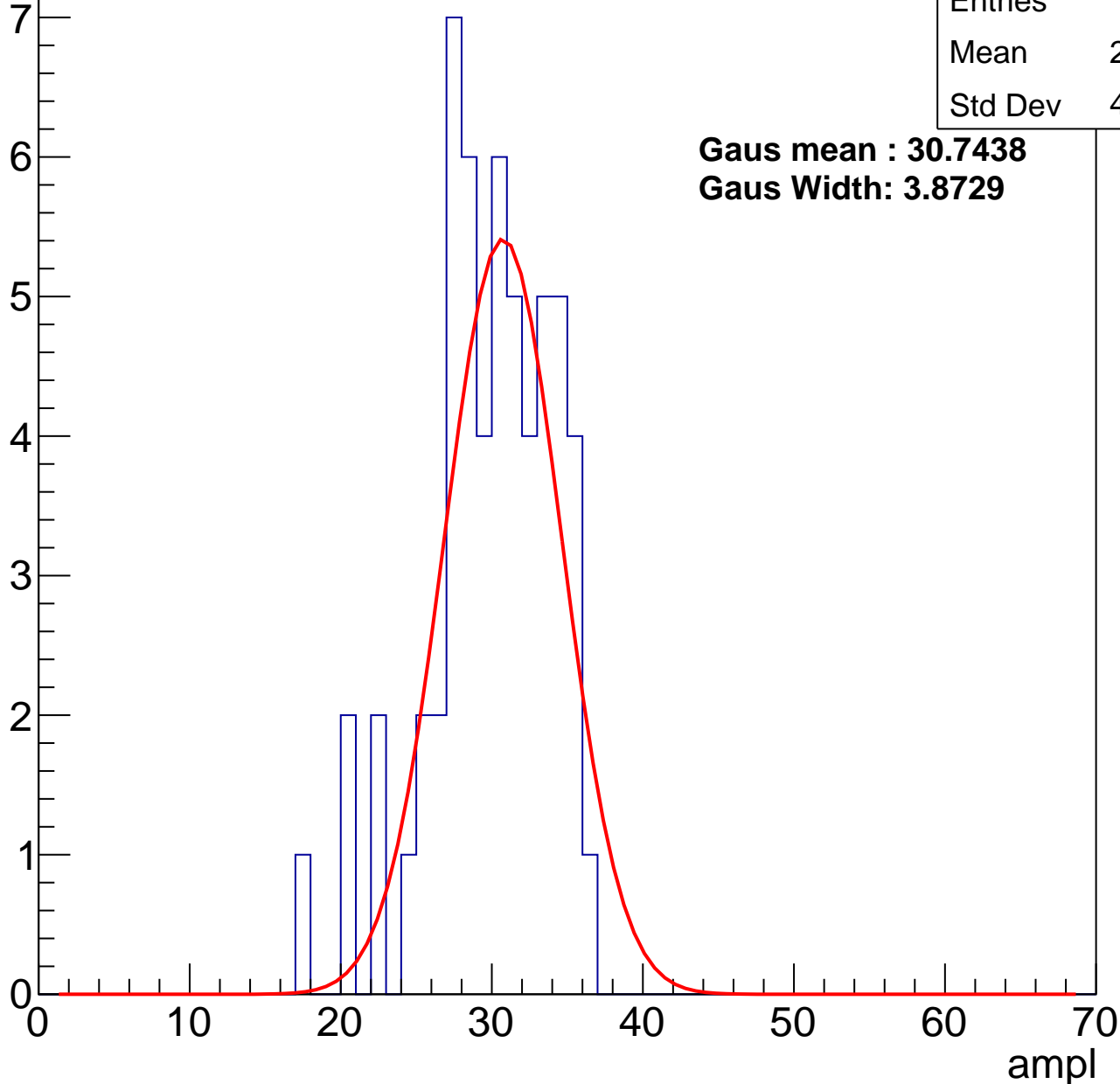
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	57
Mean	29.37
Std Dev	4.115

**Gaus mean : 30.7438**

**Gaus Width: 3.8729**



# B1L103S, U11-ch118, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	78
Mean	36.73
Std Dev	4.125

**Gaus mean : 36.9719**

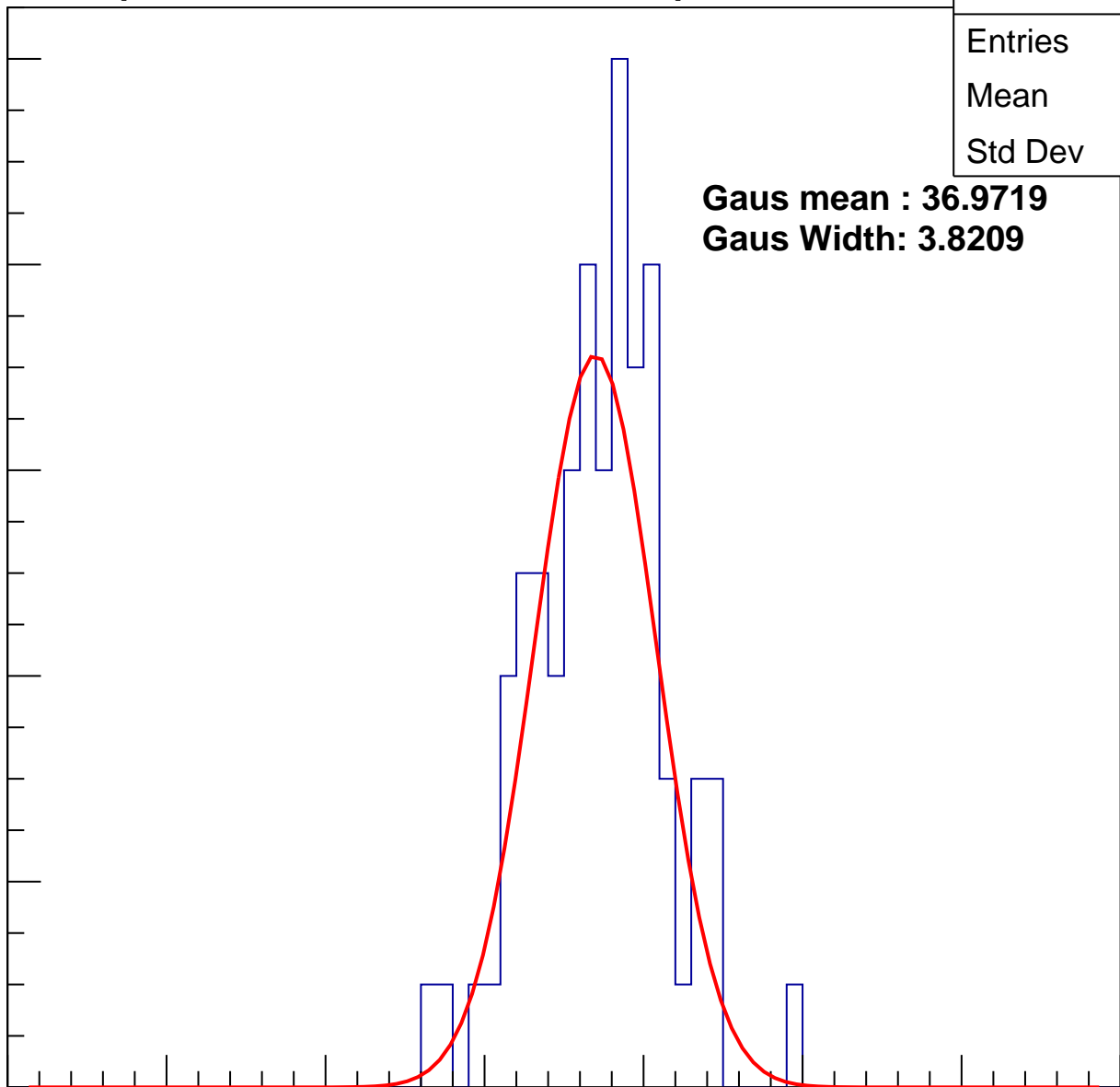
**Gaus Width: 3.8209**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U11-ch118, adc2

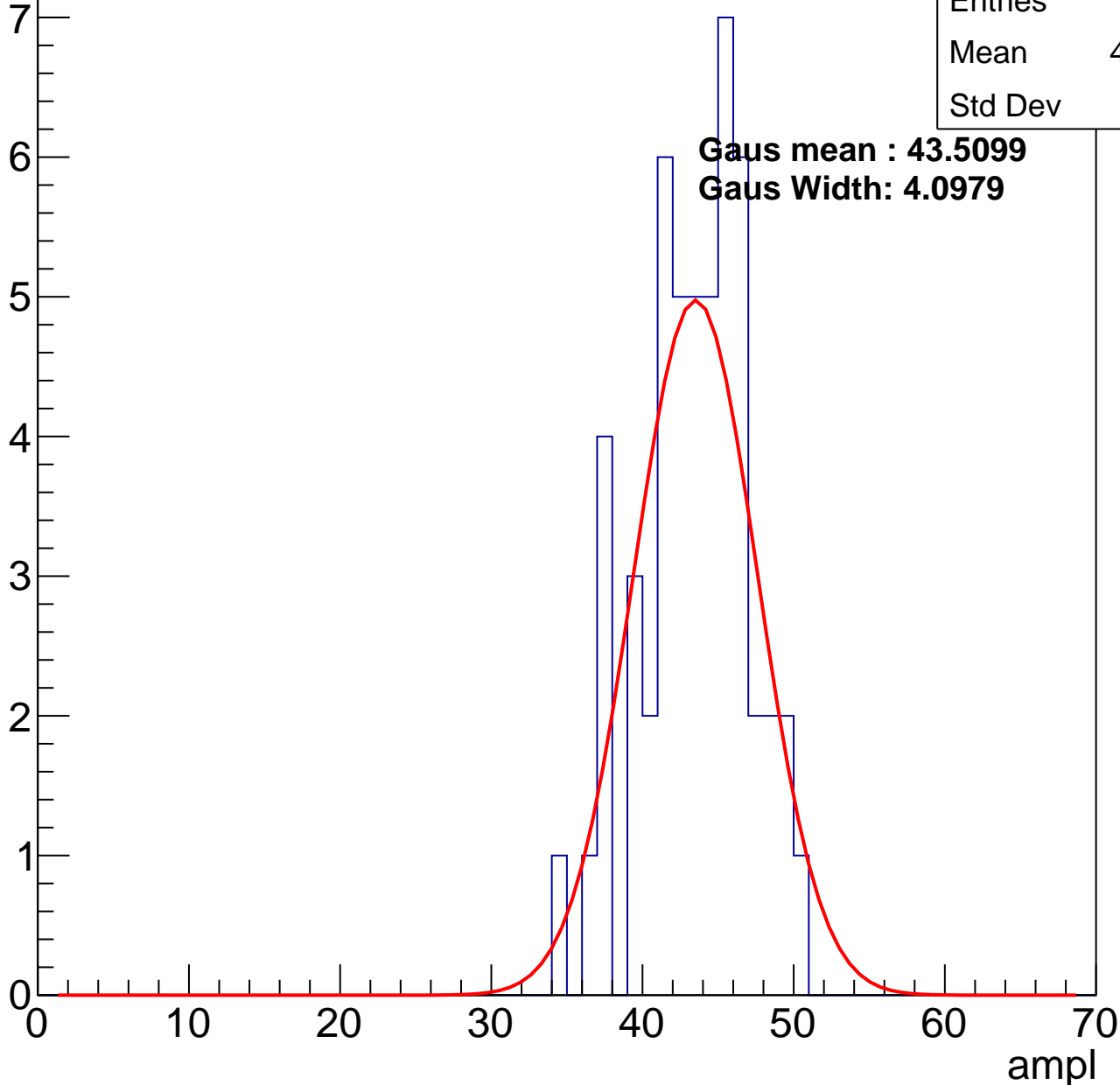
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	52
Mean	42.98
Std Dev	3.56

**Gaus mean : 43.5099**

**Gaus Width: 4.0979**

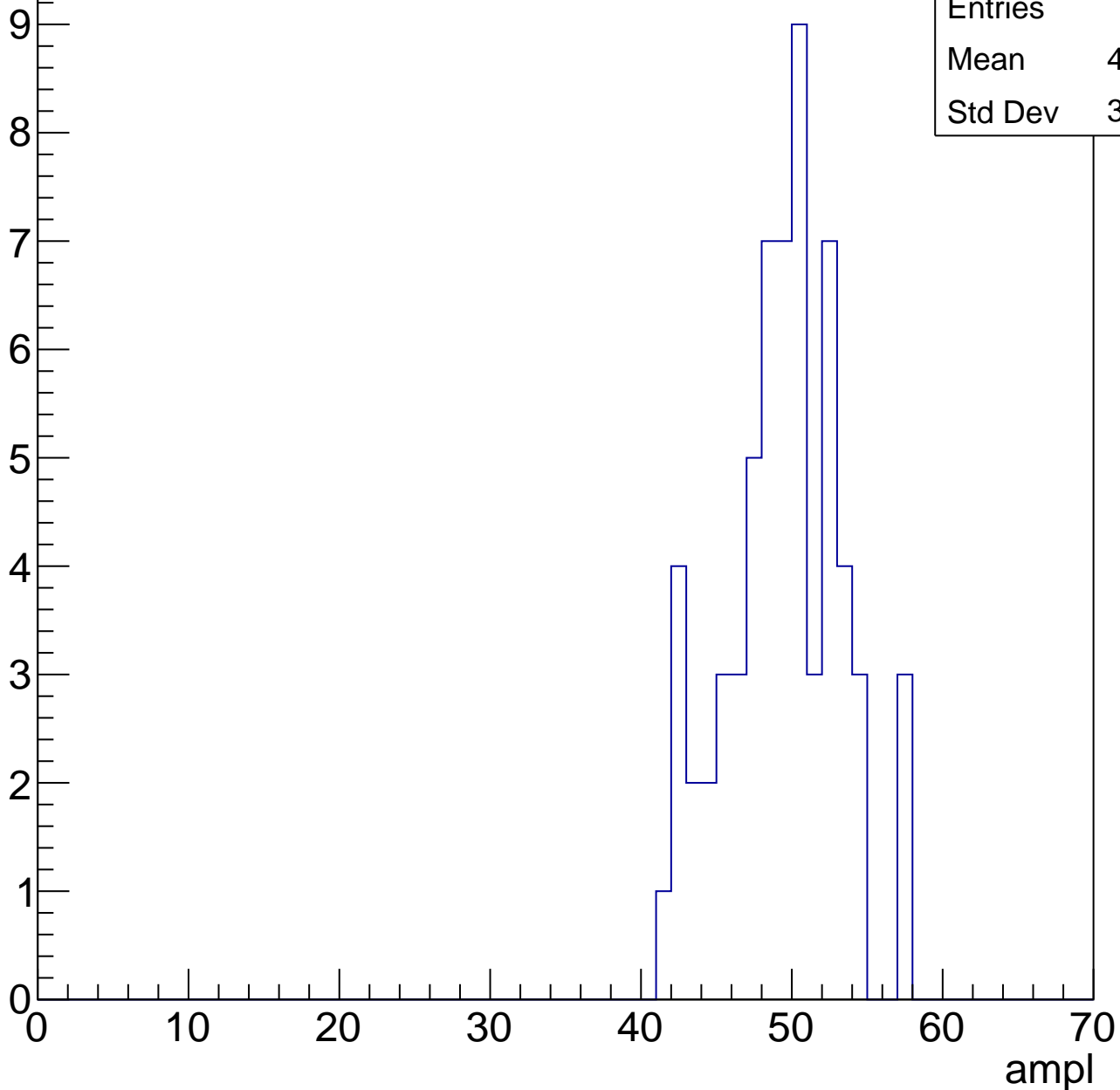


# B1L103S, U11-ch118, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	48.92
Std Dev	3.777

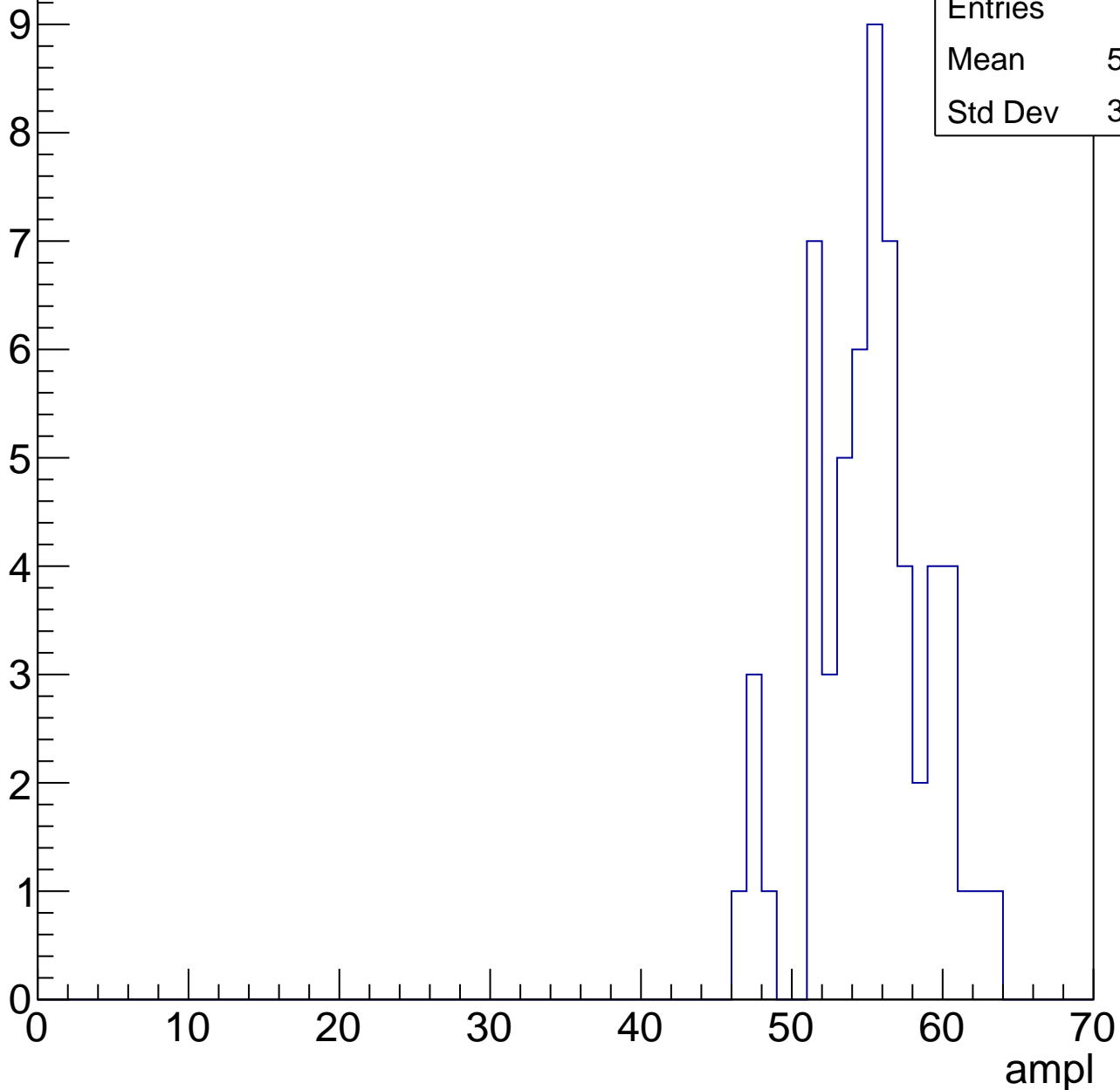


# B1L103S, U11-ch118, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

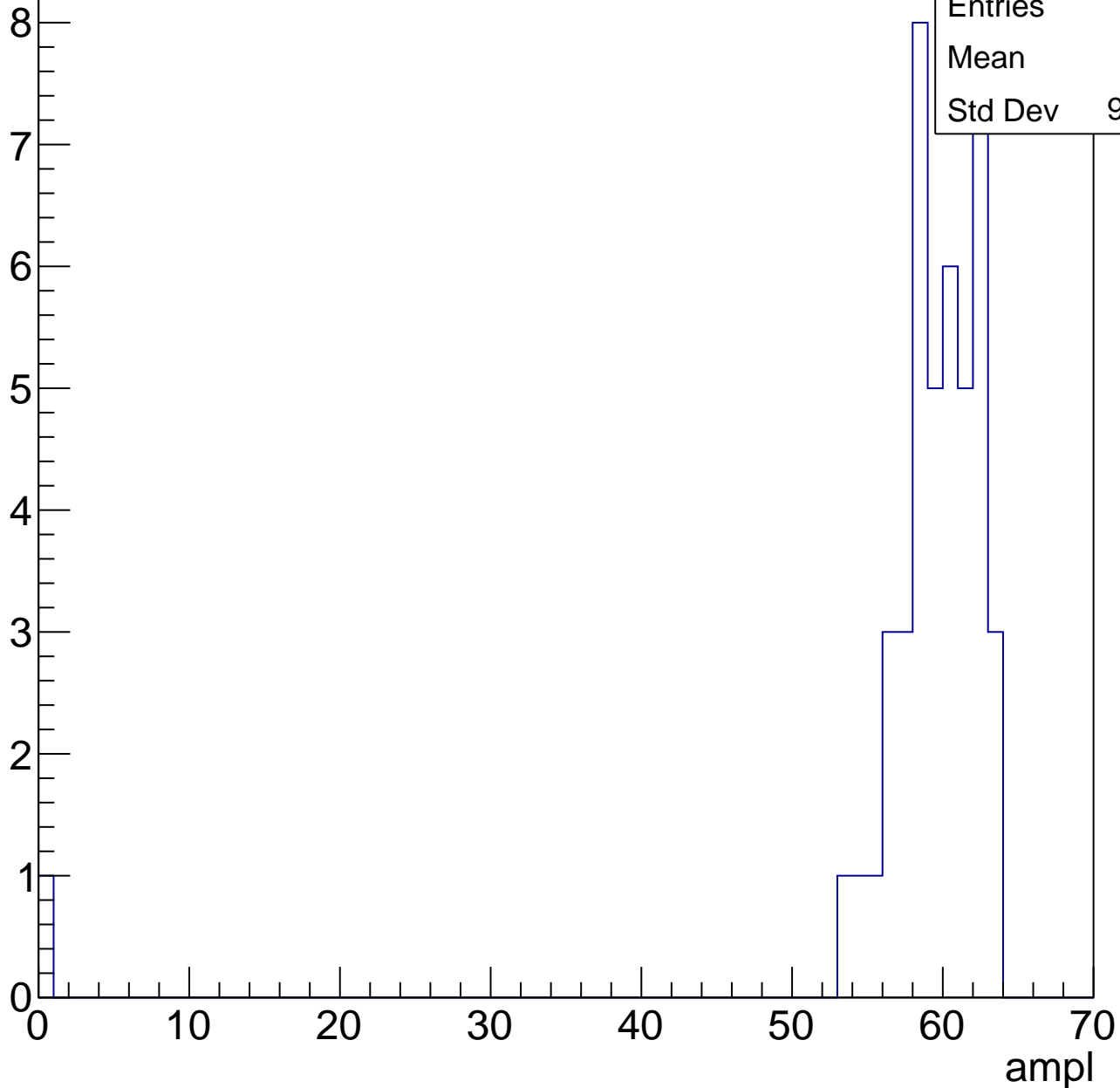
Entries	59
Mean	54.75
Std Dev	3.767



# B1L103S, U11-ch118, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

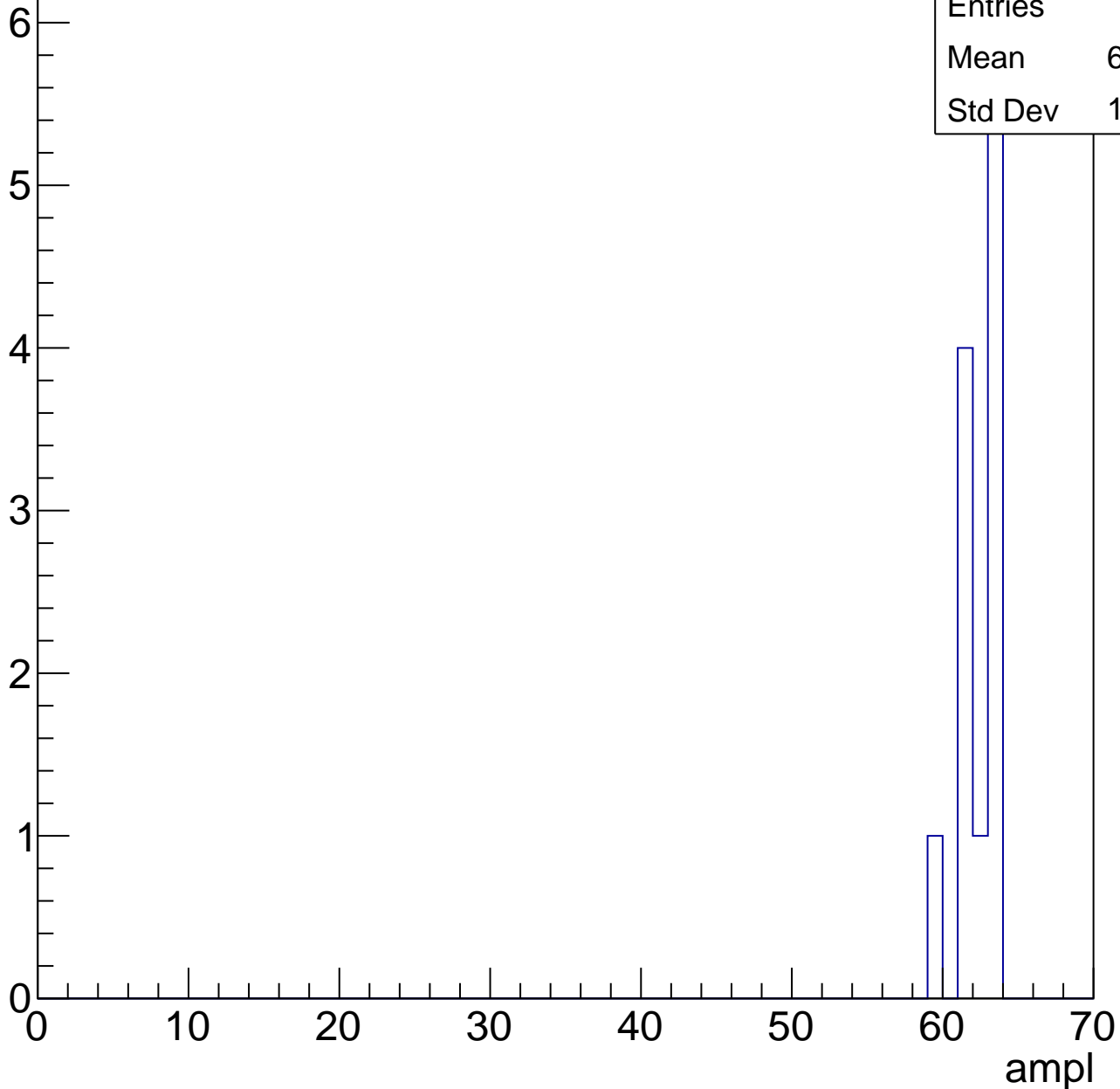


# B1L103S, U11-ch118, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	12
Mean	61.92
Std Dev	1.256





# B1L103S, U11-ch118, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L103S, U11-ch119, adc0

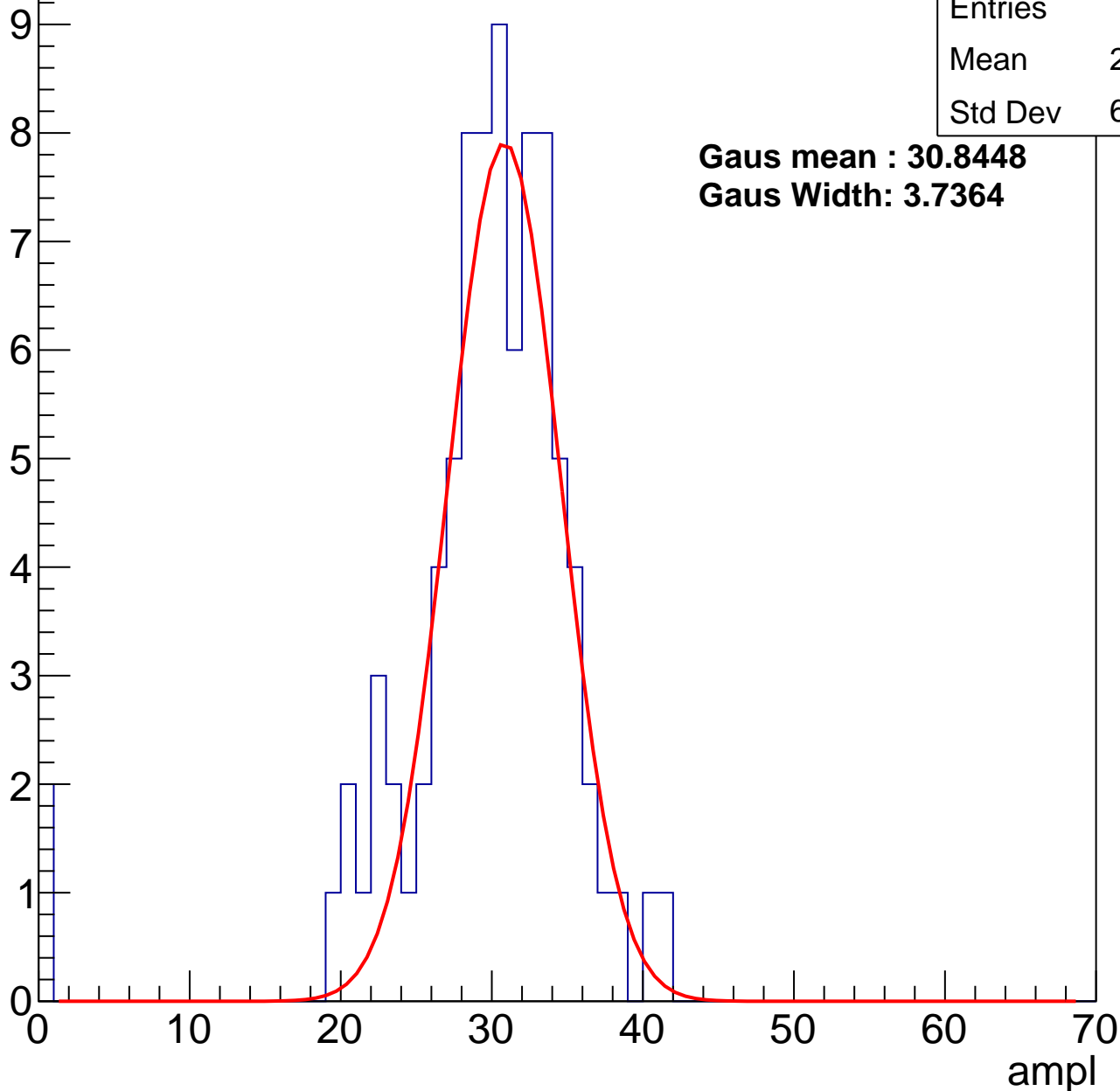
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	85
Mean	29.12
Std Dev	6.284

**Gaus mean : 30.8448**

**Gaus Width: 3.7364**



# B1L103S, U11-ch119, adc1

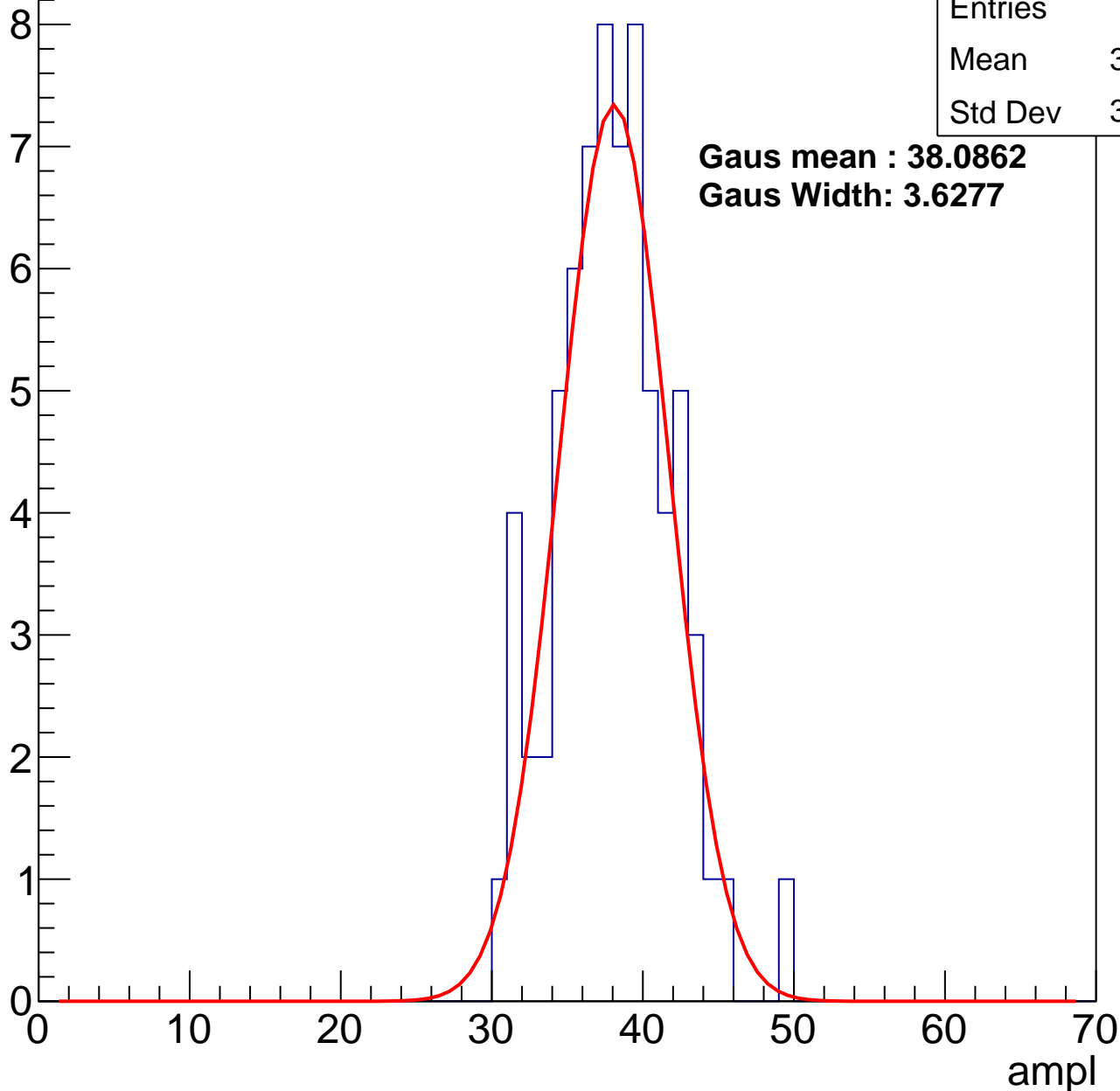
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	70
Mean	37.59
Std Dev	3.713

**Gaus mean : 38.0862**

**Gaus Width: 3.6277**



# B1L103S, U11-ch119, adc2

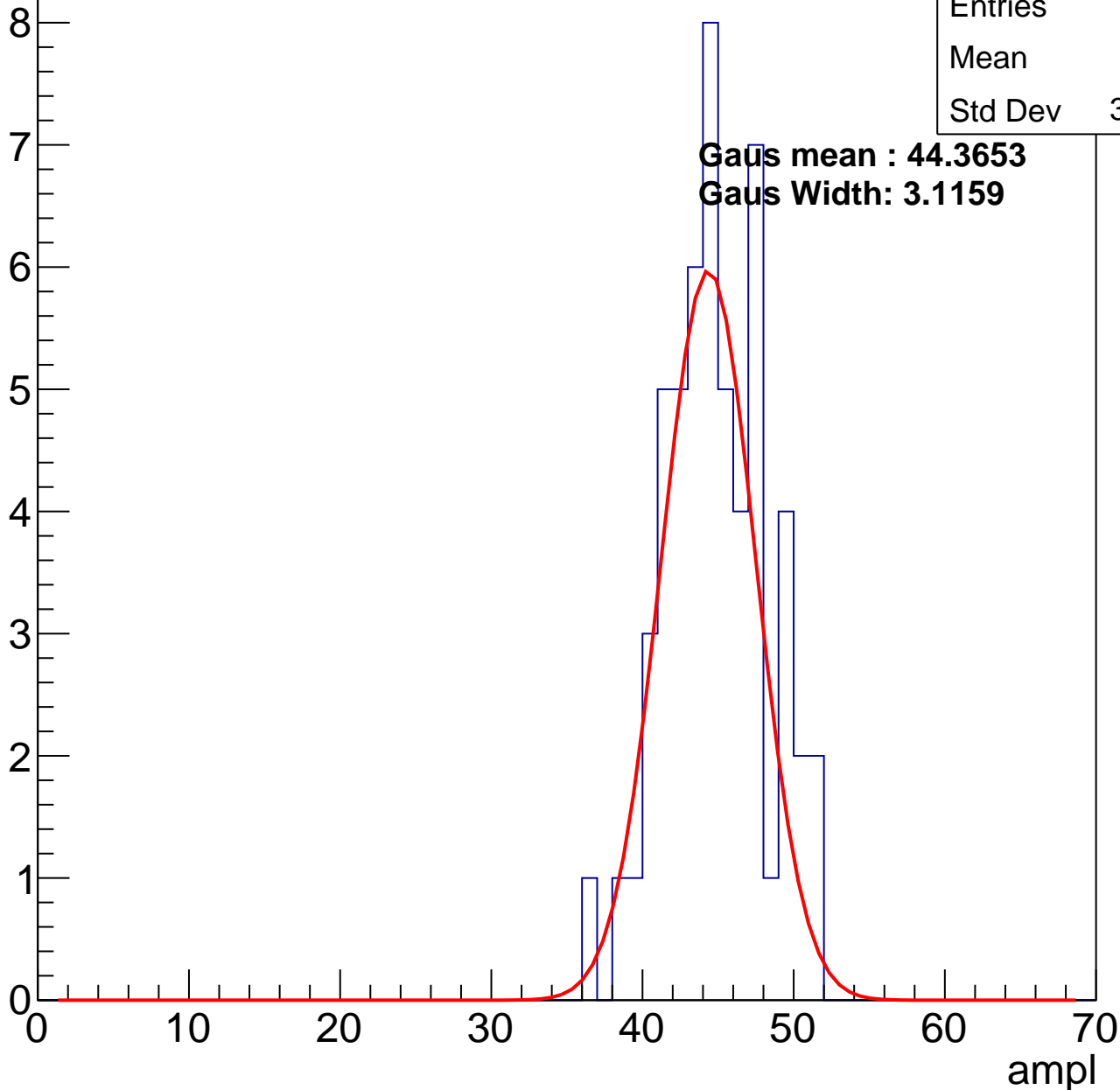
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	55
Mean	44.4
Std Dev	3.317

**Gaus mean : 44.3653**

**Gaus Width: 3.1159**

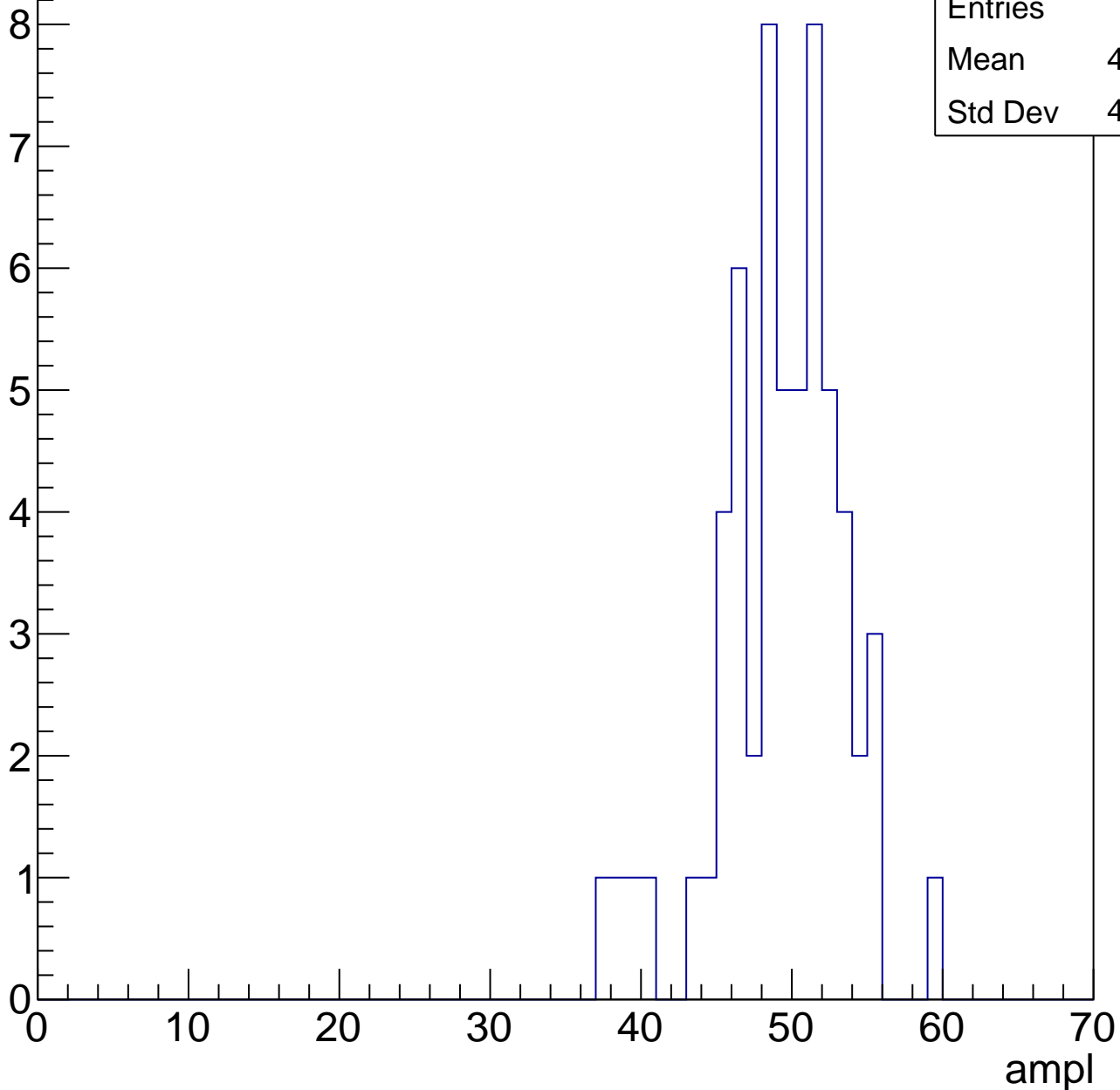


# B1L103S, U11-ch119, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	59
Mean	48.85
Std Dev	4.206

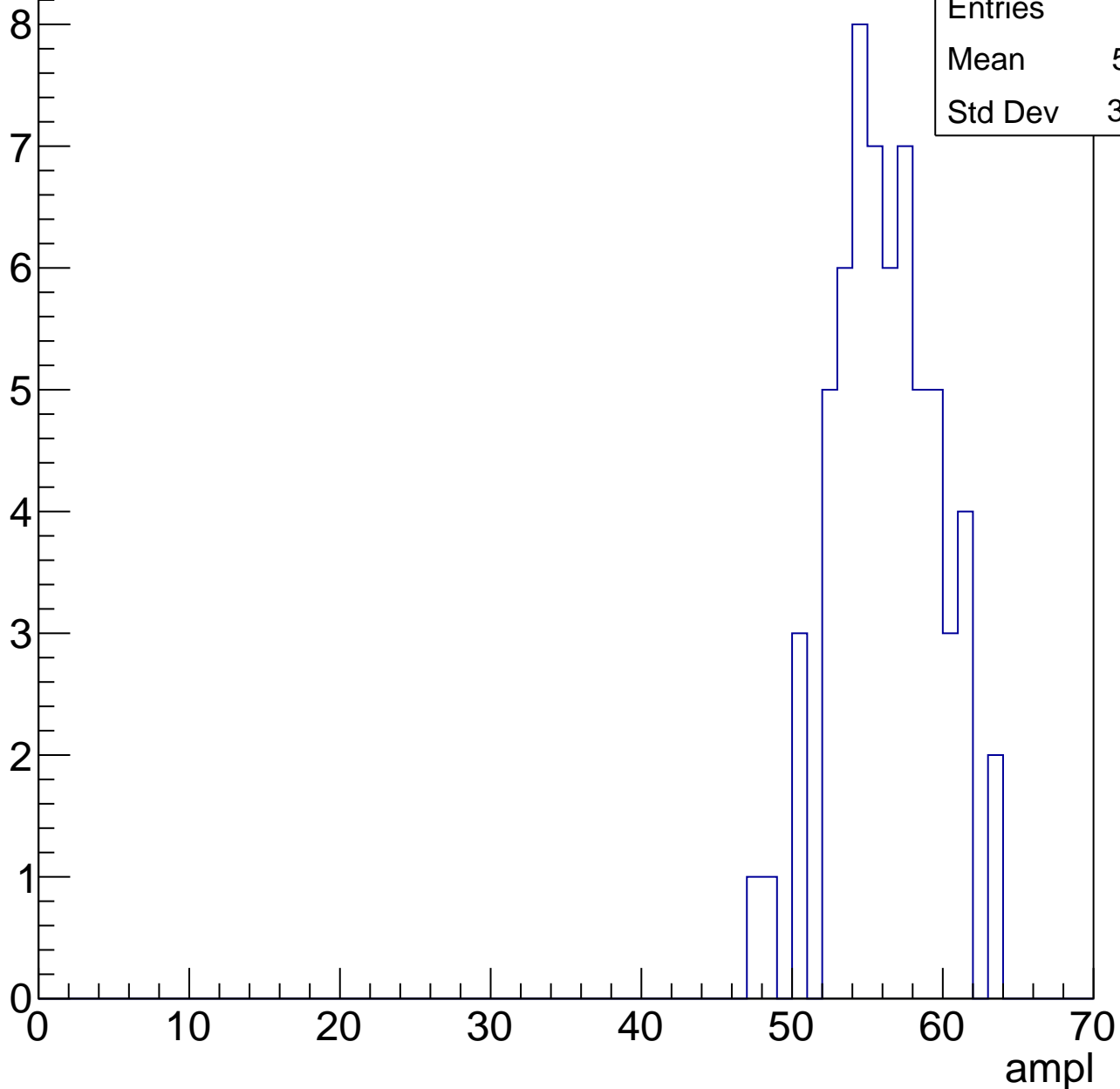


# B1L103S, U11-ch119, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	55.71
Std Dev	3.425

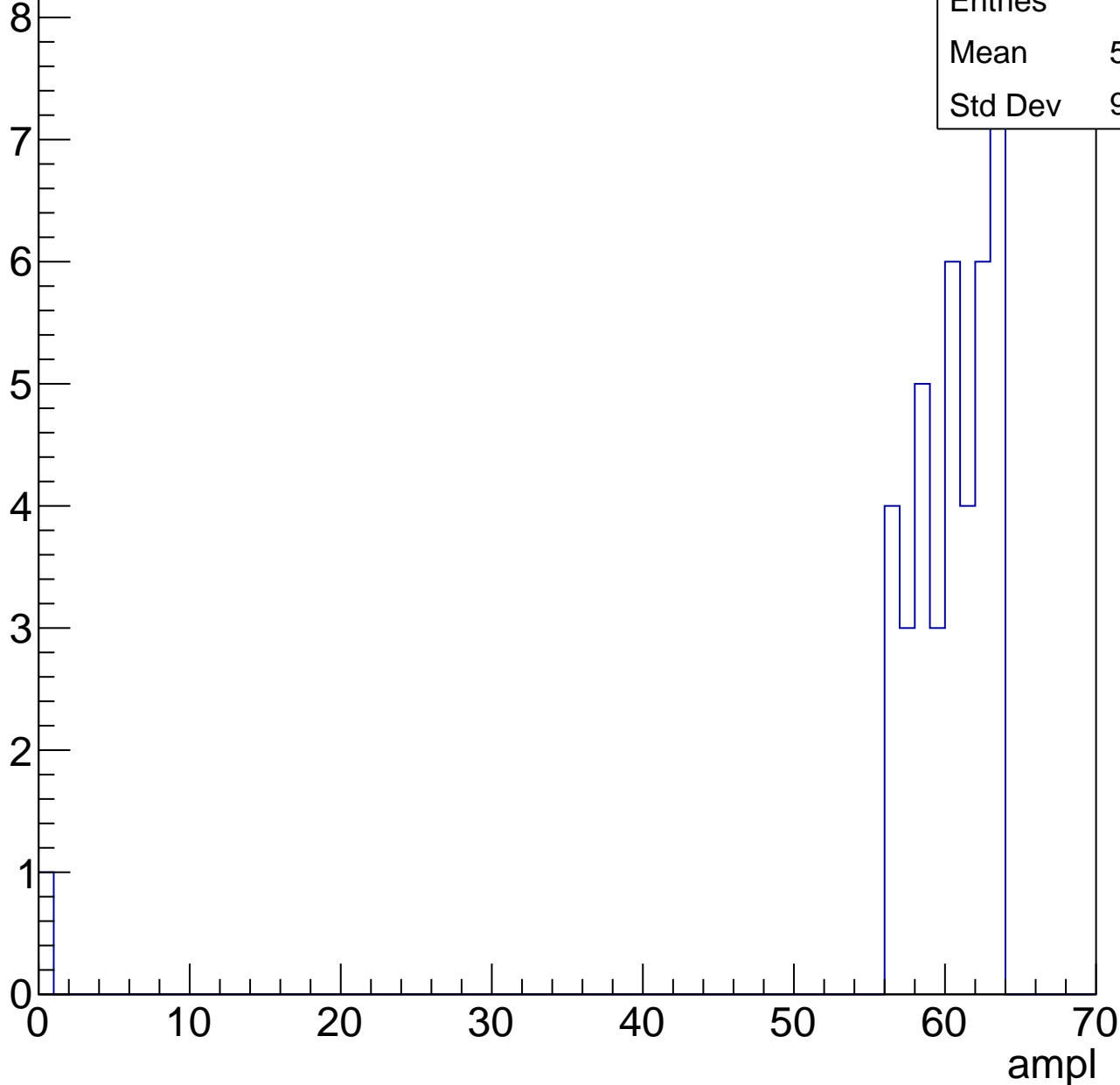


# B1L103S, U11-ch119, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

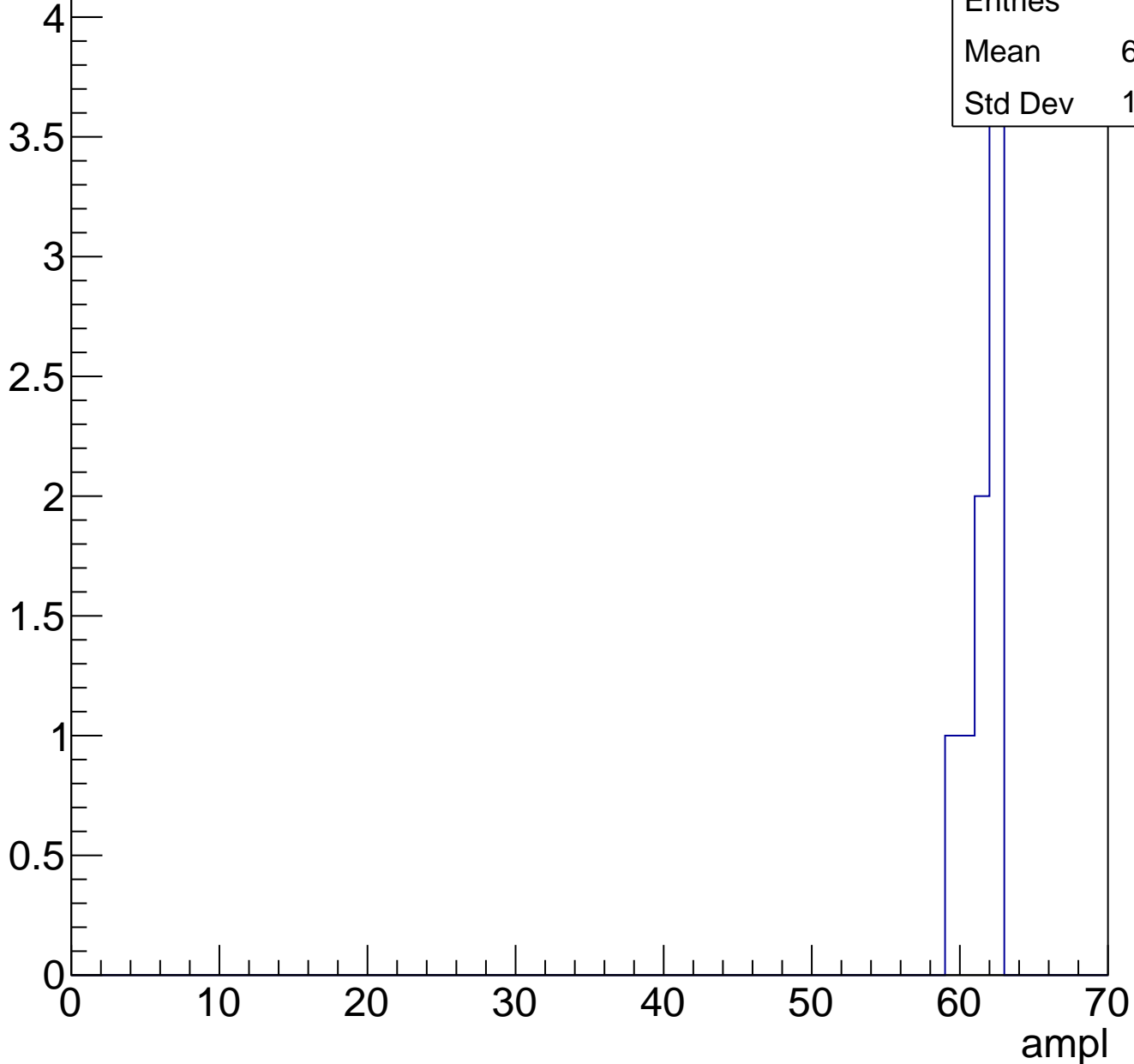
Entries	40
Mean	58.55
Std Dev	9.656



# B1L103S, U11-ch119, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U11-ch119, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U11-ch120, adc0

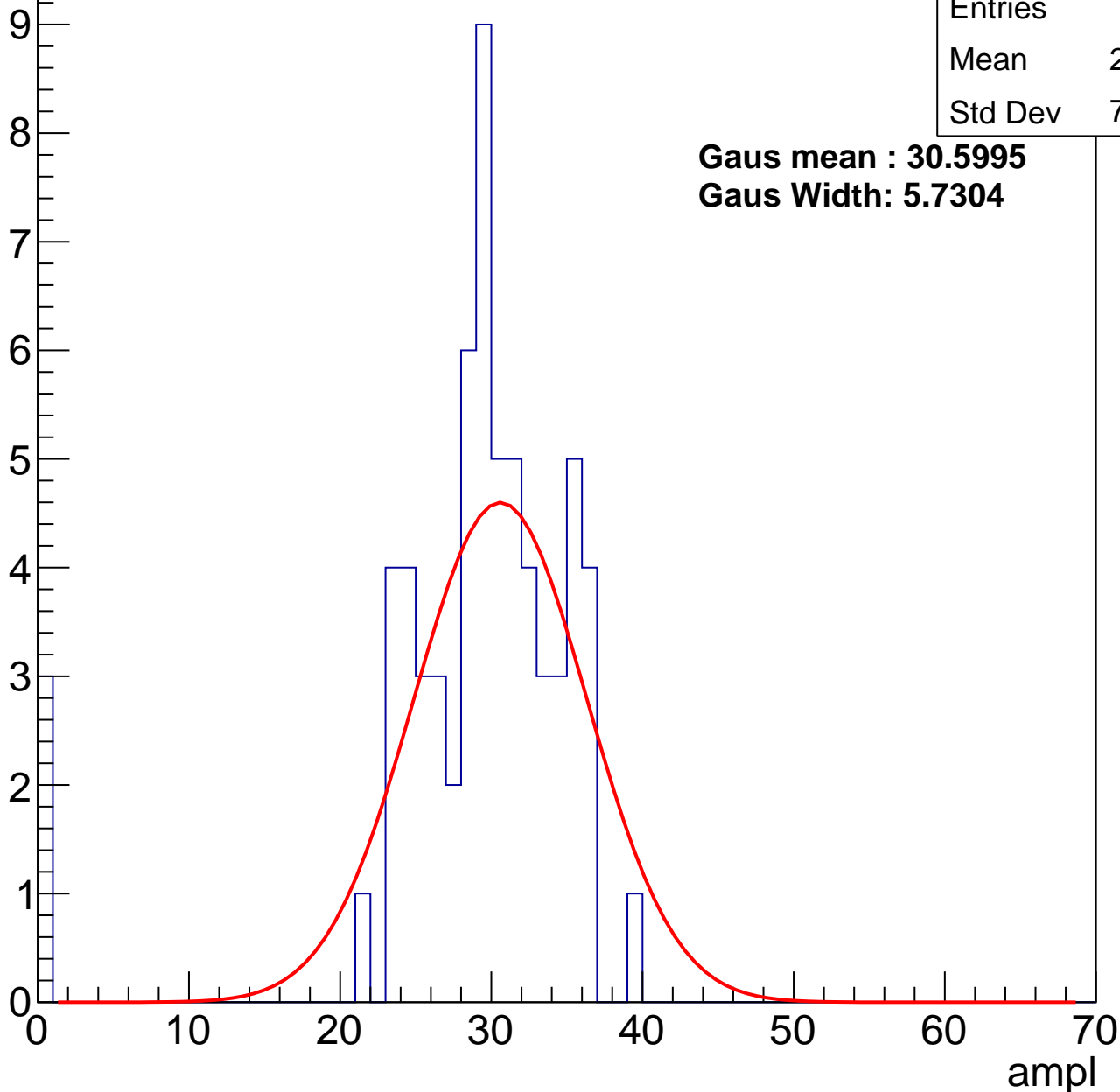
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	28.26
Std Dev	7.385

**Gaus mean : 30.5995**

**Gaus Width: 5.7304**



# B1L103S, U11-ch120, adc1

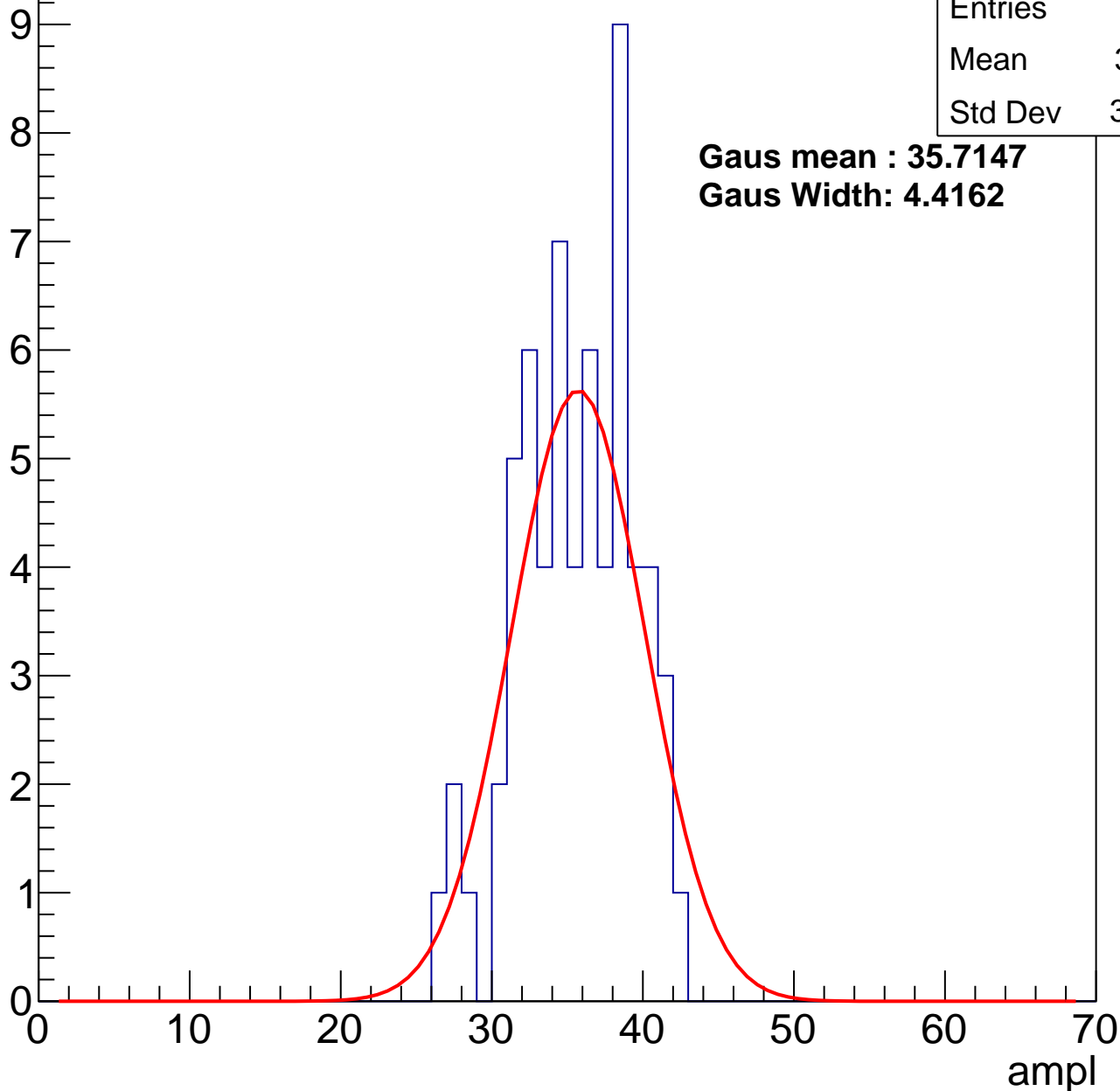
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	35.11
Std Dev	3.755

**Gaus mean : 35.7147**

**Gaus Width: 4.4162**



# B1L103S, U11-ch120, adc2

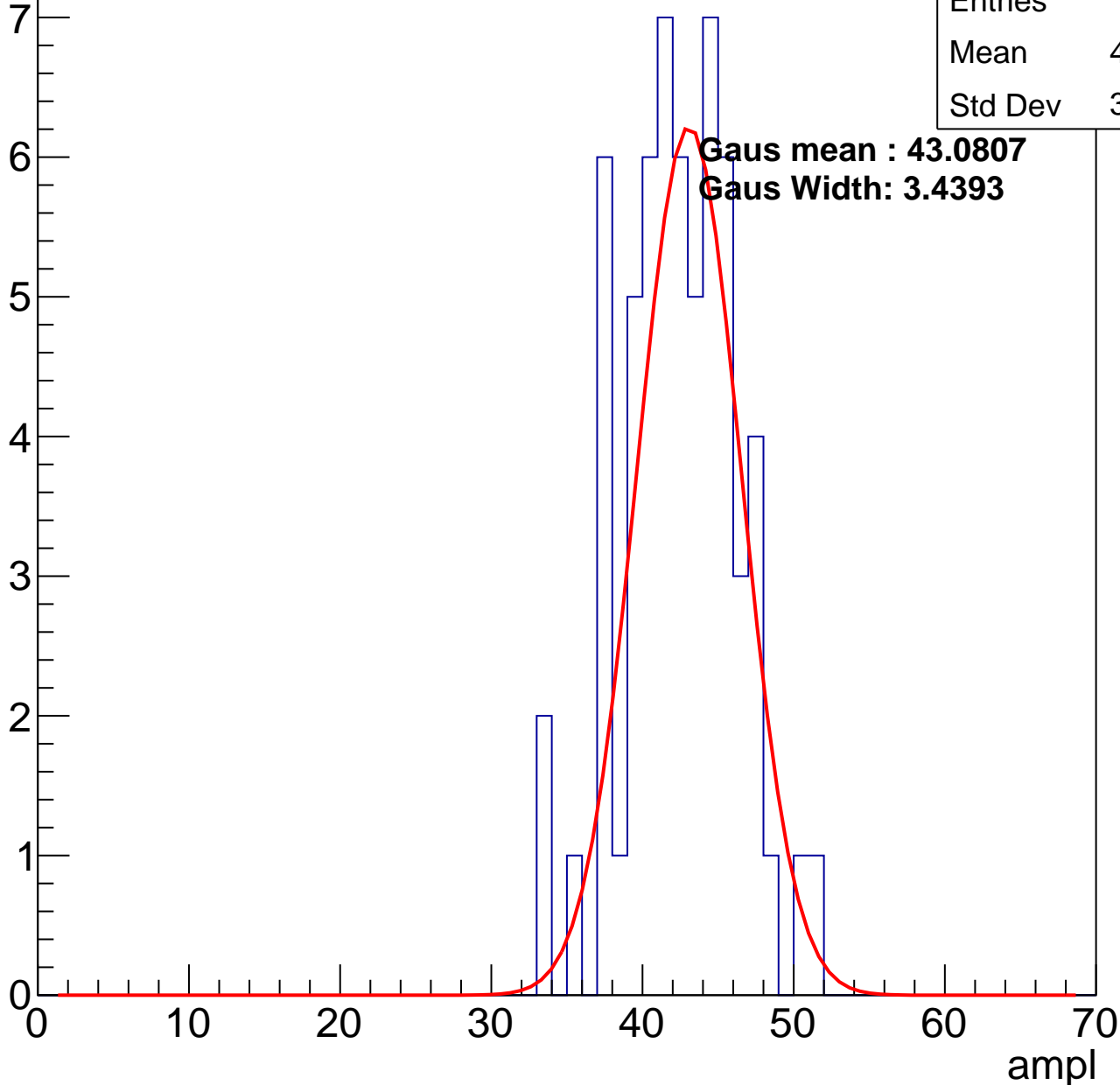
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	41.98
Std Dev	3.744

**Gaus mean : 43.0807**

**Gaus Width: 3.4393**

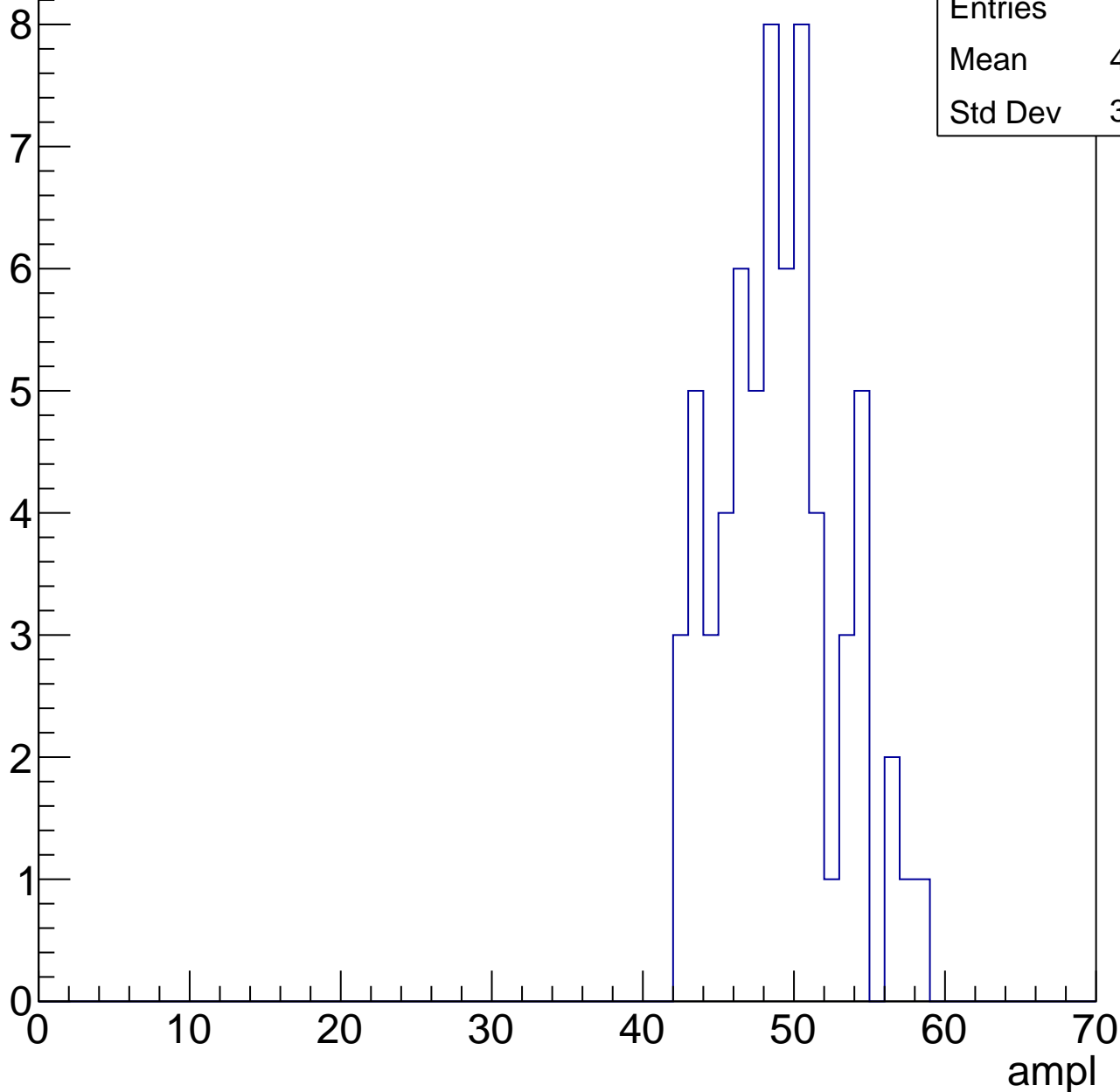


# B1L103S, U11-ch120, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	48.52
Std Dev	3.887

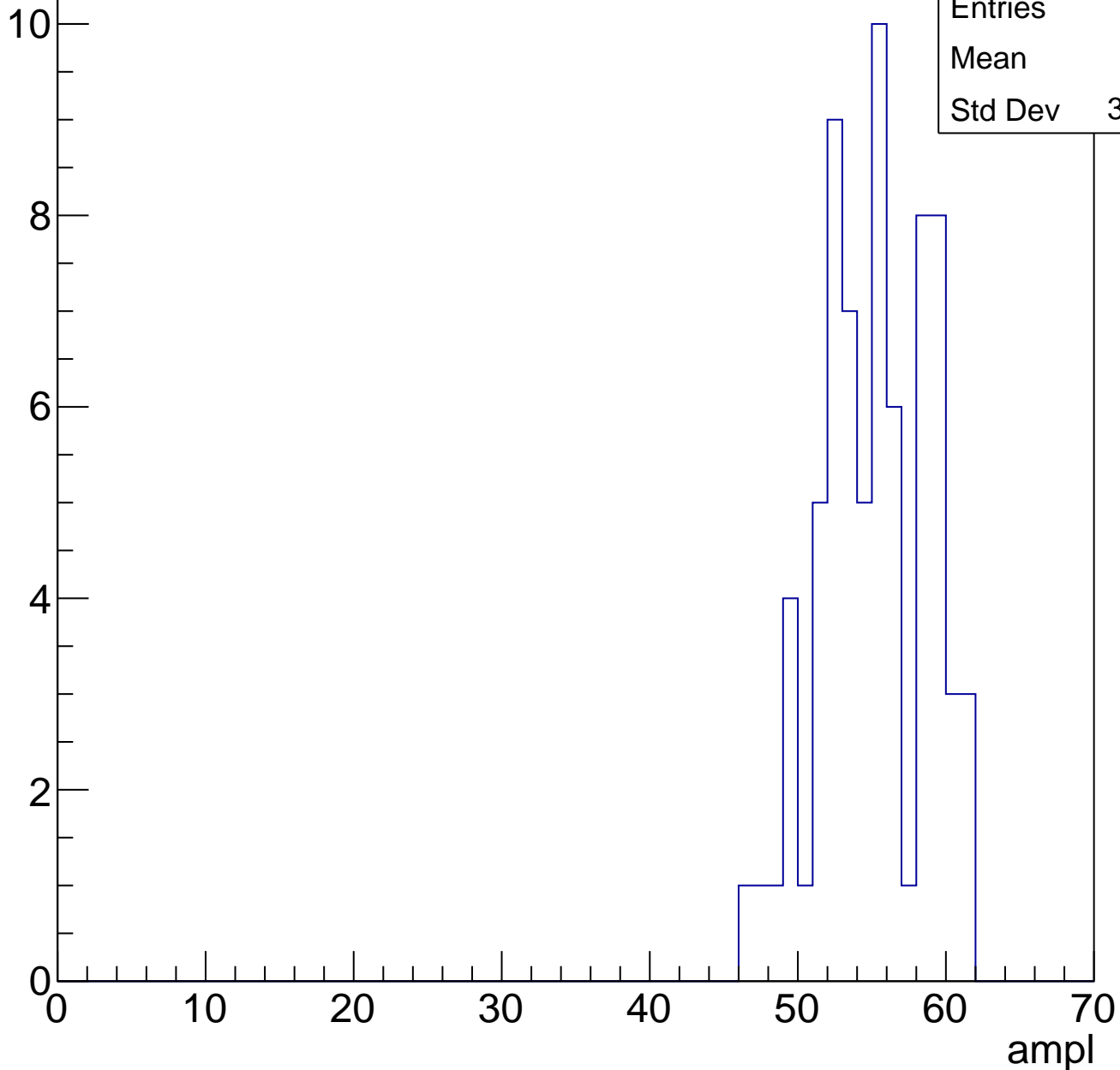


# B1L103S, U11-ch120, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	73
Mean	54.7
Std Dev	3.595

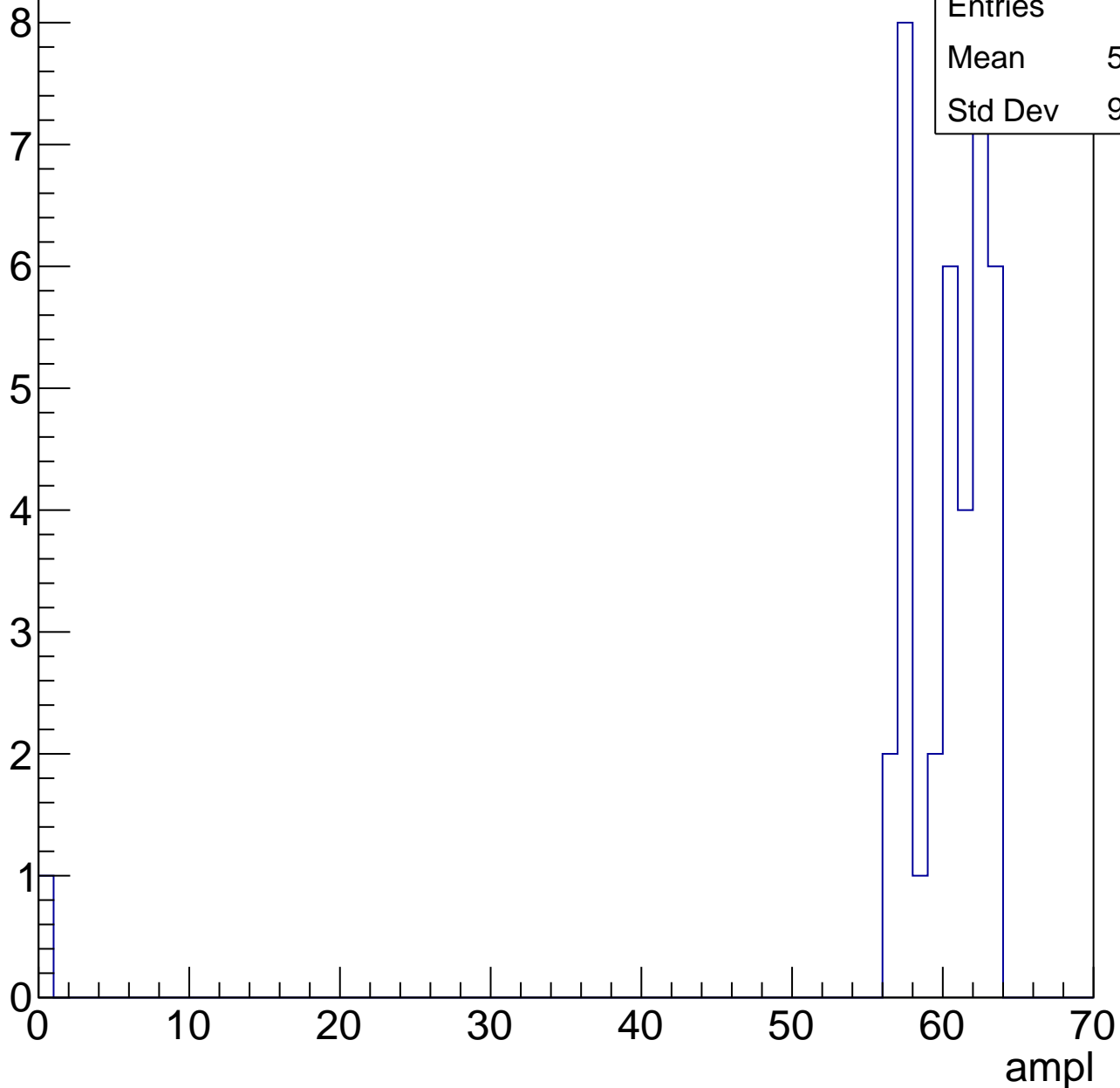
Entry



# B1L103S, U11-ch120, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

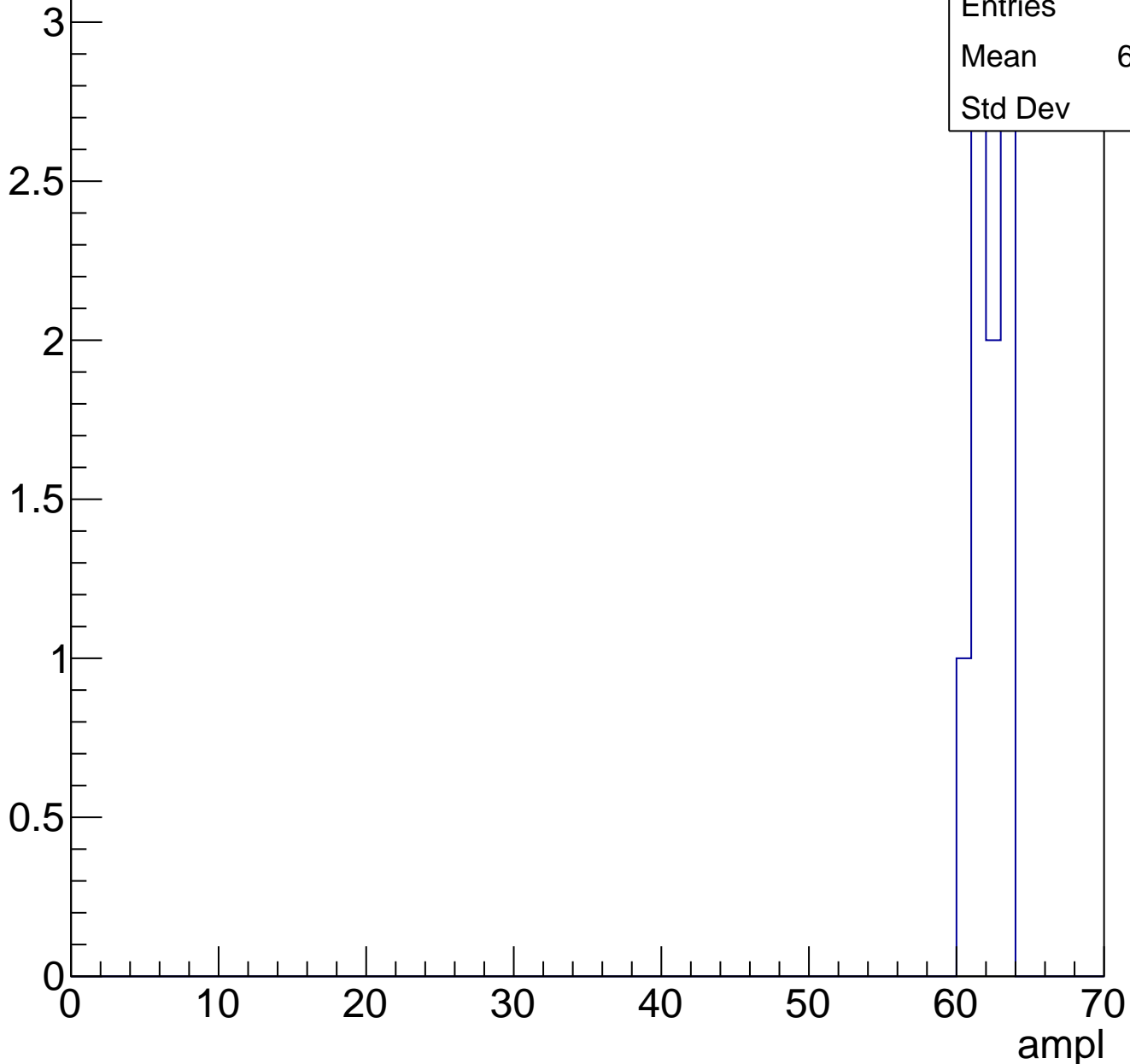
Entry



# B1L103S, U11-ch120, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U11-ch120, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U11-ch121, adc0

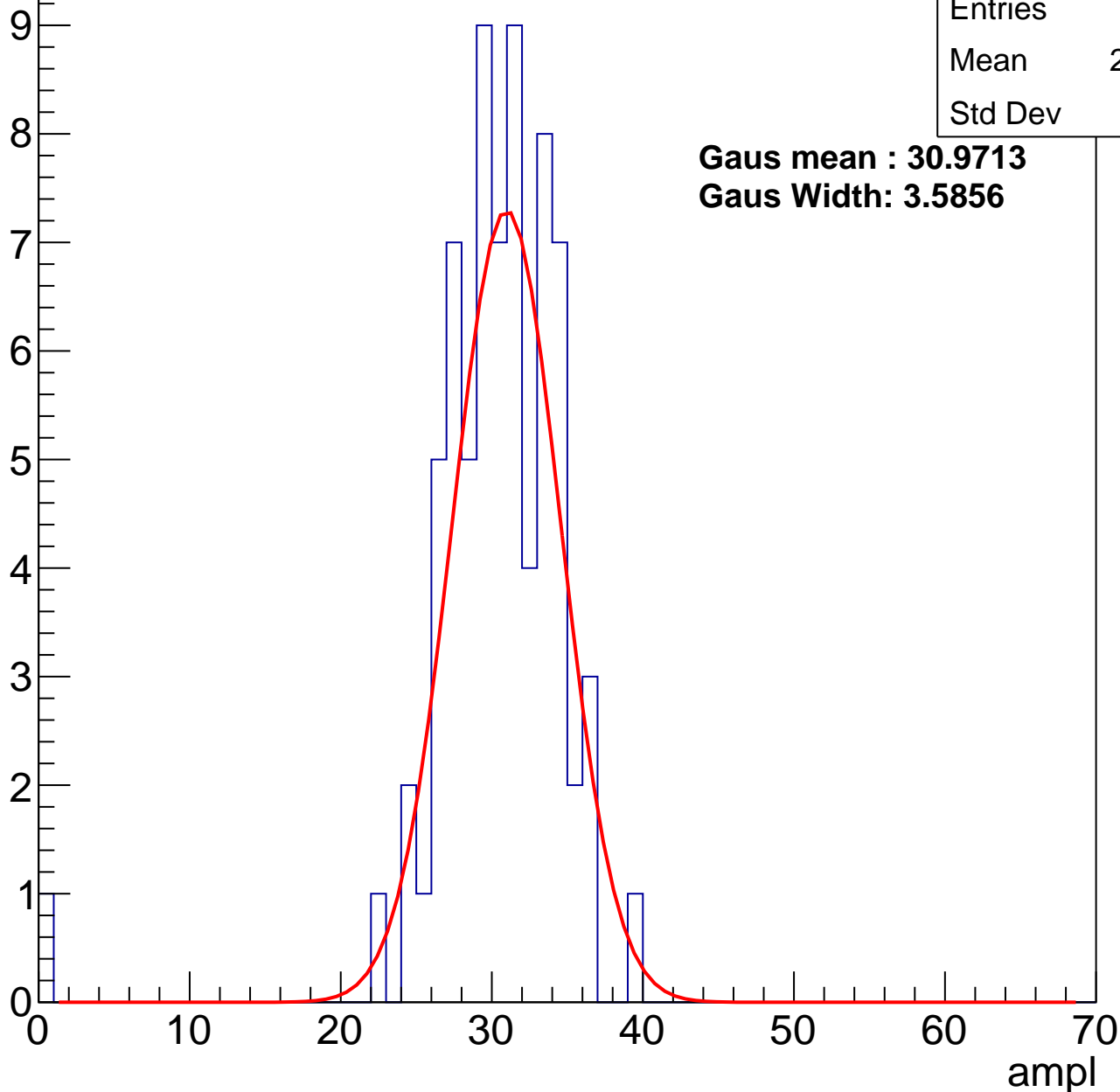
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	72
Mean	29.88
Std Dev	4.83

**Gaus mean : 30.9713**

**Gaus Width: 3.5856**



# B1L103S, U11-ch121, adc1

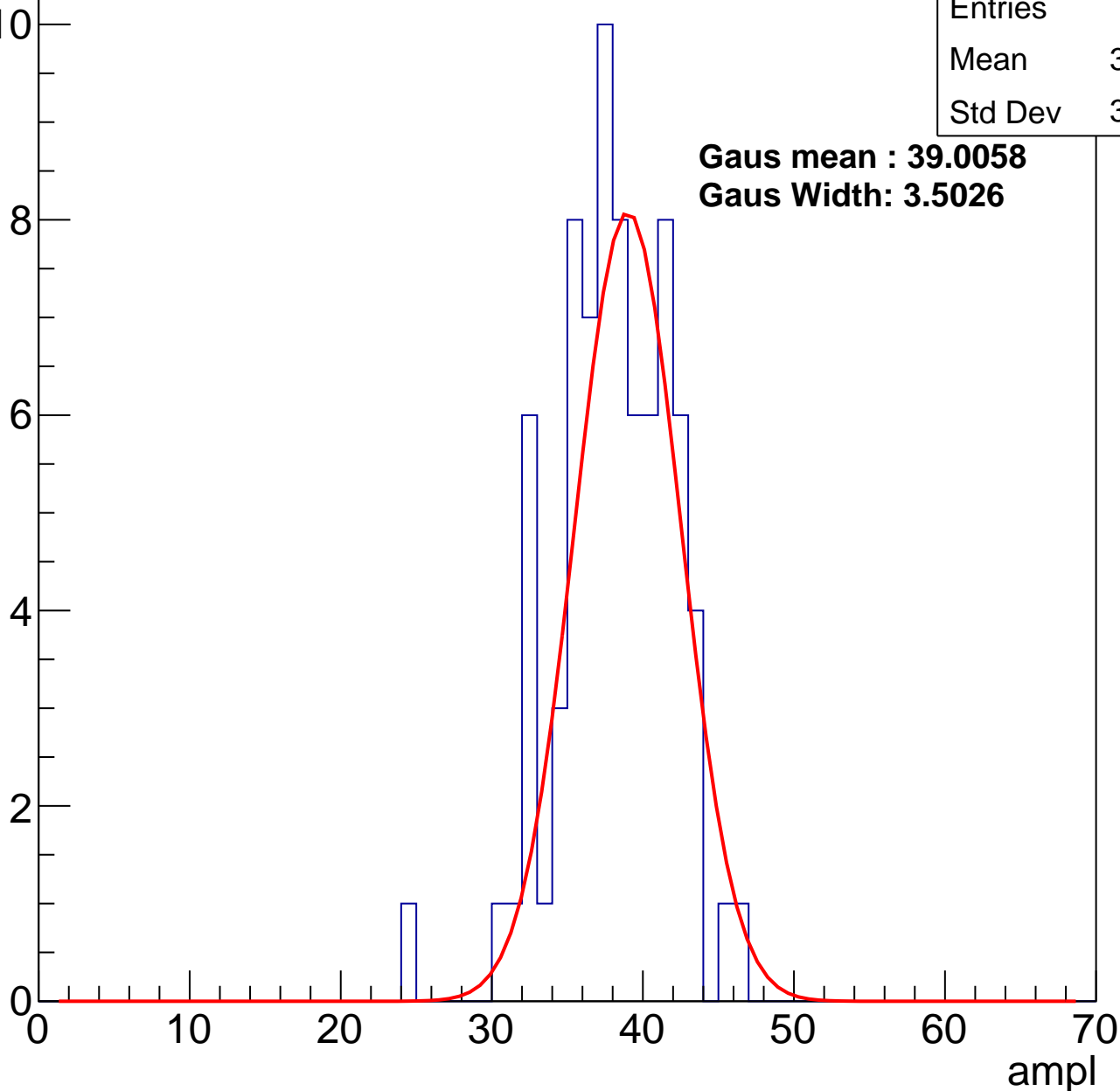
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	78
Mean	37.63
Std Dev	3.769

**Gaus mean : 39.0058**

**Gaus Width: 3.5026**



# B1L103S, U11-ch121, adc2

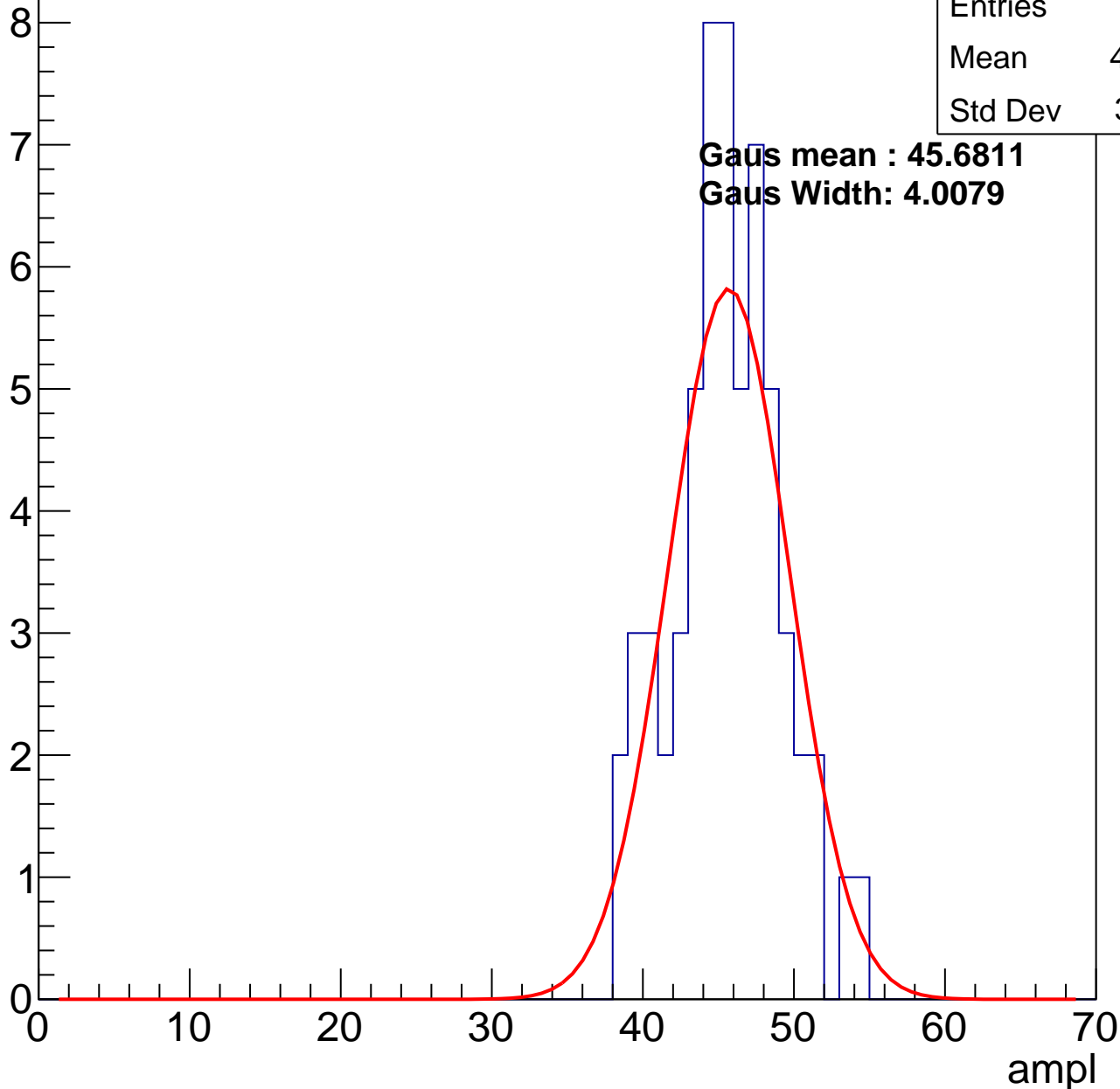
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	60
Mean	45.05
Std Dev	3.561

**Gaus mean : 45.6811**

**Gaus Width: 4.0079**

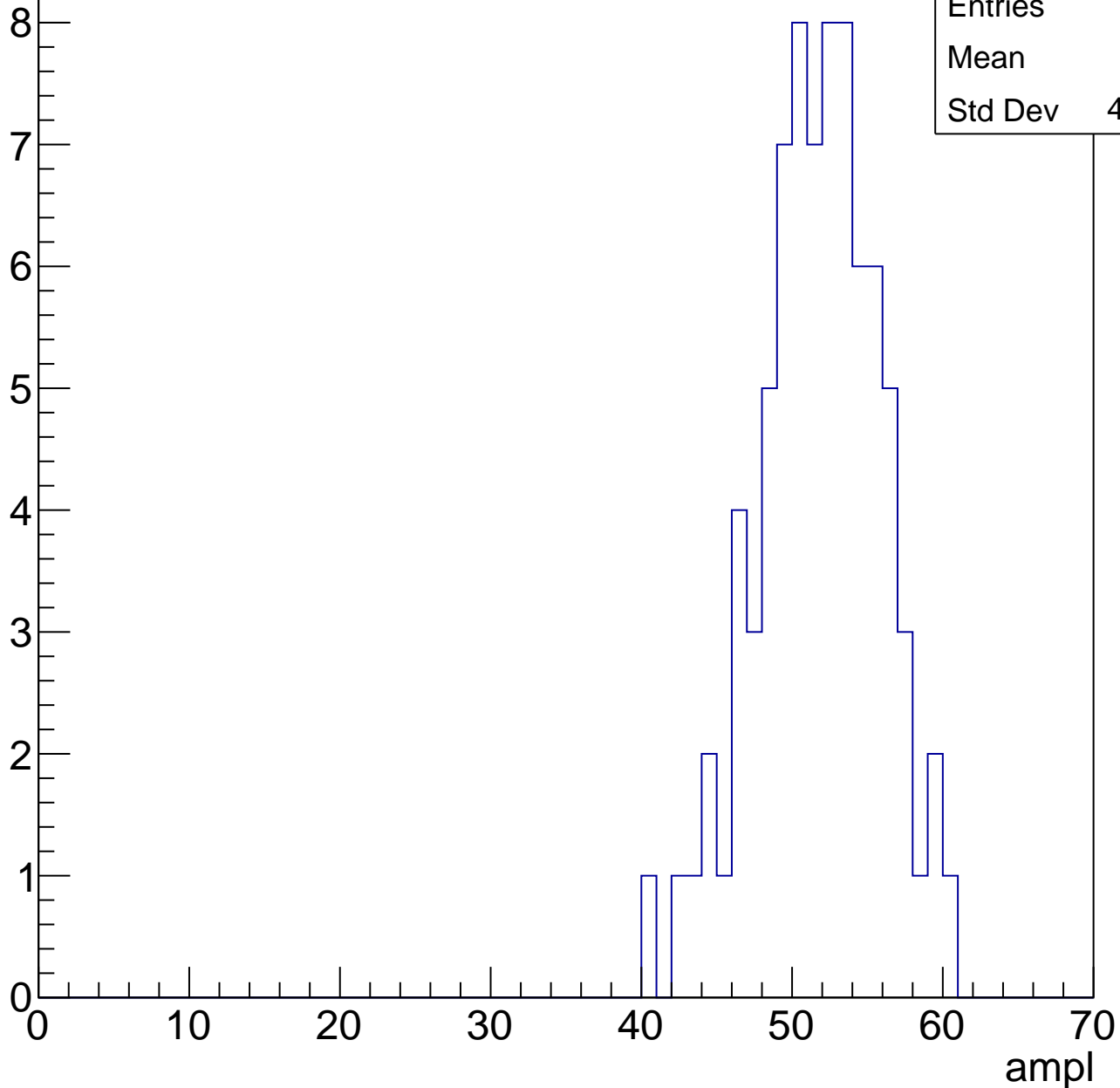


# B1L103S, U11-ch121, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	80
Mean	51.3
Std Dev	4.035

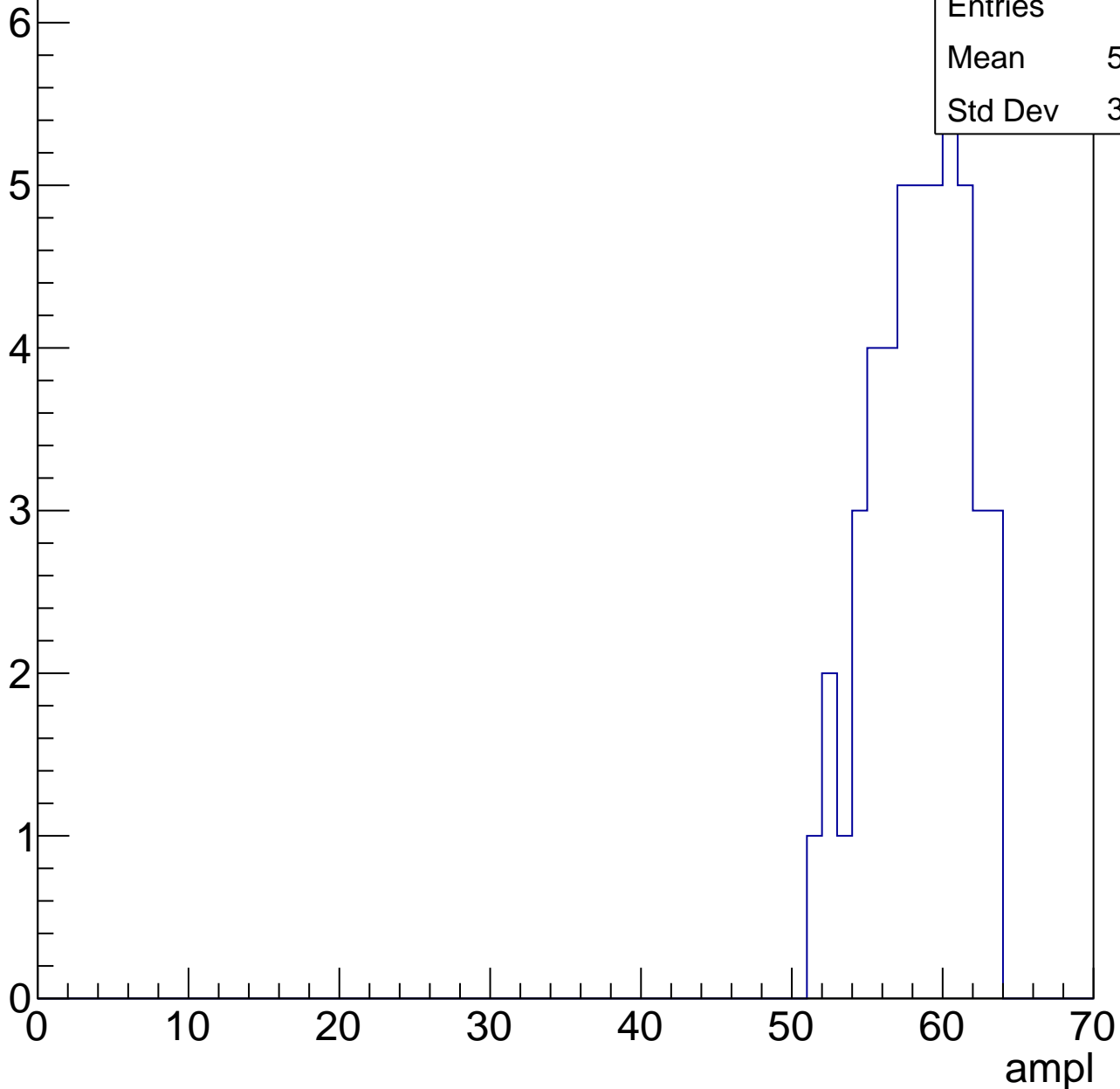


# B1L103S, U11-ch121, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	47
Mean	57.96
Std Dev	3.087

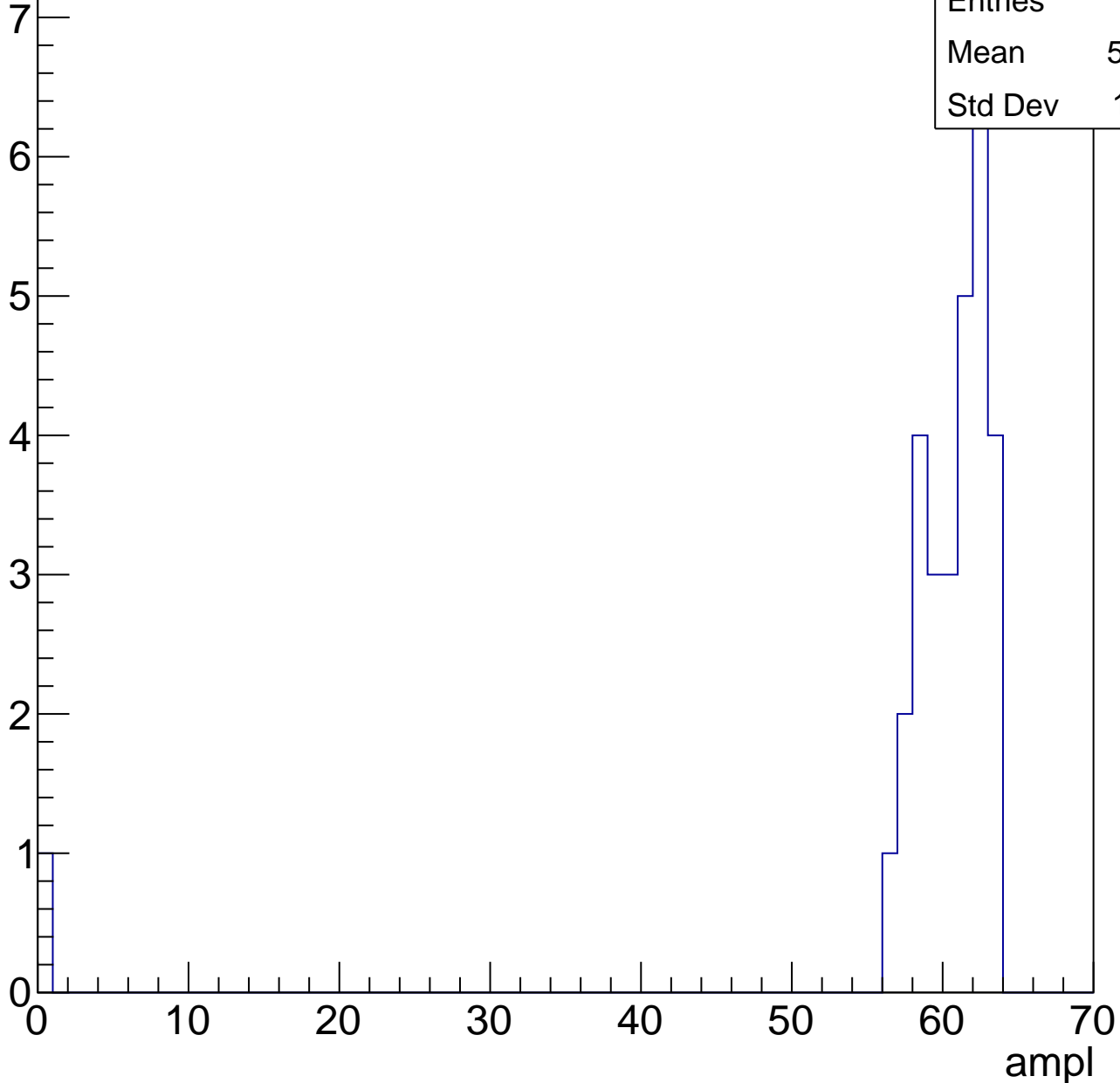


# B1L103S, U11-ch121, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	30
Mean	58.33
Std Dev	11.01



# B1L103S, U11-ch121, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U11-ch121, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U11-ch122, adc0

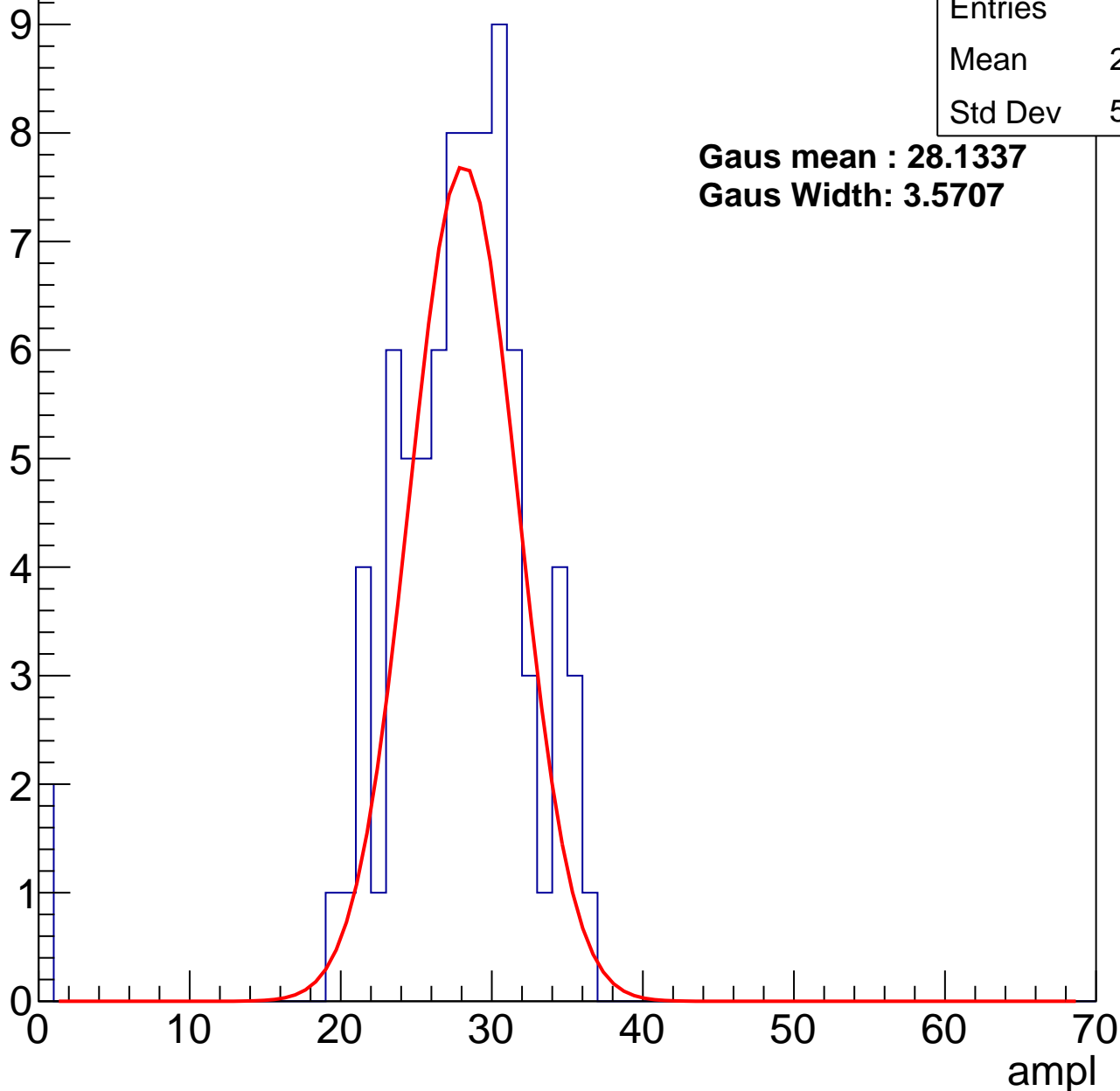
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	82
Mean	27.05
Std Dev	5.742

**Gaus mean : 28.1337**

**Gaus Width: 3.5707**



# B1L103S, U11-ch122, adc1

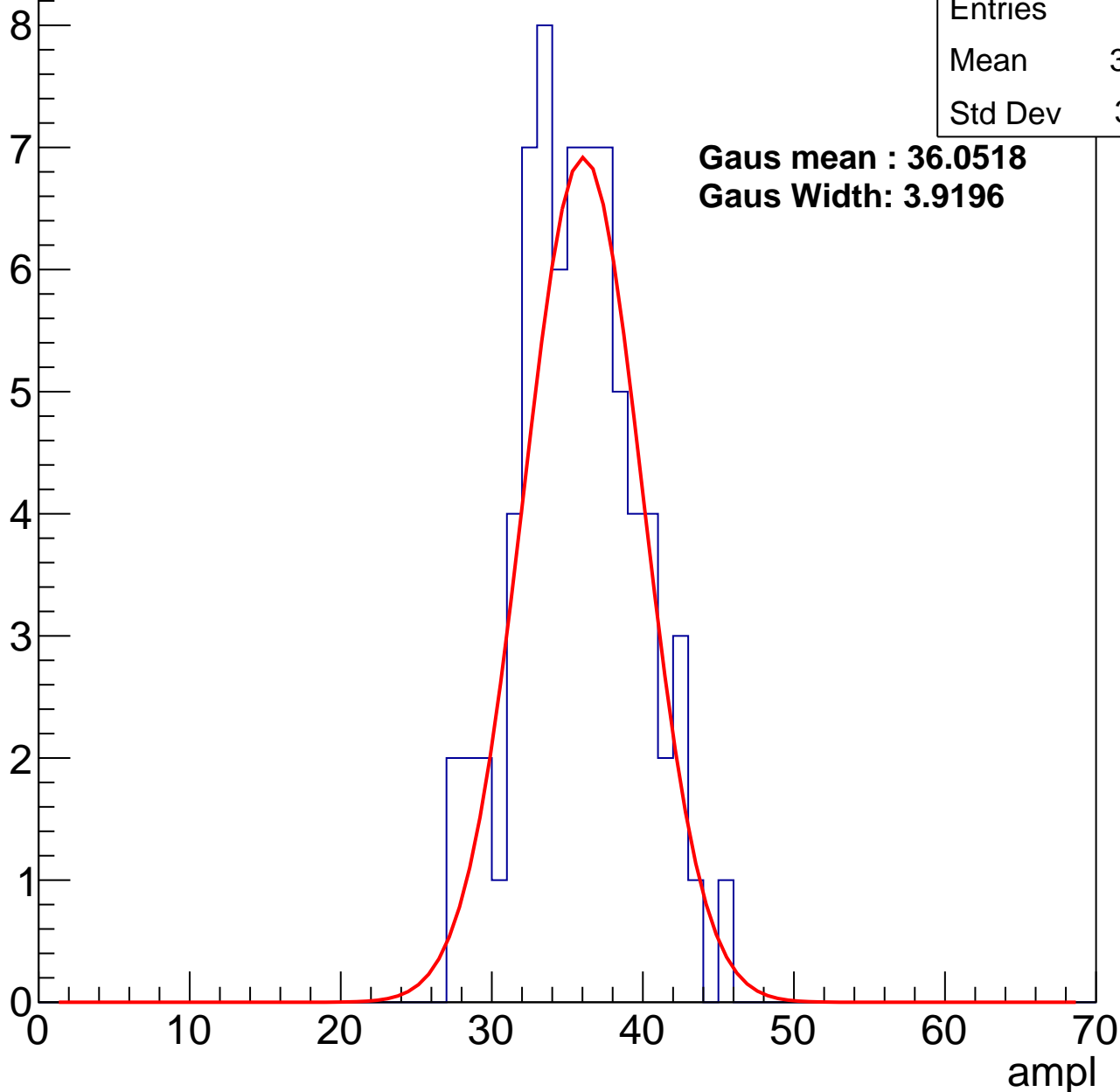
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	73
Mean	35.23
Std Dev	3.901

**Gaus mean : 36.0518**

**Gaus Width: 3.9196**



# B1L103S, U11-ch122, adc2

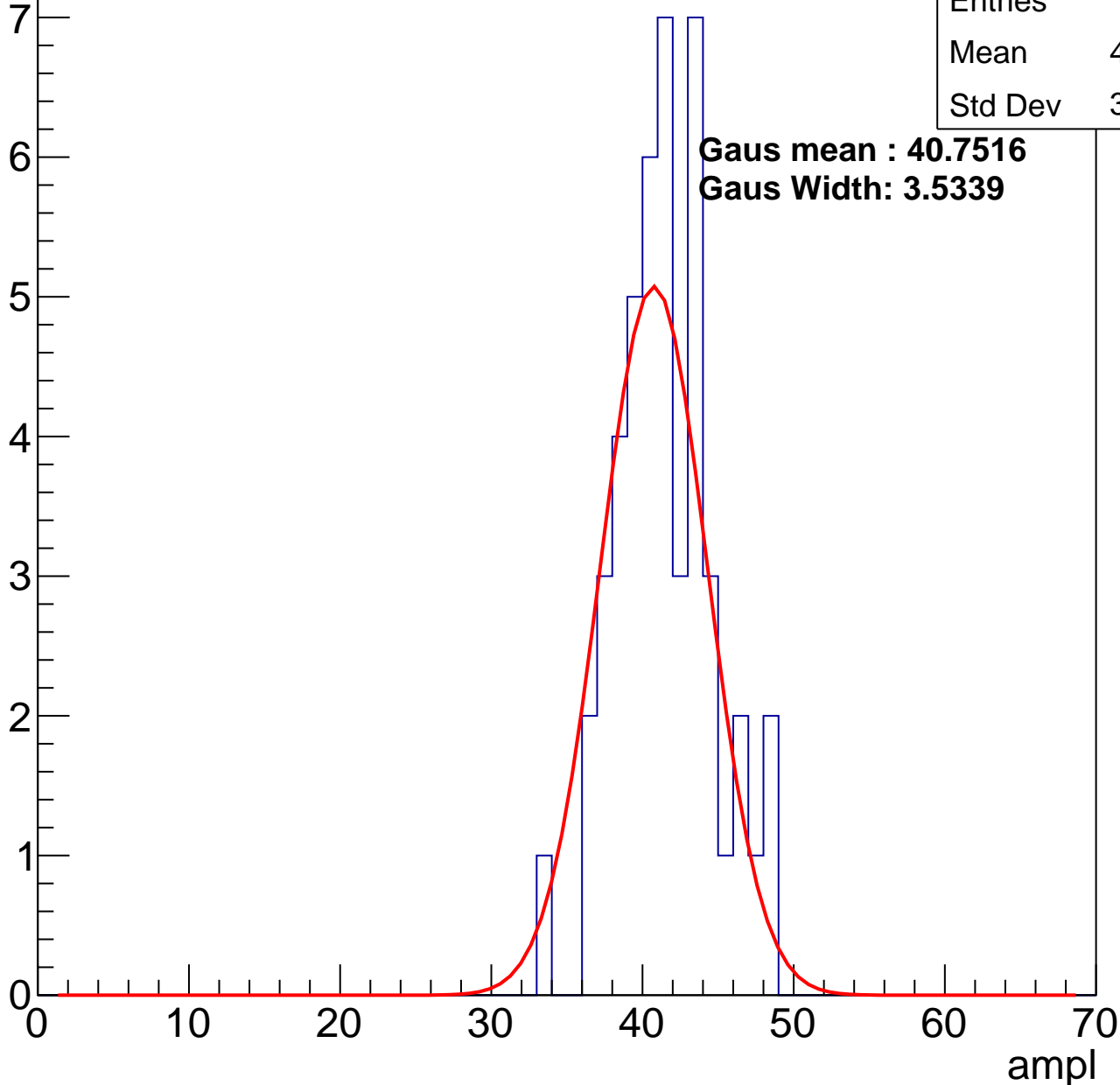
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	47
Mean	41.04
Std Dev	3.202

**Gaus mean : 40.7516**

**Gaus Width: 3.5339**

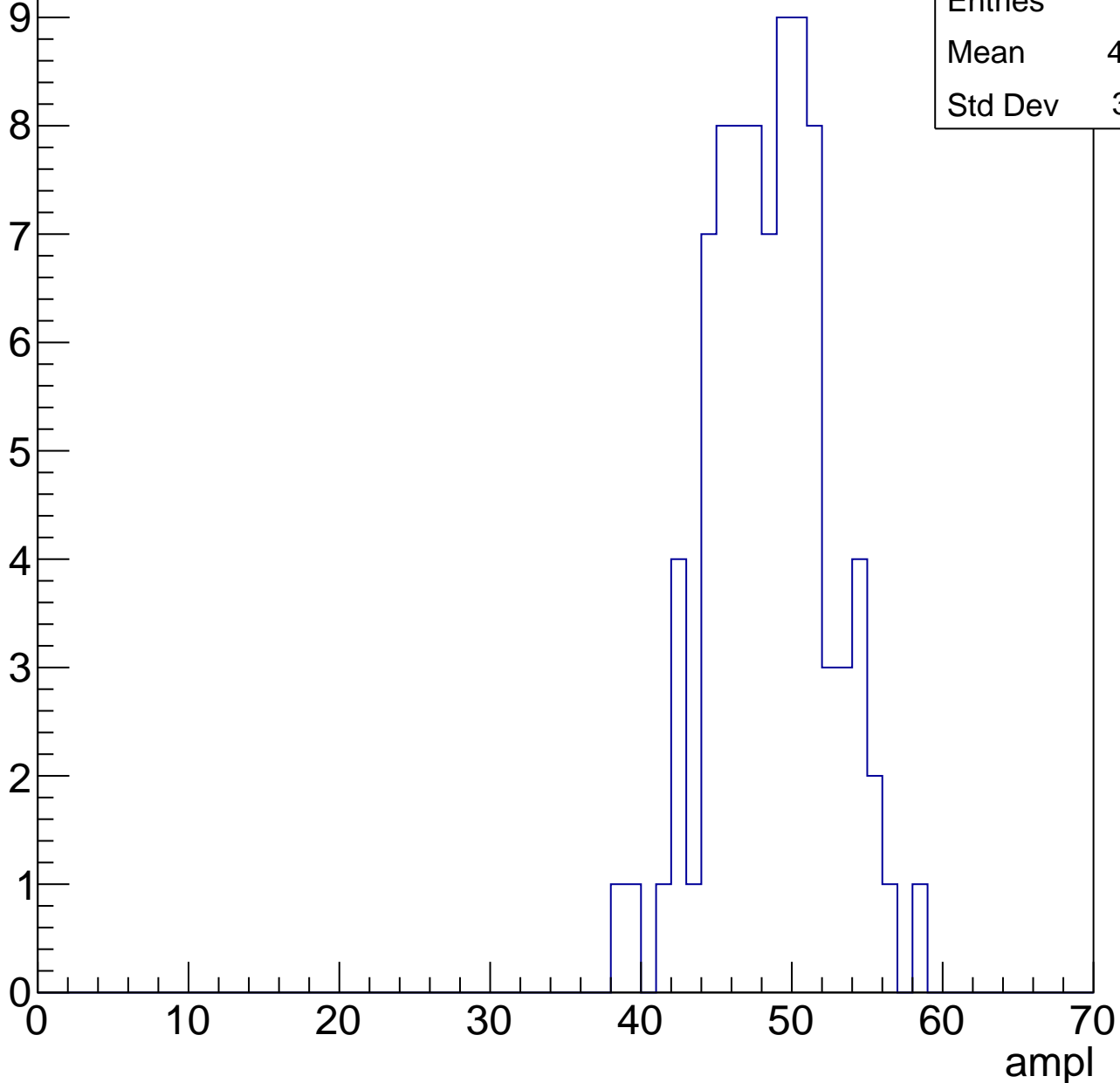


# B1L103S, U11-ch122, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	86
Mean	48.03
Std Dev	3.841

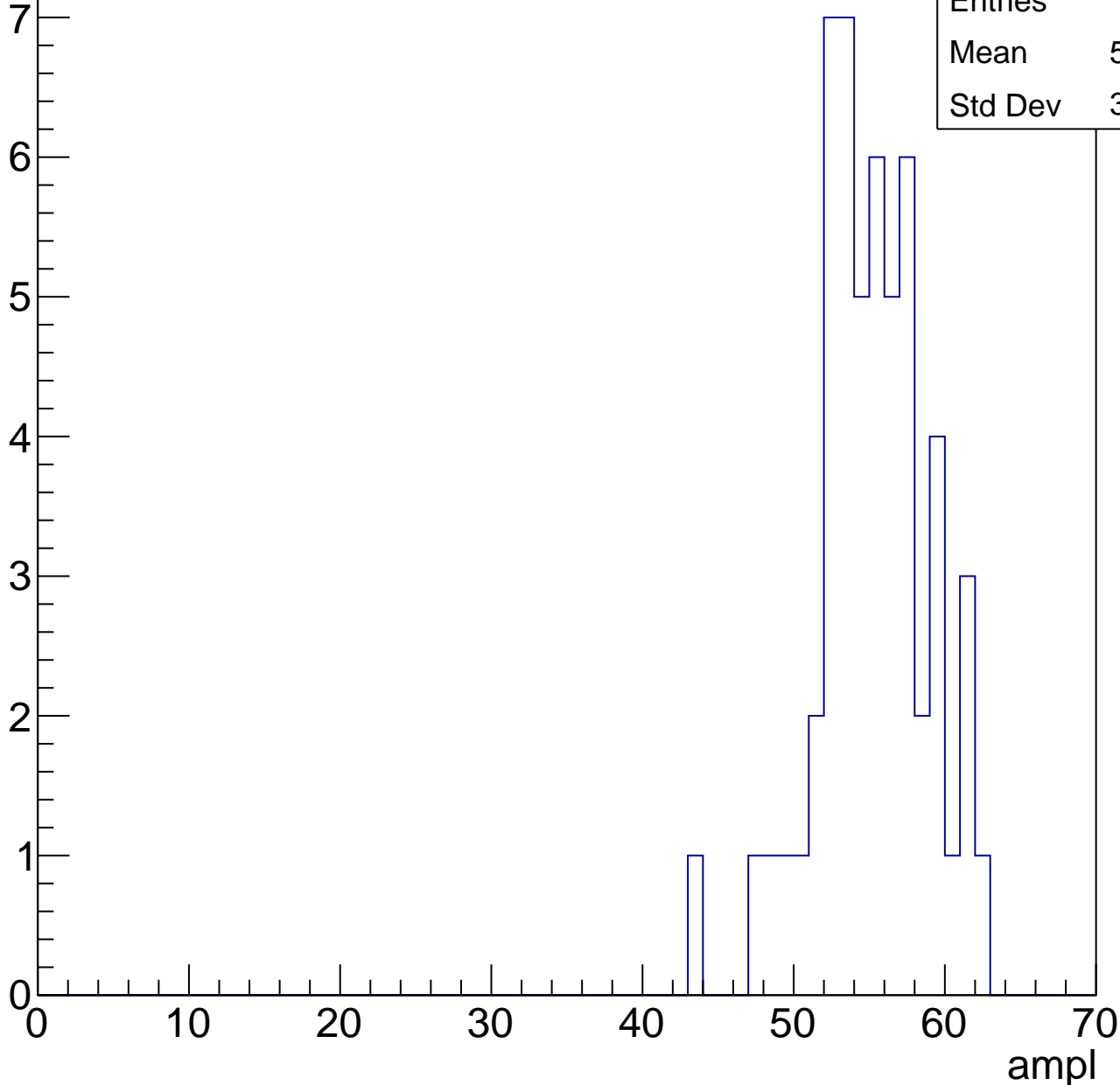


# B1L103S, U11-ch122, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

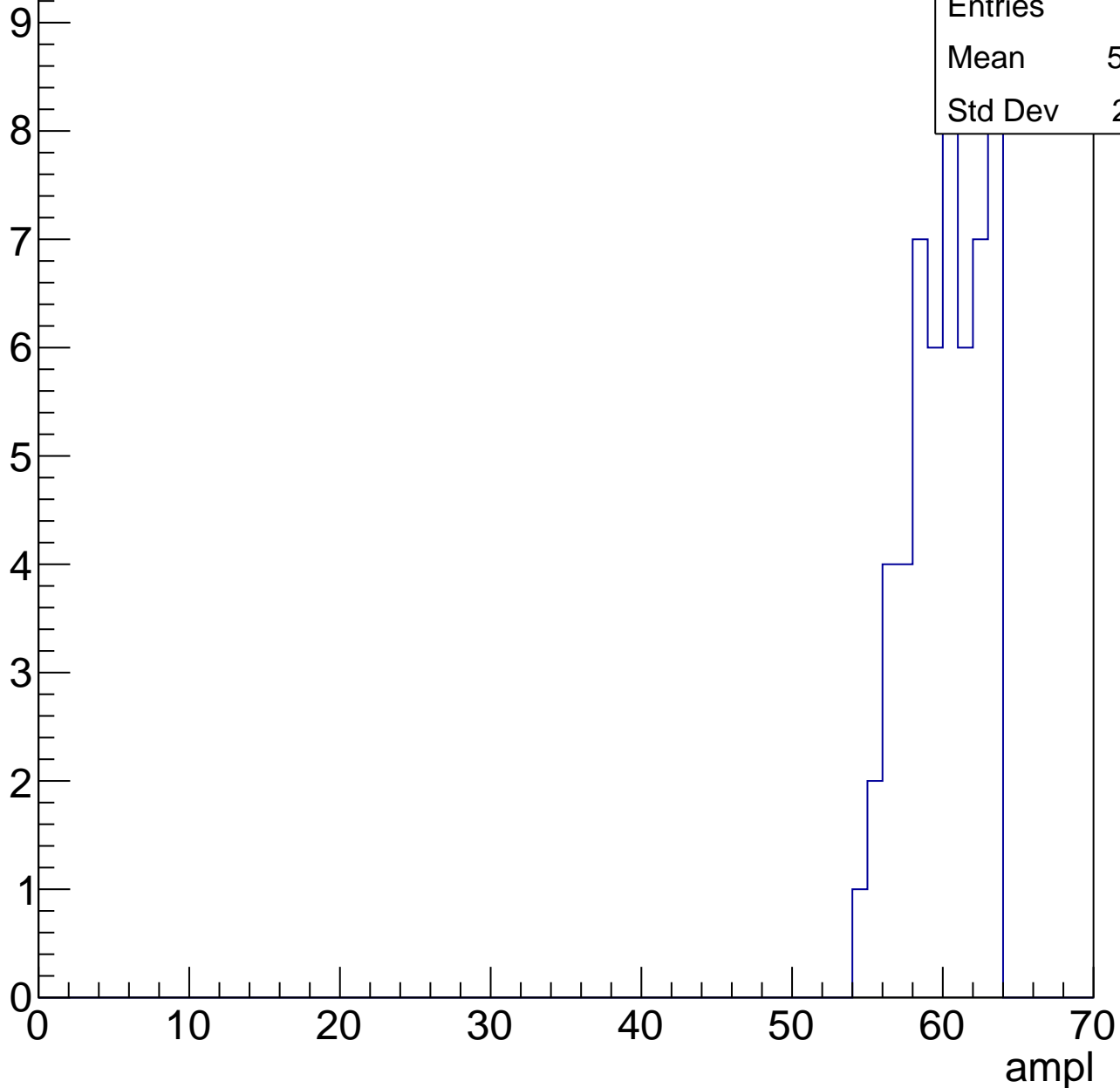
Entries	54
Mean	54.69
Std Dev	3.686



# B1L103S, U11-ch122, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U11-ch122, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

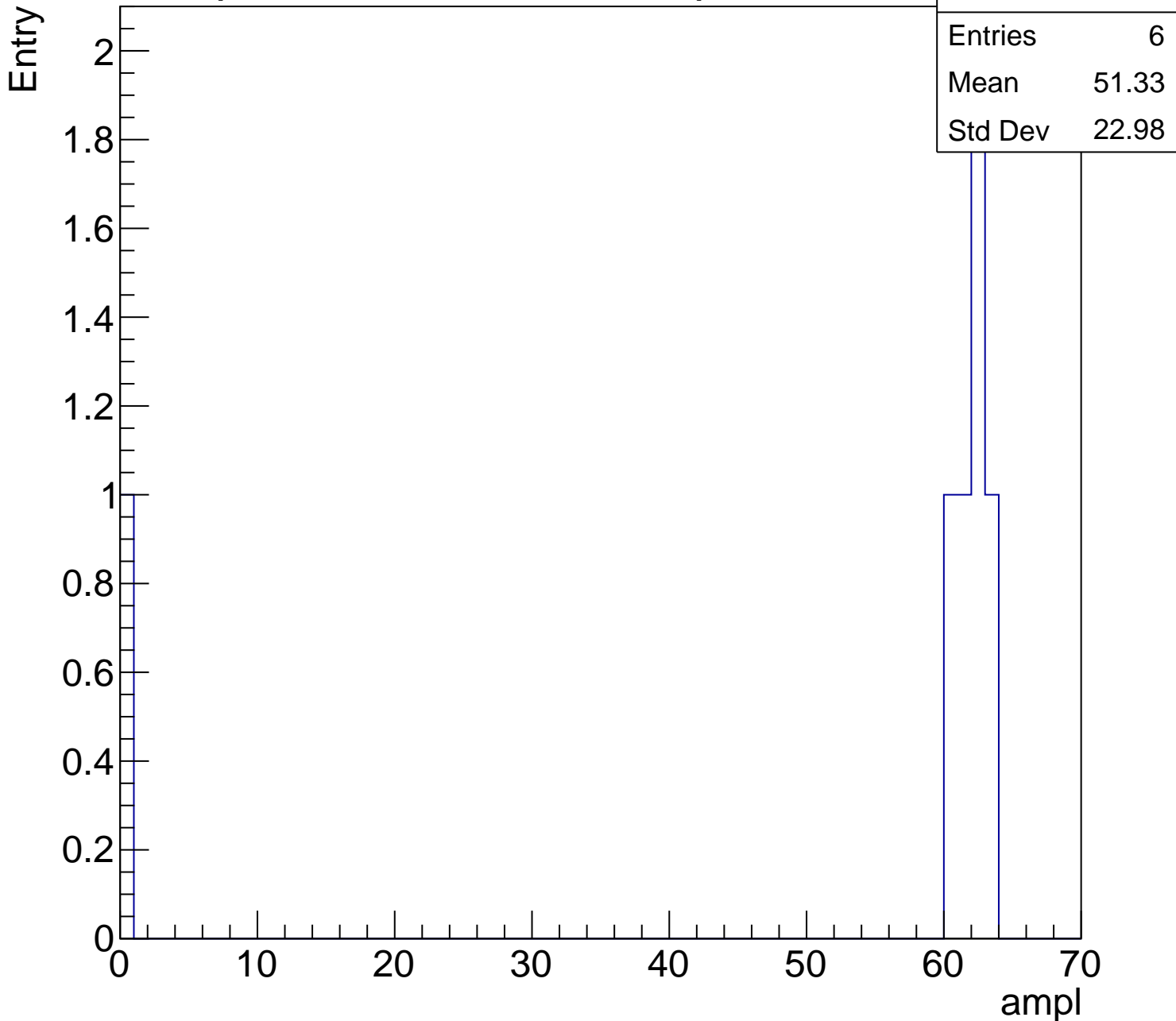
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	6
Mean	51.33
Std Dev	22.98

0 10 20 30 40 50 60 70

ampl





# B1L103S, U11-ch122, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U11-ch123, adc0

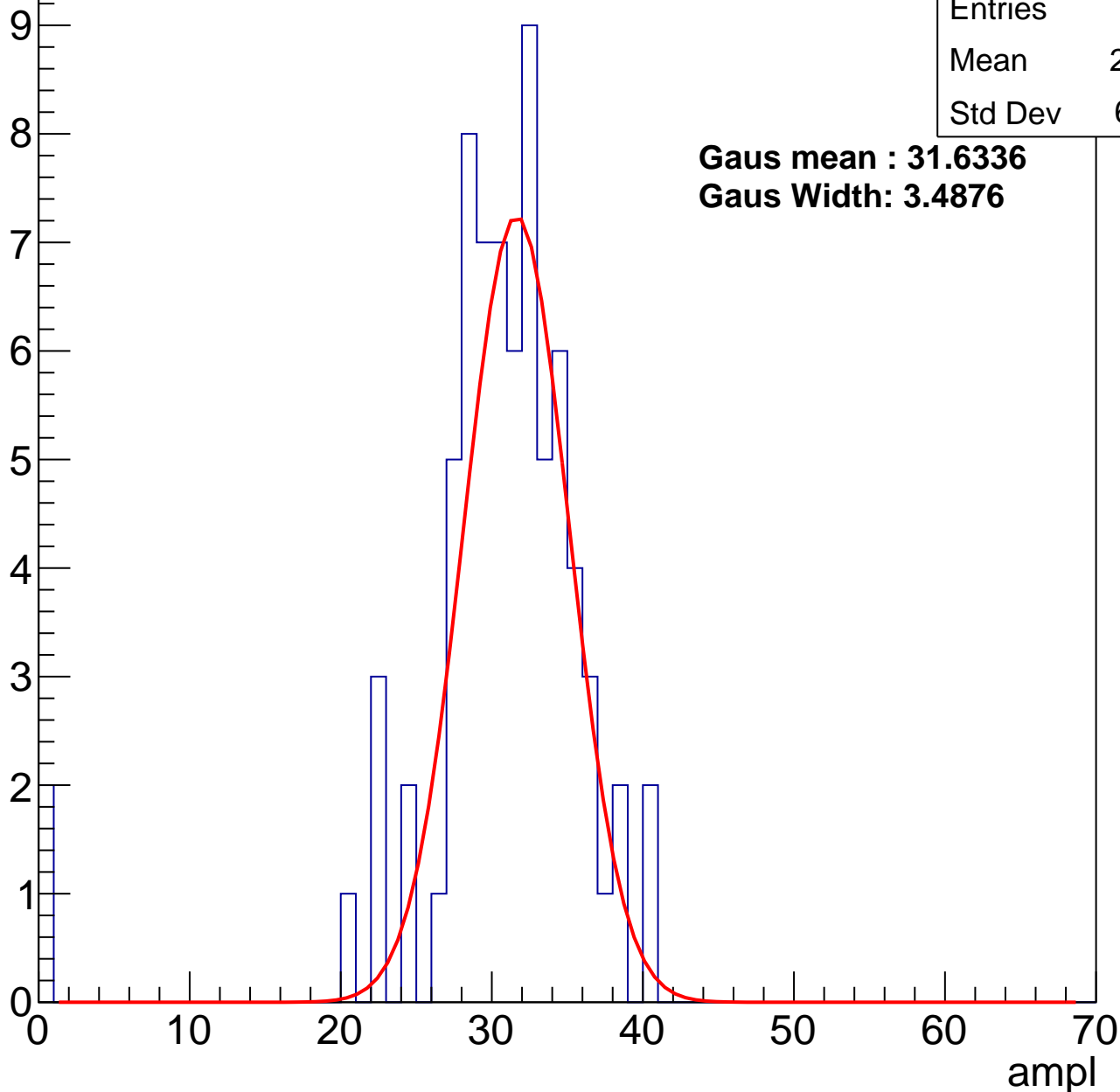
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	74
Mean	29.95
Std Dev	6.401

**Gaus mean : 31.6336**

**Gaus Width: 3.4876**



# B1L103S, U11-ch123, adc1

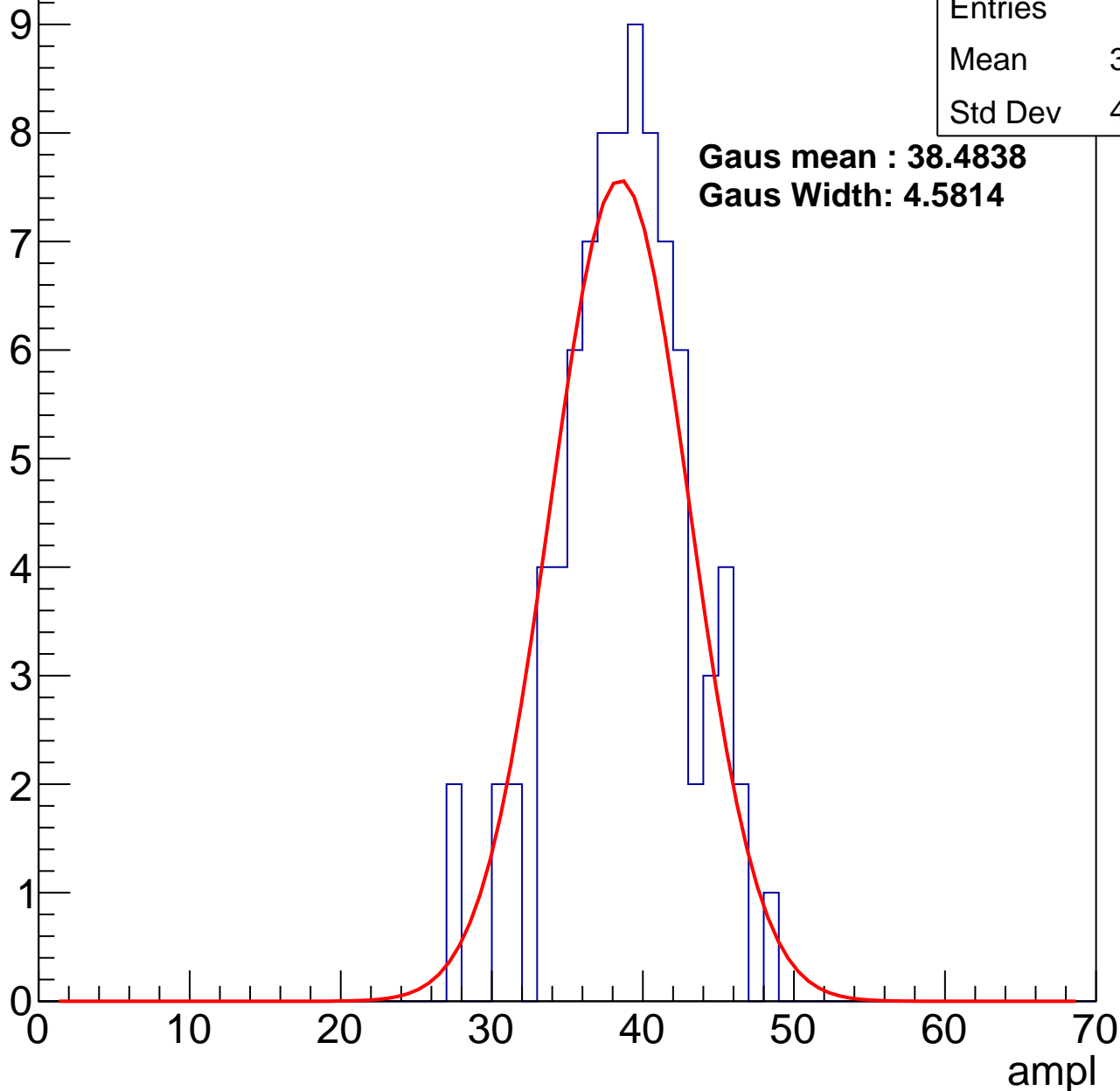
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	85
Mean	38.28
Std Dev	4.197

**Gaus mean : 38.4838**

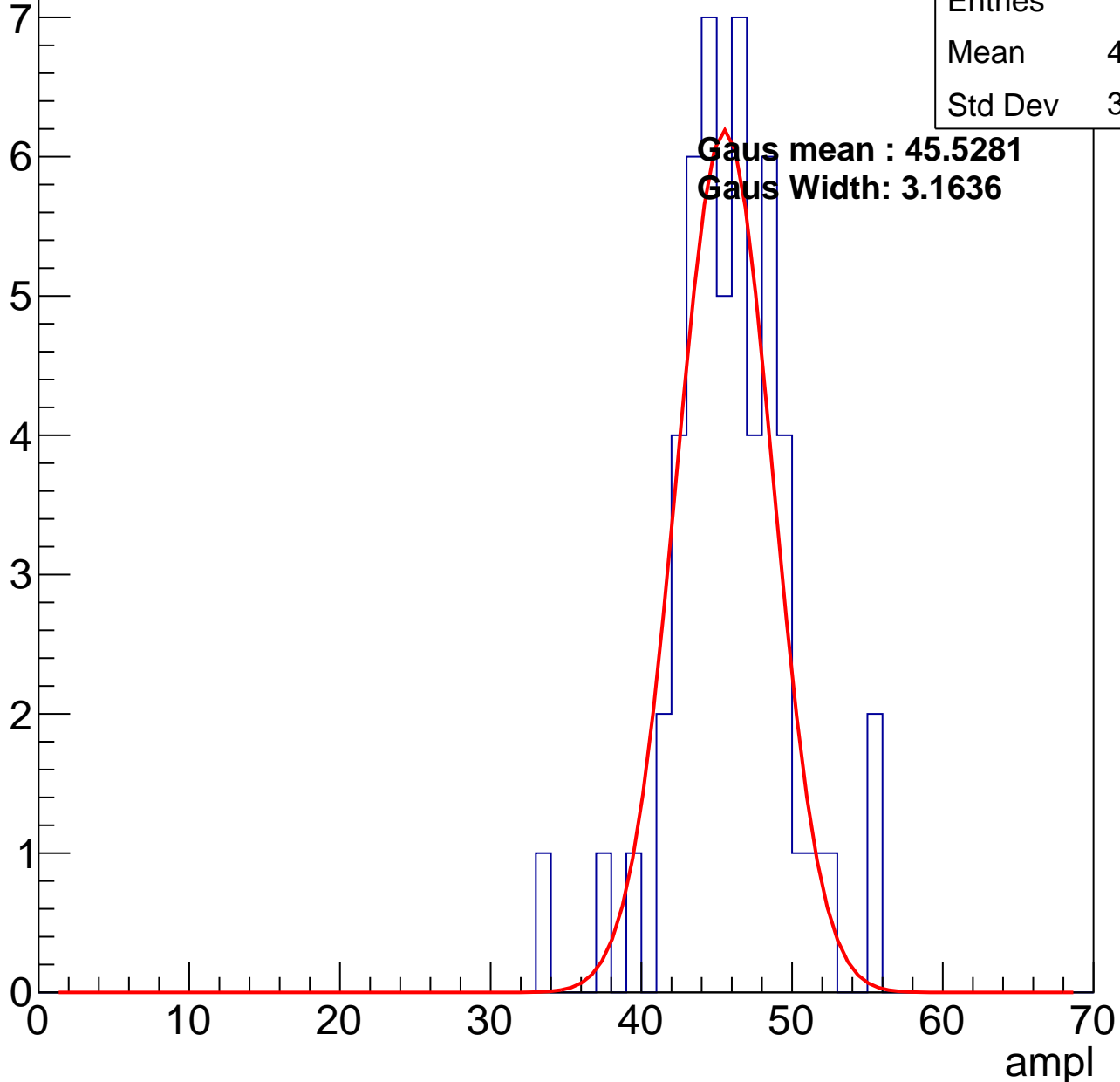
**Gaus Width: 4.5814**



# B1L103S, U11-ch123, adc2

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

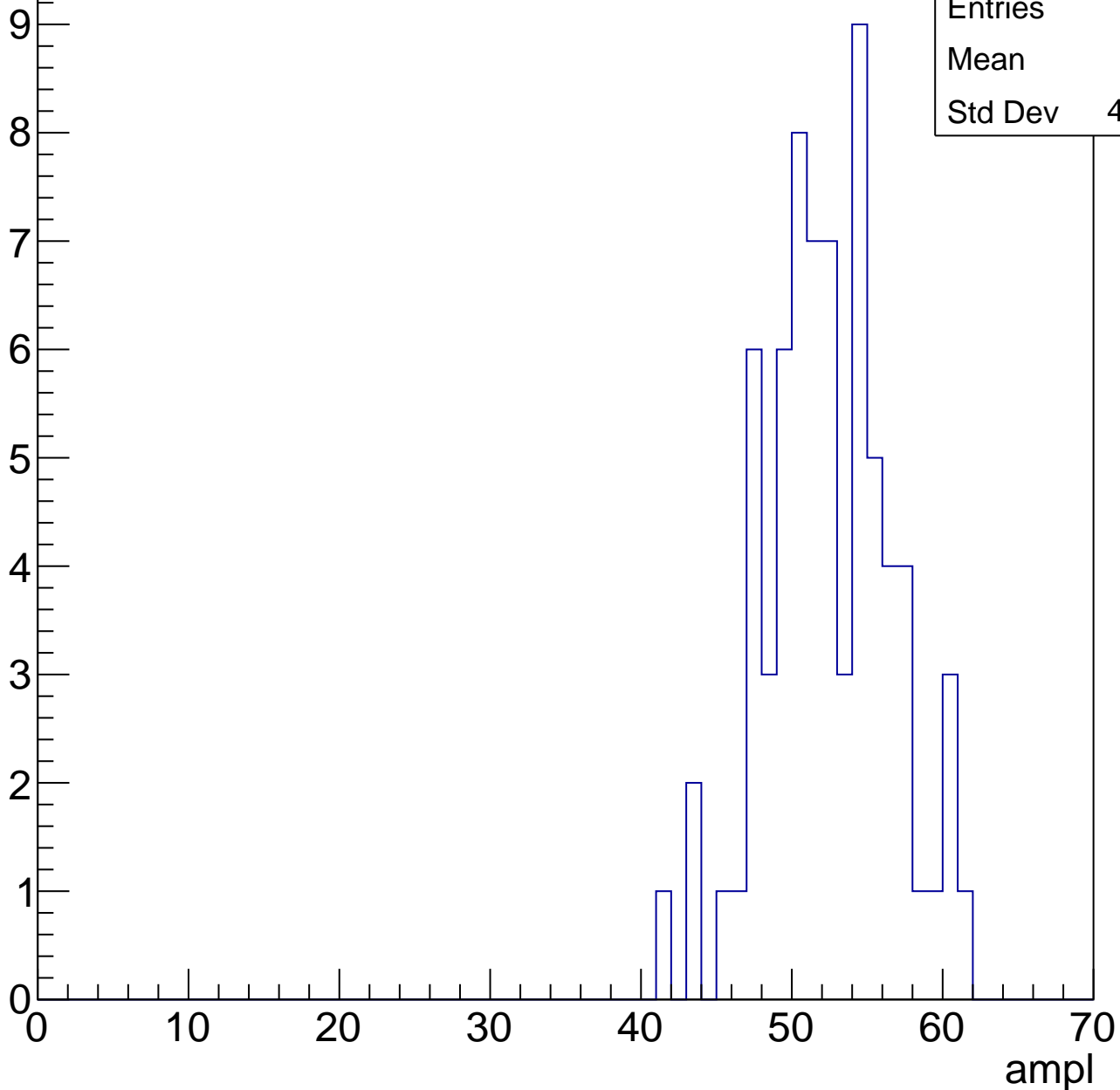


# B1L103S, U11-ch123, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	73
Mean	51.9
Std Dev	4.162

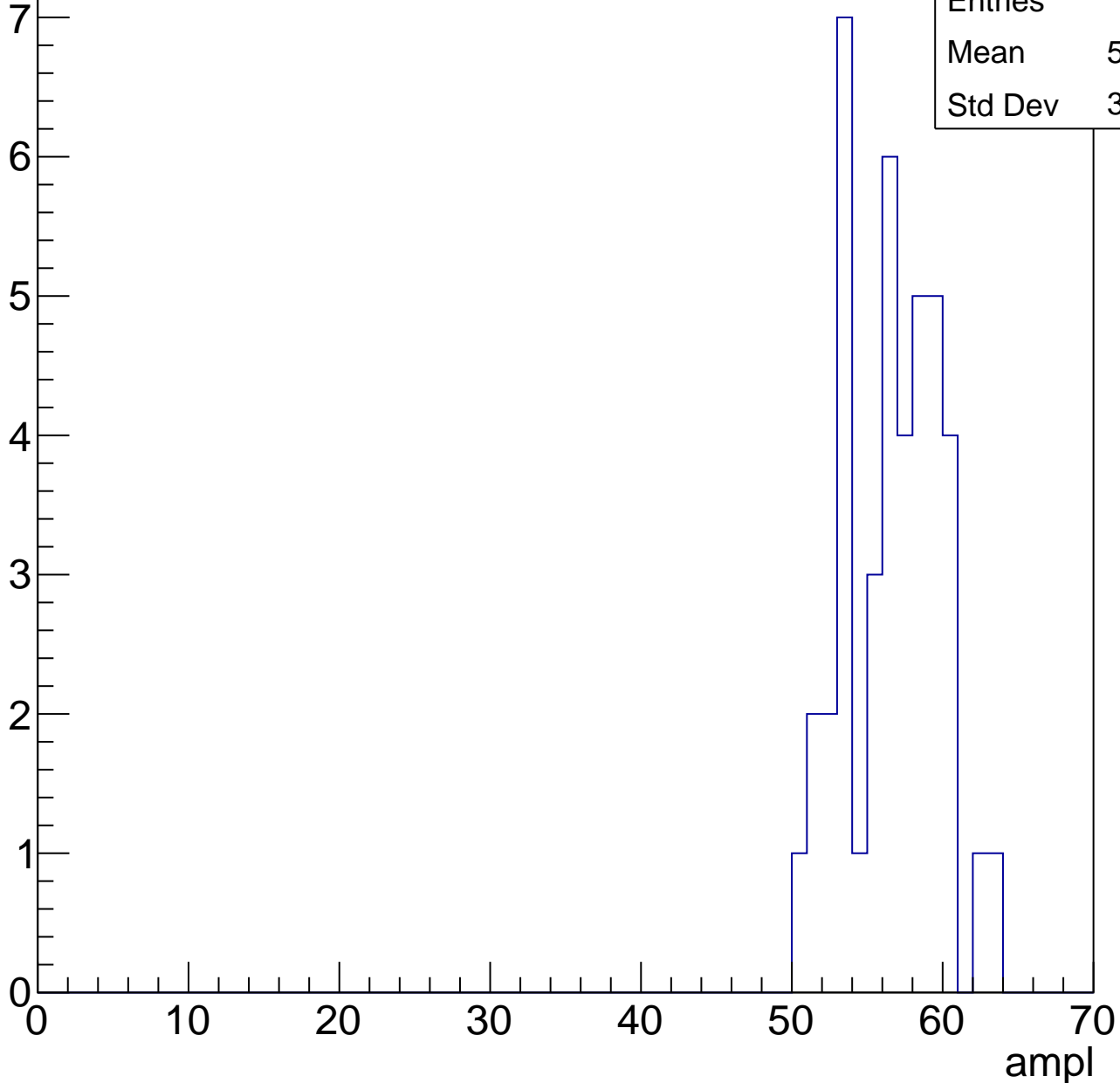


# B1L103S, U11-ch123, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	42
Mean	56.19
Std Dev	3.103

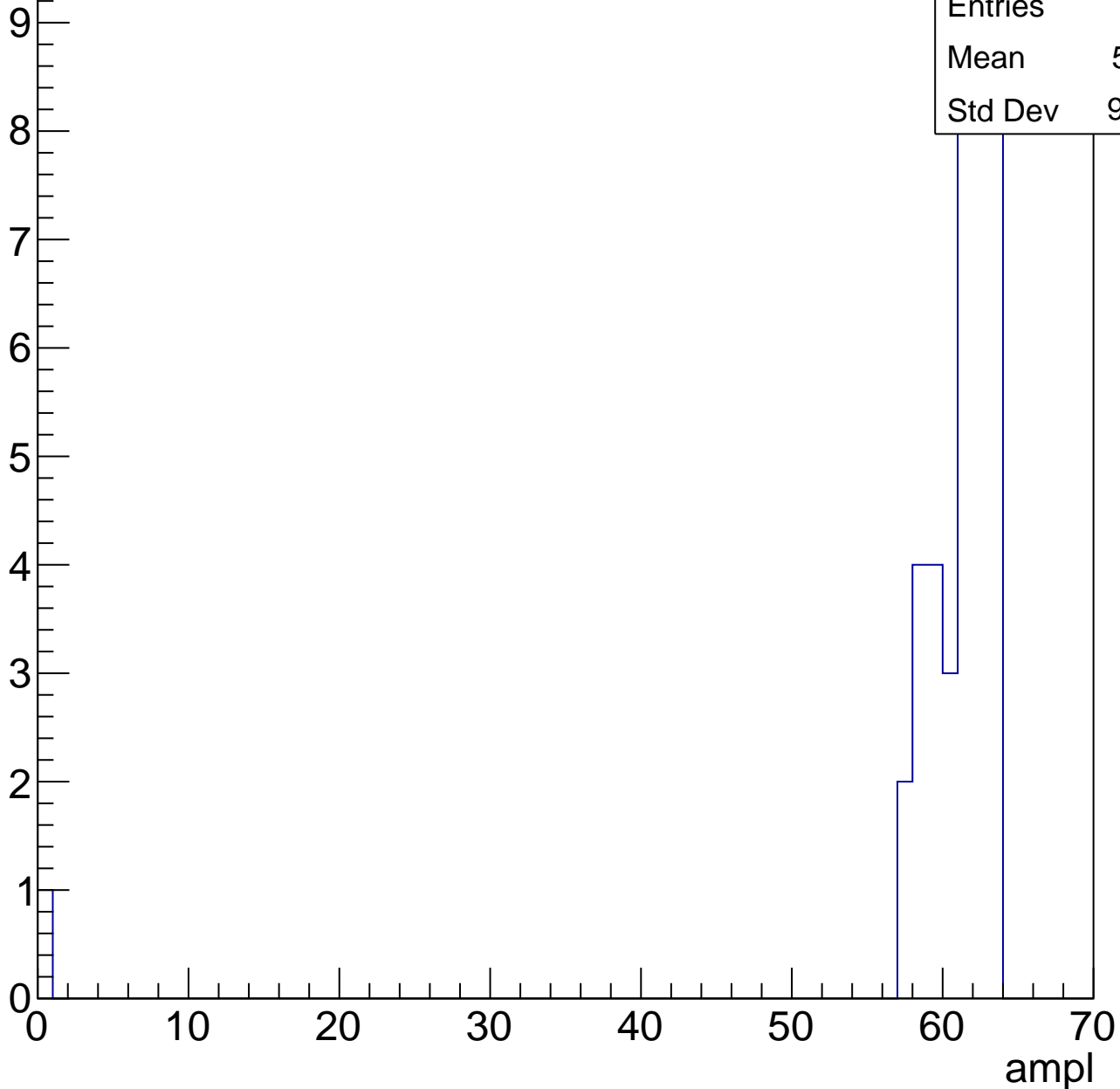


# B1L103S, U11-ch123, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	41
Mean	59.41
Std Dev	9.564



# B1L103S, U11-ch123, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0



# B1L103S, U11-ch123, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U11-ch124, adc0

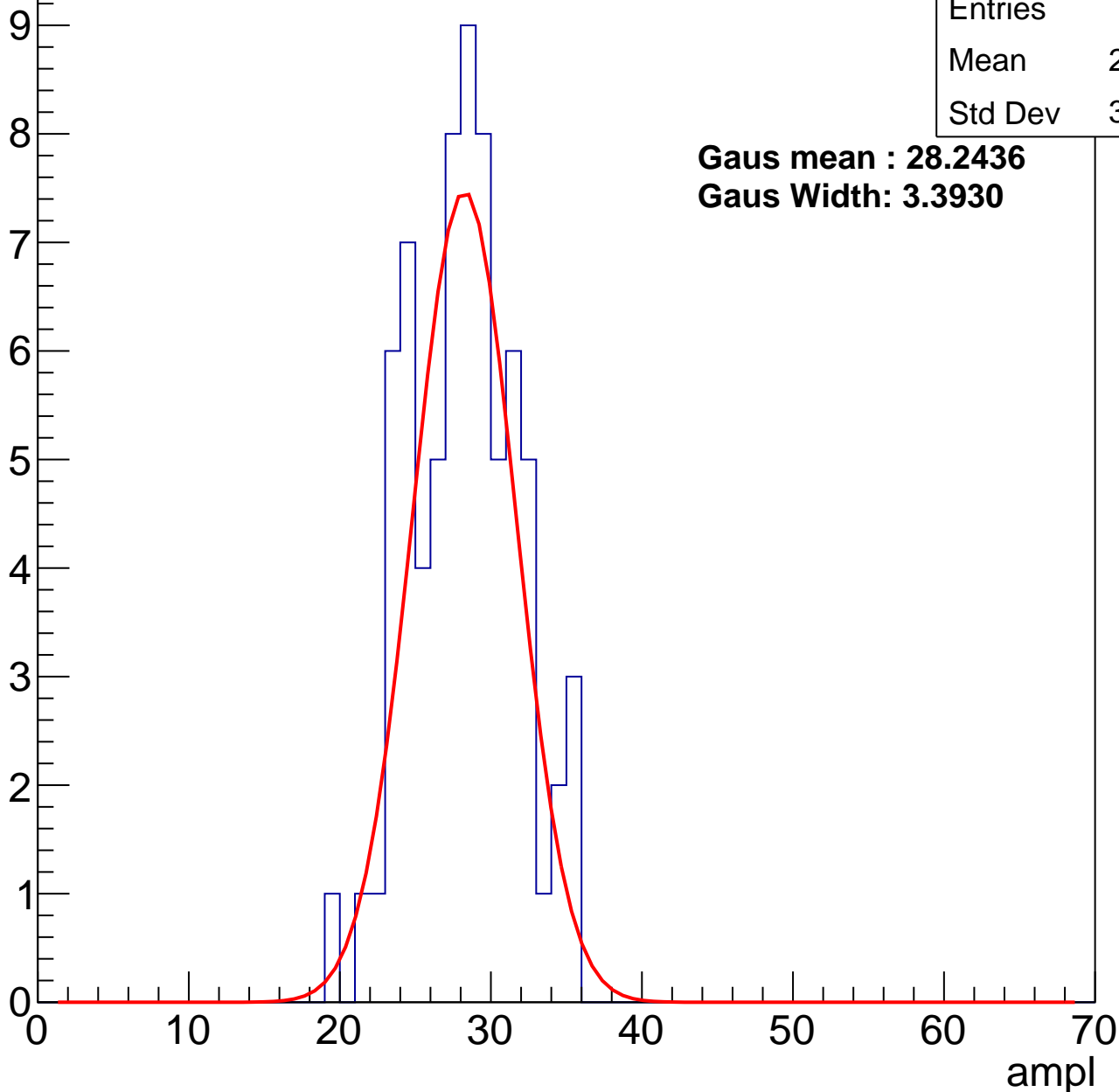
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	72
Mean	27.78
Std Dev	3.525

**Gaus mean : 28.2436**

**Gaus Width: 3.3930**



# B1L103S, U11-ch124, adc1

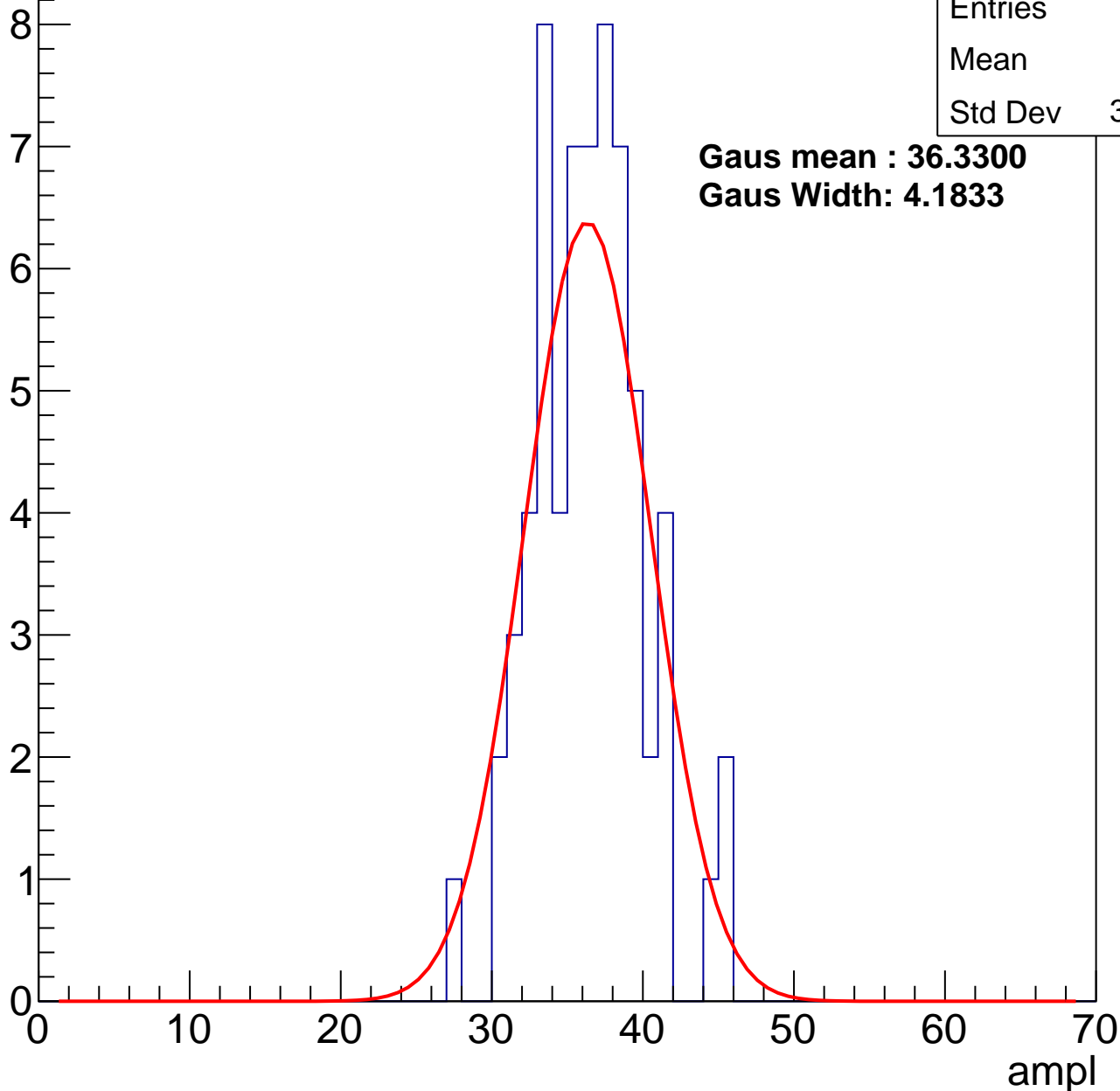
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	36
Std Dev	3.565

**Gaus mean : 36.3300**

**Gaus Width: 4.1833**



# B1L103S, U11-ch124, adc2

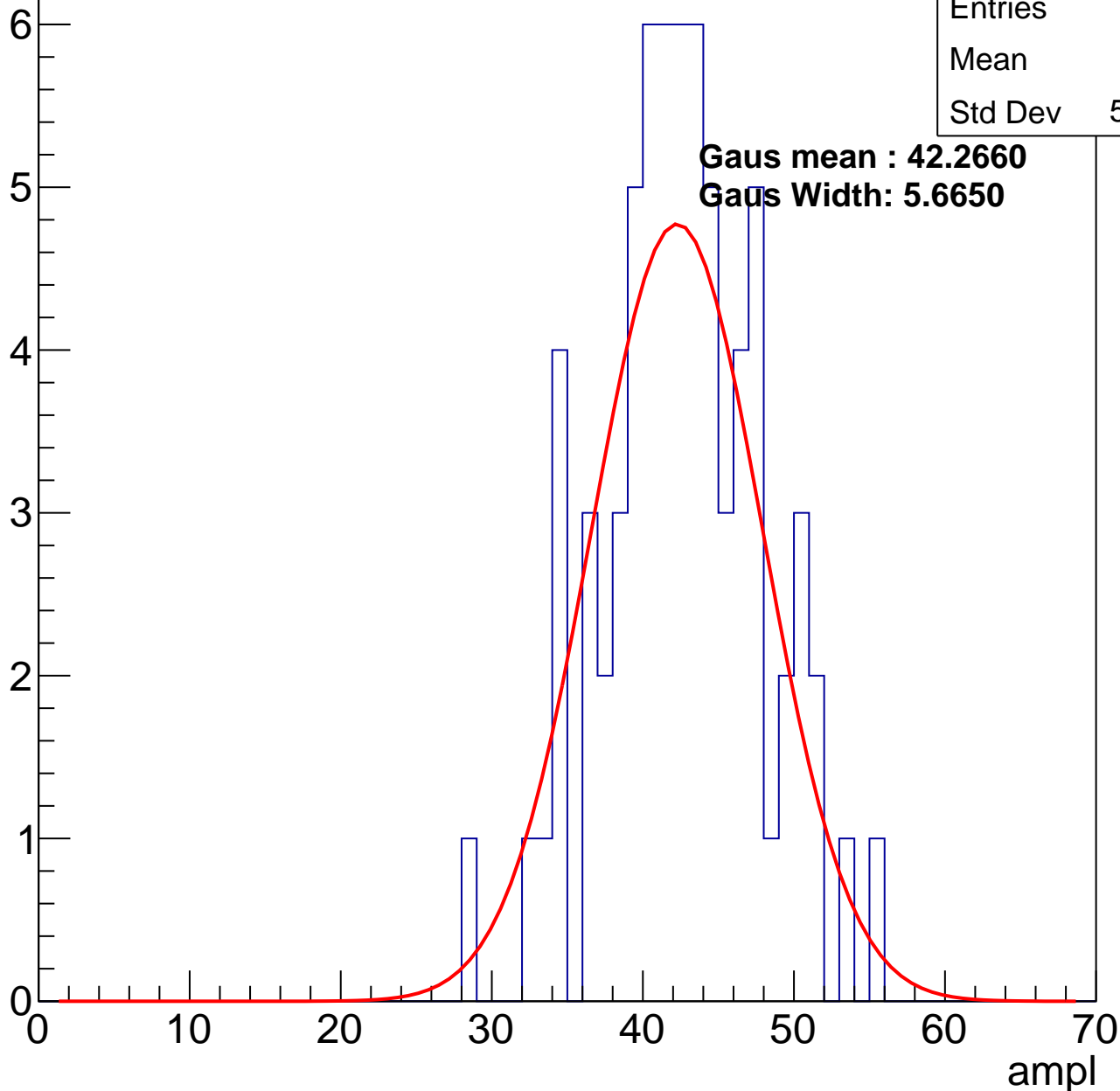
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	71
Mean	42.2
Std Dev	5.215

**Gaus mean : 42.2660**

**Gaus Width: 5.6650**

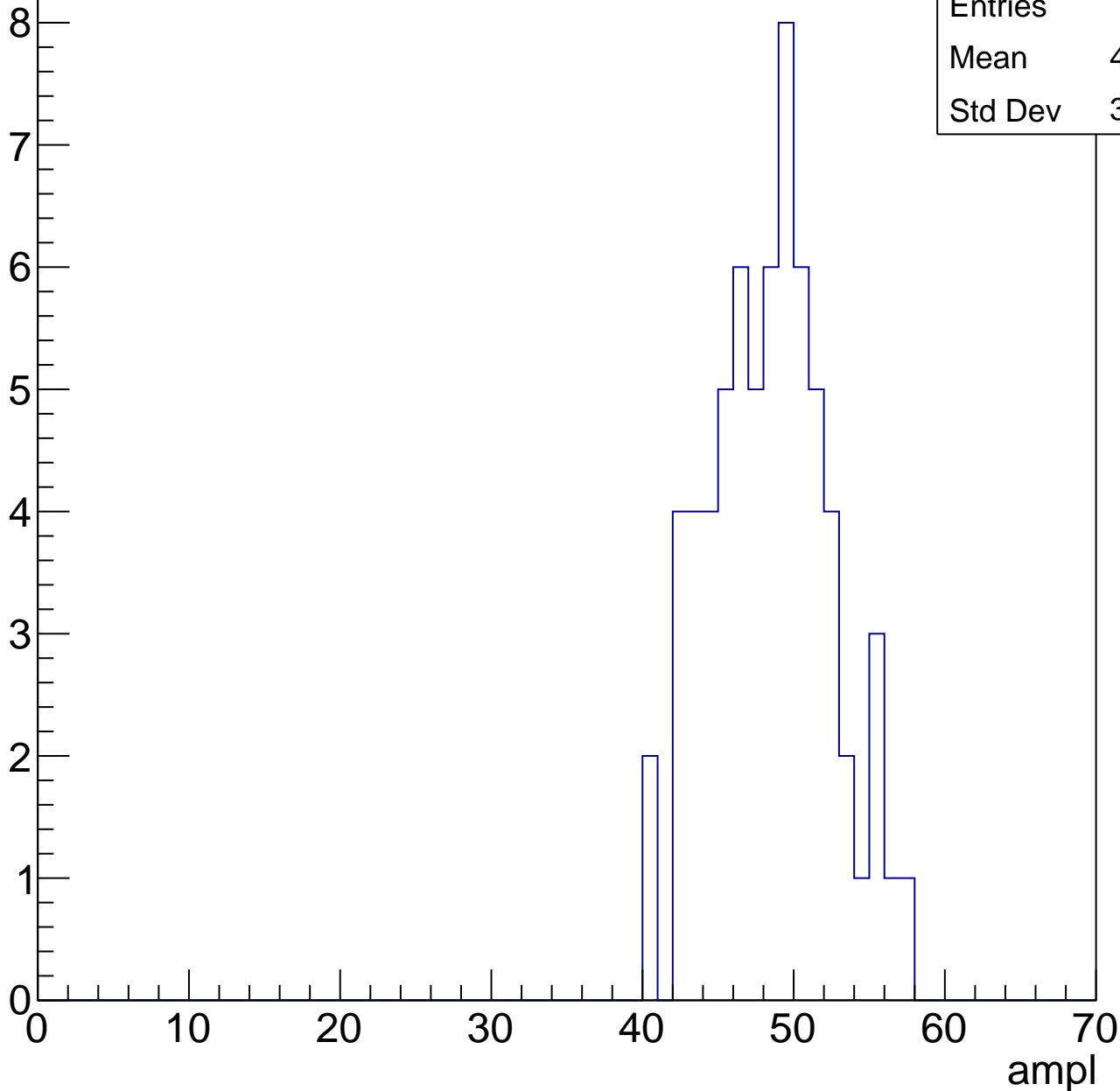


# B1L103S, U11-ch124, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	47.96
Std Dev	3.919

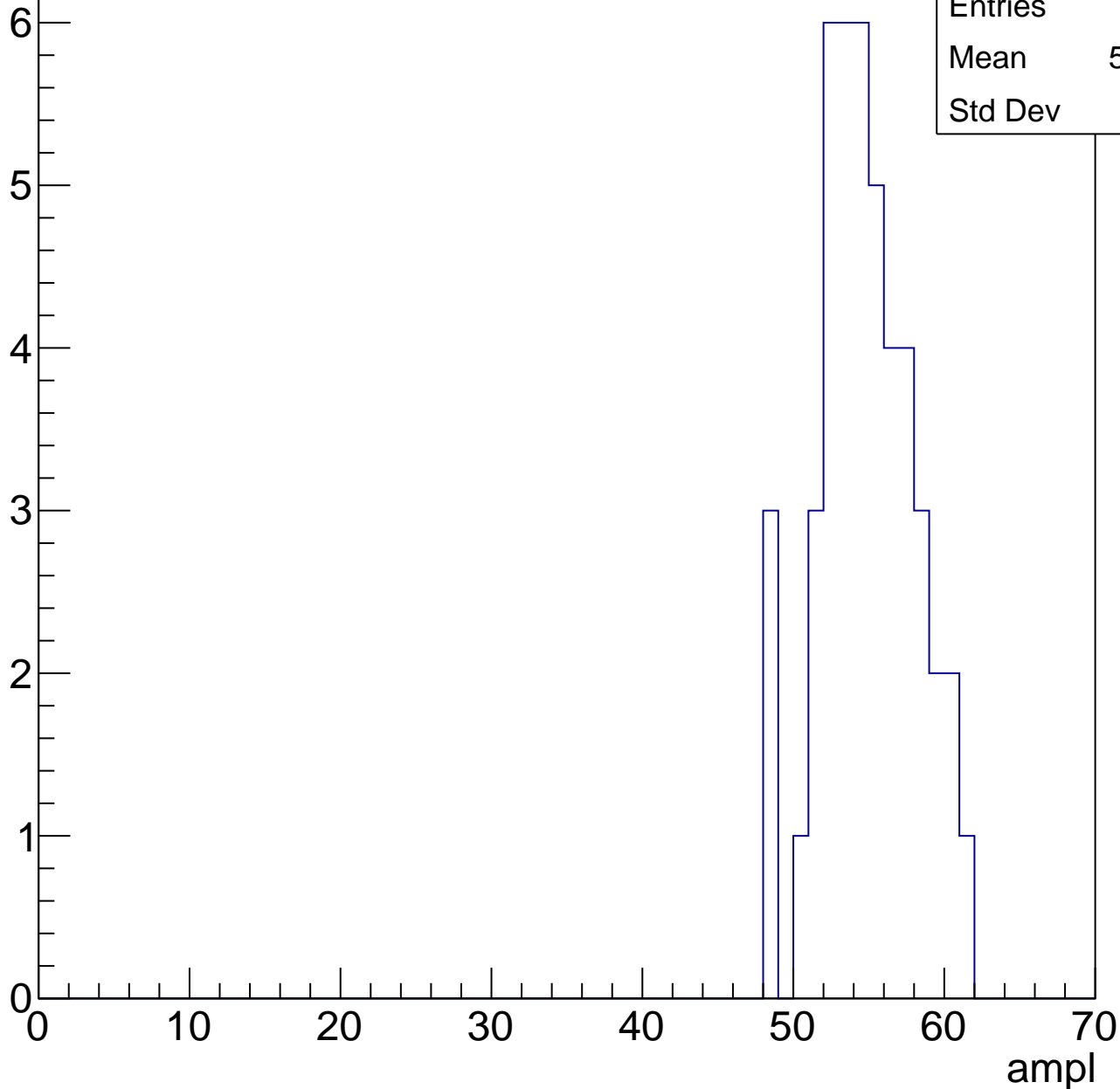


# B1L103S, U11-ch124, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	46
Mean	54.37
Std Dev	3.13

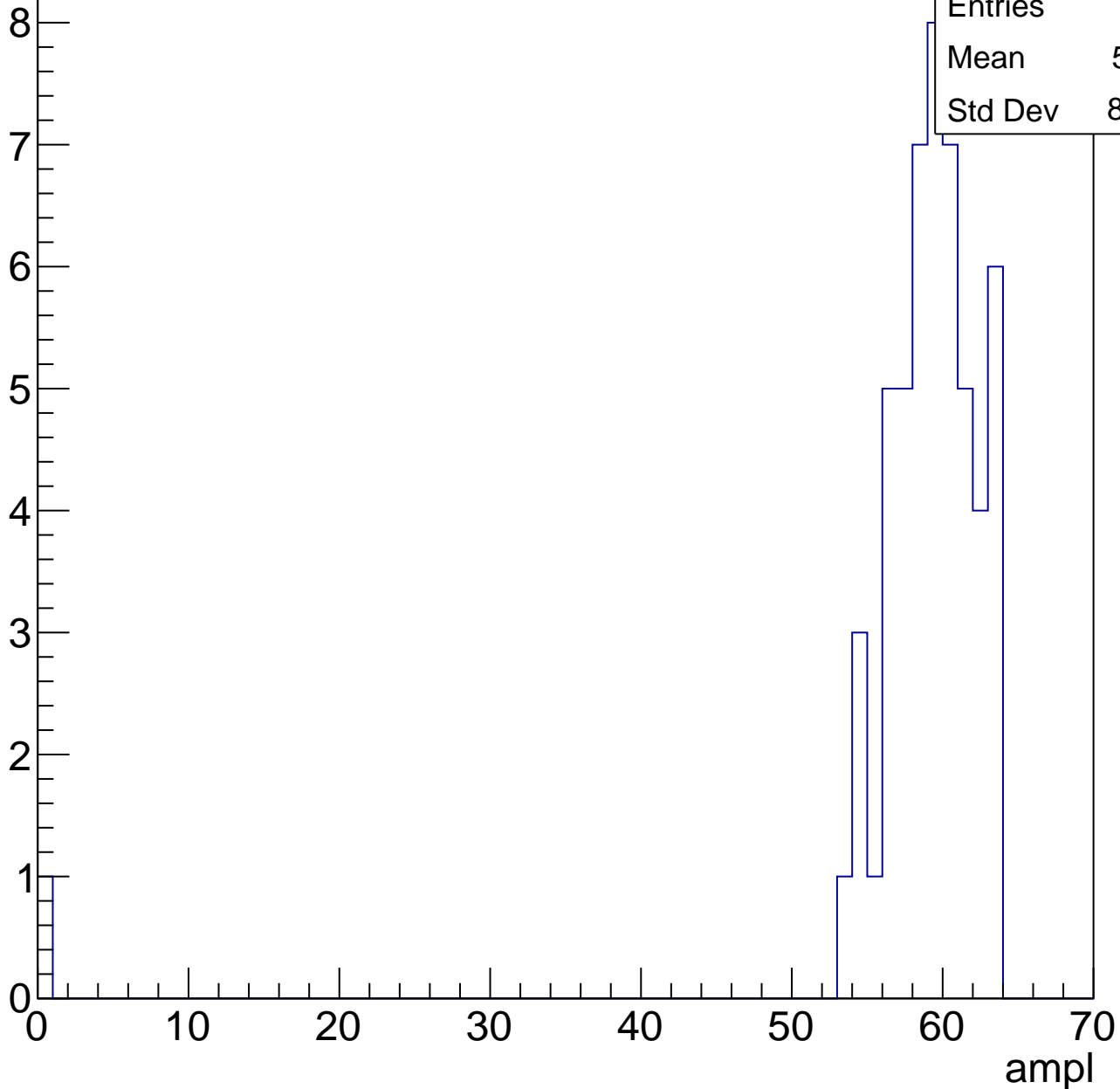


# B1L103S, U11-ch124, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	53
Mean	57.81
Std Dev	8.427

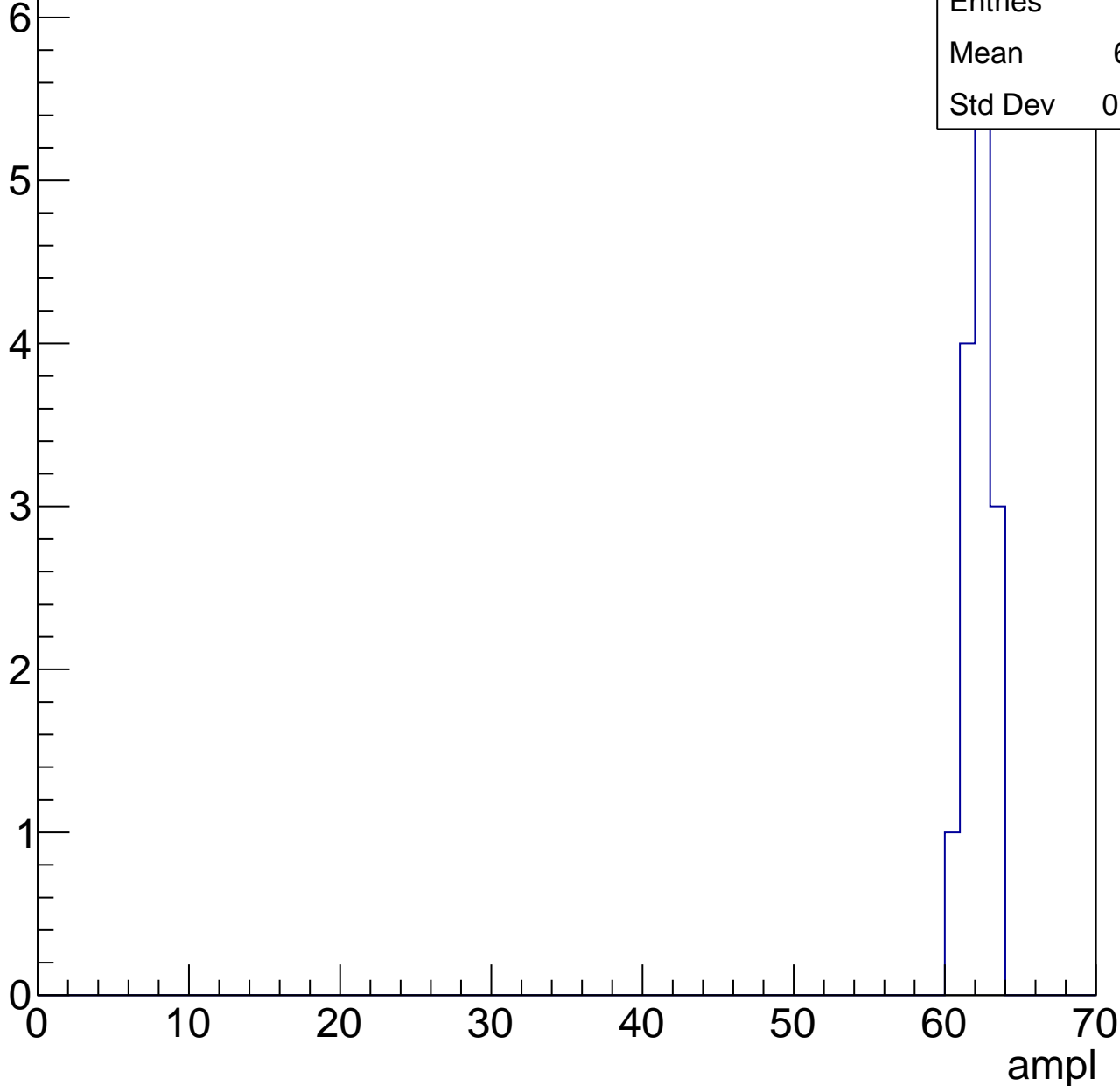


# B1L103S, U11-ch124, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	14
Mean	61.79
Std Dev	0.8601





# B1L103S, U11-ch124, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	3
Mean	21
Std Dev	29.7

# B1L103S, U11-ch125, adc0

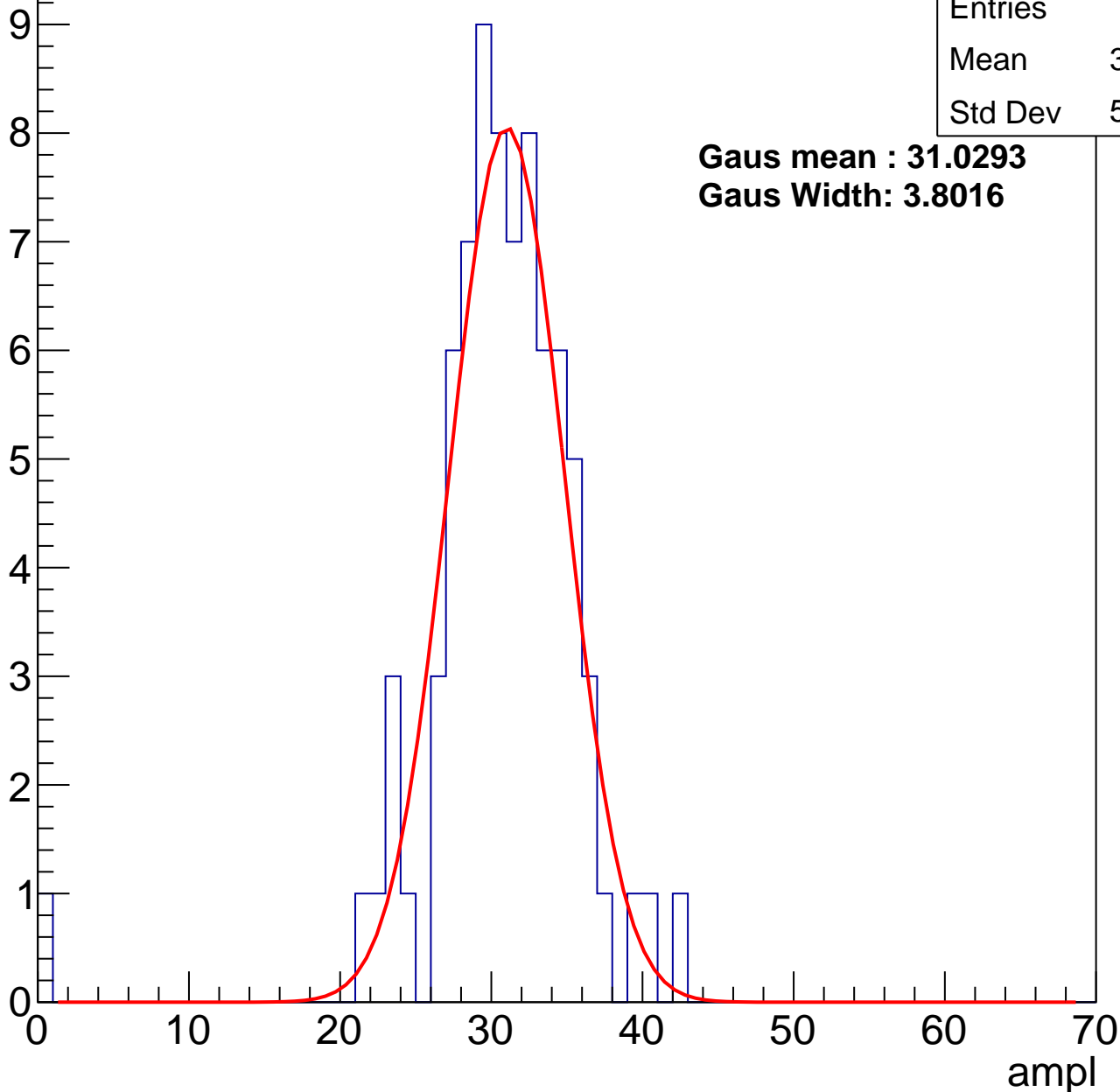
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	79
Mean	30.24
Std Dev	5.227

**Gaus mean : 31.0293**

**Gaus Width: 3.8016**



# B1L103S, U11-ch125, adc1

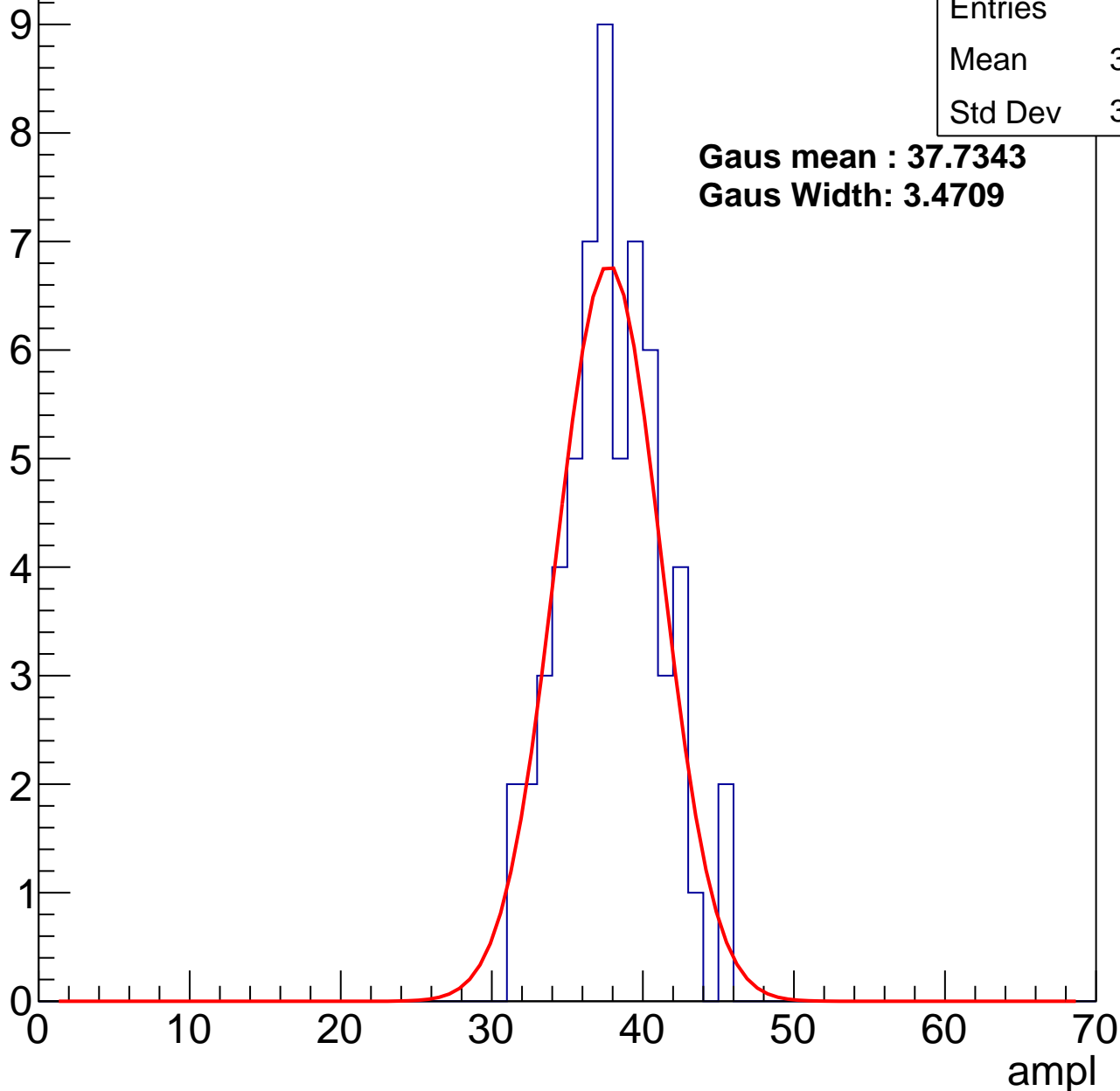
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	60
Mean	37.47
Std Dev	3.212

**Gaus mean : 37.7343**

**Gaus Width: 3.4709**



# B1L103S, U11-ch125, adc2

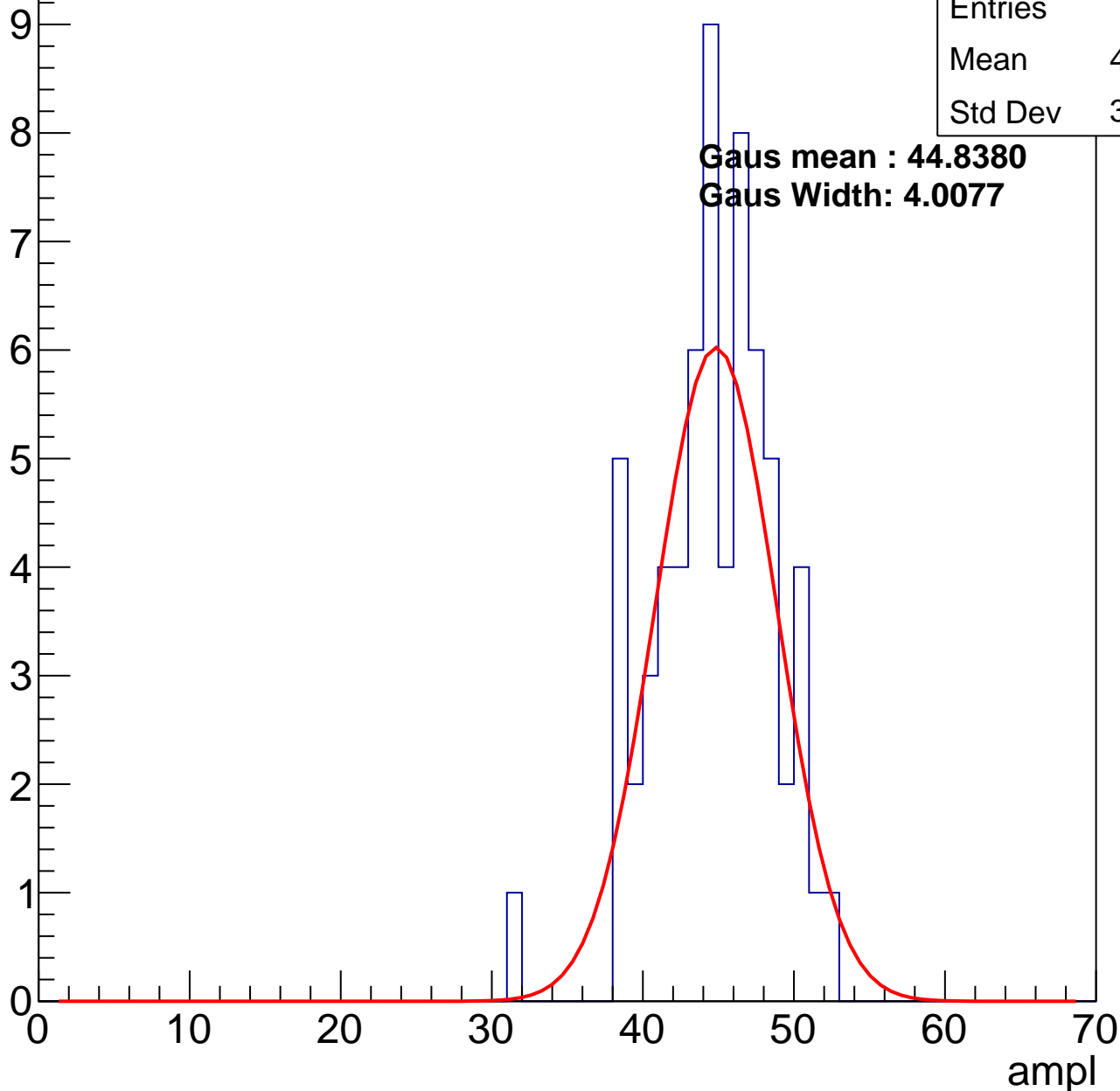
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	44.25
Std Dev	3.879

**Gaus mean : 44.8380**

**Gaus Width: 4.0077**

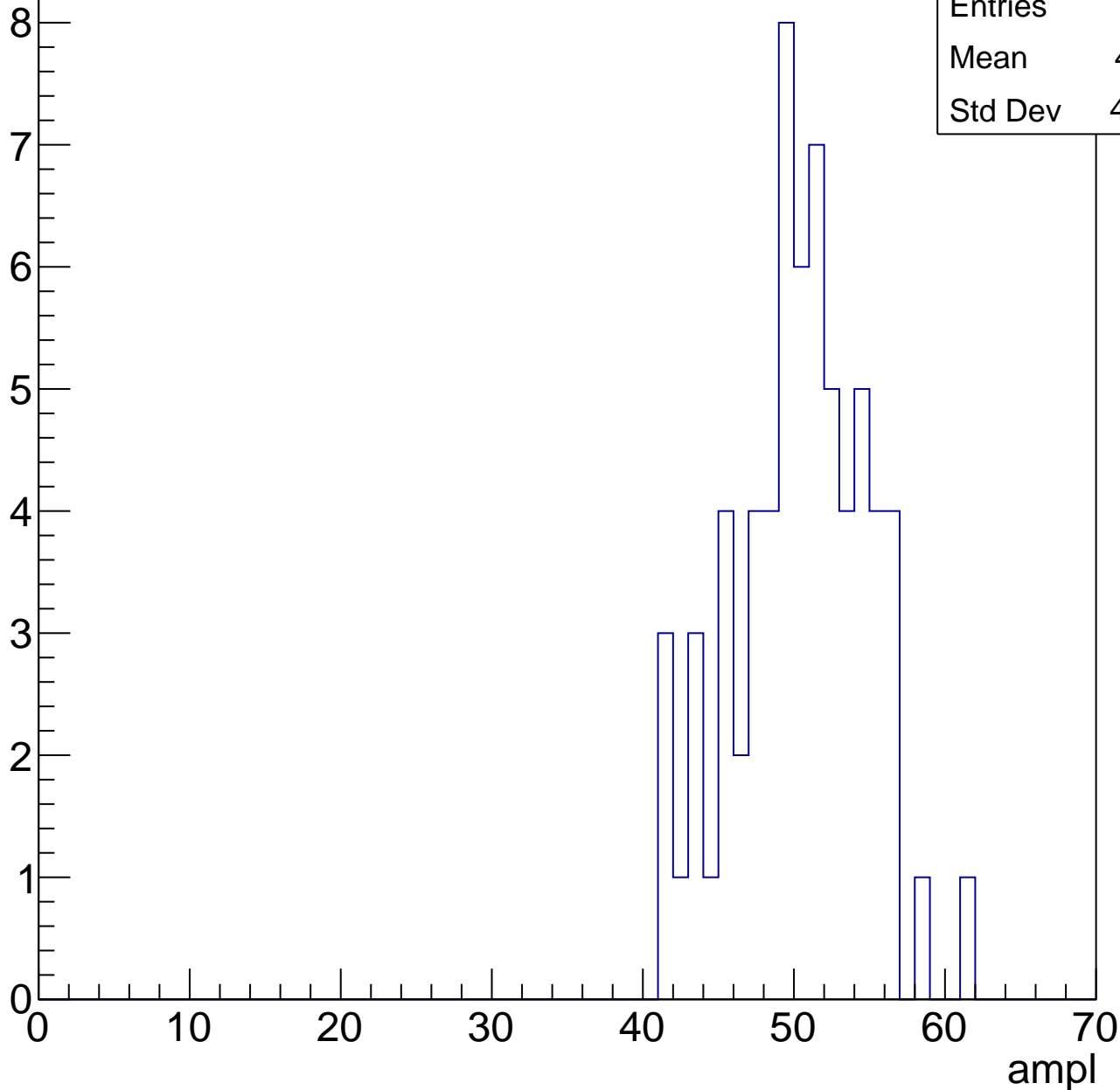


# B1L103S, U11-ch125, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	49.91
Std Dev	4.325

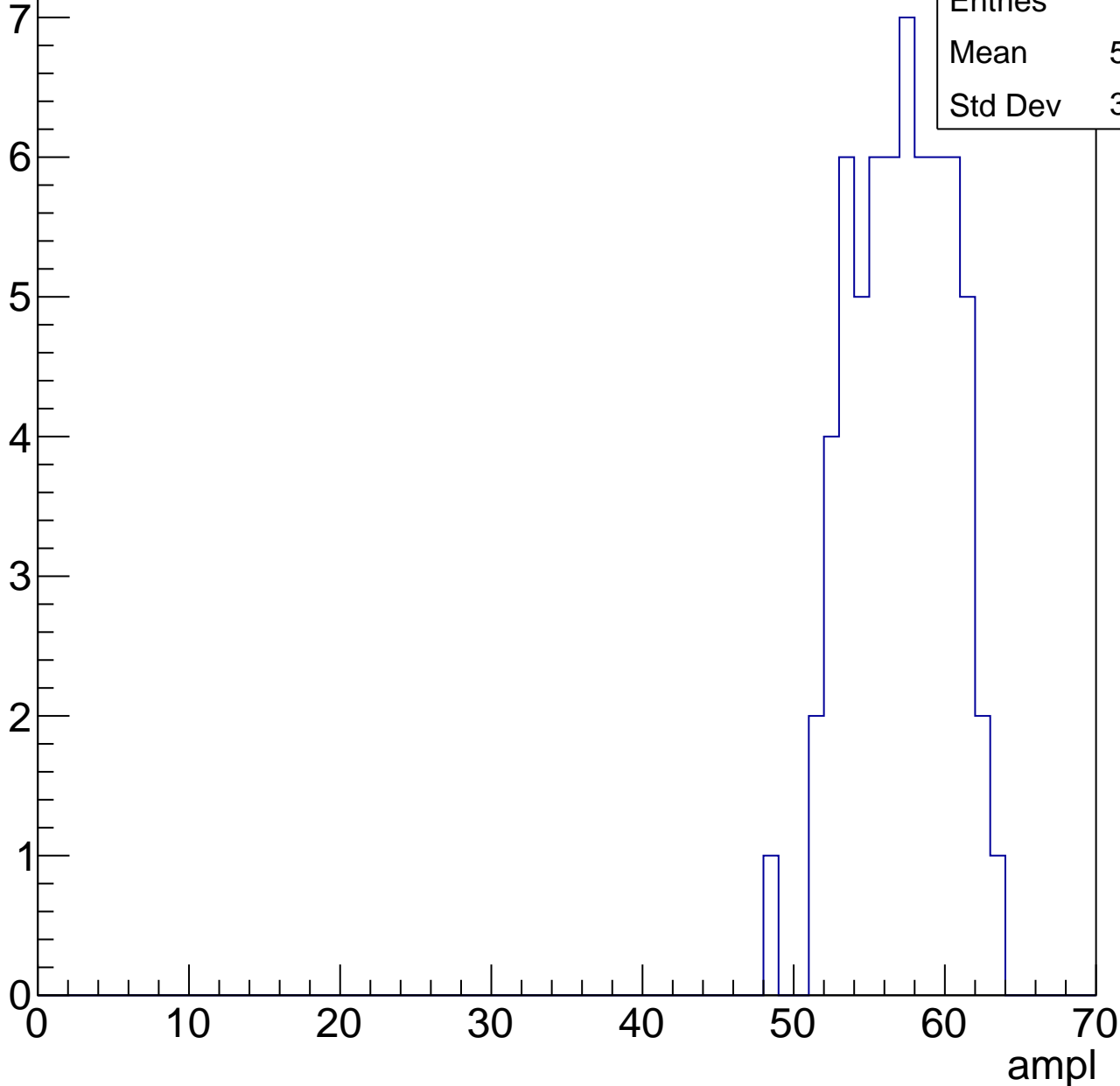


# B1L103S, U11-ch125, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	56.59
Std Dev	3.245

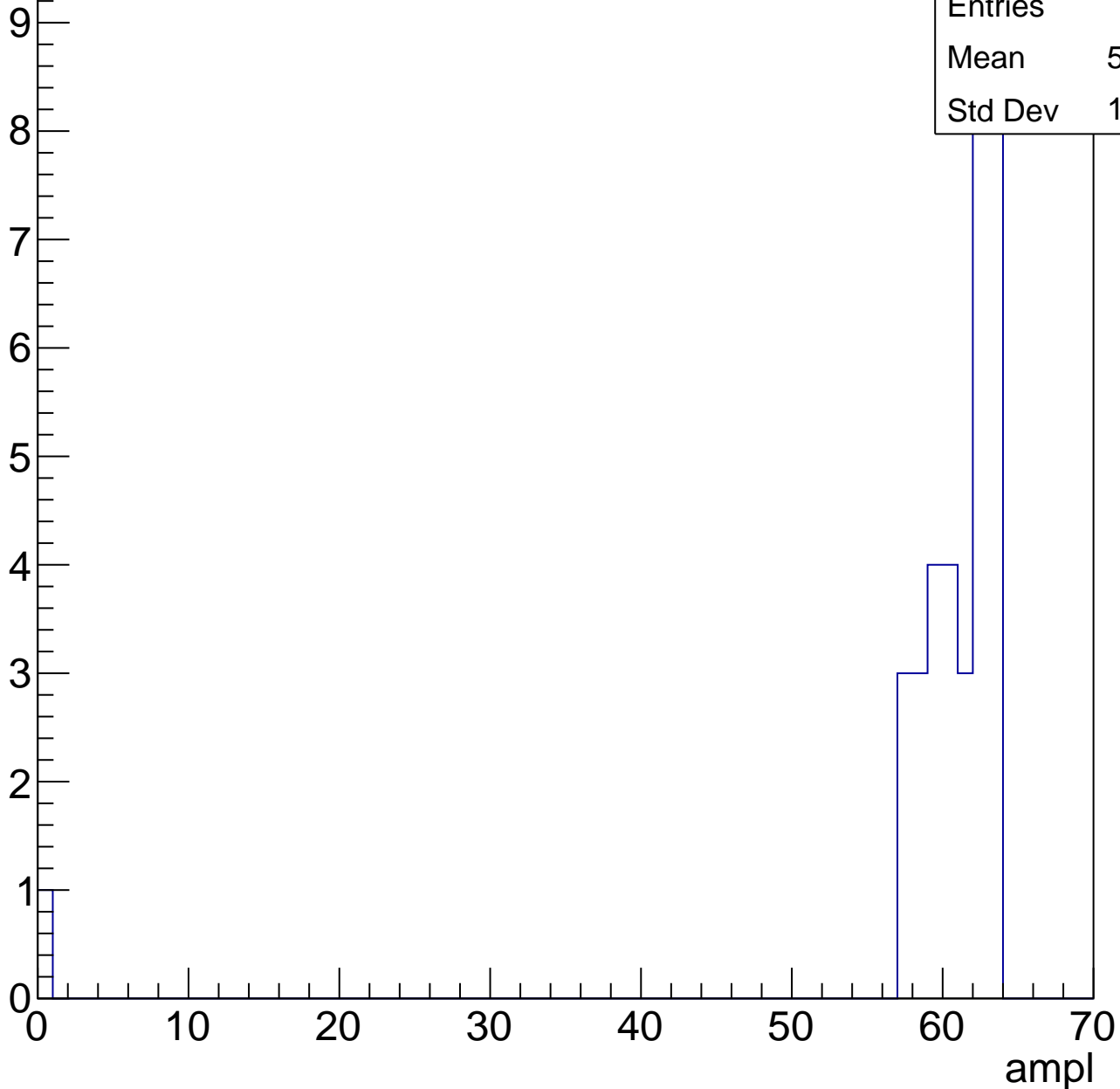


# B1L103S, U11-ch125, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	35
Mean	59.06
Std Dev	10.32



# B1L103S, U11-ch125, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

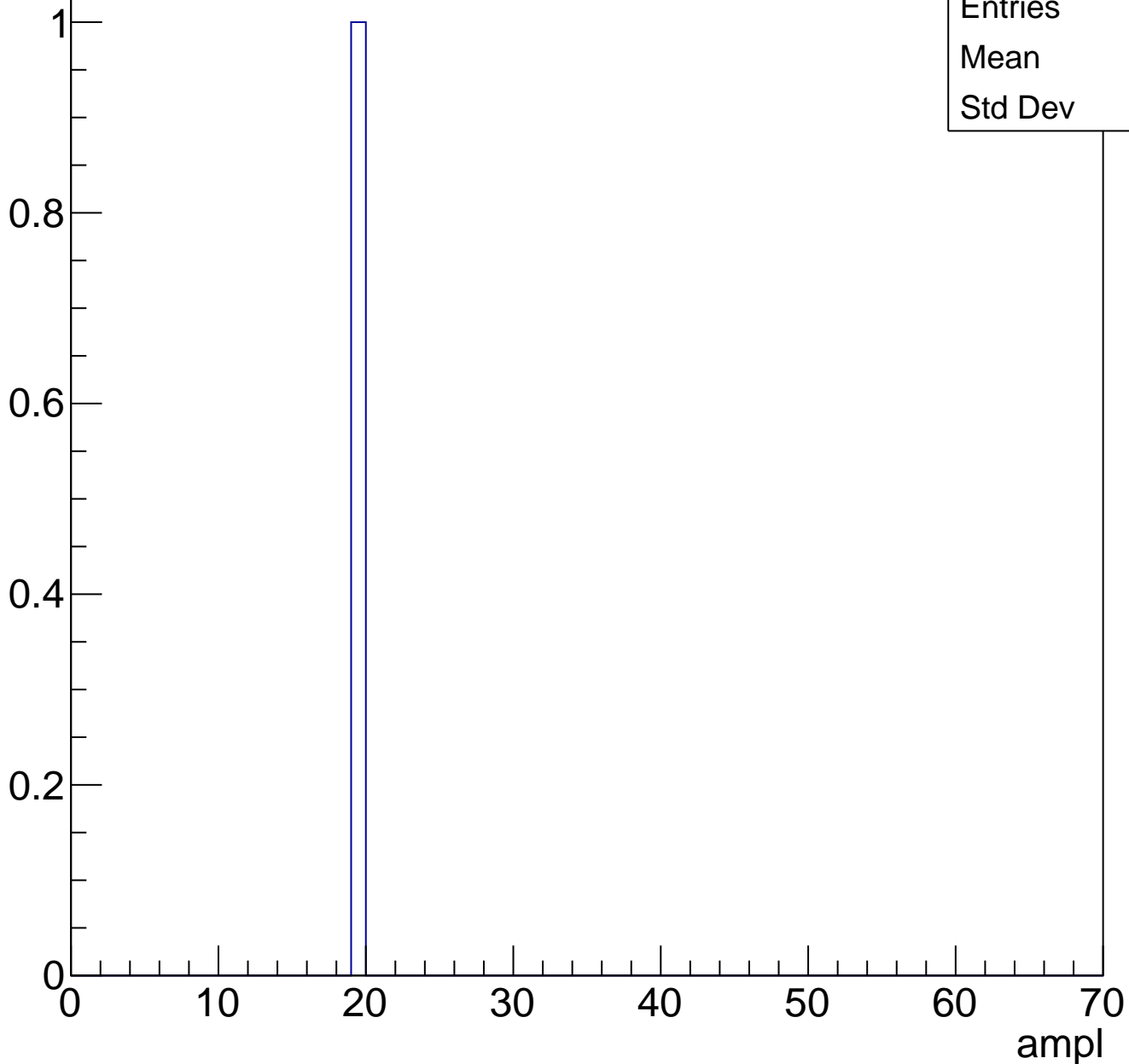




# B1L103S, U11-ch125, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U11-ch126, adc0

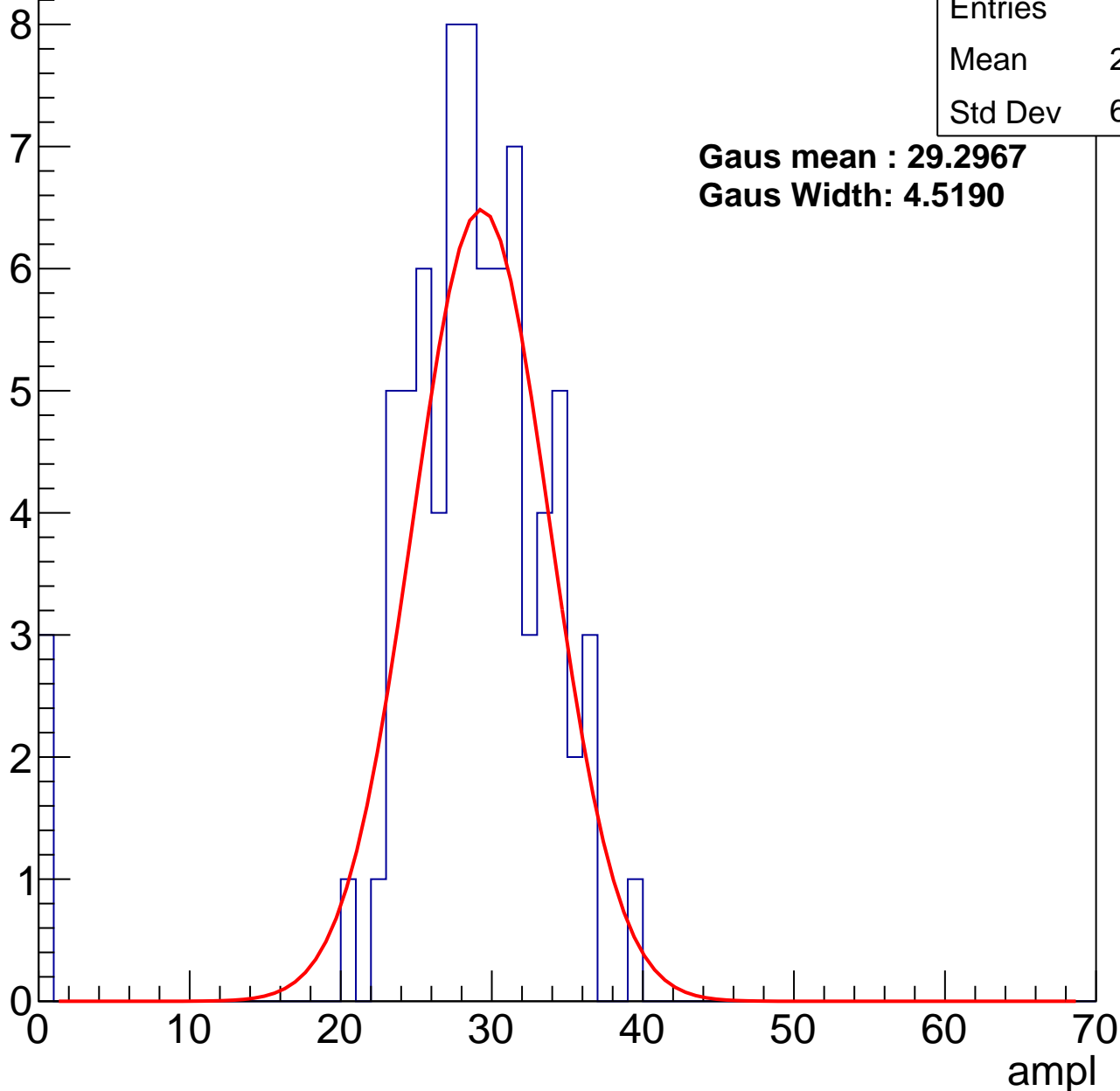
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	78
Mean	27.65
Std Dev	6.754

**Gaus mean : 29.2967**

**Gaus Width: 4.5190**



# B1L103S, U11-ch126, adc1

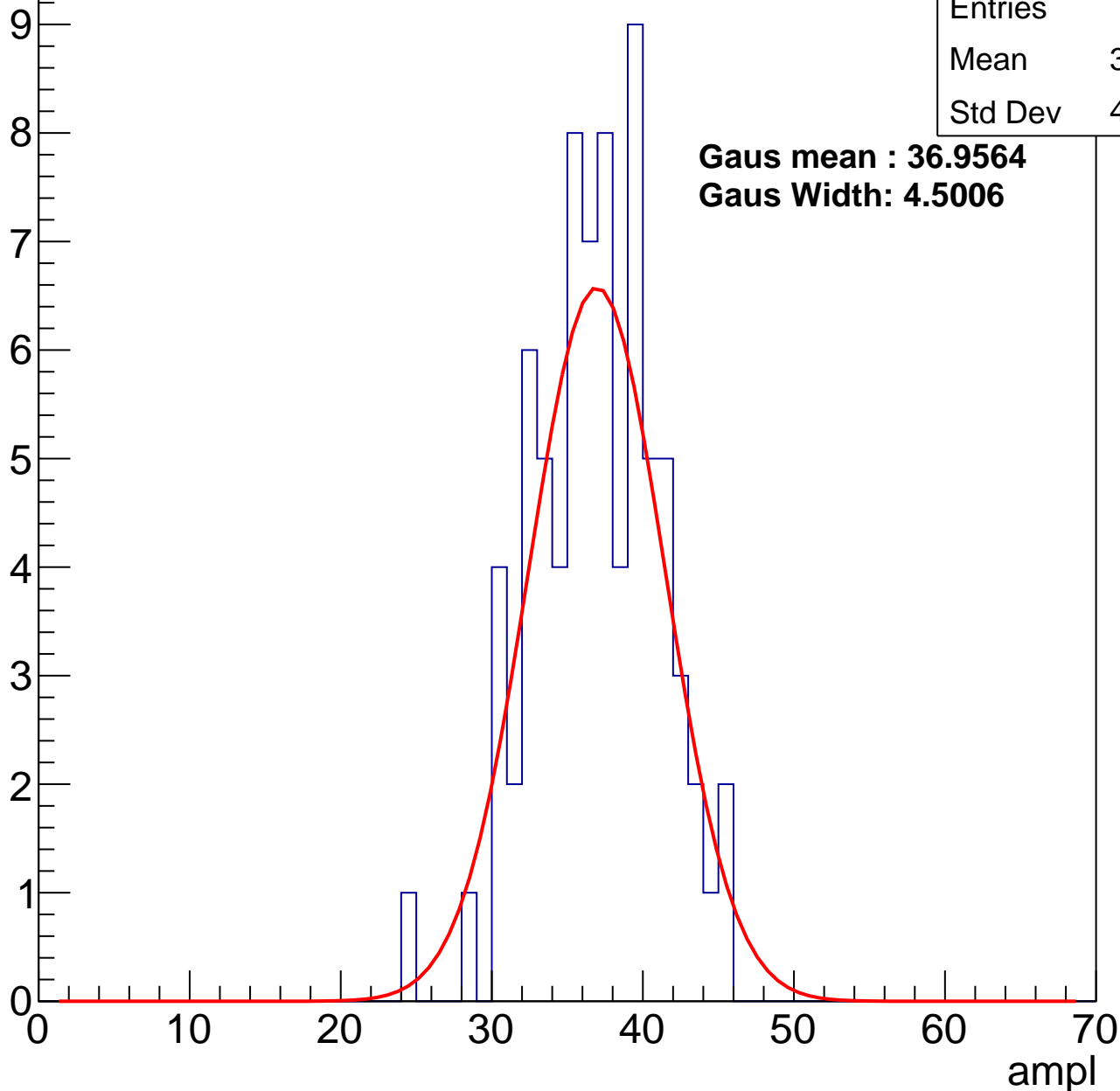
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	77
Mean	36.48
Std Dev	4.095

**Gaus mean : 36.9564**

**Gaus Width: 4.5006**



# B1L103S, U11-ch126, adc2

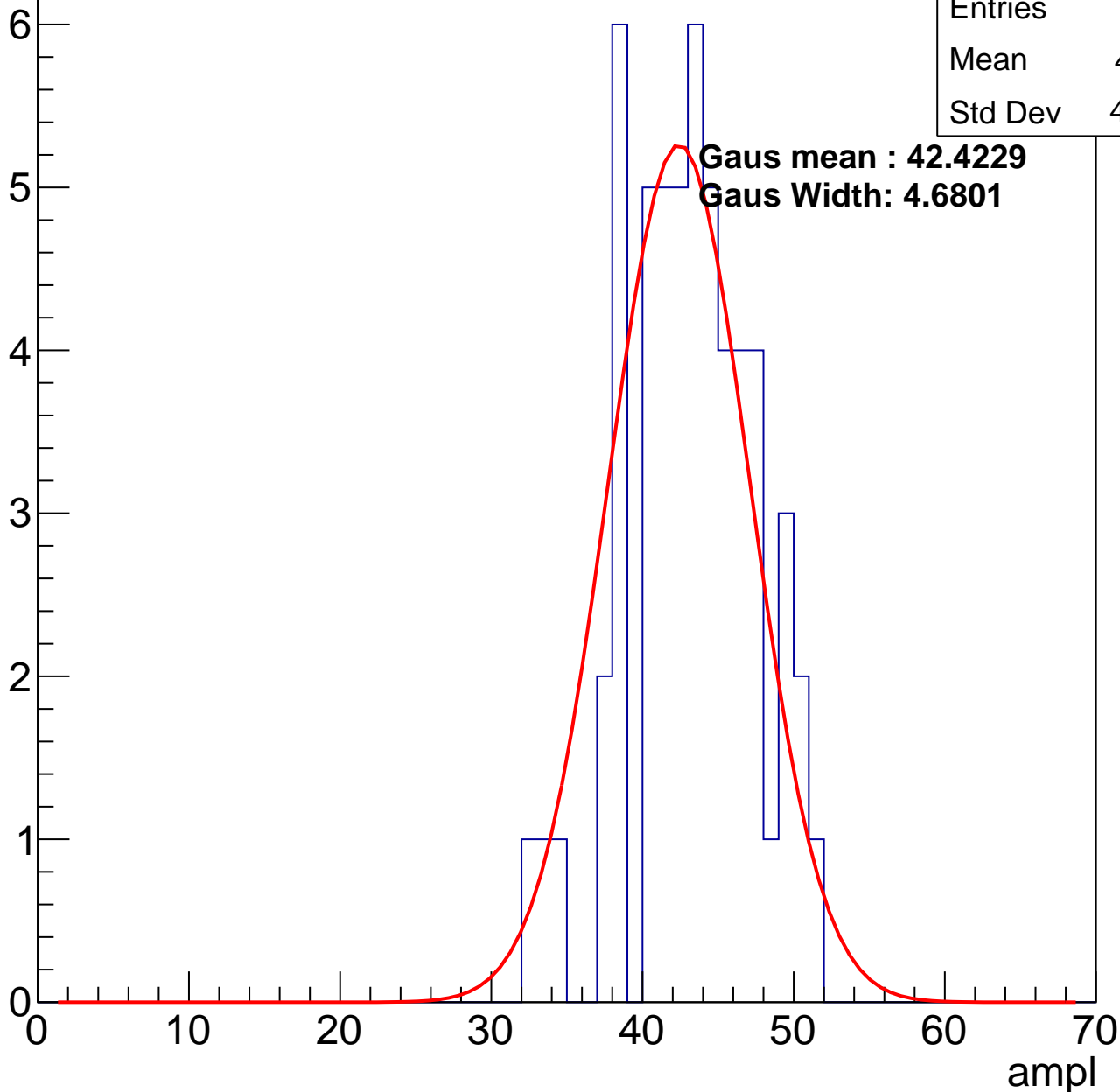
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	56
Mean	42.71
Std Dev	4.237

**Gaus mean : 42.4229**

**Gaus Width: 4.6801**

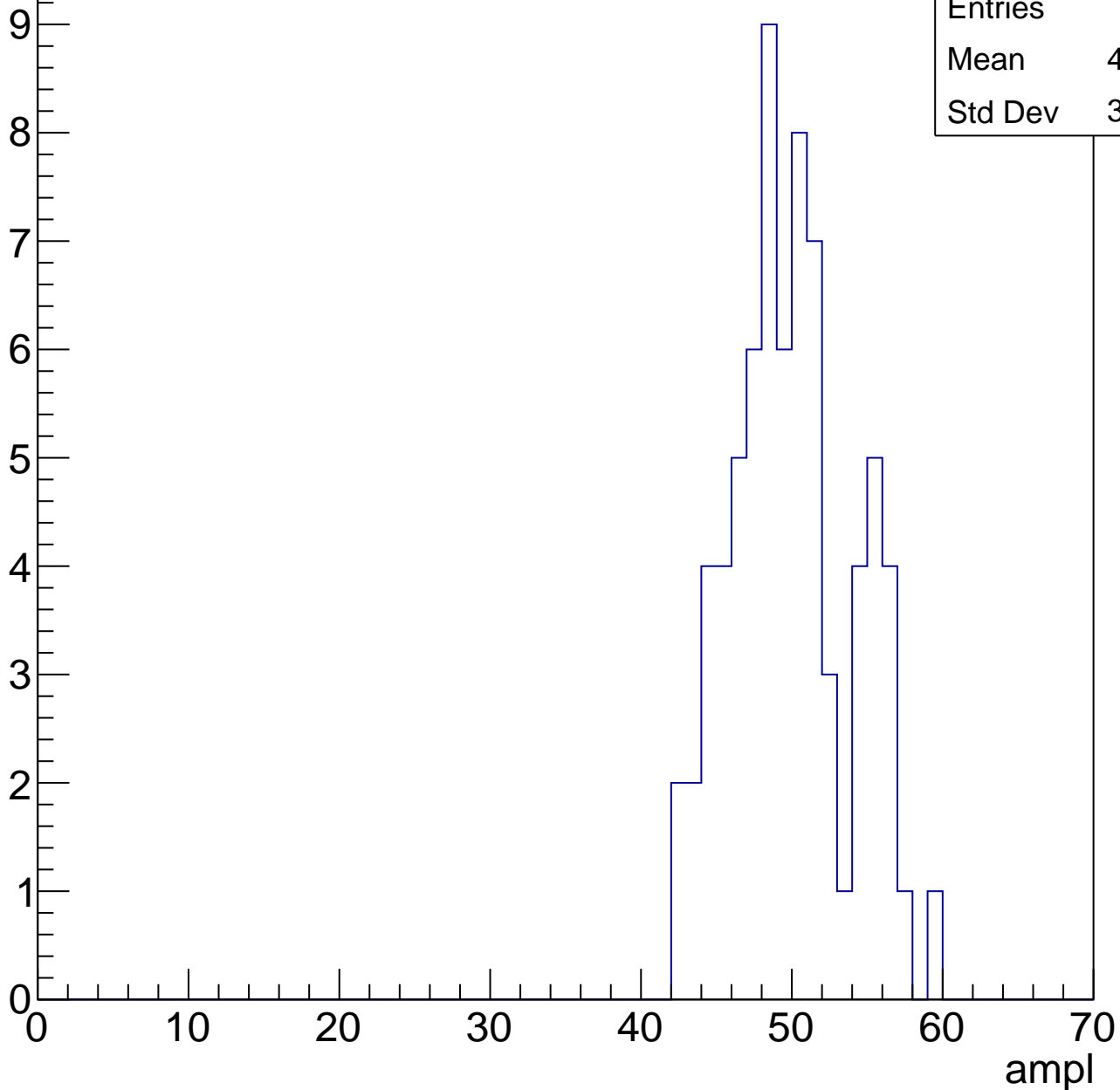


# B1L103S, U11-ch126, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	72
Mean	49.46
Std Dev	3.937

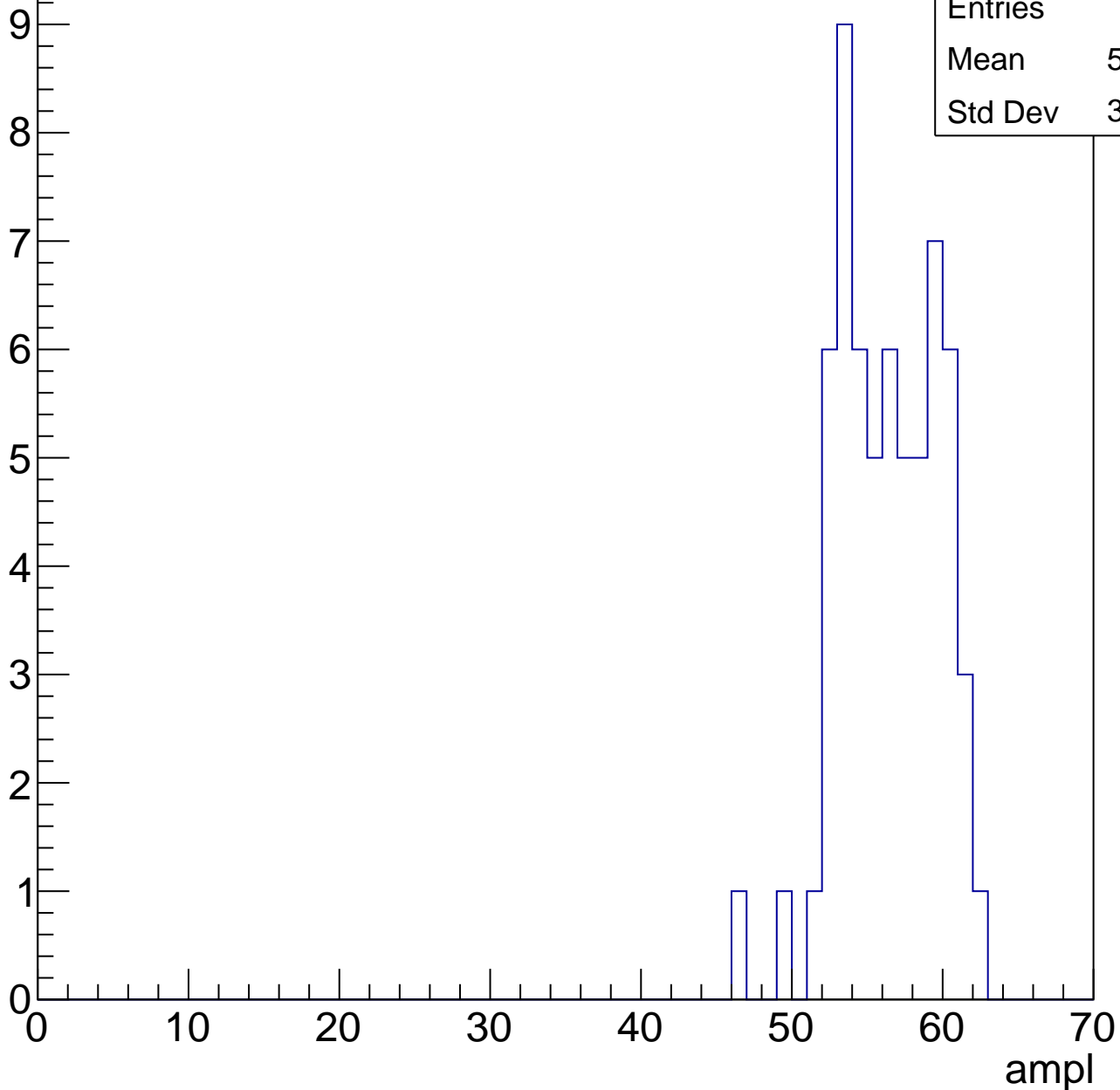


# B1L103S, U11-ch126, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	55.85
Std Dev	3.296

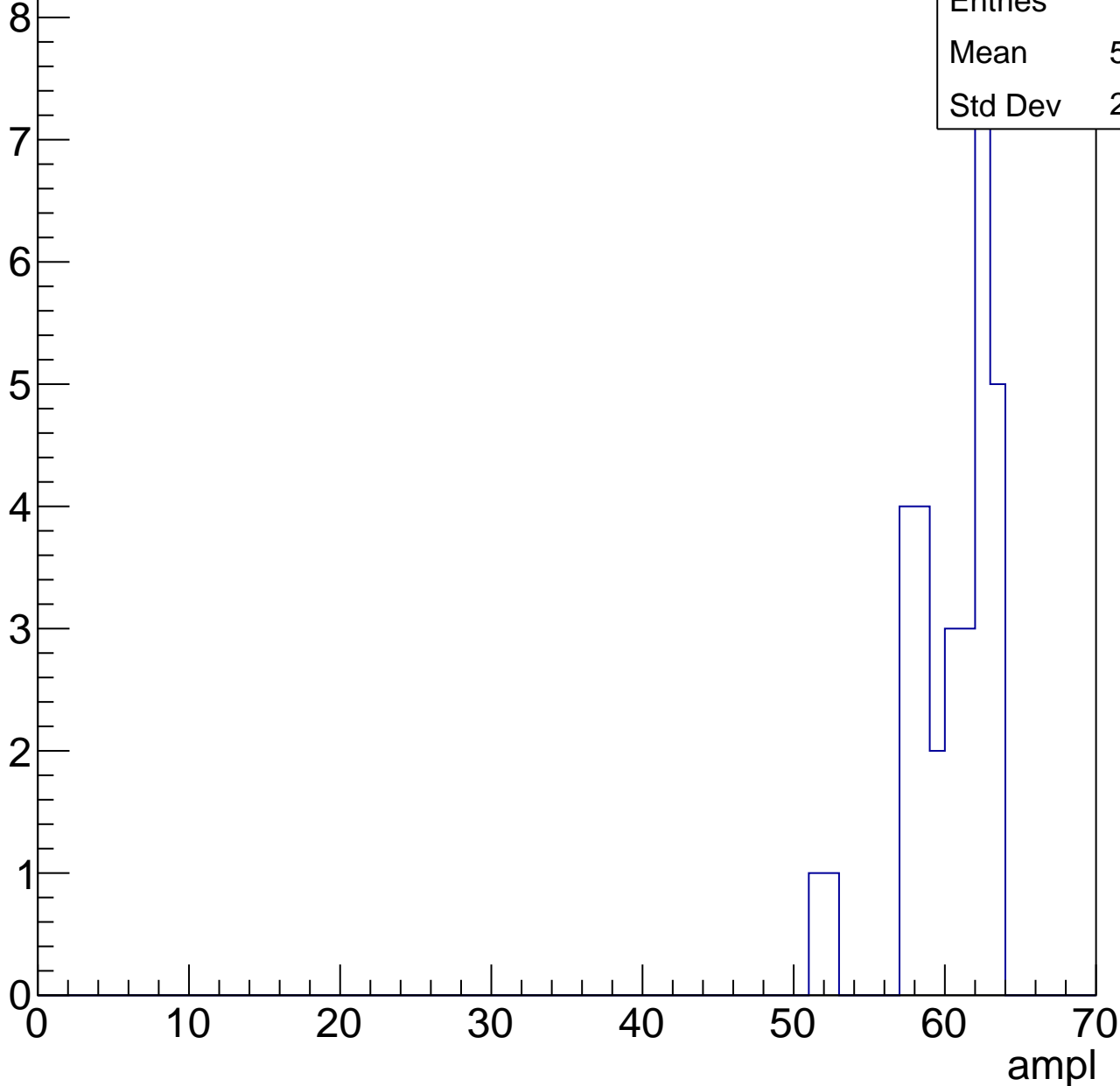


# B1L103S, U11-ch126, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

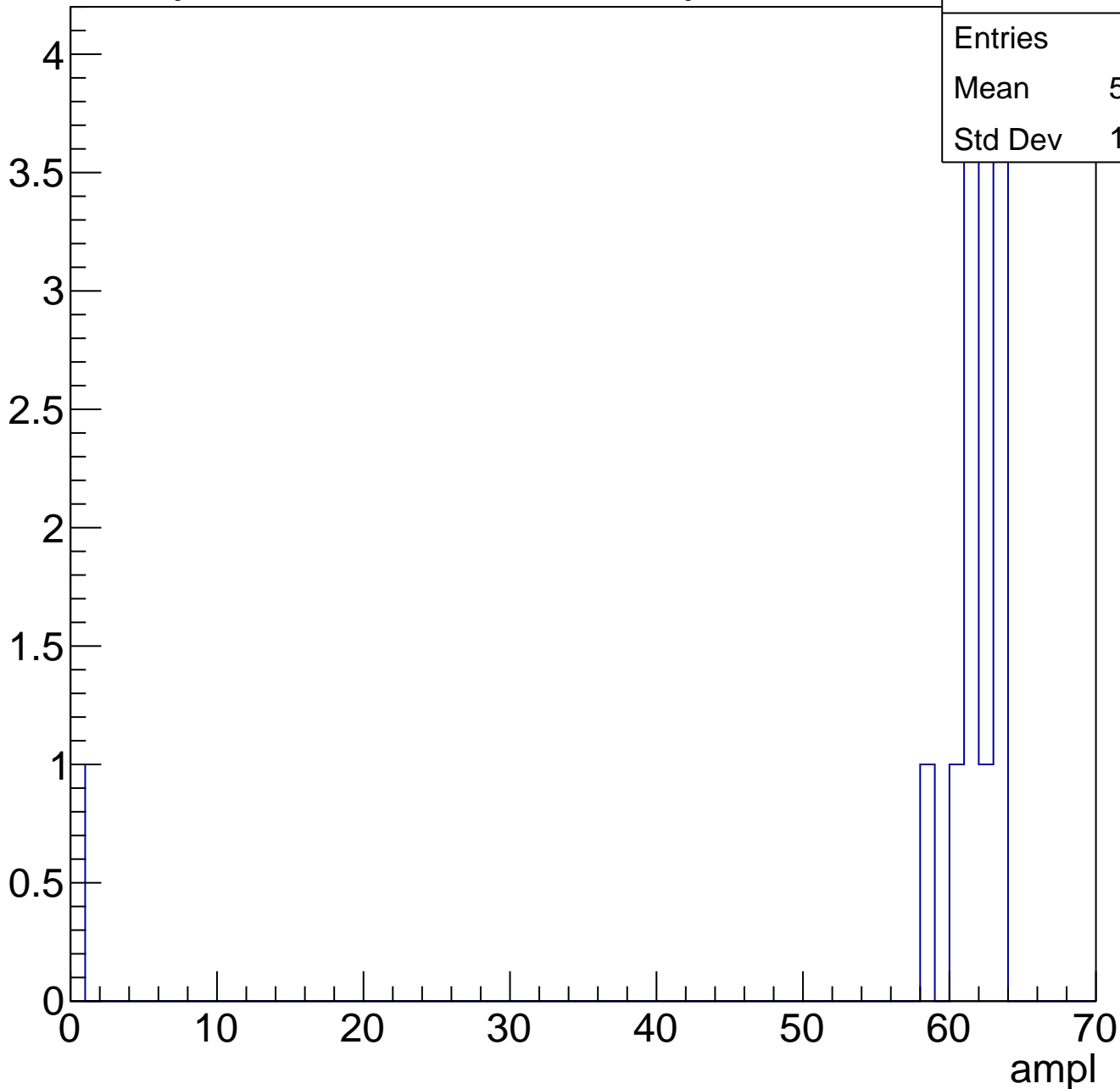
Entries	31
Mean	59.84
Std Dev	2.996



# B1L103S, U11-ch126, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U11-ch126, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U11-ch127, adc0

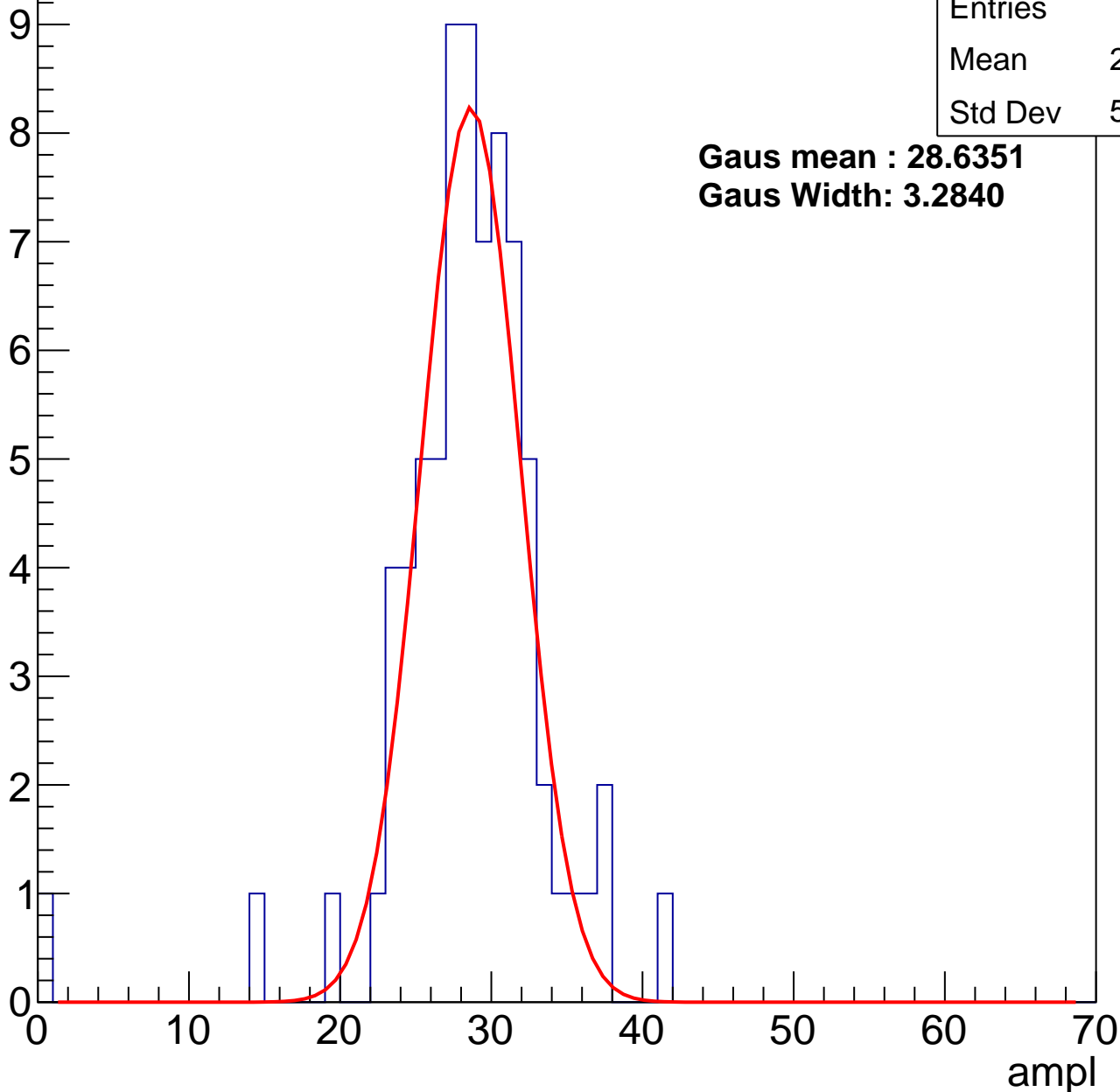
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	75
Mean	27.99
Std Dev	5.224

**Gaus mean : 28.6351**

**Gaus Width: 3.2840**



# B1L103S, U11-ch127, adc1

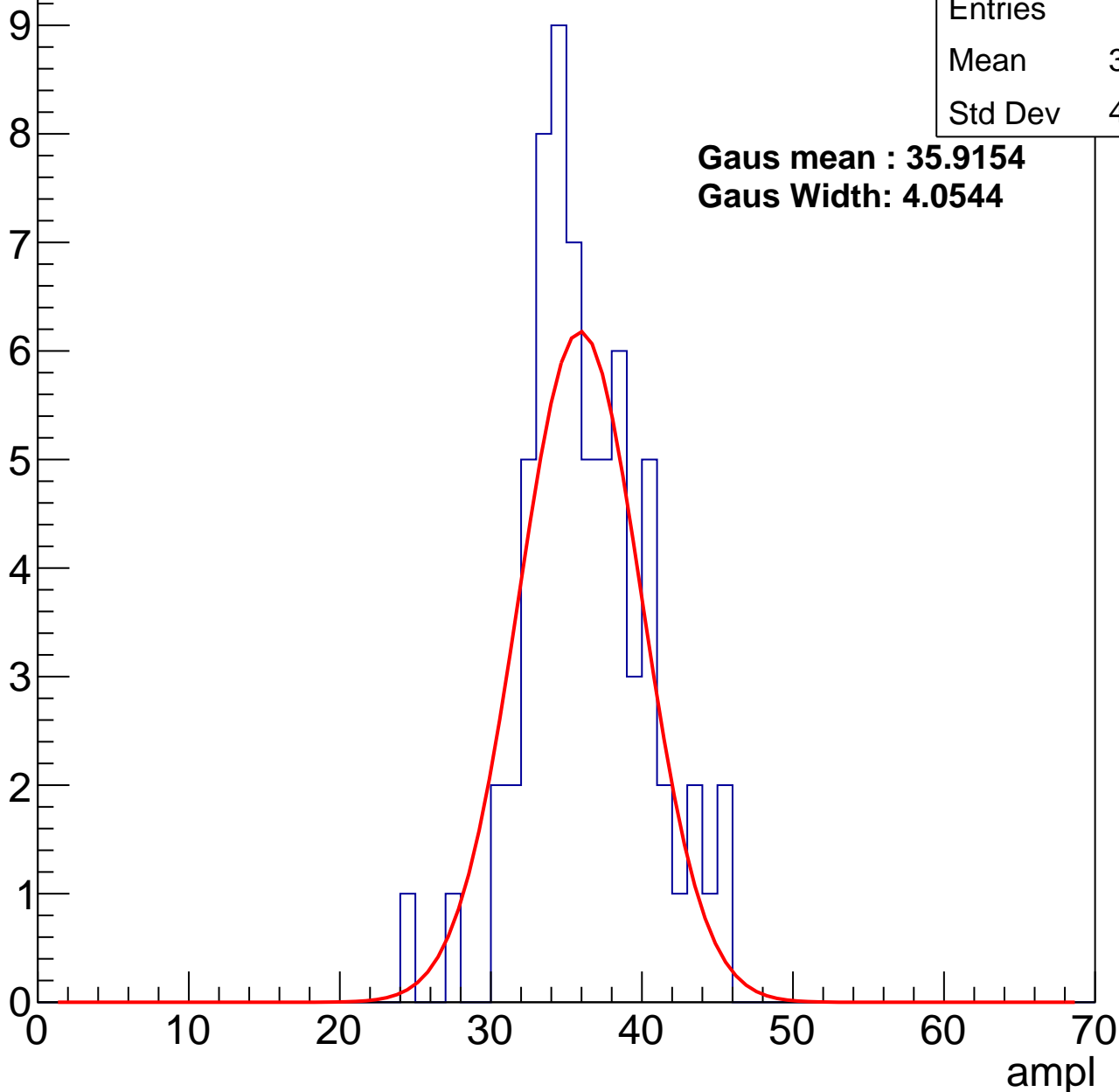
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	35.85
Std Dev	4.027

**Gaus mean : 35.9154**

**Gaus Width: 4.0544**



# B1L103S, U11-ch127, adc2

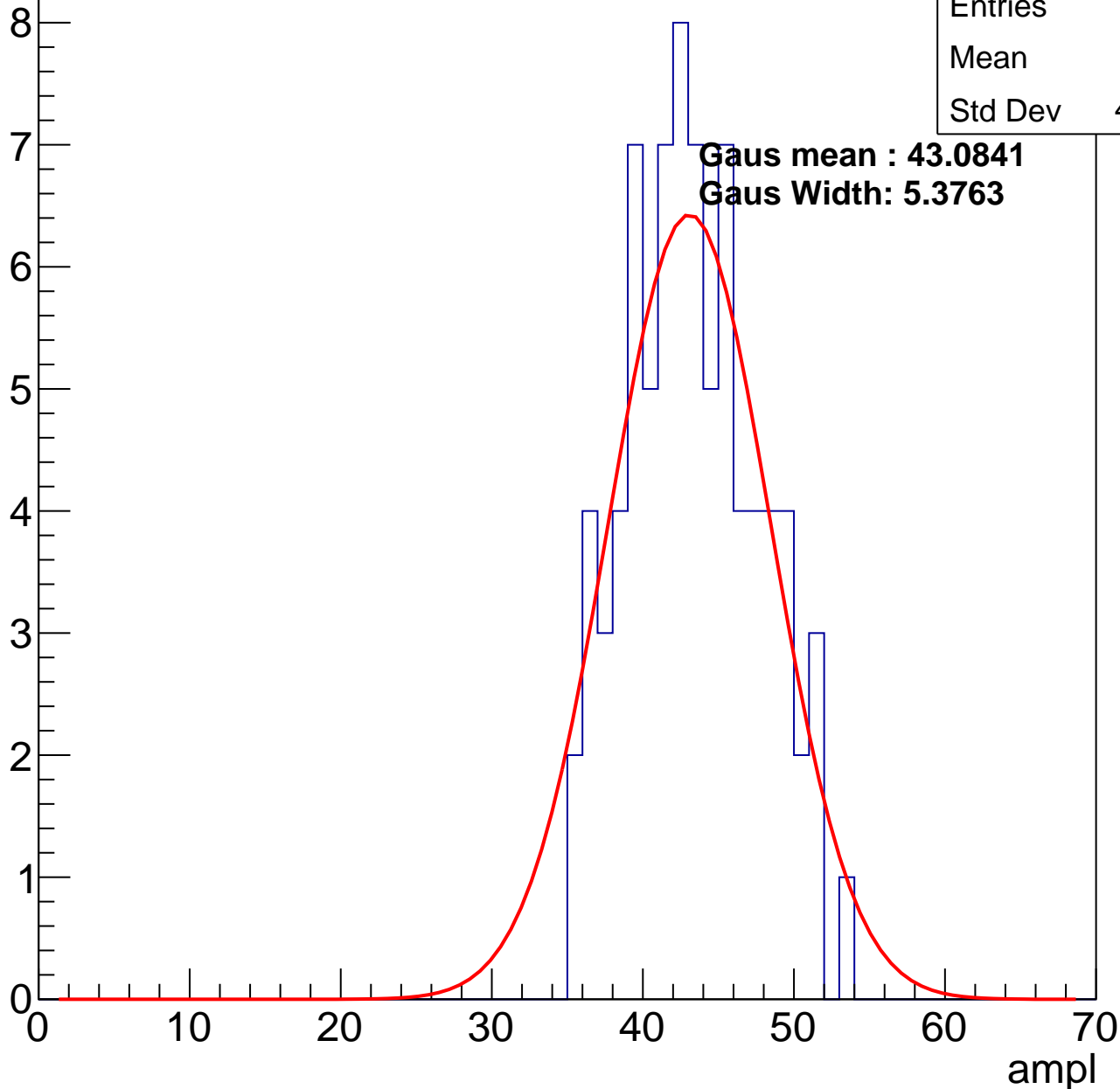
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	81
Mean	42.9
Std Dev	4.291

**Gaus mean : 43.0841**

**Gaus Width: 5.3763**

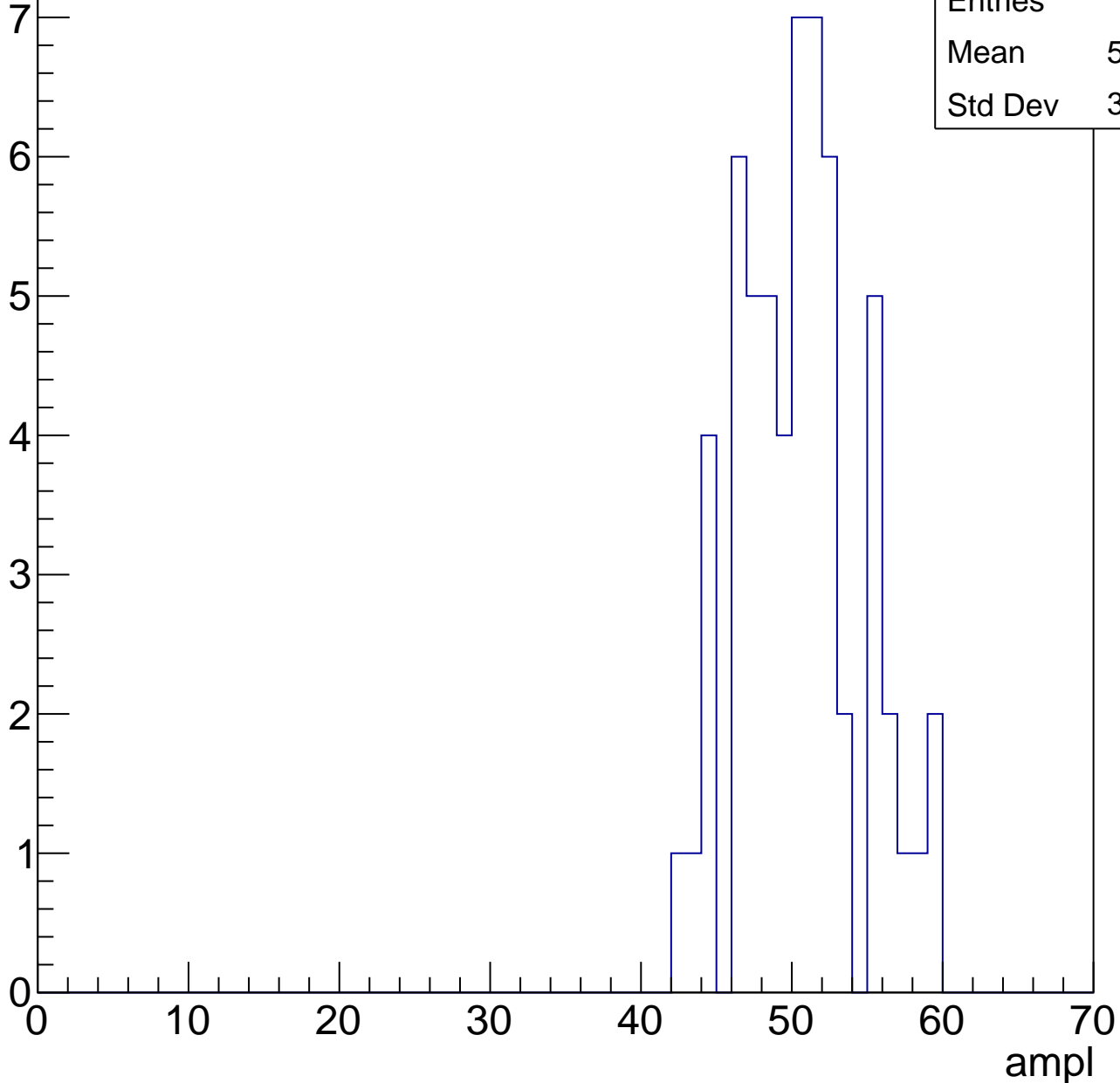


# B1L103S, U11-ch127, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	59
Mean	50.05
Std Dev	3.998

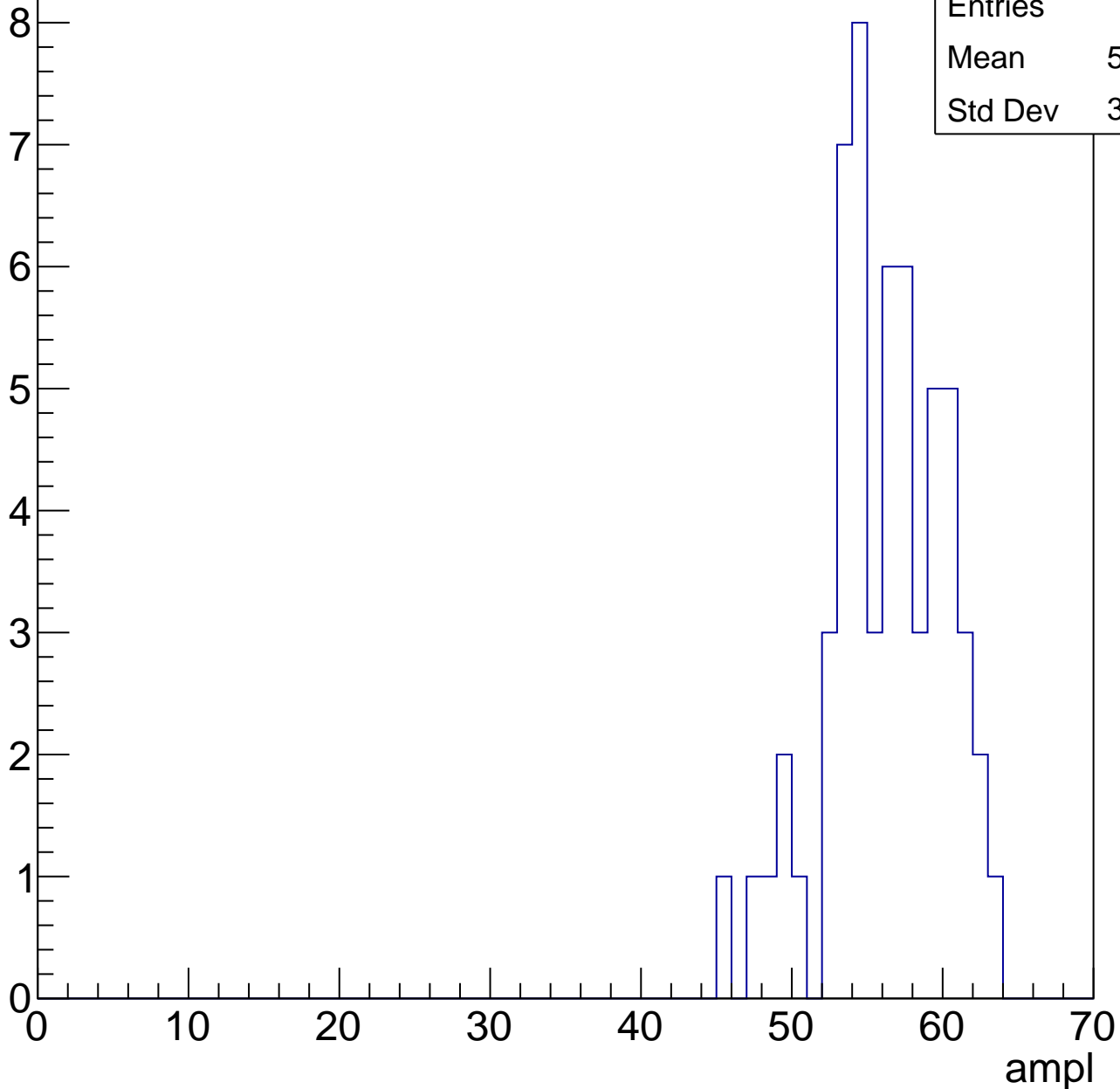


# B1L103S, U11-ch127, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	58
Mean	55.67
Std Dev	3.892

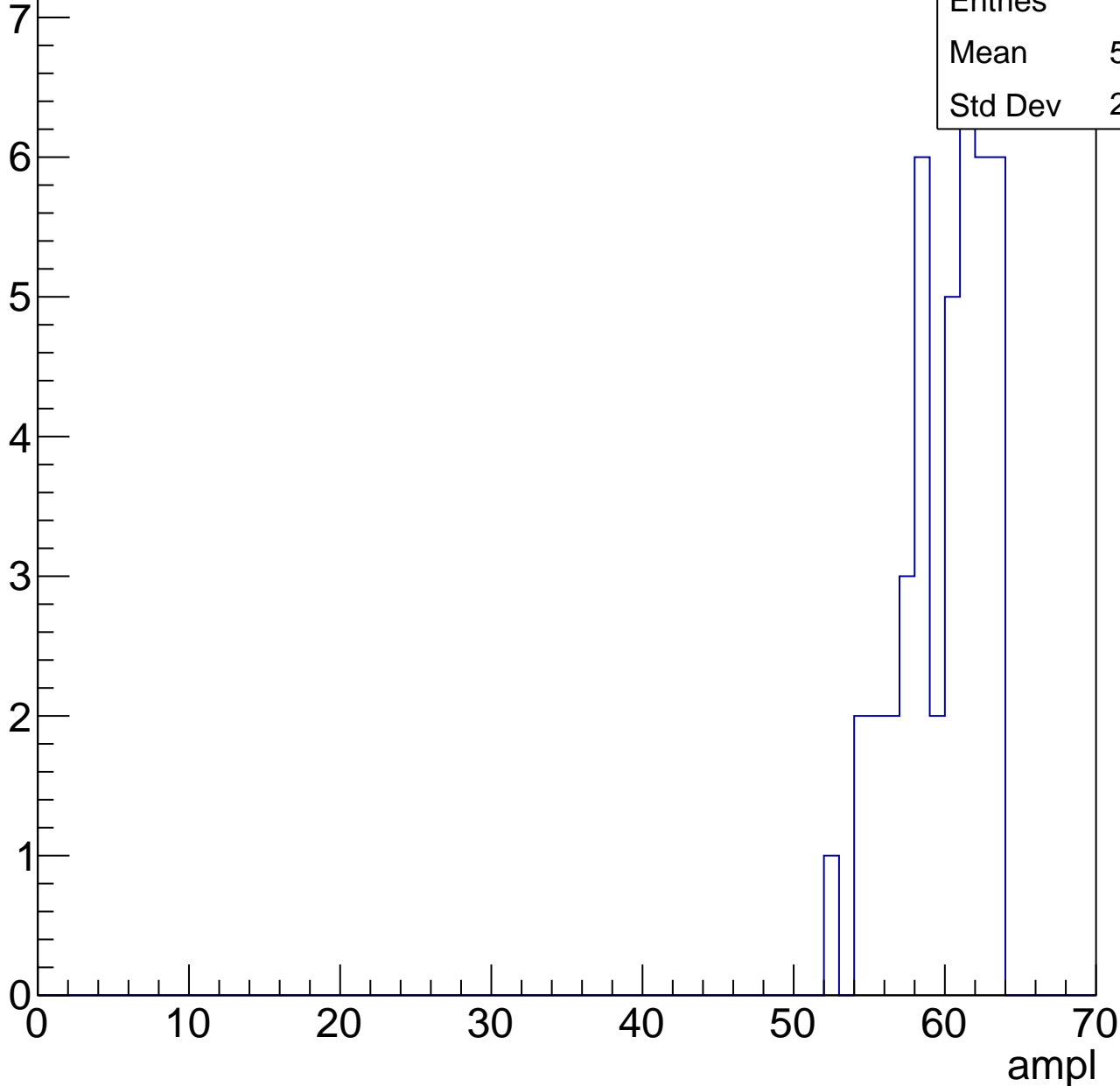


# B1L103S, U11-ch127, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	42
Mean	59.43
Std Dev	2.855



# B1L103S, U11-ch127, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U11-ch127, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

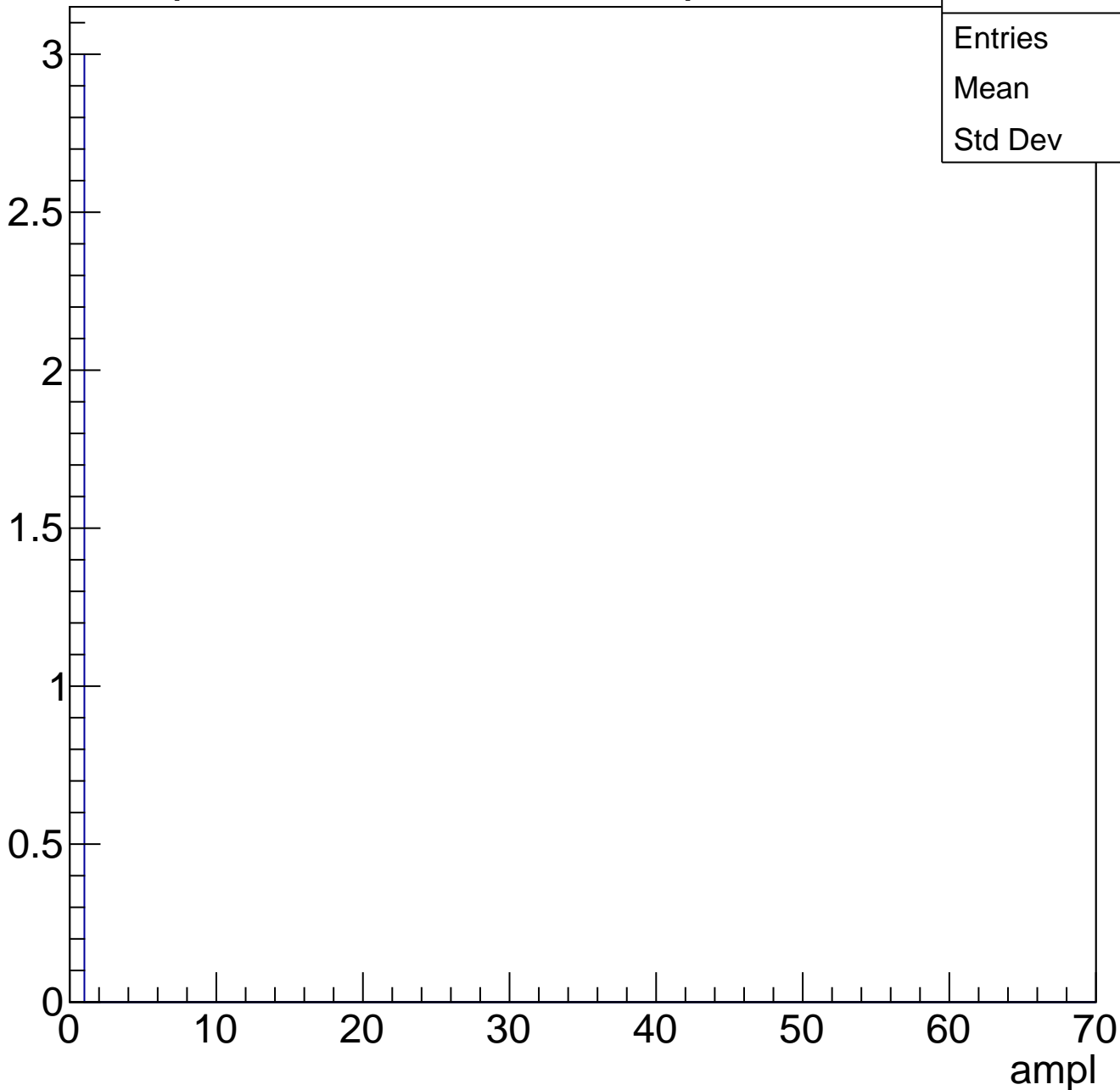
Entry



# B1L103S, U11-ch127, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	3
Mean	0
Std Dev	0