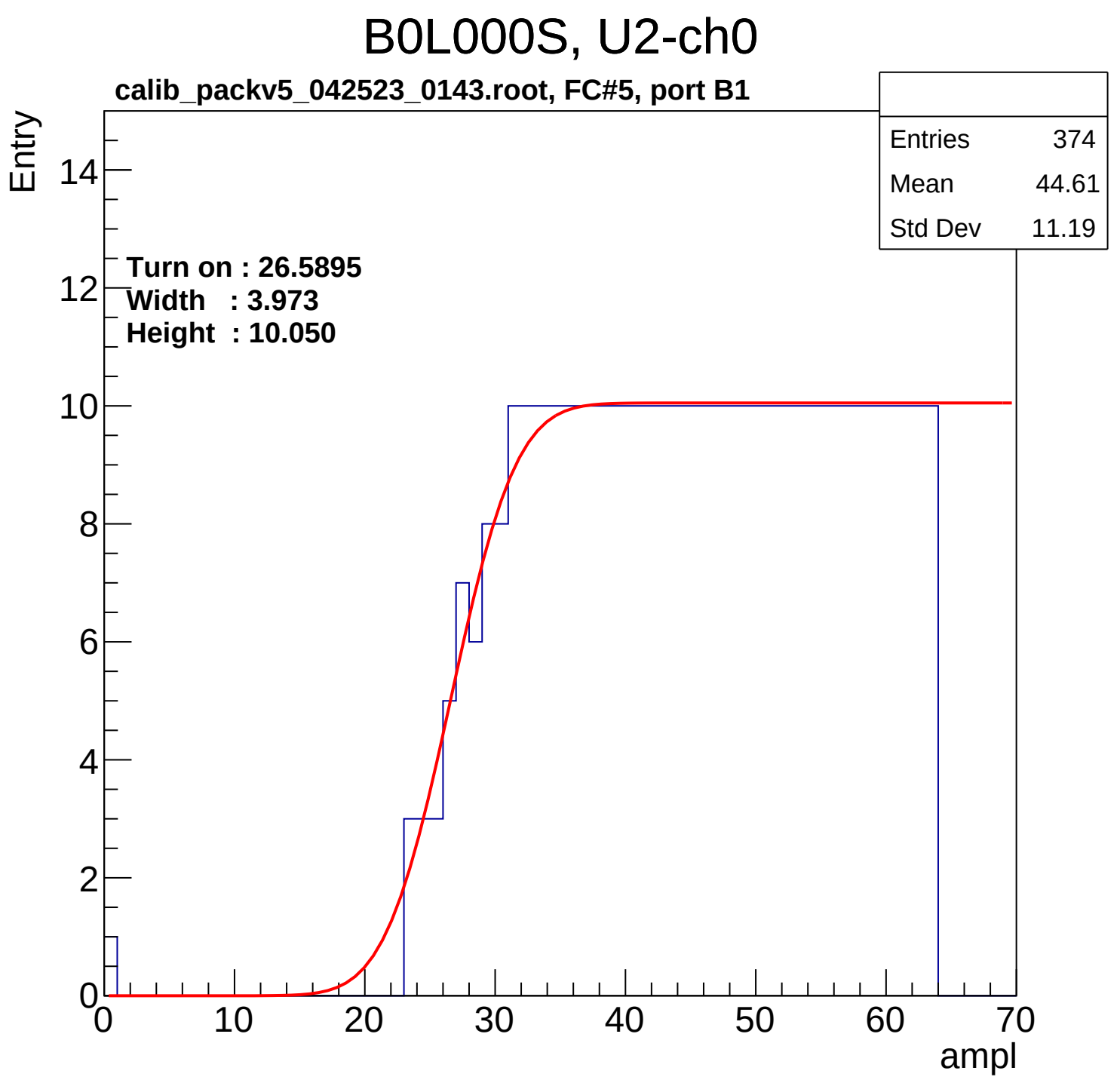
B0L000S, U2-ch0
calib_packv5_042523_0143.root, FC#5, port B1
Entries 374
Mean 44.61
Std Dev 11.19
Turn on : 26.5895
Width : 3.973
Height : 10.050
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ampl
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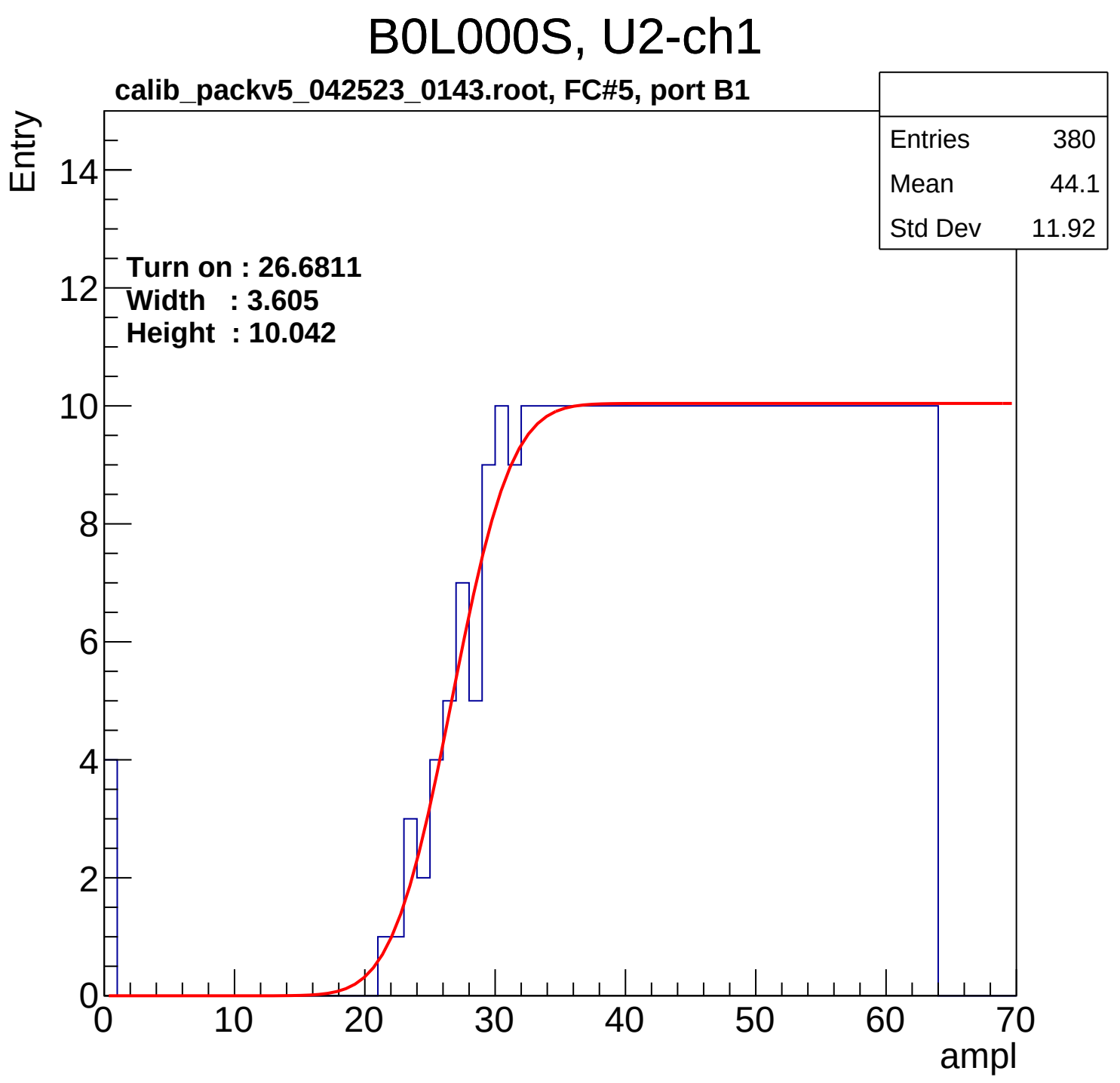
B0L000S, U2-ch1
calib_packv5_042523_0143.root, FC#5, port B1
Entries 380
Mean 44.1
Std Dev 11.92
Turn on : 26.6811
Width : 3.605
Height : 10.042
Entry
ampl
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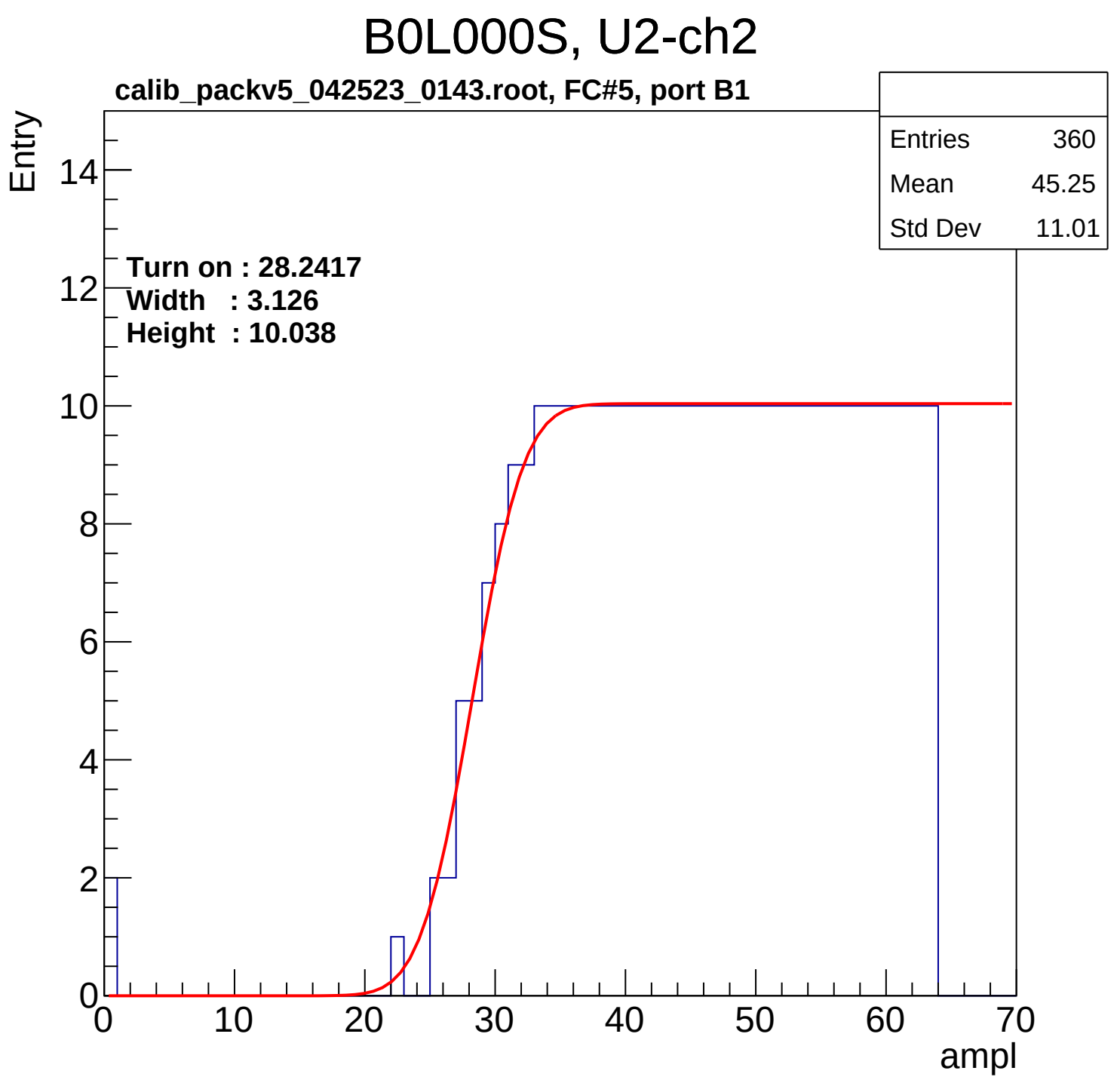
B0L000S, U2-ch2
calib_packv5_042523_0143.root, FC#5, port B1
Entries 360
Mean 45.25
Std Dev 11.01
Turn on : 28.2417
Width : 3.126
Height : 10.038
Entry
ampl
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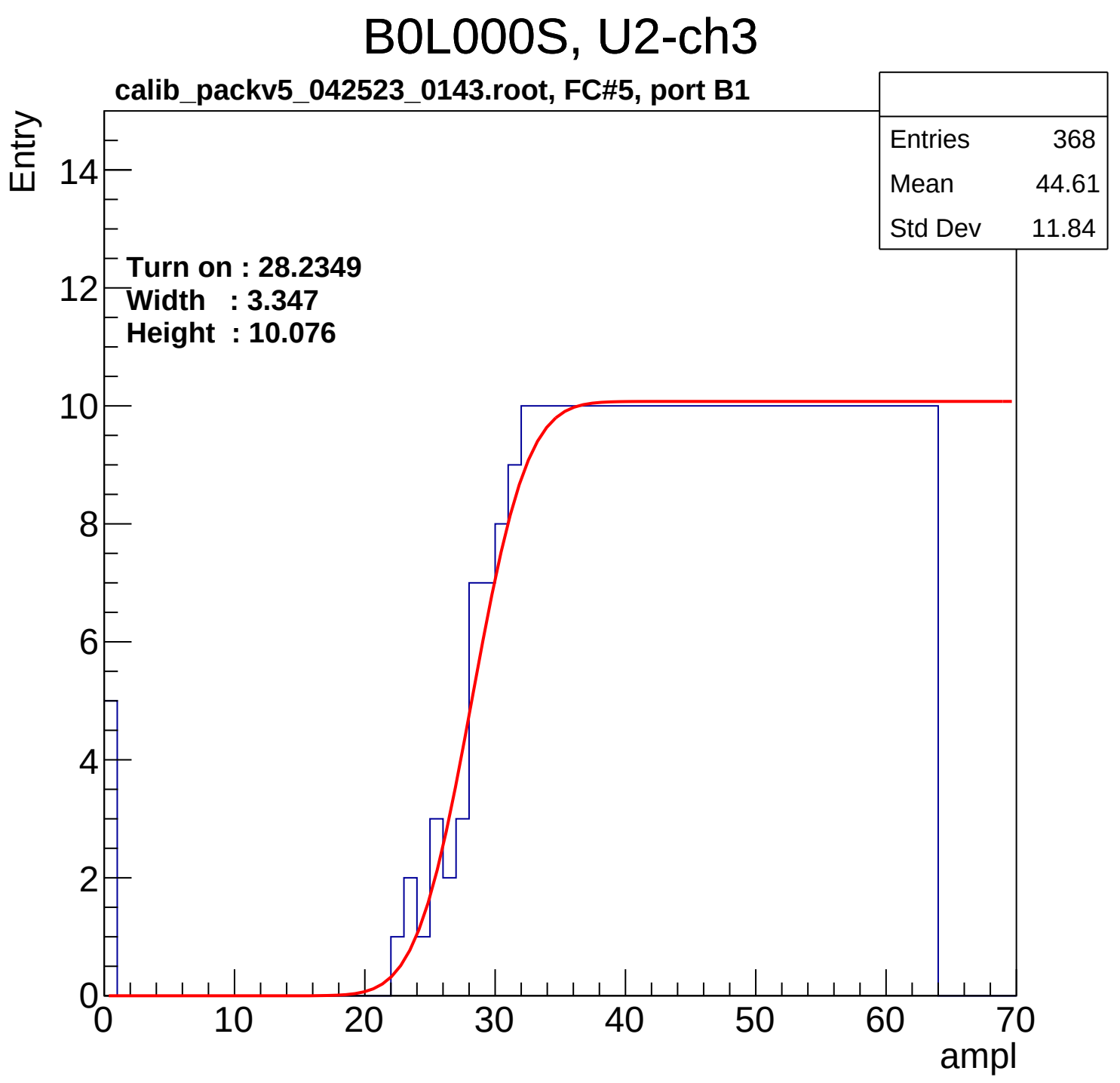
B0L000S, U2-ch3
calib_packv5_042523_0143.root, FC#5, port B1
Entries 368
Mean 44.61
Std Dev 11.84
Turn on : 28.2349
Width : 3.347
Height : 10.076
Entry
ampl
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2
4
6
8
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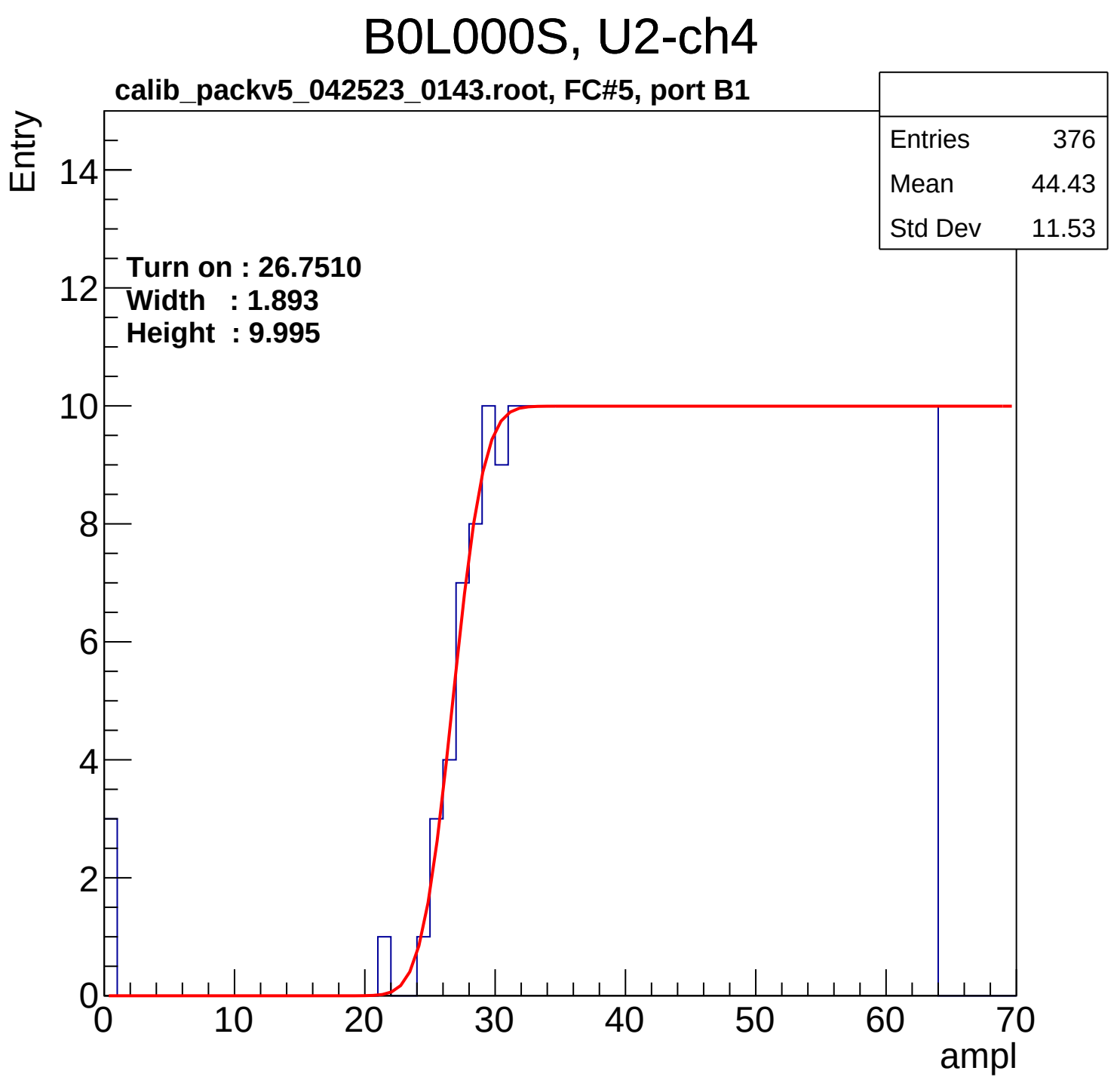
B0L000S, U2-ch4
calib_packv5_042523_0143.root, FC#5, port B1
Entries 376
Mean 44.43
Std Dev 11.53
Turn on : 26.7510
Width : 1.893
Height : 9.995
Entry
ampl
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2
4
6
8
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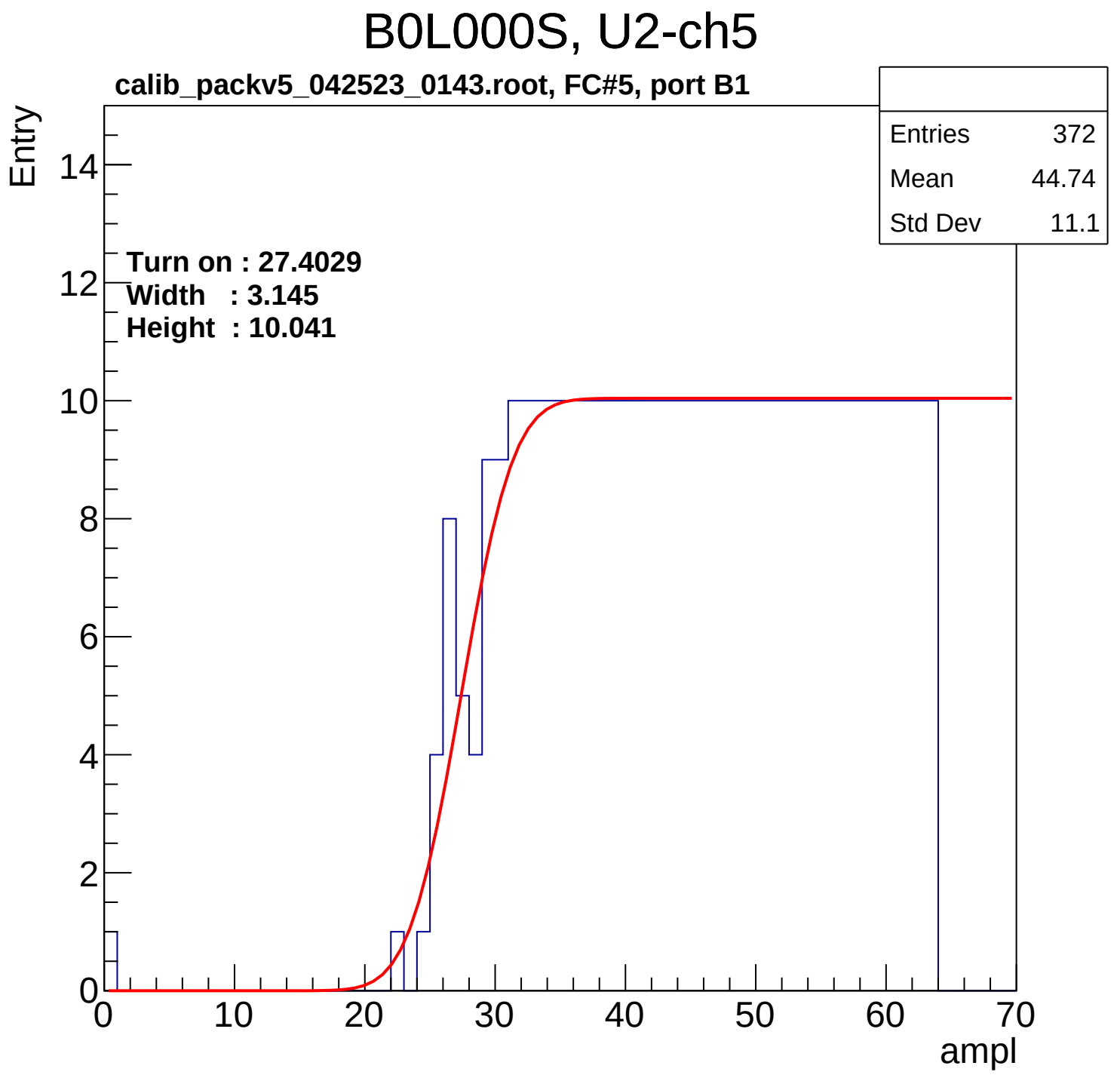
B0L000S, U2-ch5
calib_packv5_042523_0143.root, FC#5, port B1
Entries 372
Mean 44.74
Std Dev 11.1
Turn on : 27.4029
Width : 3.145
Height : 10.041
Entry
ampl
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2
4
6
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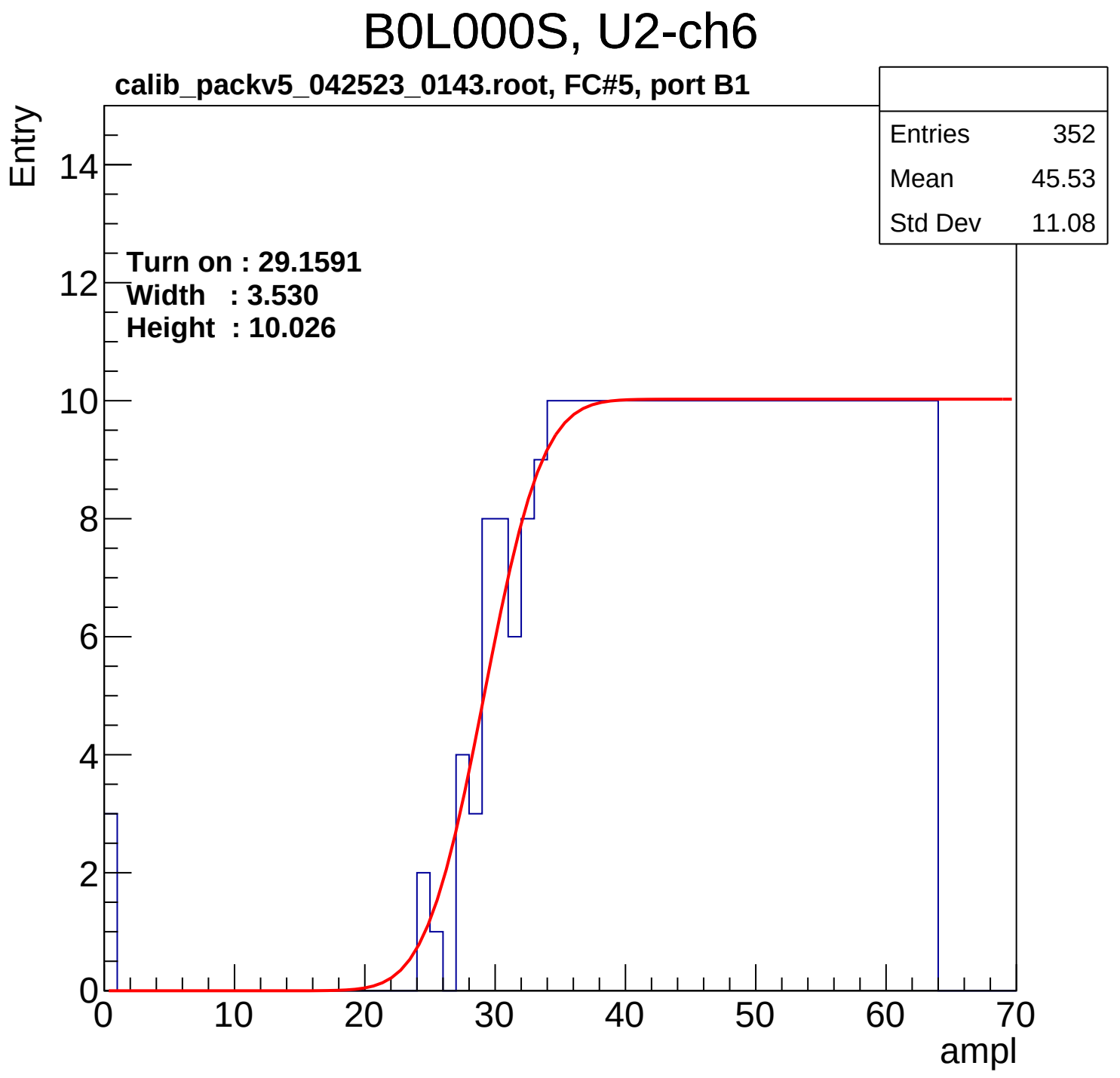
B0L000S, U2-ch6
calib_packv5_042523_0143.root, FC#5, port B1
Entries 352
Mean 45.53
Std Dev 11.08
Turn on : 29.1591
Width : 3.530
Height : 10.026
Entry
ampl
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4
6
8
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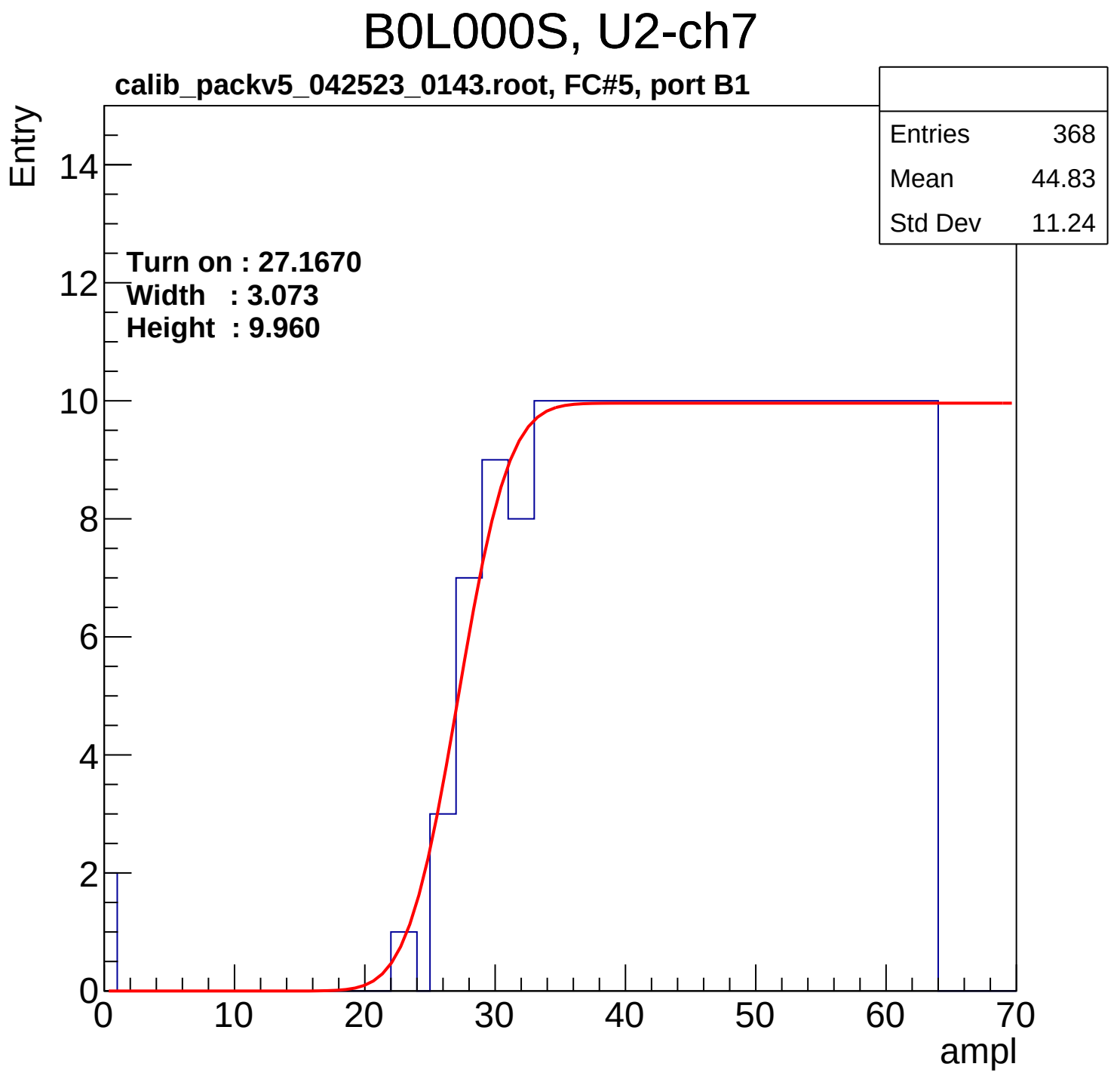
B0L000S, U2-ch7
calib_packv5_042523_0143.root, FC#5, port B1
Entries 368
Mean 44.83
Std Dev 11.24
Turn on : 27.1670
Width : 3.073
Height : 9.960
Entry
ampl
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2
4
6
8
10
12
14
0
10
20
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60
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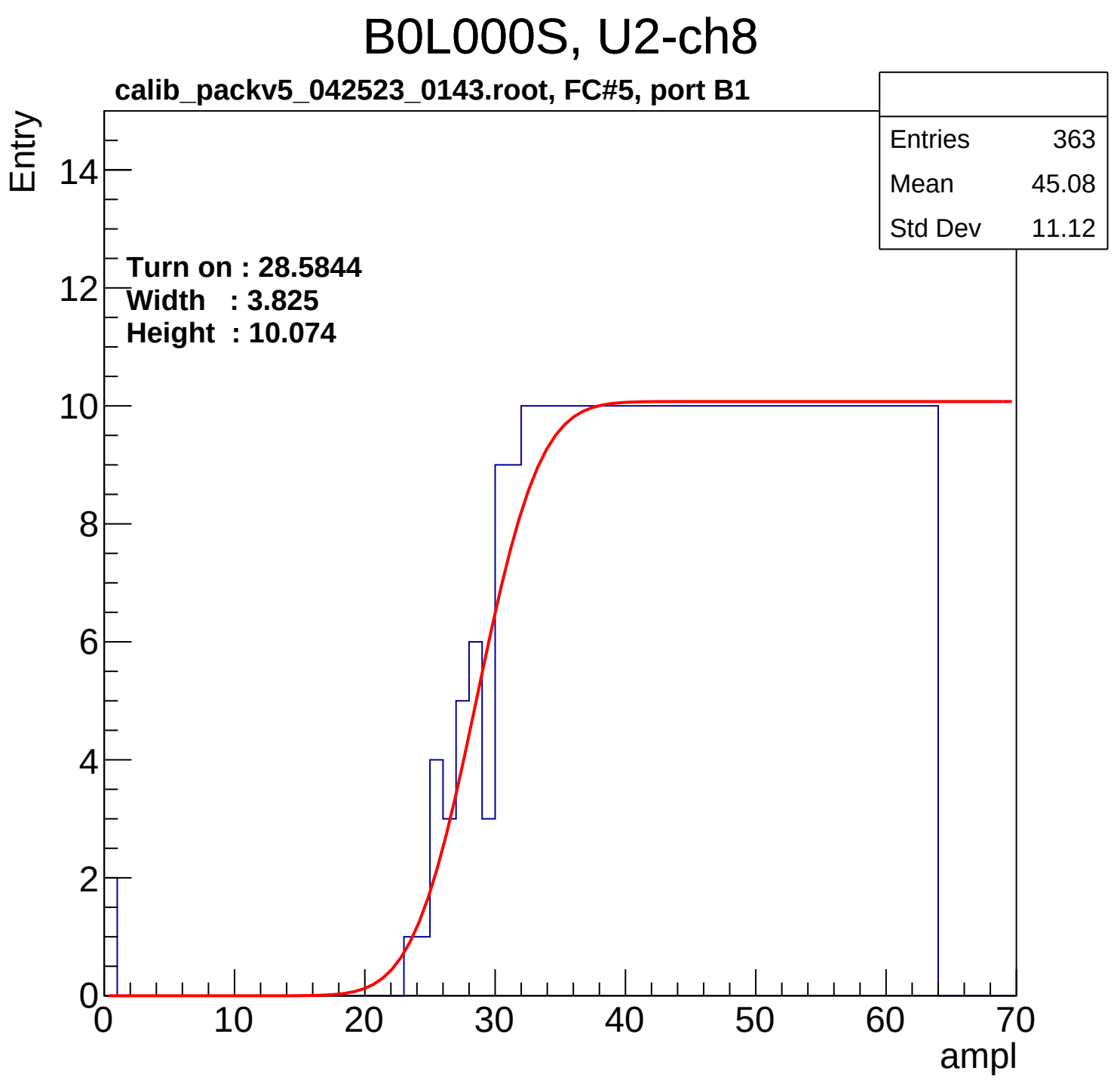
B0L000S, U2-ch8
calib_packv5_042523_0143.root, FC#5, port B1
Entries 363
Mean 45.08
Std Dev 11.12
Turn on : 28.5844
Width : 3.825
Height : 10.074
Entry
ampl
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4
6
8
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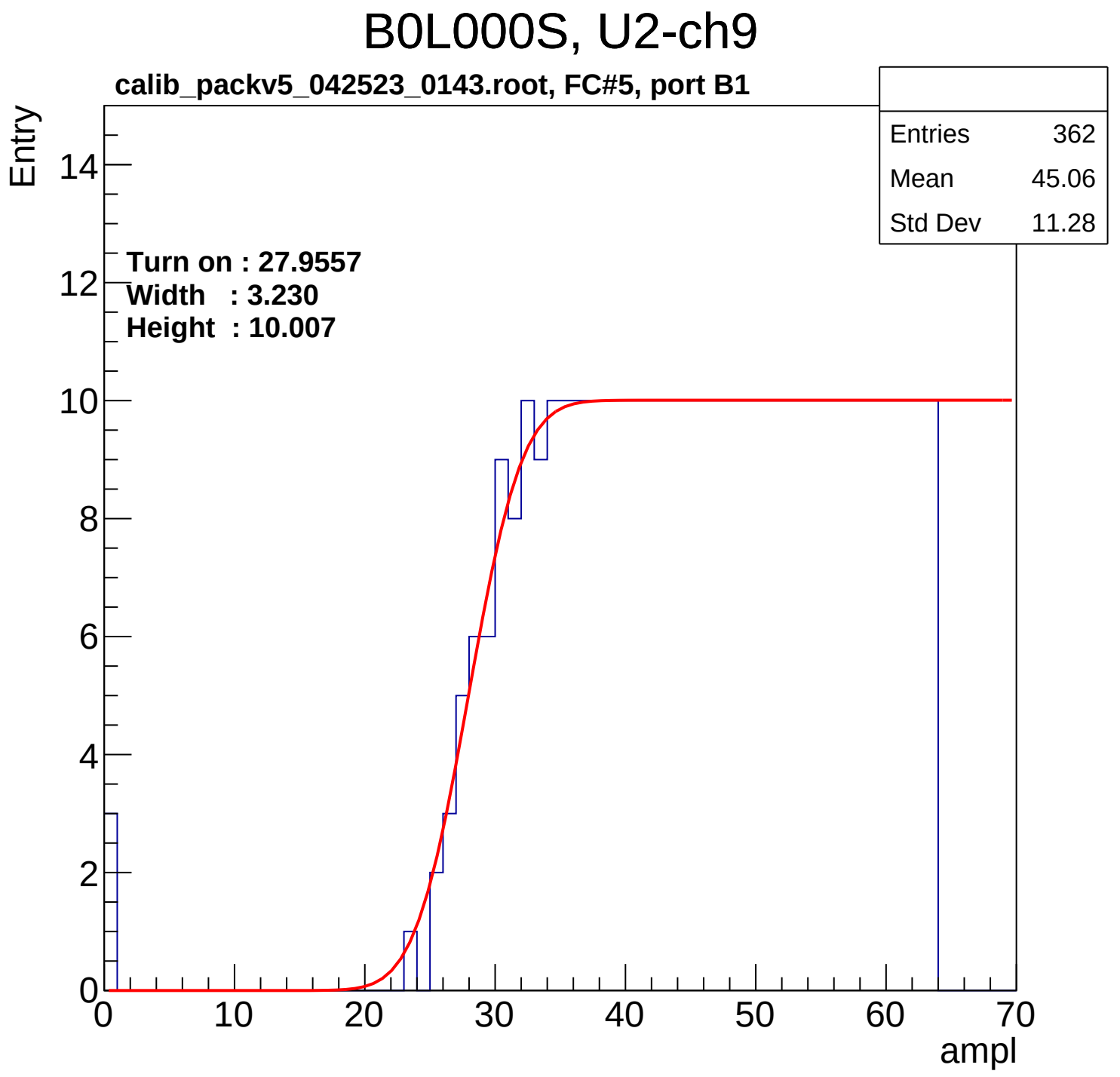
B0L000S, U2-ch9
calib_packv5_042523_0143.root, FC#5, port B1
Entries 362
Mean 45.06
Std Dev 11.28
Turn on : 27.9557
Width : 3.230
Height : 10.007
Entry
ampl
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2
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6
8
10
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0
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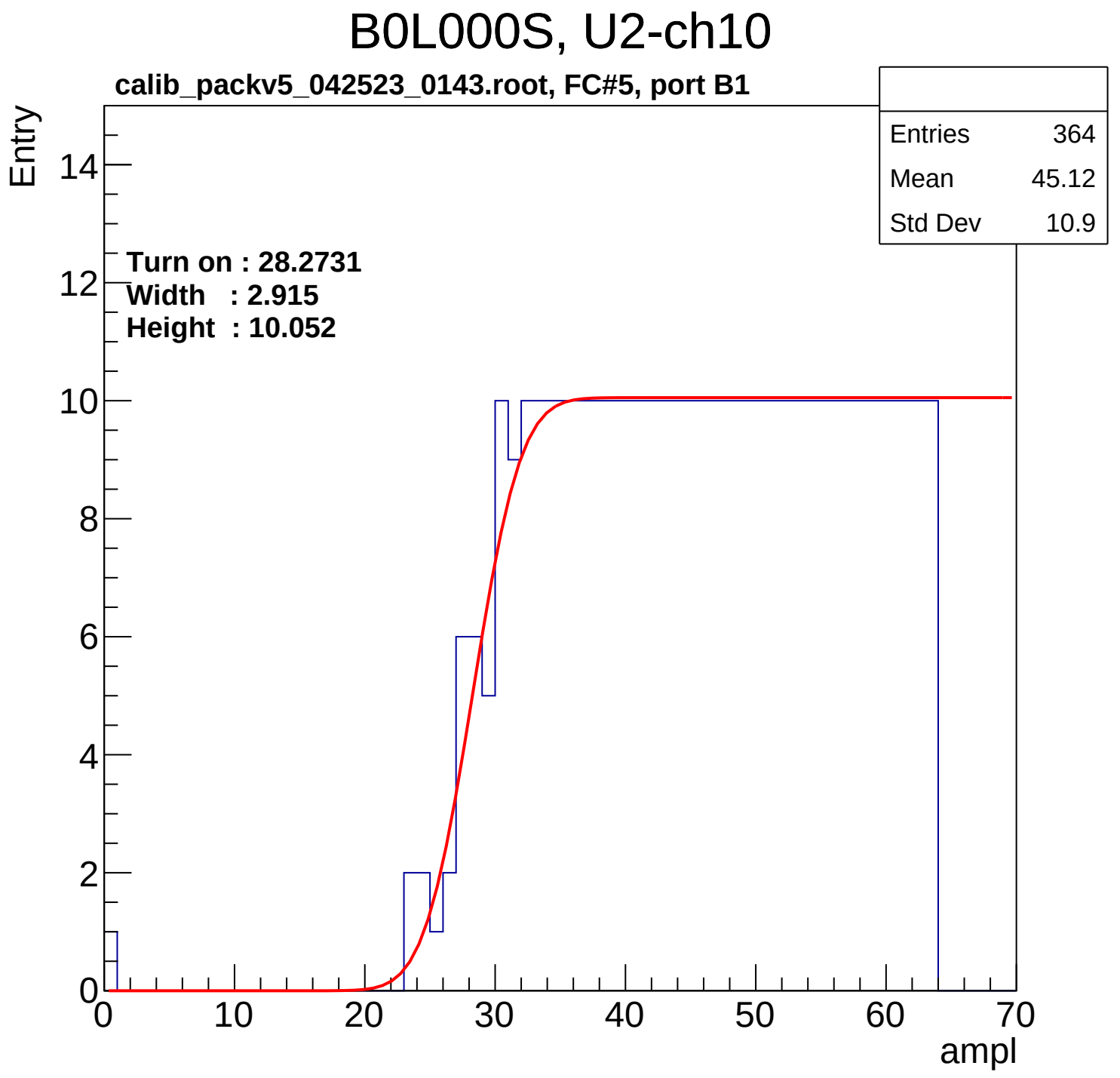
B0L000S, U2-ch10
calib_packv5_042523_0143.root, FC#5, port B1
Entries 364
Mean 45.12
Std Dev 10.9
Turn on : 28.2731
Width : 2.915
Height : 10.052
Entry
ampl
0
2
4
6
8
10
12
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0
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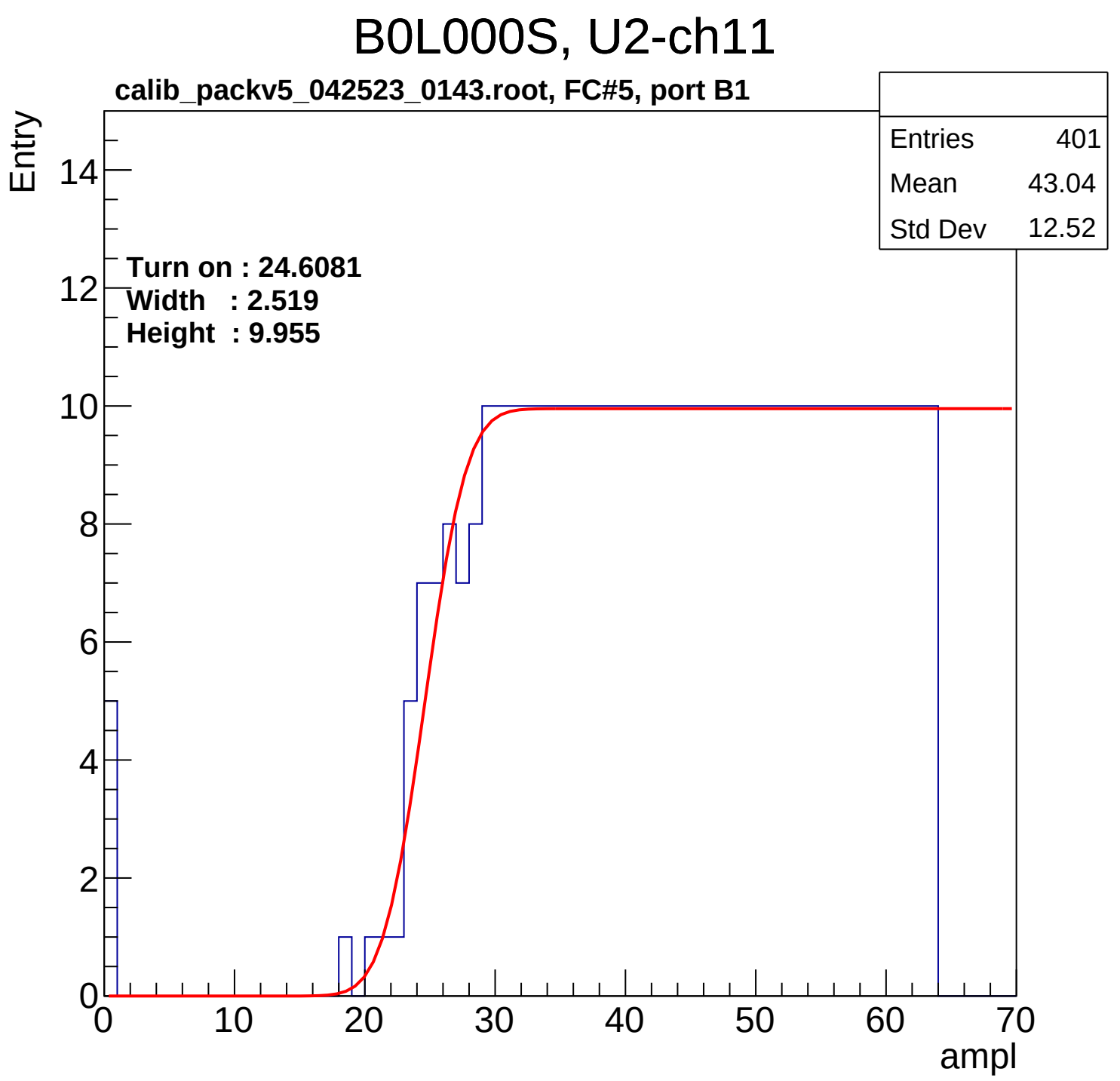
B0L000S, U2-ch11
calib_packv5_042523_0143.root, FC#5, port B1
Entries 401
Mean 43.04
Std Dev 12.52
Turn on : 24.6081
Width : 2.519
Height : 9.955
Entry
ampl
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2
4
6
8
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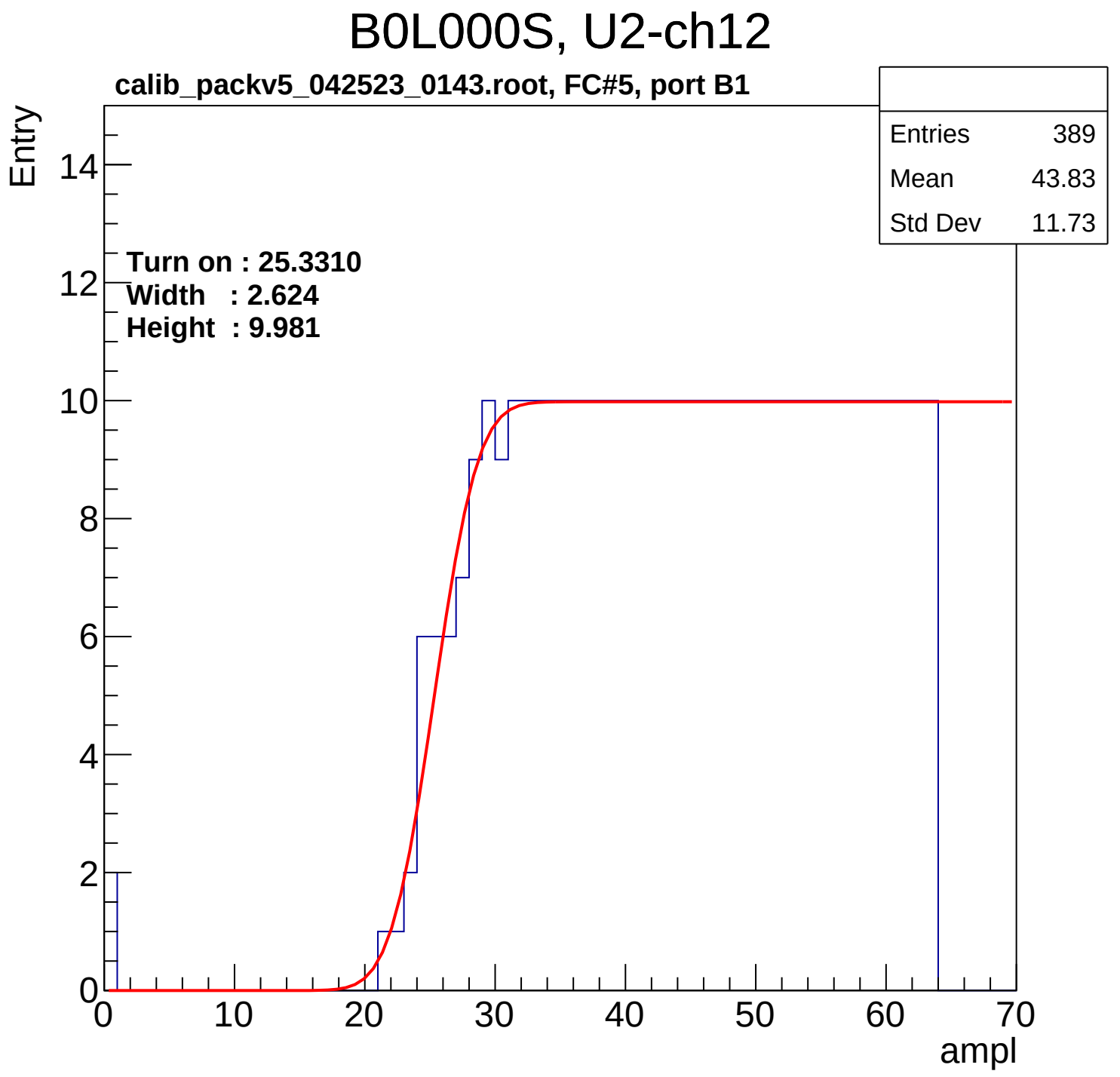
B0L000S, U2-ch12
calib_packv5_042523_0143.root, FC#5, port B1
Entries 389
Mean 43.83
Std Dev 11.73
Turn on : 25.3310
Width : 2.624
Height : 9.981
Entry
ampl
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2
4
6
8
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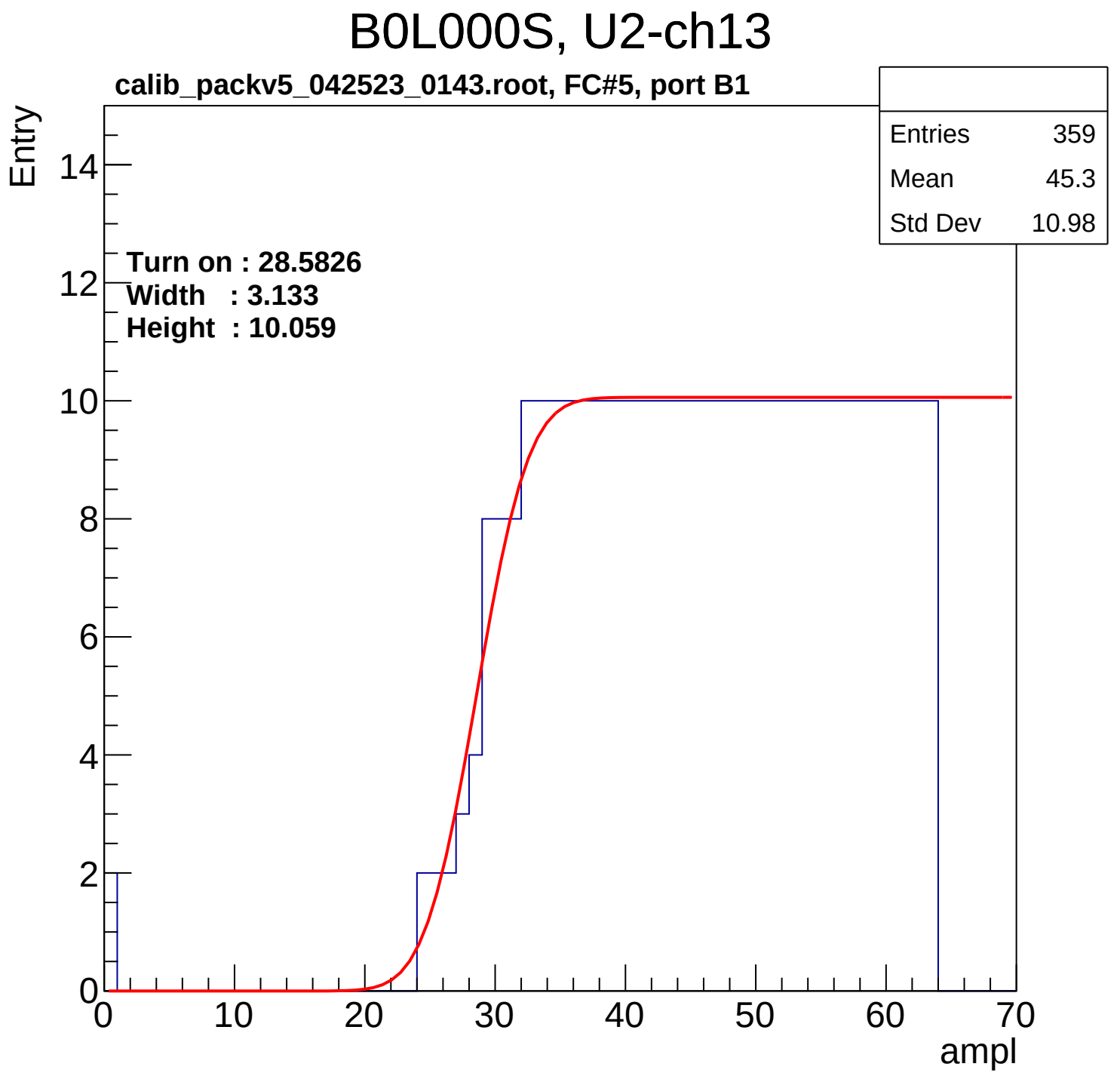
B0L000S, U2-ch13
calib_packv5_042523_0143.root, FC#5, port B1
Entries 359
Mean 45.3
Std Dev 10.98
Turn on : 28.5826
Width : 3.133
Height : 10.059
Entry
ampl
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4
6
8
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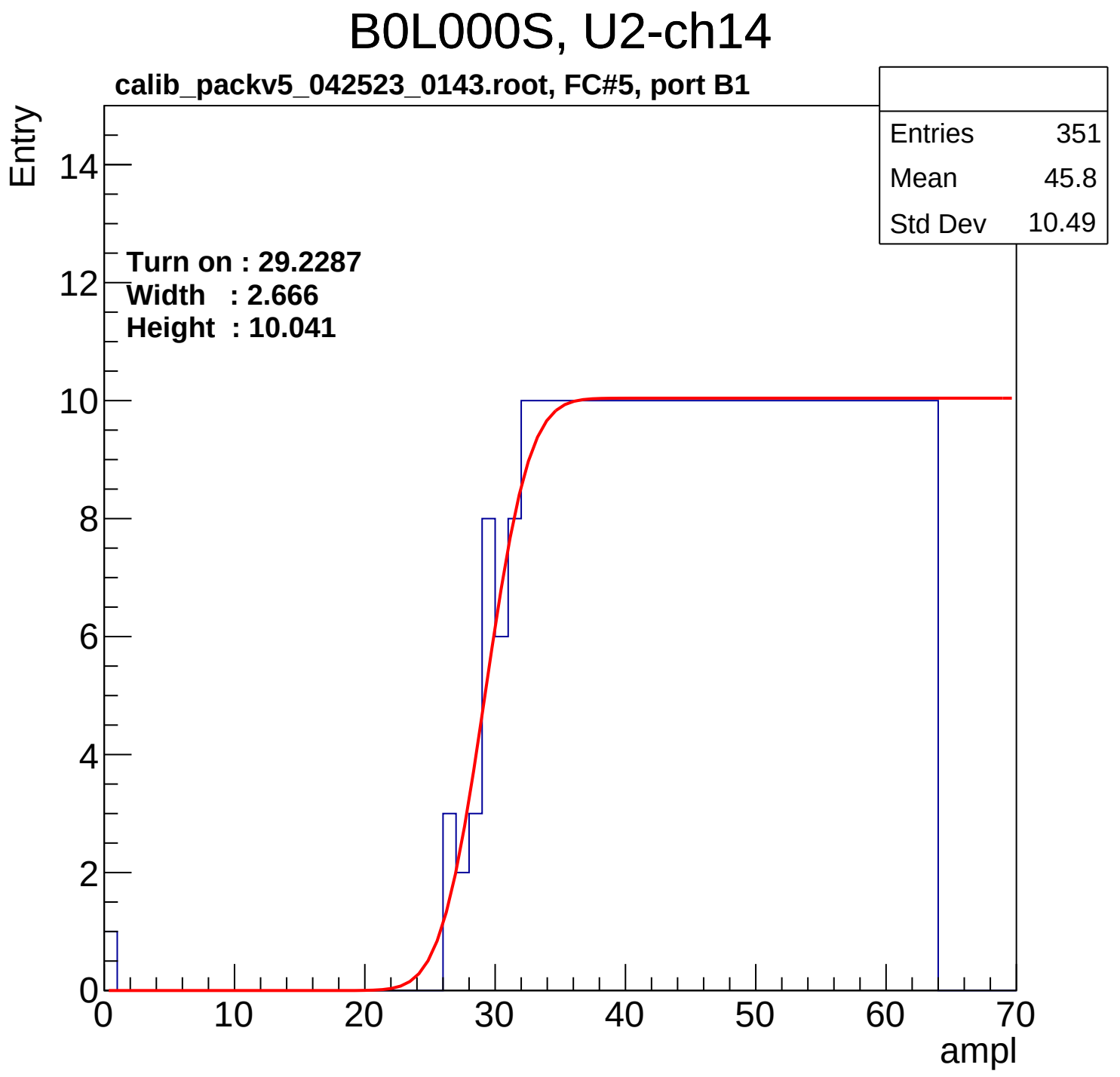
B0L000S, U2-ch14
calib_packv5_042523_0143.root, FC#5, port B1
Entries 351
Mean 45.8
Std Dev 10.49
Turn on : 29.2287
Width : 2.666
Height : 10.041
Entry
ampl
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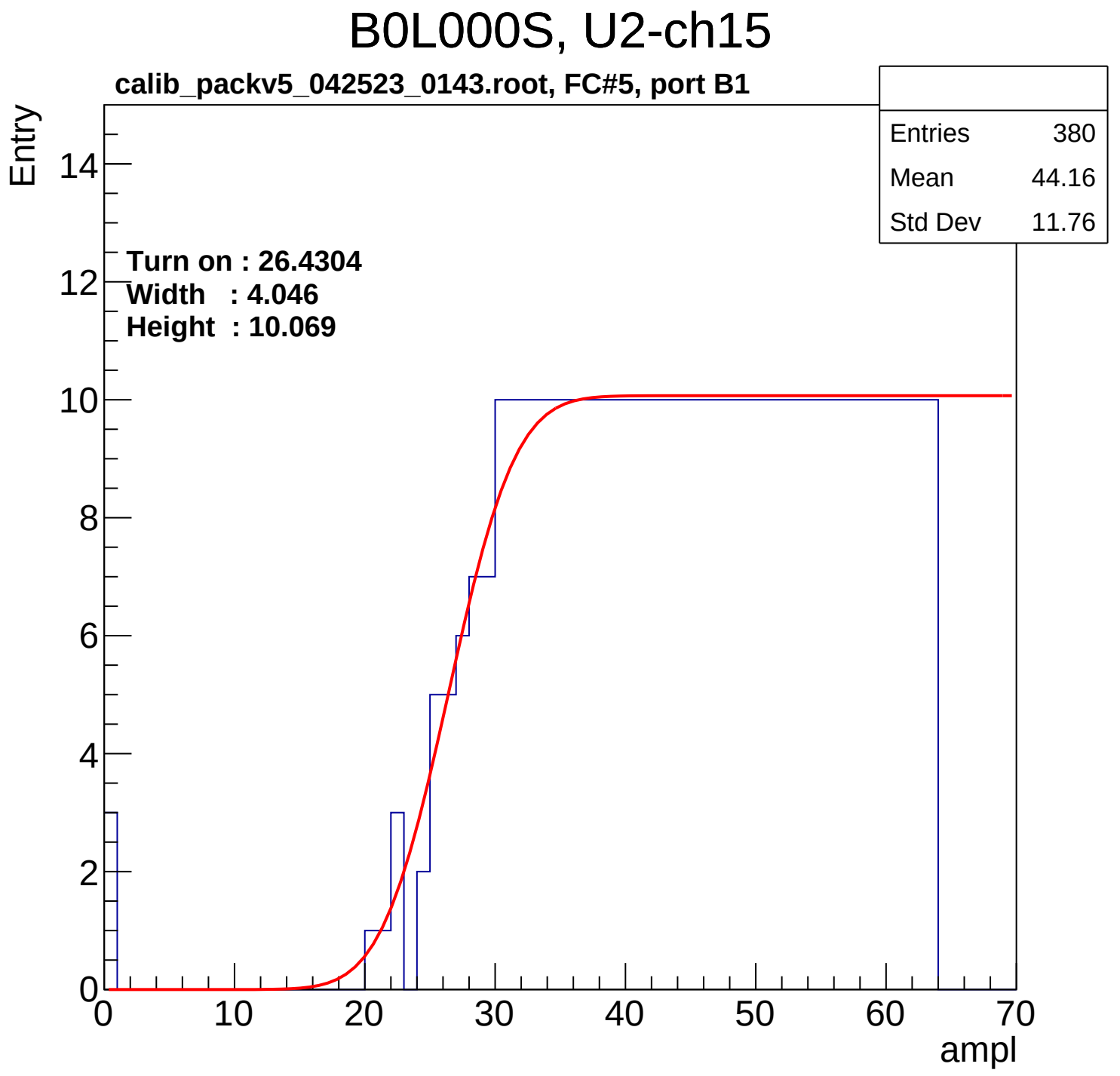
B0L000S, U2-ch15
calib_packv5_042523_0143.root, FC#5, port B1
Entries 380
Mean 44.16
Std Dev 11.76
Turn on : 26.4304
Width : 4.046
Height : 10.069
Entry
ampl
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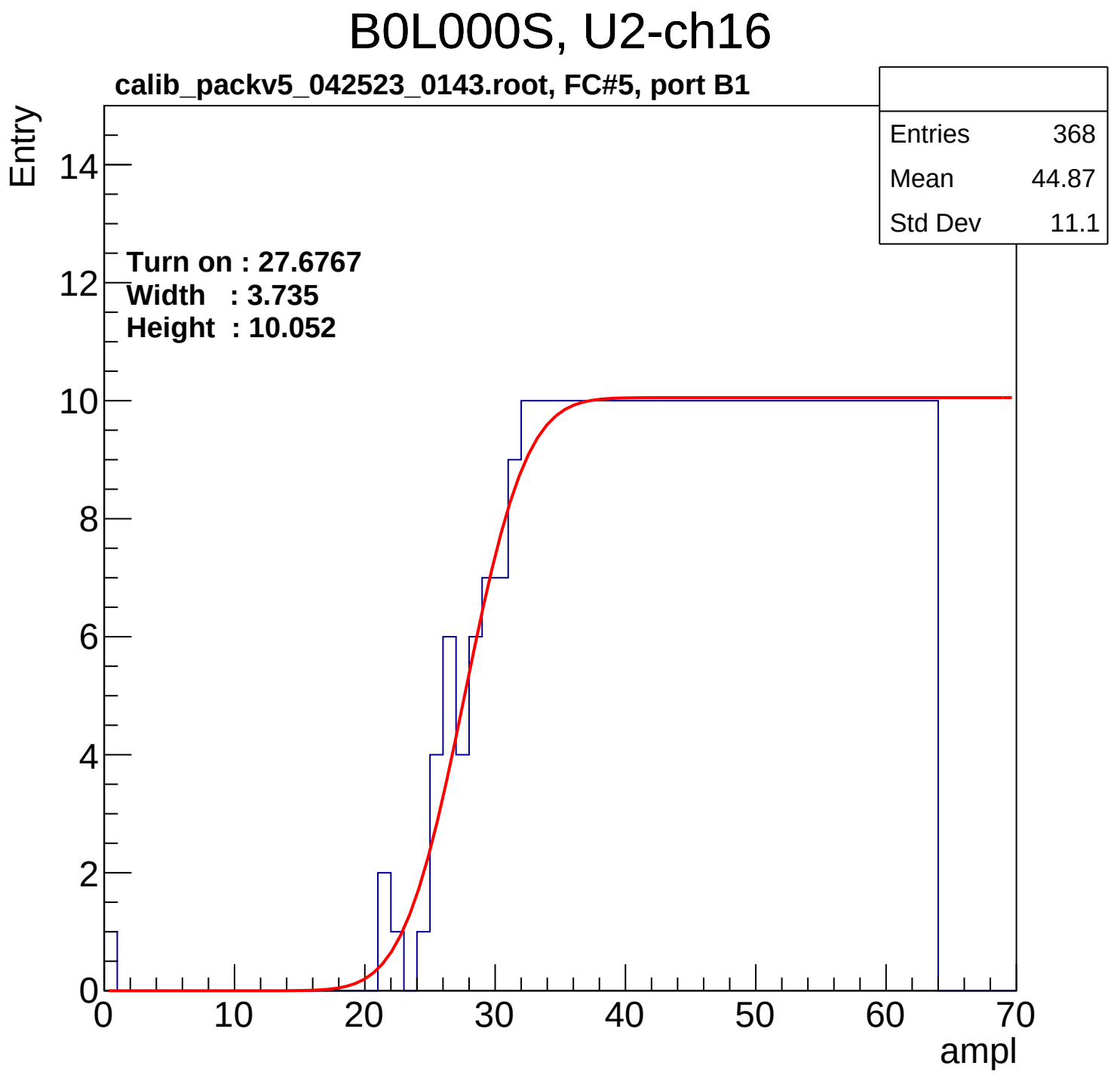
B0L000S, U2-ch16
calib_packv5_042523_0143.root, FC#5, port B1
Entries 368
Mean 44.87
Std Dev 11.1
Turn on : 27.6767
Width : 3.735
Height : 10.052
Entry
ampl
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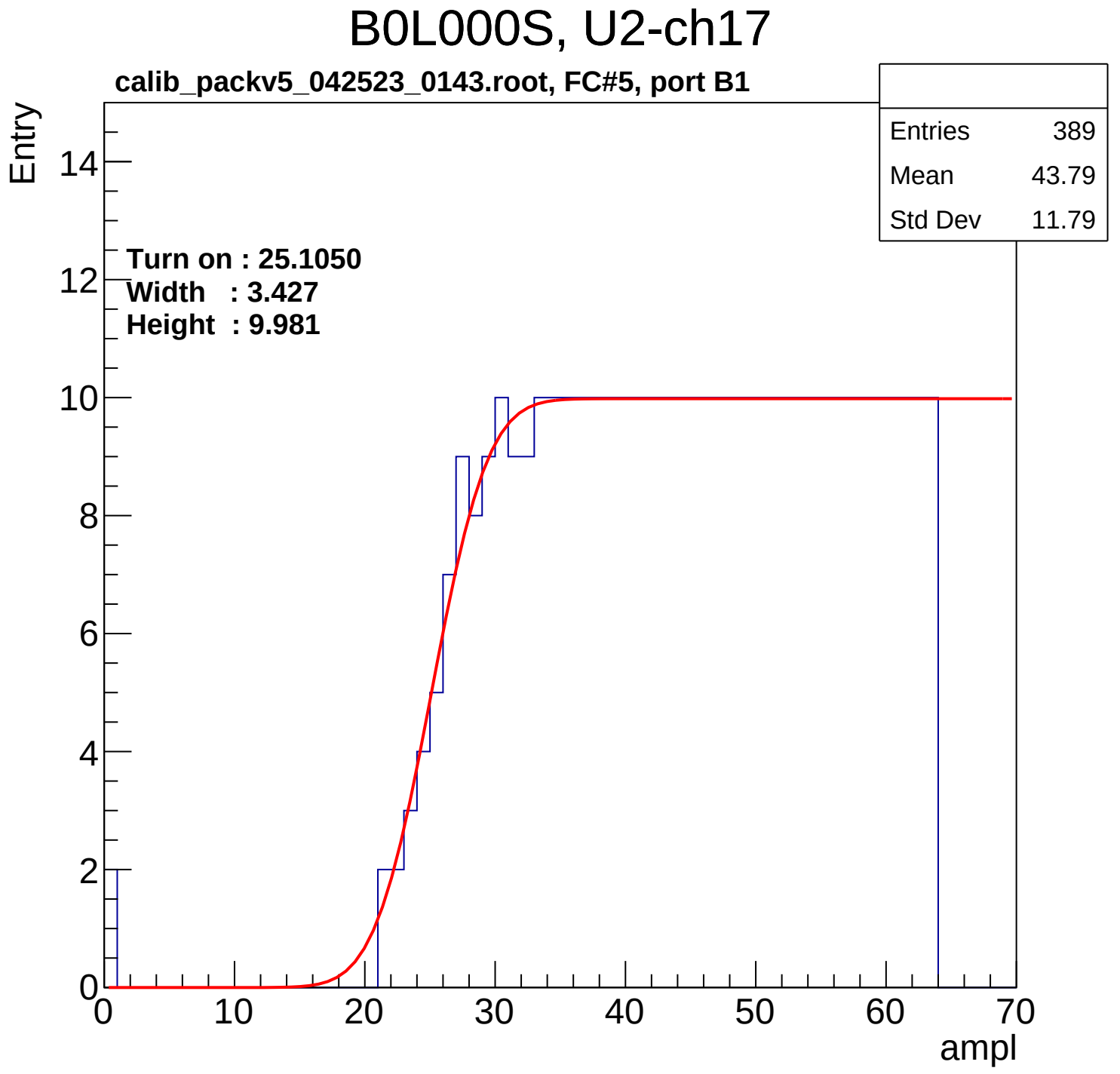
B0L000S, U2-ch17
calib_packv5_042523_0143.root, FC#5, port B1
Entries 389
Mean 43.79
Std Dev 11.79
Turn on : 25.1050
Width : 3.427
Height : 9.981
Entry
ampl
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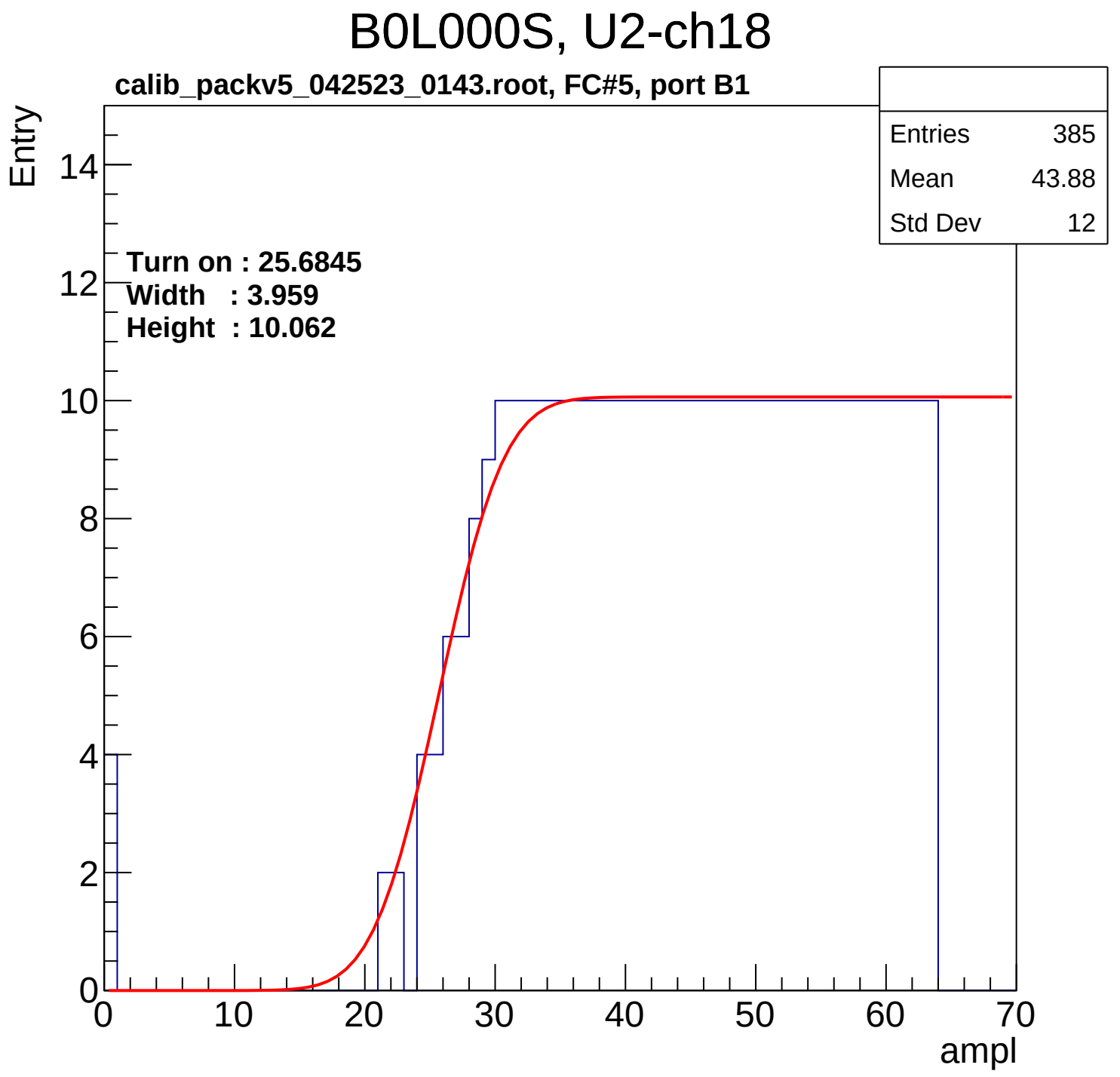
B0L000S, U2-ch18
calib_packv5_042523_0143.root, FC#5, port B1
Entries 385
Mean 43.88
Std Dev 12
Turn on : 25.6845
Width : 3.959
Height : 10.062
Entry
ampl
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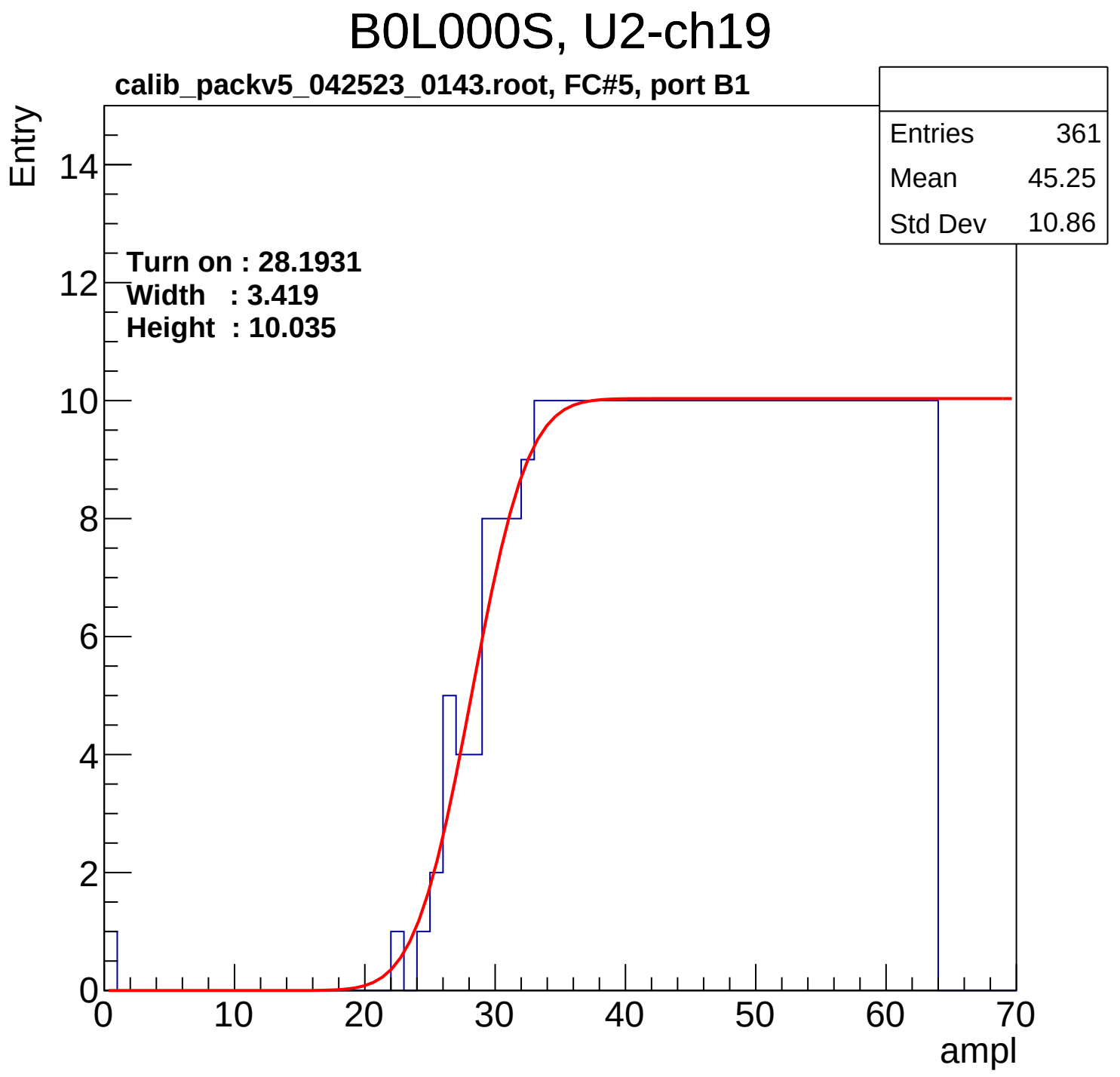
B0L000S, U2-ch19
calib_packv5_042523_0143.root, FC#5, port B1
Entries 361
Mean 45.25
Std Dev 10.86
Turn on : 28.1931
Width : 3.419
Height : 10.035
Entry
ampl
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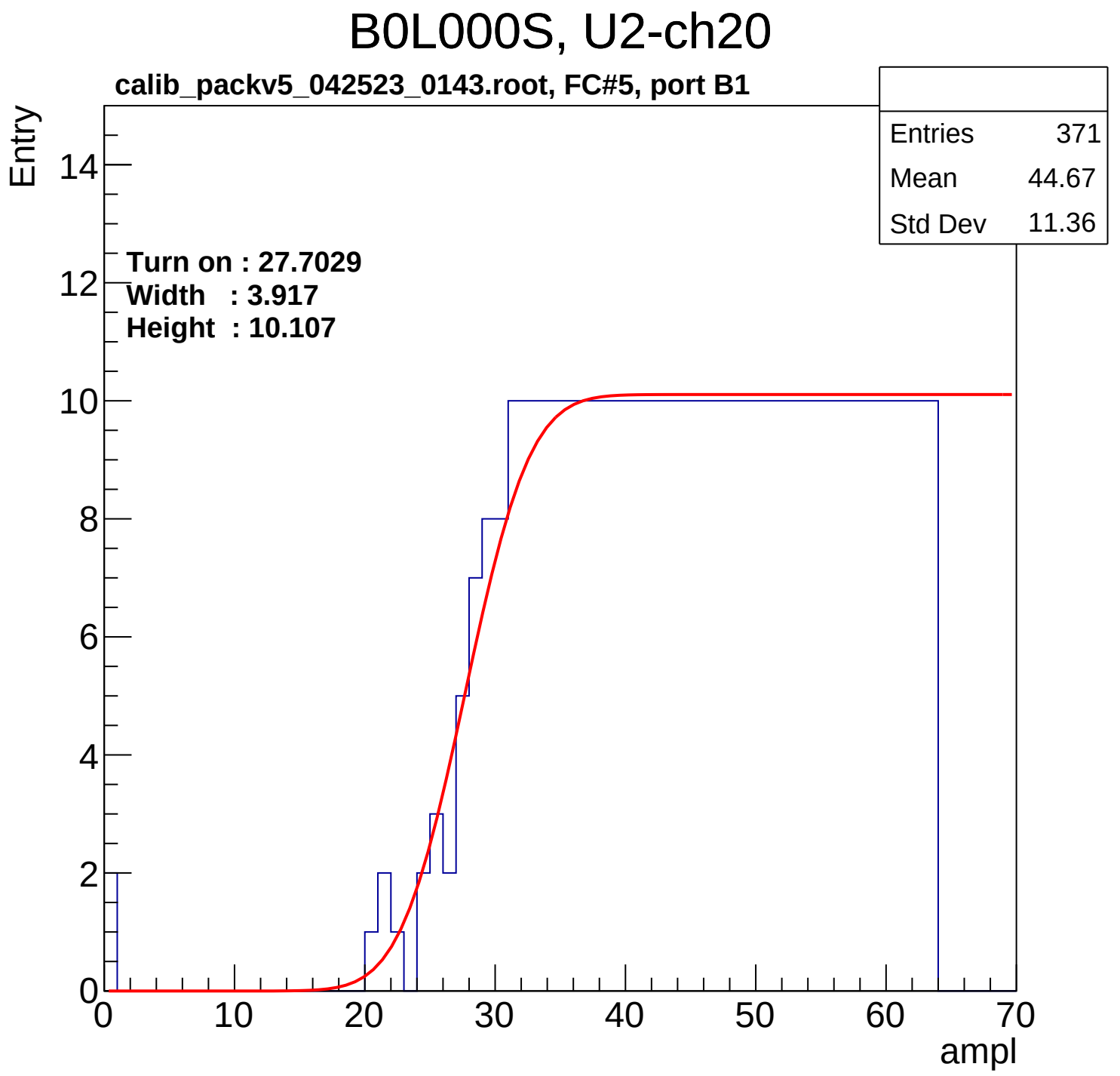
B0L000S, U2-ch20
calib_packv5_042523_0143.root, FC#5, port B1
Entries 371
Mean 44.67
Std Dev 11.36
Turn on : 27.7029
Width : 3.917
Height : 10.107
Entry
ampl
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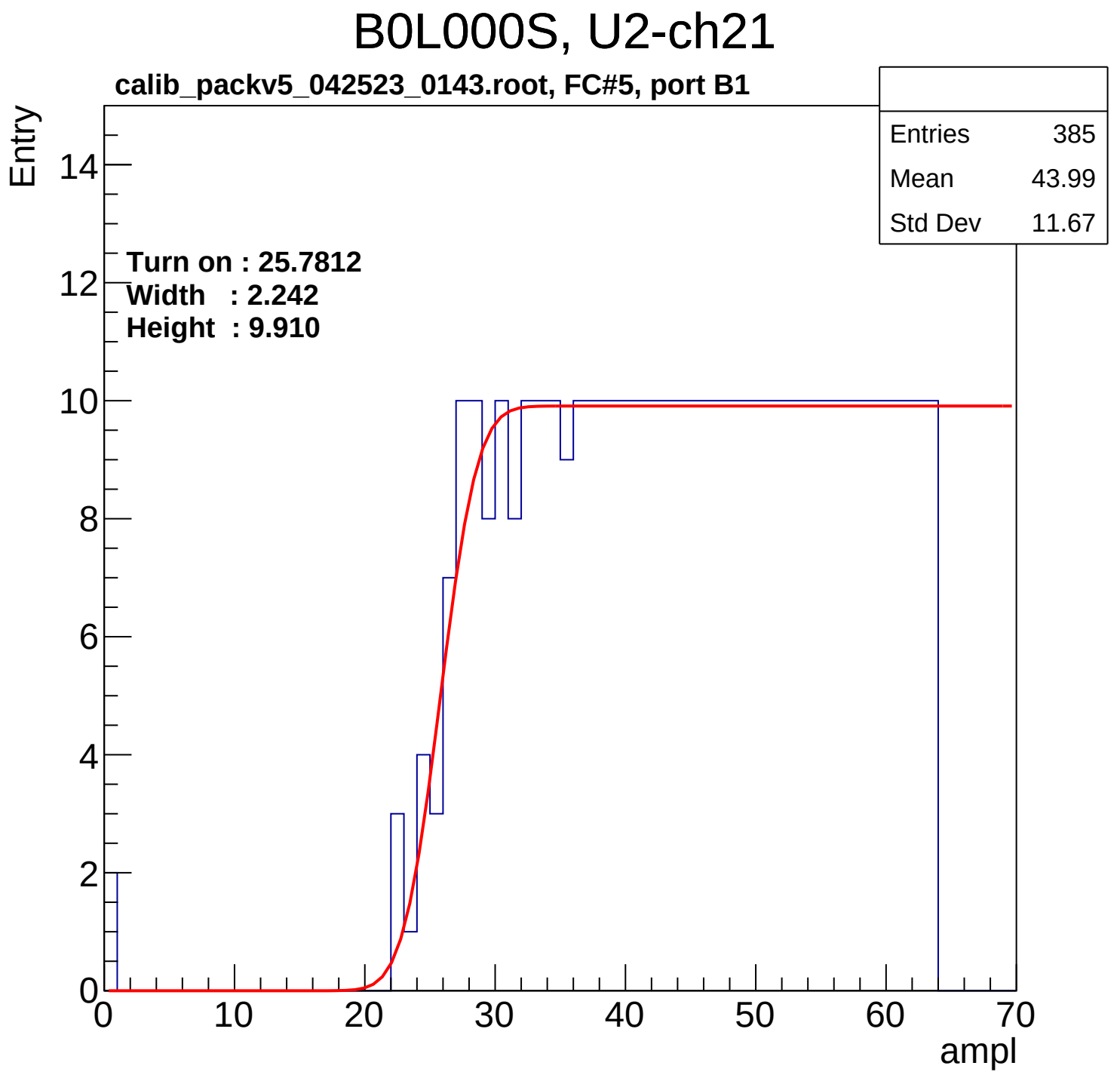
B0L000S, U2-ch21
calib_packv5_042523_0143.root, FC#5, port B1
Entries 385
Mean 43.99
Std Dev 11.67
Turn on : 25.7812
Width : 2.242
Height : 9.910
Entry
ampl
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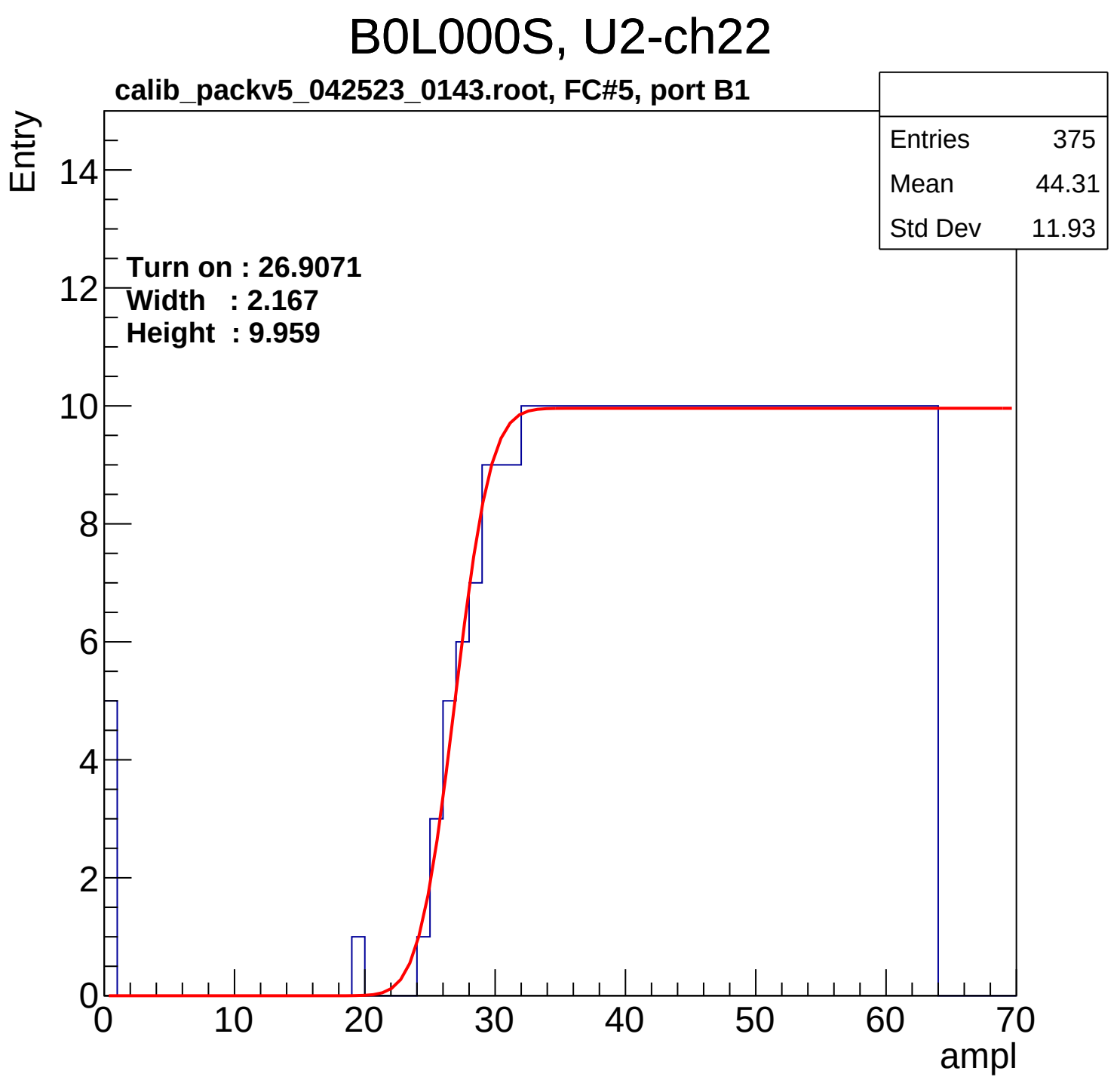
B0L000S, U2-ch22
calib_packv5_042523_0143.root, FC#5, port B1
Entries 375
Mean 44.31
Std Dev 11.93
Turn on : 26.9071
Width : 2.167
Height : 9.959
Entry
ampl
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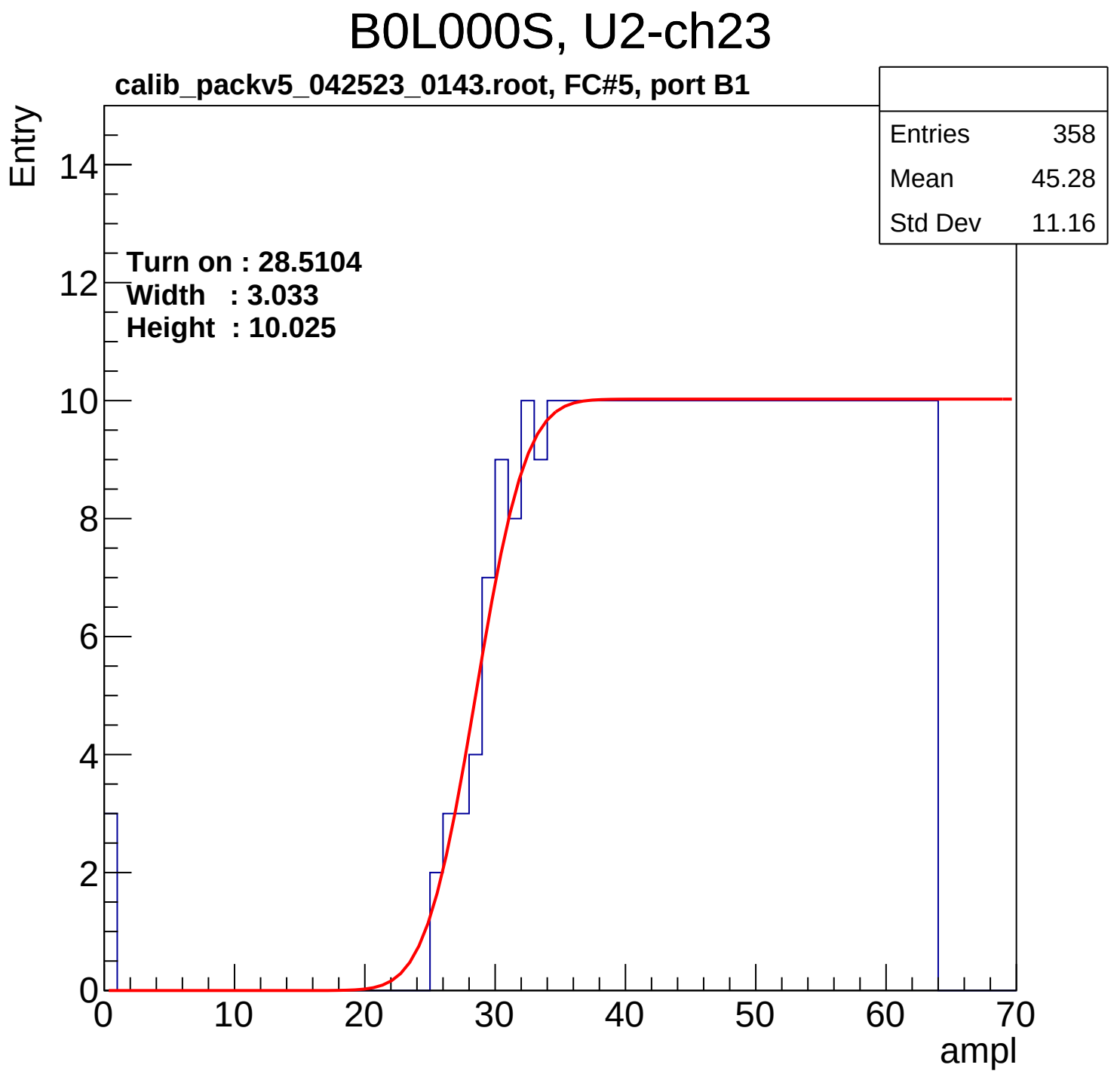
B0L000S, U2-ch23
calib_packv5_042523_0143.root, FC#5, port B1
Entries 358
Mean 45.28
Std Dev 11.16
Turn on : 28.5104
Width : 3.033
Height : 10.025
Entry
ampl
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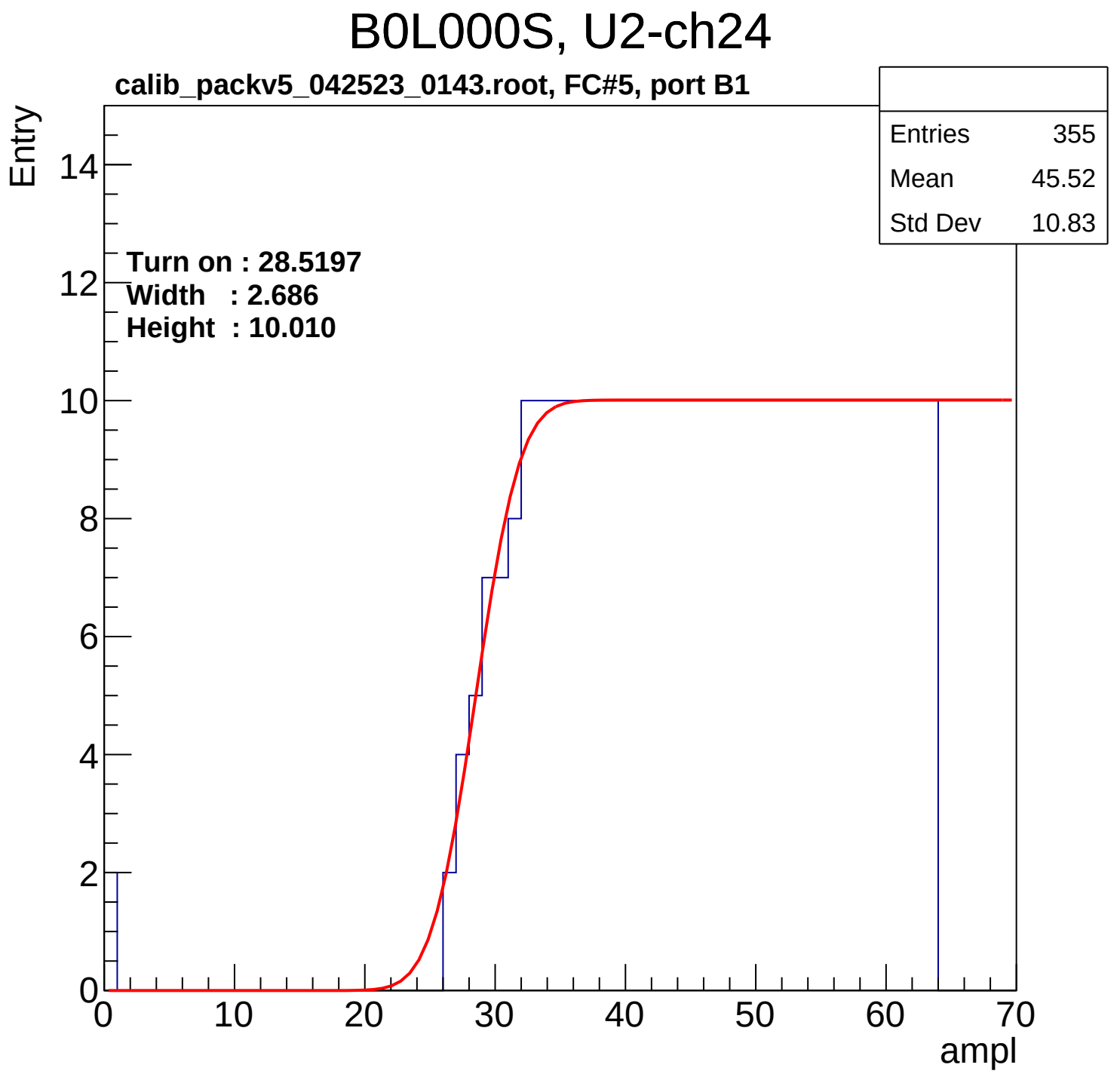
B0L000S, U2-ch24
calib_packv5_042523_0143.root, FC#5, port B1
Entries 355
Mean 45.52
Std Dev 10.83
Turn on : 28.5197
Width : 2.686
Height : 10.010
Entry
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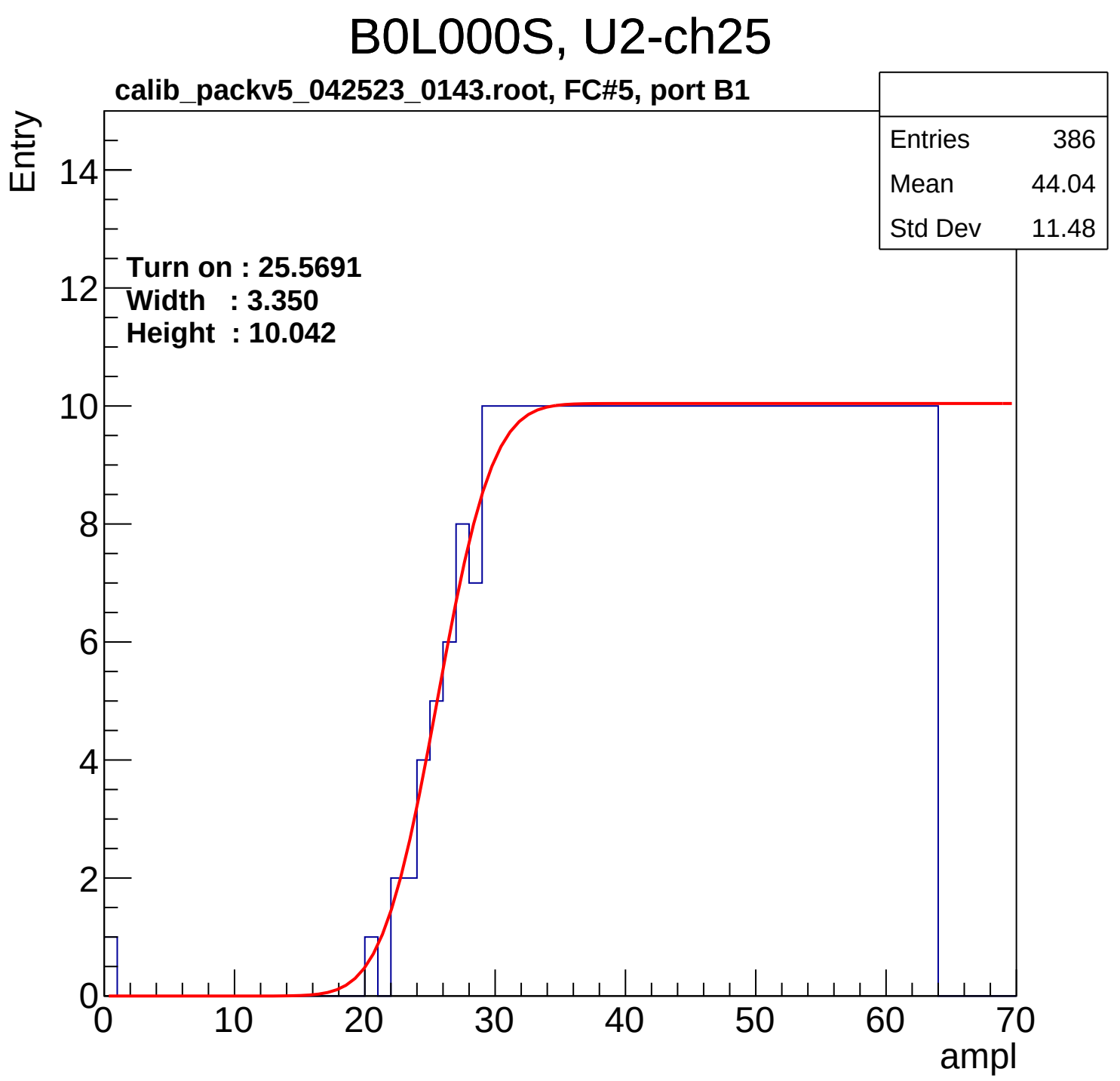
B0L000S, U2-ch25
calib_packv5_042523_0143.root, FC#5, port B1
Entries 386
Mean 44.04
Std Dev 11.48
Turn on : 25.5691
Width : 3.350
Height : 10.042
Entry
ampl
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8
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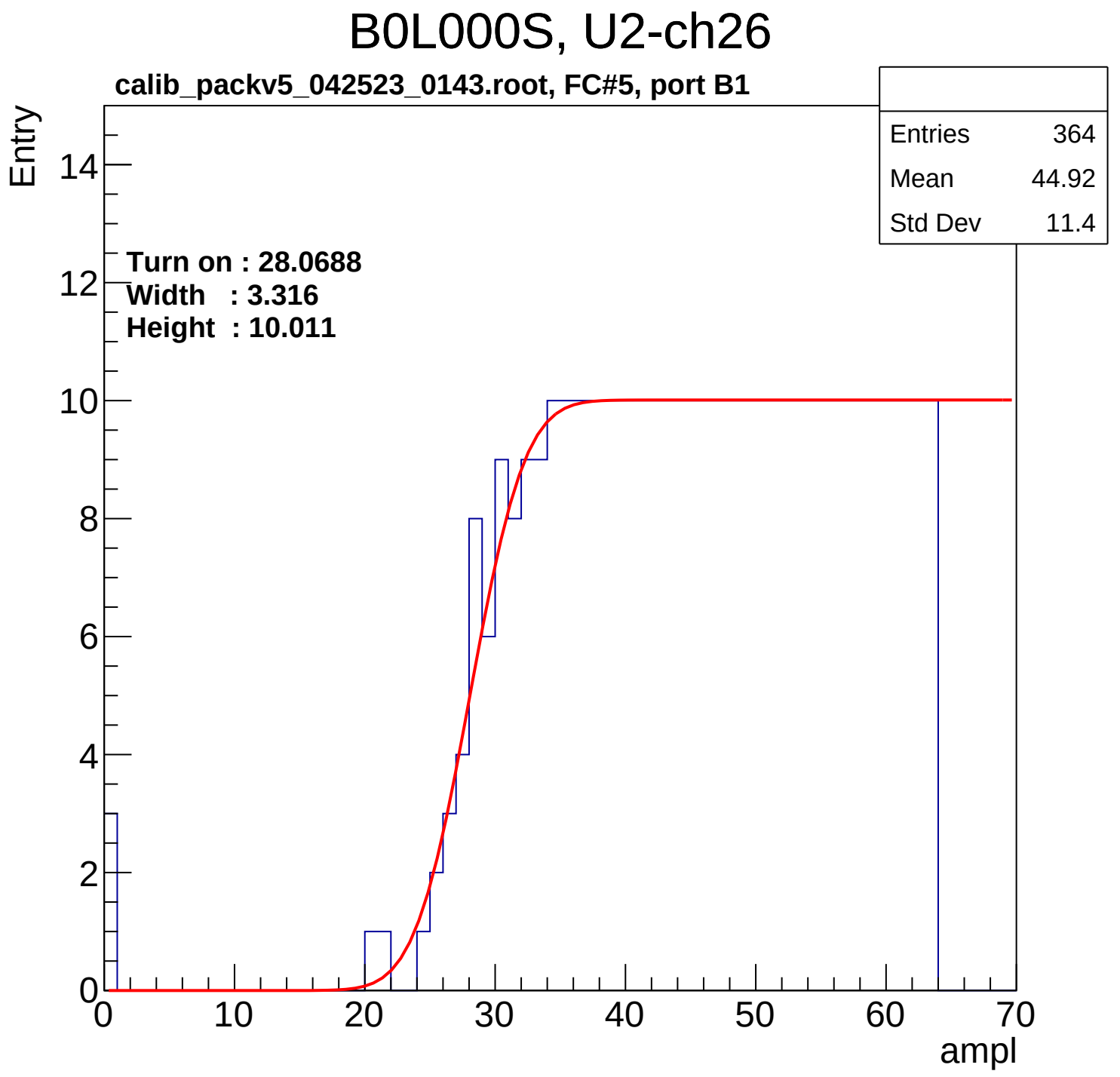
B0L000S, U2-ch26
calib_packv5_042523_0143.root, FC#5, port B1
Entries 364
Mean 44.92
Std Dev 11.4
Turn on : 28.0688
Width : 3.316
Height : 10.011
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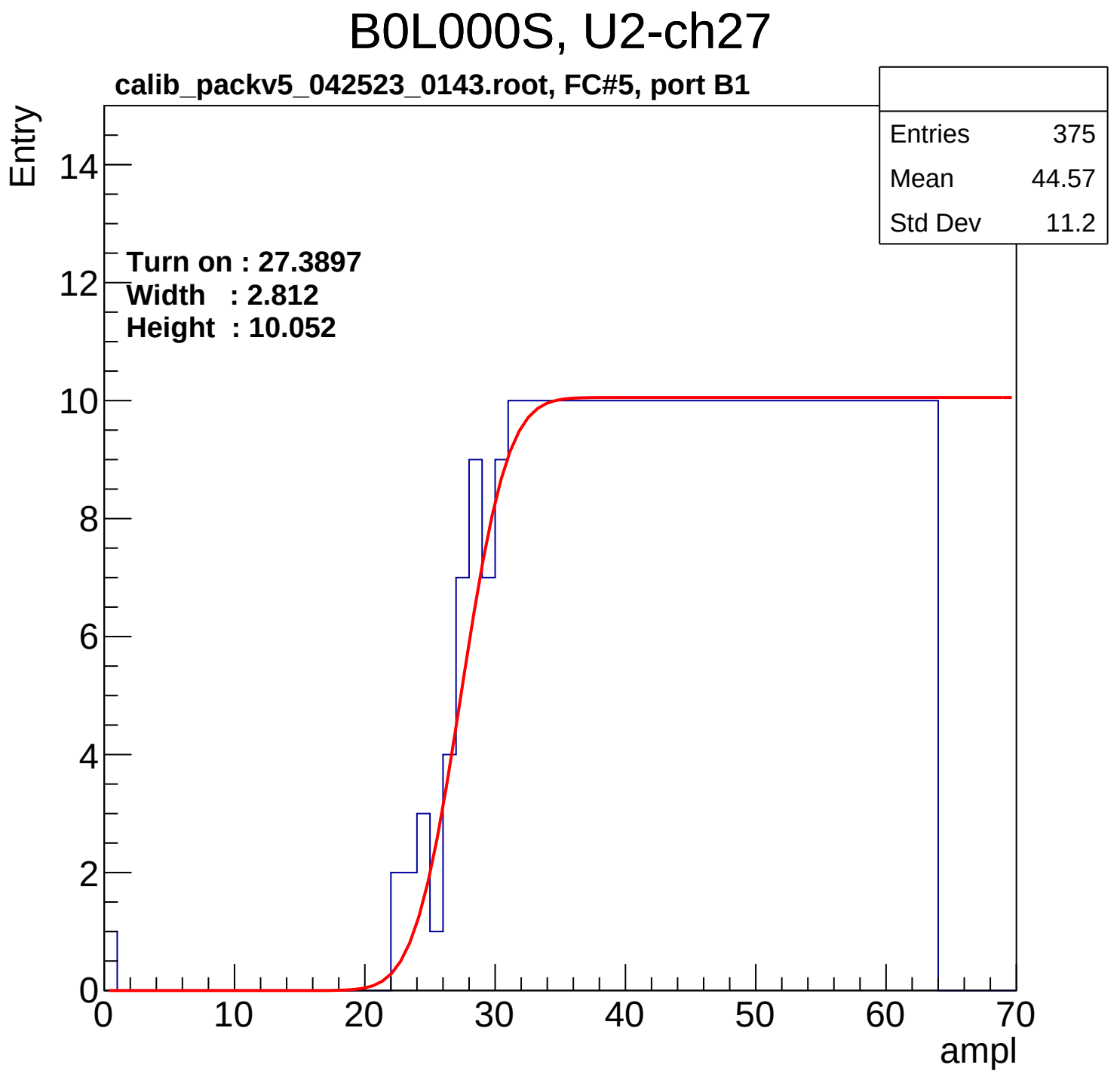
B0L000S, U2-ch27
calib_packv5_042523_0143.root, FC#5, port B1
Entries 375
Mean 44.57
Std Dev 11.2
Turn on : 27.3897
Width : 2.812
Height : 10.052
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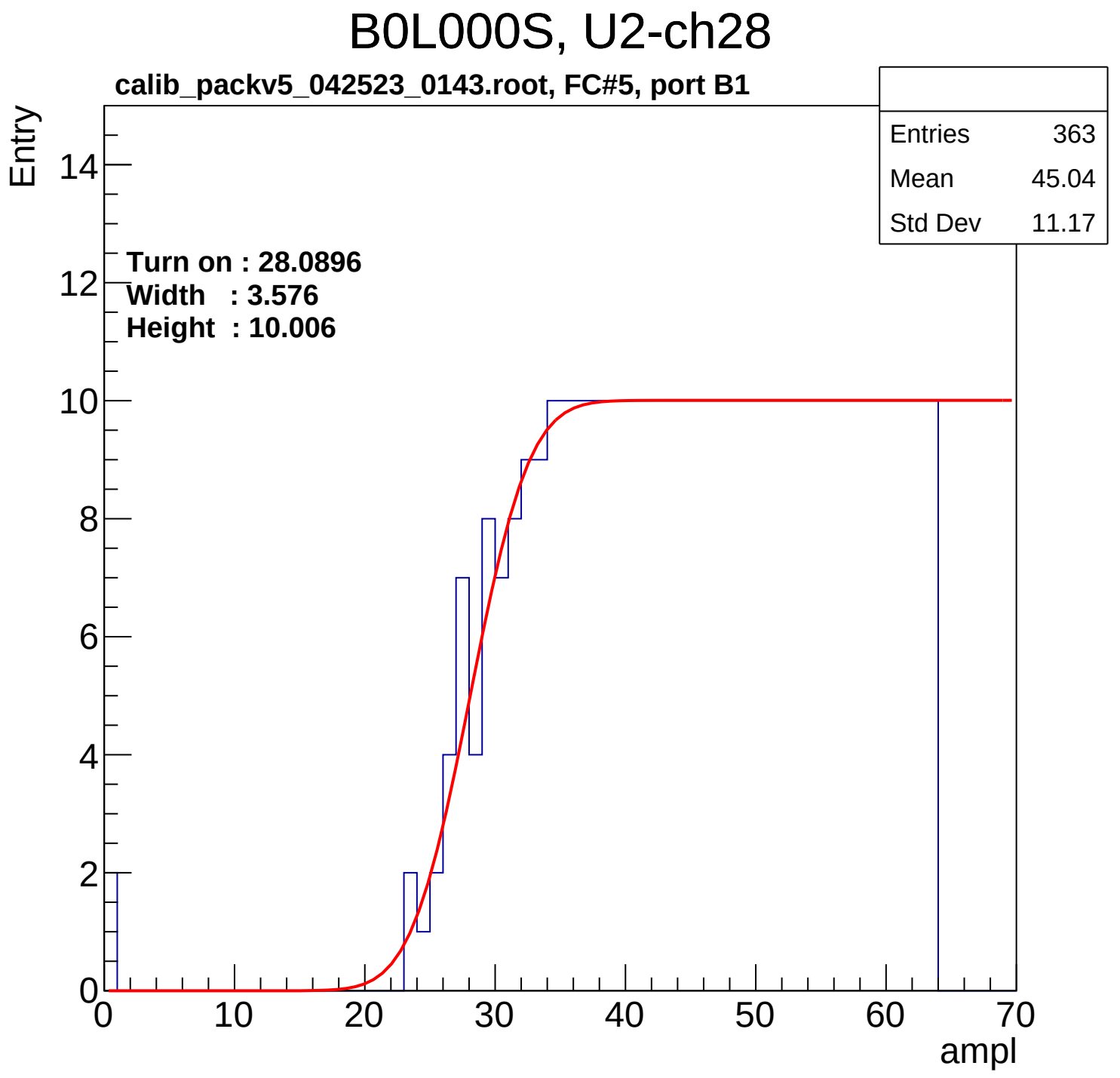
B0L000S, U2-ch28
calib_packv5_042523_0143.root, FC#5, port B1
Entries 363
Mean 45.04
Std Dev 11.17
Turn on : 28.0896
Width : 3.576
Height : 10.006
Entry
ampl
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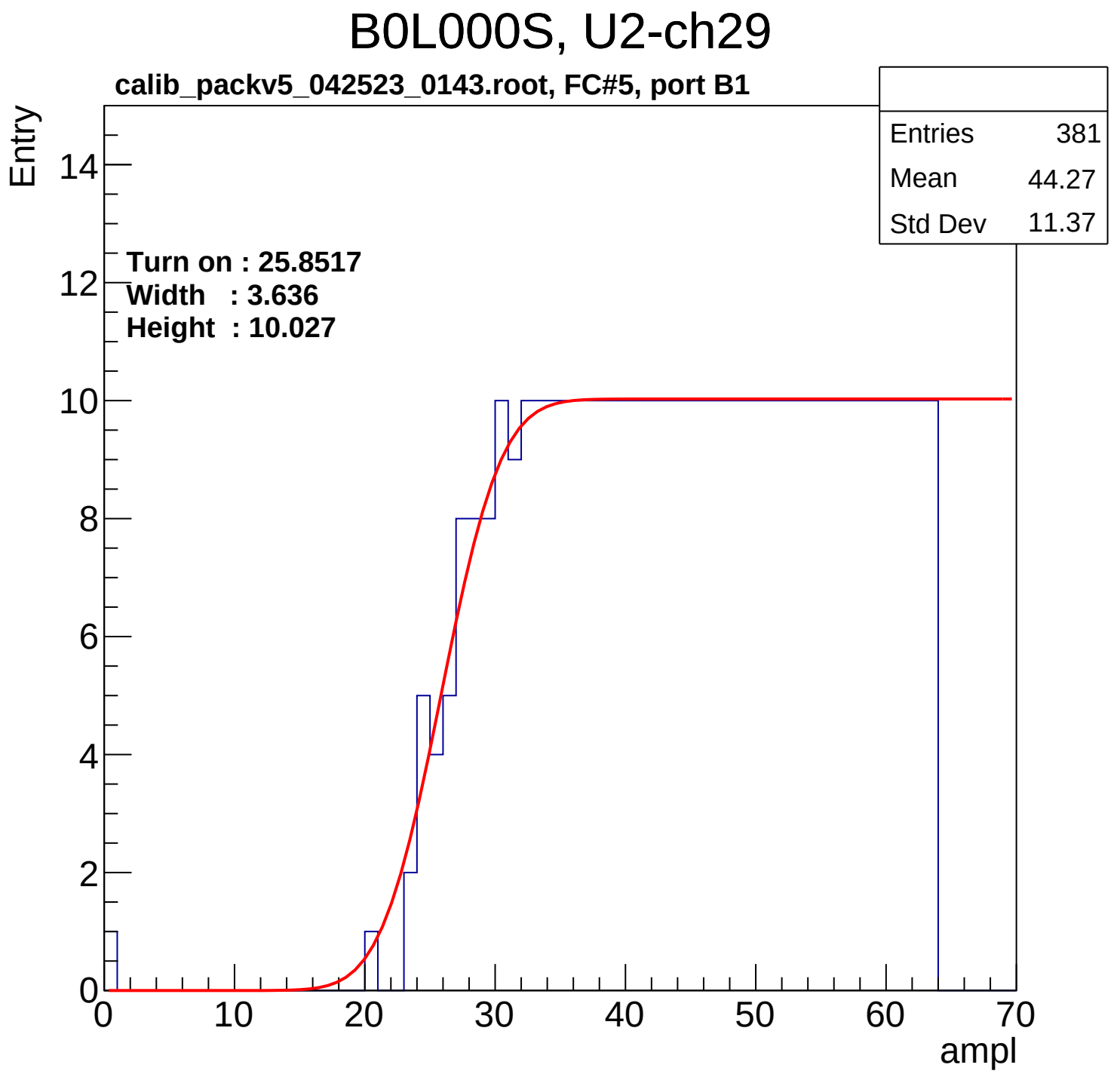
B0L000S, U2-ch29
calib_packv5_042523_0143.root, FC#5, port B1
Entries 381
Mean 44.27
Std Dev 11.37
Turn on : 25.8517
Width : 3.636
Height : 10.027
Entry
ampl
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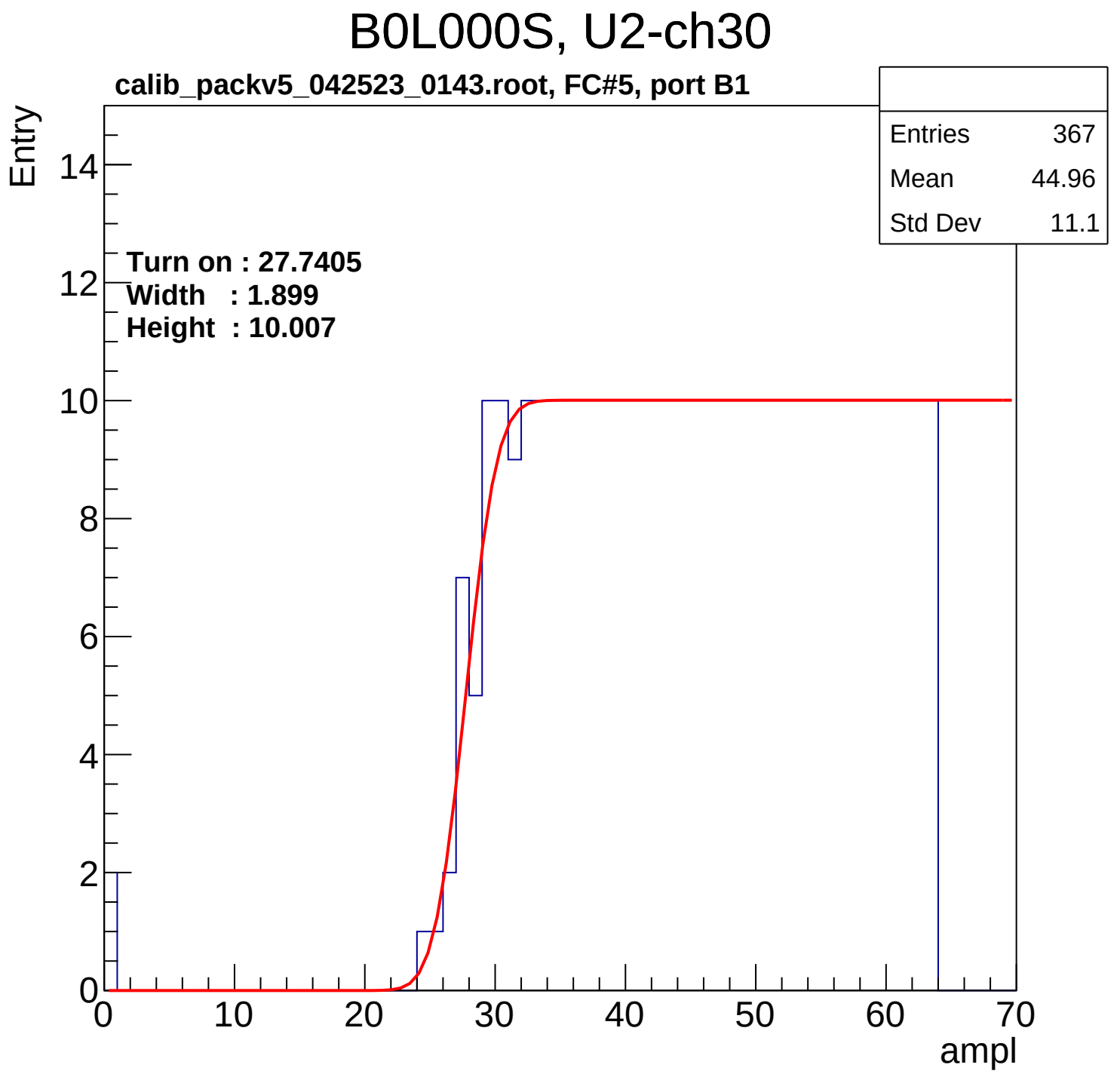
B0L000S, U2-ch30
calib_packv5_042523_0143.root, FC#5, port B1
Entries 367
Mean 44.96
Std Dev 11.1
Turn on : 27.7405
Width : 1.899
Height : 10.007
Entry
ampl
0
2
4
6
8
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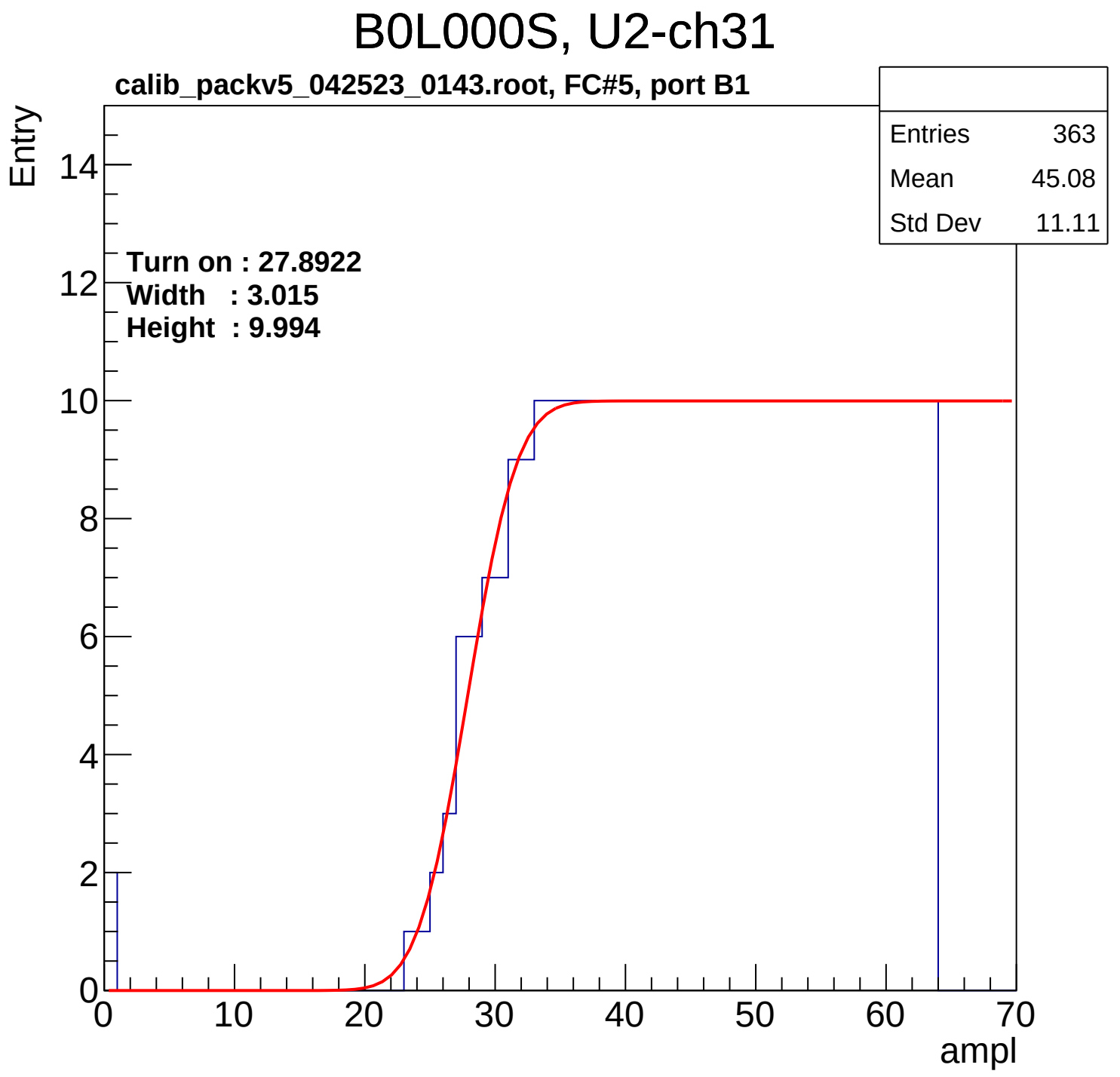
B0L000S, U2-ch31
calib_packv5_042523_0143.root, FC#5, port B1
Entries 363
Mean 45.08
Std Dev 11.11
Turn on : 27.8922
Width : 3.015
Height : 9.994
Entry
ampl
0
2
4
6
8
10
12
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0
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40
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60
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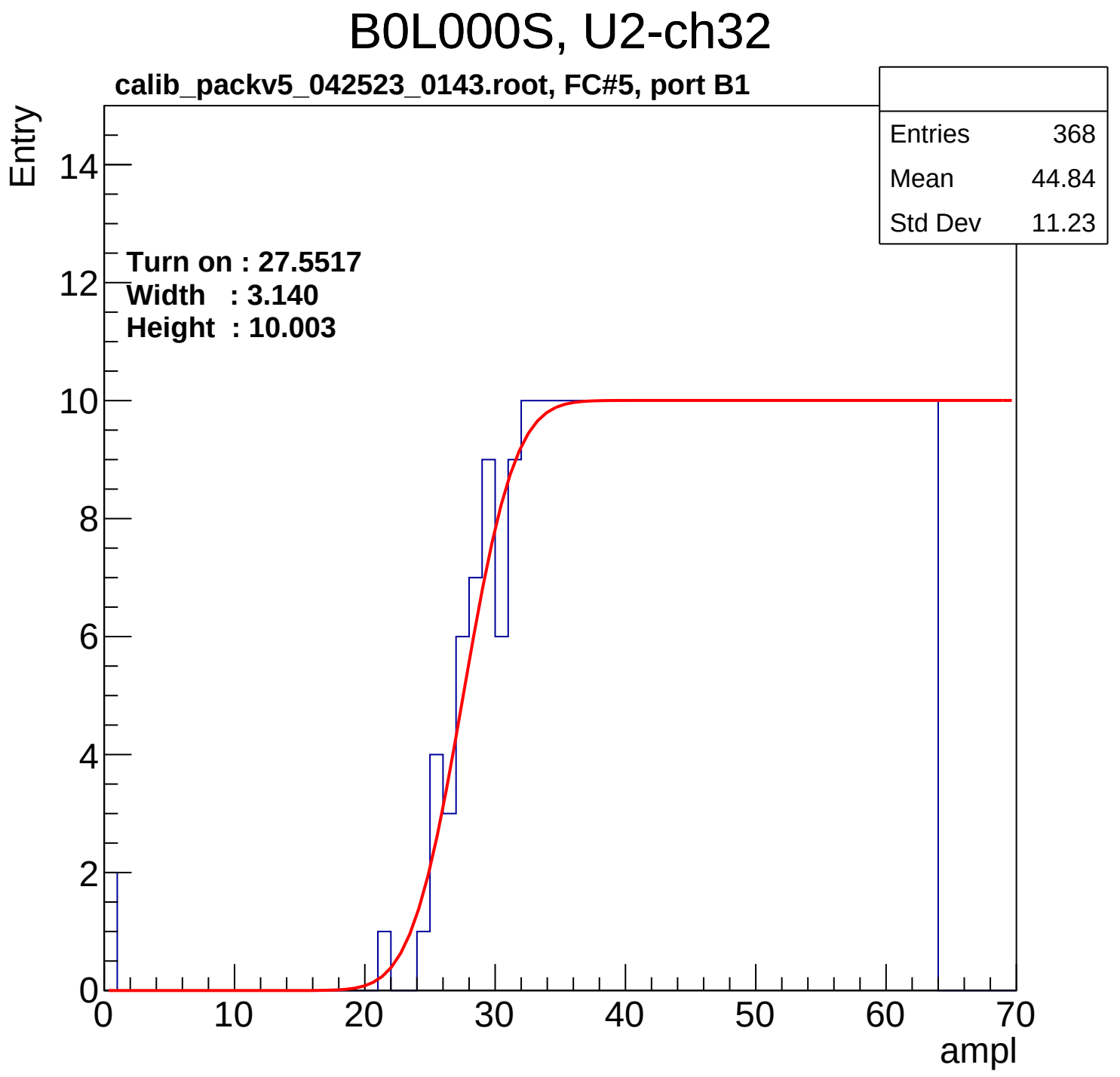
B0L000S, U2-ch32
calib_packv5_042523_0143.root, FC#5, port B1
Entries 368
Mean 44.84
Std Dev 11.23
Turn on : 27.5517
Width : 3.140
Height : 10.003
Entry
ampl
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2
4
6
8
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0
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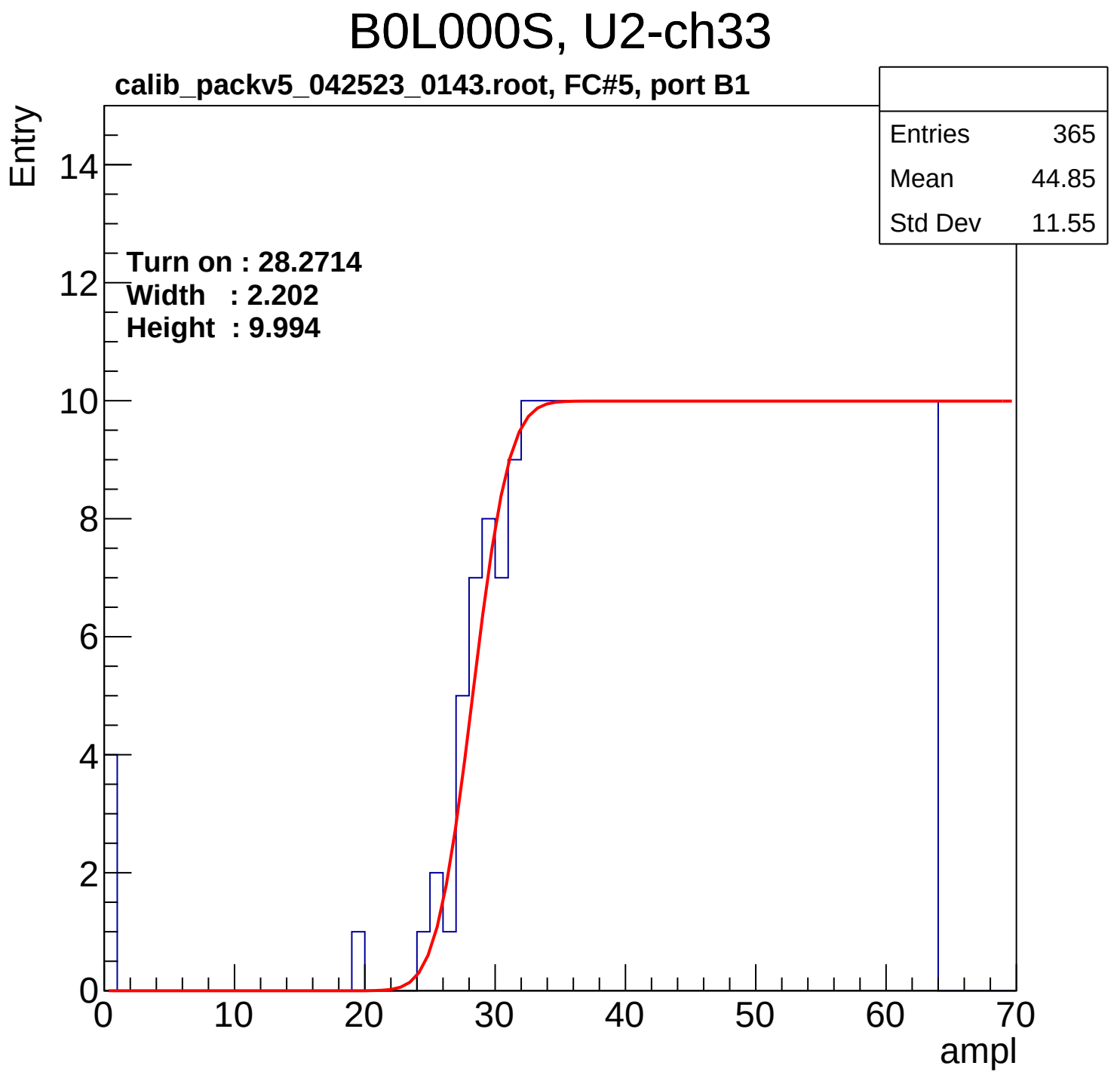
B0L000S, U2-ch33
calib_packv5_042523_0143.root, FC#5, port B1
Entries 365
Mean 44.85
Std Dev 11.55
Turn on : 28.2714
Width : 2.202
Height : 9.994
Entry
ampl
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2
4
6
8
10
12
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0
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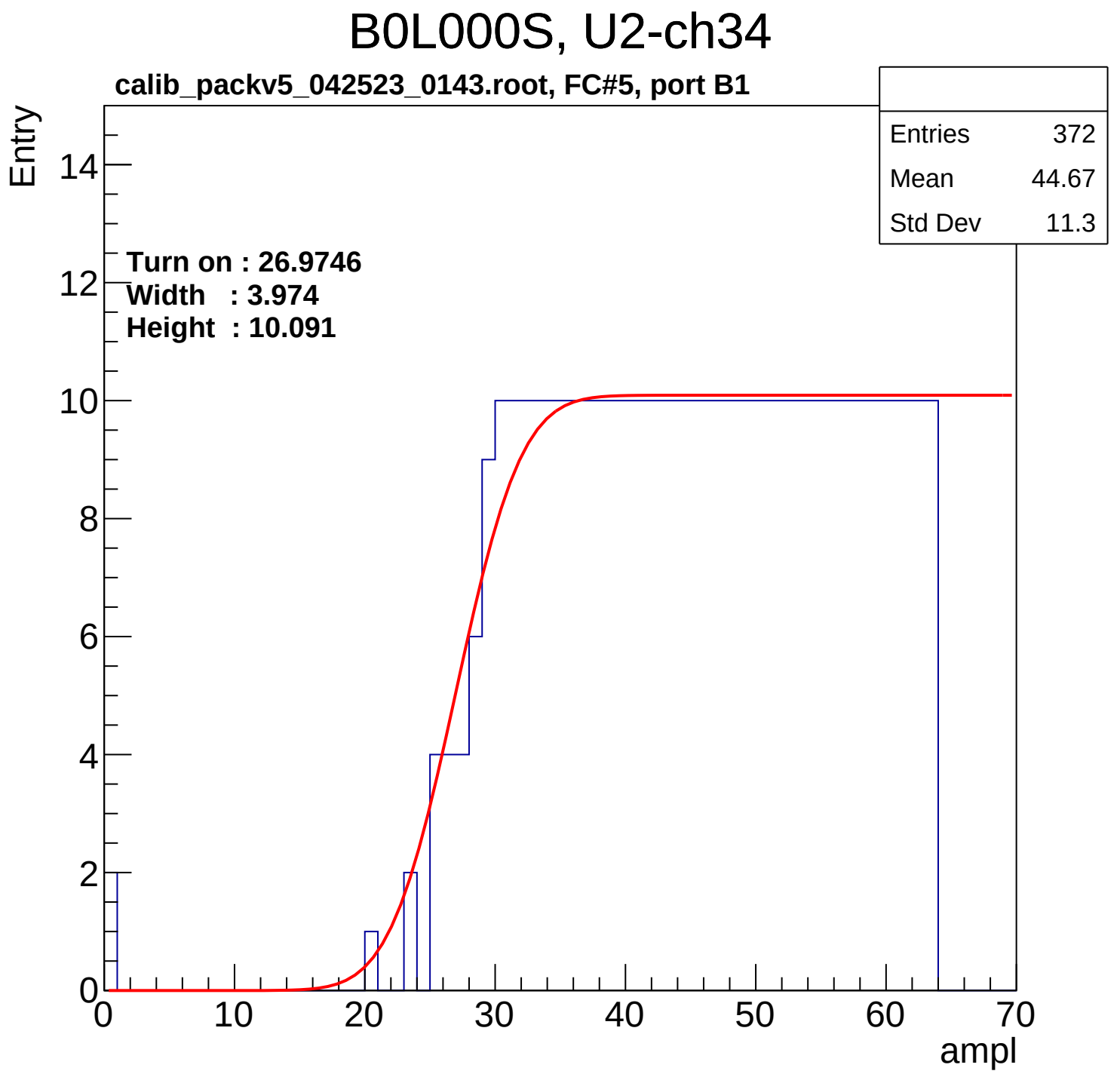
B0L000S, U2-ch34
calib_packv5_042523_0143.root, FC#5, port B1
Entries 372
Mean 44.67
Std Dev 11.3
Turn on : 26.9746
Width : 3.974
Height : 10.091
Entry
ampl
0
2
4
6
8
10
12
14
0
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20
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60
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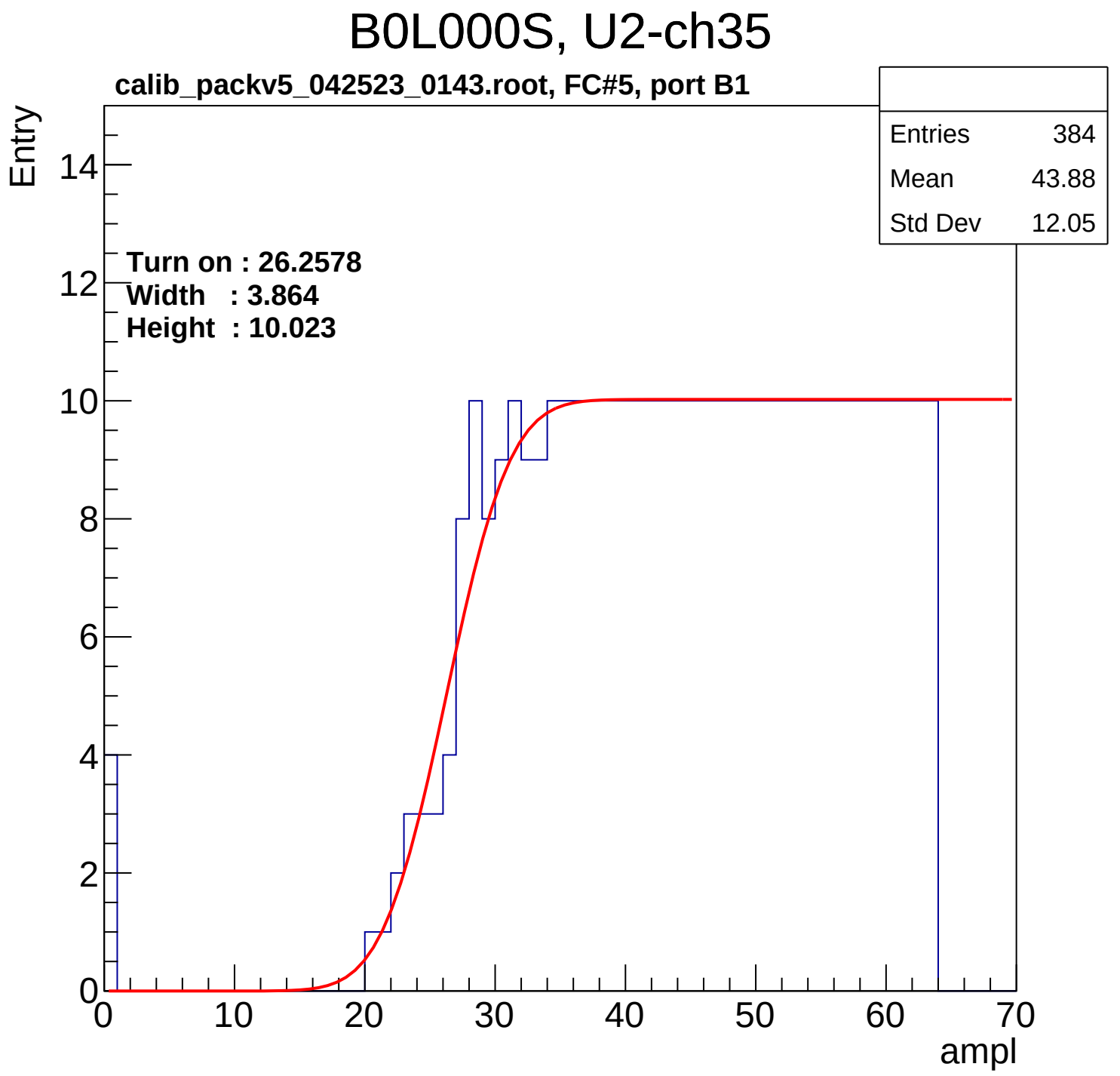
B0L000S, U2-ch35
calib_packv5_042523_0143.root, FC#5, port B1
Entries 384
Mean 43.88
Std Dev 12.05
Turn on : 26.2578
Width : 3.864
Height : 10.023
Entry
ampl
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2
4
6
8
10
12
14
0
10
20
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40
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60
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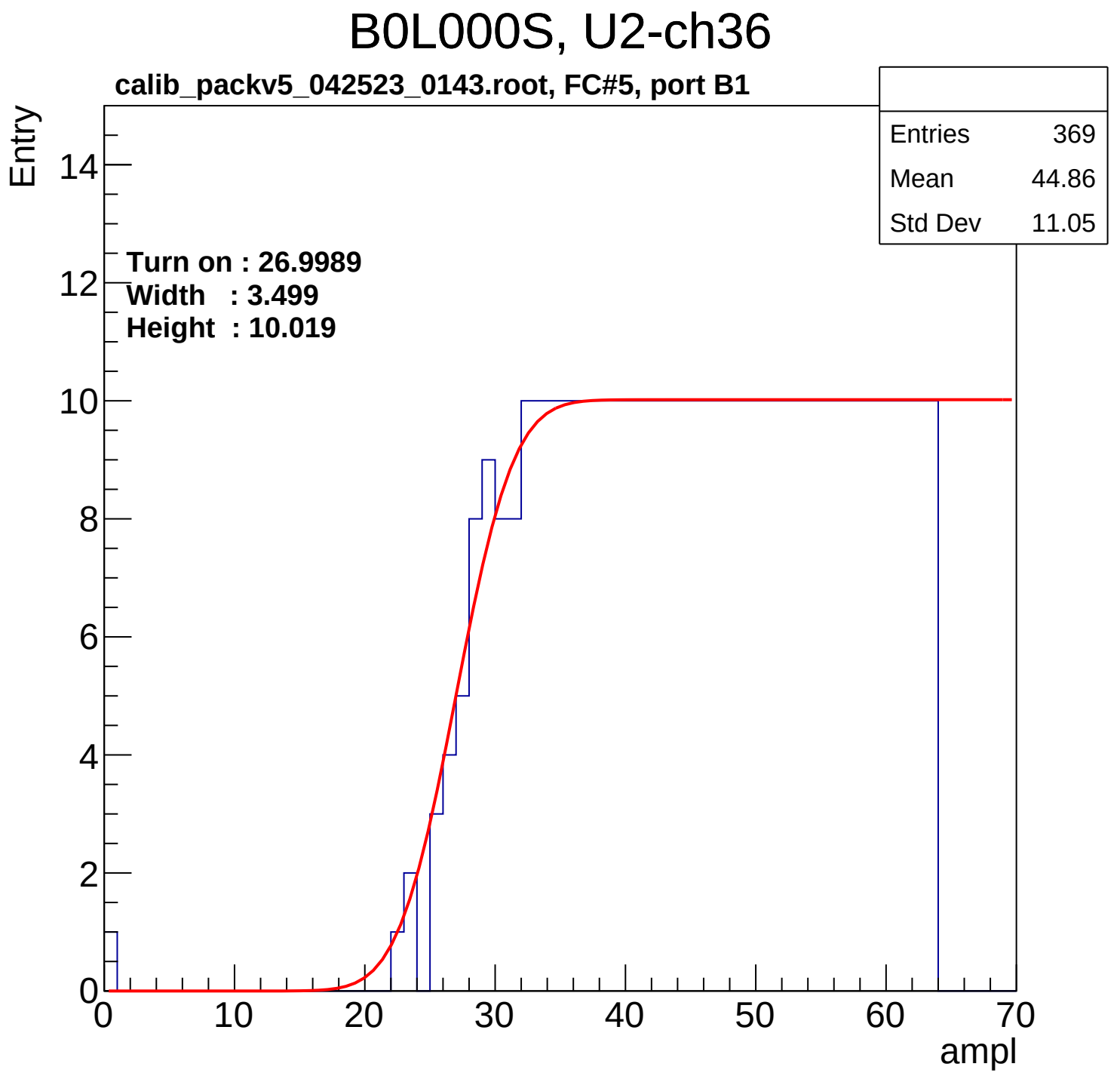
B0L000S, U2-ch36
calib_packv5_042523_0143.root, FC#5, port B1
Entries 369
Mean 44.86
Std Dev 11.05
Turn on : 26.9989
Width : 3.499
Height : 10.019
Entry
ampl
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2
4
6
8
10
12
14
0
10
20
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40
50
60
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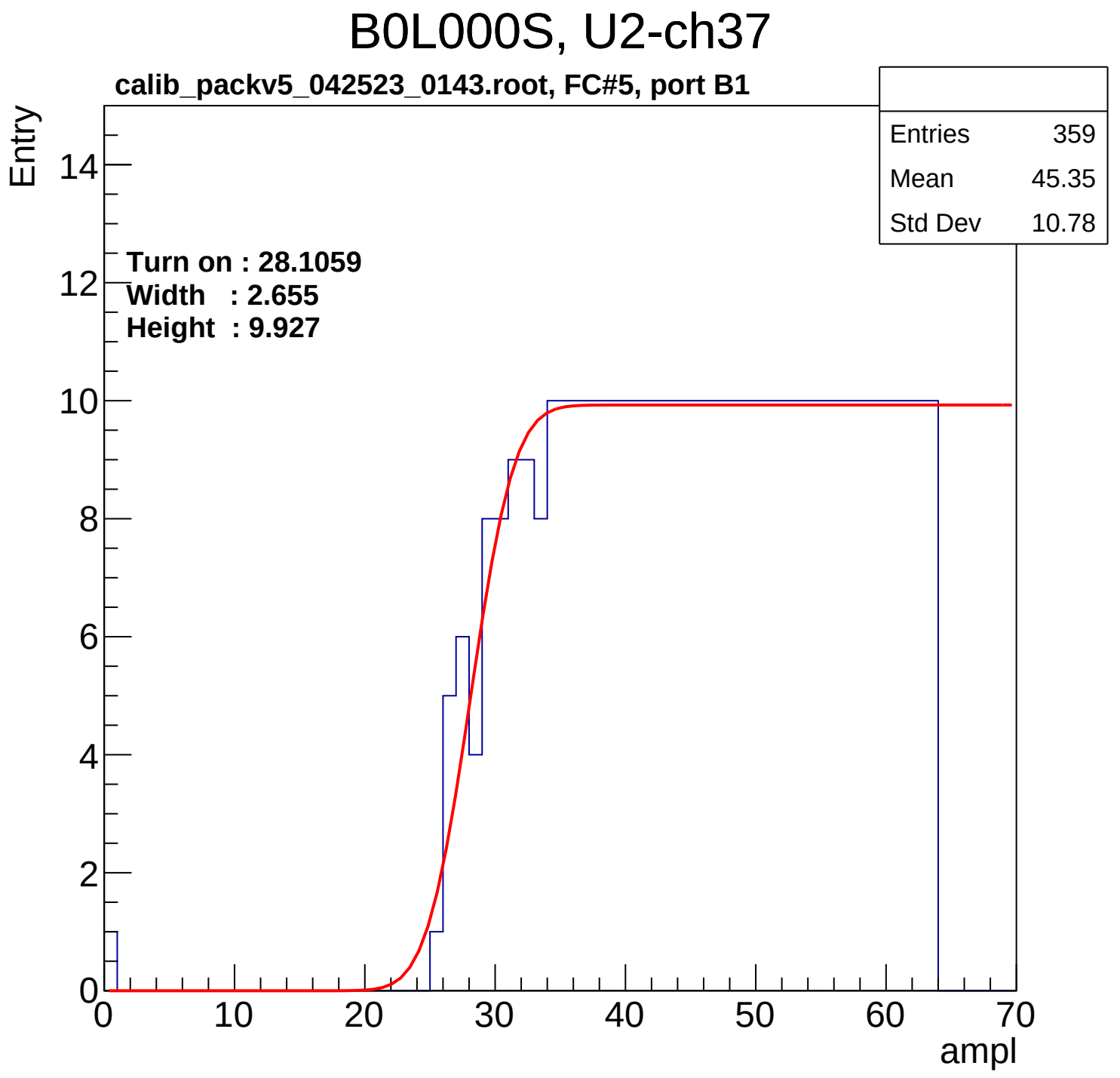
B0L000S, U2-ch37
calib_packv5_042523_0143.root, FC#5, port B1
Entries 359
Mean 45.35
Std Dev 10.78
Turn on : 28.1059
Width : 2.655
Height : 9.927
Entry
ampl
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2
4
6
8
10
12
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0
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60
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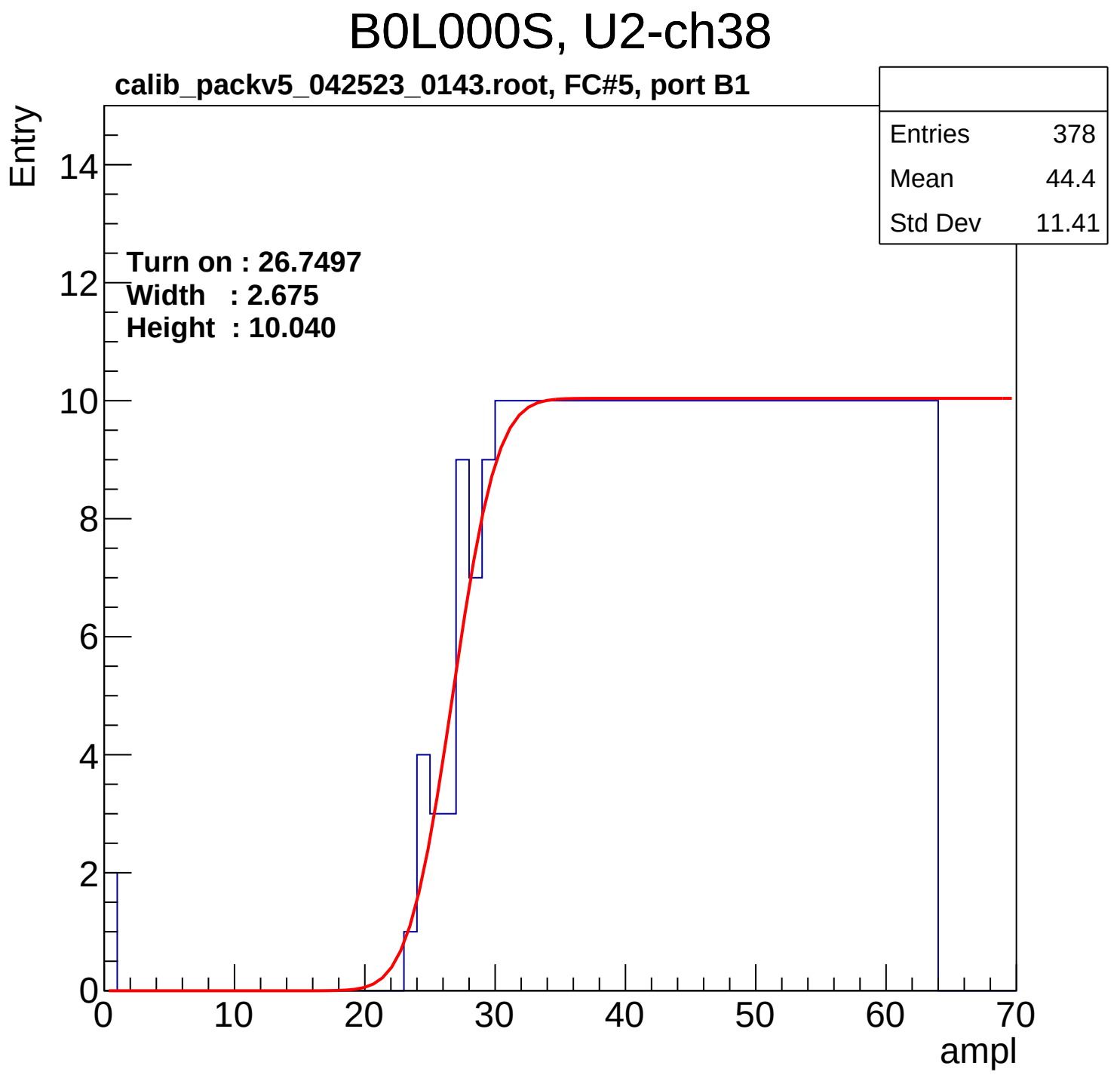
B0L000S, U2-ch38
calib_packv5_042523_0143.root, FC#5, port B1
Entries 378
Mean 44.4
Std Dev 11.41
Turn on : 26.7497
Width : 2.675
Height : 10.040
Entry
ampl
0
2
4
6
8
10
12
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0
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40
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60
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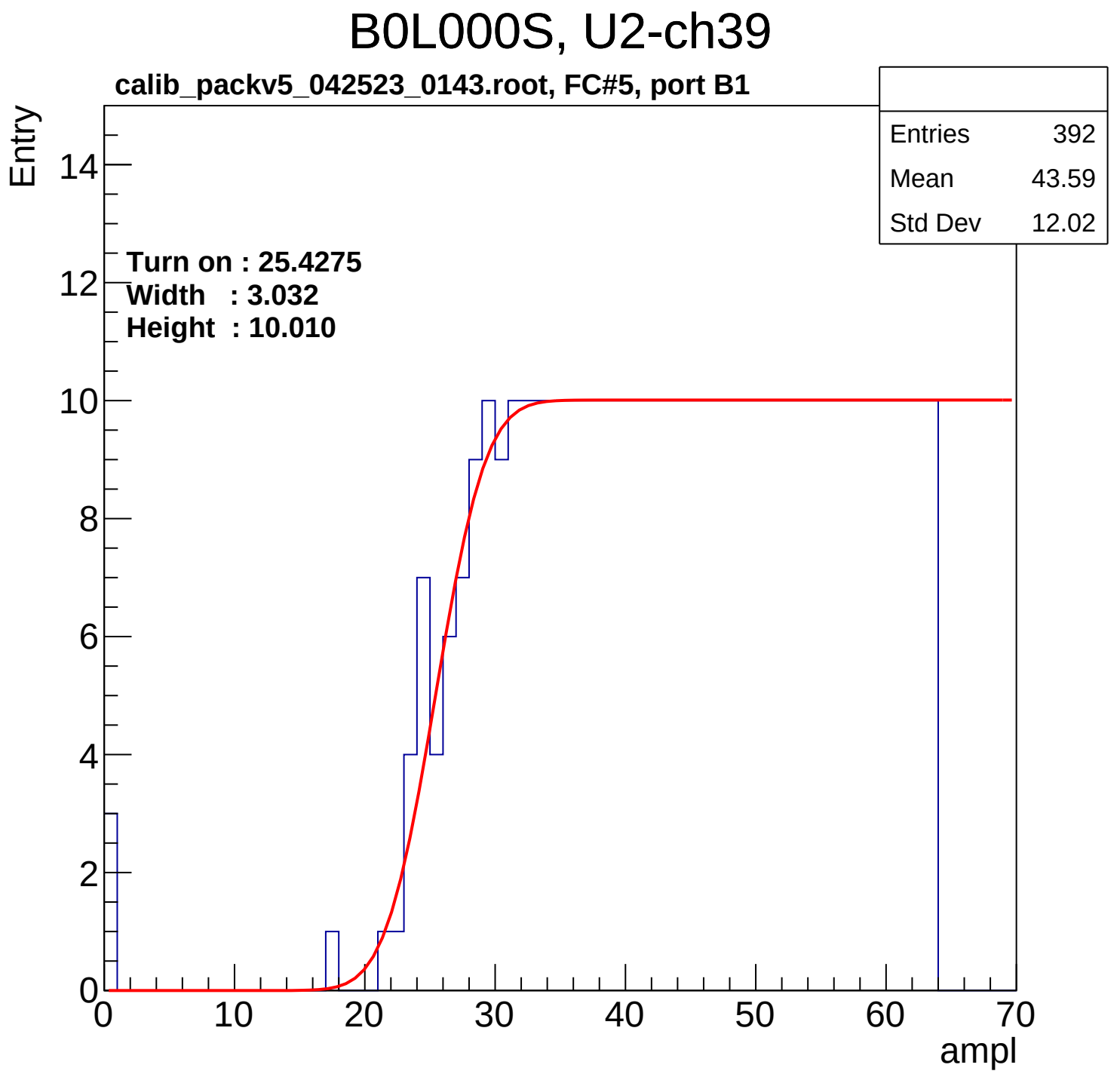
B0L000S, U2-ch39
calib_packv5_042523_0143.root, FC#5, port B1
Entries 392
Mean 43.59
Std Dev 12.02
Turn on : 25.4275
Width : 3.032
Height : 10.010
Entry
ampl
0
2
4
6
8
10
12
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0
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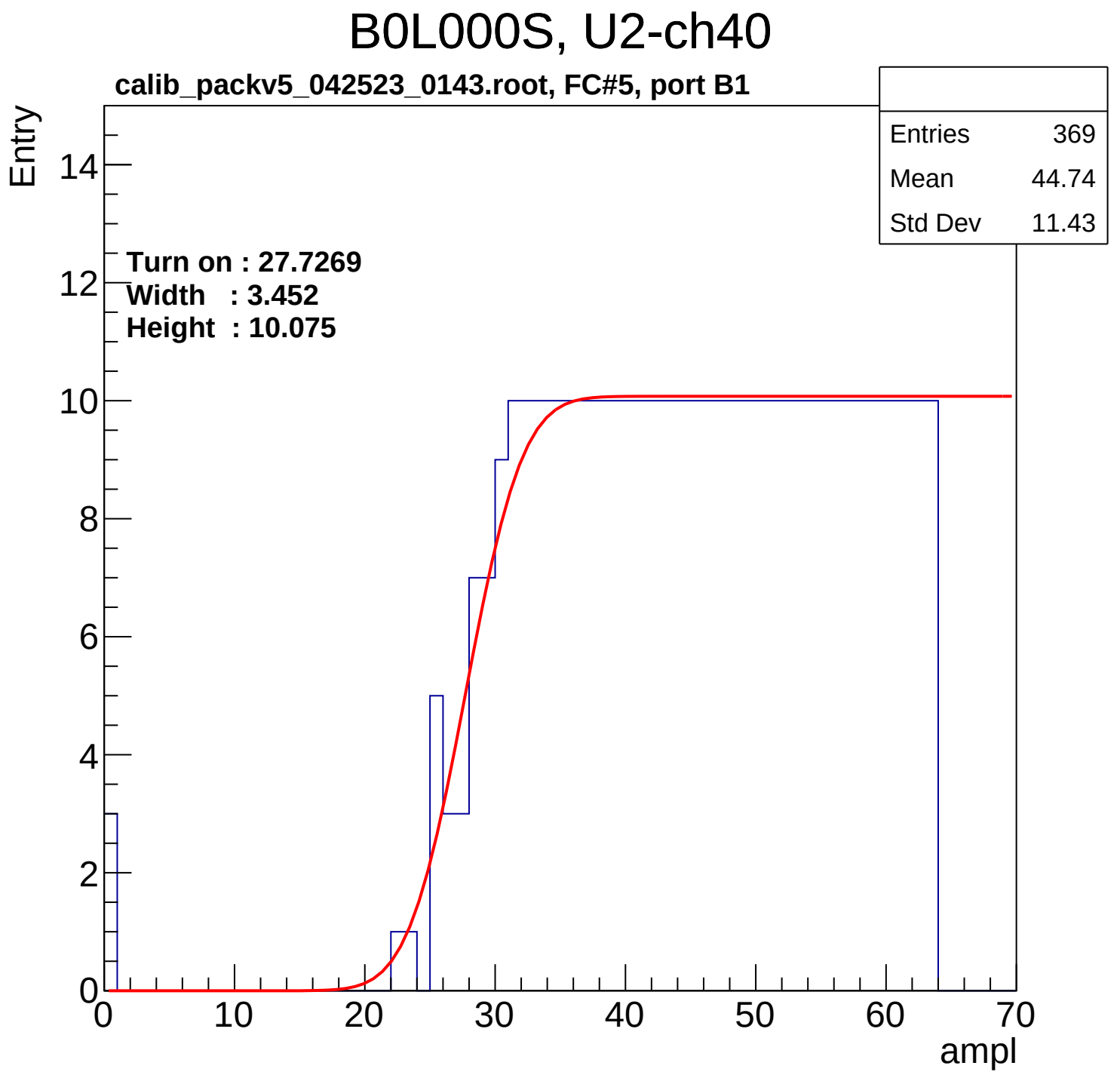
B0L000S, U2-ch40
calib_packv5_042523_0143.root, FC#5, port B1
Entries 369
Mean 44.74
Std Dev 11.43
Turn on : 27.7269
Width : 3.452
Height : 10.075
Entry
ampl
0
2
4
6
8
10
12
14
0
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20
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60
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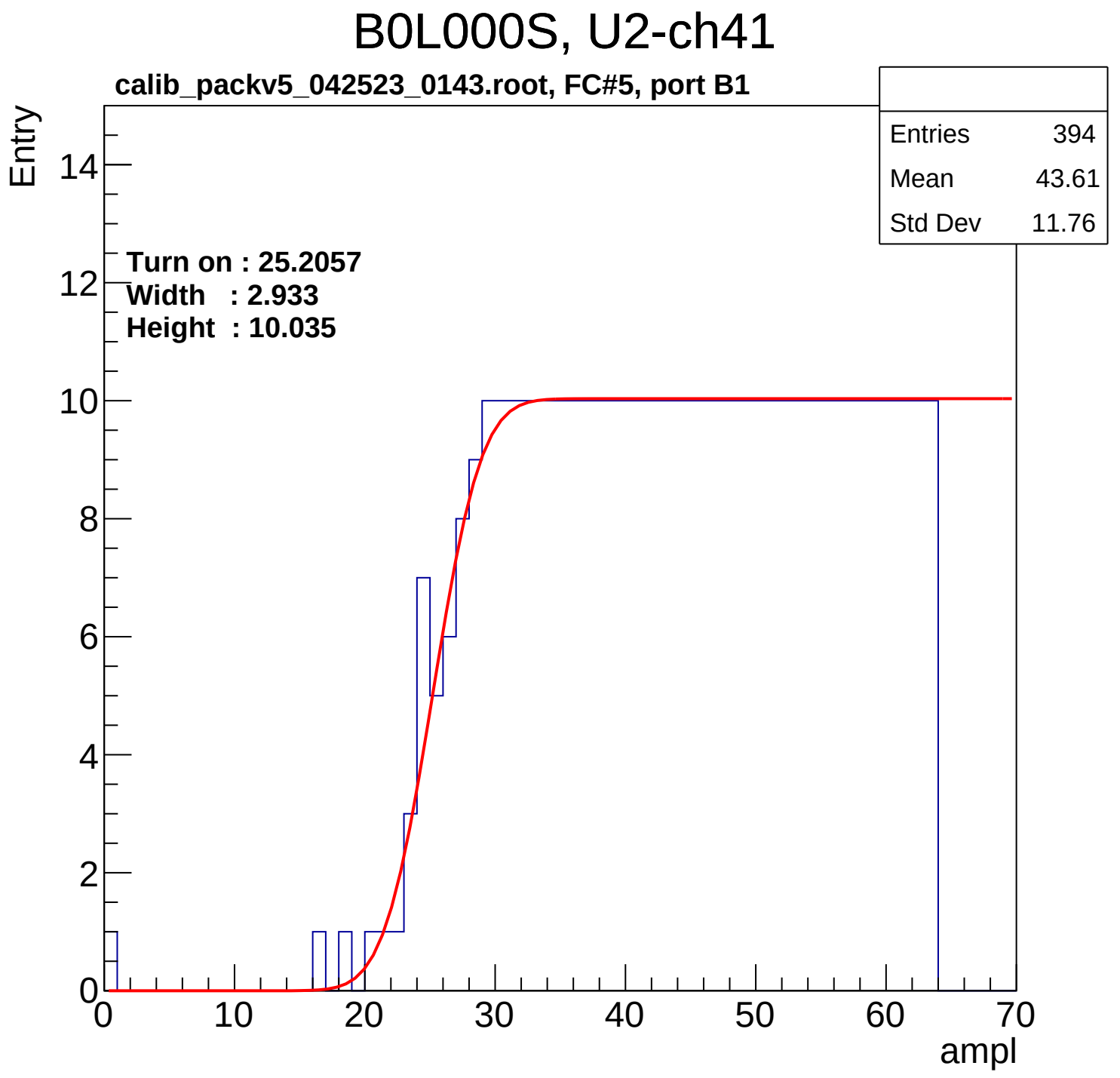
B0L000S, U2-ch41
calib_packv5_042523_0143.root, FC#5, port B1
Entries 394
Mean 43.61
Std Dev 11.76
Turn on : 25.2057
Width : 2.933
Height : 10.035
Entry
ampl
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2
4
6
8
10
12
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0
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20
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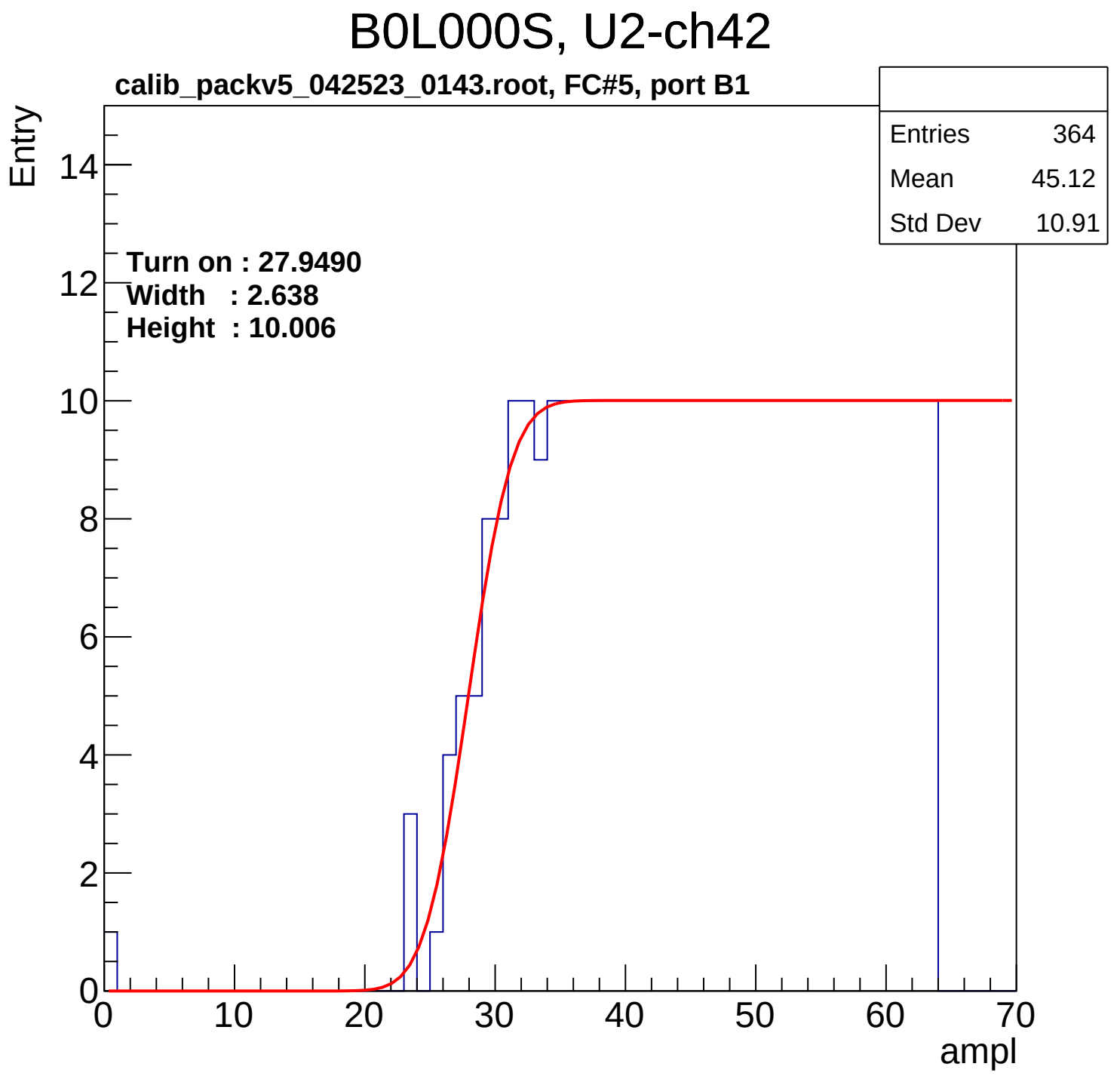
B0L000S, U2-ch42
calib_packv5_042523_0143.root, FC#5, port B1
Entries 364
Mean 45.12
Std Dev 10.91
Turn on : 27.9490
Width : 2.638
Height : 10.006
Entry
ampl
0
2
4
6
8
10
12
14
0
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20
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60
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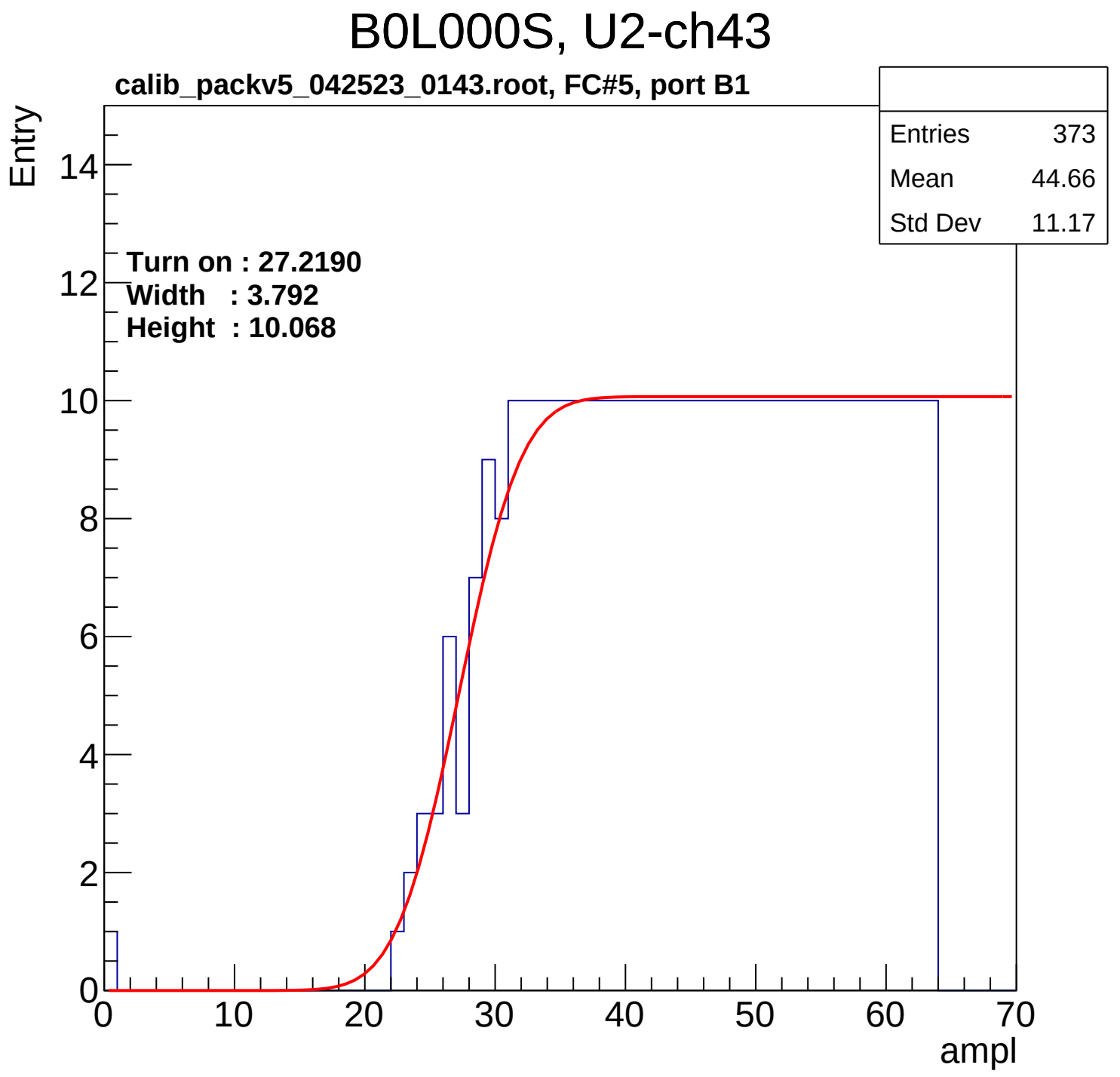
B0L000S, U2-ch43
calib_packv5_042523_0143.root, FC#5, port B1
Entries 373
Mean 44.66
Std Dev 11.17
Turn on : 27.2190
Width : 3.792
Height : 10.068
Entry
ampl
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4
6
8
10
12
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0
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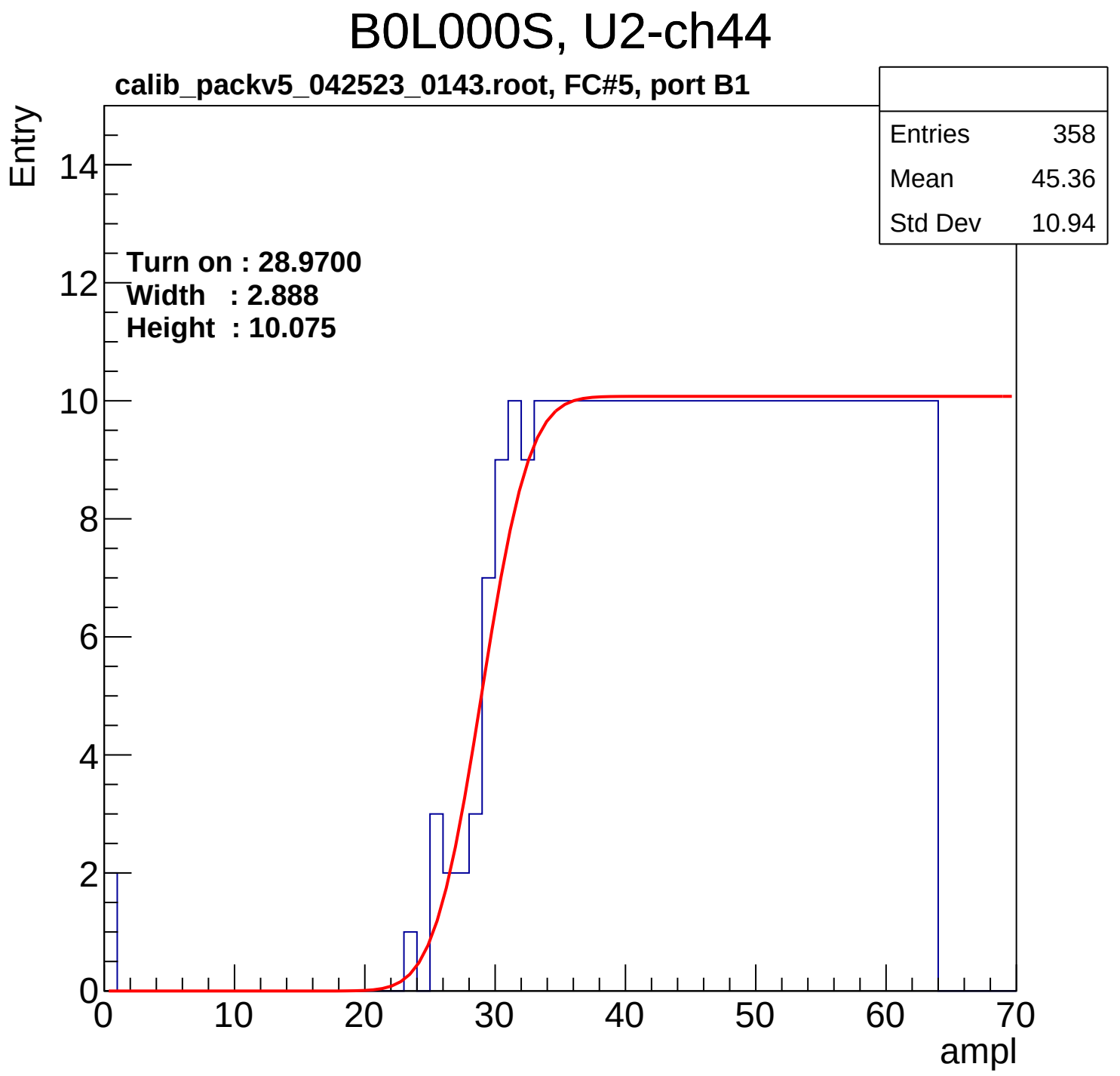
B0L000S, U2-ch44
calib_packv5_042523_0143.root, FC#5, port B1
Entries 358
Mean 45.36
Std Dev 10.94
Turn on : 28.9700
Width : 2.888
Height : 10.075
Entry
ampl
0
2
4
6
8
10
12
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0
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60
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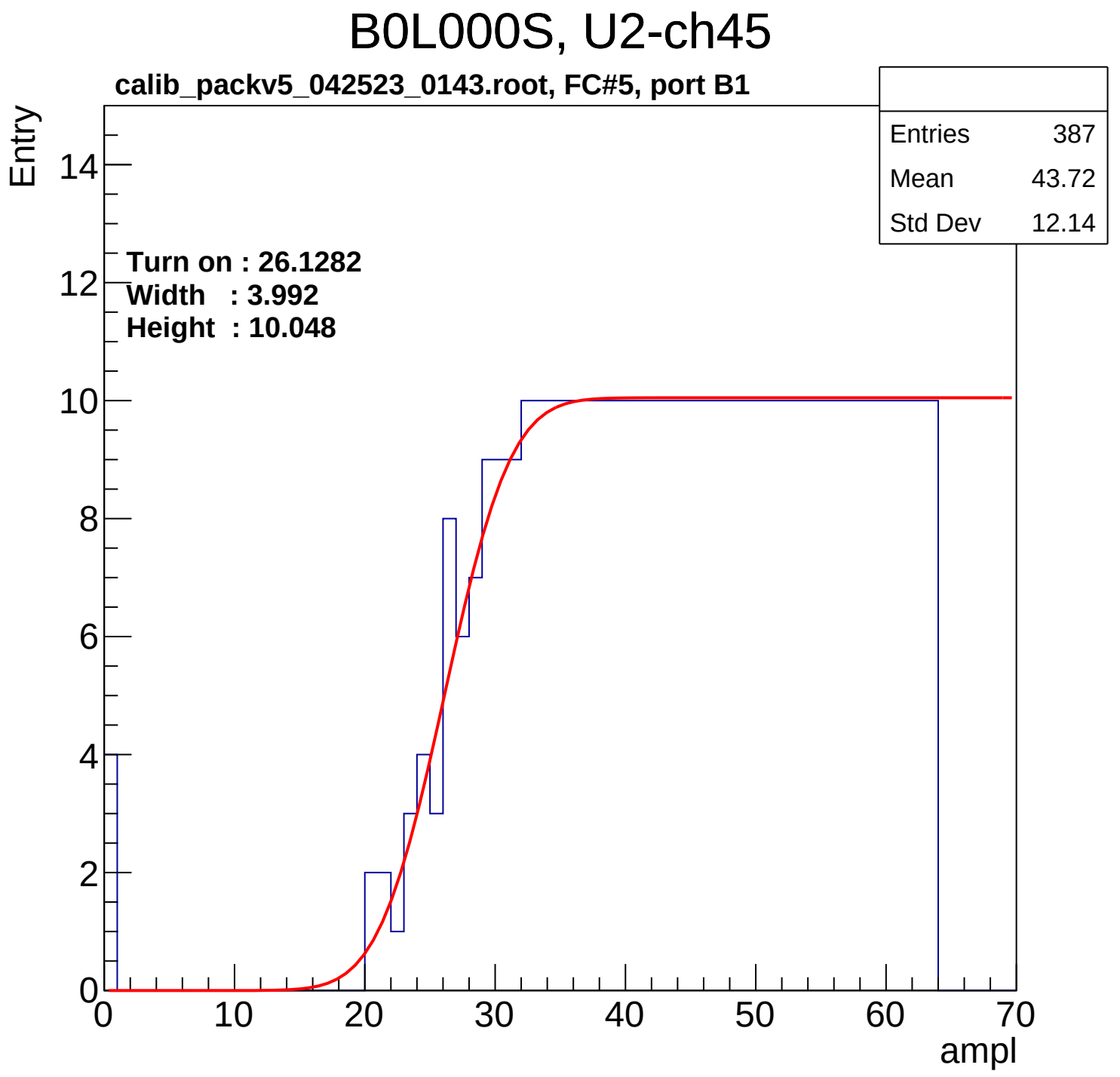
B0L000S, U2-ch45
calib_packv5_042523_0143.root, FC#5, port B1
Entries 387
Mean 43.72
Std Dev 12.14
Turn on : 26.1282
Width : 3.992
Height : 10.048
Entry
ampl
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6
8
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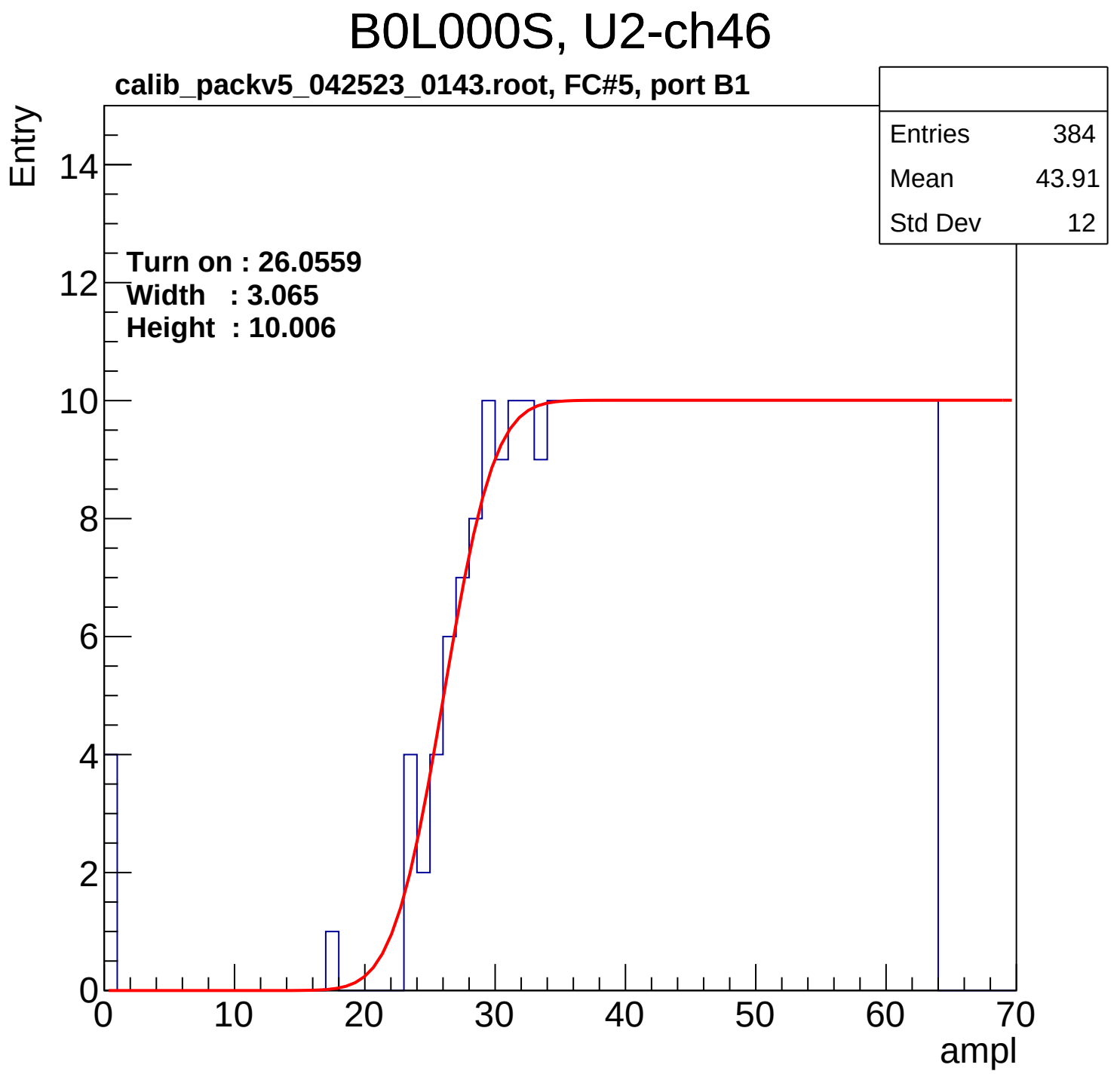
B0L000S, U2-ch46
calib_packv5_042523_0143.root, FC#5, port B1
Entries 384
Mean 43.91
Std Dev 12
Turn on : 26.0559
Width : 3.065
Height : 10.006
Entry
ampl
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8
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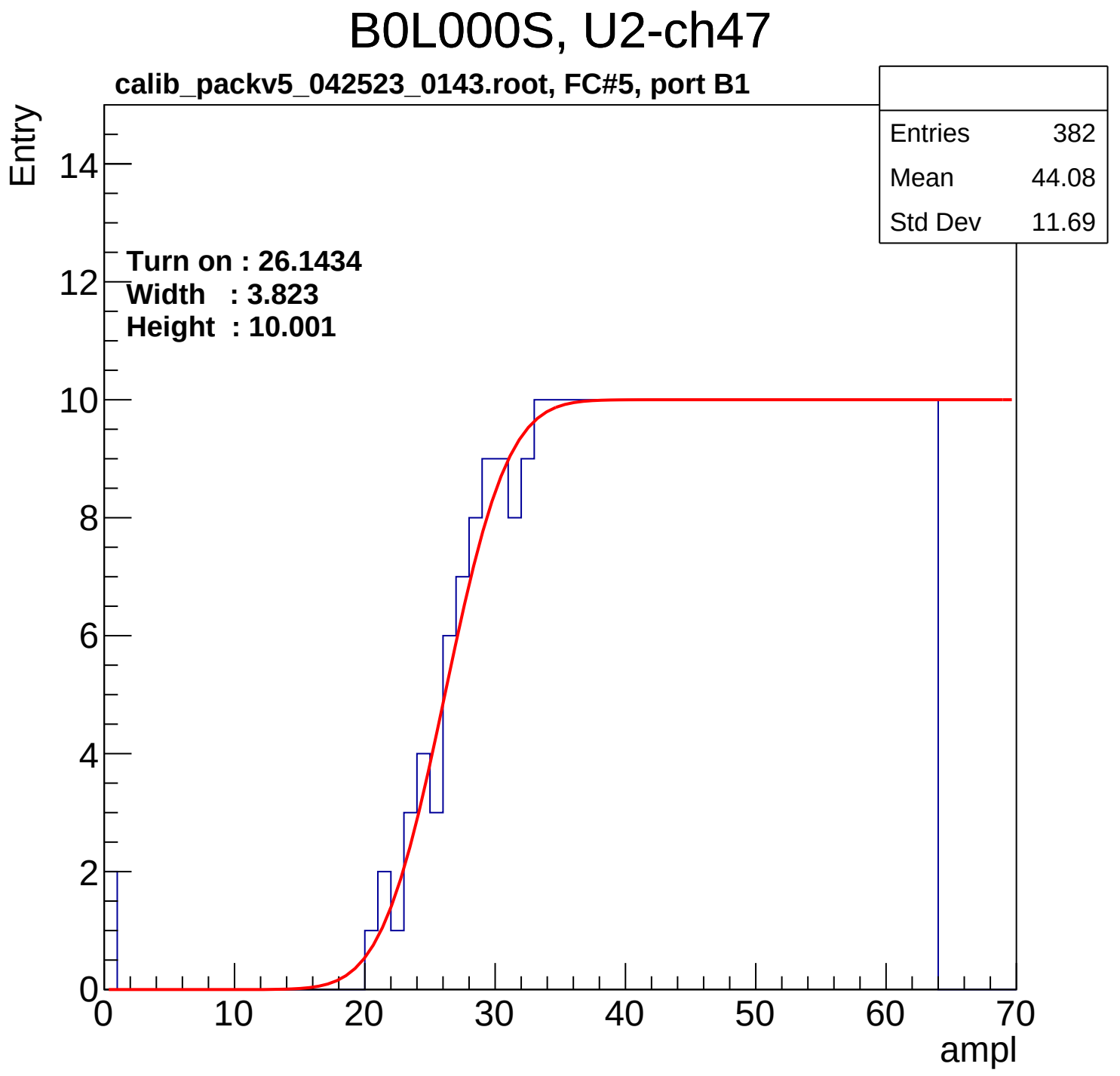
B0L000S, U2-ch47
calib_packv5_042523_0143.root, FC#5, port B1
Entries 382
Mean 44.08
Std Dev 11.69
Turn on : 26.1434
Width : 3.823
Height : 10.001
Entry
ampl
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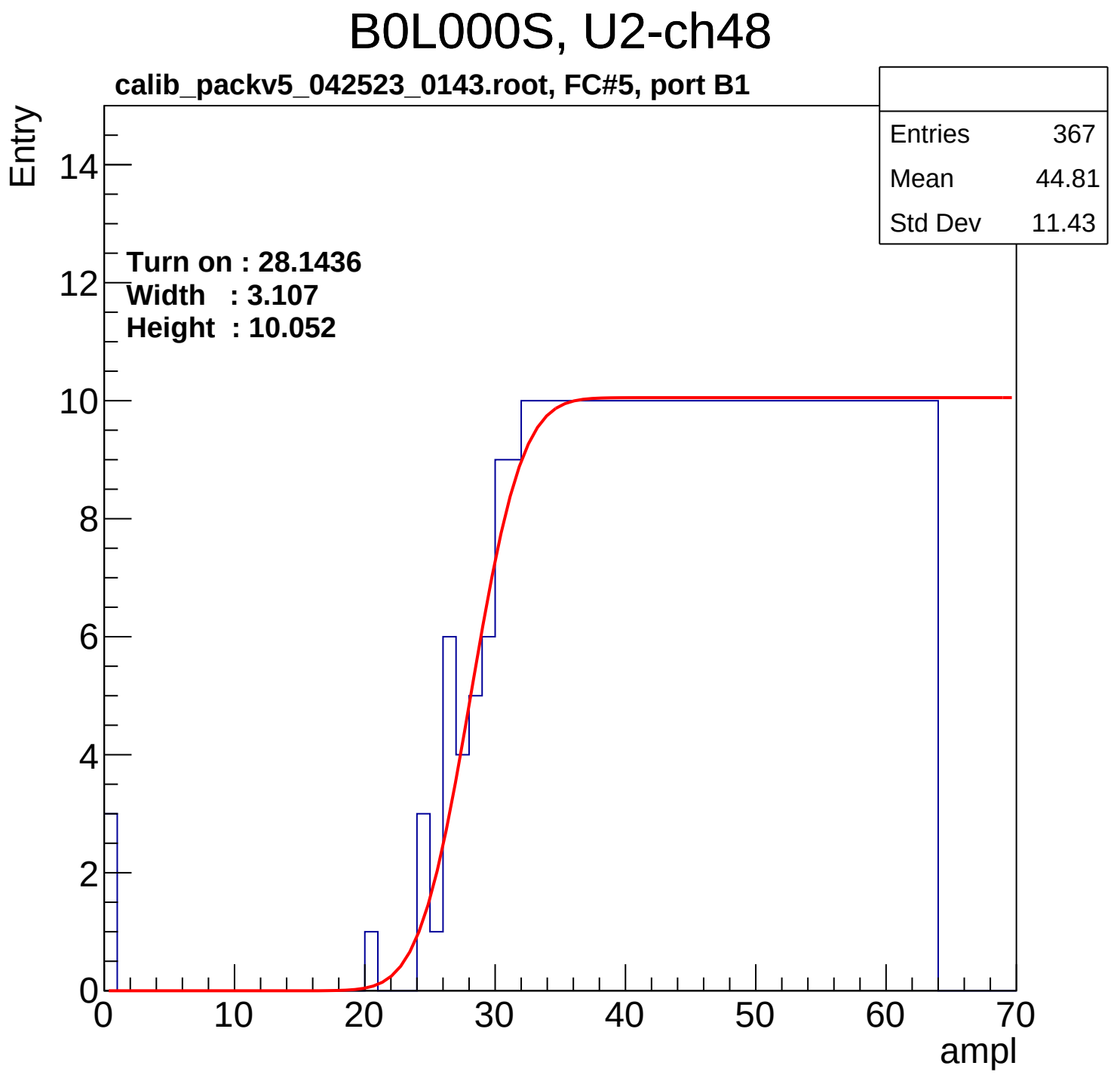
B0L000S, U2-ch48
calib_packv5_042523_0143.root, FC#5, port B1
Entries 367
Mean 44.81
Std Dev 11.43
Turn on : 28.1436
Width : 3.107
Height : 10.052
Entry
ampl
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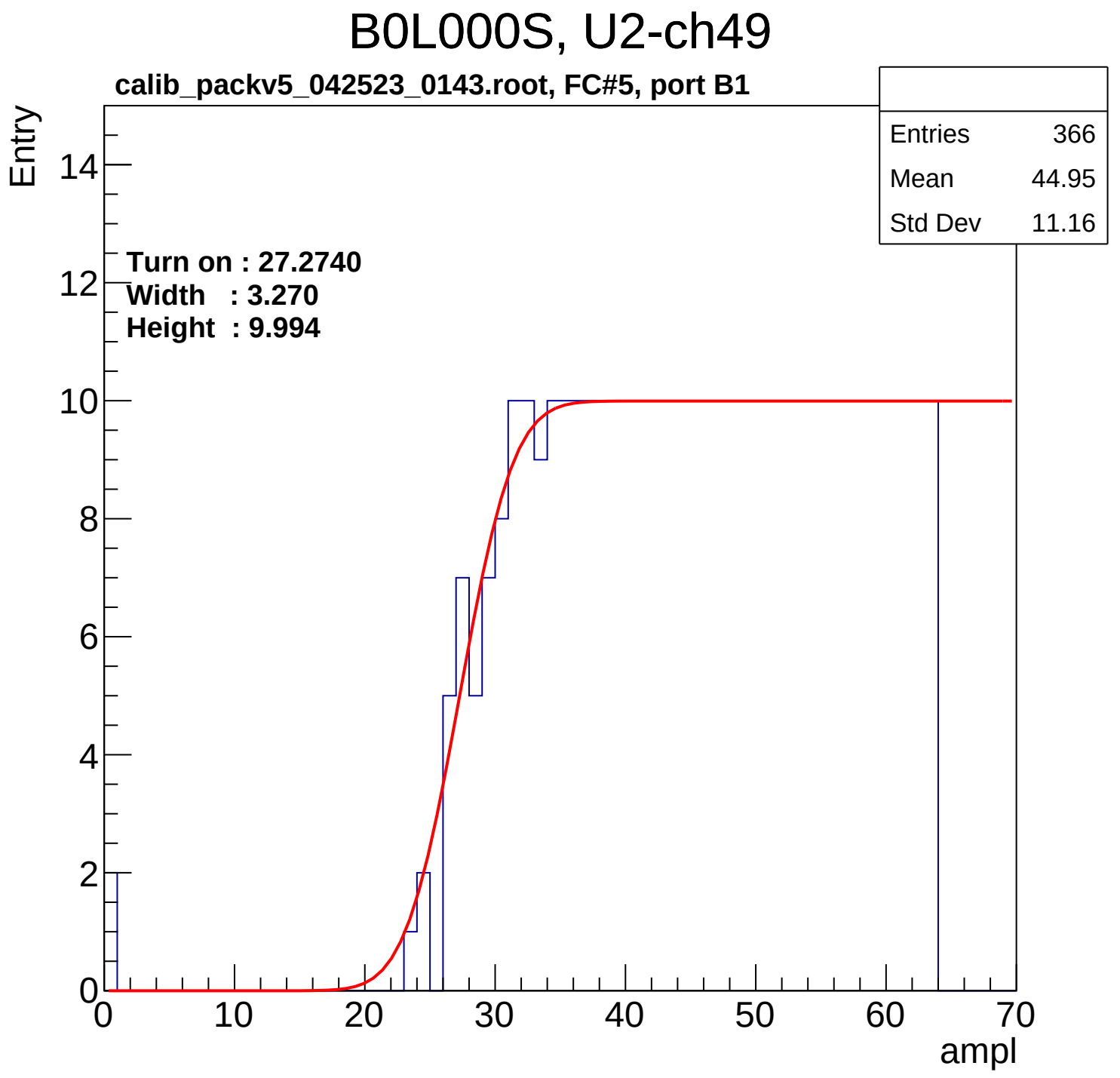
B0L000S, U2-ch49
calib_packv5_042523_0143.root, FC#5, port B1
Entries 366
Mean 44.95
Std Dev 11.16
Turn on : 27.2740
Width : 3.270
Height : 9.994
Entry
ampl
0
2
4
6
8
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12
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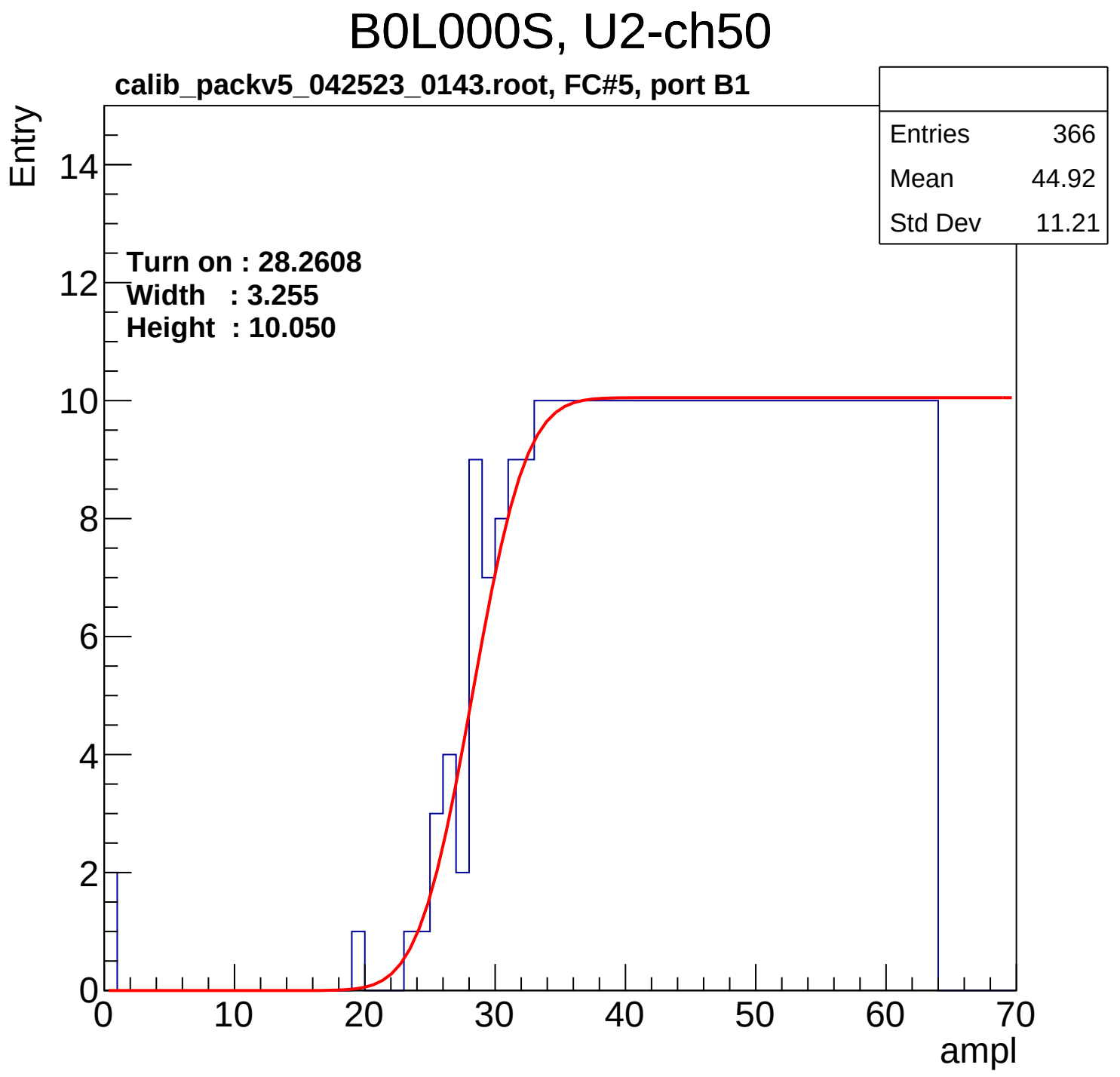
B0L000S, U2-ch50
calib_packv5_042523_0143.root, FC#5, port B1
Entries 366
Mean 44.92
Std Dev 11.21
Turn on : 28.2608
Width : 3.255
Height : 10.050
Entry
ampl
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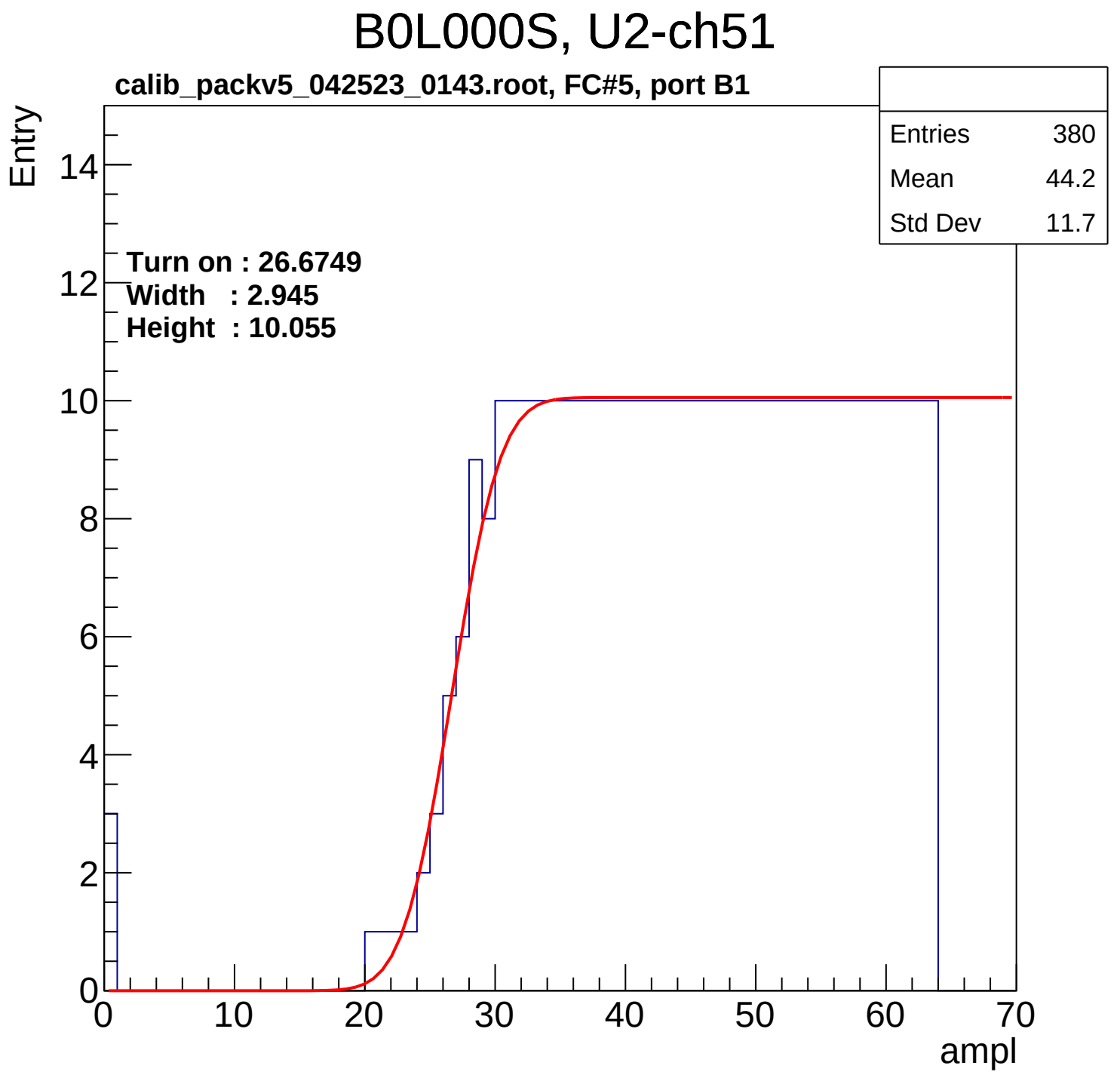
B0L000S, U2-ch51
calib_packv5_042523_0143.root, FC#5, port B1
Entries 380
Mean 44.2
Std Dev 11.7
Turn on : 26.6749
Width : 2.945
Height : 10.055
Entry
ampl
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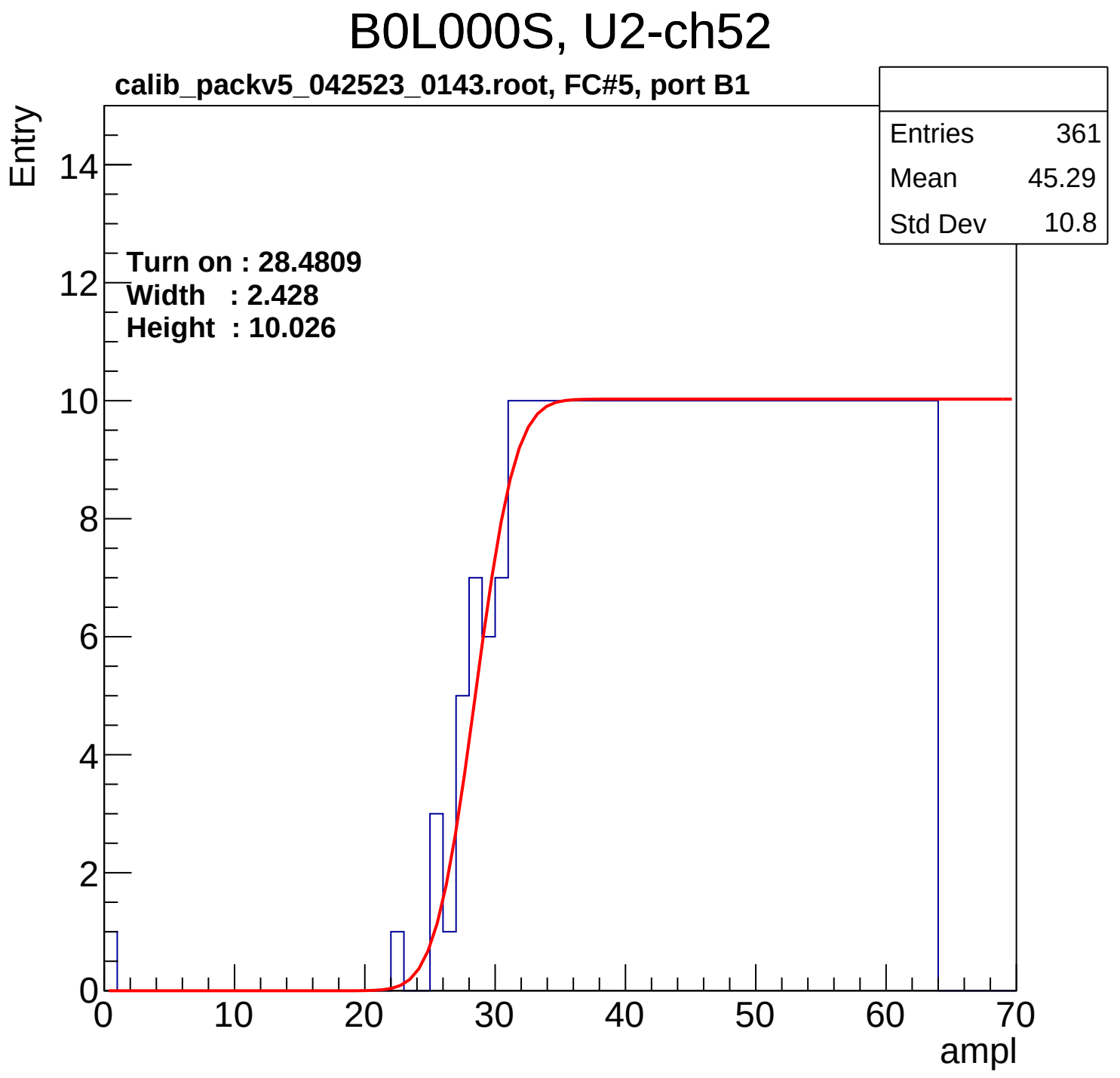
B0L000S, U2-ch52
calib_packv5_042523_0143.root, FC#5, port B1
Entries 361
Mean 45.29
Std Dev 10.8
Turn on : 28.4809
Width : 2.428
Height : 10.026
Entry
ampl
0
2
4
6
8
10
12
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0
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40
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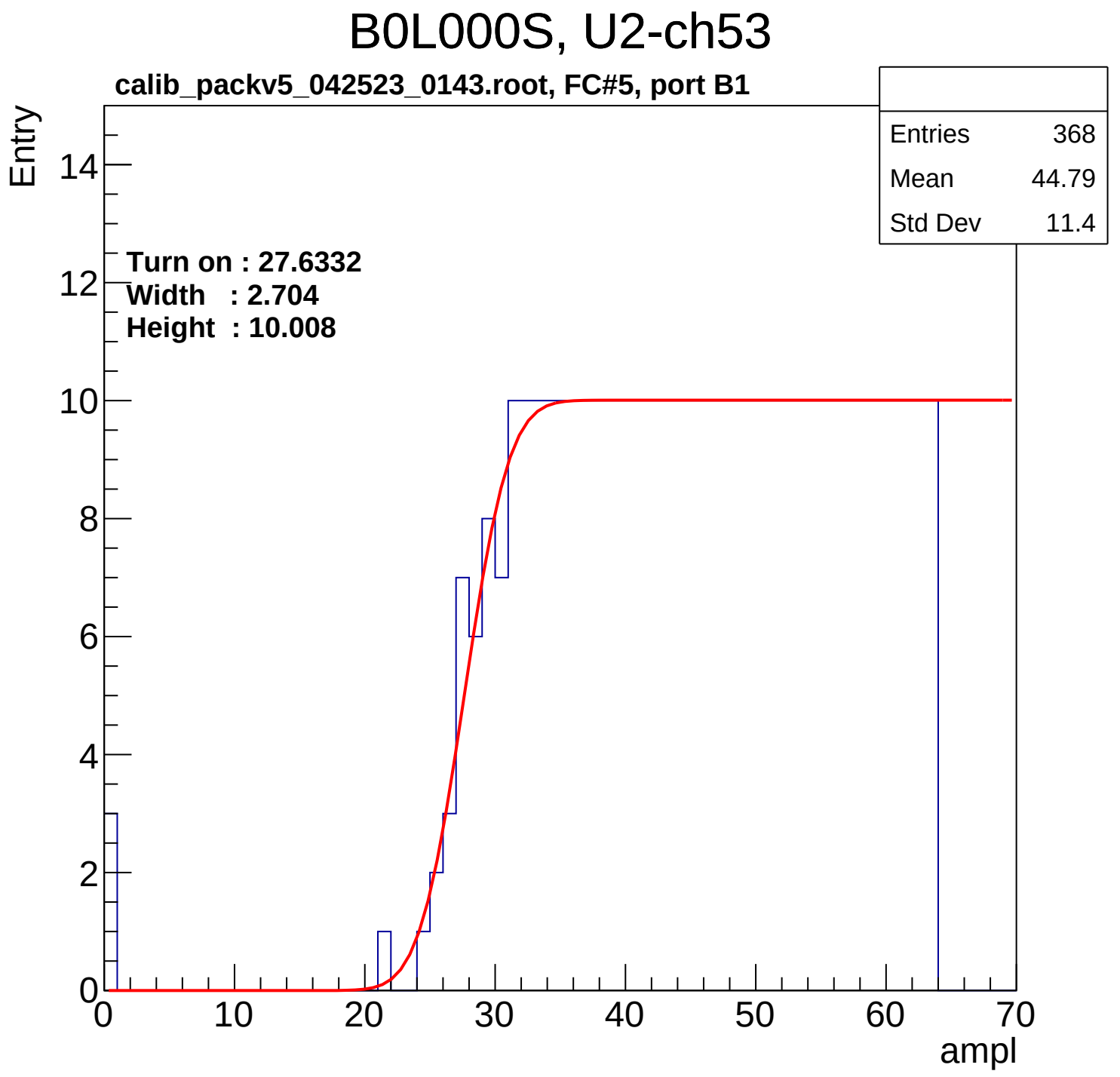
B0L000S, U2-ch53
calib_packv5_042523_0143.root, FC#5, port B1
Entries 368
Mean 44.79
Std Dev 11.4
Turn on : 27.6332
Width : 2.704
Height : 10.008
Entry
ampl
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6
8
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0
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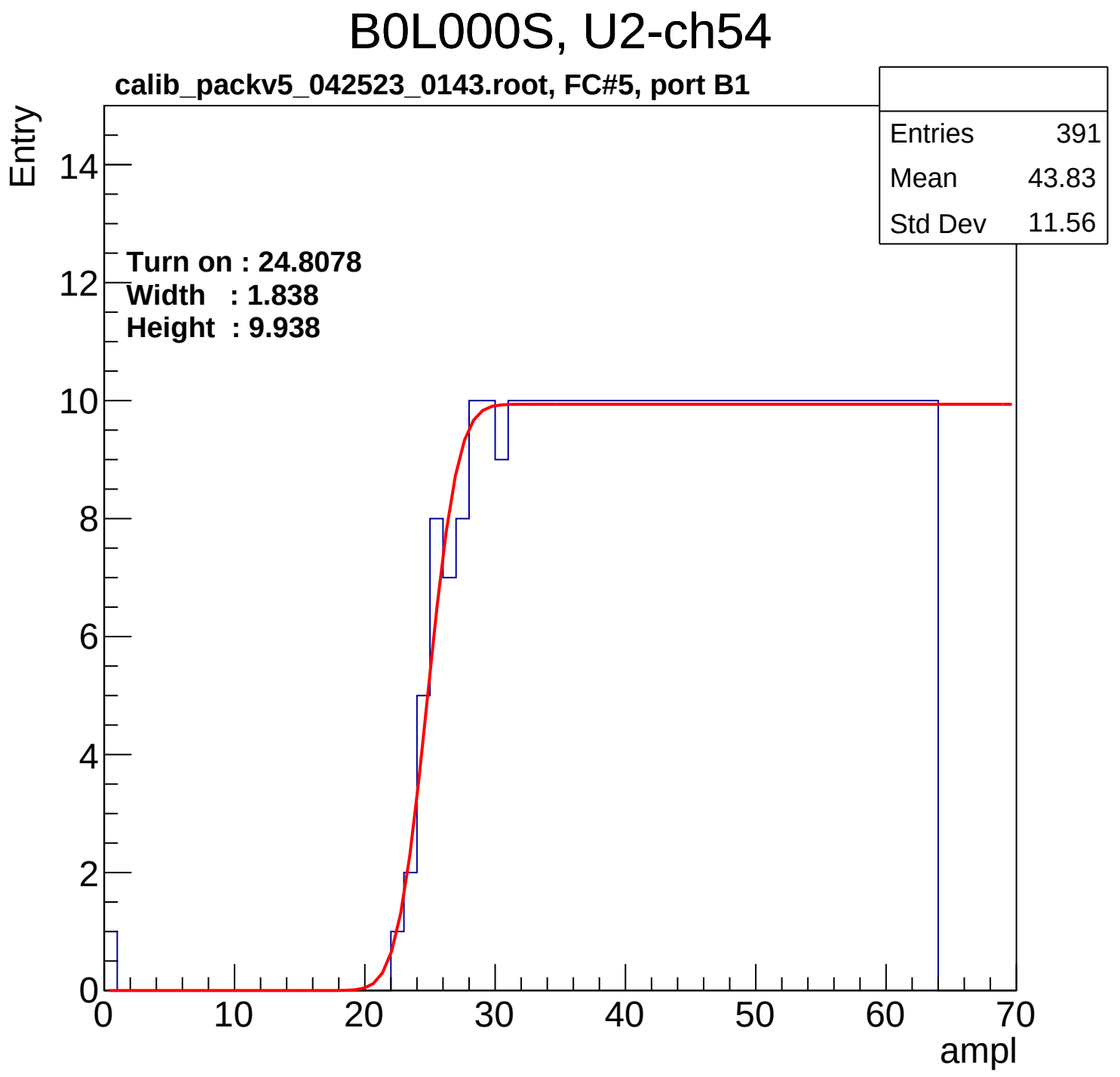
B0L000S, U2-ch54
calib_packv5_042523_0143.root, FC#5, port B1
Entries 391
Mean 43.83
Std Dev 11.56
Turn on : 24.8078
Width : 1.838
Height : 9.938
Entry
ampl
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2
4
6
8
10
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20
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40
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60
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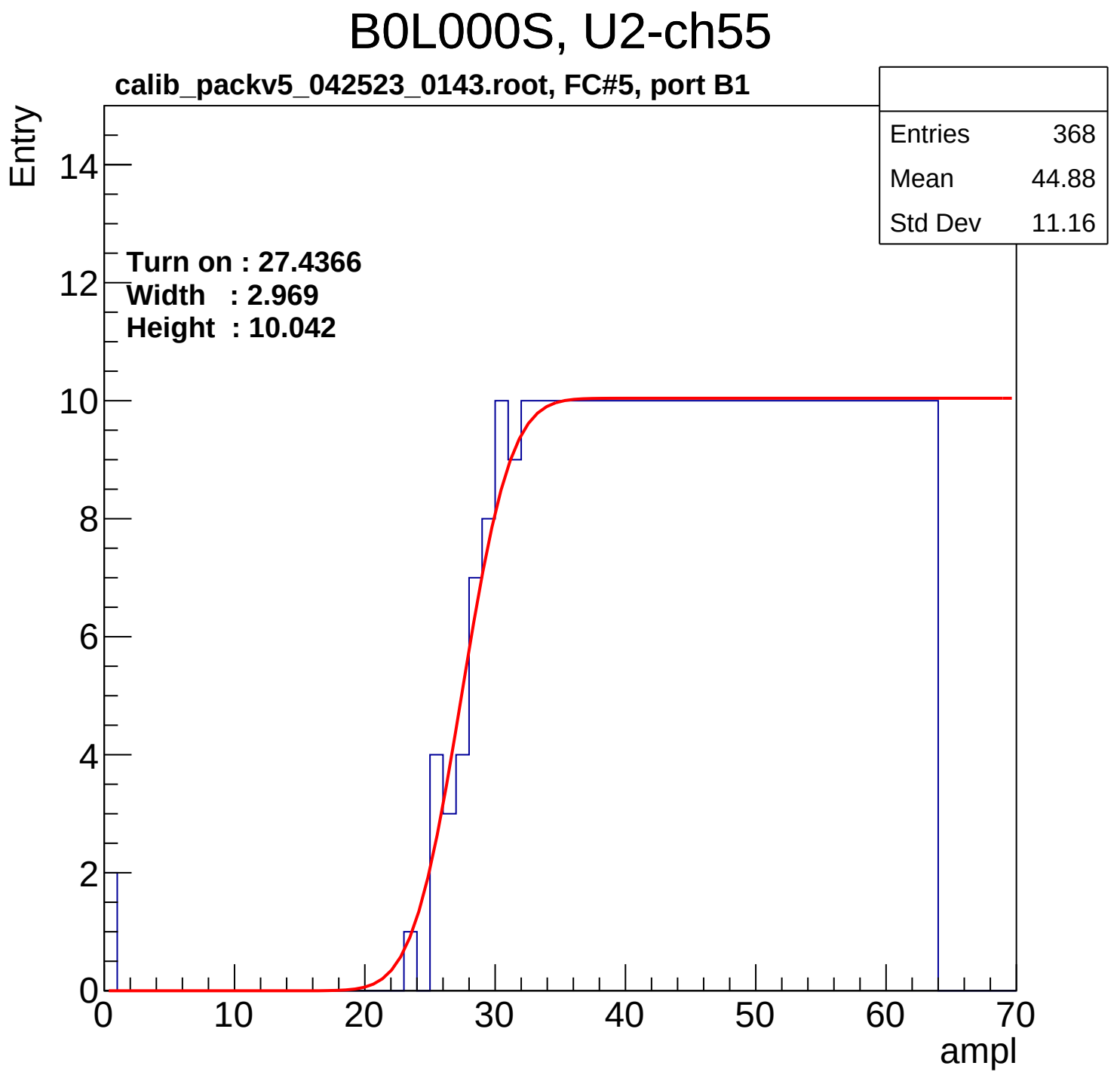
B0L000S, U2-ch55
calib_packv5_042523_0143.root, FC#5, port B1
Entries 368
Mean 44.88
Std Dev 11.16
Turn on : 27.4366
Width : 2.969
Height : 10.042
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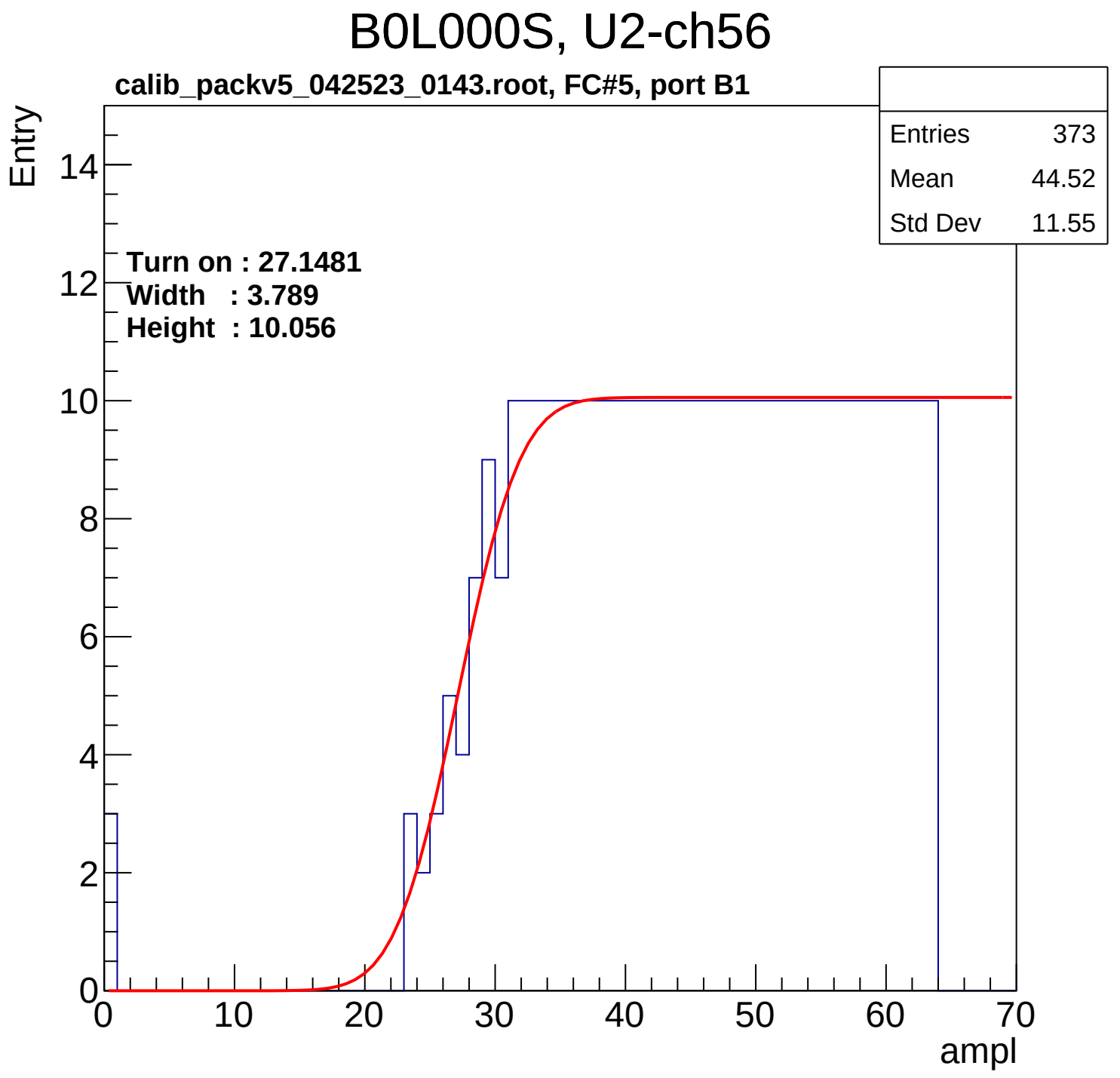
B0L000S, U2-ch56
calib_packv5_042523_0143.root, FC#5, port B1
Entries 373
Mean 44.52
Std Dev 11.55
Turn on : 27.1481
Width : 3.789
Height : 10.056
Entry
ampl
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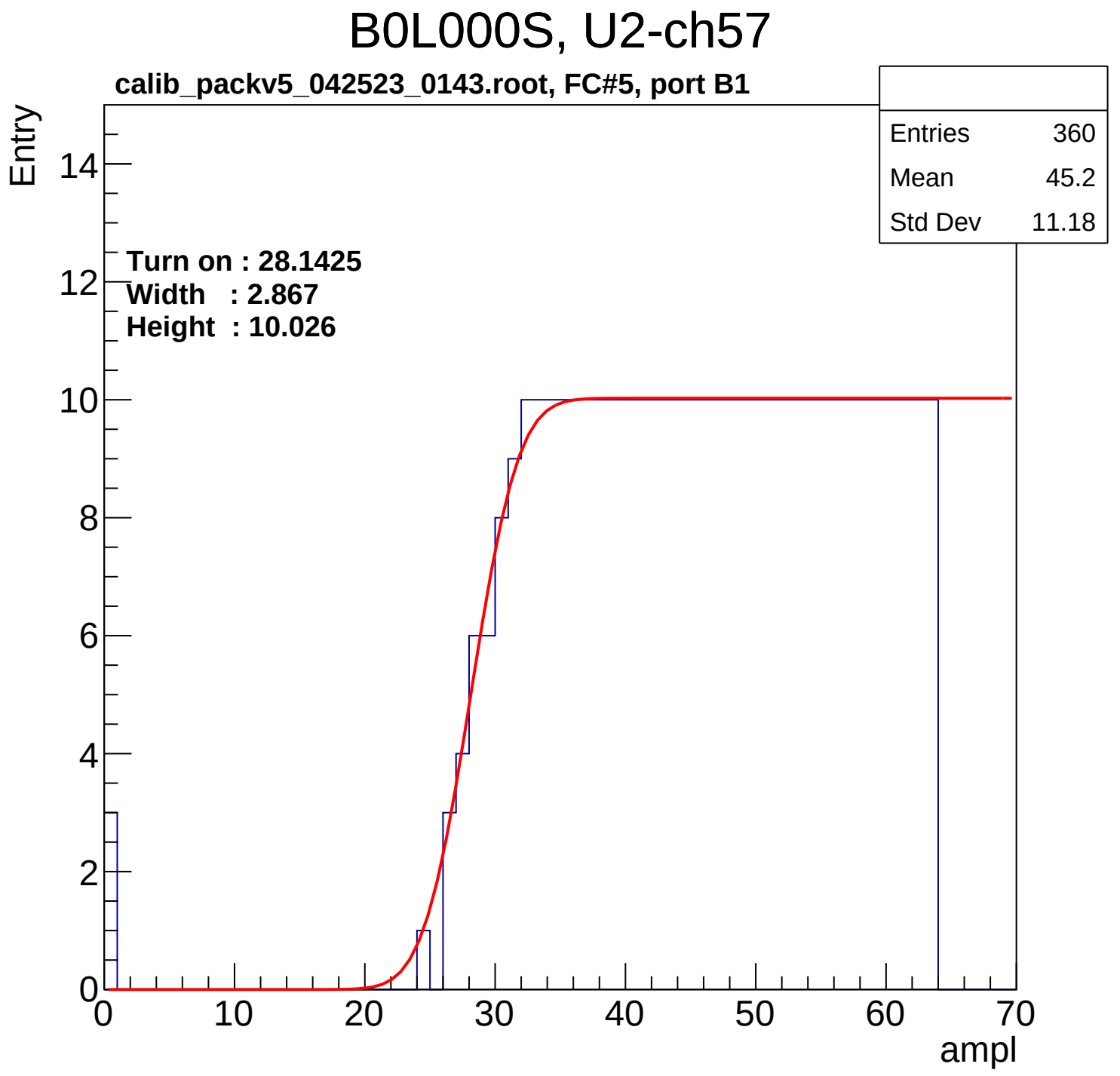
B0L000S, U2-ch57
calib_packv5_042523_0143.root, FC#5, port B1
Entries 360
Mean 45.2
Std Dev 11.18
Turn on : 28.1425
Width : 2.867
Height : 10.026
Entry
ampl
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2
4
6
8
10
12
14
0
10
20
30
40
50
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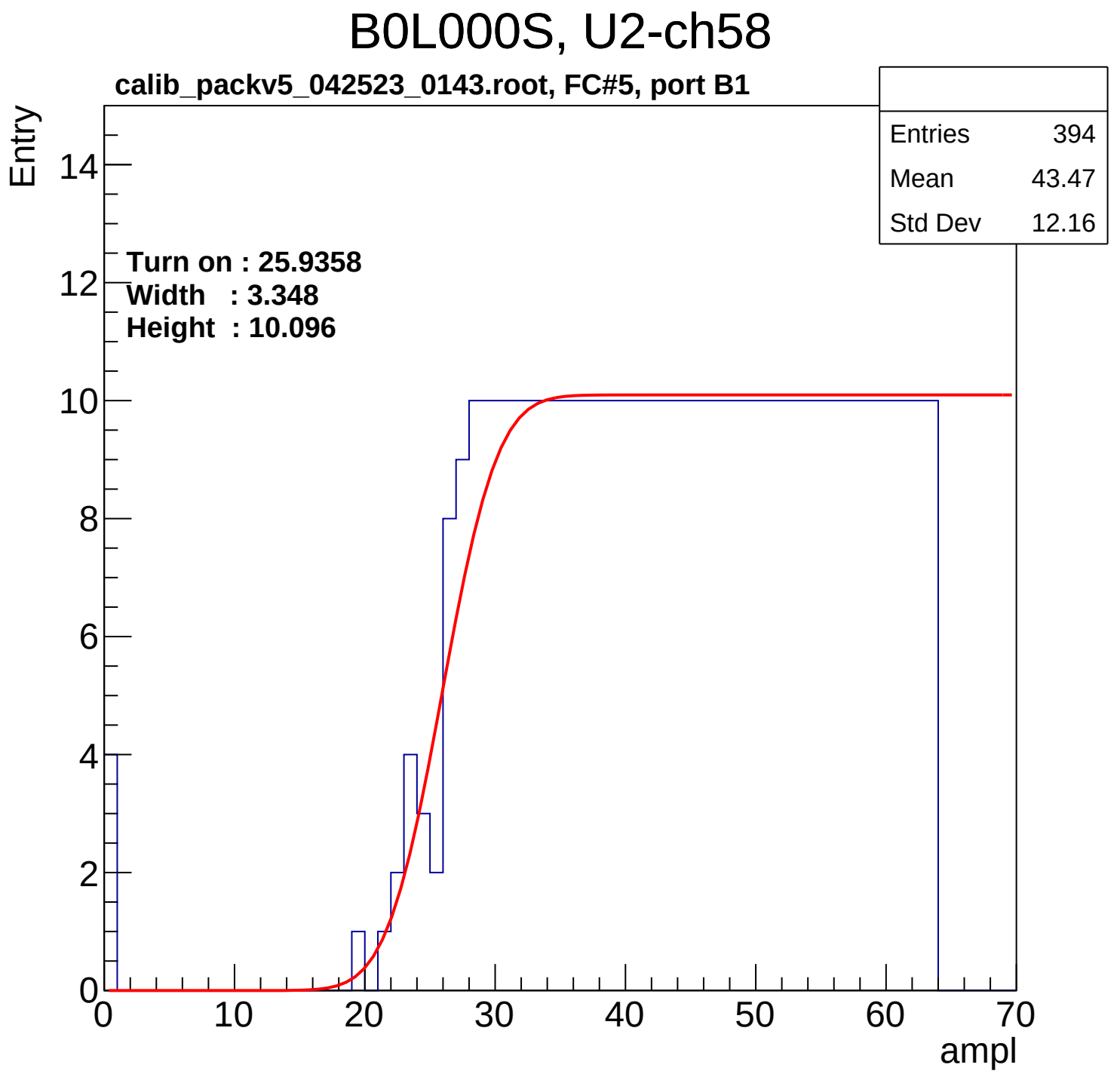
B0L000S, U2-ch58
calib_packv5_042523_0143.root, FC#5, port B1
Entries 394
Mean 43.47
Std Dev 12.16
Turn on : 25.9358
Width : 3.348
Height : 10.096
Entry
ampl
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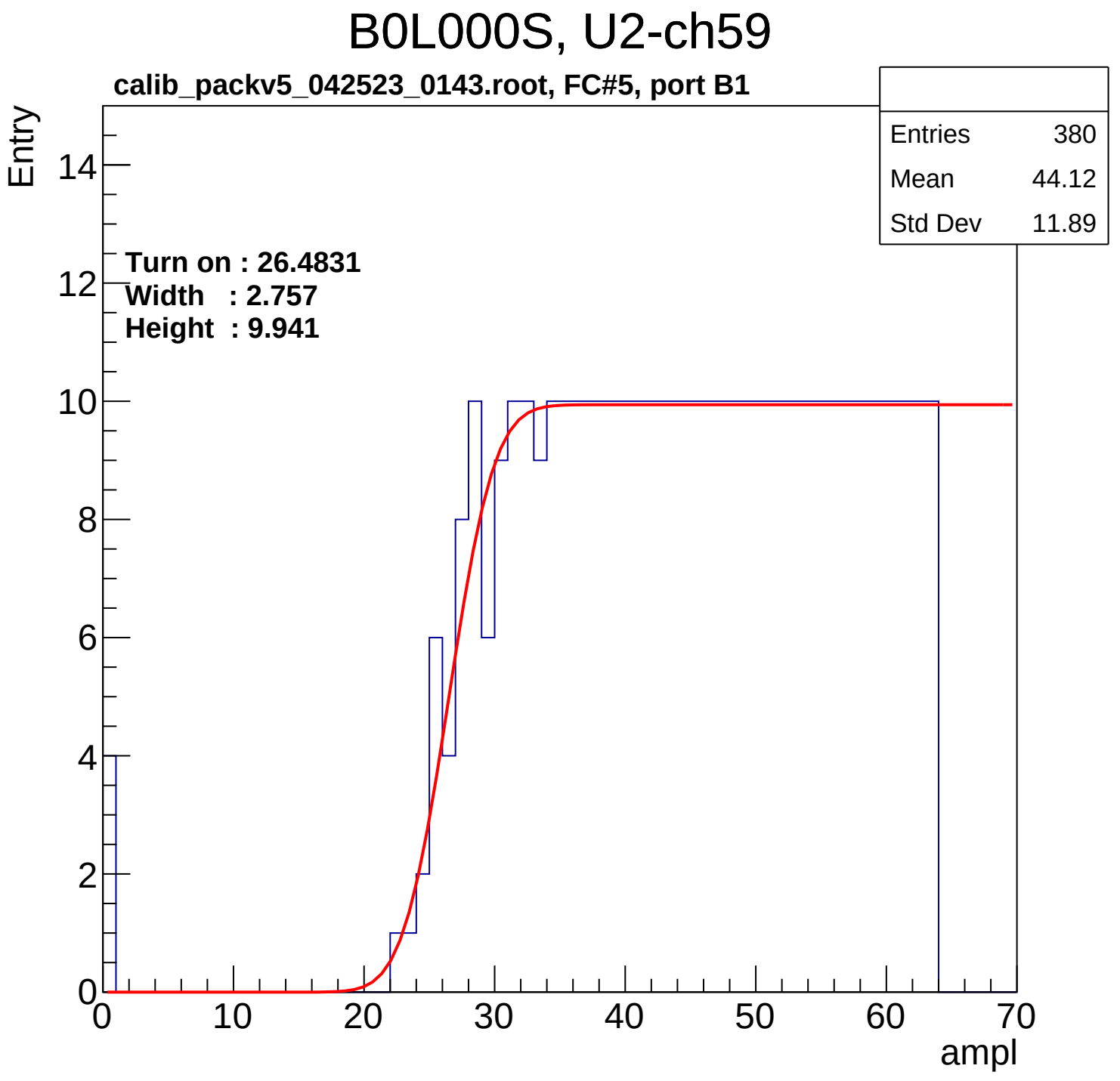
B0L000S, U2-ch59
calib_packv5_042523_0143.root, FC#5, port B1
Entries 380
Mean 44.12
Std Dev 11.89
Turn on : 26.4831
Width : 2.757
Height : 9.941
Entry
ampl
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2
4
6
8
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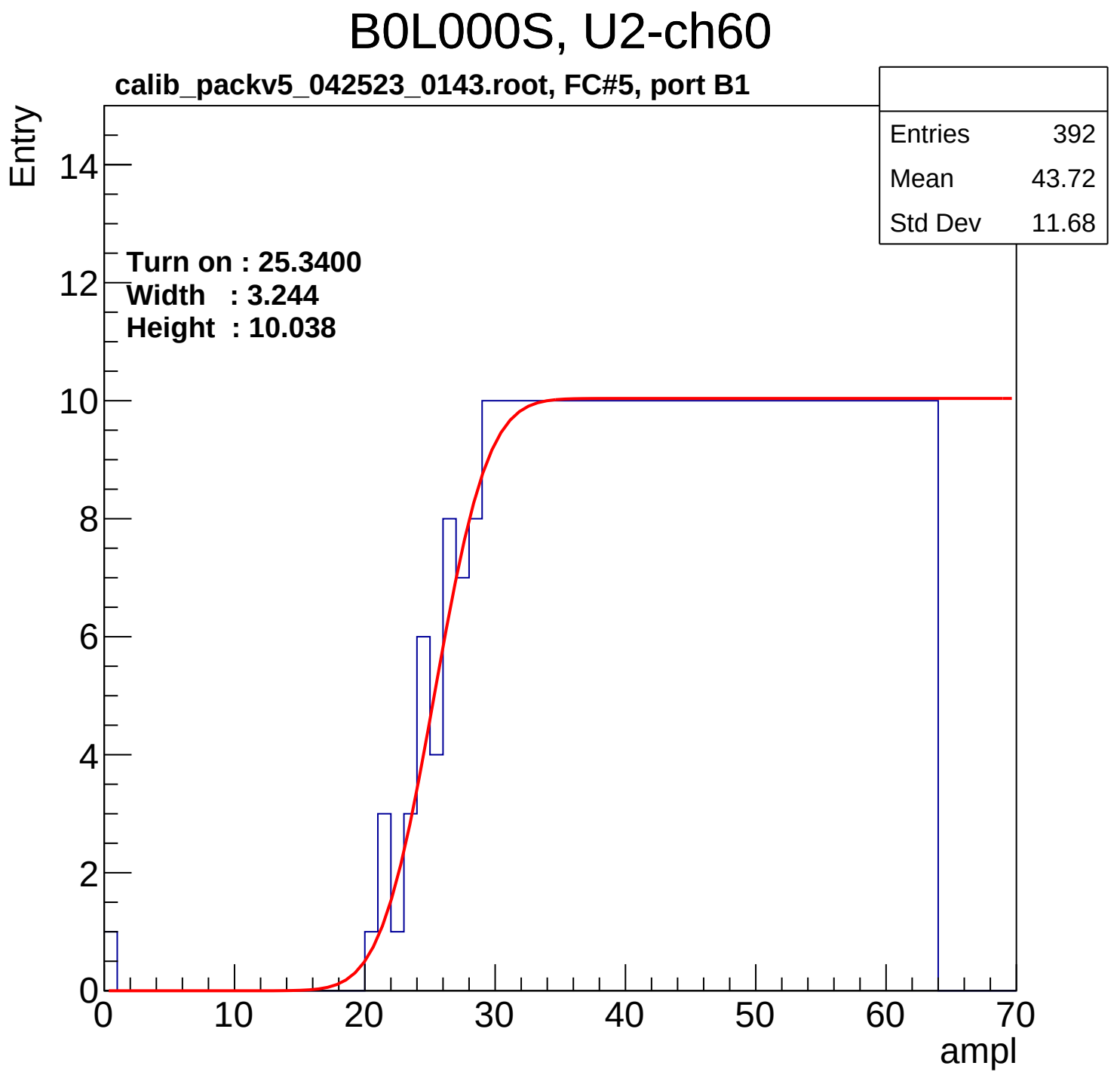
B0L000S, U2-ch60
calib_packv5_042523_0143.root, FC#5, port B1
Entries 392
Mean 43.72
Std Dev 11.68
Turn on : 25.3400
Width : 3.244
Height : 10.038
Entry
ampl
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2
4
6
8
10
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60
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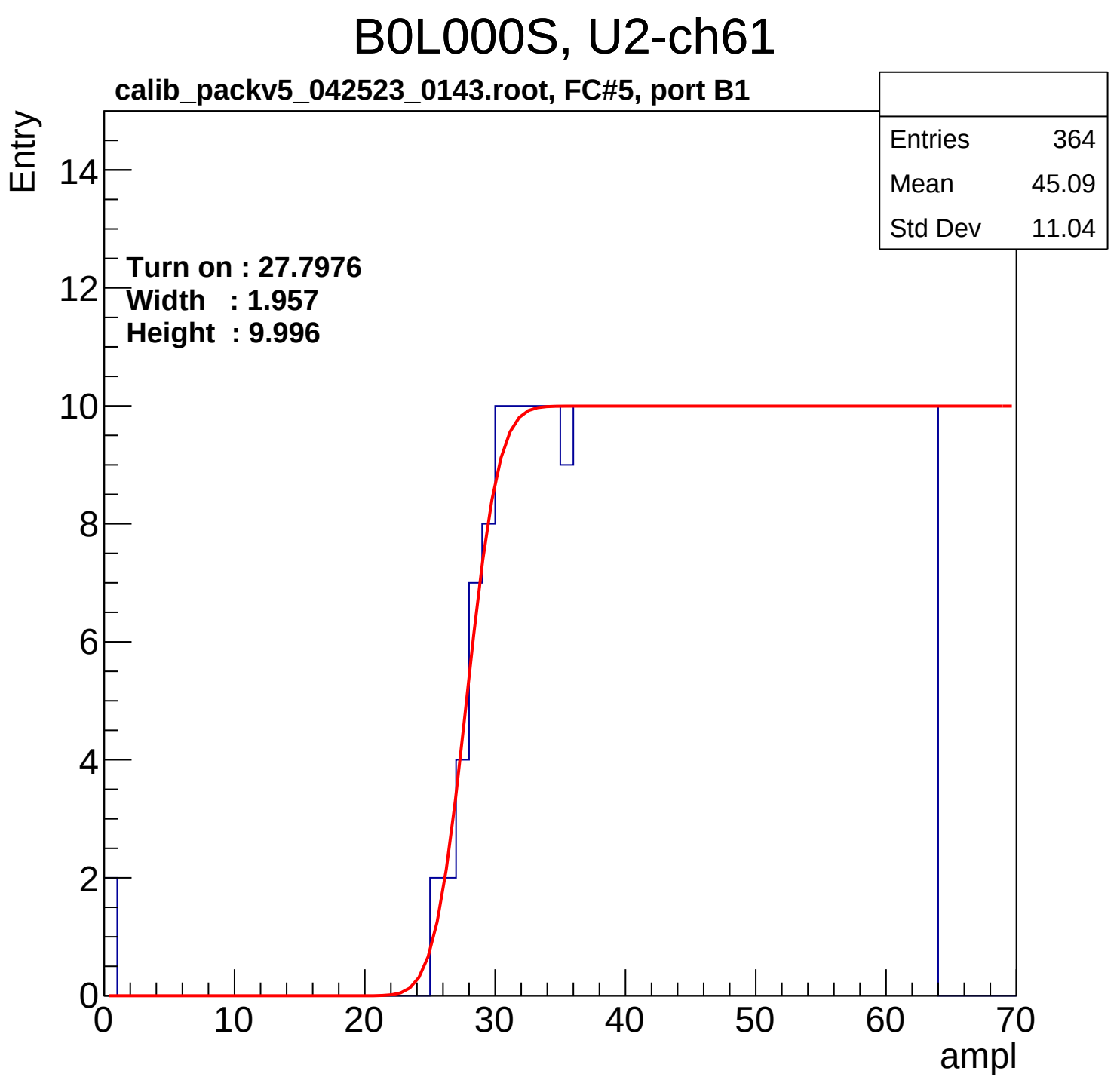
B0L000S, U2-ch61
calib_packv5_042523_0143.root, FC#5, port B1
Entries 364
Mean 45.09
Std Dev 11.04
Turn on : 27.7976
Width : 1.957
Height : 9.996
Entry
ampl
0
2
4
6
8
10
12
14
0
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40
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60
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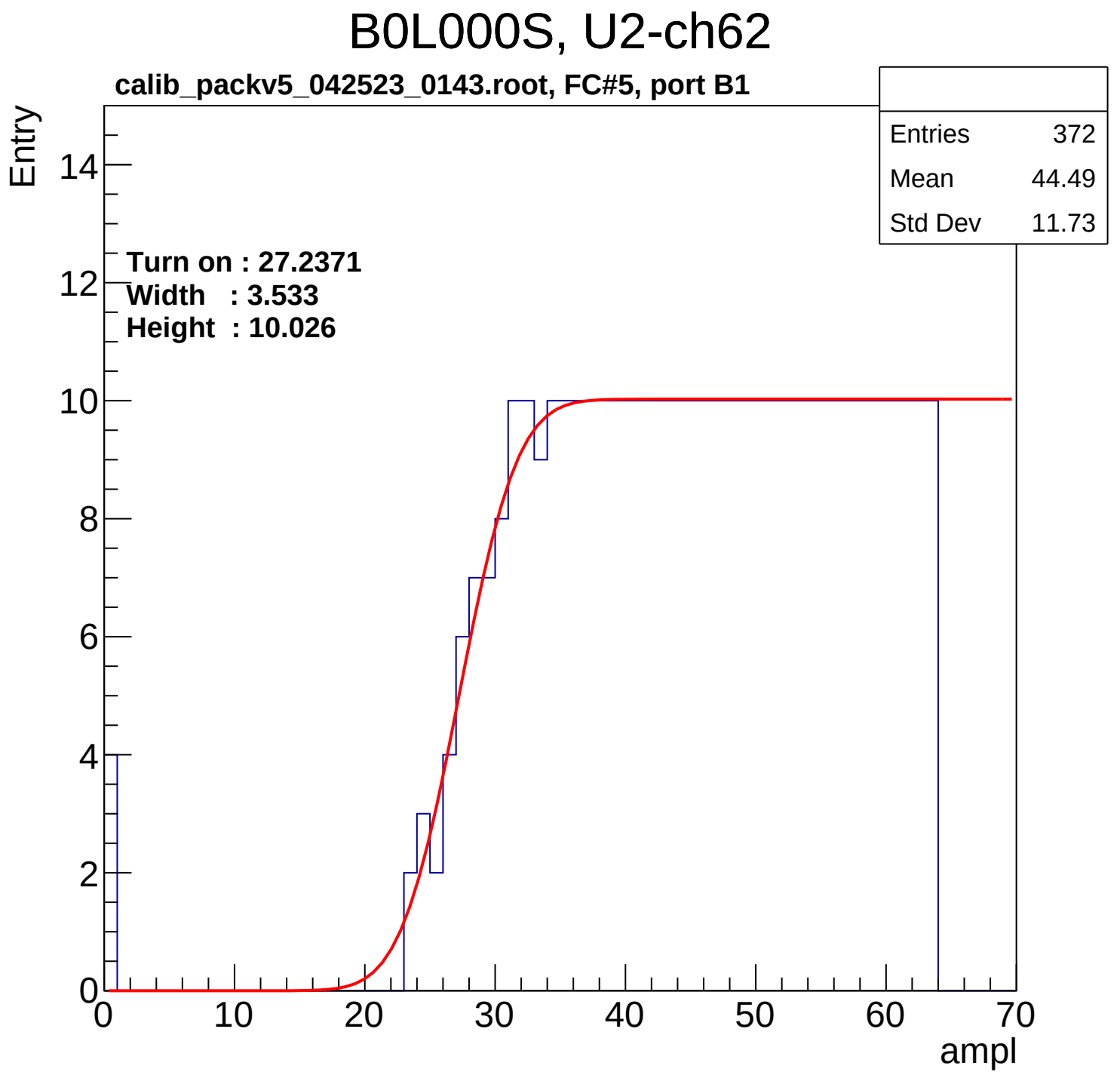
B0L000S, U2-ch62
calib_packv5_042523_0143.root, FC#5, port B1
Entries 372
Mean 44.49
Std Dev 11.73
Turn on : 27.2371
Width : 3.533
Height : 10.026
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
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60
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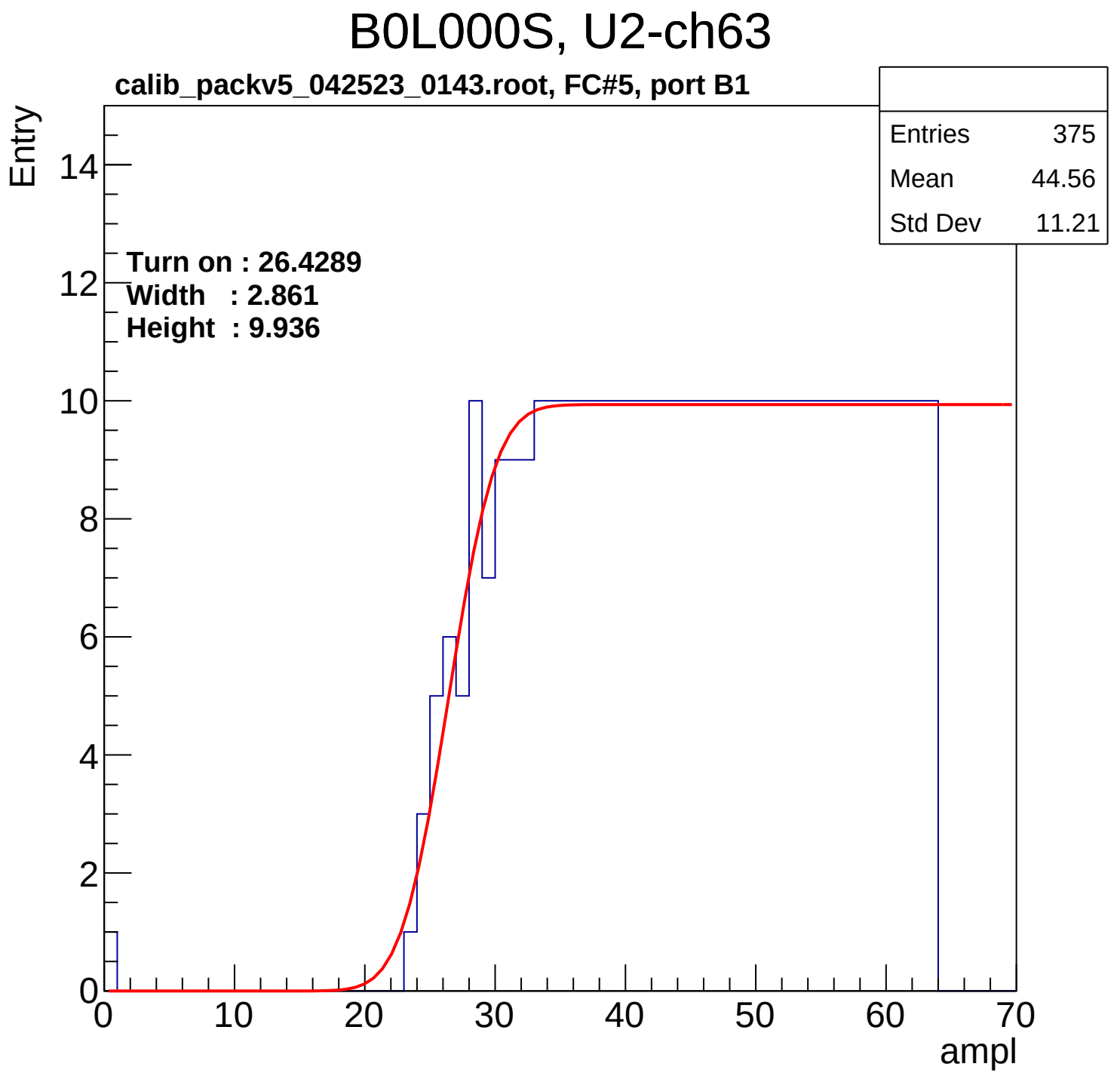
B0L000S, U2-ch63
calib_packv5_042523_0143.root, FC#5, port B1
Entries 375
Mean 44.56
Std Dev 11.21
Turn on : 26.4289
Width : 2.861
Height : 9.936
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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40
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60
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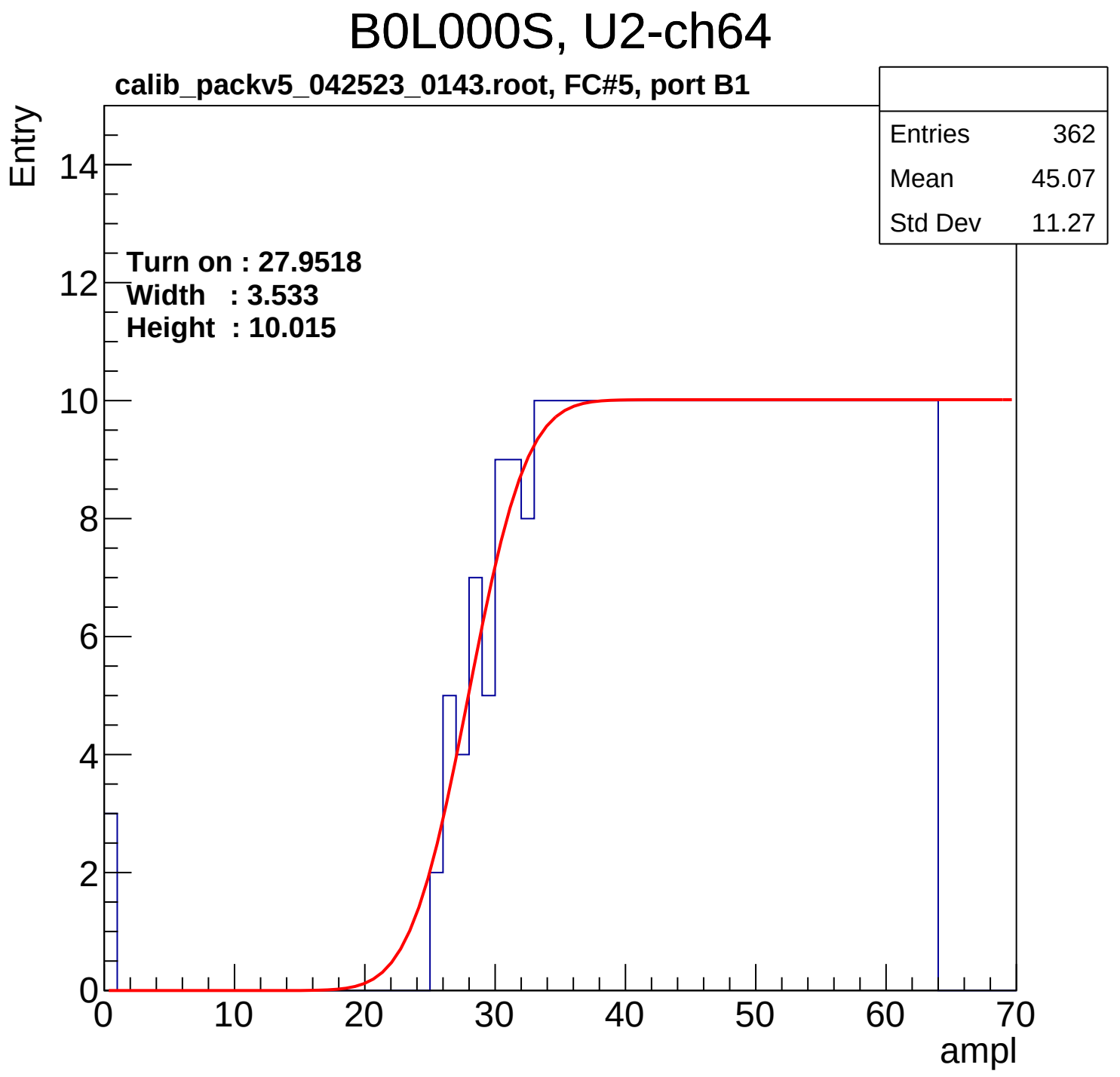
B0L000S, U2-ch64
calib_packv5_042523_0143.root, FC#5, port B1
Entries 362
Mean 45.07
Std Dev 11.27
Turn on : 27.9518
Width : 3.533
Height : 10.015
Entry
ampl
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2
4
6
8
10
12
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0
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60
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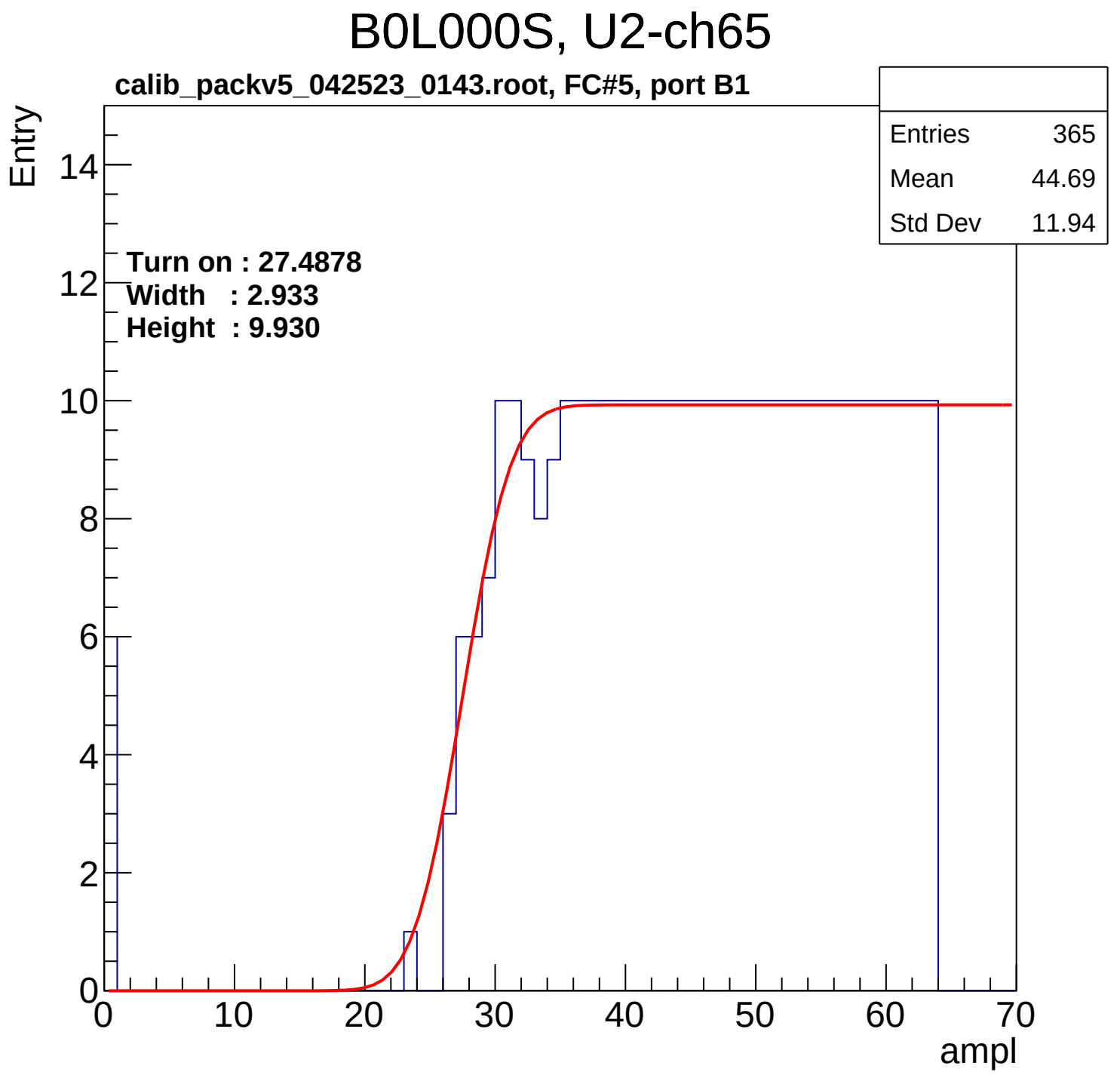
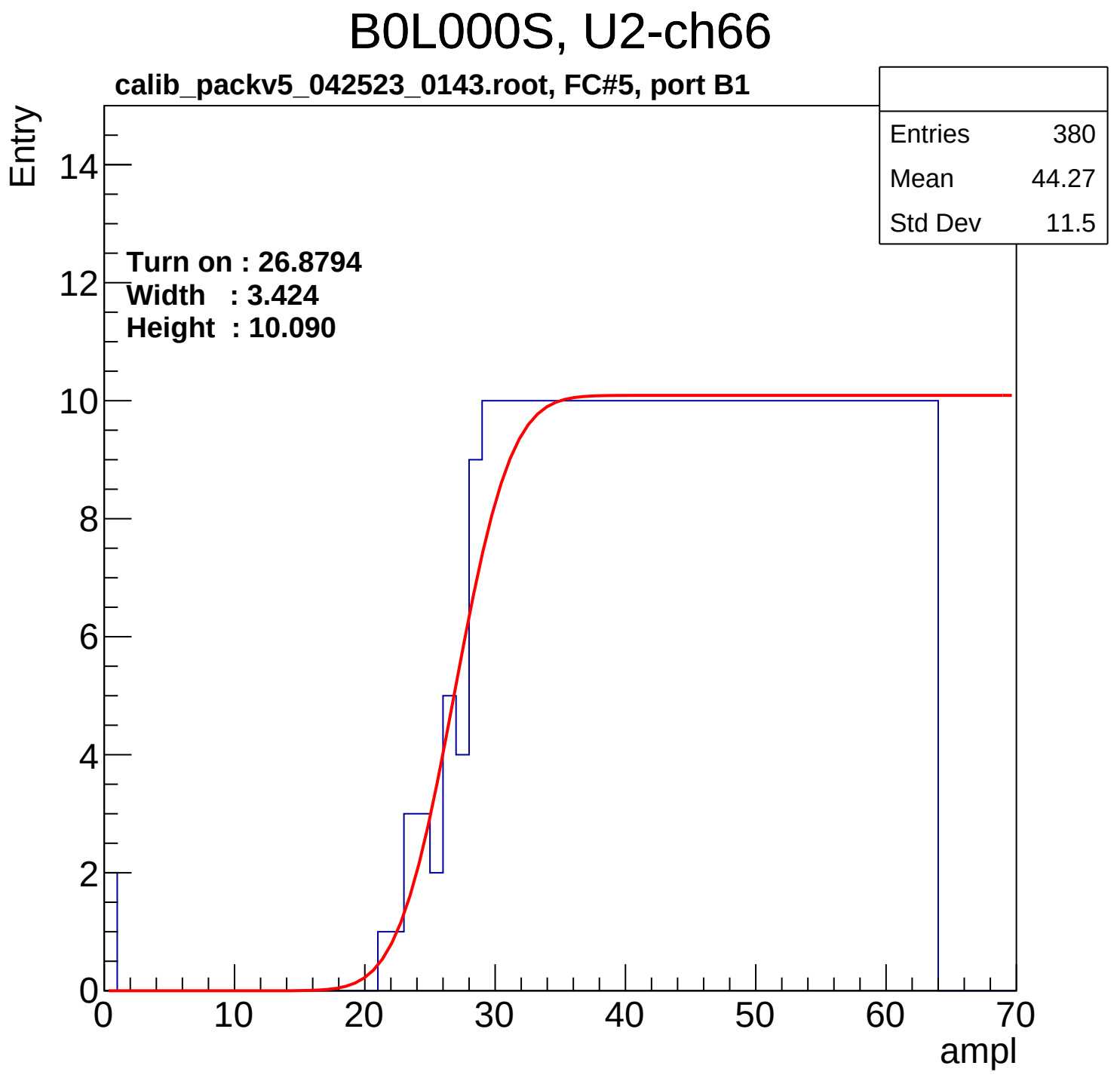

B0L000S, U2-ch65
calib_packv5_042523_0143.root, FC#5, port B1
Entries 365
Mean 44.69
Std Dev 11.94
Turn on : 27.4878
Width : 2.933
Height : 9.930
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L000S, U2-ch66
calib_packv5_042523_0143.root, FC#5, port B1
Entries 380
Mean 44.27
Std Dev 11.5
Turn on : 26.8794
Width : 3.424
Height : 10.090
Entry
ampl
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4
6
8
10
12
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0
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20
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40
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60
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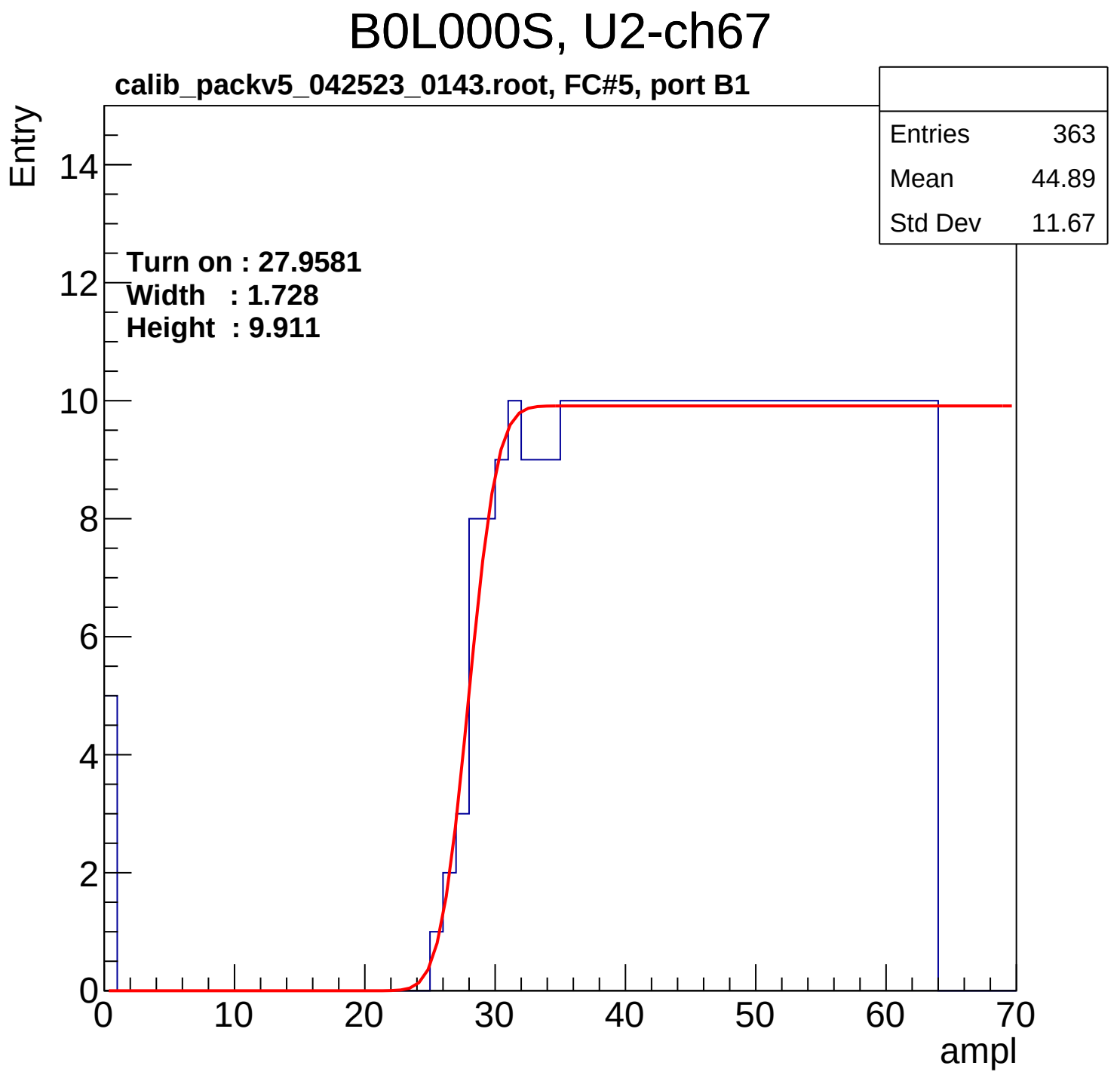
B0L000S, U2-ch67
calib_packv5_042523_0143.root, FC#5, port B1
Entries 363
Mean 44.89
Std Dev 11.67
Turn on : 27.9581
Width : 1.728
Height : 9.911
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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40
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60
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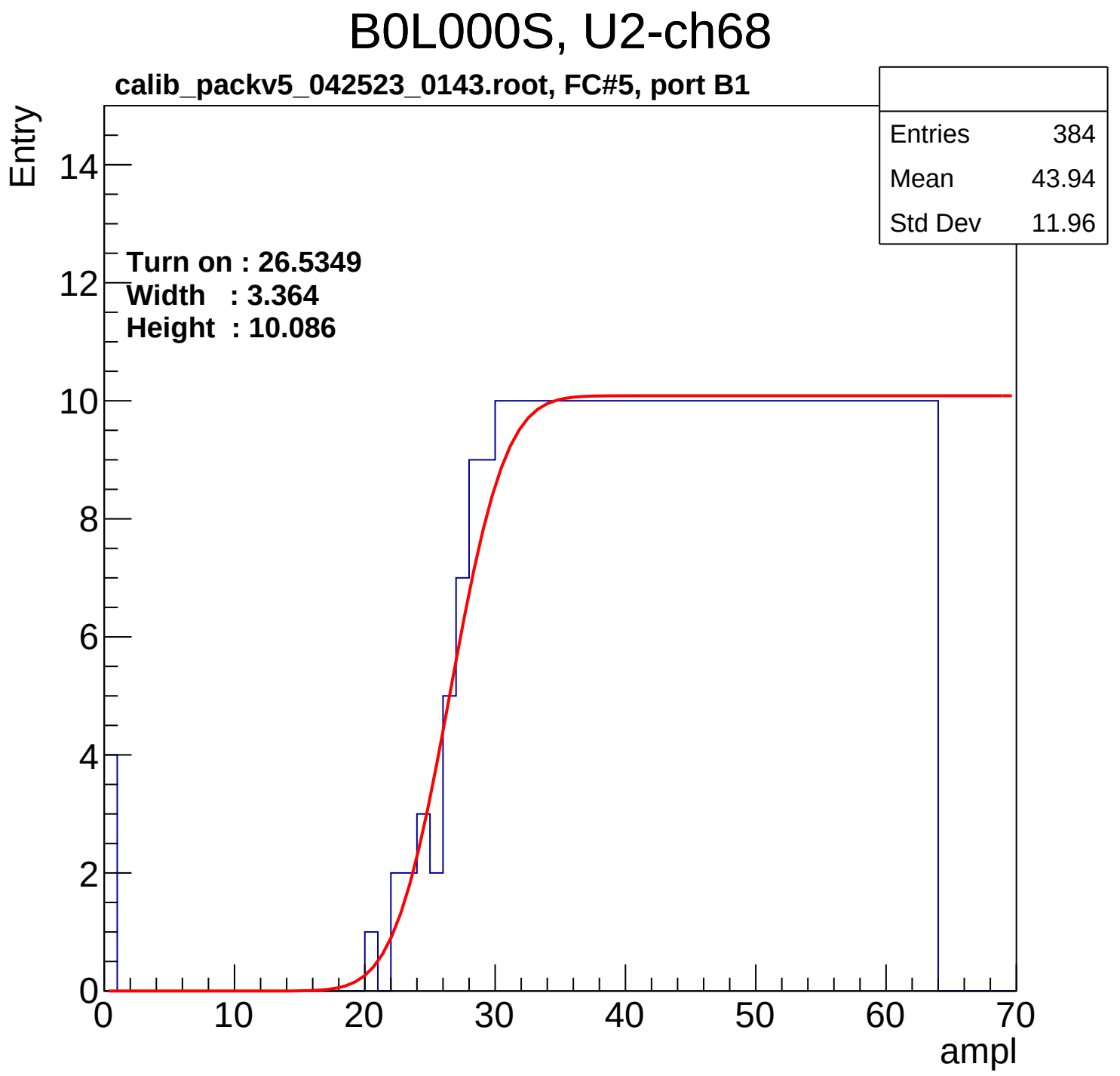
B0L000S, U2-ch68
calib_packv5_042523_0143.root, FC#5, port B1
Entries 384
Mean 43.94
Std Dev 11.96
Turn on : 26.5349
Width : 3.364
Height : 10.086
Entry
ampl
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6
8
10
12
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0
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20
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40
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60
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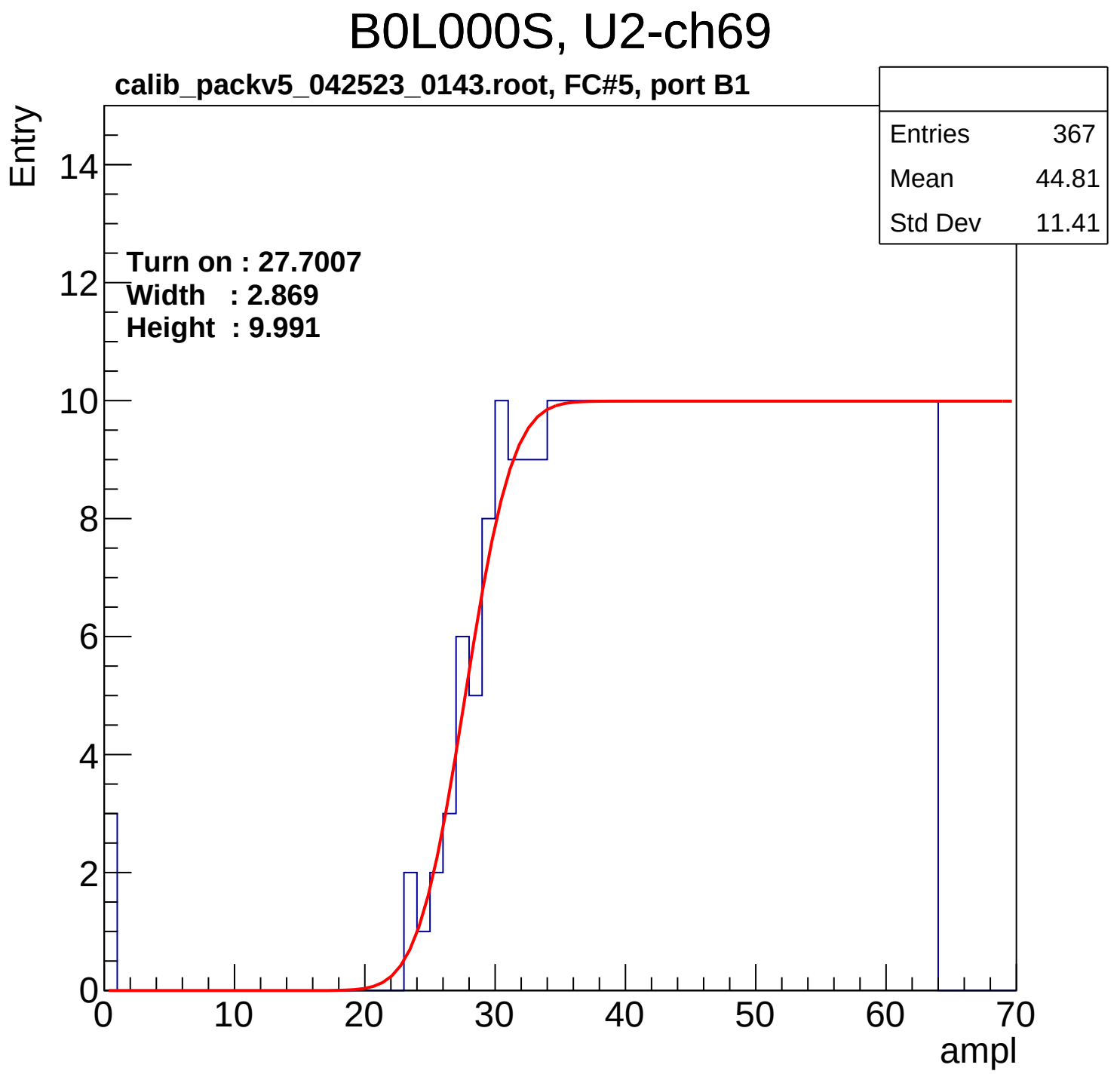
B0L000S, U2-ch69
calib_packv5_042523_0143.root, FC#5, port B1
Entries 367
Mean 44.81
Std Dev 11.41
Turn on : 27.7007
Width : 2.869
Height : 9.991
Entry
ampl
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2
4
6
8
10
12
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0
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60
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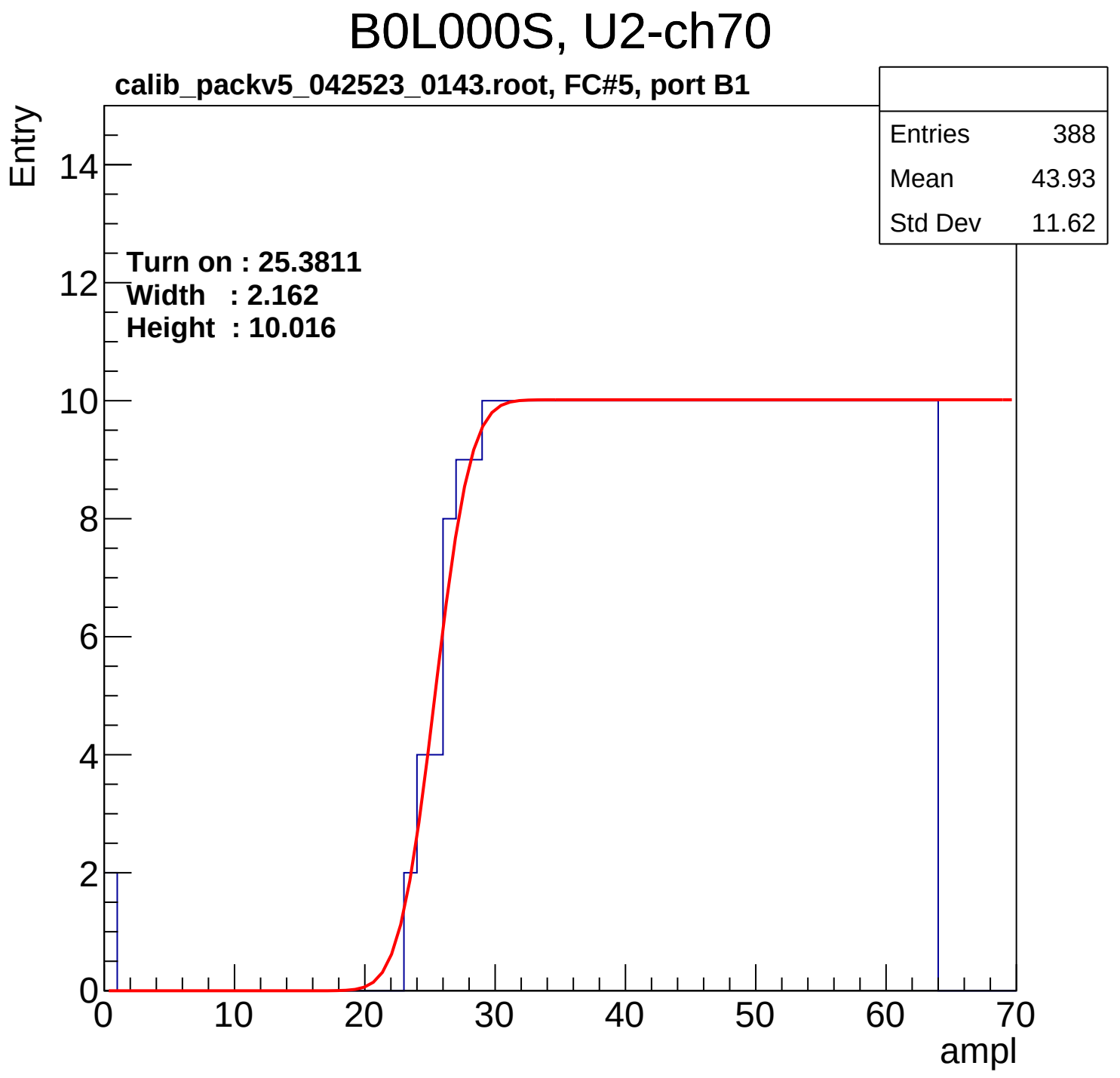
B0L000S, U2-ch70
calib_packv5_042523_0143.root, FC#5, port B1
Entries 388
Mean 43.93
Std Dev 11.62
Turn on : 25.3811
Width : 2.162
Height : 10.016
Entry
ampl
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2
4
6
8
10
12
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60
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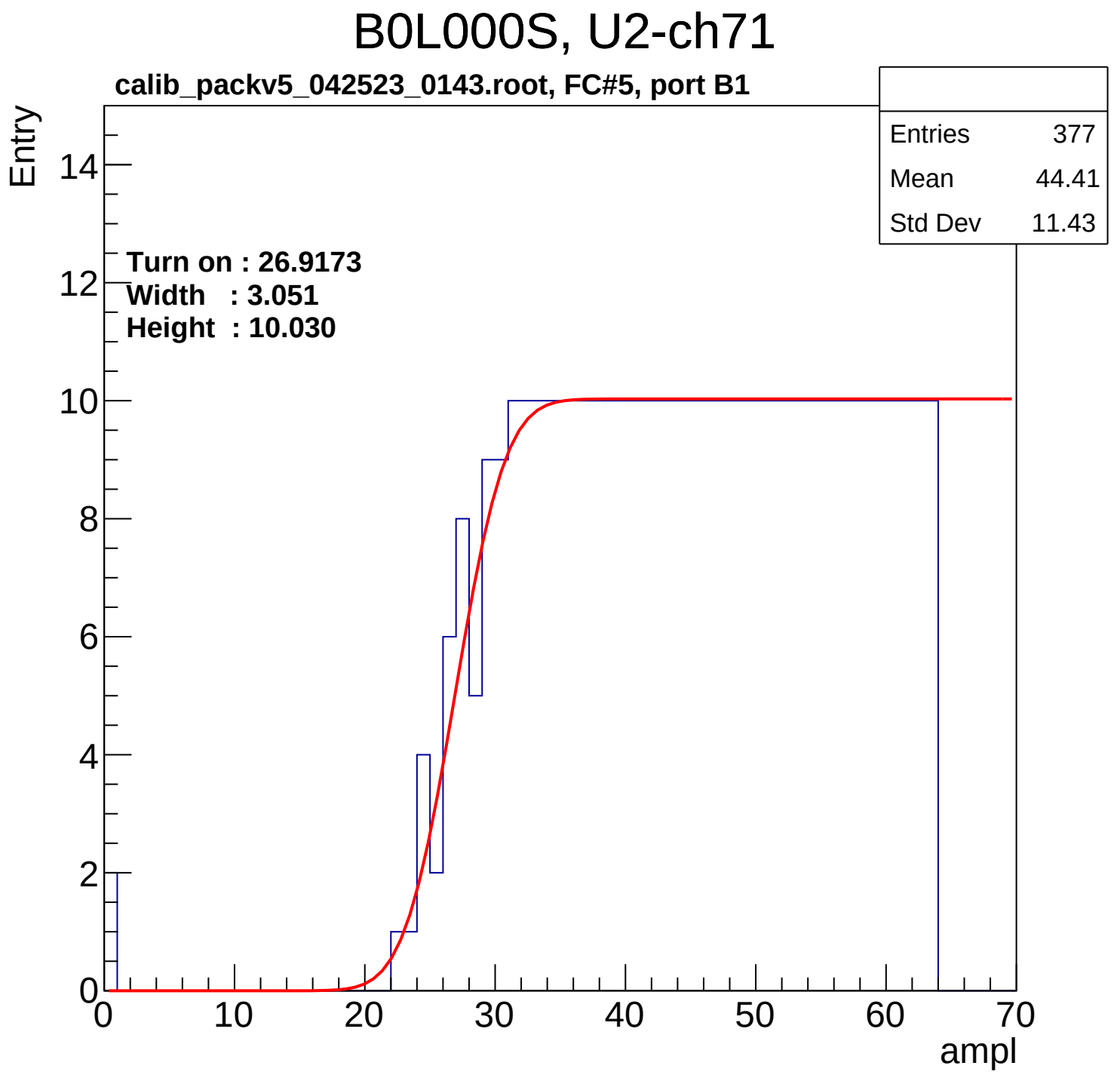
B0L000S, U2-ch71
calib_packv5_042523_0143.root, FC#5, port B1
Entries 377
Mean 44.41
Std Dev 11.43
Turn on : 26.9173
Width : 3.051
Height : 10.030
Entry
ampl
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2
4
6
8
10
12
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0
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20
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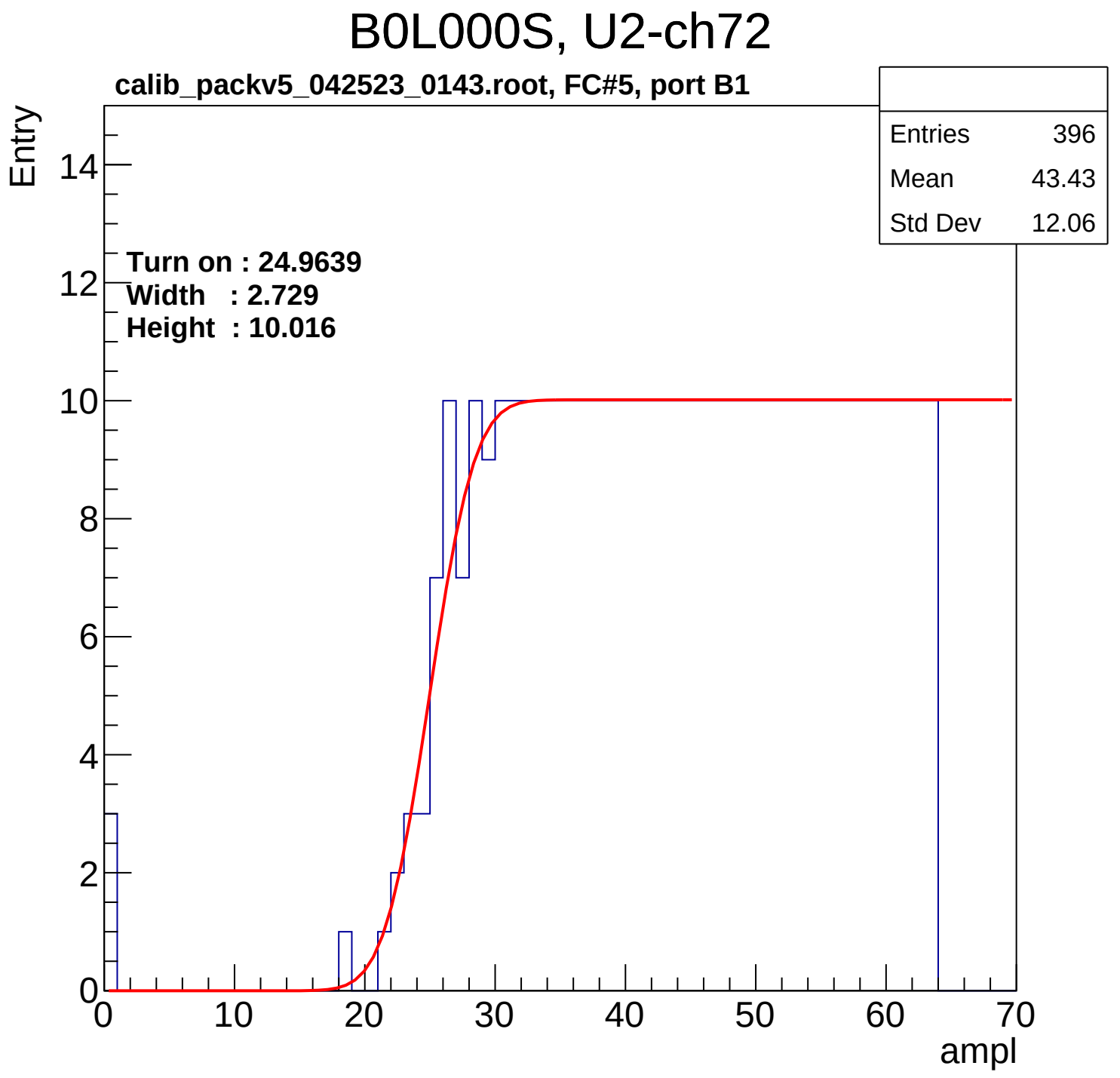
B0L000S, U2-ch72
calib_packv5_042523_0143.root, FC#5, port B1
Entries 396
Mean 43.43
Std Dev 12.06
Turn on : 24.9639
Width : 2.729
Height : 10.016
Entry
ampl
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6
8
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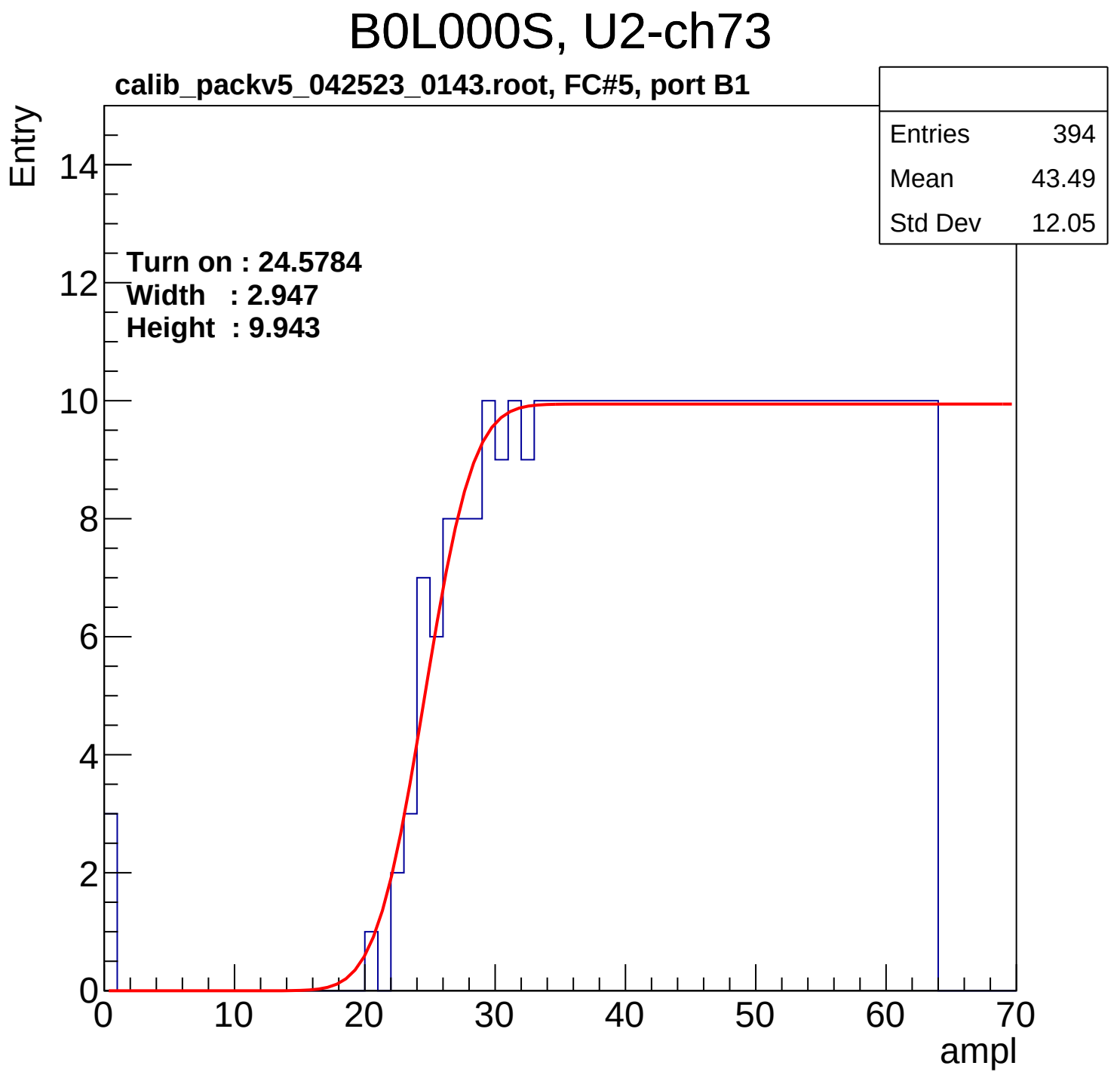
B0L000S, U2-ch73
calib_packv5_042523_0143.root, FC#5, port B1
Entries 394
Mean 43.49
Std Dev 12.05
Turn on : 24.5784
Width : 2.947
Height : 9.943
Entry
ampl
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6
8
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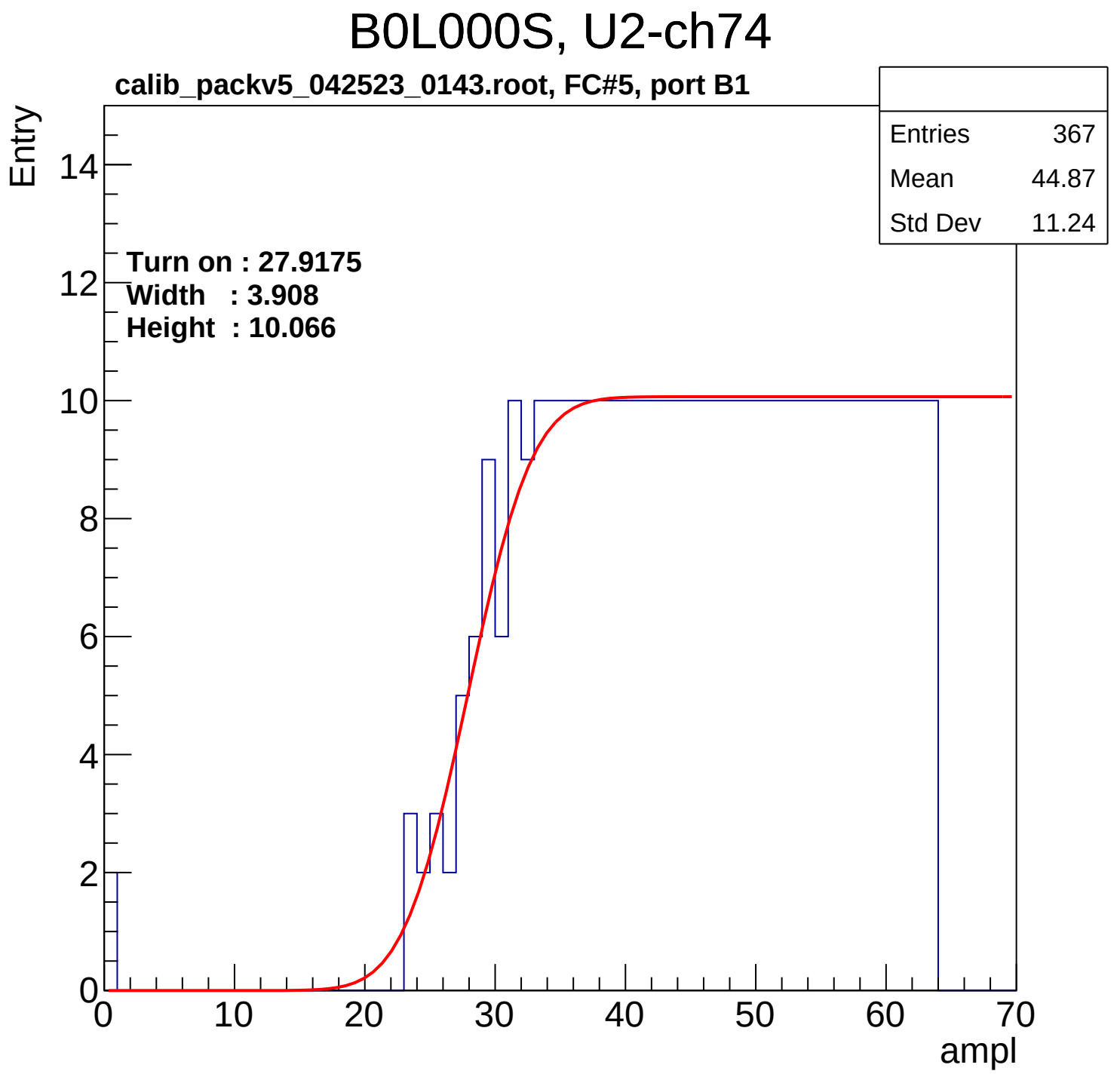
B0L000S, U2-ch74
calib_packv5_042523_0143.root, FC#5, port B1
Entries 367
Mean 44.87
Std Dev 11.24
Turn on : 27.9175
Width : 3.908
Height : 10.066
Entry
ampl
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4
6
8
10
12
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60
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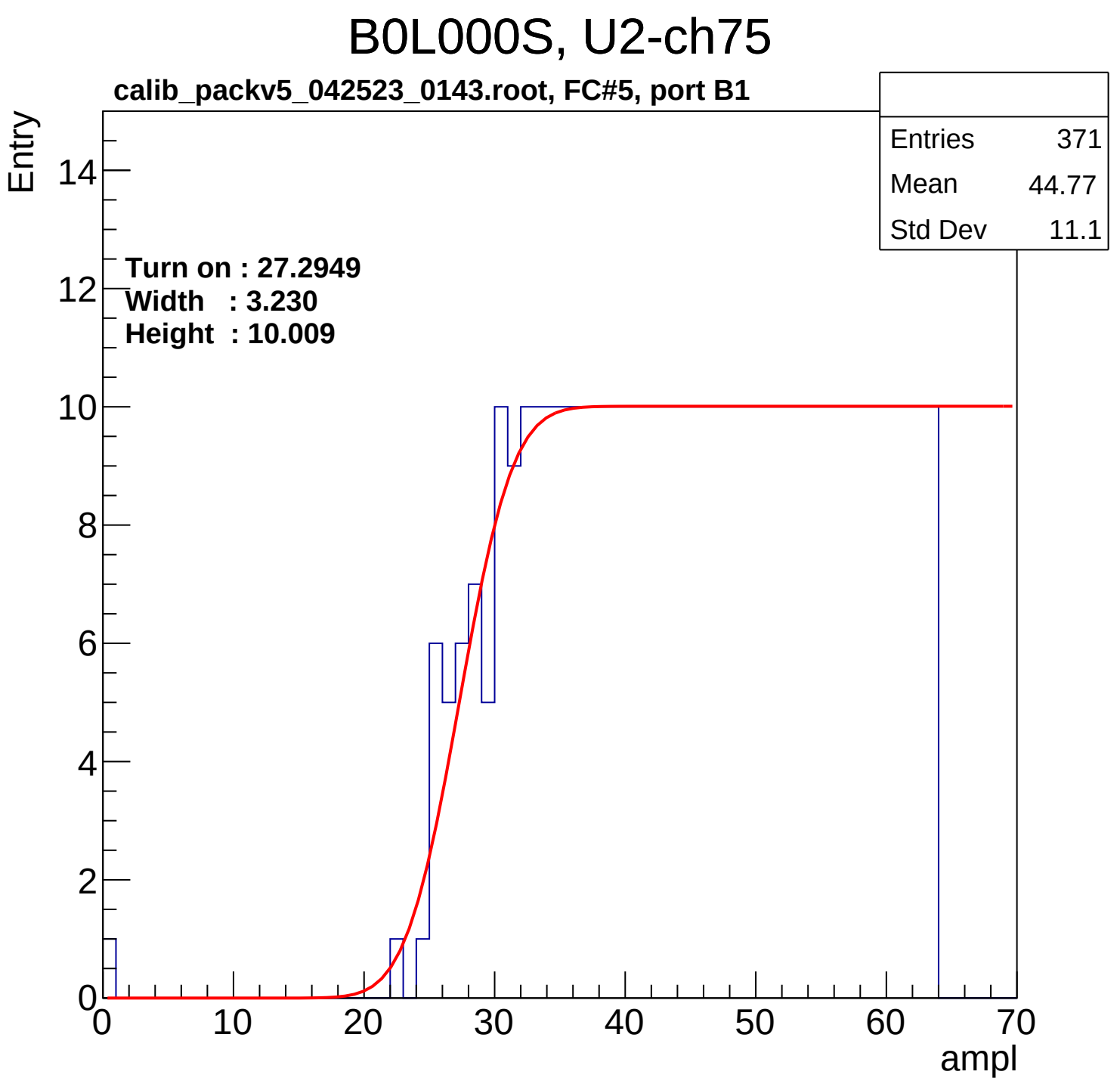
B0L000S, U2-ch75
calib_packv5_042523_0143.root, FC#5, port B1
Entries 371
Mean 44.77
Std Dev 11.1
Turn on : 27.2949
Width : 3.230
Height : 10.009
Entry
ampl
0
2
4
6
8
10
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0
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60
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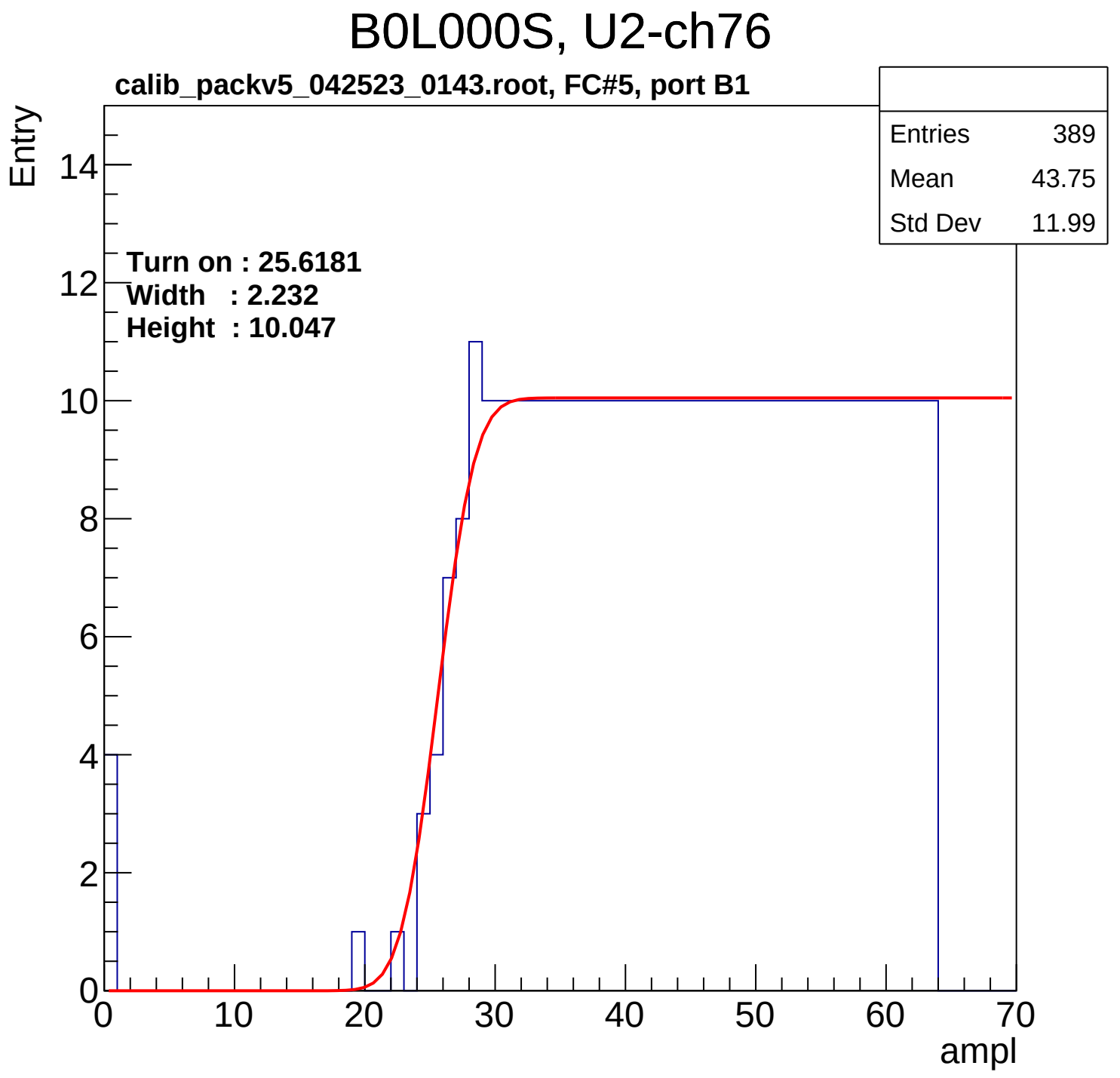
B0L000S, U2-ch76
calib_packv5_042523_0143.root, FC#5, port B1
Entries 389
Mean 43.75
Std Dev 11.99
Turn on : 25.6181
Width : 2.232
Height : 10.047
Entry
ampl
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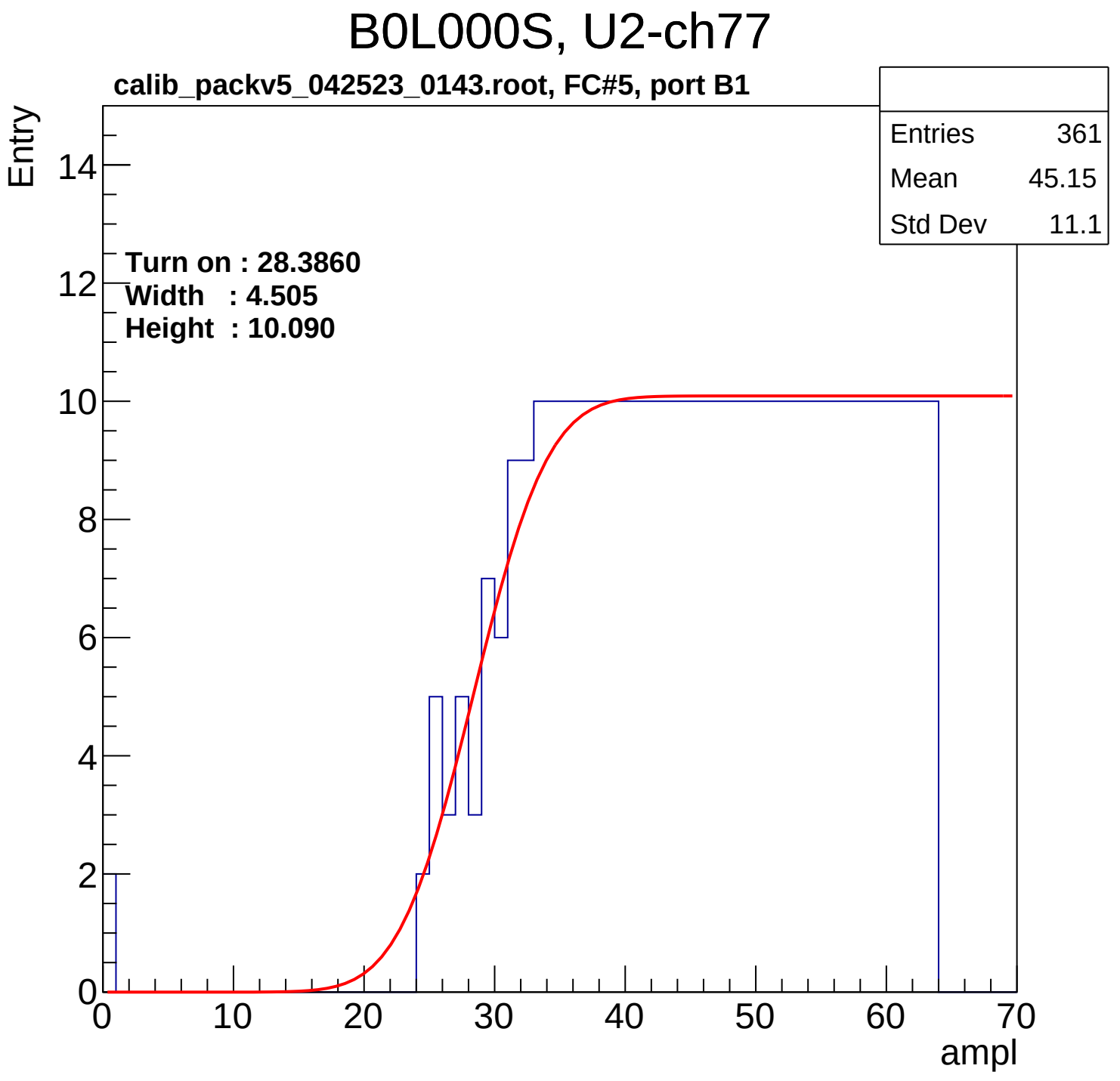
B0L000S, U2-ch77
calib_packv5_042523_0143.root, FC#5, port B1
Entries 361
Mean 45.15
Std Dev 11.1
Turn on : 28.3860
Width : 4.505
Height : 10.090
Entry
ampl
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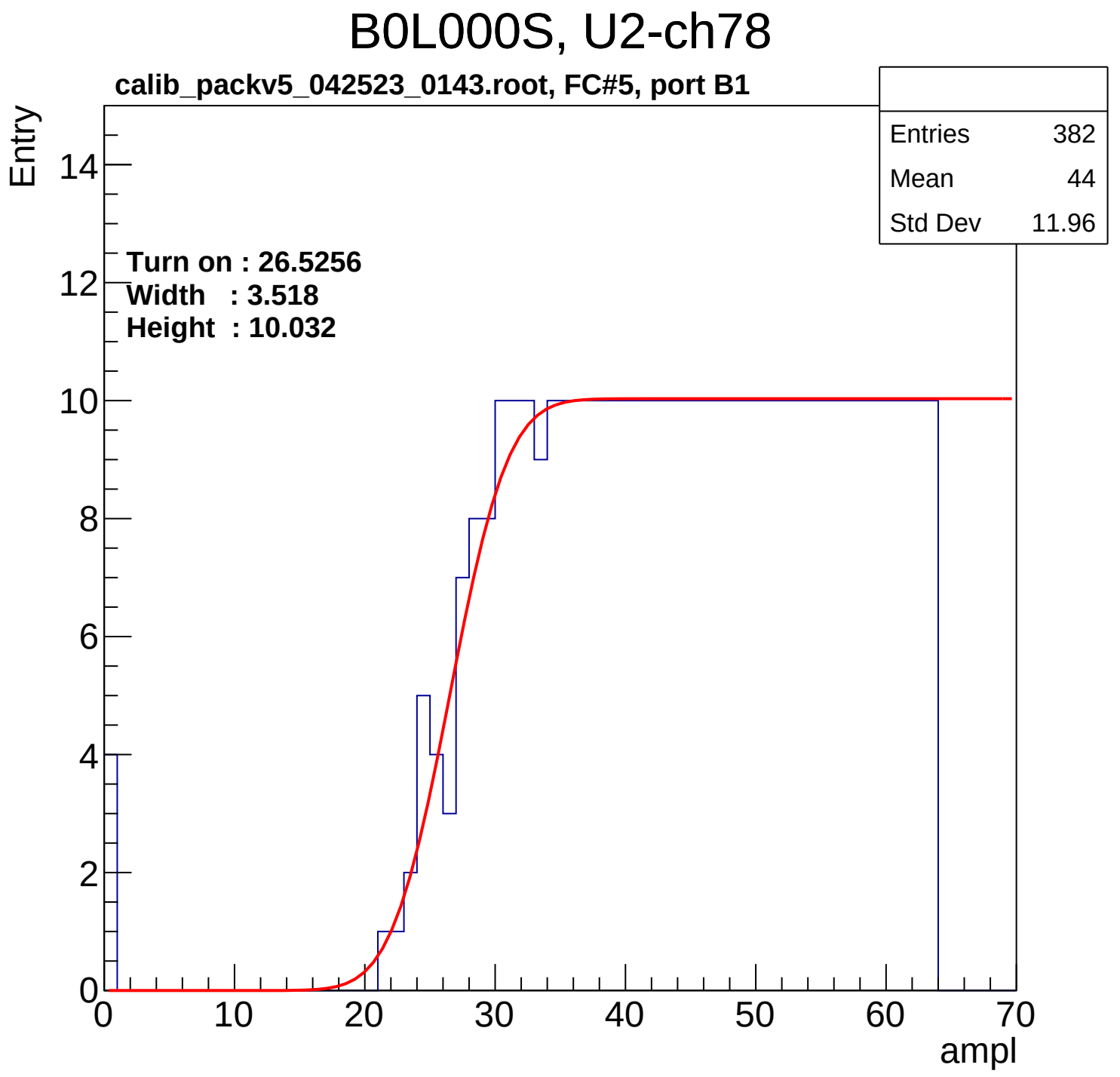
B0L000S, U2-ch78
calib_packv5_042523_0143.root, FC#5, port B1
Entries 382
Mean 44
Std Dev 11.96
Turn on : 26.5256
Width : 3.518
Height : 10.032
Entry
ampl
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6
8
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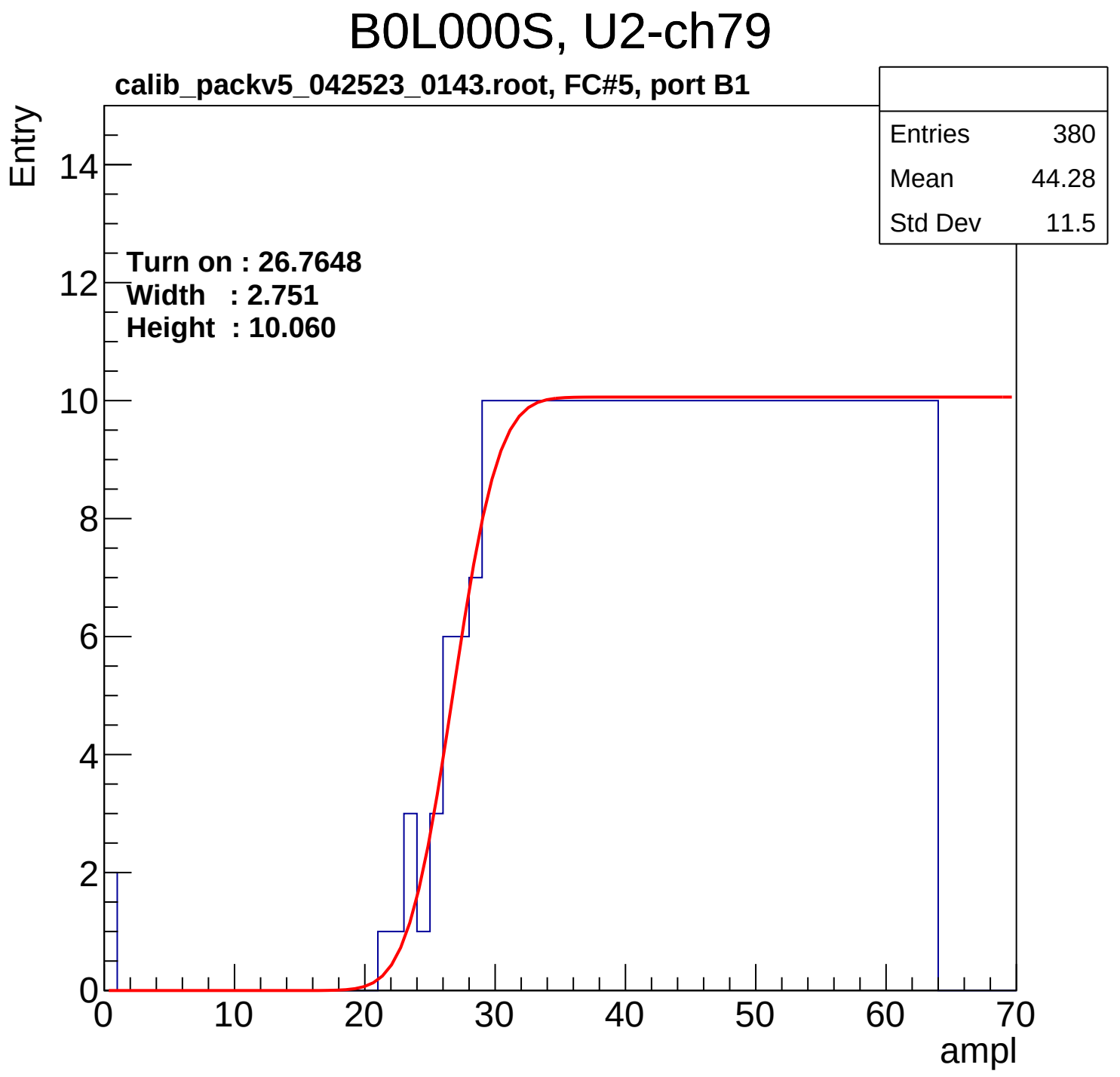
B0L000S, U2-ch79
calib_packv5_042523_0143.root, FC#5, port B1
Entries 380
Mean 44.28
Std Dev 11.5
Turn on : 26.7648
Width : 2.751
Height : 10.060
Entry
ampl
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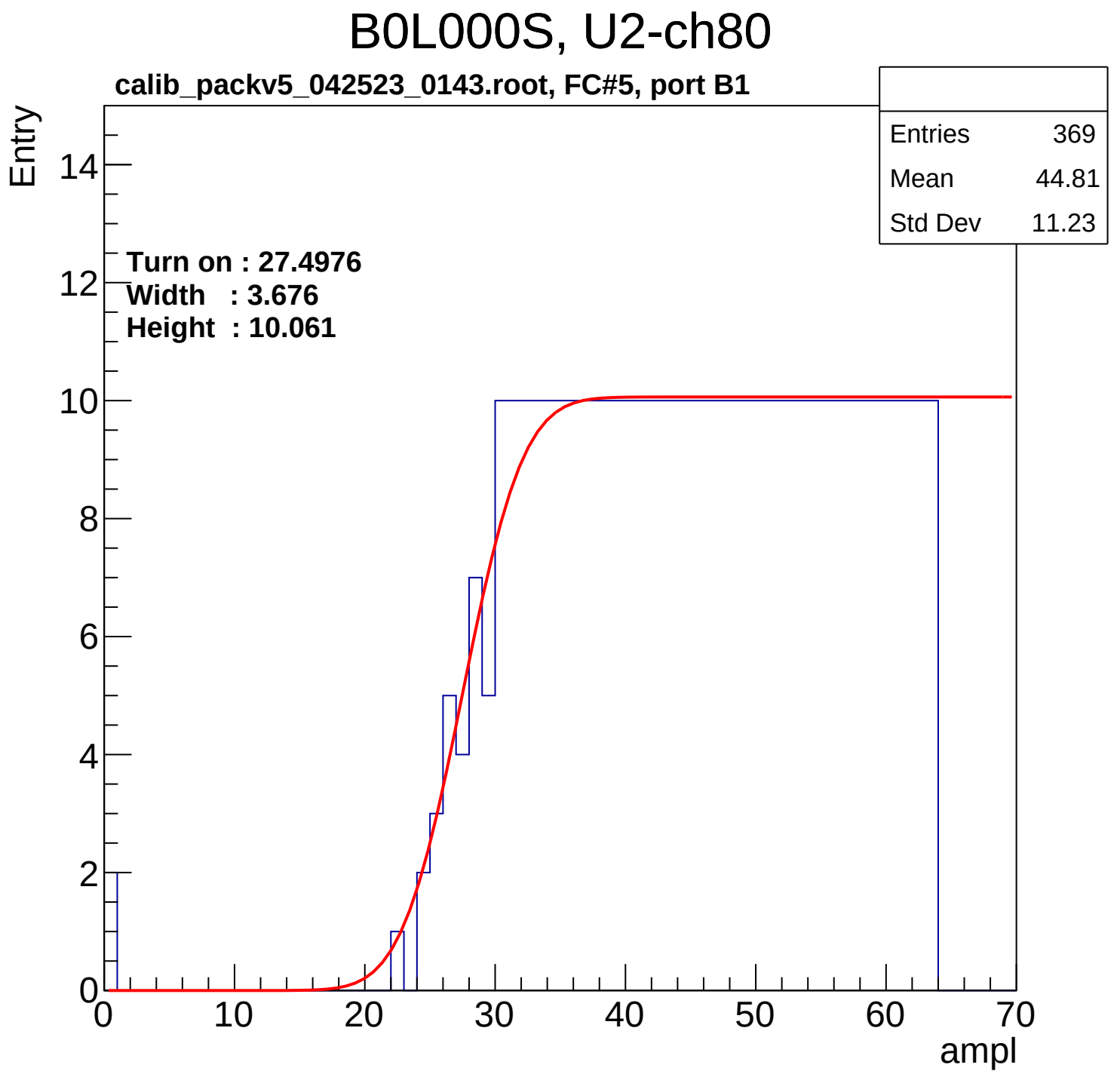
B0L000S, U2-ch80
calib_packv5_042523_0143.root, FC#5, port B1
Entries 369
Mean 44.81
Std Dev 11.23
Turn on : 27.4976
Width : 3.676
Height : 10.061
Entry
ampl
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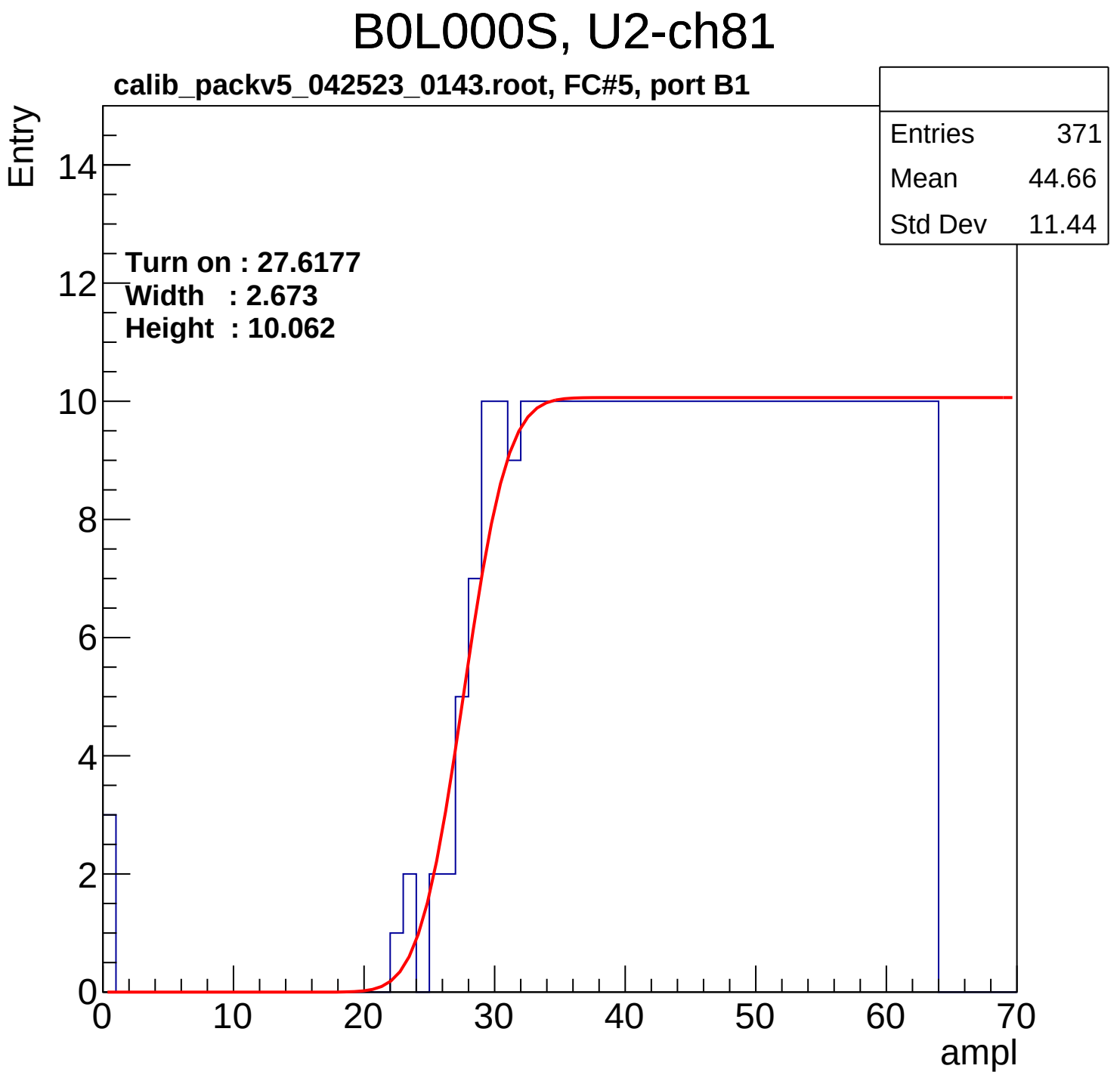
B0L000S, U2-ch81
calib_packv5_042523_0143.root, FC#5, port B1
Entries 371
Mean 44.66
Std Dev 11.44
Turn on : 27.6177
Width : 2.673
Height : 10.062
Entry
ampl
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4
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8
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0
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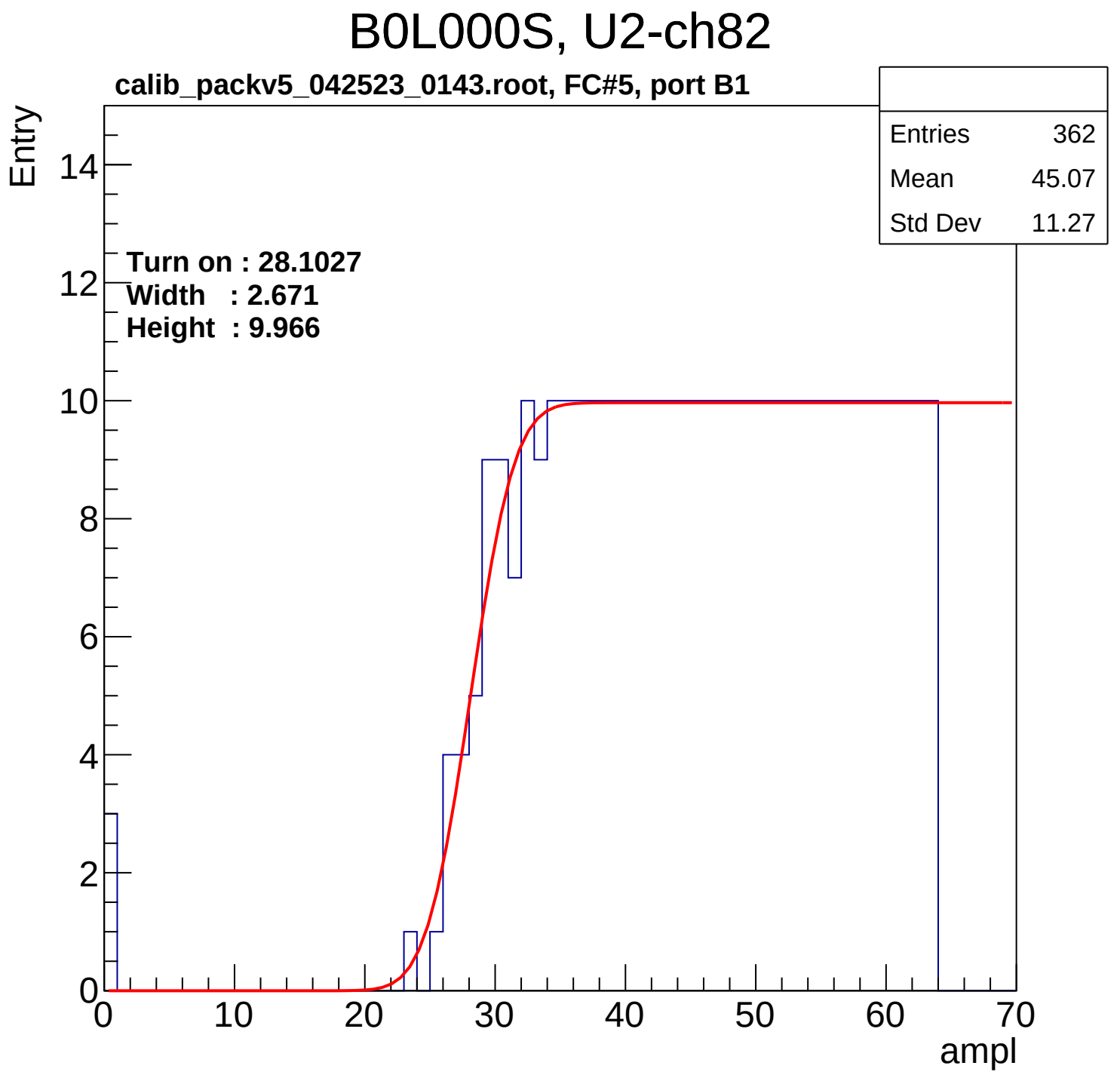
B0L000S, U2-ch82
calib_packv5_042523_0143.root, FC#5, port B1
Entries 362
Mean 45.07
Std Dev 11.27
Turn on : 28.1027
Width : 2.671
Height : 9.966
Entry
ampl
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6
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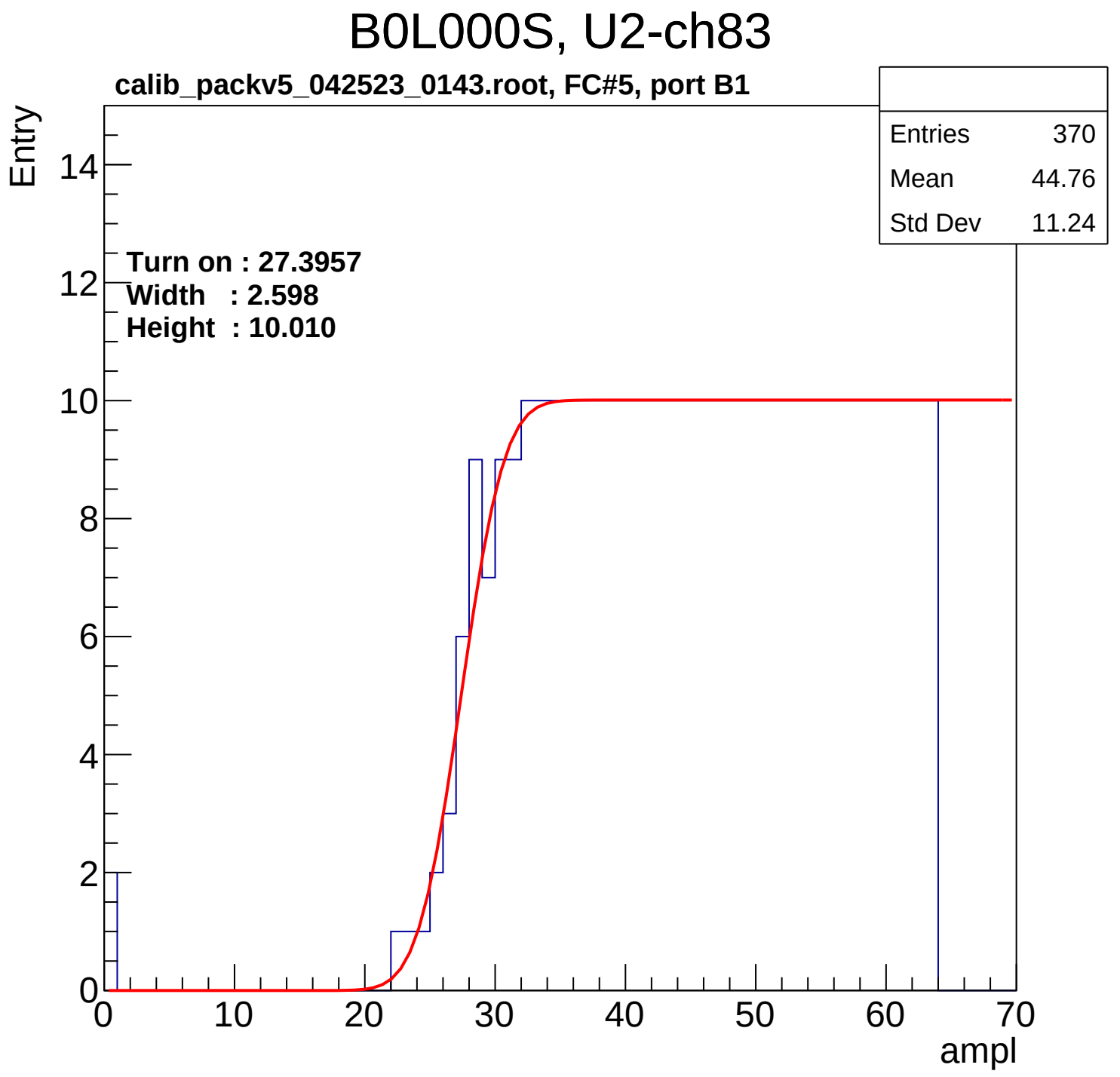
B0L000S, U2-ch83
calib_packv5_042523_0143.root, FC#5, port B1
Entries 370
Mean 44.76
Std Dev 11.24
Turn on : 27.3957
Width : 2.598
Height : 10.010
Entry
ampl
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2
4
6
8
10
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60
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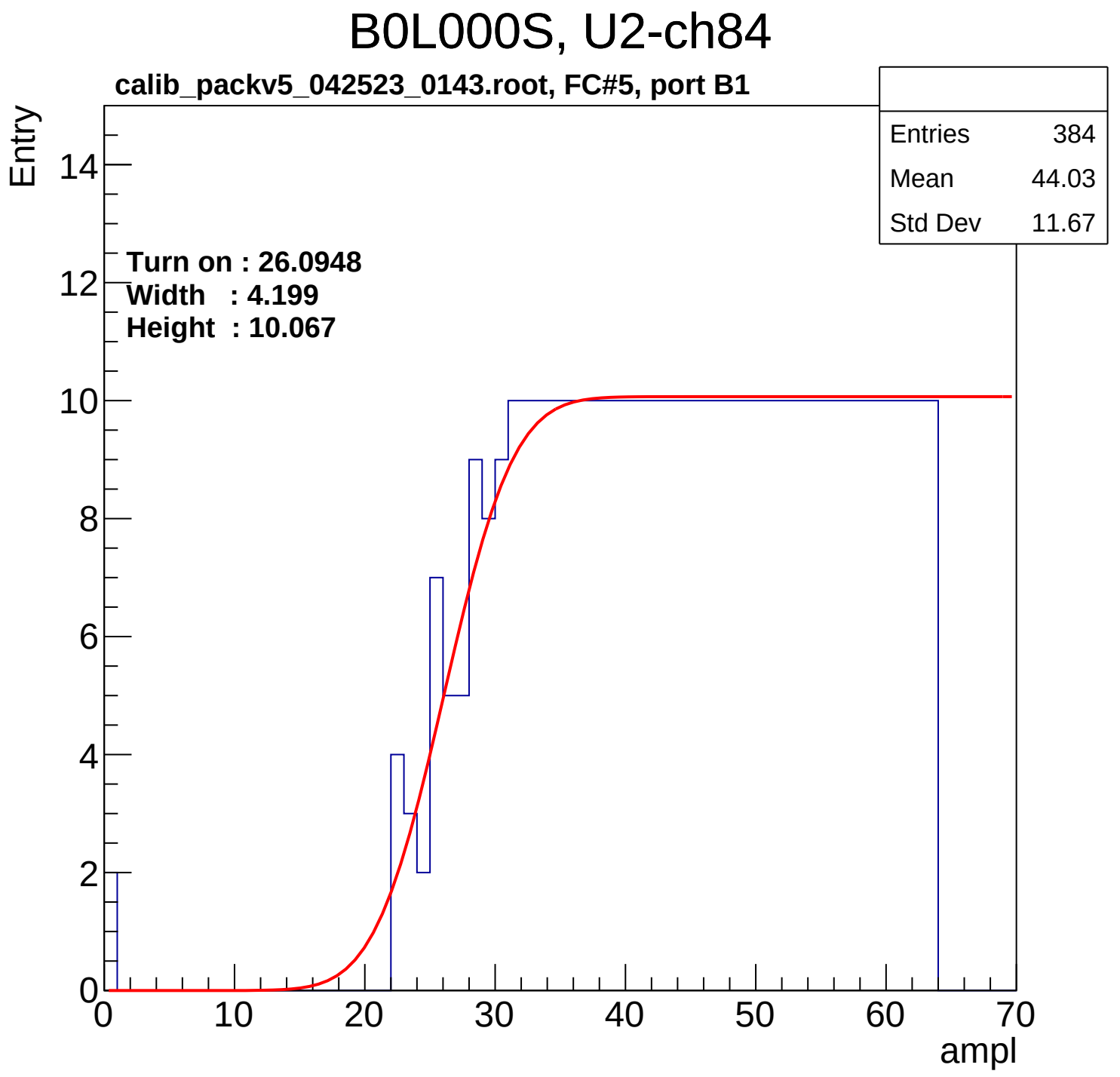
B0L000S, U2-ch84
calib_packv5_042523_0143.root, FC#5, port B1
Entries 384
Mean 44.03
Std Dev 11.67
Turn on : 26.0948
Width : 4.199
Height : 10.067
Entry
ampl
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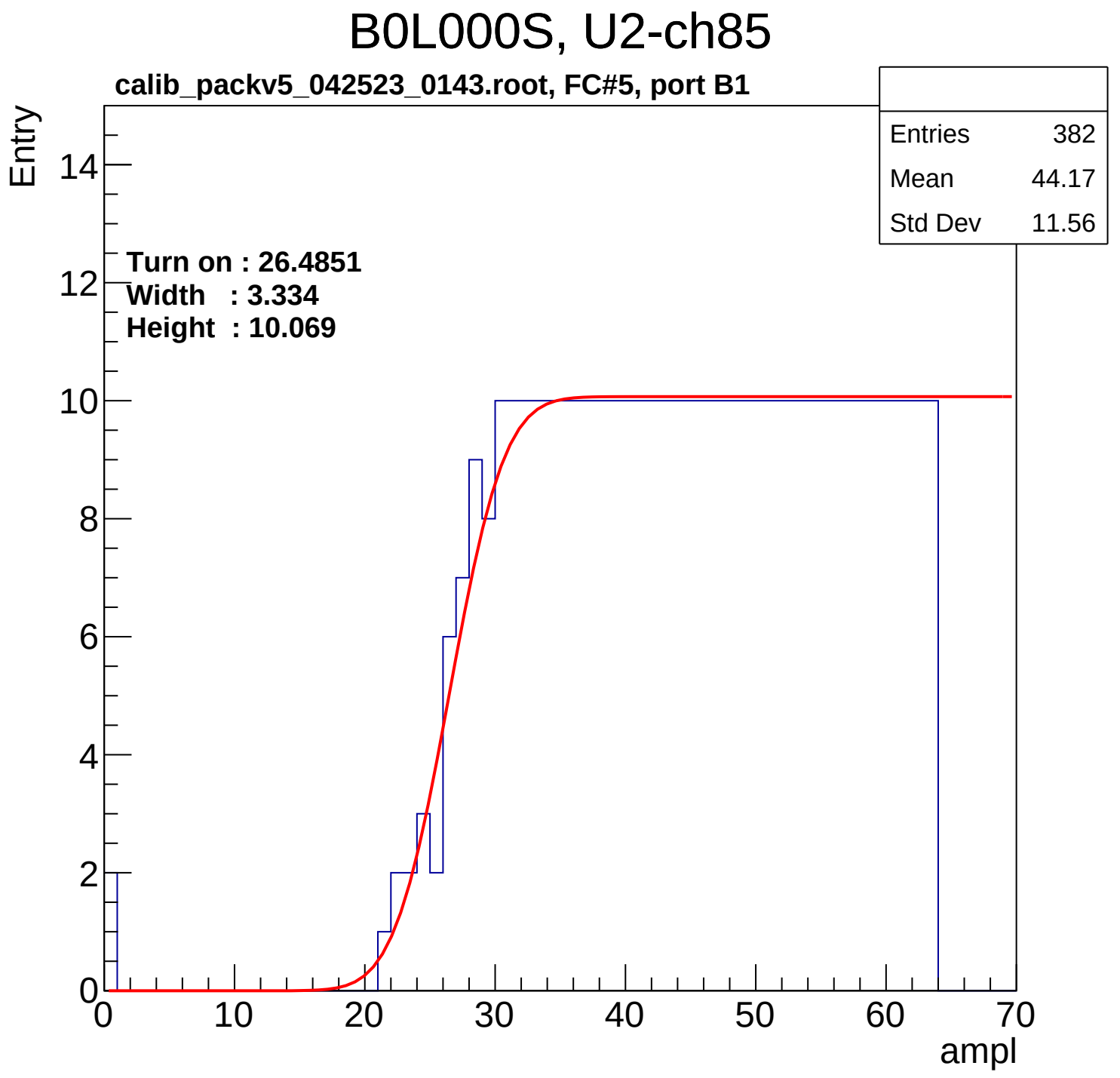
B0L000S, U2-ch85
calib_packv5_042523_0143.root, FC#5, port B1
Entries 382
Mean 44.17
Std Dev 11.56
Turn on : 26.4851
Width : 3.334
Height : 10.069
Entry
ampl
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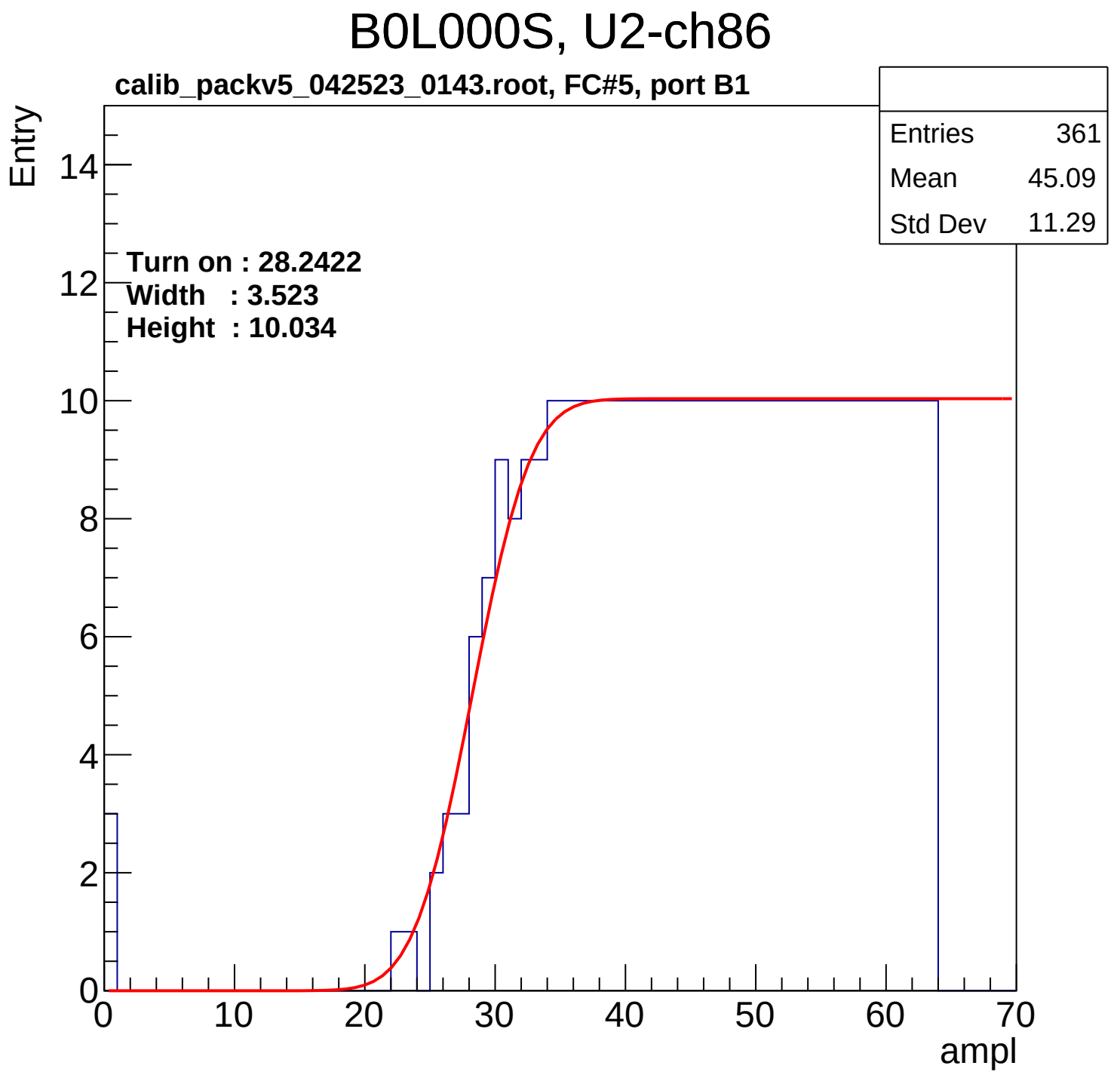
B0L000S, U2-ch86
calib_packv5_042523_0143.root, FC#5, port B1
Entries 361
Mean 45.09
Std Dev 11.29
Turn on : 28.2422
Width : 3.523
Height : 10.034
Entry
ampl
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4
6
8
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12
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10
20
30
40
50
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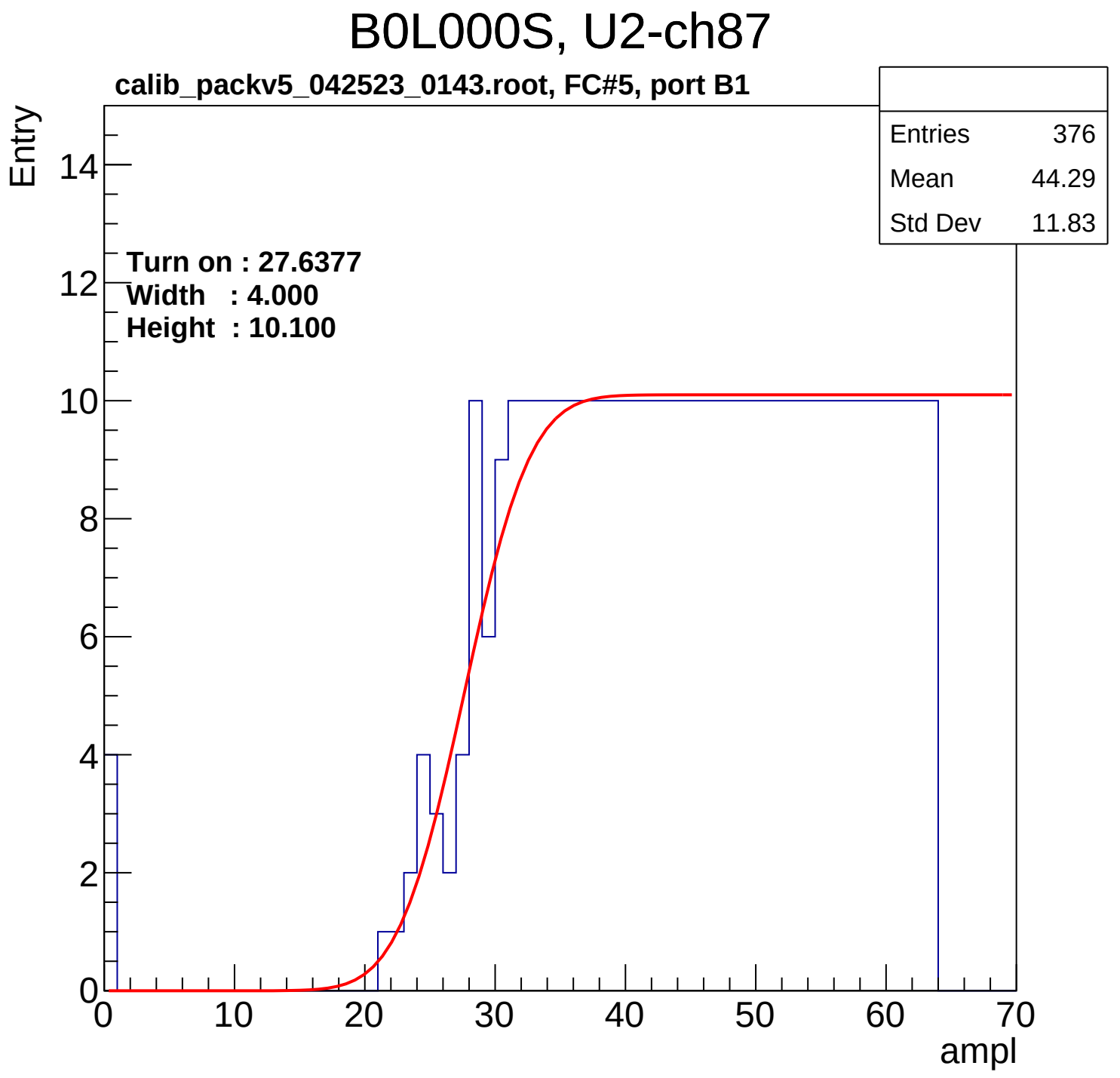
B0L000S, U2-ch87
calib_packv5_042523_0143.root, FC#5, port B1
Entries 376
Mean 44.29
Std Dev 11.83
Turn on : 27.6377
Width : 4.000
Height : 10.100
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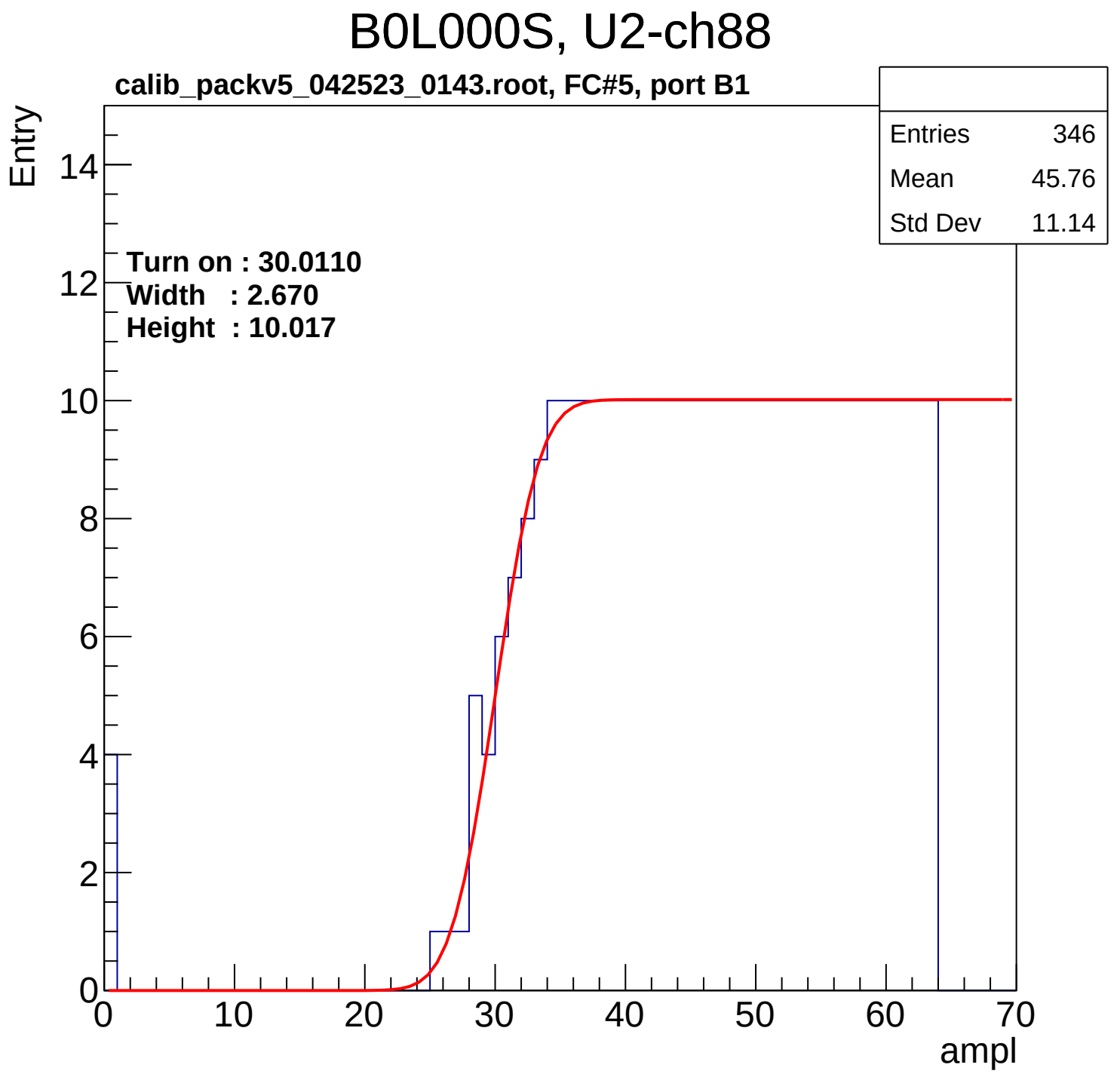
B0L000S, U2-ch88
calib_packv5_042523_0143.root, FC#5, port B1
Entries 346
Mean 45.76
Std Dev 11.14
Turn on : 30.0110
Width : 2.670
Height : 10.017
Entry
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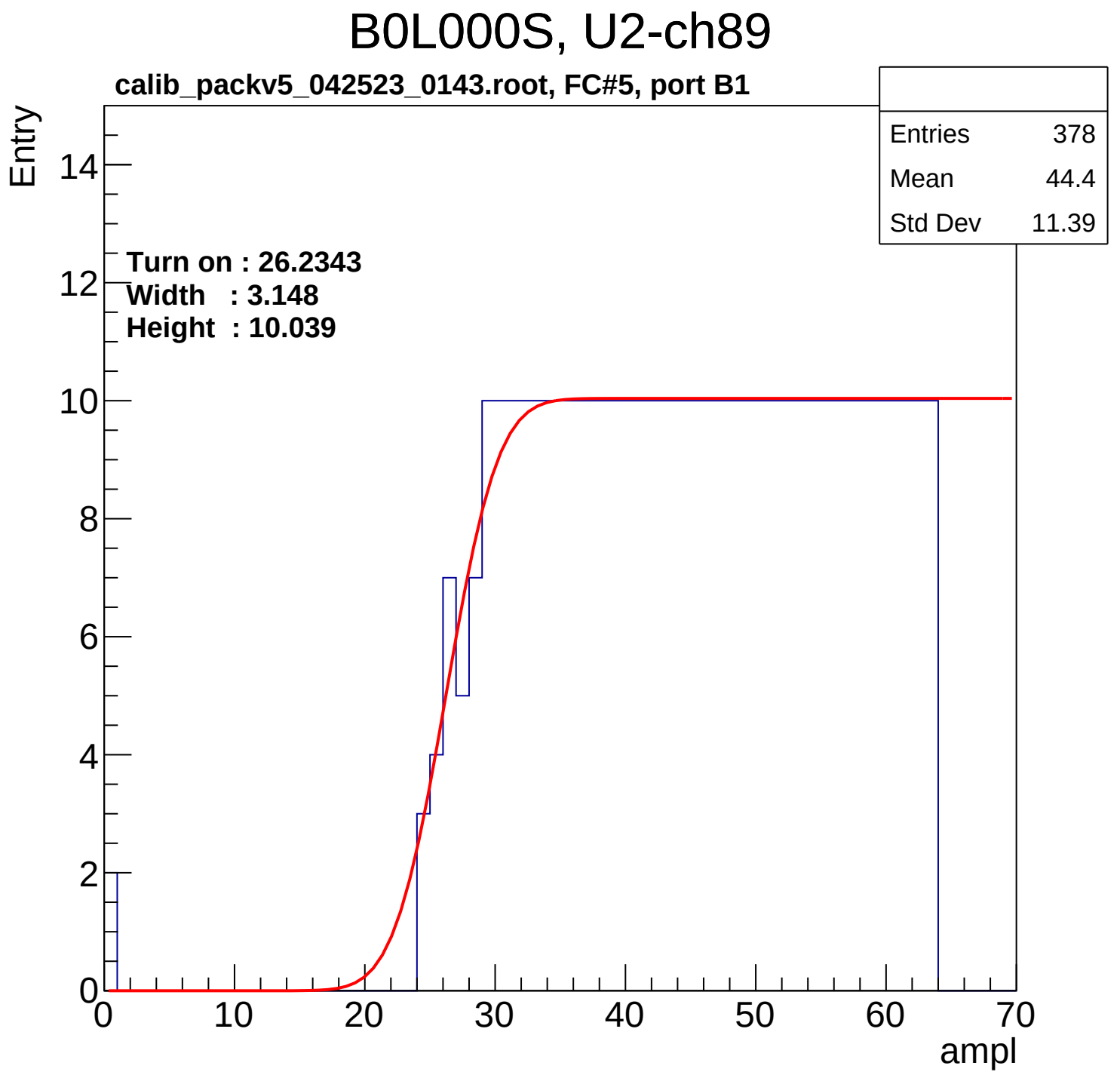
B0L000S, U2-ch89
calib_packv5_042523_0143.root, FC#5, port B1
Entries 378
Mean 44.4
Std Dev 11.39
Turn on : 26.2343
Width : 3.148
Height : 10.039
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ampl
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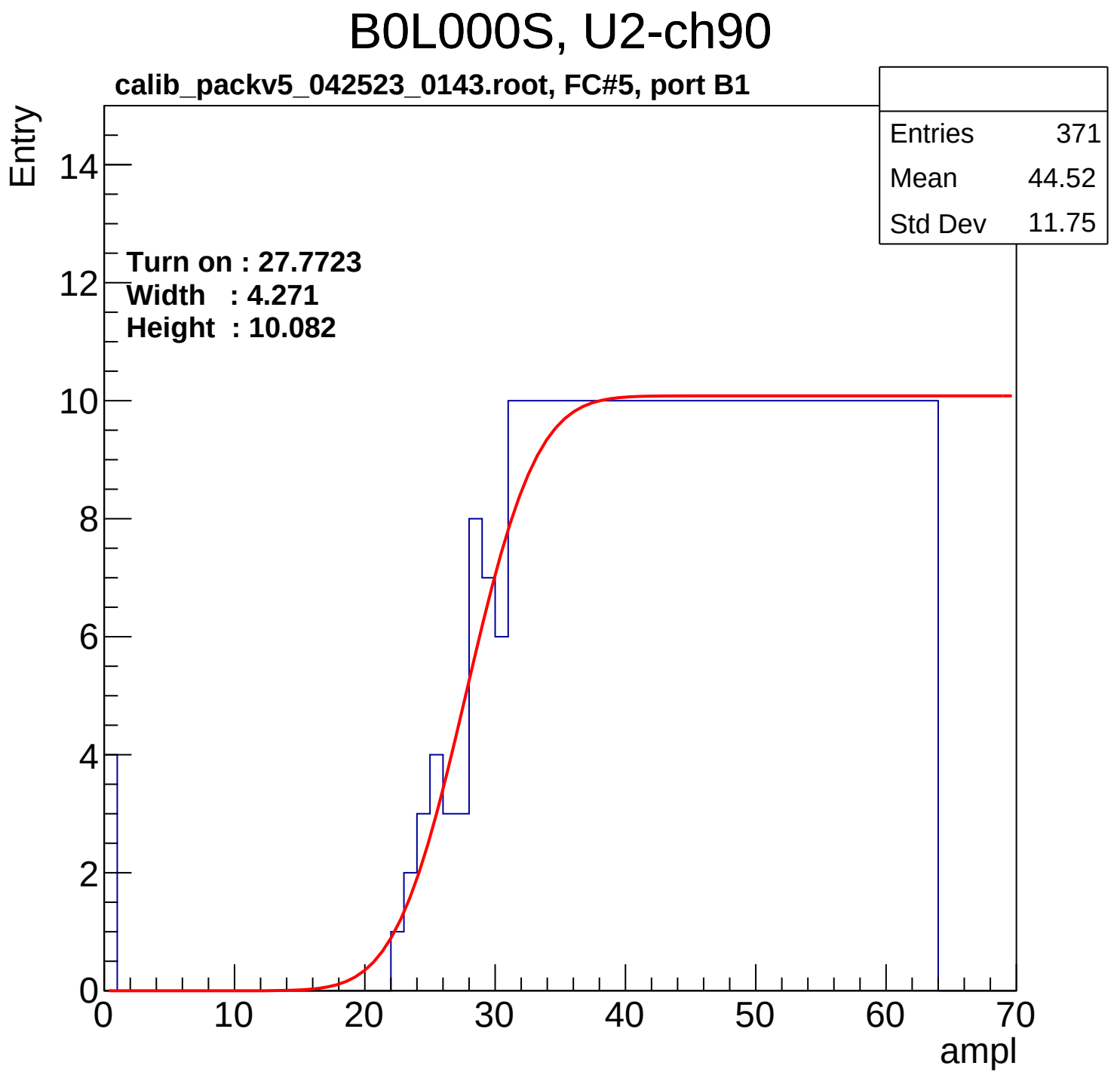
B0L000S, U2-ch90
calib_packv5_042523_0143.root, FC#5, port B1
Entries 371
Mean 44.52
Std Dev 11.75
Turn on : 27.7723
Width : 4.271
Height : 10.082
Entry
ampl
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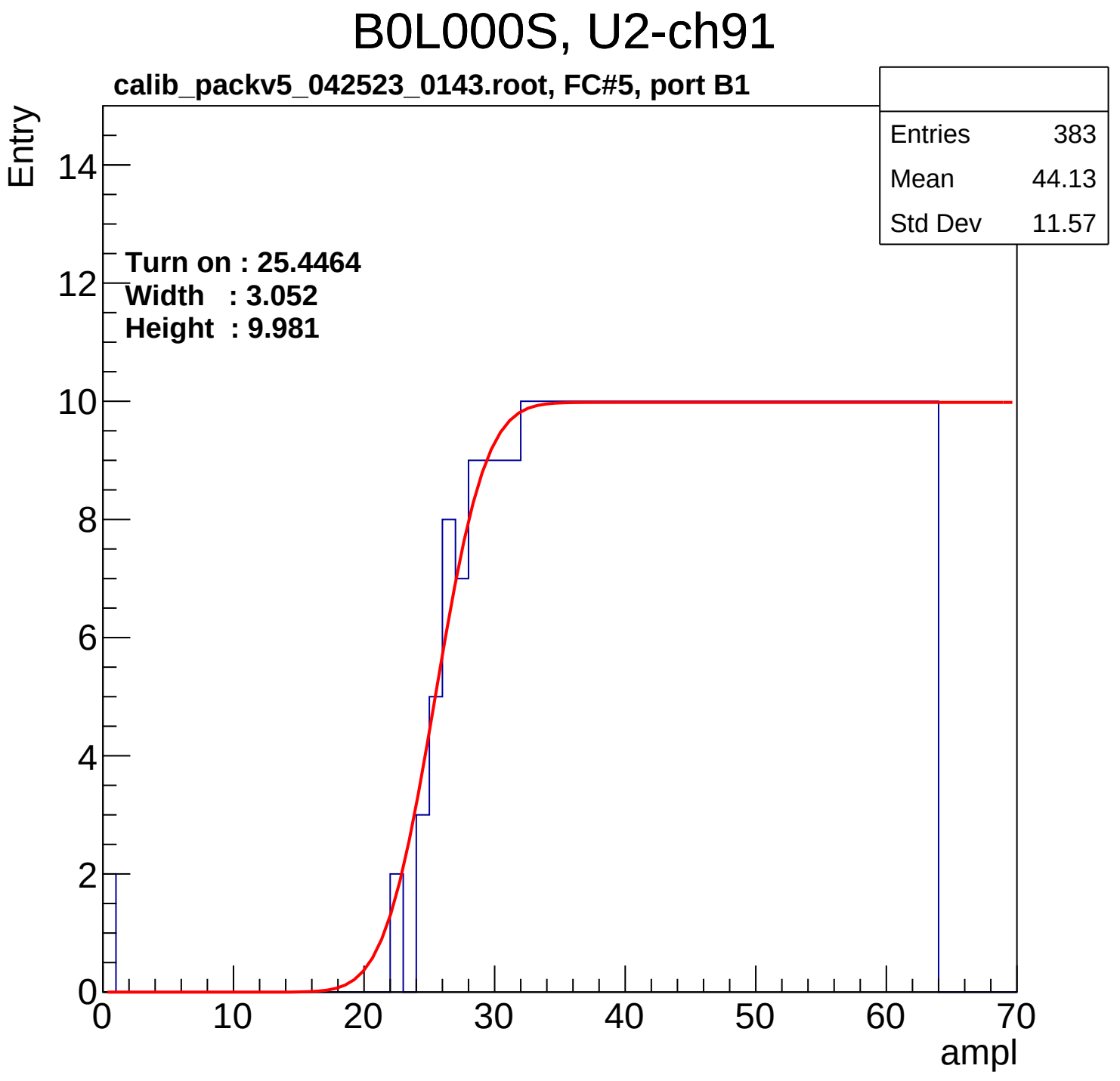
B0L000S, U2-ch91
calib_packv5_042523_0143.root, FC#5, port B1
Entries 383
Mean 44.13
Std Dev 11.57
Turn on : 25.4464
Width : 3.052
Height : 9.981
Entry
ampl
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4
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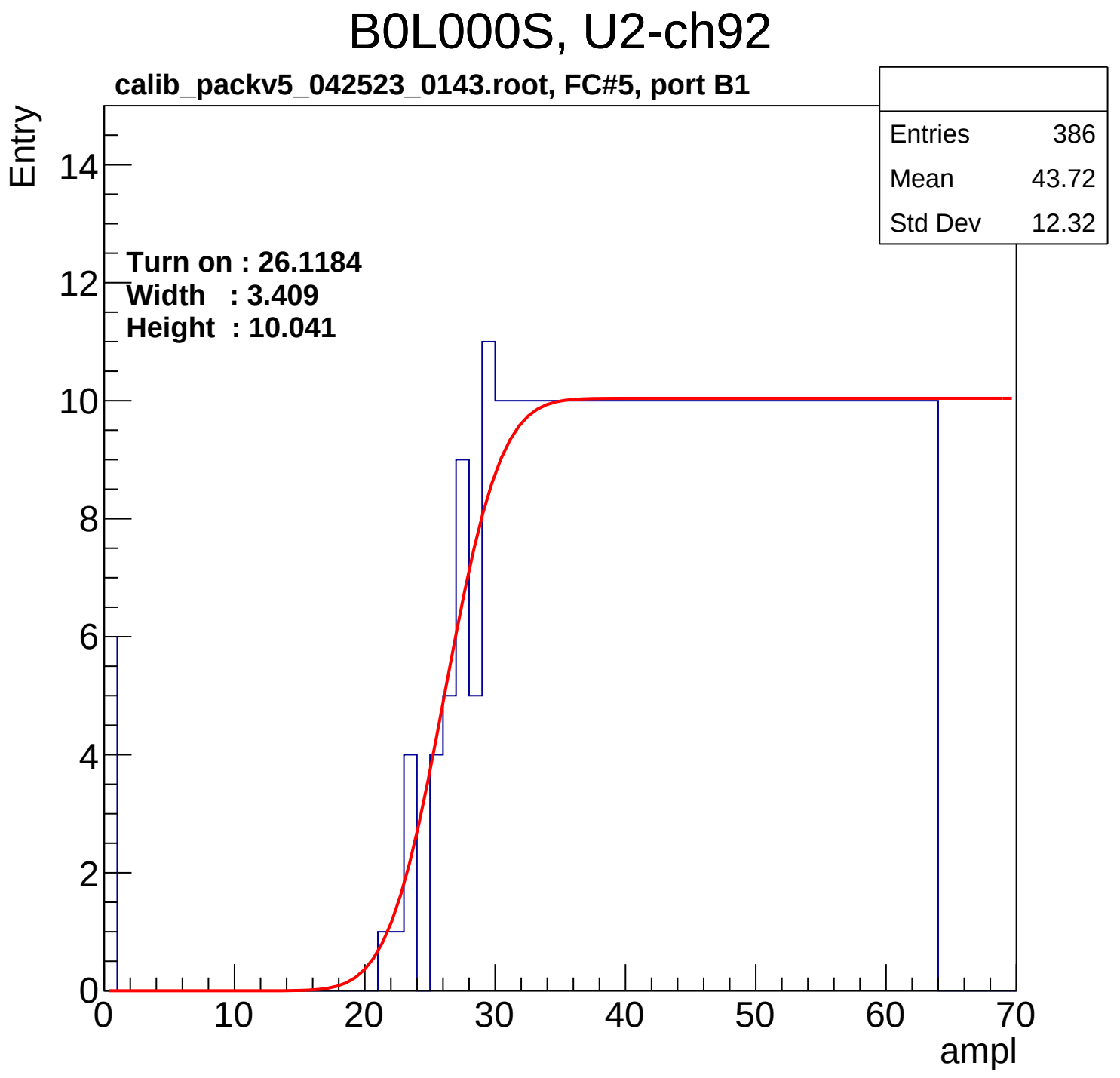
B0L000S, U2-ch92
calib_packv5_042523_0143.root, FC#5, port B1
Entries 386
Mean 43.72
Std Dev 12.32
Turn on : 26.1184
Width : 3.409
Height : 10.041
Entry
ampl
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2
4
6
8
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0
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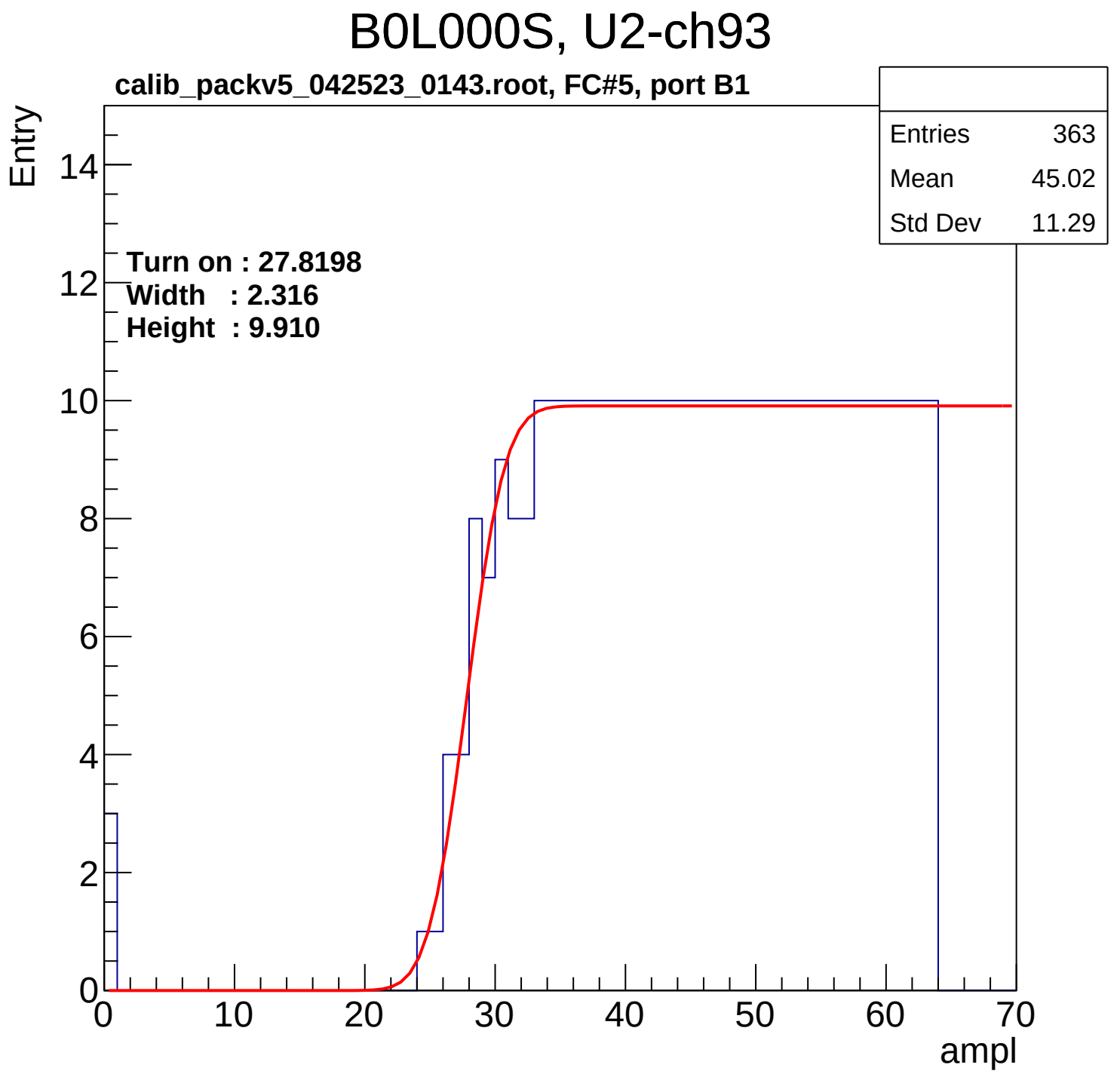
B0L000S, U2-ch93
calib_packv5_042523_0143.root, FC#5, port B1
Entries 363
Mean 45.02
Std Dev 11.29
Turn on : 27.8198
Width : 2.316
Height : 9.910
Entry
ampl
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6
8
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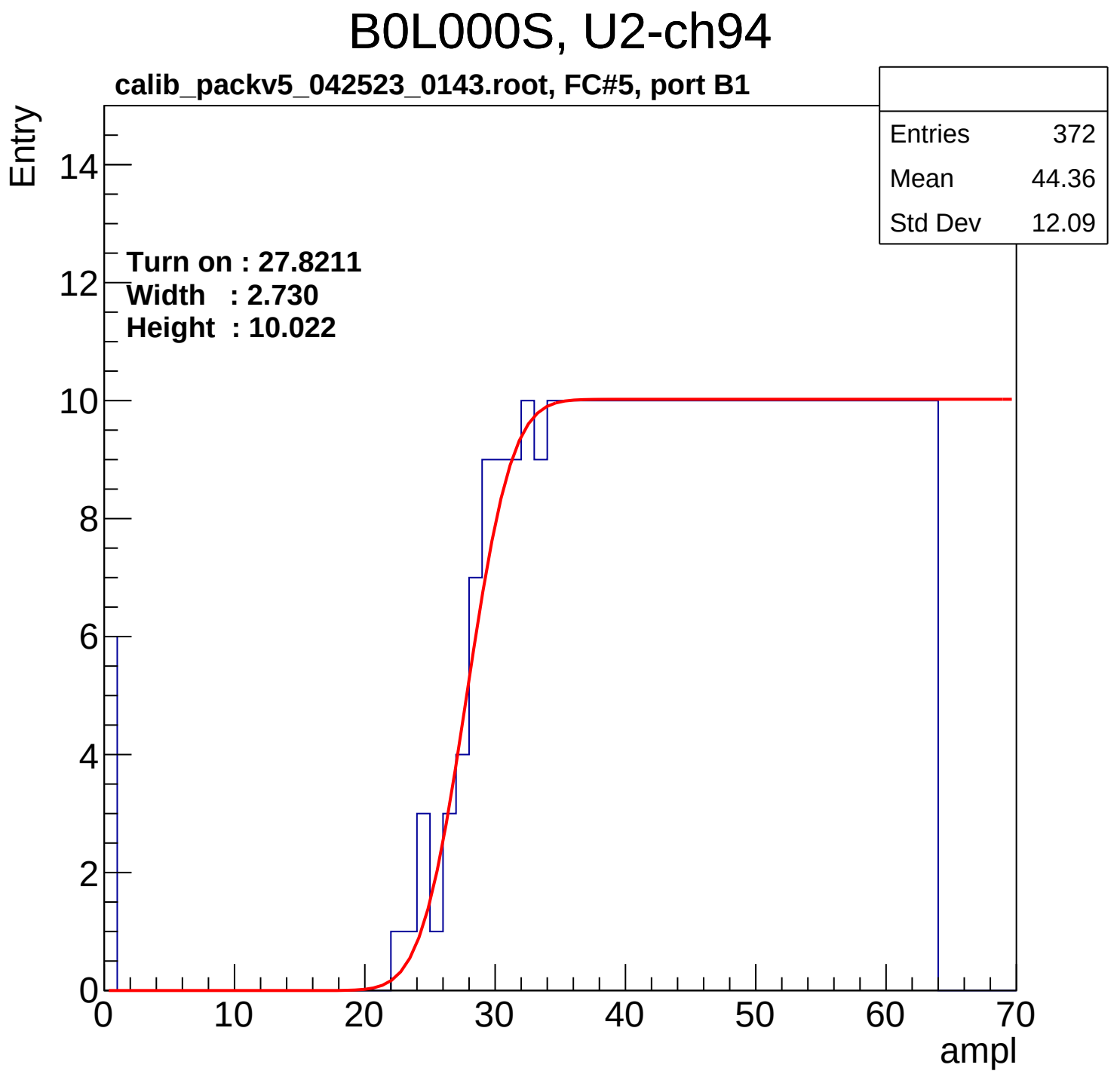
B0L000S, U2-ch94
calib_packv5_042523_0143.root, FC#5, port B1
Entries 372
Mean 44.36
Std Dev 12.09
Turn on : 27.8211
Width : 2.730
Height : 10.022
Entry
ampl
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2
4
6
8
10
12
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60
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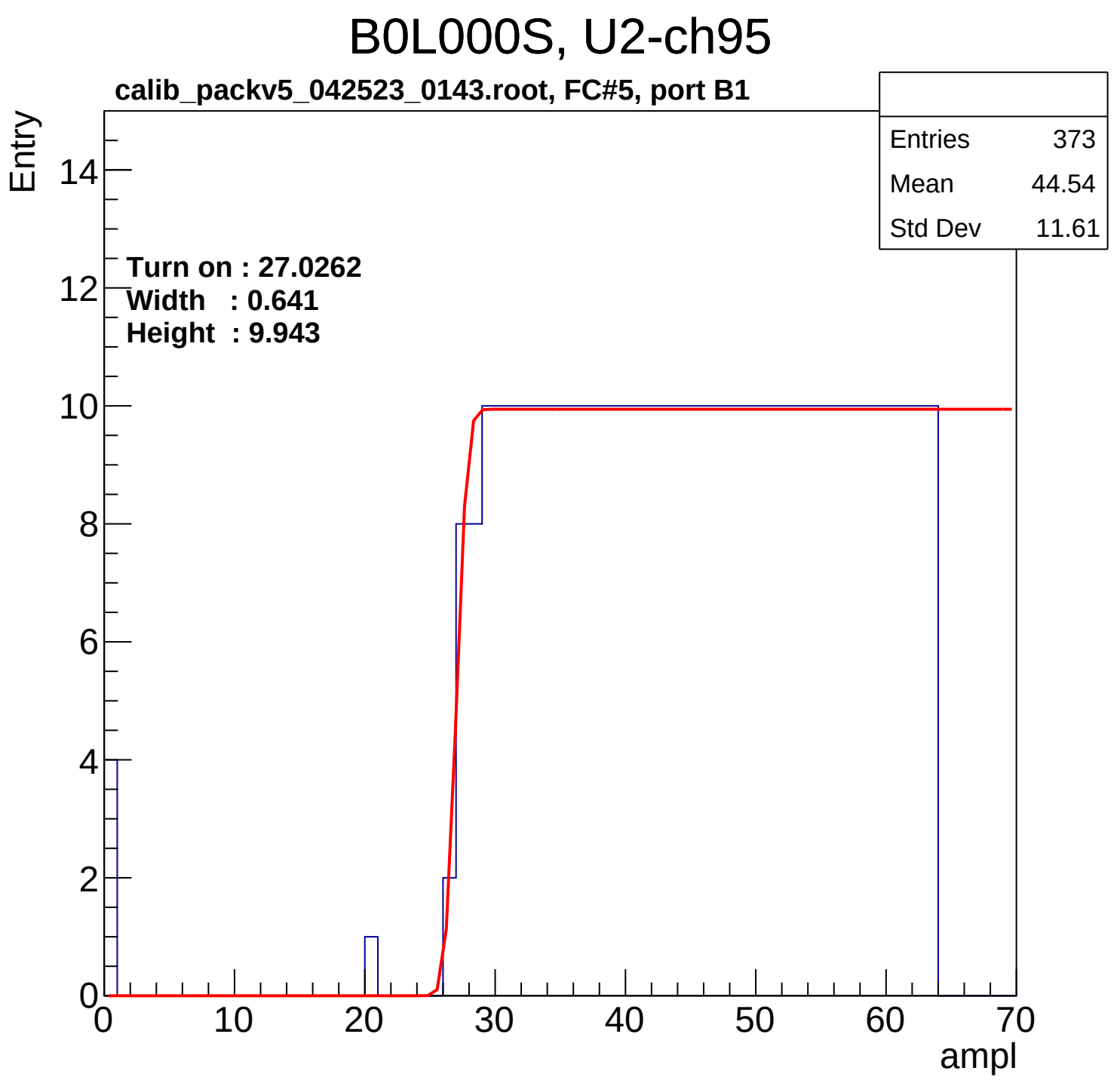
B0L000S, U2-ch95
calib_packv5_042523_0143.root, FC#5, port B1
Entries 373
Mean 44.54
Std Dev 11.61
Turn on : 27.0262
Width : 0.641
Height : 9.943
Entry
ampl
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6
8
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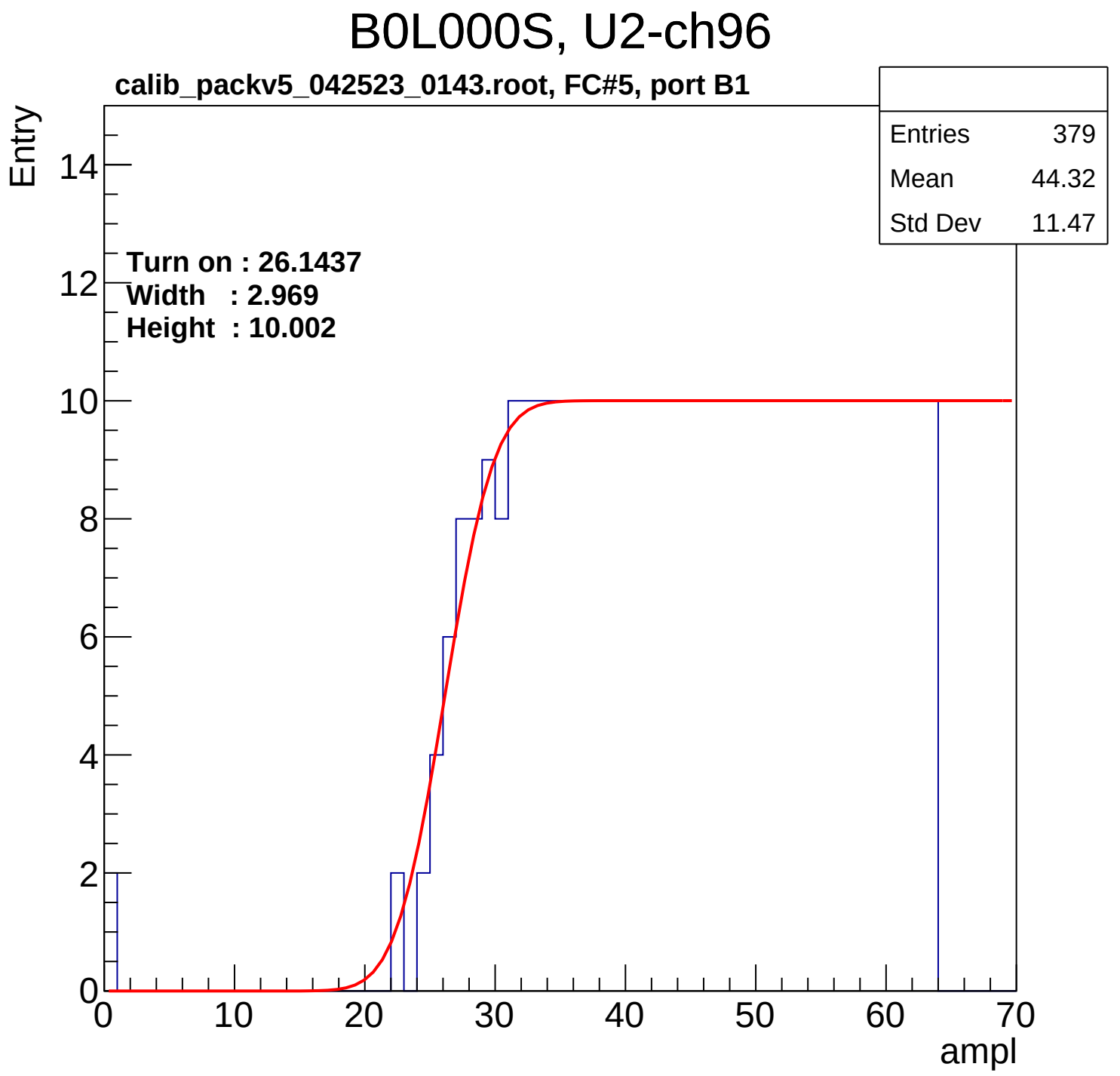
B0L000S, U2-ch96
calib_packv5_042523_0143.root, FC#5, port B1
Entries 379
Mean 44.32
Std Dev 11.47
Turn on : 26.1437
Width : 2.969
Height : 10.002
Entry
ampl
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6
8
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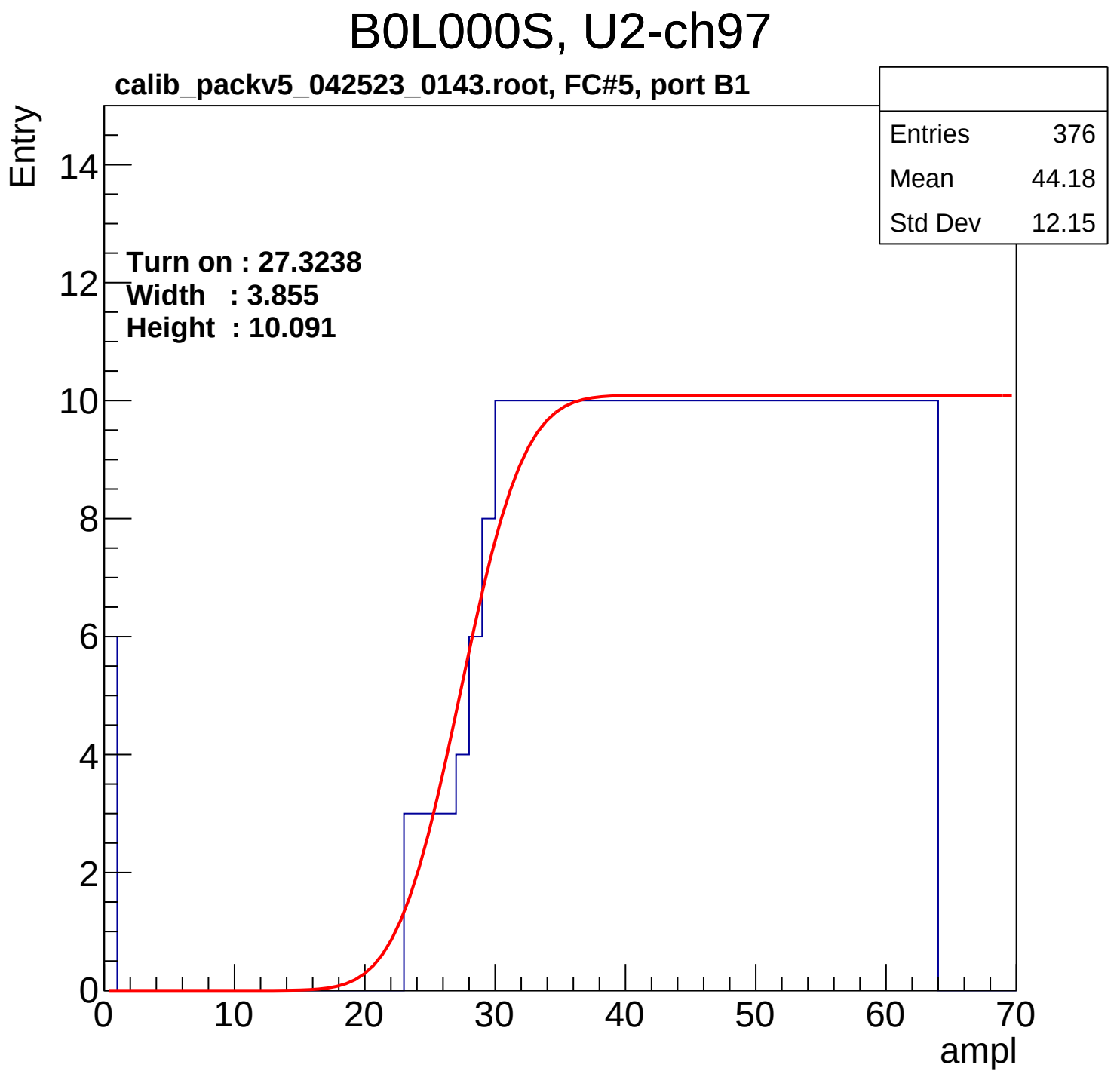
B0L000S, U2-ch97
calib_packv5_042523_0143.root, FC#5, port B1
Entries 376
Mean 44.18
Std Dev 12.15
Turn on : 27.3238
Width : 3.855
Height : 10.091
Entry
ampl
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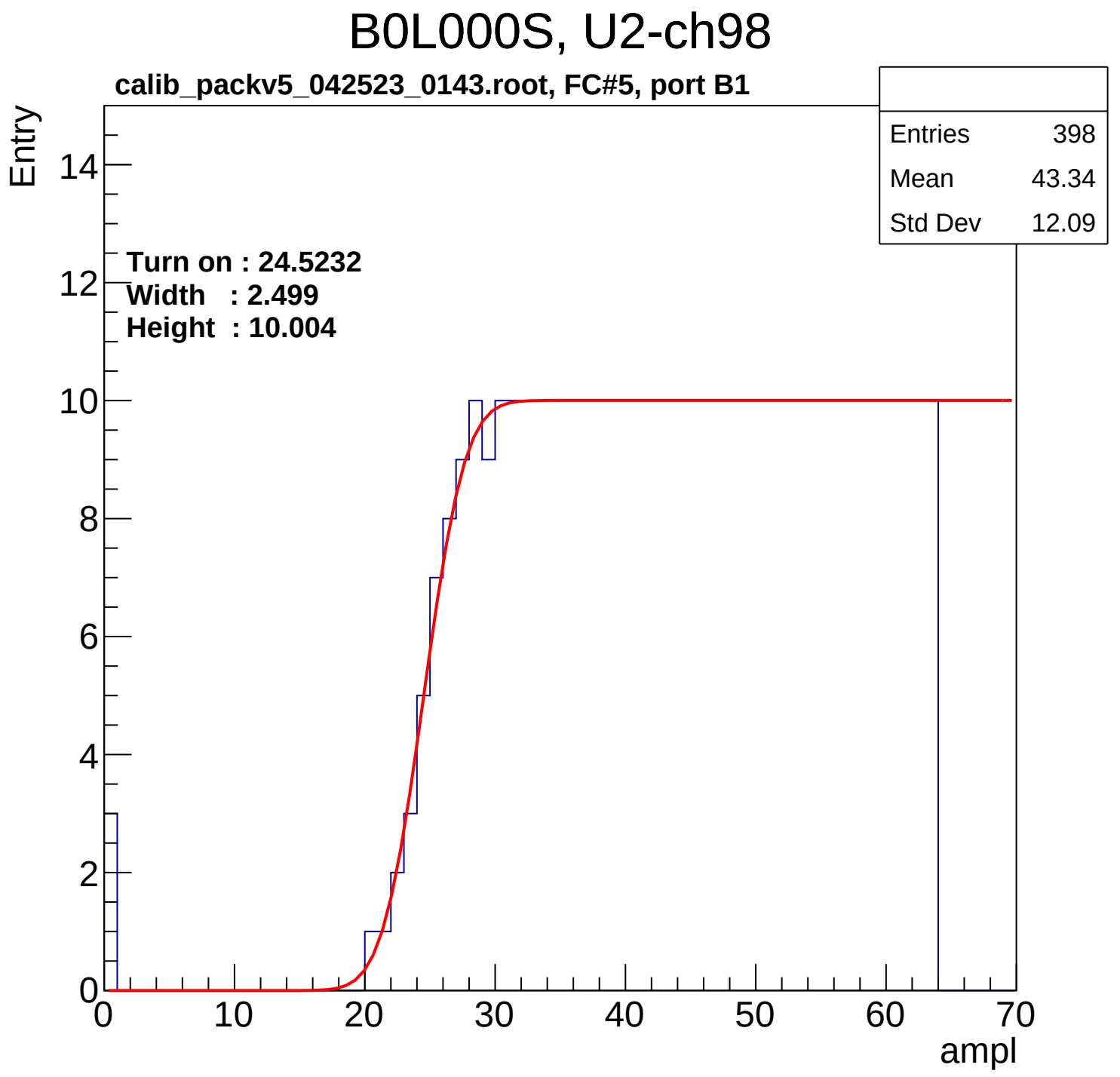
B0L000S, U2-ch98
calib_packv5_042523_0143.root, FC#5, port B1
Entries 398
Mean 43.34
Std Dev 12.09
Turn on : 24.5232
Width : 2.499
Height : 10.004
Entry
ampl
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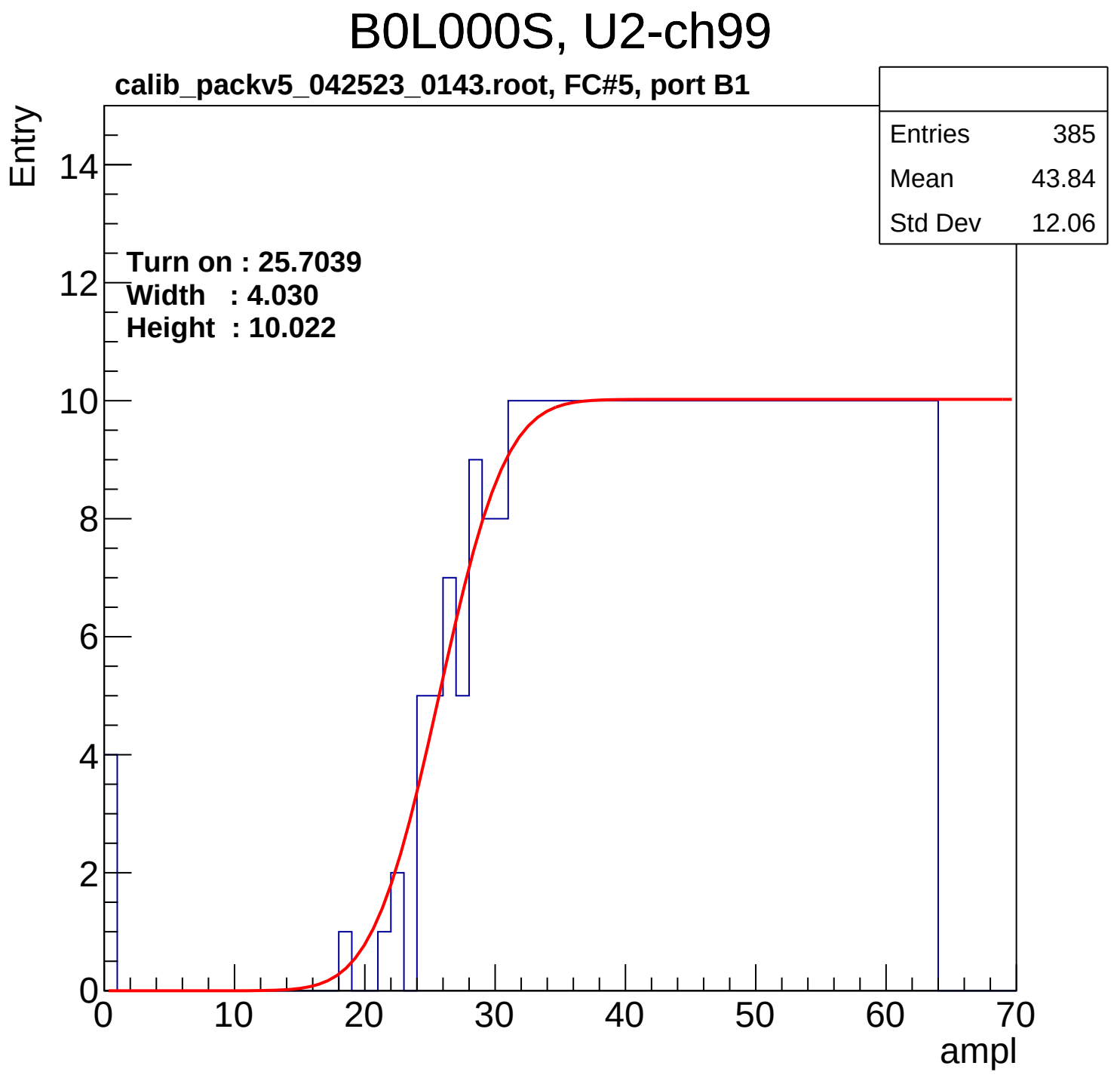
B0L000S, U2-ch99
calib_packv5_042523_0143.root, FC#5, port B1
Entries 385
Mean 43.84
Std Dev 12.06
Turn on : 25.7039
Width : 4.030
Height : 10.022
Entry
ampl
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6
8
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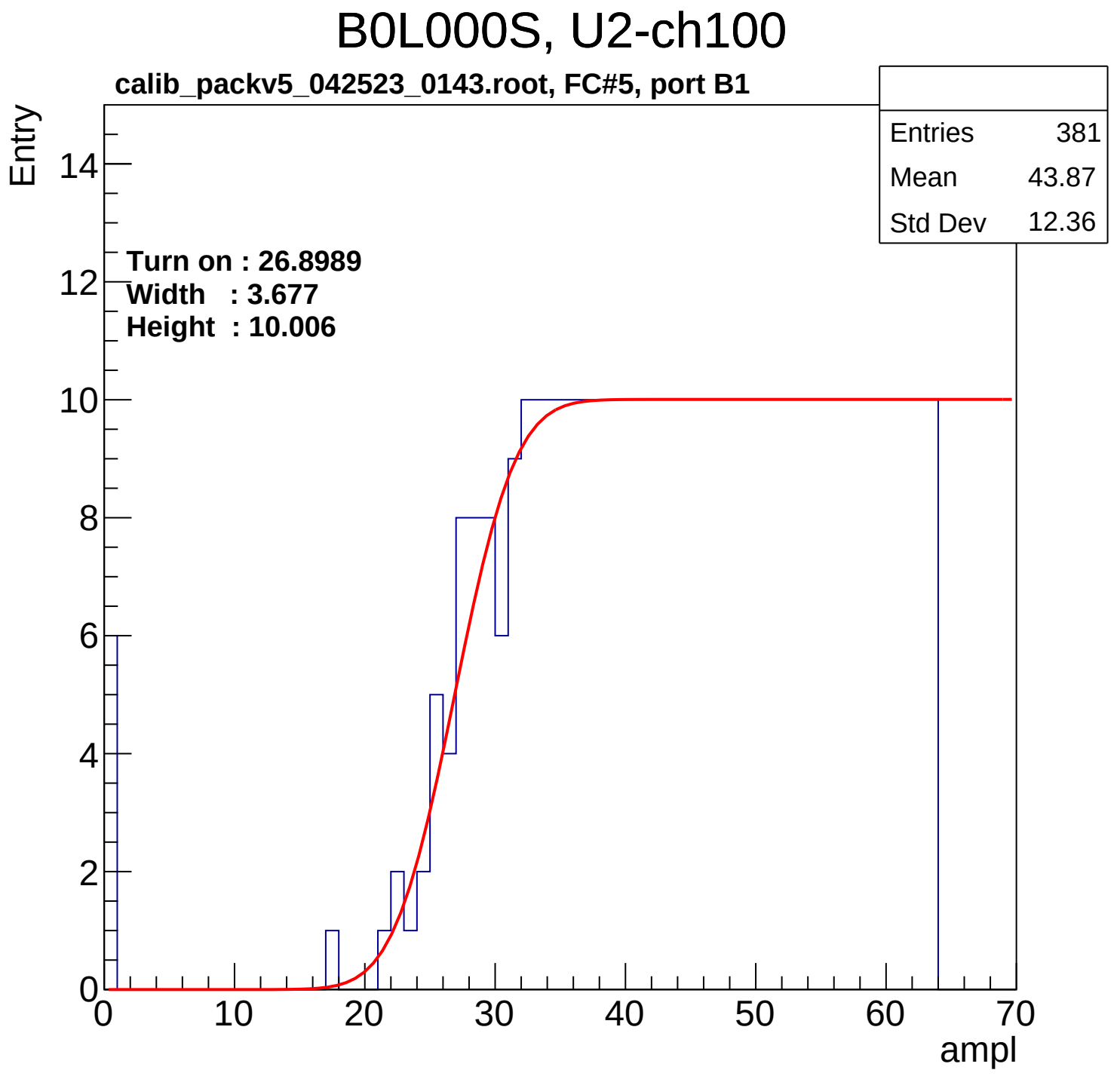
B0L000S, U2-ch100
calib_packv5_042523_0143.root, FC#5, port B1
Entries 381
Mean 43.87
Std Dev 12.36
Turn on : 26.8989
Width : 3.677
Height : 10.006
Entry
ampl
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8
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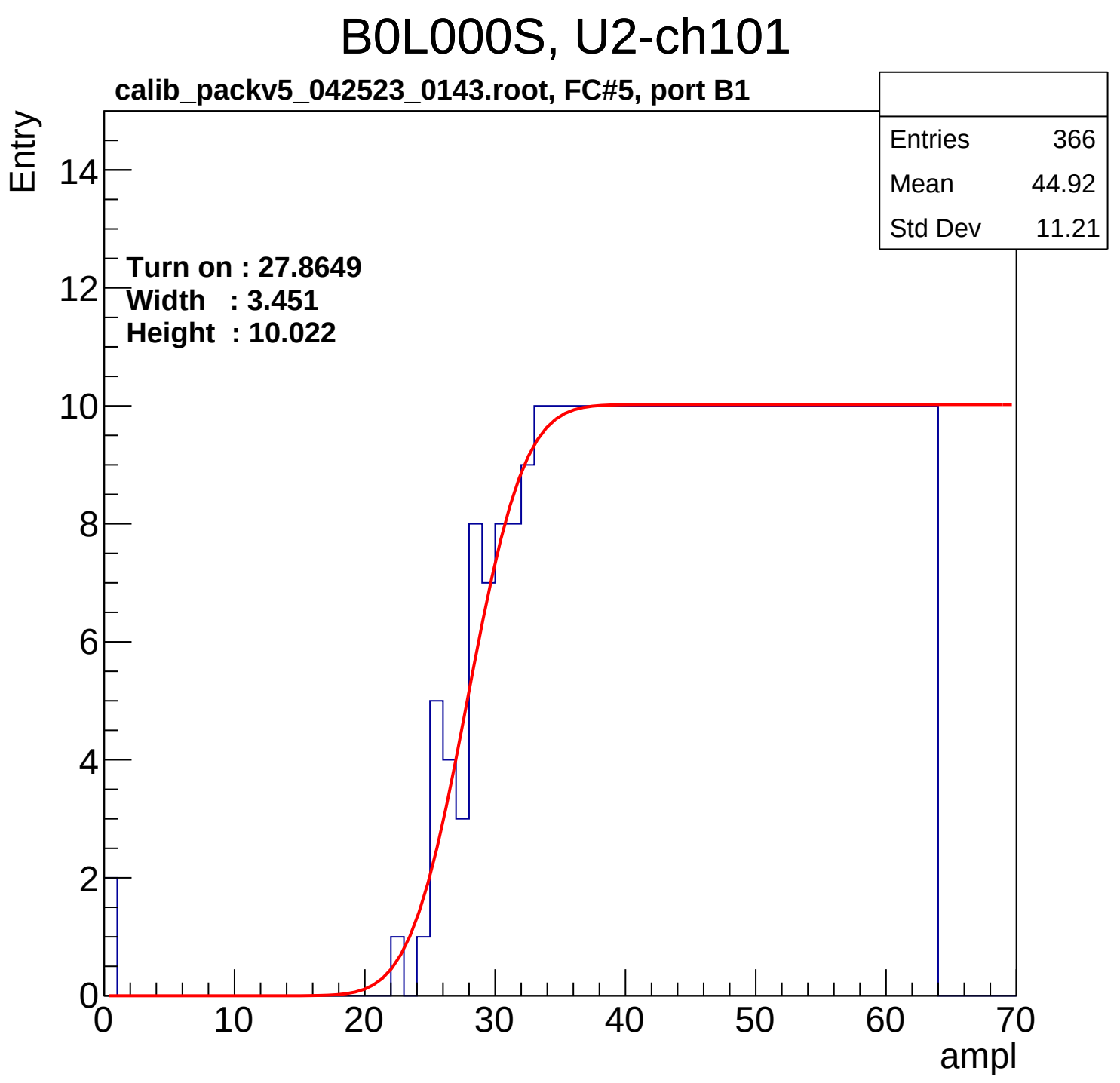
B0L000S, U2-ch101
calib_packv5_042523_0143.root, FC#5, port B1
Entries 366
Mean 44.92
Std Dev 11.21
Turn on : 27.8649
Width : 3.451
Height : 10.022
Entry
ampl
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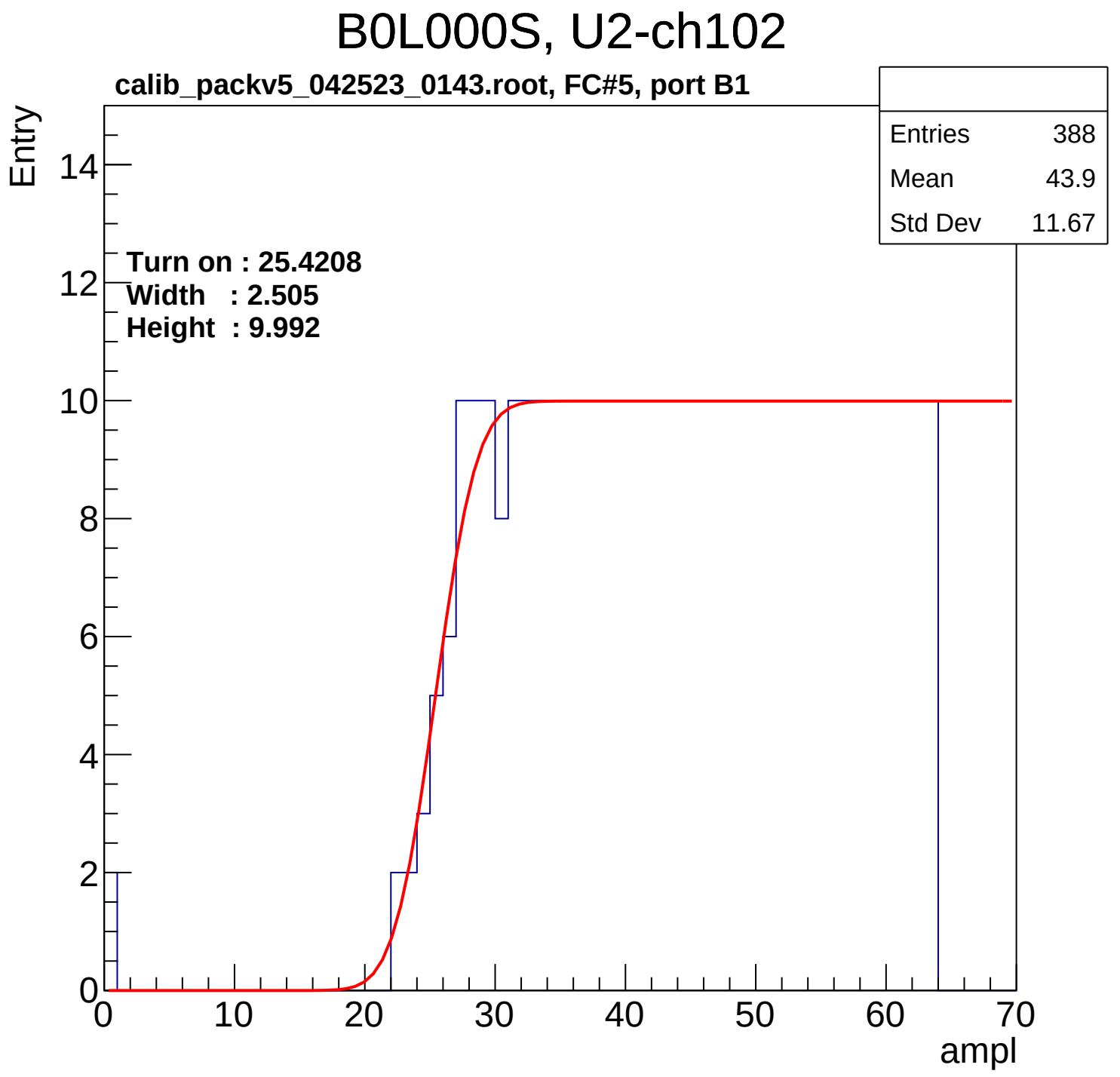
B0L000S, U2-ch102
calib_packv5_042523_0143.root, FC#5, port B1
Entries 388
Mean 43.9
Std Dev 11.67
Turn on : 25.4208
Width : 2.505
Height : 9.992
Entry
ampl
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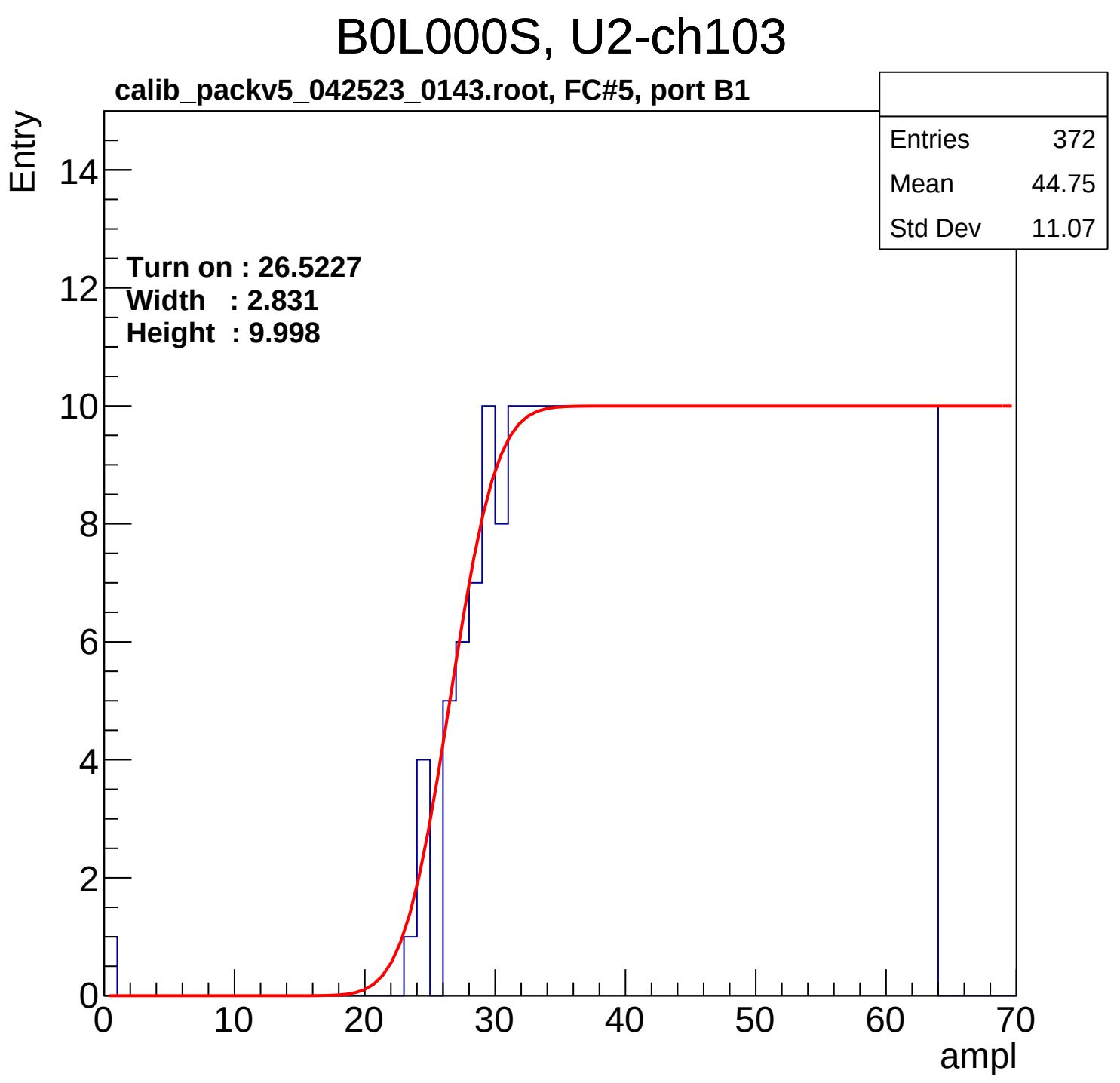
B0L000S, U2-ch103
calib_packv5_042523_0143.root, FC#5, port B1
Entries 372
Mean 44.75
Std Dev 11.07
Turn on : 26.5227
Width : 2.831
Height : 9.998
Entry
ampl
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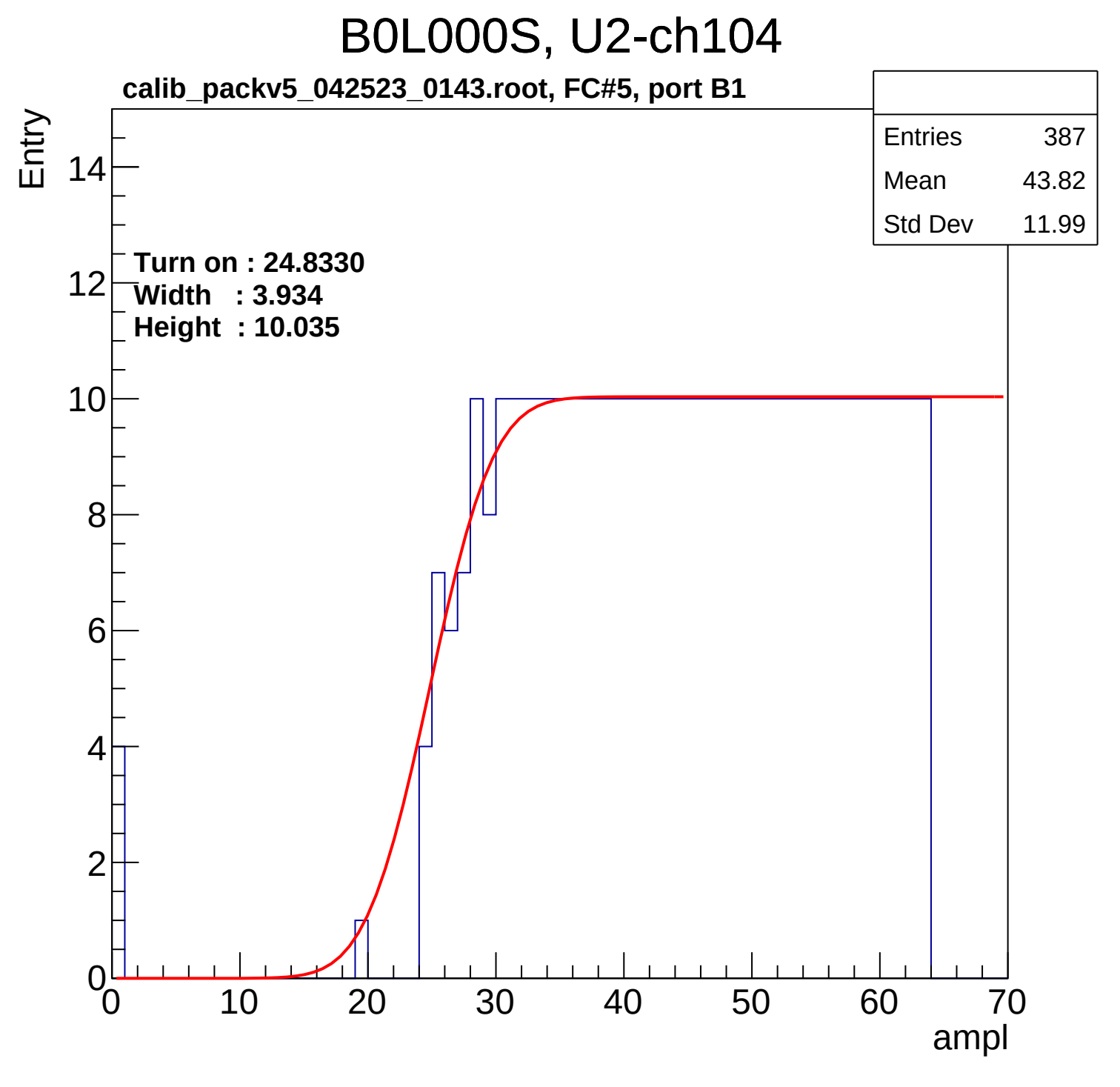
B0L000S, U2-ch104
calib_packv5_042523_0143.root, FC#5, port B1
Entries 387
Mean 43.82
Std Dev 11.99
Turn on : 24.8330
Width : 3.934
Height : 10.035
Entry
ampl
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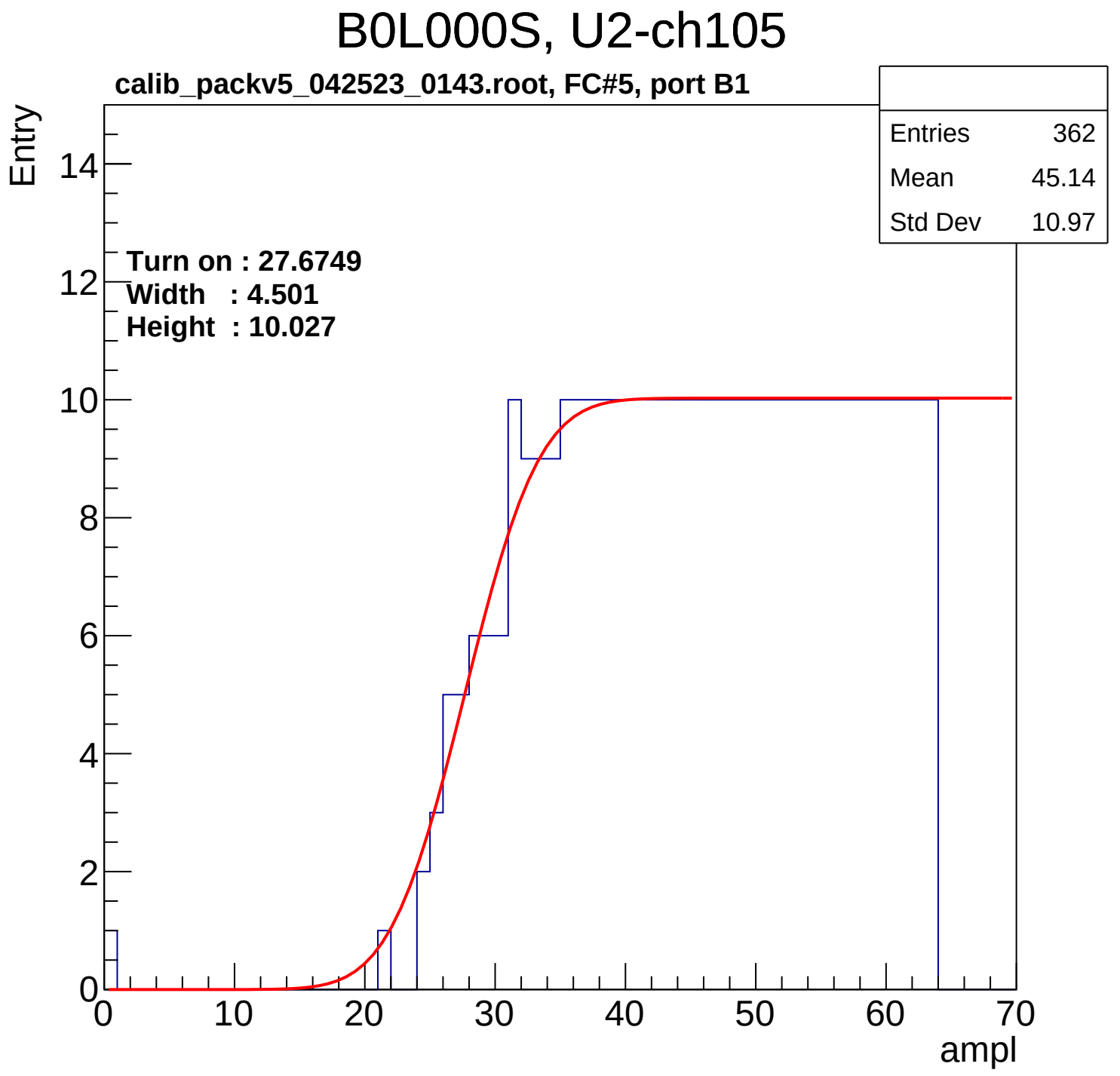
B0L000S, U2-ch105
calib_packv5_042523_0143.root, FC#5, port B1
Entries 362
Mean 45.14
Std Dev 10.97
Turn on : 27.6749
Width : 4.501
Height : 10.027
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ampl
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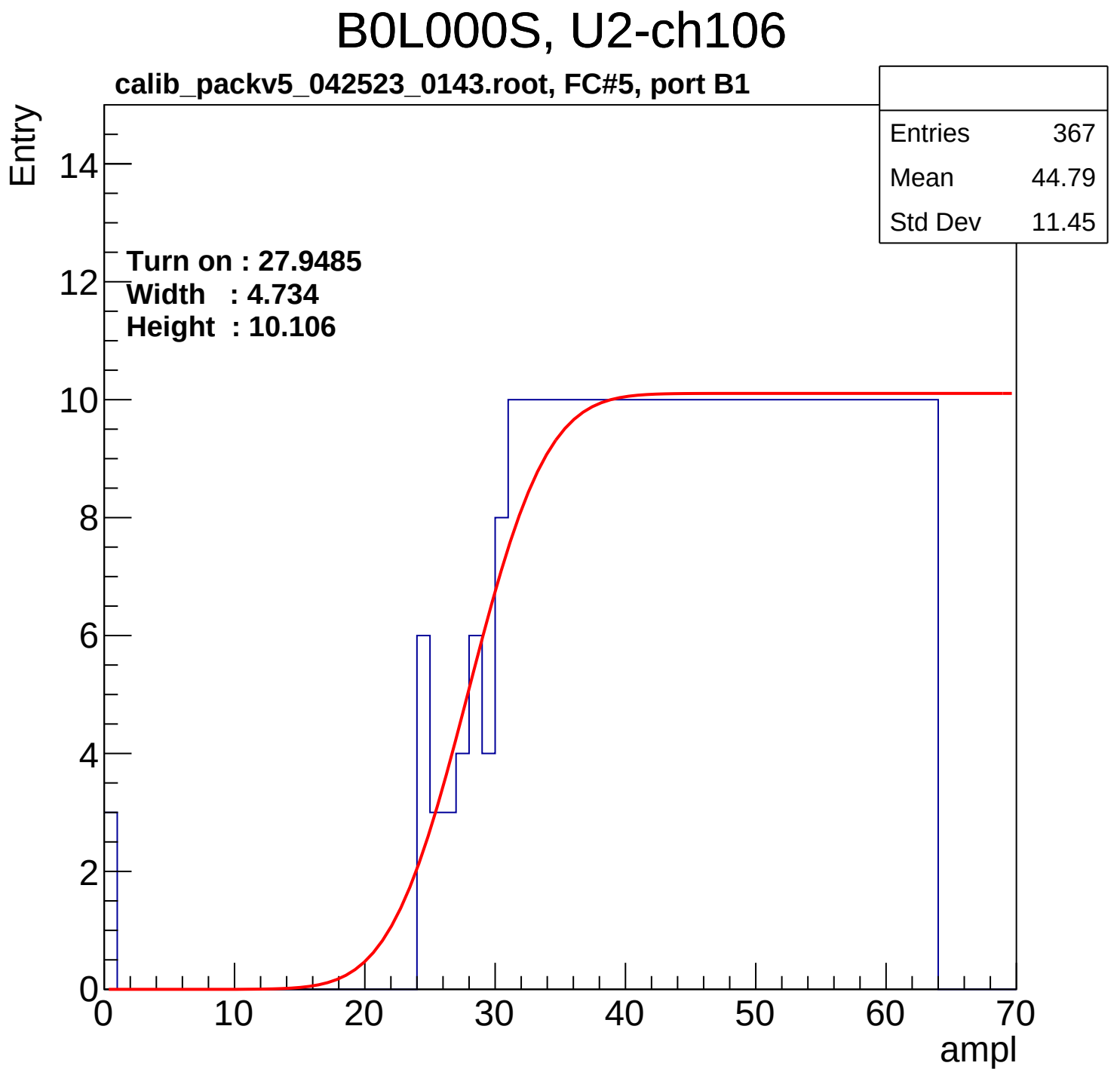
B0L000S, U2-ch106
calib_packv5_042523_0143.root, FC#5, port B1
Entries 367
Mean 44.79
Std Dev 11.45
Turn on : 27.9485
Width : 4.734
Height : 10.106
Entry
ampl
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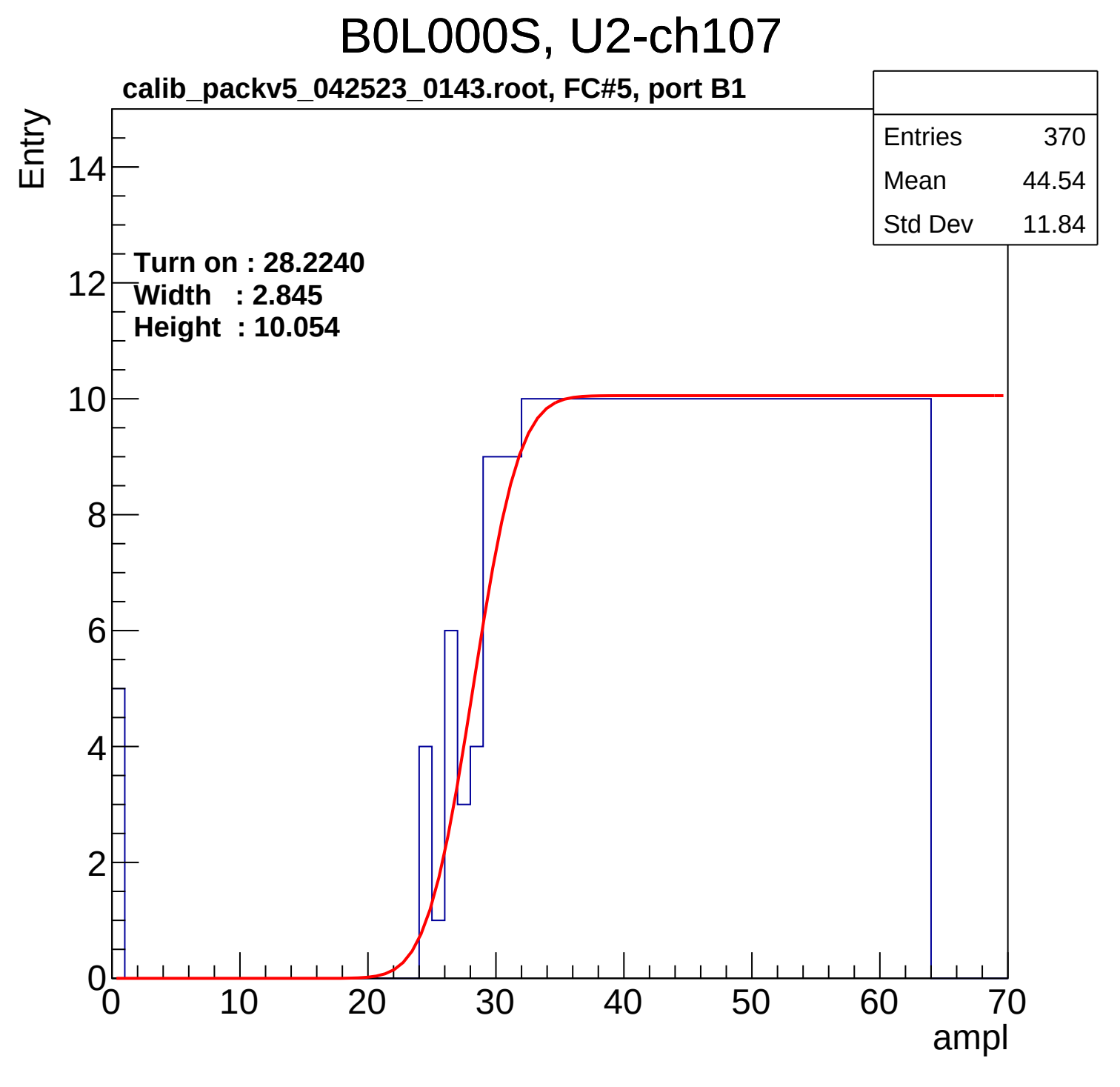
B0L000S, U2-ch107
calib_packv5_042523_0143.root, FC#5, port B1
Entries 370
Mean 44.54
Std Dev 11.84
Turn on : 28.2240
Width : 2.845
Height : 10.054
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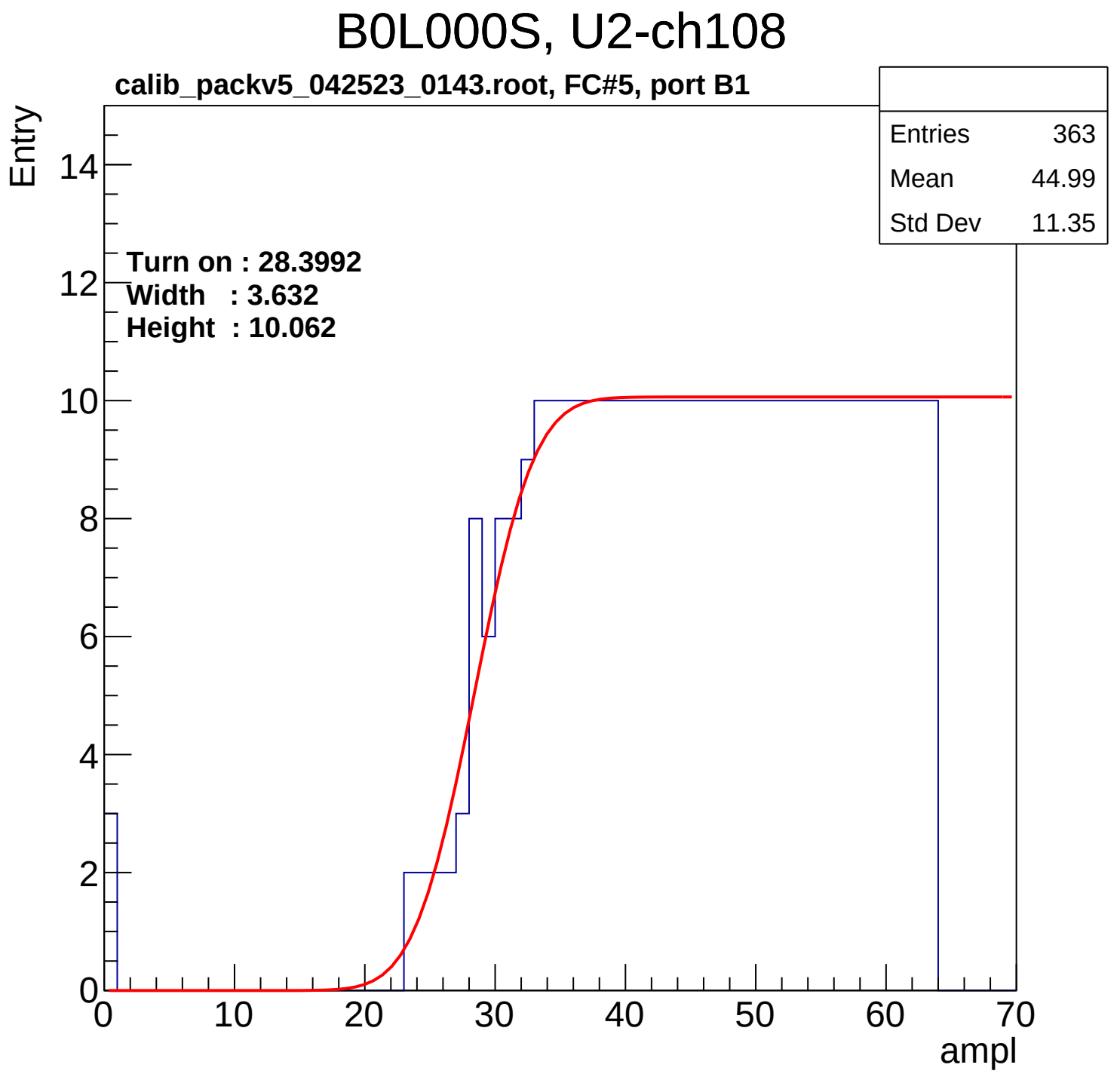
B0L000S, U2-ch108
calib_packv5_042523_0143.root, FC#5, port B1
Entries 363
Mean 44.99
Std Dev 11.35
Turn on : 28.3992
Width : 3.632
Height : 10.062
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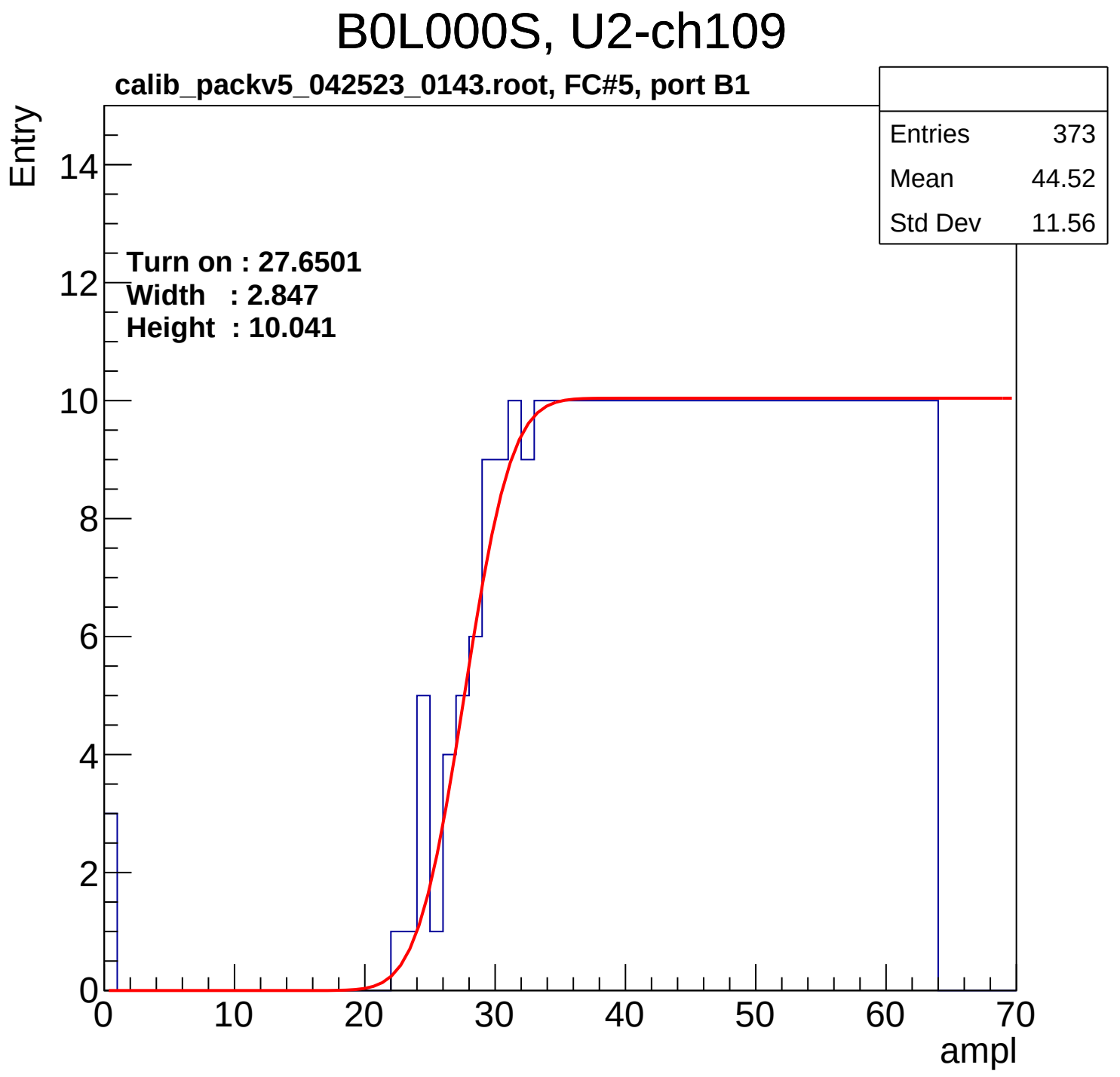
B0L000S, U2-ch109
calib_packv5_042523_0143.root, FC#5, port B1
Entries 373
Mean 44.52
Std Dev 11.56
Turn on : 27.6501
Width : 2.847
Height : 10.041
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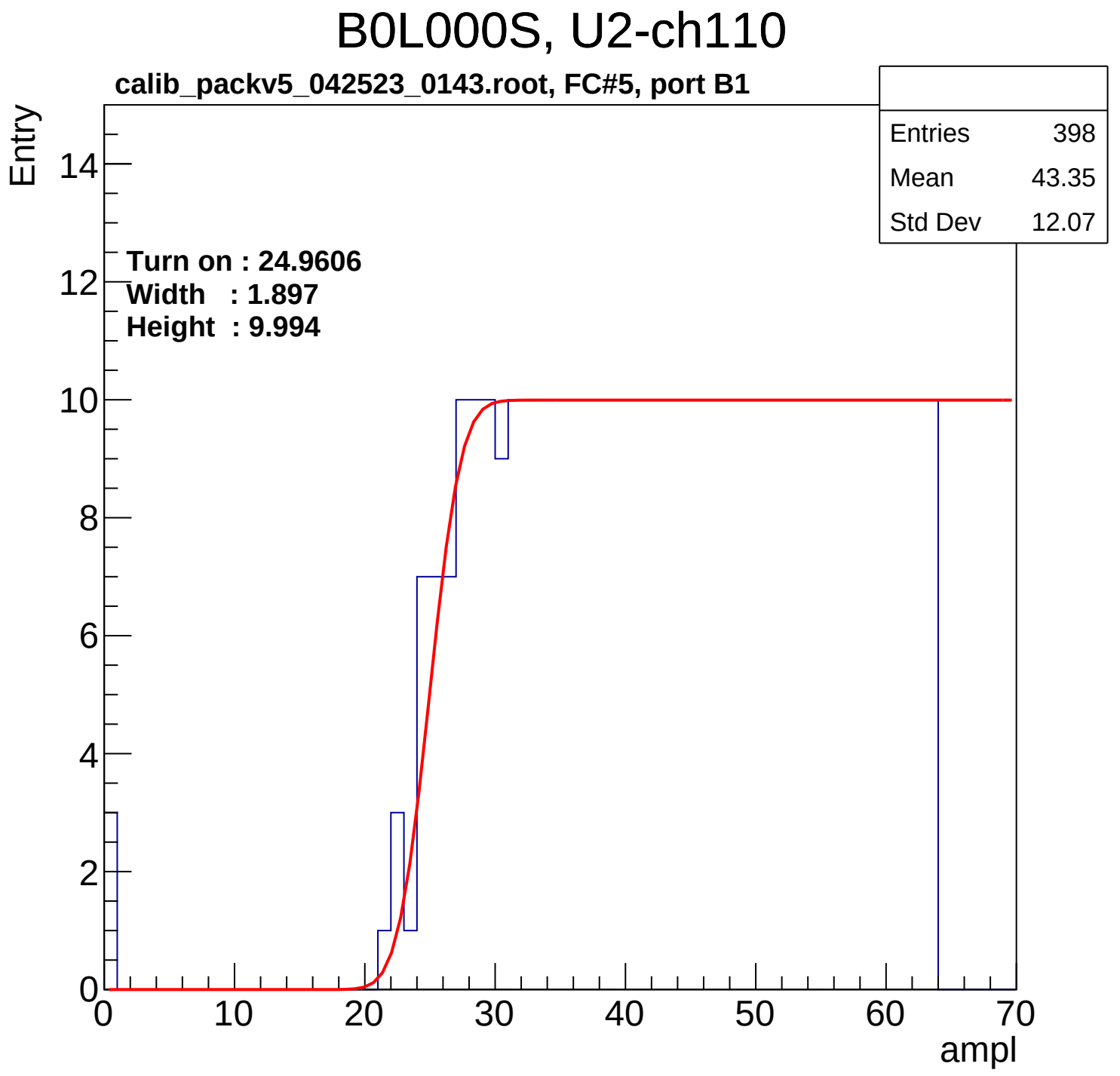
B0L000S, U2-ch110
calib_packv5_042523_0143.root, FC#5, port B1
Entries 398
Mean 43.35
Std Dev 12.07
Turn on : 24.9606
Width : 1.897
Height : 9.994
Entry
ampl
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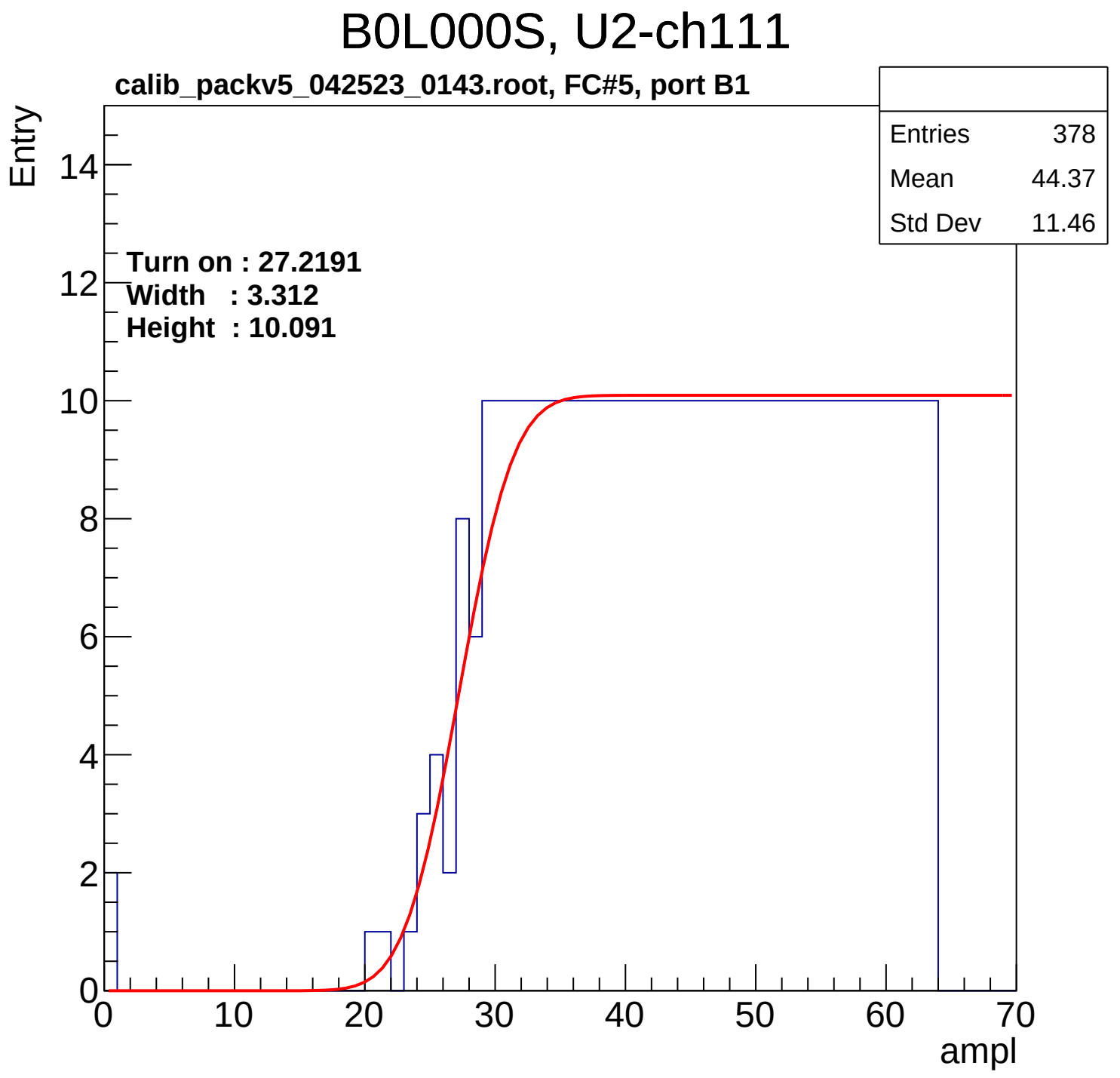
B0L000S, U2-ch111
calib_packv5_042523_0143.root, FC#5, port B1
Entries 378
Mean 44.37
Std Dev 11.46
Turn on : 27.2191
Width : 3.312
Height : 10.091
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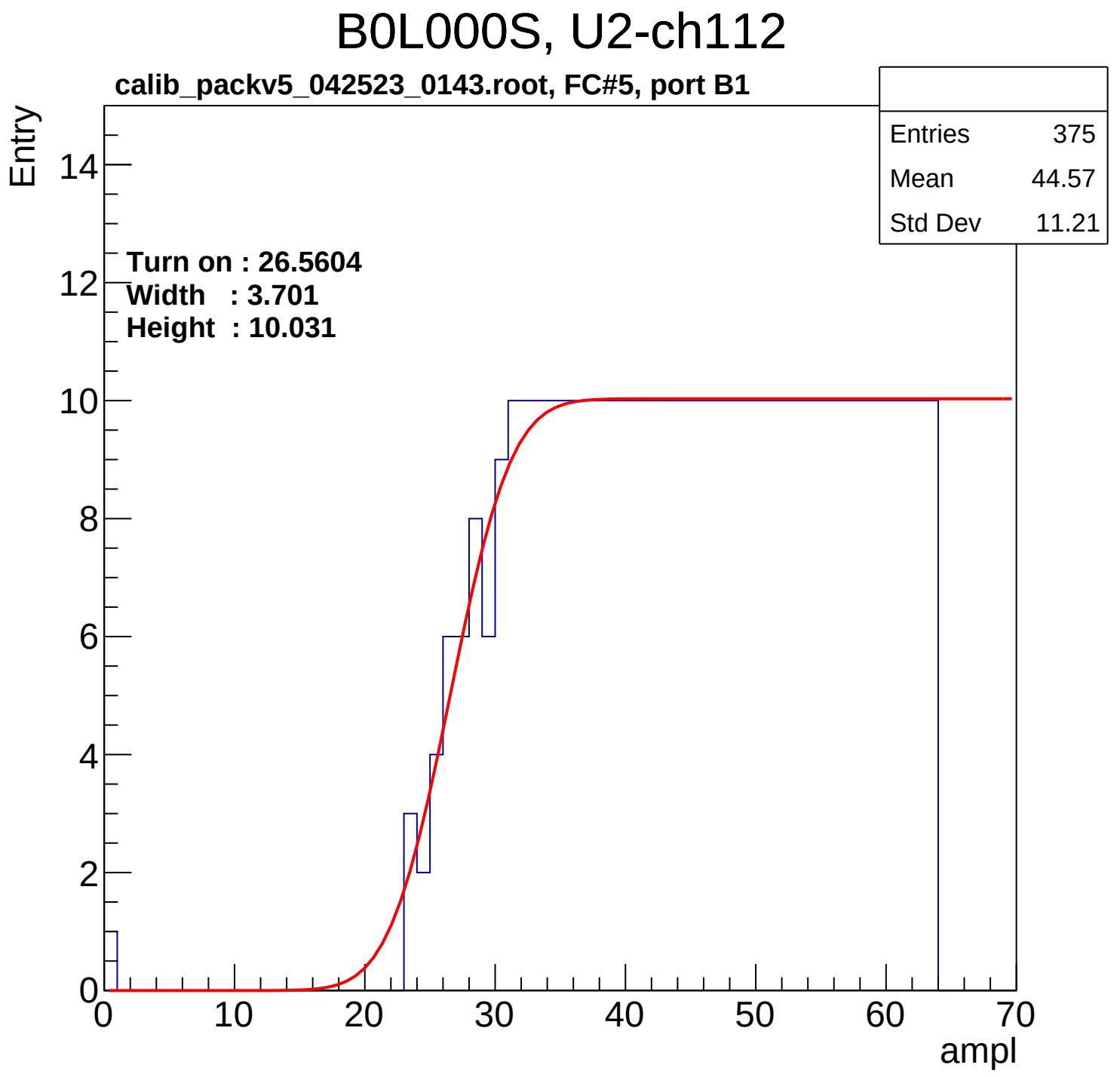
B0L000S, U2-ch112
calib_packv5_042523_0143.root, FC#5, port B1
Entries 375
Mean 44.57
Std Dev 11.21
Turn on : 26.5604
Width : 3.701
Height : 10.031
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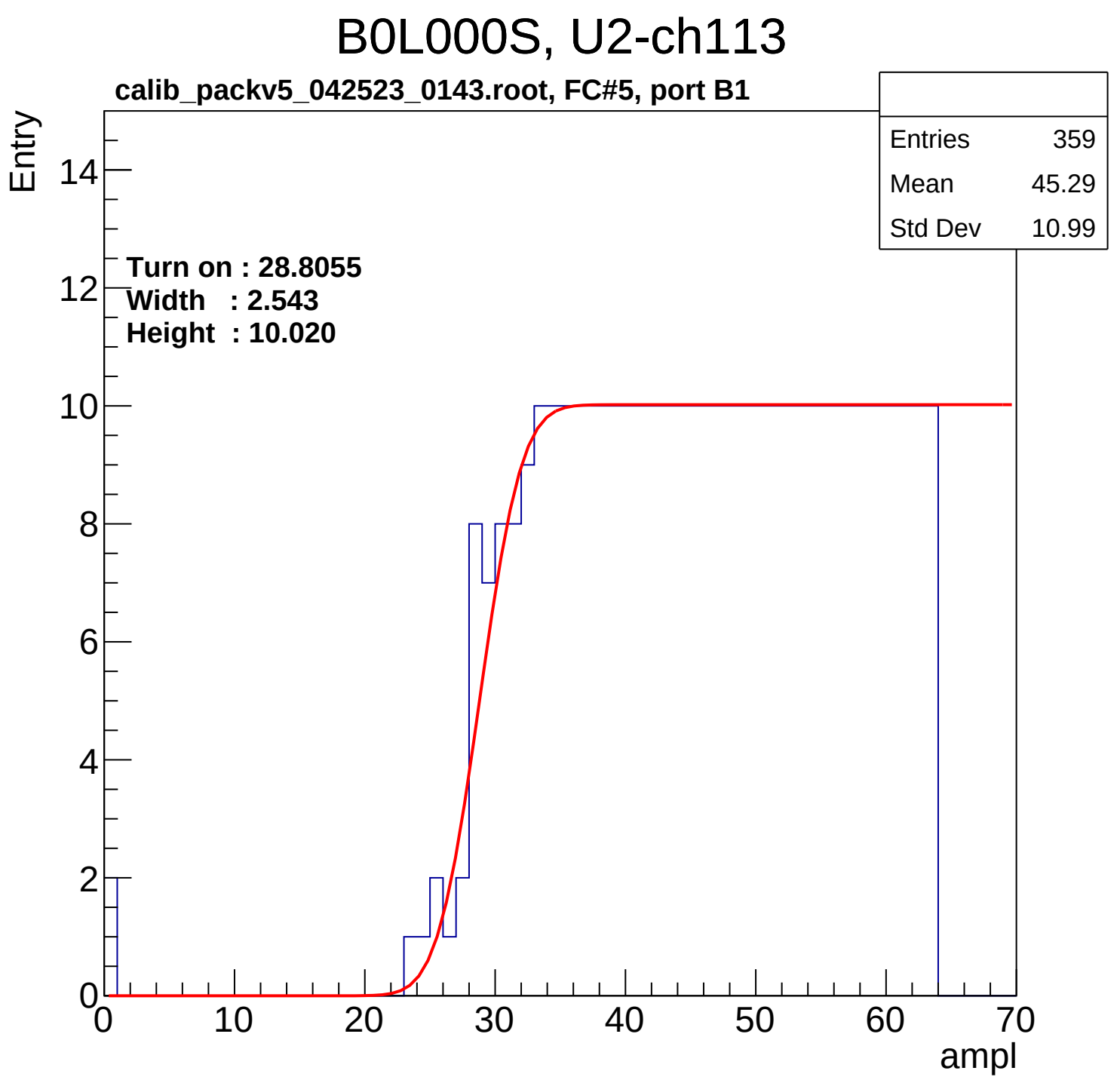
B0L000S, U2-ch113
calib_packv5_042523_0143.root, FC#5, port B1
Entries 359
Mean 45.29
Std Dev 10.99
Turn on : 28.8055
Width : 2.543
Height : 10.020
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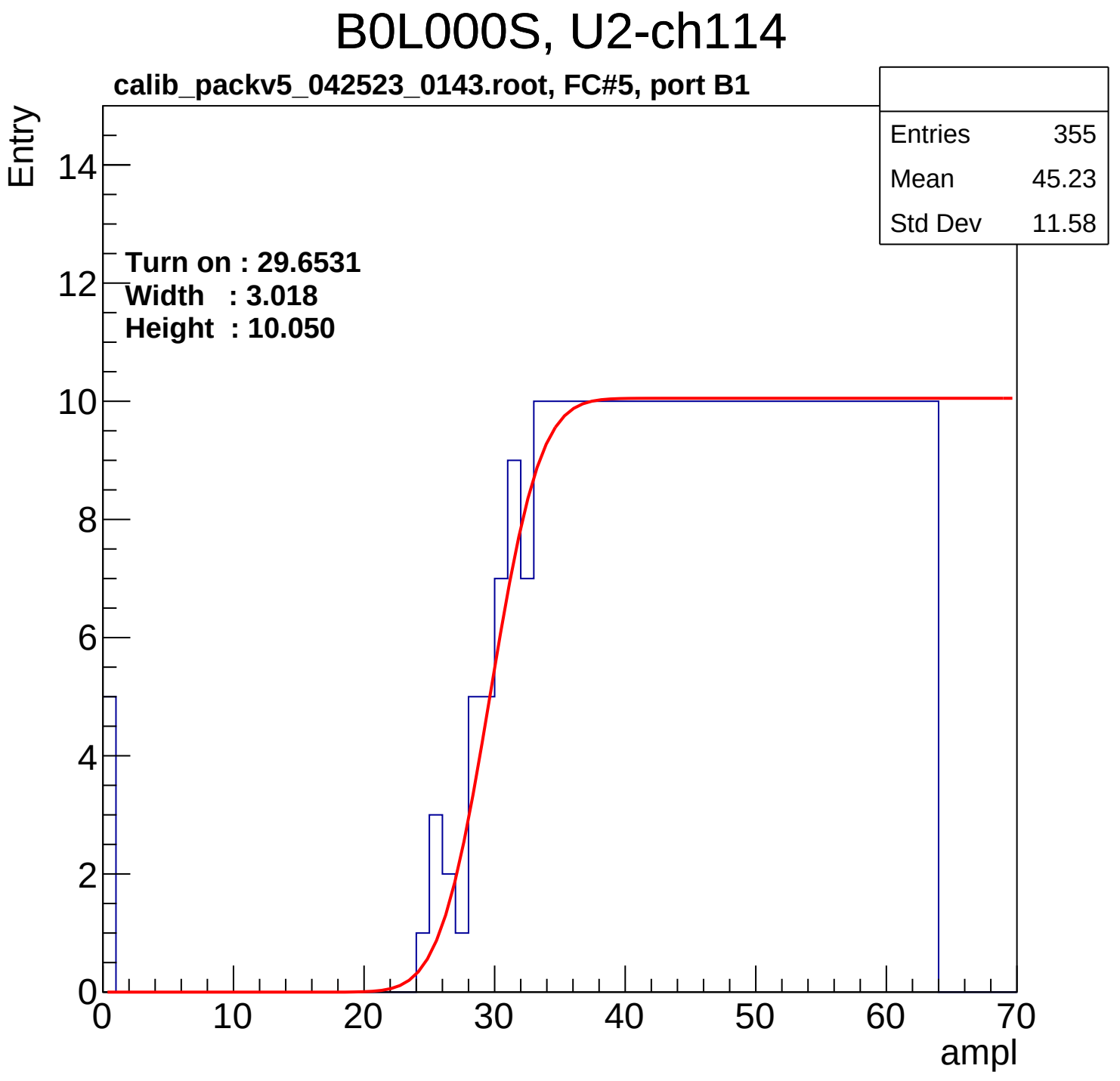
B0L000S, U2-ch114
calib_packv5_042523_0143.root, FC#5, port B1
Entries 355
Mean 45.23
Std Dev 11.58
Turn on : 29.6531
Width : 3.018
Height : 10.050
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ampl
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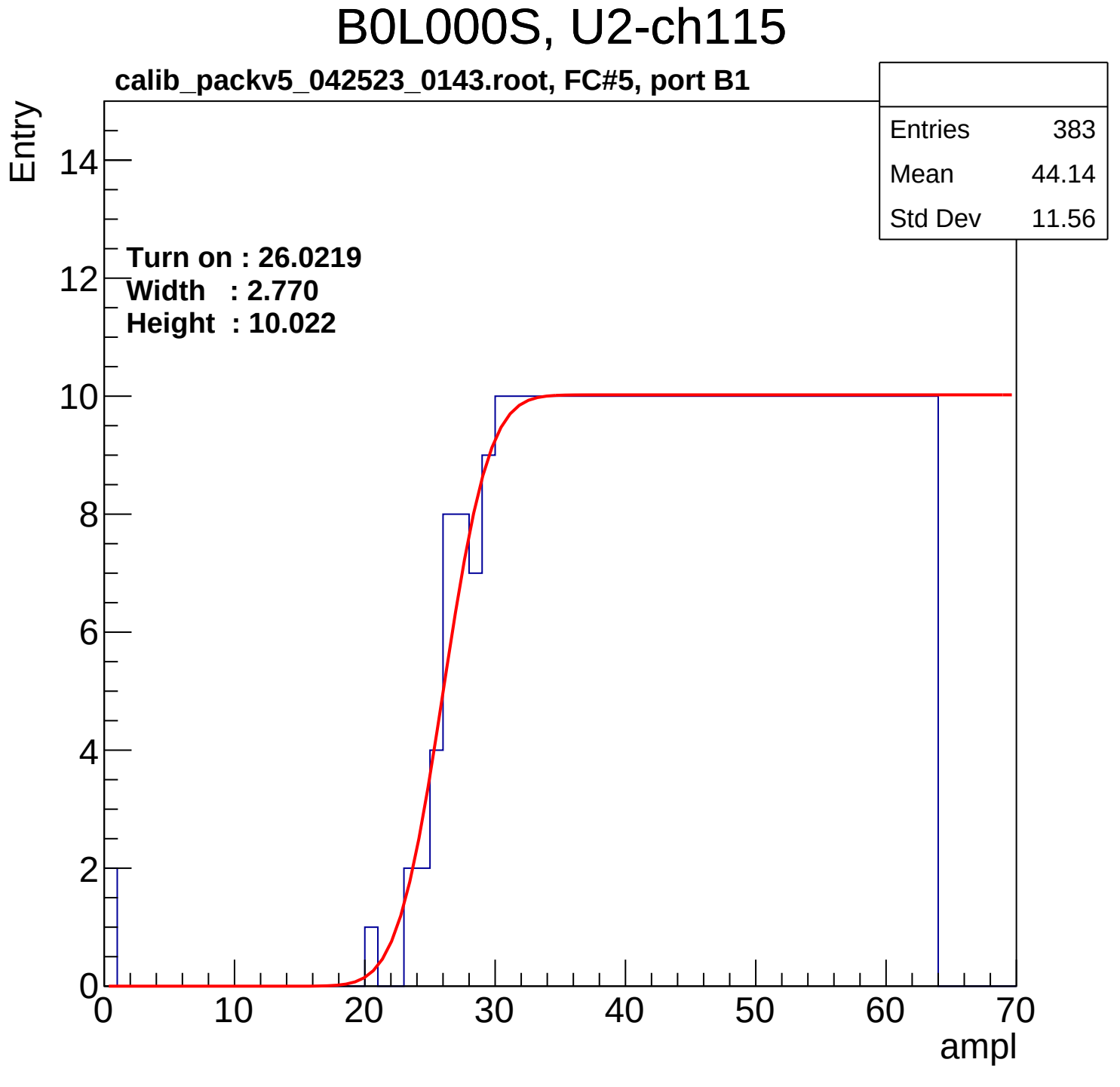
B0L000S, U2-ch115
calib_packv5_042523_0143.root, FC#5, port B1
Entries 383
Mean 44.14
Std Dev 11.56
Turn on : 26.0219
Width : 2.770
Height : 10.022
Entry
ampl
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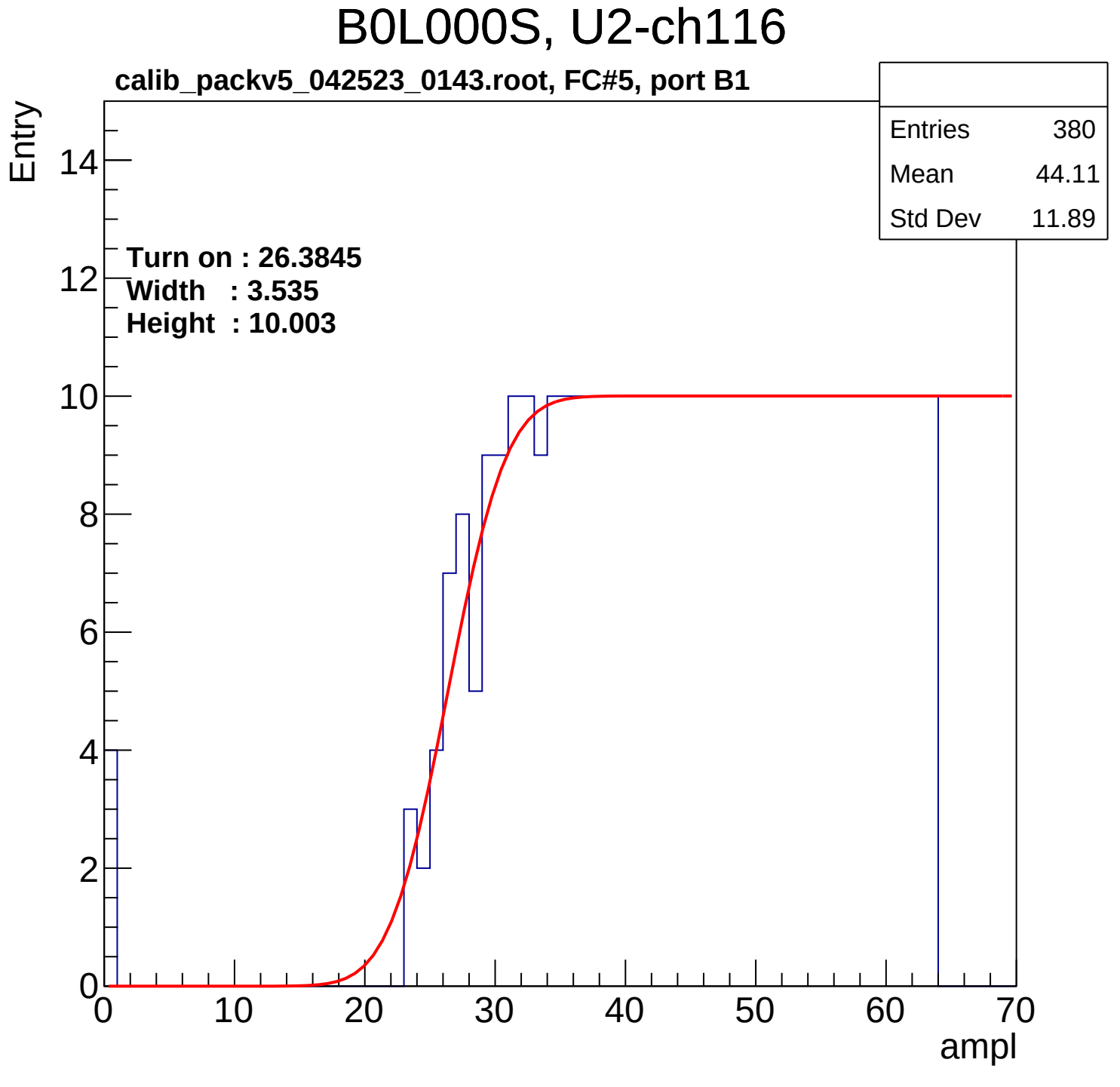
B0L000S, U2-ch116
calib_packv5_042523_0143.root, FC#5, port B1
Entries 380
Mean 44.11
Std Dev 11.89
Turn on : 26.3845
Width : 3.535
Height : 10.003
Entry
ampl
0
2
4
6
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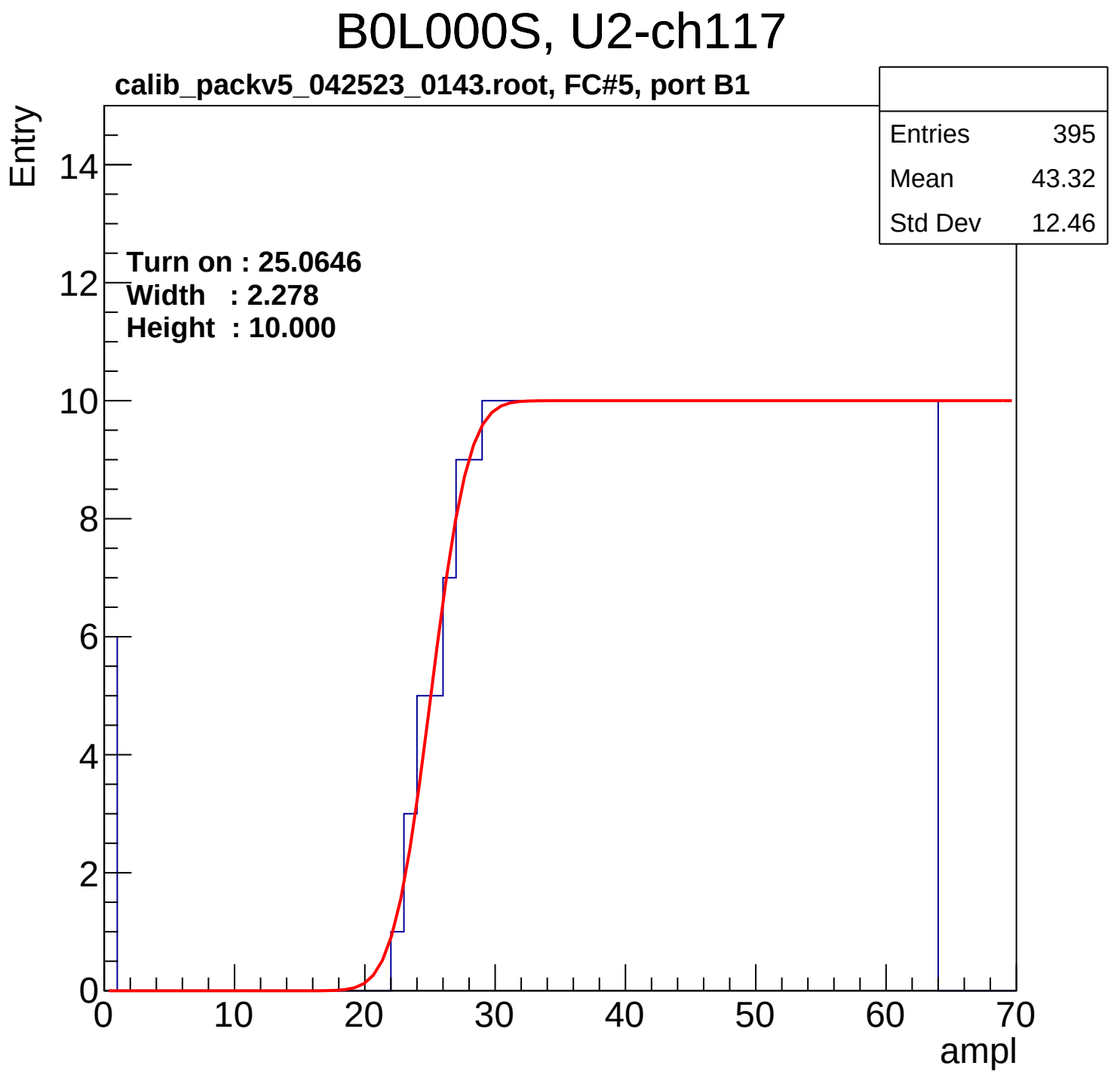
B0L000S, U2-ch117
calib_packv5_042523_0143.root, FC#5, port B1
Entries 395
Mean 43.32
Std Dev 12.46
Turn on : 25.0646
Width : 2.278
Height : 10.000
Entry
ampl
0
2
4
6
8
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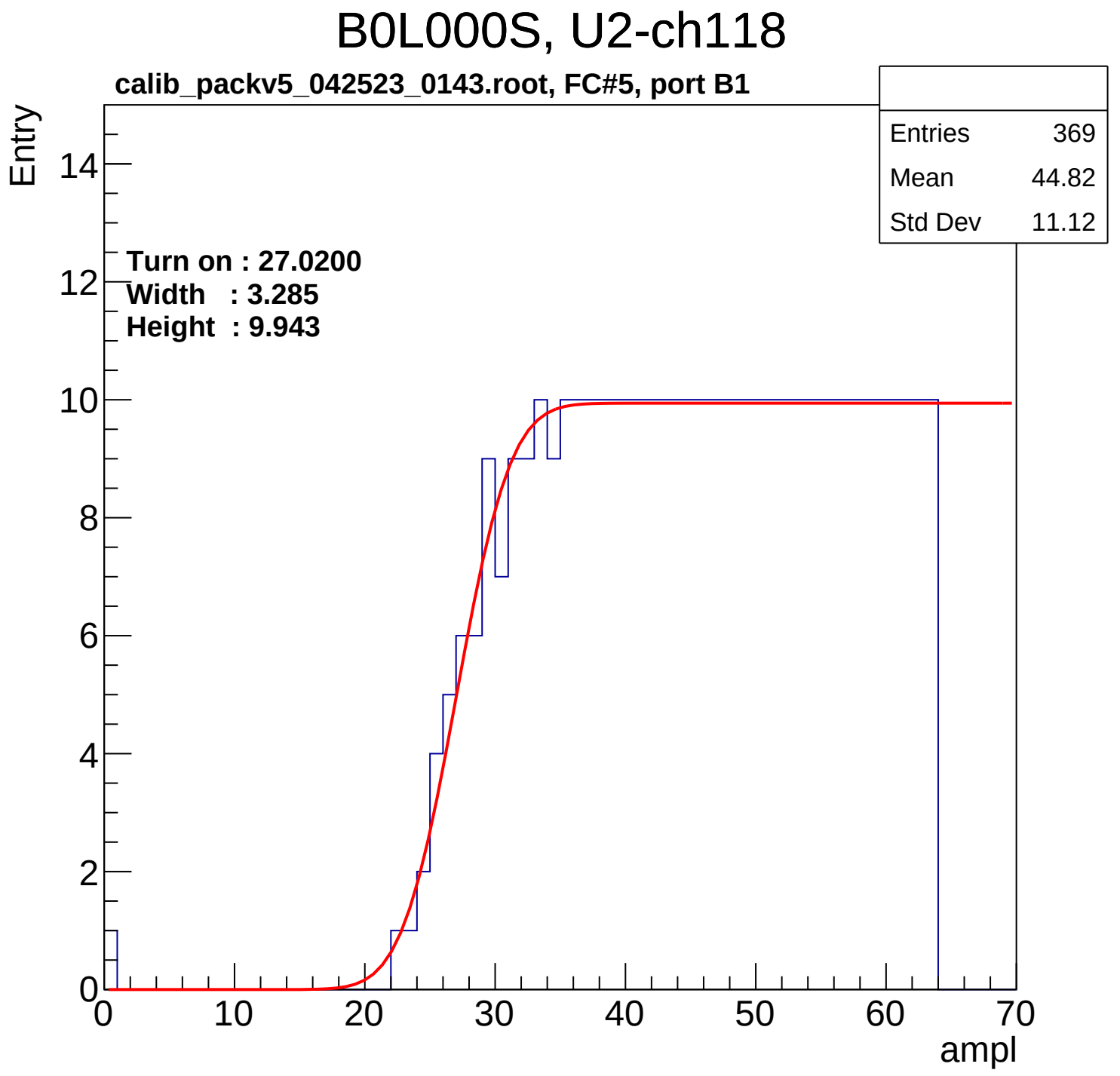
B0L000S, U2-ch118
calib_packv5_042523_0143.root, FC#5, port B1
Entries 369
Mean 44.82
Std Dev 11.12
Turn on : 27.0200
Width : 3.285
Height : 9.943
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
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60
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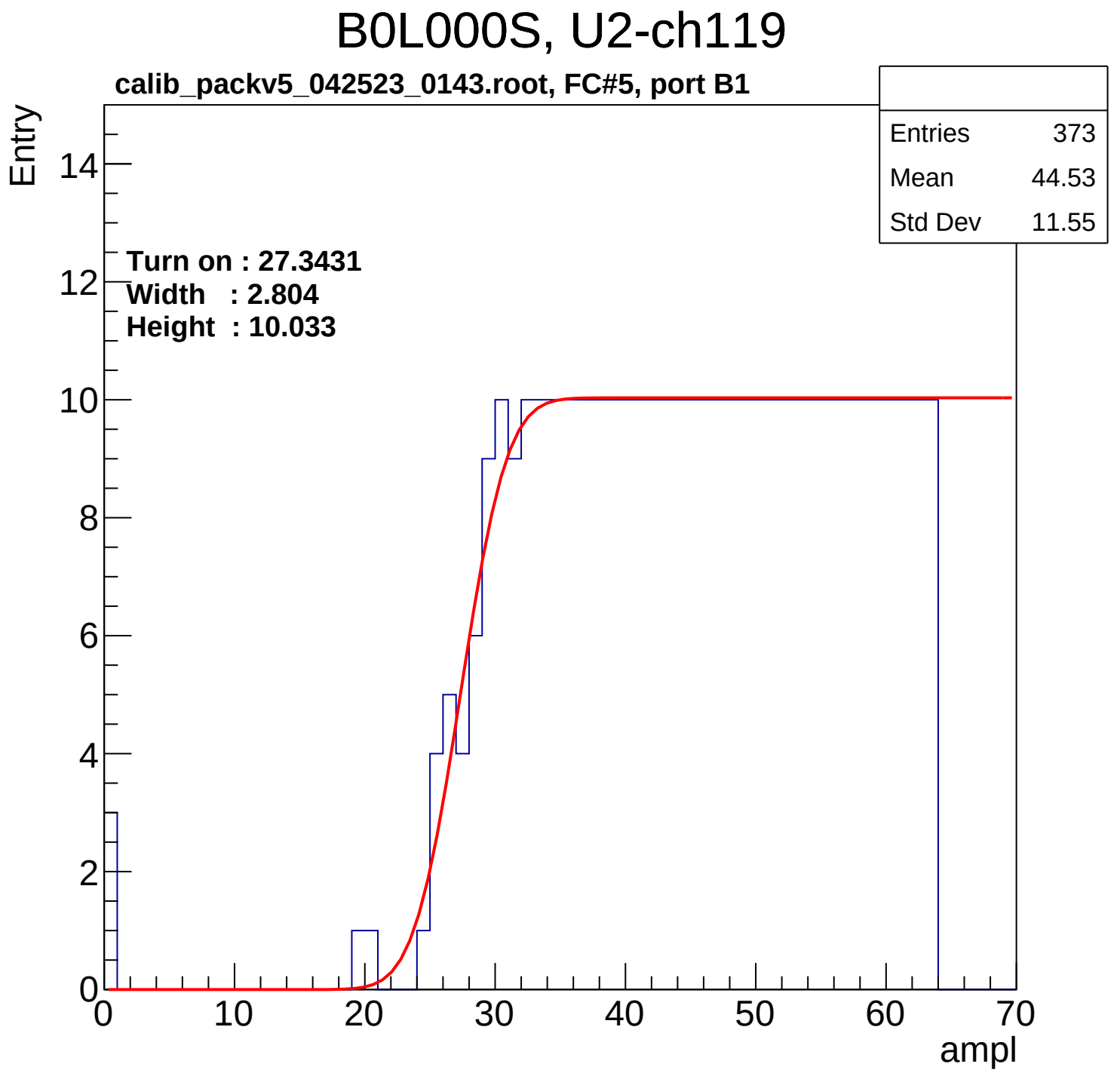
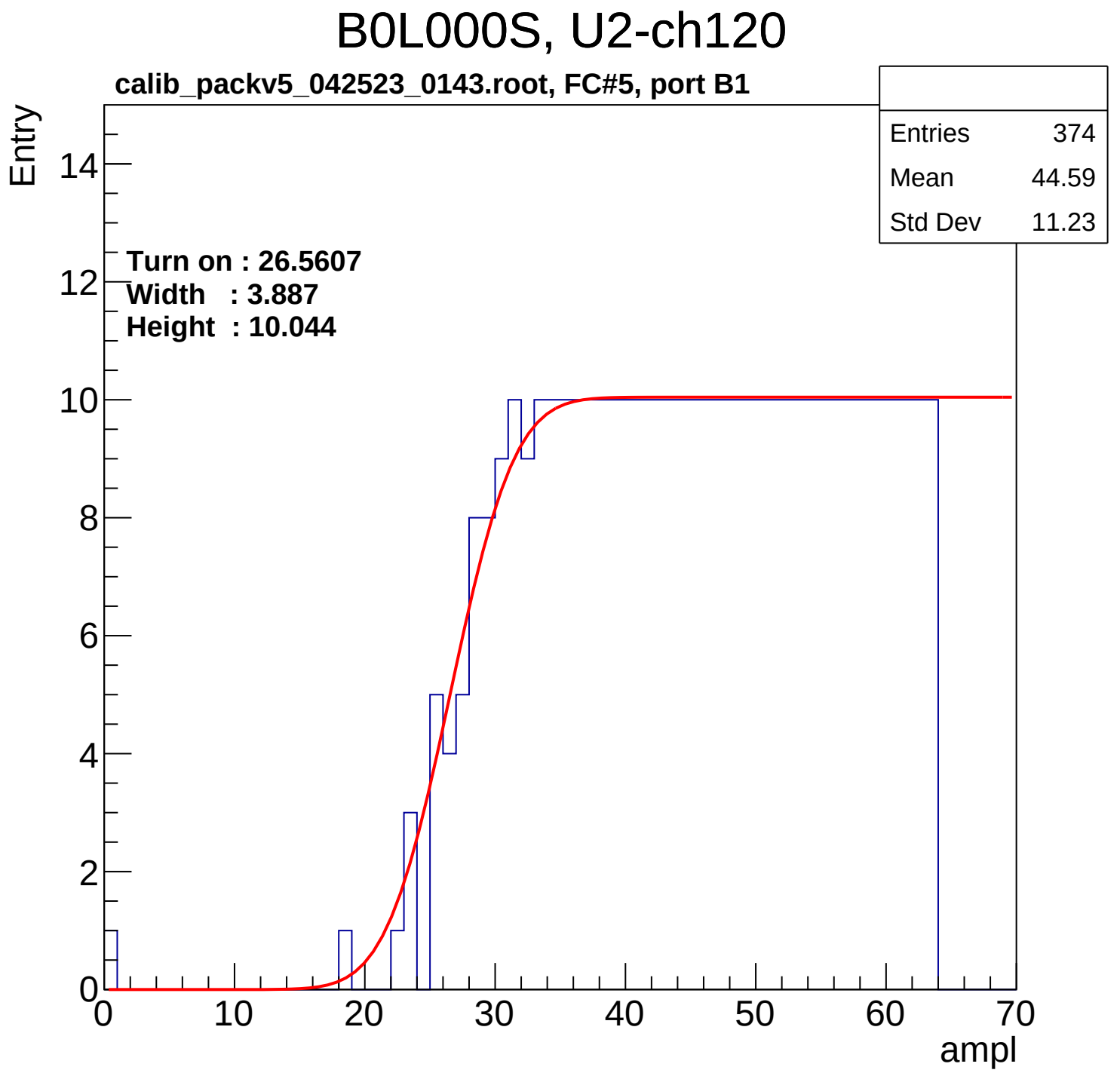

B0L000S, U2-ch119
calib_packv5_042523_0143.root, FC#5, port B1
Entries 373
Mean 44.53
Std Dev 11.55
Turn on : 27.3431
Width : 2.804
Height : 10.033
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L000S, U2-ch120
calib_packv5_042523_0143.root, FC#5, port B1
Entries 374
Mean 44.59
Std Dev 11.23
Turn on : 26.5607
Width : 3.887
Height : 10.044
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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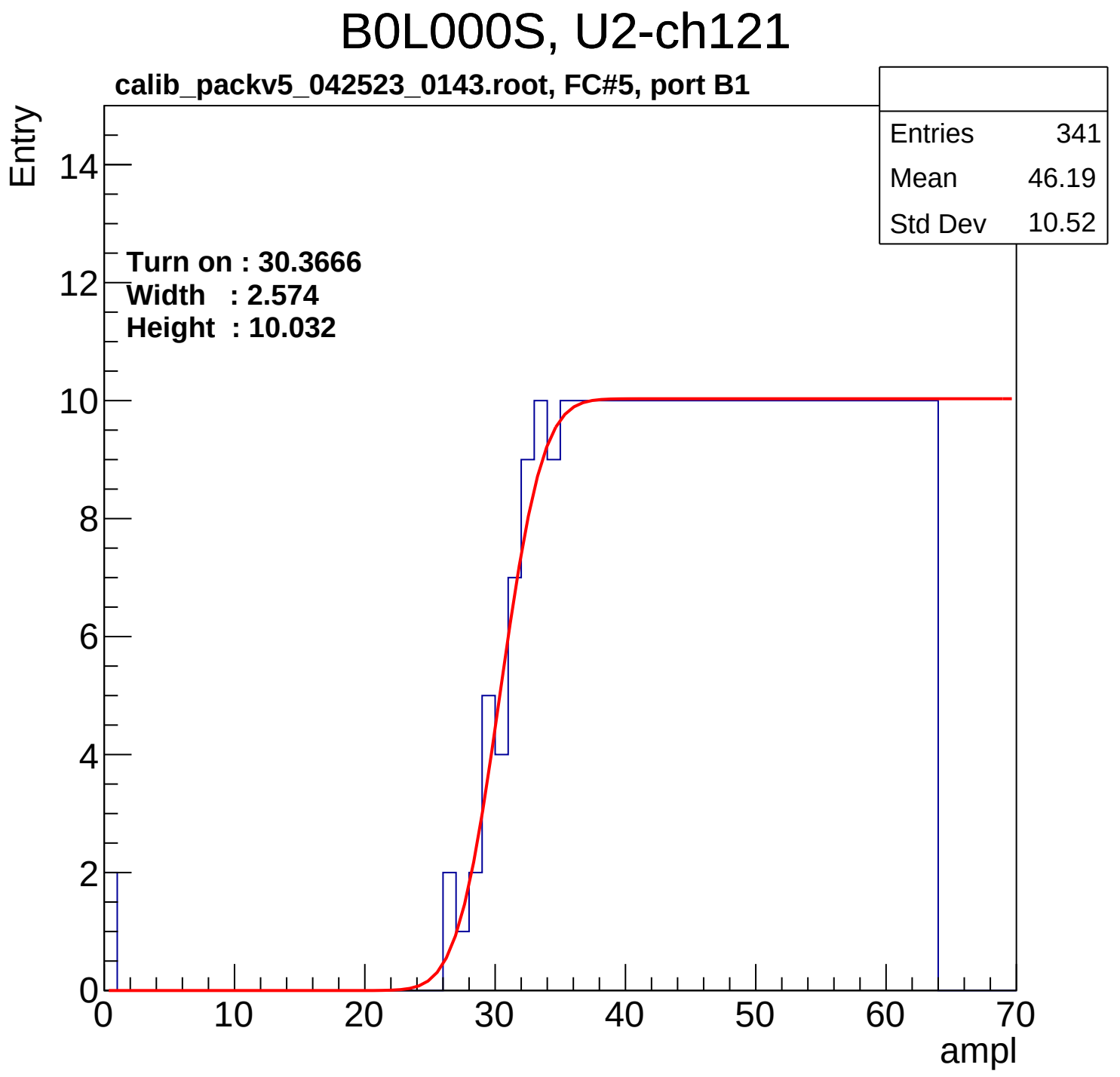
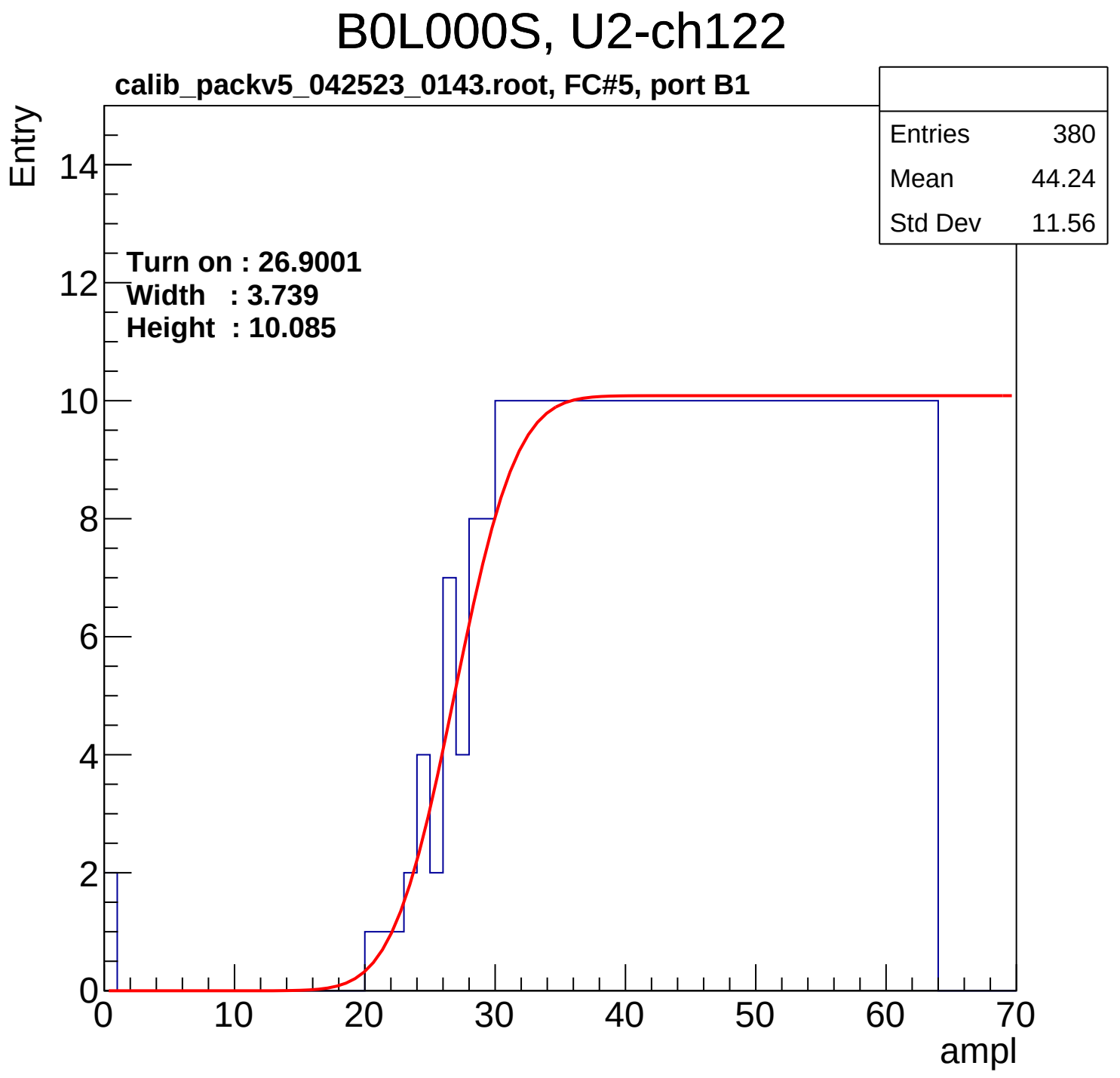

B0L000S, U2-ch121
calib_packv5_042523_0143.root, FC#5, port B1
Entries 341
Mean 46.19
Std Dev 10.52
Turn on : 30.3666
Width : 2.574
Height : 10.032
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L000S, U2-ch122
calib_packv5_042523_0143.root, FC#5, port B1
Entries 380
Mean 44.24
Std Dev 11.56
Turn on : 26.9001
Width : 3.739
Height : 10.085
Entry
ampl
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6
8
10
12
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0
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40
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60
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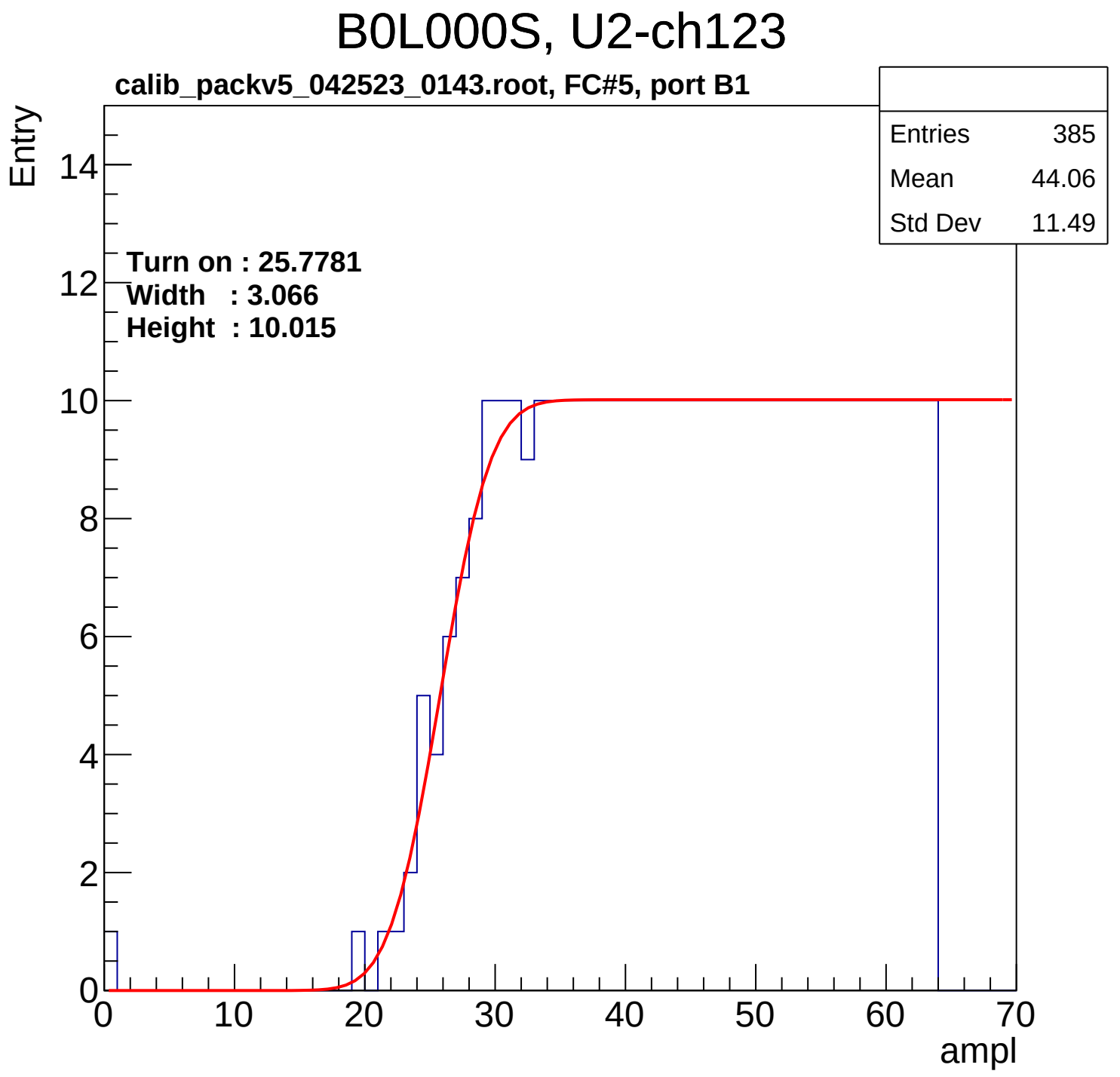
B0L000S, U2-ch123
calib_packv5_042523_0143.root, FC#5, port B1
Entries 385
Mean 44.06
Std Dev 11.49
Turn on : 25.7781
Width : 3.066
Height : 10.015
Entry
ampl
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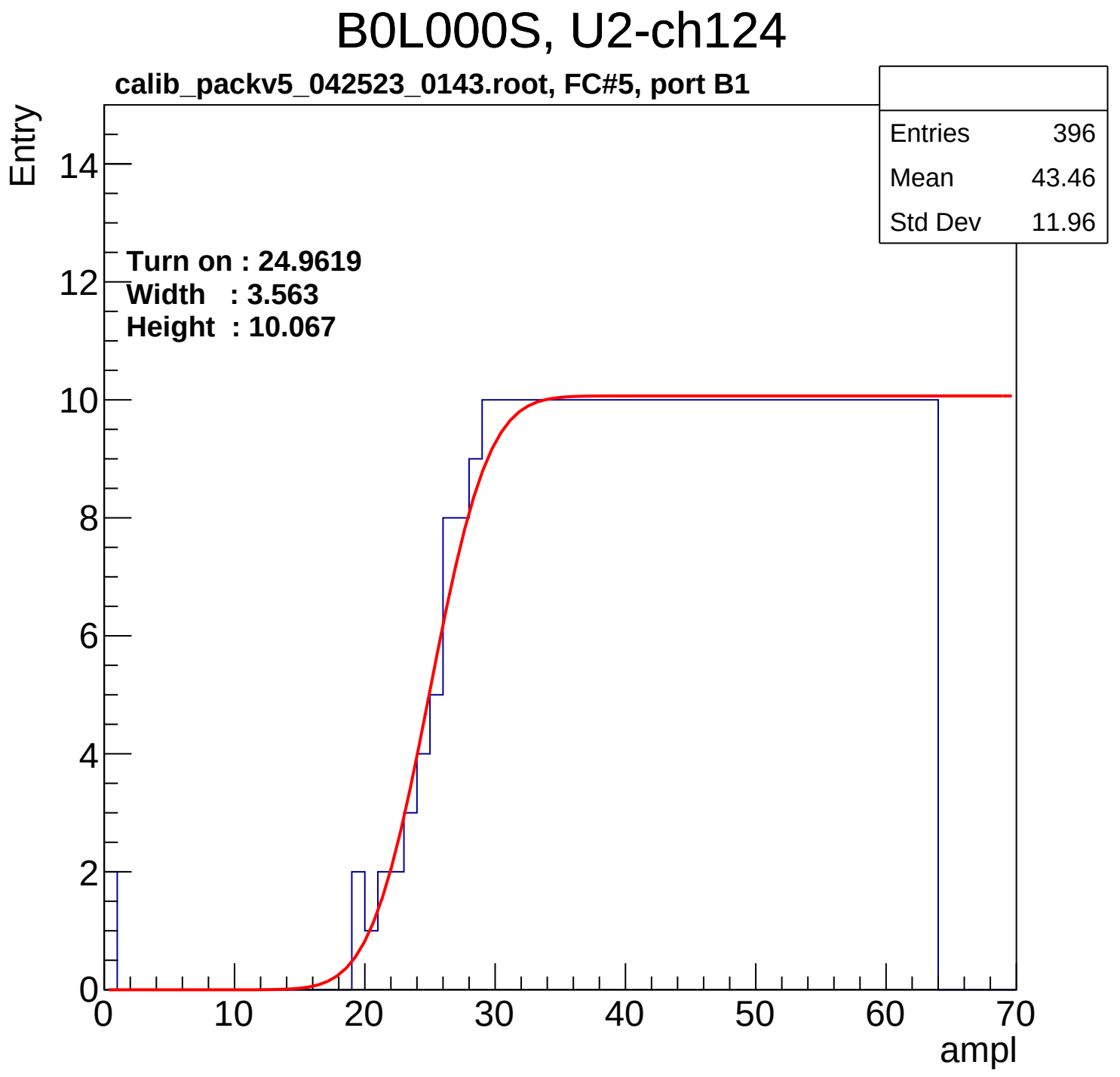
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L000S, U2-ch124
calib_packv5_042523_0143.root, FC#5, port B1
Entries 396
Mean 43.46
Std Dev 11.96
Turn on : 24.9619
Width : 3.563
Height : 10.067
Entry
ampl
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4
6
8
10
12
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0
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20
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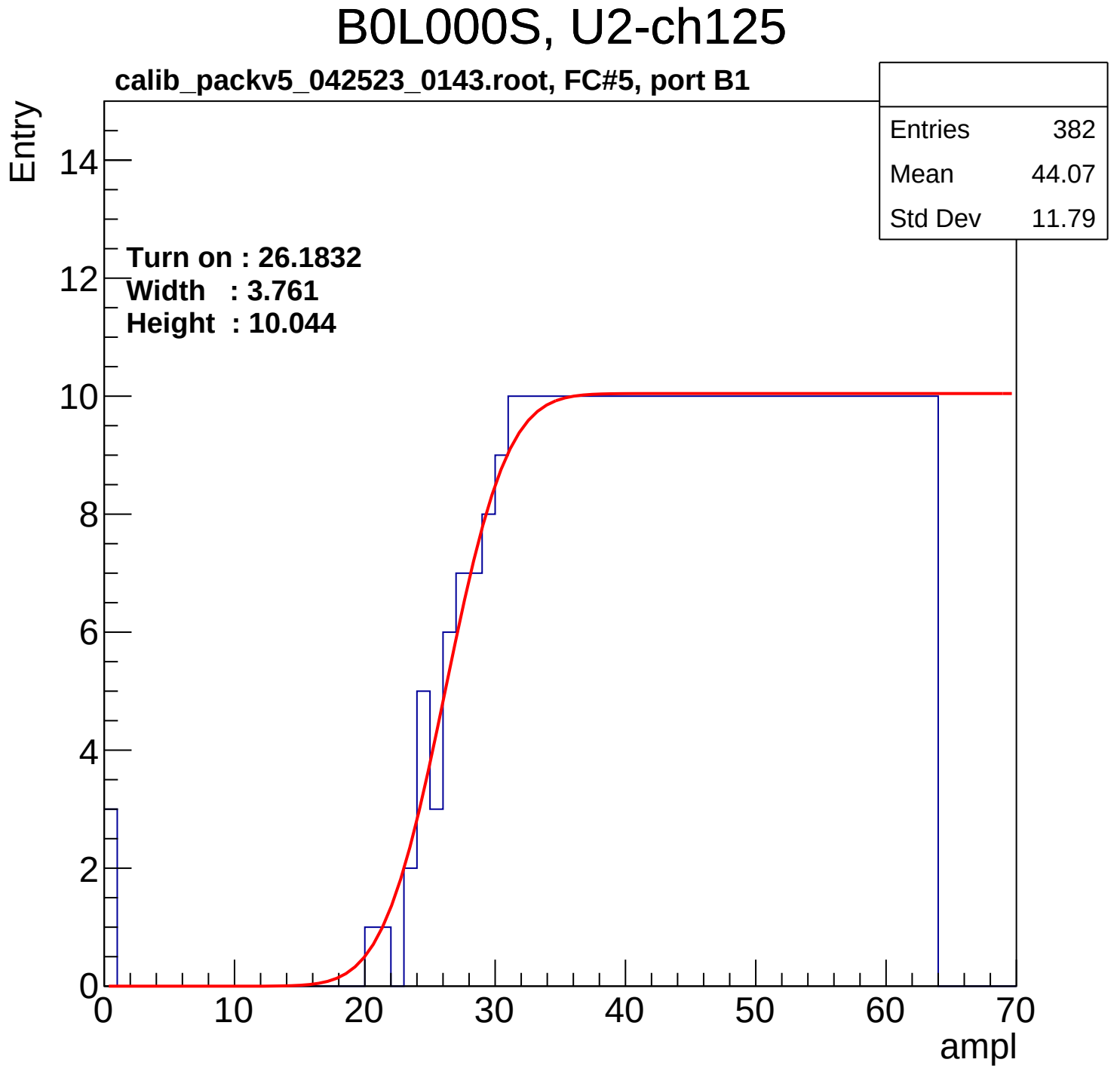
40
50
60
70


B0L000S, U2-ch125
calib_packv5_042523_0143.root, FC#5, port B1
Entries 382
Mean 44.07
Std Dev 11.79
Turn on : 26.1832
Width : 3.761
Height : 10.044
Entry
ampl
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2
4
6
8
10
12
14
0
10
20
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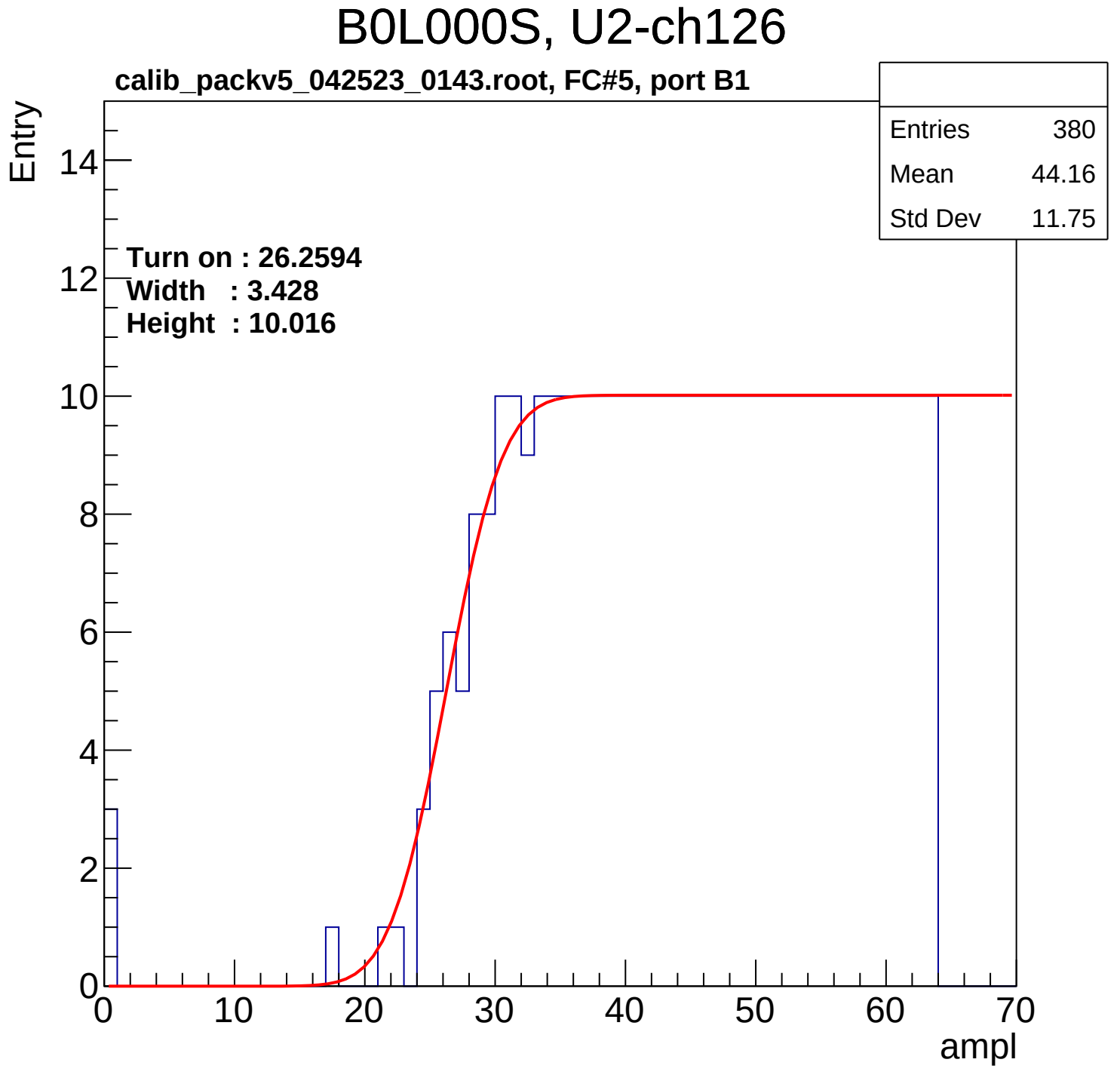
40
50
60
70


B0L000S, U2-ch126
calib_packv5_042523_0143.root, FC#5, port B1
Entries 380
Mean 44.16
Std Dev 11.75
Turn on : 26.2594
Width : 3.428
Height : 10.016
Entry
ampl
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2
4
6
8
10
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0
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20
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60
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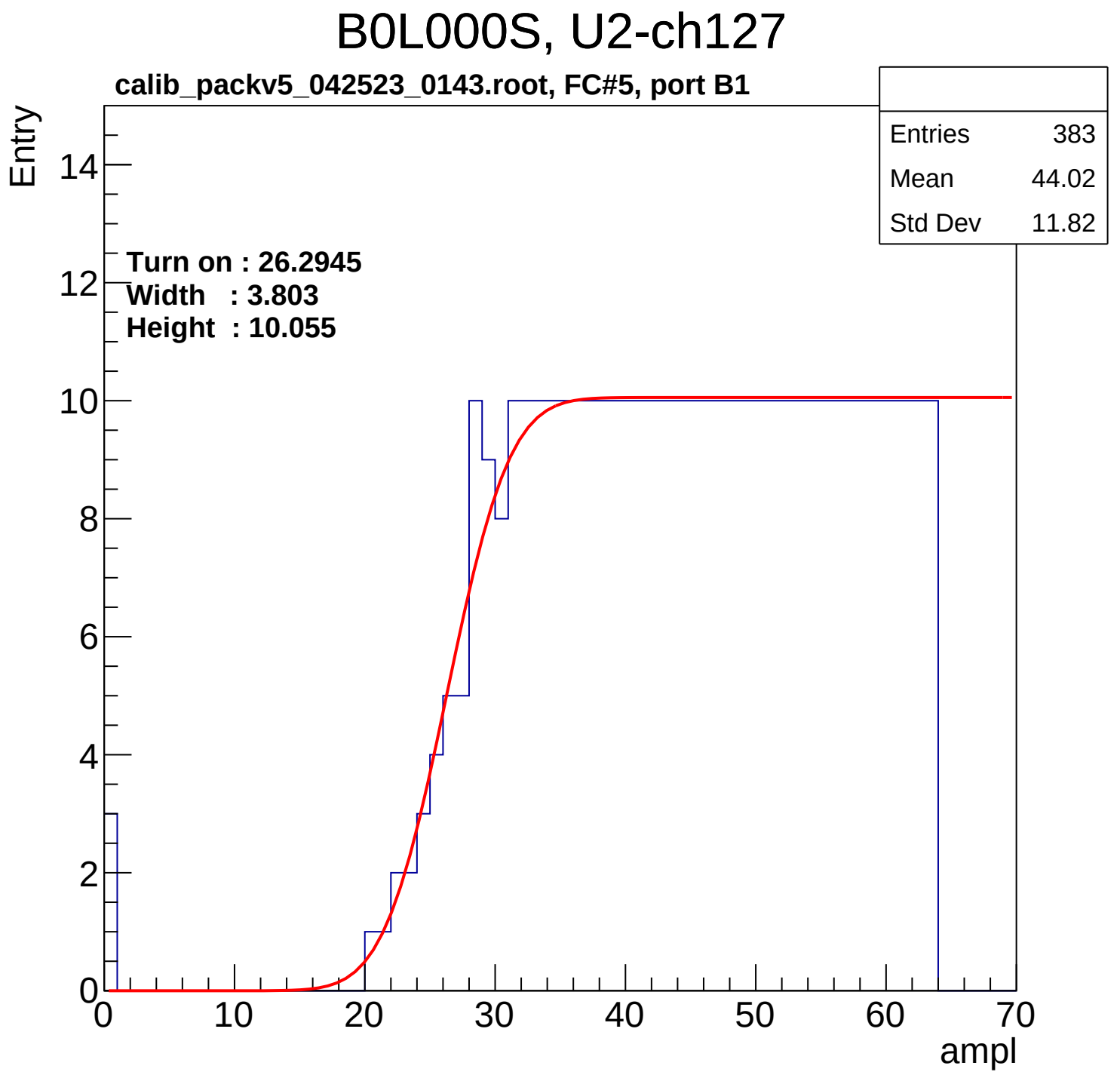
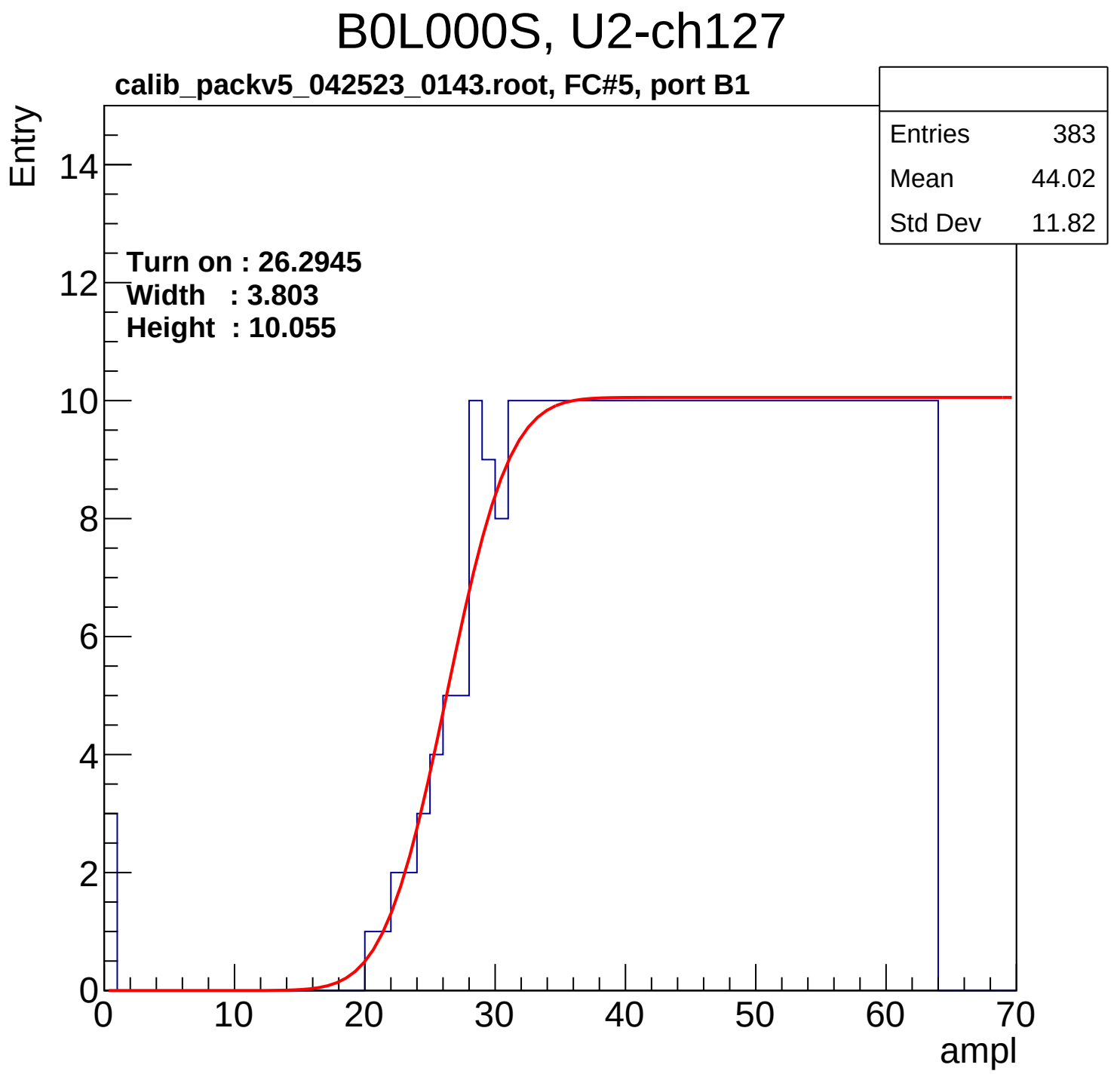

B0L000S, U2-ch127
calib_packv5_042523_0143.root, FC#5, port B1
Entries 383
Mean 44.02
Std Dev 11.82
Turn on : 26.2945
Width : 3.803
Height : 10.055
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L000S, U2-ch127
calib_packv5_042523_0143.root, FC#5, port B1
Entries 383
Mean 44.02
Std Dev 11.82
Turn on : 26.2945
Width : 3.803
Height : 10.055
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70