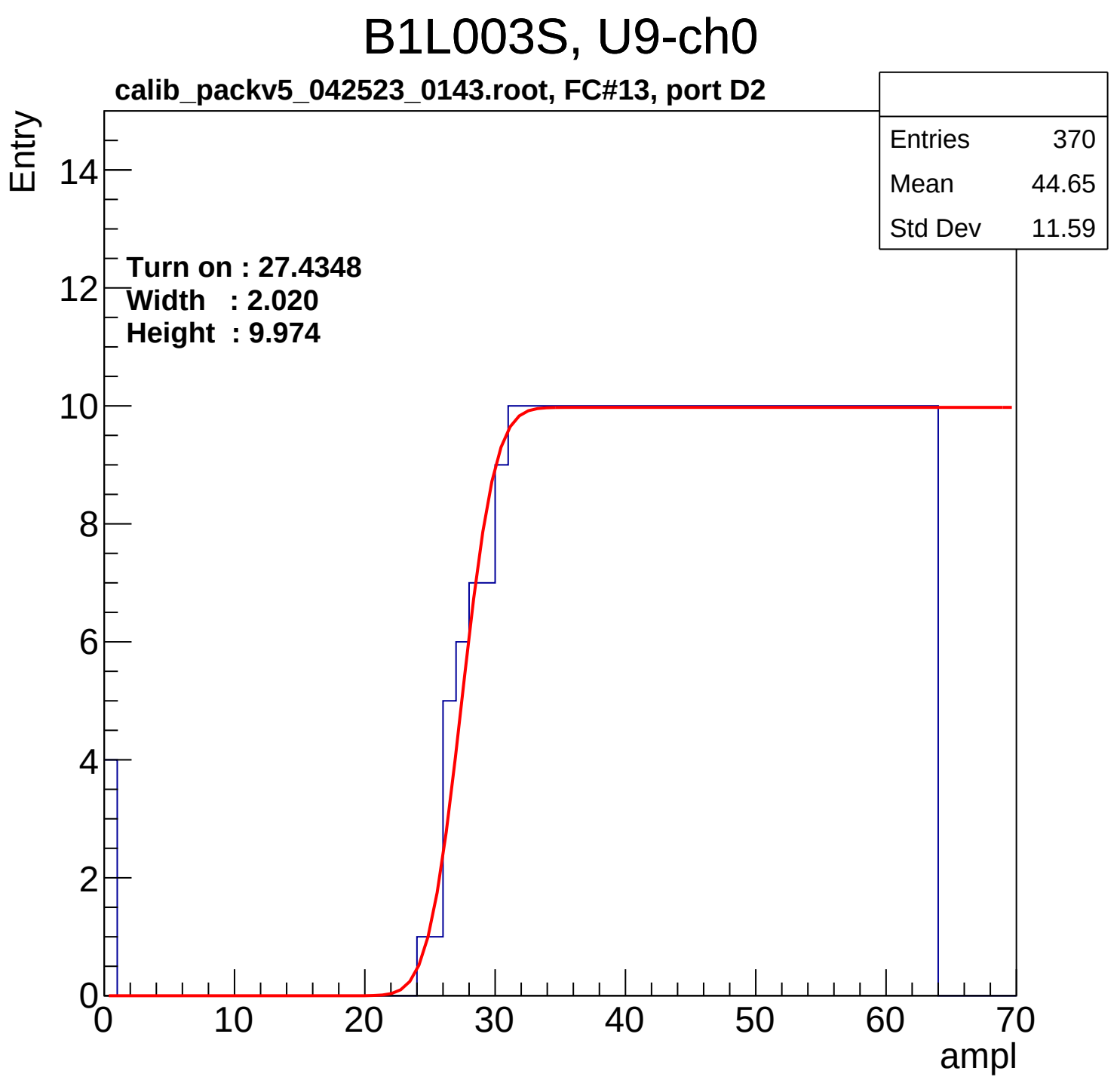
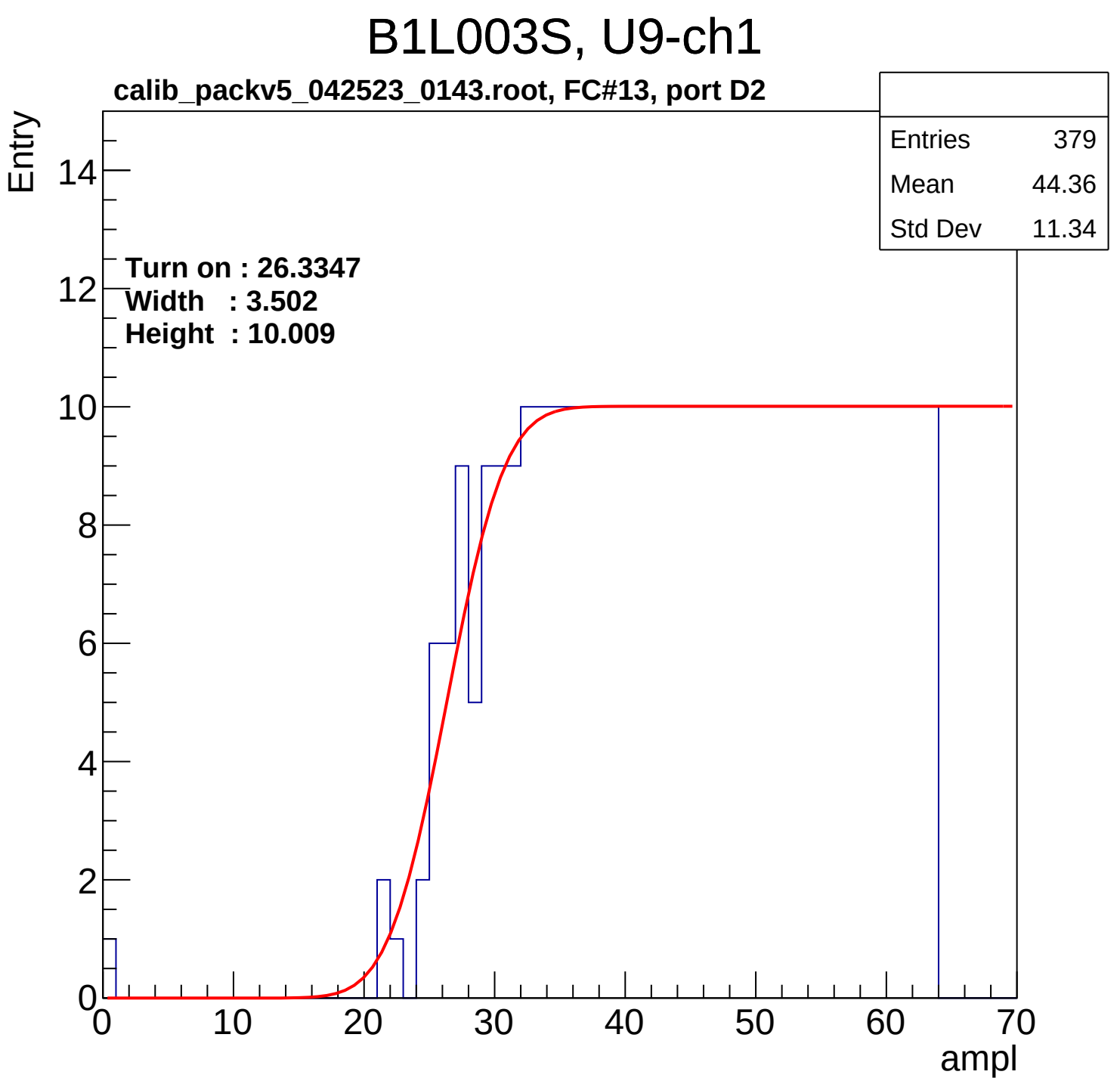
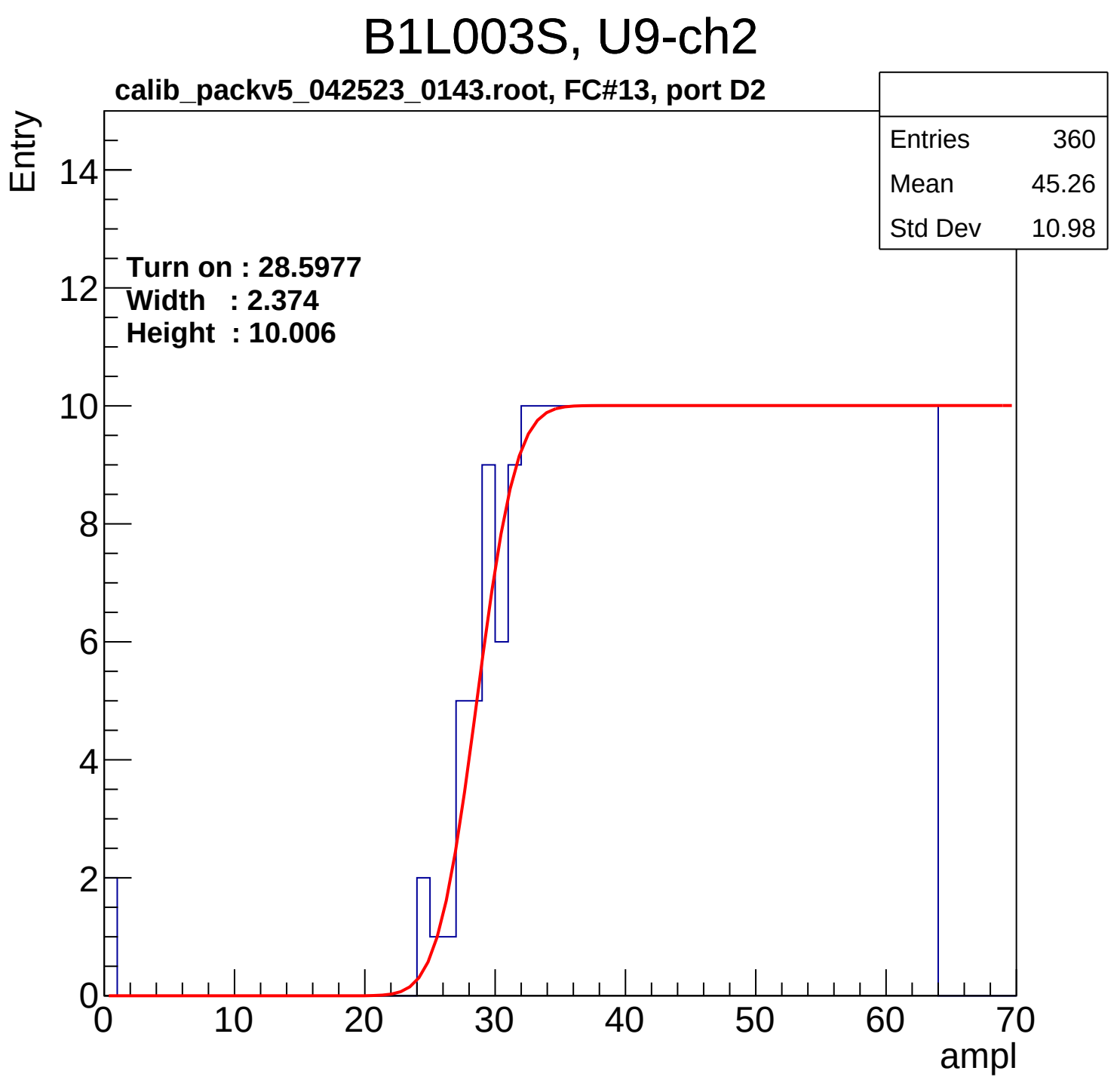
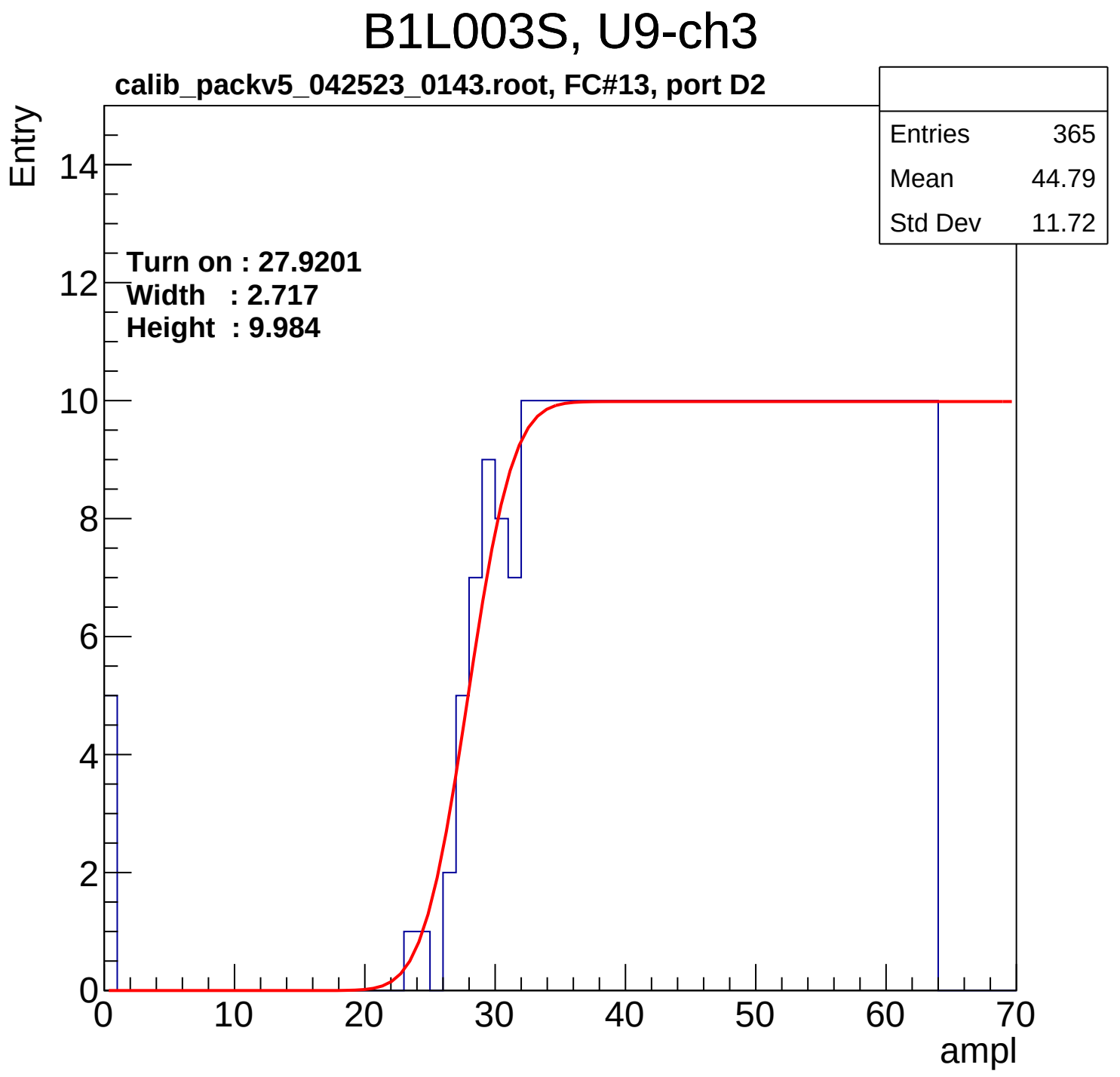
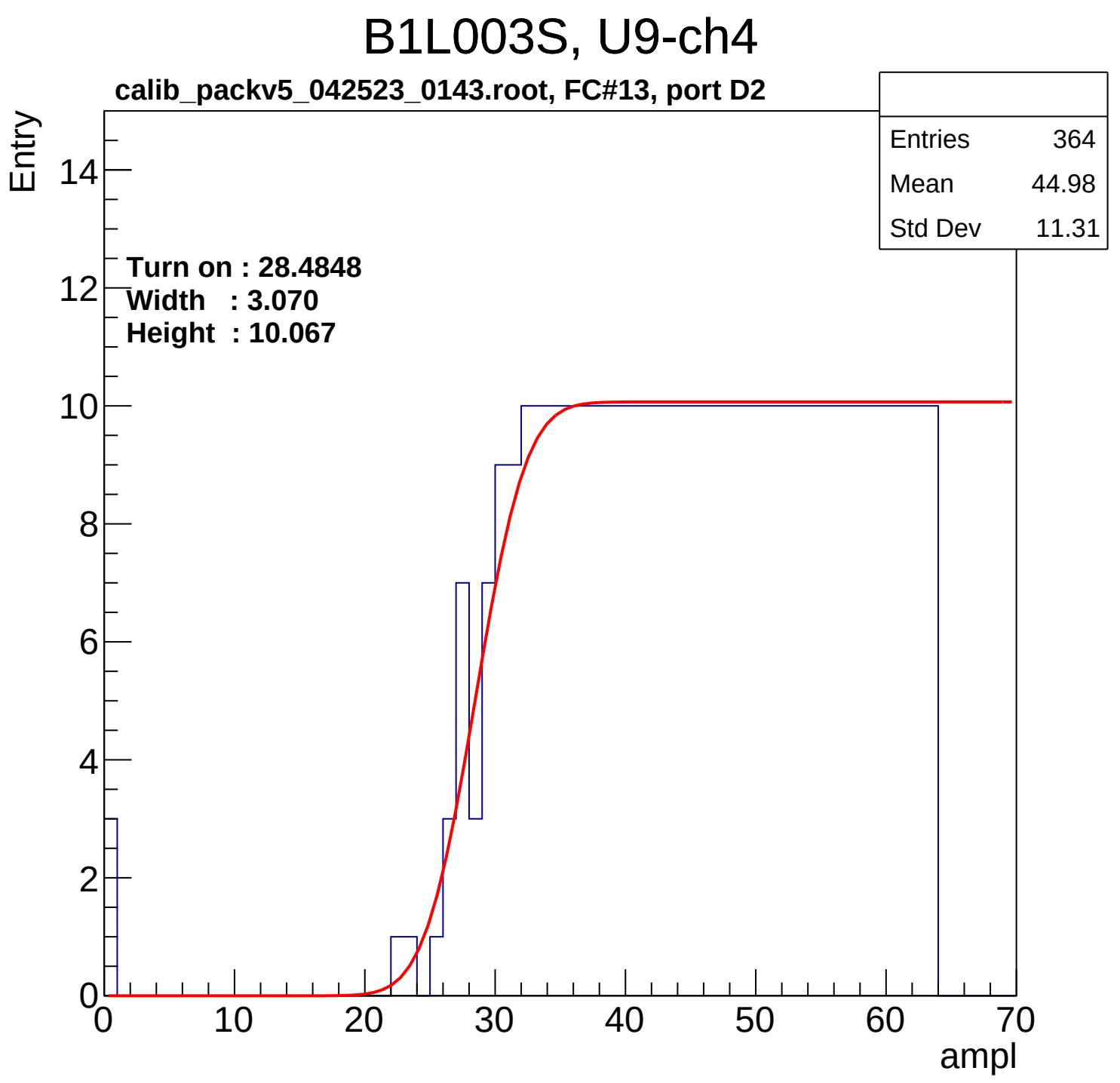
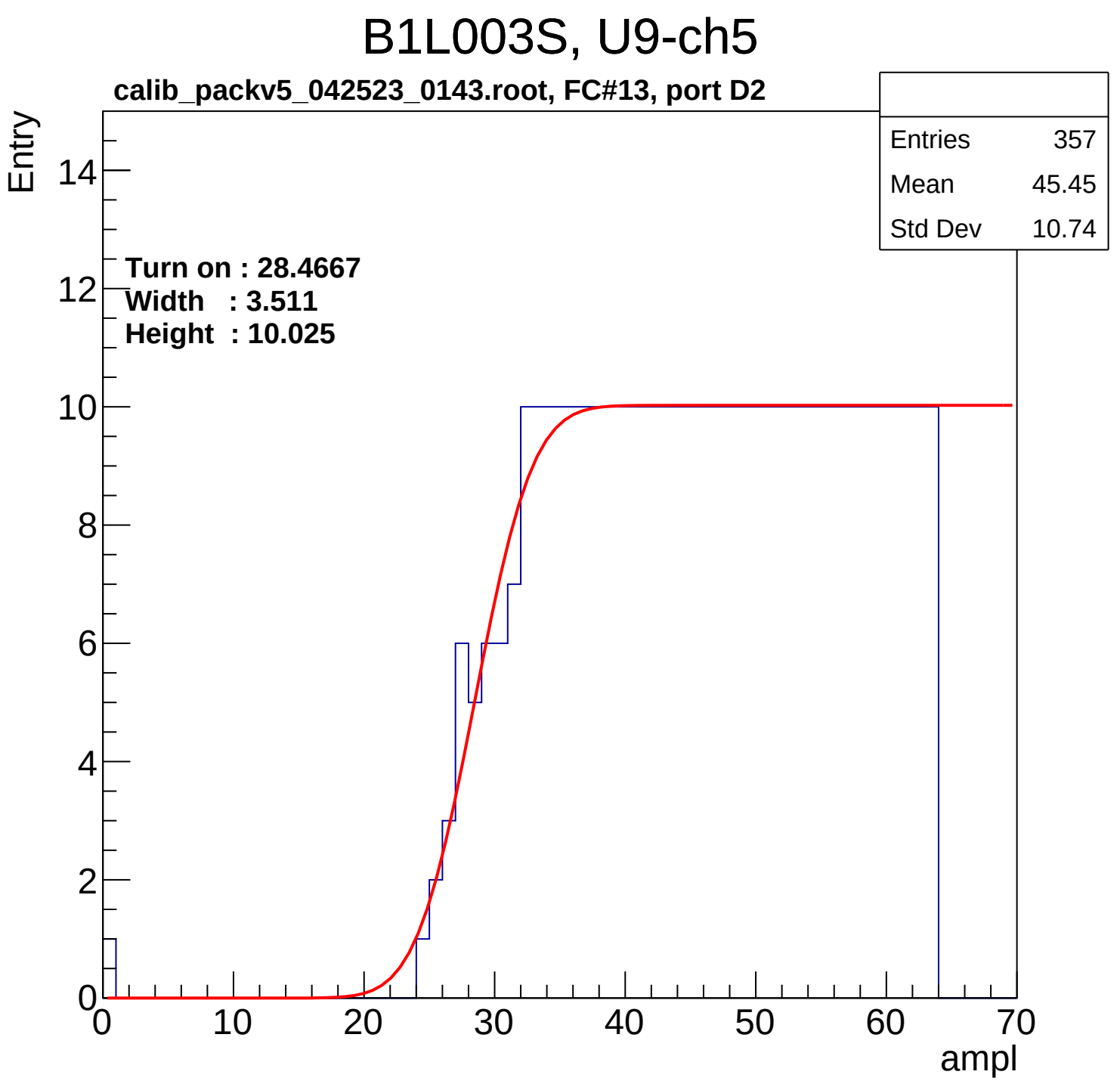

B1L003S, U9-ch0
calib_packv5_042523_0143.root, FC#13, port D2
Entries 370
Mean 44.65
Std Dev 11.59
Turn on : 27.4348
Width : 2.020
Height : 9.974
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

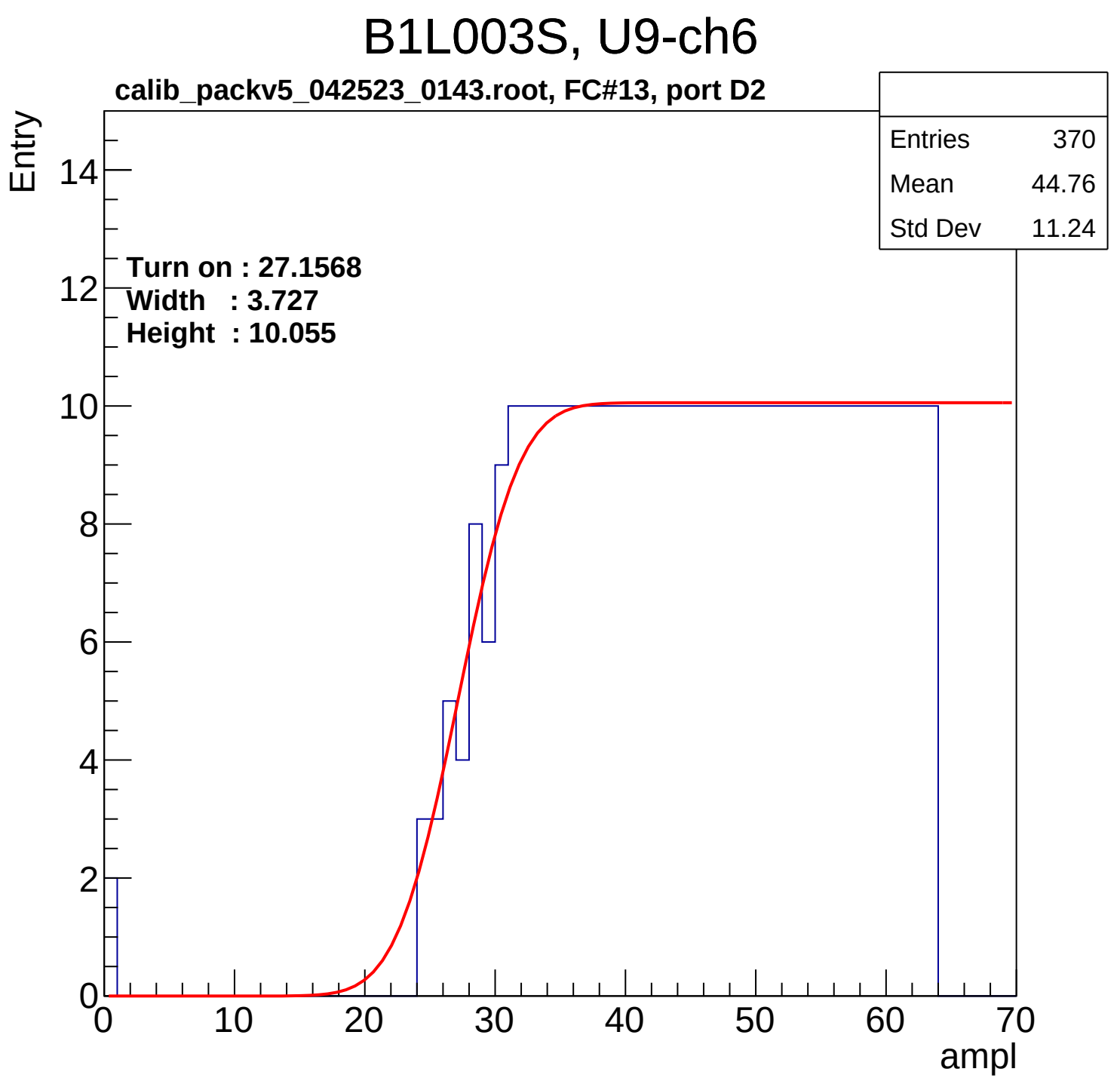

B1L003S, U9-ch1
calib_packv5_042523_0143.root, FC#13, port D2
Entries 379
Mean 44.36
Std Dev 11.34
Turn on : 26.3347
Width : 3.502
Height : 10.009
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

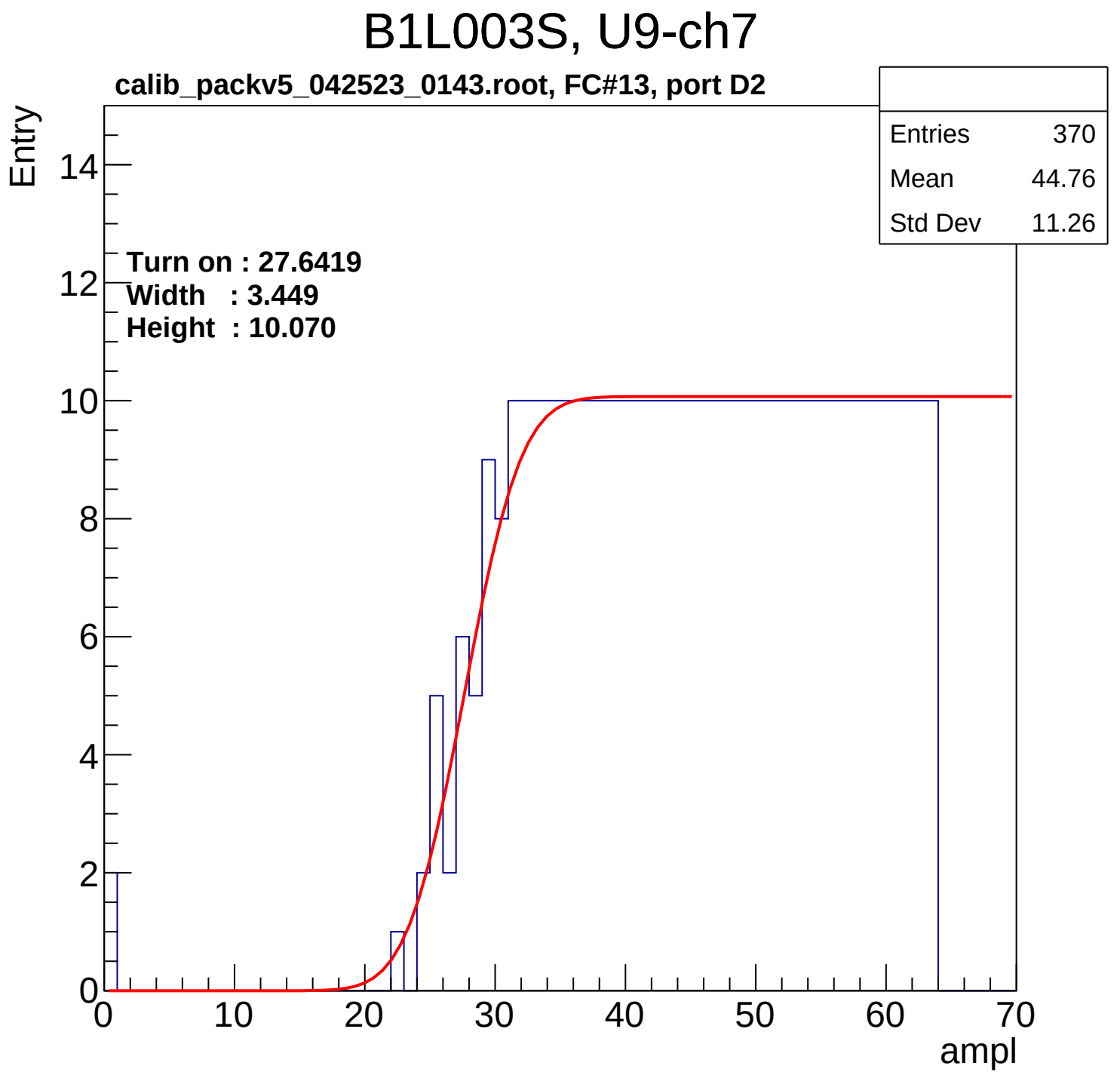

B1L003S, U9-ch2
calib_packv5_042523_0143.root, FC#13, port D2
Entries 360
Mean 45.26
Std Dev 10.98
Turn on : 28.5977
Width : 2.374
Height : 10.006
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

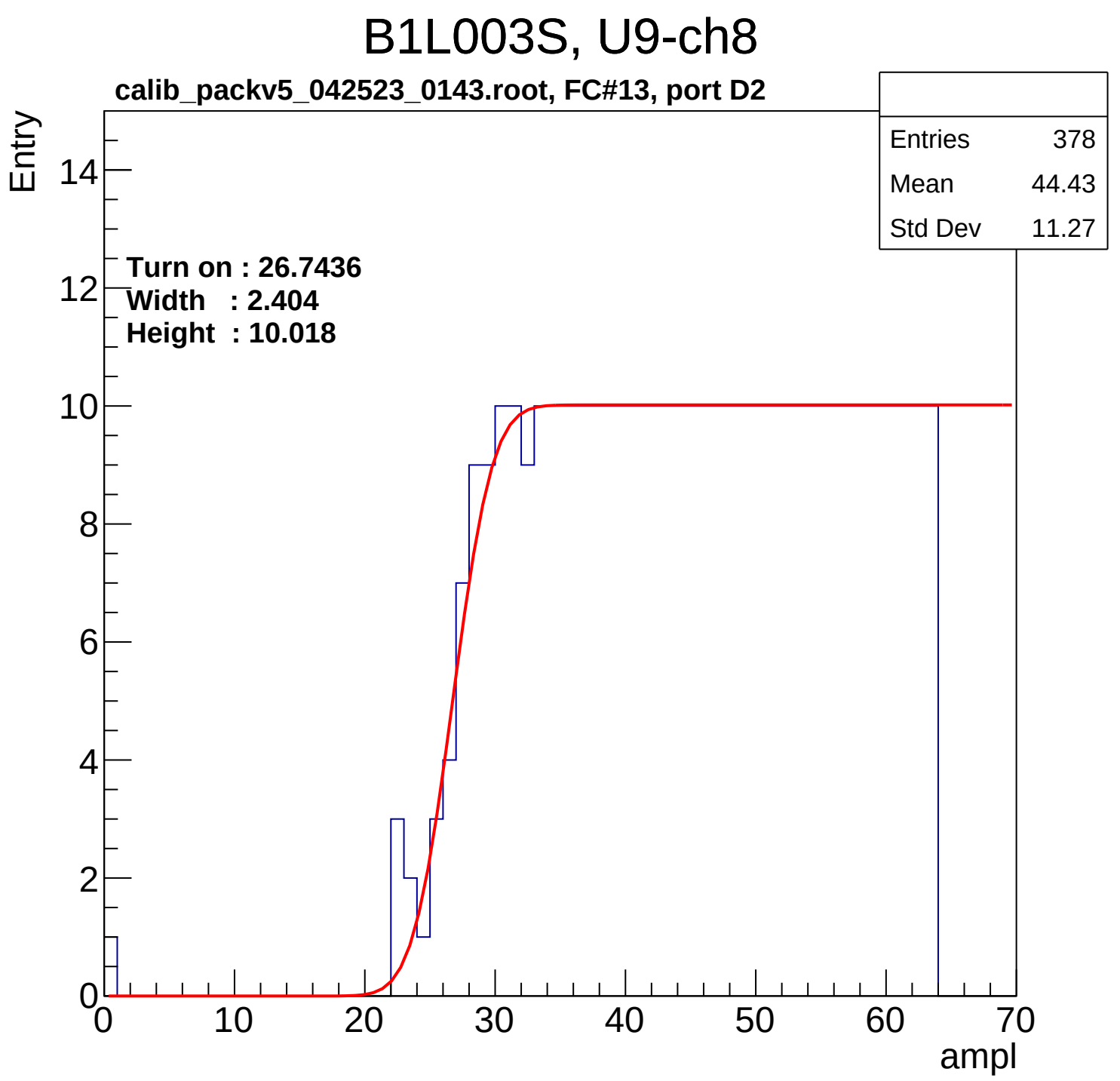

B1L003S, U9-ch3
calib_packv5_042523_0143.root, FC#13, port D2
Entries 365
Mean 44.79
Std Dev 11.72
Turn on : 27.9201
Width : 2.717
Height : 9.984
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

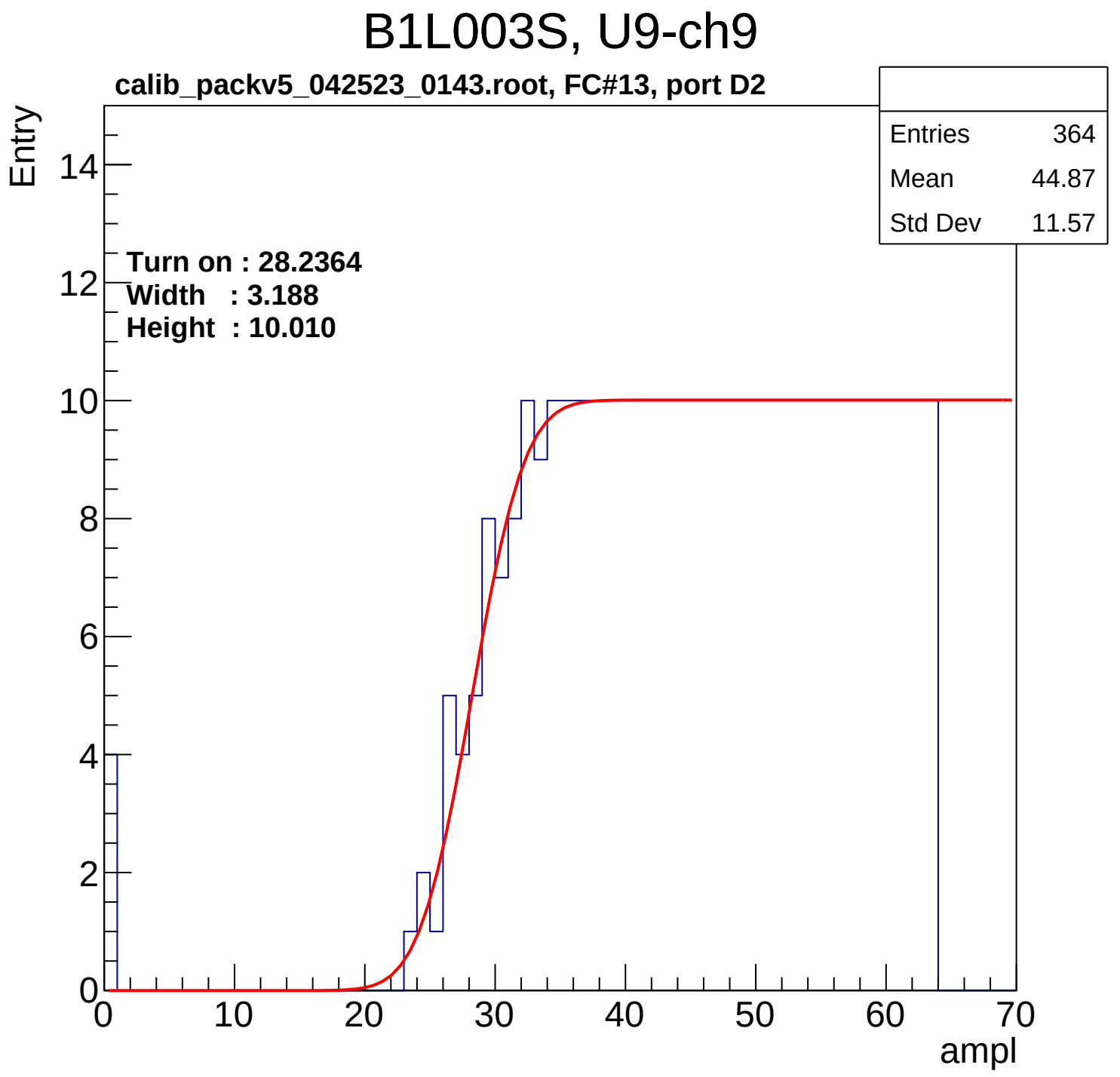

B1L003S, U9-ch4
calib_packv5_042523_0143.root, FC#13, port D2
Entries 364
Mean 44.98
Std Dev 11.31
Turn on : 28.4848
Width : 3.070
Height : 10.067
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

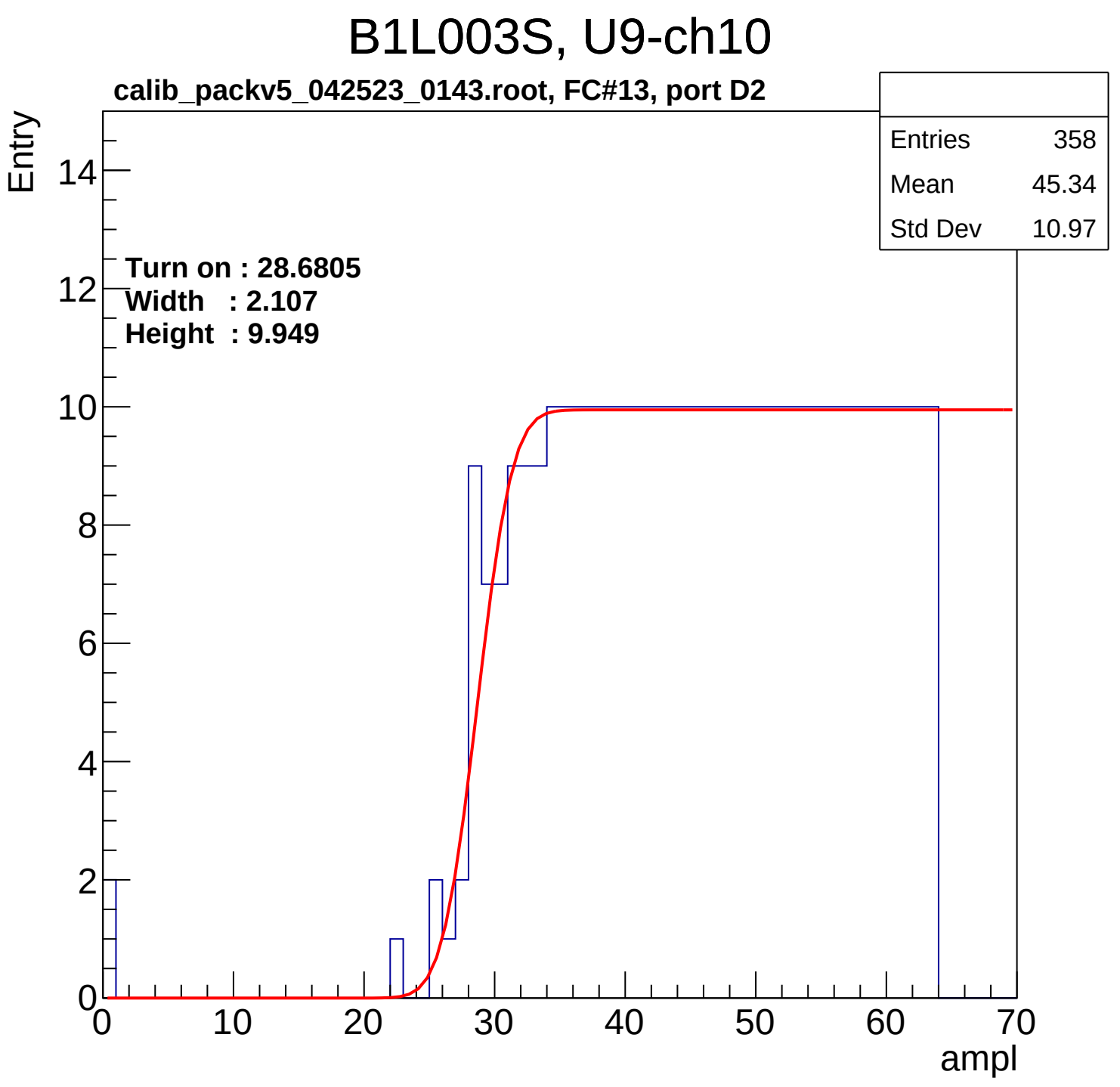

B1L003S, U9-ch5
calib_packv5_042523_0143.root, FC#13, port D2
Entries 357
Mean 45.45
Std Dev 10.74
Turn on : 28.4667
Width : 3.511
Height : 10.025
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

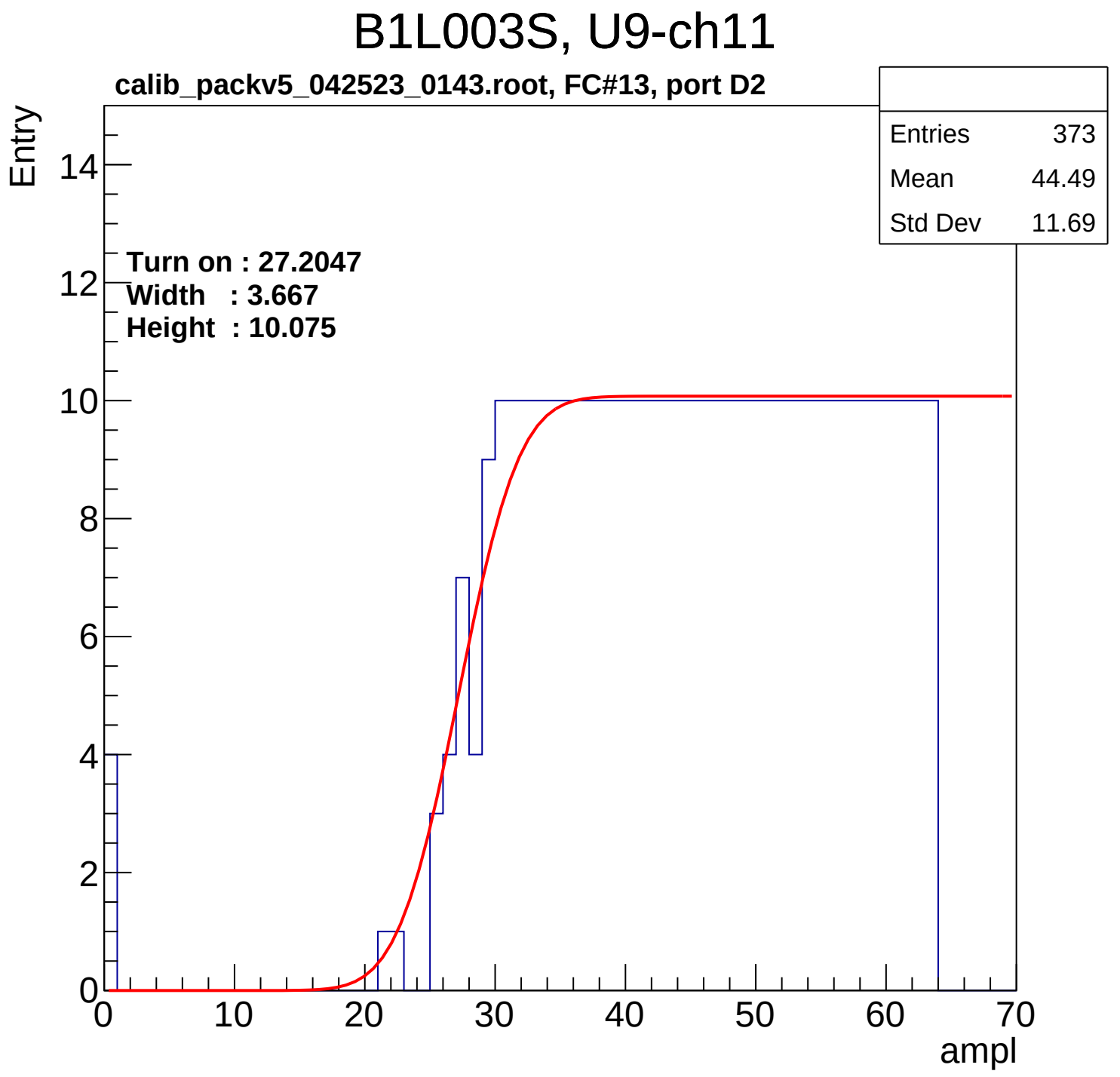

B1L003S, U9-ch6
calib_packv5_042523_0143.root, FC#13, port D2
Entries 370
Mean 44.76
Std Dev 11.24
Turn on : 27.1568
Width : 3.727
Height : 10.055
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

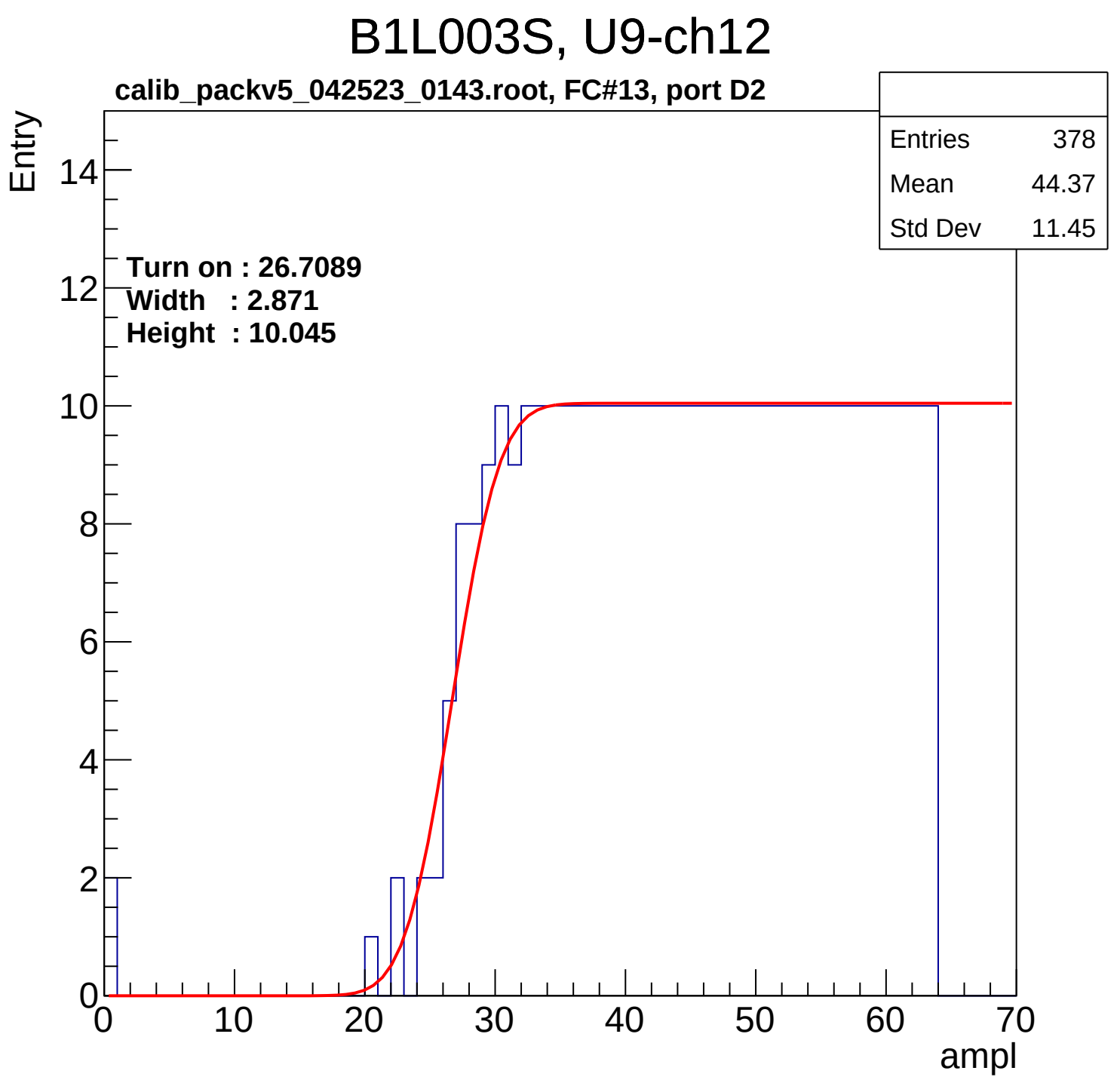

B1L003S, U9-ch7
calib_packv5_042523_0143.root, FC#13, port D2
Entries 370
Mean 44.76
Std Dev 11.26
Turn on : 27.6419
Width : 3.449
Height : 10.070
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

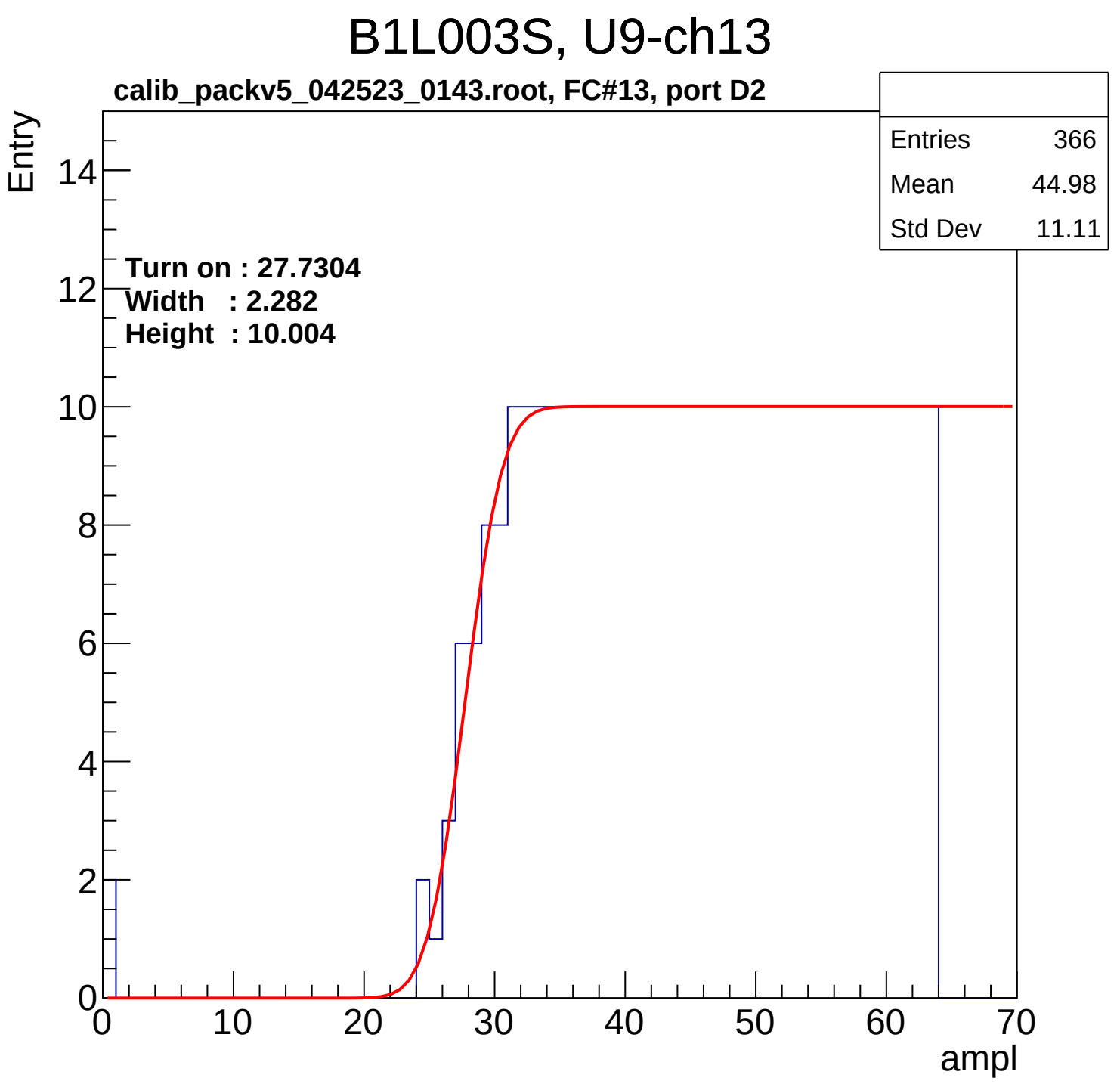

B1L003S, U9-ch8
calib_packv5_042523_0143.root, FC#13, port D2
Entries 378
Mean 44.43
Std Dev 11.27
Turn on : 26.7436
Width : 2.404
Height : 10.018
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

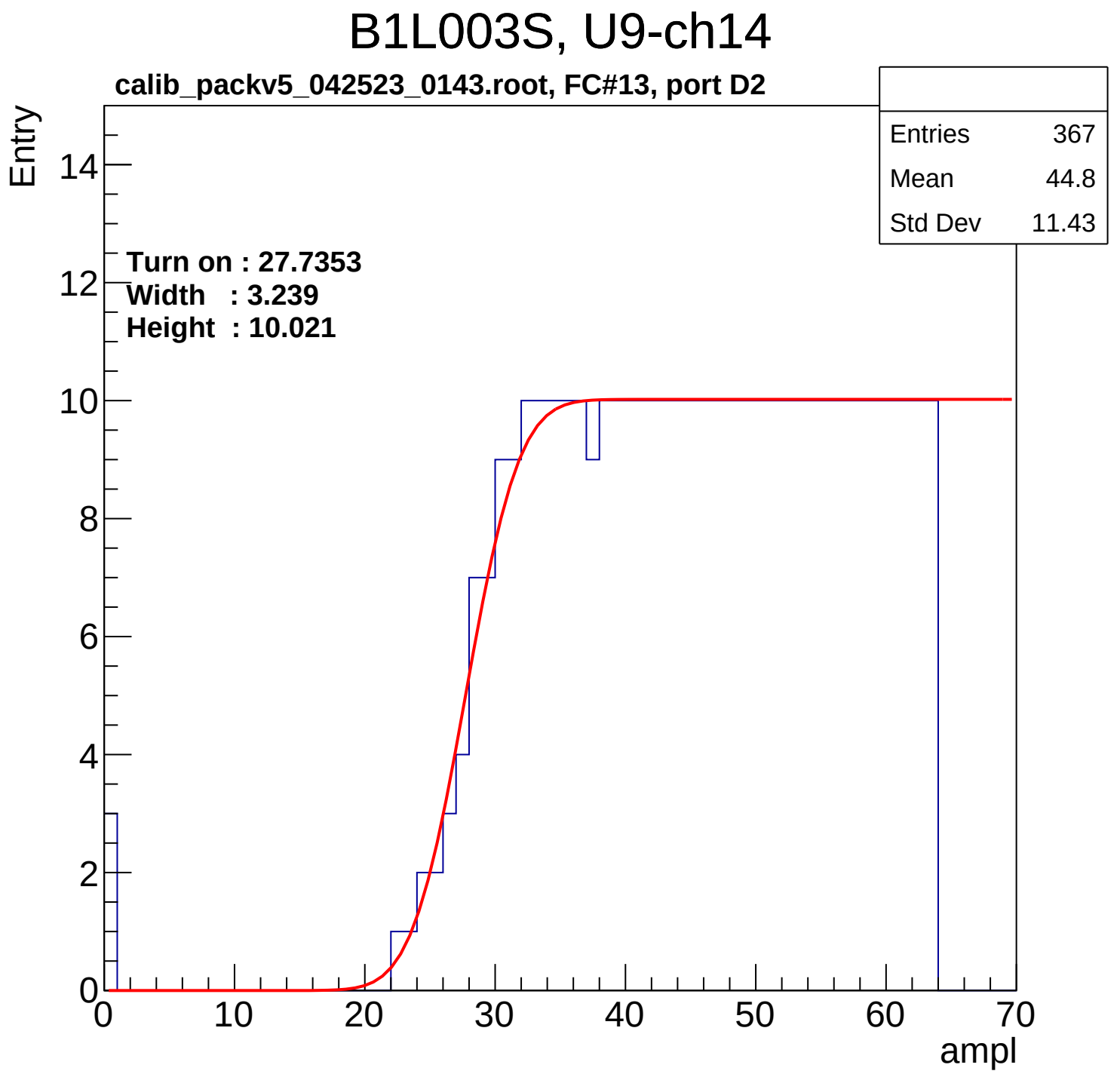

B1L003S, U9-ch9
calib_packv5_042523_0143.root, FC#13, port D2
Entries 364
Mean 44.87
Std Dev 11.57
Turn on : 28.2364
Width : 3.188
Height : 10.010
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

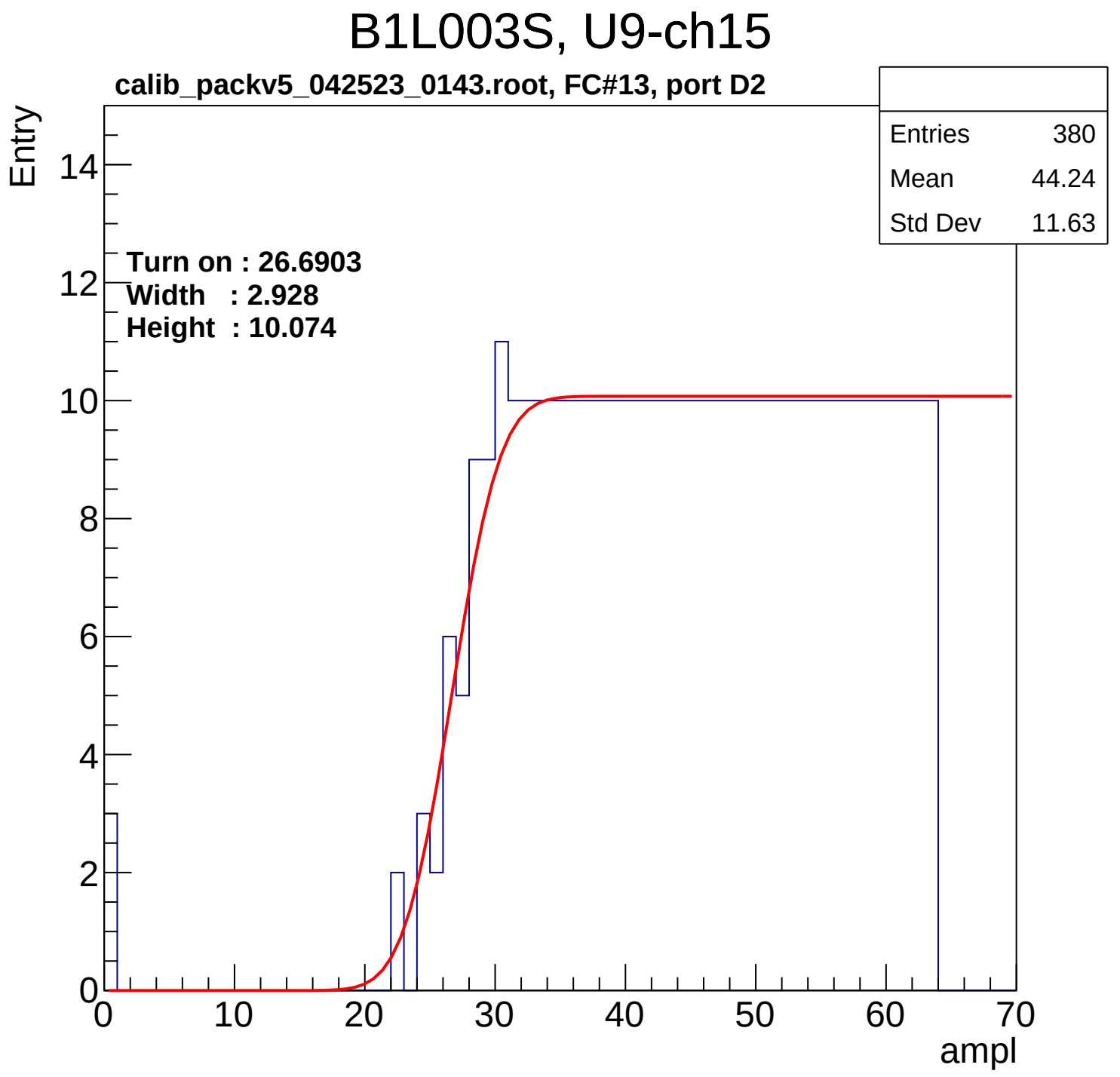

B1L003S, U9-ch10
calib_packv5_042523_0143.root, FC#13, port D2
Entries 358
Mean 45.34
Std Dev 10.97
Turn on : 28.6805
Width : 2.107
Height : 9.949
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

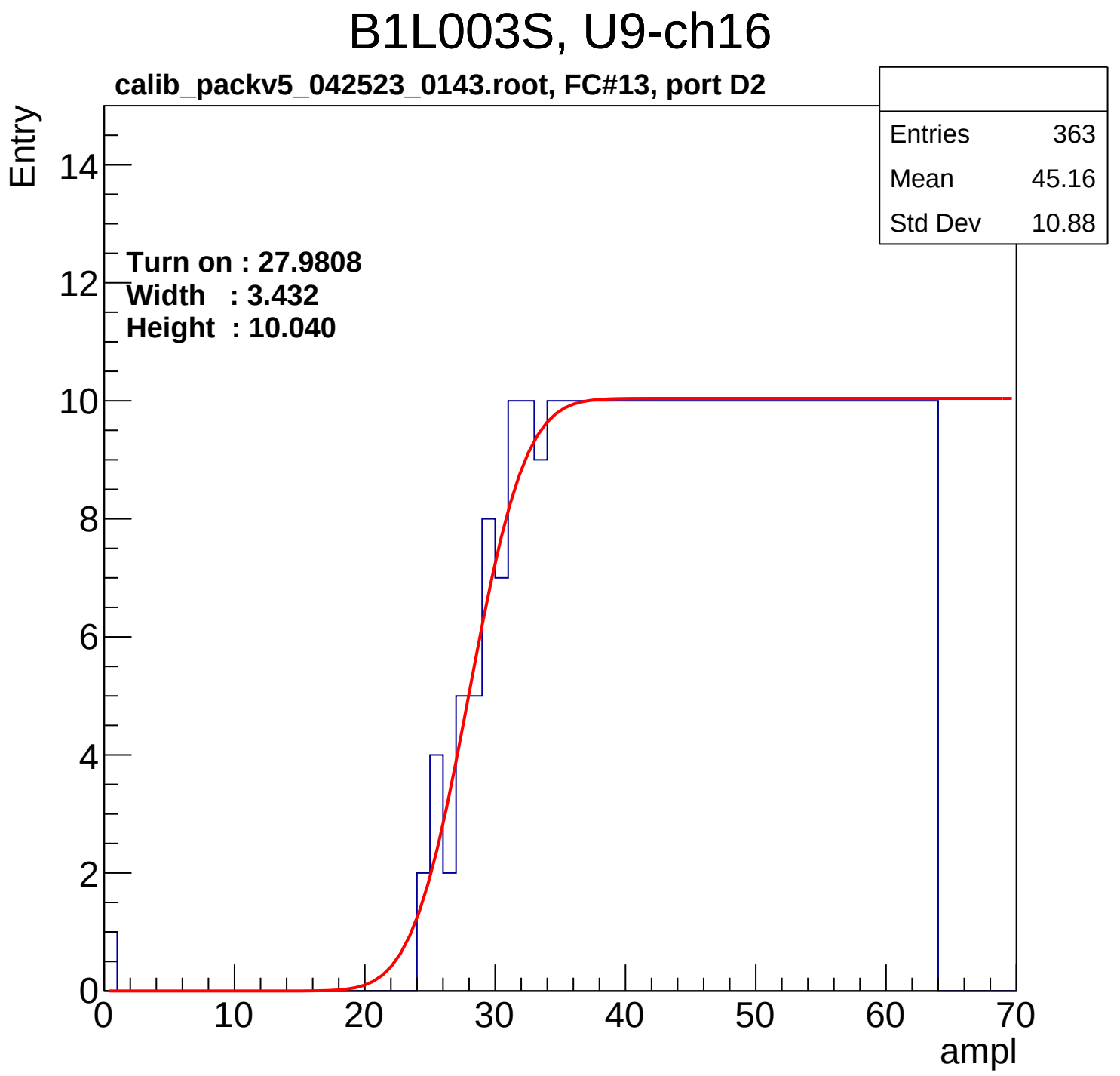

B1L003S, U9-ch11
calib_packv5_042523_0143.root, FC#13, port D2
Entries 373
Mean 44.49
Std Dev 11.69
Turn on : 27.2047
Width : 3.667
Height : 10.075
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

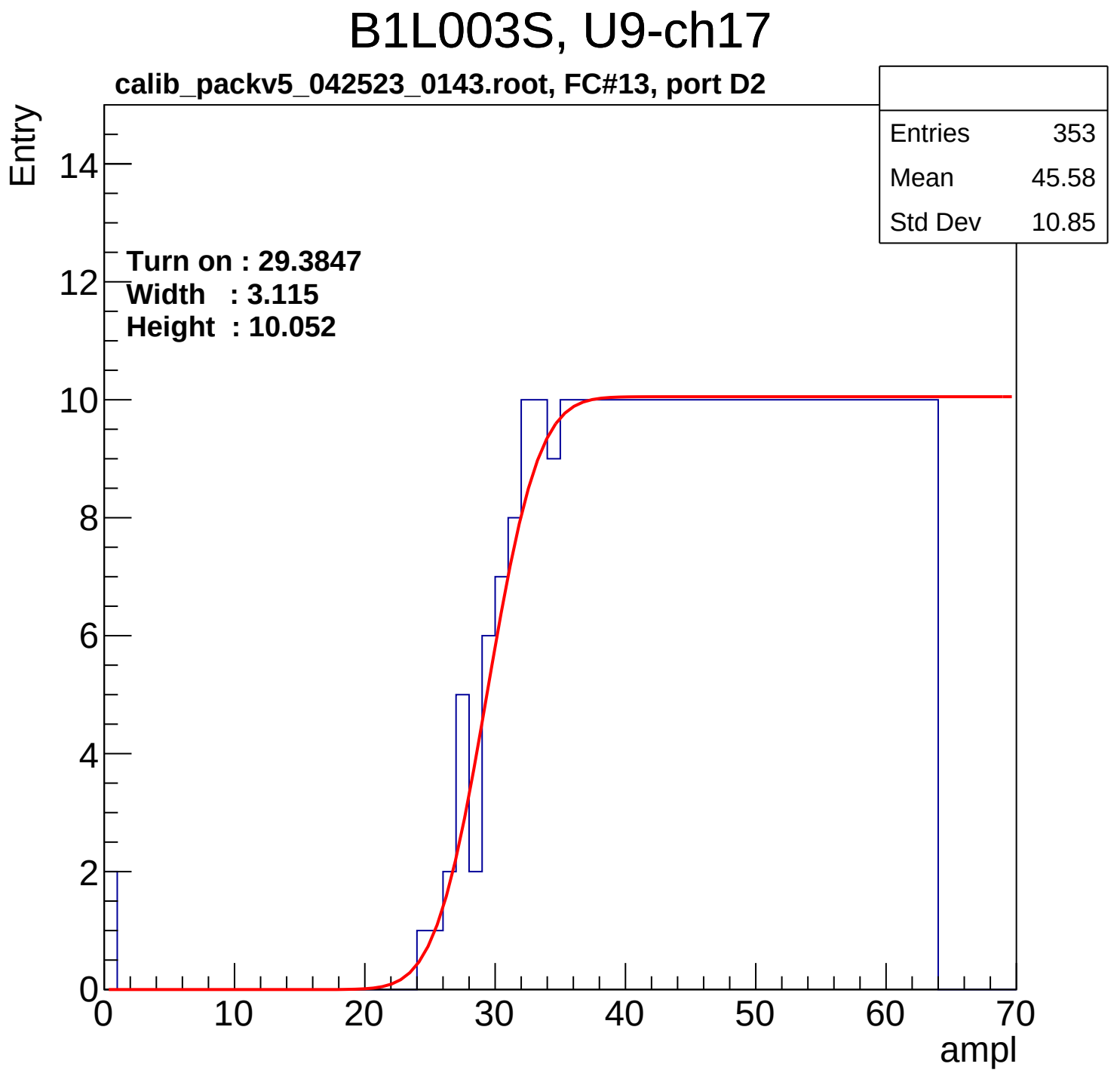

B1L003S, U9-ch12
calib_packv5_042523_0143.root, FC#13, port D2
Entries 378
Mean 44.37
Std Dev 11.45
Turn on : 26.7089
Width : 2.871
Height : 10.045
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

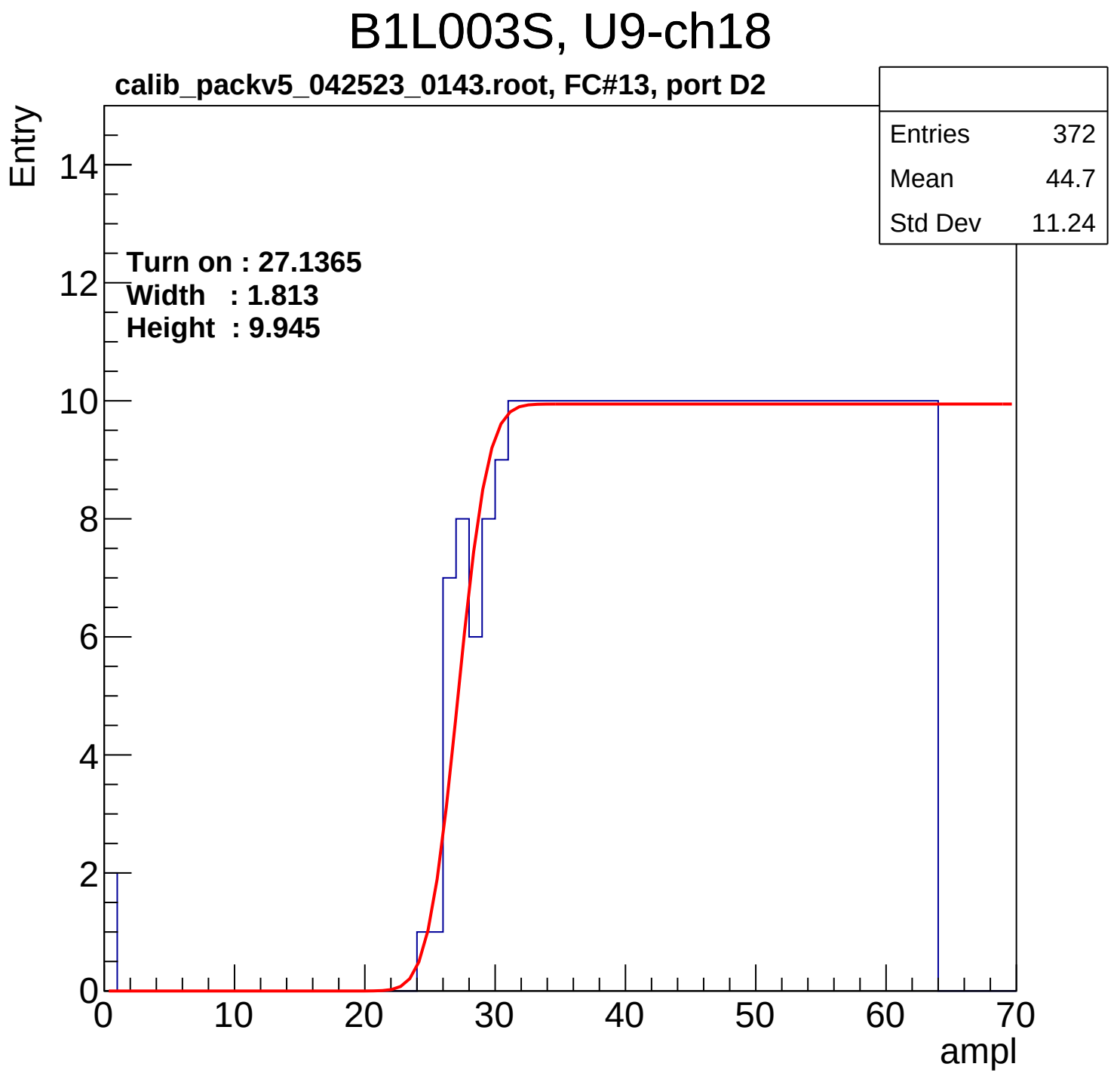

B1L003S, U9-ch13
calib_packv5_042523_0143.root, FC#13, port D2
Entries 366
Mean 44.98
Std Dev 11.11
Turn on : 27.7304
Width : 2.282
Height : 10.004
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

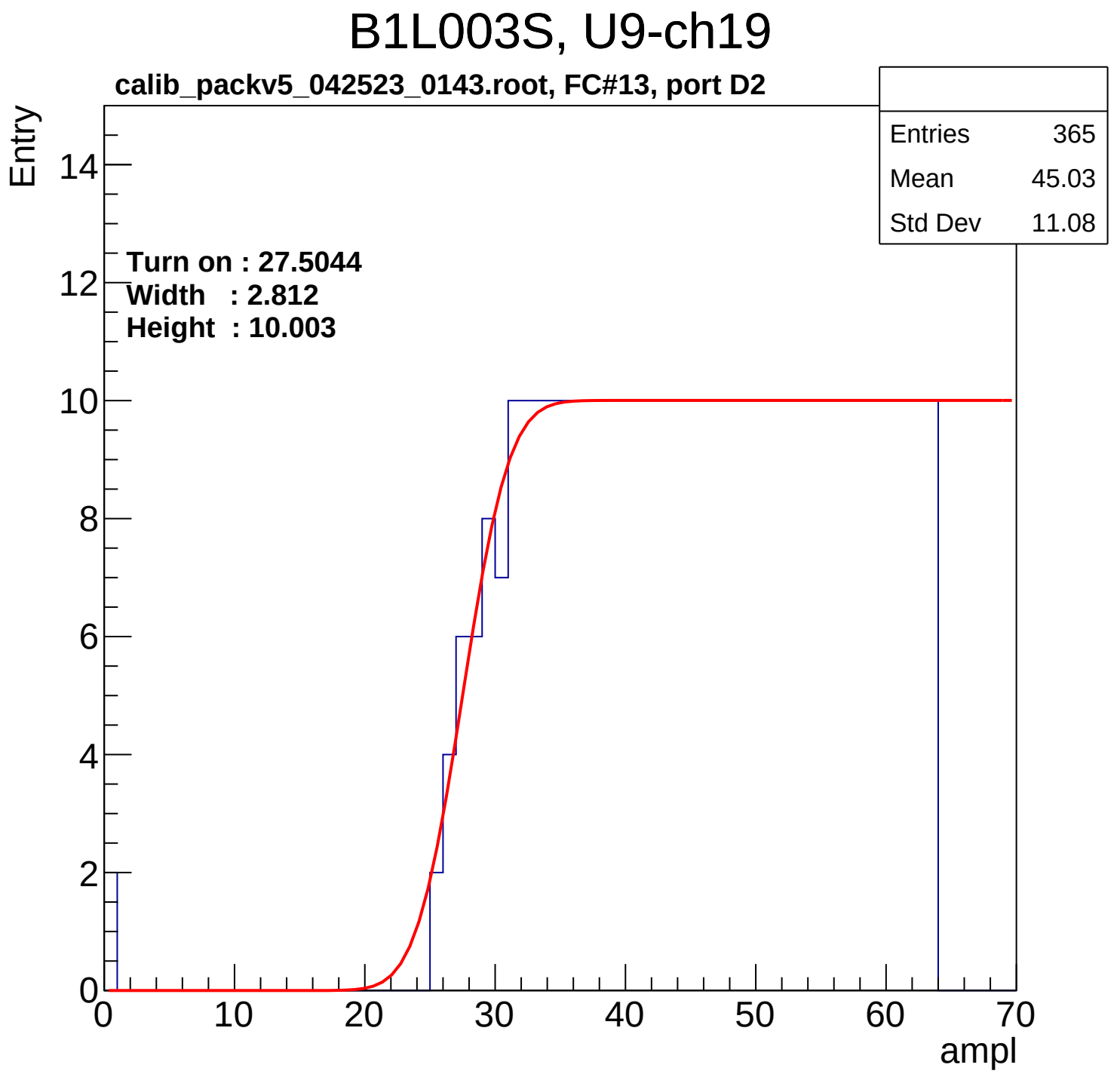

B1L003S, U9-ch14
calib_packv5_042523_0143.root, FC#13, port D2
Entries 367
Mean 44.8
Std Dev 11.43
Turn on : 27.7353
Width : 3.239
Height : 10.021
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

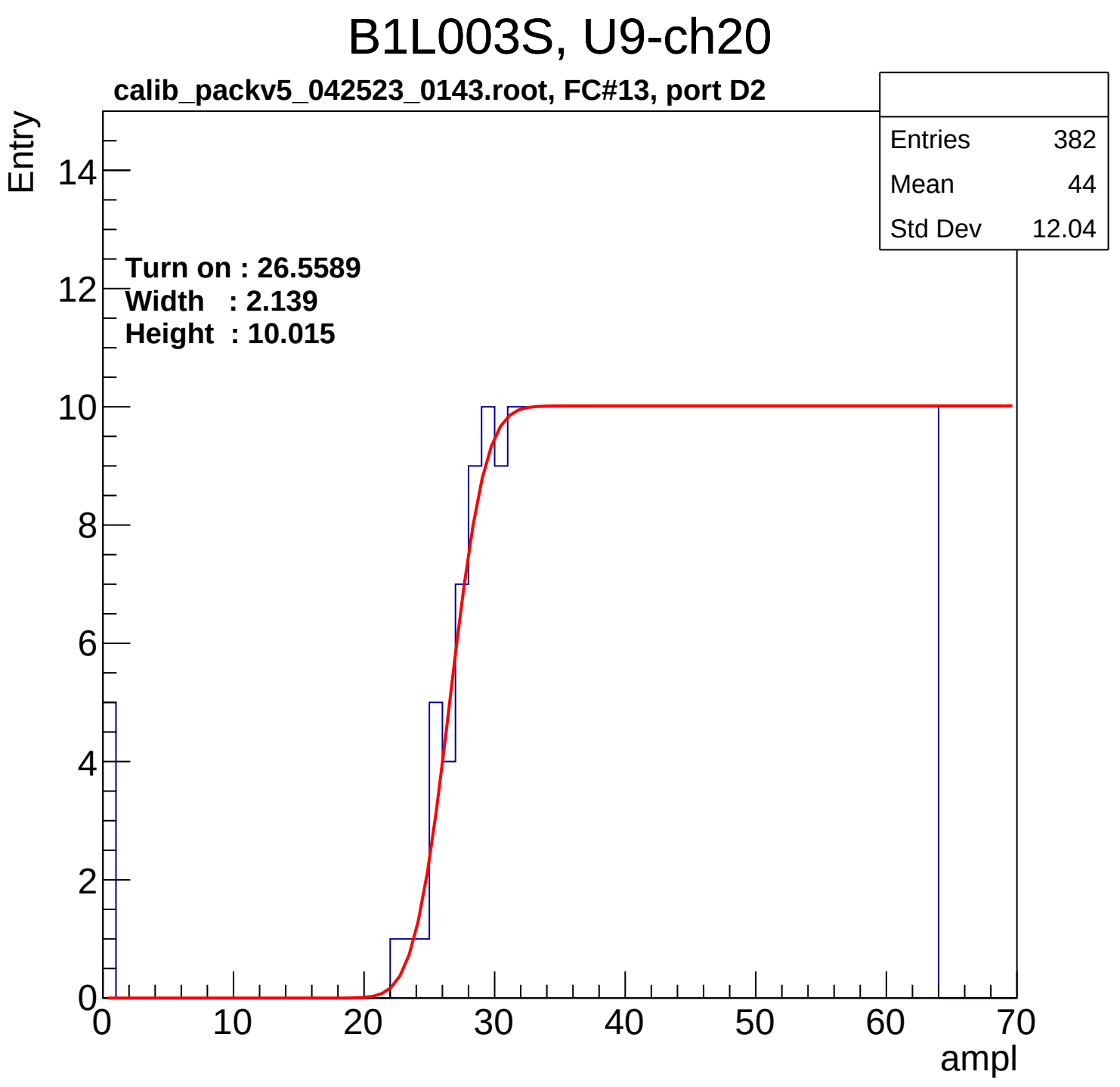

B1L003S, U9-ch15
calib_packv5_042523_0143.root, FC#13, port D2
Entries 380
Mean 44.24
Std Dev 11.63
Turn on : 26.6903
Width : 2.928
Height : 10.074
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

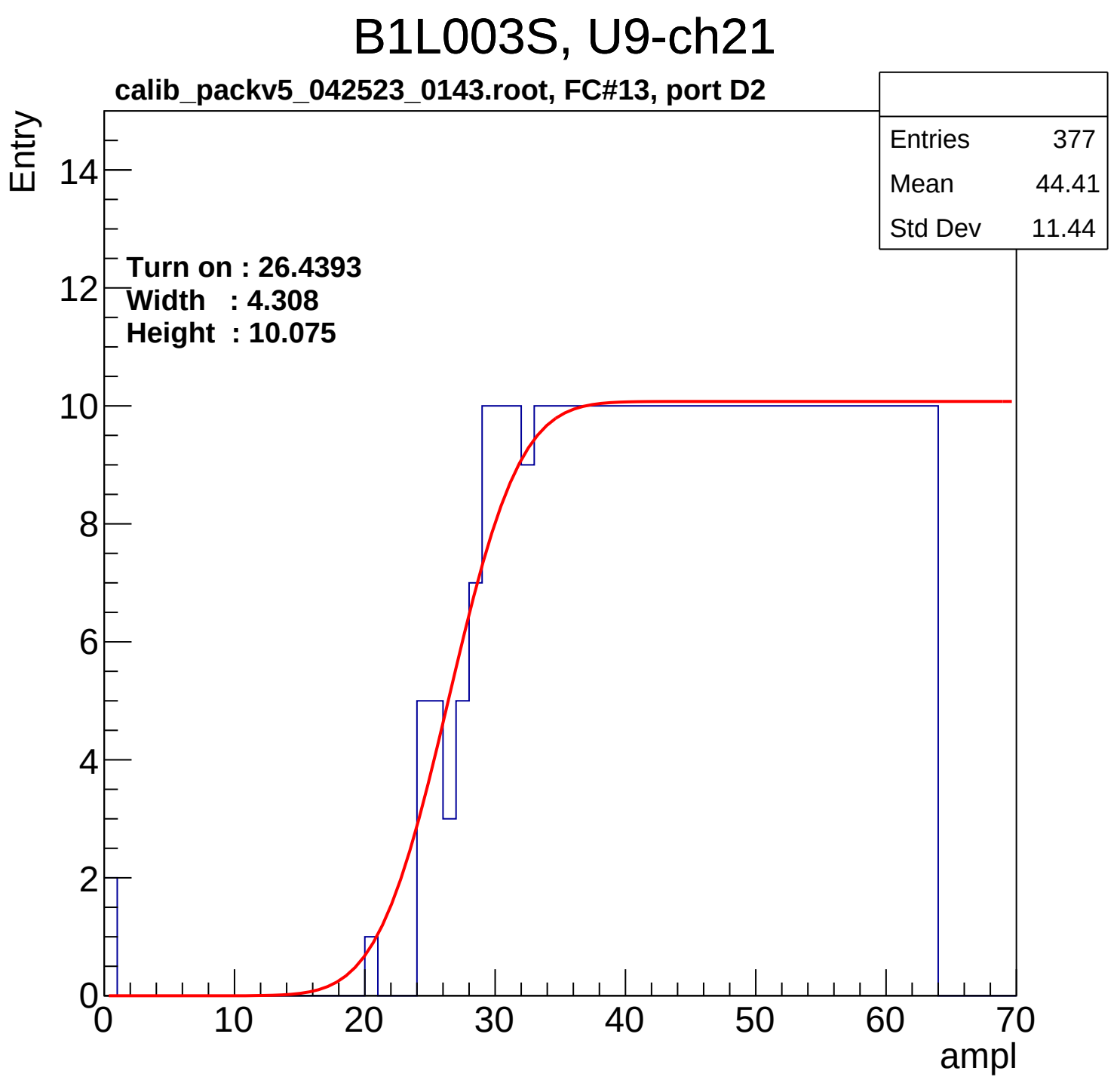

B1L003S, U9-ch16
calib_packv5_042523_0143.root, FC#13, port D2
Entries 363
Mean 45.16
Std Dev 10.88
Turn on : 27.9808
Width : 3.432
Height : 10.040
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

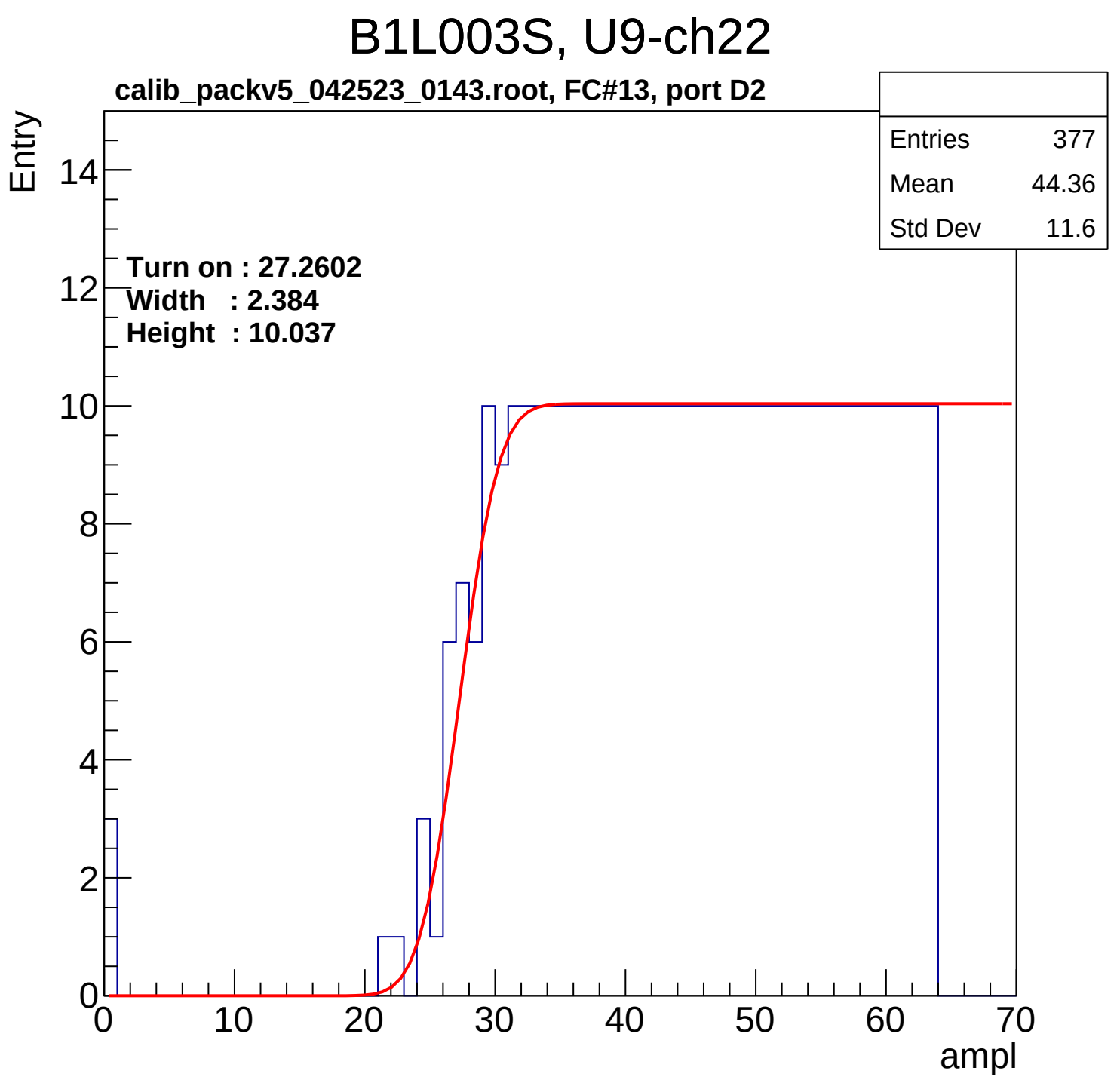

B1L003S, U9-ch17
calib_packv5_042523_0143.root, FC#13, port D2
Entries 353
Mean 45.58
Std Dev 10.85
Turn on : 29.3847
Width : 3.115
Height : 10.052
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

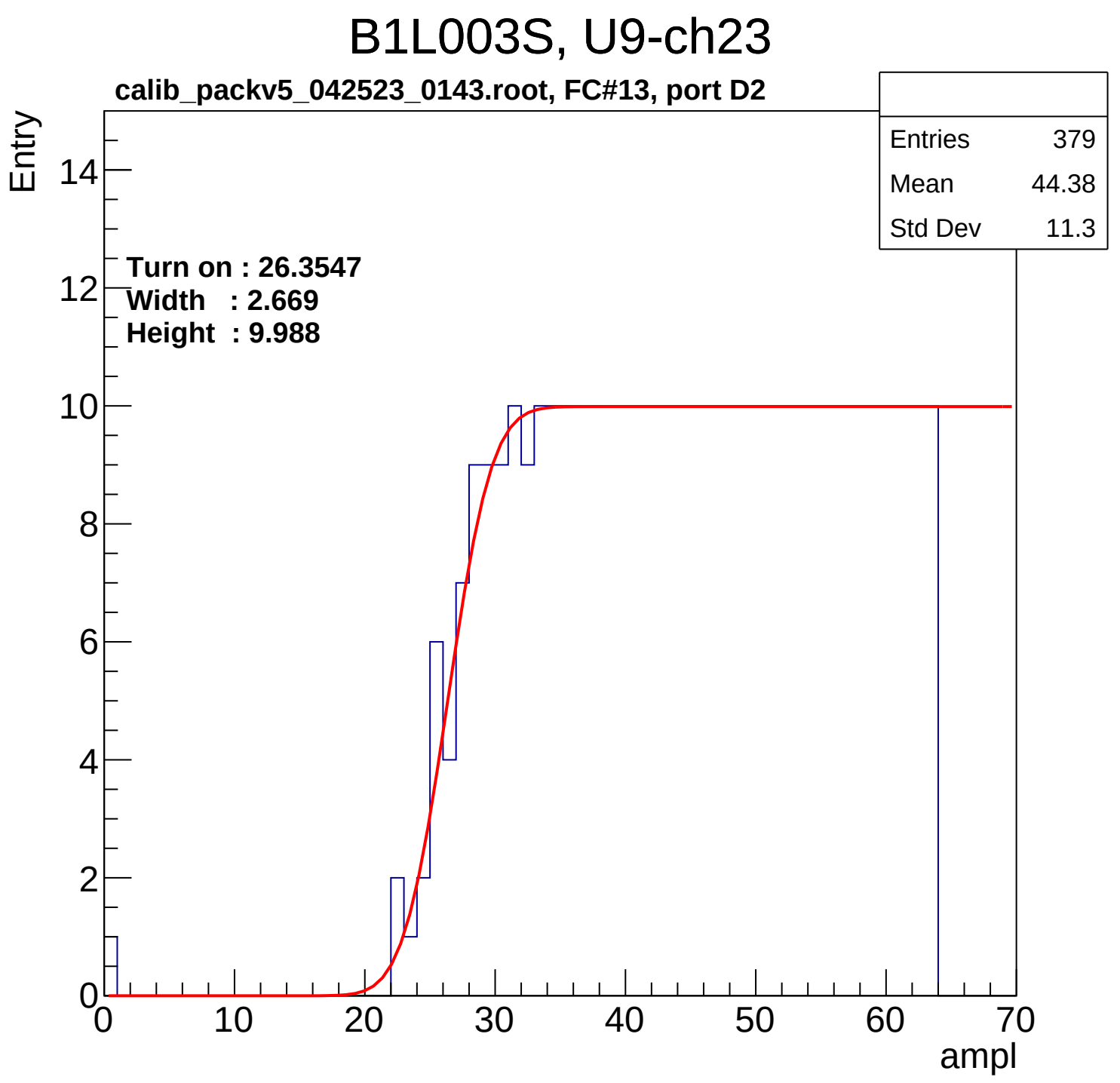

B1L003S, U9-ch18
calib_packv5_042523_0143.root, FC#13, port D2
Entries 372
Mean 44.7
Std Dev 11.24
Turn on : 27.1365
Width : 1.813
Height : 9.945
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

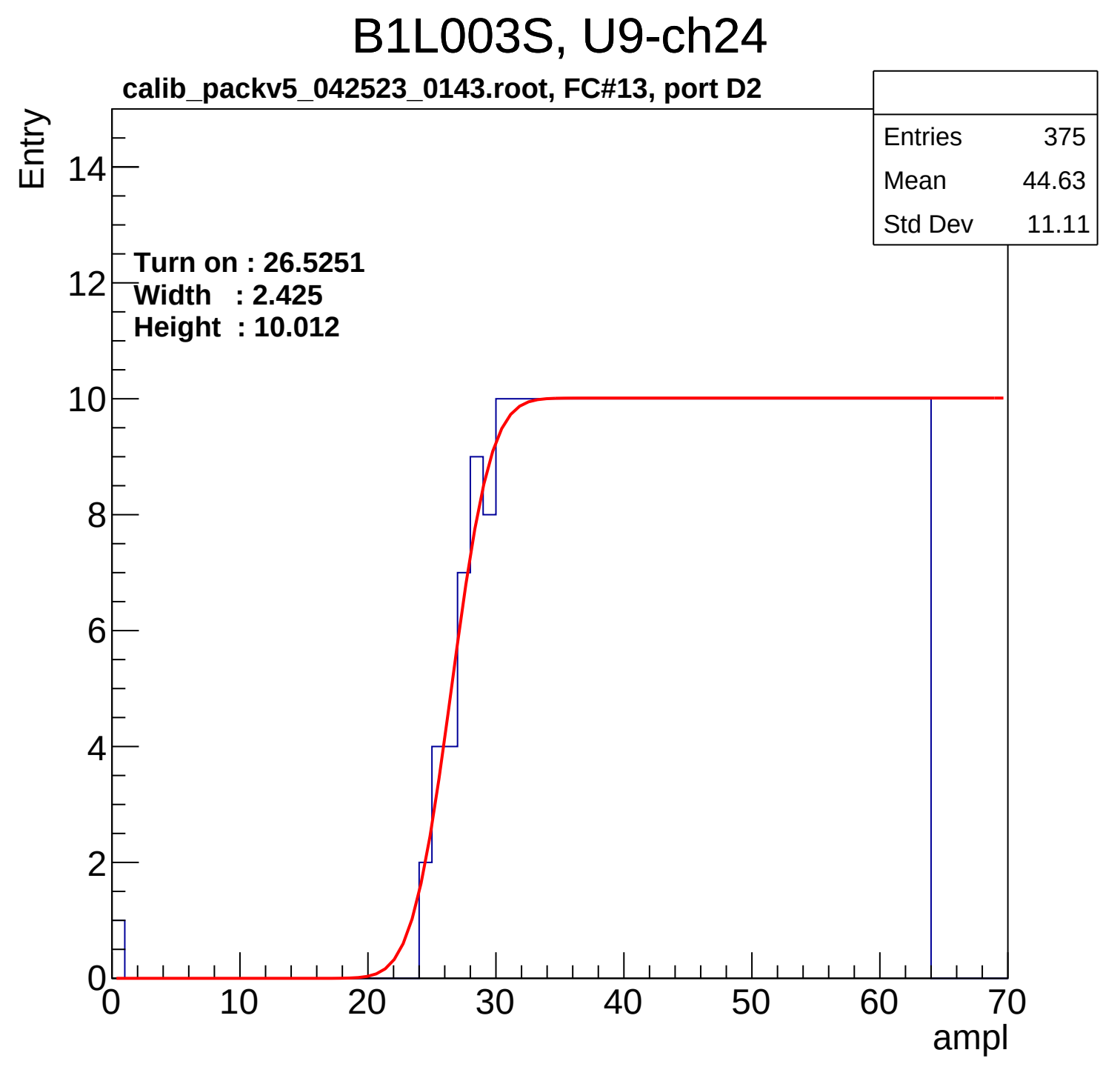

B1L003S, U9-ch19
calib_packv5_042523_0143.root, FC#13, port D2
Entries 365
Mean 45.03
Std Dev 11.08
Turn on : 27.5044
Width : 2.812
Height : 10.003
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

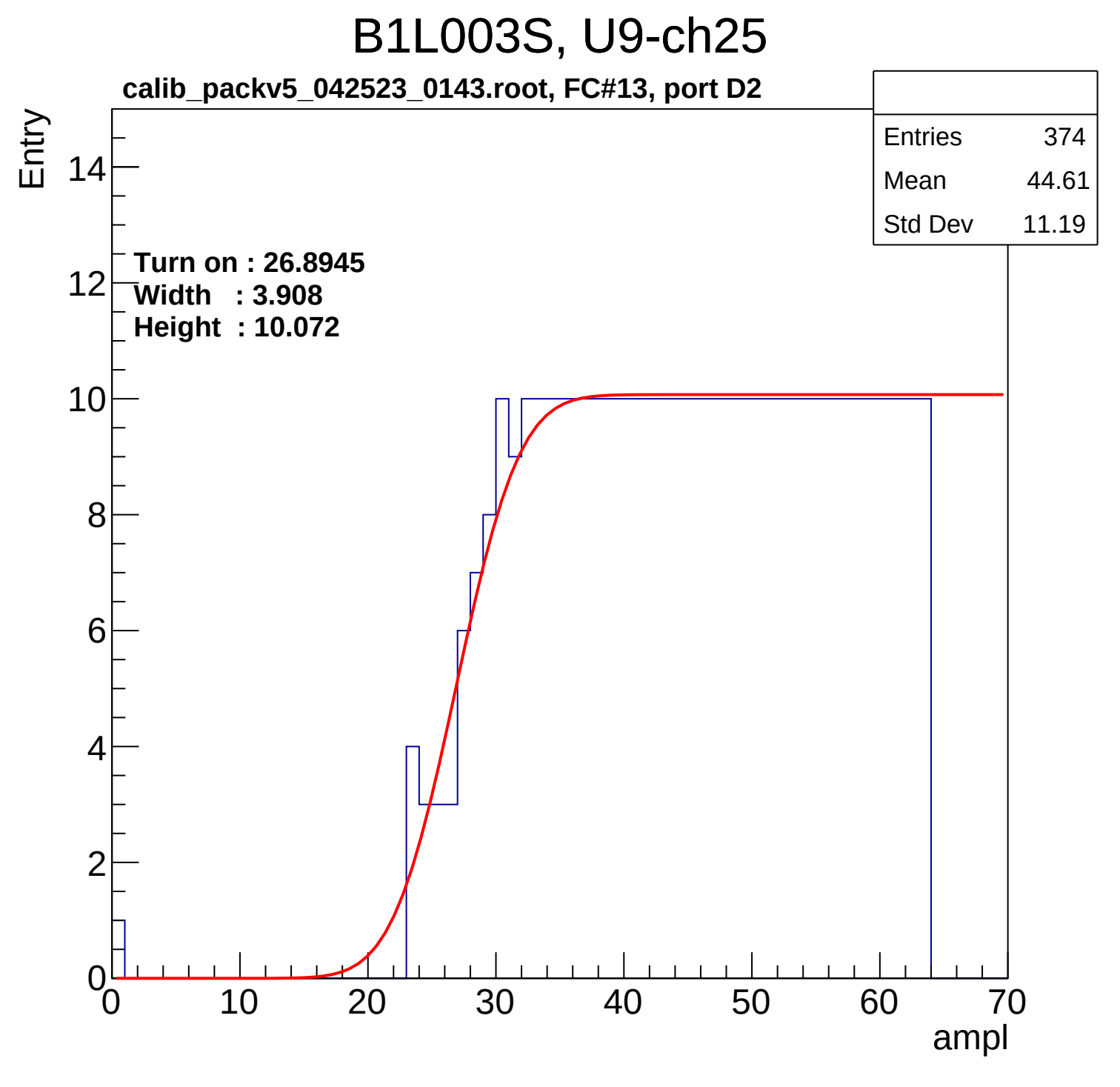

B1L003S, U9-ch20
calib_packv5_042523_0143.root, FC#13, port D2
Entries 382
Mean 44
Std Dev 12.04
Turn on : 26.5589
Width : 2.139
Height : 10.015
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

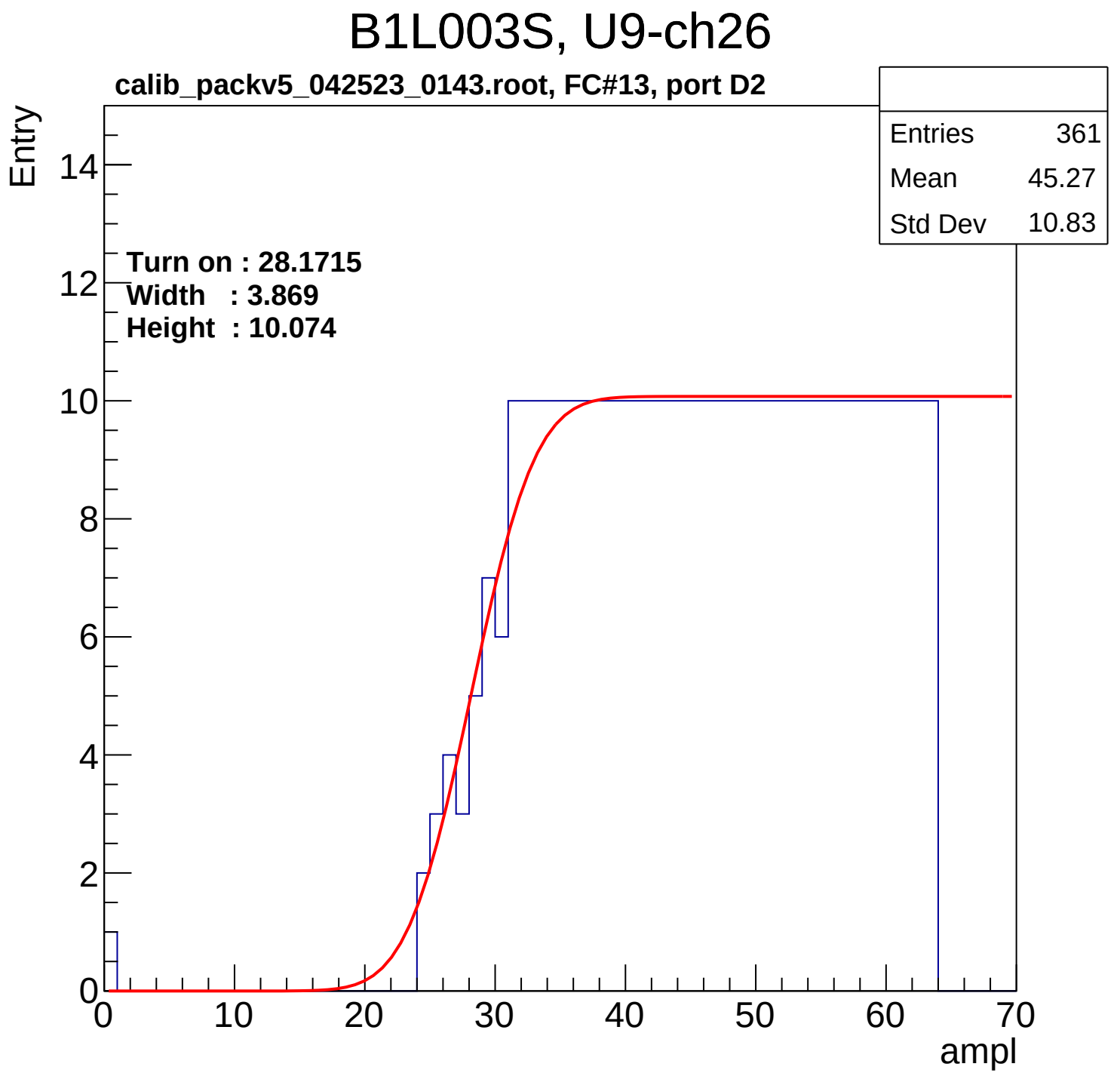

B1L003S, U9-ch21
calib_packv5_042523_0143.root, FC#13, port D2
Entries 377
Mean 44.41
Std Dev 11.44
Turn on : 26.4393
Width : 4.308
Height : 10.075
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

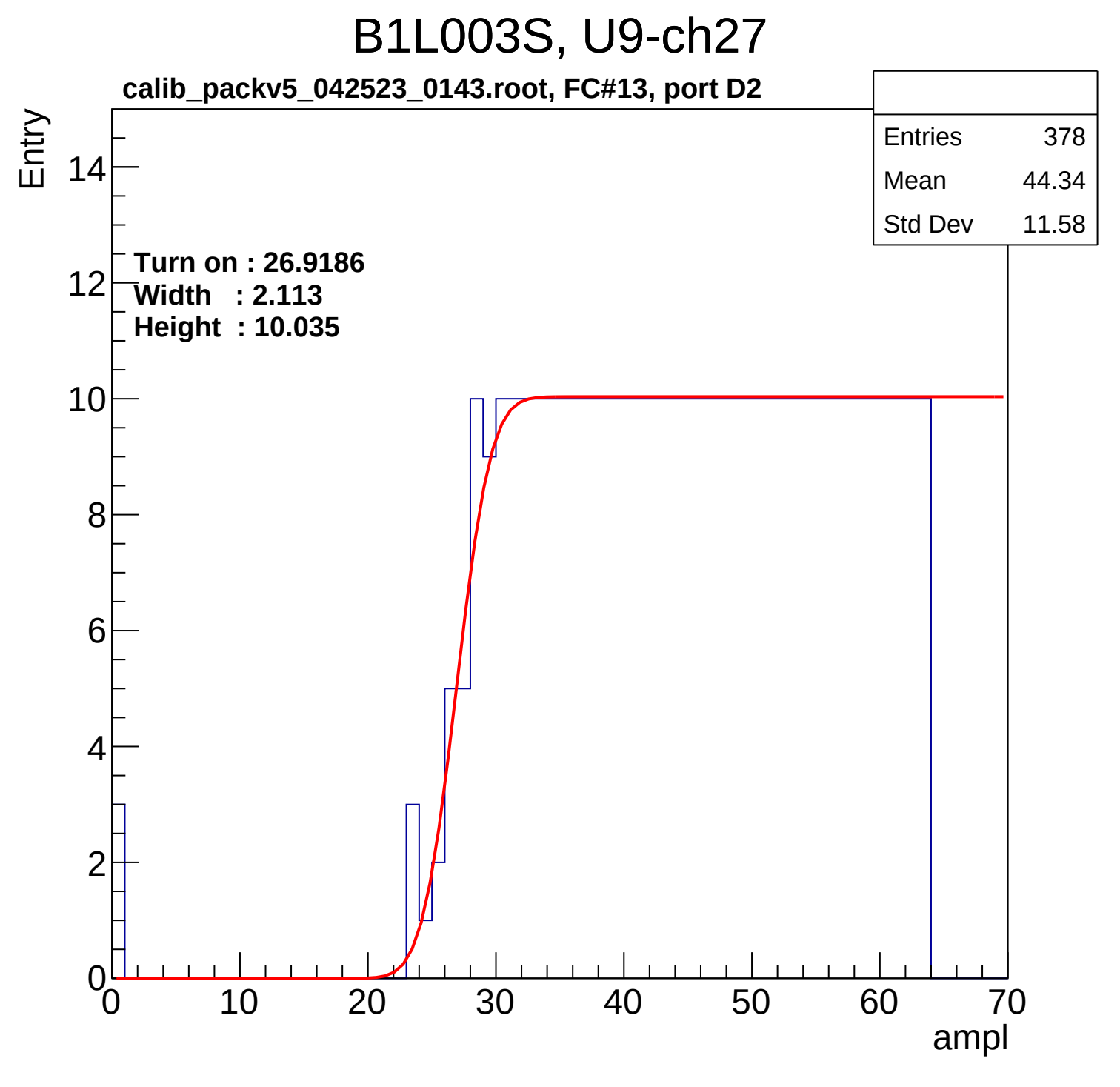

B1L003S, U9-ch22
calib_packv5_042523_0143.root, FC#13, port D2
Entries 377
Mean 44.36
Std Dev 11.6
Turn on : 27.2602
Width : 2.384
Height : 10.037
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

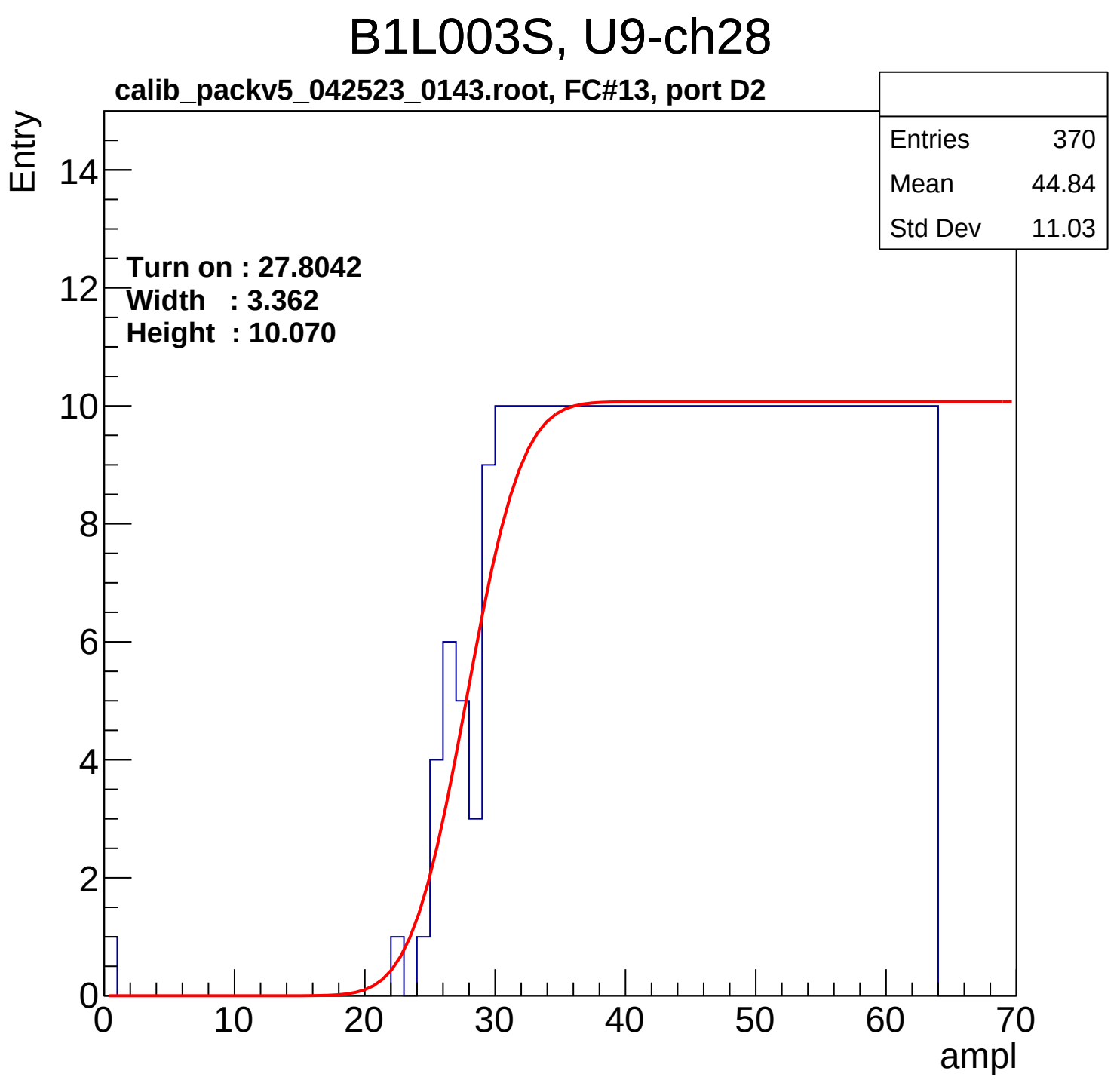

B1L003S, U9-ch23
calib_packv5_042523_0143.root, FC#13, port D2
Entries 379
Mean 44.38
Std Dev 11.3
Turn on : 26.3547
Width : 2.669
Height : 9.988
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

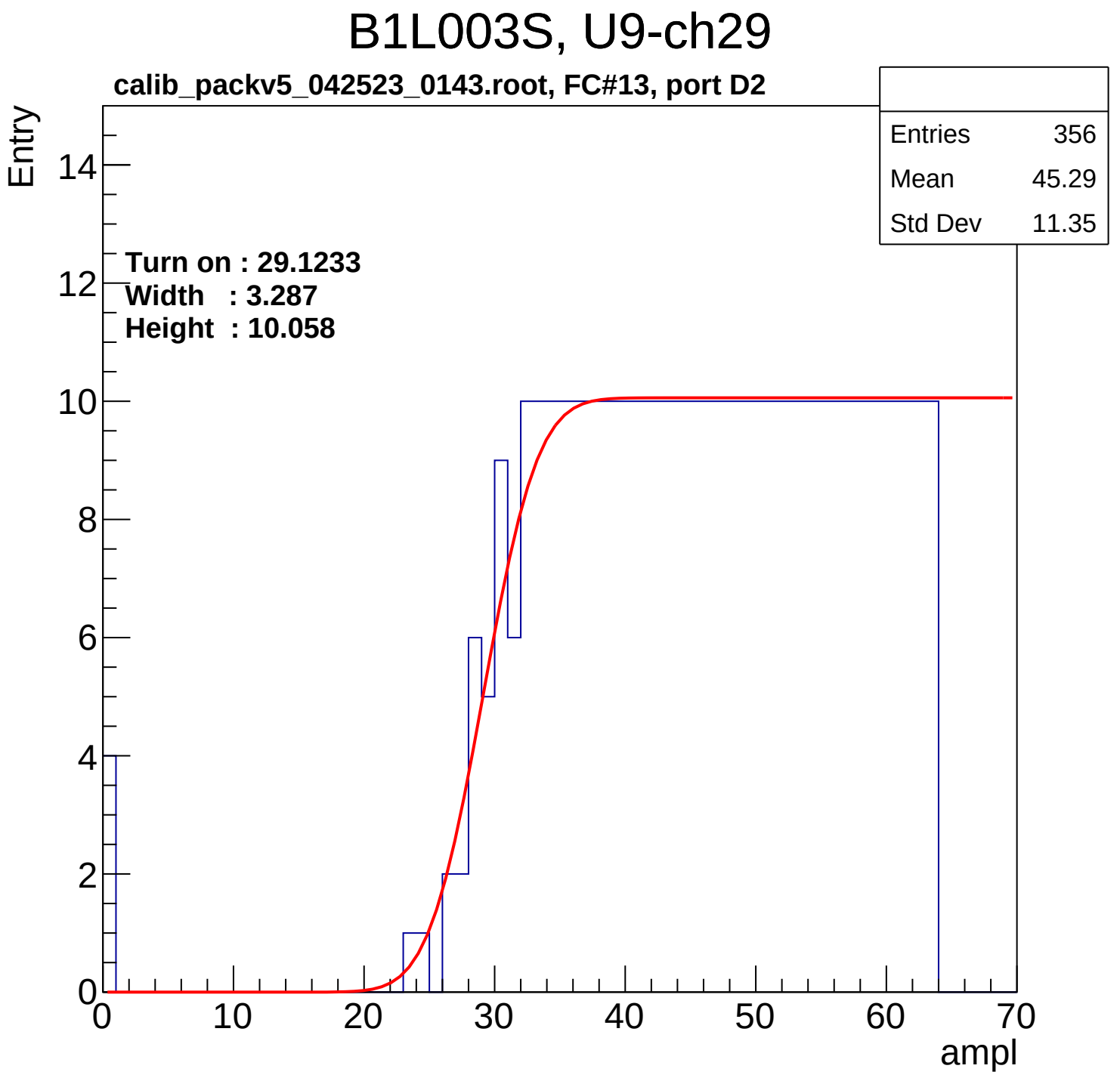

B1L003S, U9-ch24
calib_packv5_042523_0143.root, FC#13, port D2
Entries 375
Mean 44.63
Std Dev 11.11
Turn on : 26.5251
Width : 2.425
Height : 10.012
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

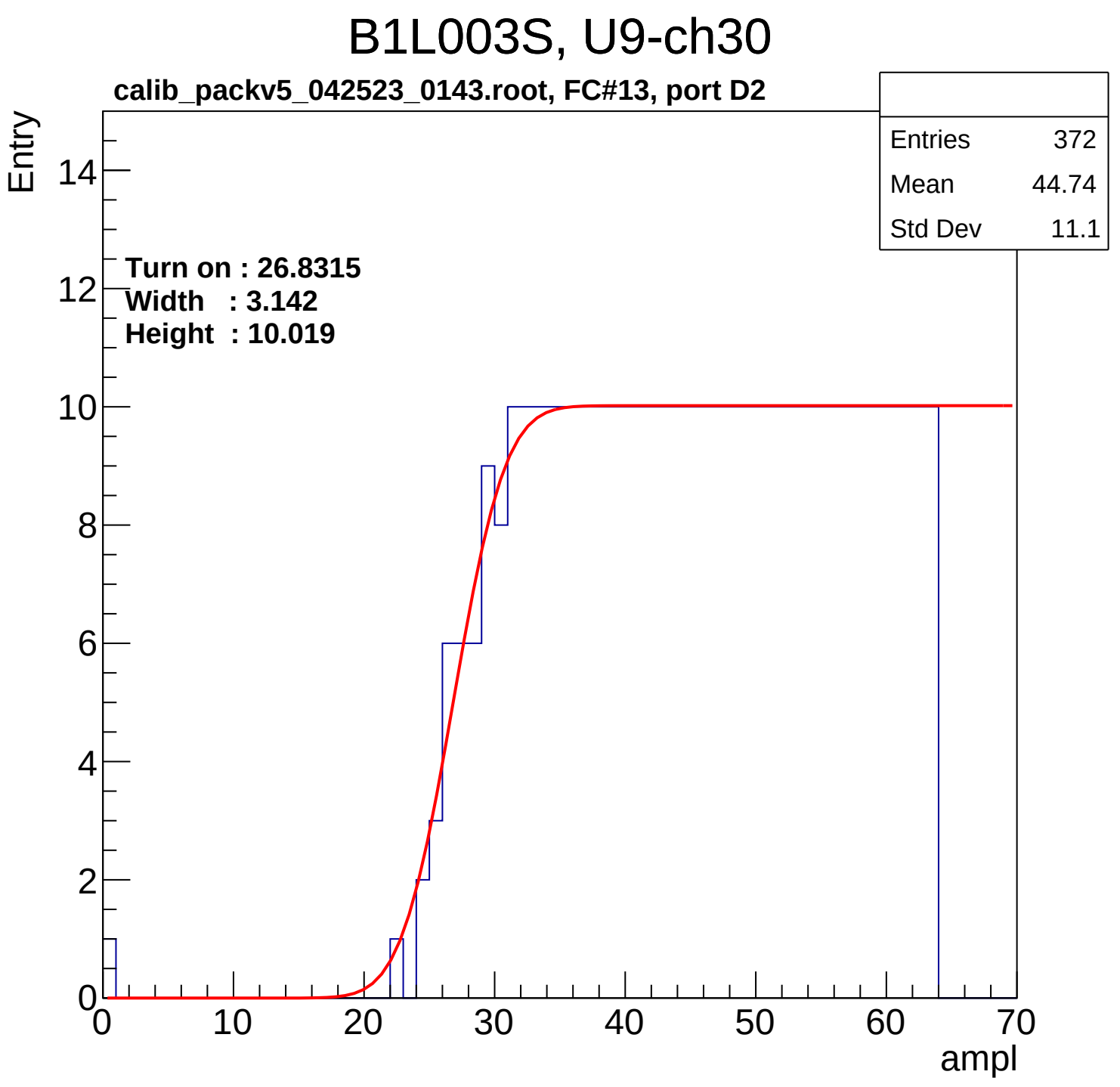

B1L003S, U9-ch25
calib_packv5_042523_0143.root, FC#13, port D2
Entries 374
Mean 44.61
Std Dev 11.19
Turn on : 26.8945
Width : 3.908
Height : 10.072
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

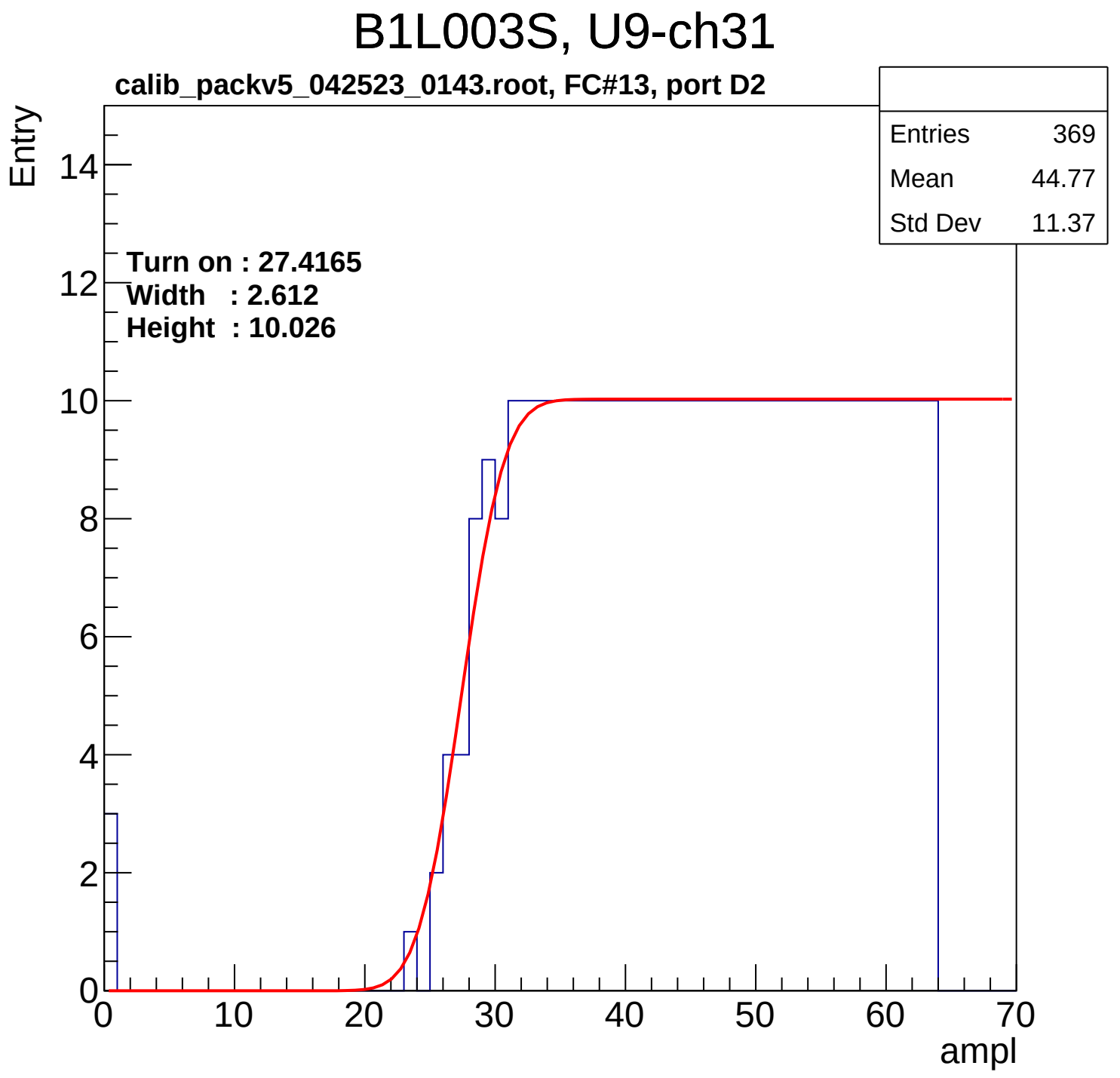

B1L003S, U9-ch26
calib_packv5_042523_0143.root, FC#13, port D2
Entries 361
Mean 45.27
Std Dev 10.83
Turn on : 28.1715
Width : 3.869
Height : 10.074
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

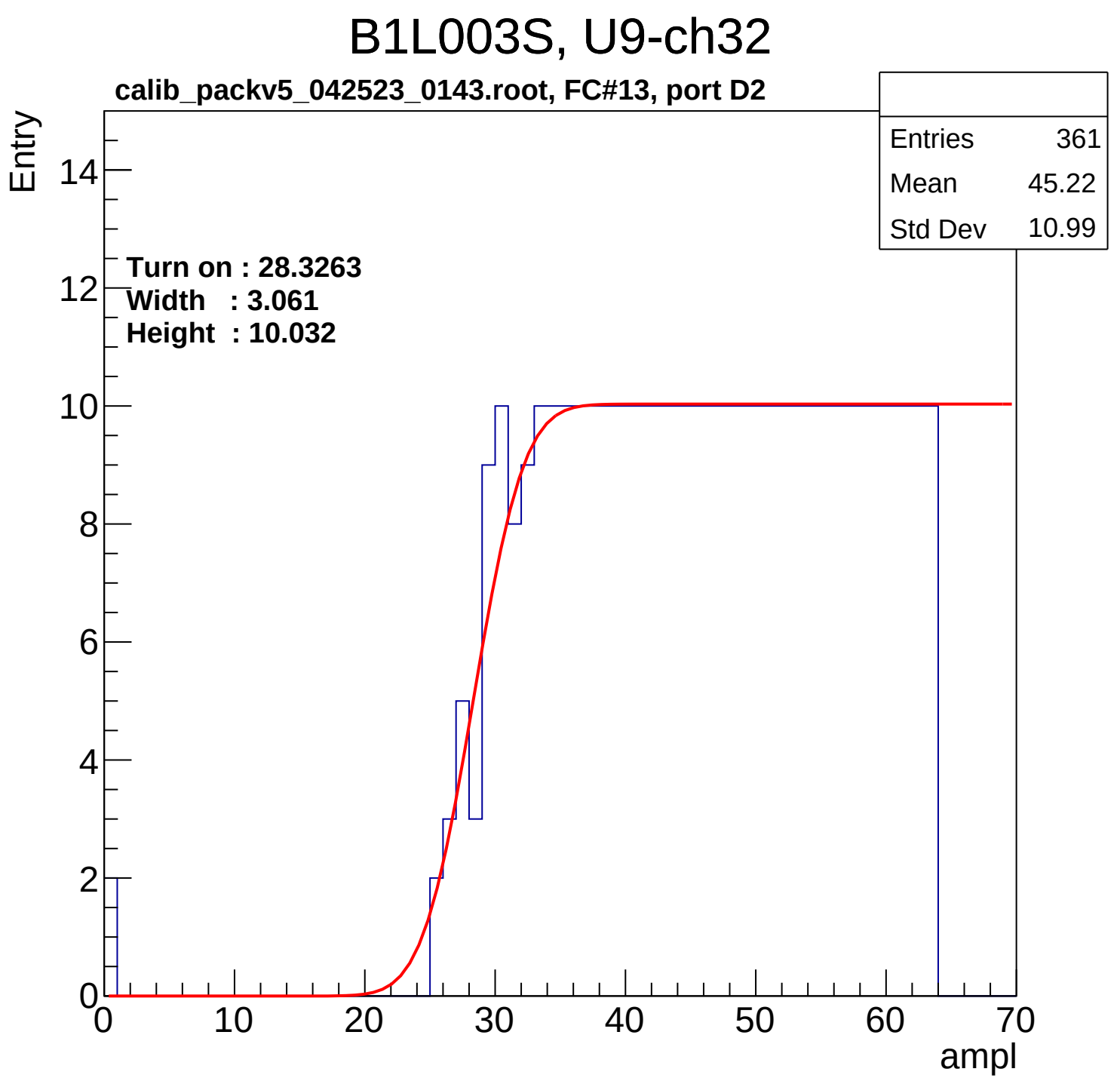

B1L003S, U9-ch27
calib_packv5_042523_0143.root, FC#13, port D2
Entries 378
Mean 44.34
Std Dev 11.58
Turn on : 26.9186
Width : 2.113
Height : 10.035
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

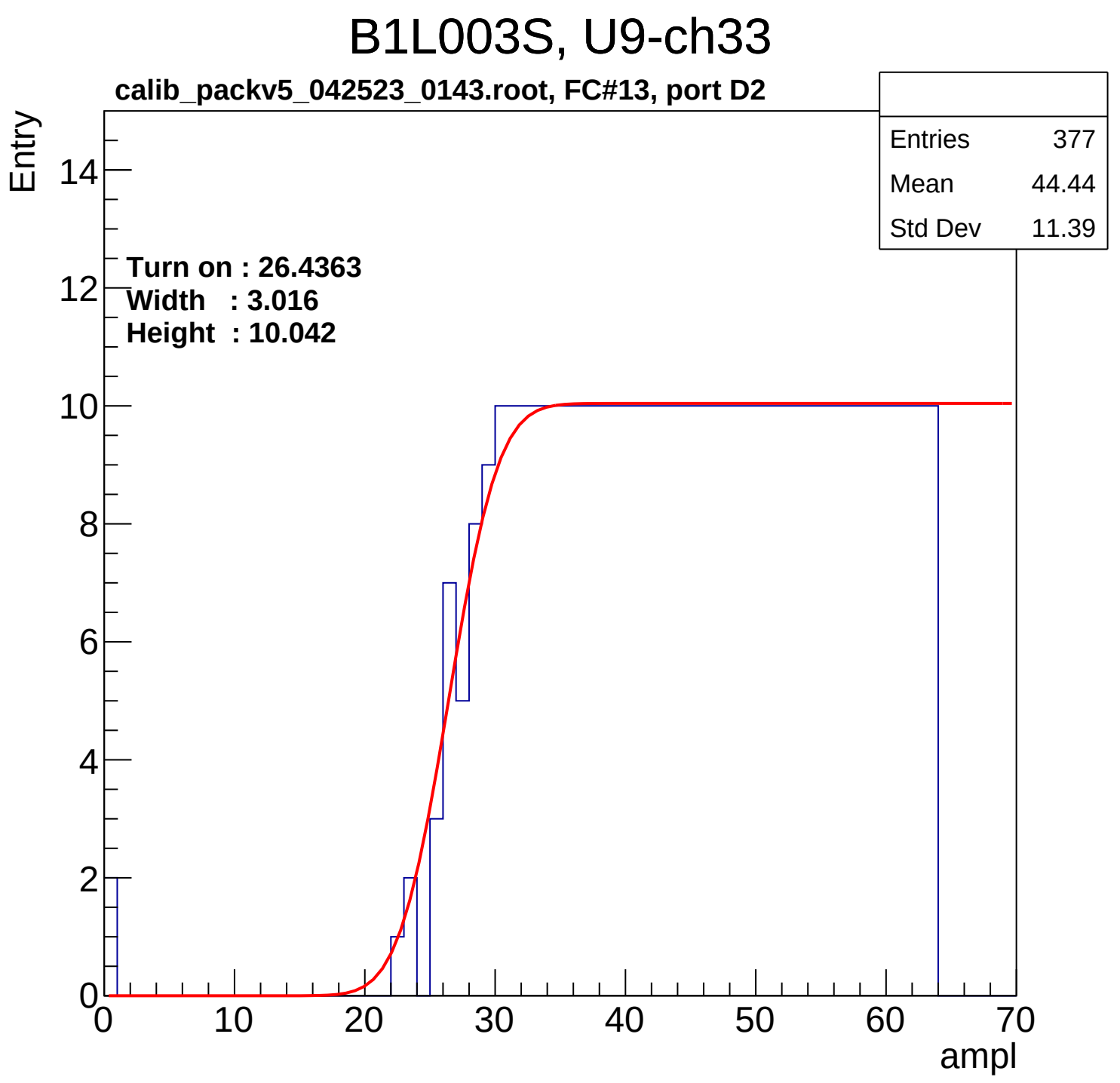

B1L003S, U9-ch28
calib_packv5_042523_0143.root, FC#13, port D2
Entries 370
Mean 44.84
Std Dev 11.03
Turn on : 27.8042
Width : 3.362
Height : 10.070
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

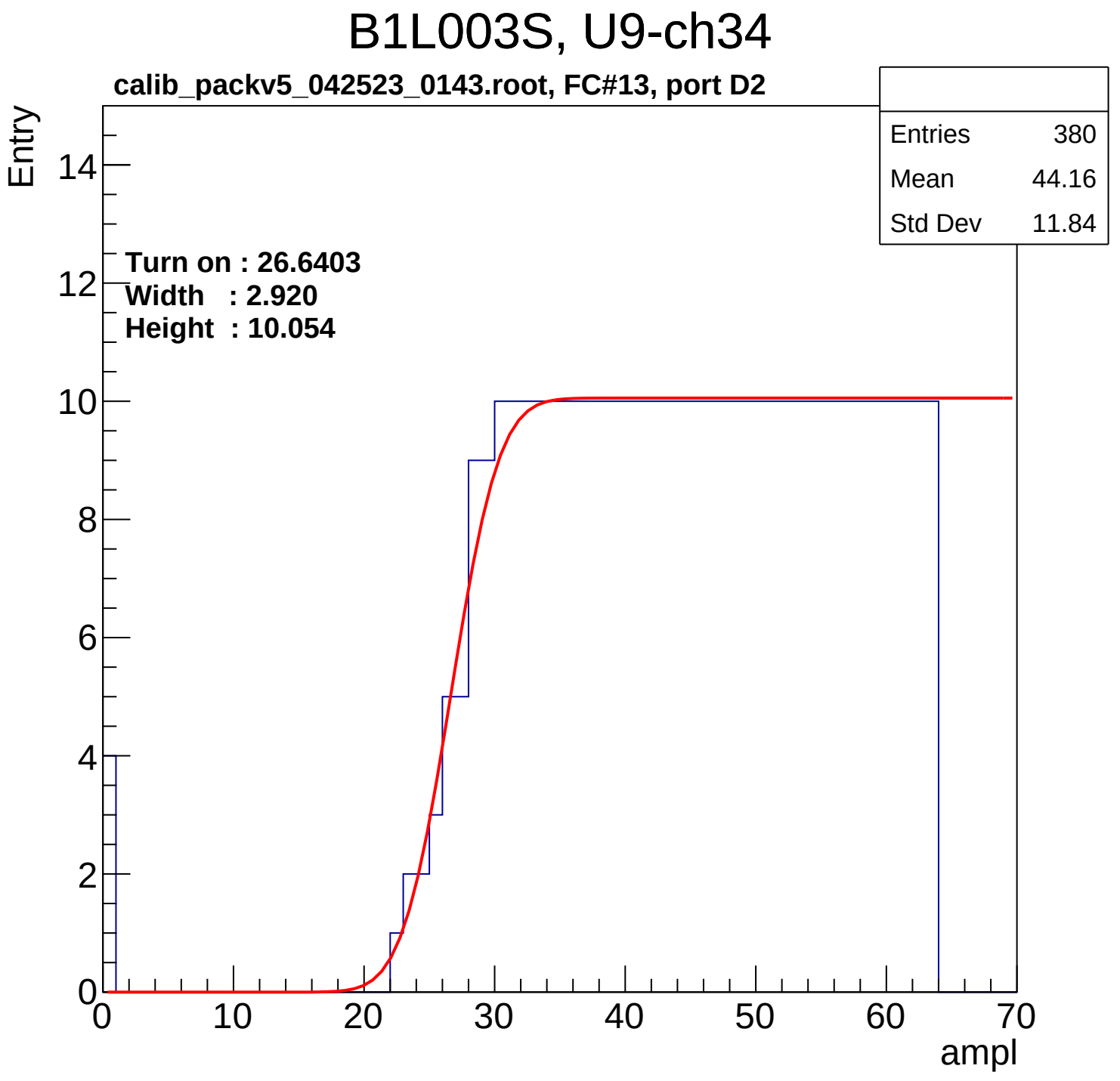

B1L003S, U9-ch29
calib_packv5_042523_0143.root, FC#13, port D2
Entries 356
Mean 45.29
Std Dev 11.35
Turn on : 29.1233
Width : 3.287
Height : 10.058
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

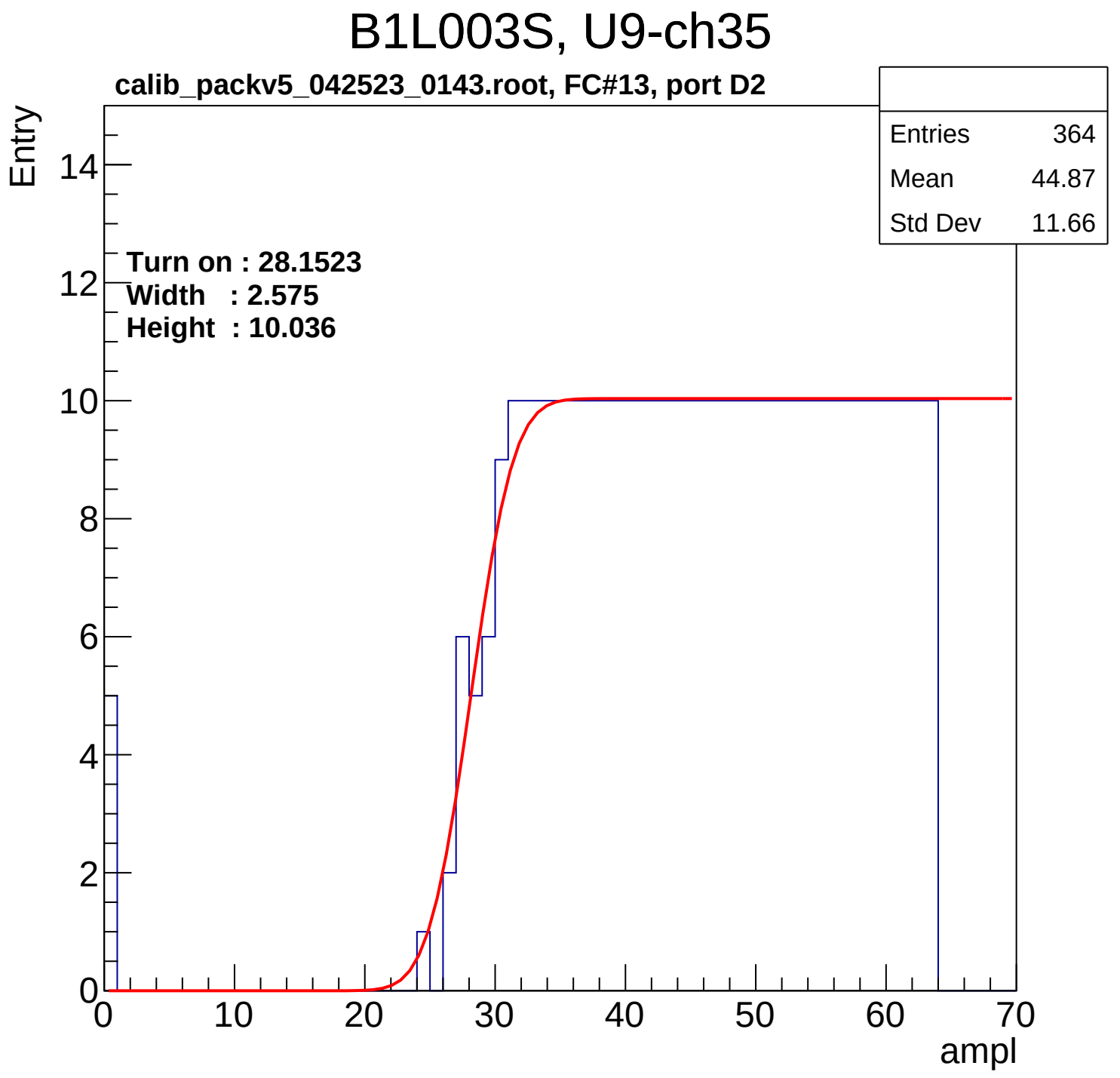

B1L003S, U9-ch30
calib_packv5_042523_0143.root, FC#13, port D2
Entries 372
Mean 44.74
Std Dev 11.1
Turn on : 26.8315
Width : 3.142
Height : 10.019
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

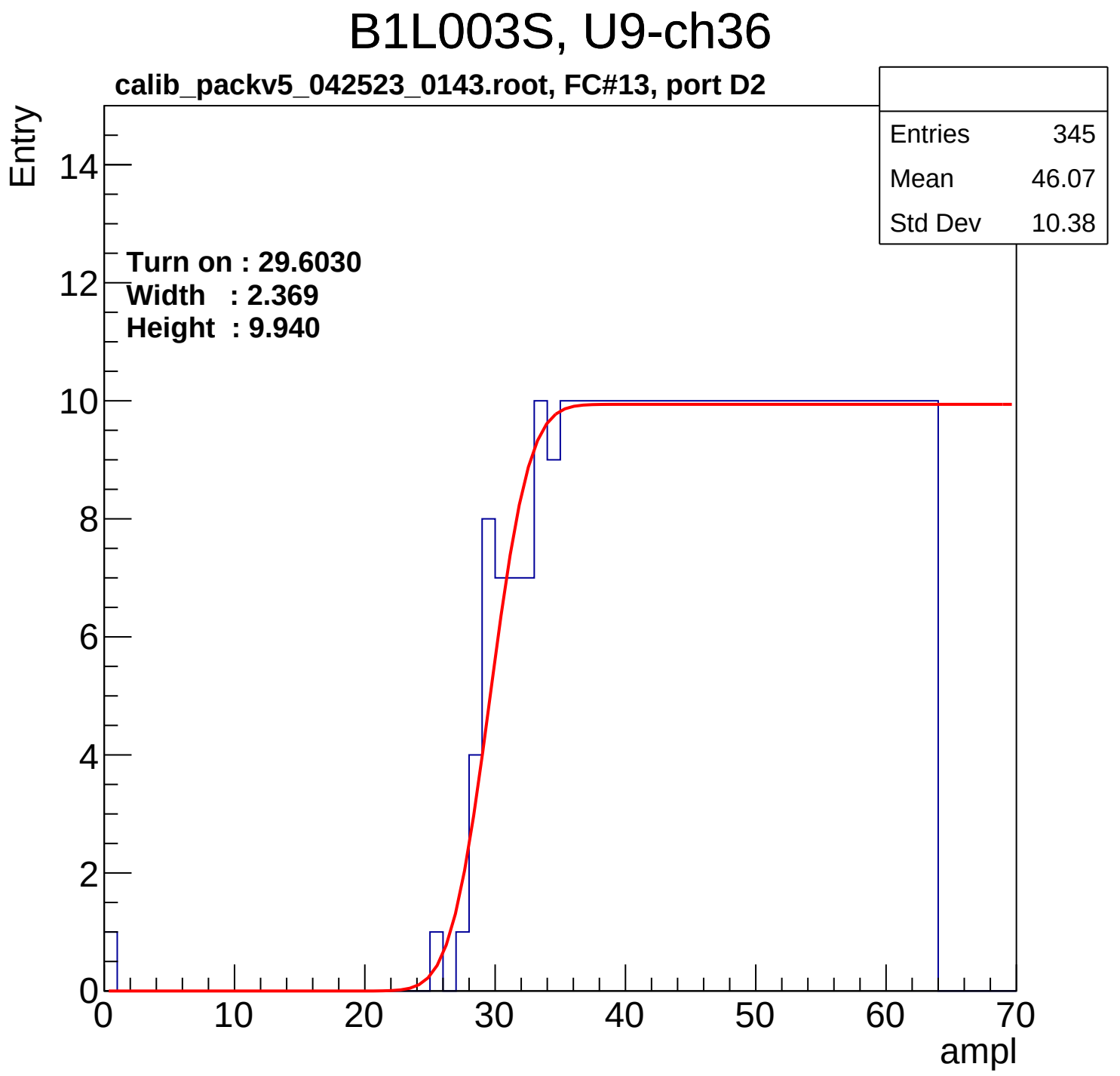

B1L003S, U9-ch31
calib_packv5_042523_0143.root, FC#13, port D2
Entries 369
Mean 44.77
Std Dev 11.37
Turn on : 27.4165
Width : 2.612
Height : 10.026
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

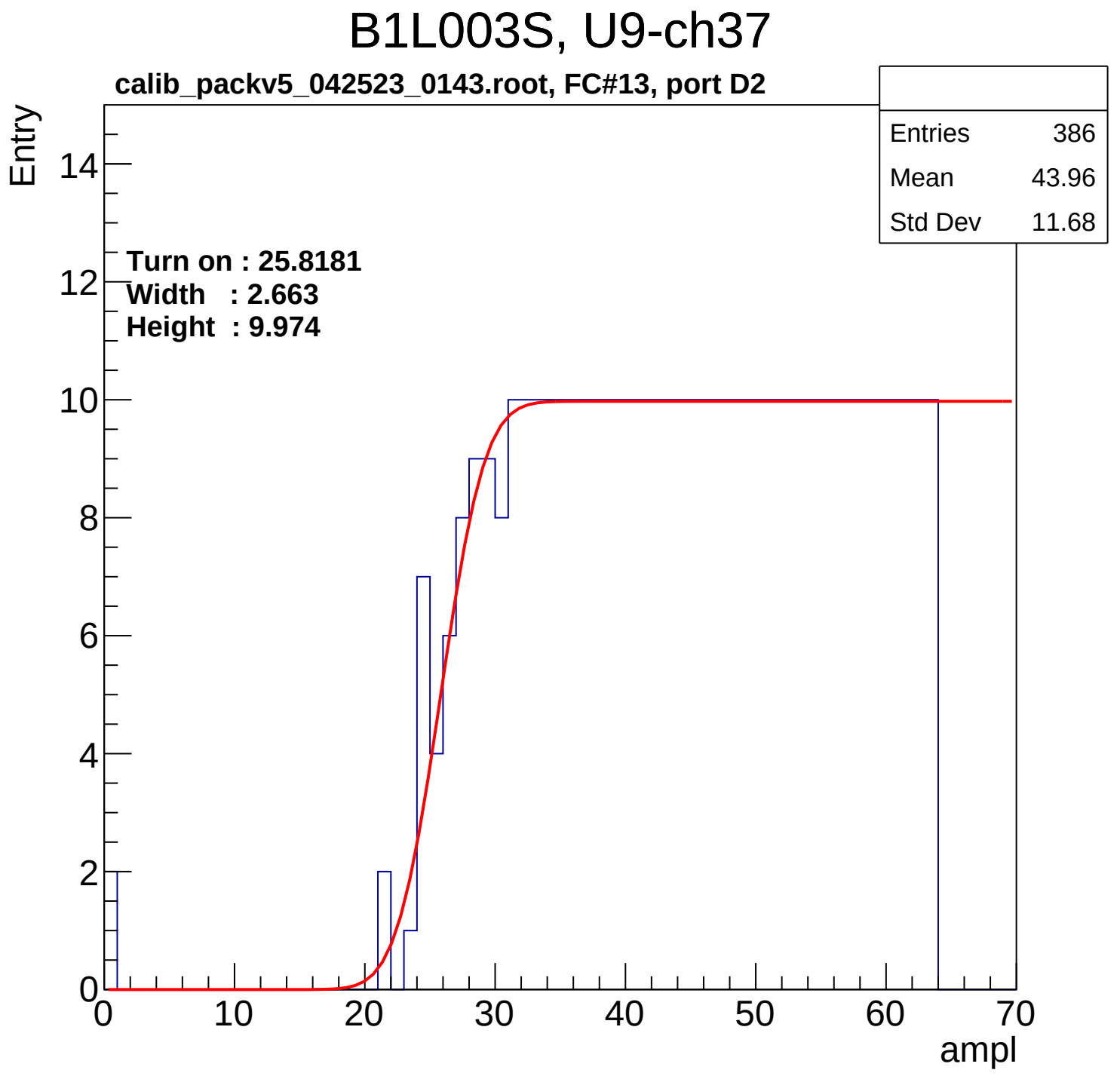

B1L003S, U9-ch32
calib_packv5_042523_0143.root, FC#13, port D2
Entries 361
Mean 45.22
Std Dev 10.99
Turn on : 28.3263
Width : 3.061
Height : 10.032
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

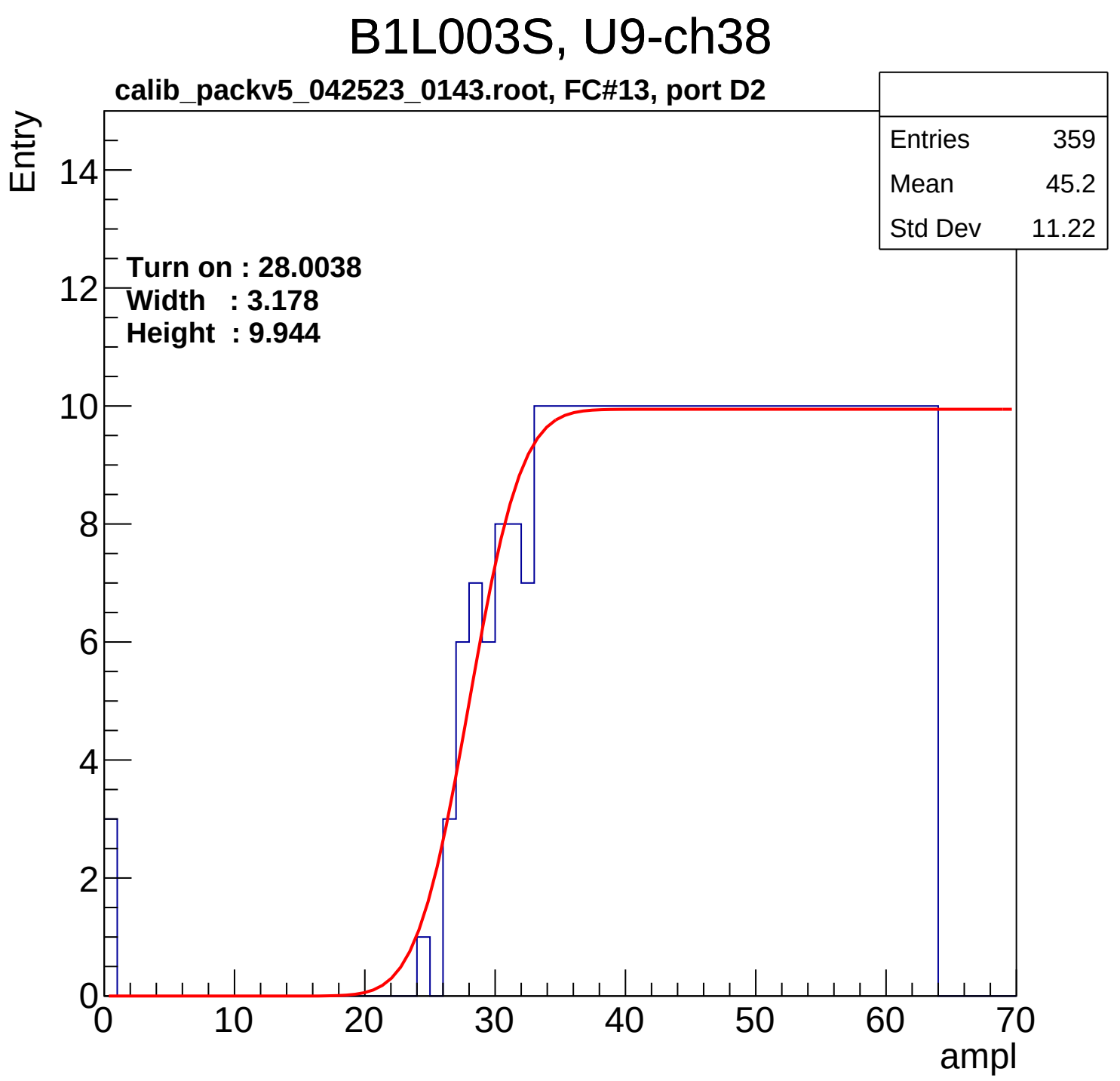

B1L003S, U9-ch33
calib_packv5_042523_0143.root, FC#13, port D2
Entries 377
Mean 44.44
Std Dev 11.39
Turn on : 26.4363
Width : 3.016
Height : 10.042
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

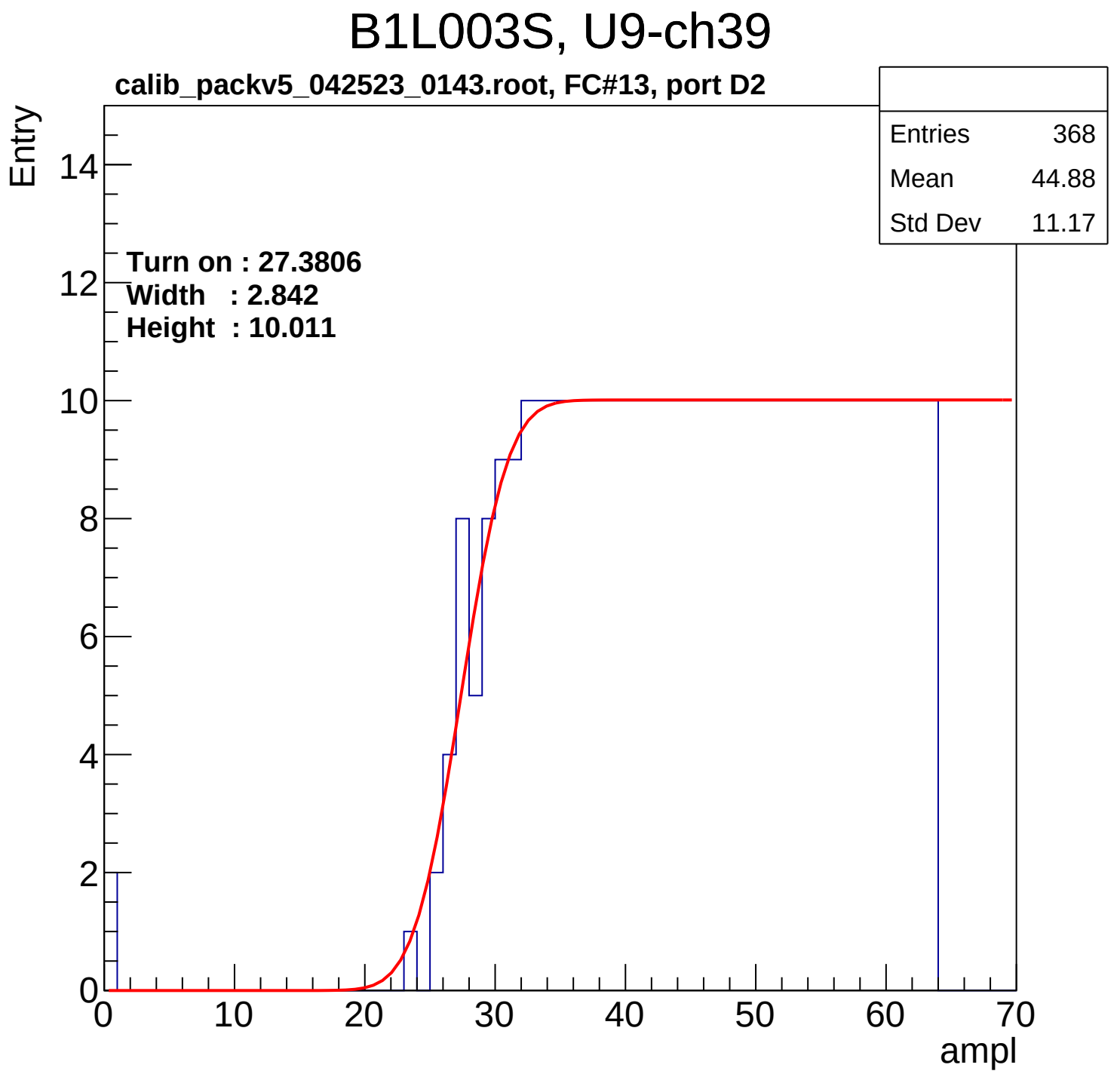

B1L003S, U9-ch34
calib_packv5_042523_0143.root, FC#13, port D2
Entries 380
Mean 44.16
Std Dev 11.84
Turn on : 26.6403
Width : 2.920
Height : 10.054
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

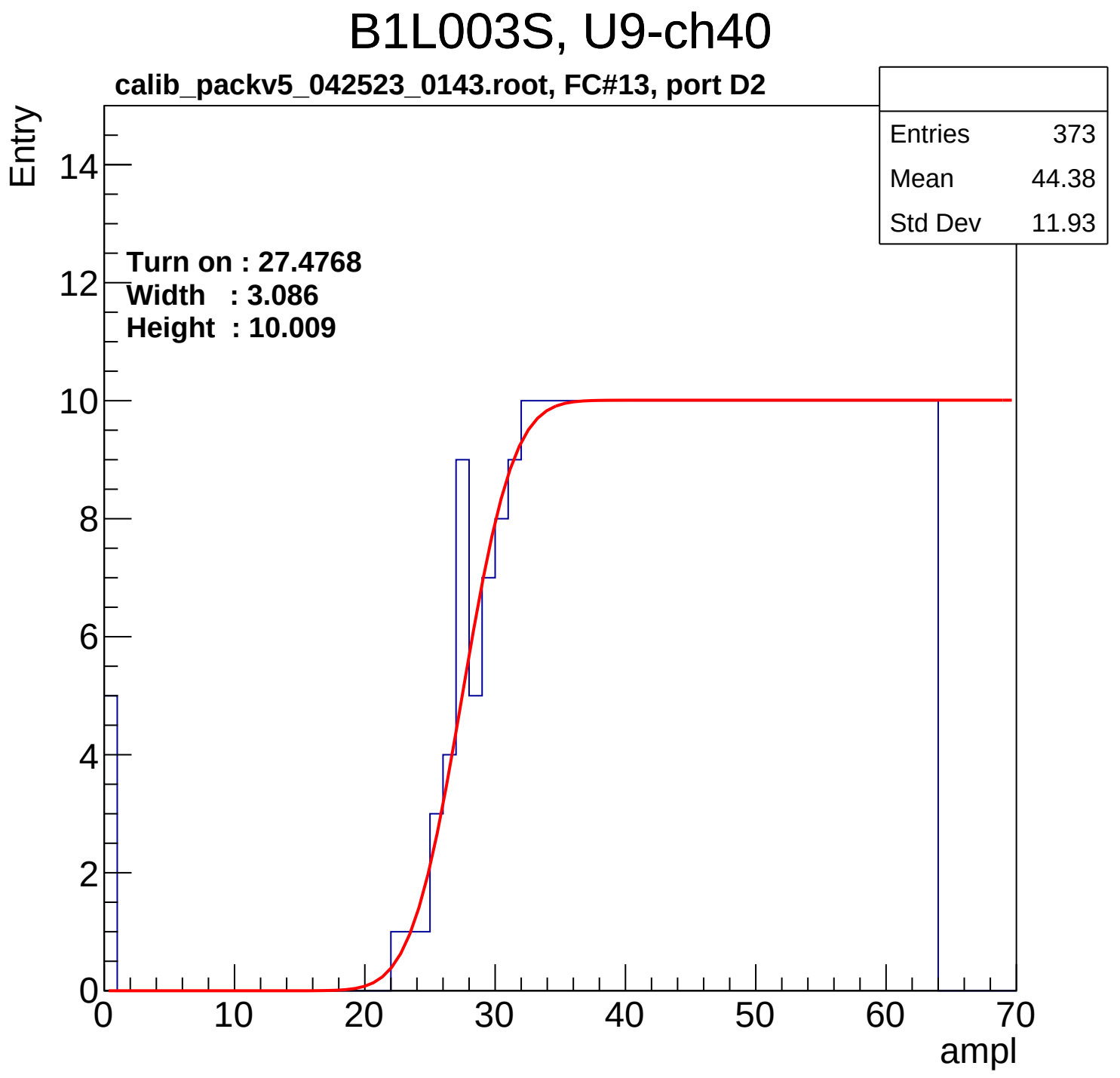

B1L003S, U9-ch35
calib_packv5_042523_0143.root, FC#13, port D2
Entries 364
Mean 44.87
Std Dev 11.66
Turn on : 28.1523
Width : 2.575
Height : 10.036
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

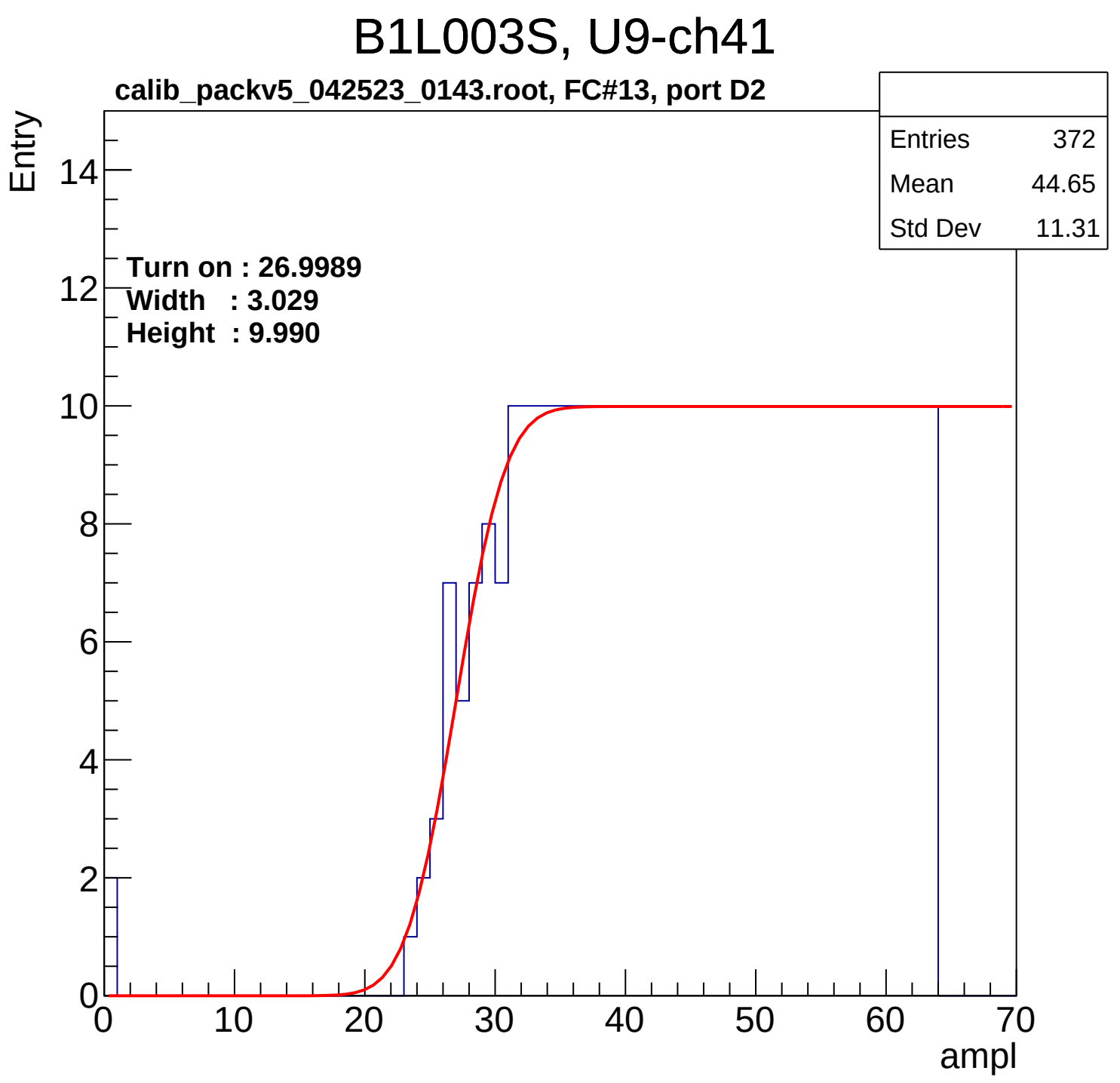

B1L003S, U9-ch36
calib_packv5_042523_0143.root, FC#13, port D2
Entries 345
Mean 46.07
Std Dev 10.38
Turn on : 29.6030
Width : 2.369
Height : 9.940
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

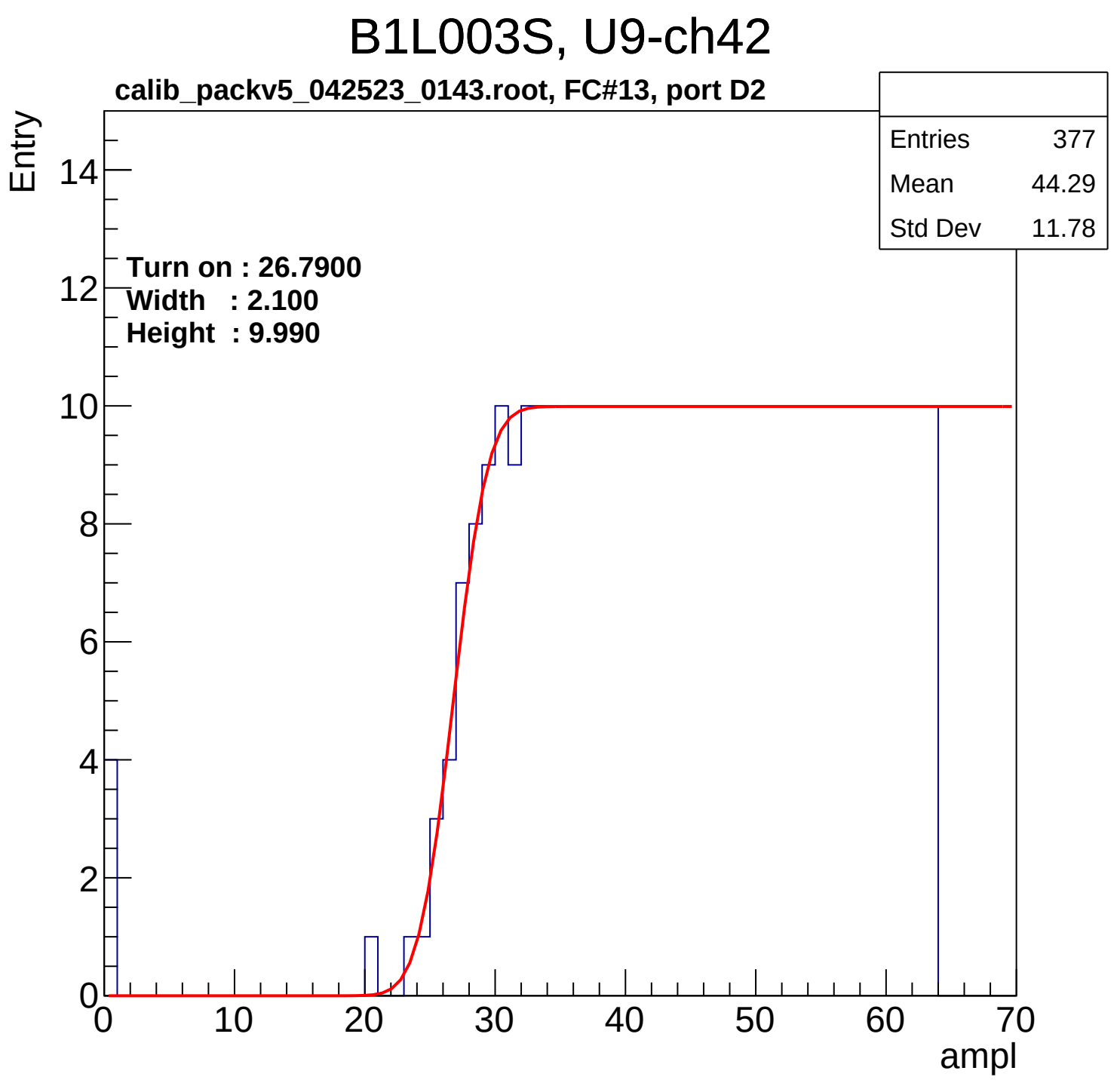

B1L003S, U9-ch37
calib_packv5_042523_0143.root, FC#13, port D2
Entries 386
Mean 43.96
Std Dev 11.68
Turn on : 25.8181
Width : 2.663
Height : 9.974
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

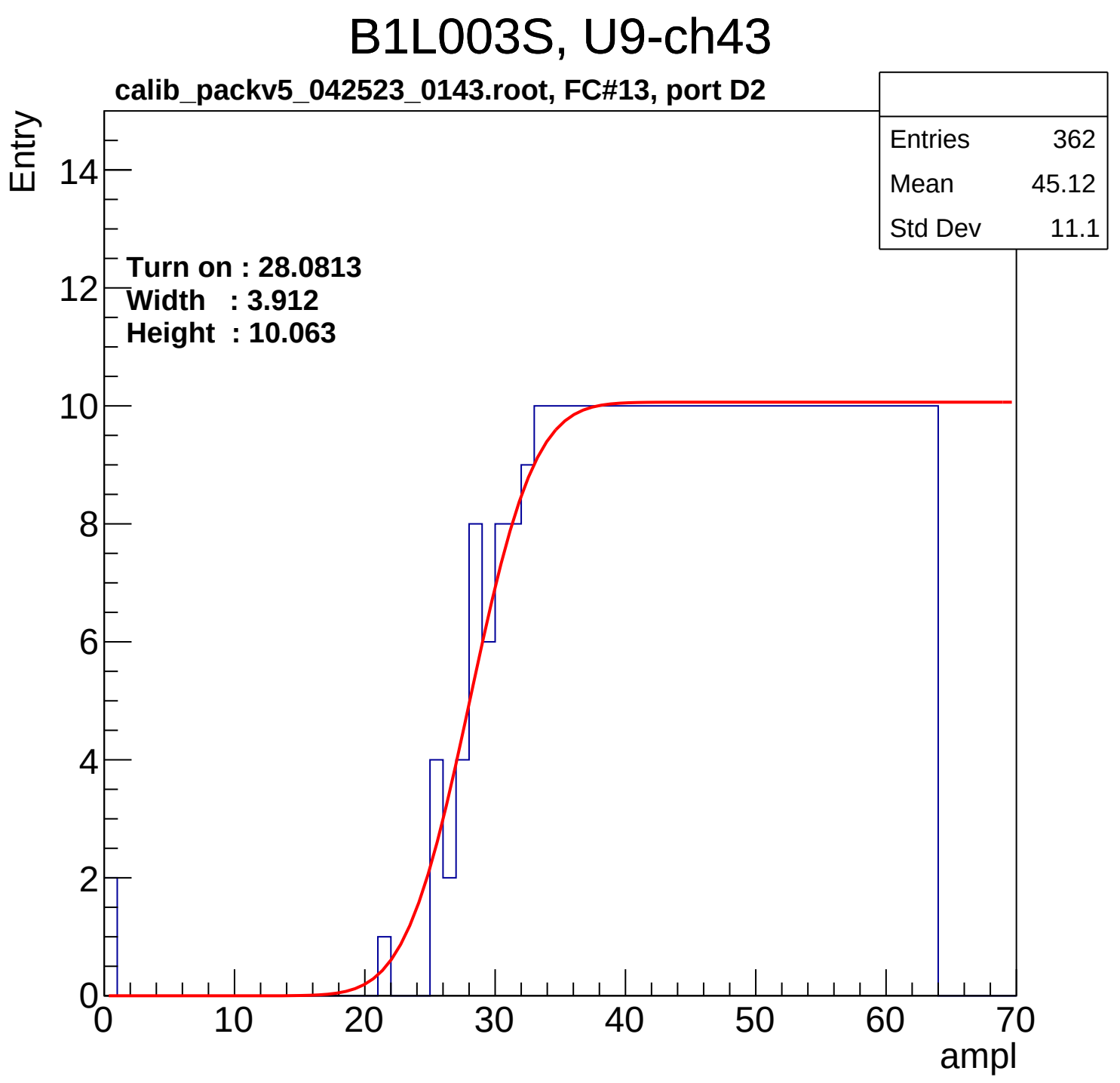

B1L003S, U9-ch38
calib_packv5_042523_0143.root, FC#13, port D2
Entries 359
Mean 45.2
Std Dev 11.22
Turn on : 28.0038
Width : 3.178
Height : 9.944
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

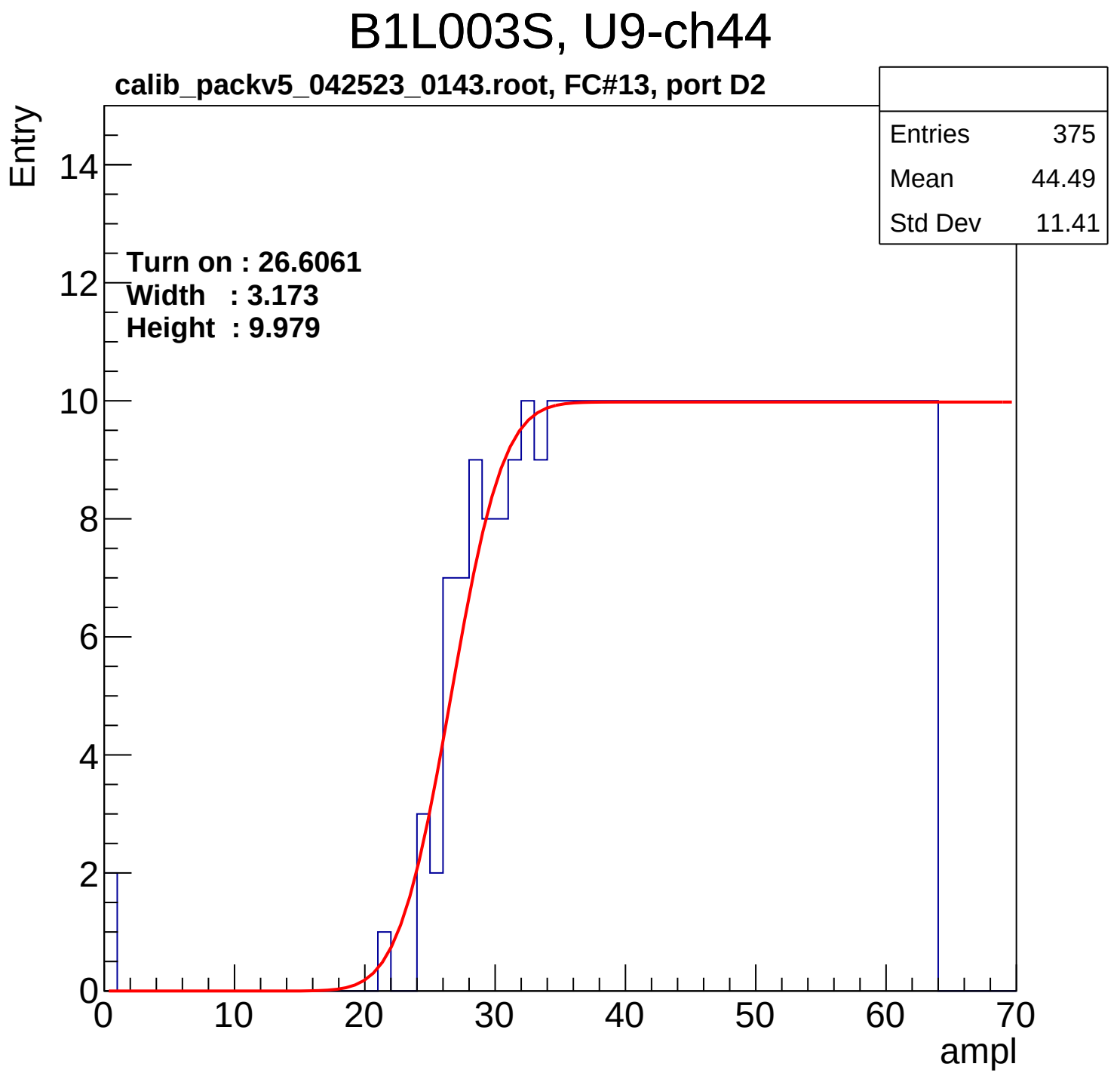

B1L003S, U9-ch39
calib_packv5_042523_0143.root, FC#13, port D2
Entries 368
Mean 44.88
Std Dev 11.17
Turn on : 27.3806
Width : 2.842
Height : 10.011
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

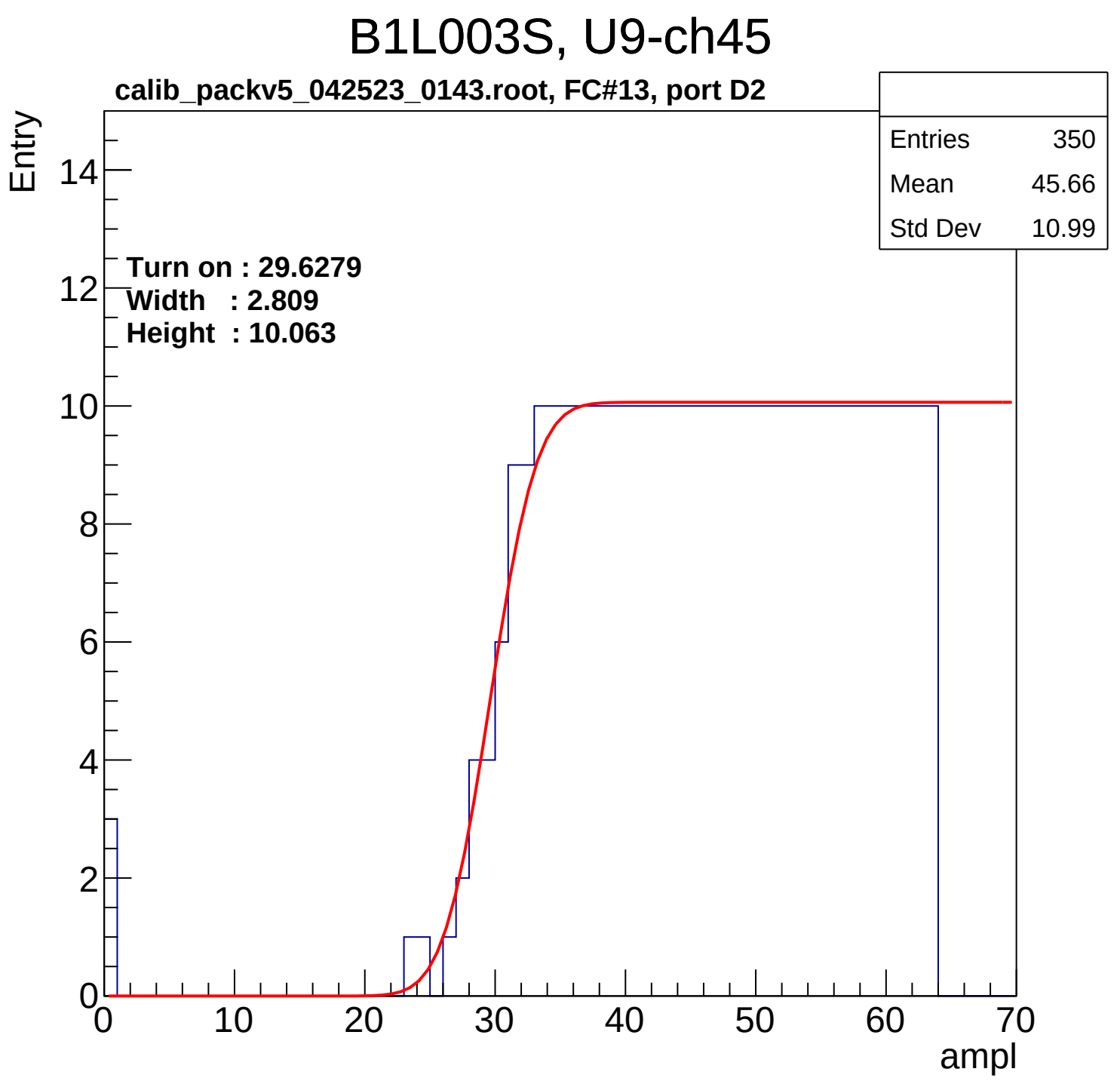

B1L003S, U9-ch40
calib_packv5_042523_0143.root, FC#13, port D2
Entries 373
Mean 44.38
Std Dev 11.93
Turn on : 27.4768
Width : 3.086
Height : 10.009
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

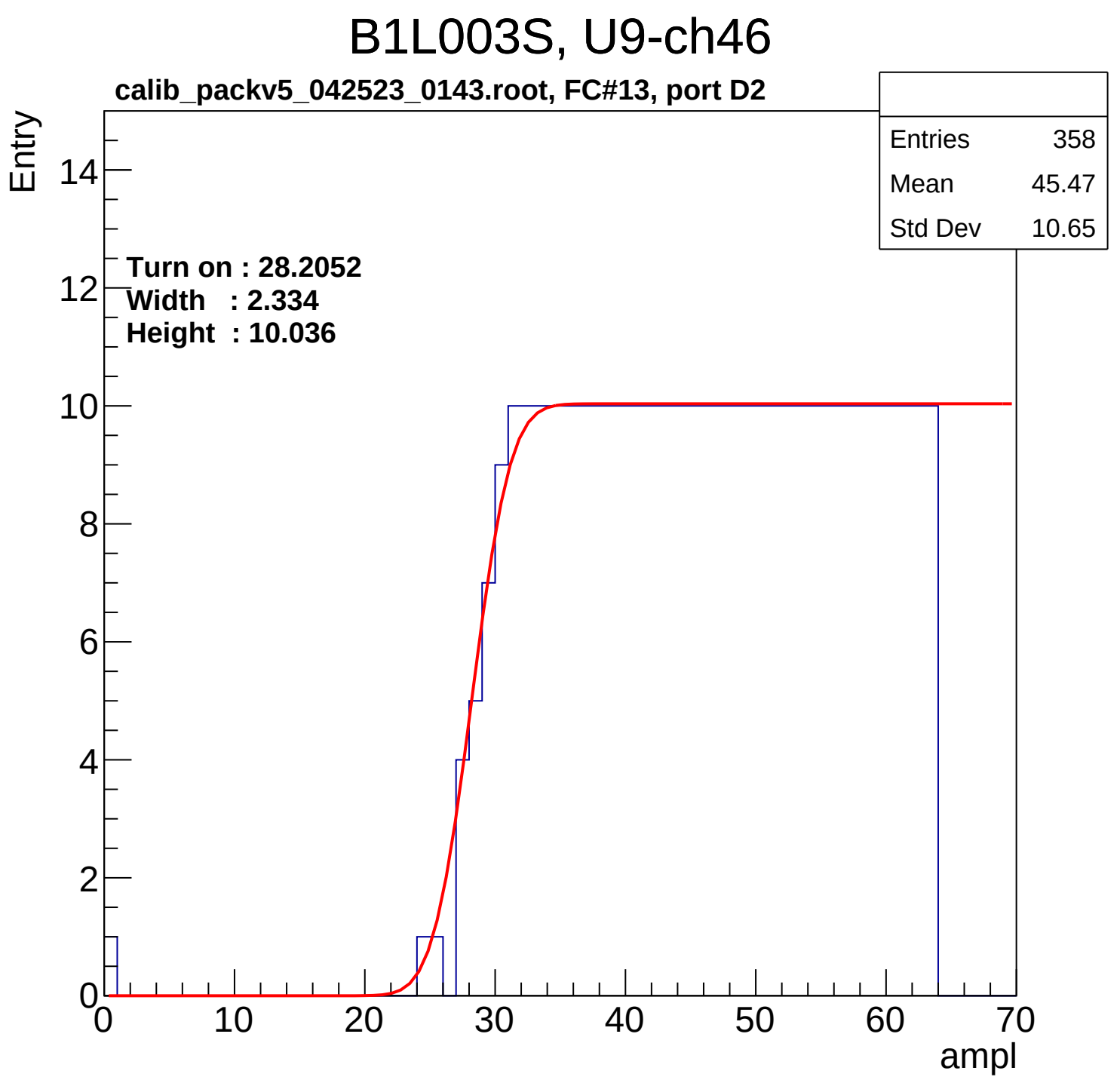

B1L003S, U9-ch41
calib_packv5_042523_0143.root, FC#13, port D2
Entries 372
Mean 44.65
Std Dev 11.31
Turn on : 26.9989
Width : 3.029
Height : 9.990
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

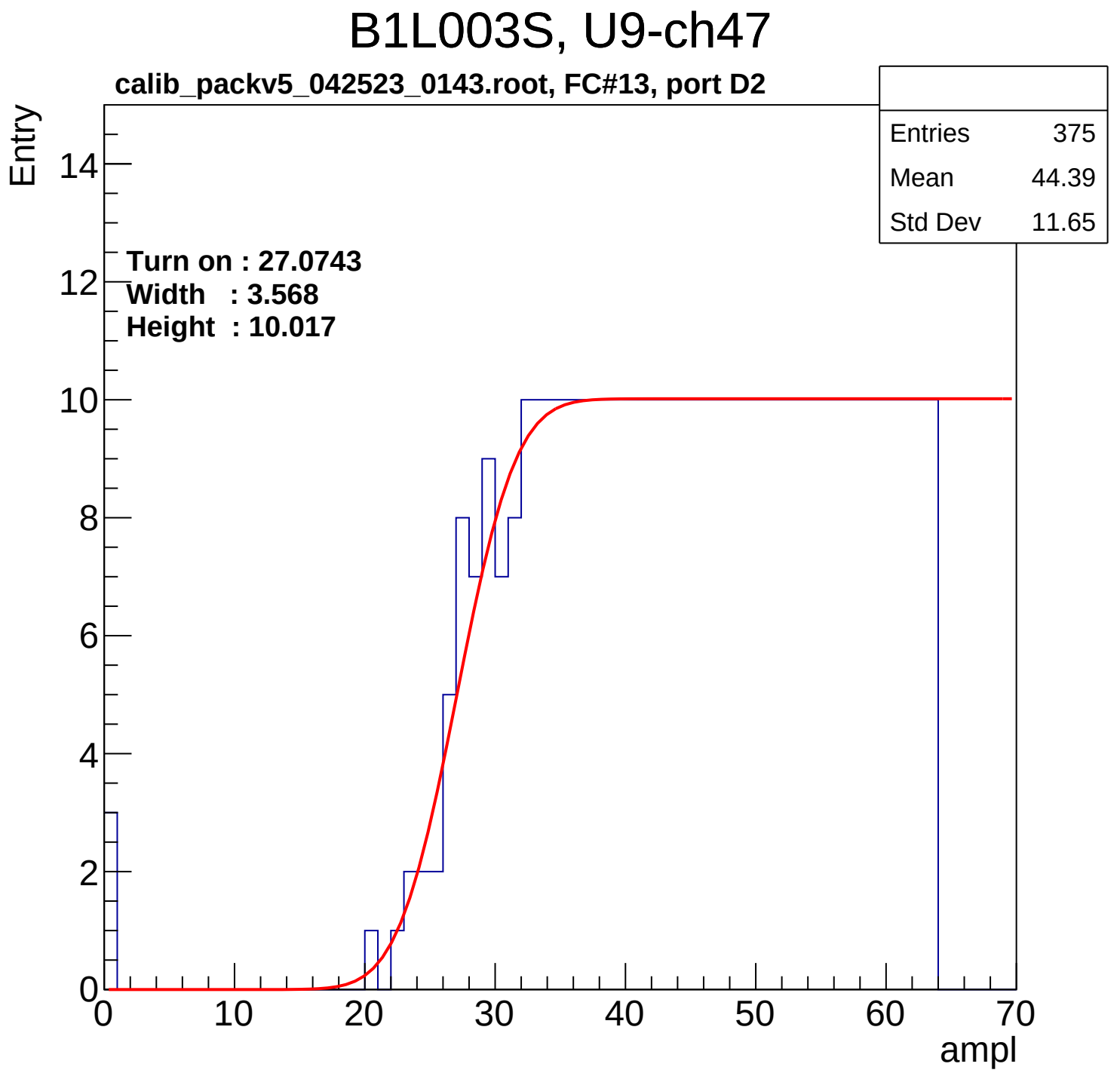

B1L003S, U9-ch42
calib_packv5_042523_0143.root, FC#13, port D2
Entries 377
Mean 44.29
Std Dev 11.78
Turn on : 26.7900
Width : 2.100
Height : 9.990
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

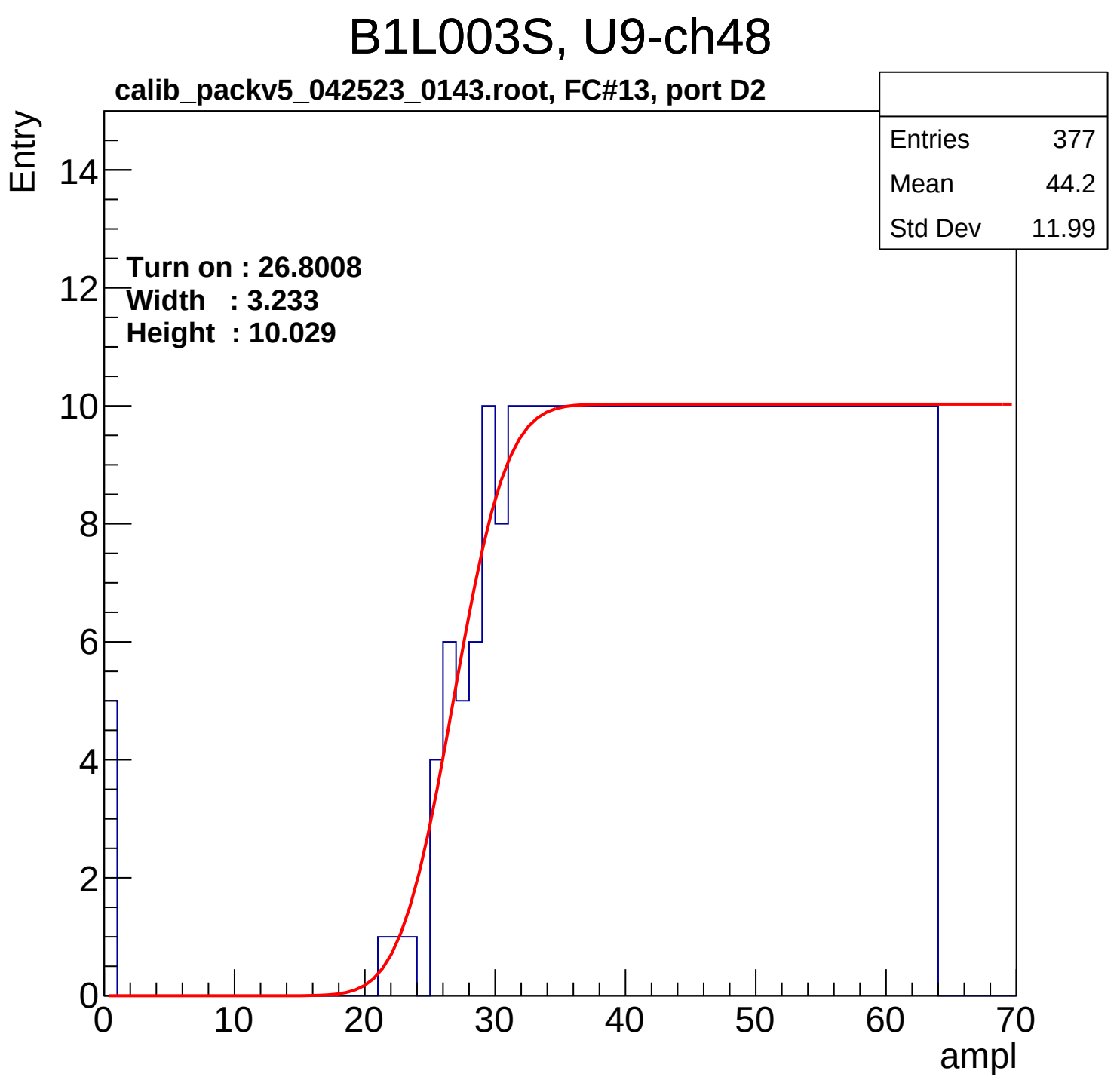

B1L003S, U9-ch43
calib_packv5_042523_0143.root, FC#13, port D2
Entries 362
Mean 45.12
Std Dev 11.1
Turn on : 28.0813
Width : 3.912
Height : 10.063
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

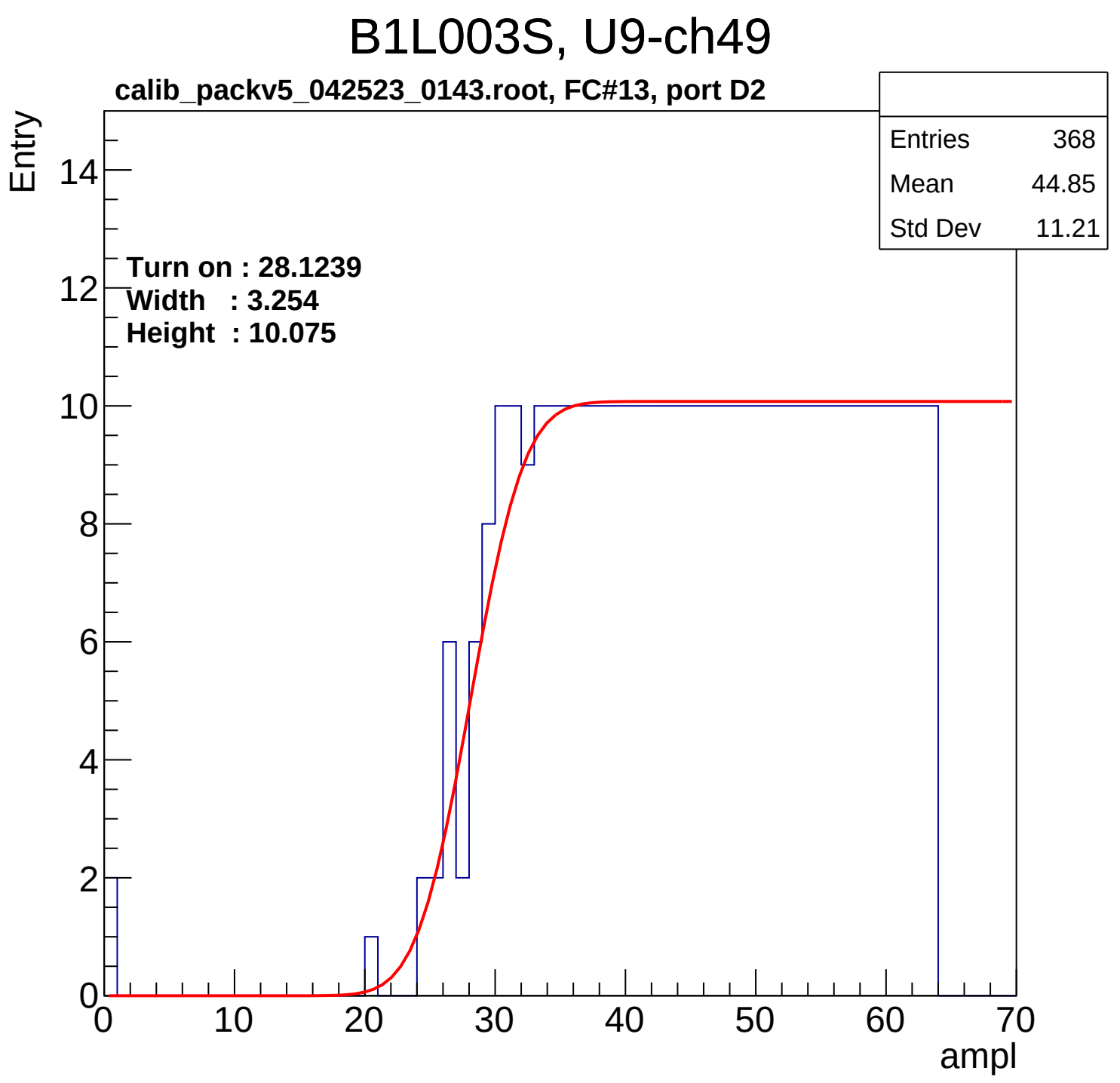

B1L003S, U9-ch44
calib_packv5_042523_0143.root, FC#13, port D2
Entries 375
Mean 44.49
Std Dev 11.41
Turn on : 26.6061
Width : 3.173
Height : 9.979
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

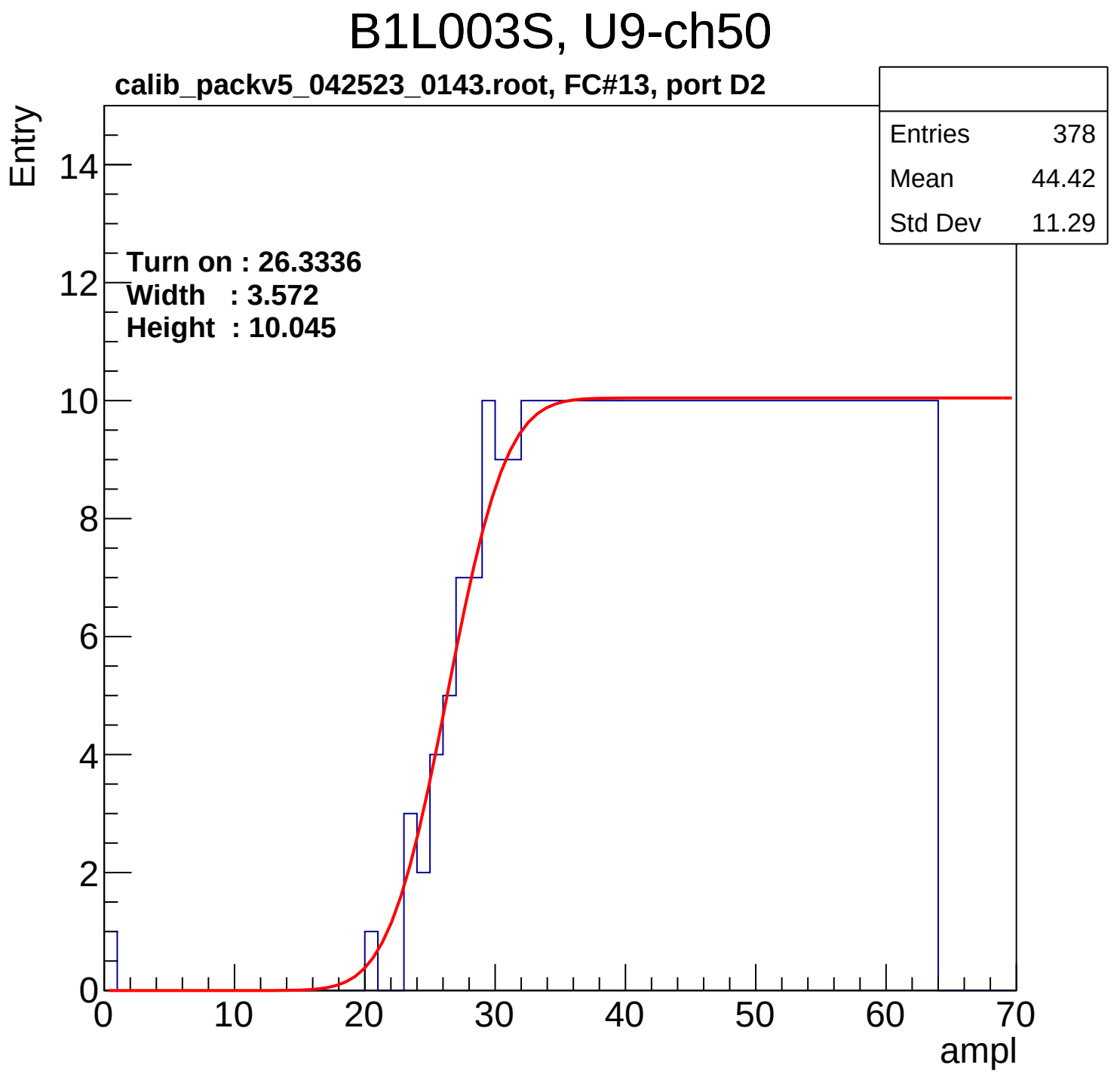

B1L003S, U9-ch45
calib_packv5_042523_0143.root, FC#13, port D2
Entries 350
Mean 45.66
Std Dev 10.99
Turn on : 29.6279
Width : 2.809
Height : 10.063
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

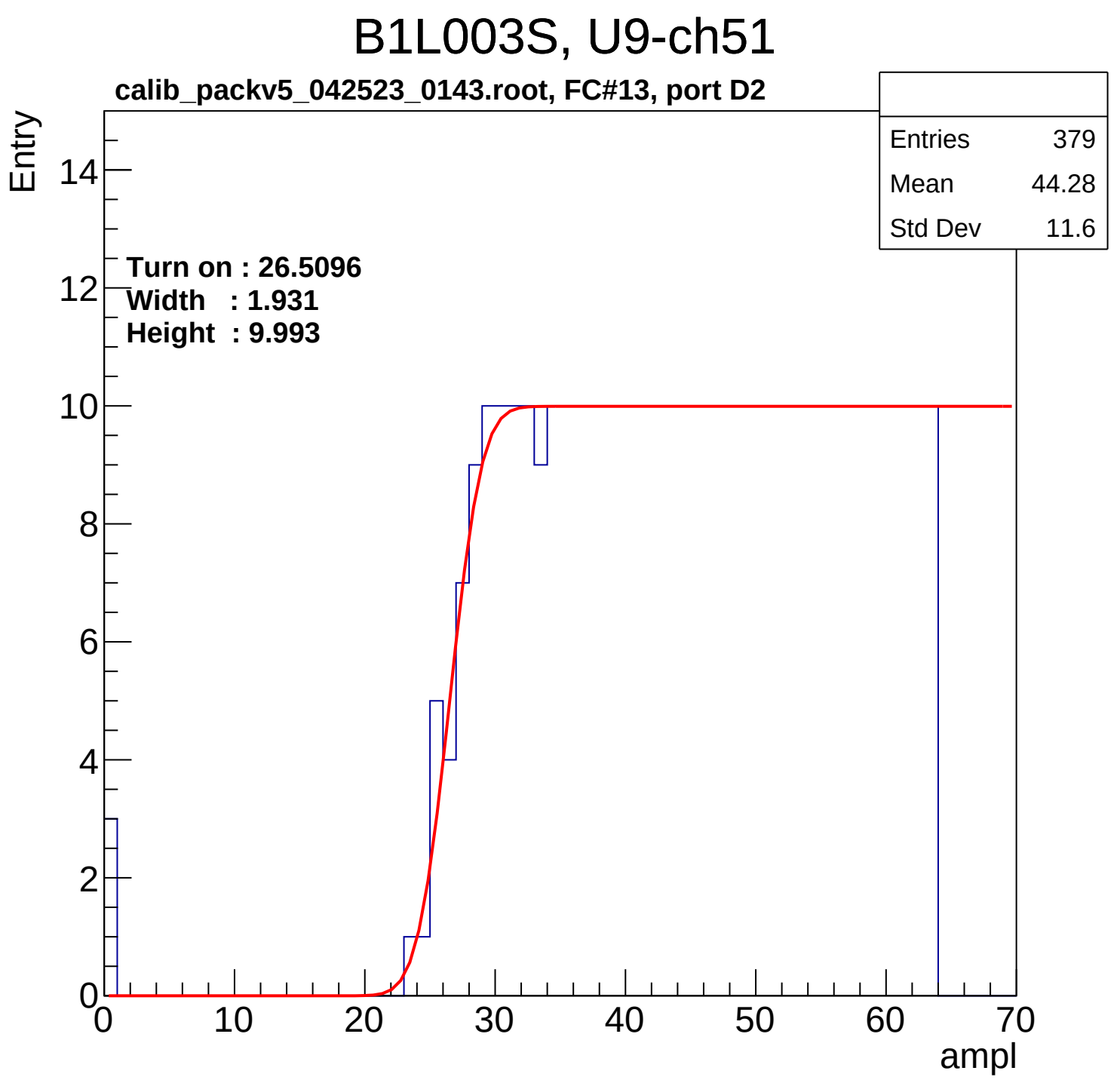

B1L003S, U9-ch46
calib_packv5_042523_0143.root, FC#13, port D2
Entries 358
Mean 45.47
Std Dev 10.65
Turn on : 28.2052
Width : 2.334
Height : 10.036
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

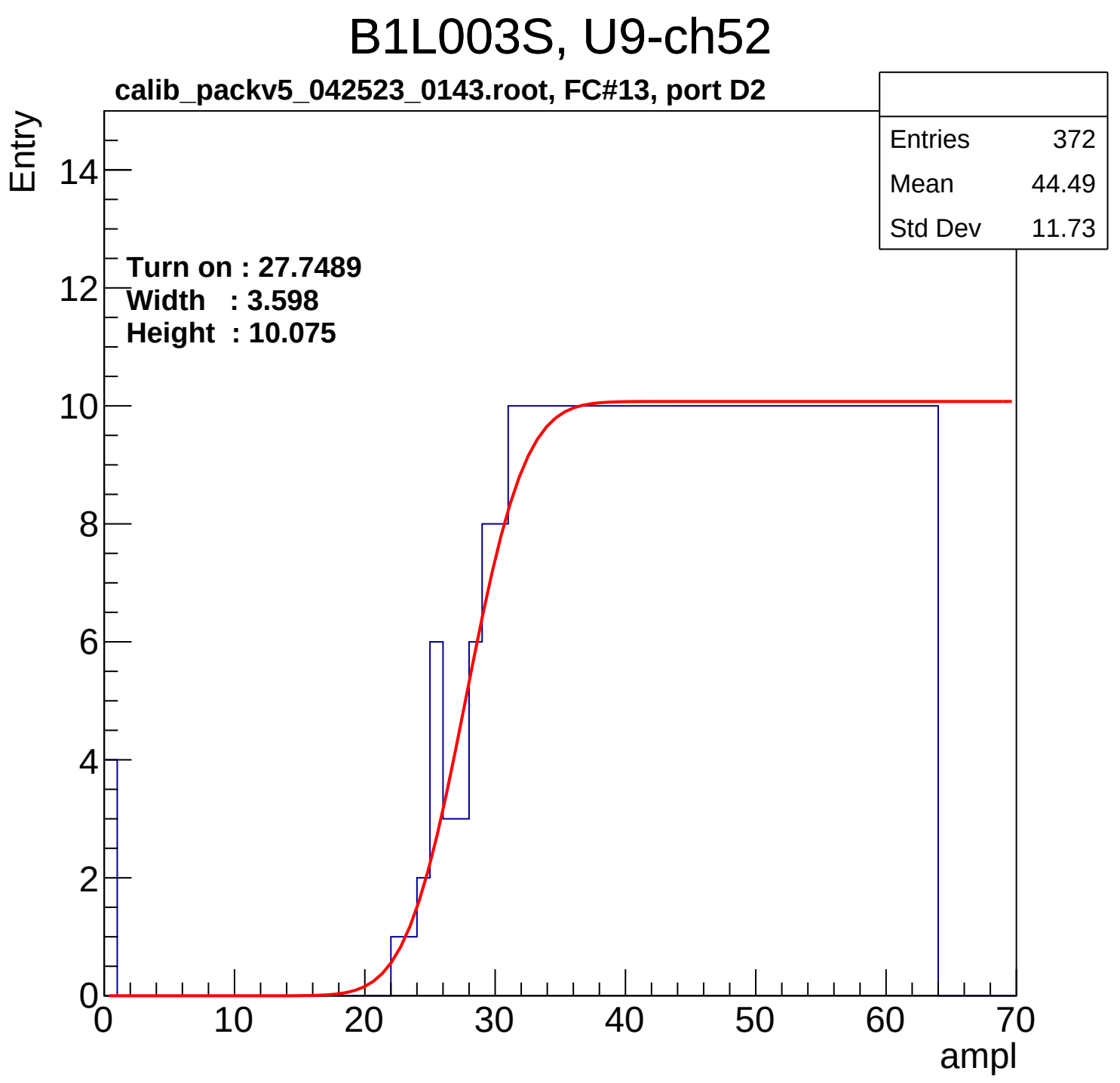

B1L003S, U9-ch47
calib_packv5_042523_0143.root, FC#13, port D2
Entries 375
Mean 44.39
Std Dev 11.65
Turn on : 27.0743
Width : 3.568
Height : 10.017
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

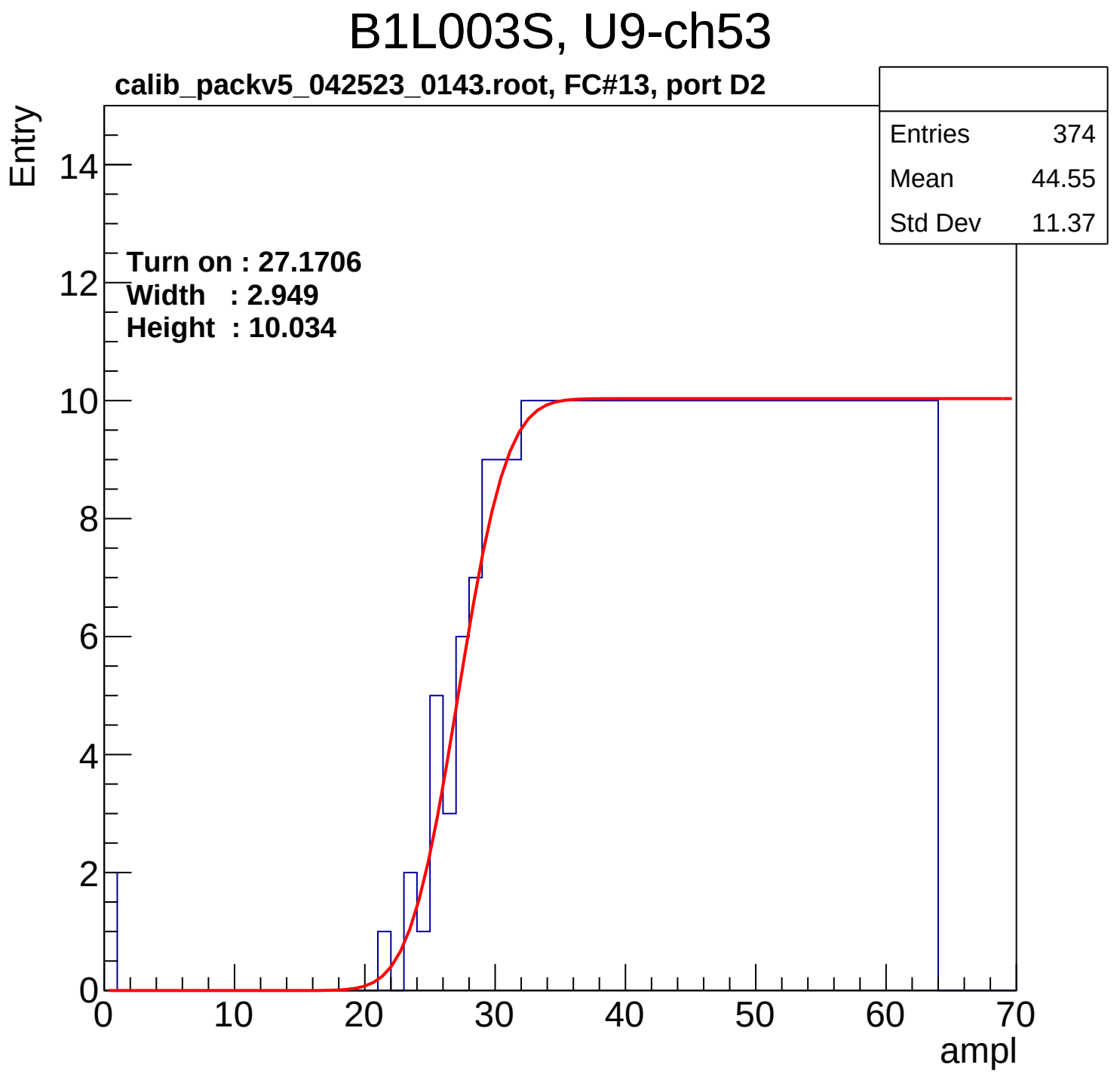

B1L003S, U9-ch48
calib_packv5_042523_0143.root, FC#13, port D2
Entries 377
Mean 44.2
Std Dev 11.99
Turn on : 26.8008
Width : 3.233
Height : 10.029
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

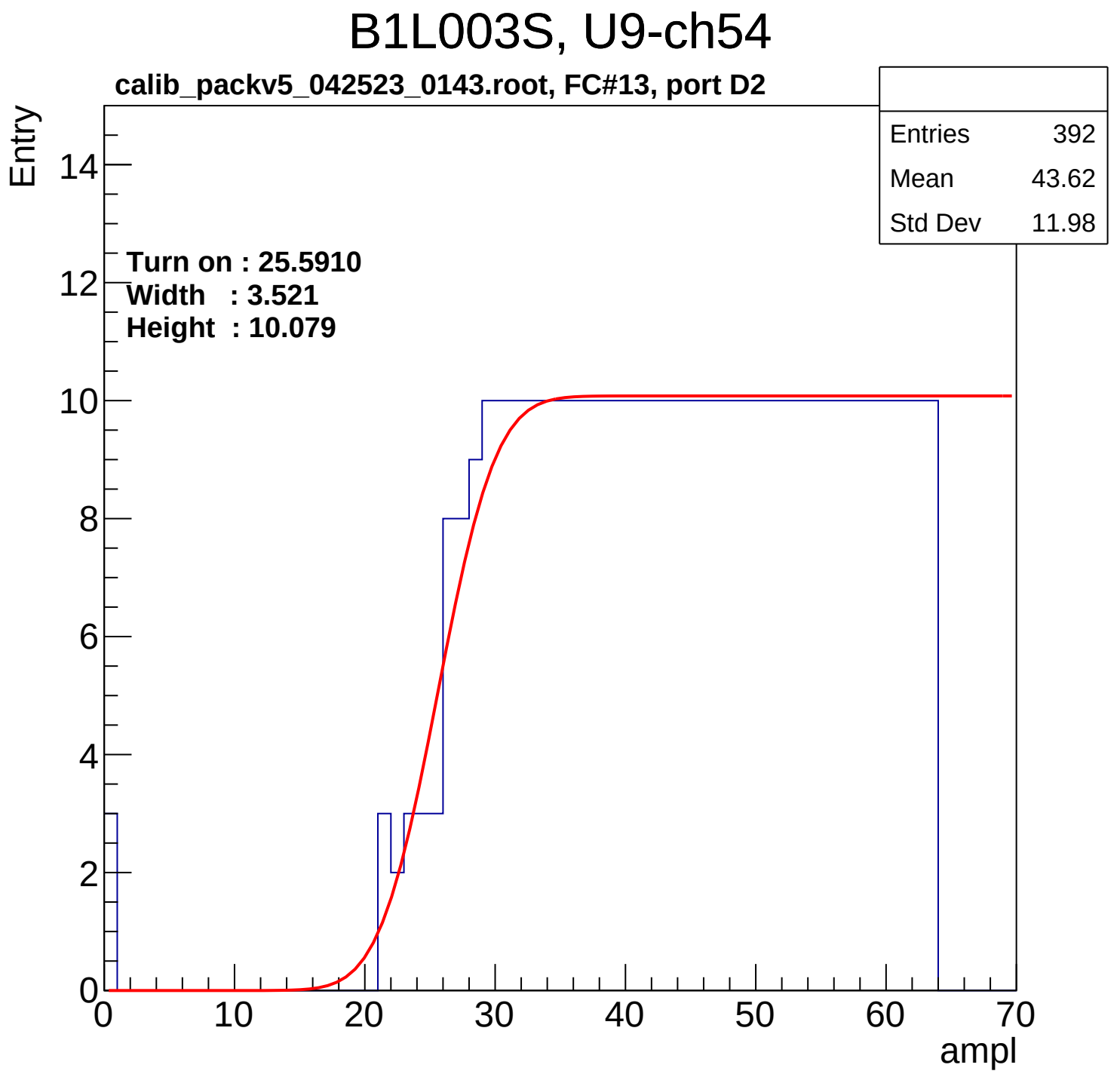

B1L003S, U9-ch49
calib_packv5_042523_0143.root, FC#13, port D2
Entries 368
Mean 44.85
Std Dev 11.21
Turn on : 28.1239
Width : 3.254
Height : 10.075
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

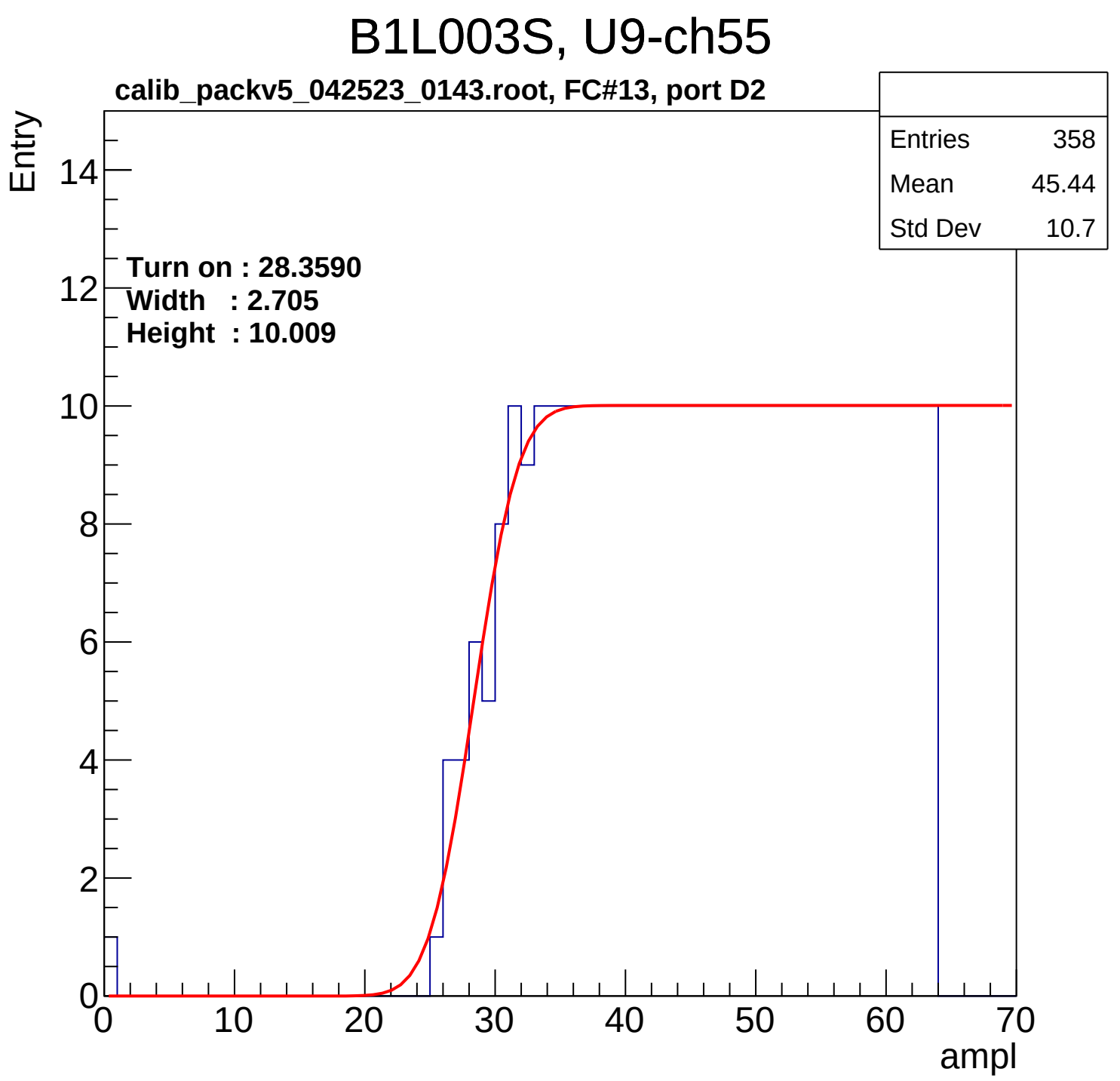

B1L003S, U9-ch50
calib_packv5_042523_0143.root, FC#13, port D2
Entries 378
Mean 44.42
Std Dev 11.29
Turn on : 26.3336
Width : 3.572
Height : 10.045
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

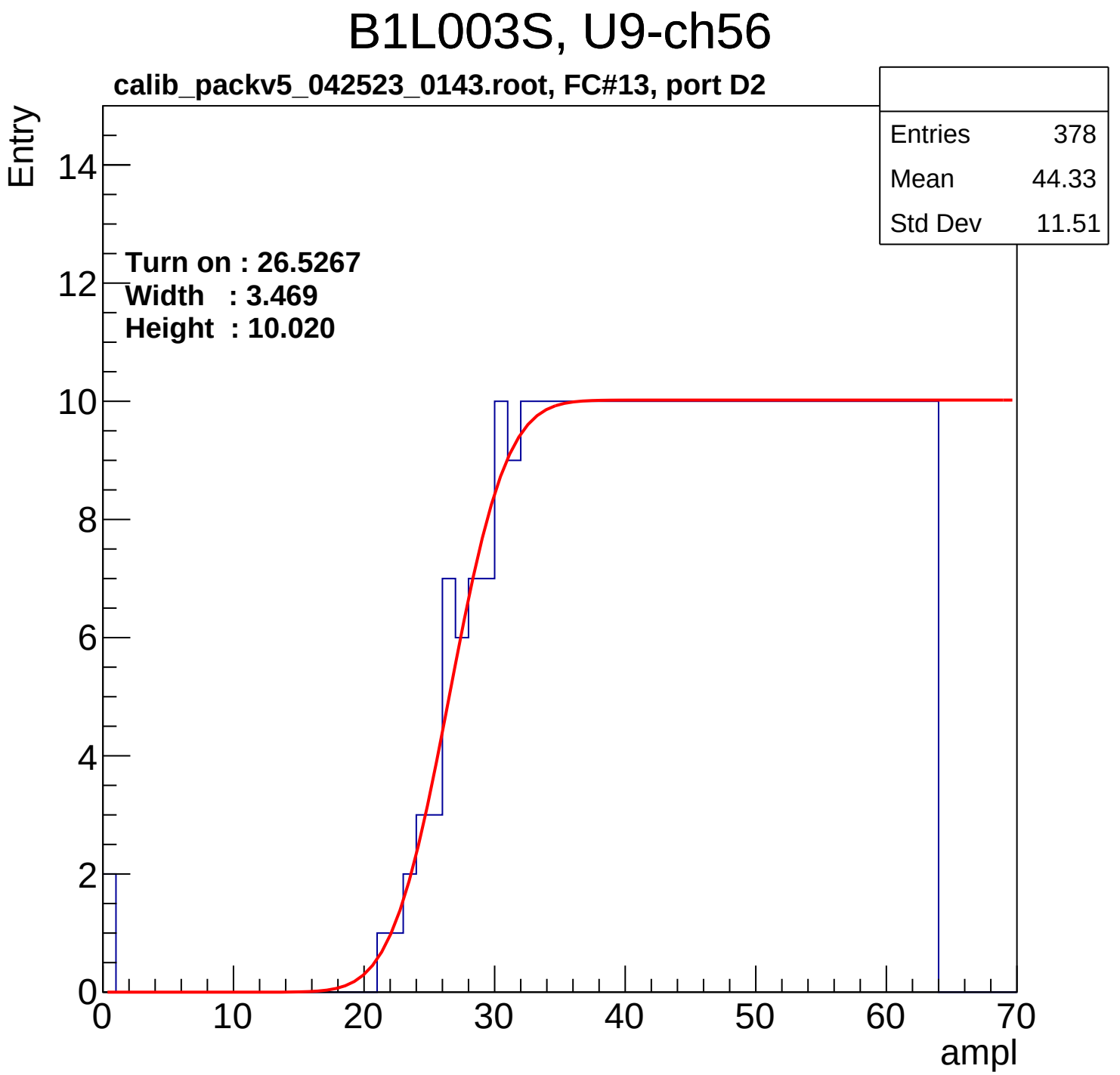

B1L003S, U9-ch51
calib_packv5_042523_0143.root, FC#13, port D2
Entries 379
Mean 44.28
Std Dev 11.6
Turn on : 26.5096
Width : 1.931
Height : 9.993
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

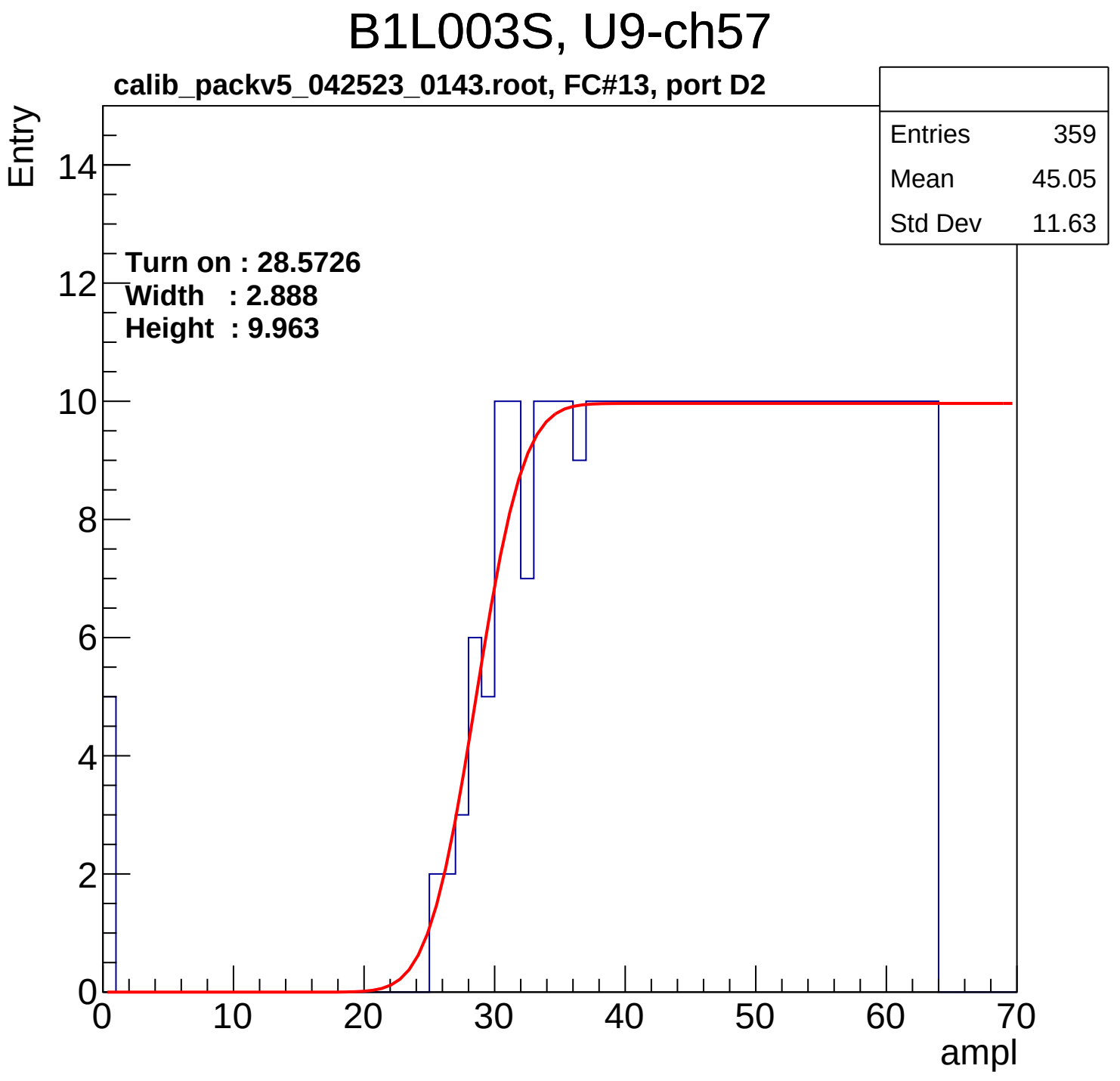

B1L003S, U9-ch52
calib_packv5_042523_0143.root, FC#13, port D2
Entries 372
Mean 44.49
Std Dev 11.73
Turn on : 27.7489
Width : 3.598
Height : 10.075
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

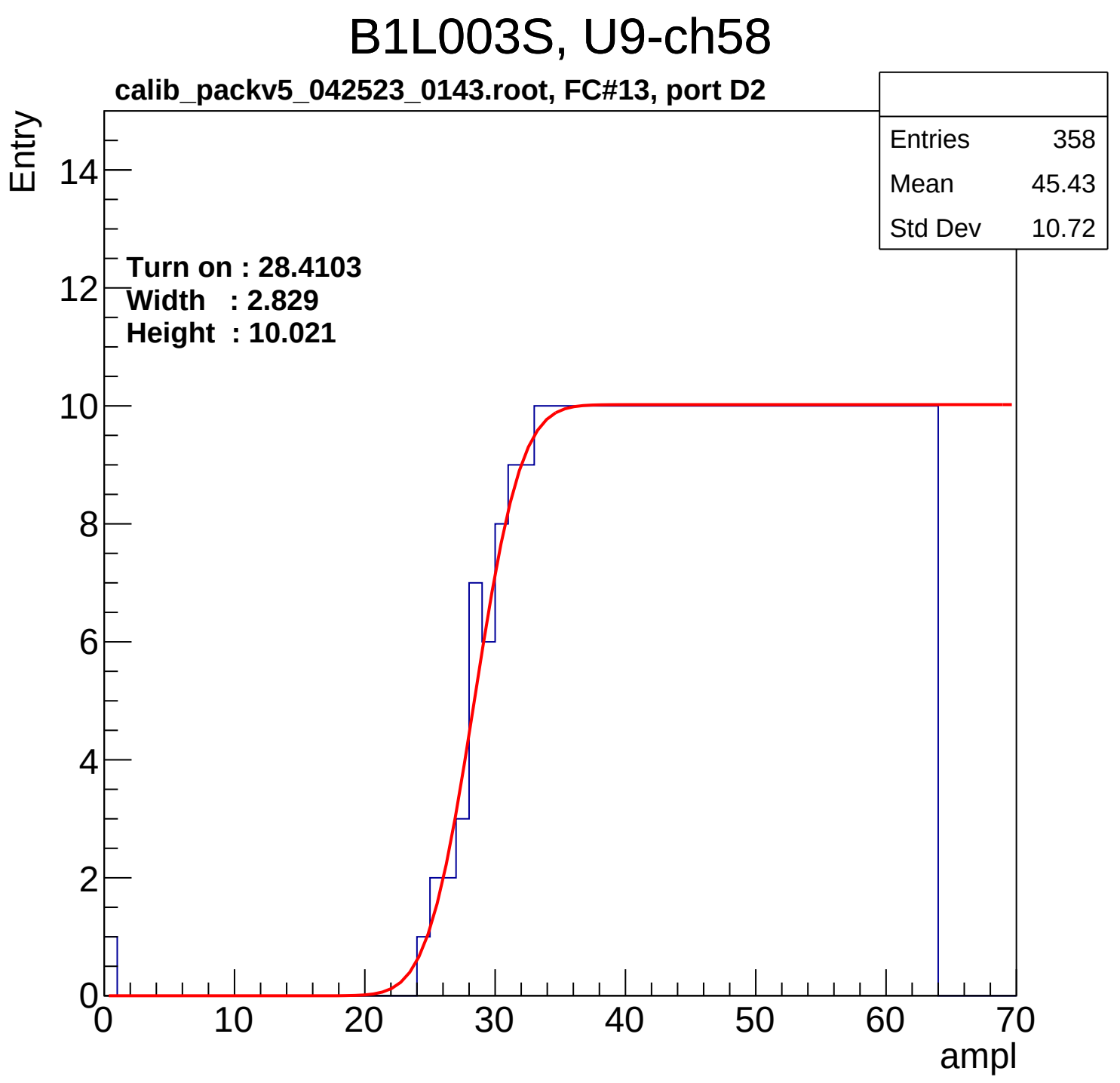

B1L003S, U9-ch53
calib_packv5_042523_0143.root, FC#13, port D2
Entries 374
Mean 44.55
Std Dev 11.37
Turn on : 27.1706
Width : 2.949
Height : 10.034
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

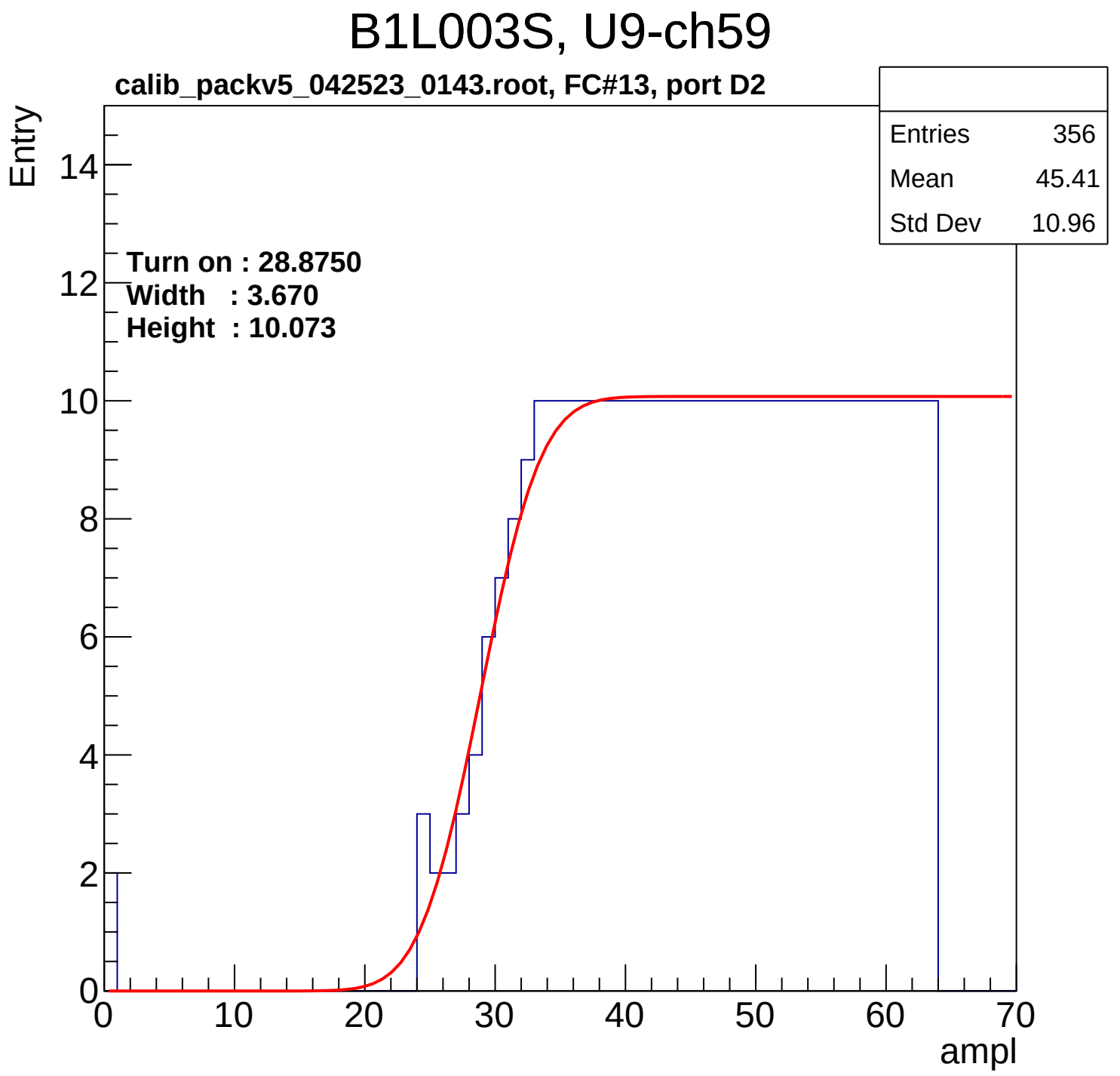

B1L003S, U9-ch54
calib_packv5_042523_0143.root, FC#13, port D2
Entries 392
Mean 43.62
Std Dev 11.98
Turn on : 25.5910
Width : 3.521
Height : 10.079
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

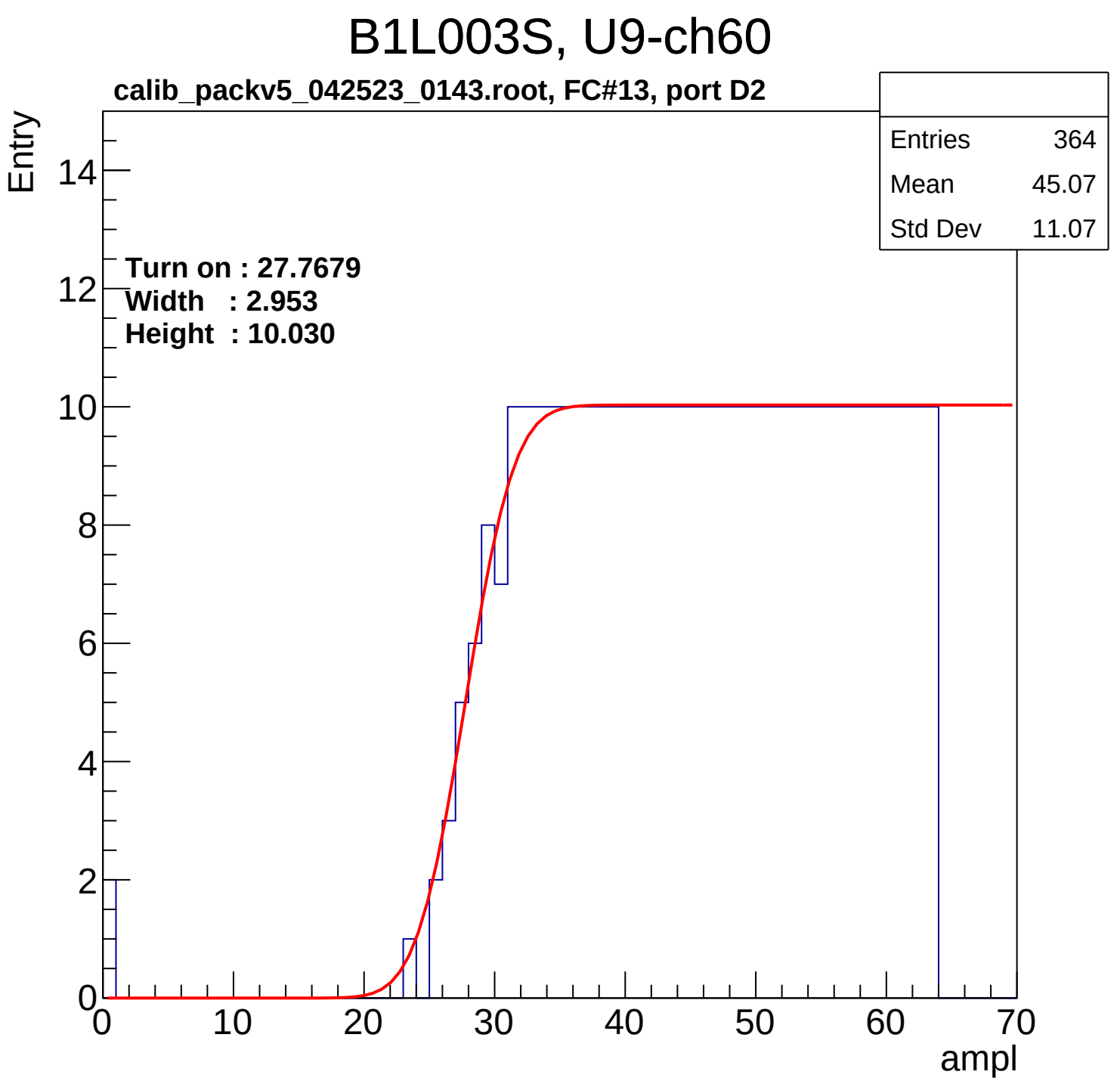

B1L003S, U9-ch55
calib_packv5_042523_0143.root, FC#13, port D2
Entries 358
Mean 45.44
Std Dev 10.7
Turn on : 28.3590
Width : 2.705
Height : 10.009
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

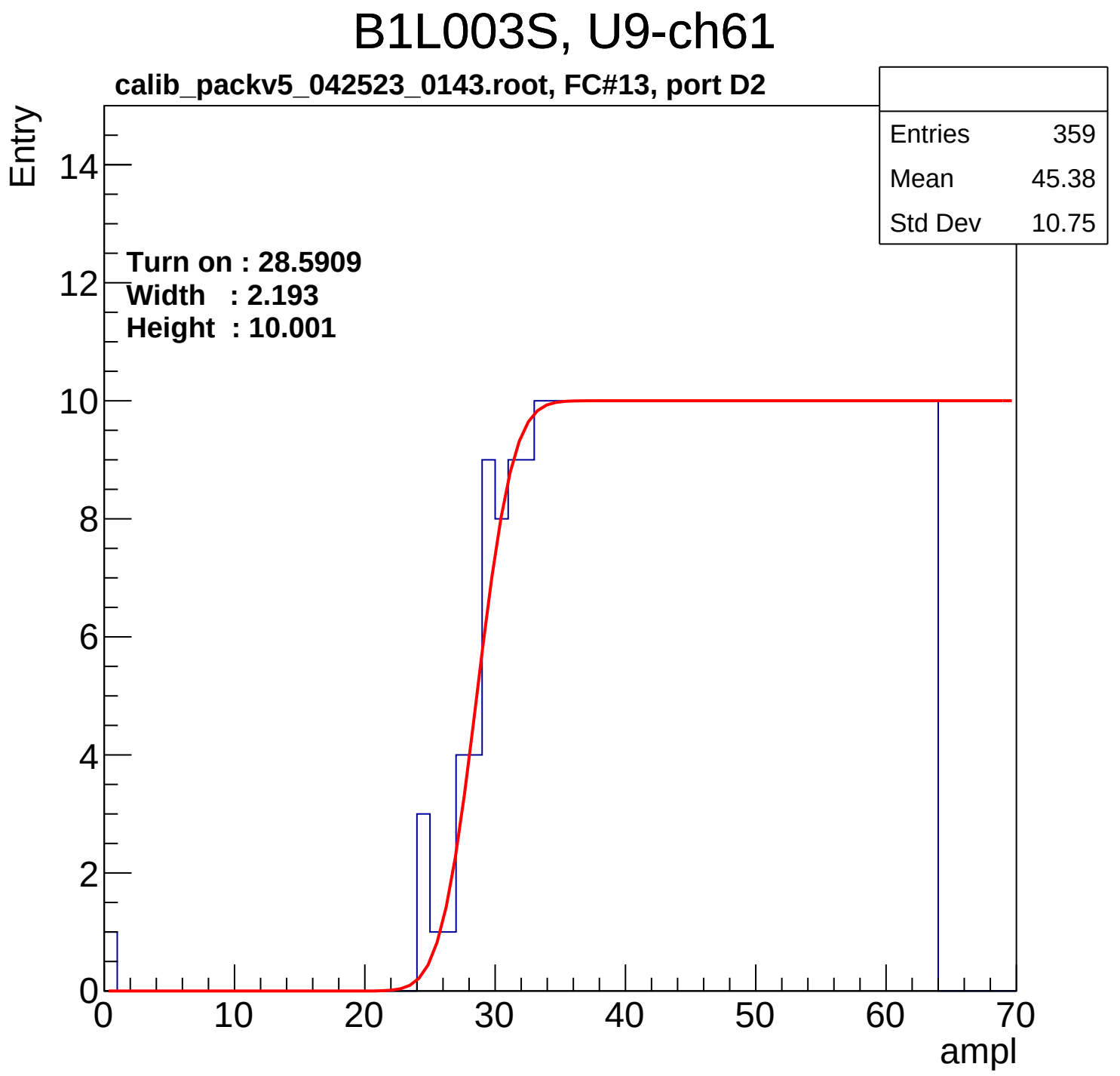

B1L003S, U9-ch56
calib_packv5_042523_0143.root, FC#13, port D2
Entries 378
Mean 44.33
Std Dev 11.51
Turn on : 26.5267
Width : 3.469
Height : 10.020
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

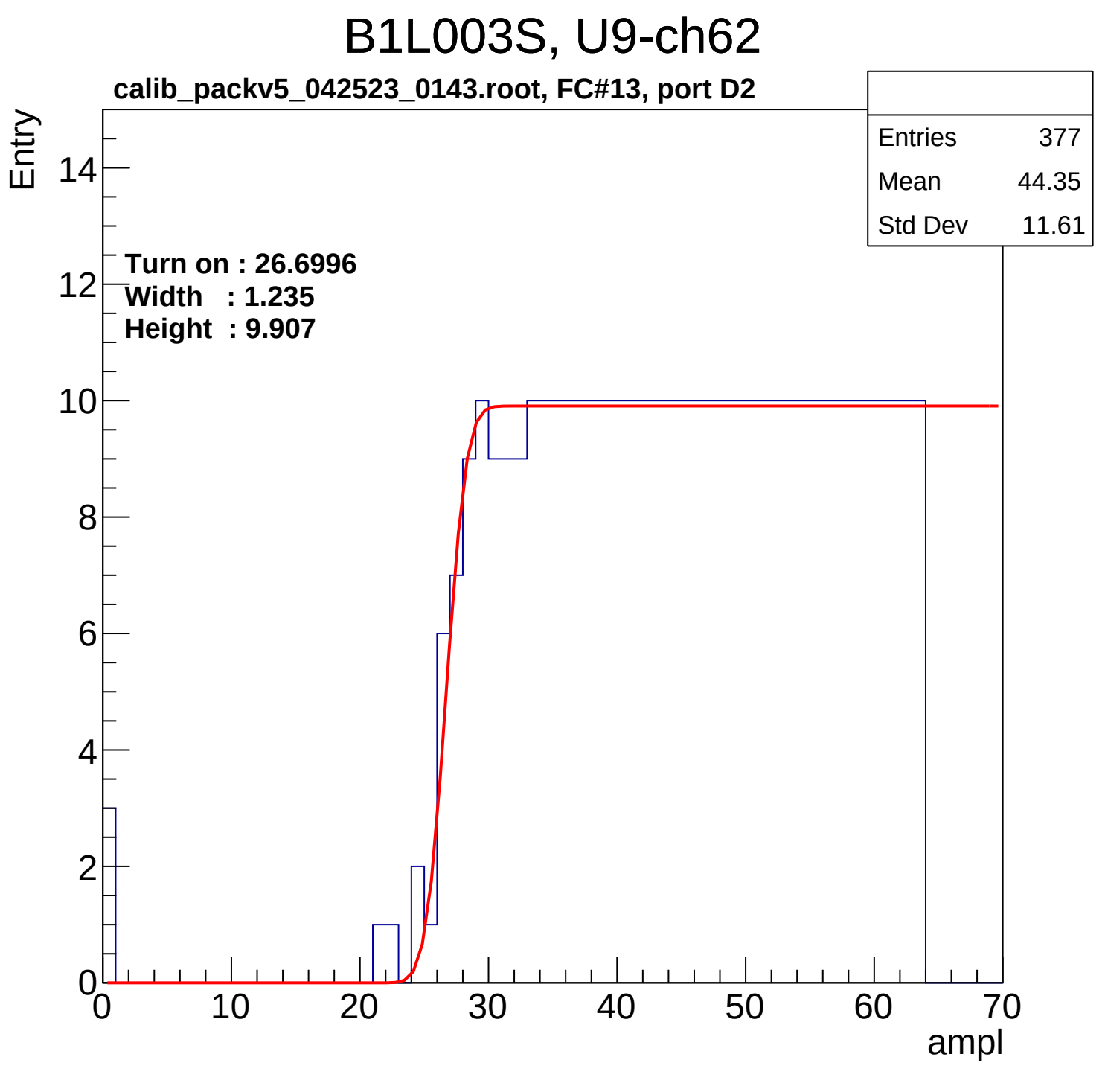

B1L003S, U9-ch57
calib_packv5_042523_0143.root, FC#13, port D2
Entries 359
Mean 45.05
Std Dev 11.63
Turn on : 28.5726
Width : 2.888
Height : 9.963
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

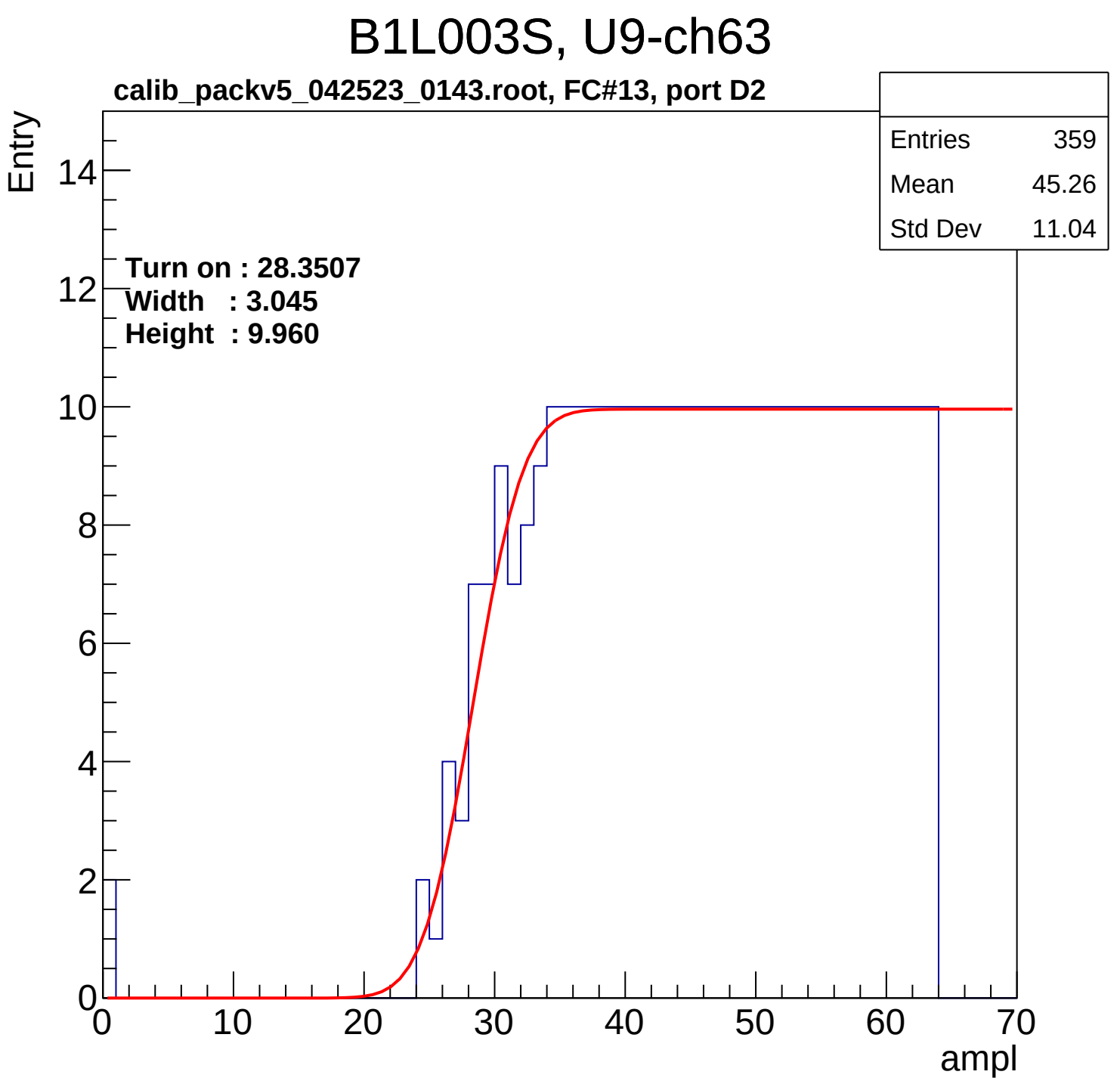

B1L003S, U9-ch58
calib_packv5_042523_0143.root, FC#13, port D2
Entries 358
Mean 45.43
Std Dev 10.72
Turn on : 28.4103
Width : 2.829
Height : 10.021
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

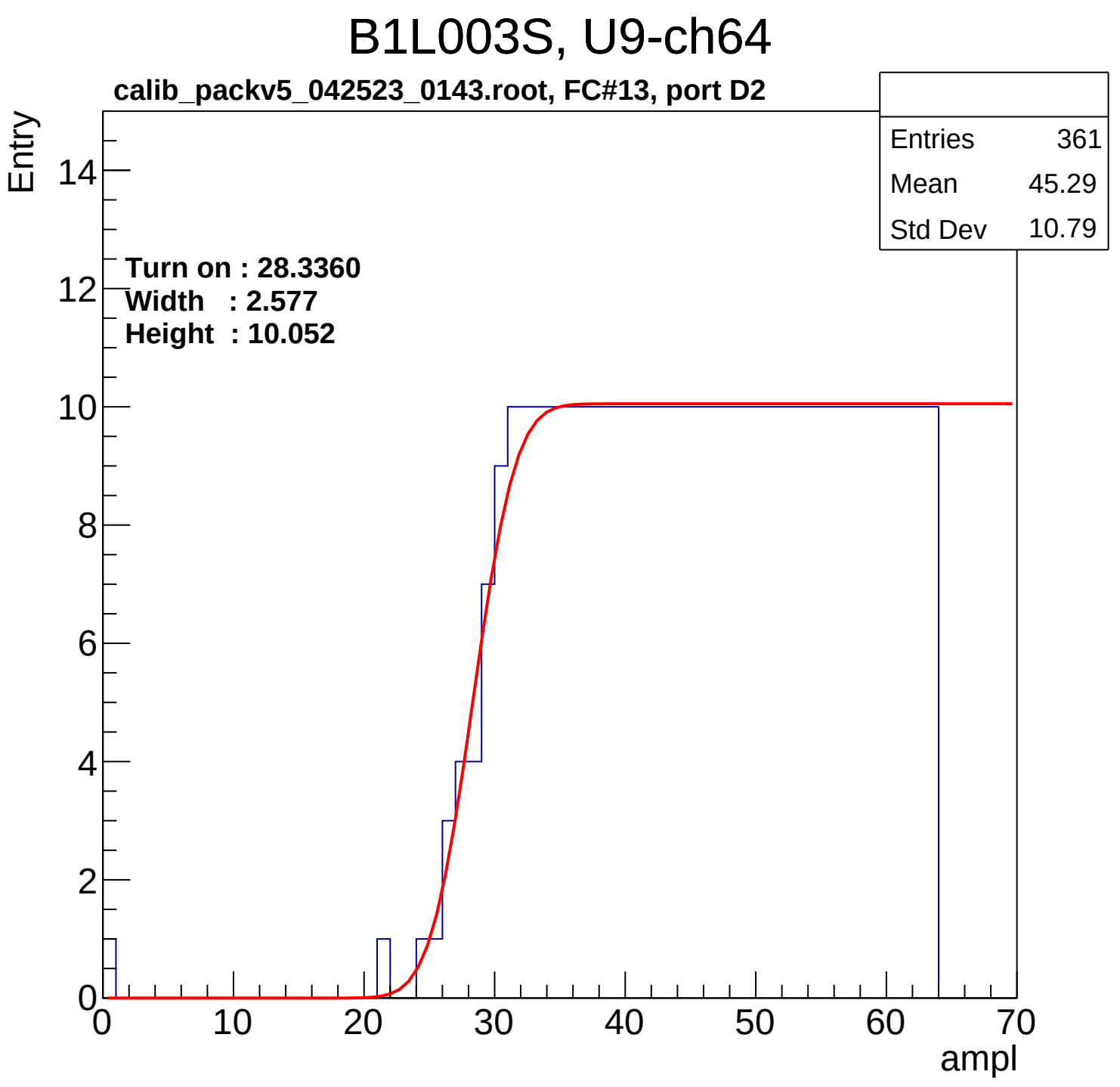

B1L003S, U9-ch59
calib_packv5_042523_0143.root, FC#13, port D2
Entries 356
Mean 45.41
Std Dev 10.96
Turn on : 28.8750
Width : 3.670
Height : 10.073
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

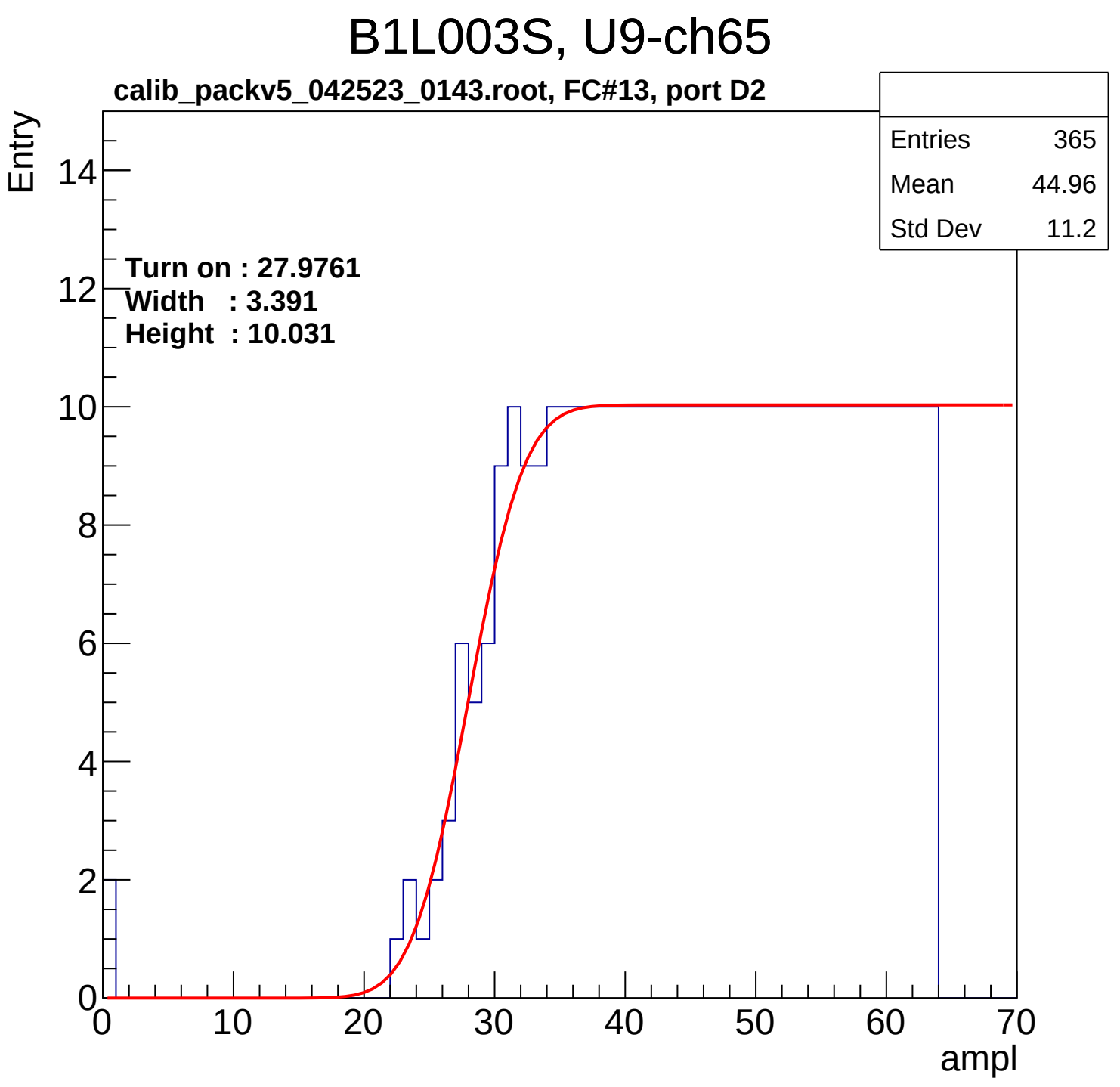

B1L003S, U9-ch60
calib_packv5_042523_0143.root, FC#13, port D2
Entries 364
Mean 45.07
Std Dev 11.07
Turn on : 27.7679
Width : 2.953
Height : 10.030
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

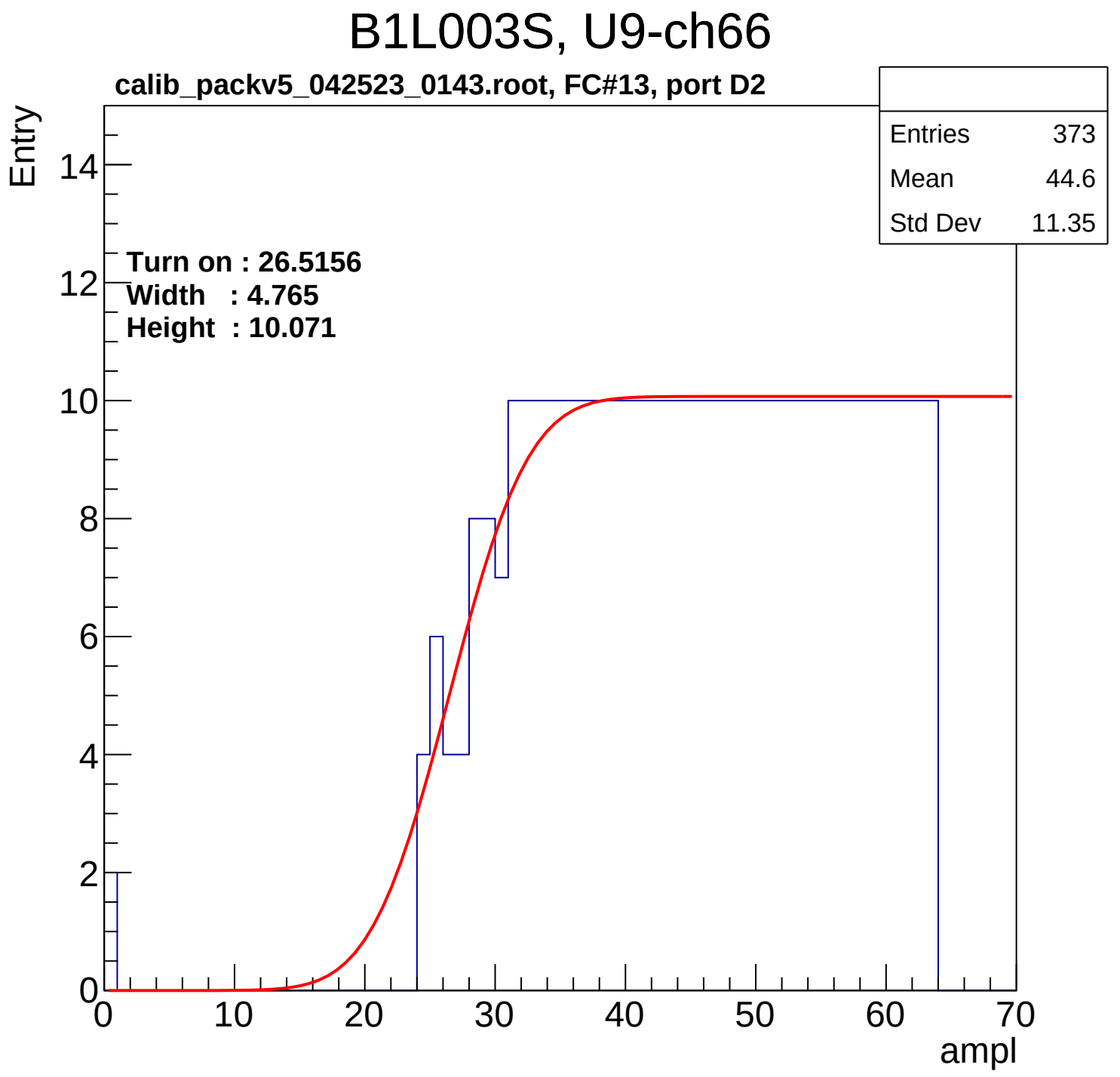

B1L003S, U9-ch61
calib_packv5_042523_0143.root, FC#13, port D2
Entries 359
Mean 45.38
Std Dev 10.75
Turn on : 28.5909
Width : 2.193
Height : 10.001
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

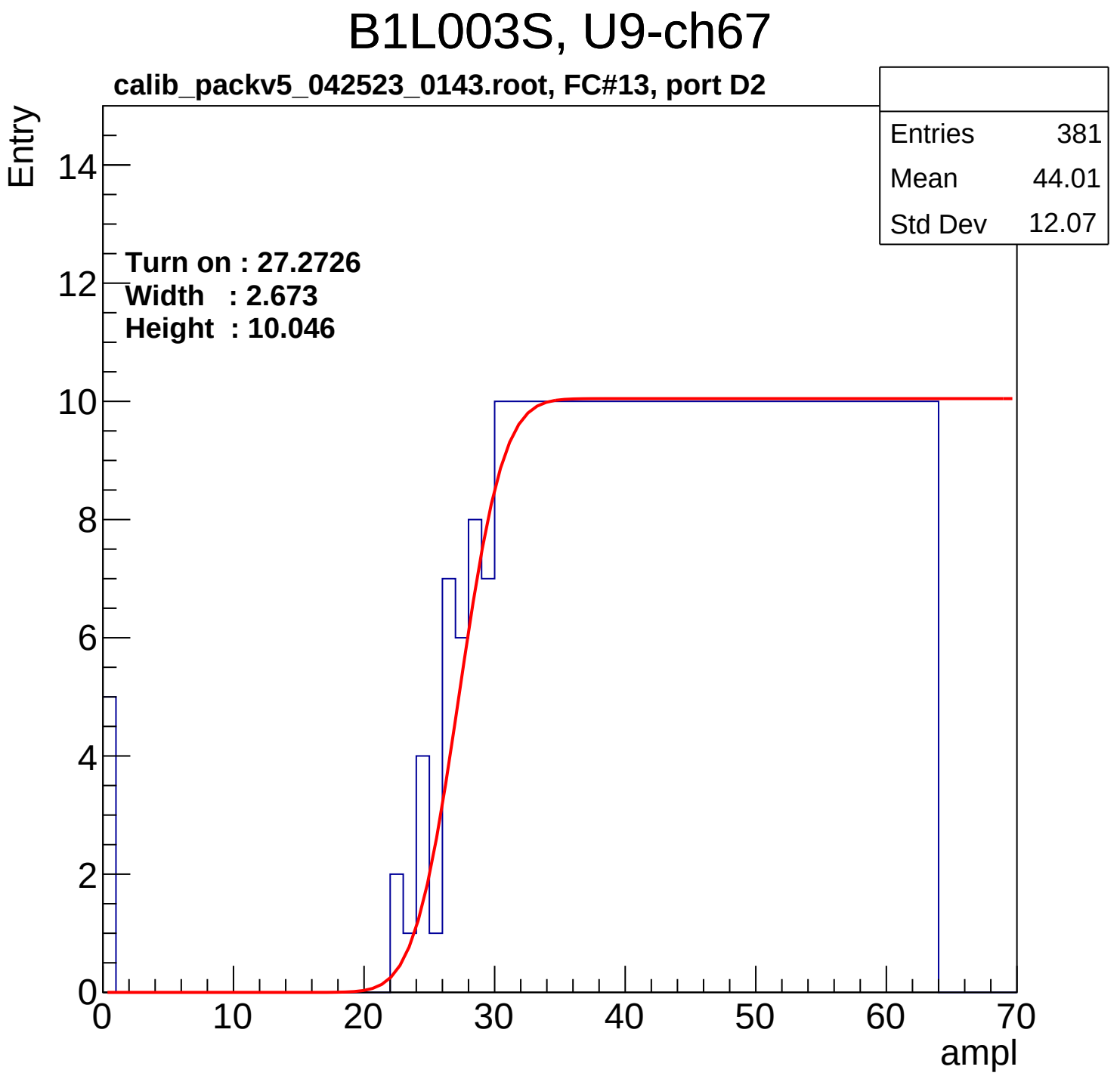

B1L003S, U9-ch62
calib_packv5_042523_0143.root, FC#13, port D2
Entries 377
Mean 44.35
Std Dev 11.61
Turn on : 26.6996
Width : 1.235
Height : 9.907
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

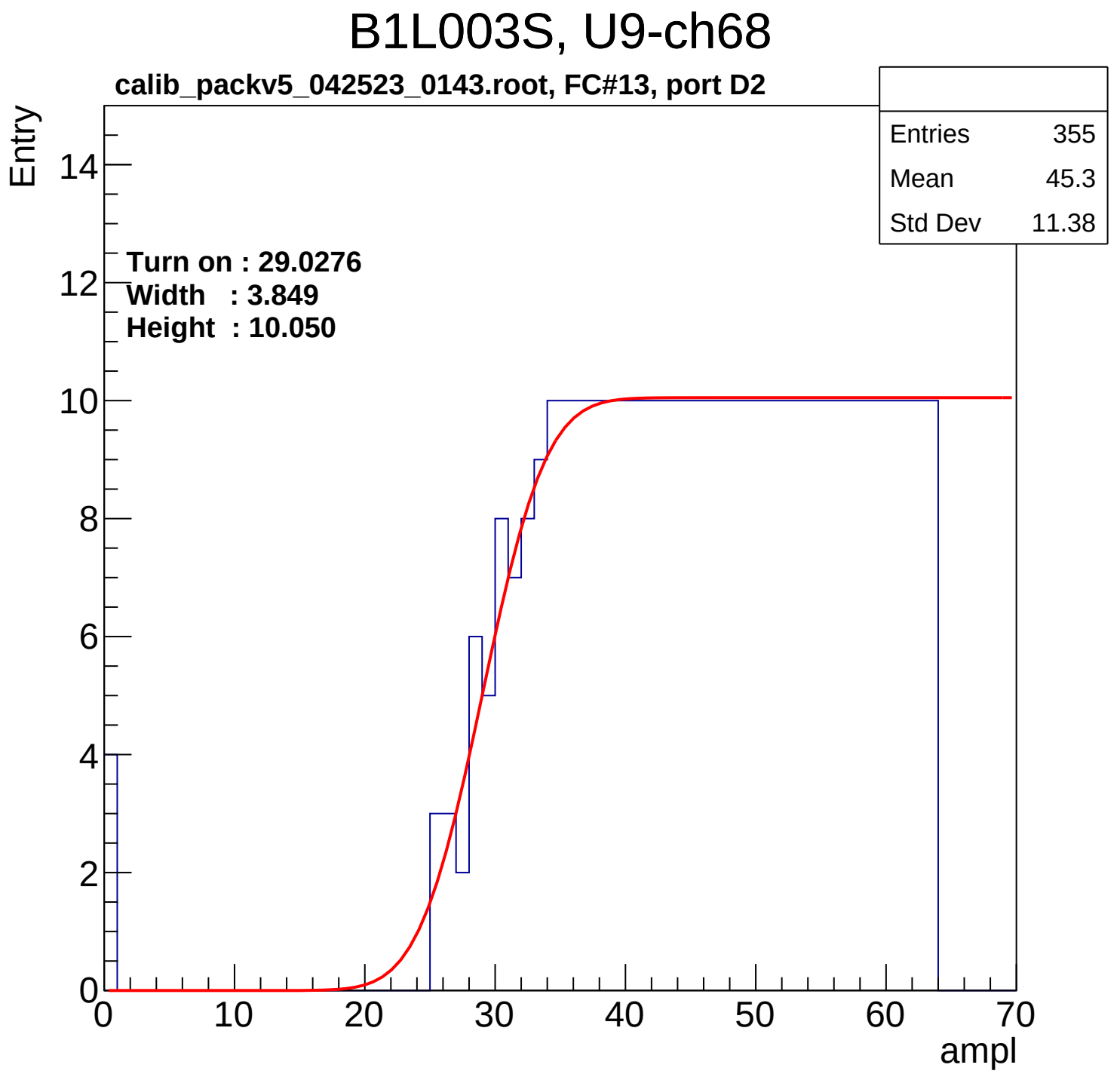

B1L003S, U9-ch63
calib_packv5_042523_0143.root, FC#13, port D2
Entries 359
Mean 45.26
Std Dev 11.04
Turn on : 28.3507
Width : 3.045
Height : 9.960
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

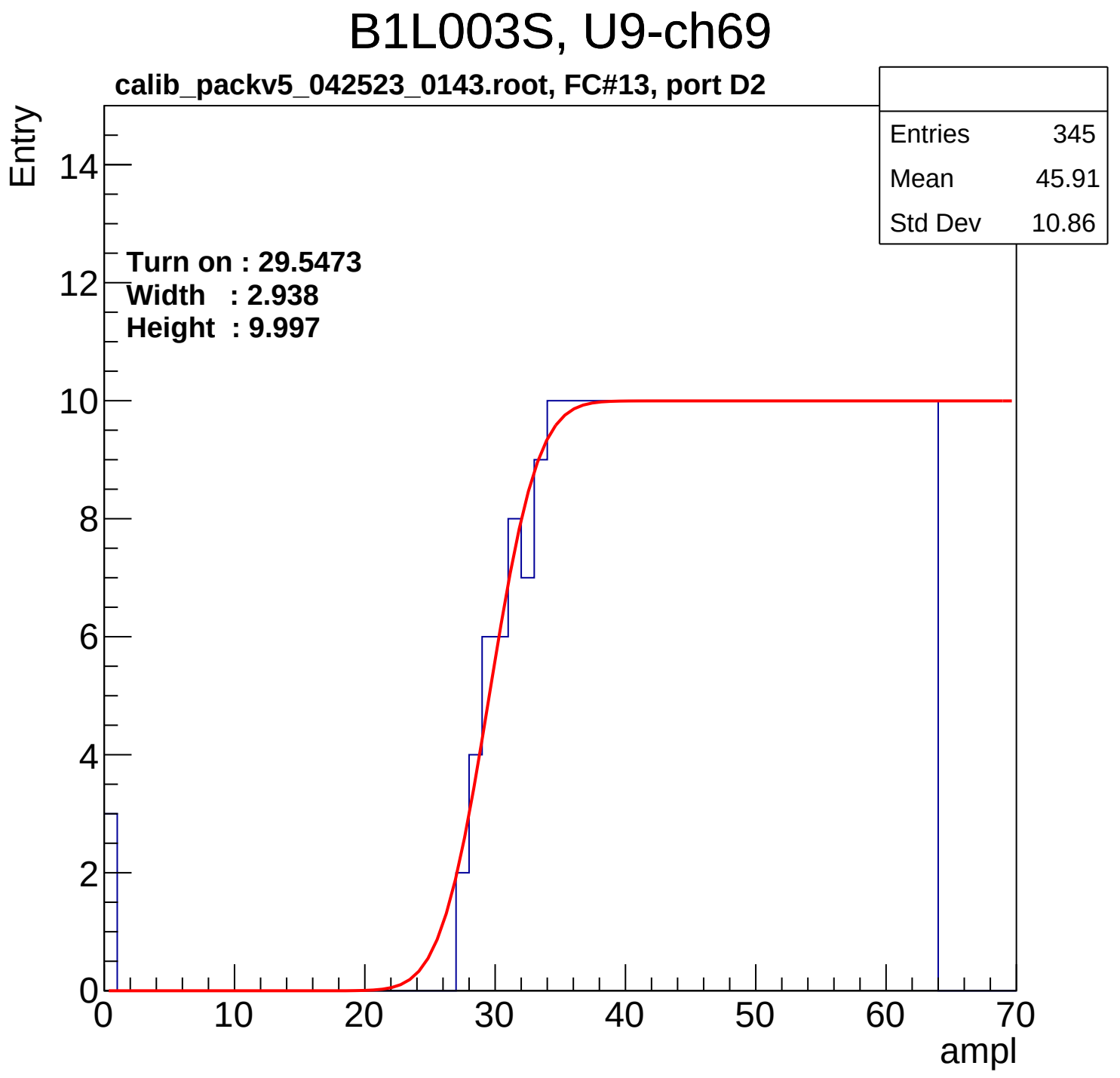

B1L003S, U9-ch64
calib_packv5_042523_0143.root, FC#13, port D2
Entries 361
Mean 45.29
Std Dev 10.79
Turn on : 28.3360
Width : 2.577
Height : 10.052
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

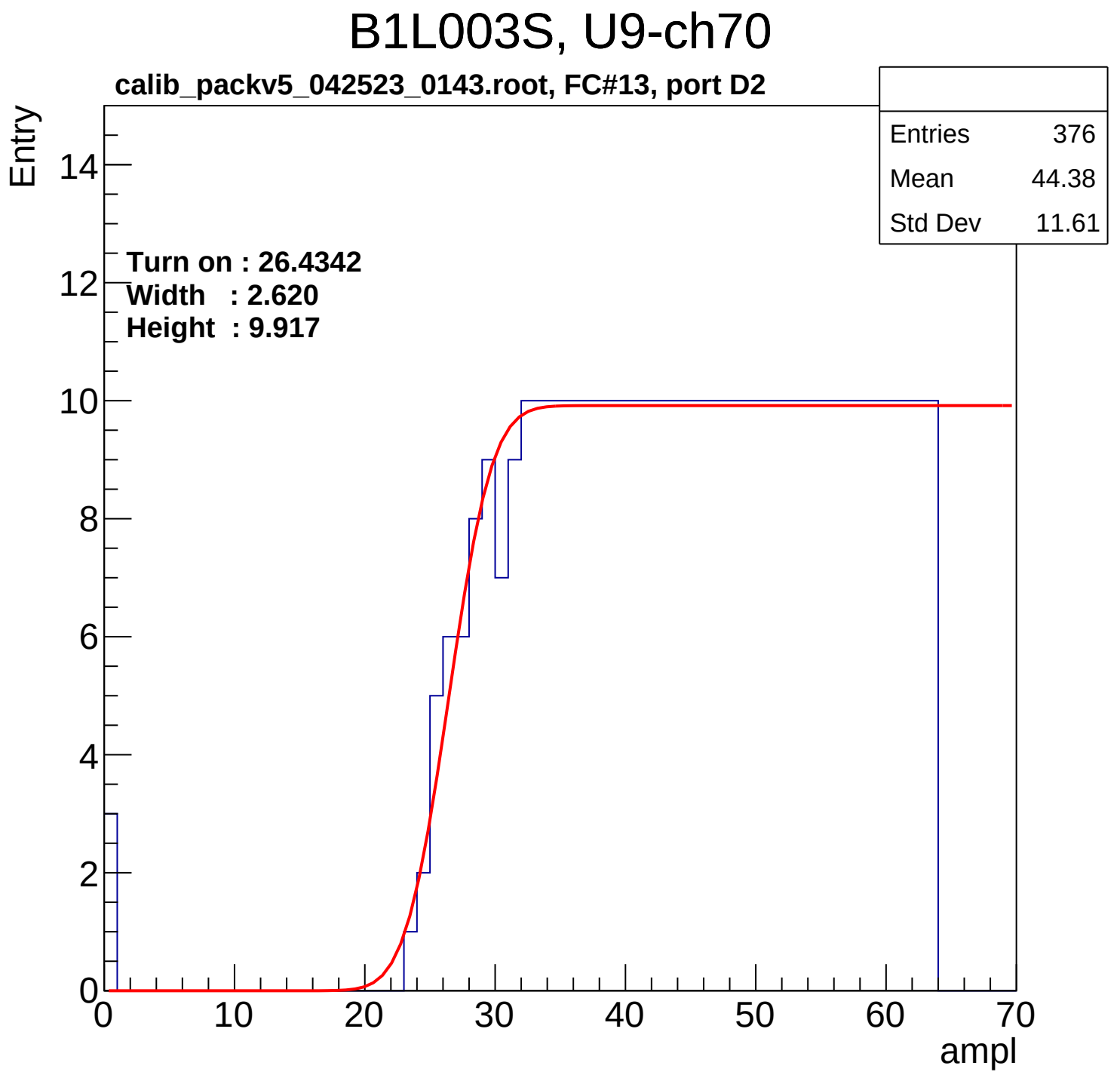

B1L003S, U9-ch65
calib_packv5_042523_0143.root, FC#13, port D2
Entries 365
Mean 44.96
Std Dev 11.2
Turn on : 27.9761
Width : 3.391
Height : 10.031
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

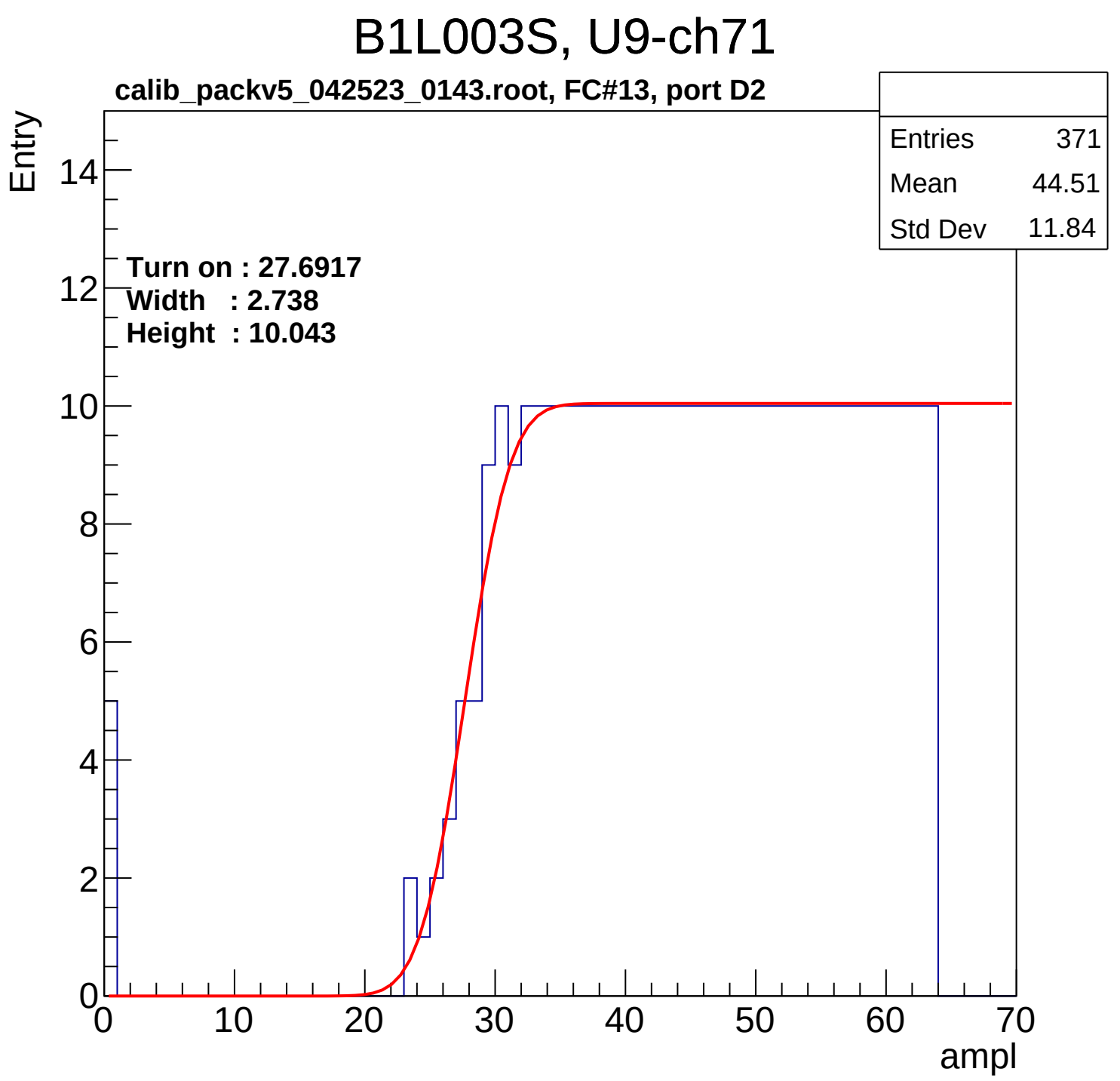

B1L003S, U9-ch66
calib_packv5_042523_0143.root, FC#13, port D2
Entries 373
Mean 44.6
Std Dev 11.35
Turn on : 26.5156
Width : 4.765
Height : 10.071
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

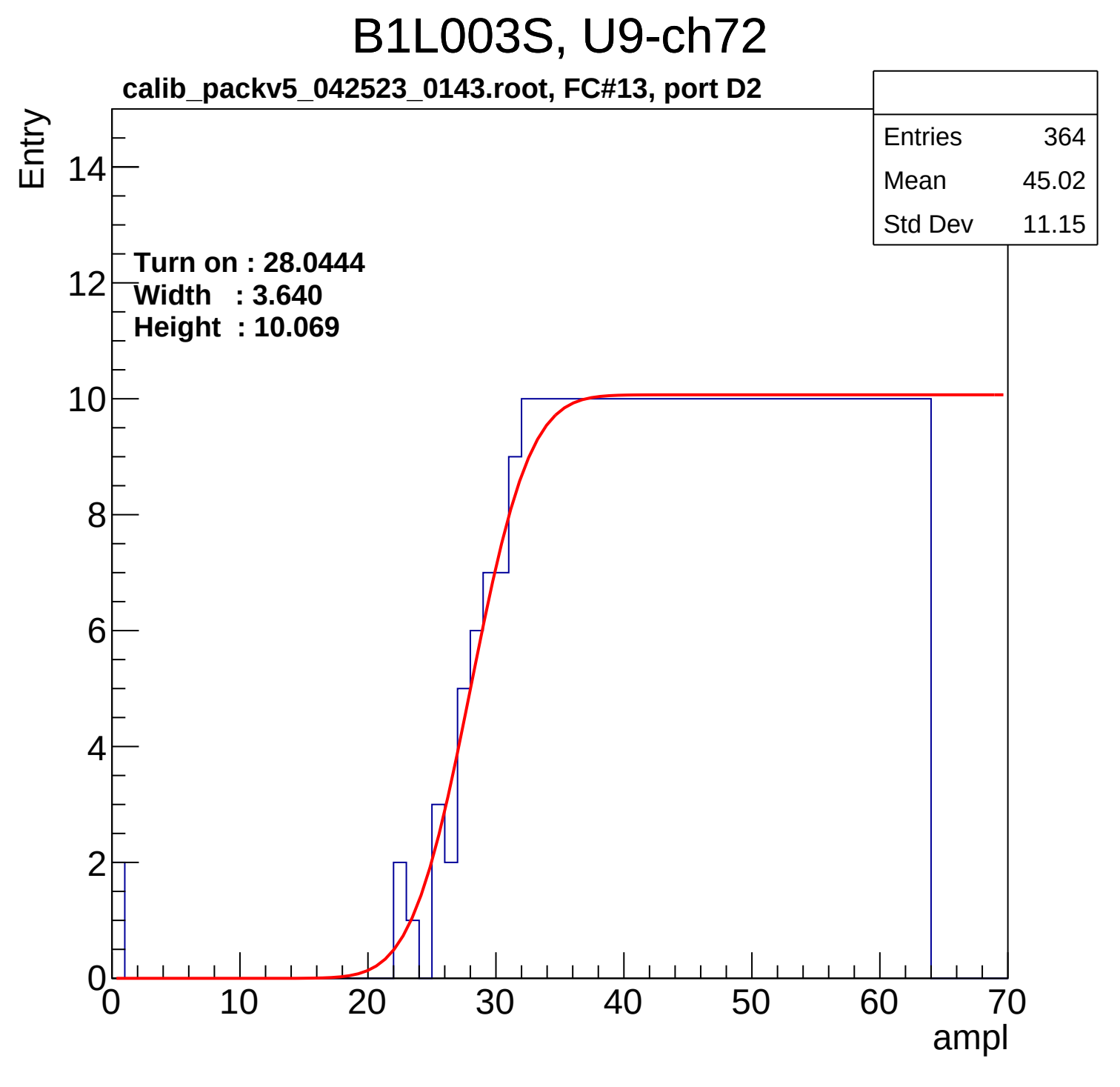

B1L003S, U9-ch67
calib_packv5_042523_0143.root, FC#13, port D2
Entries 381
Mean 44.01
Std Dev 12.07
Turn on : 27.2726
Width : 2.673
Height : 10.046
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

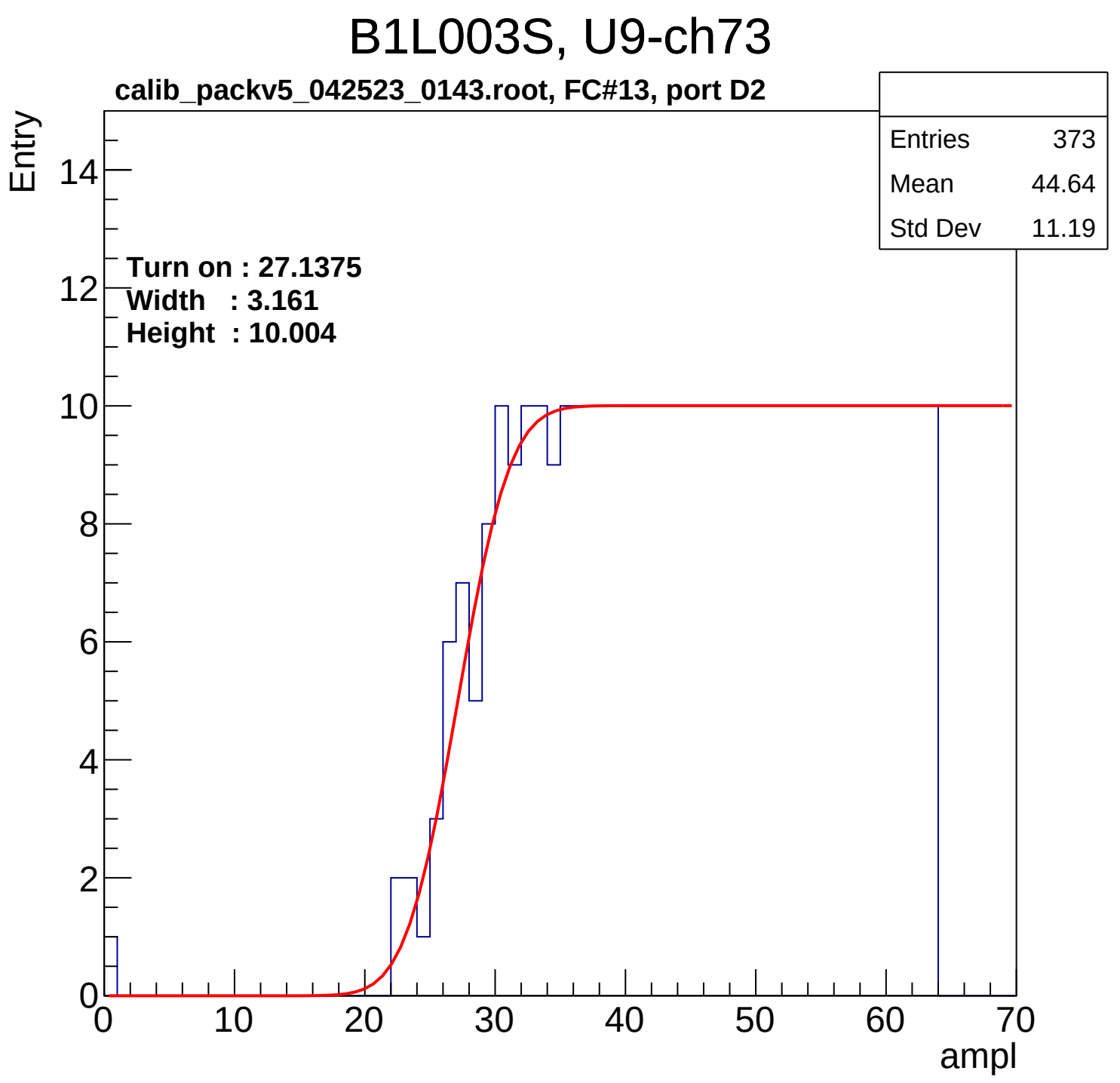

B1L003S, U9-ch68
calib_packv5_042523_0143.root, FC#13, port D2
Entries 355
Mean 45.3
Std Dev 11.38
Turn on : 29.0276
Width : 3.849
Height : 10.050
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

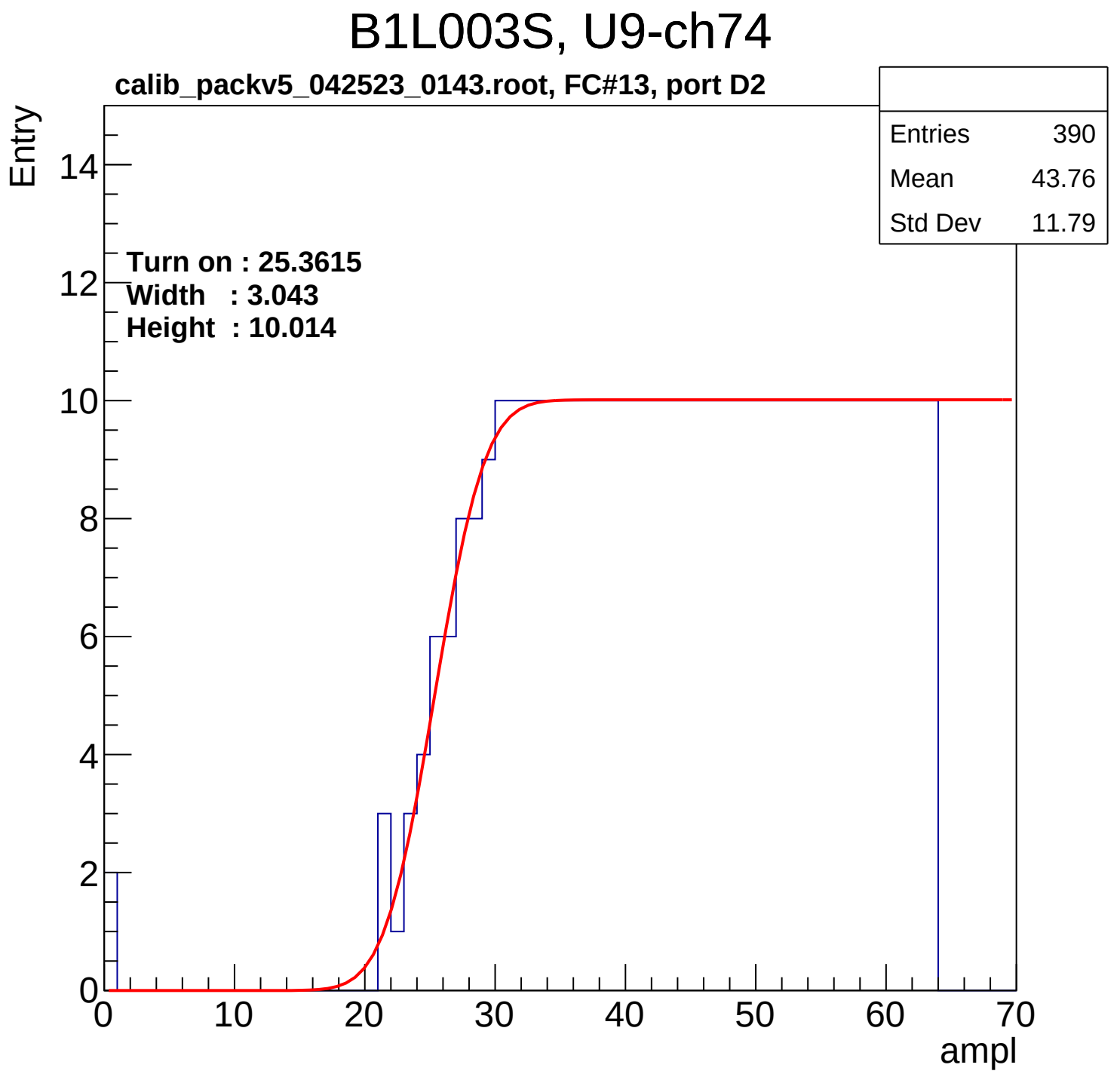

B1L003S, U9-ch69
calib_packv5_042523_0143.root, FC#13, port D2
Entries 345
Mean 45.91
Std Dev 10.86
Turn on : 29.5473
Width : 2.938
Height : 9.997
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

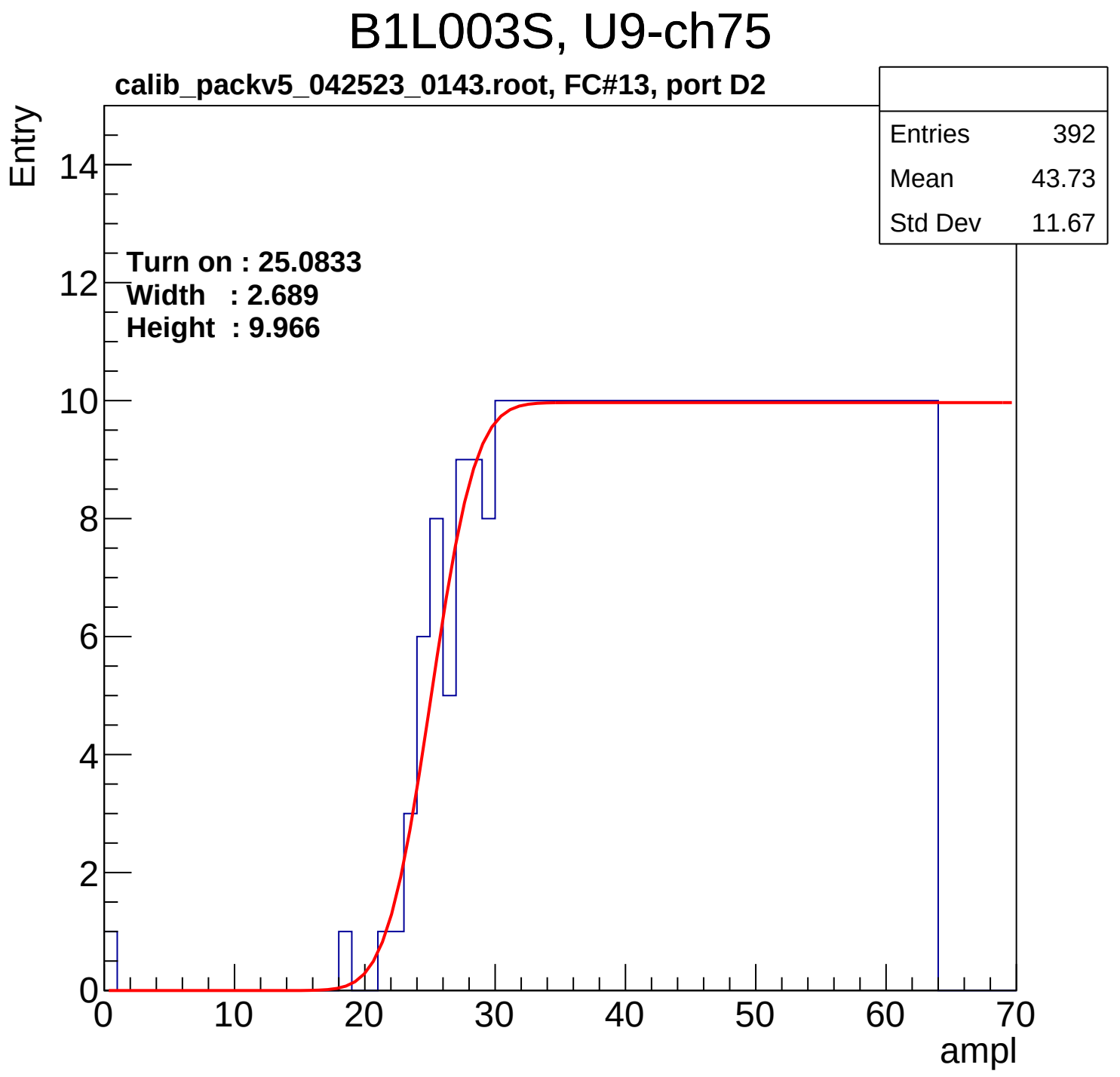

B1L003S, U9-ch70
calib_packv5_042523_0143.root, FC#13, port D2
Entries 376
Mean 44.38
Std Dev 11.61
Turn on : 26.4342
Width : 2.620
Height : 9.917
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

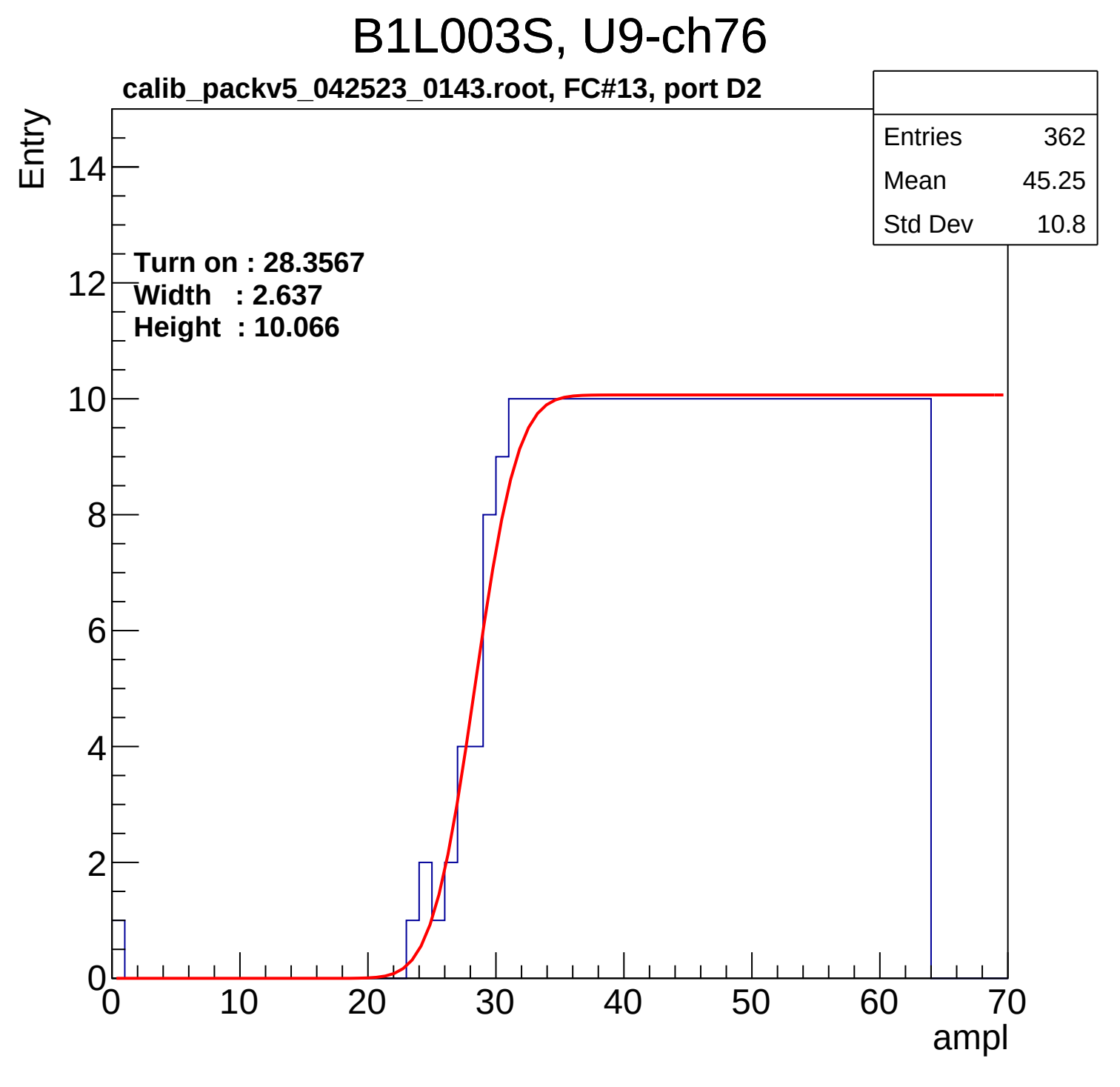

B1L003S, U9-ch71
calib_packv5_042523_0143.root, FC#13, port D2
Entries 371
Mean 44.51
Std Dev 11.84
Turn on : 27.6917
Width : 2.738
Height : 10.043
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

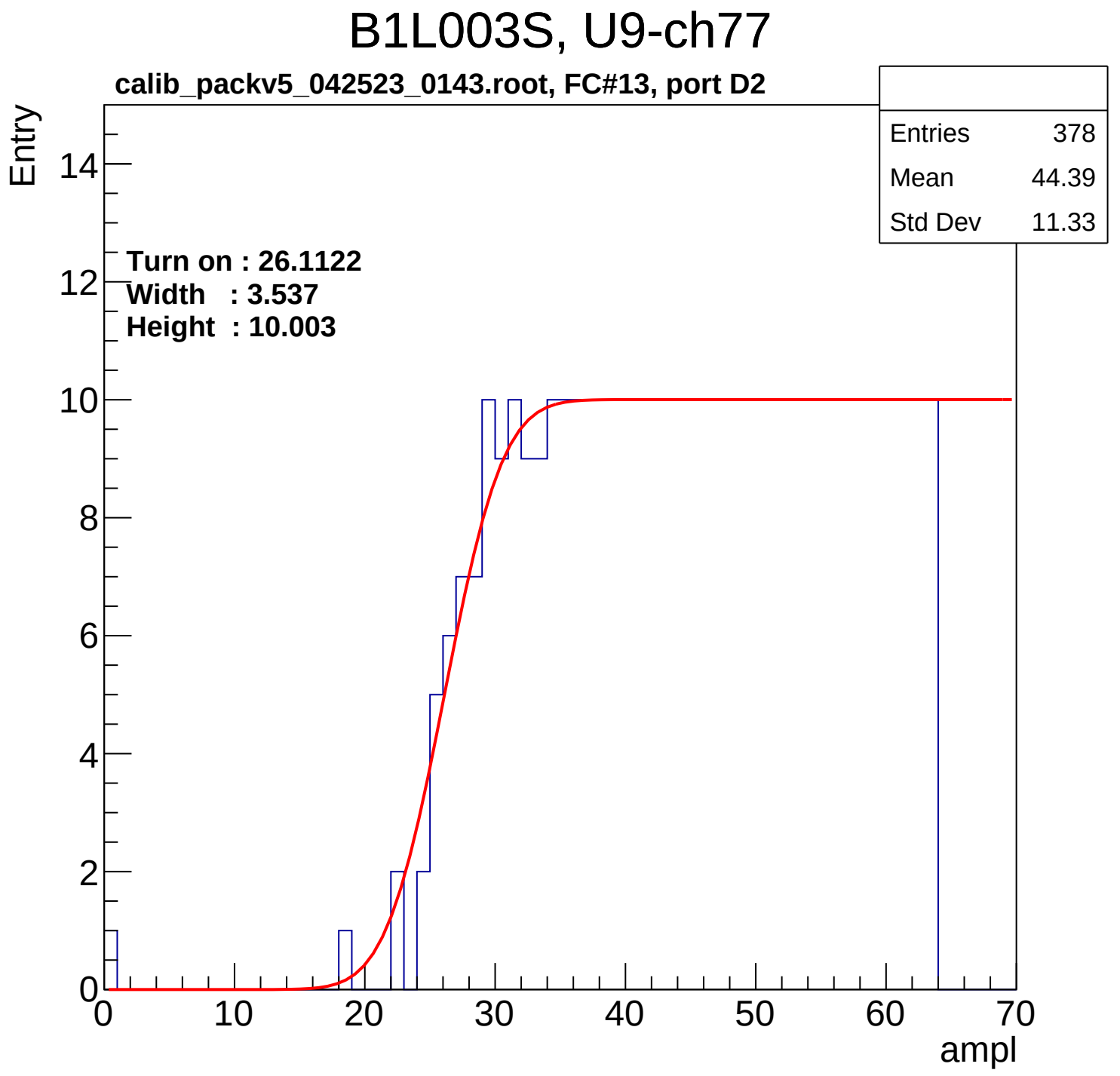

B1L003S, U9-ch72
calib_packv5_042523_0143.root, FC#13, port D2
Entries 364
Mean 45.02
Std Dev 11.15
Turn on : 28.0444
Width : 3.640
Height : 10.069
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

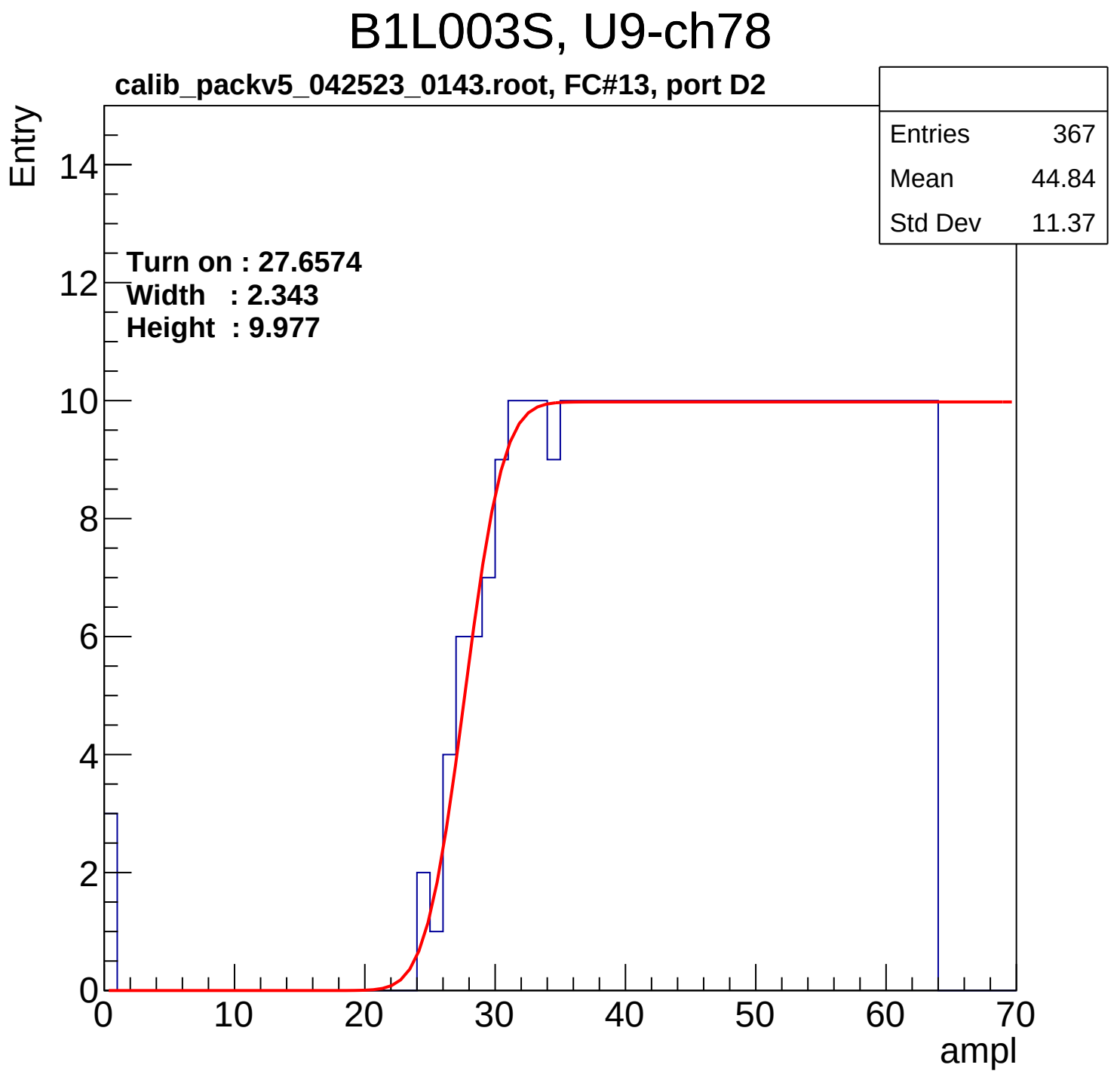

B1L003S, U9-ch73
calib_packv5_042523_0143.root, FC#13, port D2
Entries 373
Mean 44.64
Std Dev 11.19
Turn on : 27.1375
Width : 3.161
Height : 10.004
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

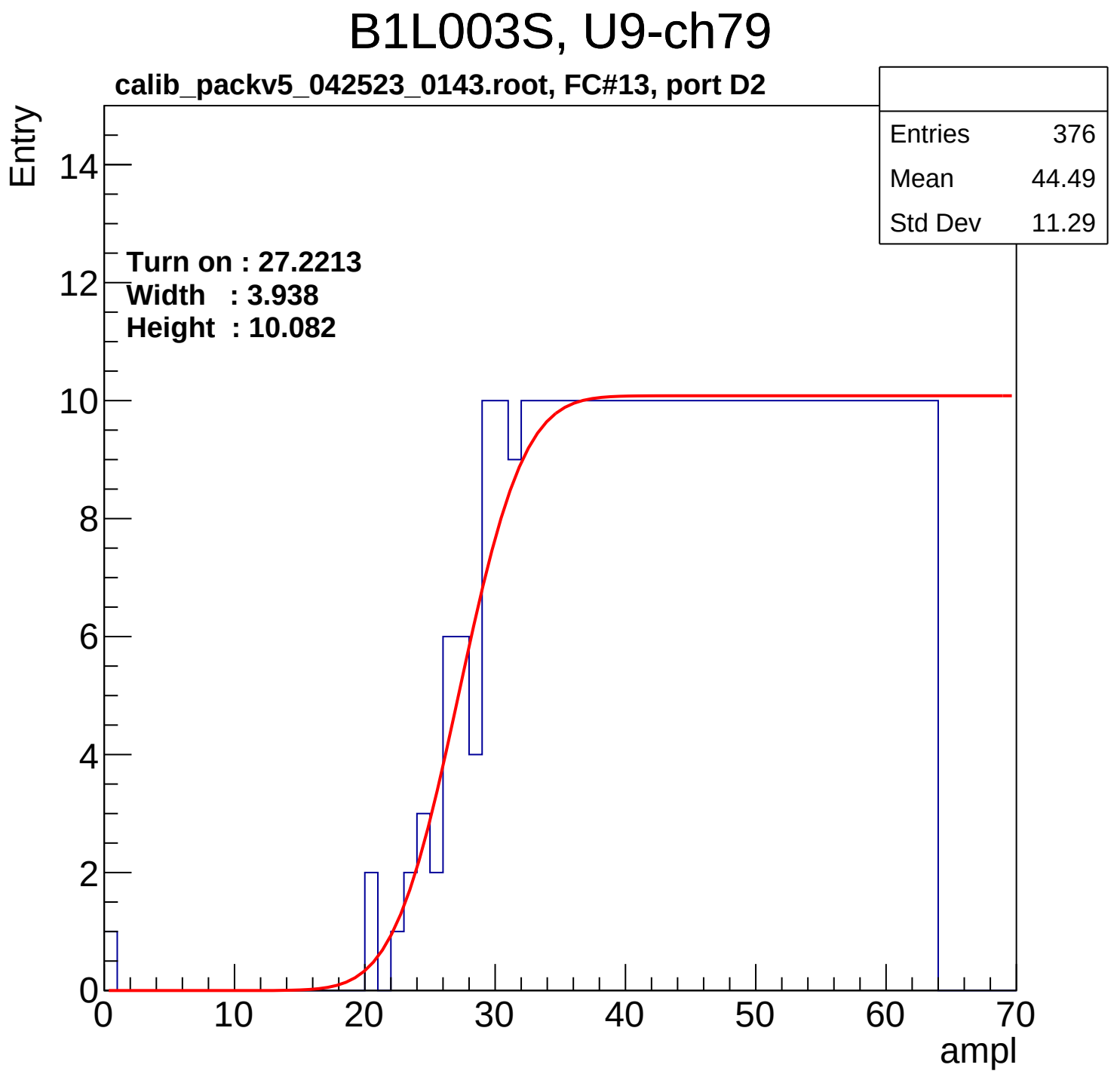

B1L003S, U9-ch74
calib_packv5_042523_0143.root, FC#13, port D2
Entries 390
Mean 43.76
Std Dev 11.79
Turn on : 25.3615
Width : 3.043
Height : 10.014
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

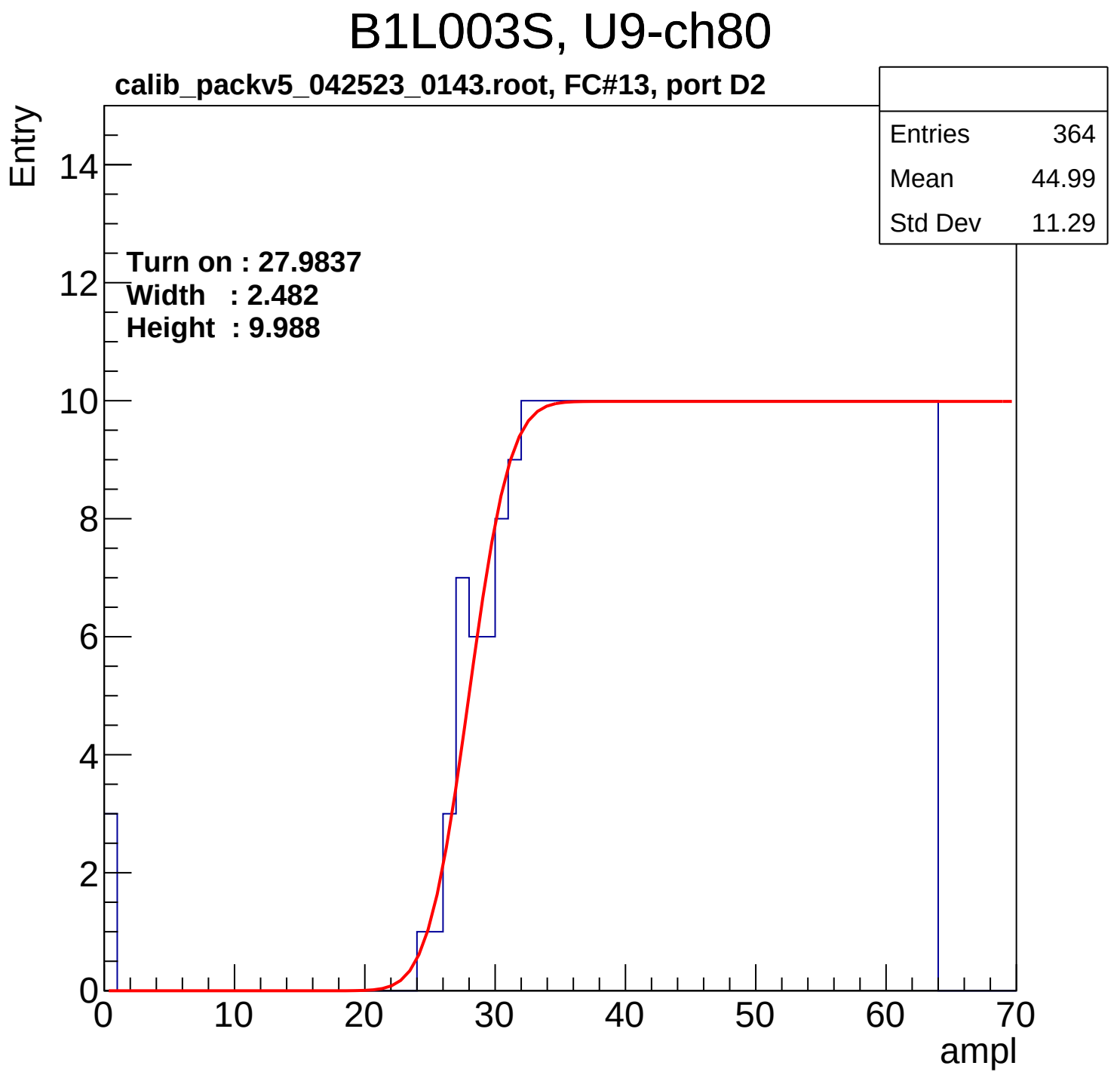

B1L003S, U9-ch75
calib_packv5_042523_0143.root, FC#13, port D2
Entries 392
Mean 43.73
Std Dev 11.67
Turn on : 25.0833
Width : 2.689
Height : 9.966
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

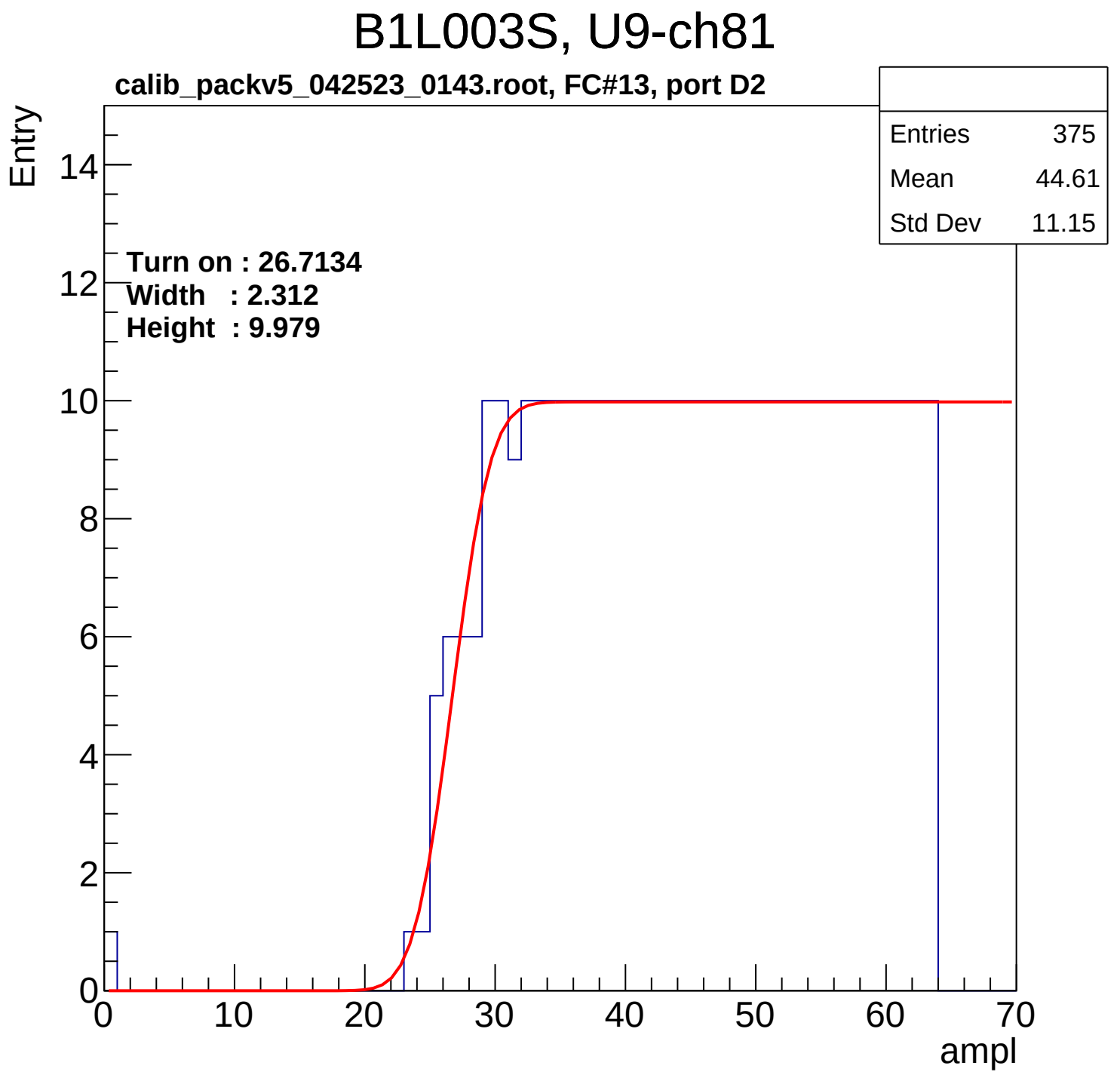

B1L003S, U9-ch76
calib_packv5_042523_0143.root, FC#13, port D2
Entries 362
Mean 45.25
Std Dev 10.8
Turn on : 28.3567
Width : 2.637
Height : 10.066
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

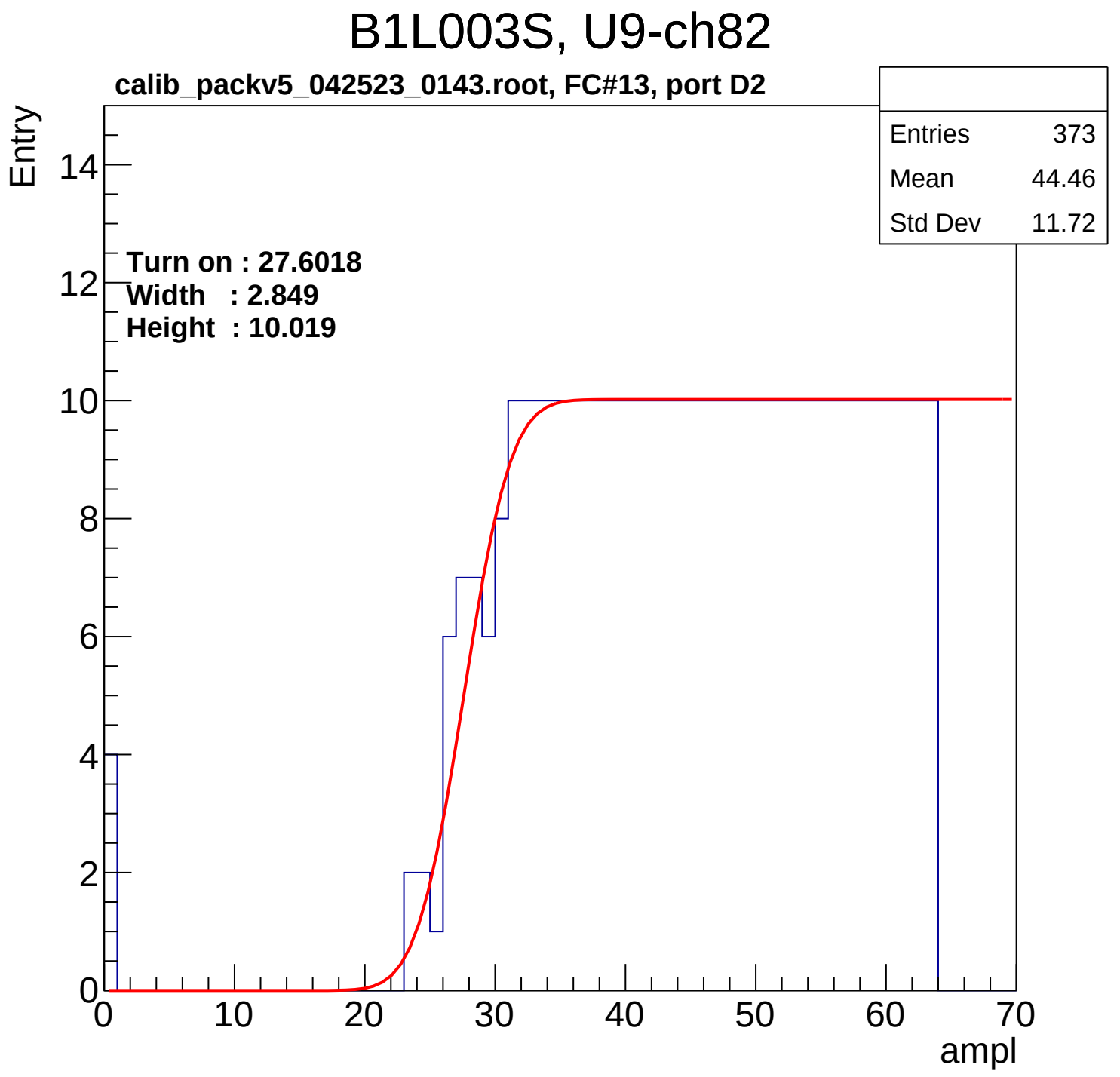

B1L003S, U9-ch77
calib_packv5_042523_0143.root, FC#13, port D2
Entries 378
Mean 44.39
Std Dev 11.33
Turn on : 26.1122
Width : 3.537
Height : 10.003
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

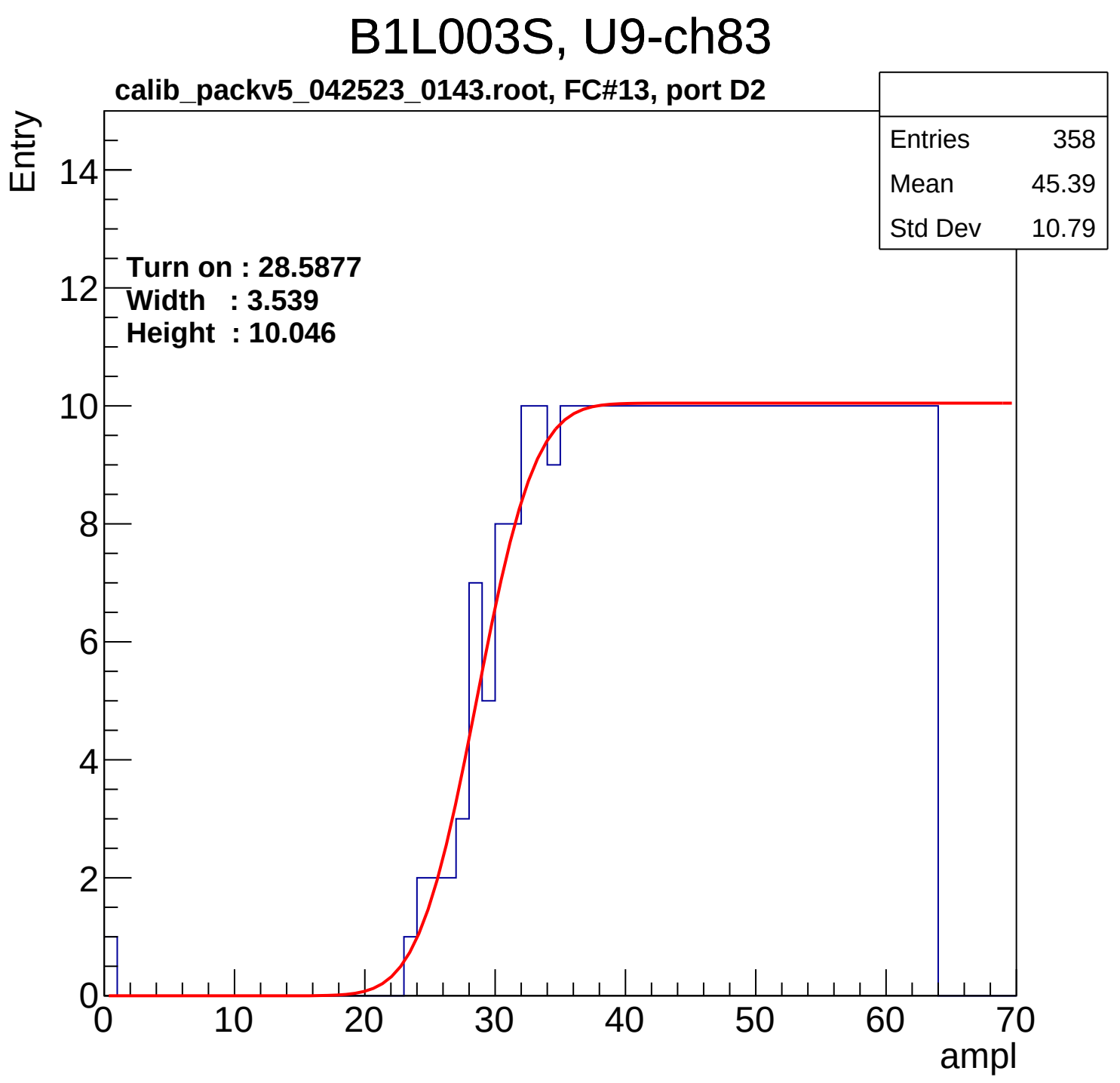

B1L003S, U9-ch78
calib_packv5_042523_0143.root, FC#13, port D2
Entries 367
Mean 44.84
Std Dev 11.37
Turn on : 27.6574
Width : 2.343
Height : 9.977
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

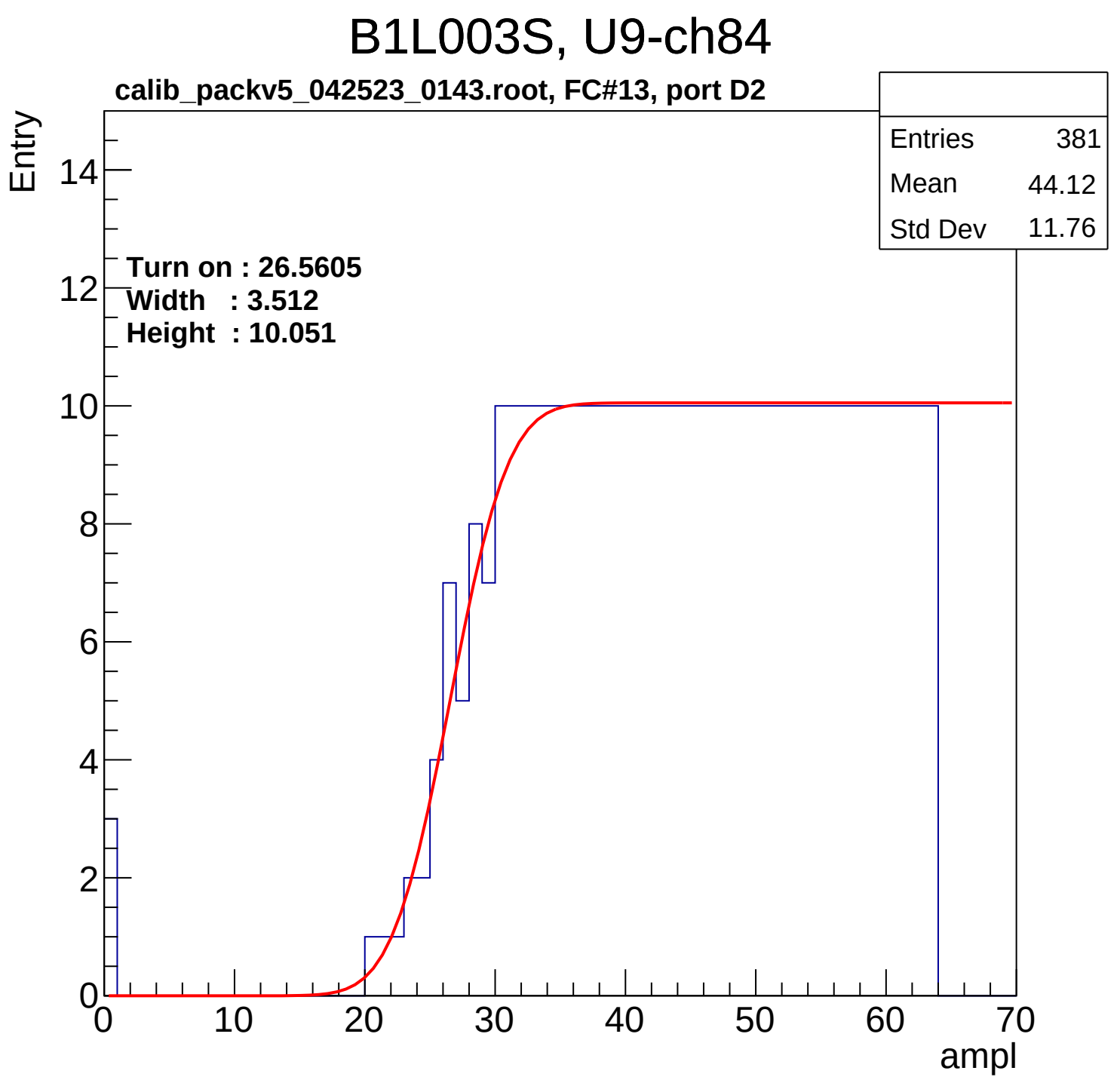

B1L003S, U9-ch79
calib_packv5_042523_0143.root, FC#13, port D2
Entries 376
Mean 44.49
Std Dev 11.29
Turn on : 27.2213
Width : 3.938
Height : 10.082
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

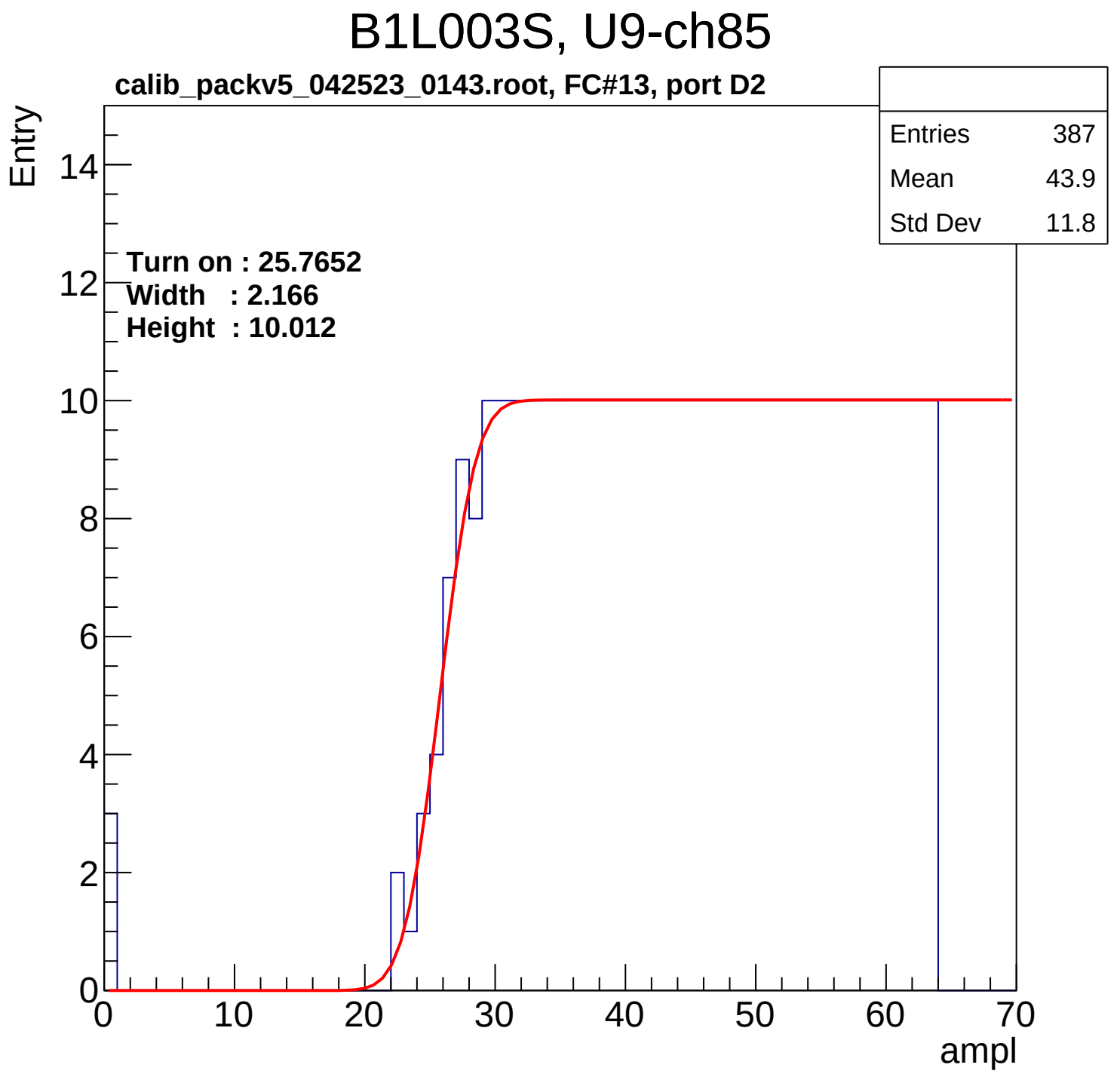

B1L003S, U9-ch80
calib_packv5_042523_0143.root, FC#13, port D2
Entries 364
Mean 44.99
Std Dev 11.29
Turn on : 27.9837
Width : 2.482
Height : 9.988
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

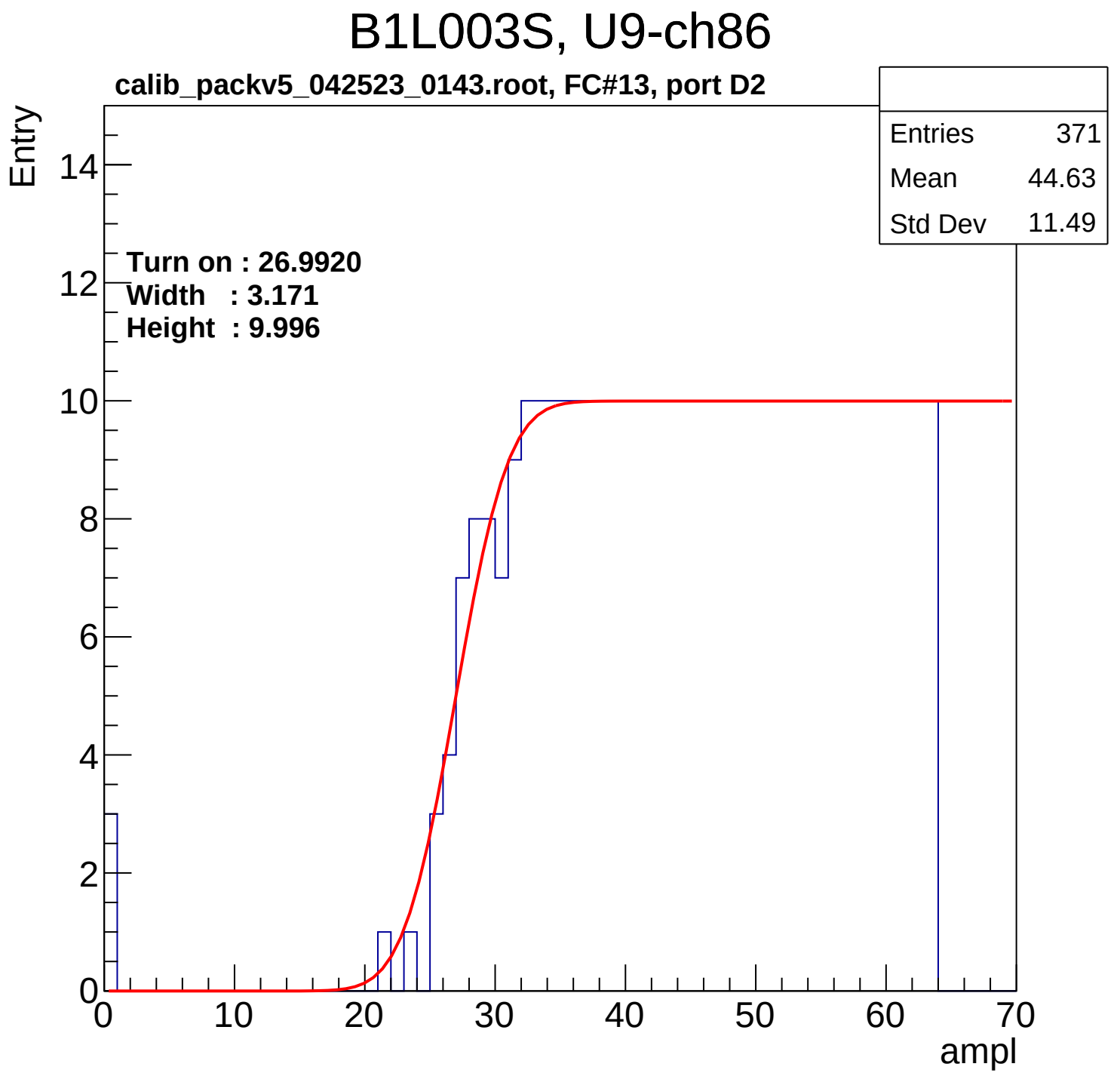

B1L003S, U9-ch81
calib_packv5_042523_0143.root, FC#13, port D2
Entries 375
Mean 44.61
Std Dev 11.15
Turn on : 26.7134
Width : 2.312
Height : 9.979
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

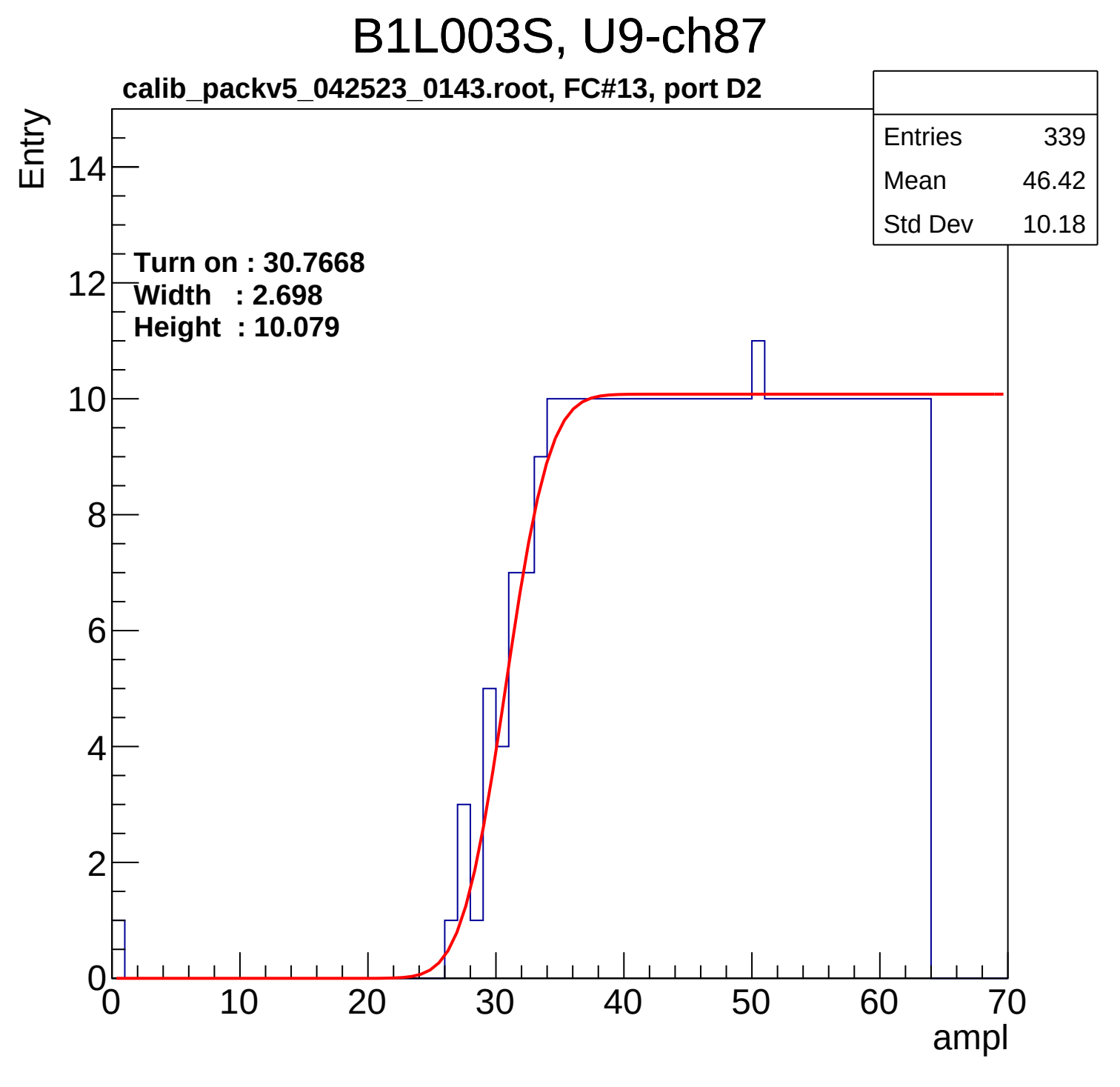

B1L003S, U9-ch82
calib_packv5_042523_0143.root, FC#13, port D2
Entries 373
Mean 44.46
Std Dev 11.72
Turn on : 27.6018
Width : 2.849
Height : 10.019
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

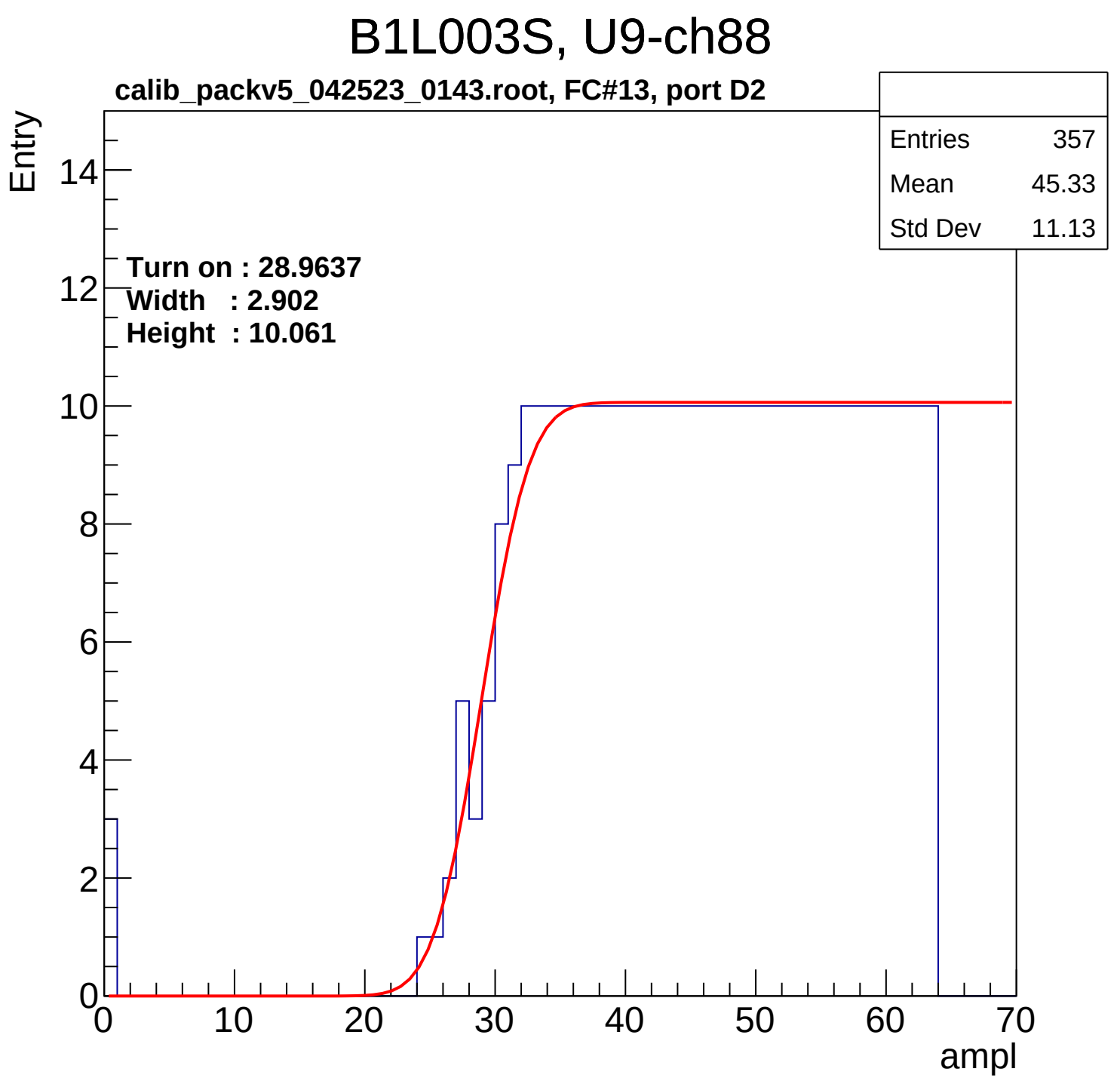

B1L003S, U9-ch83
calib_packv5_042523_0143.root, FC#13, port D2
Entries 358
Mean 45.39
Std Dev 10.79
Turn on : 28.5877
Width : 3.539
Height : 10.046
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

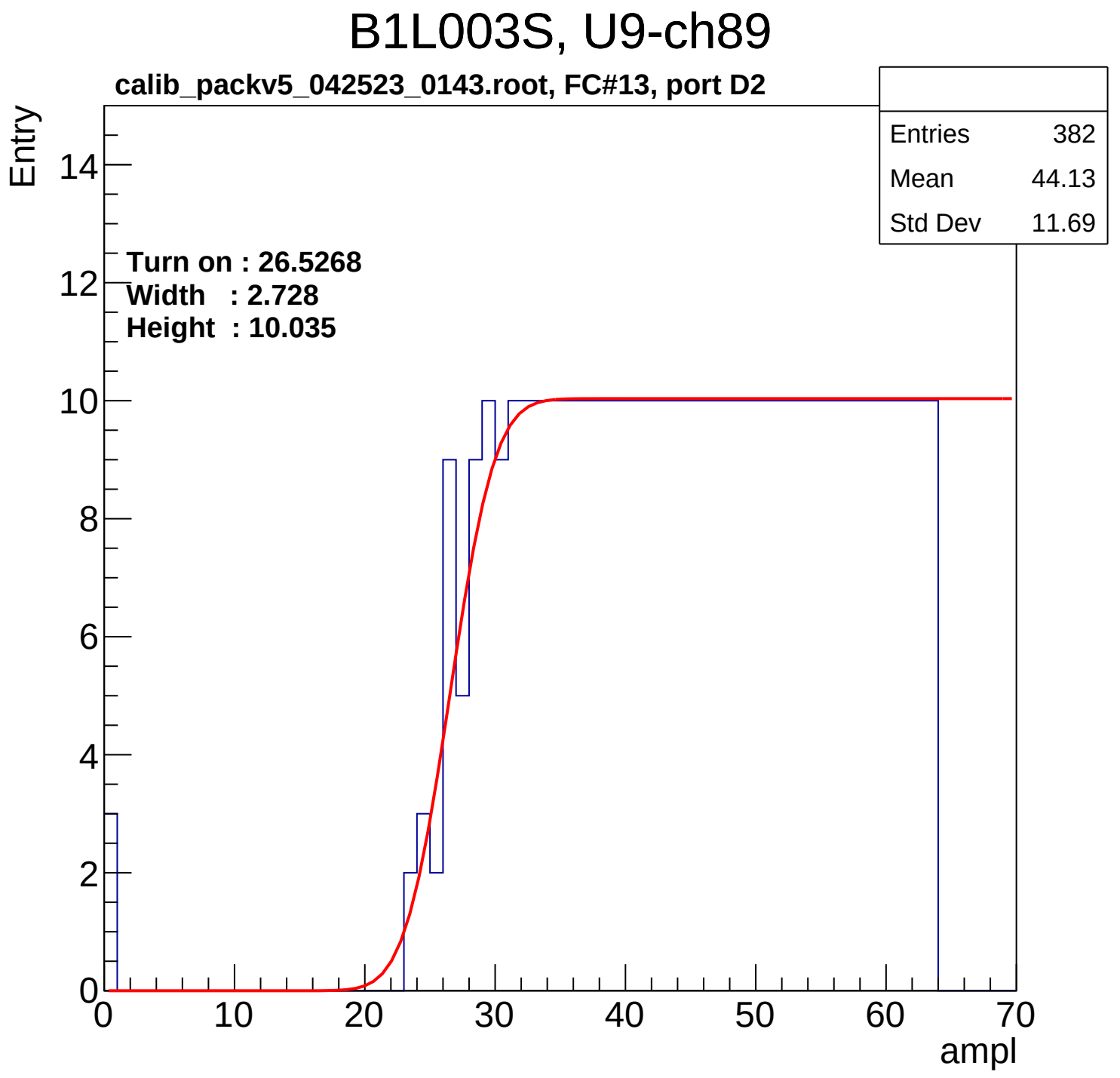

B1L003S, U9-ch84
calib_packv5_042523_0143.root, FC#13, port D2
Entries 381
Mean 44.12
Std Dev 11.76
Turn on : 26.5605
Width : 3.512
Height : 10.051
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

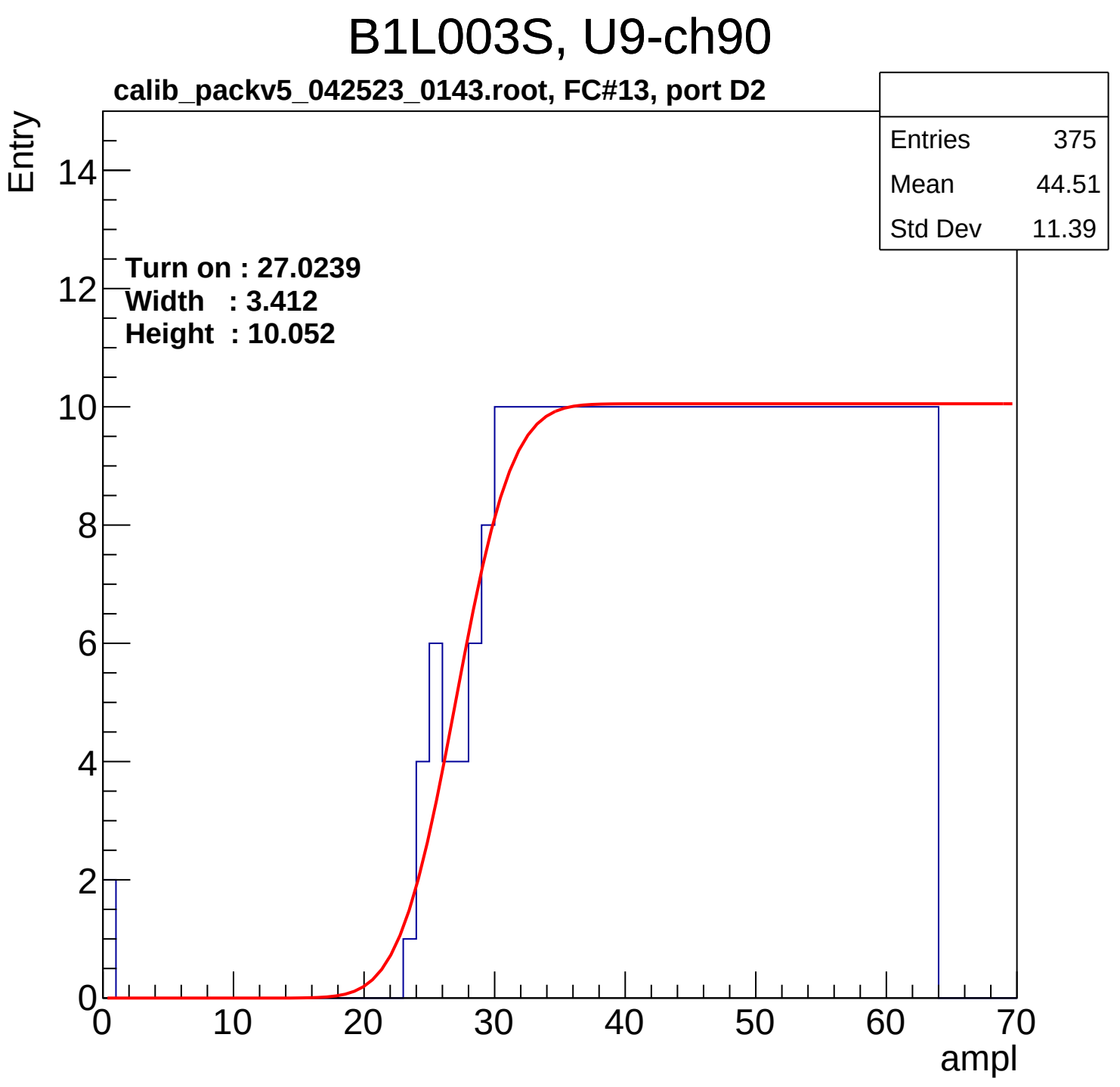

B1L003S, U9-ch85
calib_packv5_042523_0143.root, FC#13, port D2
Entries 387
Mean 43.9
Std Dev 11.8
Turn on : 25.7652
Width : 2.166
Height : 10.012
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

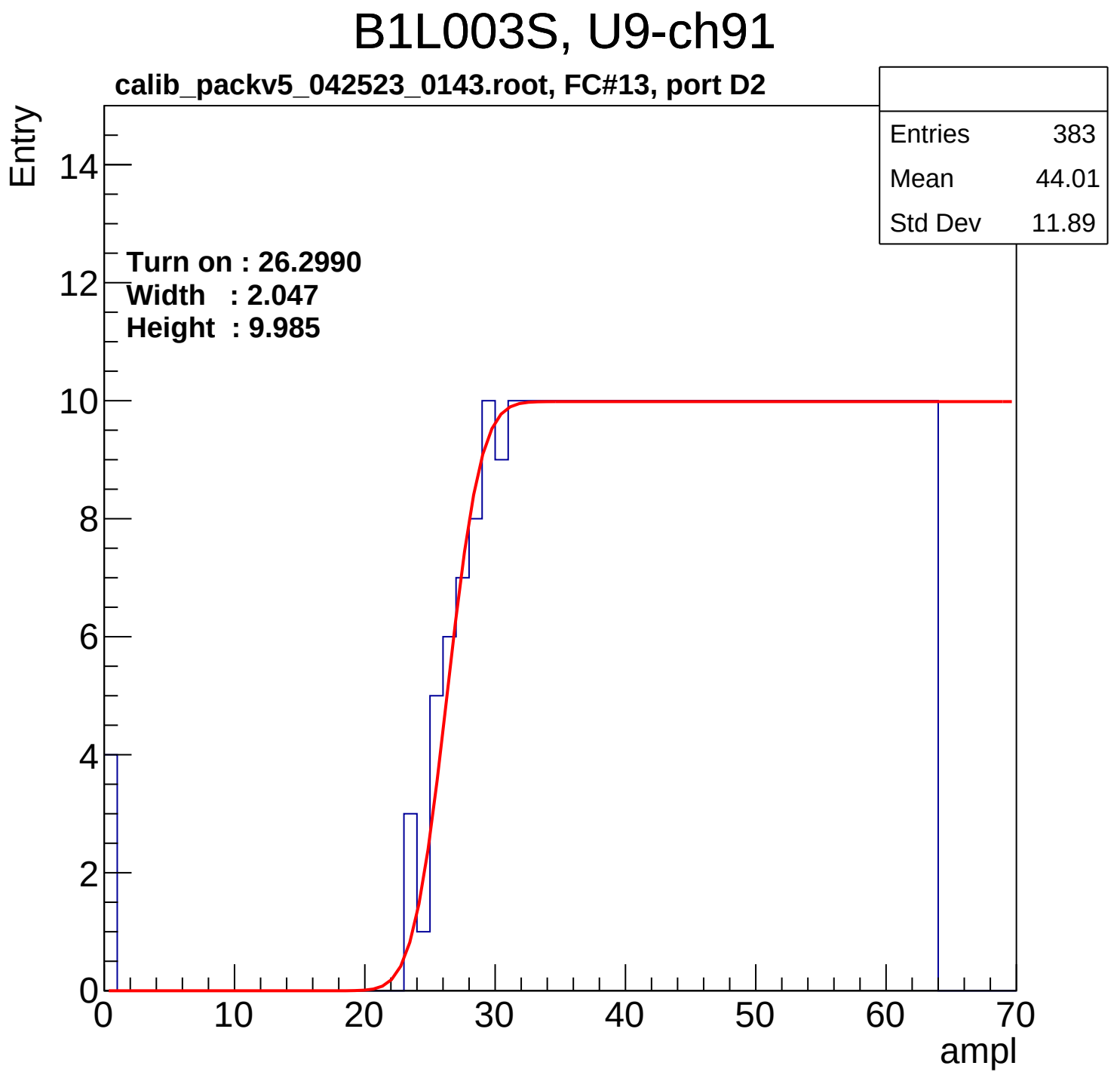

B1L003S, U9-ch86
calib_packv5_042523_0143.root, FC#13, port D2
Entries 371
Mean 44.63
Std Dev 11.49
Turn on : 26.9920
Width : 3.171
Height : 9.996
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

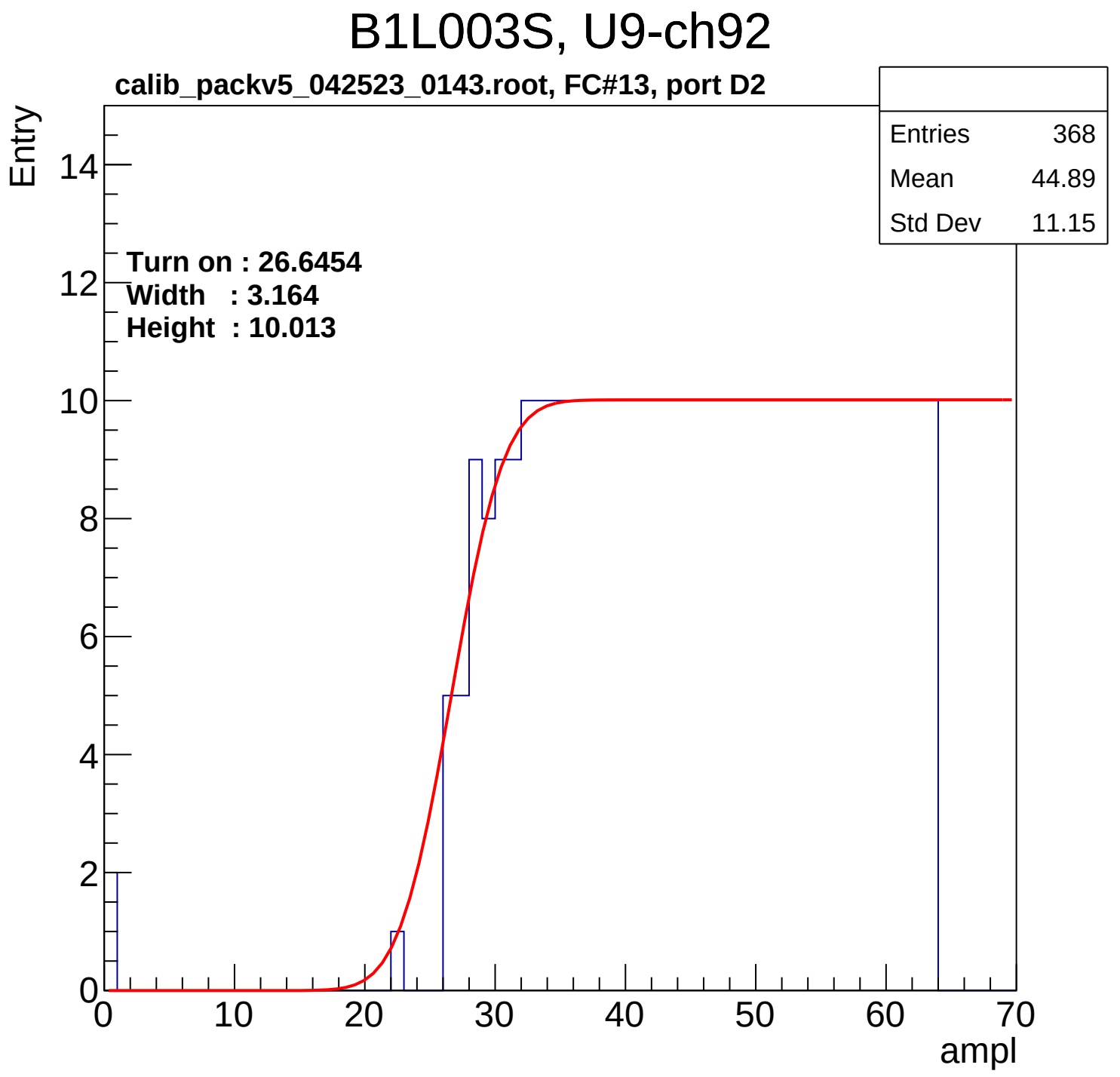

B1L003S, U9-ch87
calib_packv5_042523_0143.root, FC#13, port D2
Entries 339
Mean 46.42
Std Dev 10.18
Turn on : 30.7668
Width : 2.698
Height : 10.079
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

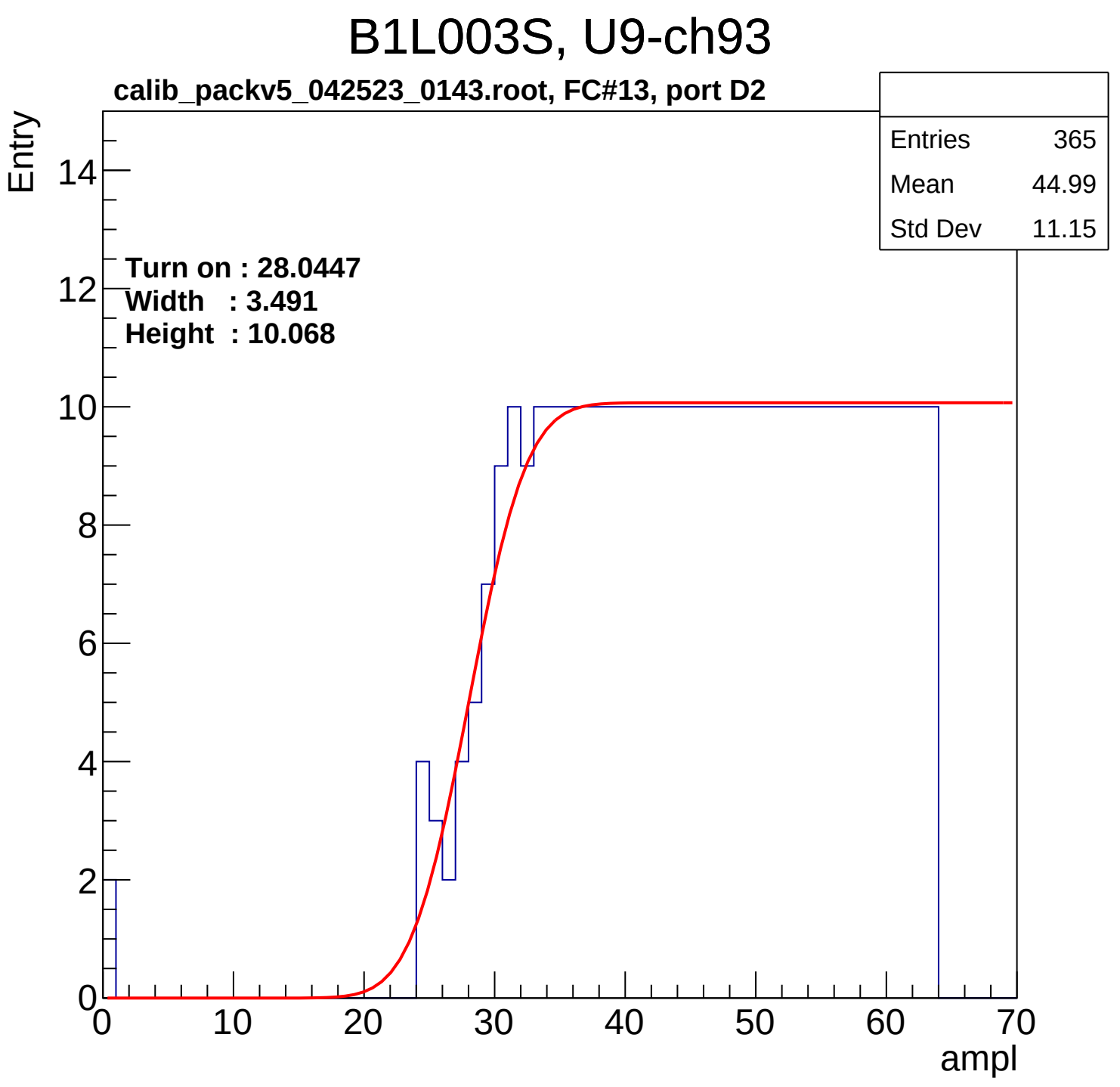

B1L003S, U9-ch88
calib_packv5_042523_0143.root, FC#13, port D2
Entries 357
Mean 45.33
Std Dev 11.13
Turn on : 28.9637
Width : 2.902
Height : 10.061
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

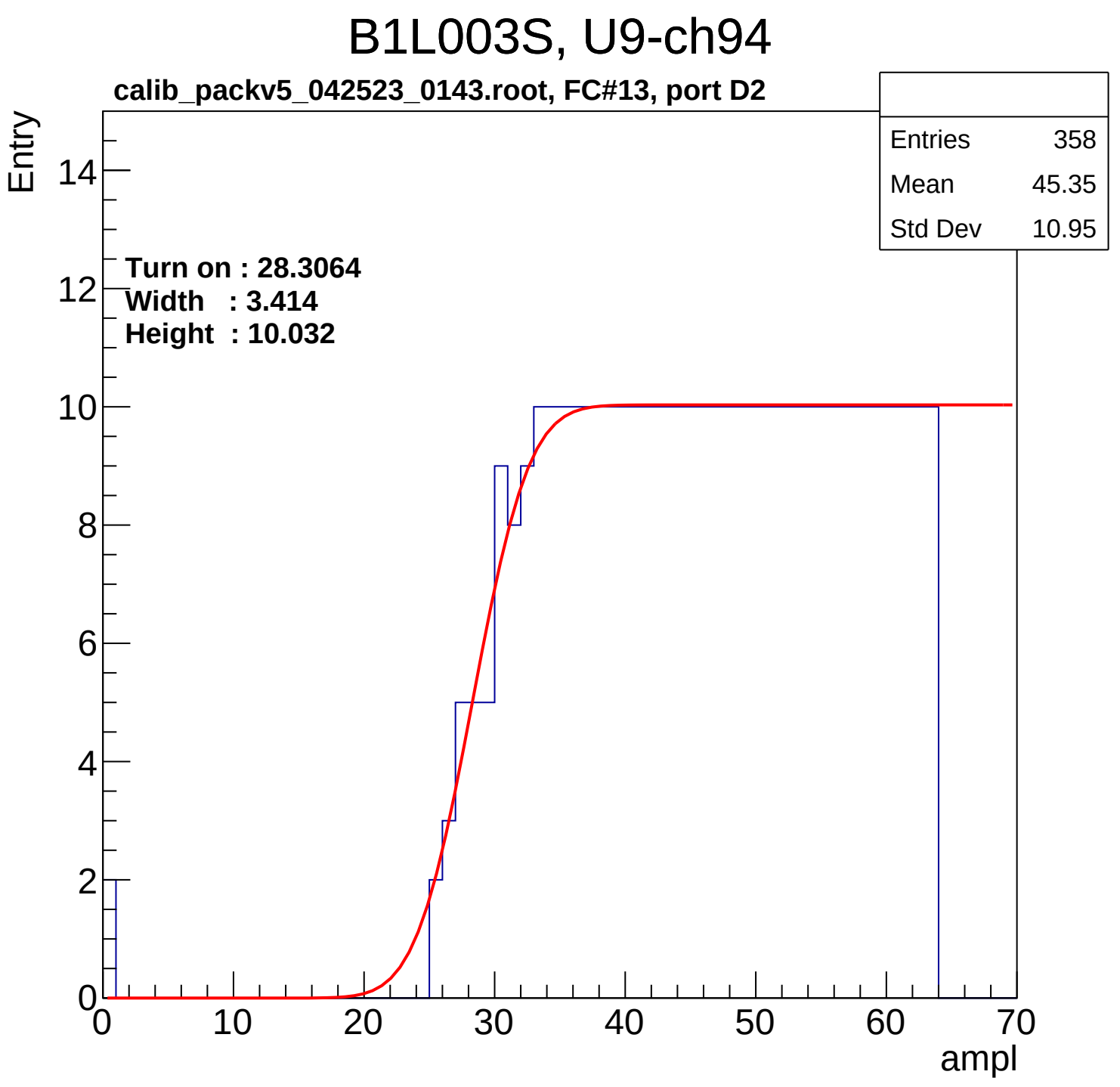

B1L003S, U9-ch89
calib_packv5_042523_0143.root, FC#13, port D2
Entries 382
Mean 44.13
Std Dev 11.69
Turn on : 26.5268
Width : 2.728
Height : 10.035
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

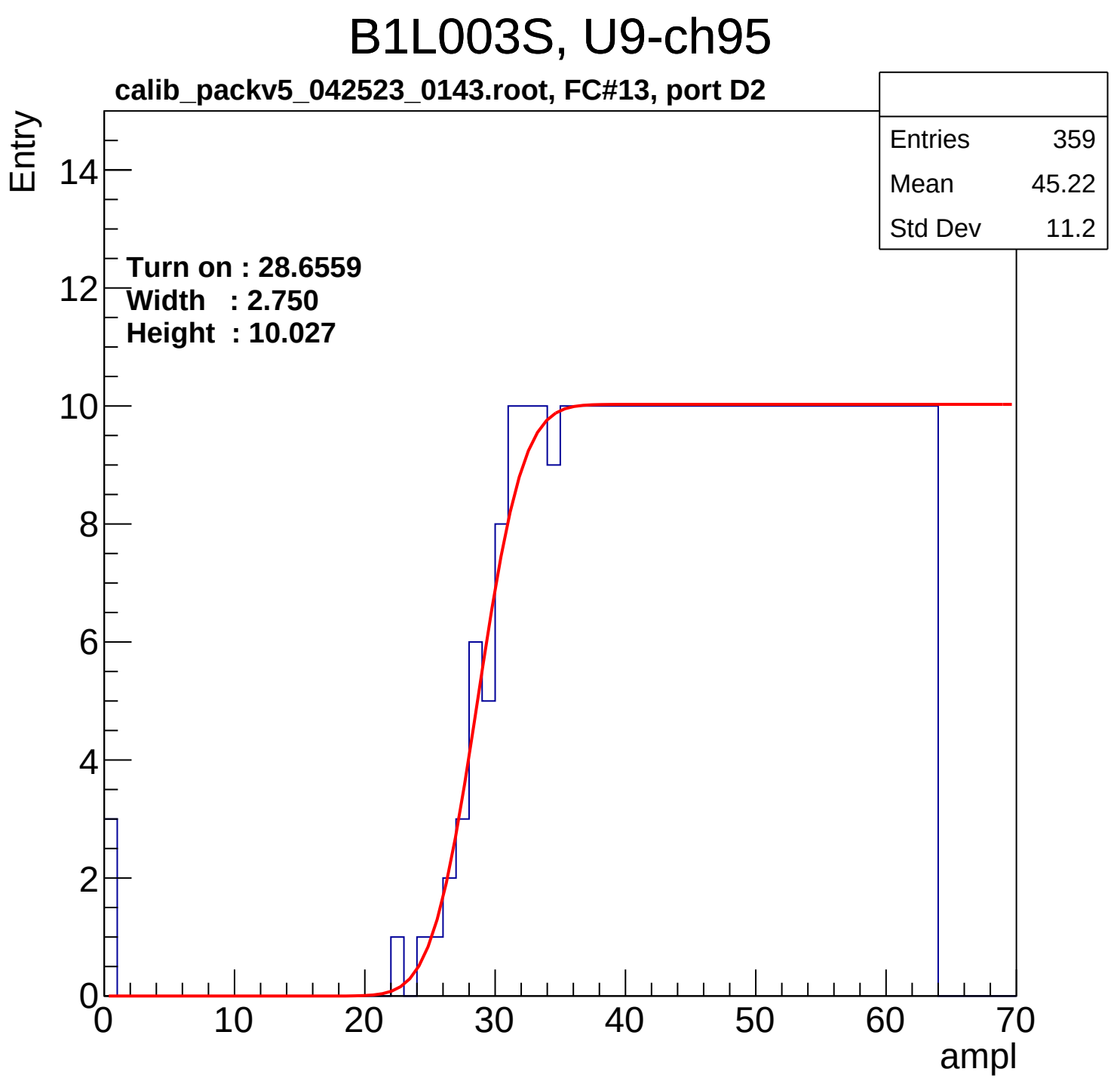

B1L003S, U9-ch90
calib_packv5_042523_0143.root, FC#13, port D2
Entries 375
Mean 44.51
Std Dev 11.39
Turn on : 27.0239
Width : 3.412
Height : 10.052
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

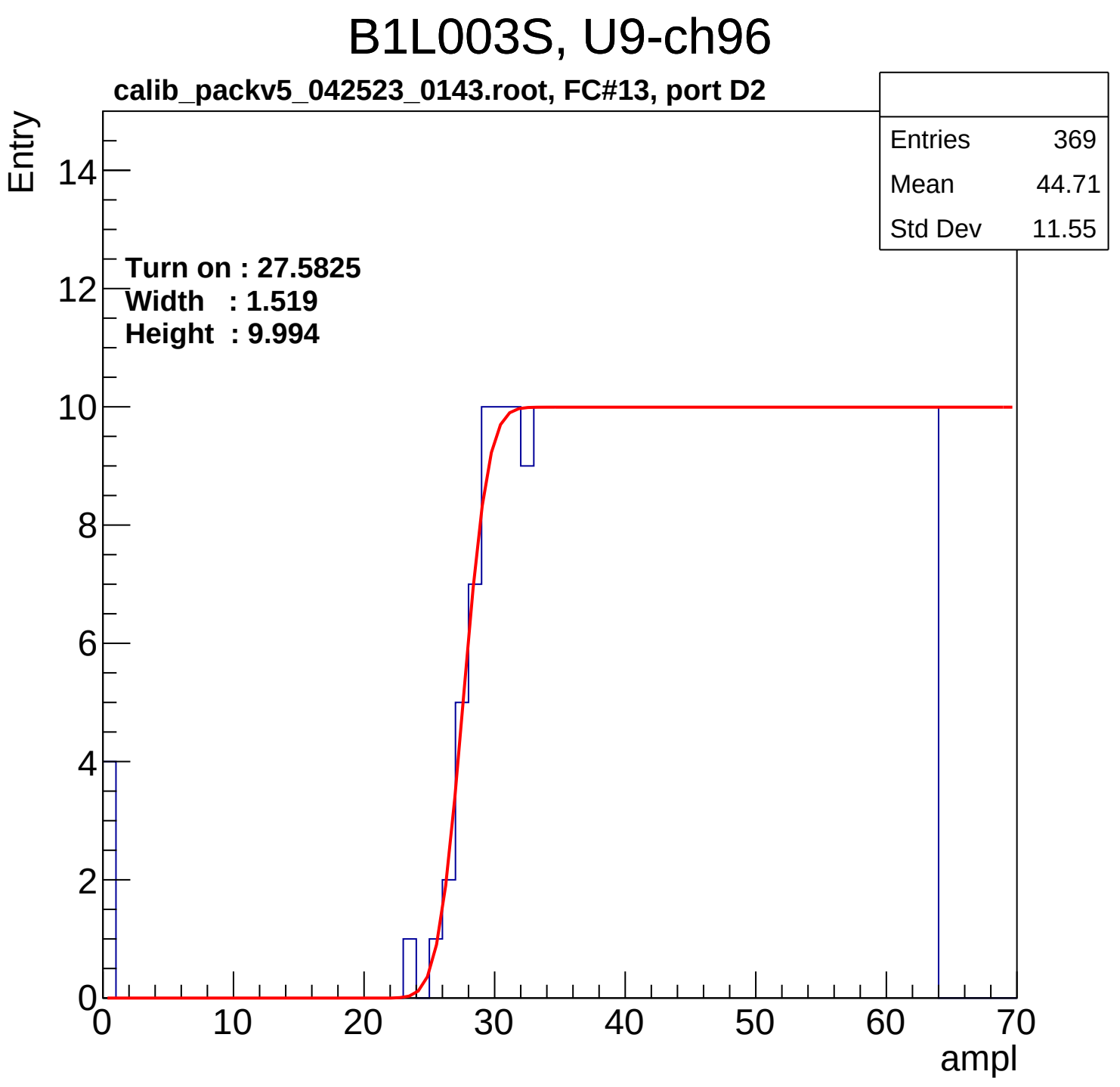

B1L003S, U9-ch91
calib_packv5_042523_0143.root, FC#13, port D2
Entries 383
Mean 44.01
Std Dev 11.89
Turn on : 26.2990
Width : 2.047
Height : 9.985
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

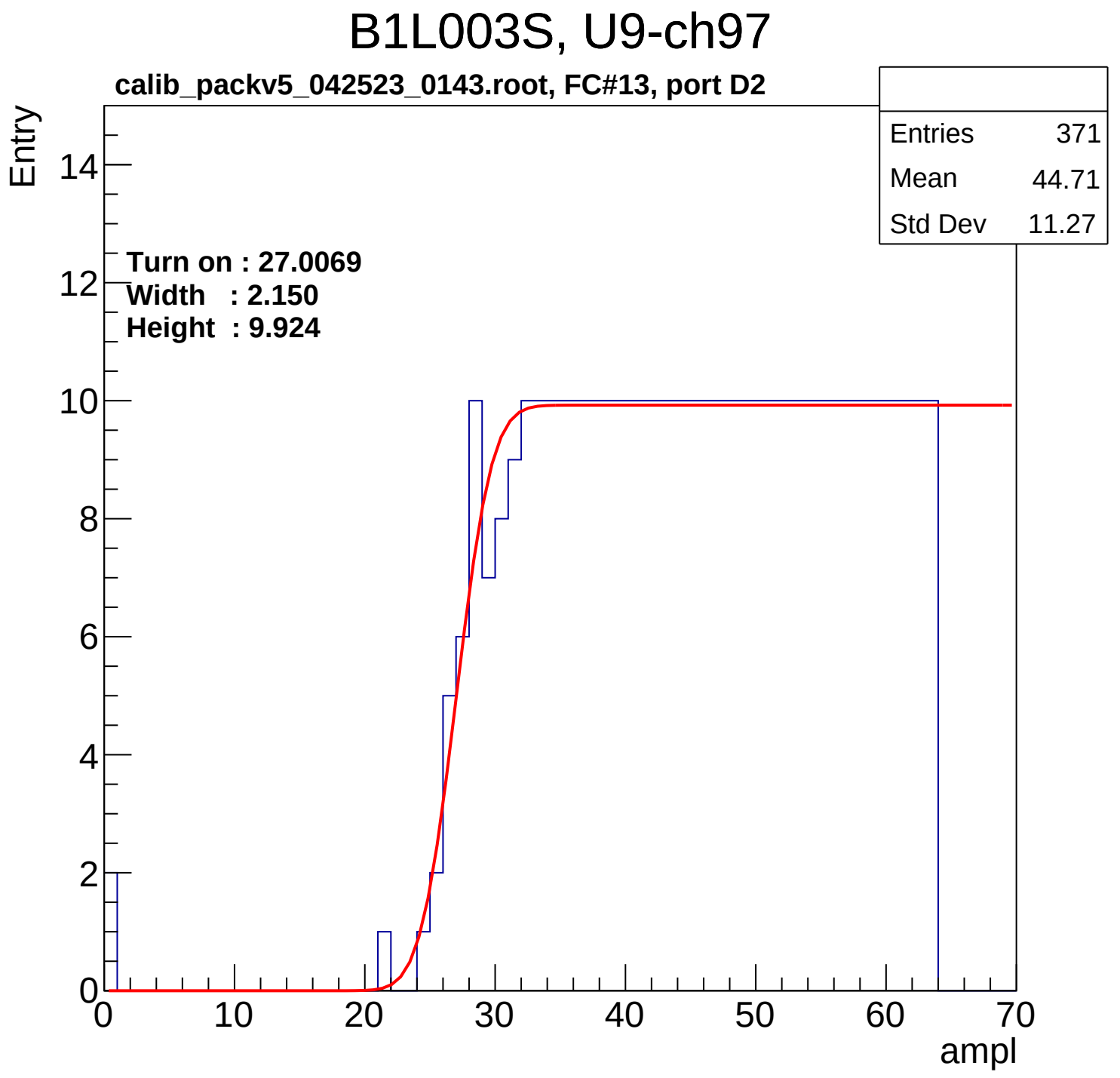

B1L003S, U9-ch92
calib_packv5_042523_0143.root, FC#13, port D2
Entries 368
Mean 44.89
Std Dev 11.15
Turn on : 26.6454
Width : 3.164
Height : 10.013
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

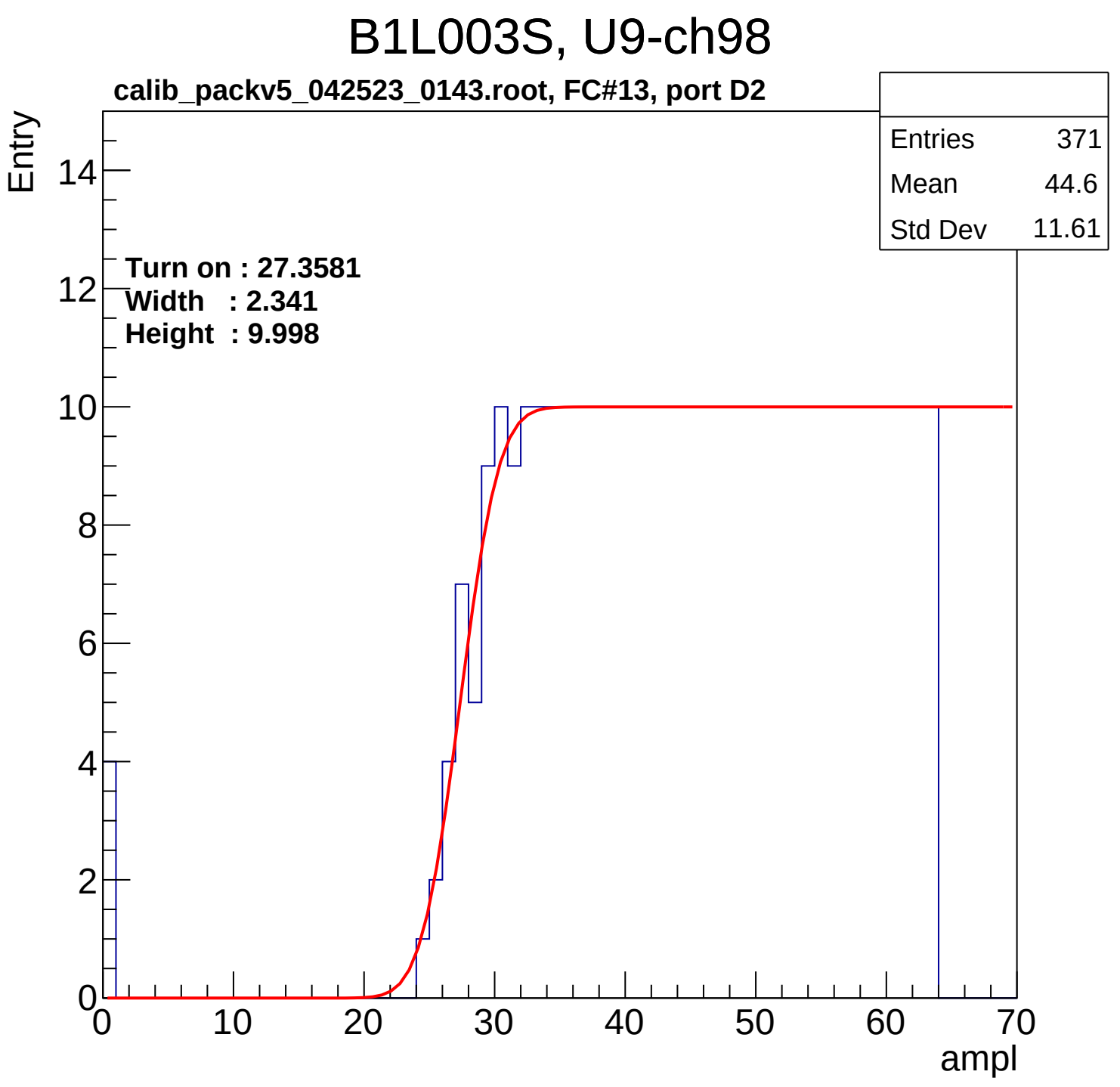

B1L003S, U9-ch93
calib_packv5_042523_0143.root, FC#13, port D2
Entries 365
Mean 44.99
Std Dev 11.15
Turn on : 28.0447
Width : 3.491
Height : 10.068
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

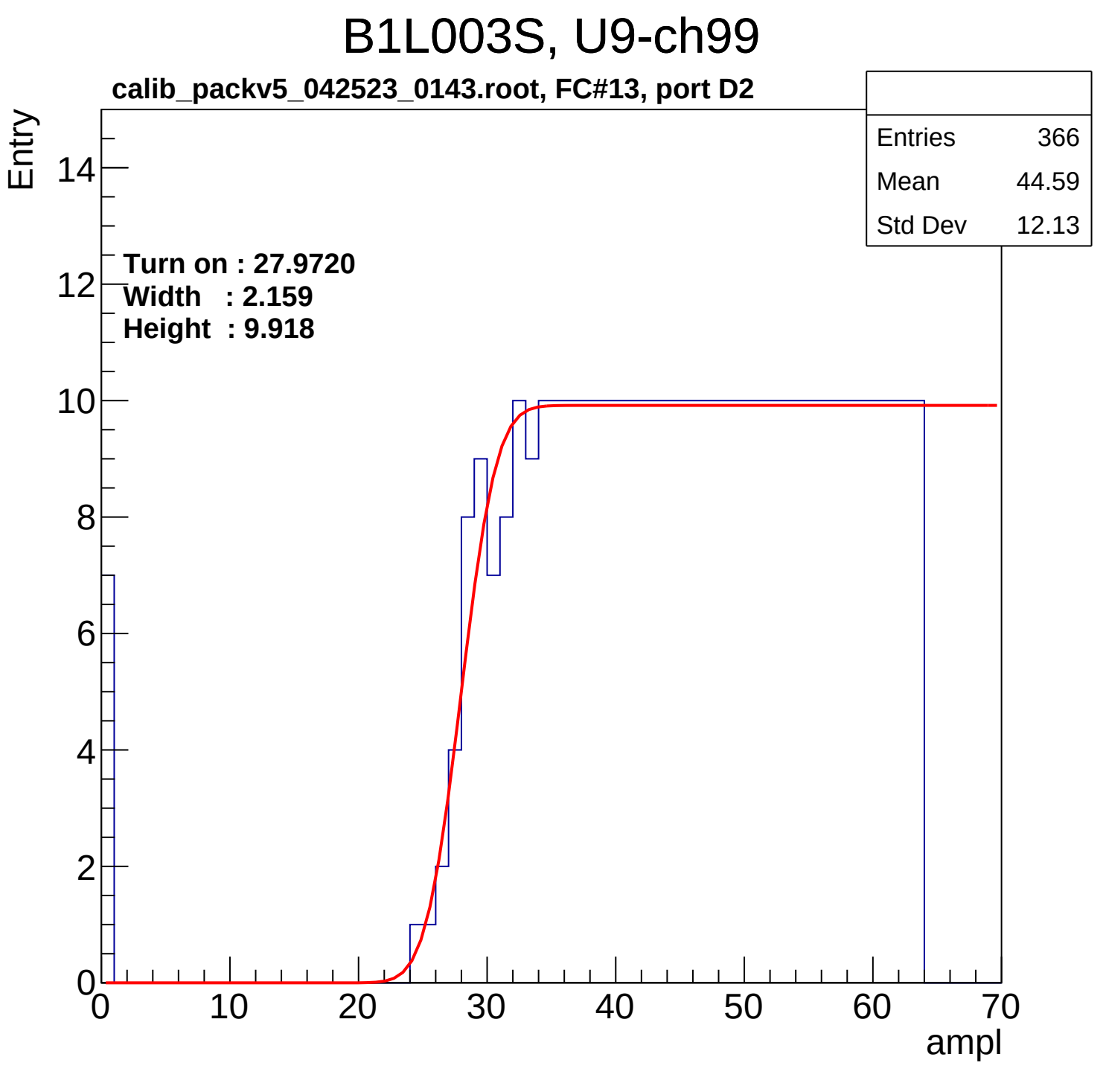

B1L003S, U9-ch94
calib_packv5_042523_0143.root, FC#13, port D2
Entries 358
Mean 45.35
Std Dev 10.95
Turn on : 28.3064
Width : 3.414
Height : 10.032
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

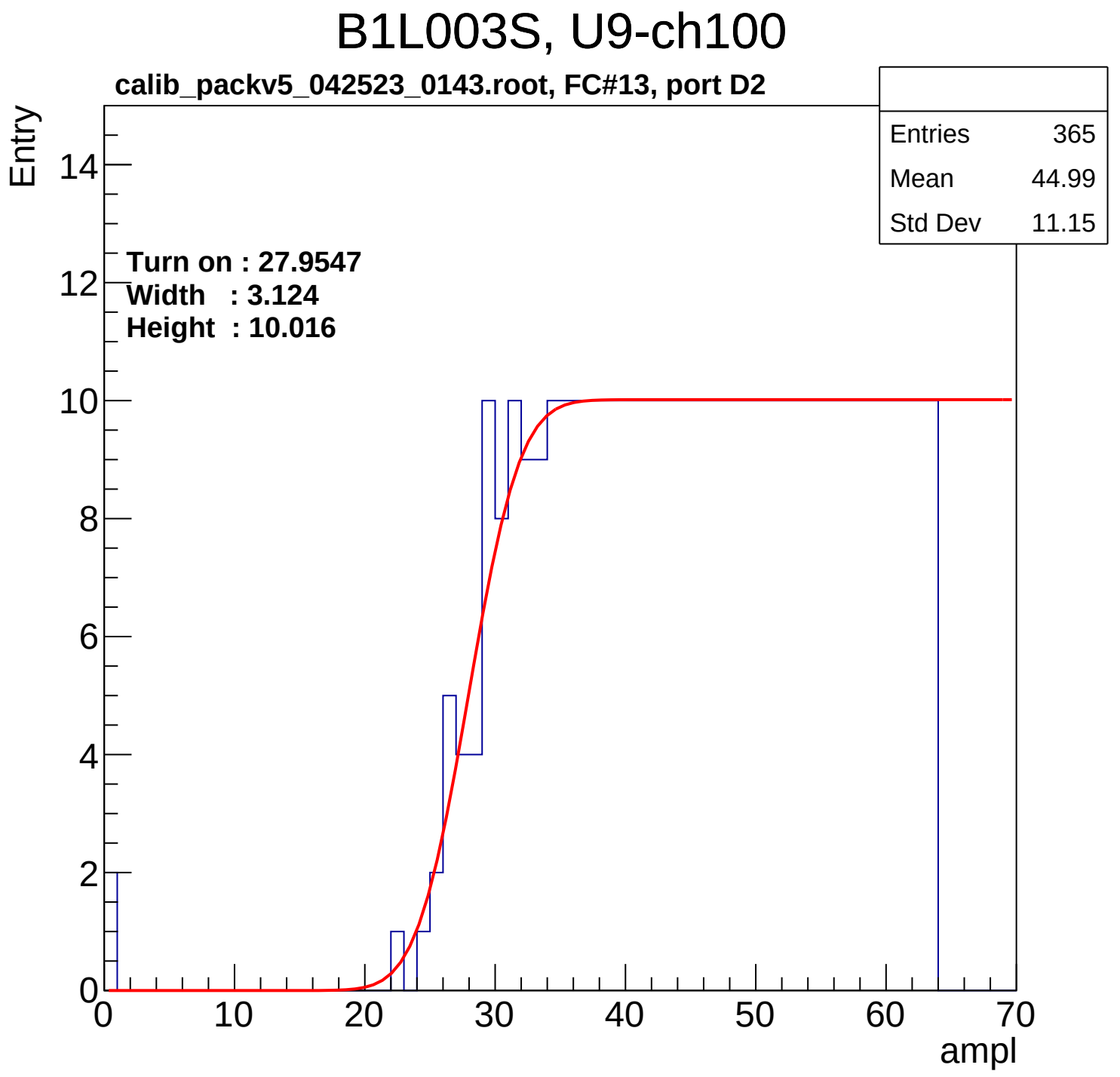

B1L003S, U9-ch95
calib_packv5_042523_0143.root, FC#13, port D2
Entries 359
Mean 45.22
Std Dev 11.2
Turn on : 28.6559
Width : 2.750
Height : 10.027
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

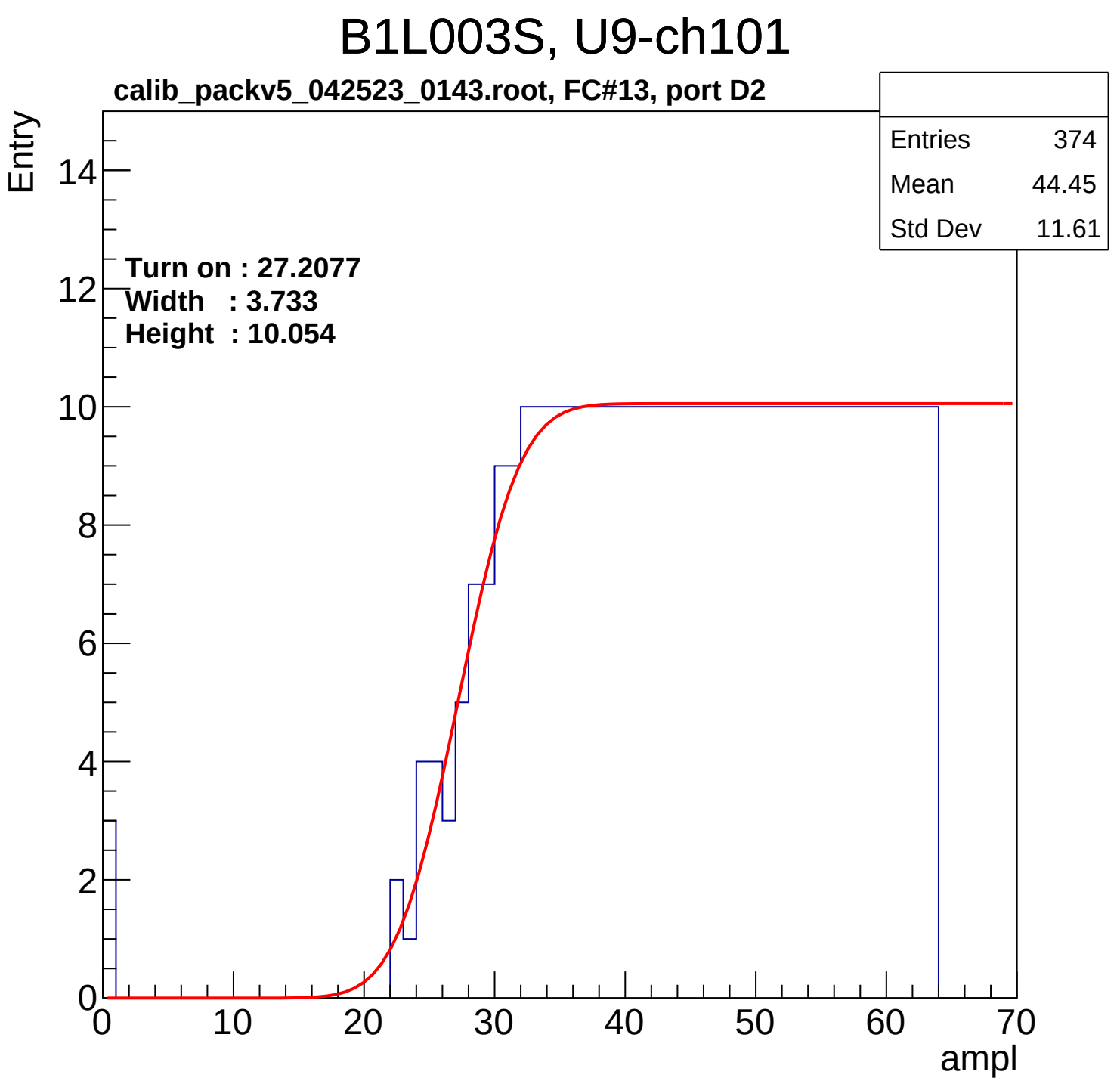

B1L003S, U9-ch96
calib_packv5_042523_0143.root, FC#13, port D2
Entries 369
Mean 44.71
Std Dev 11.55
Turn on : 27.5825
Width : 1.519
Height : 9.994
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

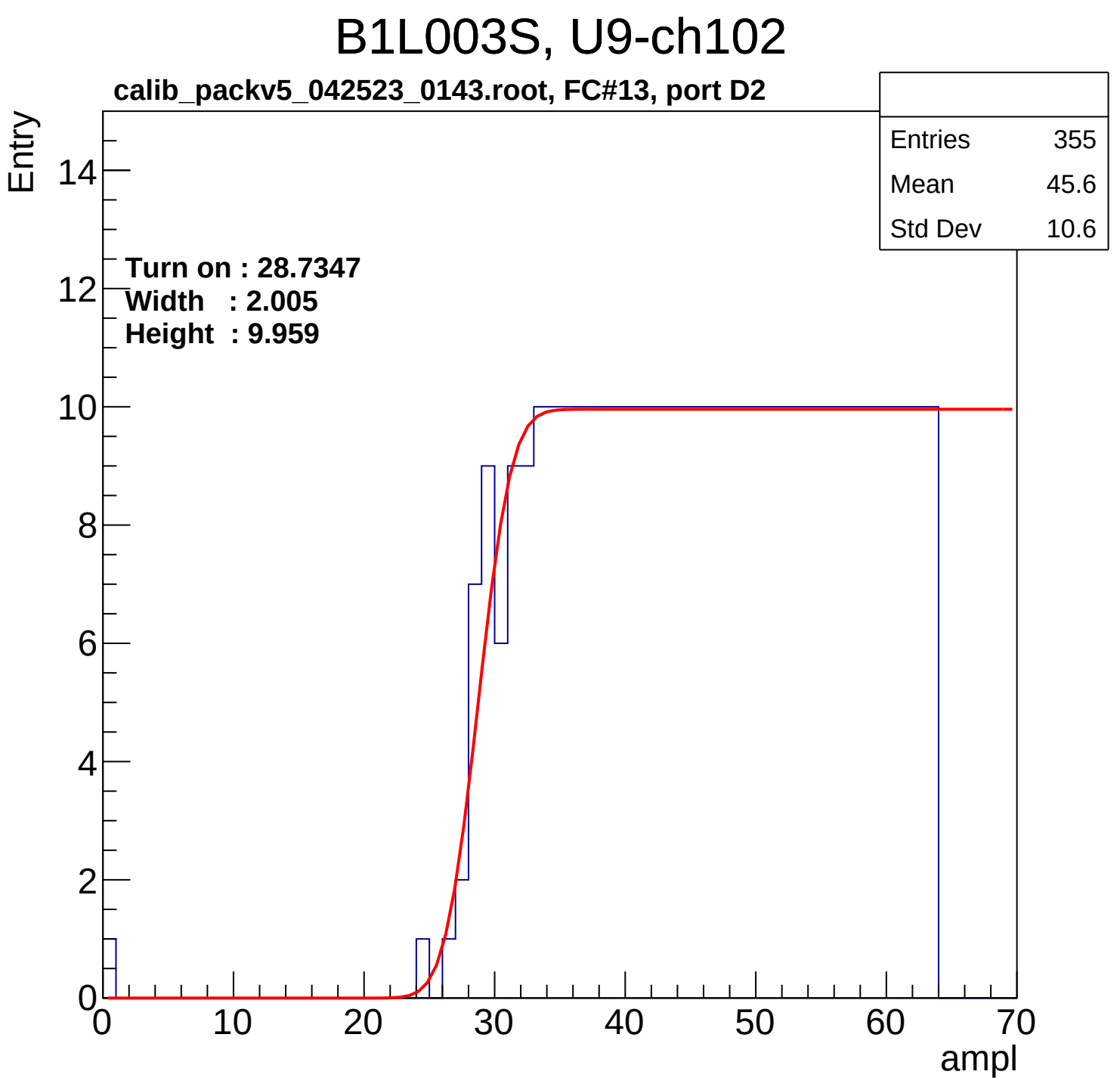

B1L003S, U9-ch97
calib_packv5_042523_0143.root, FC#13, port D2
Entries 371
Mean 44.71
Std Dev 11.27
Turn on : 27.0069
Width : 2.150
Height : 9.924
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

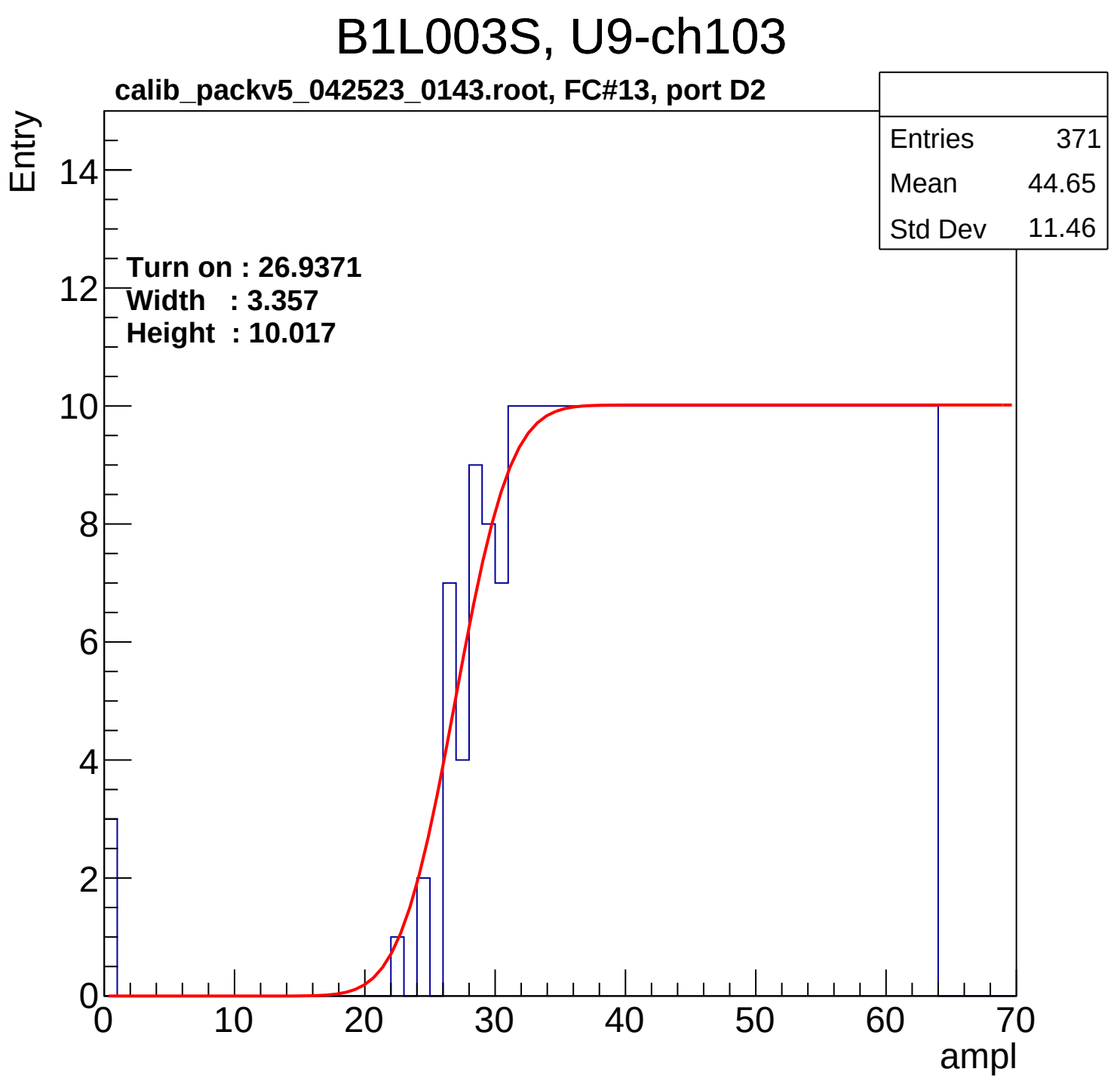

B1L003S, U9-ch98
calib_packv5_042523_0143.root, FC#13, port D2
Entries 371
Mean 44.6
Std Dev 11.61
Turn on : 27.3581
Width : 2.341
Height : 9.998
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

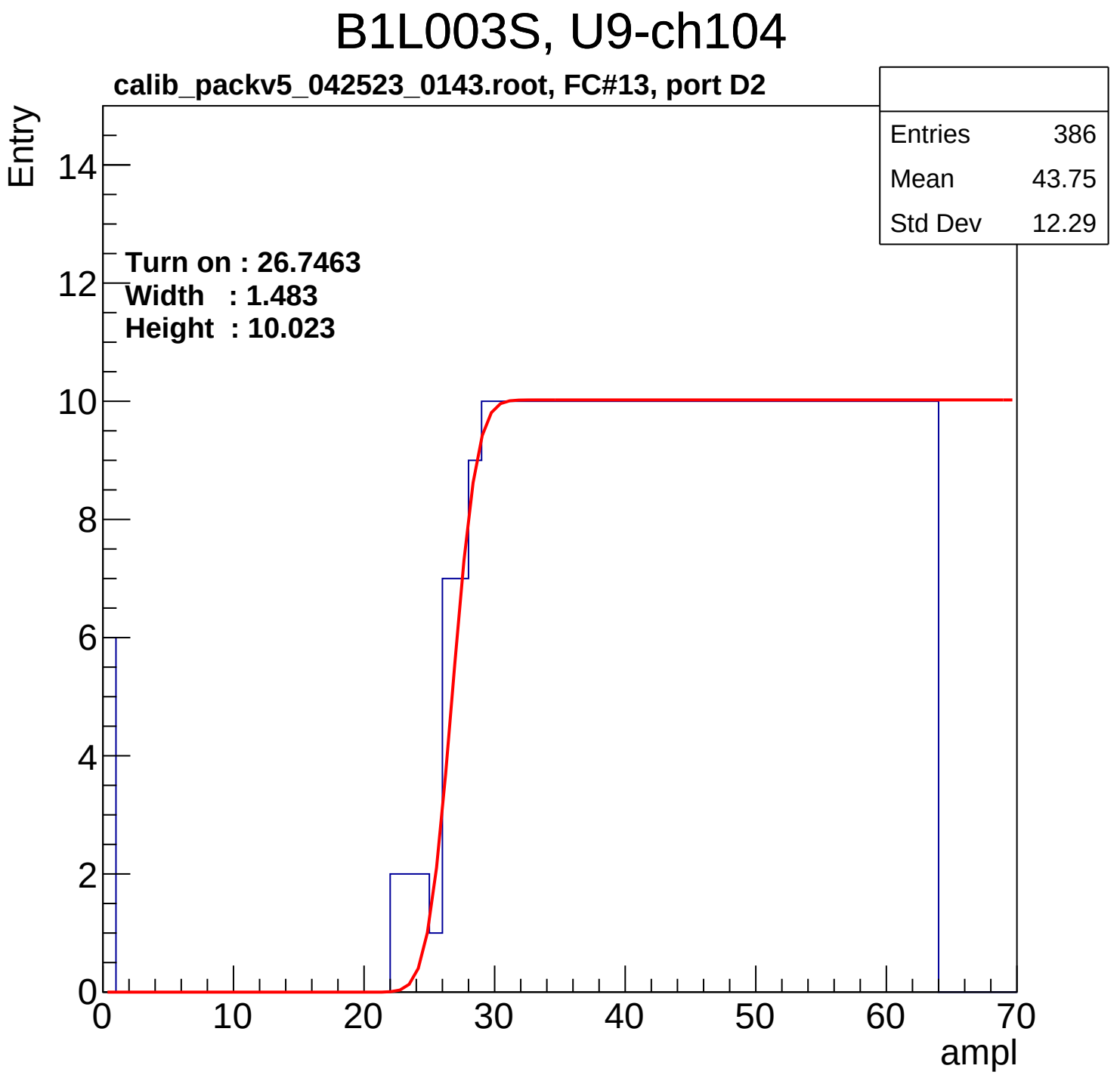

B1L003S, U9-ch99
calib_packv5_042523_0143.root, FC#13, port D2
Entries 366
Mean 44.59
Std Dev 12.13
Turn on : 27.9720
Width : 2.159
Height : 9.918
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

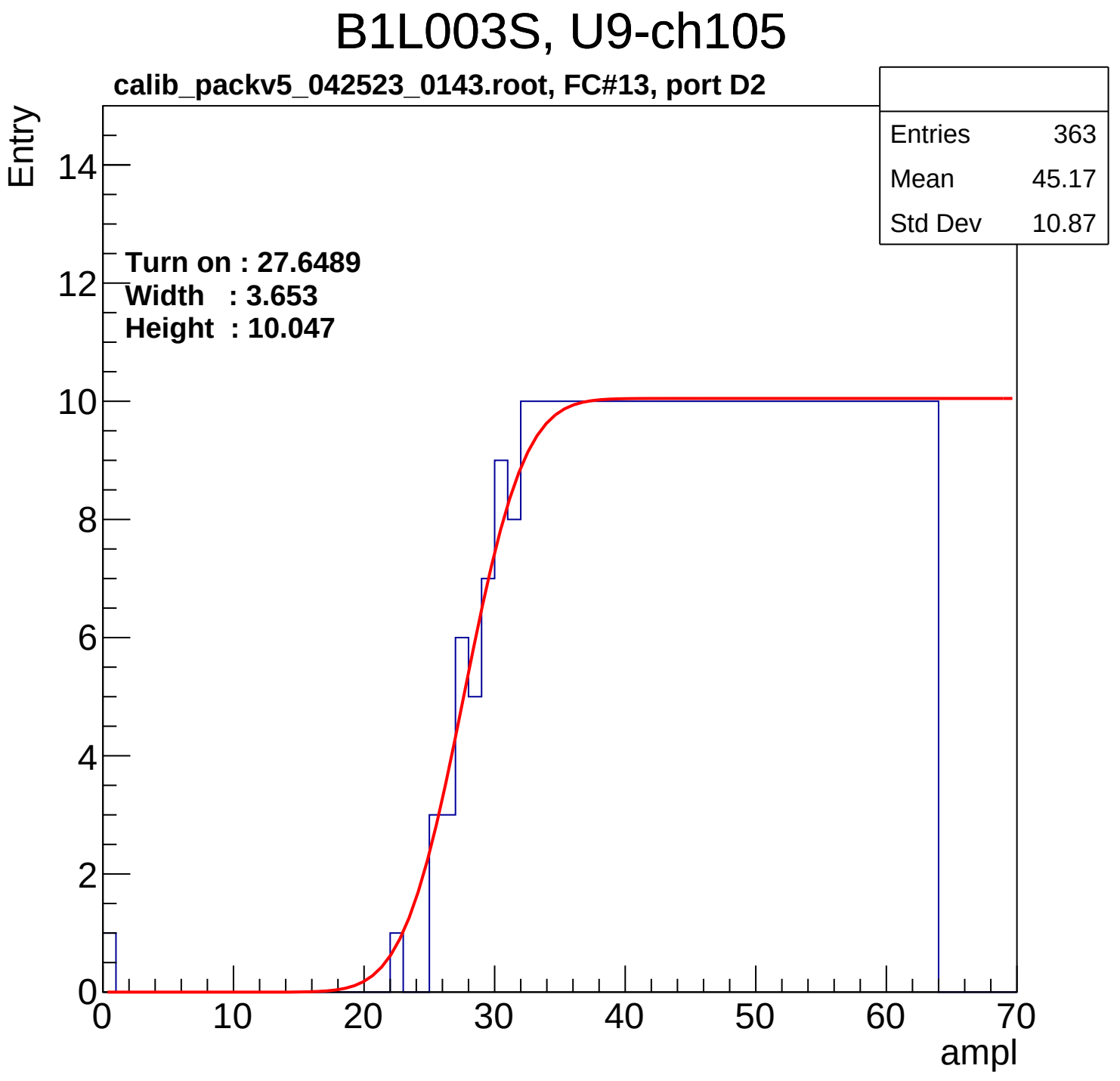

B1L003S, U9-ch100
calib_packv5_042523_0143.root, FC#13, port D2
Entries 365
Mean 44.99
Std Dev 11.15
Turn on : 27.9547
Width : 3.124
Height : 10.016
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

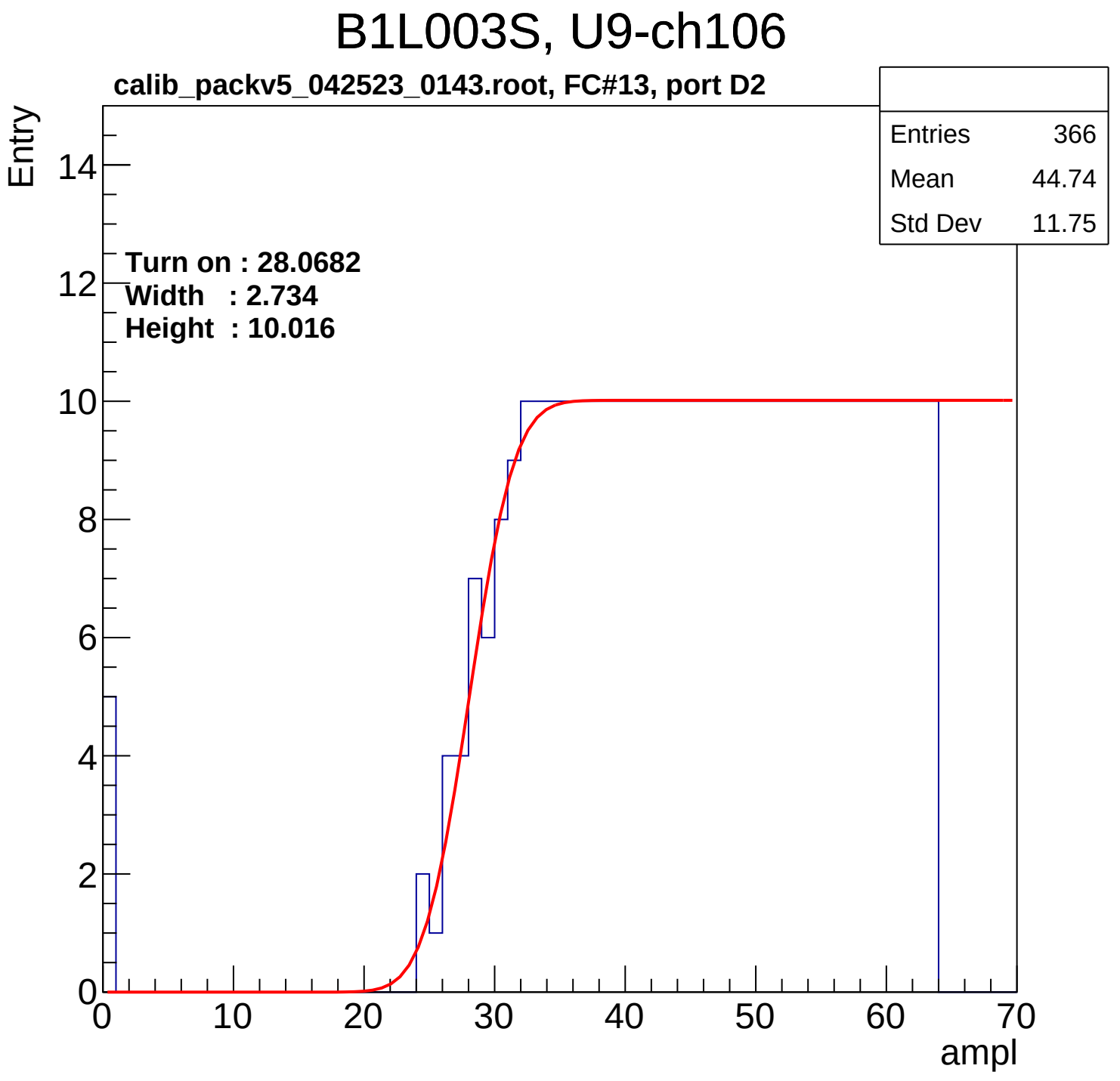

B1L003S, U9-ch101
calib_packv5_042523_0143.root, FC#13, port D2
Entries 374
Mean 44.45
Std Dev 11.61
Turn on : 27.2077
Width : 3.733
Height : 10.054
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

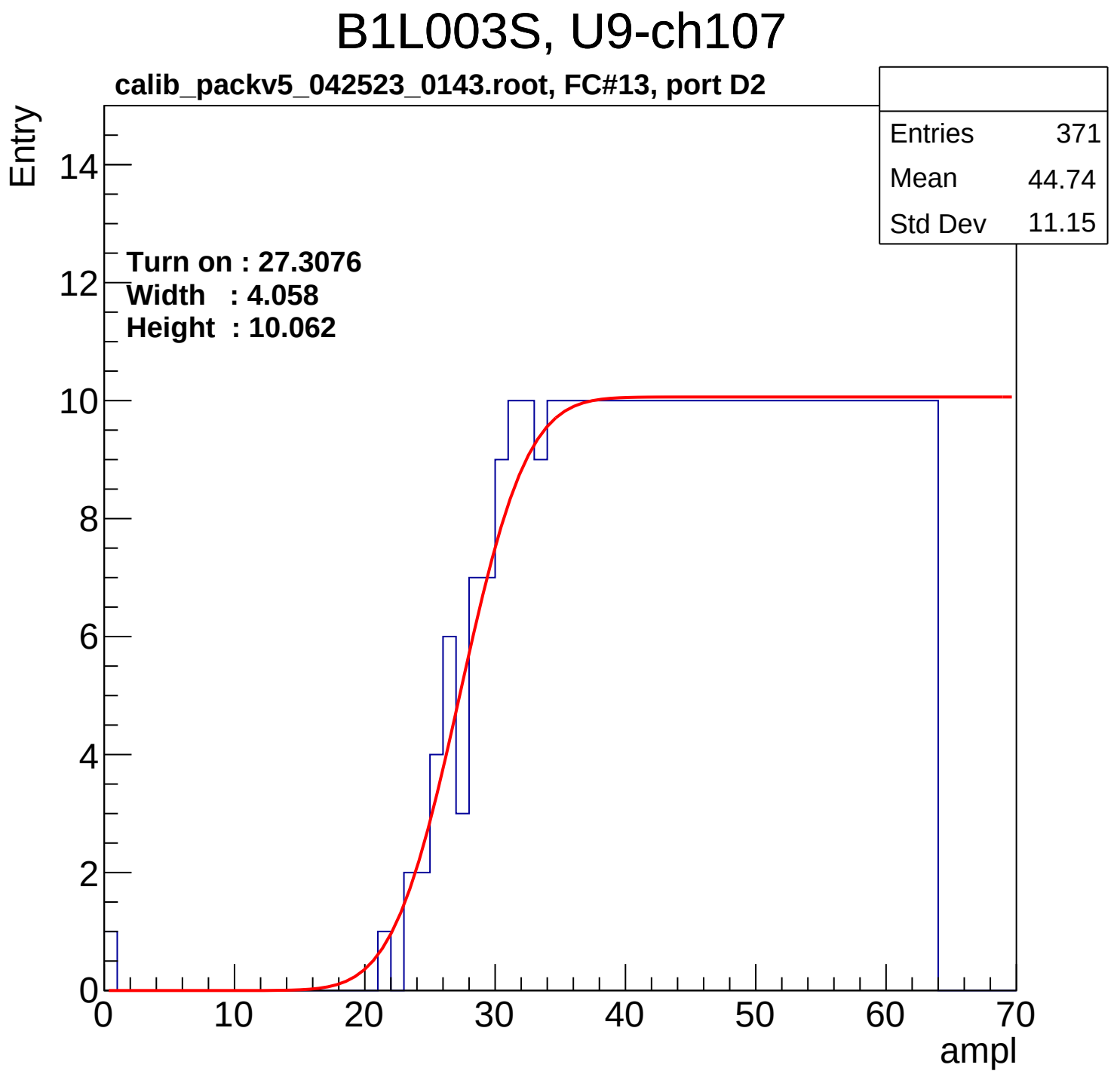

B1L003S, U9-ch102
calib_packv5_042523_0143.root, FC#13, port D2
Entries 355
Mean 45.6
Std Dev 10.6
Turn on : 28.7347
Width : 2.005
Height : 9.959
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

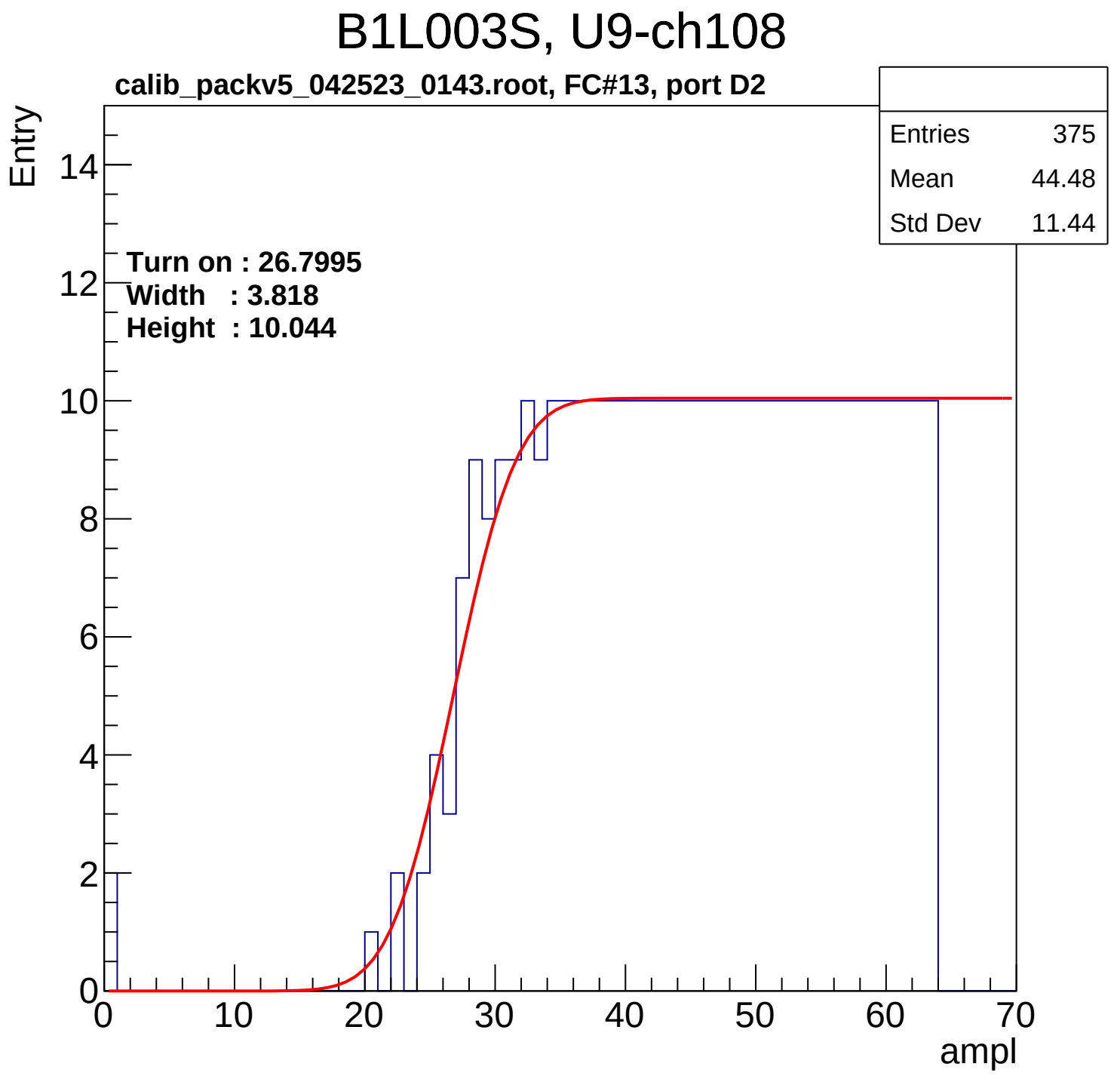

B1L003S, U9-ch103
calib_packv5_042523_0143.root, FC#13, port D2
Entries 371
Mean 44.65
Std Dev 11.46
Turn on : 26.9371
Width : 3.357
Height : 10.017
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

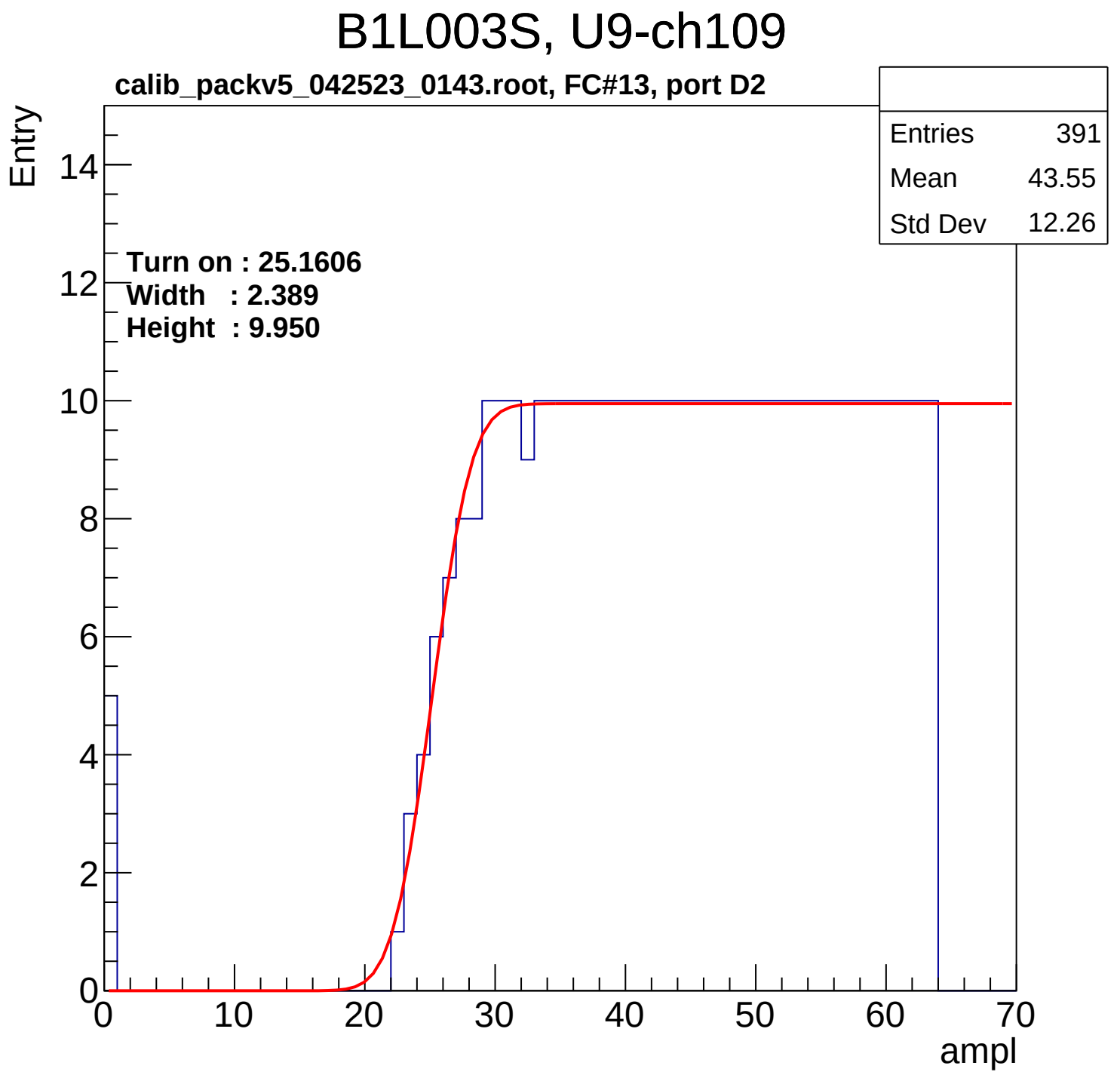

B1L003S, U9-ch104
calib_packv5_042523_0143.root, FC#13, port D2
Entries 386
Mean 43.75
Std Dev 12.29
Turn on : 26.7463
Width : 1.483
Height : 10.023
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

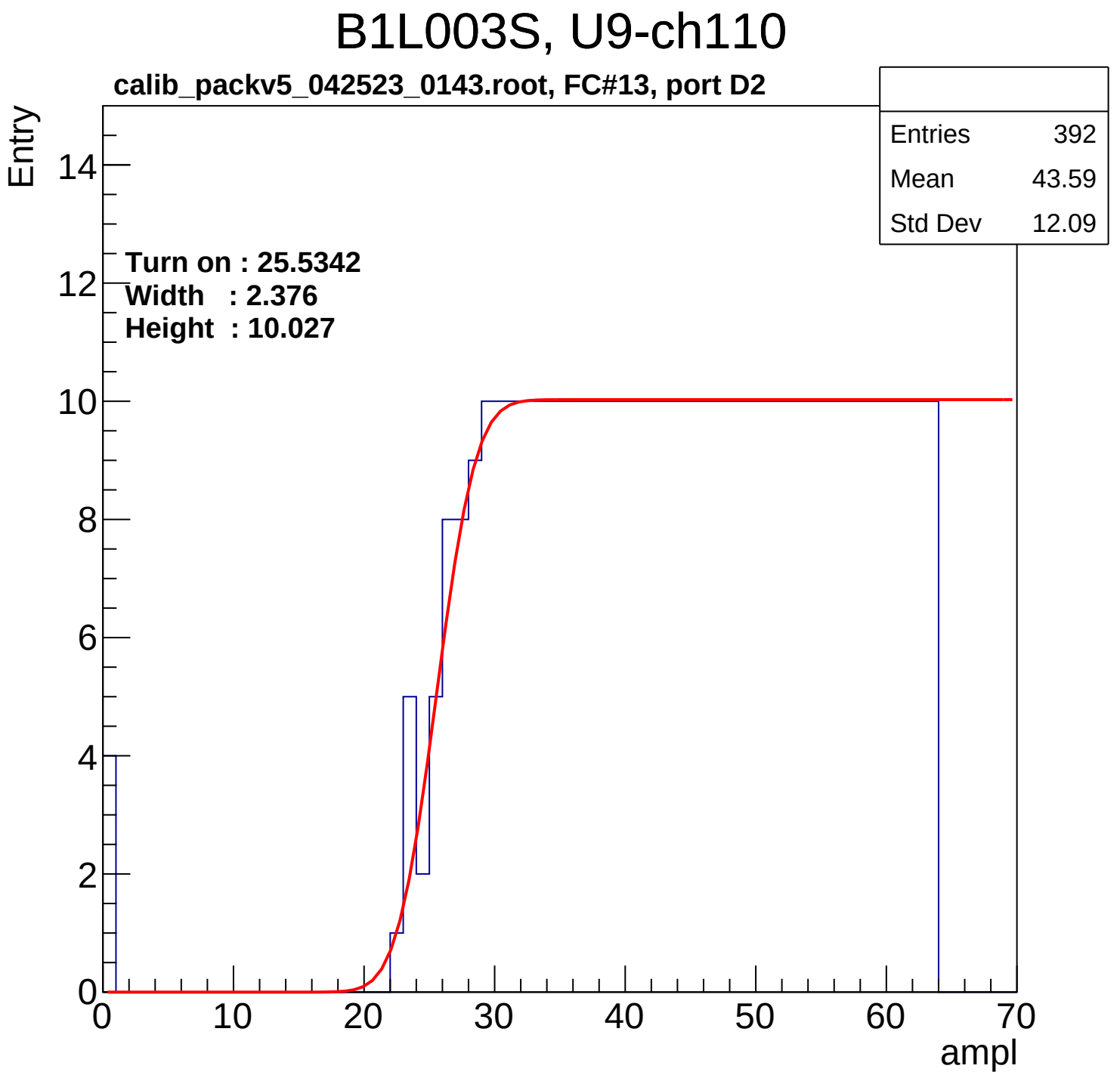

B1L003S, U9-ch105
calib_packv5_042523_0143.root, FC#13, port D2
Entries 363
Mean 45.17
Std Dev 10.87
Turn on : 27.6489
Width : 3.653
Height : 10.047
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

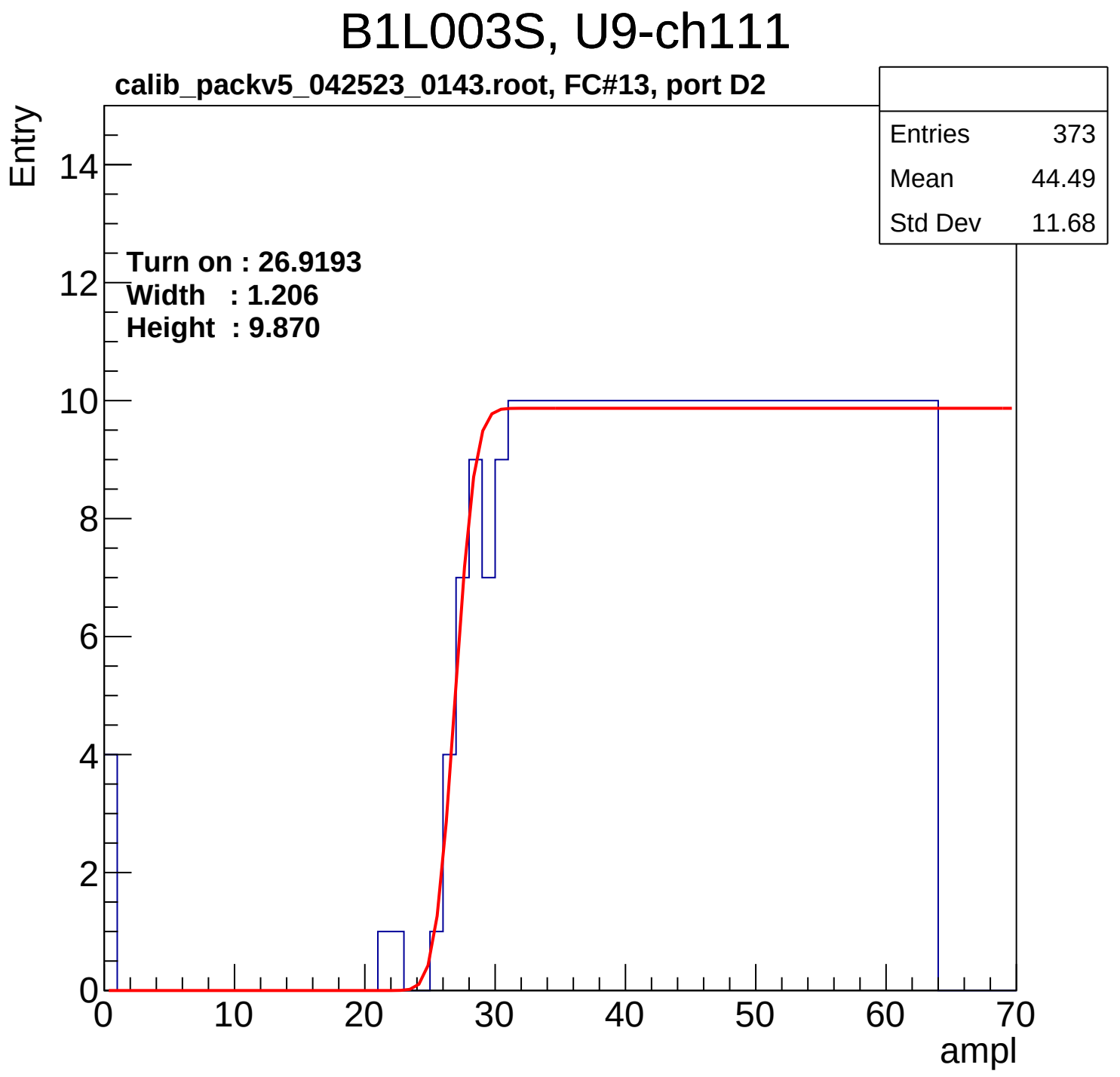

B1L003S, U9-ch106
calib_packv5_042523_0143.root, FC#13, port D2
Entries 366
Mean 44.74
Std Dev 11.75
Turn on : 28.0682
Width : 2.734
Height : 10.016
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

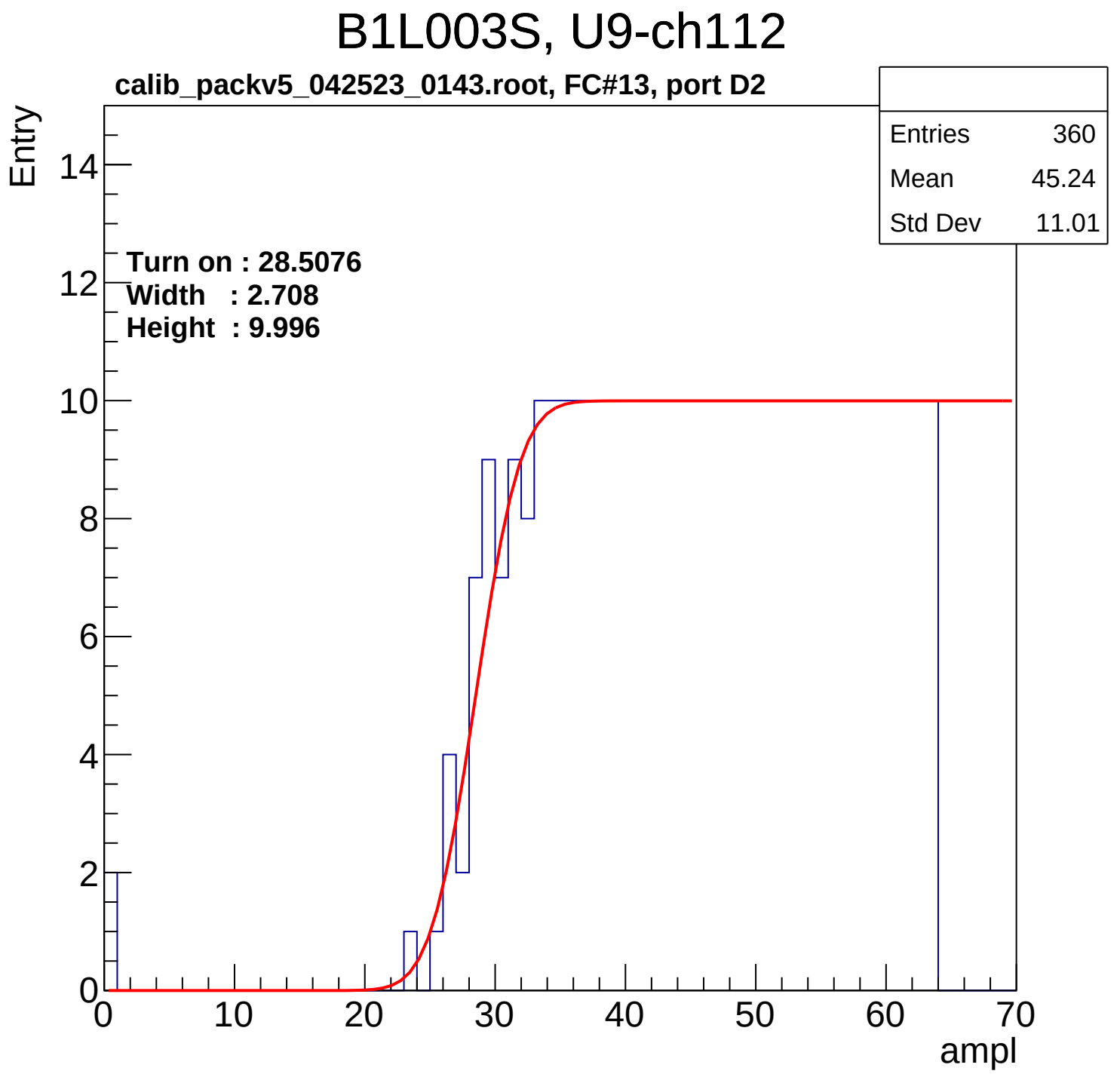

B1L003S, U9-ch107
calib_packv5_042523_0143.root, FC#13, port D2
Entries 371
Mean 44.74
Std Dev 11.15
Turn on : 27.3076
Width : 4.058
Height : 10.062
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

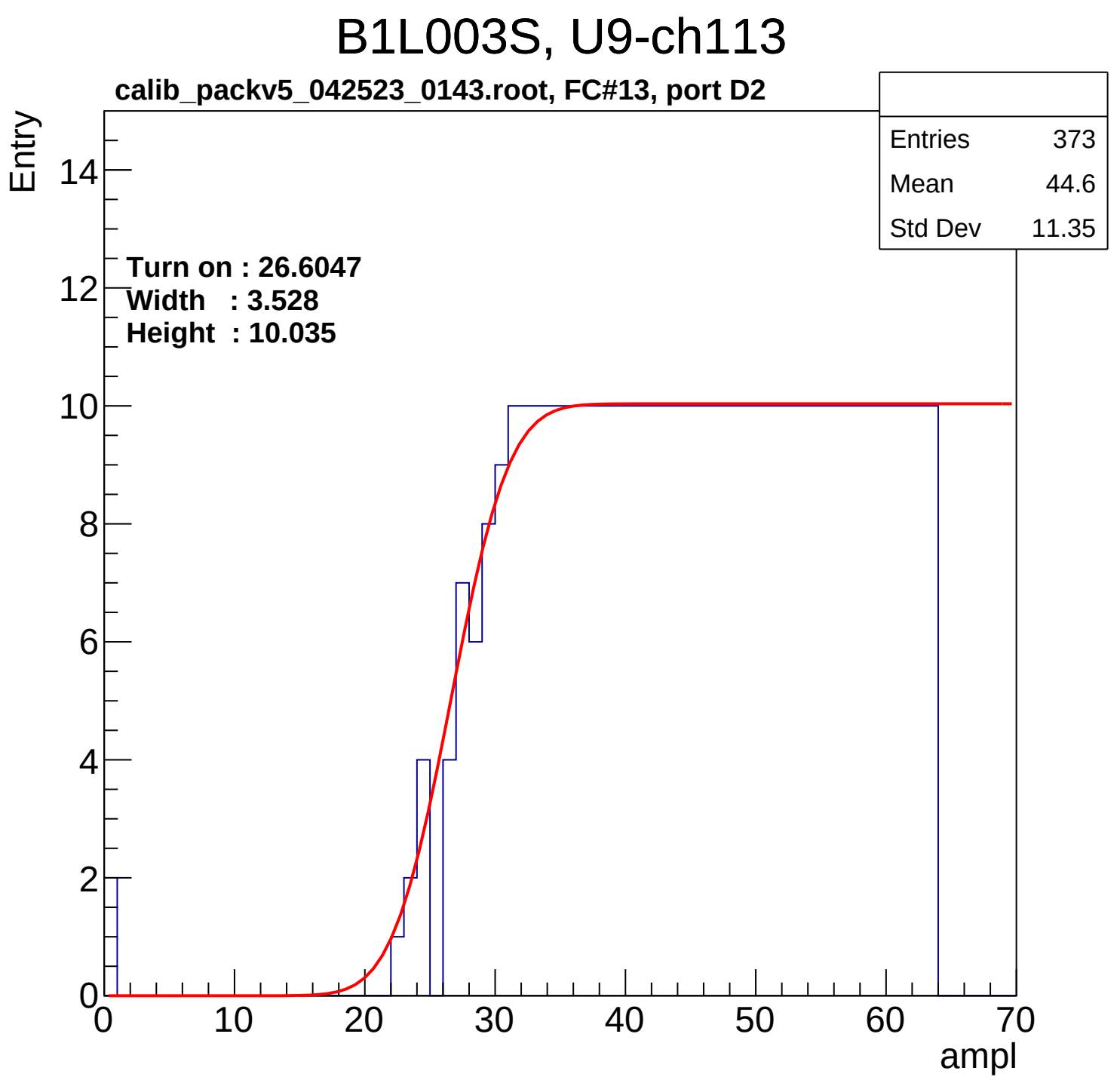

B1L003S, U9-ch108
calib_packv5_042523_0143.root, FC#13, port D2
Entries 375
Mean 44.48
Std Dev 11.44
Turn on : 26.7995
Width : 3.818
Height : 10.044
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

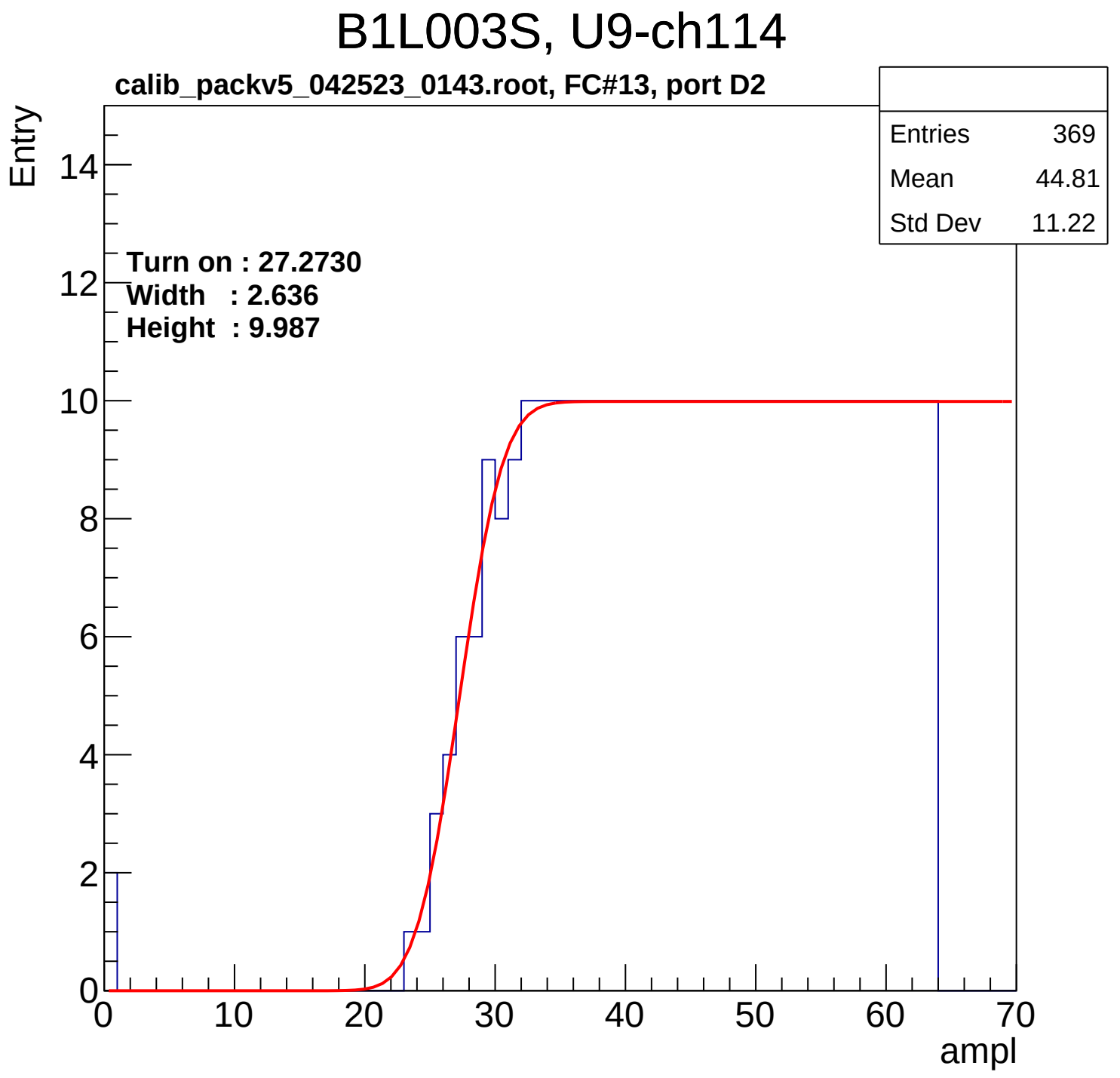

B1L003S, U9-ch109
calib_packv5_042523_0143.root, FC#13, port D2
Entries 391
Mean 43.55
Std Dev 12.26
Turn on : 25.1606
Width : 2.389
Height : 9.950
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

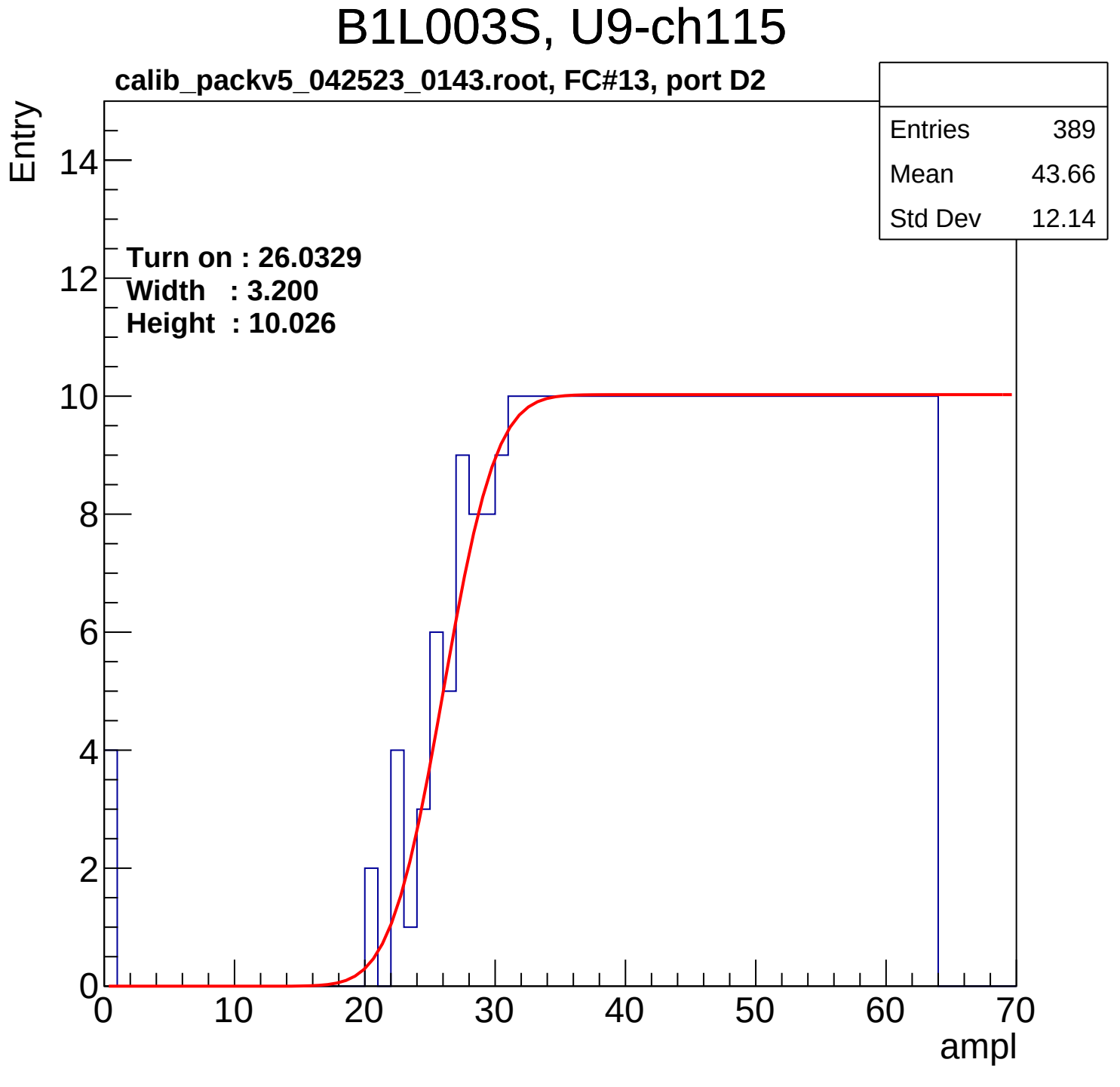

B1L003S, U9-ch110
calib_packv5_042523_0143.root, FC#13, port D2
Entries 392
Mean 43.59
Std Dev 12.09
Turn on : 25.5342
Width : 2.376
Height : 10.027
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

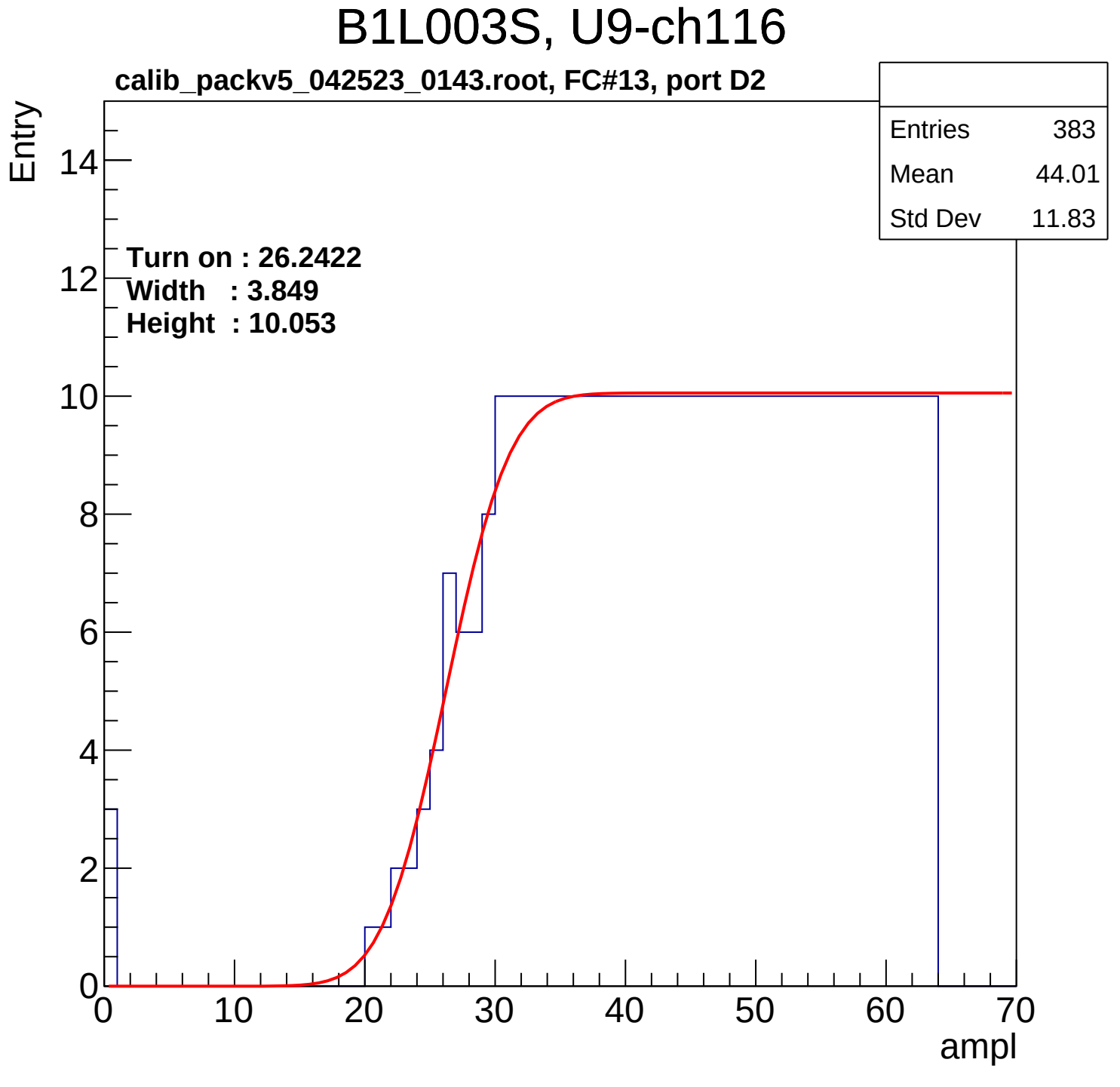

B1L003S, U9-ch111
calib_packv5_042523_0143.root, FC#13, port D2
Entries 373
Mean 44.49
Std Dev 11.68
Turn on : 26.9193
Width : 1.206
Height : 9.870
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

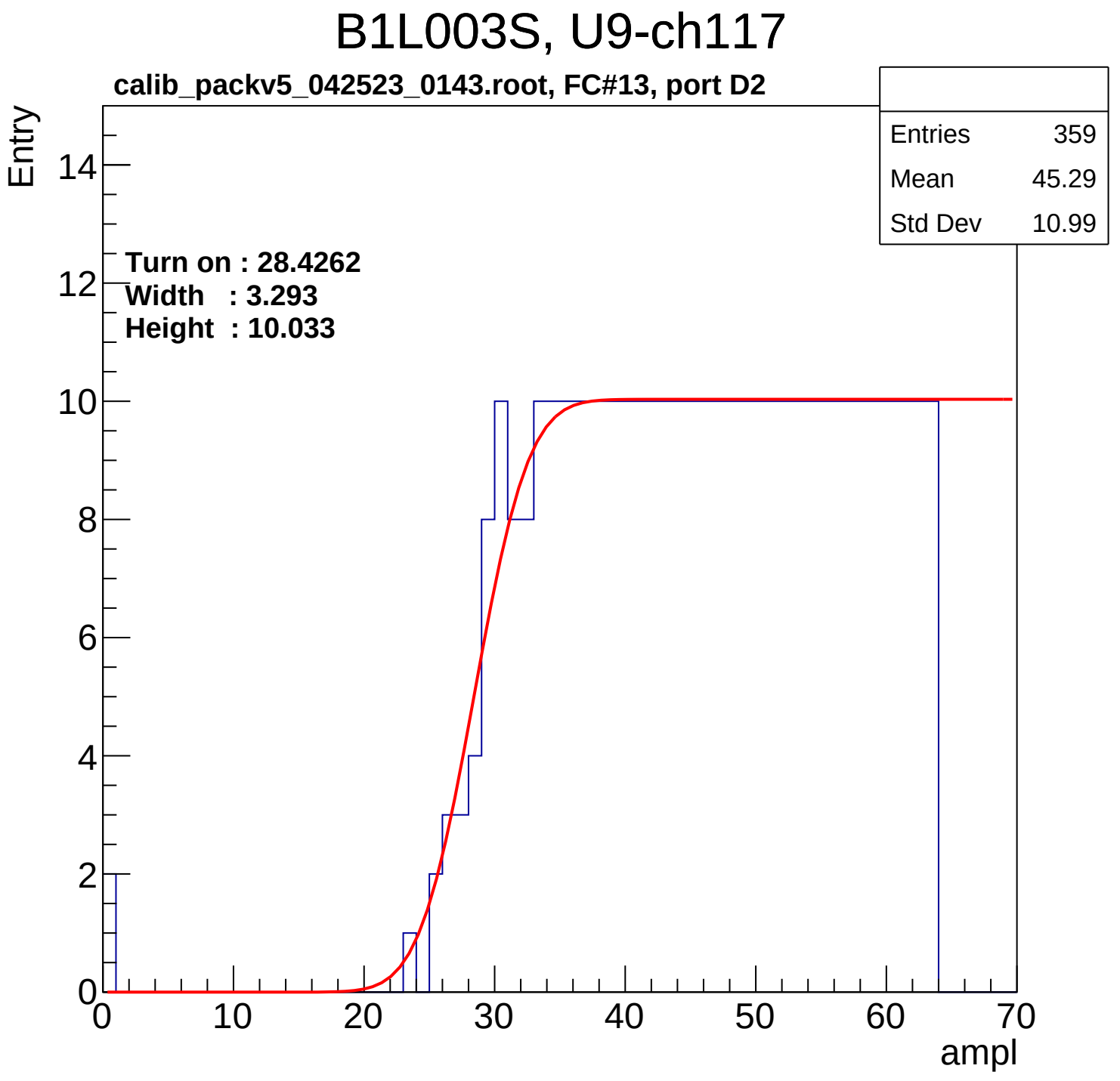

B1L003S, U9-ch112
calib_packv5_042523_0143.root, FC#13, port D2
Entries 360
Mean 45.24
Std Dev 11.01
Turn on : 28.5076
Width : 2.708
Height : 9.996
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

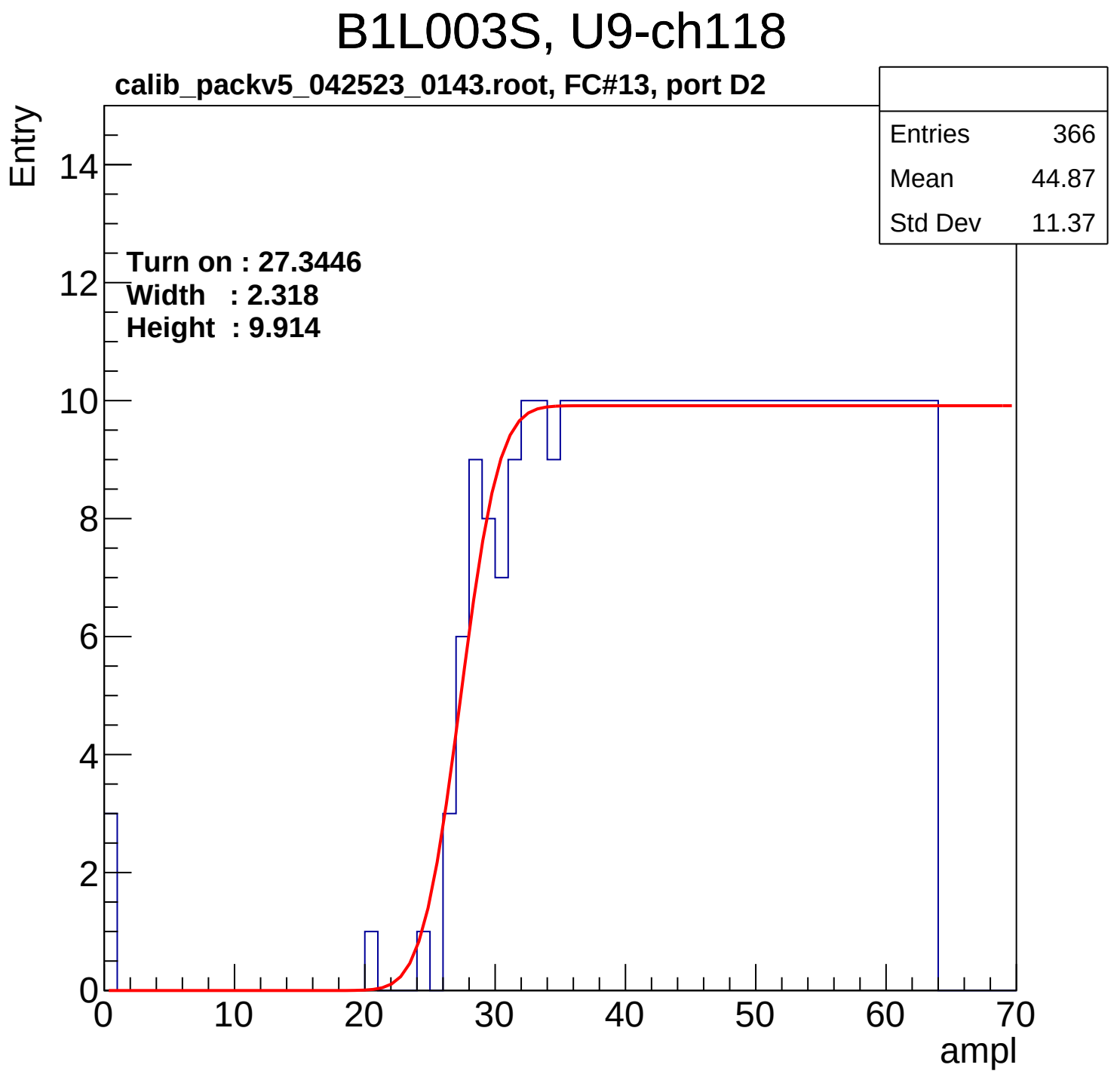

B1L003S, U9-ch113
calib_packv5_042523_0143.root, FC#13, port D2
Entries 373
Mean 44.6
Std Dev 11.35
Turn on : 26.6047
Width : 3.528
Height : 10.035
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

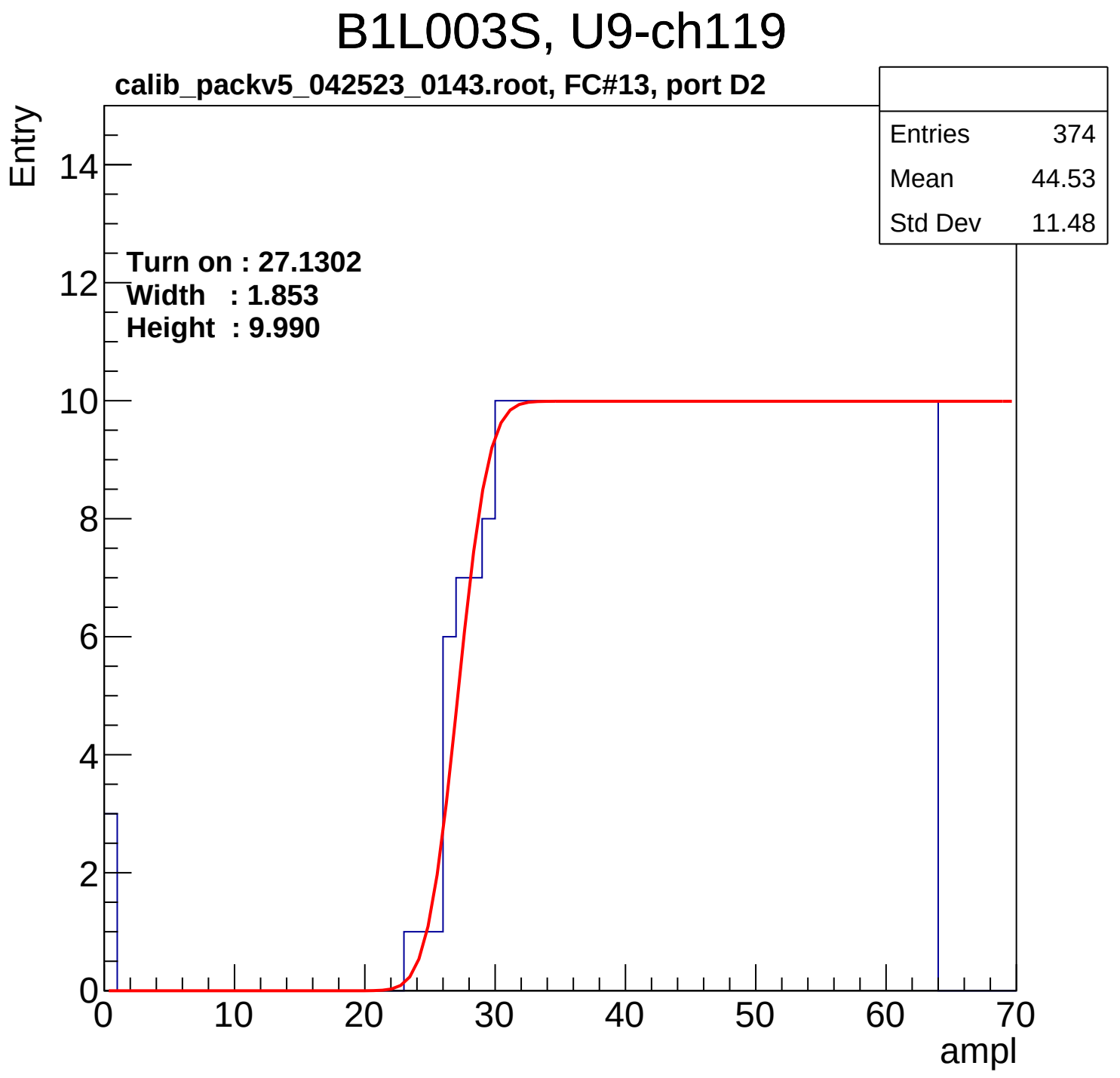

B1L003S, U9-ch114
calib_packv5_042523_0143.root, FC#13, port D2
Entries 369
Mean 44.81
Std Dev 11.22
Turn on : 27.2730
Width : 2.636
Height : 9.987
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

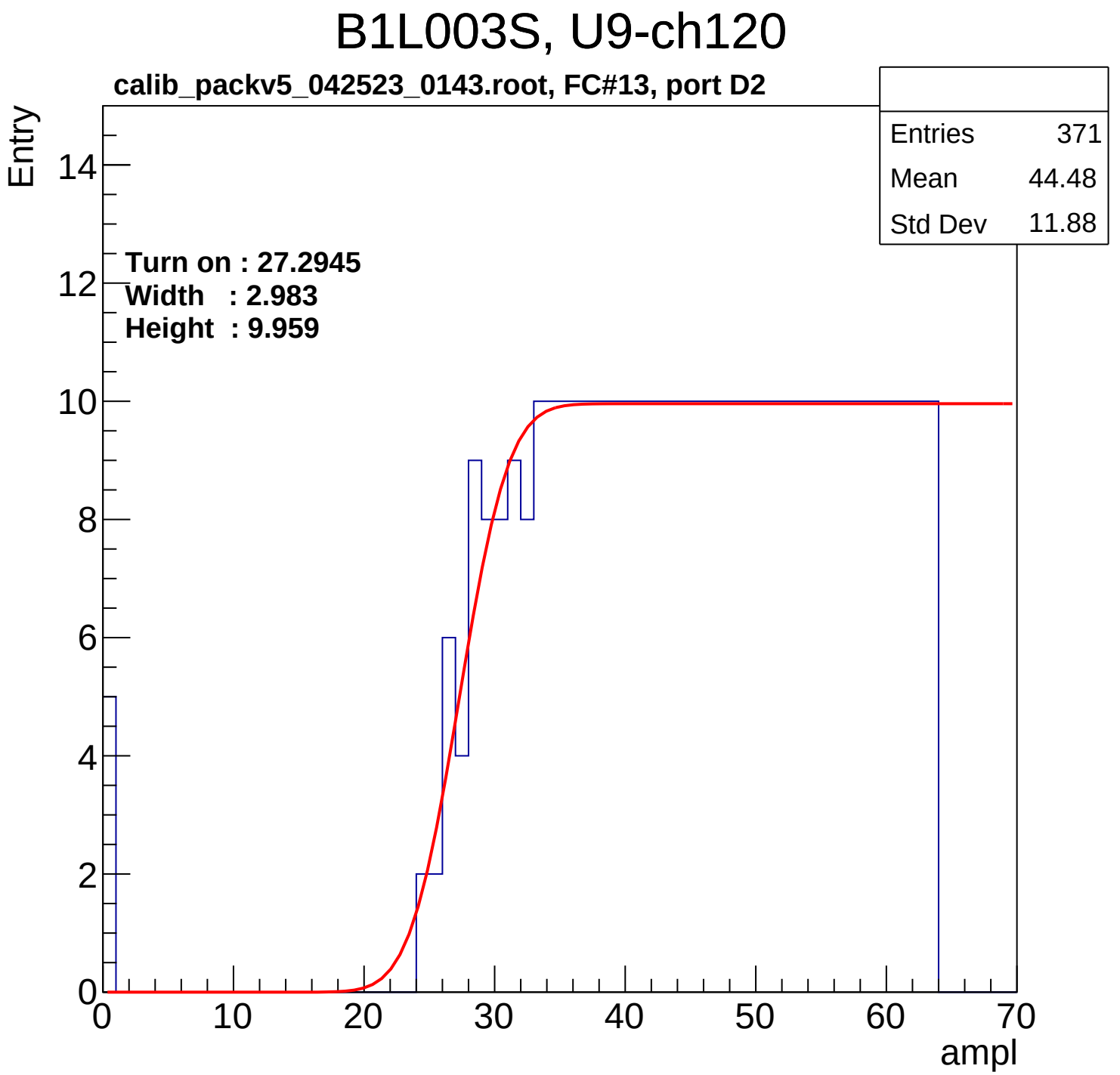

B1L003S, U9-ch115
calib_packv5_042523_0143.root, FC#13, port D2
Entries 389
Mean 43.66
Std Dev 12.14
Turn on : 26.0329
Width : 3.200
Height : 10.026
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

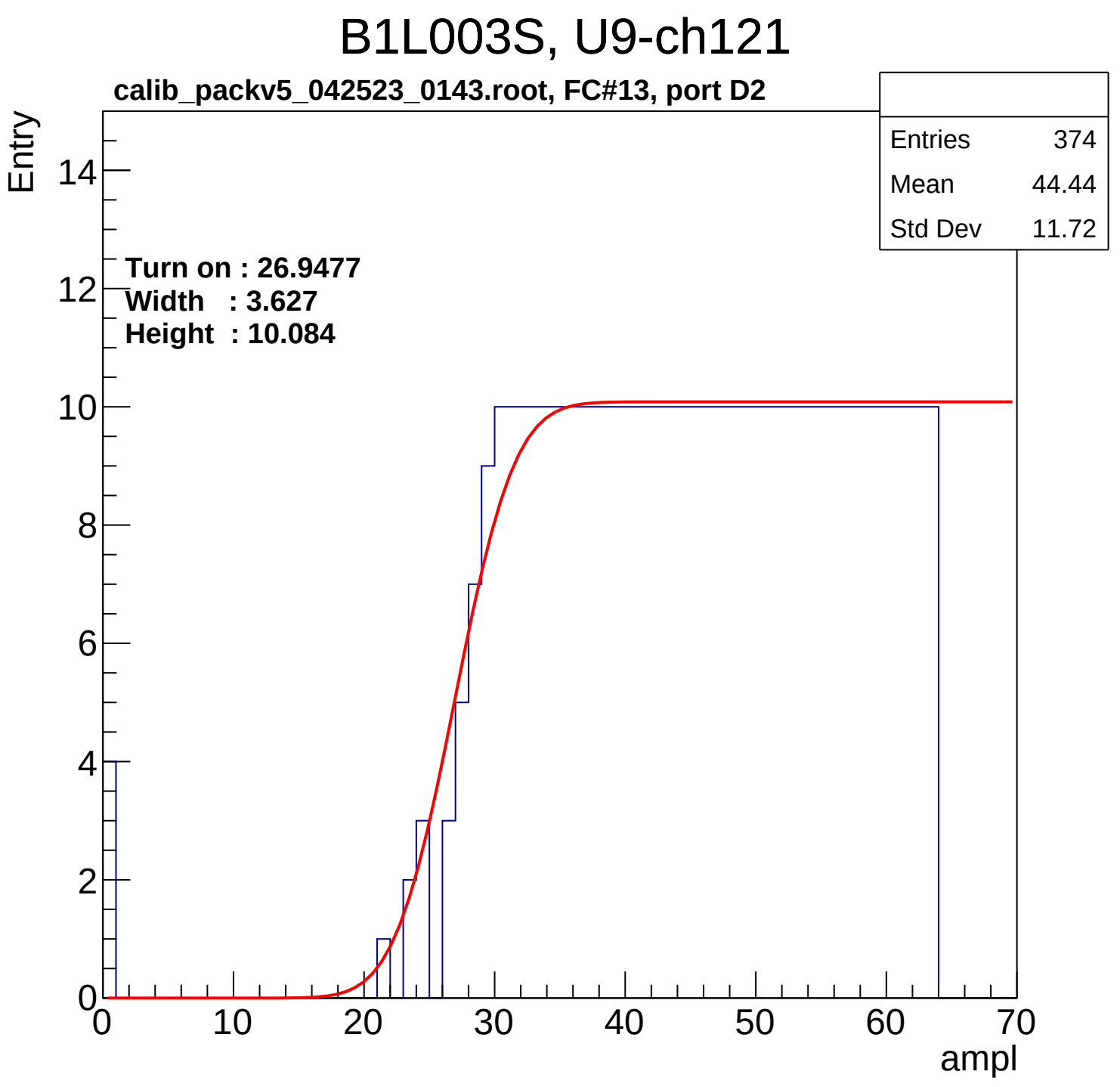

B1L003S, U9-ch116
calib_packv5_042523_0143.root, FC#13, port D2
Entries 383
Mean 44.01
Std Dev 11.83
Turn on : 26.2422
Width : 3.849
Height : 10.053
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

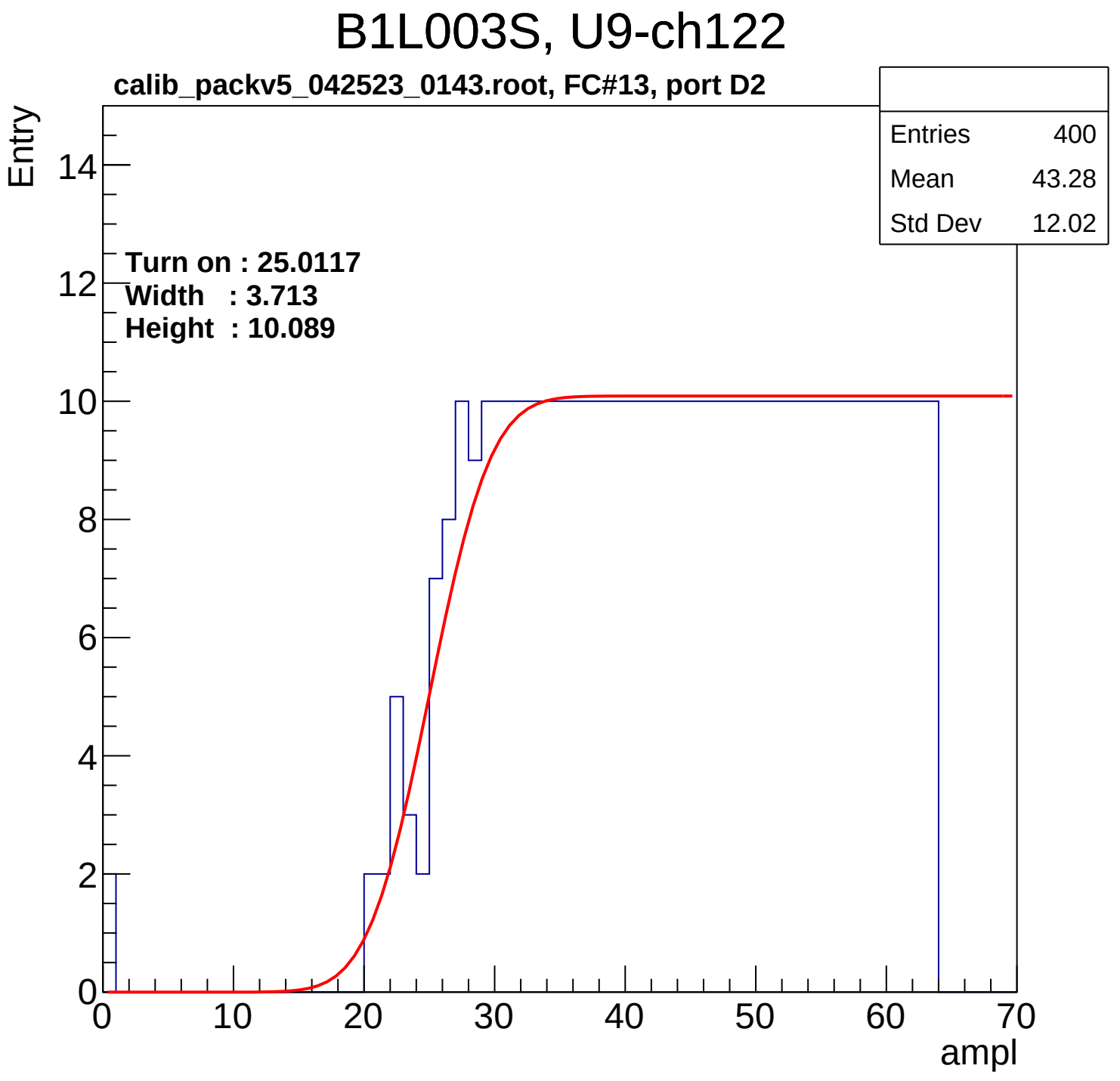

B1L003S, U9-ch117
calib_packv5_042523_0143.root, FC#13, port D2
Entries 359
Mean 45.29
Std Dev 10.99
Turn on : 28.4262
Width : 3.293
Height : 10.033
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

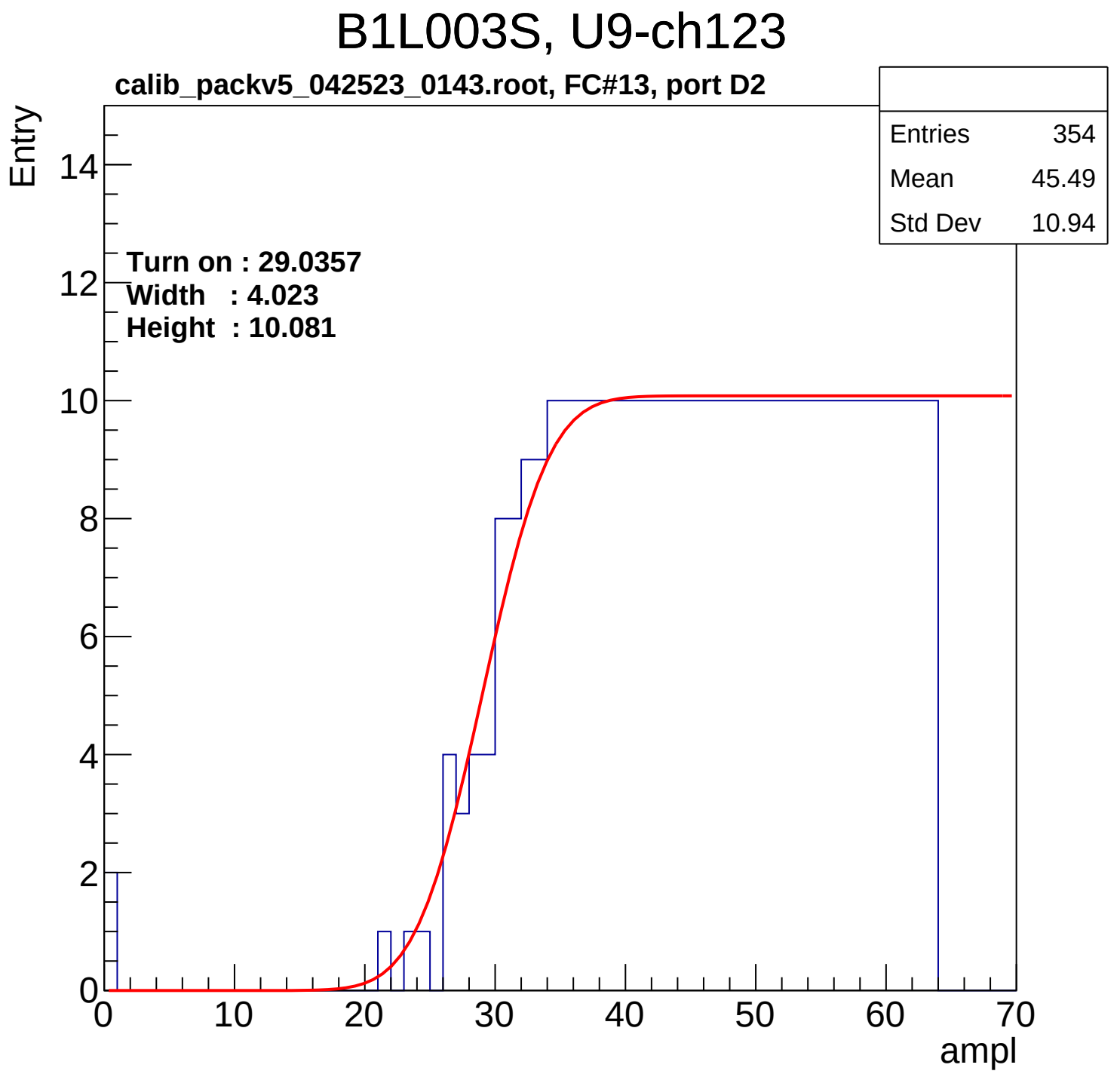

B1L003S, U9-ch118
calib_packv5_042523_0143.root, FC#13, port D2
Entries 366
Mean 44.87
Std Dev 11.37
Turn on : 27.3446
Width : 2.318
Height : 9.914
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

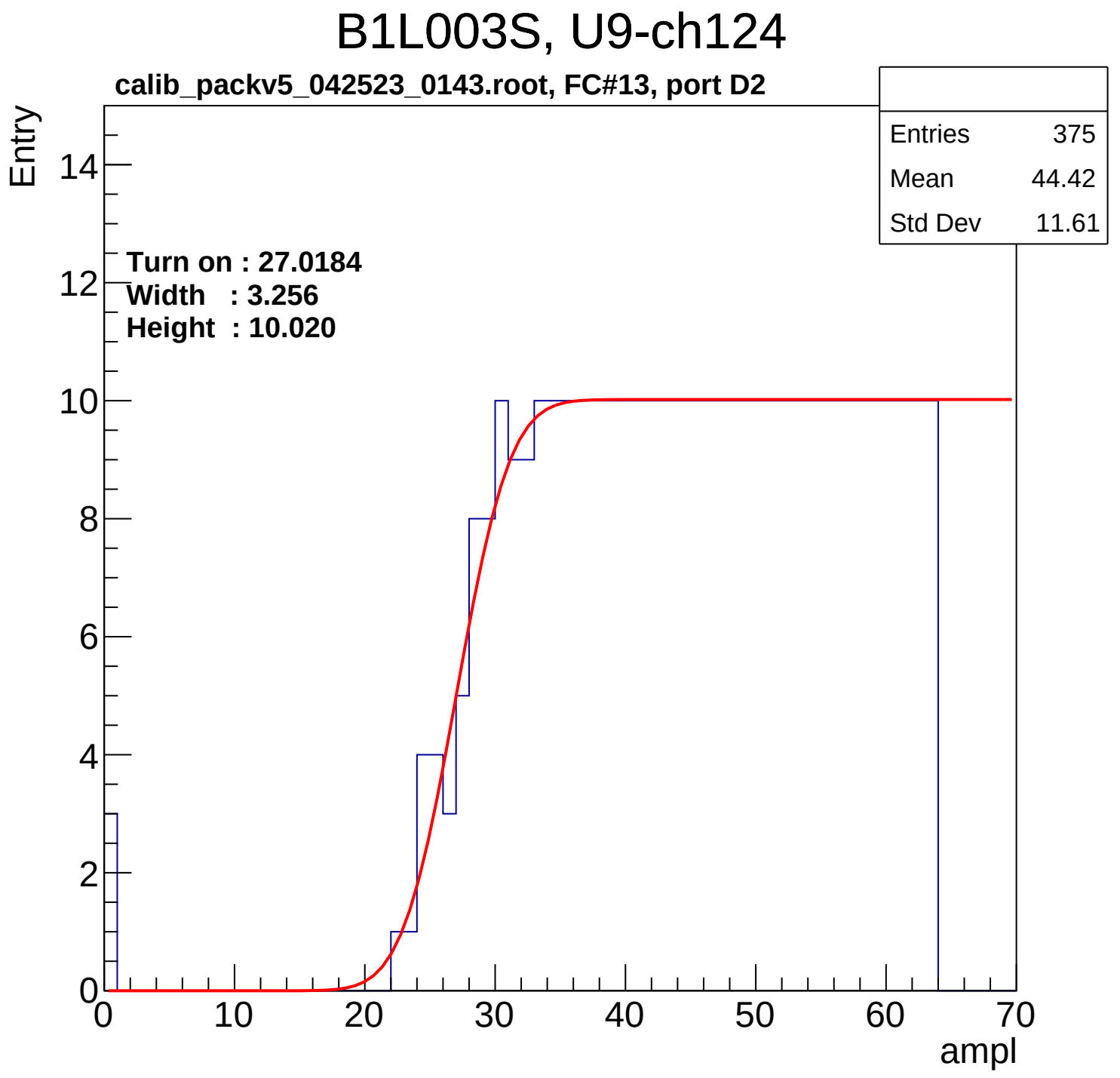

B1L003S, U9-ch119
calib_packv5_042523_0143.root, FC#13, port D2
Entries 374
Mean 44.53
Std Dev 11.48
Turn on : 27.1302
Width : 1.853
Height : 9.990
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

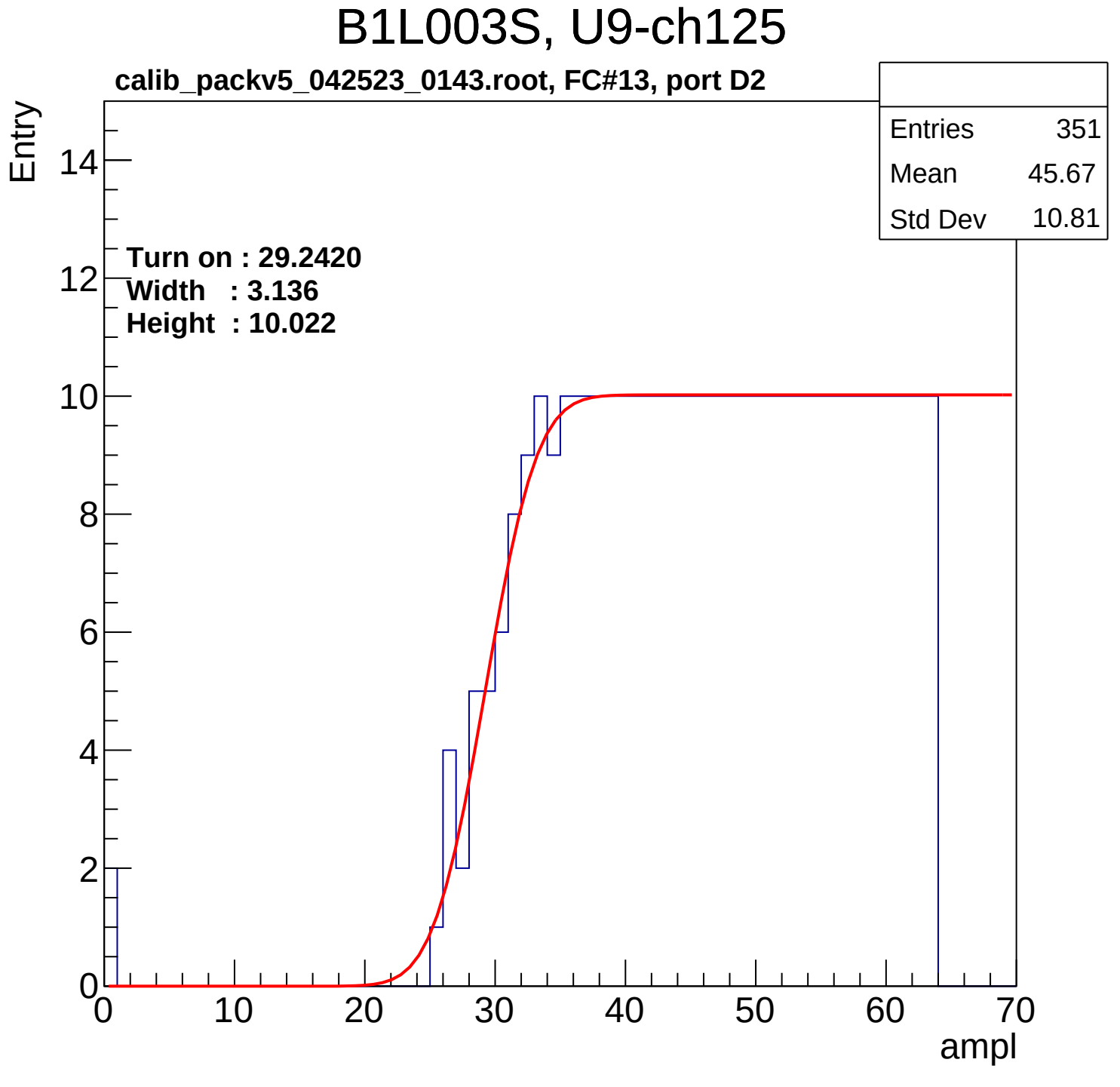

B1L003S, U9-ch120
calib_packv5_042523_0143.root, FC#13, port D2
Entries 371
Mean 44.48
Std Dev 11.88
Turn on : 27.2945
Width : 2.983
Height : 9.959
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

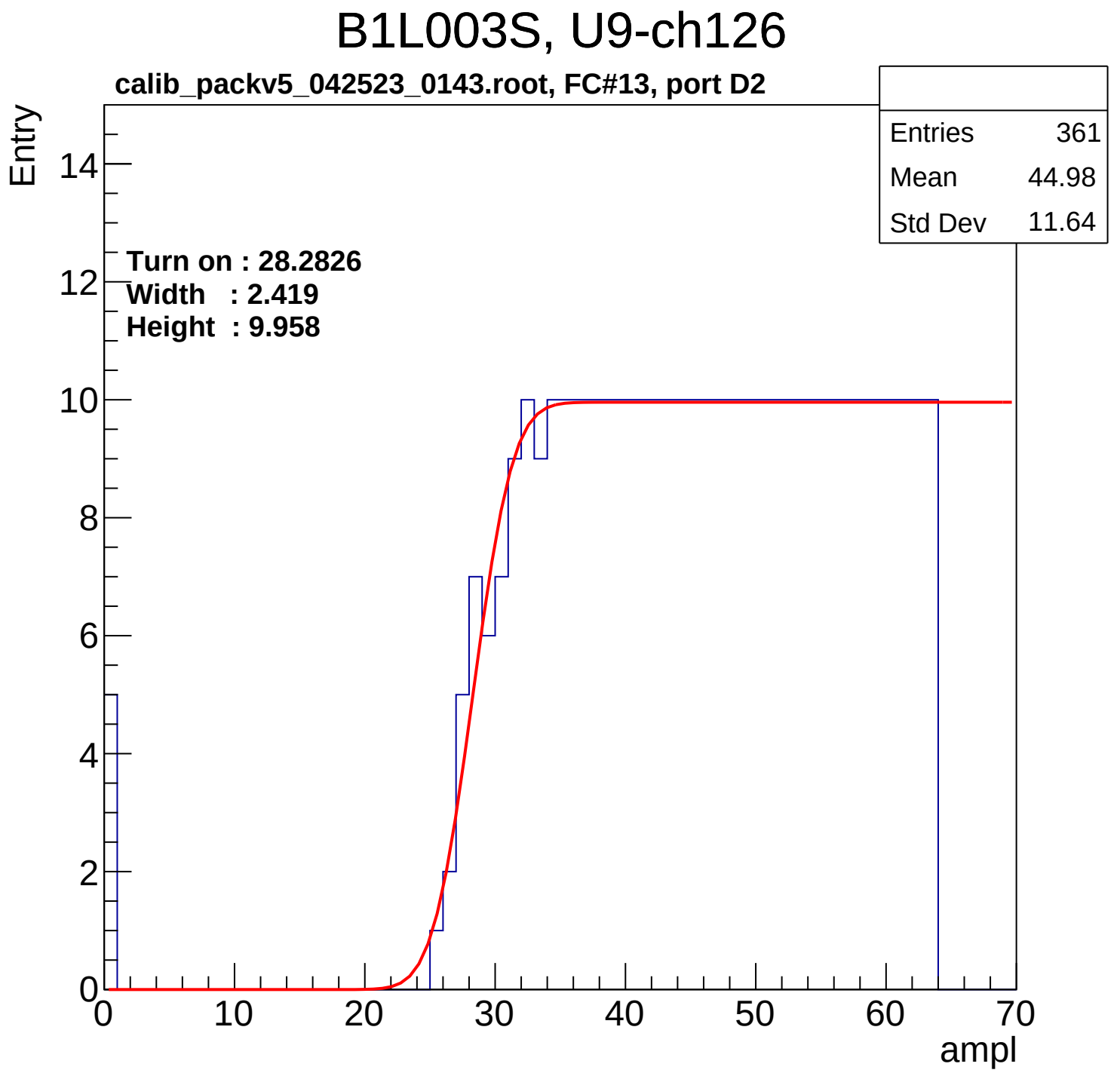

B1L003S, U9-ch121
calib_packv5_042523_0143.root, FC#13, port D2
Entries 374
Mean 44.44
Std Dev 11.72
Turn on : 26.9477
Width : 3.627
Height : 10.084
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

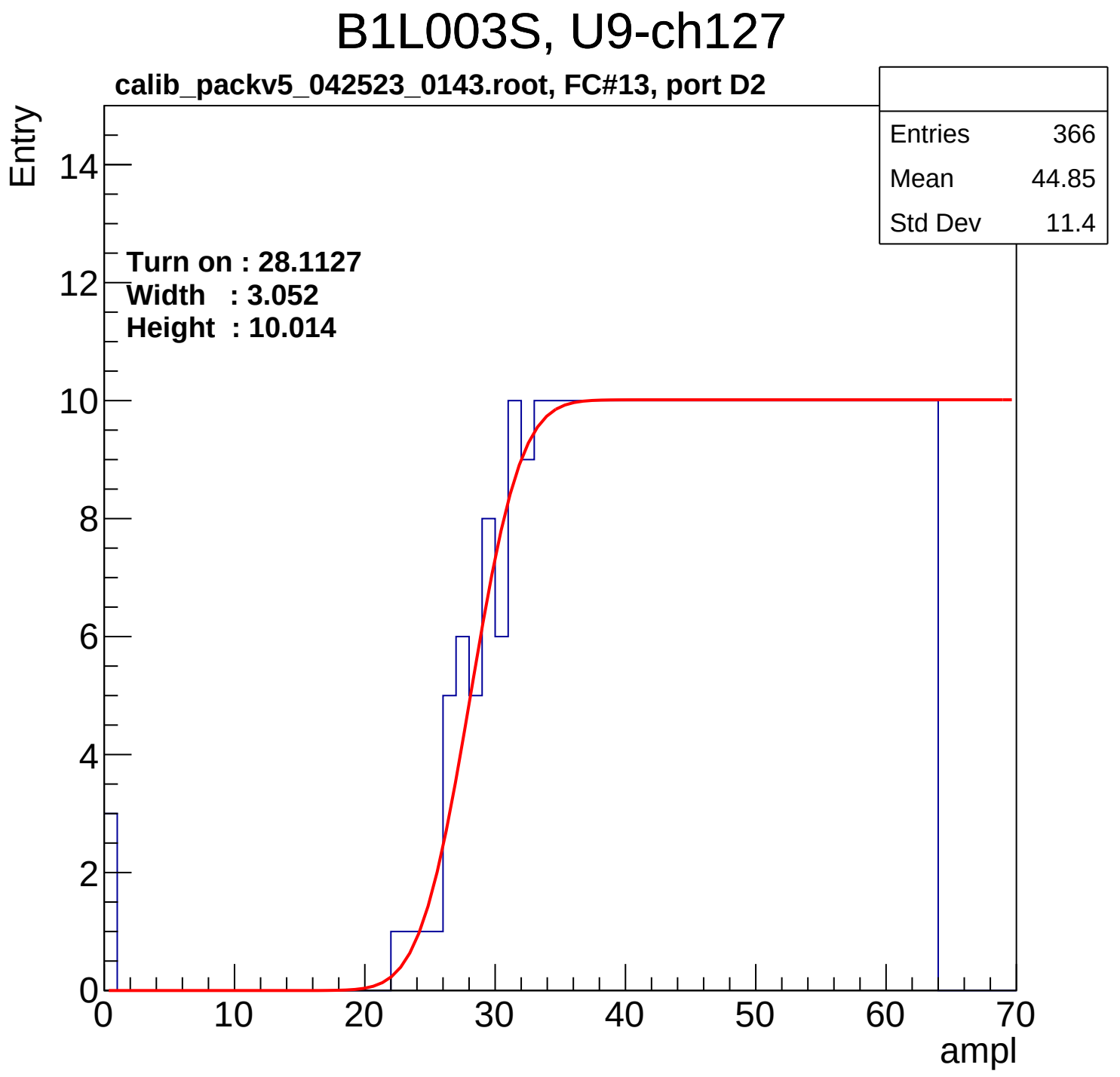

B1L003S, U9-ch122
calib_packv5_042523_0143.root, FC#13, port D2
Entries 400
Mean 43.28
Std Dev 12.02
Turn on : 25.0117
Width : 3.713
Height : 10.089
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

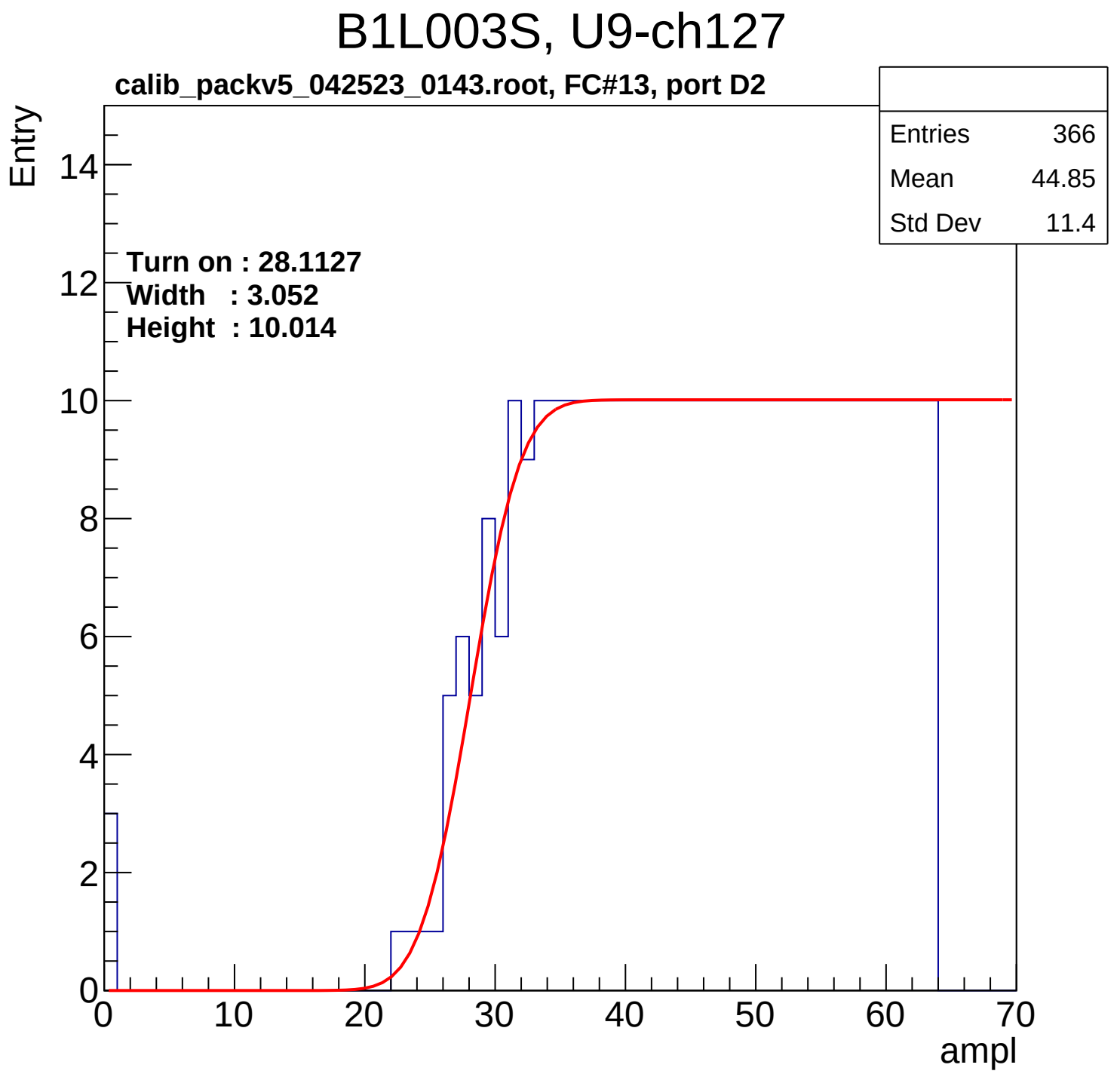

B1L003S, U9-ch123
calib_packv5_042523_0143.root, FC#13, port D2
Entries 354
Mean 45.49
Std Dev 10.94
Turn on : 29.0357
Width : 4.023
Height : 10.081
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L003S, U9-ch124
calib_packv5_042523_0143.root, FC#13, port D2
Entries 375
Mean 44.42
Std Dev 11.61
Turn on : 27.0184
Width : 3.256
Height : 10.020
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L003S, U9-ch125
calib_packv5_042523_0143.root, FC#13, port D2
Entries 351
Mean 45.67
Std Dev 10.81
Turn on : 29.2420
Width : 3.136
Height : 10.022
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L003S, U9-ch126
calib_packv5_042523_0143.root, FC#13, port D2
Entries 361
Mean 44.98
Std Dev 11.64
Turn on : 28.2826
Width : 2.419
Height : 9.958
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L003S, U9-ch127
calib_packv5_042523_0143.root, FC#13, port D2
Entries 366
Mean 44.85
Std Dev 11.4
Turn on : 28.1127
Width : 3.052
Height : 10.014
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L003S, U9-ch127
calib_packv5_042523_0143.root, FC#13, port D2
Entries 366
Mean 44.85
Std Dev 11.4
Turn on : 28.1127
Width : 3.052
Height : 10.014
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70