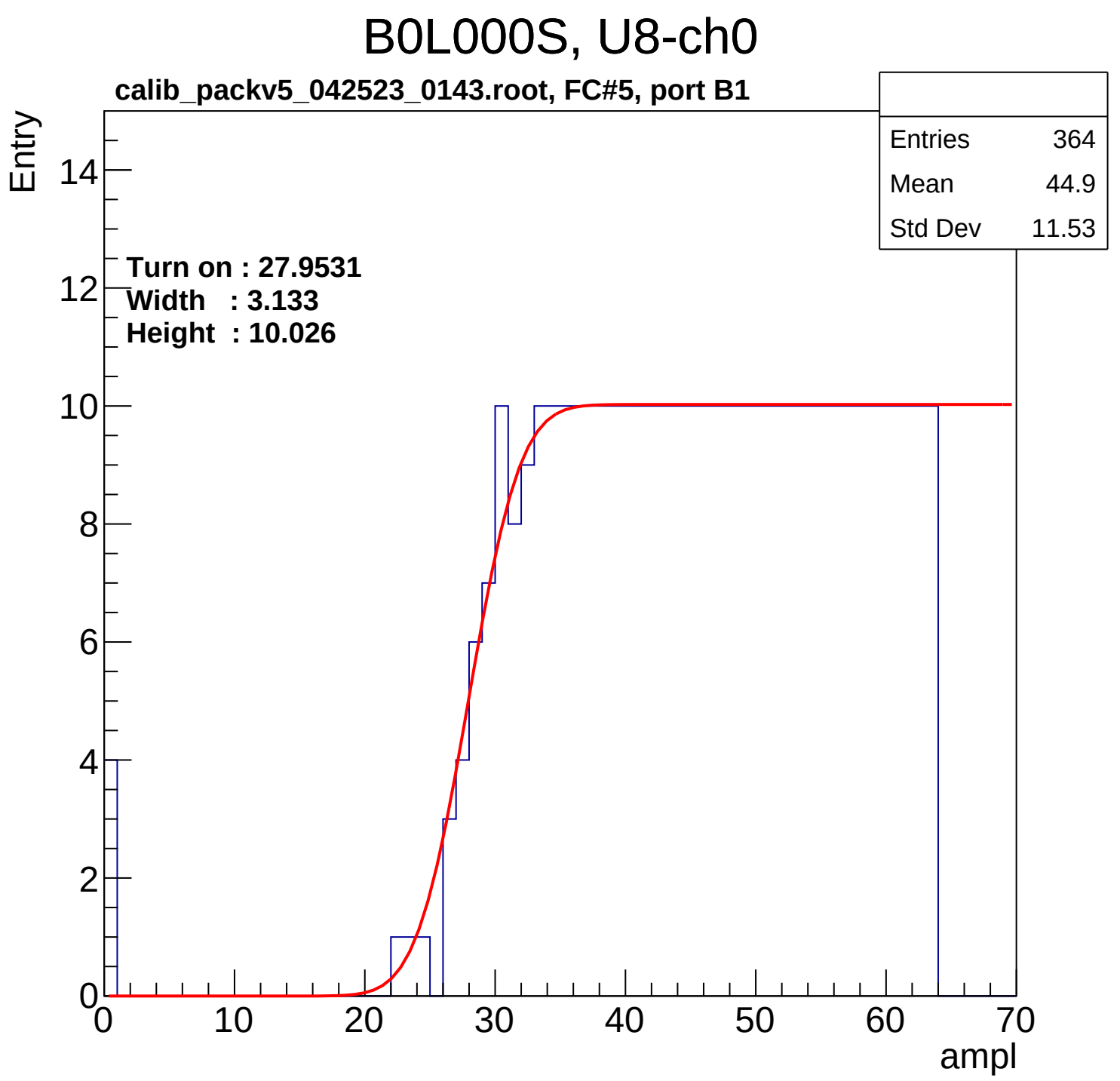
B0L000S, U8-ch0
calib_packv5_042523_0143.root, FC#5, port B1
Entries 364
Mean 44.9
Std Dev 11.53
Turn on : 27.9531
Width : 3.133
Height : 10.026
Entry
ampl
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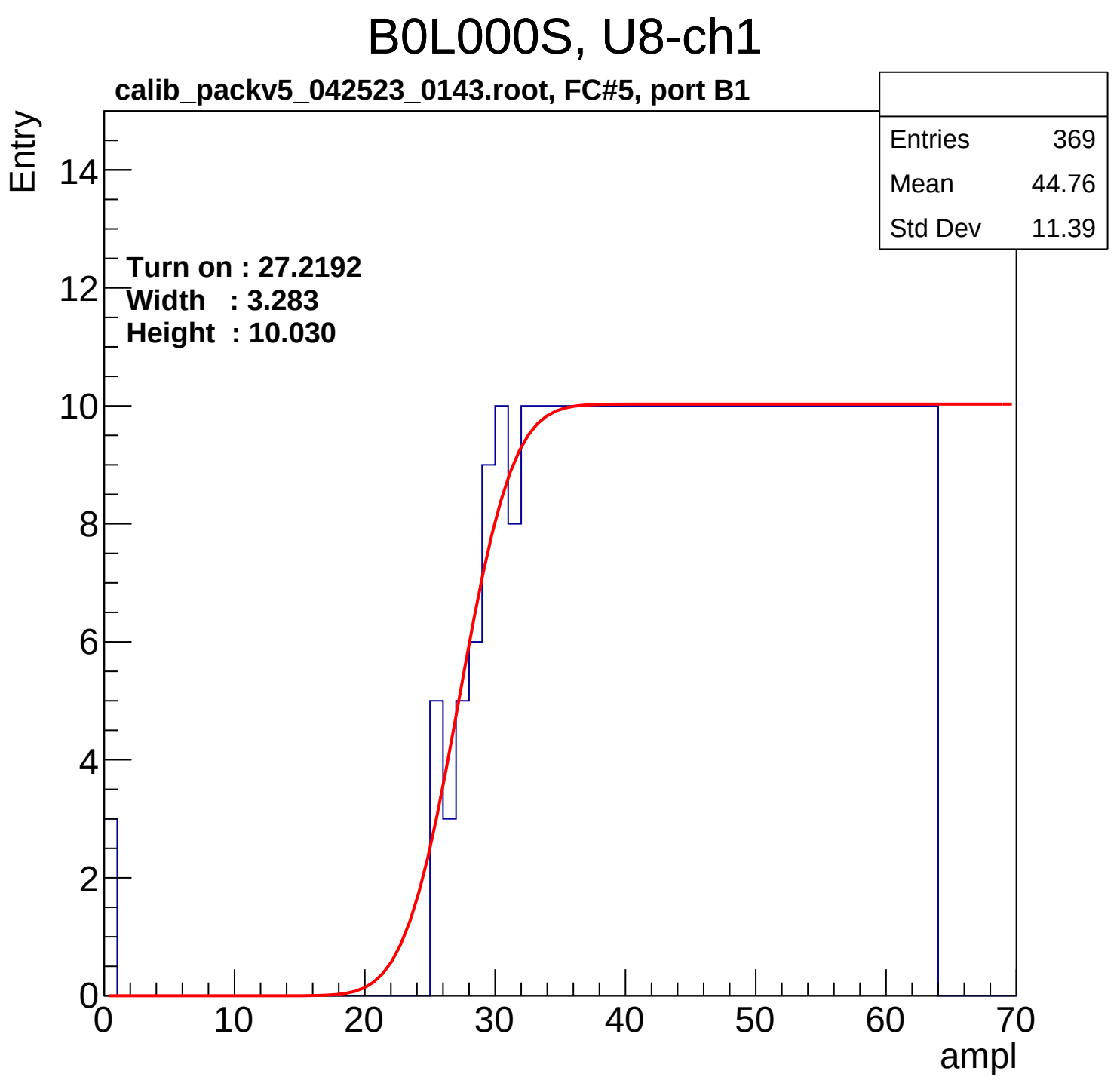
B0L000S, U8-ch1
calib_packv5_042523_0143.root, FC#5, port B1
Entries 369
Mean 44.76
Std Dev 11.39
Turn on : 27.2192
Width : 3.283
Height : 10.030
Entry
ampl
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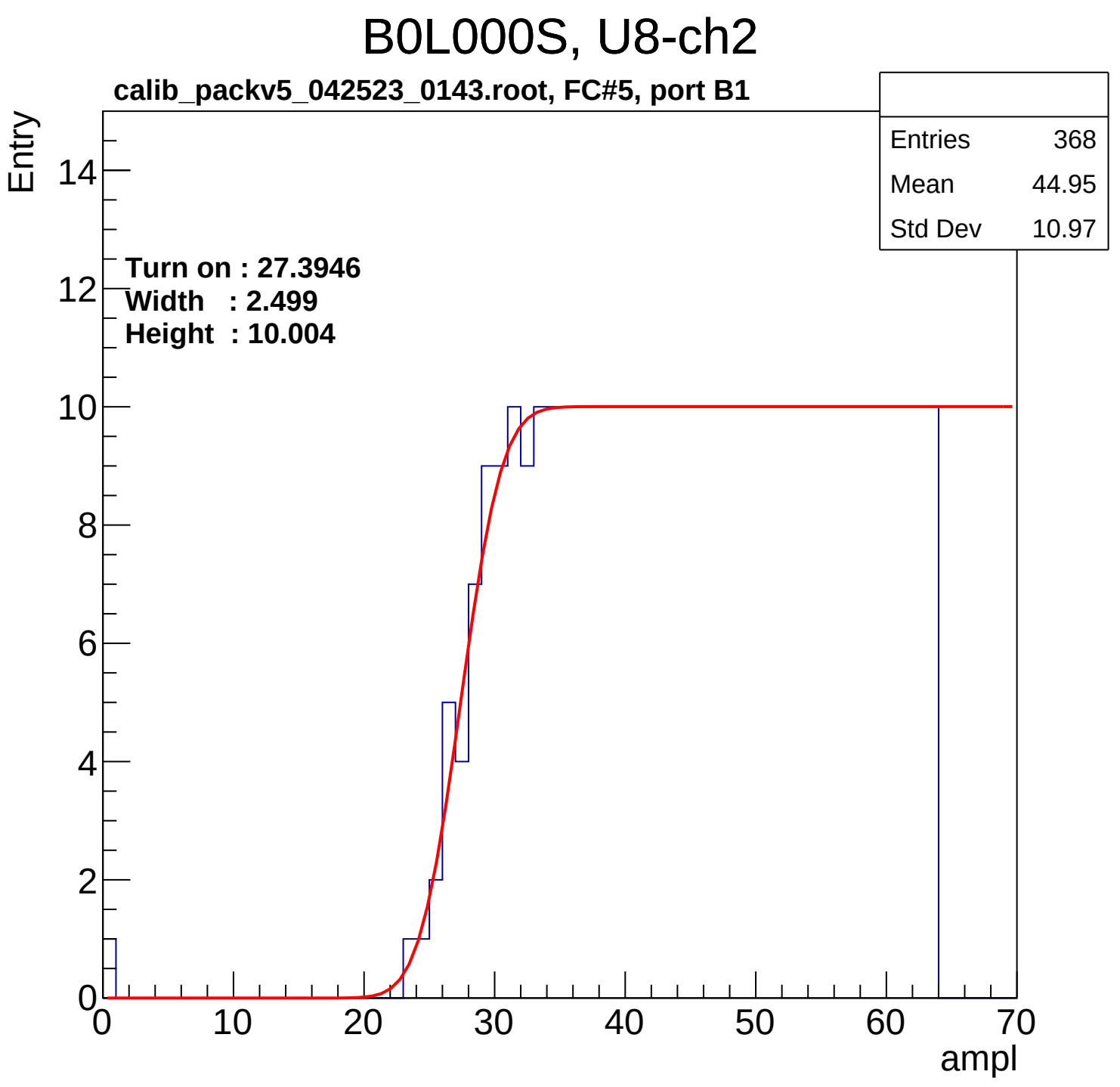
B0L000S, U8-ch2
calib_packv5_042523_0143.root, FC#5, port B1
Entries 368
Mean 44.95
Std Dev 10.97
Turn on : 27.3946
Width : 2.499
Height : 10.004
Entry
ampl
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2
4
6
8
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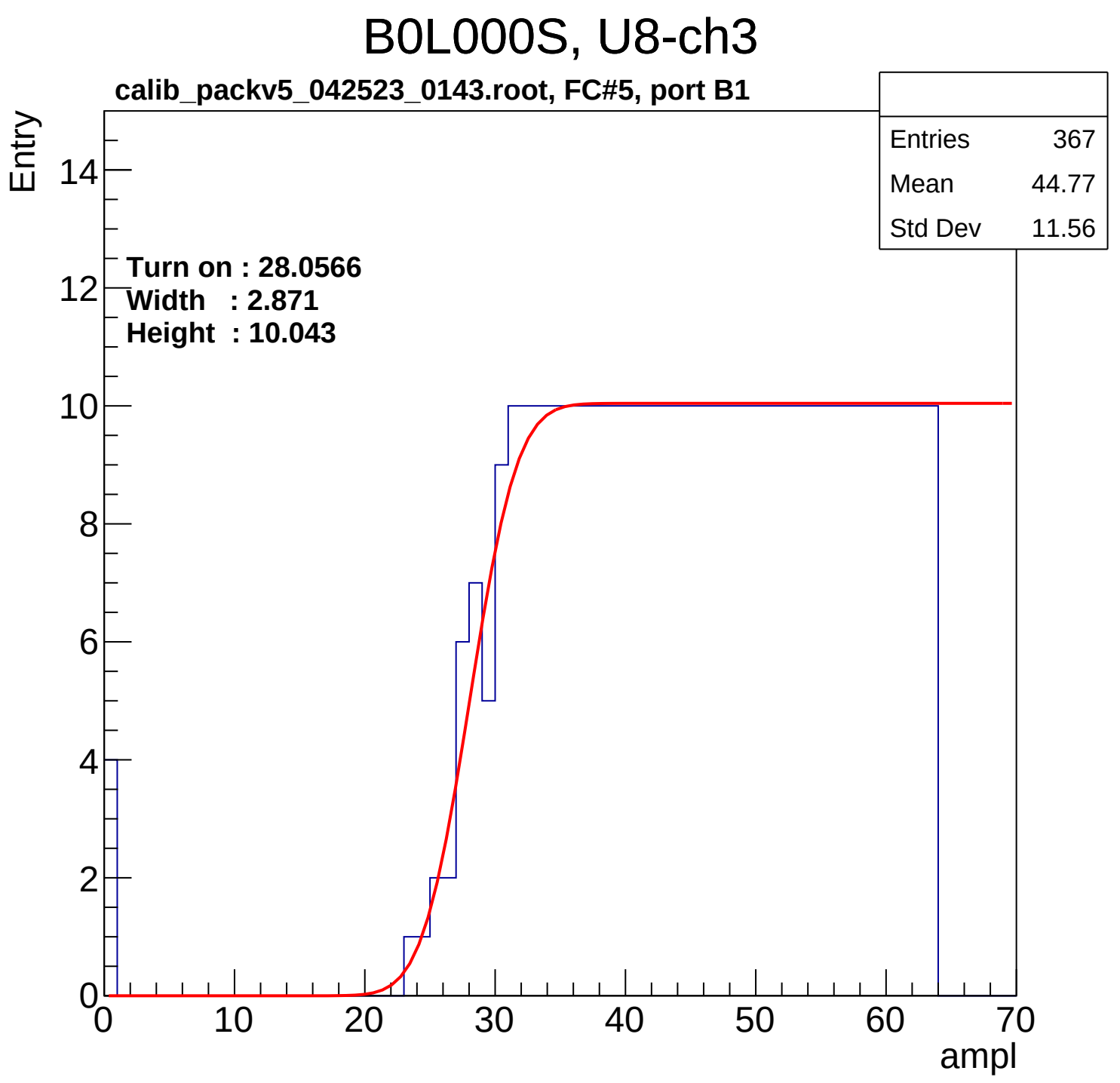
B0L000S, U8-ch3
calib_packv5_042523_0143.root, FC#5, port B1
Entries 367
Mean 44.77
Std Dev 11.56
Turn on : 28.0566
Width : 2.871
Height : 10.043
Entry
ampl
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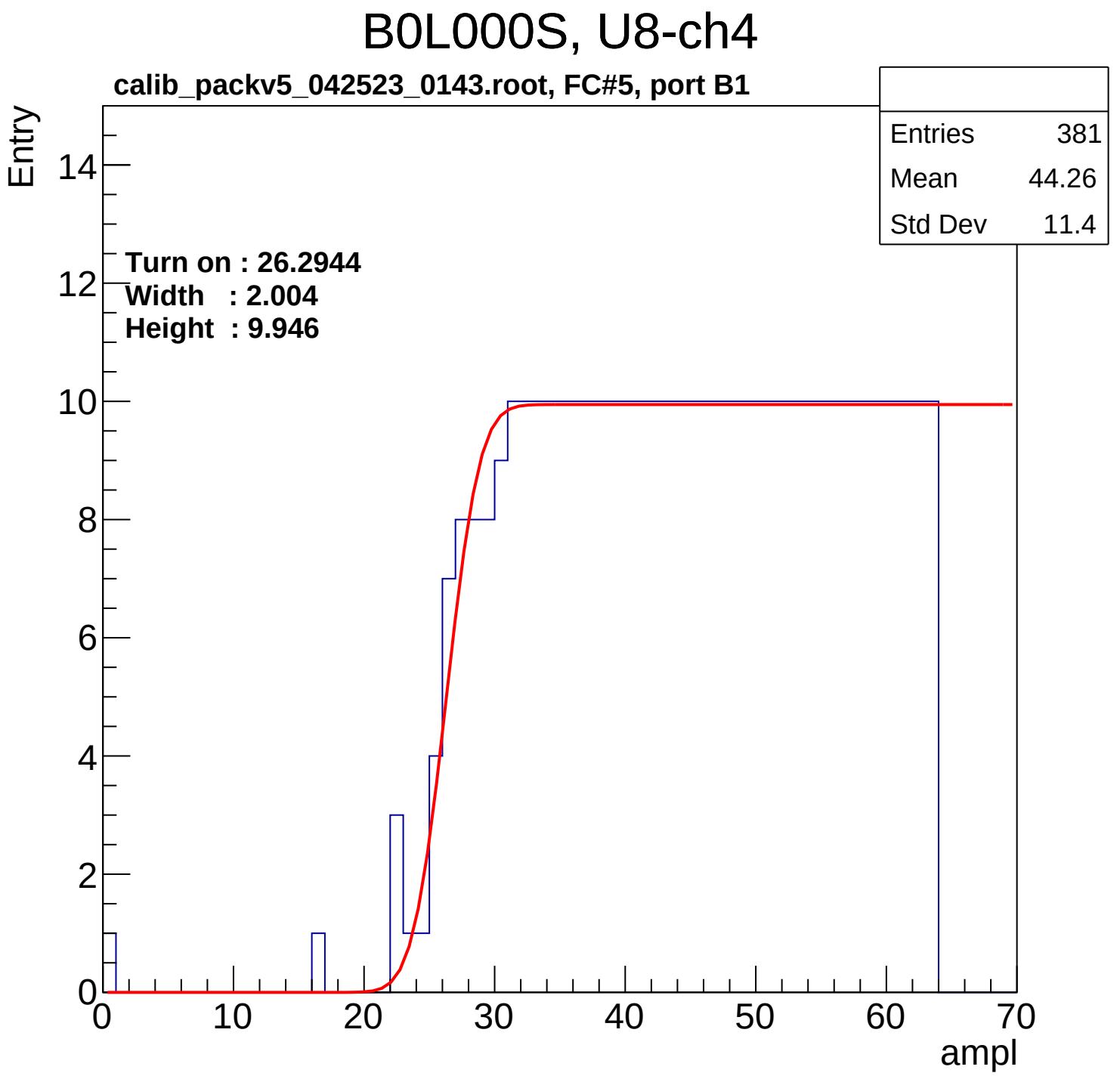
B0L000S, U8-ch4
calib_packv5_042523_0143.root, FC#5, port B1
Entries 381
Mean 44.26
Std Dev 11.4
Turn on : 26.2944
Width : 2.004
Height : 9.946
Entry
ampl
0
2
4
6
8
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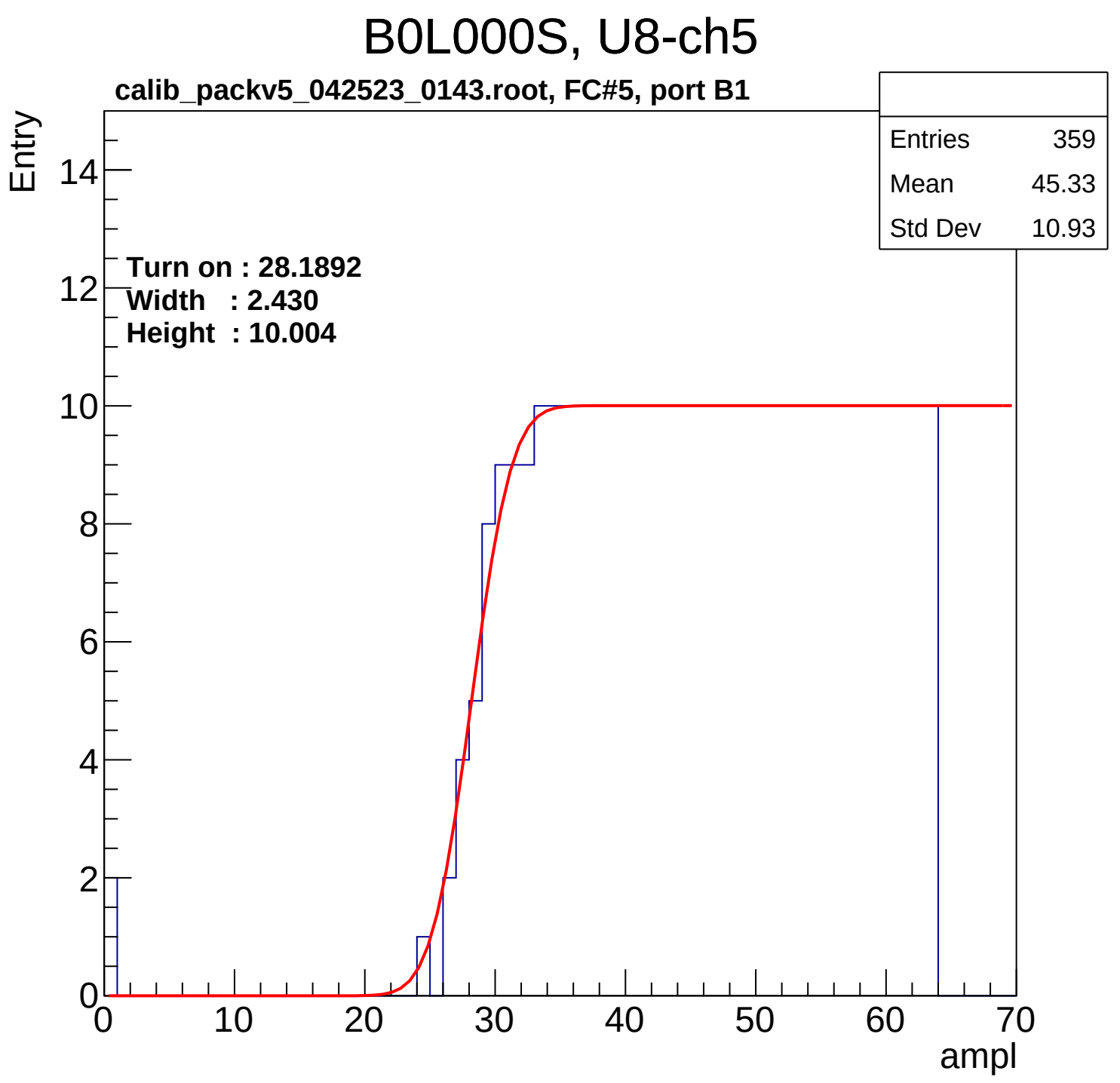
B0L000S, U8-ch5
calib_packv5_042523_0143.root, FC#5, port B1
Entries 359
Mean 45.33
Std Dev 10.93
Turn on : 28.1892
Width : 2.430
Height : 10.004
Entry
ampl
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4
6
8
10
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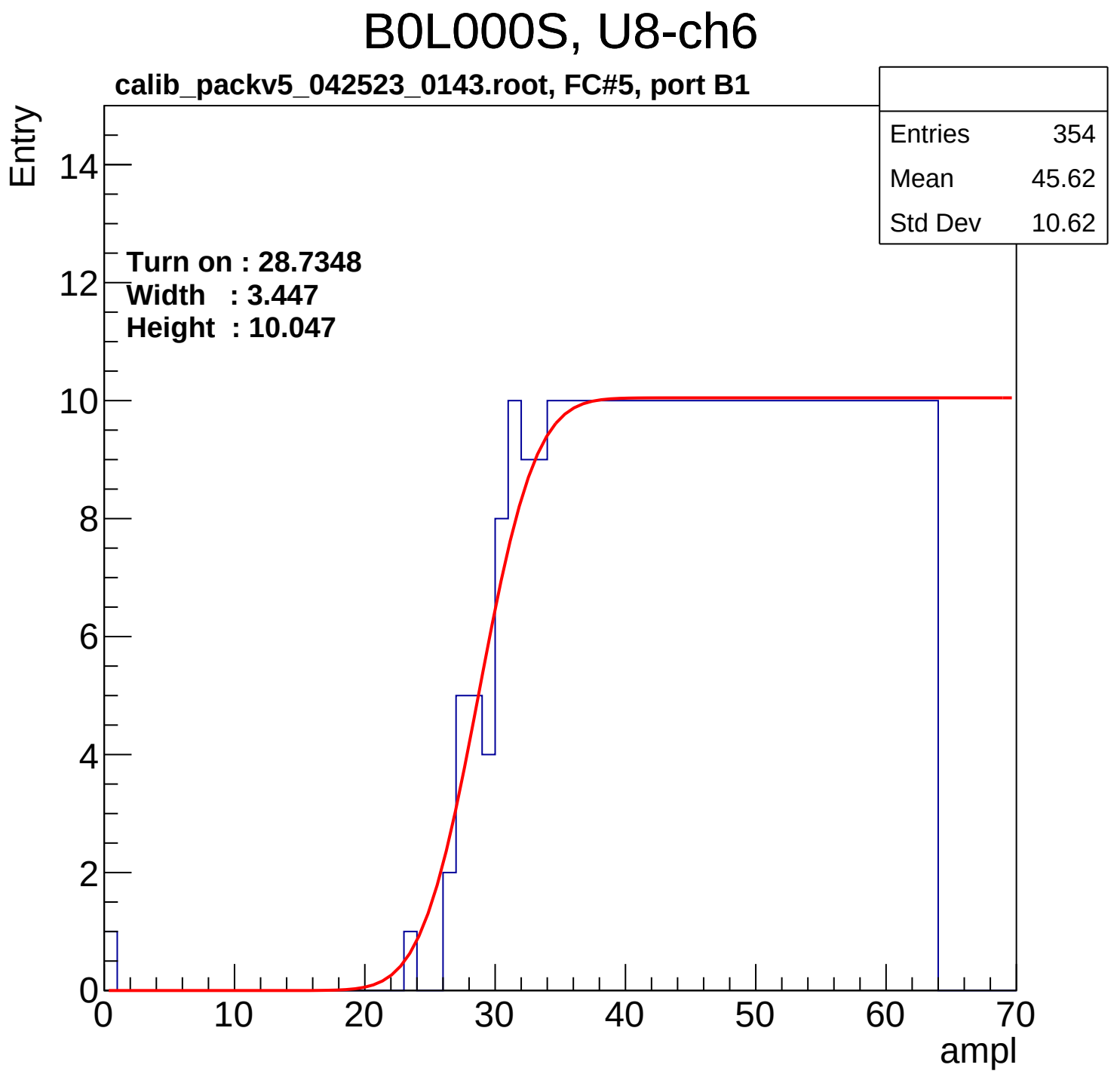
B0L000S, U8-ch6
calib_packv5_042523_0143.root, FC#5, port B1
Entries 354
Mean 45.62
Std Dev 10.62
Turn on : 28.7348
Width : 3.447
Height : 10.047
Entry
ampl
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4
6
8
10
12
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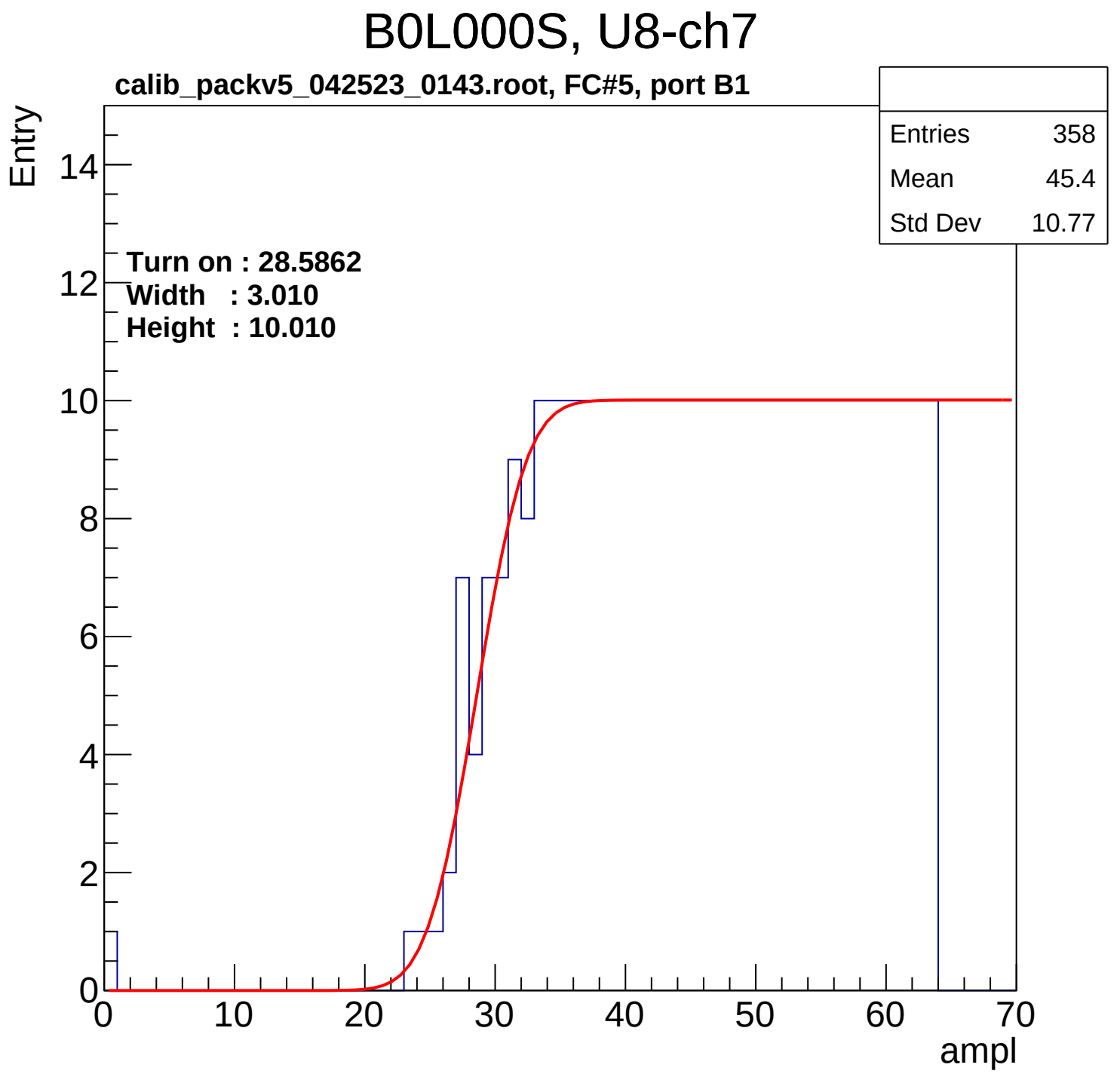
B0L000S, U8-ch7
calib_packv5_042523_0143.root, FC#5, port B1
Entries 358
Mean 45.4
Std Dev 10.77
Turn on : 28.5862
Width : 3.010
Height : 10.010
Entry
ampl
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2
4
6
8
10
12
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0
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60
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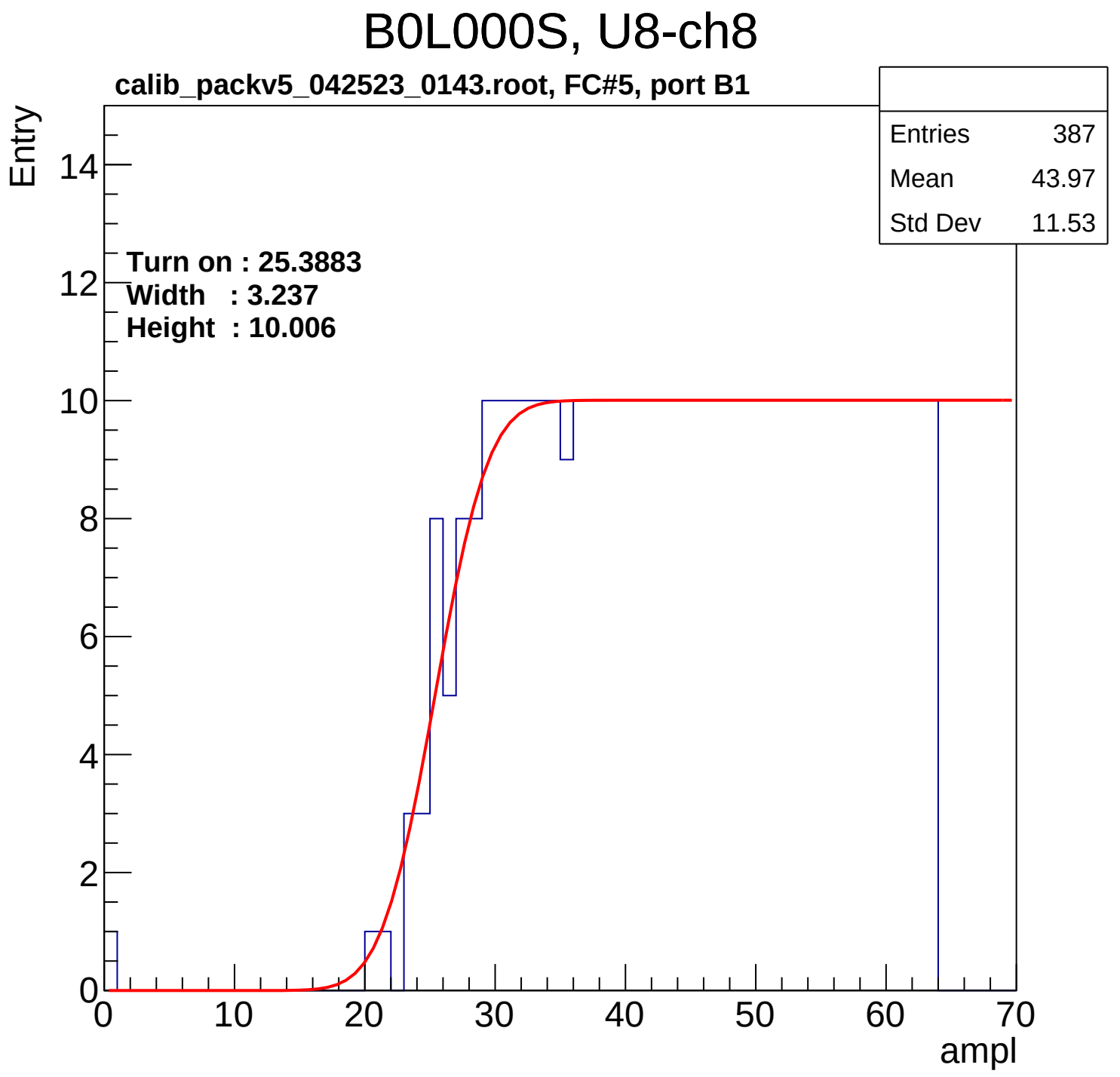
B0L000S, U8-ch8
calib_packv5_042523_0143.root, FC#5, port B1
Entries 387
Mean 43.97
Std Dev 11.53
Turn on : 25.3883
Width : 3.237
Height : 10.006
Entry
ampl
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6
8
10
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0
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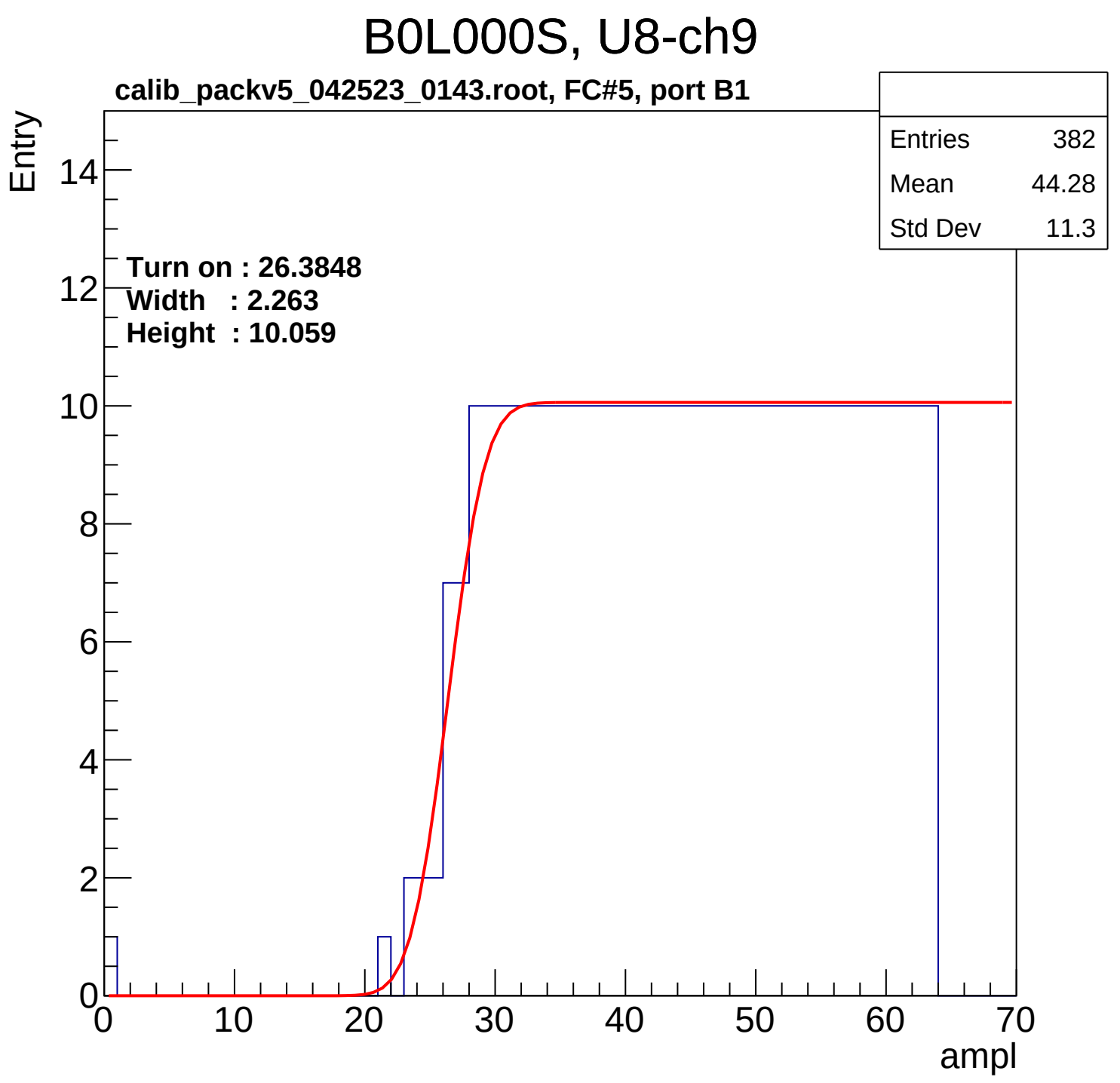
B0L000S, U8-ch9
calib_packv5_042523_0143.root, FC#5, port B1
Entries 382
Mean 44.28
Std Dev 11.3
Turn on : 26.3848
Width : 2.263
Height : 10.059
Entry
ampl
0
2
4
6
8
10
12
14
0
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20
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60
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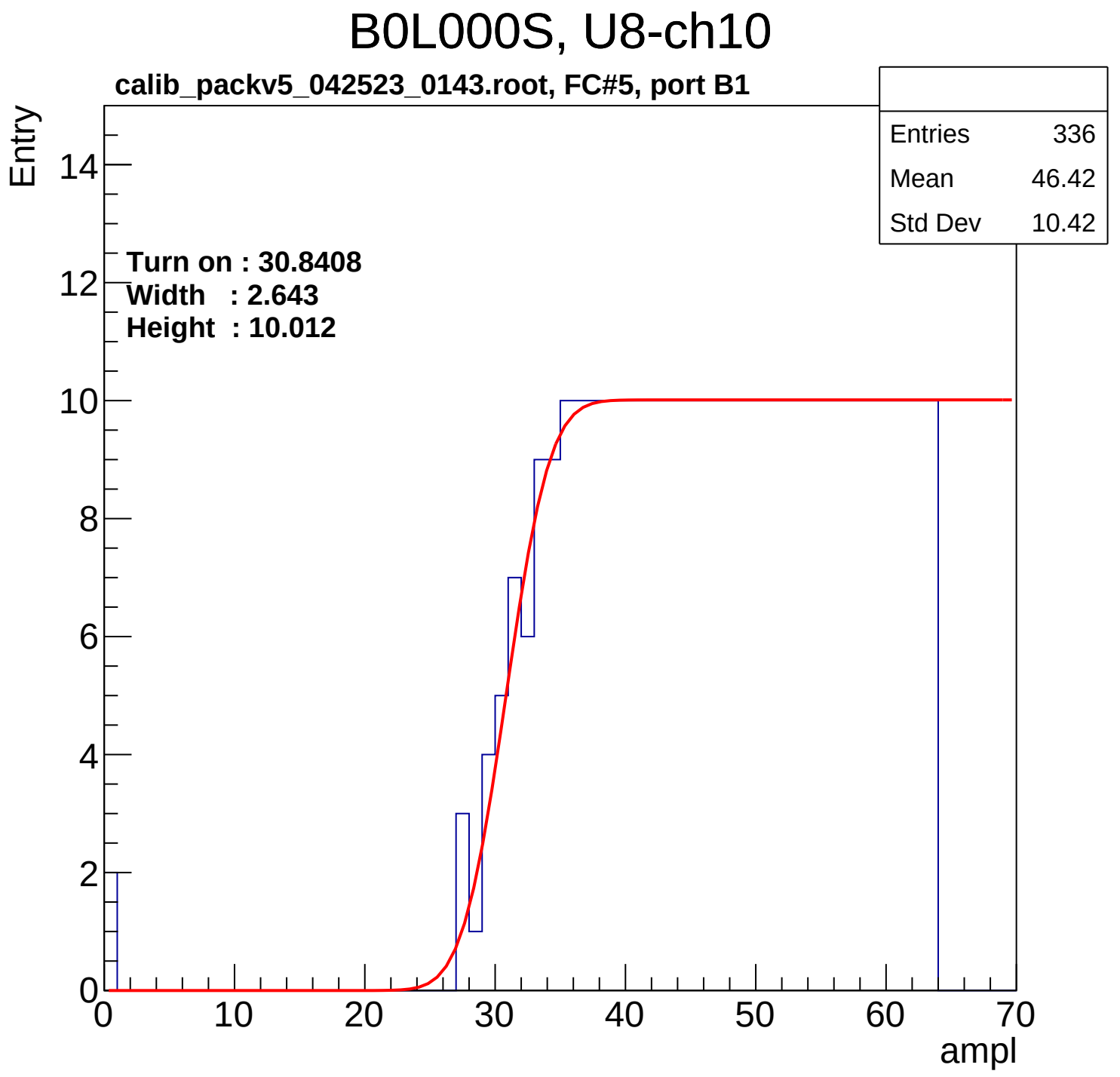
B0L000S, U8-ch10
calib_packv5_042523_0143.root, FC#5, port B1
Entries 336
Mean 46.42
Std Dev 10.42
Turn on : 30.8408
Width : 2.643
Height : 10.012
Entry
ampl
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8
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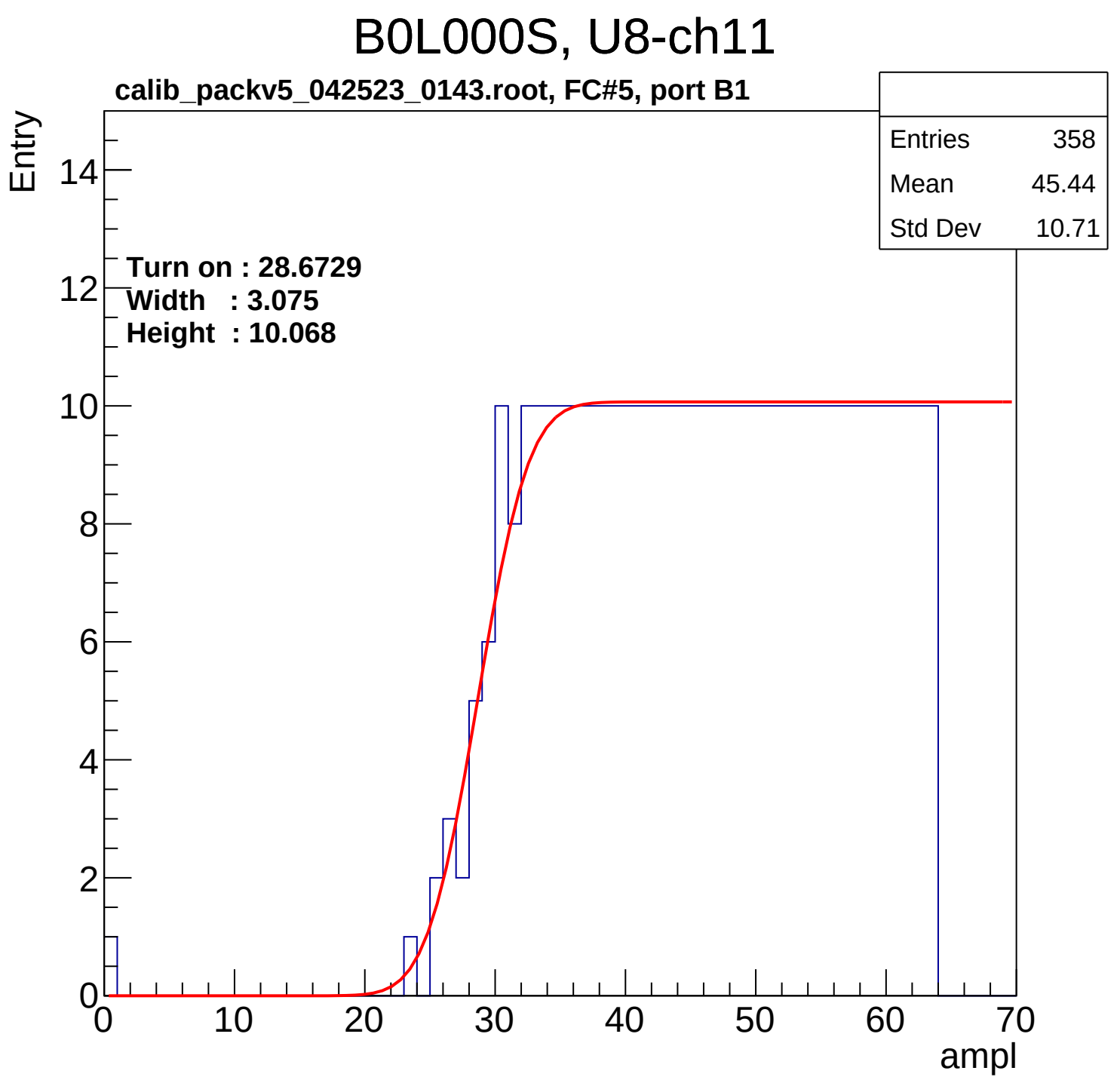
B0L000S, U8-ch11
calib_packv5_042523_0143.root, FC#5, port B1
Entries 358
Mean 45.44
Std Dev 10.71
Turn on : 28.6729
Width : 3.075
Height : 10.068
Entry
ampl
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2
4
6
8
10
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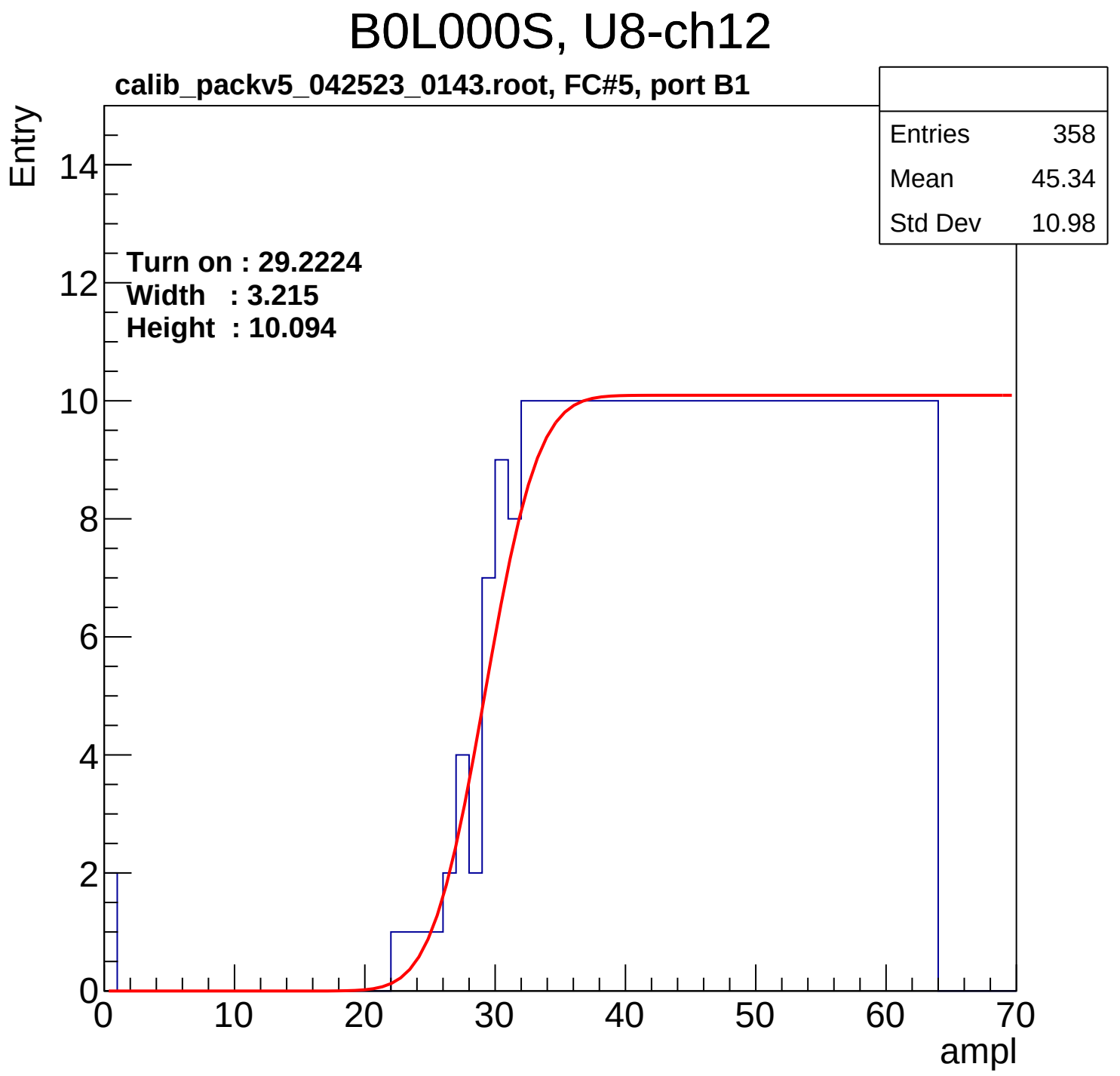
B0L000S, U8-ch12
calib_packv5_042523_0143.root, FC#5, port B1
Entries 358
Mean 45.34
Std Dev 10.98
Turn on : 29.2224
Width : 3.215
Height : 10.094
Entry
ampl
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2
4
6
8
10
12
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0
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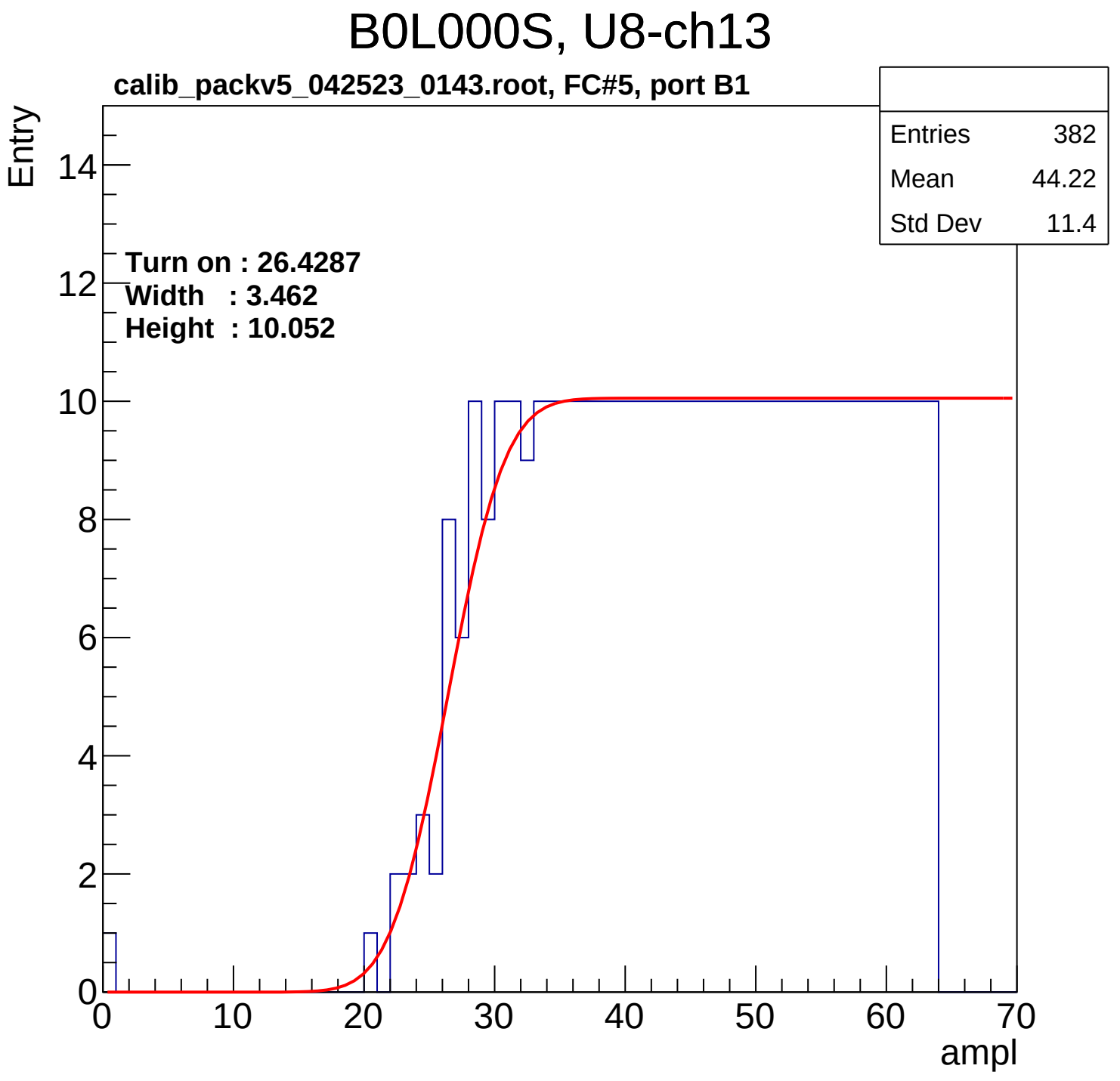
B0L000S, U8-ch13
calib_packv5_042523_0143.root, FC#5, port B1
Entries 382
Mean 44.22
Std Dev 11.4
Turn on : 26.4287
Width : 3.462
Height : 10.052
Entry
ampl
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6
8
10
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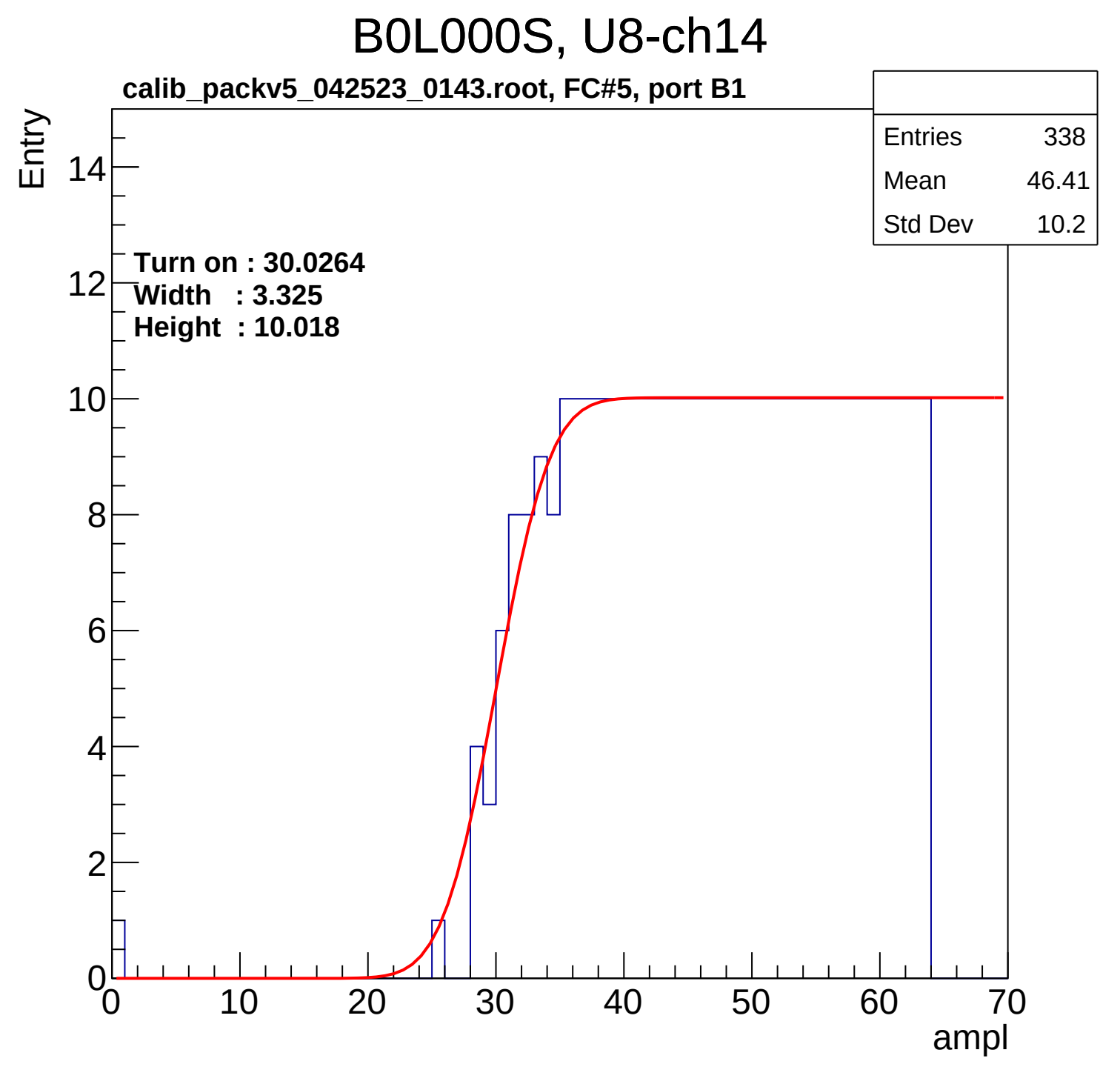
B0L000S, U8-ch14
calib_packv5_042523_0143.root, FC#5, port B1
Entries 338
Mean 46.41
Std Dev 10.2
Turn on : 30.0264
Width : 3.325
Height : 10.018
Entry
ampl
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6
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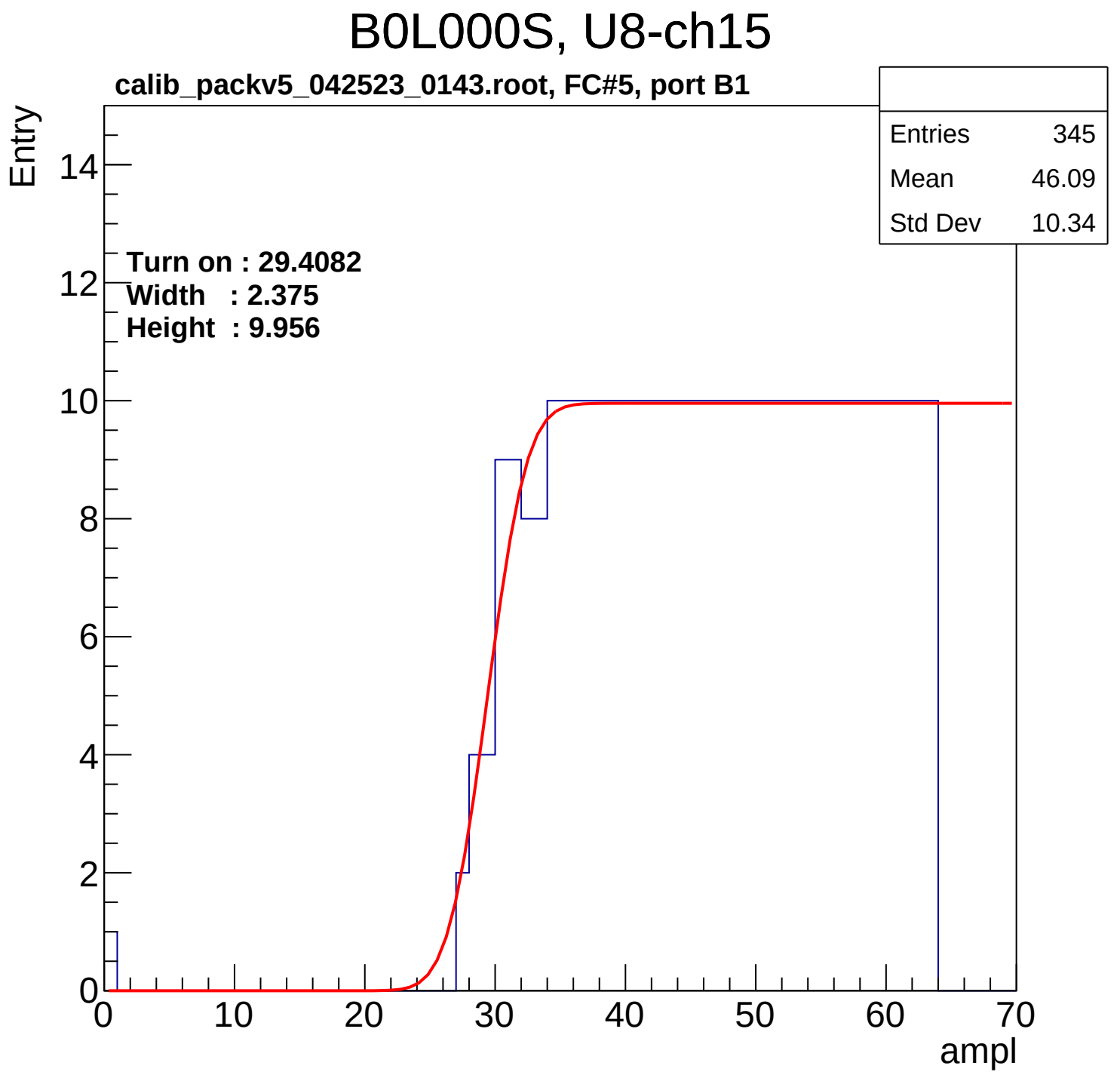
B0L000S, U8-ch15
calib_packv5_042523_0143.root, FC#5, port B1
Entries 345
Mean 46.09
Std Dev 10.34
Turn on : 29.4082
Width : 2.375
Height : 9.956
Entry
ampl
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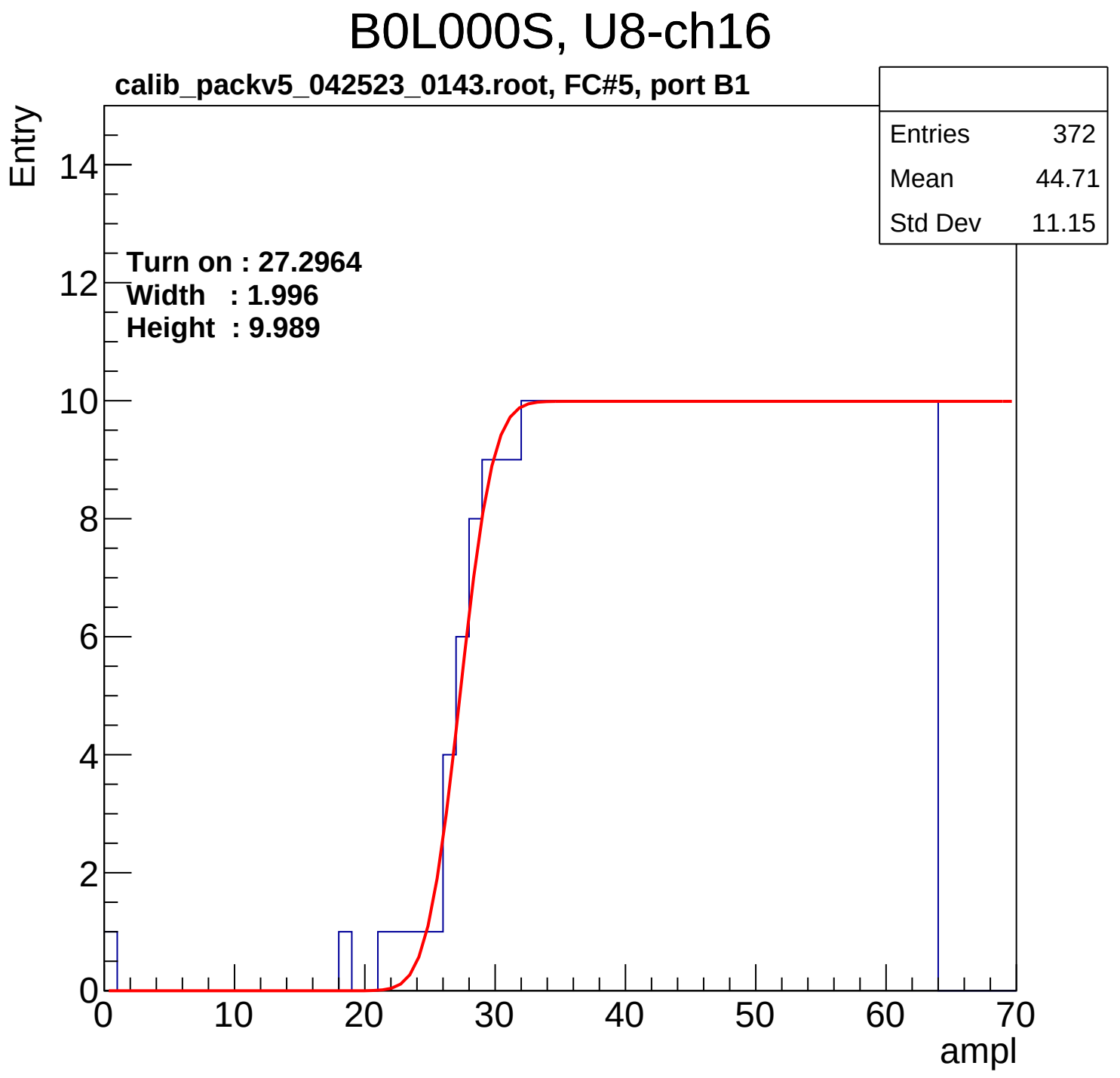
B0L000S, U8-ch16
calib_packv5_042523_0143.root, FC#5, port B1
Entries 372
Mean 44.71
Std Dev 11.15
Turn on : 27.2964
Width : 1.996
Height : 9.989
Entry
ampl
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8
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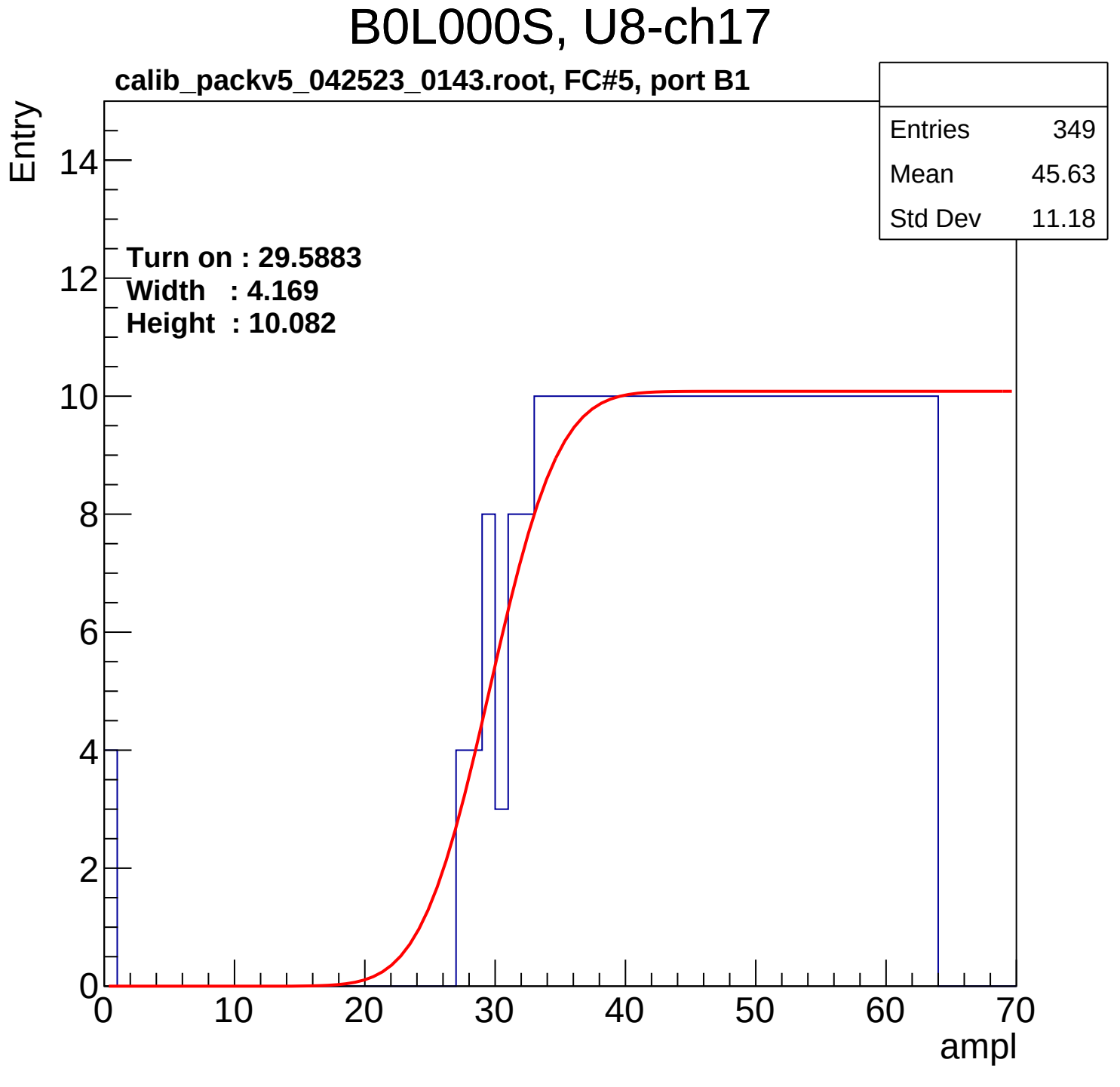
B0L000S, U8-ch17
calib_packv5_042523_0143.root, FC#5, port B1
Entries 349
Mean 45.63
Std Dev 11.18
Turn on : 29.5883
Width : 4.169
Height : 10.082
Entry
ampl
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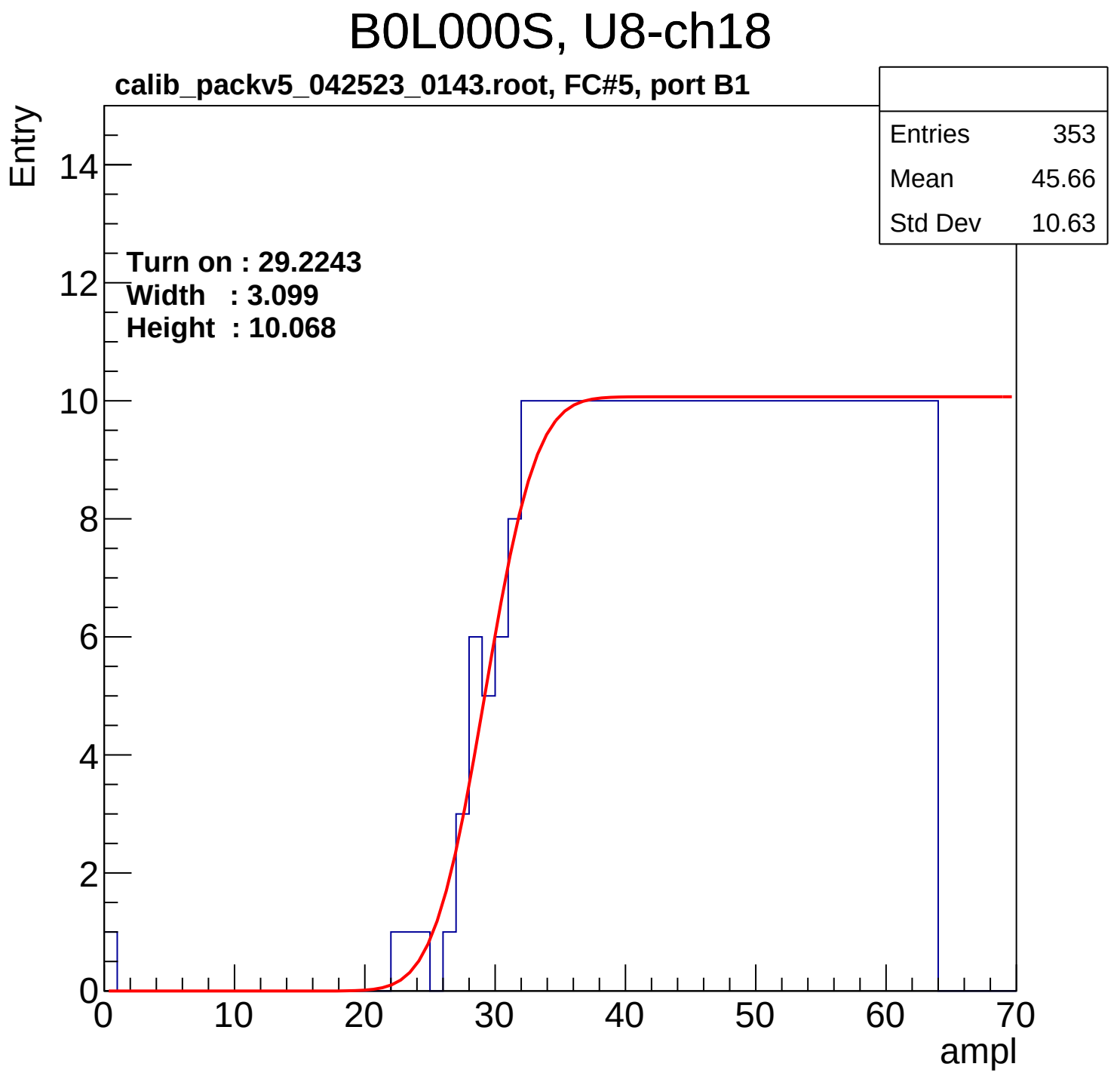
B0L000S, U8-ch18
calib_packv5_042523_0143.root, FC#5, port B1
Entries 353
Mean 45.66
Std Dev 10.63
Turn on : 29.2243
Width : 3.099
Height : 10.068
Entry
ampl
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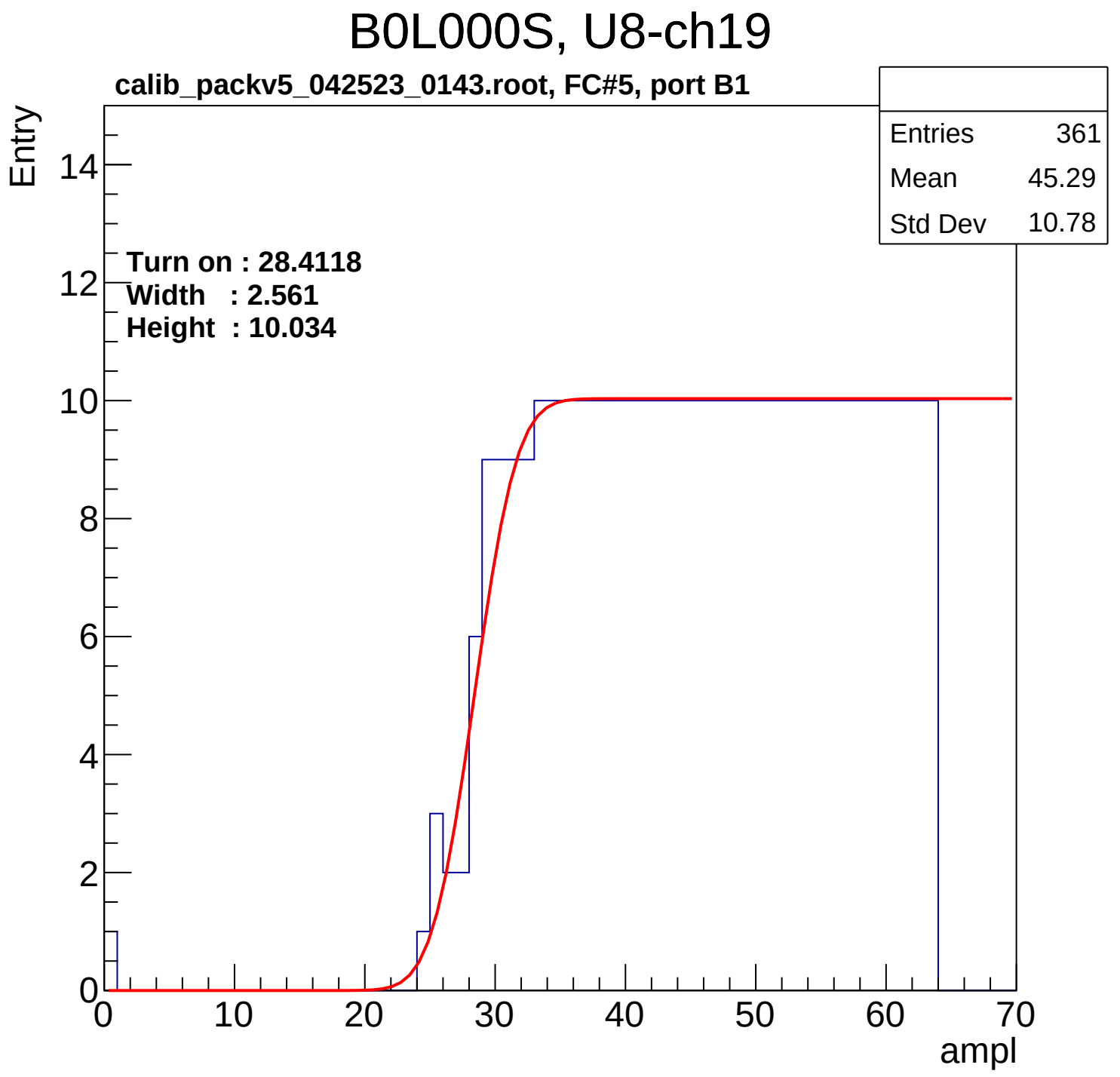
B0L000S, U8-ch19
calib_packv5_042523_0143.root, FC#5, port B1
Entries 361
Mean 45.29
Std Dev 10.78
Turn on : 28.4118
Width : 2.561
Height : 10.034
Entry
ampl
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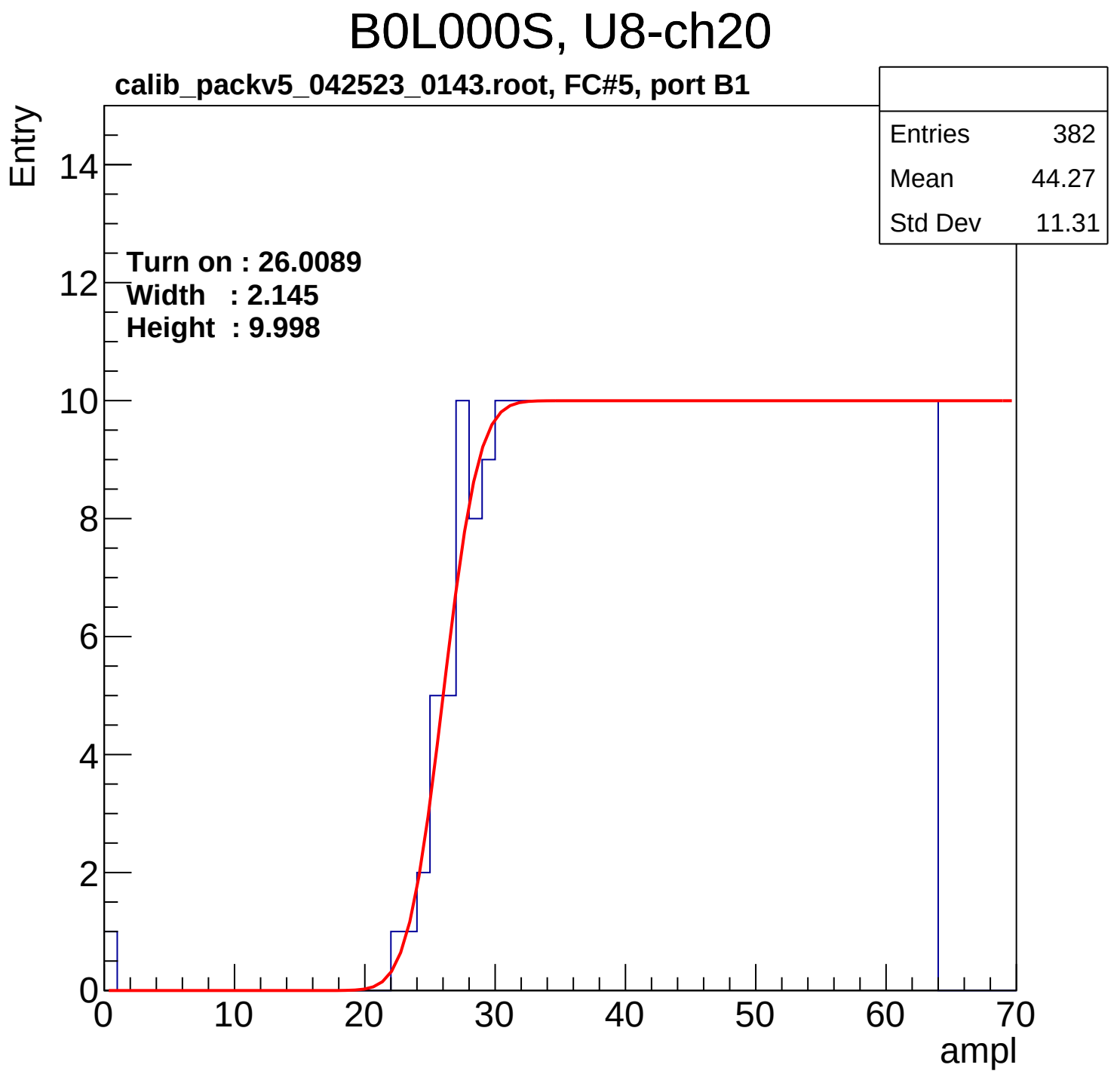
B0L000S, U8-ch20
calib_packv5_042523_0143.root, FC#5, port B1
Entries 382
Mean 44.27
Std Dev 11.31
Turn on : 26.0089
Width : 2.145
Height : 9.998
Entry
ampl
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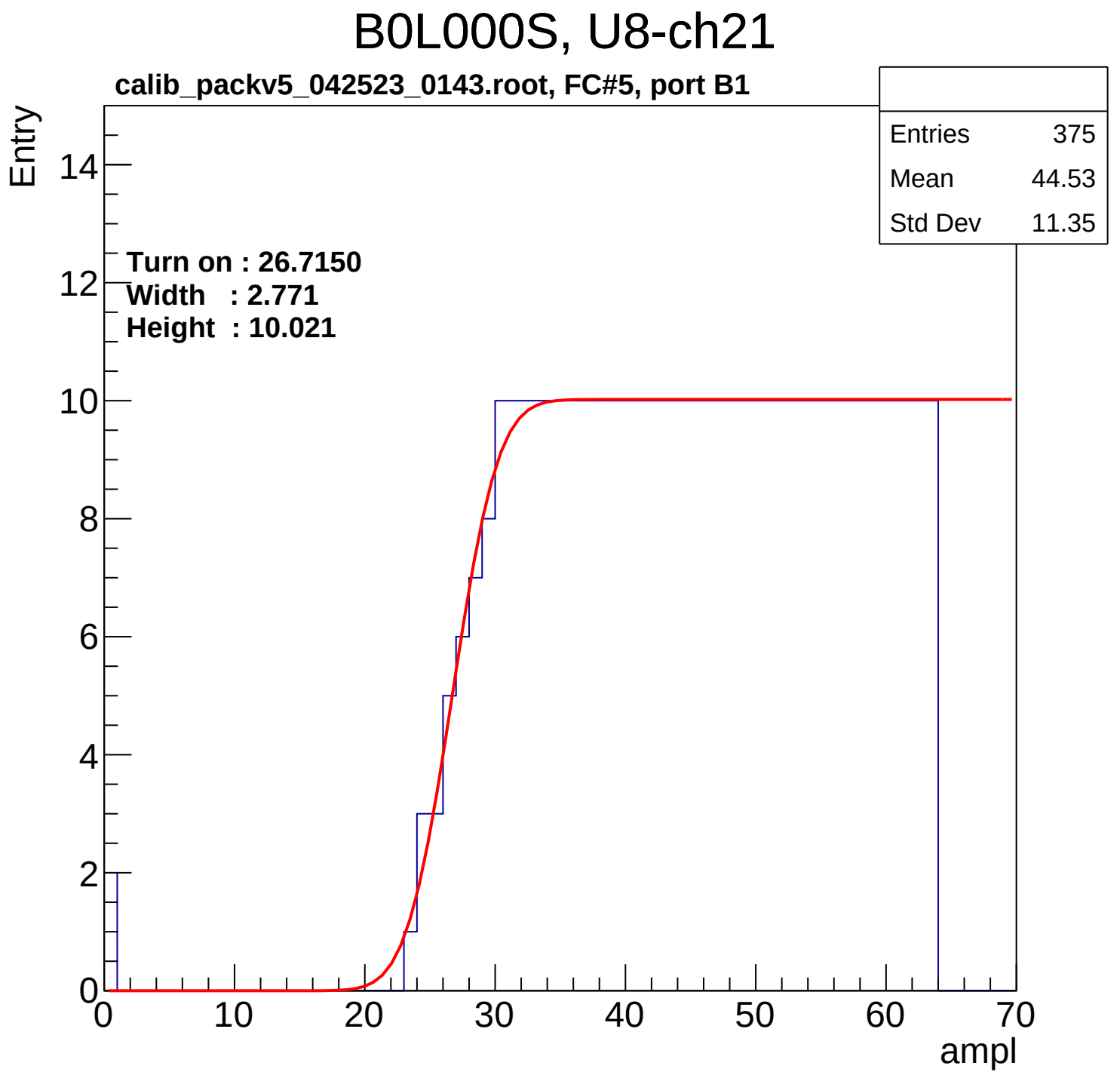
B0L000S, U8-ch21
calib_packv5_042523_0143.root, FC#5, port B1
Entries 375
Mean 44.53
Std Dev 11.35
Turn on : 26.7150
Width : 2.771
Height : 10.021
Entry
ampl
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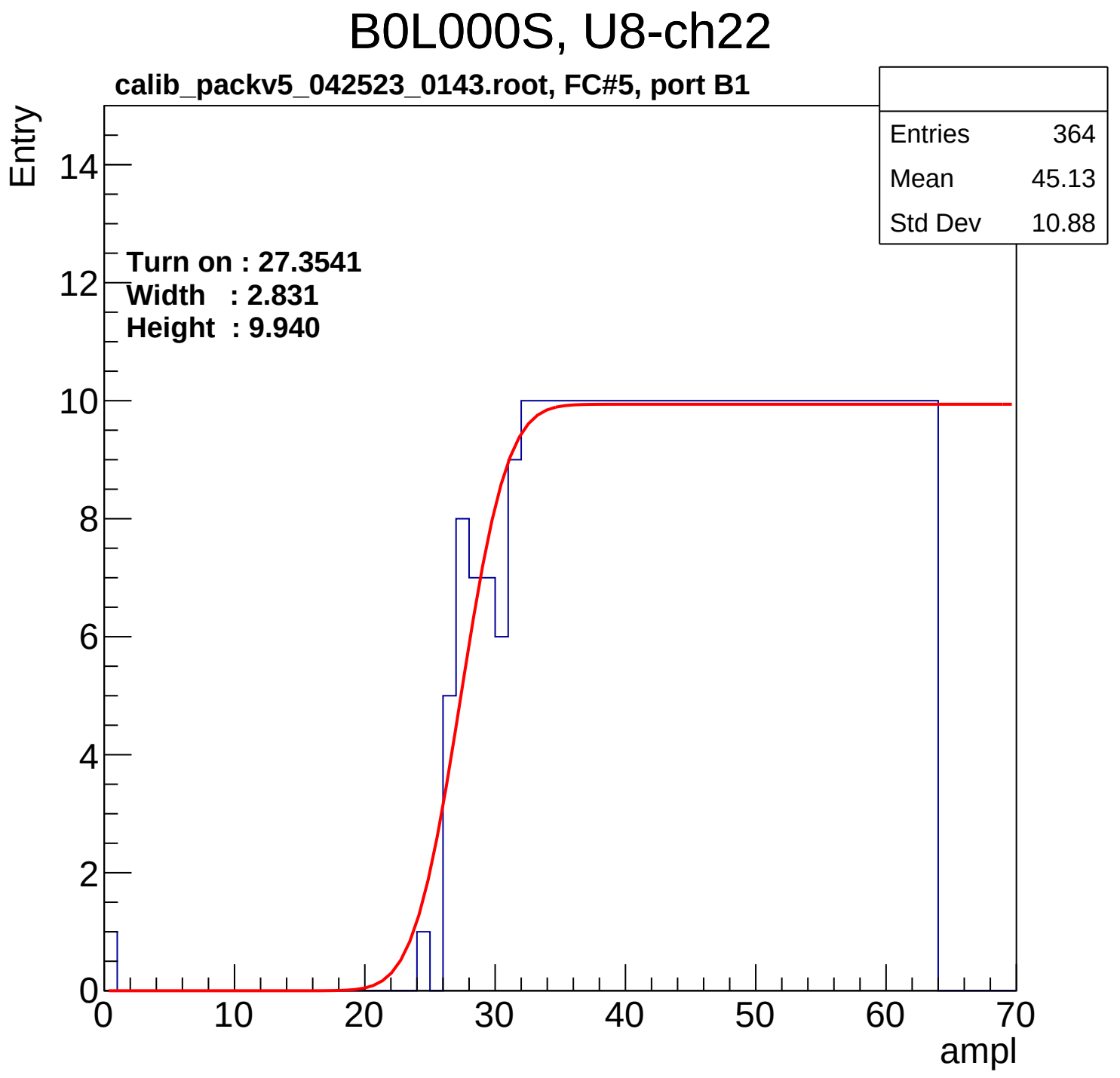
B0L000S, U8-ch22
calib_packv5_042523_0143.root, FC#5, port B1
Entries 364
Mean 45.13
Std Dev 10.88
Turn on : 27.3541
Width : 2.831
Height : 9.940
Entry
ampl
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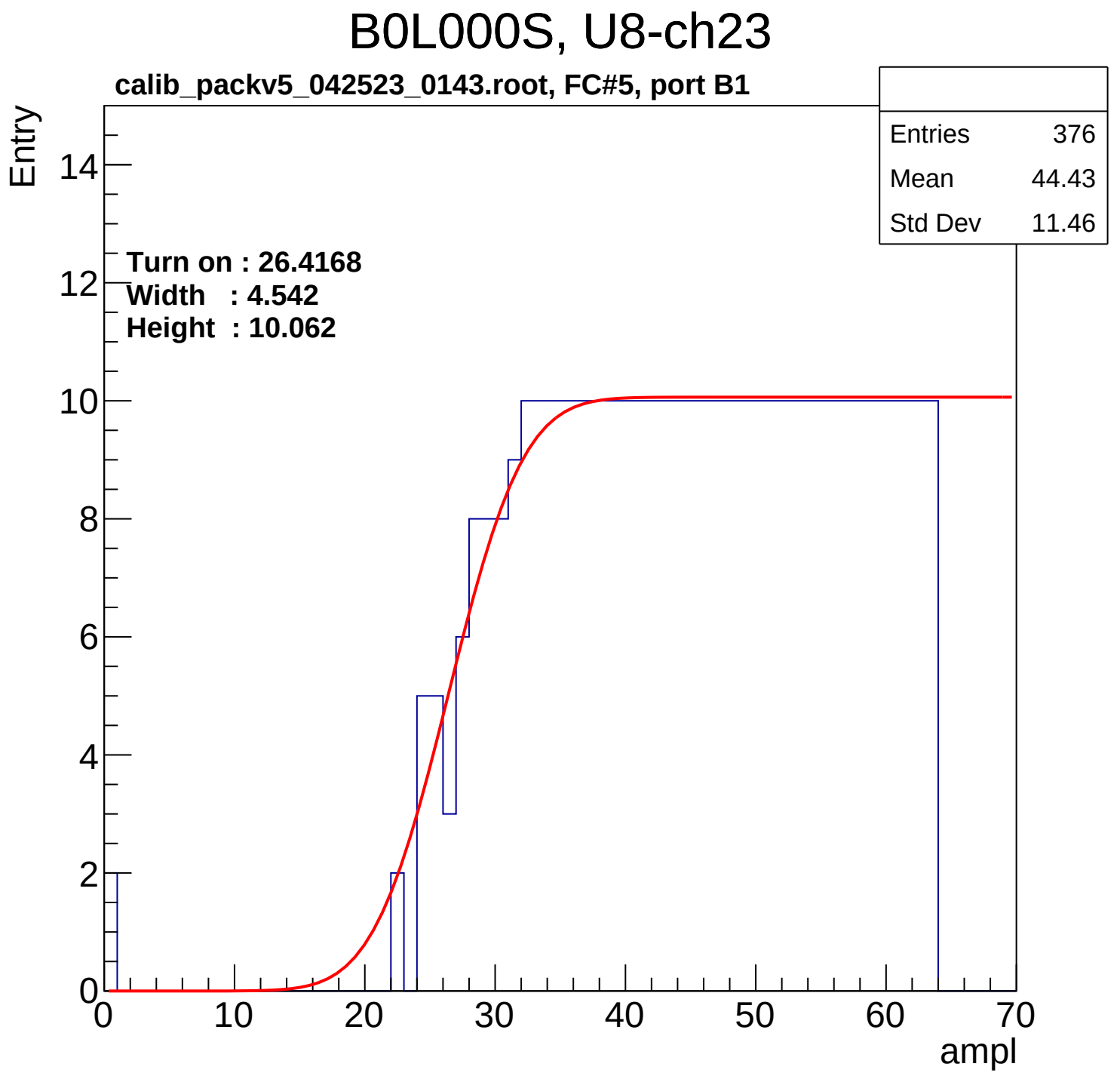
B0L000S, U8-ch23
calib_packv5_042523_0143.root, FC#5, port B1
Entries 376
Mean 44.43
Std Dev 11.46
Turn on : 26.4168
Width : 4.542
Height : 10.062
Entry
ampl
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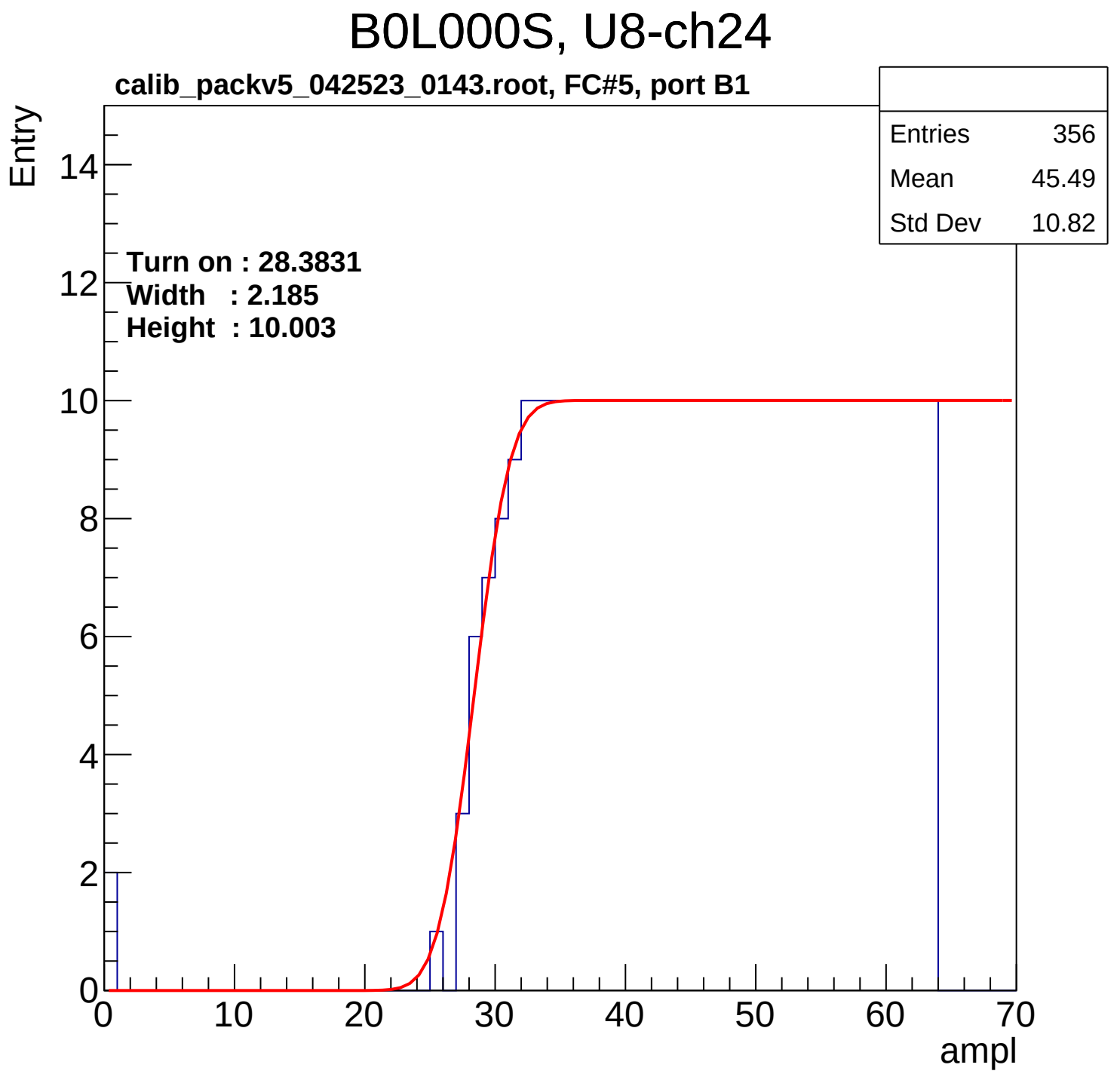
B0L000S, U8-ch24
calib_packv5_042523_0143.root, FC#5, port B1
Entries 356
Mean 45.49
Std Dev 10.82
Turn on : 28.3831
Width : 2.185
Height : 10.003
Entry
ampl
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6
8
10
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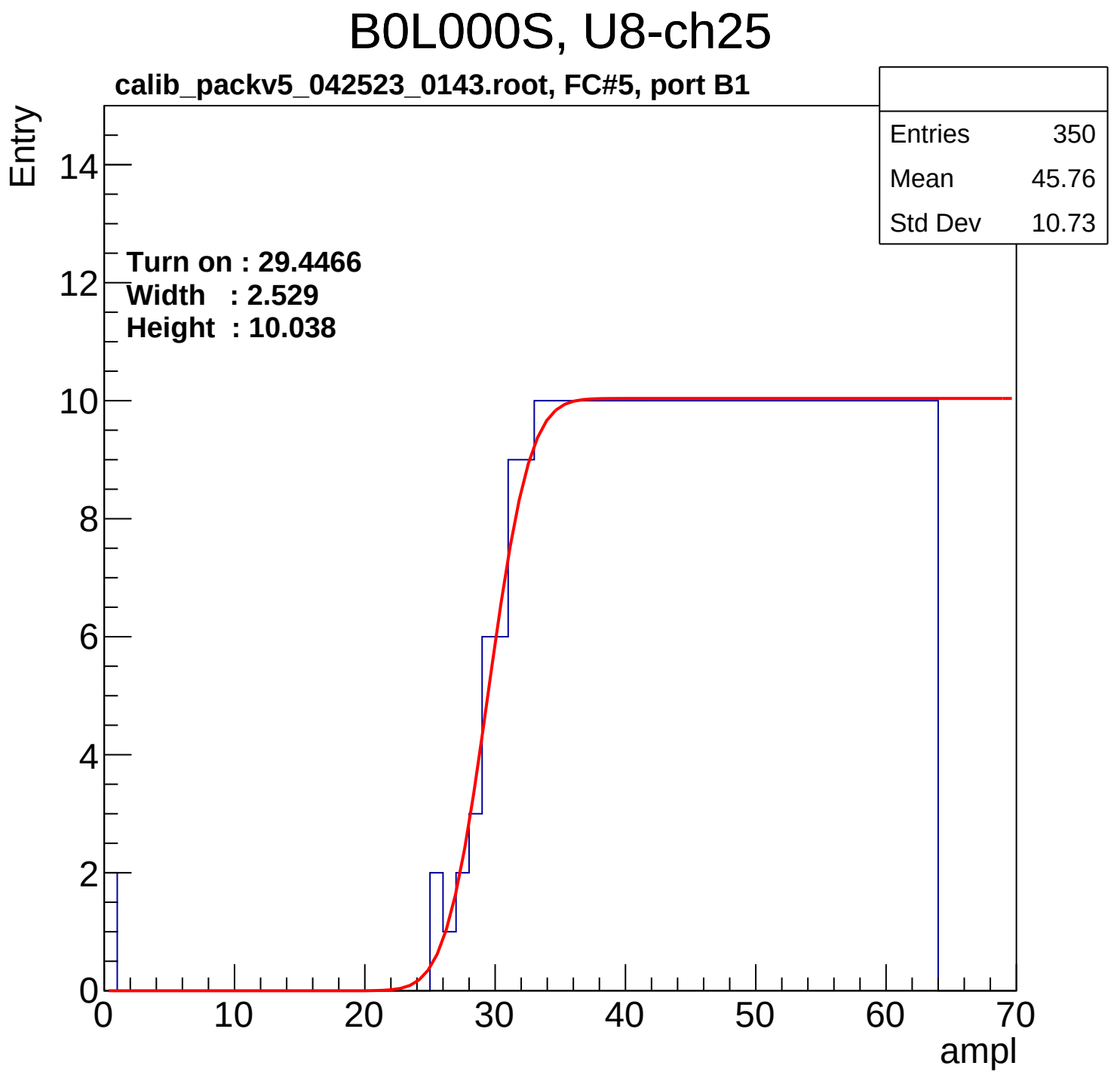
B0L000S, U8-ch25
calib_packv5_042523_0143.root, FC#5, port B1
Entries 350
Mean 45.76
Std Dev 10.73
Turn on : 29.4466
Width : 2.529
Height : 10.038
Entry
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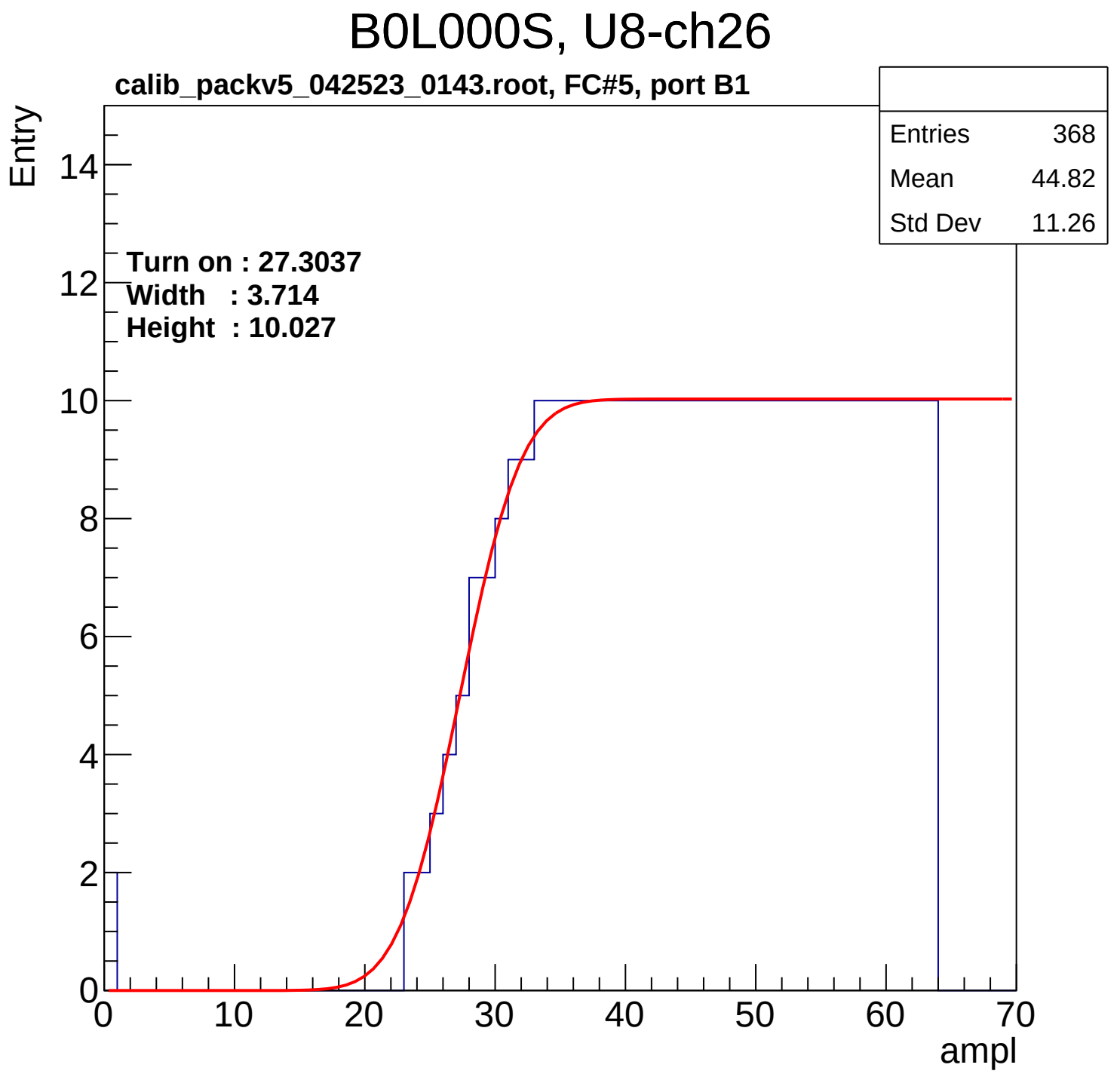
B0L000S, U8-ch26
calib_packv5_042523_0143.root, FC#5, port B1
Entries 368
Mean 44.82
Std Dev 11.26
Turn on : 27.3037
Width : 3.714
Height : 10.027
Entry
ampl
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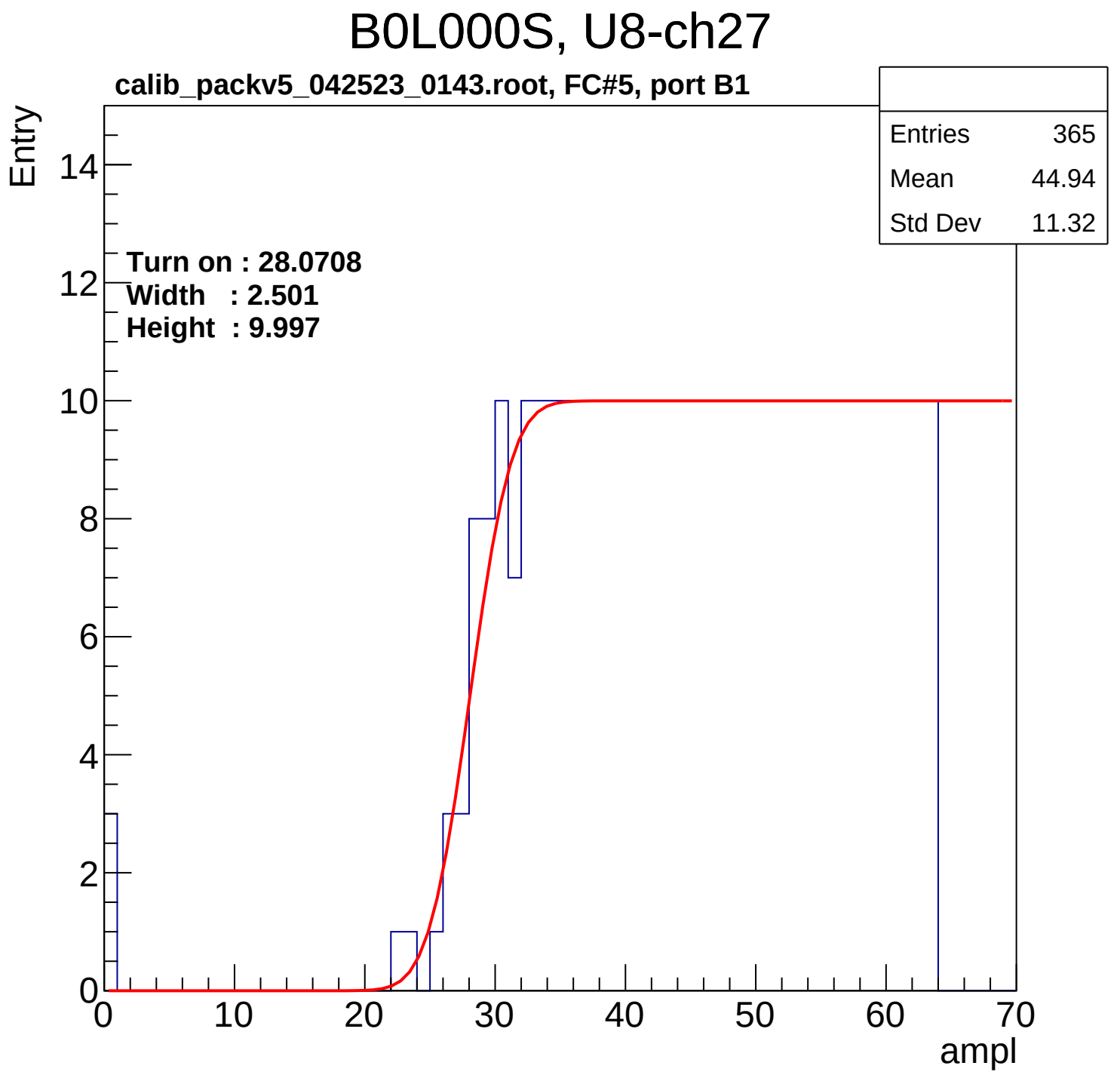
B0L000S, U8-ch27
calib_packv5_042523_0143.root, FC#5, port B1
Entries 365
Mean 44.94
Std Dev 11.32
Turn on : 28.0708
Width : 2.501
Height : 9.997
Entry
ampl
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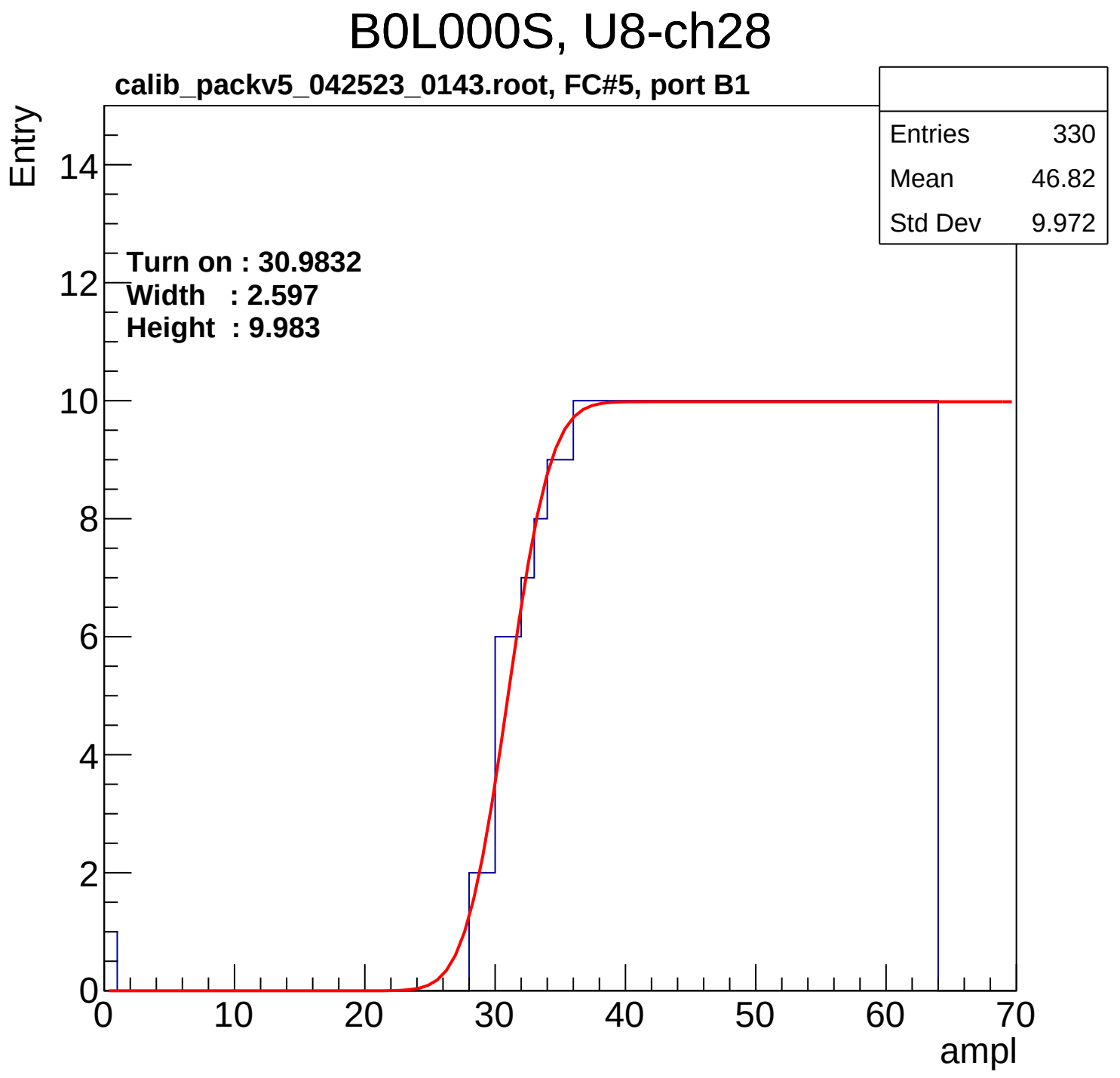
B0L000S, U8-ch28
calib_packv5_042523_0143.root, FC#5, port B1
Entries 330
Mean 46.82
Std Dev 9.972
Turn on : 30.9832
Width : 2.597
Height : 9.983
Entry
ampl
0
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4
6
8
10
12
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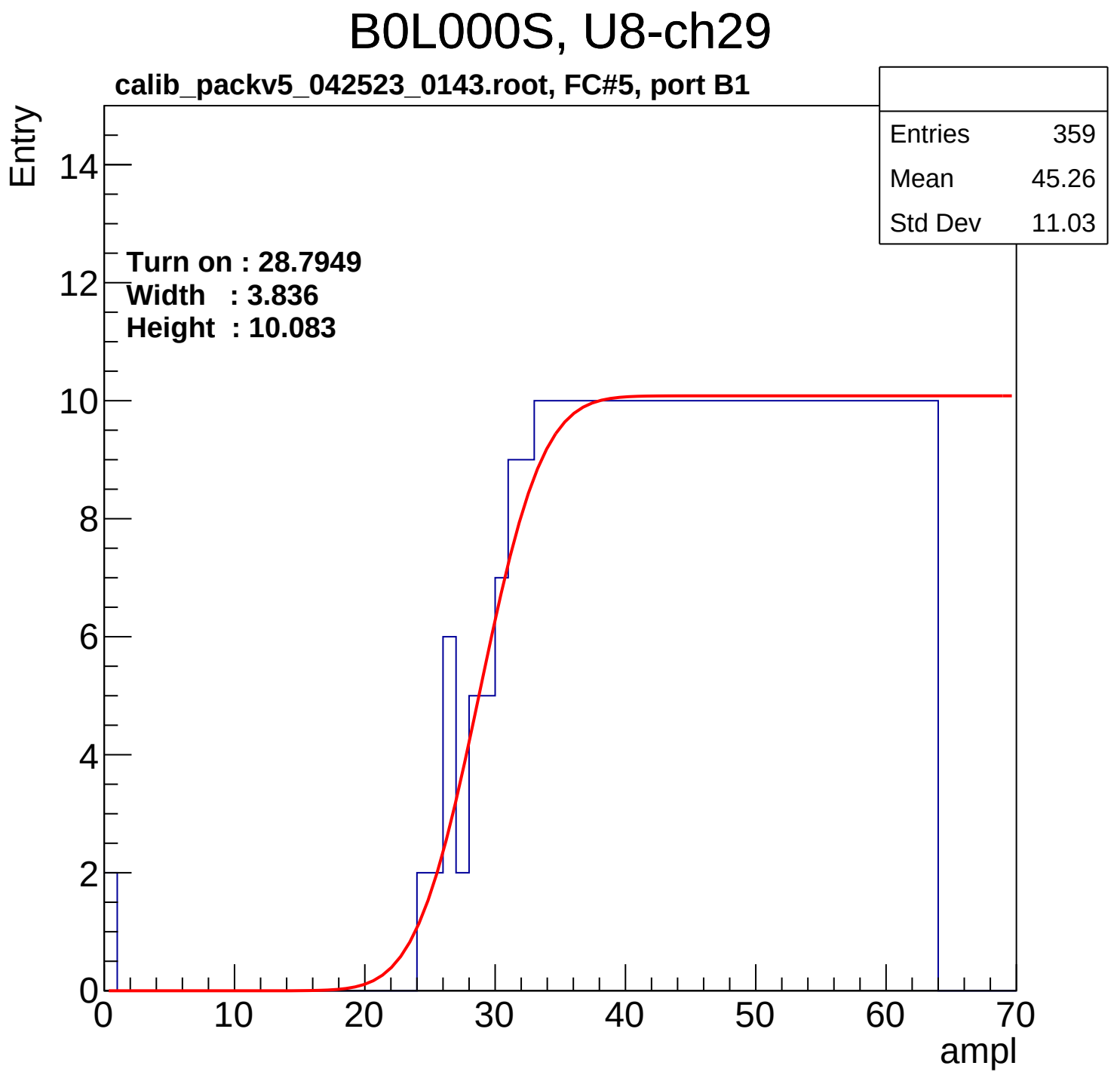
B0L000S, U8-ch29
calib_packv5_042523_0143.root, FC#5, port B1
Entries 359
Mean 45.26
Std Dev 11.03
Turn on : 28.7949
Width : 3.836
Height : 10.083
Entry
ampl
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8
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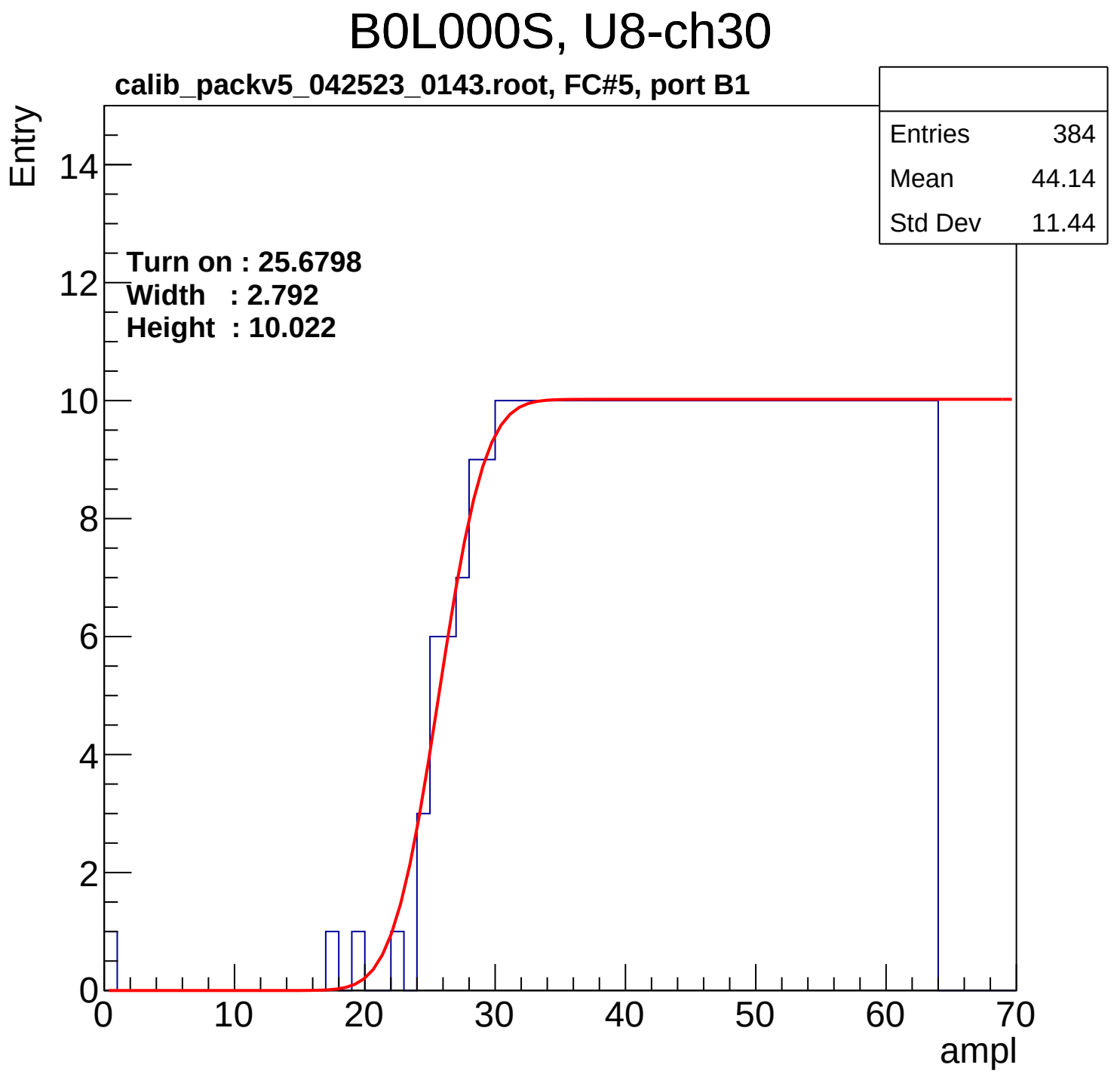
B0L000S, U8-ch30
calib_packv5_042523_0143.root, FC#5, port B1
Entries 384
Mean 44.14
Std Dev 11.44
Turn on : 25.6798
Width : 2.792
Height : 10.022
Entry
ampl
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4
6
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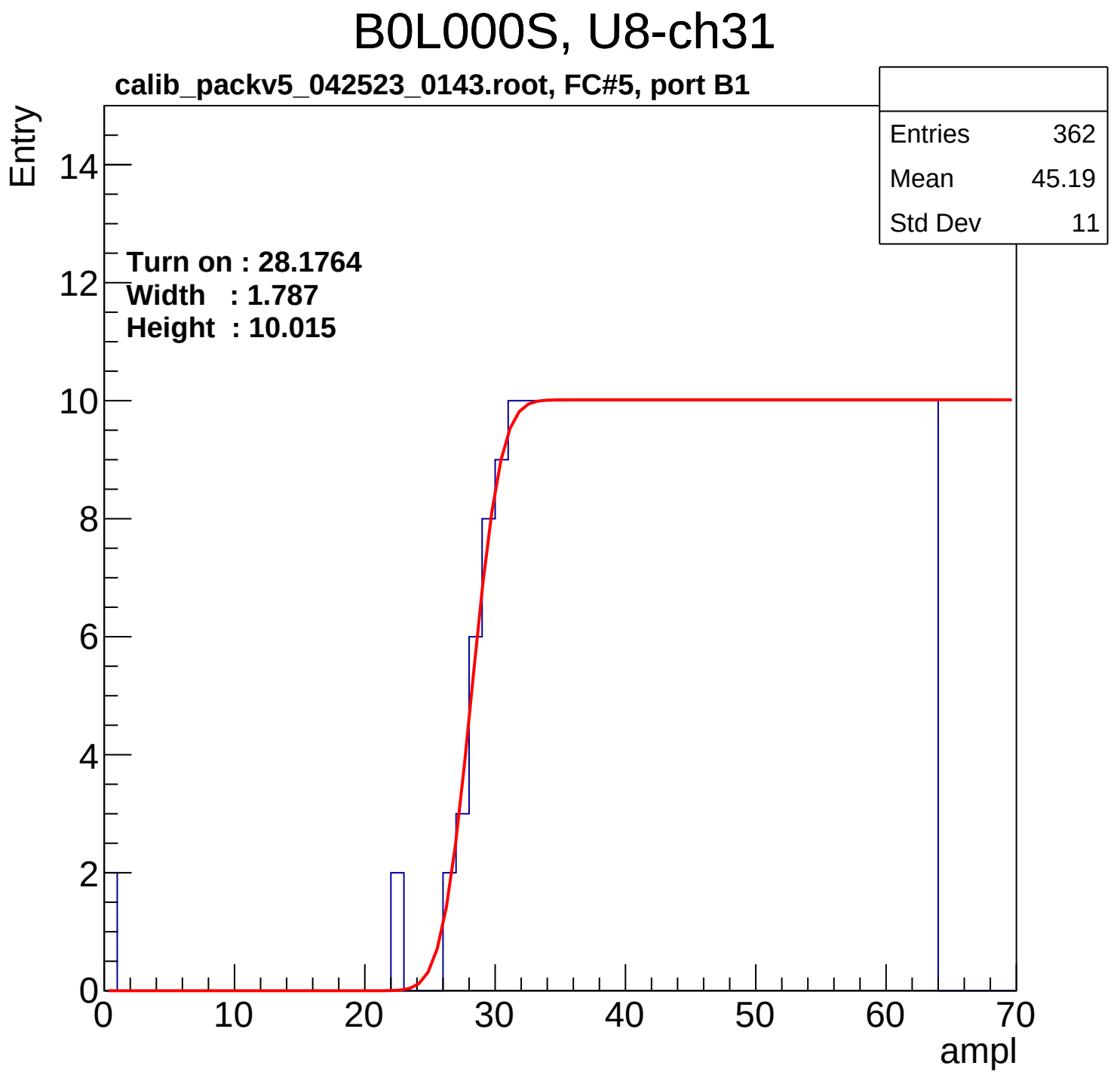
B0L000S, U8-ch31
calib_packv5_042523_0143.root, FC#5, port B1
Entries 362
Mean 45.19
Std Dev 11
Turn on : 28.1764
Width : 1.787
Height : 10.015
Entry
ampl
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2
4
6
8
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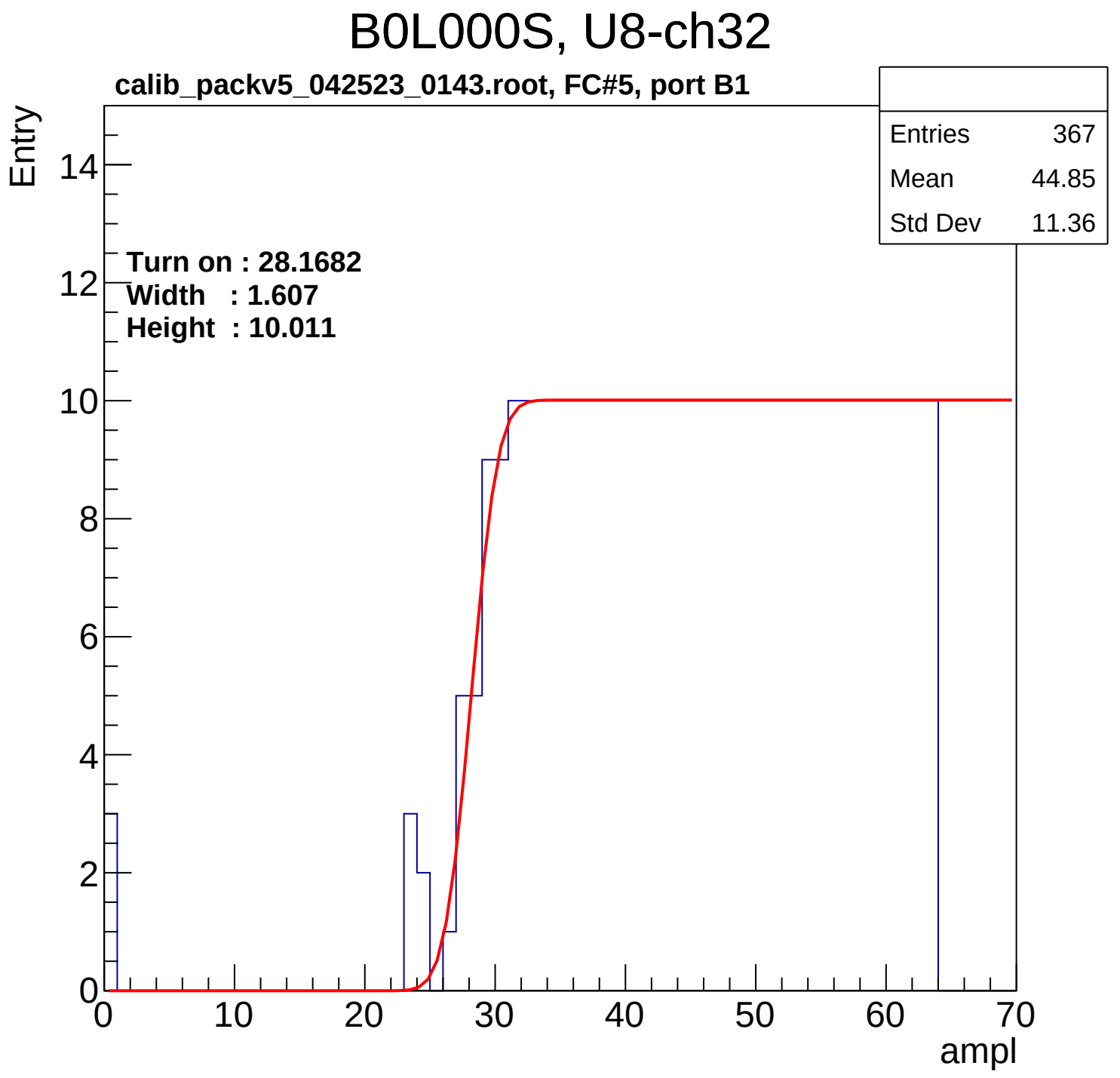
B0L000S, U8-ch32
calib_packv5_042523_0143.root, FC#5, port B1
Entries 367
Mean 44.85
Std Dev 11.36
Turn on : 28.1682
Width : 1.607
Height : 10.011
Entry
ampl
0
2
4
6
8
10
12
14
0
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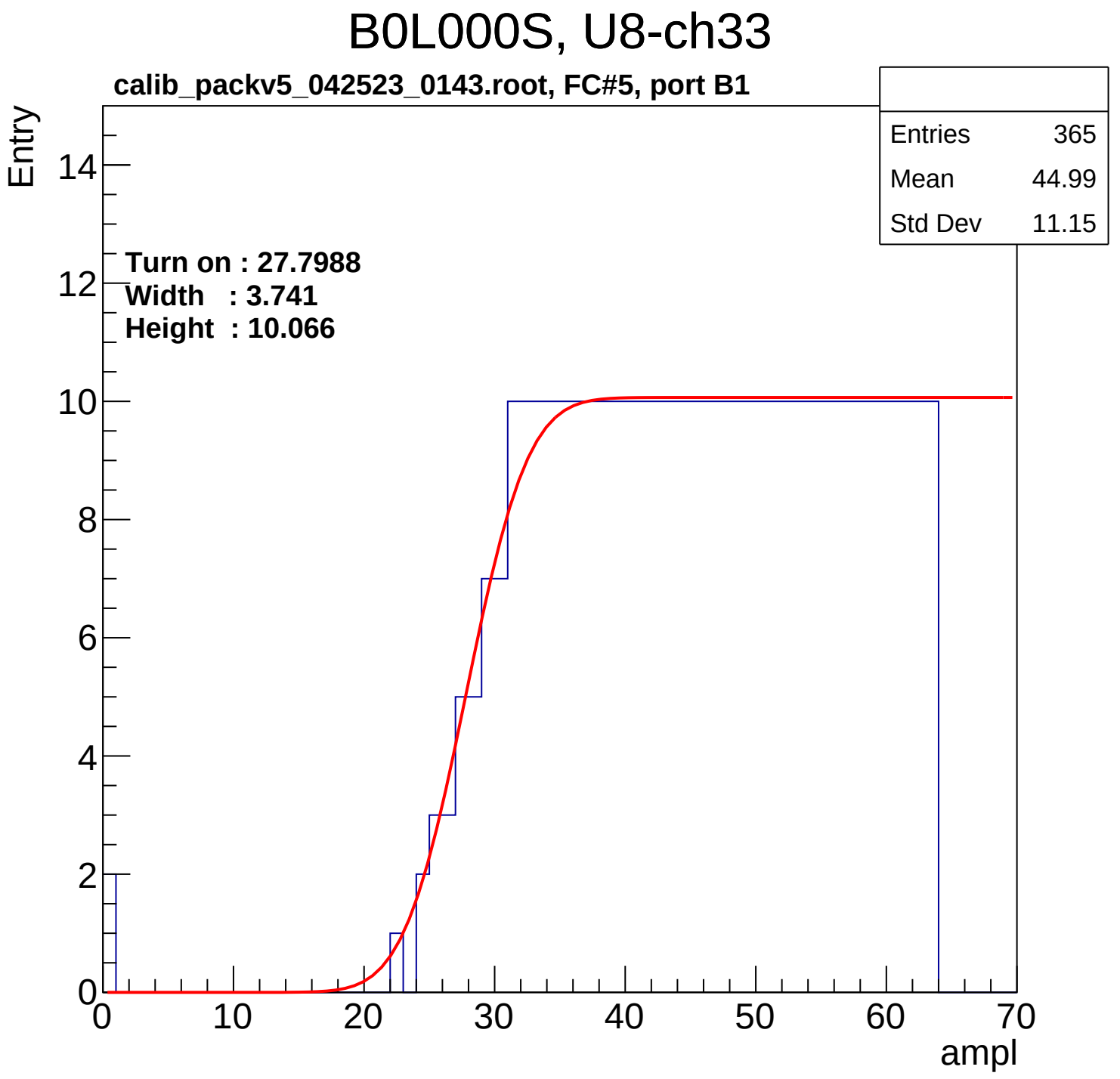
B0L000S, U8-ch33
calib_packv5_042523_0143.root, FC#5, port B1
Entries 365
Mean 44.99
Std Dev 11.15
Turn on : 27.7988
Width : 3.741
Height : 10.066
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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40
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60
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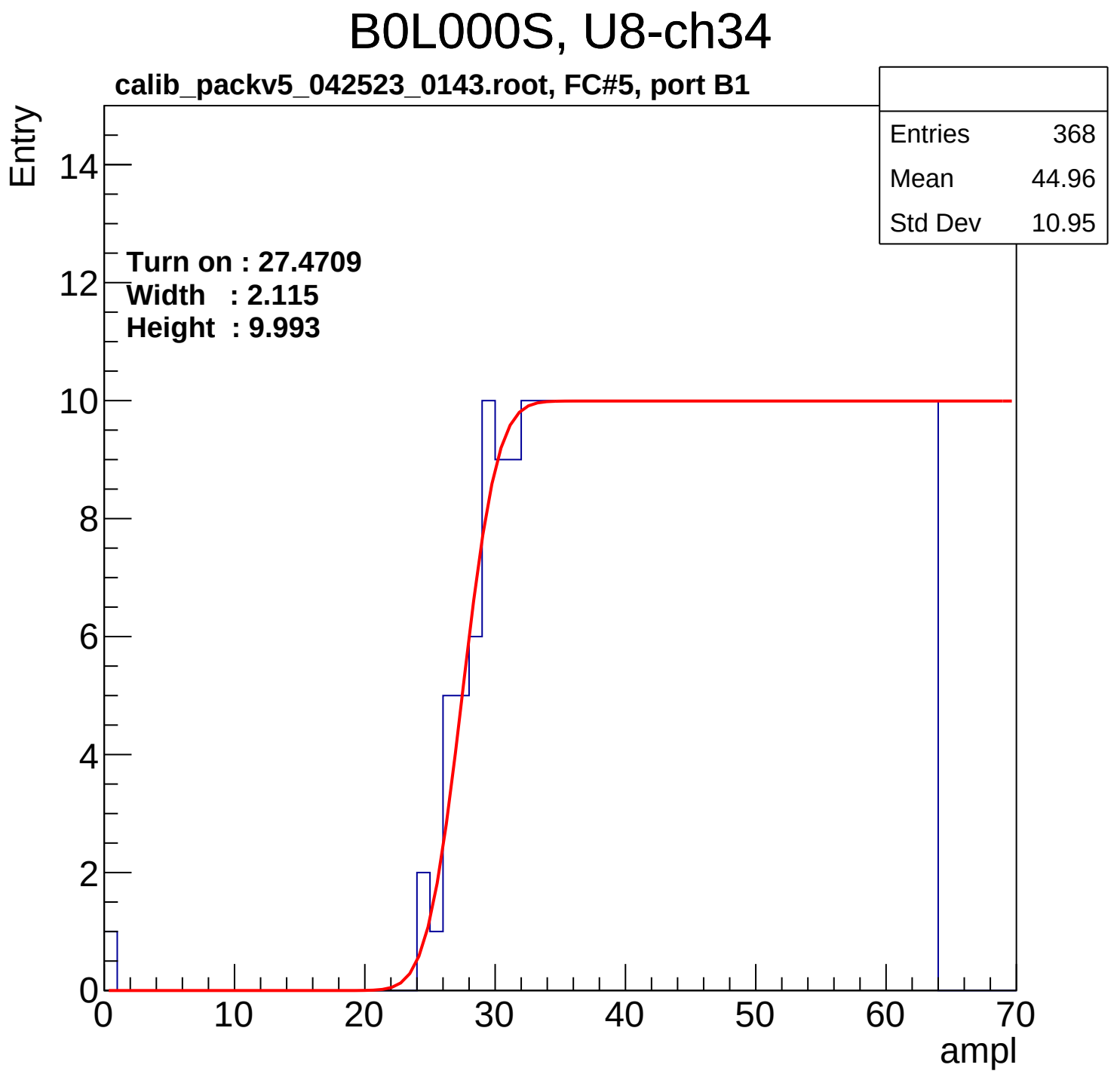
B0L000S, U8-ch34
calib_packv5_042523_0143.root, FC#5, port B1
Entries 368
Mean 44.96
Std Dev 10.95
Turn on : 27.4709
Width : 2.115
Height : 9.993
Entry
ampl
0
2
4
6
8
10
12
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0
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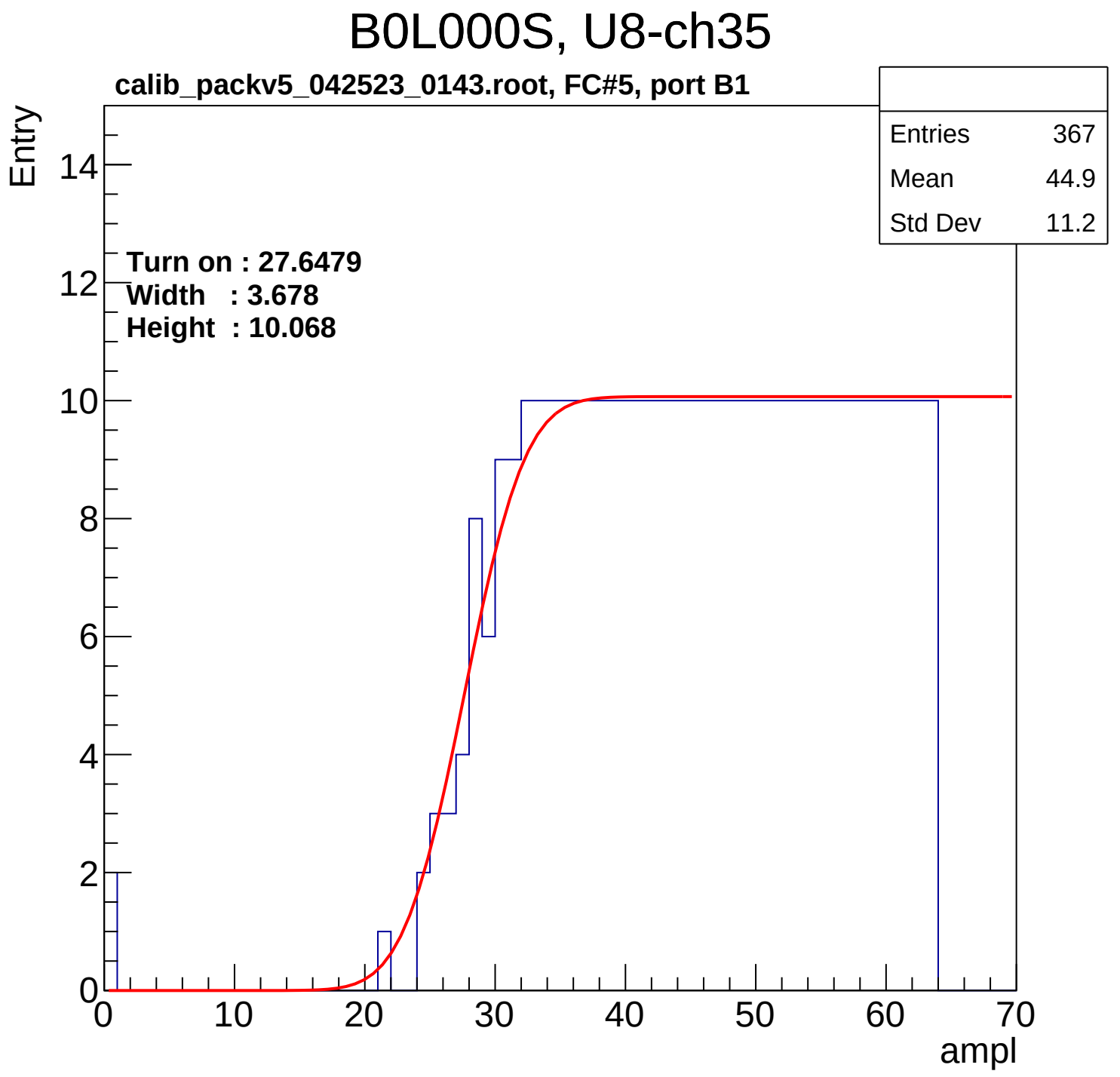
B0L000S, U8-ch35
calib_packv5_042523_0143.root, FC#5, port B1
Entries 367
Mean 44.9
Std Dev 11.2
Turn on : 27.6479
Width : 3.678
Height : 10.068
Entry
ampl
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2
4
6
8
10
12
14
0
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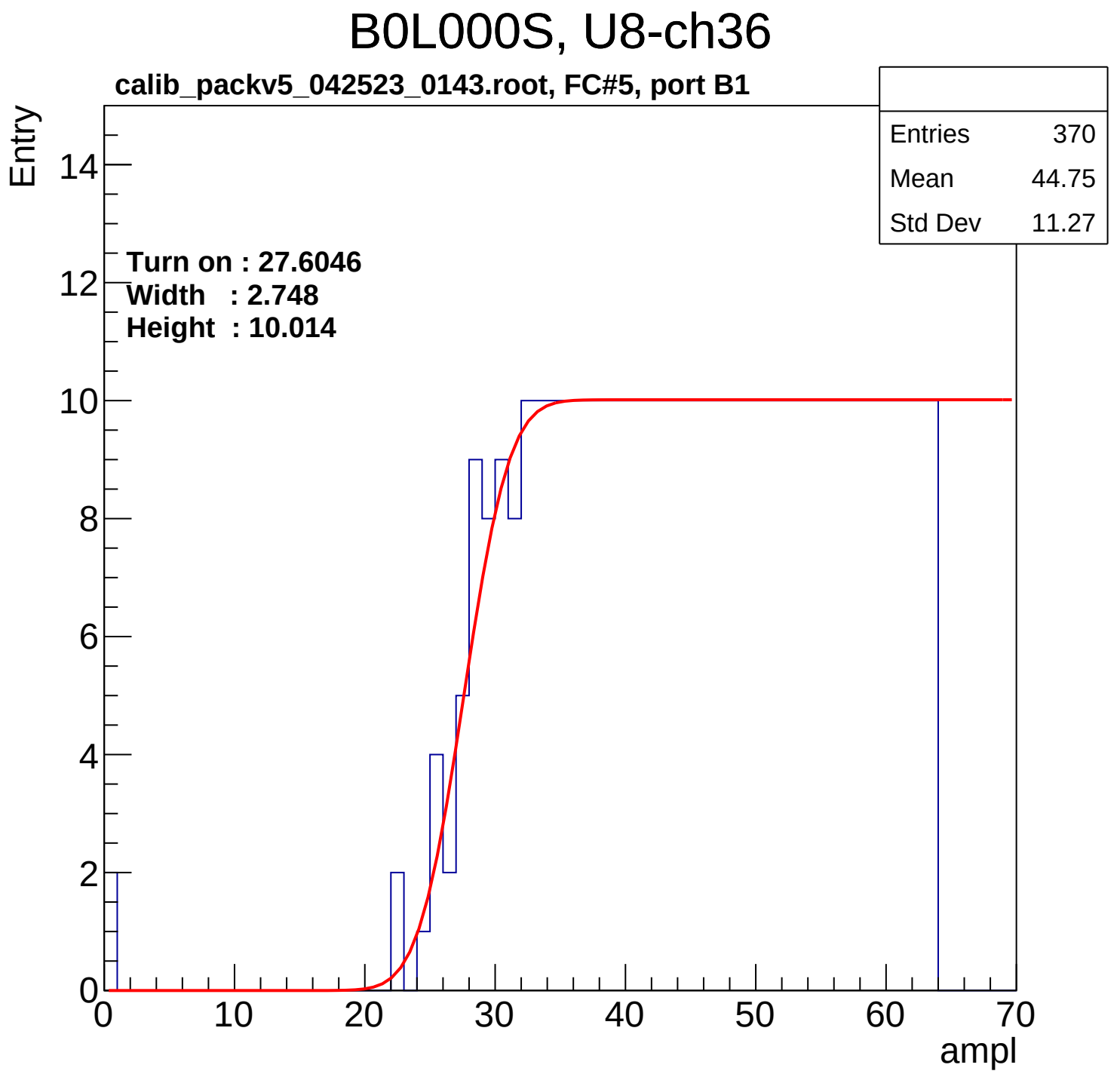
B0L000S, U8-ch36
calib_packv5_042523_0143.root, FC#5, port B1
Entries 370
Mean 44.75
Std Dev 11.27
Turn on : 27.6046
Width : 2.748
Height : 10.014
Entry
ampl
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2
4
6
8
10
12
14
0
10
20
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40
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60
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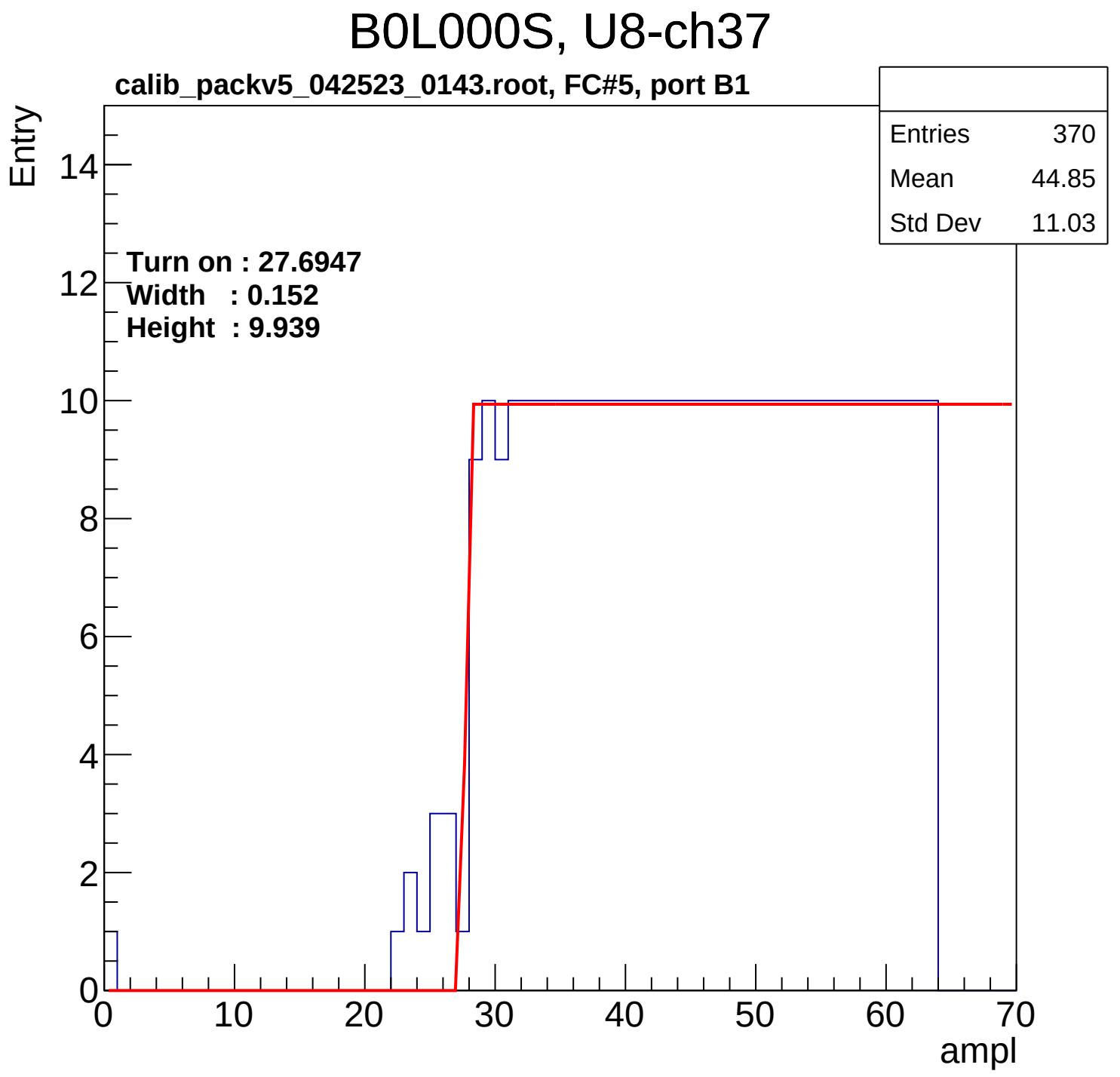
B0L000S, U8-ch37
calib_packv5_042523_0143.root, FC#5, port B1
Entries 370
Mean 44.85
Std Dev 11.03
Turn on : 27.6947
Width : 0.152
Height : 9.939
Entry
ampl
0
2
4
6
8
10
12
14
0
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20
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40
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60
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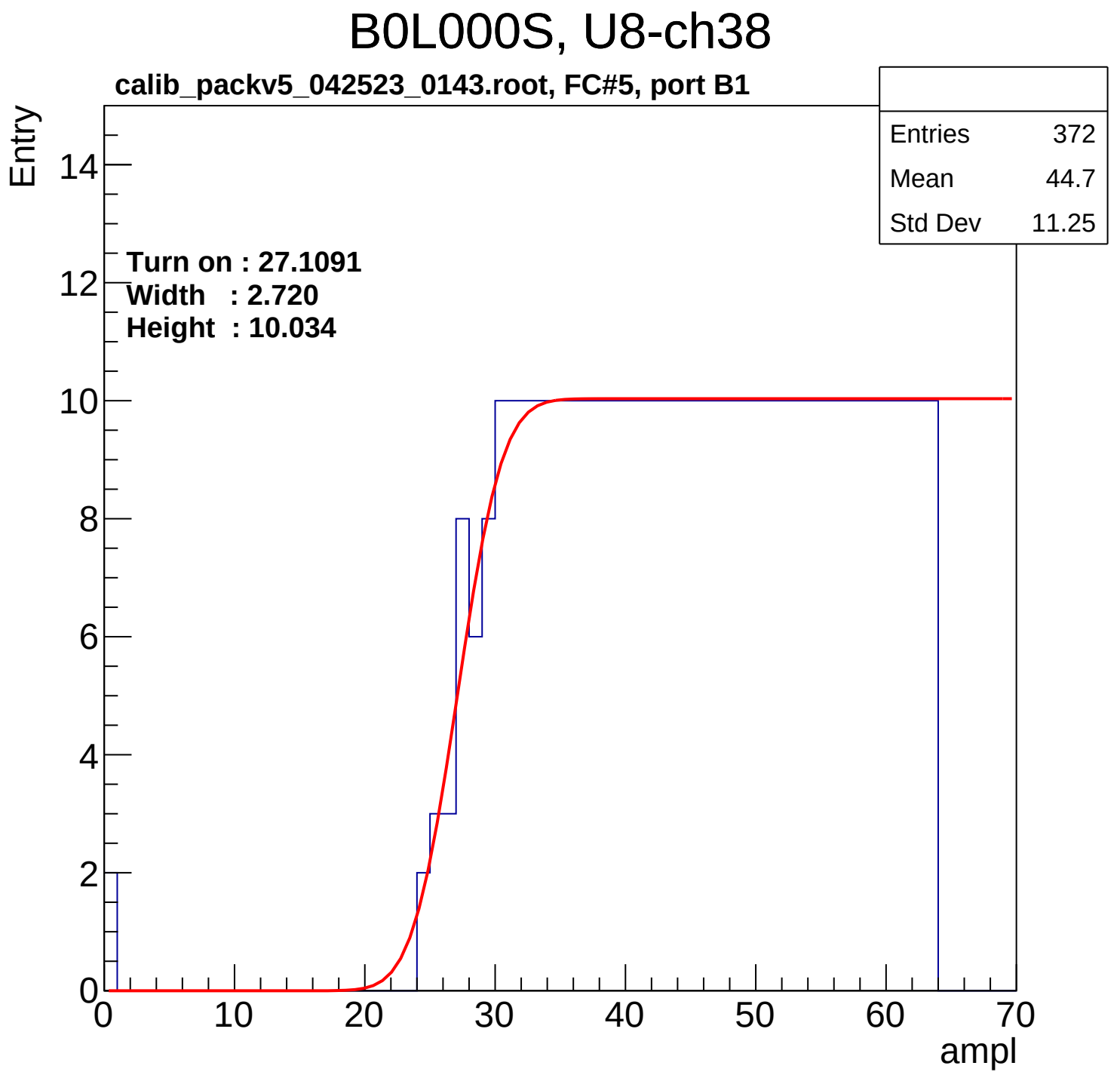
B0L000S, U8-ch38
calib_packv5_042523_0143.root, FC#5, port B1
Entries 372
Mean 44.7
Std Dev 11.25
Turn on : 27.1091
Width : 2.720
Height : 10.034
Entry
ampl
0
2
4
6
8
10
12
14
0
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20
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40
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60
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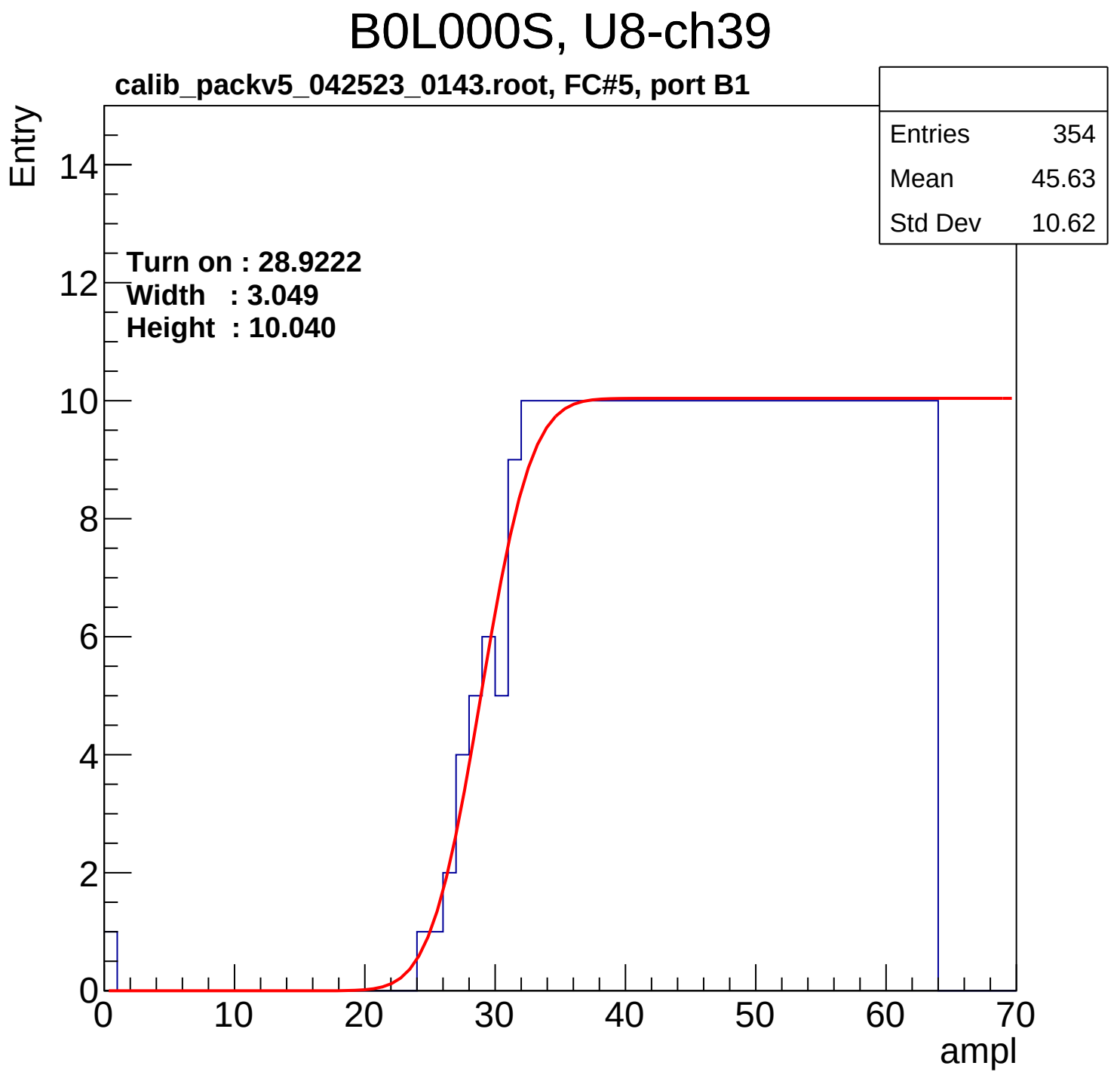
B0L000S, U8-ch39
calib_packv5_042523_0143.root, FC#5, port B1
Entries 354
Mean 45.63
Std Dev 10.62
Turn on : 28.9222
Width : 3.049
Height : 10.040
Entry
ampl
0
2
4
6
8
10
12
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0
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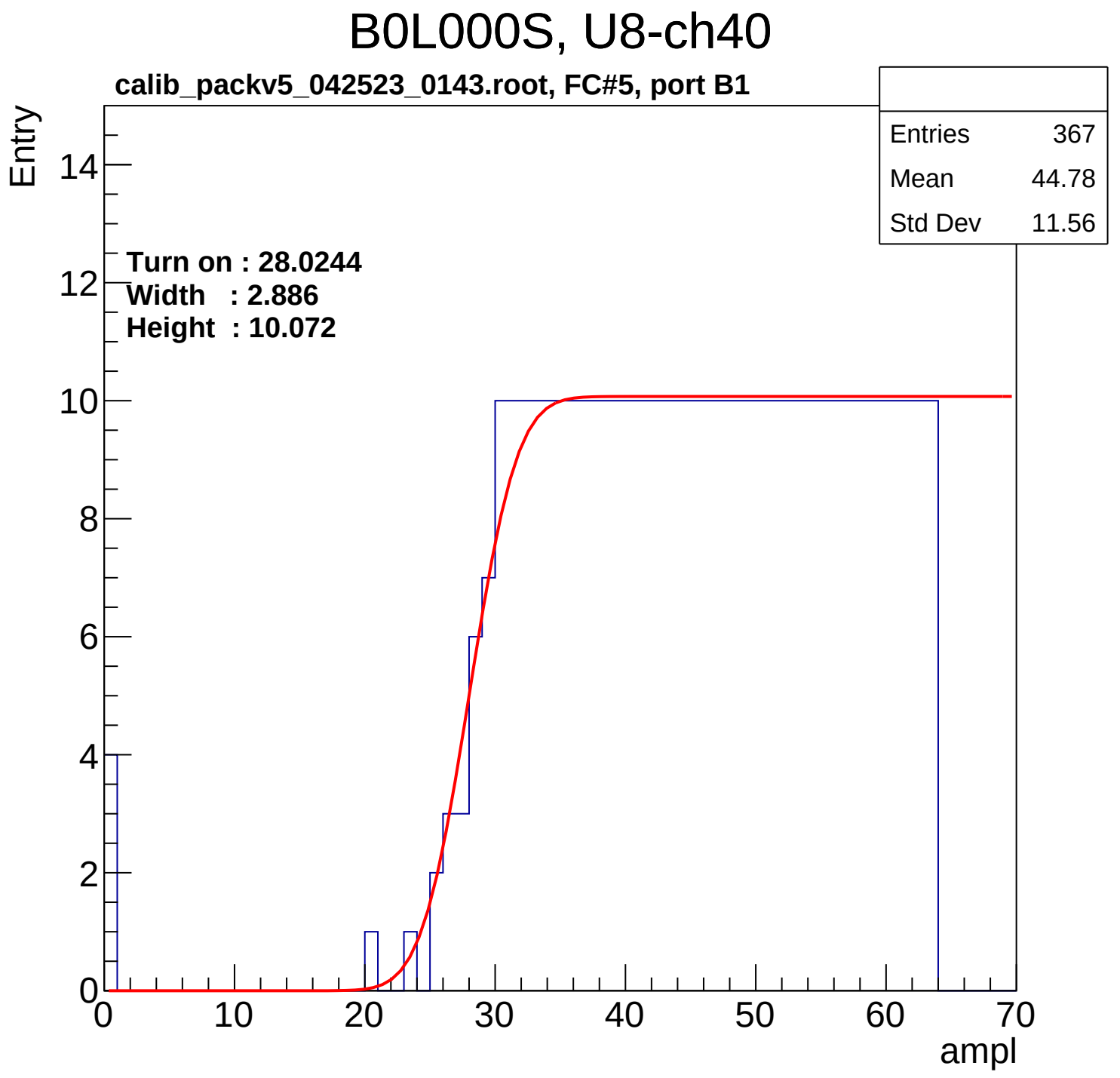
B0L000S, U8-ch40
calib_packv5_042523_0143.root, FC#5, port B1
Entries 367
Mean 44.78
Std Dev 11.56
Turn on : 28.0244
Width : 2.886
Height : 10.072
Entry
ampl
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4
6
8
10
12
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0
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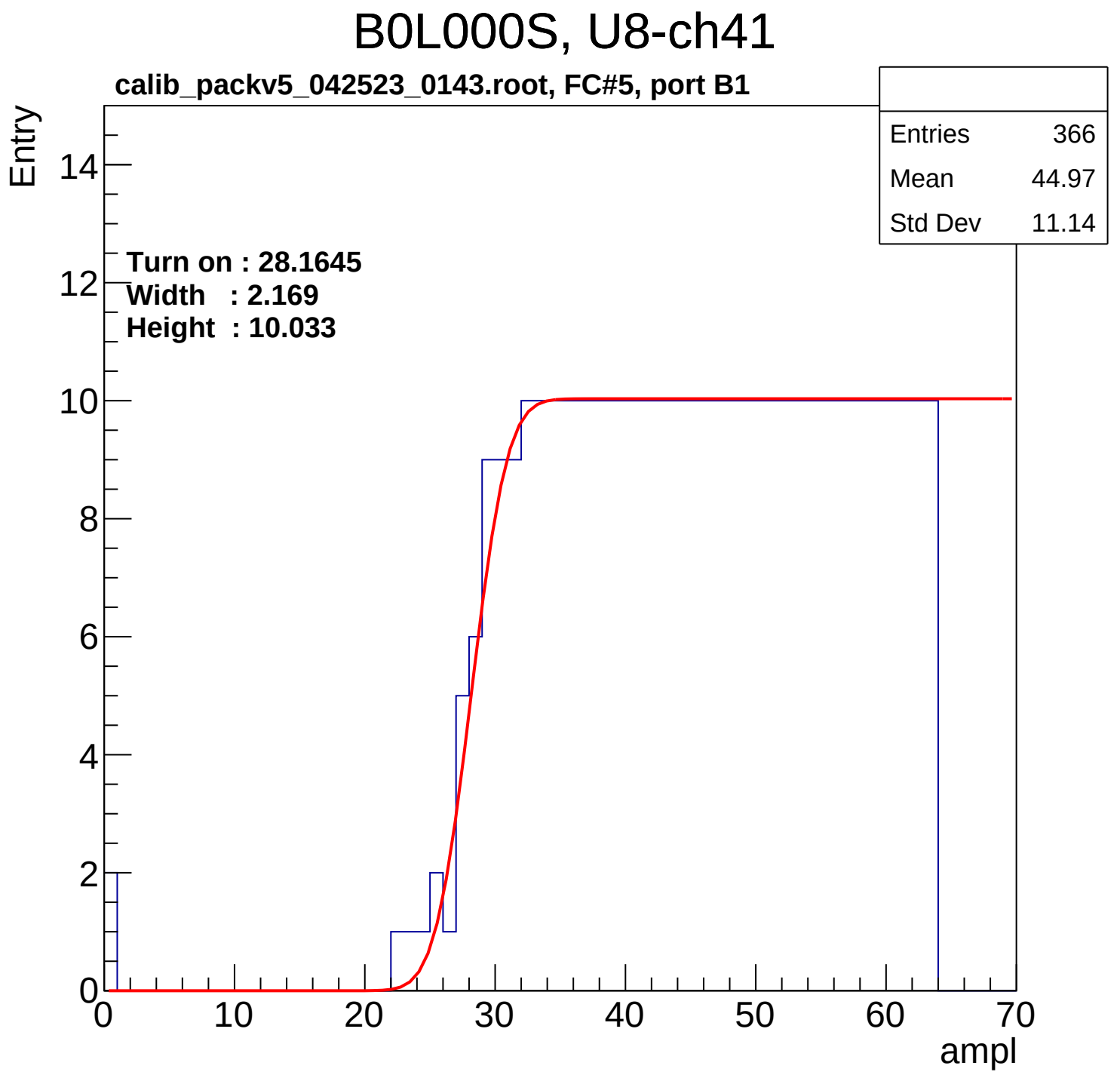
B0L000S, U8-ch41
calib_packv5_042523_0143.root, FC#5, port B1
Entries 366
Mean 44.97
Std Dev 11.14
Turn on : 28.1645
Width : 2.169
Height : 10.033
Entry
ampl
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2
4
6
8
10
12
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0
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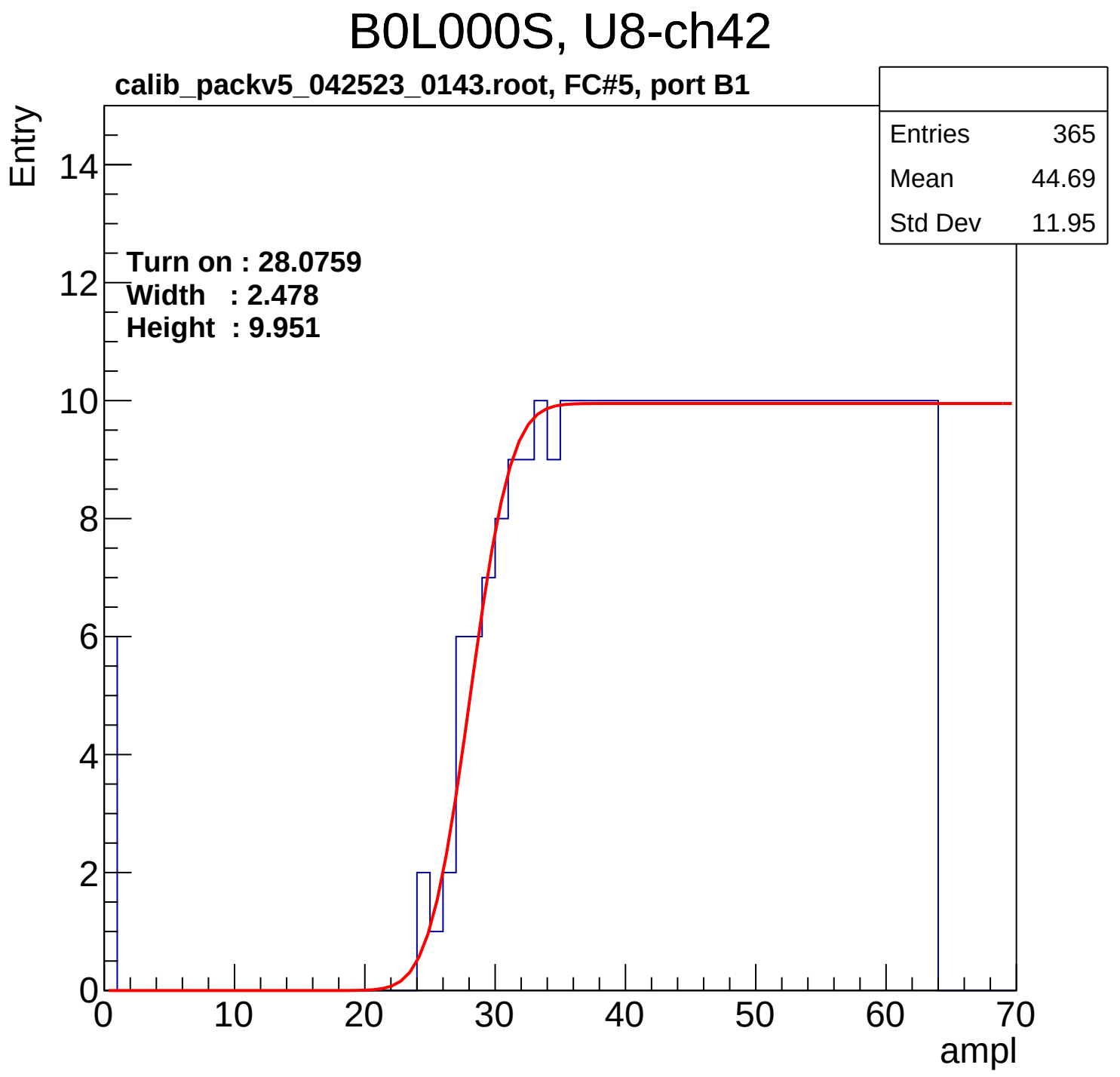
B0L000S, U8-ch42
calib_packv5_042523_0143.root, FC#5, port B1
Entries 365
Mean 44.69
Std Dev 11.95
Turn on : 28.0759
Width : 2.478
Height : 9.951
Entry
ampl
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2
4
6
8
10
12
14
0
10
20
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40
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60
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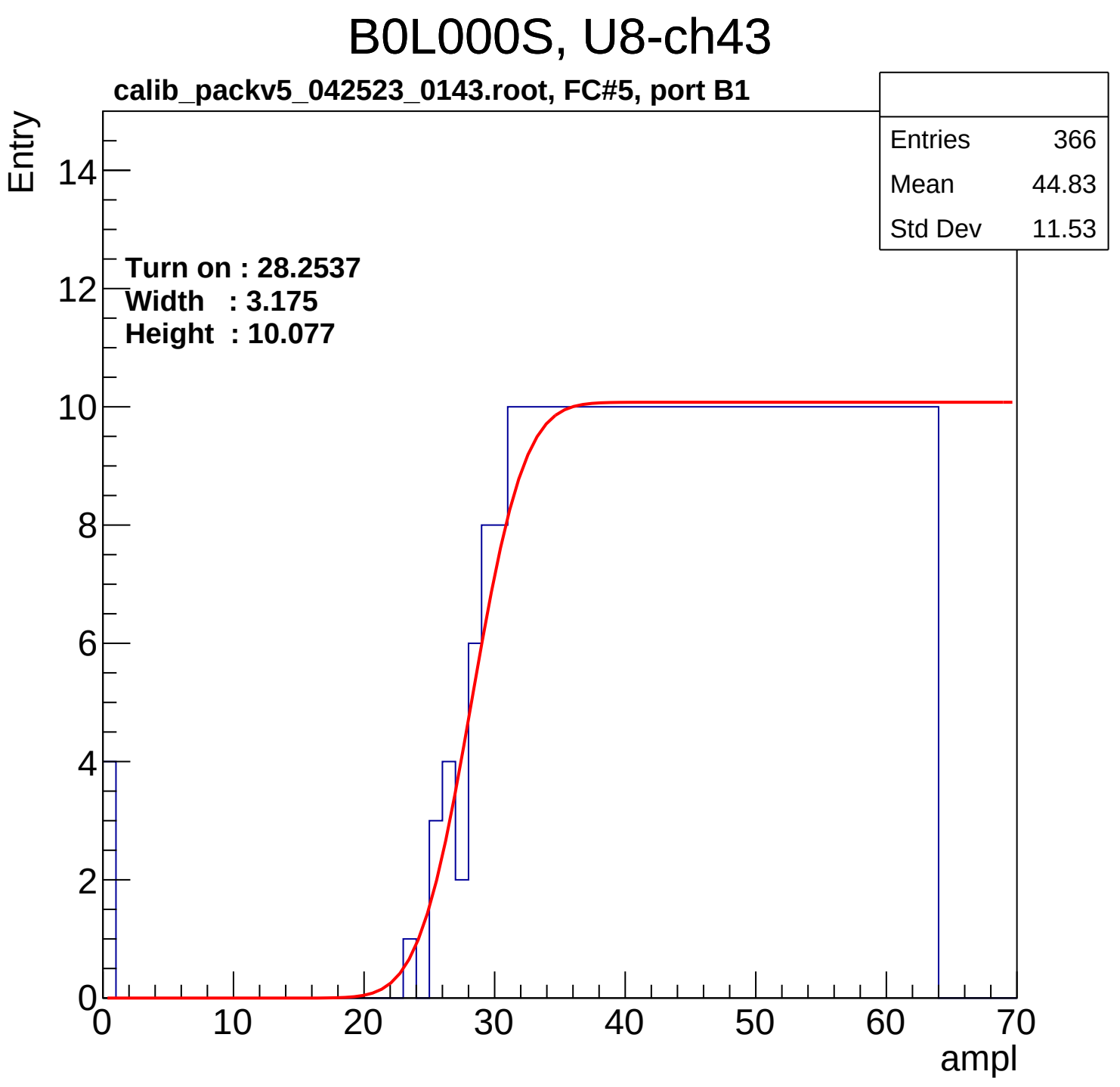
B0L000S, U8-ch43
calib_packv5_042523_0143.root, FC#5, port B1
Entries 366
Mean 44.83
Std Dev 11.53
Turn on : 28.2537
Width : 3.175
Height : 10.077
Entry
ampl
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6
8
10
12
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0
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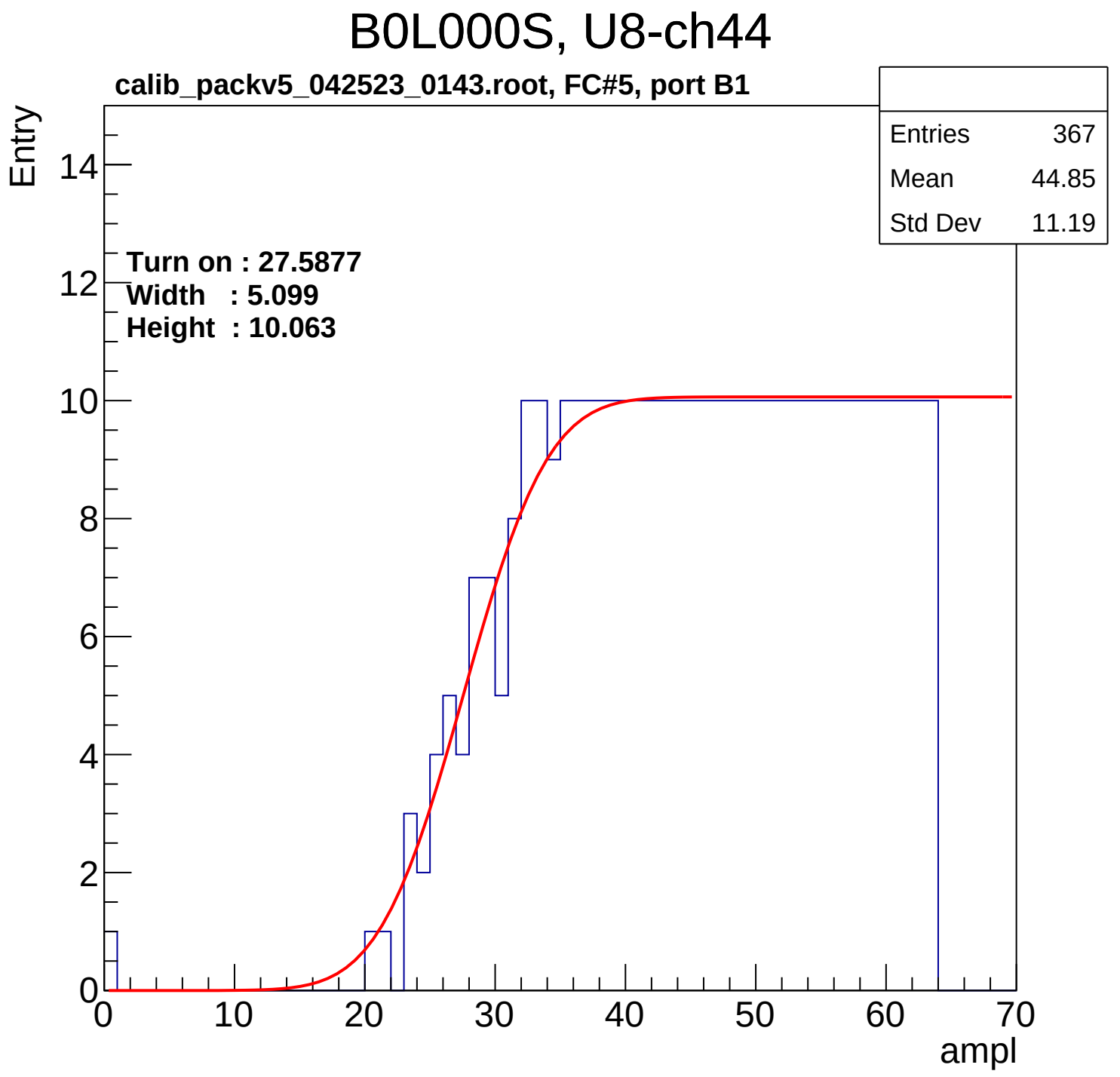
B0L000S, U8-ch44
calib_packv5_042523_0143.root, FC#5, port B1
Entries 367
Mean 44.85
Std Dev 11.19
Turn on : 27.5877
Width : 5.099
Height : 10.063
Entry
ampl
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6
8
10
12
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0
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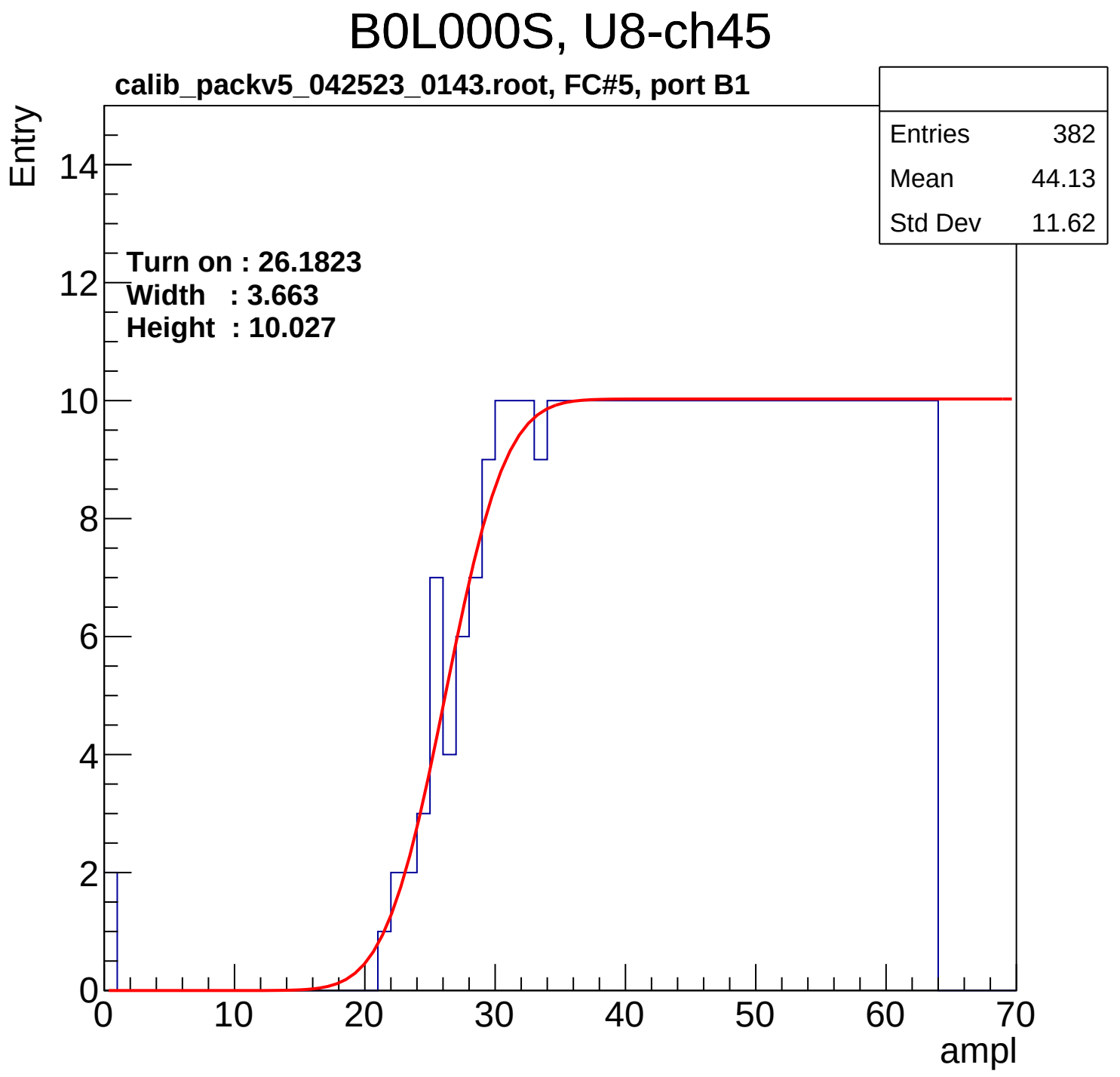
B0L000S, U8-ch45
calib_packv5_042523_0143.root, FC#5, port B1
Entries 382
Mean 44.13
Std Dev 11.62
Turn on : 26.1823
Width : 3.663
Height : 10.027
Entry
ampl
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6
8
10
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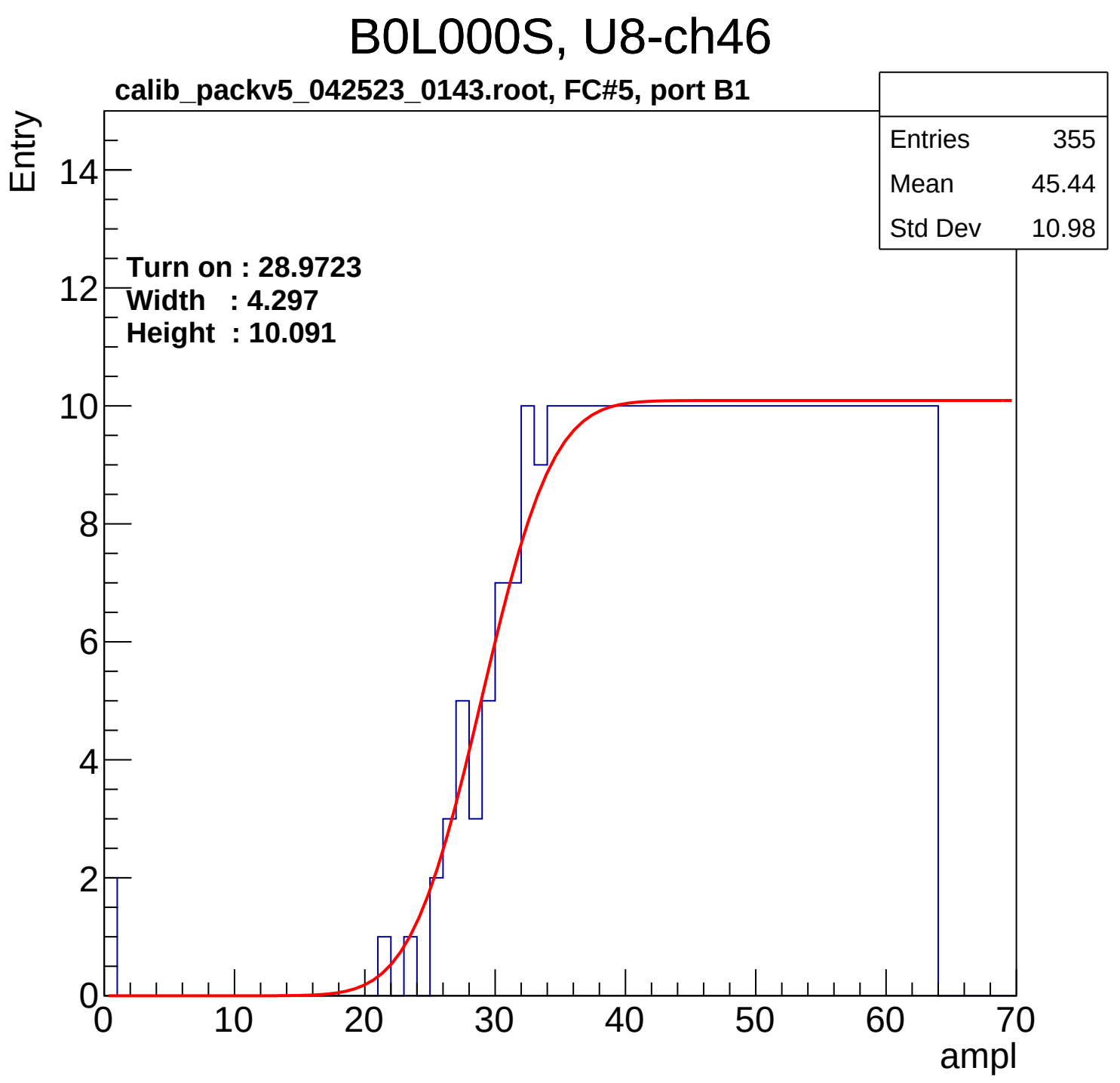
B0L000S, U8-ch46
calib_packv5_042523_0143.root, FC#5, port B1
Entries 355
Mean 45.44
Std Dev 10.98
Turn on : 28.9723
Width : 4.297
Height : 10.091
Entry
ampl
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6
8
10
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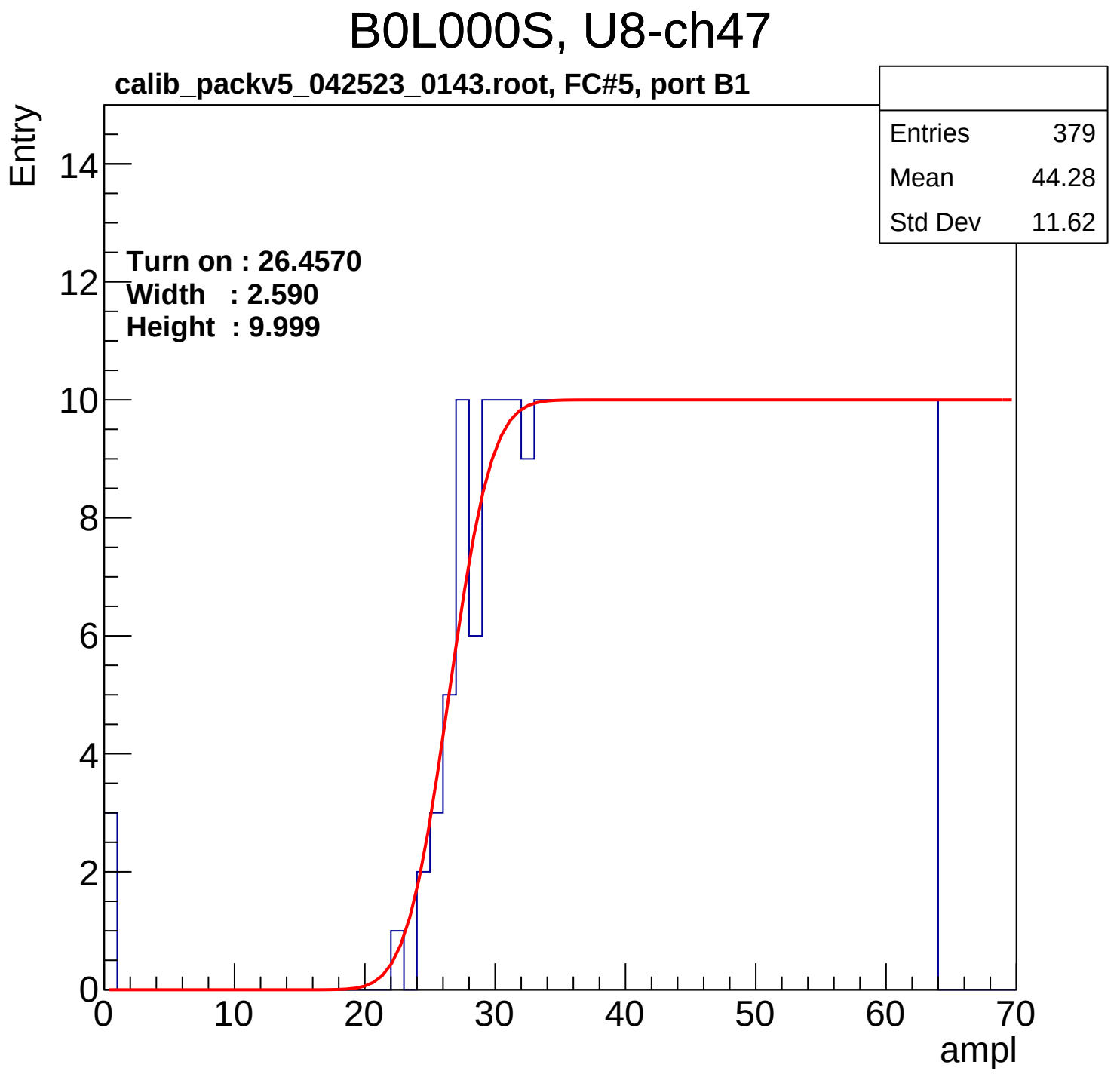
B0L000S, U8-ch47
calib_packv5_042523_0143.root, FC#5, port B1
Entries 379
Mean 44.28
Std Dev 11.62
Turn on : 26.4570
Width : 2.590
Height : 9.999
Entry
ampl
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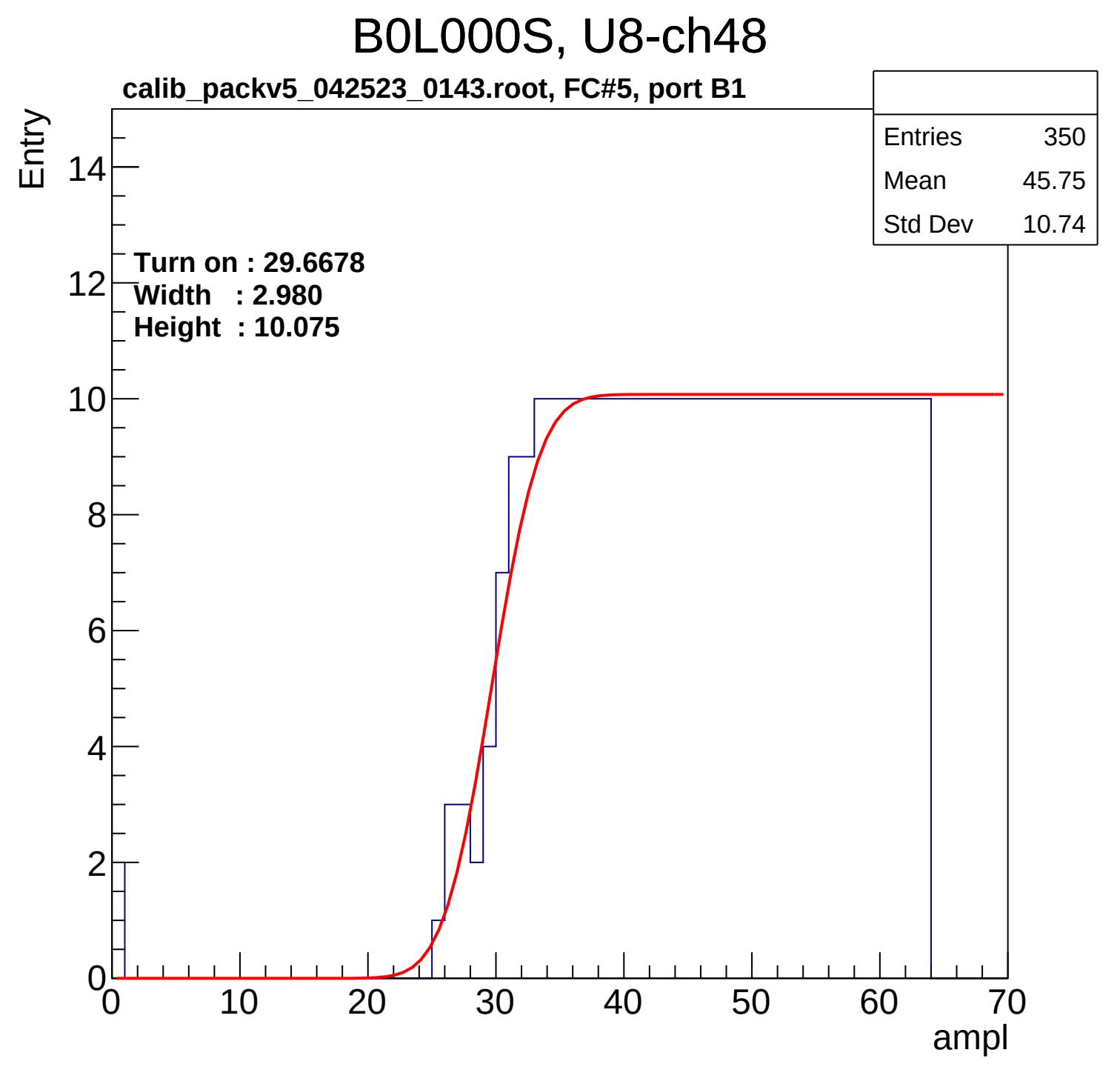
B0L000S, U8-ch48
calib_packv5_042523_0143.root, FC#5, port B1
Entries 350
Mean 45.75
Std Dev 10.74
Turn on : 29.6678
Width : 2.980
Height : 10.075
Entry
ampl
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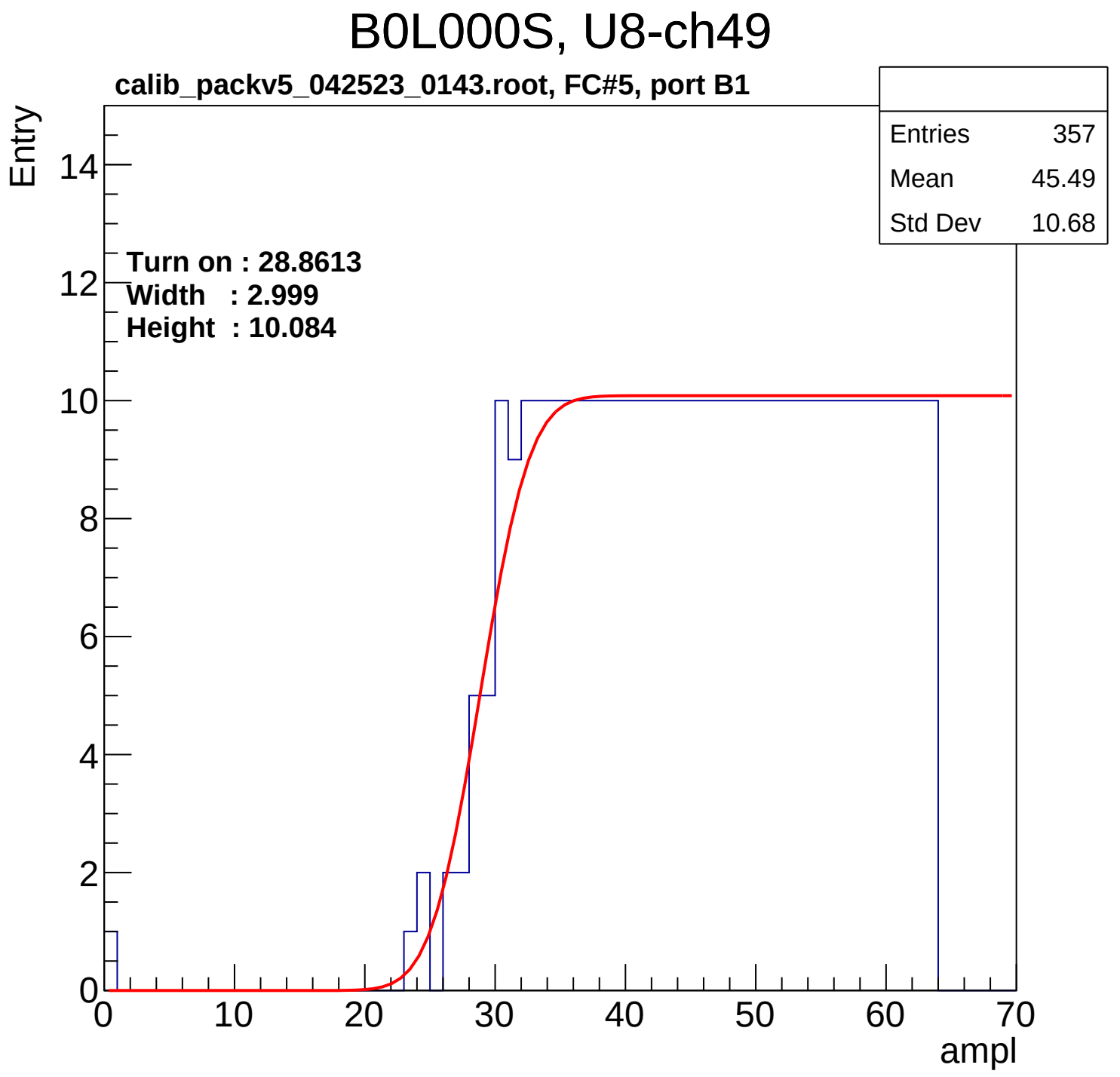
B0L000S, U8-ch49
calib_packv5_042523_0143.root, FC#5, port B1
Entries 357
Mean 45.49
Std Dev 10.68
Turn on : 28.8613
Width : 2.999
Height : 10.084
Entry
ampl
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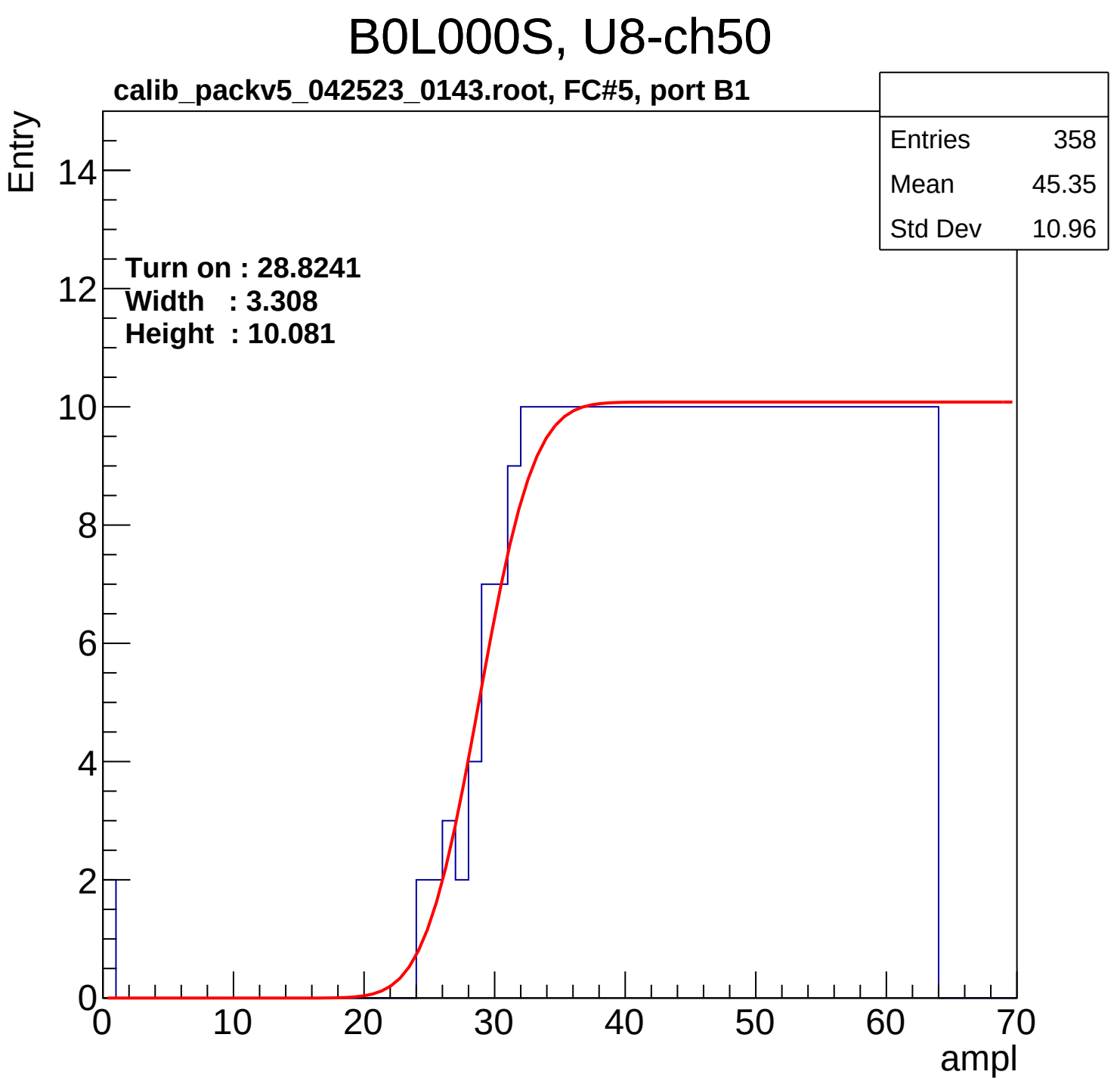
B0L000S, U8-ch50
calib_packv5_042523_0143.root, FC#5, port B1
Entries 358
Mean 45.35
Std Dev 10.96
Turn on : 28.8241
Width : 3.308
Height : 10.081
Entry
ampl
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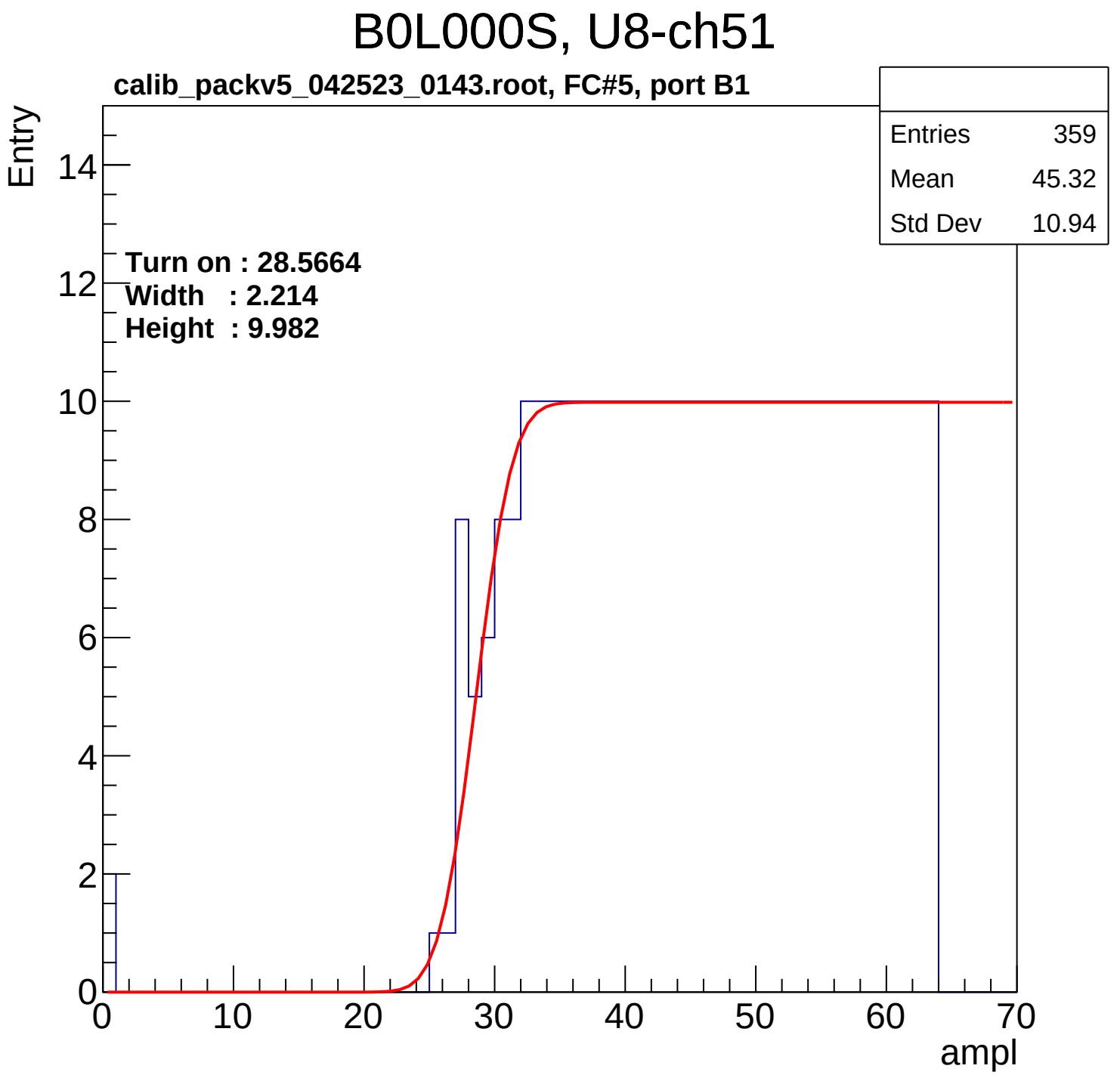
B0L000S, U8-ch51
calib_packv5_042523_0143.root, FC#5, port B1
Entries 359
Mean 45.32
Std Dev 10.94
Turn on : 28.5664
Width : 2.214
Height : 9.982
Entry
ampl
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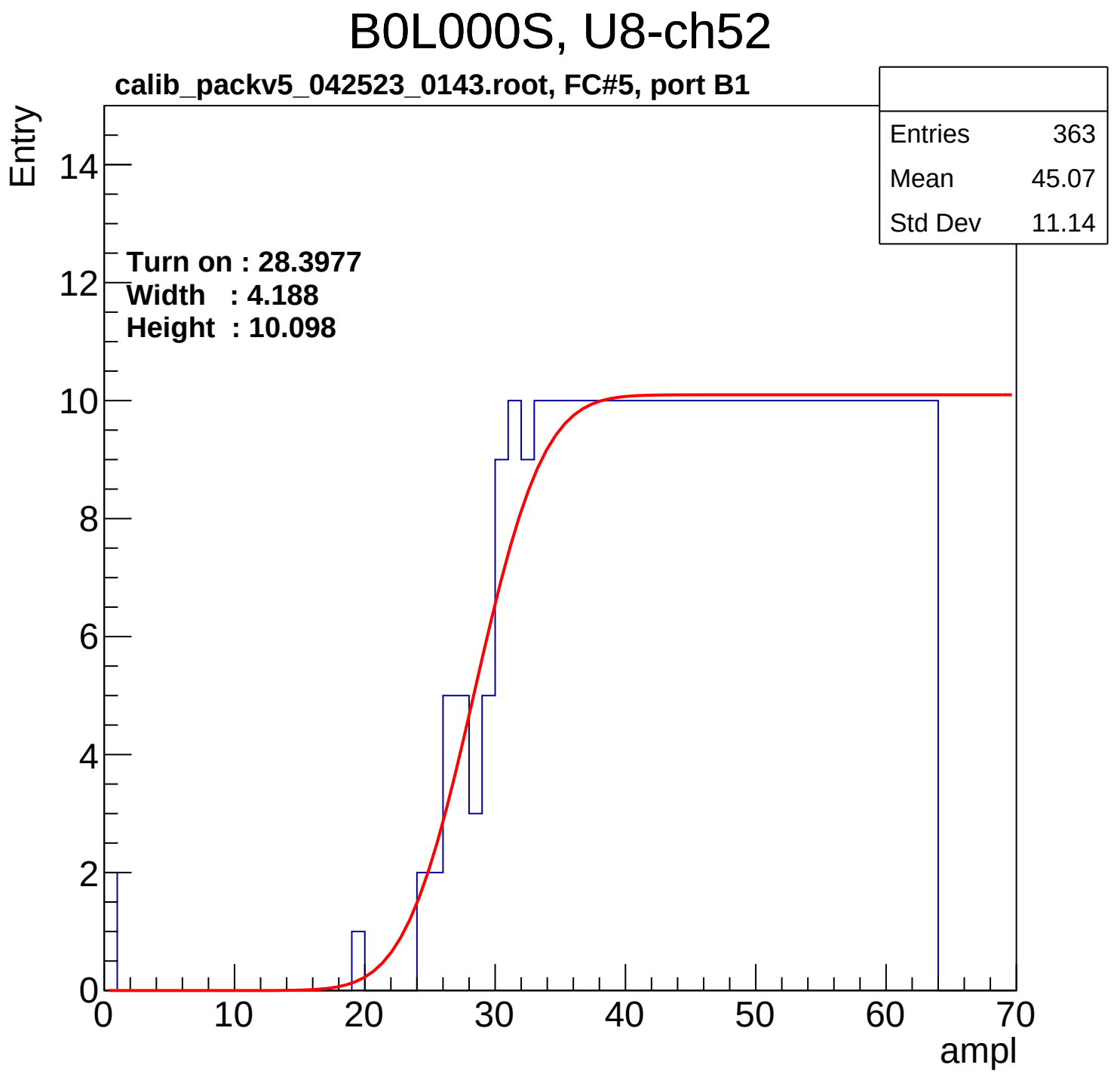
B0L000S, U8-ch52
calib_packv5_042523_0143.root, FC#5, port B1
Entries 363
Mean 45.07
Std Dev 11.14
Turn on : 28.3977
Width : 4.188
Height : 10.098
Entry
ampl
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6
8
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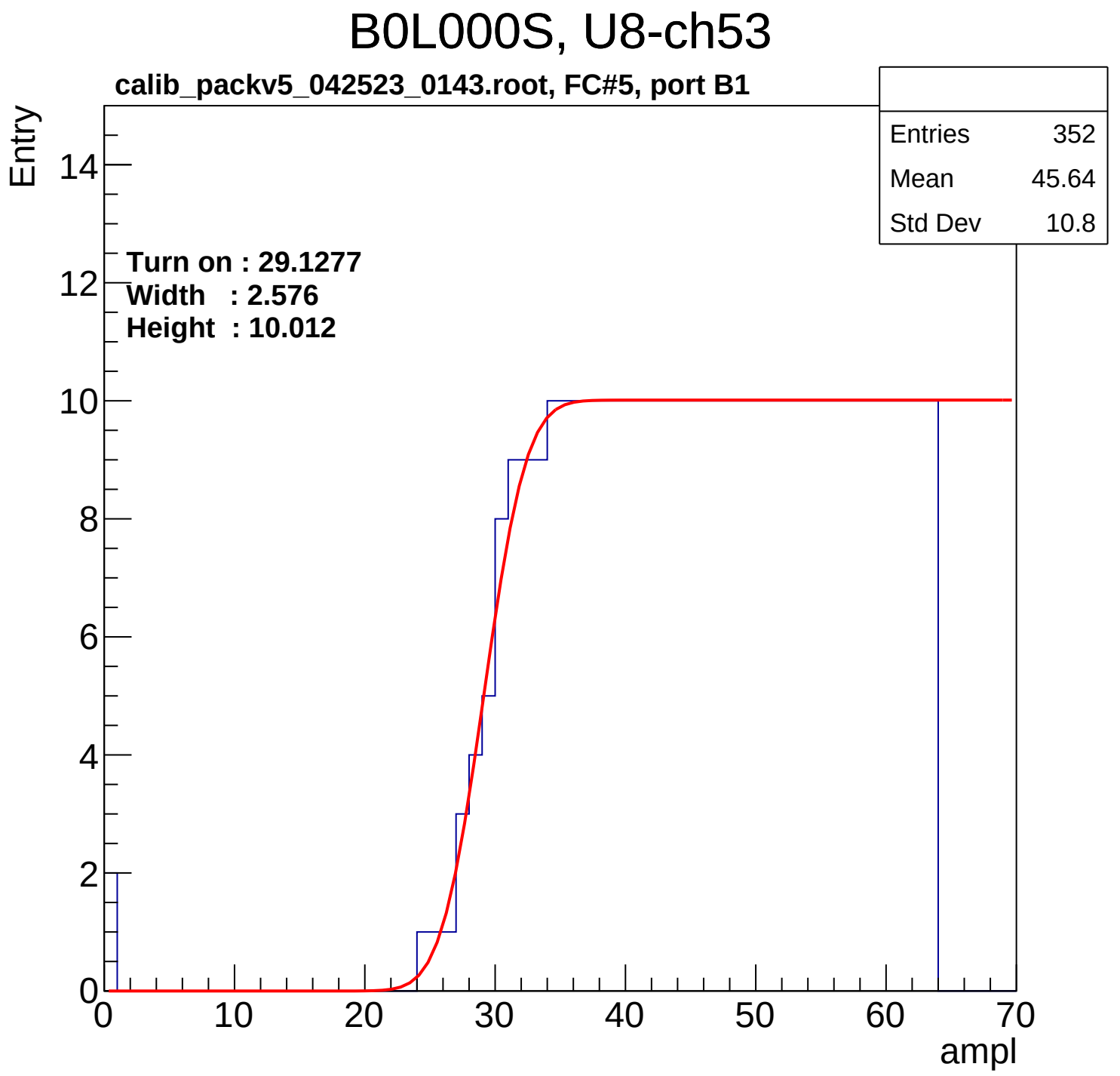
B0L000S, U8-ch53
calib_packv5_042523_0143.root, FC#5, port B1
Entries 352
Mean 45.64
Std Dev 10.8
Turn on : 29.1277
Width : 2.576
Height : 10.012
Entry
ampl
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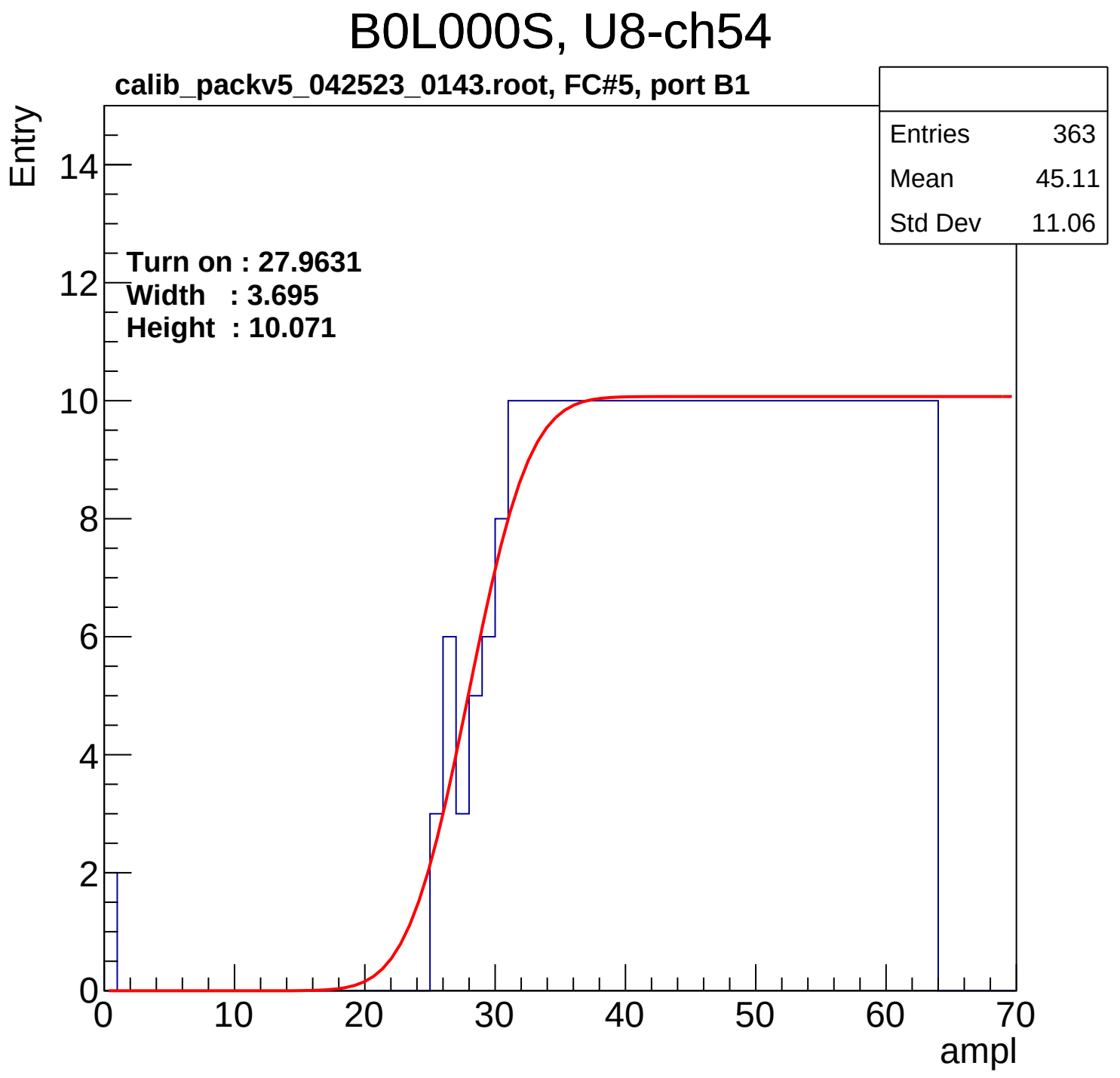
B0L000S, U8-ch54
calib_packv5_042523_0143.root, FC#5, port B1
Entries 363
Mean 45.11
Std Dev 11.06
Turn on : 27.9631
Width : 3.695
Height : 10.071
Entry
ampl
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4
6
8
10
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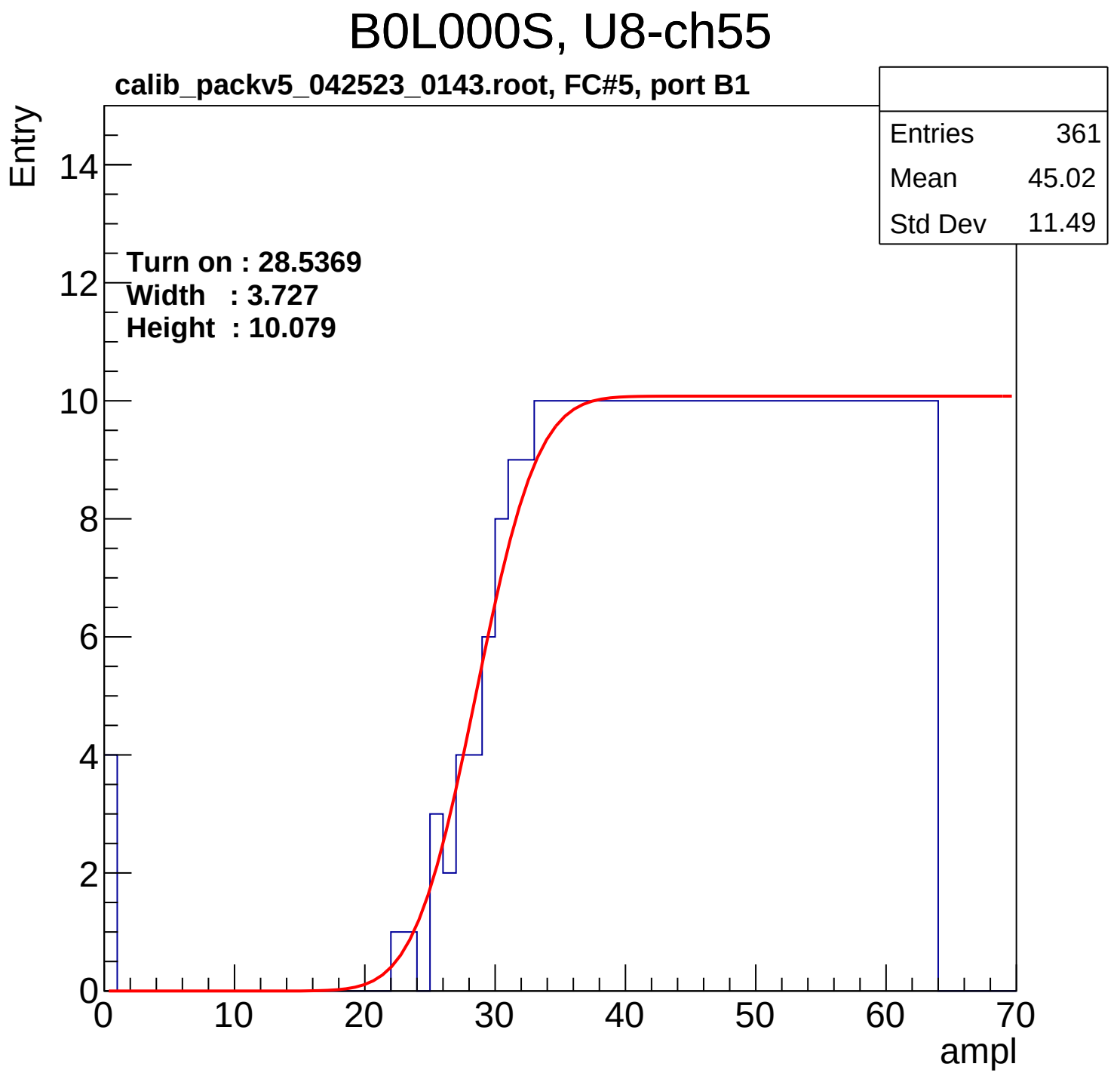
B0L000S, U8-ch55
calib_packv5_042523_0143.root, FC#5, port B1
Entries 361
Mean 45.02
Std Dev 11.49
Turn on : 28.5369
Width : 3.727
Height : 10.079
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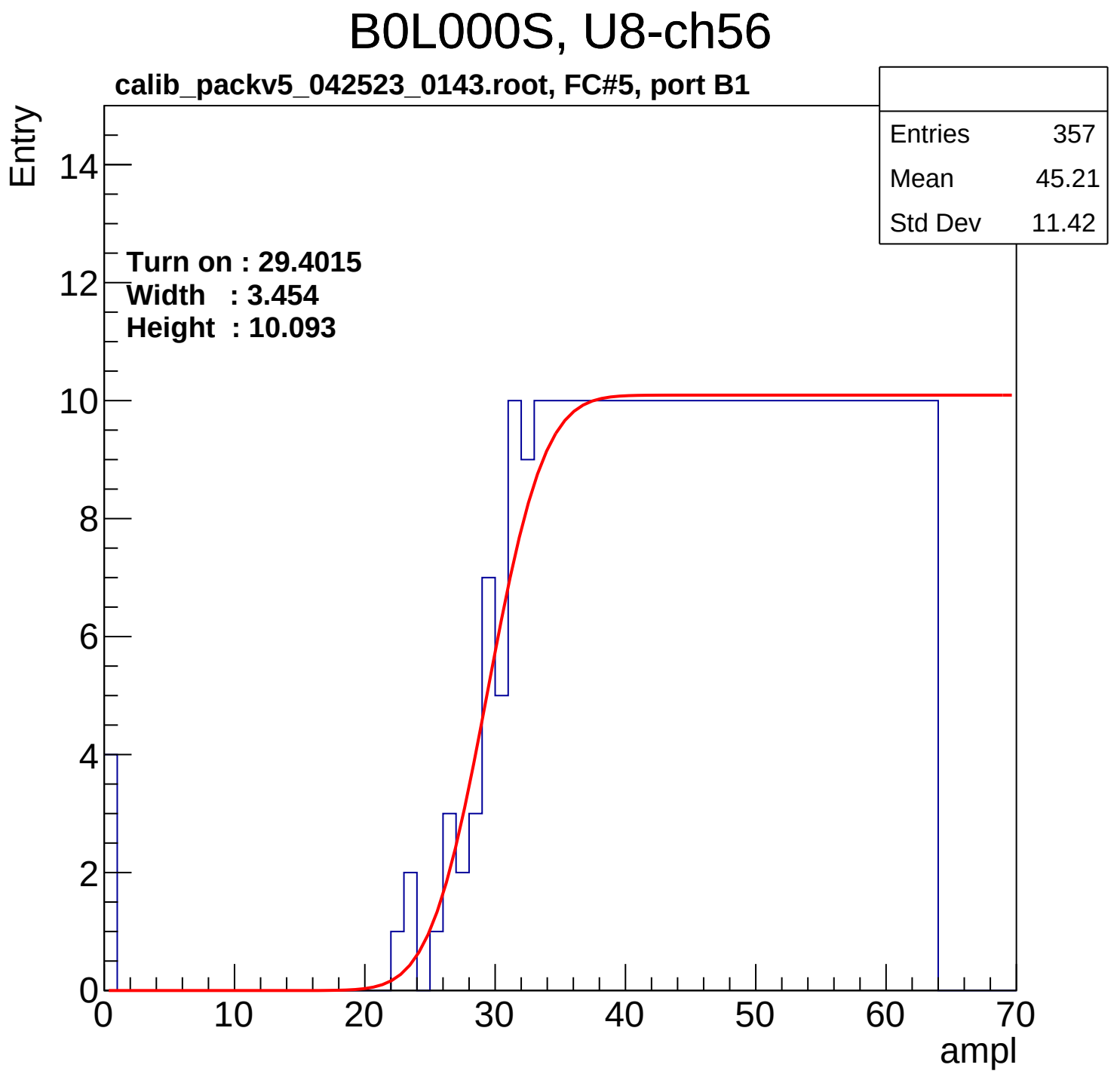
B0L000S, U8-ch56
calib_packv5_042523_0143.root, FC#5, port B1
Entries 357
Mean 45.21
Std Dev 11.42
Turn on : 29.4015
Width : 3.454
Height : 10.093
Entry
ampl
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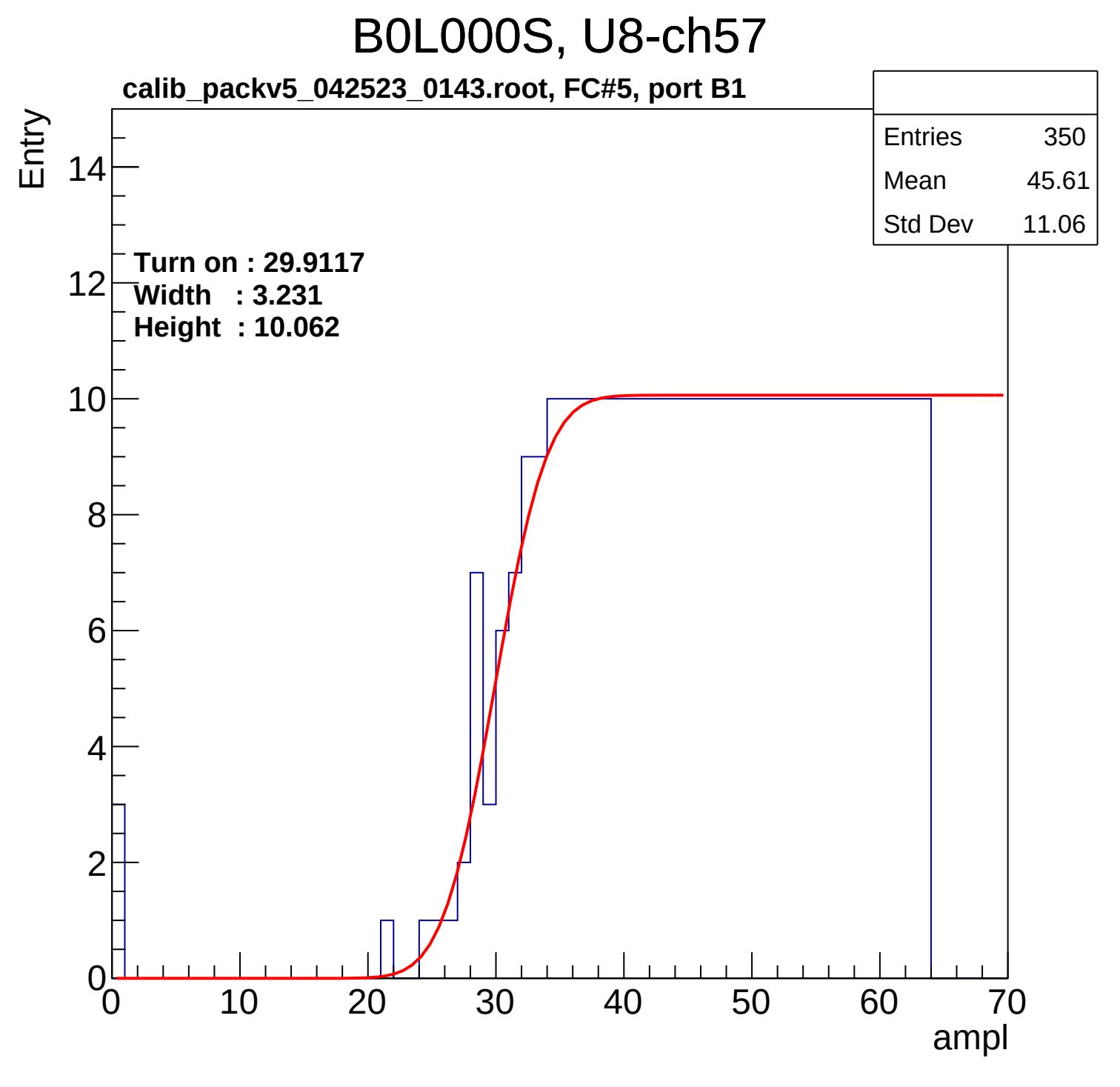
B0L000S, U8-ch57
calib_packv5_042523_0143.root, FC#5, port B1
Entries 350
Mean 45.61
Std Dev 11.06
Turn on : 29.9117
Width : 3.231
Height : 10.062
Entry
ampl
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4
6
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20
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40
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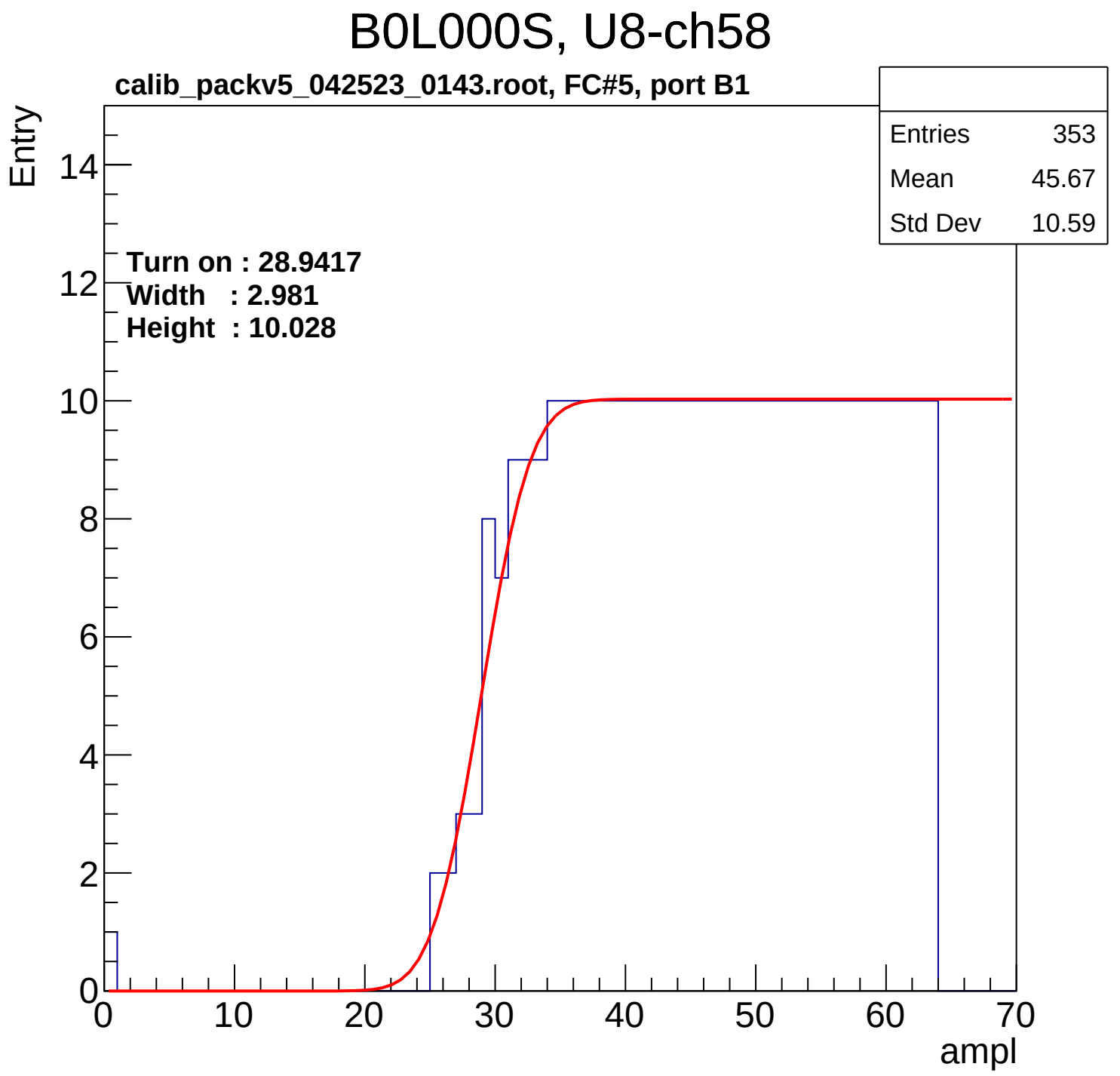
B0L000S, U8-ch58
calib_packv5_042523_0143.root, FC#5, port B1
Entries 353
Mean 45.67
Std Dev 10.59
Turn on : 28.9417
Width : 2.981
Height : 10.028
Entry
ampl
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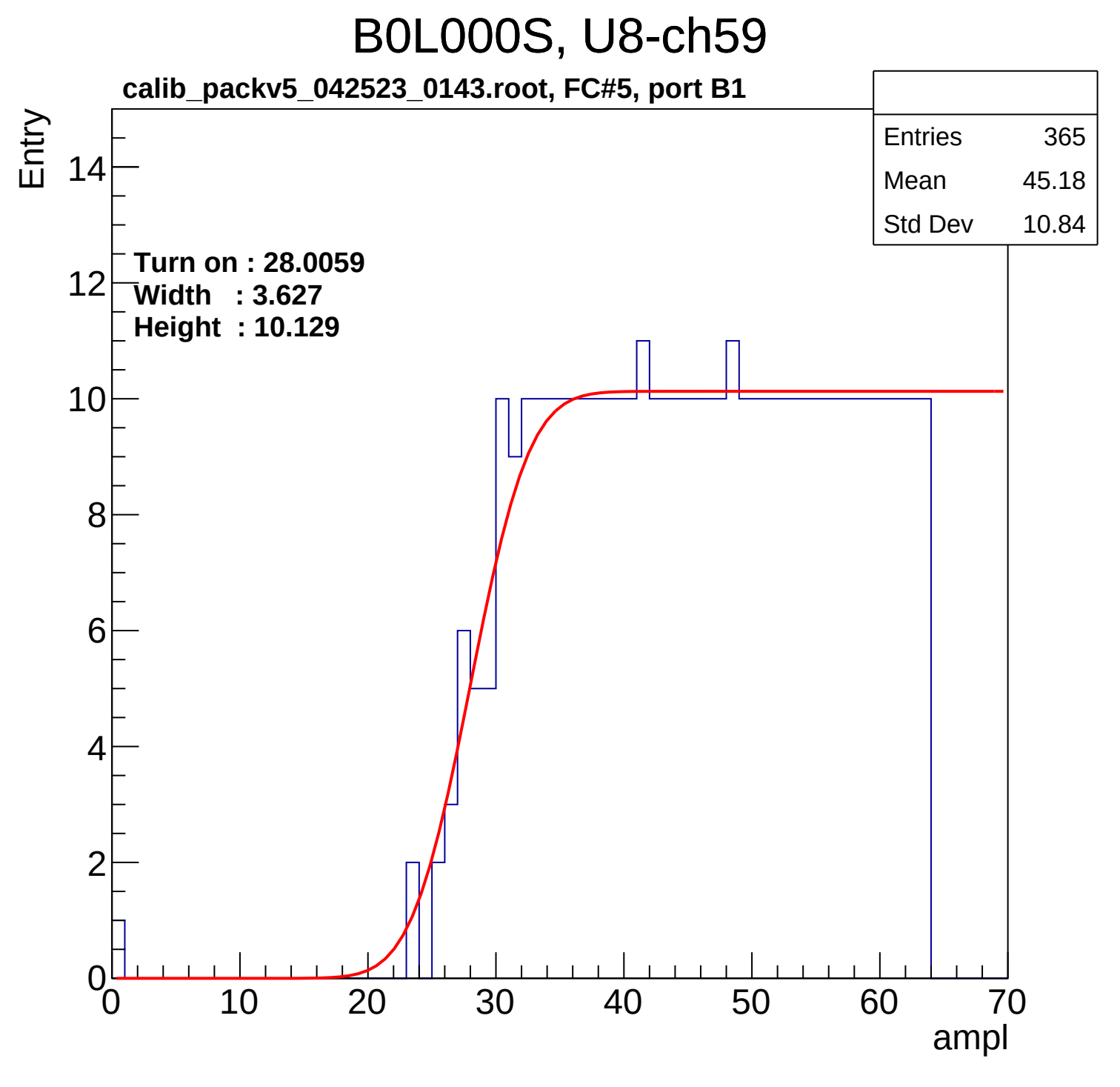
B0L000S, U8-ch59
calib_packv5_042523_0143.root, FC#5, port B1
Entries 365
Mean 45.18
Std Dev 10.84
Turn on : 28.0059
Width : 3.627
Height : 10.129
Entry
ampl
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4
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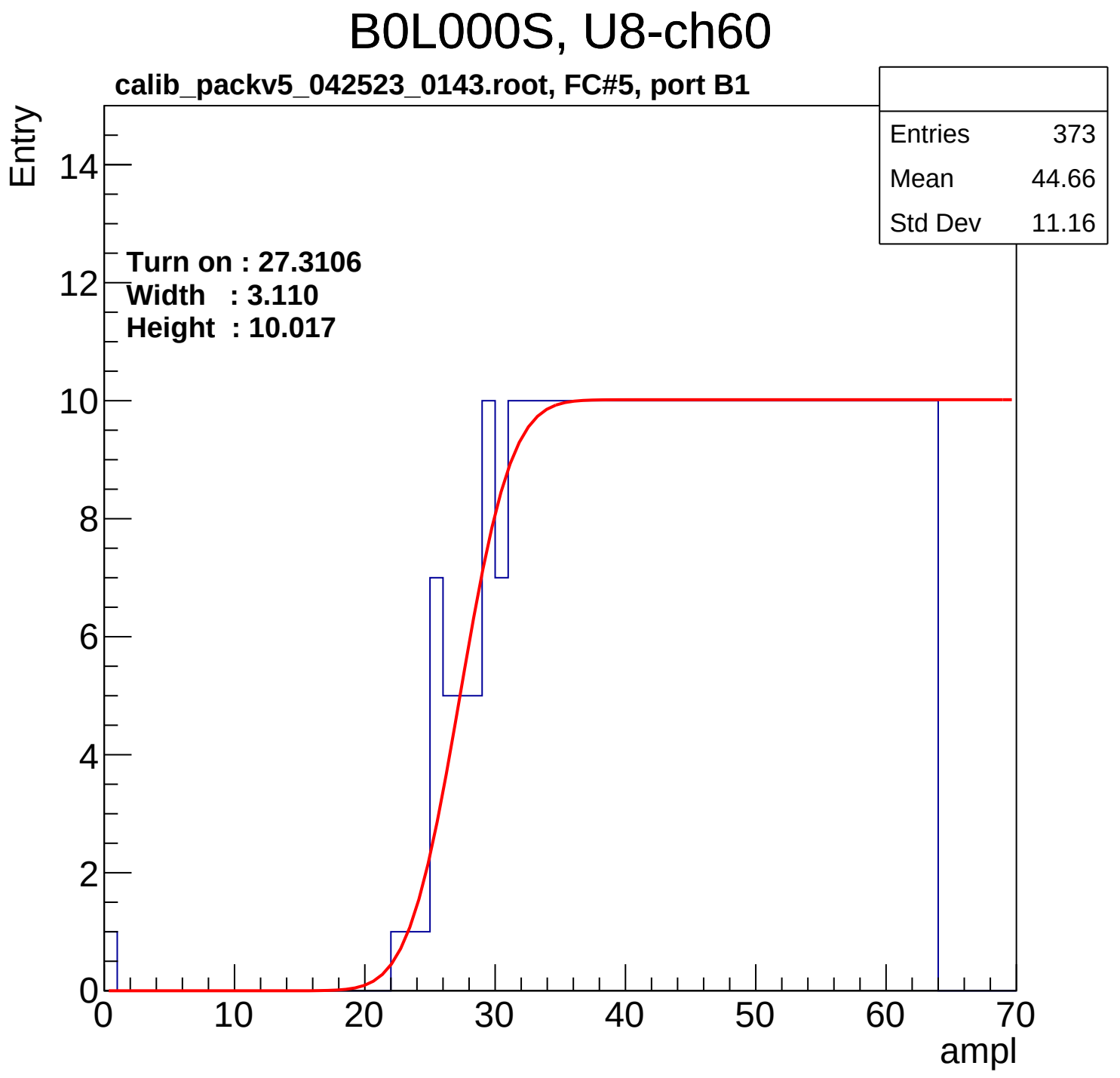
B0L000S, U8-ch60
calib_packv5_042523_0143.root, FC#5, port B1
Entries 373
Mean 44.66
Std Dev 11.16
Turn on : 27.3106
Width : 3.110
Height : 10.017
Entry
ampl
0
2
4
6
8
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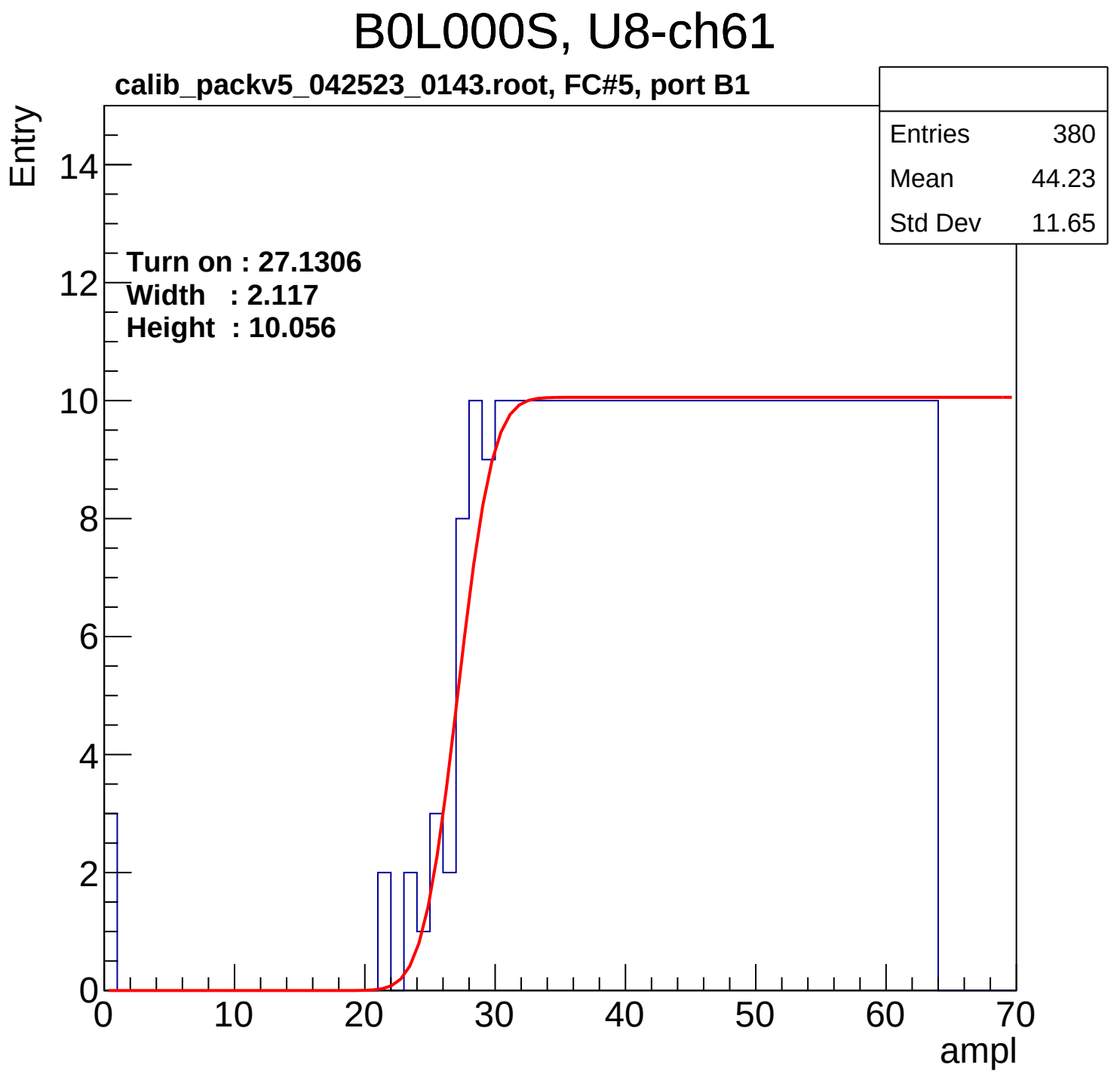
B0L000S, U8-ch61
calib_packv5_042523_0143.root, FC#5, port B1
Entries 380
Mean 44.23
Std Dev 11.65
Turn on : 27.1306
Width : 2.117
Height : 10.056
Entry
ampl
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2
4
6
8
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0
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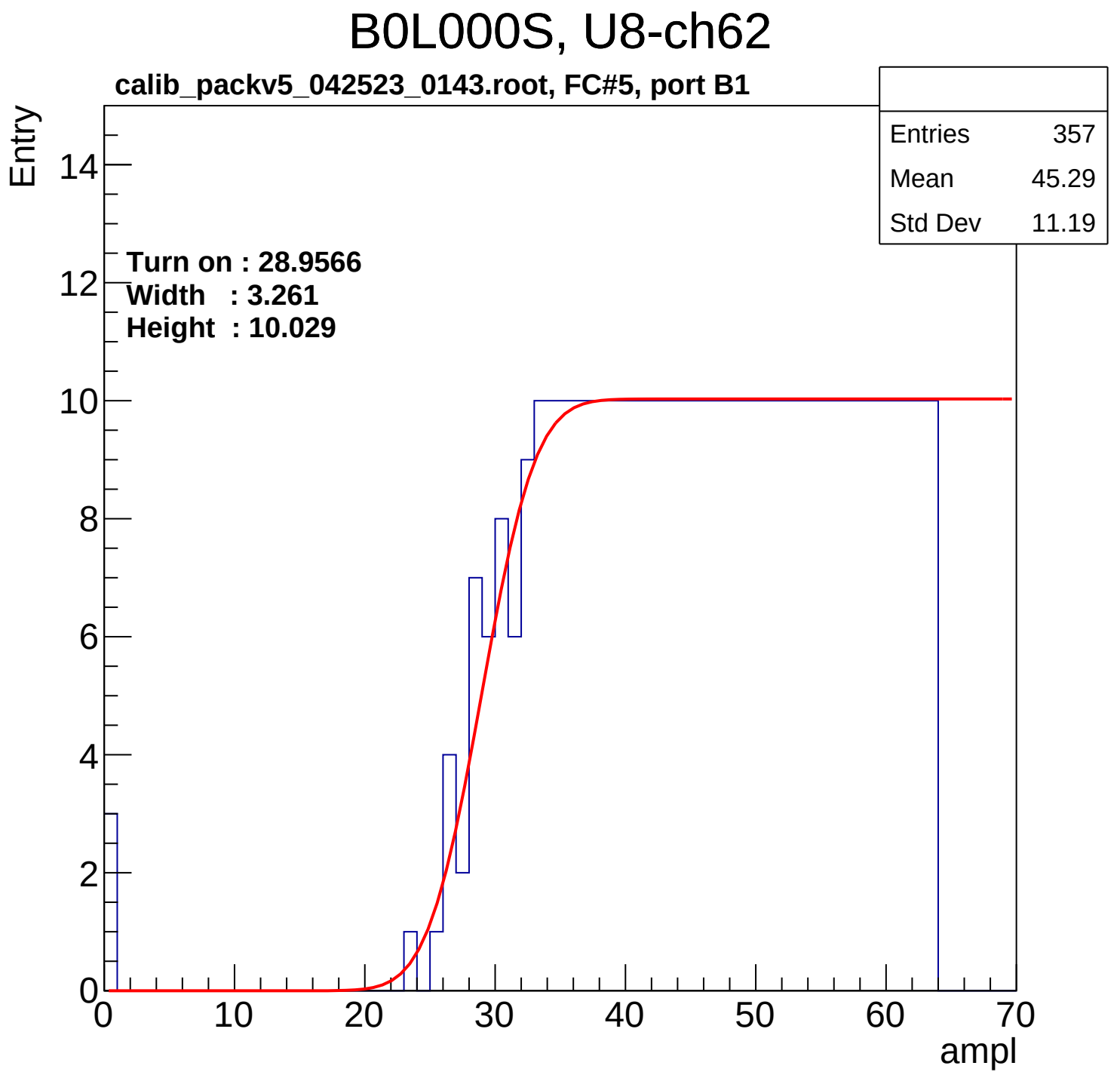
B0L000S, U8-ch62
calib_packv5_042523_0143.root, FC#5, port B1
Entries 357
Mean 45.29
Std Dev 11.19
Turn on : 28.9566
Width : 3.261
Height : 10.029
Entry
ampl
0
2
4
6
8
10
12
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0
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40
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60
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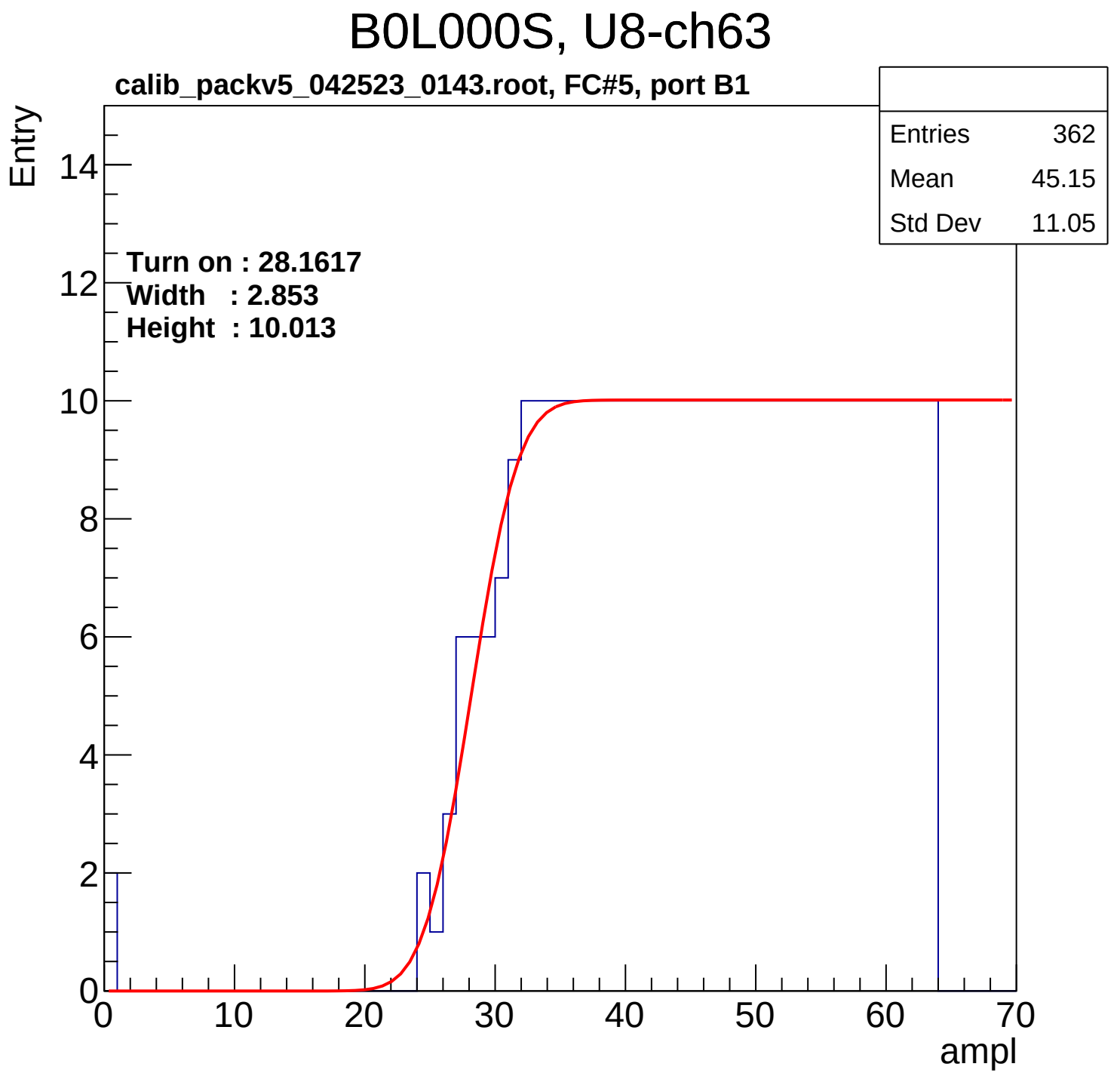
B0L000S, U8-ch63
calib_packv5_042523_0143.root, FC#5, port B1
Entries 362
Mean 45.15
Std Dev 11.05
Turn on : 28.1617
Width : 2.853
Height : 10.013
Entry
ampl
0
2
4
6
8
10
12
14
0
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40
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60
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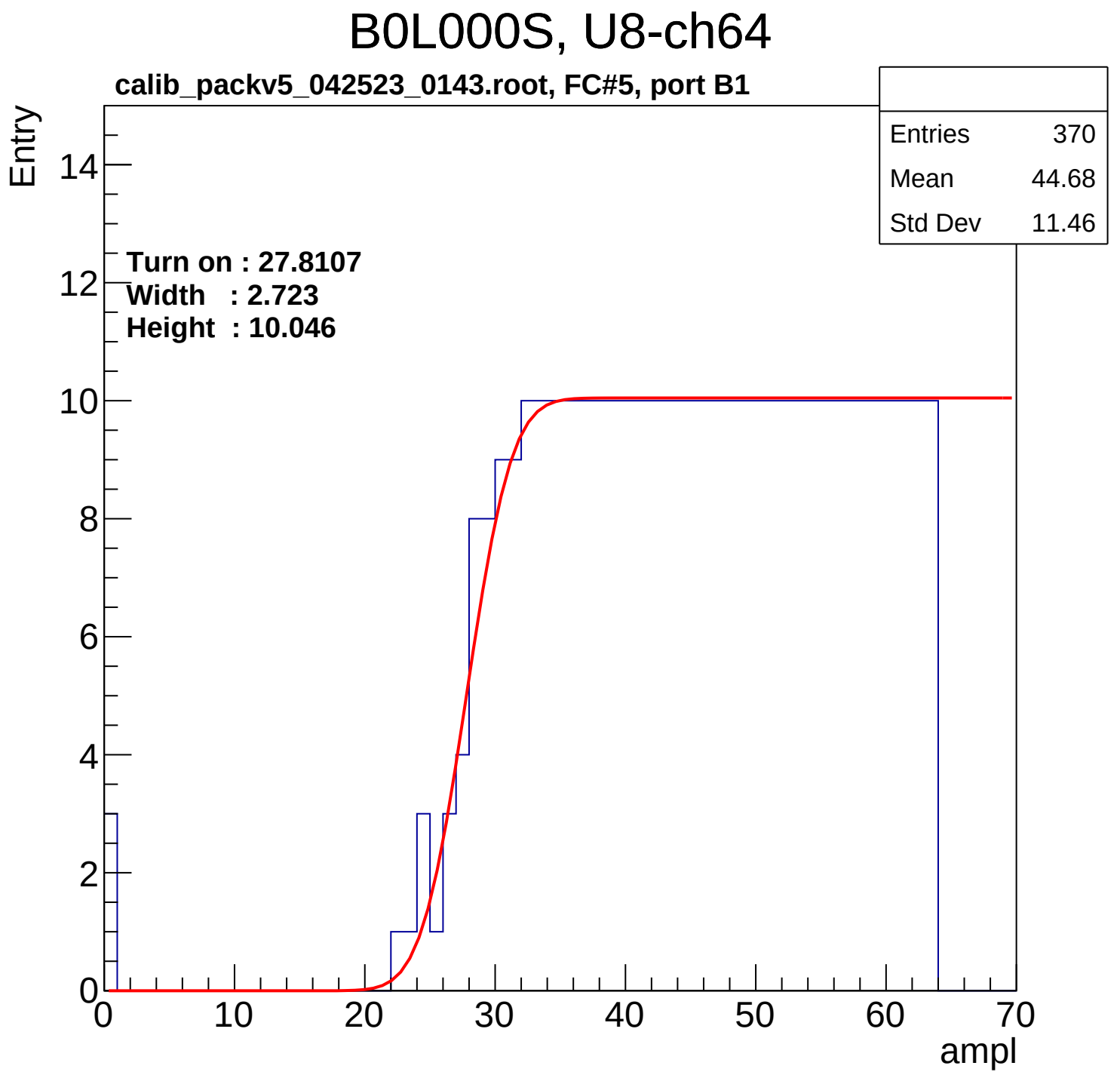
B0L000S, U8-ch64
calib_packv5_042523_0143.root, FC#5, port B1
Entries 370
Mean 44.68
Std Dev 11.46
Turn on : 27.8107
Width : 2.723
Height : 10.046
Entry
ampl
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4
6
8
10
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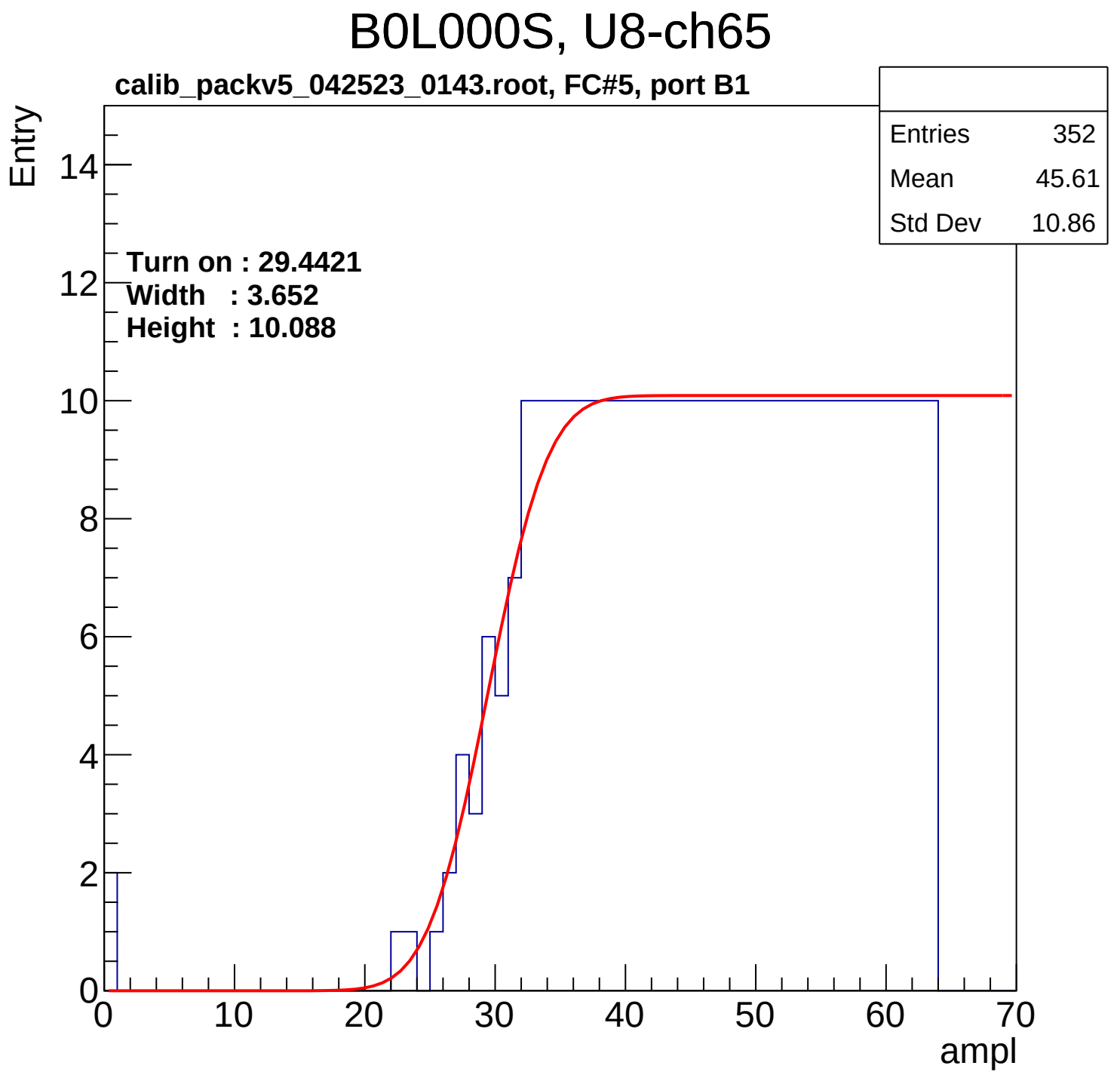
B0L000S, U8-ch65
calib_packv5_042523_0143.root, FC#5, port B1
Entries 352
Mean 45.61
Std Dev 10.86
Turn on : 29.4421
Width : 3.652
Height : 10.088
Entry
ampl
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2
4
6
8
10
12
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0
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60
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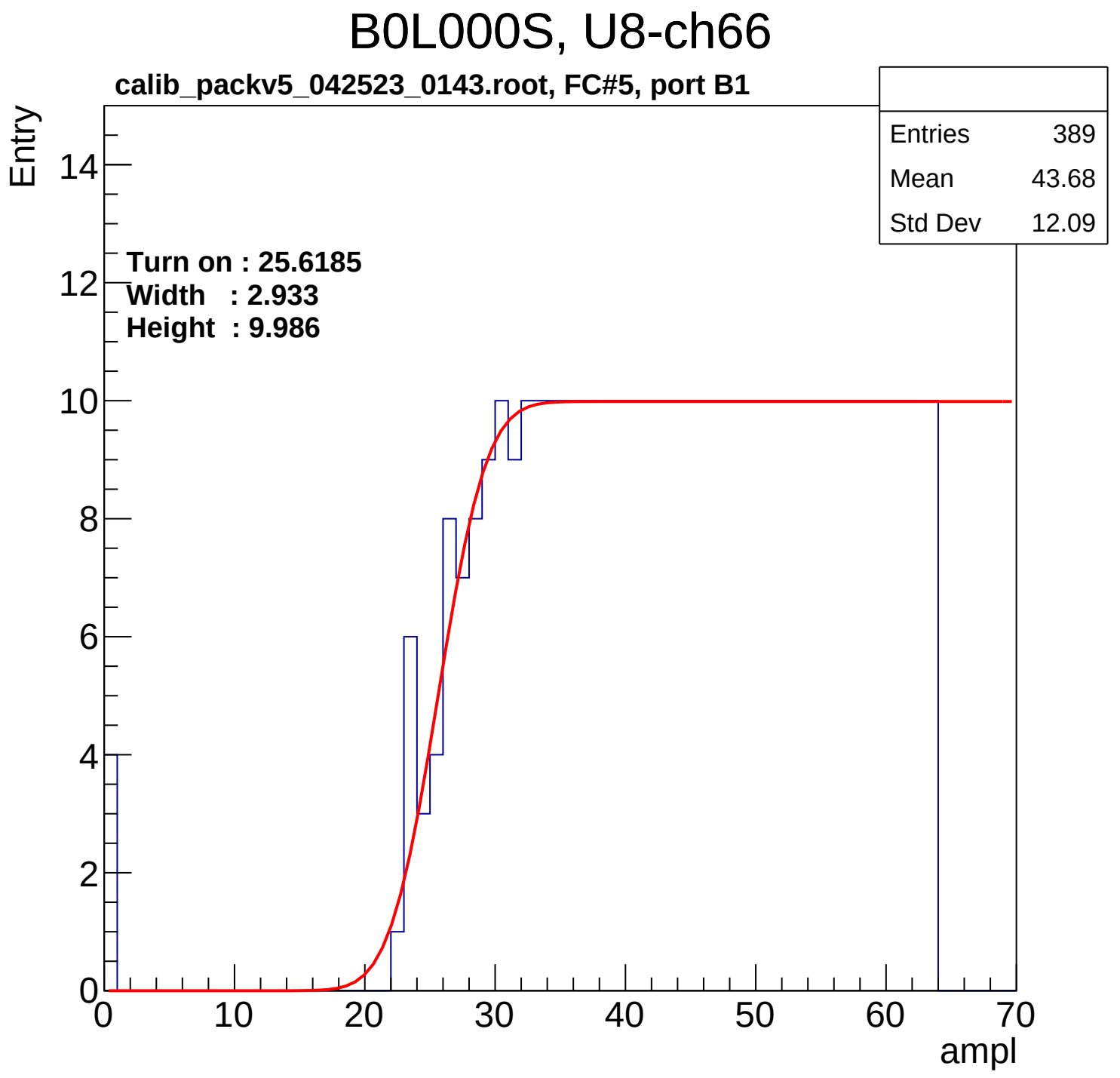
B0L000S, U8-ch66
calib_packv5_042523_0143.root, FC#5, port B1
Entries 389
Mean 43.68
Std Dev 12.09
Turn on : 25.6185
Width : 2.933
Height : 9.986
Entry
ampl
0
2
4
6
8
10
12
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0
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60
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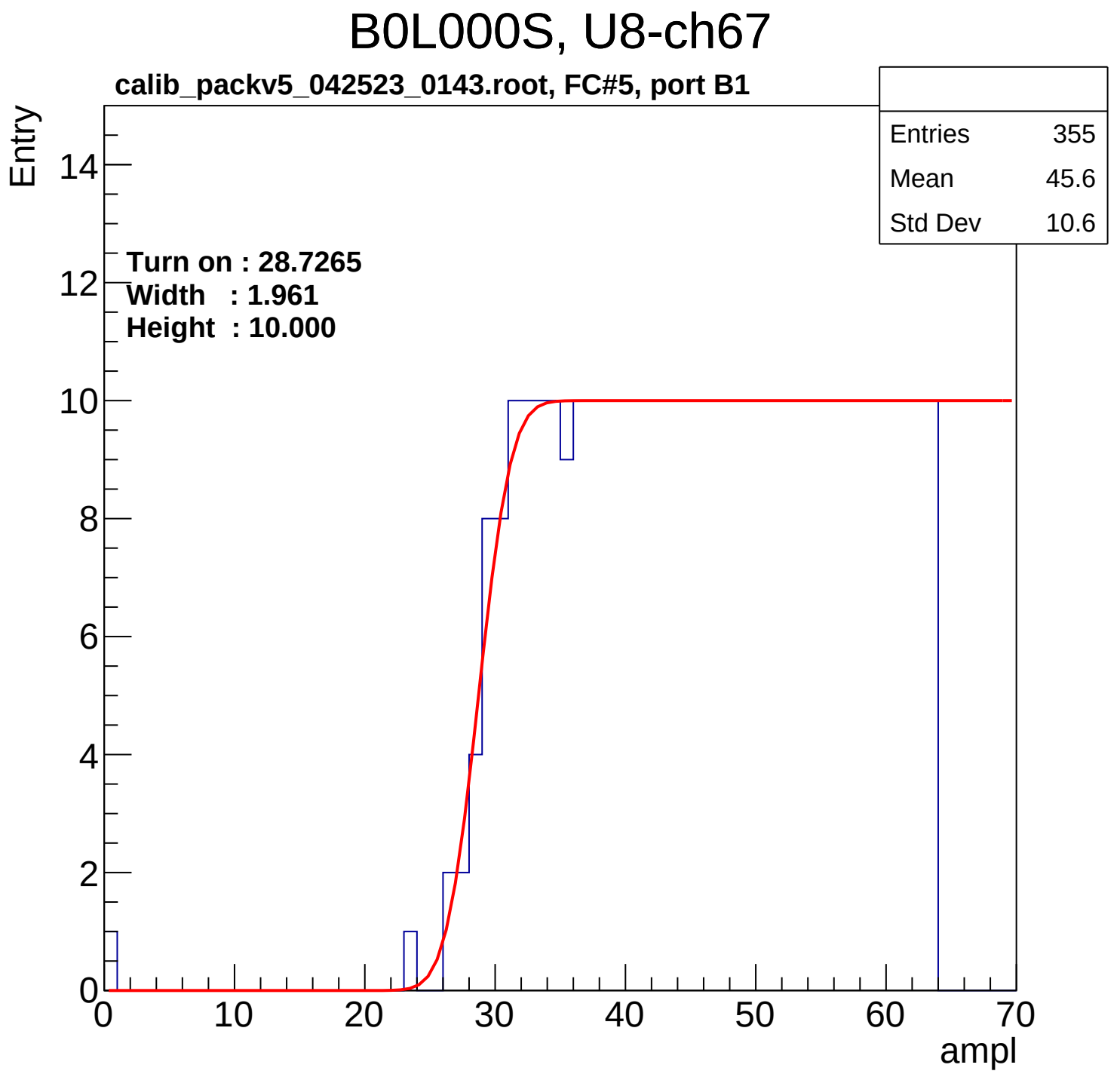
B0L000S, U8-ch67
calib_packv5_042523_0143.root, FC#5, port B1
Entries 355
Mean 45.6
Std Dev 10.6
Turn on : 28.7265
Width : 1.961
Height : 10.000
Entry
ampl
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2
4
6
8
10
12
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0
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60
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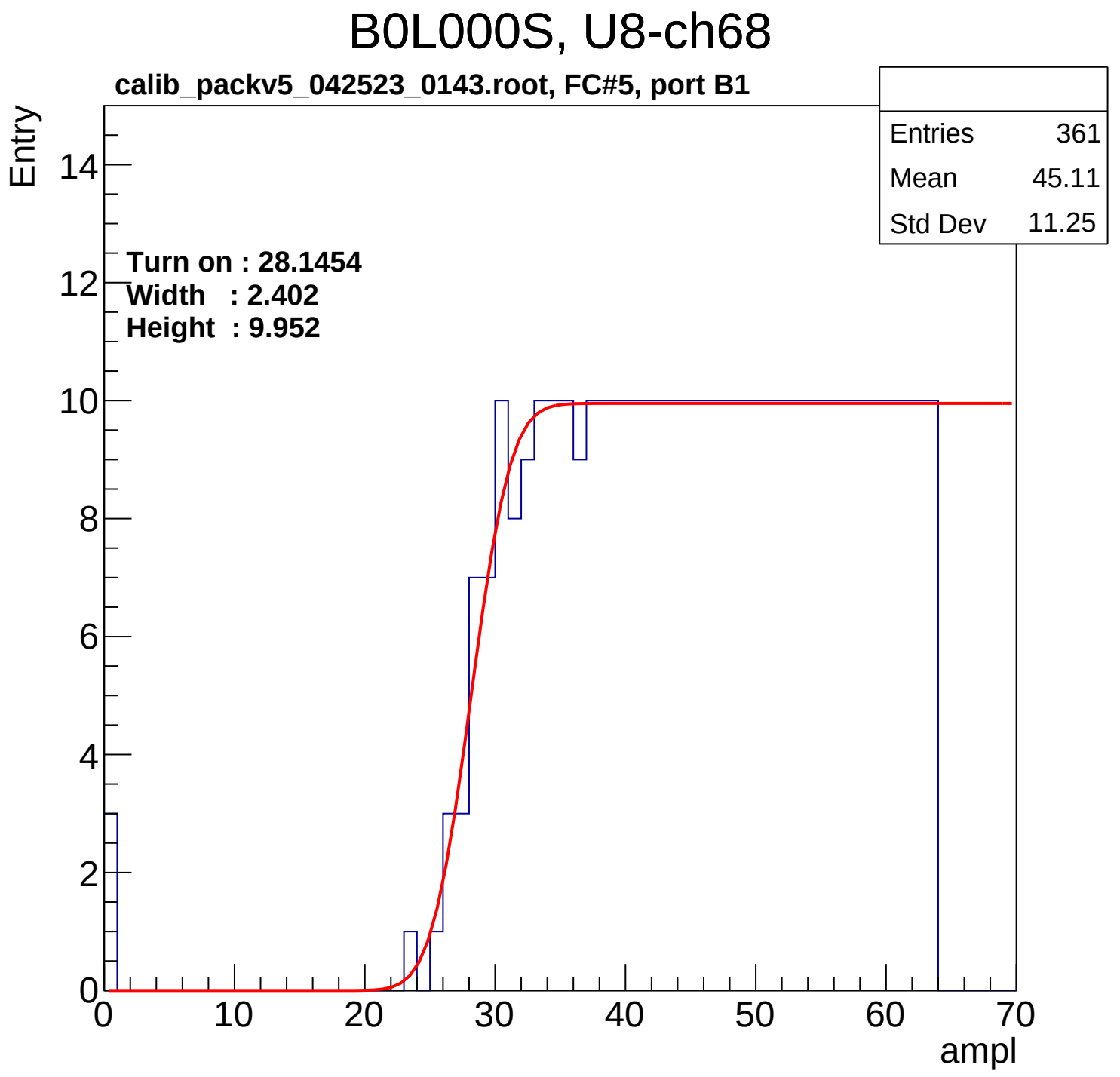
B0L000S, U8-ch68
calib_packv5_042523_0143.root, FC#5, port B1
Entries 361
Mean 45.11
Std Dev 11.25
Turn on : 28.1454
Width : 2.402
Height : 9.952
Entry
ampl
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2
4
6
8
10
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0
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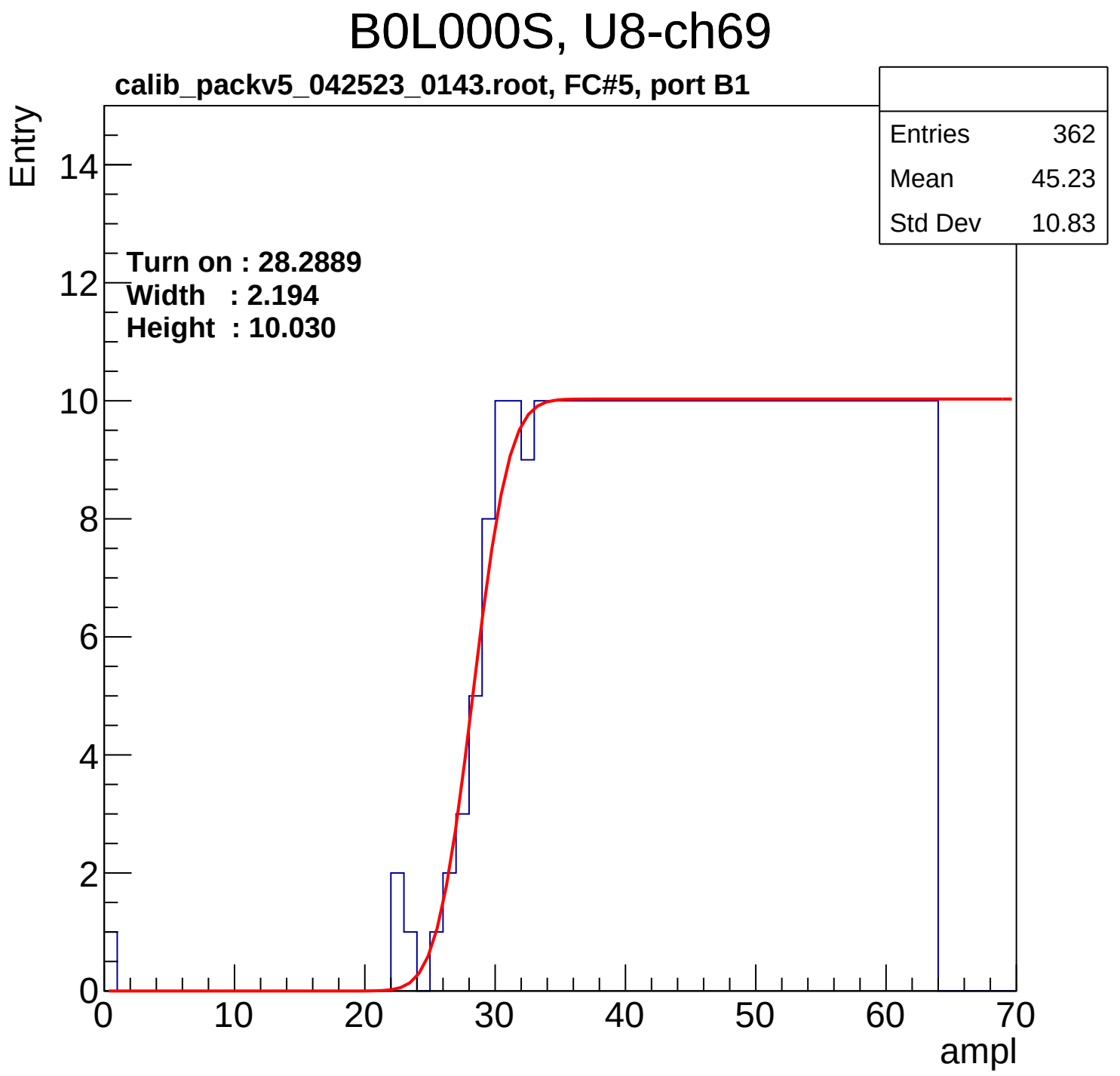
B0L000S, U8-ch69
calib_packv5_042523_0143.root, FC#5, port B1
Entries 362
Mean 45.23
Std Dev 10.83
Turn on : 28.2889
Width : 2.194
Height : 10.030
Entry
ampl
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4
6
8
10
12
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0
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60
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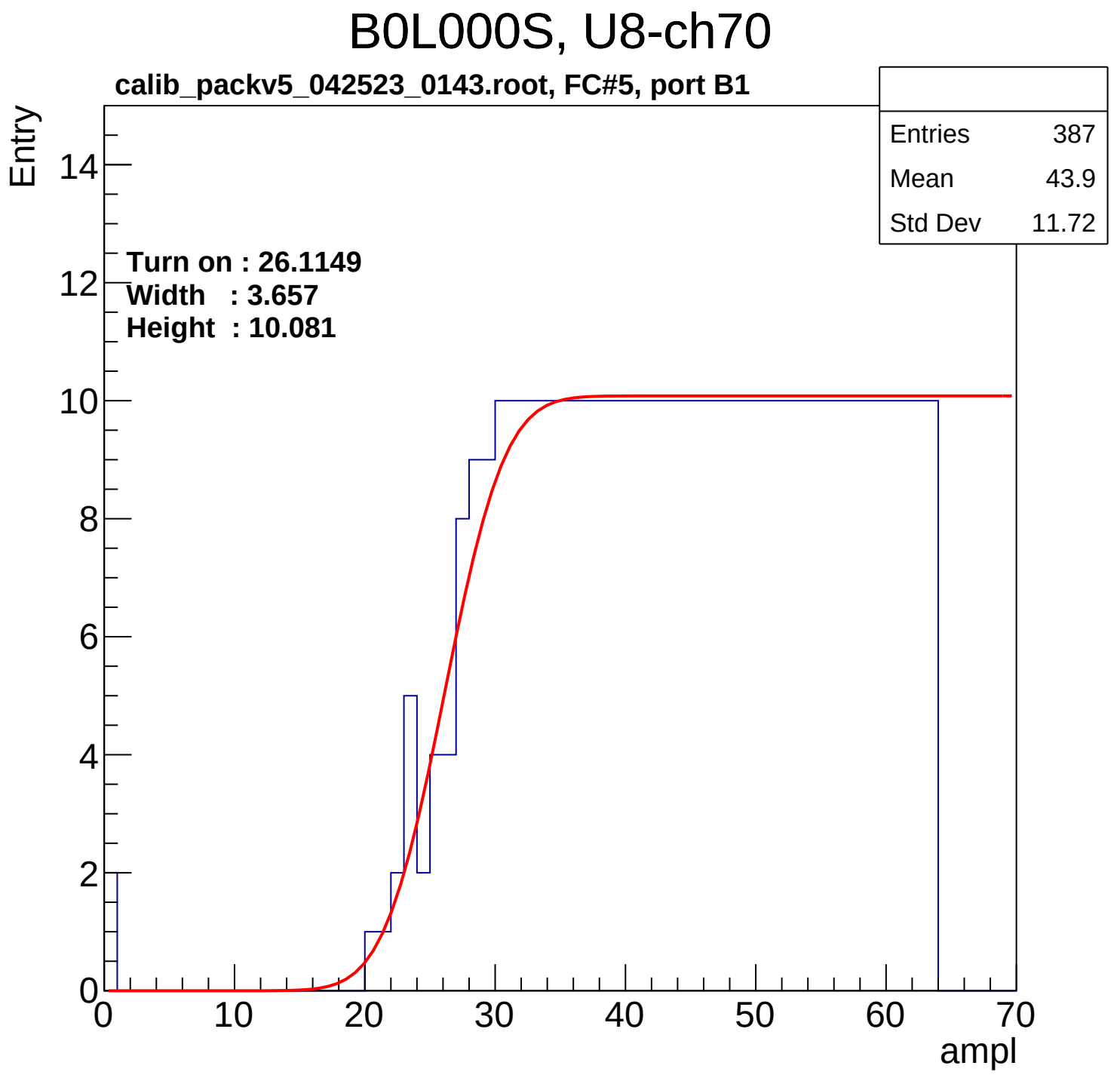
B0L000S, U8-ch70
calib_packv5_042523_0143.root, FC#5, port B1
Entries 387
Mean 43.9
Std Dev 11.72
Turn on : 26.1149
Width : 3.657
Height : 10.081
Entry
ampl
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2
4
6
8
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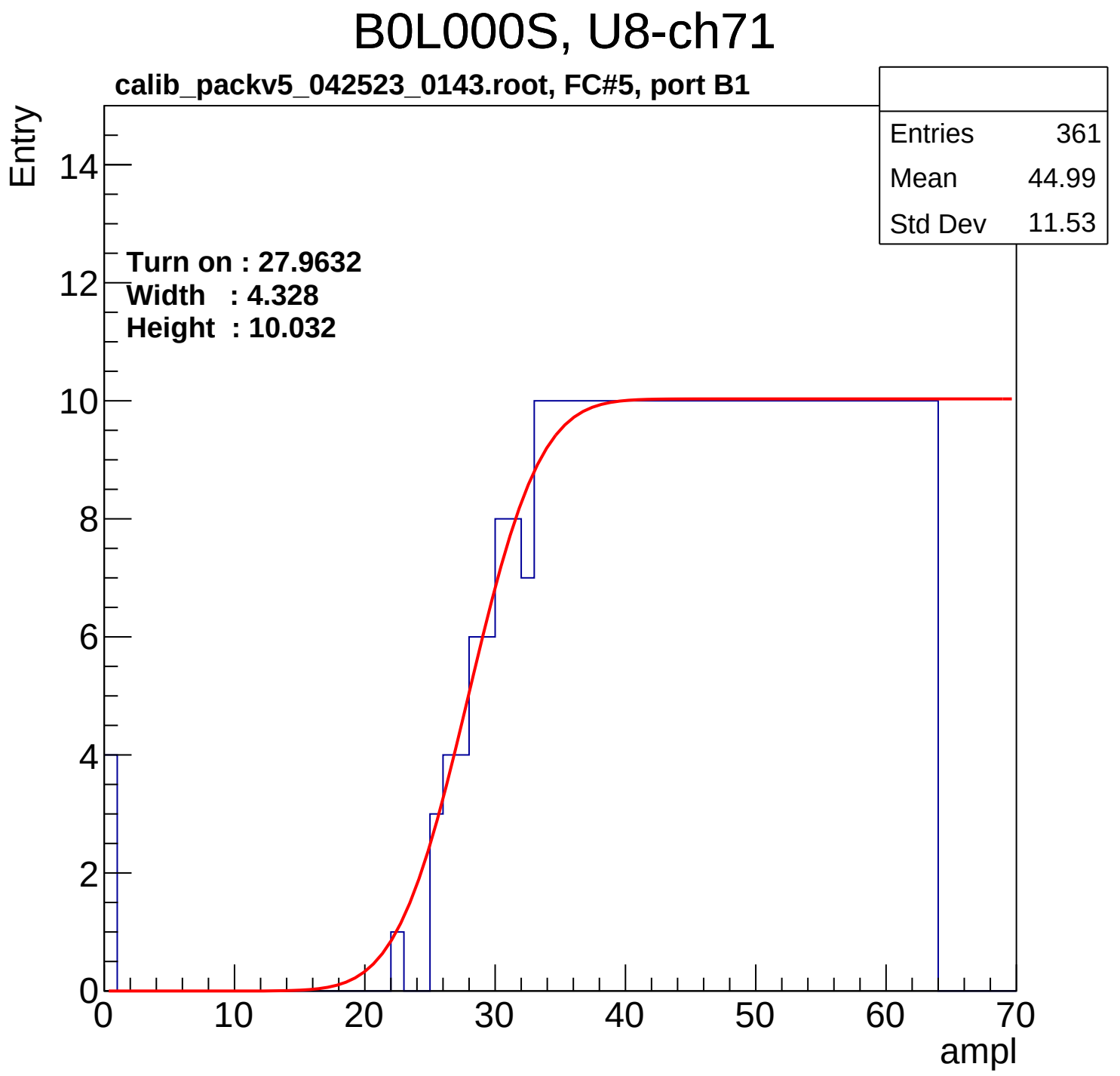
B0L000S, U8-ch71
calib_packv5_042523_0143.root, FC#5, port B1
Entries 361
Mean 44.99
Std Dev 11.53
Turn on : 27.9632
Width : 4.328
Height : 10.032
Entry
ampl
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2
4
6
8
10
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0
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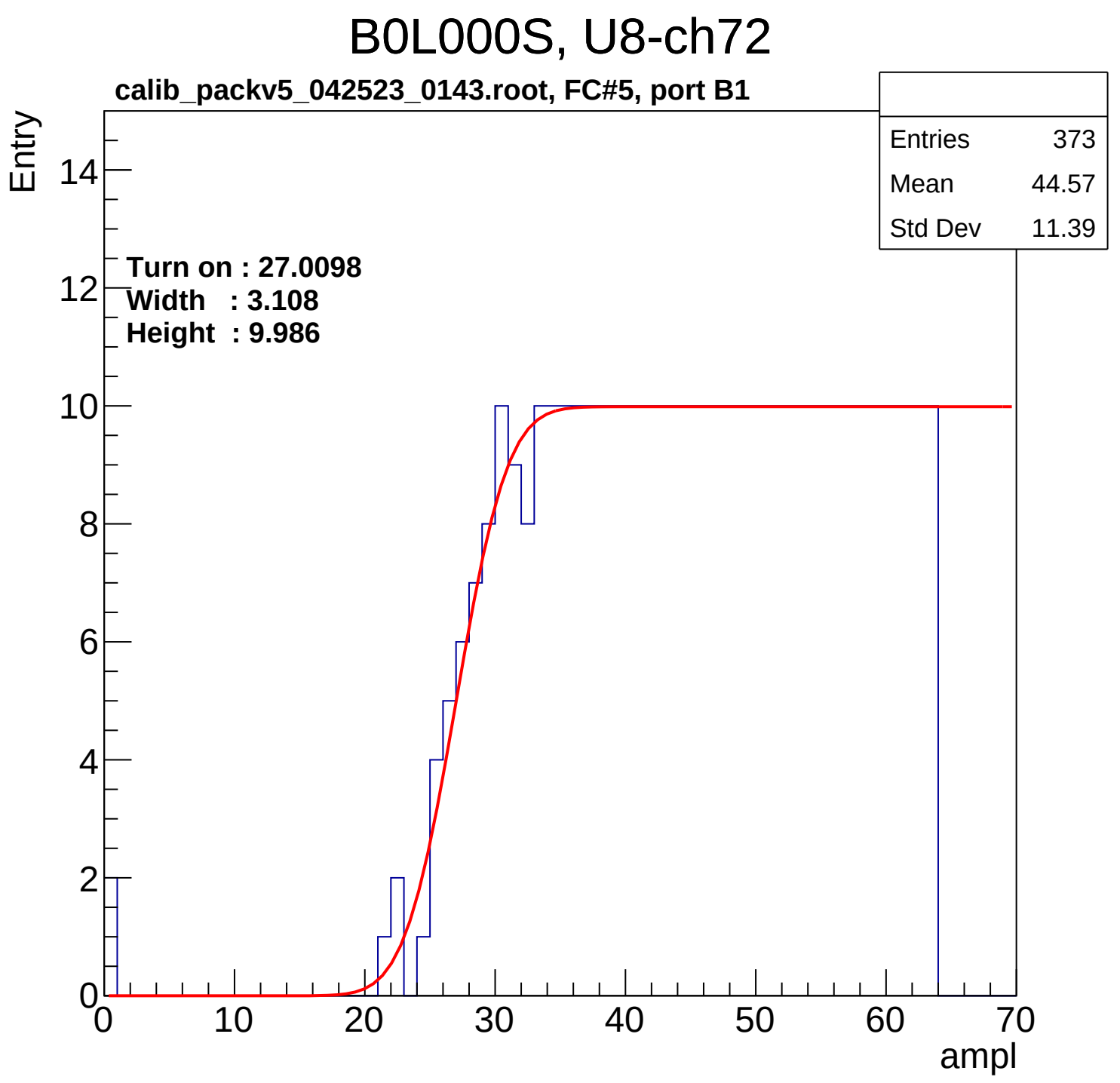
B0L000S, U8-ch72
calib_packv5_042523_0143.root, FC#5, port B1
Entries 373
Mean 44.57
Std Dev 11.39
Turn on : 27.0098
Width : 3.108
Height : 9.986
Entry
ampl
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4
6
8
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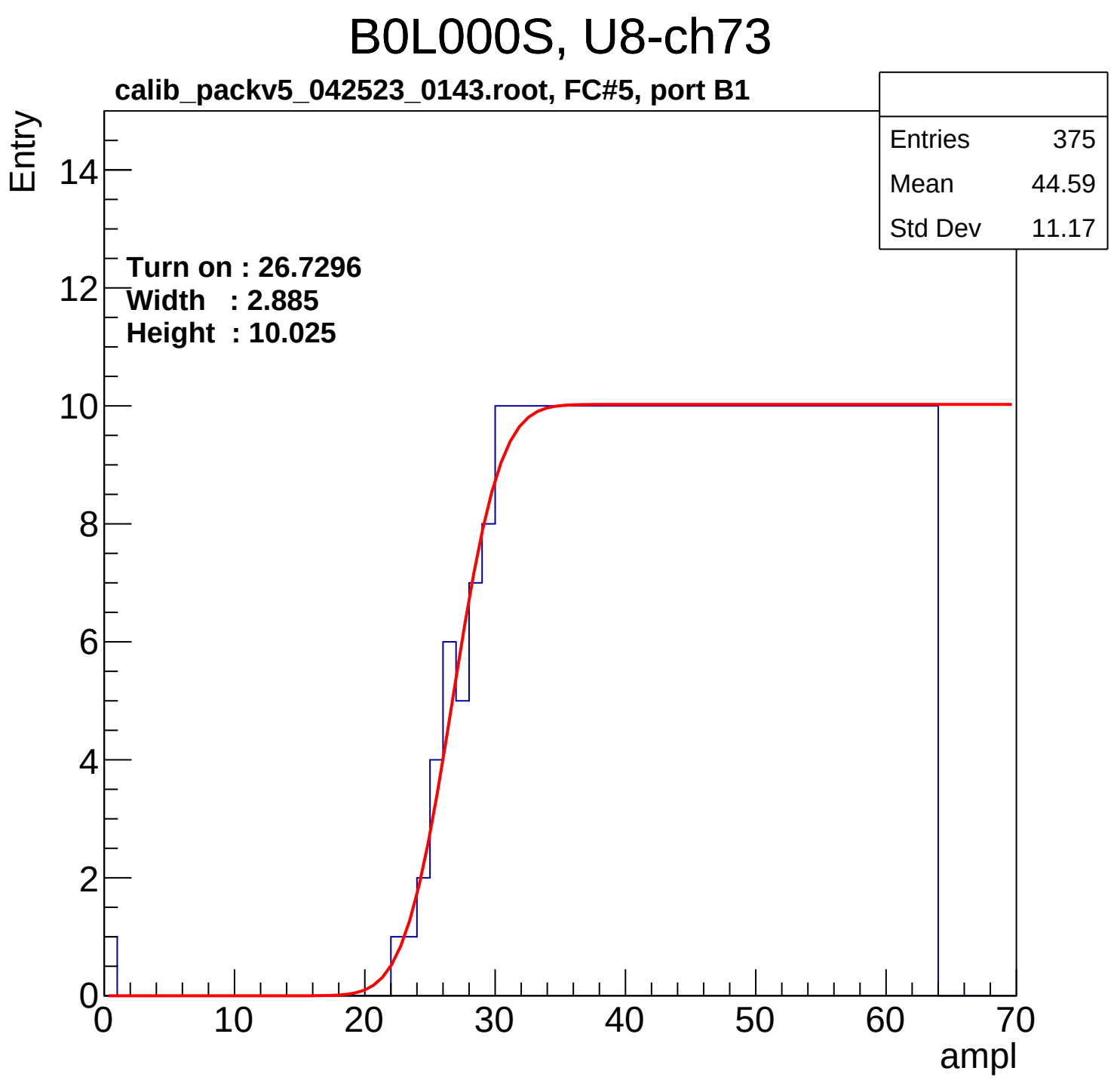
B0L000S, U8-ch73
calib_packv5_042523_0143.root, FC#5, port B1
Entries 375
Mean 44.59
Std Dev 11.17
Turn on : 26.7296
Width : 2.885
Height : 10.025
Entry
ampl
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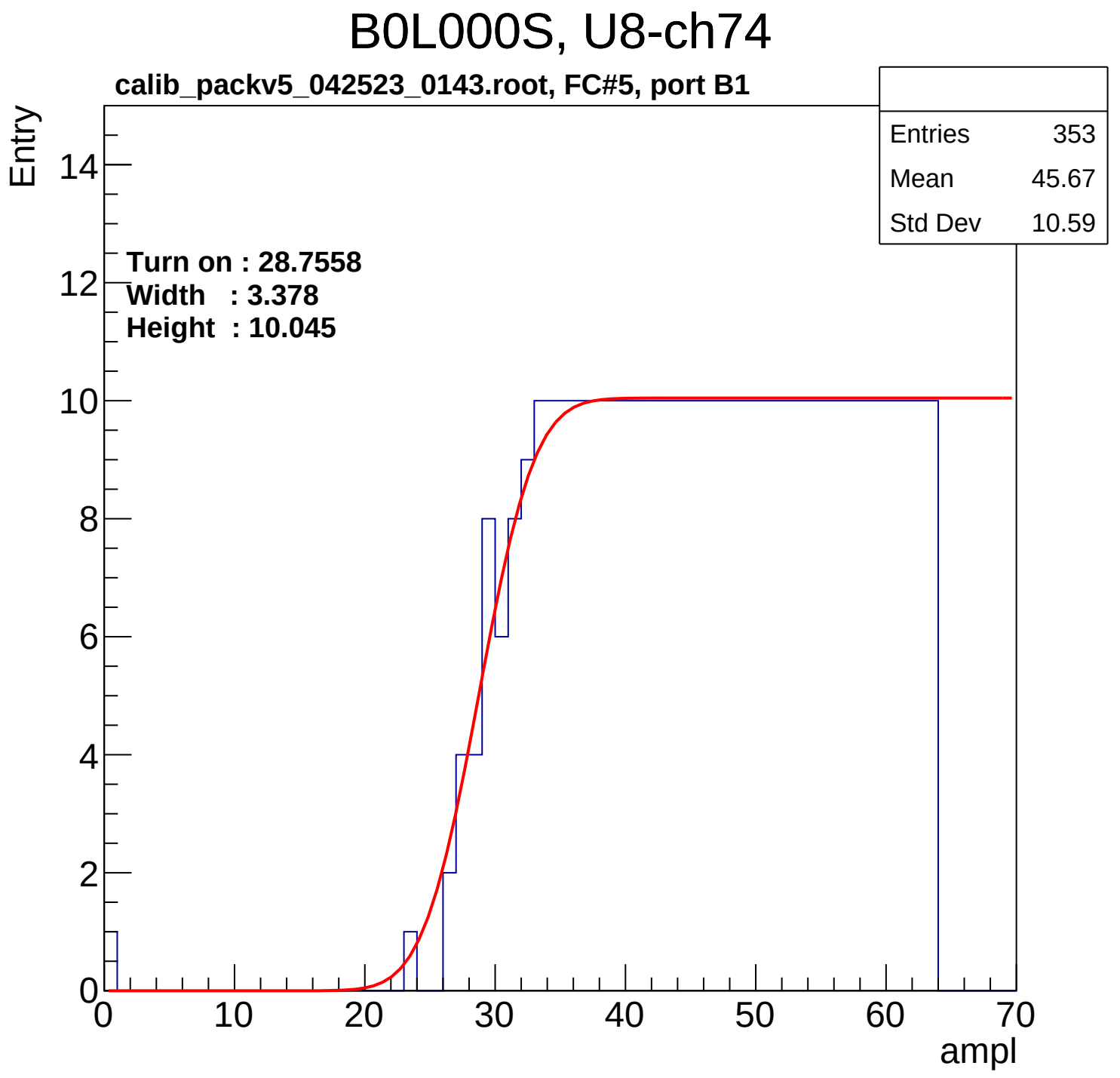
B0L000S, U8-ch74
calib_packv5_042523_0143.root, FC#5, port B1
Entries 353
Mean 45.67
Std Dev 10.59
Turn on : 28.7558
Width : 3.378
Height : 10.045
Entry
ampl
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8
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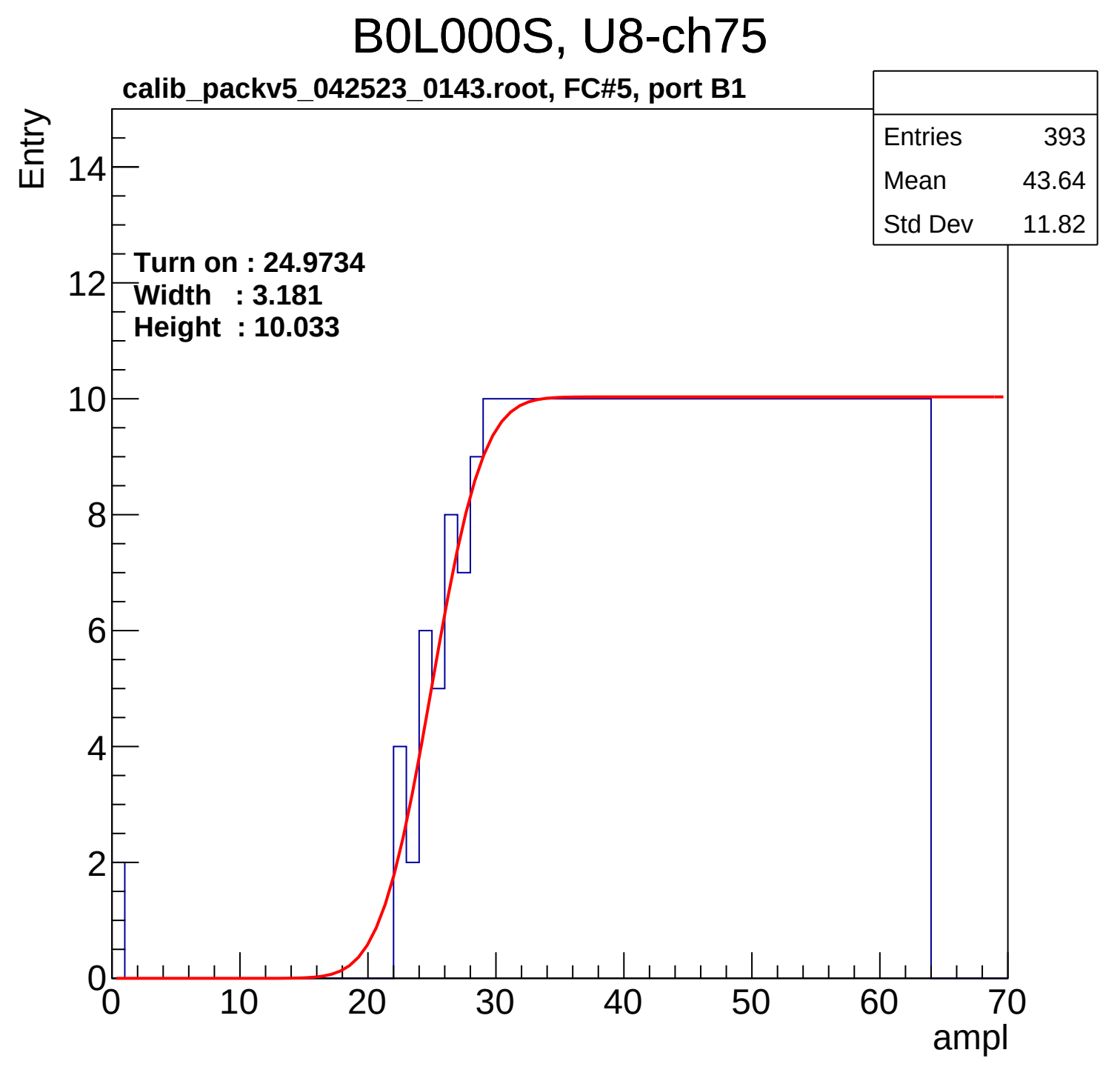
B0L000S, U8-ch75
calib_packv5_042523_0143.root, FC#5, port B1
Entries 393
Mean 43.64
Std Dev 11.82
Turn on : 24.9734
Width : 3.181
Height : 10.033
Entry
ampl
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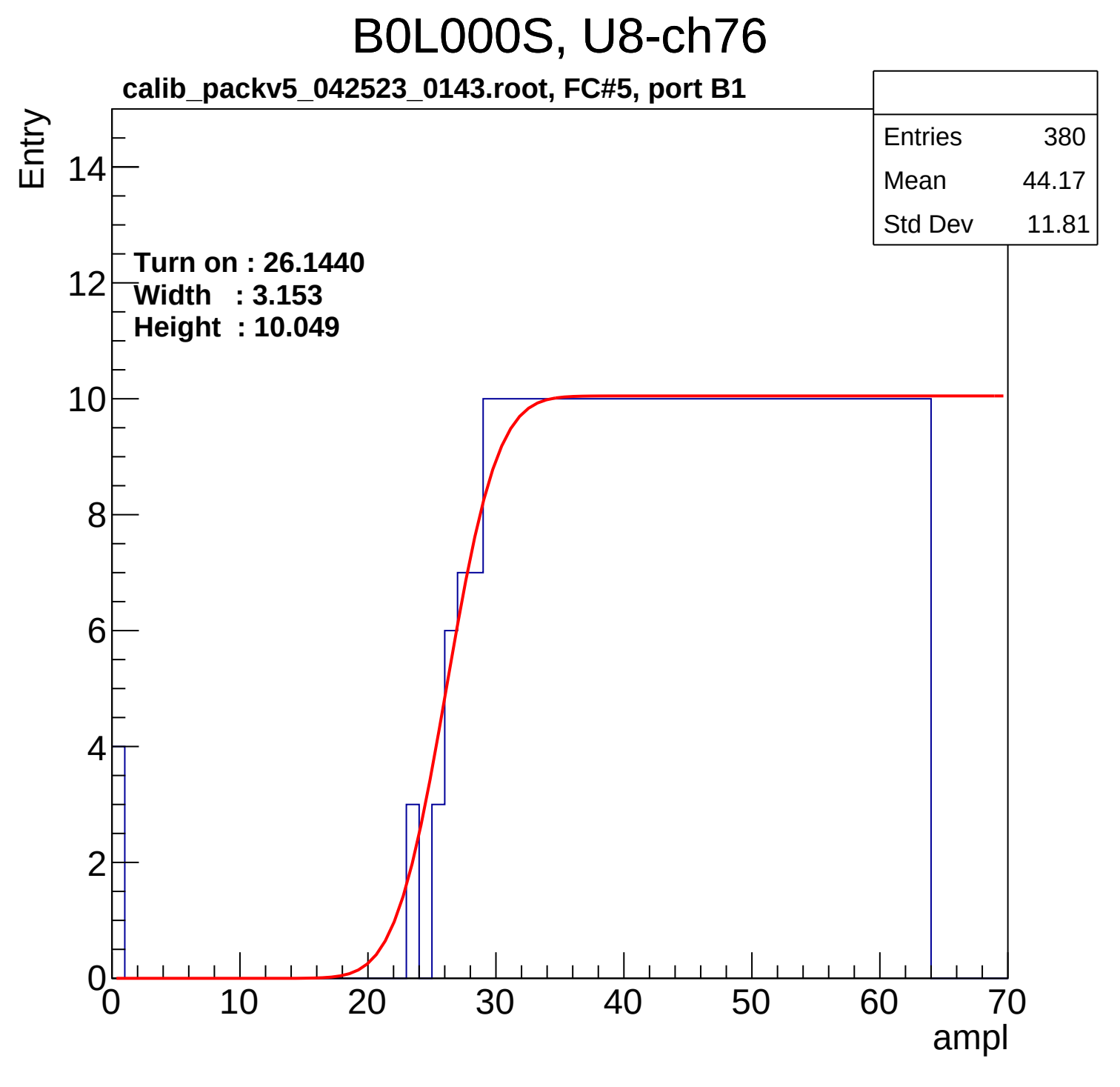
B0L000S, U8-ch76
calib_packv5_042523_0143.root, FC#5, port B1
Entries 380
Mean 44.17
Std Dev 11.81
Turn on : 26.1440
Width : 3.153
Height : 10.049
Entry
ampl
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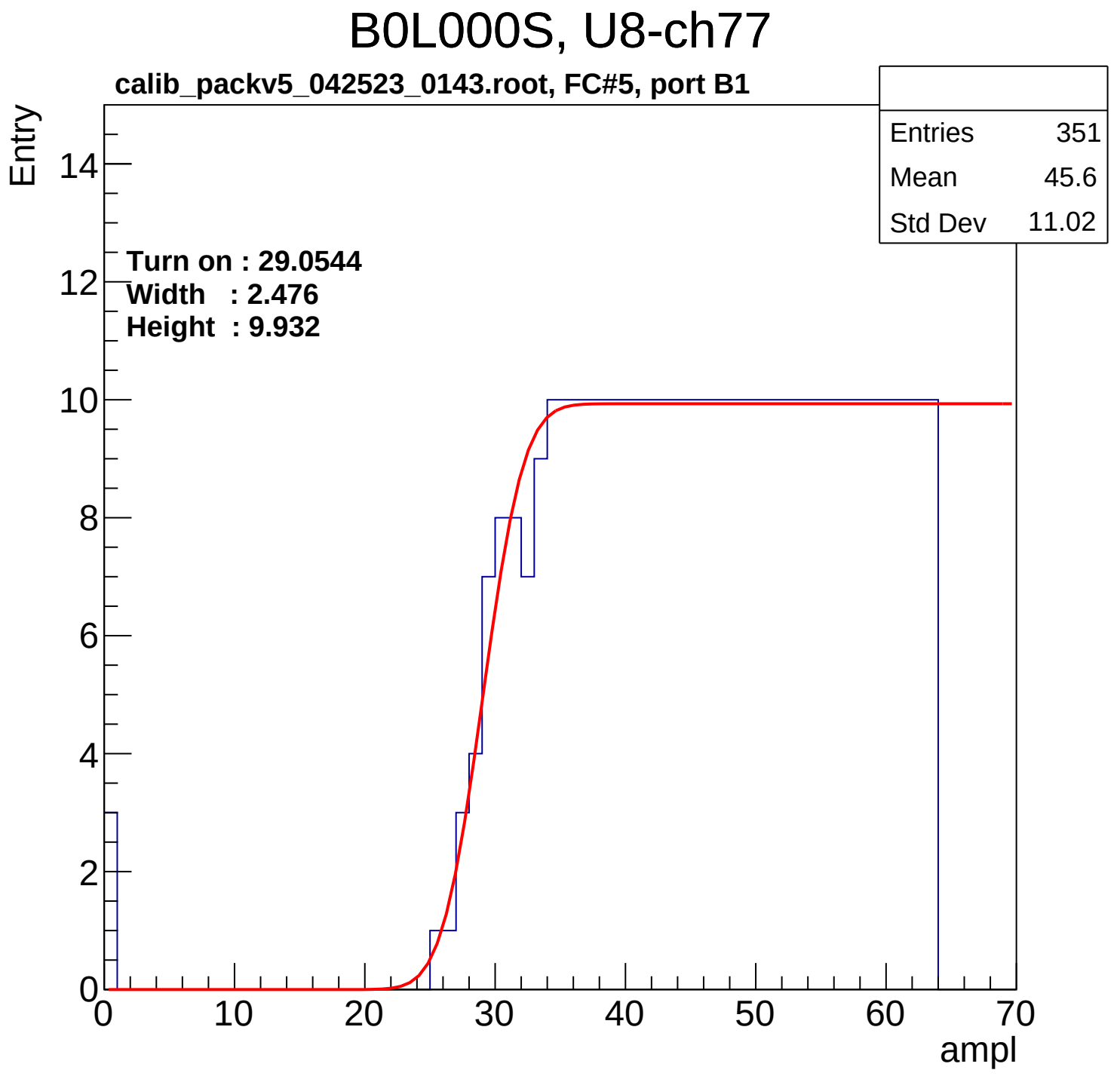
B0L000S, U8-ch77
calib_packv5_042523_0143.root, FC#5, port B1
Entries 351
Mean 45.6
Std Dev 11.02
Turn on : 29.0544
Width : 2.476
Height : 9.932
Entry
ampl
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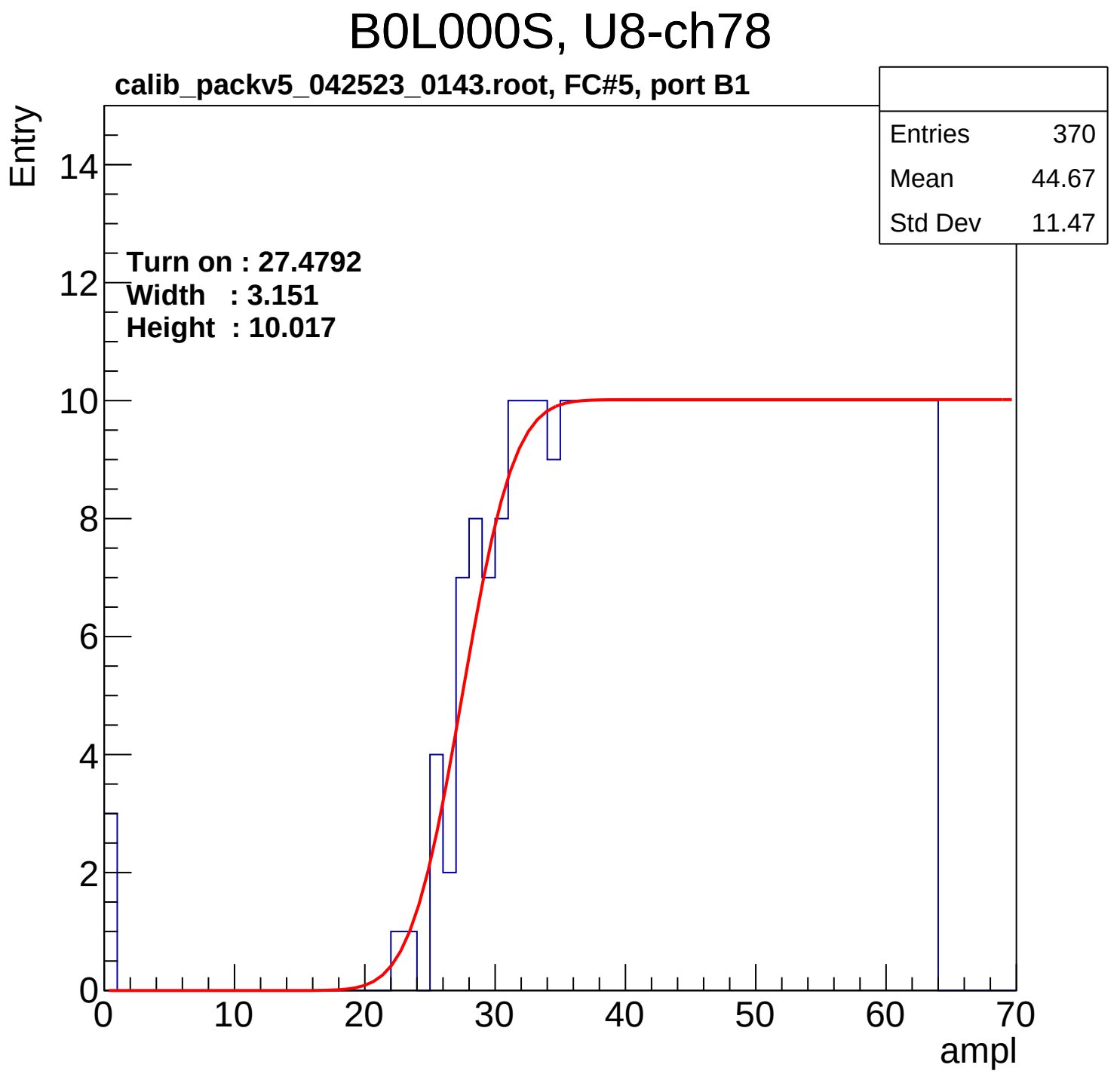
B0L000S, U8-ch78
calib_packv5_042523_0143.root, FC#5, port B1
Entries 370
Mean 44.67
Std Dev 11.47
Turn on : 27.4792
Width : 3.151
Height : 10.017
Entry
ampl
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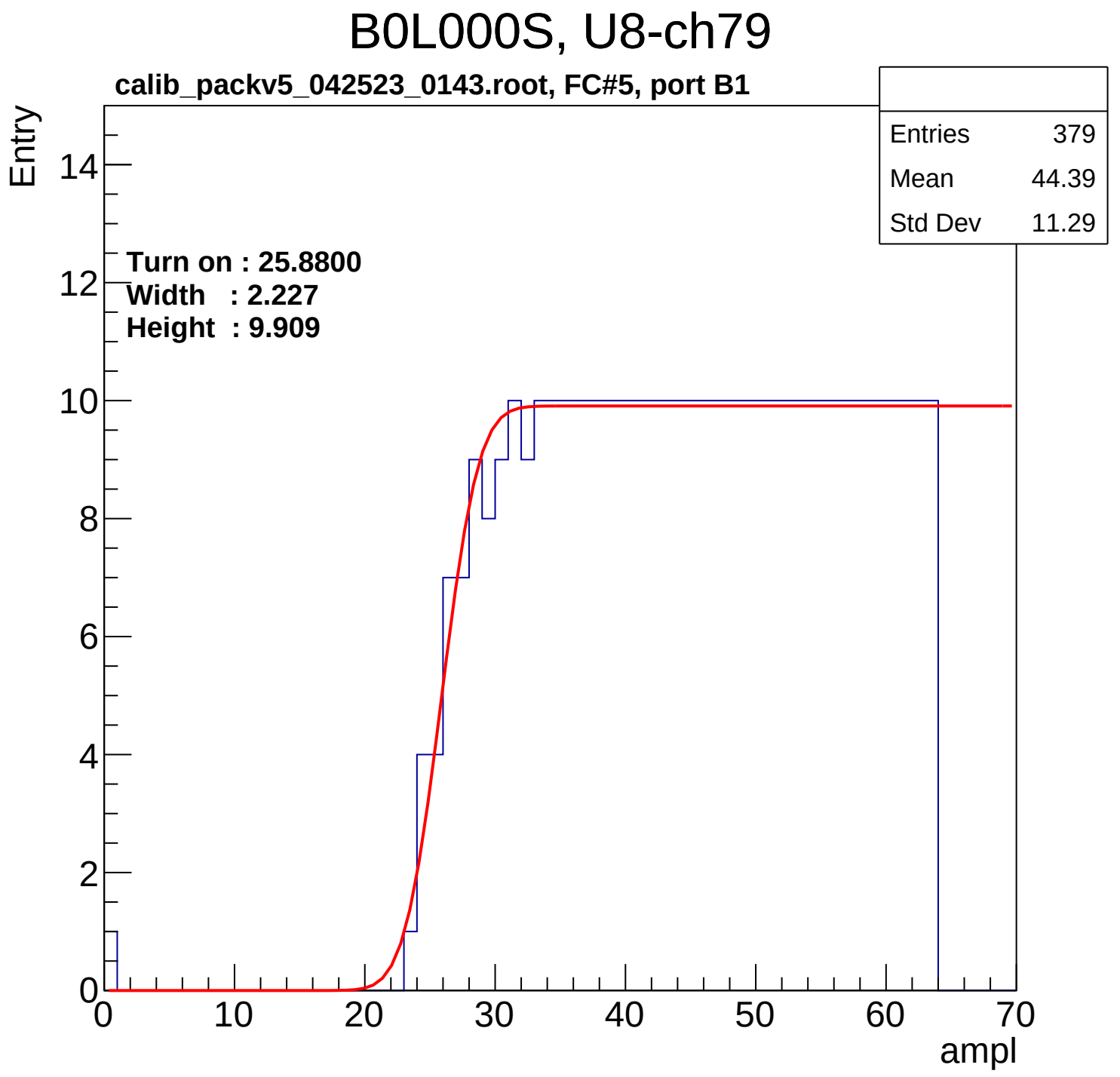
B0L000S, U8-ch79
calib_packv5_042523_0143.root, FC#5, port B1
Entries 379
Mean 44.39
Std Dev 11.29
Turn on : 25.8800
Width : 2.227
Height : 9.909
Entry
ampl
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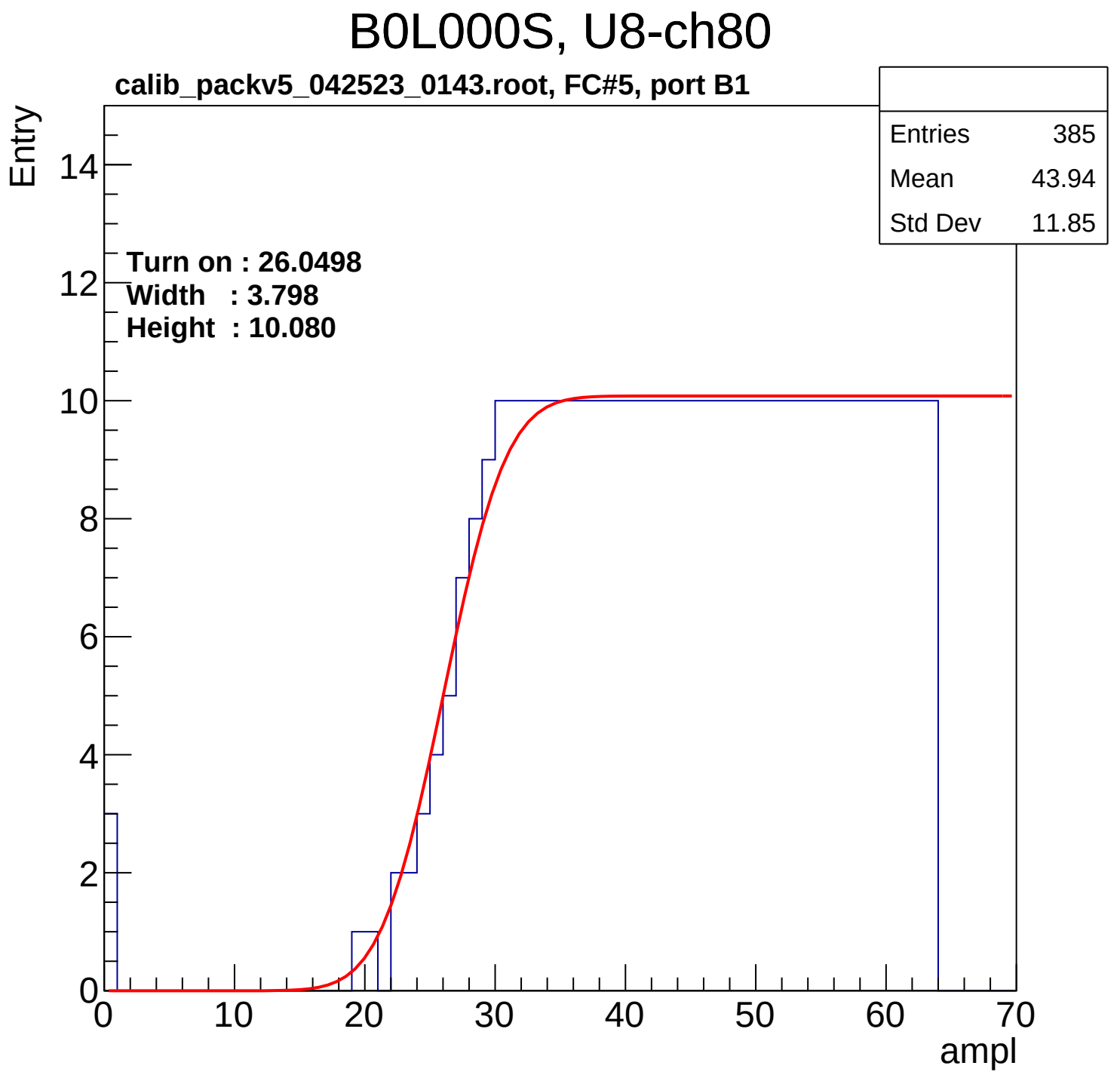
B0L000S, U8-ch80
calib_packv5_042523_0143.root, FC#5, port B1
Entries 385
Mean 43.94
Std Dev 11.85
Turn on : 26.0498
Width : 3.798
Height : 10.080
Entry
ampl
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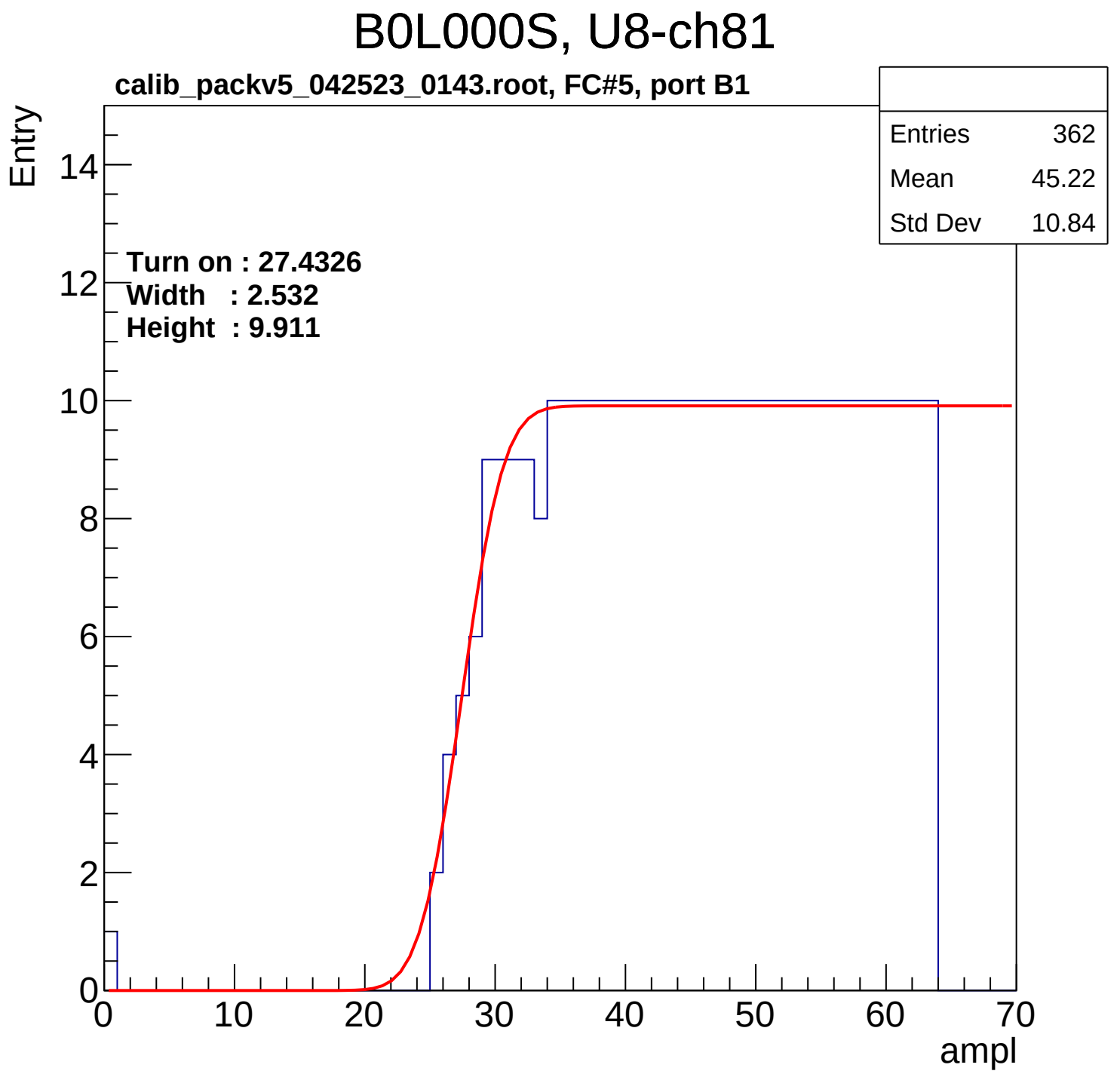
B0L000S, U8-ch81
calib_packv5_042523_0143.root, FC#5, port B1
Entries 362
Mean 45.22
Std Dev 10.84
Turn on : 27.4326
Width : 2.532
Height : 9.911
Entry
ampl
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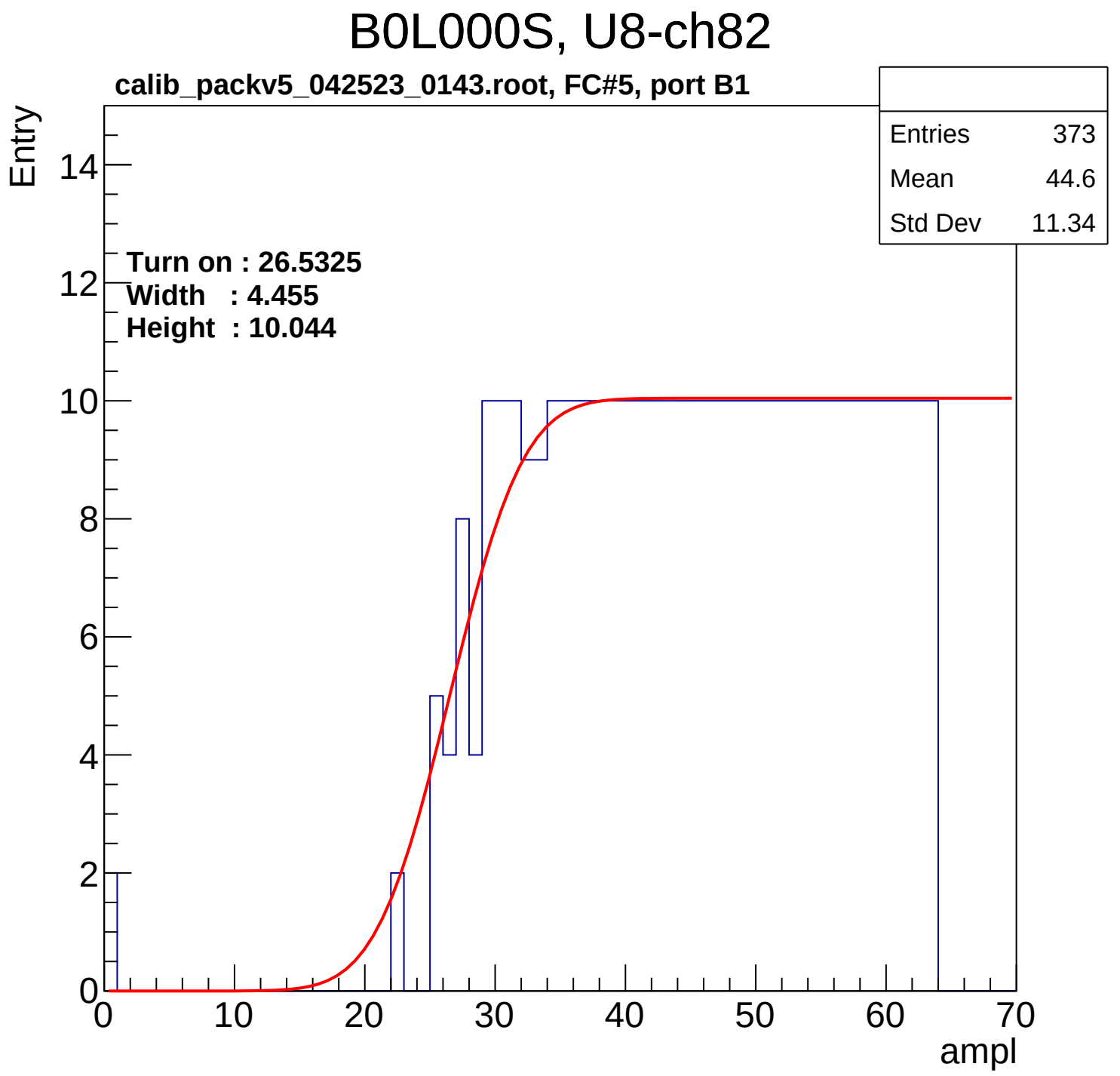
B0L000S, U8-ch82
calib_packv5_042523_0143.root, FC#5, port B1
Entries 373
Mean 44.6
Std Dev 11.34
Turn on : 26.5325
Width : 4.455
Height : 10.044
Entry
ampl
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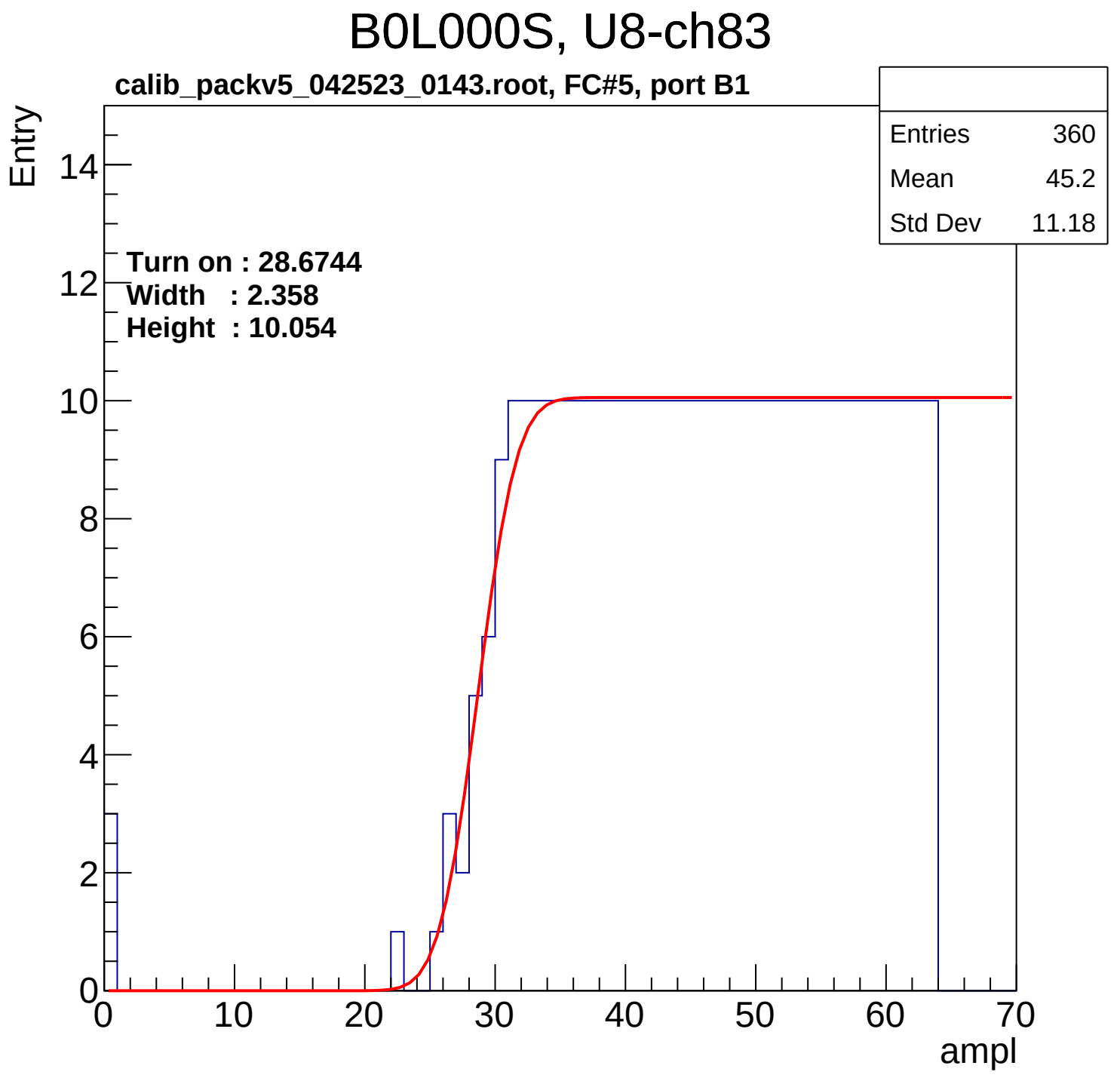
B0L000S, U8-ch83
calib_packv5_042523_0143.root, FC#5, port B1
Entries 360
Mean 45.2
Std Dev 11.18
Turn on : 28.6744
Width : 2.358
Height : 10.054
Entry
ampl
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6
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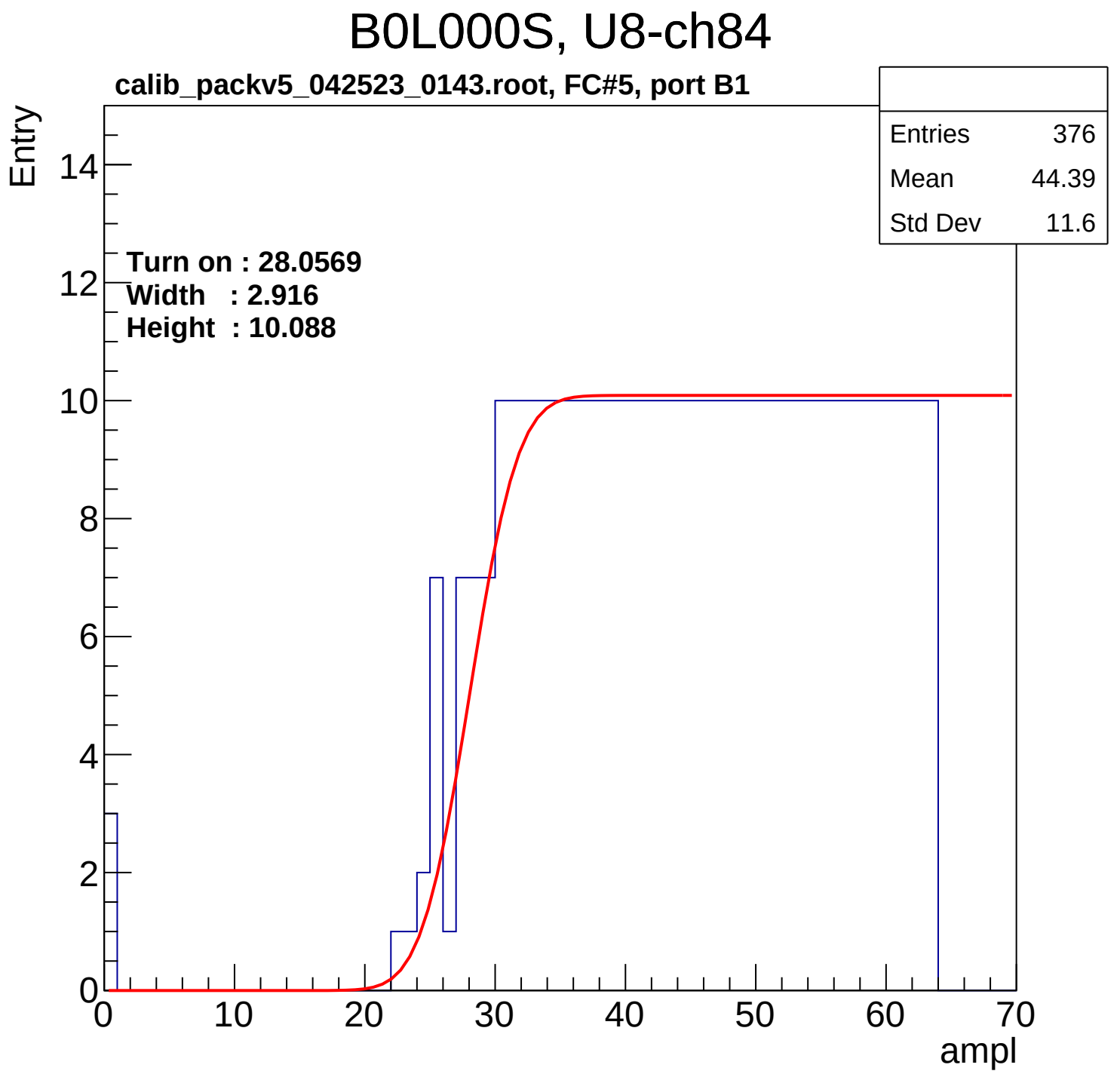
B0L000S, U8-ch84
calib_packv5_042523_0143.root, FC#5, port B1
Entries 376
Mean 44.39
Std Dev 11.6
Turn on : 28.0569
Width : 2.916
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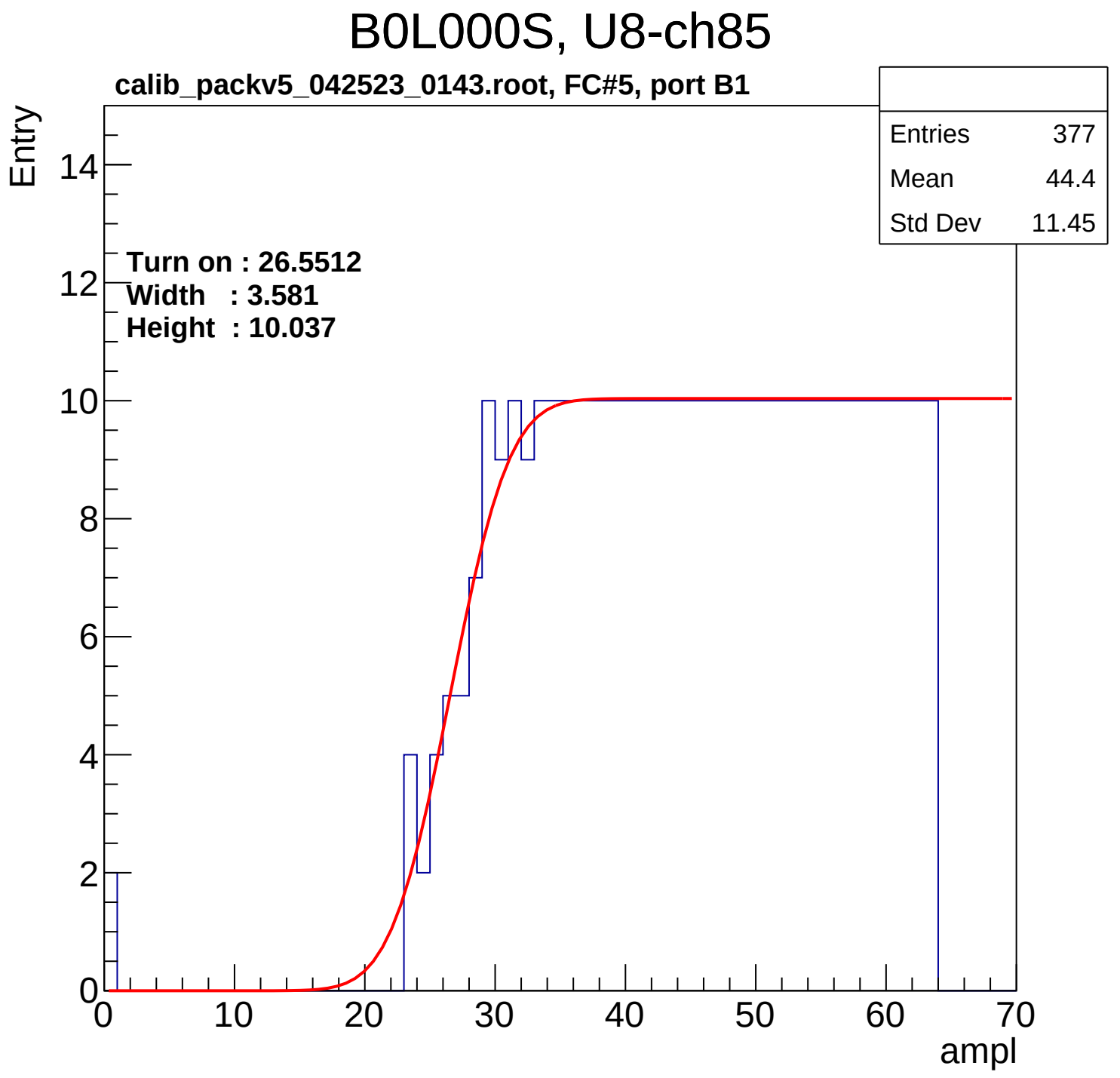
B0L000S, U8-ch85
calib_packv5_042523_0143.root, FC#5, port B1
Entries 377
Mean 44.4
Std Dev 11.45
Turn on : 26.5512
Width : 3.581
Height : 10.037
Entry
ampl
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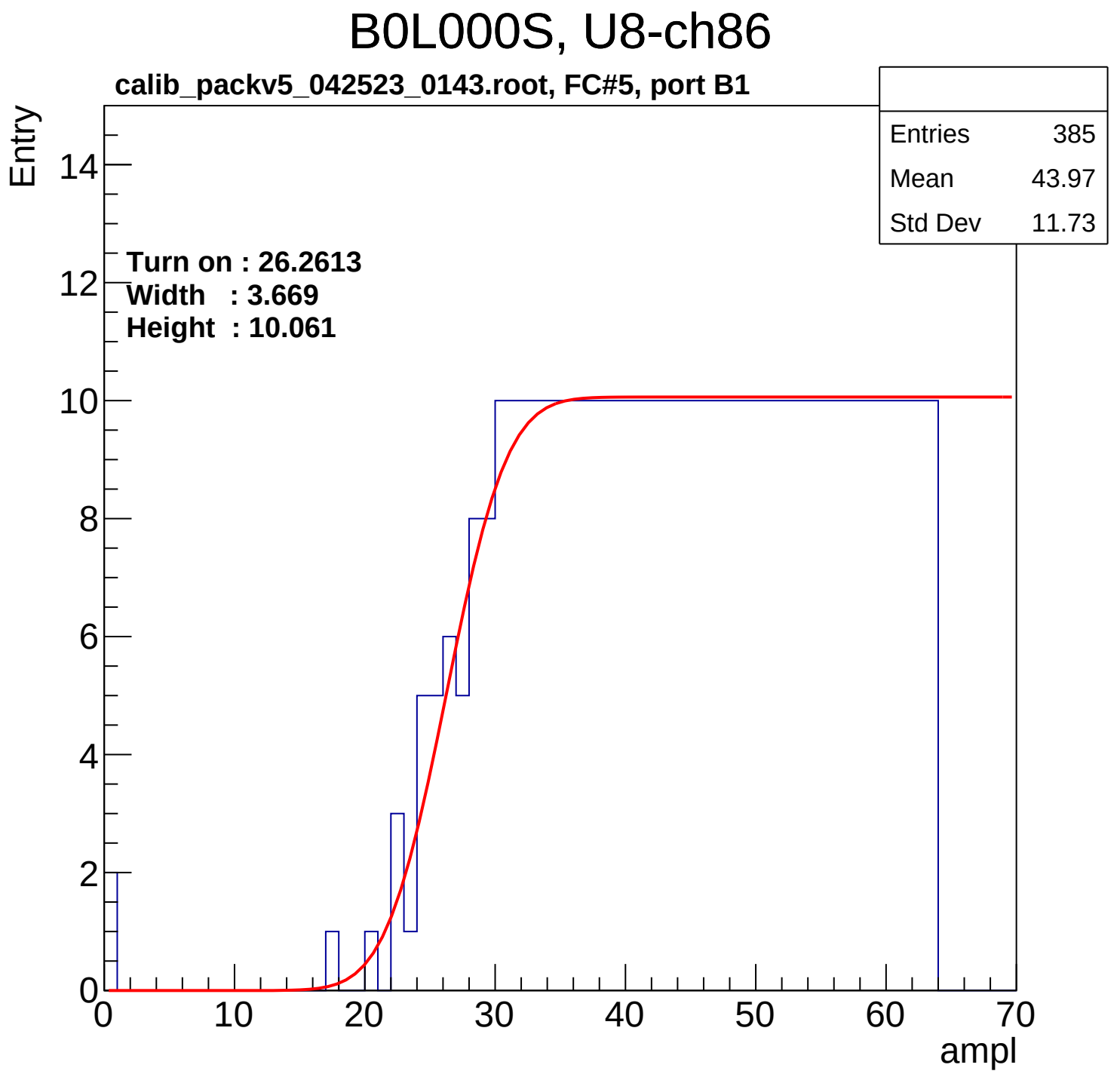
B0L000S, U8-ch86
calib_packv5_042523_0143.root, FC#5, port B1
Entries 385
Mean 43.97
Std Dev 11.73
Turn on : 26.2613
Width : 3.669
Height : 10.061
Entry
ampl
0
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4
6
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12
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10
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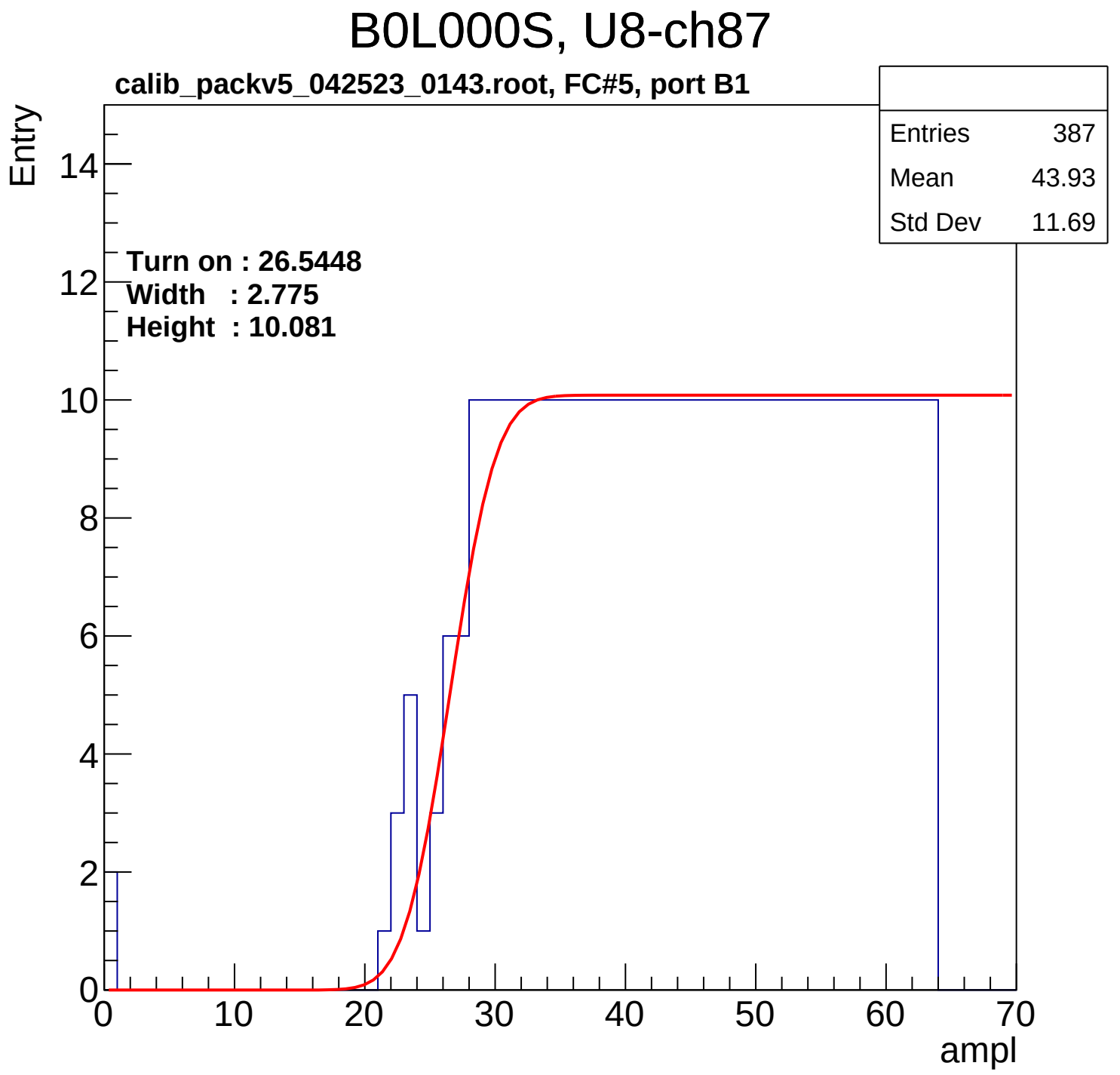
B0L000S, U8-ch87
calib_packv5_042523_0143.root, FC#5, port B1
Entries 387
Mean 43.93
Std Dev 11.69
Turn on : 26.5448
Width : 2.775
Height : 10.081
Entry
ampl
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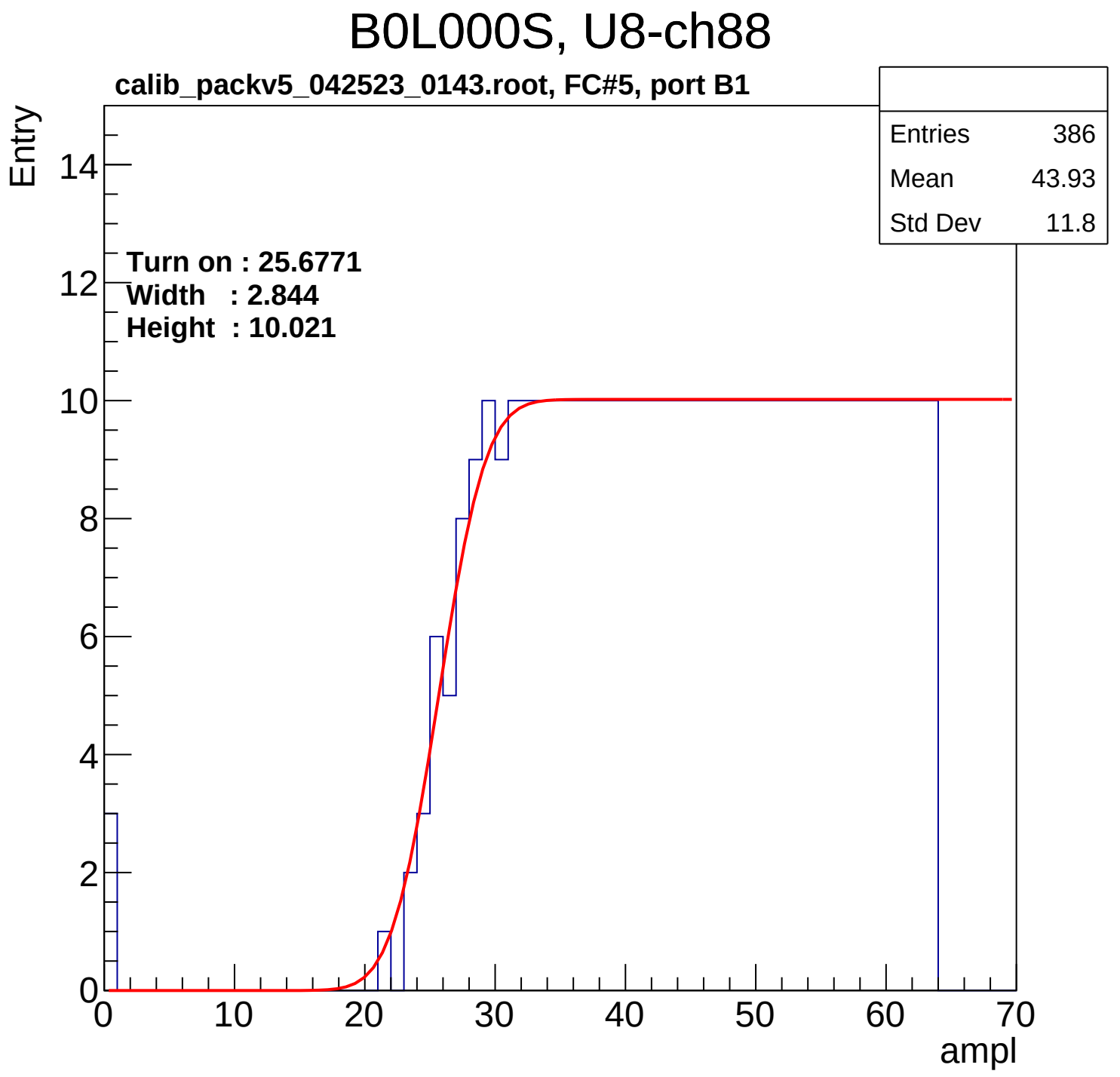
B0L000S, U8-ch88
calib_packv5_042523_0143.root, FC#5, port B1
Entries 386
Mean 43.93
Std Dev 11.8
Turn on : 25.6771
Width : 2.844
Height : 10.021
Entry
ampl
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4
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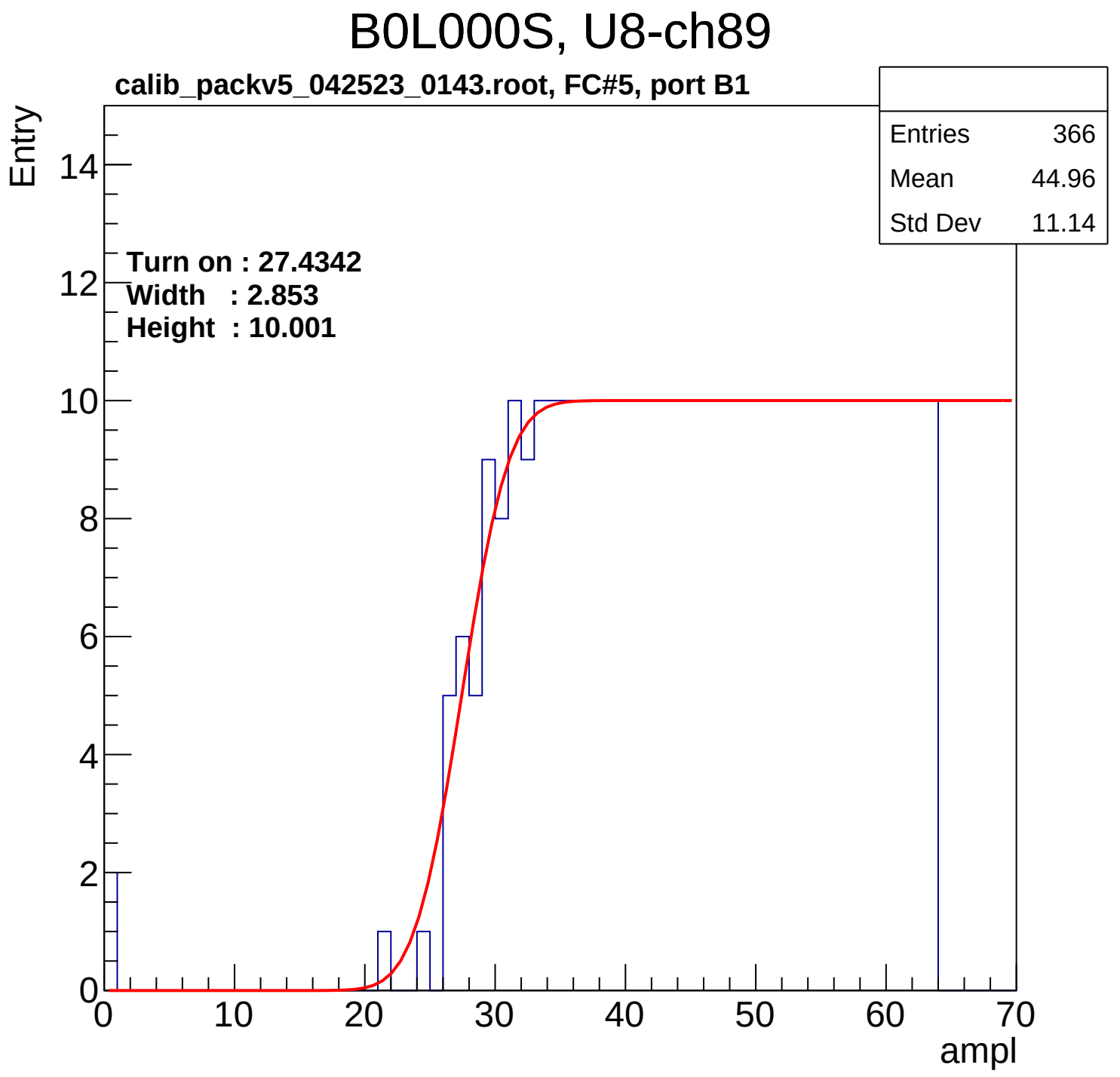
B0L000S, U8-ch89
calib_packv5_042523_0143.root, FC#5, port B1
Entries 366
Mean 44.96
Std Dev 11.14
Turn on : 27.4342
Width : 2.853
Height : 10.001
Entry
ampl
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8
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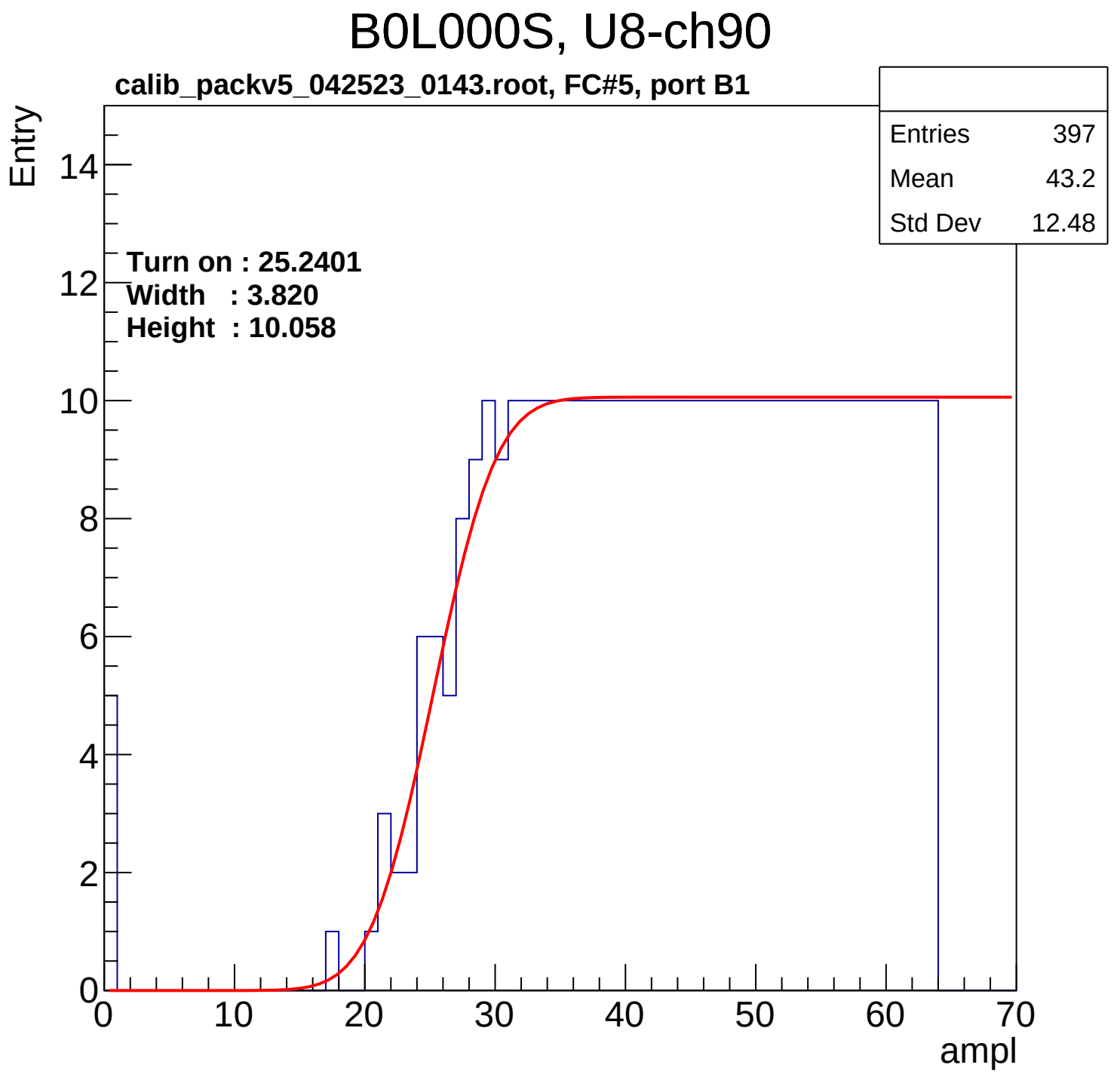
B0L000S, U8-ch90
calib_packv5_042523_0143.root, FC#5, port B1
Entries 397
Mean 43.2
Std Dev 12.48
Turn on : 25.2401
Width : 3.820
Height : 10.058
Entry
ampl
0
2
4
6
8
10
12
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0
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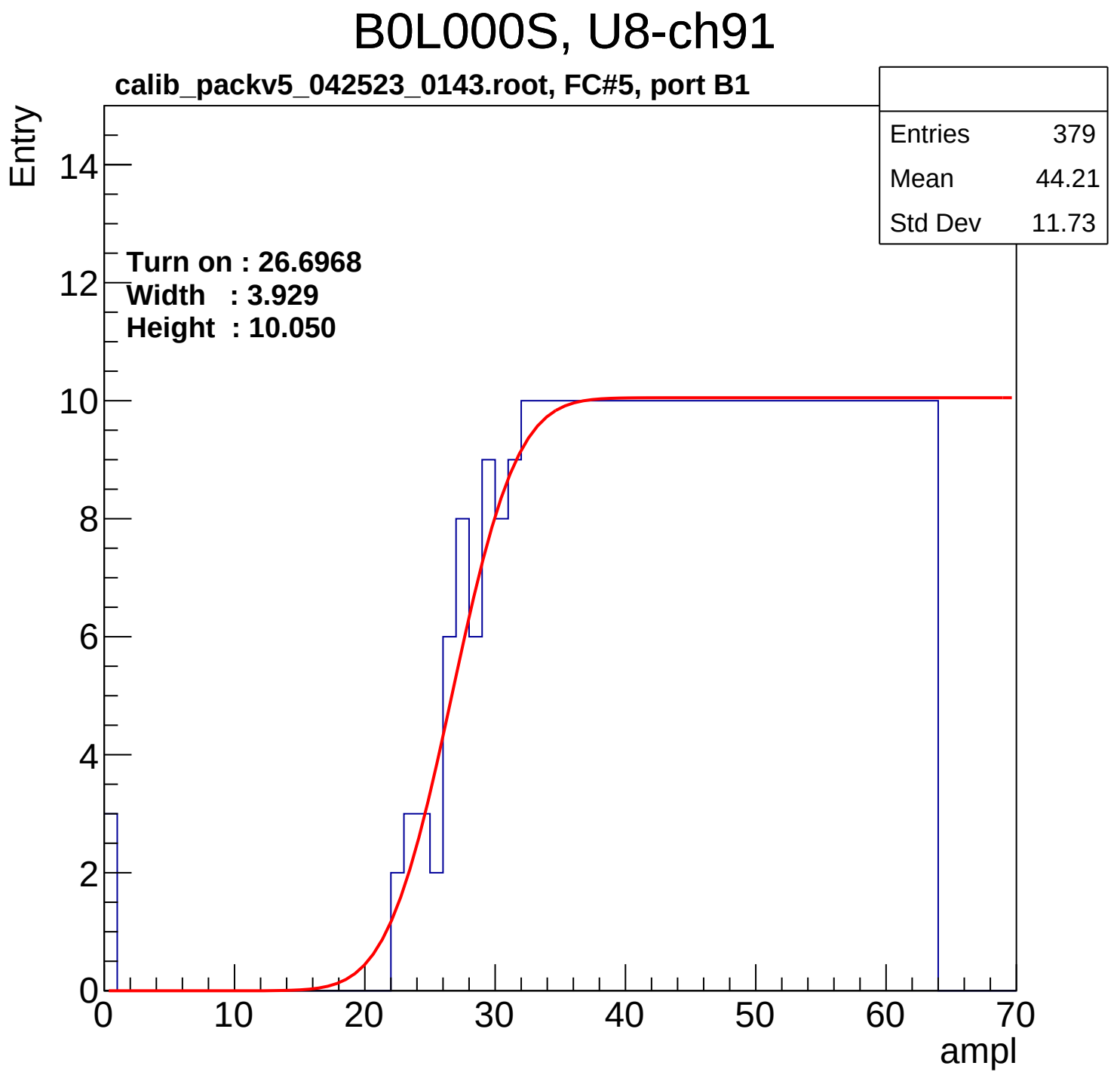
B0L000S, U8-ch91
calib_packv5_042523_0143.root, FC#5, port B1
Entries 379
Mean 44.21
Std Dev 11.73
Turn on : 26.6968
Width : 3.929
Height : 10.050
Entry
ampl
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2
4
6
8
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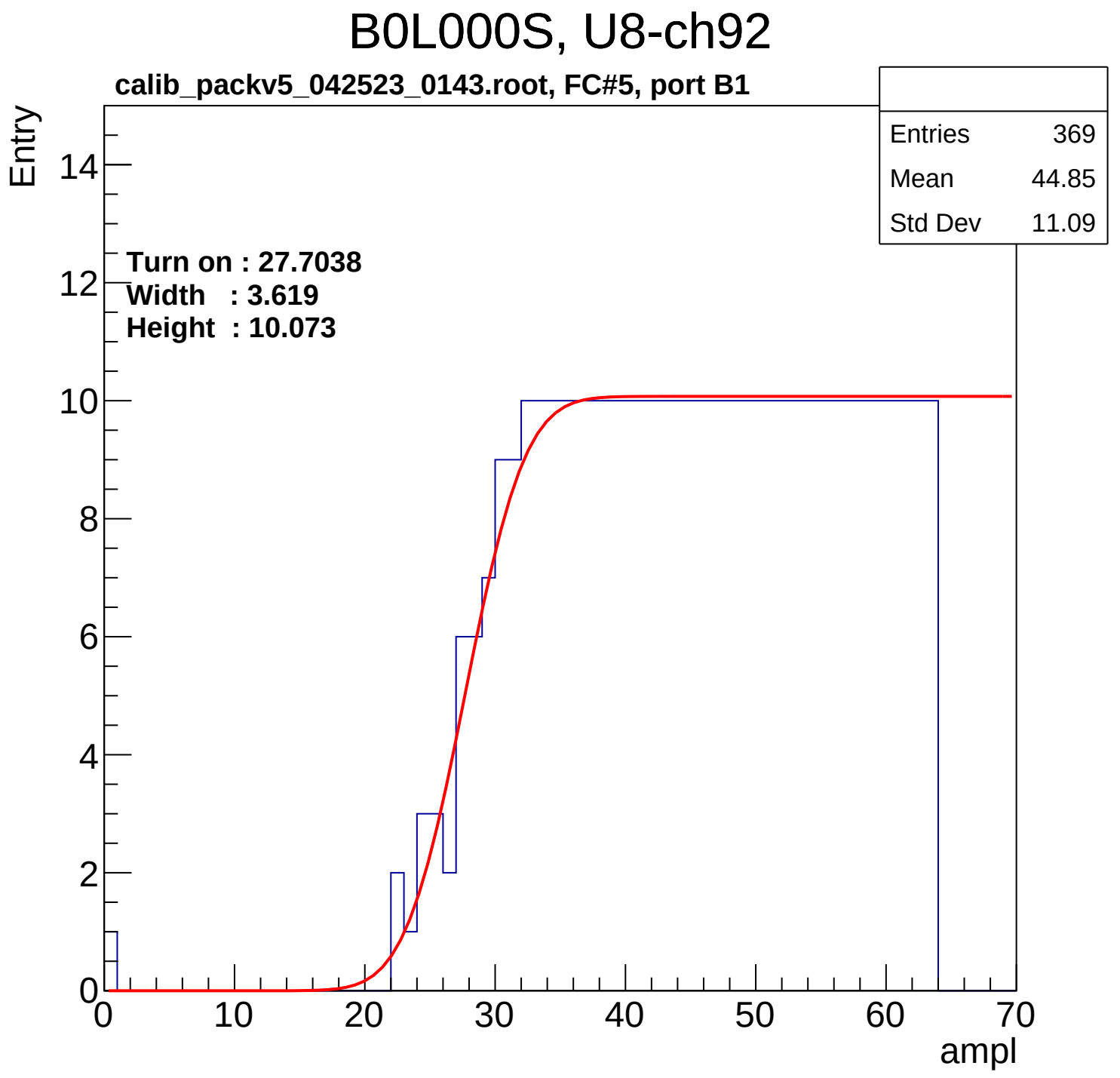
B0L000S, U8-ch92
calib_packv5_042523_0143.root, FC#5, port B1
Entries 369
Mean 44.85
Std Dev 11.09
Turn on : 27.7038
Width : 3.619
Height : 10.073
Entry
ampl
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2
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6
8
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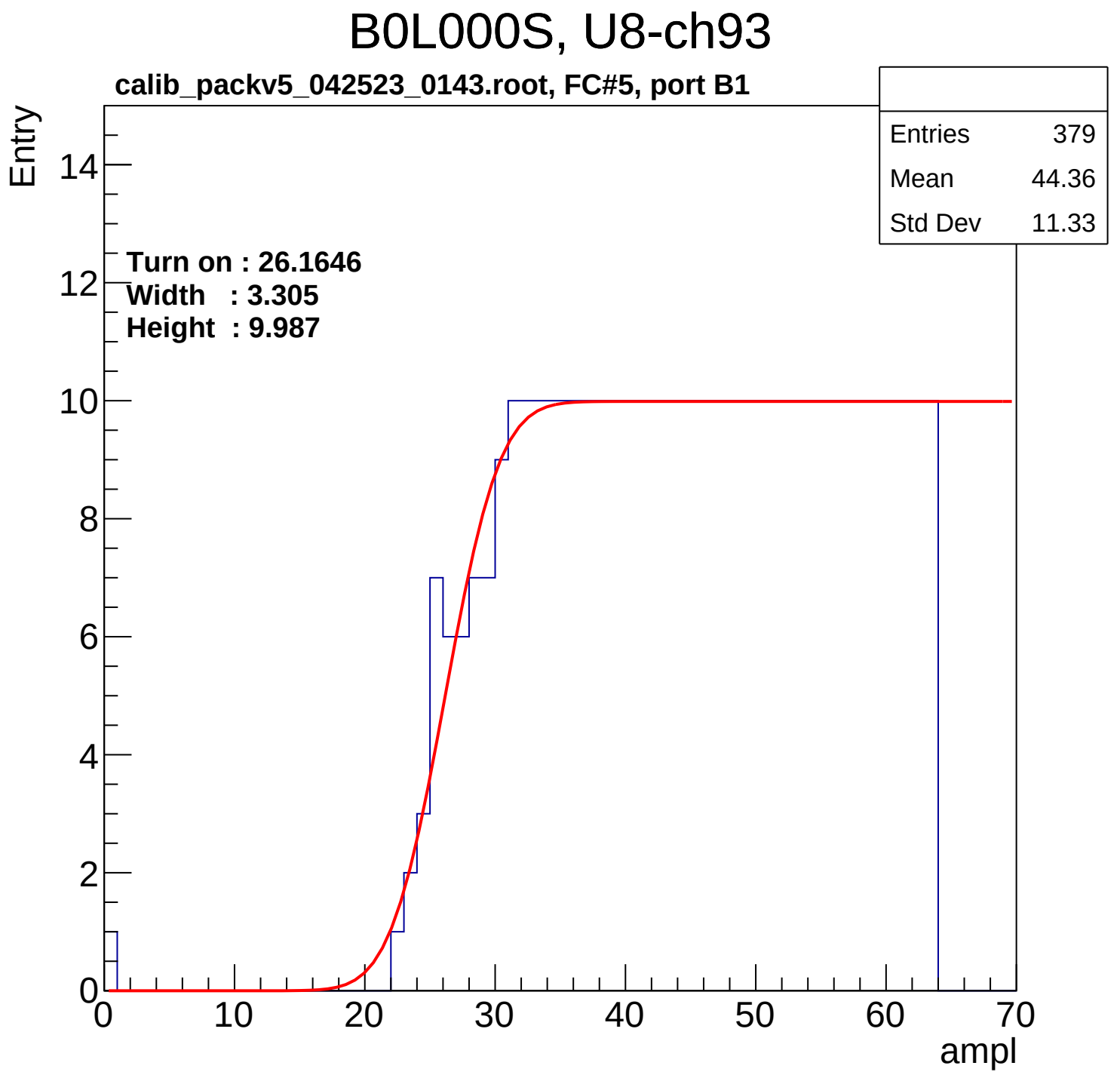
B0L000S, U8-ch93
calib_packv5_042523_0143.root, FC#5, port B1
Entries 379
Mean 44.36
Std Dev 11.33
Turn on : 26.1646
Width : 3.305
Height : 9.987
Entry
ampl
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2
4
6
8
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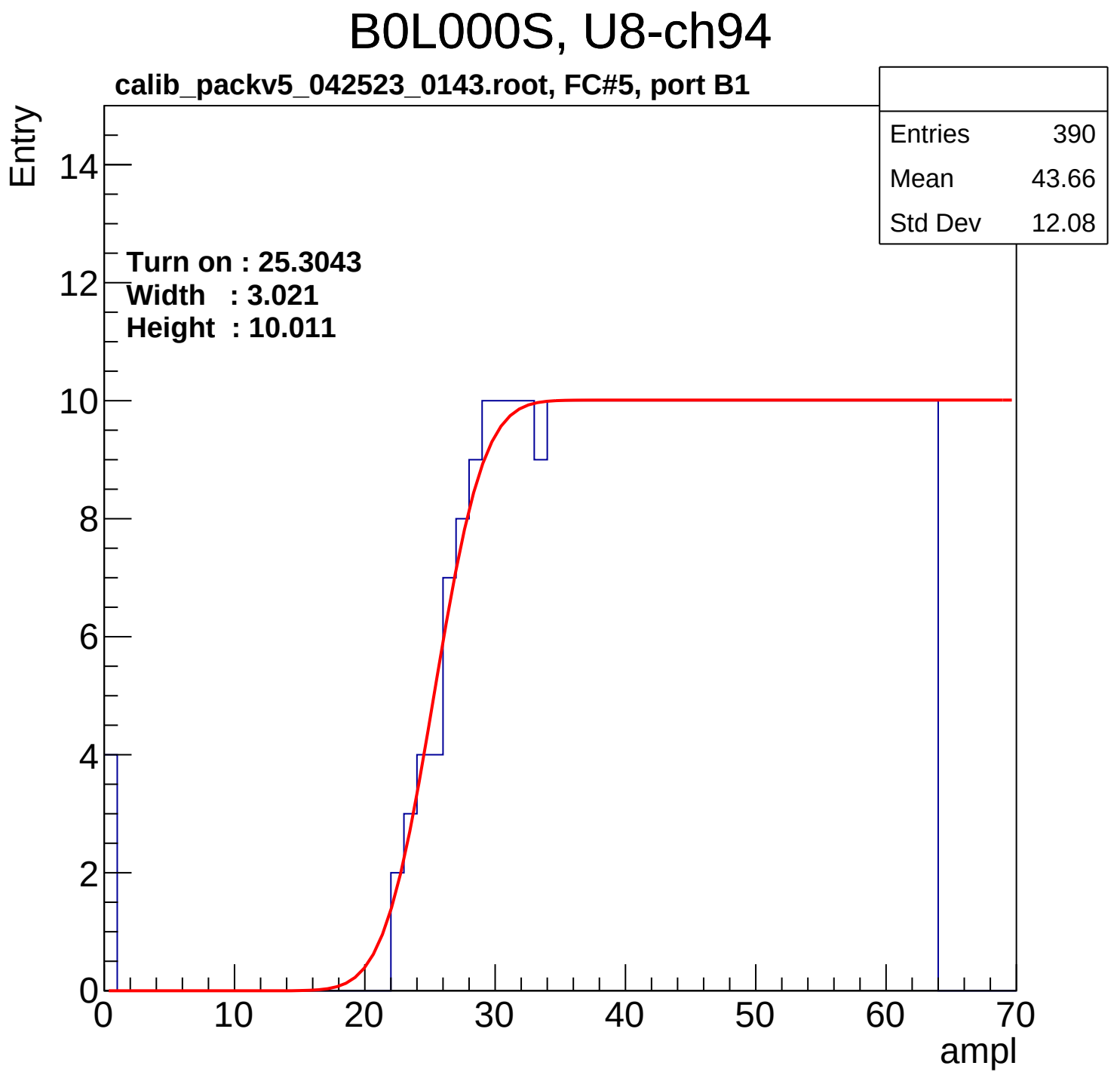
B0L000S, U8-ch94
calib_packv5_042523_0143.root, FC#5, port B1
Entries 390
Mean 43.66
Std Dev 12.08
Turn on : 25.3043
Width : 3.021
Height : 10.011
Entry
ampl
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2
4
6
8
10
12
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0
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40
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60
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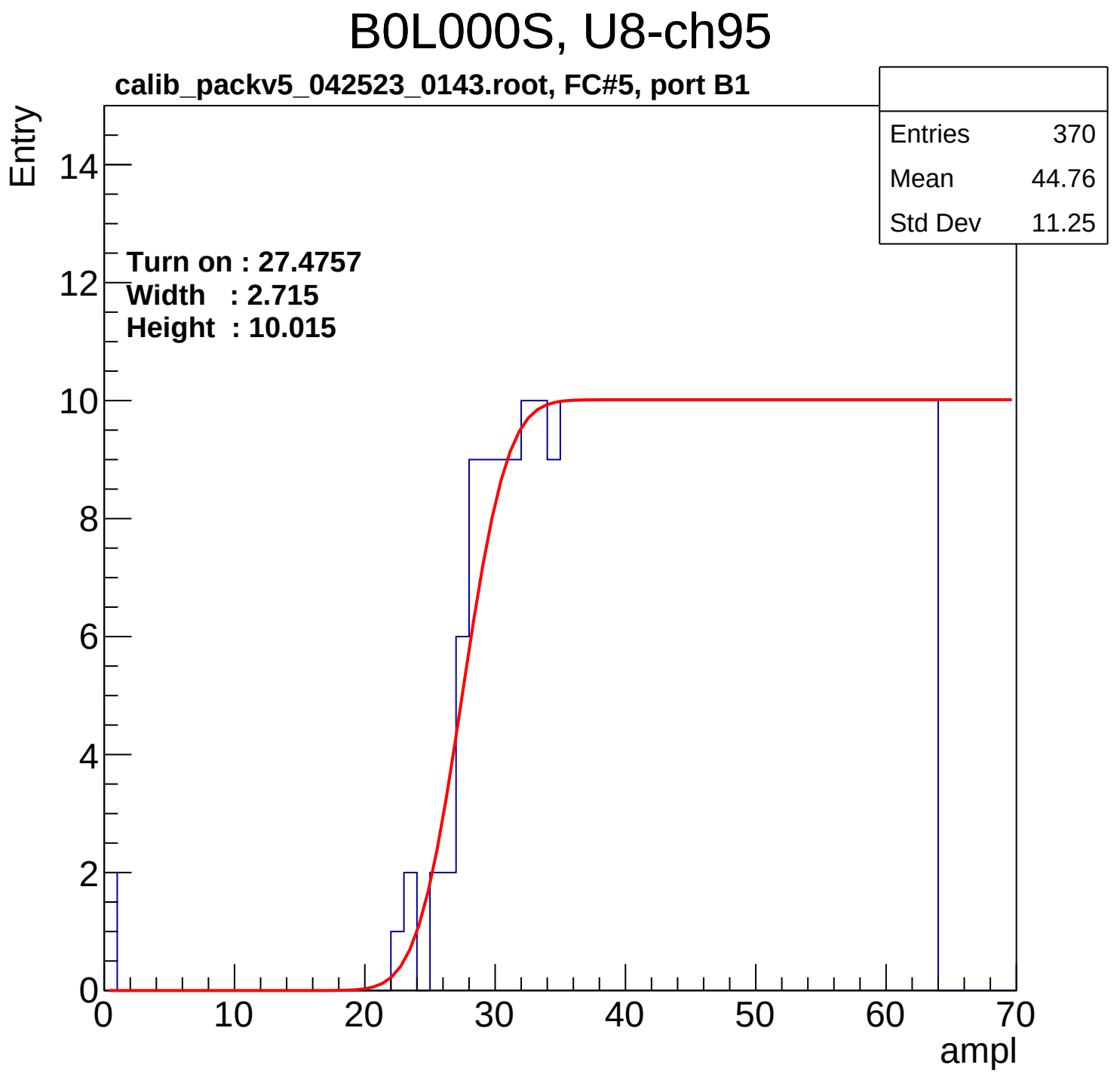
B0L000S, U8-ch95
calib_packv5_042523_0143.root, FC#5, port B1
Entries 370
Mean 44.76
Std Dev 11.25
Turn on : 27.4757
Width : 2.715
Height : 10.015
Entry
ampl
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4
6
8
10
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60
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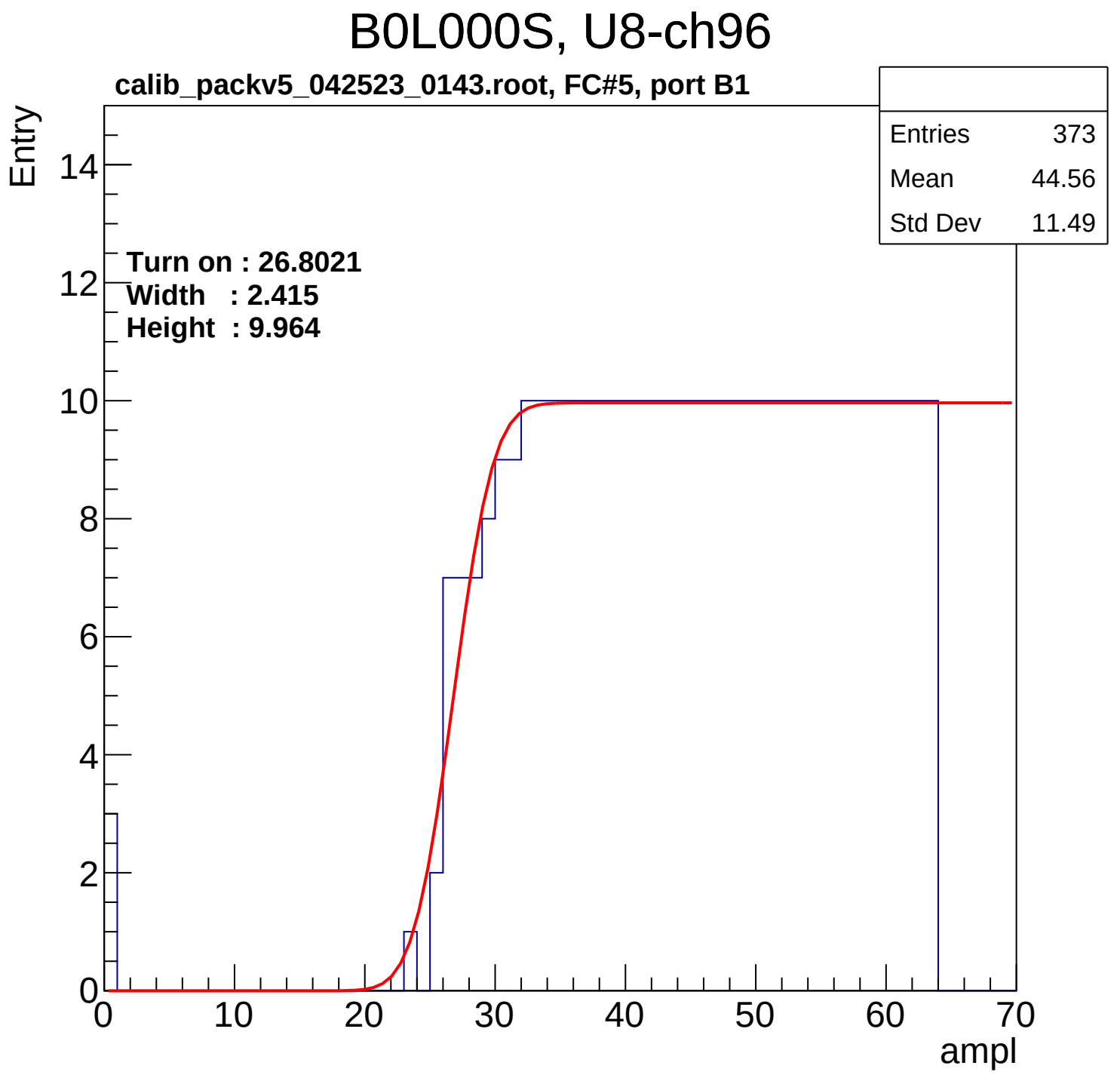
B0L000S, U8-ch96
calib_packv5_042523_0143.root, FC#5, port B1
Entries 373
Mean 44.56
Std Dev 11.49
Turn on : 26.8021
Width : 2.415
Height : 9.964
Entry
ampl
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2
4
6
8
10
12
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0
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60
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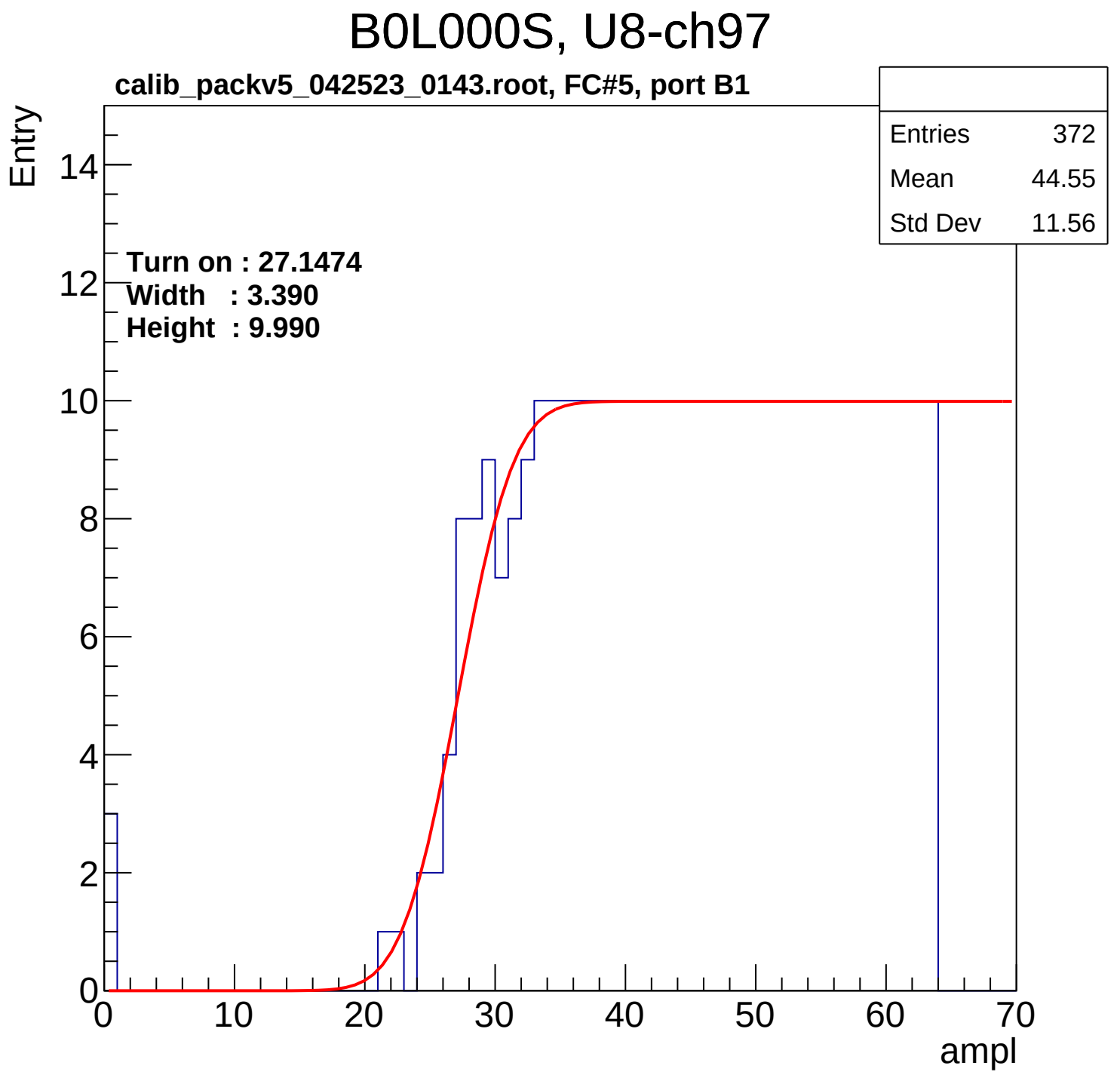
B0L000S, U8-ch97
calib_packv5_042523_0143.root, FC#5, port B1
Entries 372
Mean 44.55
Std Dev 11.56
Turn on : 27.1474
Width : 3.390
Height : 9.990
Entry
ampl
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2
4
6
8
10
12
14
0
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60
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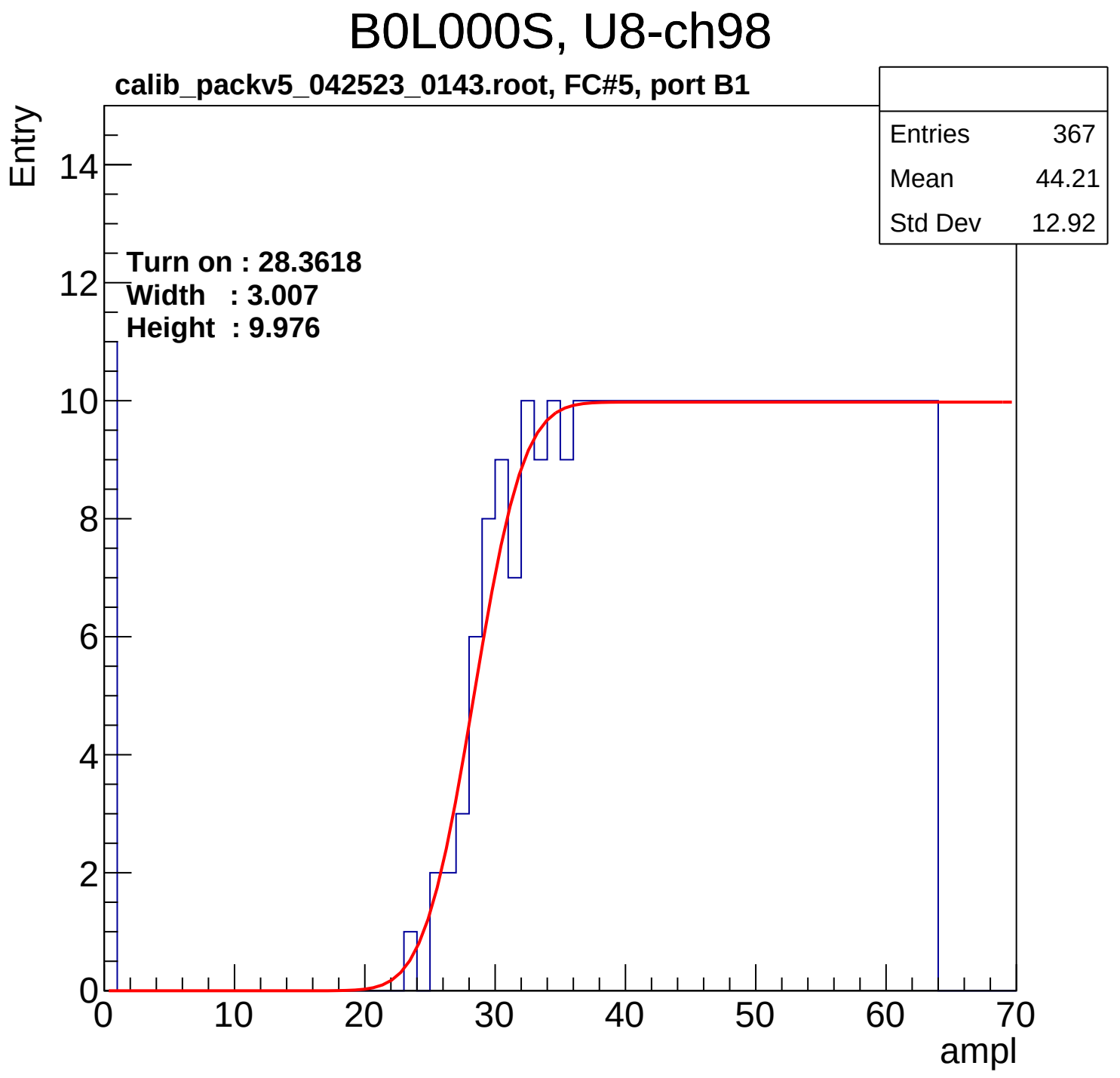
B0L000S, U8-ch98
calib_packv5_042523_0143.root, FC#5, port B1
Entries 367
Mean 44.21
Std Dev 12.92
Turn on : 28.3618
Width : 3.007
Height : 9.976
Entry
ampl
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2
4
6
8
10
12
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0
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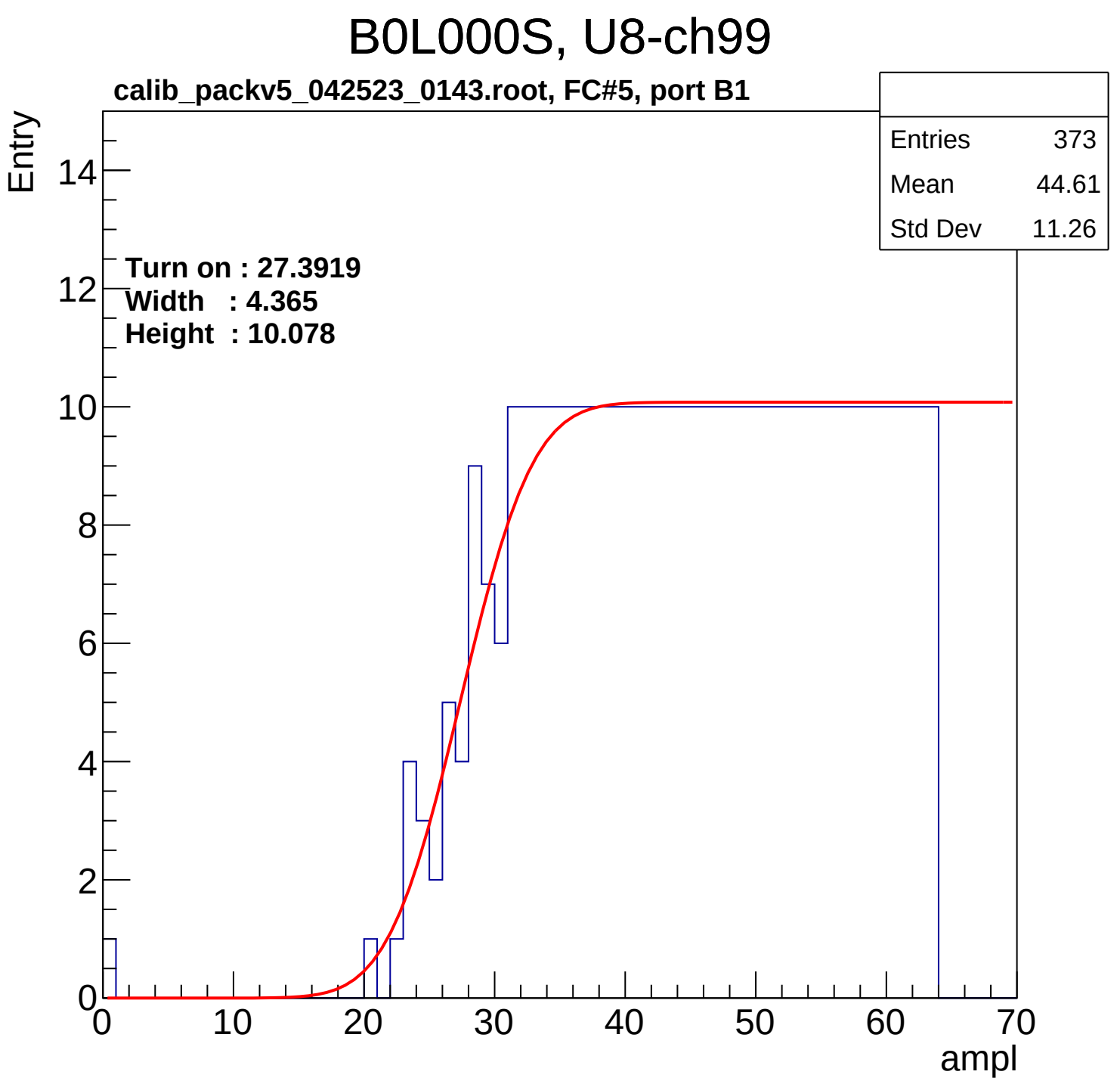
B0L000S, U8-ch99
calib_packv5_042523_0143.root, FC#5, port B1
Entries 373
Mean 44.61
Std Dev 11.26
Turn on : 27.3919
Width : 4.365
Height : 10.078
Entry
ampl
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2
4
6
8
10
12
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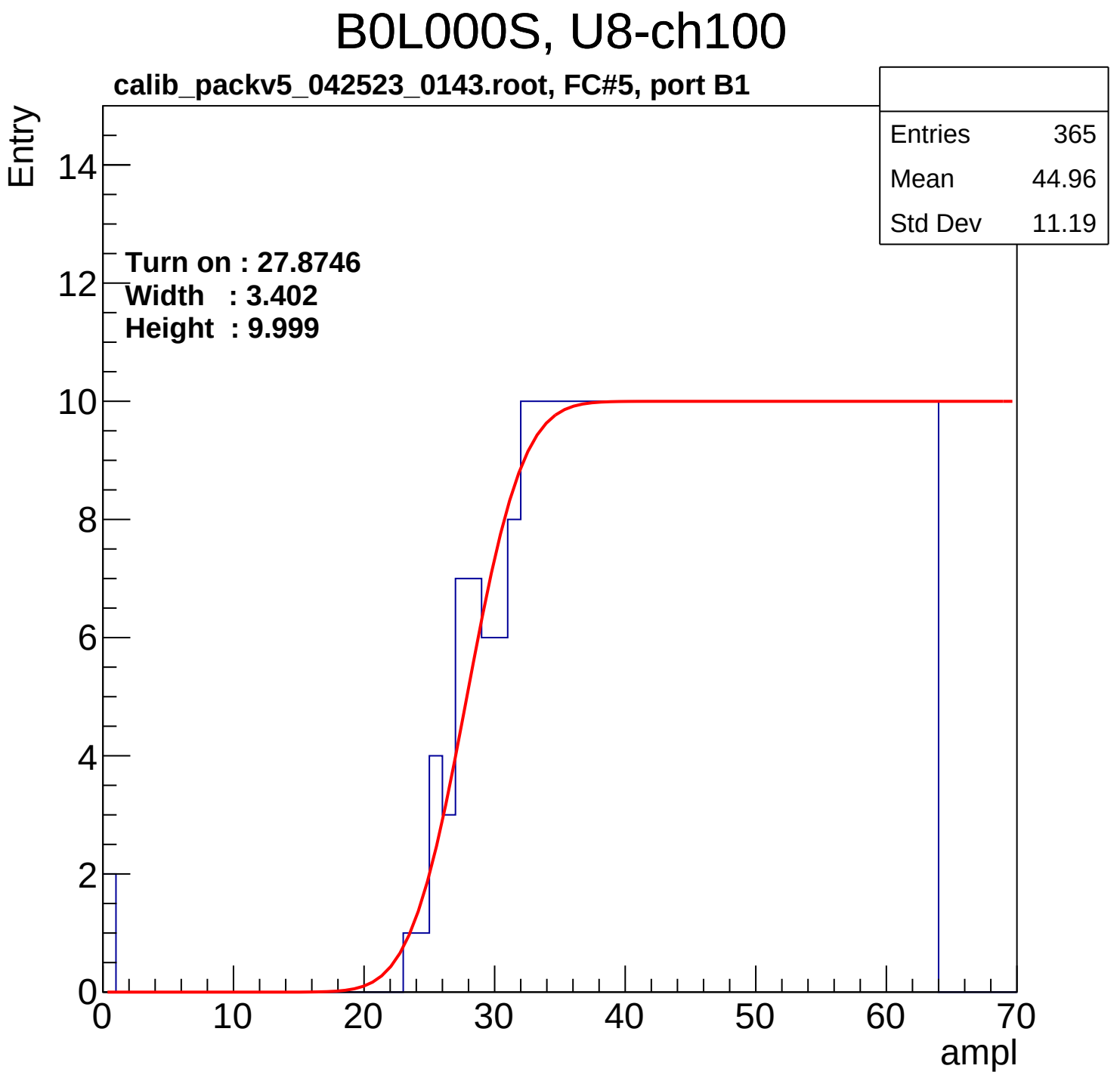
B0L000S, U8-ch100
calib_packv5_042523_0143.root, FC#5, port B1
Entries 365
Mean 44.96
Std Dev 11.19
Turn on : 27.8746
Width : 3.402
Height : 9.999
Entry
ampl
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2
4
6
8
10
12
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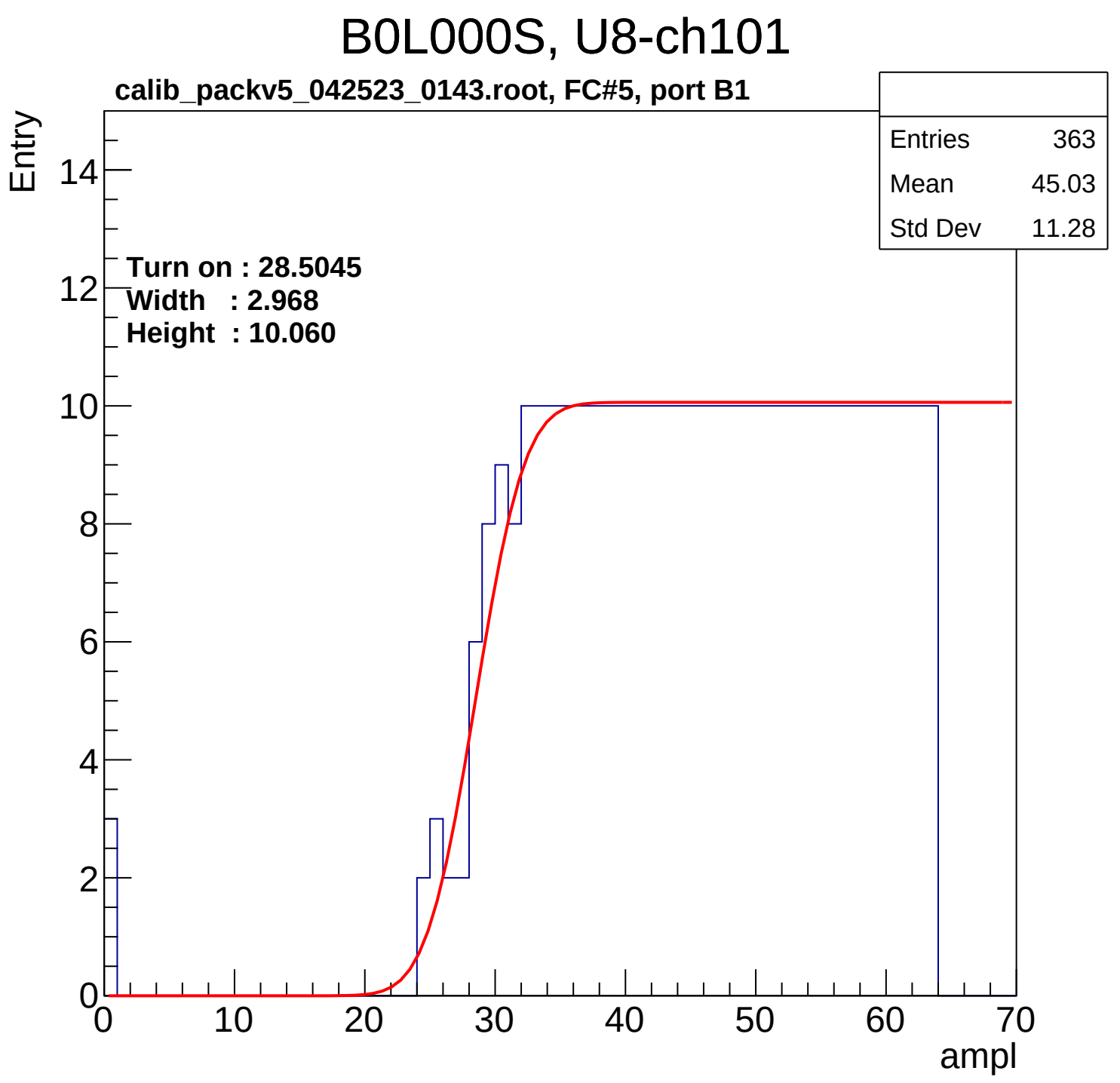
B0L000S, U8-ch101
calib_packv5_042523_0143.root, FC#5, port B1
Entries 363
Mean 45.03
Std Dev 11.28
Turn on : 28.5045
Width : 2.968
Height : 10.060
Entry
ampl
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6
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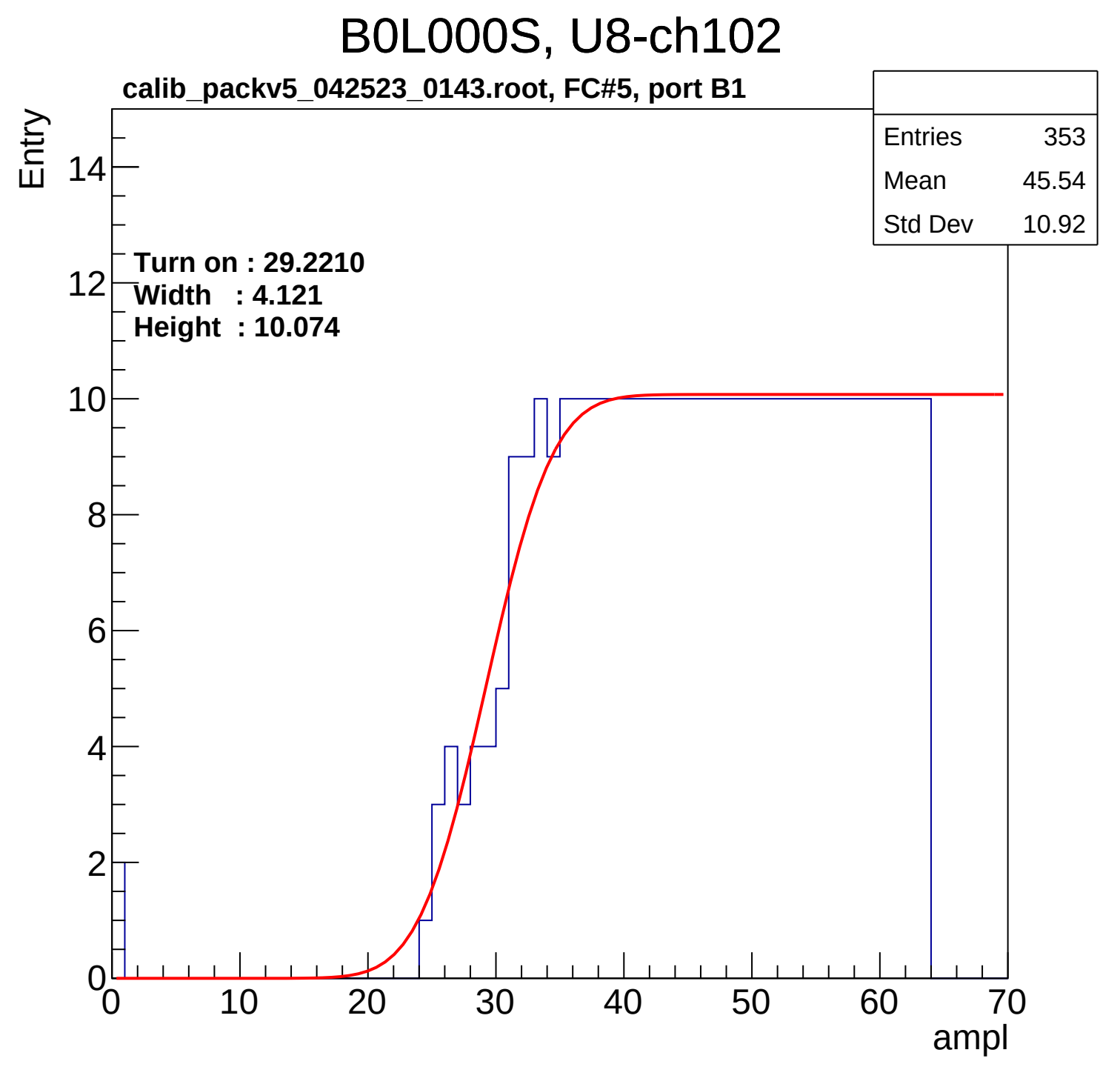
B0L000S, U8-ch102
calib_packv5_042523_0143.root, FC#5, port B1
Entries 353
Mean 45.54
Std Dev 10.92
Turn on : 29.2210
Width : 4.121
Height : 10.074
Entry
ampl
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6
8
10
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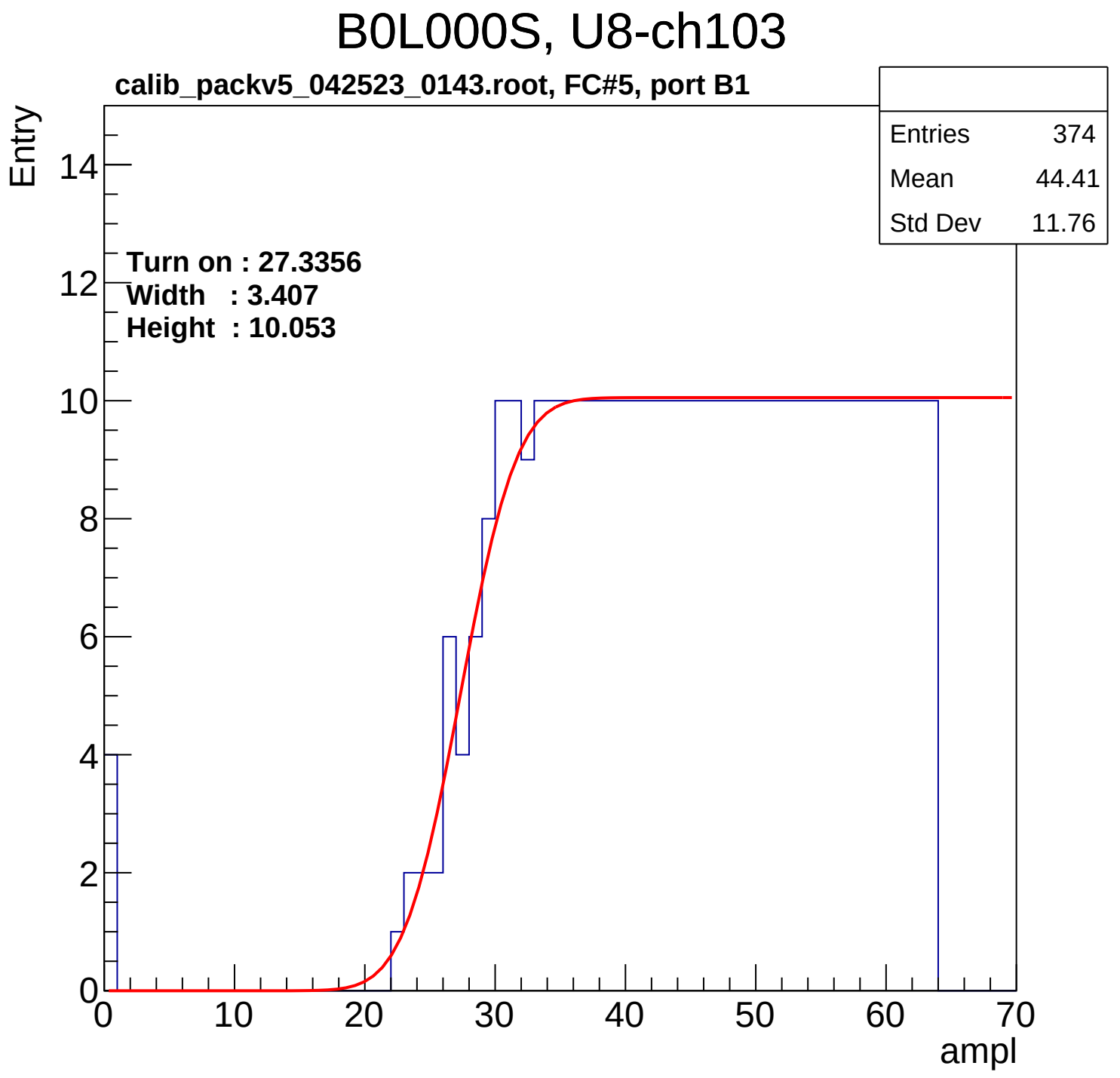
B0L000S, U8-ch103
calib_packv5_042523_0143.root, FC#5, port B1
Entries 374
Mean 44.41
Std Dev 11.76
Turn on : 27.3356
Width : 3.407
Height : 10.053
Entry
ampl
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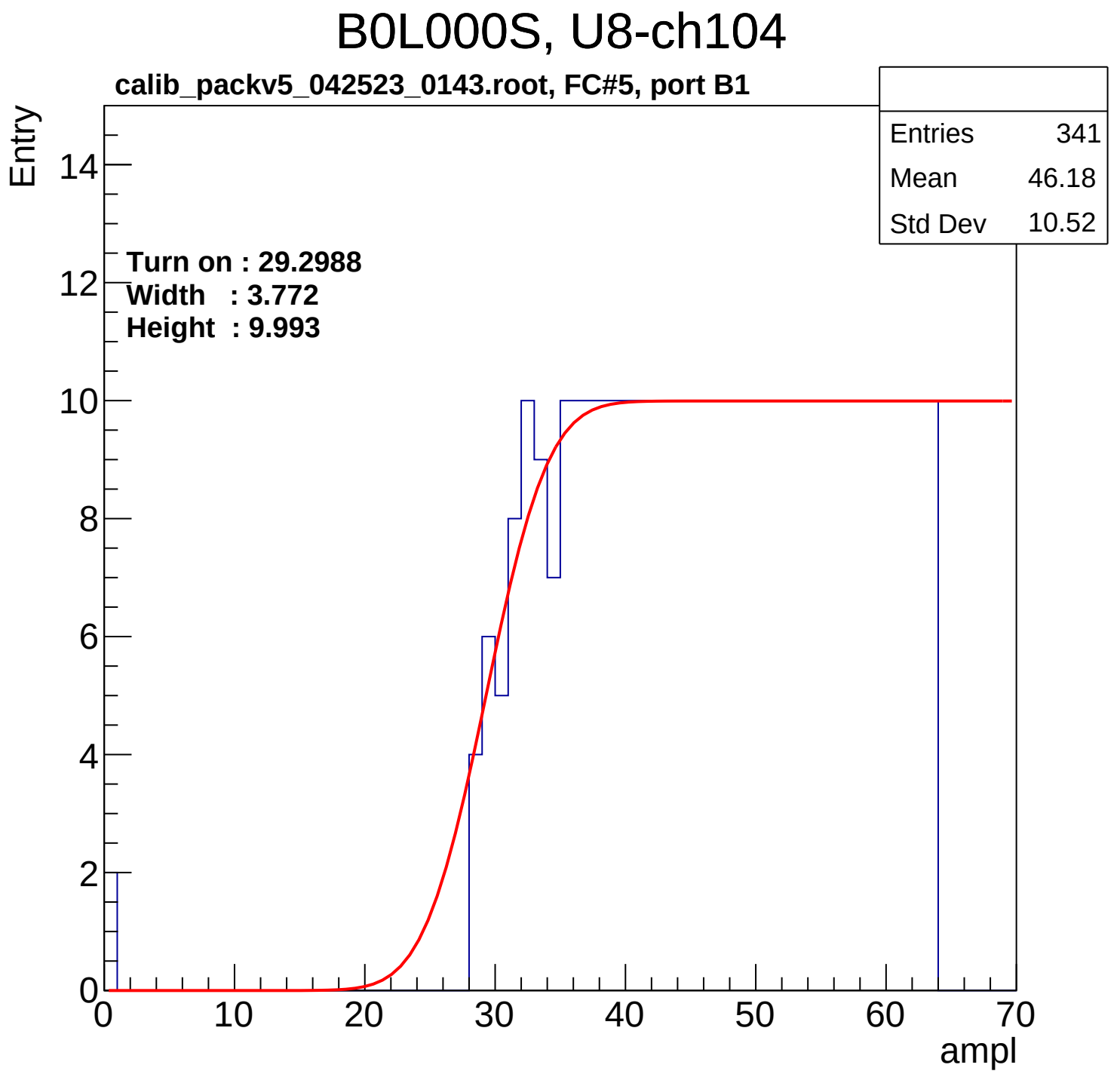
B0L000S, U8-ch104
calib_packv5_042523_0143.root, FC#5, port B1
Entries 341
Mean 46.18
Std Dev 10.52
Turn on : 29.2988
Width : 3.772
Height : 9.993
Entry
ampl
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8
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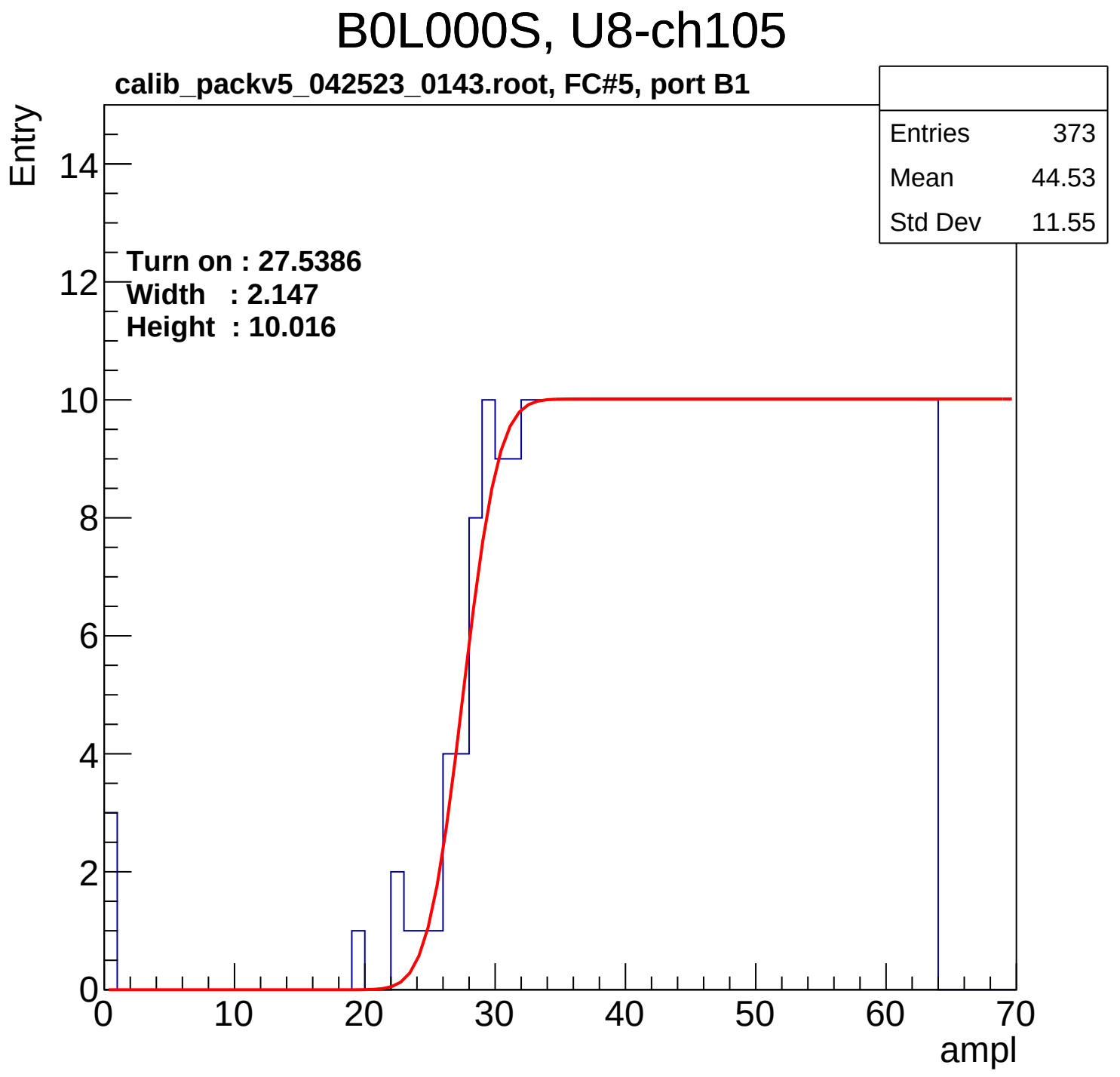
B0L000S, U8-ch105
calib_packv5_042523_0143.root, FC#5, port B1
Entries 373
Mean 44.53
Std Dev 11.55
Turn on : 27.5386
Width : 2.147
Height : 10.016
Entry
ampl
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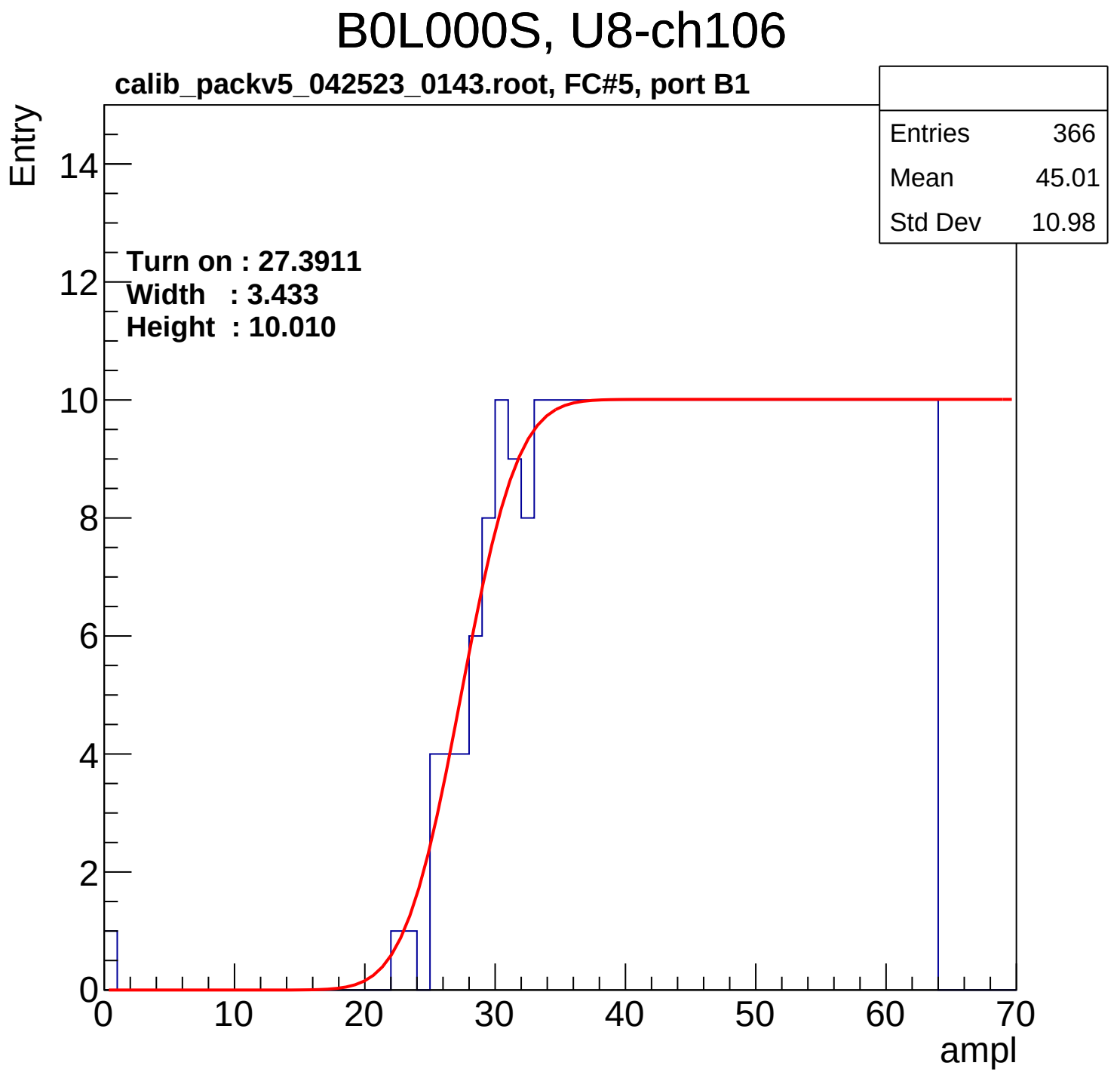
B0L000S, U8-ch106
calib_packv5_042523_0143.root, FC#5, port B1
Entries 366
Mean 45.01
Std Dev 10.98
Turn on : 27.3911
Width : 3.433
Height : 10.010
Entry
ampl
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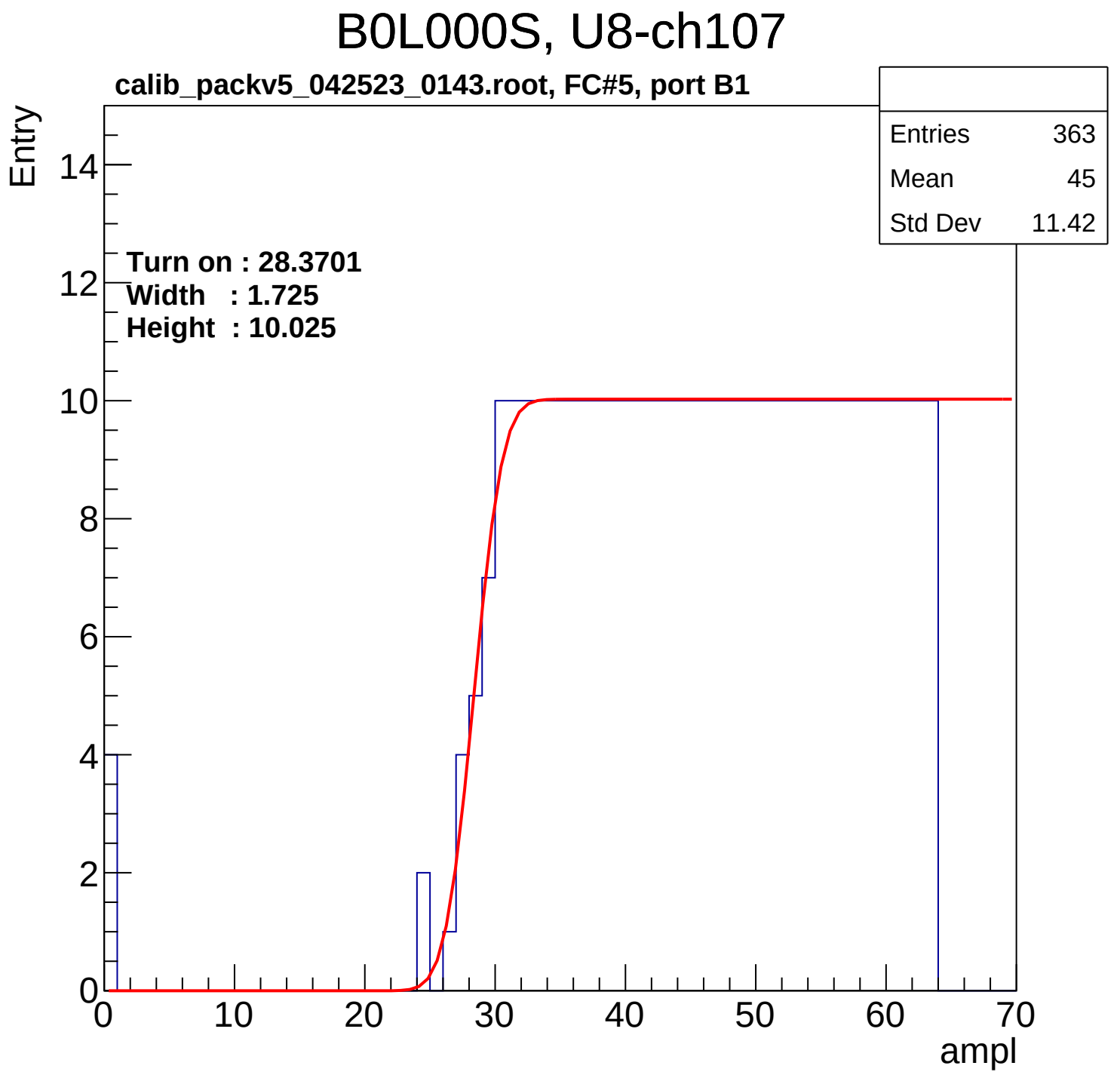
B0L000S, U8-ch107
calib_packv5_042523_0143.root, FC#5, port B1
Entries 363
Mean 45
Std Dev 11.42
Turn on : 28.3701
Width : 1.725
Height : 10.025
Entry
ampl
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8
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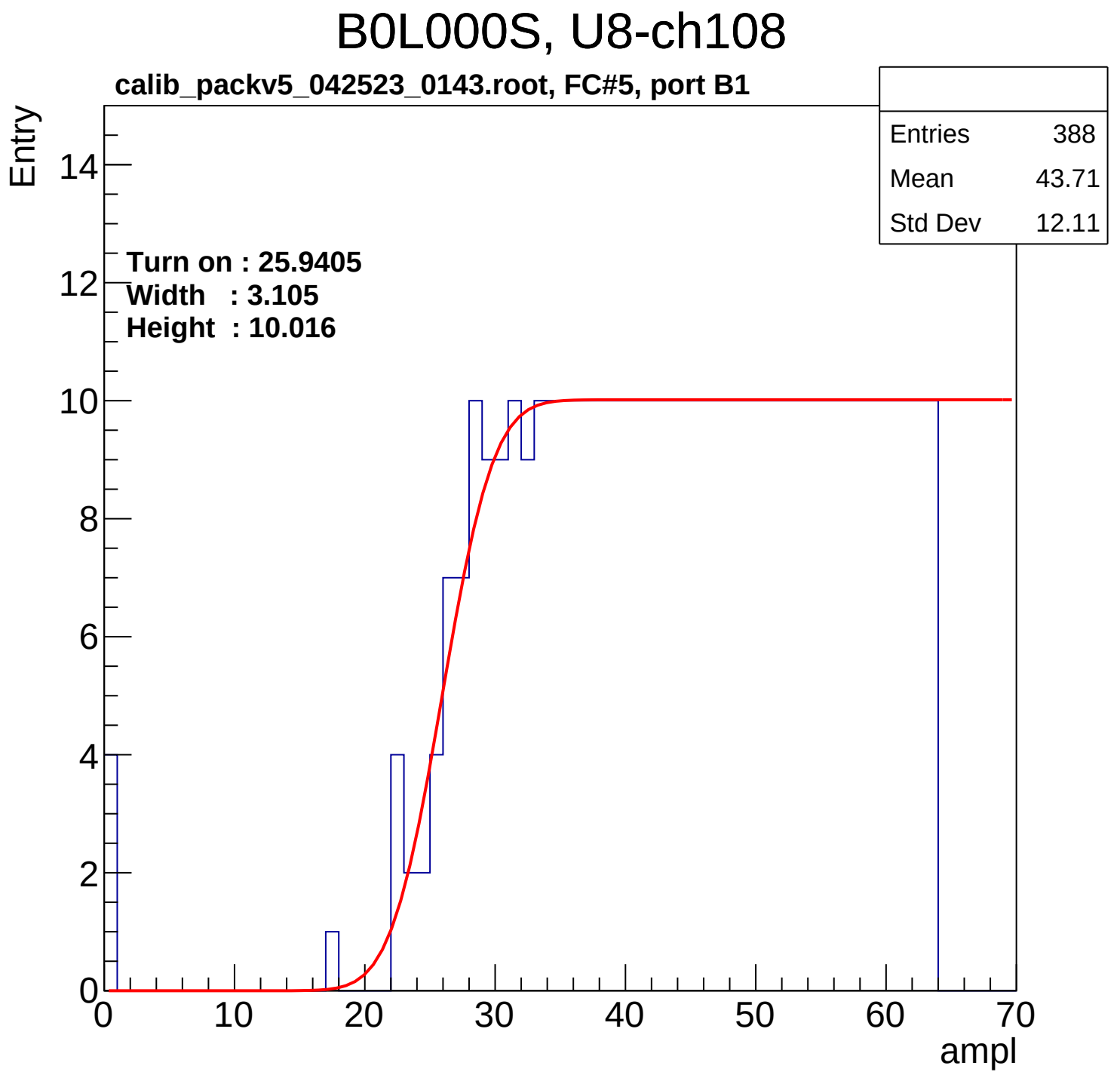
B0L000S, U8-ch108
calib_packv5_042523_0143.root, FC#5, port B1
Entries 388
Mean 43.71
Std Dev 12.11
Turn on : 25.9405
Width : 3.105
Height : 10.016
Entry
ampl
0
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6
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10
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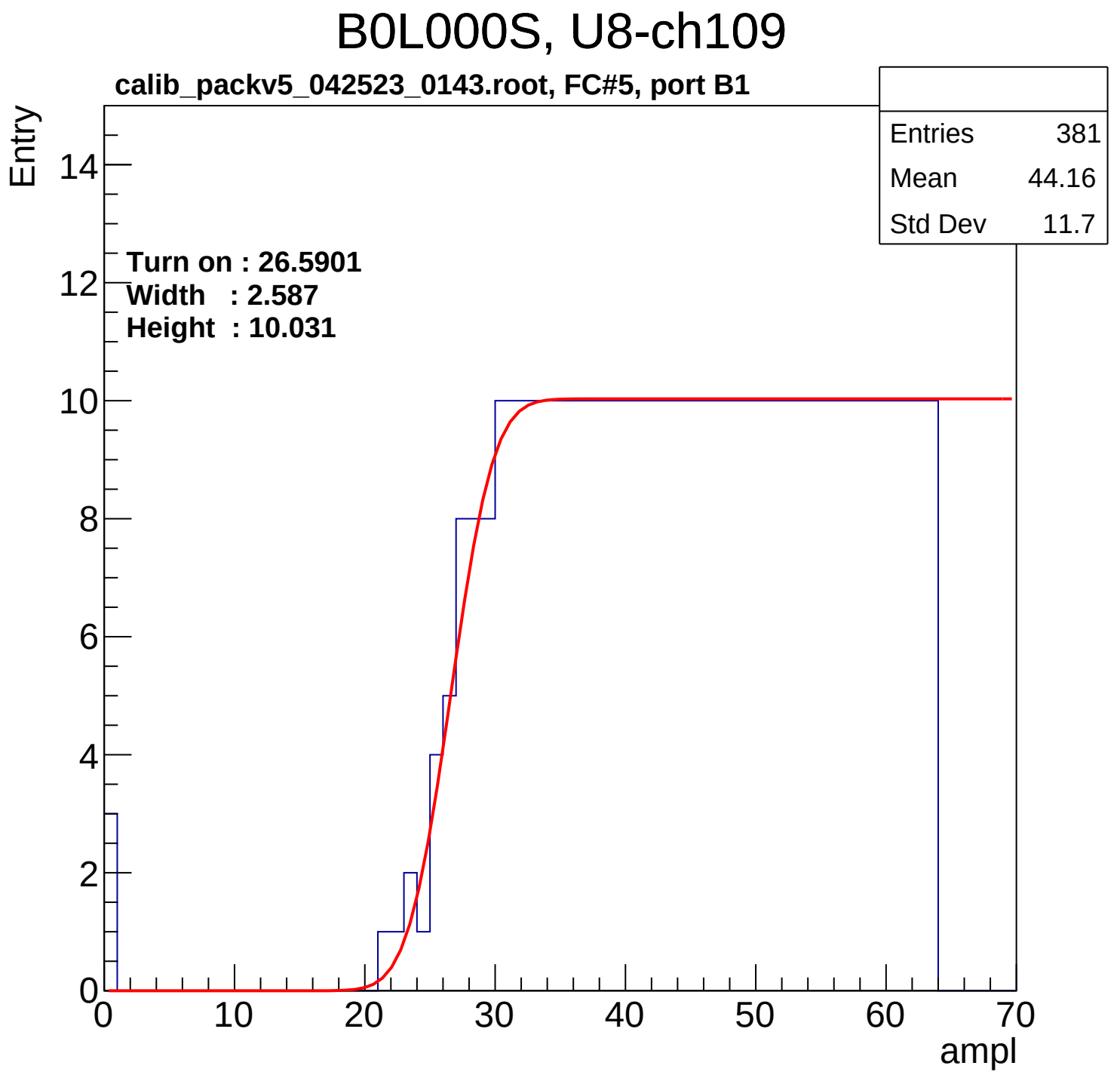
B0L000S, U8-ch109
calib_packv5_042523_0143.root, FC#5, port B1
Entries 381
Mean 44.16
Std Dev 11.7
Turn on : 26.5901
Width : 2.587
Height : 10.031
Entry
ampl
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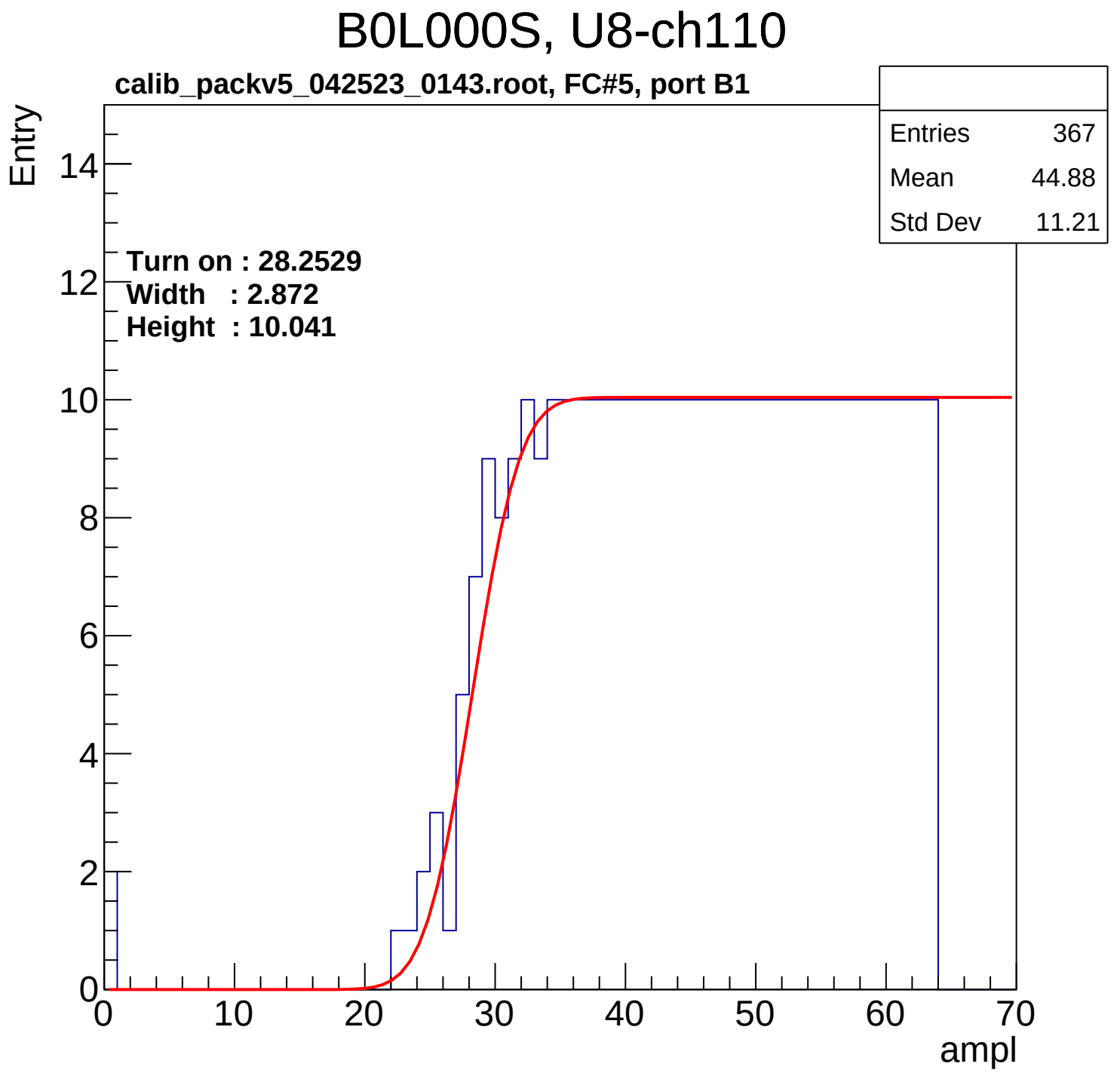
B0L000S, U8-ch110
calib_packv5_042523_0143.root, FC#5, port B1
Entries 367
Mean 44.88
Std Dev 11.21
Turn on : 28.2529
Width : 2.872
Height : 10.041
Entry
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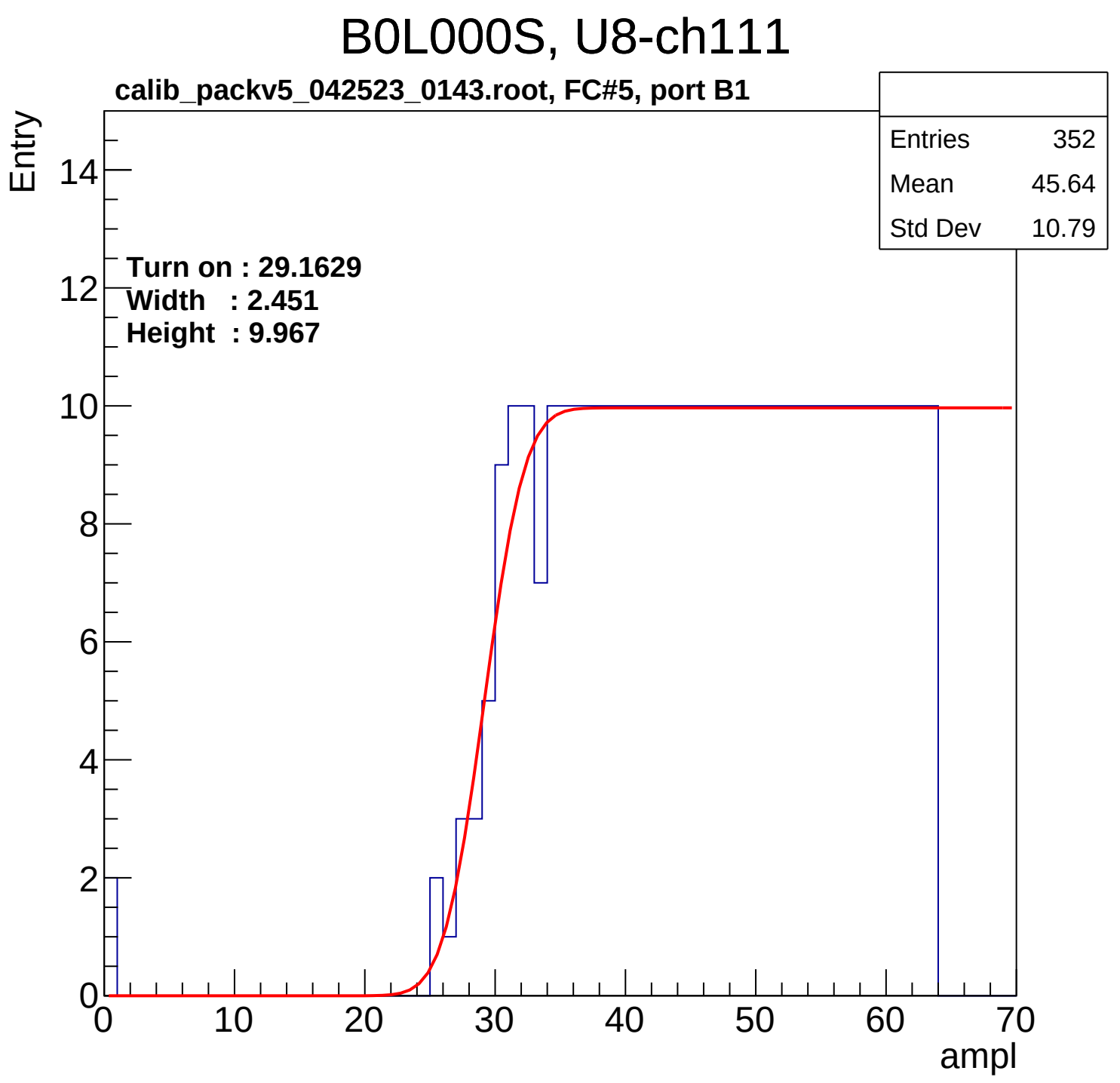
B0L000S, U8-ch111
calib_packv5_042523_0143.root, FC#5, port B1
Entries 352
Mean 45.64
Std Dev 10.79
Turn on : 29.1629
Width : 2.451
Height : 9.967
Entry
ampl
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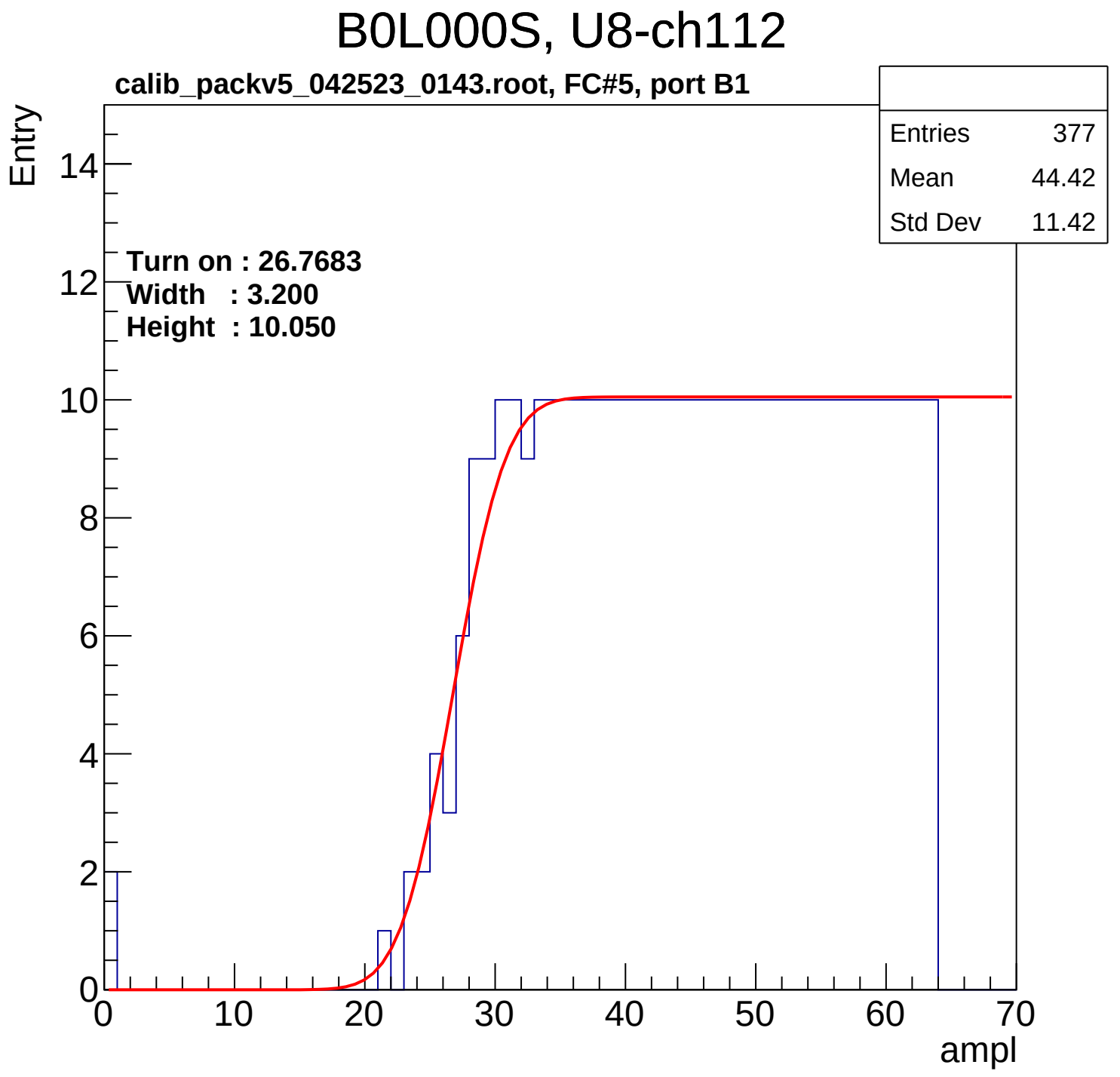
B0L000S, U8-ch112
calib_packv5_042523_0143.root, FC#5, port B1
Entries 377
Mean 44.42
Std Dev 11.42
Turn on : 26.7683
Width : 3.200
Height : 10.050
Entry
ampl
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6
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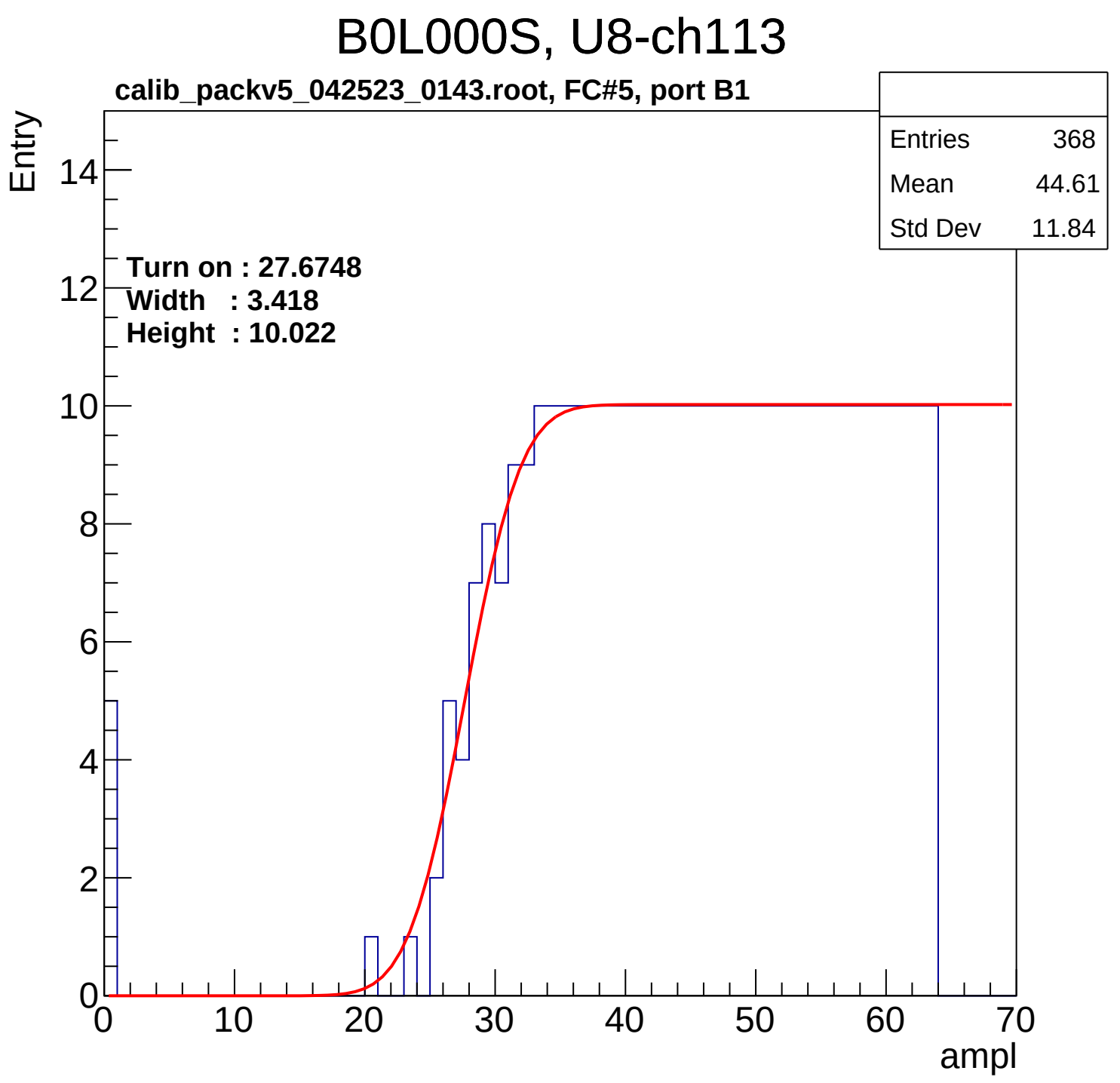
B0L000S, U8-ch113
calib_packv5_042523_0143.root, FC#5, port B1
Entries 368
Mean 44.61
Std Dev 11.84
Turn on : 27.6748
Width : 3.418
Height : 10.022
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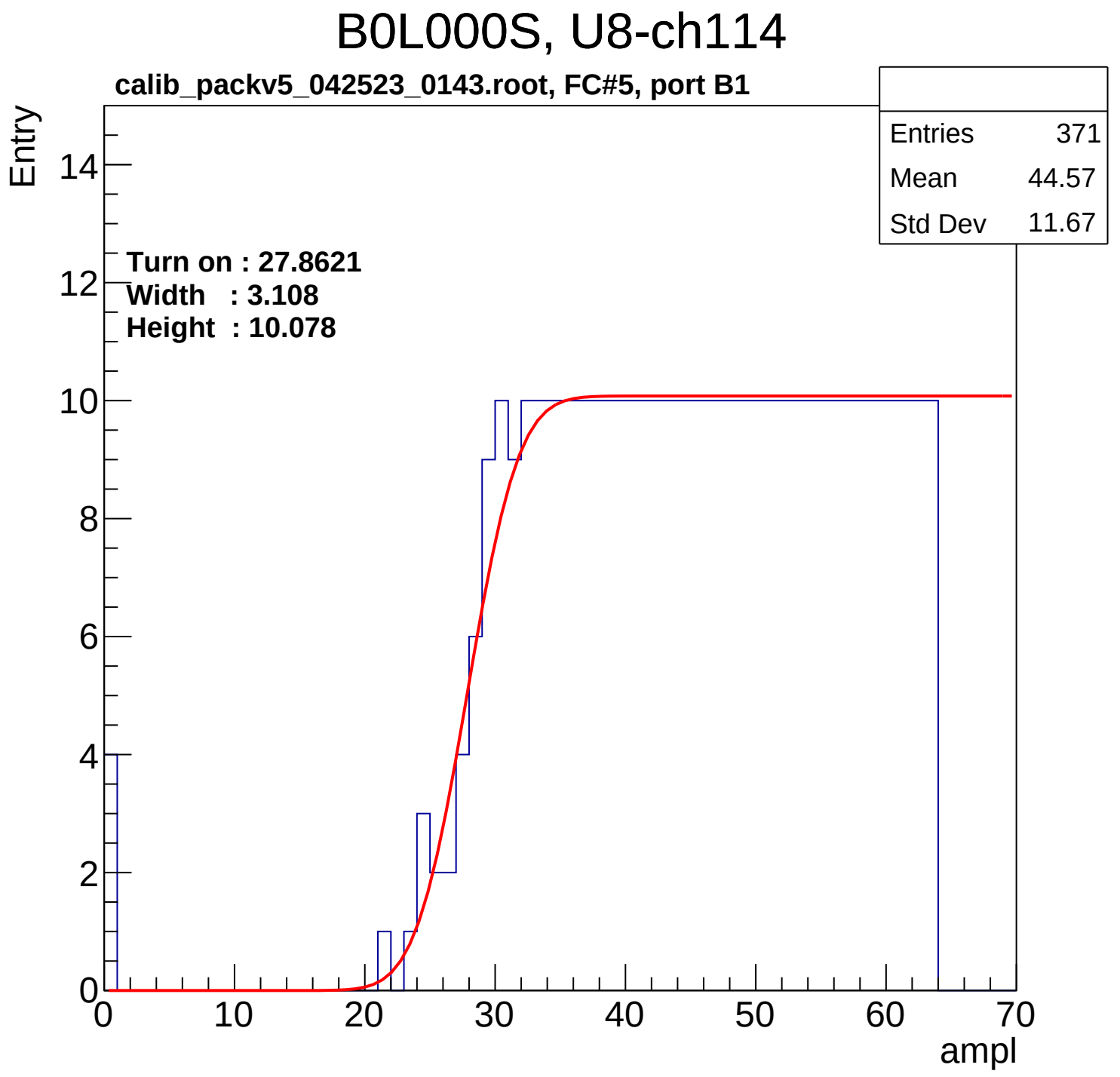
B0L000S, U8-ch114
calib_packv5_042523_0143.root, FC#5, port B1
Entries 371
Mean 44.57
Std Dev 11.67
Turn on : 27.8621
Width : 3.108
Height : 10.078
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ampl
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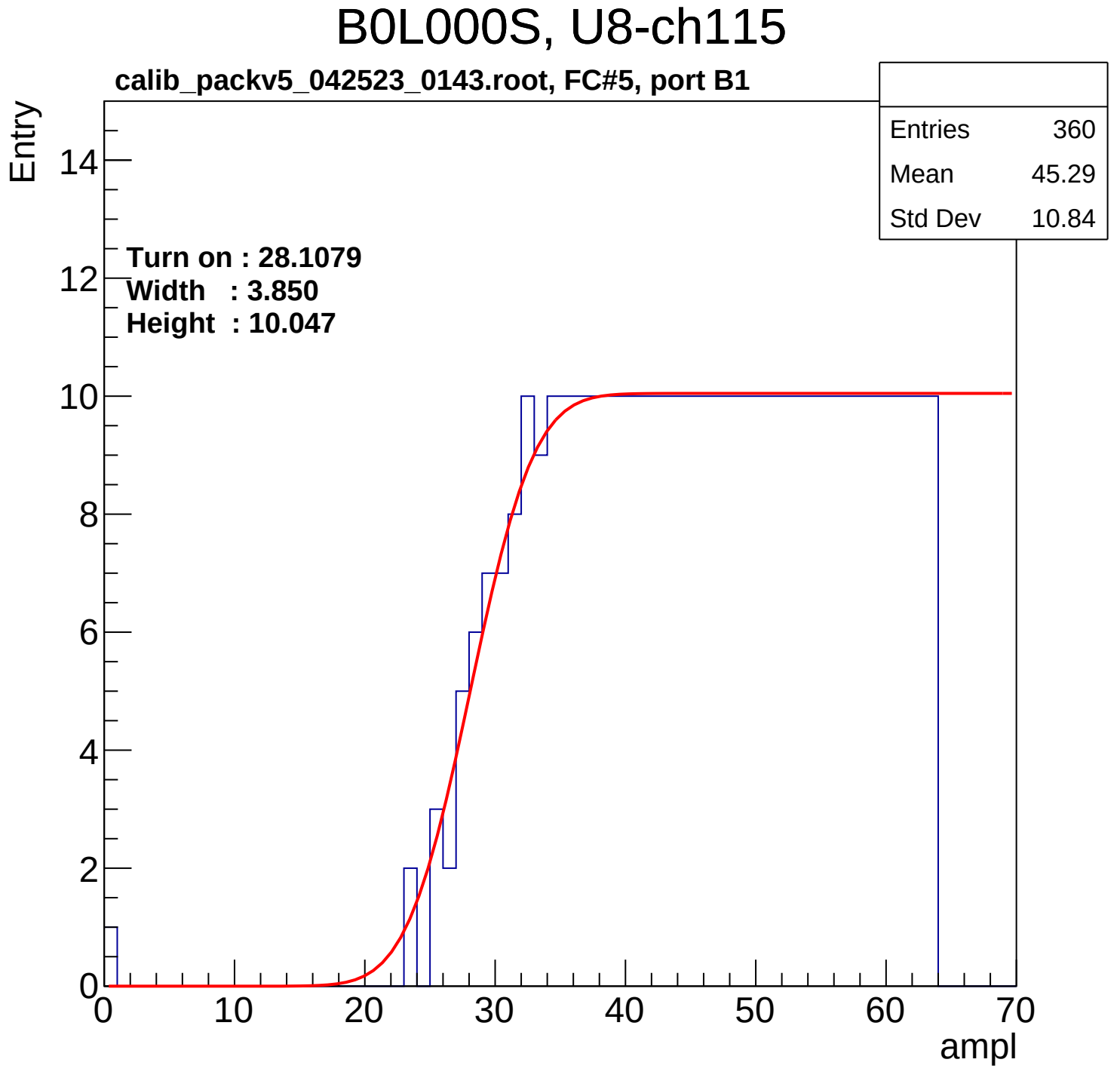
B0L000S, U8-ch115
calib_packv5_042523_0143.root, FC#5, port B1
Entries 360
Mean 45.29
Std Dev 10.84
Turn on : 28.1079
Width : 3.850
Height : 10.047
Entry
ampl
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4
6
8
10
12
14
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10
20
30
40
50
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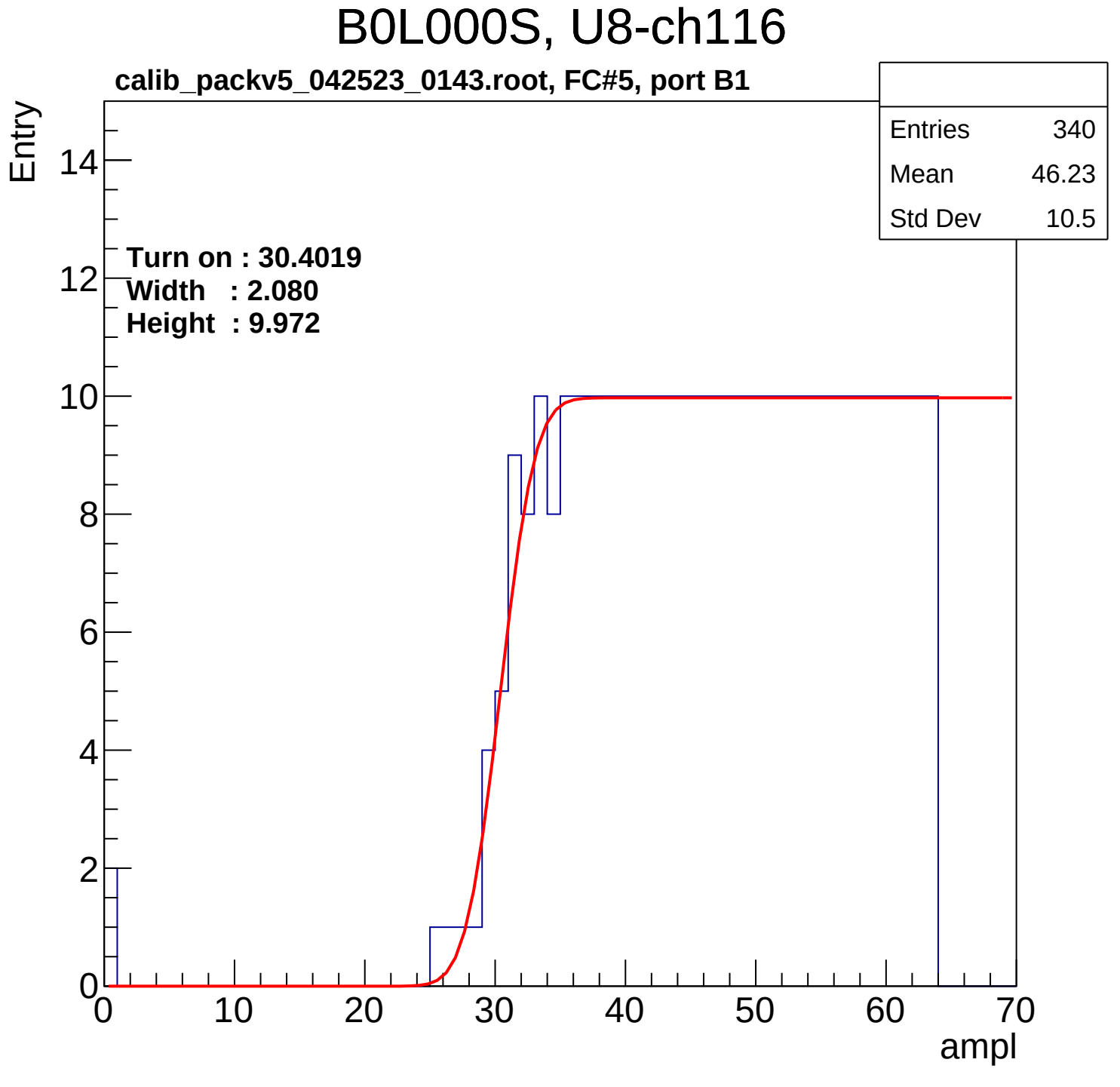
B0L000S, U8-ch116
calib_packv5_042523_0143.root, FC#5, port B1
Entries 340
Mean 46.23
Std Dev 10.5
Turn on : 30.4019
Width : 2.080
Height : 9.972
Entry
ampl
0
2
4
6
8
10
12
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0
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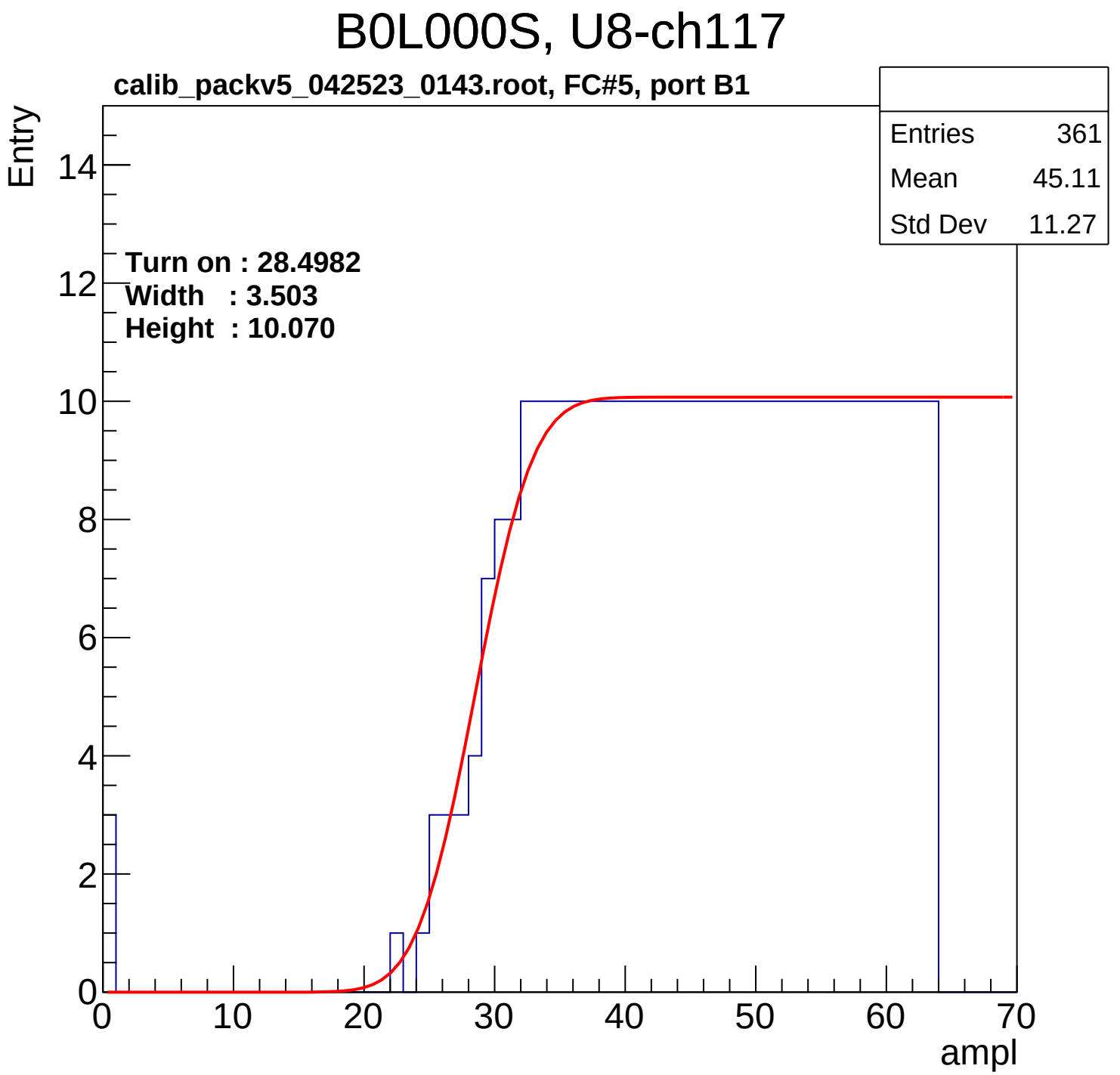
B0L000S, U8-ch117
calib_packv5_042523_0143.root, FC#5, port B1
Entries 361
Mean 45.11
Std Dev 11.27
Turn on : 28.4982
Width : 3.503
Height : 10.070
Entry
ampl
0
2
4
6
8
10
12
14
0
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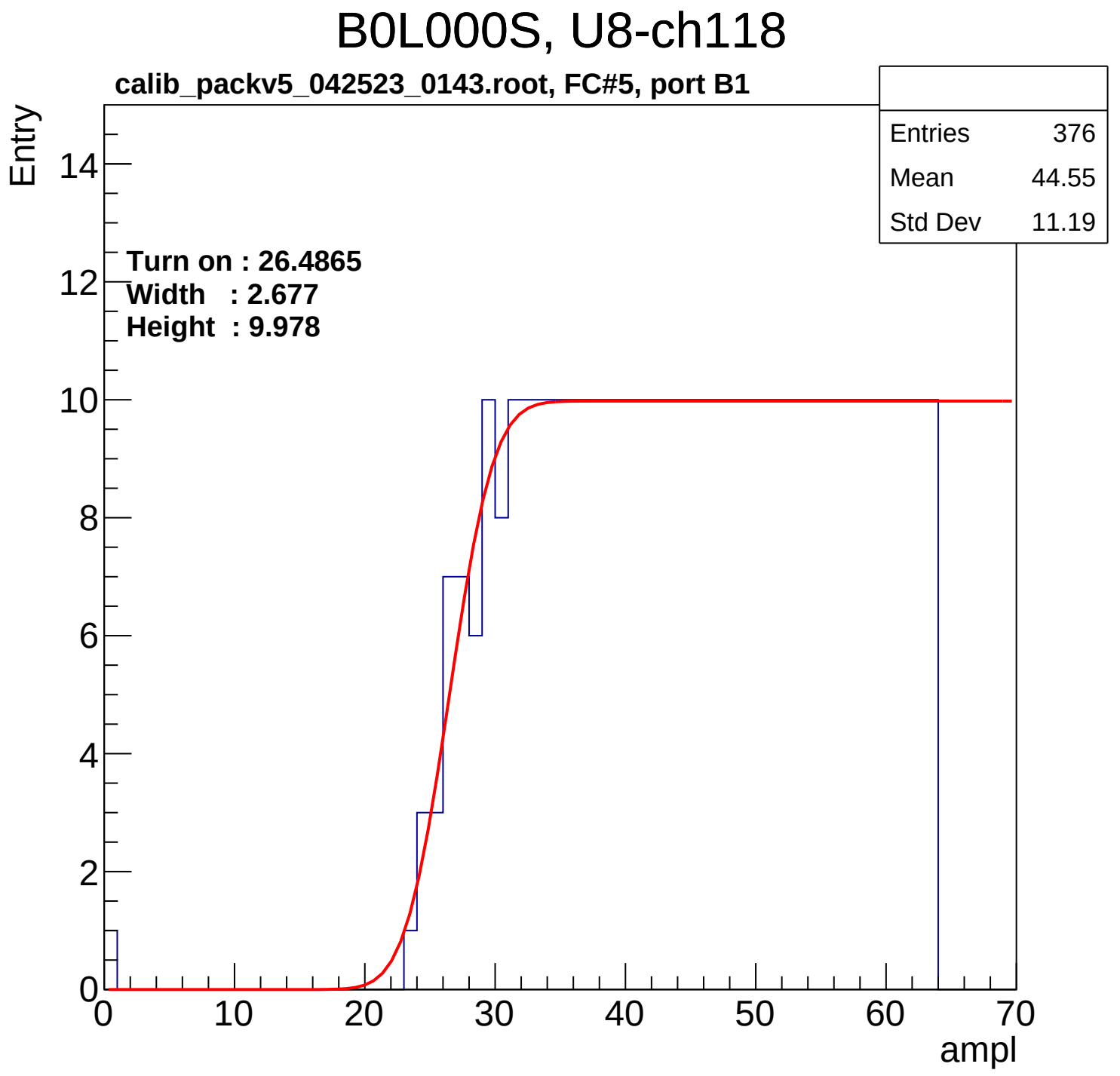
B0L000S, U8-ch118
calib_packv5_042523_0143.root, FC#5, port B1
Entries 376
Mean 44.55
Std Dev 11.19
Turn on : 26.4865
Width : 2.677
Height : 9.978
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
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60
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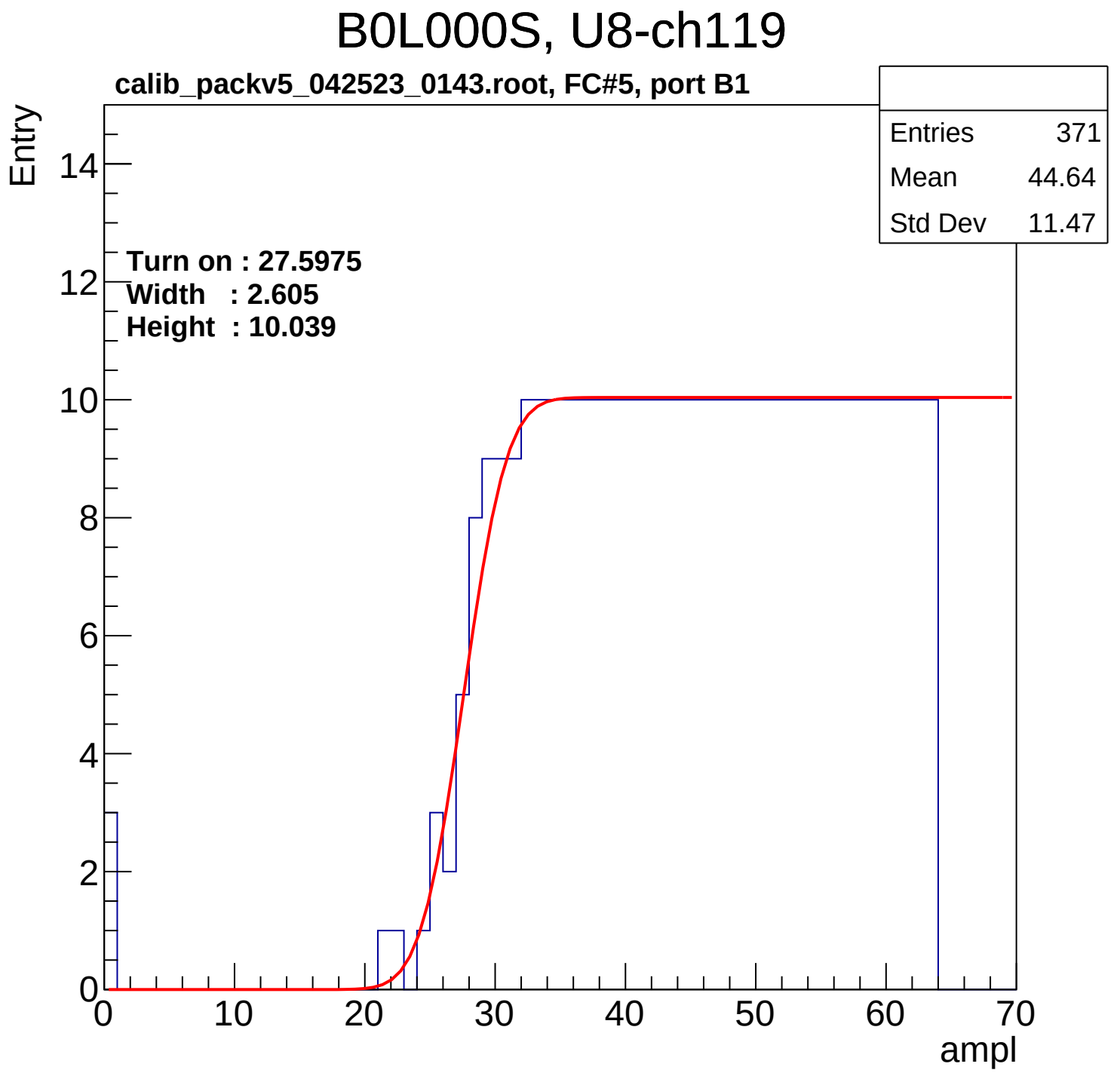
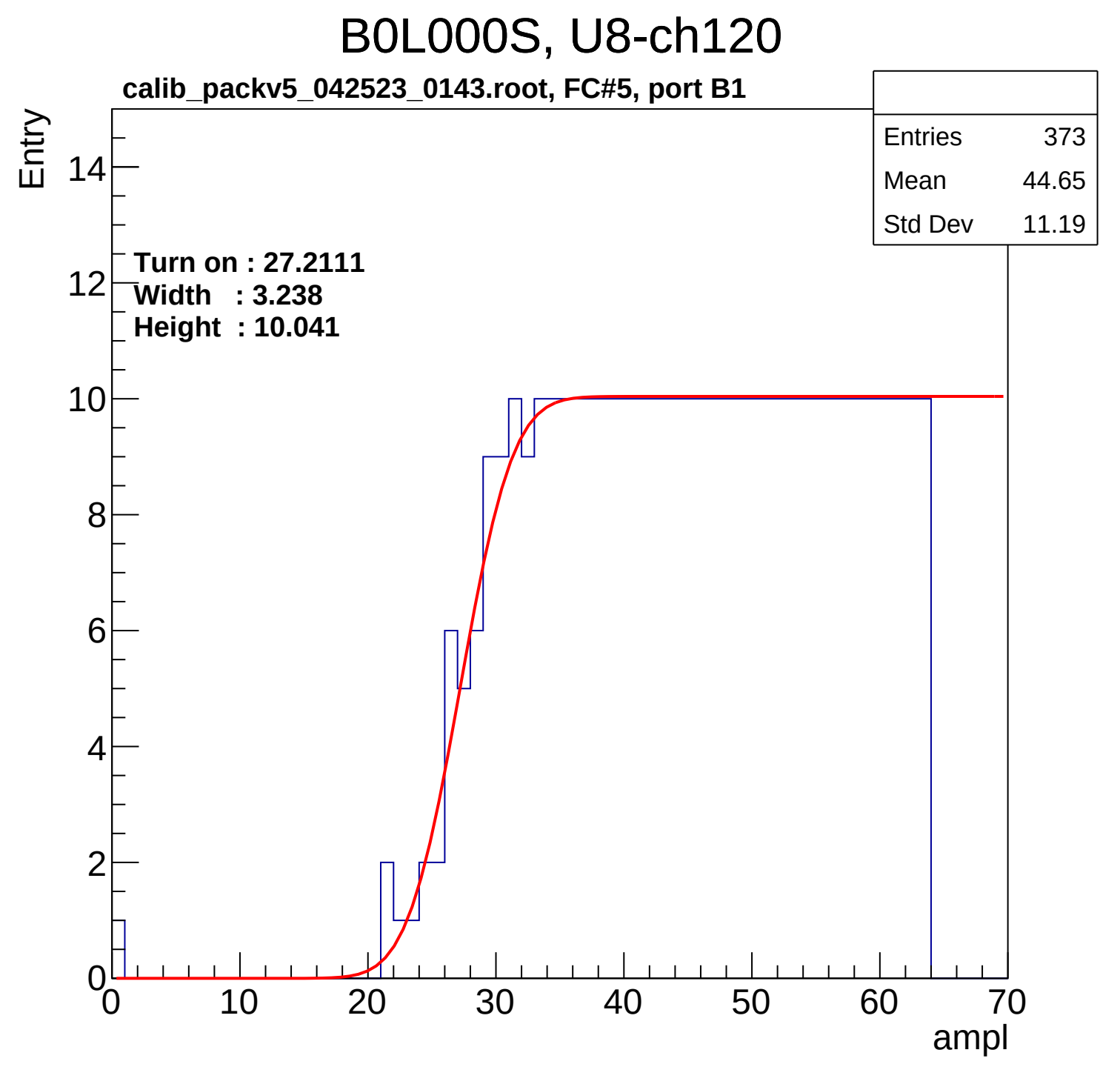
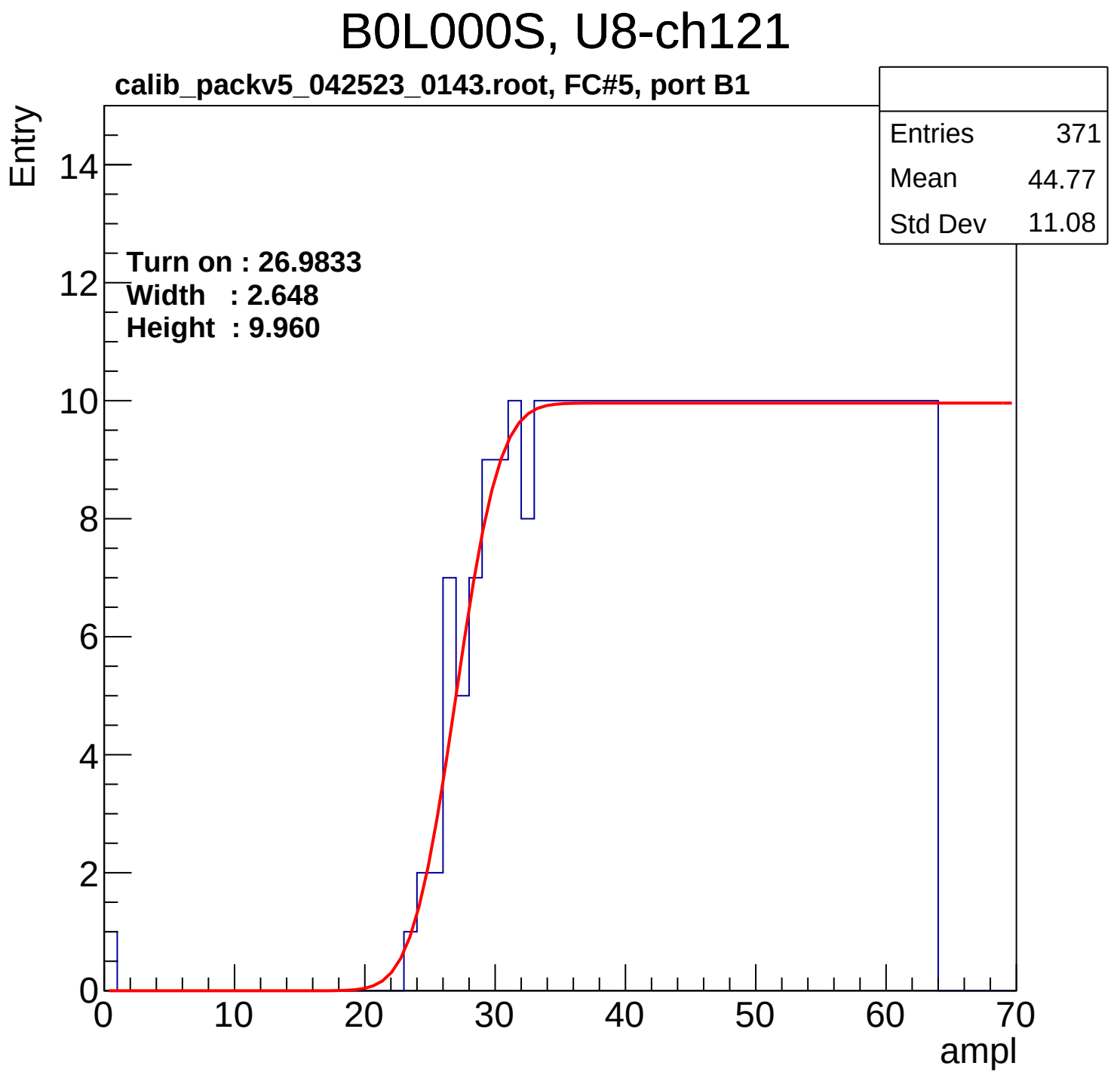

B0L000S, U8-ch119
calib_packv5_042523_0143.root, FC#5, port B1
Entries 371
Mean 44.64
Std Dev 11.47
Turn on : 27.5975
Width : 2.605
Height : 10.039
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L000S, U8-ch120
calib_packv5_042523_0143.root, FC#5, port B1
Entries 373
Mean 44.65
Std Dev 11.19
Turn on : 27.2111
Width : 3.238
Height : 10.041
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L000S, U8-ch121
calib_packv5_042523_0143.root, FC#5, port B1
Entries 371
Mean 44.77
Std Dev 11.08
Turn on : 26.9833
Width : 2.648
Height : 9.960
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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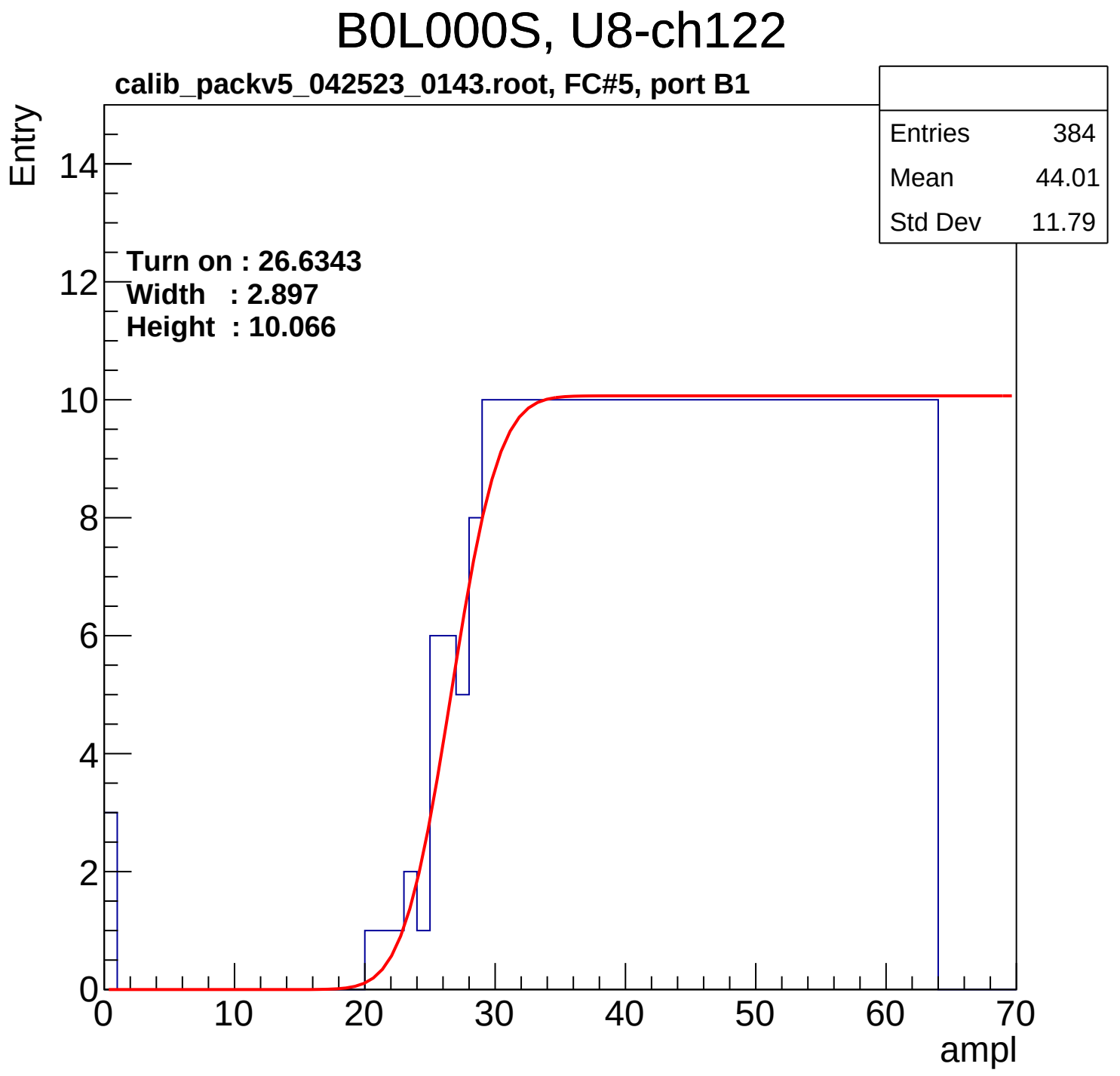
B0L000S, U8-ch122
calib_packv5_042523_0143.root, FC#5, port B1
Entries 384
Mean 44.01
Std Dev 11.79
Turn on : 26.6343
Width : 2.897
Height : 10.066
Entry
ampl
0
2
4
6
8
10
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10
20
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40
50
60
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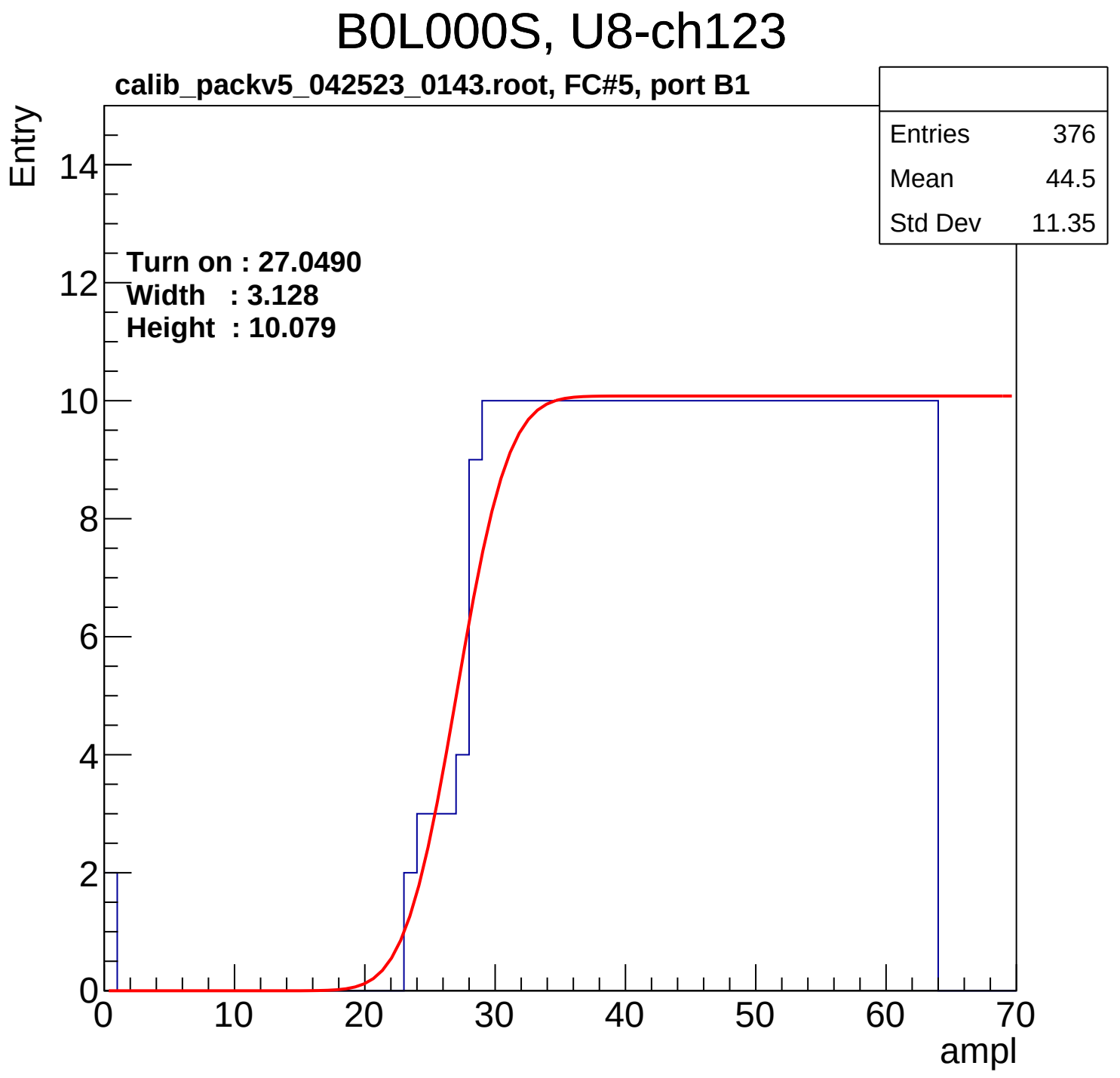
B0L000S, U8-ch123
calib_packv5_042523_0143.root, FC#5, port B1
Entries 376
Mean 44.5
Std Dev 11.35
Turn on : 27.0490
Width : 3.128
Height : 10.079
Entry
ampl
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2
4
6
8
10
12
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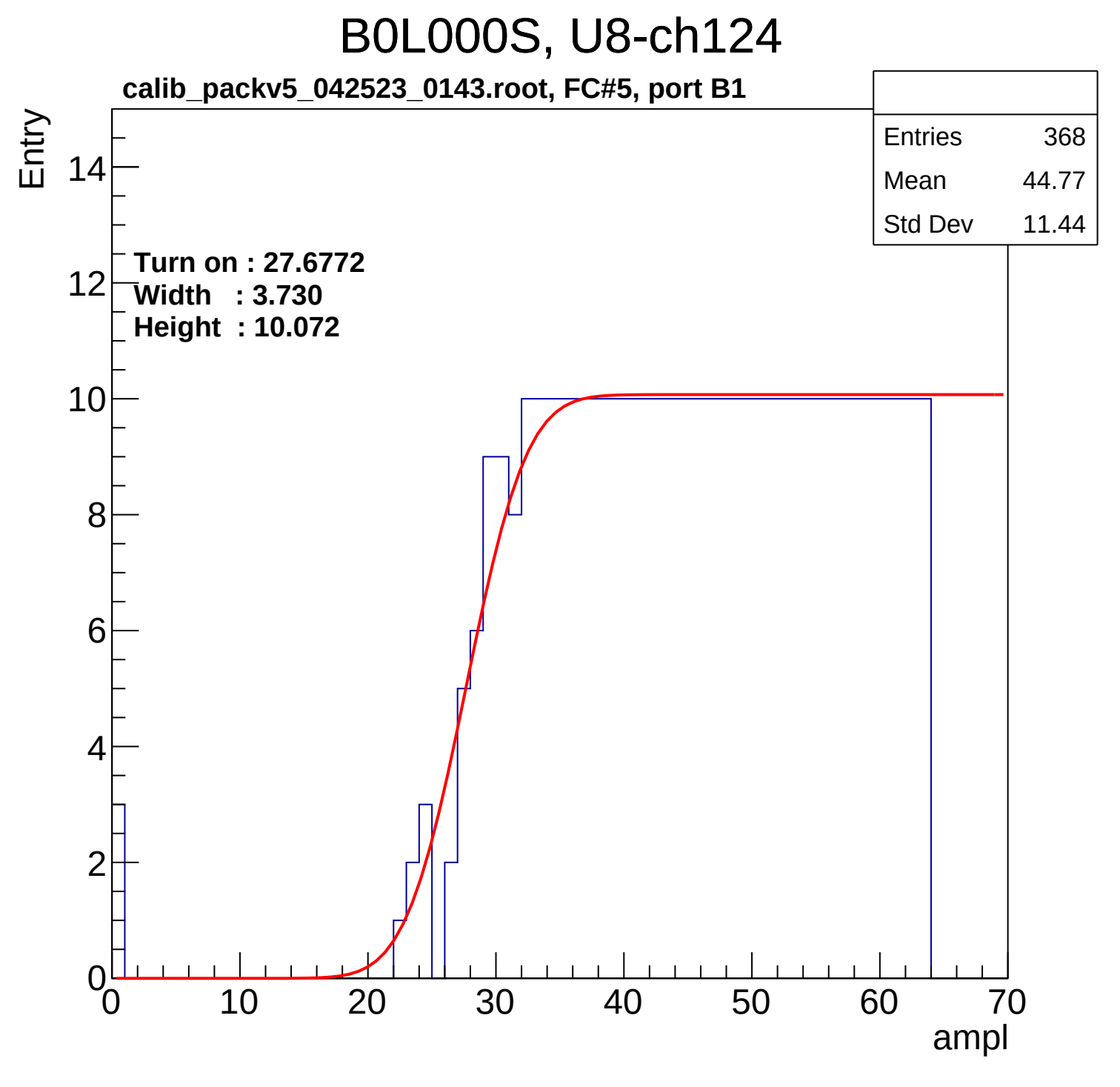
0
10
20
30
40
50
60
70


B0L000S, U8-ch124
calib_packv5_042523_0143.root, FC#5, port B1
Entries 368
Mean 44.77
Std Dev 11.44
Turn on : 27.6772
Width : 3.730
Height : 10.072
Entry
ampl
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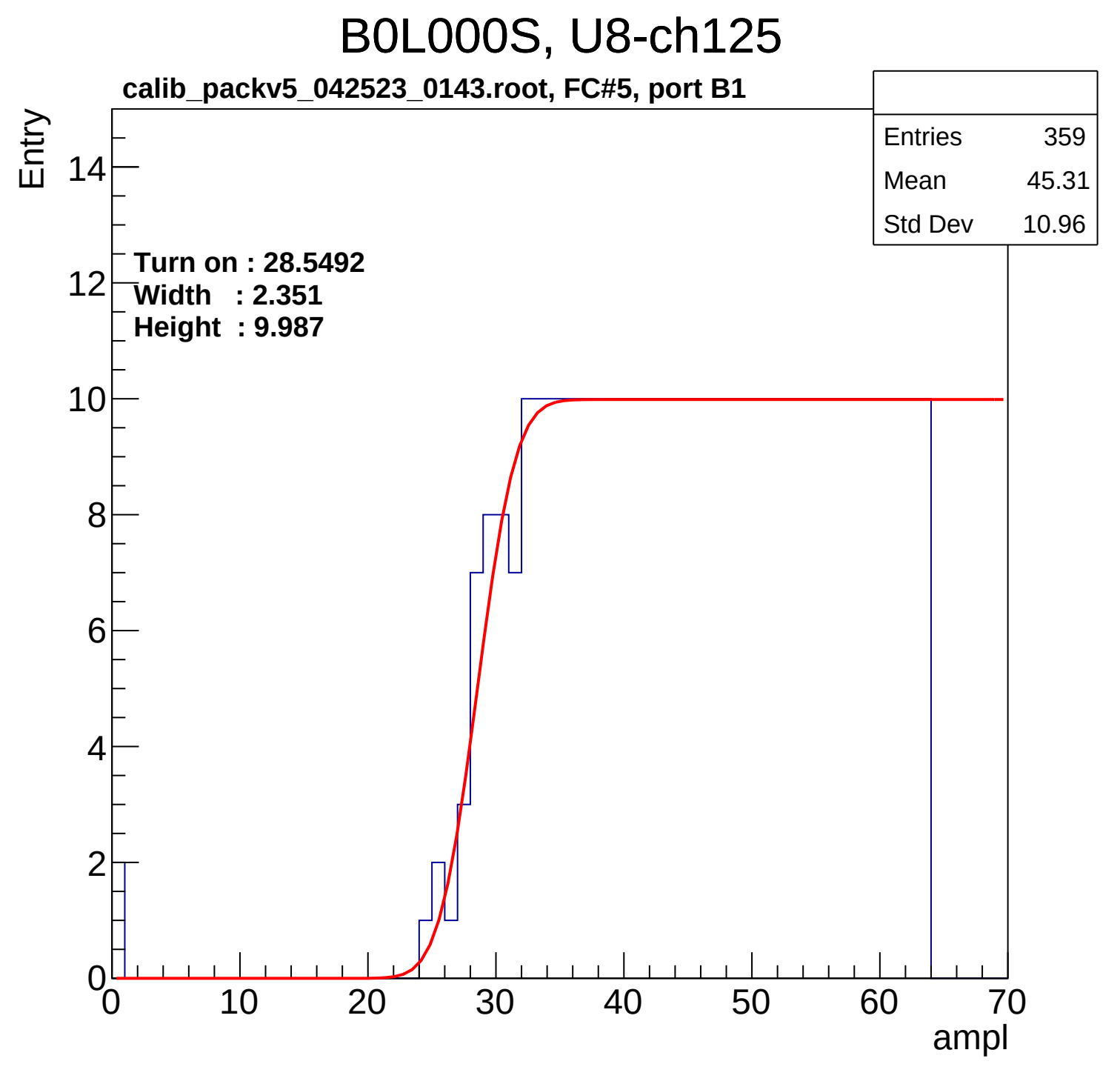
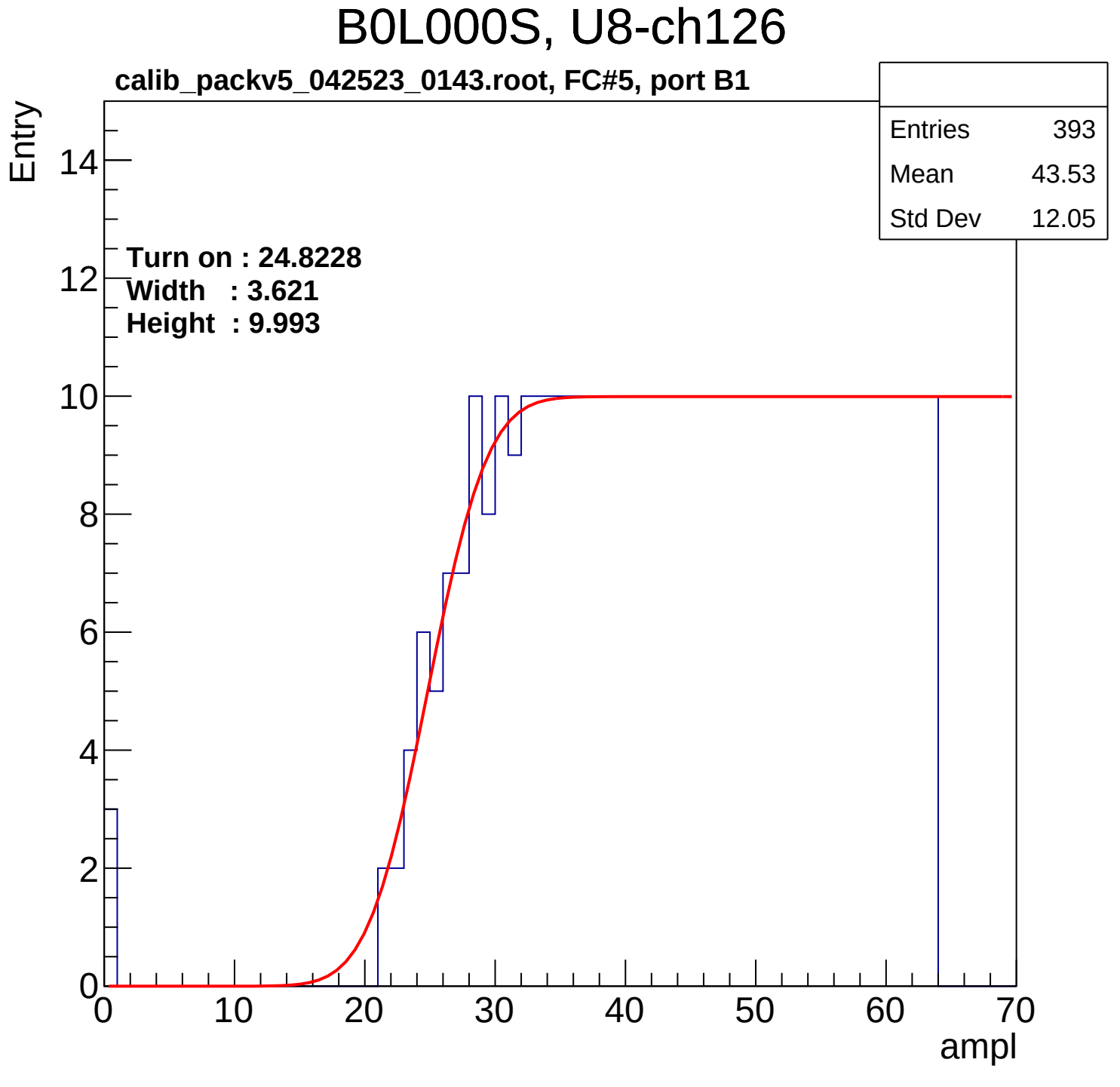
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L000S, U8-ch125
calib_packv5_042523_0143.root, FC#5, port B1
Entries 359
Mean 45.31
Std Dev 10.96
Turn on : 28.5492
Width : 2.351
Height : 9.987
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L000S, U8-ch126
calib_packv5_042523_0143.root, FC#5, port B1
Entries 393
Mean 43.53
Std Dev 12.05
Turn on : 24.8228
Width : 3.621
Height : 9.993
Entry
ampl
0
2
4
6
8
10
12
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0
10
20
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40
50
60
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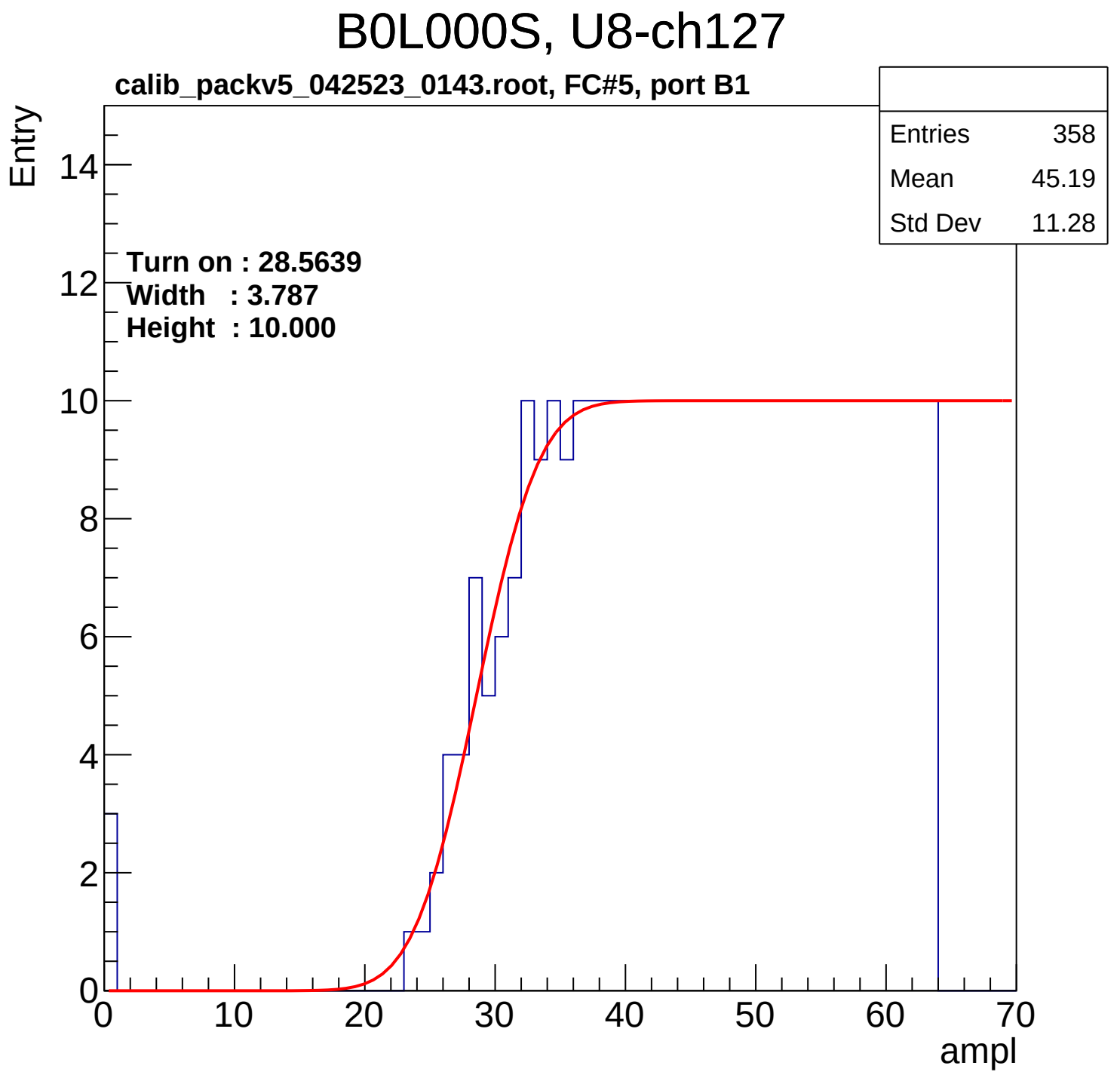
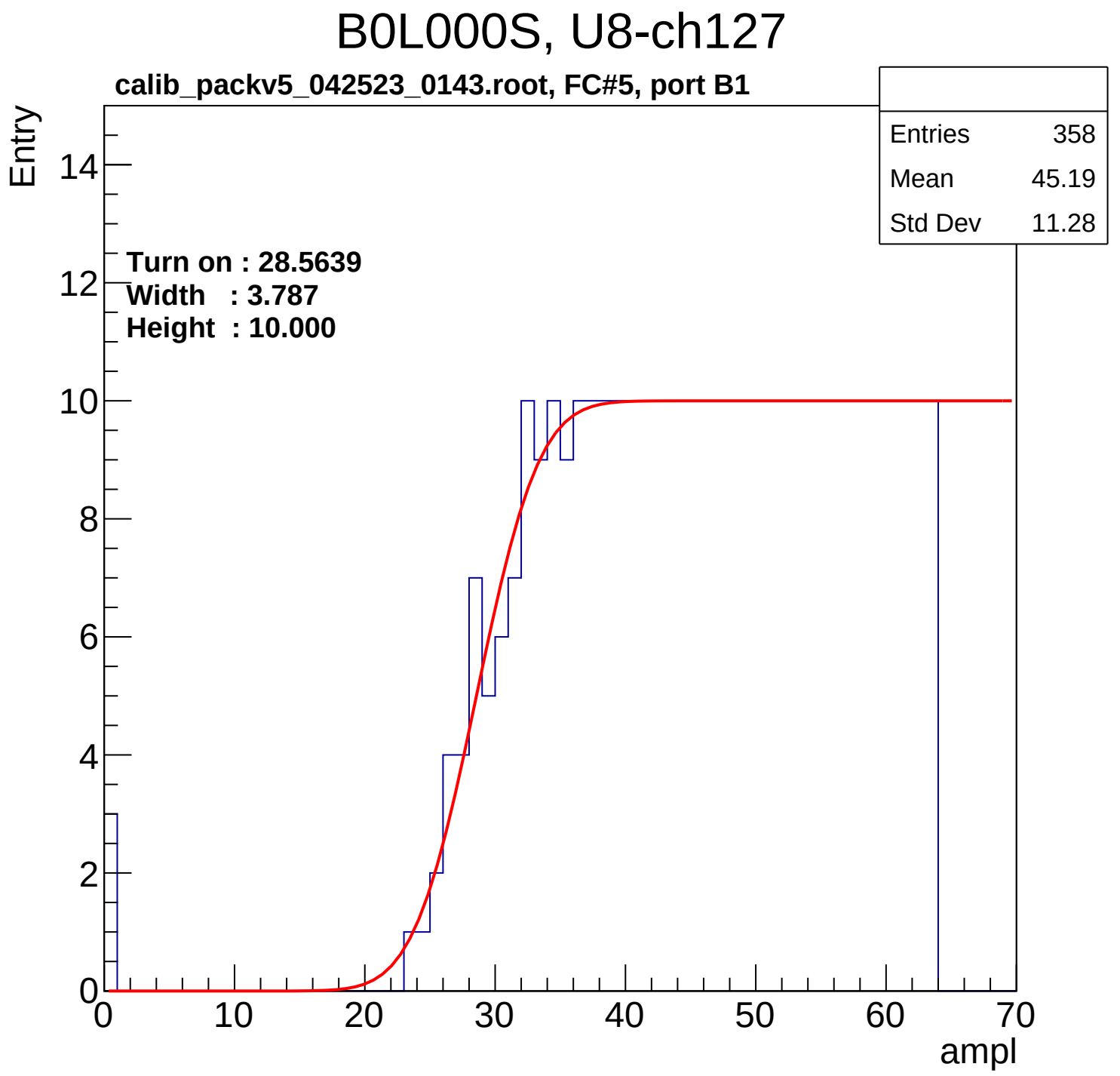

B0L000S, U8-ch127
calib_packv5_042523_0143.root, FC#5, port B1
Entries 358
Mean 45.19
Std Dev 11.28
Turn on : 28.5639
Width : 3.787
Height : 10.000
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L000S, U8-ch127
calib_packv5_042523_0143.root, FC#5, port B1
Entries 358
Mean 45.19
Std Dev 11.28
Turn on : 28.5639
Width : 3.787
Height : 10.000
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70