



# B0L002S, U2-ch0, adc0

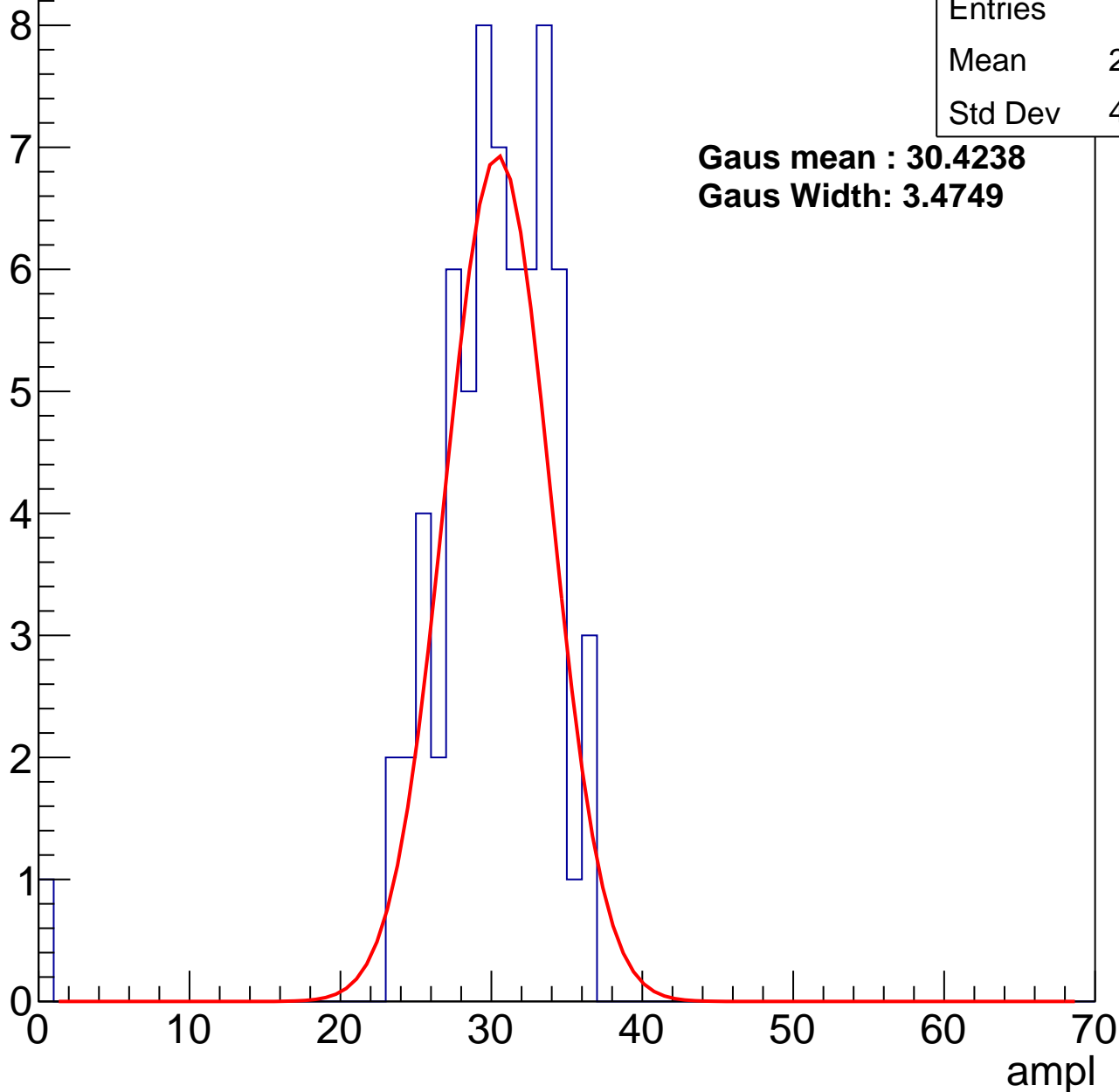
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	67
Mean	29.54
Std Dev	4.888

**Gaus mean : 30.4238**

**Gaus Width: 3.4749**



# B0L002S, U2-ch0, adc1

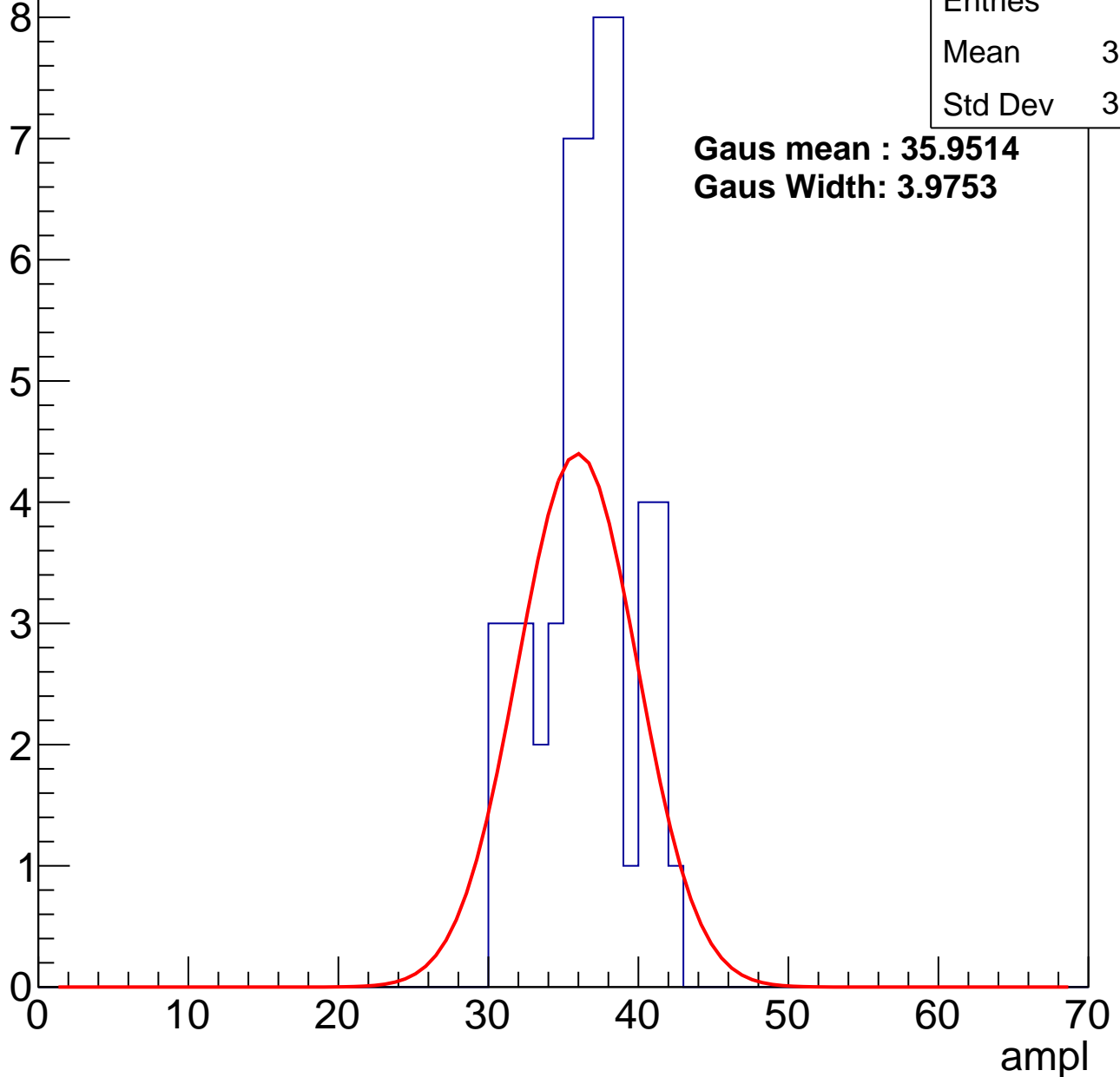
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	54
Mean	36.09
Std Dev	3.093

**Gaus mean : 35.9514**

**Gaus Width: 3.9753**



# B0L002S, U2-ch0, adc2

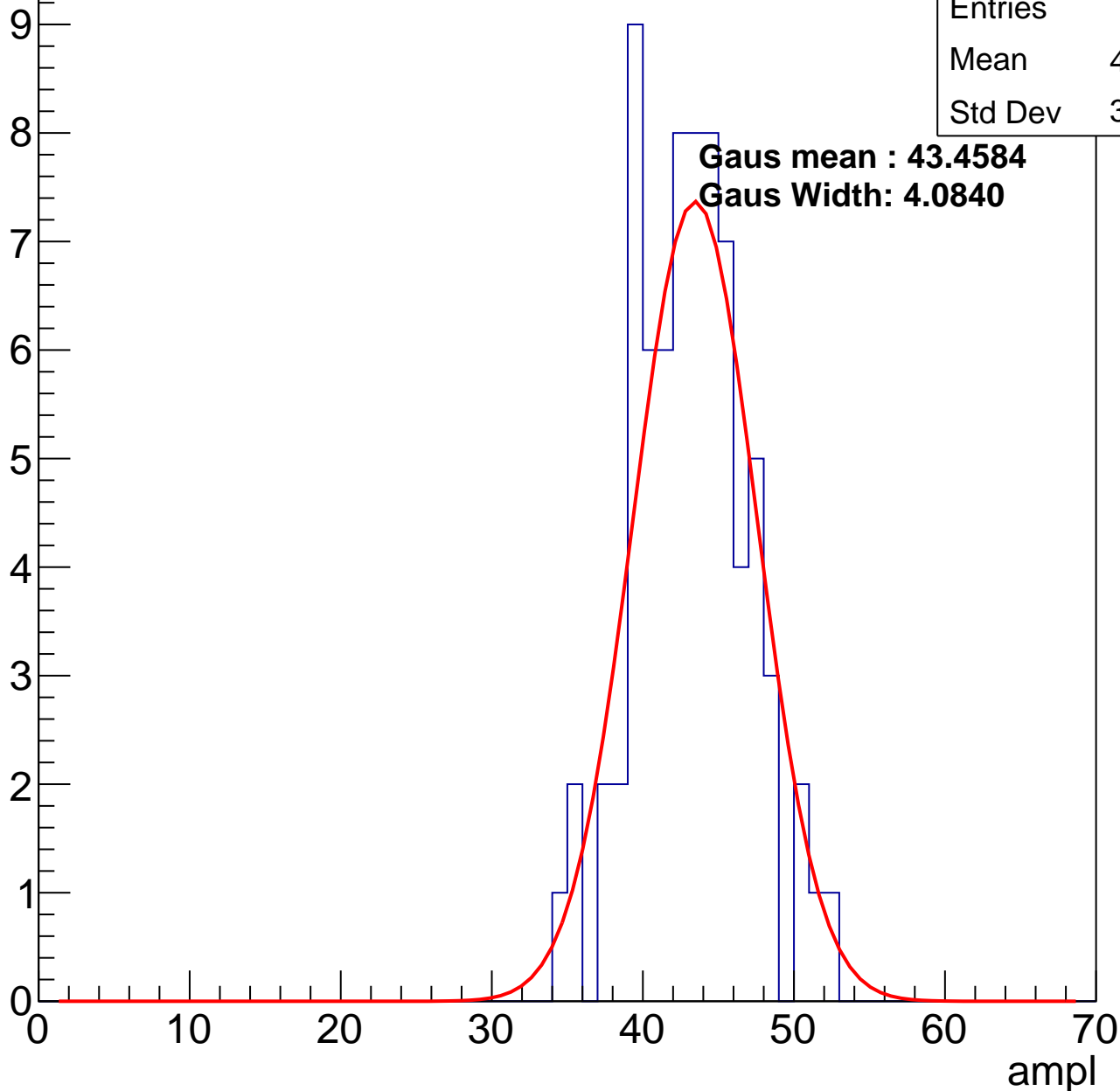
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	75
Mean	42.72
Std Dev	3.697

**Gaus mean : 43.4584**

**Gaus Width: 4.0840**



# B0L002S, U2-ch0, adc3

calib\_packv5\_042523\_0143.root, FC#8, port C1

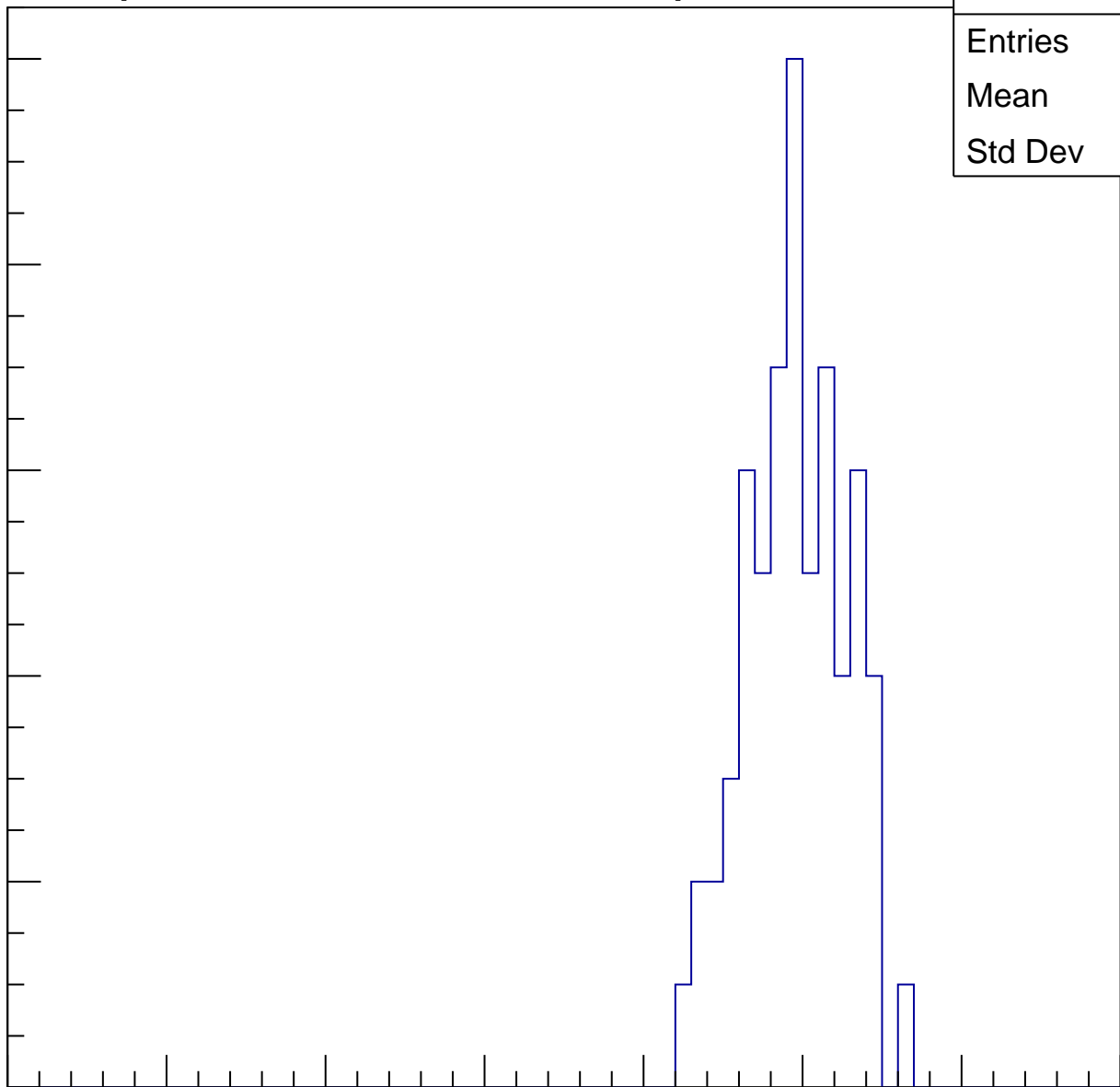
Entries	63
Mean	49.1
Std Dev	3.12

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B0L002S, U2-ch0, adc4

calib\_packv5\_042523\_0143.root, FC#8, port C1

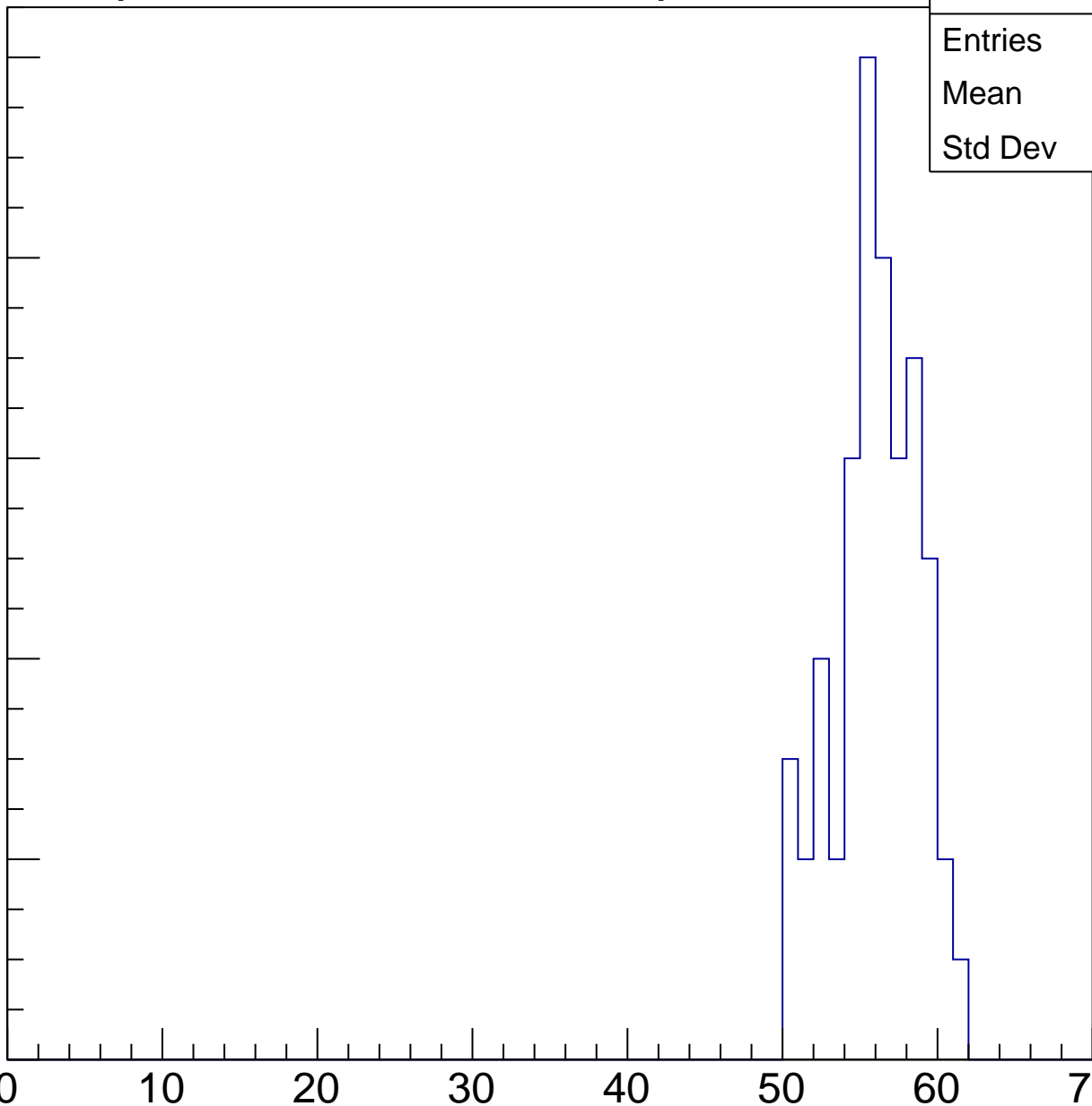
Entries	56
Mean	55.57
Std Dev	2.672

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

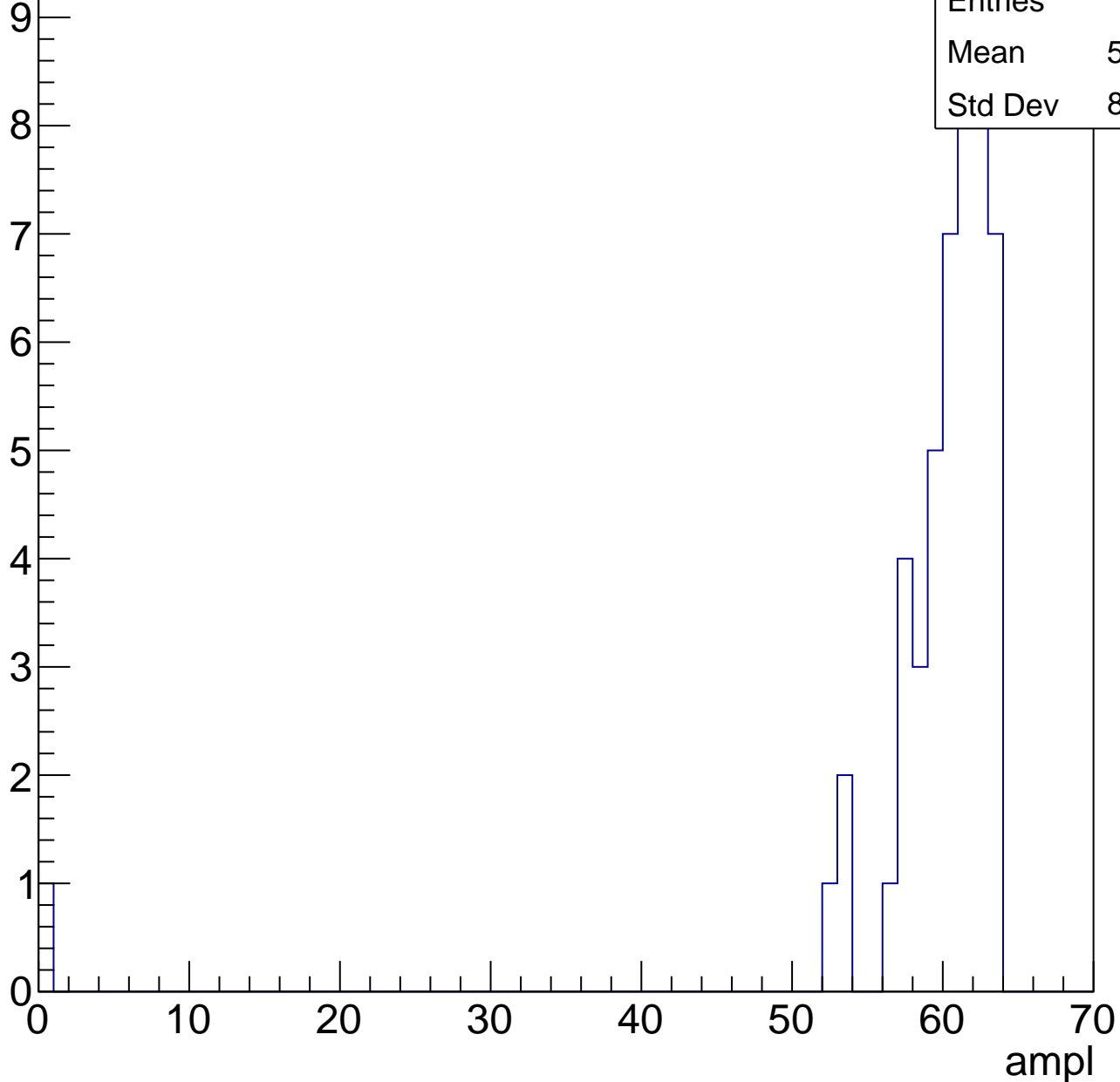


# B0L002S, U2-ch0, adc5

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	49
Mean	58.76
Std Dev	8.879



# B0L002S, U2-ch0, adc6

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

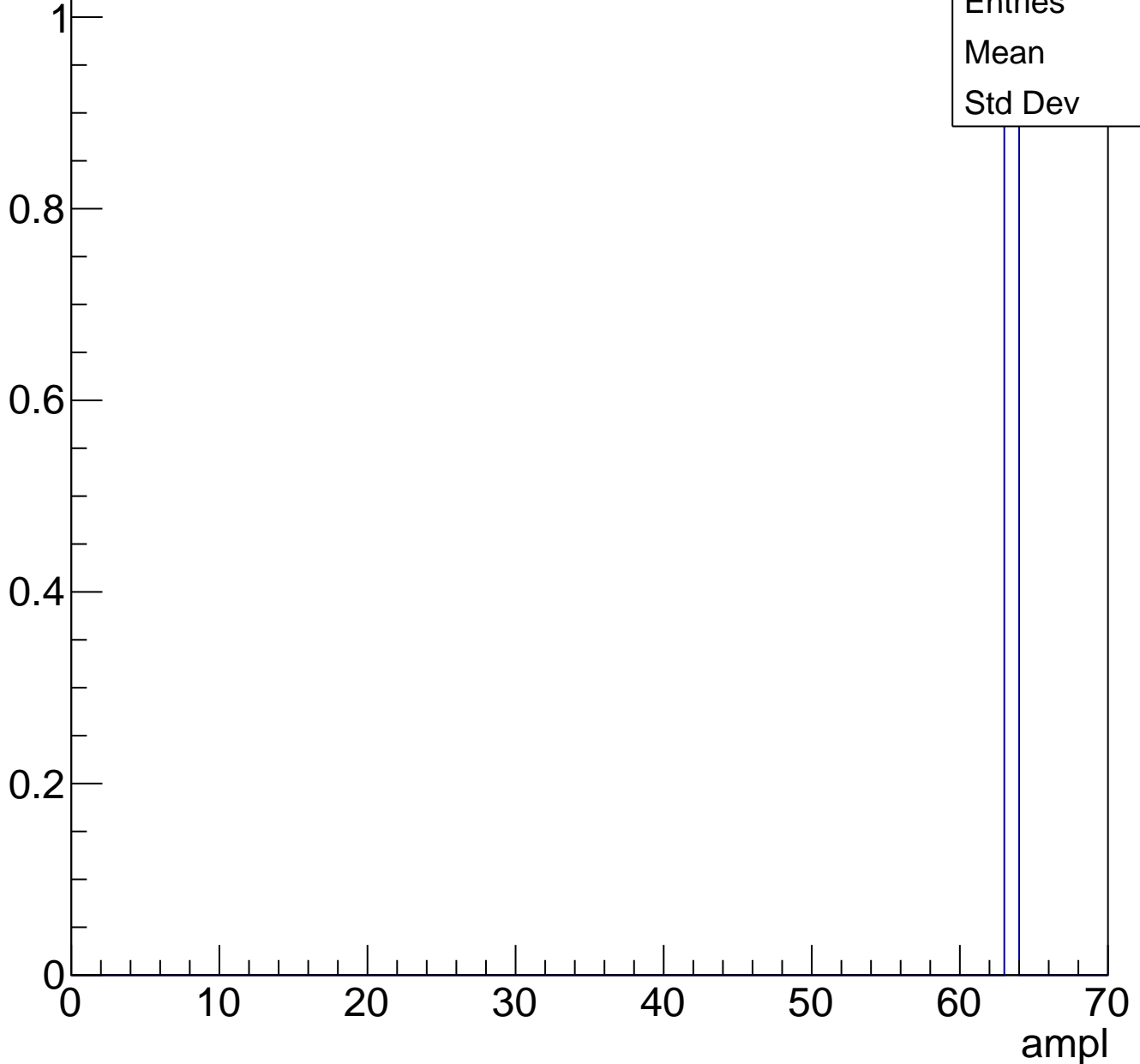




# B0L002S, U2-ch0, adc7

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



# B0L002S, U2-ch1, adc0

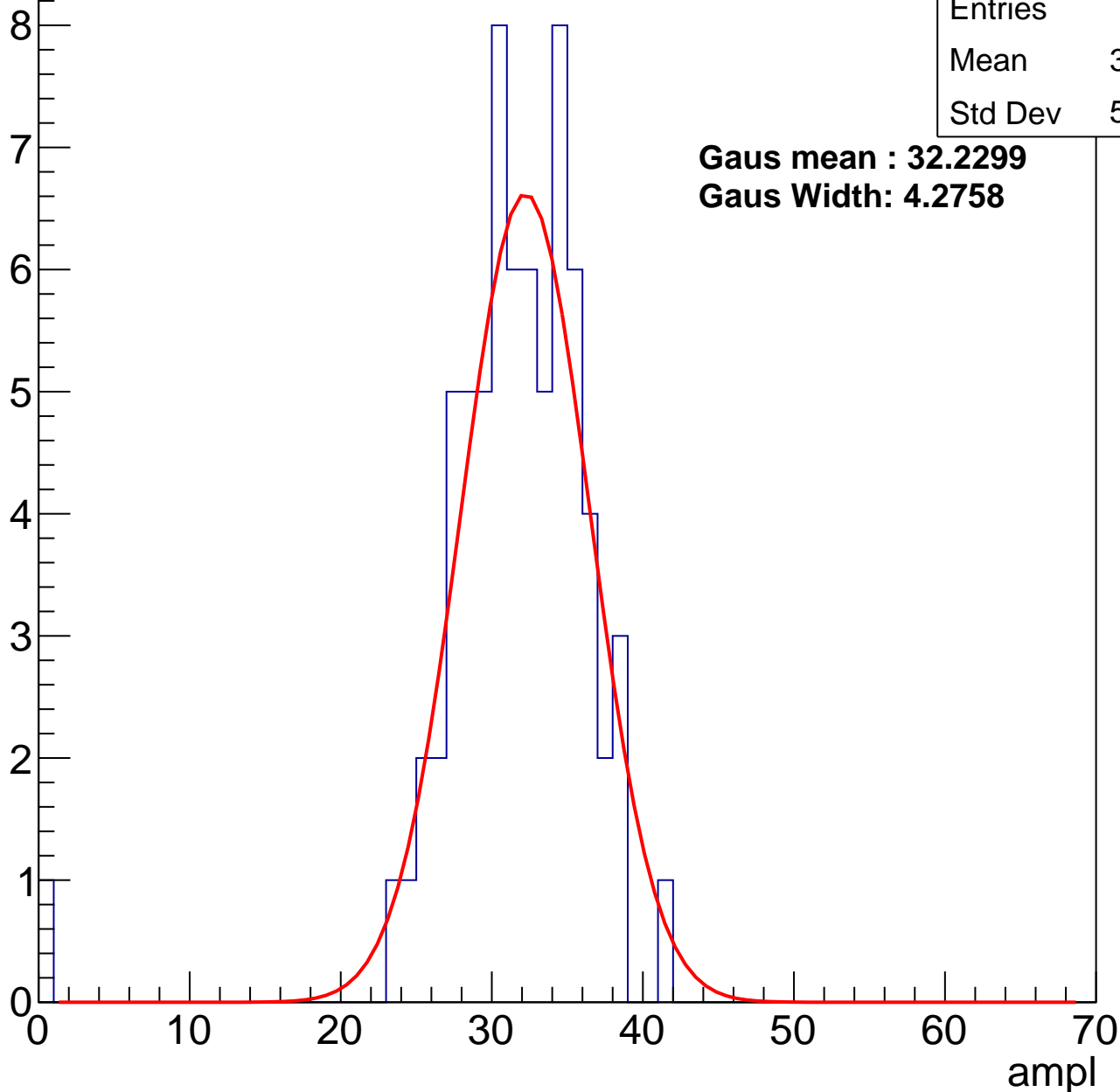
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	71
Mean	31.08
Std Dev	5.256

**Gaus mean : 32.2299**

**Gaus Width: 4.2758**



# B0L002S, U2-ch1, adc1

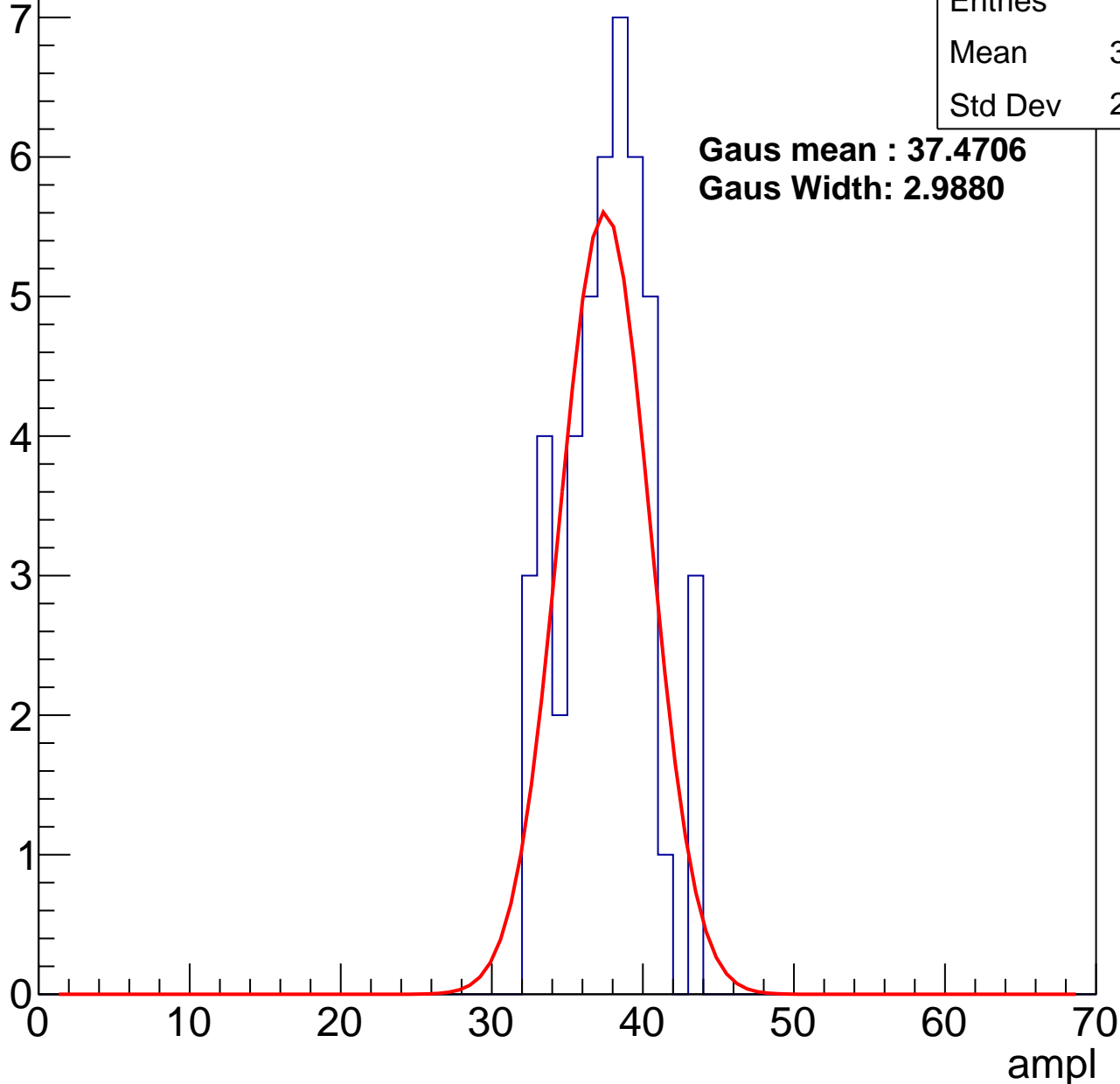
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	46
Mean	37.13
Std Dev	2.864

**Gaus mean : 37.4706**

**Gaus Width: 2.9880**



# B0L002S, U2-ch1, adc2

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	72
Mean	43.58
Std Dev	3.273

**Gaus mean : 43.7668**

**Gaus Width: 3.7095**

10

8

6

4

2

0

0

10

20

30

40

50

60

70

ampl

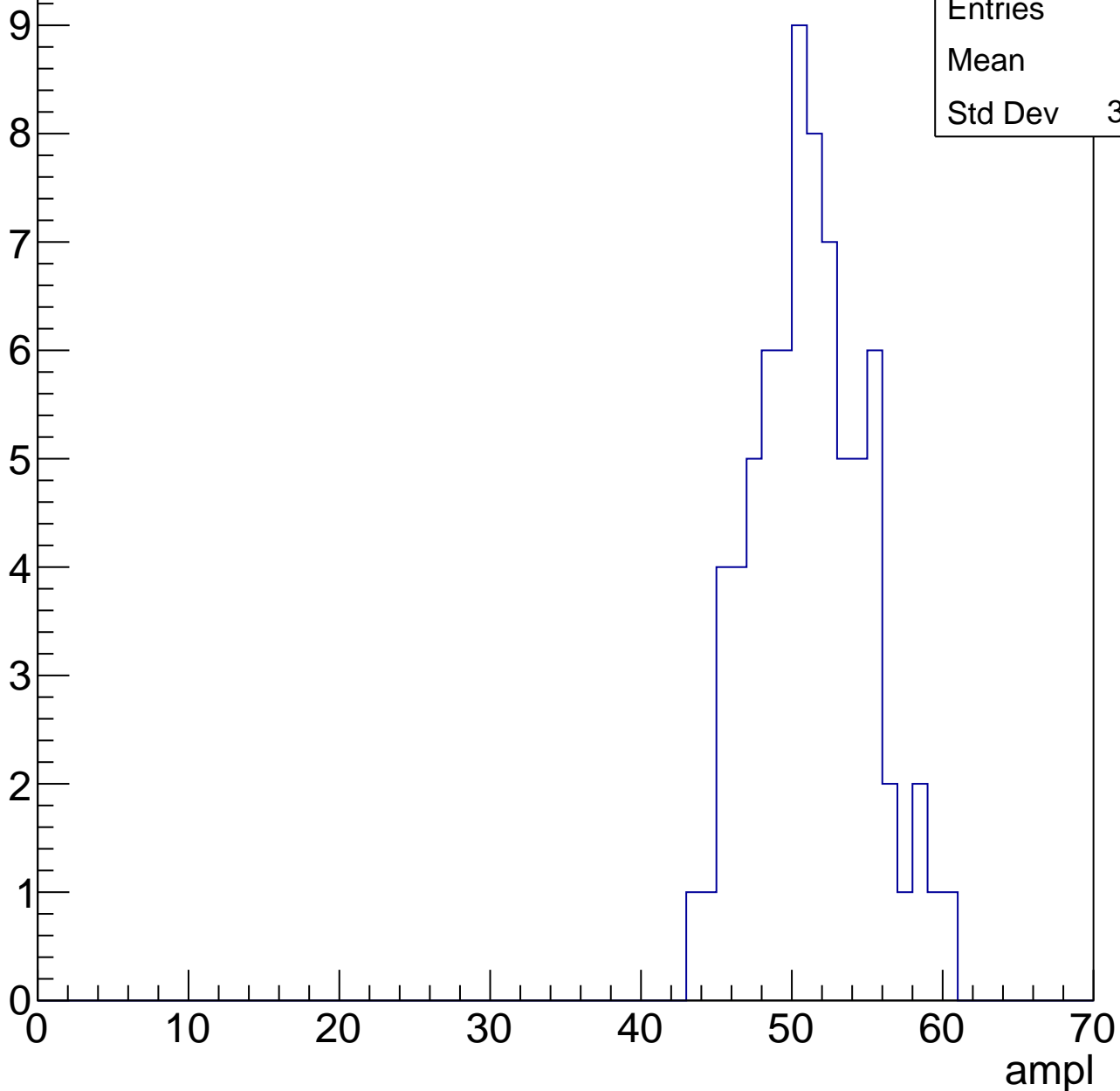


# B0L002S, U2-ch1, adc3

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

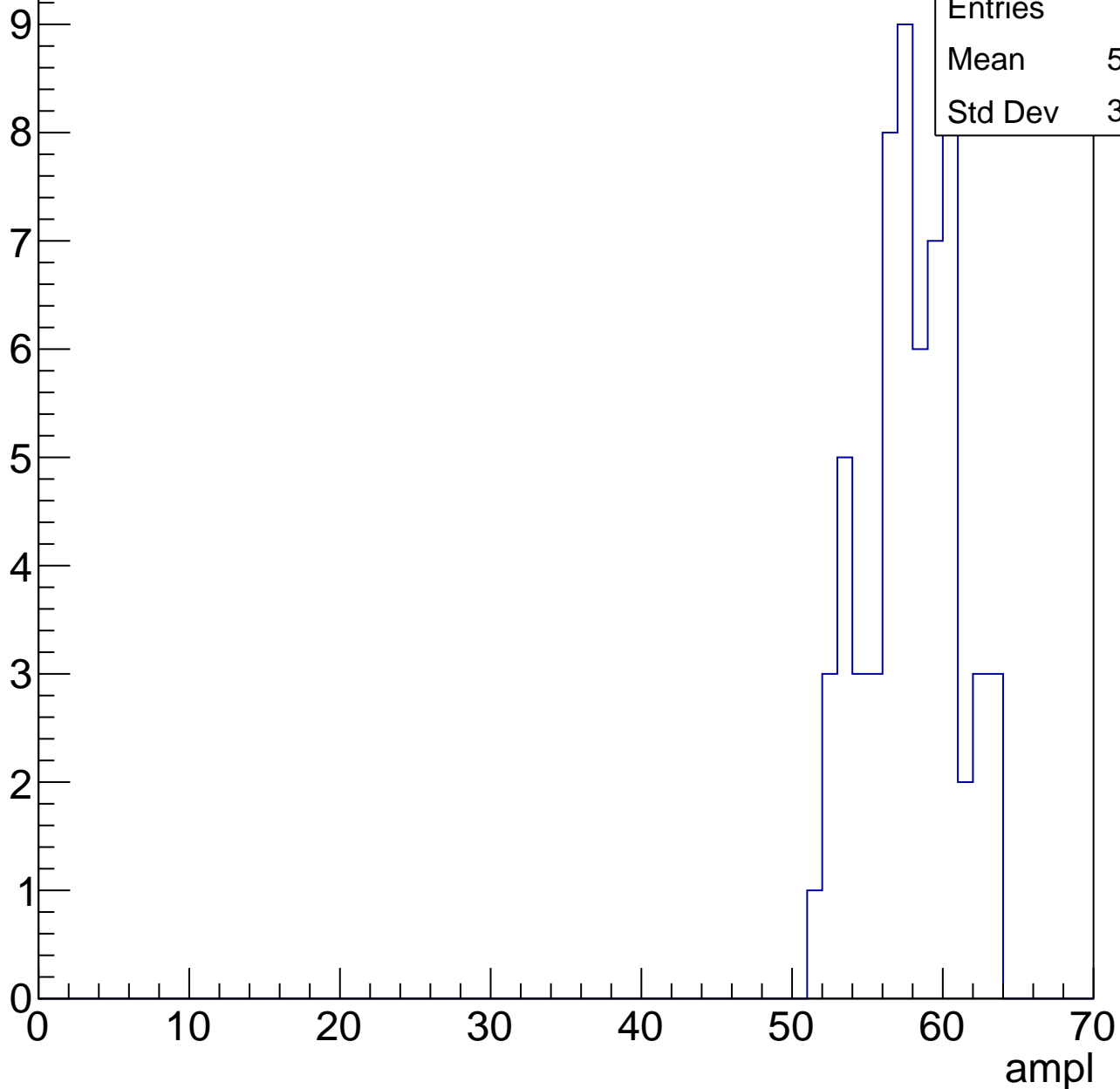
Entries	74
Mean	50.8
Std Dev	3.709



# B0L002S, U2-ch1, adc4

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



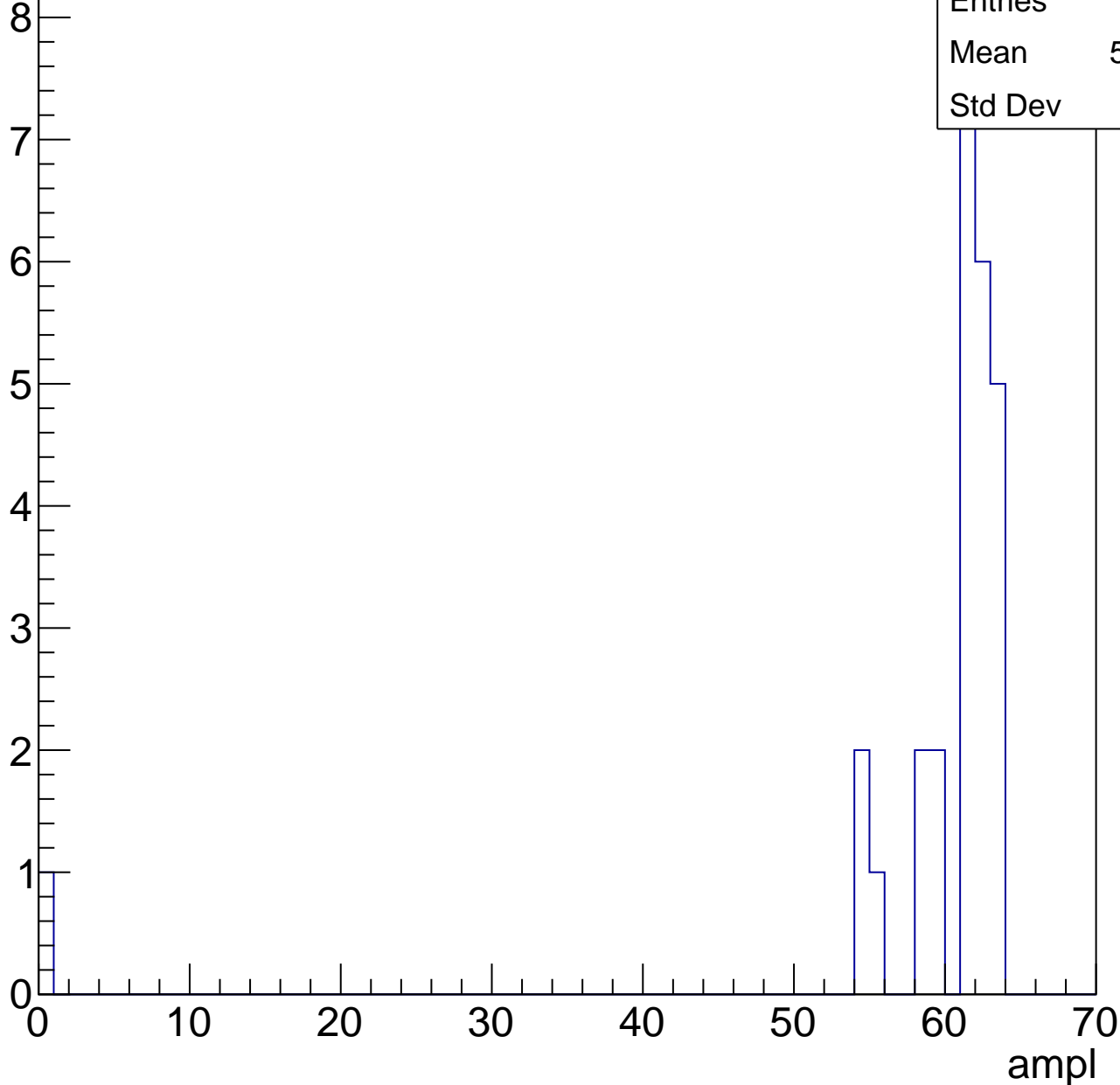
Entries	62
Mean	57.39
Std Dev	3.002

# B0L002S, U2-ch1, adc5

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	27
Mean	58.22
Std Dev	11.7



# B0L002S, U2-ch1, adc6

calib\_packv5\_042523\_0143.root, FC#8, port C1

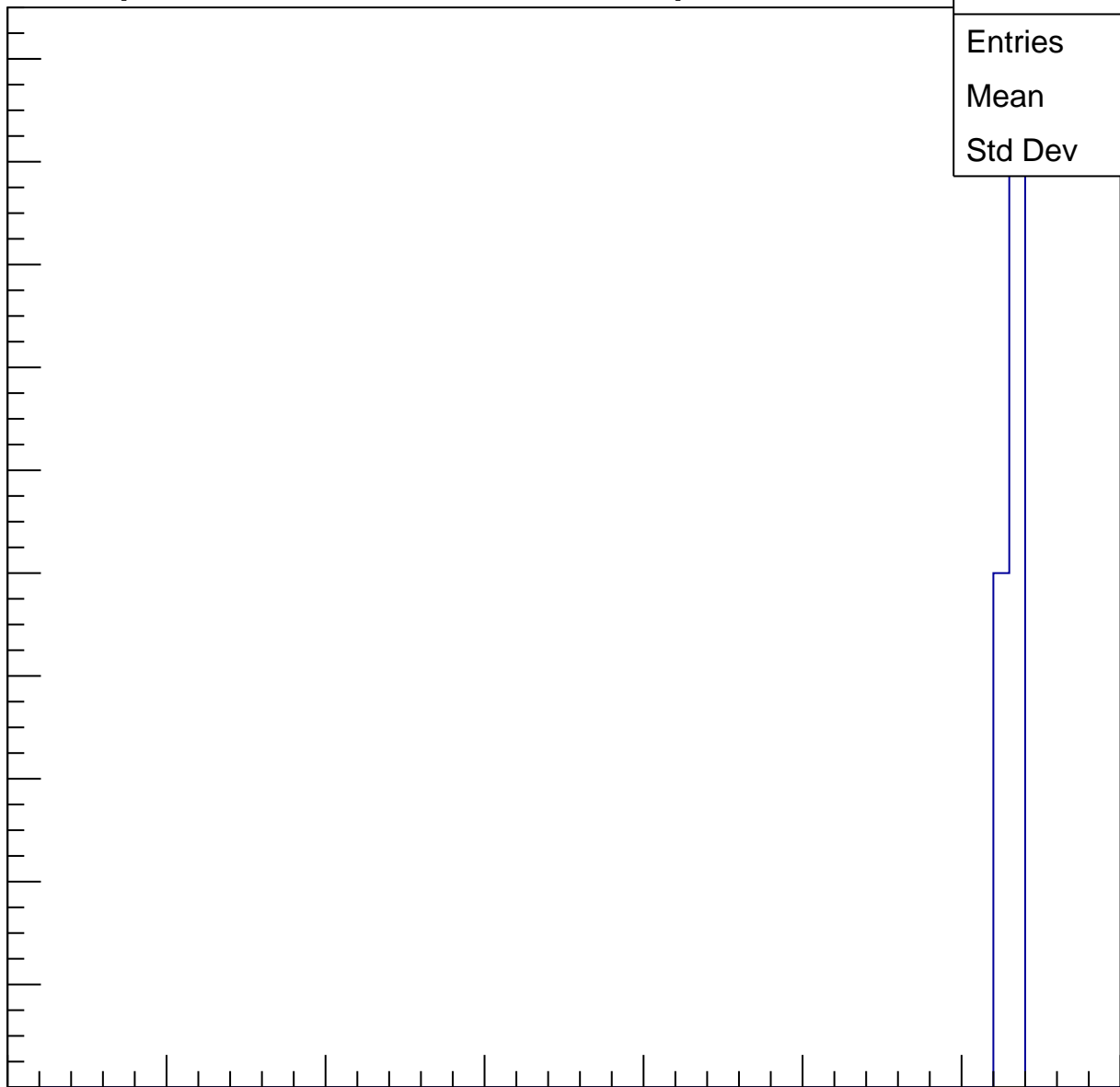
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	3
Mean	62.67
Std Dev	0.4714

0 10 20 30 40 50 60 70

ampl





# B0L002S, U2-ch1, adc7

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



Entries	1
Mean	23
Std Dev	0

# B0L002S, U2-ch2, adc0

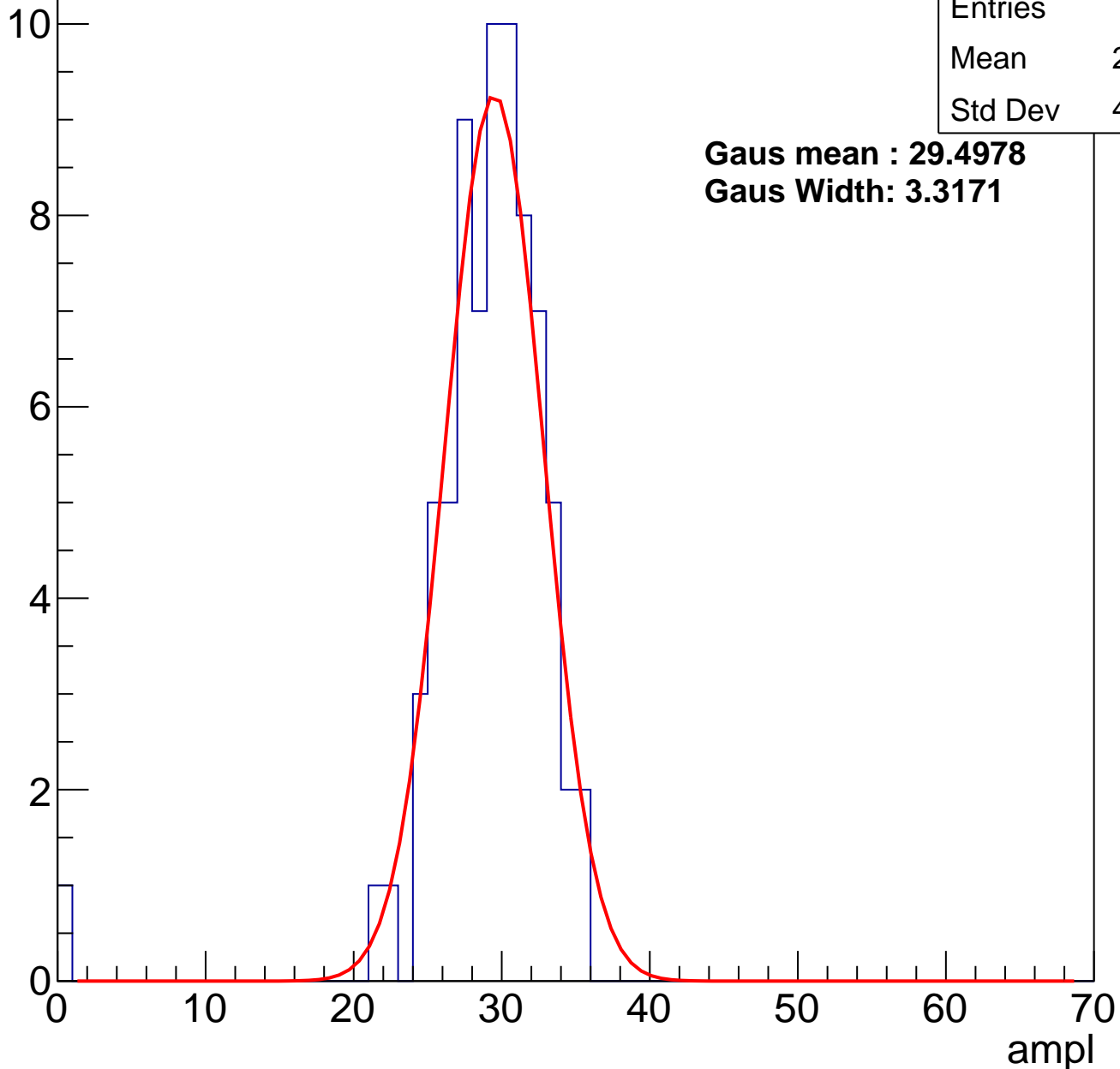
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entries	76
Mean	28.61
Std Dev	4.431

**Gaus mean : 29.4978**

**Gaus Width: 3.3171**

Entry



# B0L002S, U2-ch2, adc1

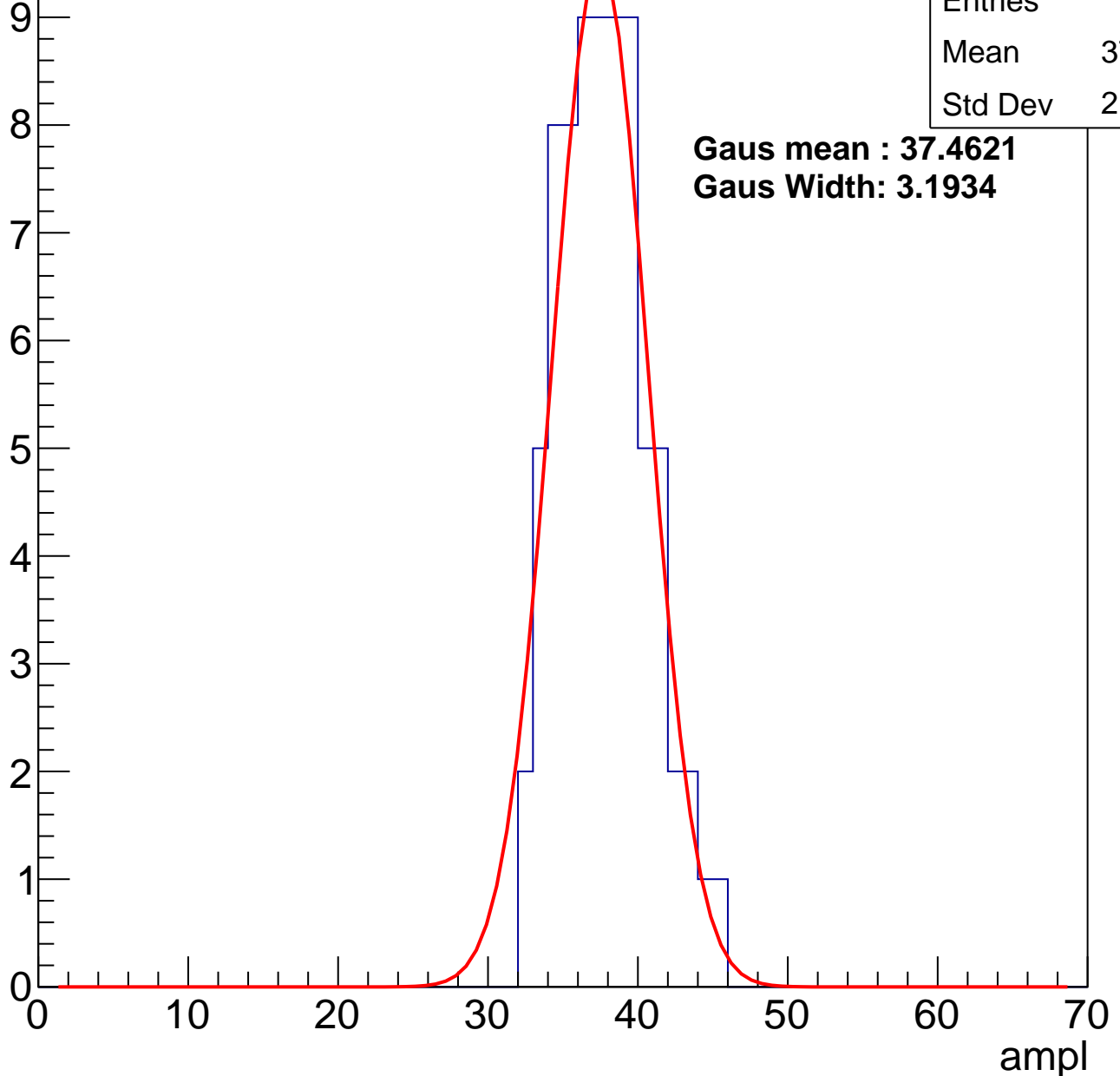
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	75
Mean	37.27
Std Dev	2.927

**Gaus mean : 37.4621**

**Gaus Width: 3.1934**



# B0L002S, U2-ch2, adc2

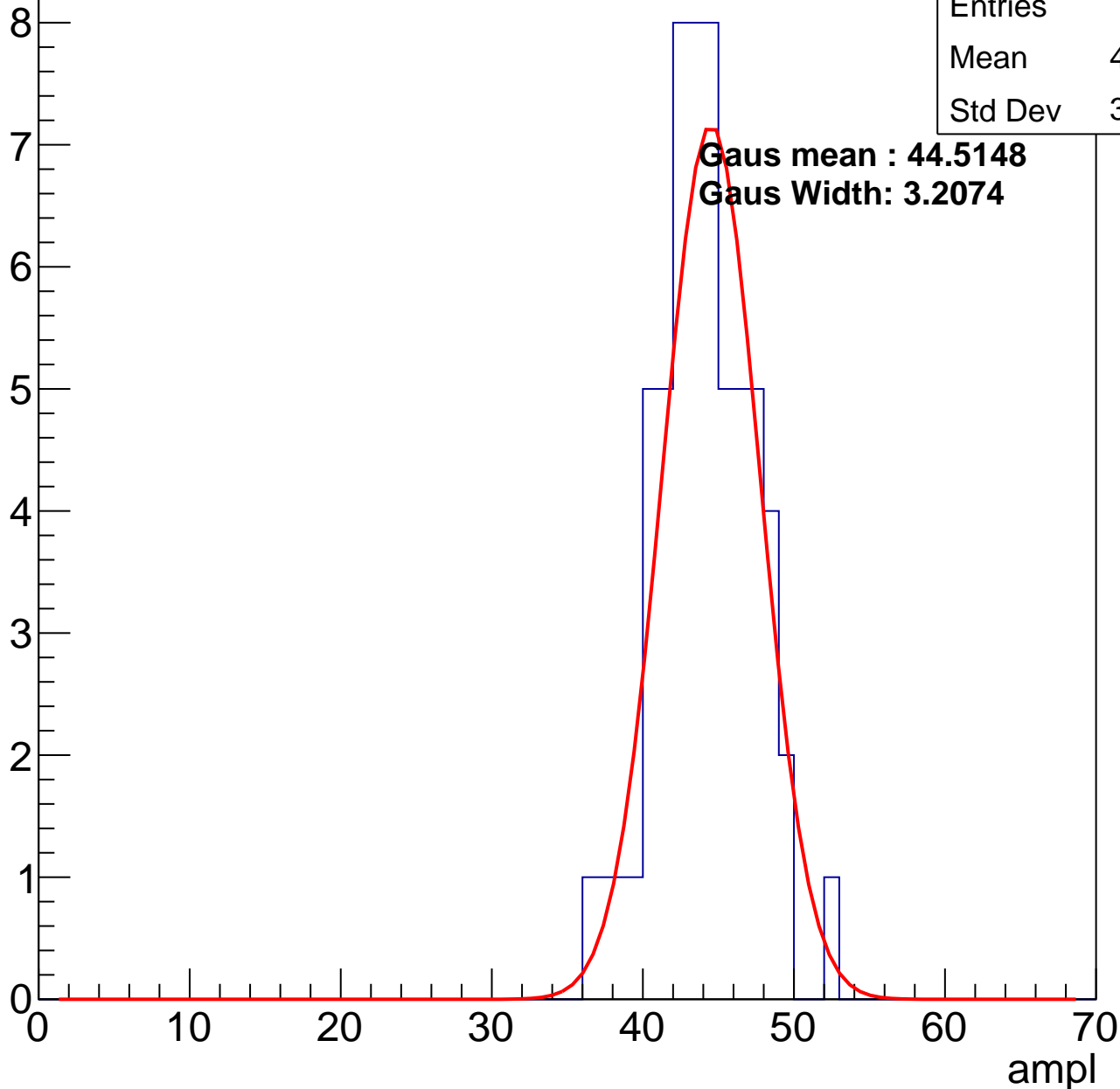
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	60
Mean	43.65
Std Dev	3.108

**Gaus mean : 44.5148**

**Gaus Width: 3.2074**

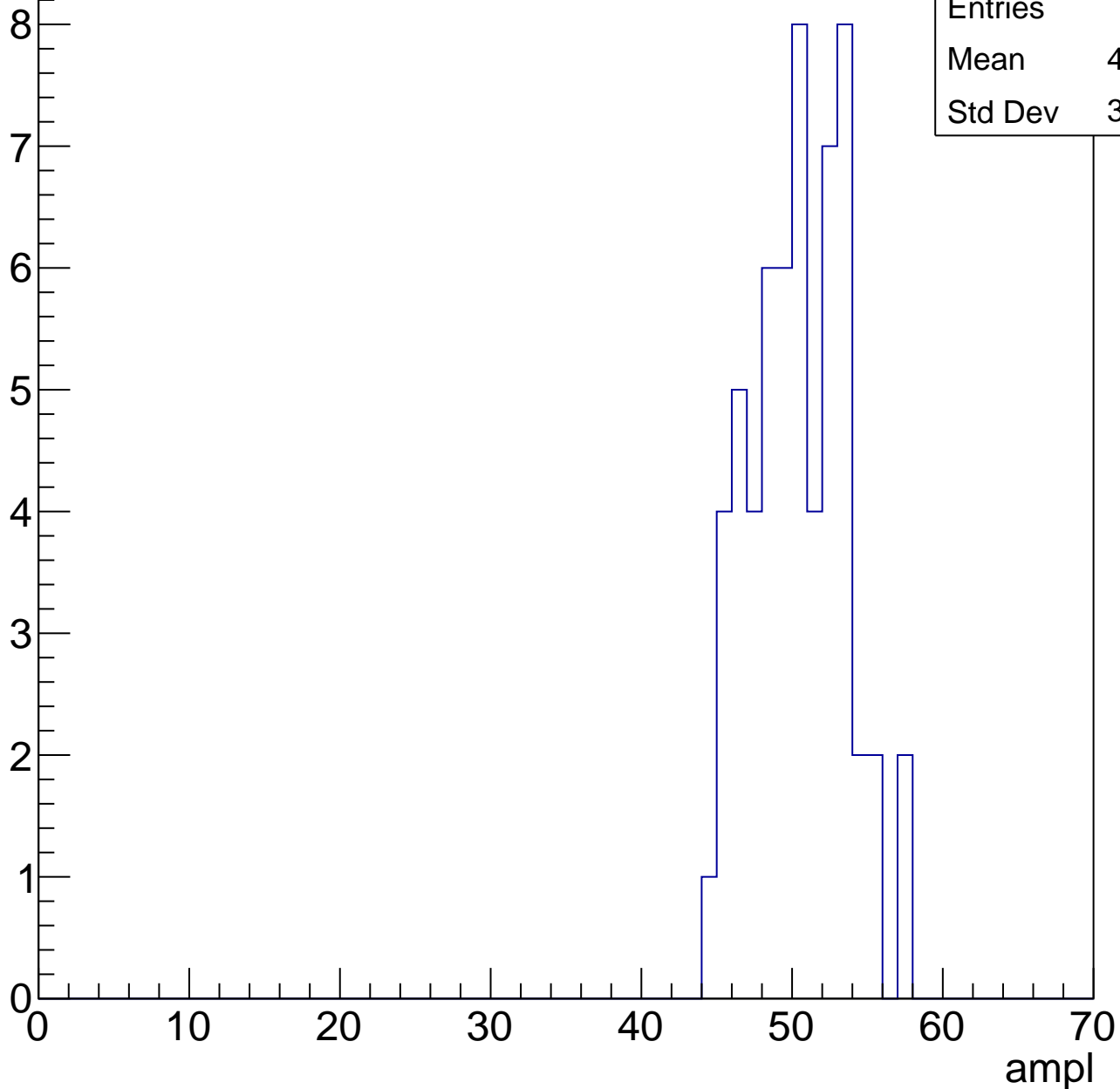


# B0L002S, U2-ch2, adc3

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	59
Mean	49.97
Std Dev	3.097

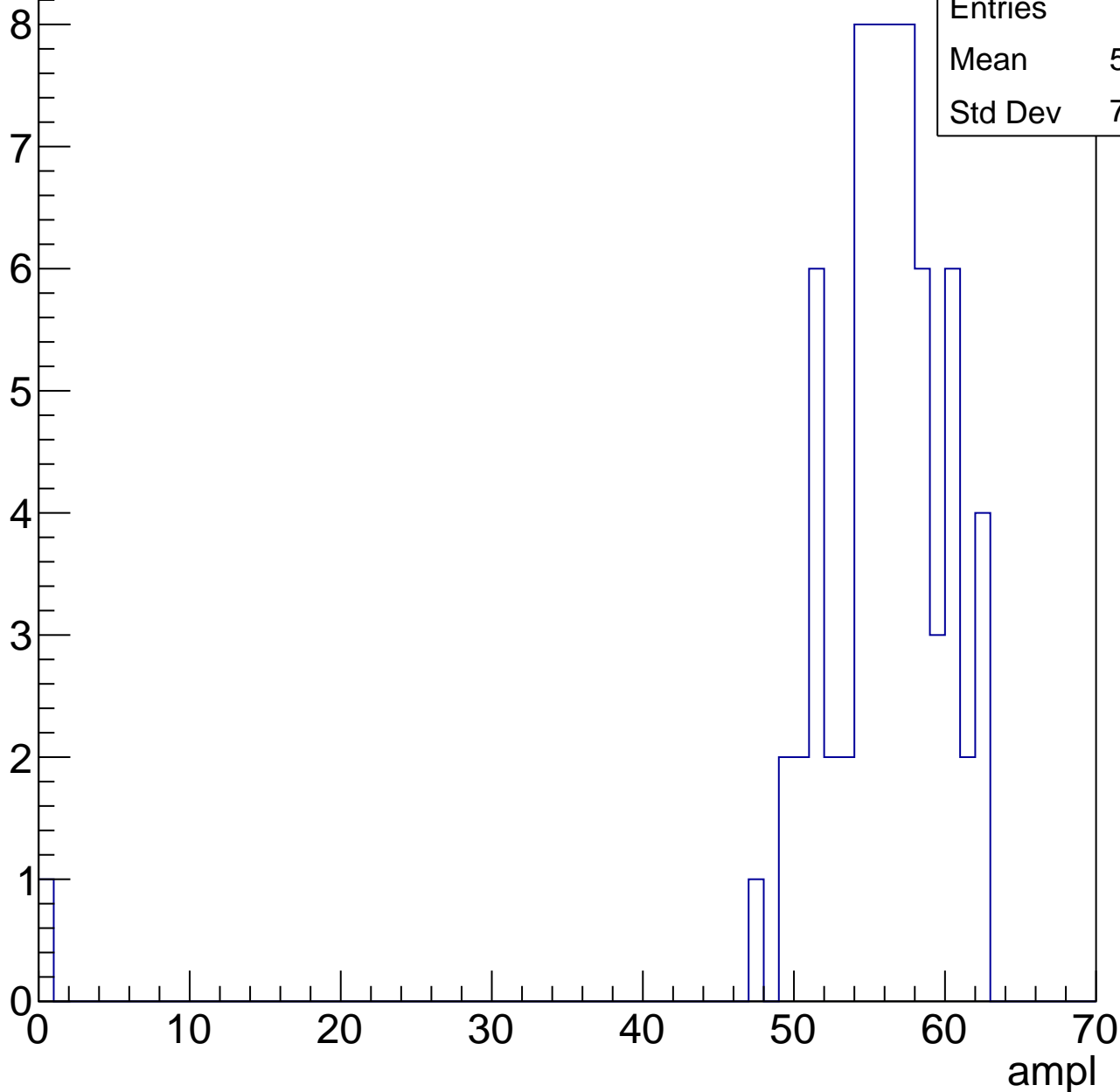


# B0L002S, U2-ch2, adc4

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

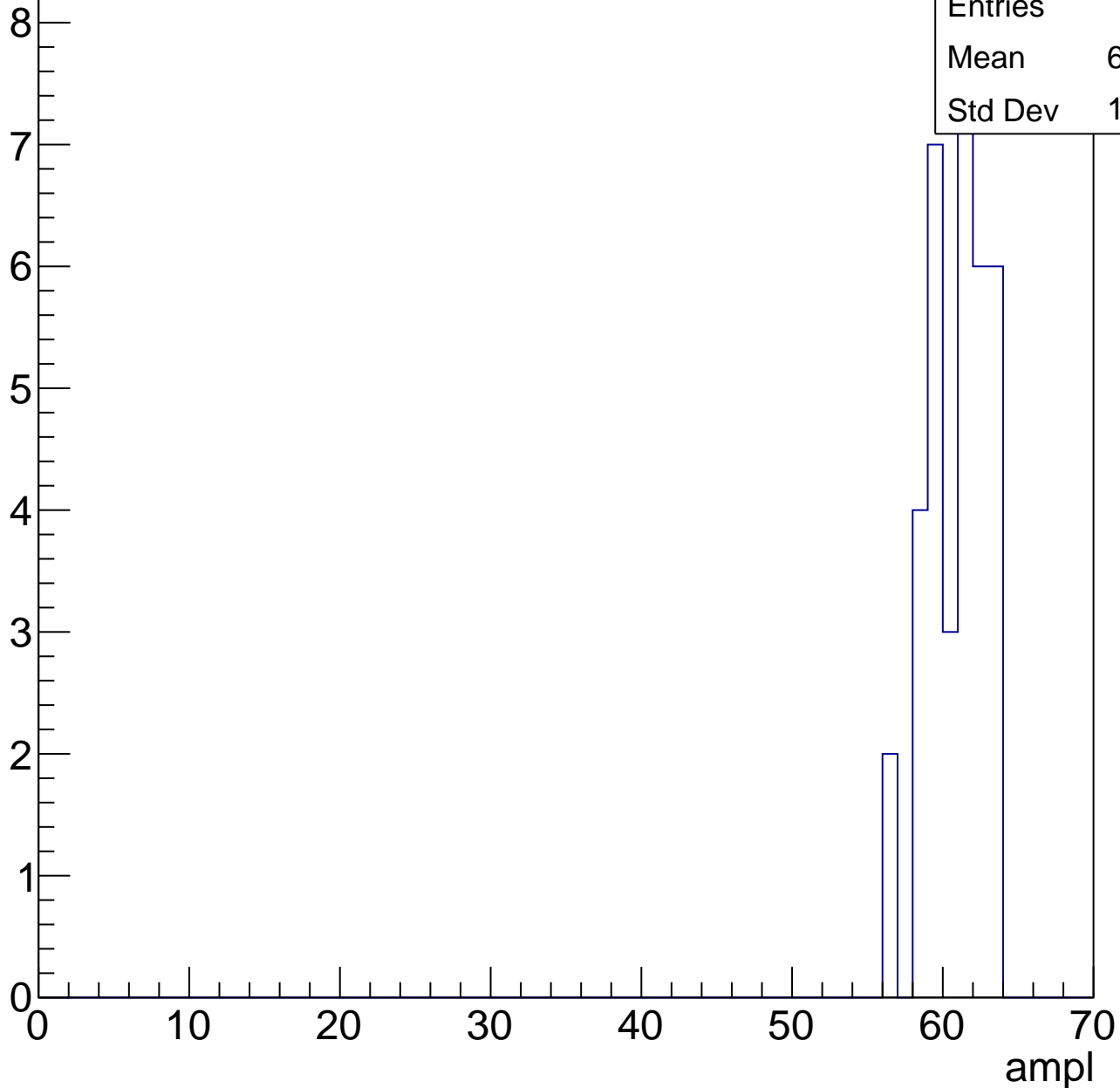
Entries	69
Mean	54.96
Std Dev	7.519



# B0L002S, U2-ch2, adc5

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

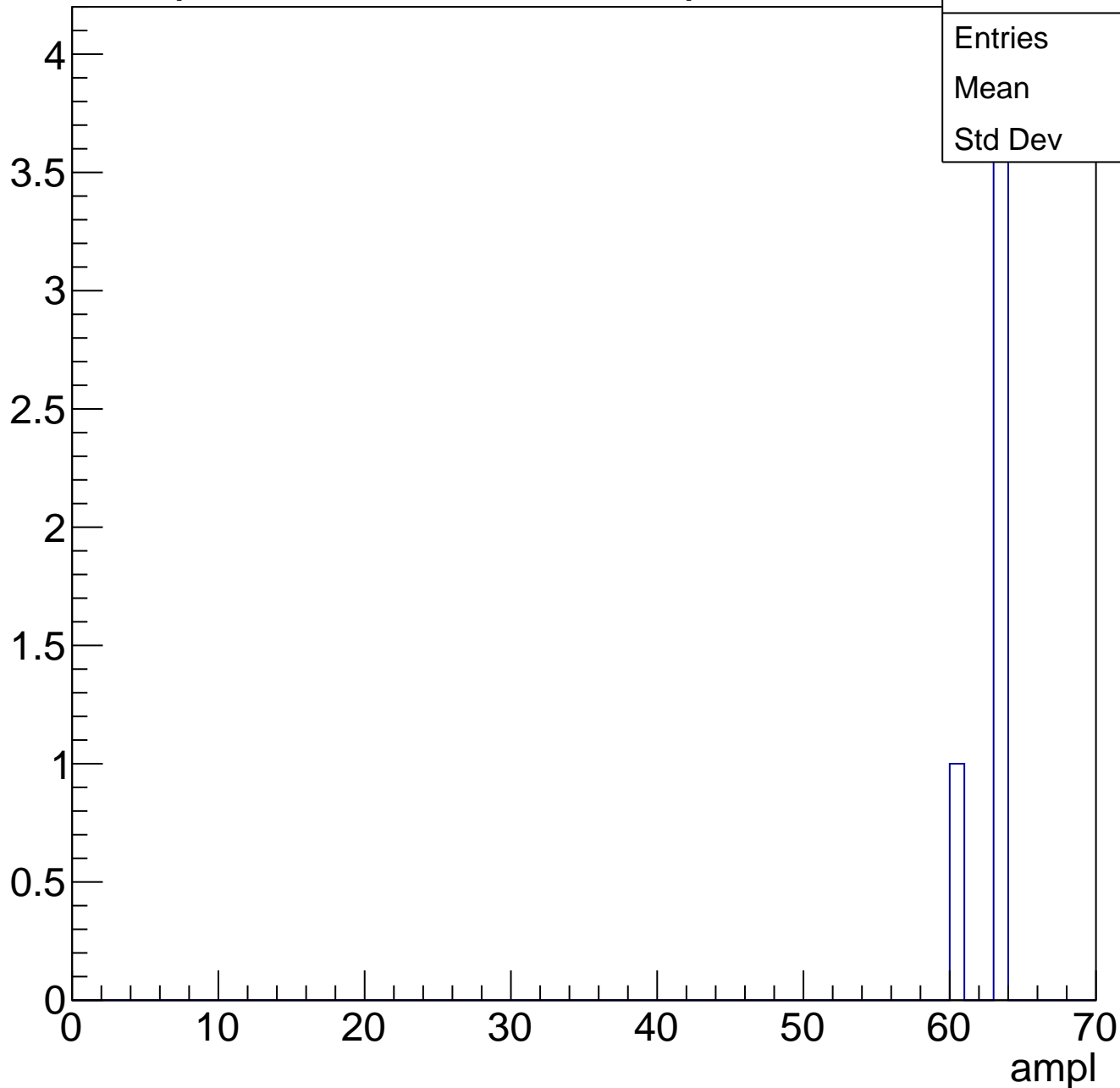


Entries	36
Mean	60.42
Std Dev	1.935

# B0L002S, U2-ch2, adc6

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

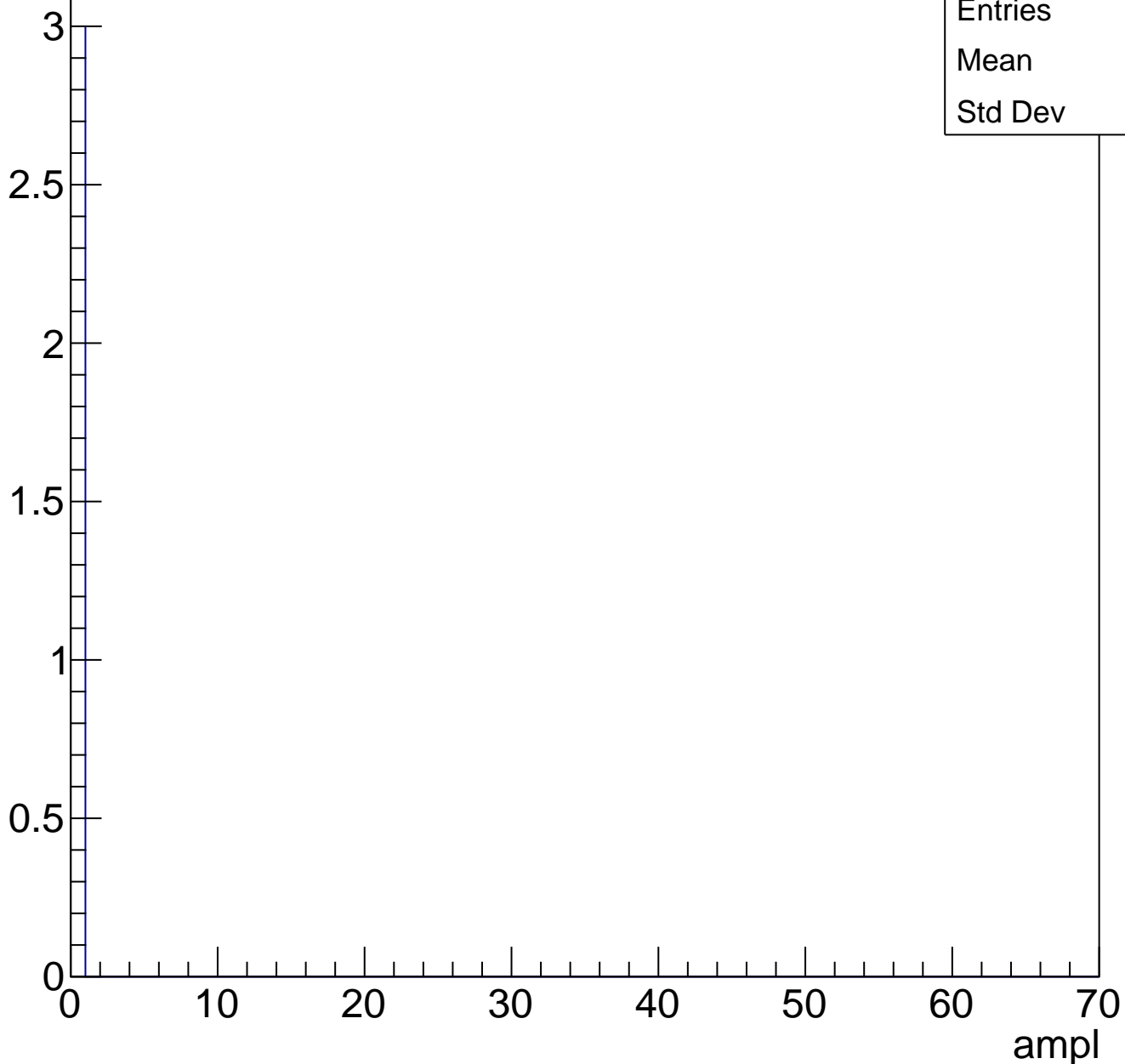




# B0L002S, U2-ch2, adc7

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



Entries	3
Mean	0
Std Dev	0

# B0L002S, U2-ch3, adc0

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entries	81
Mean	28.75
Std Dev	3.939

**Gaus mean : 29.5434**

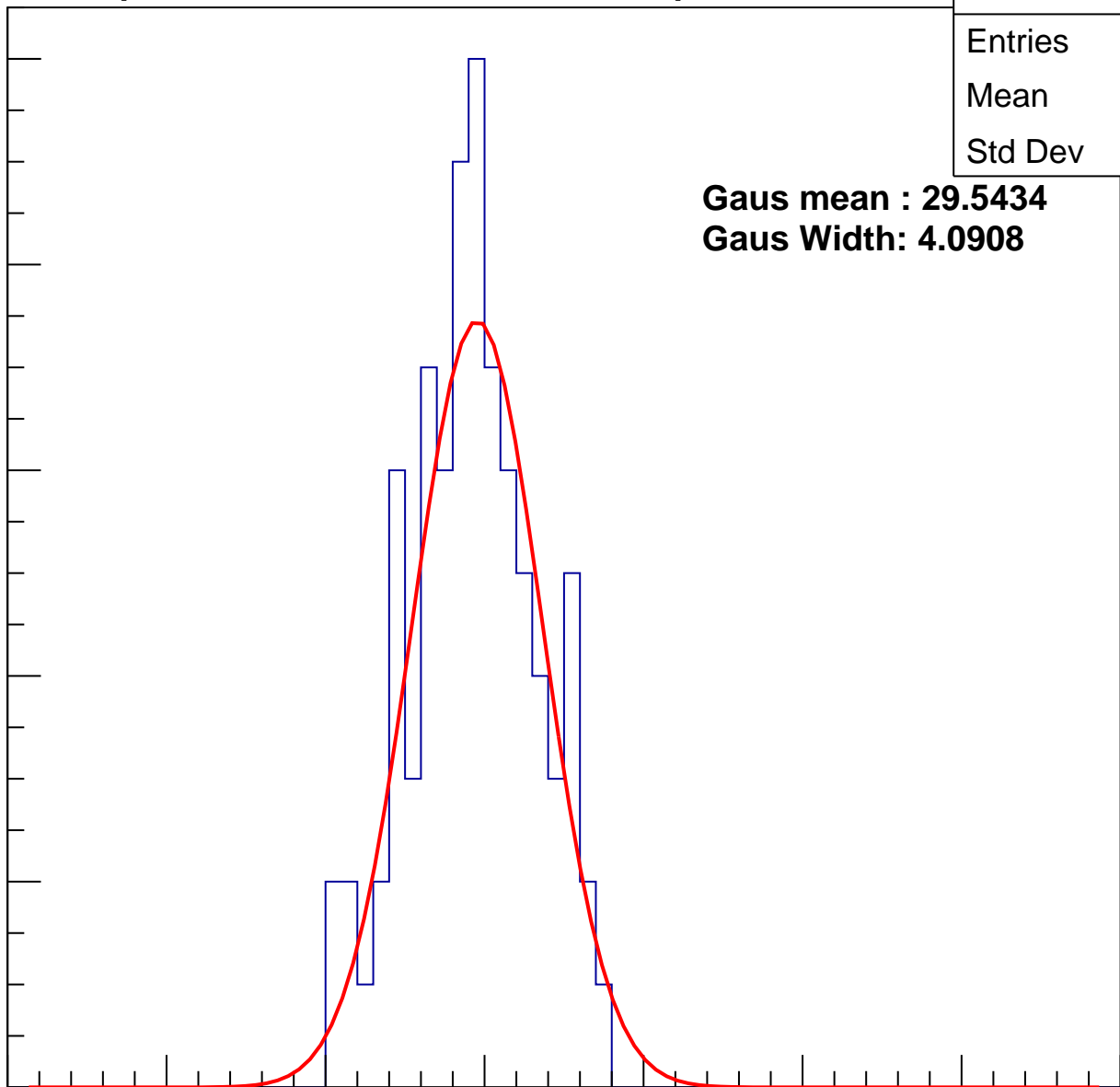
**Gaus Width: 4.0908**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L002S, U2-ch3, adc1

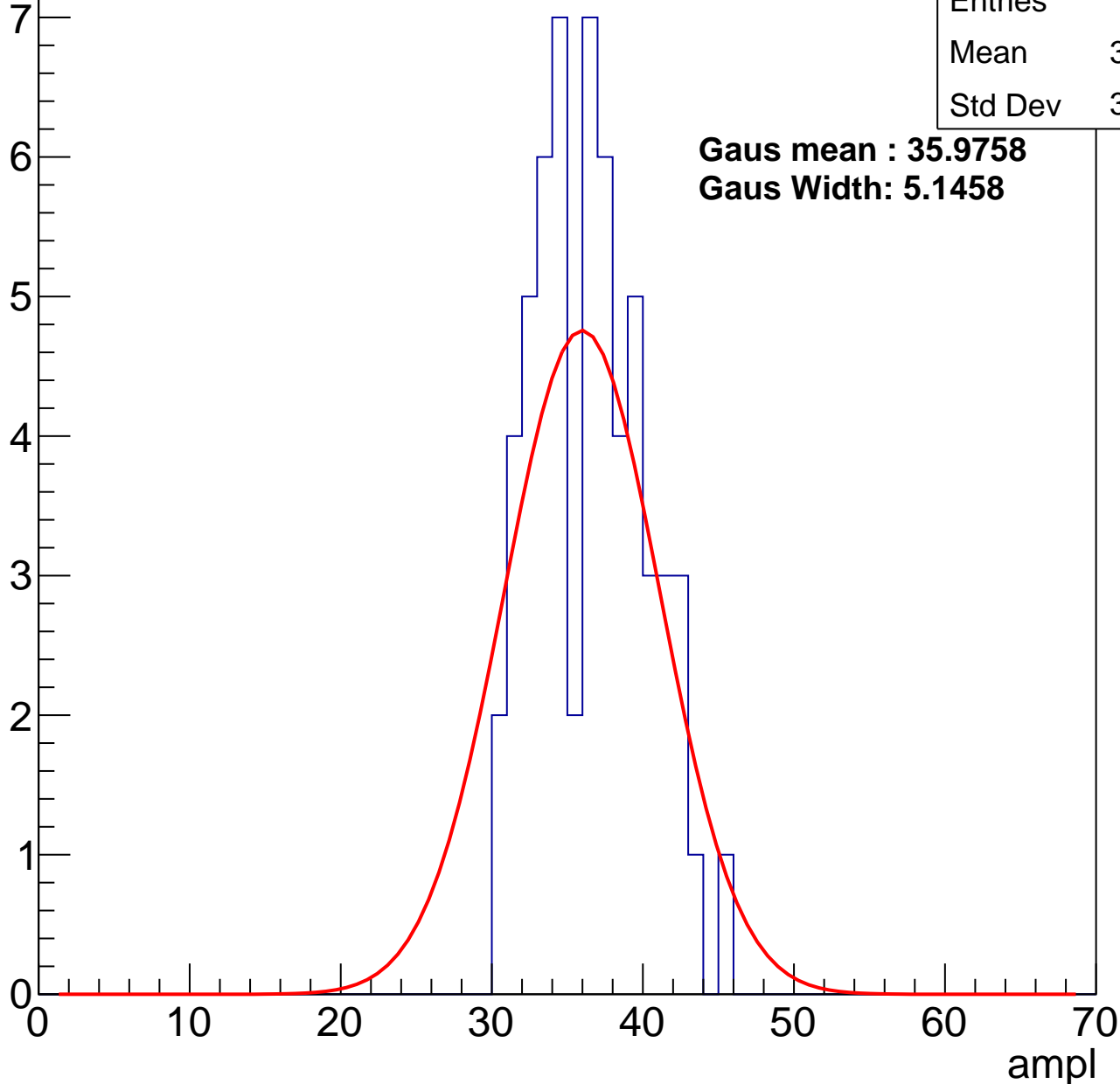
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	59
Mean	36.07
Std Dev	3.598

**Gaus mean : 35.9758**

**Gaus Width: 5.1458**



# B0L002S, U2-ch3, adc2

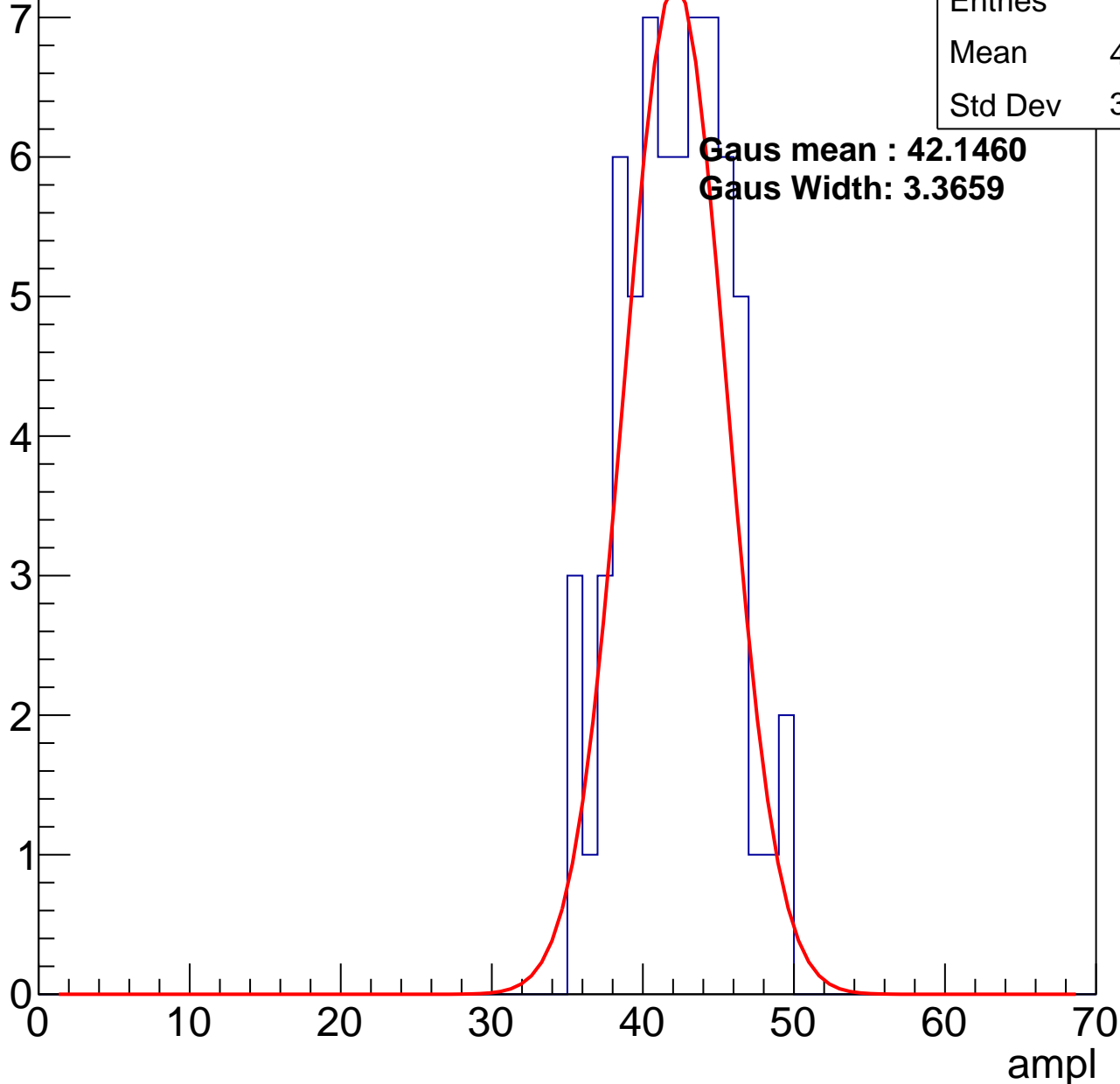
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	66
Mean	41.74
Std Dev	3.386

**Gaus mean : 42.1460**

**Gaus Width: 3.3659**

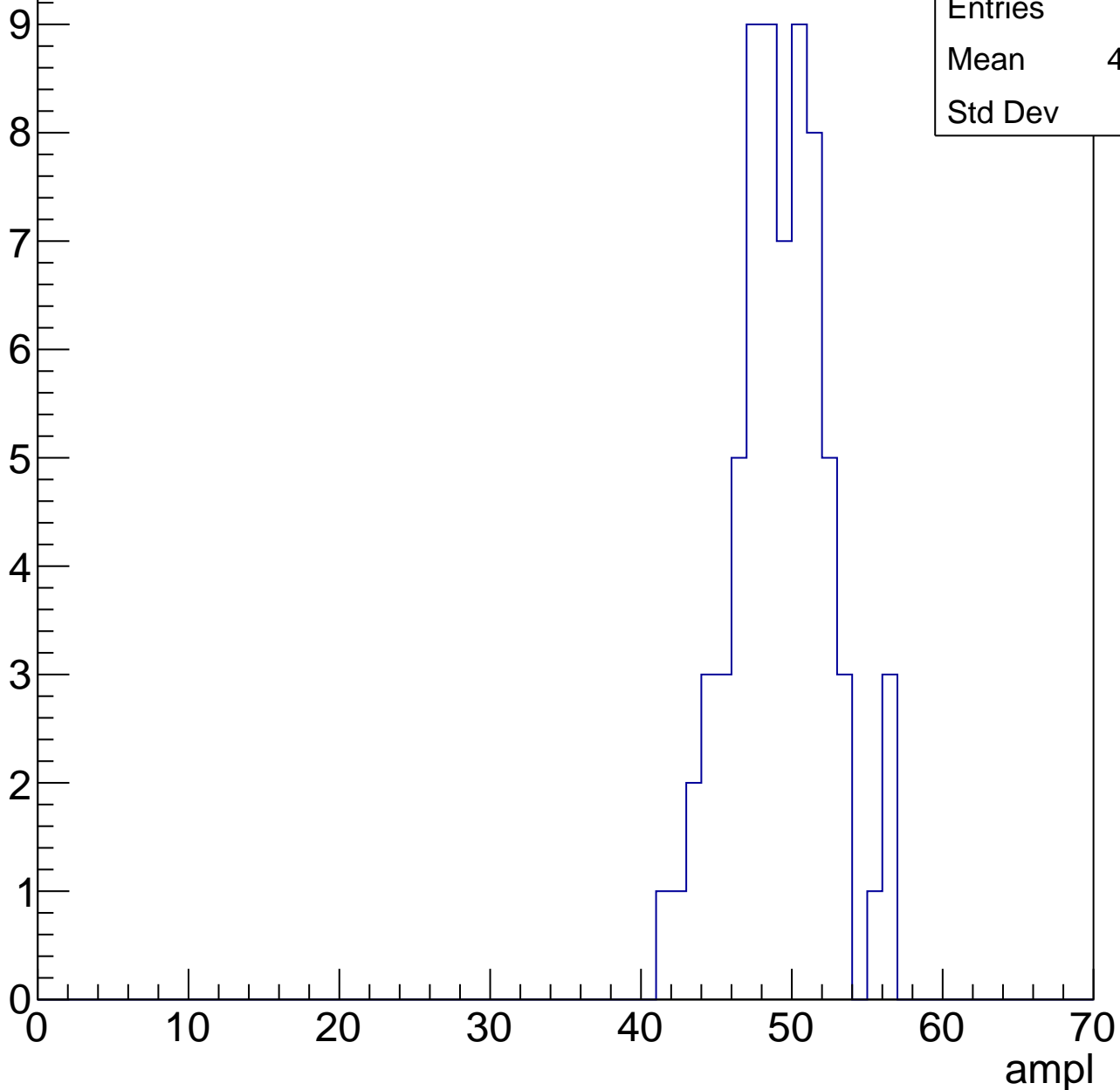


# B0L002S, U2-ch3, adc3

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	69
Mean	48.75
Std Dev	3.21

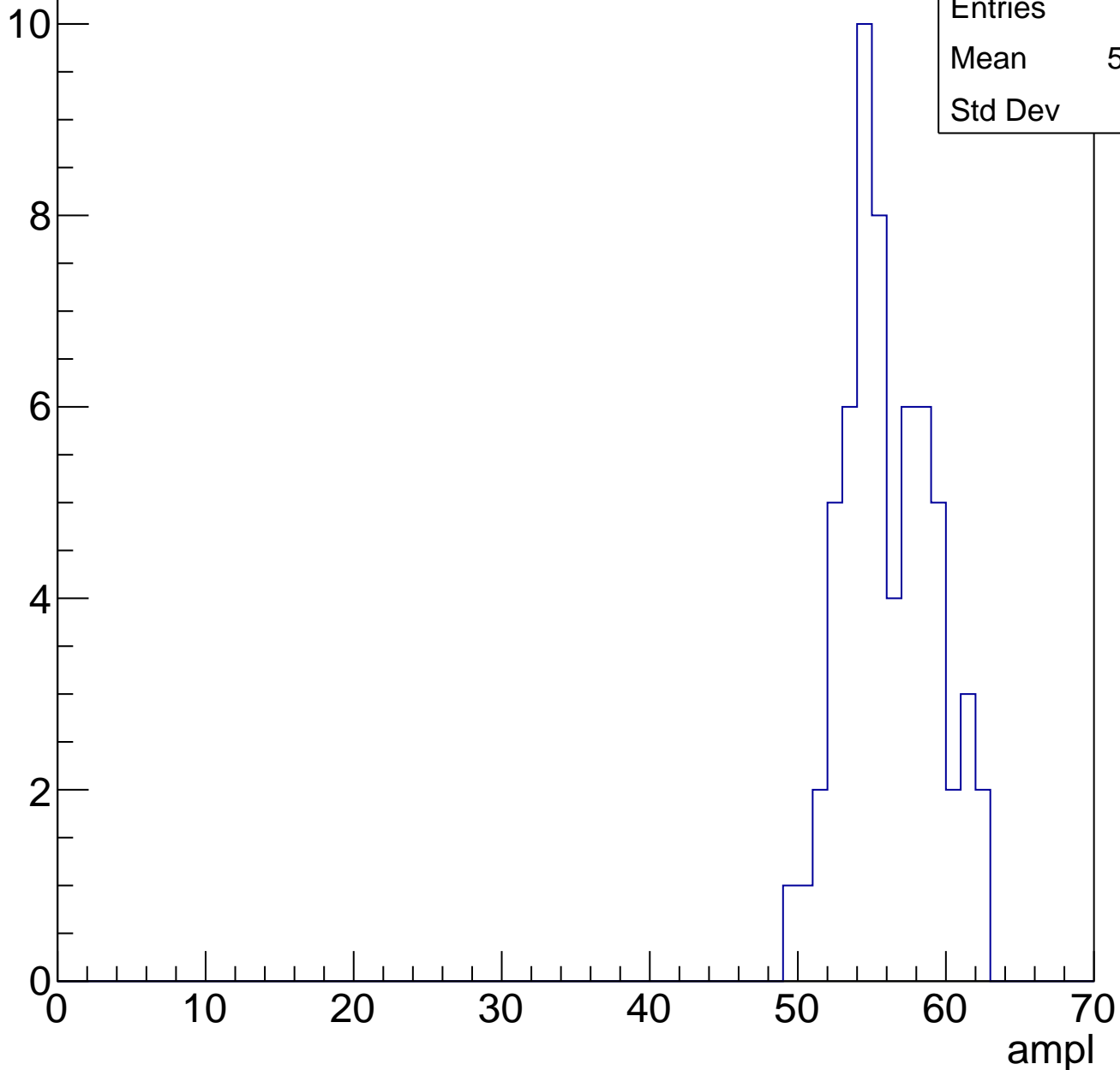


# B0L002S, U2-ch3, adc4

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entries	61
Mean	55.66
Std Dev	3.04

Entry

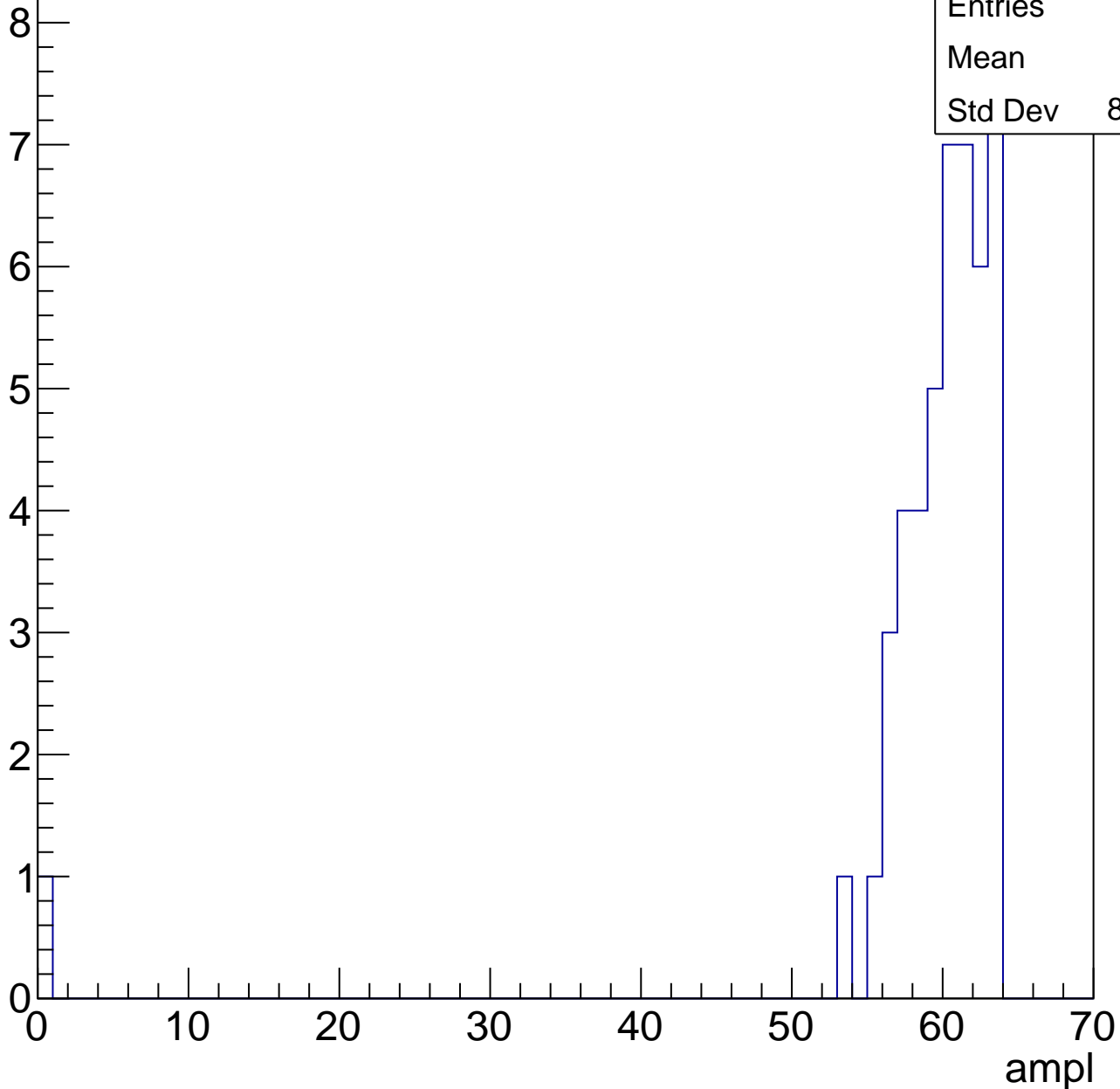


# B0L002S, U2-ch3, adc5

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	47
Mean	58.6
Std Dev	8.979



# B0L002S, U2-ch3, adc6

calib\_packv5\_042523\_0143.root, FC#8, port C1

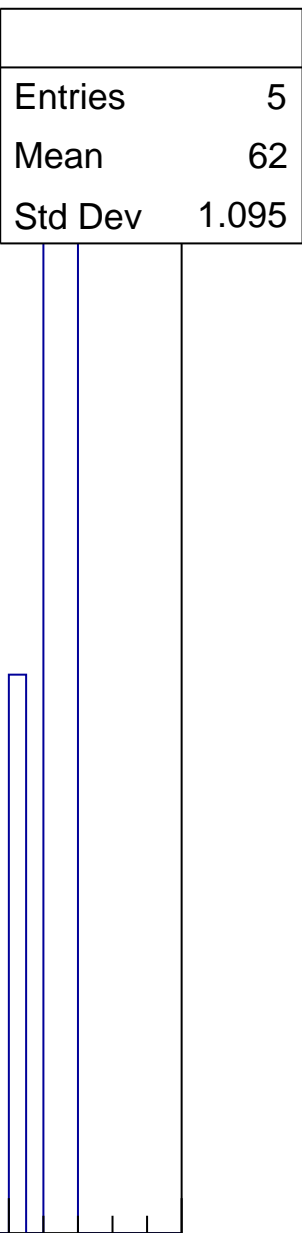
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	5
Mean	62
Std Dev	1.095

0 10 20 30 40 50 60 70

ampl

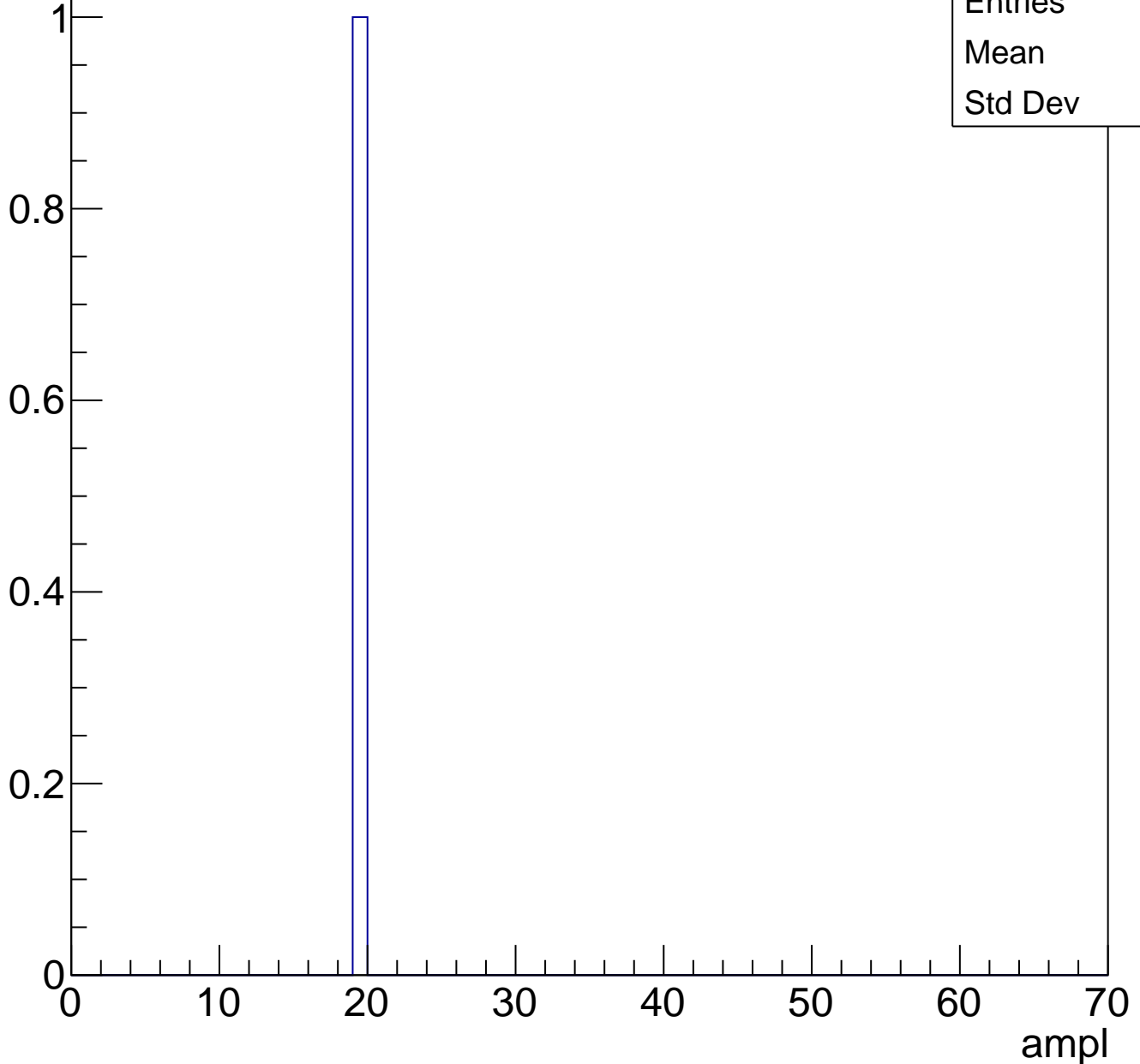




# B0L002S, U2-ch3, adc7

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



# B0L002S, U2-ch4, adc0

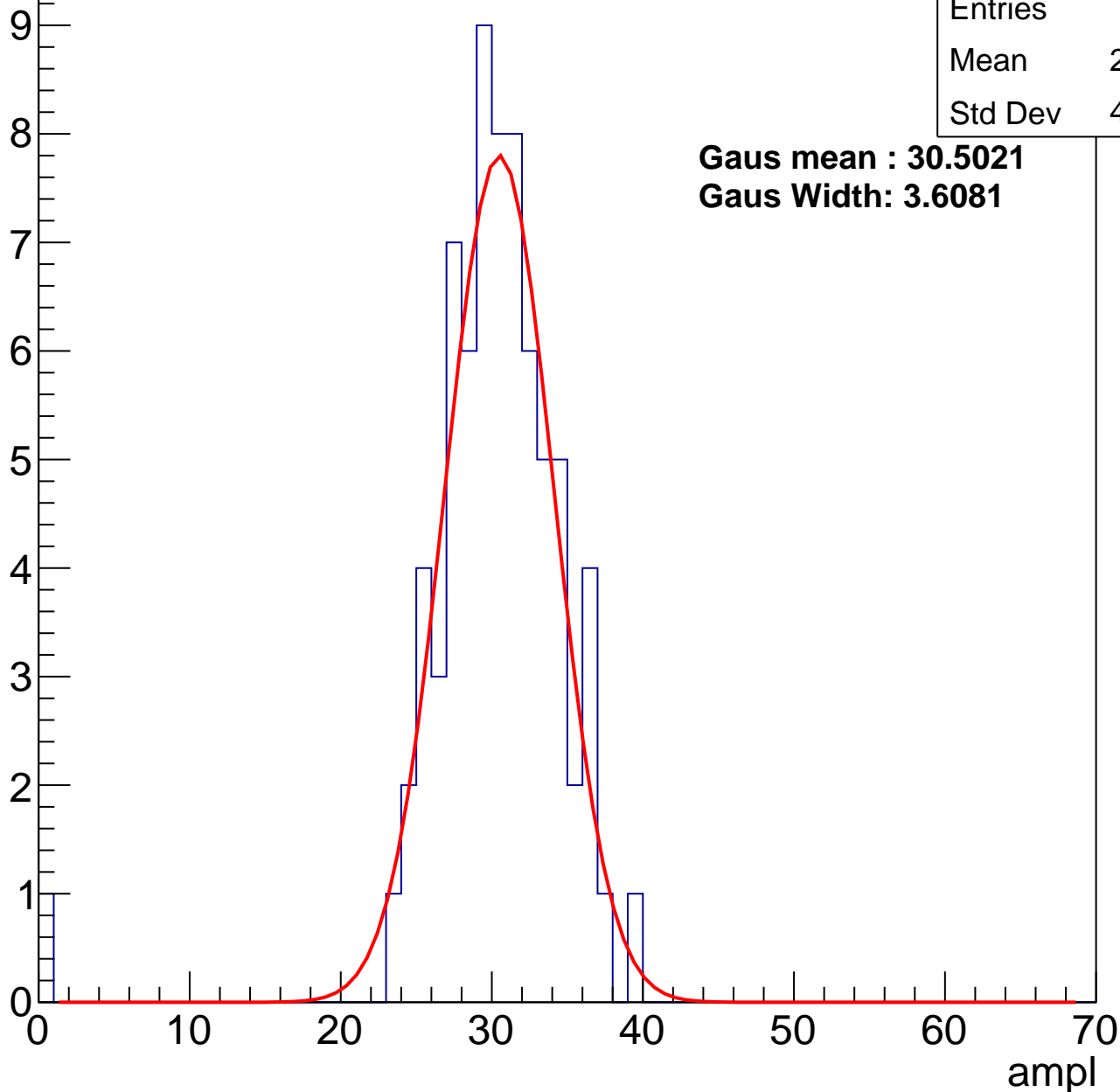
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	73
Mean	29.75
Std Dev	4.884

**Gaus mean : 30.5021**

**Gaus Width: 3.6081**



# B0L002S, U2-ch4, adc1

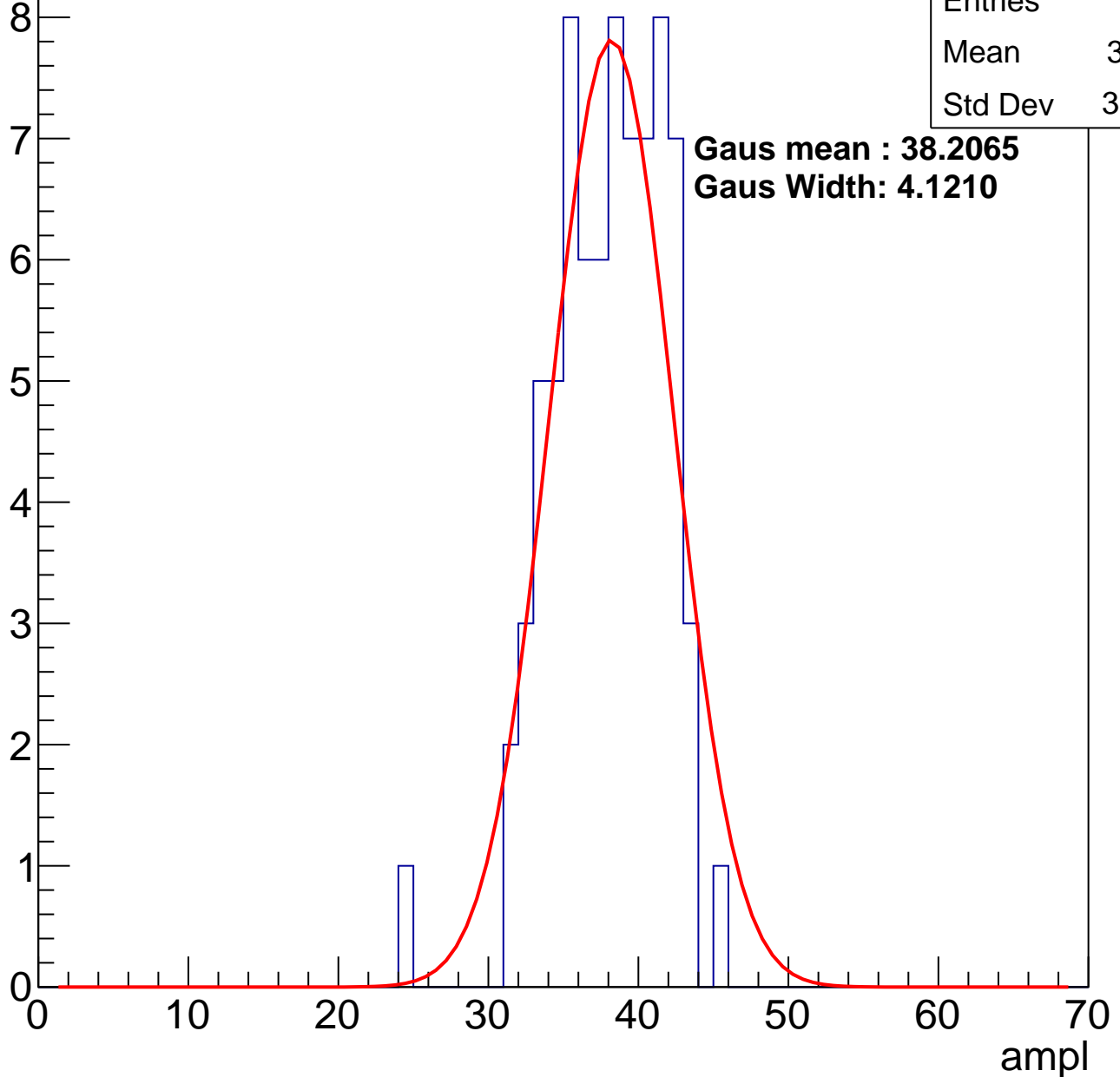
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	77
Mean	37.51
Std Dev	3.663

**Gaus mean : 38.2065**

**Gaus Width: 4.1210**



# B0L002S, U2-ch4, adc2

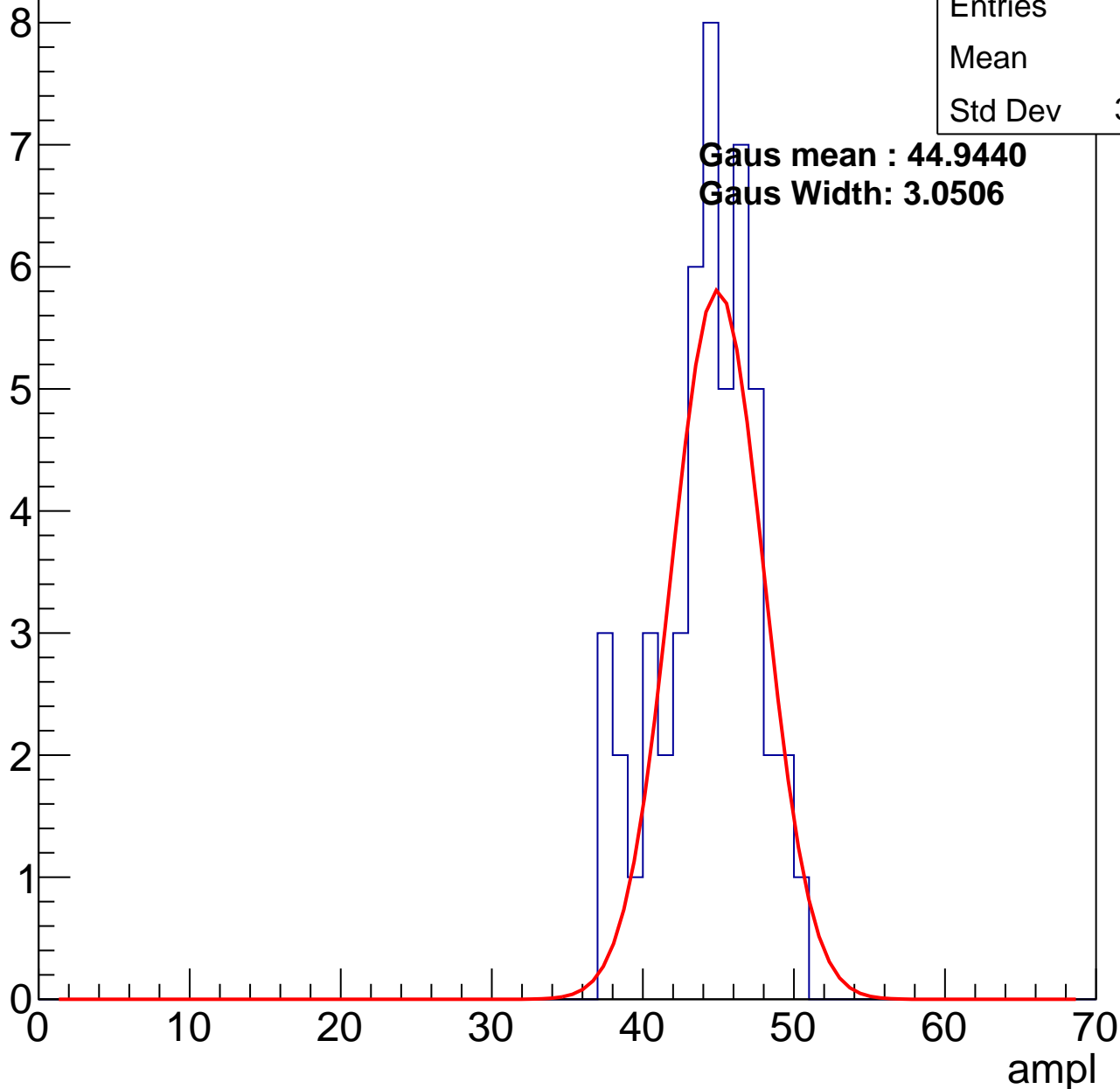
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	50
Mean	43.8
Std Dev	3.231

**Gaus mean : 44.9440**

**Gaus Width: 3.0506**

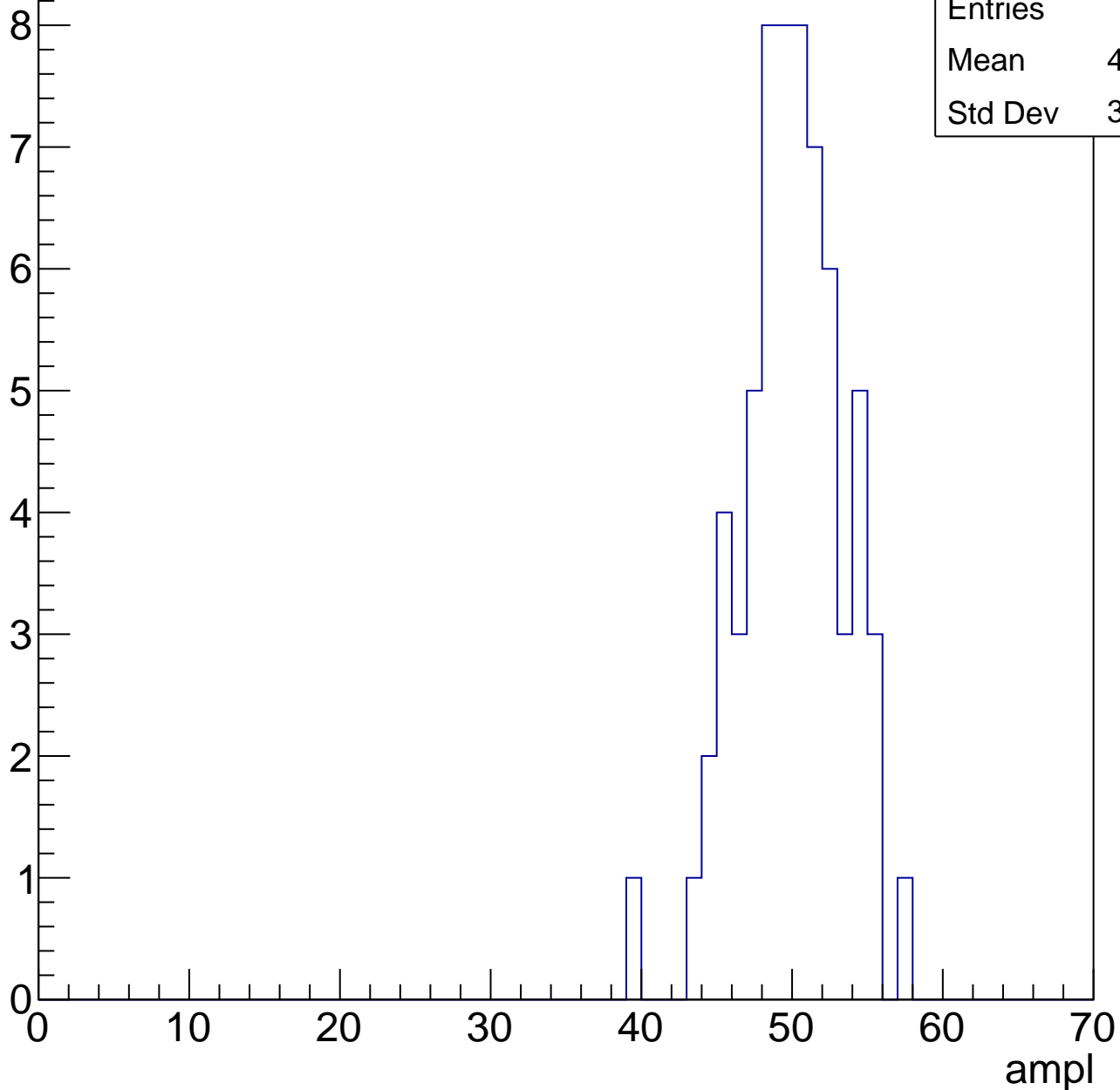


# B0L002S, U2-ch4, adc3

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	65
Mean	49.52
Std Dev	3.333

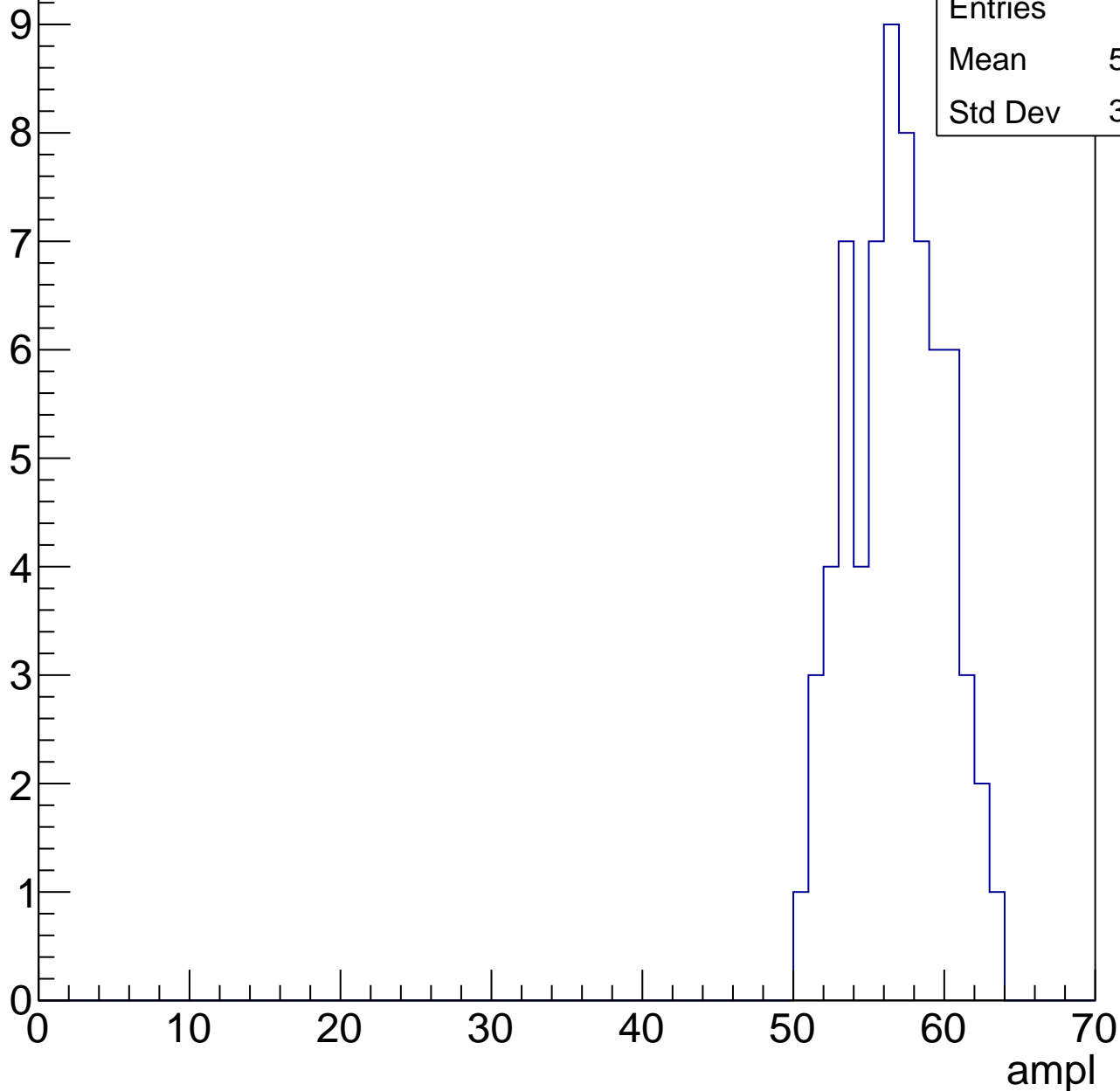


# B0L002S, U2-ch4, adc4

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

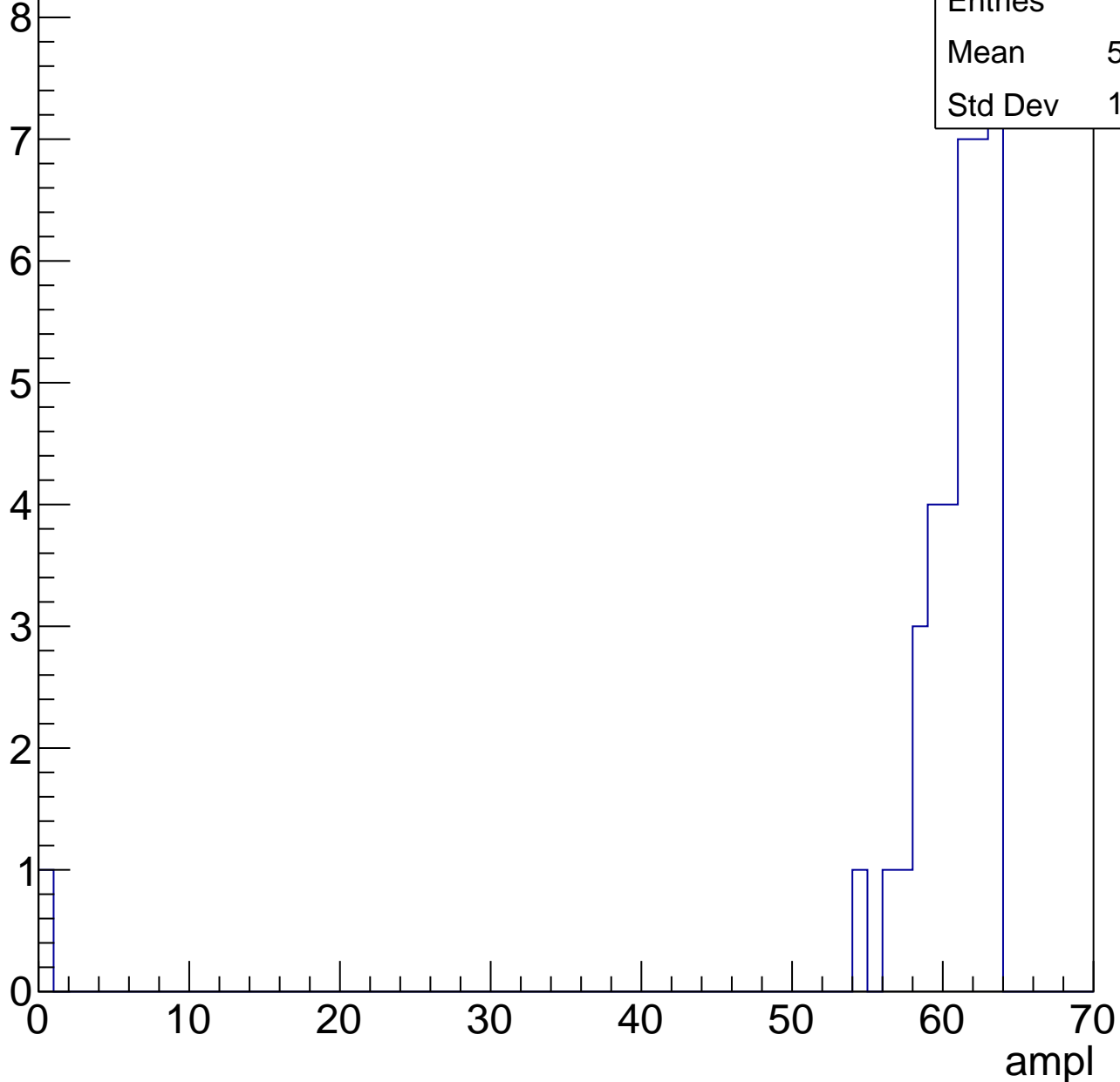
Entries	68
Mean	56.37
Std Dev	3.053



# B0L002S, U2-ch4, adc5

calib\_packv5\_042523\_0143.root, FC#8, port C1

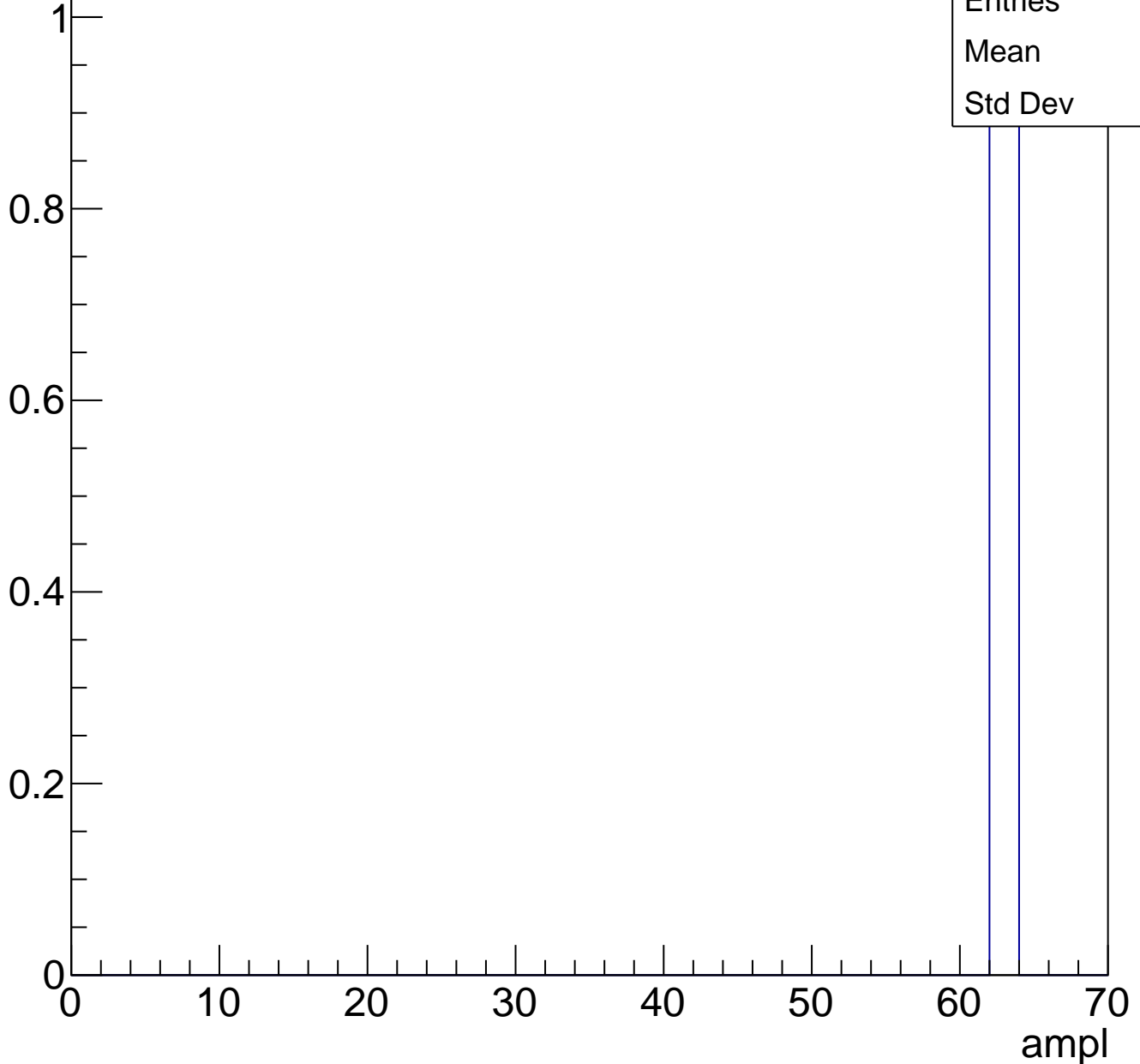
Entry



# B0L002S, U2-ch4, adc6

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry





# B0L002S, U2-ch4, adc7

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L002S, U2-ch5, adc0

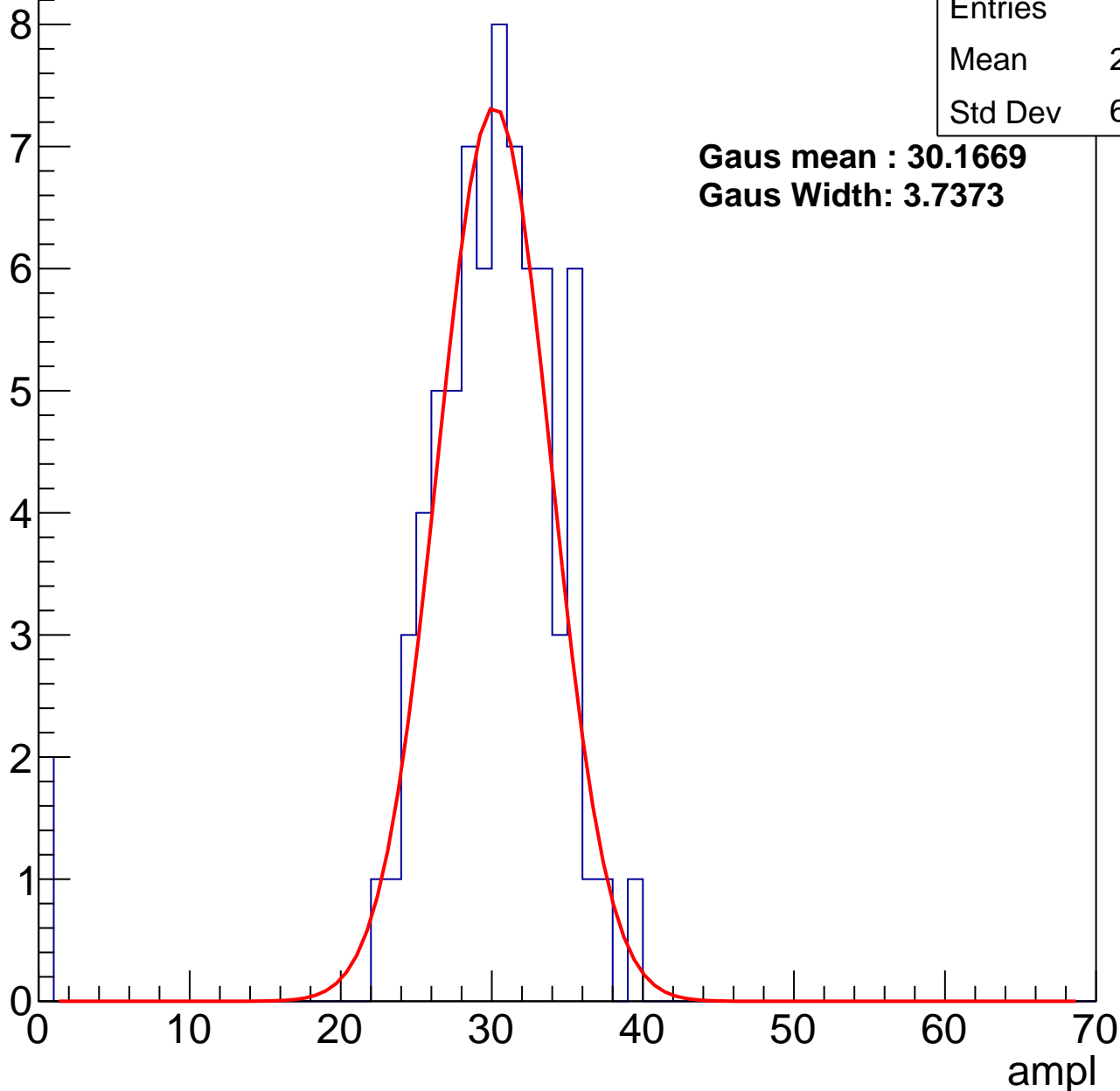
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	73
Mean	29.08
Std Dev	6.045

**Gaus mean : 30.1669**

**Gaus Width: 3.7373**



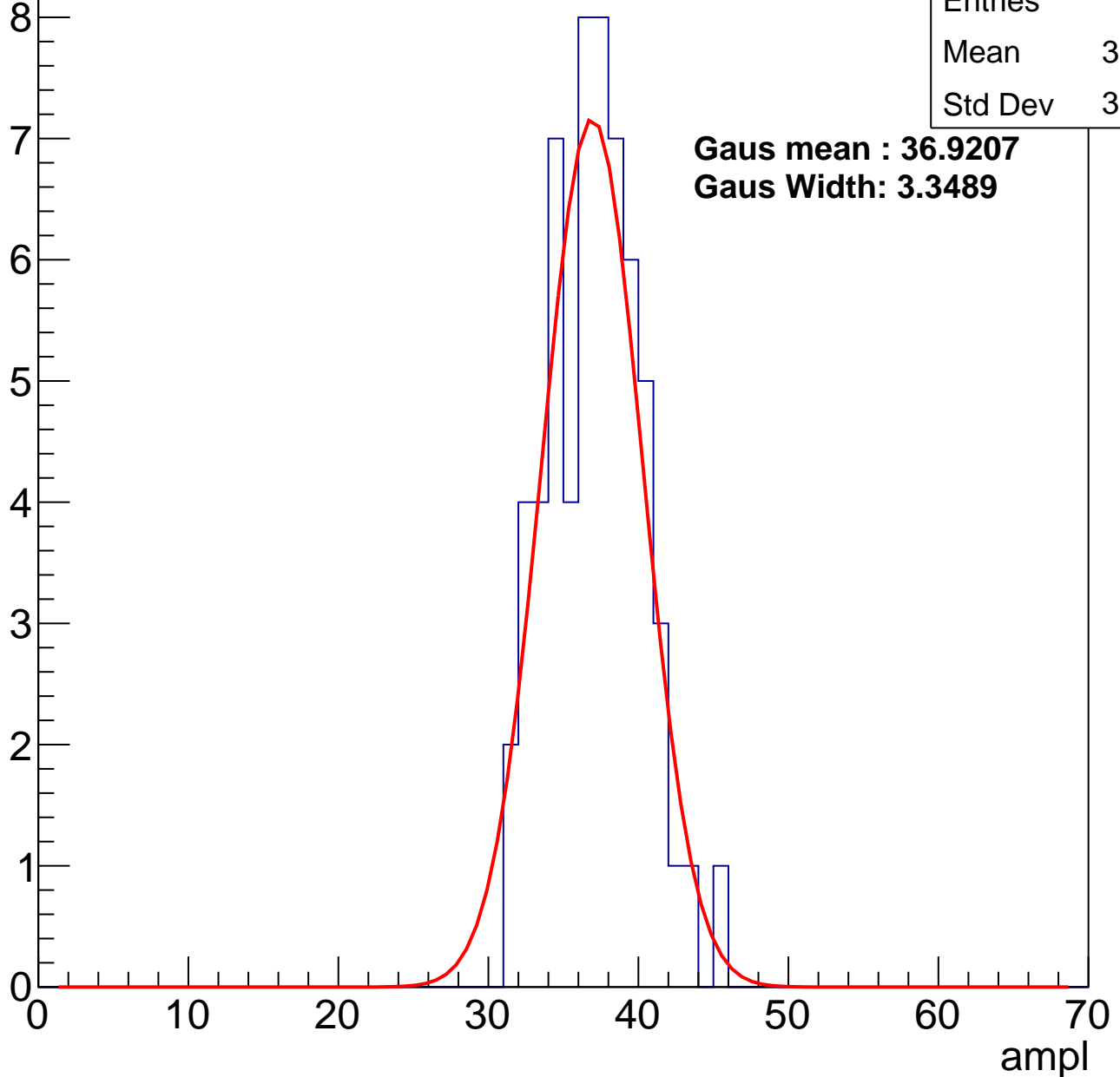
# B0L002S, U2-ch5, adc1

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	61
Mean	36.67
Std Dev	3.045

**Gaus mean : 36.9207**  
**Gaus Width: 3.3489**



# B0L002S, U2-ch5, adc2

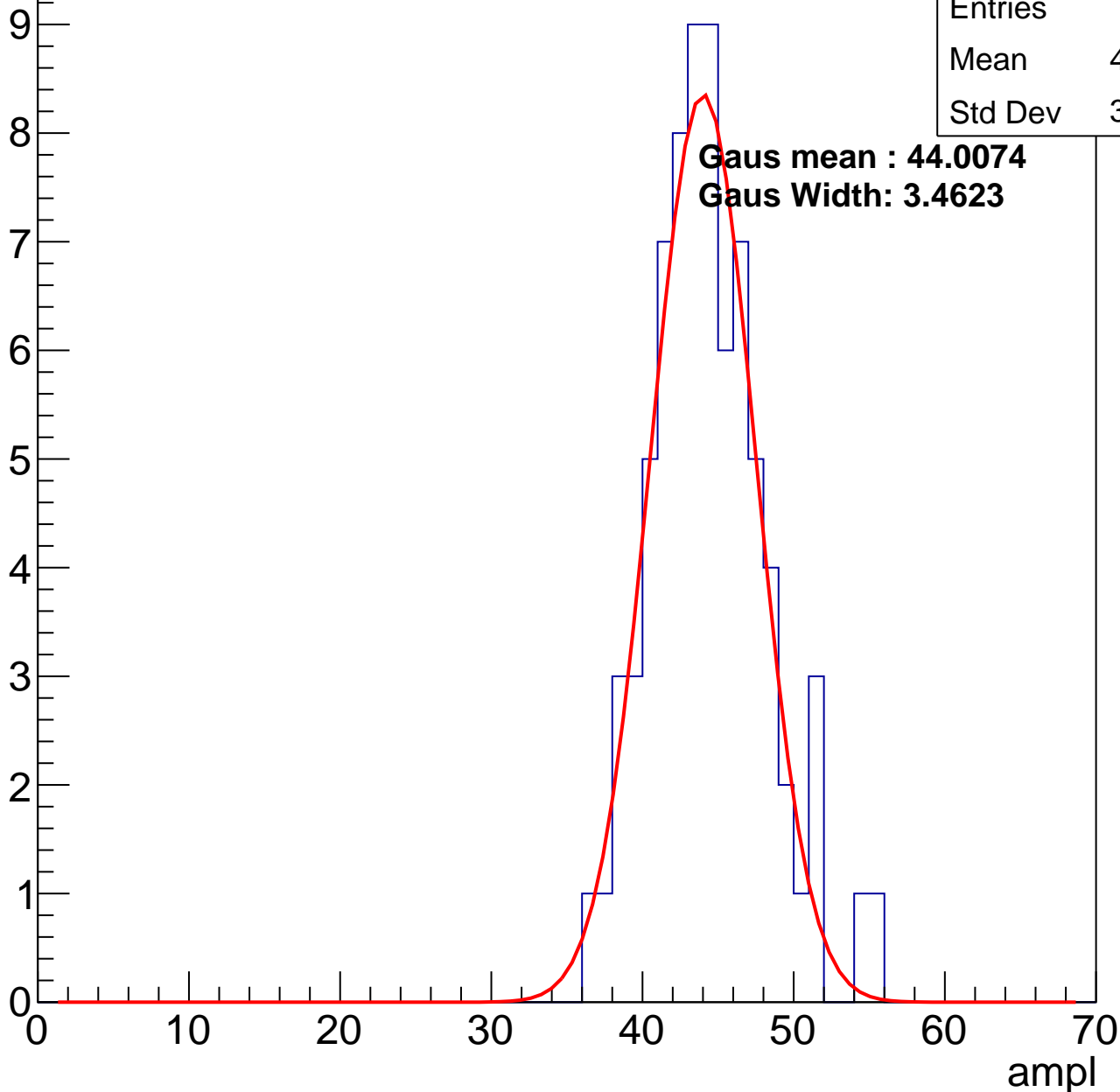
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	76
Mean	43.93
Std Dev	3.764

**Gaus mean : 44.0074**

**Gaus Width: 3.4623**

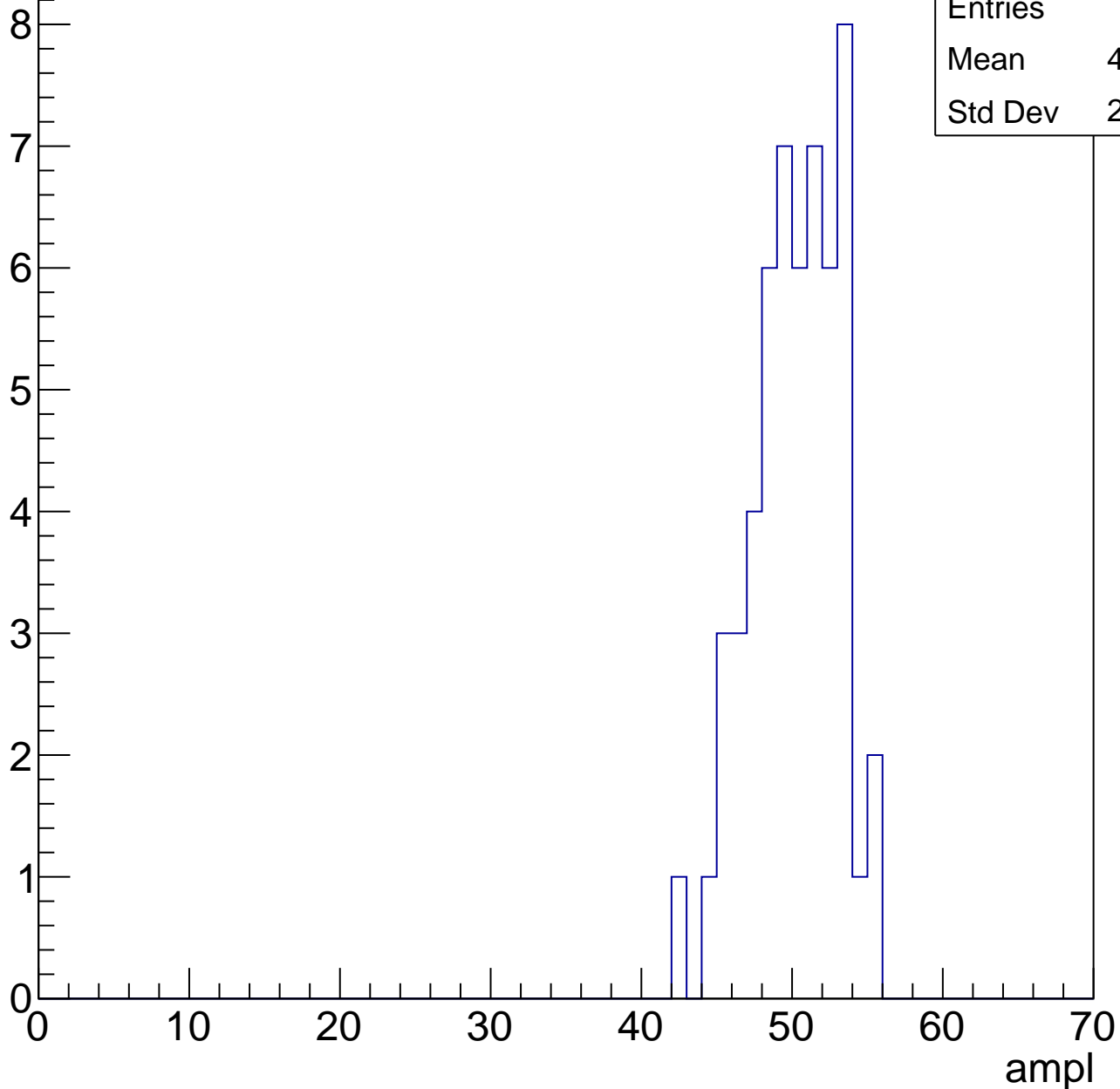


# B0L002S, U2-ch5, adc3

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	55
Mean	49.73
Std Dev	2.876

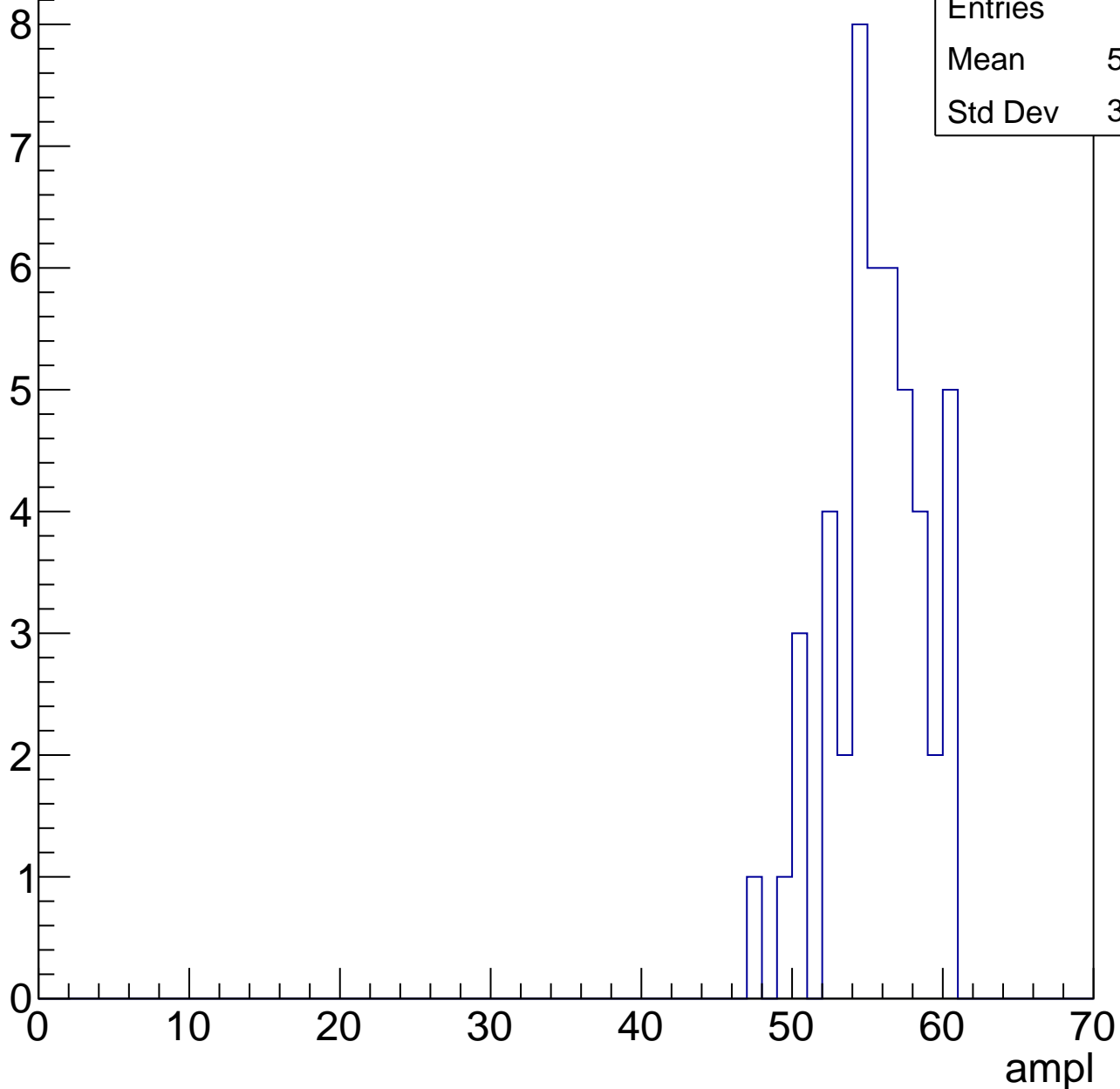


# B0L002S, U2-ch5, adc4

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

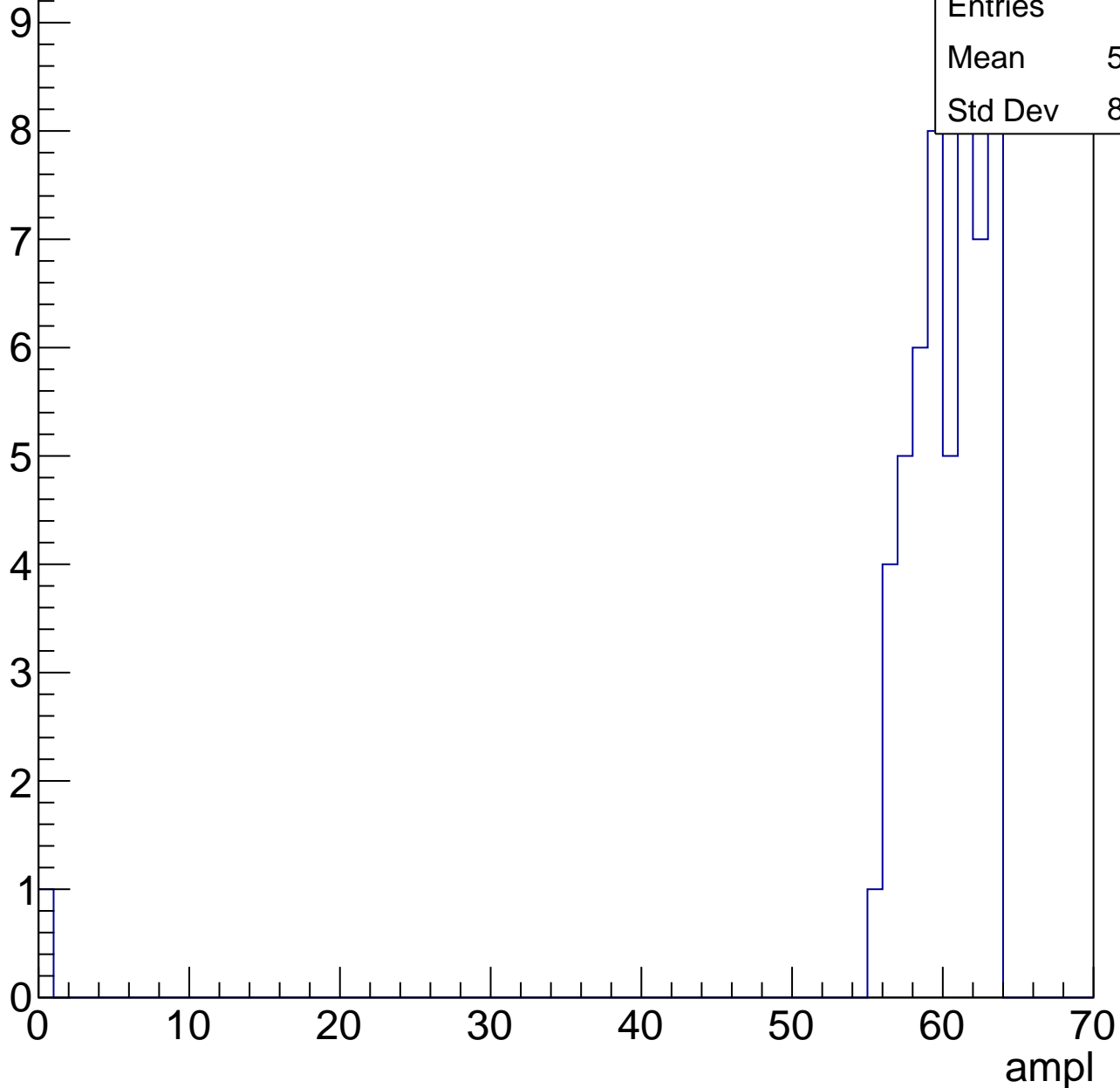
Entries	47
Mean	55.17
Std Dev	3.076



# B0L002S, U2-ch5, adc5

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



# B0L002S, U2-ch5, adc6

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry





# B0L002S, U2-ch5, adc7

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L002S, U2-ch6, adc0

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entries	64
Mean	31.94
Std Dev	3.056

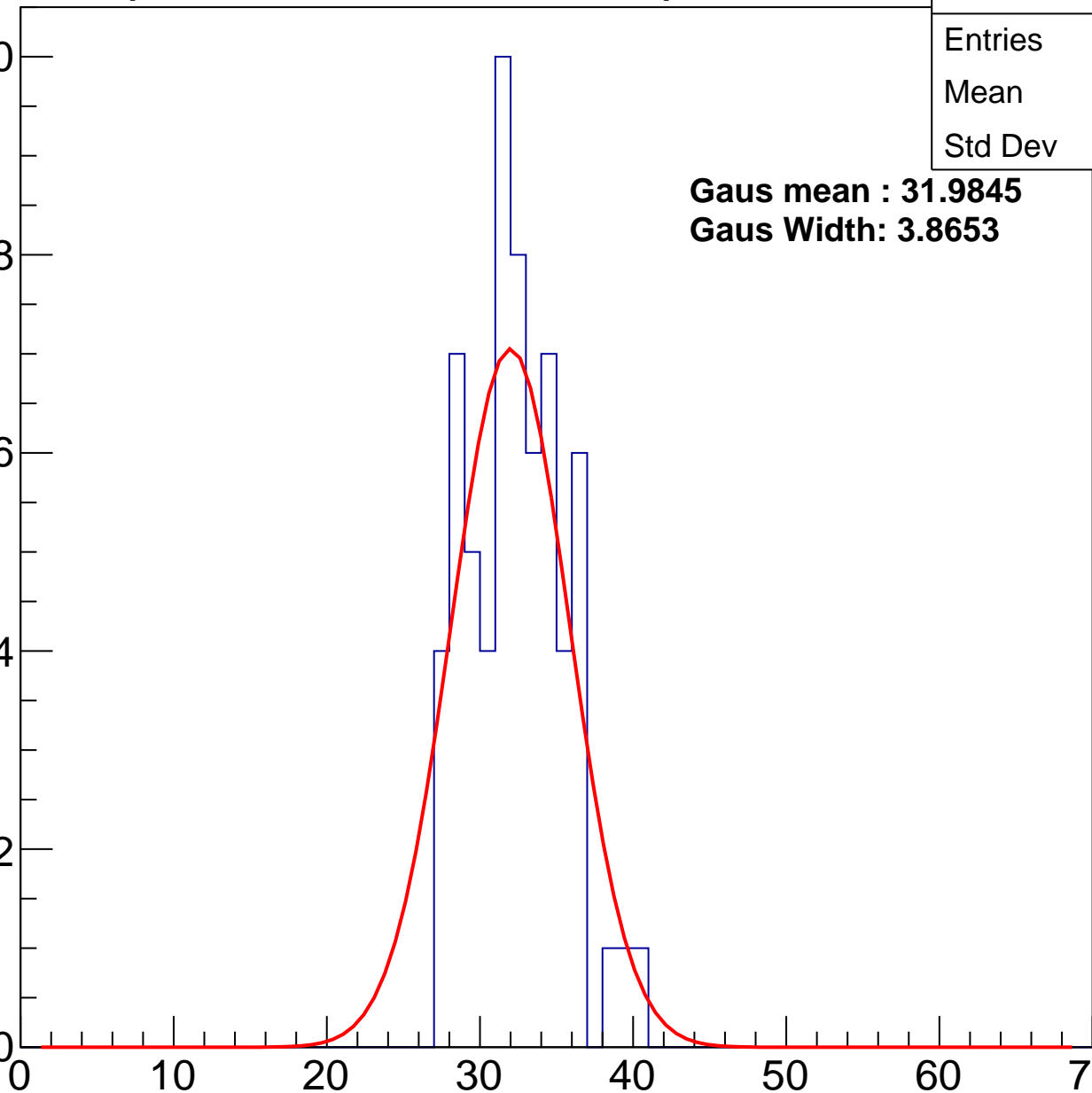
**Gaus mean : 31.9845**

**Gaus Width: 3.8653**

Entry

10  
8  
6  
4  
2  
0

ampl



# B0L002S, U2-ch6, adc1

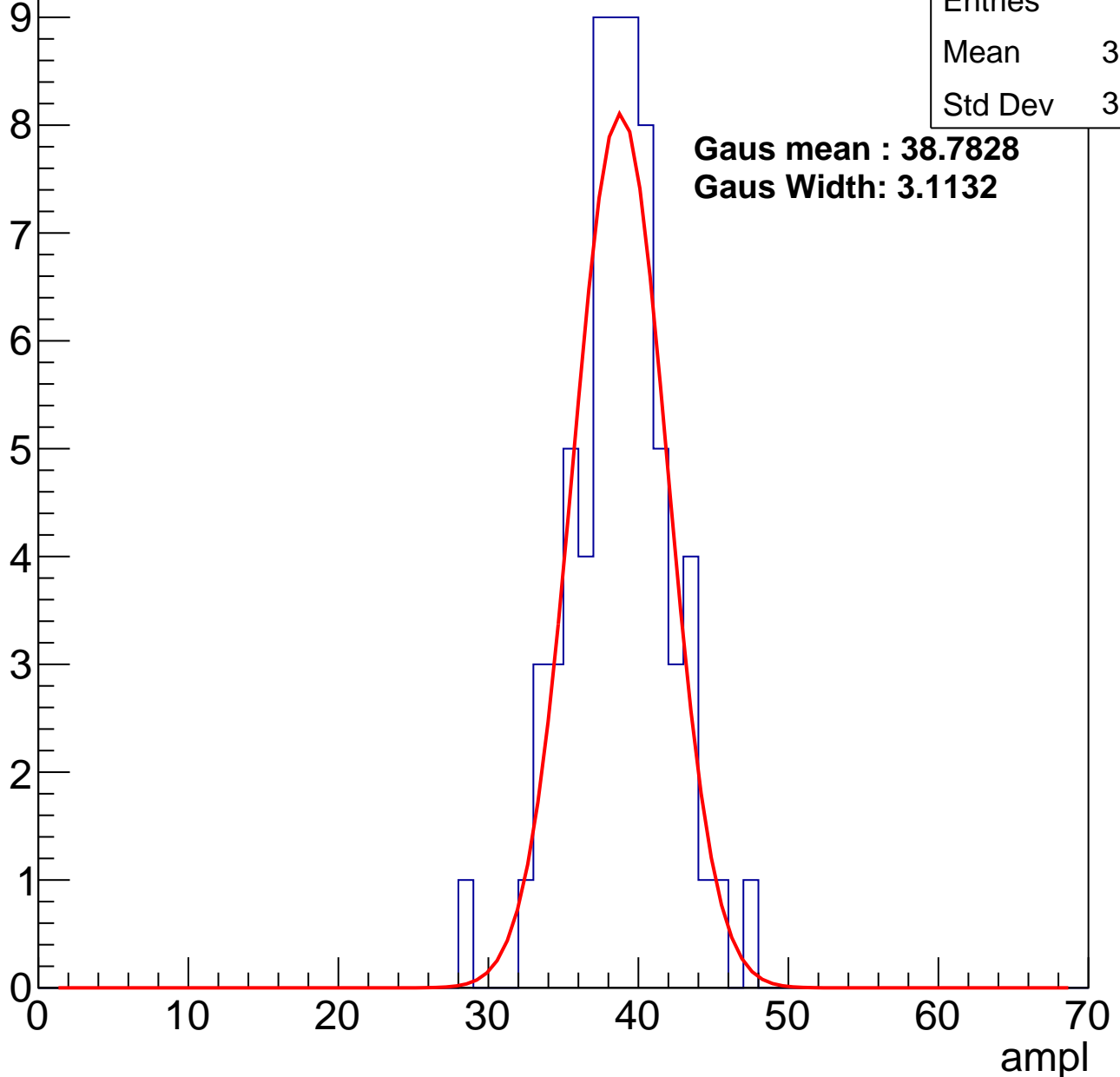
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	67
Mean	38.28
Std Dev	3.286

**Gaus mean : 38.7828**

**Gaus Width: 3.1132**



# B0L002S, U2-ch6, adc2

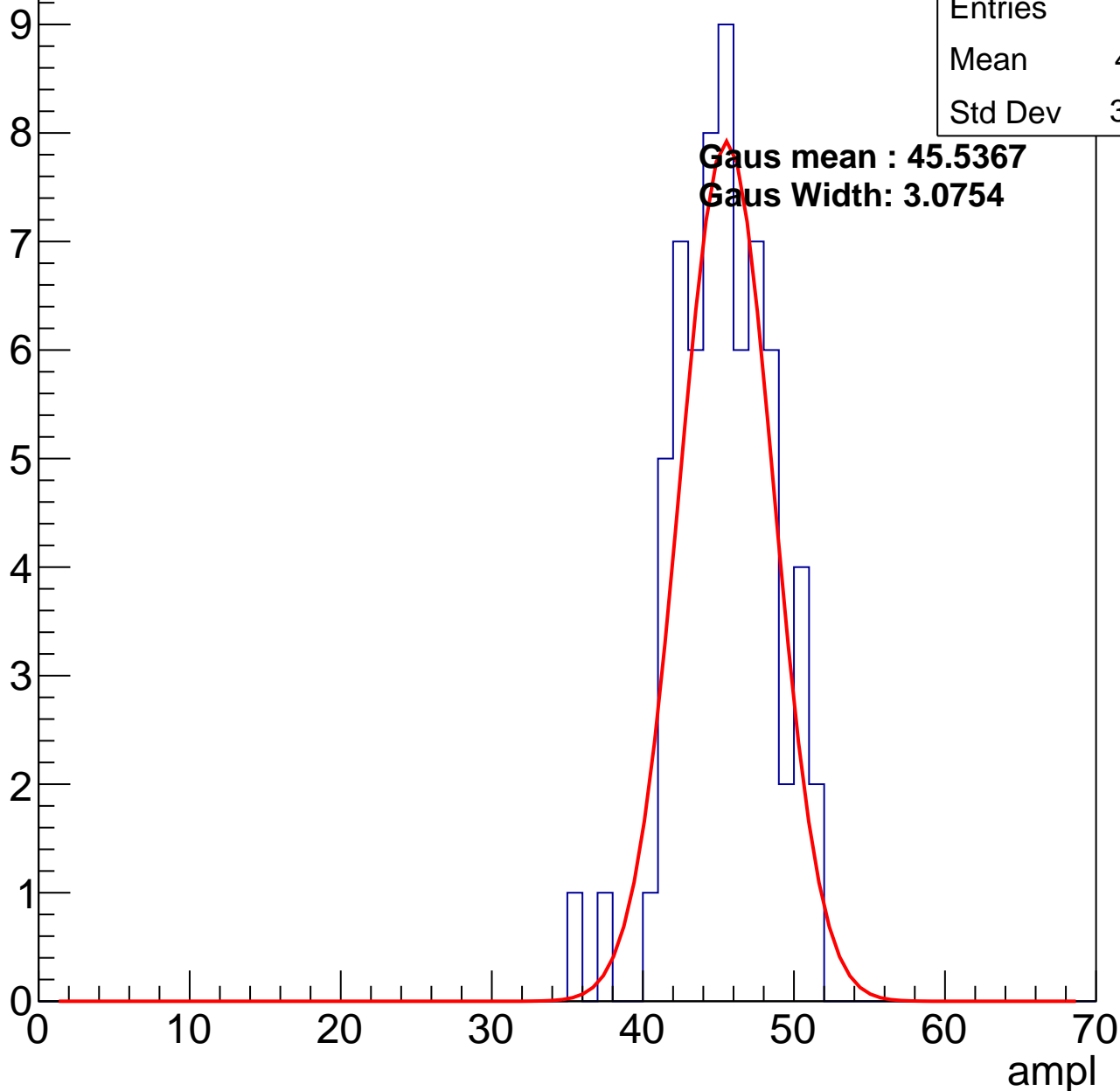
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	65
Mean	44.91
Std Dev	3.175

**Gaus mean : 45.5367**

**Gaus Width: 3.0754**

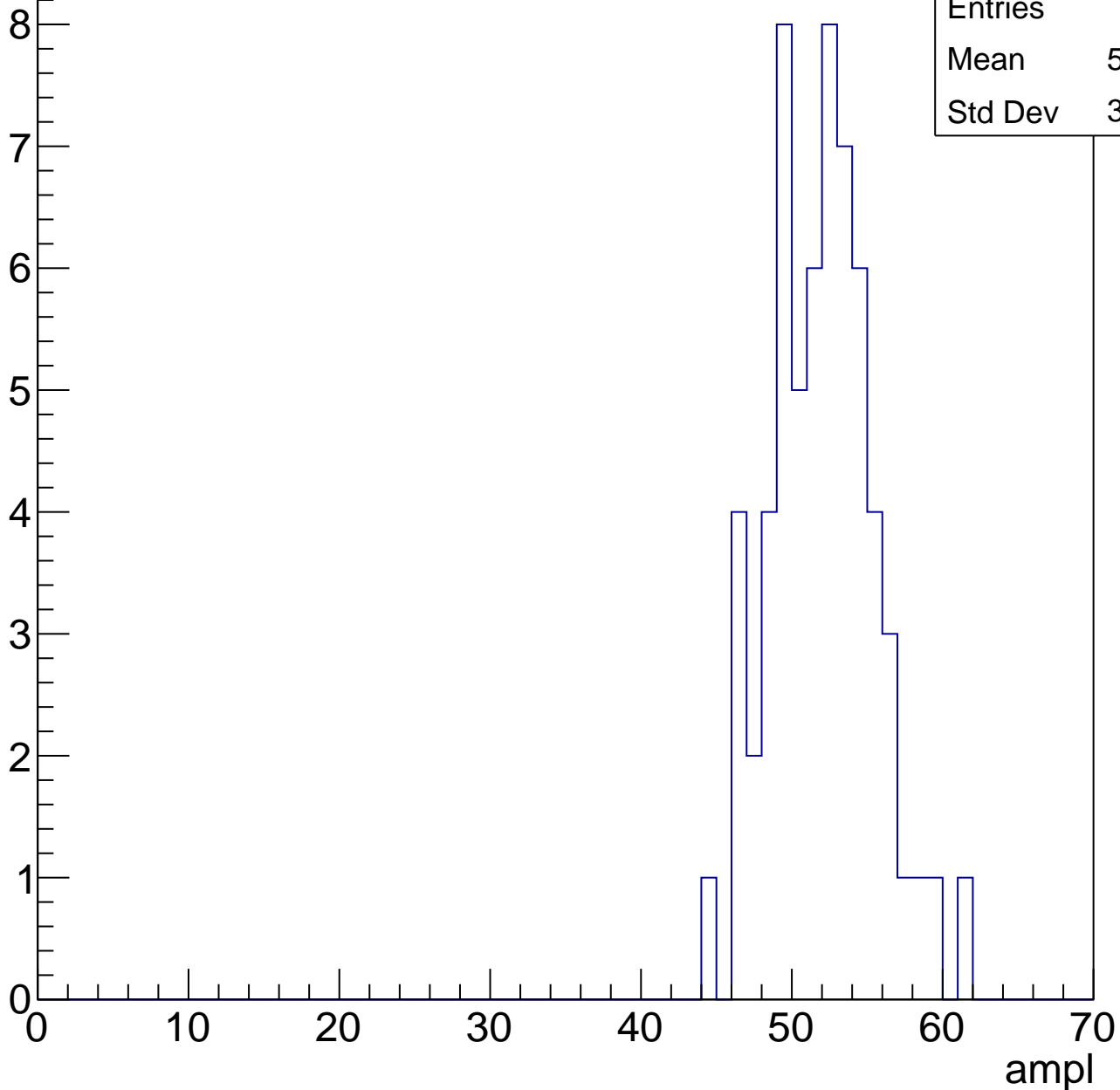


# B0L002S, U2-ch6, adc3

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	62
Mean	51.55
Std Dev	3.392



# B0L002S, U2-ch6, adc4

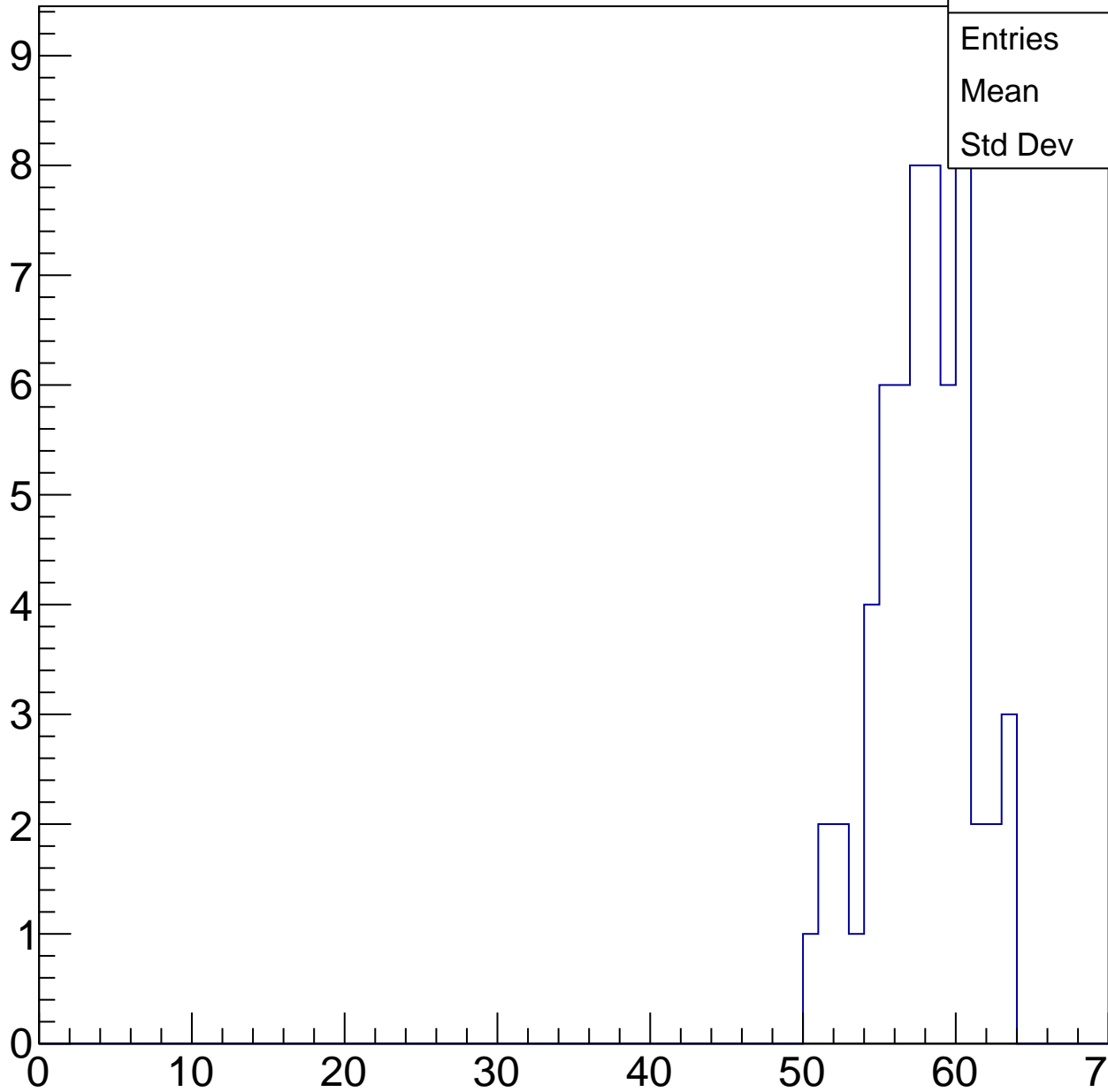
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	60
Mean	57.33
Std Dev	3.026

ampl

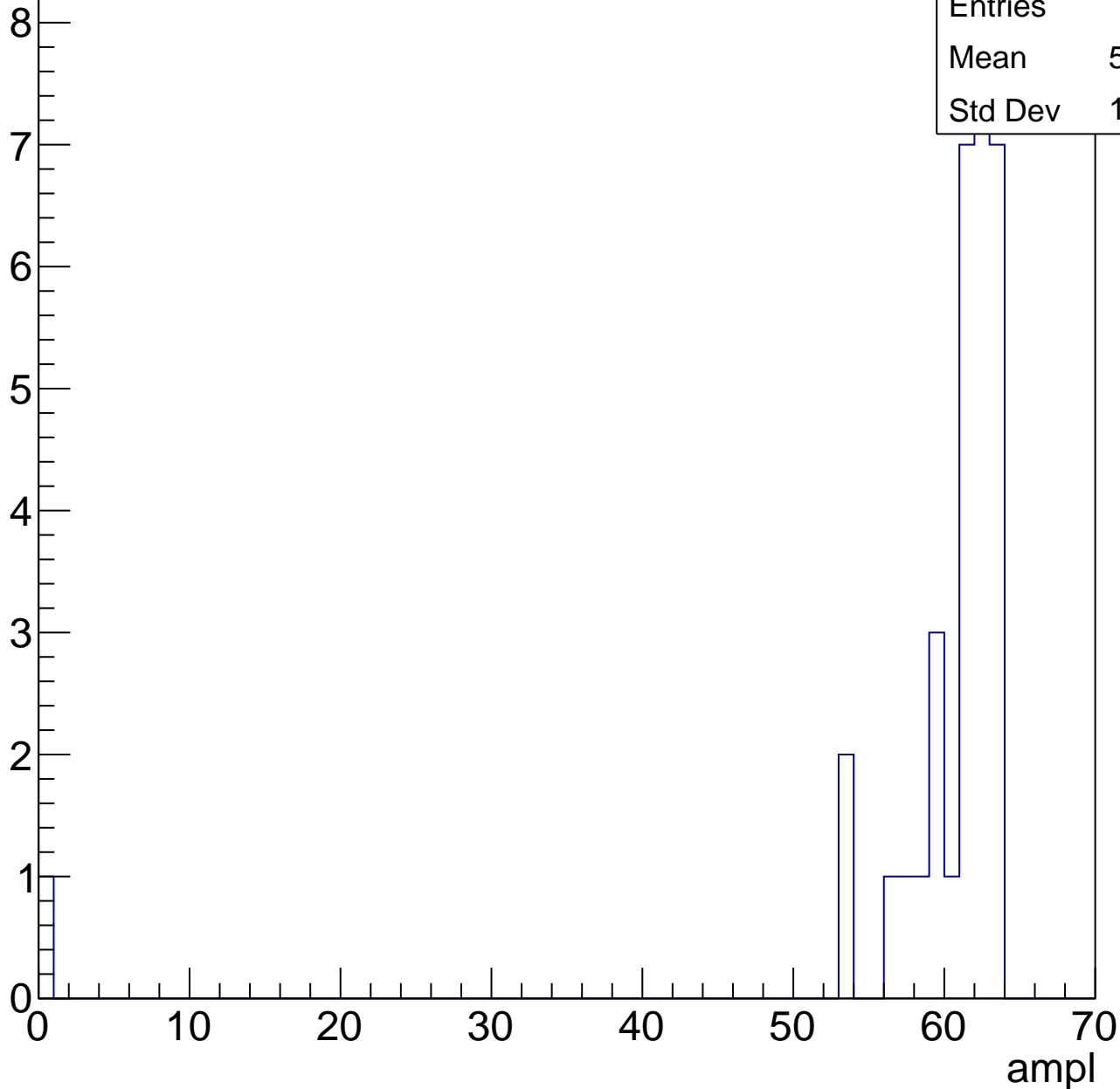


# B0L002S, U2-ch6, adc5

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	32
Mean	58.69
Std Dev	10.86



# B0L002S, U2-ch6, adc6

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



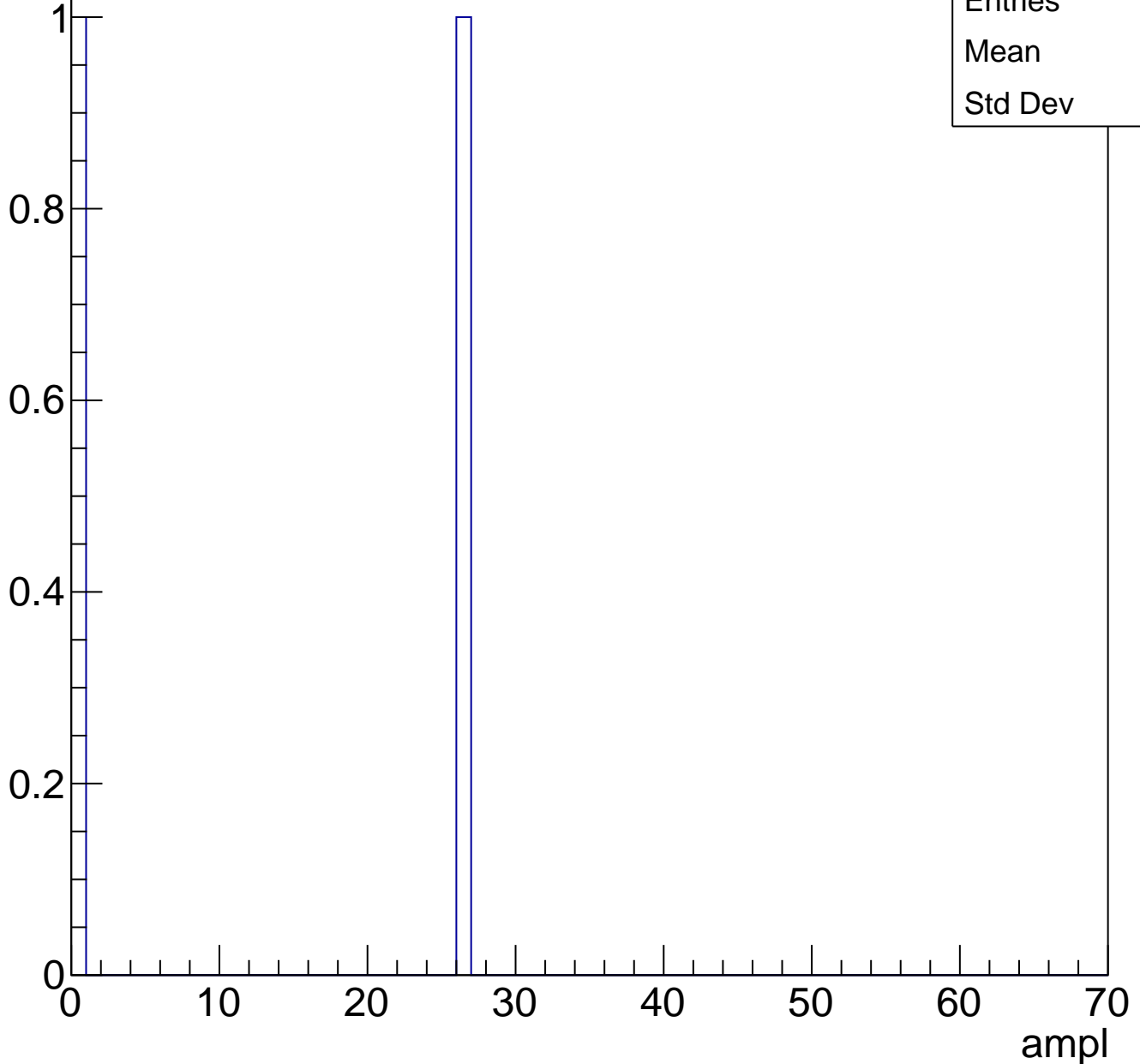
Entries	0
Mean	0
Std Dev	0



# B0L002S, U2-ch6, adc7

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



Entries	2
Mean	13
Std Dev	13

# B0L002S, U2-ch7, adc0

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entries	84
Mean	31.7
Std Dev	3.68

**Gaus mean : 32.3024**

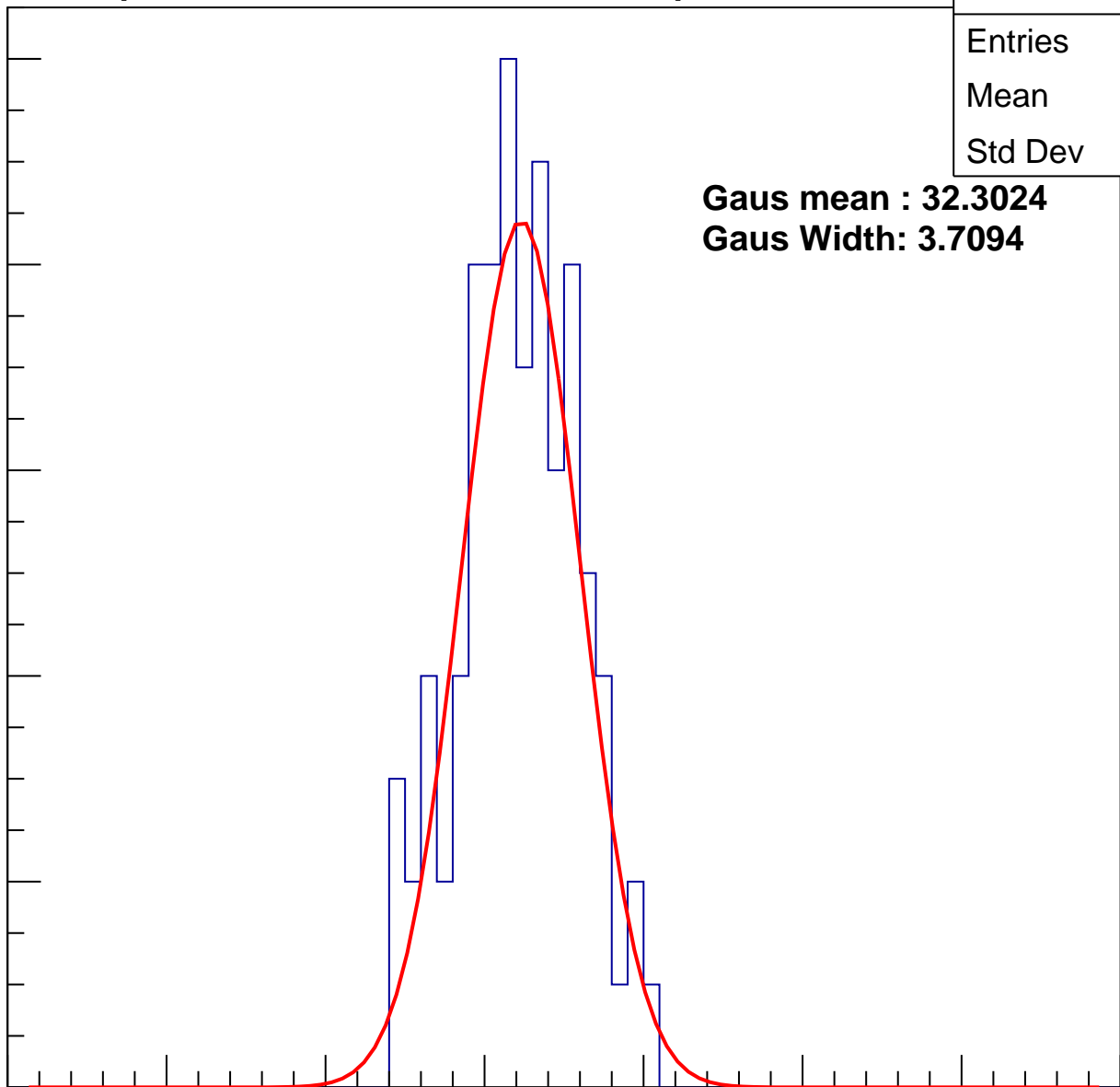
**Gaus Width: 3.7094**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L002S, U2-ch7, adc1

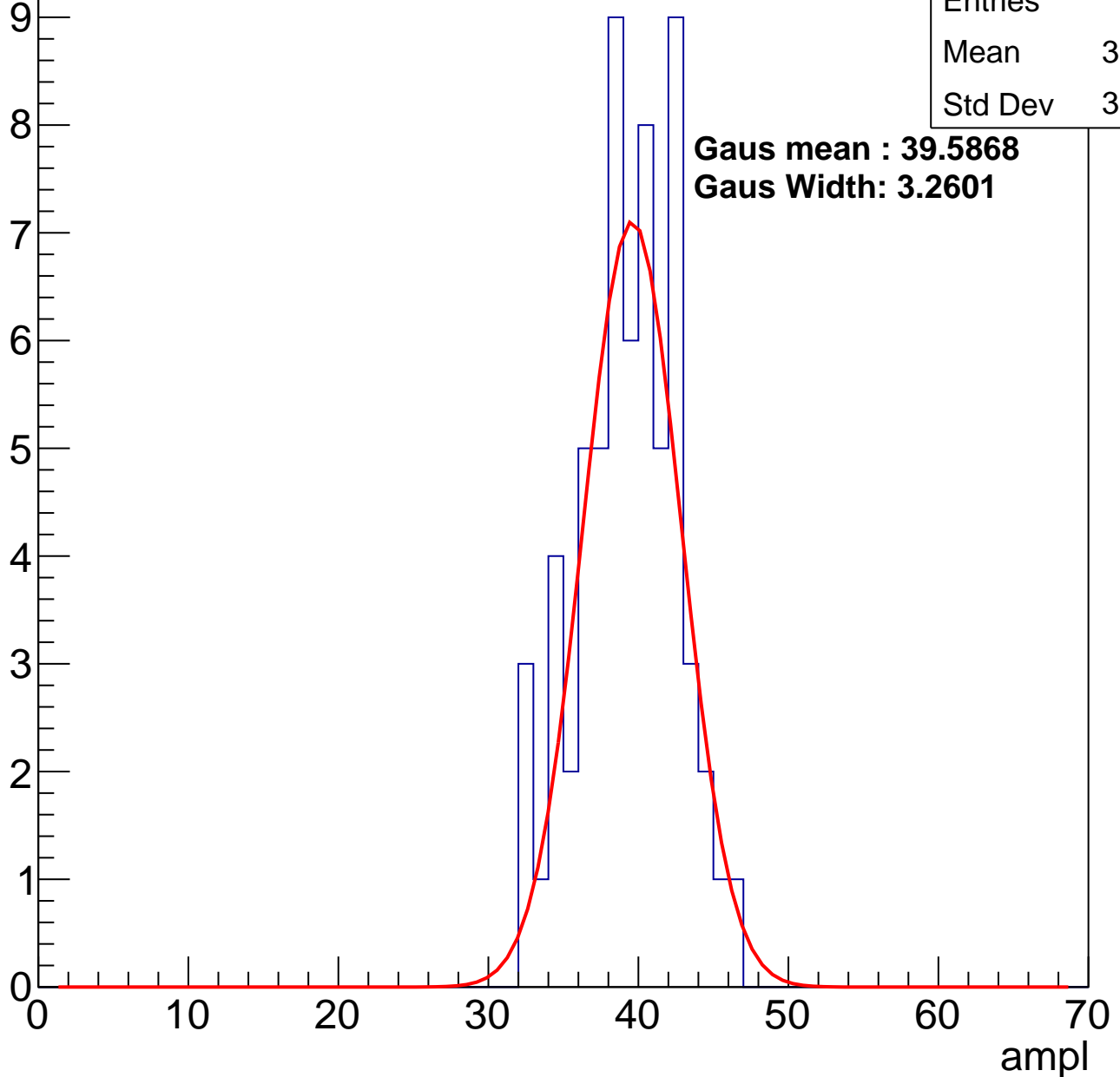
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	64
Mean	38.86
Std Dev	3.259

**Gaus mean : 39.5868**

**Gaus Width: 3.2601**



# B0L002S, U2-ch7, adc2

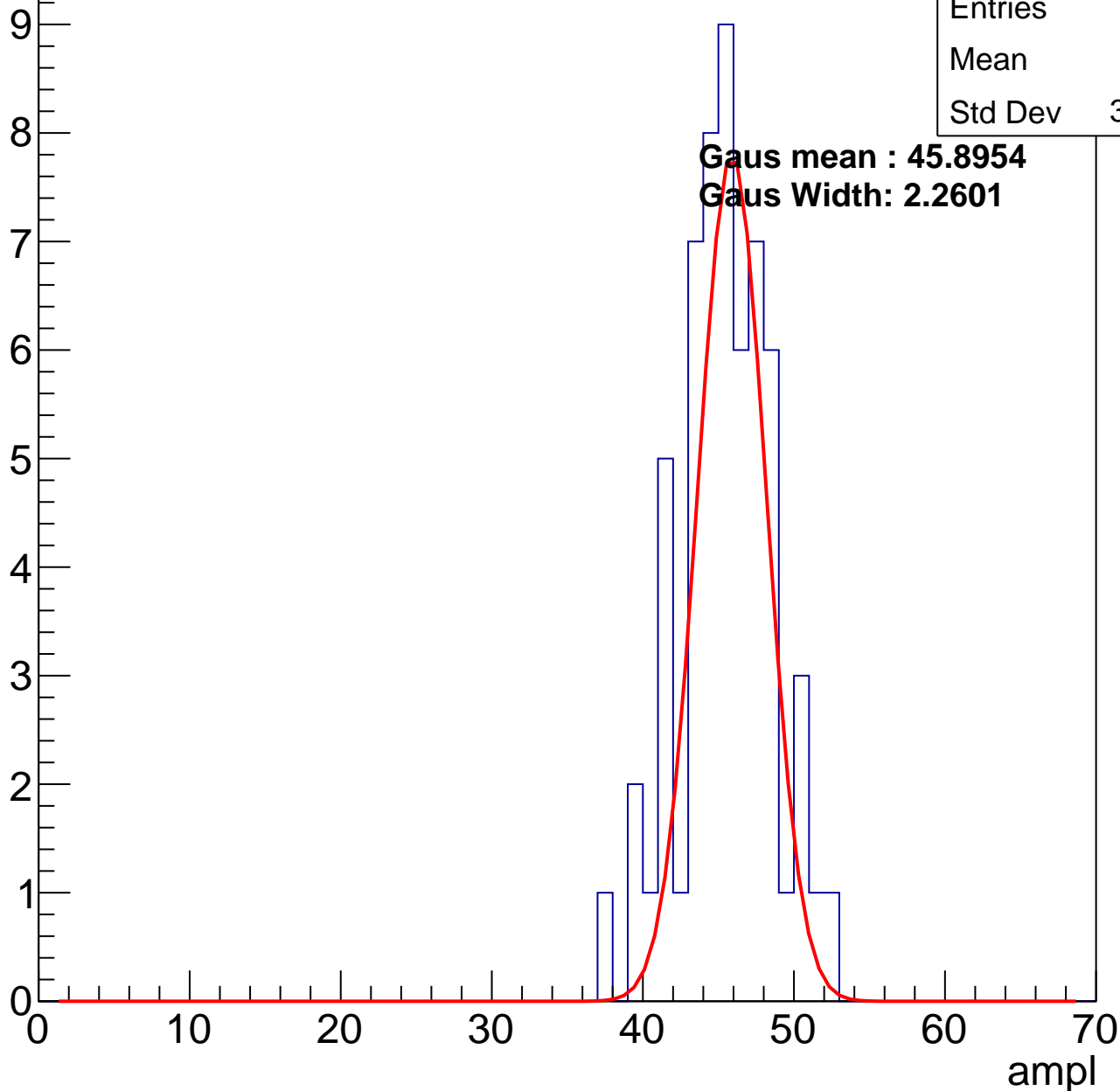
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	59
Mean	45
Std Dev	3.053

**Gaus mean : 45.8954**

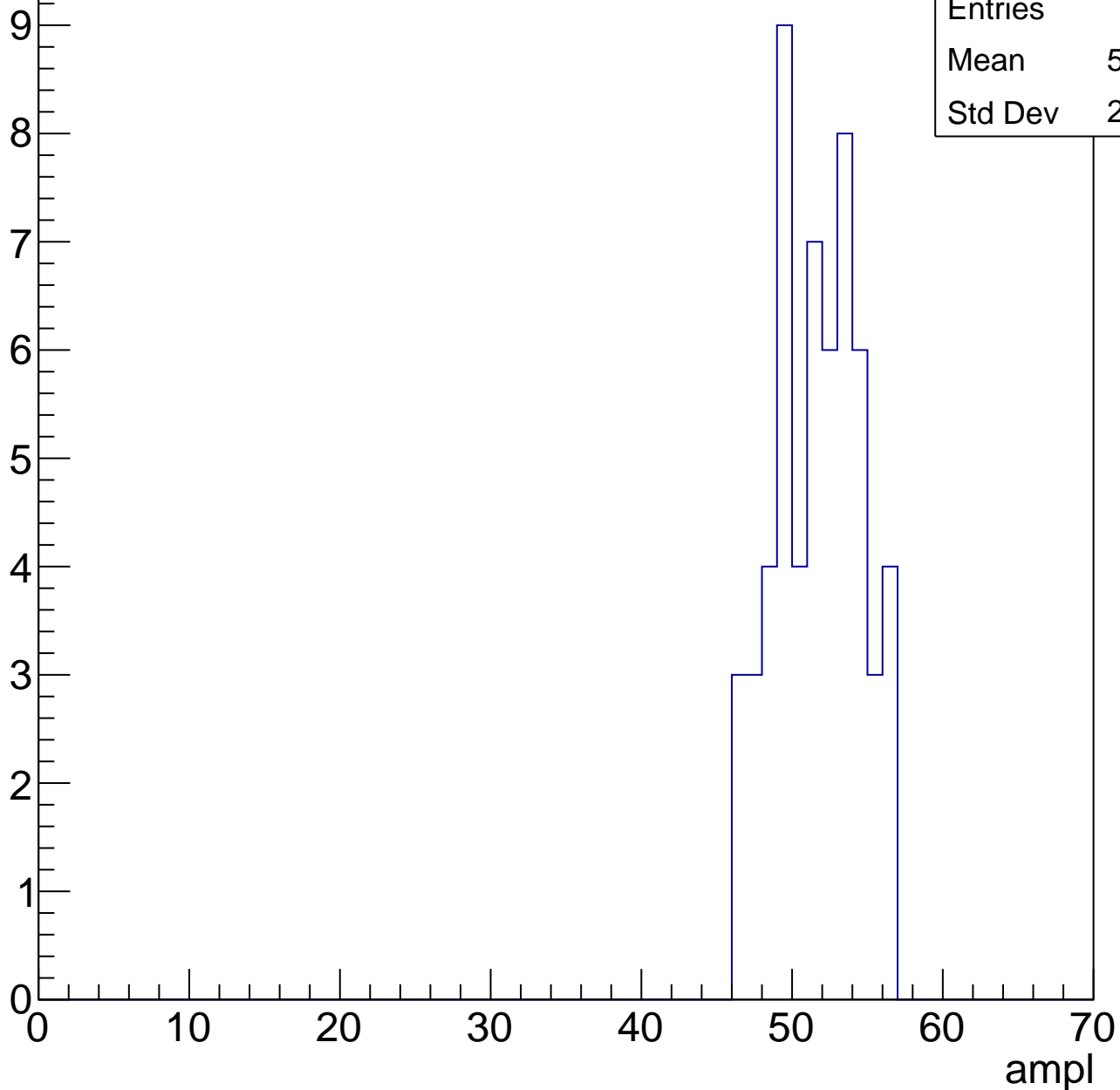
**Gaus Width: 2.2601**



# B0L002S, U2-ch7, adc3

calib\_packv5\_042523\_0143.root, FC#8, port C1

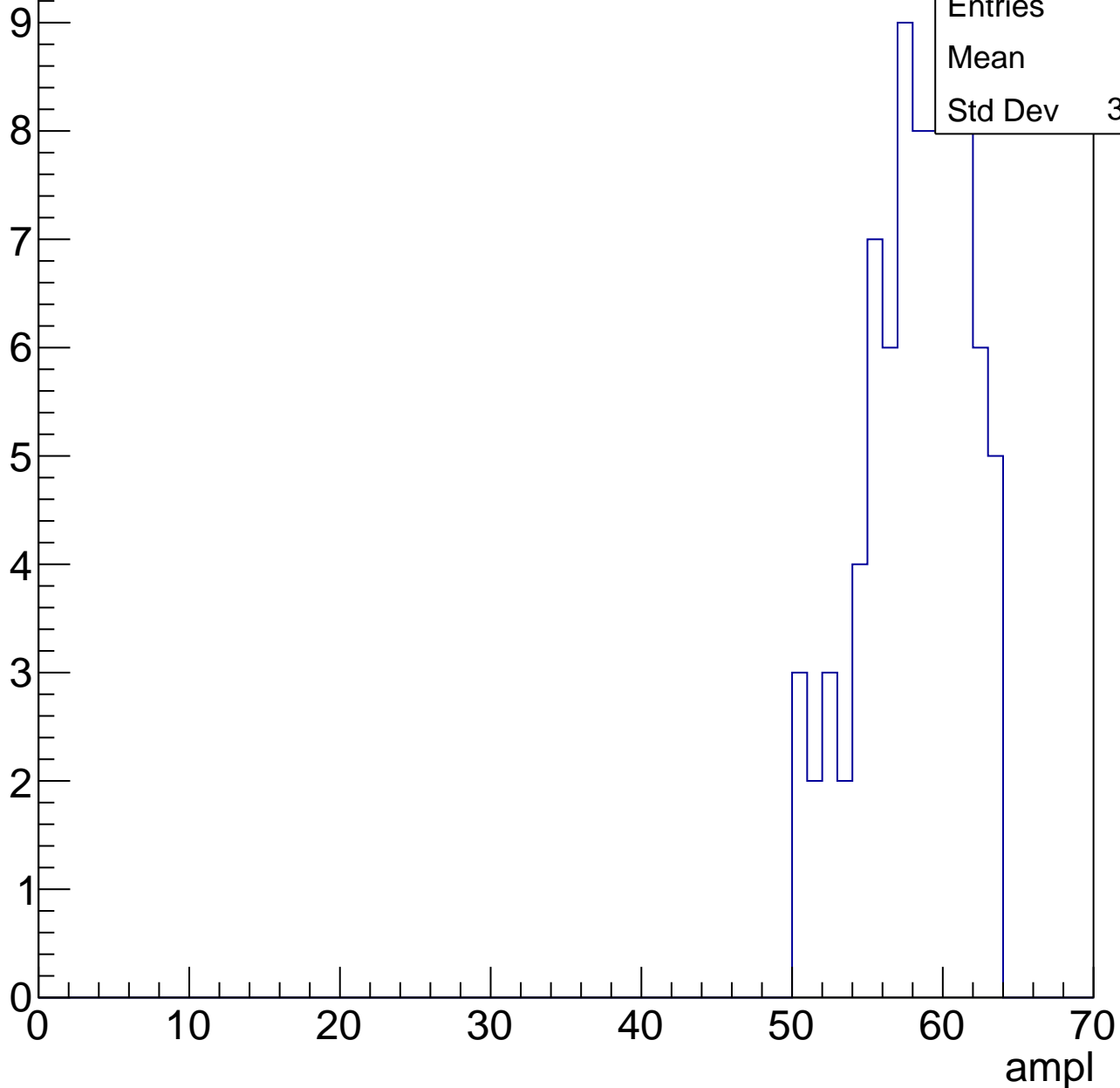
Entry



# B0L002S, U2-ch7, adc4

calib\_packv5\_042523\_0143.root, FC#8, port C1

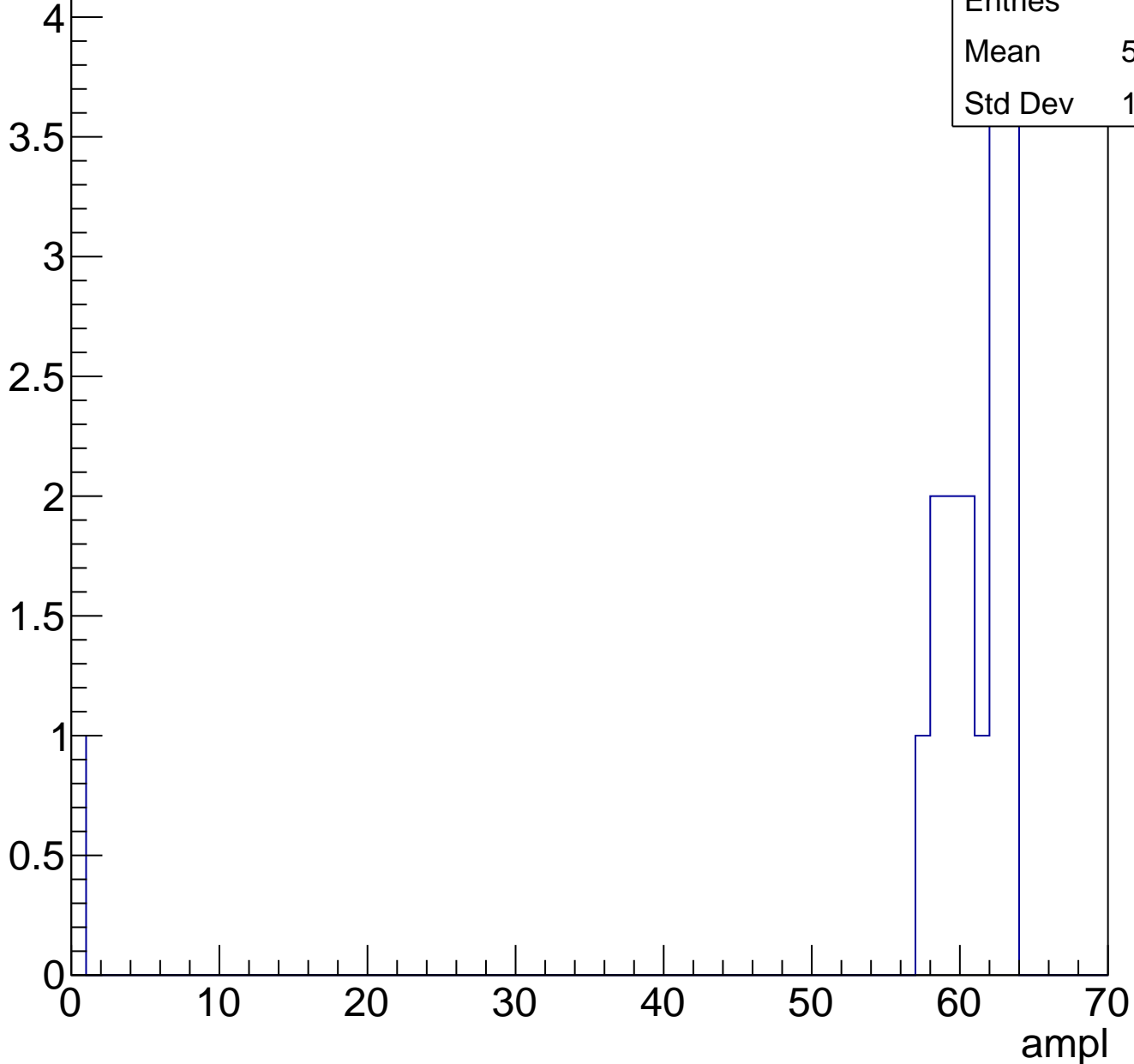
Entry



# B0L002S, U2-ch7, adc5

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



# B0L002S, U2-ch7, adc6

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

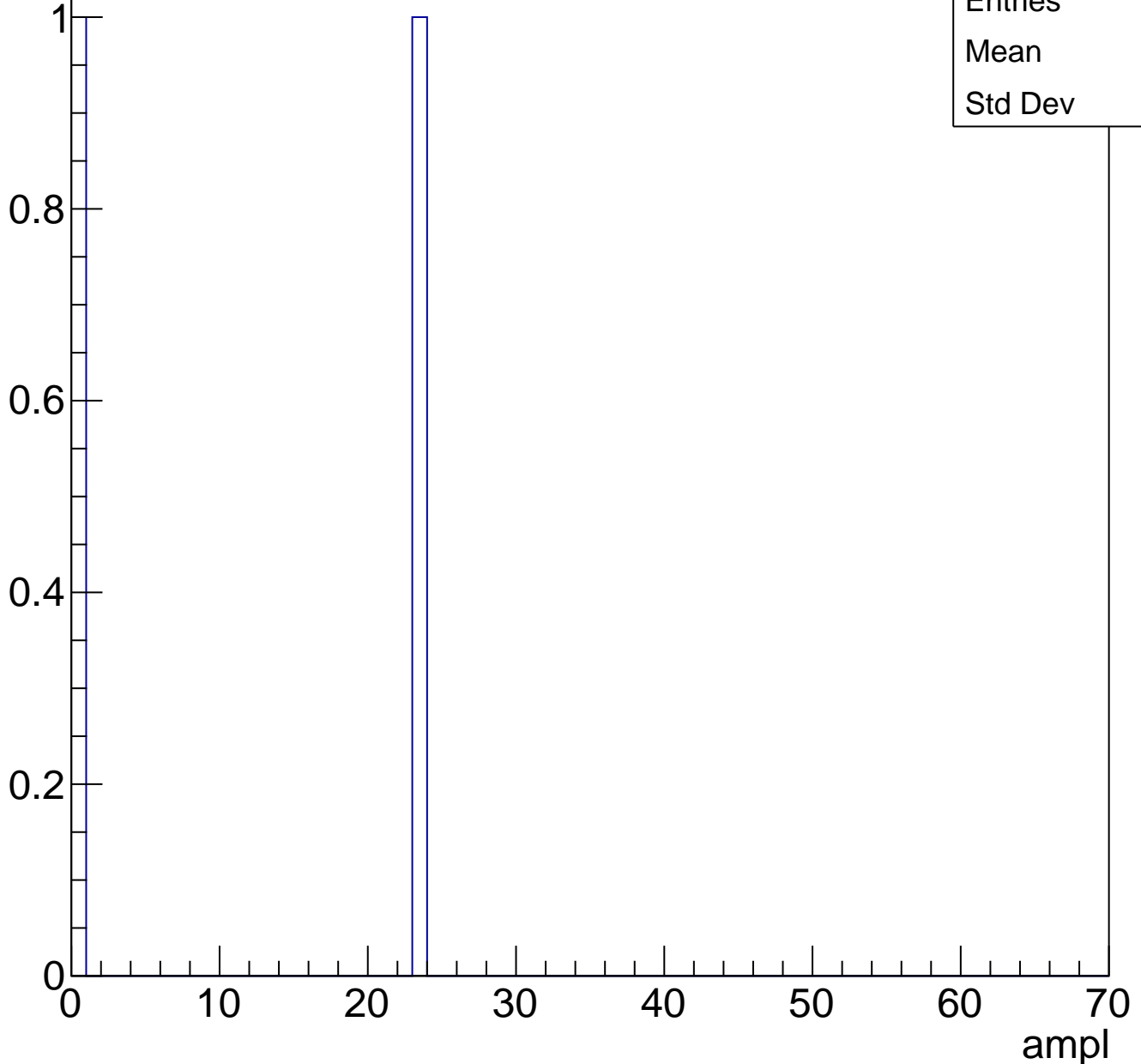




# B0L002S, U2-ch7, adc7

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



# B0L002S, U2-ch8, adc0

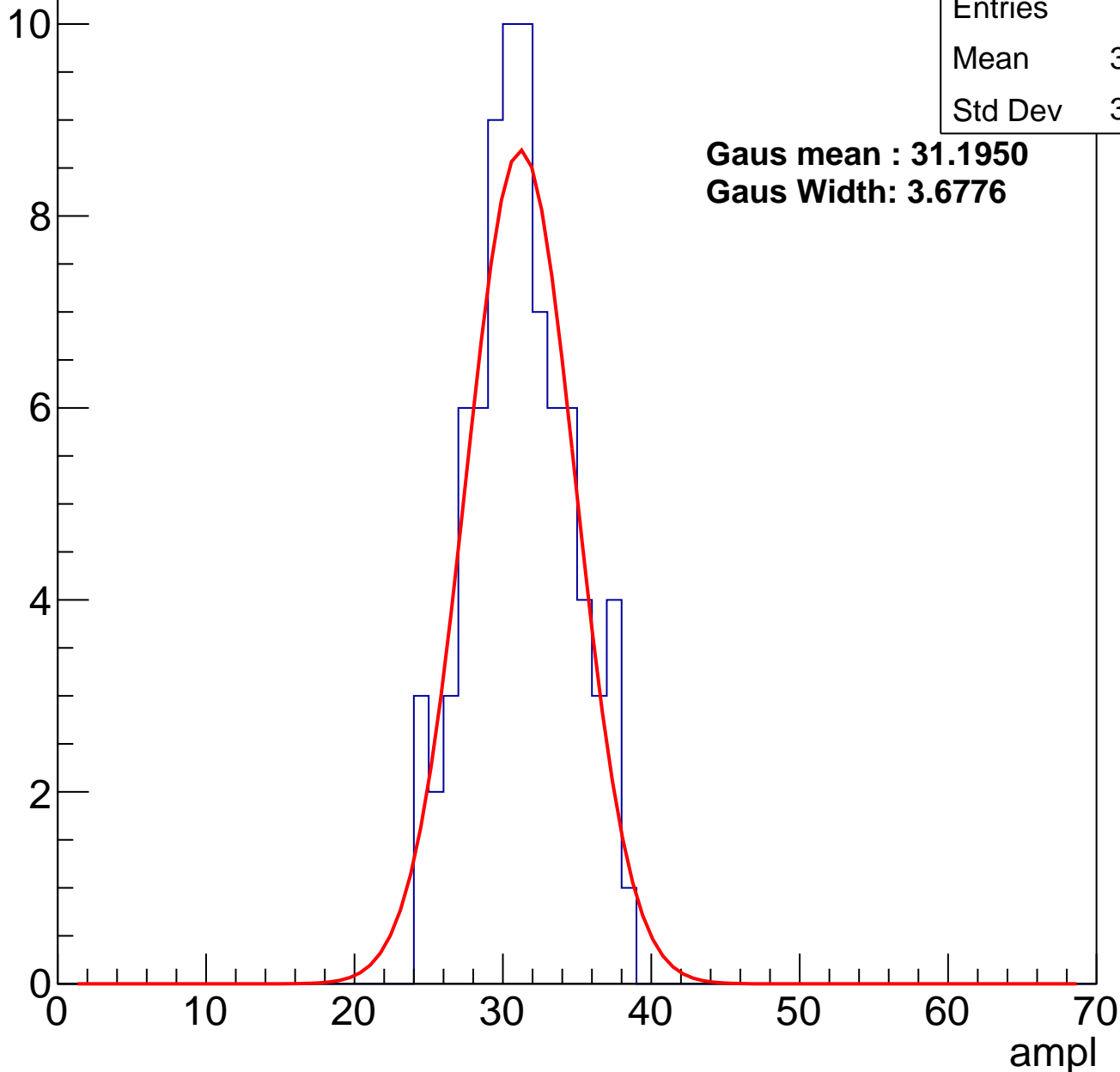
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entries	80
Mean	30.76
Std Dev	3.359

**Gaus mean : 31.1950**

**Gaus Width: 3.6776**

Entry

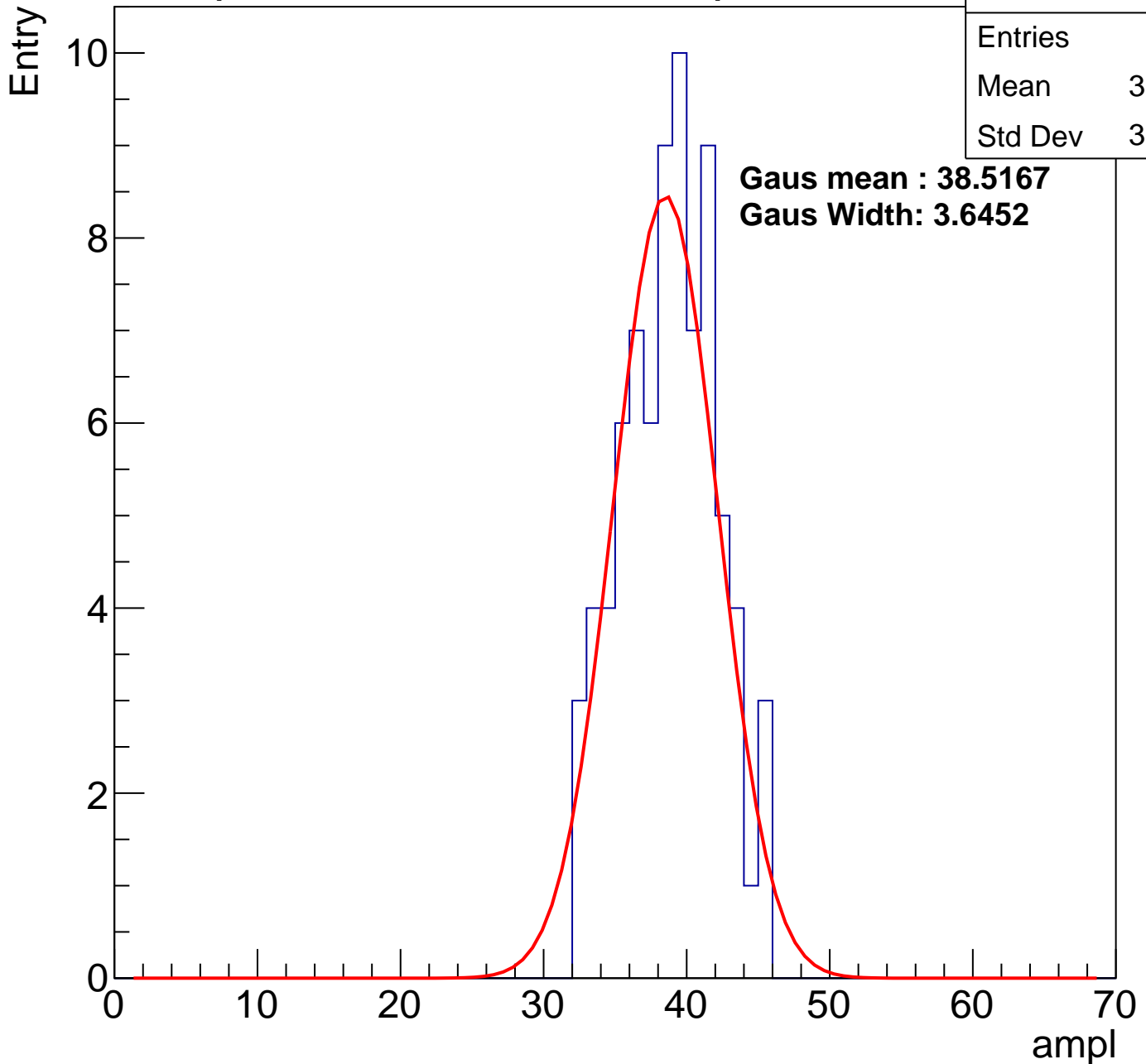


# B0L002S, U2-ch8, adc1

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entries	78
Mean	38.33
Std Dev	3.269

**Gaus mean : 38.5167**  
**Gaus Width: 3.6452**



# B0L002S, U2-ch8, adc2

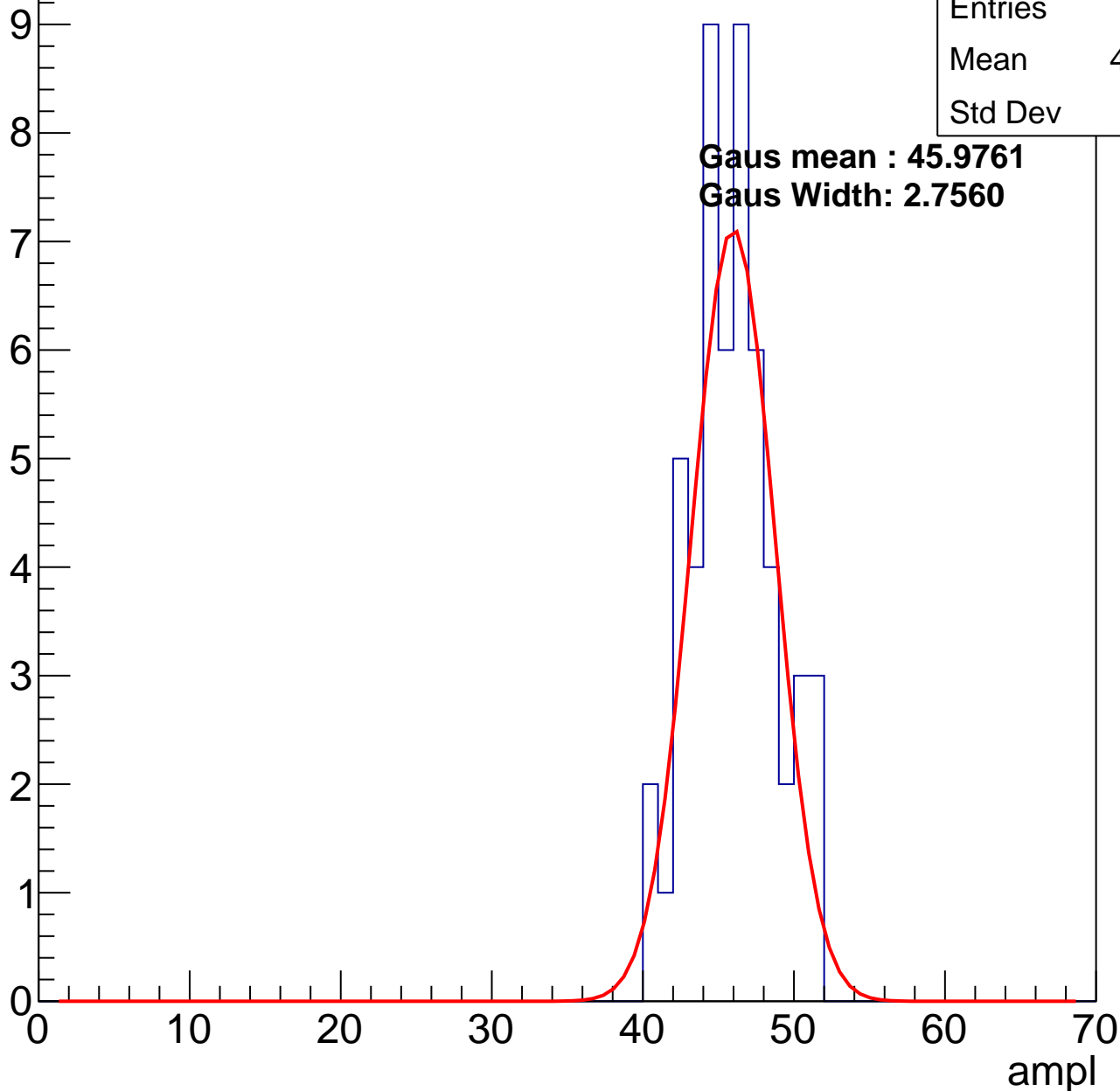
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	54
Mean	45.52
Std Dev	2.74

**Gaus mean : 45.9761**

**Gaus Width: 2.7560**

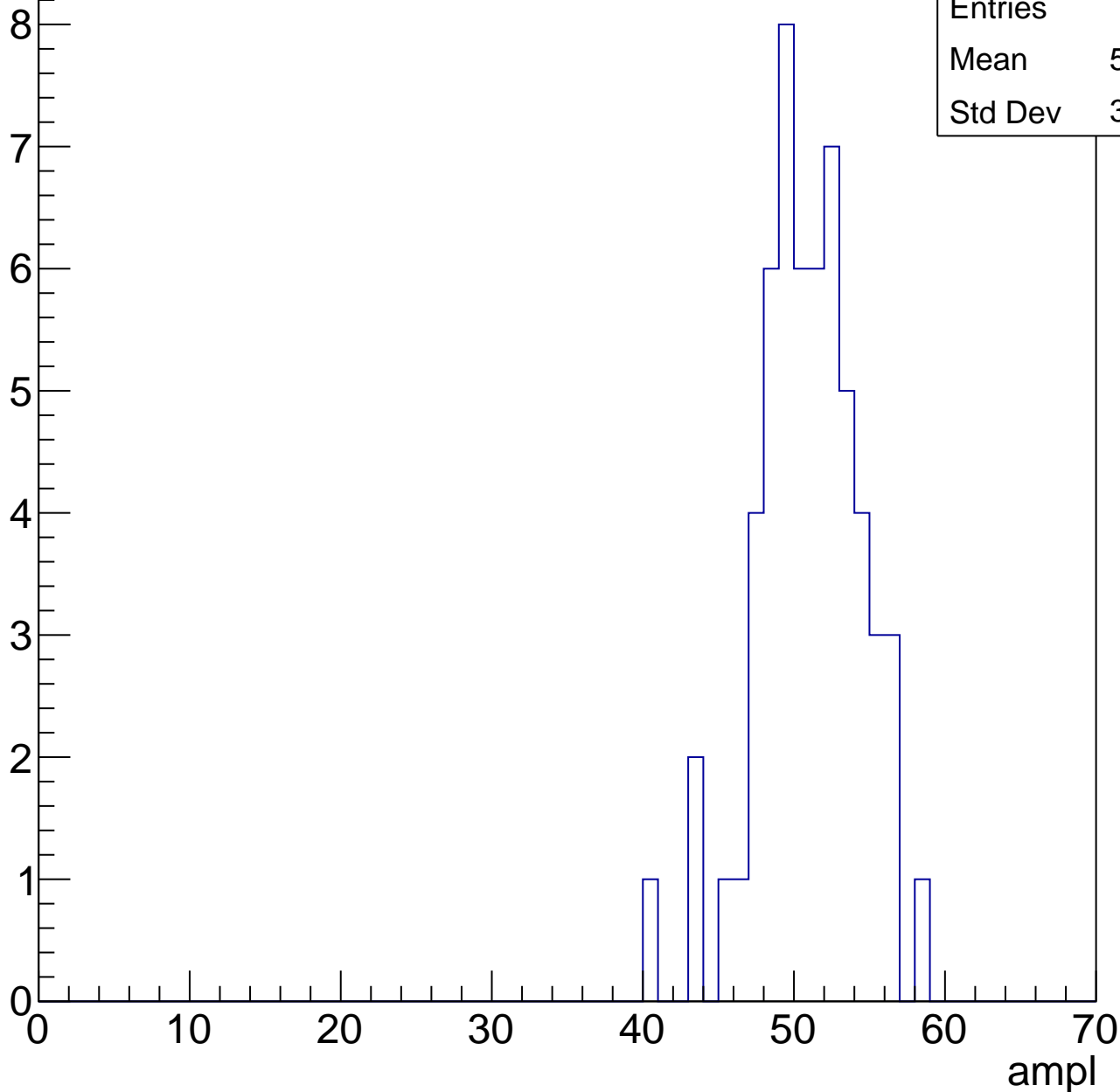


# B0L002S, U2-ch8, adc3

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	58
Mean	50.47
Std Dev	3.435

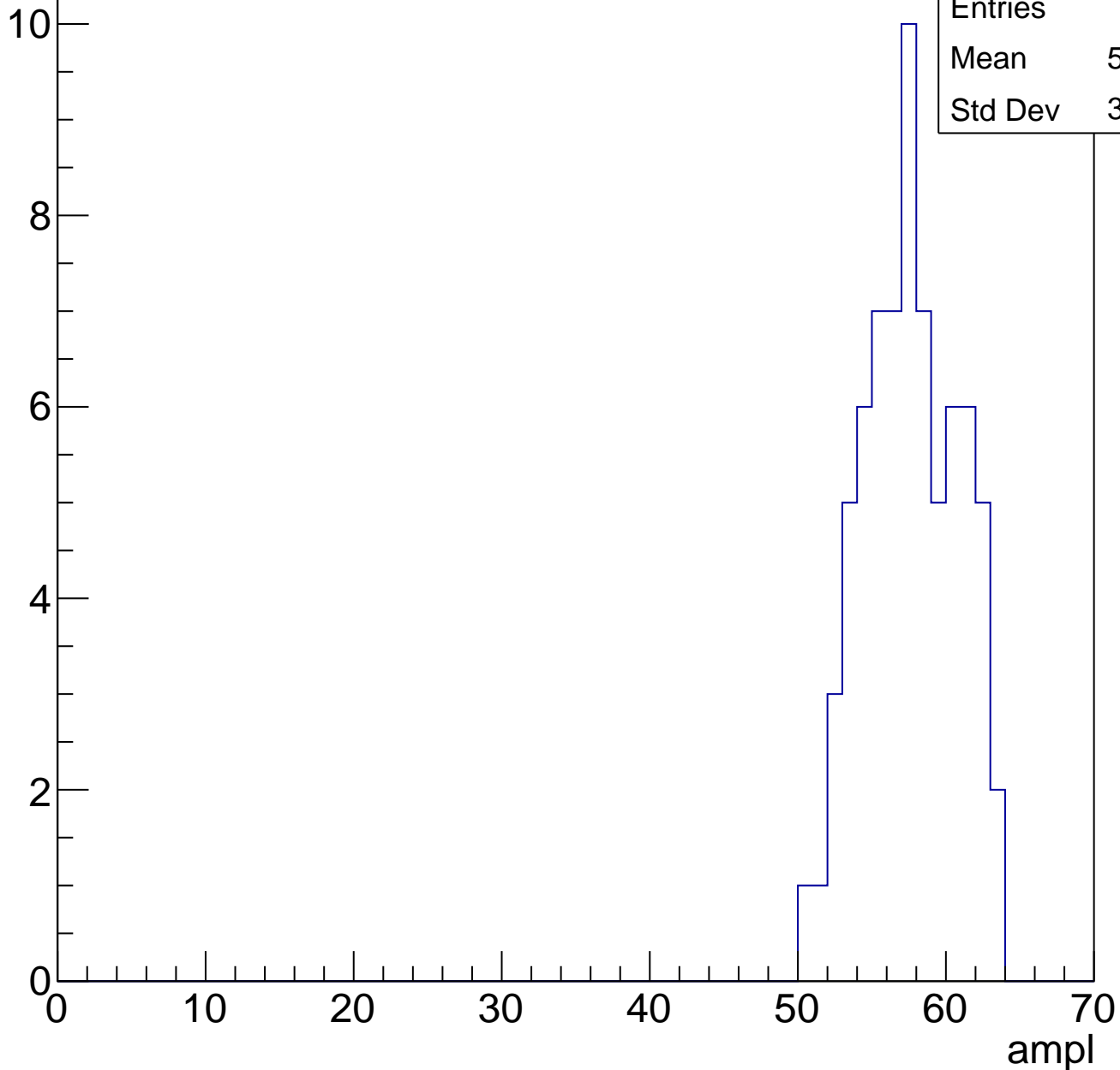


# B0L002S, U2-ch8, adc4

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entries	71
Mean	57.13
Std Dev	3.144

Entry

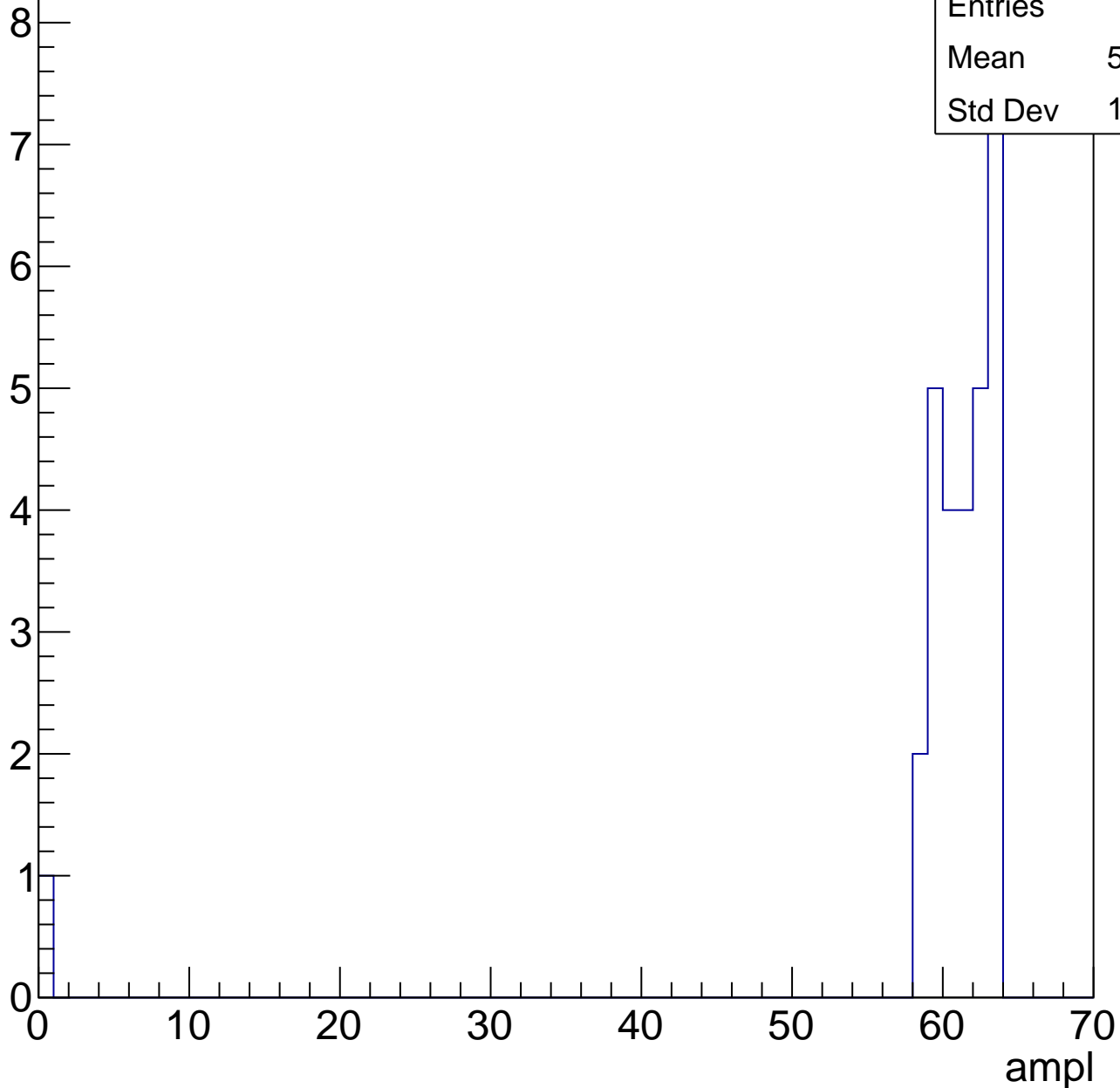


# B0L002S, U2-ch8, adc5

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	29
Mean	58.93
Std Dev	11.26



# B0L002S, U2-ch8, adc6

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



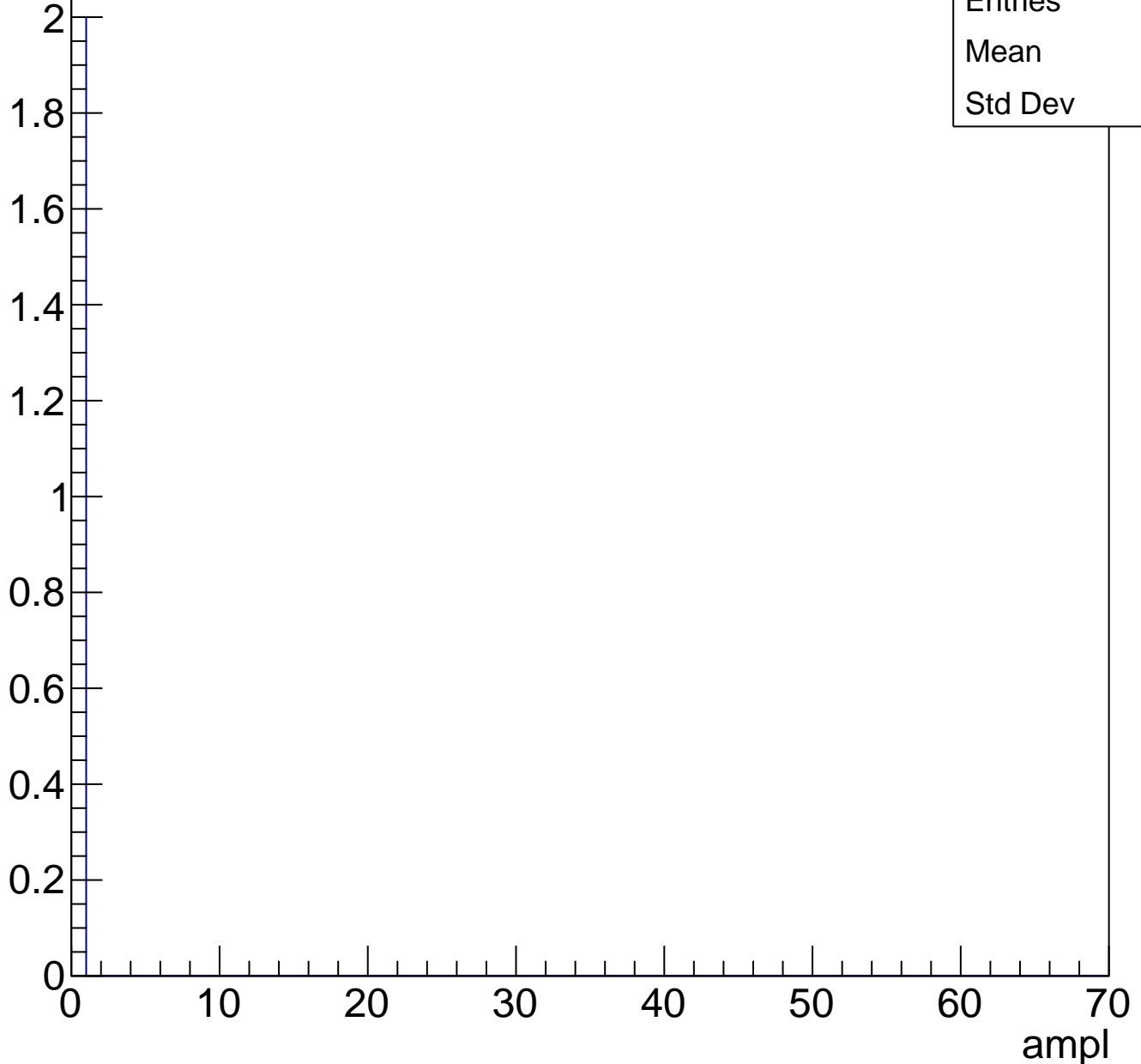
Entries	0
Mean	0
Std Dev	0



# B0L002S, U2-ch8, adc7

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



Entries	2
Mean	0
Std Dev	0

# B0L002S, U2-ch9, adc0

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entries	82
Mean	31.13
Std Dev	5.936

**Gaus mean : 32.2941**

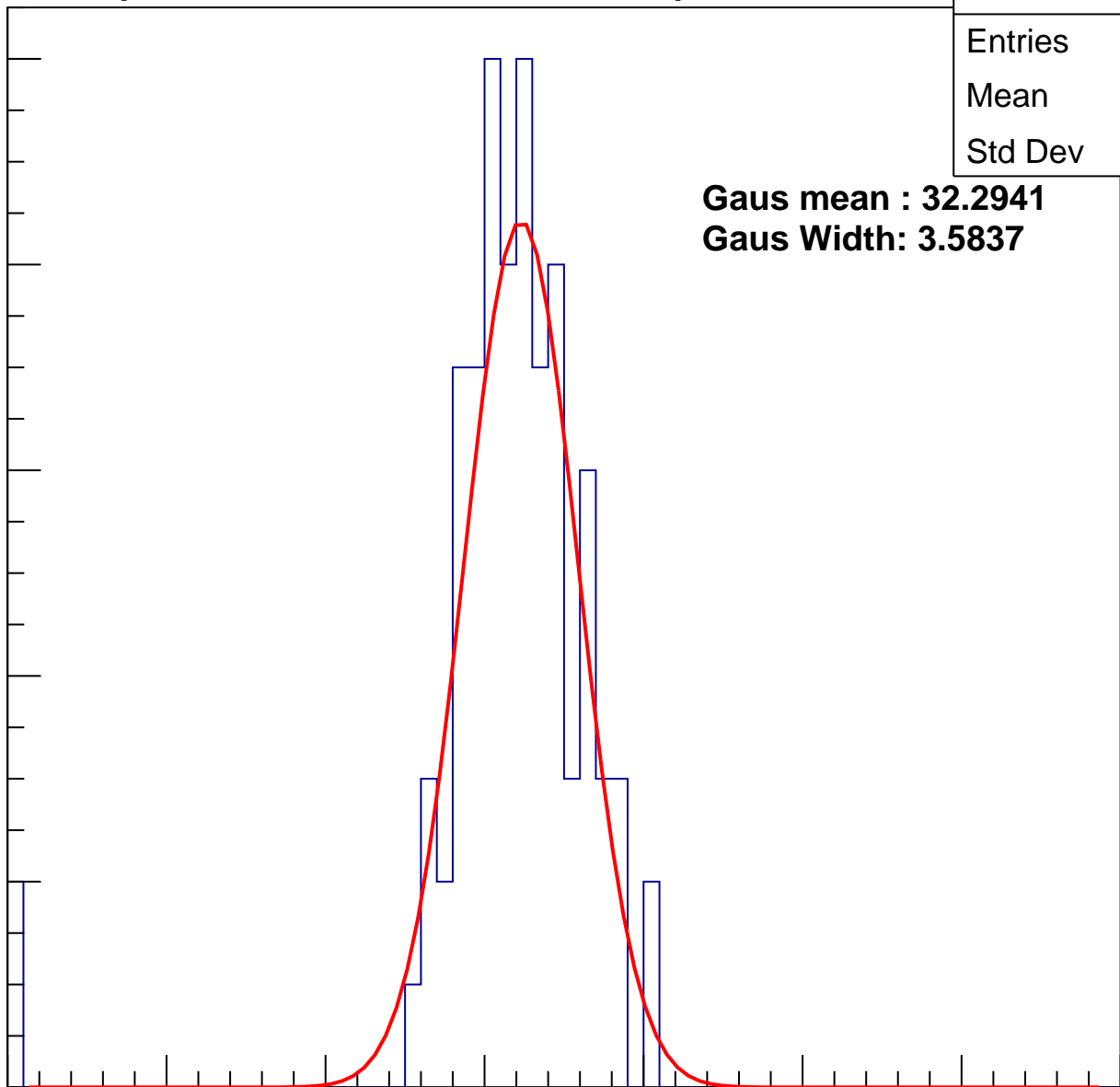
**Gaus Width: 3.5837**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



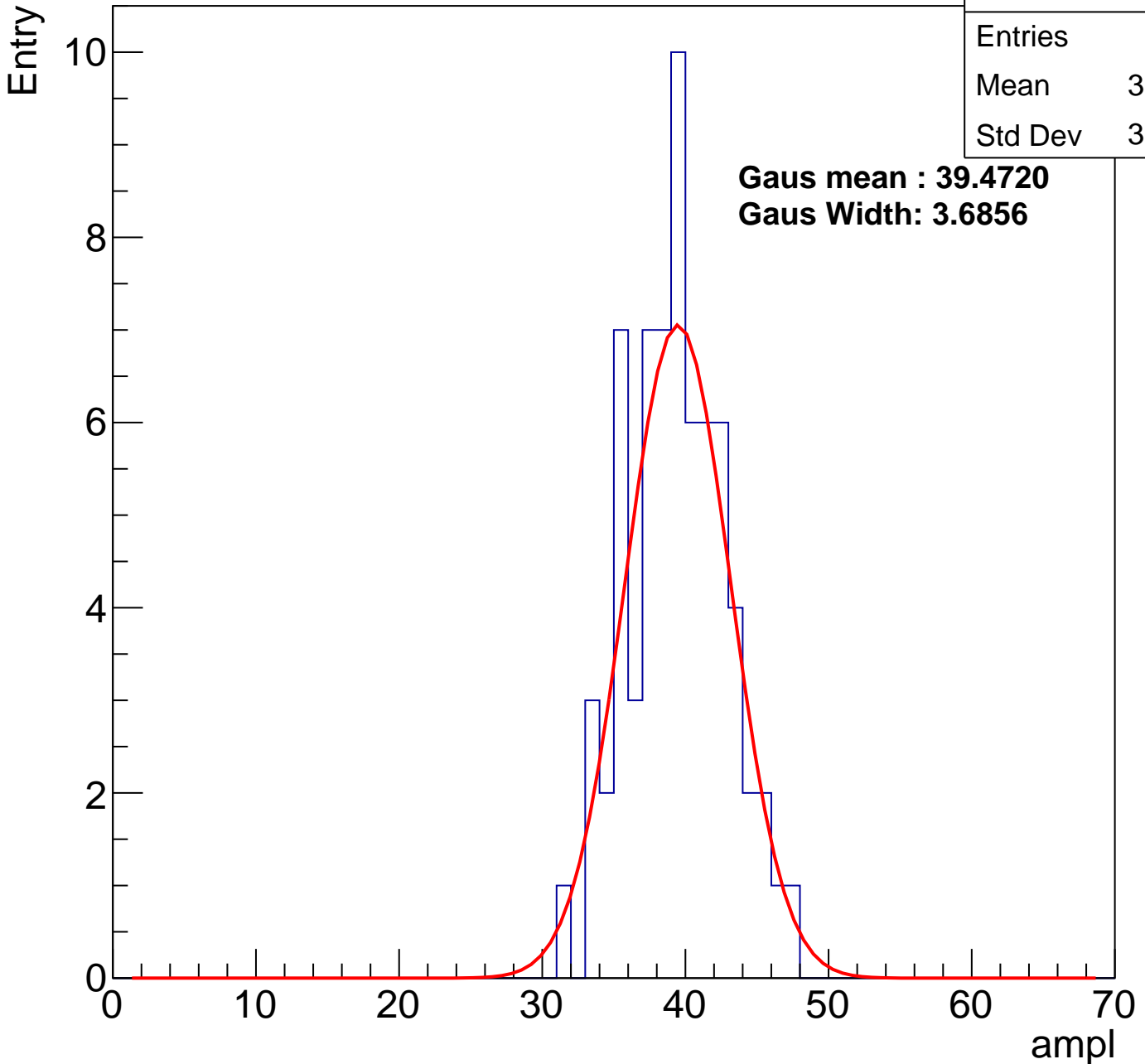
# B0L002S, U2-ch9, adc1

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entries	68
Mean	38.93
Std Dev	3.384

**Gaus mean : 39.4720**

**Gaus Width: 3.6856**



# B0L002S, U2-ch9, adc2

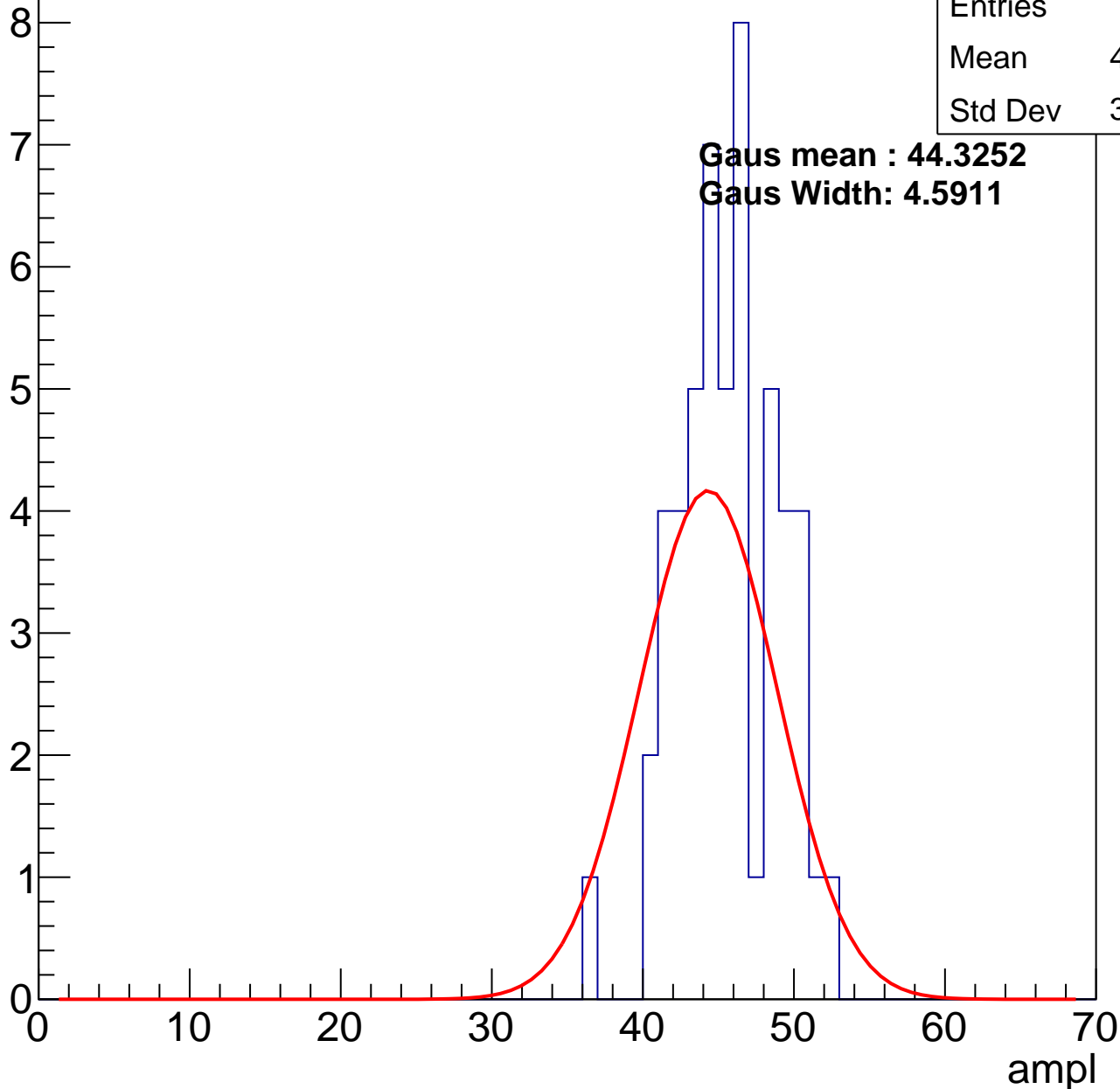
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	52
Mean	45.19
Std Dev	3.288

**Gaus mean : 44.3252**

**Gaus Width: 4.5911**

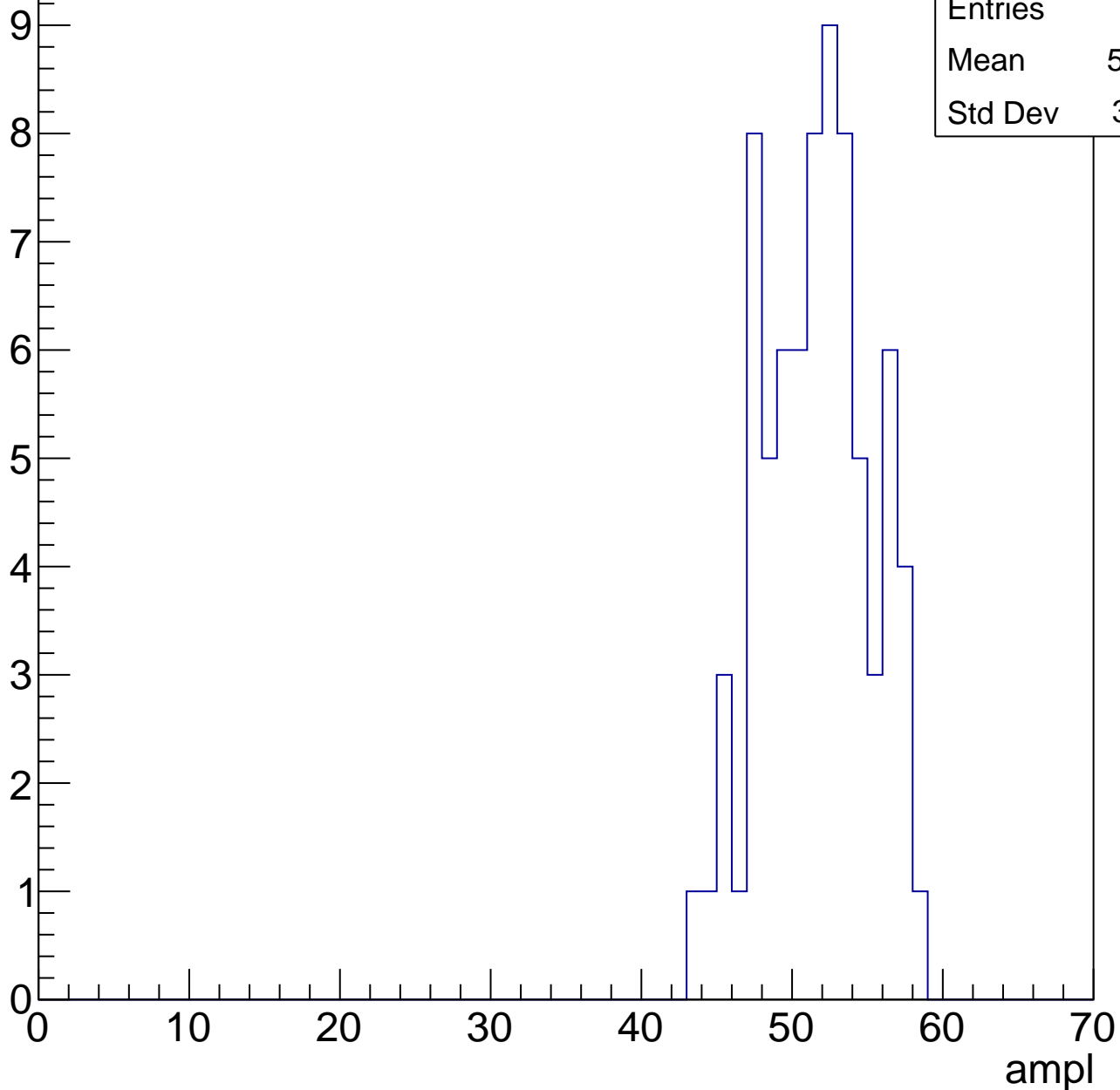


# B0L002S, U2-ch9, adc3

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	75
Mean	51.13
Std Dev	3.511

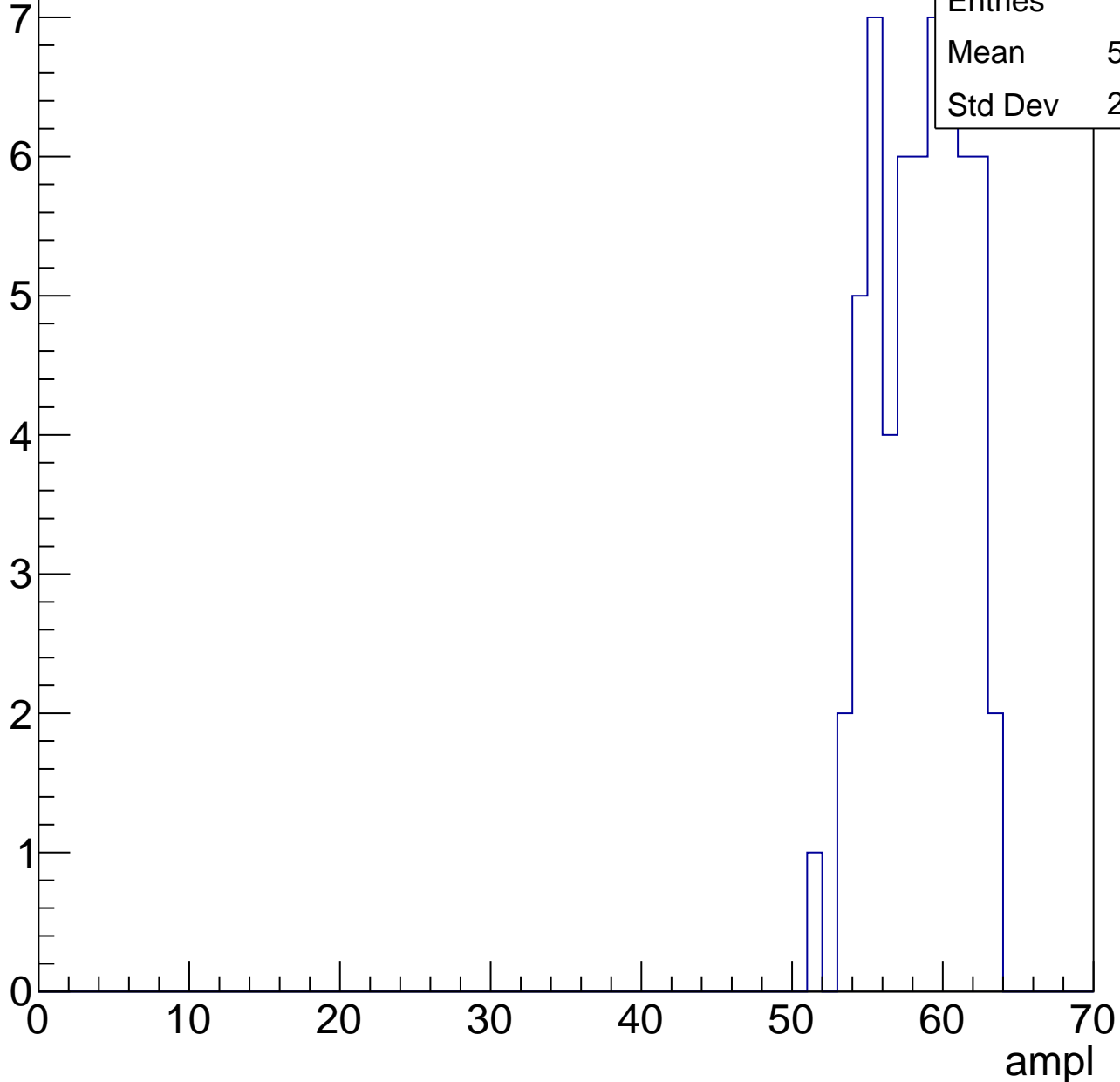


# B0L002S, U2-ch9, adc4

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	59
Mean	58.02
Std Dev	2.908

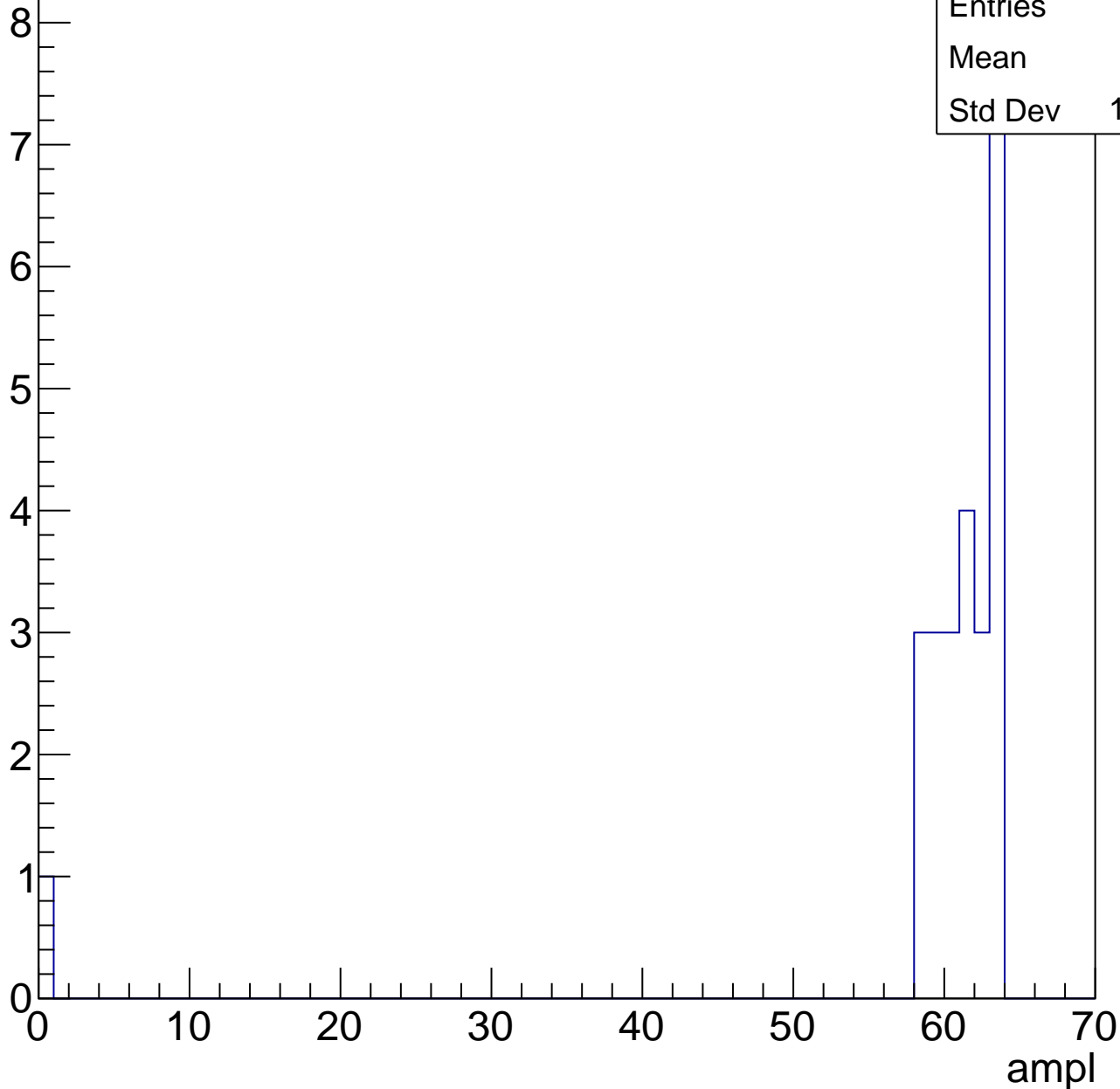


# B0L002S, U2-ch9, adc5

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	25
Mean	58.6
Std Dev	12.09



# B0L002S, U2-ch9, adc6

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry





# B0L002S, U2-ch9, adc7

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L002S, U2-ch10, adc0

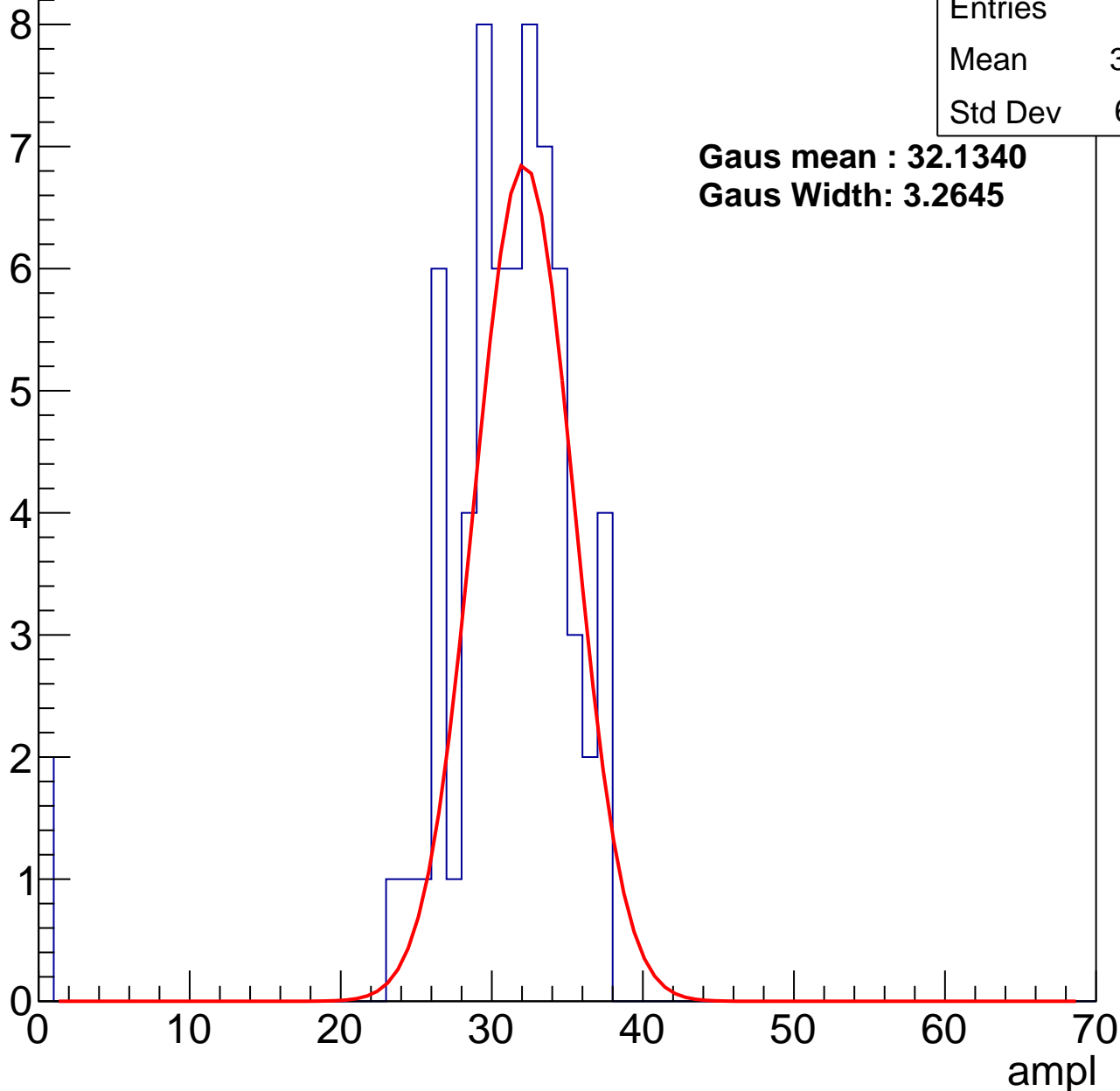
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	66
Mean	30.02
Std Dev	6.251

**Gaus mean : 32.1340**

**Gaus Width: 3.2645**



# B0L002S, U2-ch10, adc1

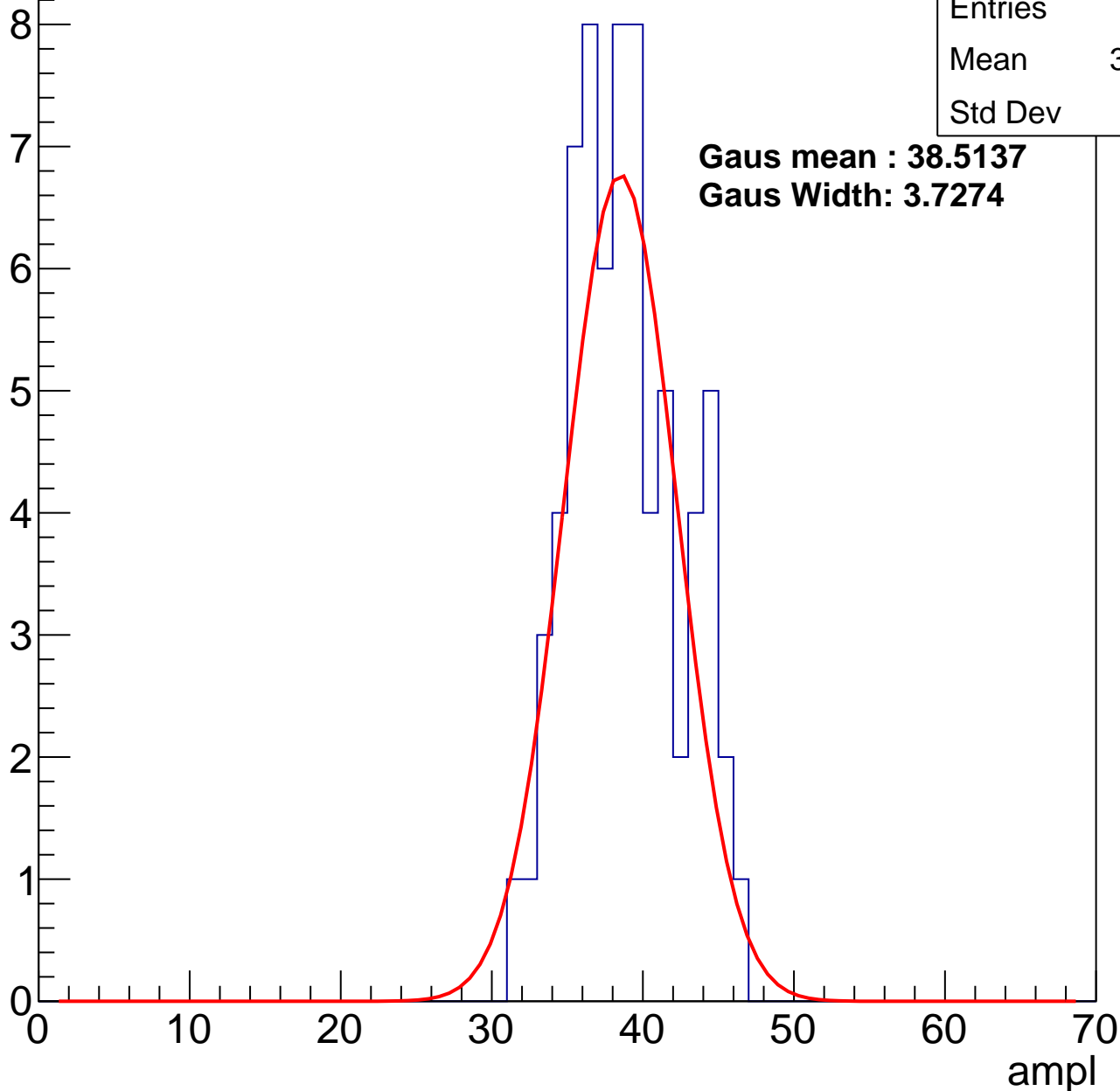
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	69
Mean	38.35
Std Dev	3.53

**Gaus mean : 38.5137**

**Gaus Width: 3.7274**



# B0L002S, U2-ch10, adc2

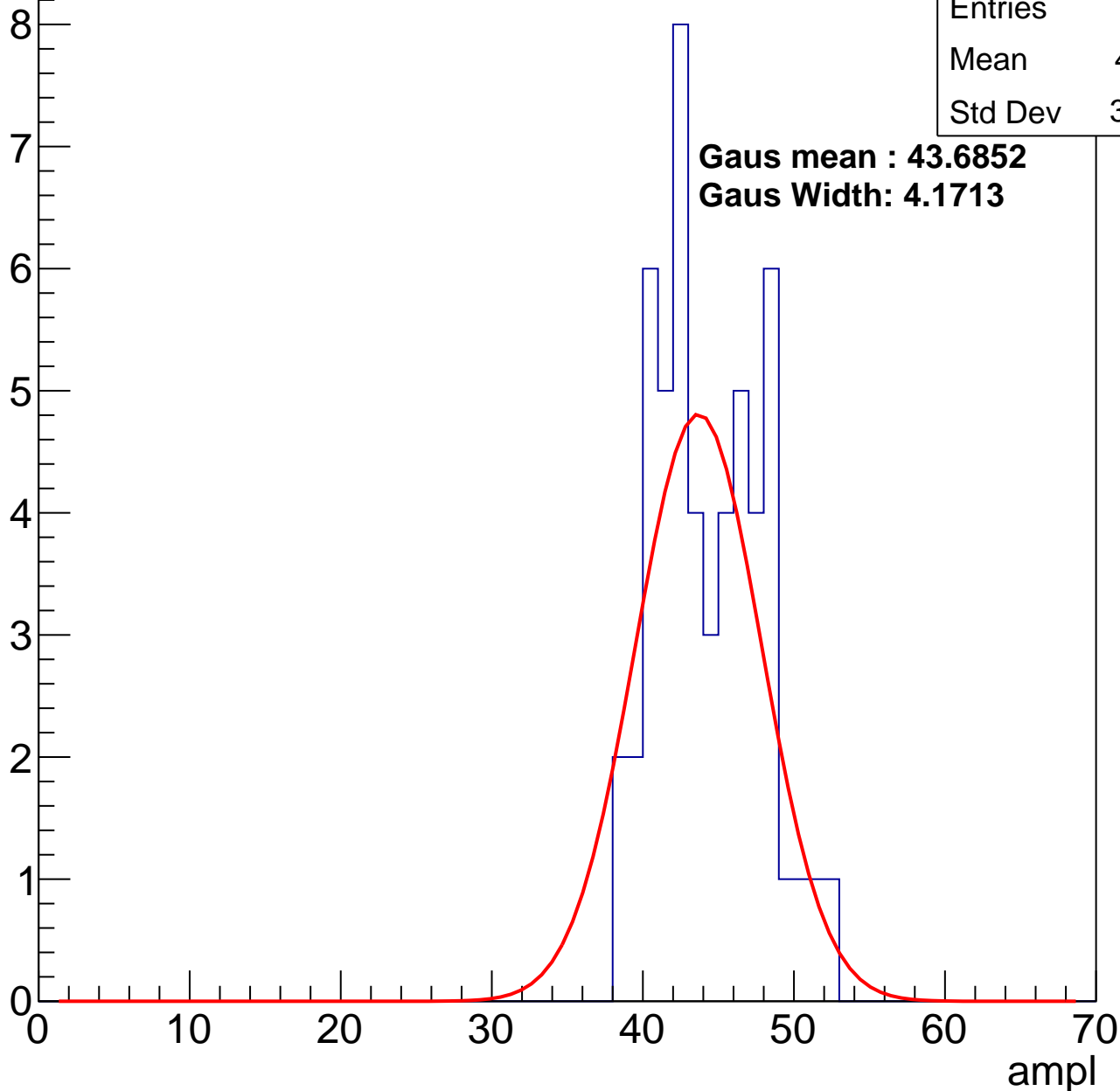
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	53
Mean	43.91
Std Dev	3.444

**Gaus mean : 43.6852**

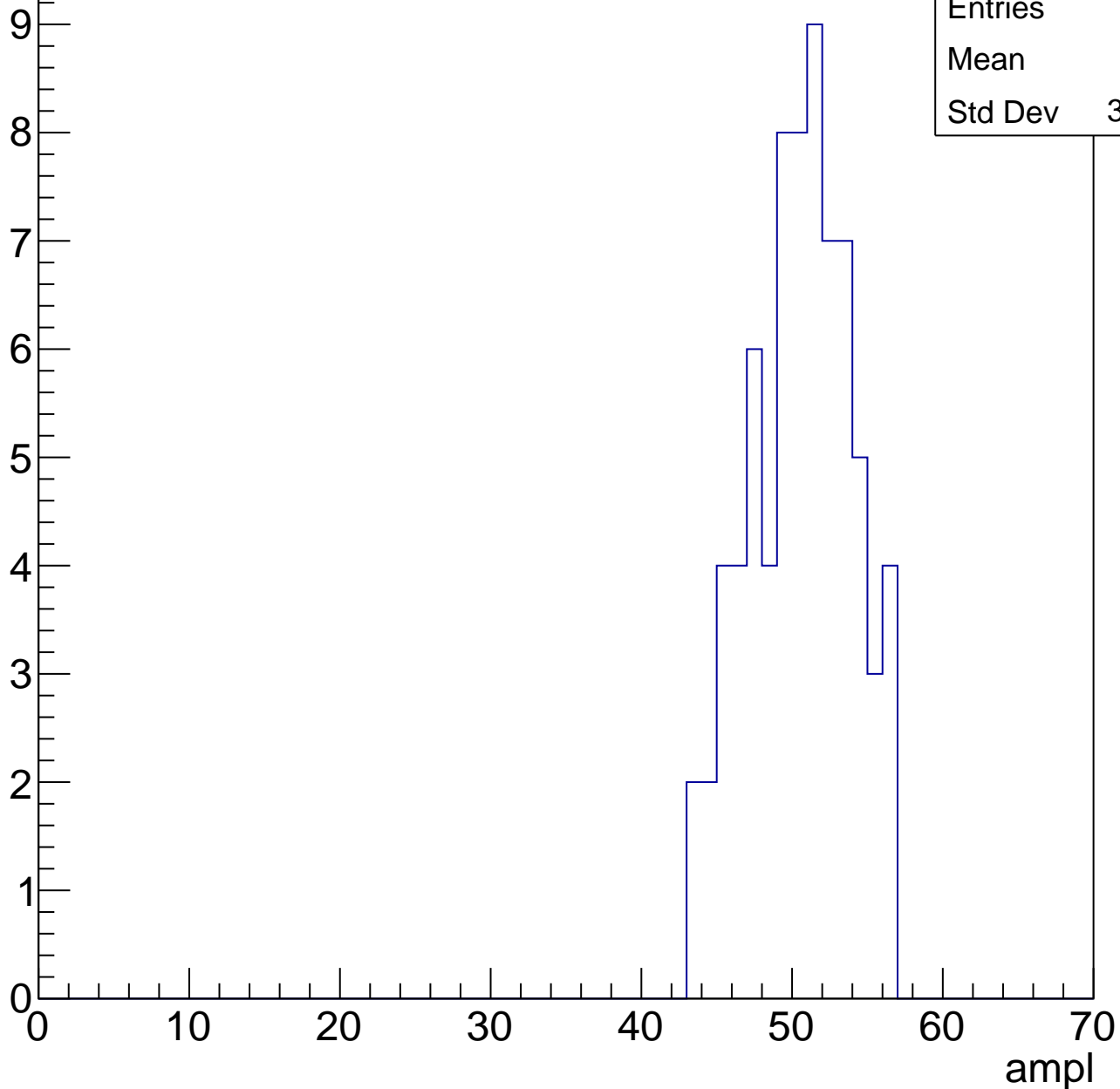
**Gaus Width: 4.1713**



# B0L002S, U2-ch10, adc3

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

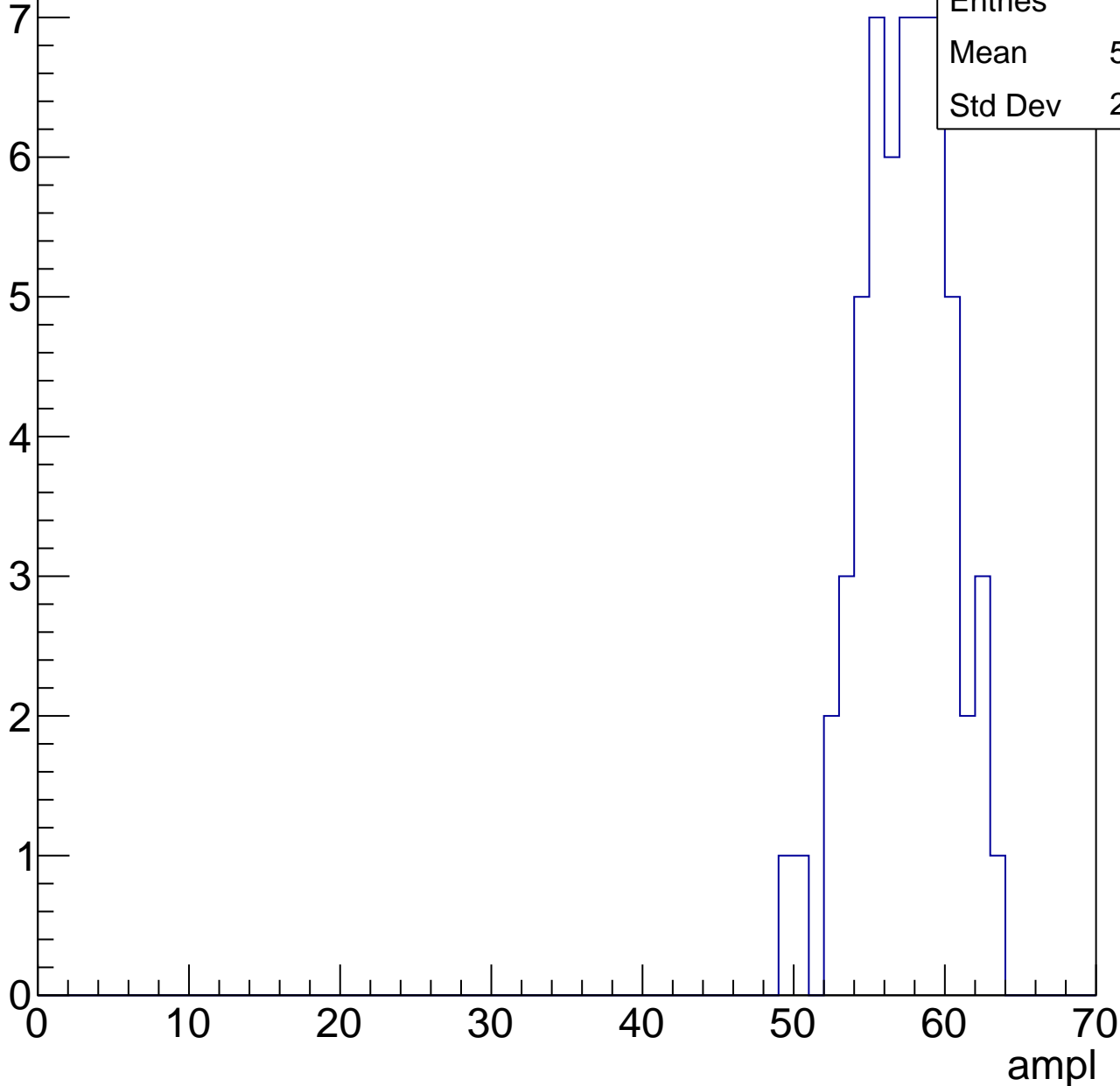


# B0L002S, U2-ch10, adc4

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	57
Mean	56.88
Std Dev	2.997



# B0L002S, U2-ch10, adc5

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	38
Mean	59.21
Std Dev	9.913

ampl

0

10

20

30

40

50

60

70

# B0L002S, U2-ch10, adc6

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry





# B0L002S, U2-ch10, adc7

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



Entries	2
Mean	0
Std Dev	0

# B0L002S, U2-ch11, adc0

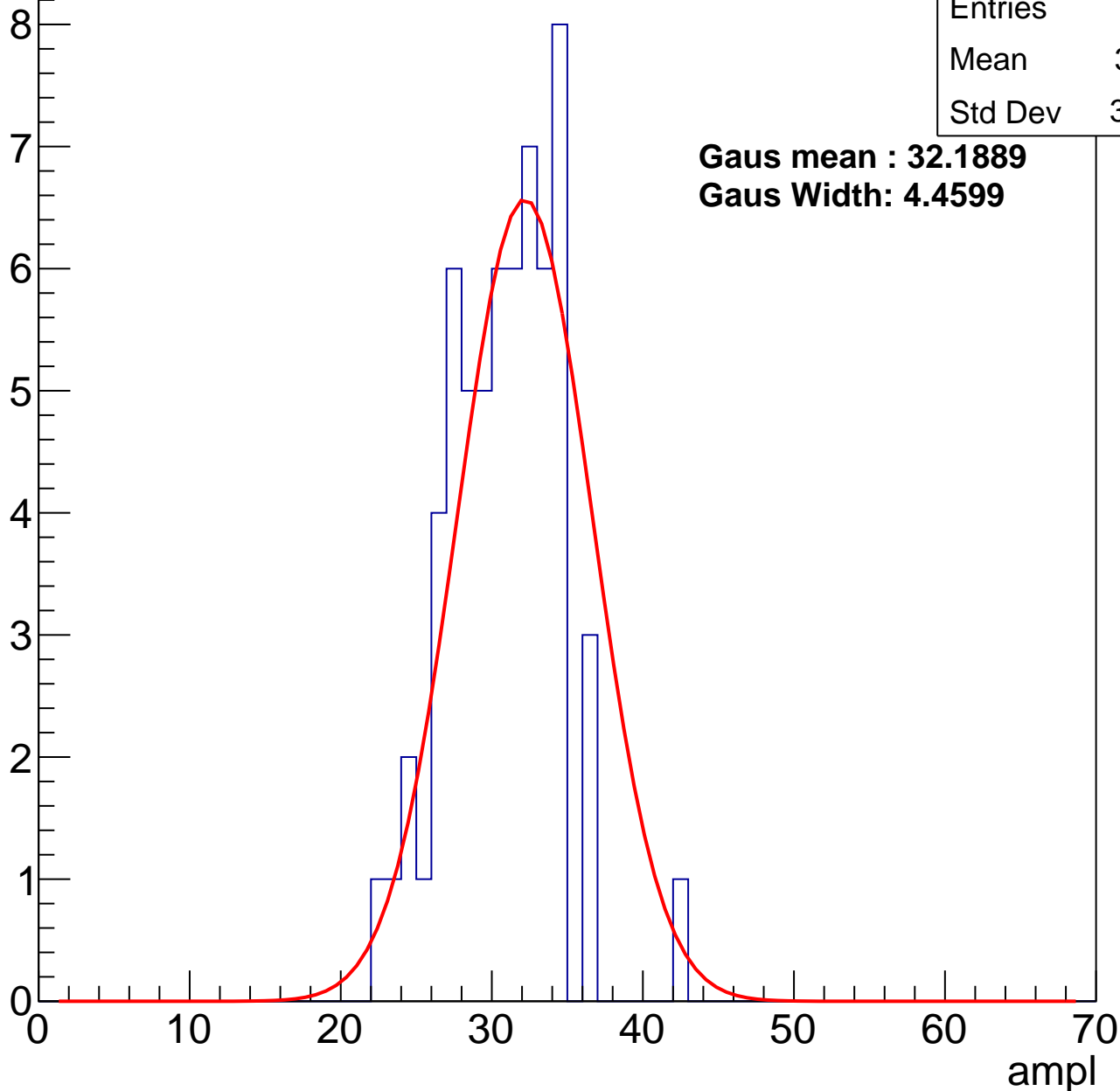
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	62
Mean	30.31
Std Dev	3.626

**Gaus mean : 32.1889**

**Gaus Width: 4.4599**



# B0L002S, U2-ch11, adc1

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entries	60
Mean	36.38
Std Dev	3.397

**Gaus mean : 37.4850**

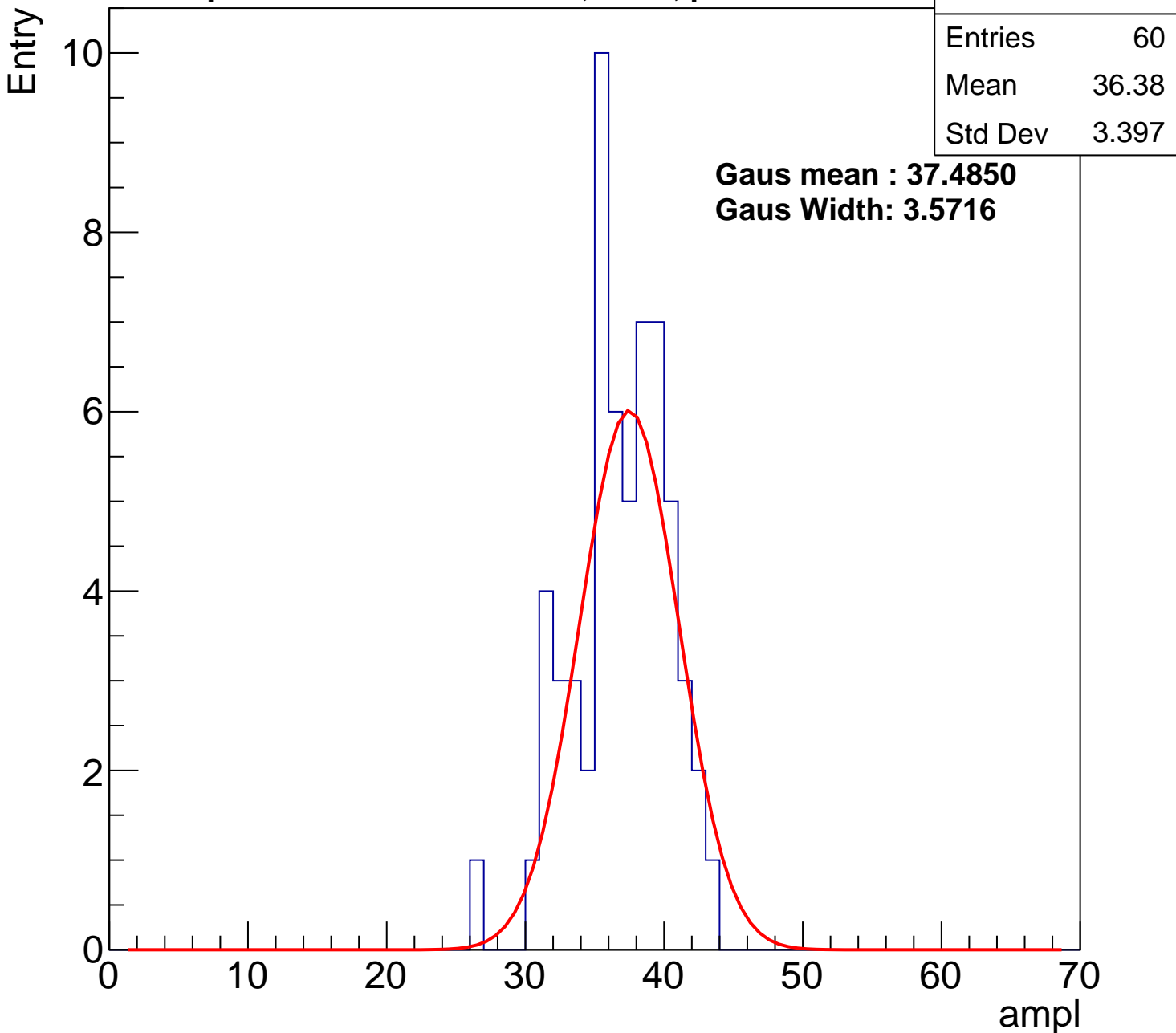
**Gaus Width: 3.5716**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L002S, U2-ch11, adc2

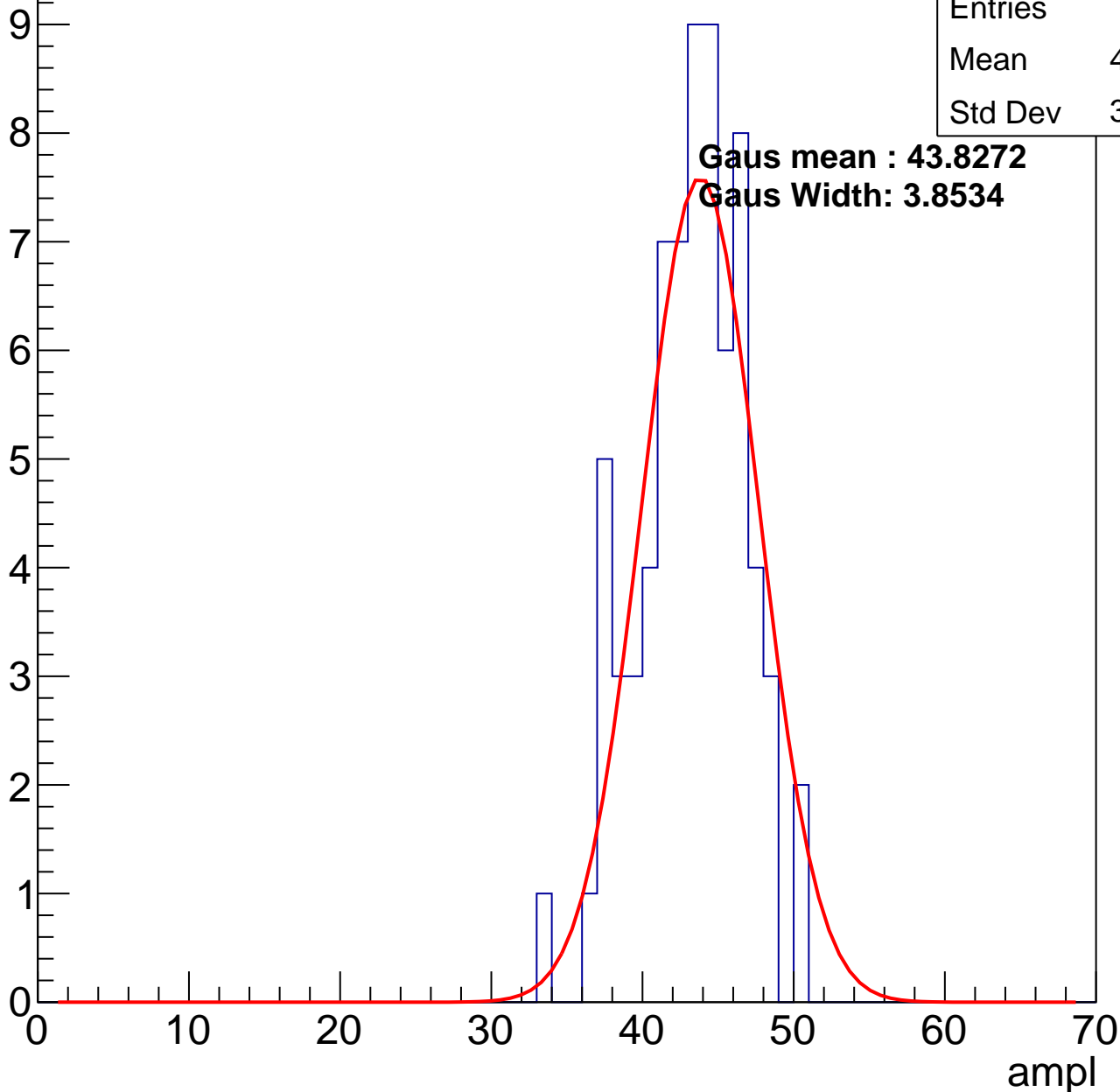
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	72
Mean	42.76
Std Dev	3.458

**Gaus mean : 43.8272**

**Gaus Width: 3.8534**

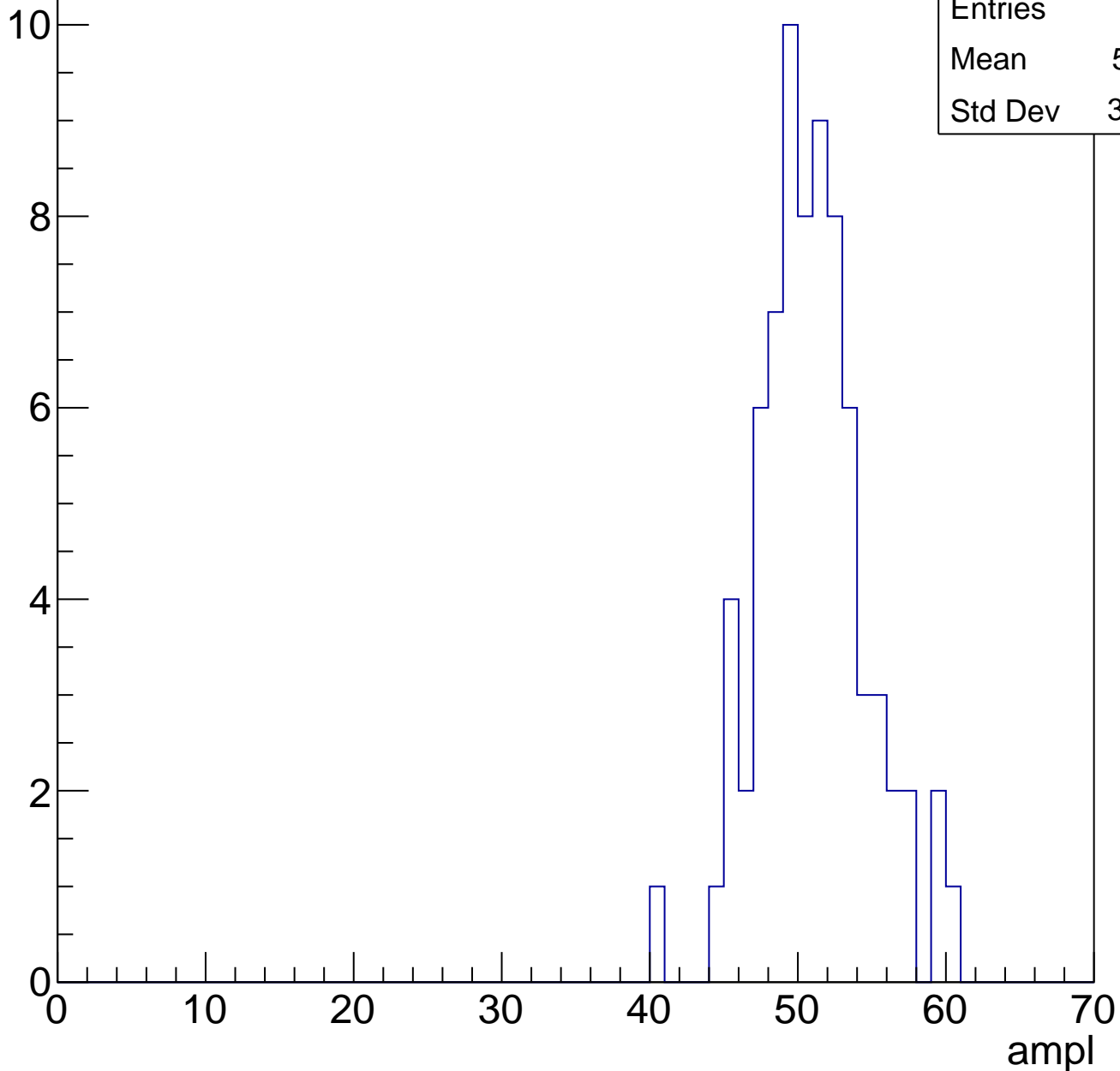


# B0L002S, U2-ch11, adc3

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entries	75
Mean	50.51
Std Dev	3.635

Entry



# B0L002S, U2-ch11, adc4

calib\_packv5\_042523\_0143.root, FC#8, port C1

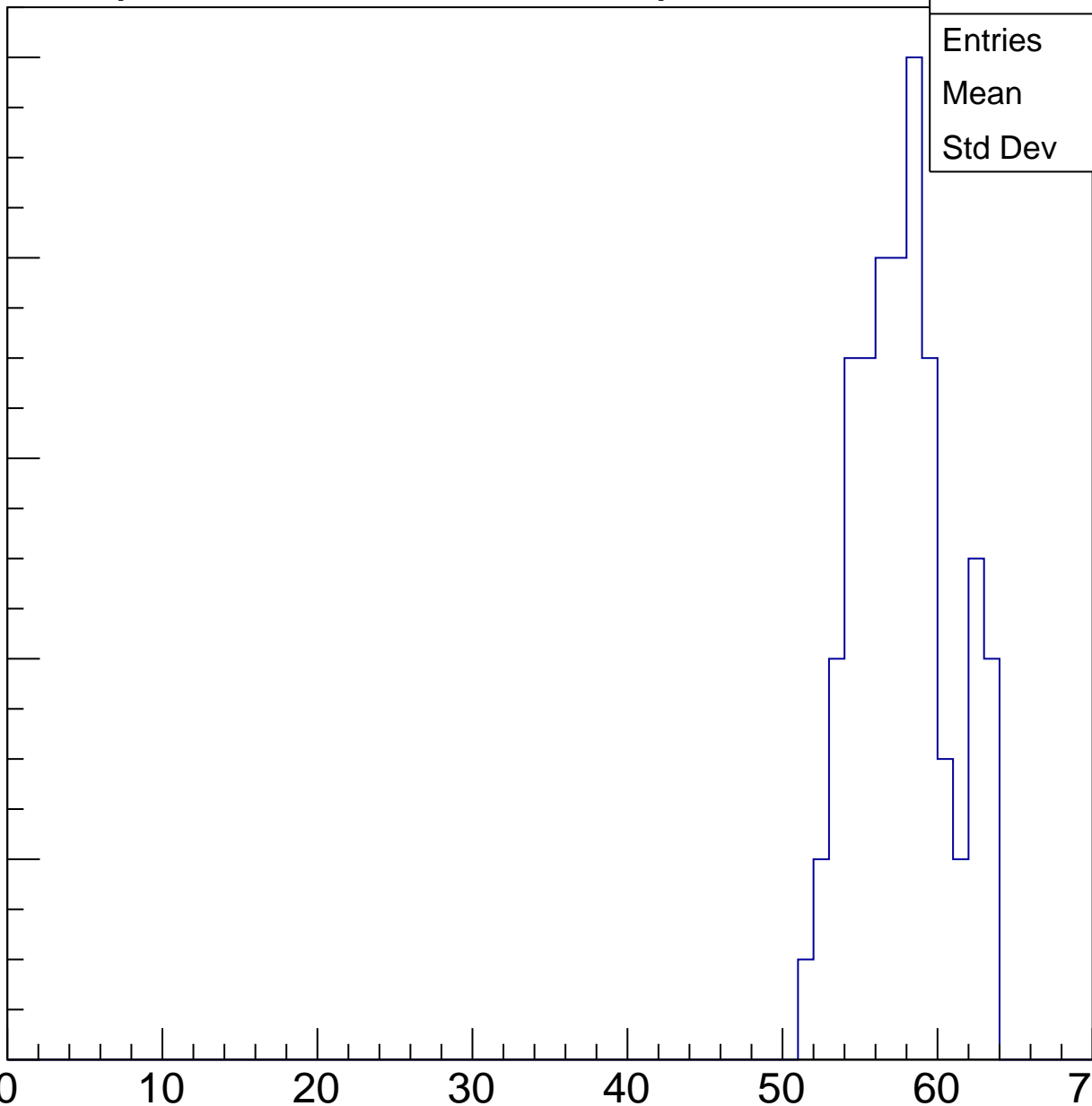
Entries	68
Mean	57.22
Std Dev	2.999

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

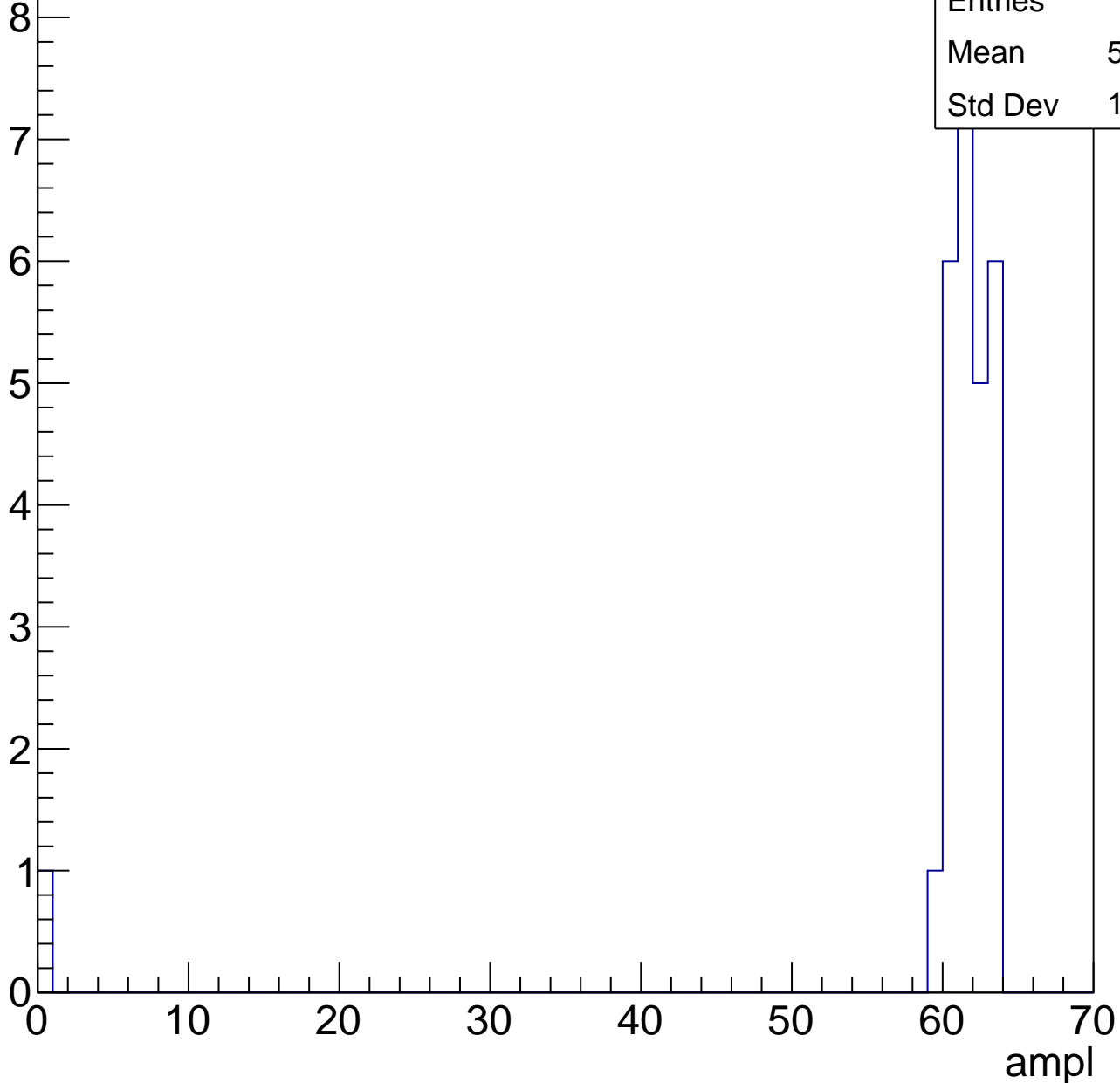


# B0L002S, U2-ch11, adc5

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	27
Mean	59.07
Std Dev	11.64



# B0L002S, U2-ch11, adc6

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



Entries	0
Mean	0
Std Dev	0



# B0L002S, U2-ch11, adc7

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



# B0L002S, U2-ch12, adc0

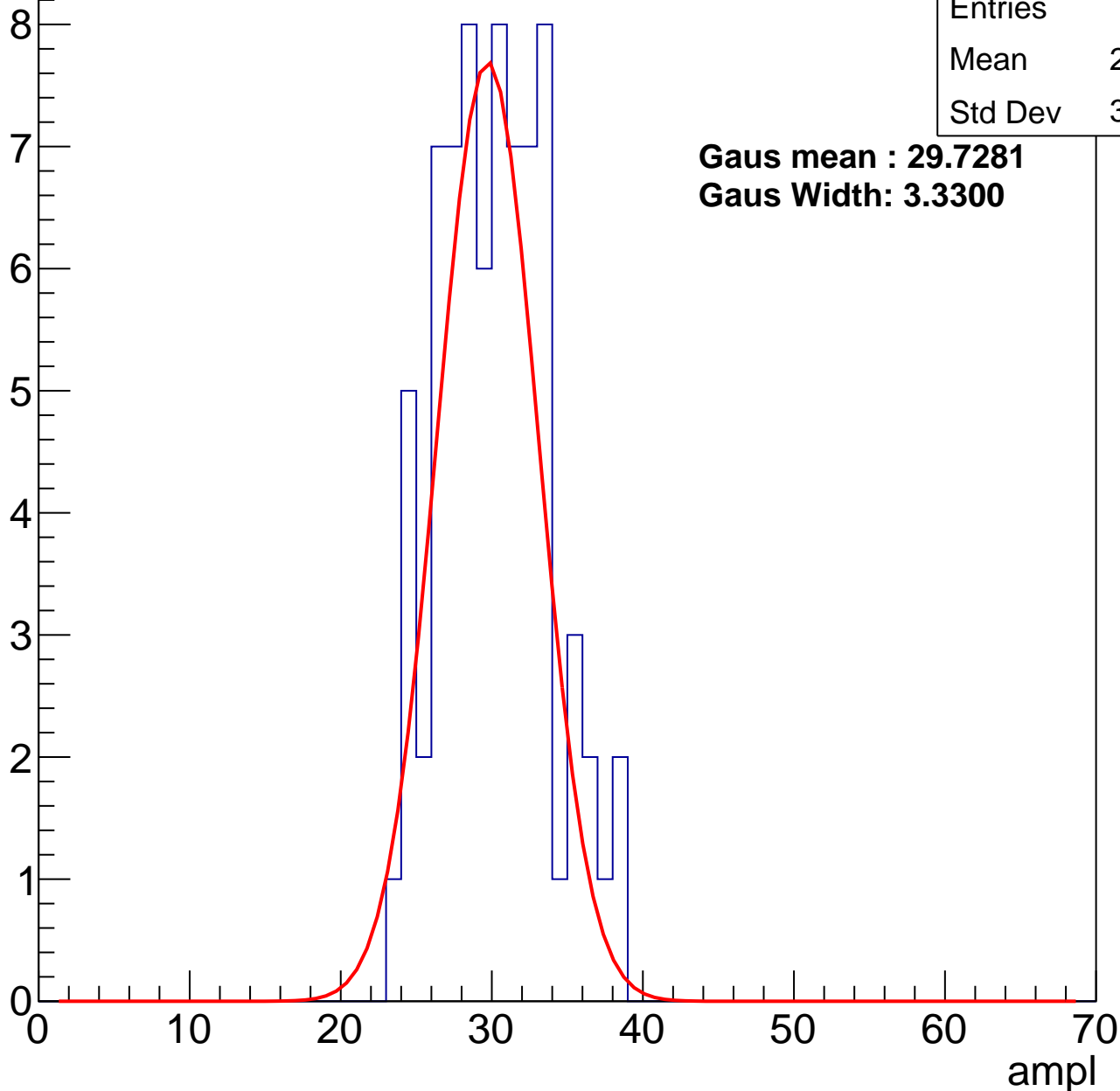
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	75
Mean	29.75
Std Dev	3.529

**Gaus mean : 29.7281**

**Gaus Width: 3.3300**



# B0L002S, U2-ch12, adc1

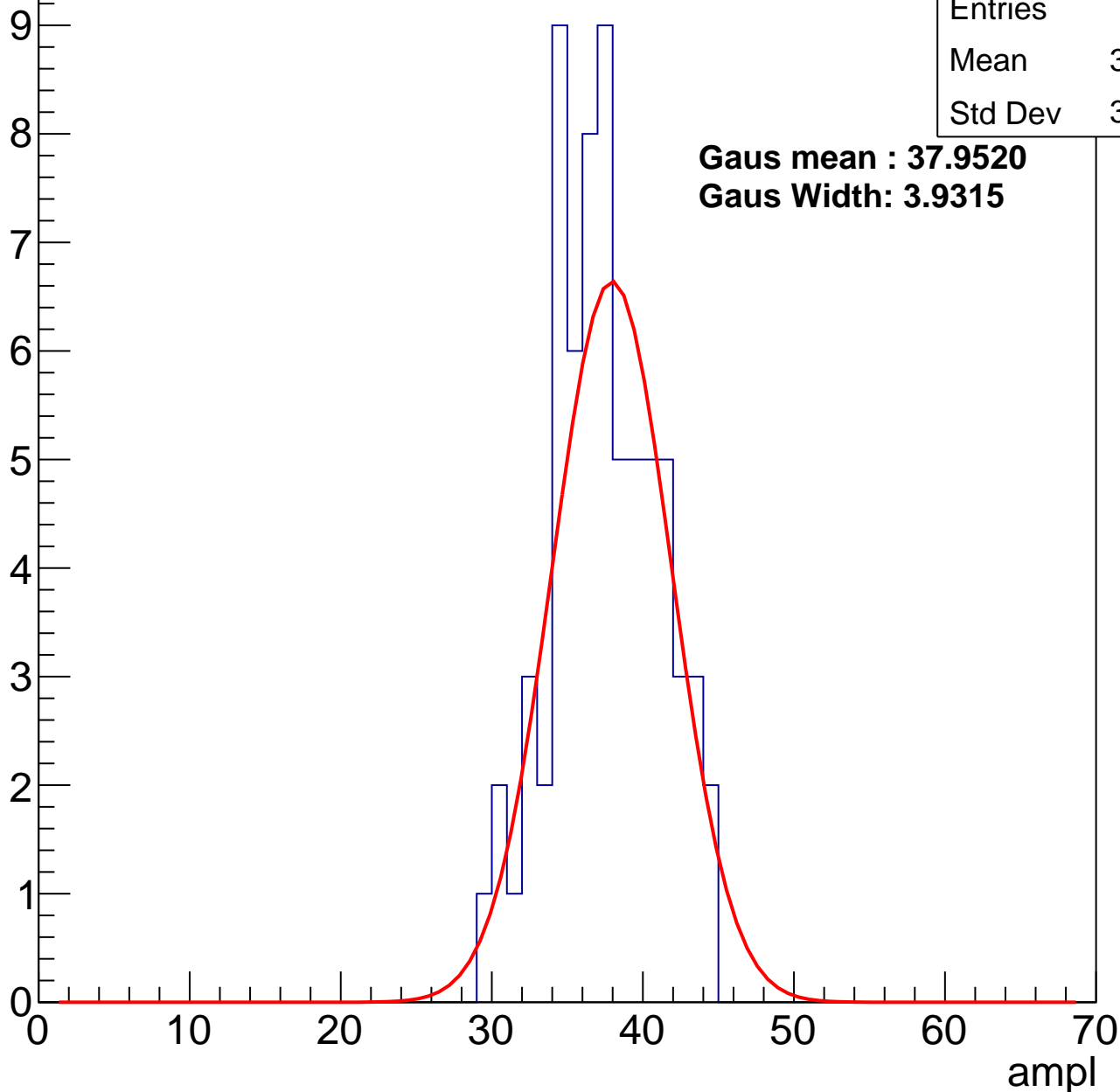
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	69
Mean	36.99
Std Dev	3.508

**Gaus mean : 37.9520**

**Gaus Width: 3.9315**



# B0L002S, U2-ch12, adc2

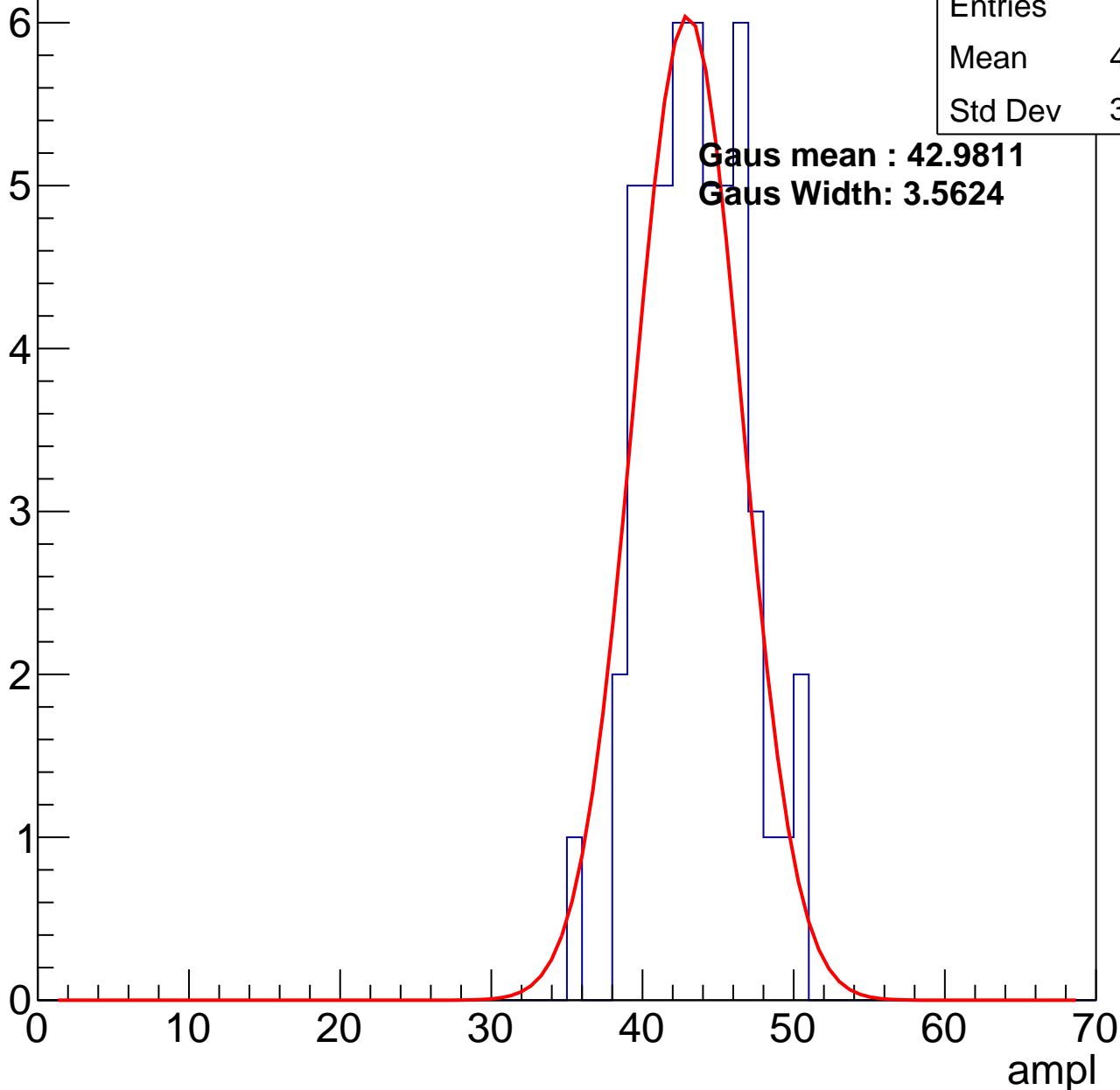
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	53
Mean	43.02
Std Dev	3.224

**Gaus mean : 42.9811**

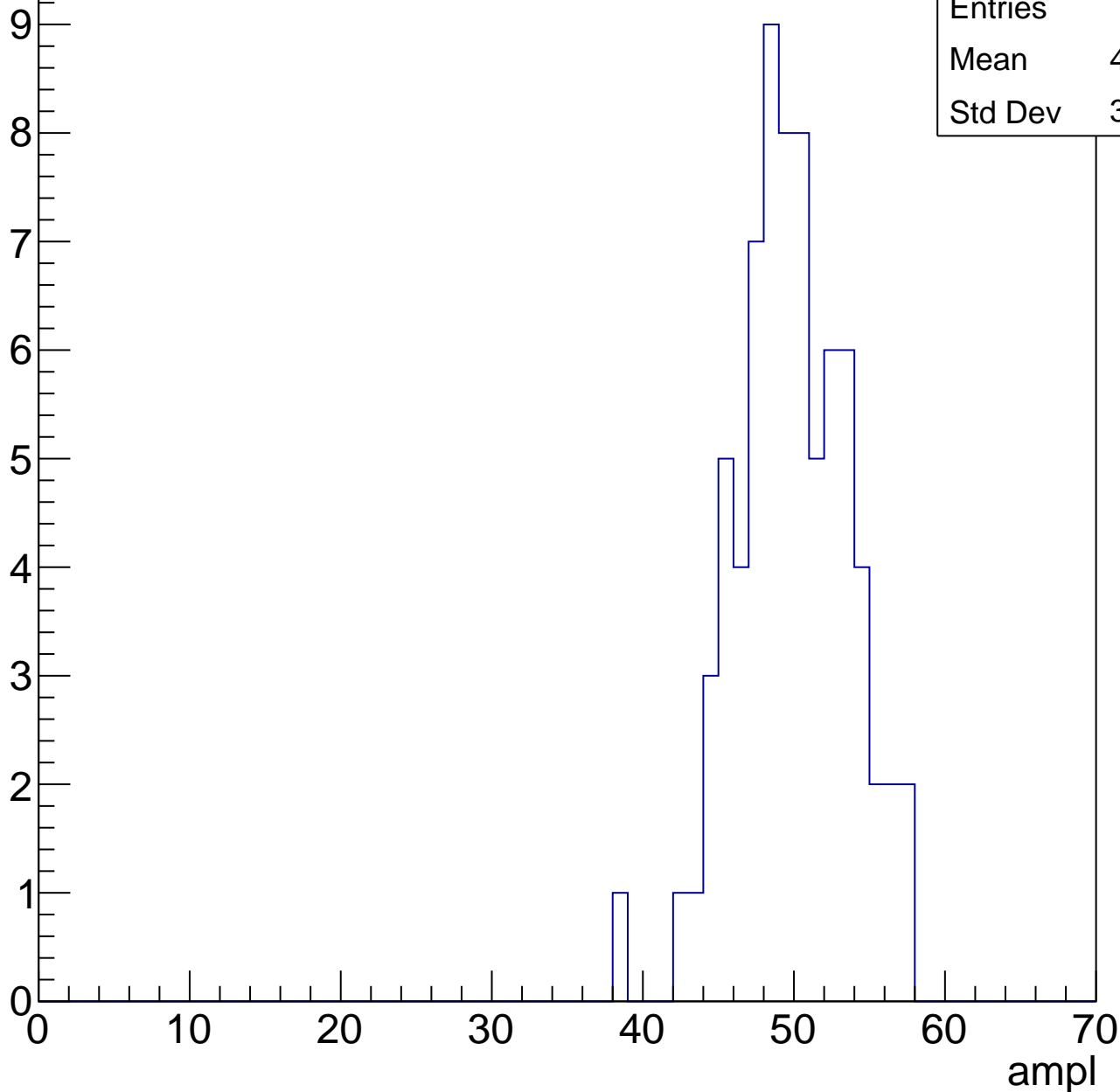
**Gaus Width: 3.5624**



# B0L002S, U2-ch12, adc3

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



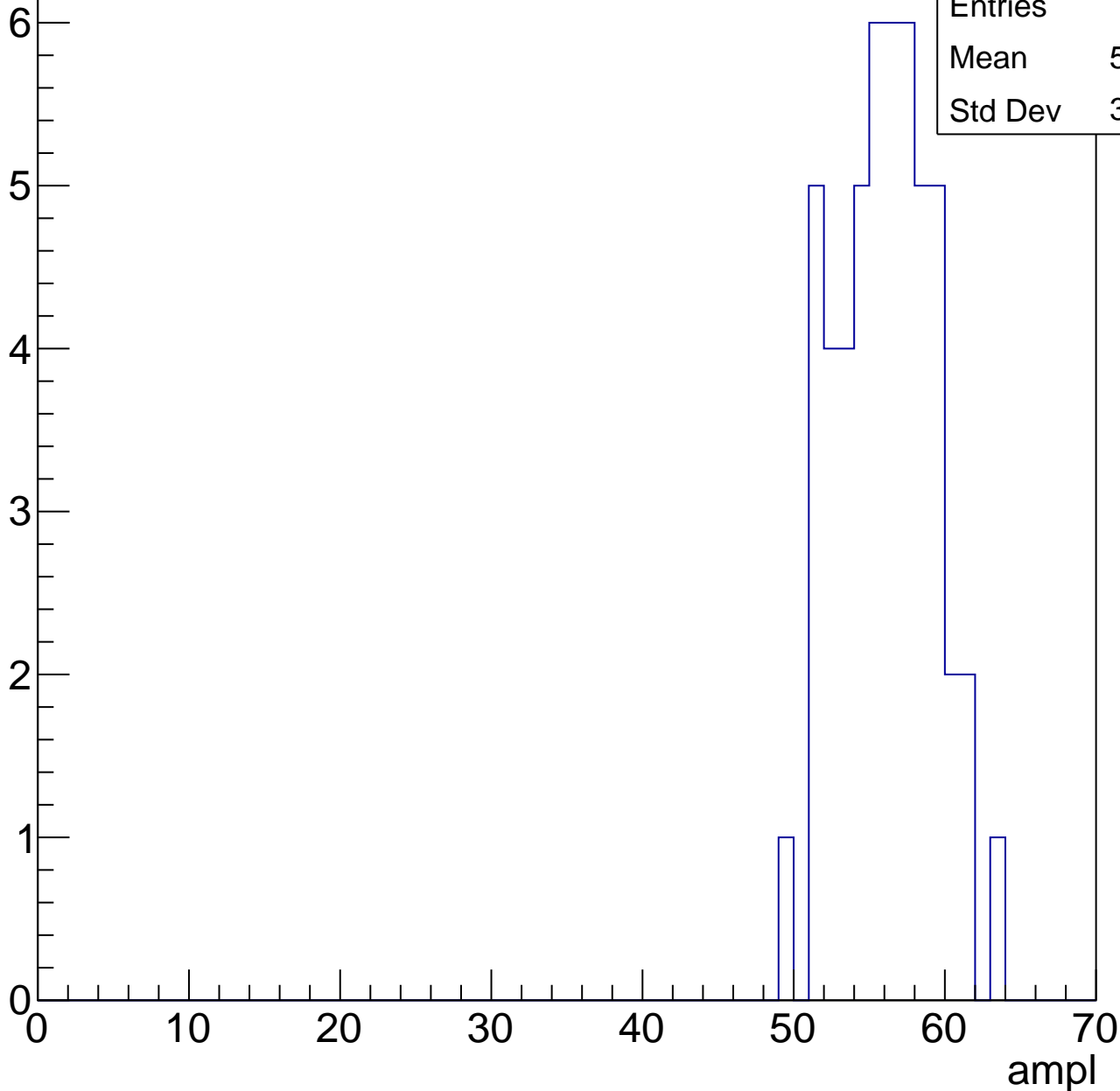
Entries	74
Mean	49.38
Std Dev	3.675

# B0L002S, U2-ch12, adc4

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	52
Mean	55.62
Std Dev	3.083



# B0L002S, U2-ch12, adc5

calib\_packv5\_042523\_0143.root, FC#8, port C1

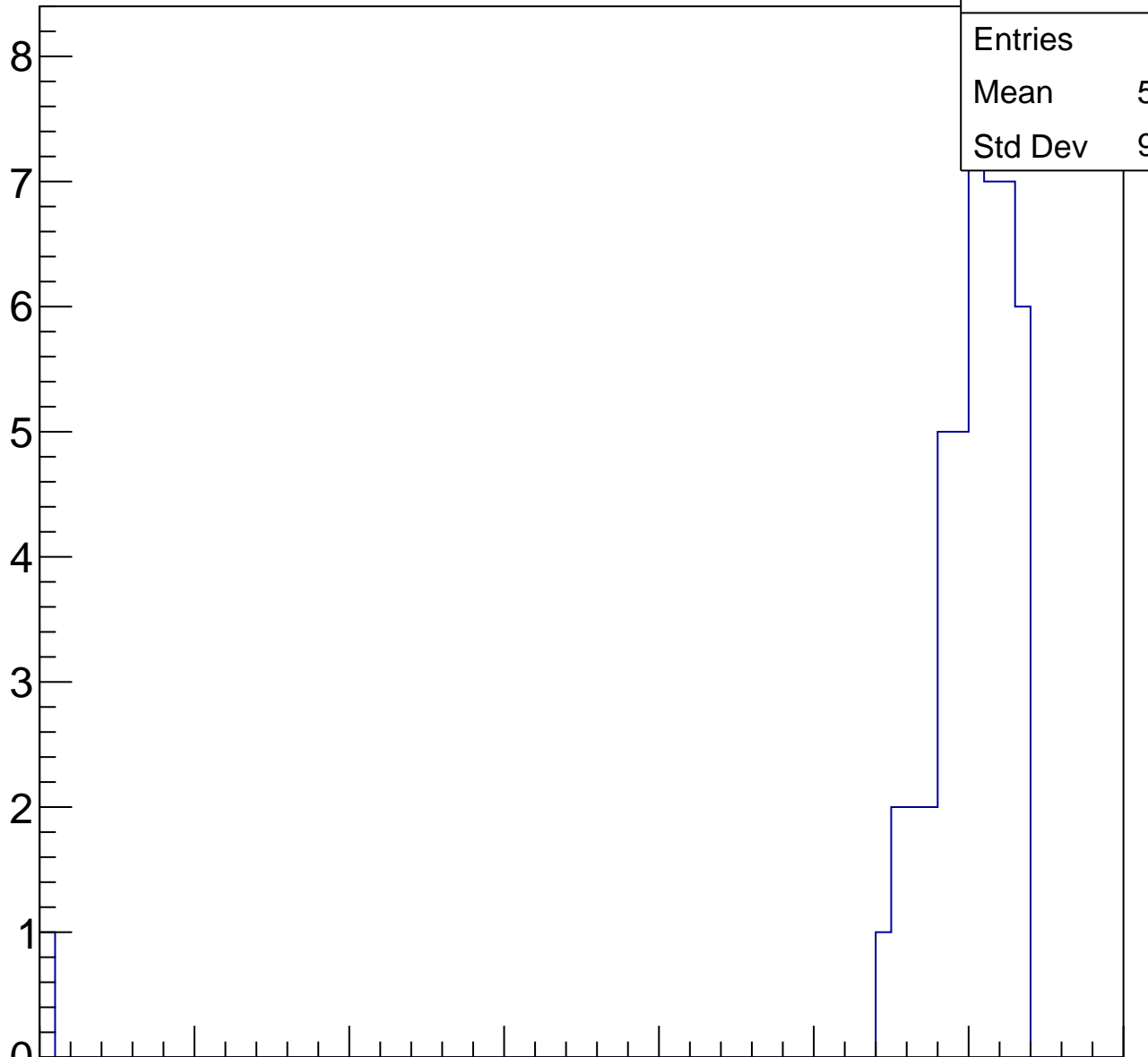
Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	46
Mean	58.57
Std Dev	9.035

ampl

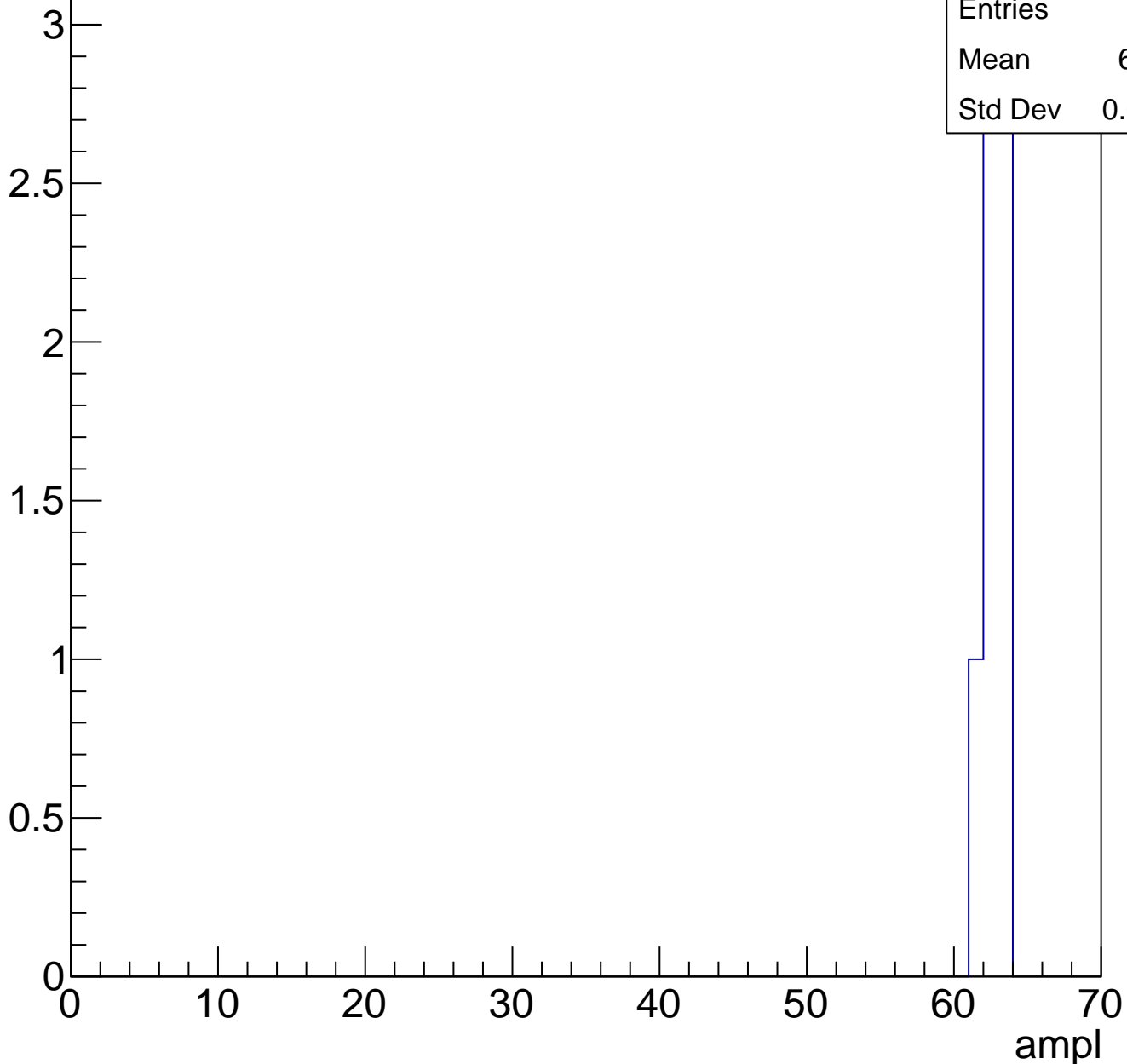
0 10 20 30 40 50 60 70



# B0L002S, U2-ch12, adc6

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry





# B0L002S, U2-ch12, adc7

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L002S, U2-ch13, adc0

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entries	76
Mean	30.67
Std Dev	3.385

**Gaus mean : 30.7379**

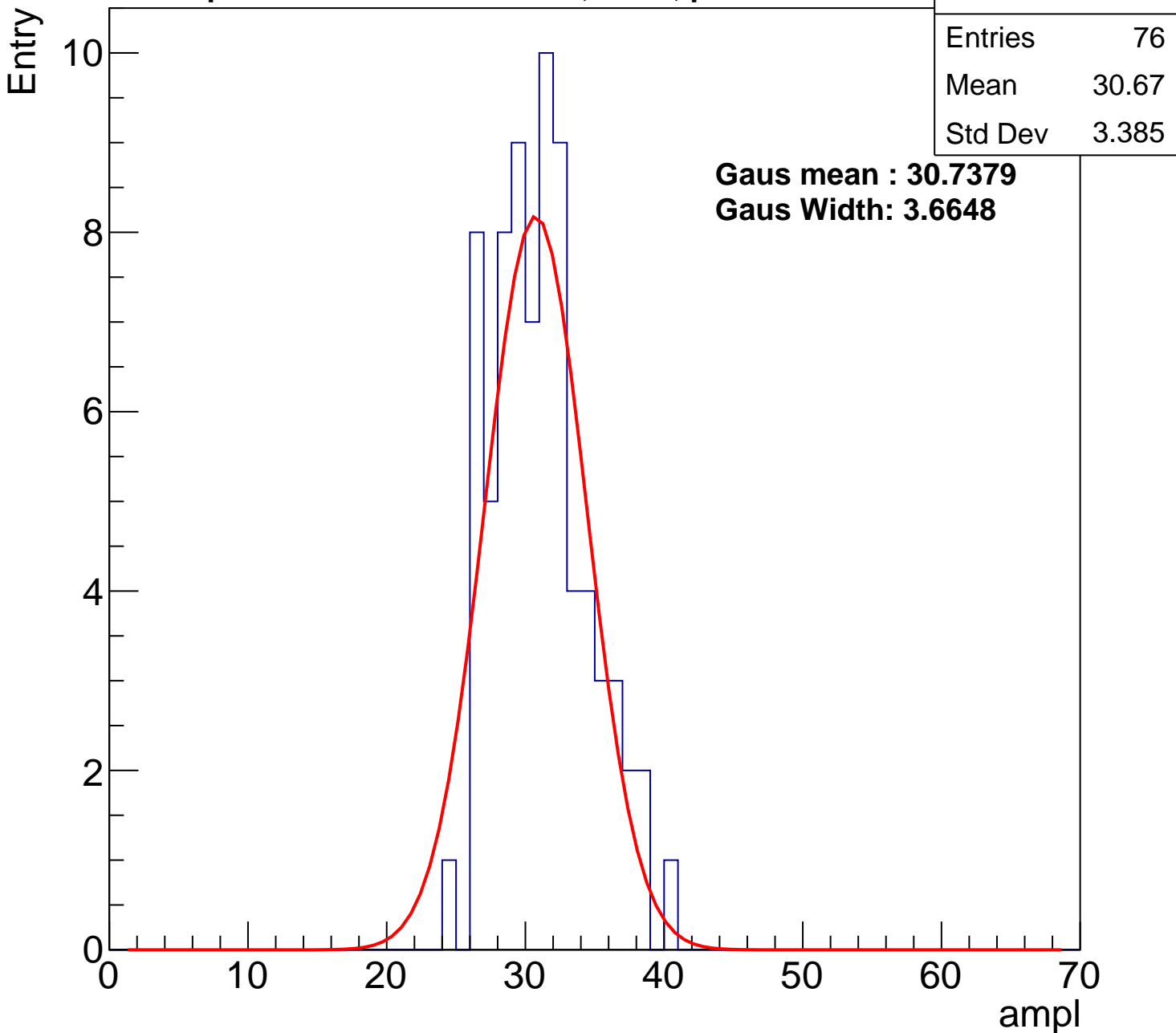
**Gaus Width: 3.6648**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



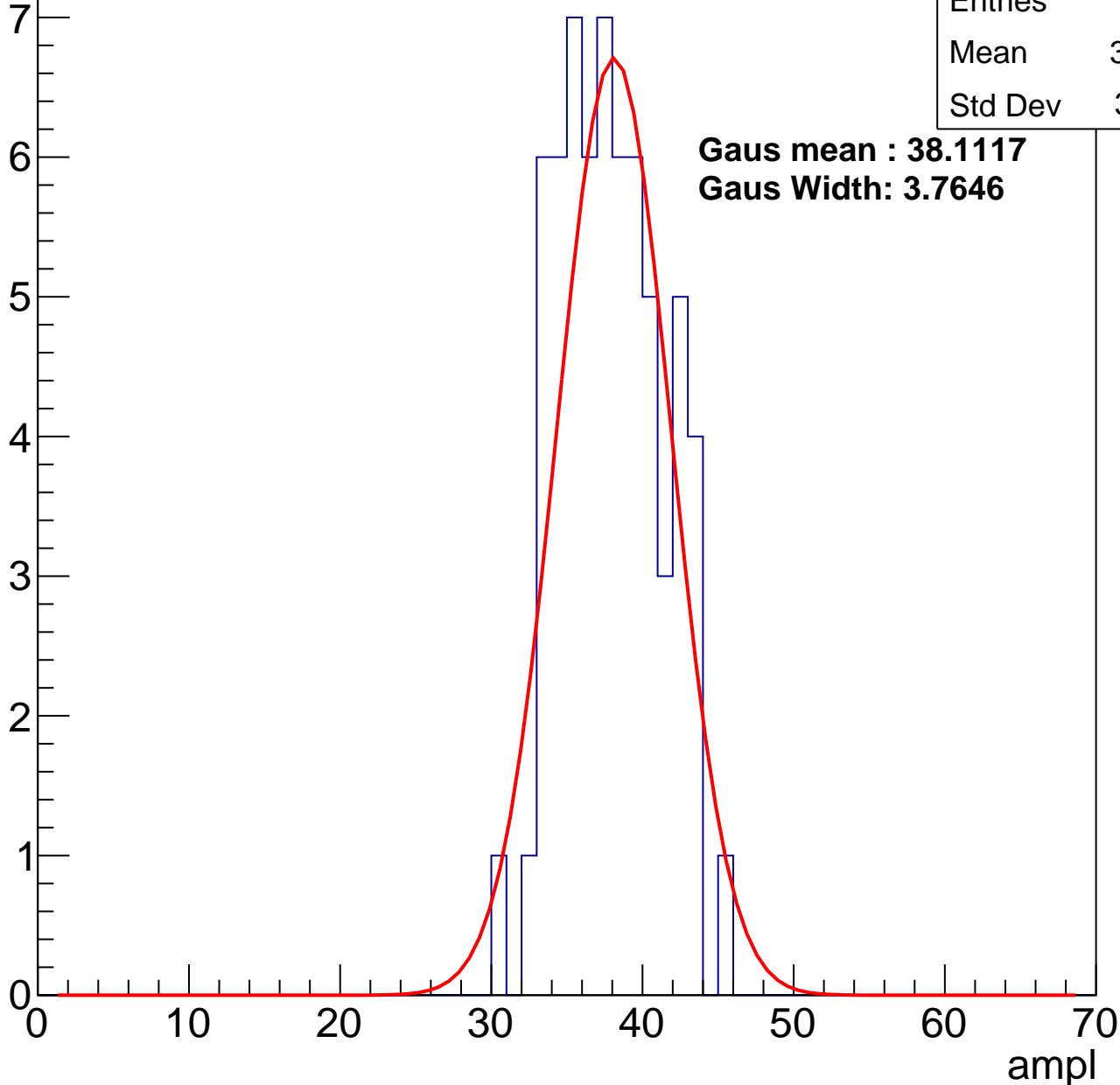
# B0L002S, U2-ch13, adc1

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	64
Mean	37.44
Std Dev	3.311

**Gaus mean : 38.1117**  
**Gaus Width: 3.7646**



# B0L002S, U2-ch13, adc2

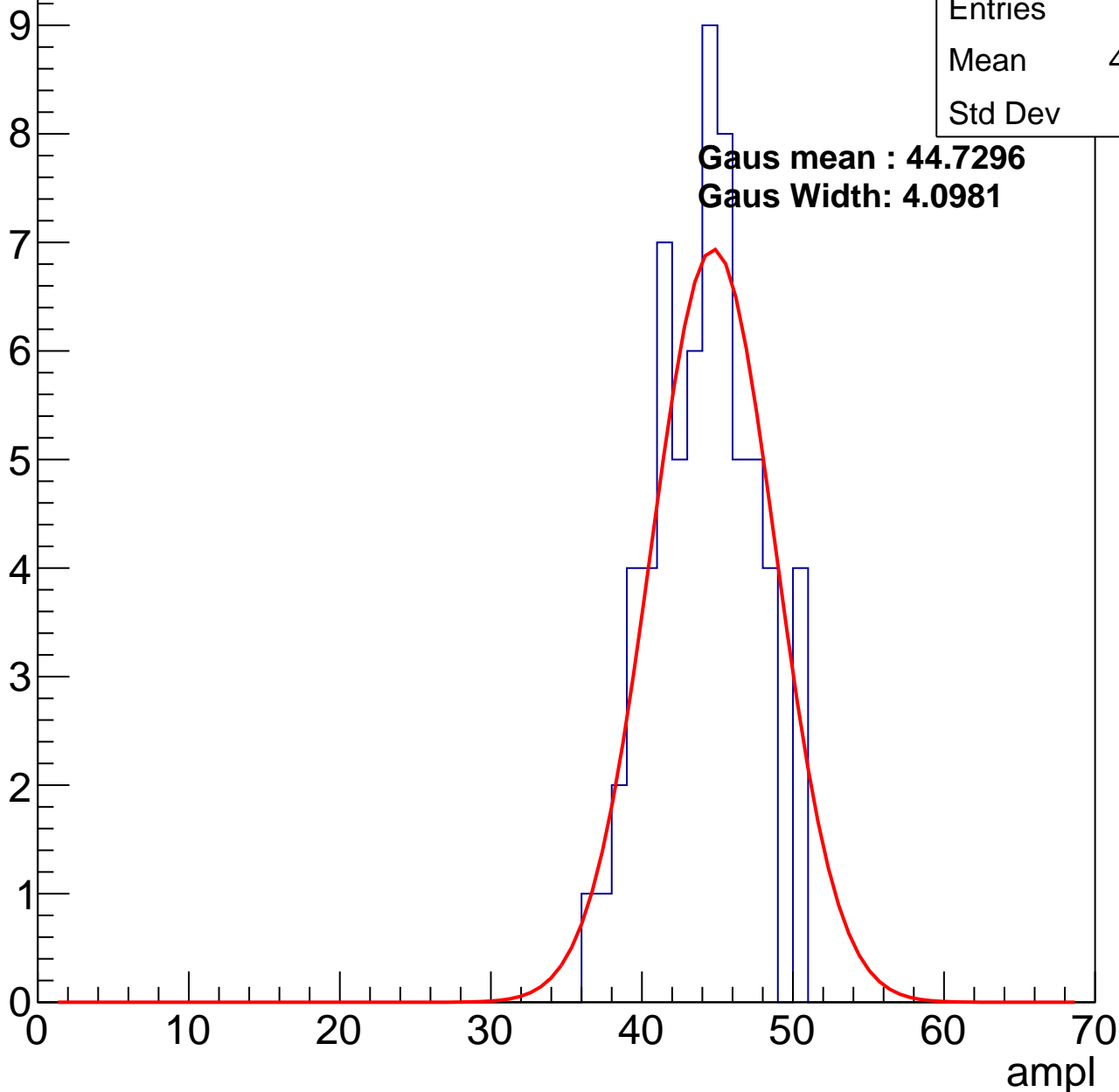
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	65
Mean	43.58
Std Dev	3.3

**Gaus mean : 44.7296**

**Gaus Width: 4.0981**

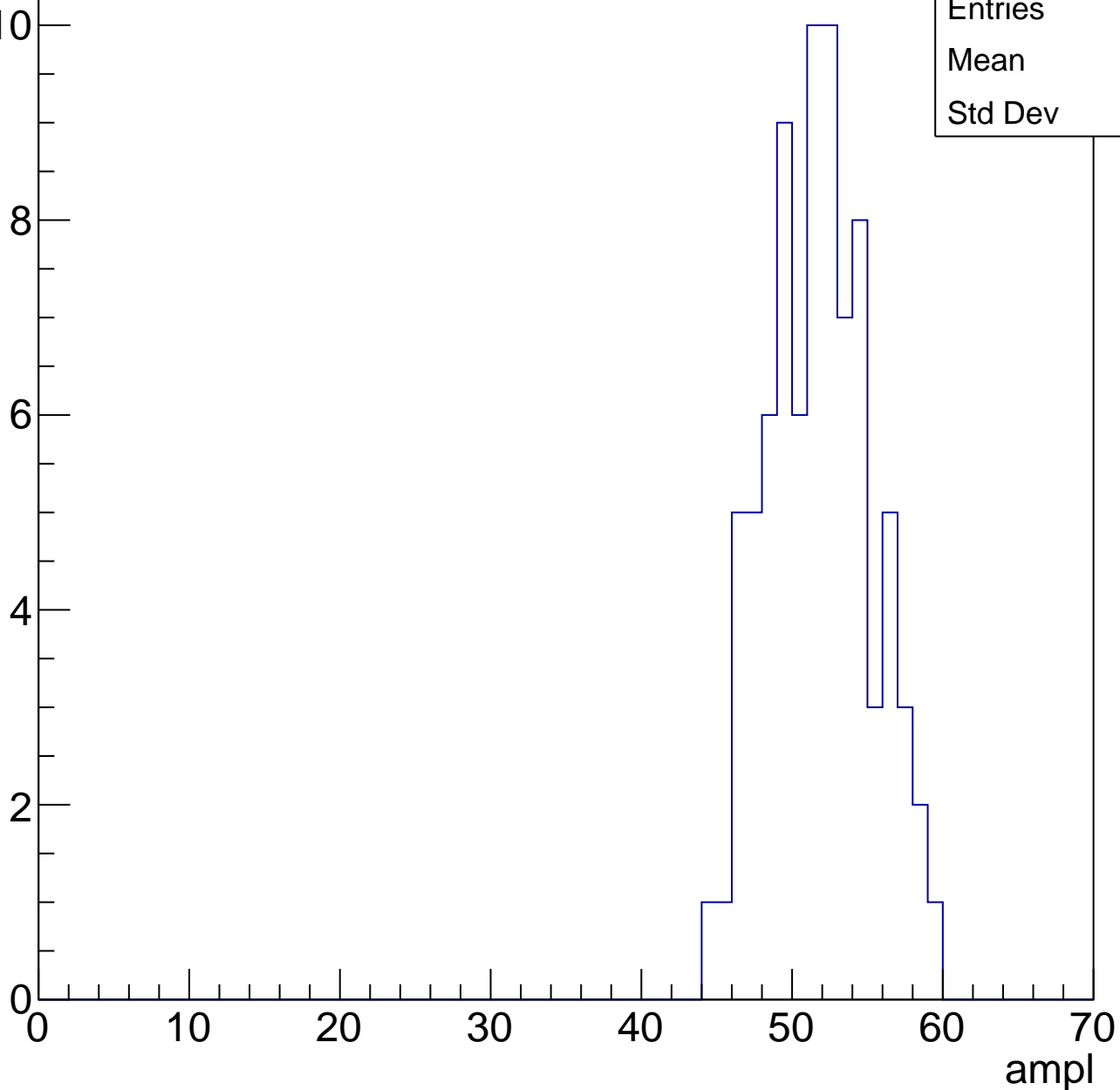


# B0L002S, U2-ch13, adc3

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	82
Mean	51.3
Std Dev	3.37

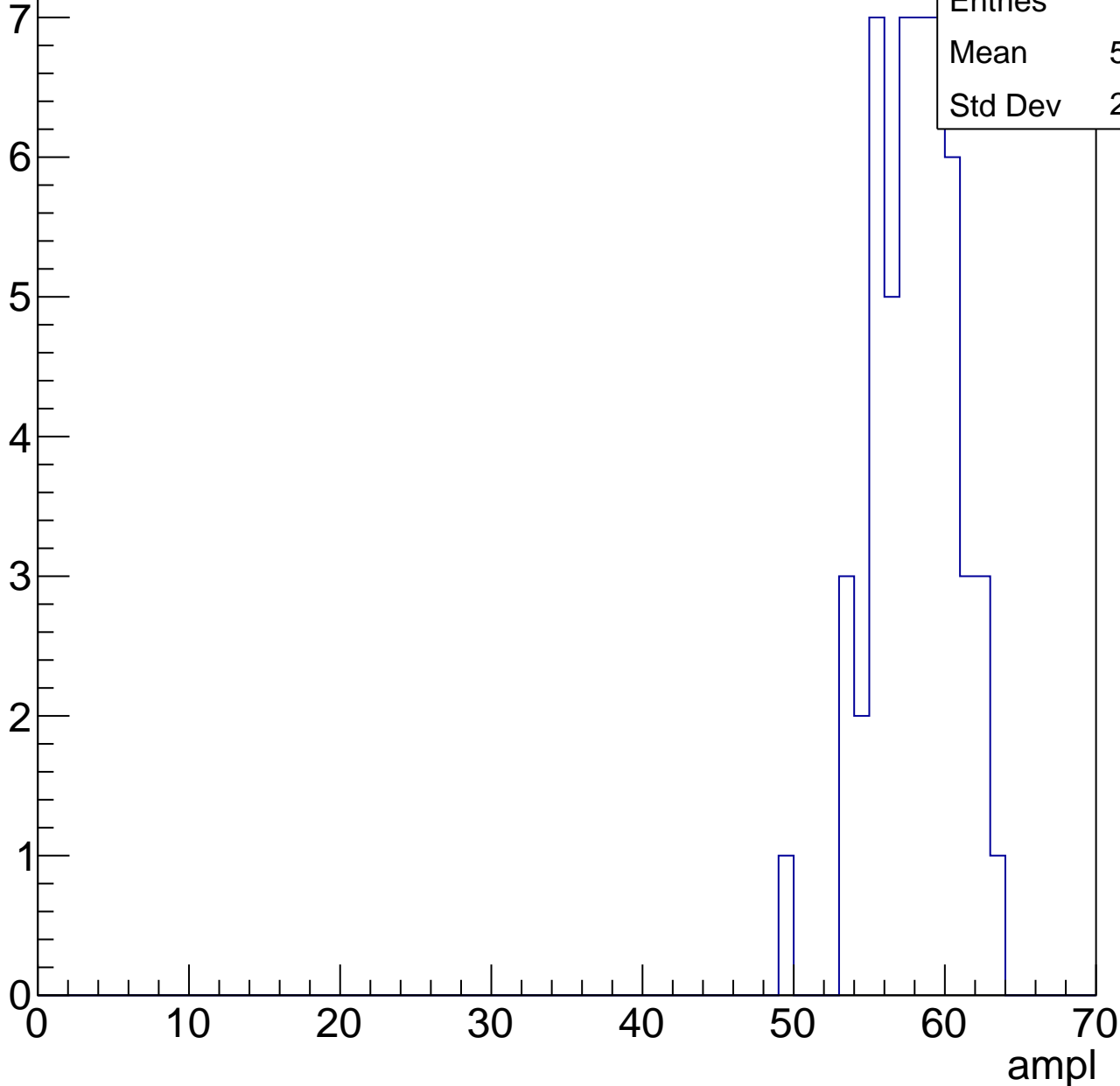


# B0L002S, U2-ch13, adc4

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	52
Mean	57.52
Std Dev	2.763



# B0L002S, U2-ch13, adc5

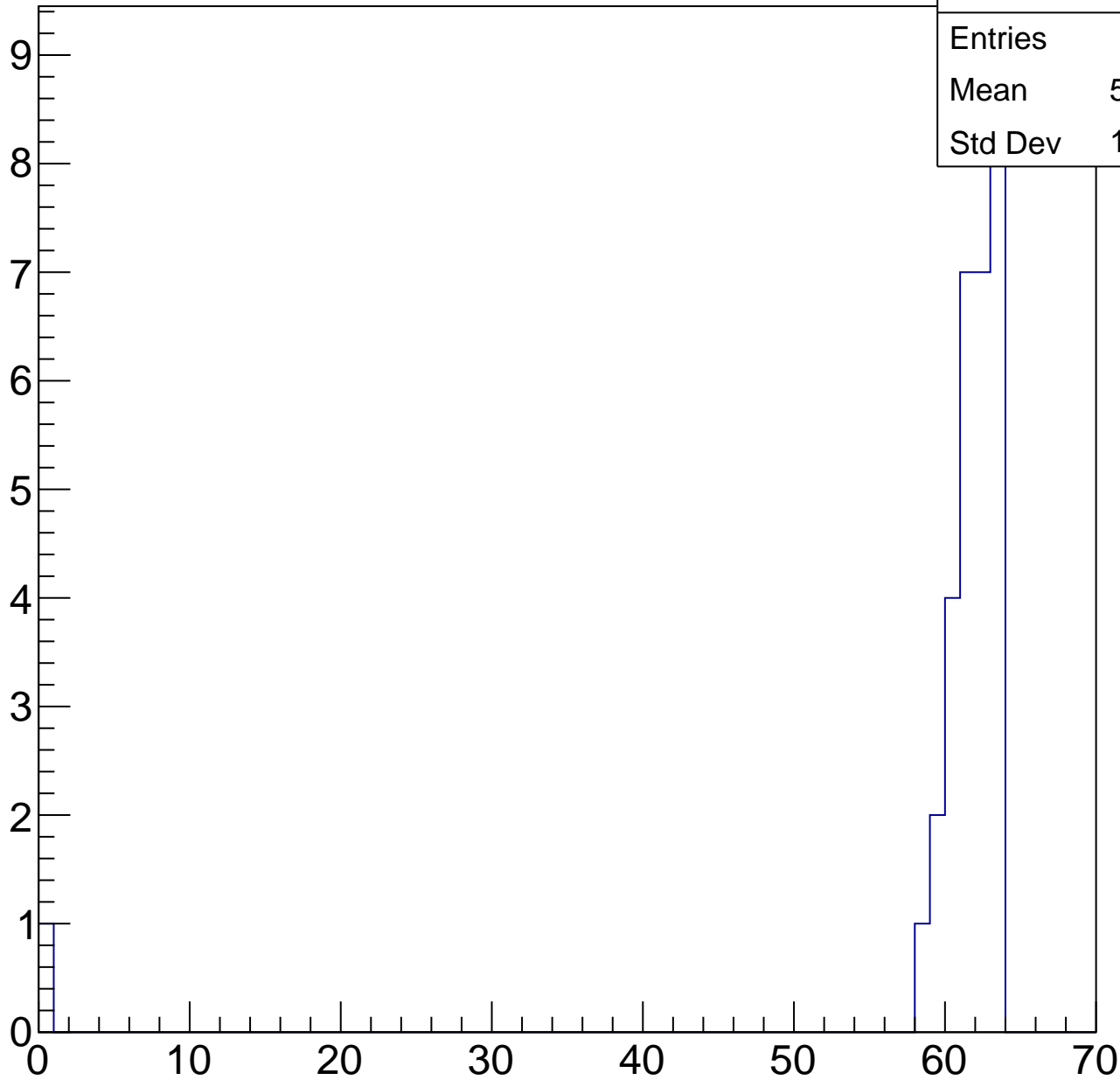
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	31
Mean	59.48
Std Dev	10.95

ampl



# B0L002S, U2-ch13, adc6

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



Entries	0
Mean	0
Std Dev	0



# B0L002S, U2-ch13, adc7

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L002S, U2-ch14, adc0

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entries	63
Mean	31.16
Std Dev	2.891

**Gaus mean : 31.4081**

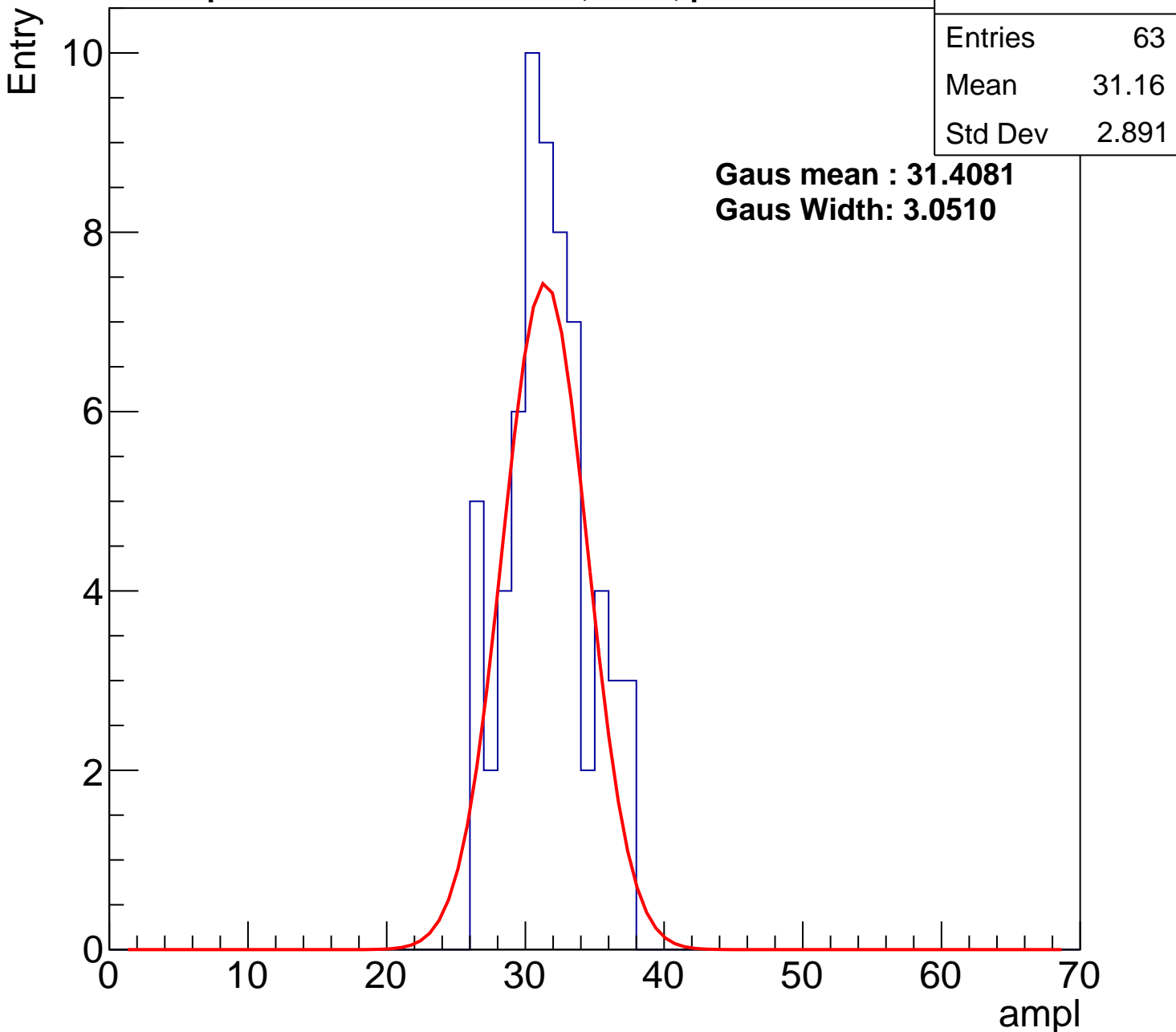
**Gaus Width: 3.0510**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L002S, U2-ch14, adc1

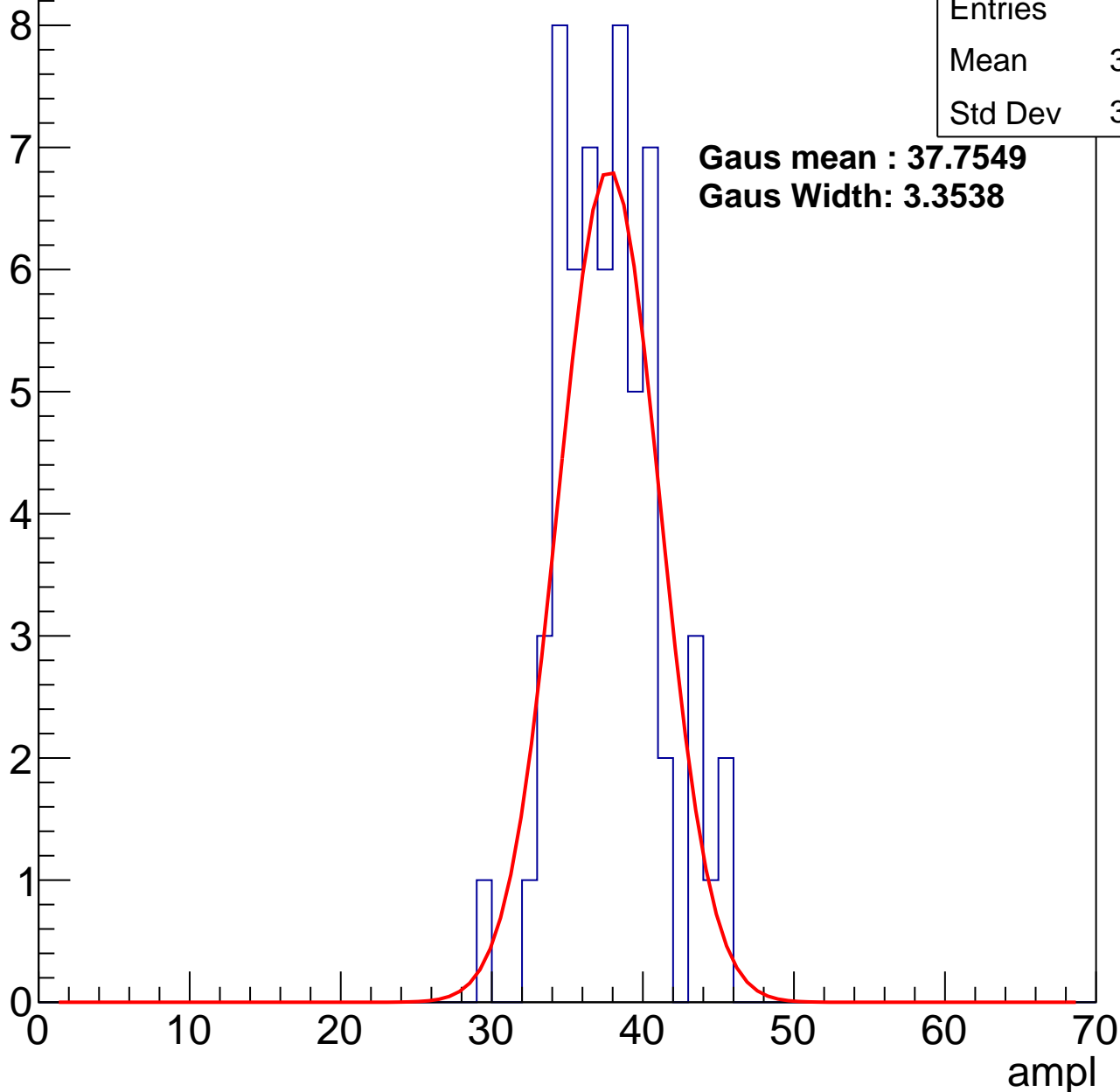
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	60
Mean	37.33
Std Dev	3.269

**Gaus mean : 37.7549**

**Gaus Width: 3.3538**



# B0L002S, U2-ch14, adc2

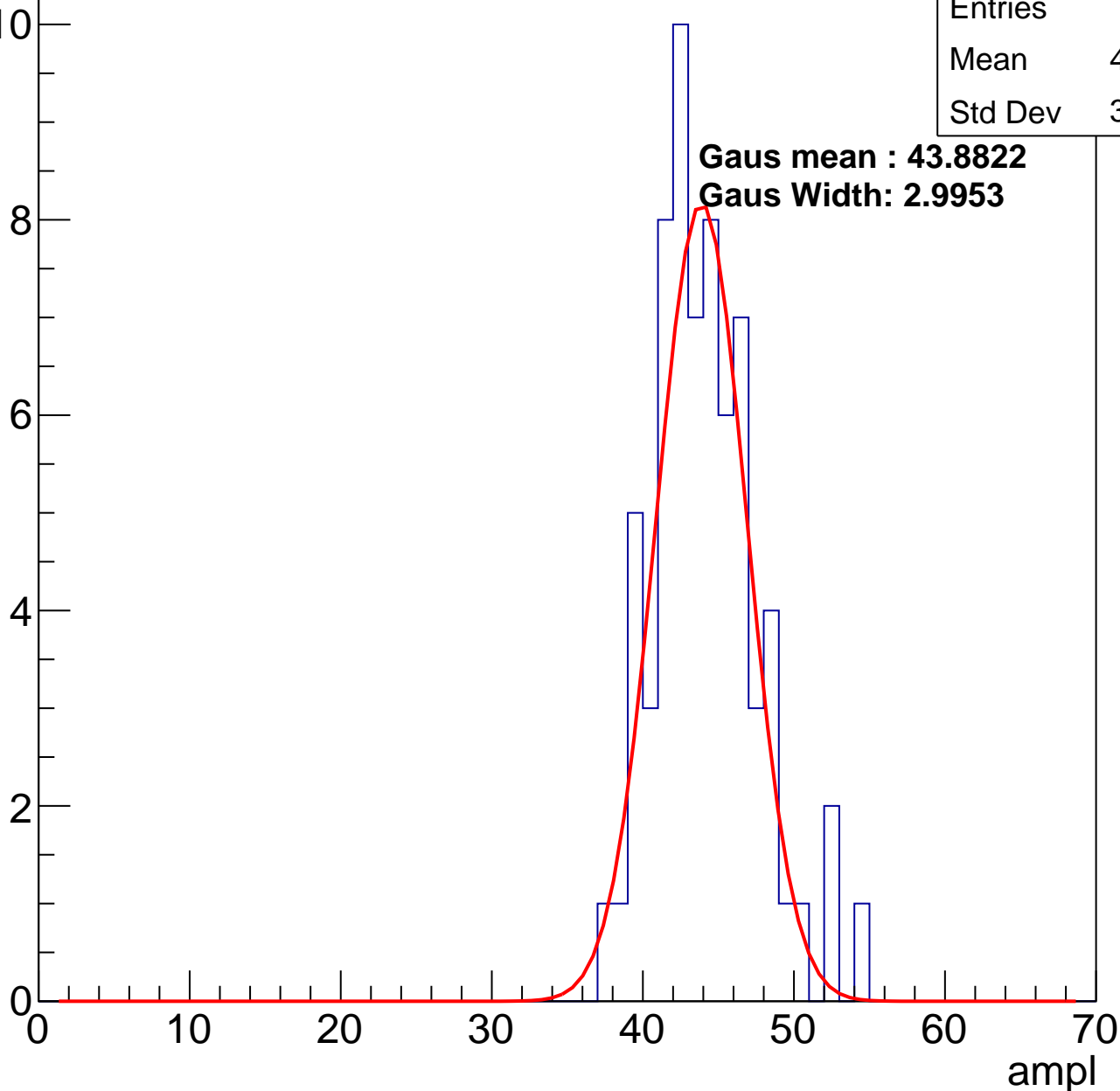
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	68
Mean	43.72
Std Dev	3.399

**Gaus mean : 43.8822**

**Gaus Width: 2.9953**

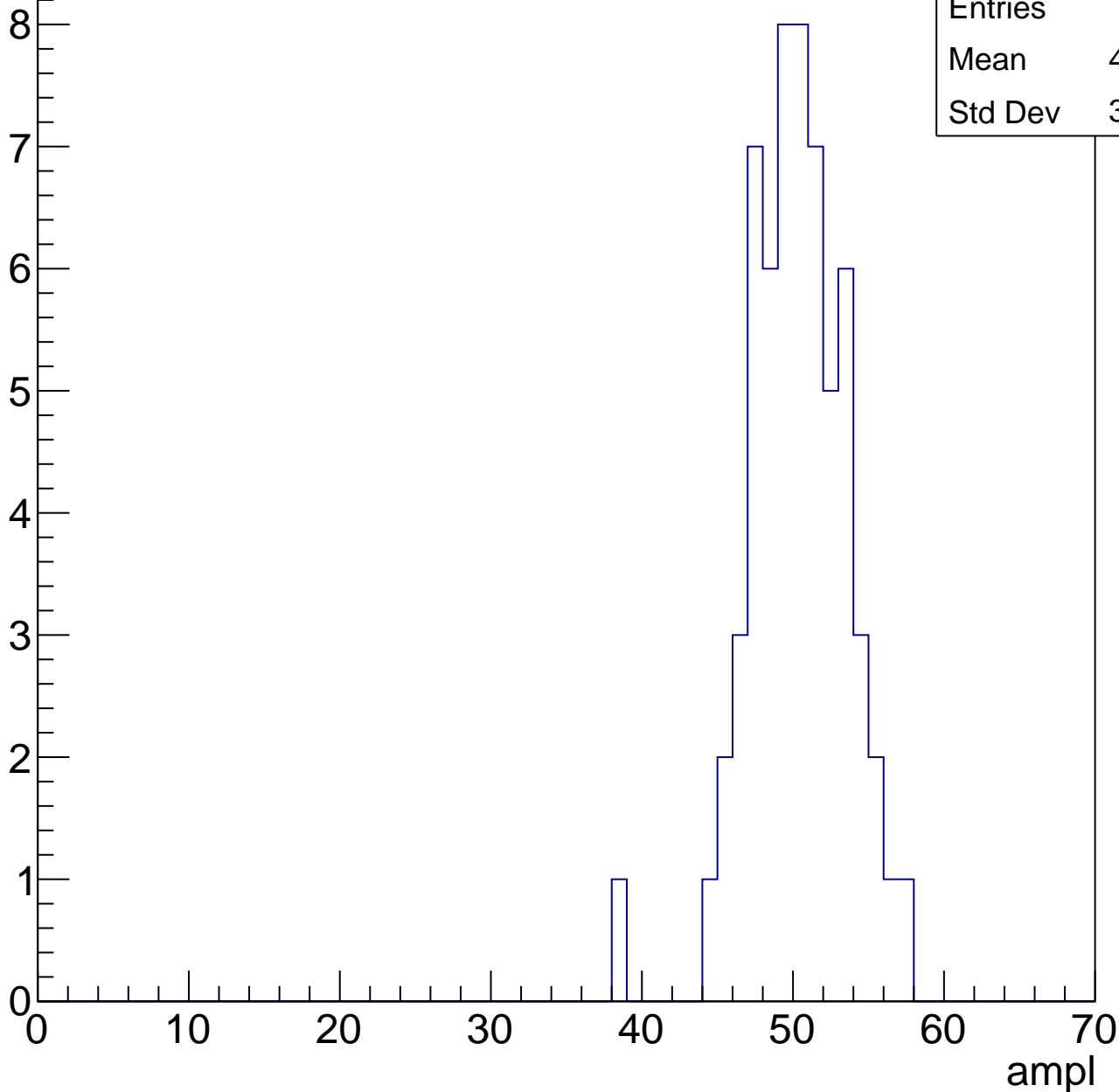


# B0L002S, U2-ch14, adc3

calib\_packv5\_042523\_0143.root, FC#8, port C1

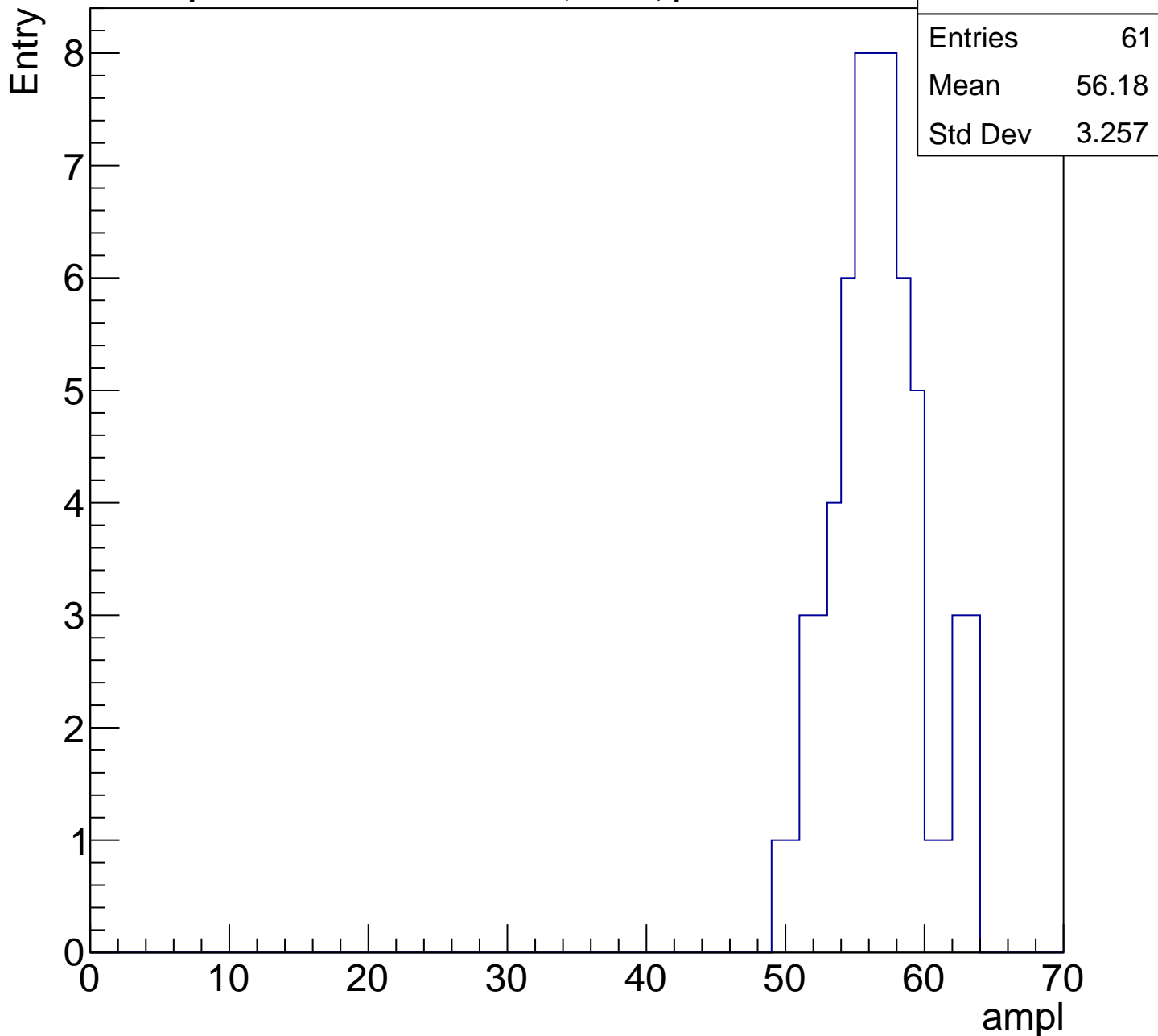
Entry

Entries	61
Mean	49.82
Std Dev	3.226



# B0L002S, U2-ch14, adc4

calib\_packv5\_042523\_0143.root, FC#8, port C1



# B0L002S, U2-ch14, adc5

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	37
Mean	58.68
Std Dev	9.921

ampl

0

10

20

30

40

50

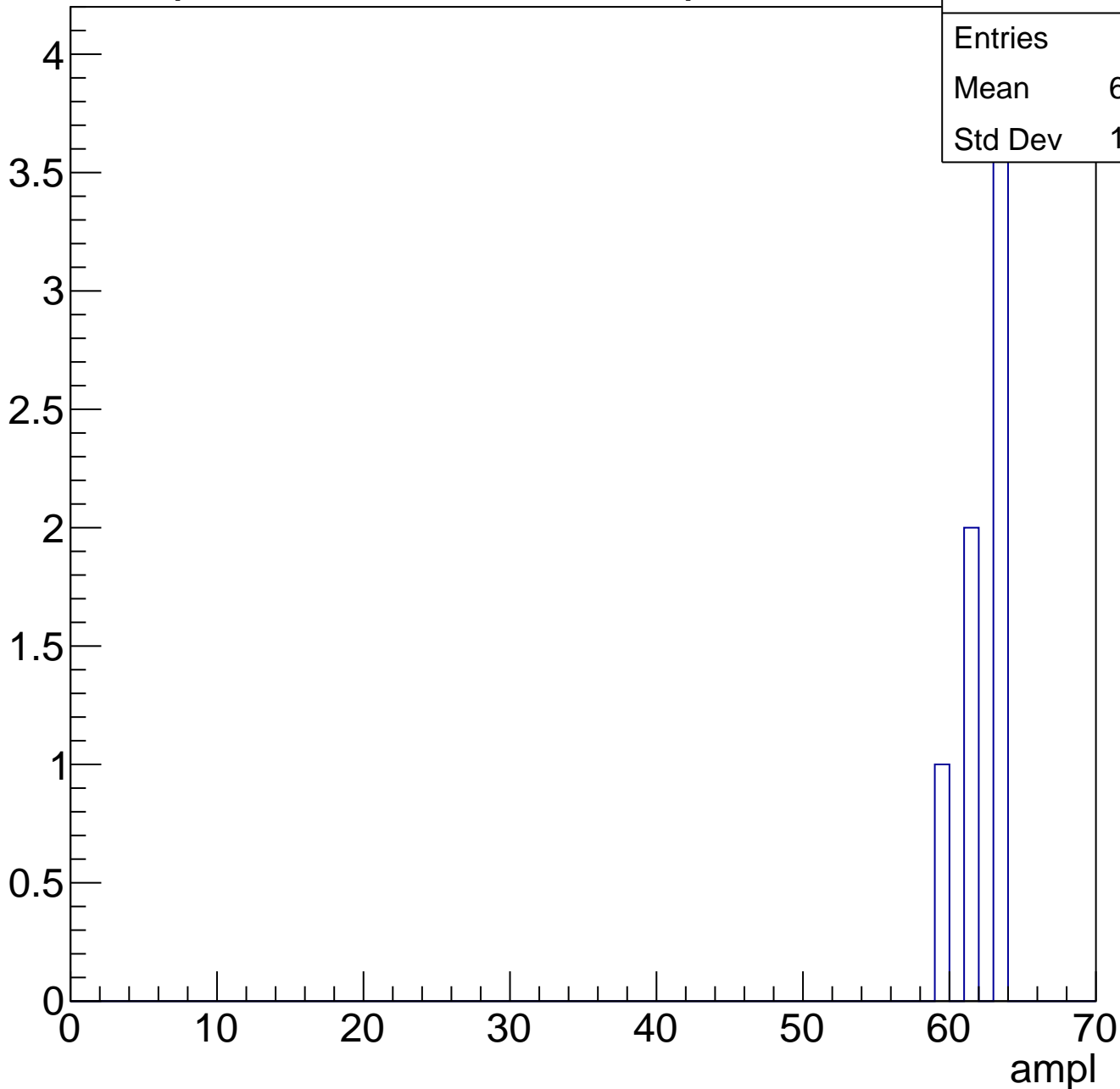
60

70

# B0L002S, U2-ch14, adc6

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry





# B0L002S, U2-ch14, adc7

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



Entries	2
Mean	12
Std Dev	12

# B0L002S, U2-ch15, adc0

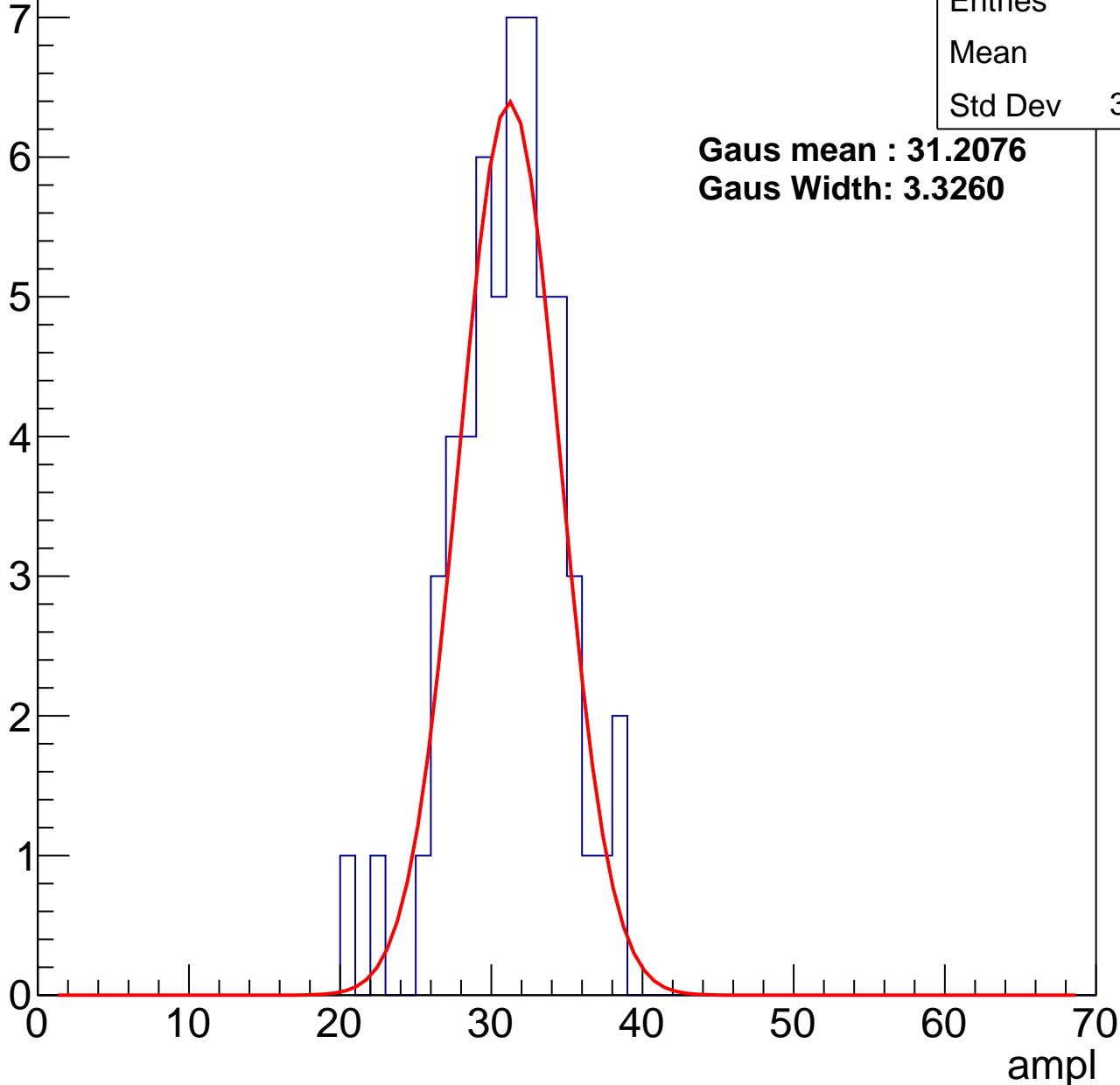
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	56
Mean	30.7
Std Dev	3.575

**Gaus mean : 31.2076**

**Gaus Width: 3.3260**



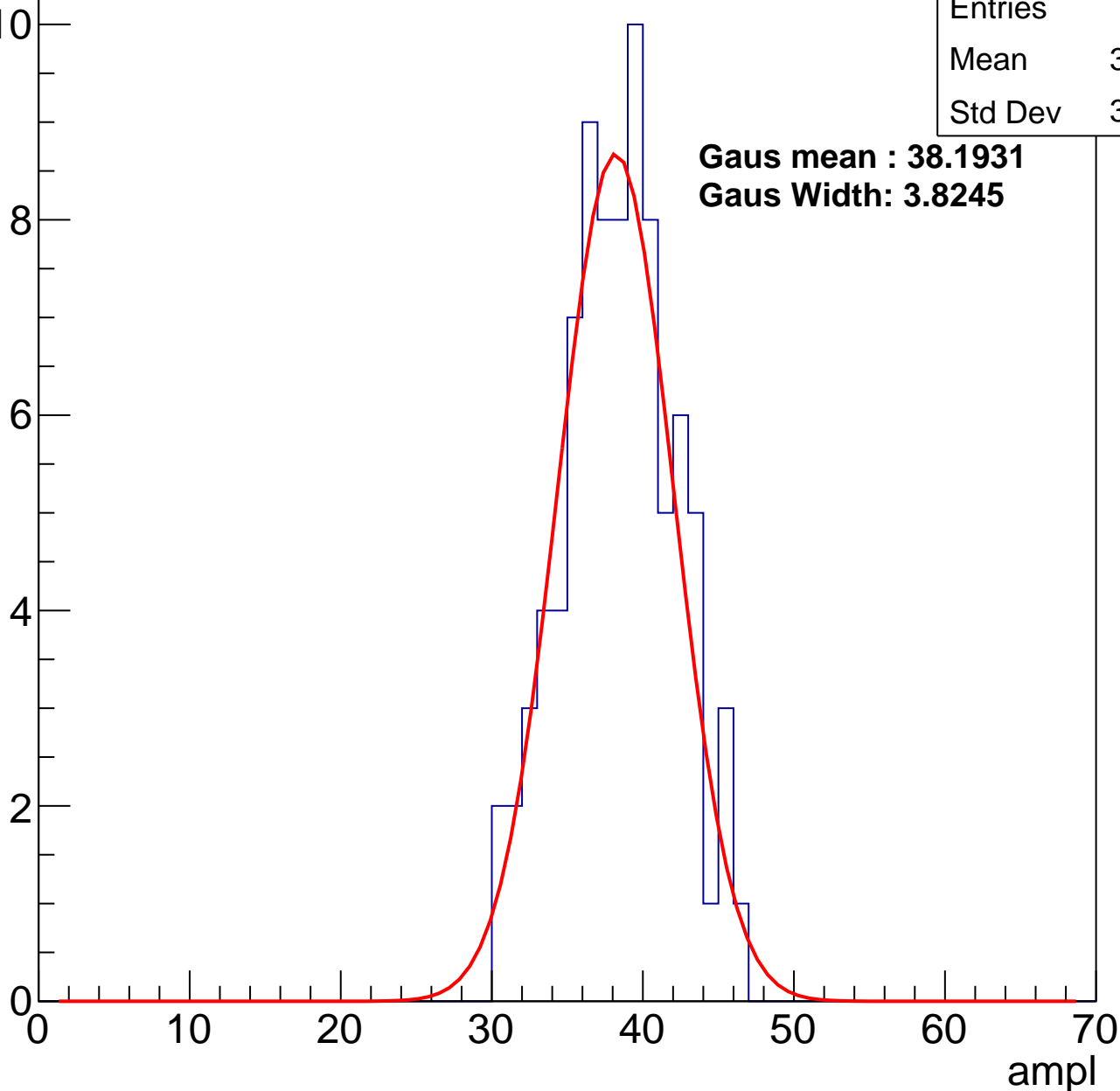
# B0L002S, U2-ch15, adc1

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

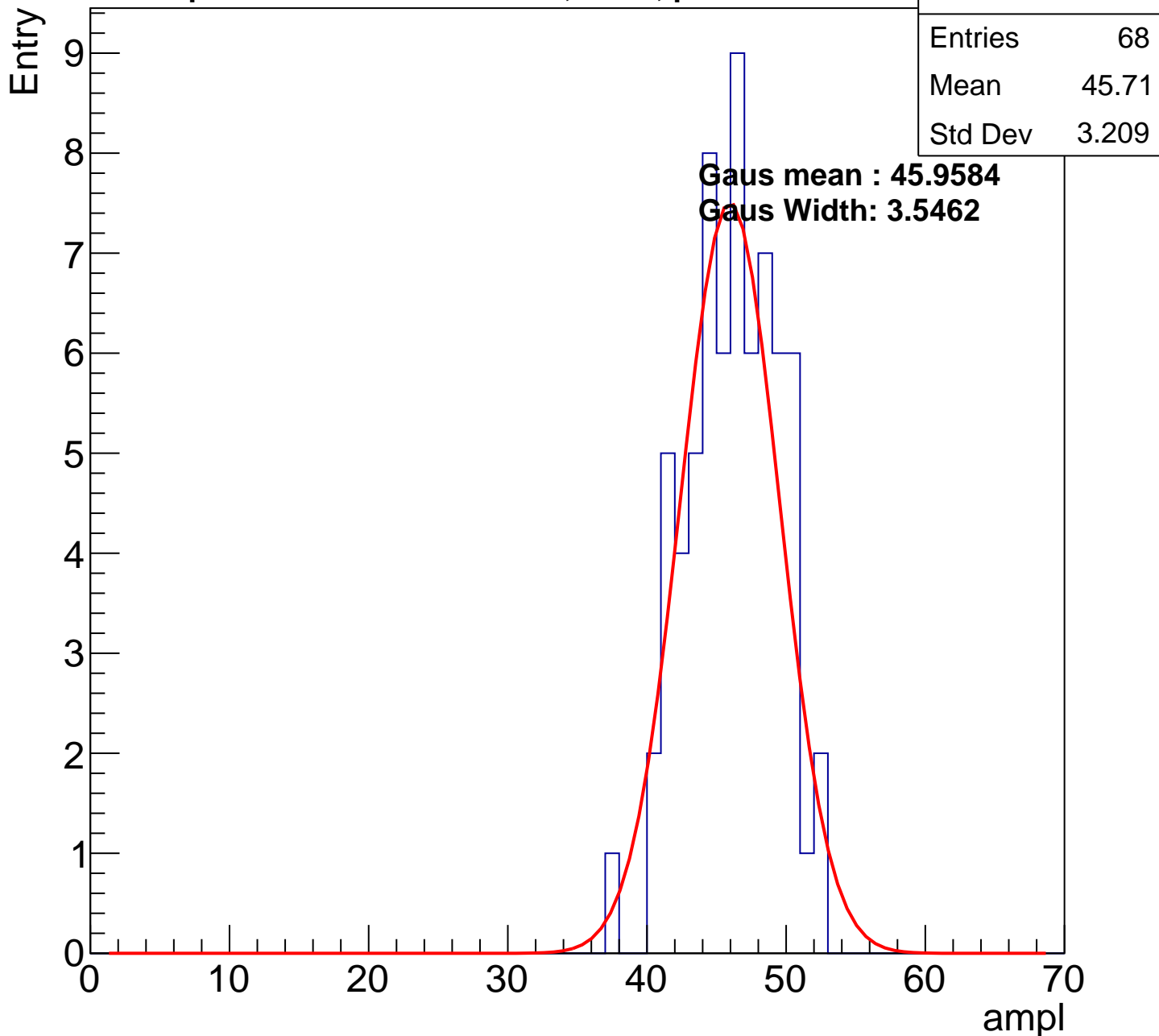
Entries	86
Mean	37.93
Std Dev	3.672

**Gaus mean : 38.1931**  
**Gaus Width: 3.8245**



# B0L002S, U2-ch15, adc2

calib\_packv5\_042523\_0143.root, FC#8, port C1

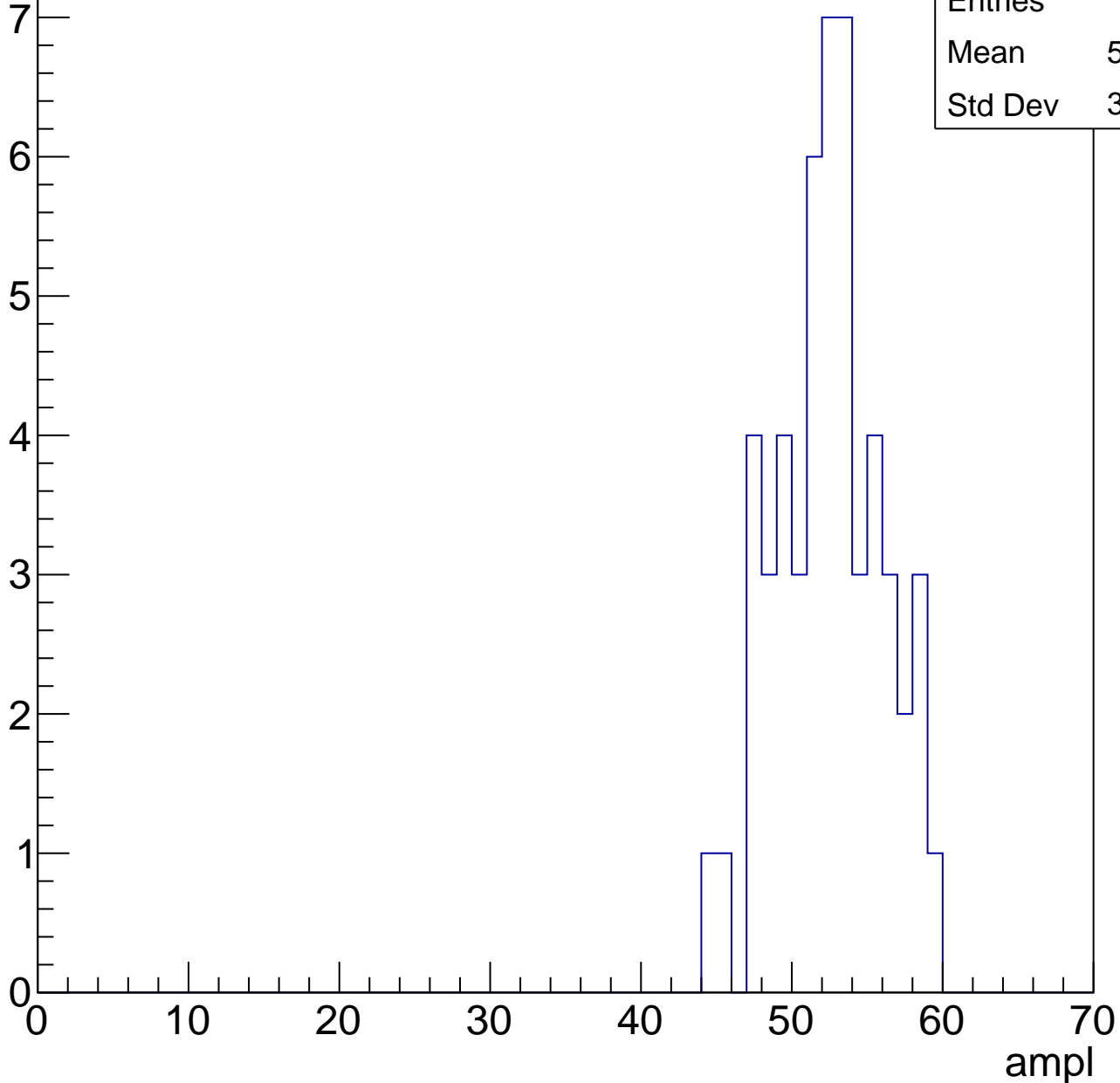


# B0L002S, U2-ch15, adc3

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	52
Mean	52.02
Std Dev	3.467

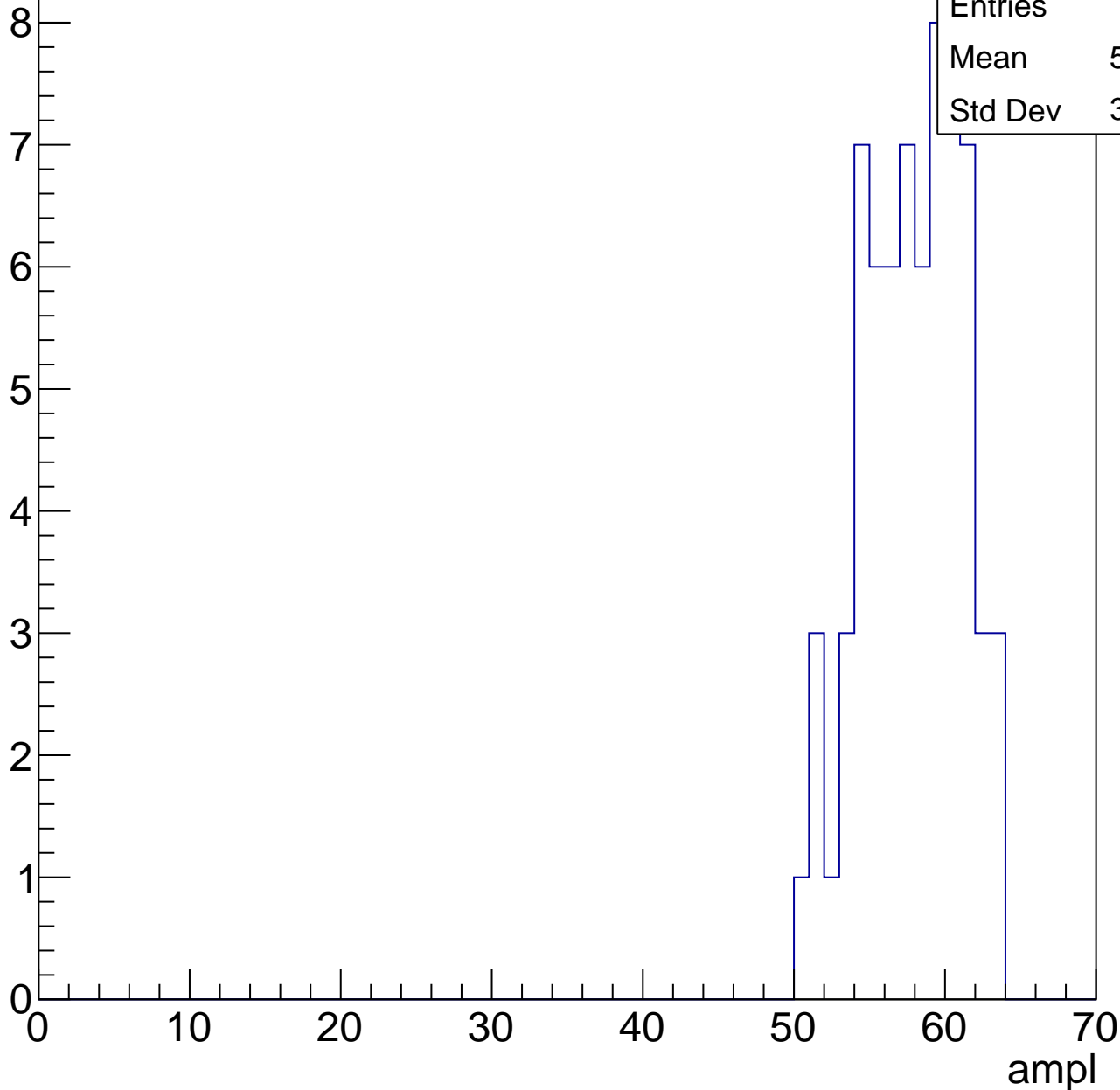


# B0L002S, U2-ch15, adc4

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	69
Mean	57.38
Std Dev	3.226

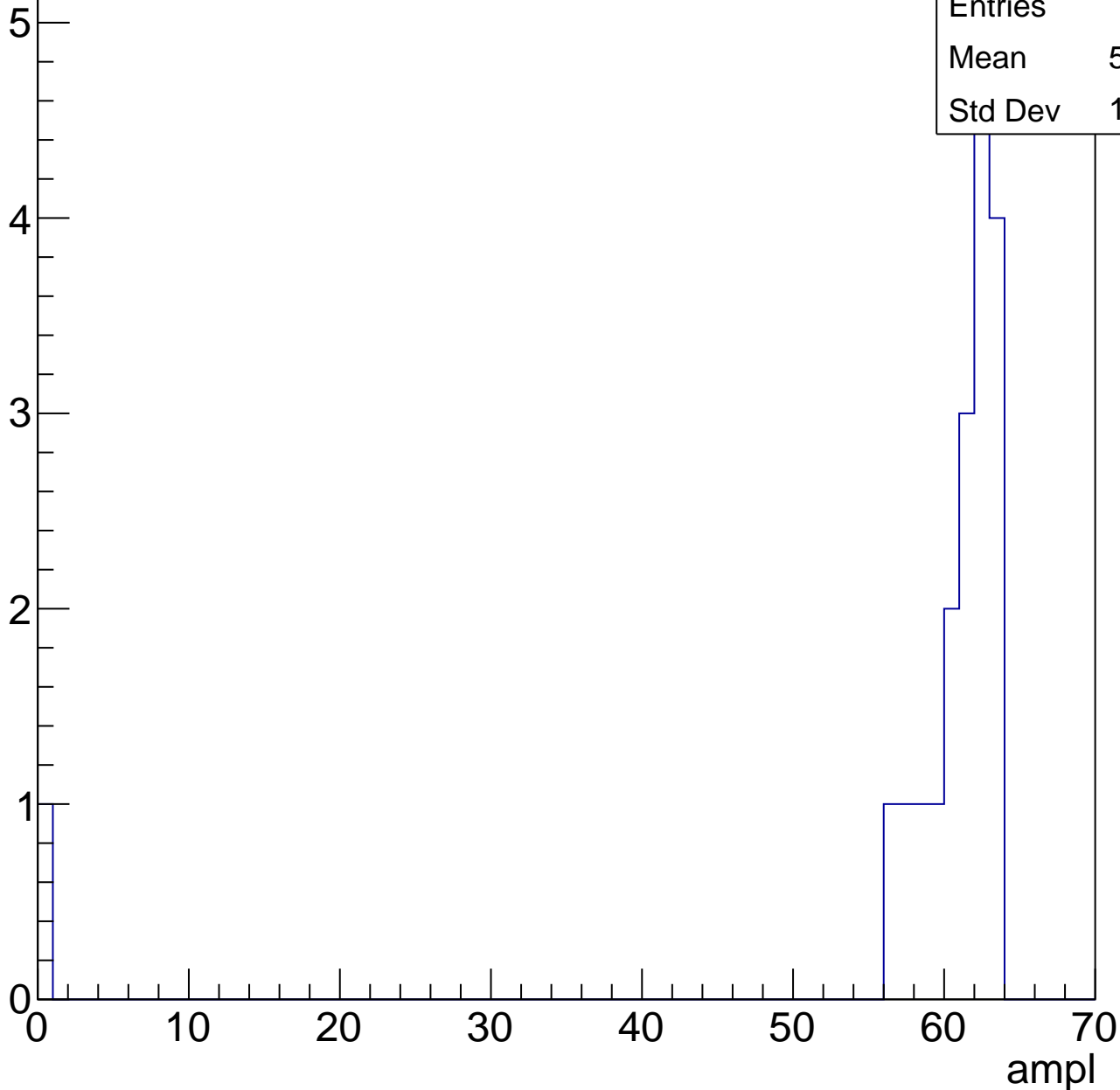


# B0L002S, U2-ch15, adc5

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	19
Mean	57.63
Std Dev	13.73



# B0L002S, U2-ch15, adc6

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry





# B0L002S, U2-ch15, adc7

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



# B0L002S, U2-ch16, adc0

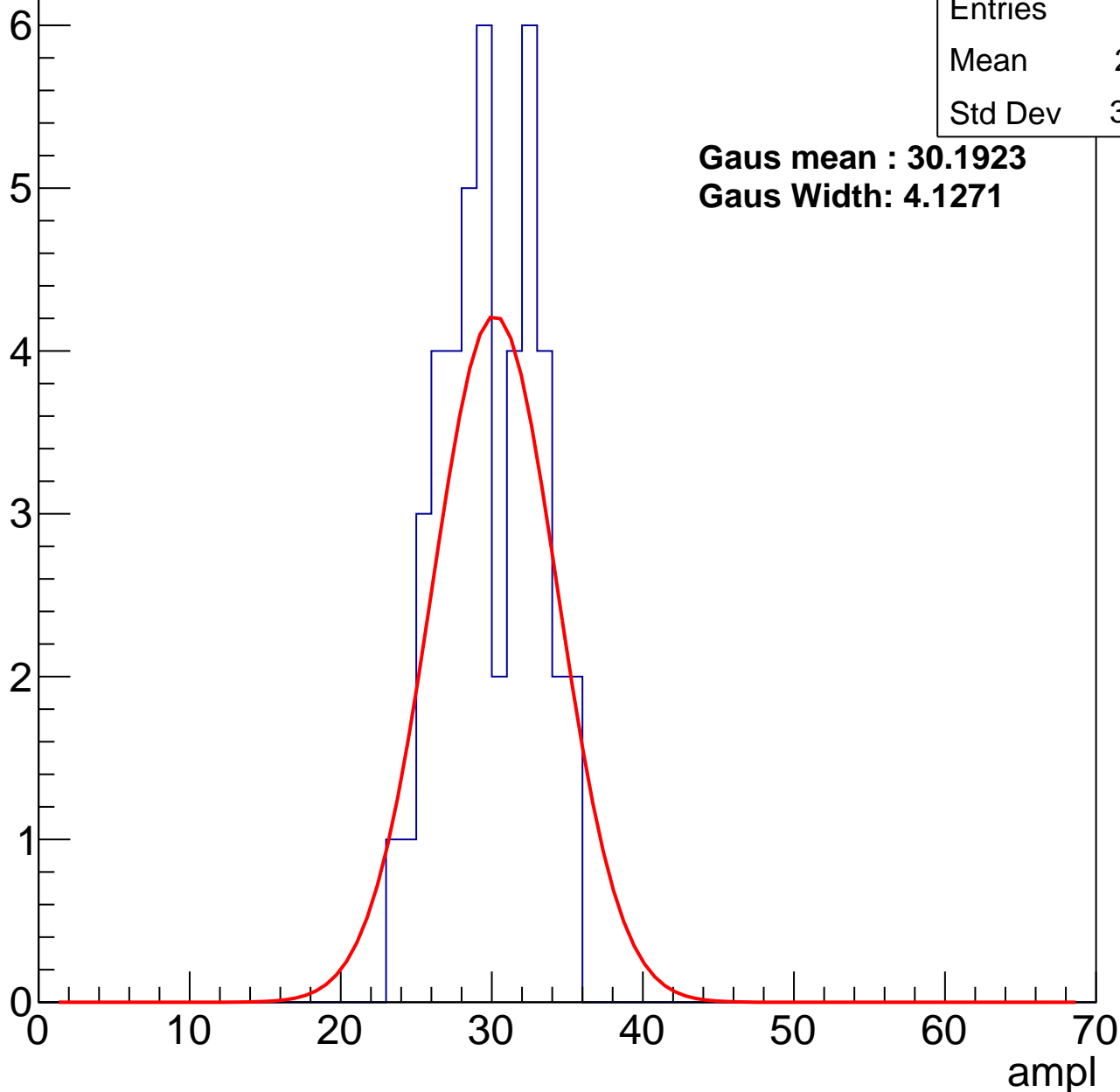
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	44
Mean	29.41
Std Dev	3.077

**Gaus mean : 30.1923**

**Gaus Width: 4.1271**



# B0L002S, U2-ch16, adc1

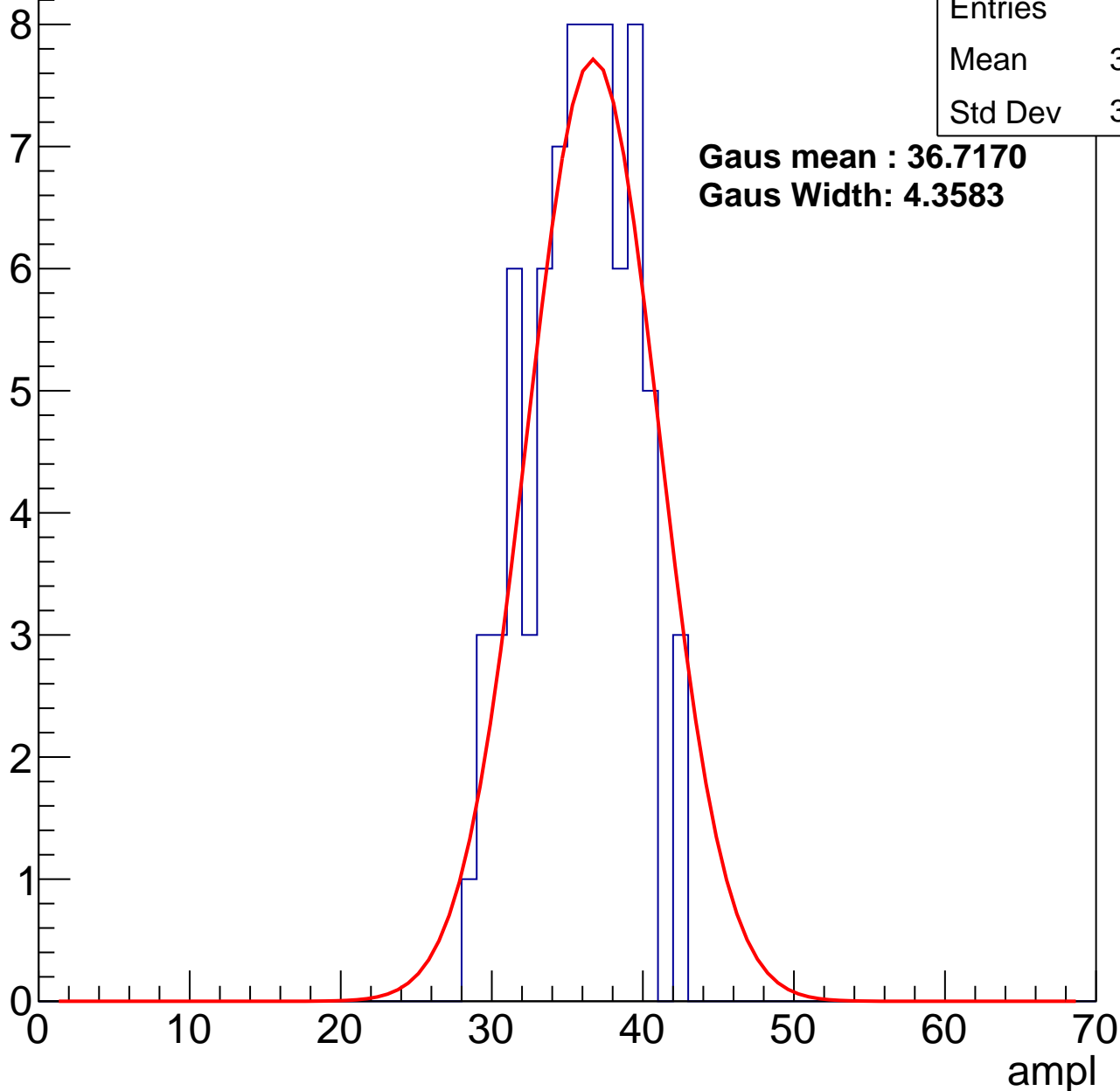
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	75
Mean	35.37
Std Dev	3.405

**Gaus mean : 36.7170**

**Gaus Width: 4.3583**



# B0L002S, U2-ch16, adc2

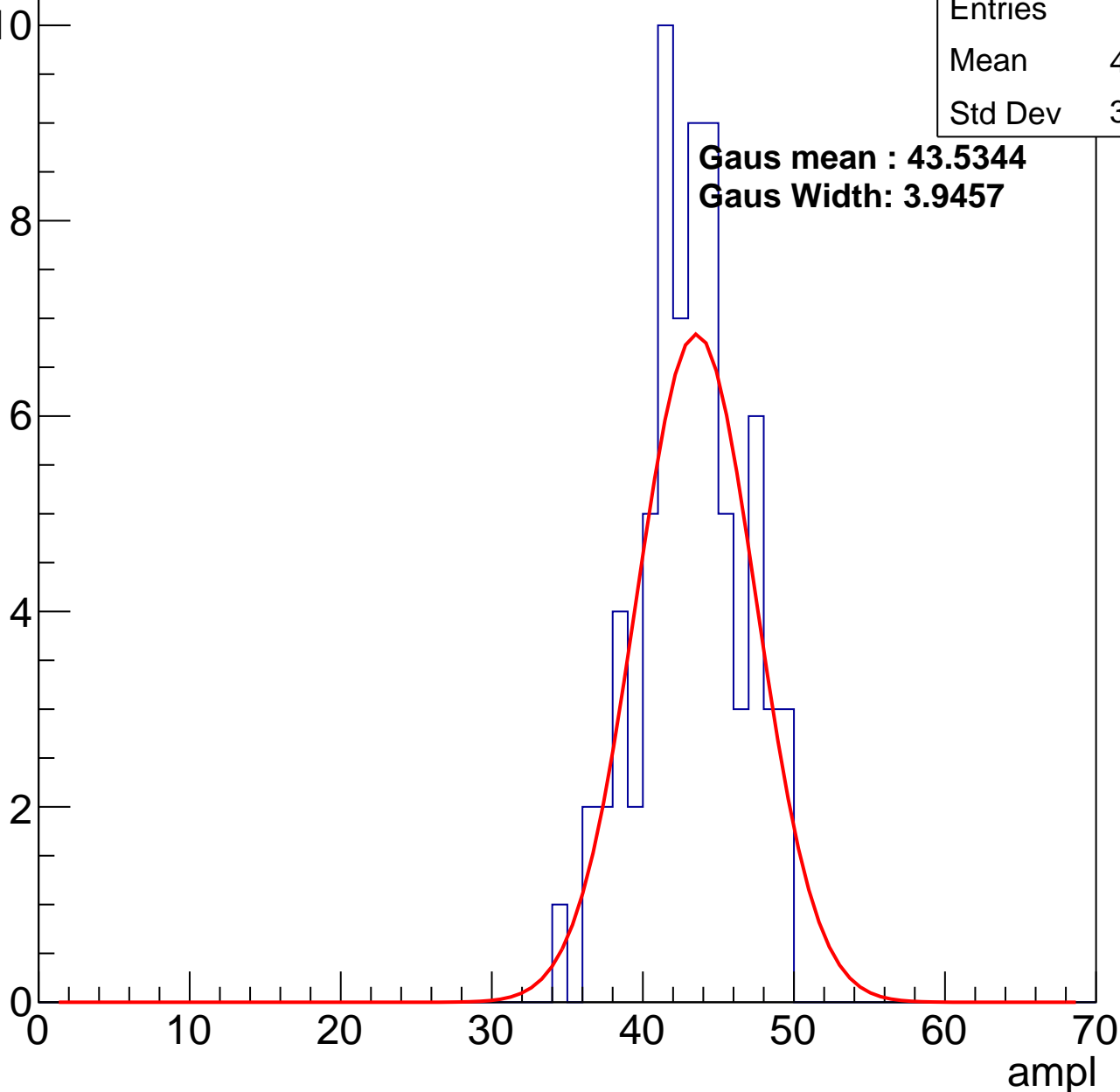
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	71
Mean	42.72
Std Dev	3.366

**Gaus mean : 43.5344**

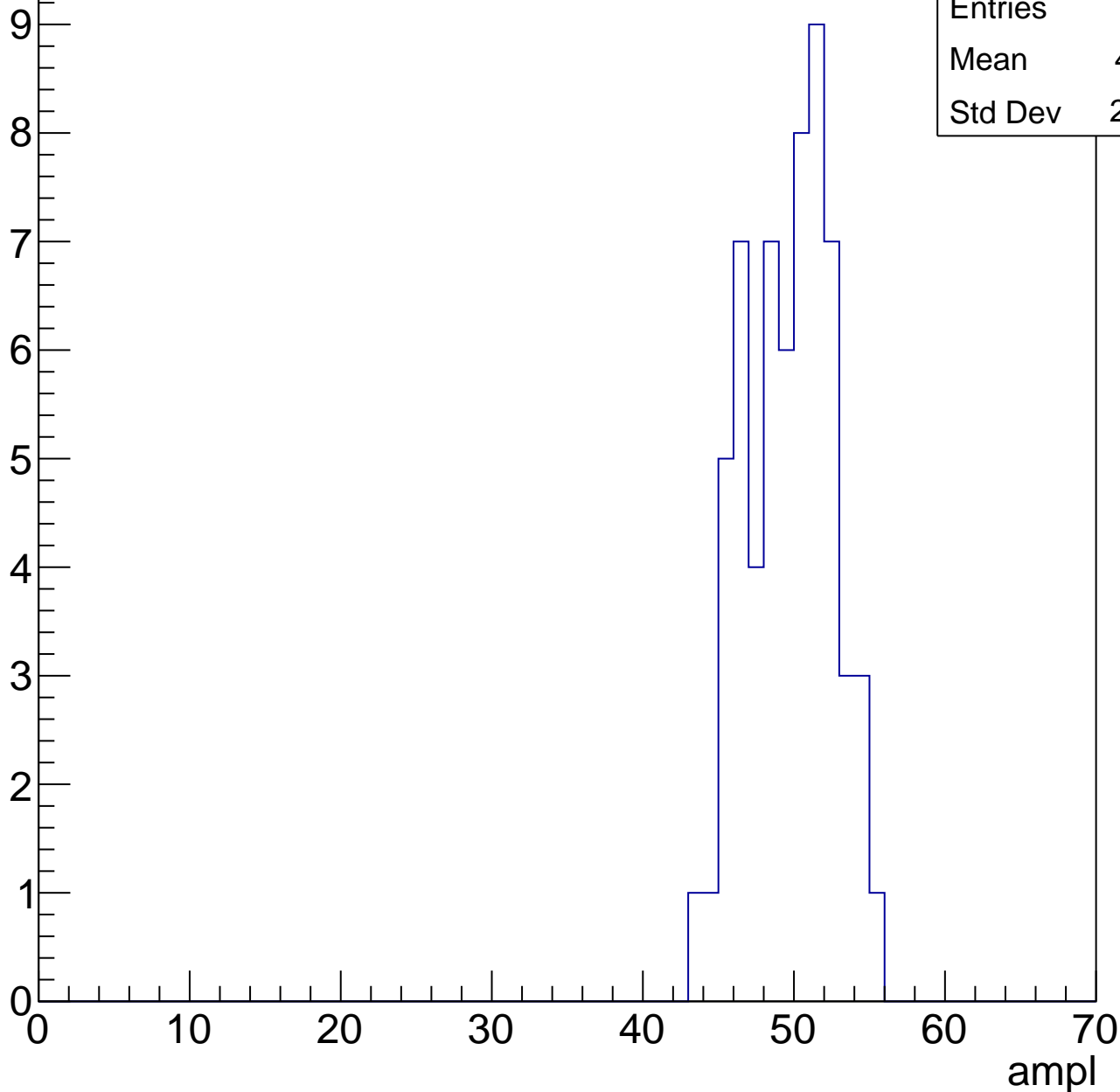
**Gaus Width: 3.9457**



# B0L002S, U2-ch16, adc3

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

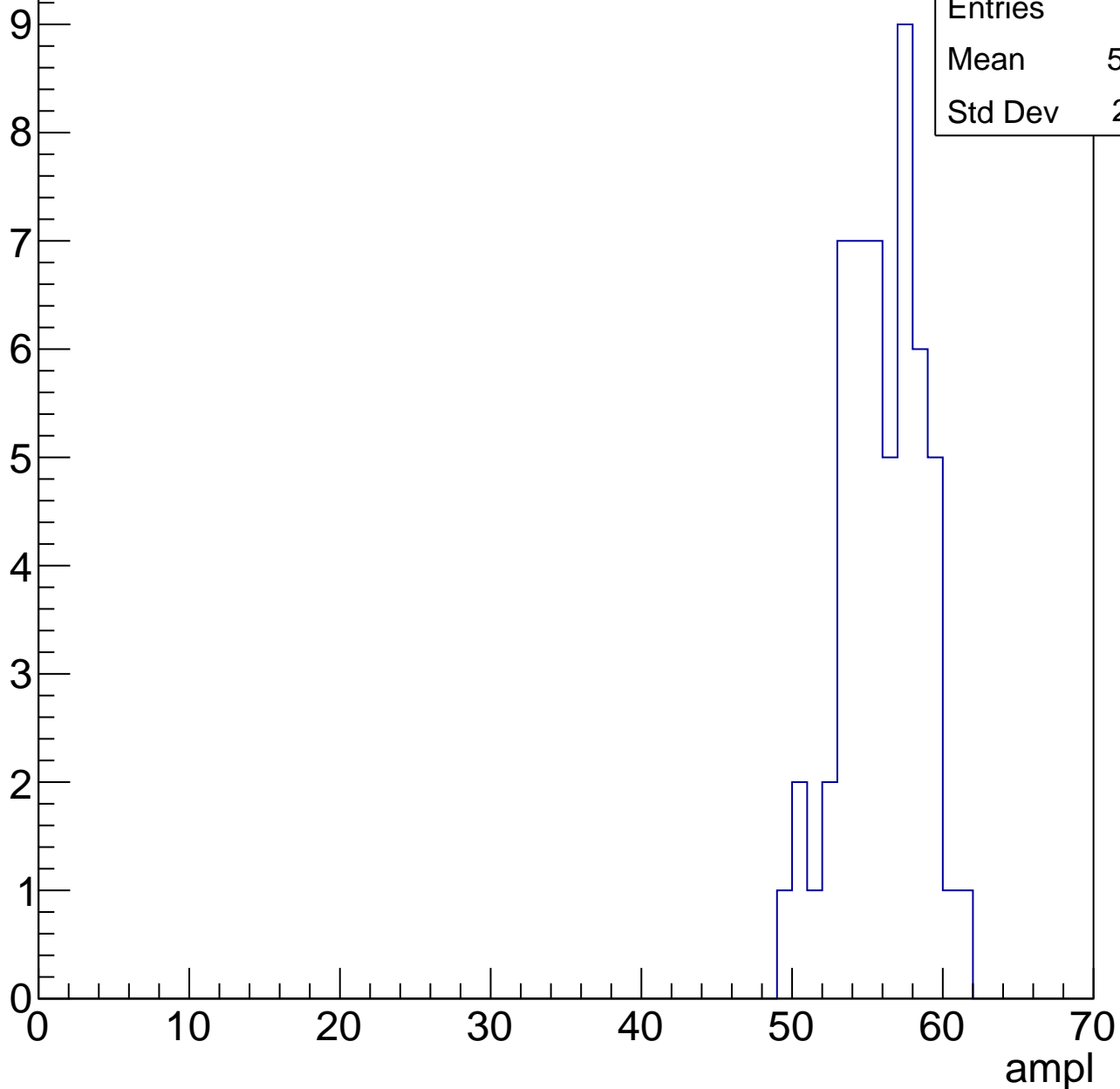


Entries	62
Mean	49.21
Std Dev	2.812

# B0L002S, U2-ch16, adc4

calib\_packv5\_042523\_0143.root, FC#8, port C1

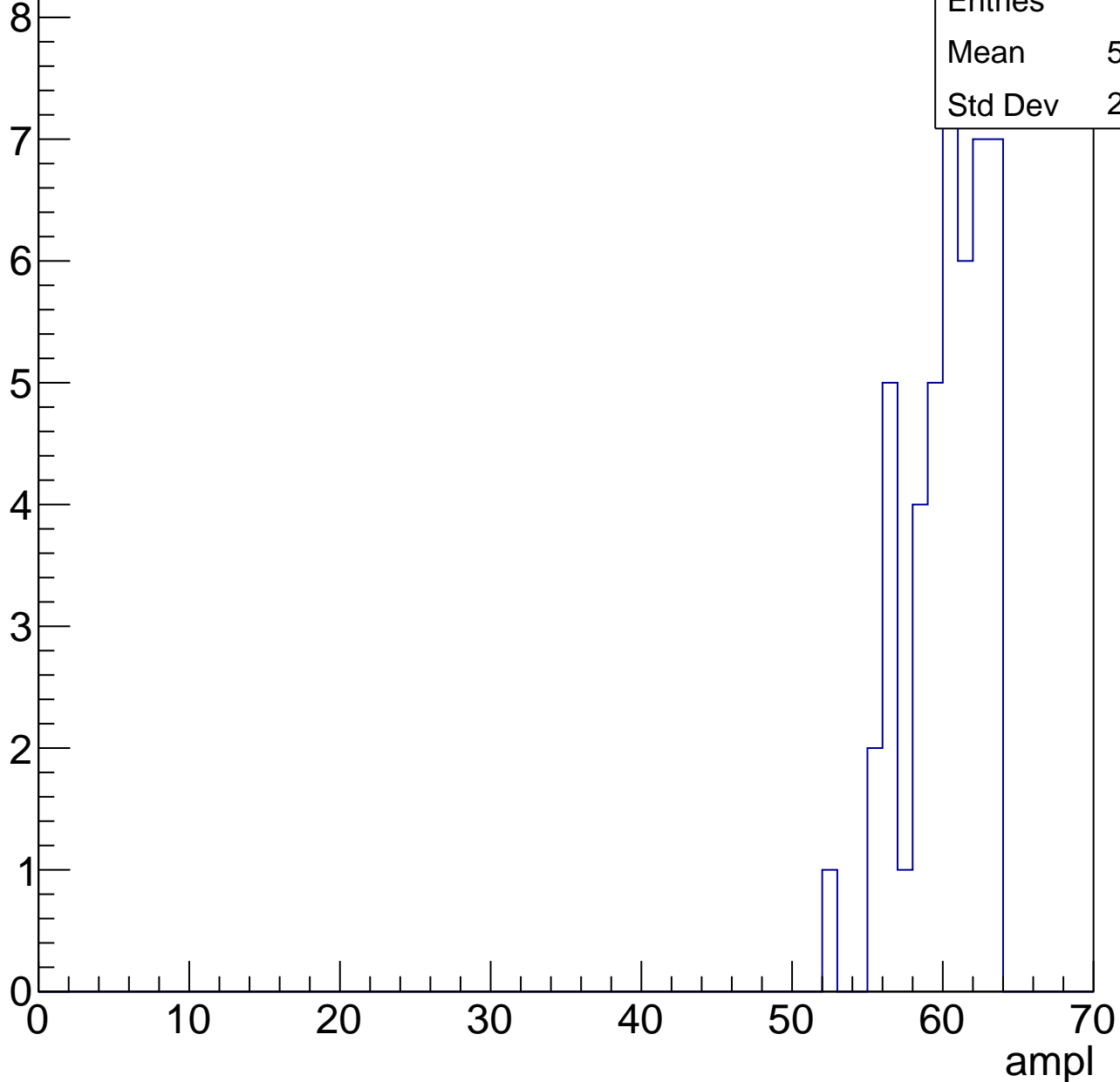
Entry



# B0L002S, U2-ch16, adc5

calib\_packv5\_042523\_0143.root, FC#8, port C1

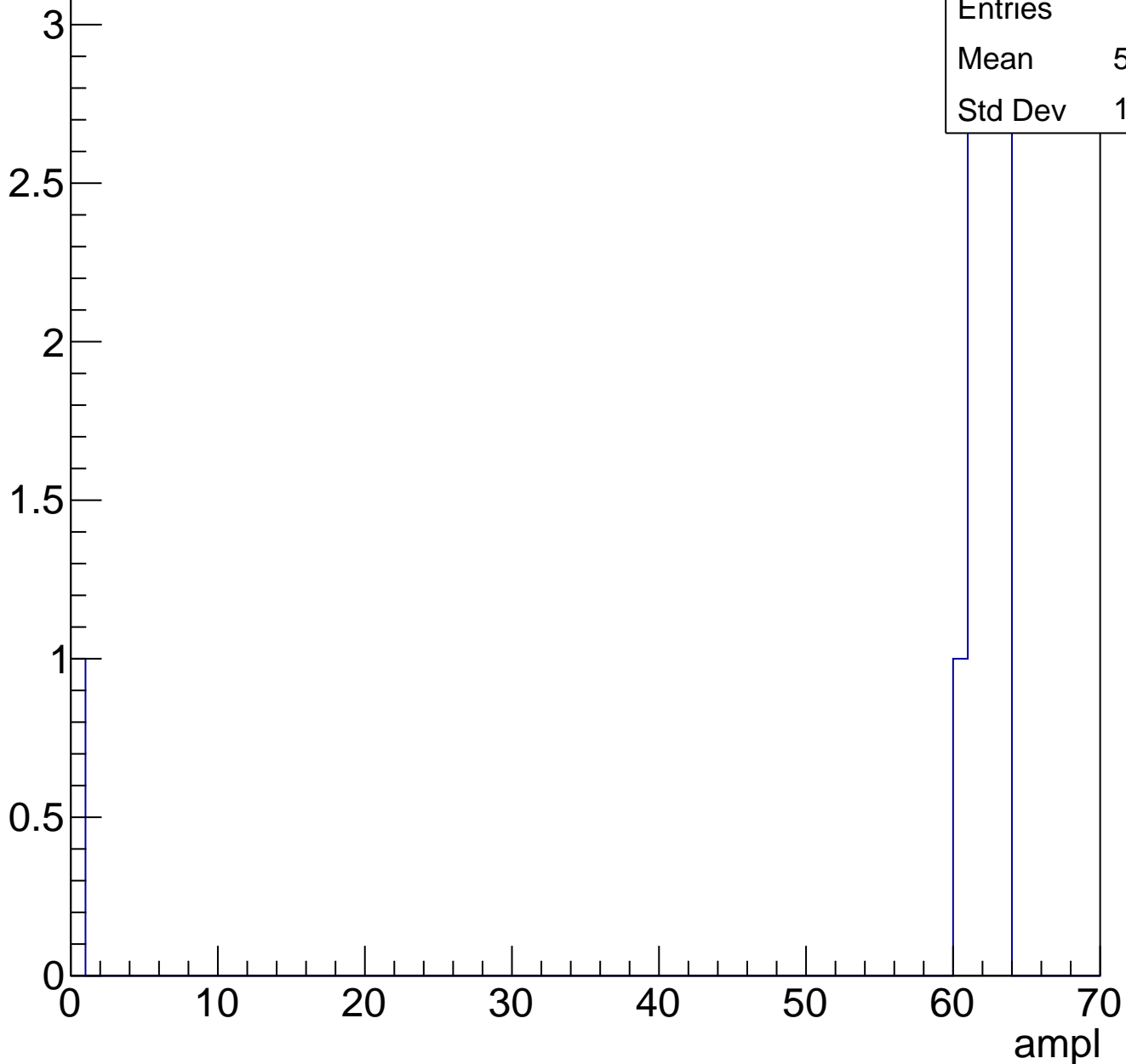
Entry



# B0L002S, U2-ch16, adc6

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

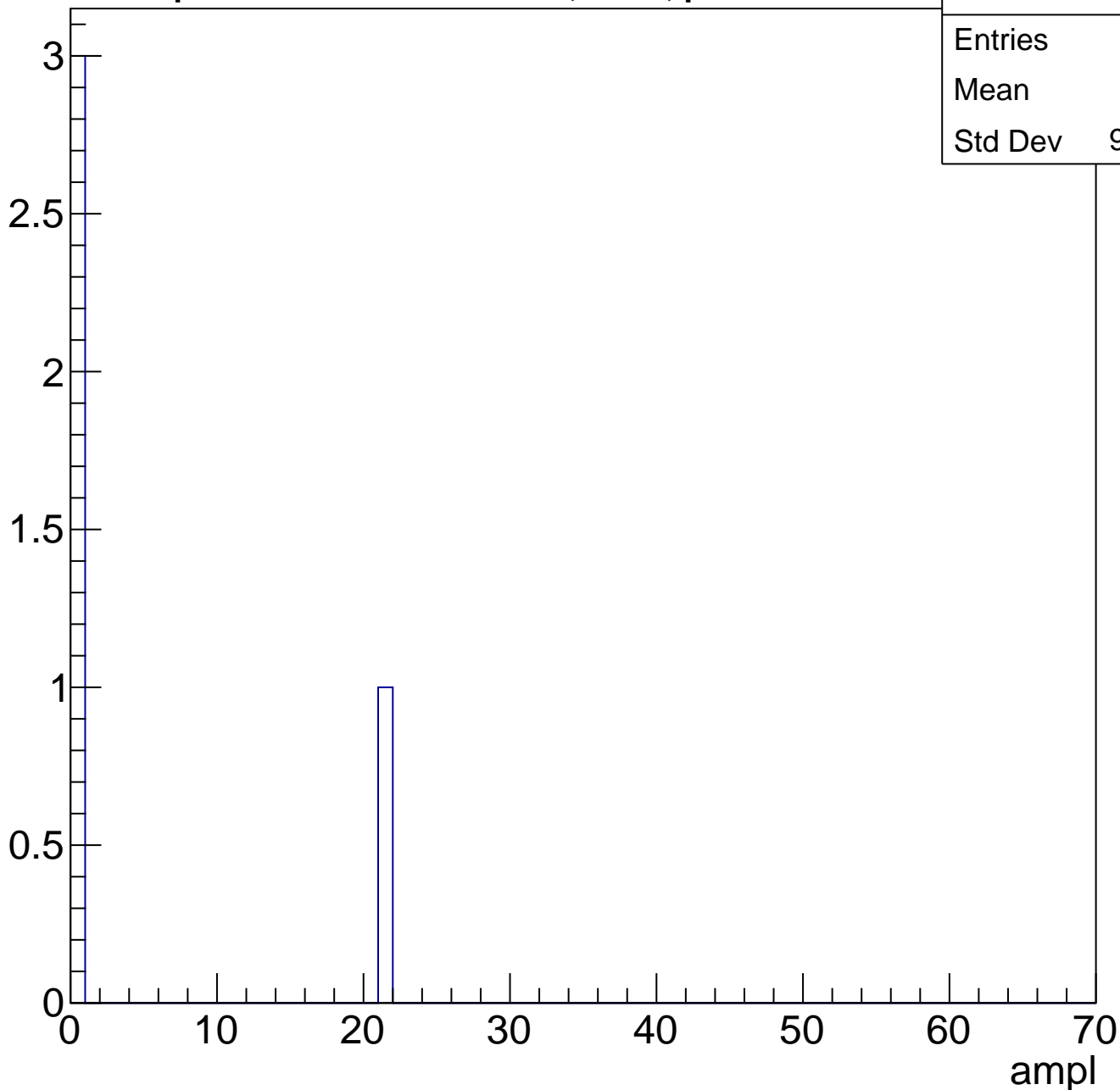




# B0L002S, U2-ch16, adc7

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



Entries	4
Mean	5.25
Std Dev	9.093

# B0L002S, U2-ch17, adc0

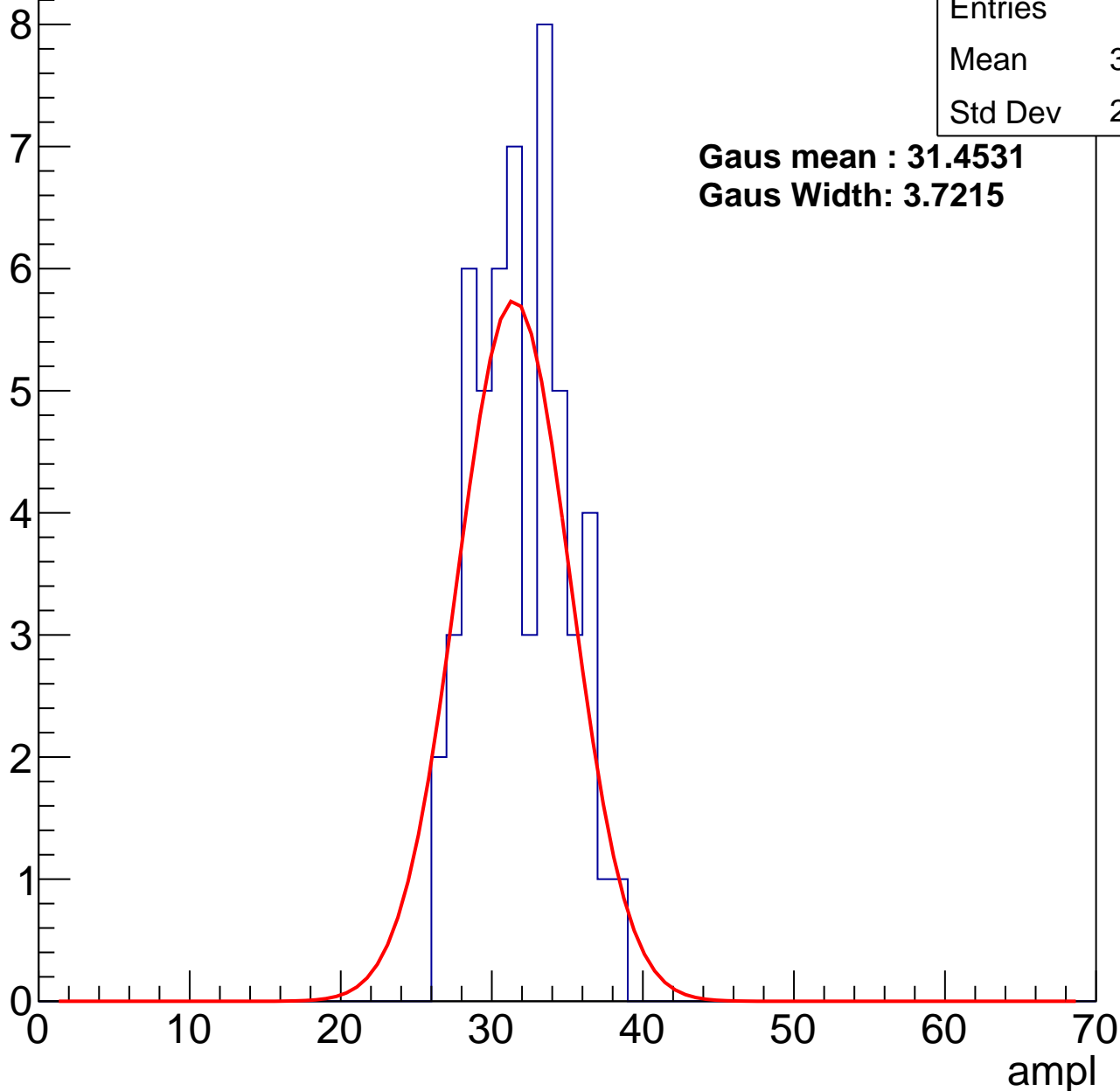
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	54
Mean	31.43
Std Dev	2.985

**Gaus mean : 31.4531**

**Gaus Width: 3.7215**



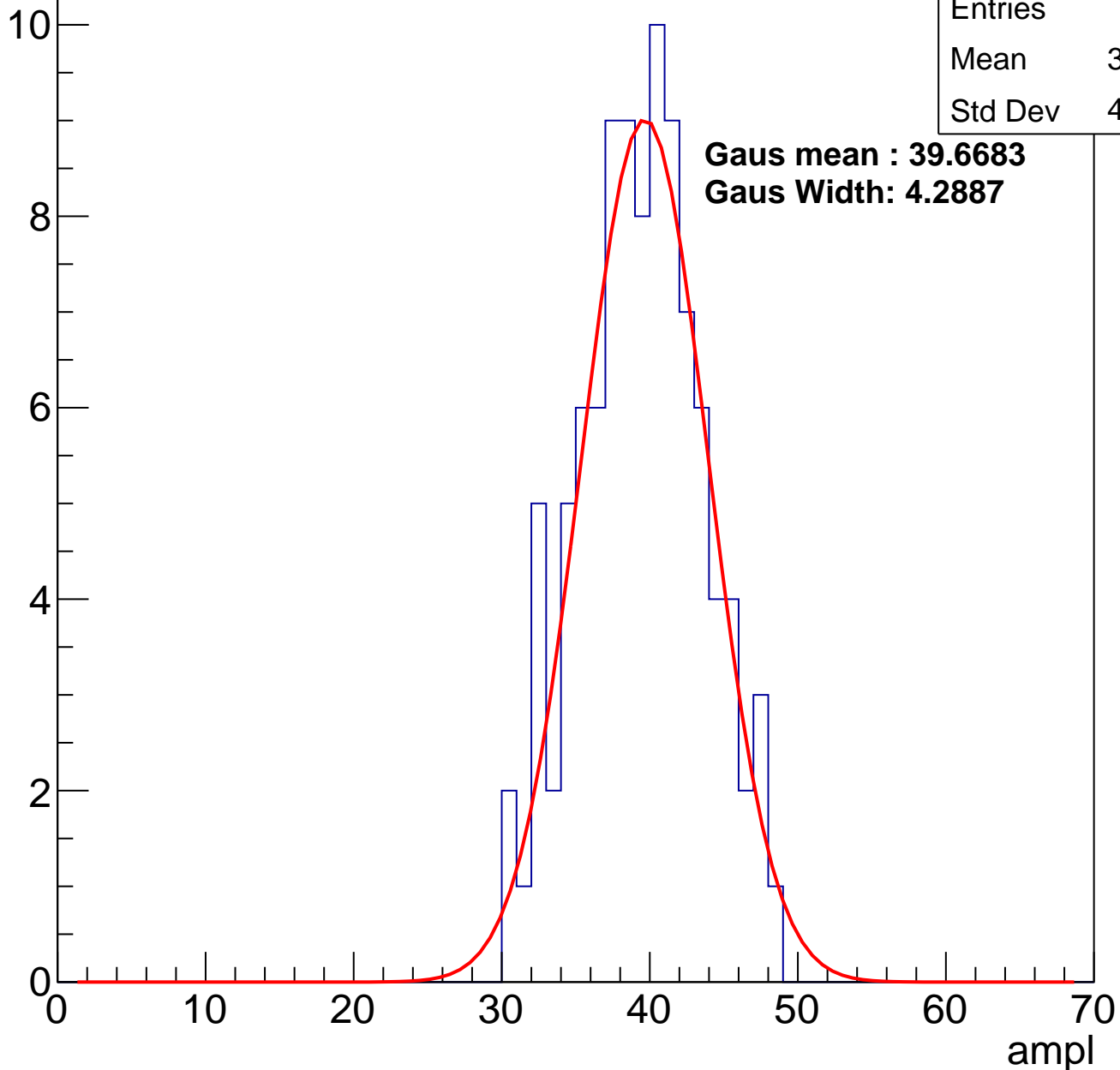
# B0L002S, U2-ch17, adc1

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entries	99
Mean	38.97
Std Dev	4.123

**Gaus mean : 39.6683**  
**Gaus Width: 4.2887**

Entry



# B0L002S, U2-ch17, adc2

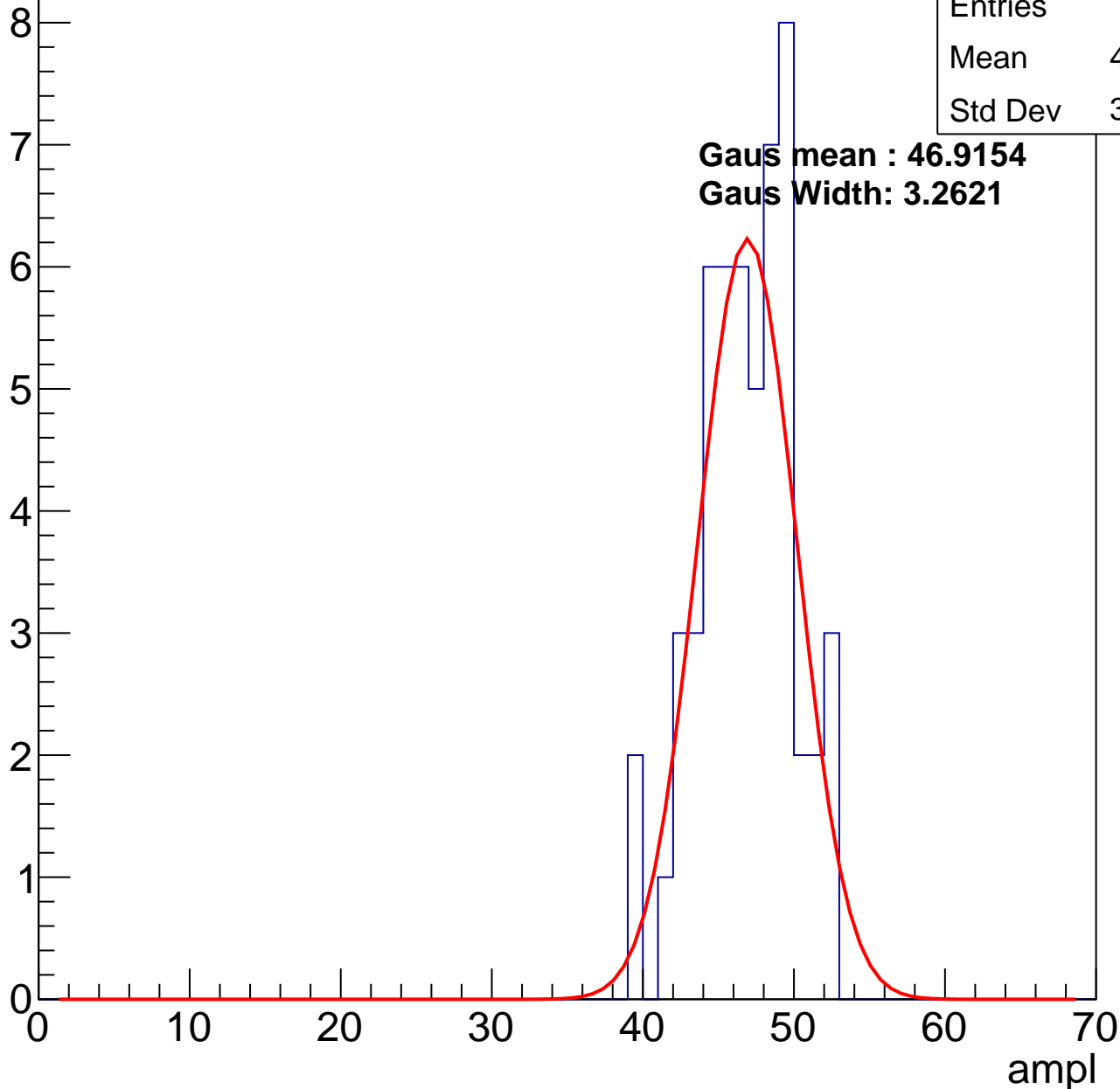
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	54
Mean	46.39
Std Dev	3.088

**Gaus mean : 46.9154**

**Gaus Width: 3.2621**

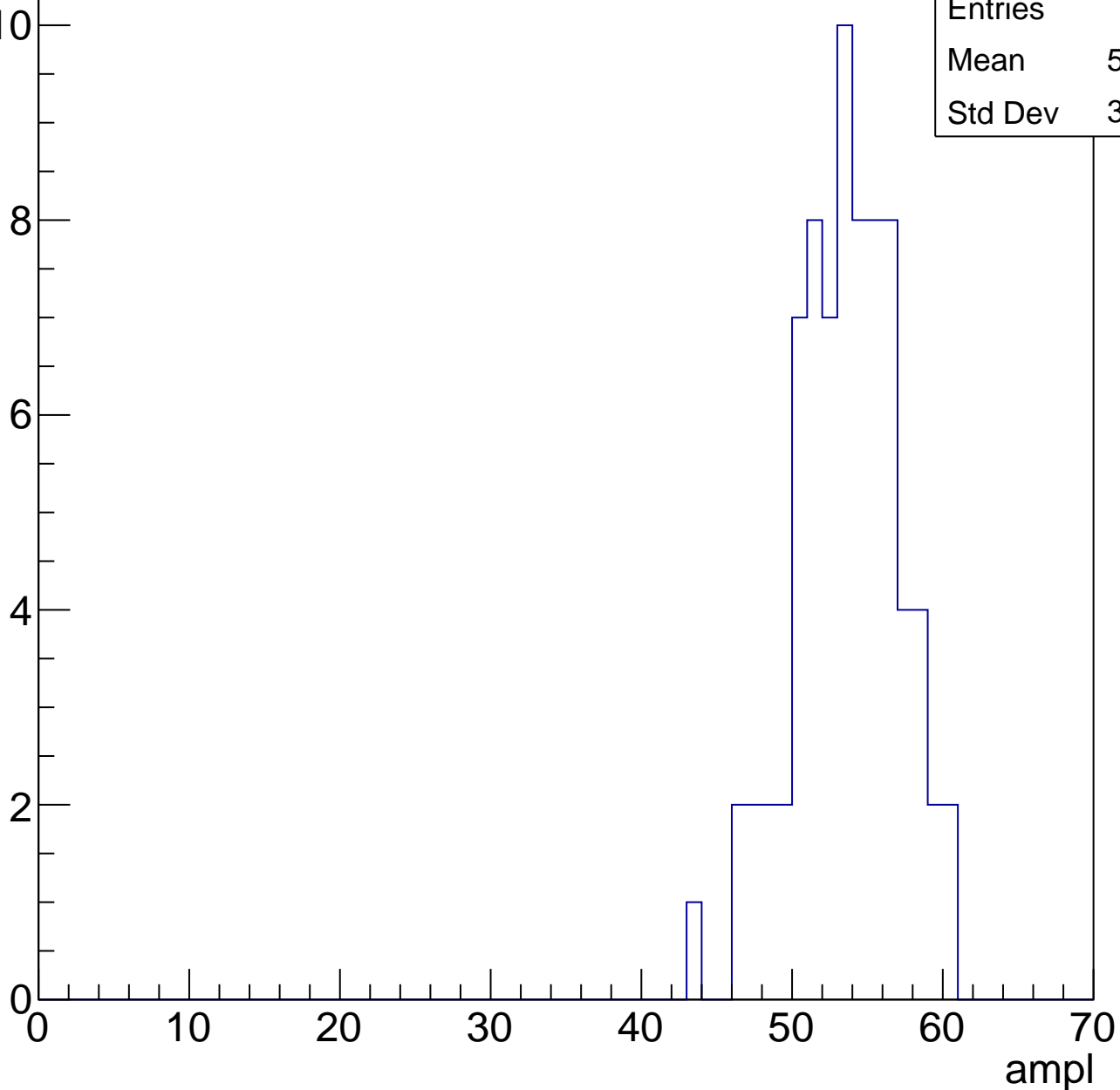


# B0L002S, U2-ch17, adc3

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	77
Mean	53.16
Std Dev	3.415

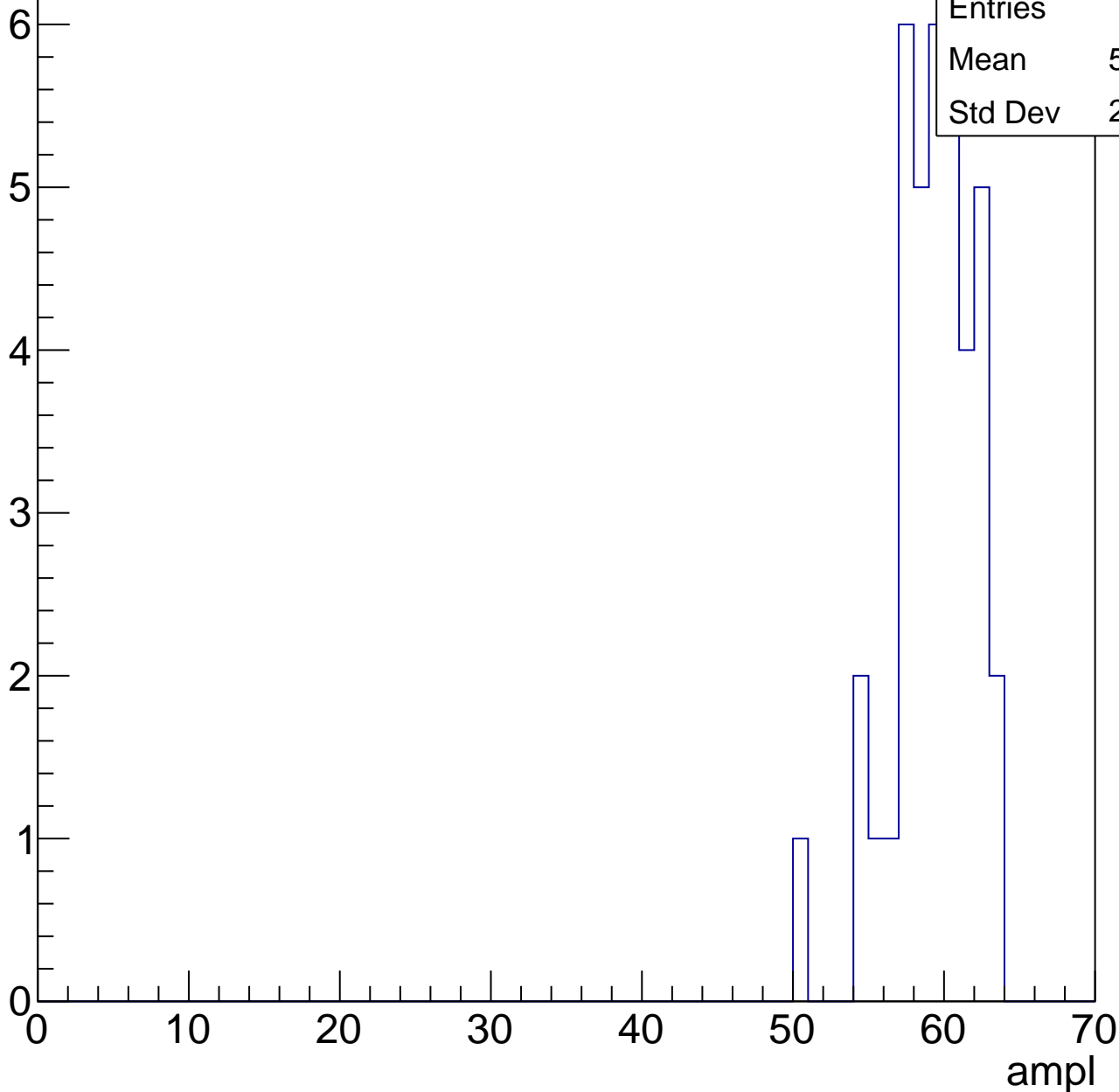


# B0L002S, U2-ch17, adc4

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	39
Mean	58.85
Std Dev	2.694

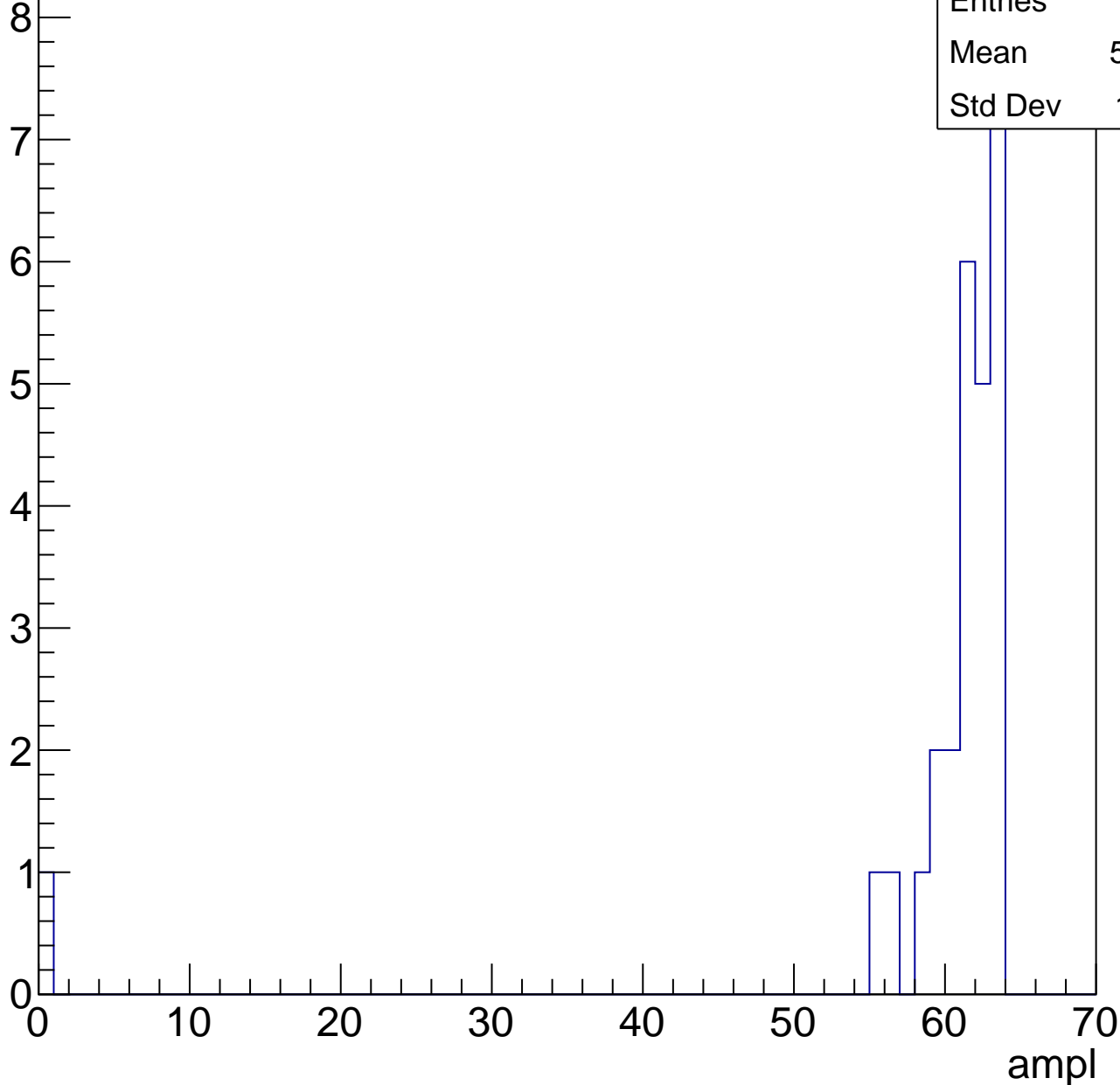


# B0L002S, U2-ch17, adc5

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	27
Mean	58.78
Std Dev	11.71



# B0L002S, U2-ch17, adc6

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



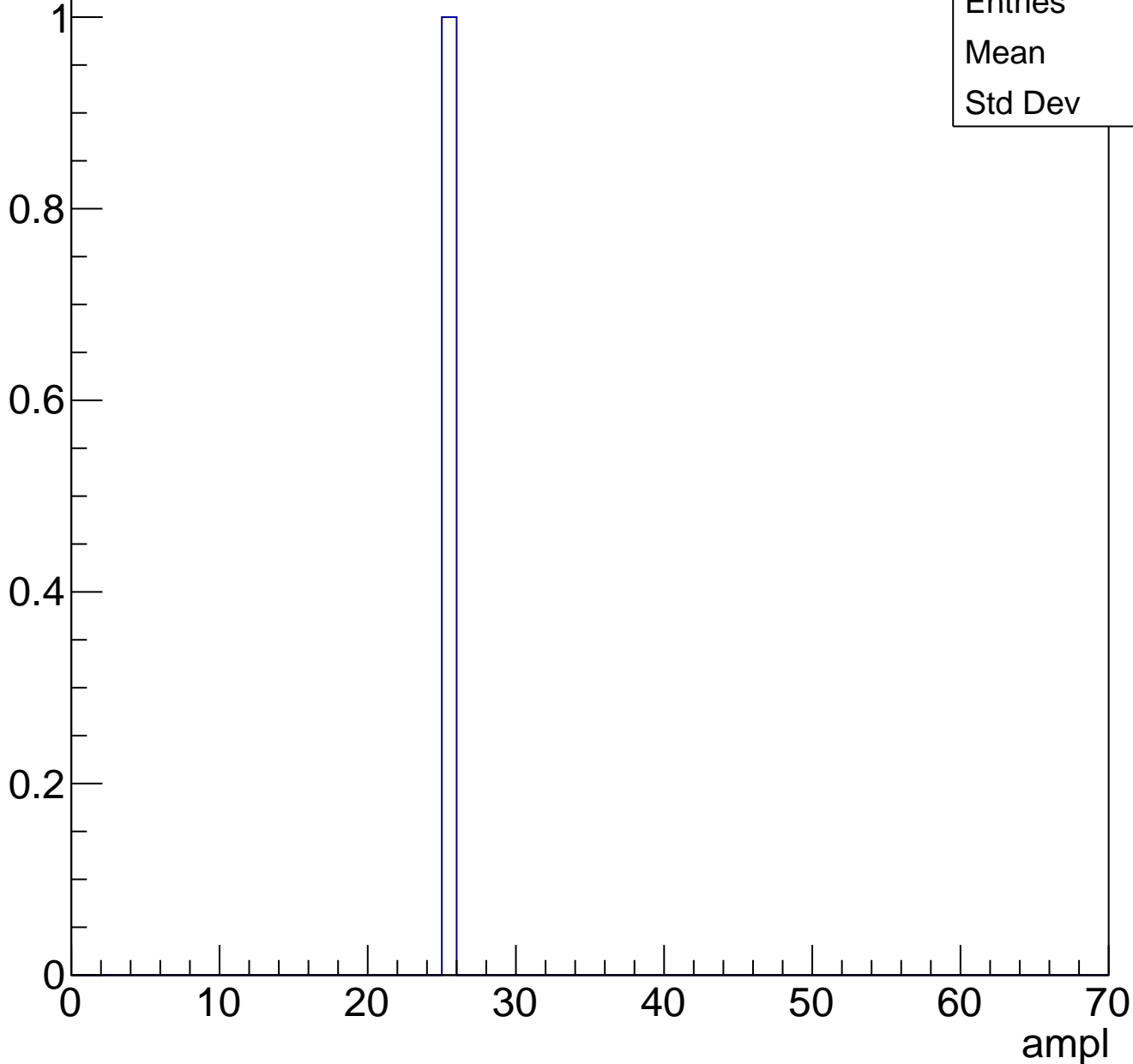
Entries	0
Mean	0
Std Dev	0



# B0L002S, U2-ch17, adc7

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



# B0L002S, U2-ch18, adc0

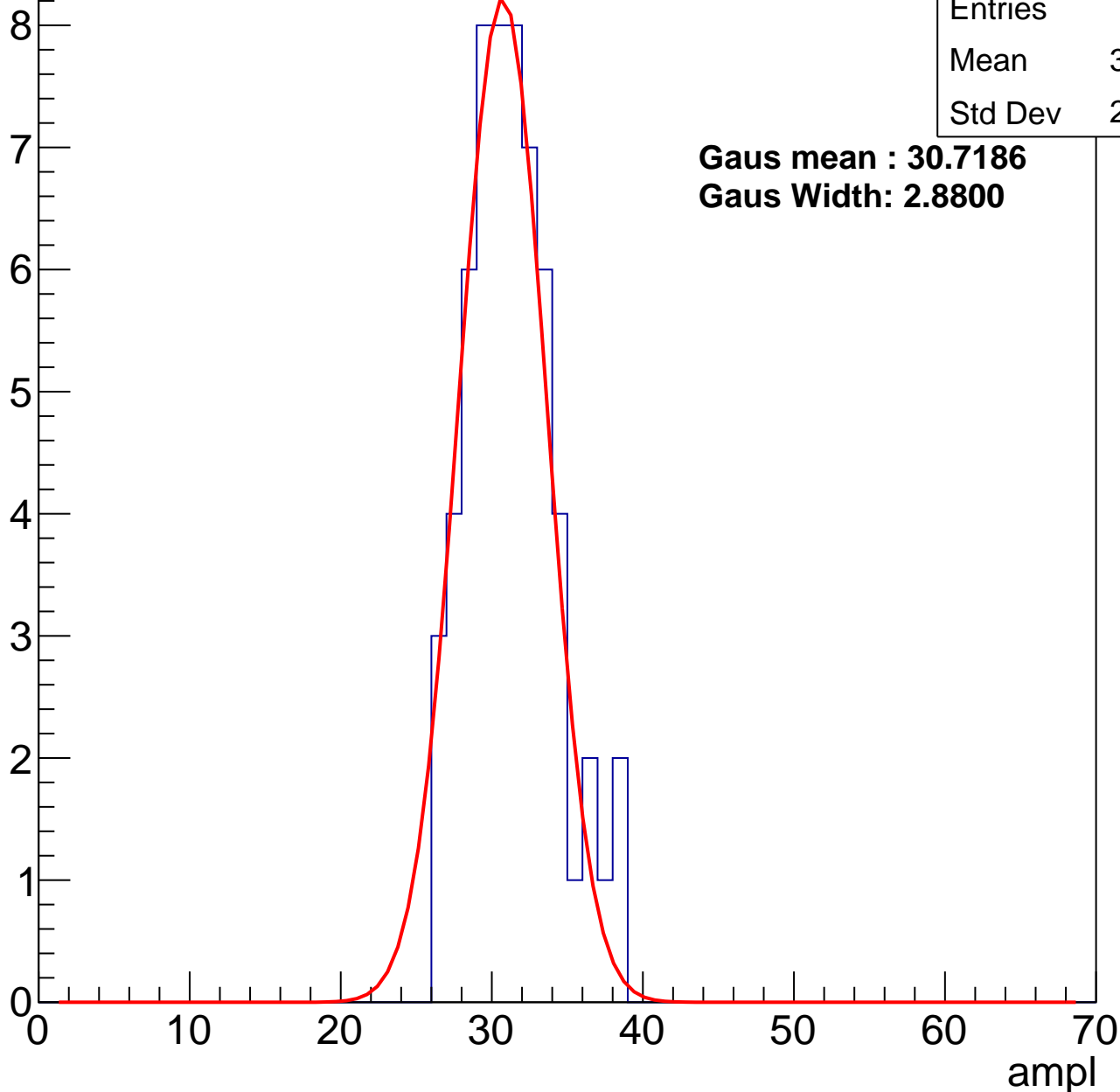
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	60
Mean	30.87
Std Dev	2.884

**Gaus mean : 30.7186**

**Gaus Width: 2.8800**



# B0L002S, U2-ch18, adc1

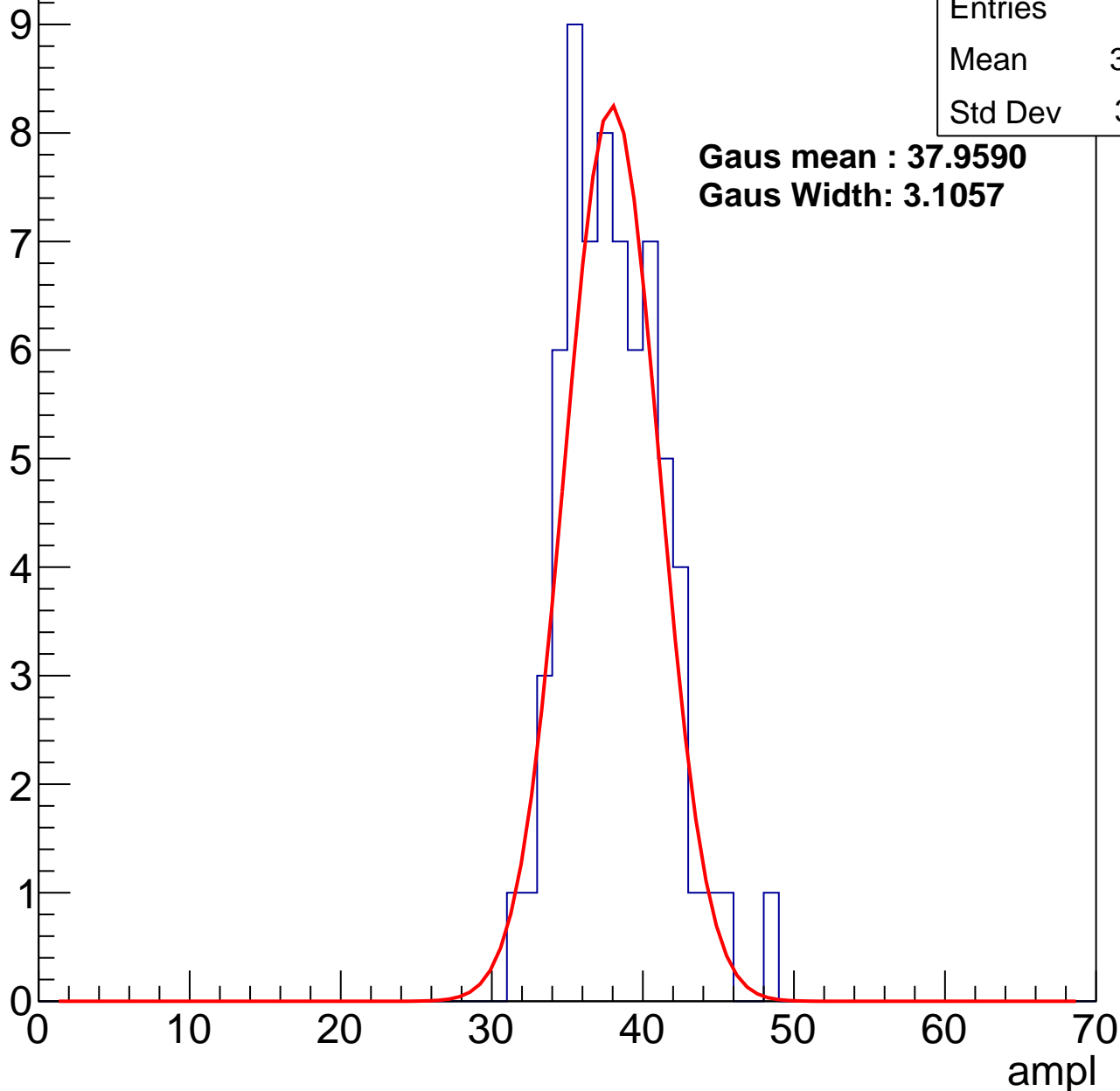
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	68
Mean	37.68
Std Dev	3.251

**Gaus mean : 37.9590**

**Gaus Width: 3.1057**



# B0L002S, U2-ch18, adc2

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	56
Mean	43.34
Std Dev	2.96

7

6

5

4

3

2

1

0

**Gaus mean : 44.0320**

**Gaus Width: 3.0931**

ampl

0

10

20

30

40

50

60

70

# B0L002S, U2-ch18, adc3

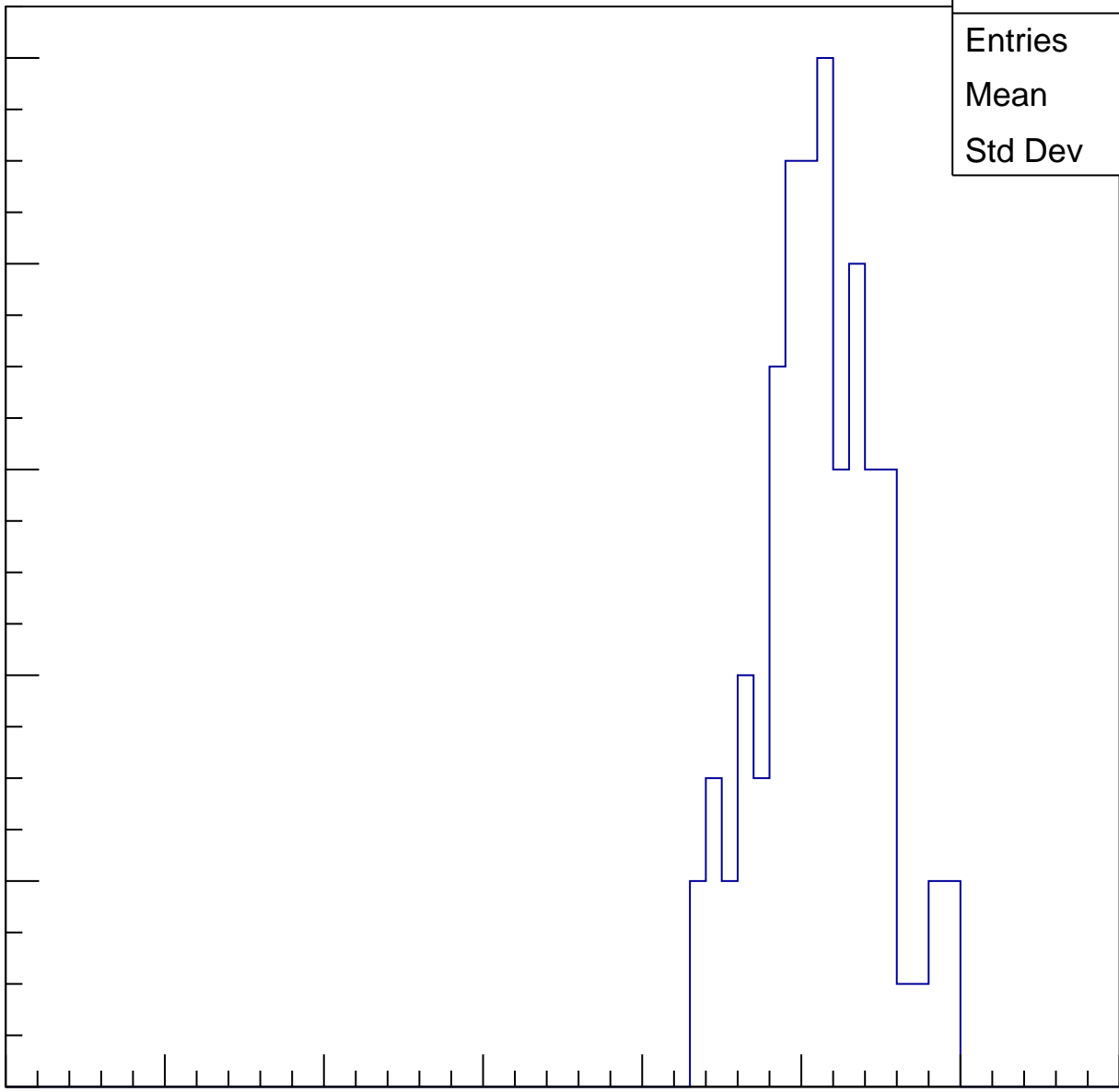
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entries	81
Mean	50.7
Std Dev	3.636

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70  
ampl

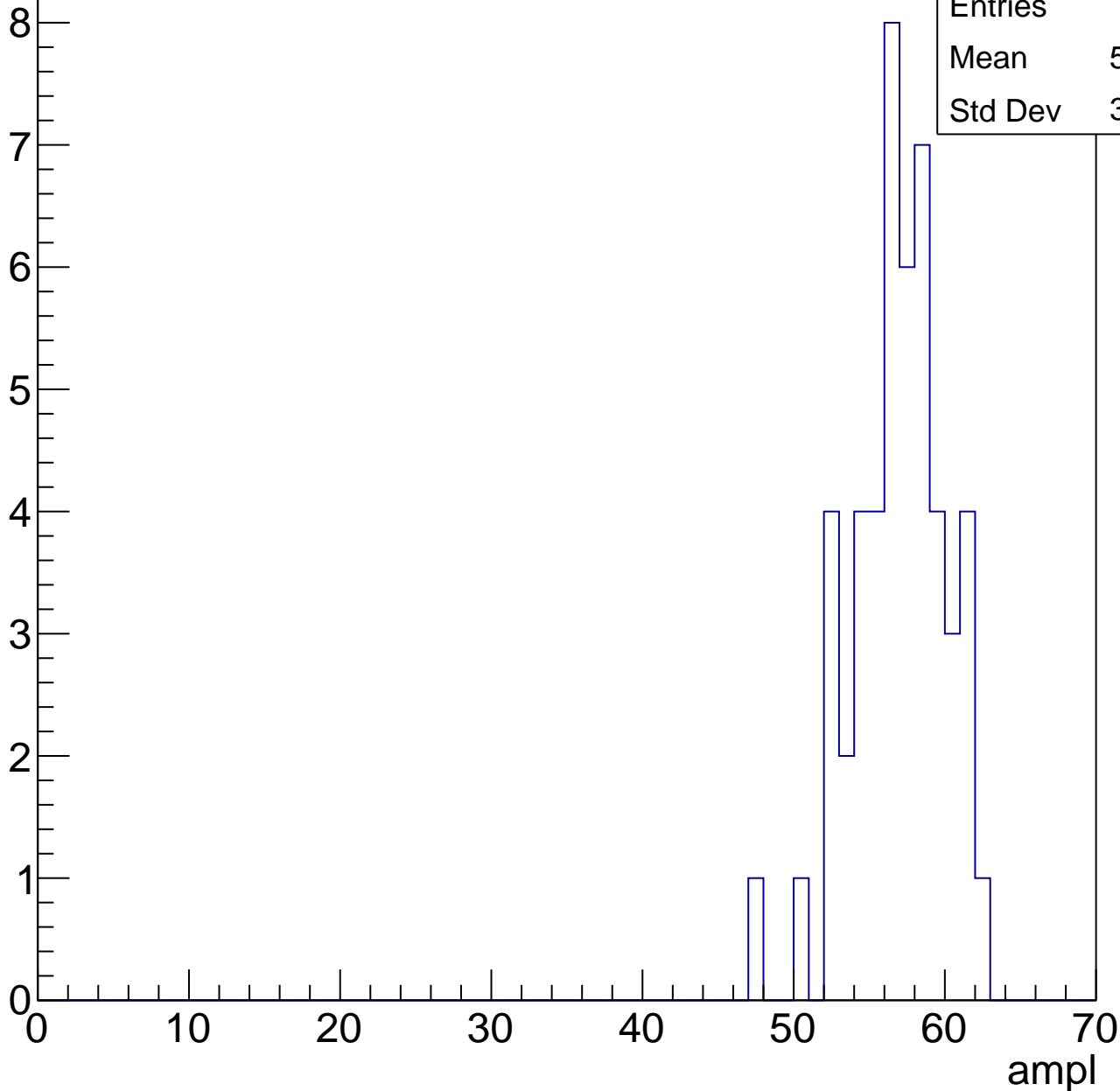


# B0L002S, U2-ch18, adc4

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

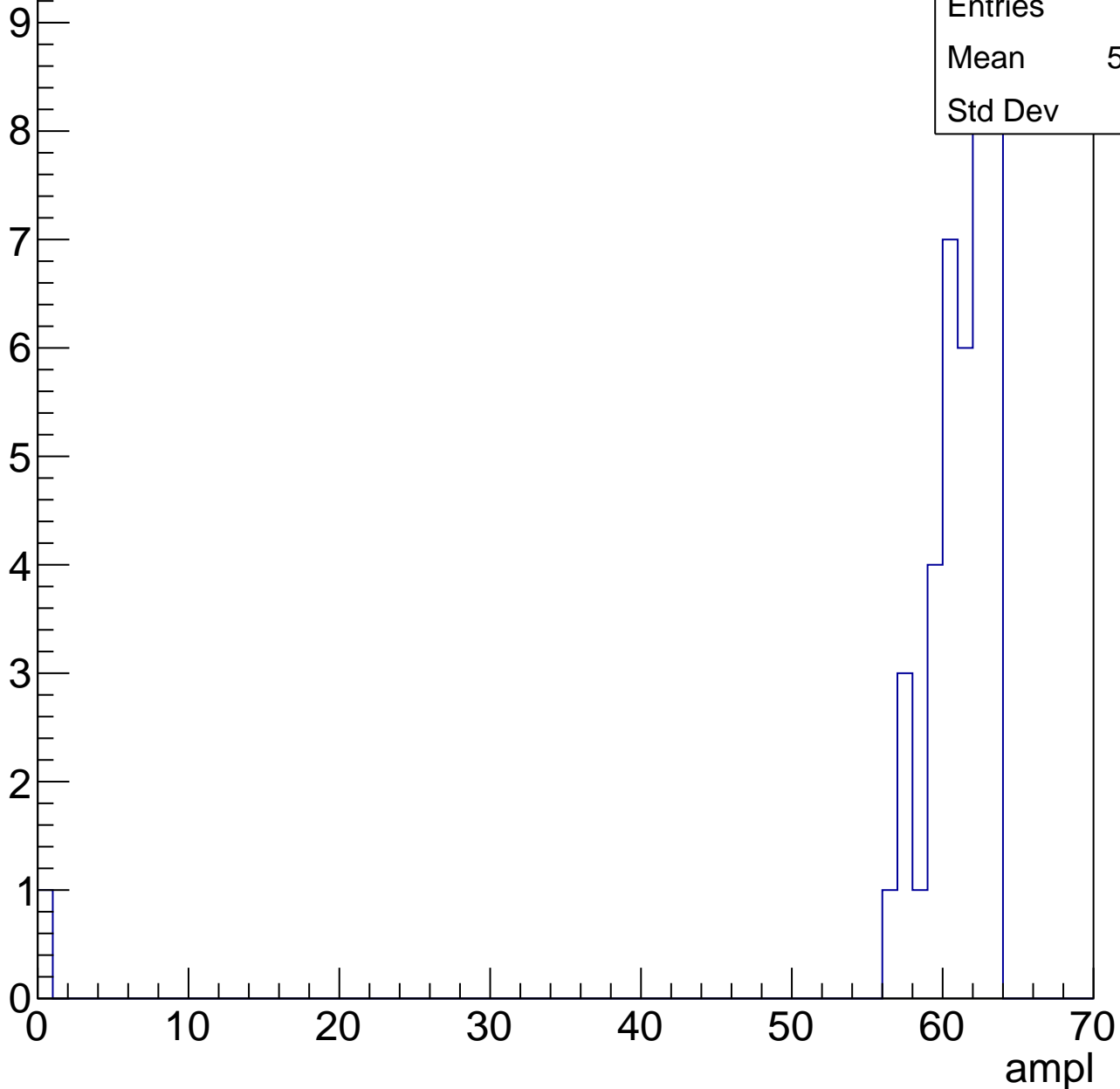
Entries	49
Mean	56.43
Std Dev	3.077



# B0L002S, U2-ch18, adc5

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



# B0L002S, U2-ch18, adc6

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

1

0.8

0.6

0.4

0.2

0

0

10

20

30

40

50

60

70

ampl

Entries

1

Mean

63

Std Dev

0



# B0L002S, U2-ch18, adc7

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L002S, U2-ch19, adc0

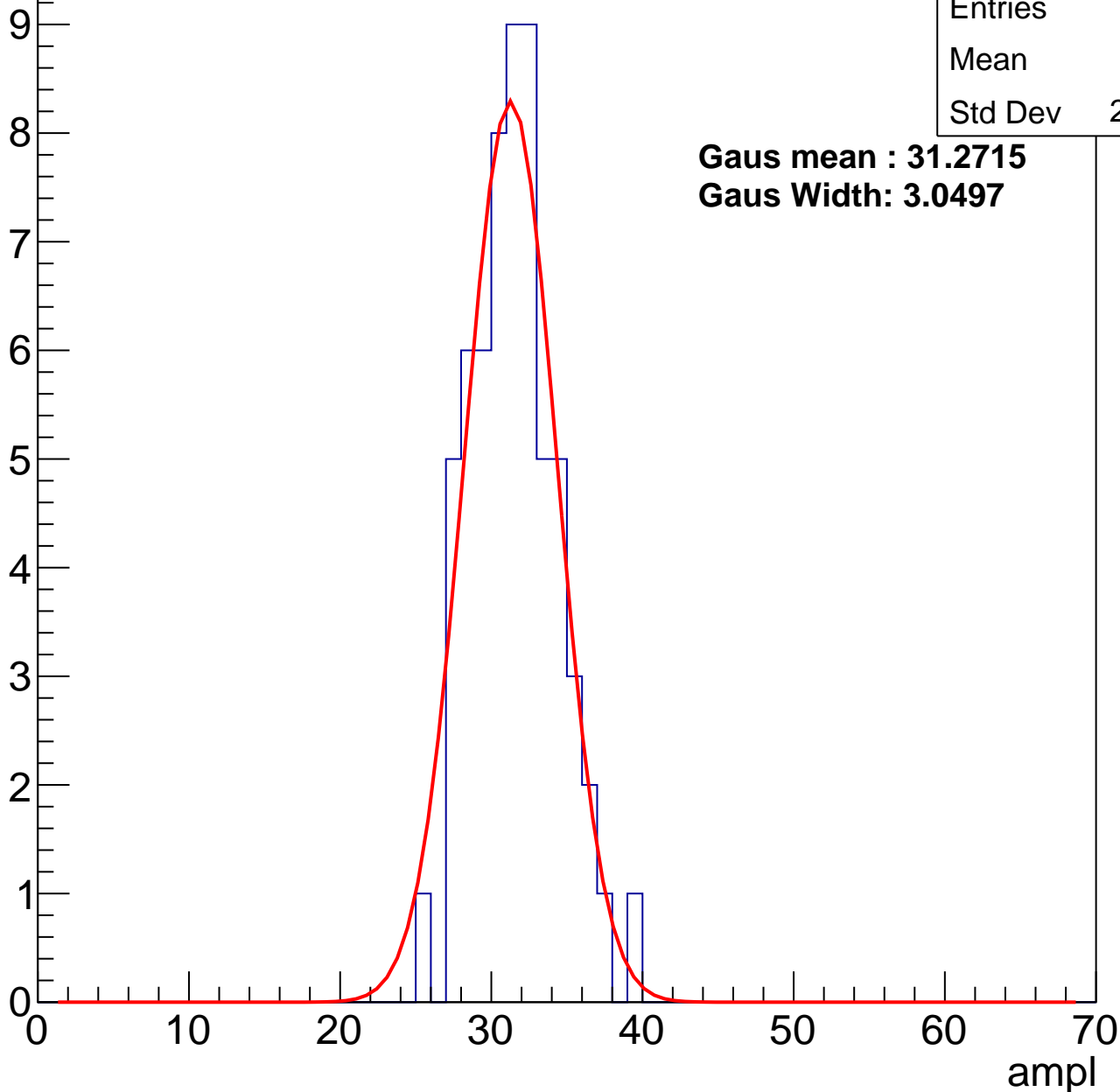
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	61
Mean	31.1
Std Dev	2.786

**Gaus mean : 31.2715**

**Gaus Width: 3.0497**



# B0L002S, U2-ch19, adc1

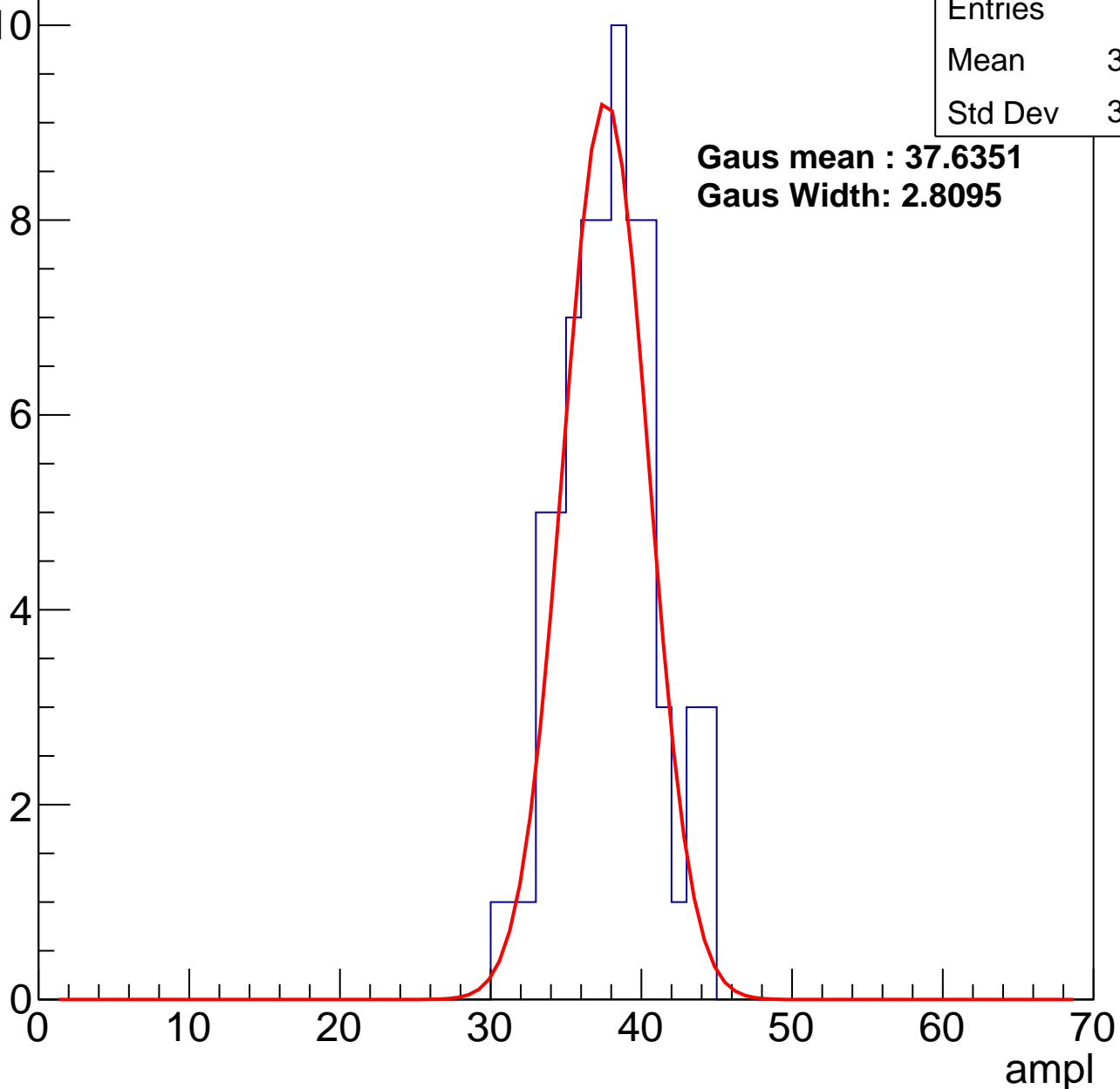
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	72
Mean	37.43
Std Dev	3.117

**Gaus mean : 37.6351**

**Gaus Width: 2.8095**



# B0L002S, U2-ch19, adc2

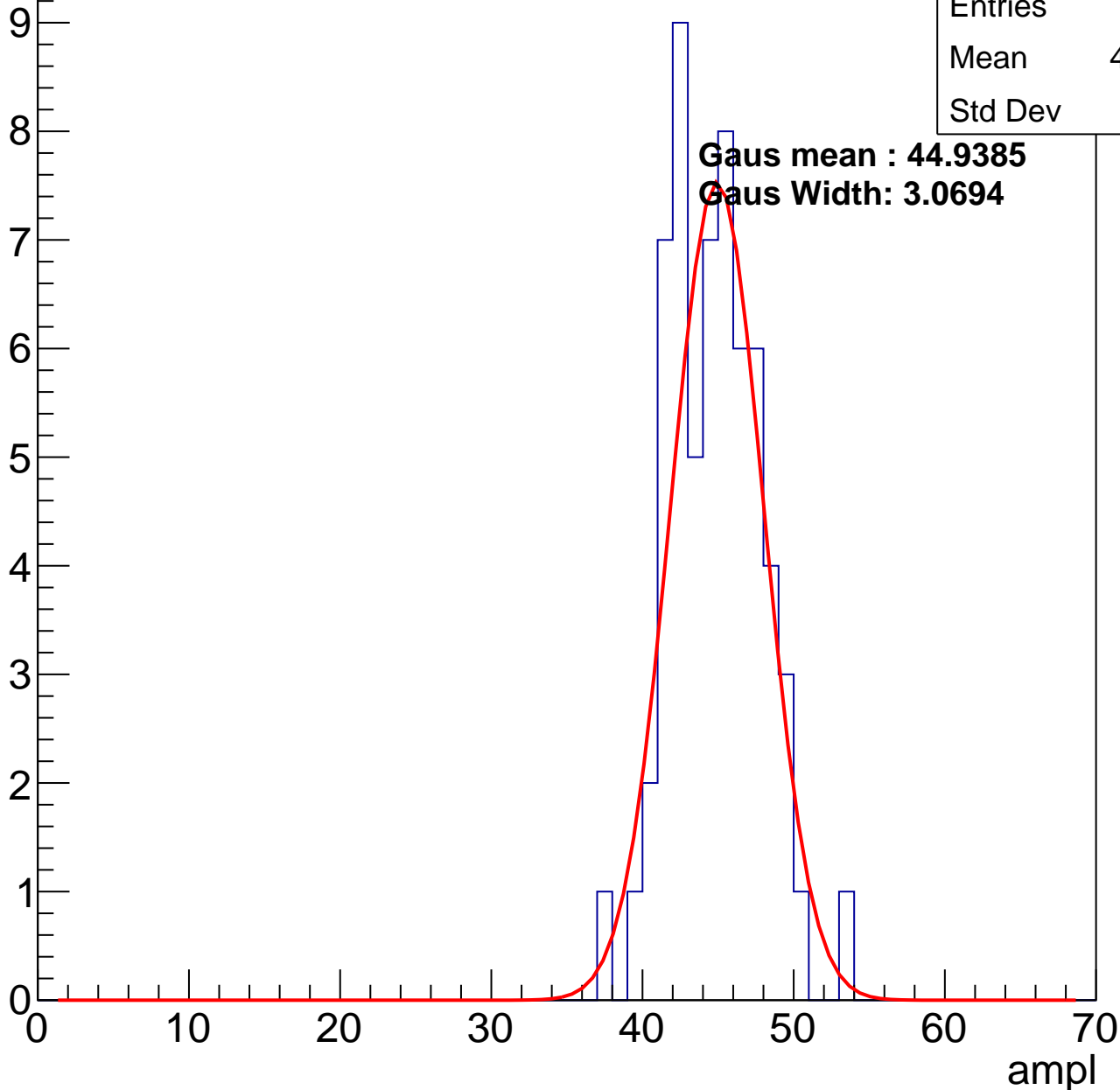
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	61
Mean	44.33
Std Dev	2.99

**Gaus mean : 44.9385**

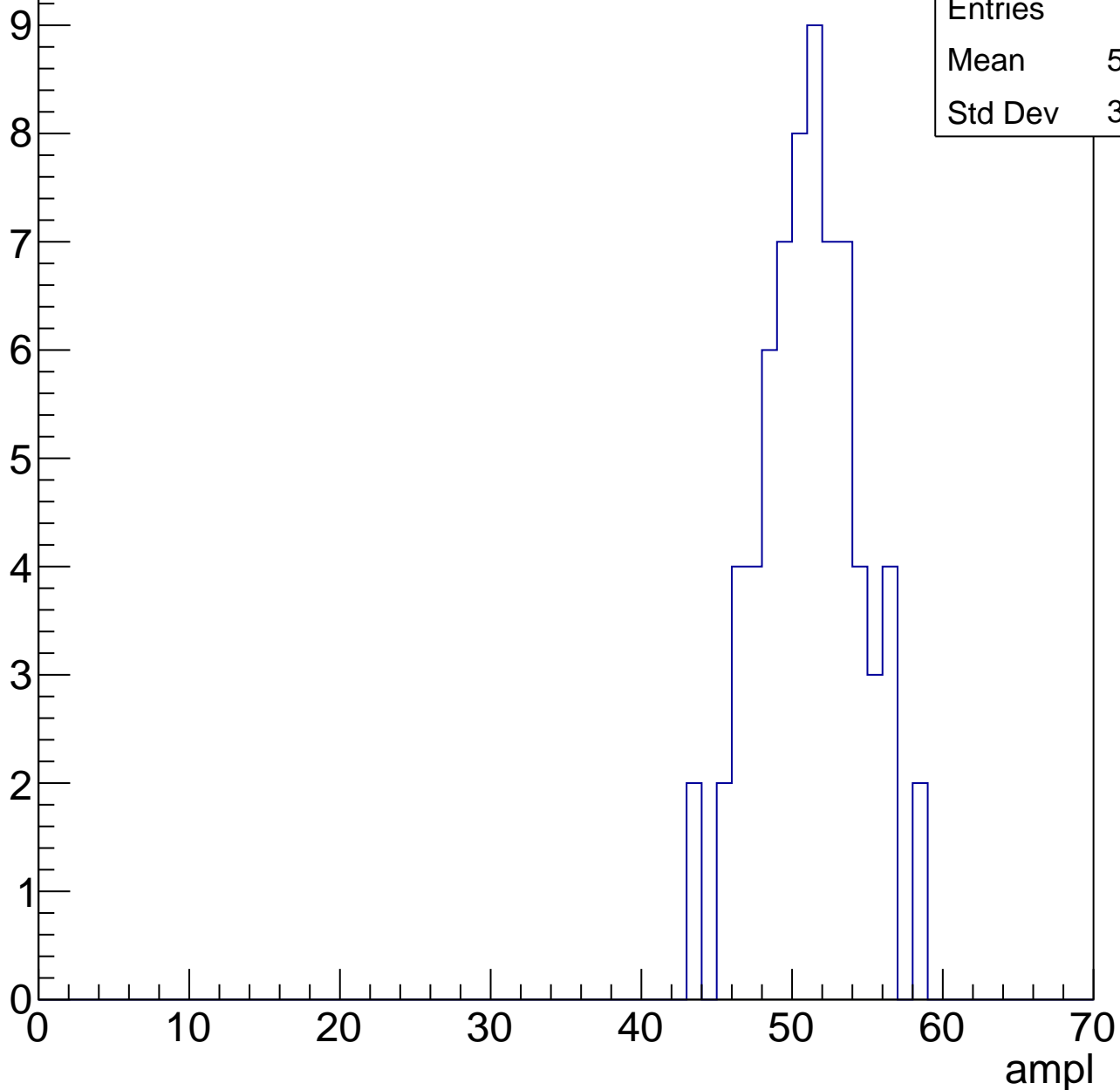
**Gaus Width: 3.0694**



# B0L002S, U2-ch19, adc3

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

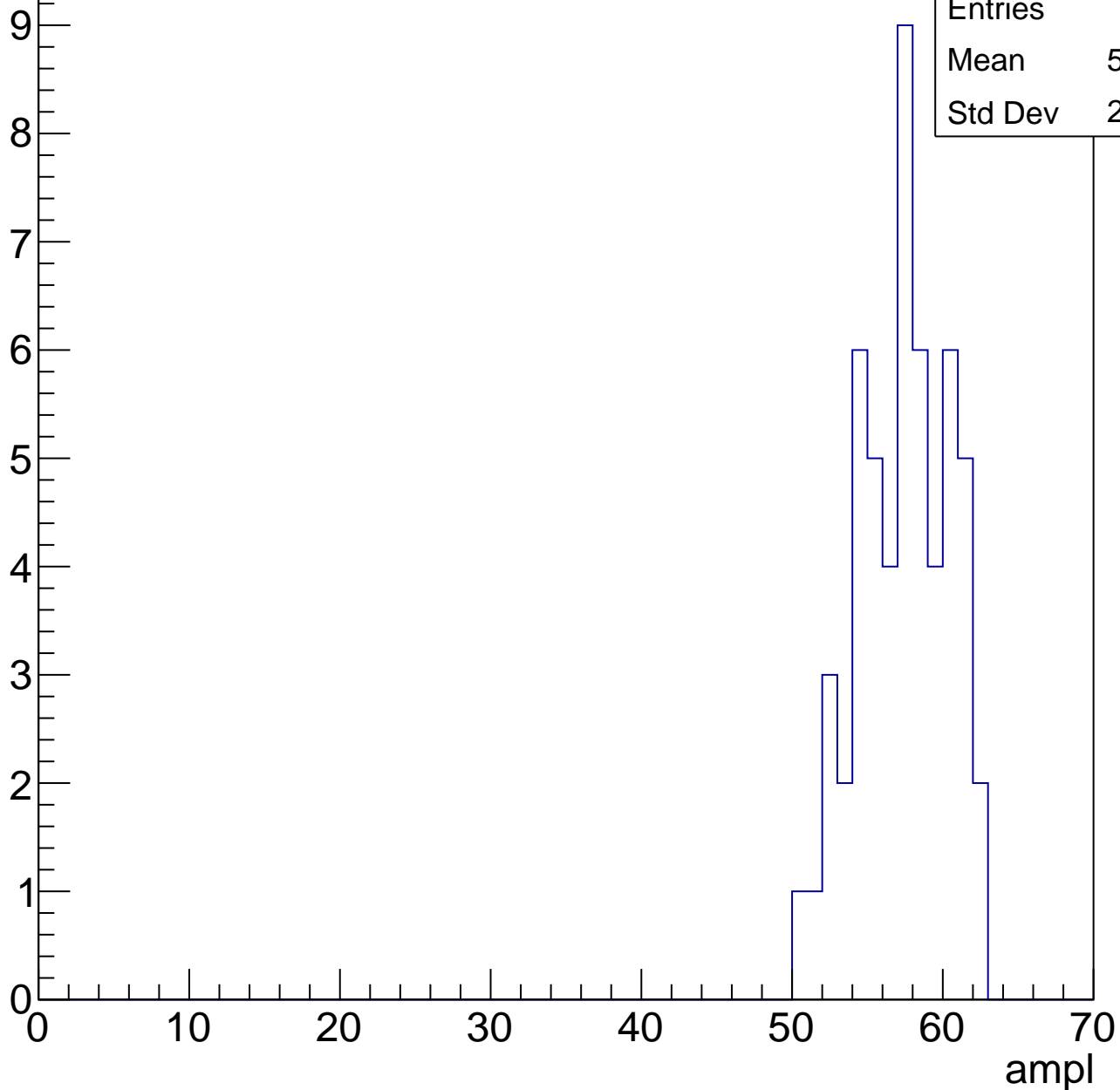


Entries	69
Mean	50.64
Std Dev	3.323

# B0L002S, U2-ch19, adc4

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

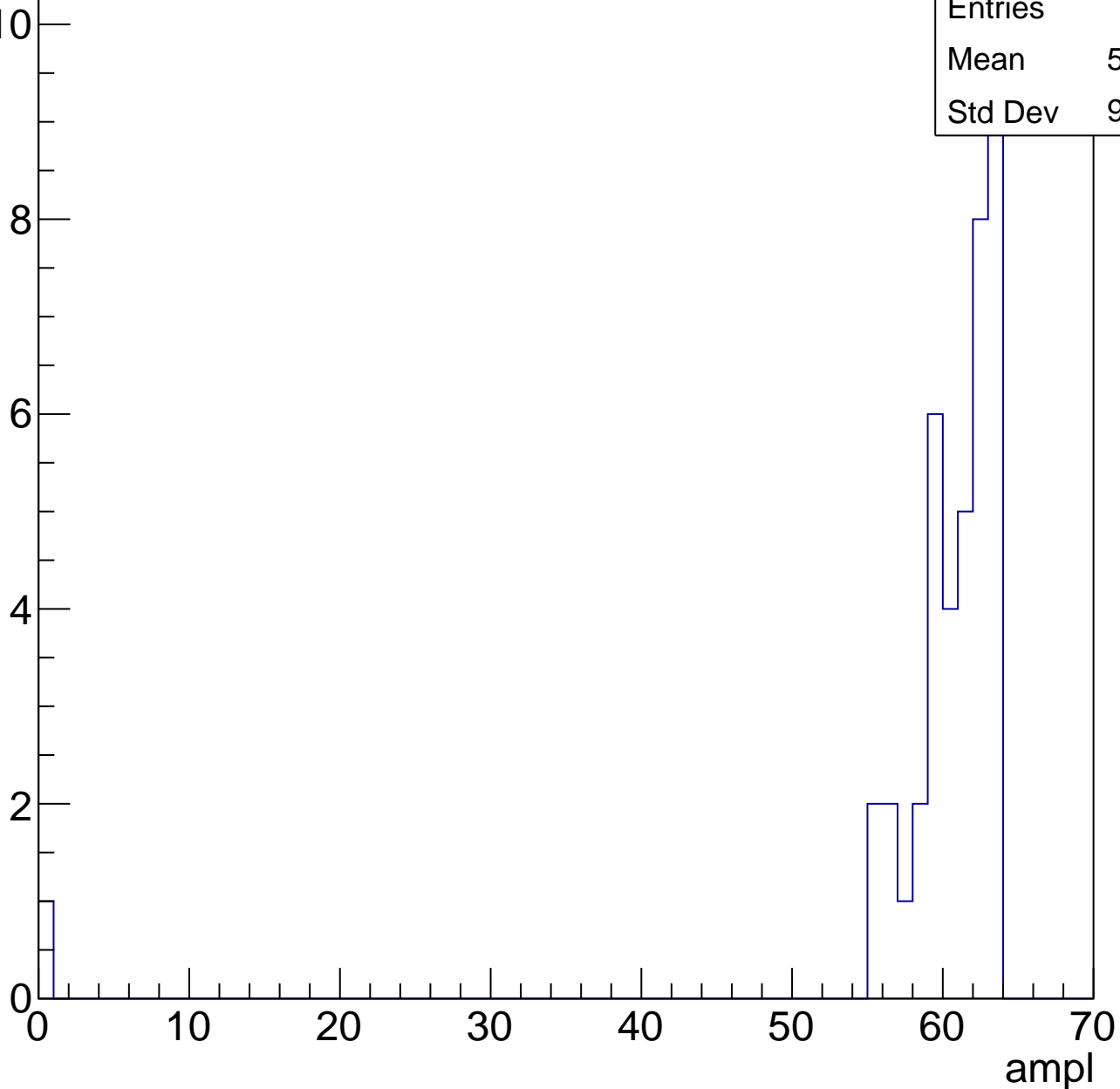


# B0L002S, U2-ch19, adc5

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	41
Mean	59.02
Std Dev	9.618



# B0L002S, U2-ch19, adc6

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



Entries	0
Mean	0
Std Dev	0



# B0L002S, U2-ch19, adc7

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L002S, U2-ch20, adc0

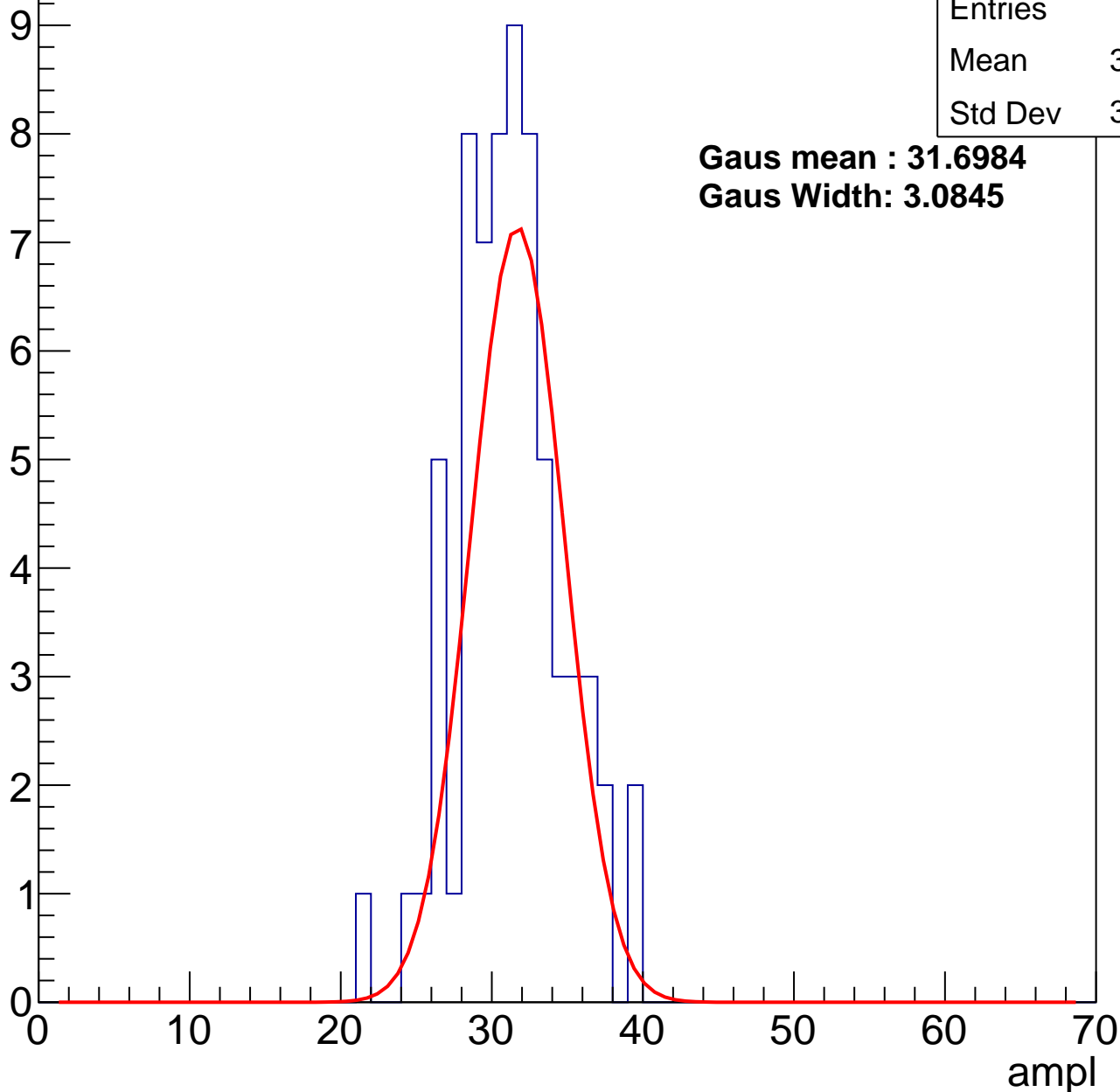
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	67
Mean	30.76
Std Dev	3.473

**Gaus mean : 31.6984**

**Gaus Width: 3.0845**



# B0L002S, U2-ch20, adc1

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entries	67
Mean	36.91
Std Dev	3.199

**Gaus mean : 37.5189**

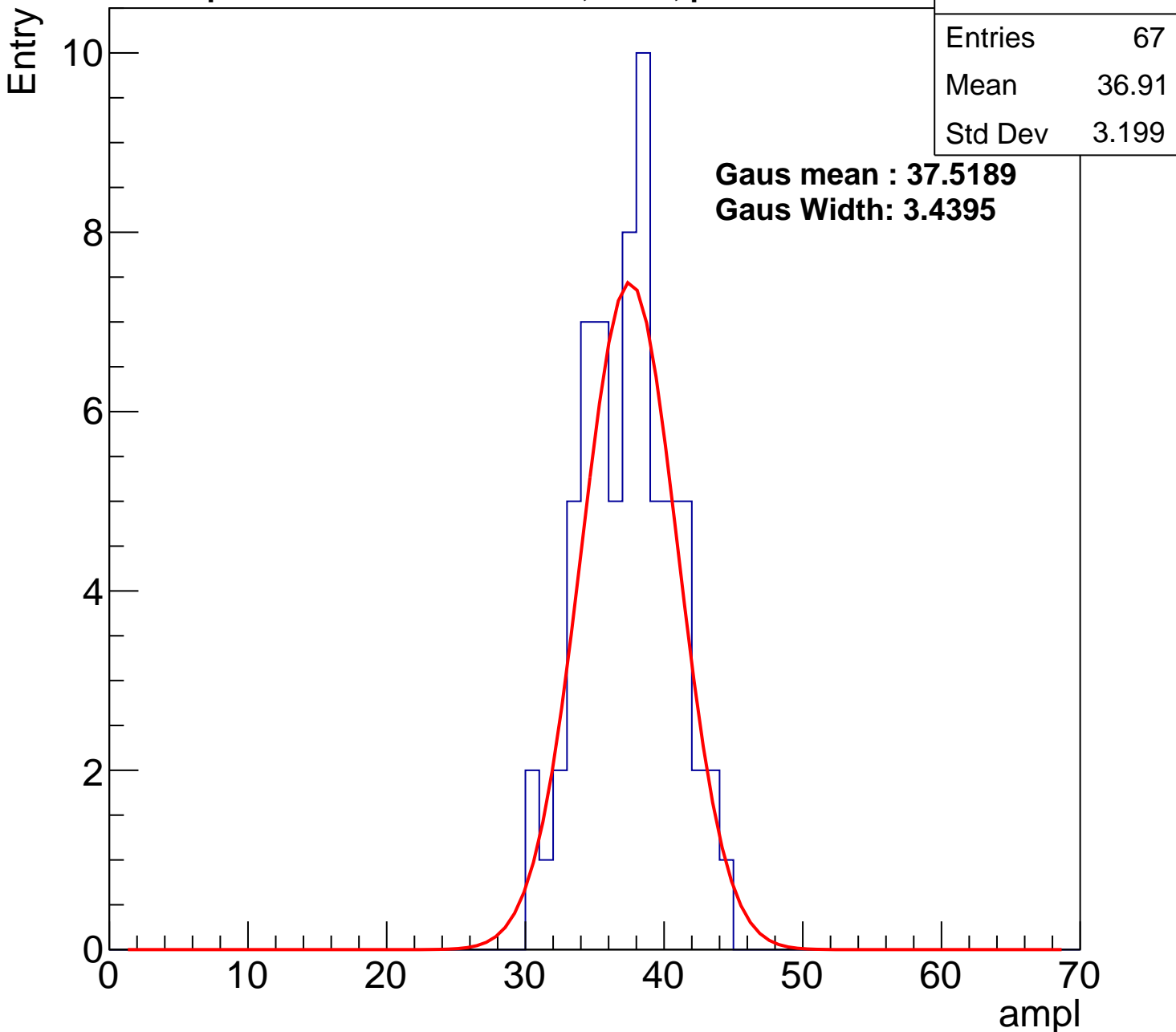
**Gaus Width: 3.4395**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B0L002S, U2-ch20, adc2

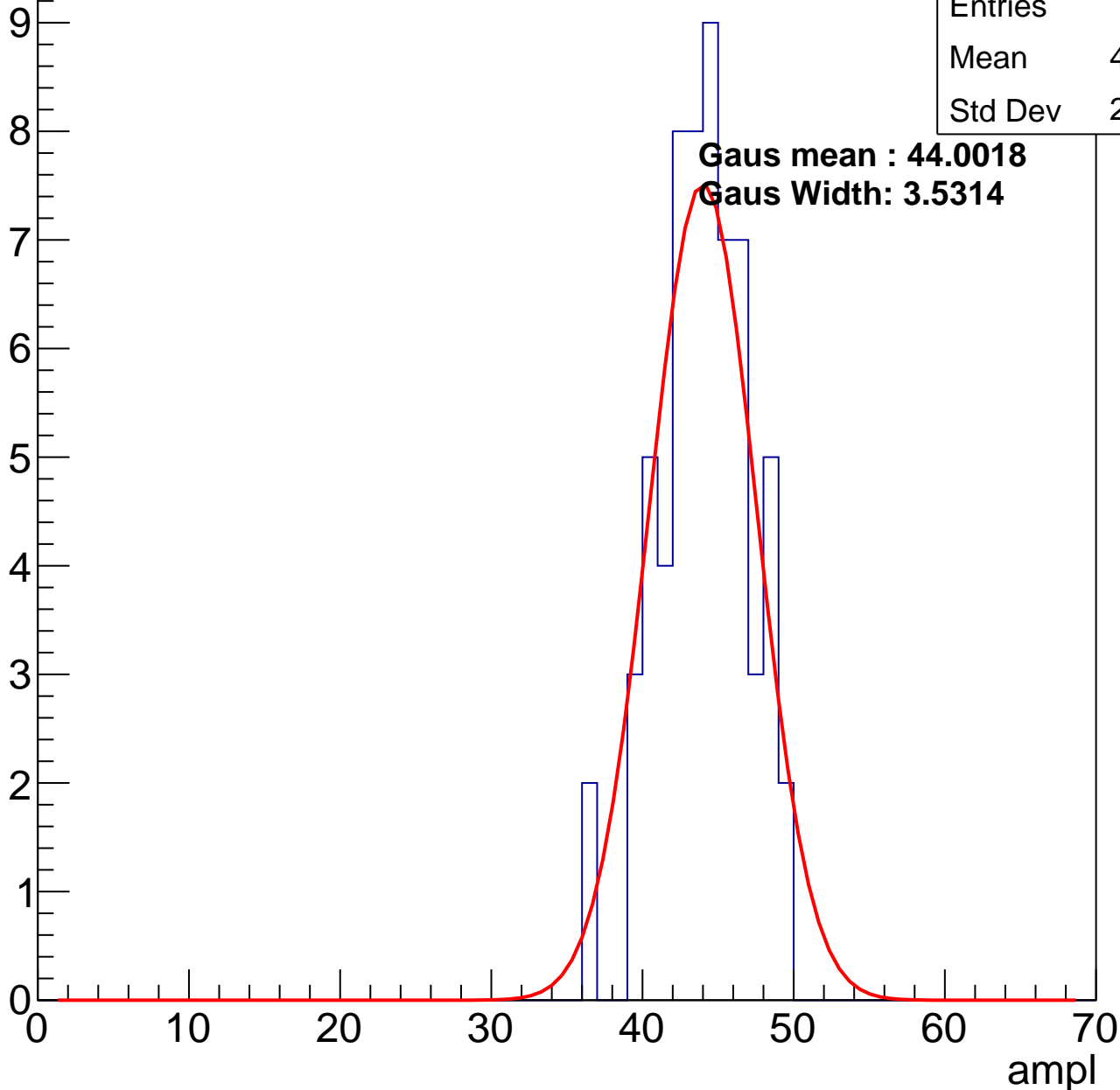
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	63
Mean	43.57
Std Dev	2.926

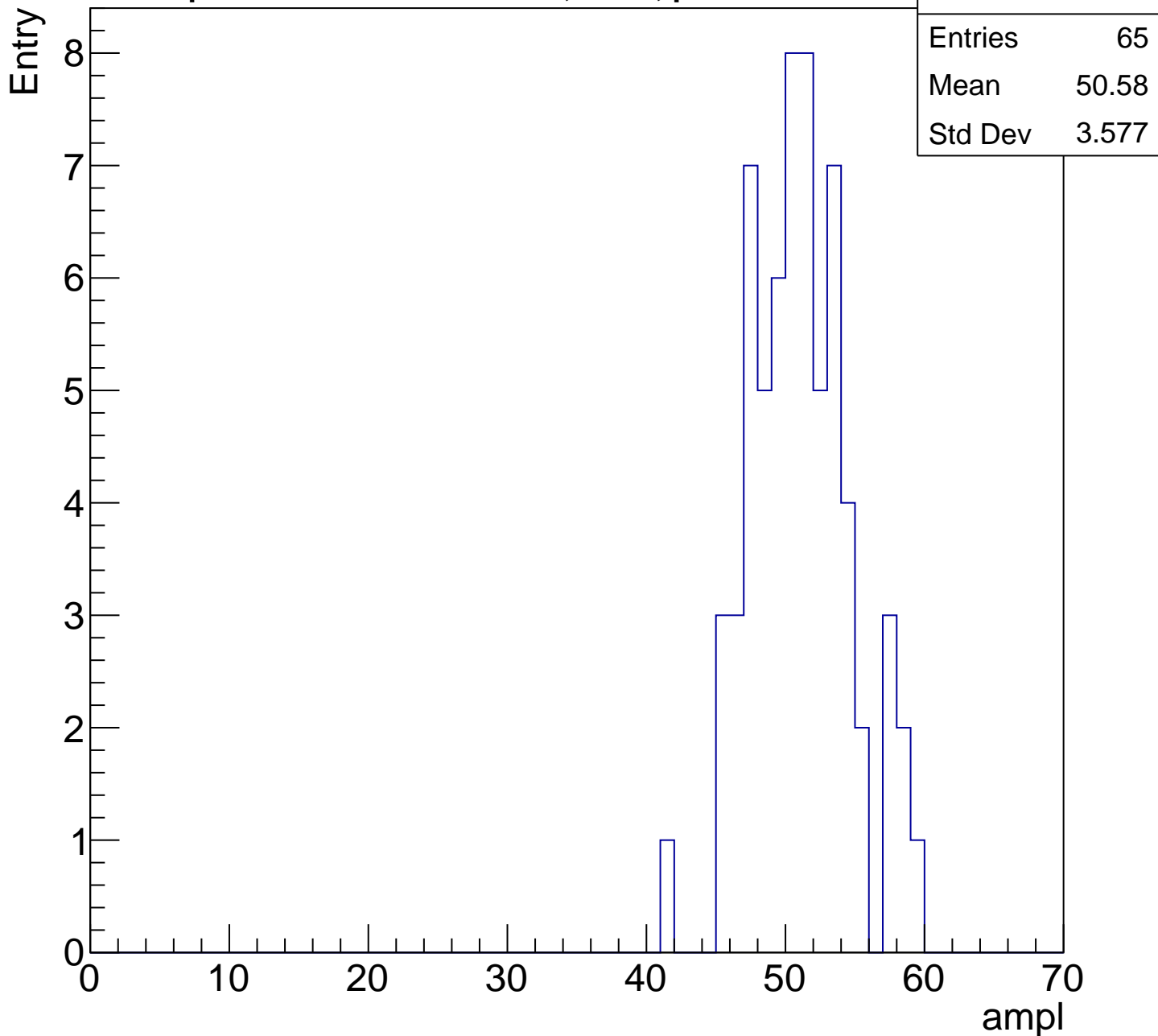
**Gaus mean : 44.0018**

**Gaus Width: 3.5314**



# B0L002S, U2-ch20, adc3

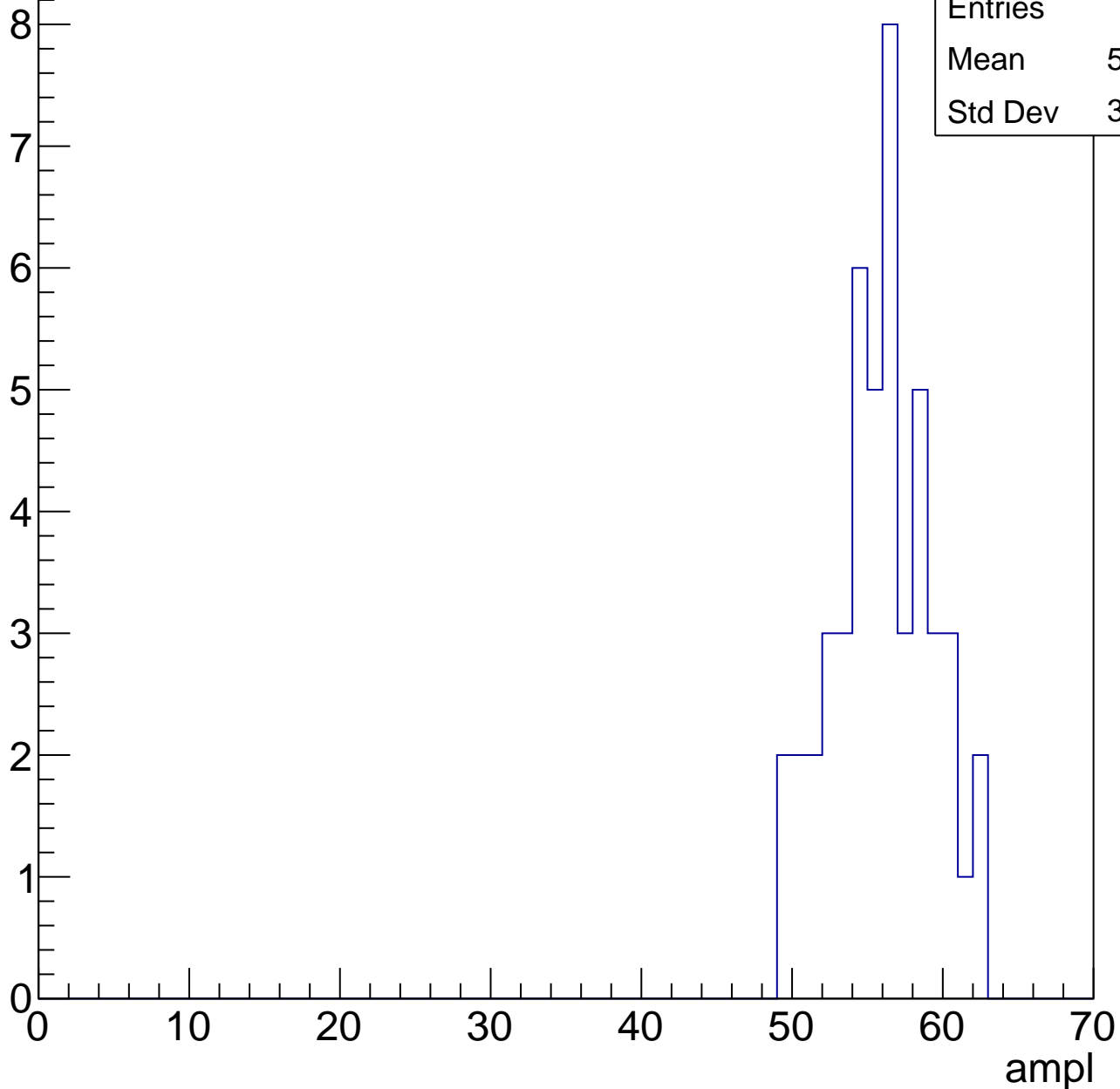
calib\_packv5\_042523\_0143.root, FC#8, port C1



# B0L002S, U2-ch20, adc4

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



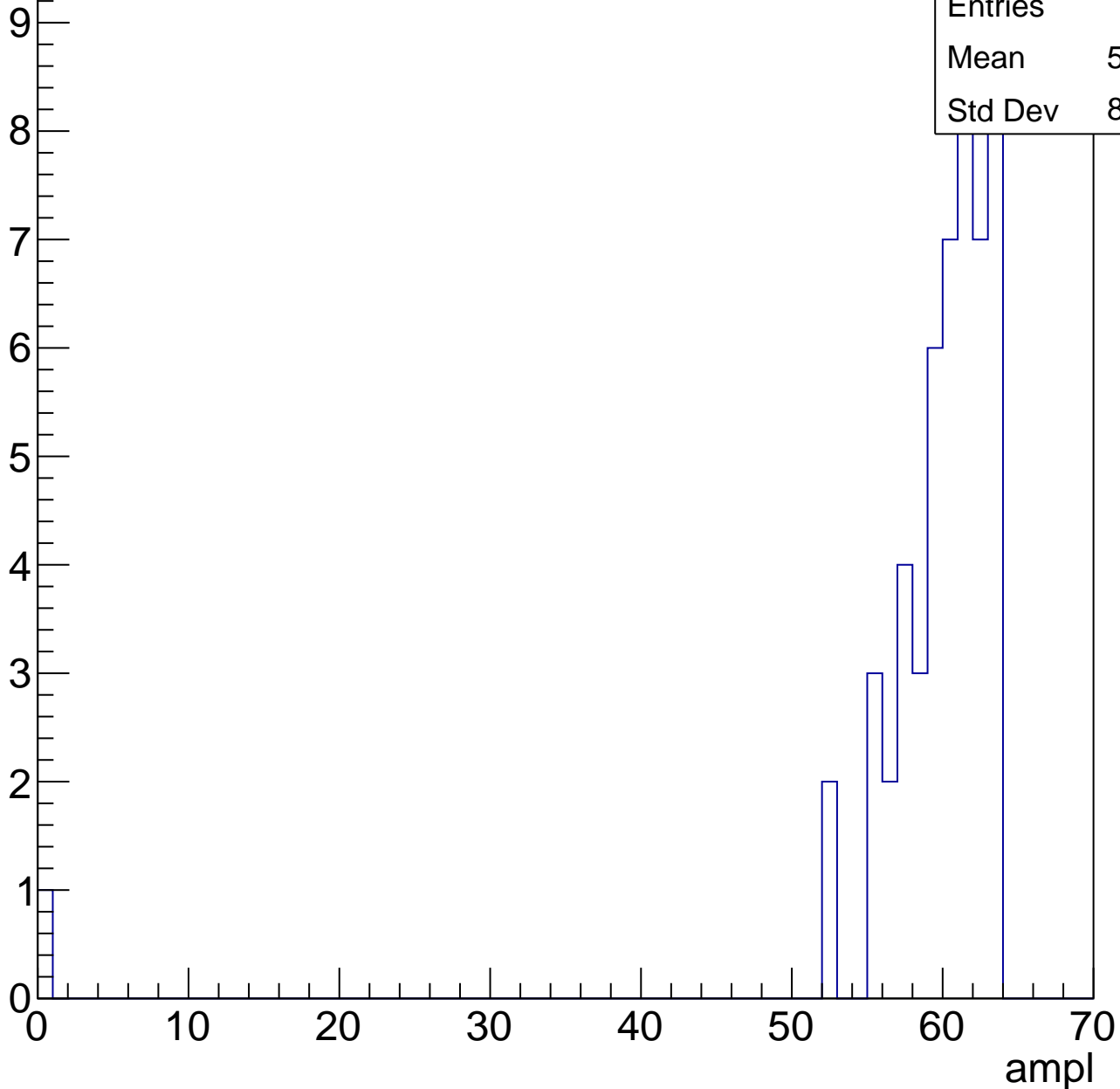
Entries	48
Mean	55.52
Std Dev	3.253

# B0L002S, U2-ch20, adc5

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	53
Mean	58.62
Std Dev	8.585



# B0L002S, U2-ch20, adc6

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry





# B0L002S, U2-ch20, adc7

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



# B0L002S, U2-ch21, adc0

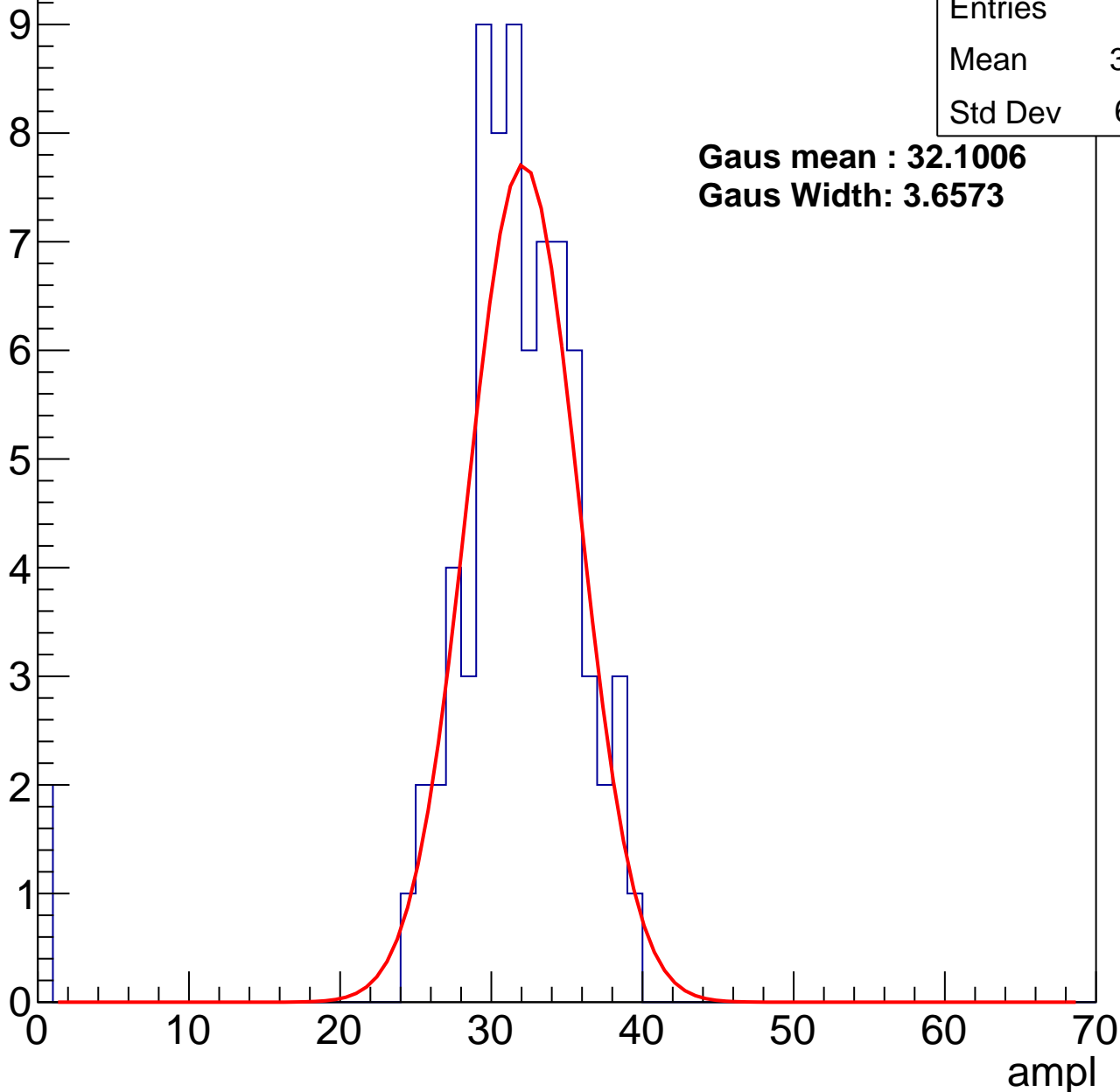
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	75
Mean	30.72
Std Dev	6.081

**Gaus mean : 32.1006**

**Gaus Width: 3.6573**



# B0L002S, U2-ch21, adc1

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entries	78
Mean	38.87
Std Dev	3.409

**Gaus mean : 39.5902**

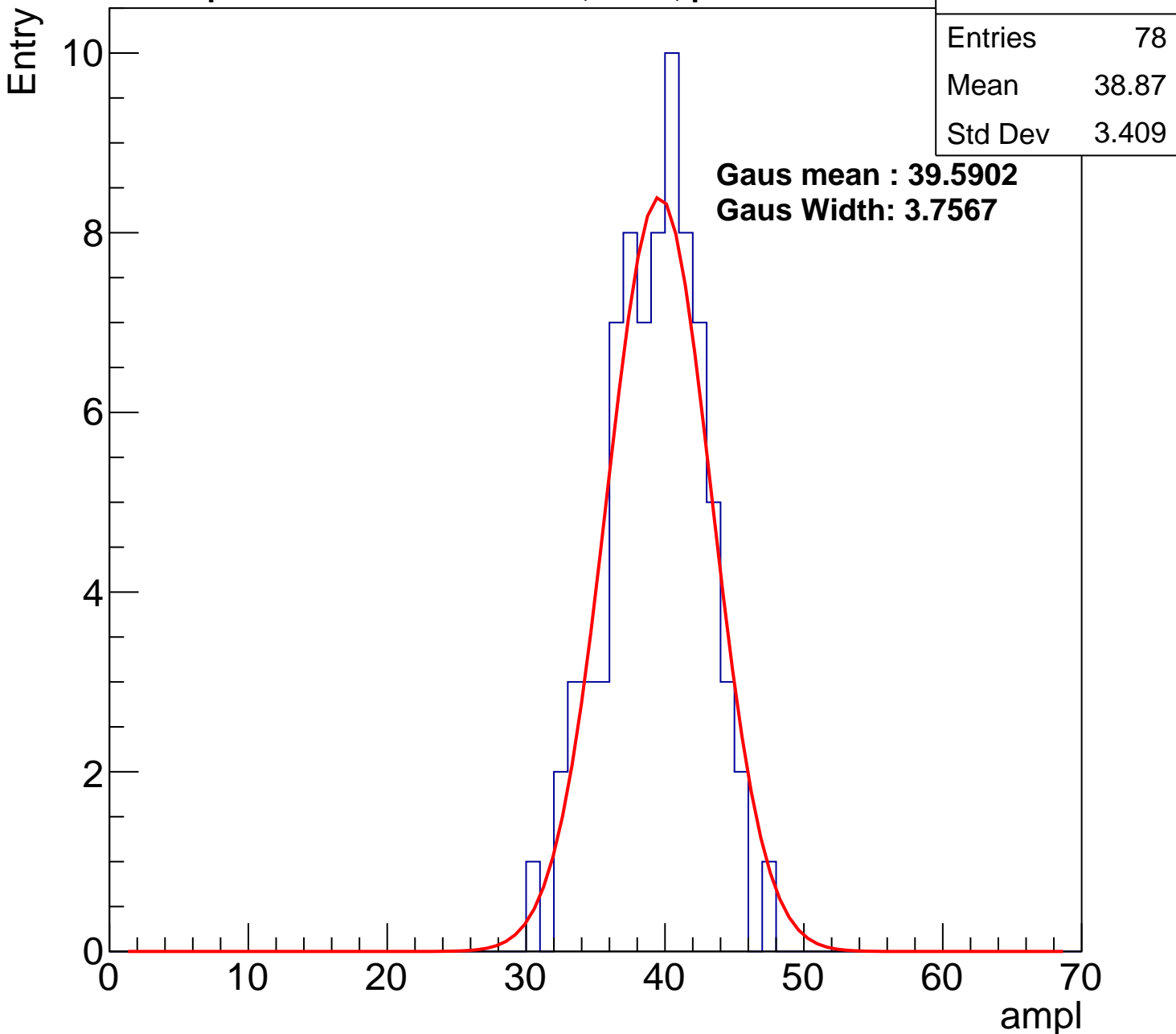
**Gaus Width: 3.7567**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B0L002S, U2-ch21, adc2

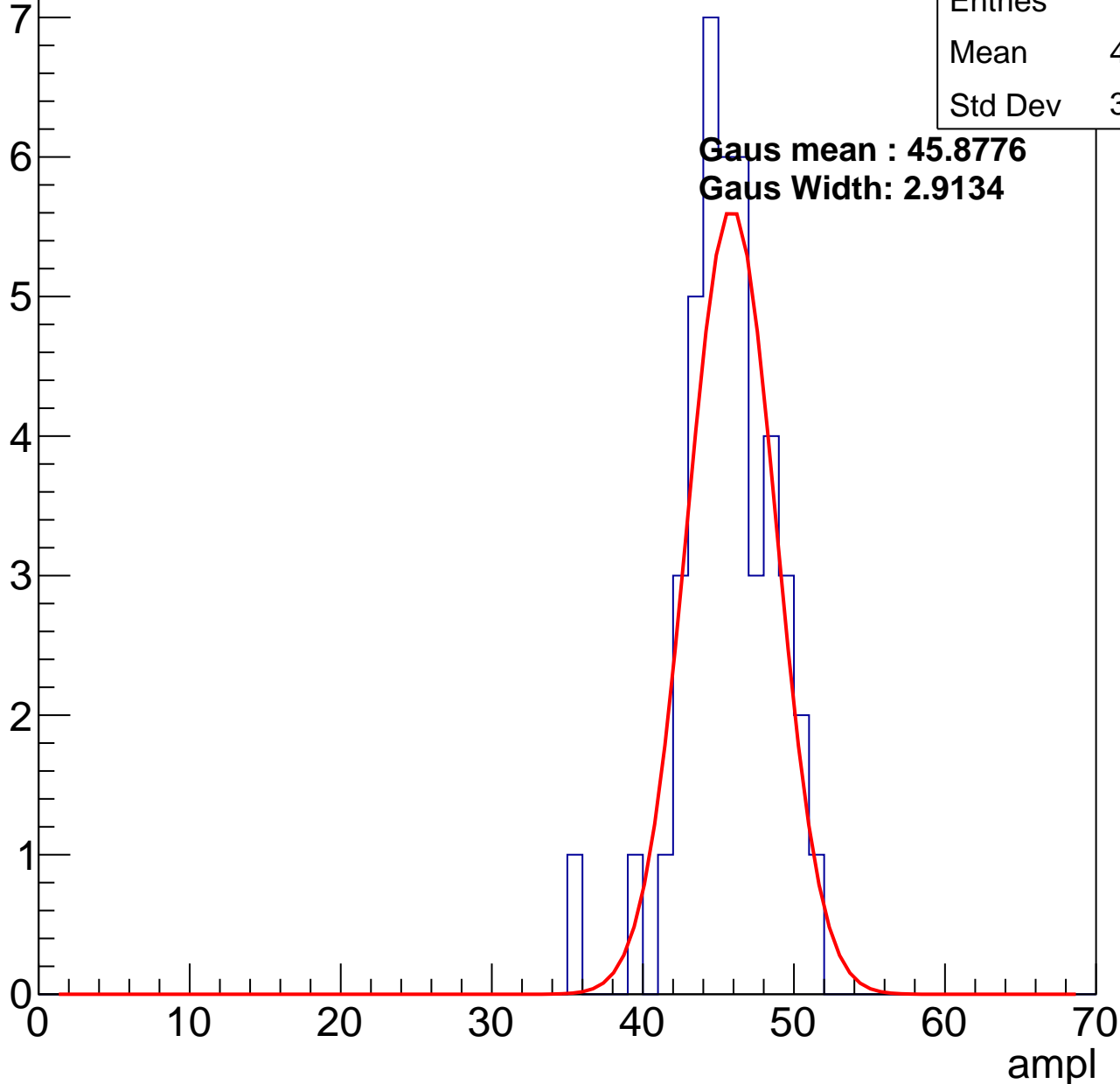
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	43
Mean	45.14
Std Dev	3.024

**Gaus mean : 45.8776**

**Gaus Width: 2.9134**



# B0L002S, U2-ch21, adc3

calib\_packv5\_042523\_0143.root, FC#8, port C1

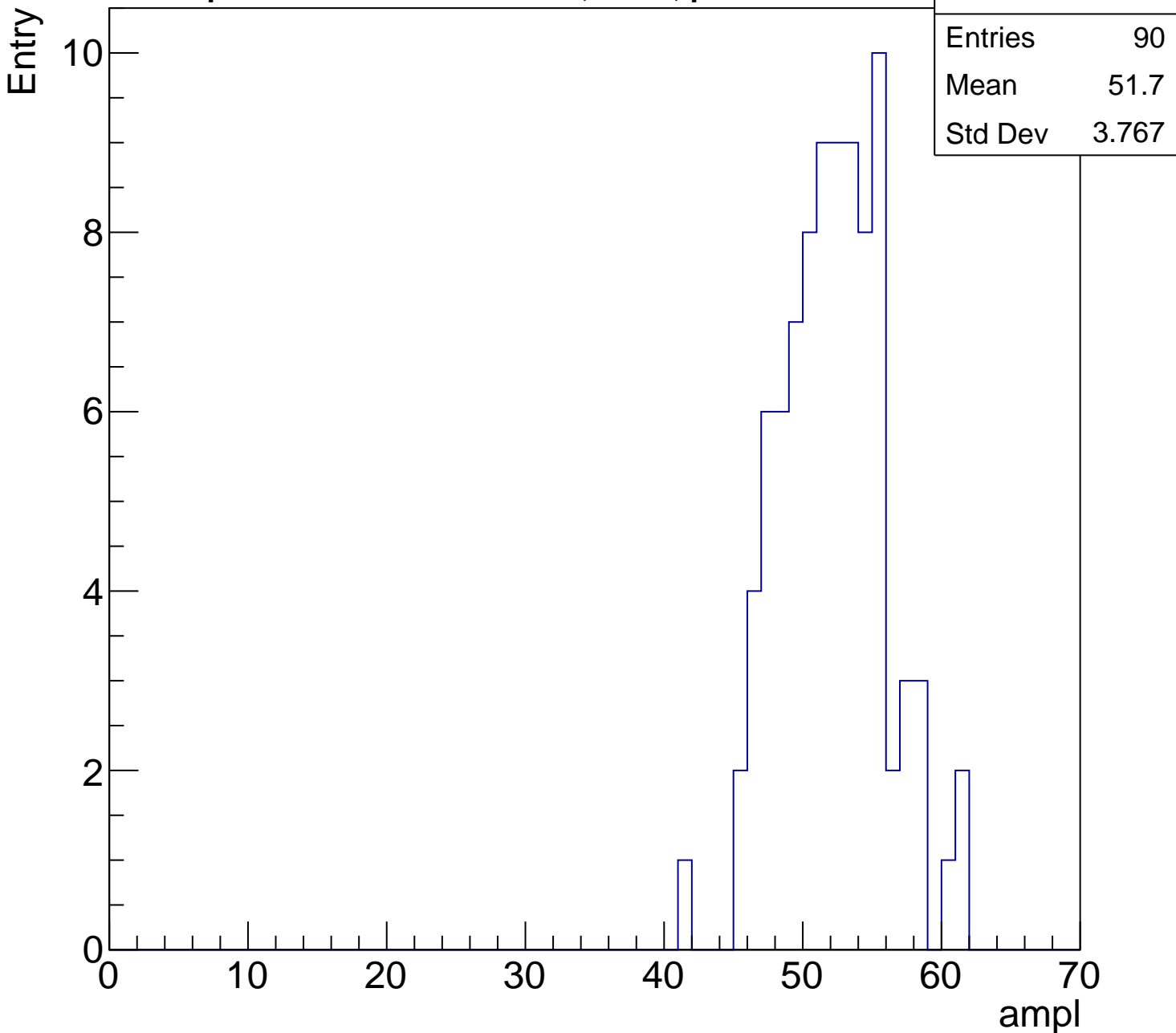
Entries	90
Mean	51.7
Std Dev	3.767

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

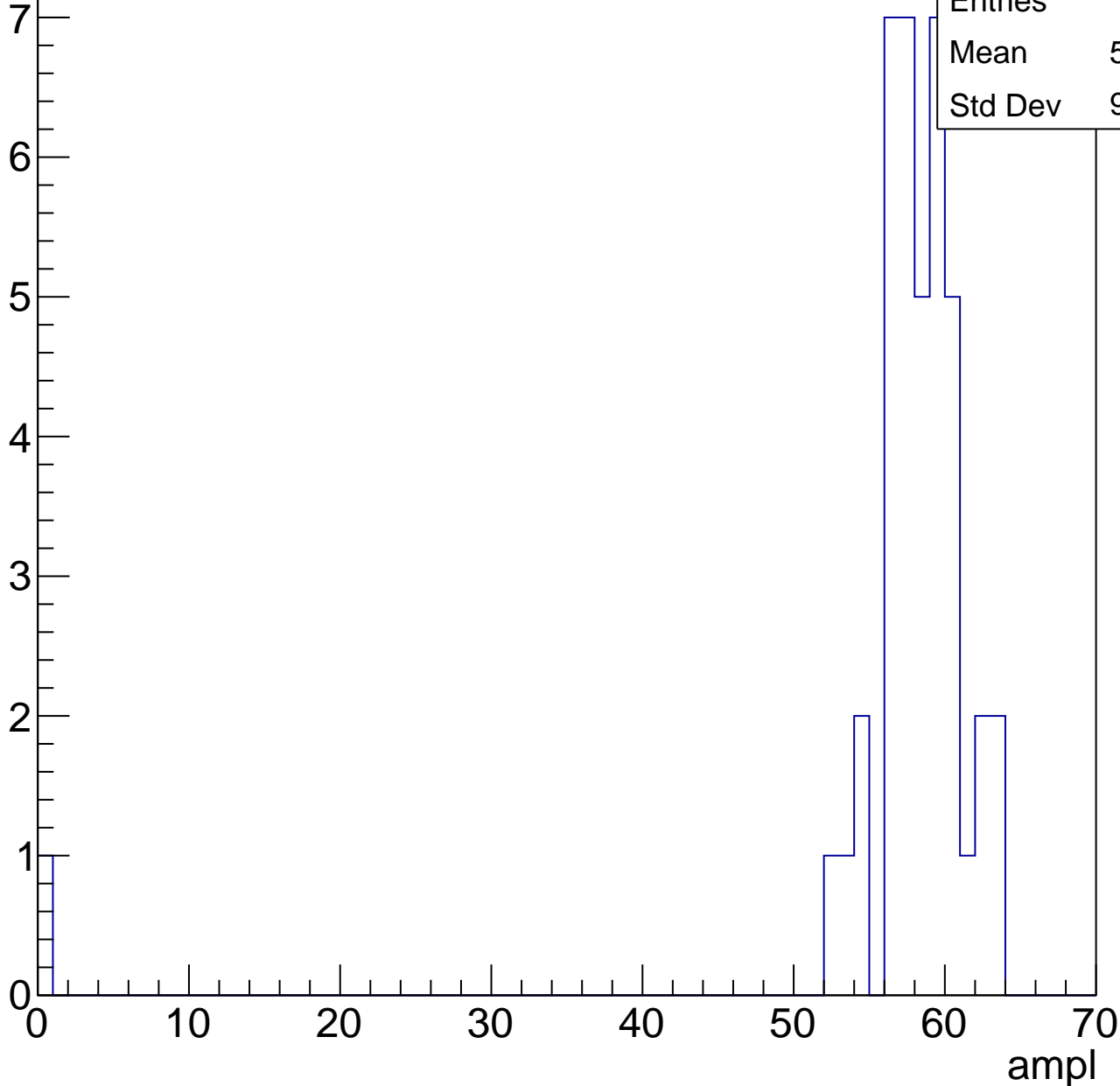


# B0L002S, U2-ch21, adc4

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	41
Mean	56.54
Std Dev	9.269

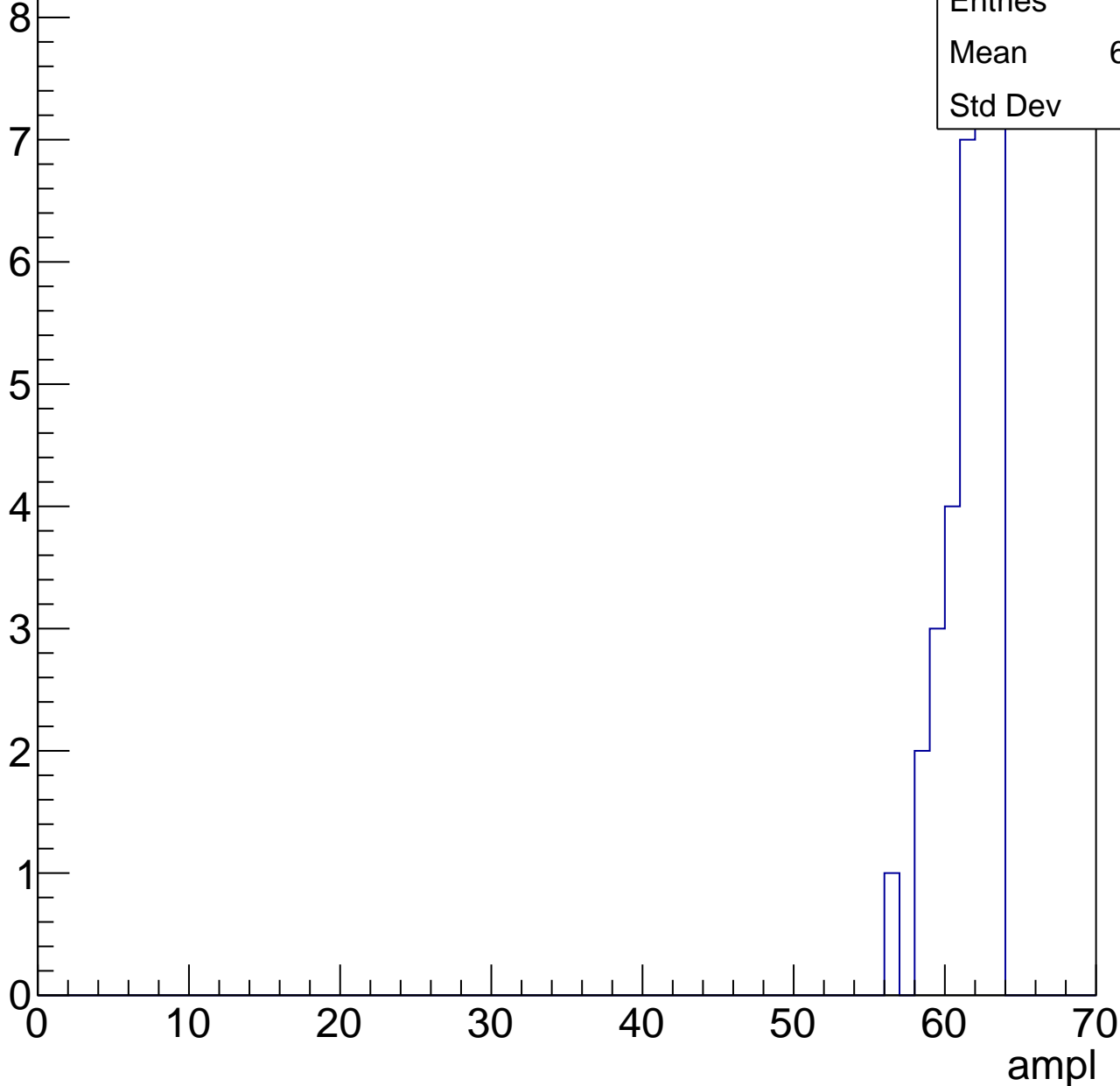


# B0L002S, U2-ch21, adc5

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	33
Mean	61.09
Std Dev	1.73



# B0L002S, U2-ch21, adc6

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



Entries	0
Mean	0
Std Dev	0



# B0L002S, U2-ch21, adc7

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L002S, U2-ch22, adc0

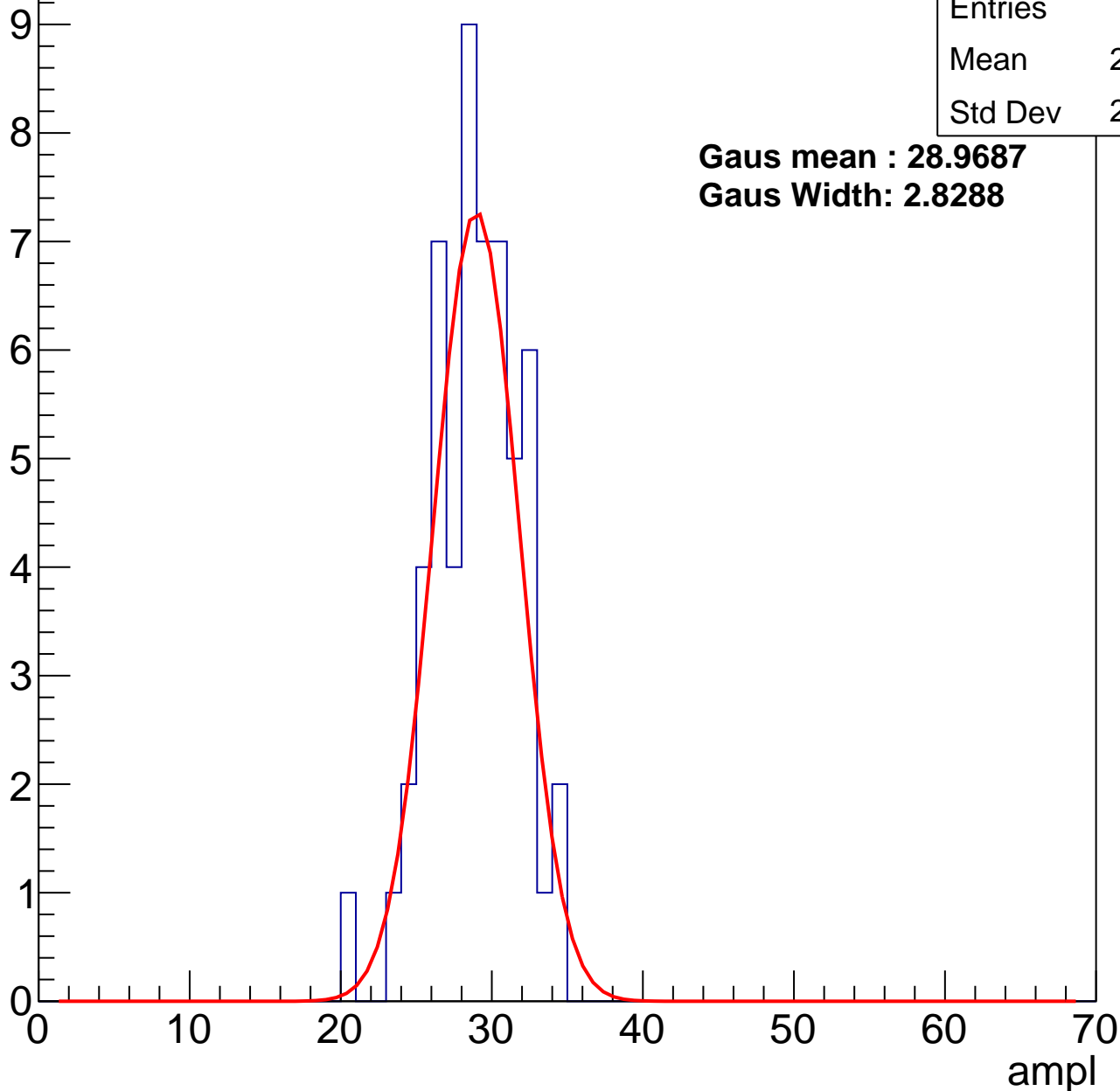
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	56
Mean	28.46
Std Dev	2.835

**Gaus mean : 28.9687**

**Gaus Width: 2.8288**



# B0L002S, U2-ch22, adc1

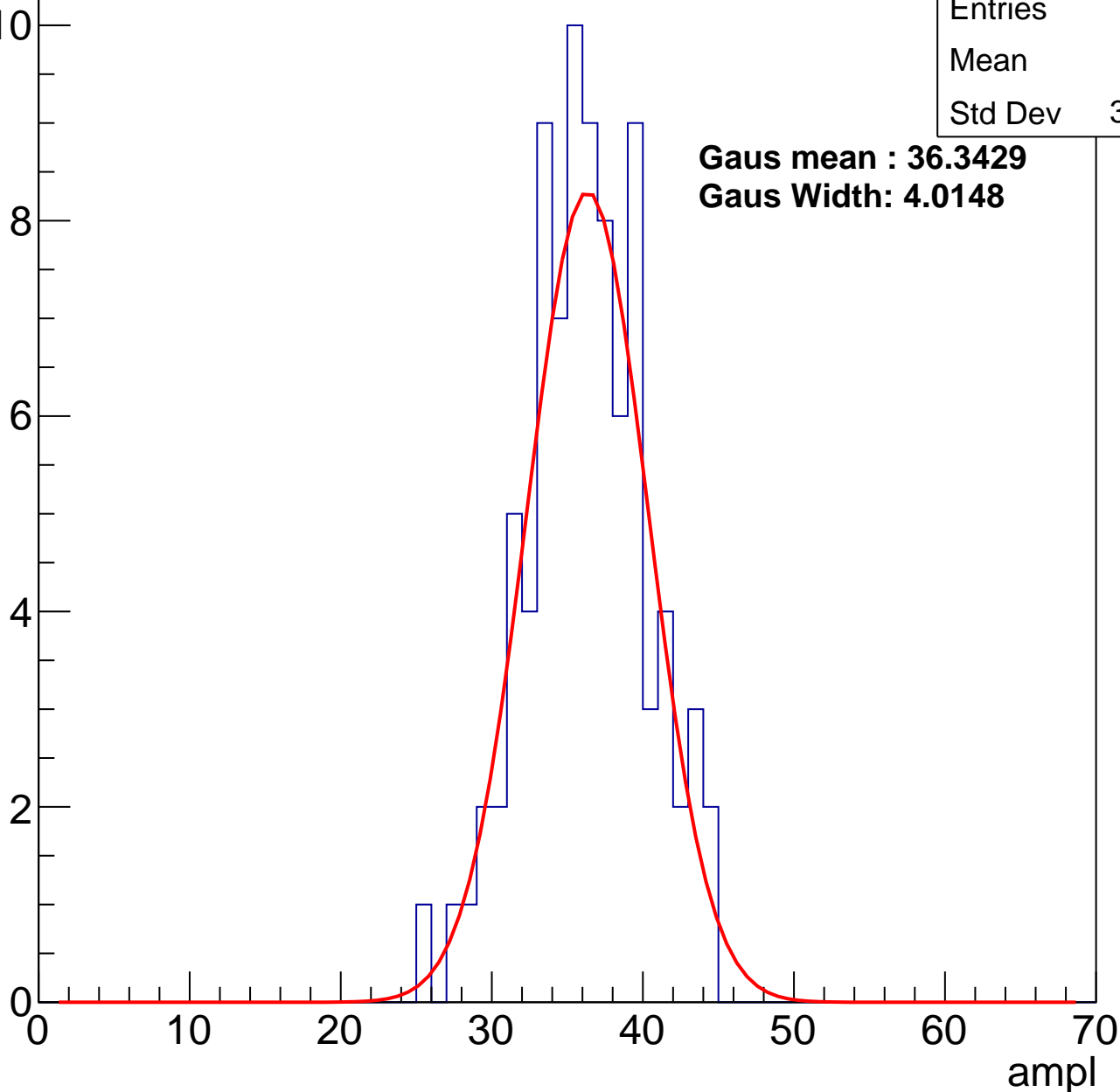
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	88
Mean	35.8
Std Dev	3.914

**Gaus mean : 36.3429**

**Gaus Width: 4.0148**



# B0L002S, U2-ch22, adc2

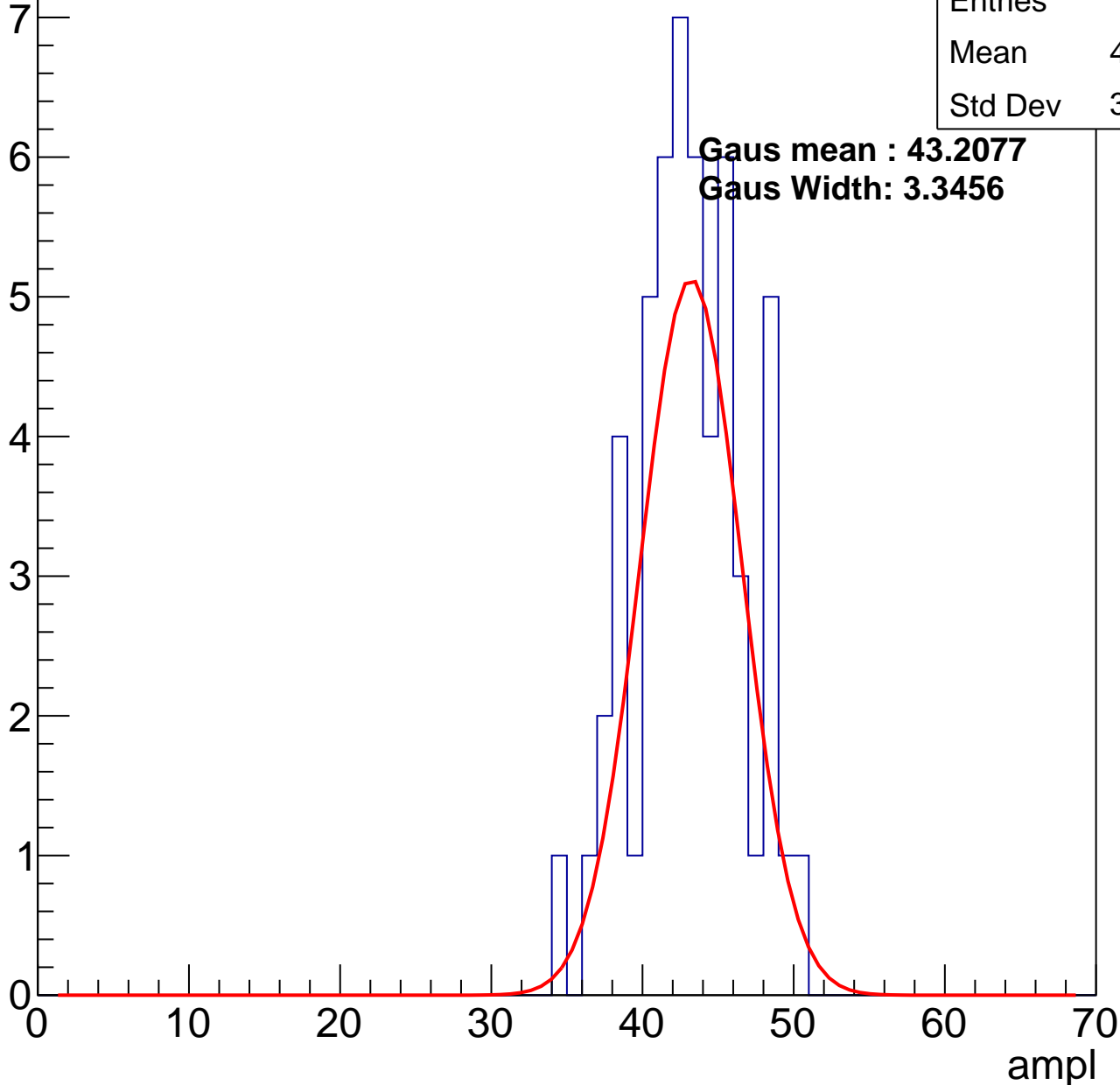
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	54
Mean	42.65
Std Dev	3.518

**Gaus mean : 43.2077**

**Gaus Width: 3.3456**

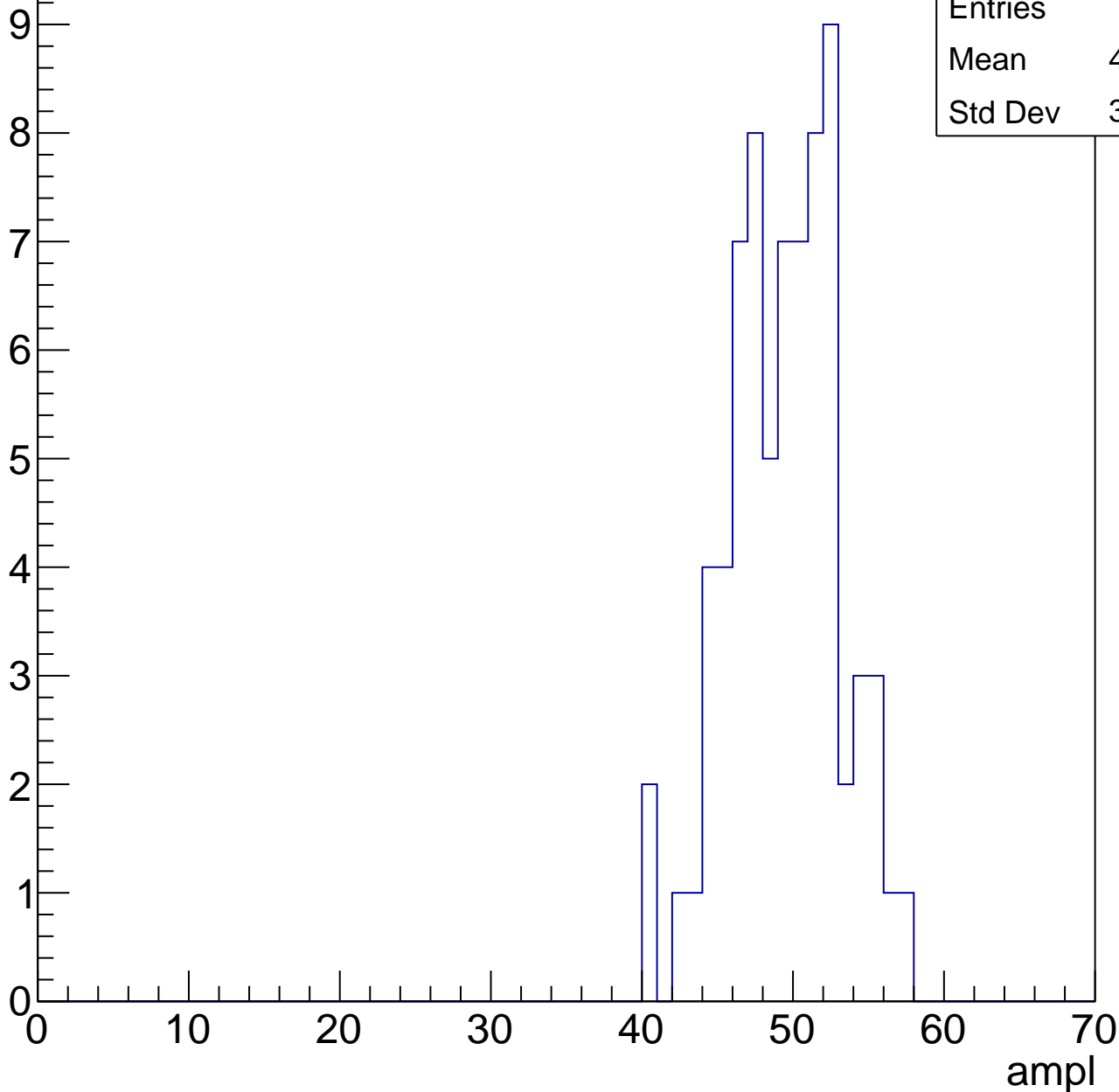


# B0L002S, U2-ch22, adc3

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

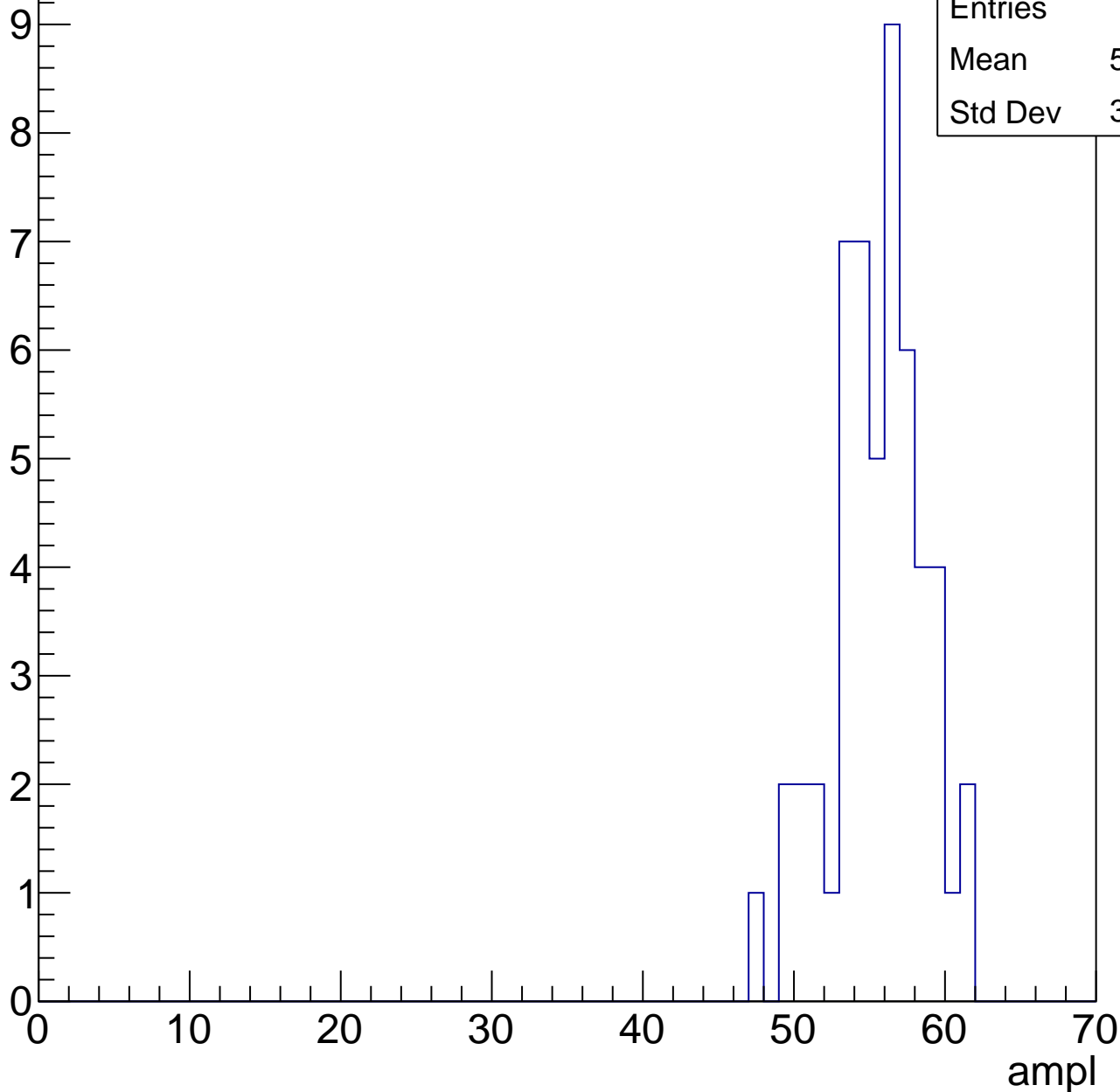
Entries	73
Mean	48.96
Std Dev	3.624



# B0L002S, U2-ch22, adc4

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

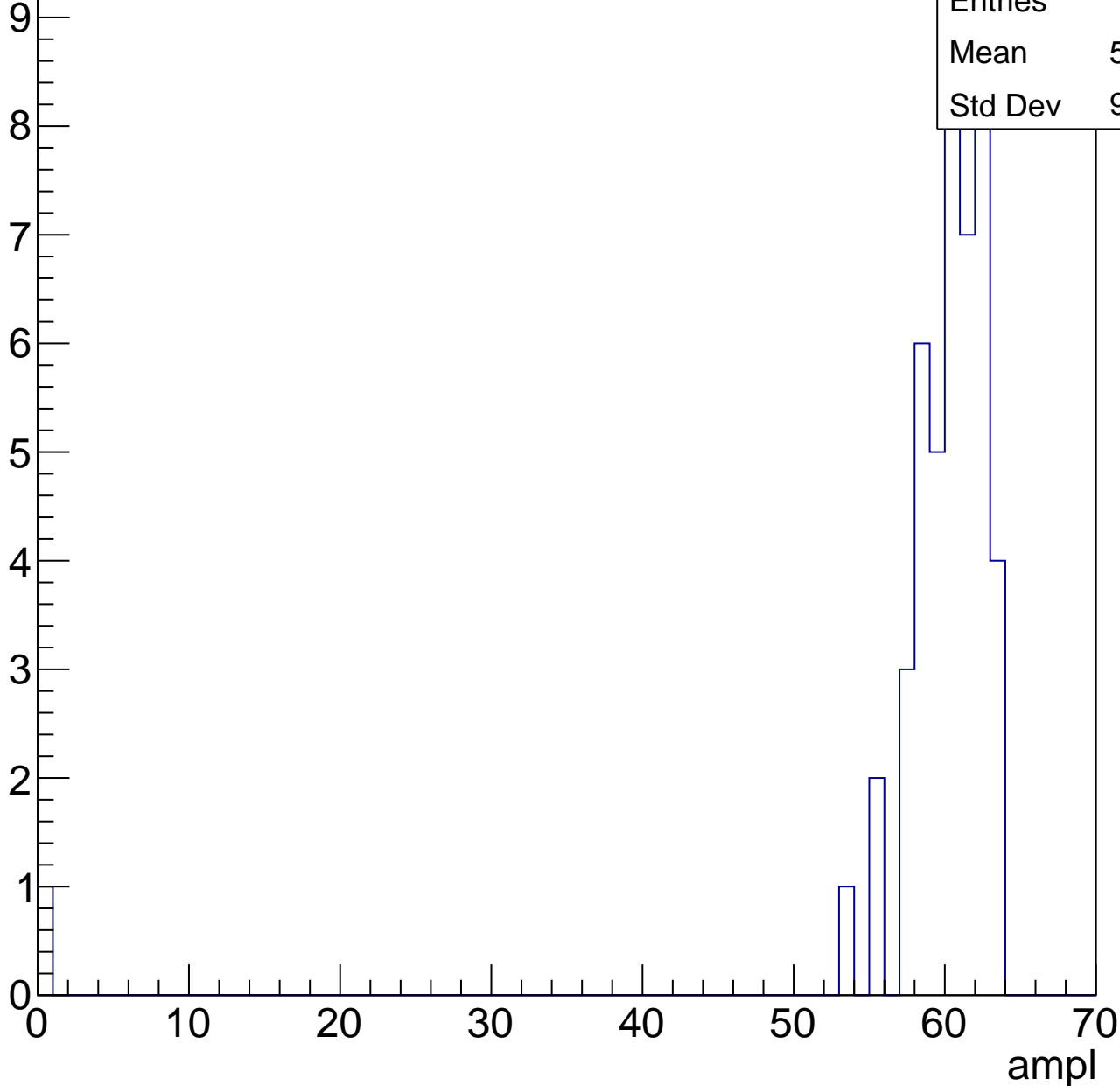


# B0L002S, U2-ch22, adc5

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	46
Mean	58.52
Std Dev	9.004

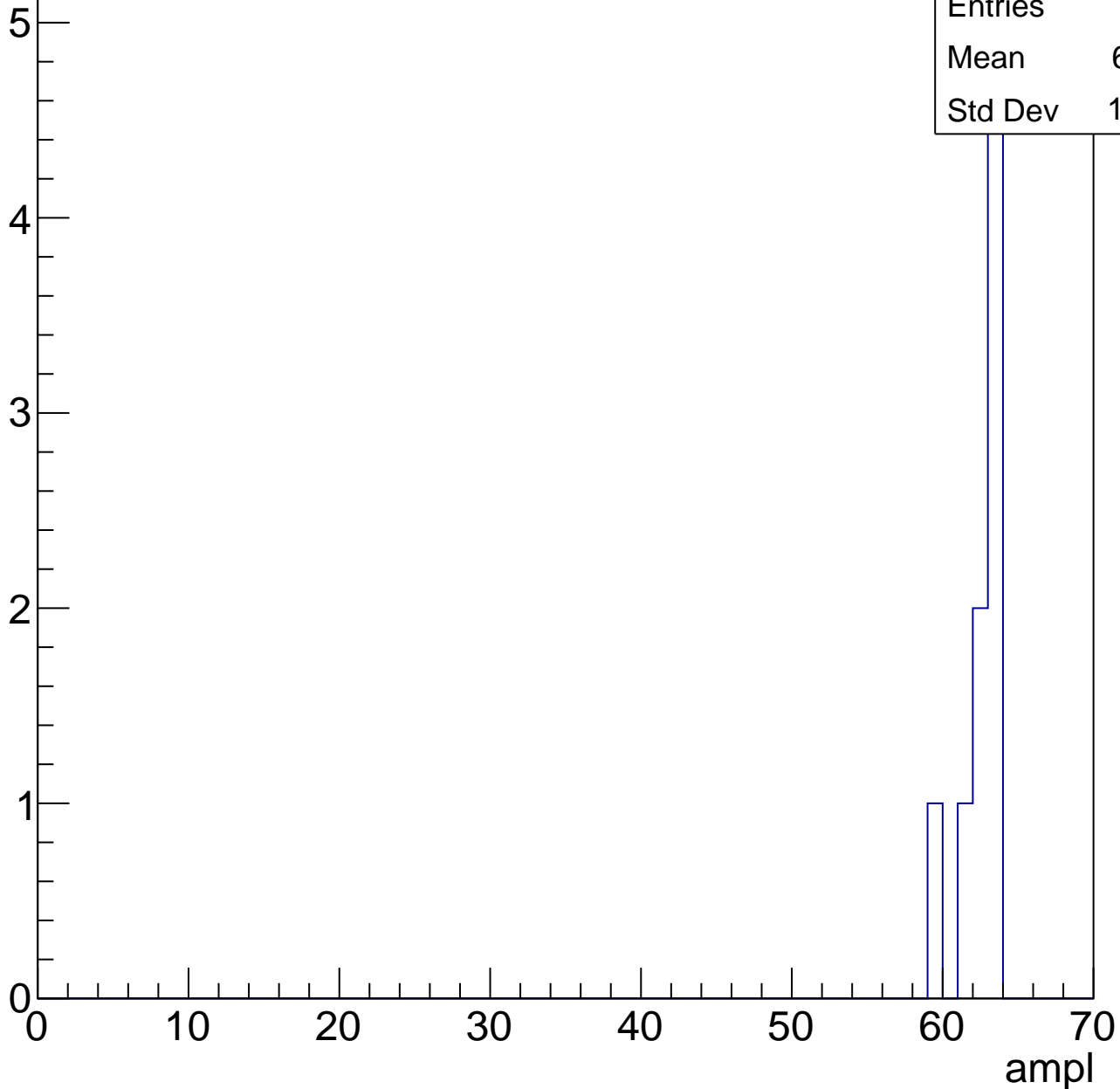


# B0L002S, U2-ch22, adc6

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	9
Mean	62.11
Std Dev	1.286





# B0L002S, U2-ch22, adc7

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



# B0L002S, U2-ch23, adc0

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entries	73
Mean	27.48
Std Dev	8.765

**Gaus mean : 30.4601**

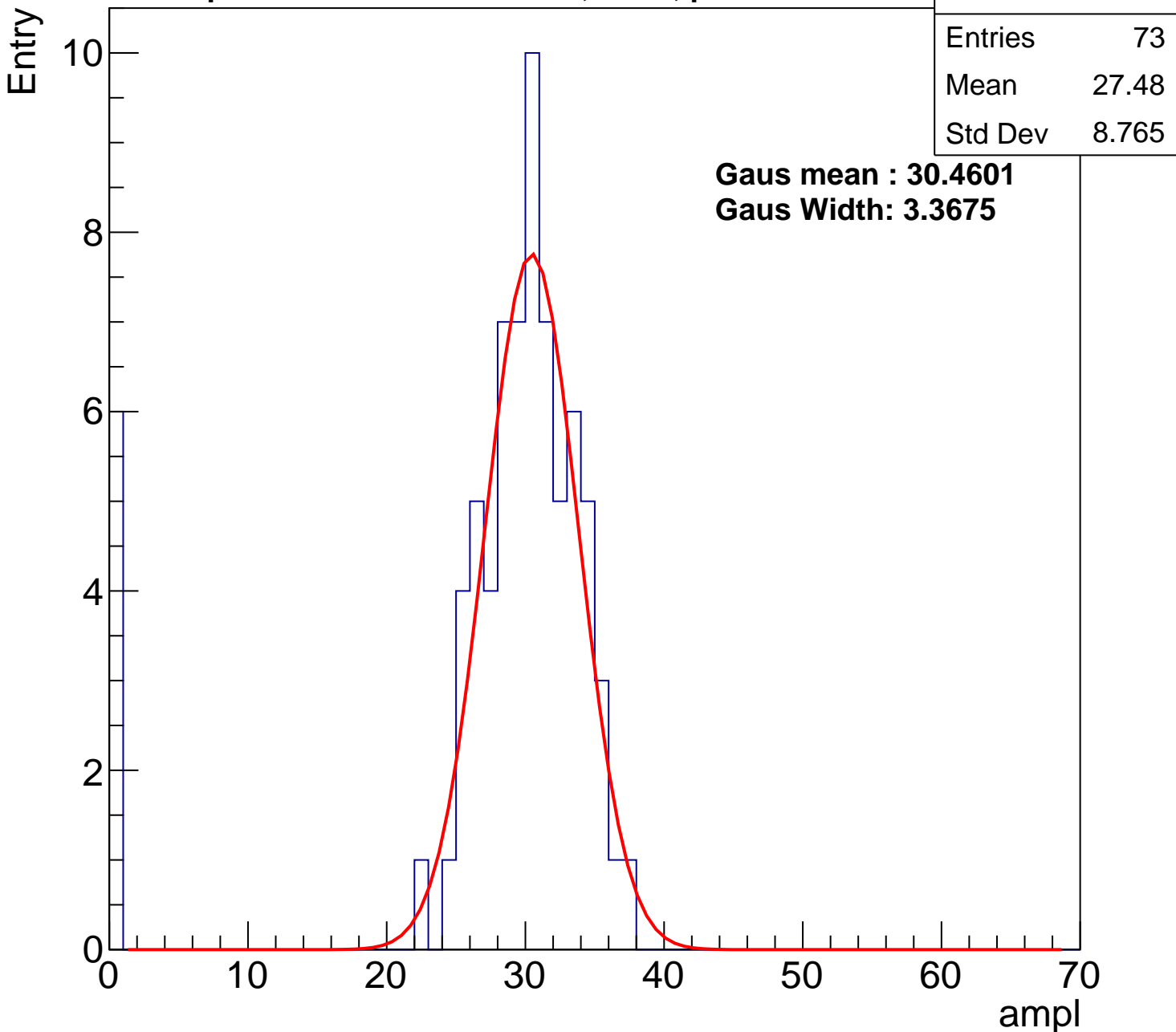
**Gaus Width: 3.3675**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B0L002S, U2-ch23, adc1

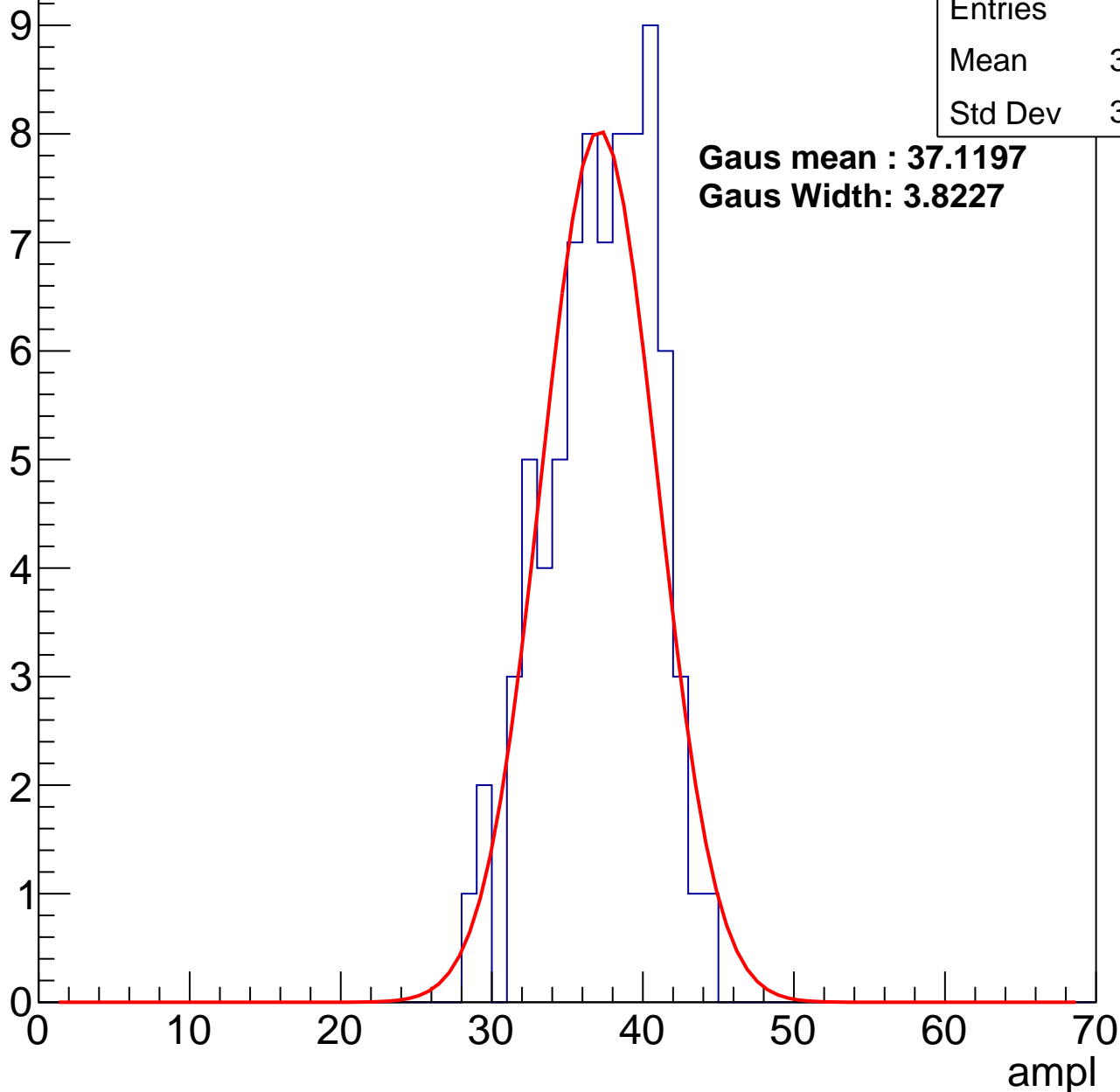
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	78
Mean	36.77
Std Dev	3.508

**Gaus mean : 37.1197**

**Gaus Width: 3.8227**



# B0L002S, U2-ch23, adc2

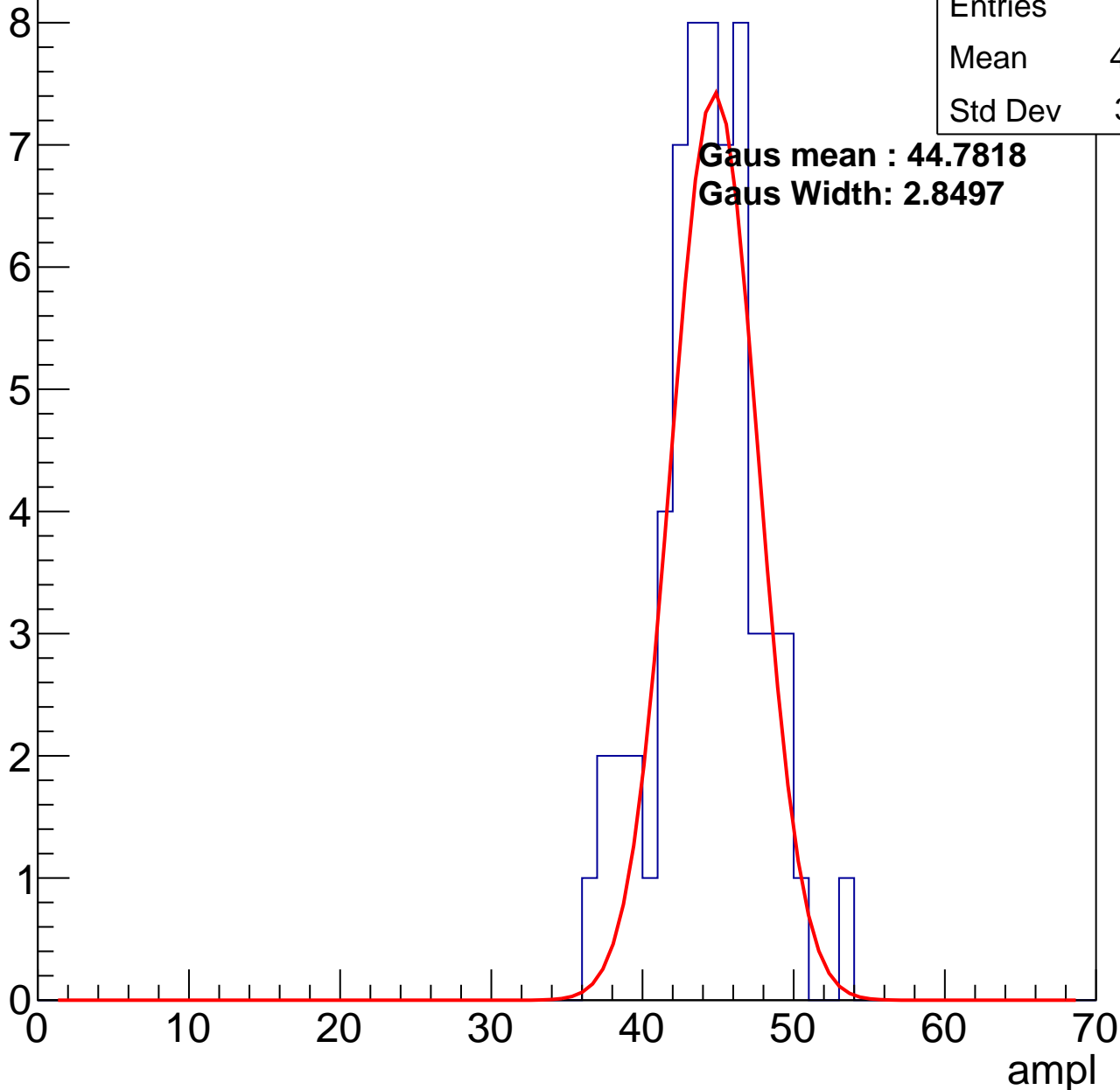
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	61
Mean	43.87
Std Dev	3.331

**Gaus mean : 44.7818**

**Gaus Width: 2.8497**

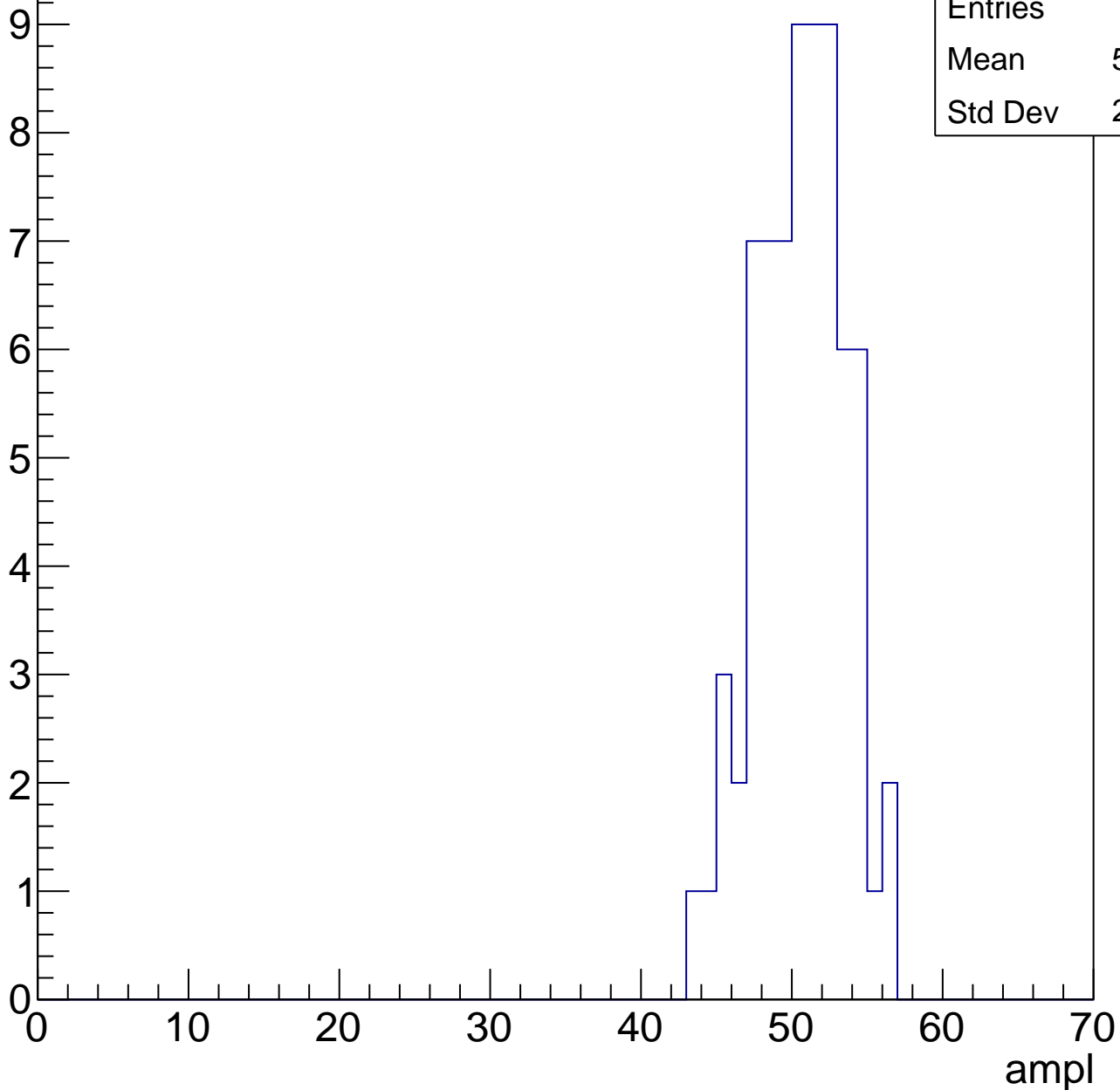


# B0L002S, U2-ch23, adc3

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	70
Mean	50.11
Std Dev	2.881

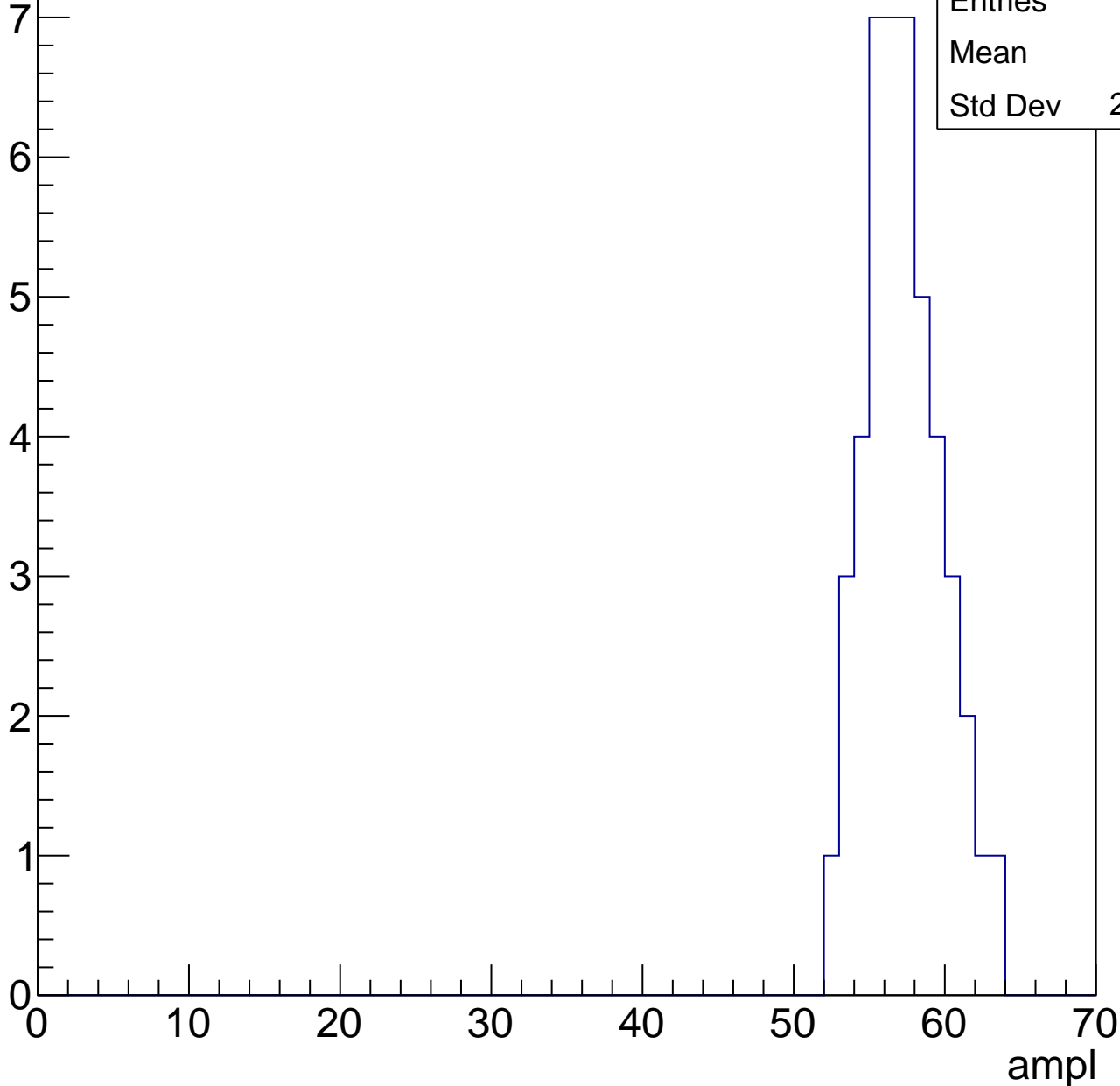


# B0L002S, U2-ch23, adc4

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	45
Mean	56.8
Std Dev	2.509



# B0L002S, U2-ch23, adc5

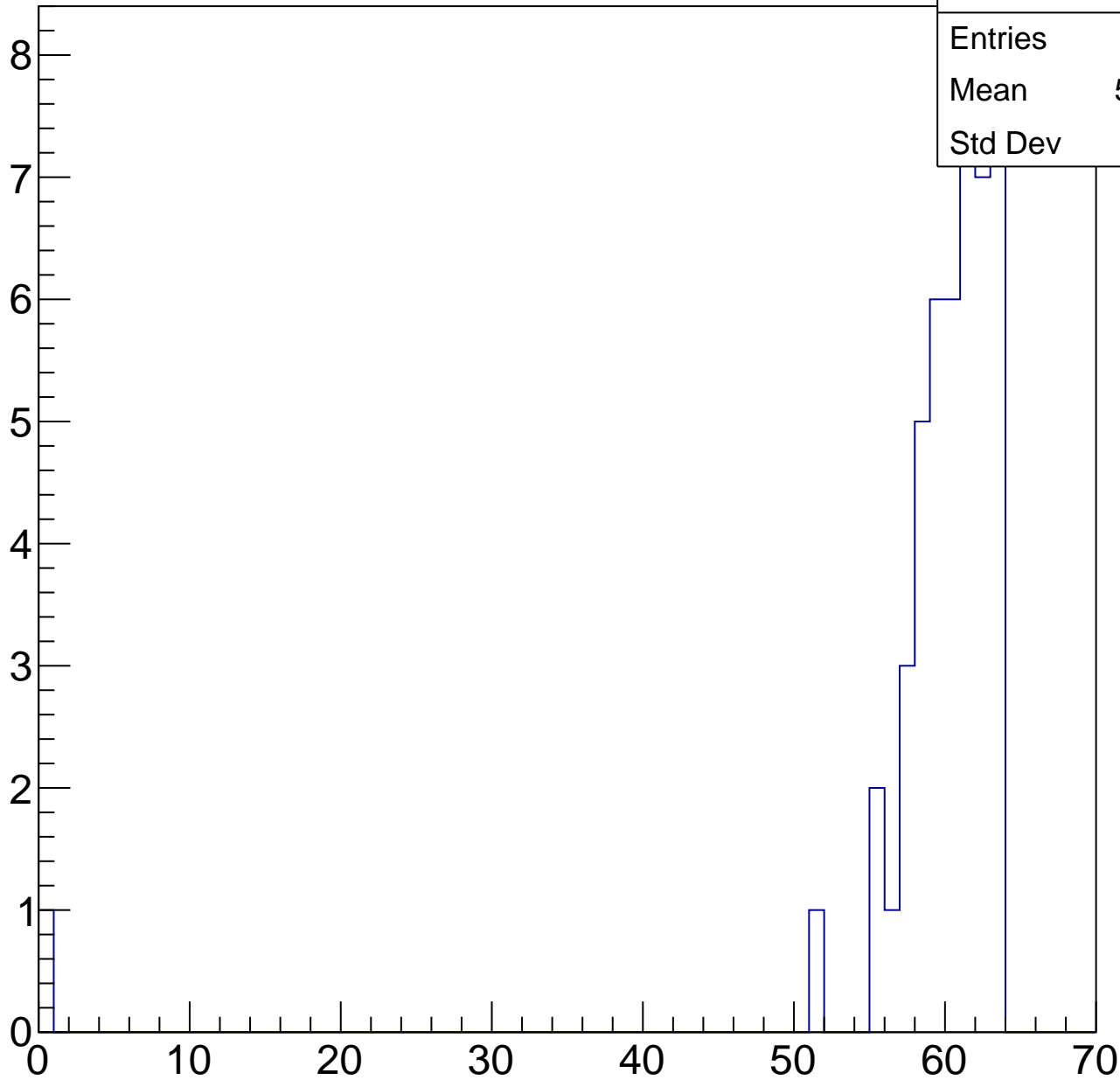
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	48
Mean	58.71
Std Dev	8.93

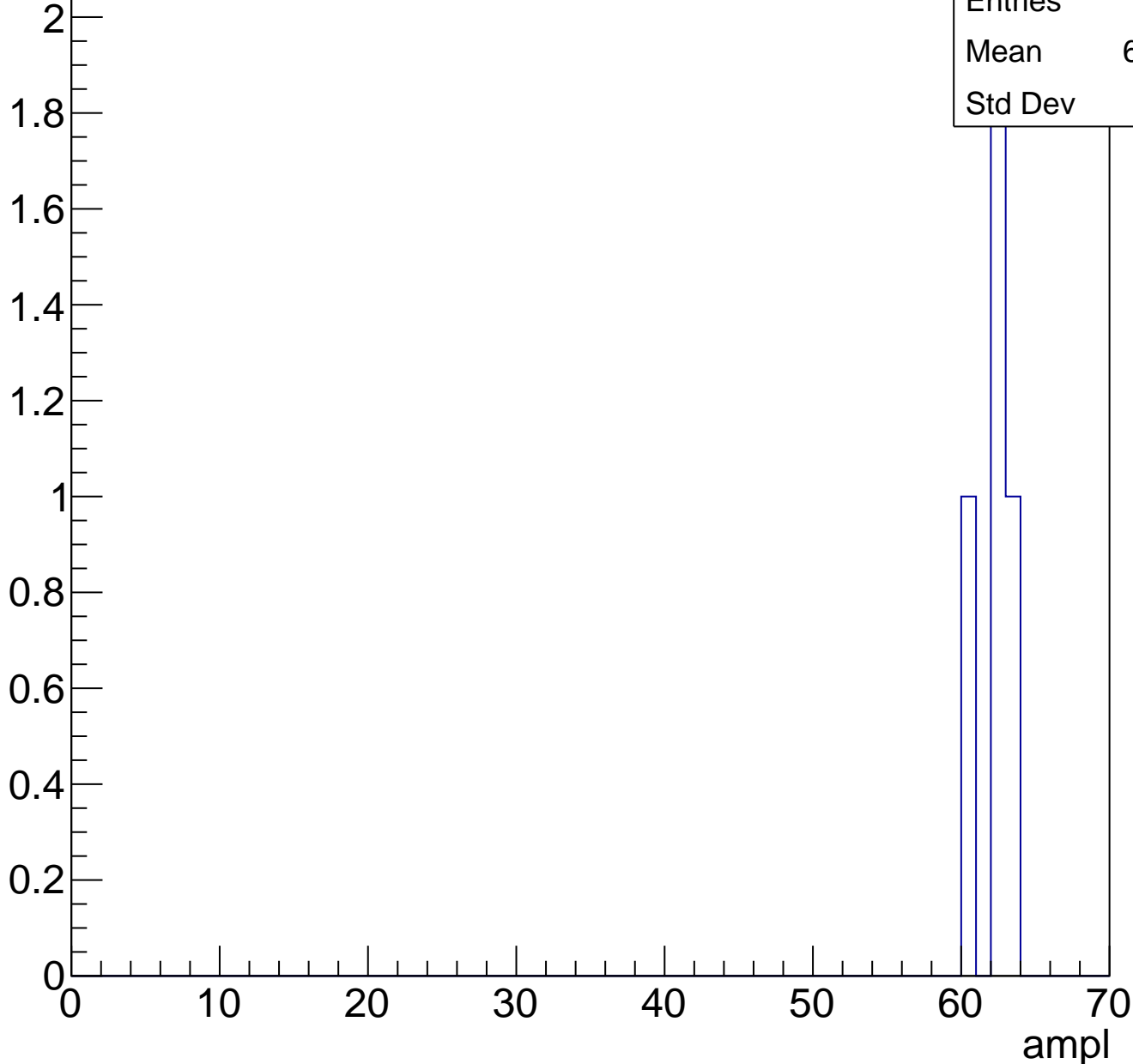
ampl



# B0L002S, U2-ch23, adc6

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry





# B0L002S, U2-ch23, adc7

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



Entries	2
Mean	0
Std Dev	0

# B0L002S, U2-ch24, adc0

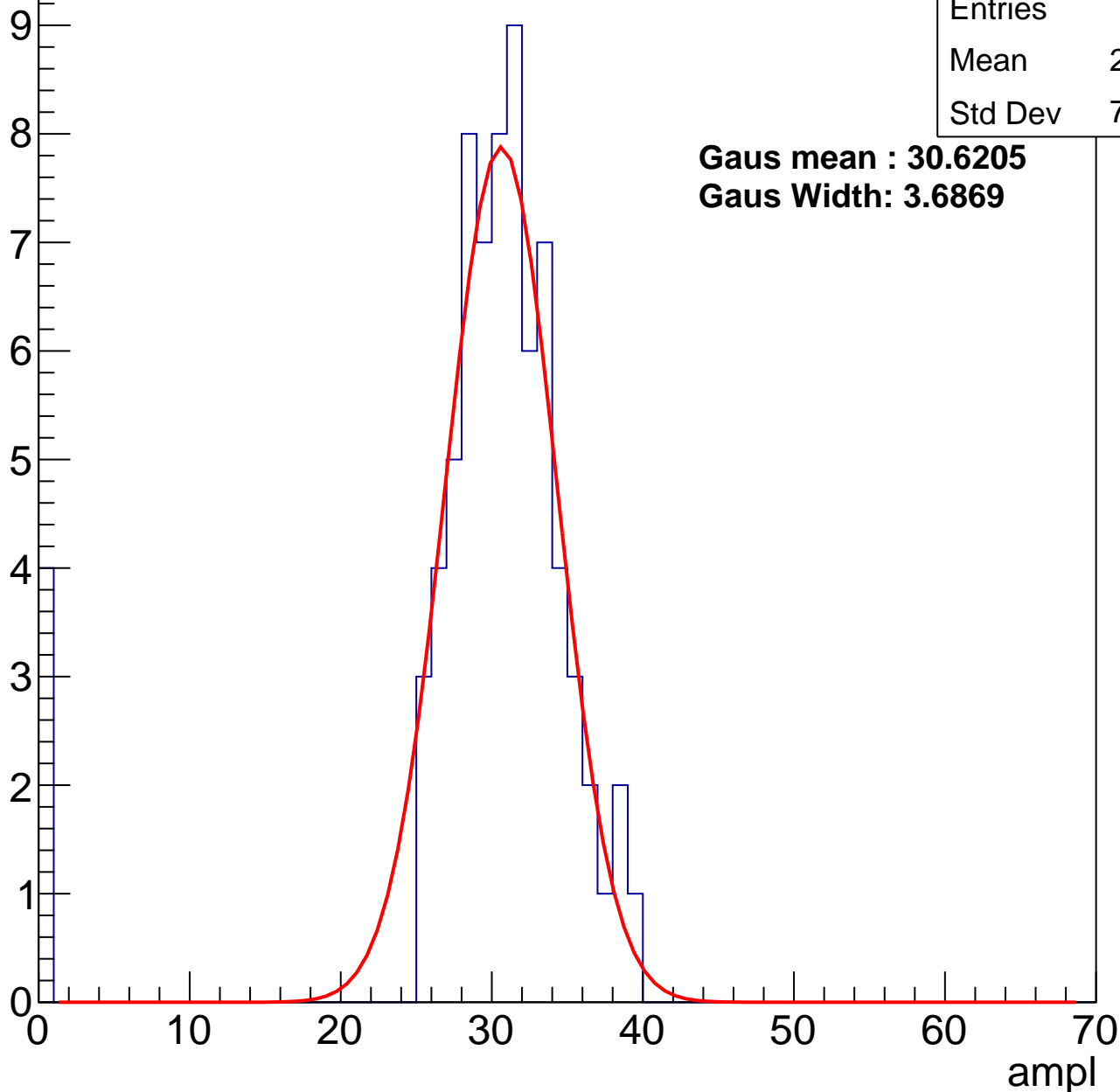
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	74
Mean	29.03
Std Dev	7.639

**Gaus mean : 30.6205**

**Gaus Width: 3.6869**



# B0L002S, U2-ch24, adc1

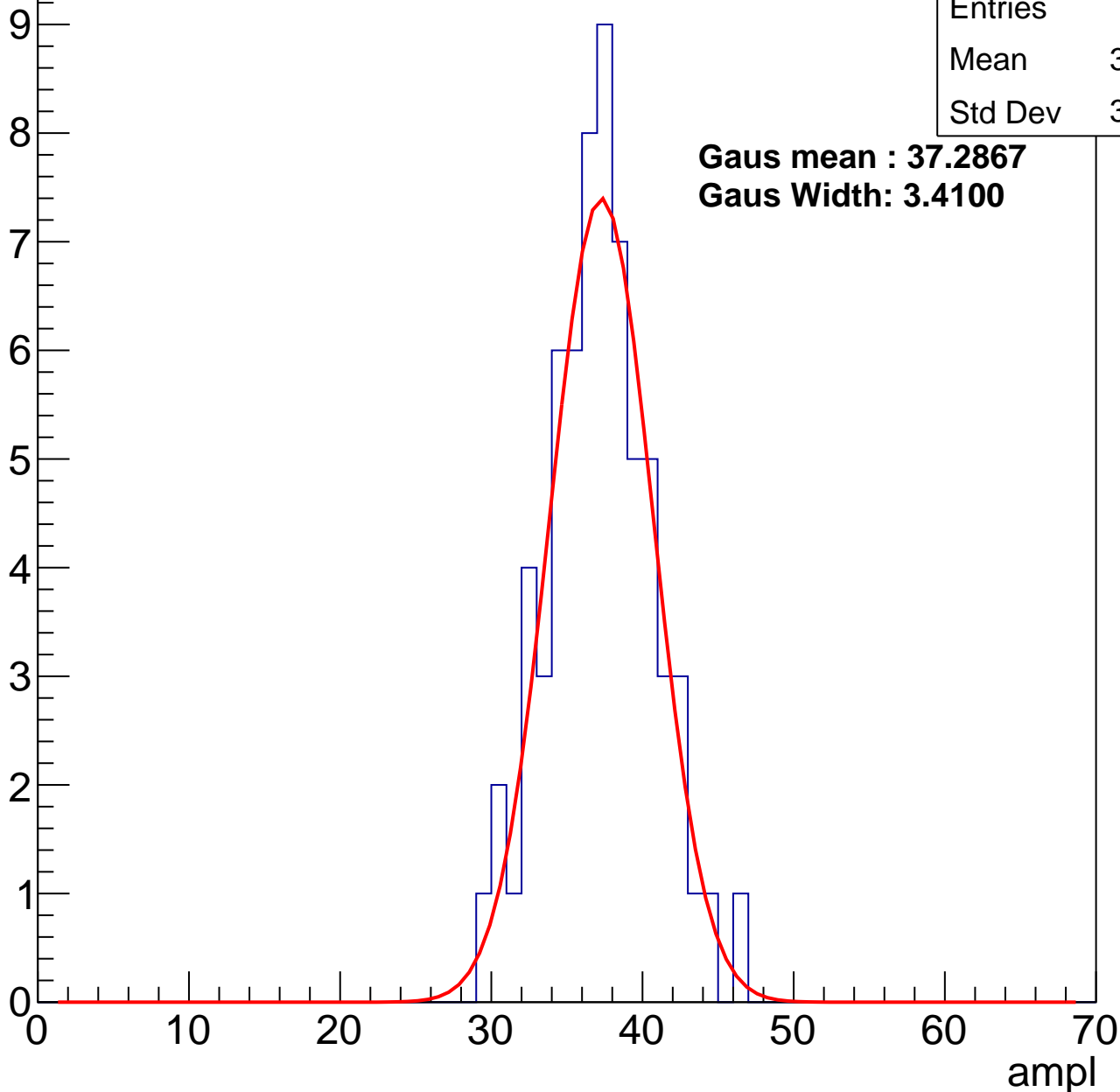
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	66
Mean	36.74
Std Dev	3.457

**Gaus mean : 37.2867**

**Gaus Width: 3.4100**



# B0L002S, U2-ch24, adc2

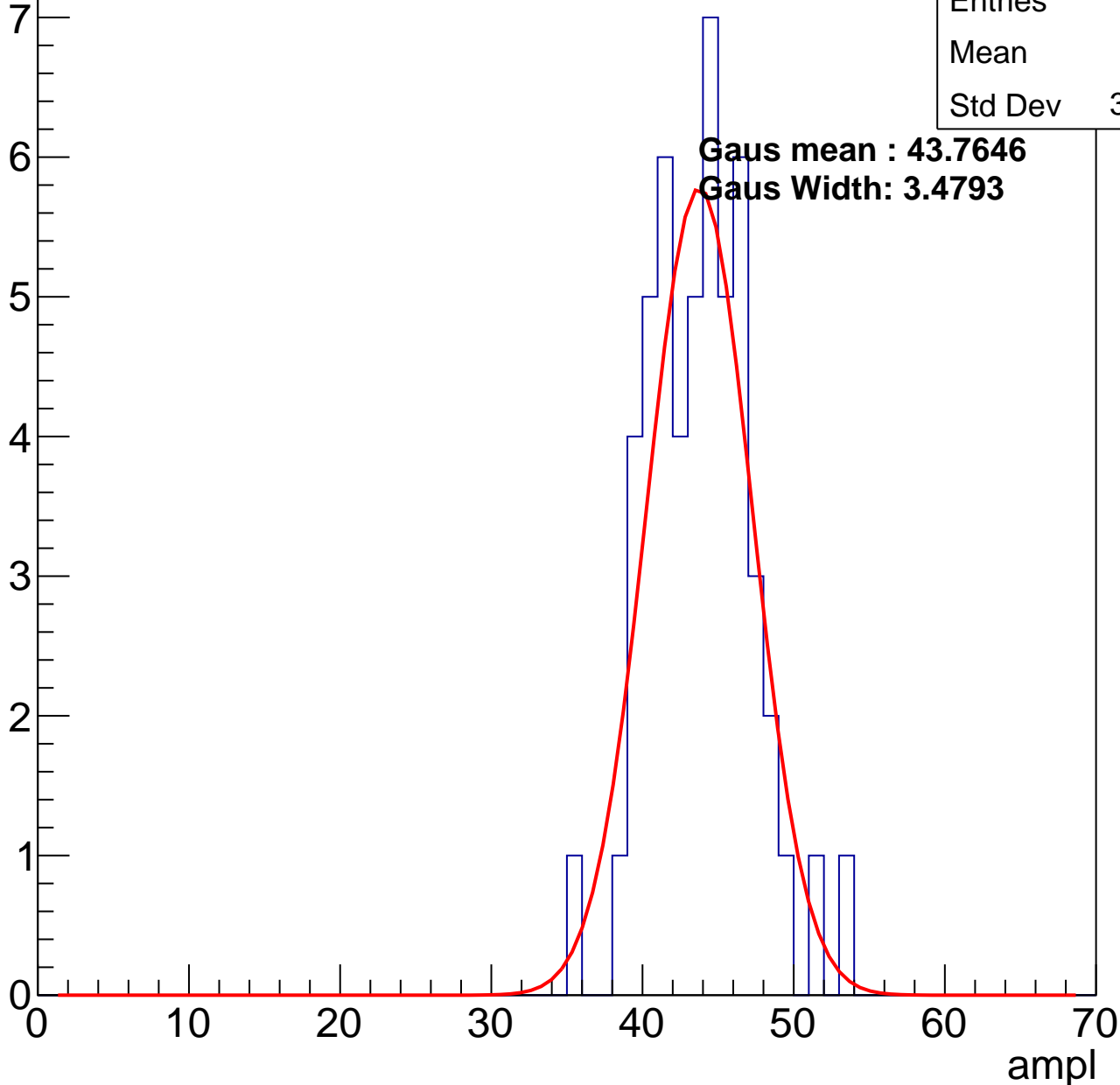
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	52
Mean	43.4
Std Dev	3.387

**Gaus mean : 43.7646**

**Gaus Width: 3.4793**

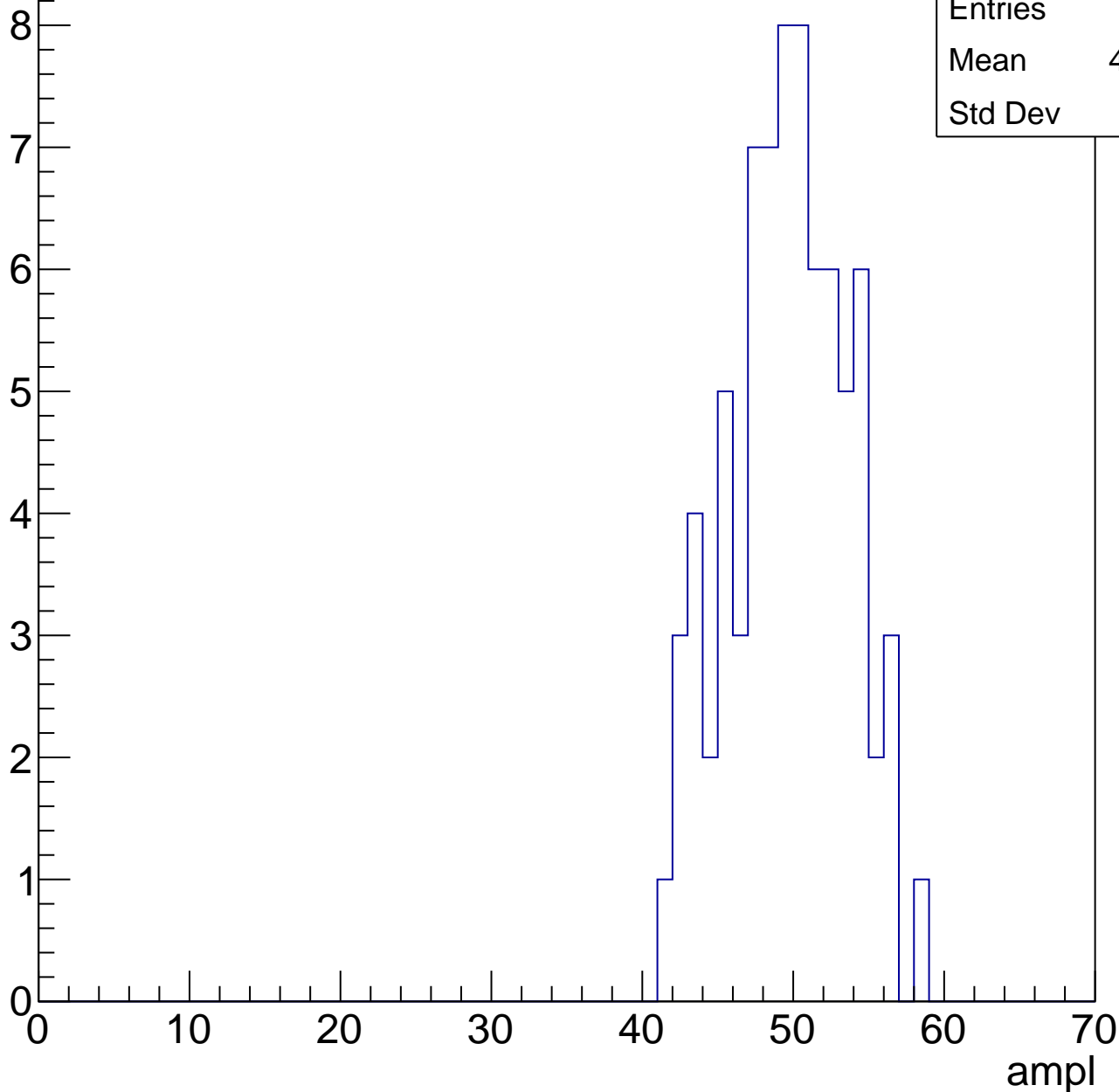


# B0L002S, U2-ch24, adc3

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

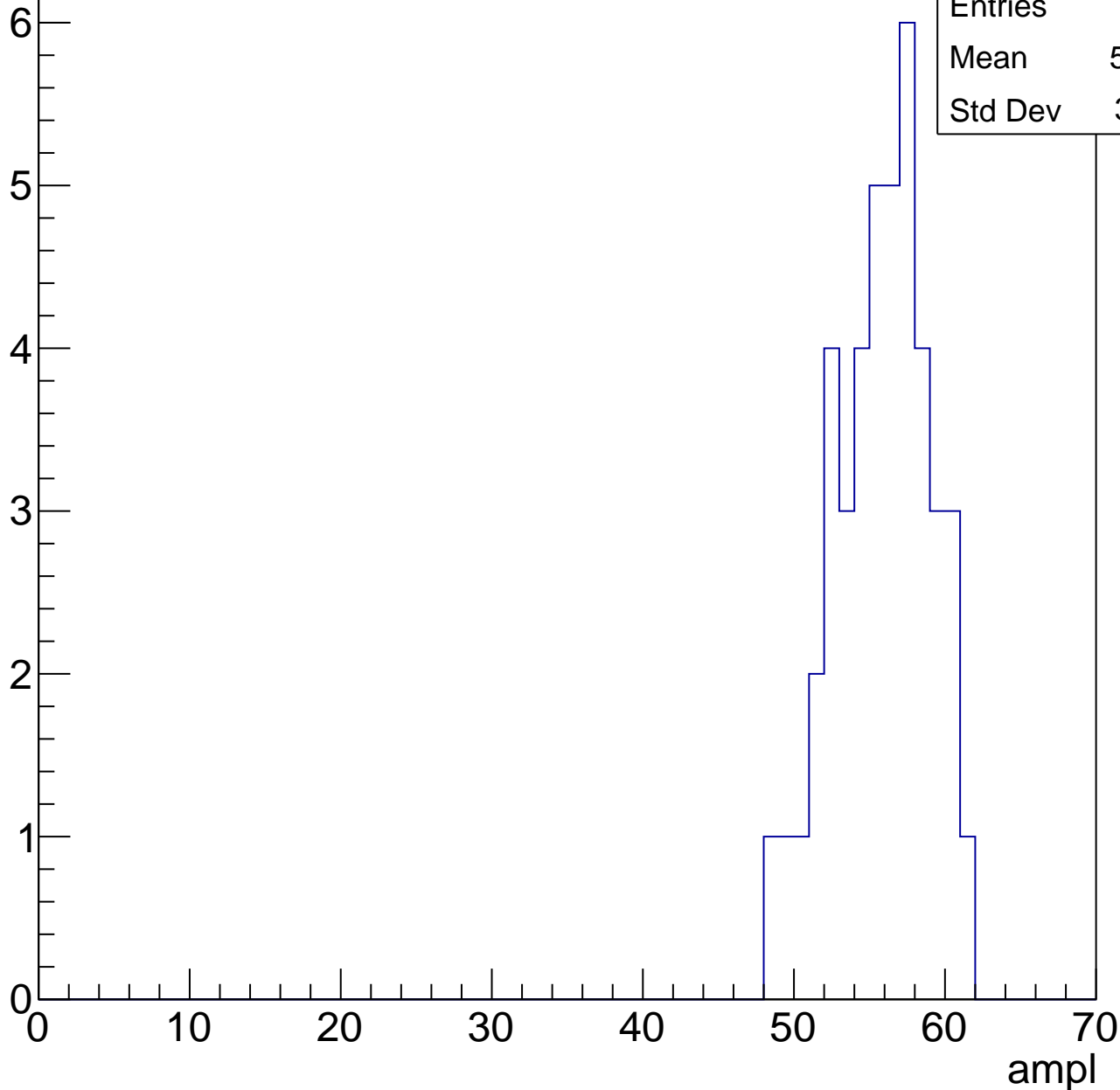
Entries	77
Mean	49.22
Std Dev	3.88



# B0L002S, U2-ch24, adc4

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

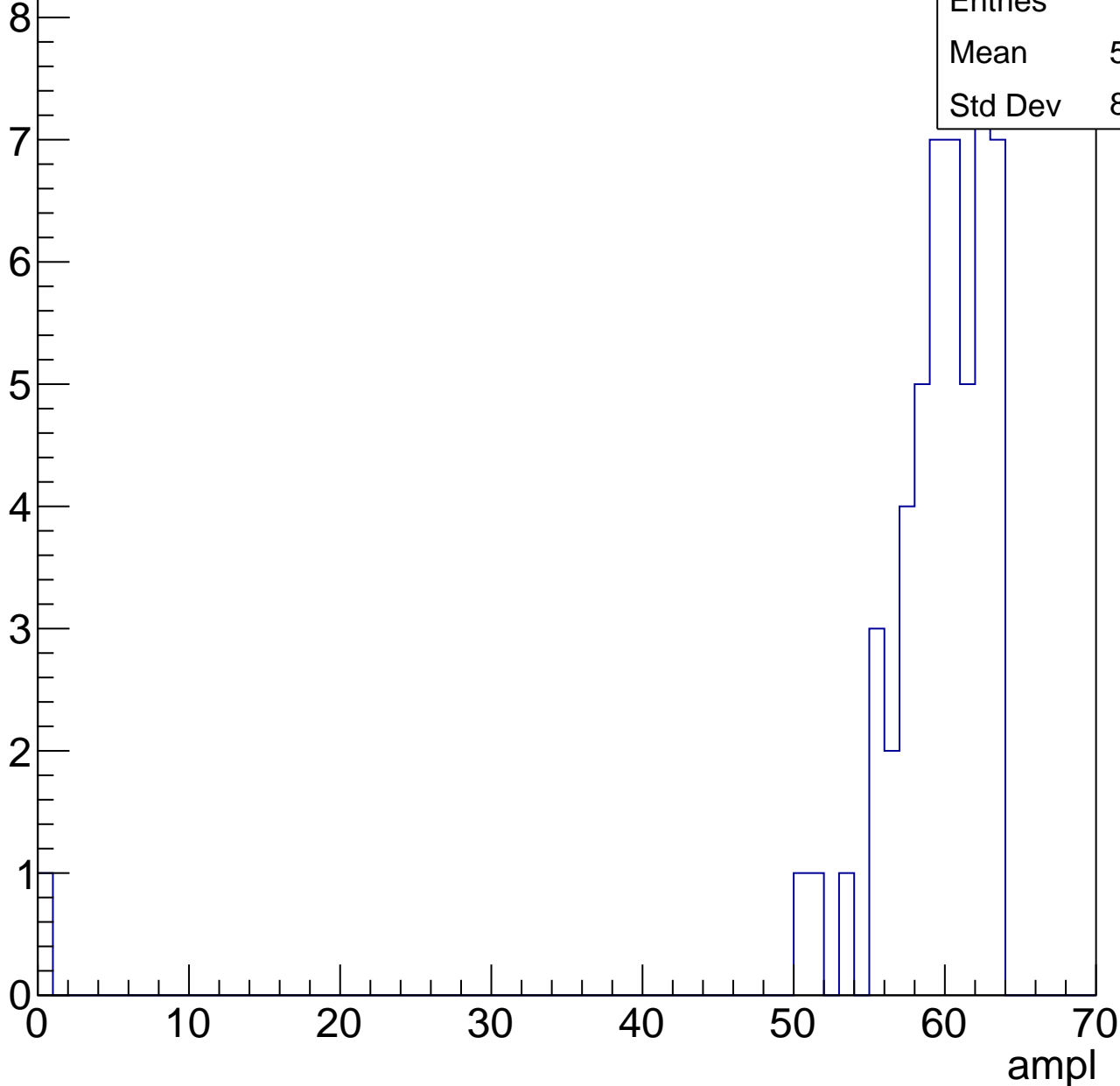


# B0L002S, U2-ch24, adc5

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

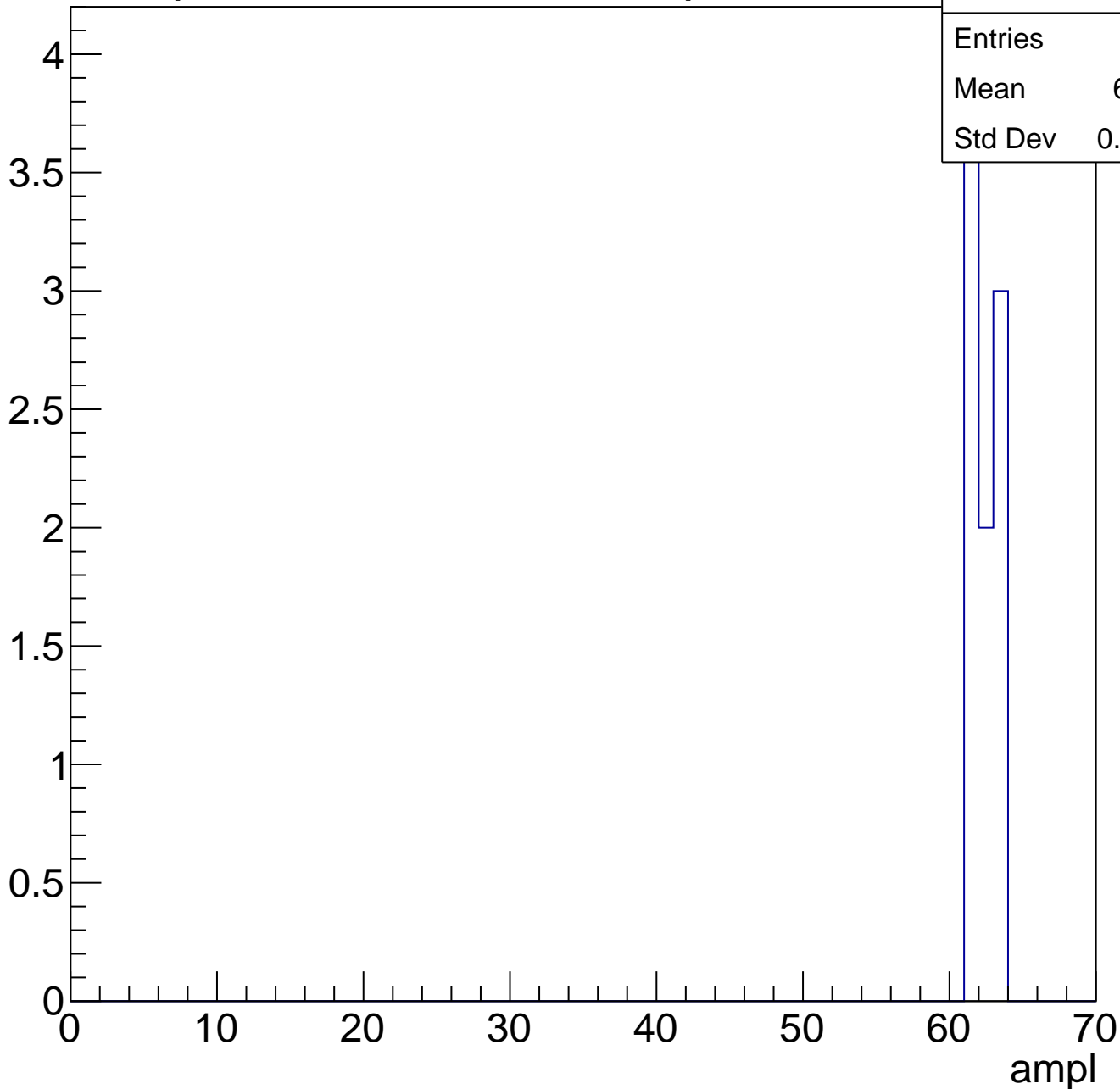
Entries	52
Mean	58.15
Std Dev	8.685



# B0L002S, U2-ch24, adc6

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

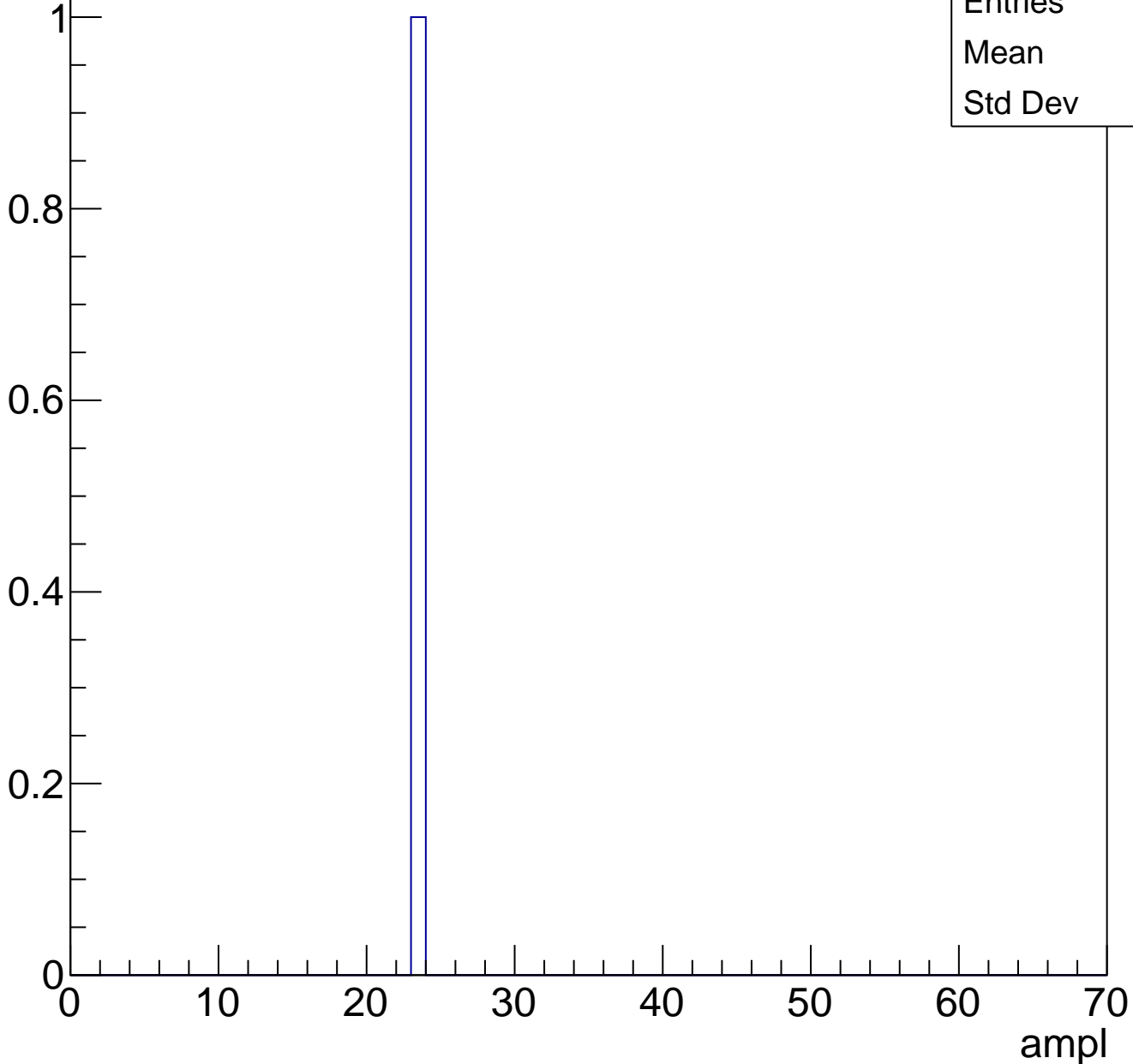




# B0L002S, U2-ch24, adc7

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



# B0L002S, U2-ch25, adc0

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entries	77
Mean	30.09
Std Dev	3.151

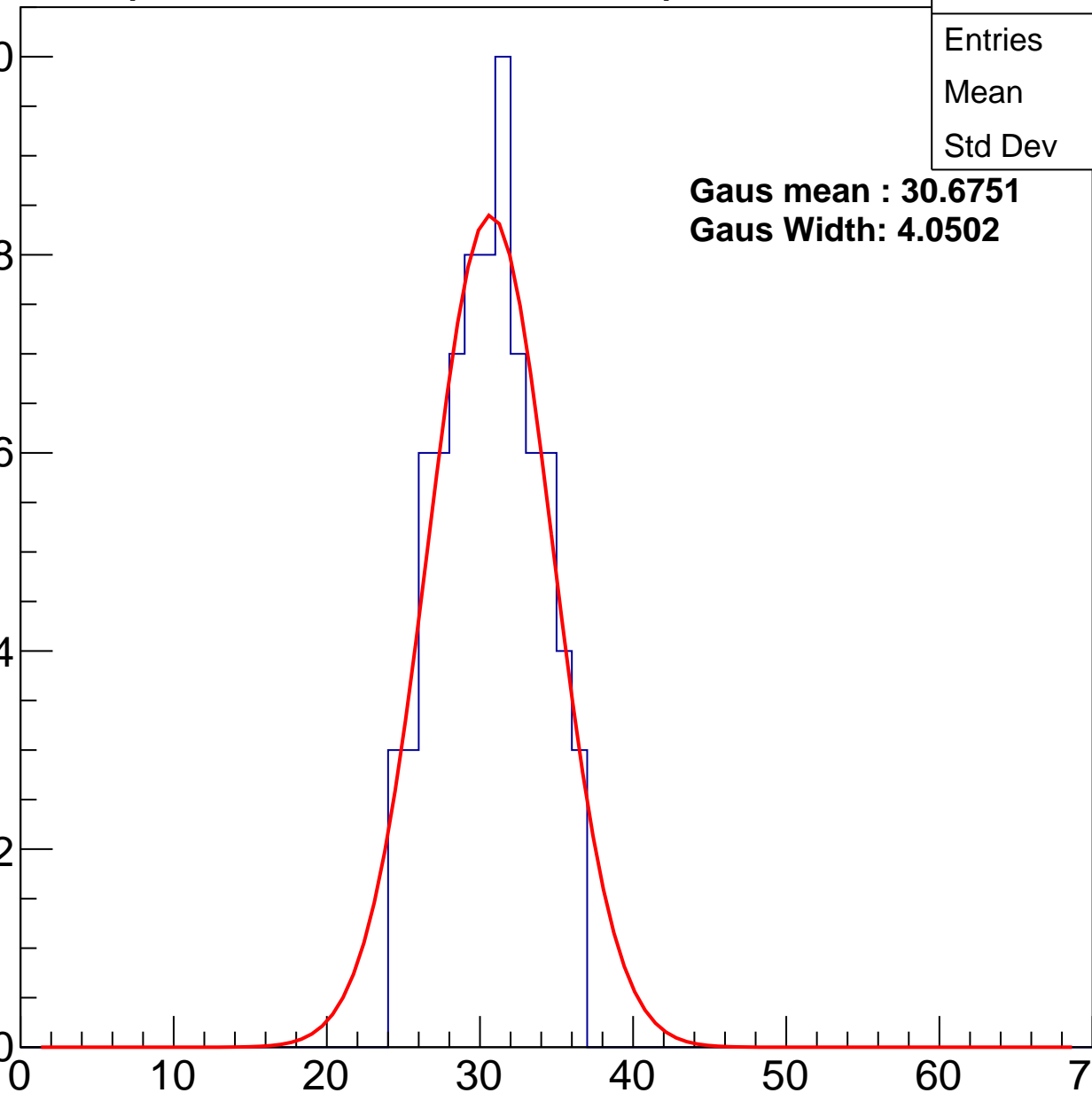
**Gaus mean : 30.6751**

**Gaus Width: 4.0502**

Entry

10  
8  
6  
4  
2  
0

ampl



# B0L002S, U2-ch25, adc1

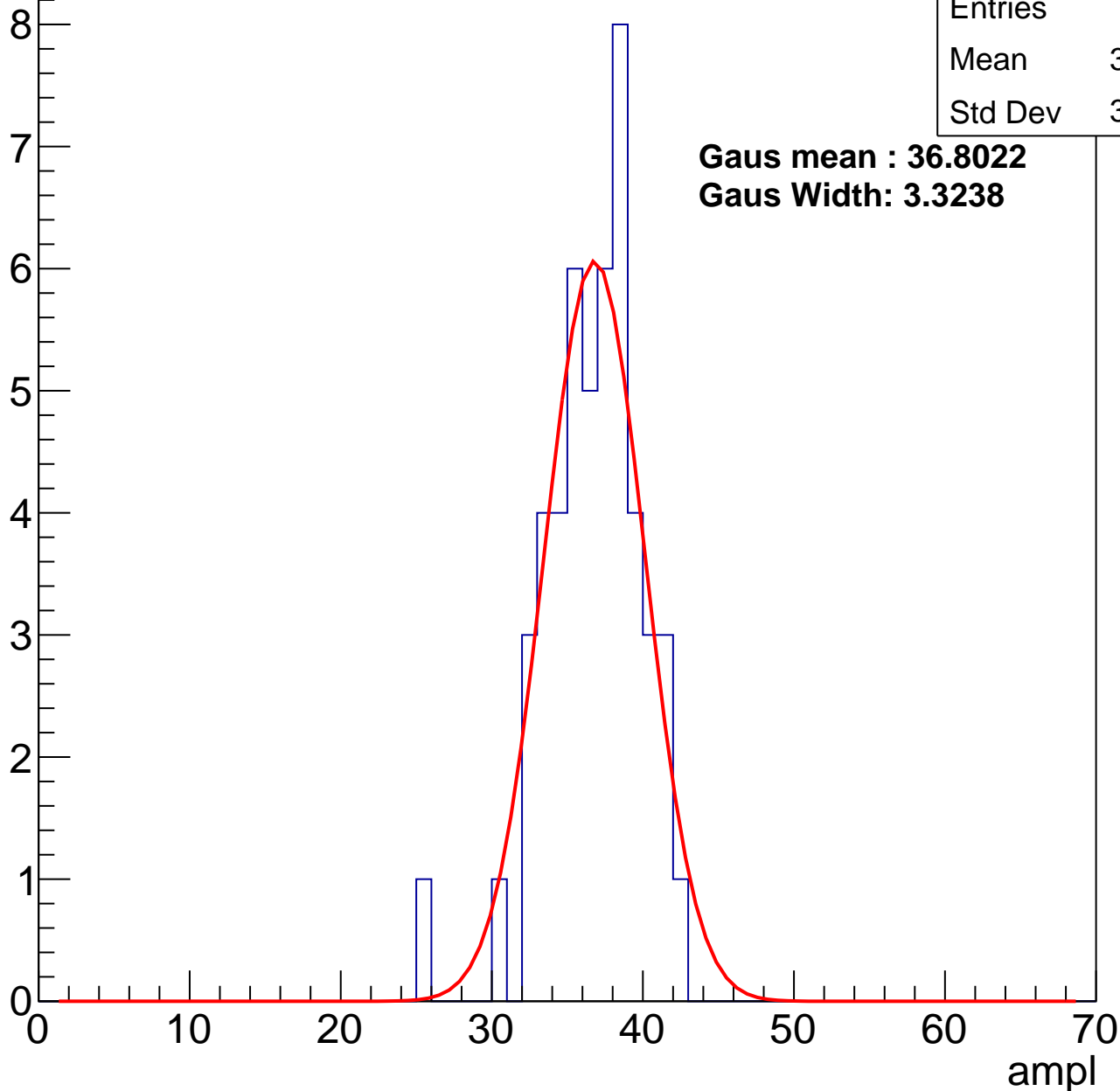
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	49
Mean	36.24
Std Dev	3.172

**Gaus mean : 36.8022**

**Gaus Width: 3.3238**



# B0L002S, U2-ch25, adc2

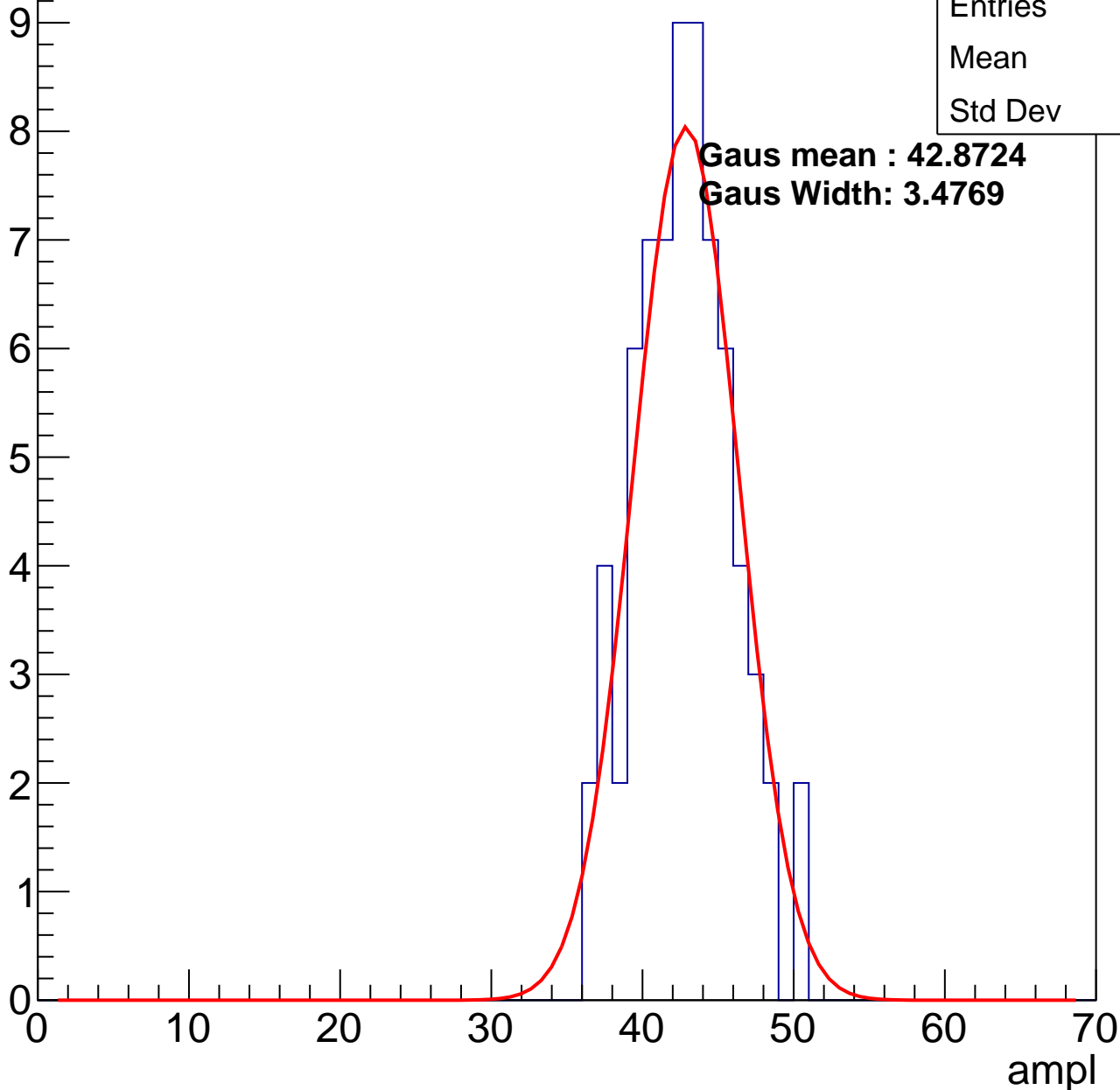
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	70
Mean	42.3
Std Dev	3.2

**Gaus mean : 42.8724**

**Gaus Width: 3.4769**

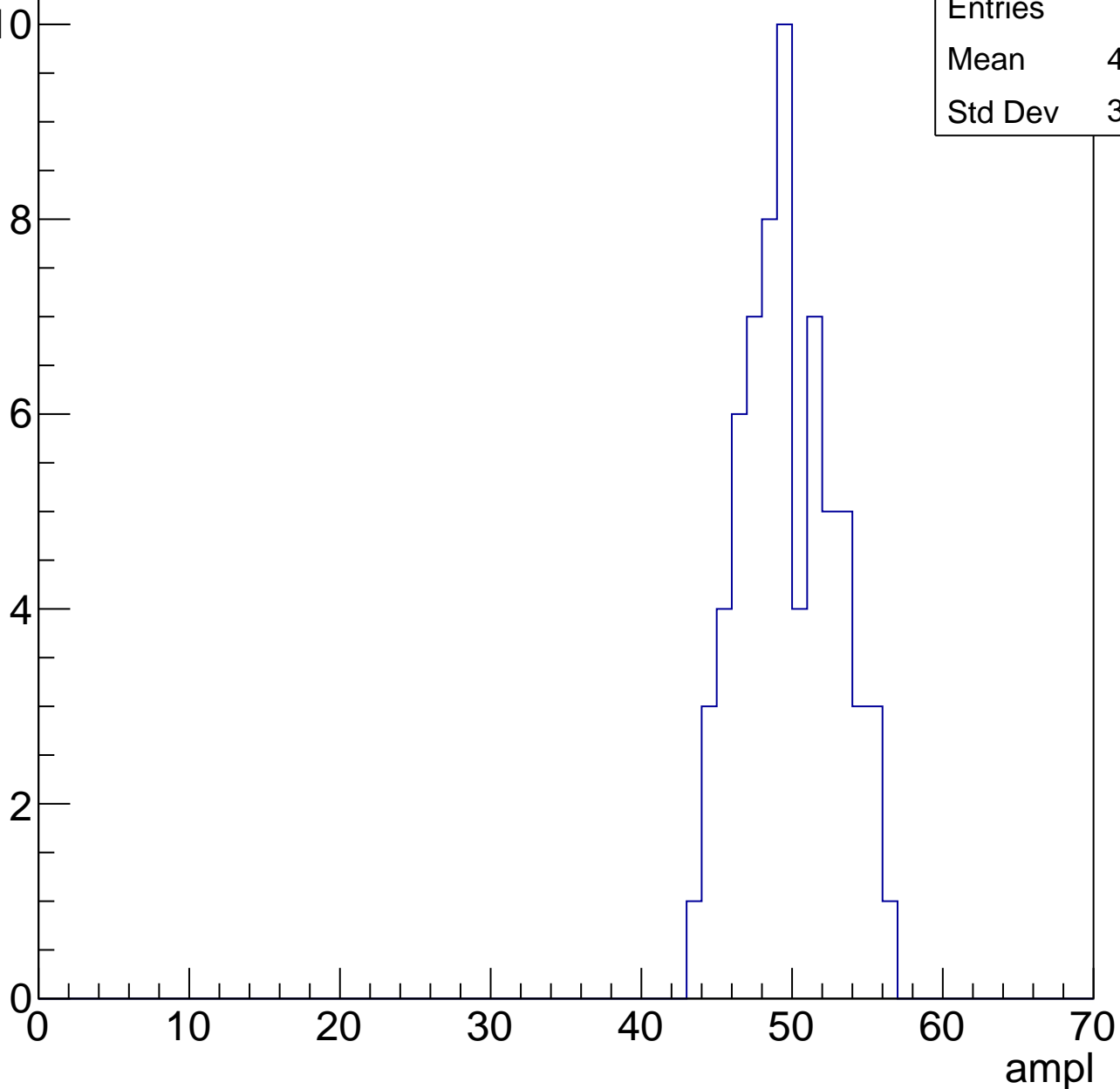


# B0L002S, U2-ch25, adc3

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	67
Mean	49.24
Std Dev	3.115

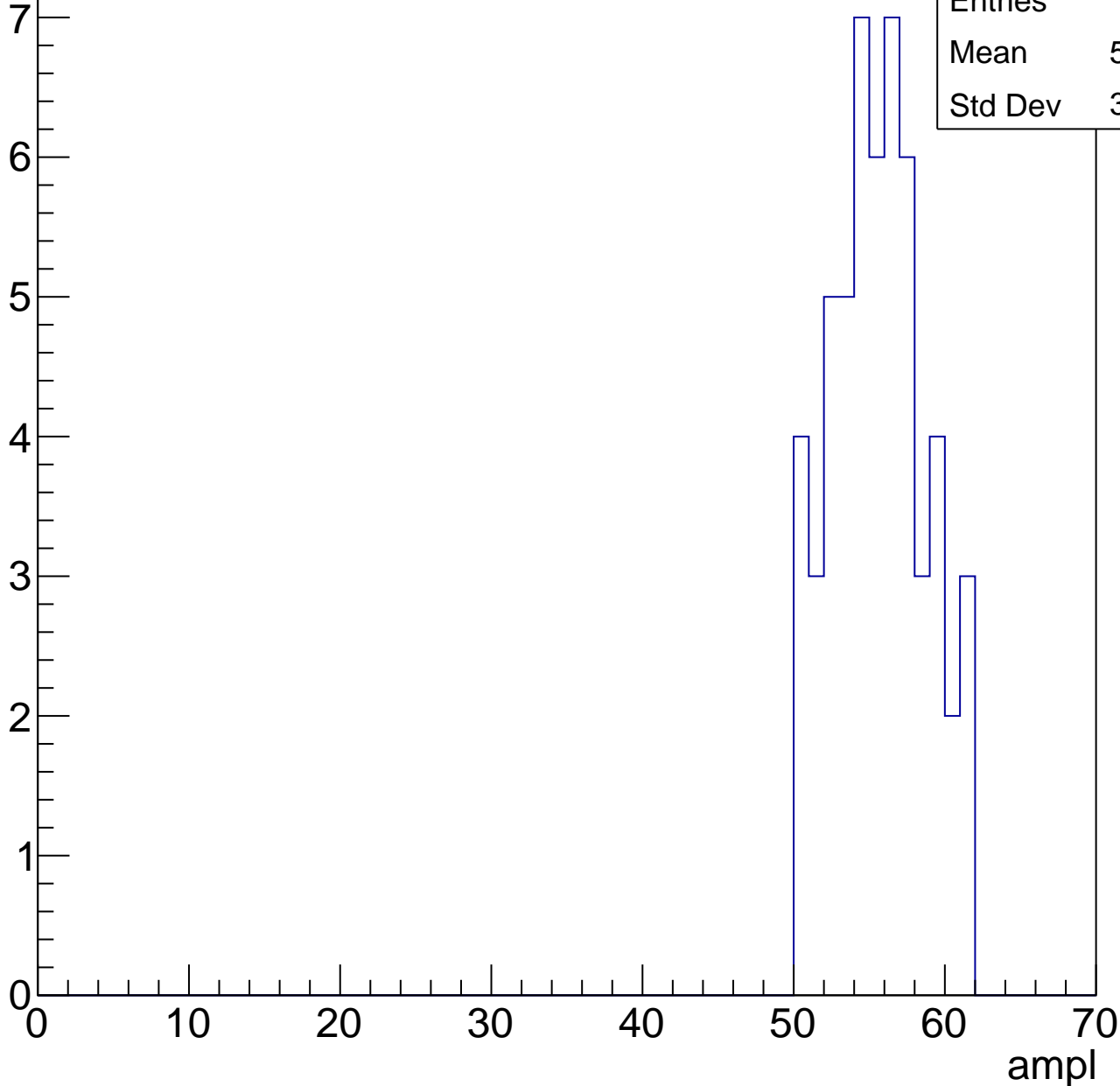


# B0L002S, U2-ch25, adc4

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	55
Mean	55.15
Std Dev	3.012



# B0L002S, U2-ch25, adc5

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

10

Entries 54

Mean 60.17

Std Dev 2.167

8

6

4

2

0

0

10

20

30

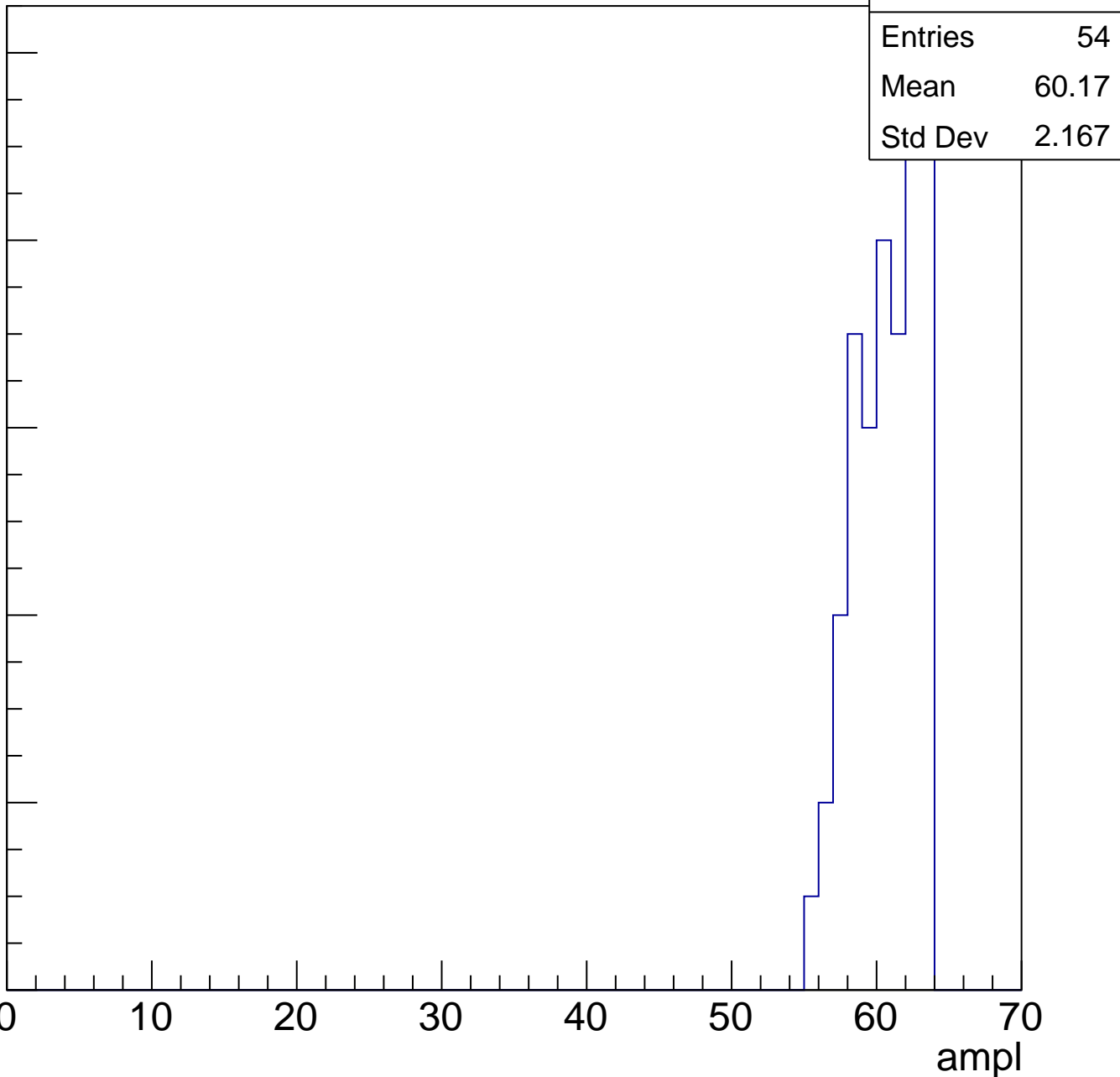
40

50

60

70

ampl



# B0L002S, U2-ch25, adc6

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry





# B0L002S, U2-ch25, adc7

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



# B0L002S, U2-ch26, adc0

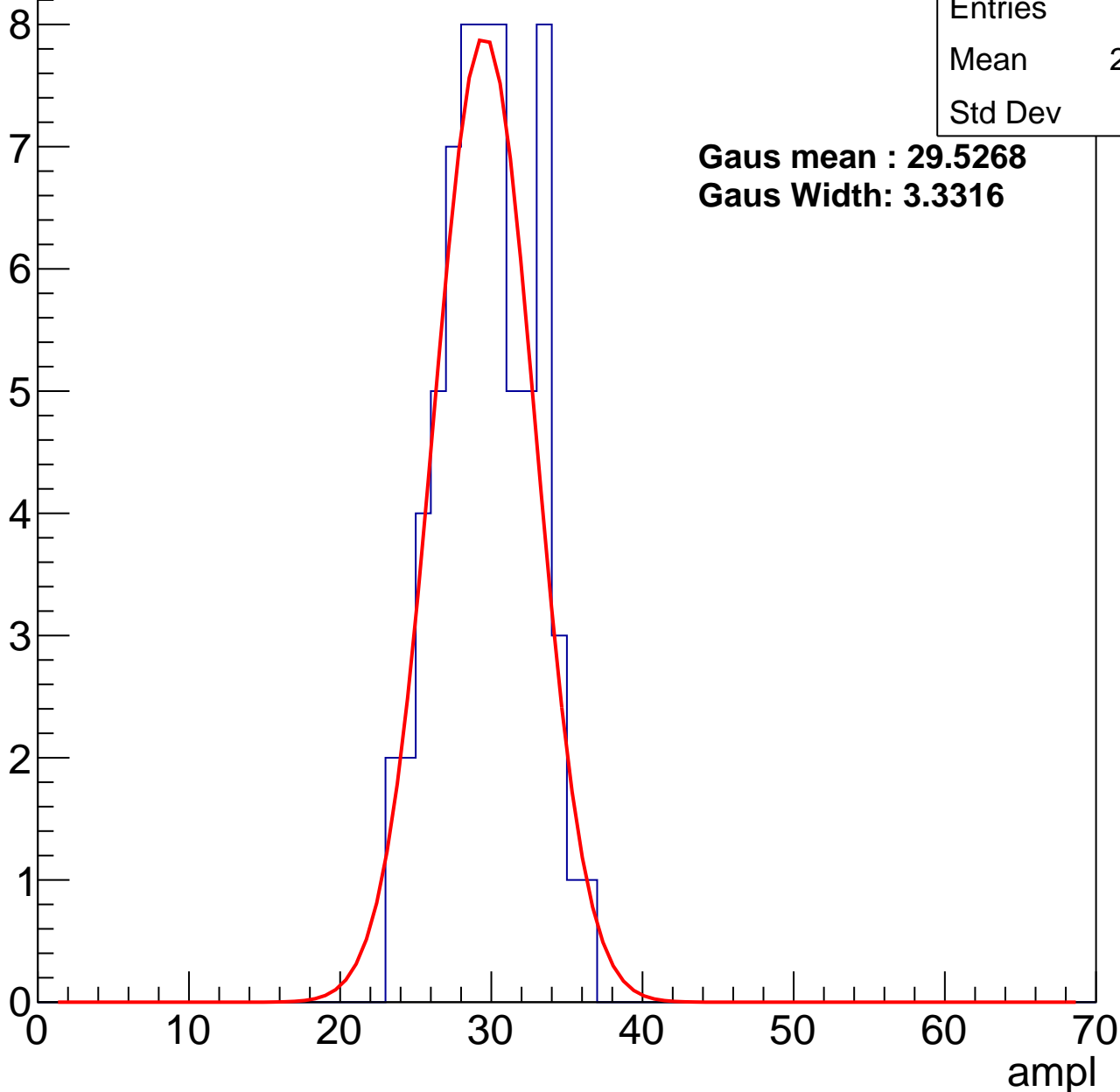
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	67
Mean	29.27
Std Dev	3.05

**Gaus mean : 29.5268**

**Gaus Width: 3.3316**



# B0L002S, U2-ch26, adc1

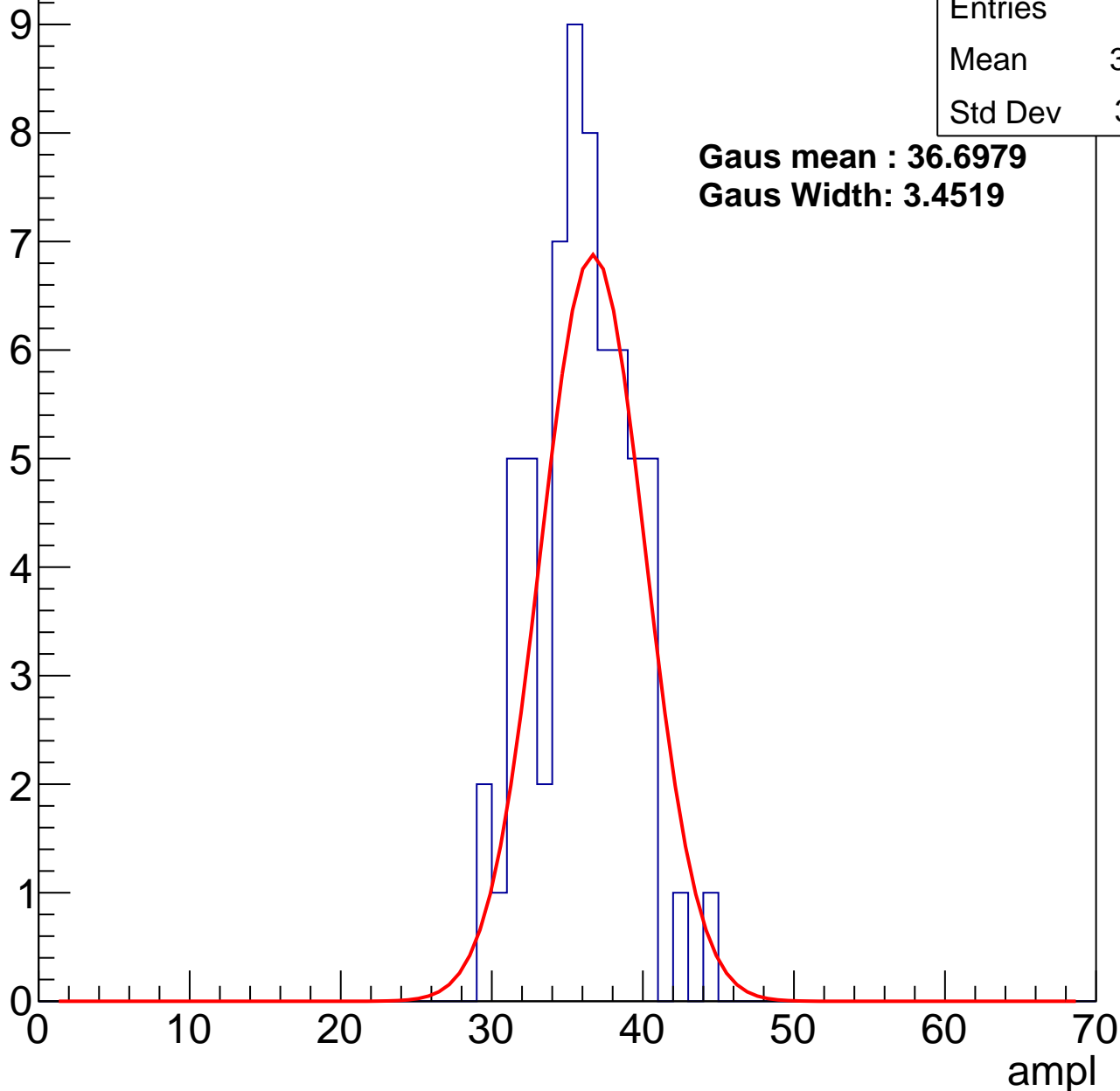
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	63
Mean	35.57
Std Dev	3.181

**Gaus mean : 36.6979**

**Gaus Width: 3.4519**



# B0L002S, U2-ch26, adc2

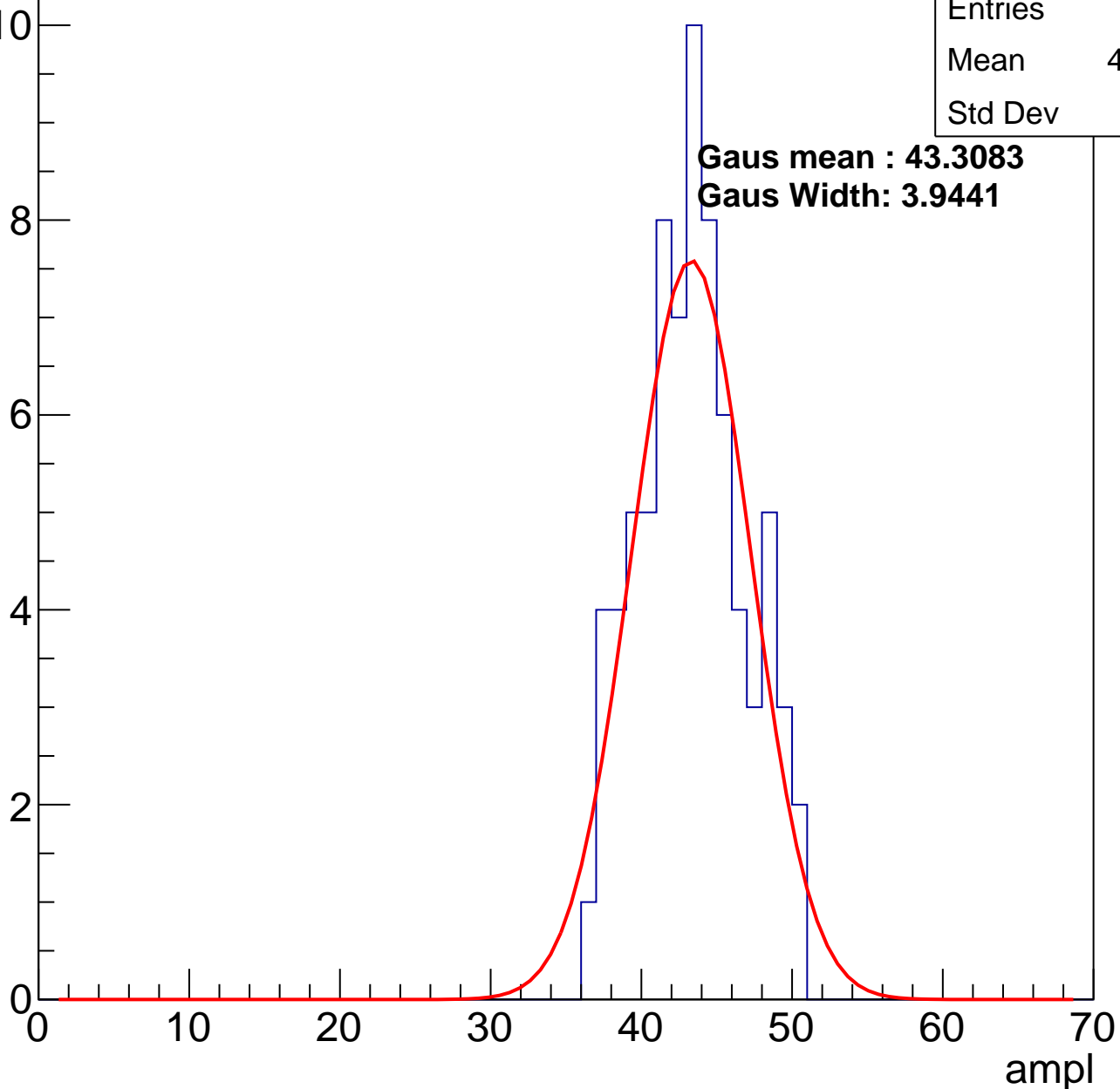
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	75
Mean	42.89
Std Dev	3.47

**Gaus mean : 43.3083**

**Gaus Width: 3.9441**

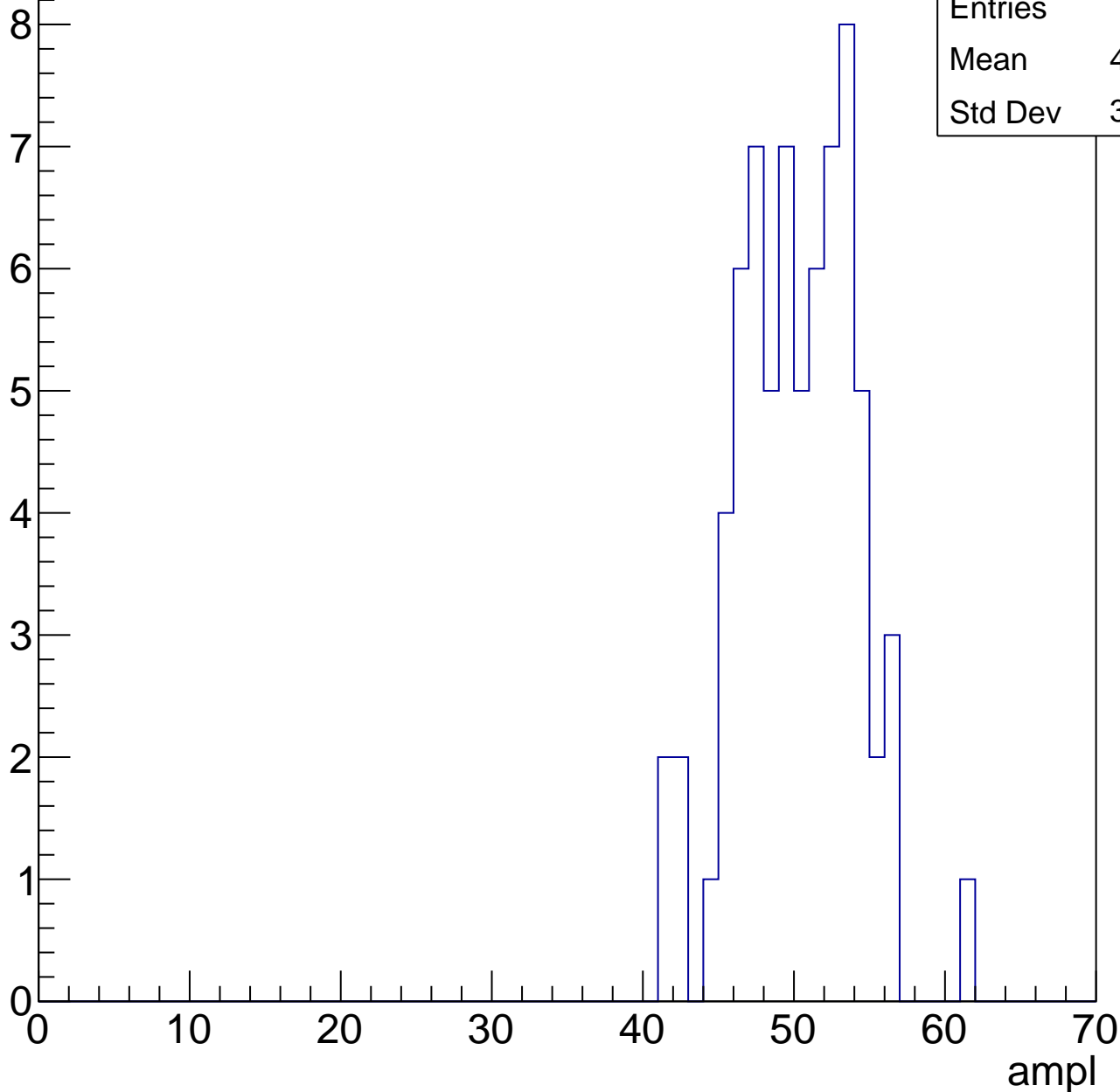


# B0L002S, U2-ch26, adc3

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	71
Mean	49.73
Std Dev	3.886

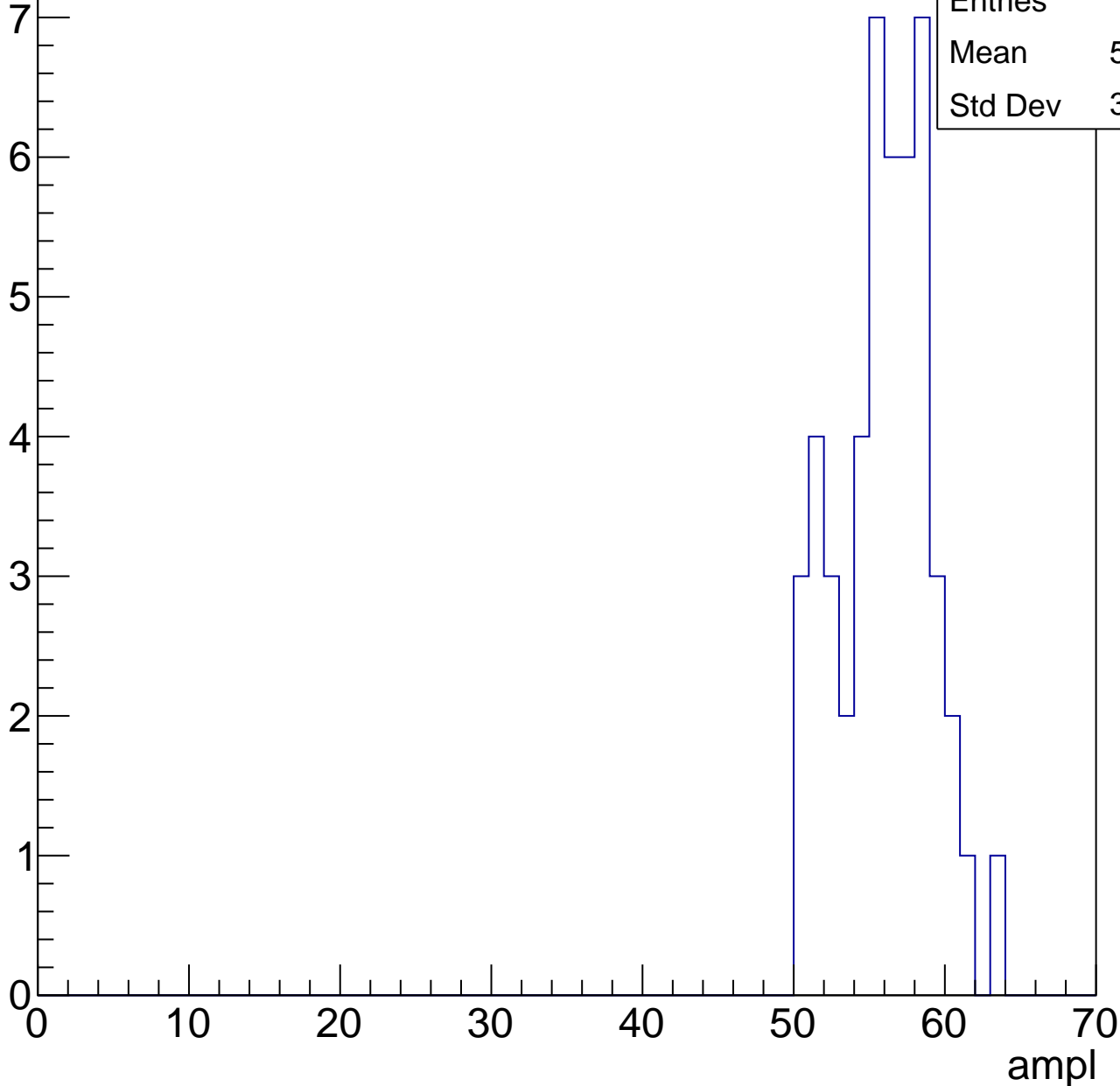


# B0L002S, U2-ch26, adc4

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	49
Mean	55.55
Std Dev	3.044



# B0L002S, U2-ch26, adc5

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	43
Mean	59.86
Std Dev	2.195

ampl

0 10 20 30 40 50 60 70

0

1

2

3

4

5

6

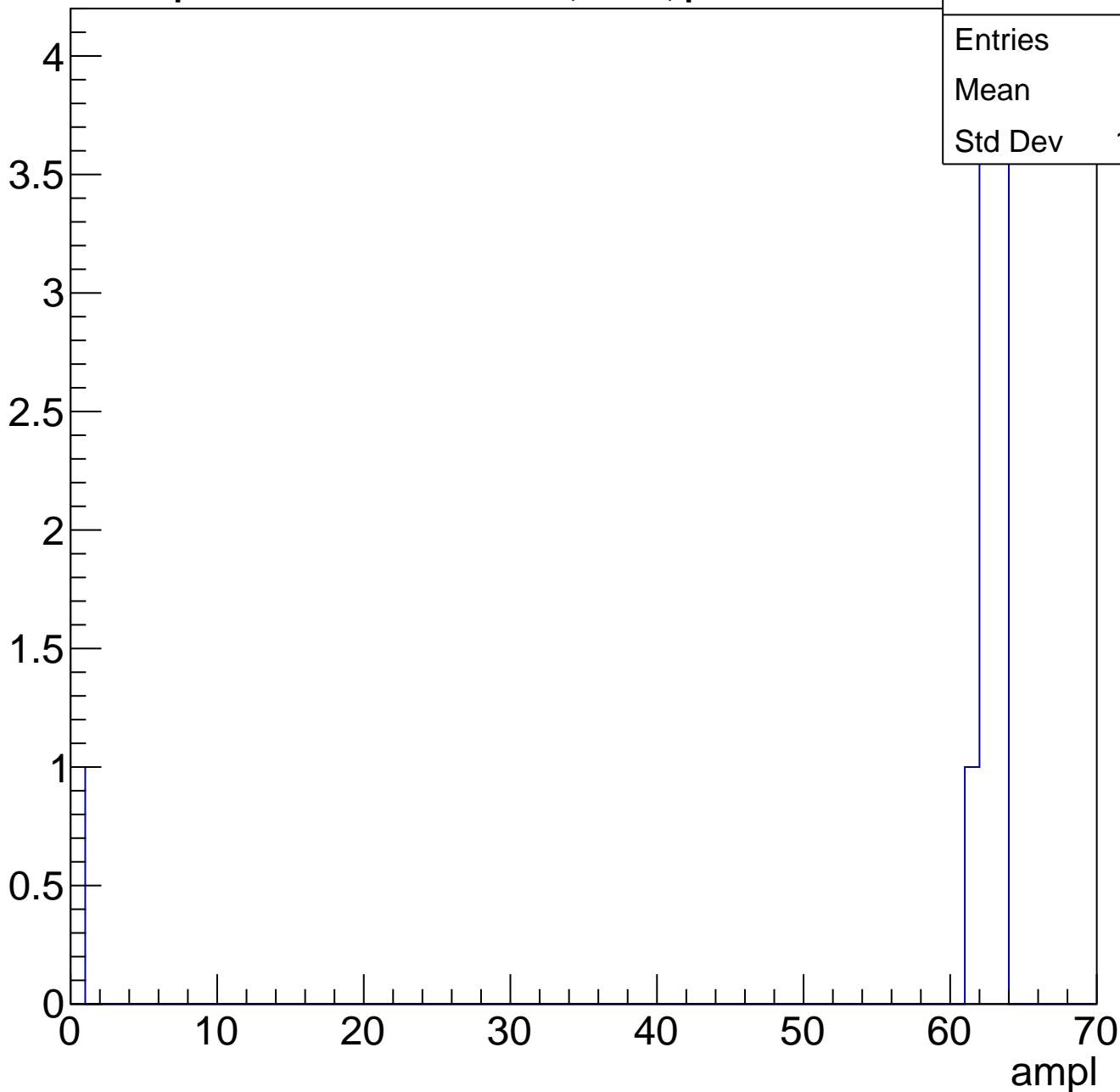
7

8

# B0L002S, U2-ch26, adc6

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry





# B0L002S, U2-ch26, adc7

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



# B0L002S, U2-ch27, adc0

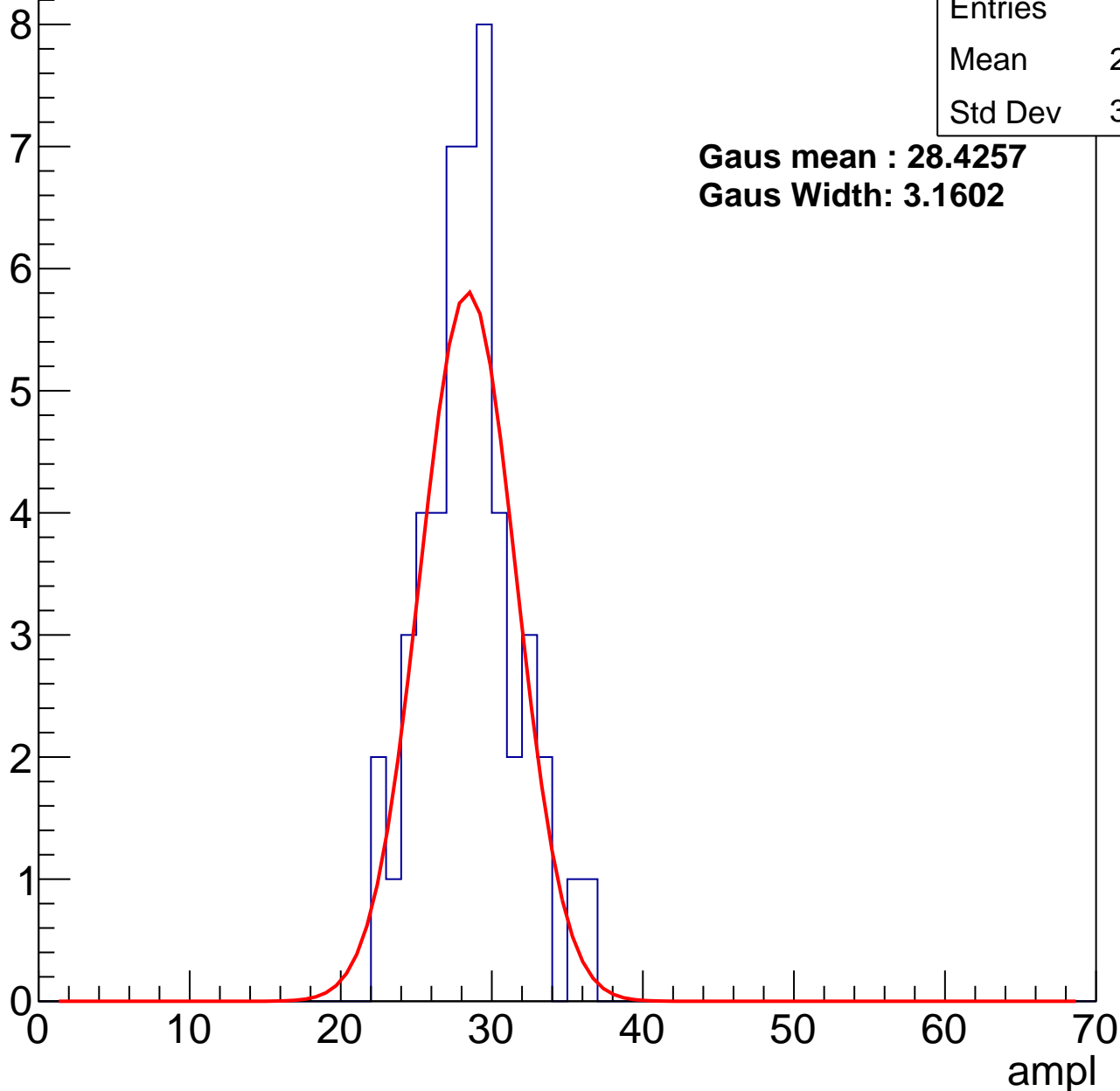
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	49
Mean	28.06
Std Dev	3.053

**Gaus mean : 28.4257**

**Gaus Width: 3.1602**



# B0L002S, U2-ch27, adc1

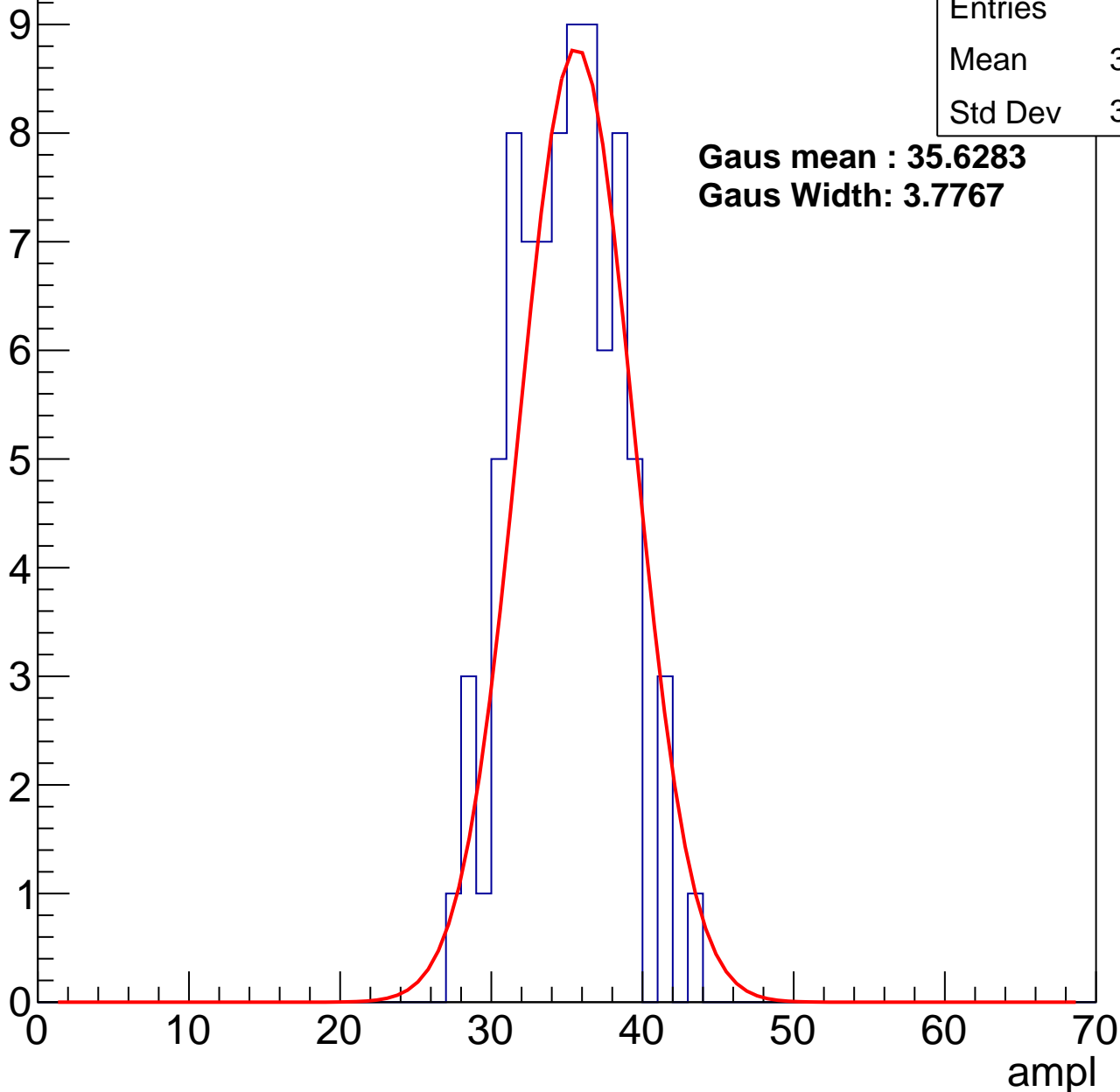
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	81
Mean	34.46
Std Dev	3.392

**Gaus mean : 35.6283**

**Gaus Width: 3.7767**



# B0L002S, U2-ch27, adc2

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entries	74
Mean	42.24
Std Dev	3.4

**Gaus mean : 42.6292**

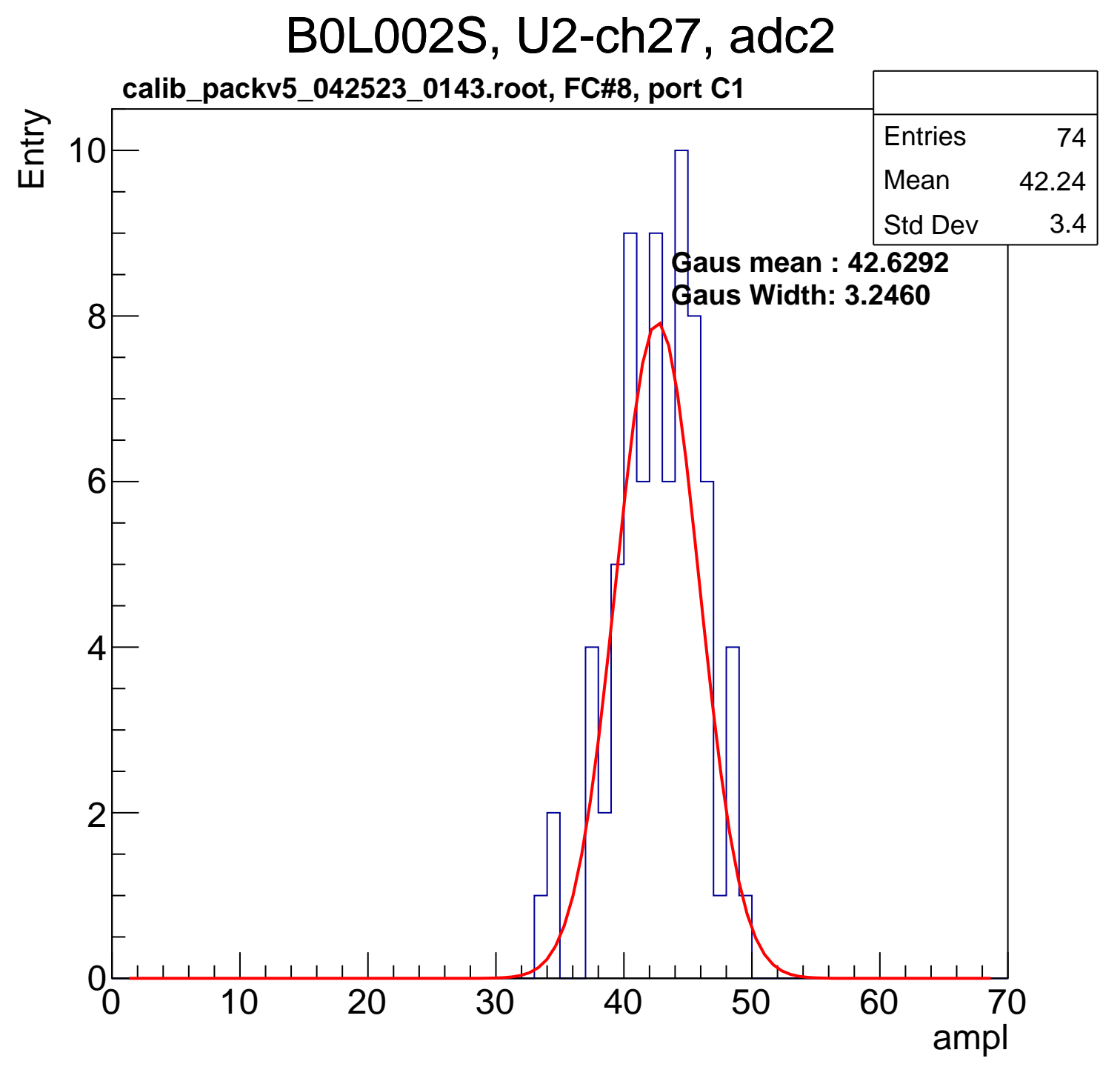
**Gaus Width: 3.2460**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

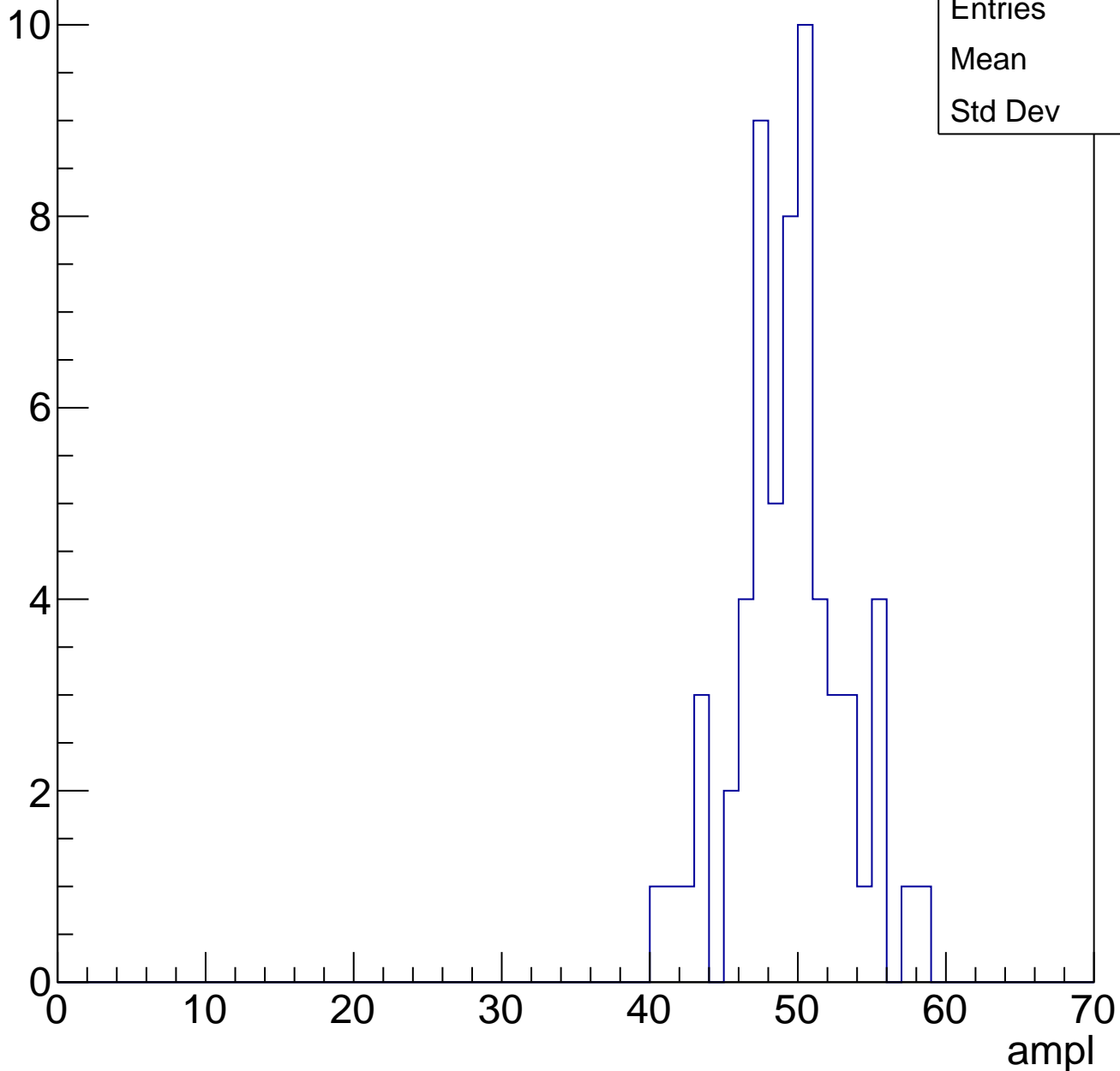


# B0L002S, U2-ch27, adc3

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entries	61
Mean	49
Std Dev	3.68

Entry

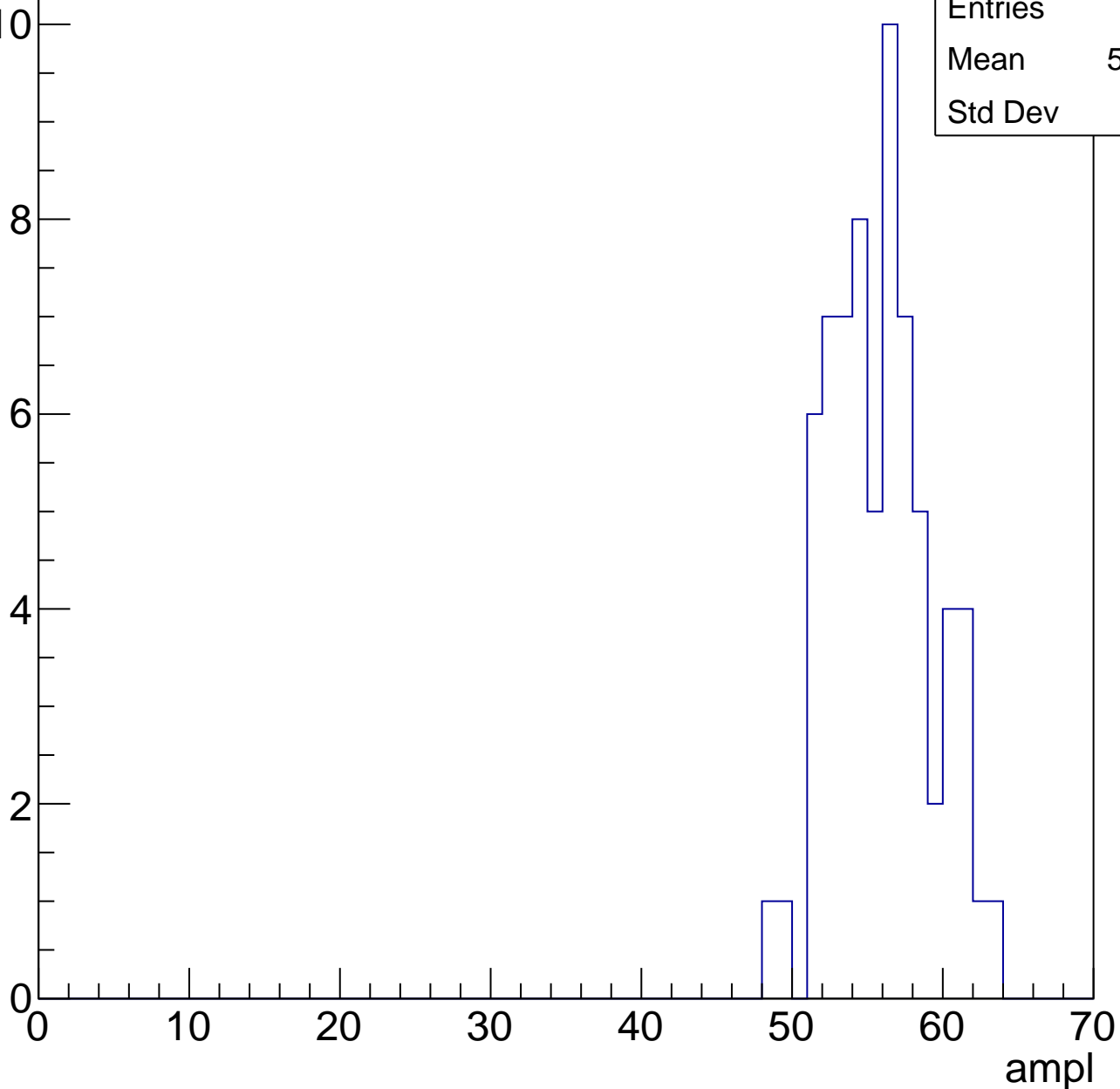


# B0L002S, U2-ch27, adc4

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	69
Mean	55.38
Std Dev	3.28



# B0L002S, U2-ch27, adc5

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	39
Mean	60.05
Std Dev	2.183

ampl

0 10 20 30 40 50 60 70

0

1

2

3

4

5

6

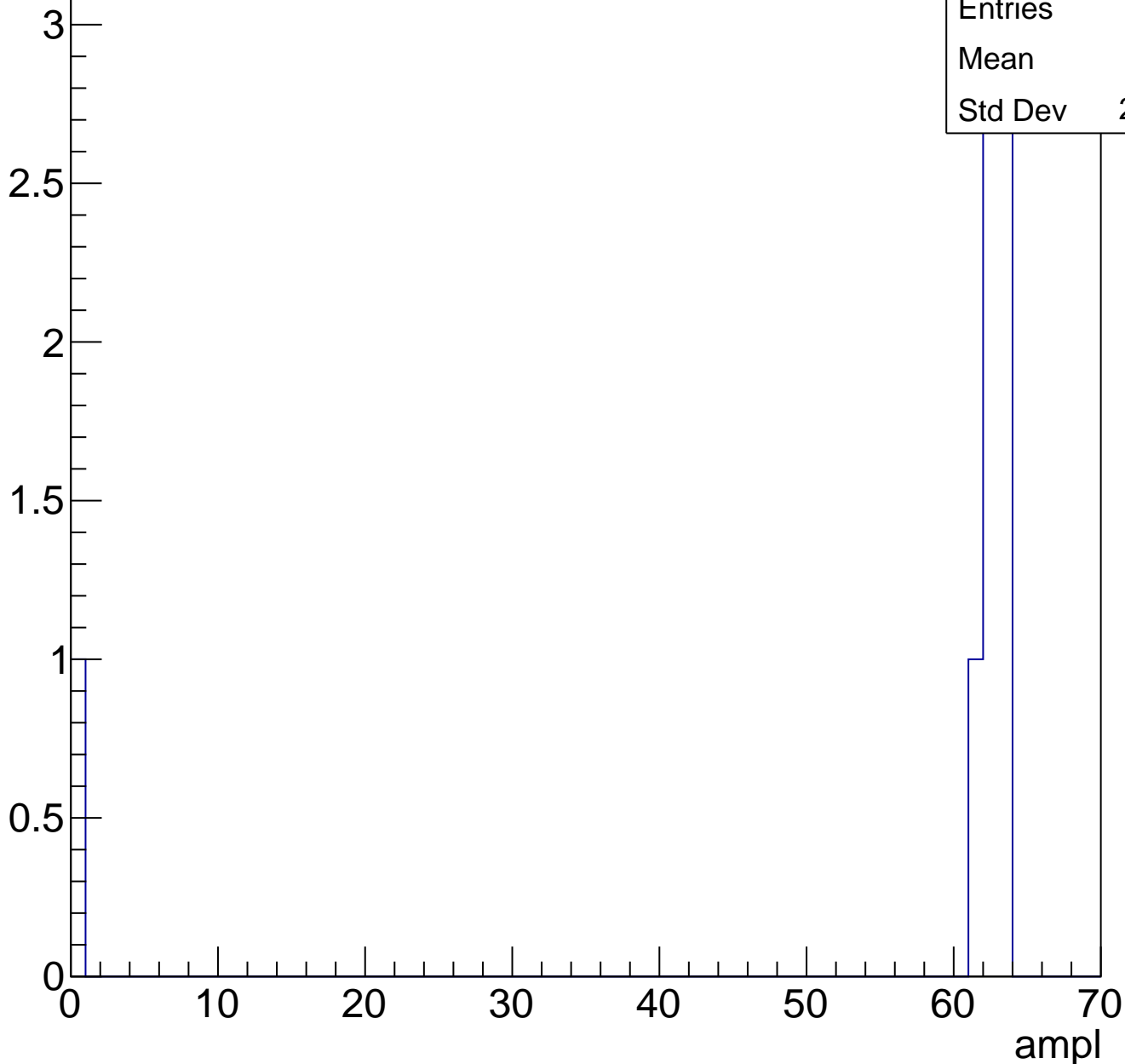
7

8

# B0L002S, U2-ch27, adc6

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry





# B0L002S, U2-ch27, adc7

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L002S, U2-ch28, adc0

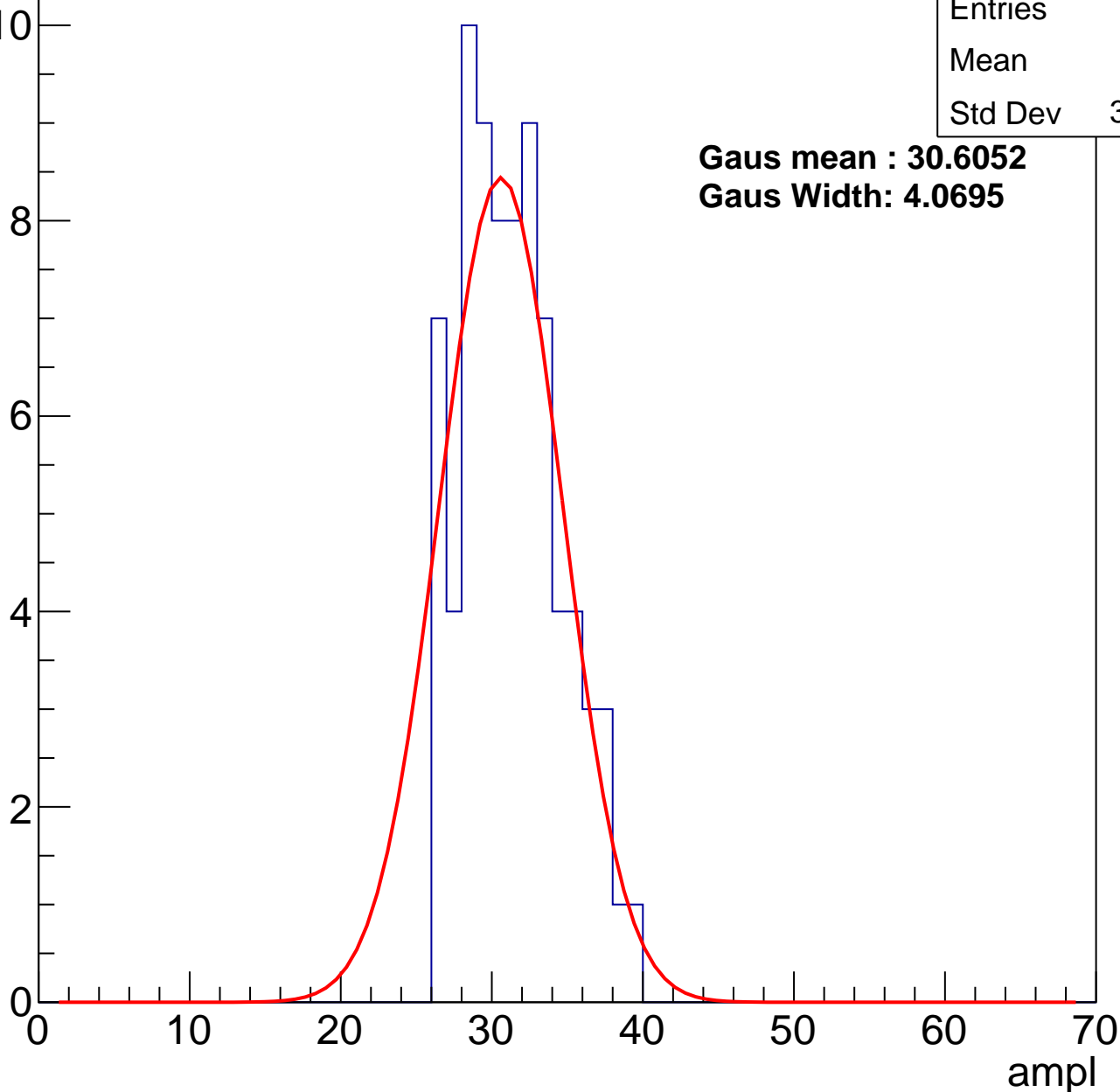
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	78
Mean	30.9
Std Dev	3.213

**Gaus mean : 30.6052**

**Gaus Width: 4.0695**



# B0L002S, U2-ch28, adc1

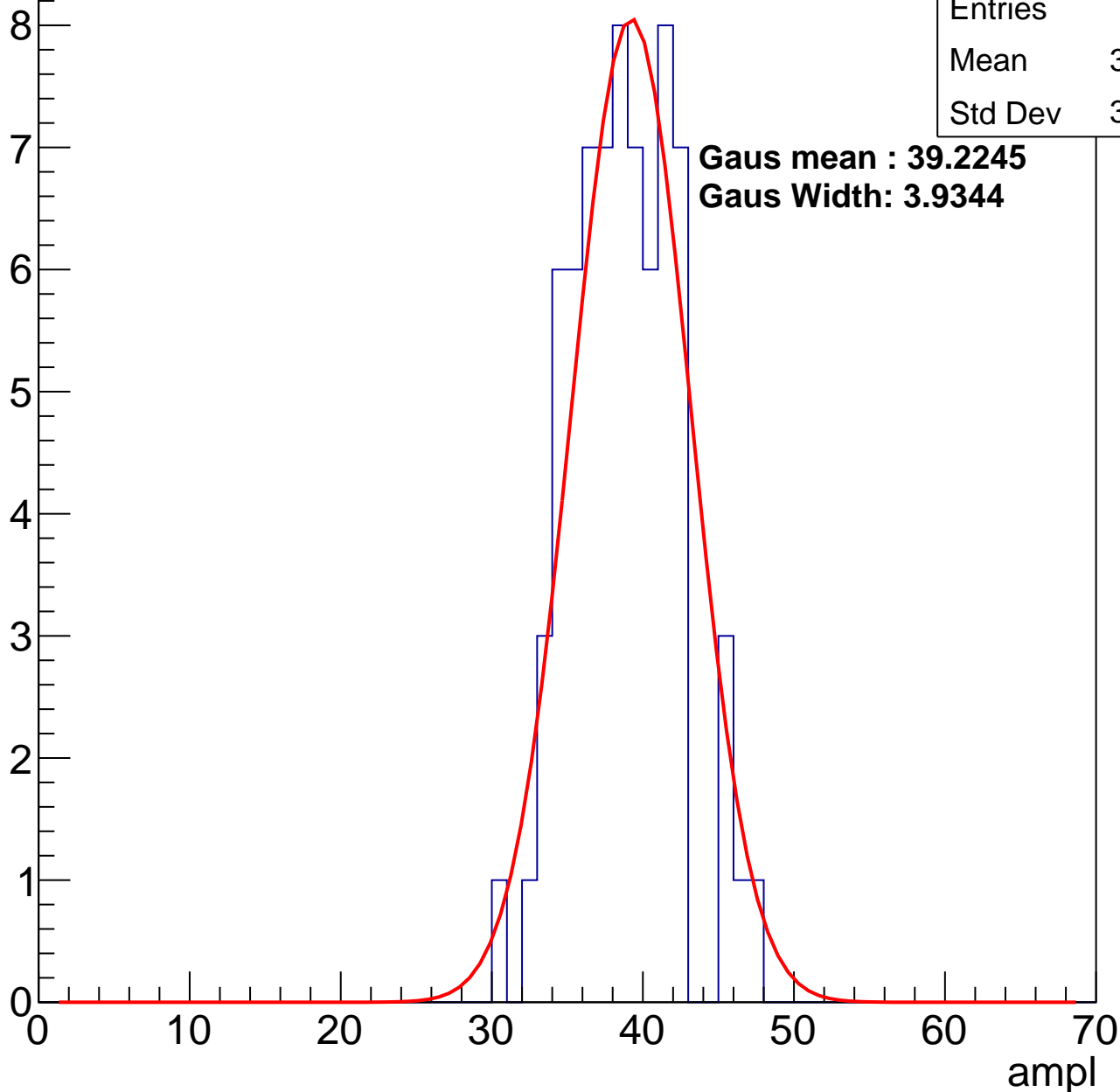
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	72
Mean	38.24
Std Dev	3.462

**Gaus mean : 39.2245**

**Gaus Width: 3.9344**



# B0L002S, U2-ch28, adc2

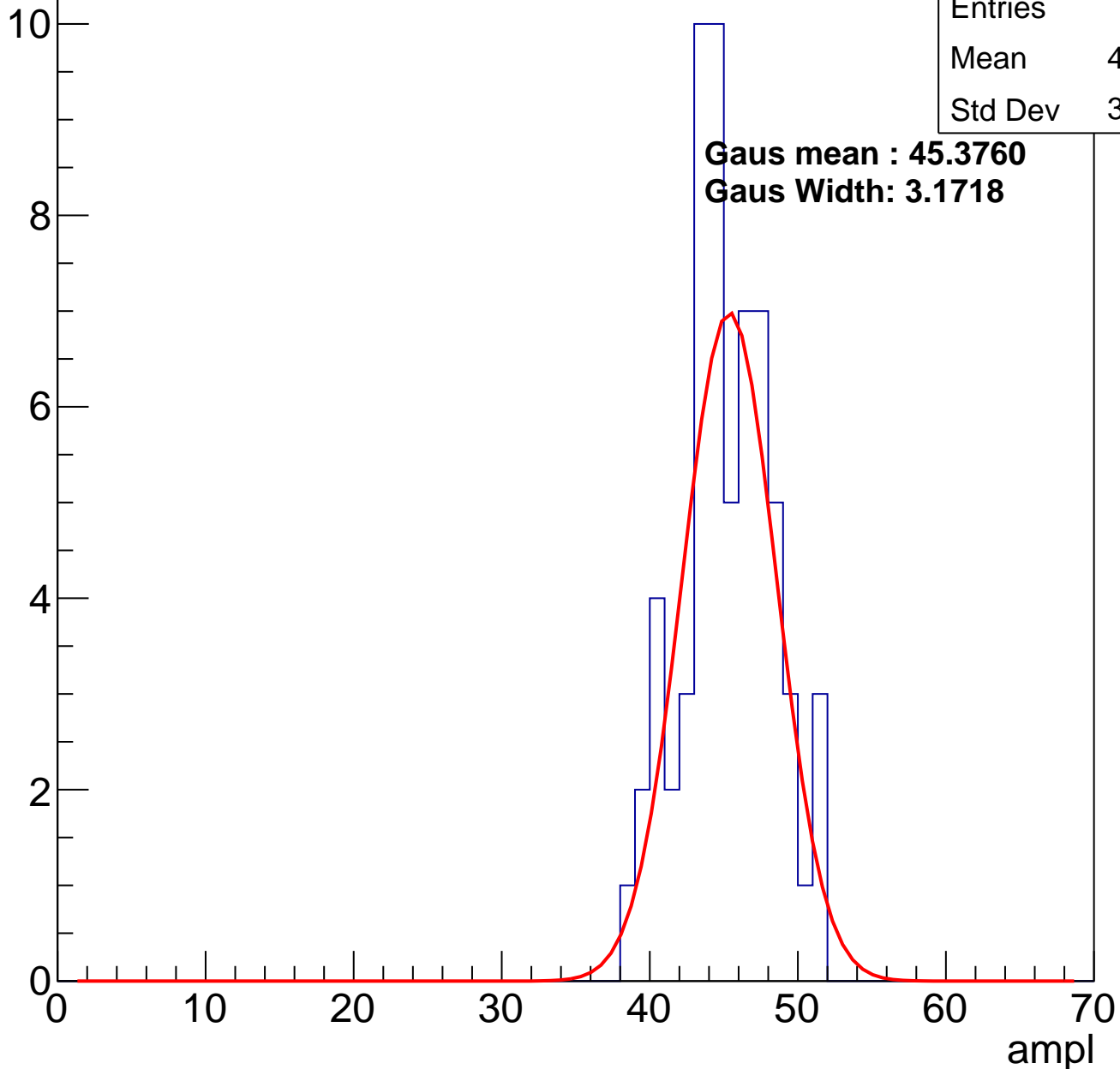
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entries	63
Mean	44.76
Std Dev	3.054

**Gaus mean : 45.3760**

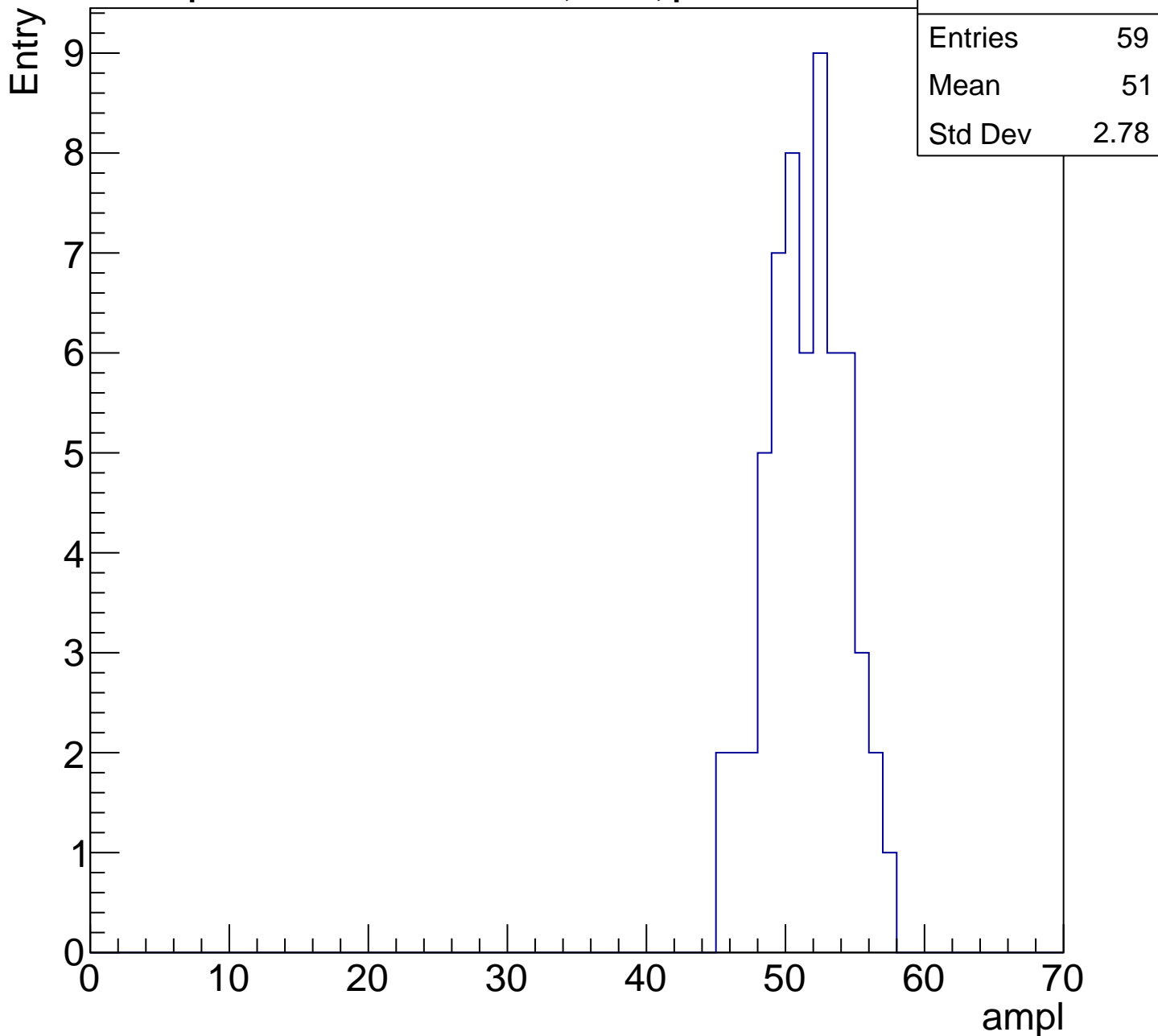
**Gaus Width: 3.1718**

Entry



# B0L002S, U2-ch28, adc3

calib\_packv5\_042523\_0143.root, FC#8, port C1

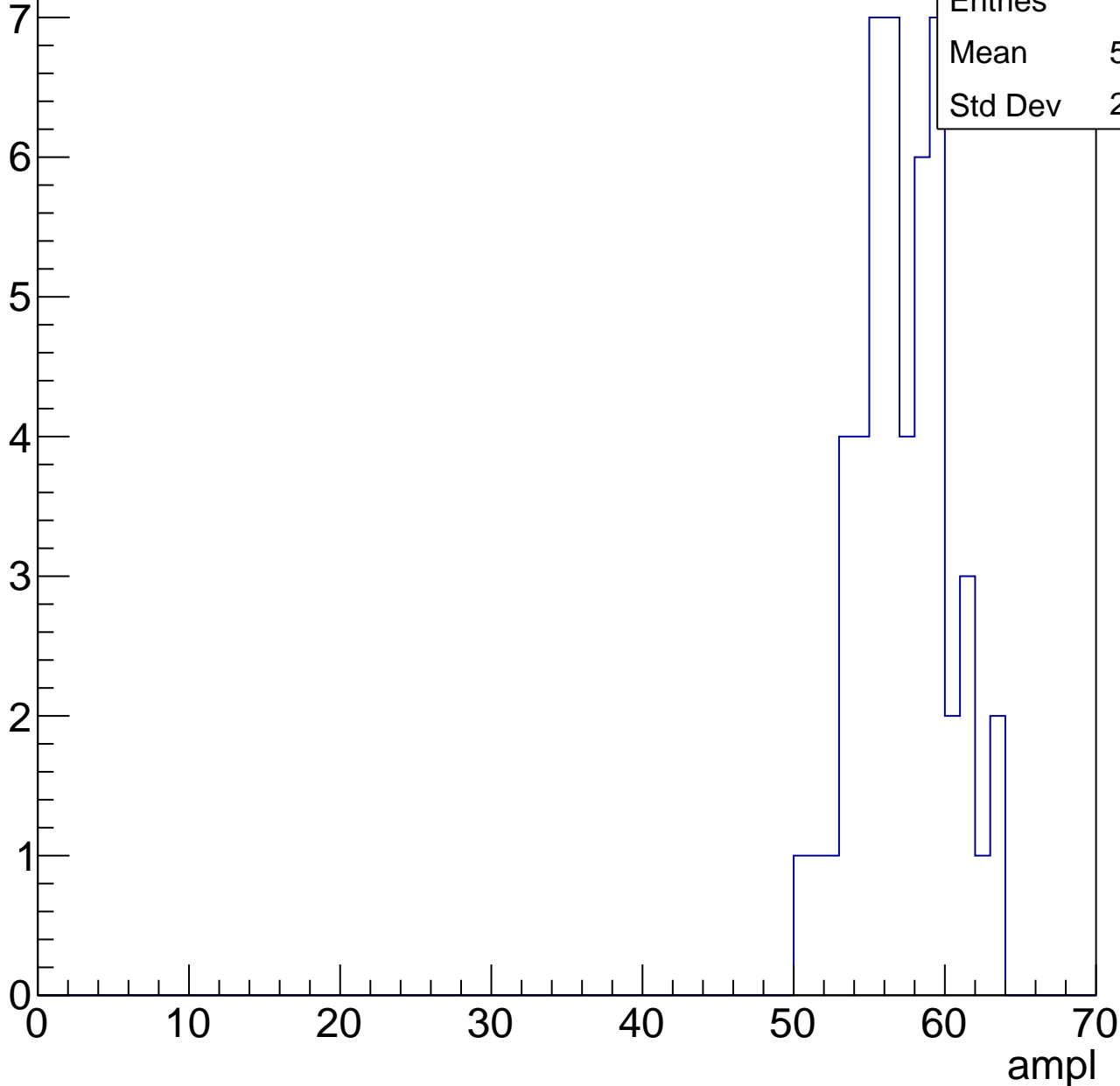


# B0L002S, U2-ch28, adc4

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

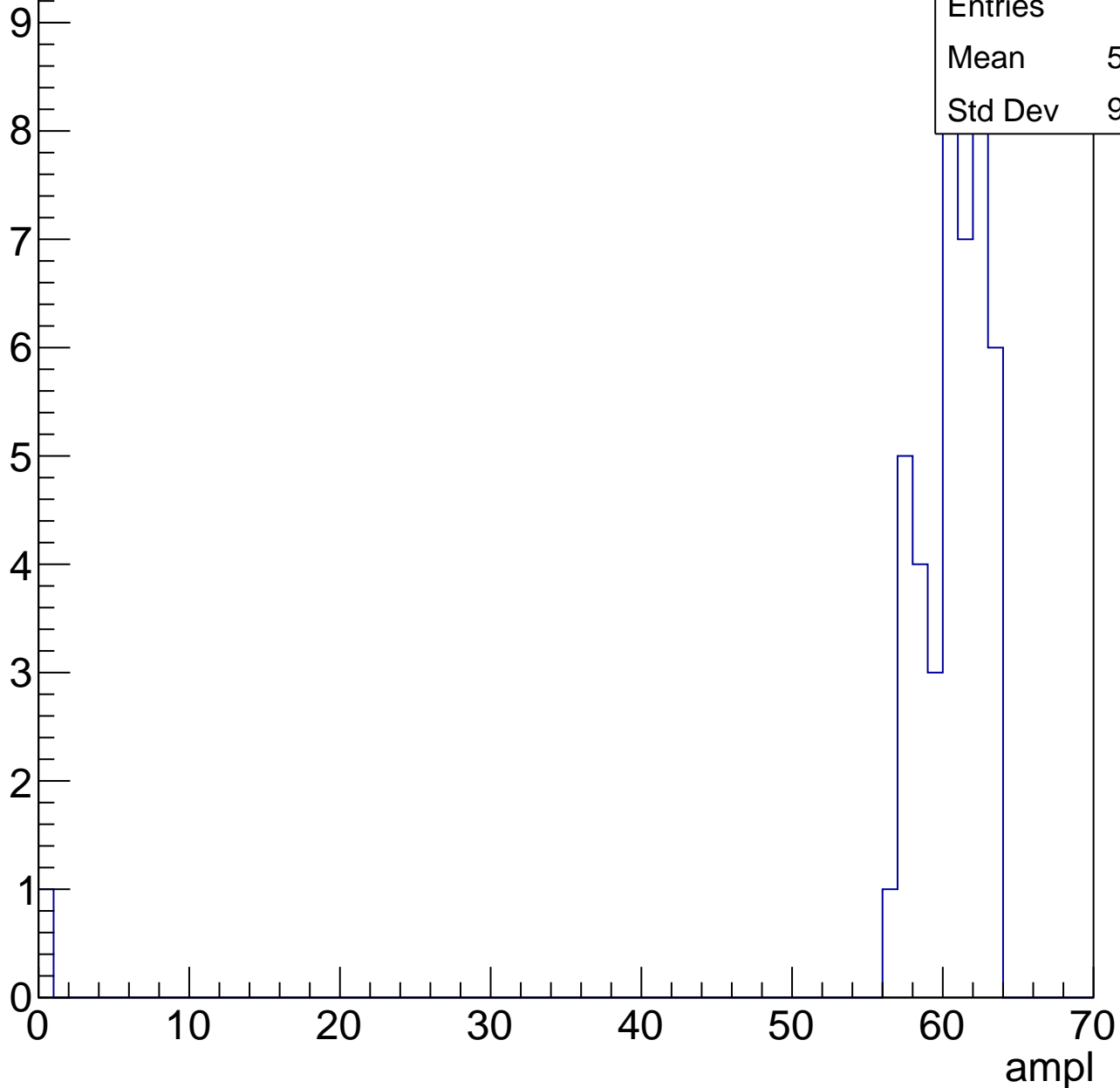
Entries	50
Mean	56.76
Std Dev	2.964



# B0L002S, U2-ch28, adc5

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



# B0L002S, U2-ch28, adc6

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	2
Mean	63
Std Dev	0

ampl



# B0L002S, U2-ch28, adc7

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



Entries	1
Mean	24
Std Dev	0

# B0L002S, U2-ch29, adc0

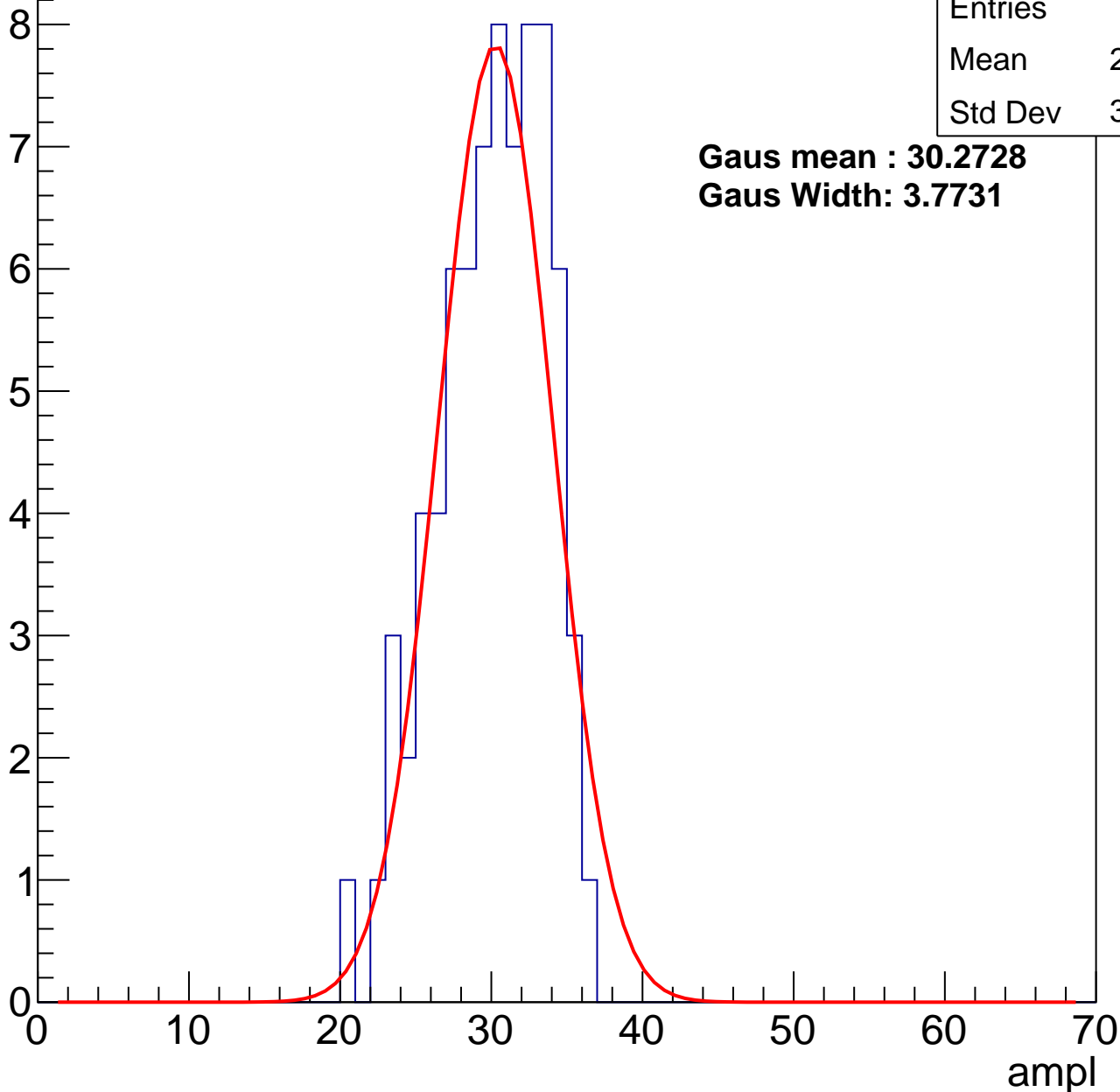
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	75
Mean	29.57
Std Dev	3.533

**Gaus mean : 30.2728**

**Gaus Width: 3.7731**



# B0L002S, U2-ch29, adc1

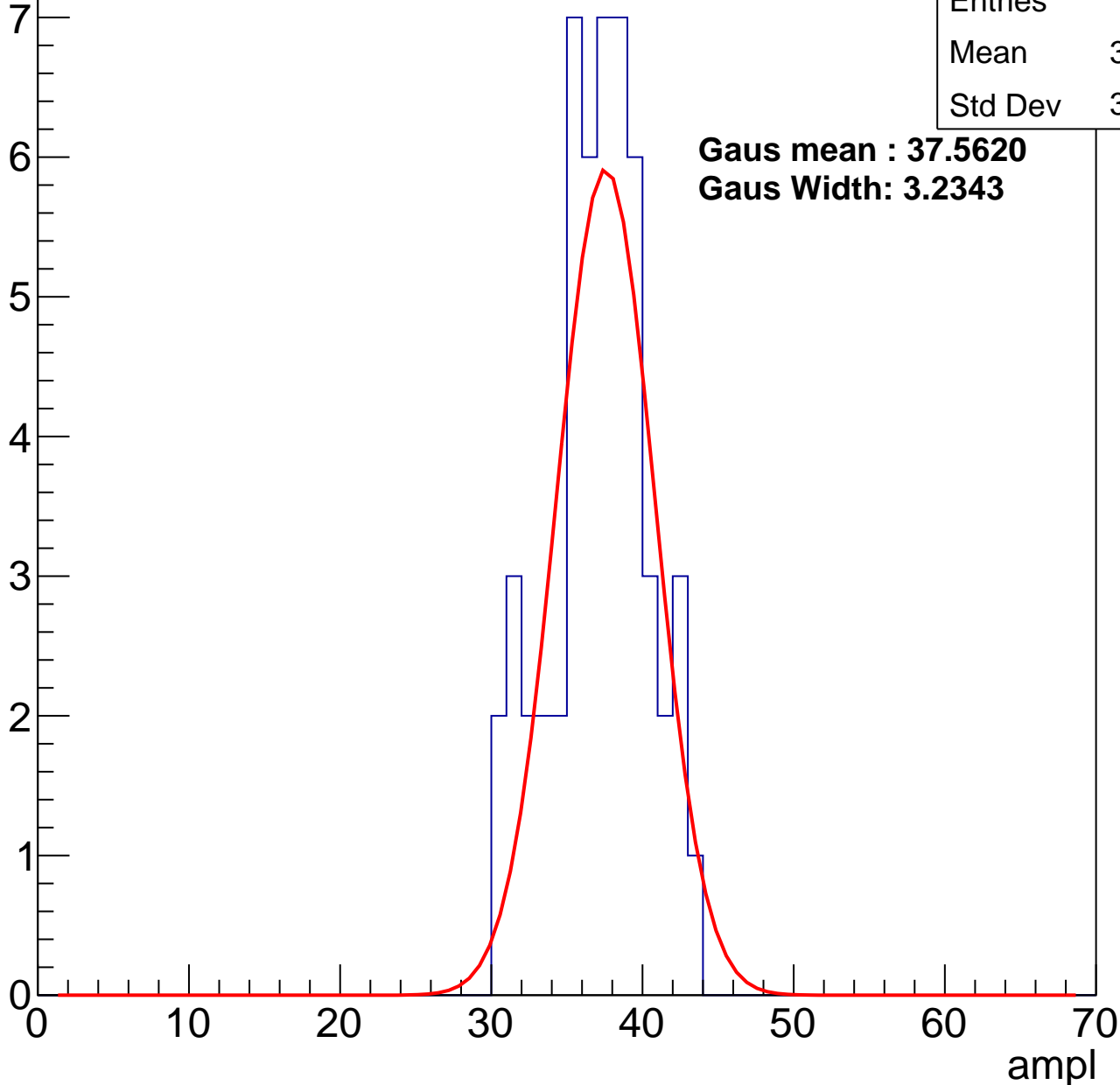
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	53
Mean	36.64
Std Dev	3.175

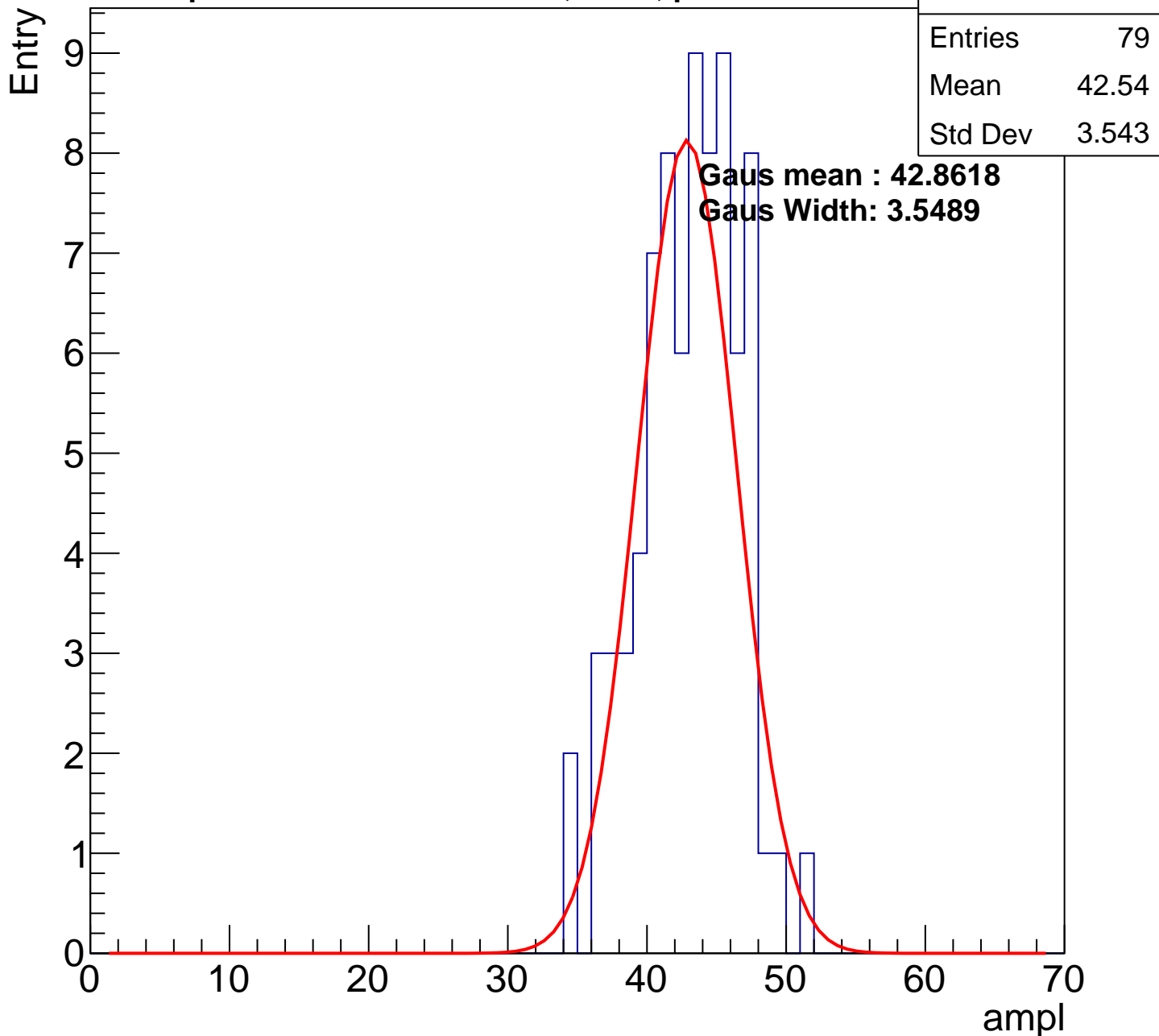
**Gaus mean : 37.5620**

**Gaus Width: 3.2343**



# B0L002S, U2-ch29, adc2

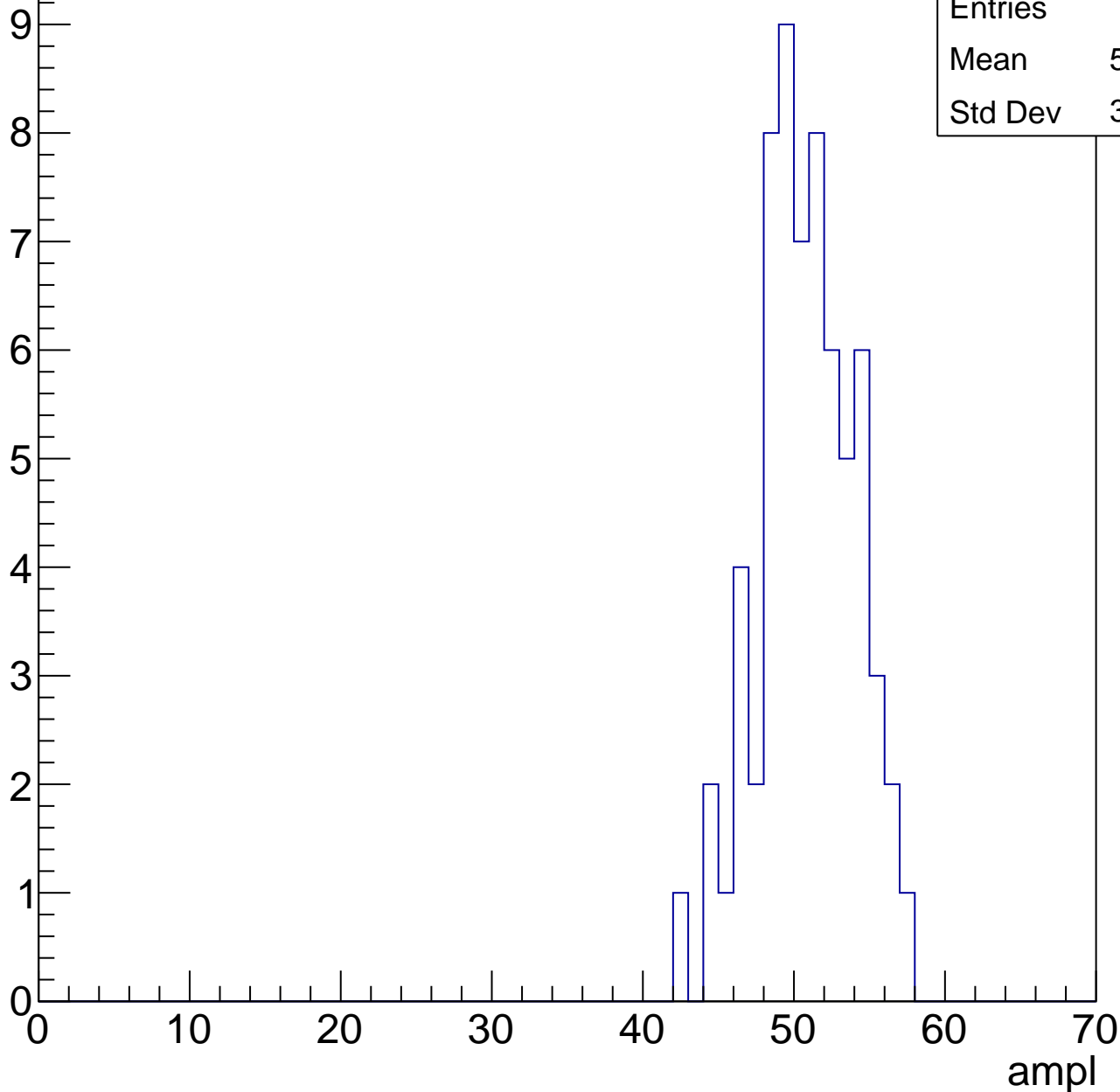
calib\_packv5\_042523\_0143.root, FC#8, port C1



# B0L002S, U2-ch29, adc3

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



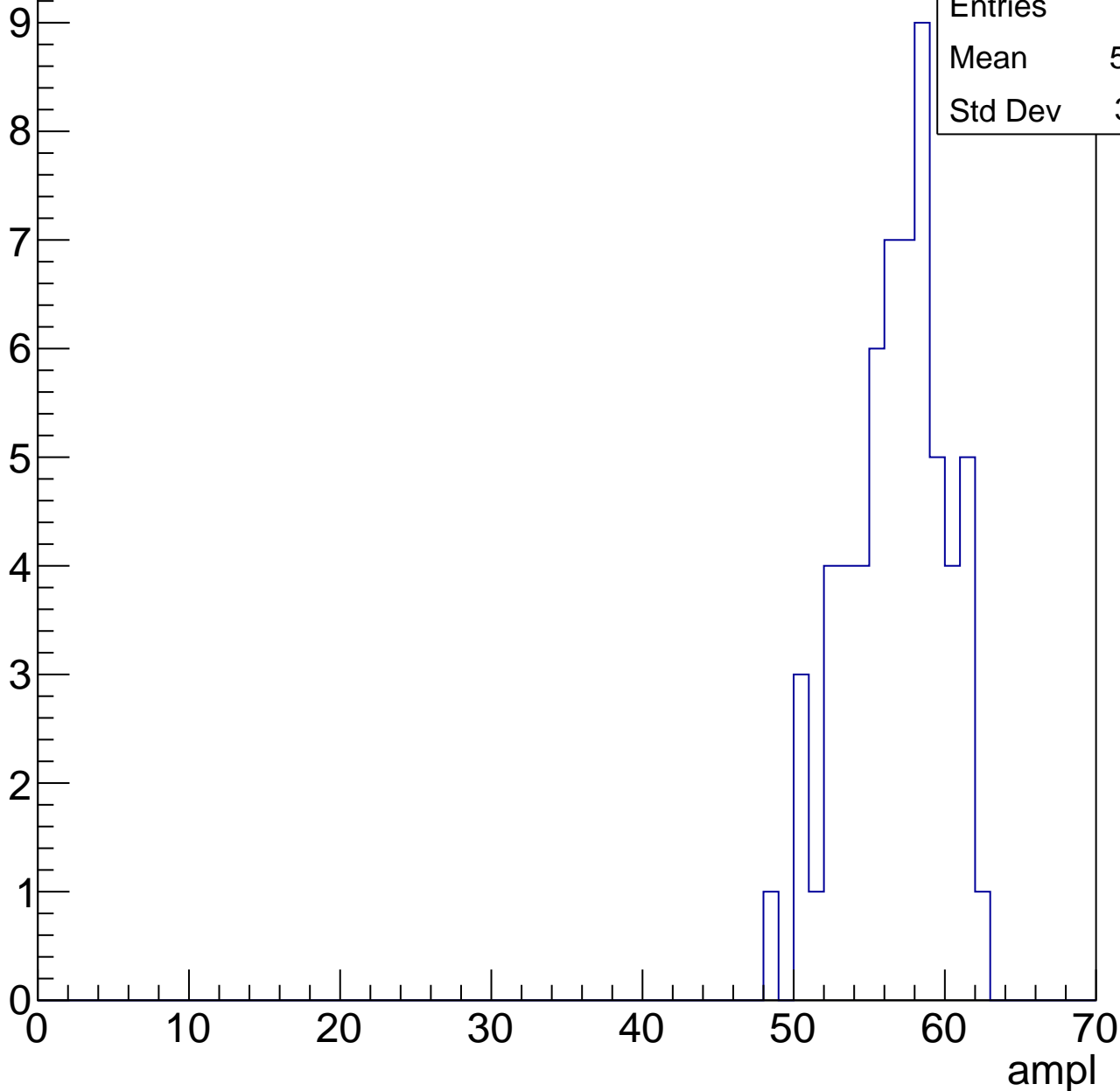
Entries	65
Mean	50.32
Std Dev	3.153

# B0L002S, U2-ch29, adc4

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	61
Mean	56.23
Std Dev	3.211

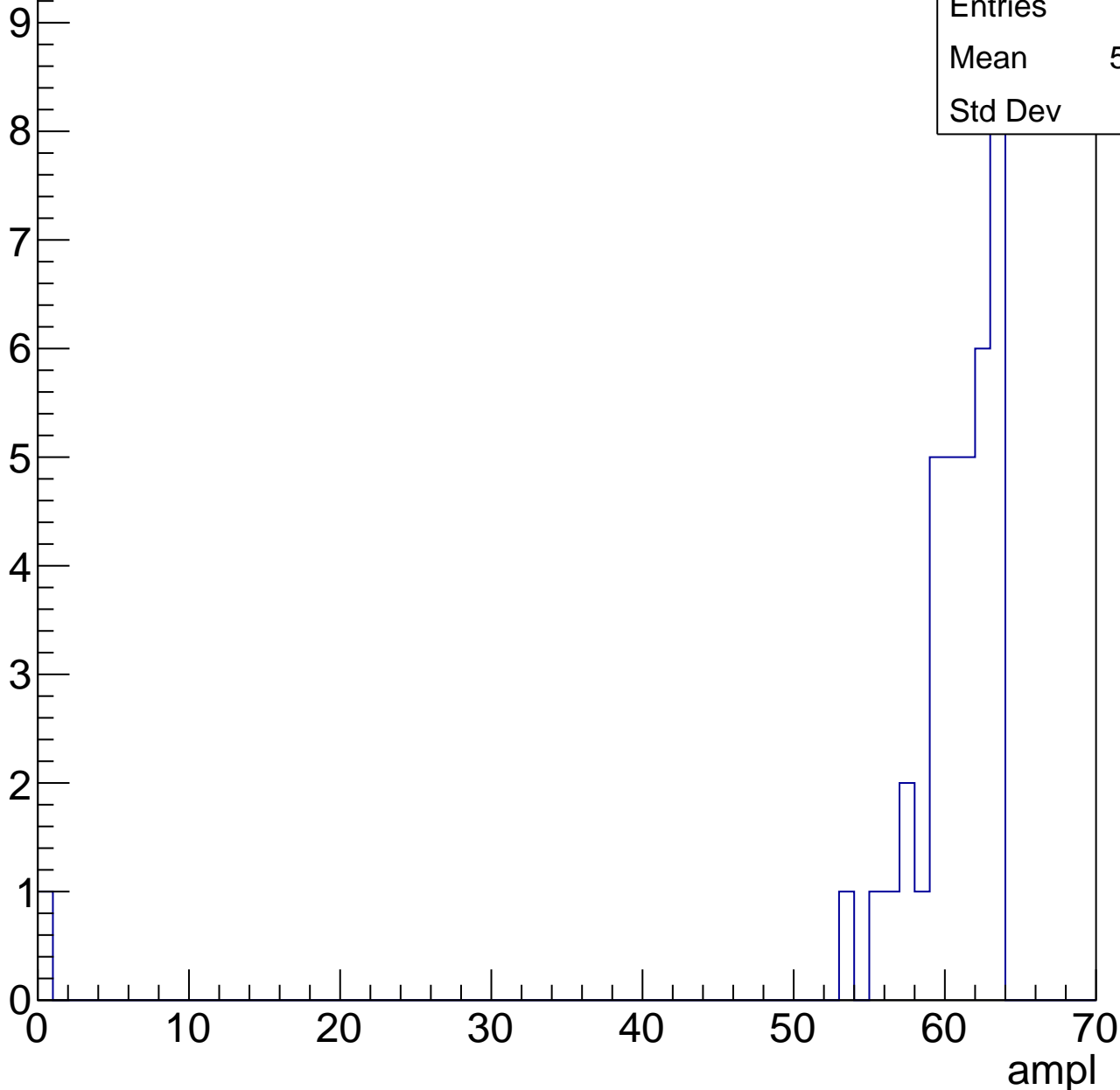


# B0L002S, U2-ch29, adc5

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

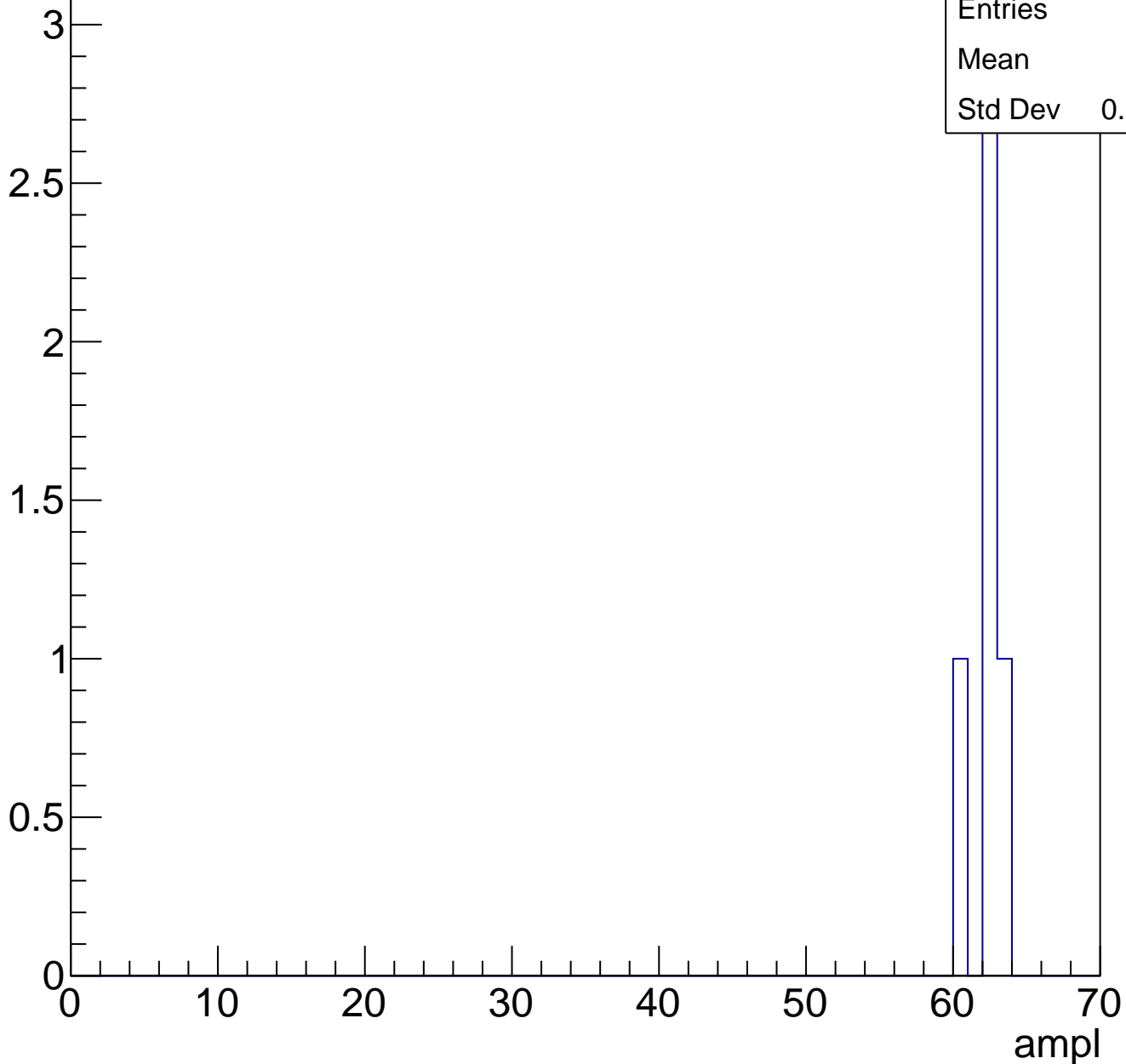
Entries	37
Mean	58.78
Std Dev	10.1



# B0L002S, U2-ch29, adc6

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry





# B0L002S, U2-ch29, adc7

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L002S, U2-ch30, adc0

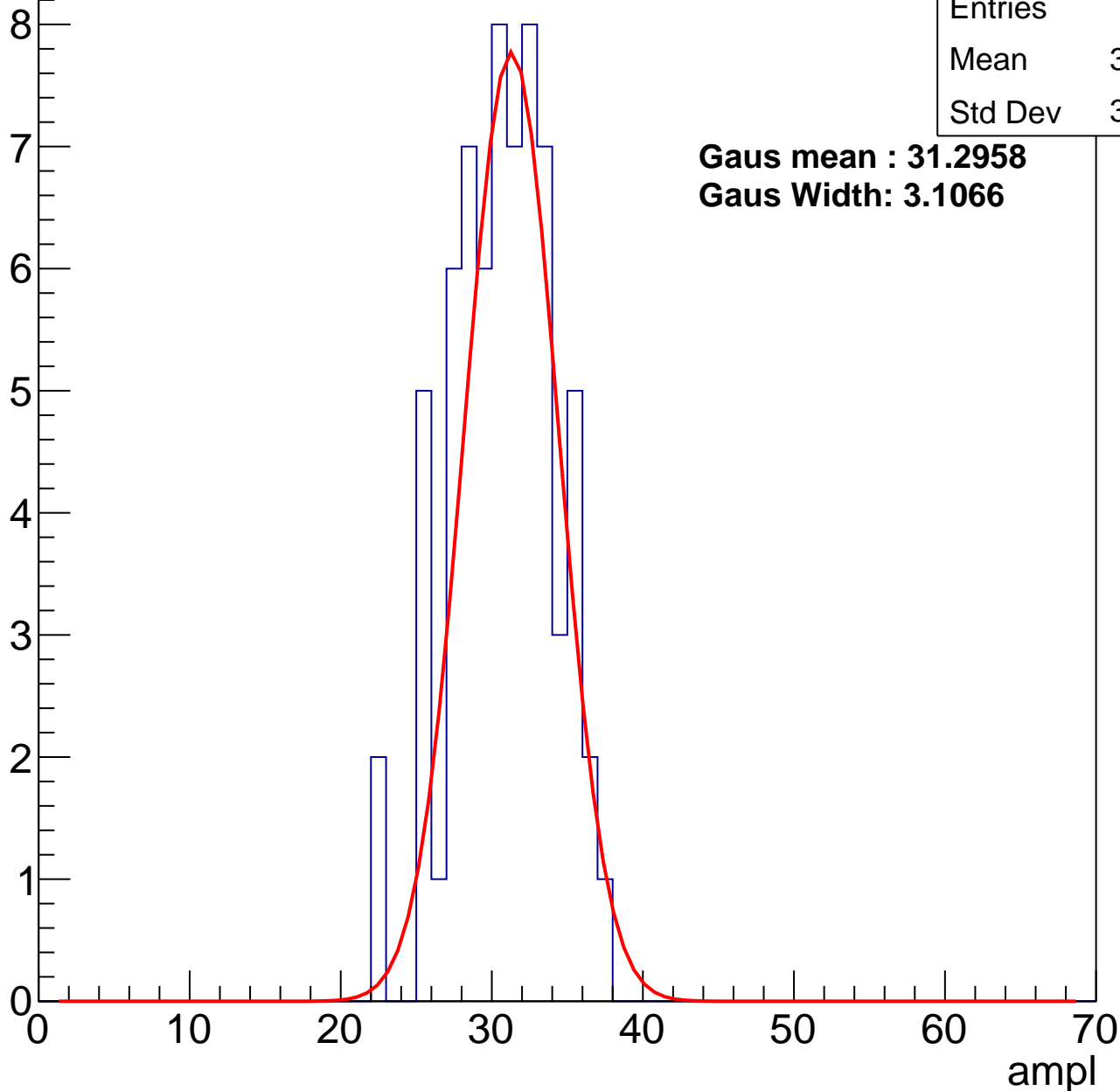
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	68
Mean	30.25
Std Dev	3.318

**Gaus mean : 31.2958**

**Gaus Width: 3.1066**



# B0L002S, U2-ch30, adc1

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entries	73
Mean	37.56
Std Dev	3.101

**Gaus mean : 37.9970**

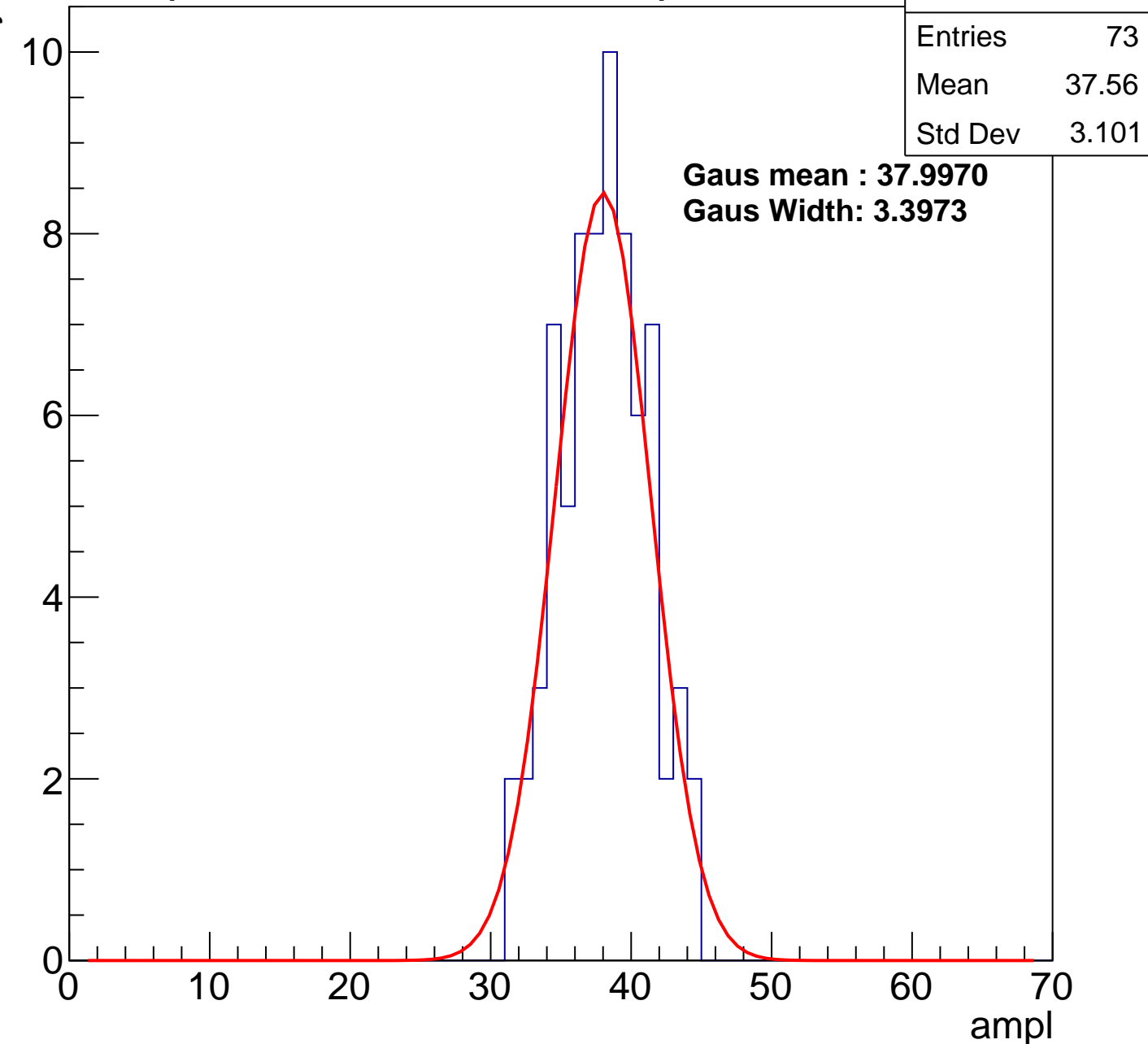
**Gaus Width: 3.3973**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B0L002S, U2-ch30, adc2

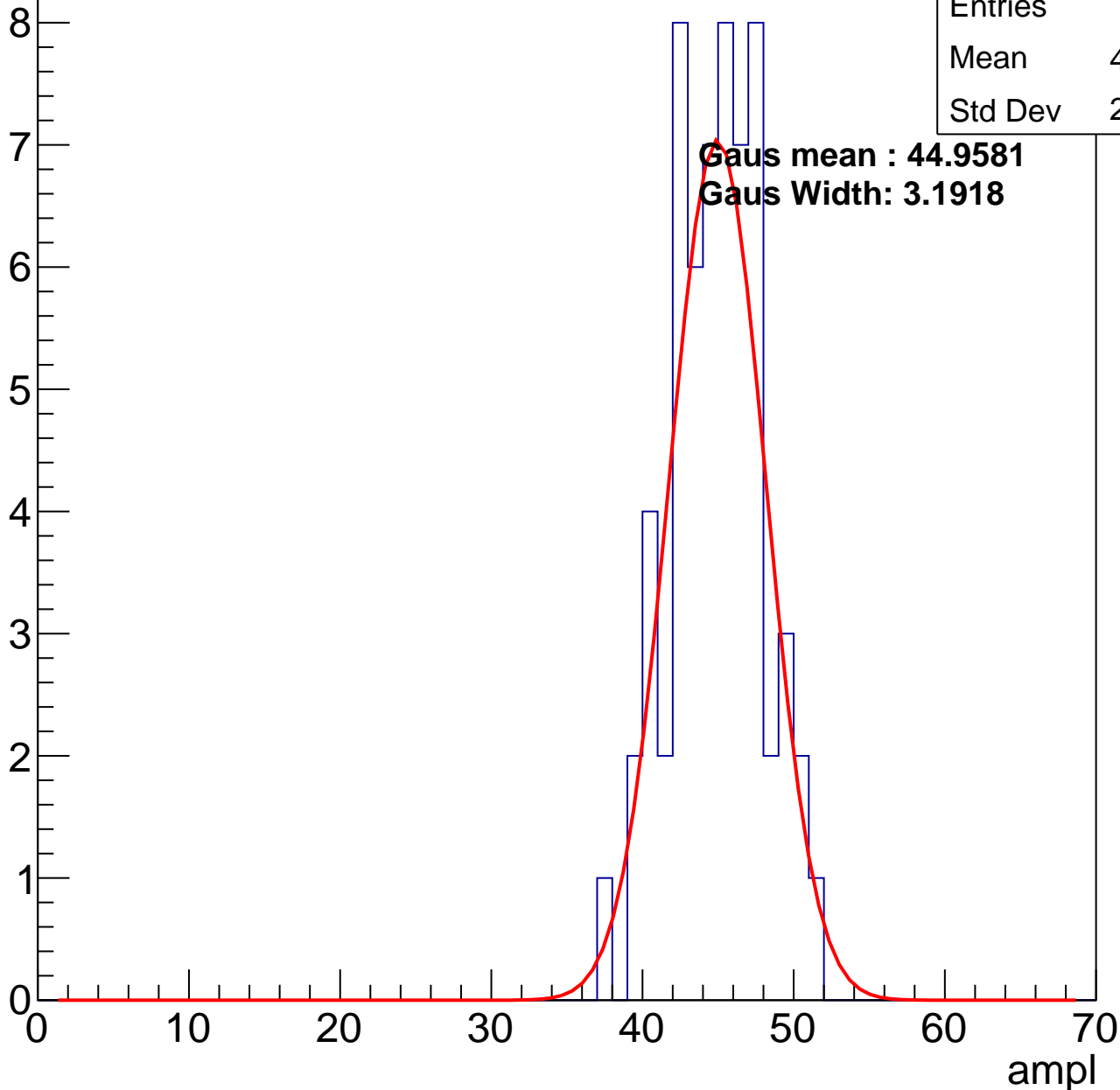
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	61
Mean	44.44
Std Dev	2.984

**Gaus mean : 44.9581**

**Gaus Width: 3.1918**

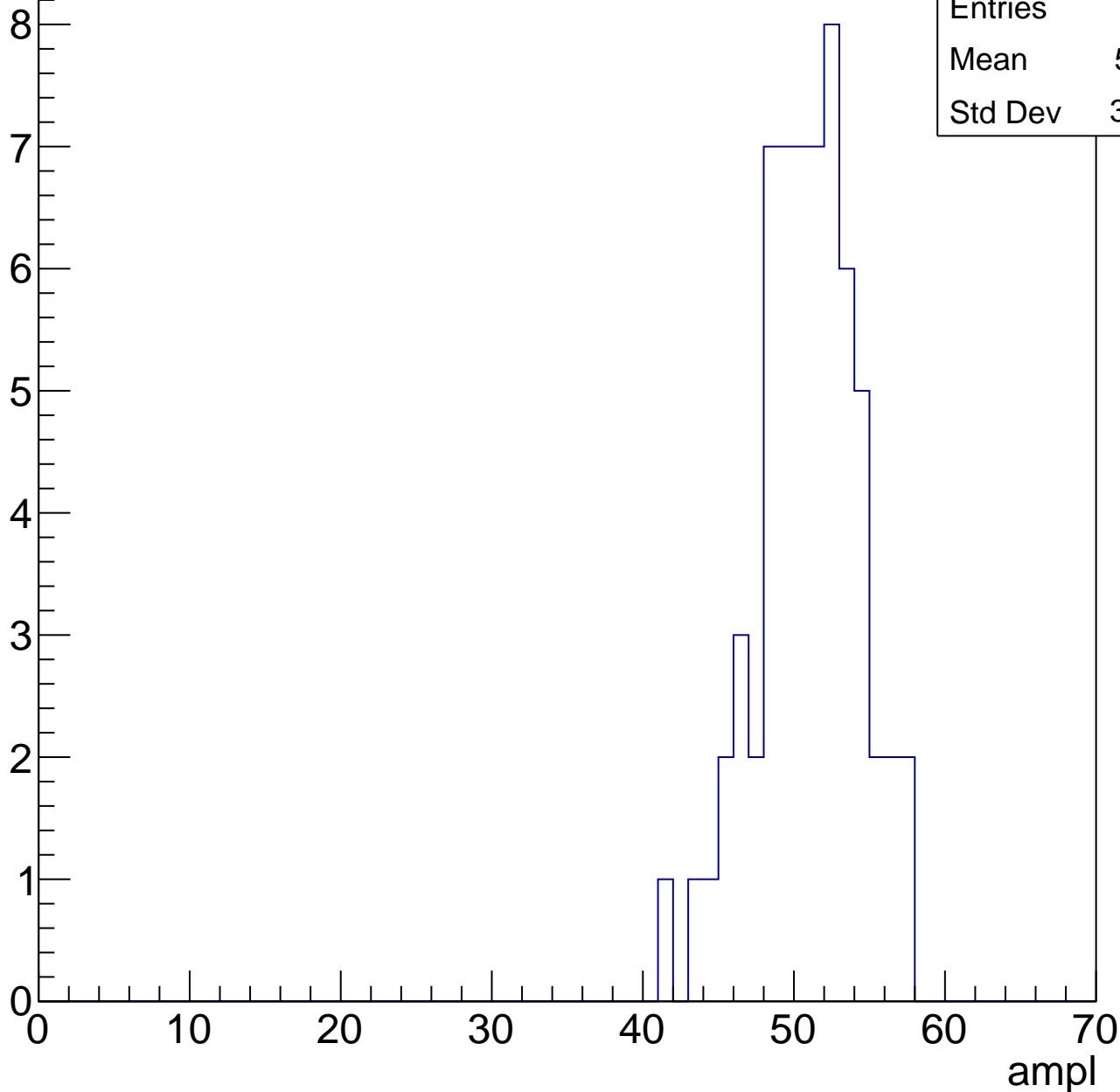


# B0L002S, U2-ch30, adc3

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

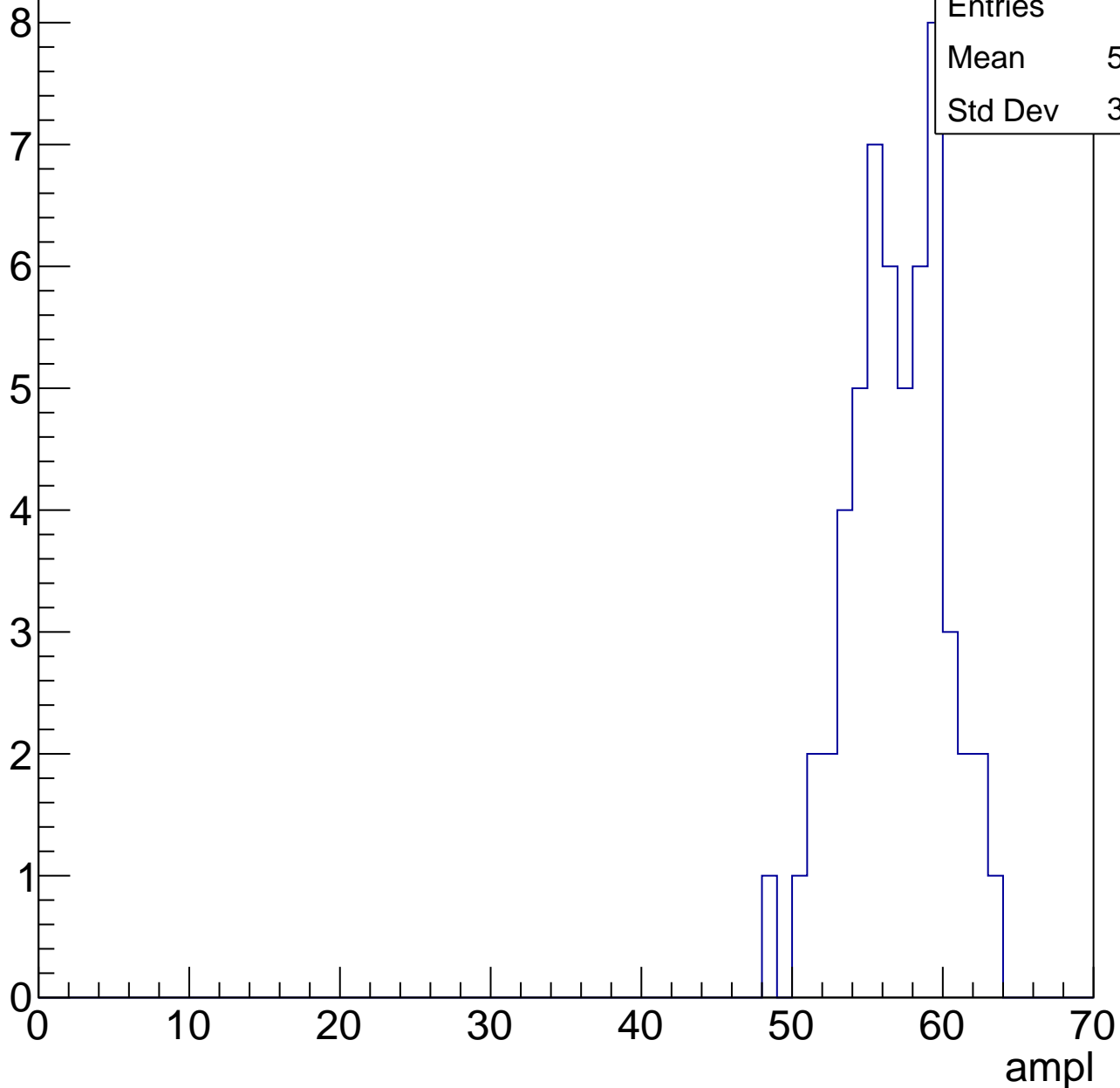
Entries	63
Mean	50.41
Std Dev	3.332



# B0L002S, U2-ch30, adc4

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



Entries	55
Mean	56.38
Std Dev	3.182

# B0L002S, U2-ch30, adc5

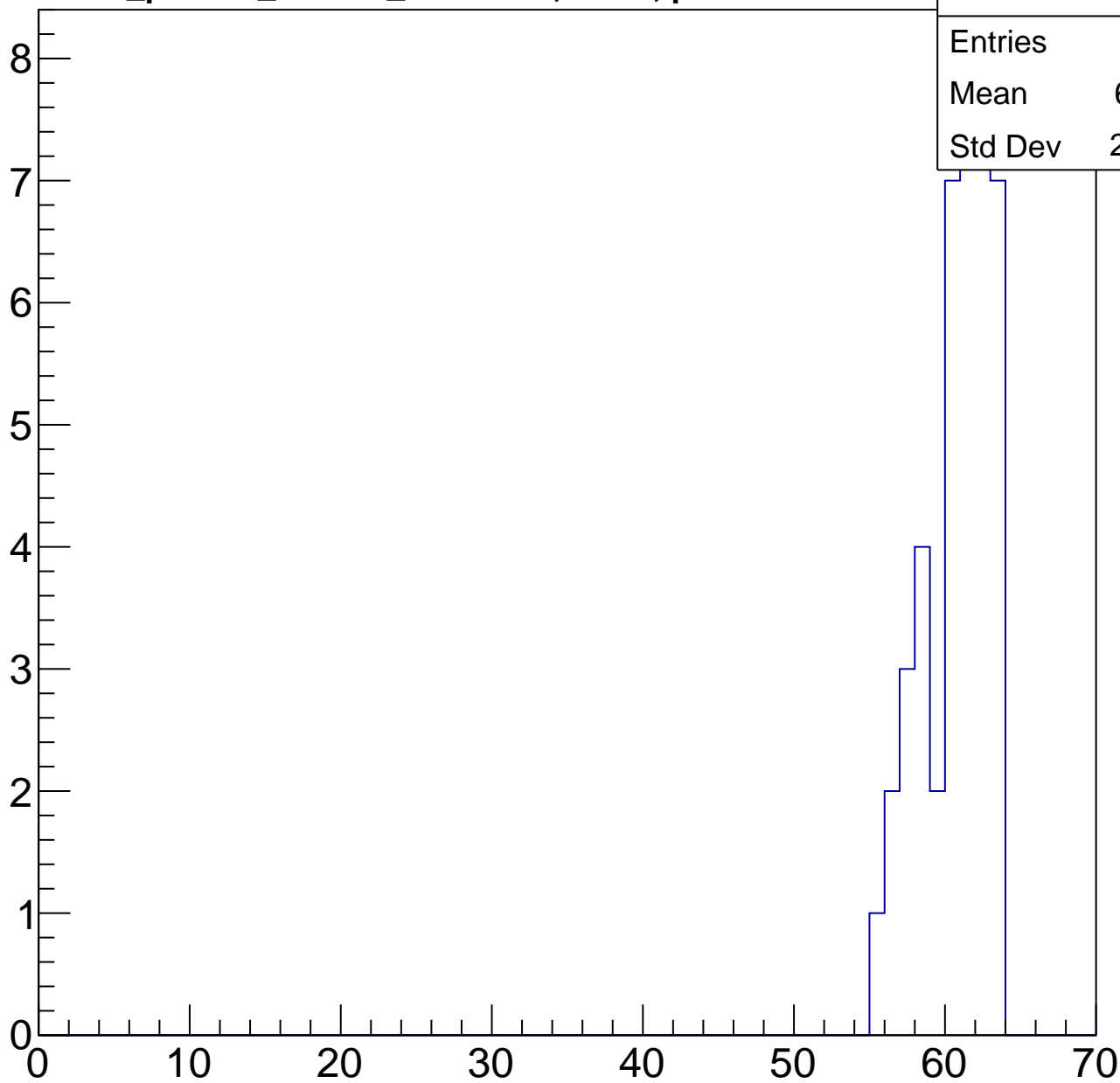
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	42
Mean	60.31
Std Dev	2.187

ampl



# B0L002S, U2-ch30, adc6

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry





# B0L002S, U2-ch30, adc7

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L002S, U2-ch31, adc0

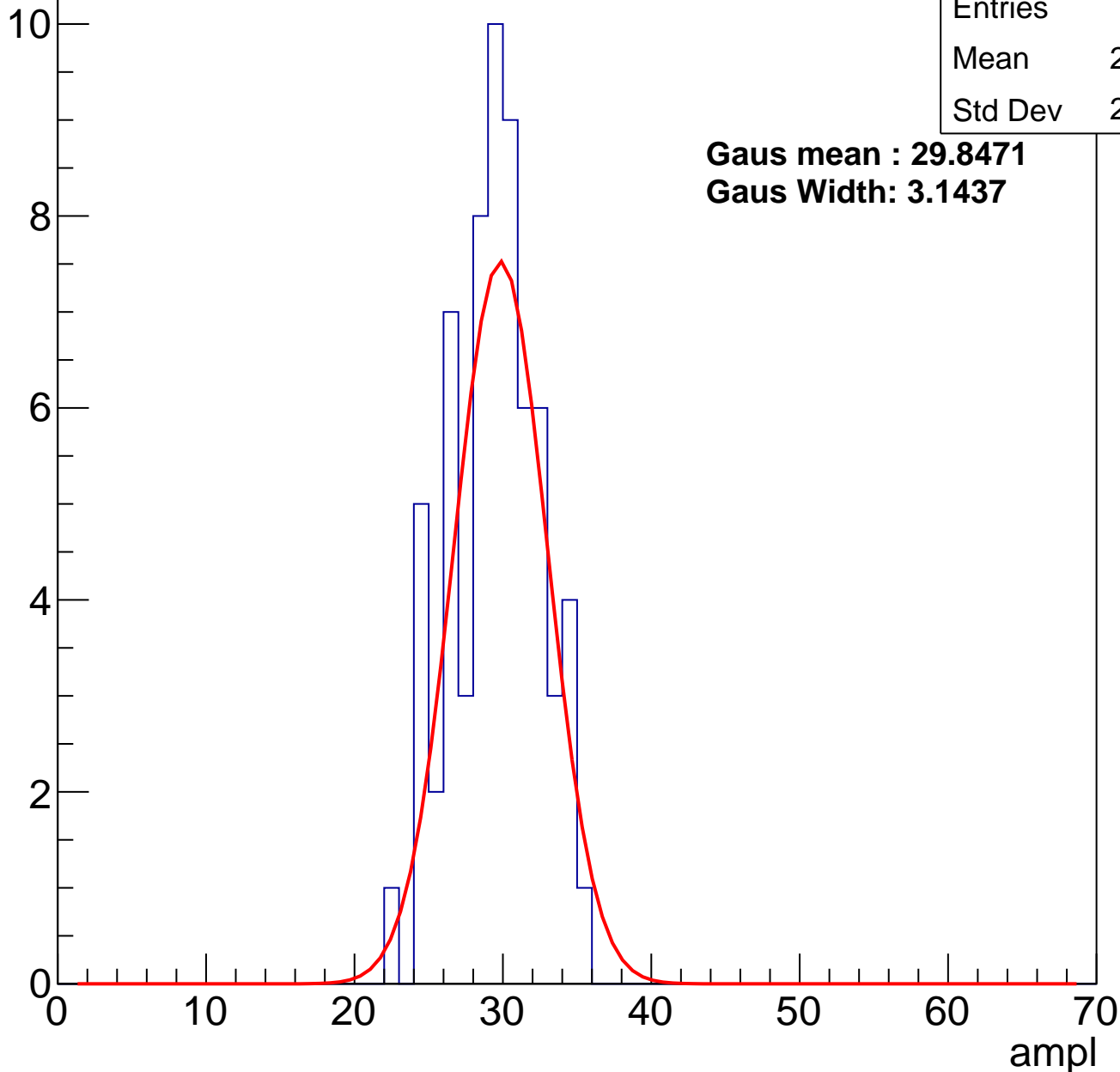
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entries	65
Mean	29.03
Std Dev	2.935

**Gaus mean : 29.8471**

**Gaus Width: 3.1437**

Entry



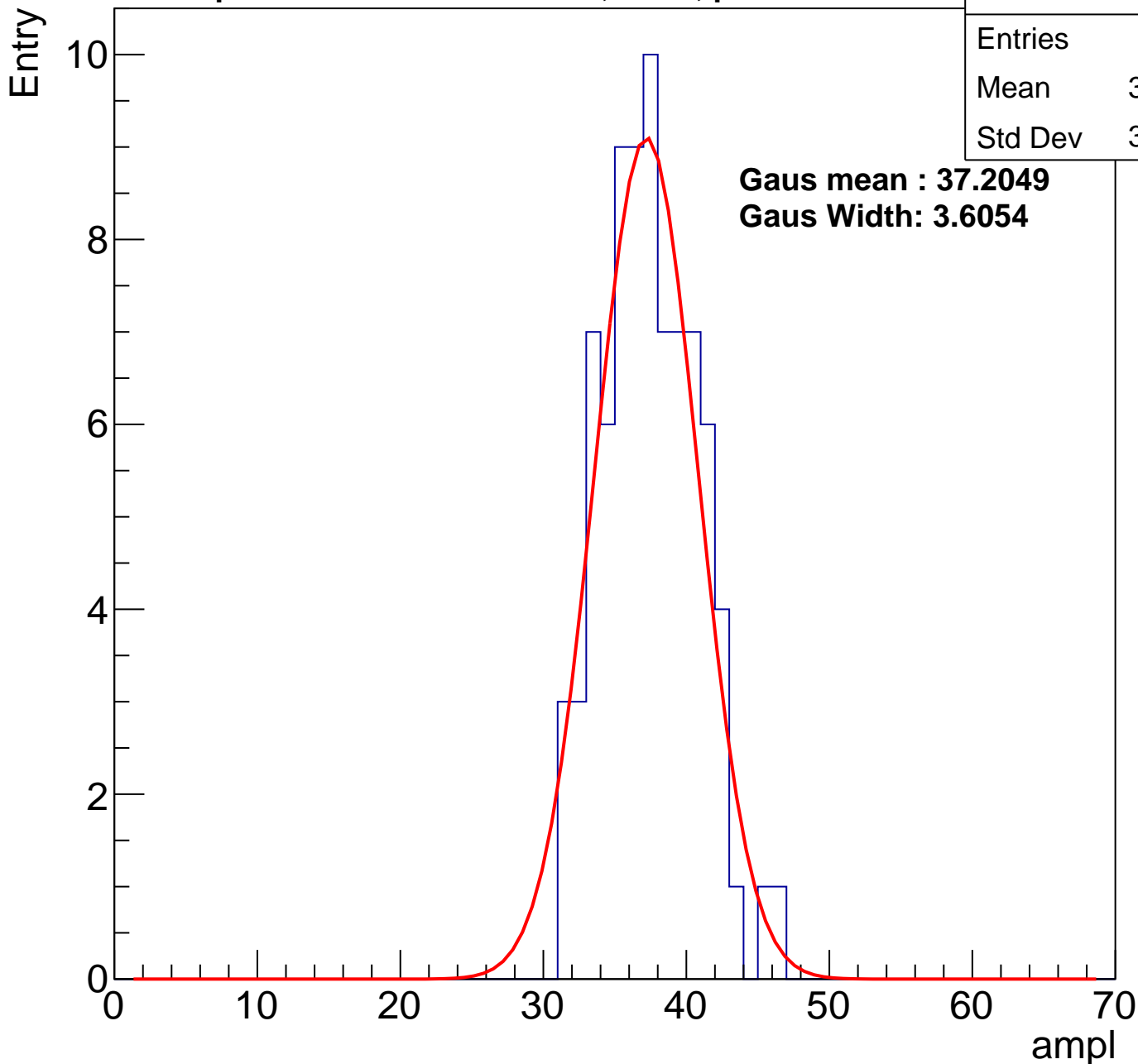
# B0L002S, U2-ch31, adc1

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entries	81
Mean	37.04
Std Dev	3.275

**Gaus mean : 37.2049**

**Gaus Width: 3.6054**



# B0L002S, U2-ch31, adc2

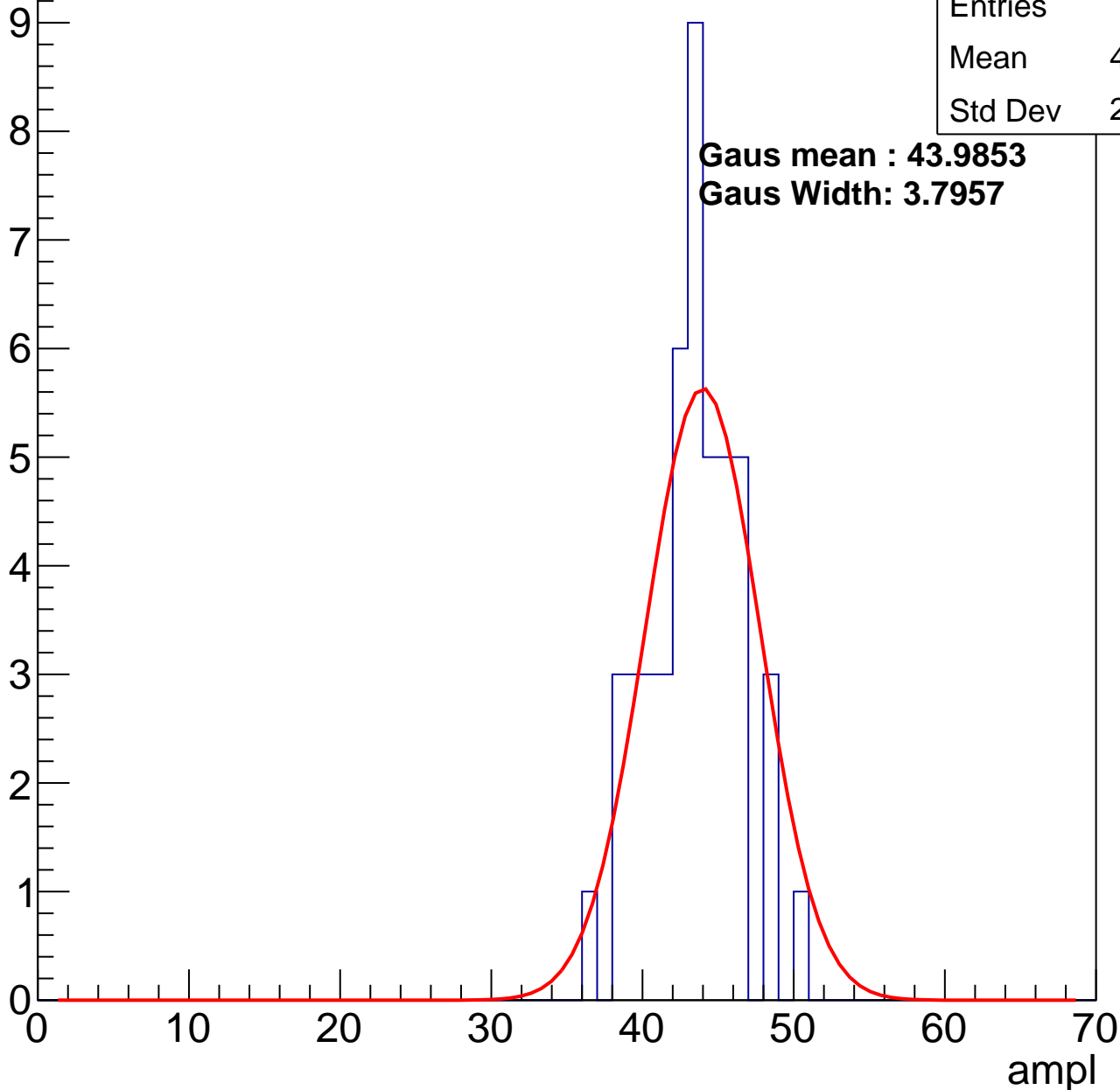
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	47
Mean	42.94
Std Dev	2.956

**Gaus mean : 43.9853**

**Gaus Width: 3.7957**



# B0L002S, U2-ch31, adc3

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entries	92
Mean	50.17
Std Dev	3.749

Entry

10

8

6

4

2

0

0

10

20

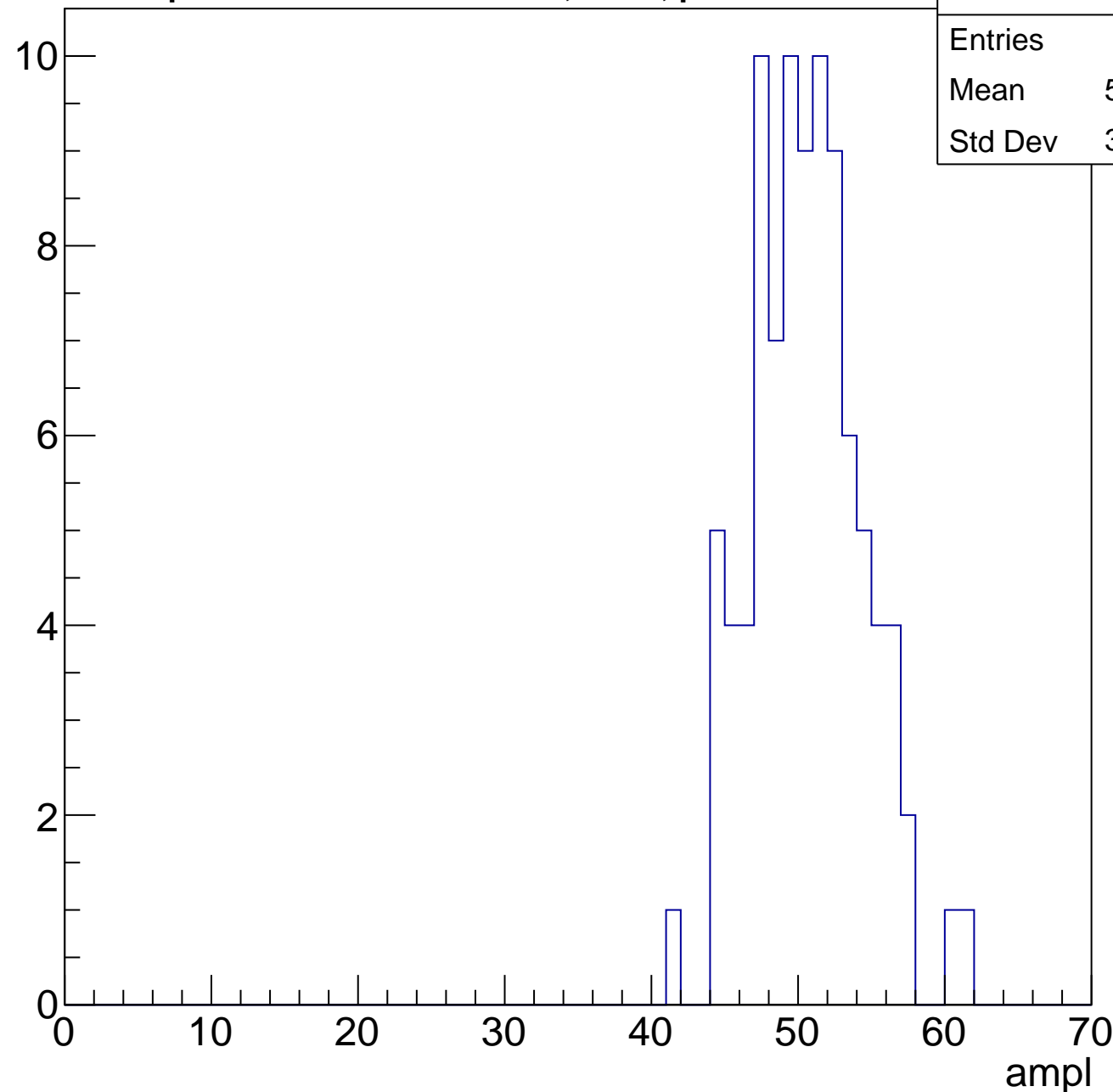
30

40

50

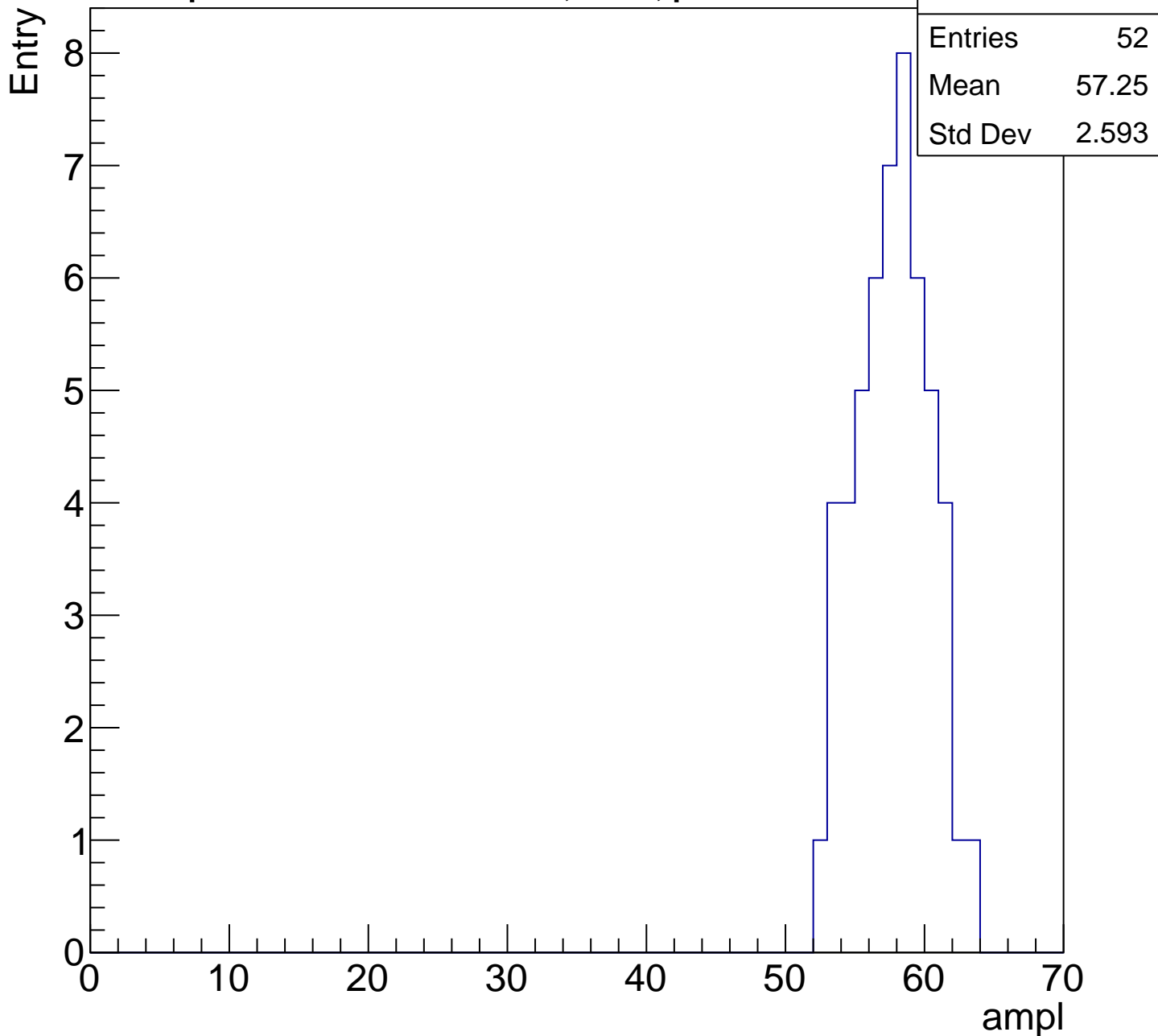
60

ampl



# B0L002S, U2-ch31, adc4

calib\_packv5\_042523\_0143.root, FC#8, port C1

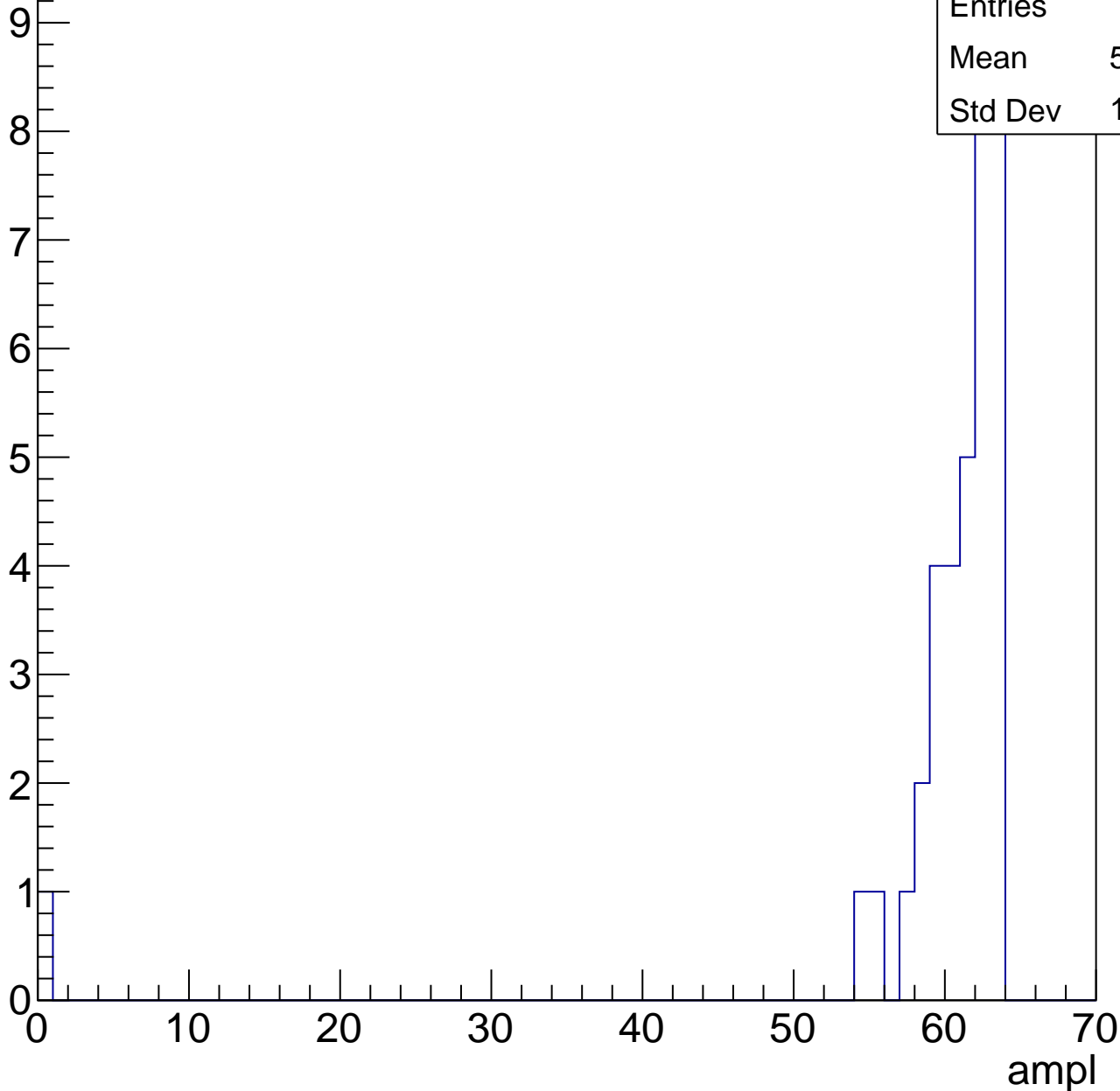


# B0L002S, U2-ch31, adc5

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	36
Mean	59.03
Std Dev	10.22



# B0L002S, U2-ch31, adc6

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry





# B0L002S, U2-ch31, adc7

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



Entries	0
Mean	0
Std Dev	0

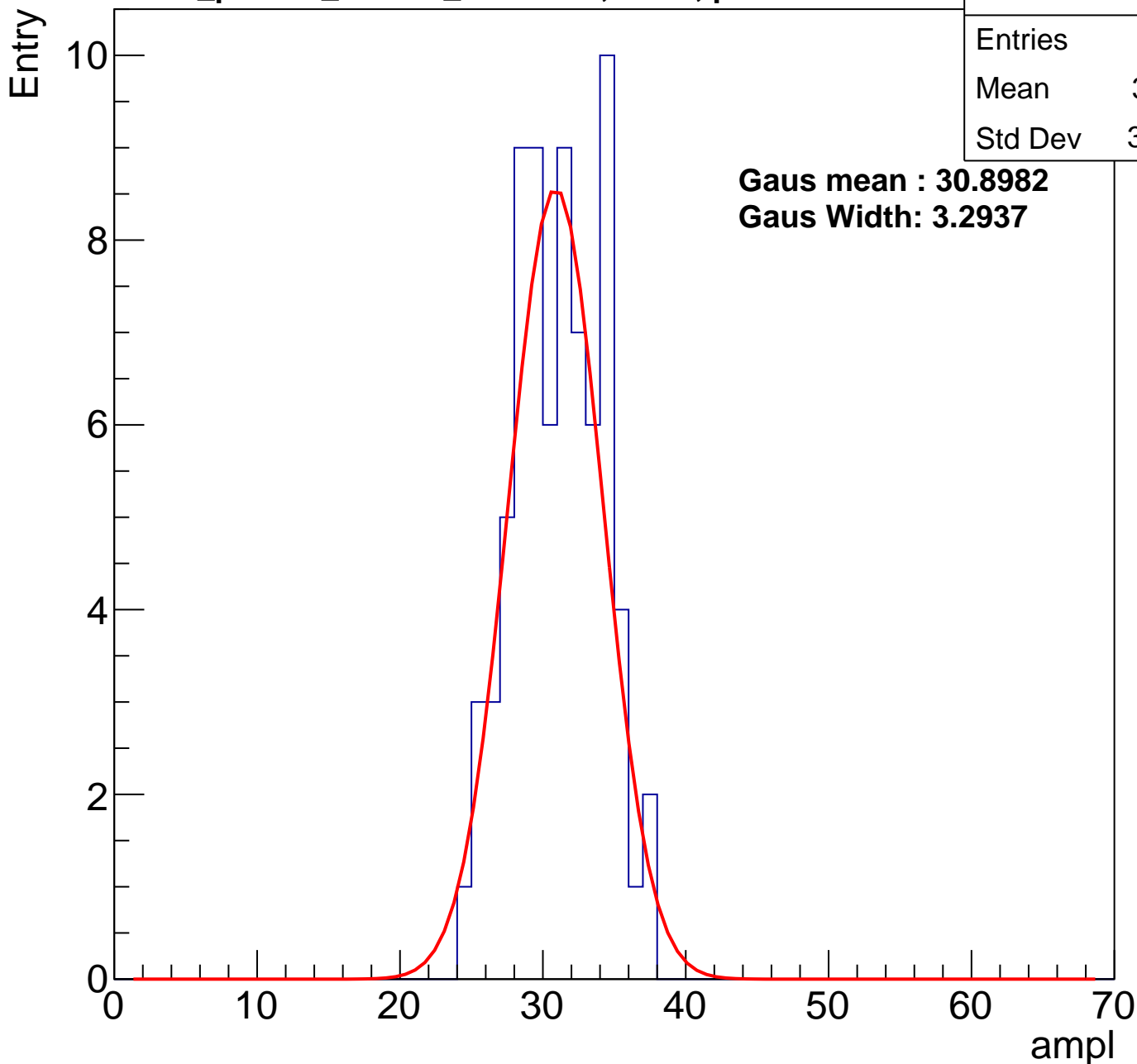
# B0L002S, U2-ch32, adc0

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entries	75
Mean	30.61
Std Dev	3.068

**Gaus mean : 30.8982**

**Gaus Width: 3.2937**



# B0L002S, U2-ch32, adc1

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entries	75
Mean	38.65
Std Dev	3.489

**Gaus mean : 38.4518**

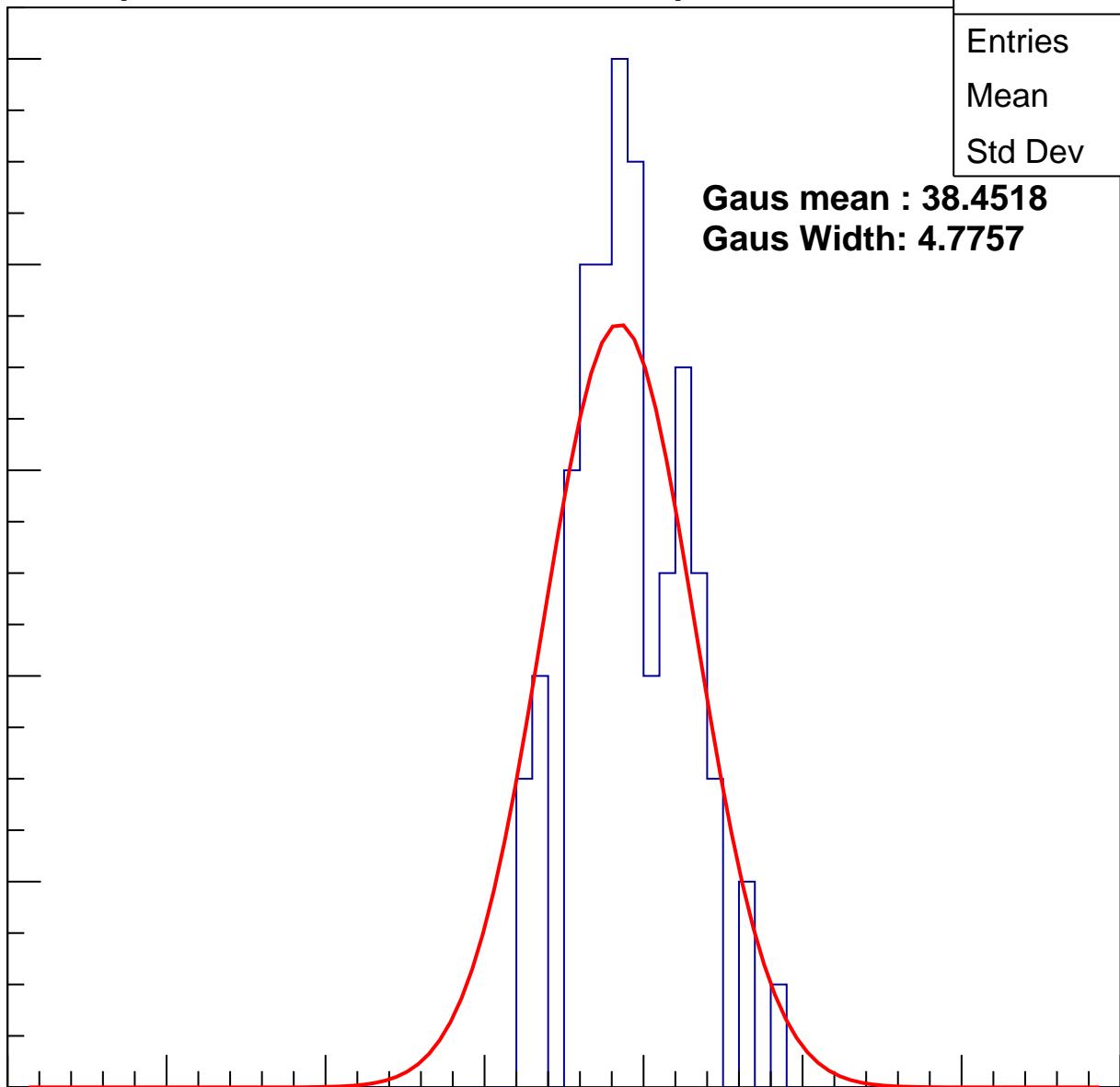
**Gaus Width: 4.7757**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L002S, U2-ch32, adc2

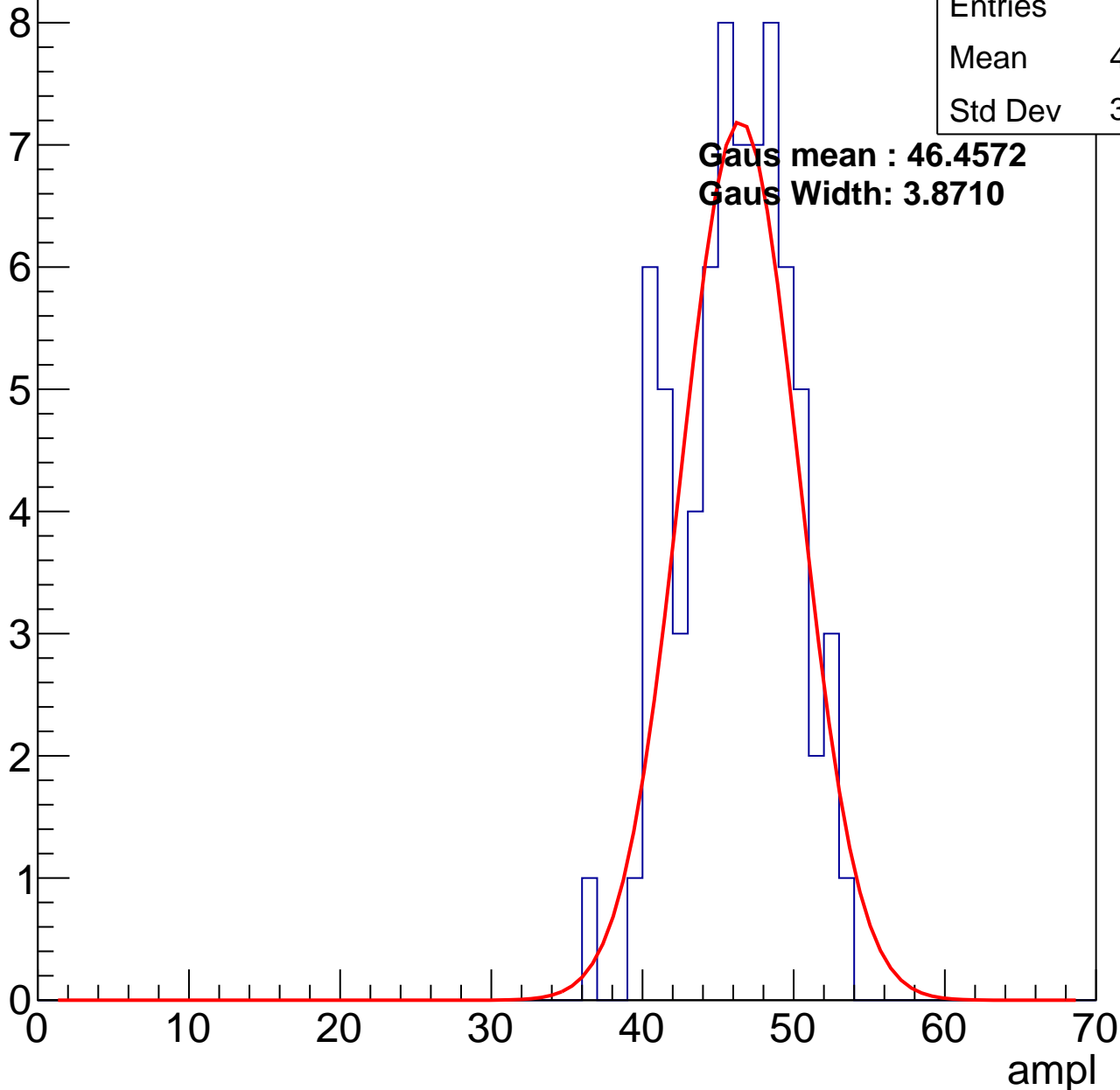
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	73
Mean	45.64
Std Dev	3.658

**Gaus mean : 46.4572**

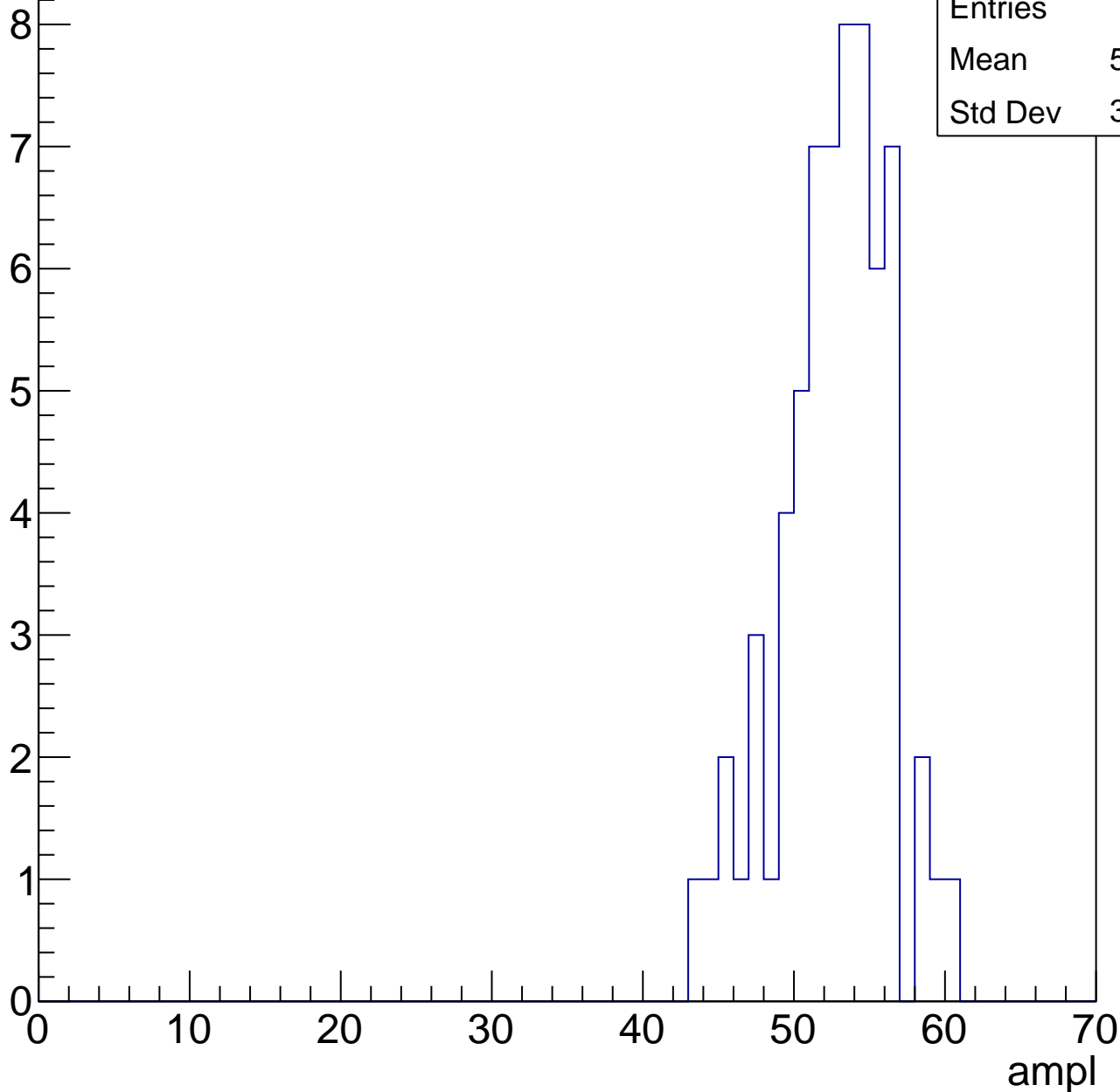
**Gaus Width: 3.8710**



# B0L002S, U2-ch32, adc3

calib\_packv5\_042523\_0143.root, FC#8, port C1

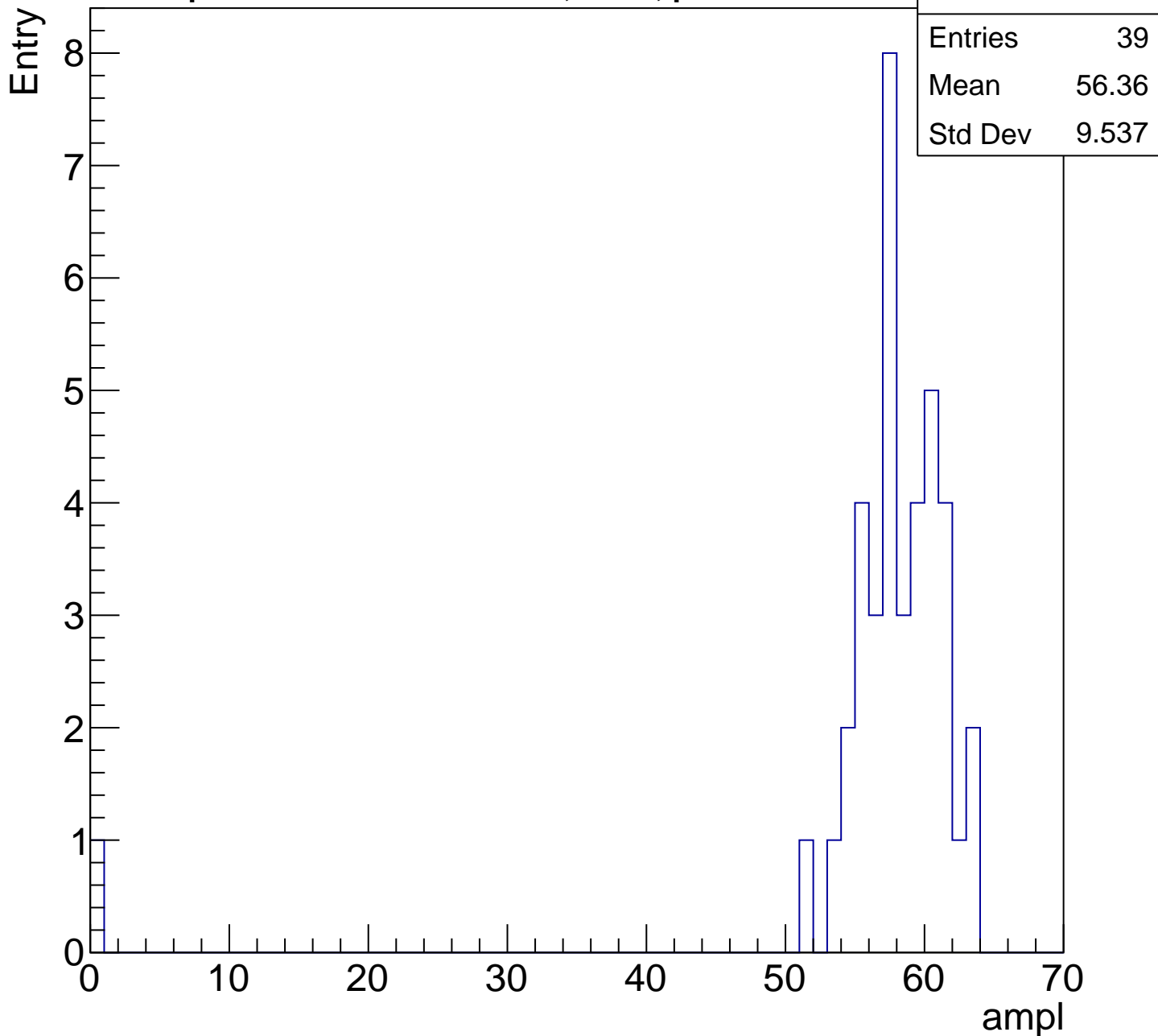
Entry



Entries	65
Mean	52.18
Std Dev	3.556

# B0L002S, U2-ch32, adc4

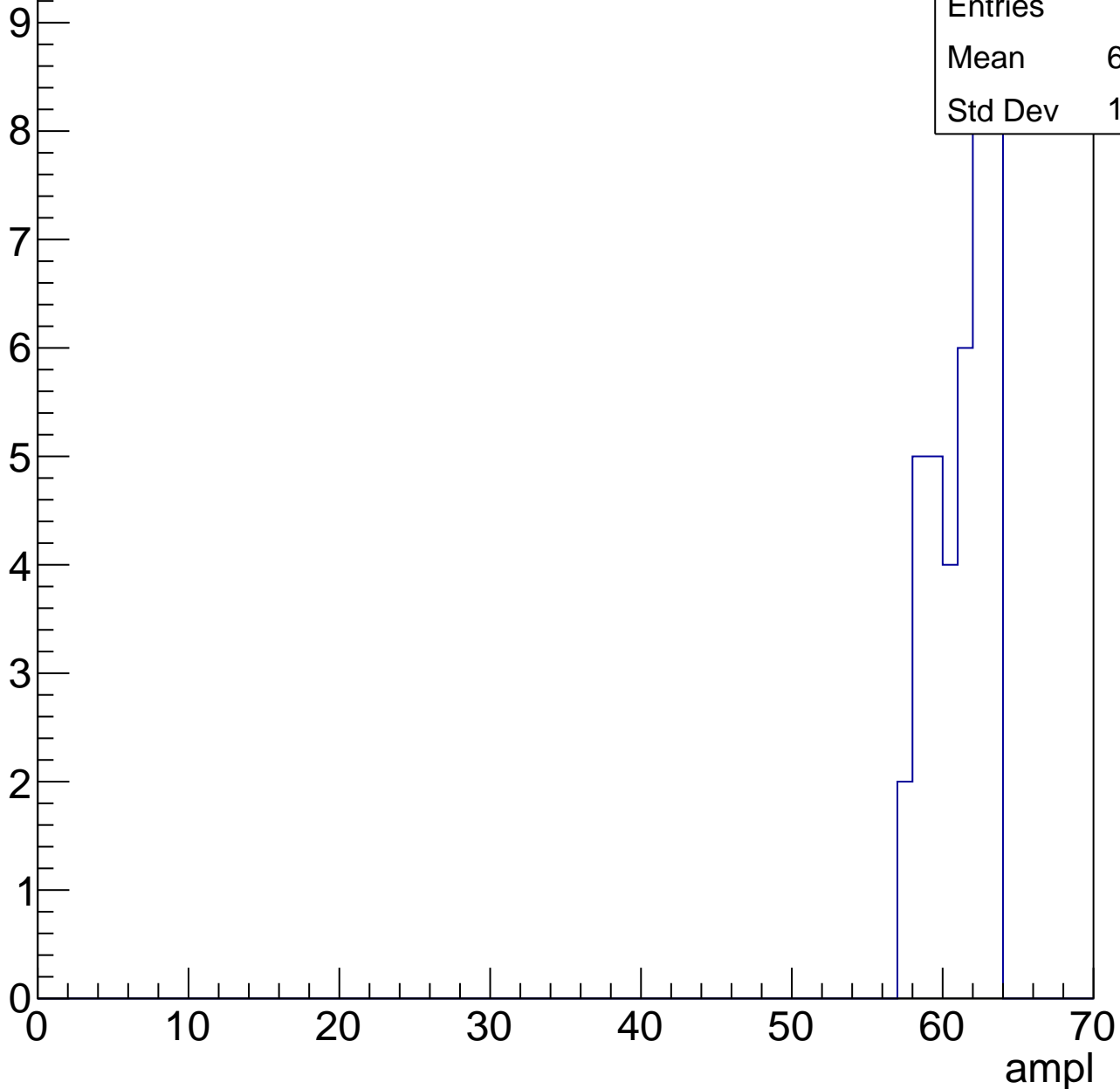
calib\_packv5\_042523\_0143.root, FC#8, port C1



# B0L002S, U2-ch32, adc5

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



# B0L002S, U2-ch32, adc6

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



Entries	0
Mean	0
Std Dev	0



# B0L002S, U2-ch32, adc7

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L002S, U2-ch33, adc0

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entries	79
Mean	29.29
Std Dev	3.576

**Gaus mean : 29.1243**

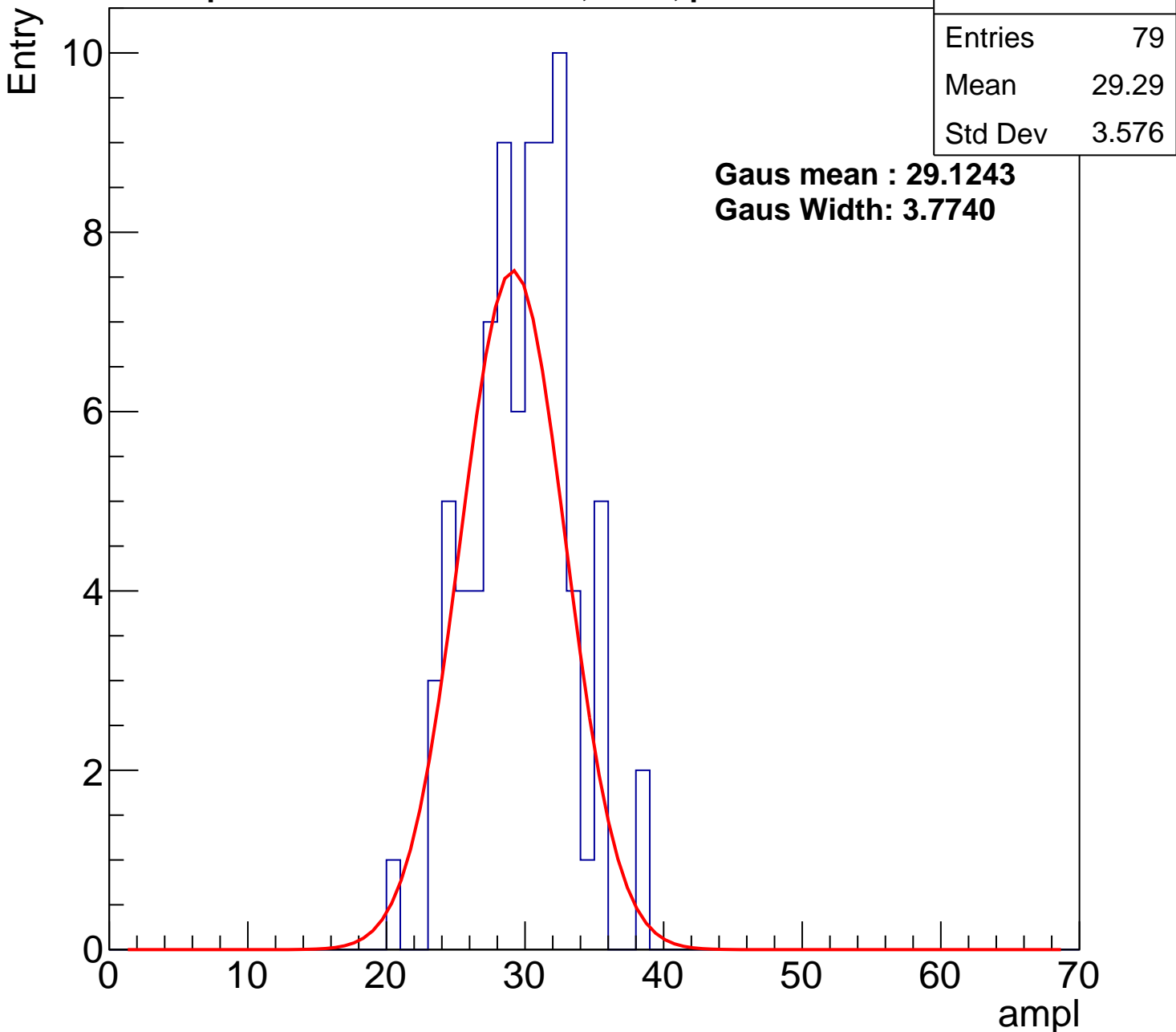
**Gaus Width: 3.7740**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L002S, U2-ch33, adc1

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entries	63
Mean	36.63
Std Dev	3.488

**Gaus mean : 36.9574**

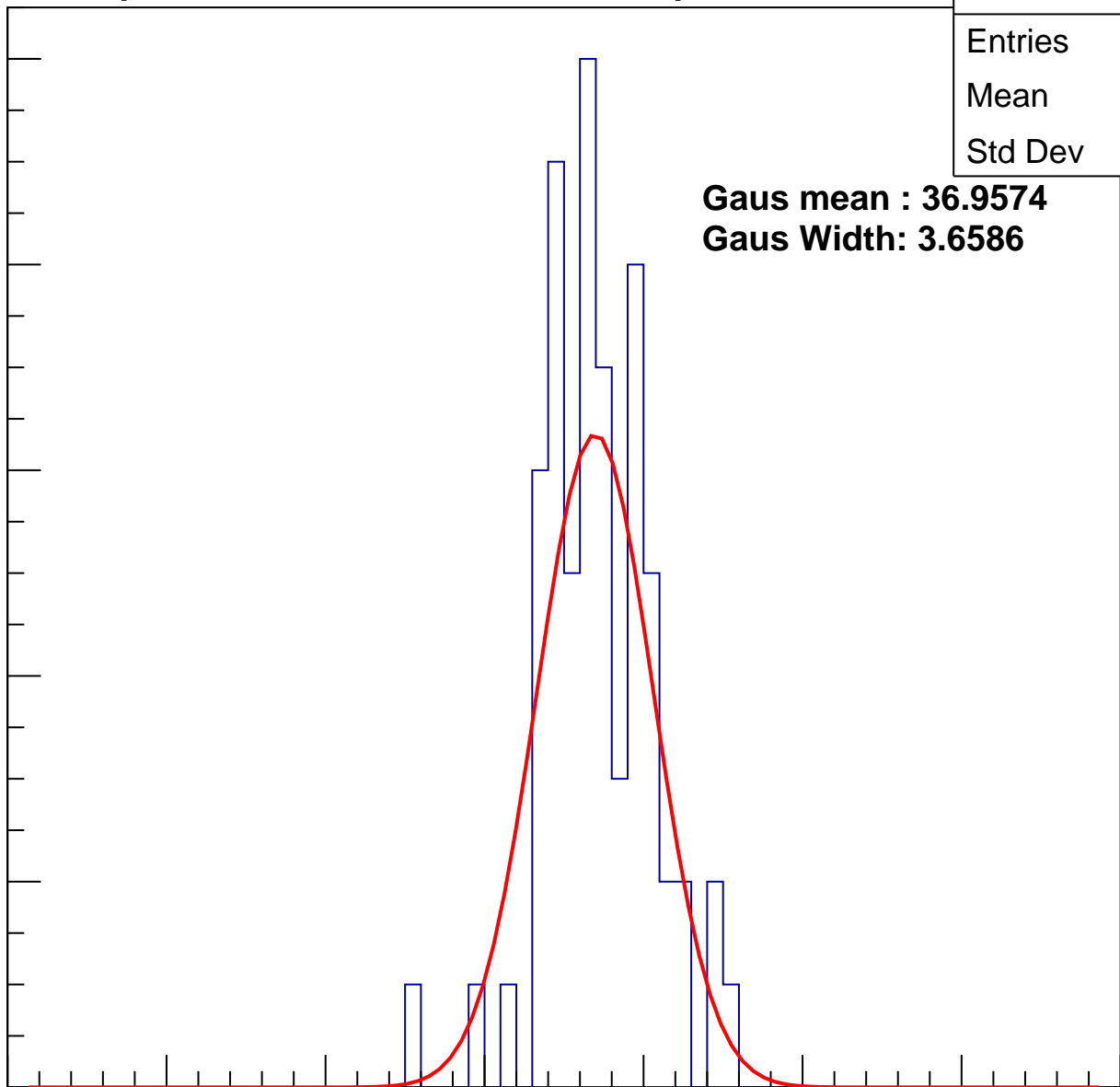
**Gaus Width: 3.6586**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L002S, U2-ch33, adc2

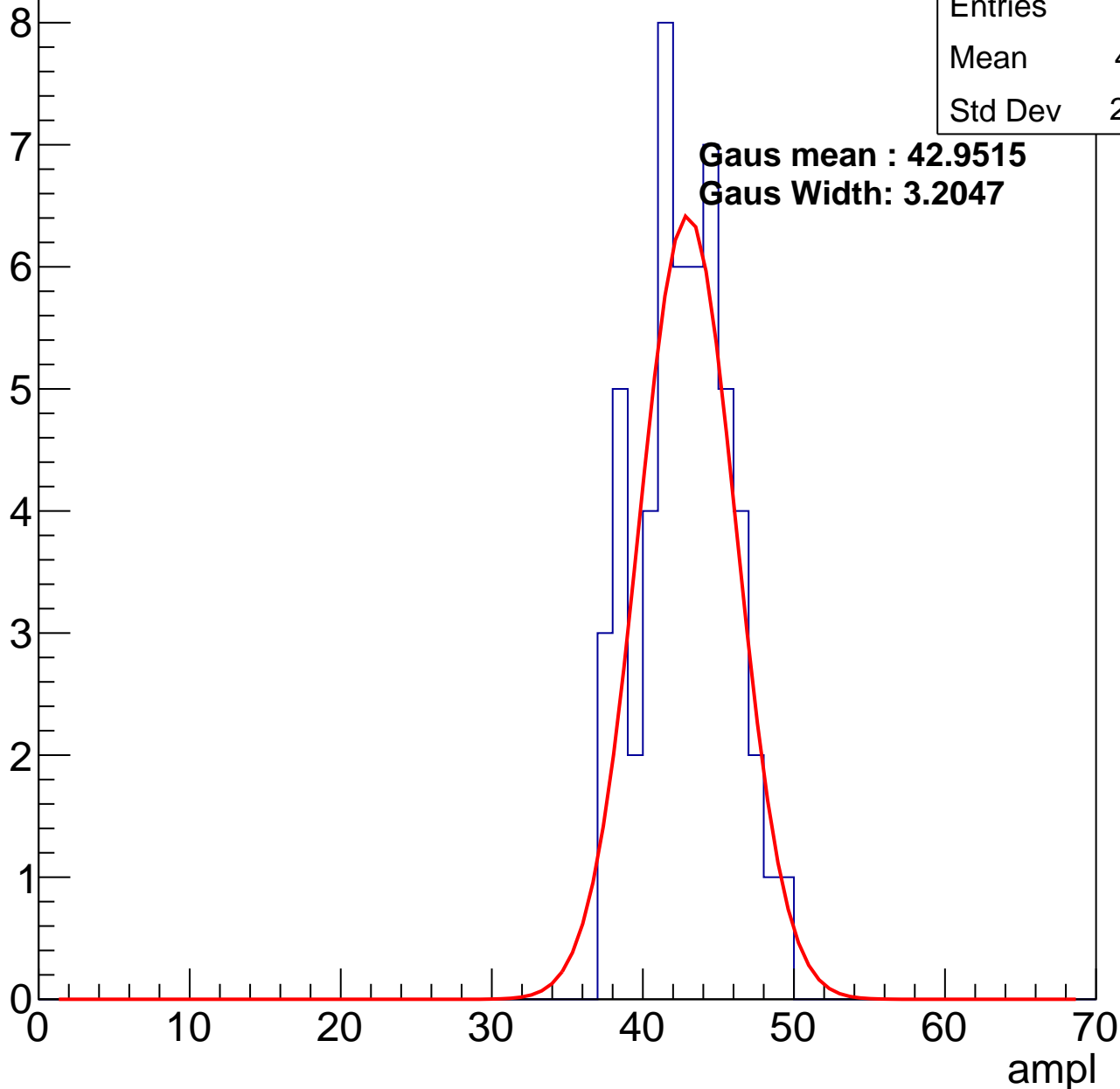
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	54
Mean	42.31
Std Dev	2.949

**Gaus mean : 42.9515**

**Gaus Width: 3.2047**



# B0L002S, U2-ch33, adc3

calib\_packv5\_042523\_0143.root, FC#8, port C1

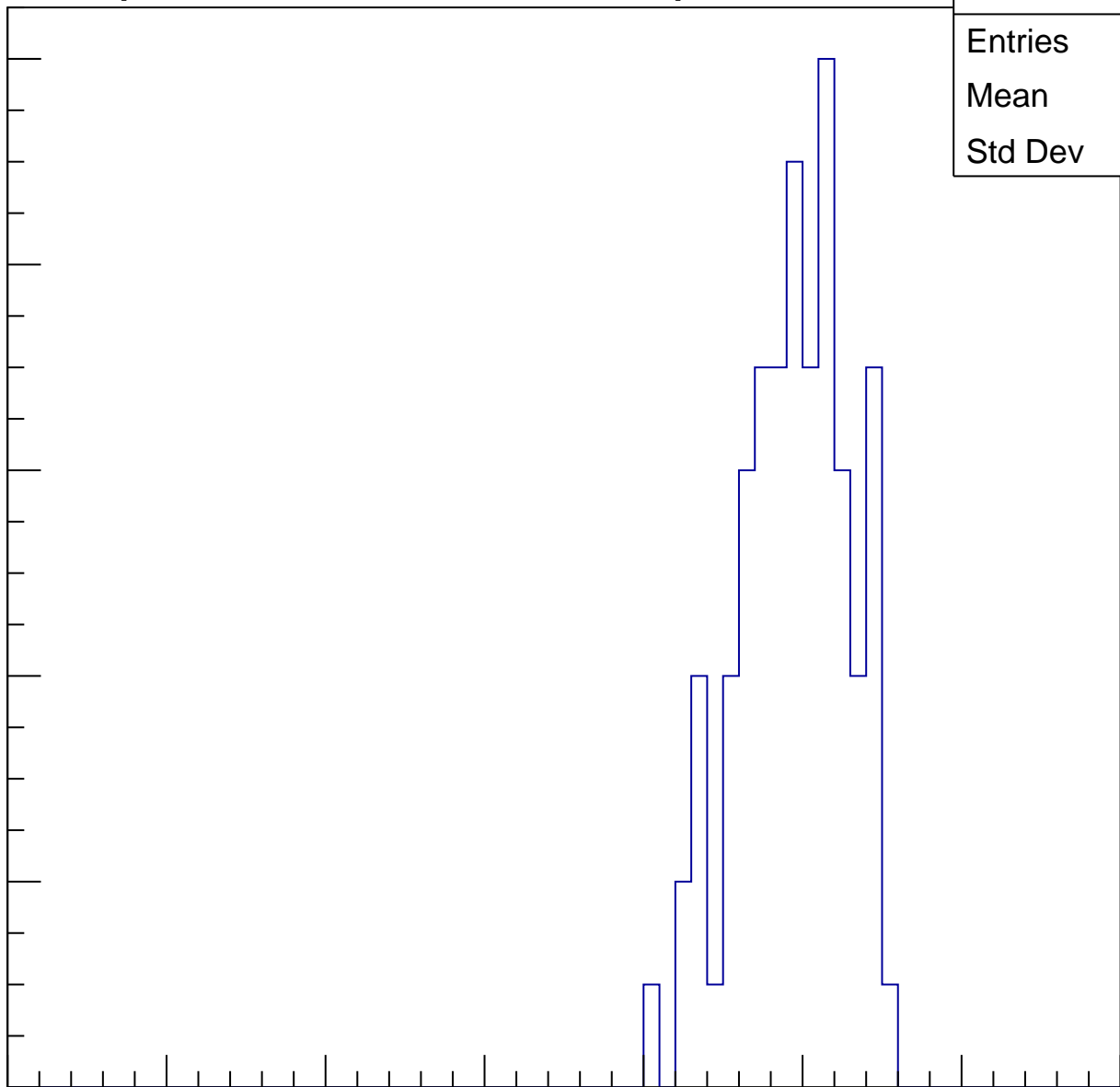
Entries	76
Mean	48.93
Std Dev	3.396

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

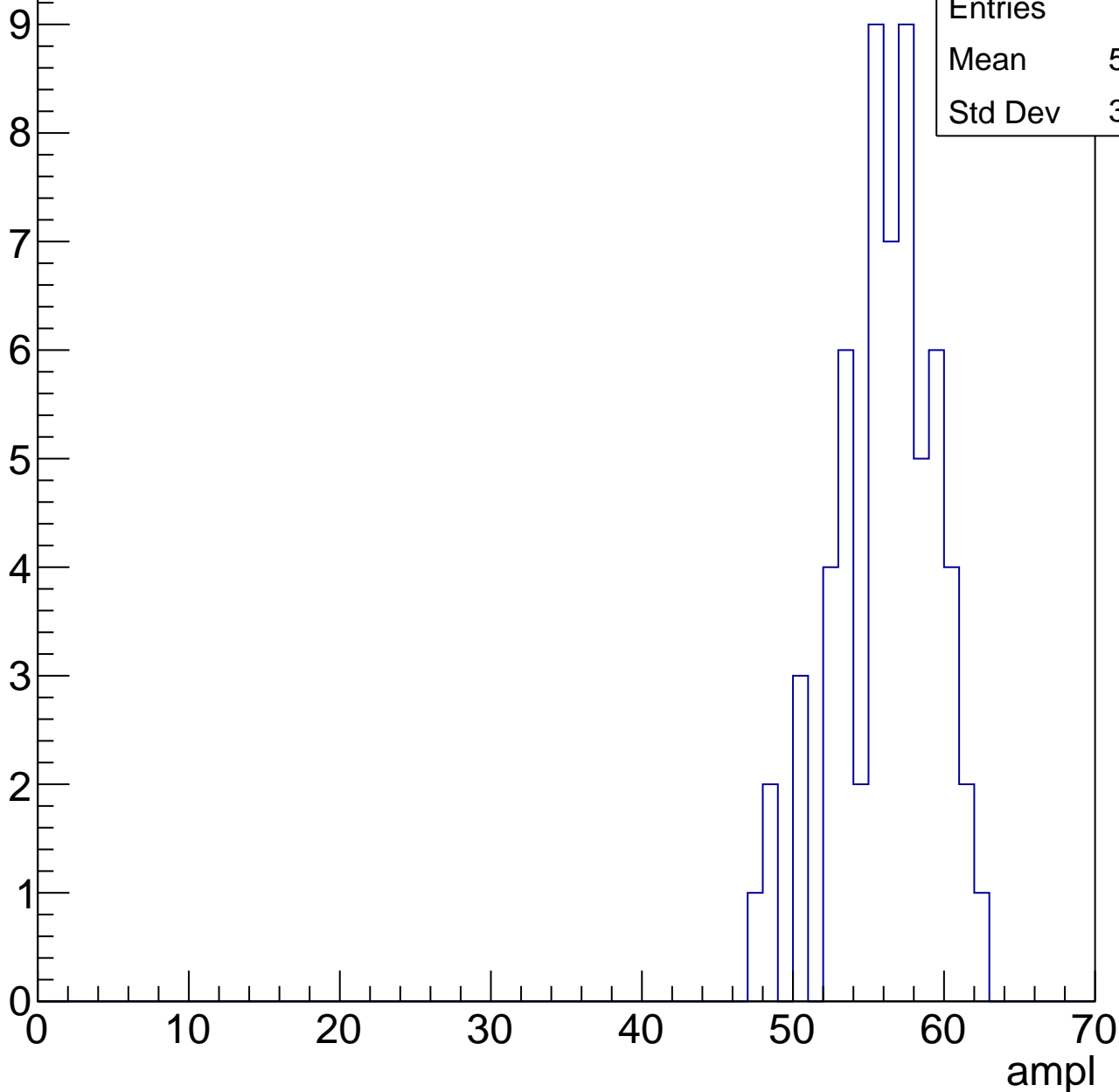


# B0L002S, U2-ch33, adc4

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	61
Mean	55.66
Std Dev	3.333

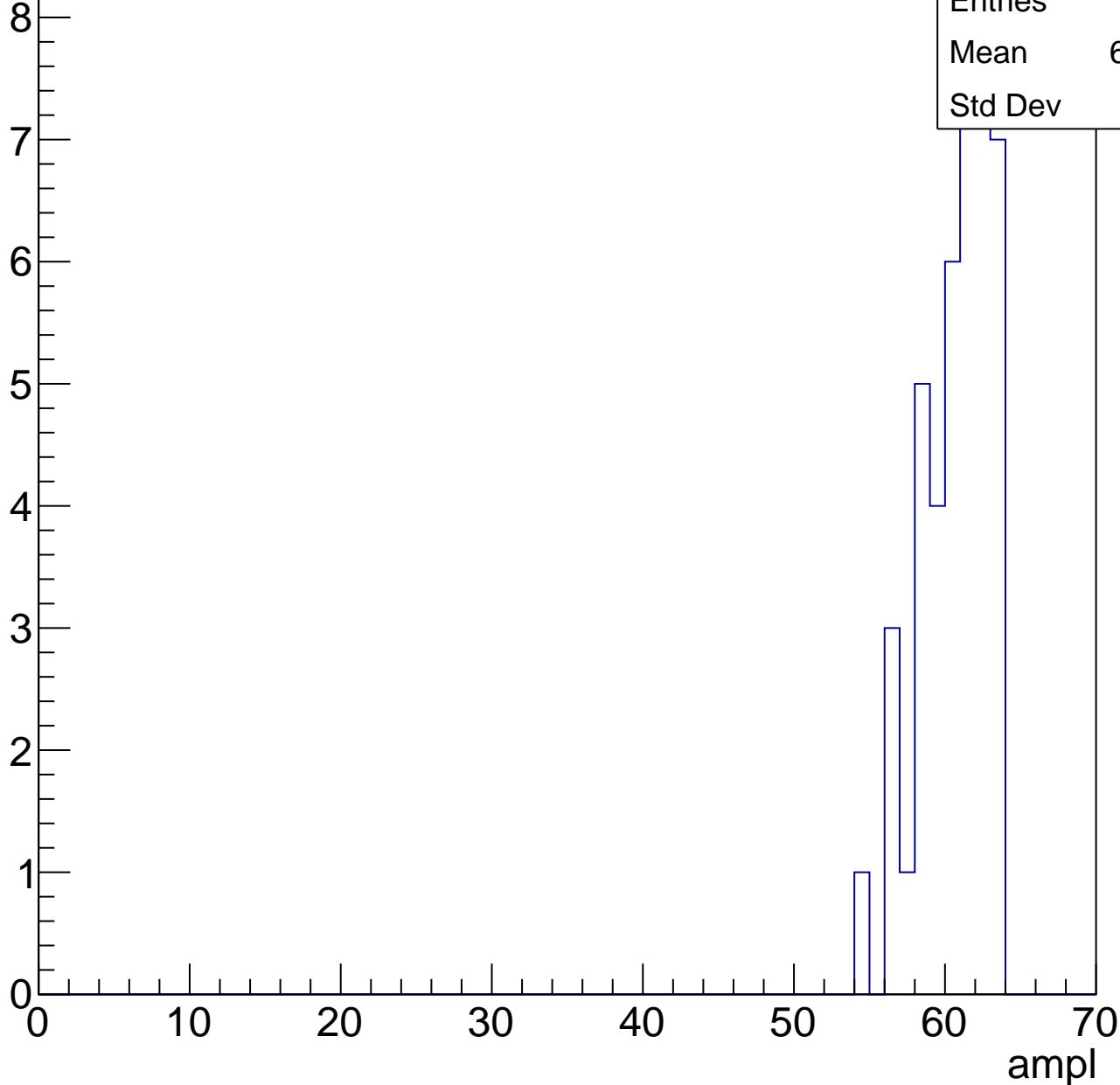


# B0L002S, U2-ch33, adc5

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

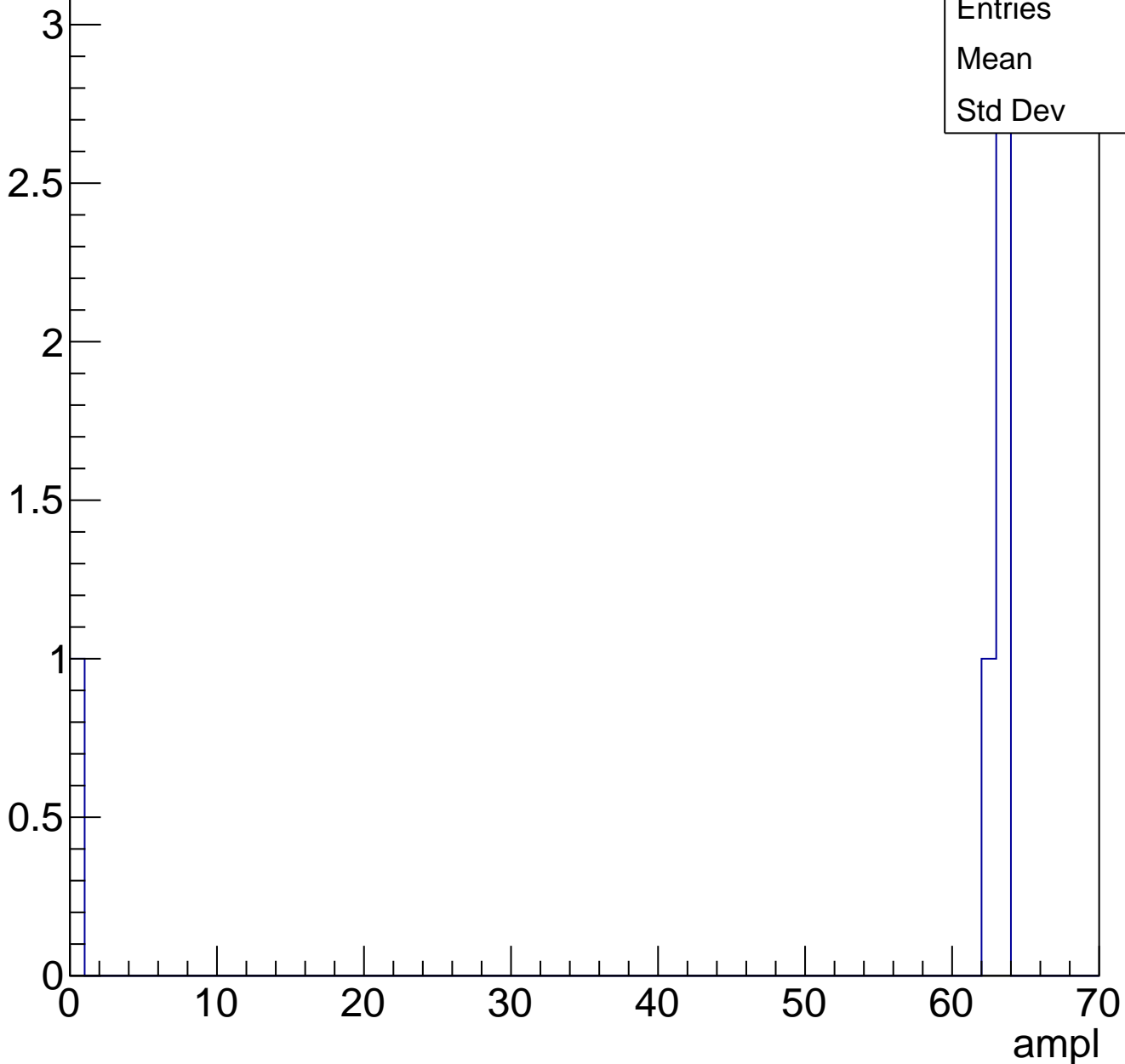
Entries	43
Mean	60.23
Std Dev	2.25



# B0L002S, U2-ch33, adc6

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry





# B0L002S, U2-ch33, adc7

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L002S, U2-ch34, adc0

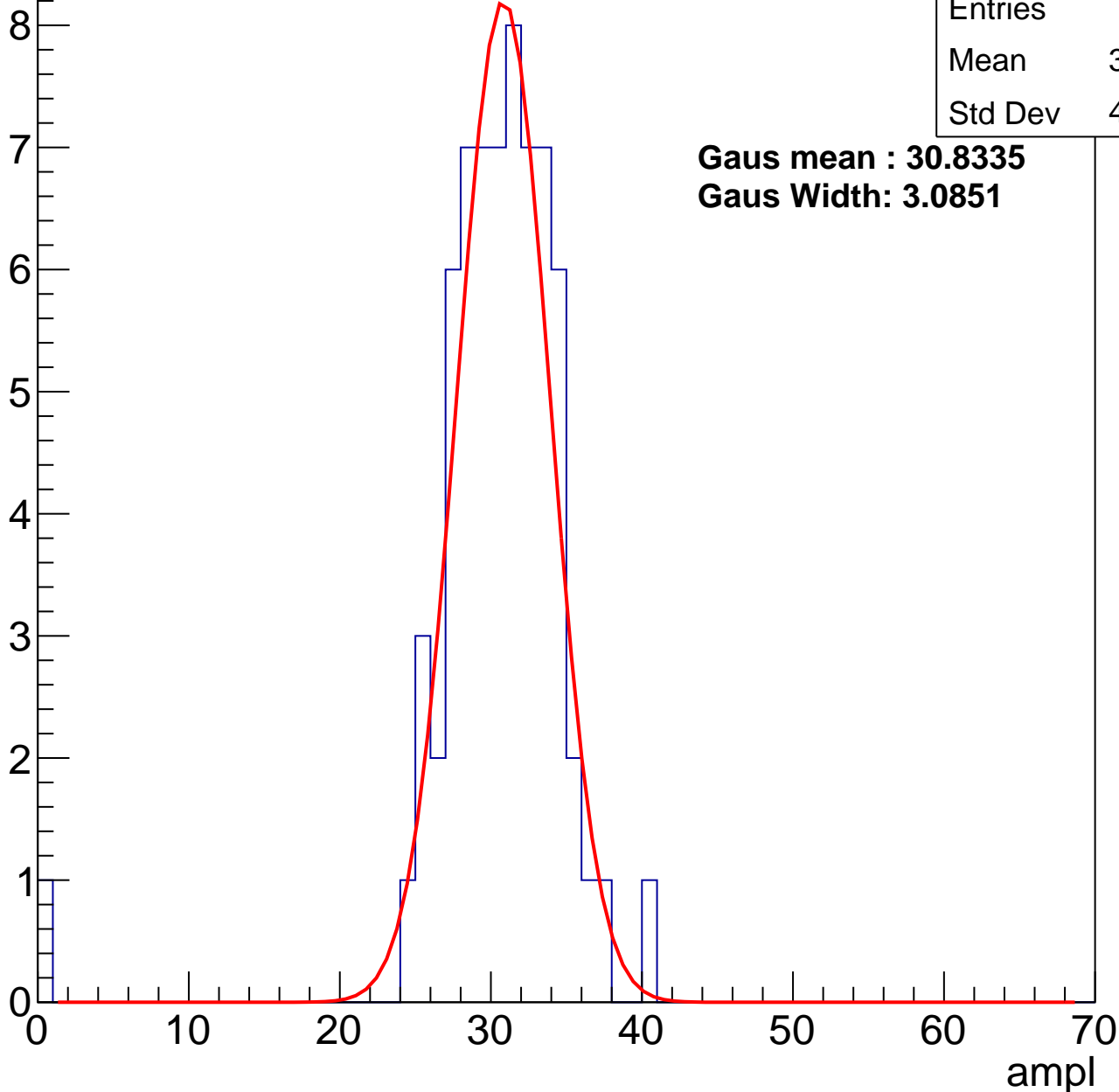
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	67
Mean	30.03
Std Dev	4.828

**Gaus mean : 30.8335**

**Gaus Width: 3.0851**



# B0L002S, U2-ch34, adc1

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entries	63
Mean	36.46
Std Dev	3.251

**Gaus mean : 37.3635**

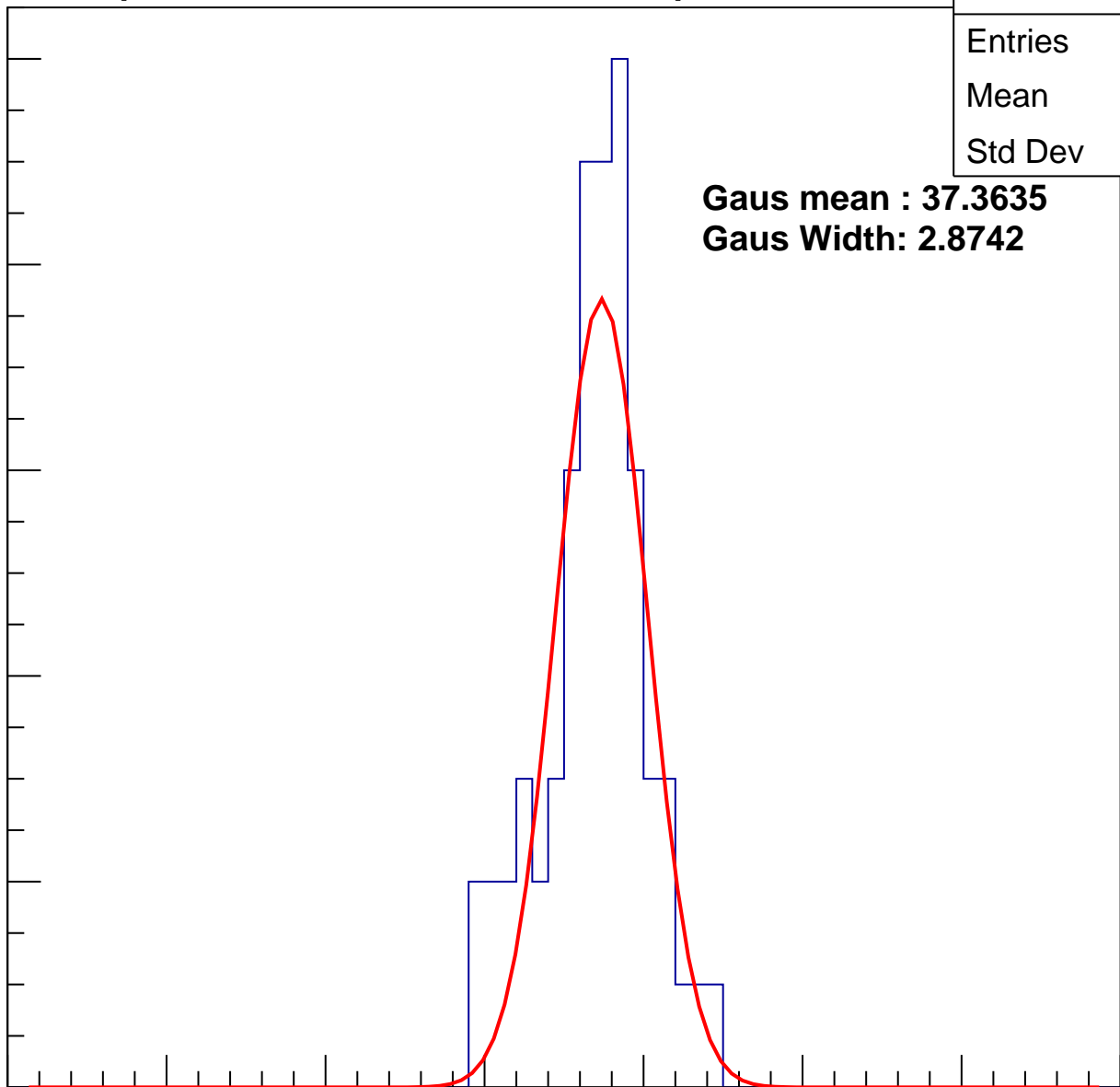
**Gaus Width: 2.8742**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B0L002S, U2-ch34, adc2

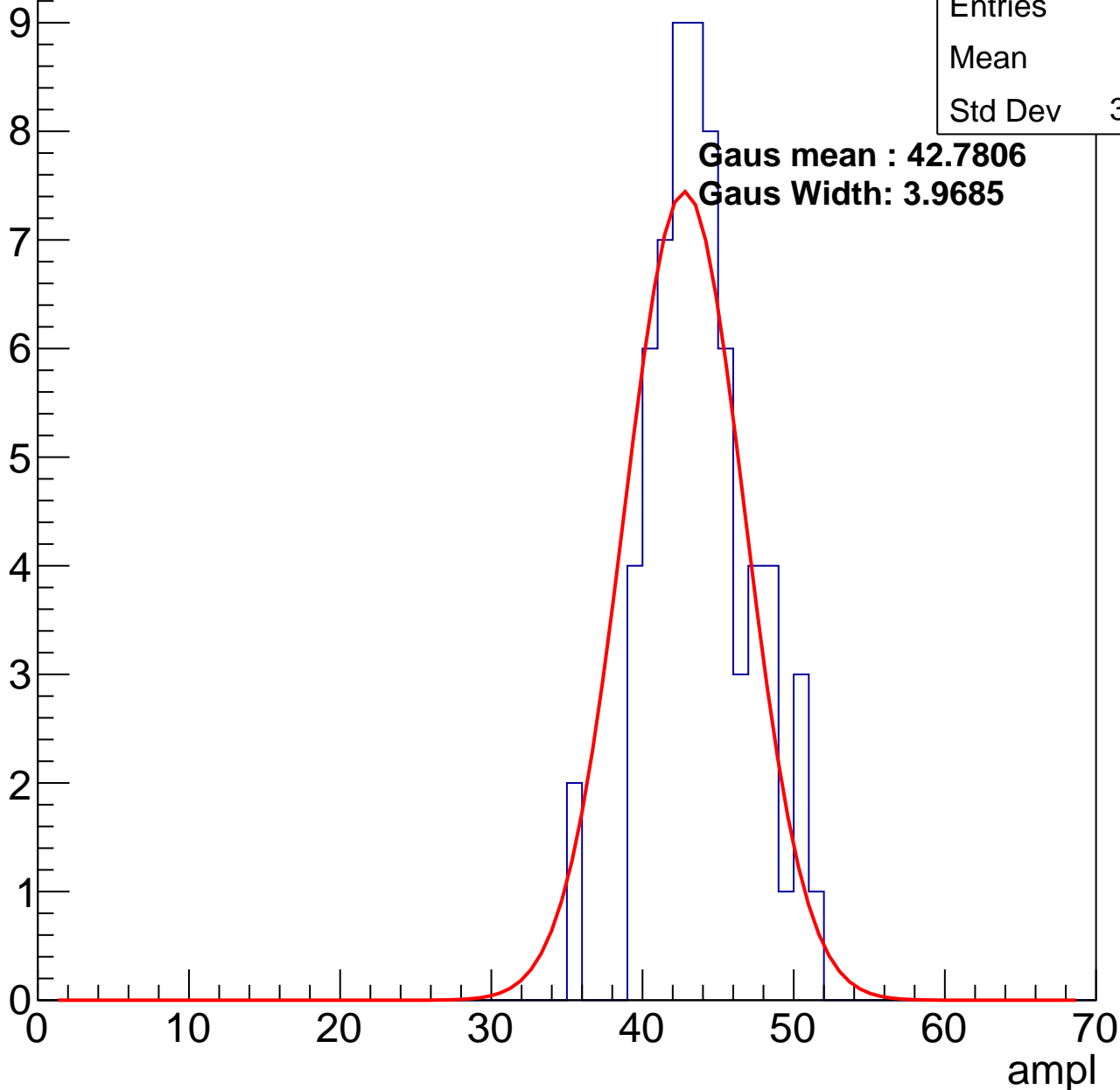
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	67
Mean	43.4
Std Dev	3.328

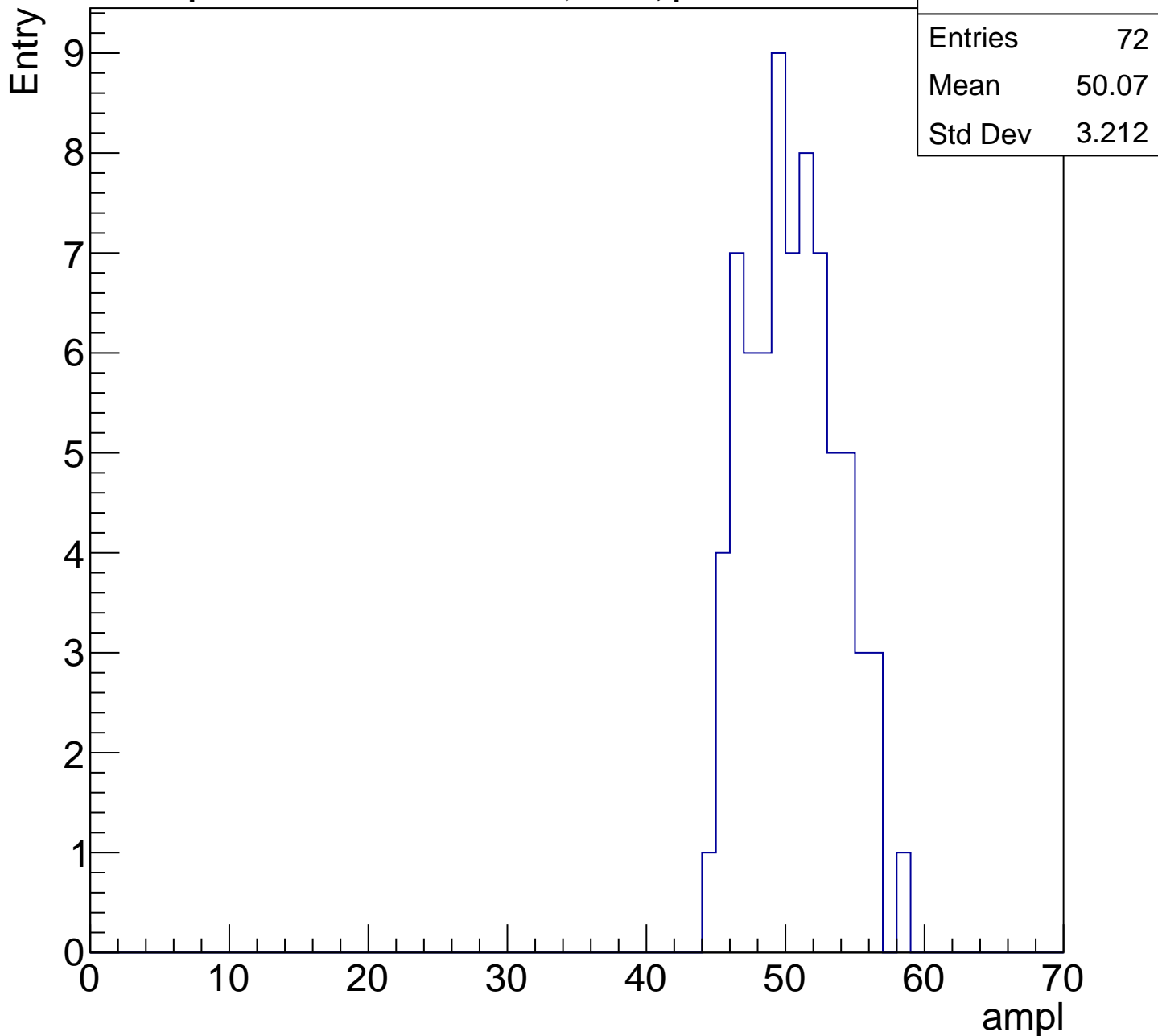
**Gaus mean : 42.7806**

**Gaus Width: 3.9685**



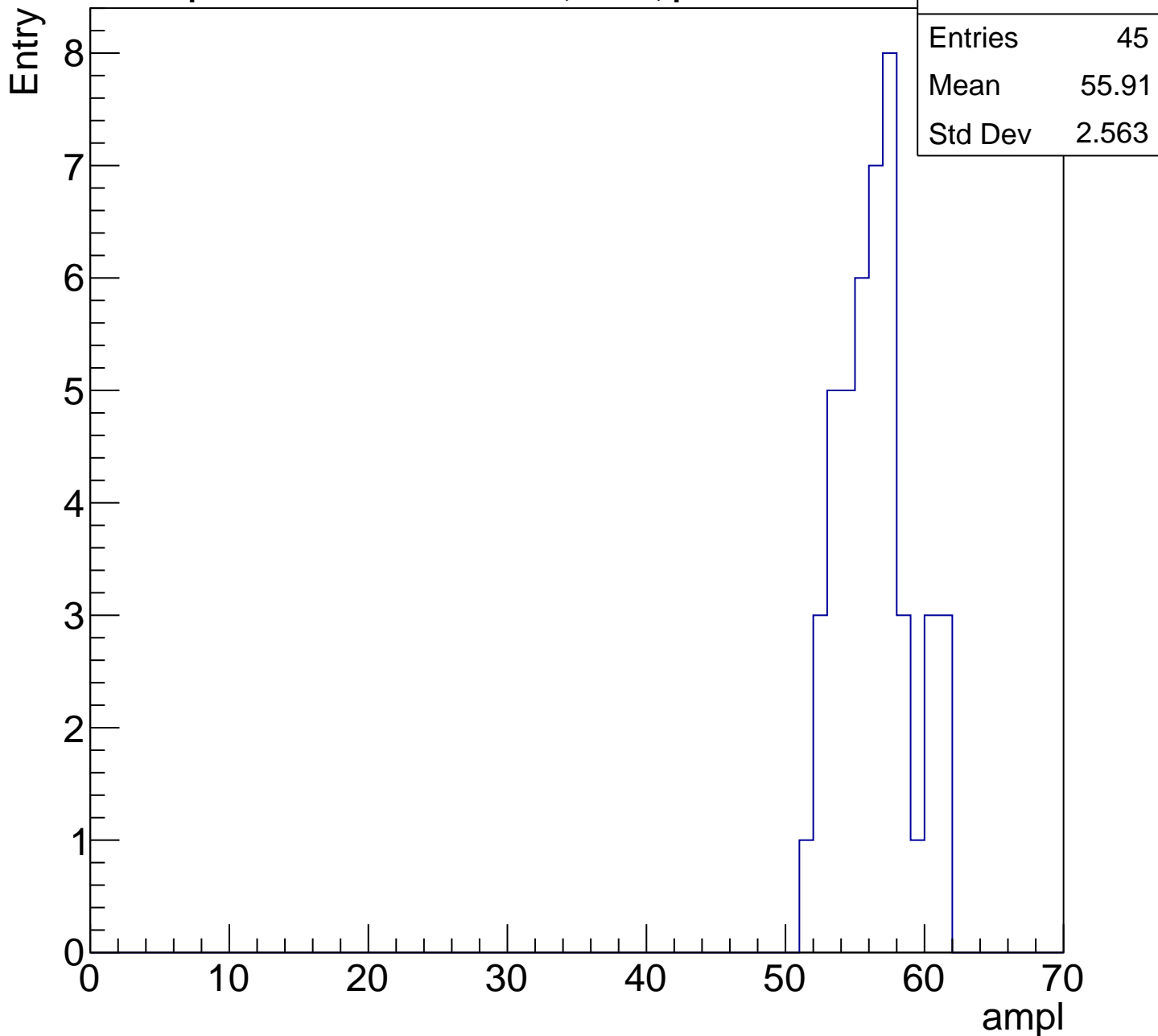
# B0L002S, U2-ch34, adc3

calib\_packv5\_042523\_0143.root, FC#8, port C1



# B0L002S, U2-ch34, adc4

calib\_packv5\_042523\_0143.root, FC#8, port C1



# B0L002S, U2-ch34, adc5

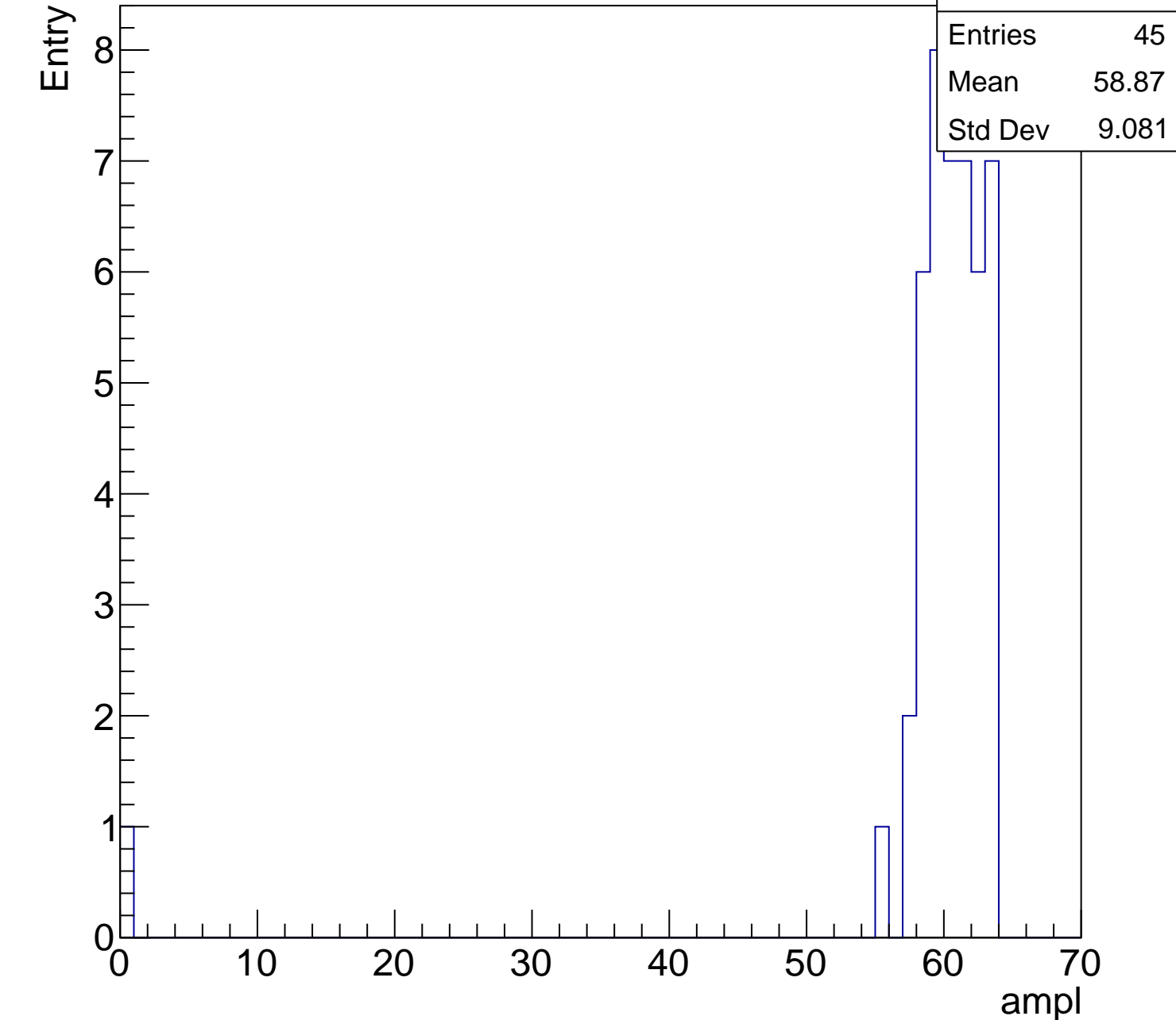
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	45
Mean	58.87
Std Dev	9.081

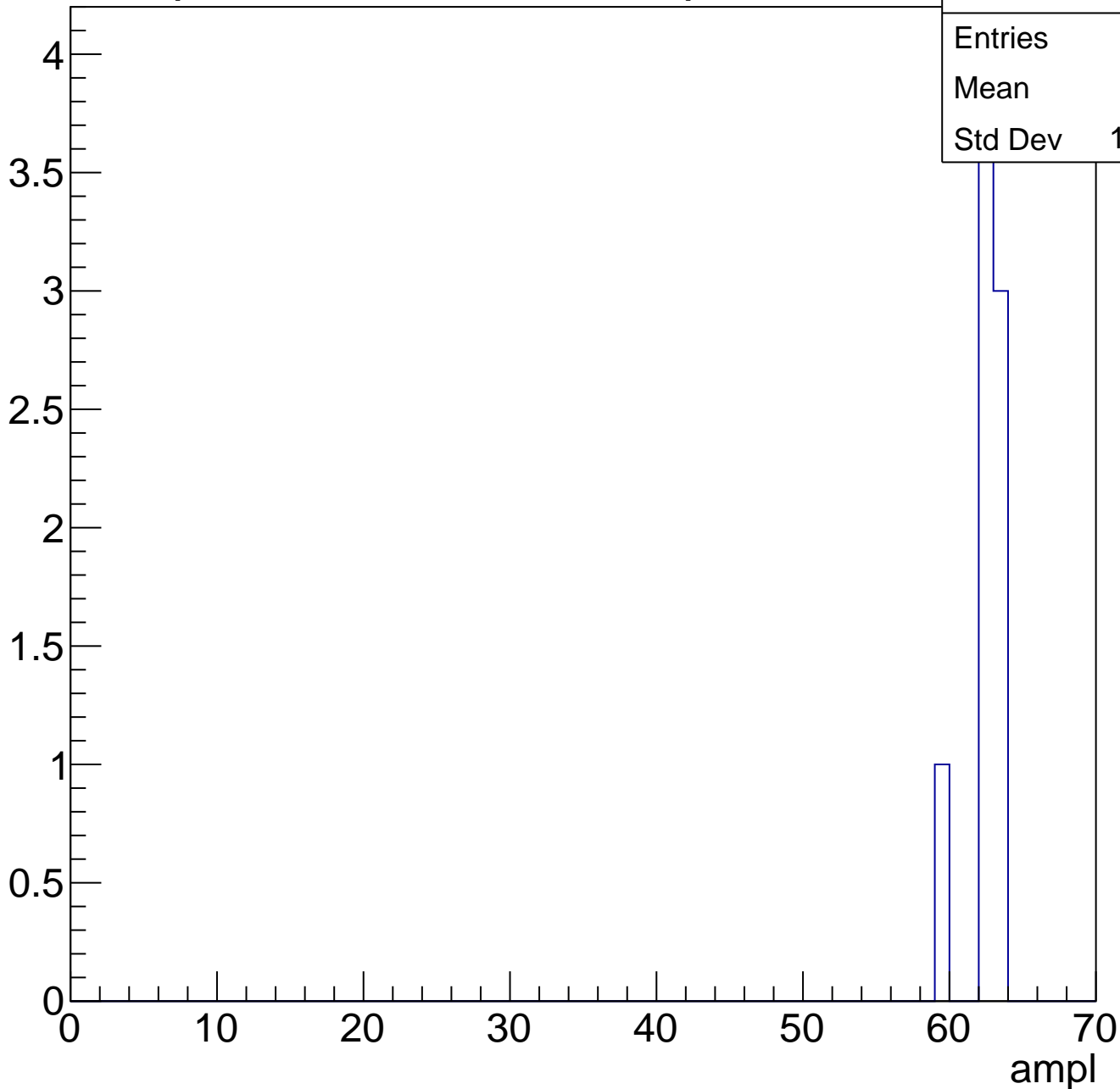
ampl



# B0L002S, U2-ch34, adc6

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry





# B0L002S, U2-ch34, adc7

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



Entries	3
Mean	7.667
Std Dev	10.84

# B0L002S, U2-ch35, adc0

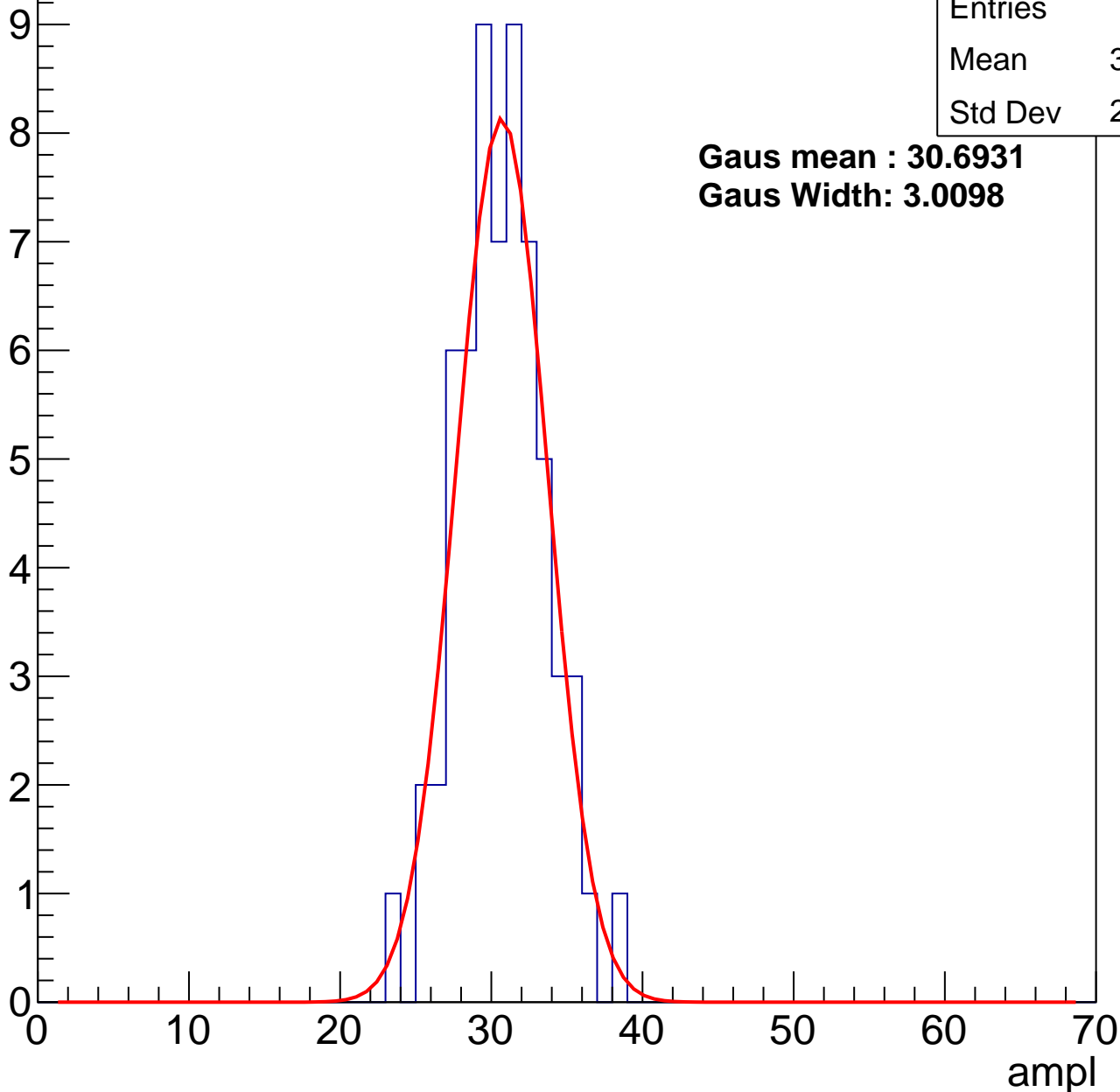
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	62
Mean	30.24
Std Dev	2.894

**Gaus mean : 30.6931**

**Gaus Width: 3.0098**



# B0L002S, U2-ch35, adc1

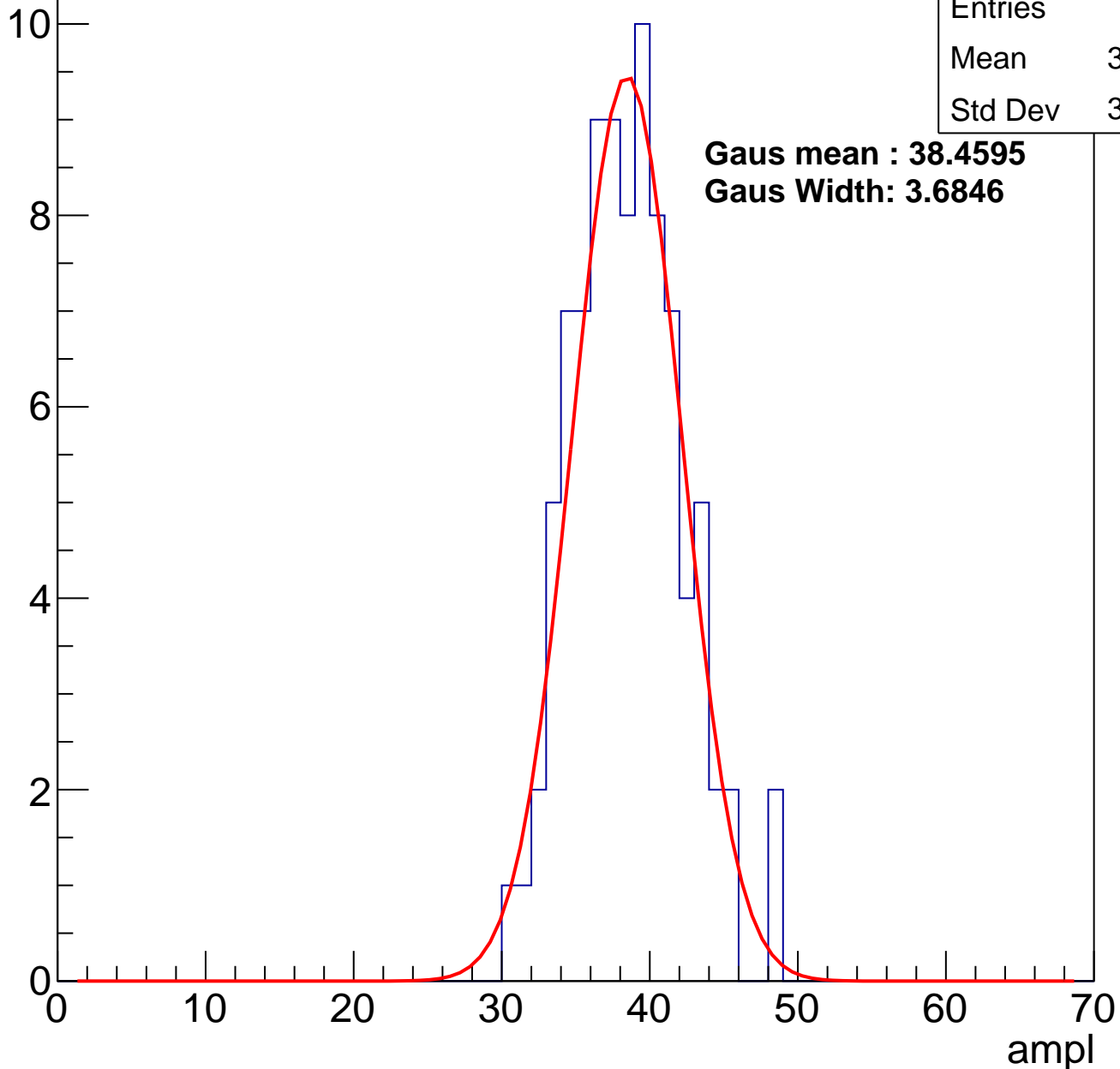
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entries	89
Mean	38.07
Std Dev	3.662

**Gaus mean : 38.4595**

**Gaus Width: 3.6846**

Entry



# B0L002S, U2-ch35, adc2

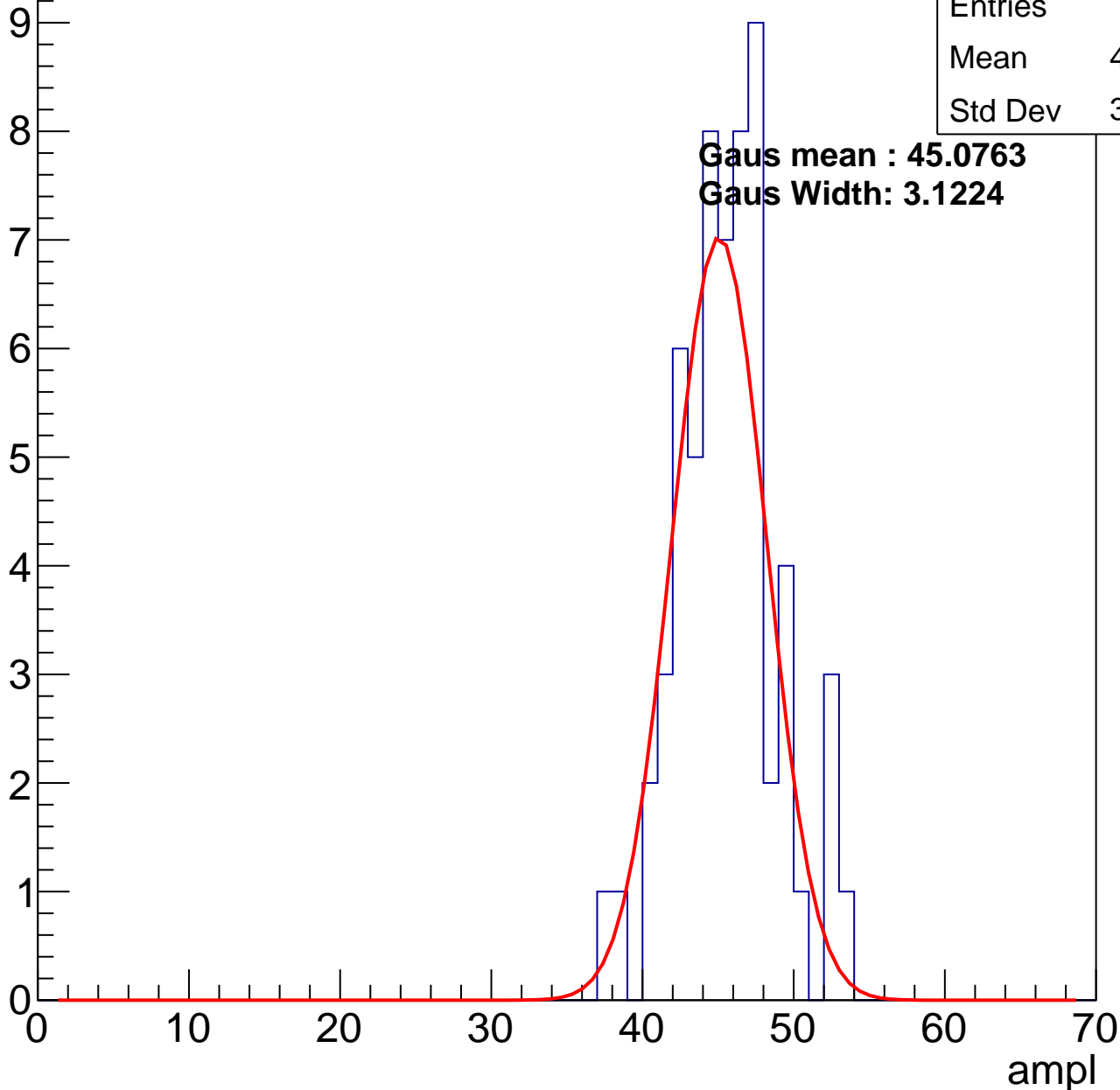
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	61
Mean	45.15
Std Dev	3.274

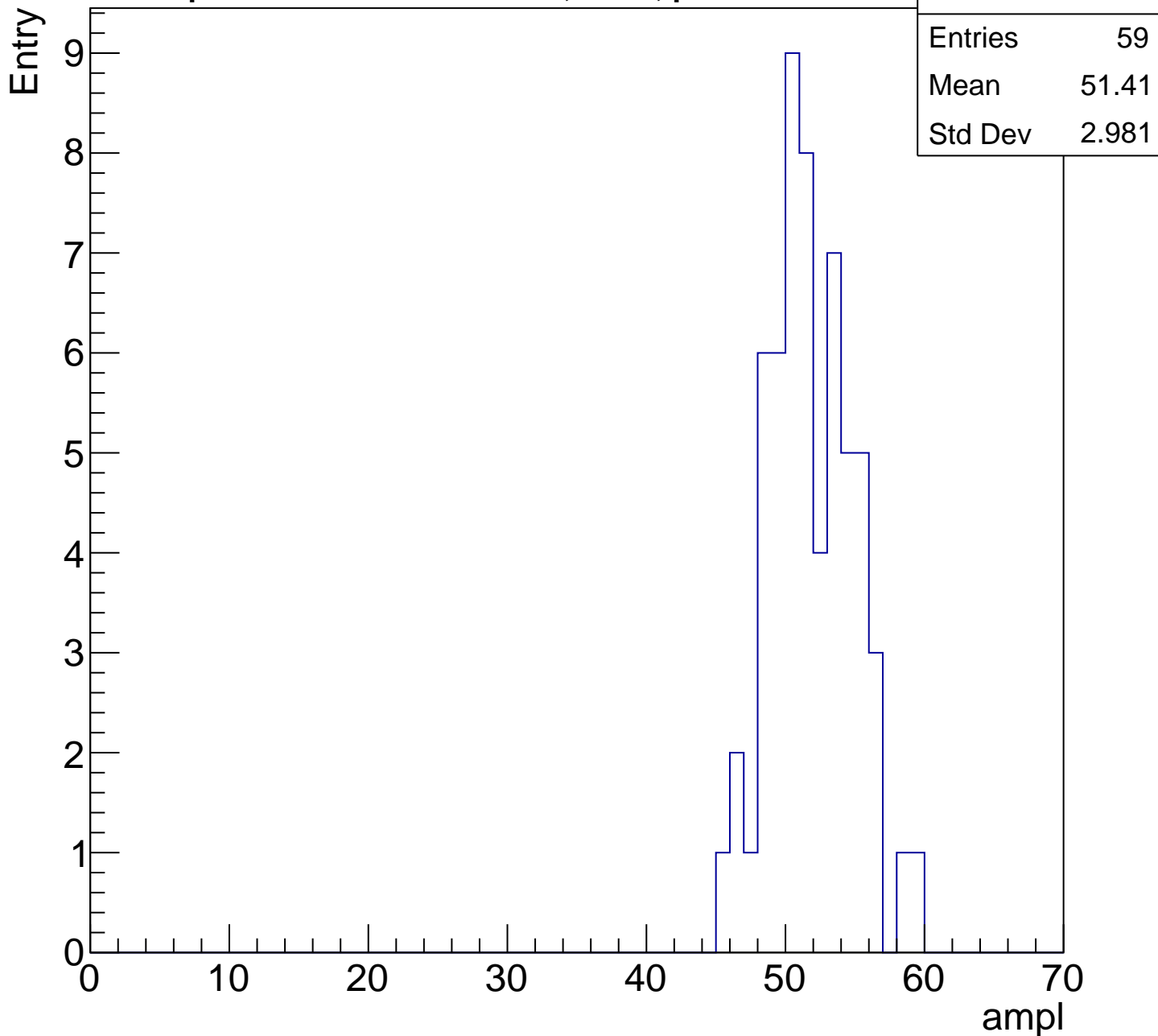
**Gaus mean : 45.0763**

**Gaus Width: 3.1224**



# B0L002S, U2-ch35, adc3

calib\_packv5\_042523\_0143.root, FC#8, port C1

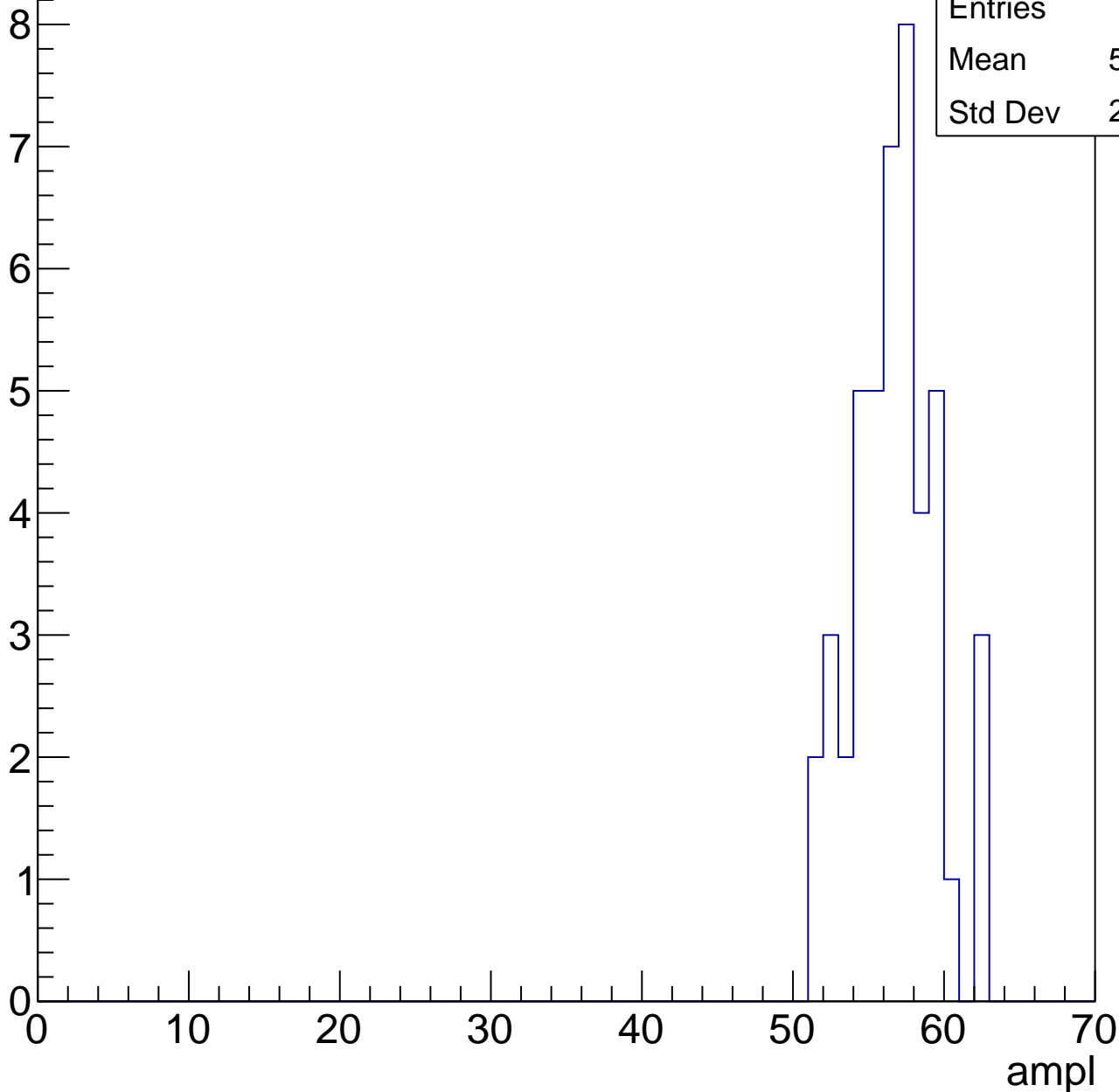


# B0L002S, U2-ch35, adc4

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	45
Mean	56.22
Std Dev	2.715



# B0L002S, U2-ch35, adc5

calib\_packv5\_042523\_0143.root, FC#8, port C1

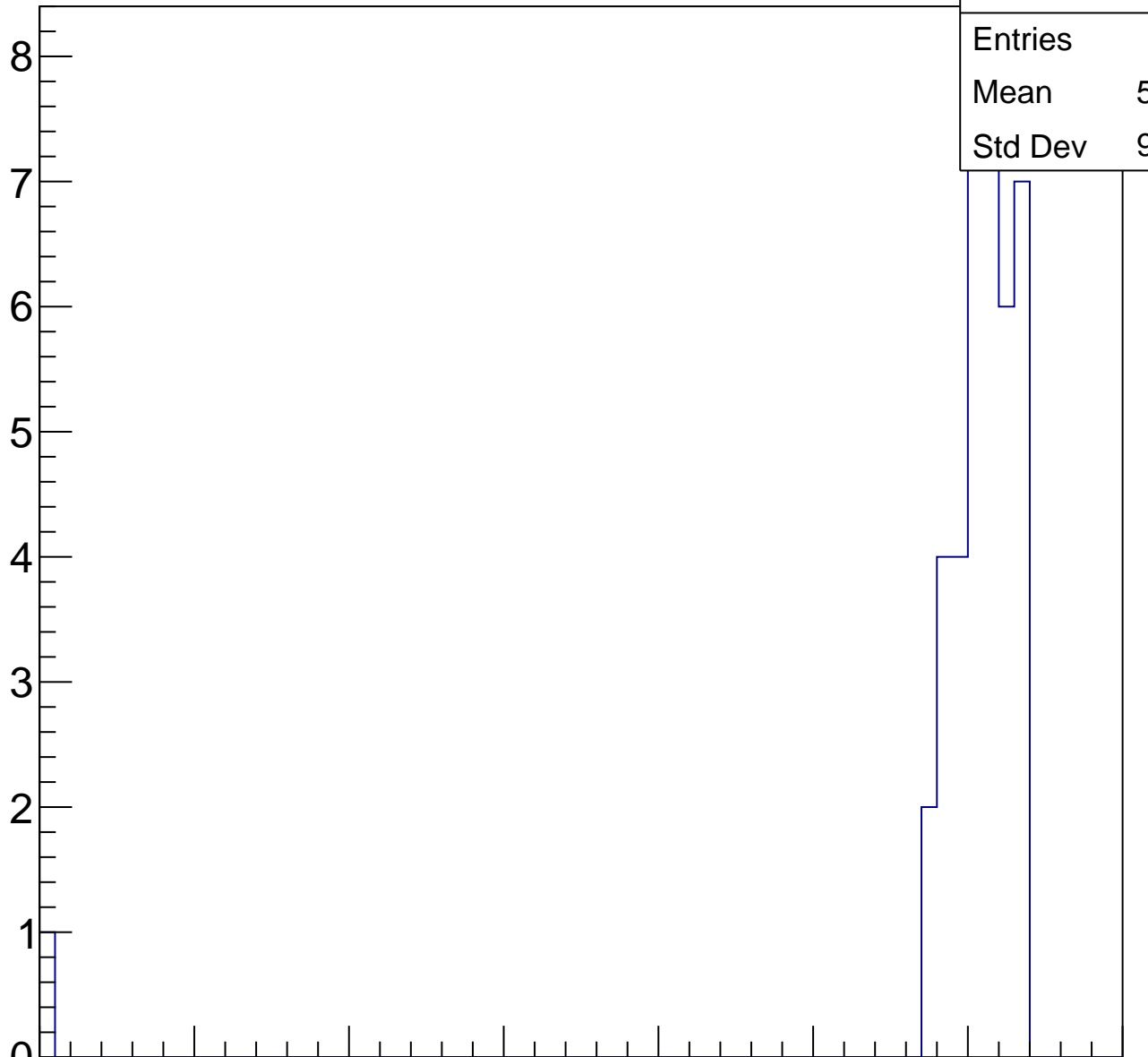
Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	40
Mean	59.08
Std Dev	9.616

ampl

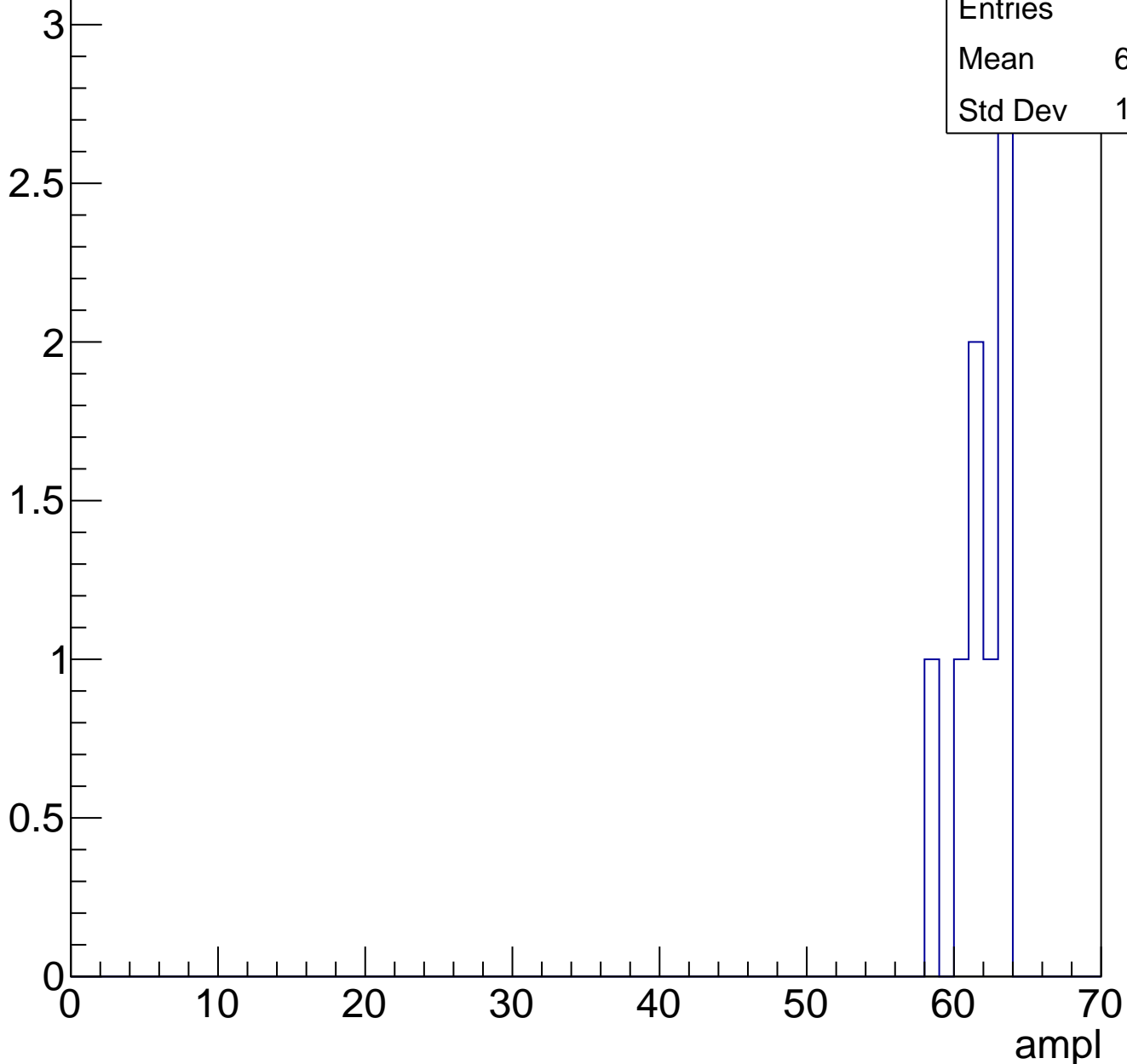
0 10 20 30 40 50 60 70



# B0L002S, U2-ch35, adc6

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry





# B0L002S, U2-ch35, adc7

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



# B0L002S, U2-ch36, adc0

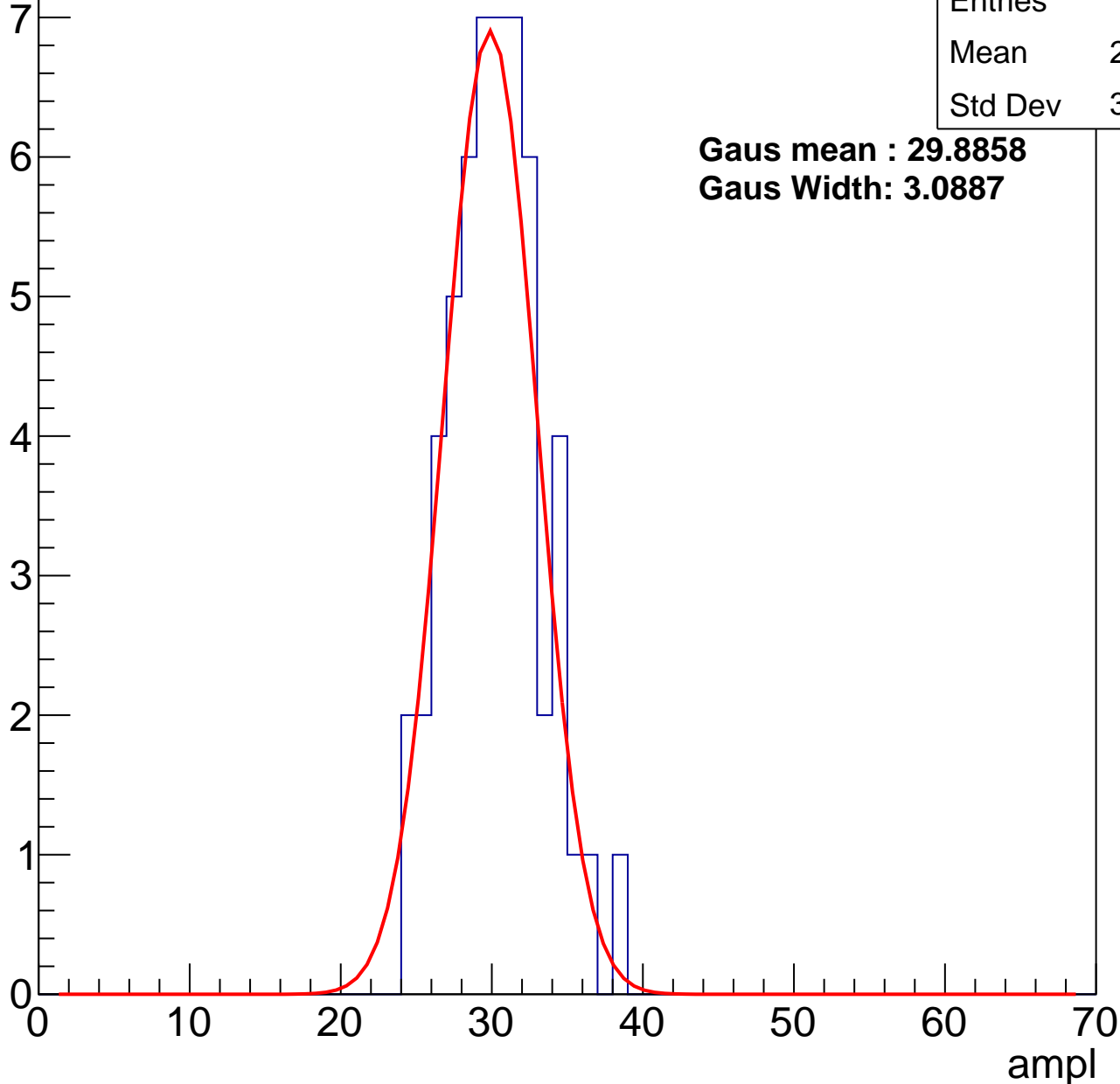
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	55
Mean	29.78
Std Dev	3.007

**Gaus mean : 29.8858**

**Gaus Width: 3.0887**



# B0L002S, U2-ch36, adc1

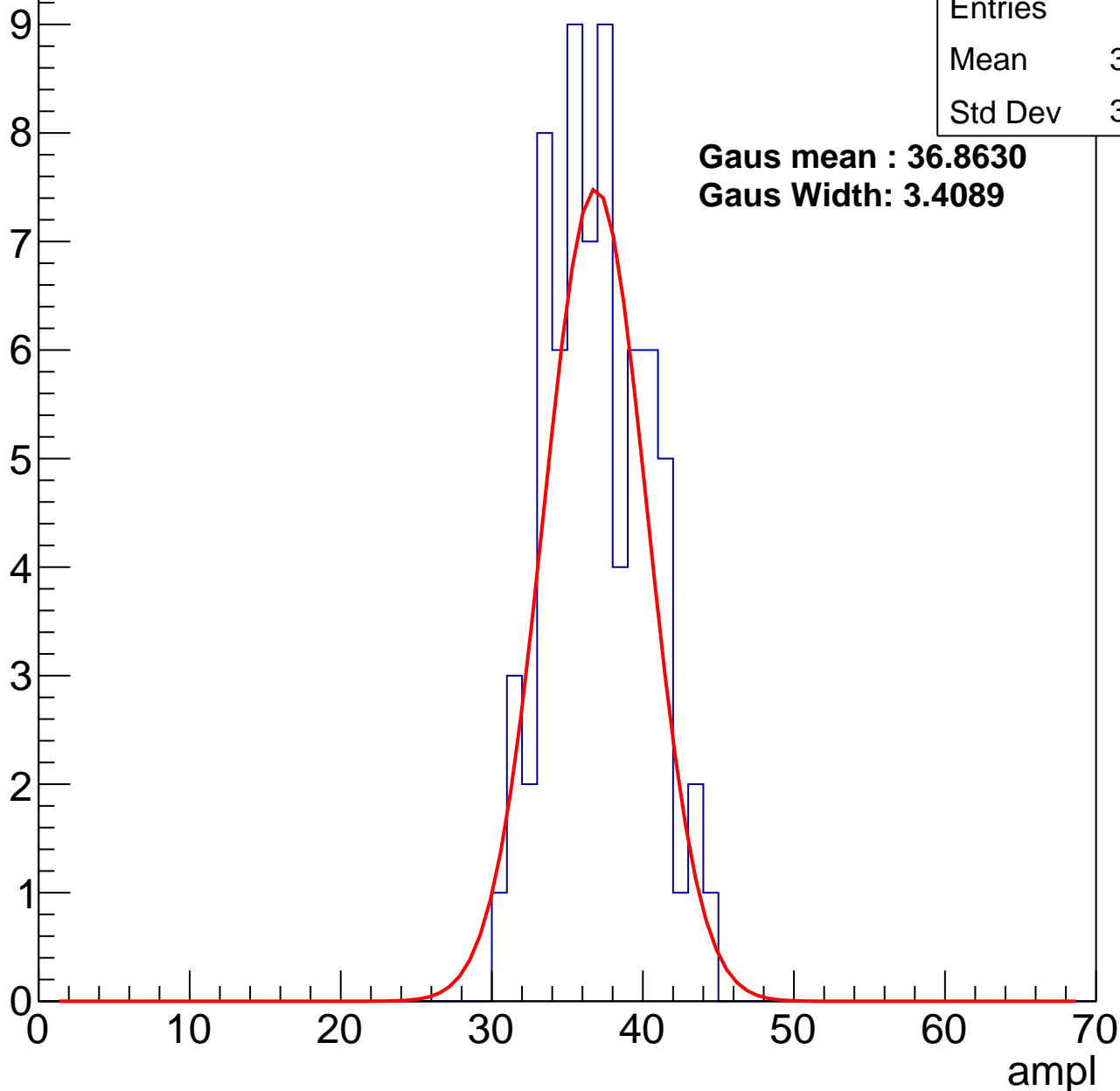
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	70
Mean	36.54
Std Dev	3.219

**Gaus mean : 36.8630**

**Gaus Width: 3.4089**



# B0L002S, U2-ch36, adc2

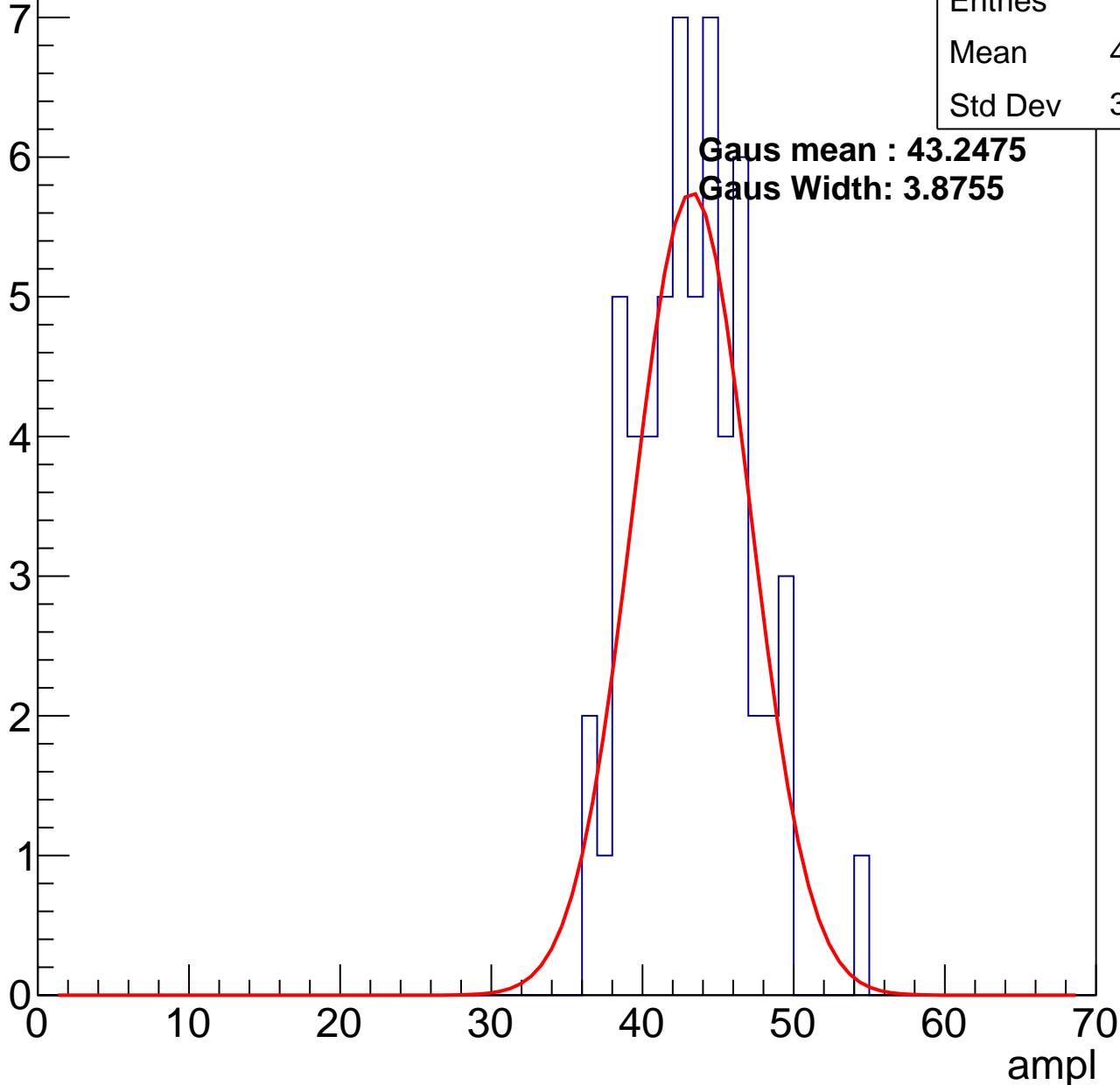
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	58
Mean	42.83
Std Dev	3.649

**Gaus mean : 43.2475**

**Gaus Width: 3.8755**

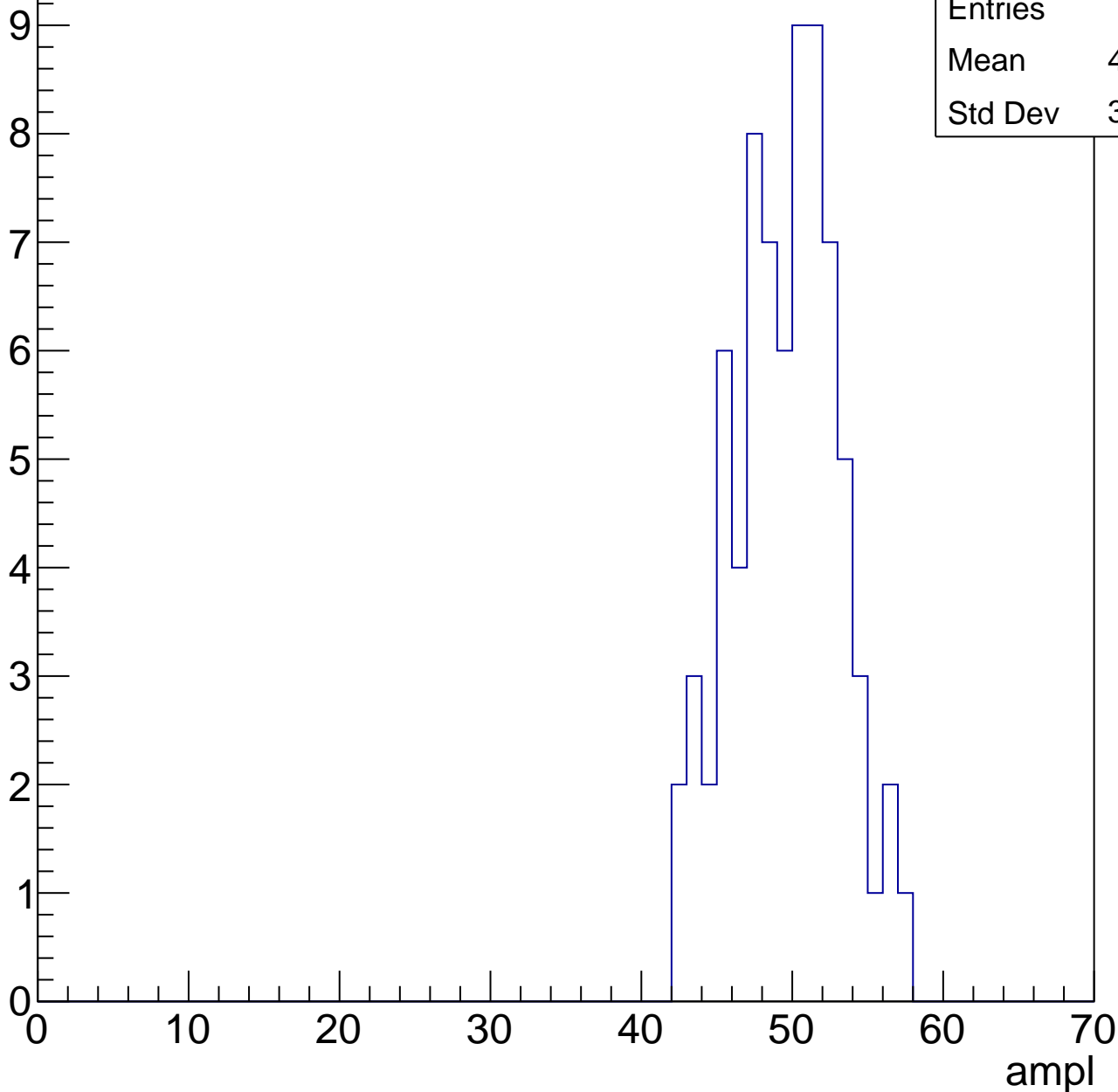


# B0L002S, U2-ch36, adc3

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	75
Mean	49.13
Std Dev	3.438

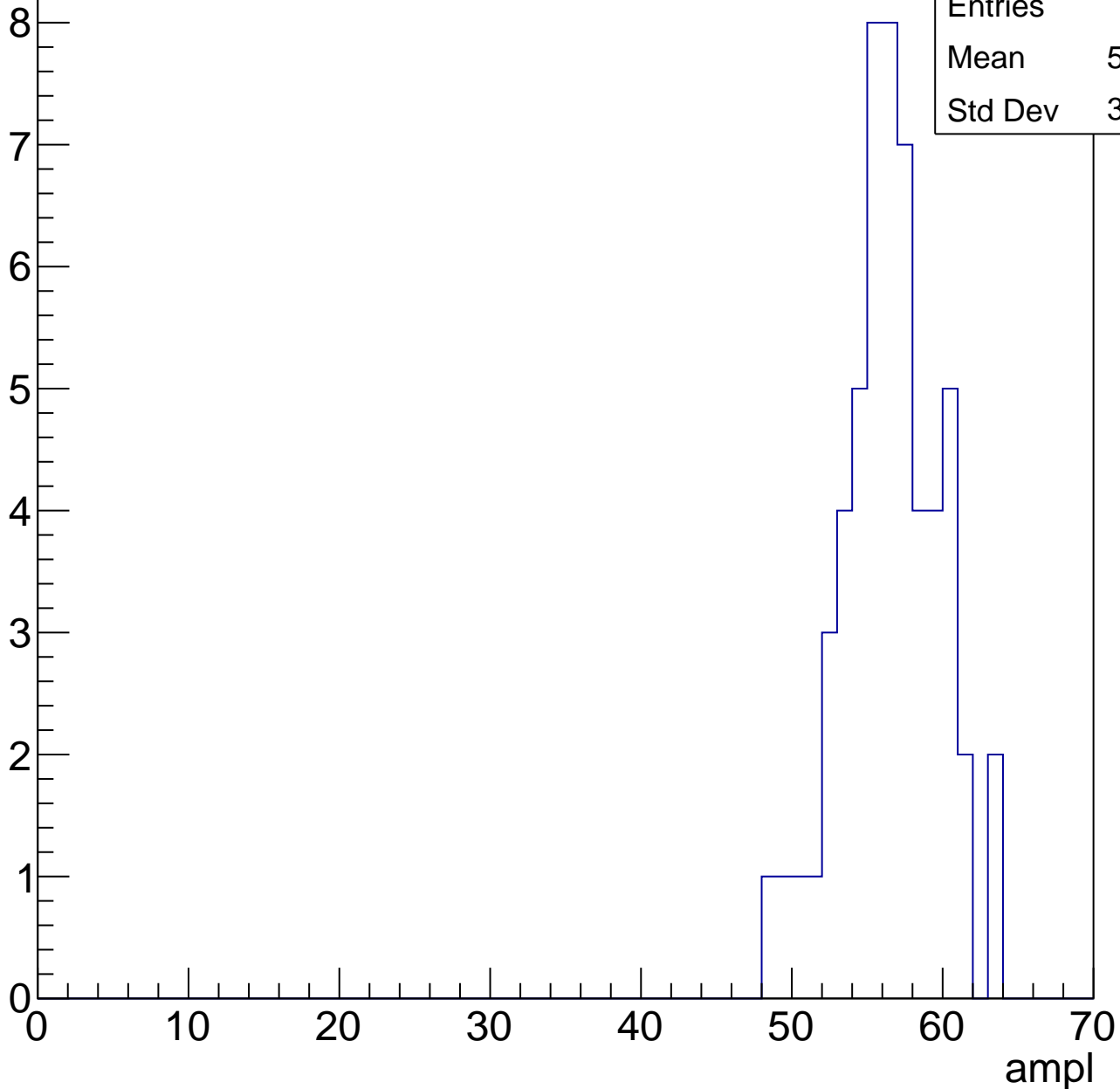


# B0L002S, U2-ch36, adc4

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	56
Mean	56.05
Std Dev	3.198

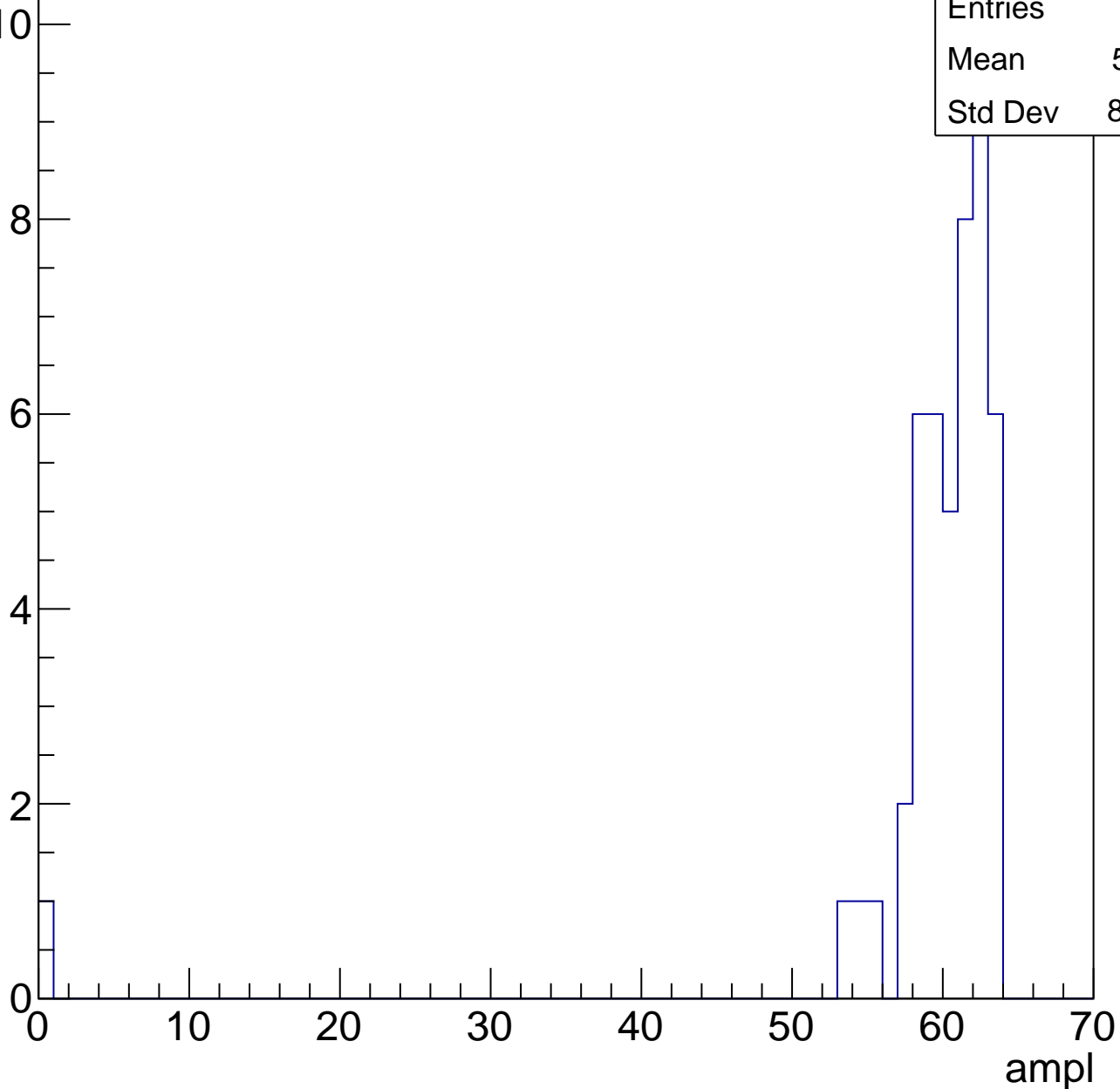


# B0L002S, U2-ch36, adc5

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	47
Mean	58.81
Std Dev	8.984



# B0L002S, U2-ch36, adc6

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry





# B0L002S, U2-ch36, adc7

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L002S, U2-ch37, adc0

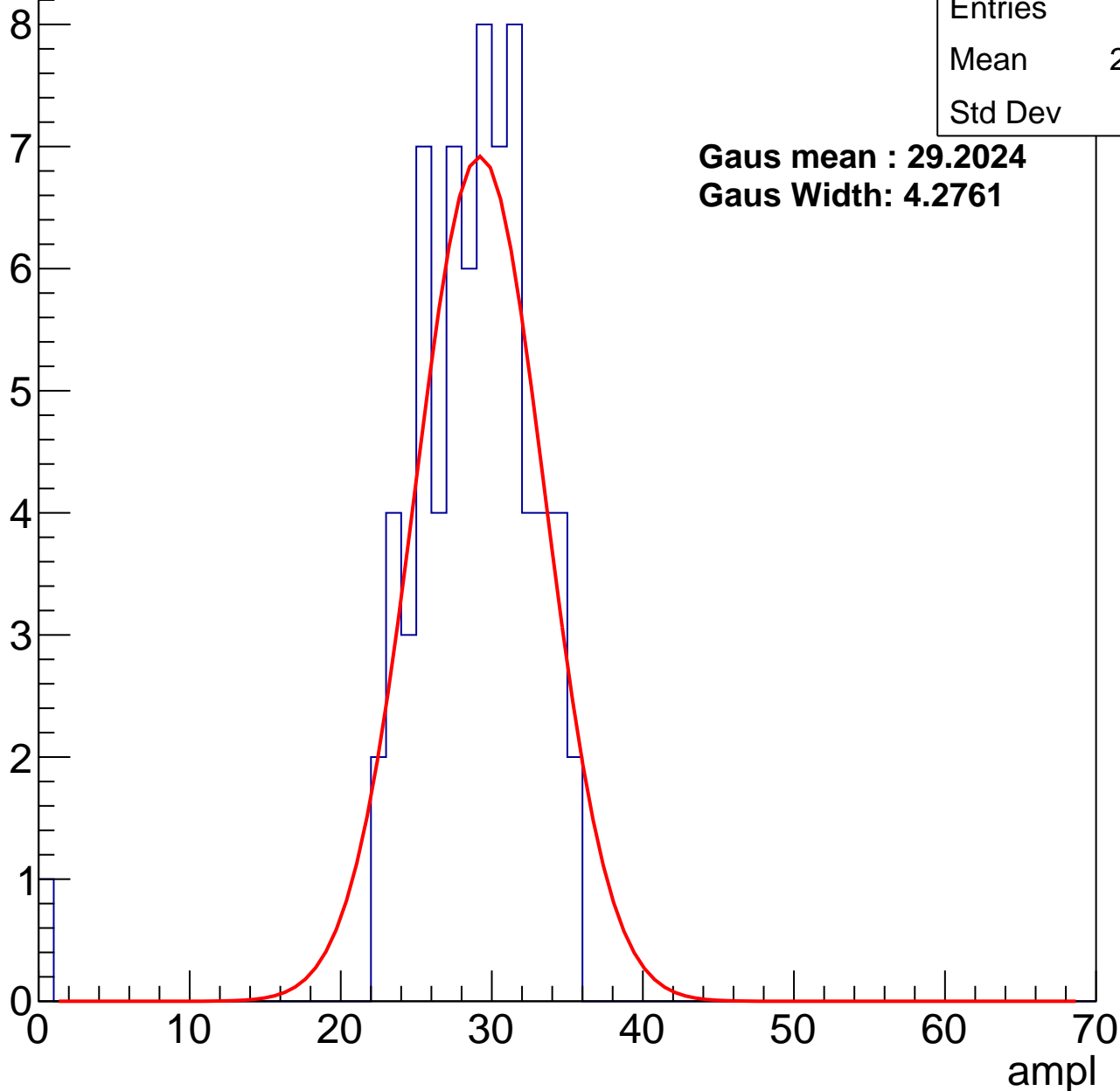
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	71
Mean	28.17
Std Dev	4.75

**Gaus mean : 29.2024**

**Gaus Width: 4.2761**



# B0L002S, U2-ch37, adc1

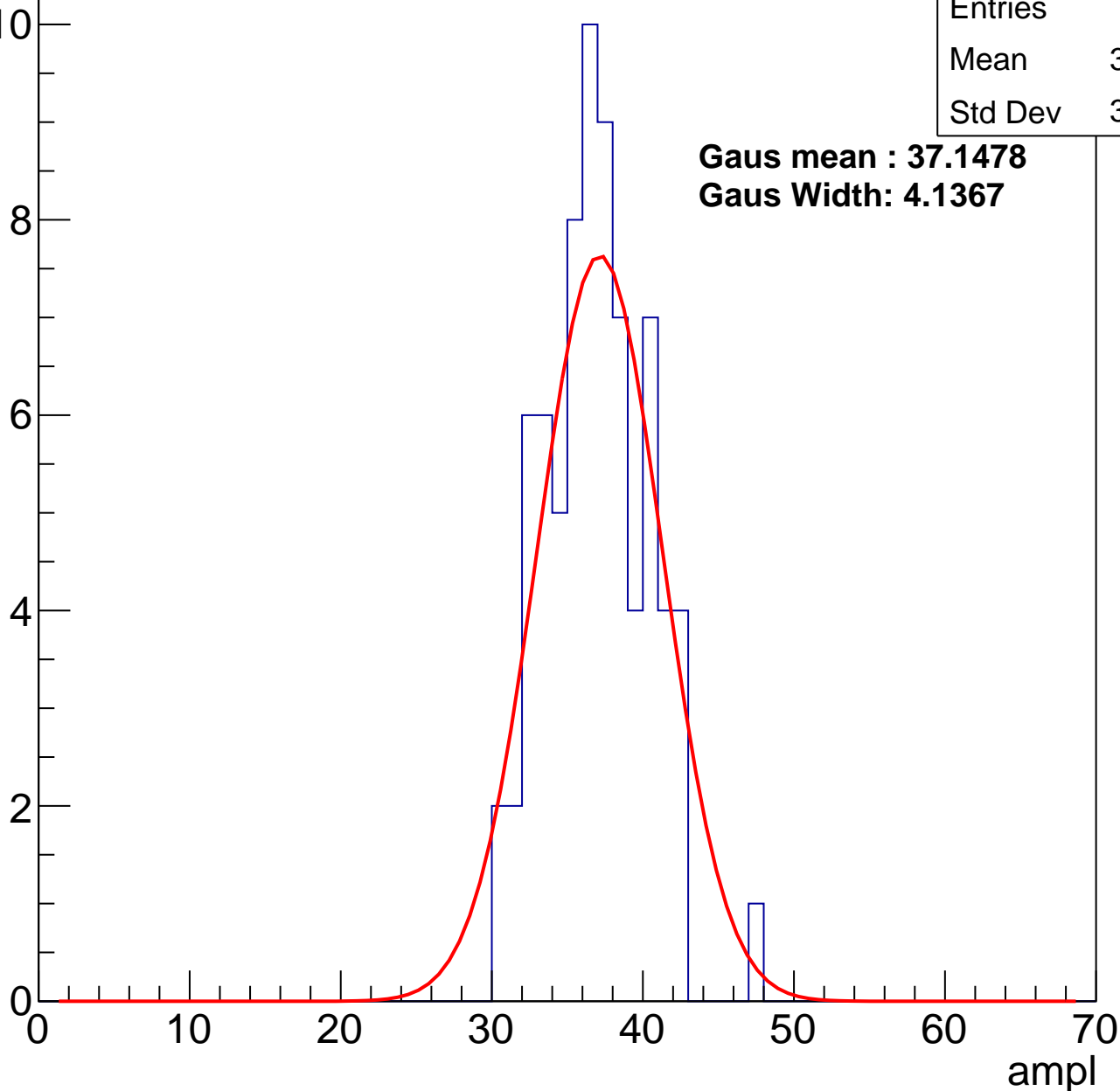
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	75
Mean	36.48
Std Dev	3.332

**Gaus mean : 37.1478**

**Gaus Width: 4.1367**



# B0L002S, U2-ch37, adc2

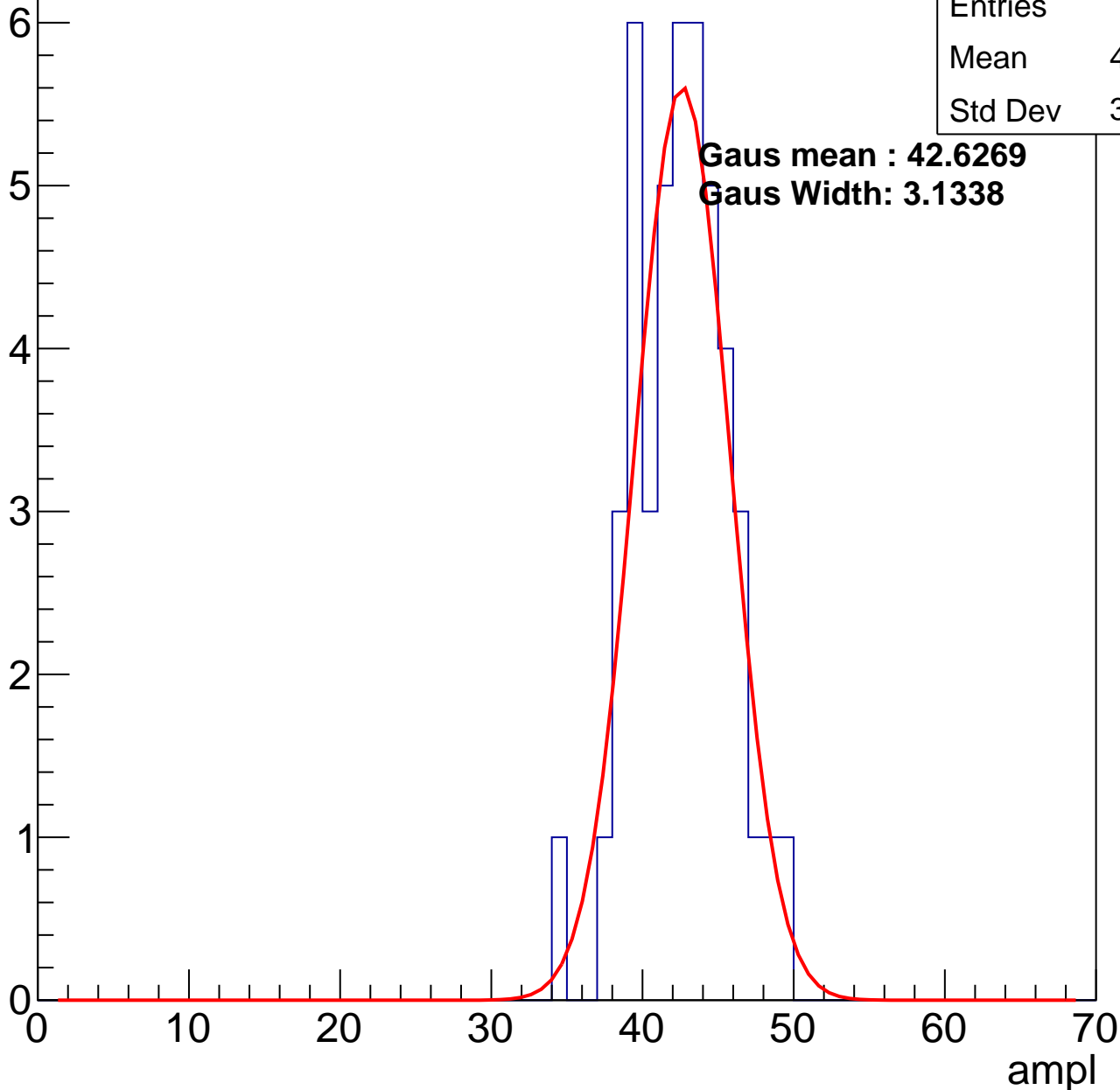
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	46
Mean	42.09
Std Dev	3.049

**Gaus mean : 42.6269**

**Gaus Width: 3.1338**

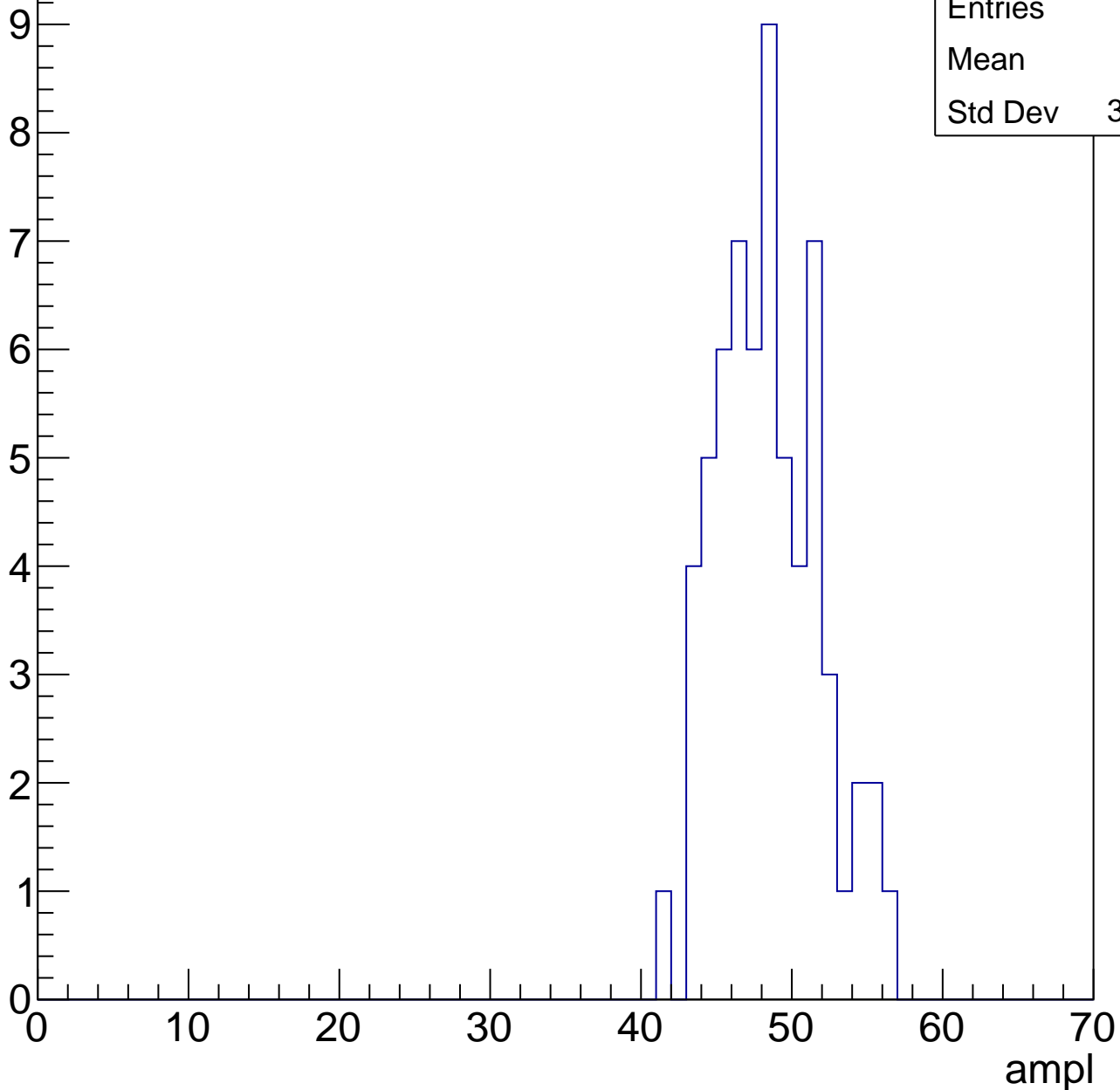


# B0L002S, U2-ch37, adc3

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	63
Mean	48
Std Dev	3.352

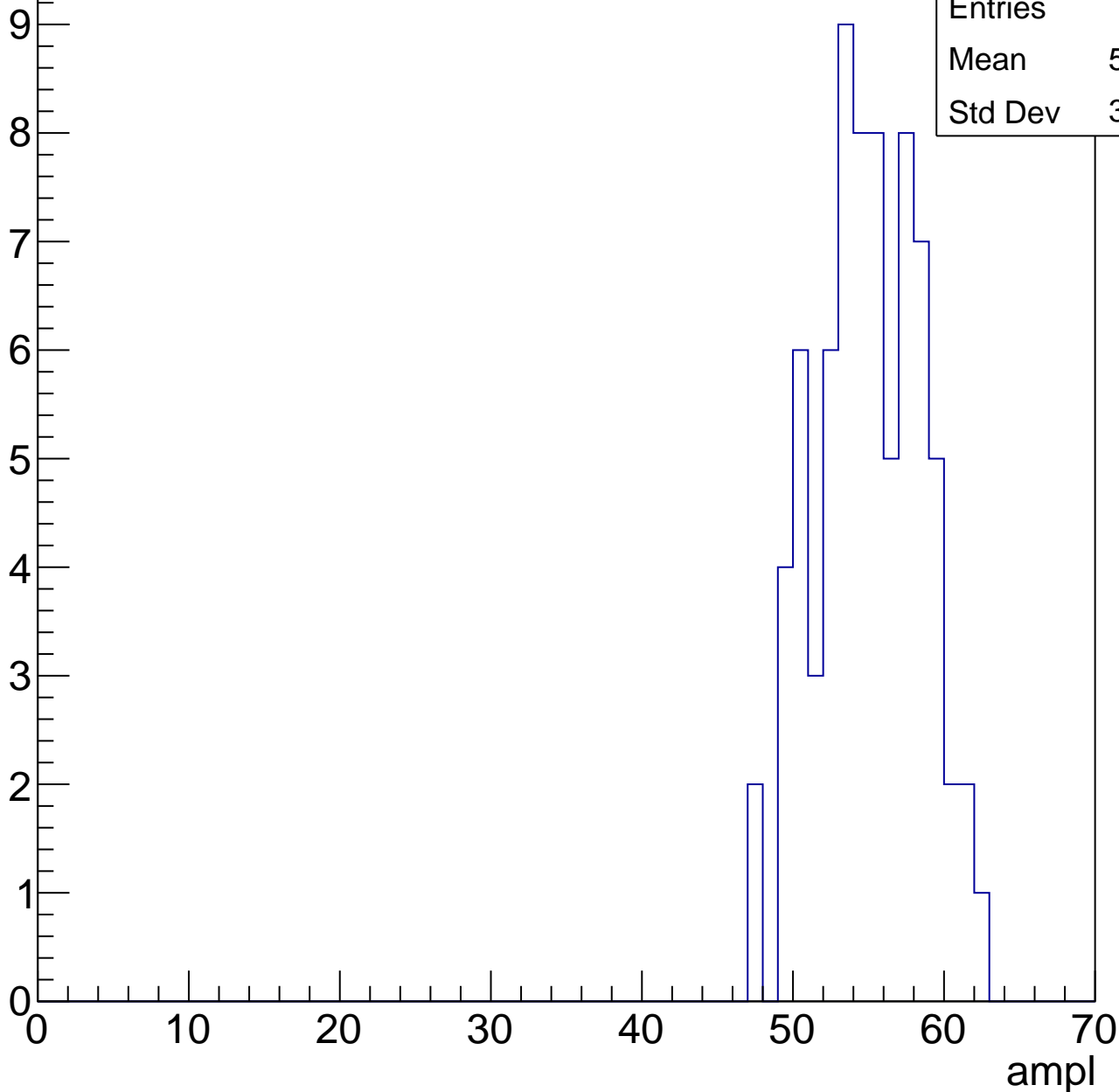


# B0L002S, U2-ch37, adc4

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	76
Mean	54.54
Std Dev	3.447

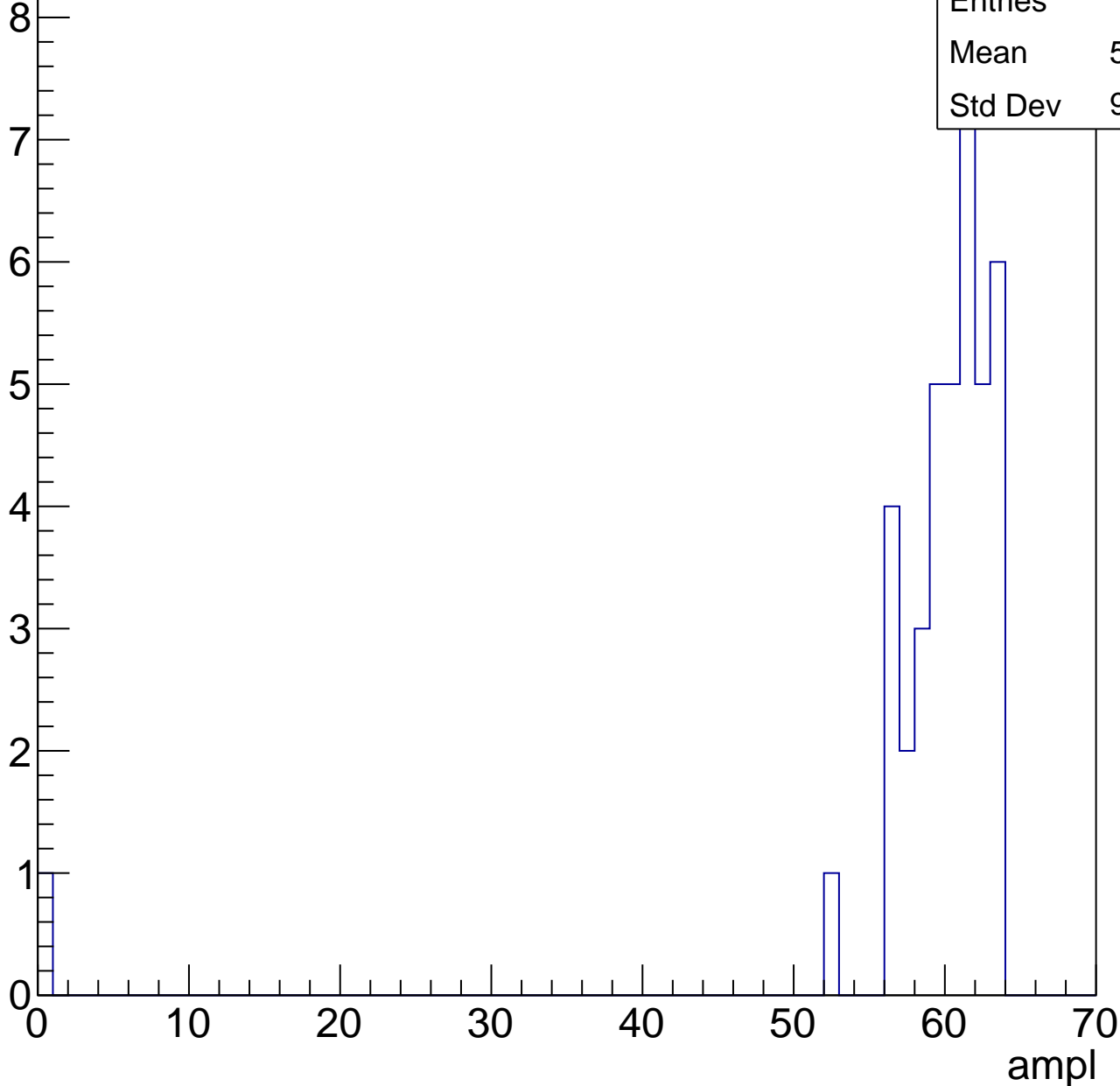


# B0L002S, U2-ch37, adc5

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

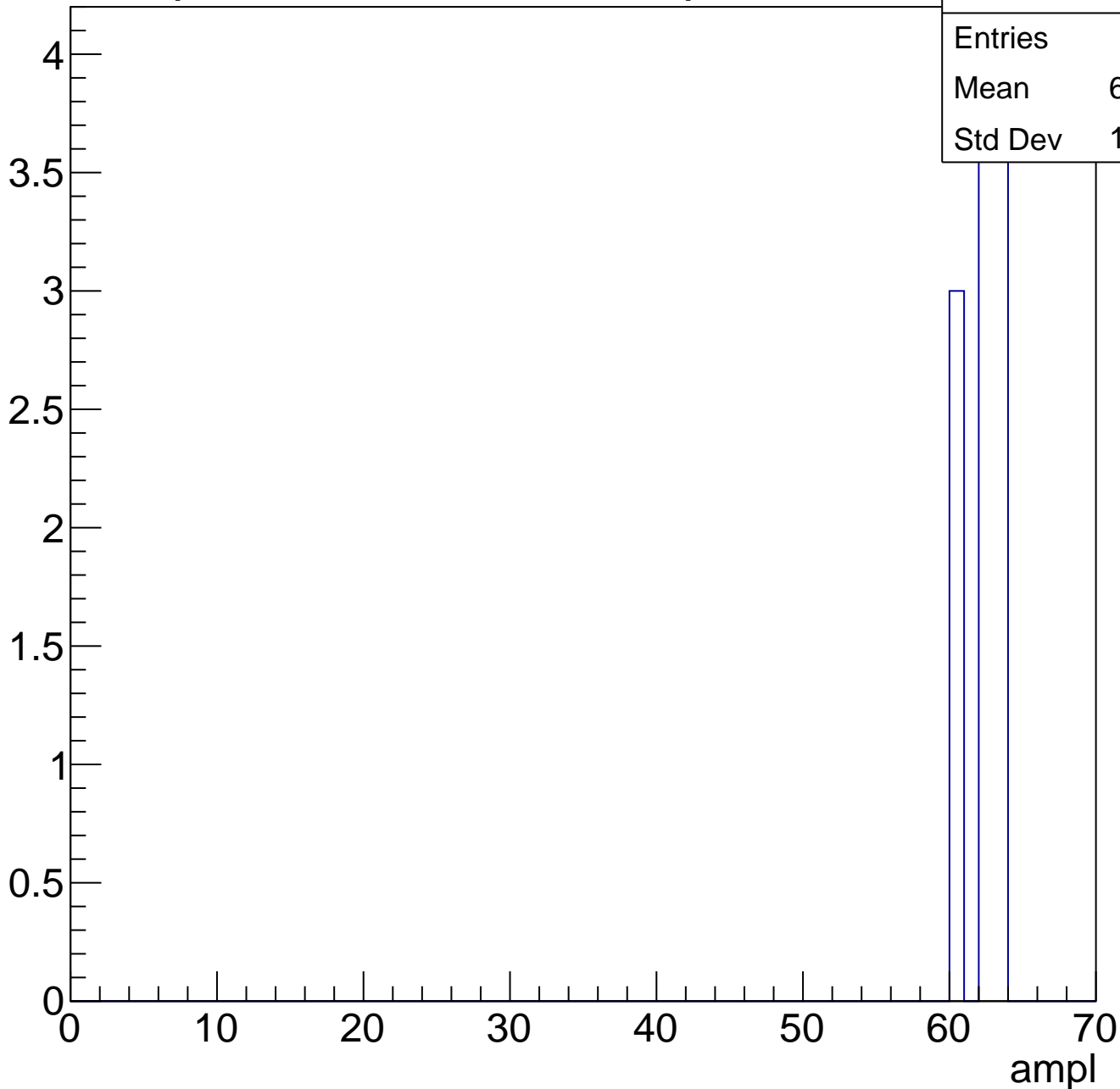
Entries	40
Mean	58.38
Std Dev	9.669



# B0L002S, U2-ch37, adc6

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry





# B0L002S, U2-ch37, adc7

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L002S, U2-ch38, adc0

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entries	76
Mean	29.37
Std Dev	3.52

**Gaus mean : 30.3255**

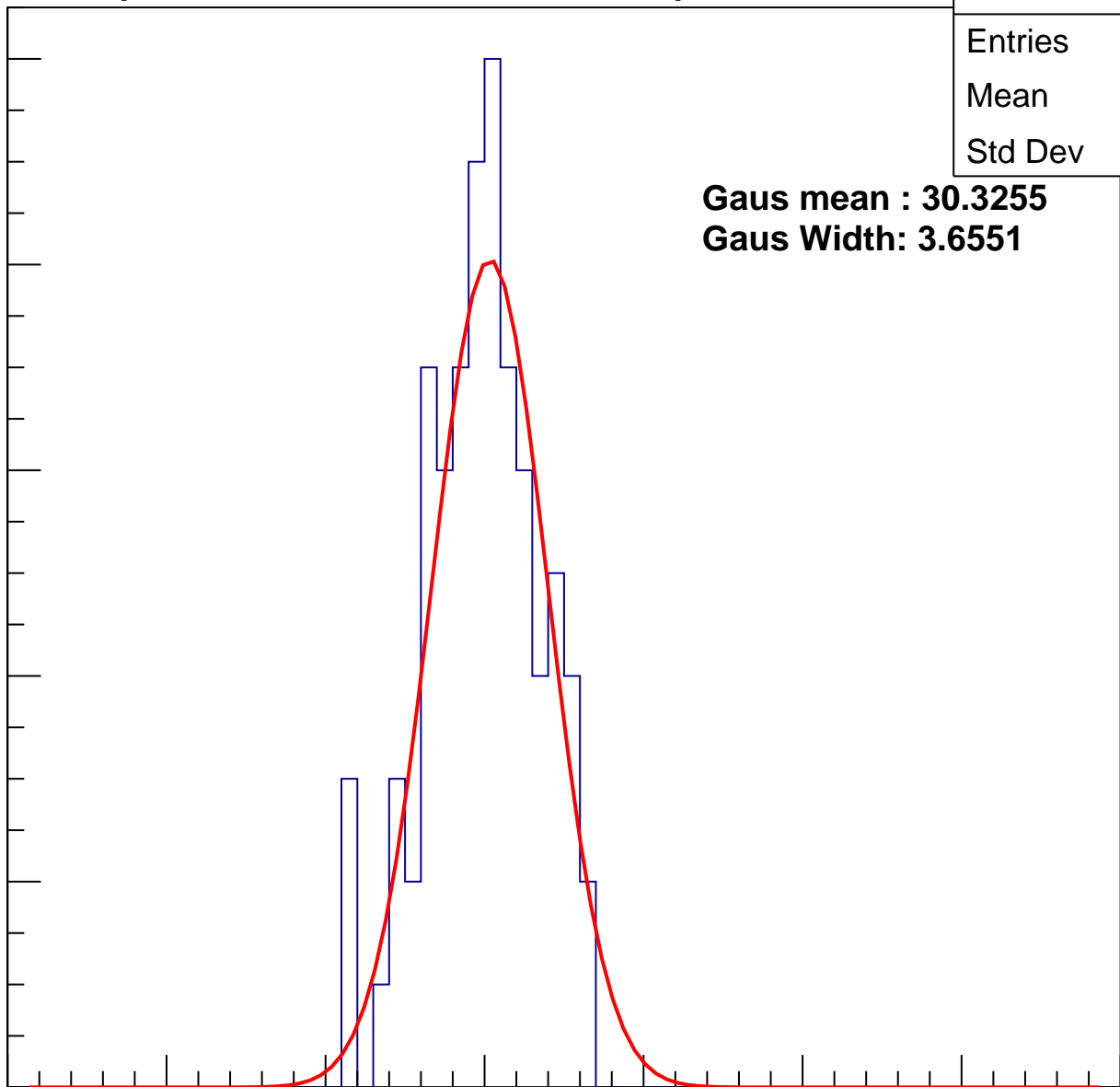
**Gaus Width: 3.6551**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L002S, U2-ch38, adc1

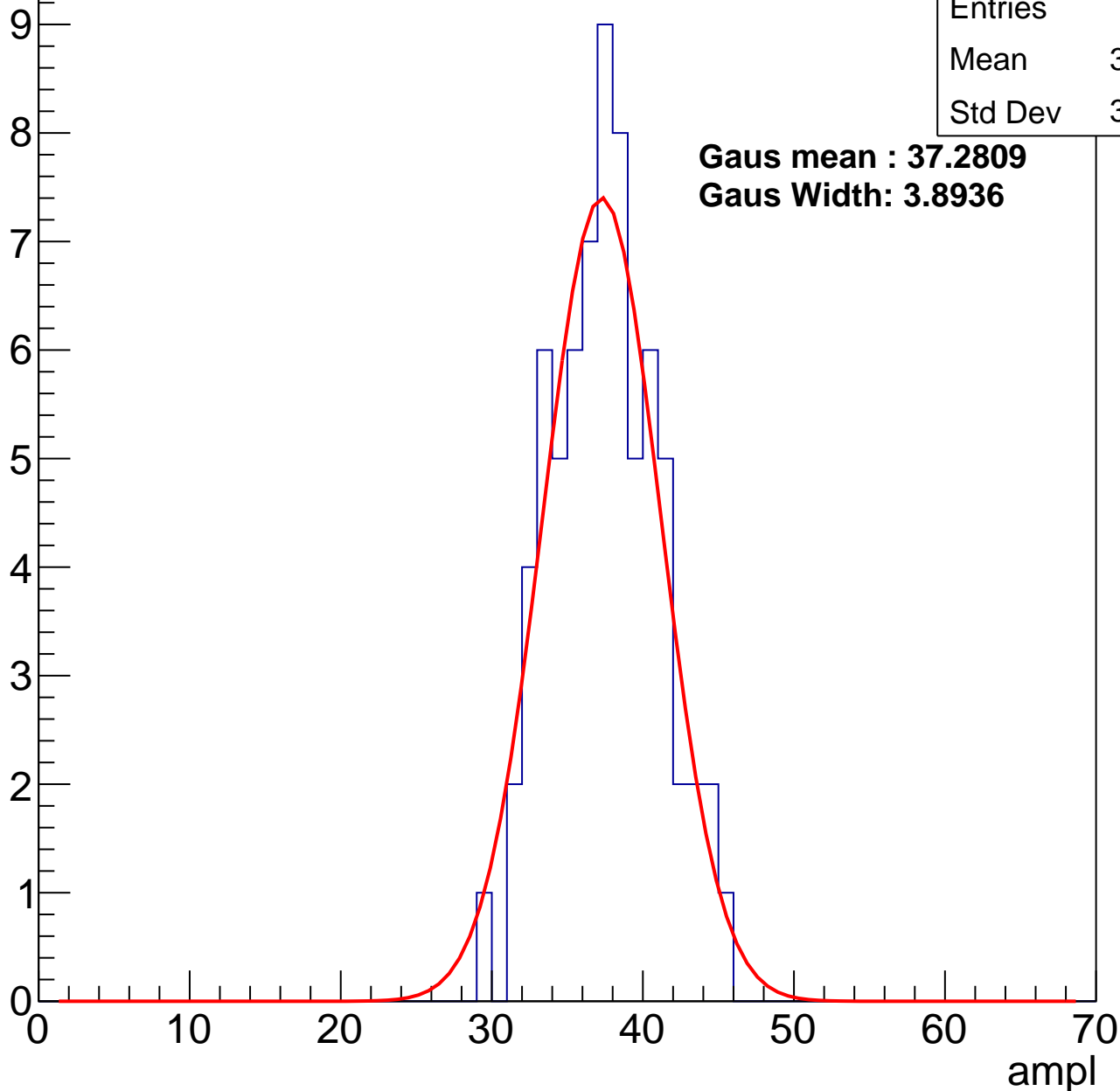
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	71
Mean	37.03
Std Dev	3.468

**Gaus mean : 37.2809**

**Gaus Width: 3.8936**



# B0L002S, U2-ch38, adc2

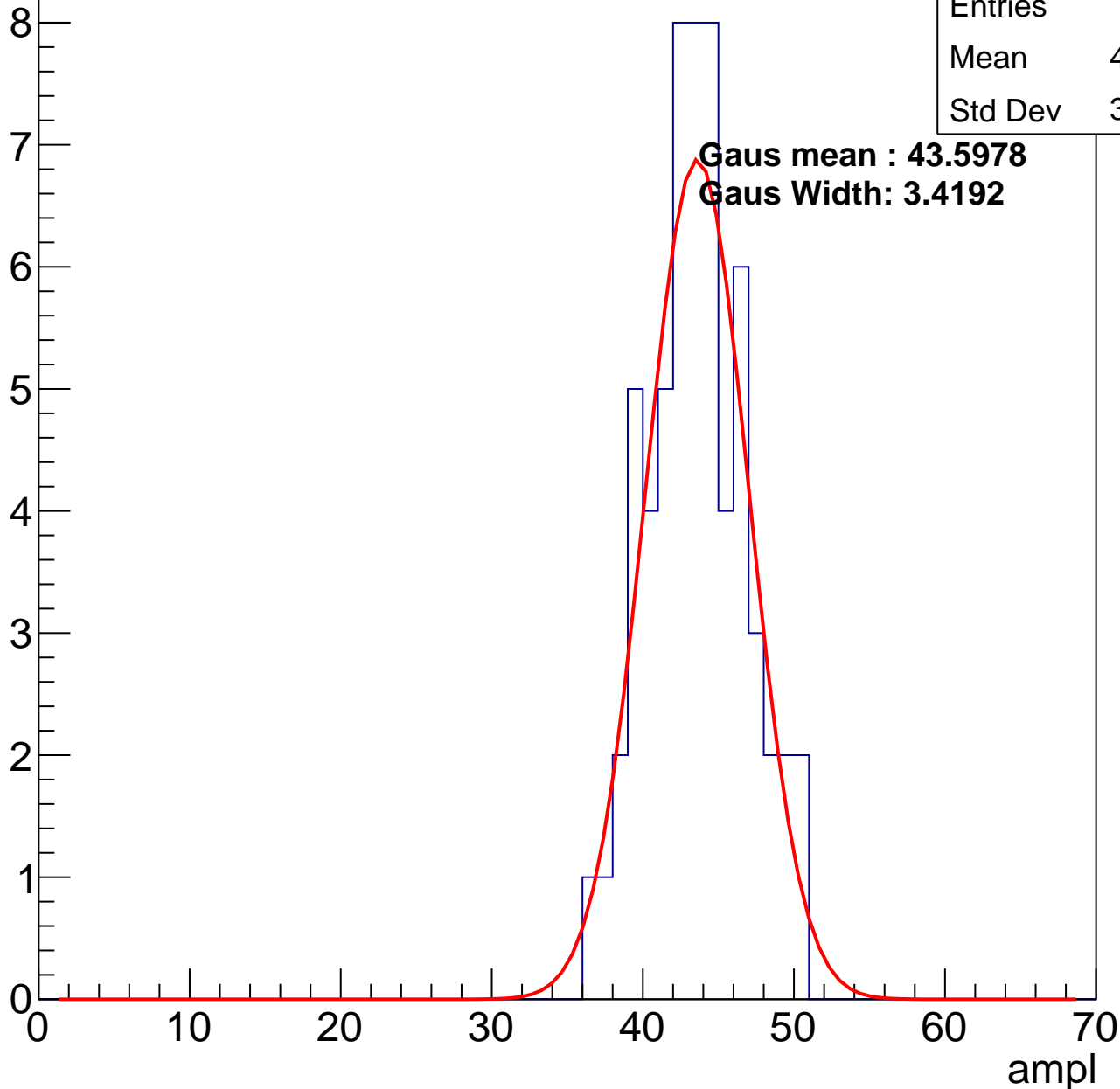
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	61
Mean	43.15
Std Dev	3.198

**Gaus mean : 43.5978**

**Gaus Width: 3.4192**

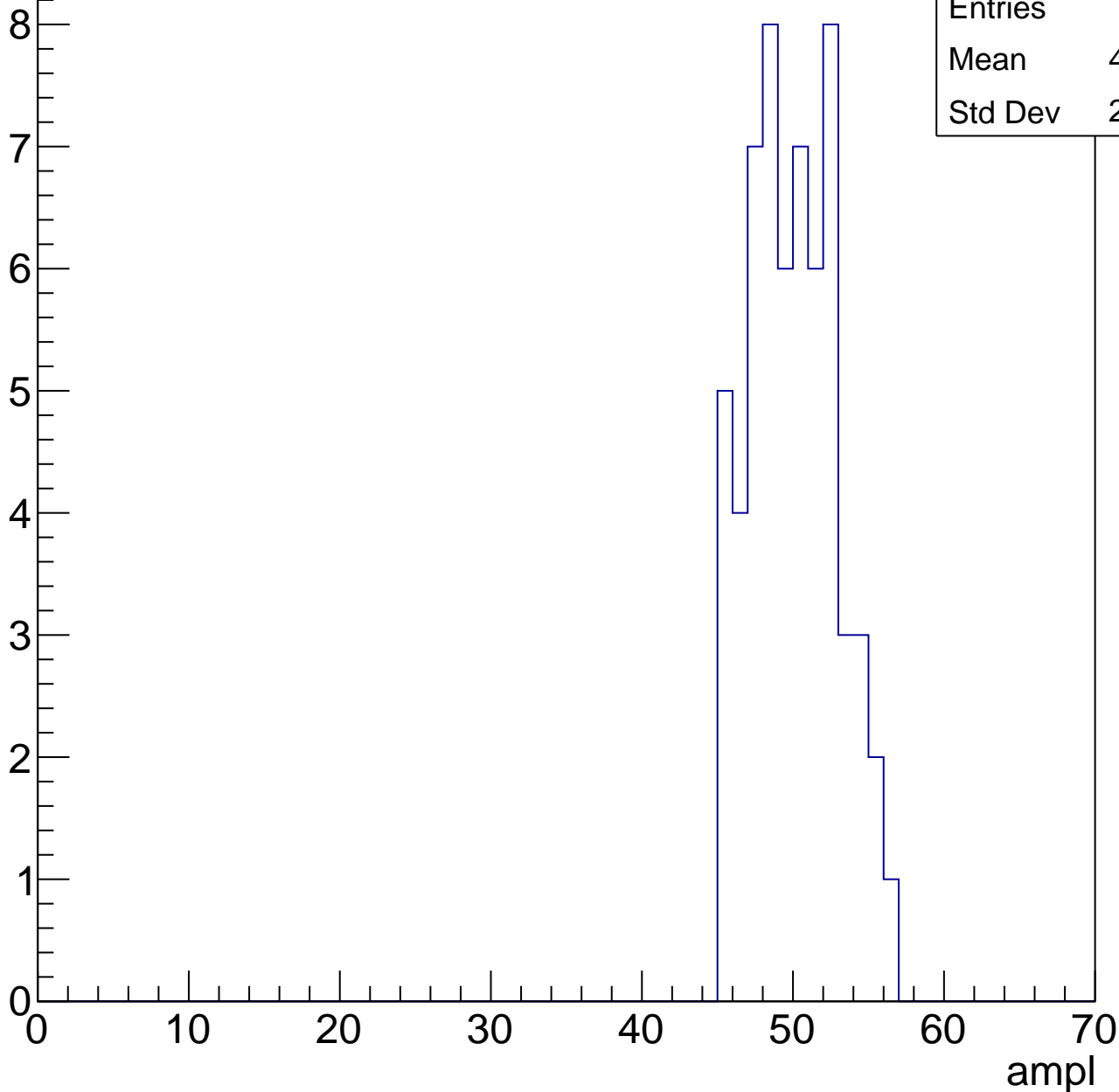


# B0L002S, U2-ch38, adc3

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	60
Mean	49.58
Std Dev	2.824

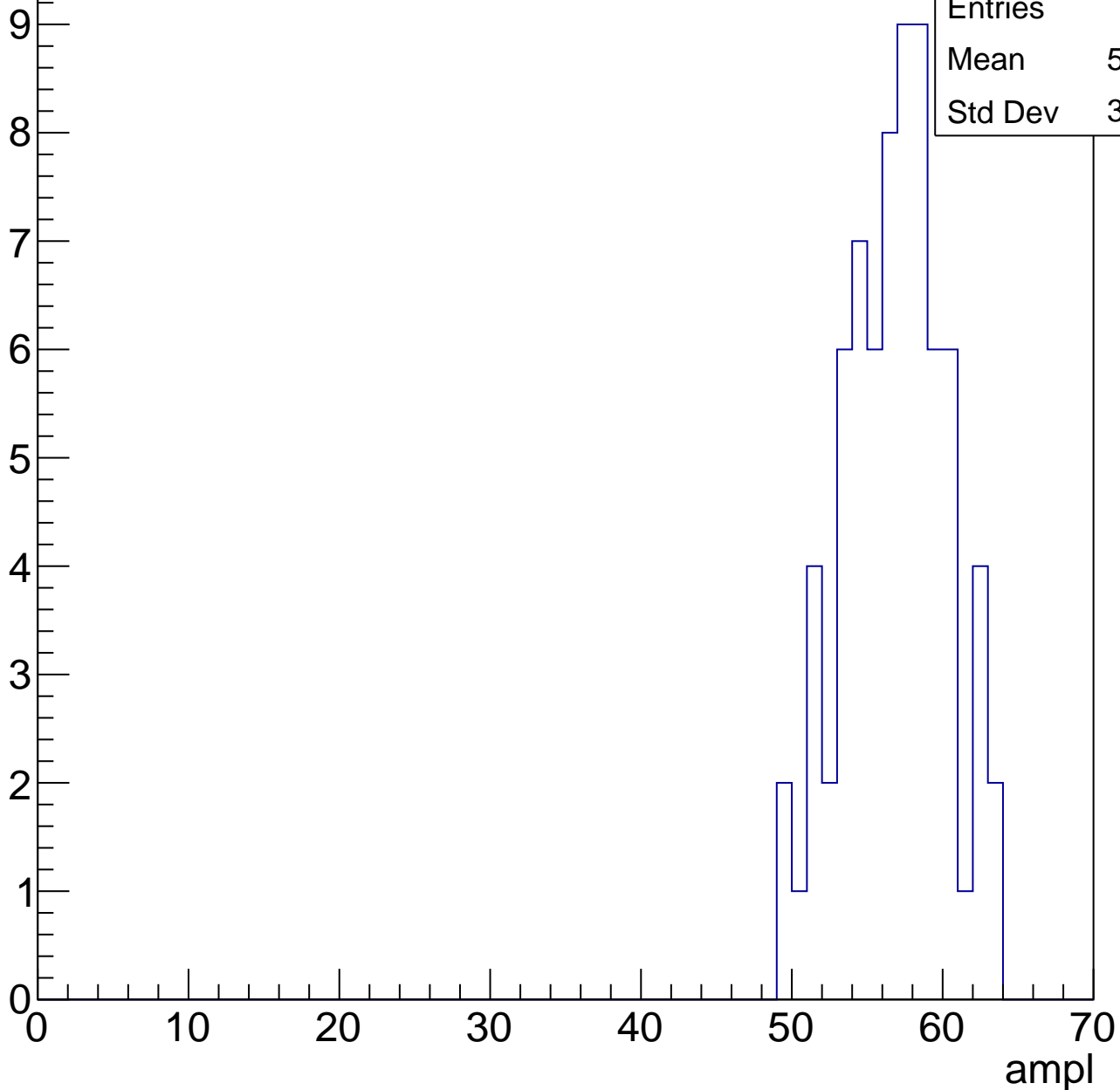


# B0L002S, U2-ch38, adc4

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	73
Mean	56.36
Std Dev	3.324

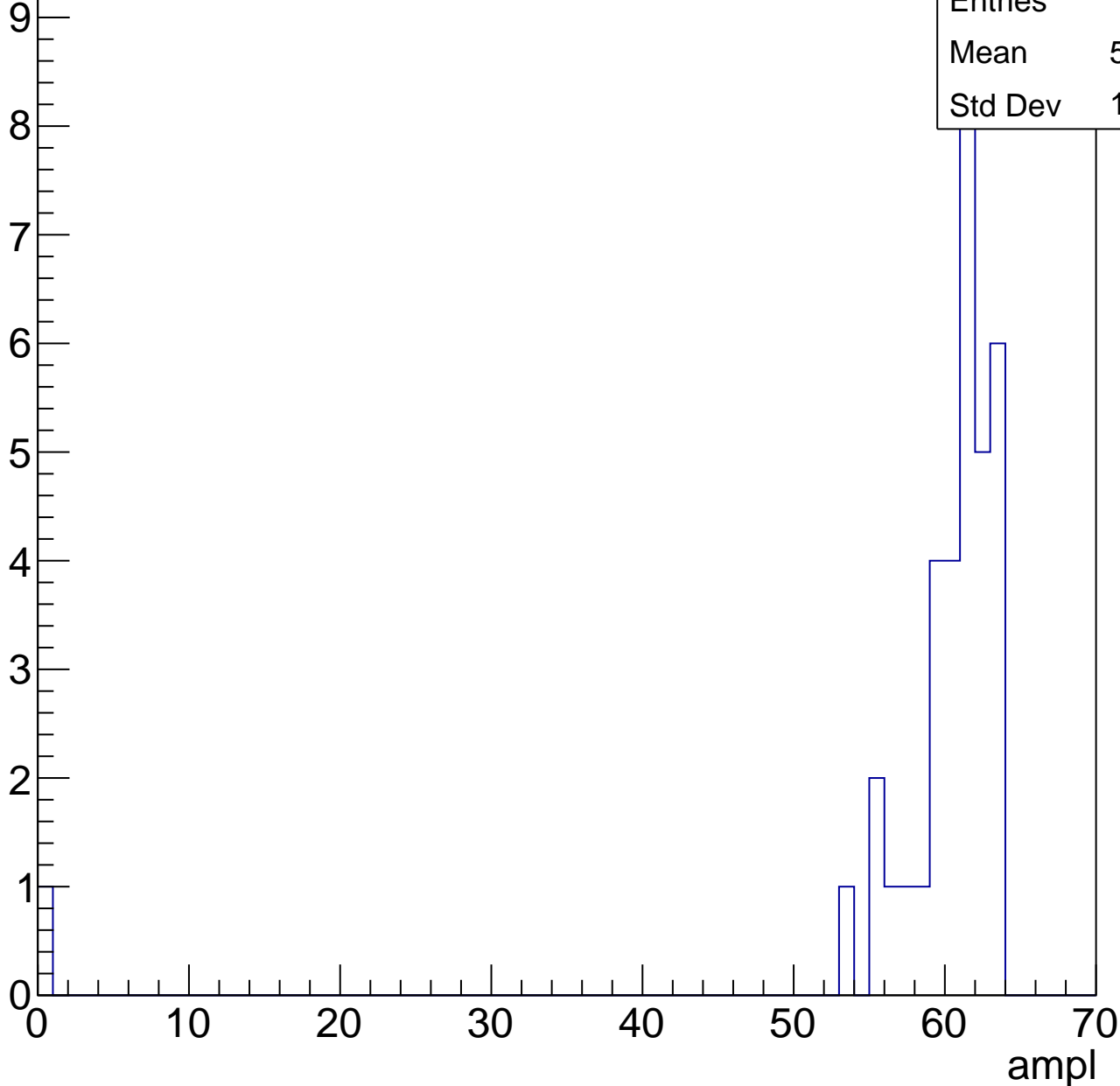


# B0L002S, U2-ch38, adc5

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	35
Mean	58.49
Std Dev	10.33



# B0L002S, U2-ch38, adc6

calib\_packv5\_042523\_0143.root, FC#8, port C1

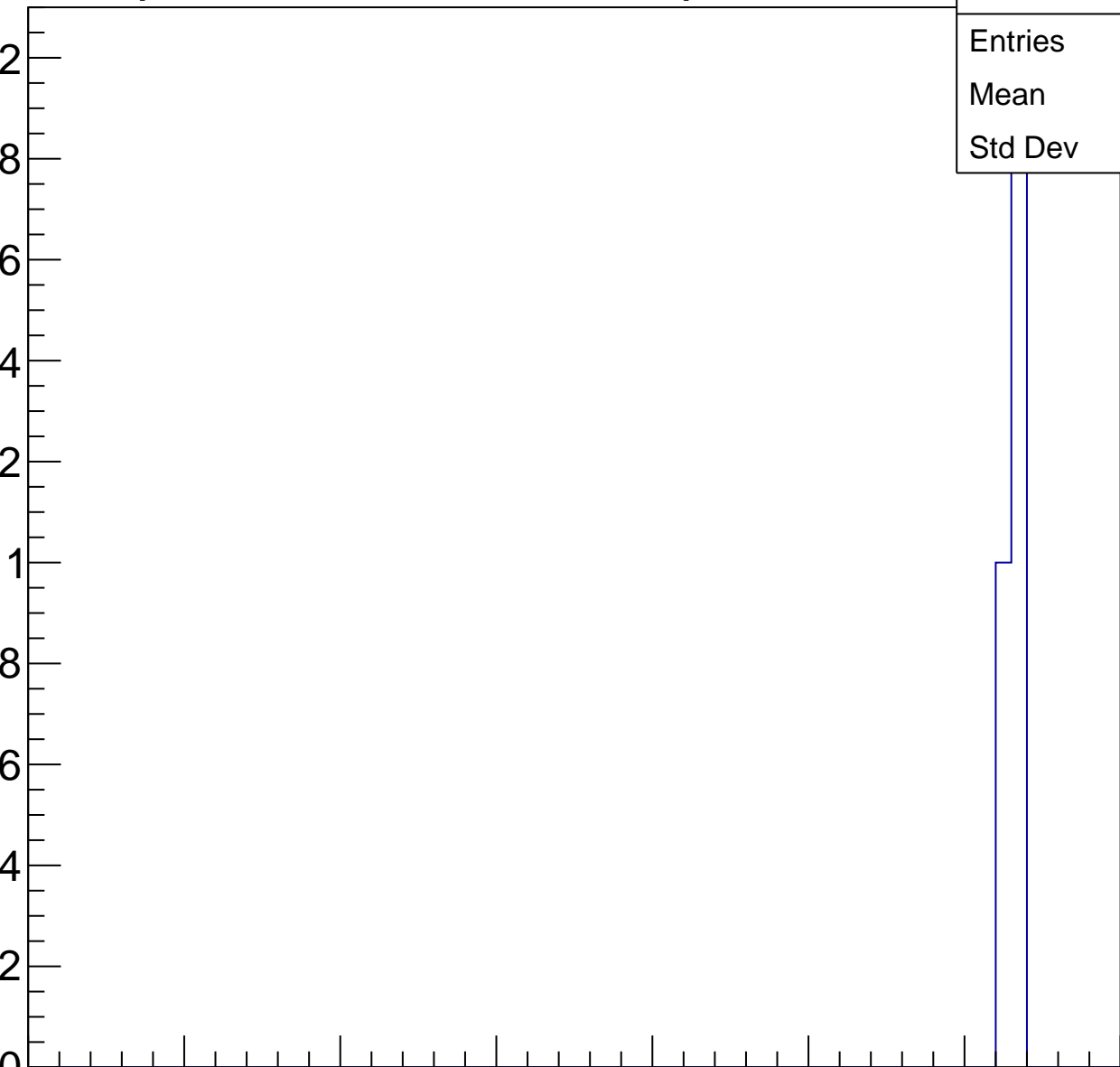
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	3
Mean	62.67
Std Dev	0.4714

0 10 20 30 40 50 60 70

ampl





# B0L002S, U2-ch38, adc7

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L002S, U2-ch39, adc0

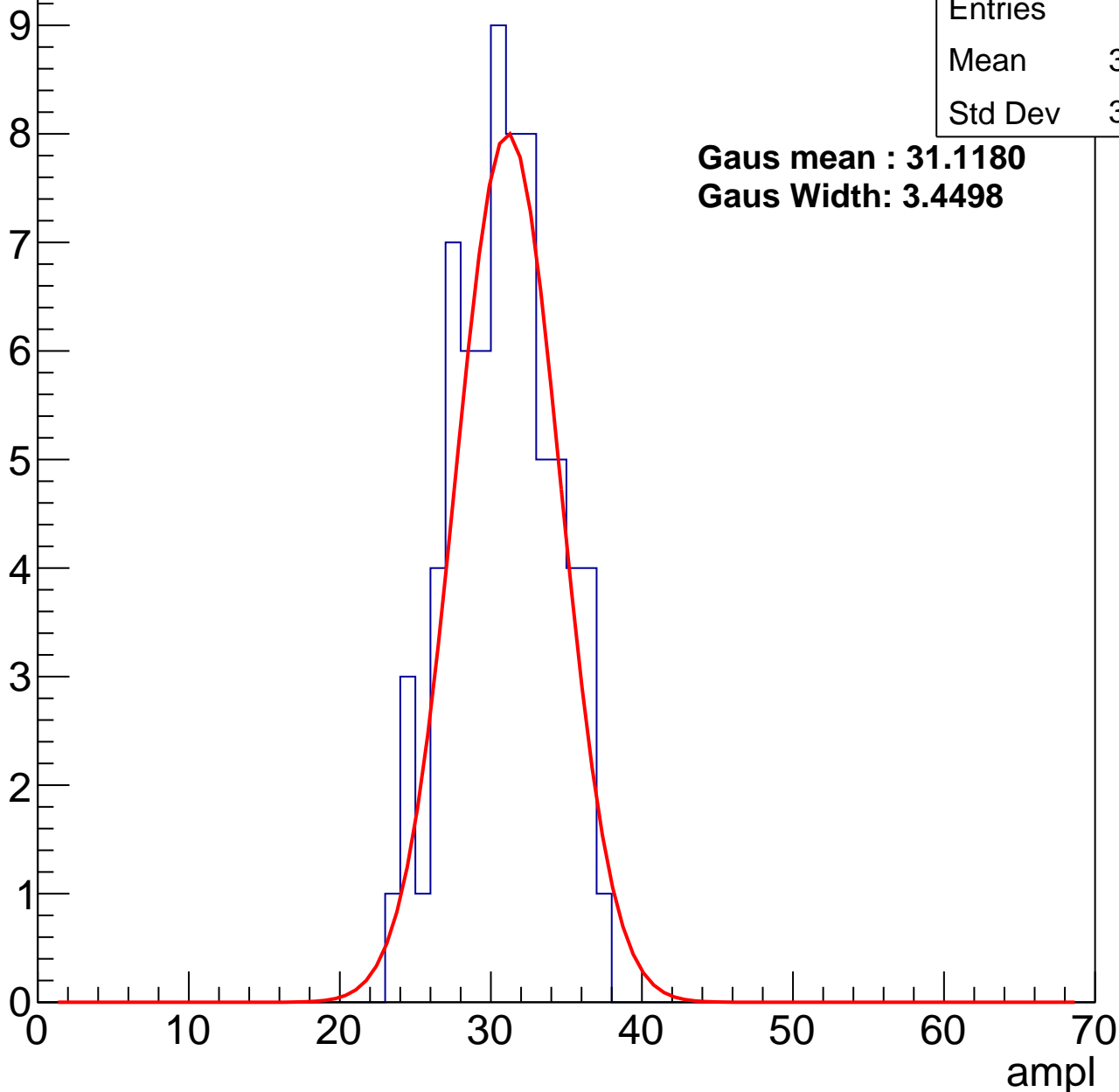
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	72
Mean	30.35
Std Dev	3.309

**Gaus mean : 31.1180**

**Gaus Width: 3.4498**



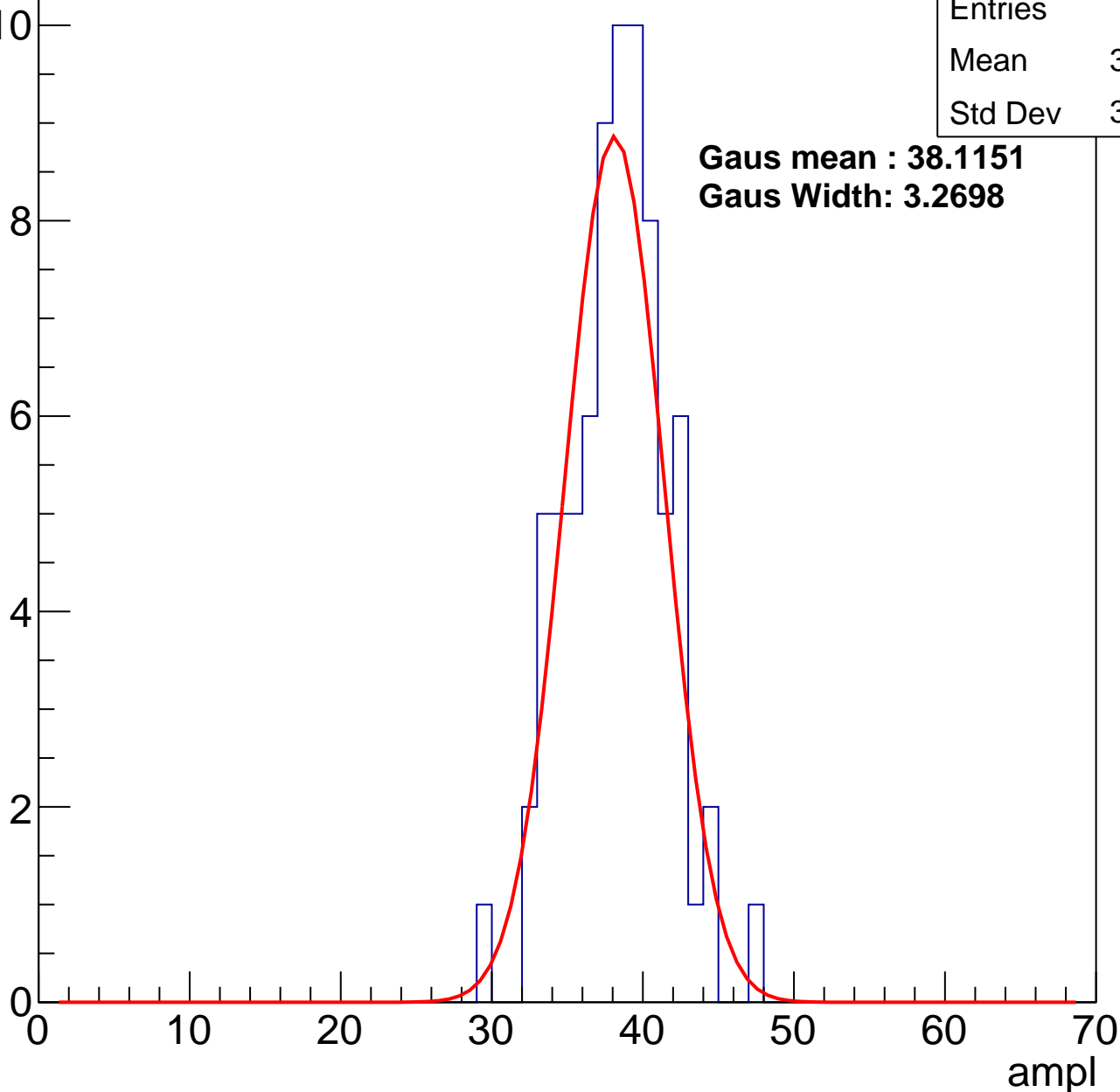
# B0L002S, U2-ch39, adc1

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	76
Mean	37.86
Std Dev	3.235

**Gaus mean : 38.1151**  
**Gaus Width: 3.2698**



# B0L002S, U2-ch39, adc2

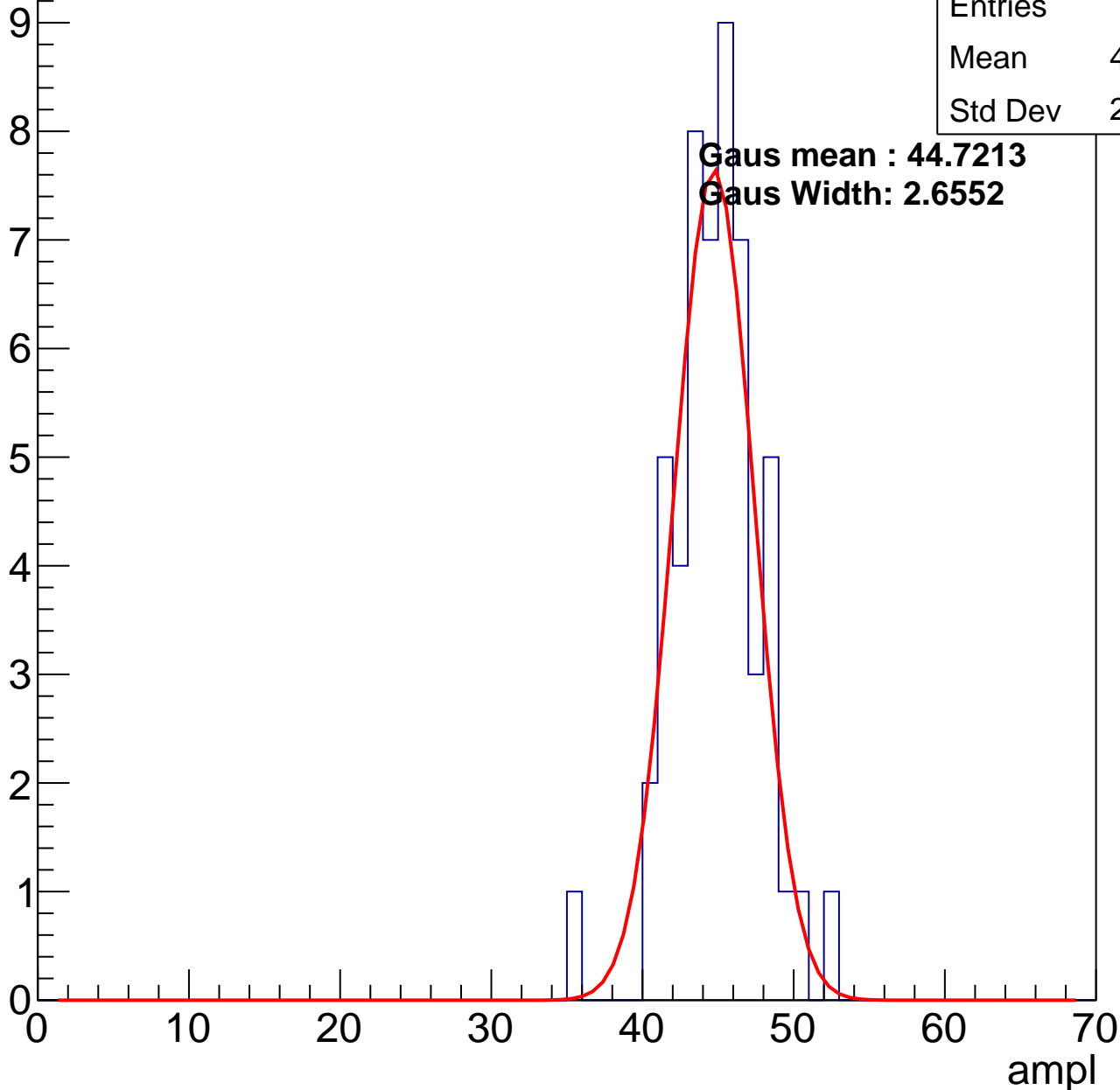
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	54
Mean	44.43
Std Dev	2.858

**Gaus mean : 44.7213**

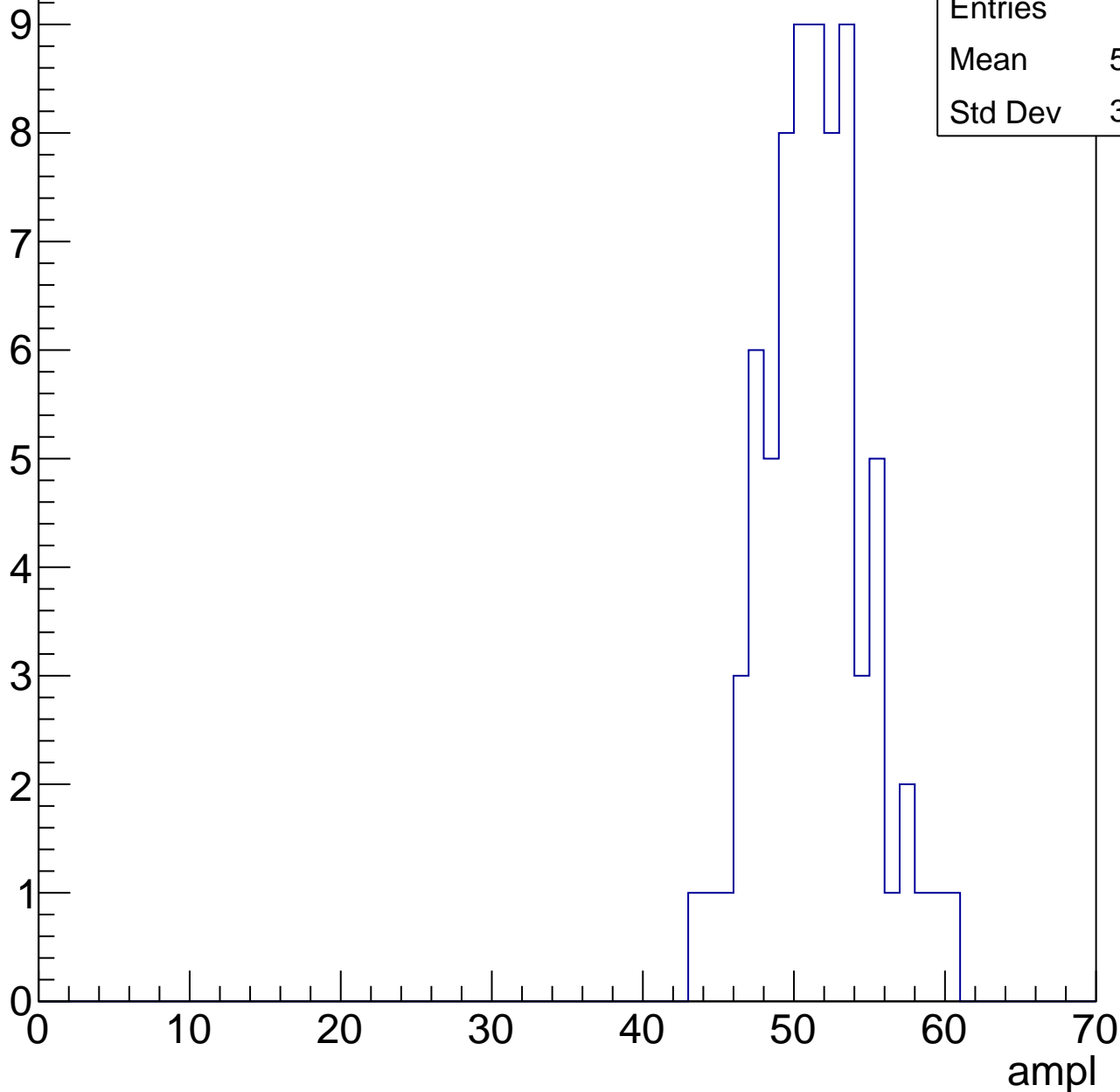
**Gaus Width: 2.6552**



# B0L002S, U2-ch39, adc3

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

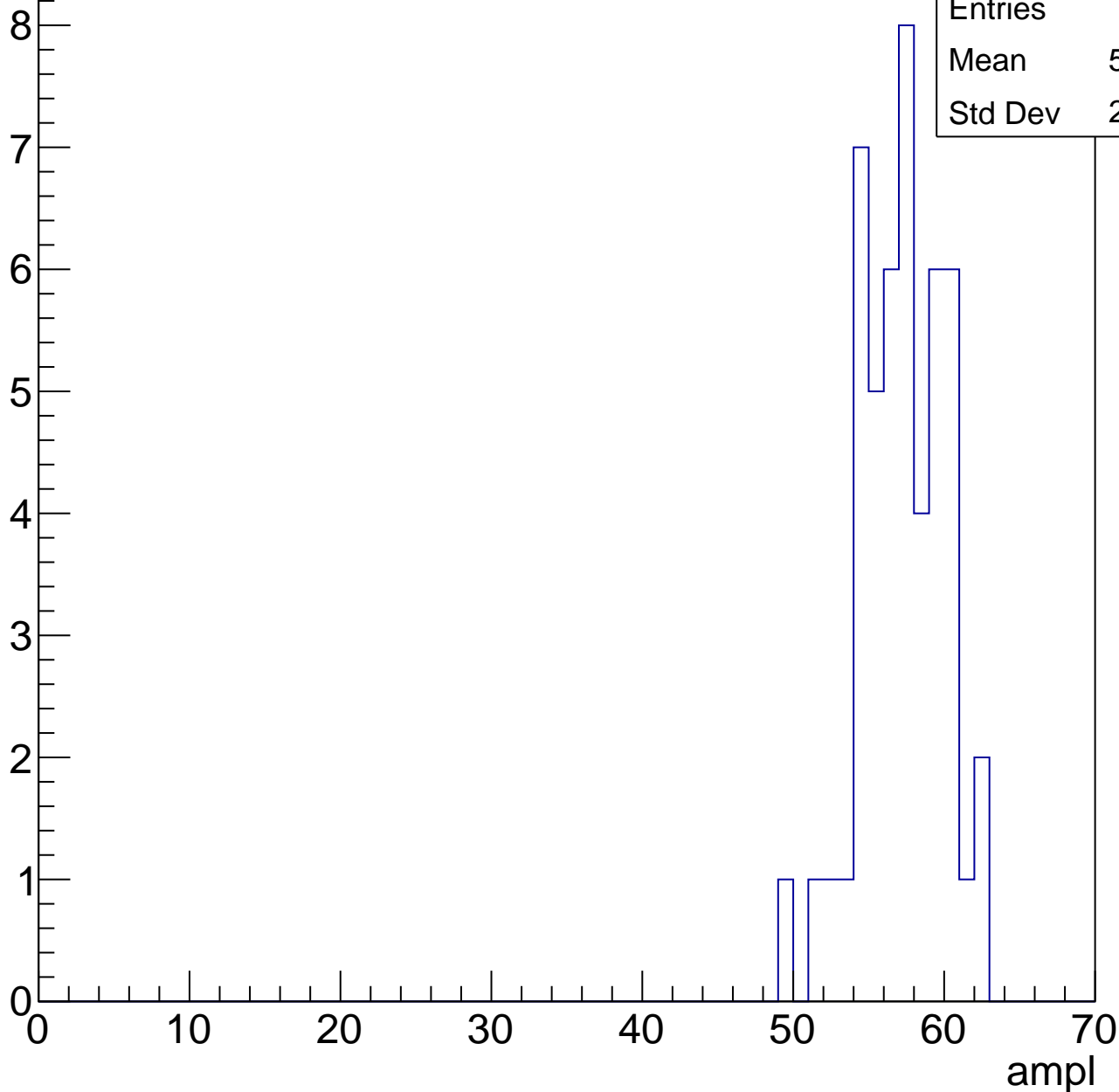


# B0L002S, U2-ch39, adc4

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	49
Mean	56.76
Std Dev	2.767



# B0L002S, U2-ch39, adc5

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

10

Entries 42

Mean 59.29

Std Dev 9.488

8

6

4

2

0

0

10

20

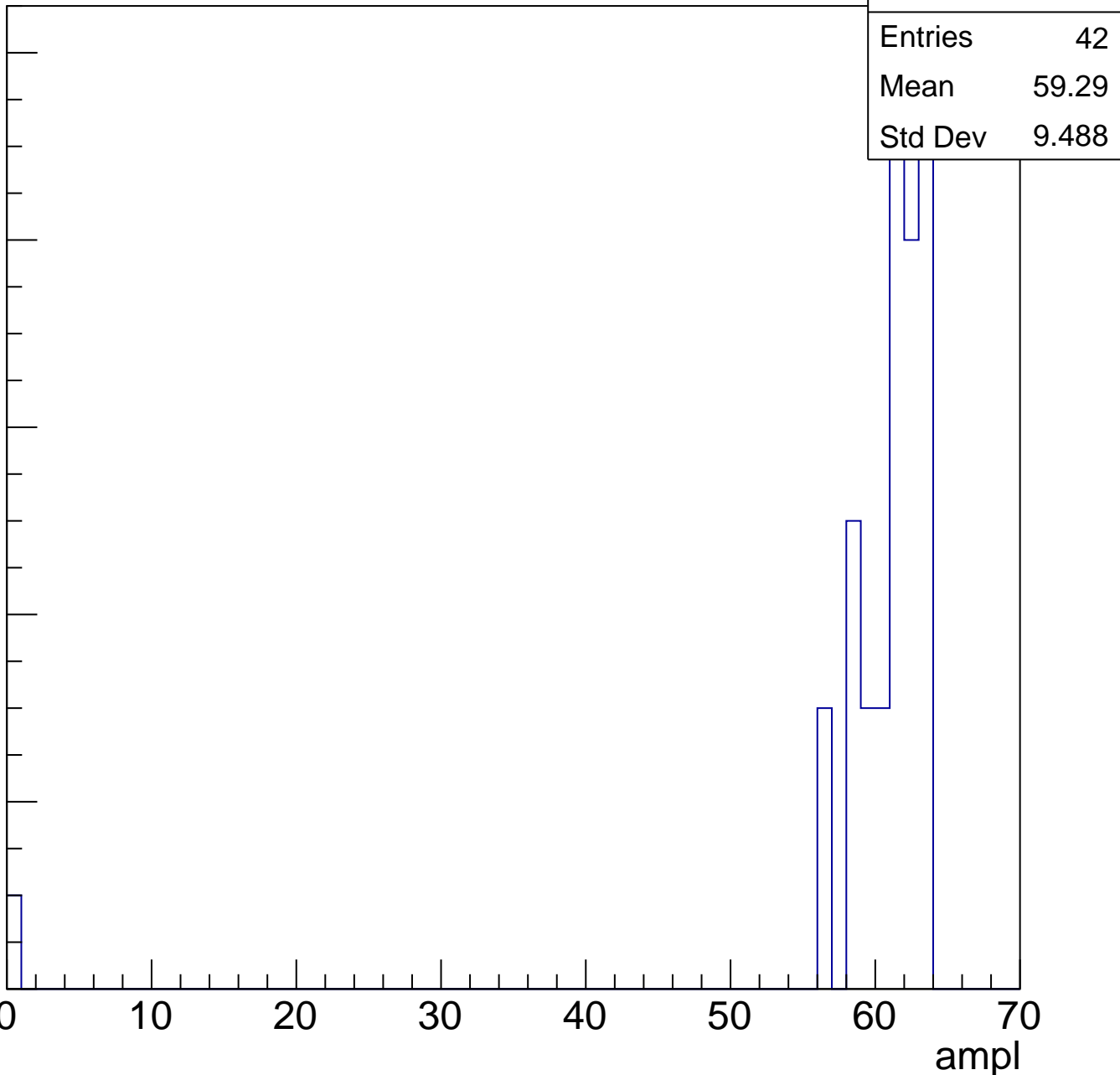
30

40

50

60

ampl



# B0L002S, U2-ch39, adc6

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



Entries	0
Mean	0
Std Dev	0



# B0L002S, U2-ch39, adc7

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



Entries	2
Mean	11
Std Dev	11

# B0L002S, U2-ch40, adc0

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entries	83
Mean	31.05
Std Dev	4.864

**Gaus mean : 32.2696**

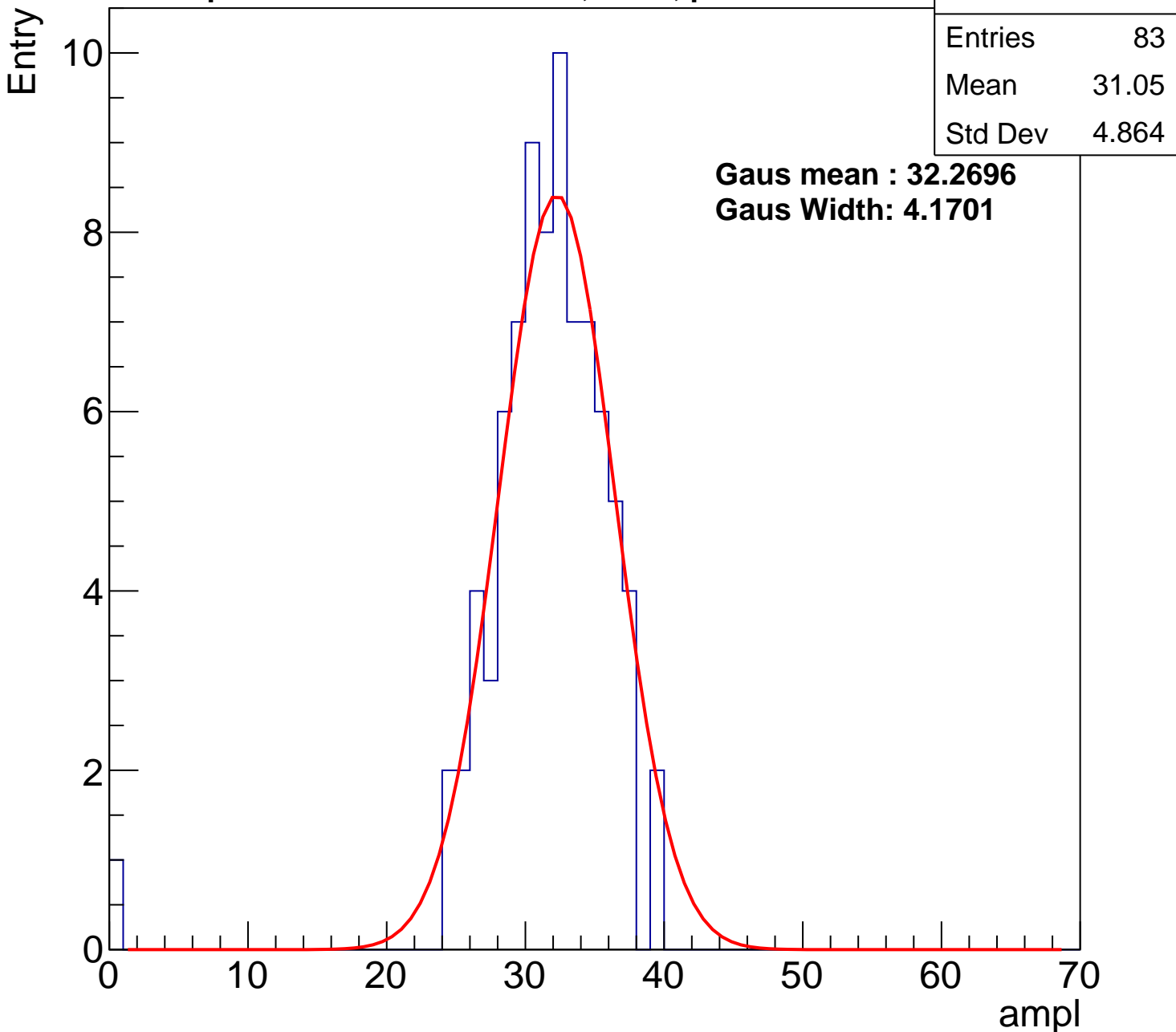
**Gaus Width: 4.1701**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L002S, U2-ch40, adc1

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

6  
5  
4  
3  
2  
1  
0

Entries	46
Mean	37.96
Std Dev	2.896

**Gaus mean : 38.6250**

**Gaus Width: 3.8024**

0  
1  
2  
3  
4  
5  
6

ampl

0 10 20 30 40 50 60 70

# B0L002S, U2-ch40, adc2

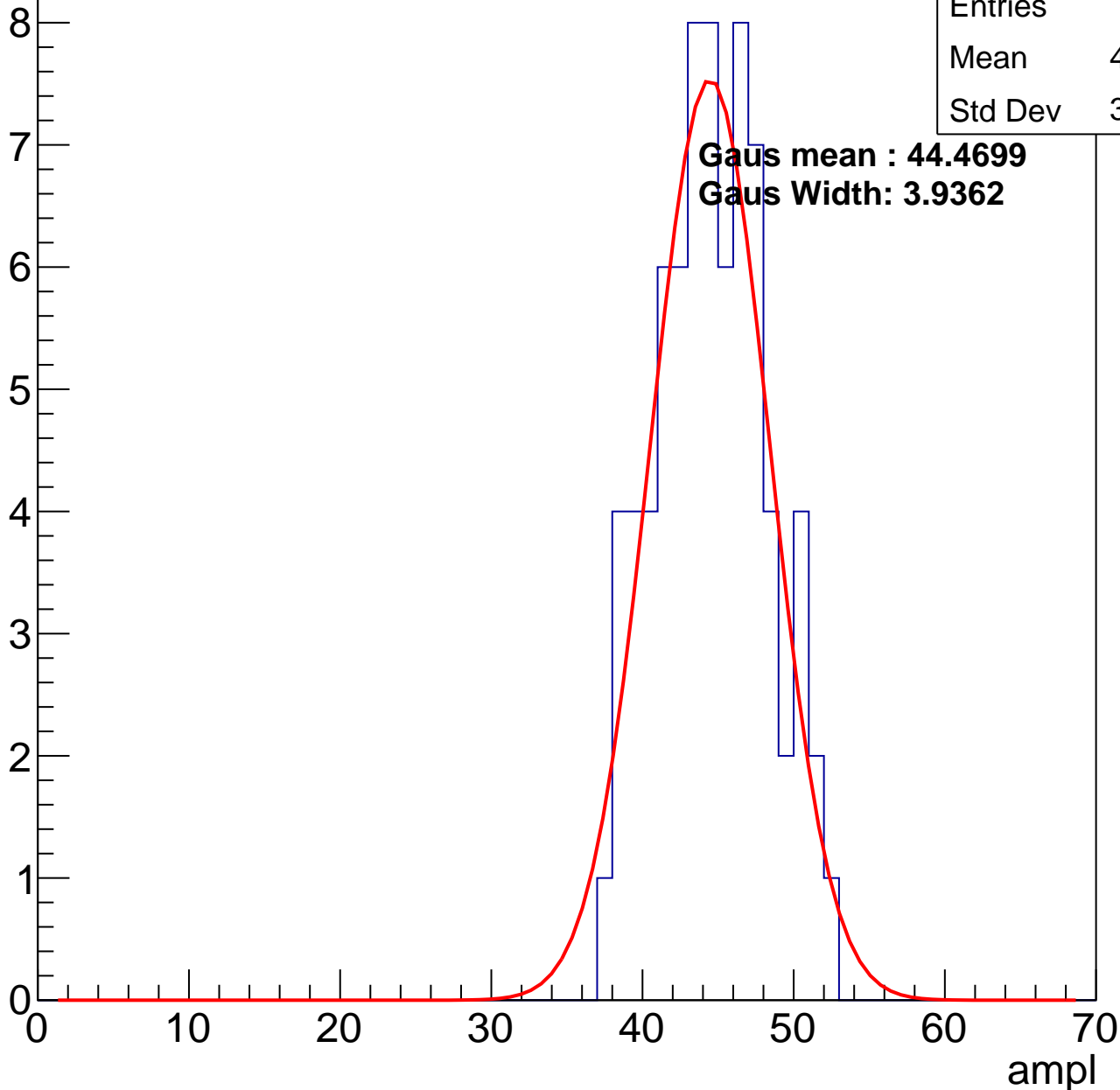
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	75
Mean	44.13
Std Dev	3.583

**Gaus mean : 44.4699**

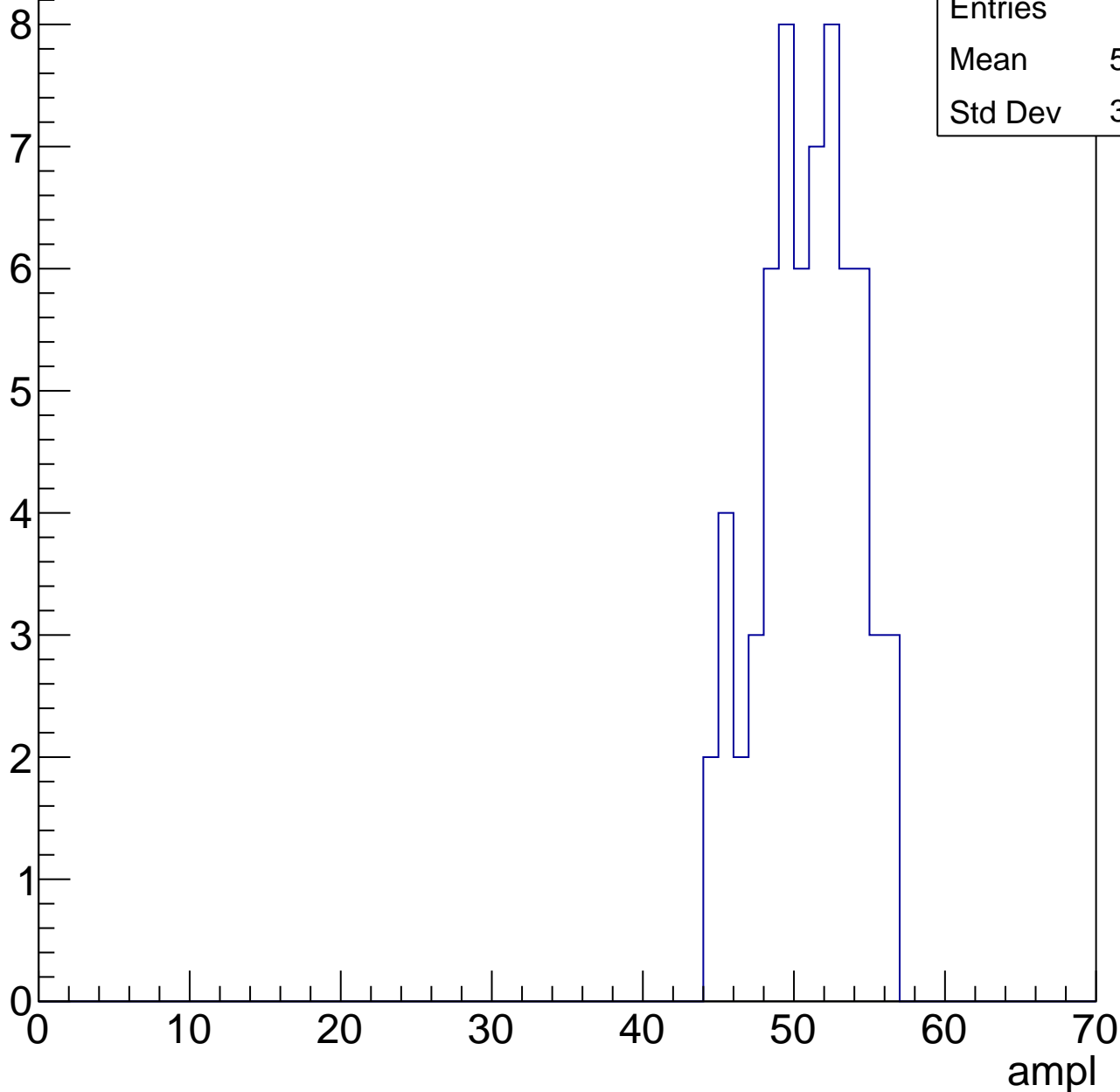
**Gaus Width: 3.9362**



# B0L002S, U2-ch40, adc3

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

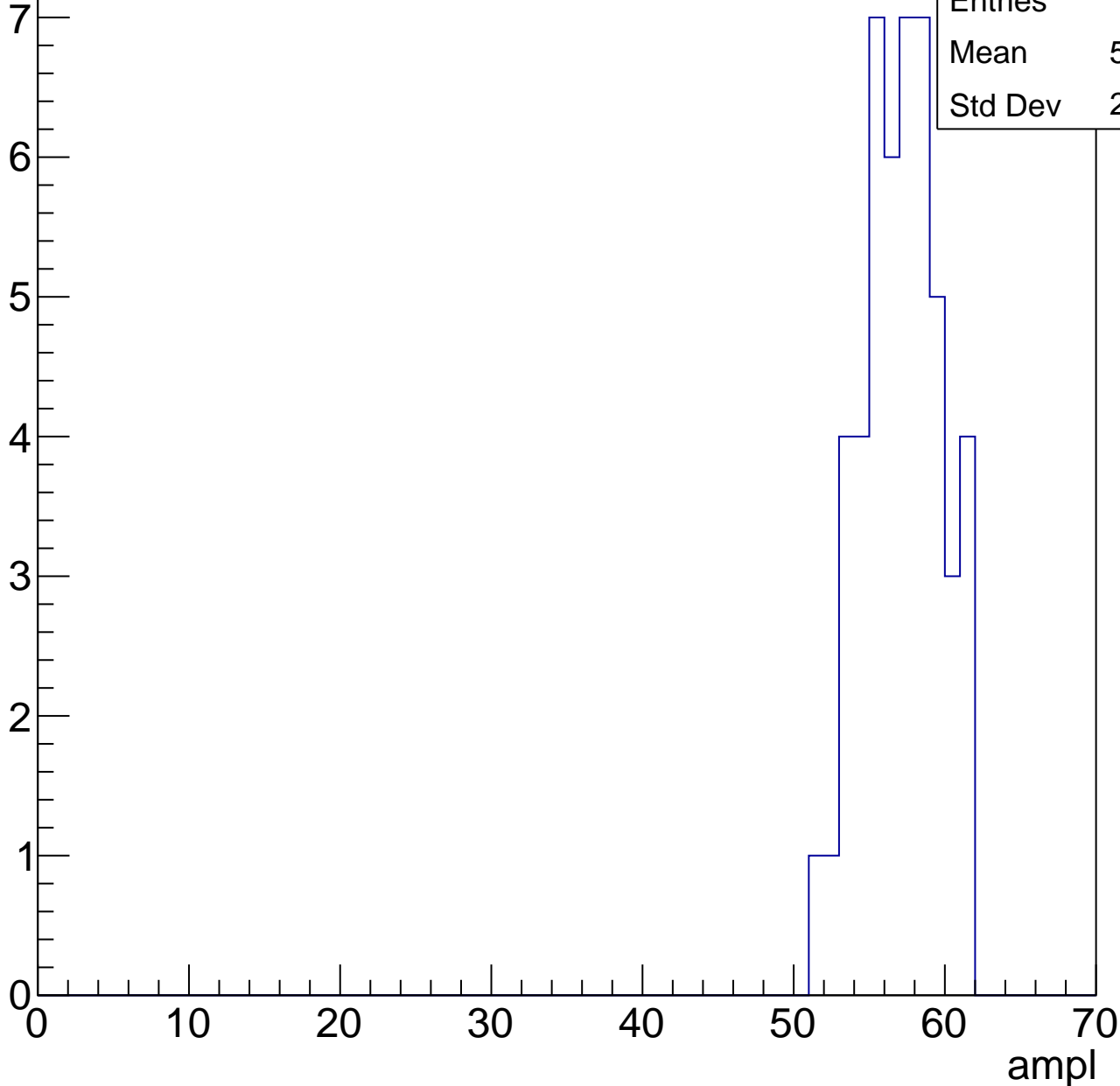


# B0L002S, U2-ch40, adc4

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	49
Mean	56.65
Std Dev	2.503

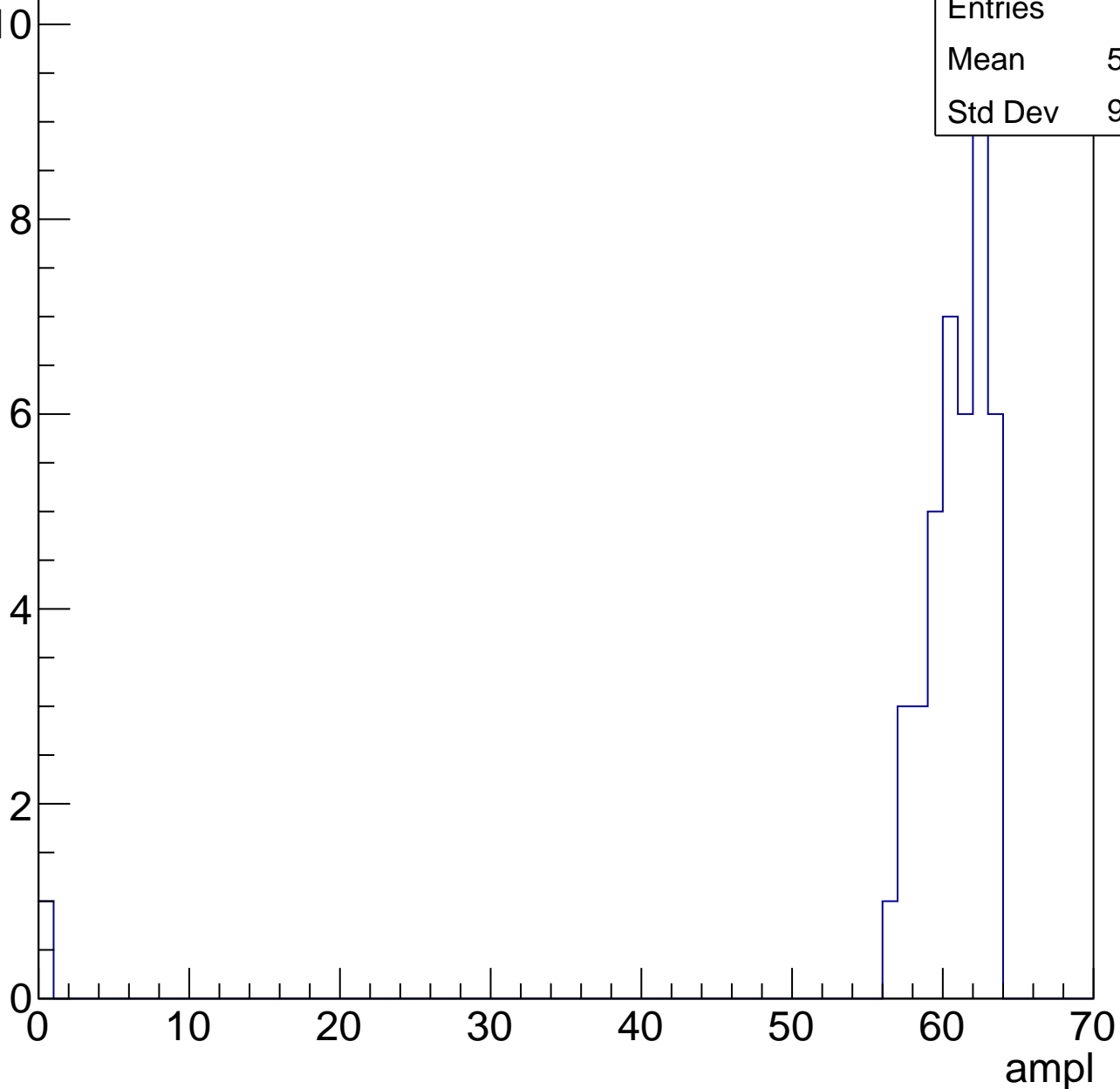


# B0L002S, U2-ch40, adc5

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

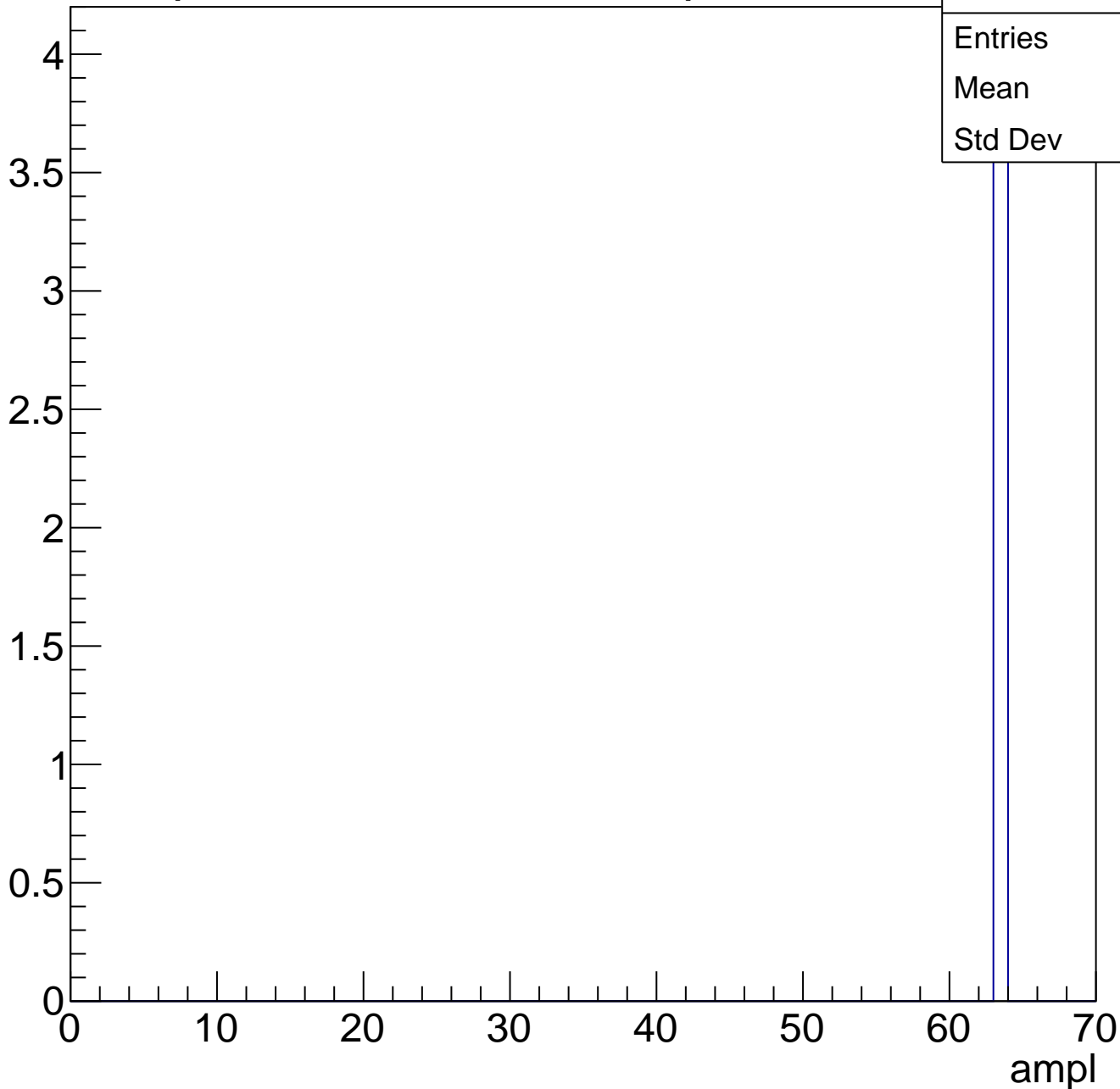
Entries	42
Mean	59.05
Std Dev	9.414



# B0L002S, U2-ch40, adc6

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry





# B0L002S, U2-ch40, adc7

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L002S, U2-ch41, adc0

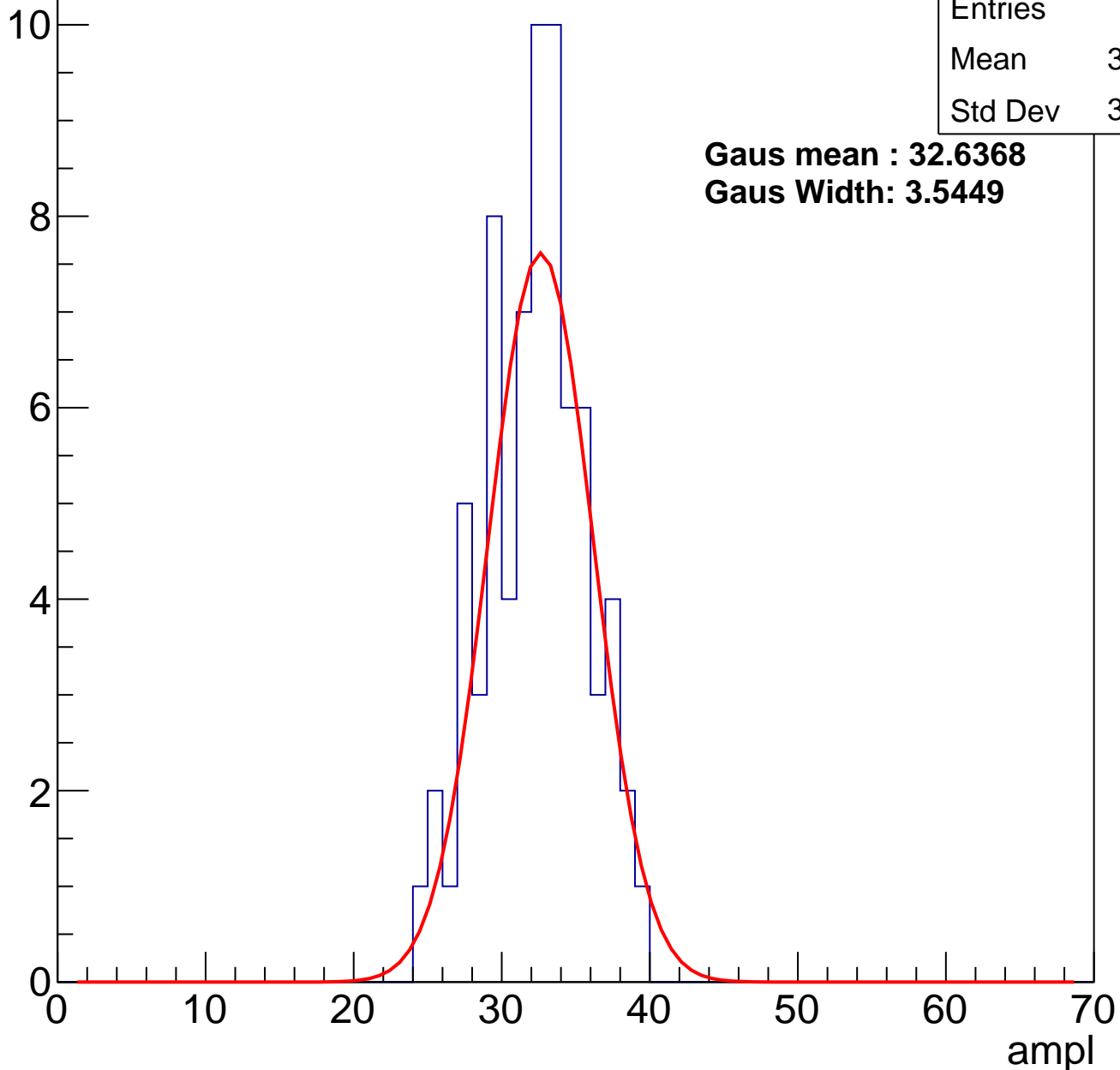
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entries	73
Mean	31.82
Std Dev	3.353

**Gaus mean : 32.6368**

**Gaus Width: 3.5449**

Entry



# B0L002S, U2-ch41, adc1

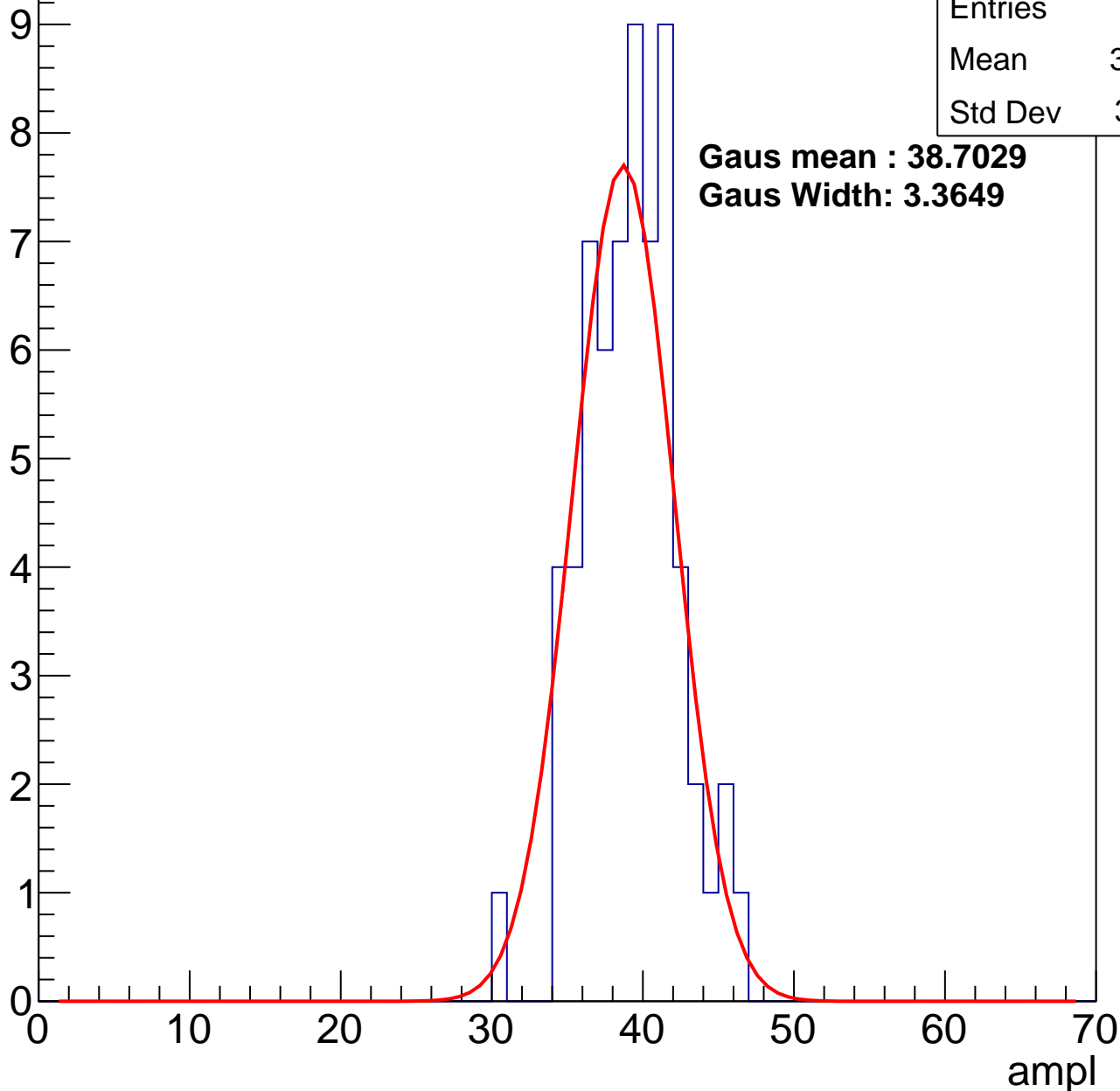
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	64
Mean	38.75
Std Dev	3.041

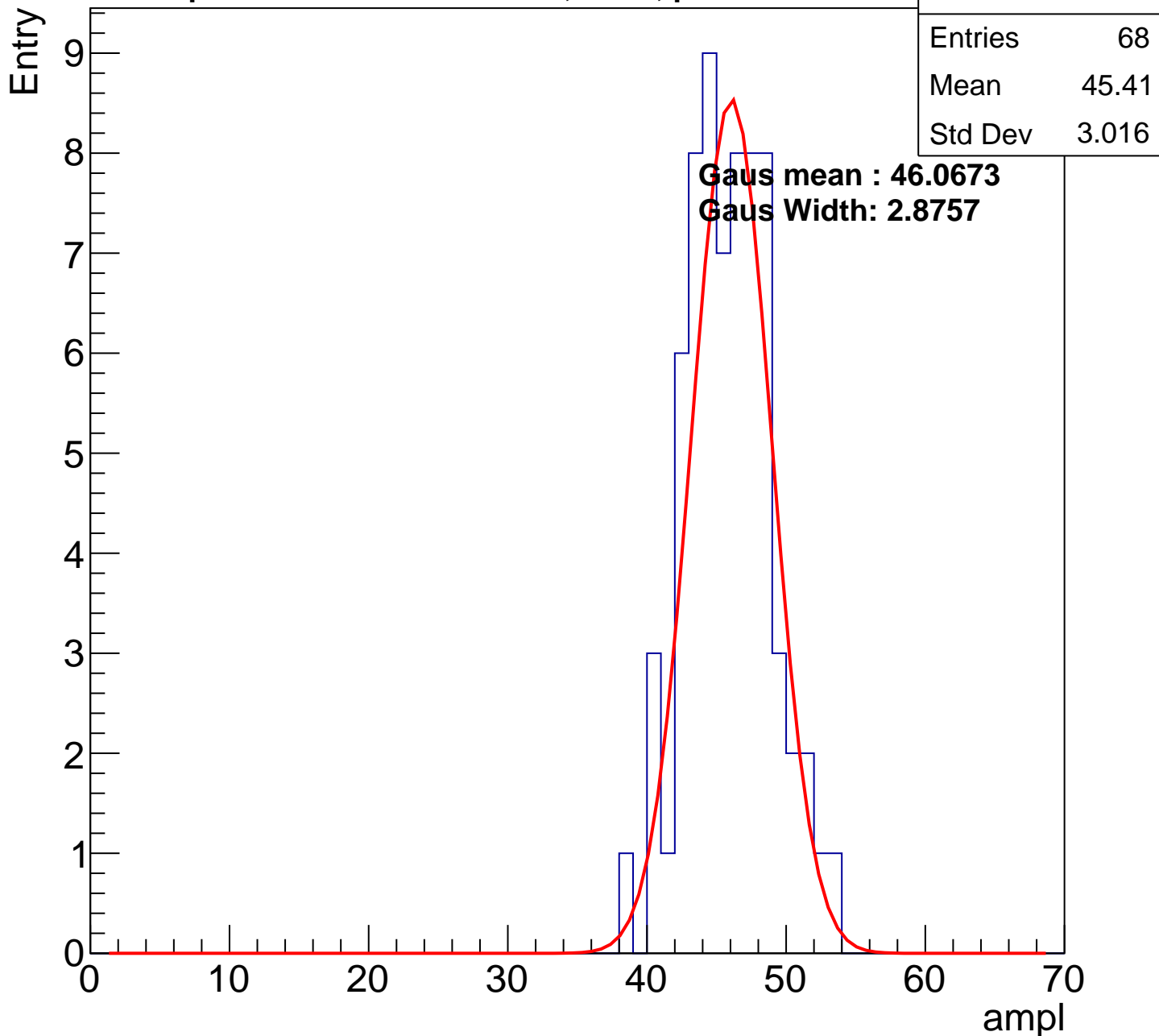
**Gaus mean : 38.7029**

**Gaus Width: 3.3649**



# B0L002S, U2-ch41, adc2

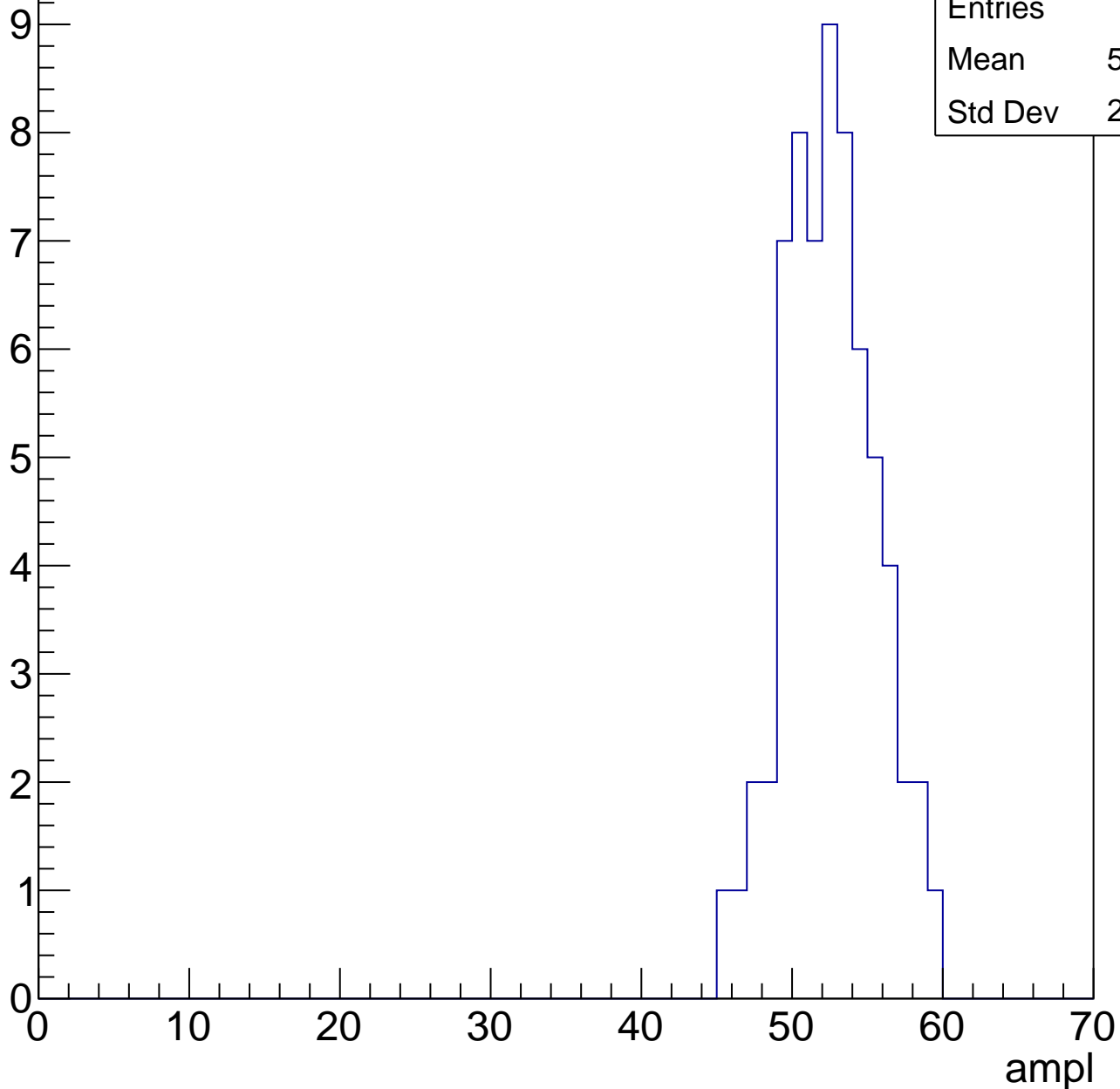
calib\_packv5\_042523\_0143.root, FC#8, port C1



# B0L002S, U2-ch41, adc3

calib\_packv5\_042523\_0143.root, FC#8, port C1

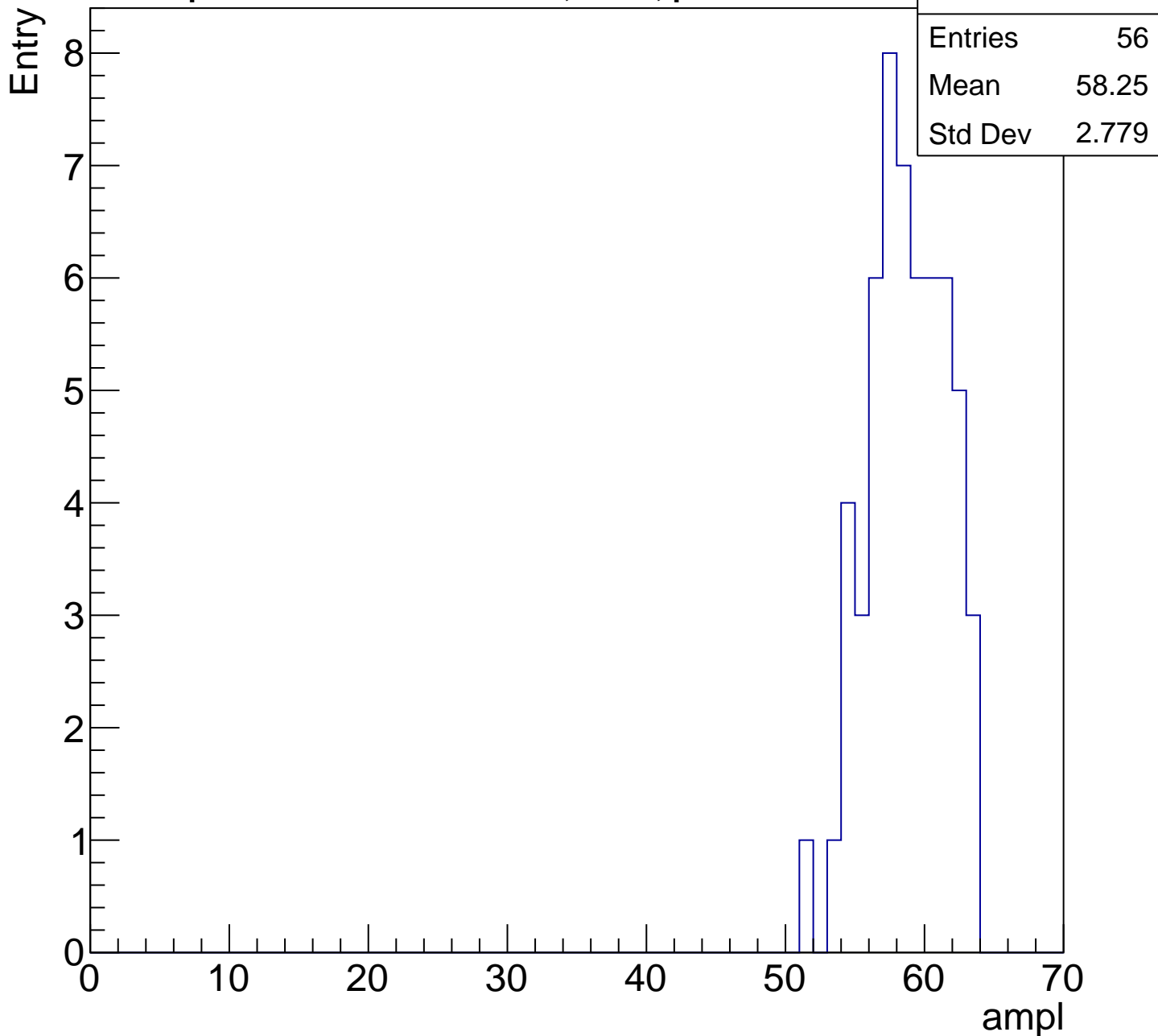
Entry



Entries	65
Mean	52.08
Std Dev	2.989

# B0L002S, U2-ch41, adc4

calib\_packv5\_042523\_0143.root, FC#8, port C1

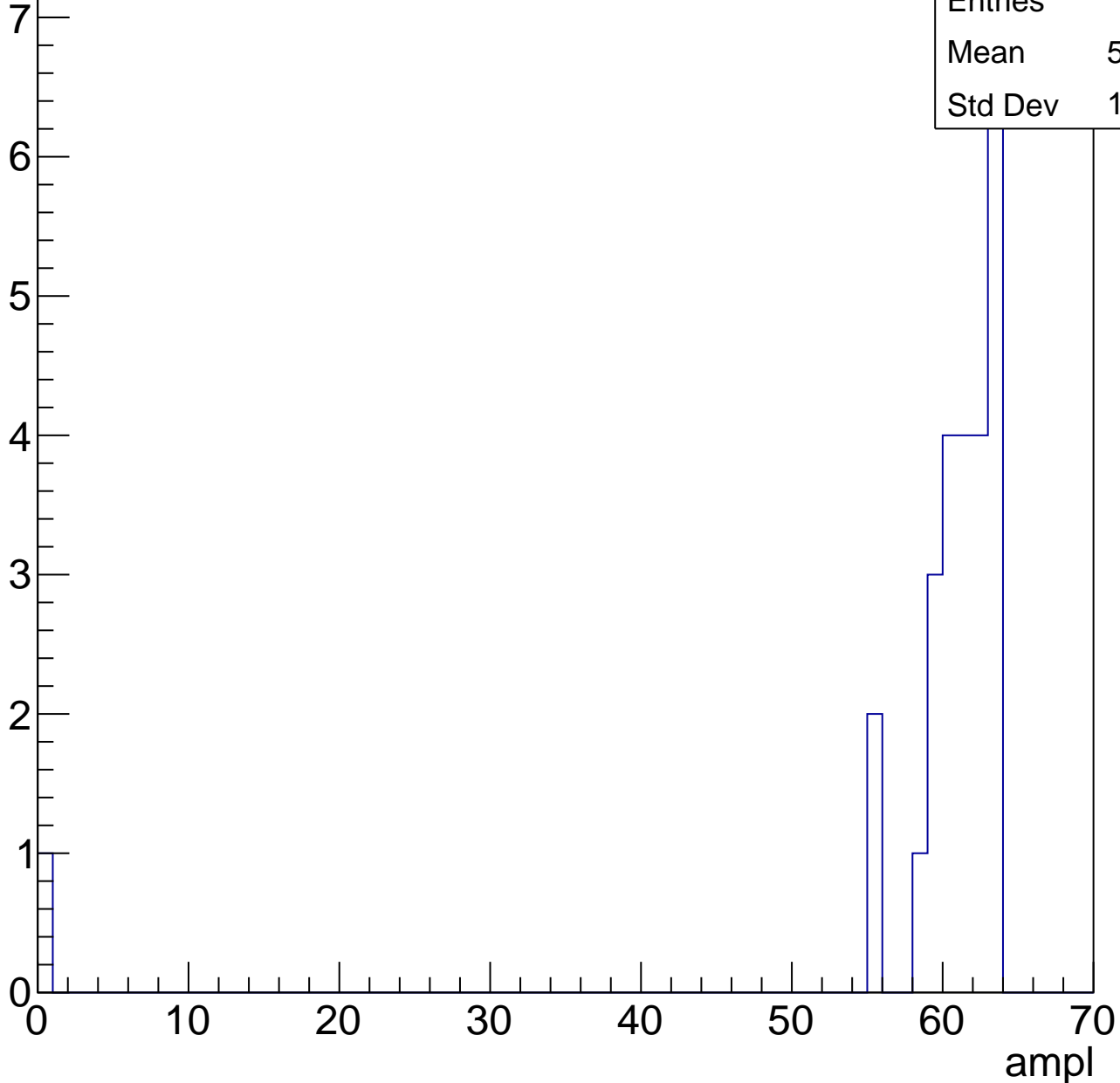


# B0L002S, U2-ch41, adc5

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	26
Mean	58.38
Std Dev	11.88



# B0L002S, U2-ch41, adc6

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry





# B0L002S, U2-ch41, adc7

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L002S, U2-ch42, adc0

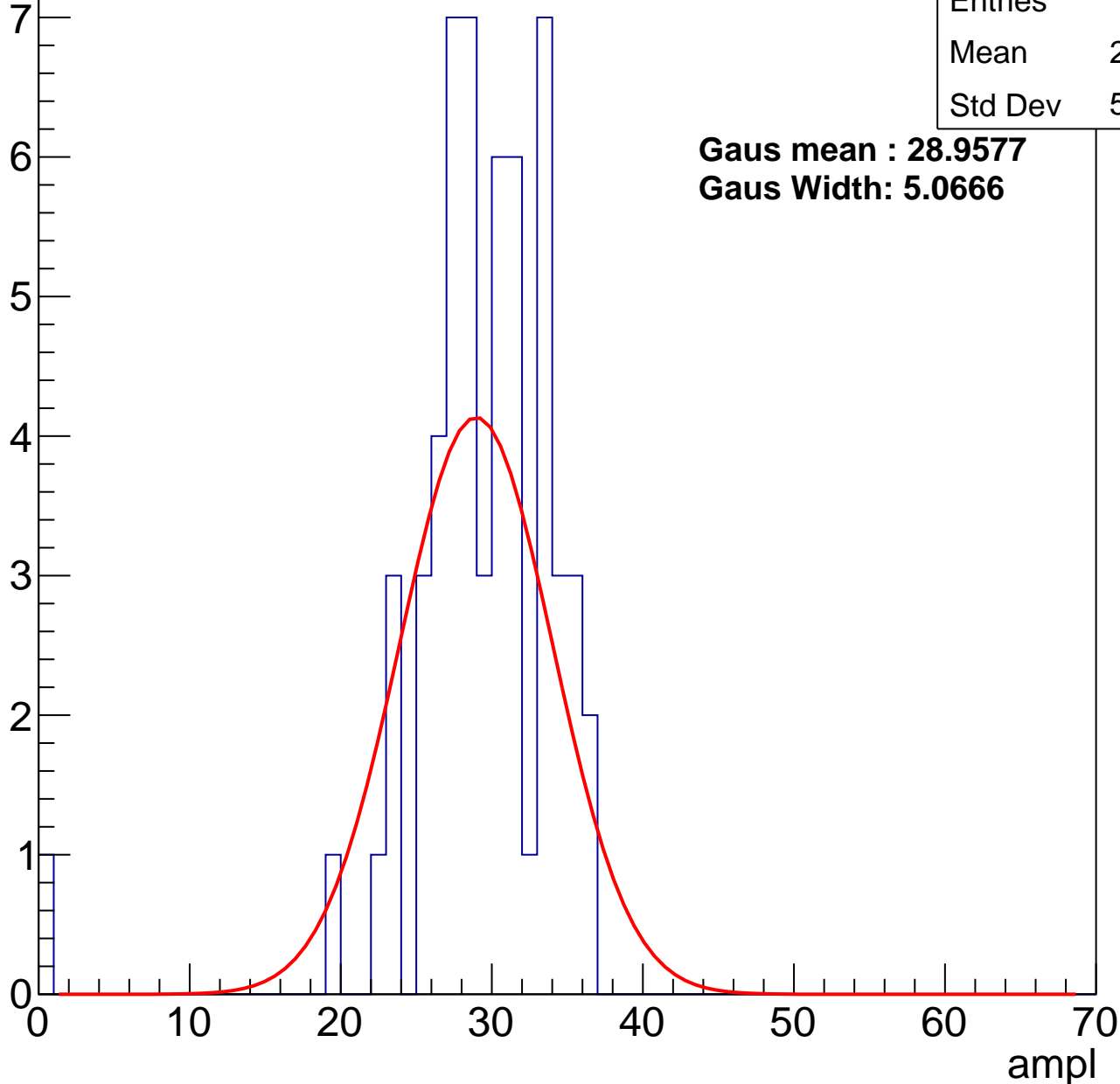
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	58
Mean	28.78
Std Dev	5.327

**Gaus mean : 28.9577**

**Gaus Width: 5.0666**



# B0L002S, U2-ch42, adc1

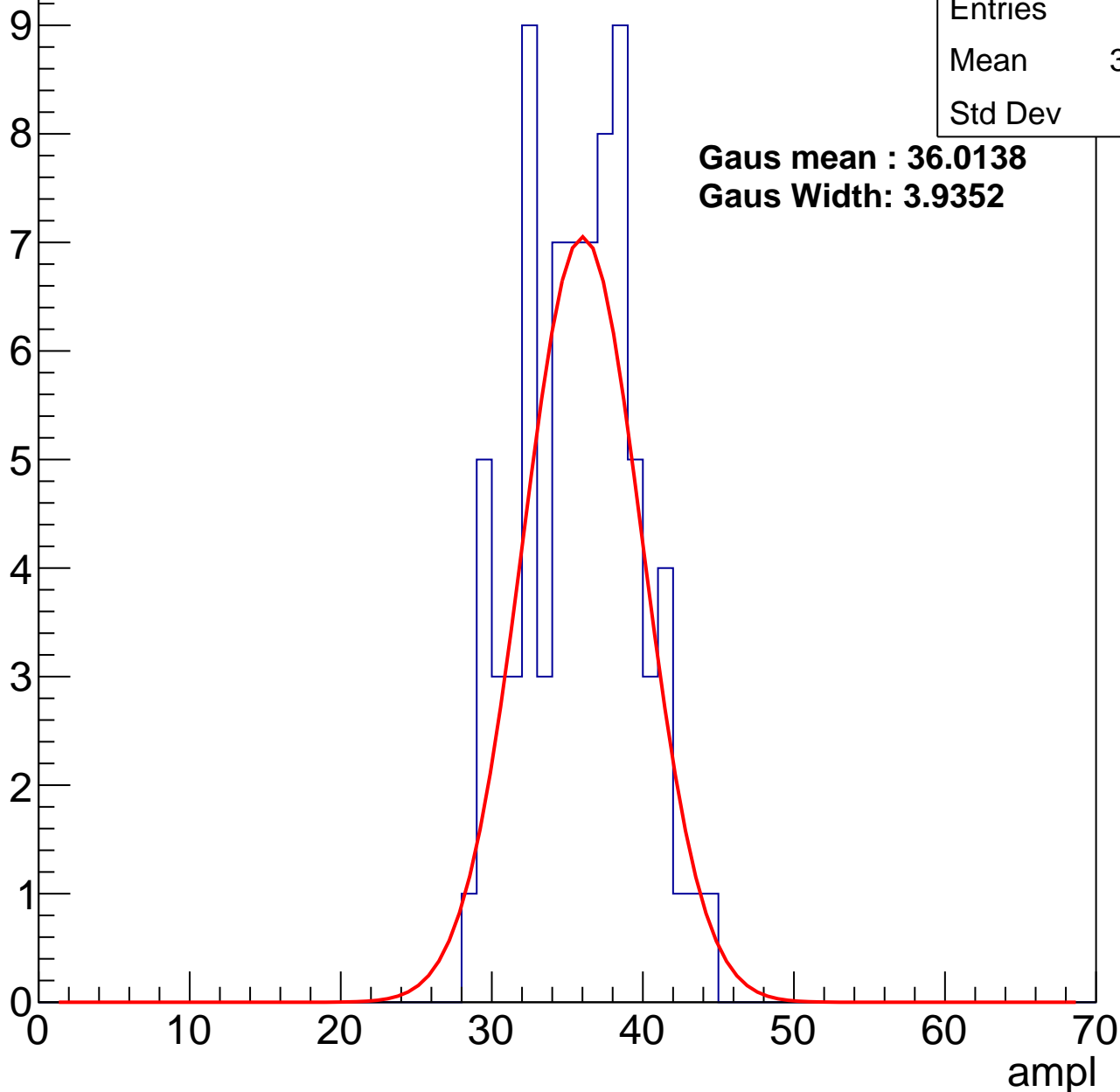
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	77
Mean	35.38
Std Dev	3.7

**Gaus mean : 36.0138**

**Gaus Width: 3.9352**



# B0L002S, U2-ch42, adc2

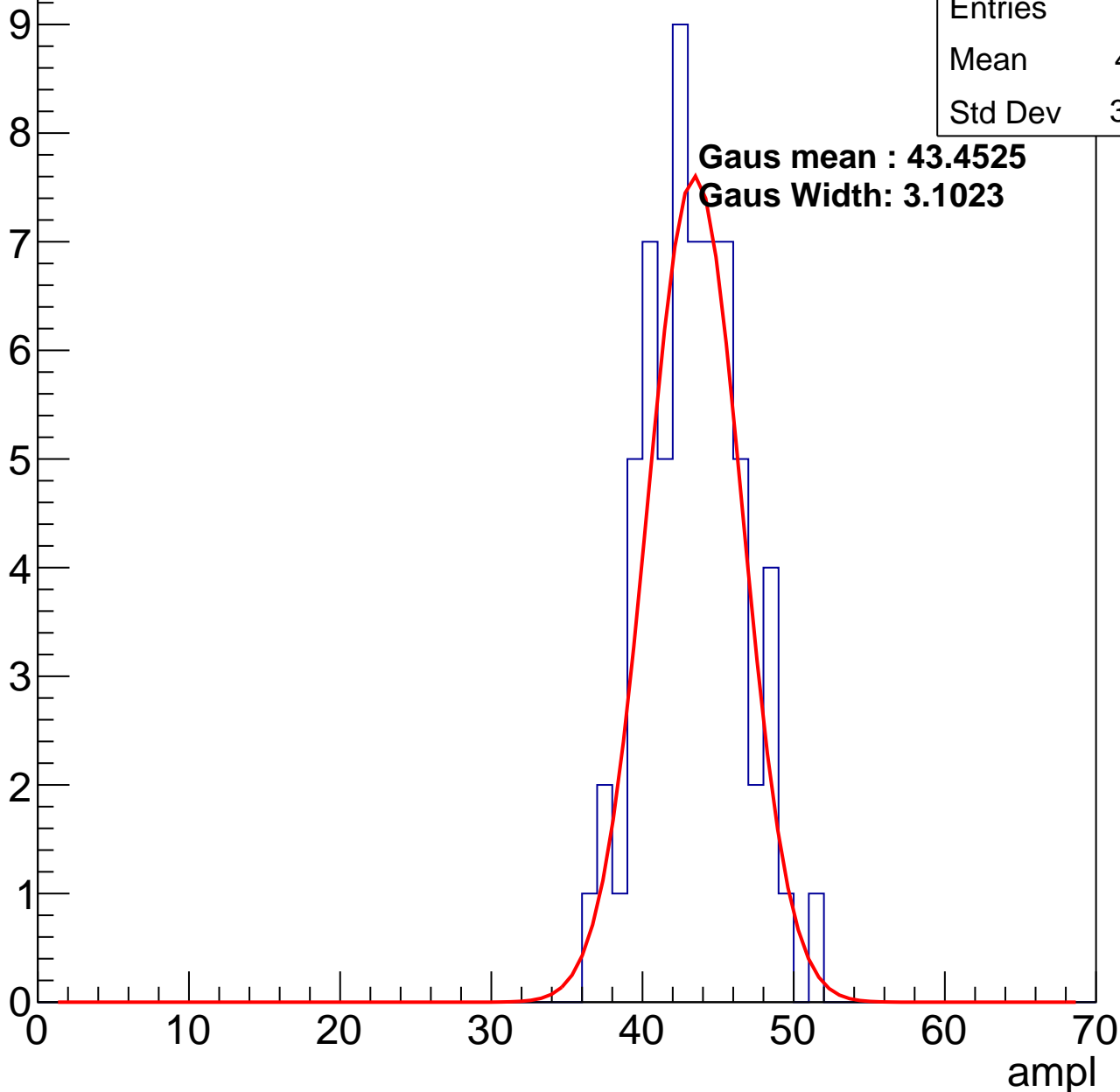
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	64
Mean	42.91
Std Dev	3.136

**Gaus mean : 43.4525**

**Gaus Width: 3.1023**

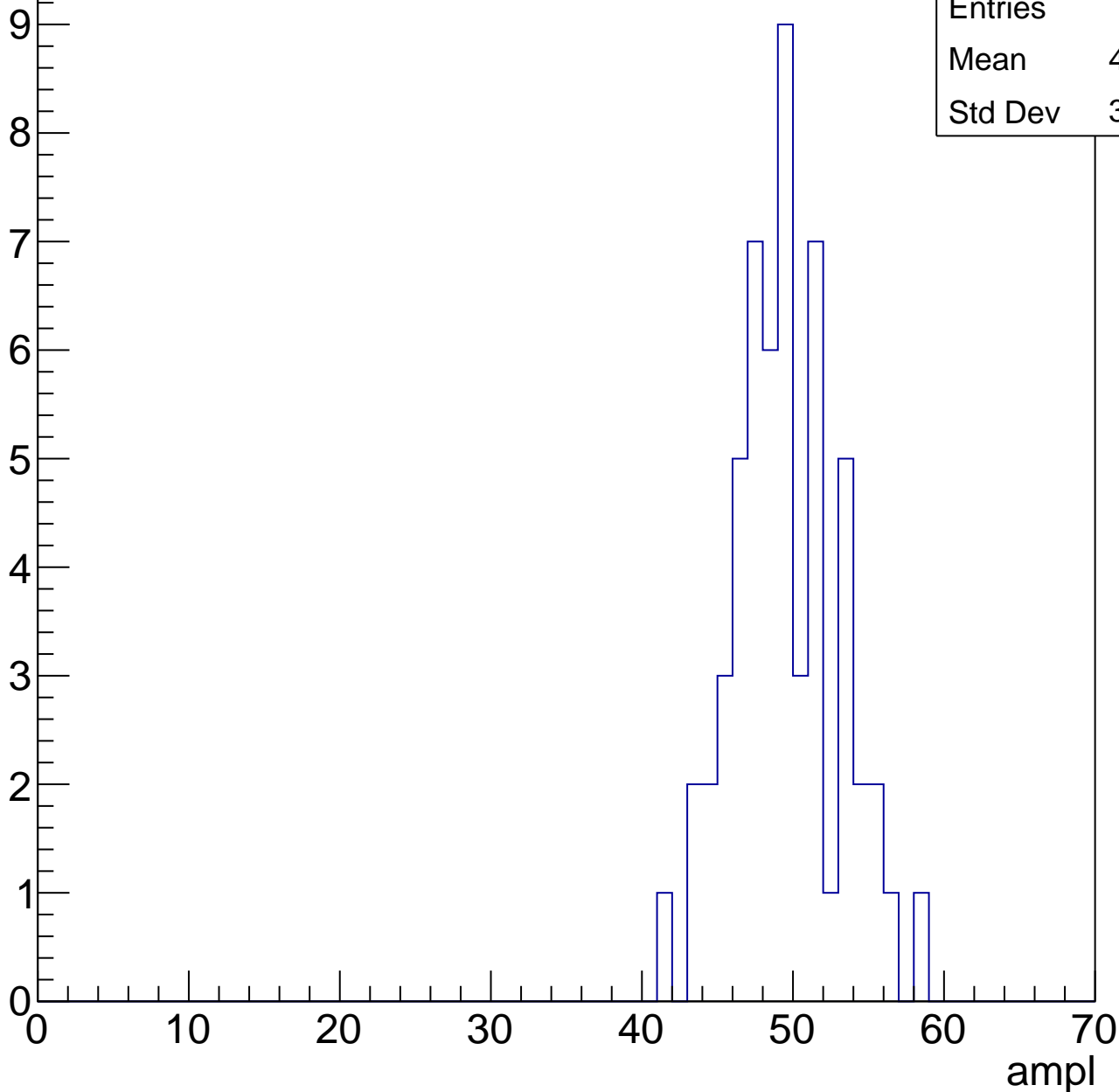


# B0L002S, U2-ch42, adc3

calib\_packv5\_042523\_0143.root, FC#8, port C1

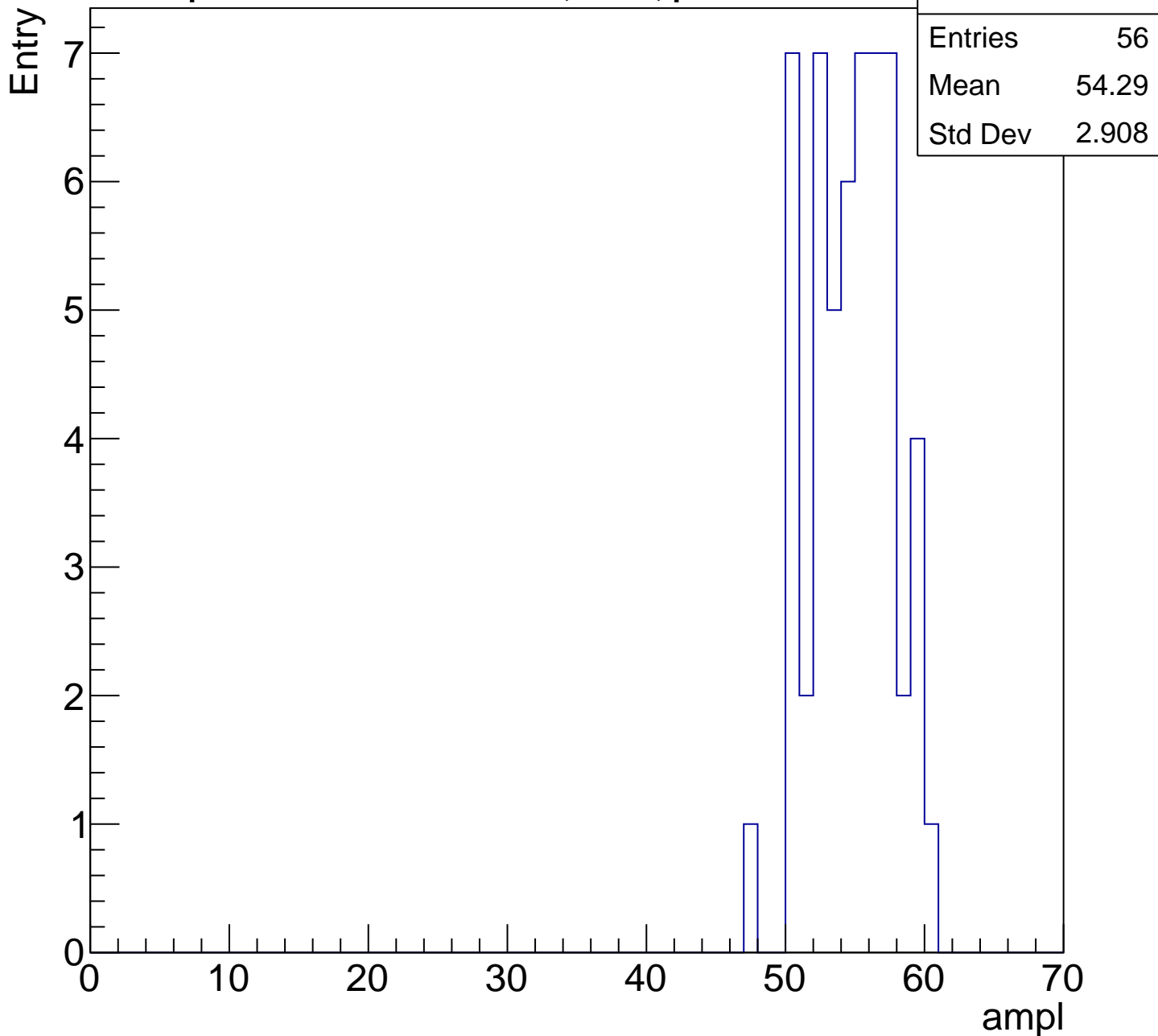
Entry

Entries	57
Mean	49.02
Std Dev	3.467



# B0L002S, U2-ch42, adc4

calib\_packv5\_042523\_0143.root, FC#8, port C1

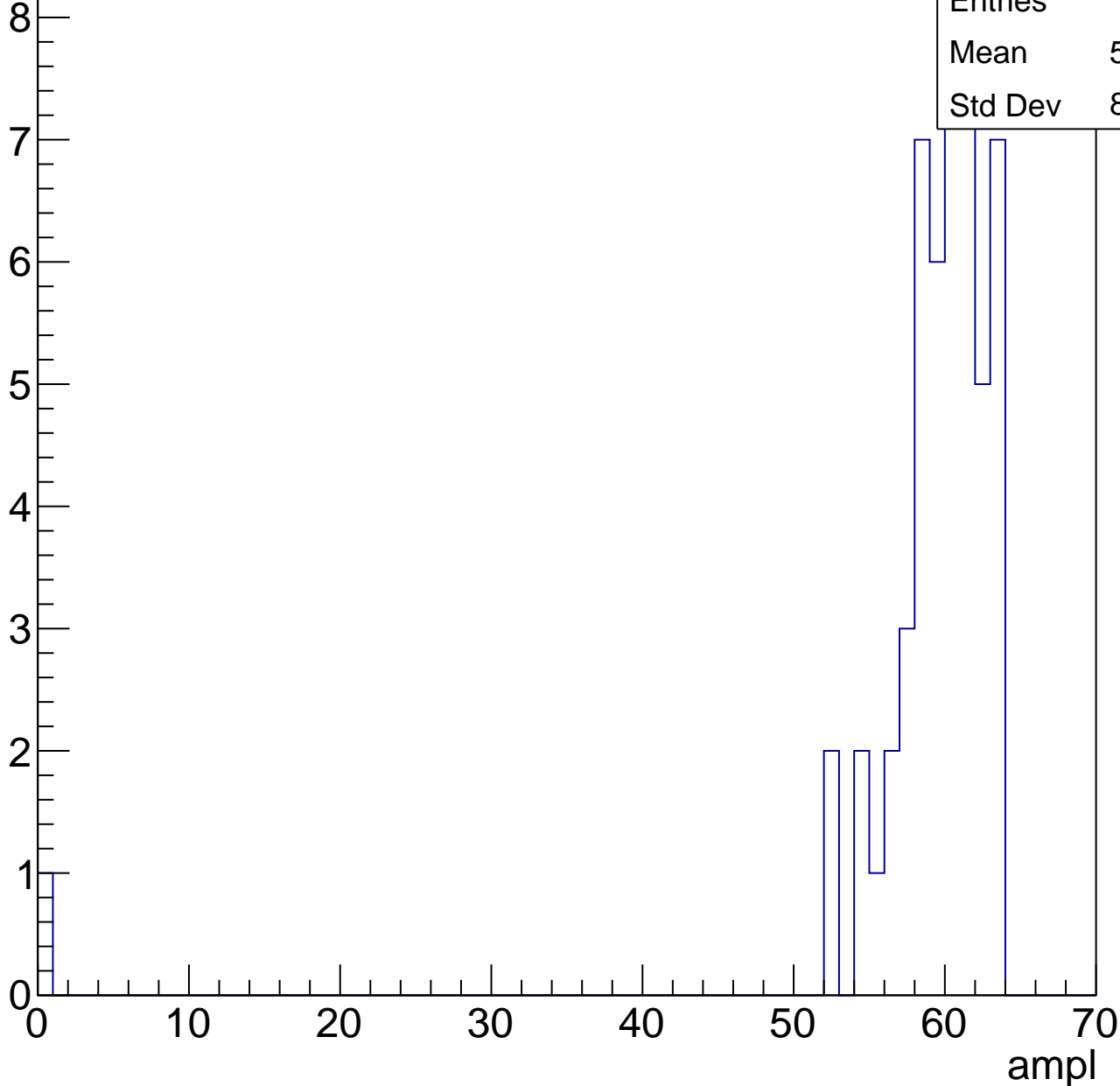


# B0L002S, U2-ch42, adc5

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	52
Mean	58.25
Std Dev	8.604

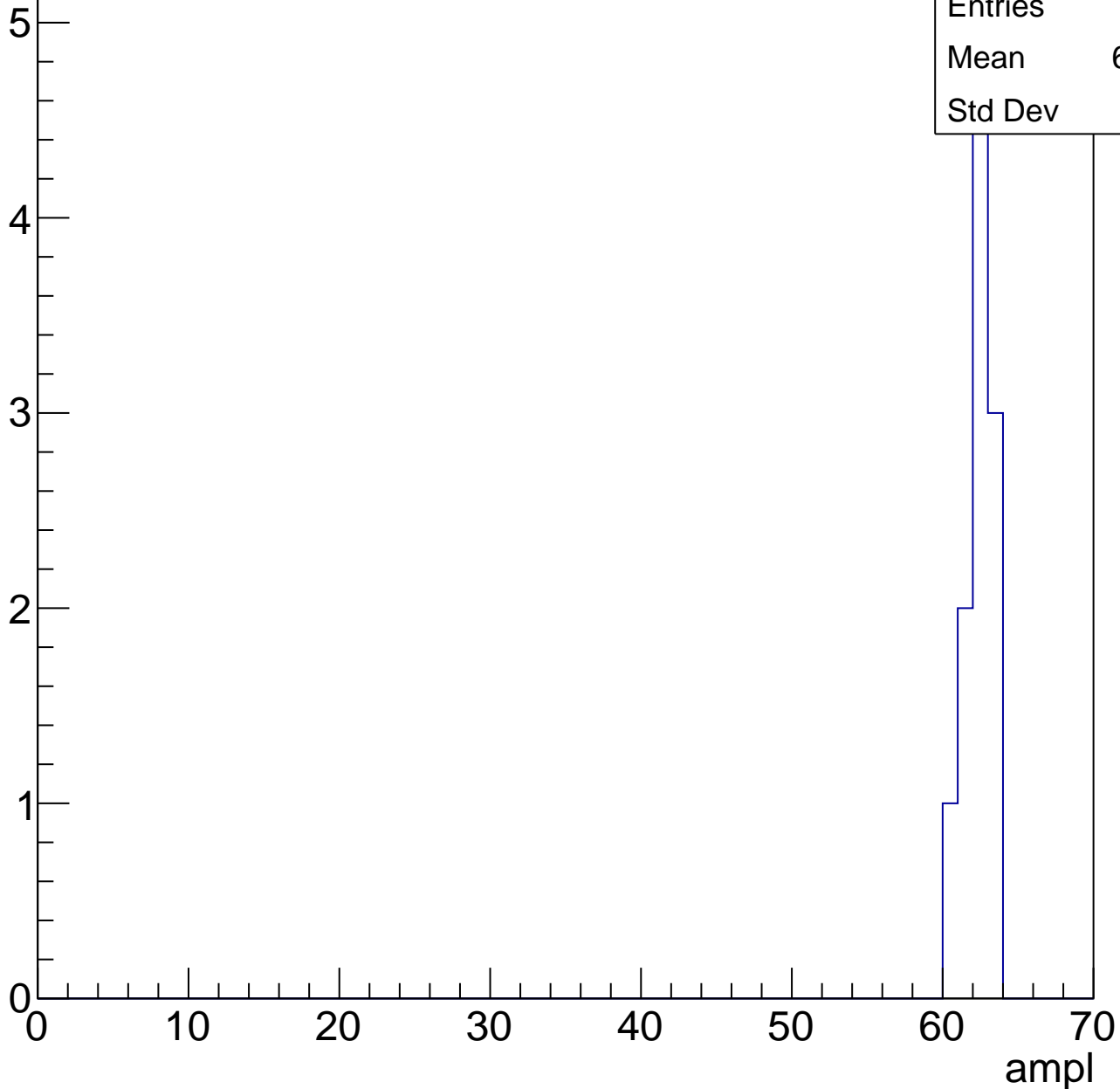


# B0L002S, U2-ch42, adc6

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	11
Mean	61.91
Std Dev	0.9





# B0L002S, U2-ch42, adc7

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L002S, U2-ch43, adc0

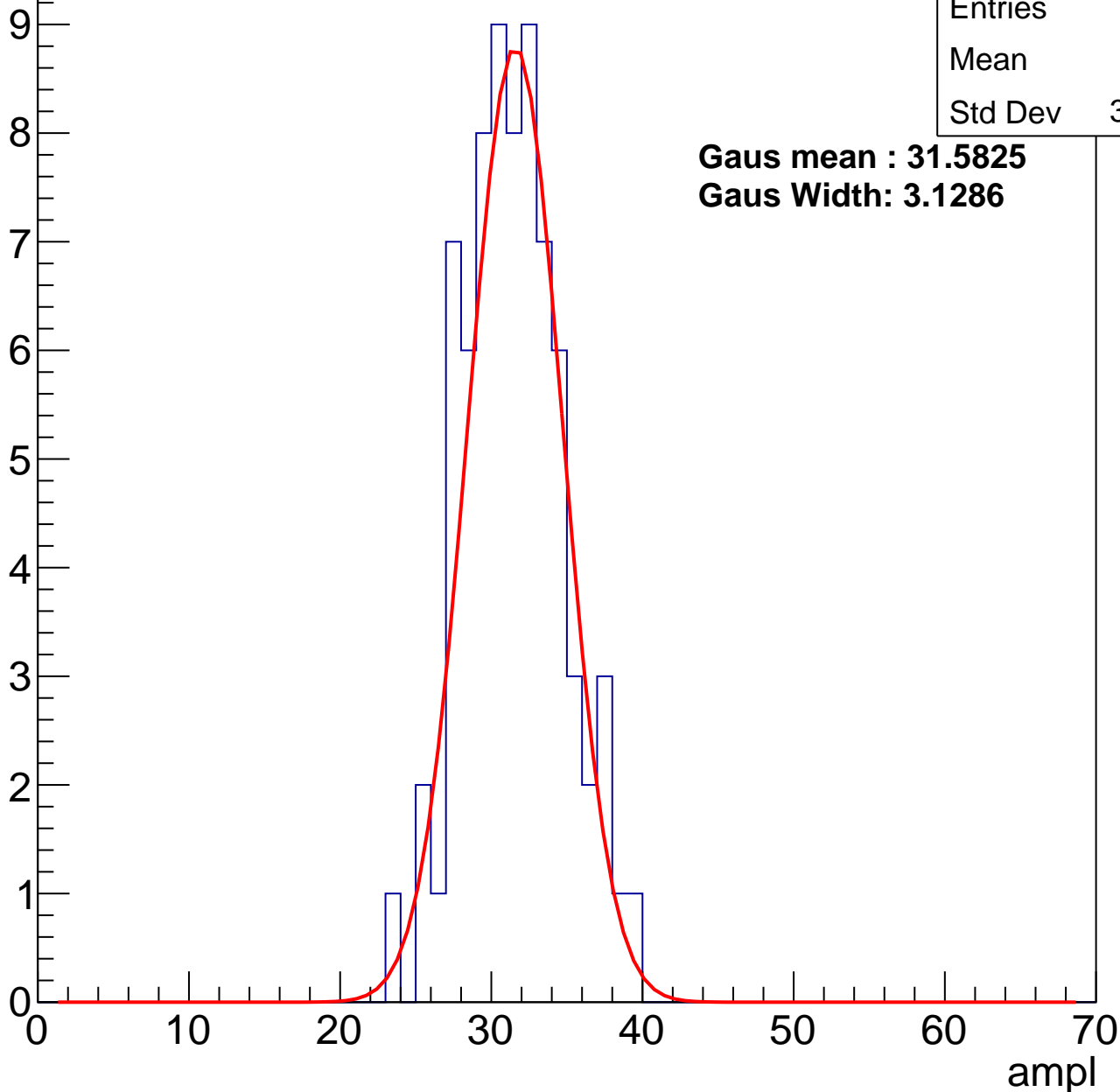
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	74
Mean	31
Std Dev	3.242

**Gaus mean : 31.5825**

**Gaus Width: 3.1286**



# B0L002S, U2-ch43, adc1

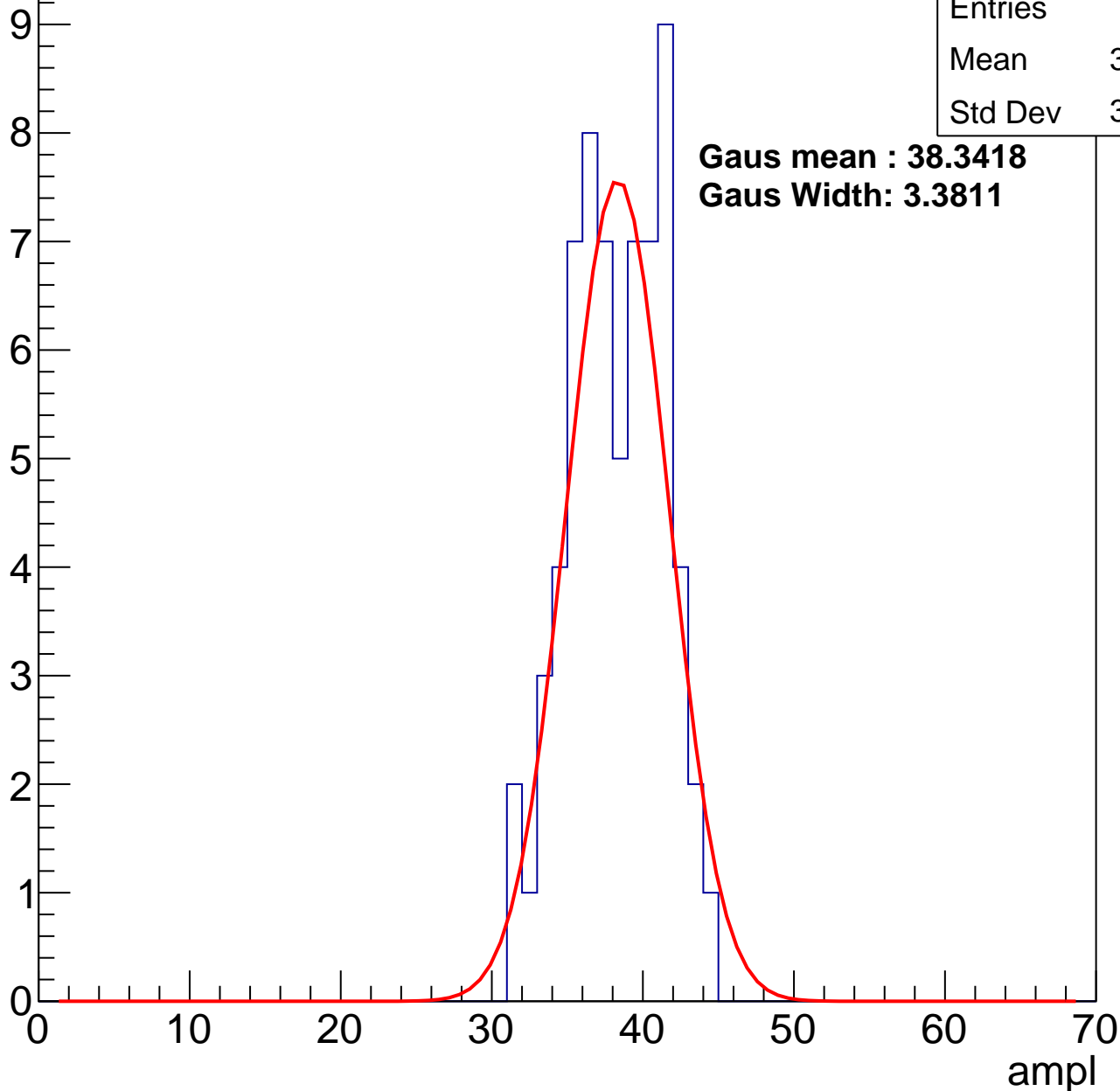
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	67
Mean	37.78
Std Dev	3.085

**Gaus mean : 38.3418**

**Gaus Width: 3.3811**



# B0L002S, U2-ch43, adc2

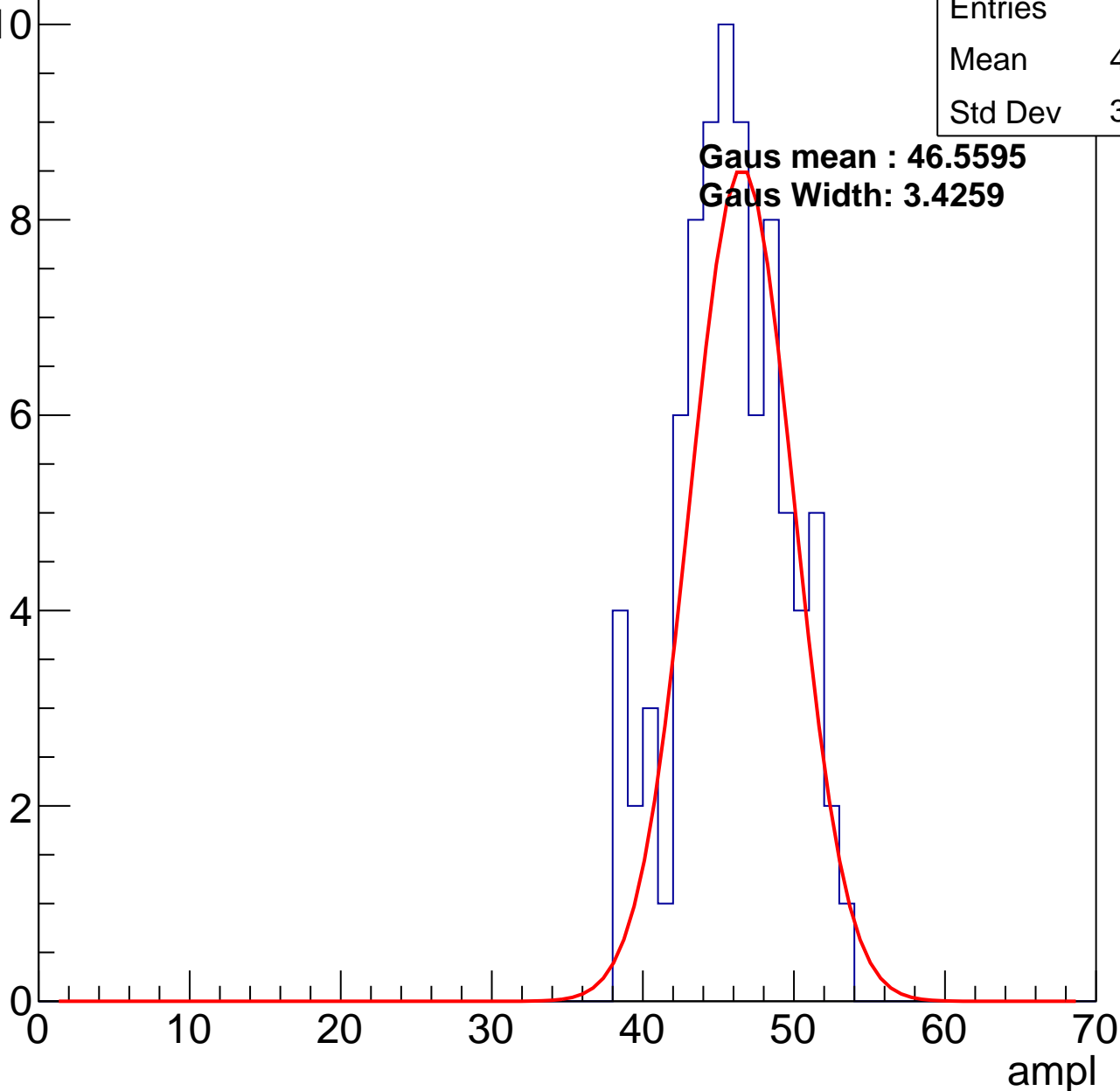
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	83
Mean	45.42
Std Dev	3.584

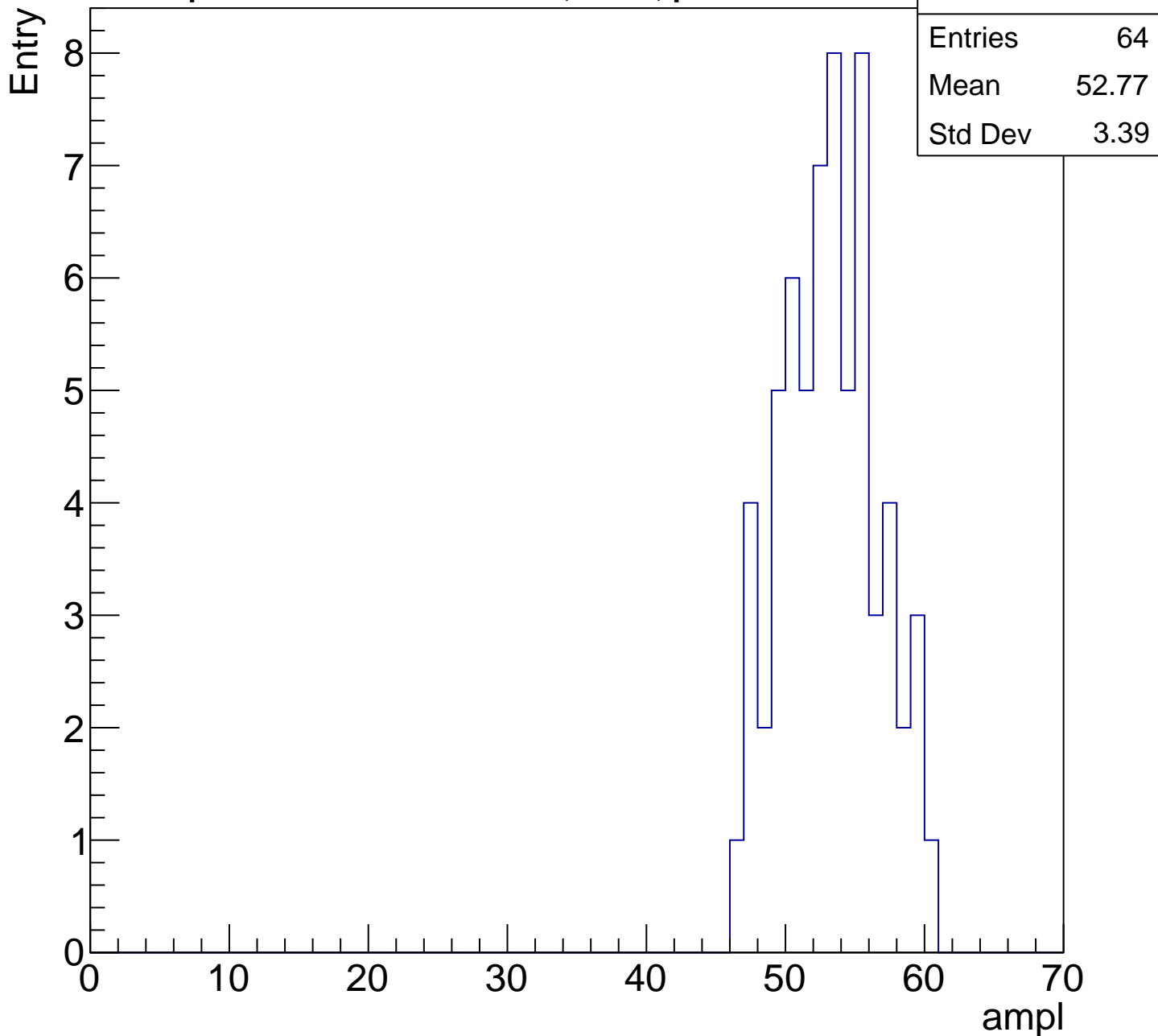
**Gaus mean : 46.5595**

**Gaus Width: 3.4259**



# B0L002S, U2-ch43, adc3

calib\_packv5\_042523\_0143.root, FC#8, port C1

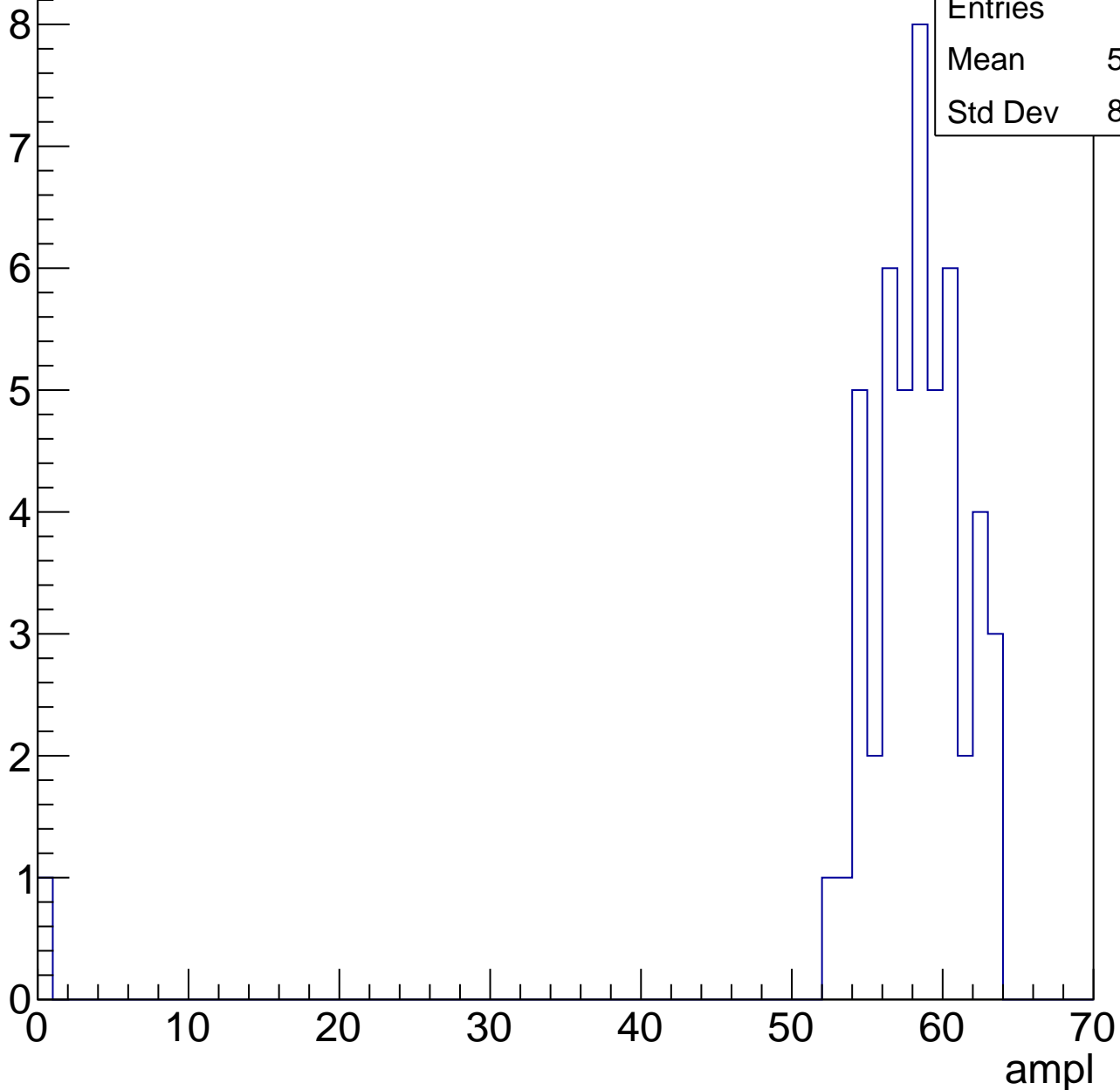


# B0L002S, U2-ch43, adc4

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	49
Mean	56.82
Std Dev	8.654

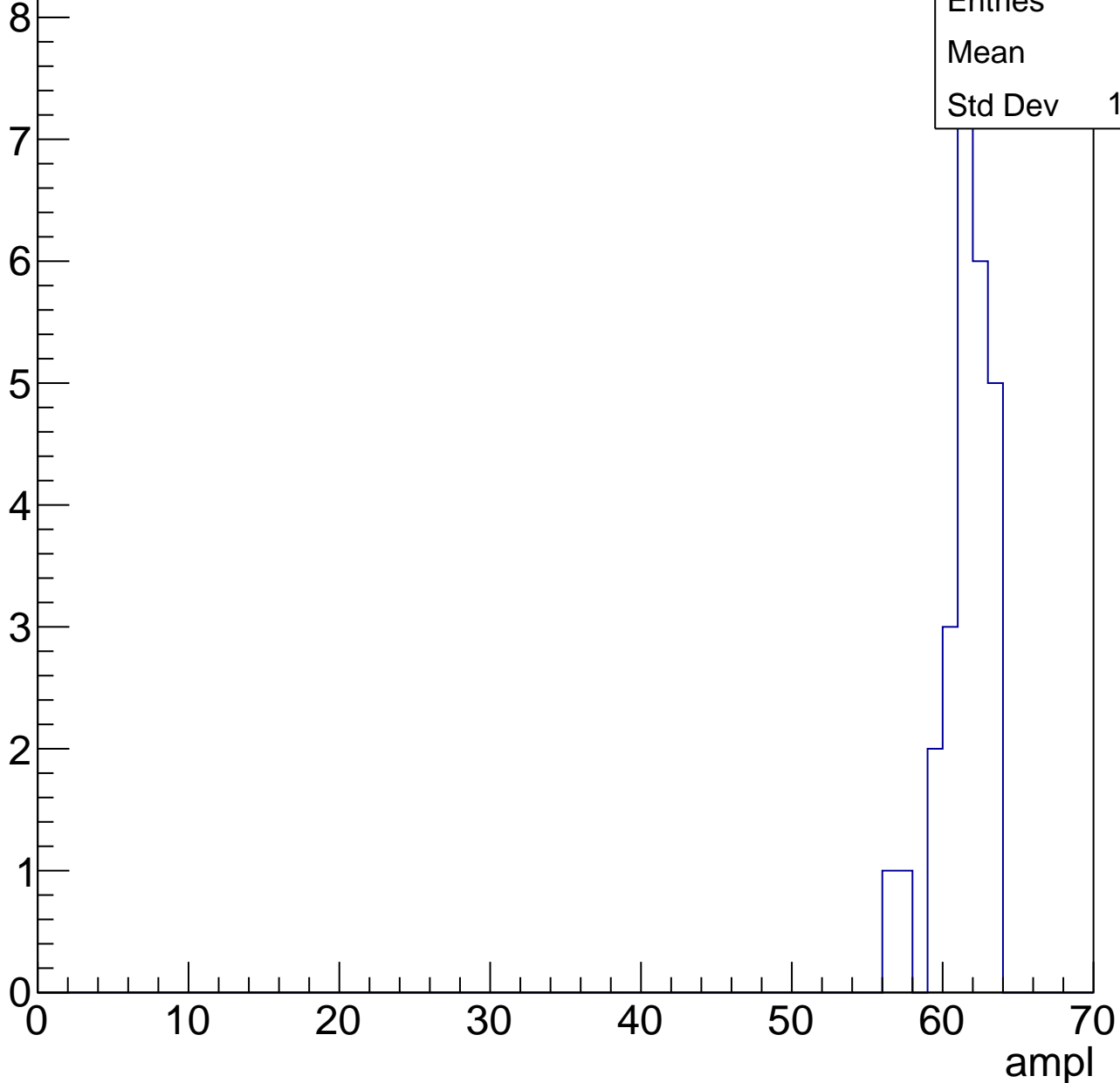


# B0L002S, U2-ch43, adc5

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	26
Mean	61
Std Dev	1.732



# B0L002S, U2-ch43, adc6

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry





# B0L002S, U2-ch43, adc7

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



# B0L002S, U2-ch44, adc0

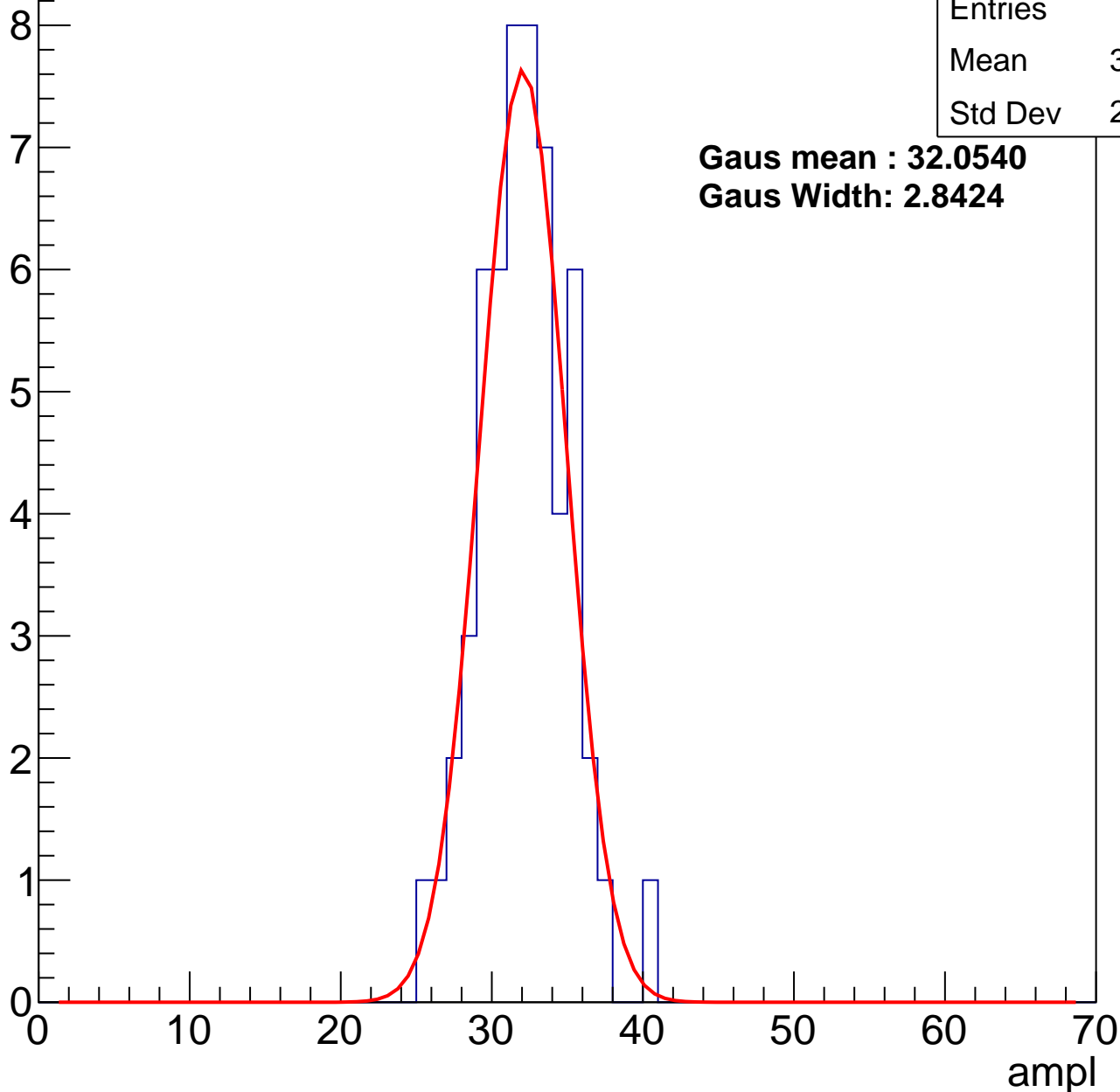
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	56
Mean	31.66
Std Dev	2.868

**Gaus mean : 32.0540**

**Gaus Width: 2.8424**



# B0L002S, U2-ch44, adc1

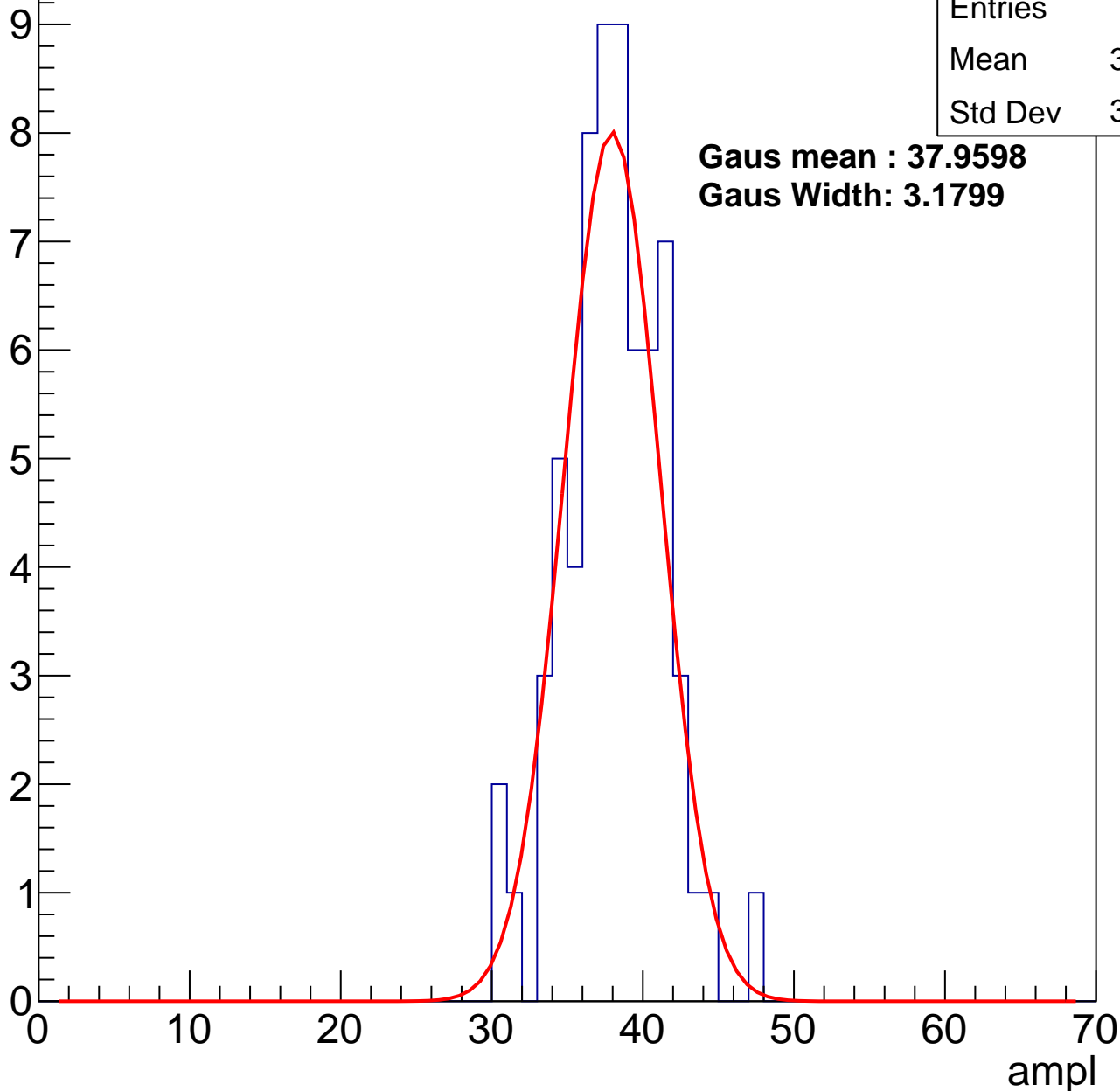
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	66
Mean	37.64
Std Dev	3.218

**Gaus mean : 37.9598**

**Gaus Width: 3.1799**



# B0L002S, U2-ch44, adc2

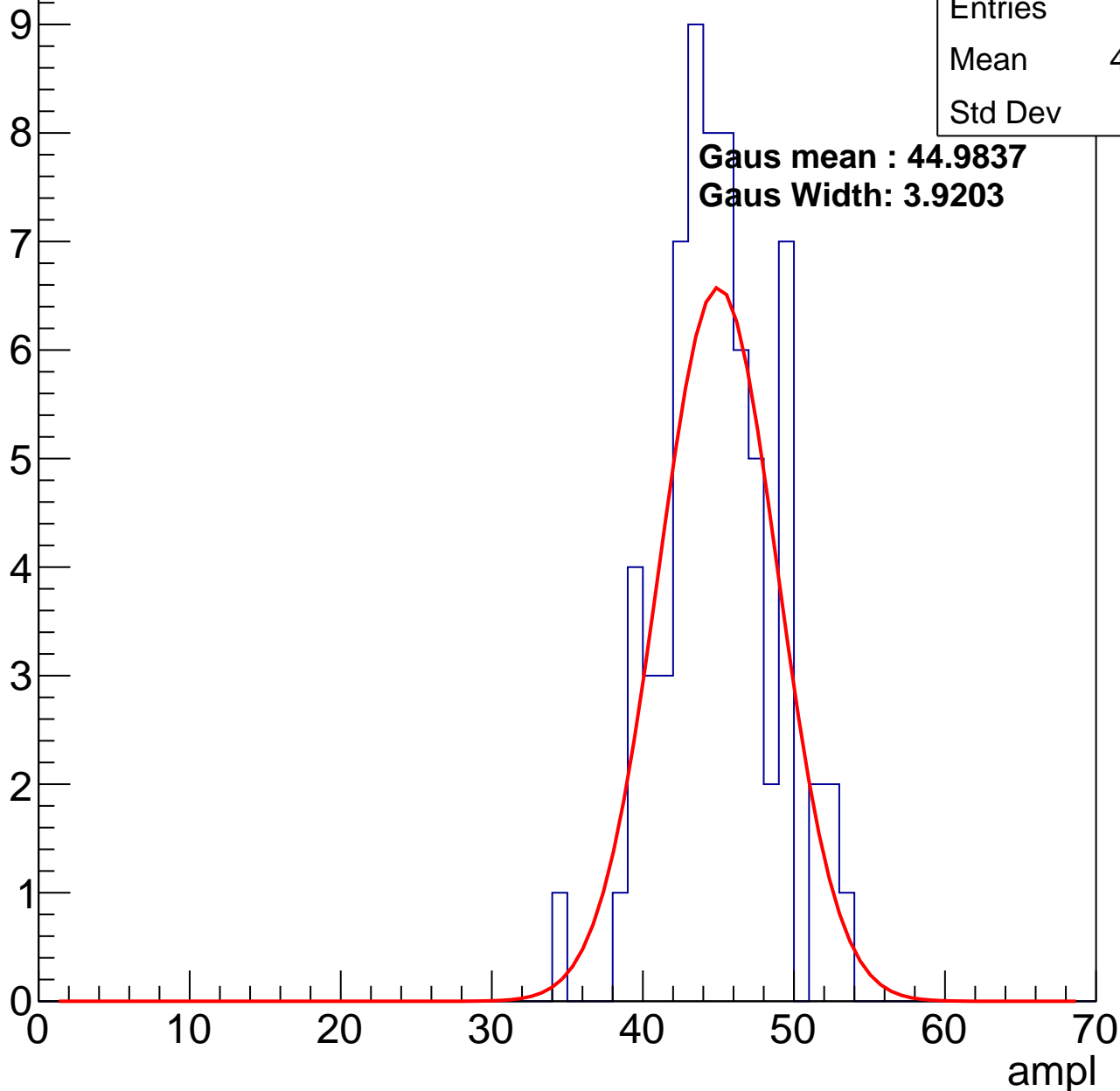
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	69
Mean	44.54
Std Dev	3.65

**Gaus mean : 44.9837**

**Gaus Width: 3.9203**



# B0L002S, U2-ch44, adc3

calib\_packv5\_042523\_0143.root, FC#8, port C1

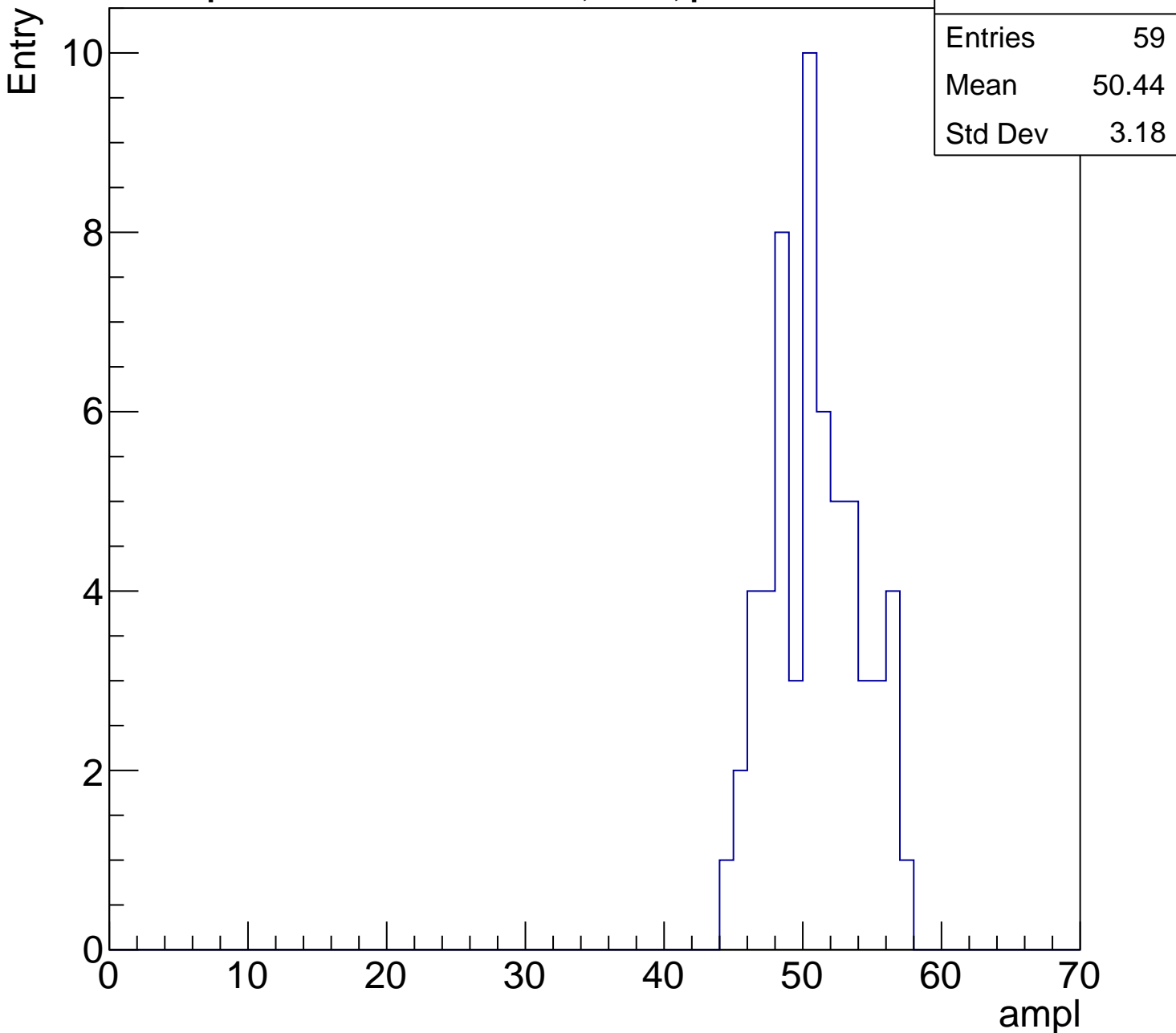
Entries	59
Mean	50.44
Std Dev	3.18

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

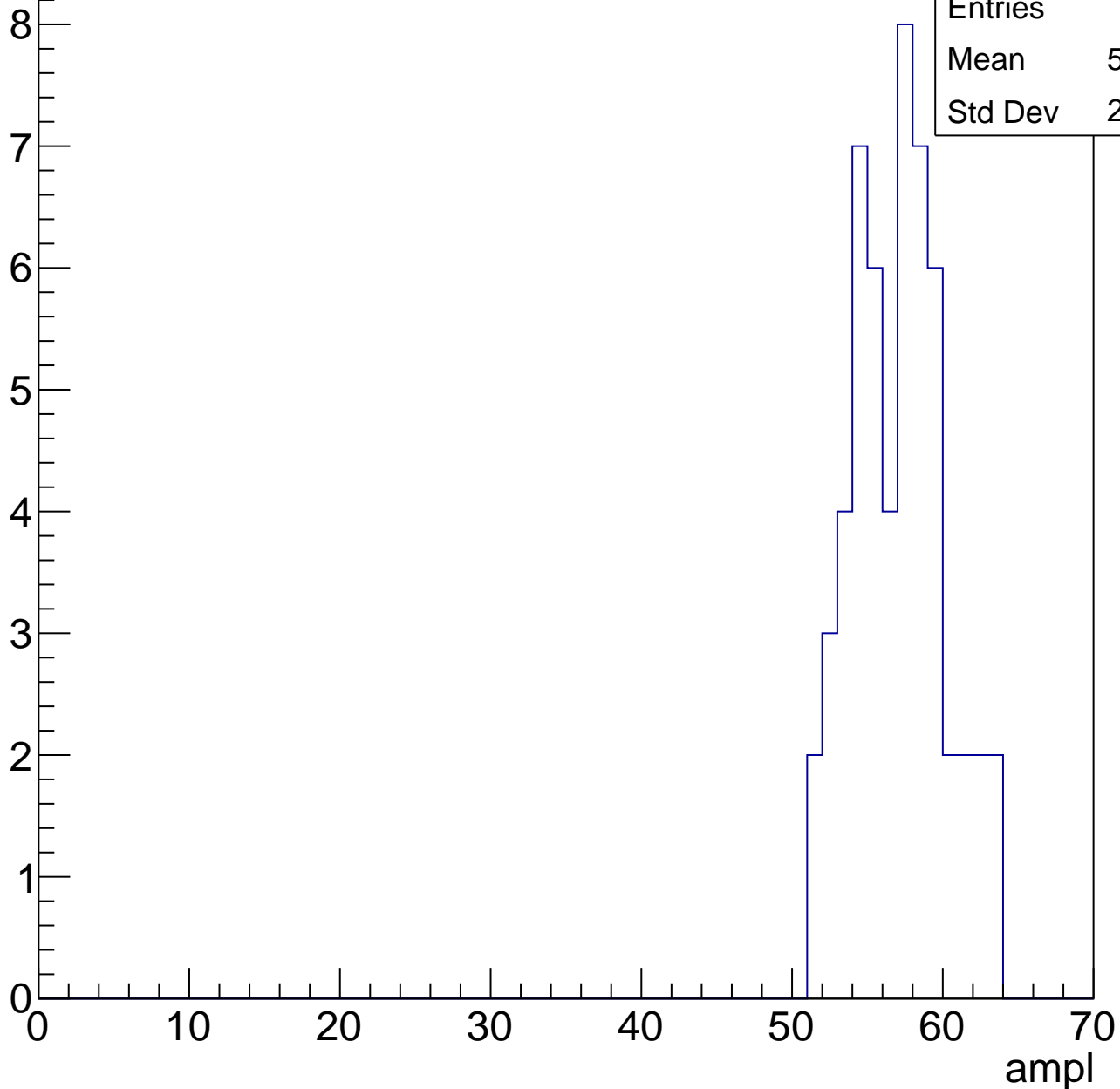


# B0L002S, U2-ch44, adc4

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

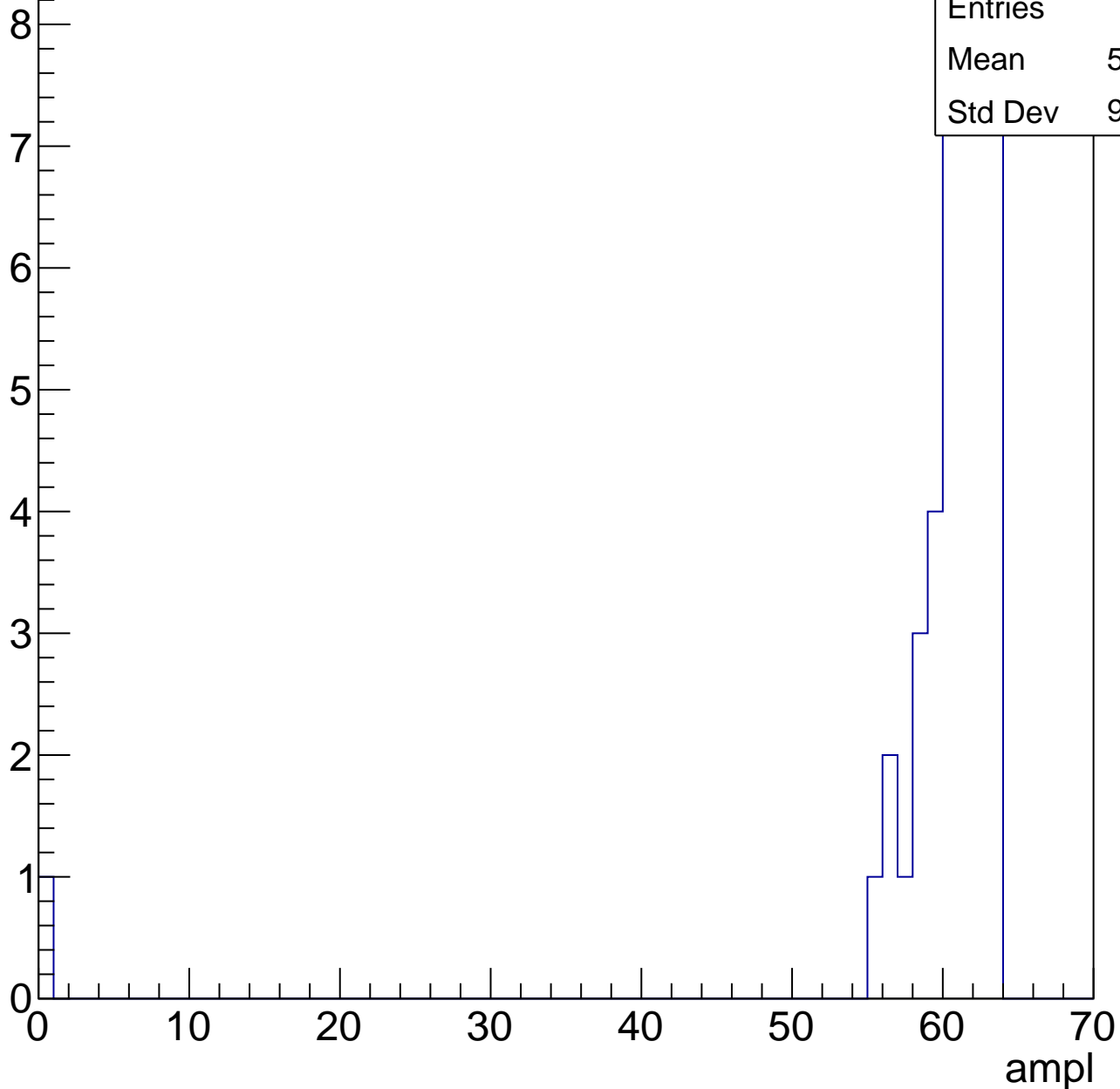
Entries	55
Mean	56.55
Std Dev	2.996



# B0L002S, U2-ch44, adc5

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



# B0L002S, U2-ch44, adc6

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



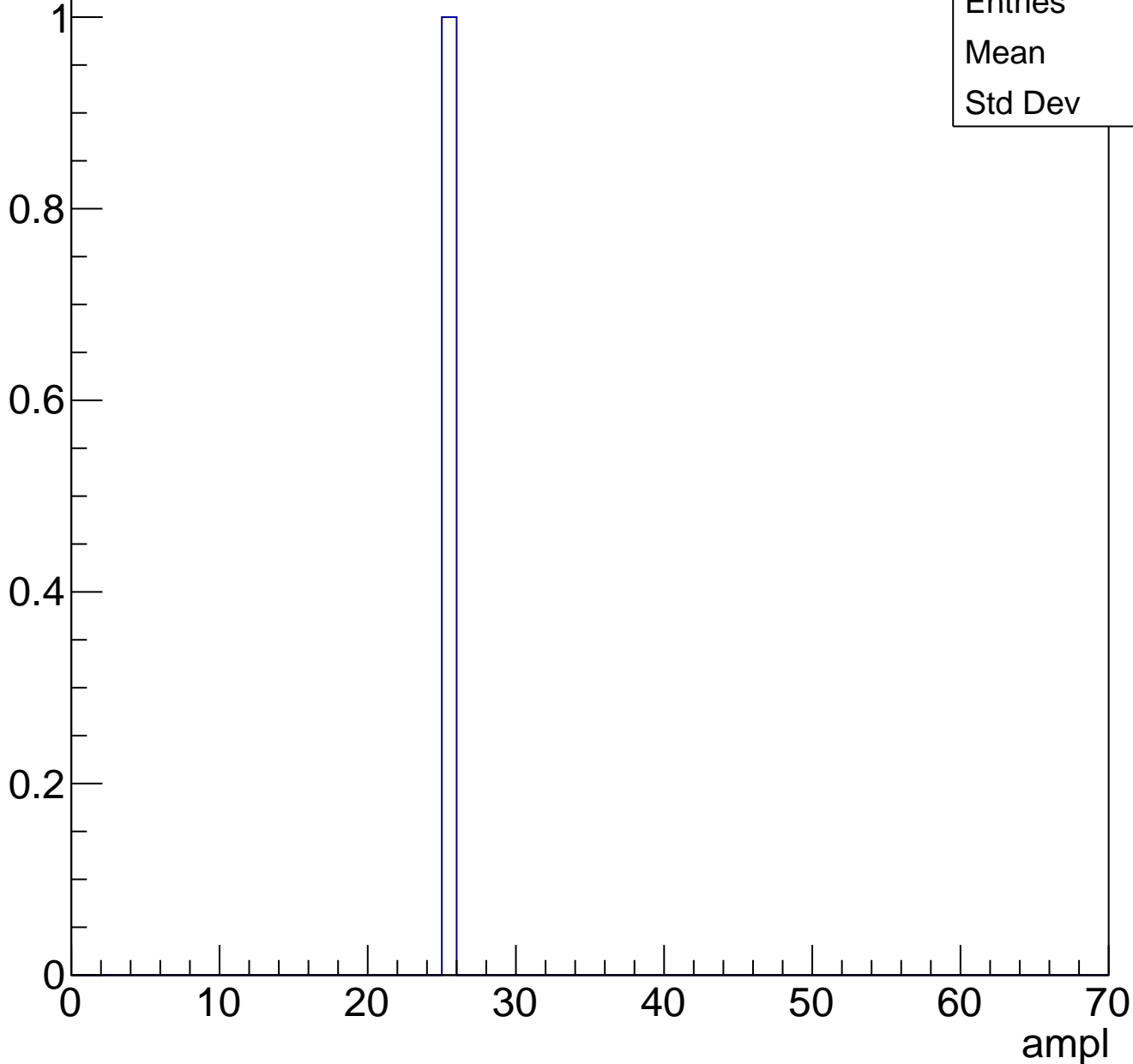
Entries	0
Mean	0
Std Dev	0



# B0L002S, U2-ch44, adc7

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



# B0L002S, U2-ch45, adc0

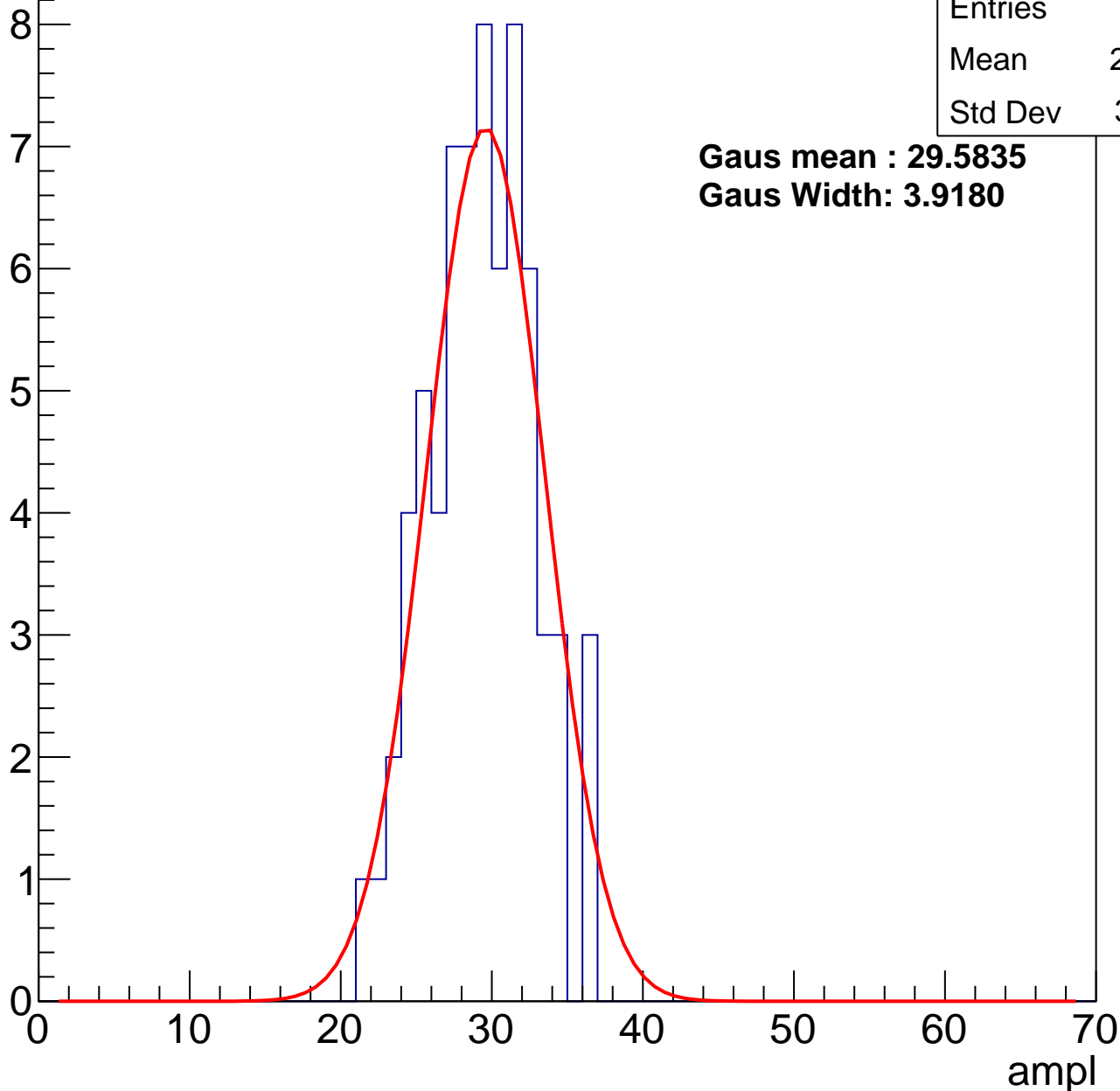
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	68
Mean	28.82
Std Dev	3.421

**Gaus mean : 29.5835**

**Gaus Width: 3.9180**



# B0L002S, U2-ch45, adc1

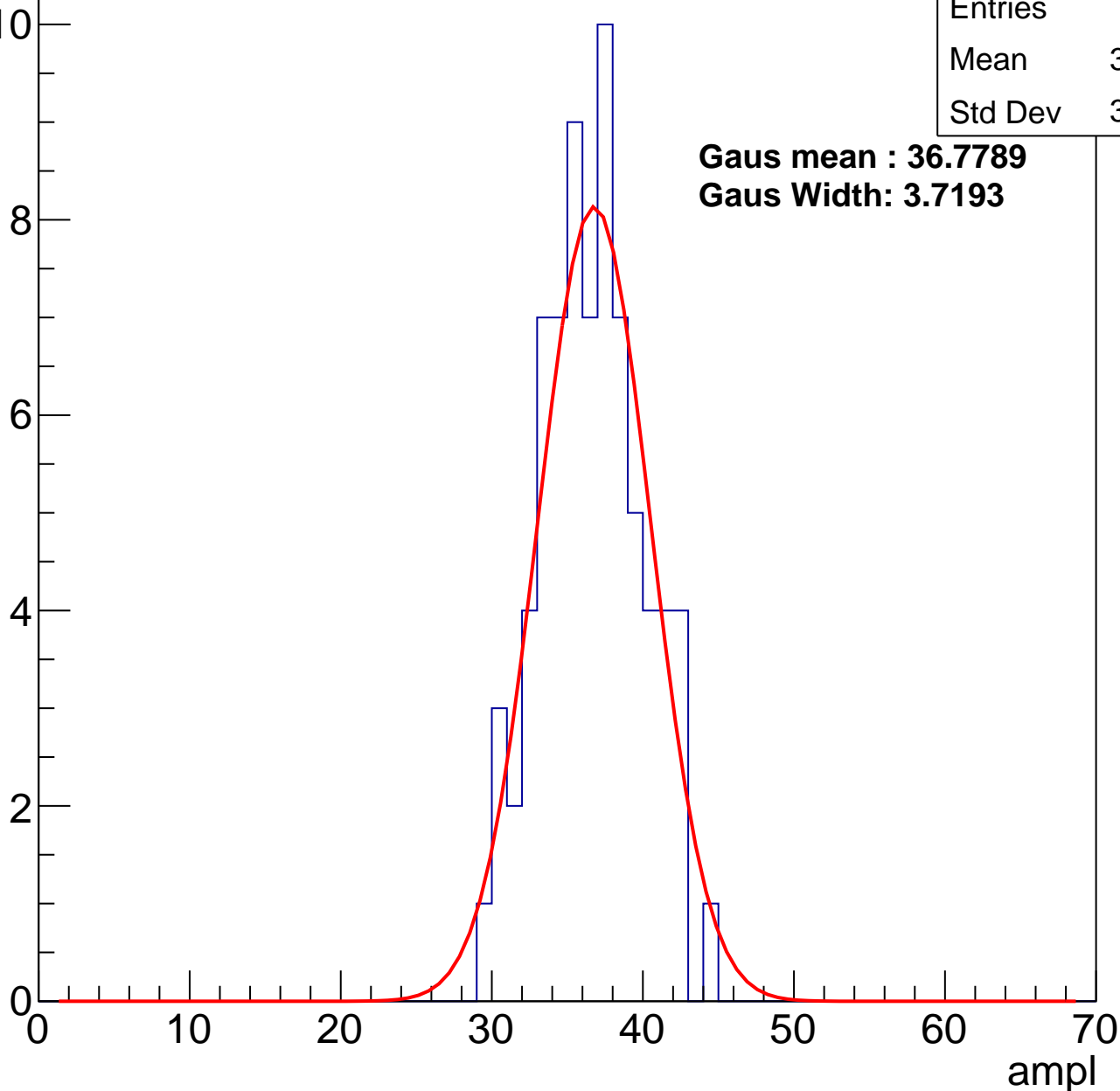
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	75
Mean	36.16
Std Dev	3.315

**Gaus mean : 36.7789**

**Gaus Width: 3.7193**



# B0L002S, U2-ch45, adc2

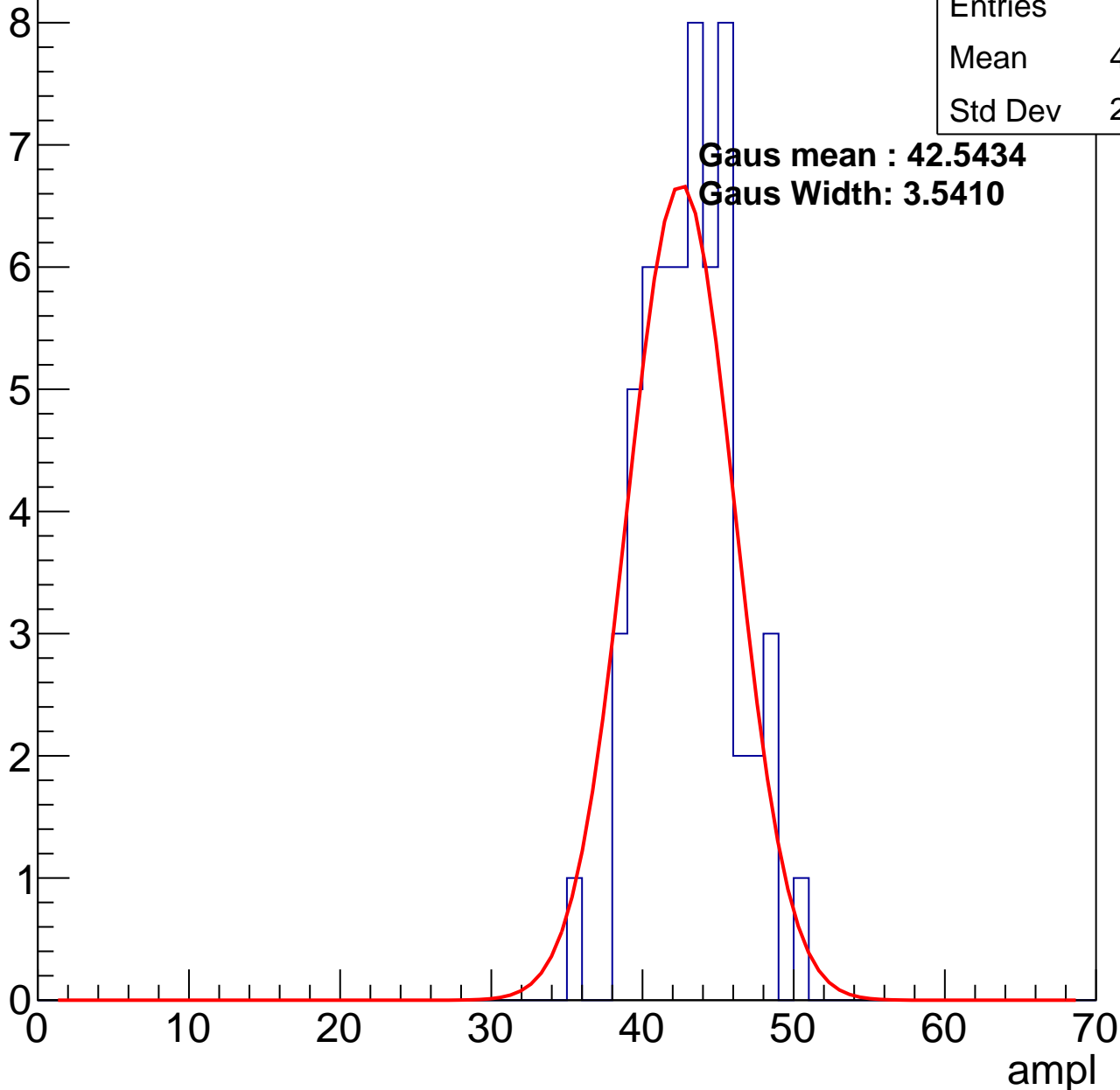
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	57
Mean	42.63
Std Dev	2.983

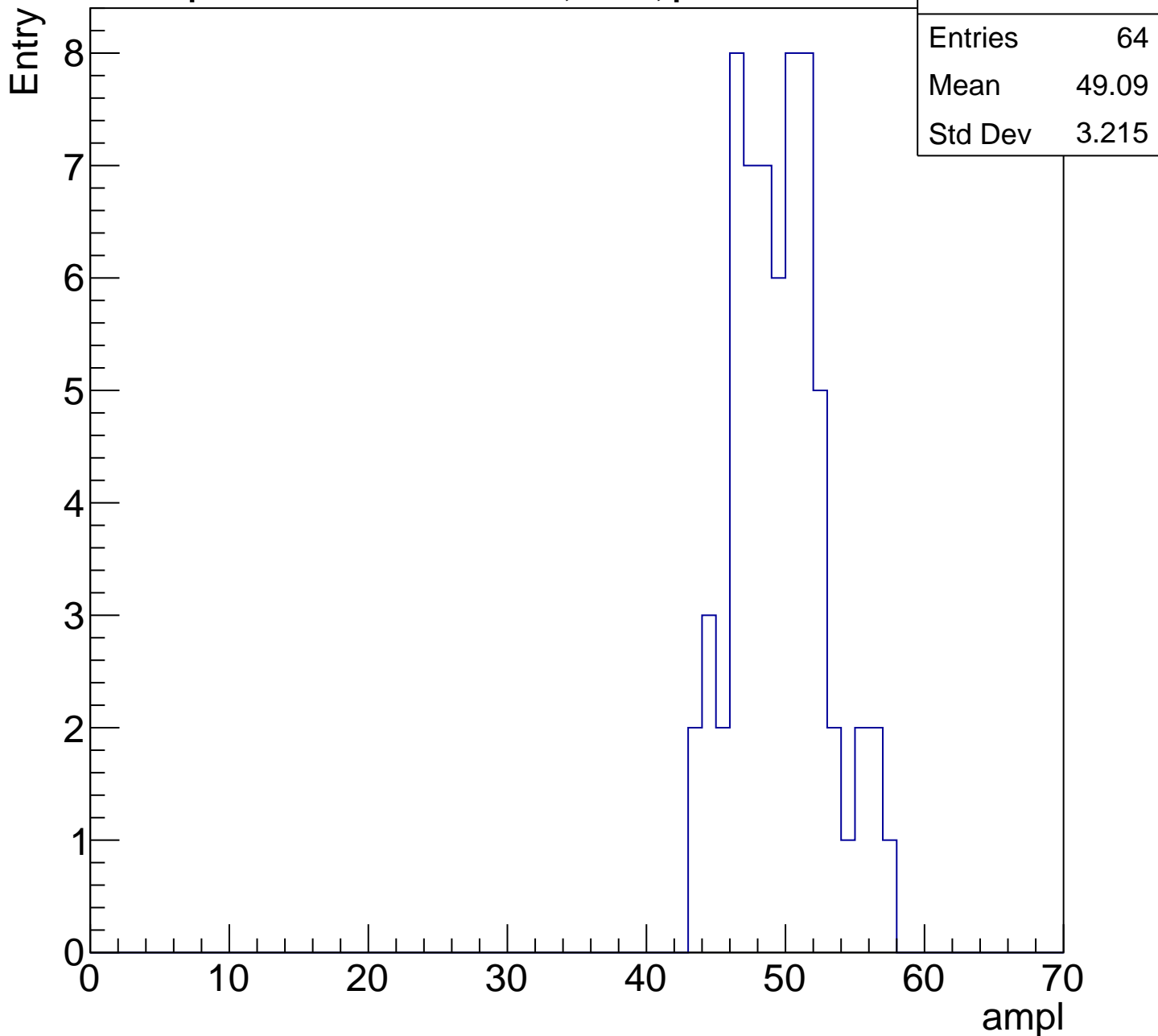
**Gaus mean : 42.5434**

**Gaus Width: 3.5410**



# B0L002S, U2-ch45, adc3

calib\_packv5\_042523\_0143.root, FC#8, port C1

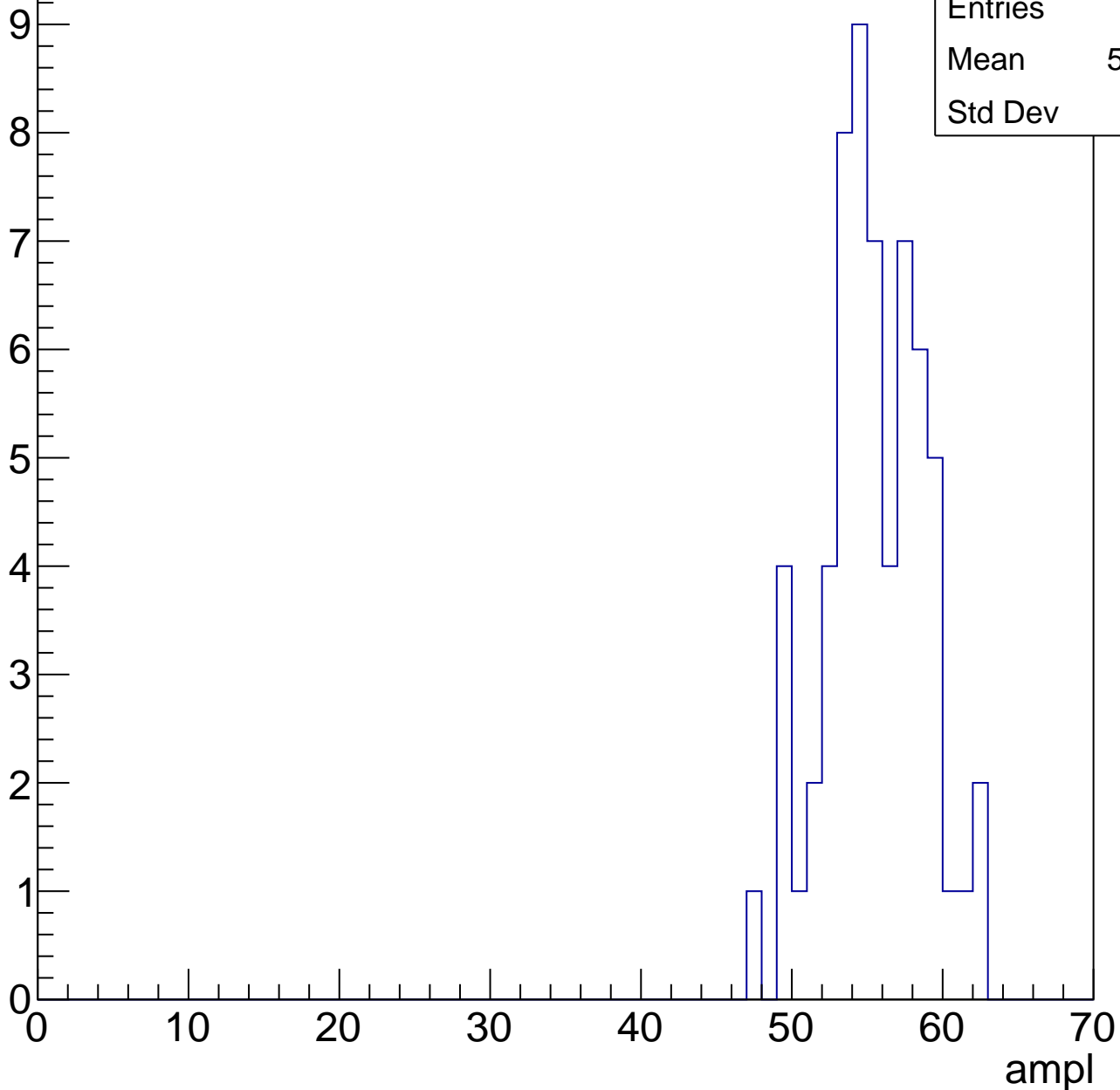


# B0L002S, U2-ch45, adc4

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	62
Mean	54.98
Std Dev	3.28

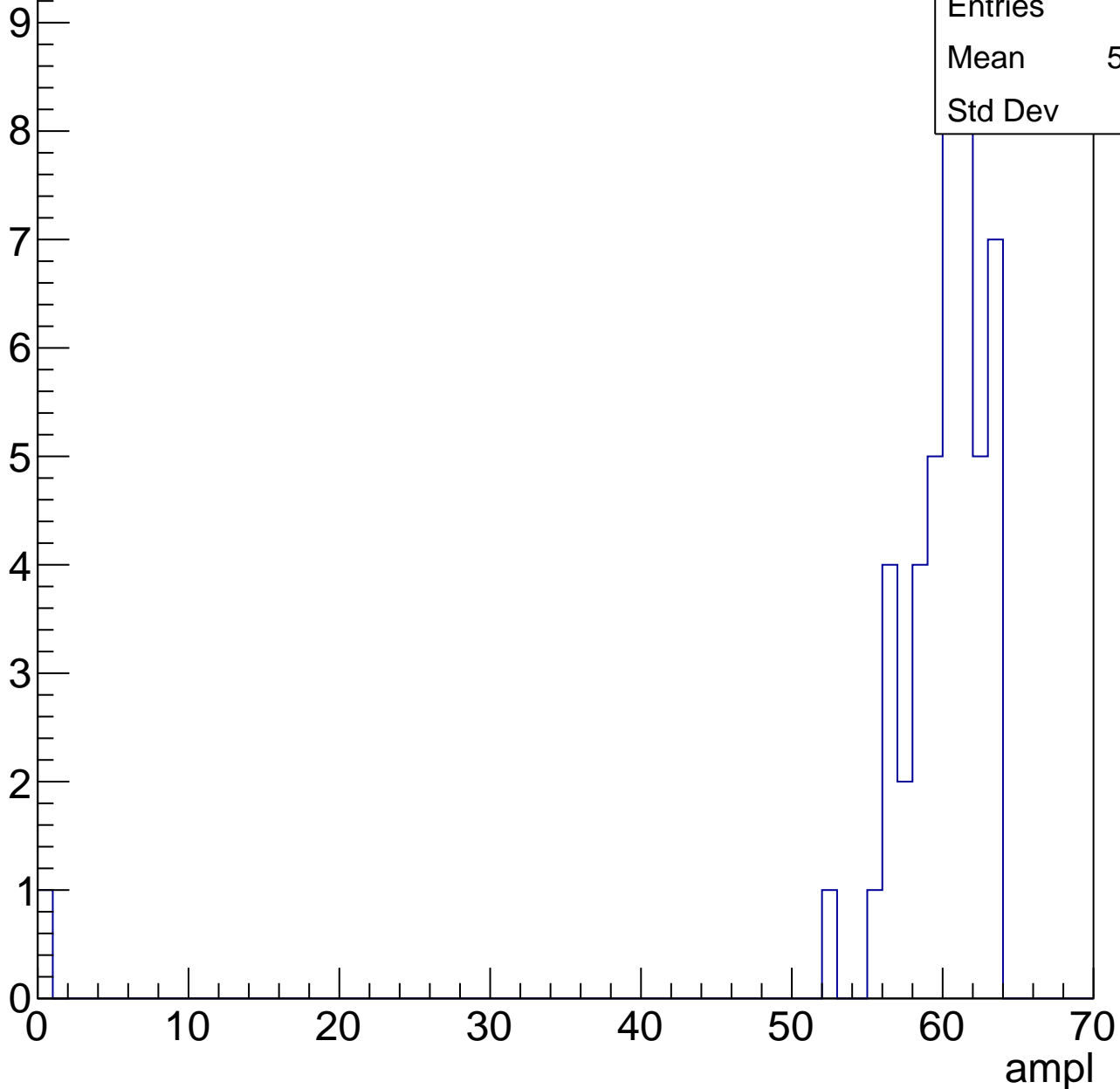


# B0L002S, U2-ch45, adc5

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	47
Mean	58.53
Std Dev	8.97



# B0L002S, U2-ch45, adc6

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry





# B0L002S, U2-ch45, adc7

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L002S, U2-ch46, adc0

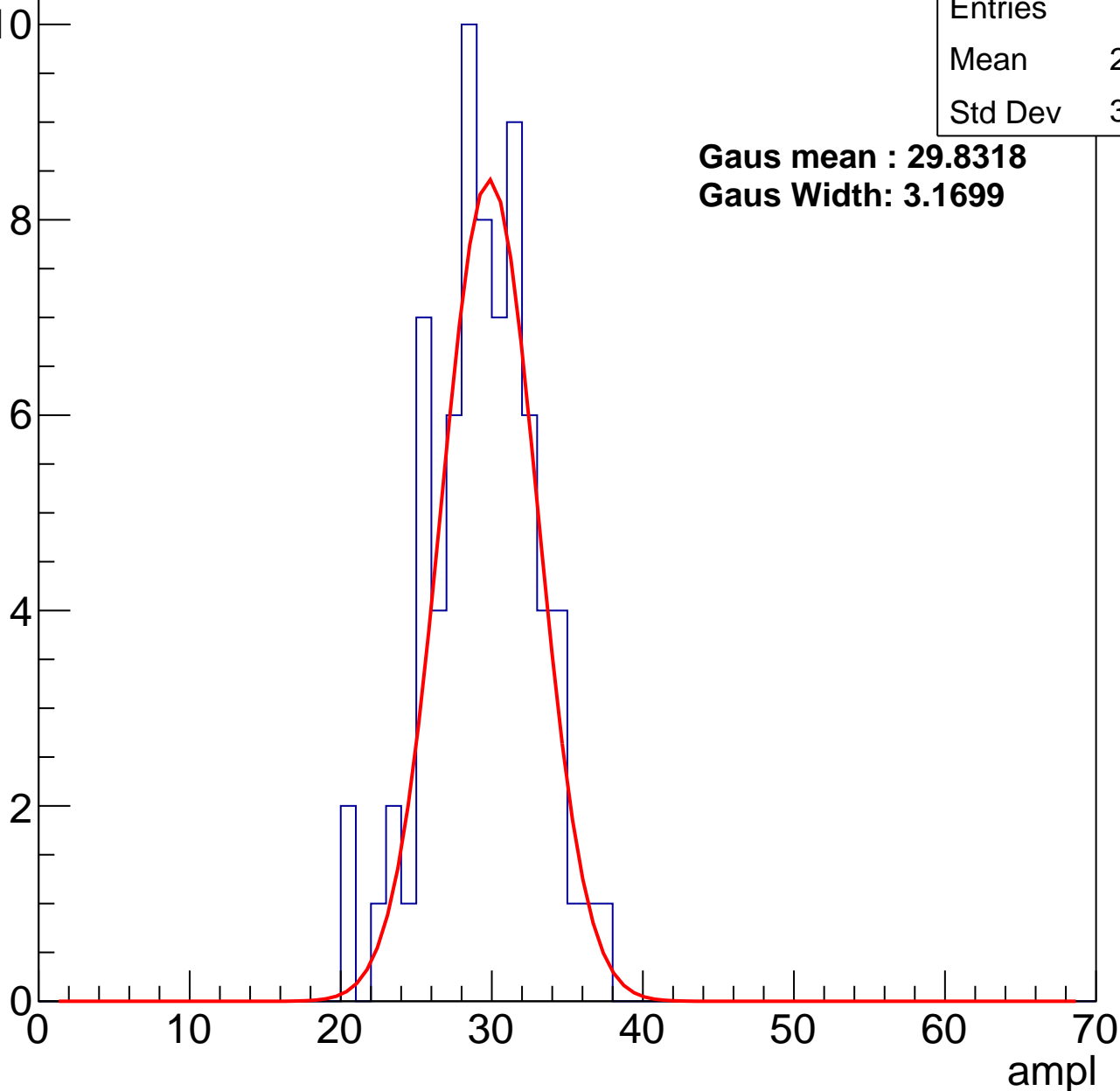
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	74
Mean	28.95
Std Dev	3.487

**Gaus mean : 29.8318**

**Gaus Width: 3.1699**



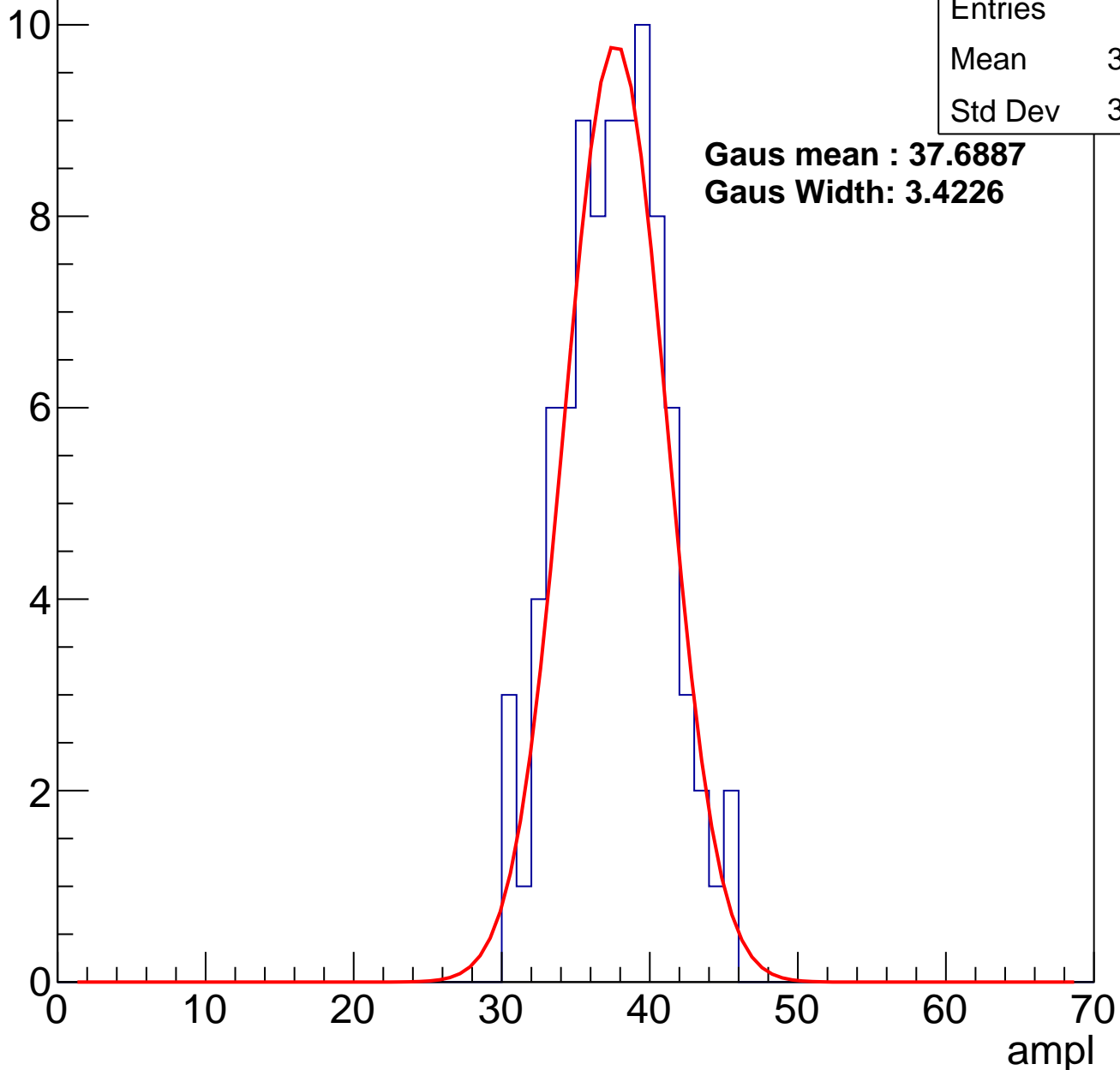
# B0L002S, U2-ch46, adc1

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entries	87
Mean	37.14
Std Dev	3.418

**Gaus mean : 37.6887**  
**Gaus Width: 3.4226**

Entry



# B0L002S, U2-ch46, adc2

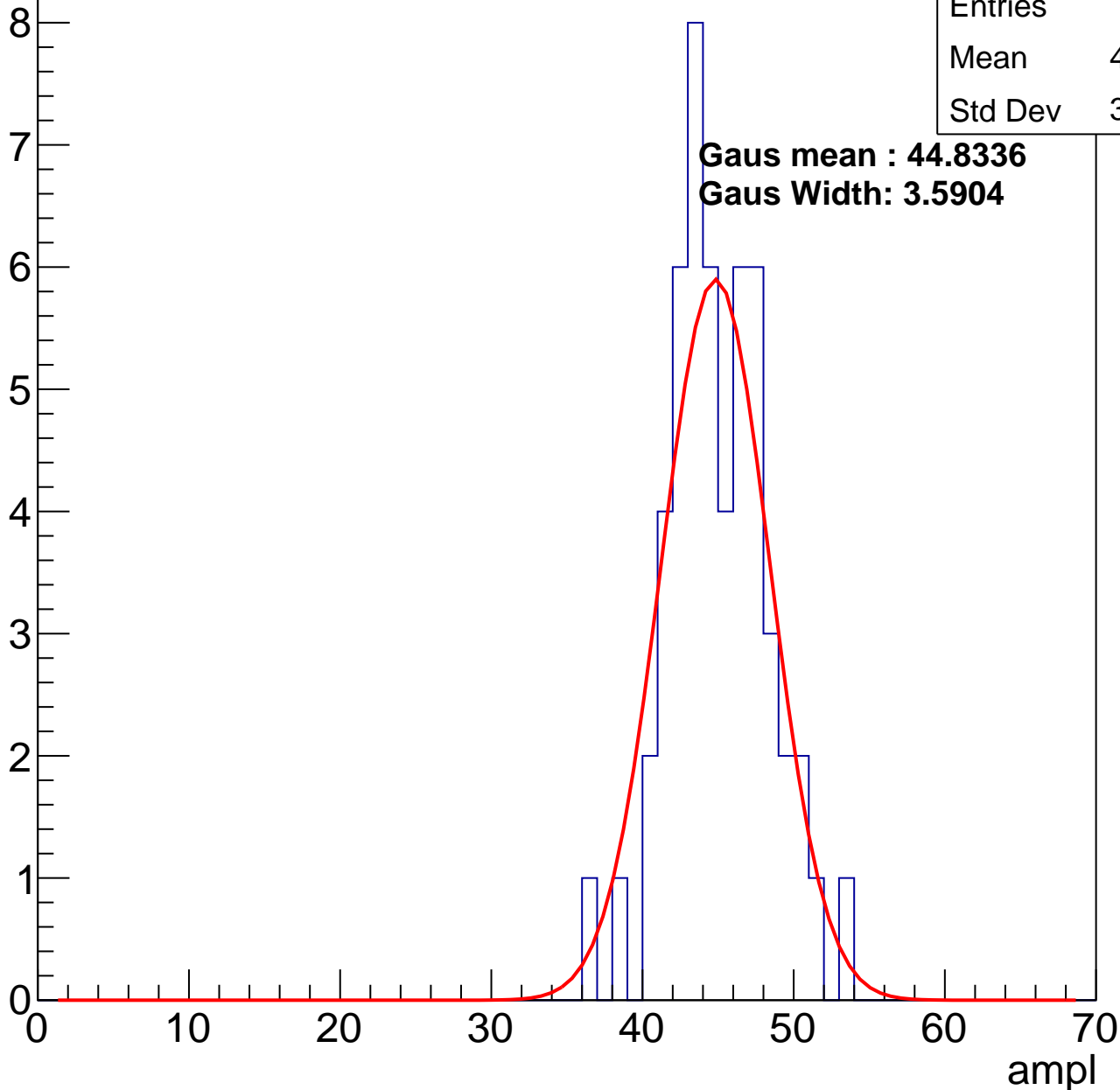
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	53
Mean	44.57
Std Dev	3.265

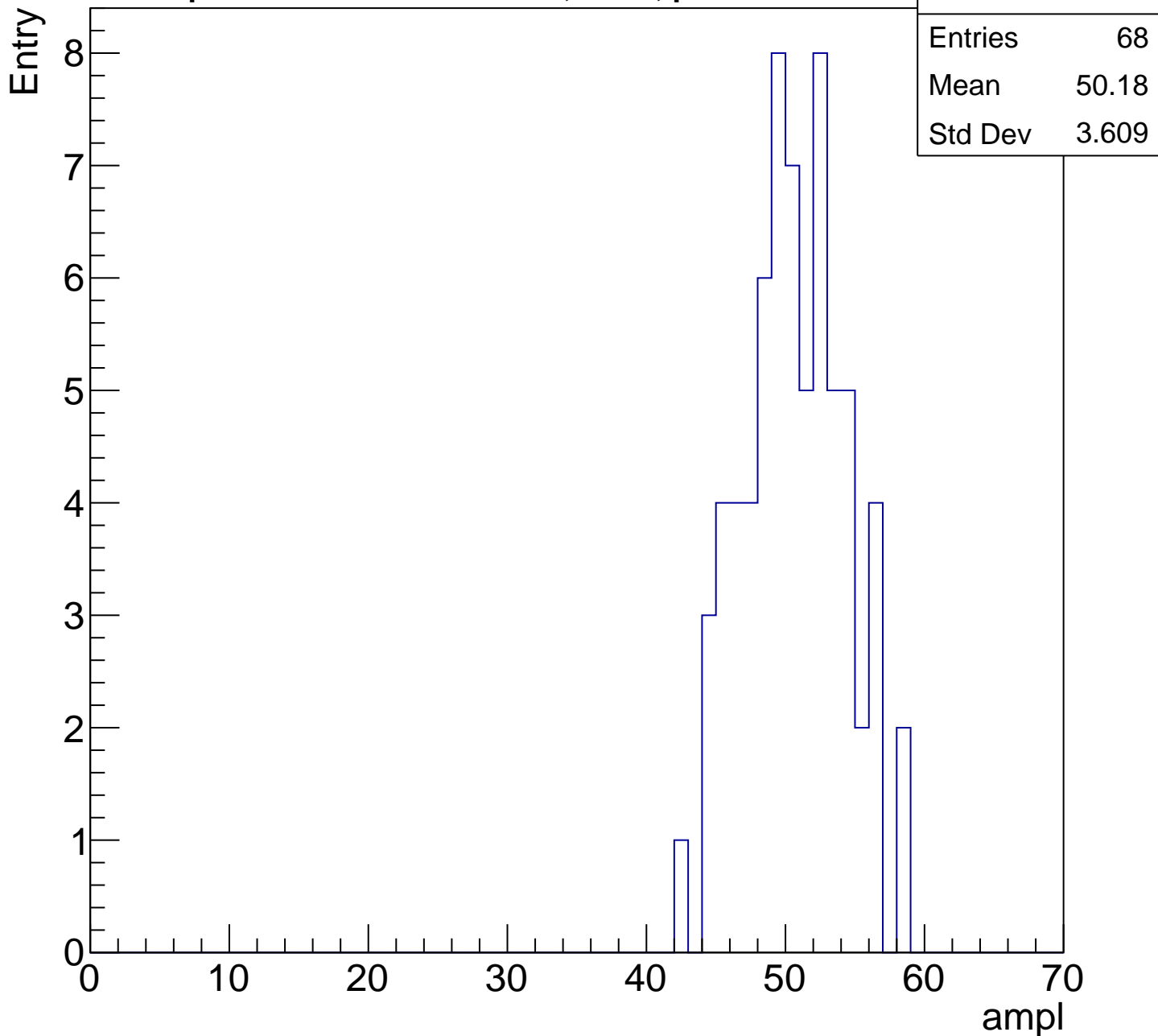
**Gaus mean : 44.8336**

**Gaus Width: 3.5904**



# B0L002S, U2-ch46, adc3

calib\_packv5\_042523\_0143.root, FC#8, port C1

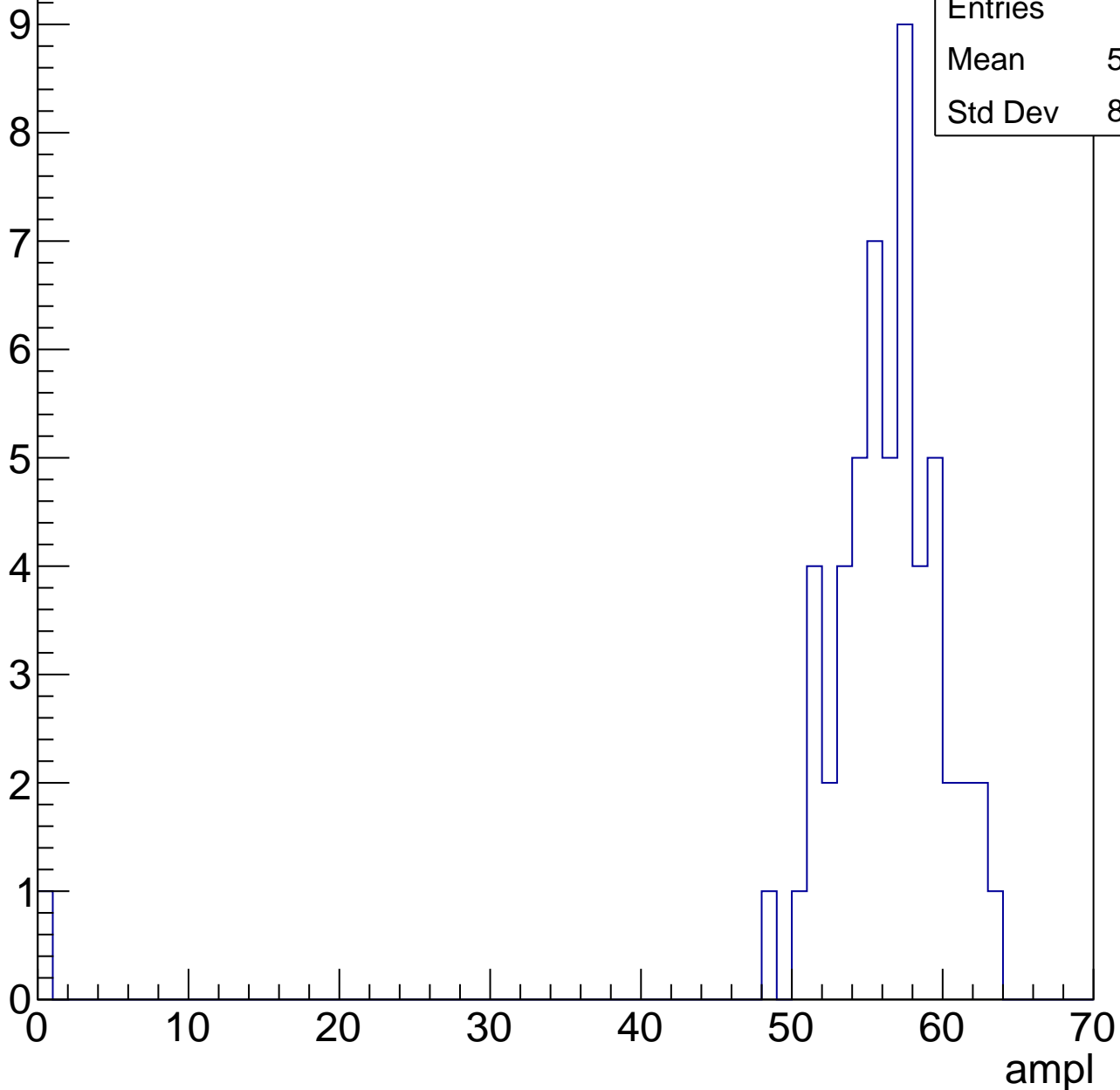


# B0L002S, U2-ch46, adc4

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	55
Mean	54.95
Std Dev	8.138



# B0L002S, U2-ch46, adc5

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	42
Mean	60.45
Std Dev	1.978

ampl

0 10 20 30 40 50 60 70

0

1

2

3

4

5

6

7

8

# B0L002S, U2-ch46, adc6

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry





# B0L002S, U2-ch46, adc7

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



# B0L002S, U2-ch47, adc0

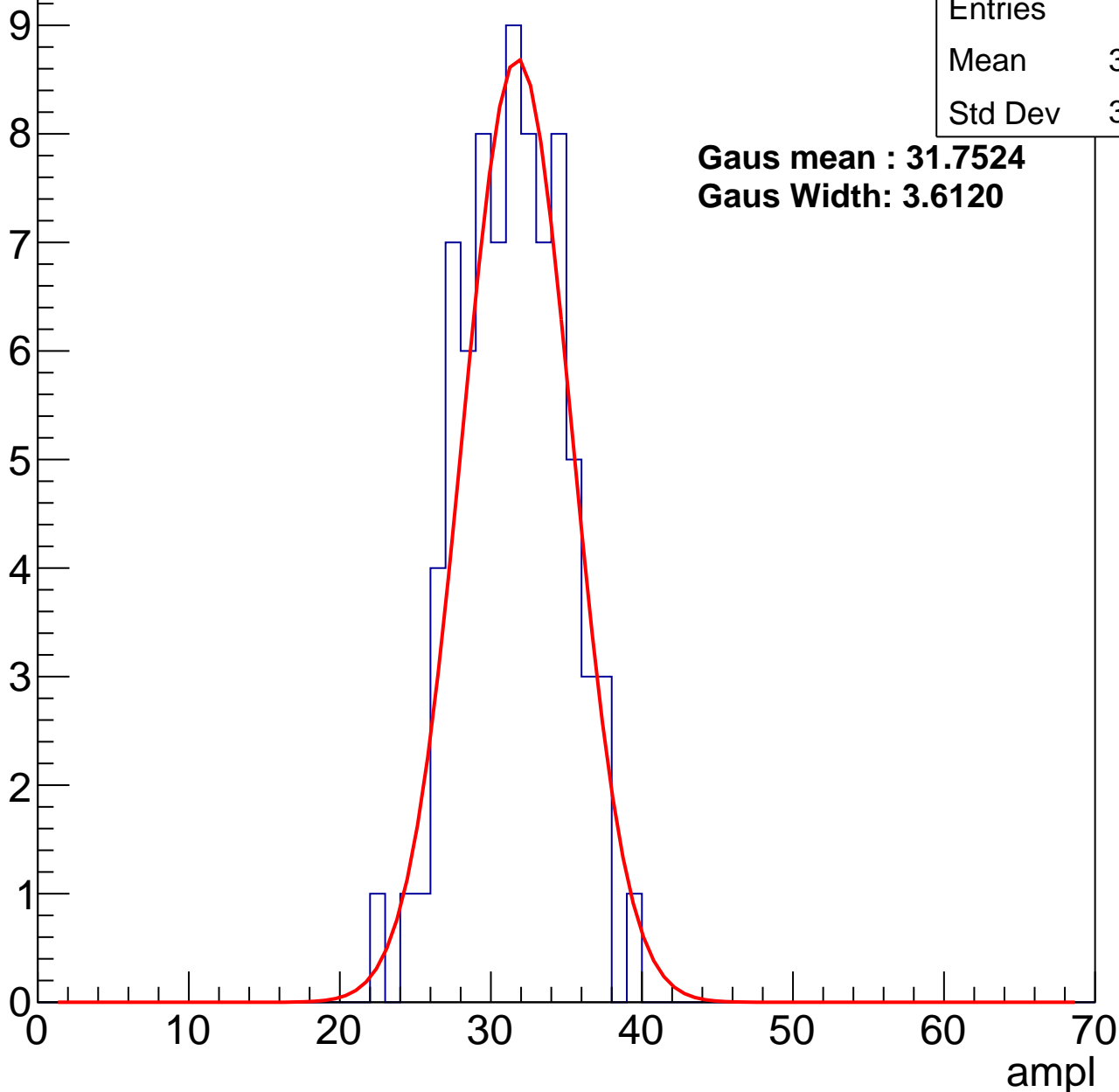
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	79
Mean	30.95
Std Dev	3.386

**Gaus mean : 31.7524**

**Gaus Width: 3.6120**



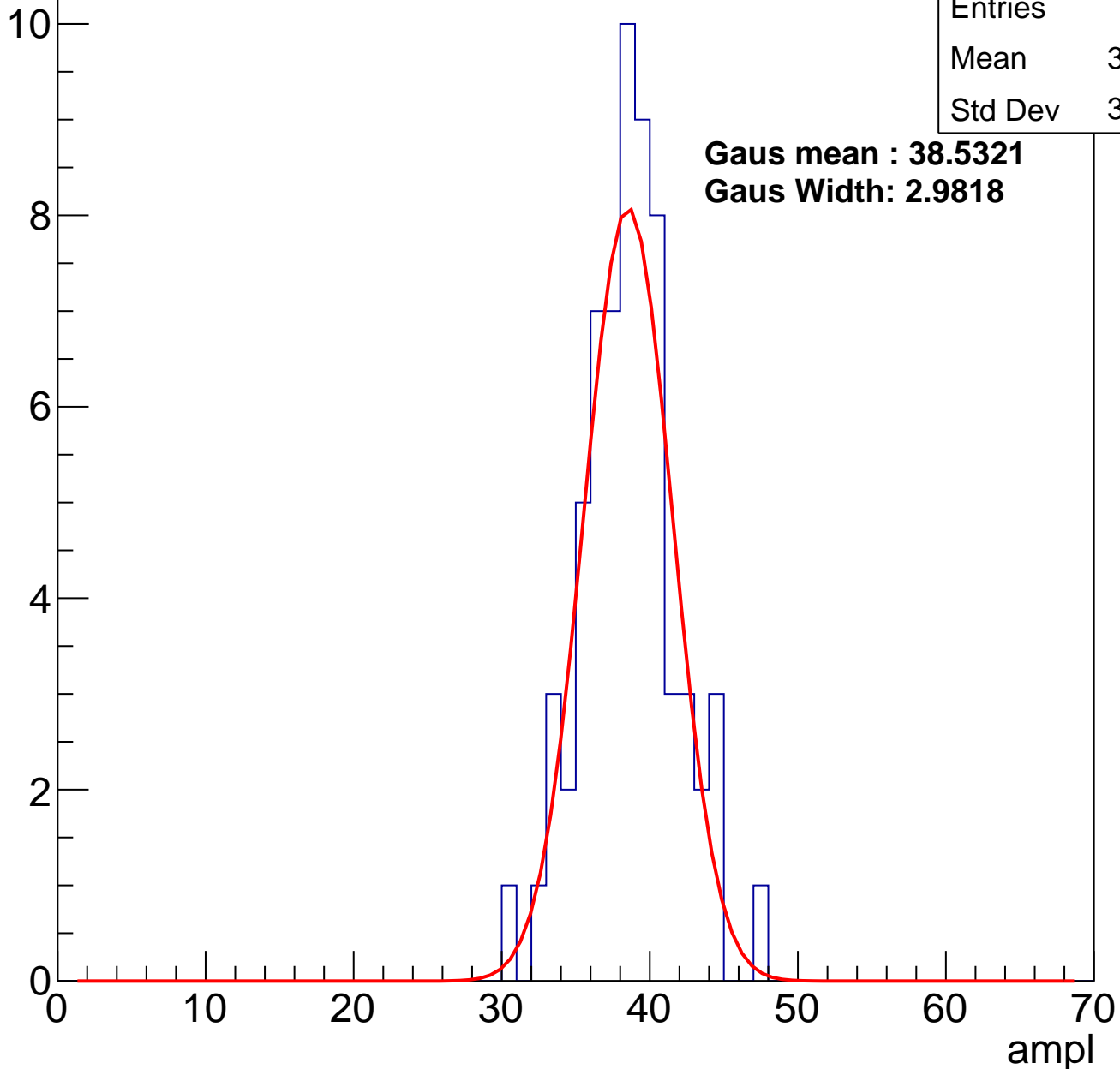
# B0L002S, U2-ch47, adc1

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entries	65
Mean	38.15
Std Dev	3.139

**Gaus mean : 38.5321**  
**Gaus Width: 2.9818**

Entry



# B0L002S, U2-ch47, adc2

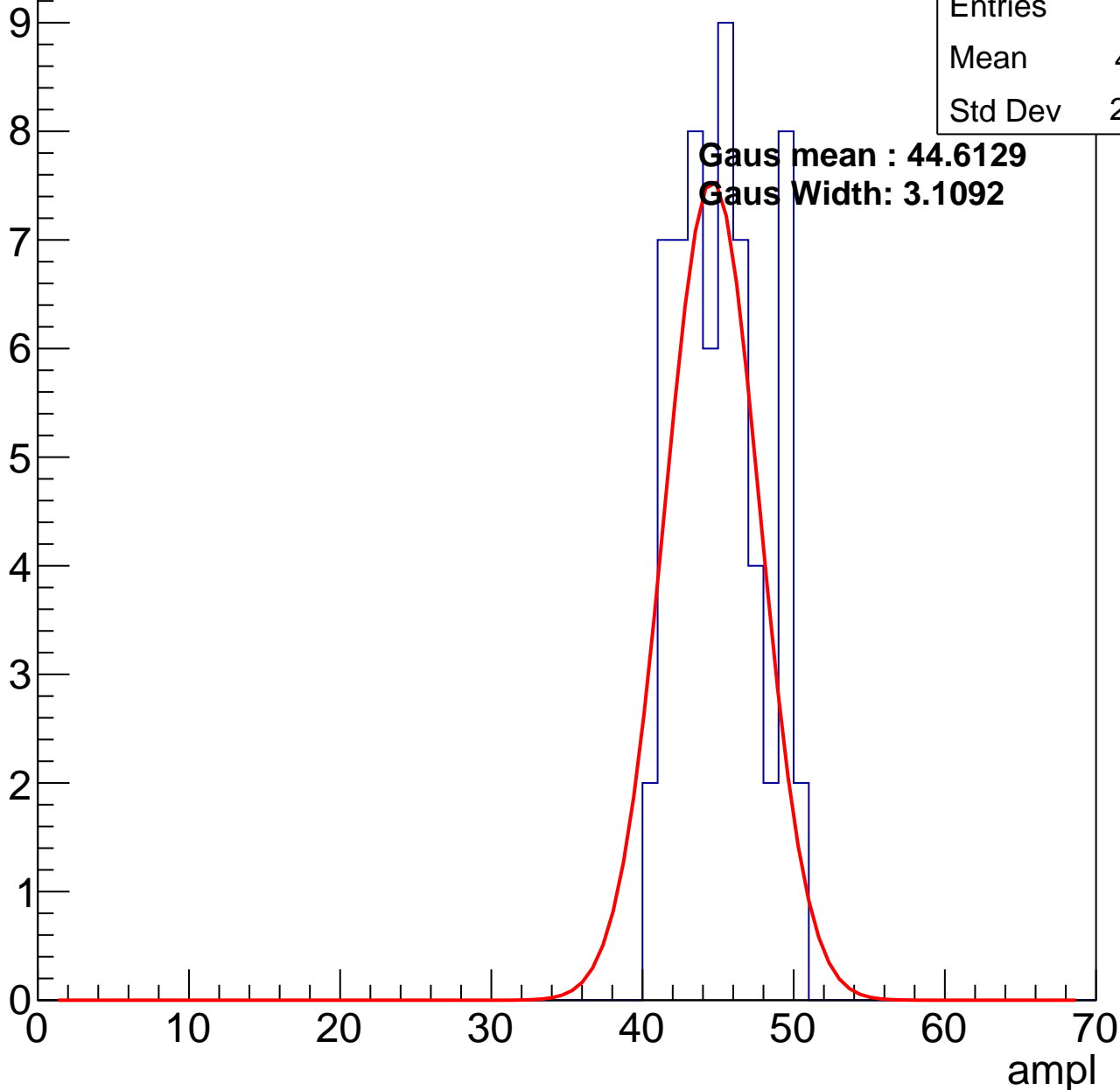
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	62
Mean	44.71
Std Dev	2.773

**Gaus mean : 44.6129**

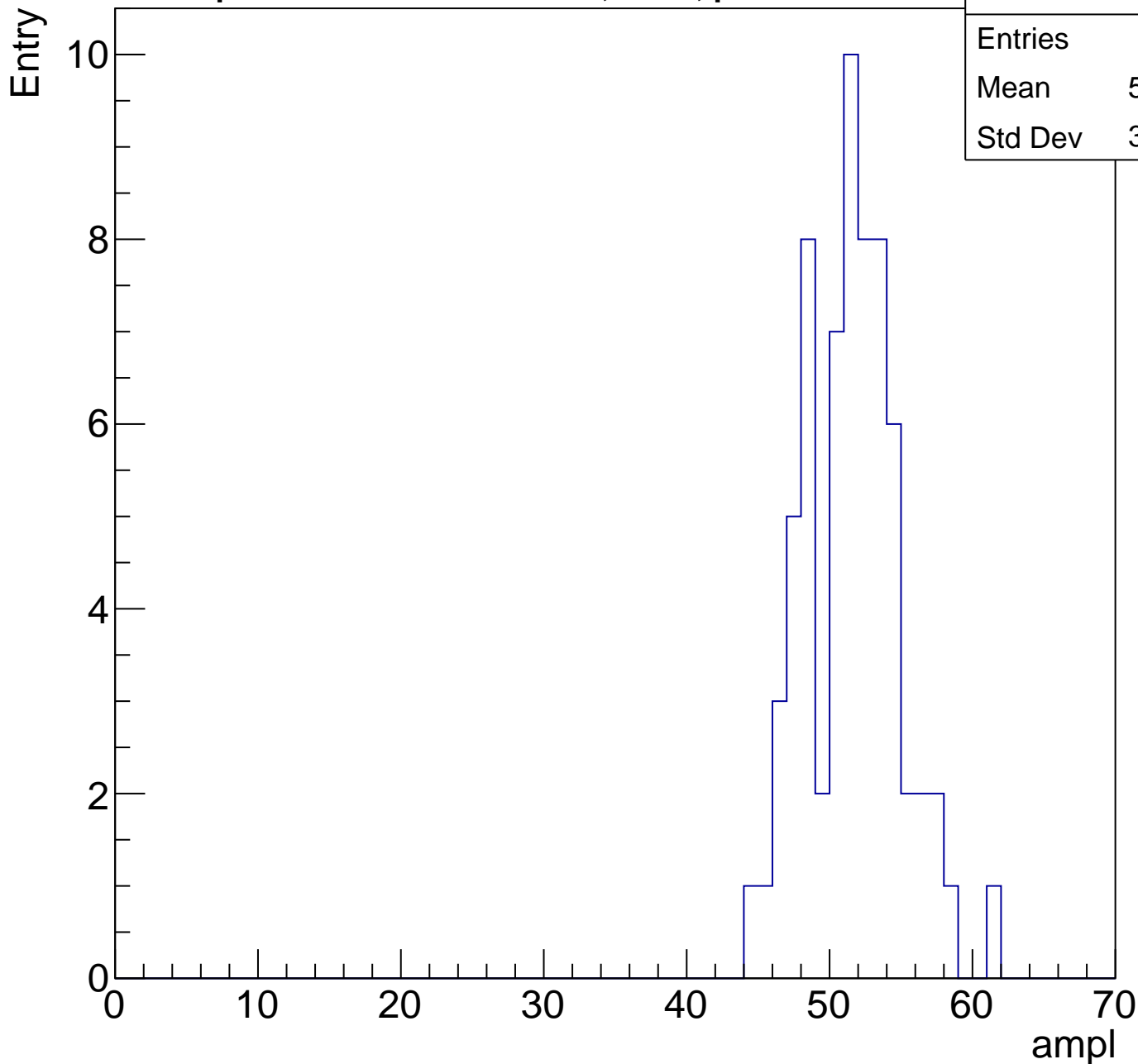
**Gaus Width: 3.1092**



# B0L002S, U2-ch47, adc3

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entries	67
Mean	51.09
Std Dev	3.286

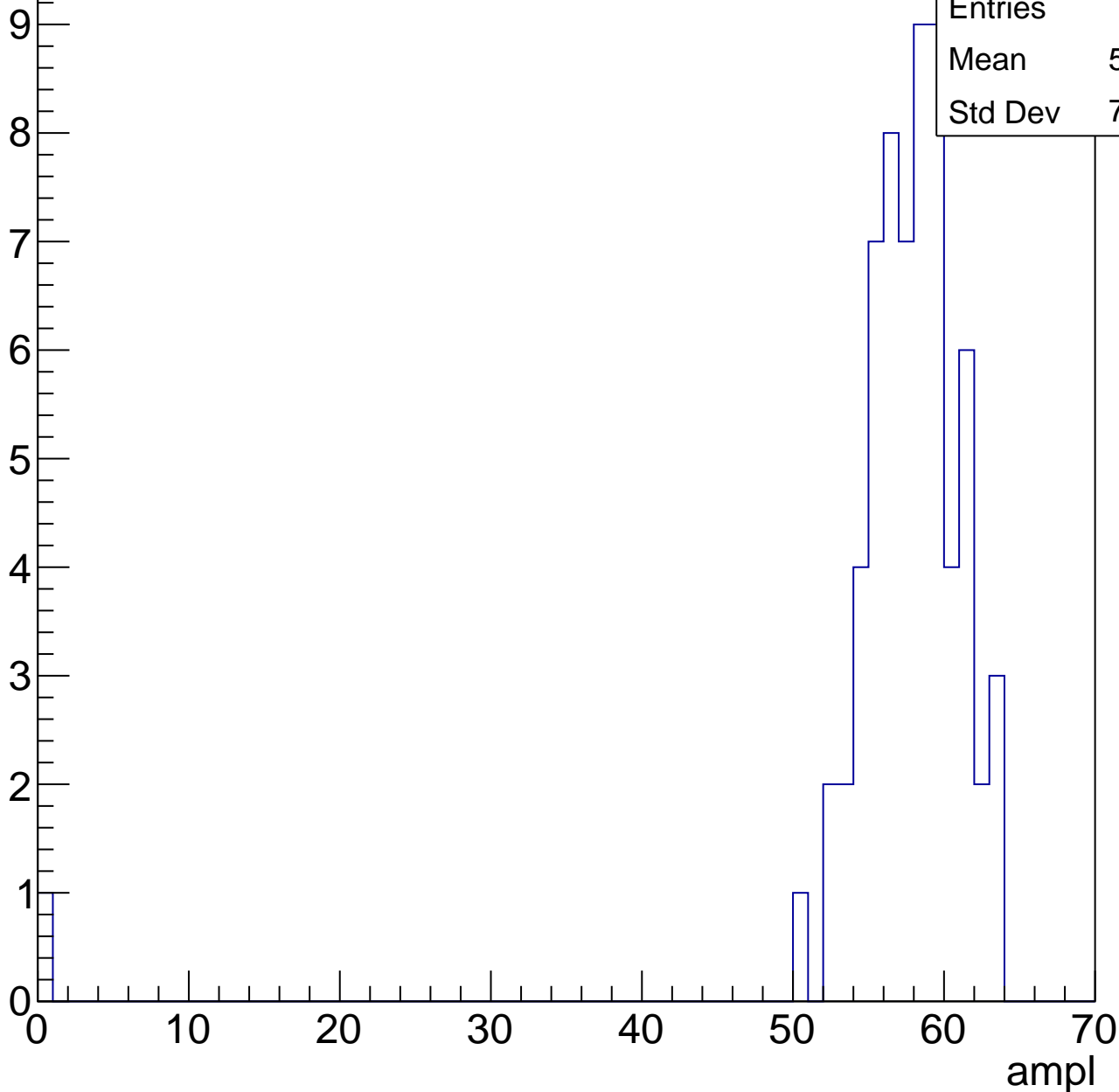


# B0L002S, U2-ch47, adc4

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	65
Mean	56.62
Std Dev	7.623

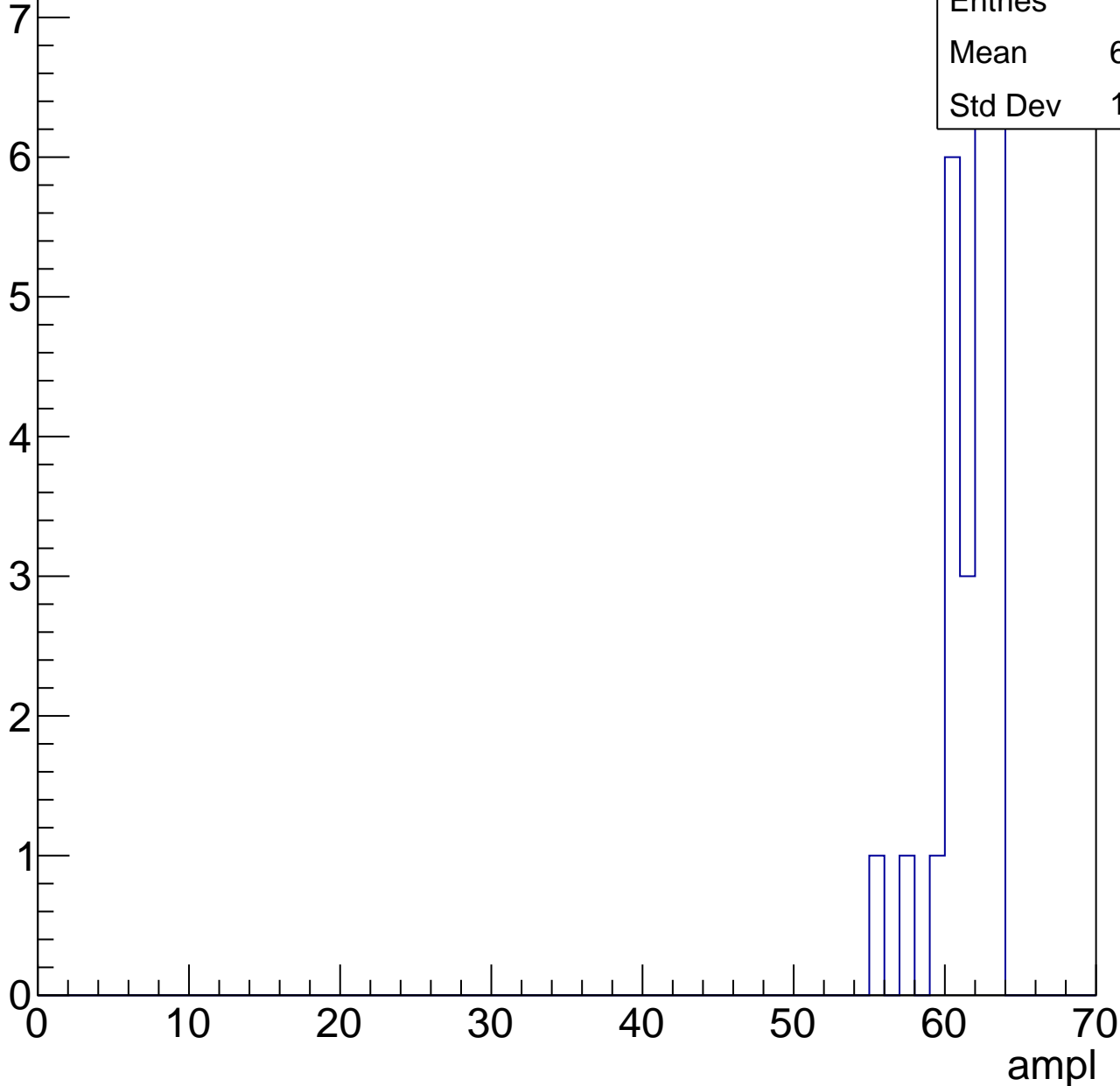


# B0L002S, U2-ch47, adc5

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	26
Mean	61.12
Std Dev	1.928



# B0L002S, U2-ch47, adc6

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry





# B0L002S, U2-ch47, adc7

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L002S, U2-ch48, adc0

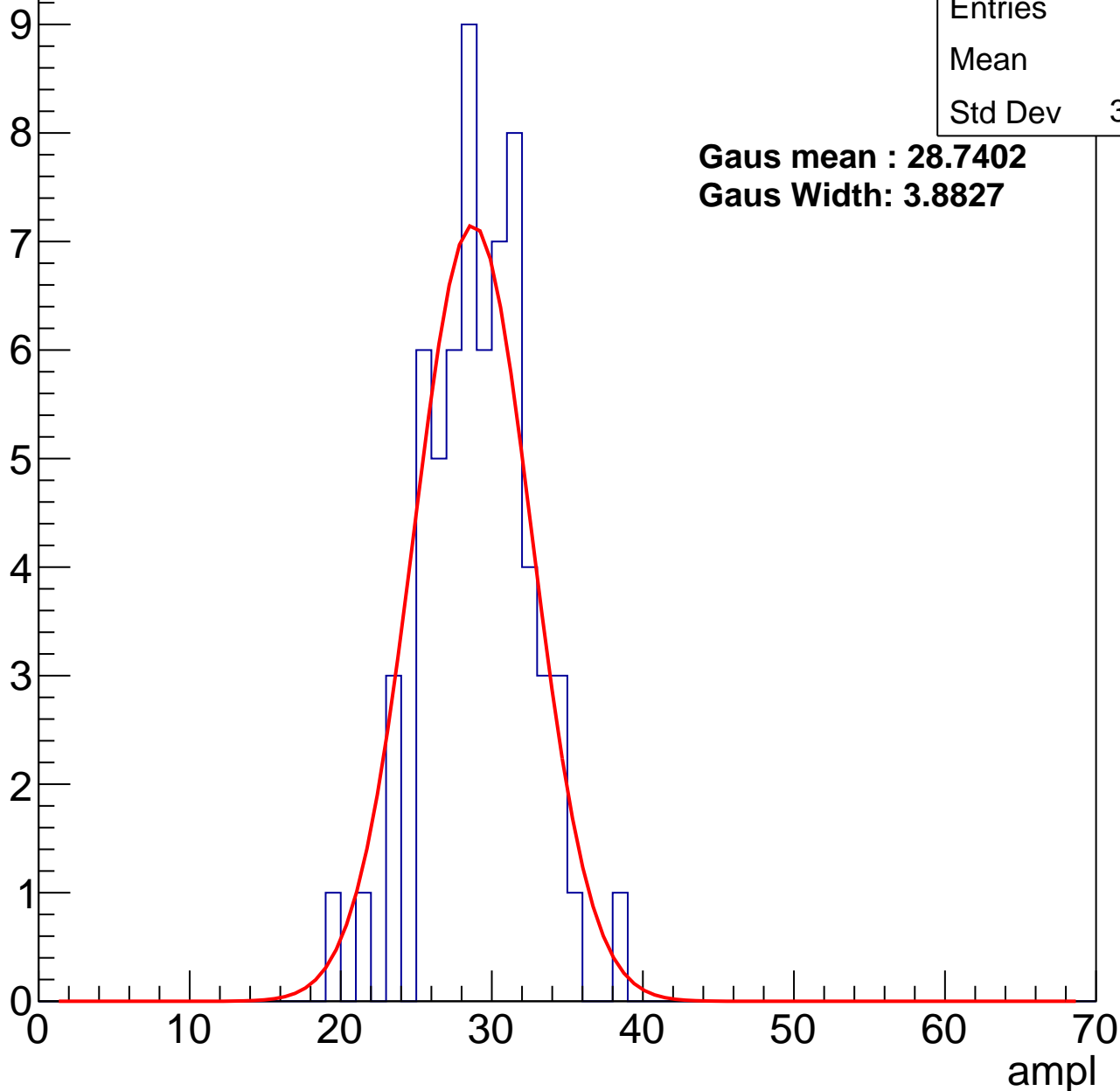
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	64
Mean	28.7
Std Dev	3.435

**Gaus mean : 28.7402**

**Gaus Width: 3.8827**



# B0L002S, U2-ch48, adc1

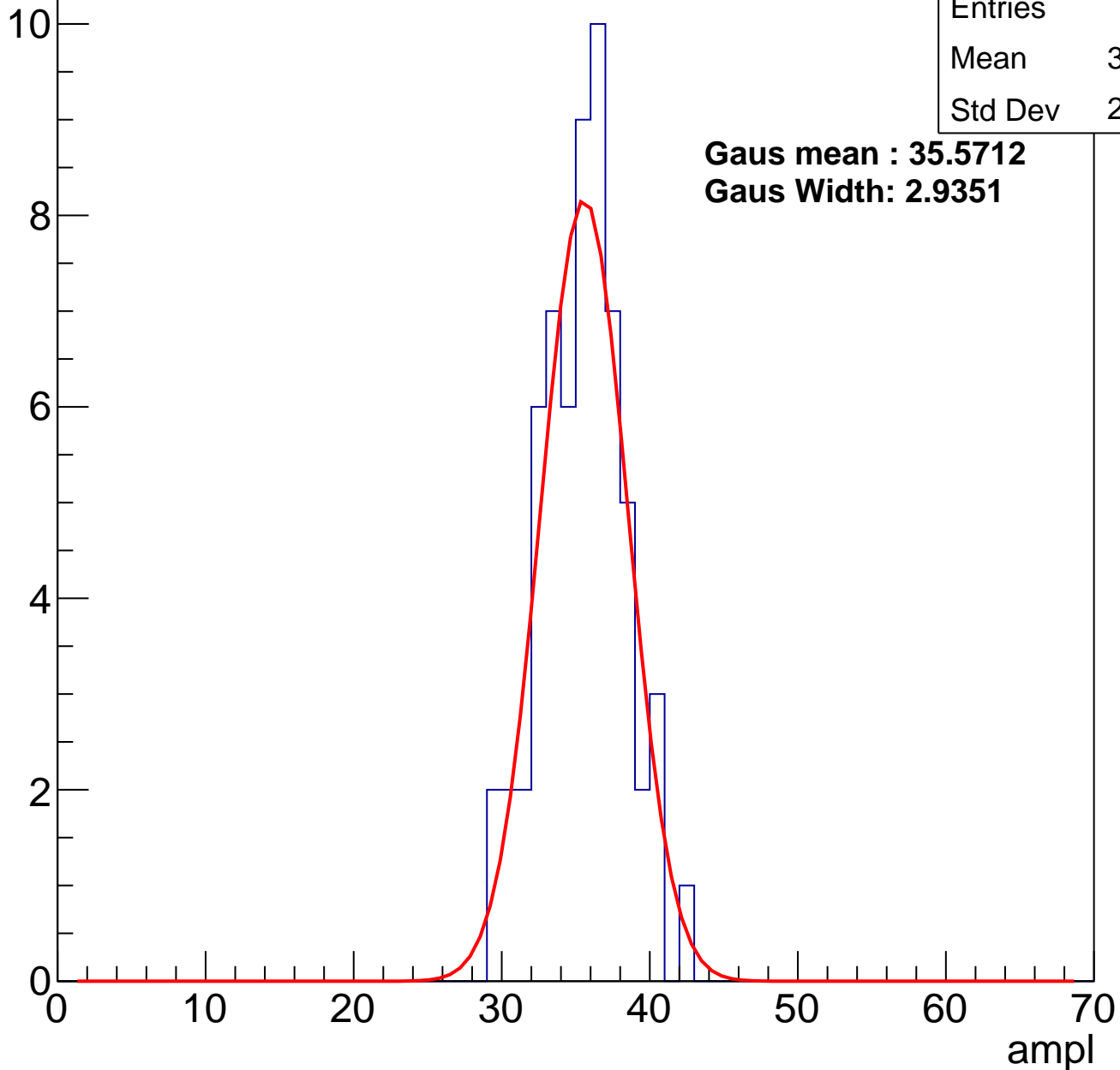
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entries	62
Mean	35.02
Std Dev	2.785

**Gaus mean : 35.5712**

**Gaus Width: 2.9351**

Entry



# B0L002S, U2-ch48, adc2

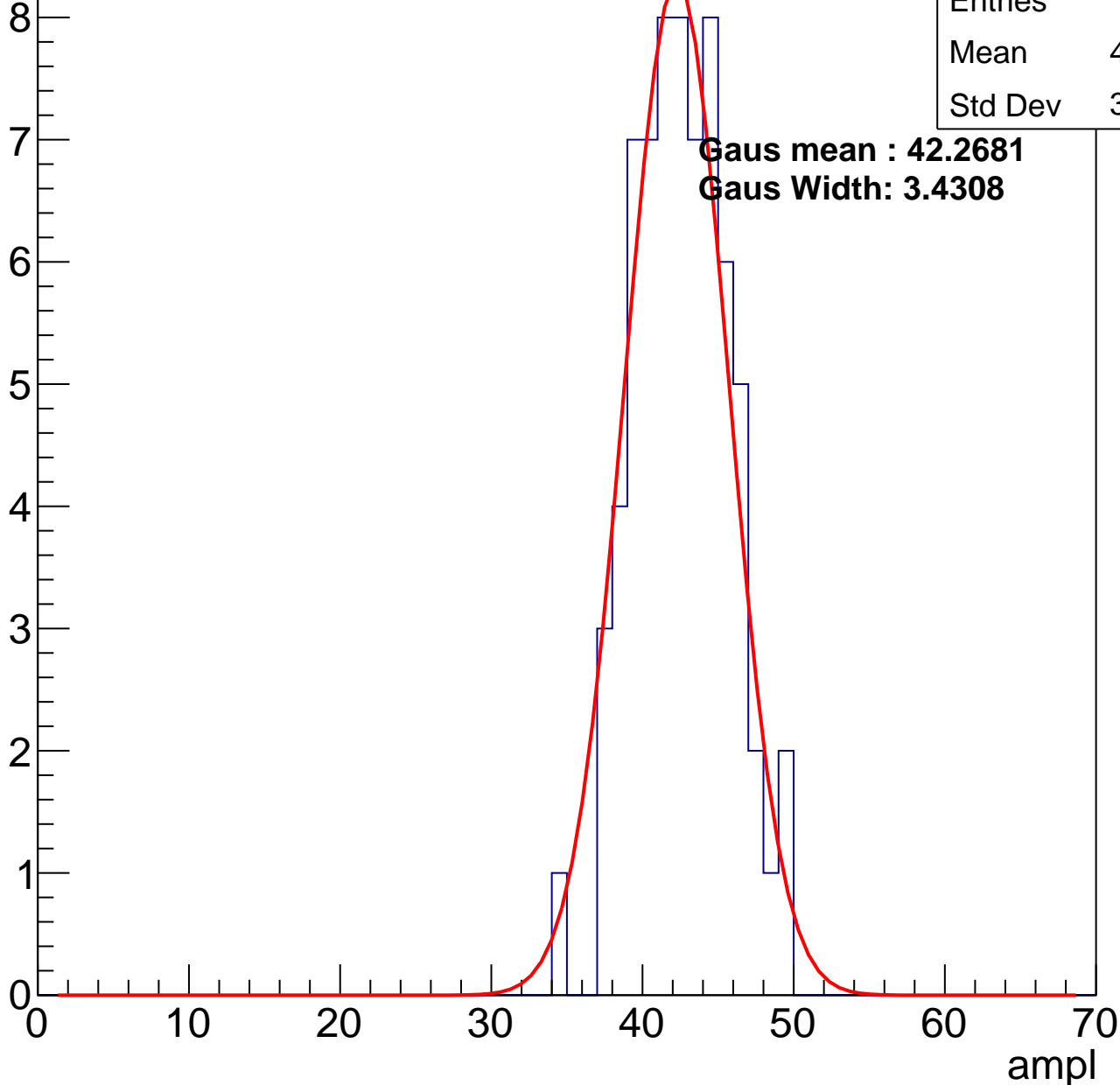
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	69
Mean	42.13
Std Dev	3.088

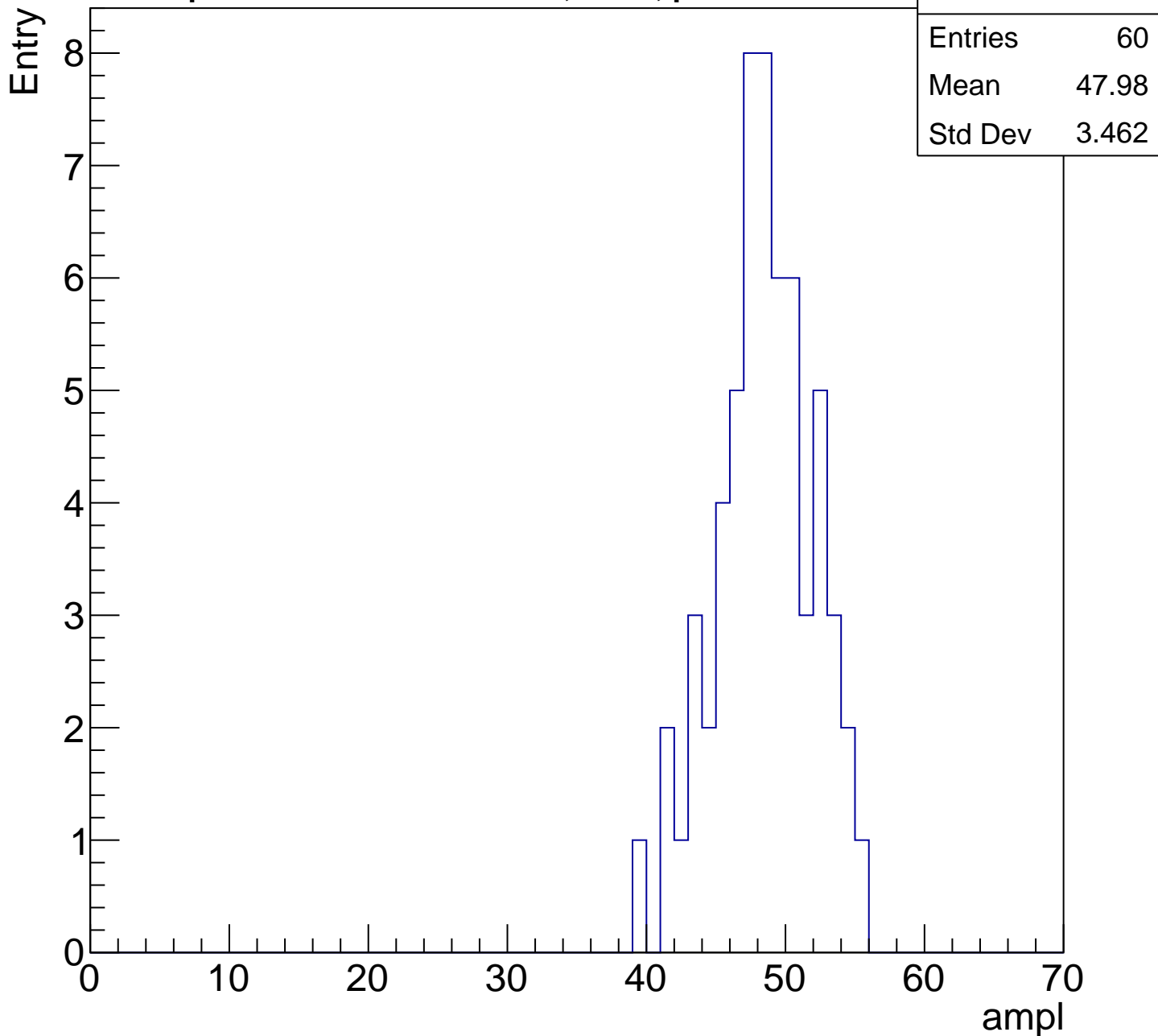
**Gaus mean : 42.2681**

**Gaus Width: 3.4308**



# B0L002S, U2-ch48, adc3

calib\_packv5\_042523\_0143.root, FC#8, port C1

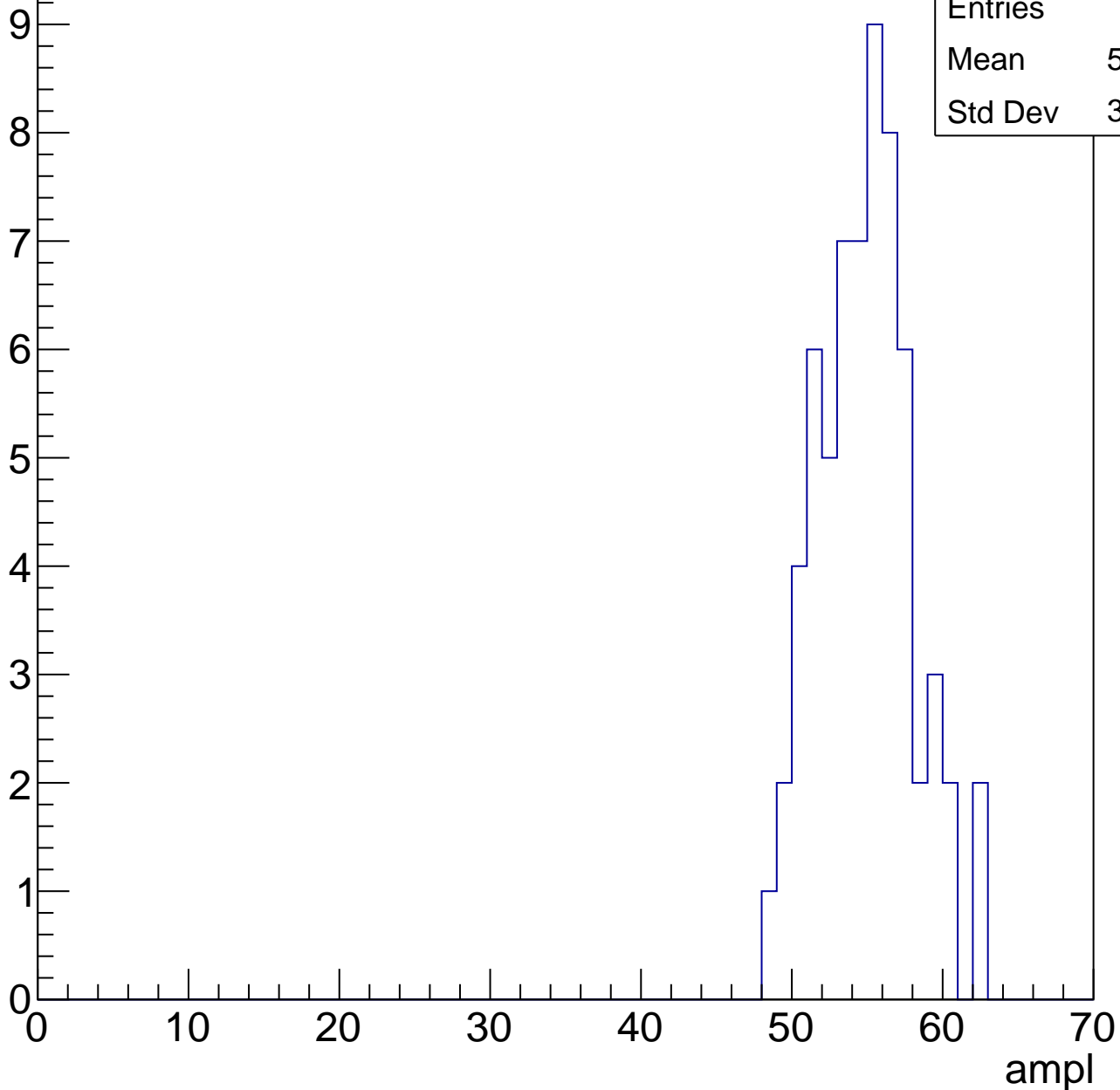


# B0L002S, U2-ch48, adc4

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	64
Mean	54.42
Std Dev	3.117

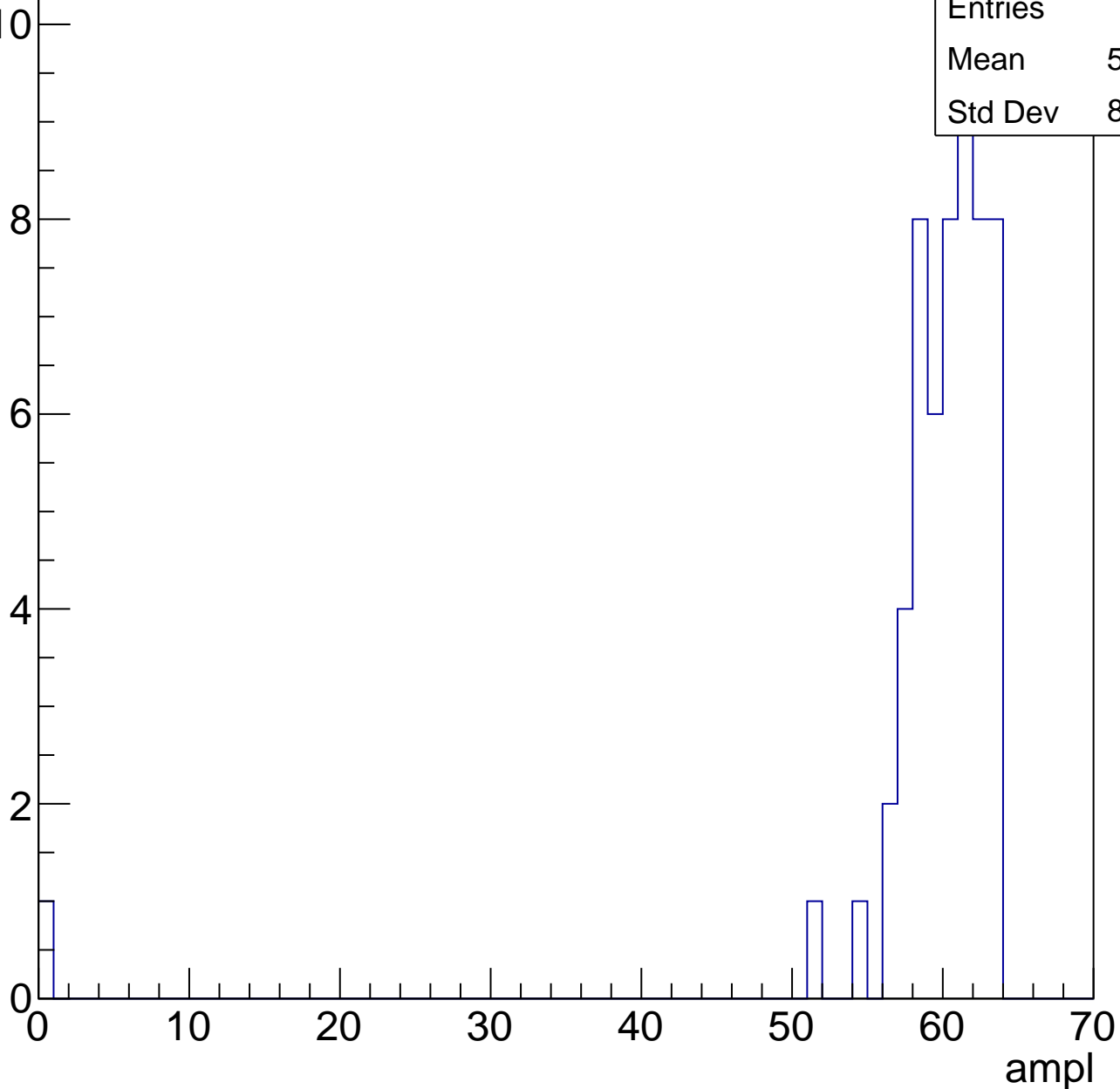


# B0L002S, U2-ch48, adc5

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

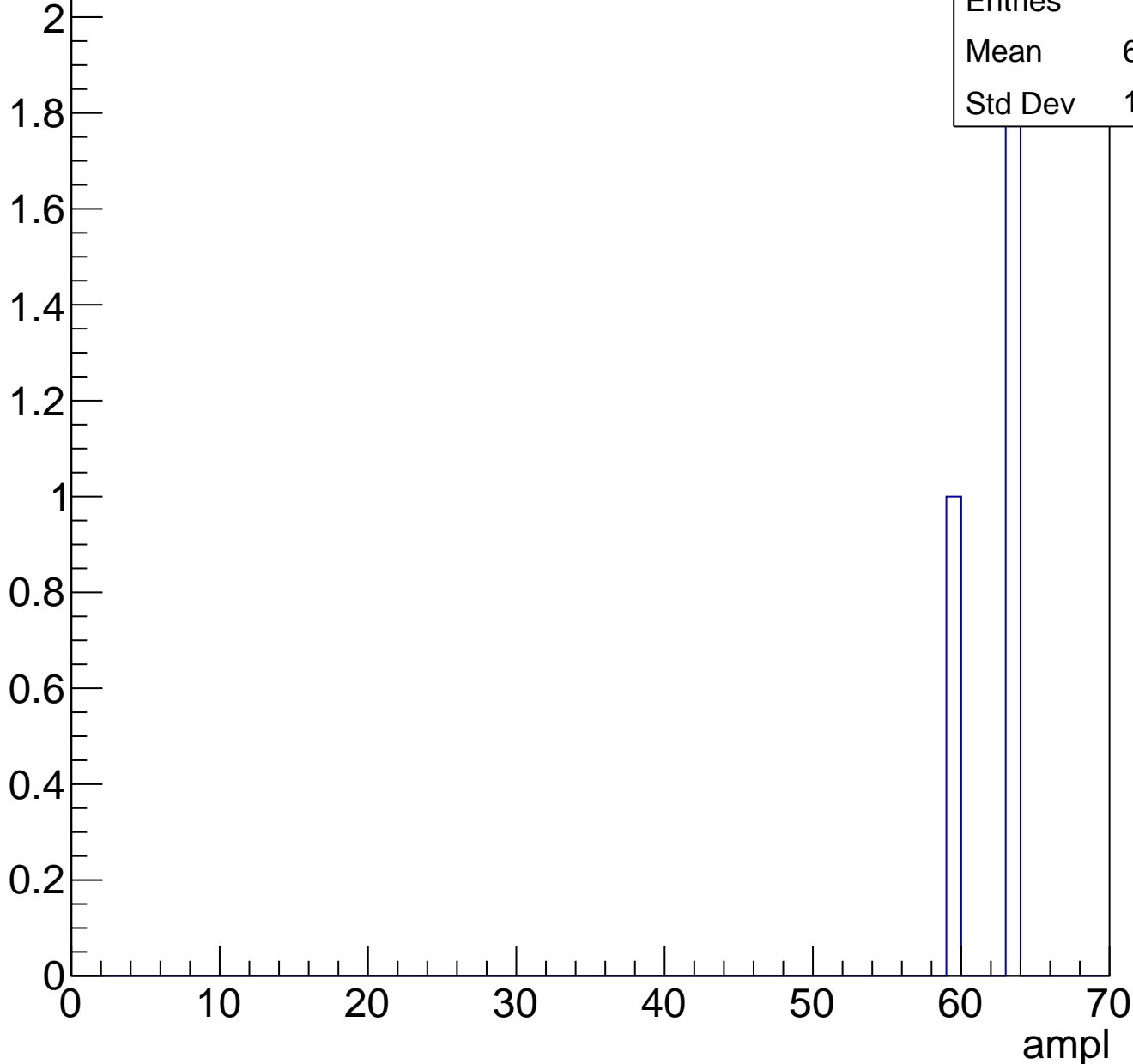
Entries	57
Mean	58.82
Std Dev	8.227



# B0L002S, U2-ch48, adc6

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry





# B0L002S, U2-ch48, adc7

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



# B0L002S, U2-ch49, adc0

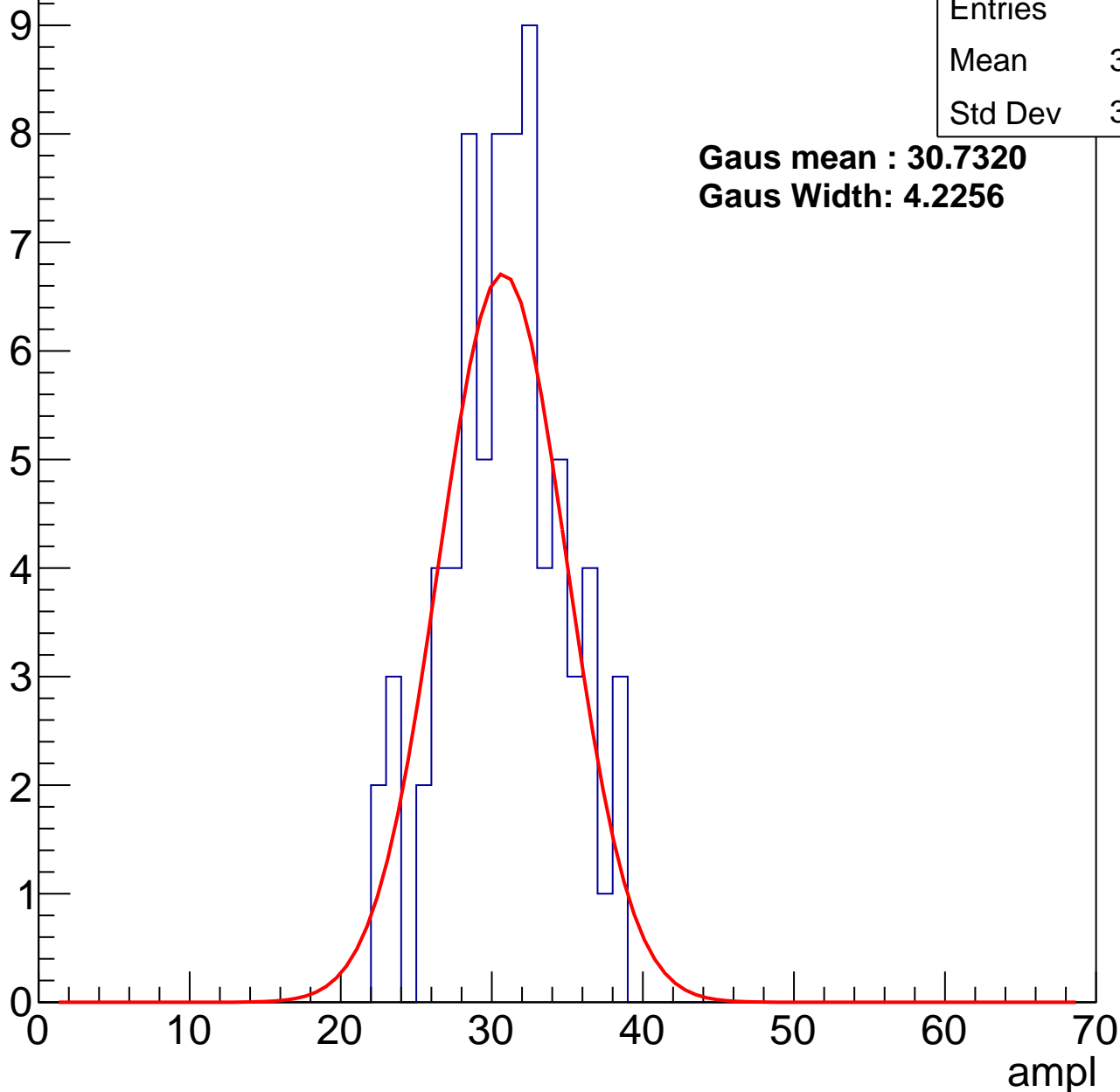
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	73
Mean	30.44
Std Dev	3.825

**Gaus mean : 30.7320**

**Gaus Width: 4.2256**



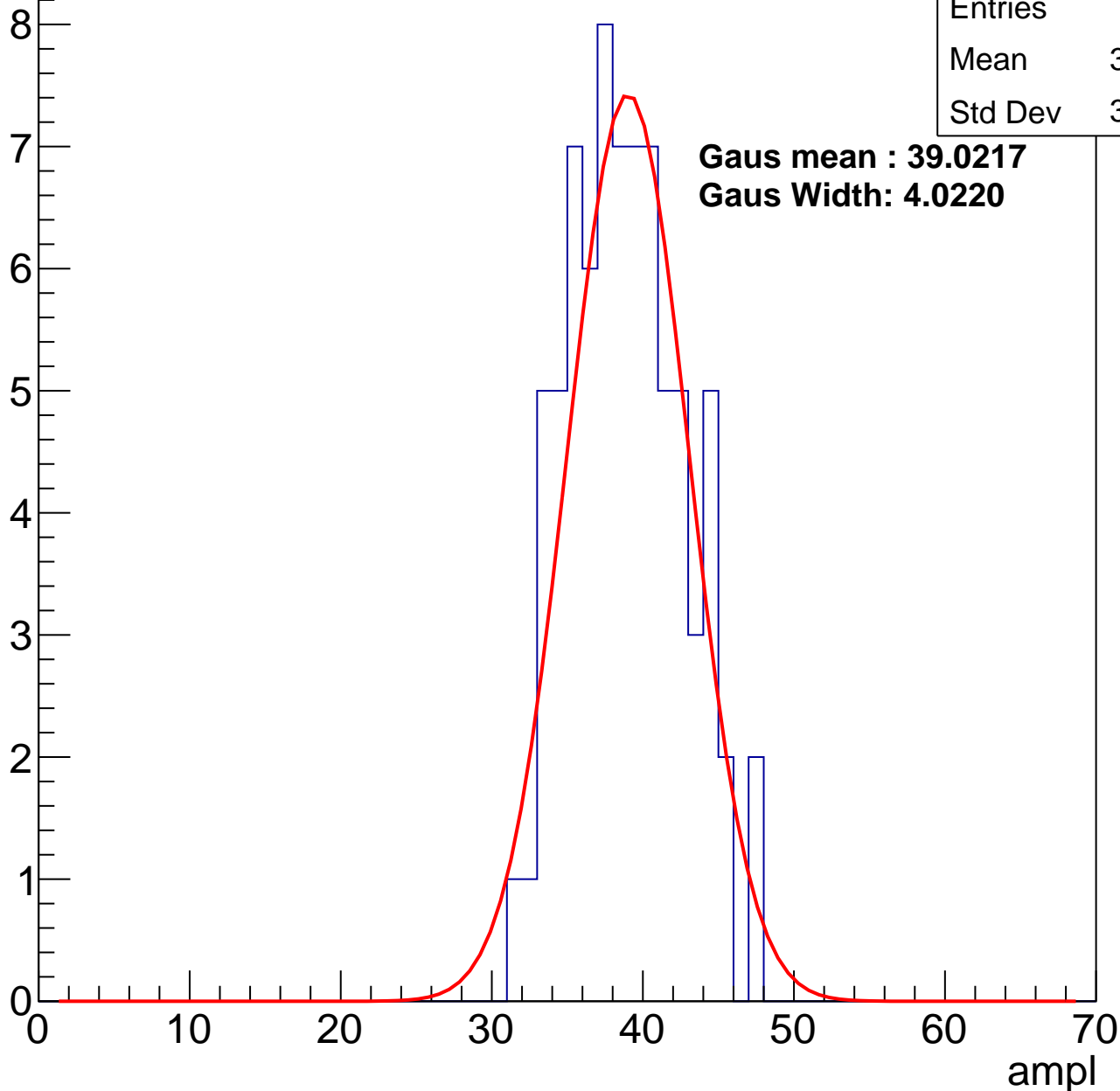
# B0L002S, U2-ch49, adc1

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	76
Mean	38.45
Std Dev	3.708

**Gaus mean : 39.0217**  
**Gaus Width: 4.0220**



# B0L002S, U2-ch49, adc2

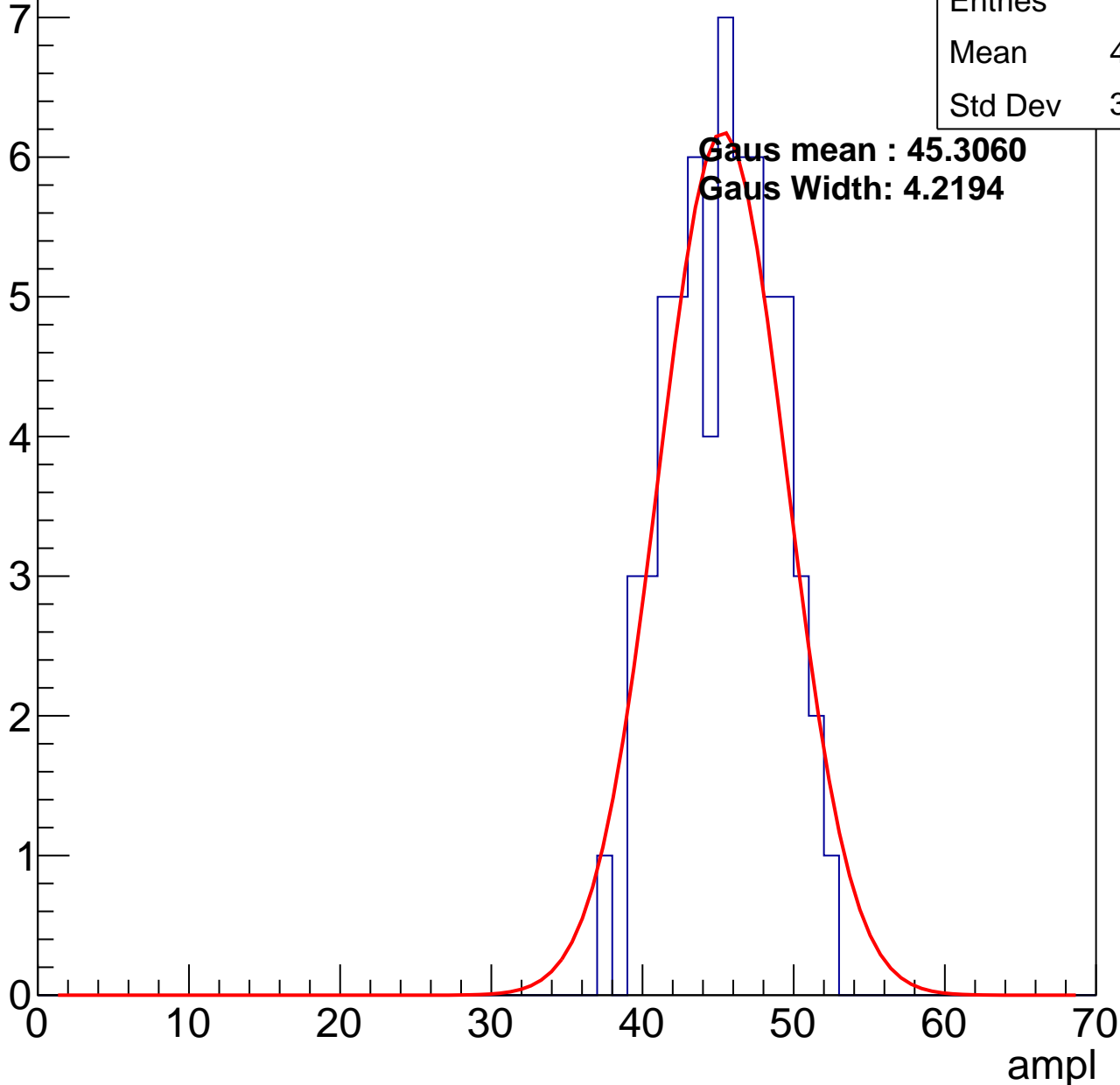
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	62
Mean	44.92
Std Dev	3.479

**Gaus mean : 45.3060**

**Gaus Width: 4.2194**

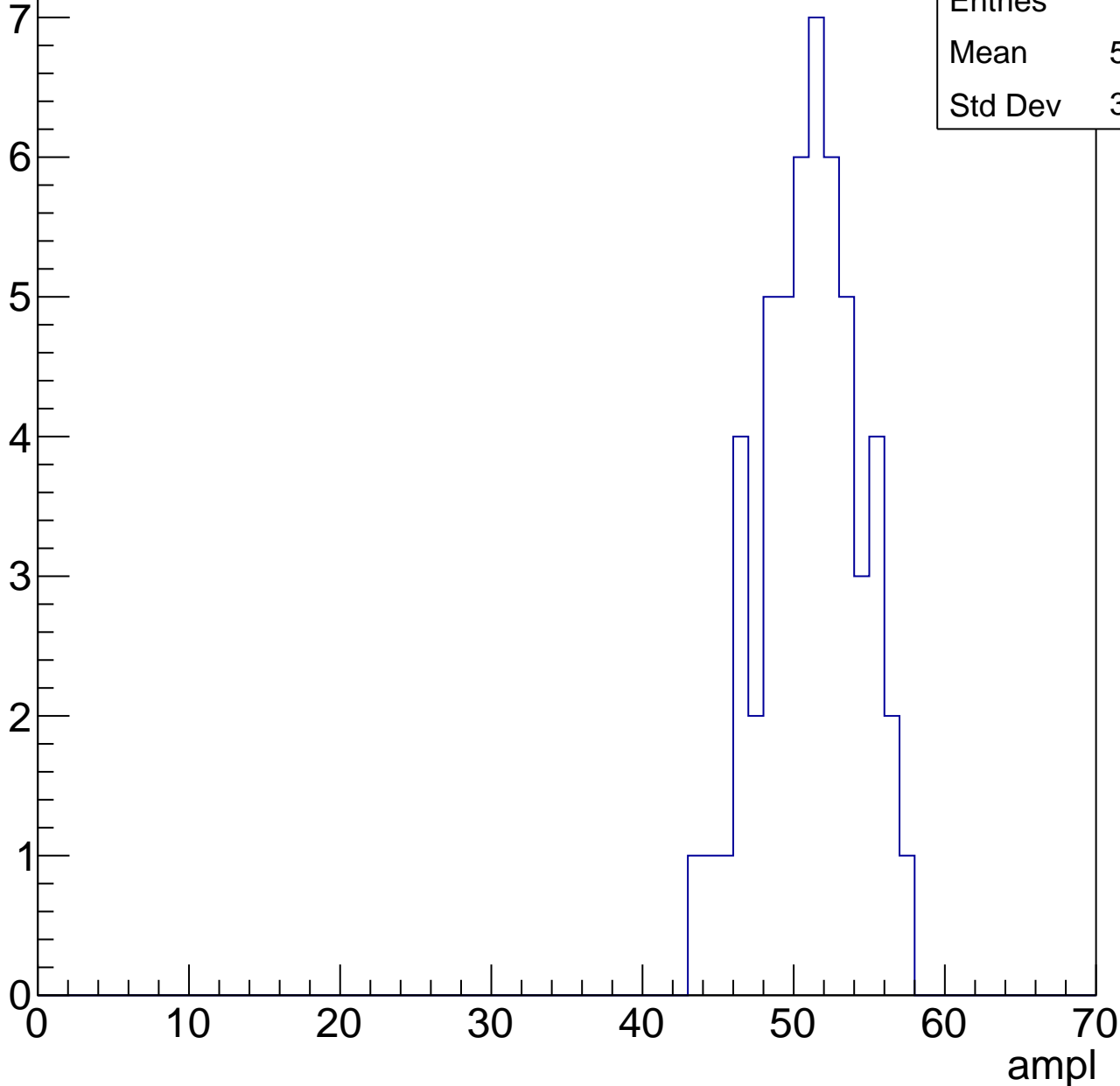


# B0L002S, U2-ch49, adc3

calib\_packv5\_042523\_0143.root, FC#8, port C1

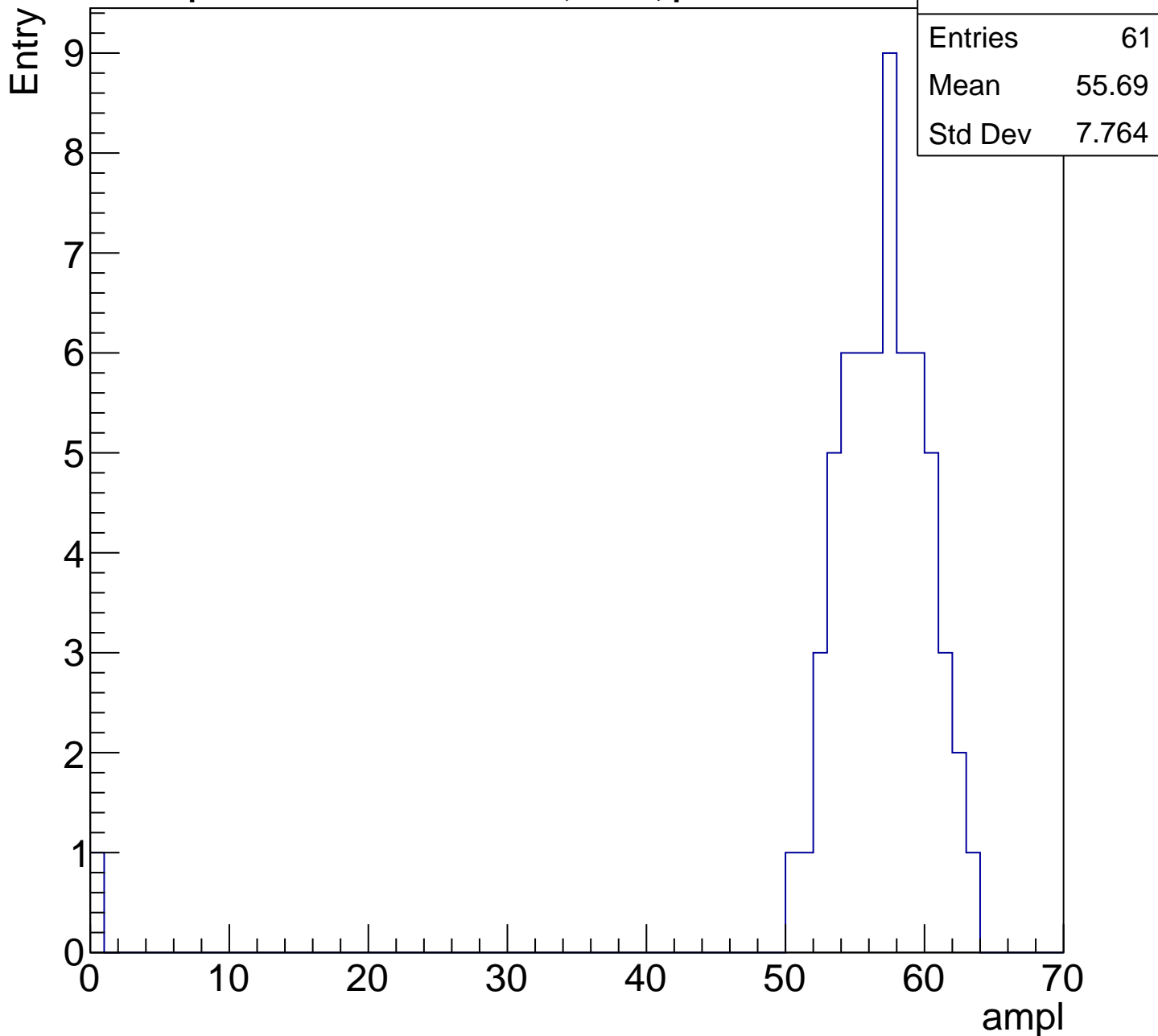
Entry

Entries	53
Mean	50.57
Std Dev	3.207



# B0L002S, U2-ch49, adc4

calib\_packv5\_042523\_0143.root, FC#8, port C1

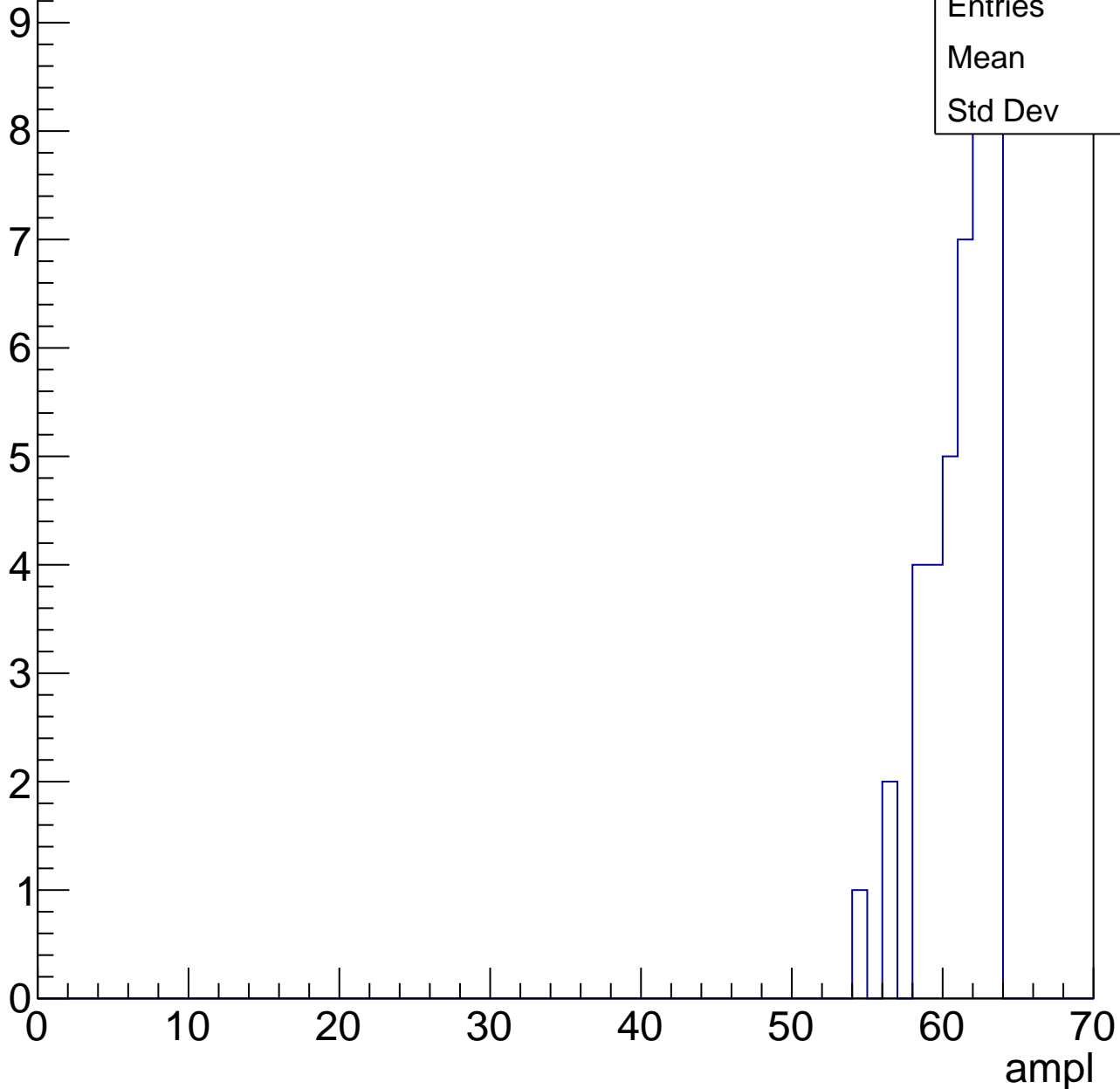


# B0L002S, U2-ch49, adc5

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	40
Mean	60.6
Std Dev	2.2



# B0L002S, U2-ch49, adc6

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



Entries	0
Mean	0
Std Dev	0



# B0L002S, U2-ch49, adc7

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



# B0L002S, U2-ch50, adc0

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entries	82
Mean	29.95
Std Dev	3.702

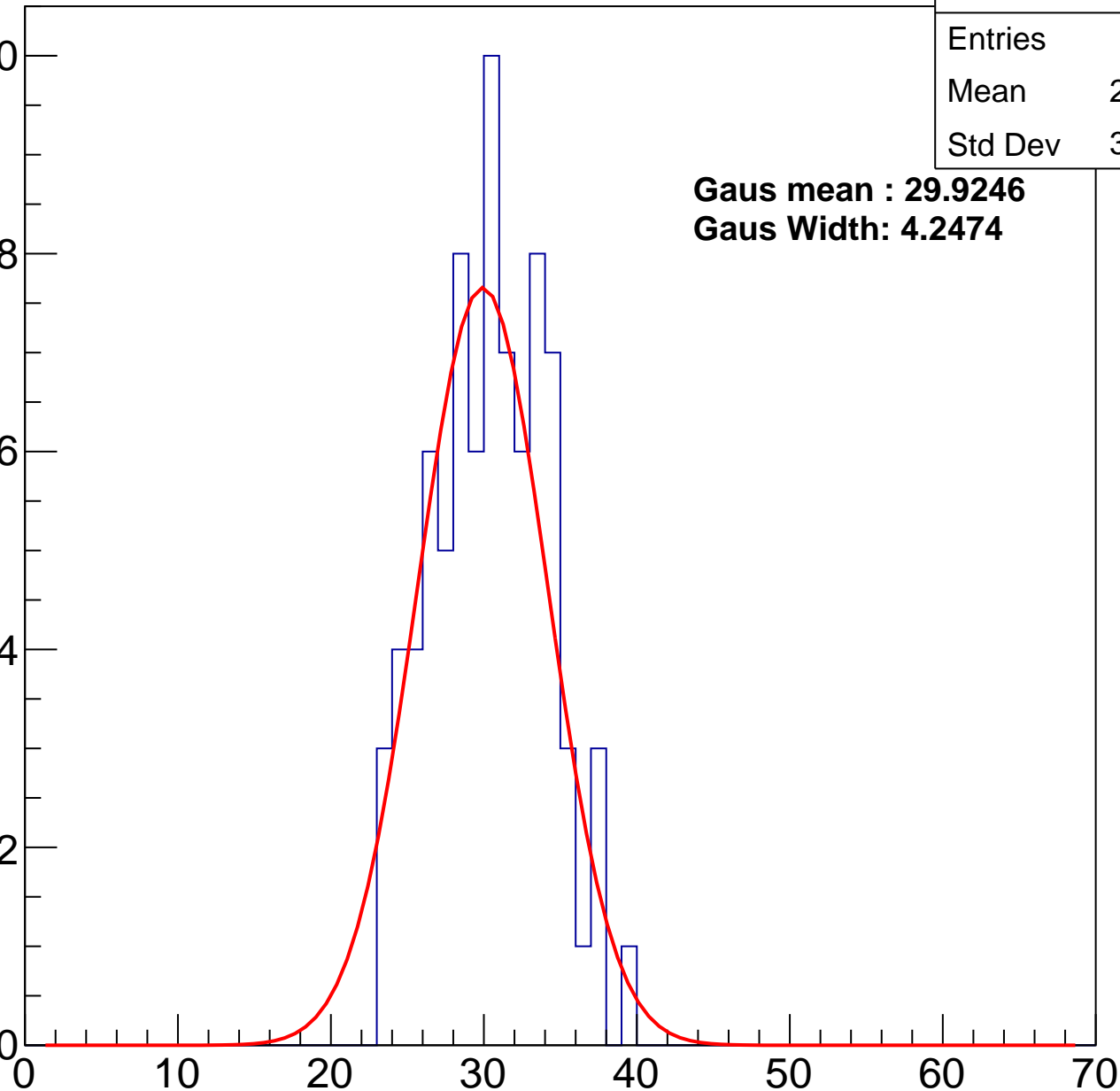
**Gaus mean : 29.9246**

**Gaus Width: 4.2474**

Entry

10  
8  
6  
4  
2  
0

ampl



# B0L002S, U2-ch50, adc1

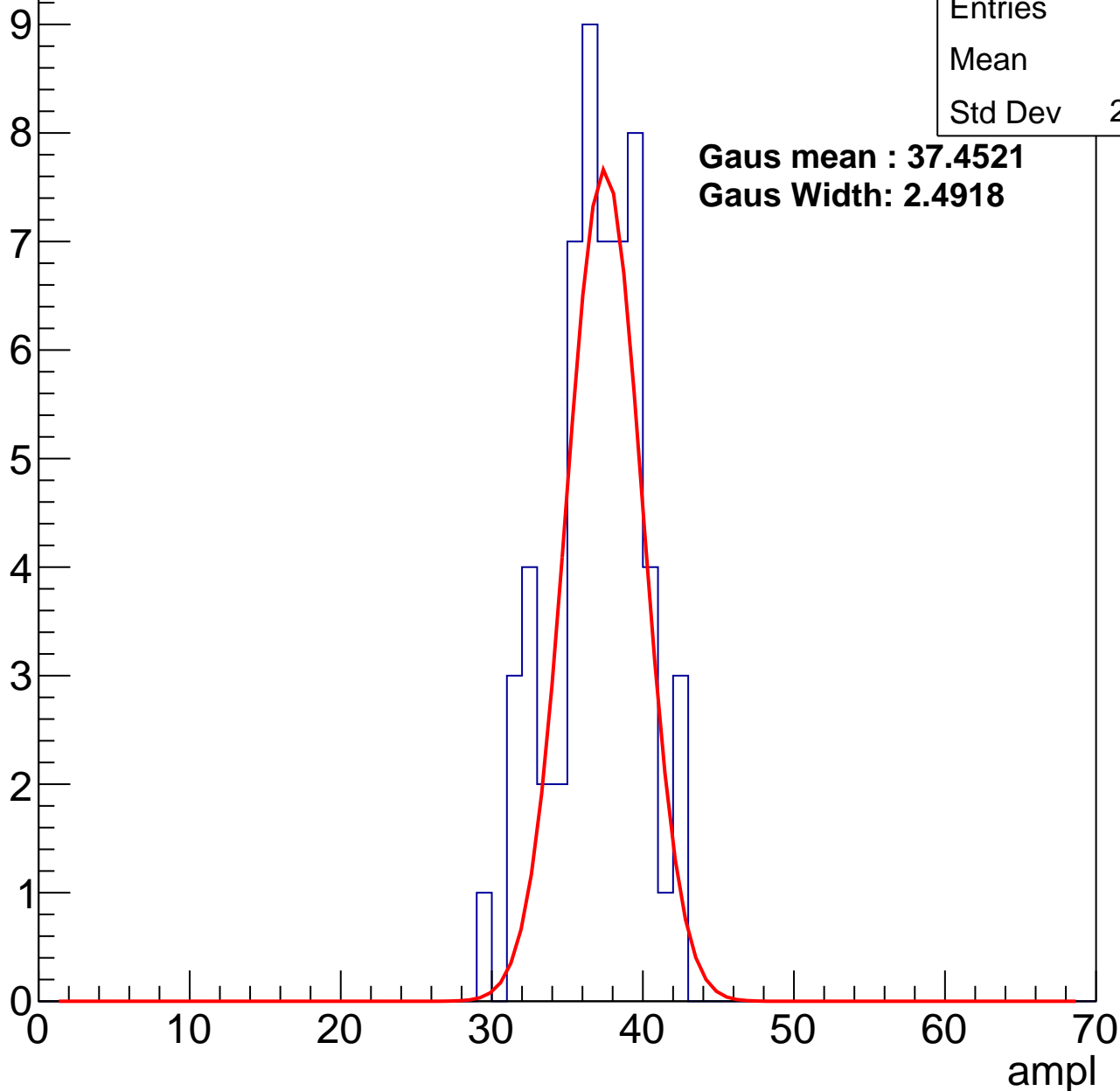
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	58
Mean	36.5
Std Dev	2.967

**Gaus mean : 37.4521**

**Gaus Width: 2.4918**



# B0L002S, U2-ch50, adc2

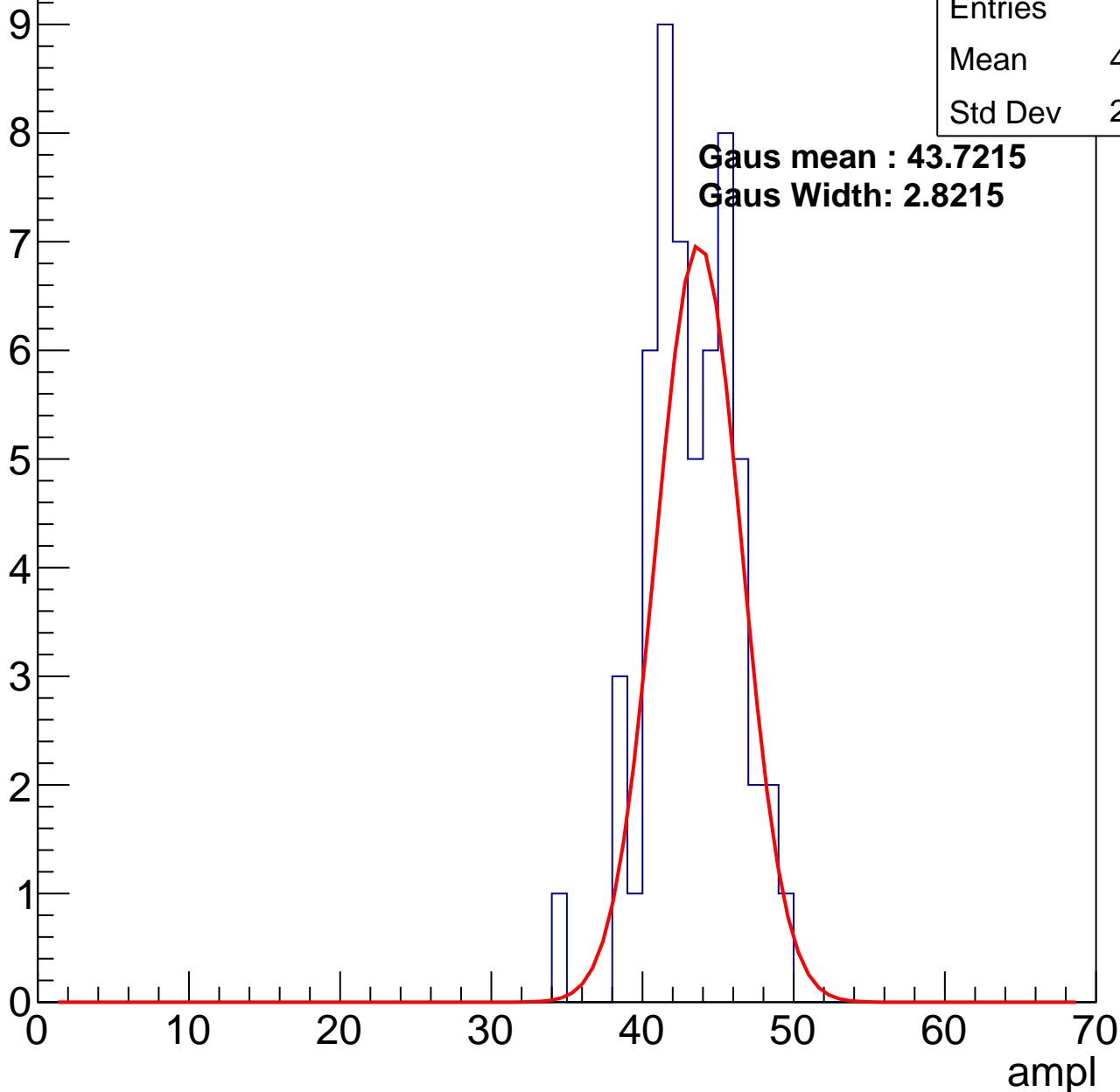
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	56
Mean	42.82
Std Dev	2.892

**Gaus mean : 43.7215**

**Gaus Width: 2.8215**

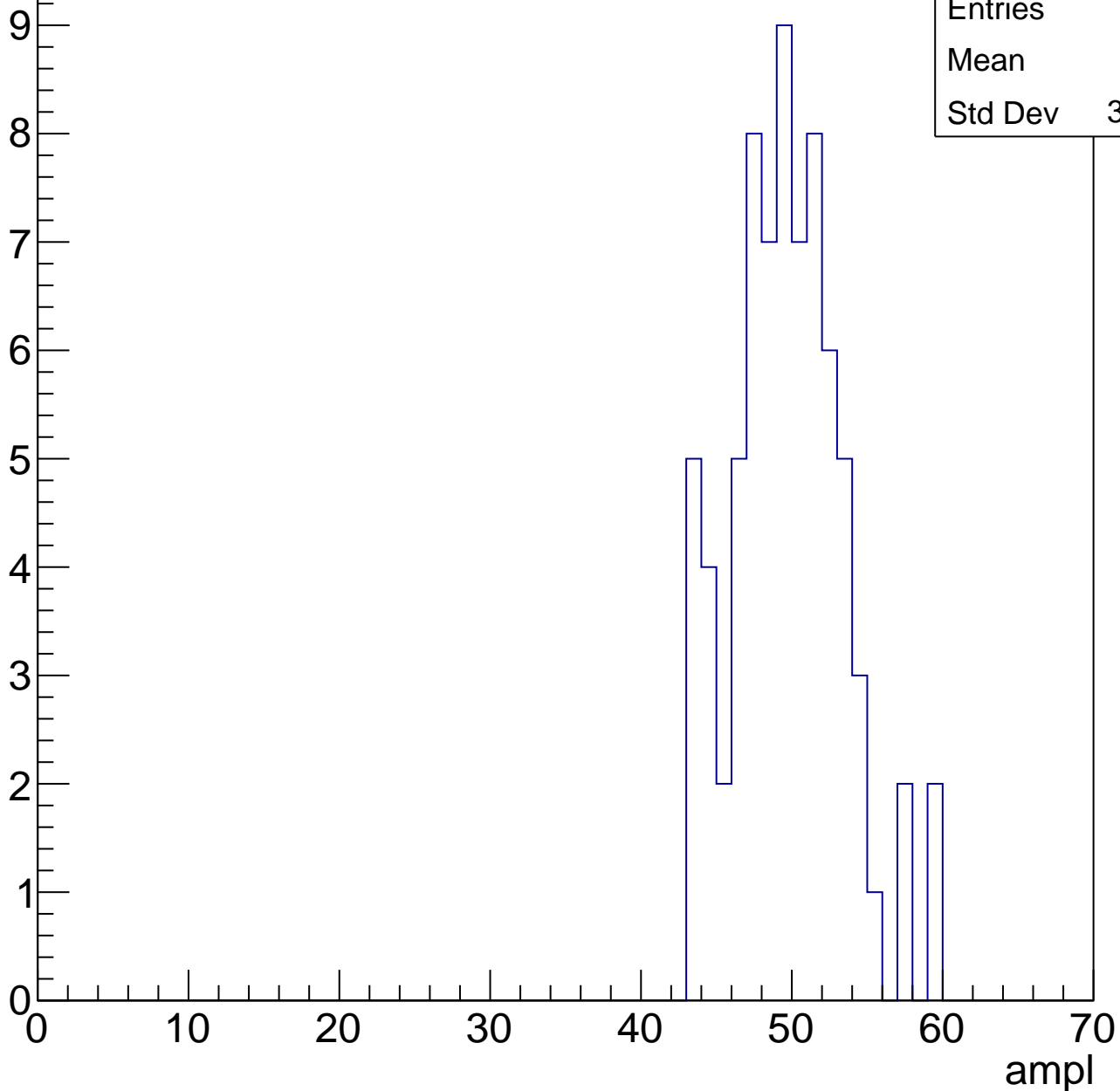


# B0L002S, U2-ch50, adc3

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	74
Mean	49.3
Std Dev	3.679

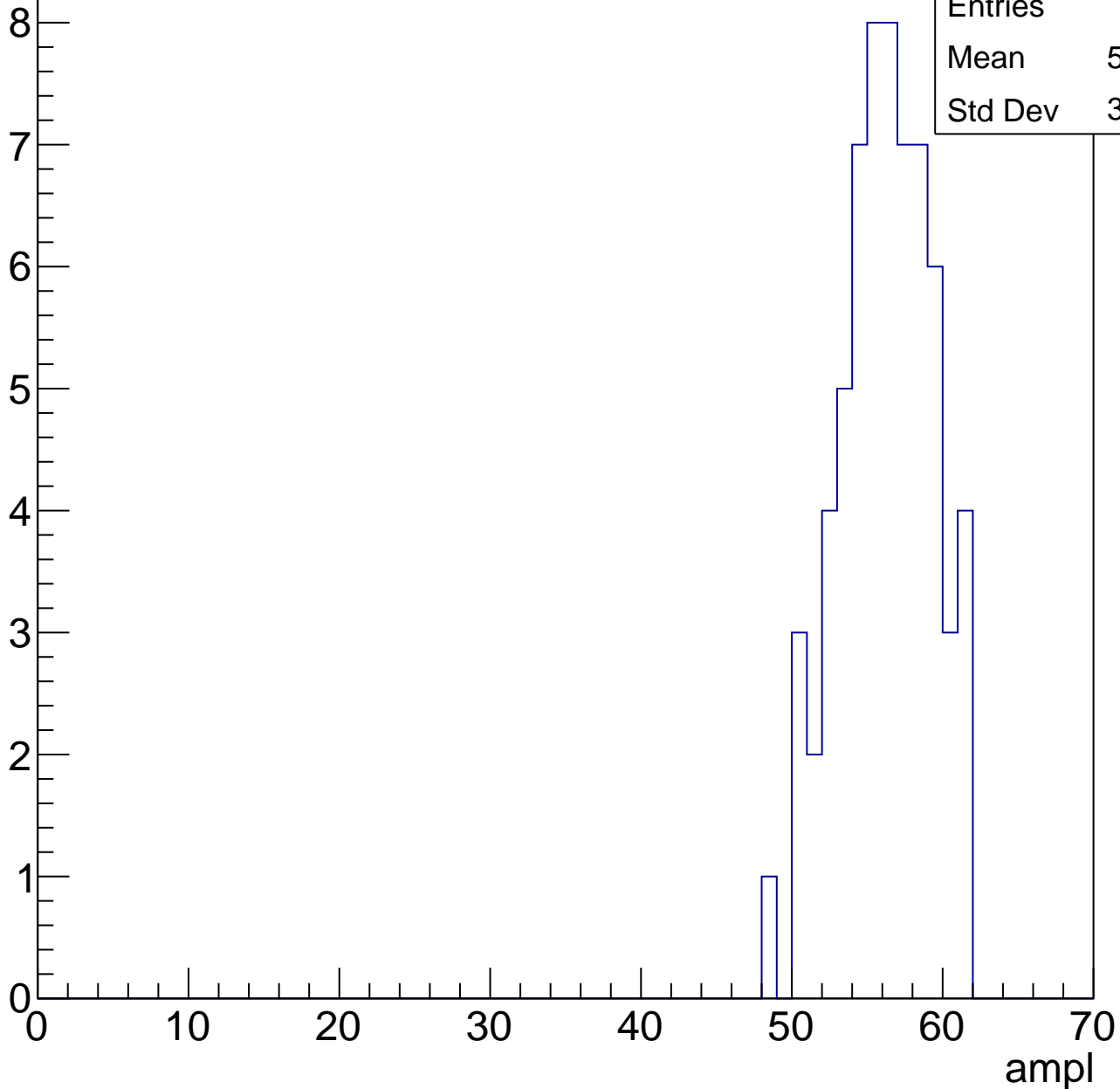


# B0L002S, U2-ch50, adc4

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	65
Mean	55.72
Std Dev	3.036

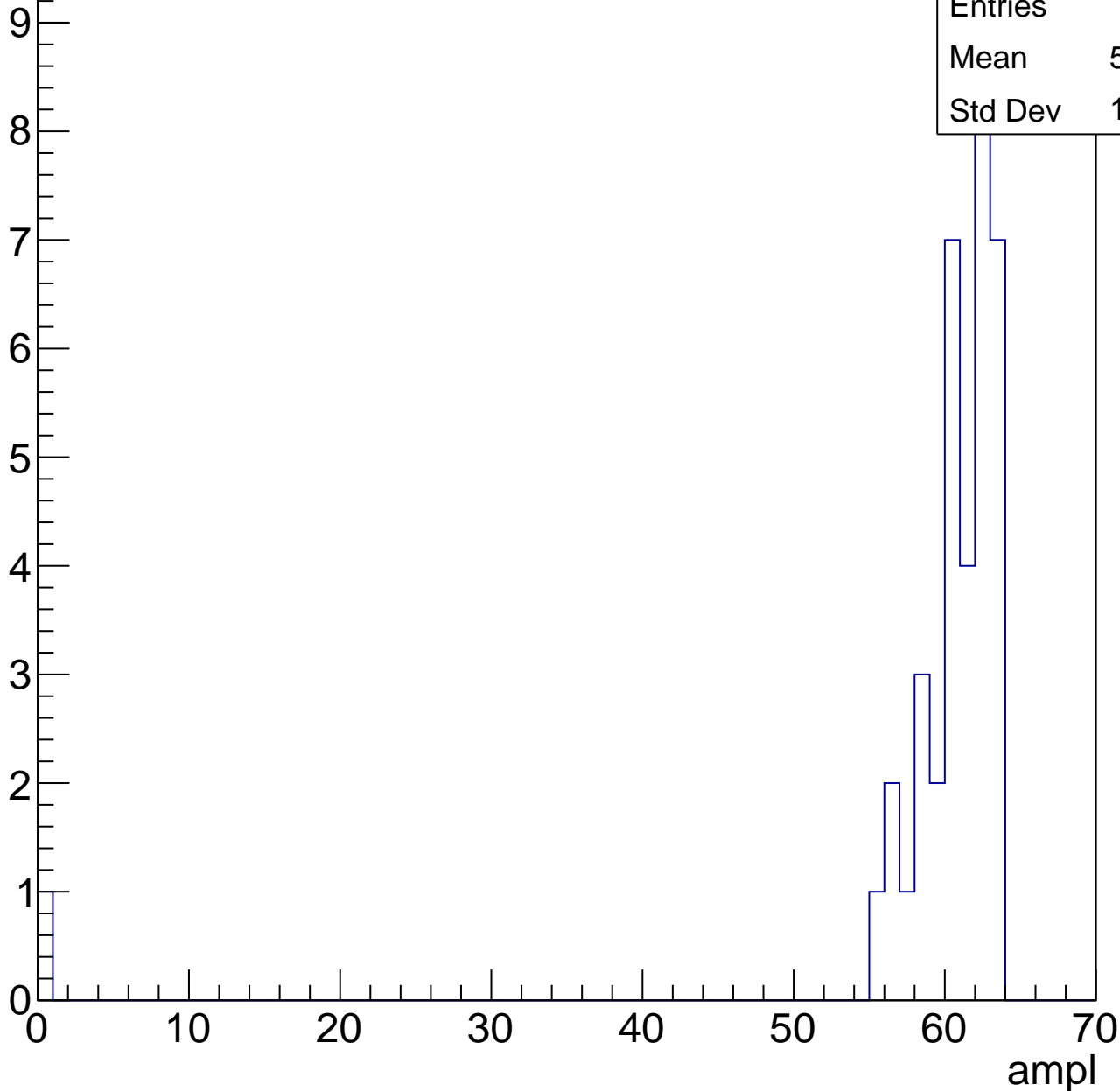


# B0L002S, U2-ch50, adc5

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	37
Mean	58.89
Std Dev	10.05



# B0L002S, U2-ch50, adc6

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry





# B0L002S, U2-ch50, adc7

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



Entries	2
Mean	11
Std Dev	11

# B0L002S, U2-ch51, adc0

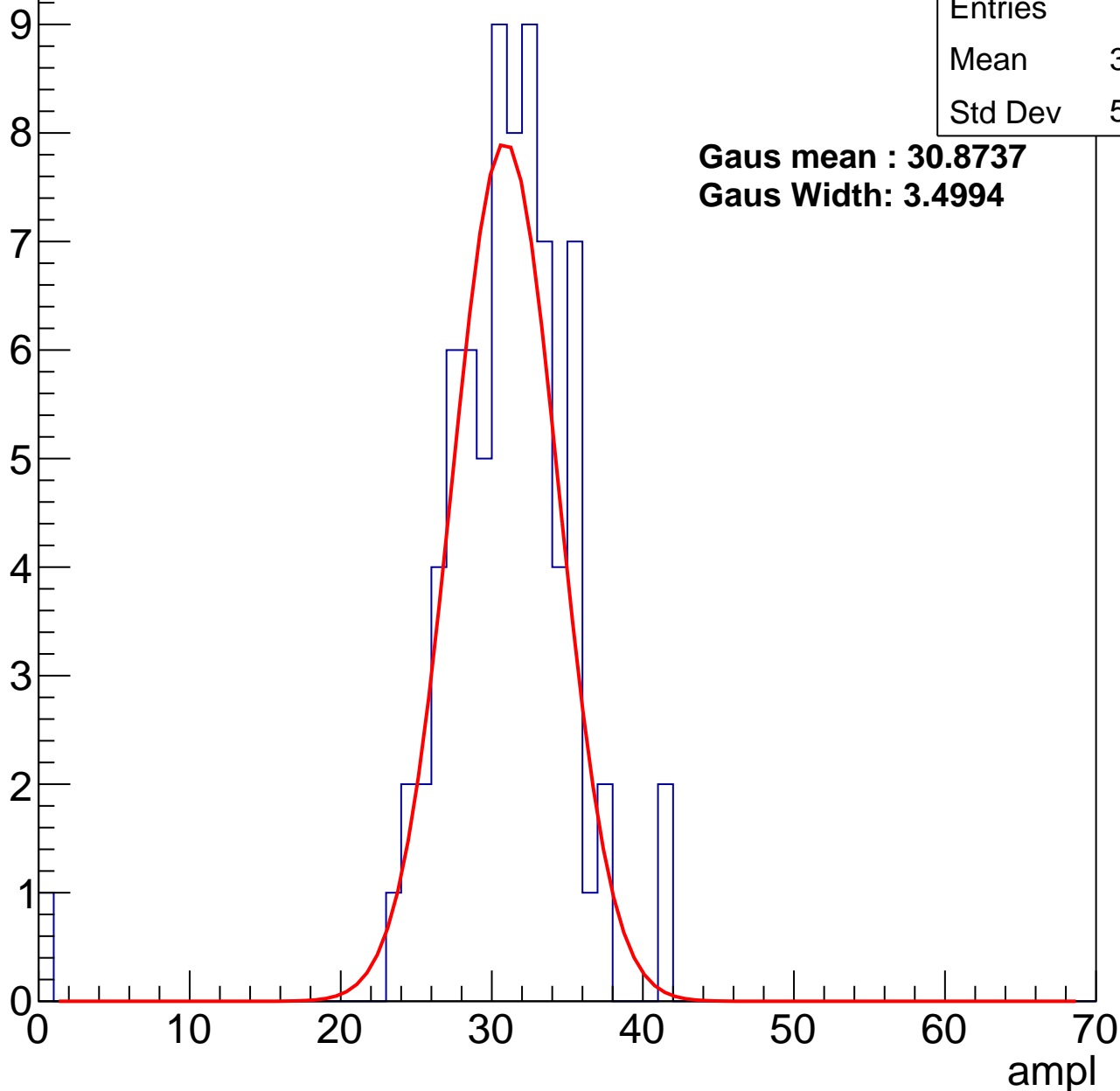
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	76
Mean	30.39
Std Dev	5.037

**Gaus mean : 30.8737**

**Gaus Width: 3.4994**



# B0L002S, U2-ch51, adc1

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entries	82
Mean	38.83
Std Dev	3.432

**Gaus mean : 39.5642**

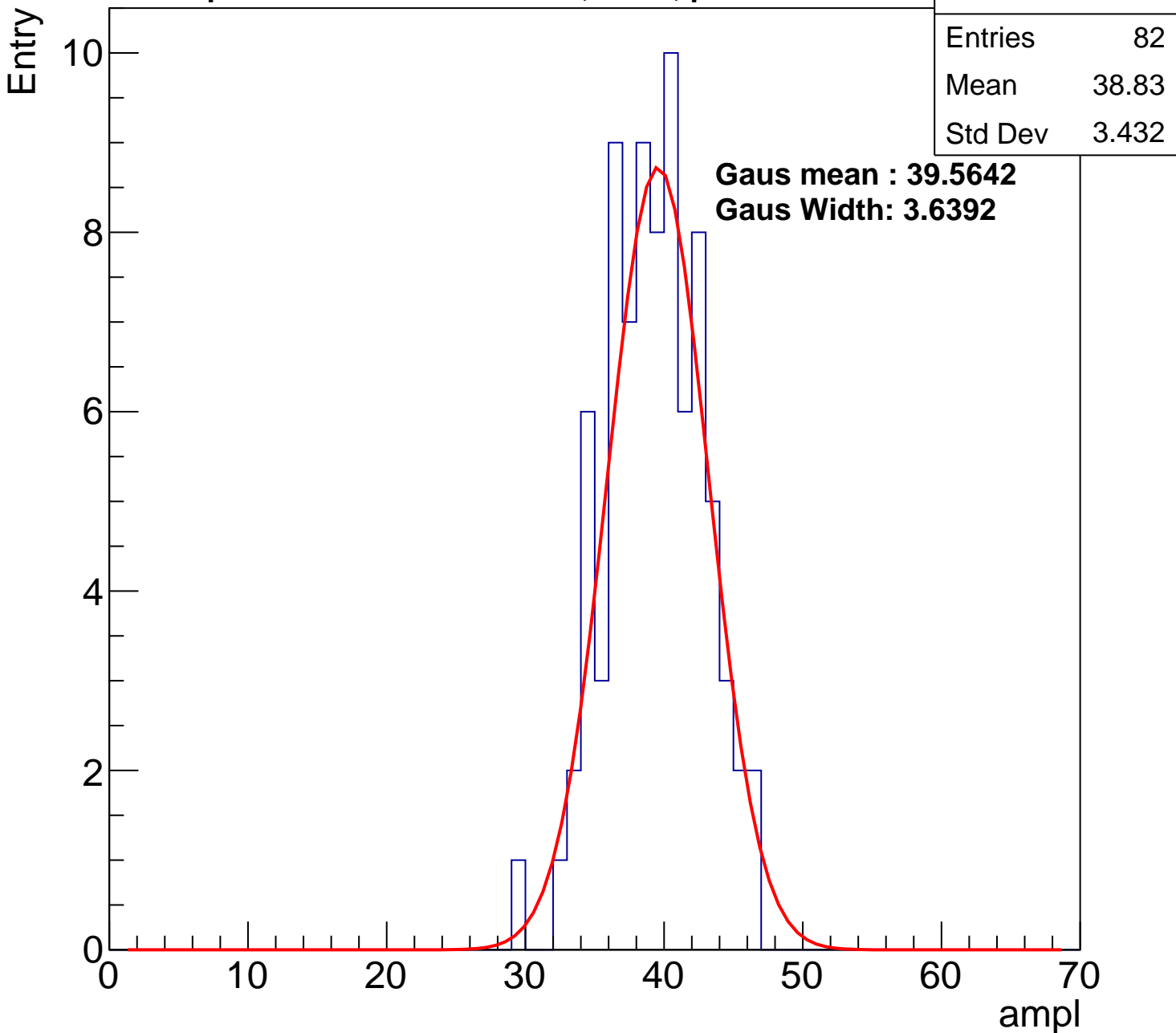
**Gaus Width: 3.6392**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B0L002S, U2-ch51, adc2

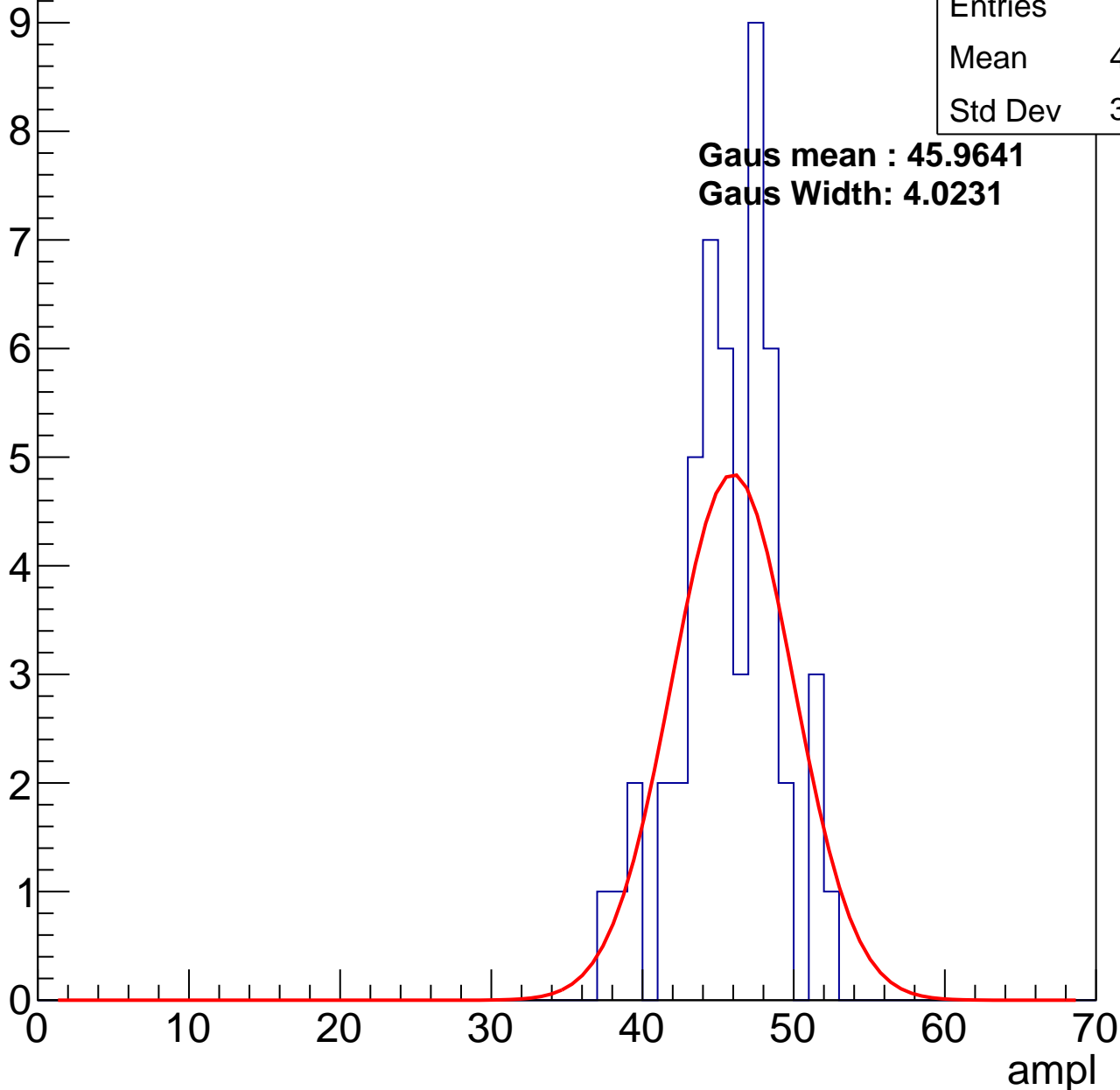
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	50
Mean	45.28
Std Dev	3.287

**Gaus mean : 45.9641**

**Gaus Width: 4.0231**

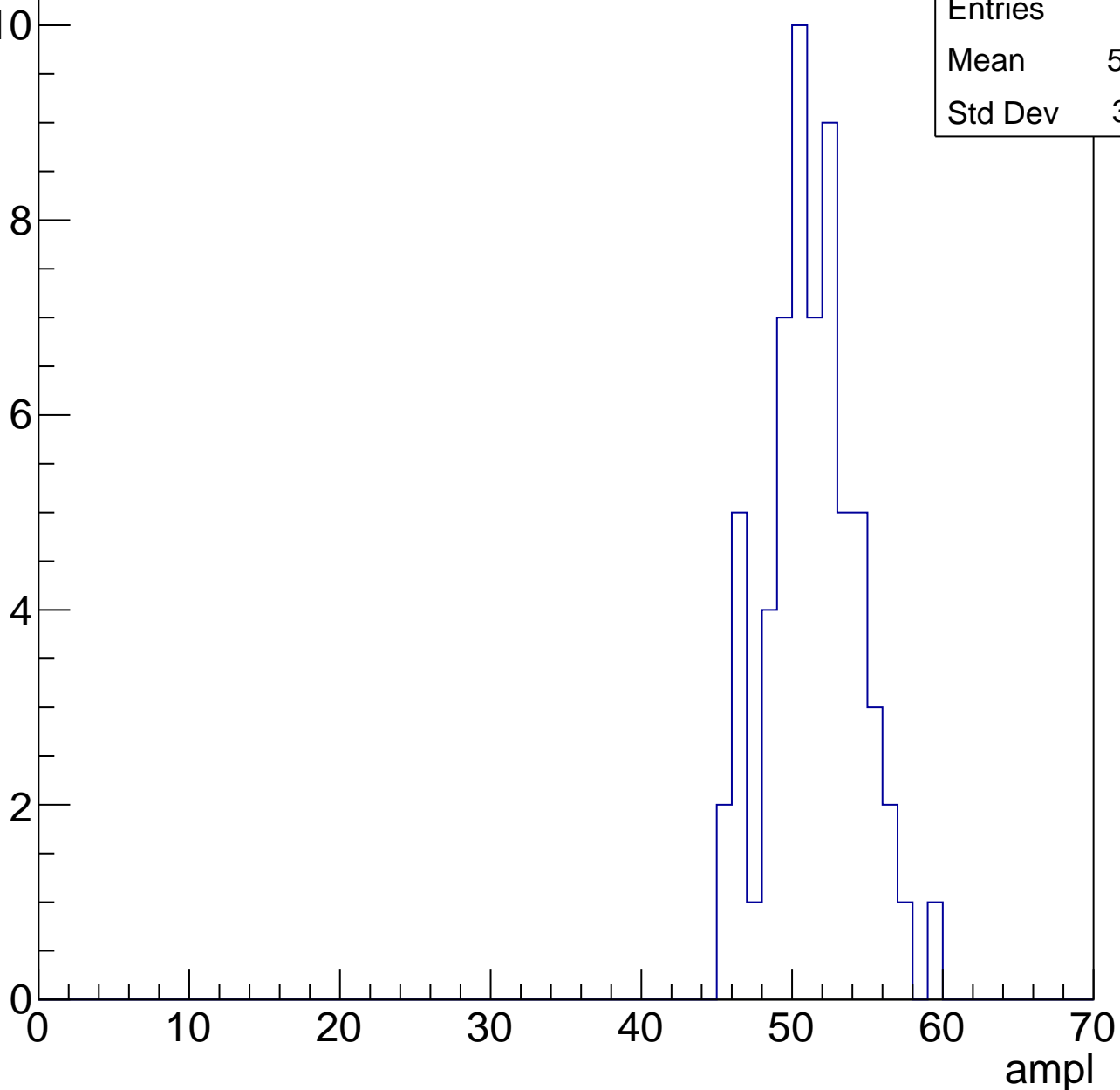


# B0L002S, U2-ch51, adc3

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

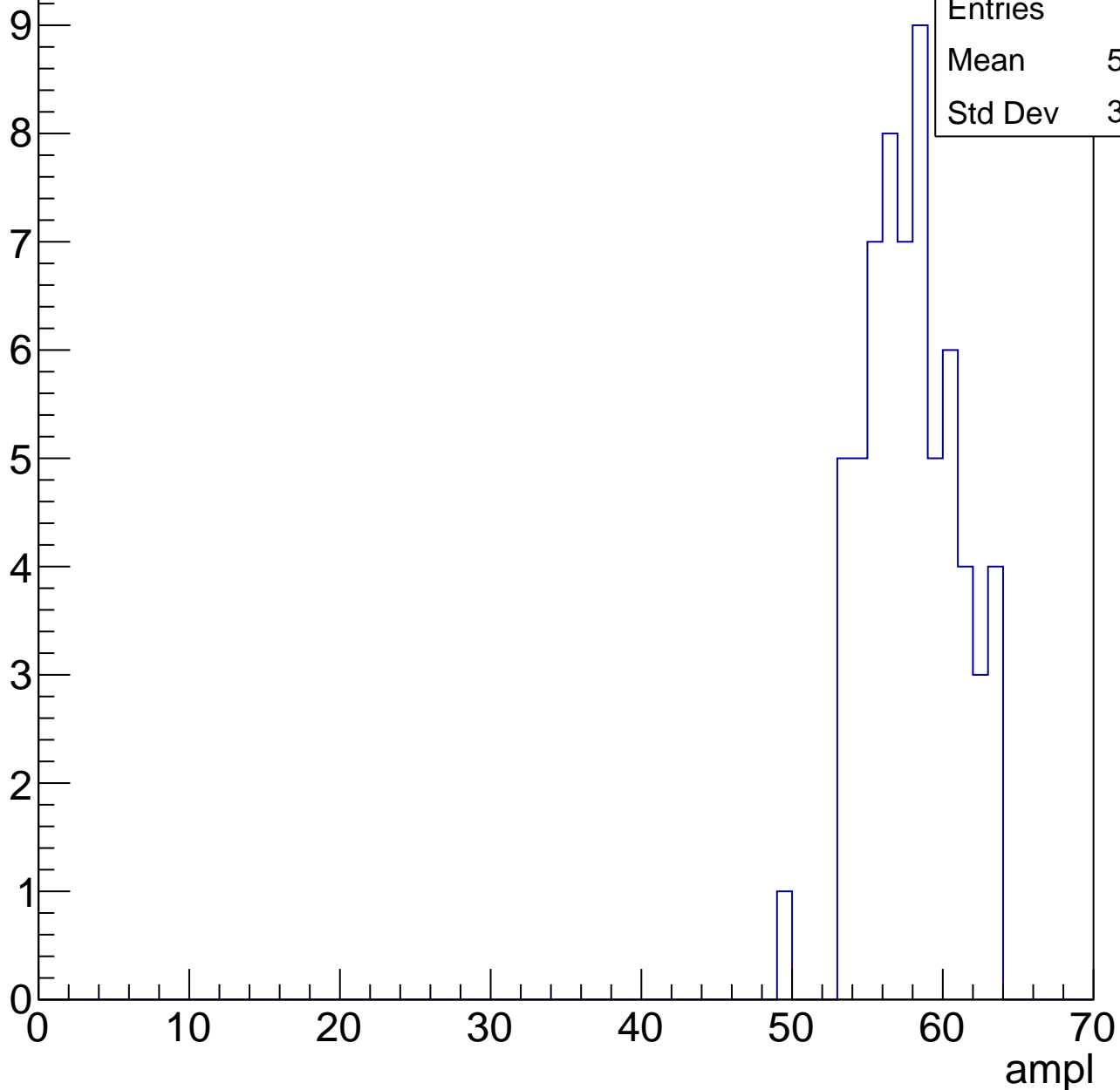
Entries	62
Mean	50.89
Std Dev	3.001



# B0L002S, U2-ch51, adc4

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

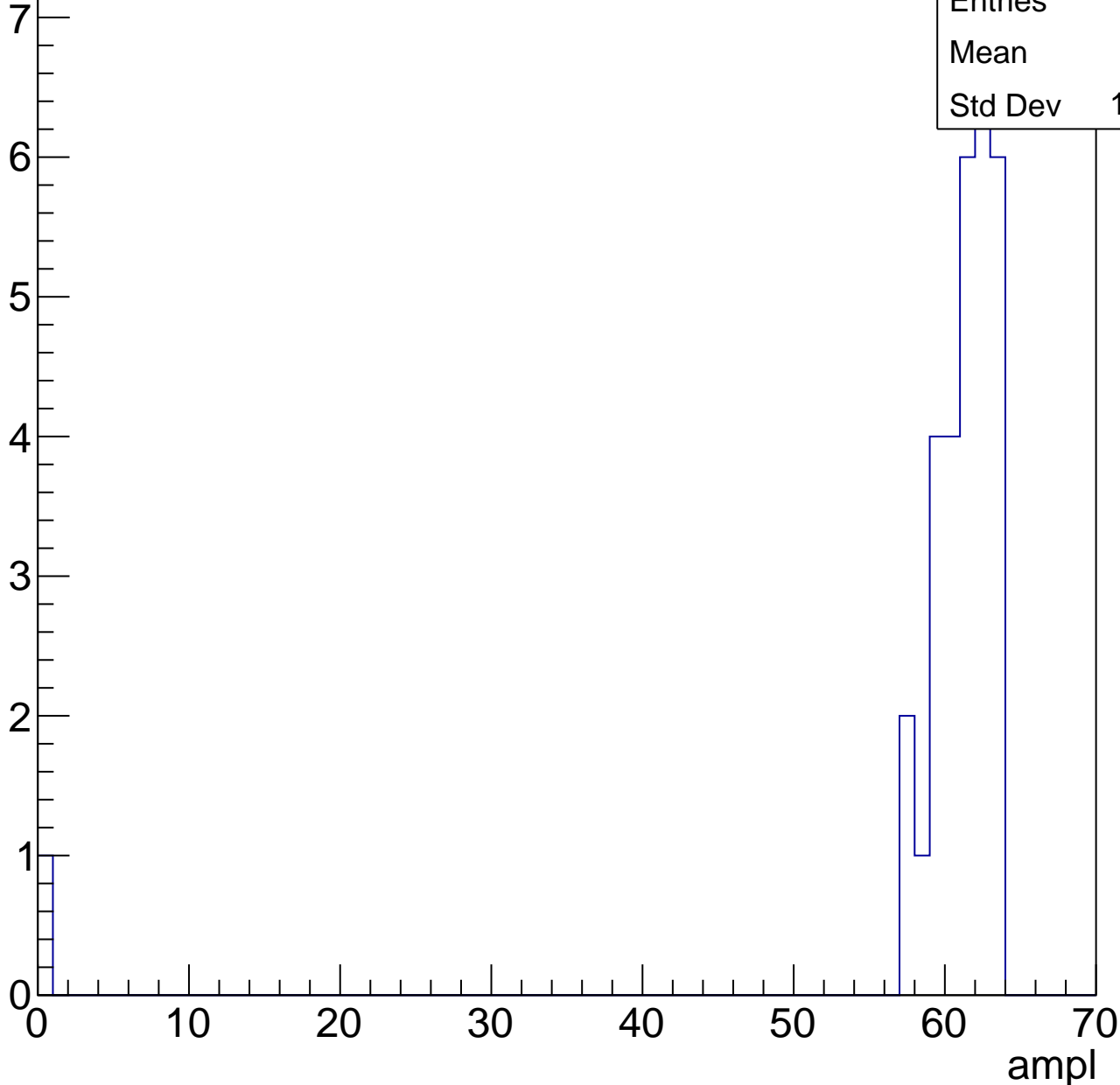


# B0L002S, U2-ch51, adc5

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	31
Mean	58.9
Std Dev	10.89



# B0L002S, U2-ch51, adc6

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



Entries	0
Mean	0
Std Dev	0



# B0L002S, U2-ch51, adc7

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



# B0L002S, U2-ch52, adc0

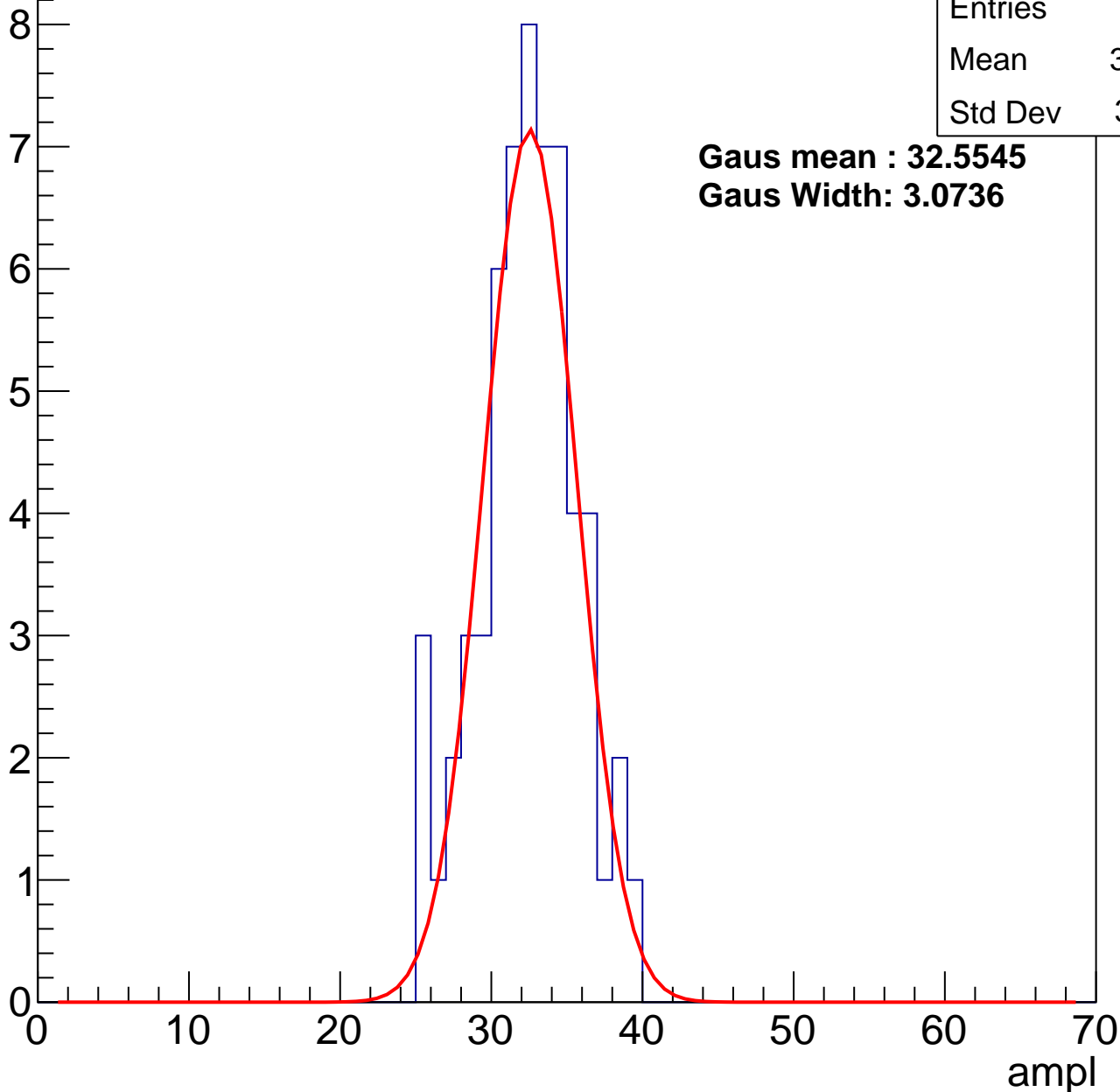
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	59
Mean	31.93
Std Dev	3.241

**Gaus mean : 32.5545**

**Gaus Width: 3.0736**



# B0L002S, U2-ch52, adc1

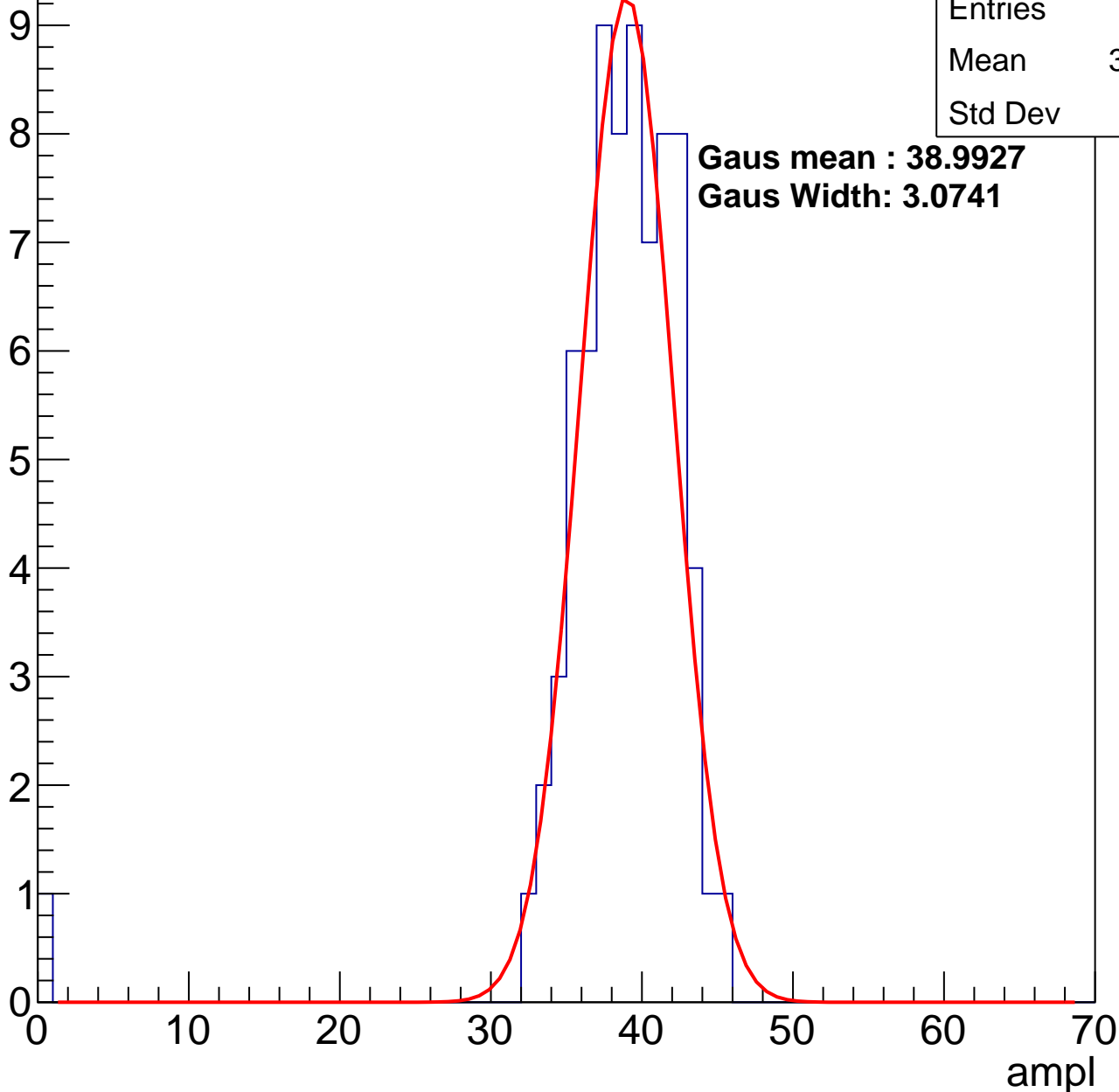
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	74
Mean	38.09
Std Dev	5.31

**Gaus mean : 38.9927**

**Gaus Width: 3.0741**

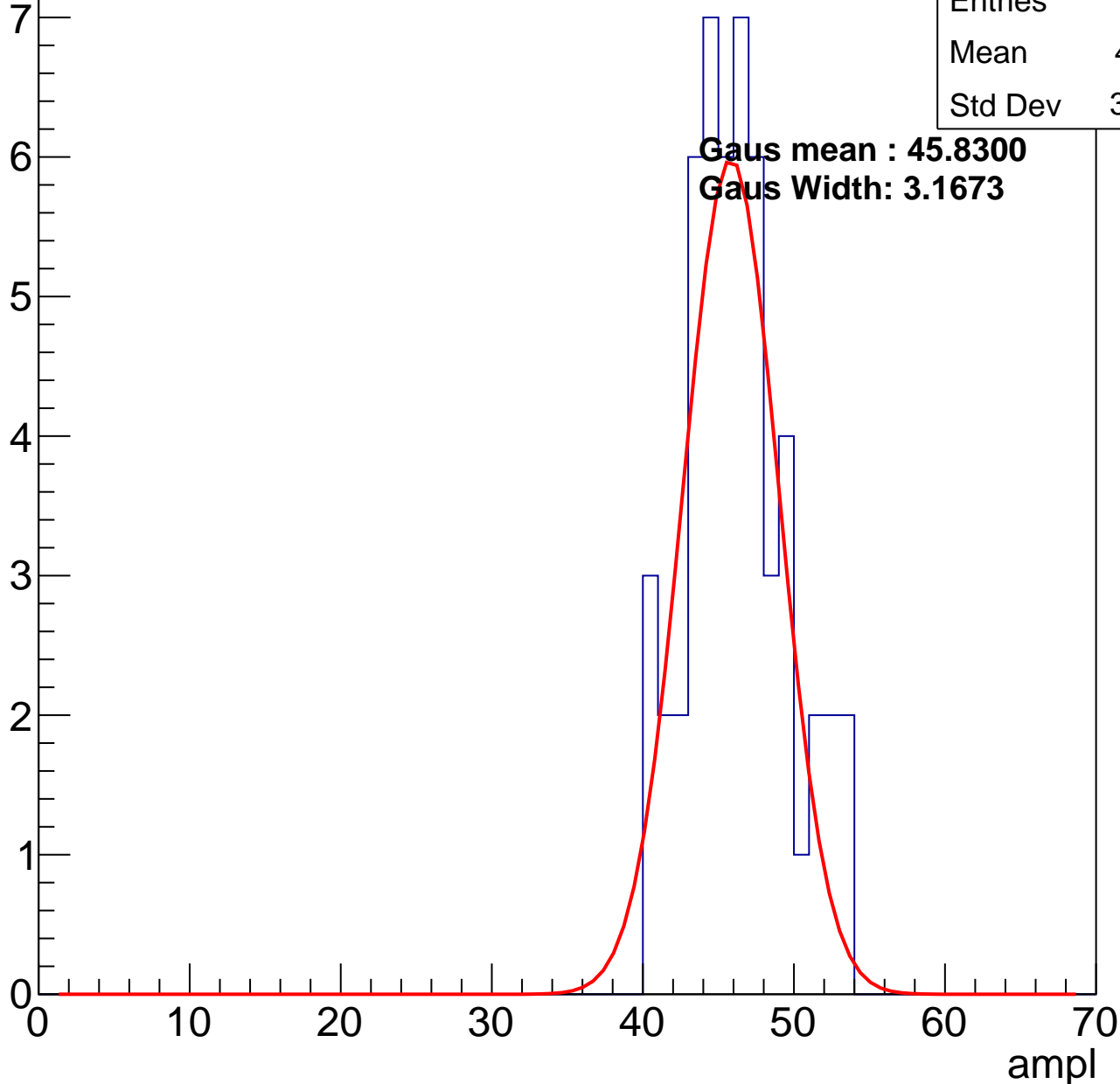


# B0L002S, U2-ch52, adc2

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

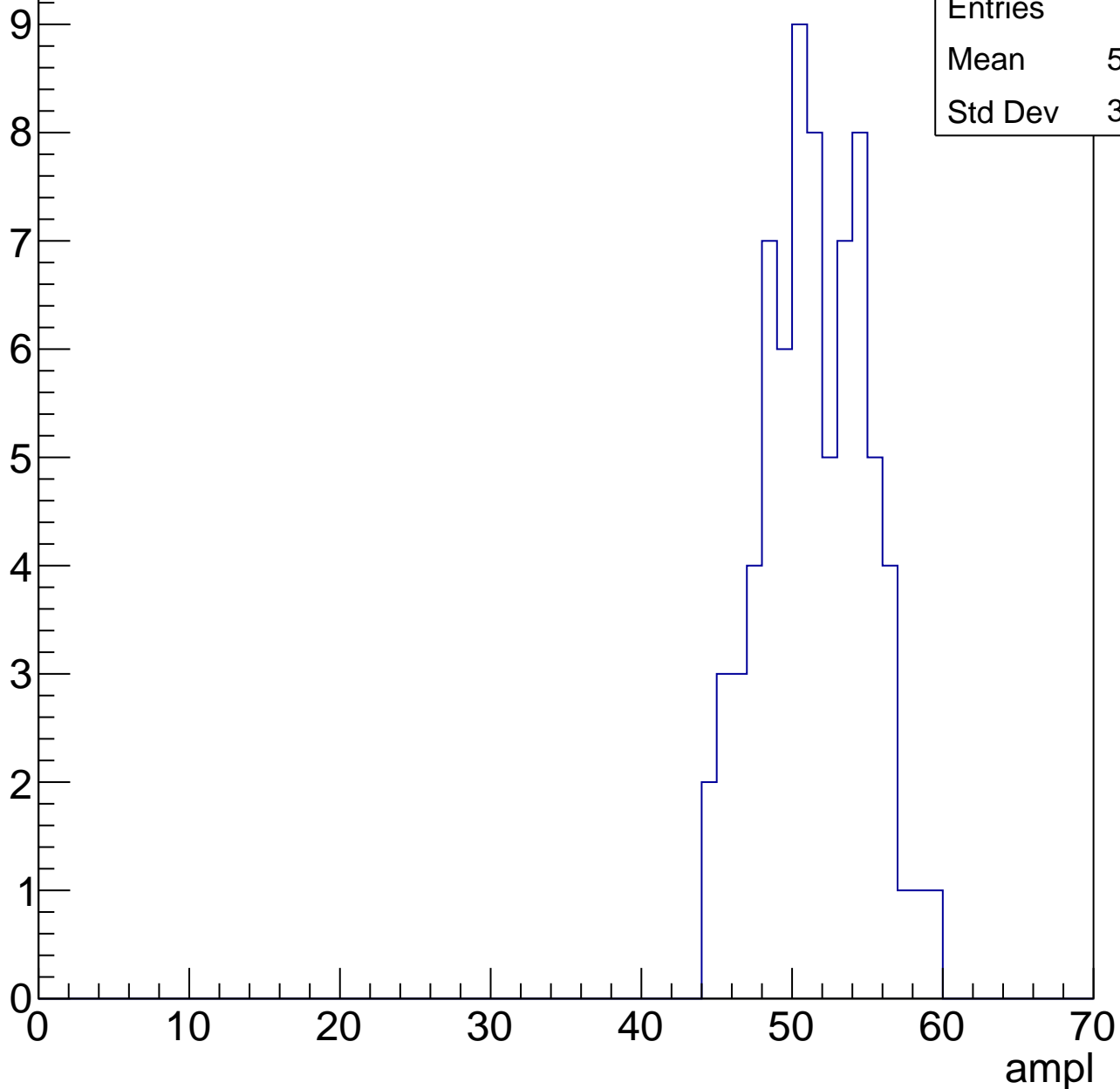
Entries	53
Mean	45.81
Std Dev	3.268



# B0L002S, U2-ch52, adc3

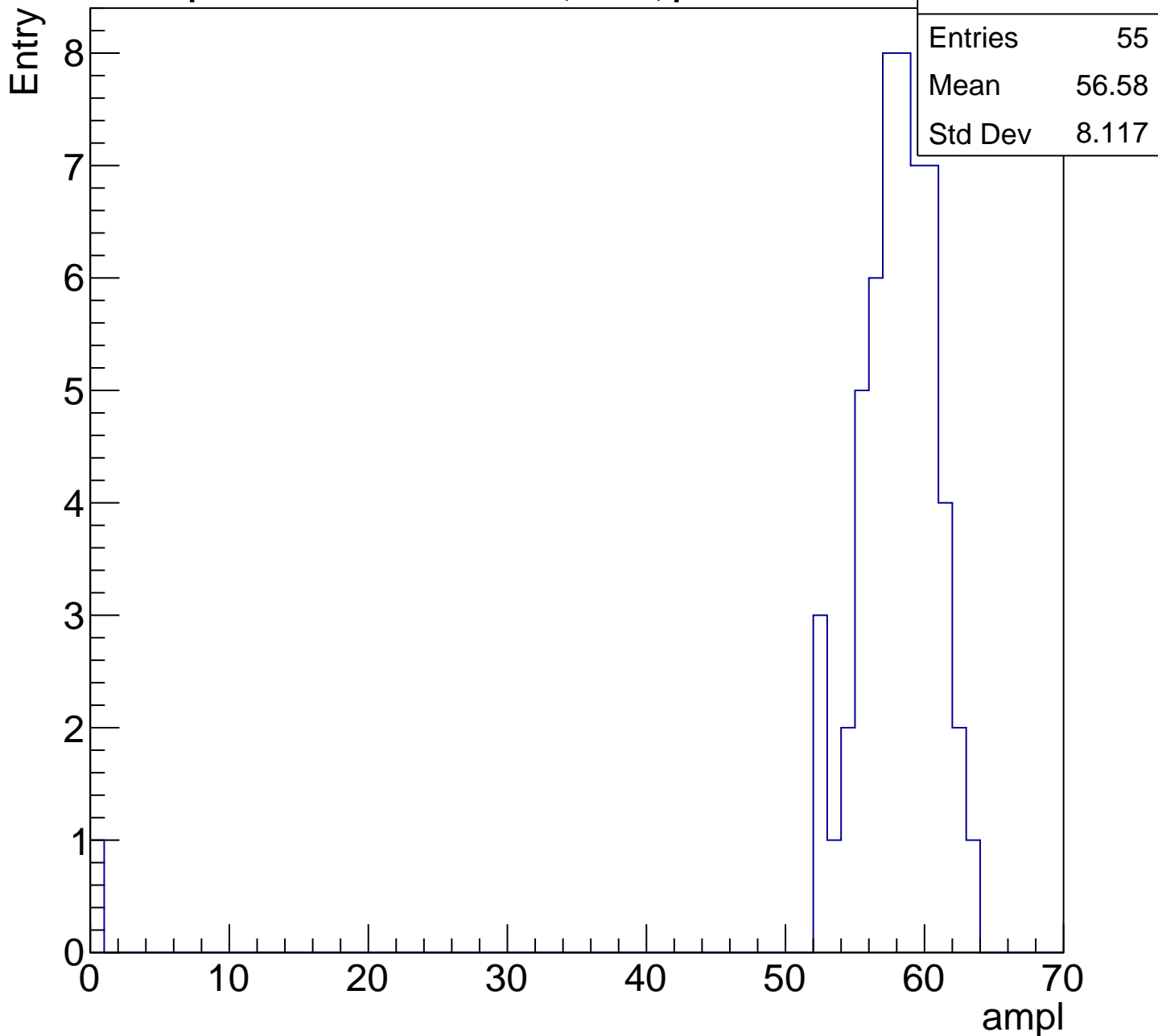
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



# B0L002S, U2-ch52, adc4

calib\_packv5\_042523\_0143.root, FC#8, port C1

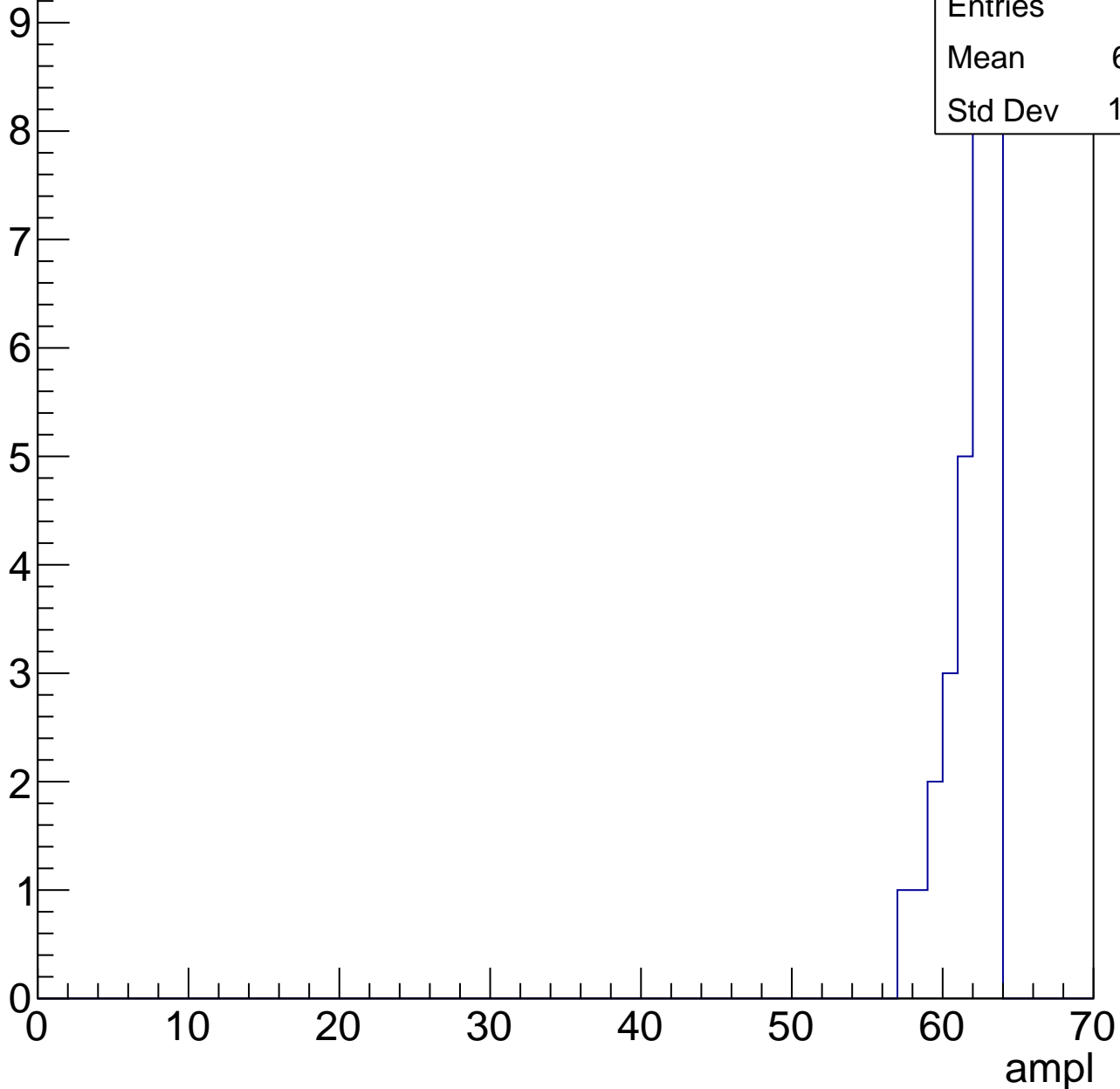


# B0L002S, U2-ch52, adc5

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	29
Mean	61.41
Std Dev	1.609



# B0L002S, U2-ch52, adc6

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry





# B0L002S, U2-ch52, adc7

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L002S, U2-ch53, adc0

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entries	72
Mean	28.06
Std Dev	7.431

**Gaus mean : 29.3755**

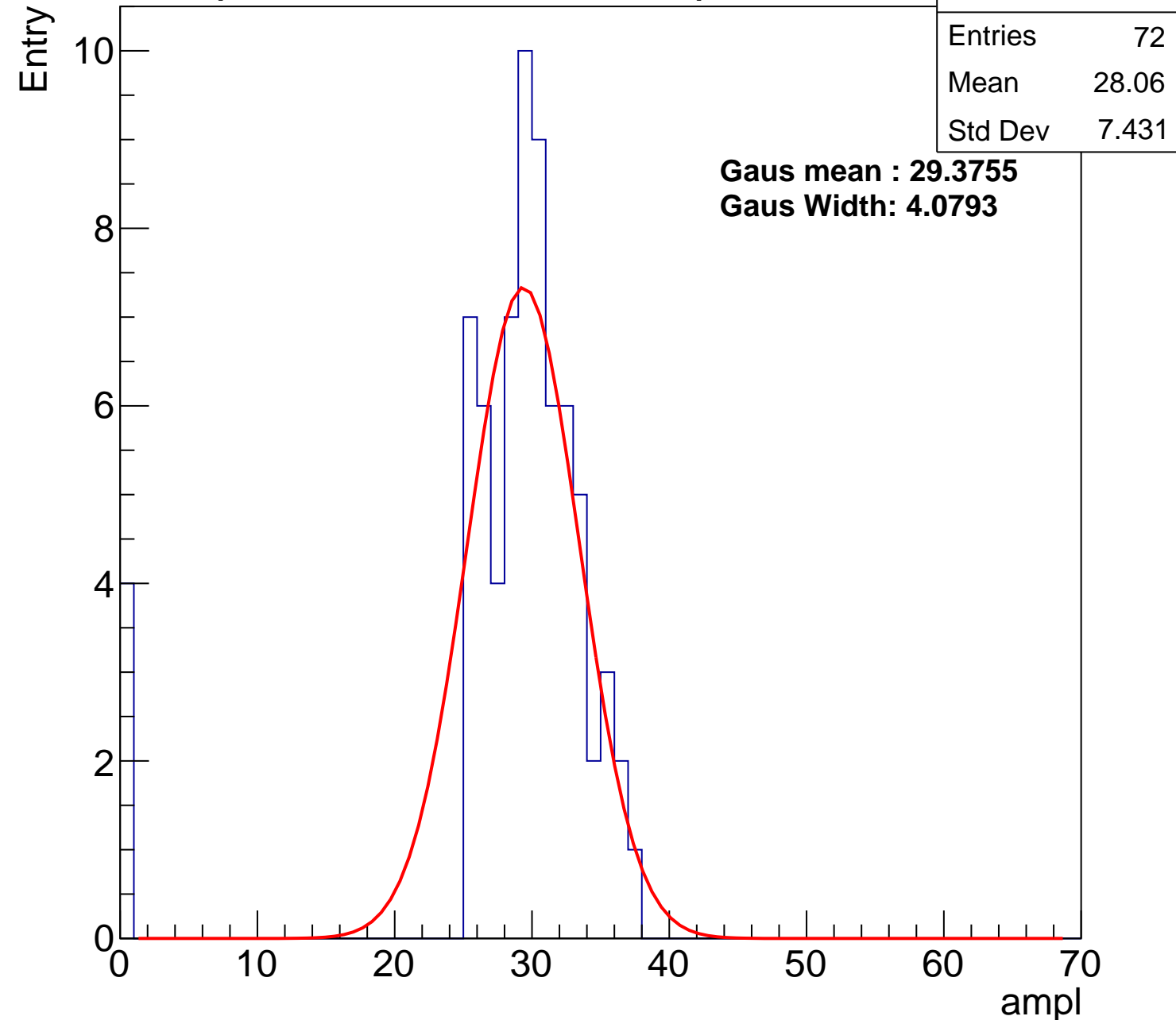
**Gaus Width: 4.0793**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L002S, U2-ch53, adc1

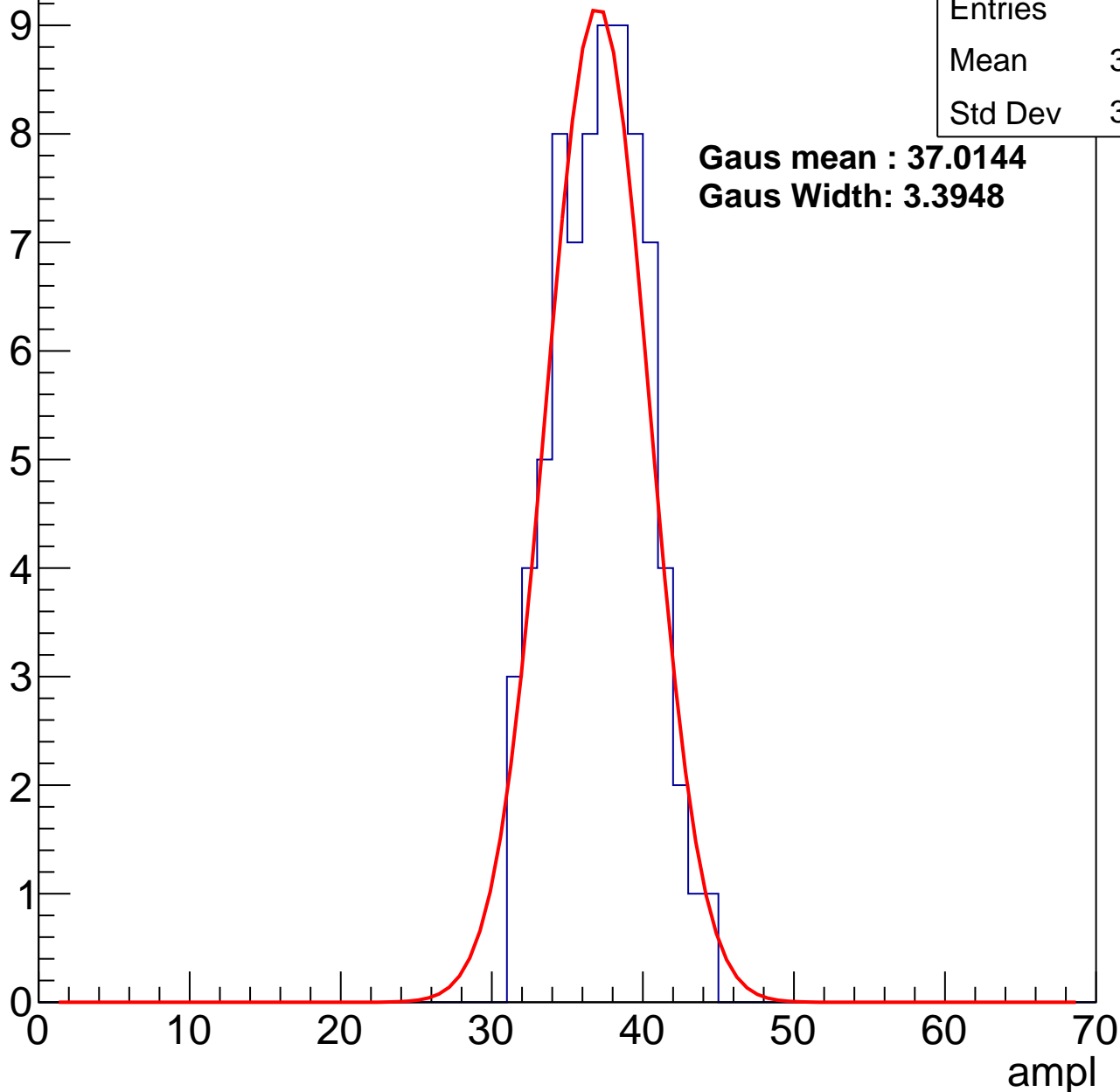
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	76
Mean	36.75
Std Dev	3.022

**Gaus mean : 37.0144**

**Gaus Width: 3.3948**



# B0L002S, U2-ch53, adc2

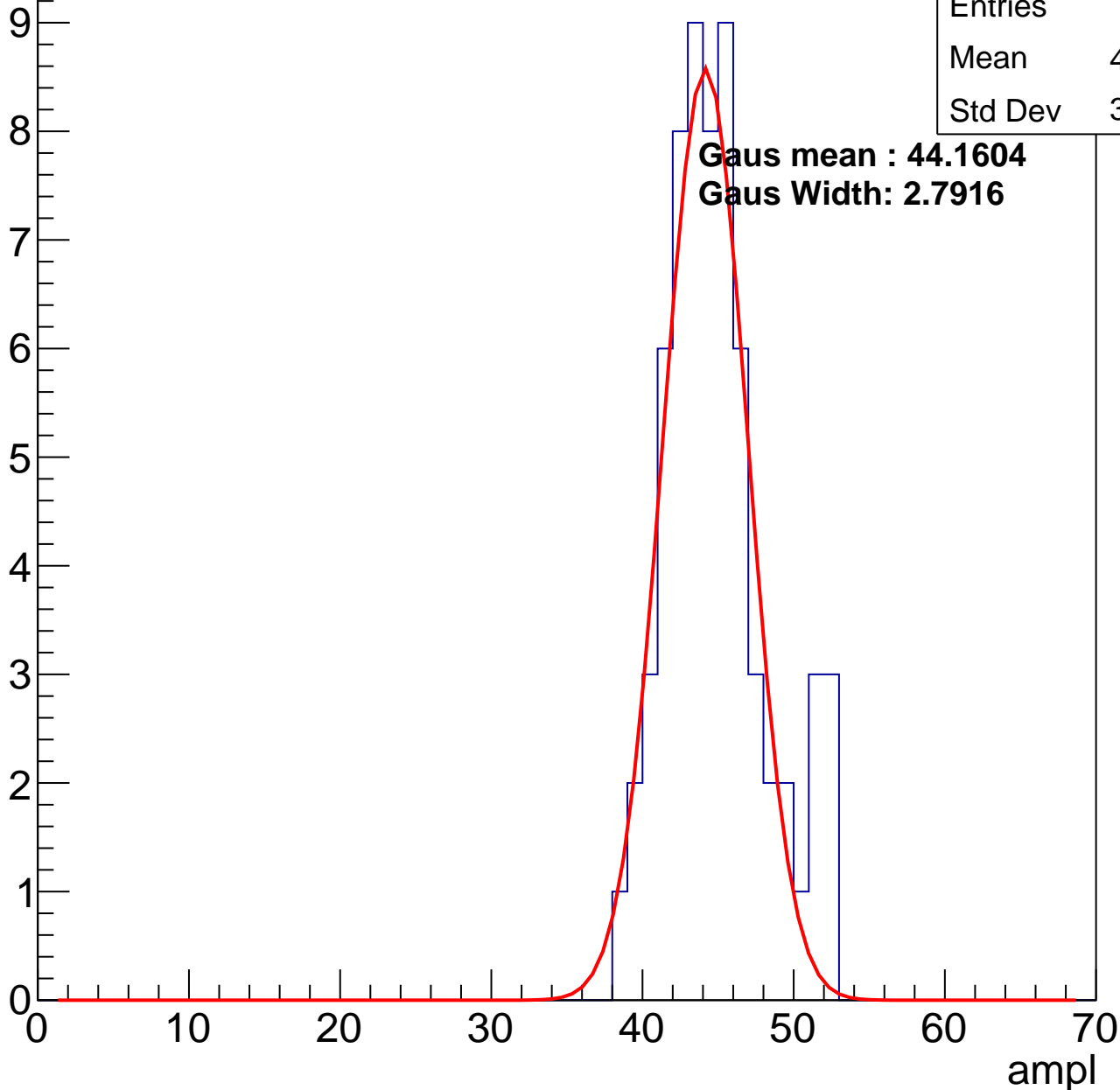
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	66
Mean	44.42
Std Dev	3.335

**Gaus mean : 44.1604**

**Gaus Width: 2.7916**

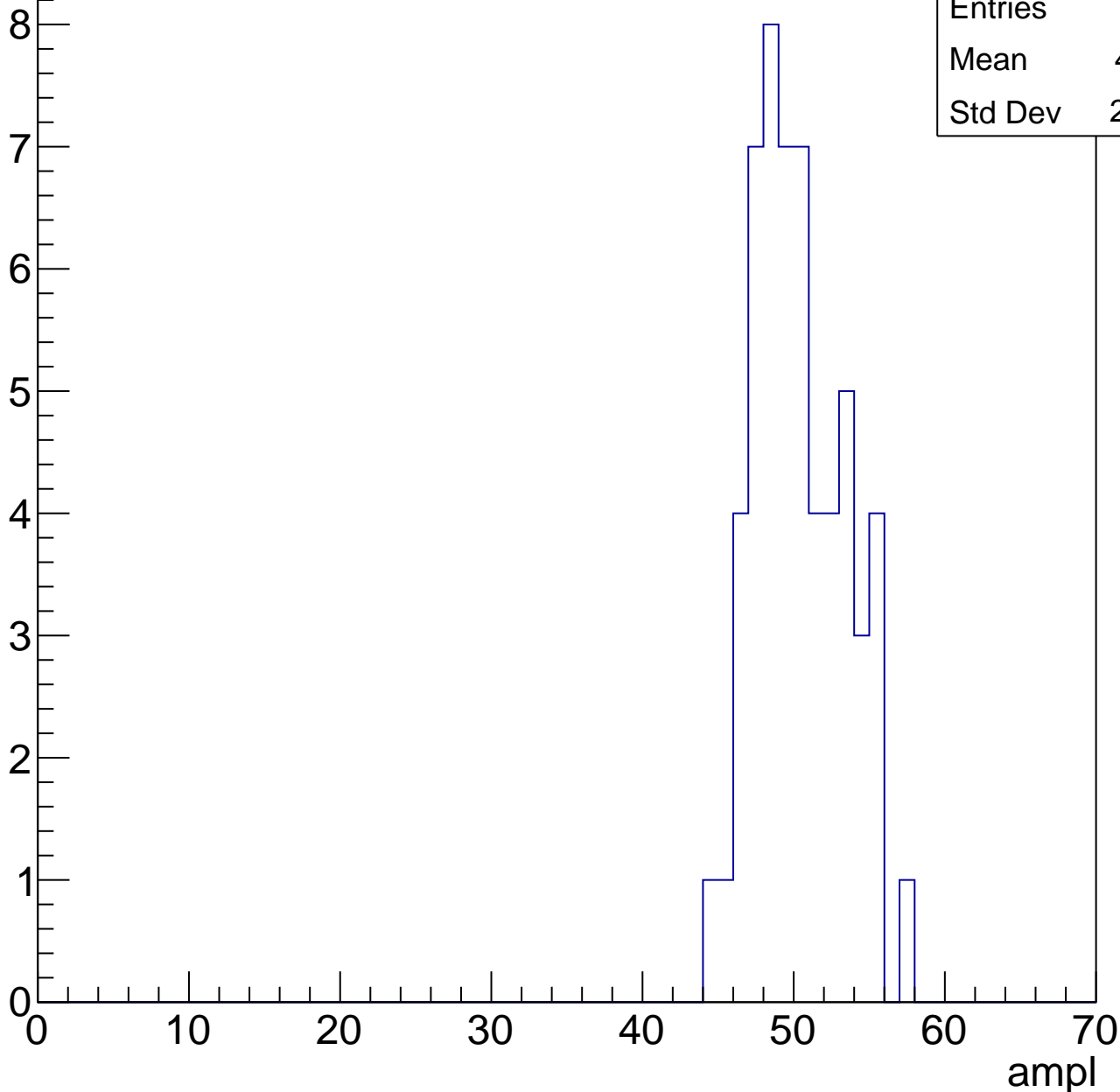


# B0L002S, U2-ch53, adc3

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	56
Mean	49.91
Std Dev	2.954



# B0L002S, U2-ch53, adc4

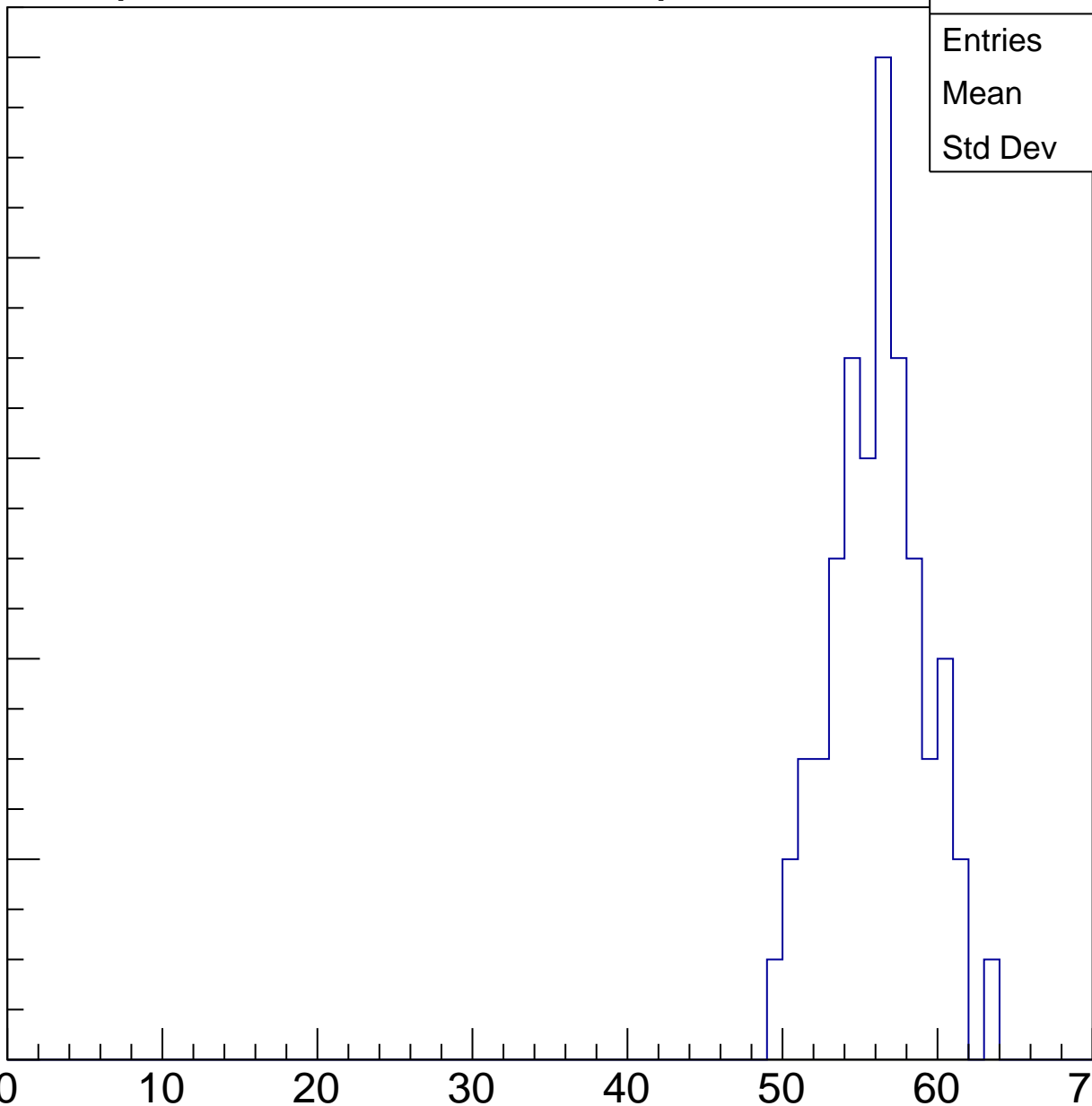
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

10  
8  
6  
4  
2  
0

Entries	59
Mean	55.63
Std Dev	3.002

ampl



# B0L002S, U2-ch53, adc5

calib\_packv5\_042523\_0143.root, FC#8, port C1

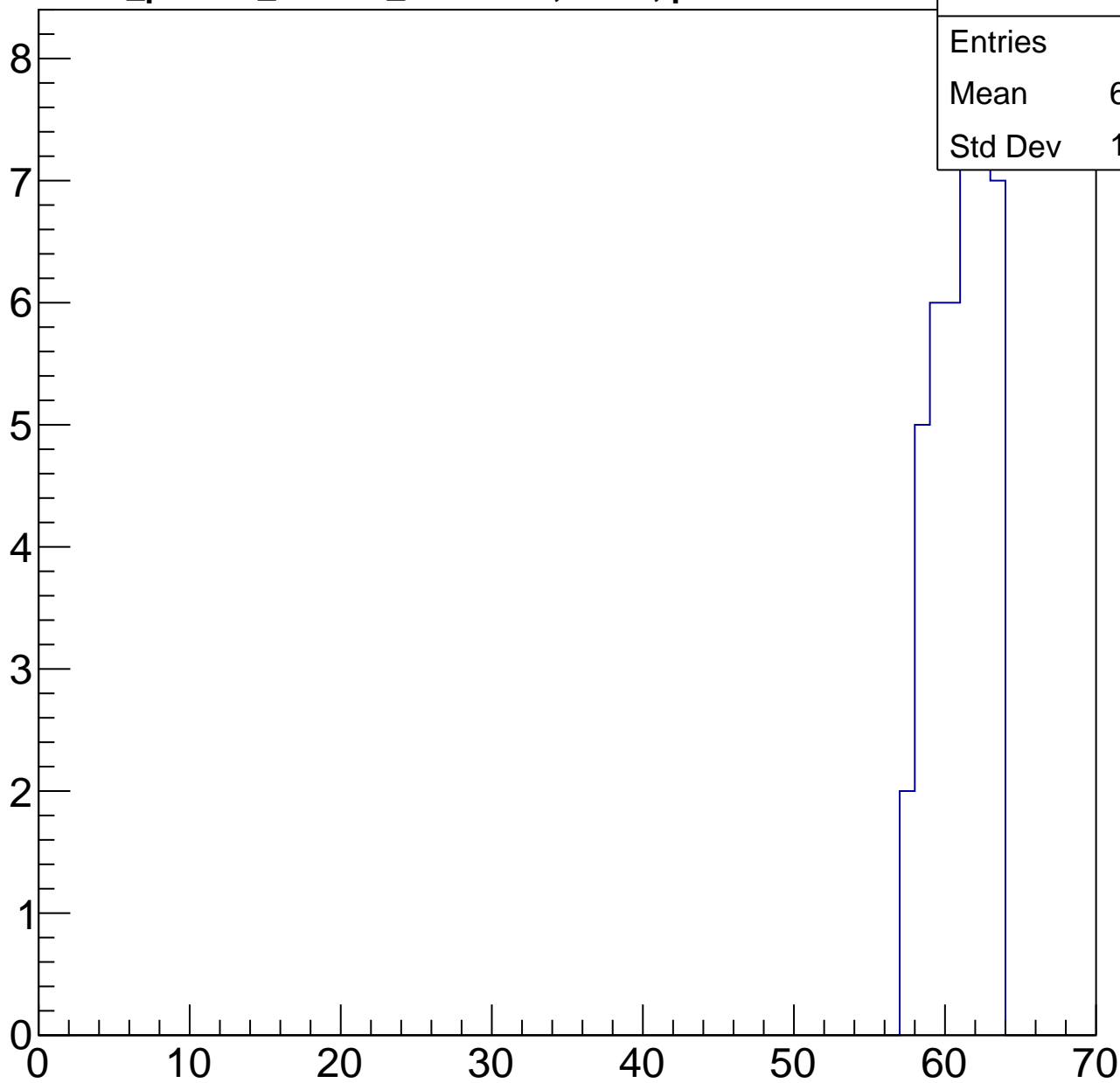
Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	42
Mean	60.55
Std Dev	1.789

ampl

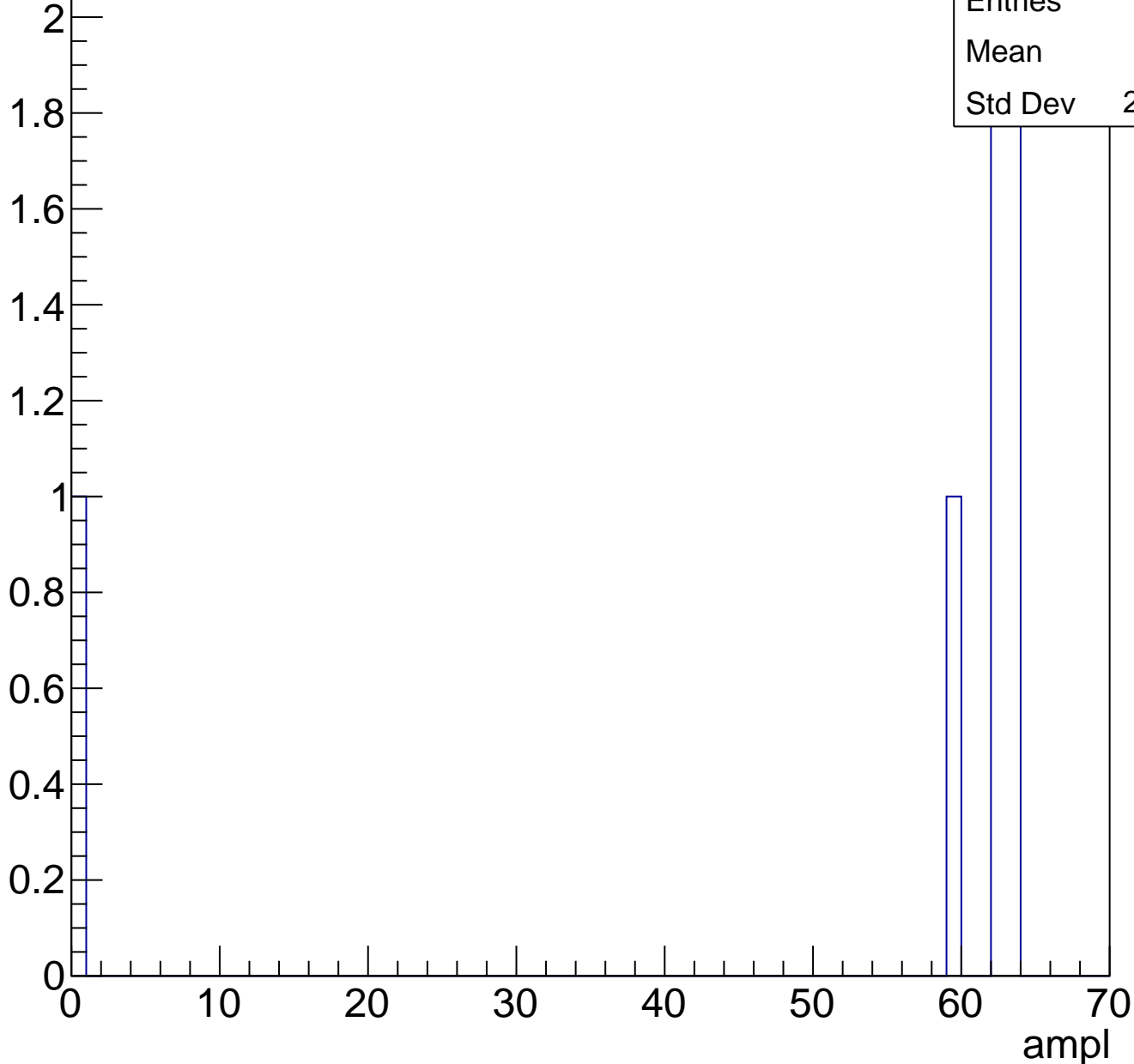
0 10 20 30 40 50 60 70



# B0L002S, U2-ch53, adc6

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry





# B0L002S, U2-ch53, adc7

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L002S, U2-ch54, adc0

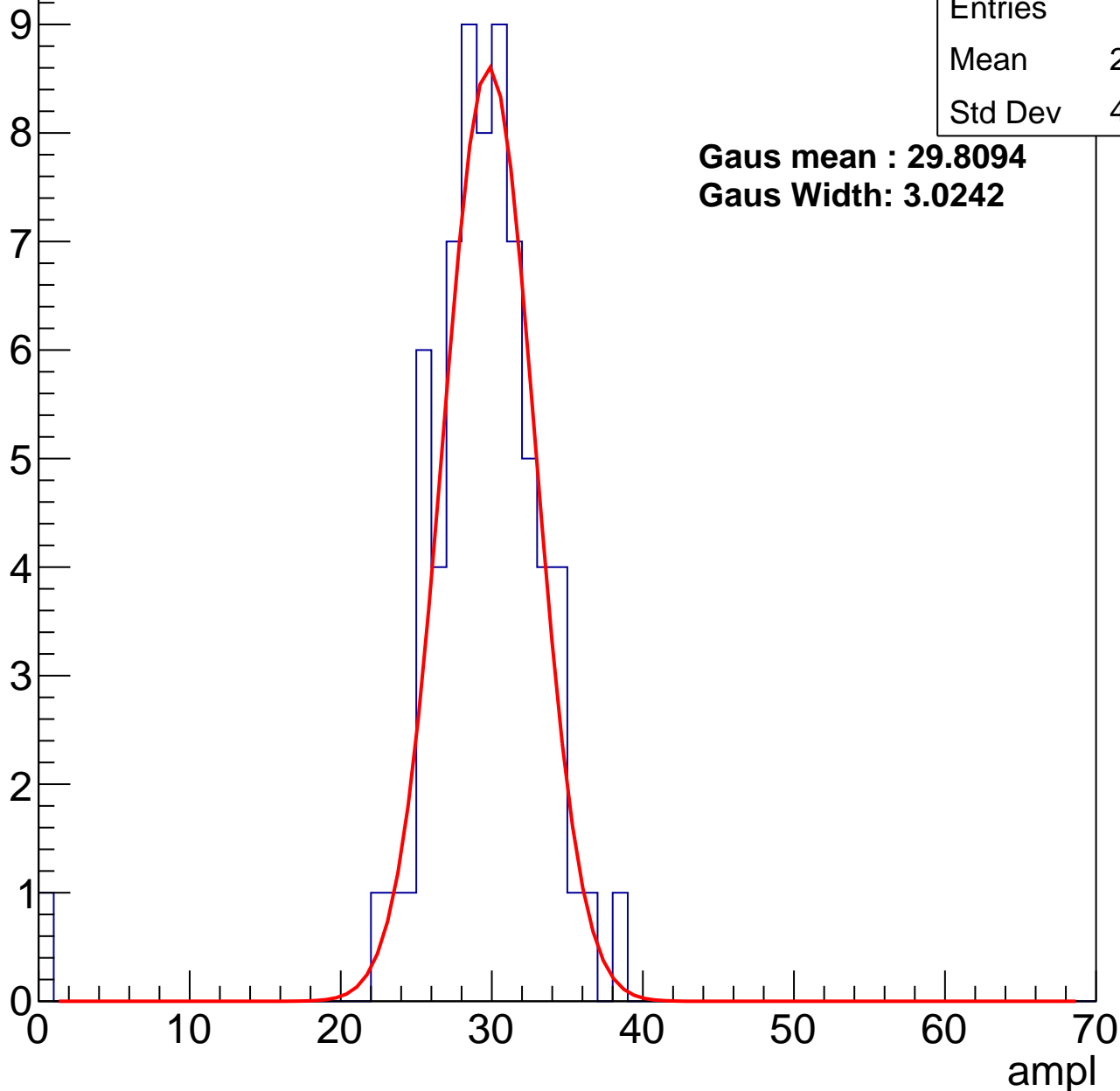
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	70
Mean	28.86
Std Dev	4.676

**Gaus mean : 29.8094**

**Gaus Width: 3.0242**



# B0L002S, U2-ch54, adc1

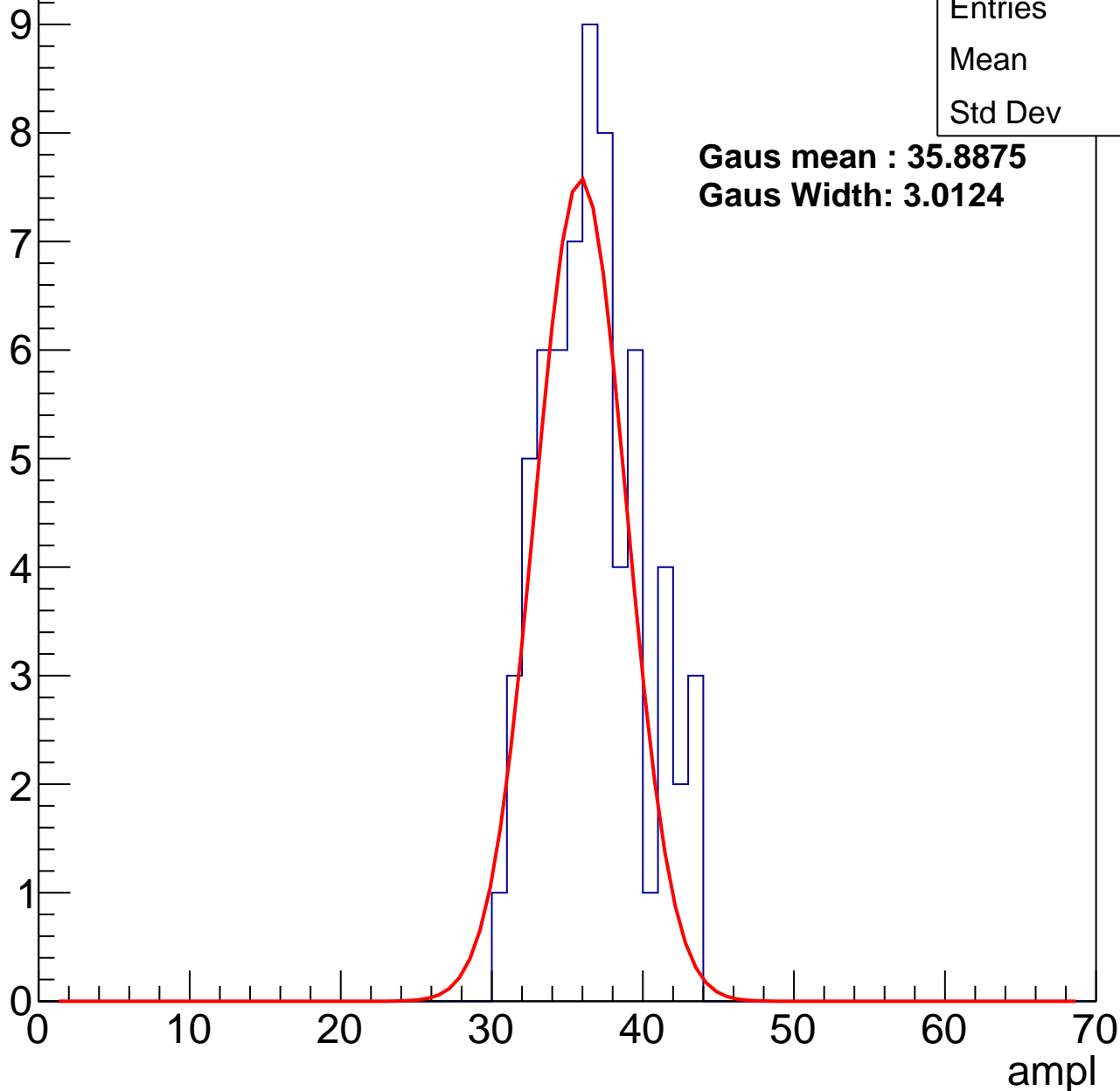
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	65
Mean	36.2
Std Dev	3.25

**Gaus mean : 35.8875**

**Gaus Width: 3.0124**



# B0L002S, U2-ch54, adc2

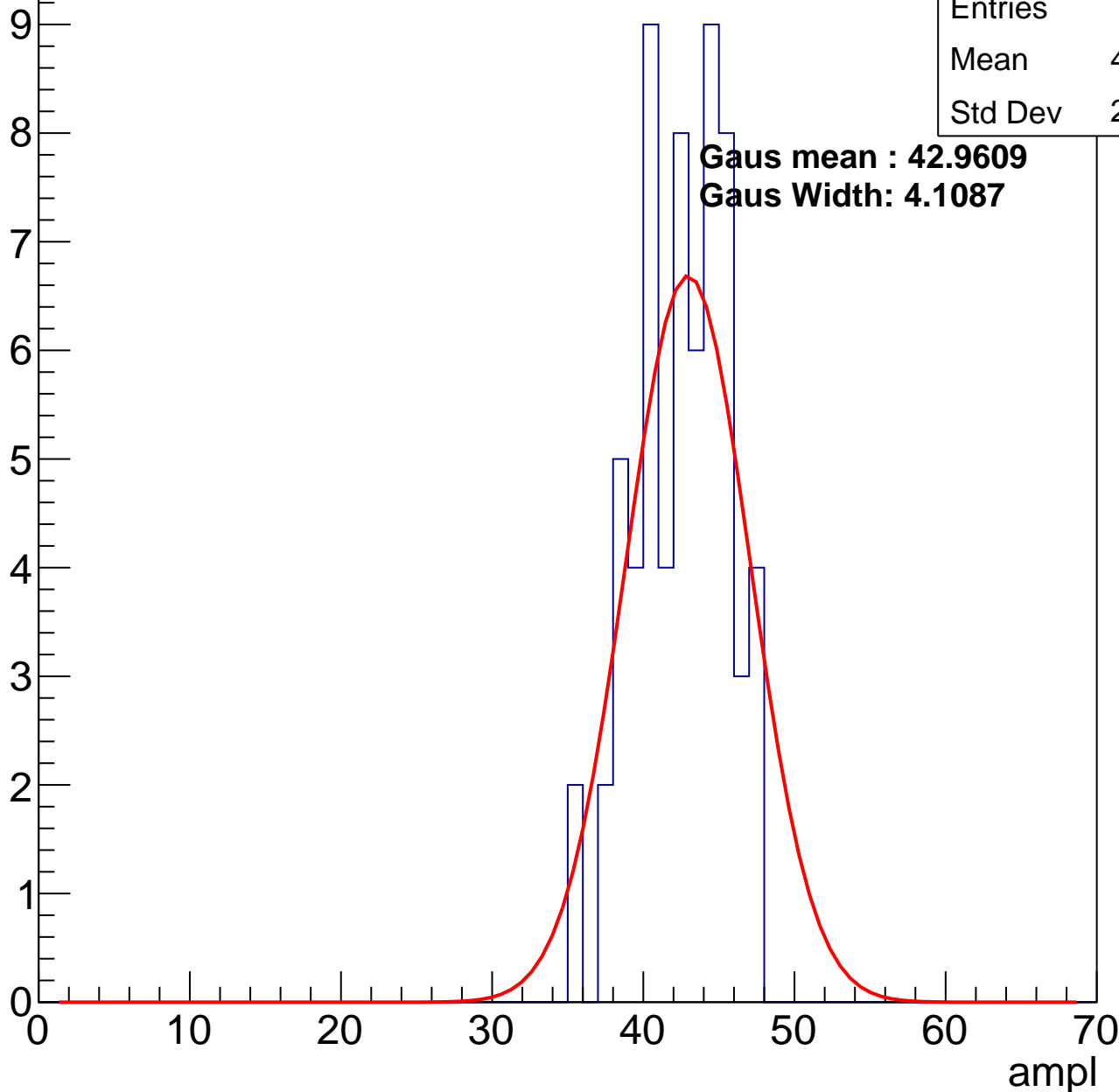
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	64
Mean	42.03
Std Dev	2.974

**Gaus mean : 42.9609**

**Gaus Width: 4.1087**



# B0L002S, U2-ch54, adc3

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entries	78
Mean	49.63
Std Dev	3.231

Entry

10

8

6

4

2

0

0

10

20

30

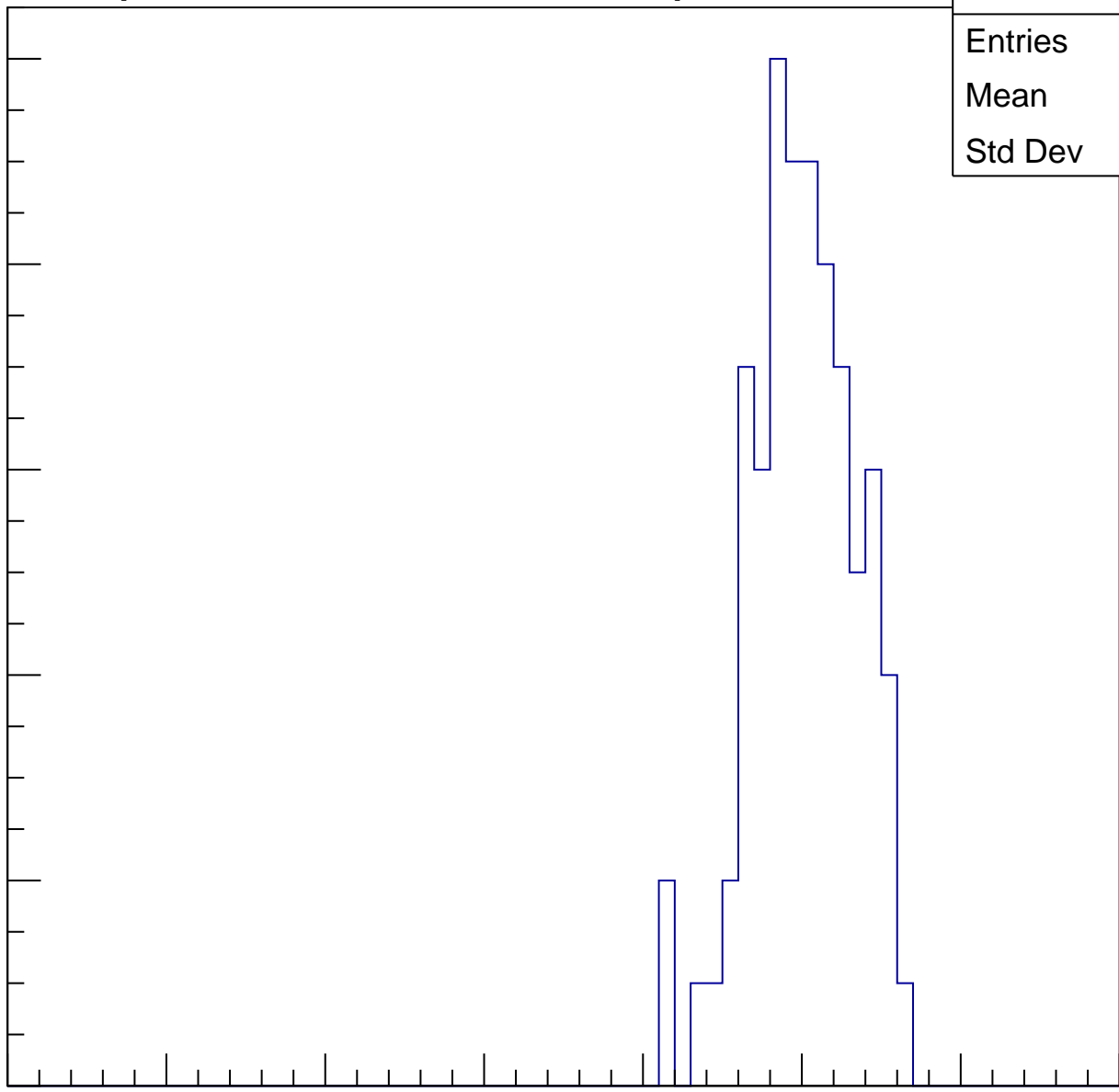
40

50

60

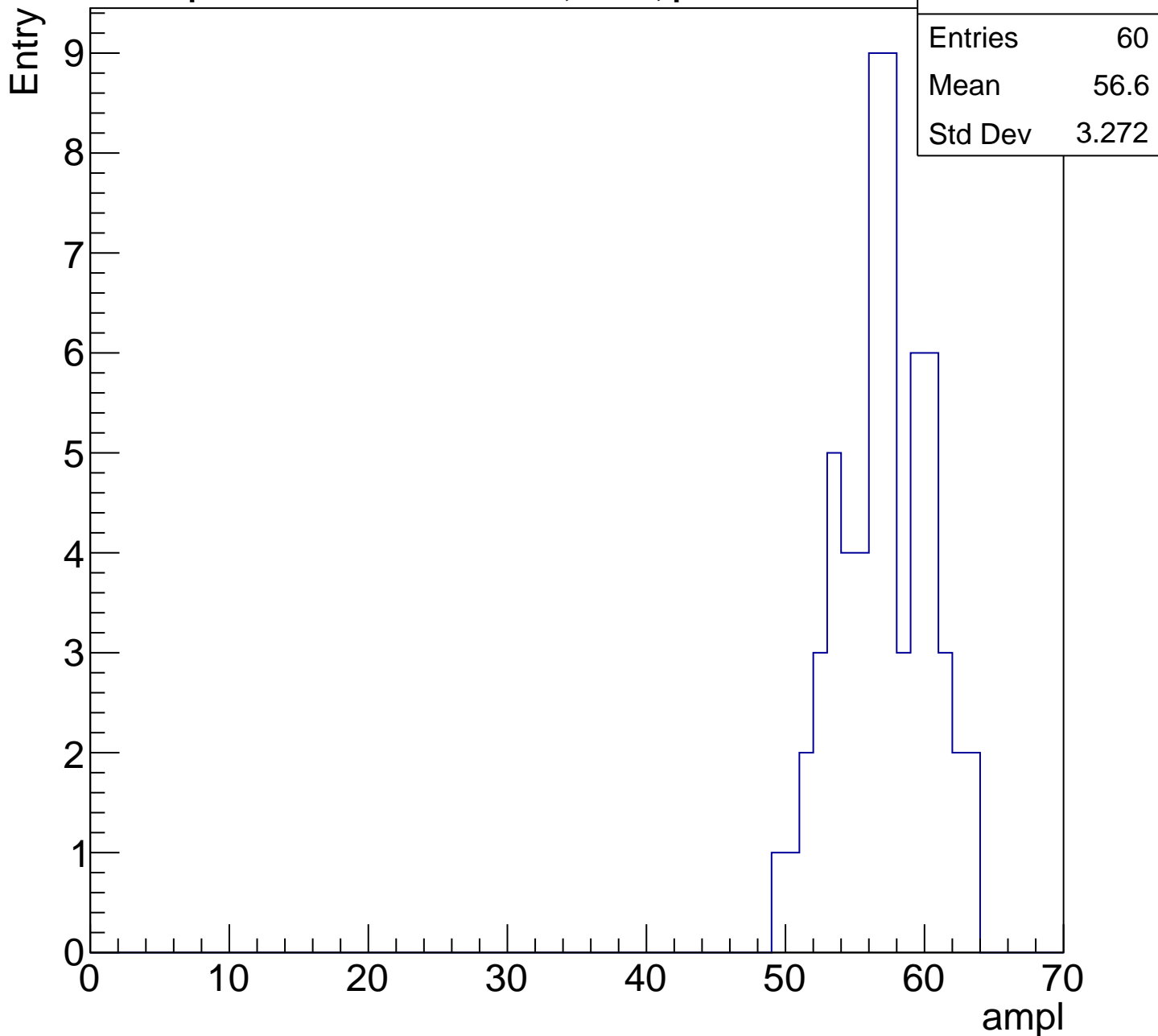
70

ampl



# B0L002S, U2-ch54, adc4

calib\_packv5\_042523\_0143.root, FC#8, port C1



# B0L002S, U2-ch54, adc5

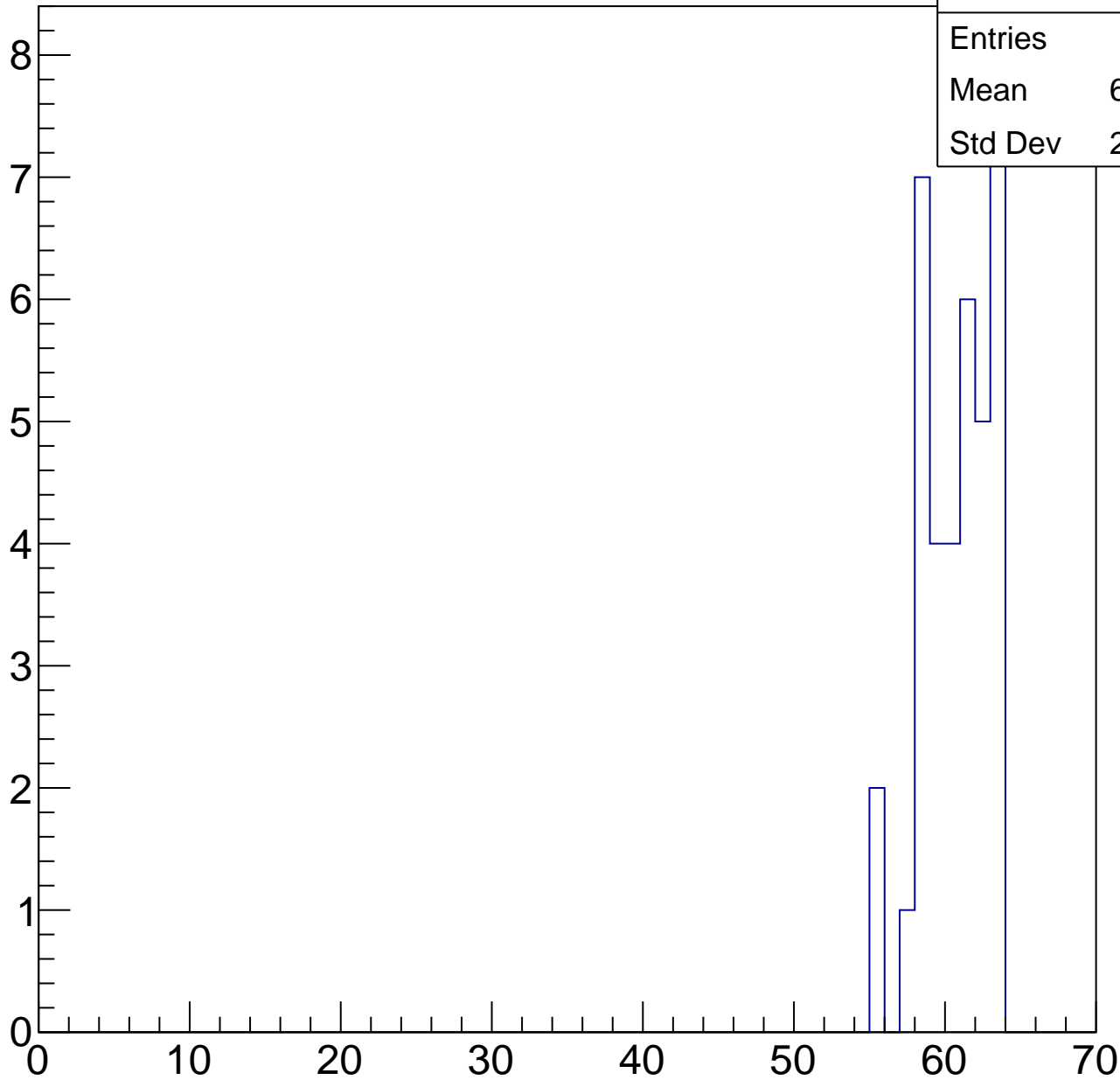
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	37
Mean	60.24
Std Dev	2.247

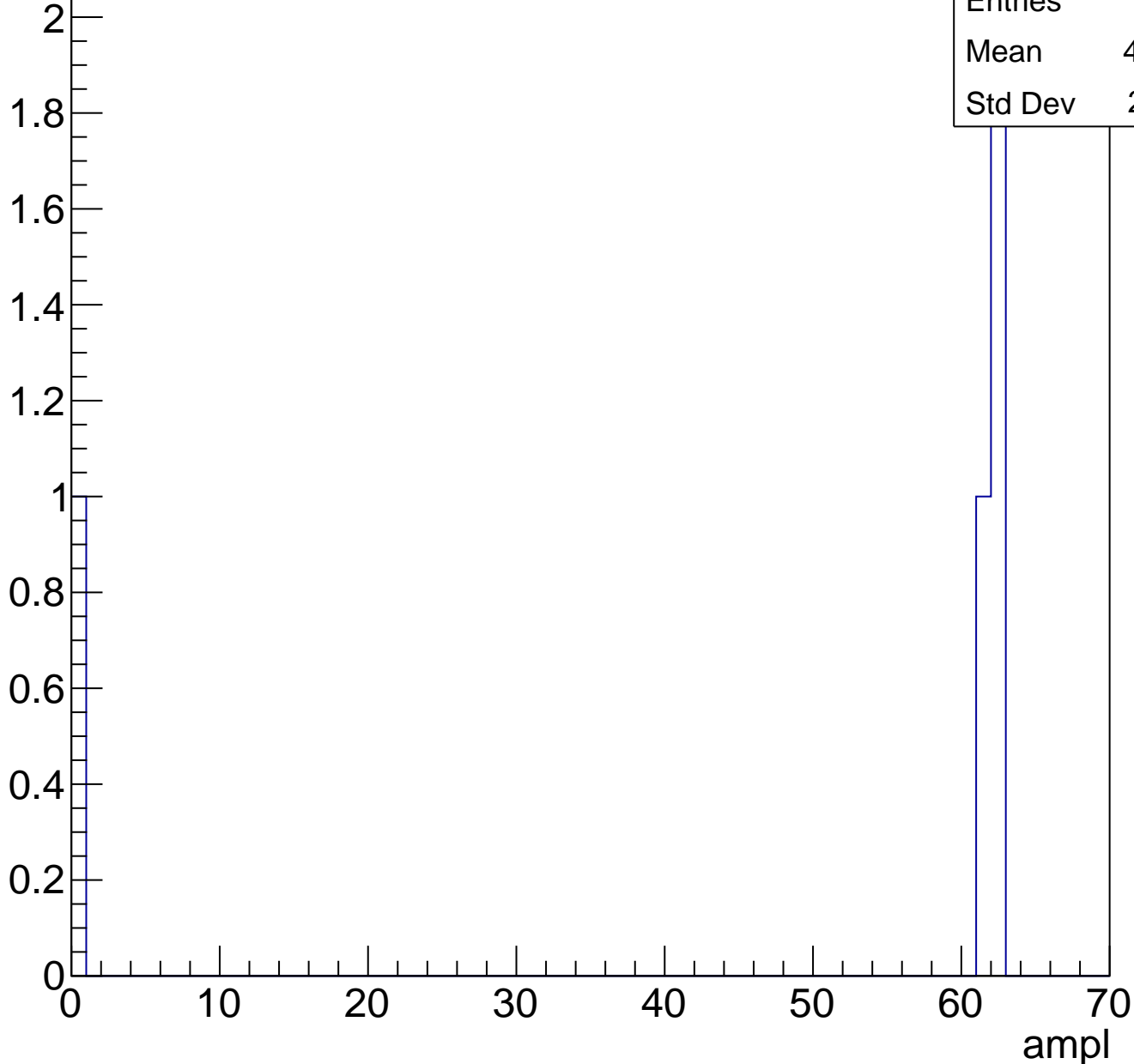
ampl



# B0L002S, U2-ch54, adc6

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry





# B0L002S, U2-ch54, adc7

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



# B0L002S, U2-ch55, adc0

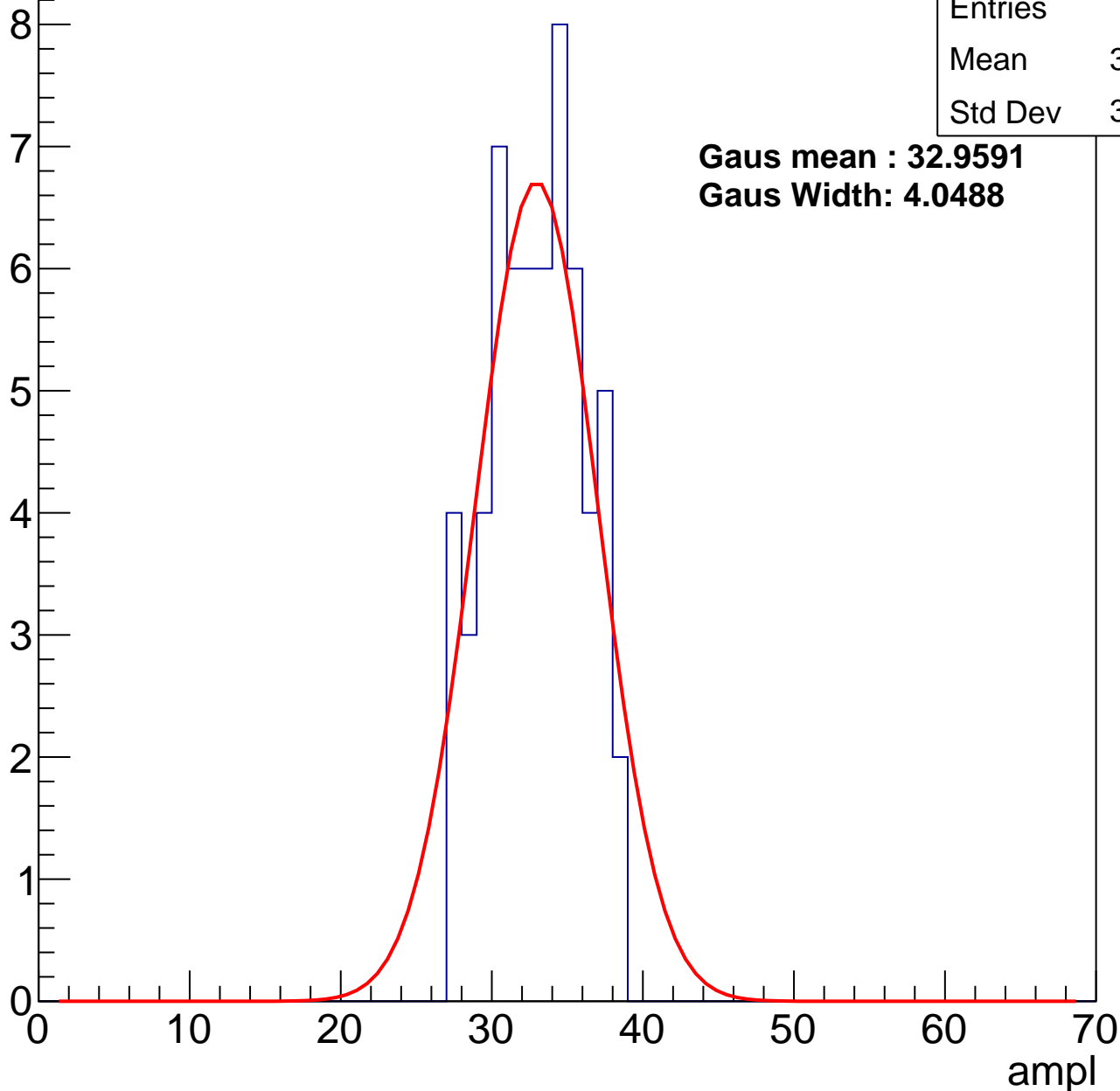
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	61
Mean	32.48
Std Dev	3.022

**Gaus mean : 32.9591**

**Gaus Width: 4.0488**



# B0L002S, U2-ch55, adc1

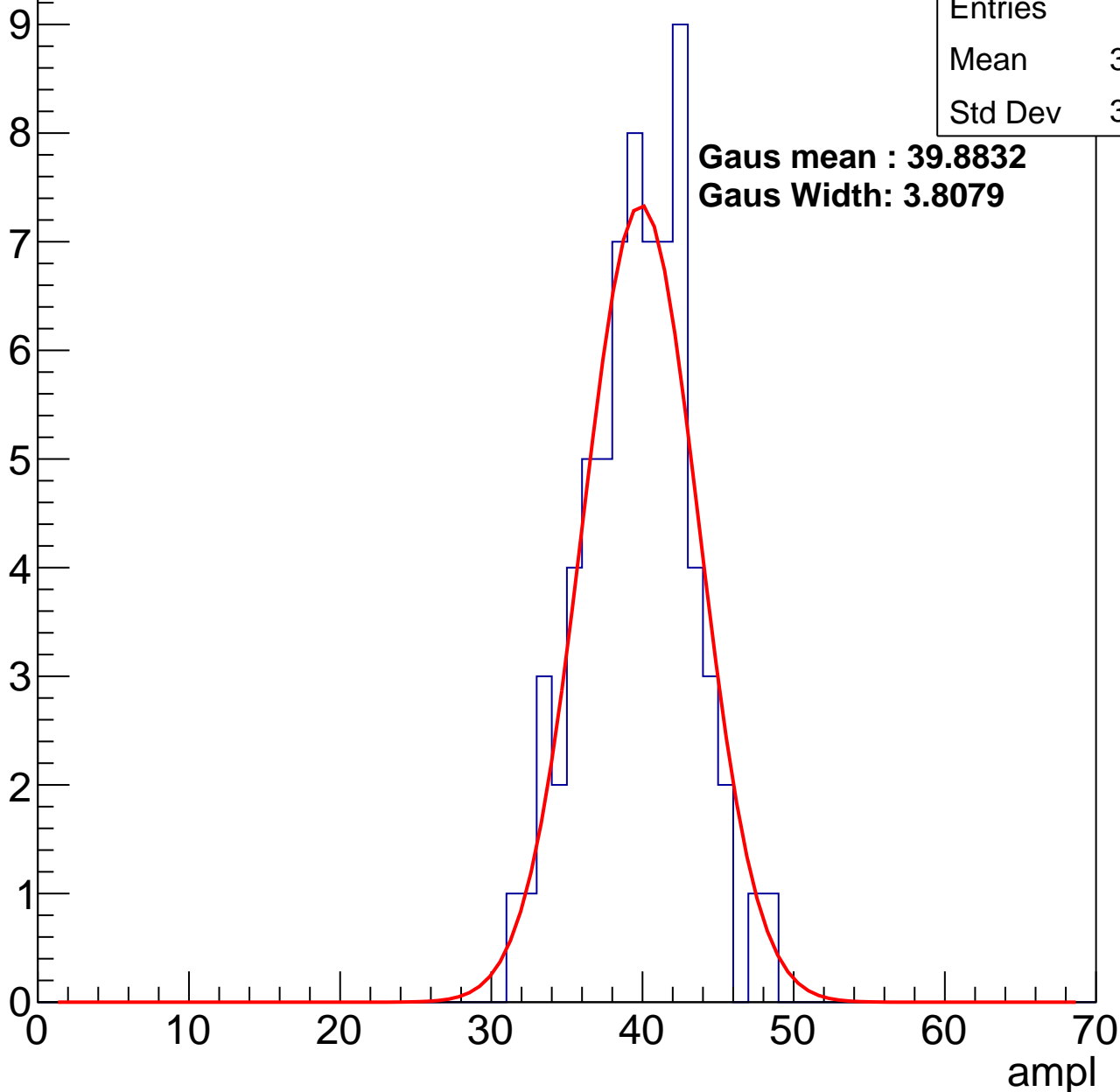
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	70
Mean	39.24
Std Dev	3.535

**Gaus mean : 39.8832**

**Gaus Width: 3.8079**

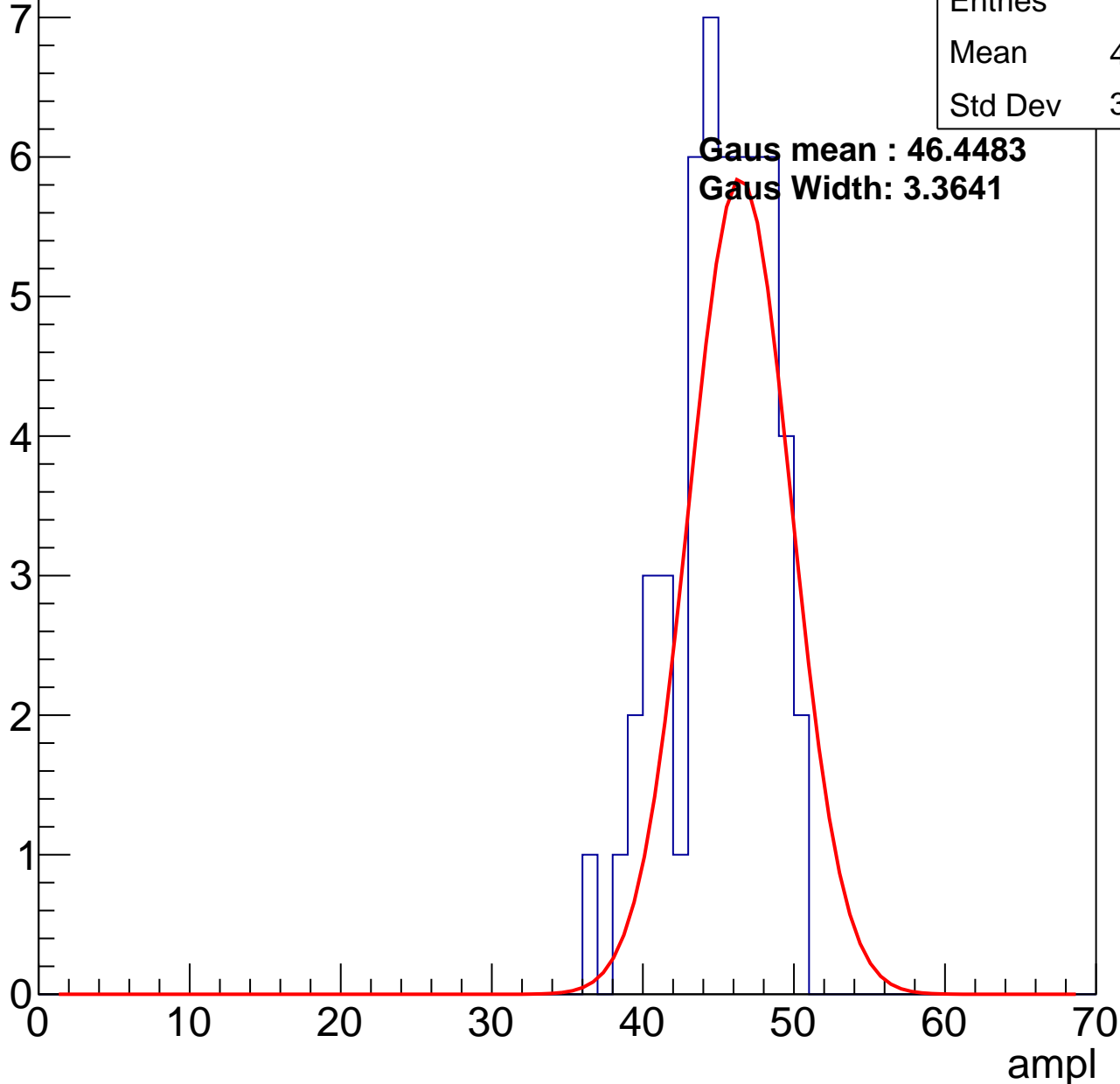


# B0L002S, U2-ch55, adc2

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

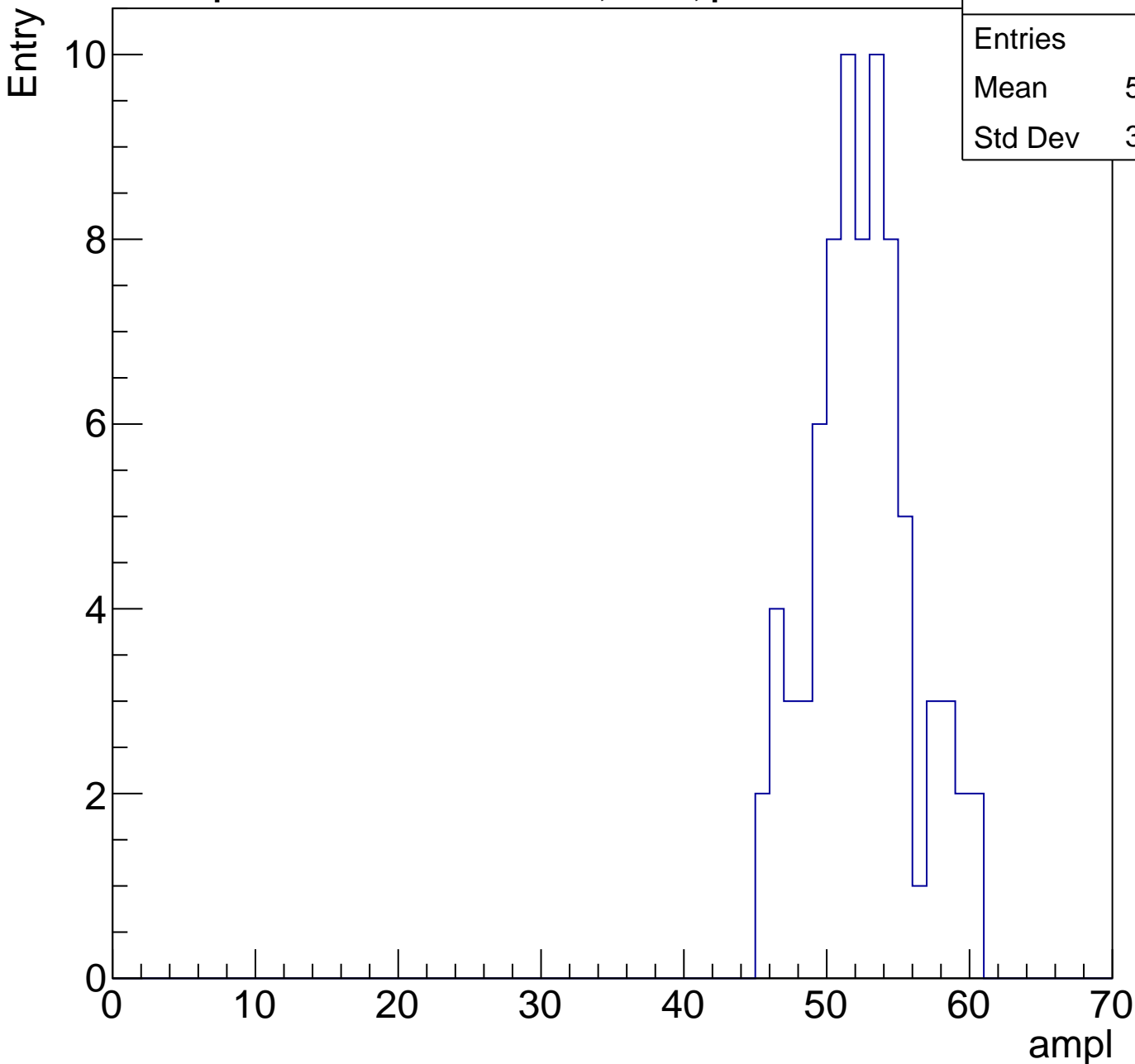
Entries	54
Mean	44.72
Std Dev	3.217



# B0L002S, U2-ch55, adc3

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entries	78
Mean	51.99
Std Dev	3.532

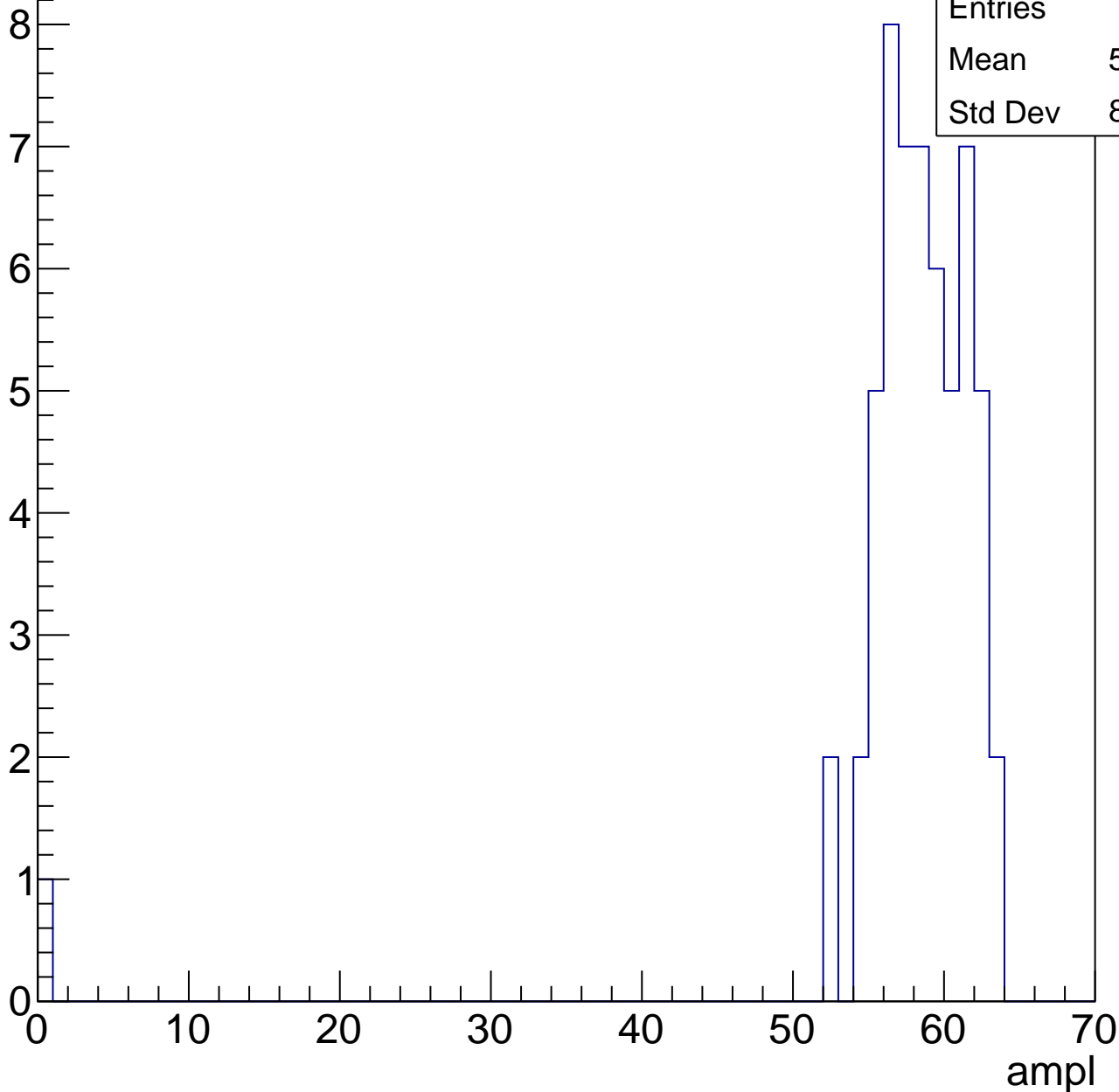


# B0L002S, U2-ch55, adc4

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	57
Mean	57.14
Std Dev	8.088

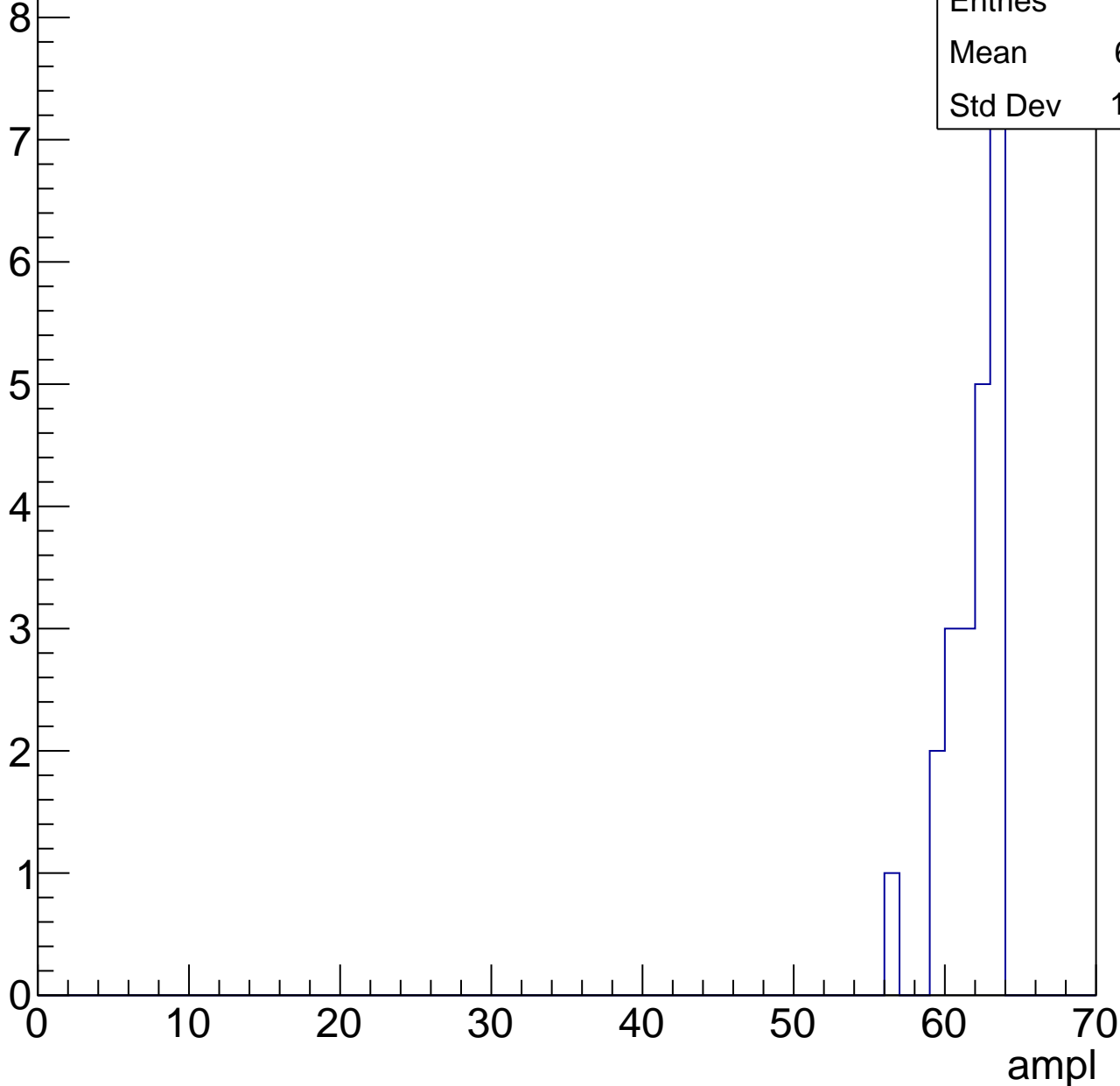


# B0L002S, U2-ch55, adc5

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	22
Mean	61.41
Std Dev	1.775



# B0L002S, U2-ch55, adc6

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



Entries	0
Mean	0
Std Dev	0



# B0L002S, U2-ch55, adc7

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

1  
0.8  
0.6  
0.4  
0.2  
0

Entries	1
Mean	26
Std Dev	0

ampl

# B0L002S, U2-ch56, adc0

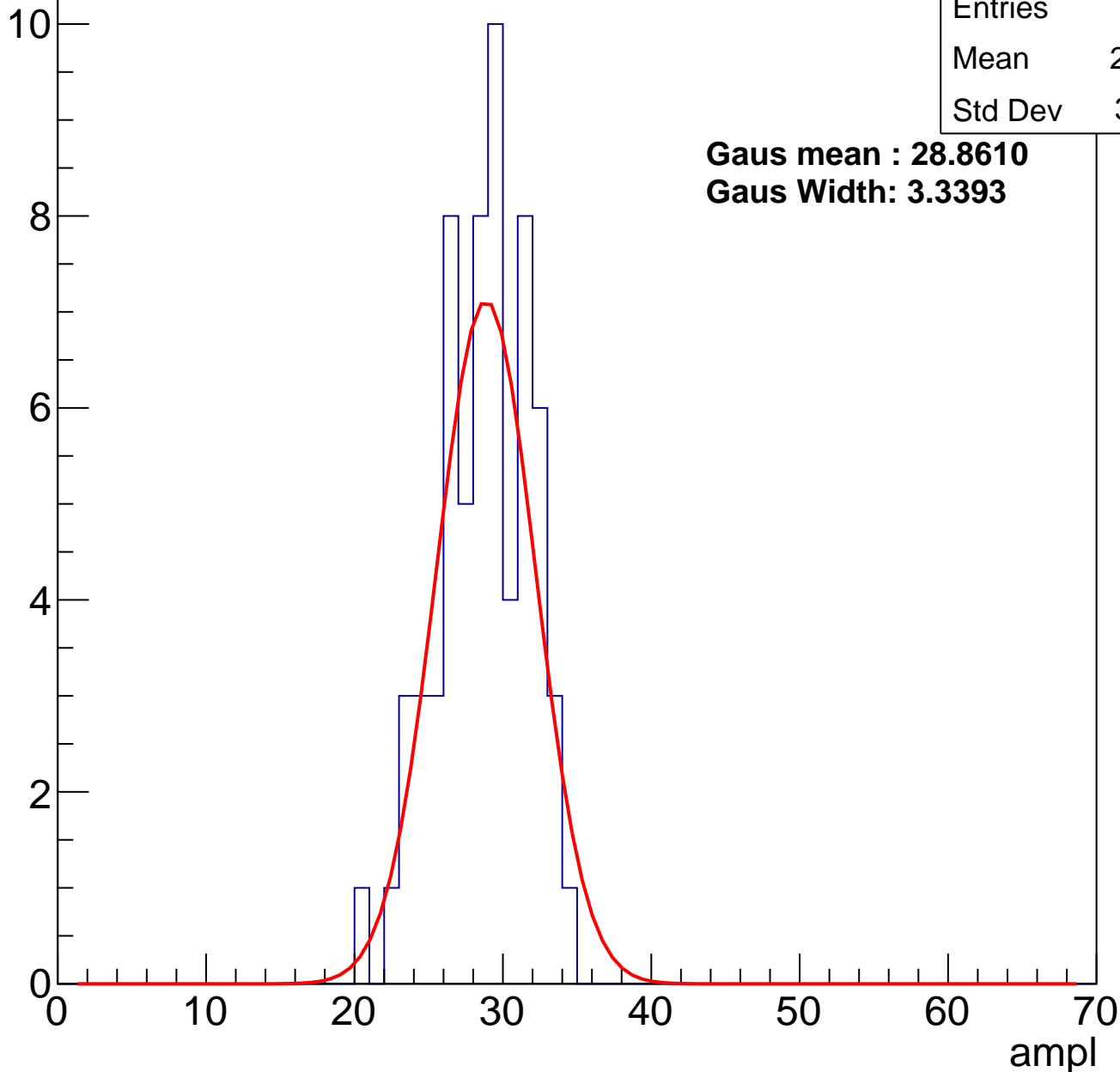
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entries	64
Mean	28.25
Std Dev	3.031

**Gaus mean : 28.8610**

**Gaus Width: 3.3393**

Entry



# B0L002S, U2-ch56, adc1

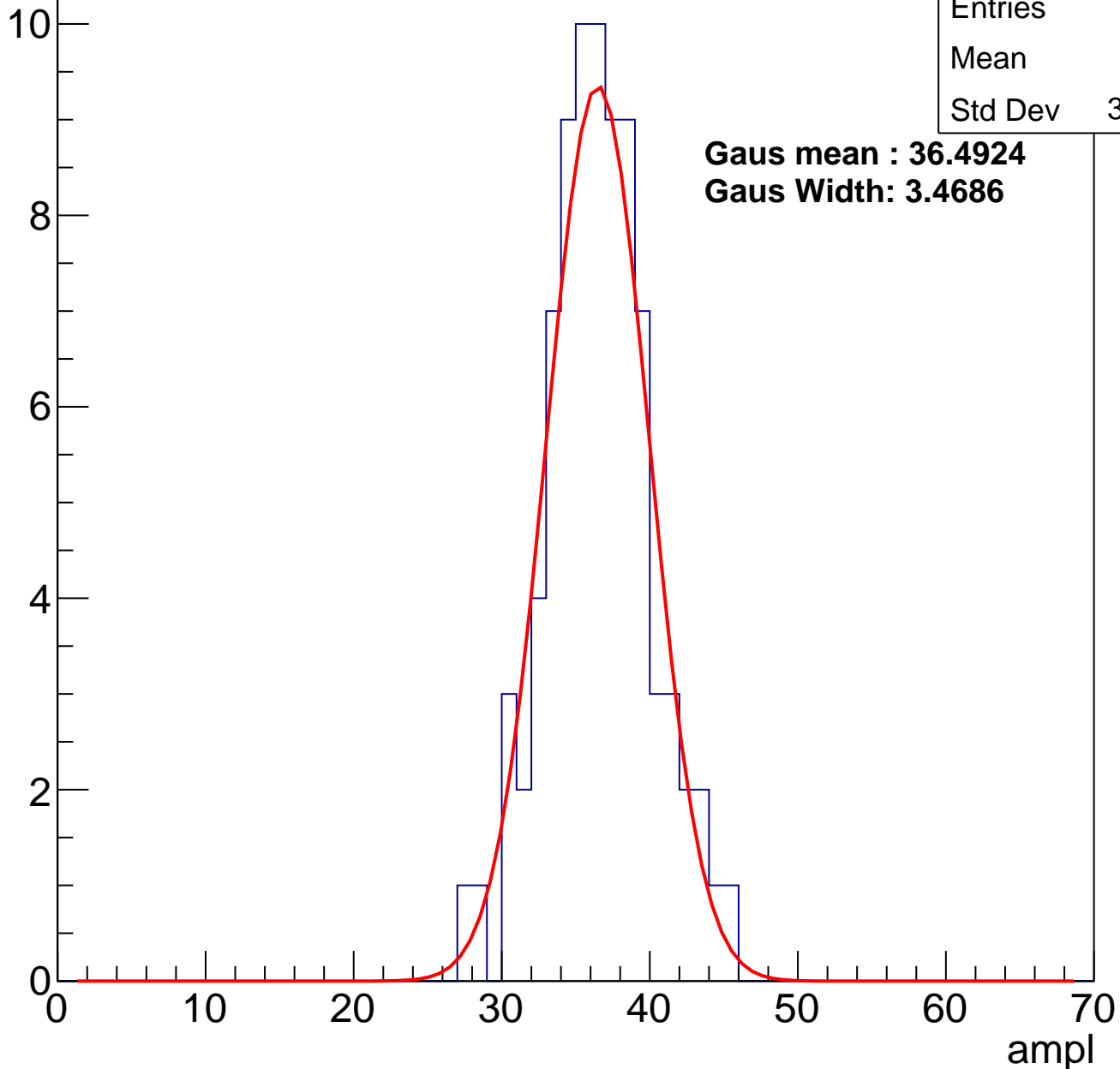
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entries	84
Mean	36.1
Std Dev	3.487

**Gaus mean : 36.4924**

**Gaus Width: 3.4686**

Entry



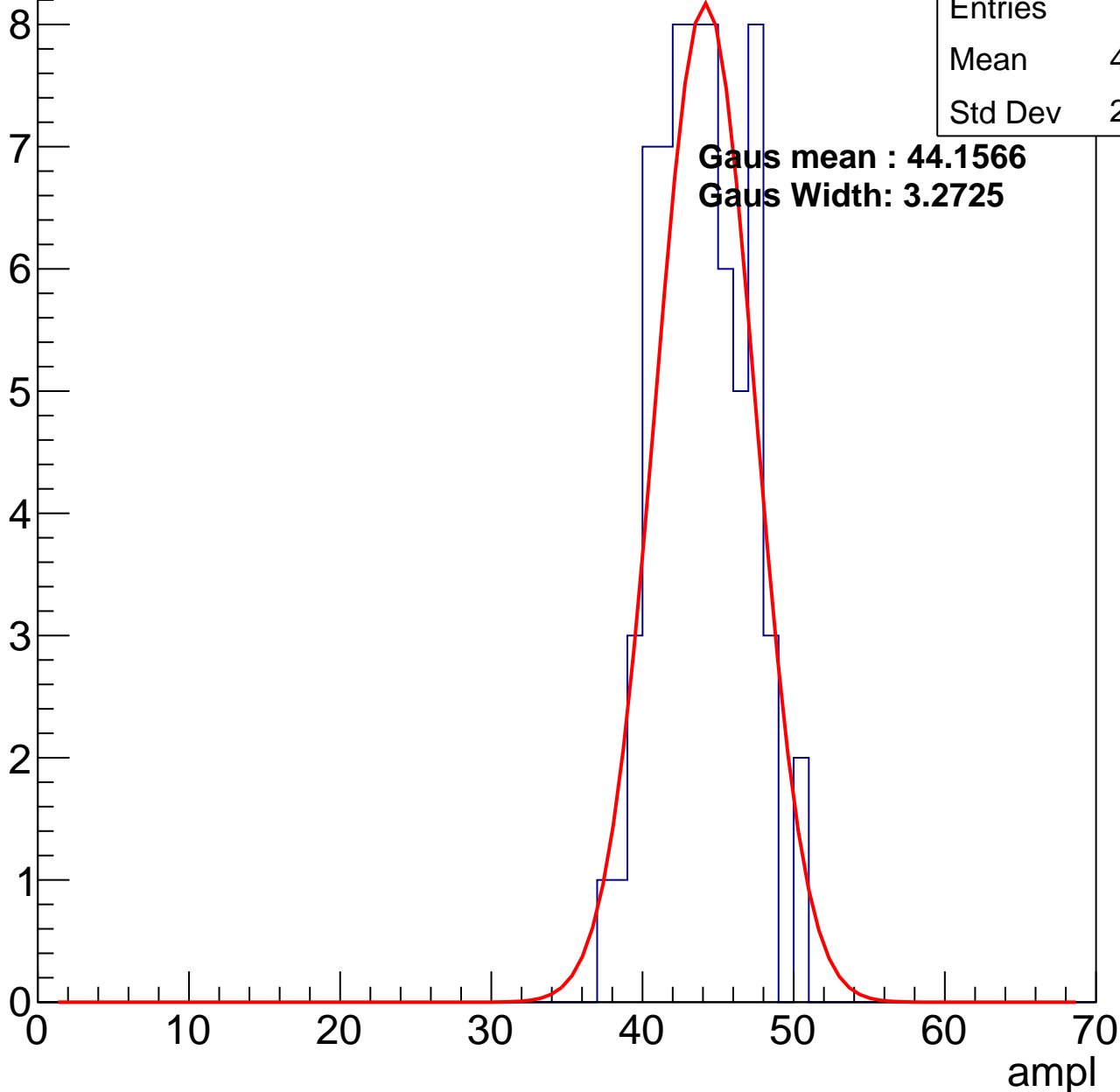
# B0L002S, U2-ch56, adc2

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	67
Mean	43.45
Std Dev	2.923

**Gaus mean : 44.1566**  
**Gaus Width: 3.2725**

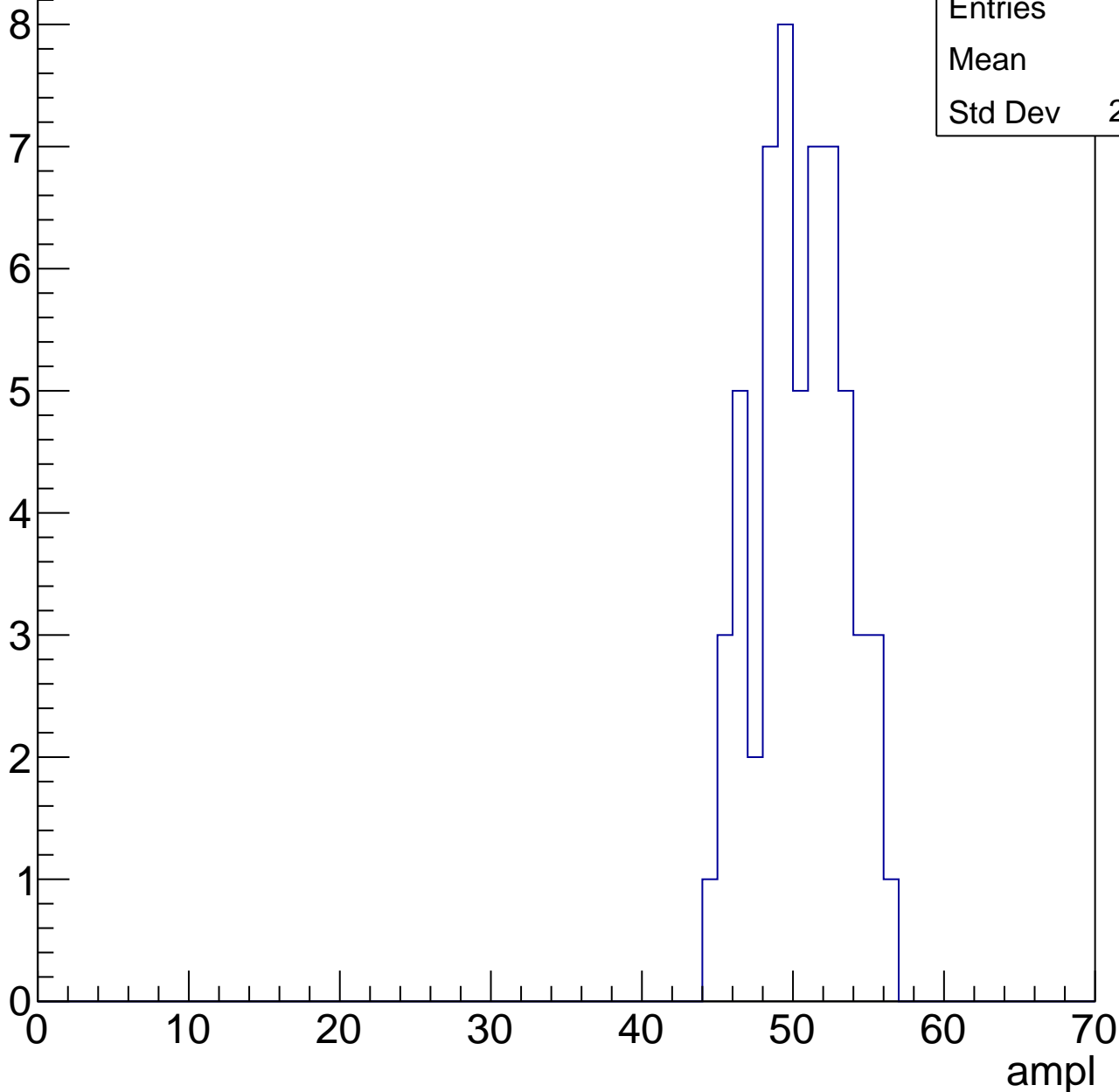


# B0L002S, U2-ch56, adc3

calib\_packv5\_042523\_0143.root, FC#8, port C1

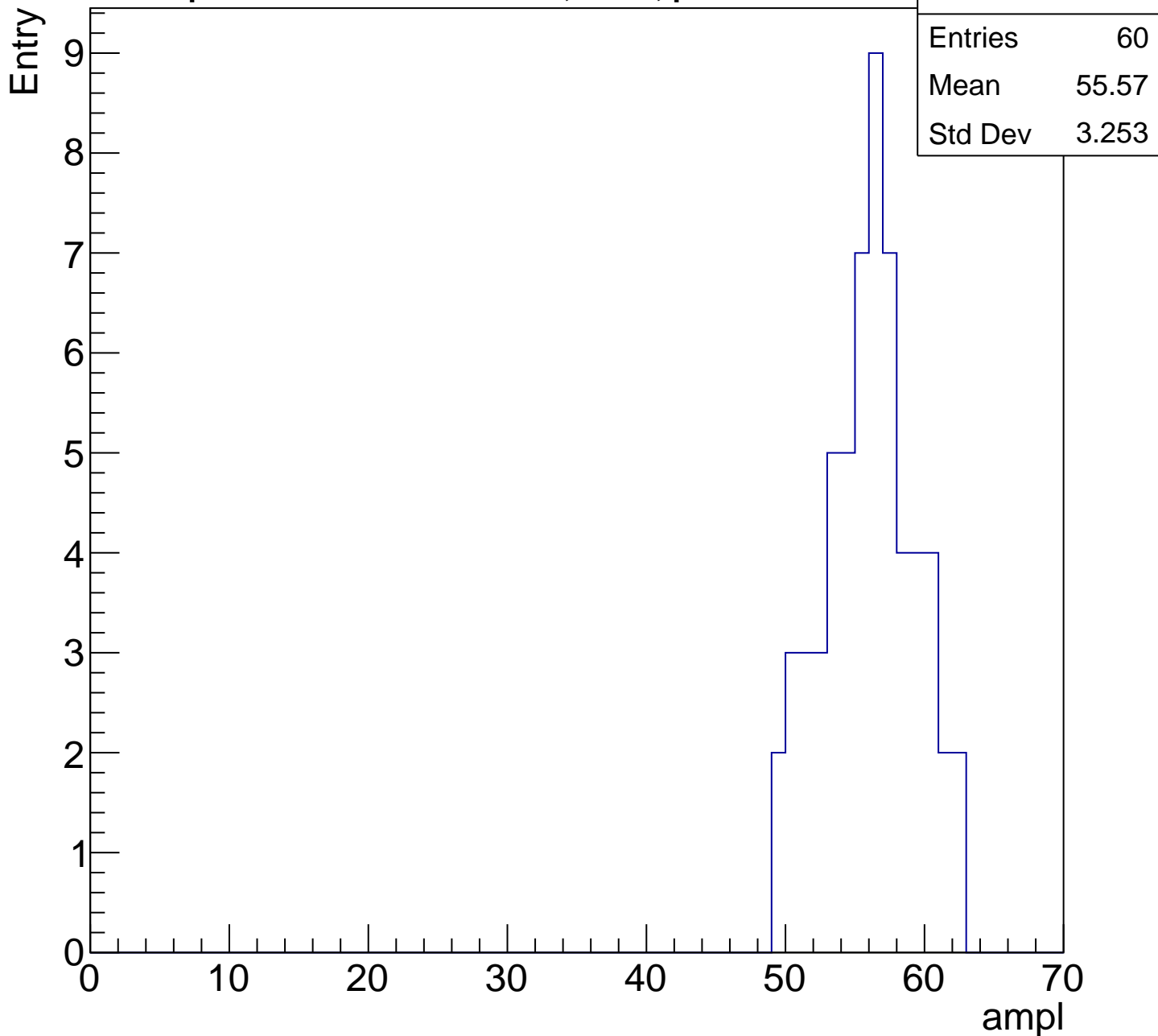
Entry

Entries	57
Mean	50
Std Dev	2.914



# B0L002S, U2-ch56, adc4

calib\_packv5\_042523\_0143.root, FC#8, port C1

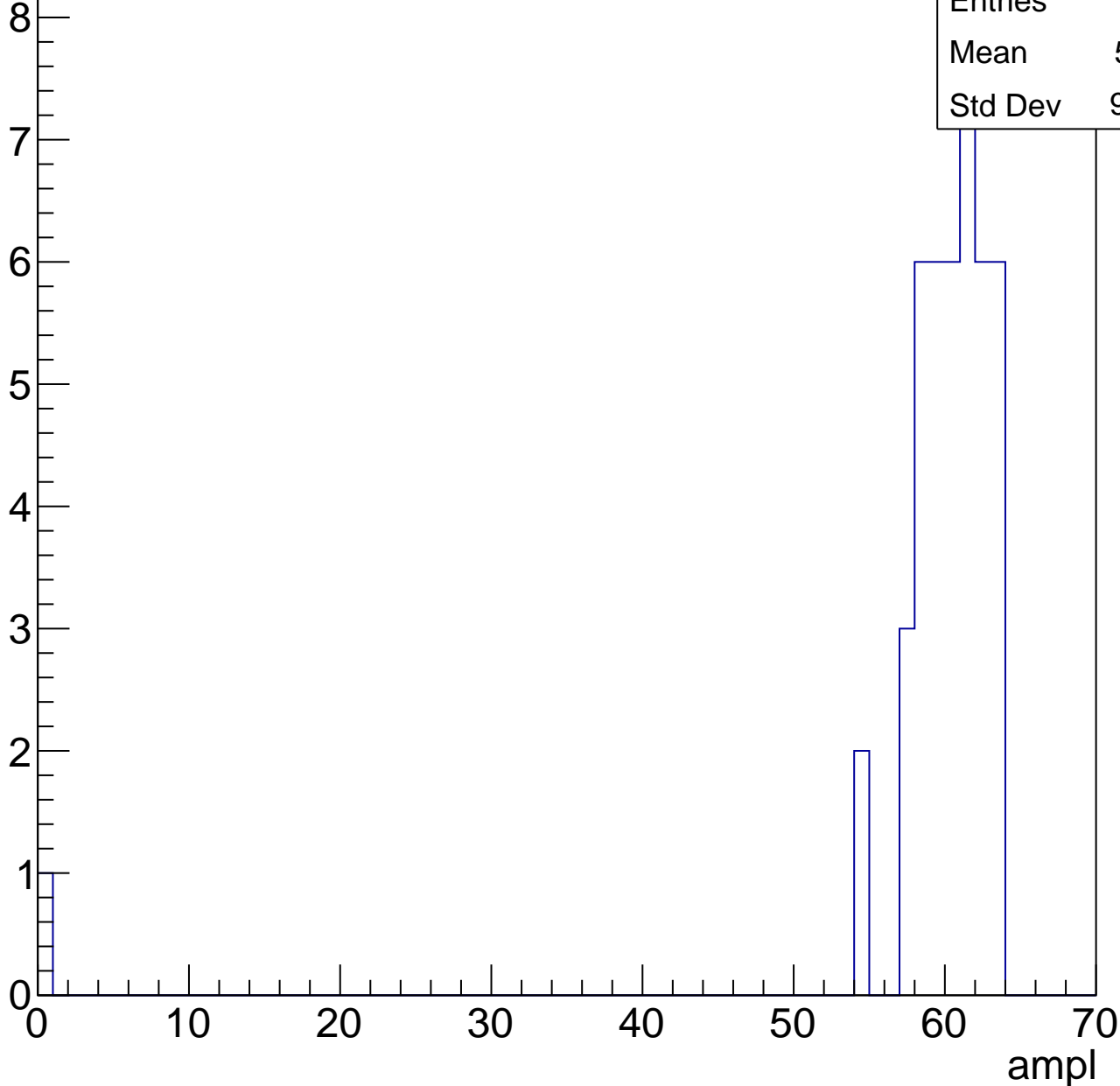


# B0L002S, U2-ch56, adc5

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

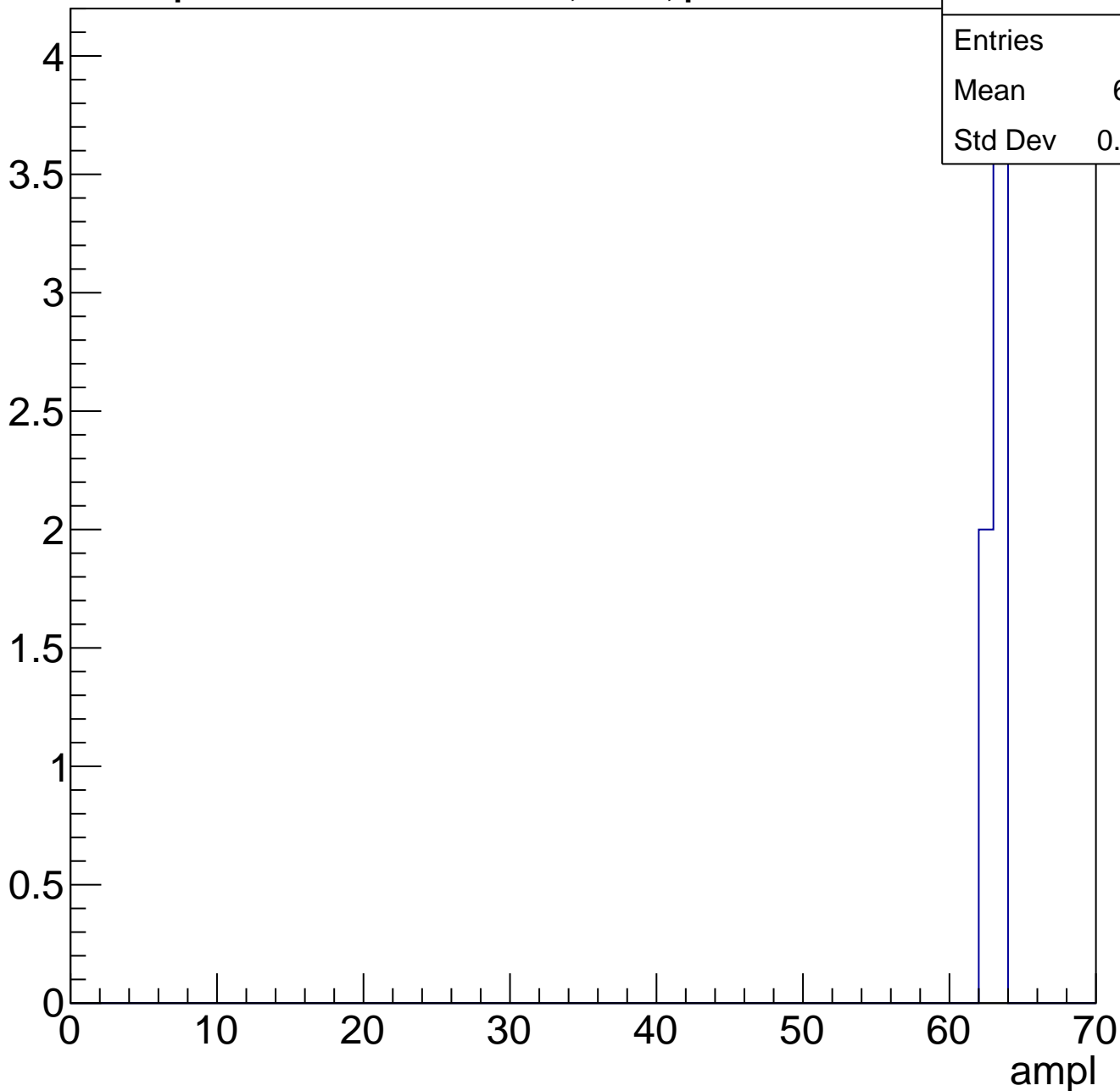
Entries	44
Mean	58.61
Std Dev	9.208



# B0L002S, U2-ch56, adc6

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry





# B0L002S, U2-ch56, adc7

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



# B0L002S, U2-ch57, adc0

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entries	90
Mean	30.04
Std Dev	5.787

**Gaus mean : 31.7471**

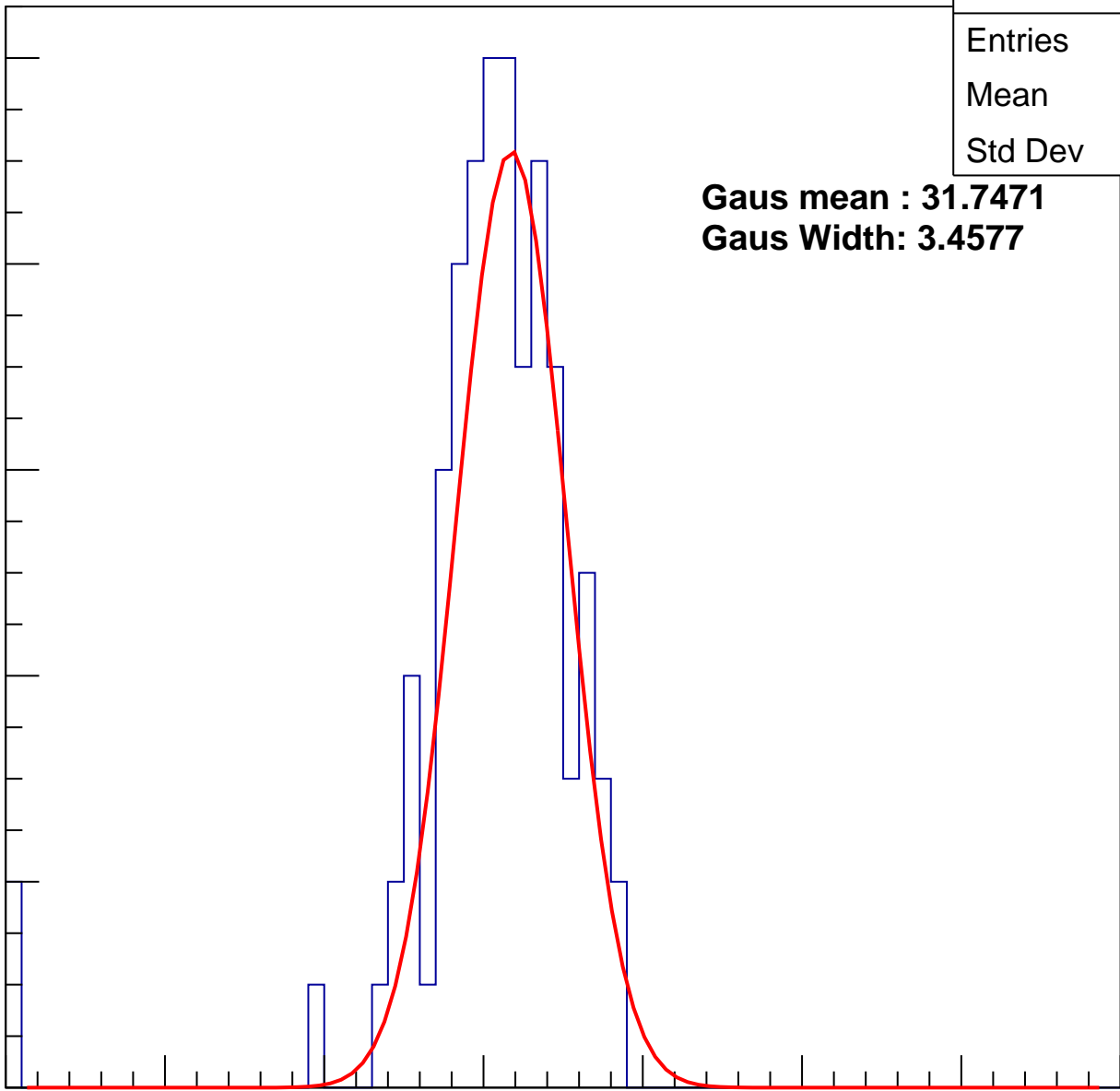
**Gaus Width: 3.4577**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L002S, U2-ch57, adc1

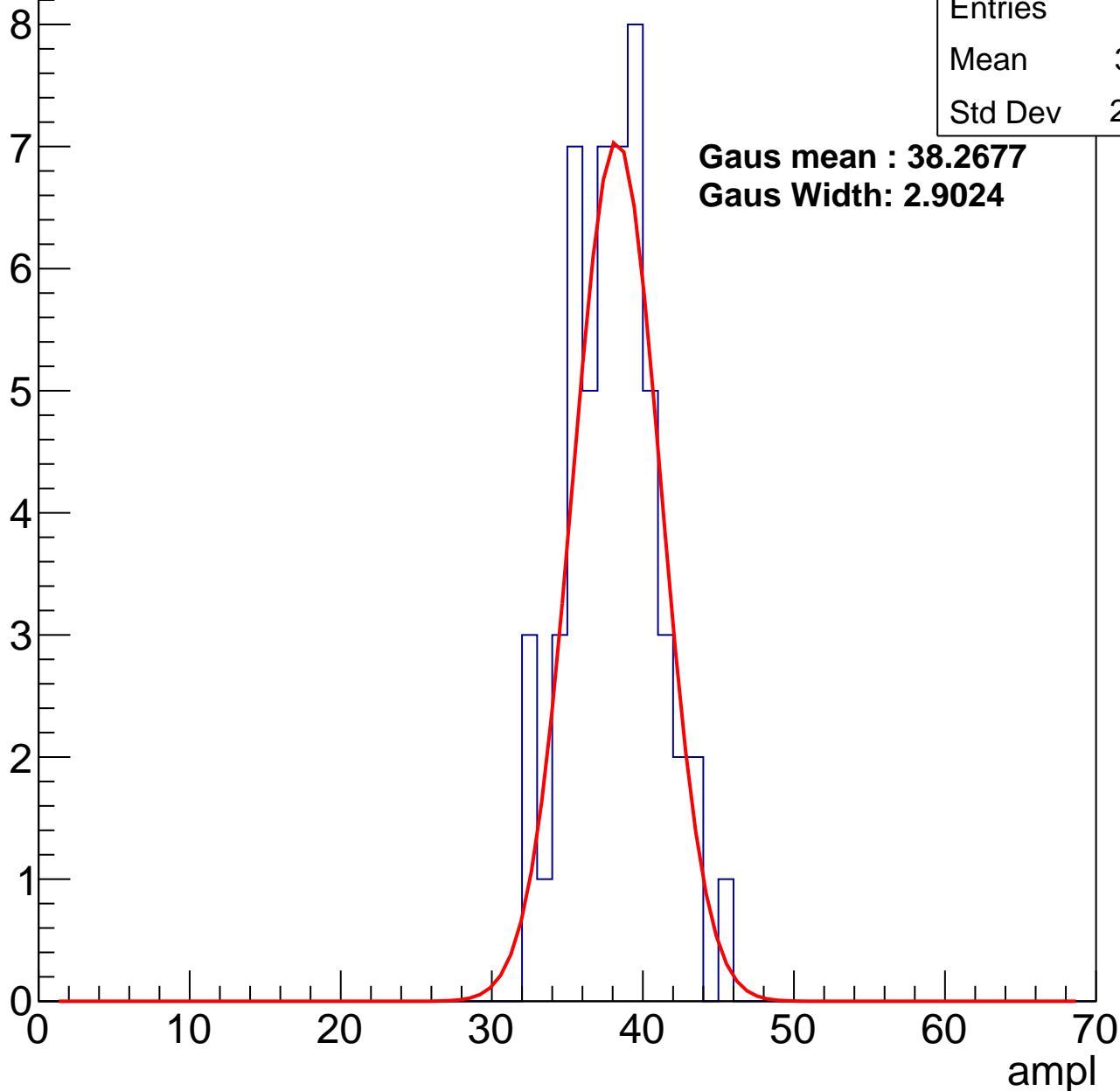
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	54
Mean	37.61
Std Dev	2.883

**Gaus mean : 38.2677**

**Gaus Width: 2.9024**



# B0L002S, U2-ch57, adc2

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entries	62
Mean	43.77
Std Dev	2.732

**Gaus mean : 44.4057**

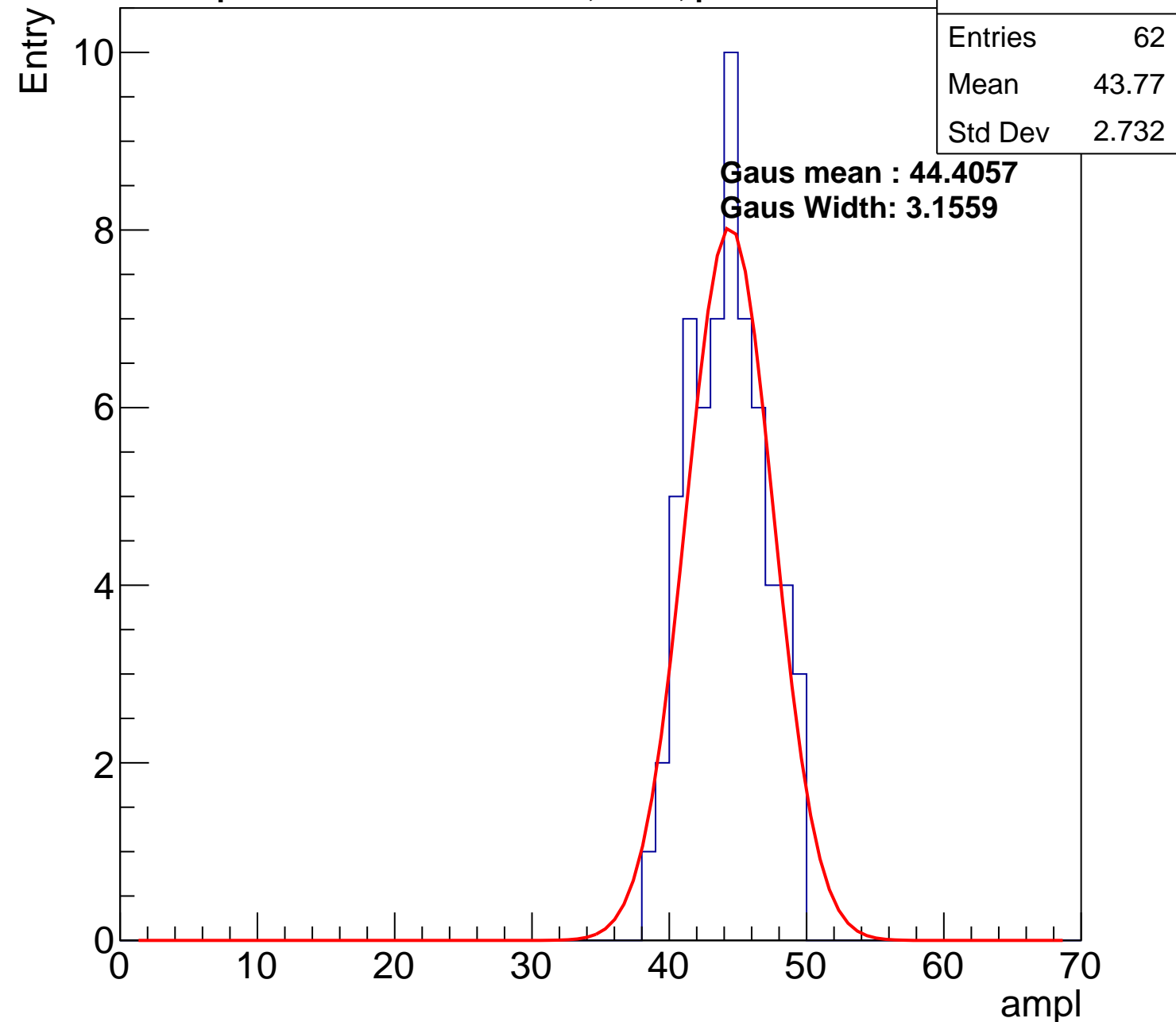
**Gaus Width: 3.1559**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

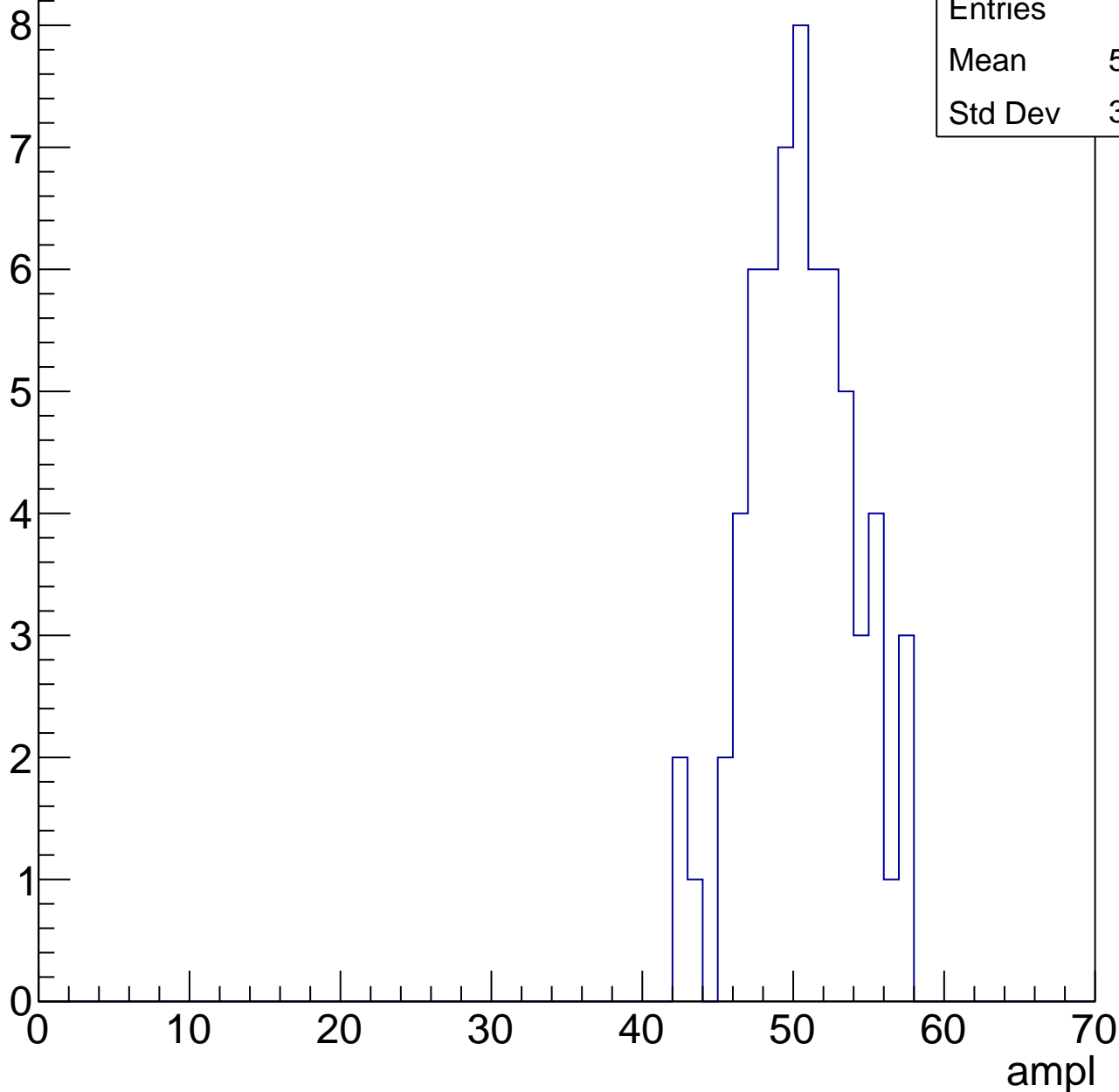


# B0L002S, U2-ch57, adc3

calib\_packv5\_042523\_0143.root, FC#8, port C1

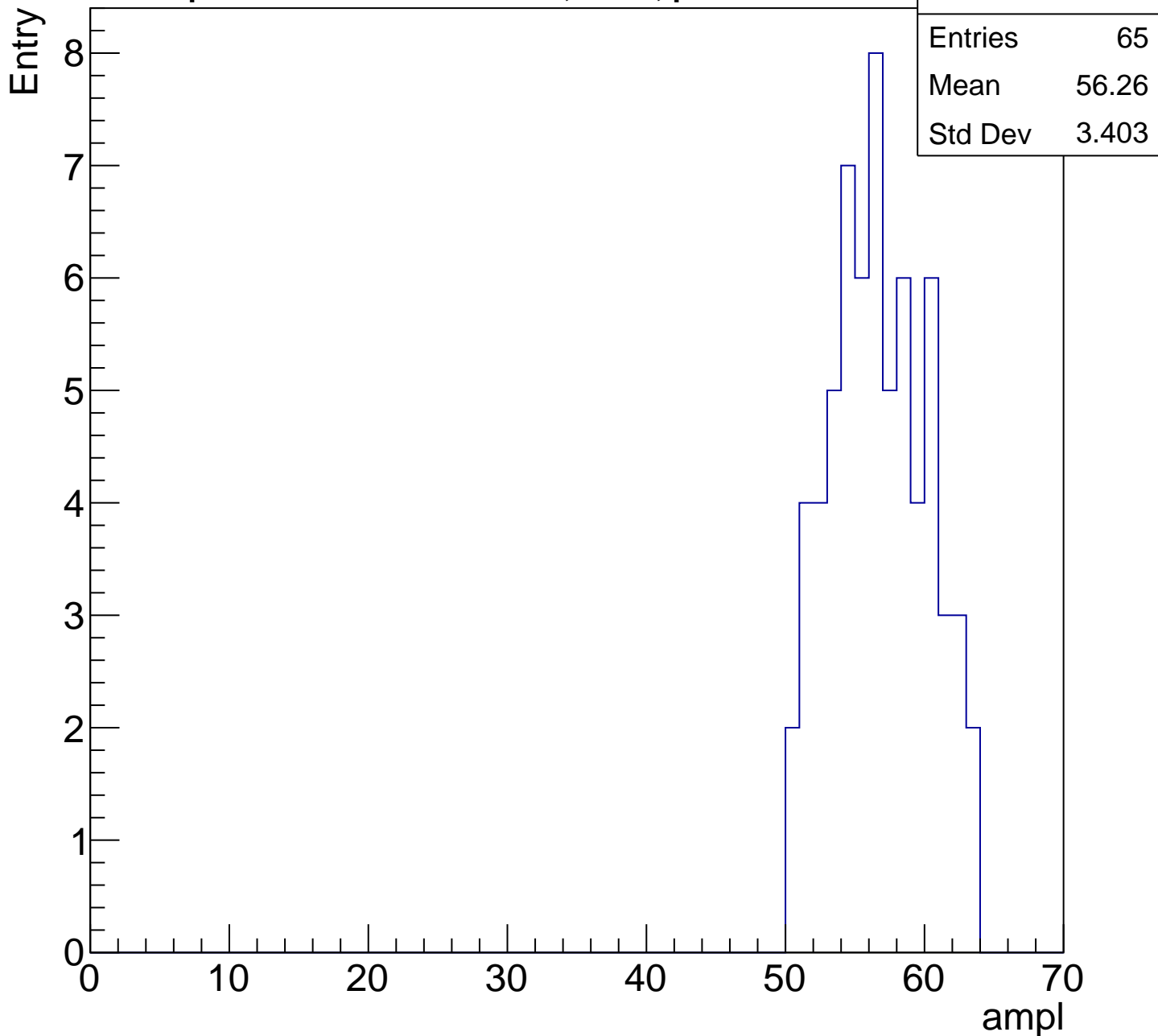
Entry

Entries	64
Mean	50.09
Std Dev	3.494



# B0L002S, U2-ch57, adc4

calib\_packv5\_042523\_0143.root, FC#8, port C1

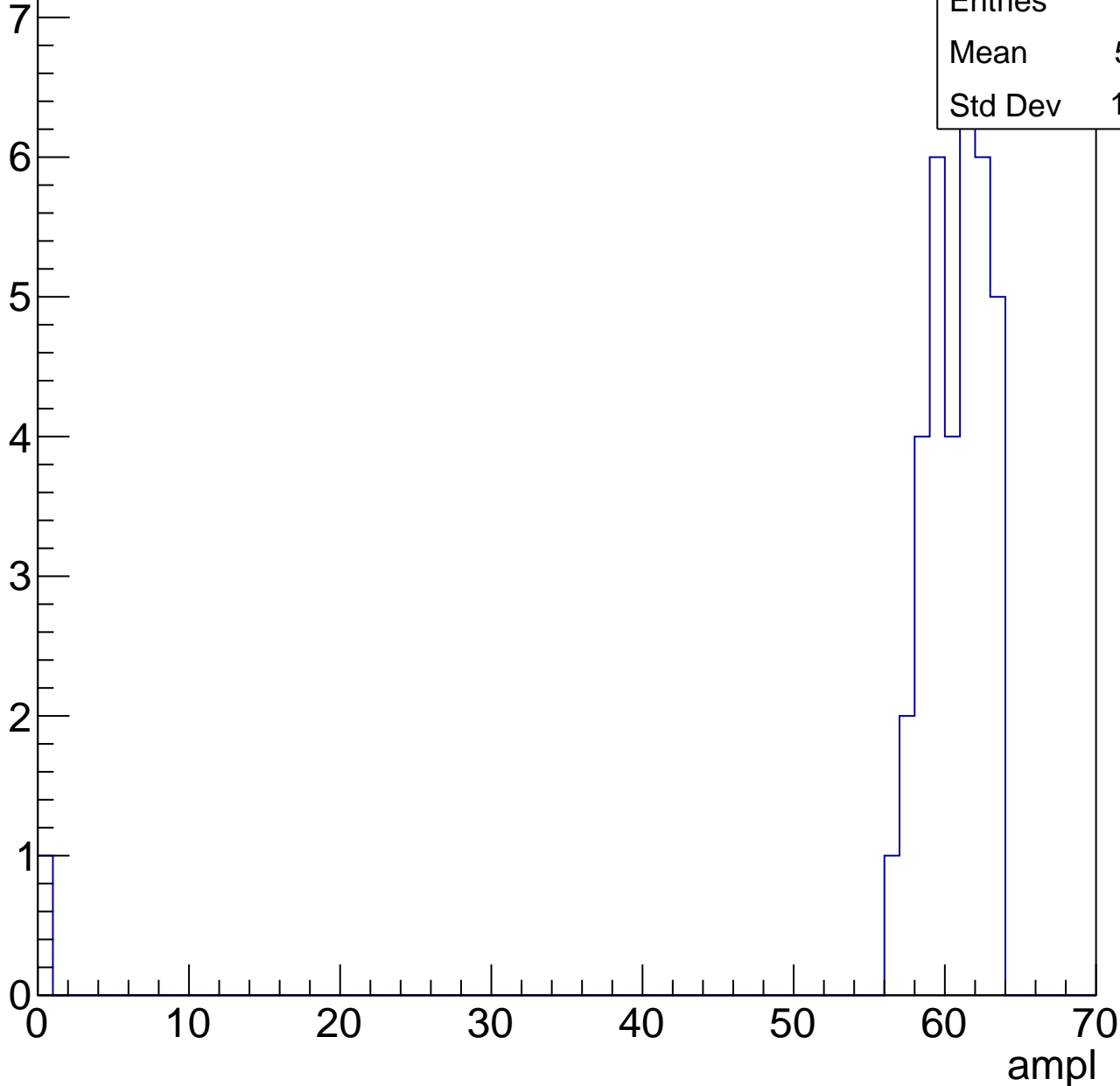


# B0L002S, U2-ch57, adc5

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	36
Mean	58.61
Std Dev	10.09



# B0L002S, U2-ch57, adc6

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry





# B0L002S, U2-ch57, adc7

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



# B0L002S, U2-ch58, adc0

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entries	82
Mean	30.54
Std Dev	3.178

**Gaus mean : 31.2403**

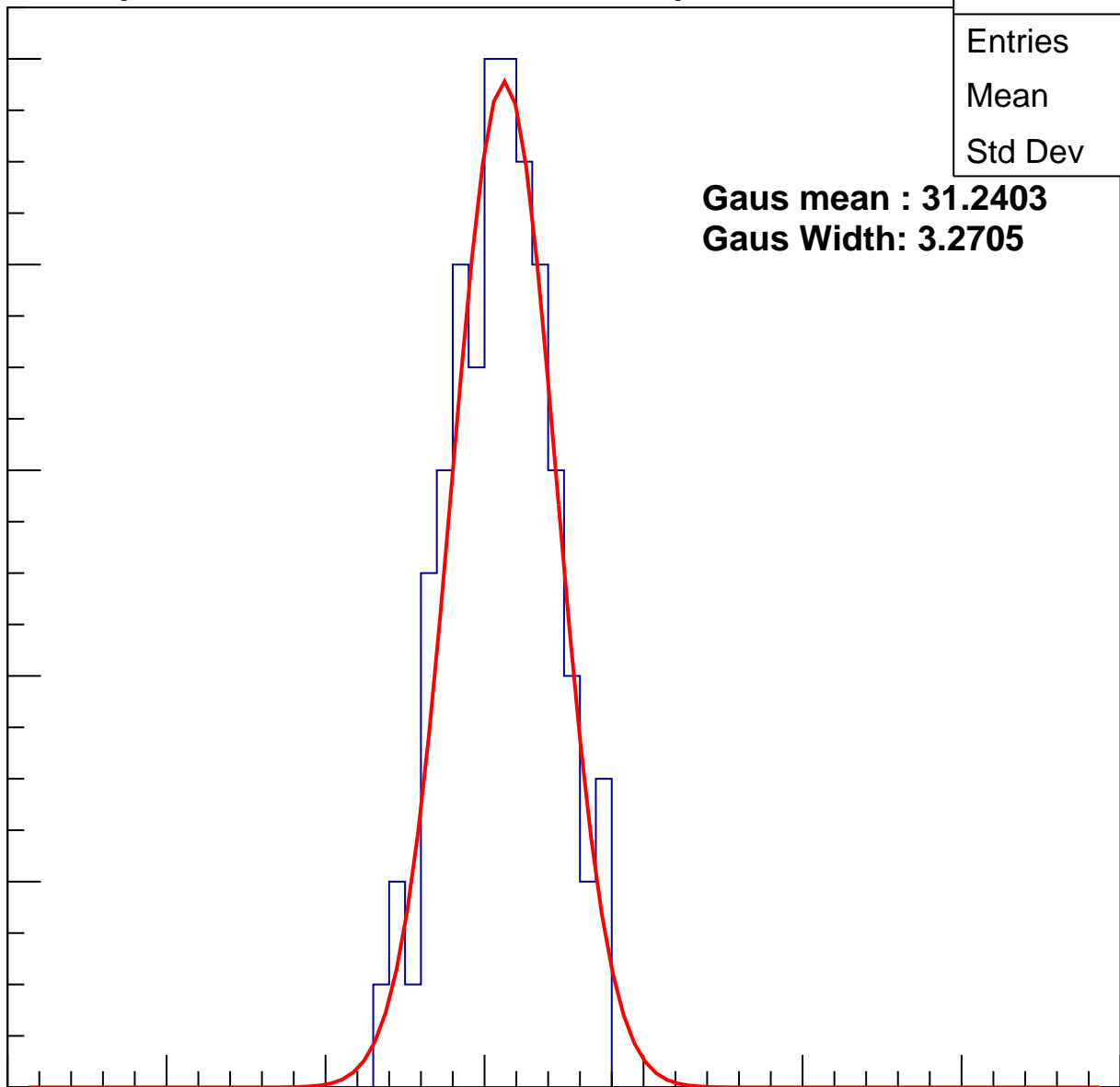
**Gaus Width: 3.2705**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L002S, U2-ch58, adc1

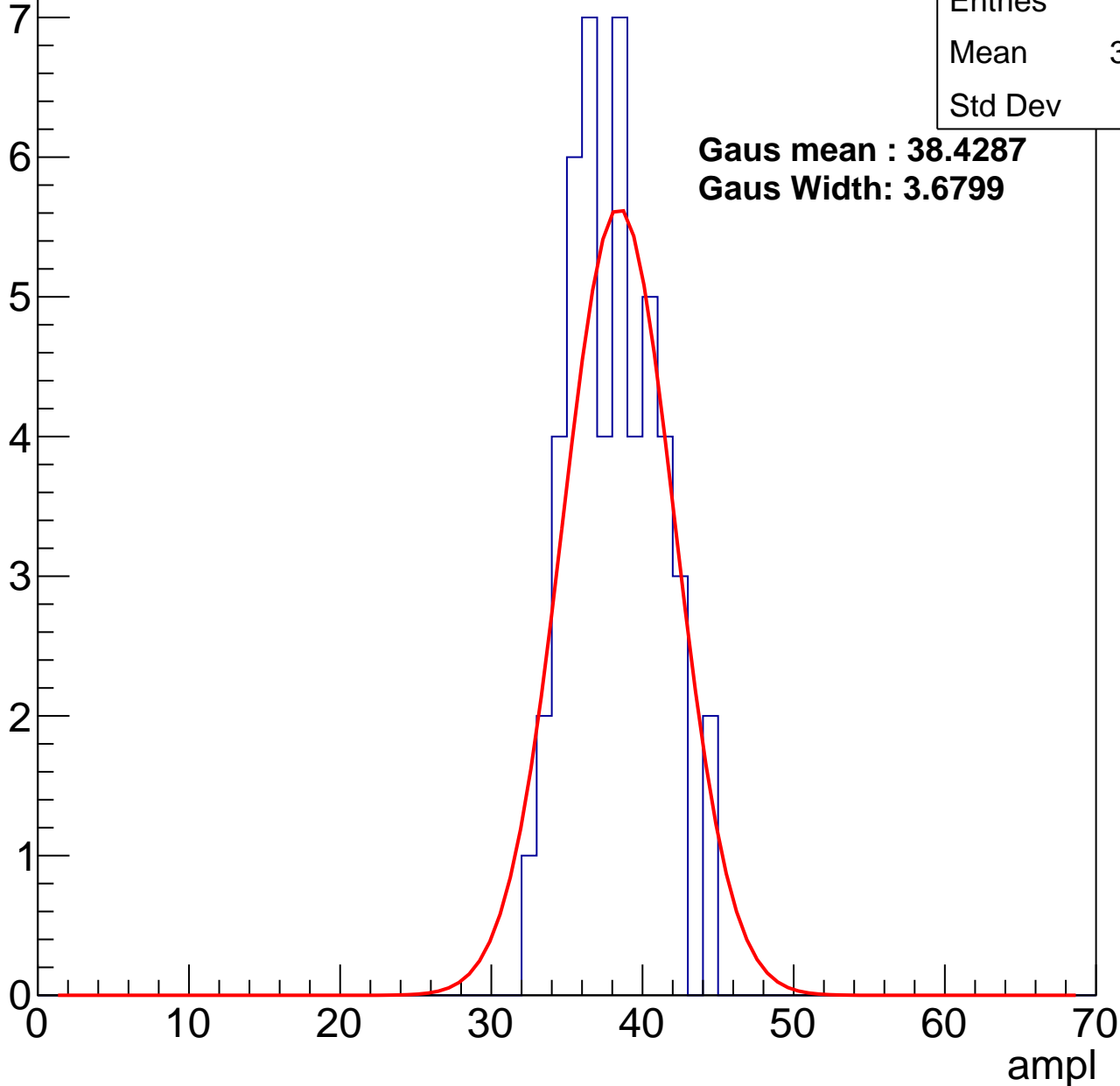
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	49
Mean	37.63
Std Dev	2.89

**Gaus mean : 38.4287**

**Gaus Width: 3.6799**



# B0L002S, U2-ch58, adc2

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entries	73
Mean	43.1
Std Dev	3.385

**Gaus mean : 43.4410**

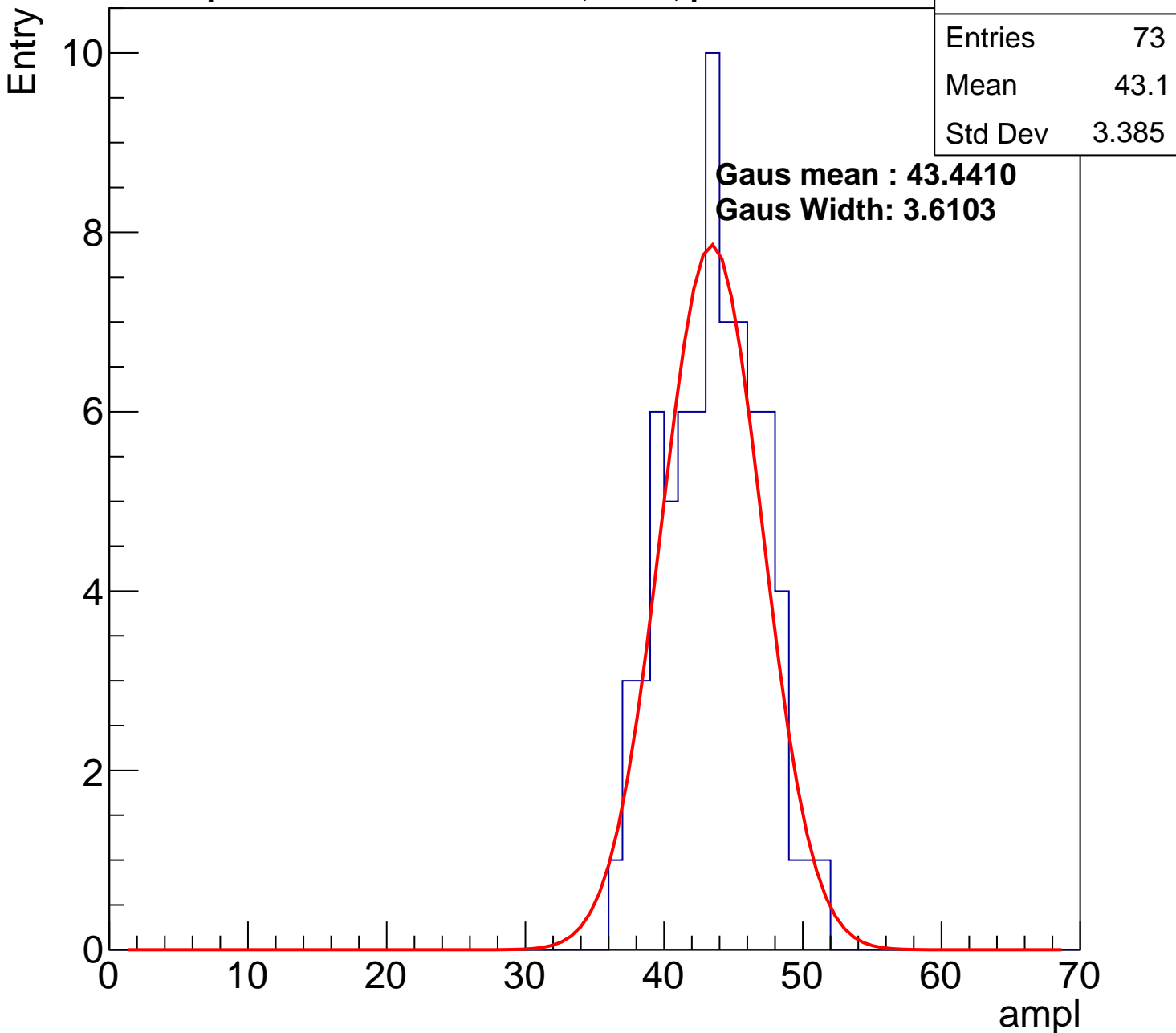
**Gaus Width: 3.6103**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

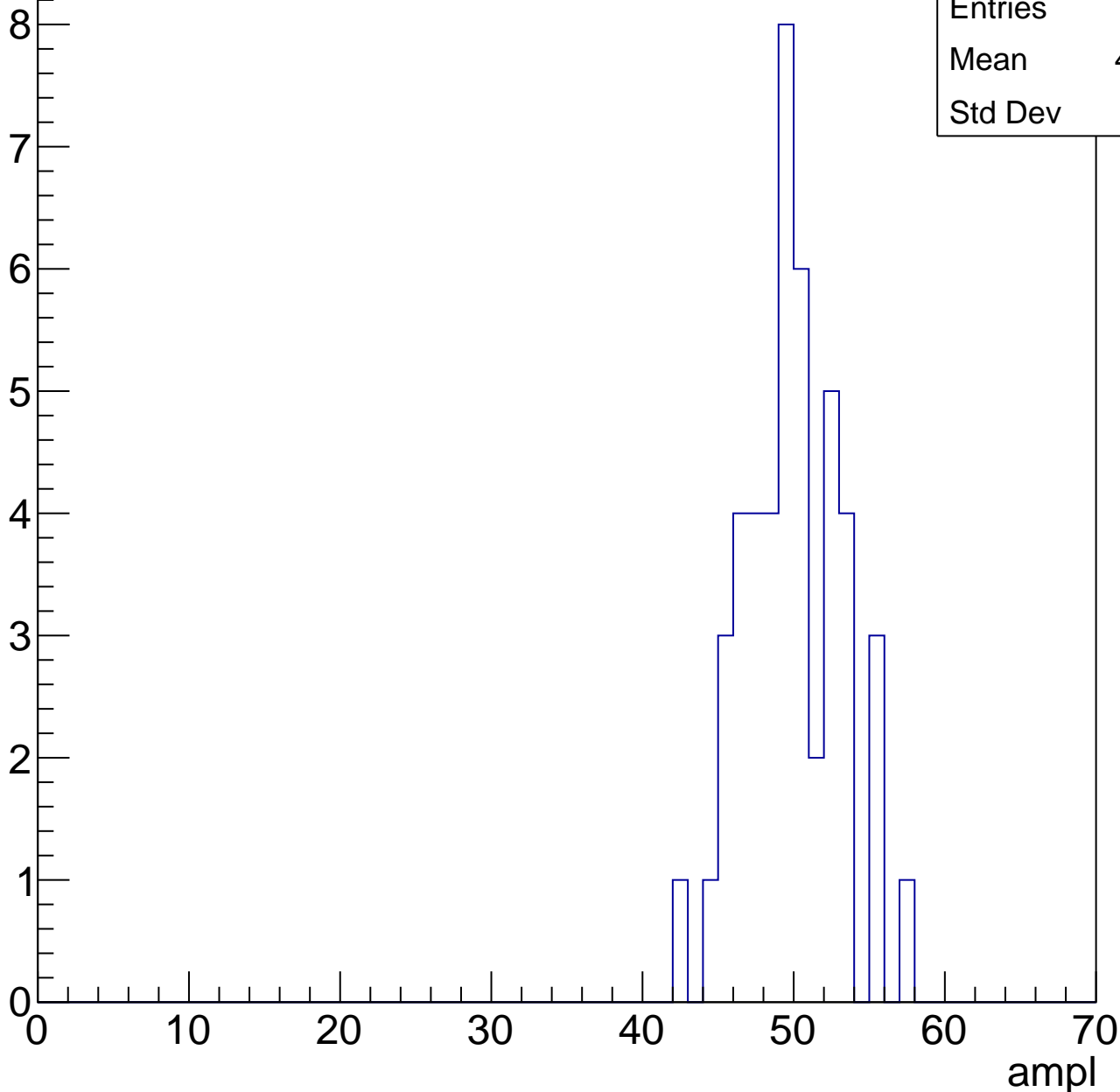


# B0L002S, U2-ch58, adc3

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

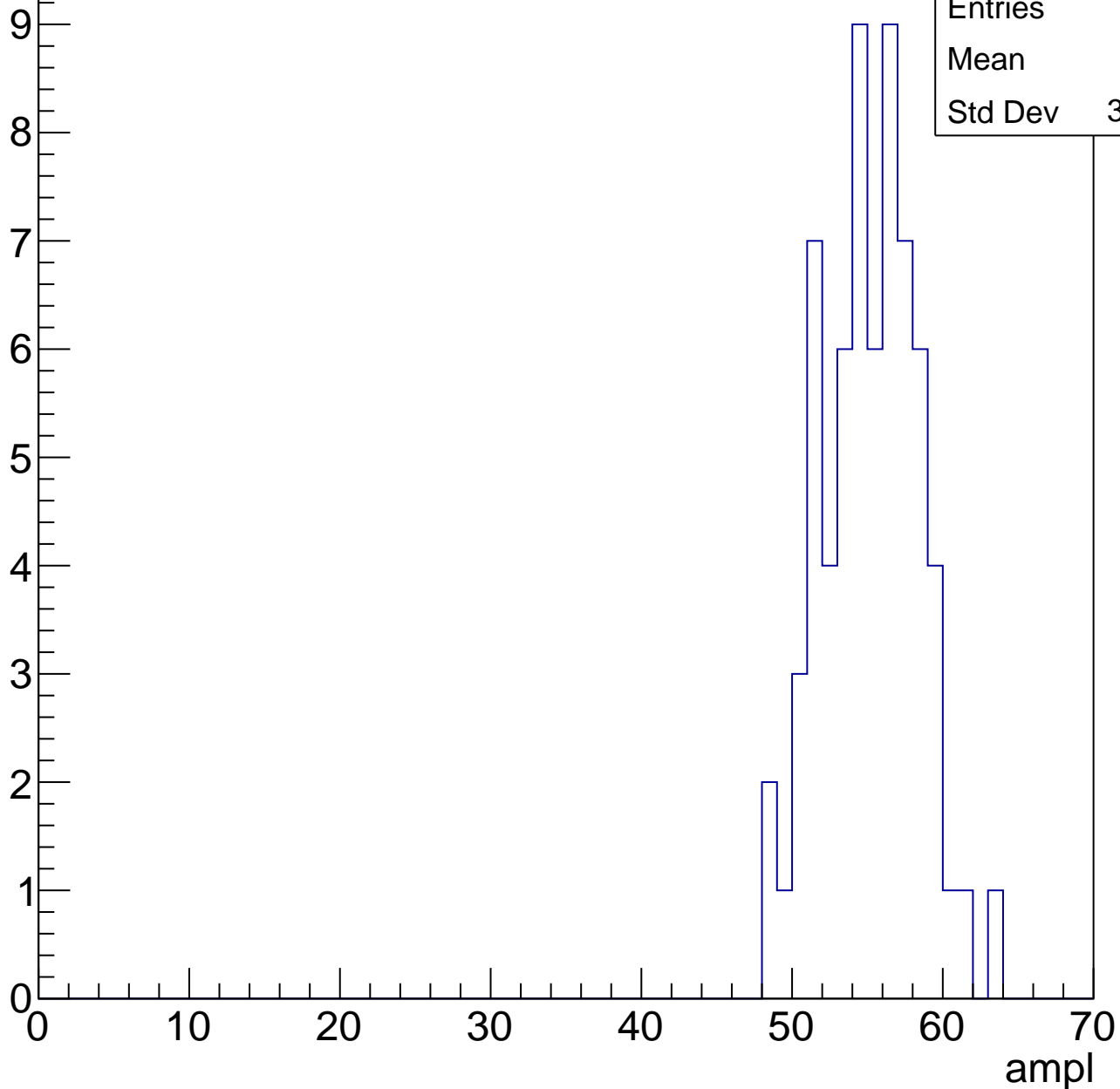
Entries	46
Mean	49.41
Std Dev	3.18



# B0L002S, U2-ch58, adc4

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

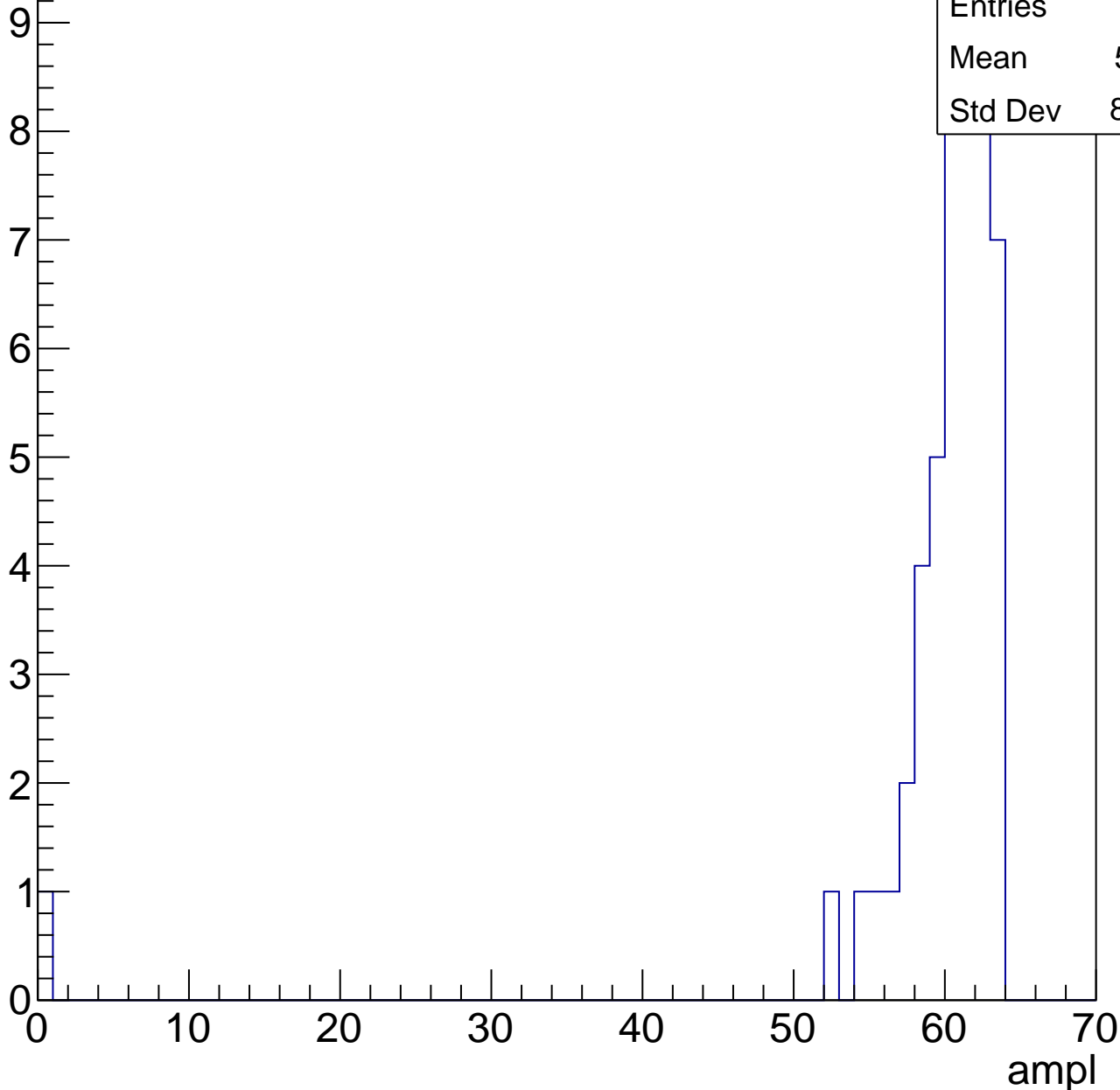


# B0L002S, U2-ch58, adc5

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	48
Mean	58.81
Std Dev	8.915



# B0L002S, U2-ch58, adc6

calib\_packv5\_042523\_0143.root, FC#8, port C1

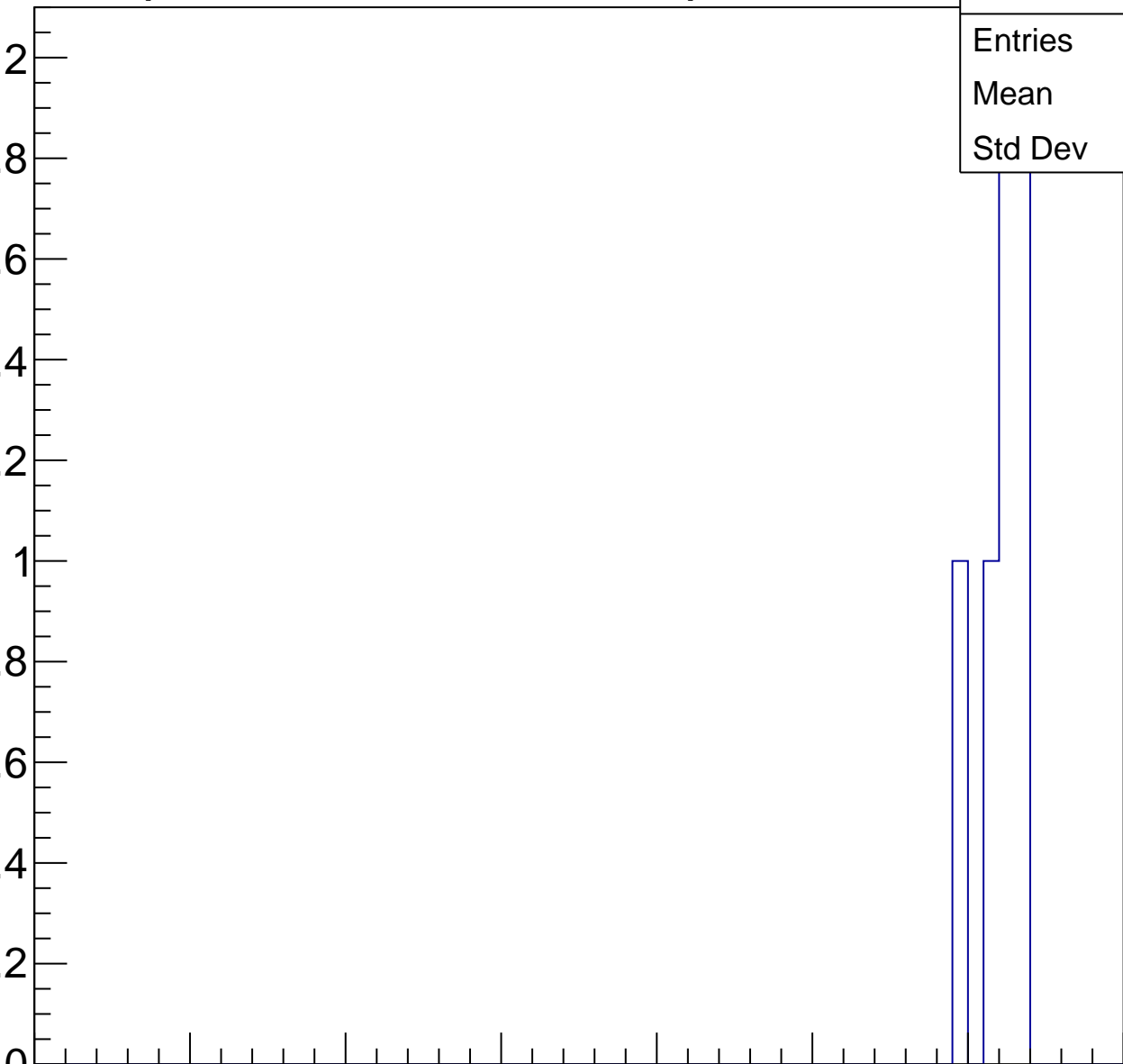
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	6
Mean	61.67
Std Dev	1.374

0 10 20 30 40 50 60 70

ampl





# B0L002S, U2-ch58, adc7

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



Entries	2
Mean	11
Std Dev	11

# B0L002S, U2-ch59, adc0

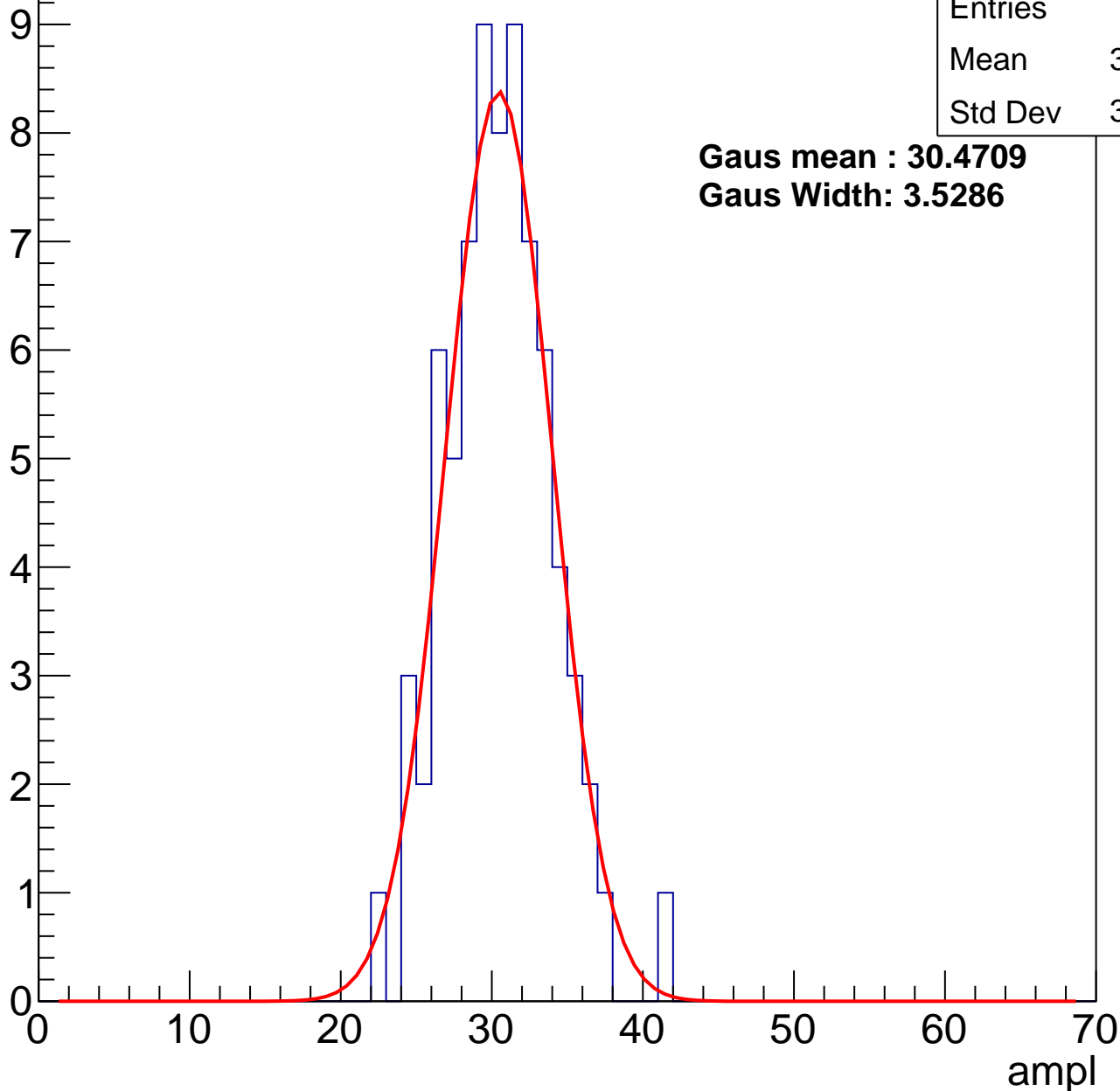
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	74
Mean	30.05
Std Dev	3.432

**Gaus mean : 30.4709**

**Gaus Width: 3.5286**



# B0L002S, U2-ch59, adc1

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entries	71
Mean	37.28
Std Dev	3.096

**Gaus mean : 37.6032**

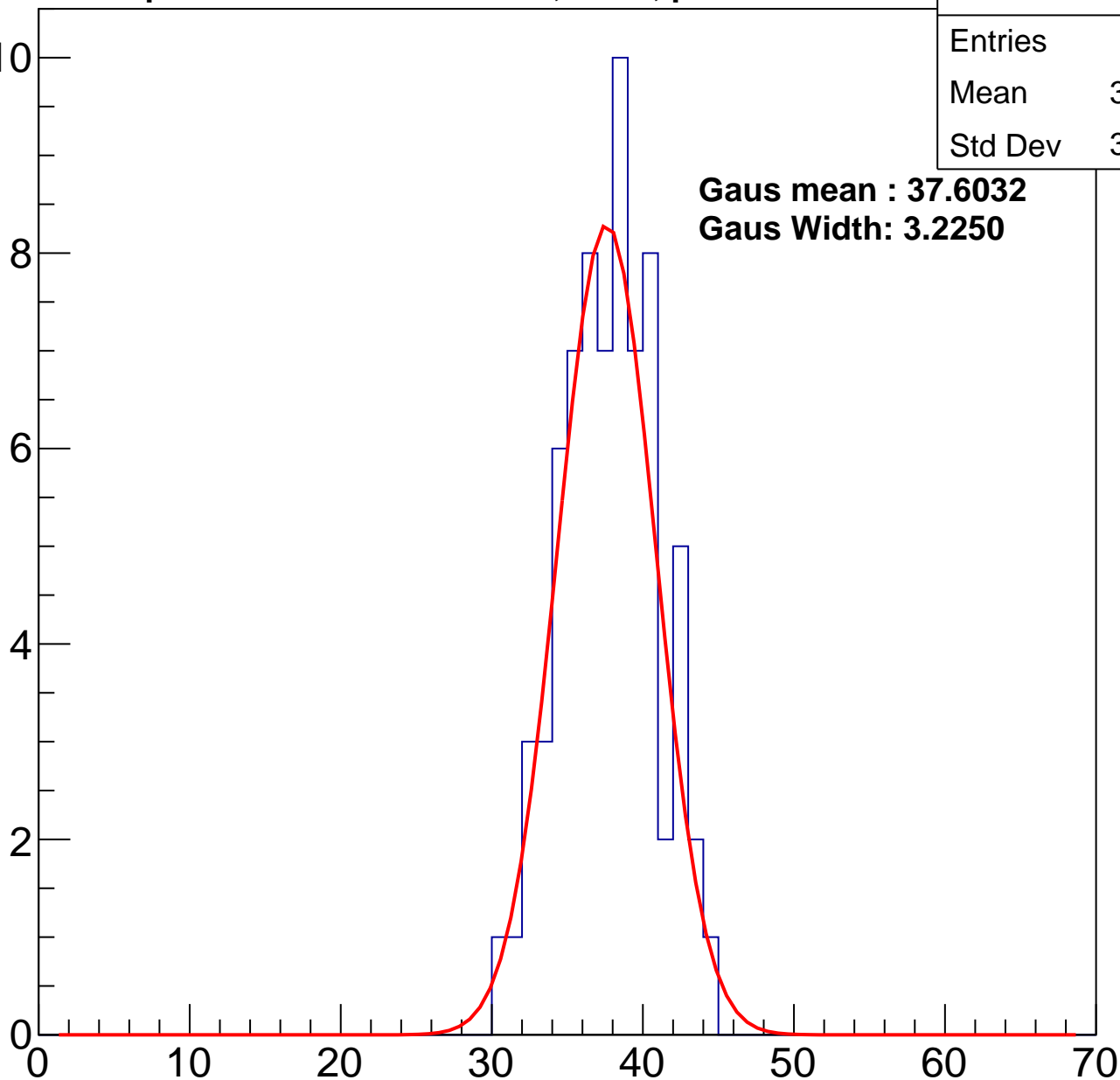
**Gaus Width: 3.2250**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B0L002S, U2-ch59, adc2

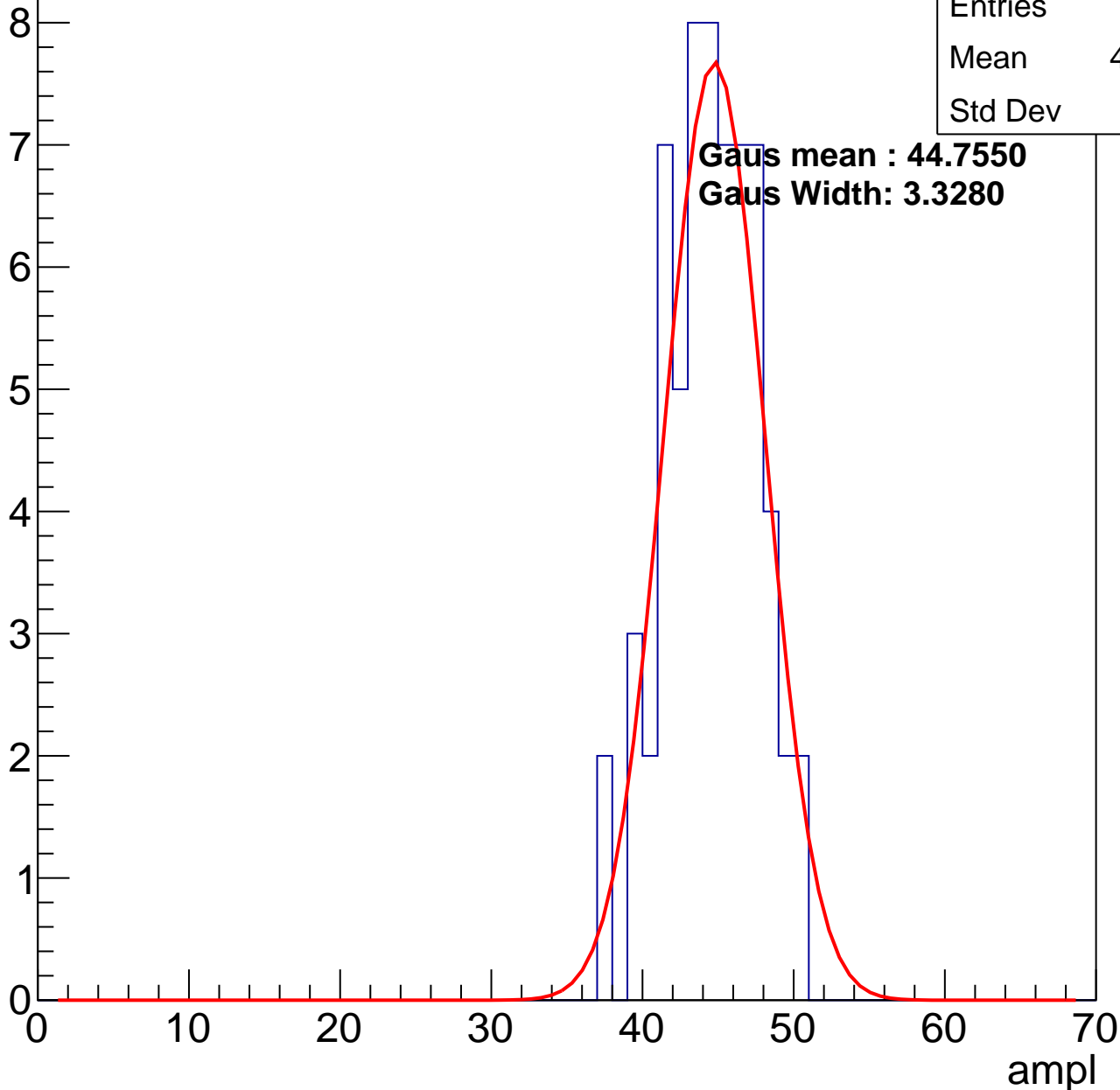
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	64
Mean	44.06
Std Dev	3.01

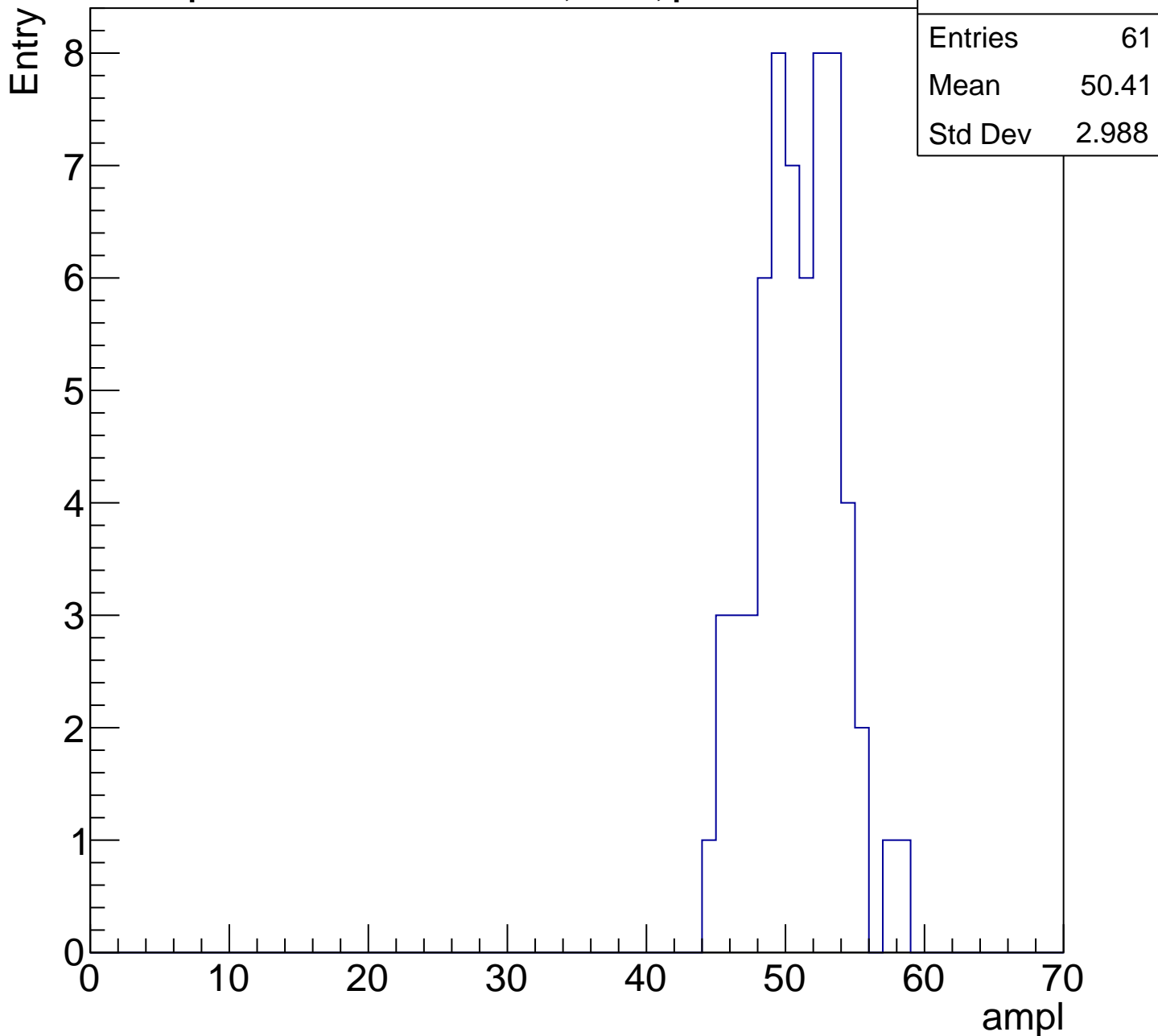
**Gaus mean : 44.7550**

**Gaus Width: 3.3280**



# B0L002S, U2-ch59, adc3

calib\_packv5\_042523\_0143.root, FC#8, port C1



# B0L002S, U2-ch59, adc4

calib\_packv5\_042523\_0143.root, FC#8, port C1

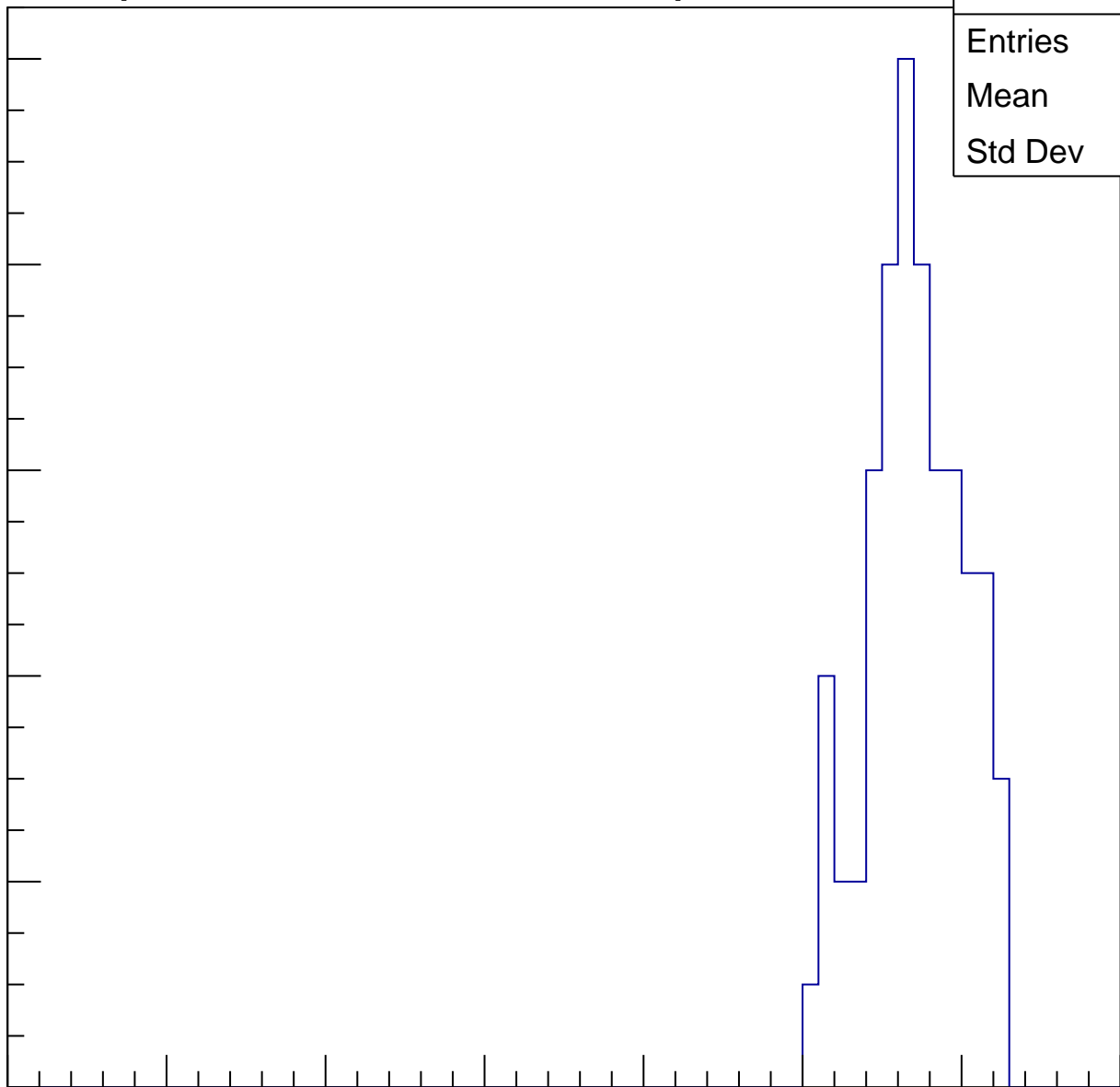
Entries	66
Mean	56.62
Std Dev	2.994

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

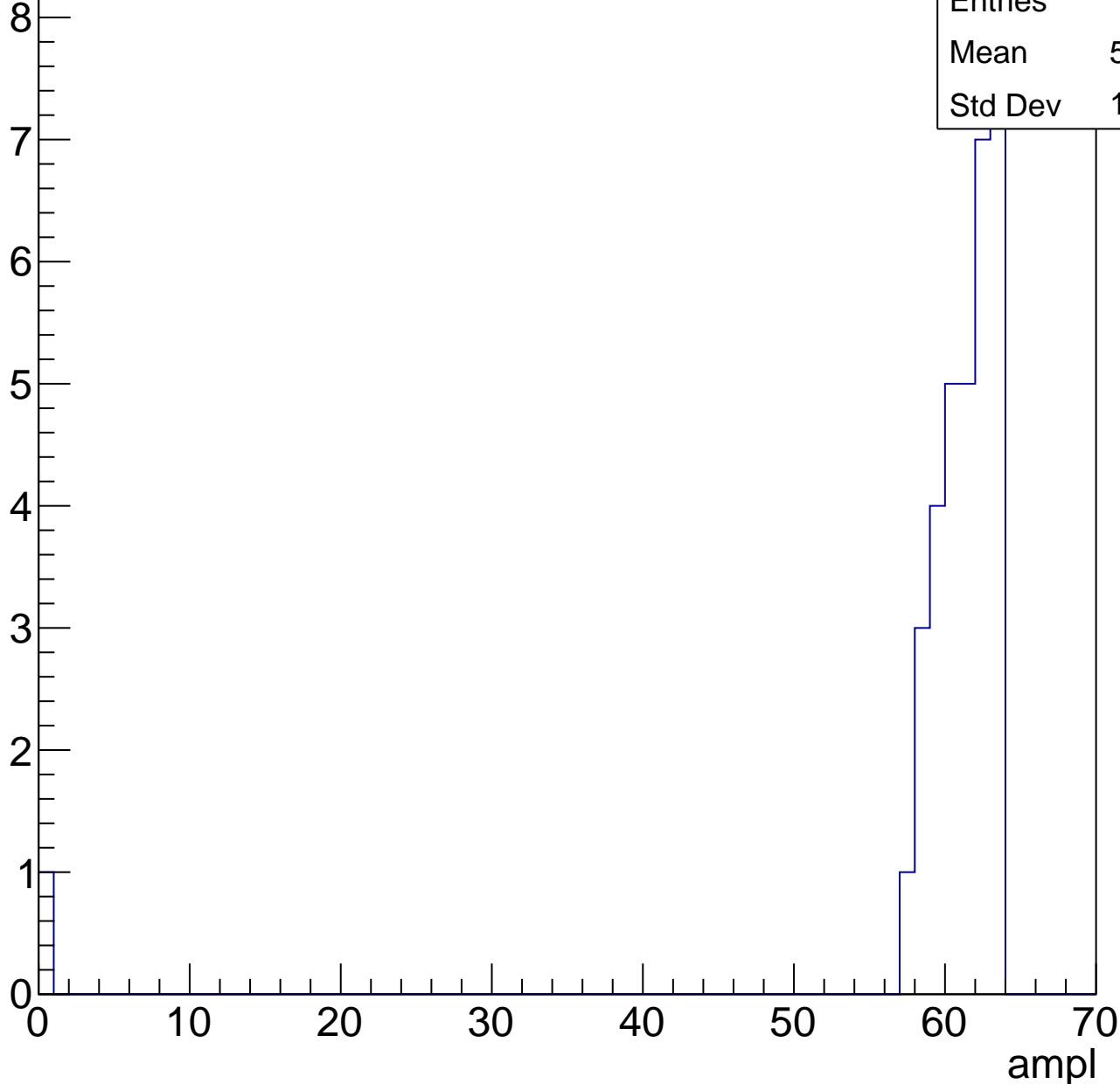


# B0L002S, U2-ch59, adc5

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	34
Mean	59.12
Std Dev	10.44



# B0L002S, U2-ch59, adc6

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



Entries	2
Mean	63
Std Dev	0



# B0L002S, U2-ch59, adc7

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



# B0L002S, U2-ch60, adc0

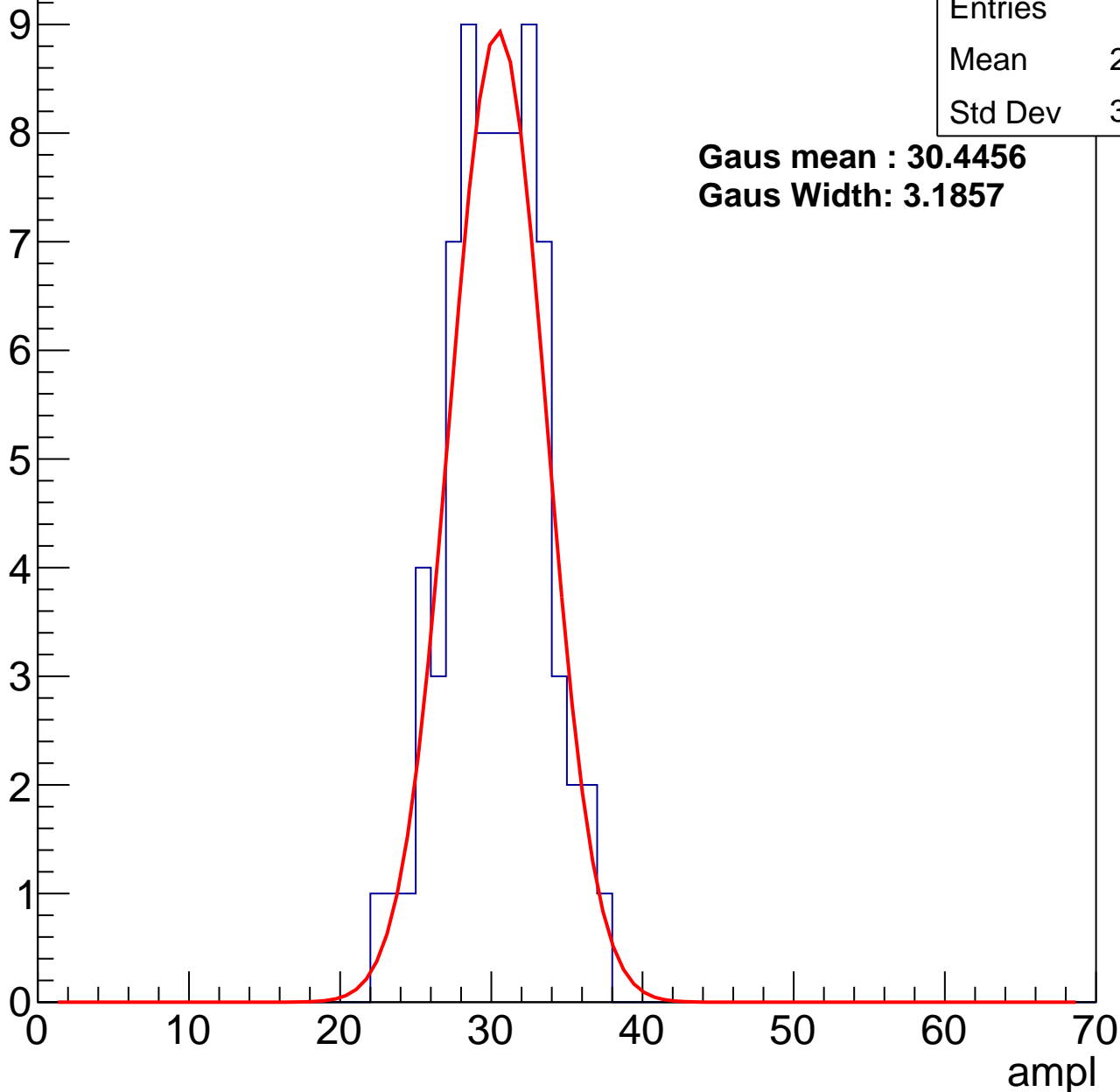
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	74
Mean	29.84
Std Dev	3.137

**Gaus mean : 30.4456**

**Gaus Width: 3.1857**



# B0L002S, U2-ch60, adc1

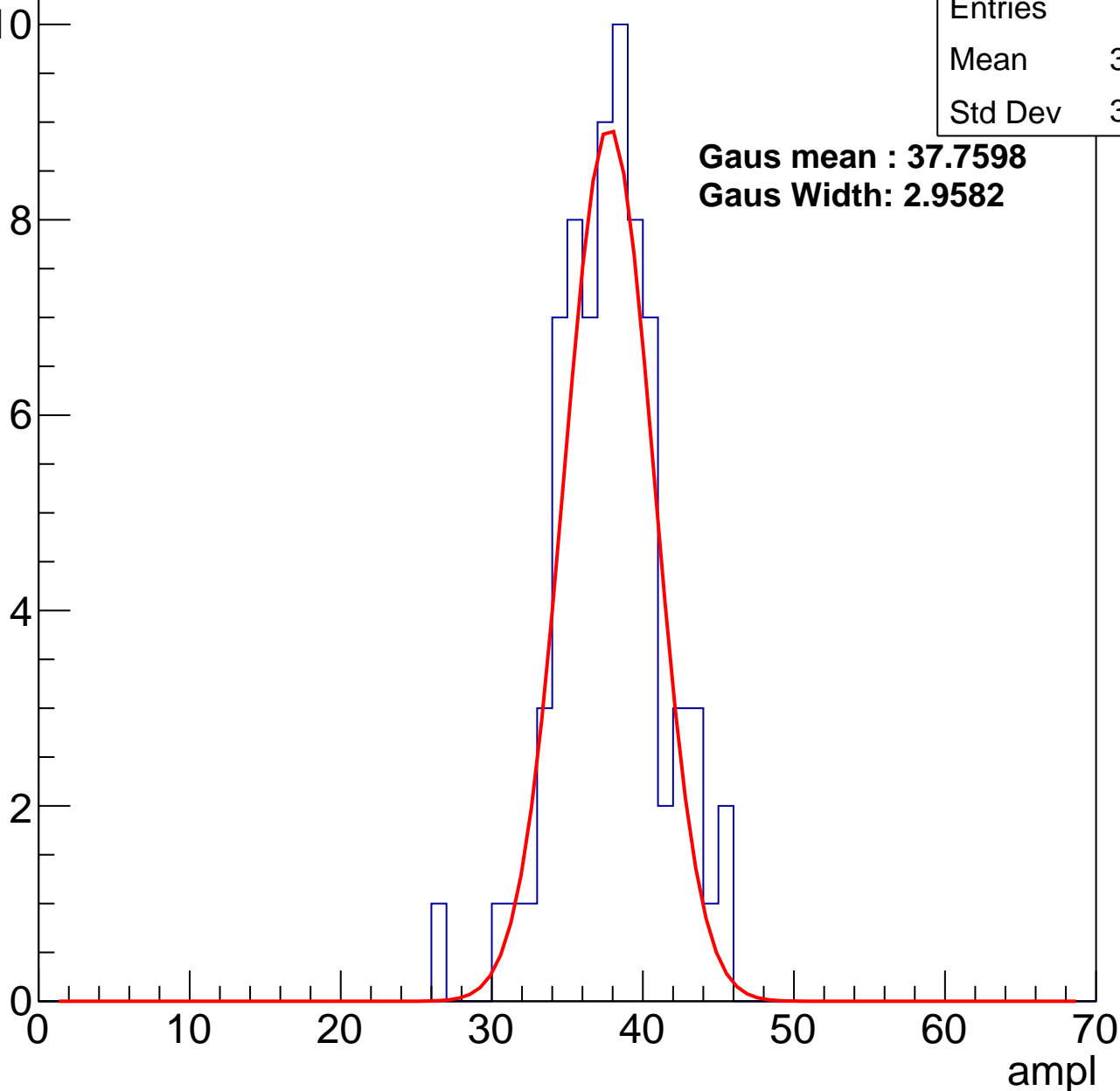
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	74
Mean	37.35
Std Dev	3.427

**Gaus mean : 37.7598**

**Gaus Width: 2.9582**



# B0L002S, U2-ch60, adc2

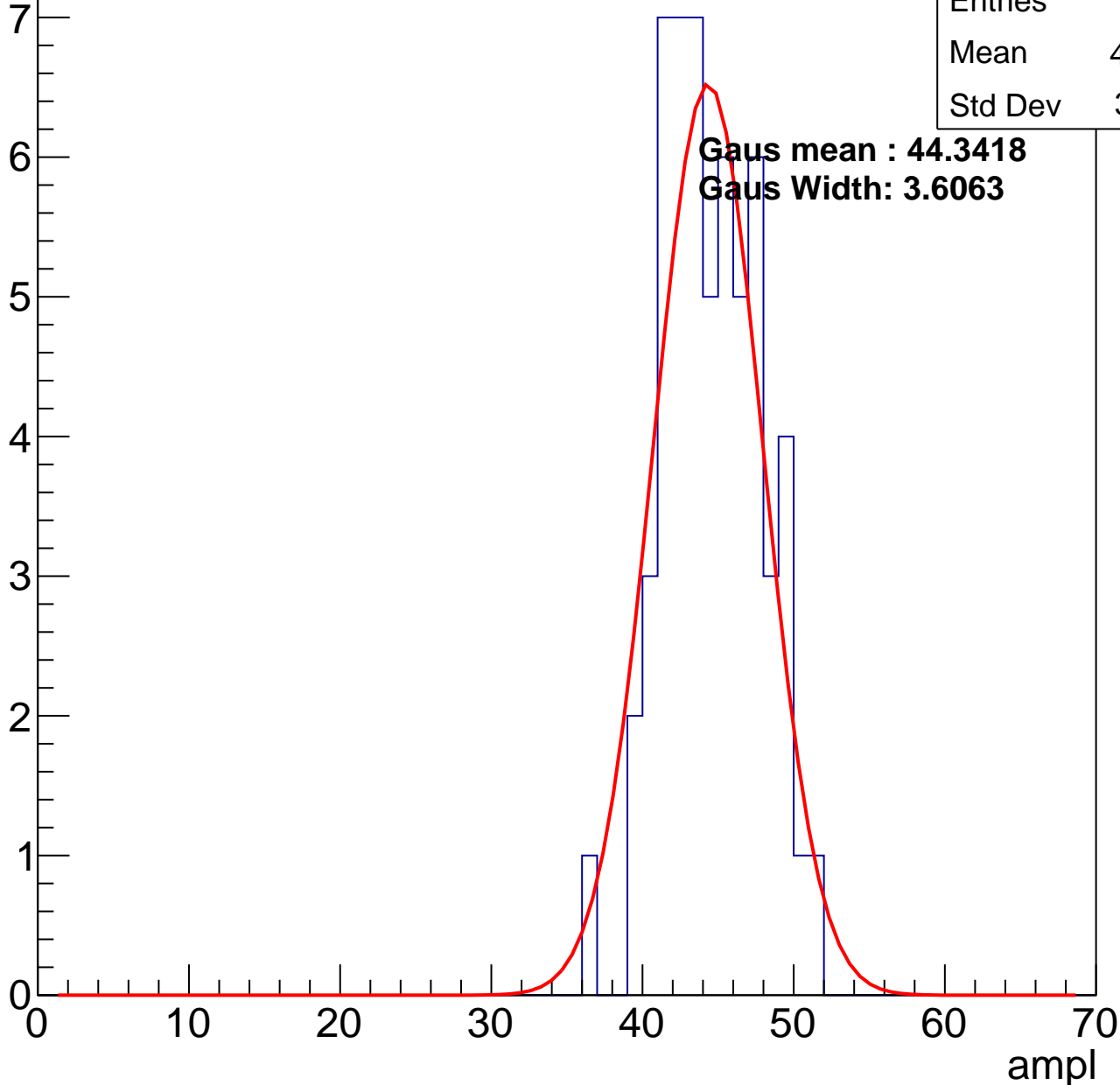
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	58
Mean	44.12
Std Dev	3.141

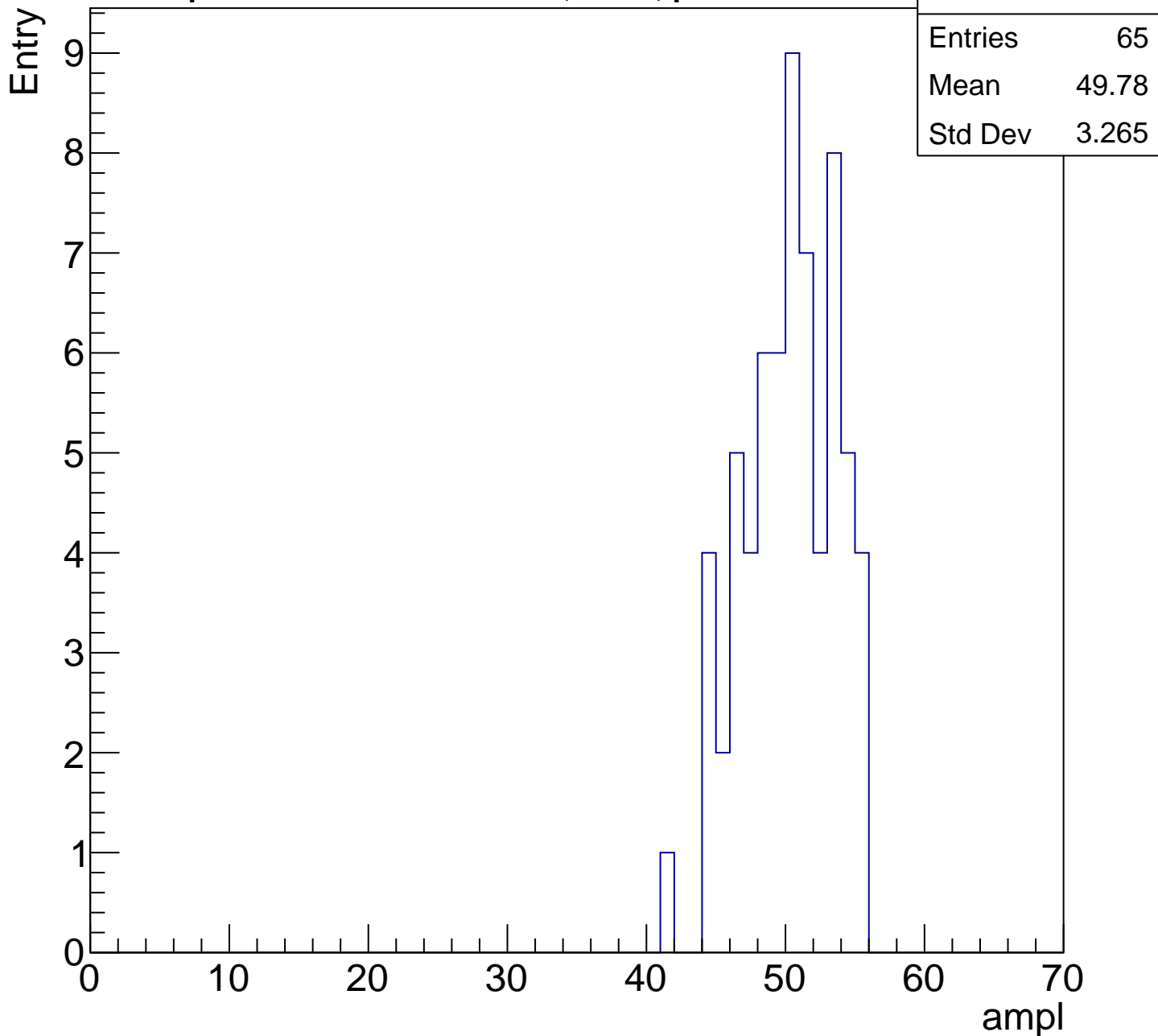
**Gaus mean : 44.3418**

**Gaus Width: 3.6063**



# B0L002S, U2-ch60, adc3

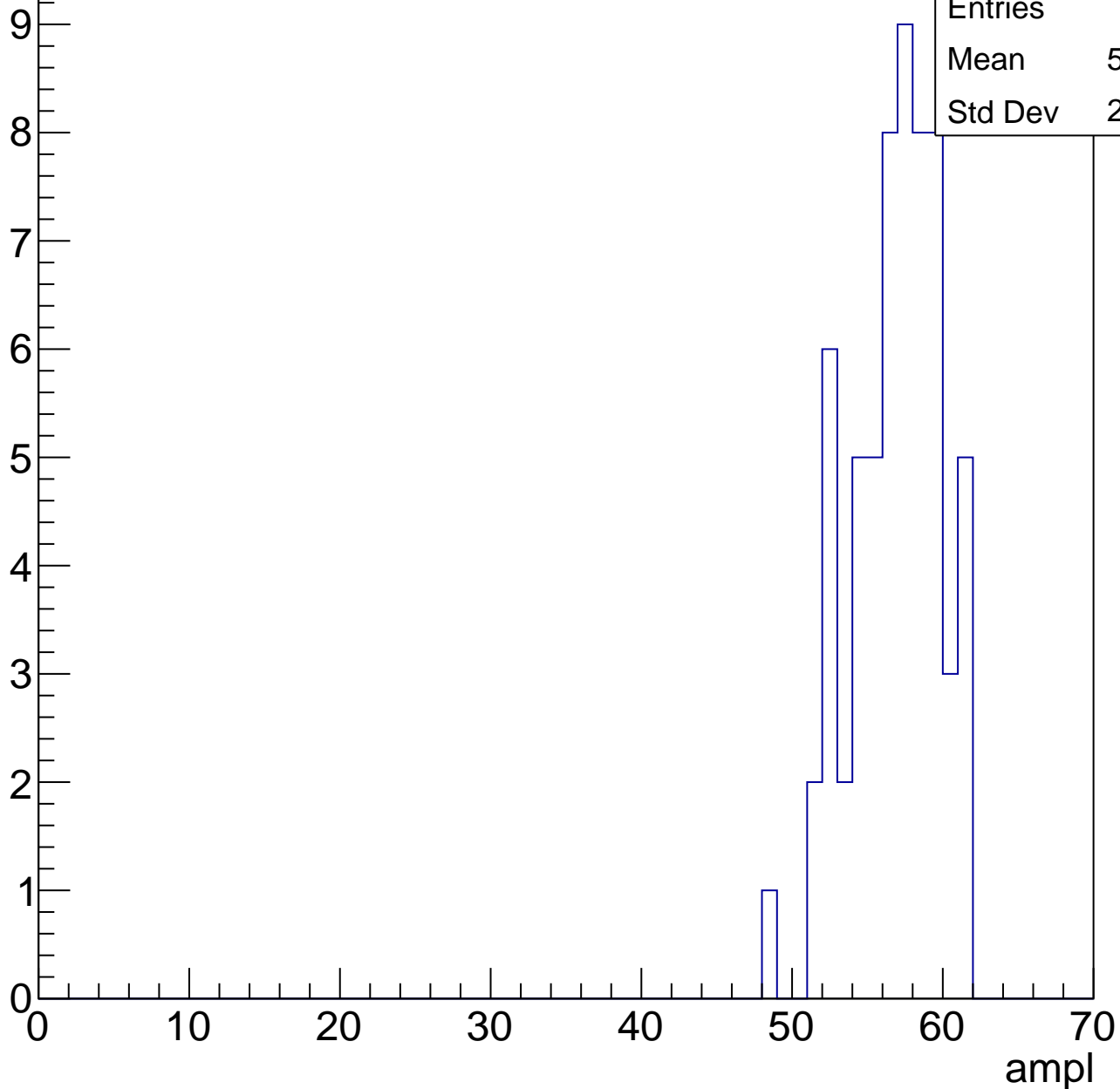
calib\_packv5\_042523\_0143.root, FC#8, port C1



# B0L002S, U2-ch60, adc4

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



Entries	62
Mean	56.37
Std Dev	2.925

# B0L002S, U2-ch60, adc5

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

10

Entries 41

Mean 59.34

Std Dev 9.619

8

6

4

2

0

0

10

20

30

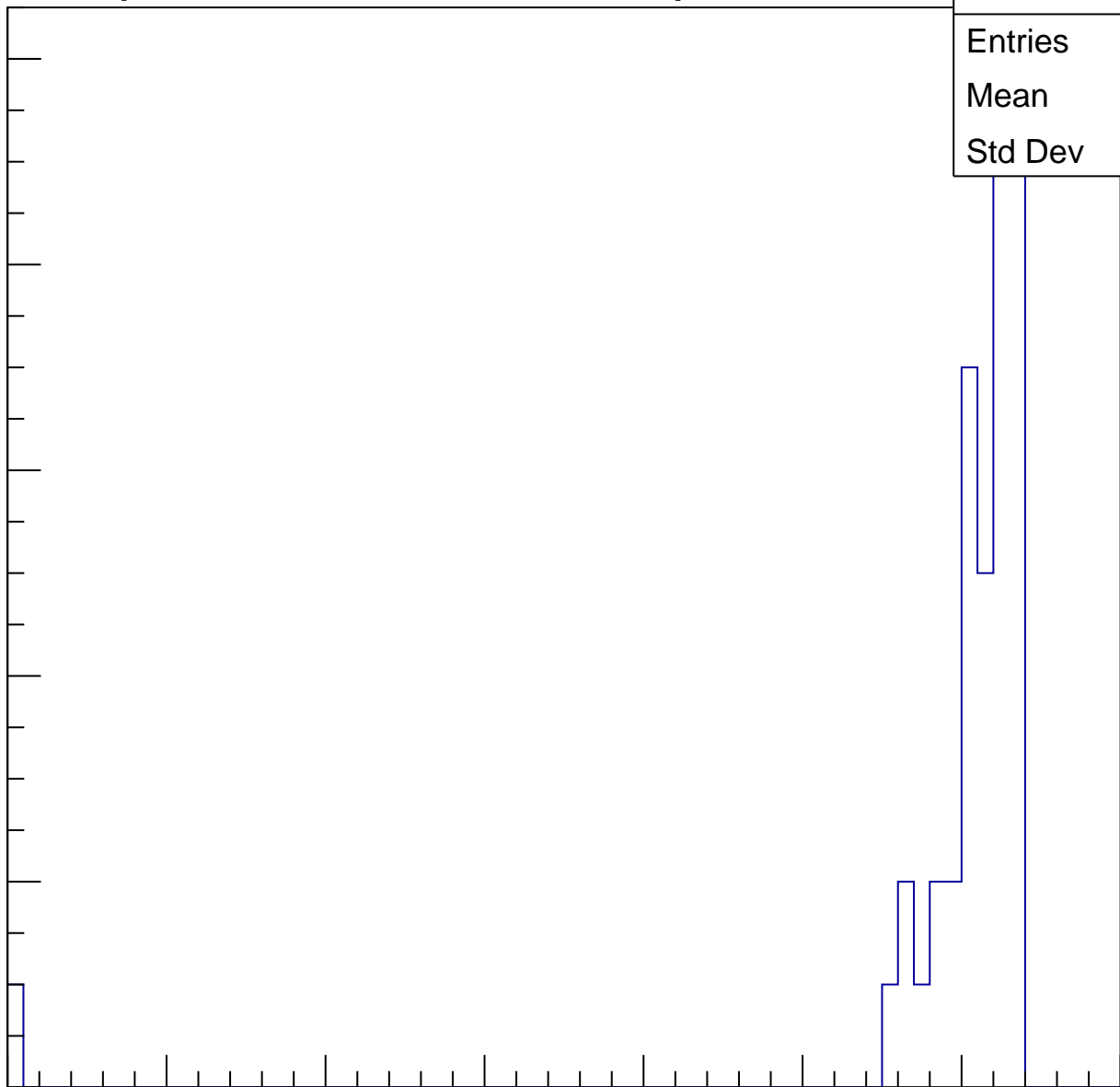
40

50

60

70

ampl



# B0L002S, U2-ch60, adc6

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



Entries	0
Mean	0
Std Dev	0



# B0L002S, U2-ch60, adc7

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L002S, U2-ch61, adc0

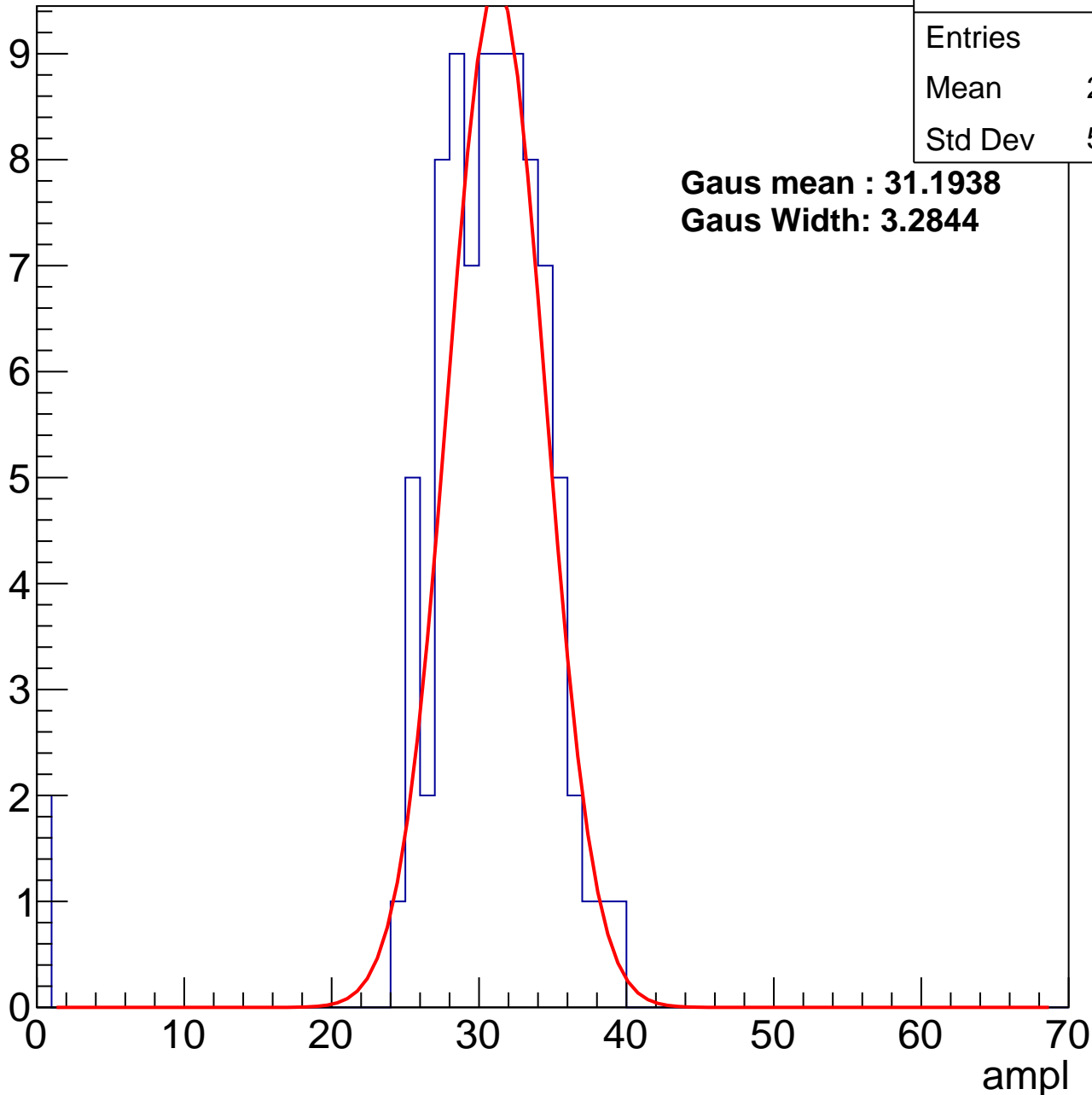
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	86
Mean	29.91
Std Dev	5.631

**Gaus mean : 31.1938**

**Gaus Width: 3.2844**



# B0L002S, U2-ch61, adc1

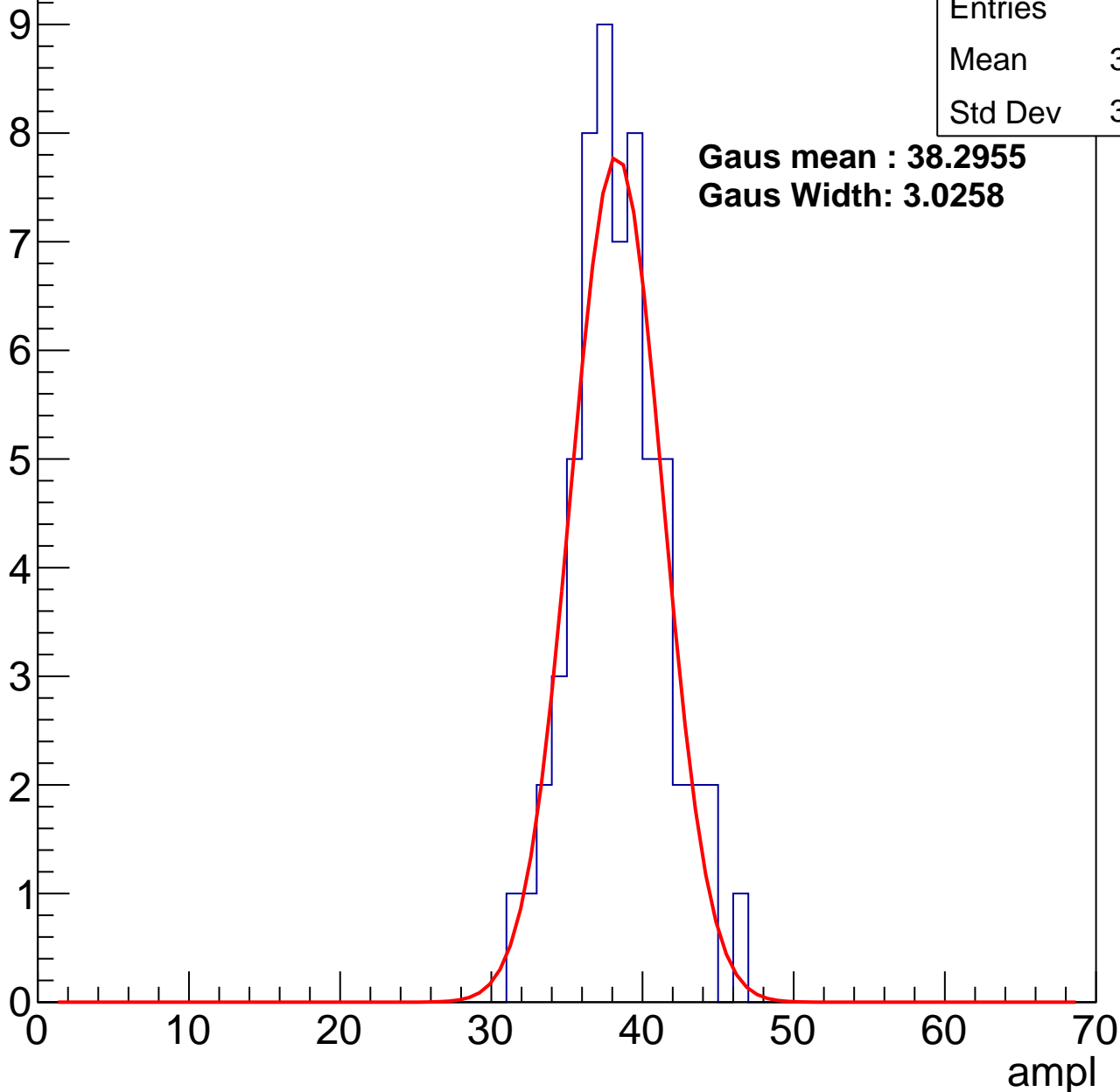
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	61
Mean	37.93
Std Dev	3.029

**Gaus mean : 38.2955**

**Gaus Width: 3.0258**



# B0L002S, U2-ch61, adc2

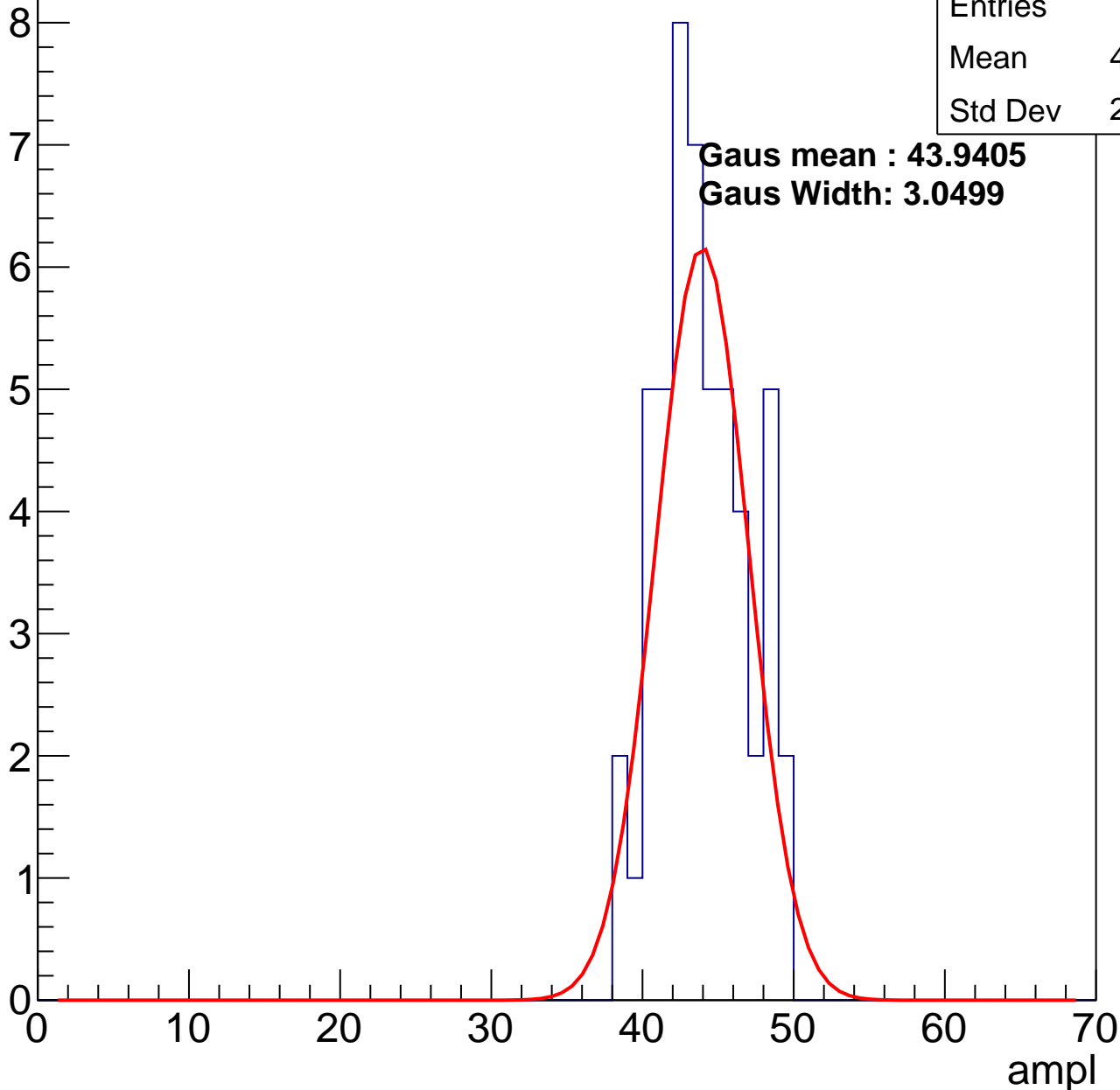
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	51
Mean	43.49
Std Dev	2.859

**Gaus mean : 43.9405**

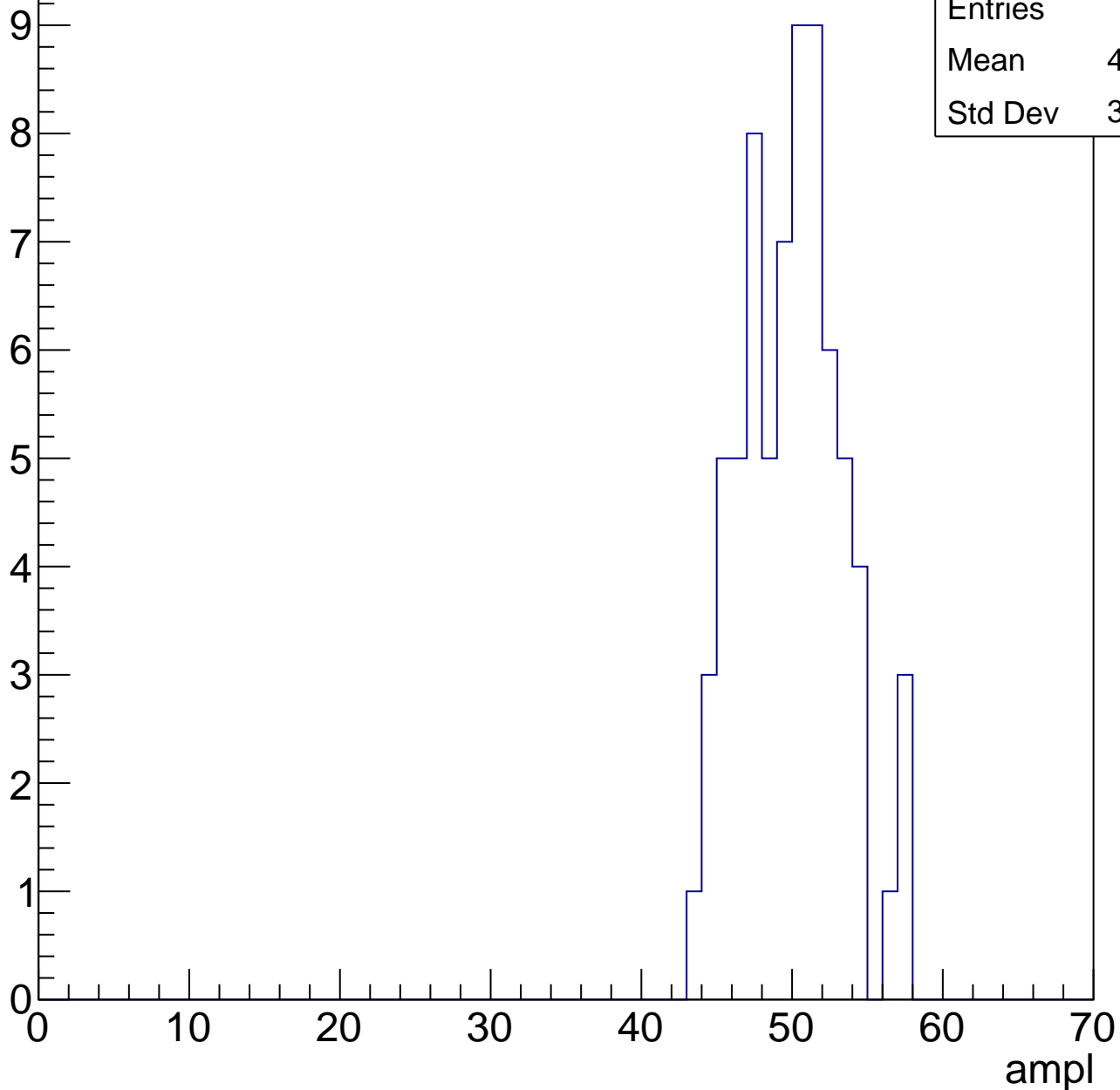
**Gaus Width: 3.0499**



# B0L002S, U2-ch61, adc3

calib\_packv5\_042523\_0143.root, FC#8, port C1

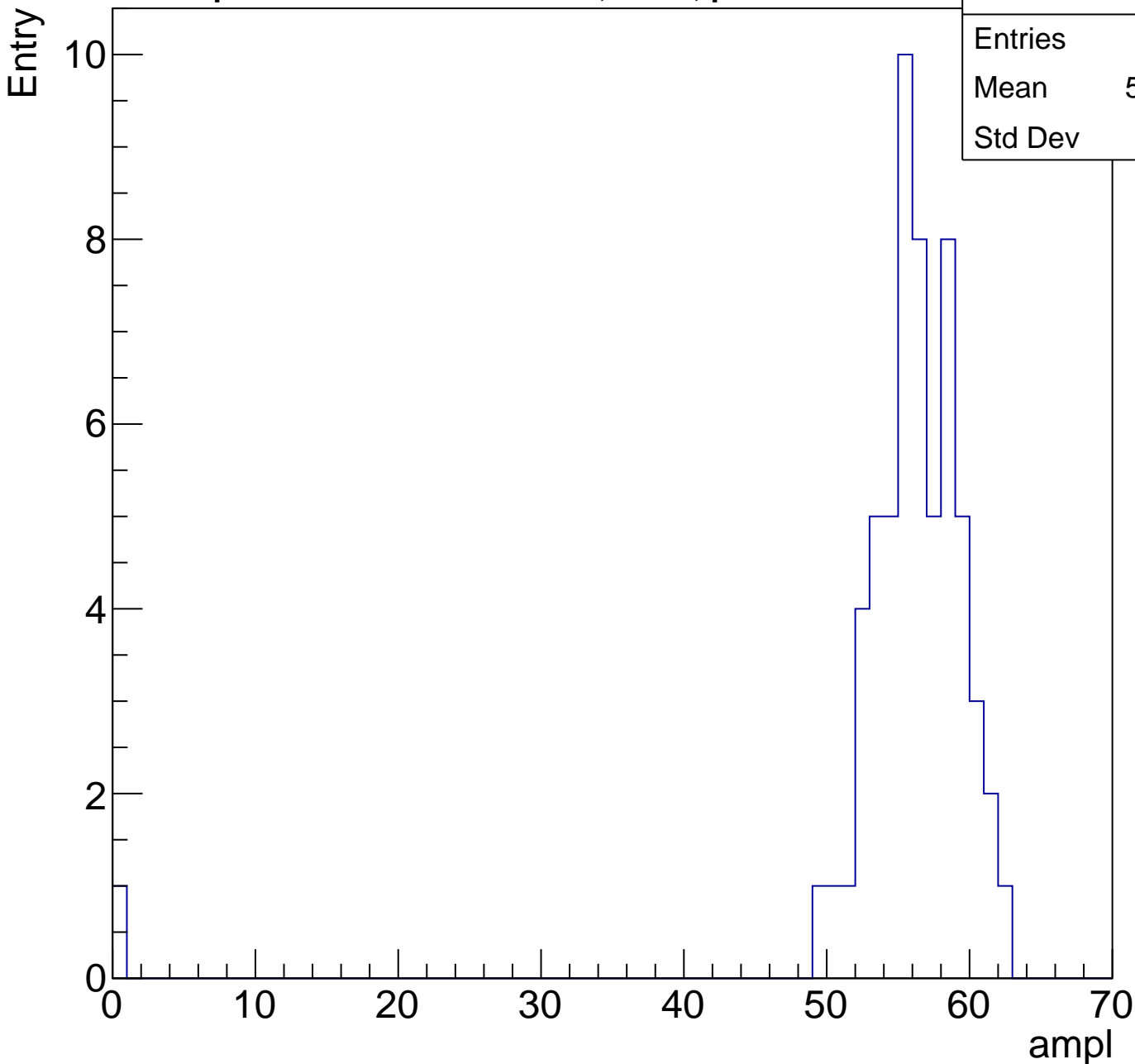
Entry



# B0L002S, U2-ch61, adc4

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entries	60
Mean	54.98
Std Dev	7.68



# B0L002S, U2-ch61, adc5

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	40
Mean	60.52
Std Dev	2.133

ampl

0 10 20 30 40 50 60 70

0

1

2

3

4

5

6

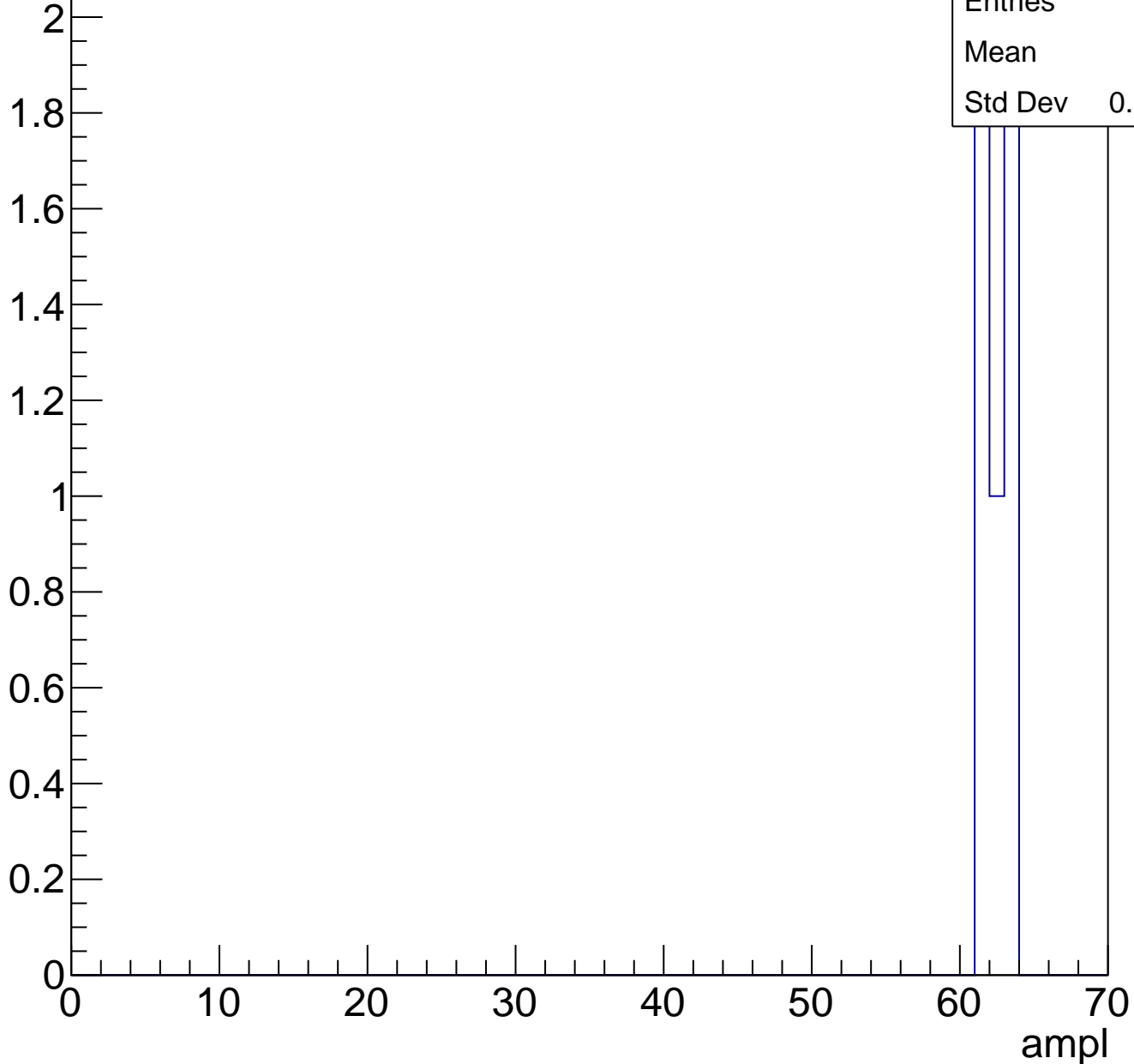
7

8

# B0L002S, U2-ch61, adc6

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry





# B0L002S, U2-ch61, adc7

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



# B0L002S, U2-ch62, adc0

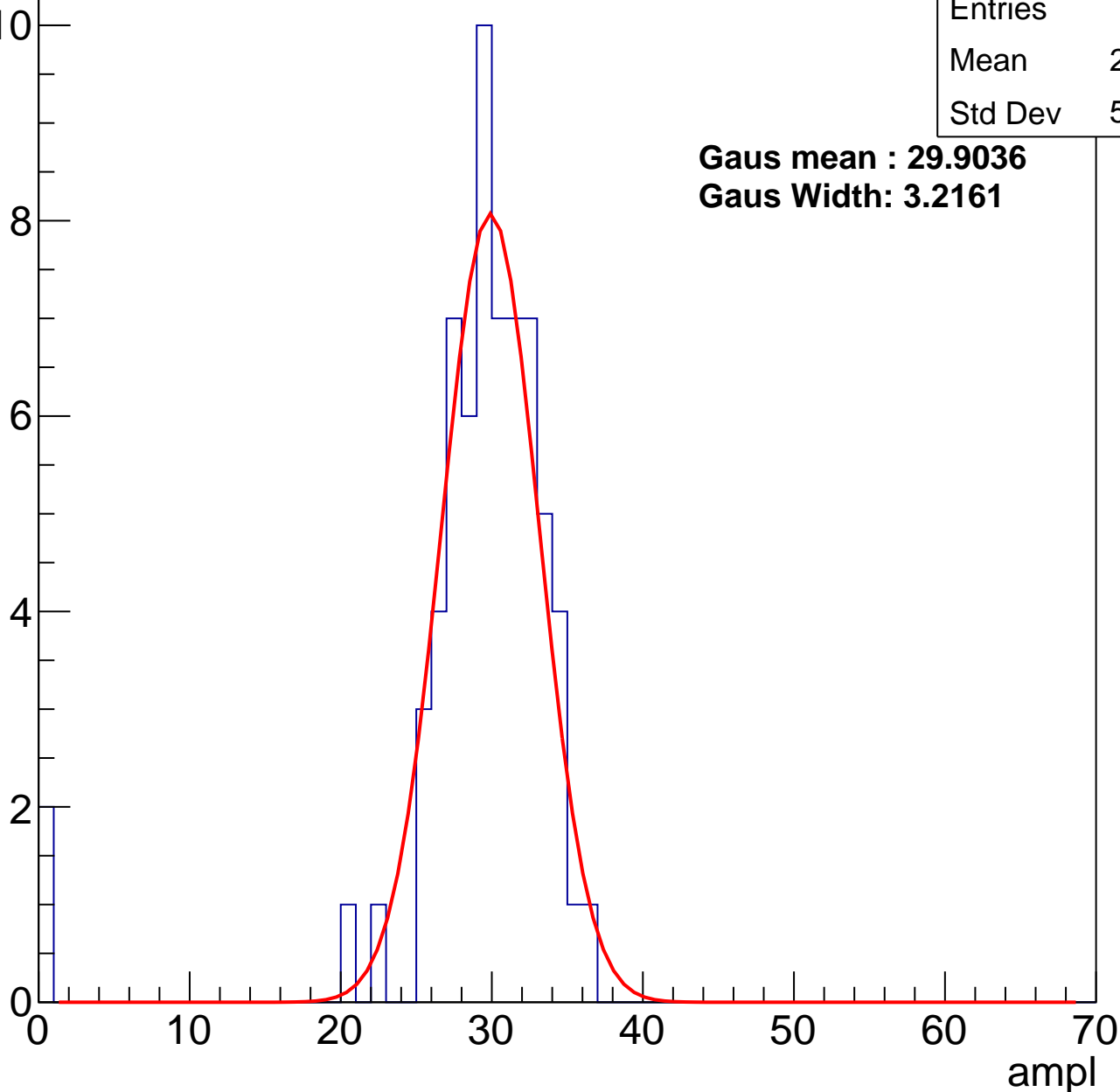
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	66
Mean	28.65
Std Dev	5.884

**Gaus mean : 29.9036**

**Gaus Width: 3.2161**



# B0L002S, U2-ch62, adc1

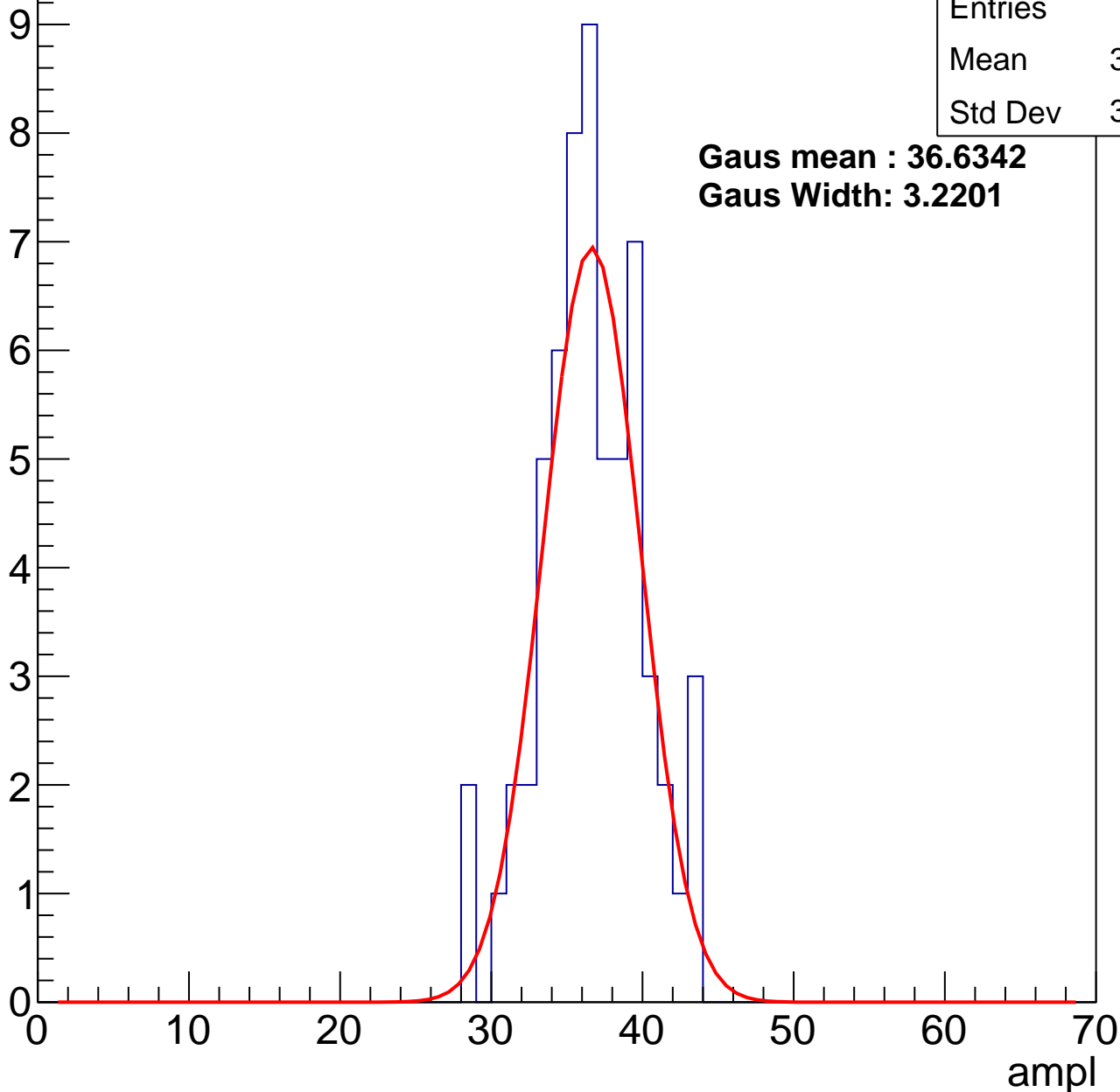
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	61
Mean	36.16
Std Dev	3.364

**Gaus mean : 36.6342**

**Gaus Width: 3.2201**



# B0L002S, U2-ch62, adc2

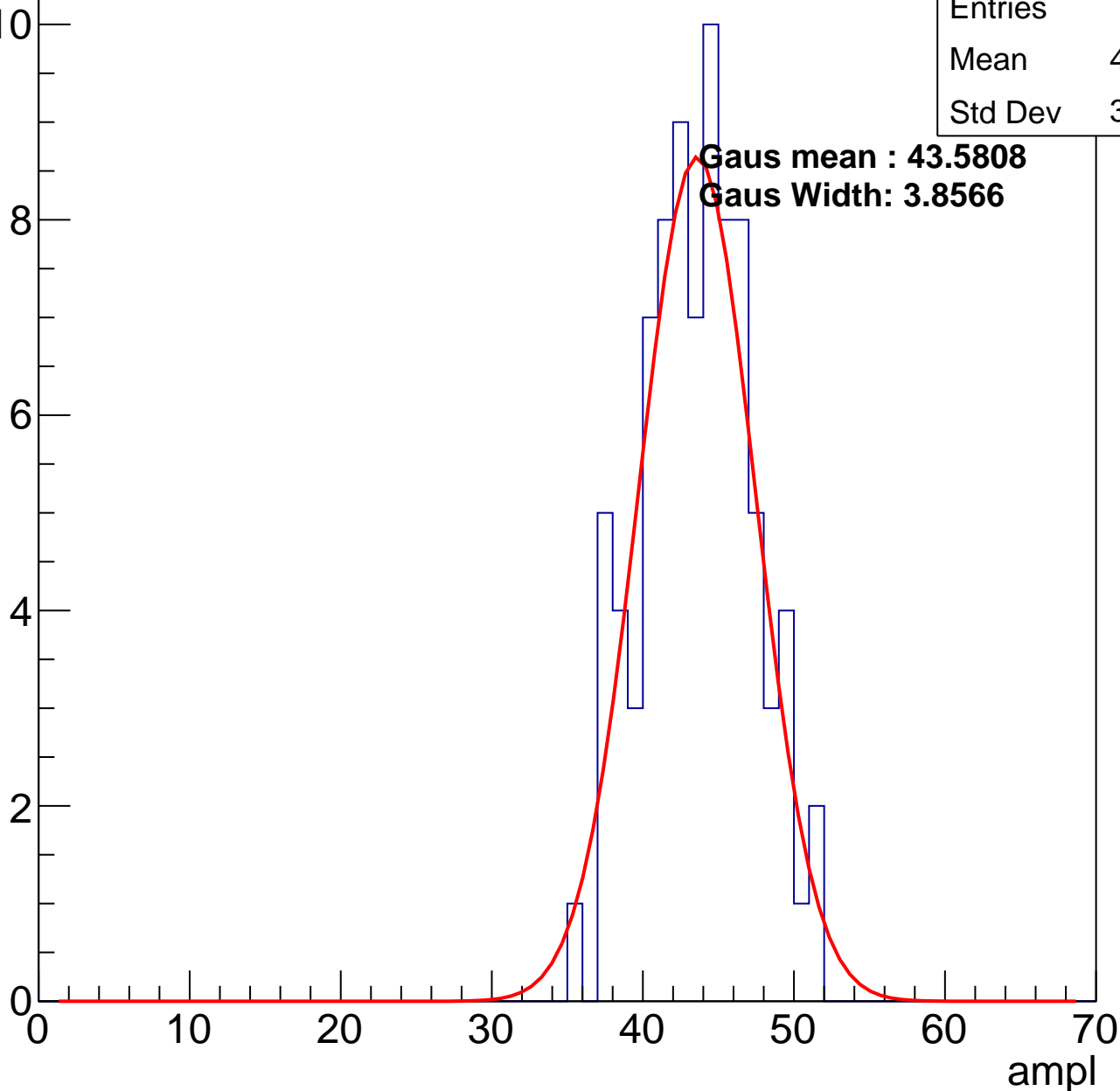
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	85
Mean	43.19
Std Dev	3.569

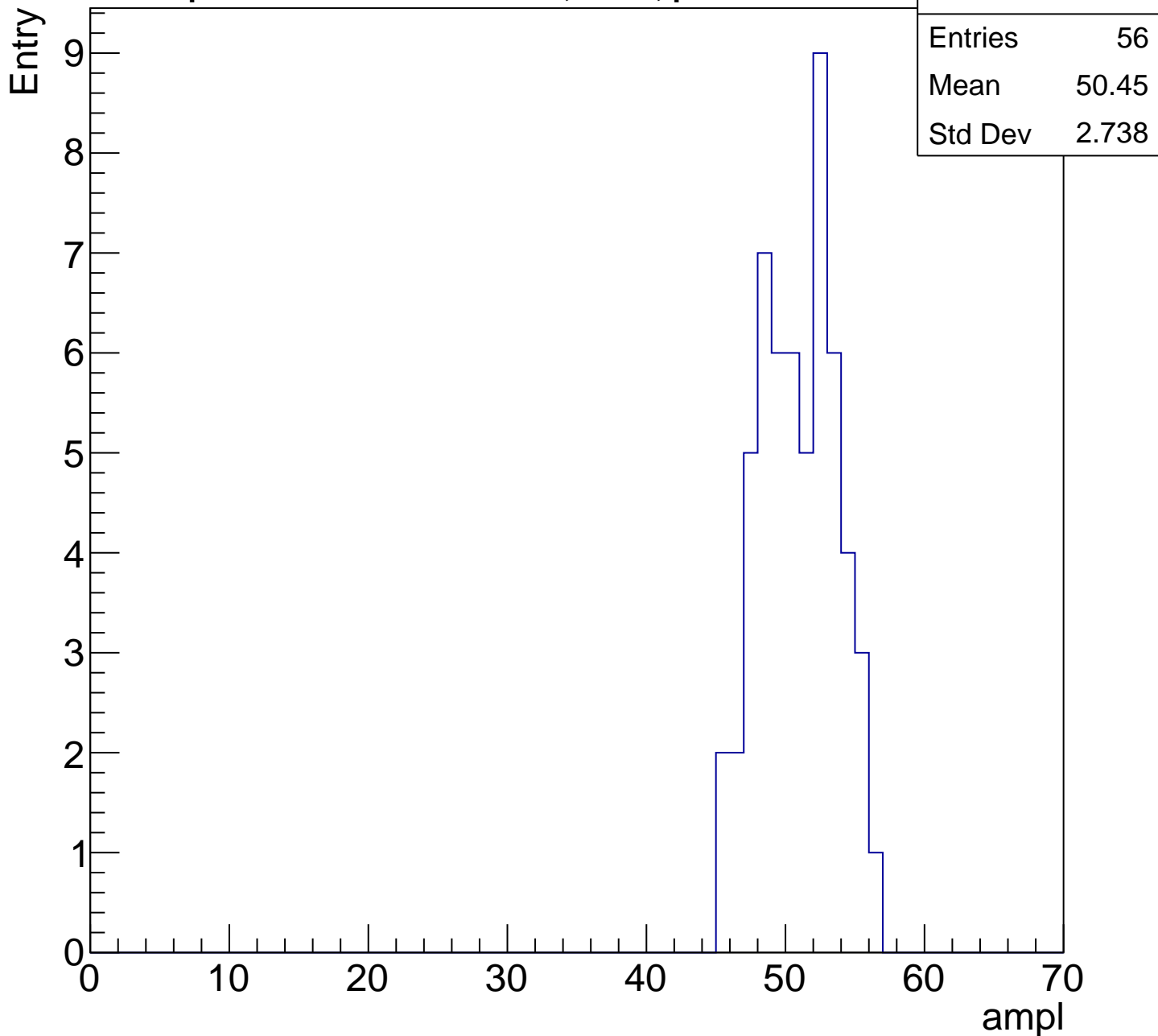
**Gaus mean : 43.5808**

**Gaus Width: 3.8566**



# B0L002S, U2-ch62, adc3

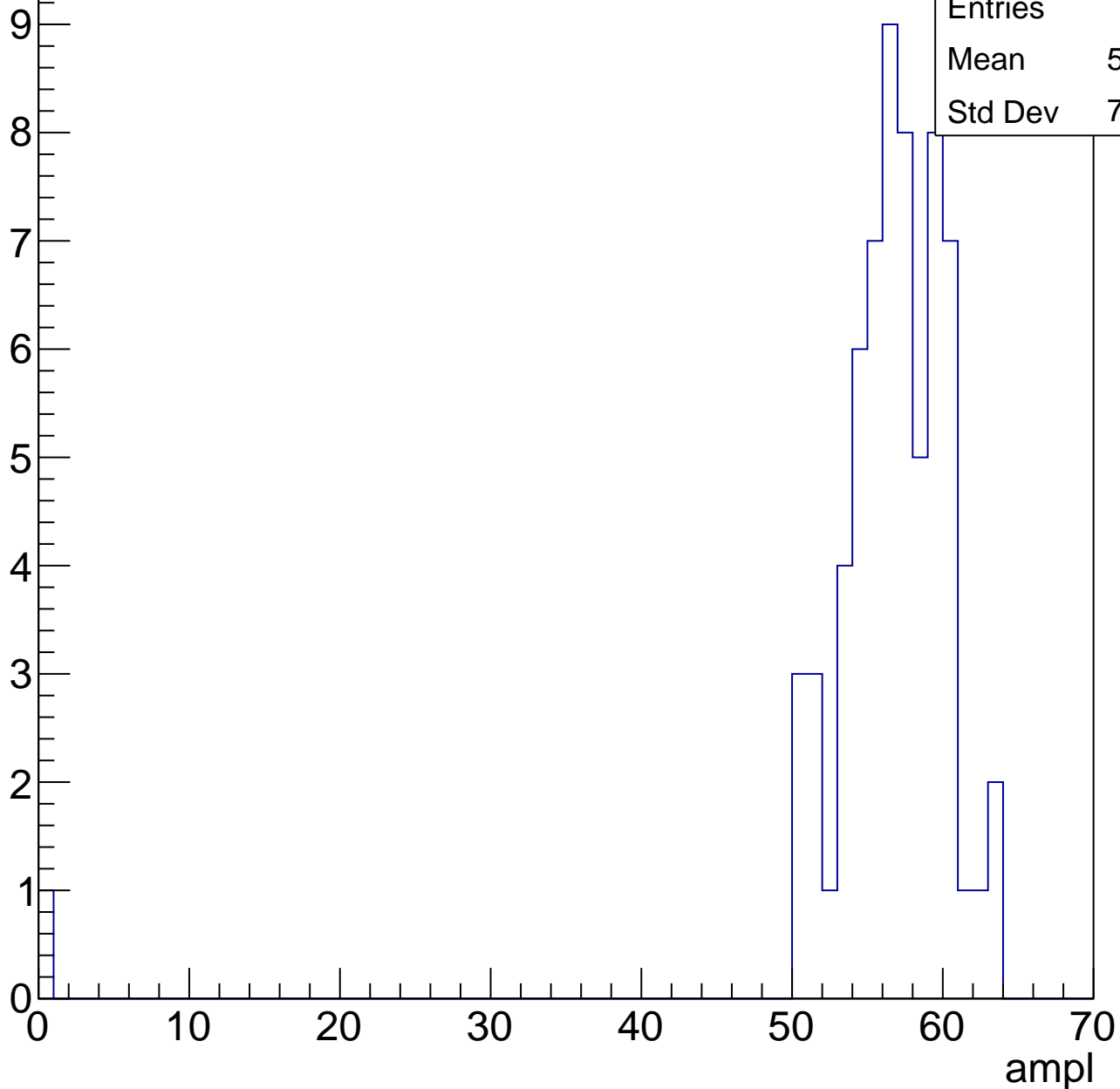
calib\_packv5\_042523\_0143.root, FC#8, port C1



# B0L002S, U2-ch62, adc4

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



# B0L002S, U2-ch62, adc5

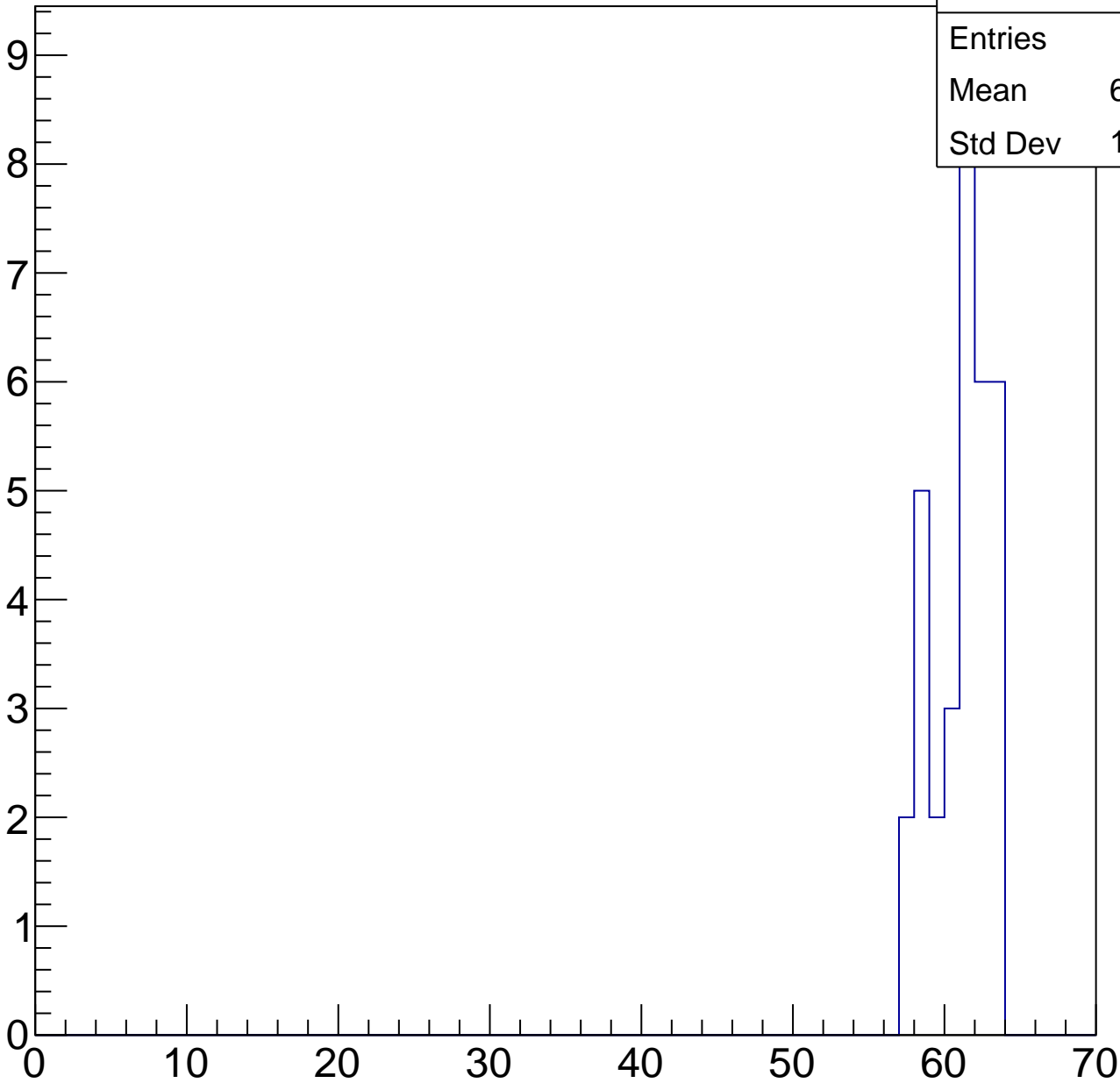
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	33
Mean	60.64
Std Dev	1.856

ampl



# B0L002S, U2-ch62, adc6

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry





# B0L002S, U2-ch62, adc7

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L002S, U2-ch63, adc0

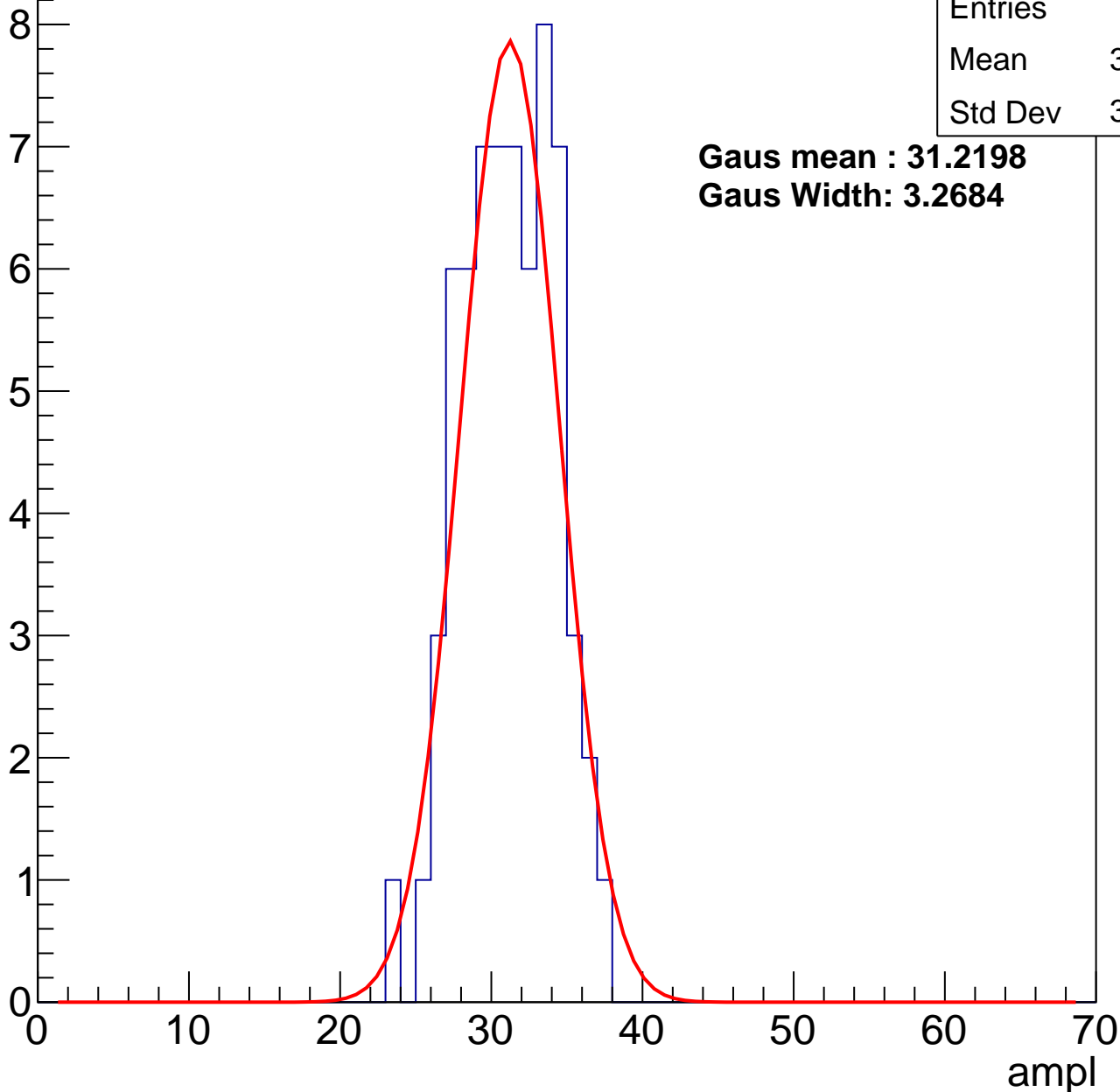
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	65
Mean	30.68
Std Dev	3.008

**Gaus mean : 31.2198**

**Gaus Width: 3.2684**



# B0L002S, U2-ch63, adc1

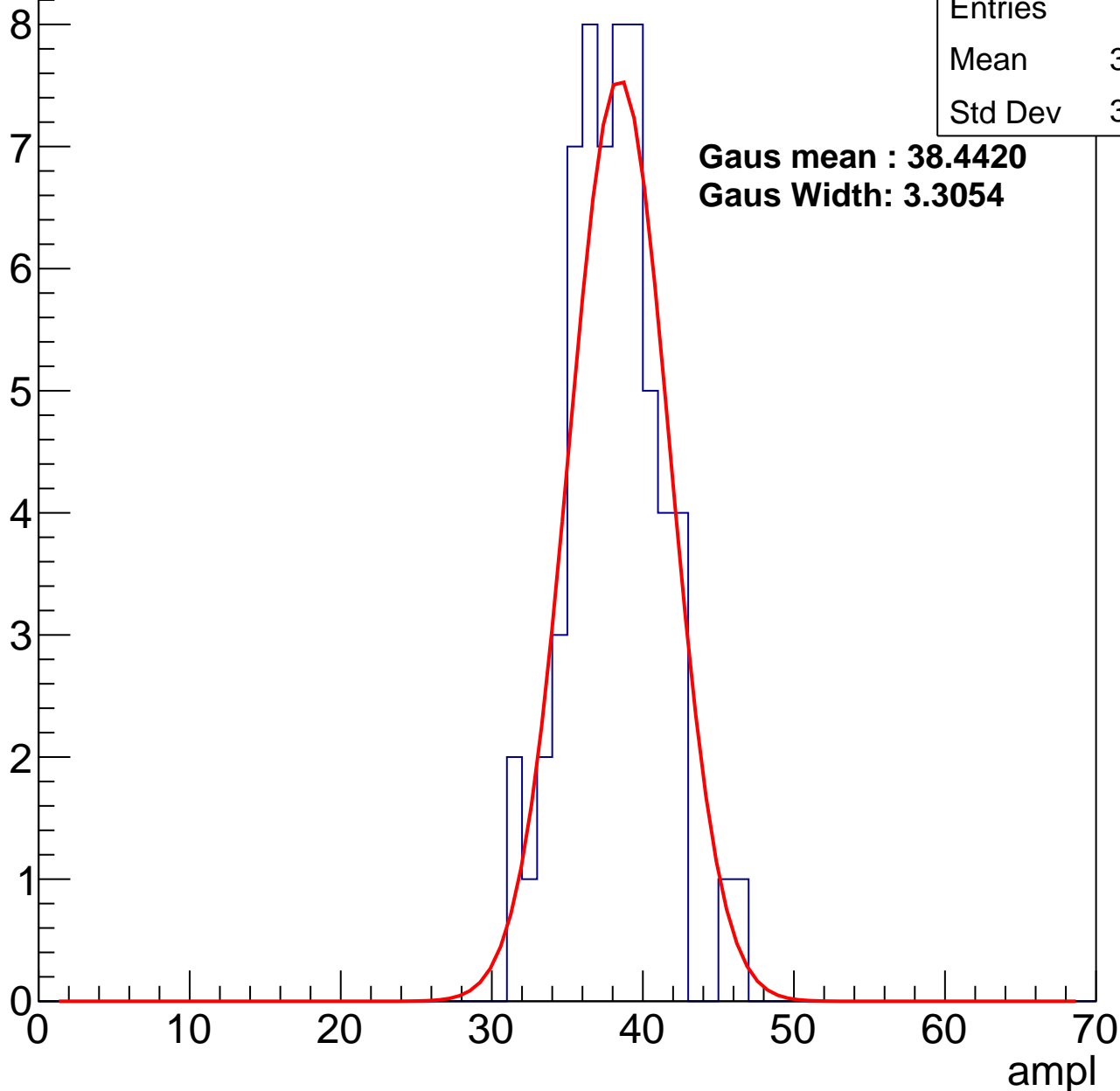
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	61
Mean	37.59
Std Dev	3.043

**Gaus mean : 38.4420**

**Gaus Width: 3.3054**



# B0L002S, U2-ch63, adc2

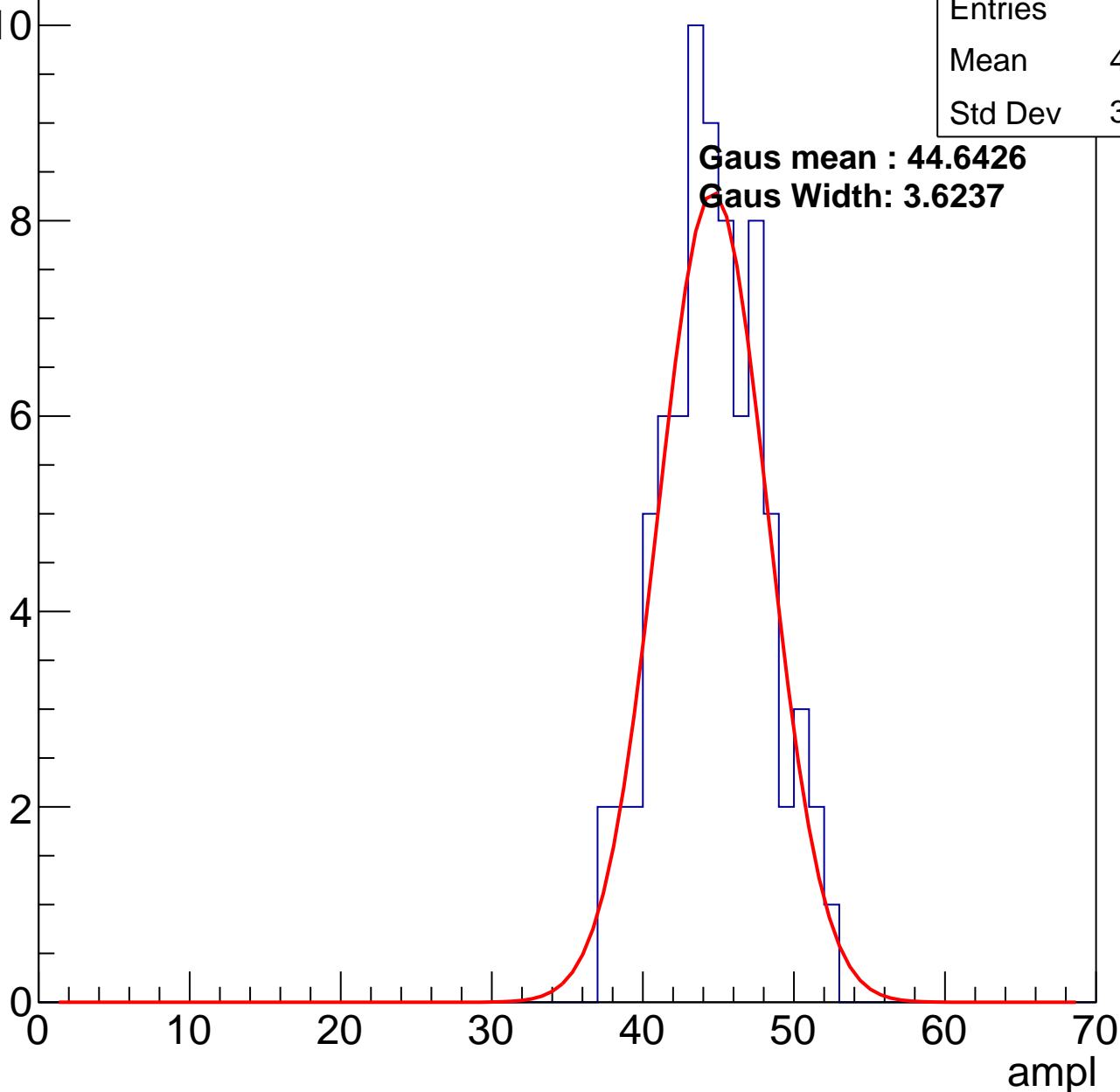
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	77
Mean	44.23
Std Dev	3.396

**Gaus mean : 44.6426**

**Gaus Width: 3.6237**

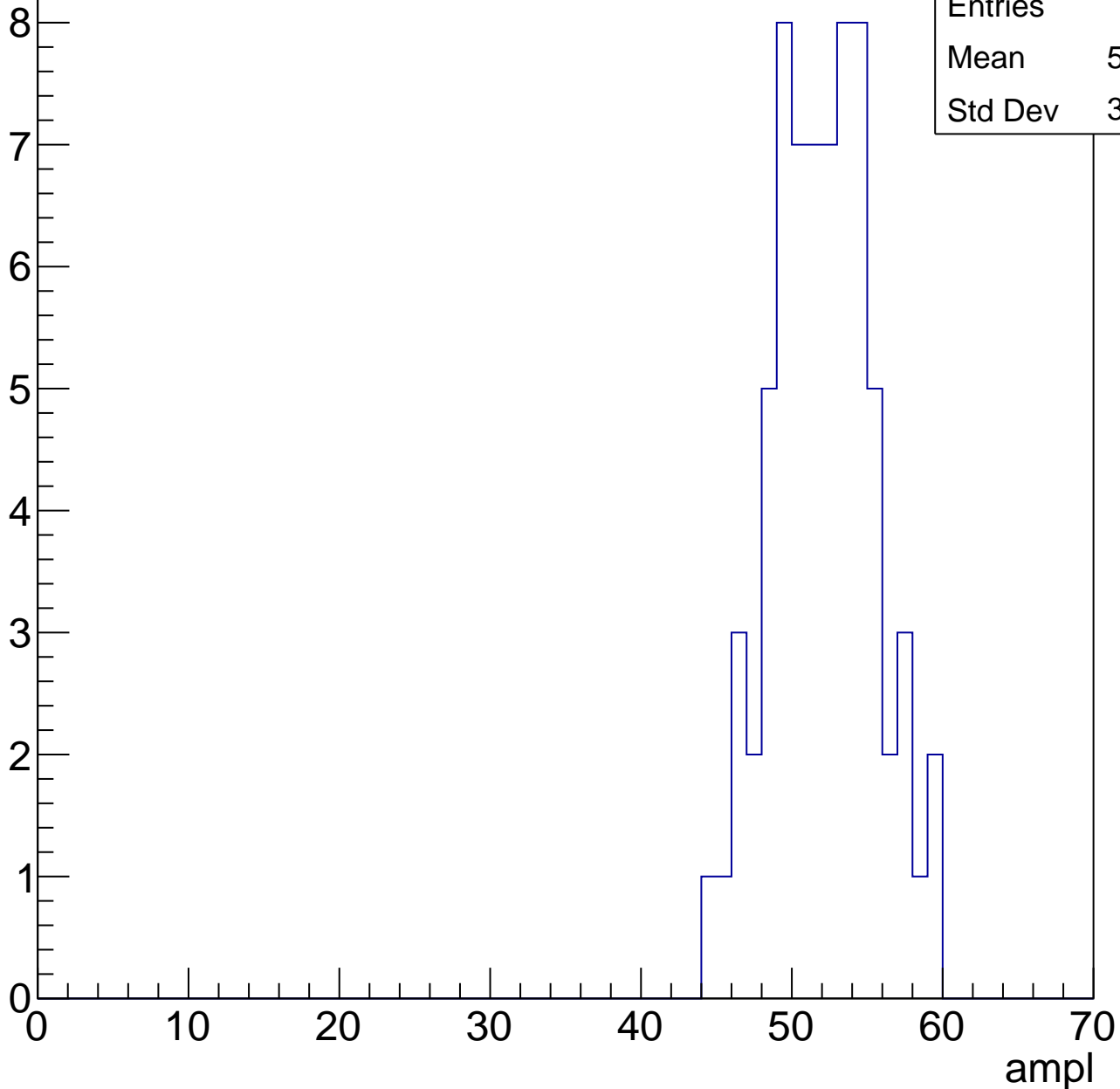


# B0L002S, U2-ch63, adc3

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

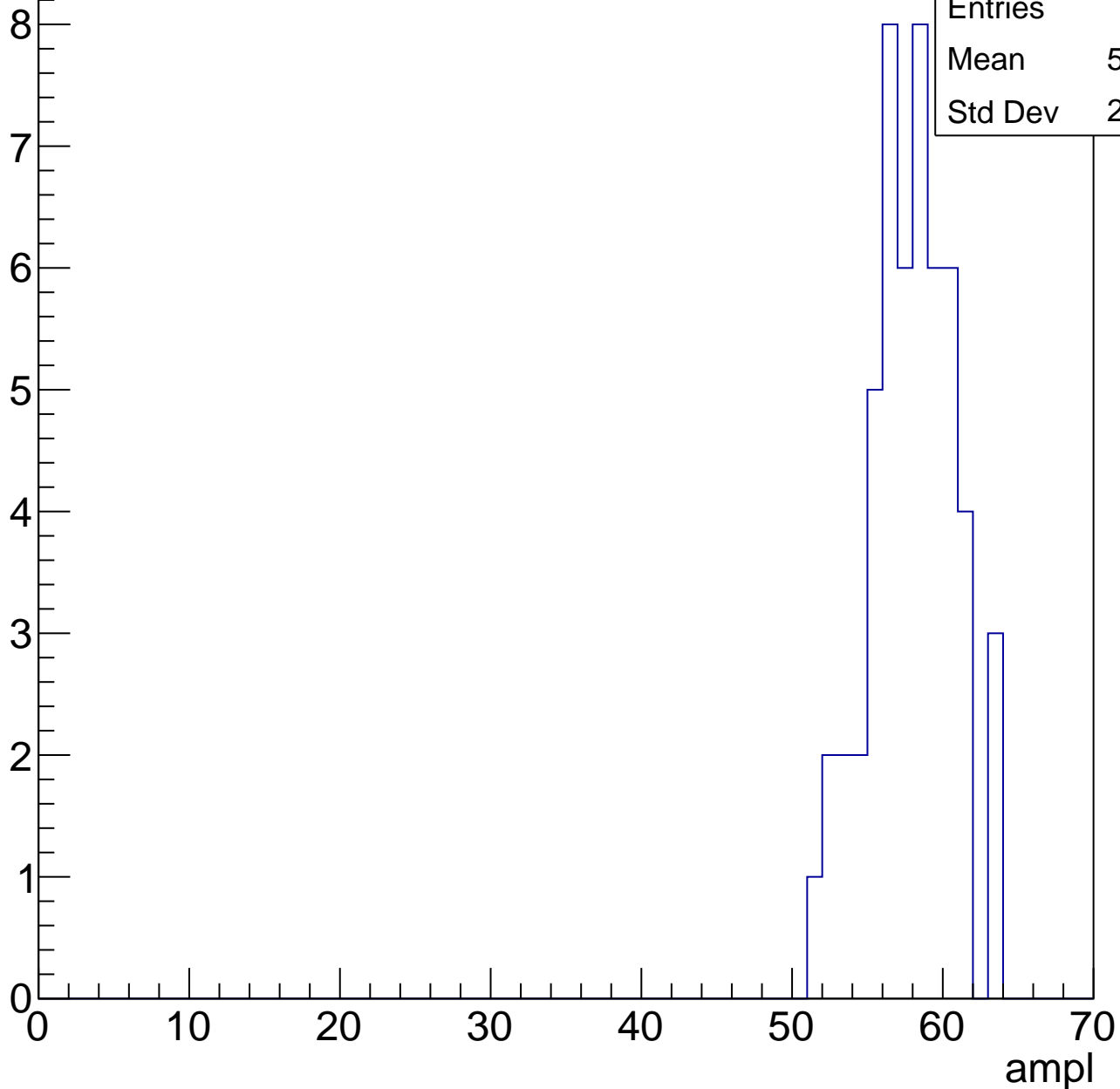
Entries	70
Mean	51.63
Std Dev	3.326



# B0L002S, U2-ch63, adc4

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



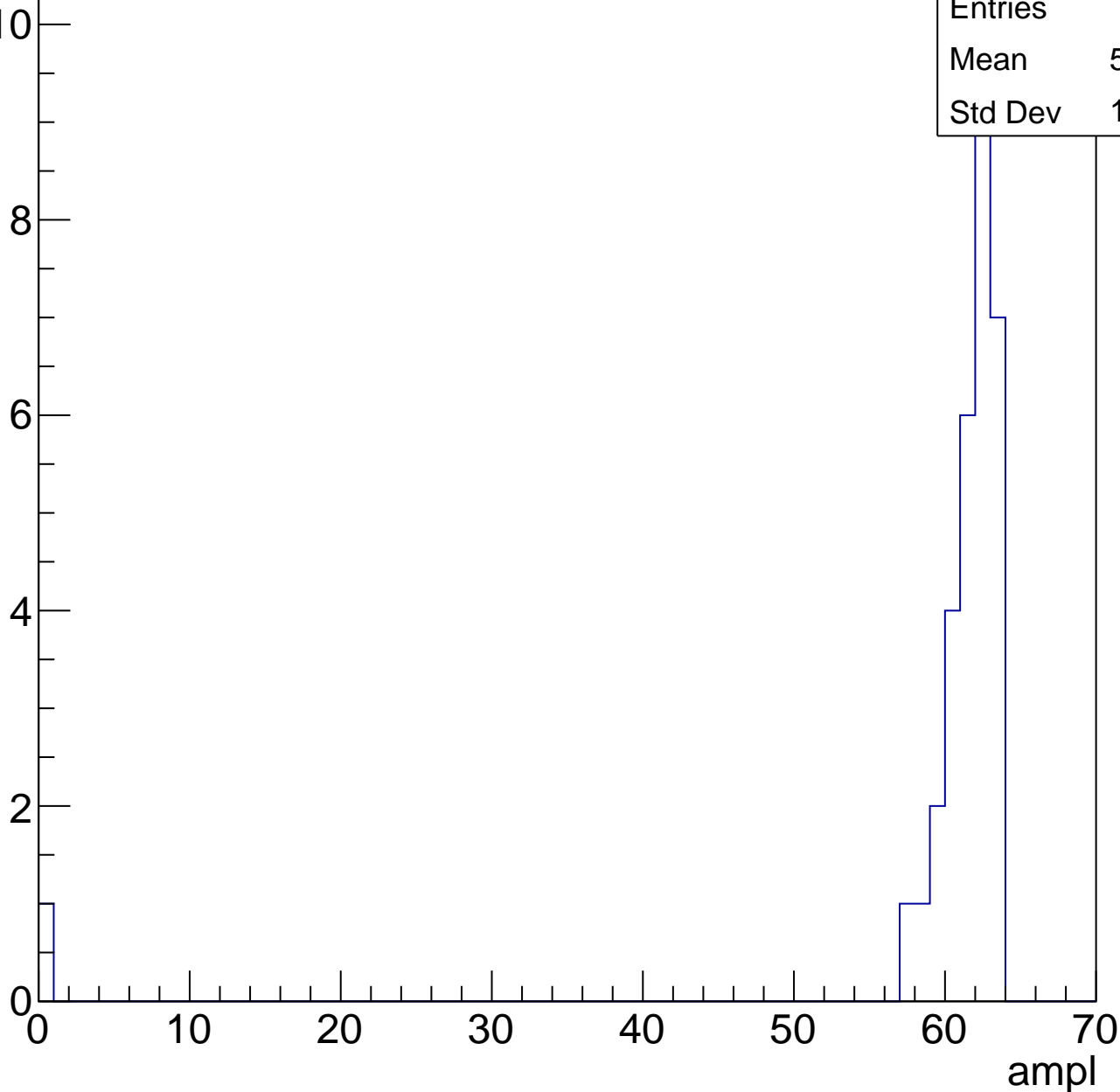
Entries	53
Mean	57.45
Std Dev	2.785

# B0L002S, U2-ch63, adc5

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	32
Mean	59.38
Std Dev	10.77



# B0L002S, U2-ch63, adc6

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



Entries	0
Mean	0
Std Dev	0



# B0L002S, U2-ch63, adc7

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



# B0L002S, U2-ch64, adc0

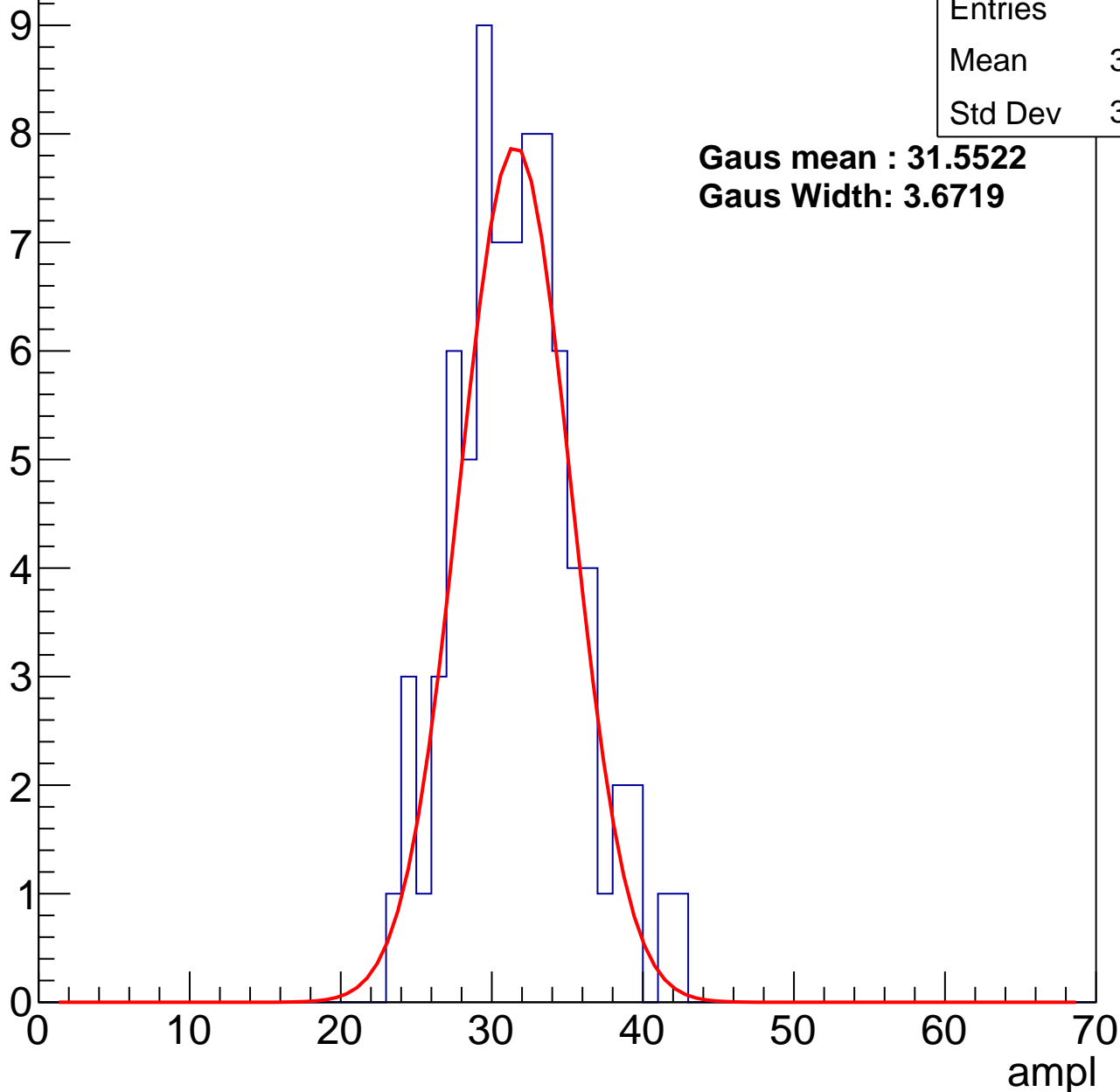
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	79
Mean	31.27
Std Dev	3.964

**Gaus mean : 31.5522**

**Gaus Width: 3.6719**



# B0L002S, U2-ch64, adc1

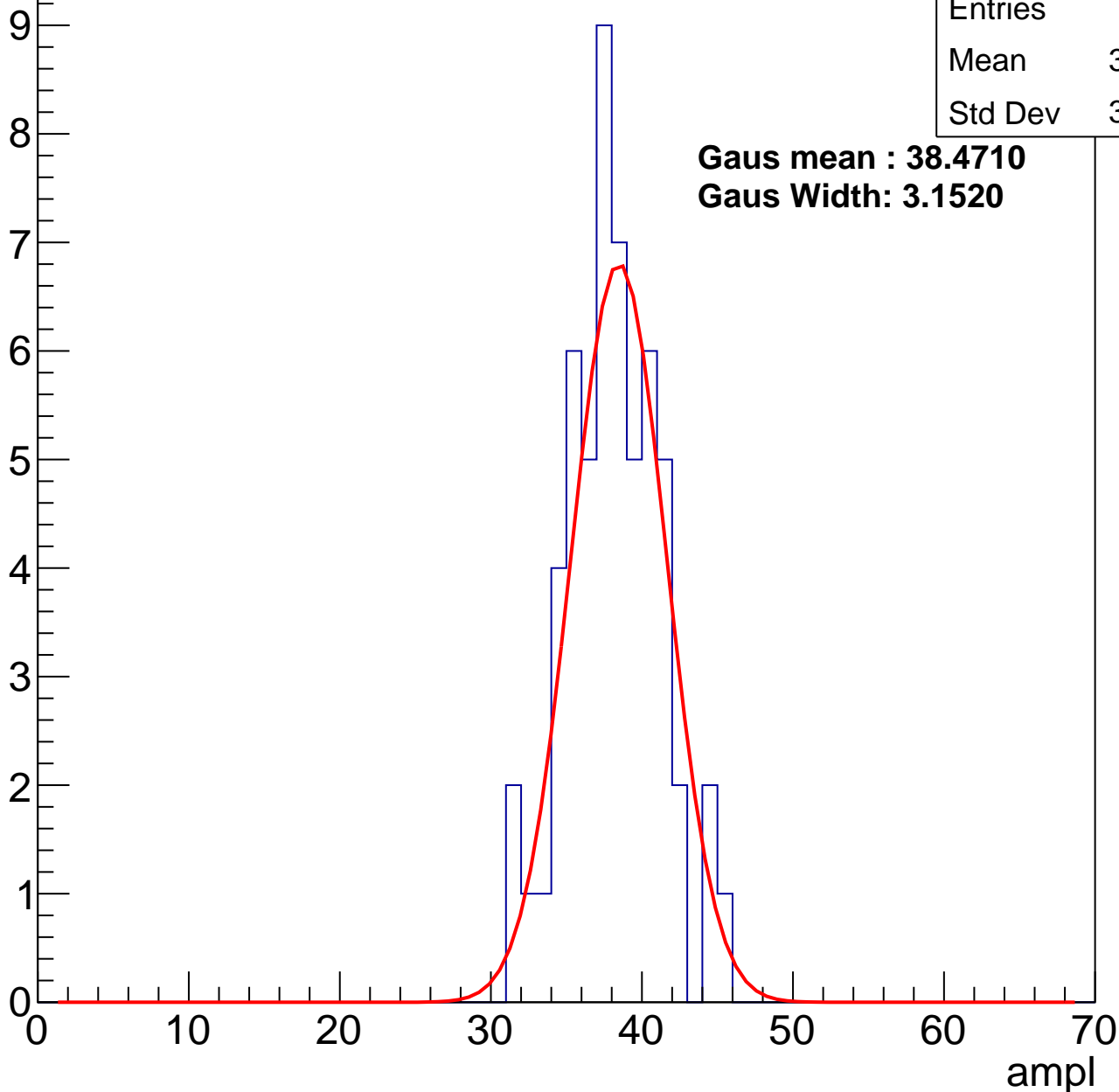
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	56
Mean	37.66
Std Dev	3.066

**Gaus mean : 38.4710**

**Gaus Width: 3.1520**



# B0L002S, U2-ch64, adc2

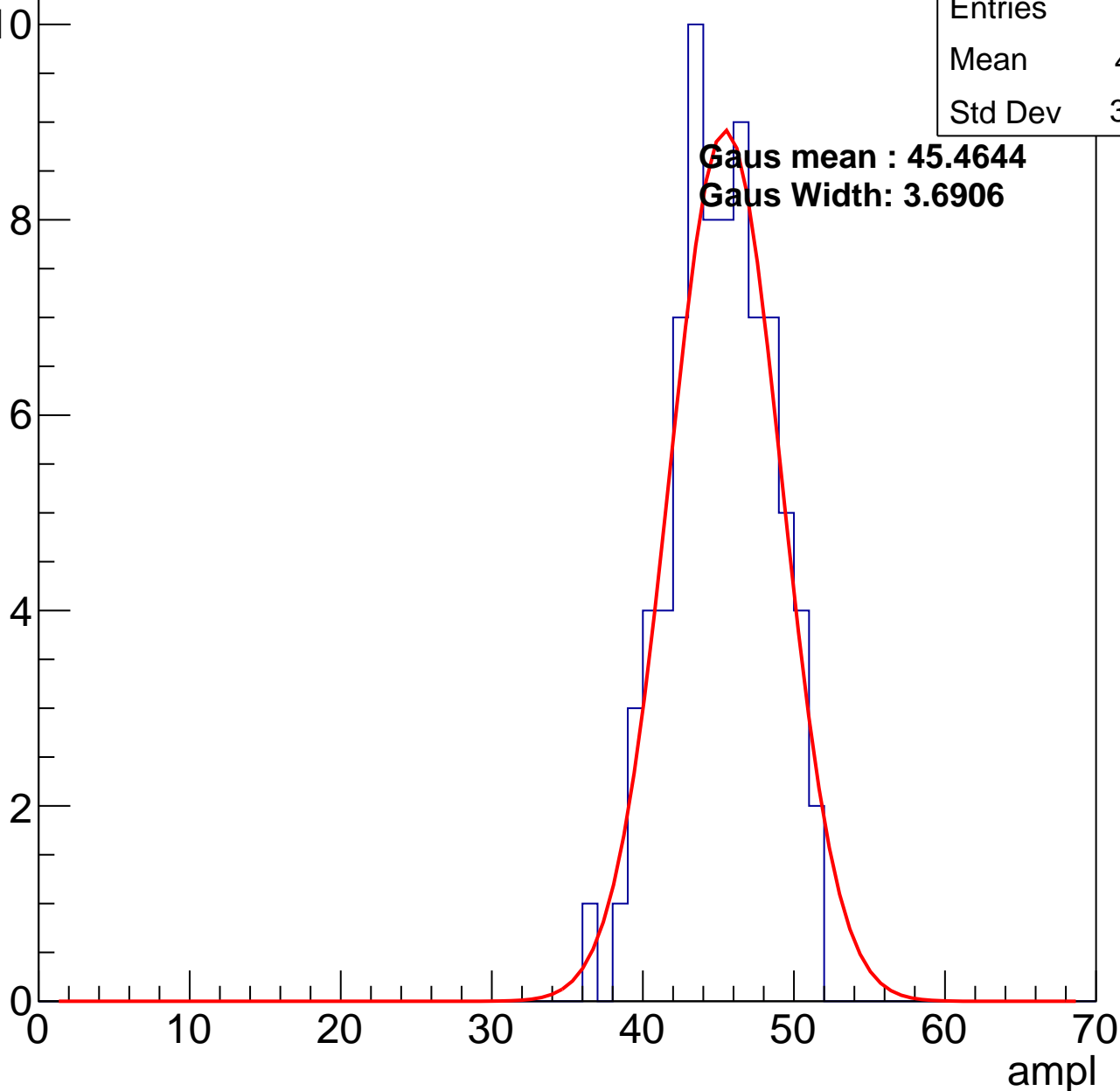
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	80
Mean	44.71
Std Dev	3.276

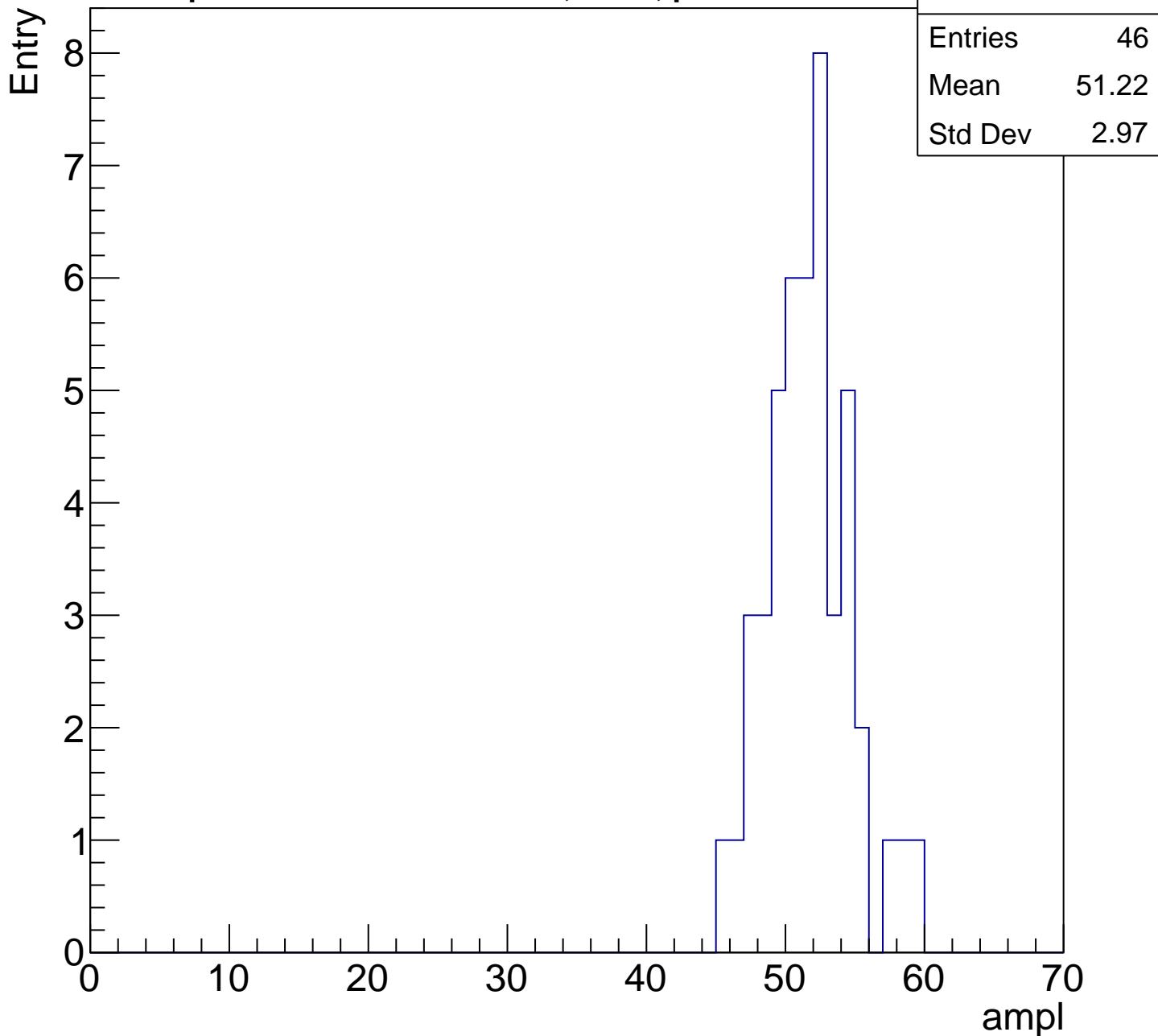
**Gaus mean : 45.4644**

**Gaus Width: 3.6906**



# B0L002S, U2-ch64, adc3

calib\_packv5\_042523\_0143.root, FC#8, port C1



# B0L002S, U2-ch64, adc4

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

7

6

5

4

3

2

1

0

Entries 57

Mean 56.39

Std Dev 2.77

0

10

20

30

40

50

ampl

60

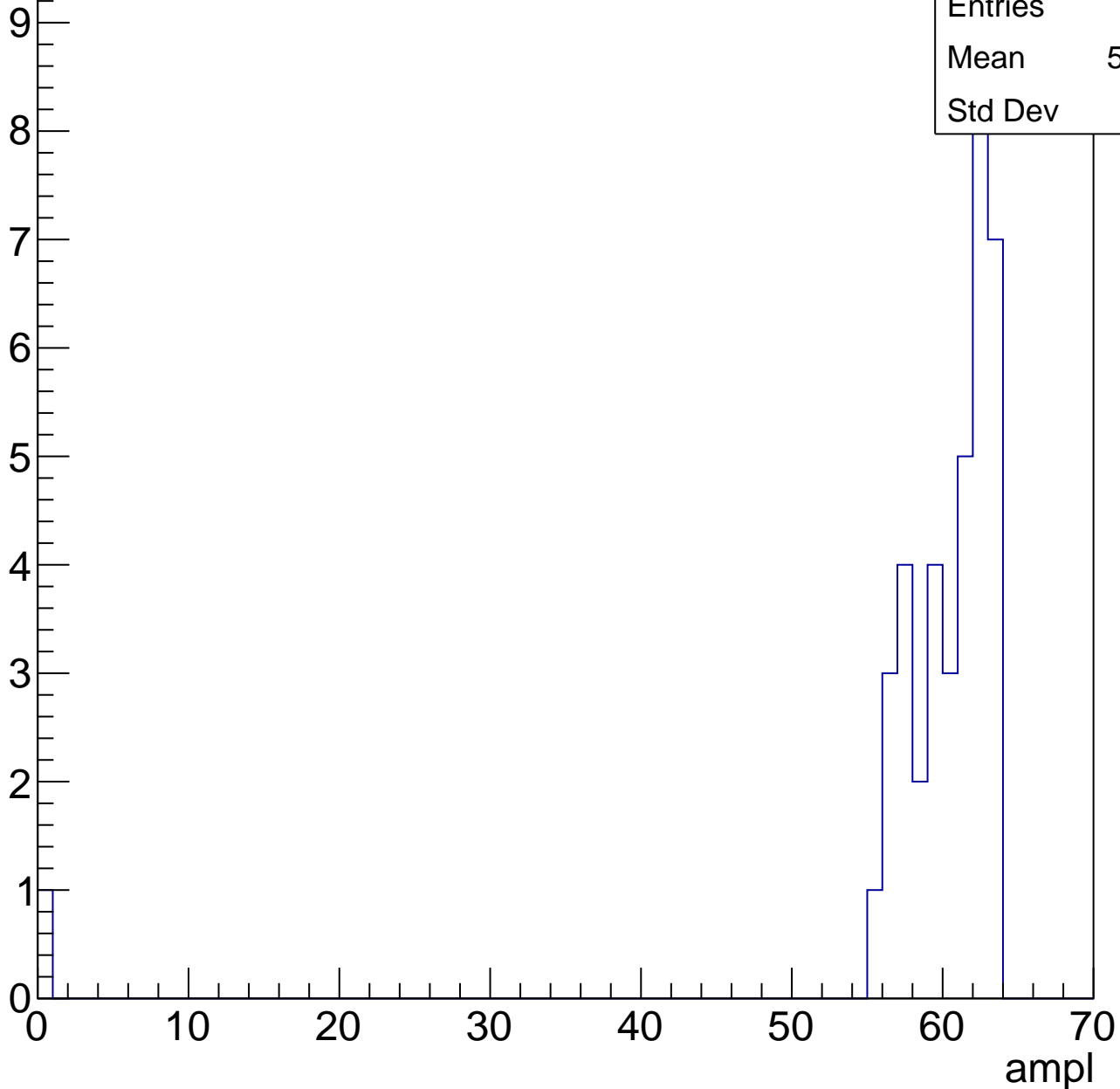
70

# B0L002S, U2-ch64, adc5

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	39
Mean	58.64
Std Dev	9.81



# B0L002S, U2-ch64, adc6

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry





# B0L002S, U2-ch64, adc7

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



# B0L002S, U2-ch65, adc0

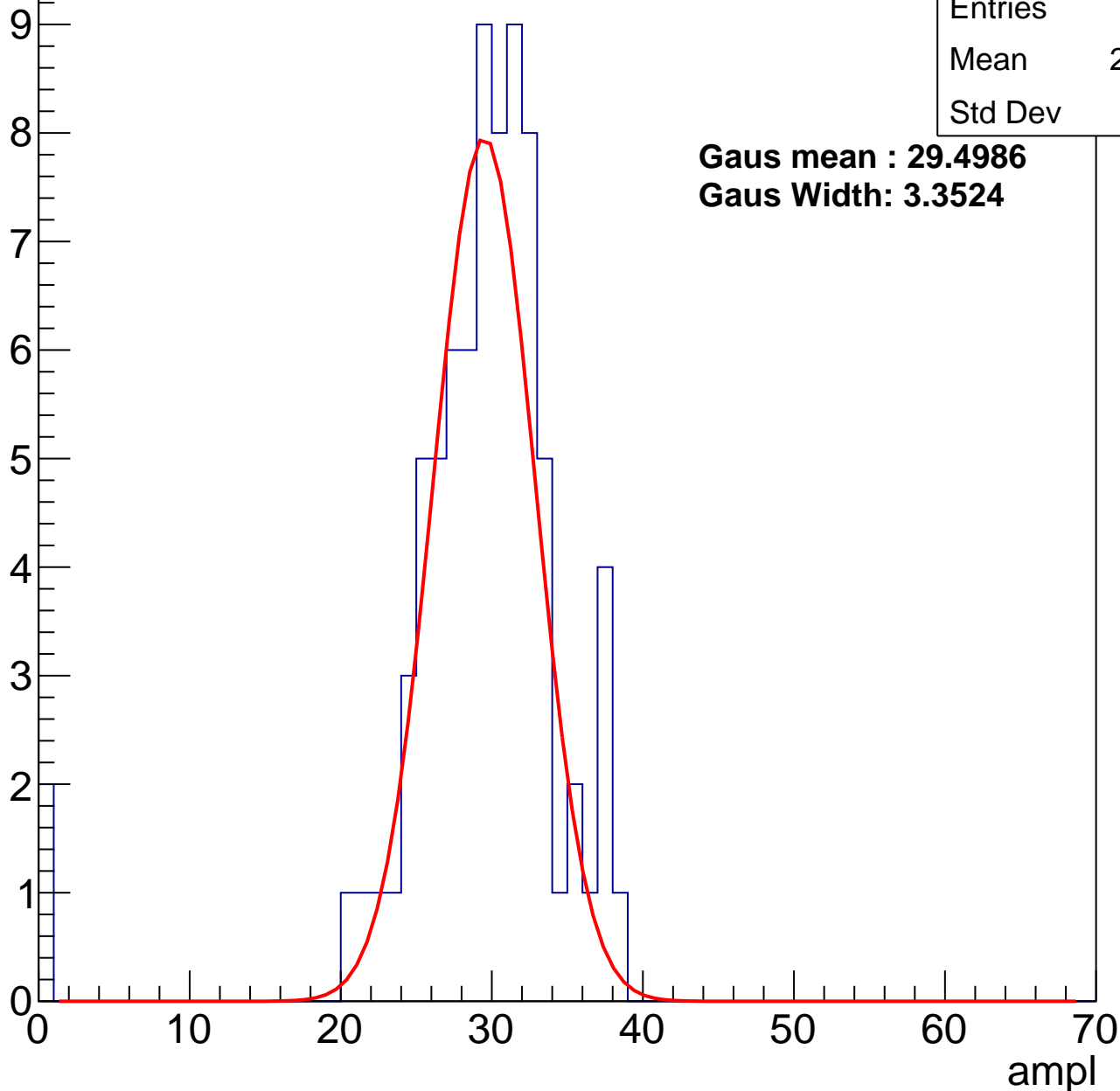
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	79
Mean	28.73
Std Dev	5.97

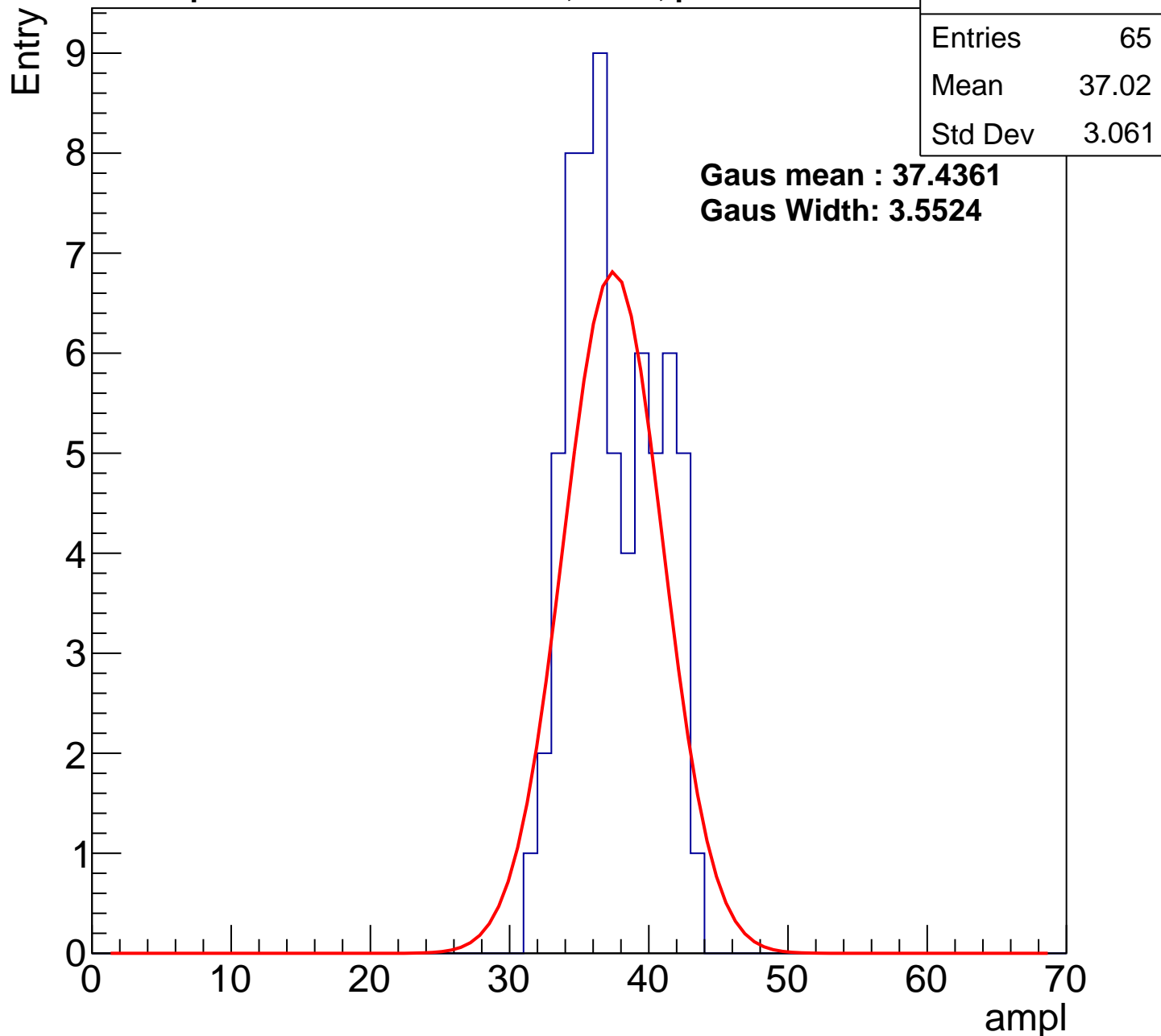
**Gaus mean : 29.4986**

**Gaus Width: 3.3524**



# B0L002S, U2-ch65, adc1

calib\_packv5\_042523\_0143.root, FC#8, port C1



# B0L002S, U2-ch65, adc2

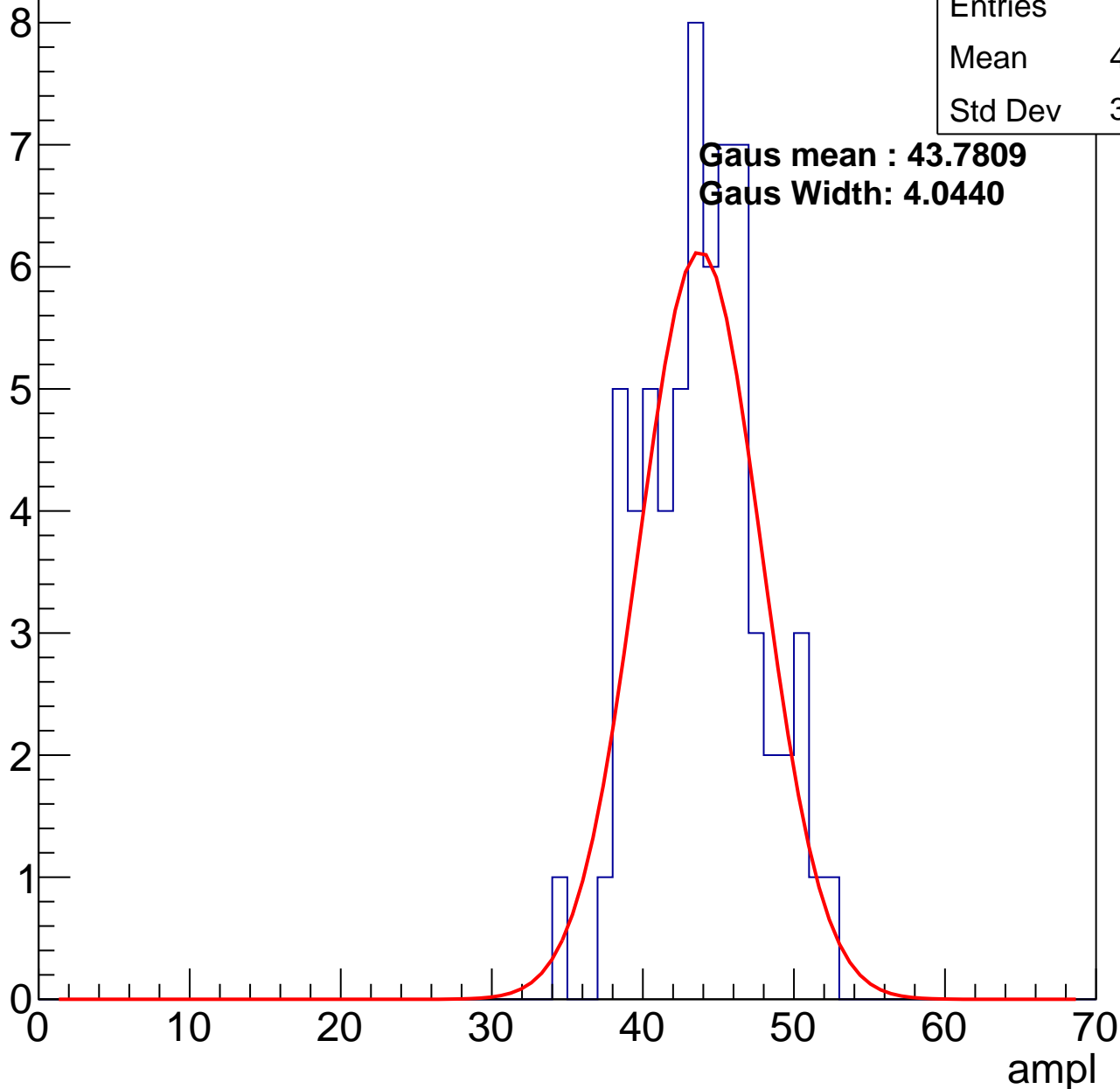
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	65
Mean	43.45
Std Dev	3.758

**Gaus mean : 43.7809**

**Gaus Width: 4.0440**

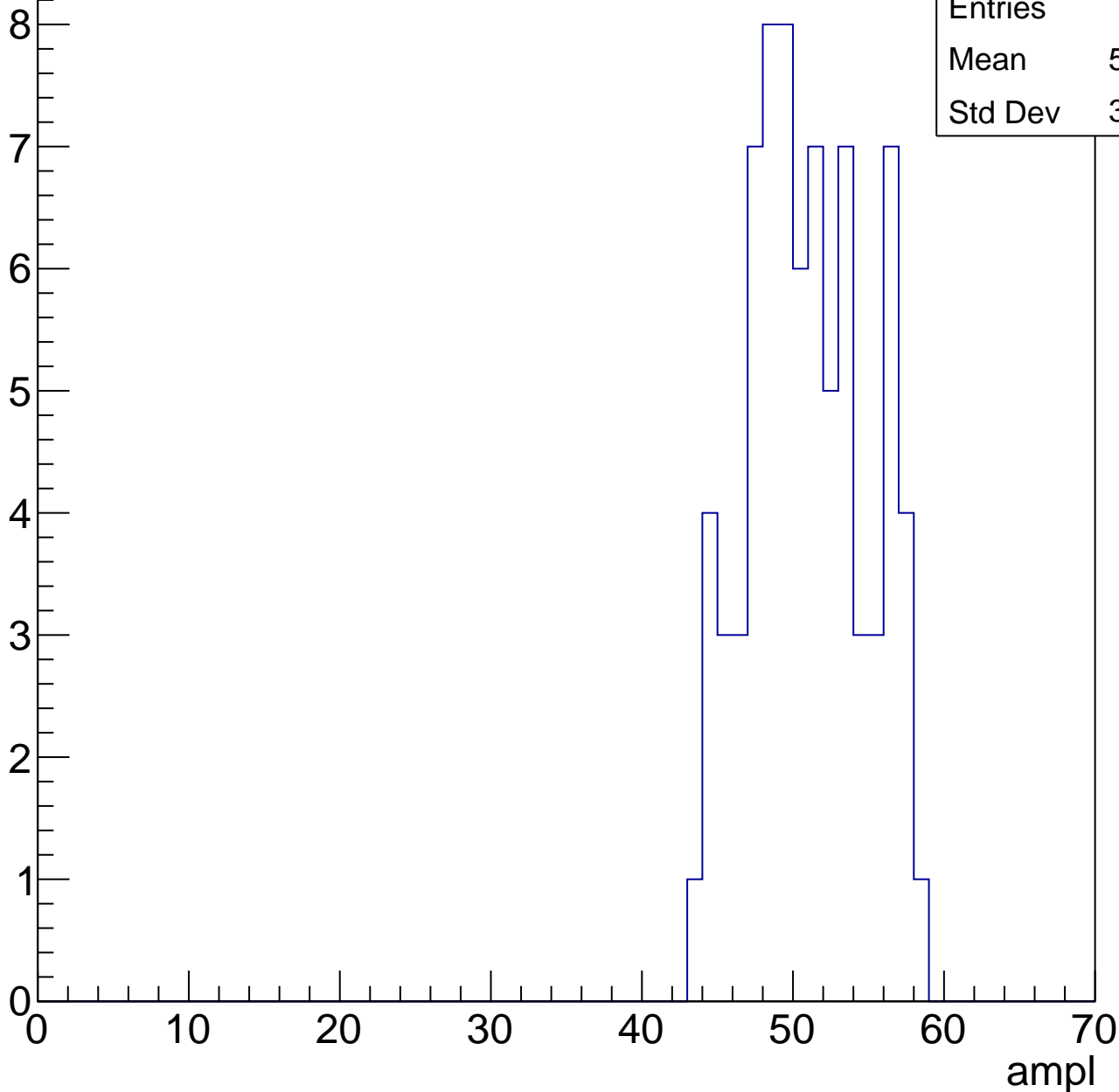


# B0L002S, U2-ch65, adc3

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

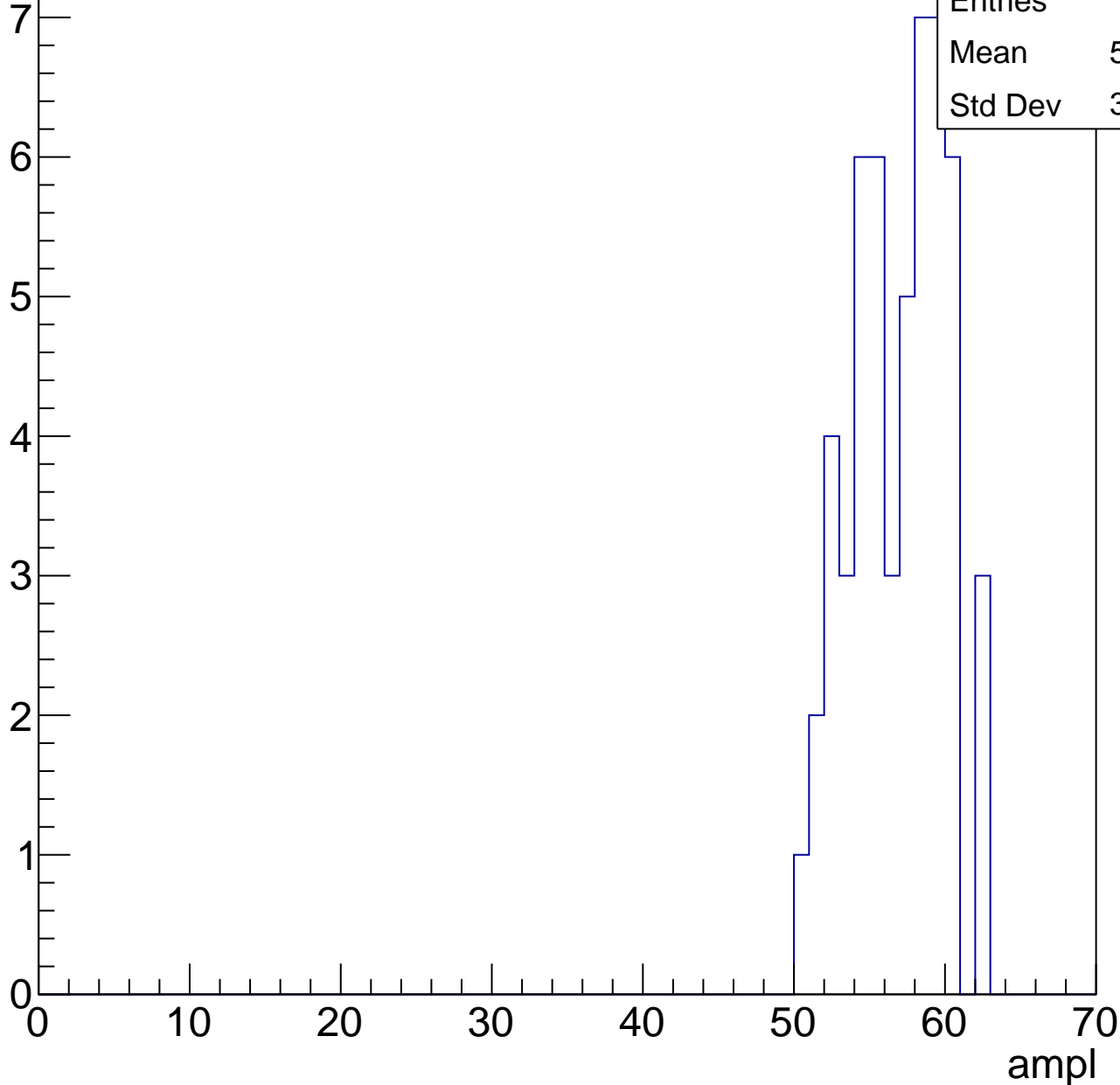
Entries	77
Mean	50.52
Std Dev	3.819



# B0L002S, U2-ch65, adc4

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

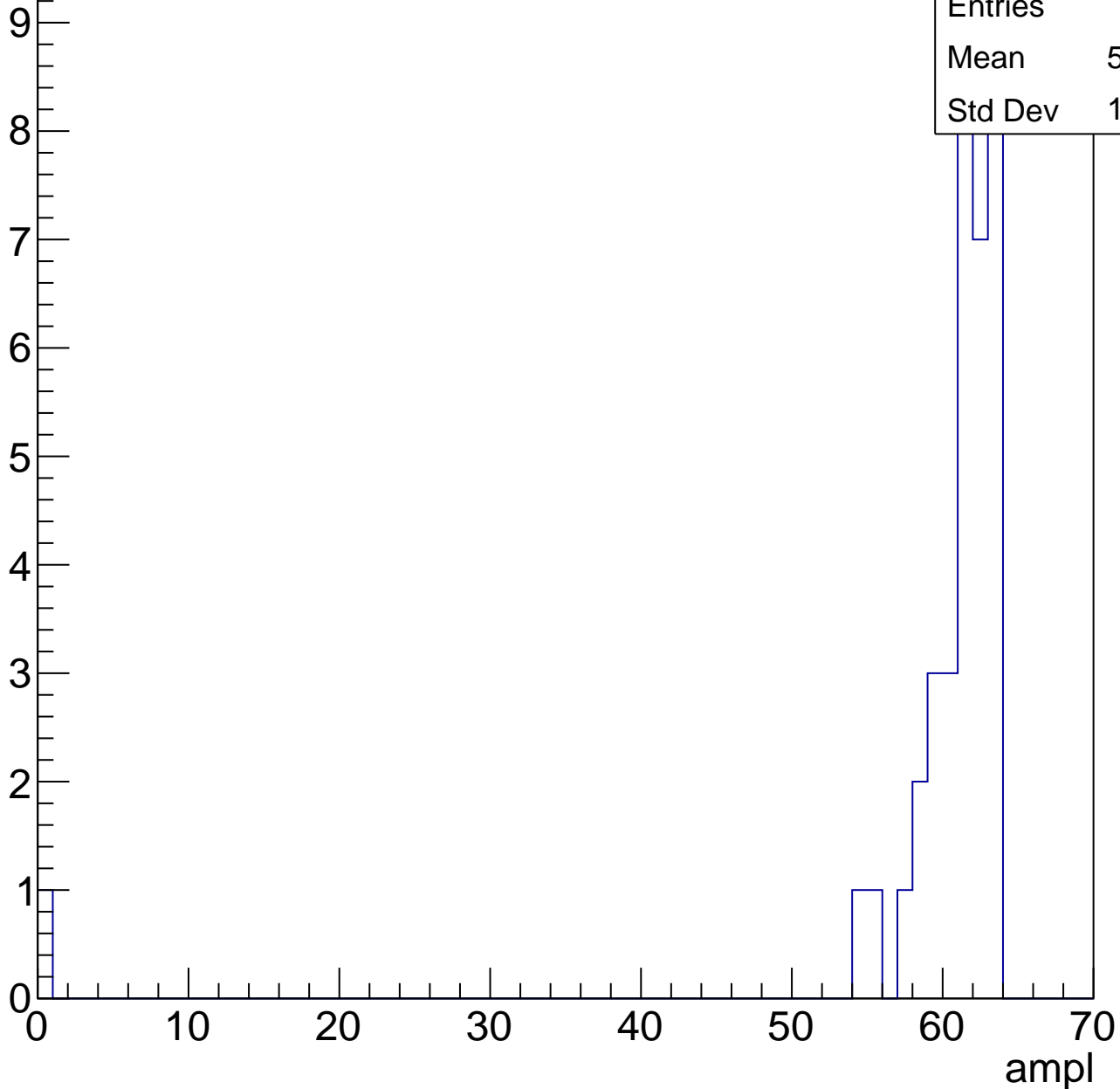


# B0L002S, U2-ch65, adc5

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	36
Mean	59.06
Std Dev	10.22



# B0L002S, U2-ch65, adc6

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	4
Mean	61.75
Std Dev	1.299

0 10 20 30 40 50 60 70

ampl

0

1

2

3

4

5

6

7

8

9

10

11

12

13

14

15

16

17

18

19

20

21

22

23

24

25

26

27

28

29

30

31

32

33

34

35

36

37

38

39

40

41

42

43

44

45

46

47

48

49

50

51

52

53

54

55

56

57

58

59

60

61

62

63

64

65

66

67

68

69

70



# B0L002S, U2-ch65, adc7

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



# B0L002S, U2-ch66, adc0

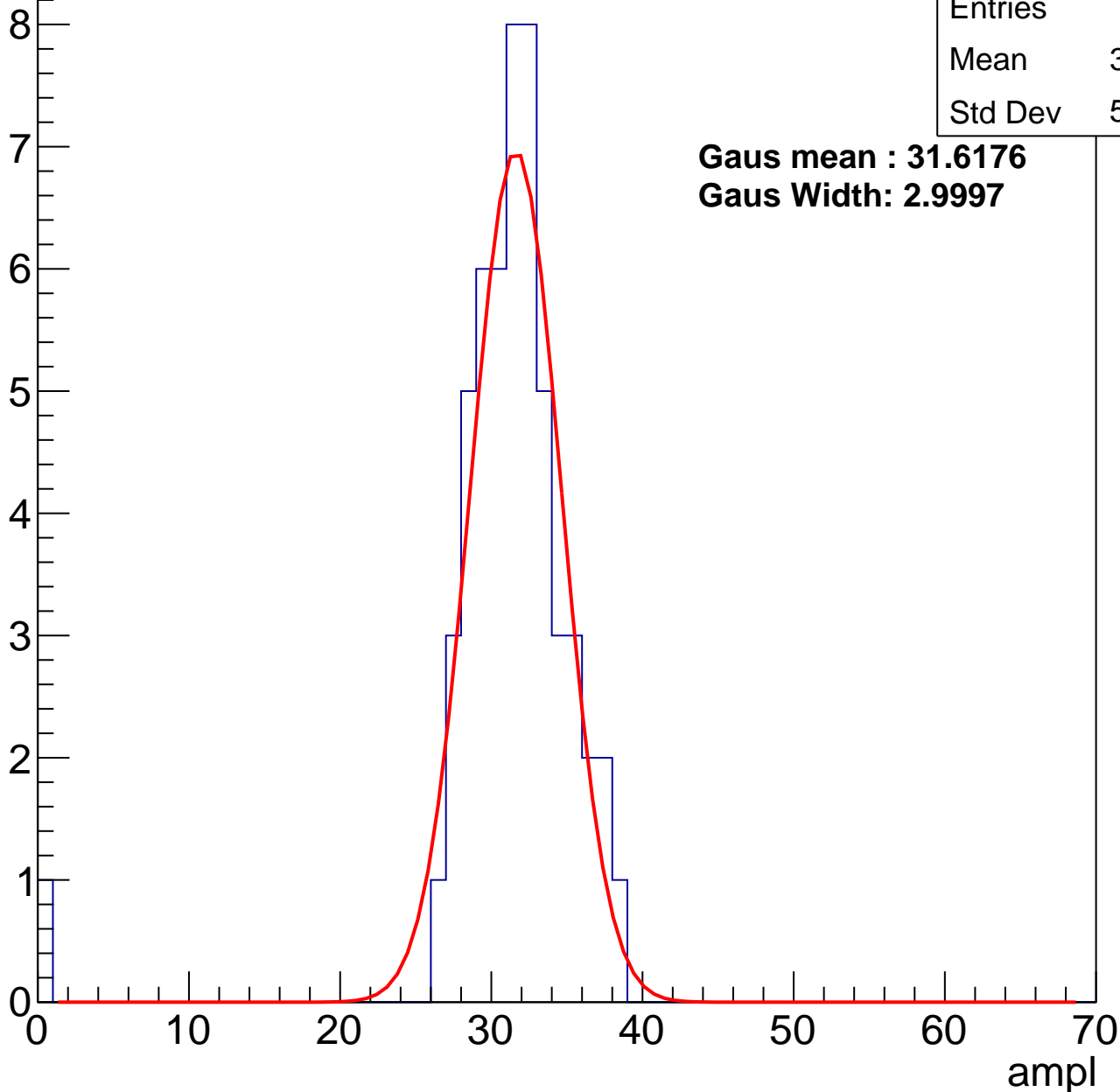
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	54
Mean	30.76
Std Dev	5.055

**Gaus mean : 31.6176**

**Gaus Width: 2.9997**



# B0L002S, U2-ch66, adc1

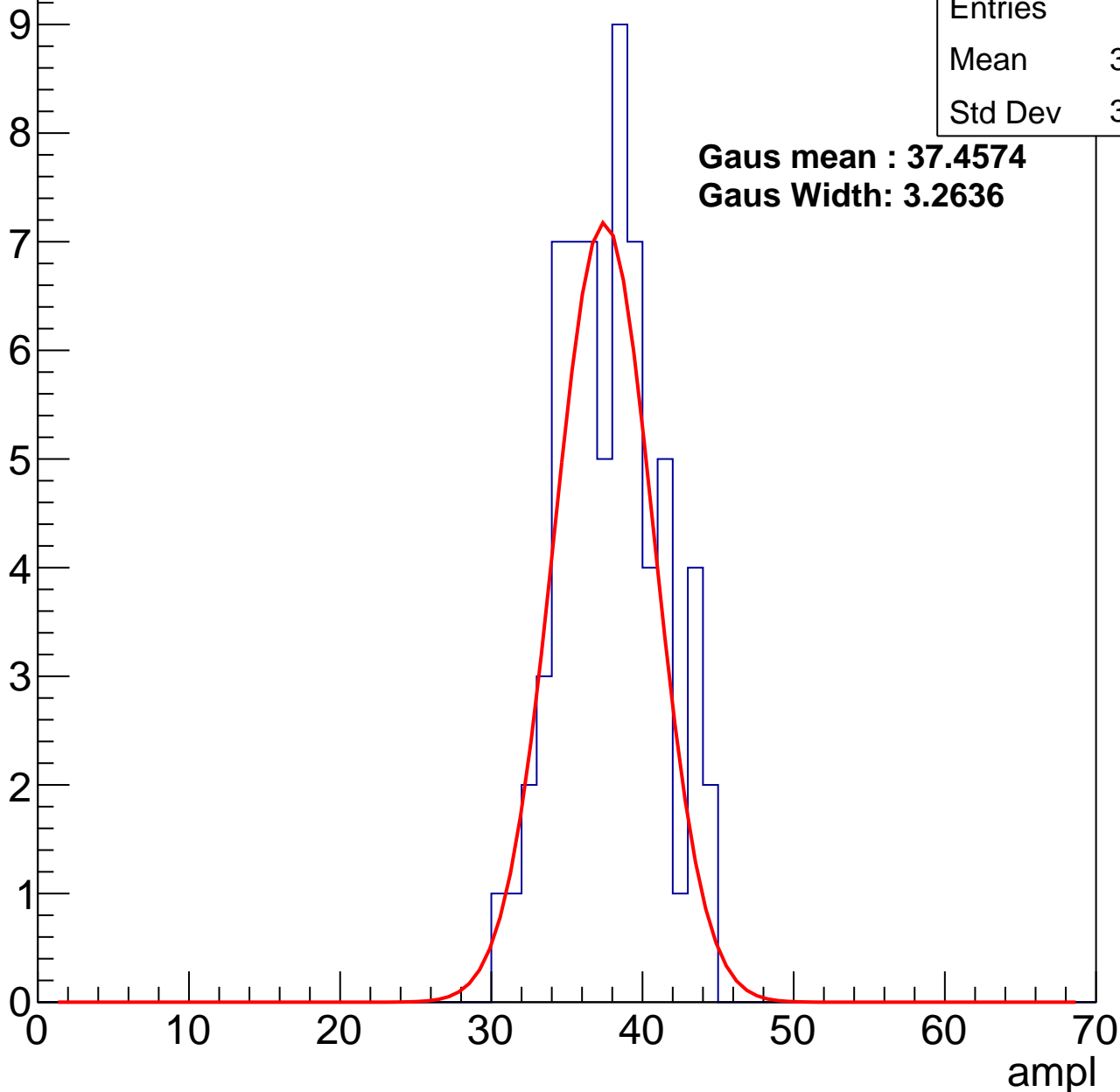
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	65
Mean	37.32
Std Dev	3.268

**Gaus mean : 37.4574**

**Gaus Width: 3.2636**



# B0L002S, U2-ch66, adc2

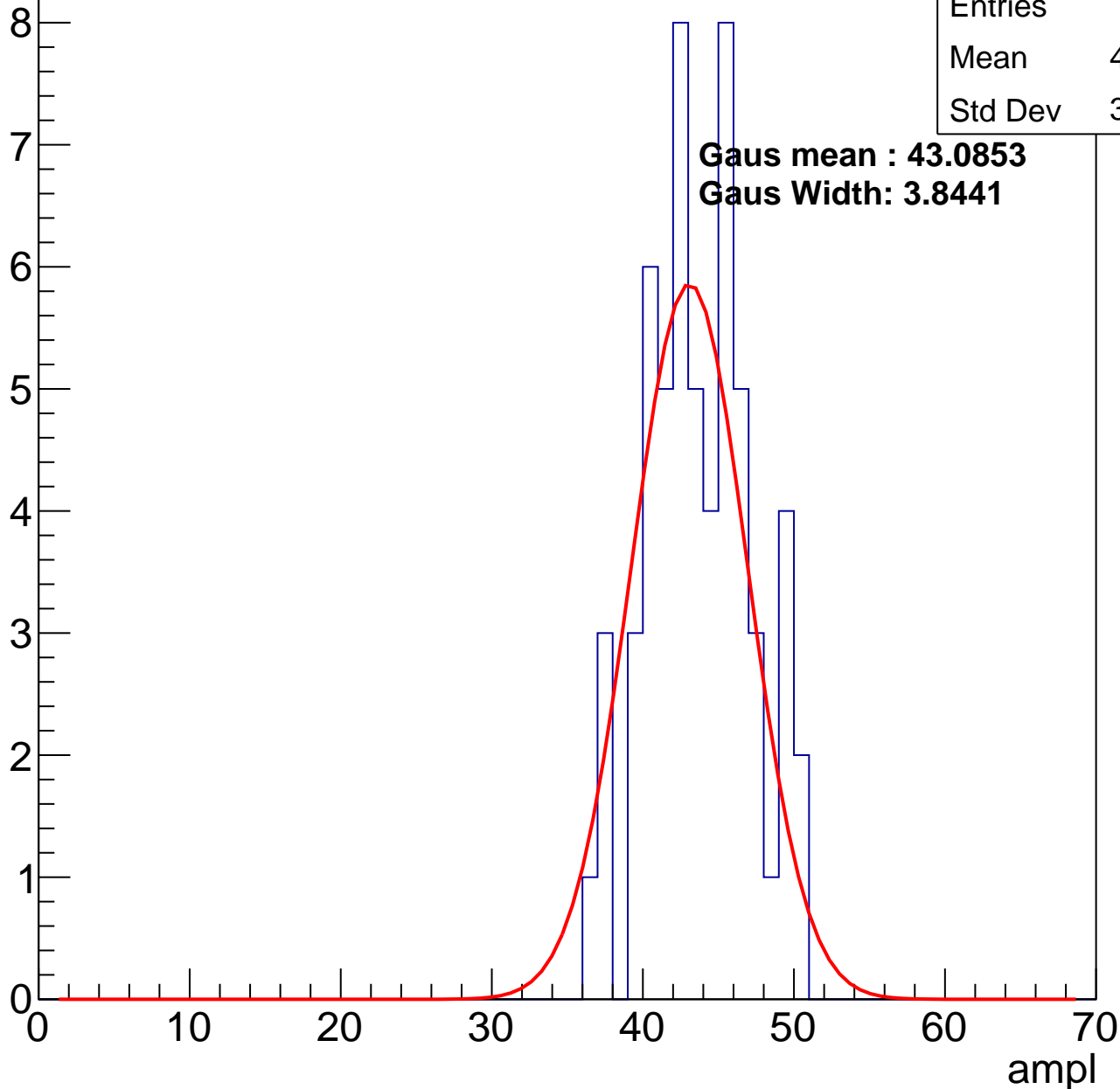
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	58
Mean	43.29
Std Dev	3.419

**Gaus mean : 43.0853**

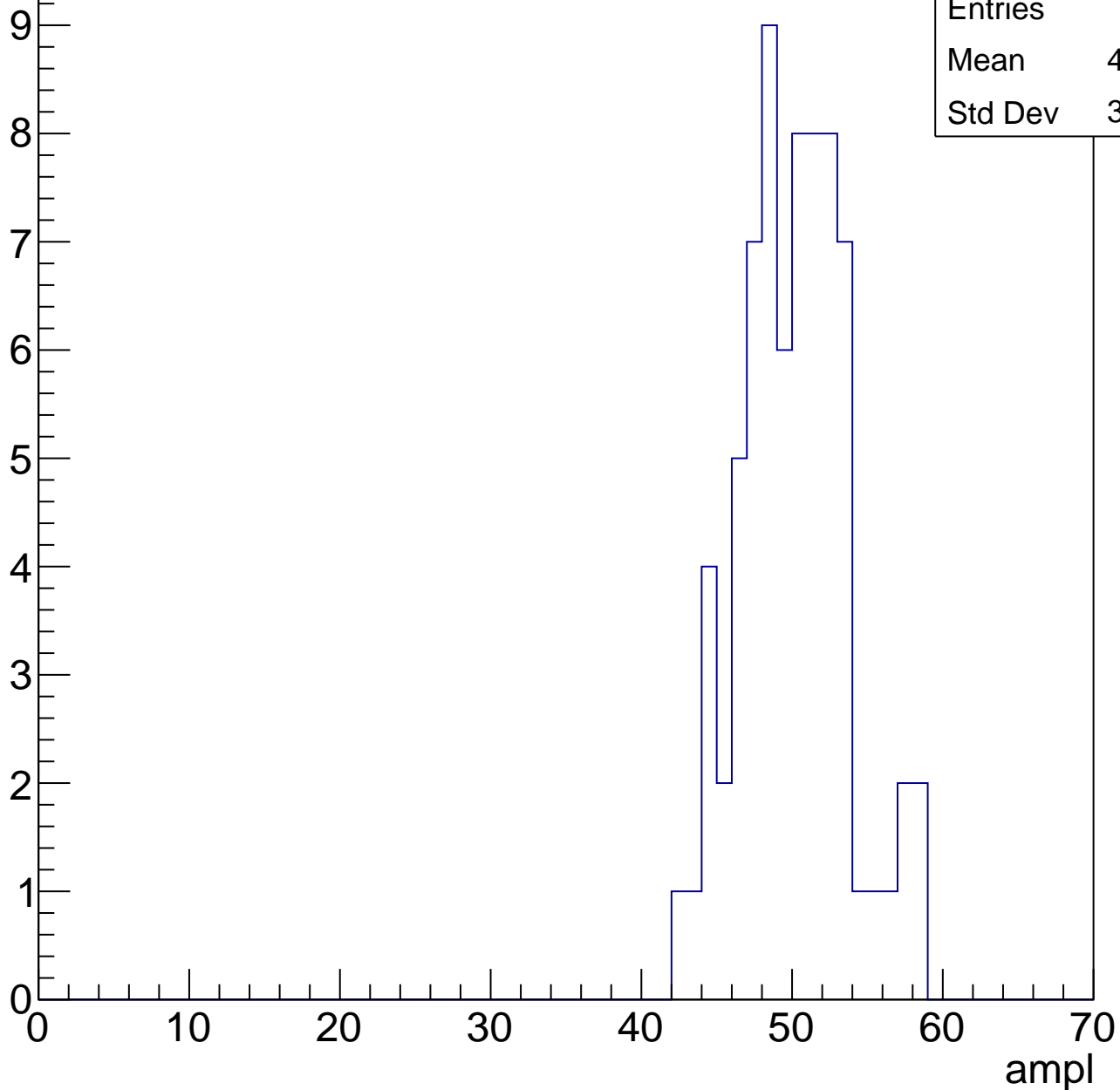
**Gaus Width: 3.8441**



# B0L002S, U2-ch66, adc3

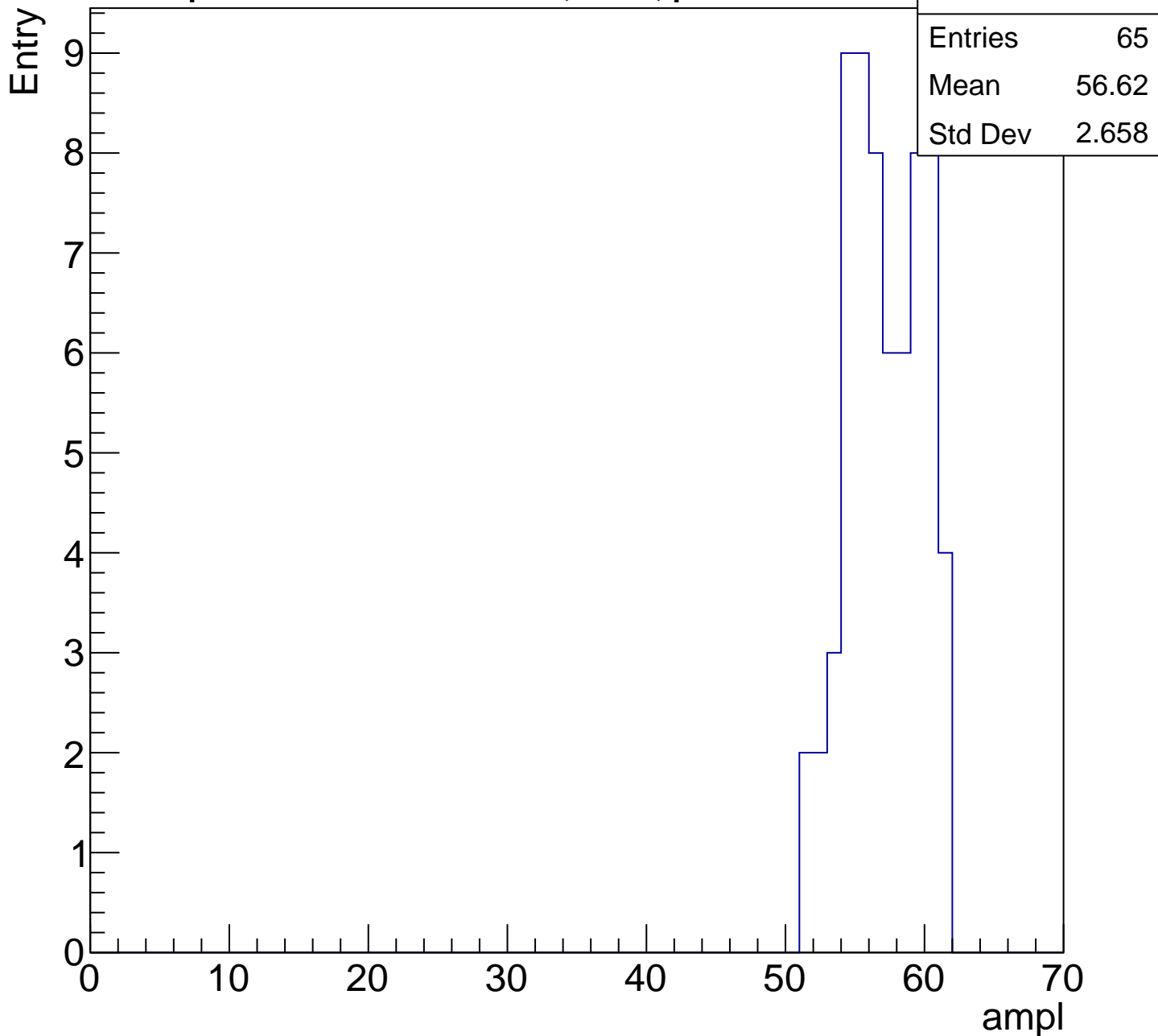
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



# B0L002S, U2-ch66, adc4

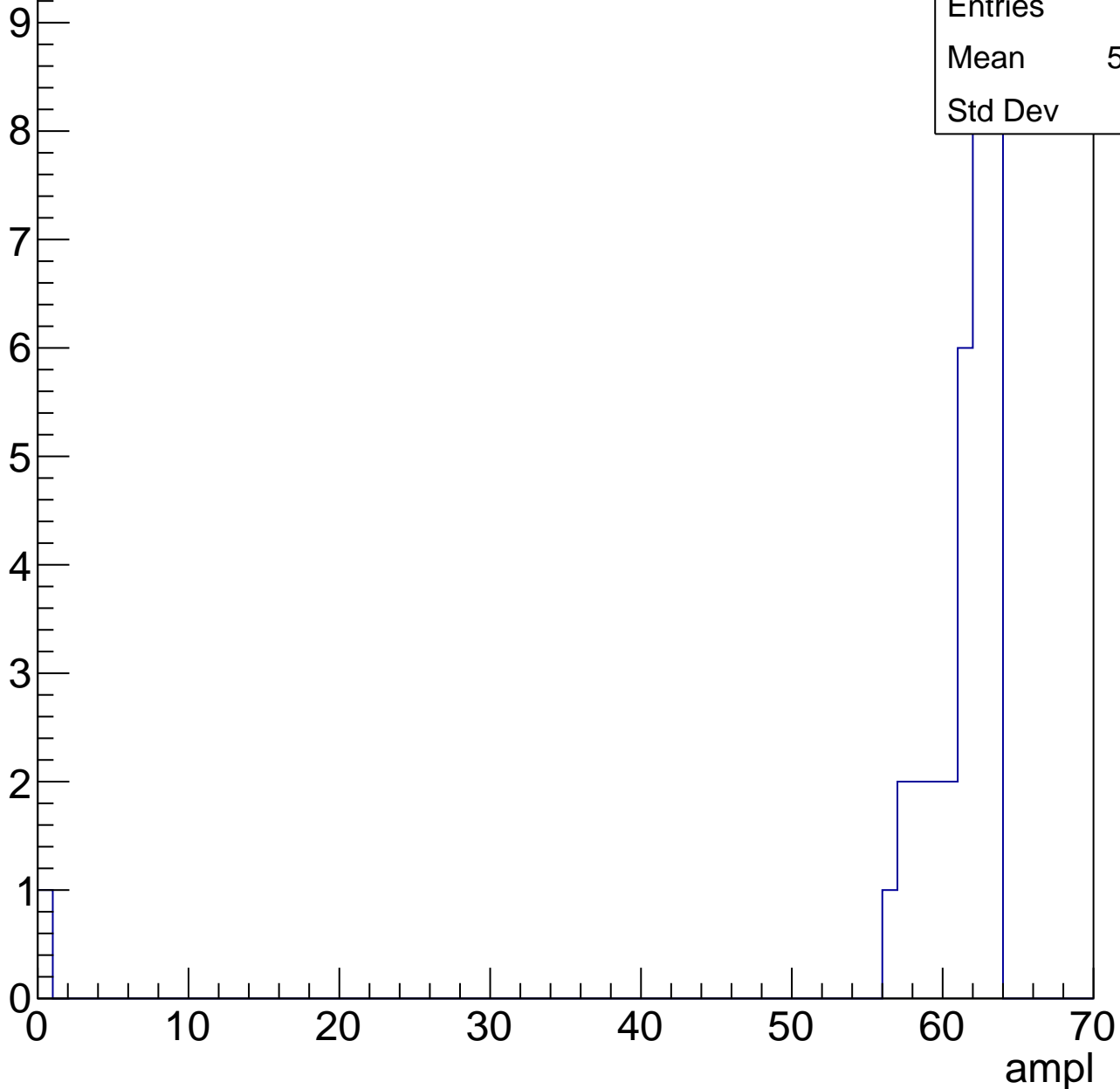
calib\_packv5\_042523\_0143.root, FC#8, port C1



# B0L002S, U2-ch66, adc5

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



# B0L002S, U2-ch66, adc6

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry





# B0L002S, U2-ch66, adc7

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L002S, U2-ch67, adc0

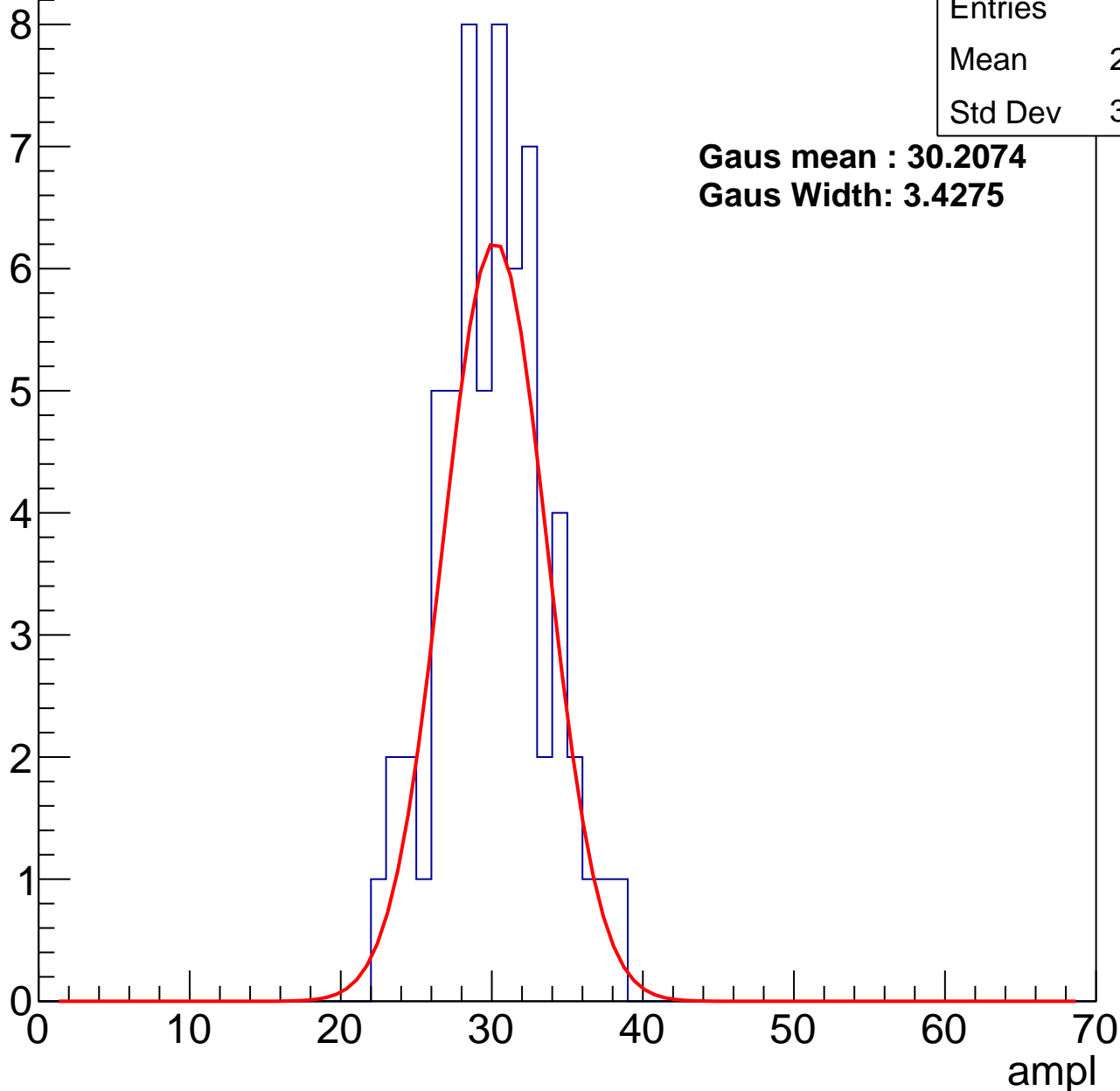
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	61
Mean	29.64
Std Dev	3.455

**Gaus mean : 30.2074**

**Gaus Width: 3.4275**



# B0L002S, U2-ch67, adc1

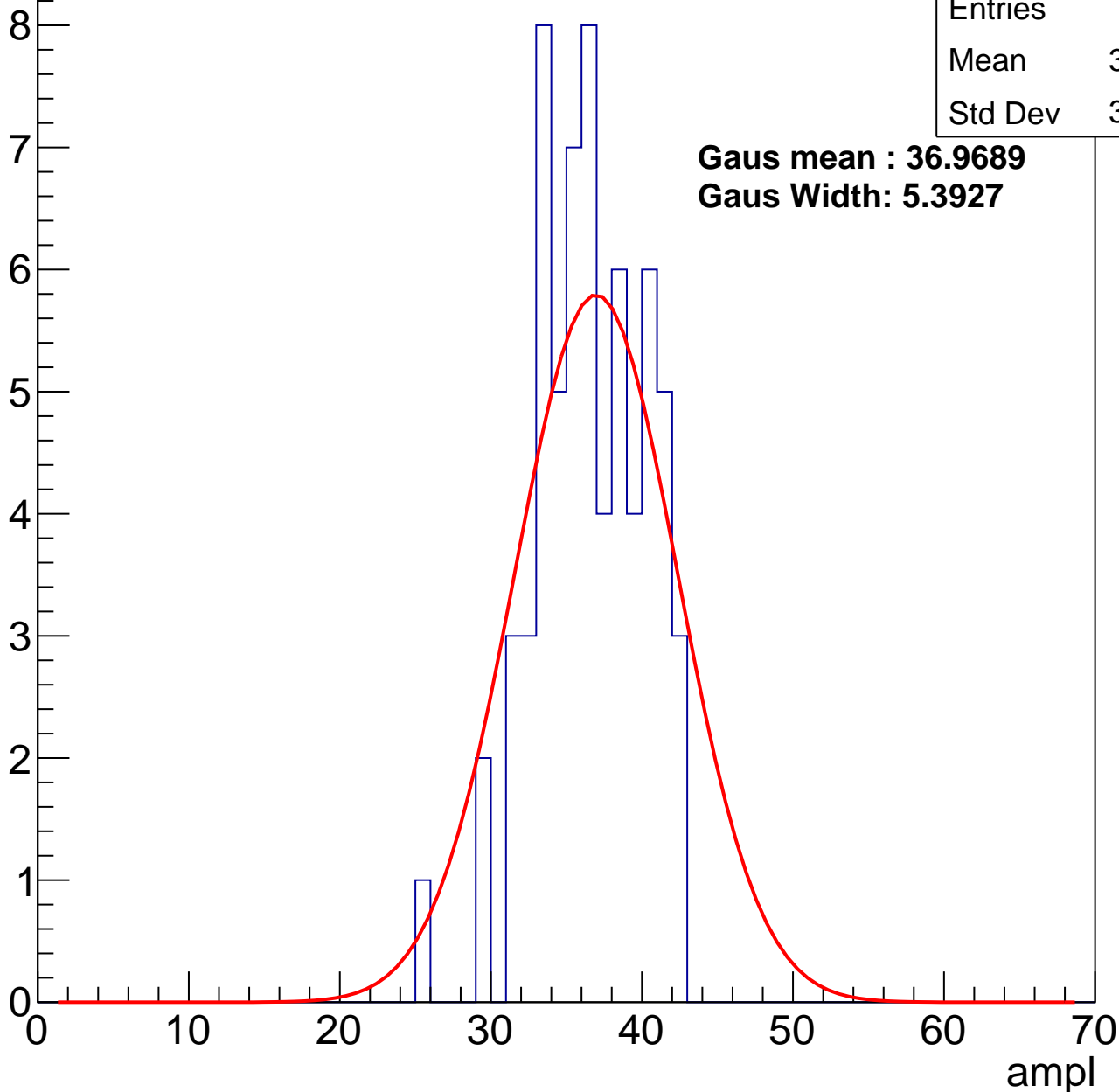
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	65
Mean	36.03
Std Dev	3.582

**Gaus mean : 36.9689**

**Gaus Width: 5.3927**



# B0L002S, U2-ch67, adc2

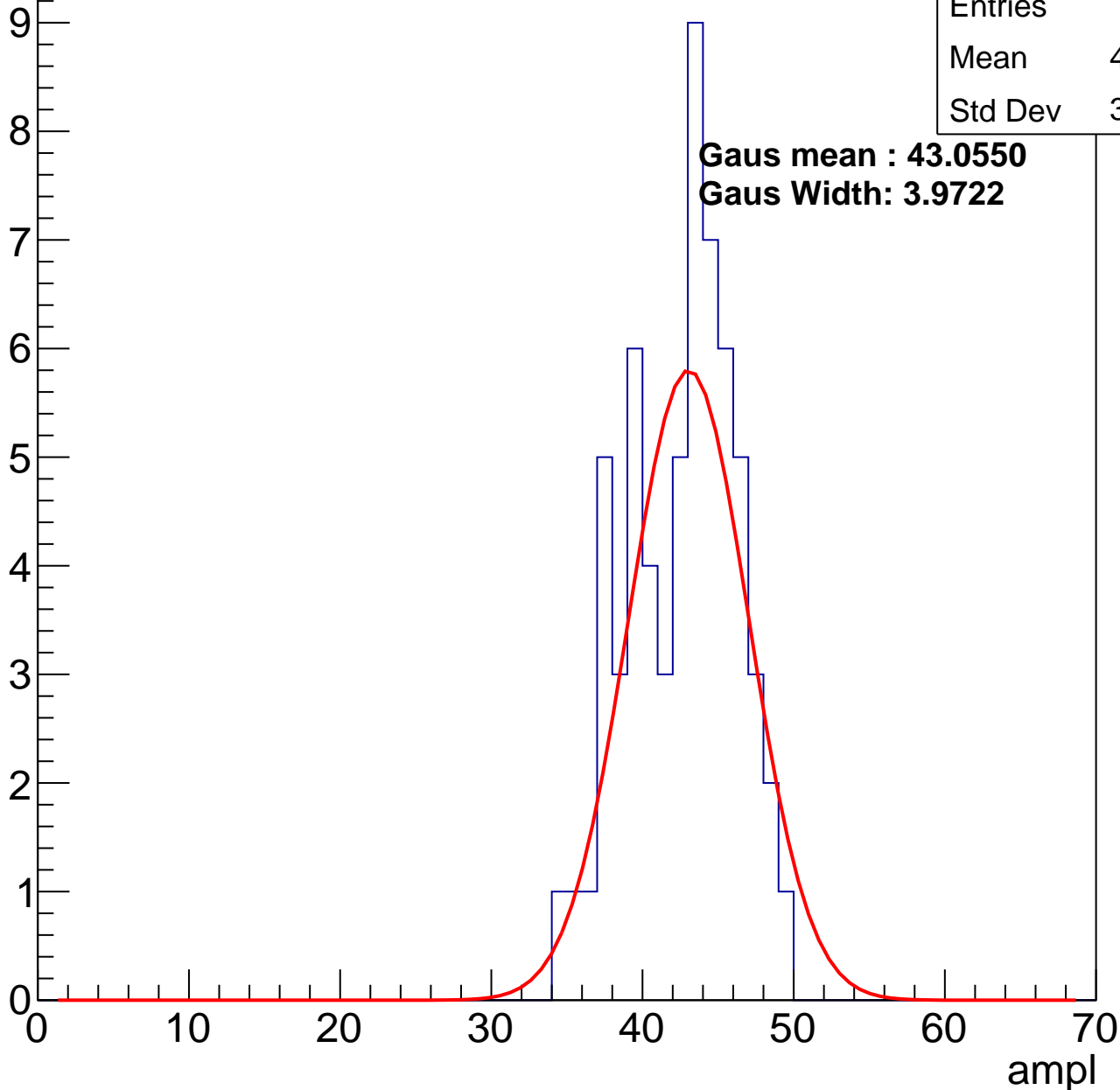
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	62
Mean	42.13
Std Dev	3.503

**Gaus mean : 43.0550**

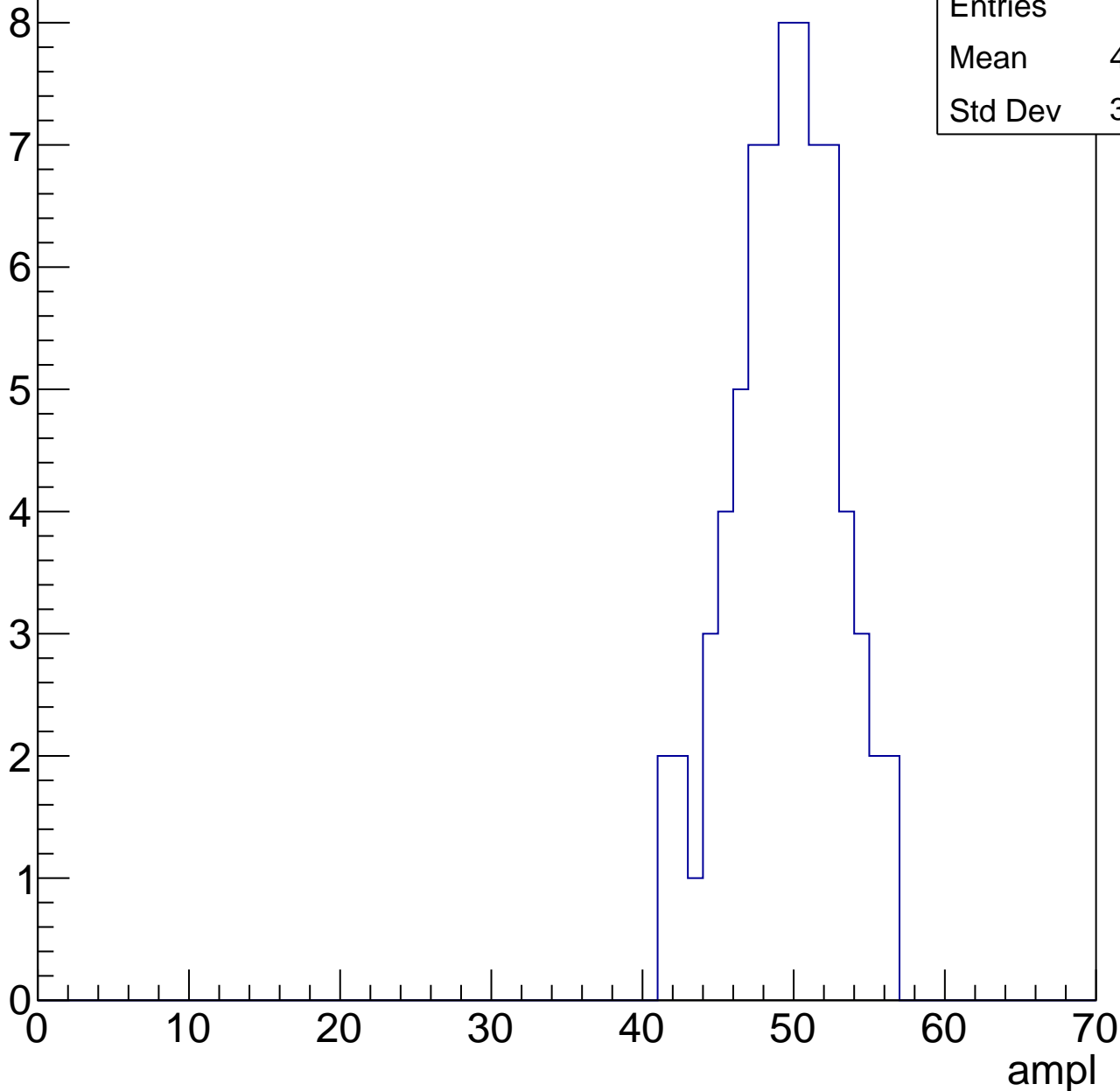
**Gaus Width: 3.9722**



# B0L002S, U2-ch67, adc3

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

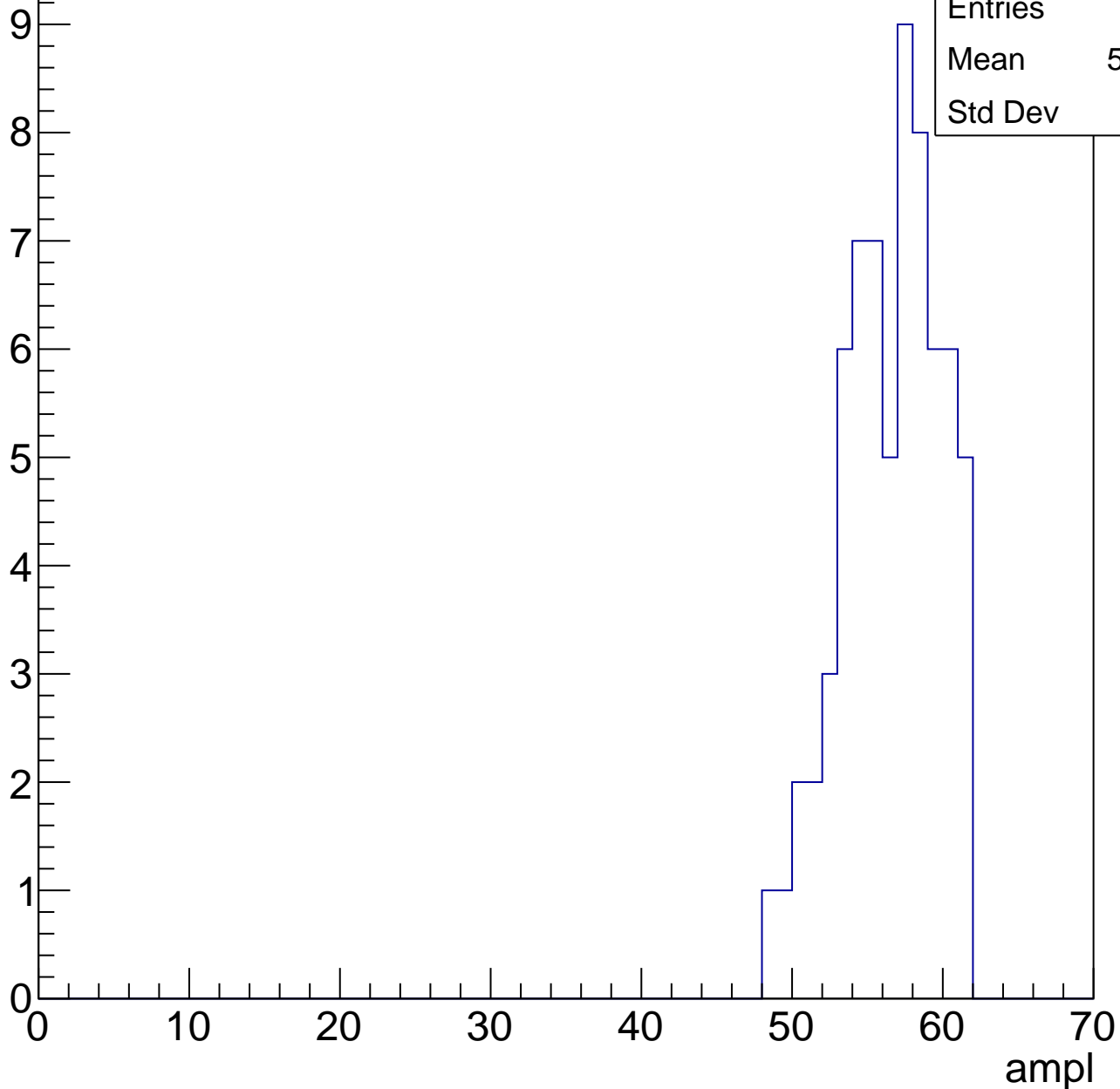


Entries	72
Mean	48.96
Std Dev	3.514

# B0L002S, U2-ch67, adc4

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

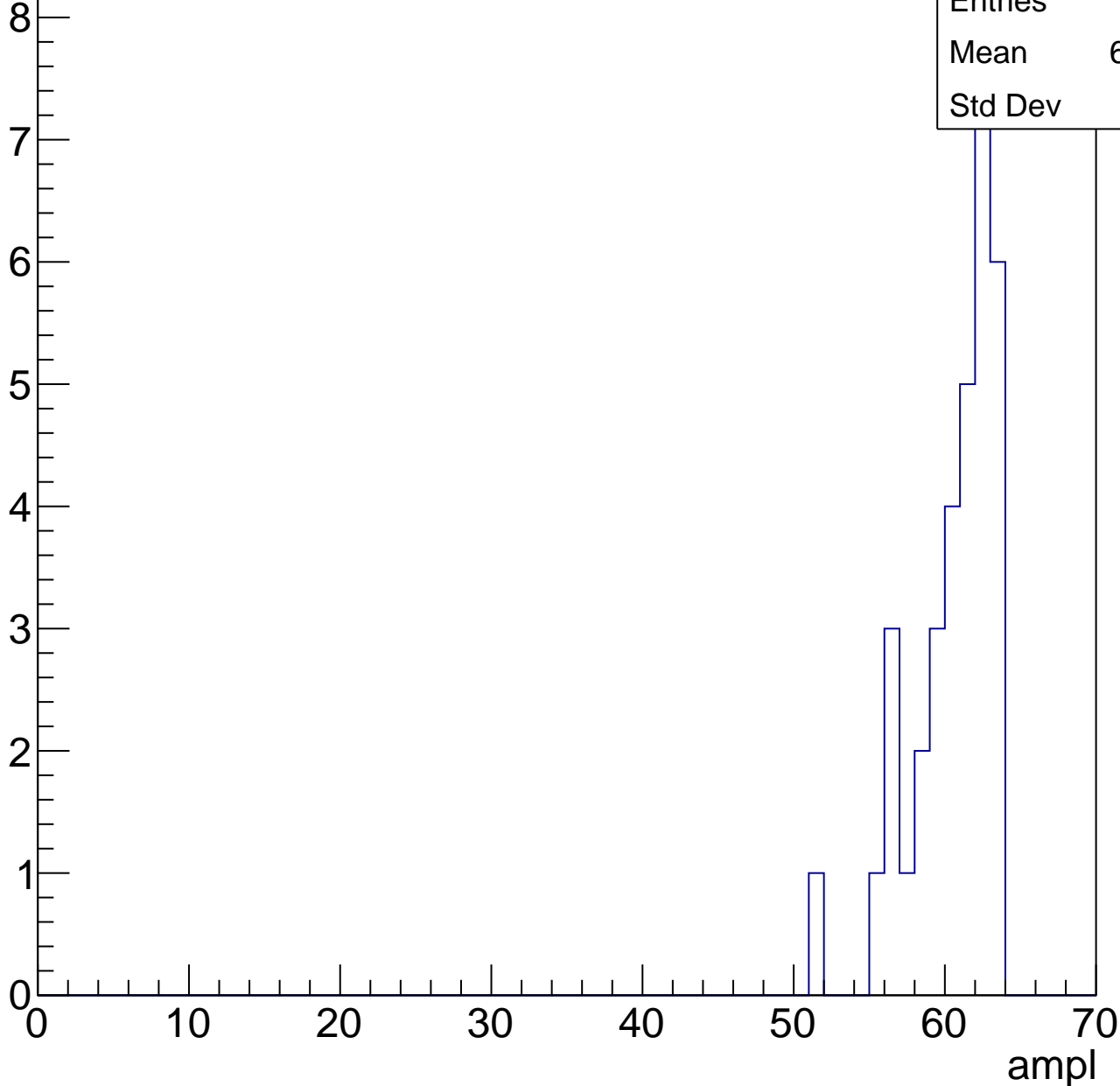


# B0L002S, U2-ch67, adc5

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

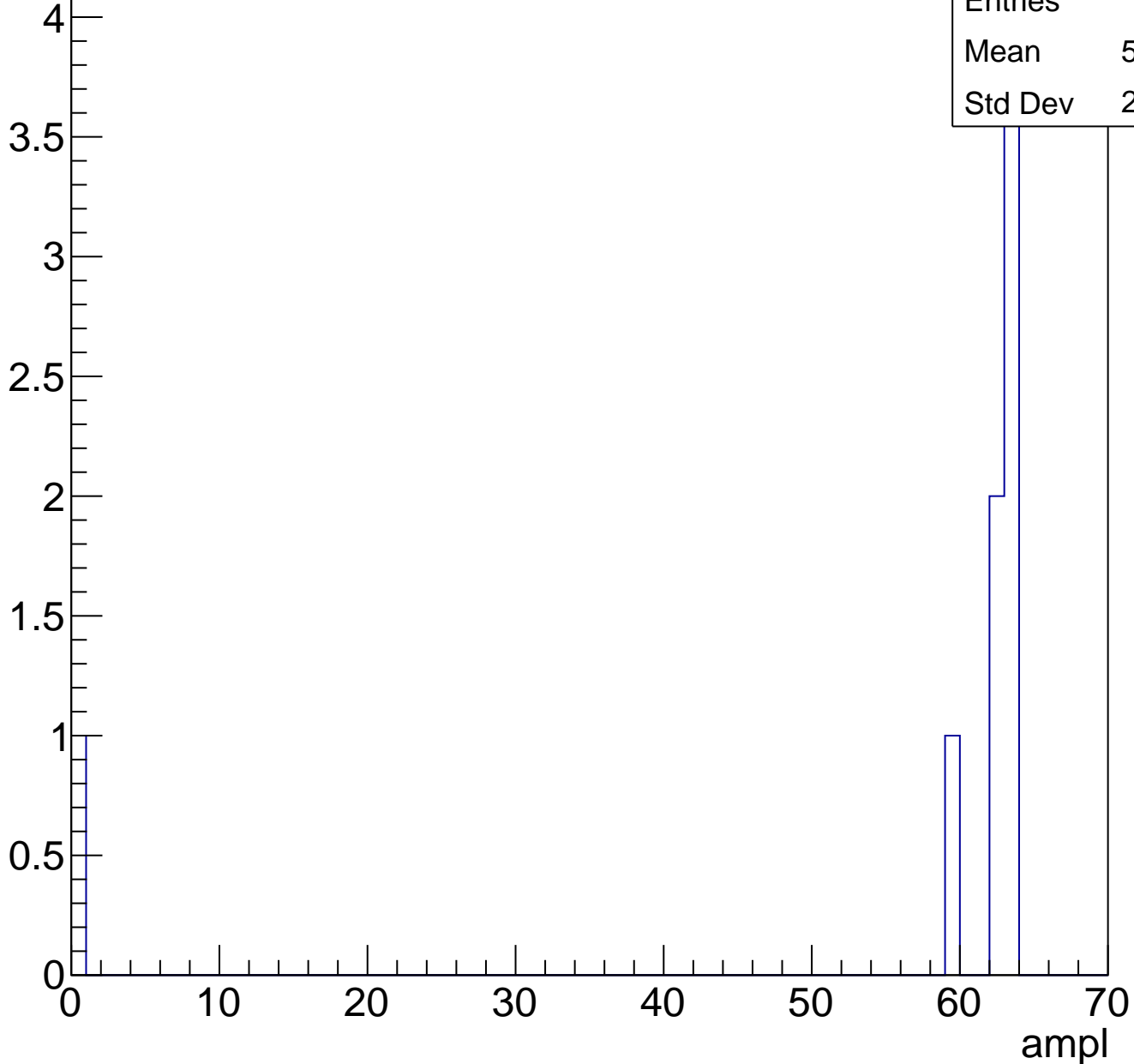
Entries	34
Mean	60.09
Std Dev	2.79



# B0L002S, U2-ch67, adc6

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry





# B0L002S, U2-ch67, adc7

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L002S, U2-ch68, adc0

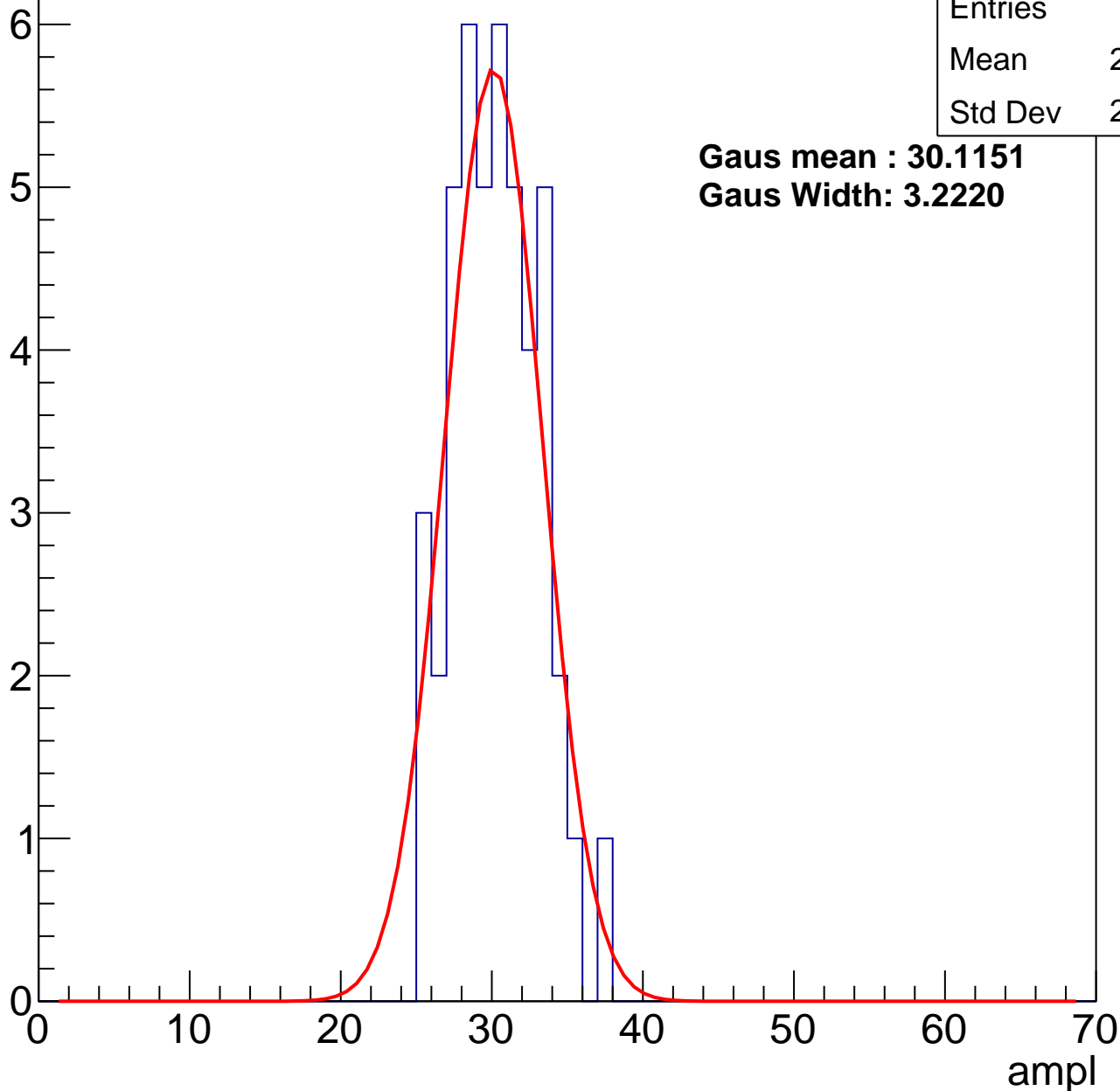
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	45
Mean	29.84
Std Dev	2.796

**Gaus mean : 30.1151**

**Gaus Width: 3.2220**



# B0L002S, U2-ch68, adc1

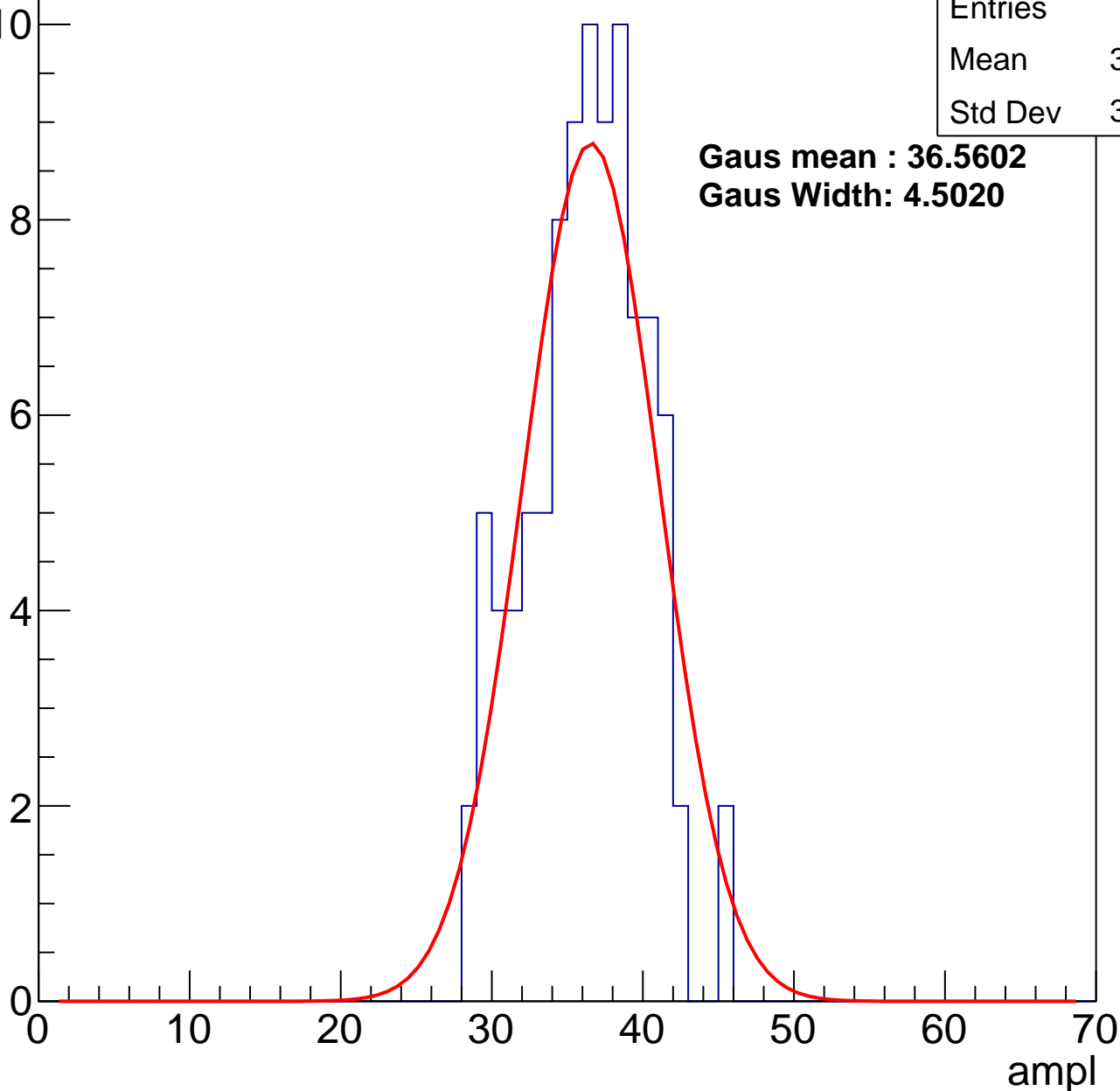
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	95
Mean	35.82
Std Dev	3.822

**Gaus mean : 36.5602**

**Gaus Width: 4.5020**



# B0L002S, U2-ch68, adc2

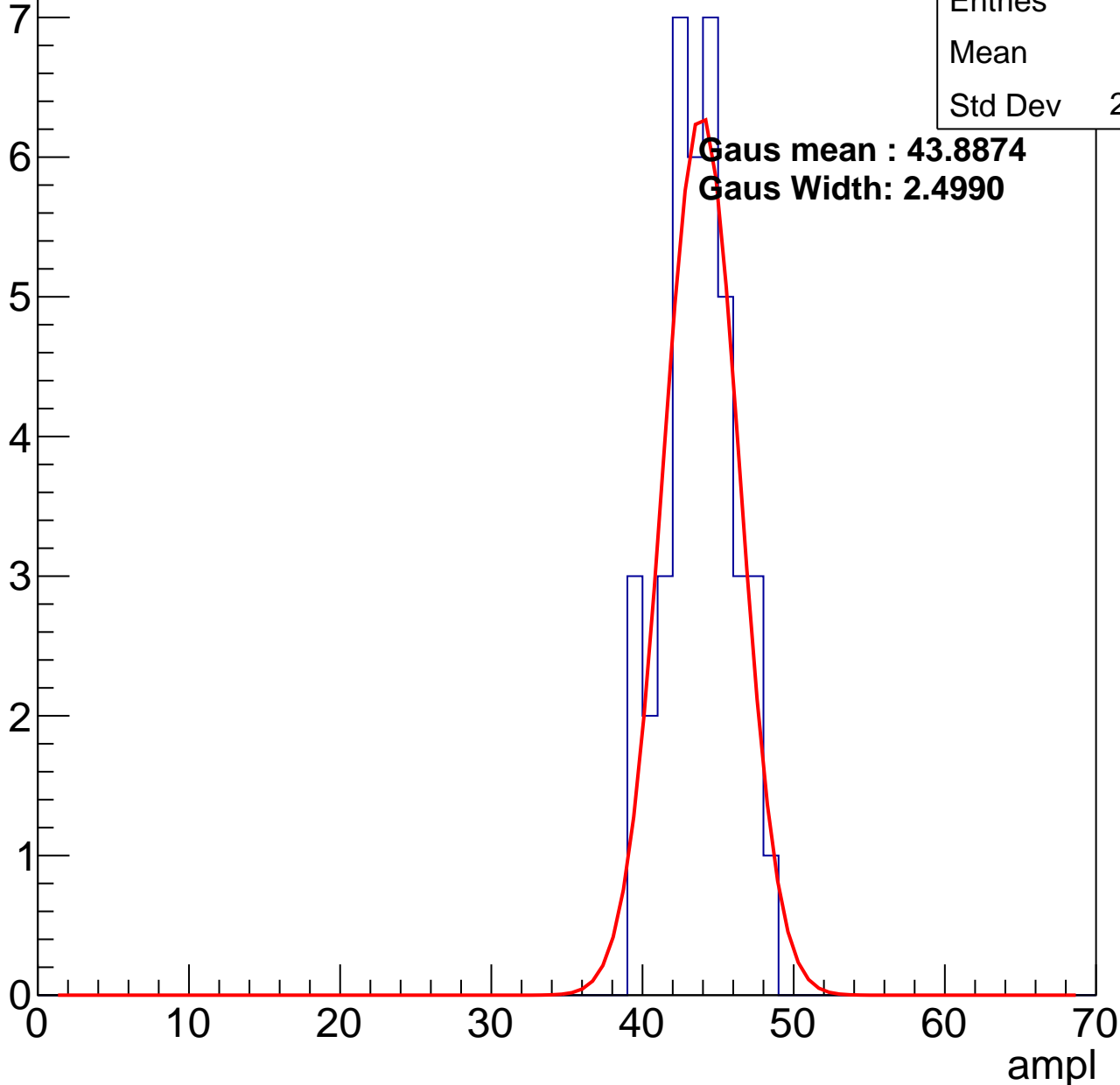
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	40
Mean	43.3
Std Dev	2.283

**Gaus mean : 43.8874**

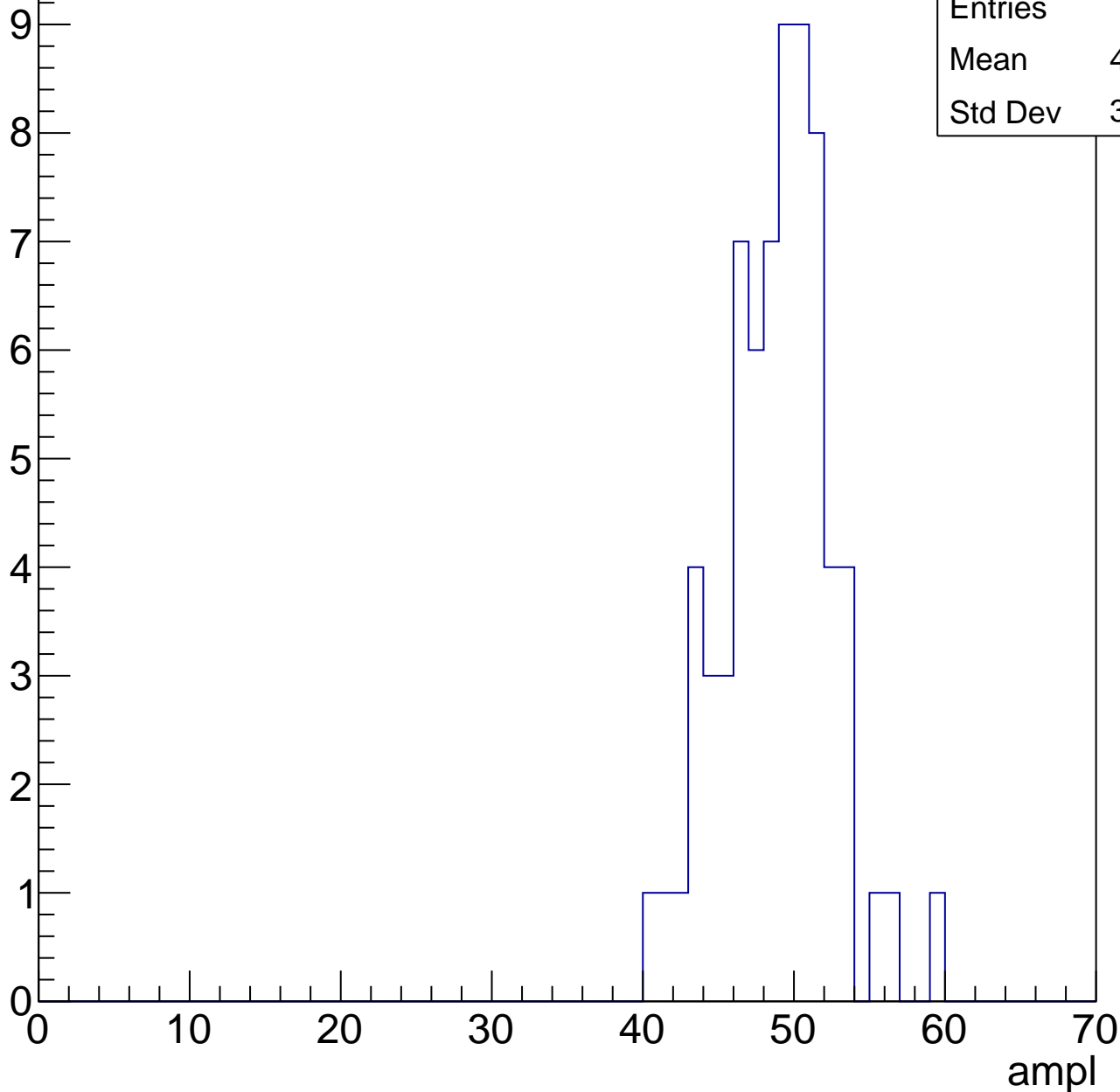
**Gaus Width: 2.4990**



# B0L002S, U2-ch68, adc3

calib\_packv5\_042523\_0143.root, FC#8, port C1

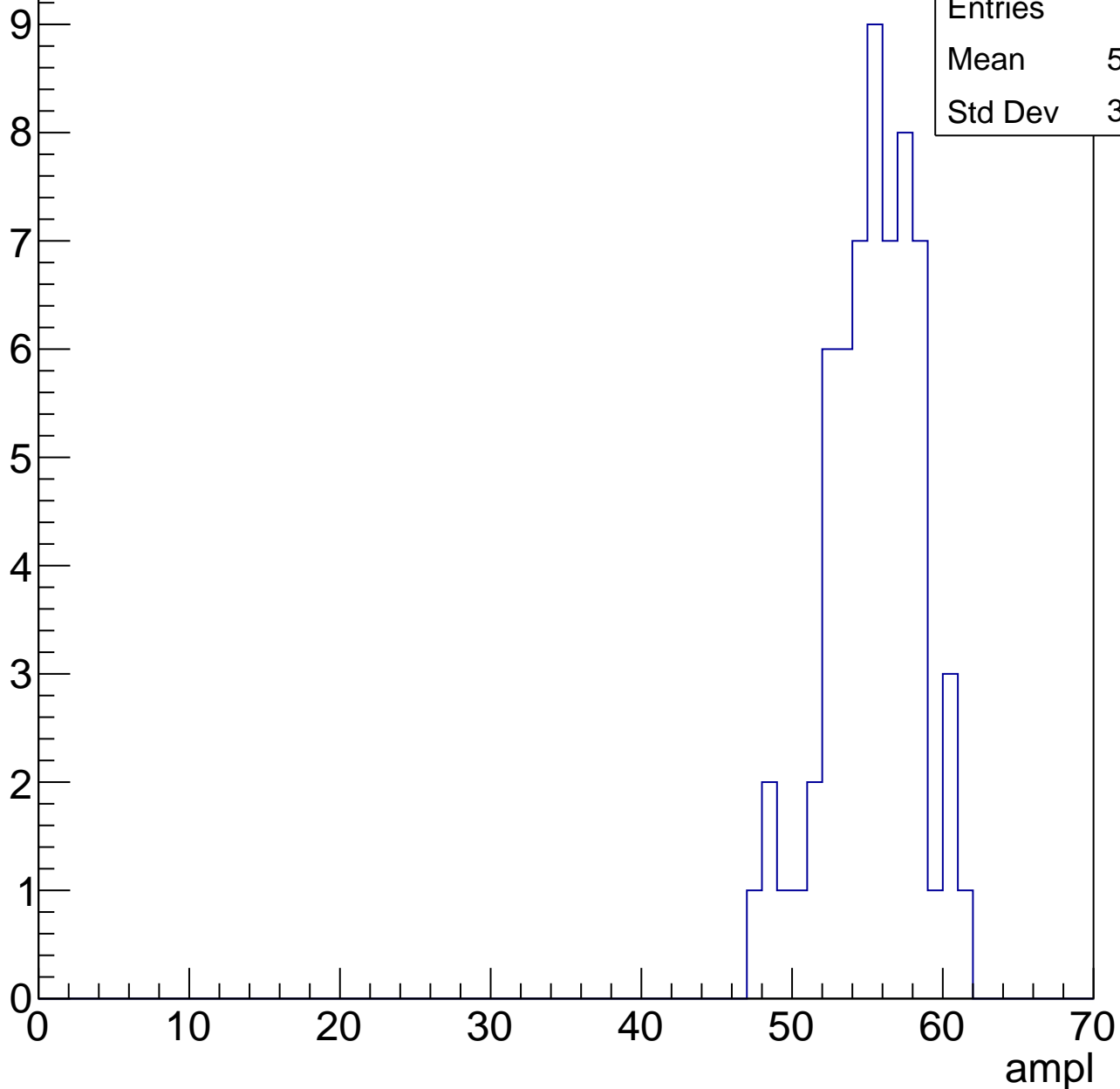
Entry



# B0L002S, U2-ch68, adc4

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

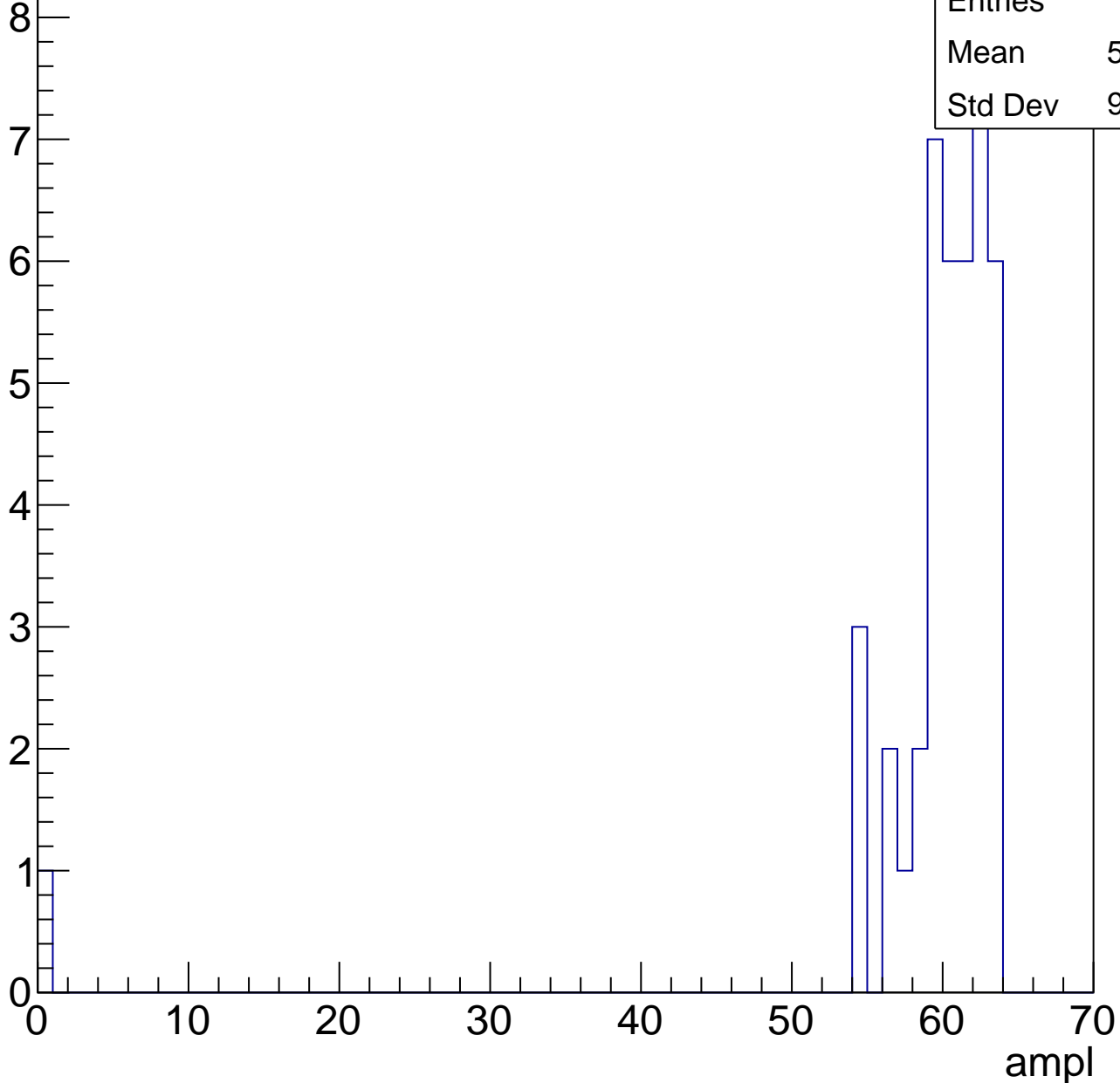


# B0L002S, U2-ch68, adc5

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

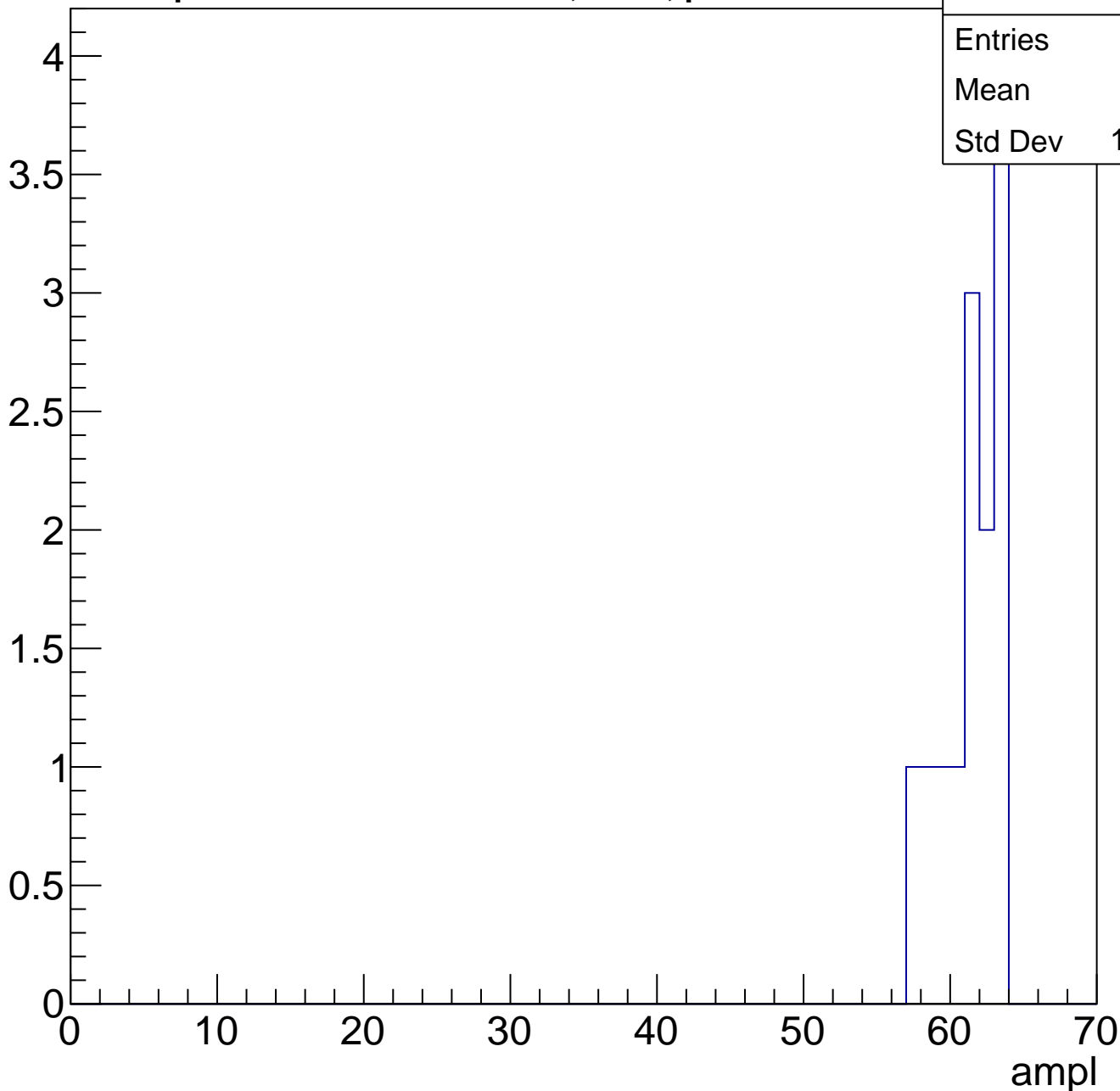
Entries	42
Mean	58.57
Std Dev	9.475



# B0L002S, U2-ch68, adc6

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



Entries	13
Mean	61
Std Dev	1.922



# B0L002S, U2-ch68, adc7

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



# B0L002S, U2-ch69, adc0

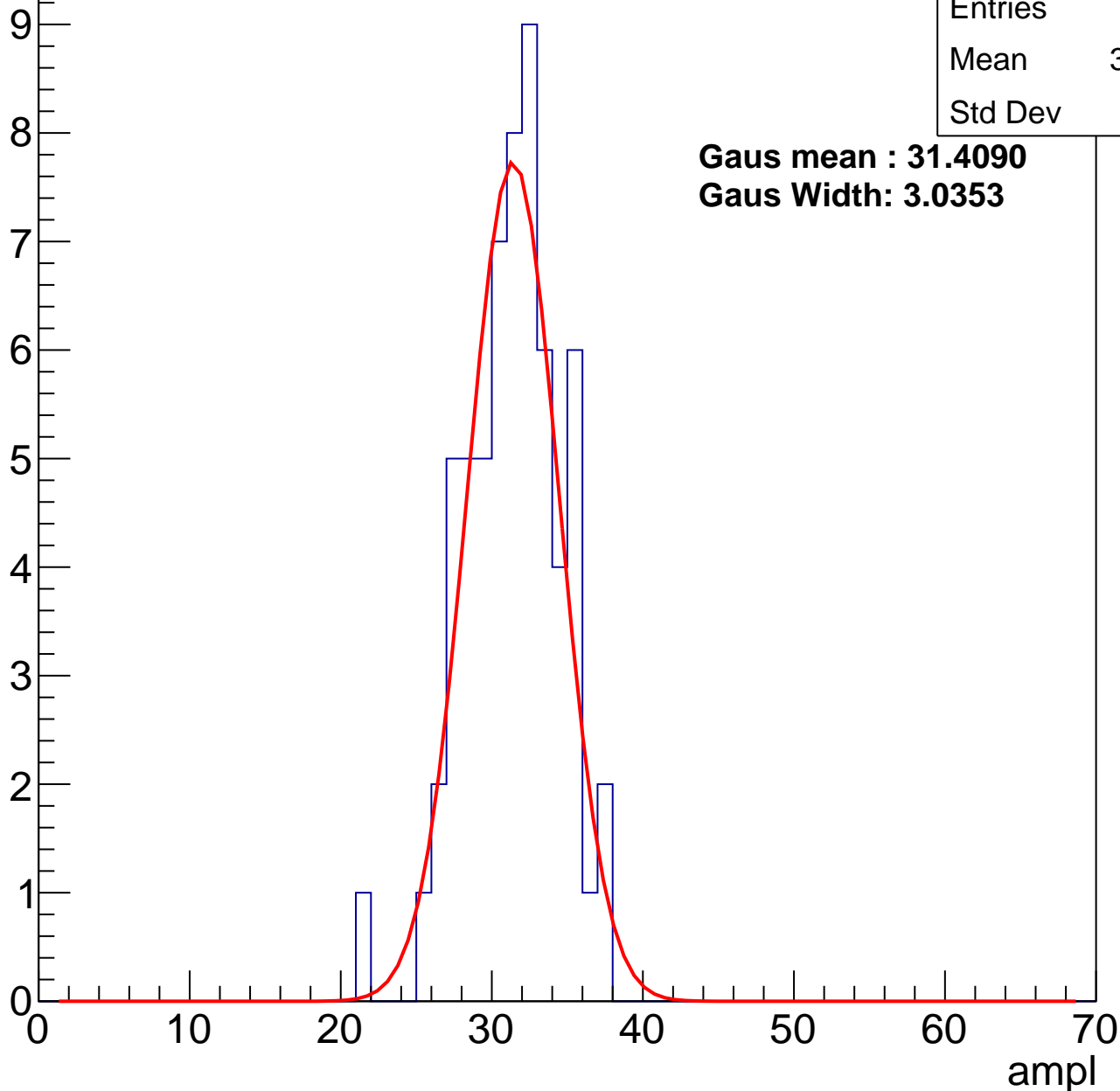
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	62
Mean	30.94
Std Dev	3.11

**Gaus mean : 31.4090**

**Gaus Width: 3.0353**



# B0L002S, U2-ch69, adc1

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entries	72
Mean	37.94
Std Dev	3.236

**Gaus mean : 38.4324**

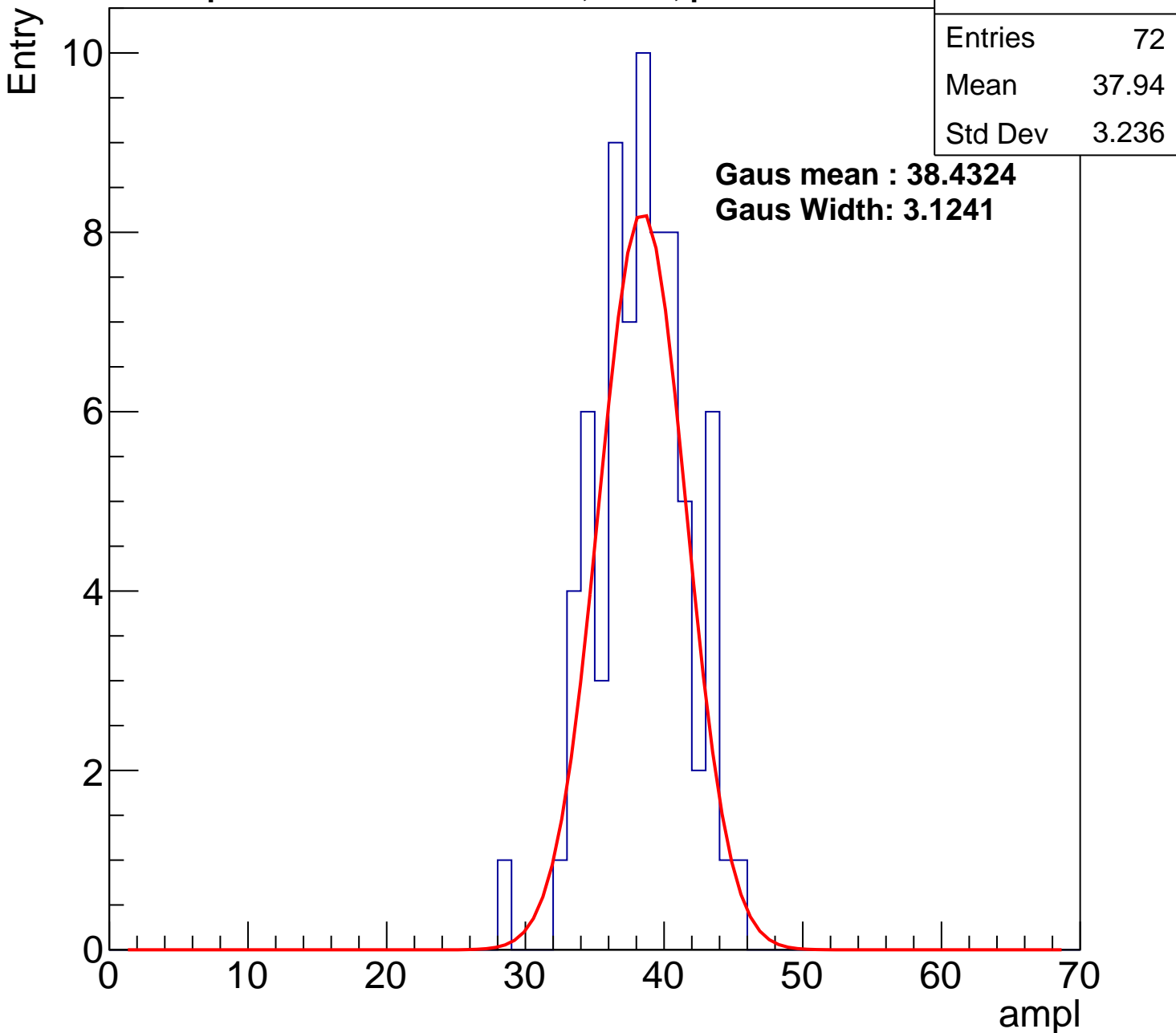
**Gaus Width: 3.1241**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B0L002S, U2-ch69, adc2

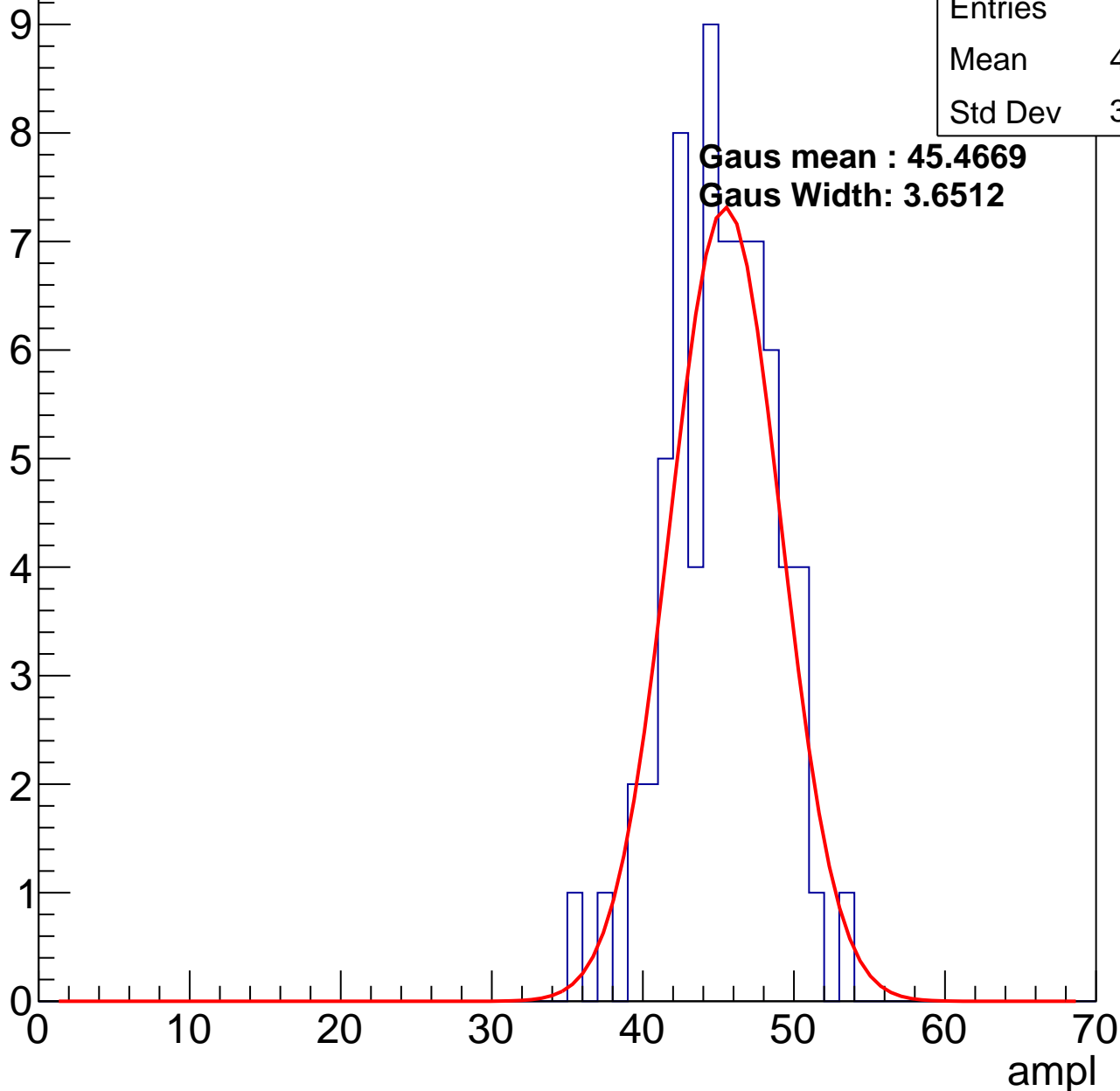
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	69
Mean	44.83
Std Dev	3.435

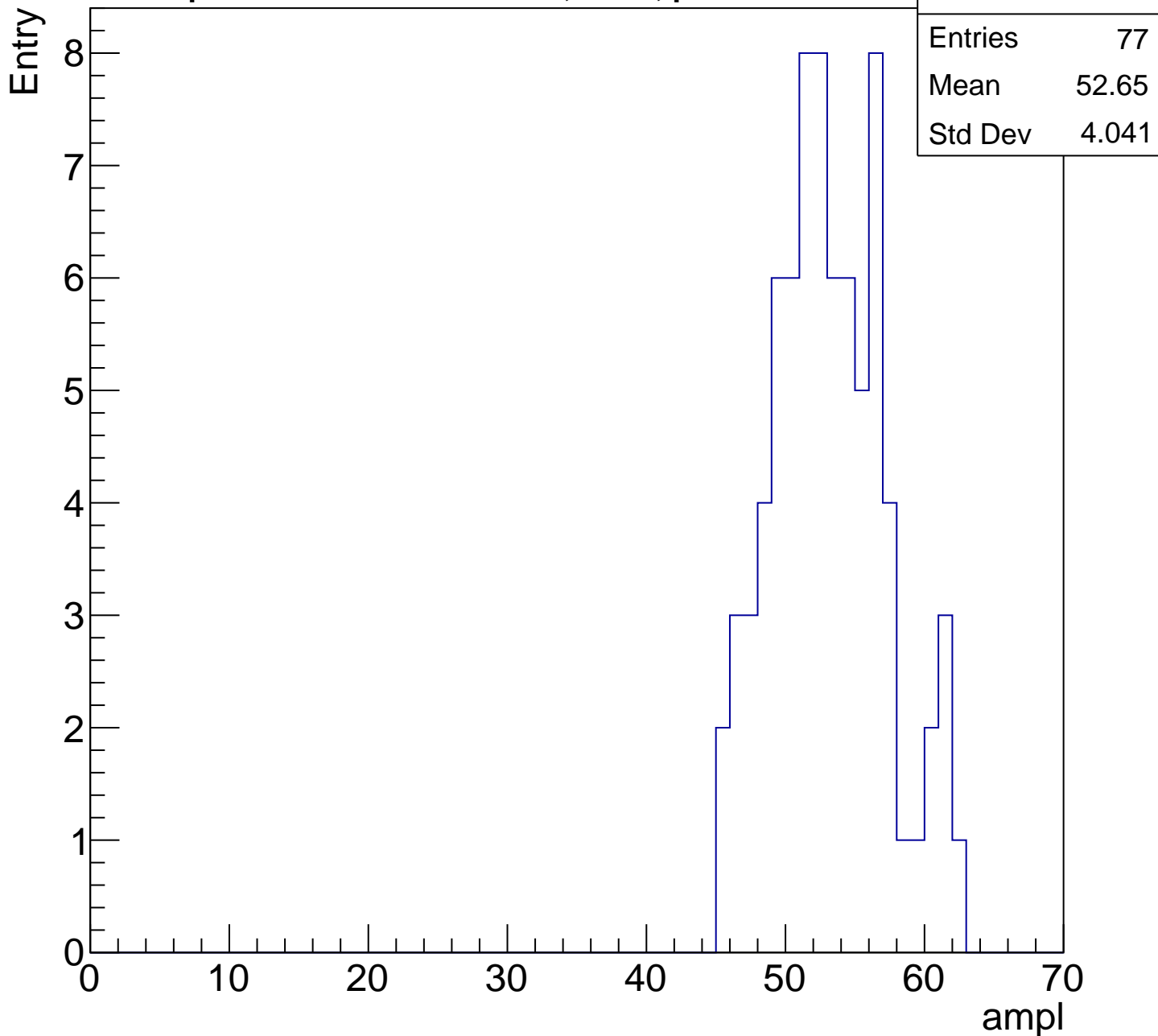
**Gaus mean : 45.4669**

**Gaus Width: 3.6512**



# B0L002S, U2-ch69, adc3

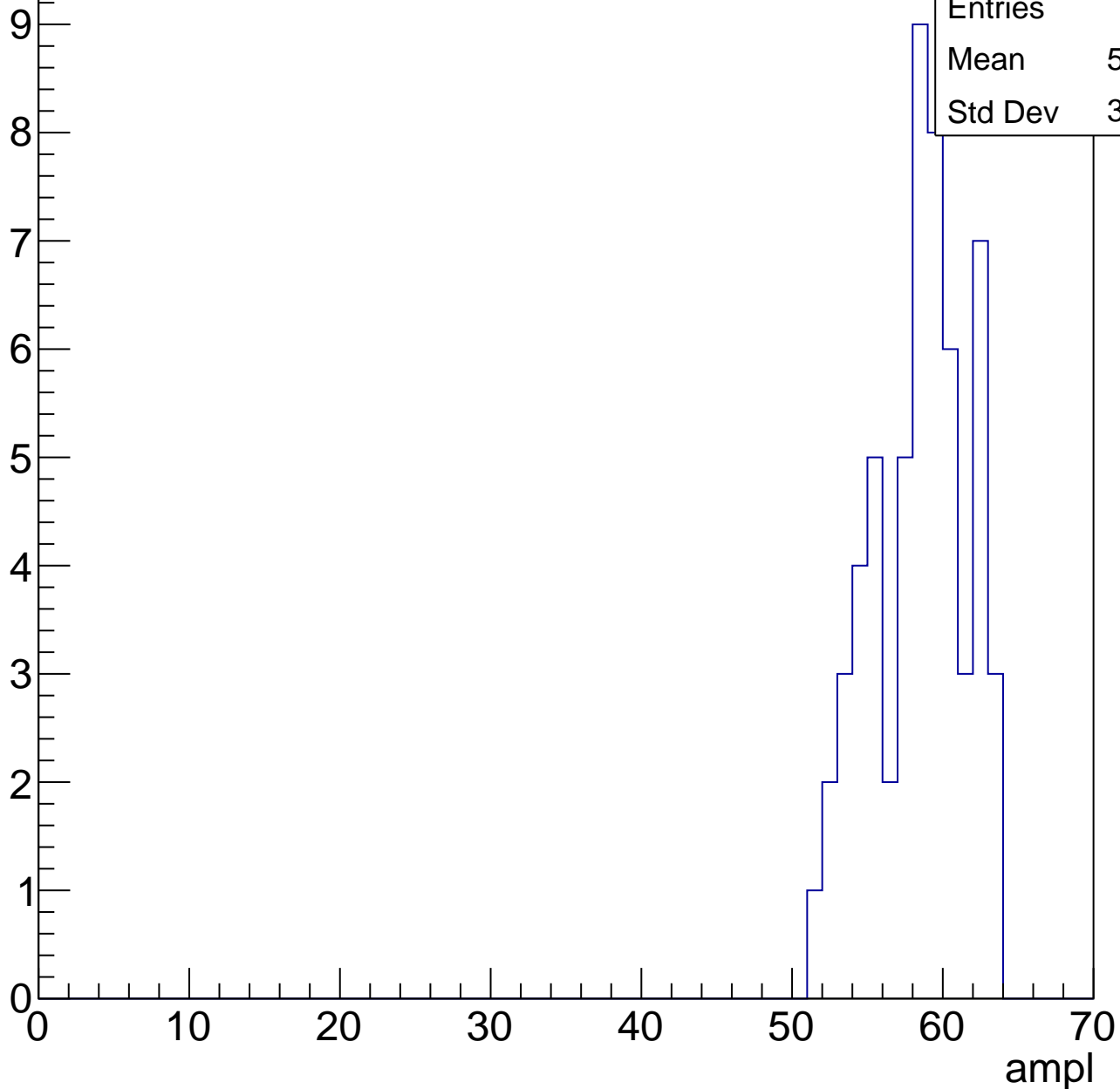
calib\_packv5\_042523\_0143.root, FC#8, port C1



# B0L002S, U2-ch69, adc4

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

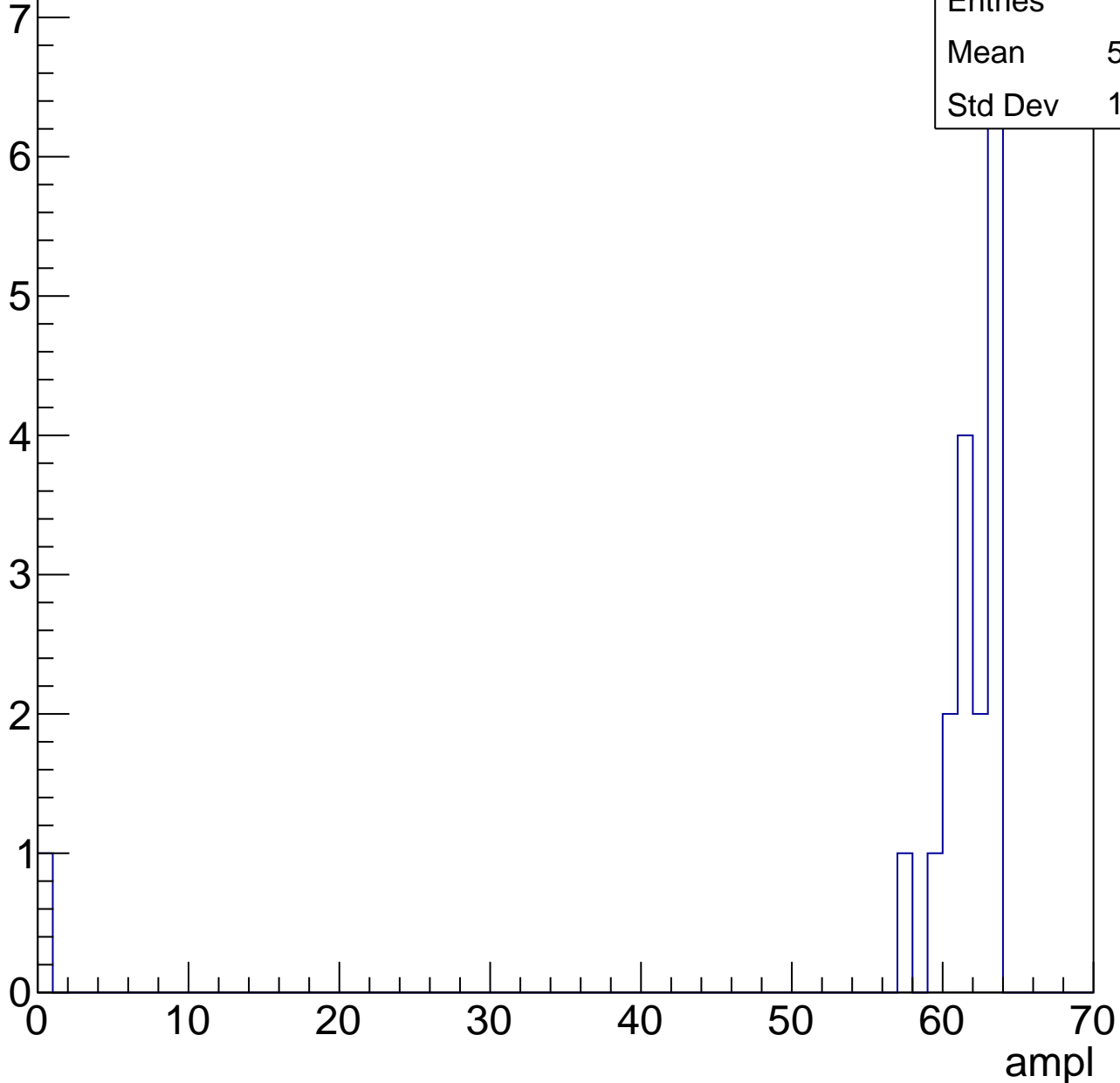


# B0L002S, U2-ch69, adc5

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	18
Mean	58.06
Std Dev	14.18



# B0L002S, U2-ch69, adc6

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



Entries	0
Mean	0
Std Dev	0



# B0L002S, U2-ch69, adc7

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L002S, U2-ch70, adc0

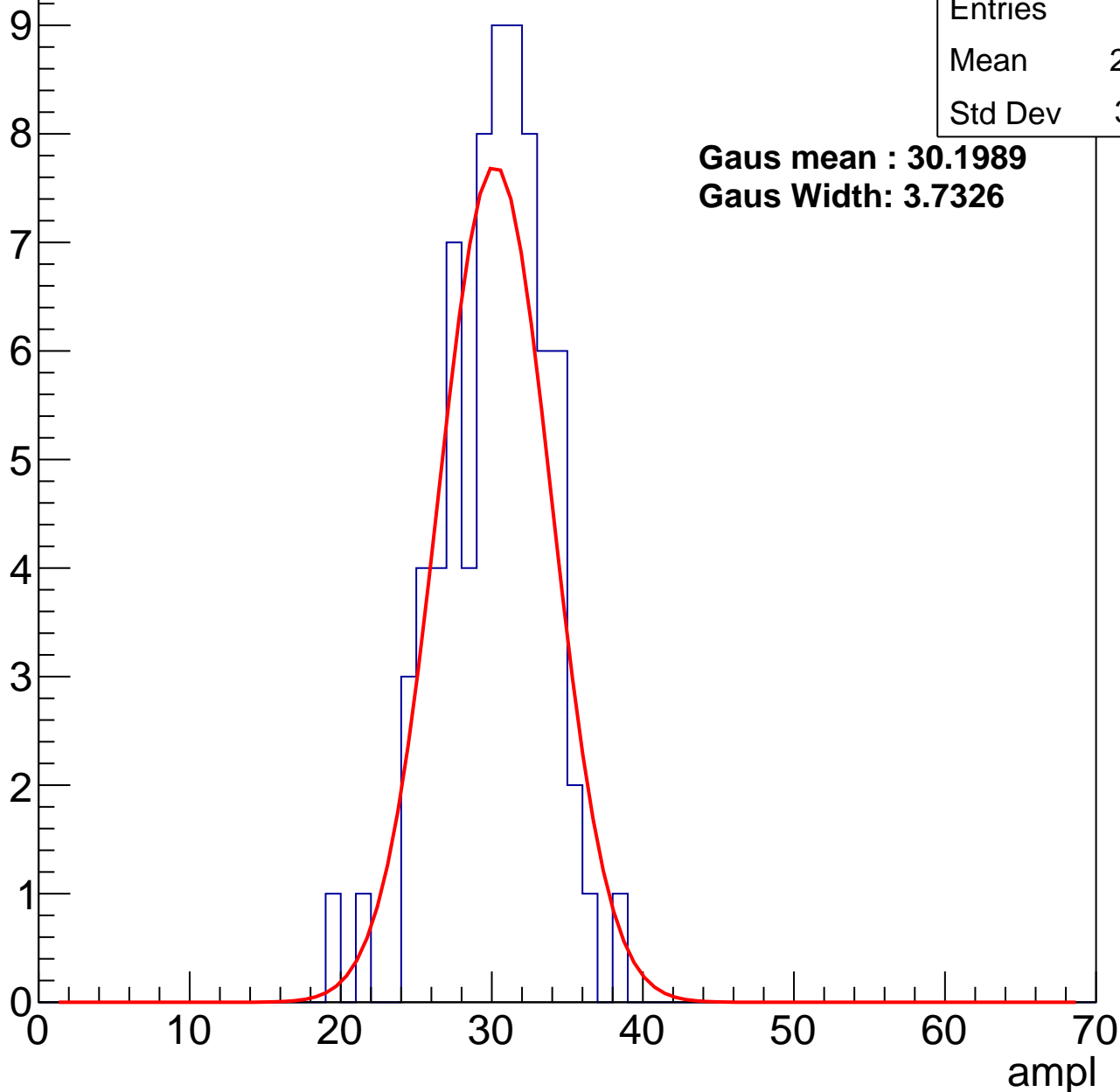
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	74
Mean	29.73
Std Dev	3.481

**Gaus mean : 30.1989**

**Gaus Width: 3.7326**



# B0L002S, U2-ch70, adc1

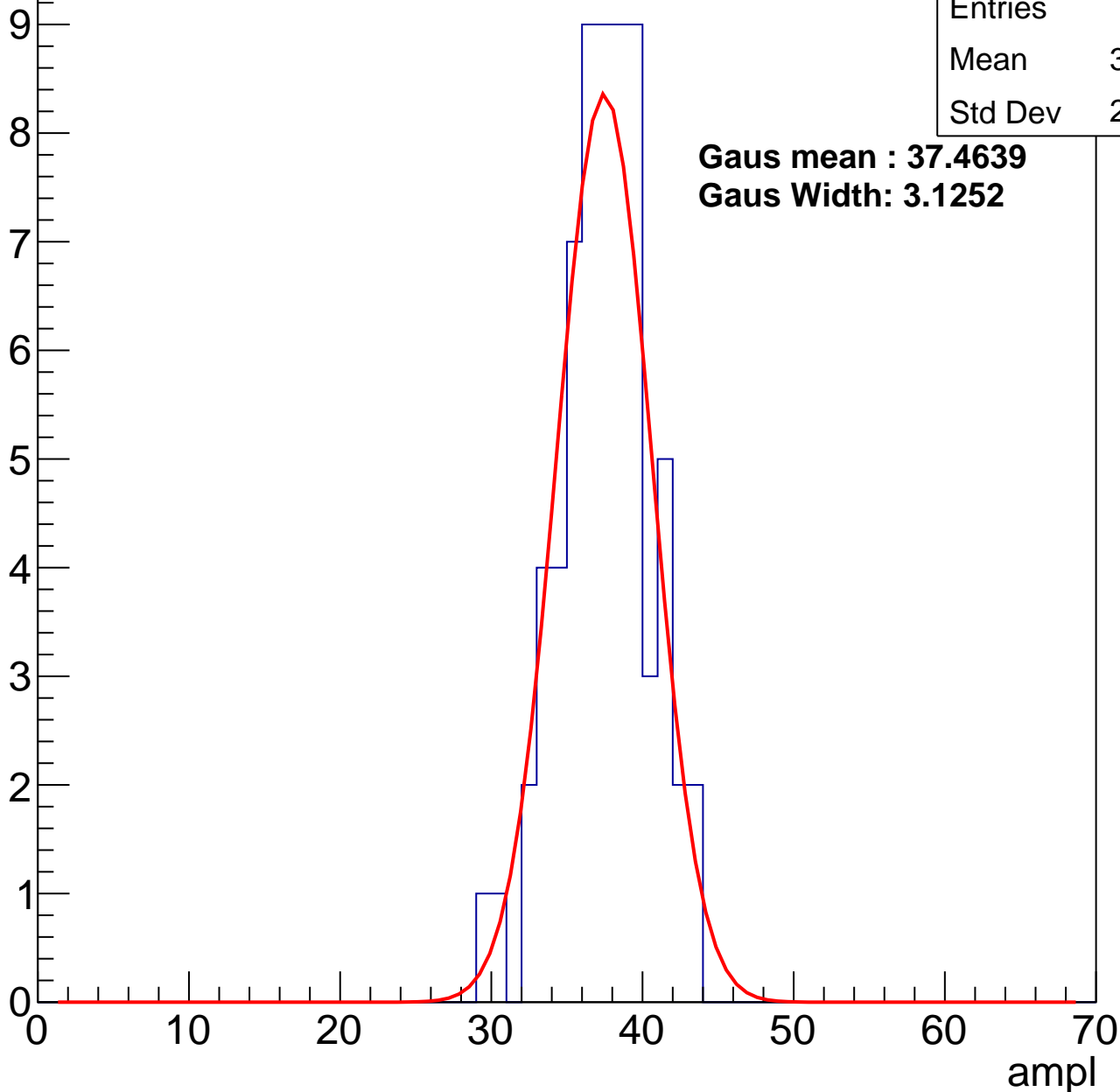
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	67
Mean	37.03
Std Dev	2.927

**Gaus mean : 37.4639**

**Gaus Width: 3.1252**



# B0L002S, U2-ch70, adc2

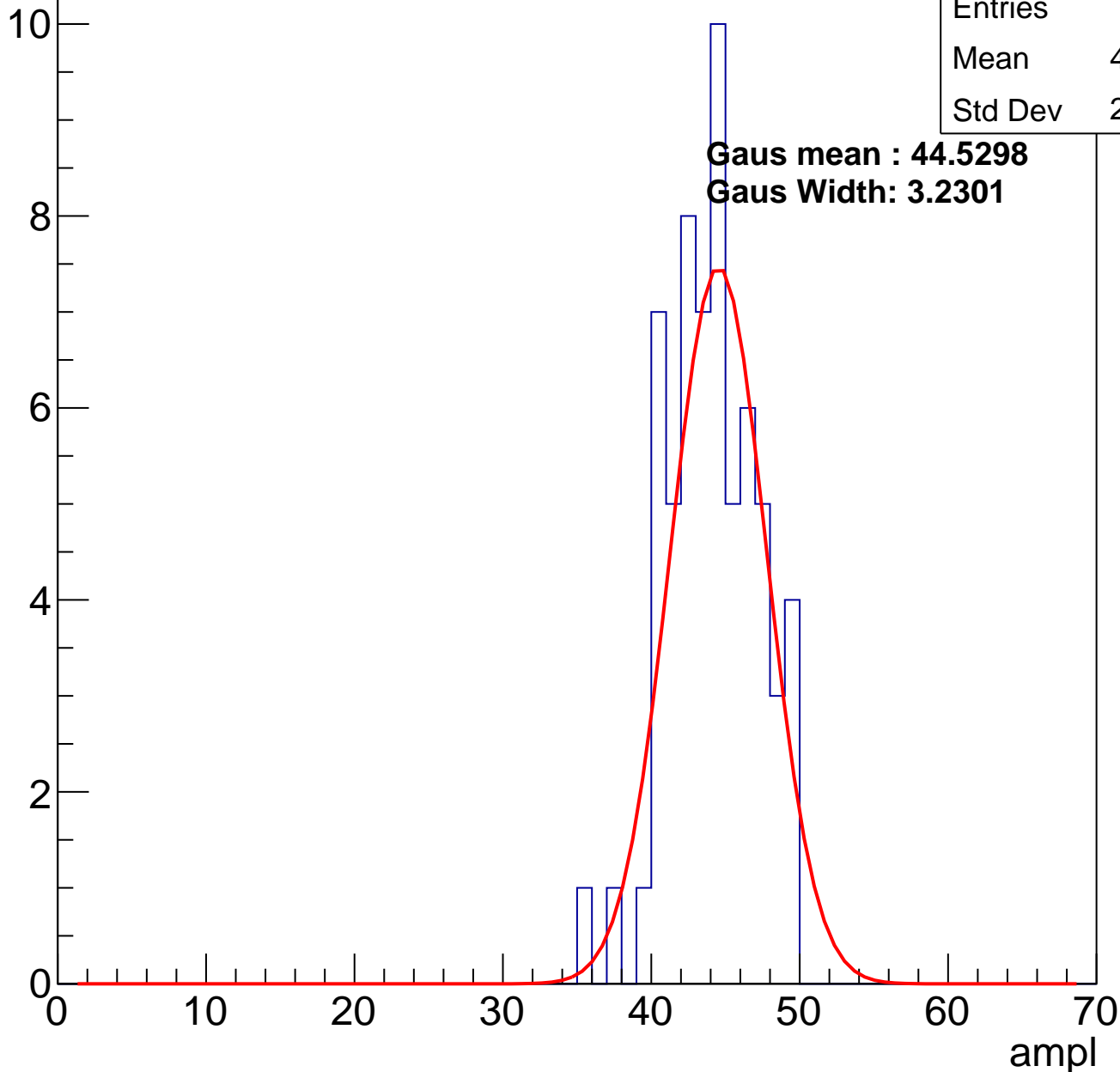
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entries	63
Mean	43.63
Std Dev	2.994

**Gaus mean : 44.5298**

**Gaus Width: 3.2301**

Entry

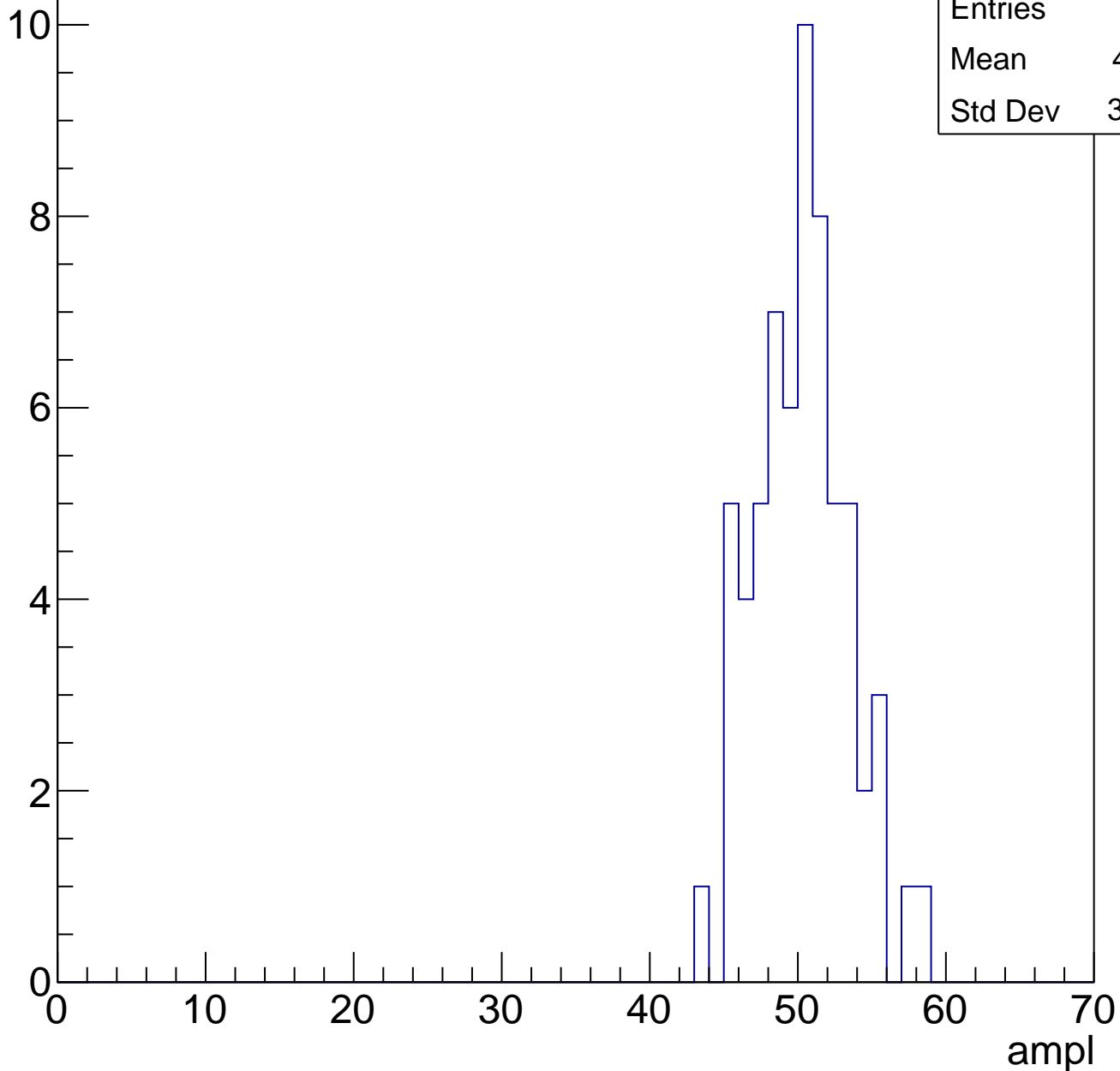


# B0L002S, U2-ch70, adc3

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entries	63
Mean	49.81
Std Dev	3.106

Entry

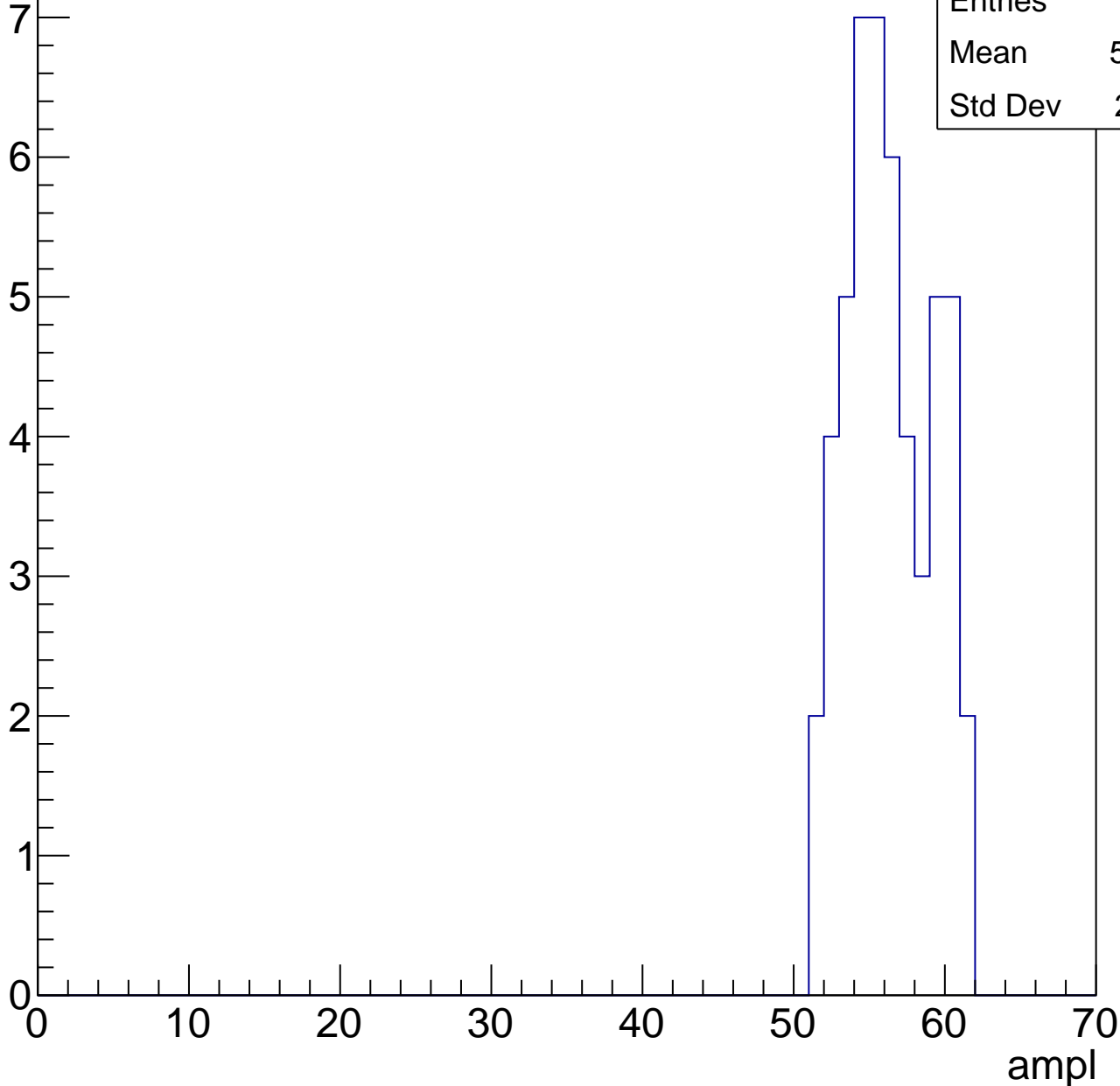


# B0L002S, U2-ch70, adc4

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	50
Mean	55.86
Std Dev	2.771

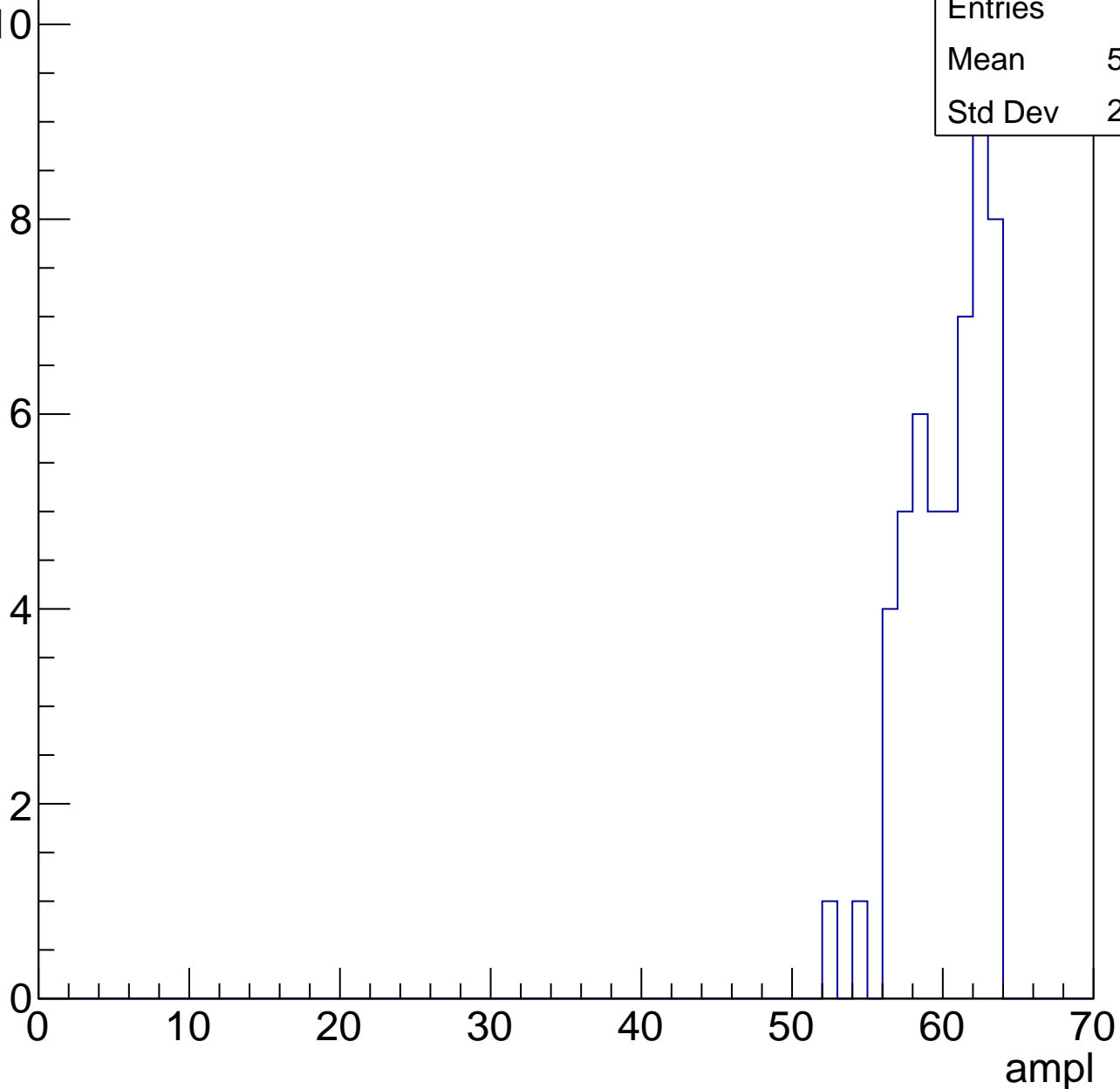


# B0L002S, U2-ch70, adc5

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

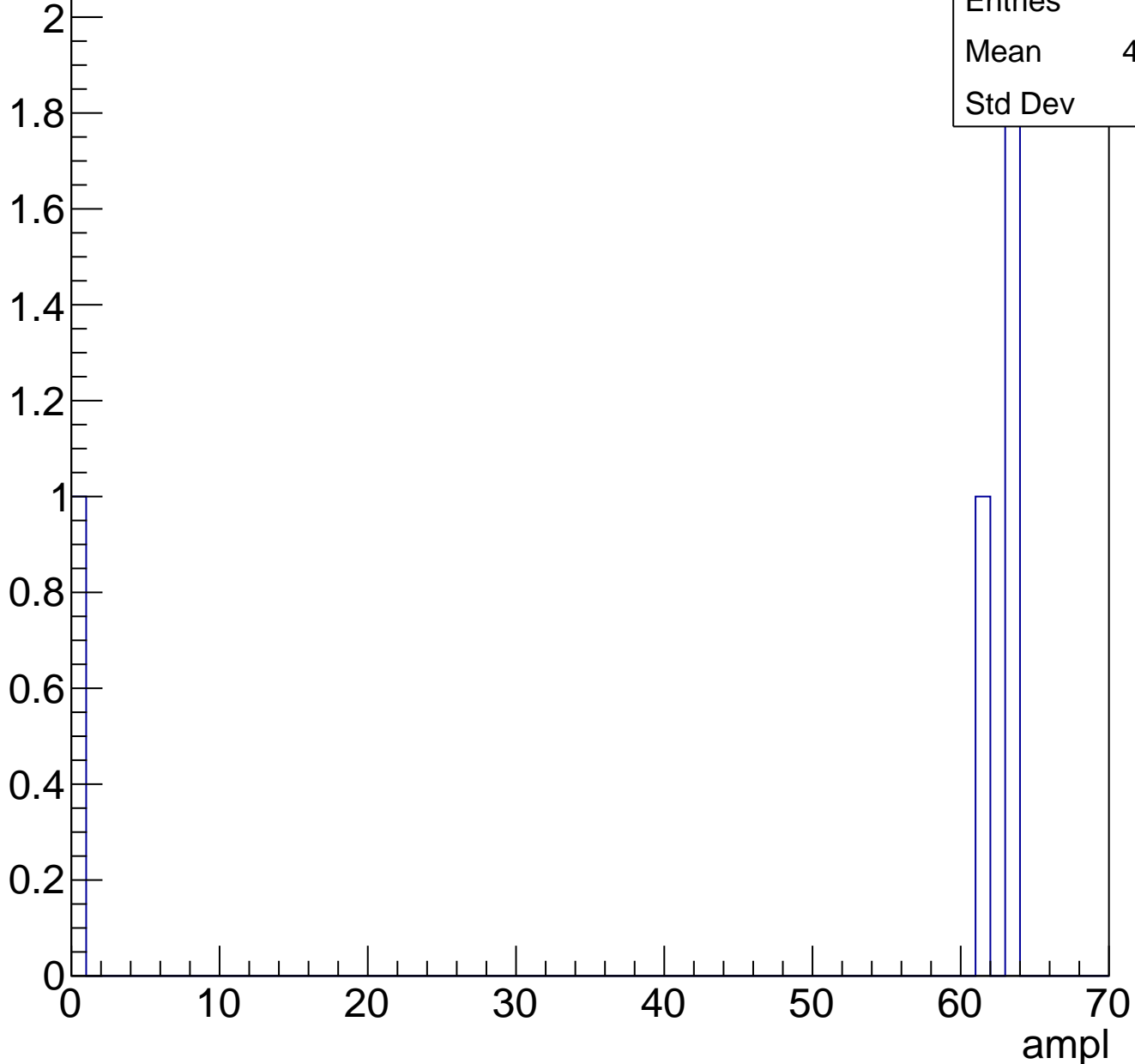
Entries	52
Mean	59.79
Std Dev	2.612



# B0L002S, U2-ch70, adc6

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



Entries	4
Mean	46.75
Std Dev	27



# B0L002S, U2-ch70, adc7

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L002S, U2-ch71, adc0

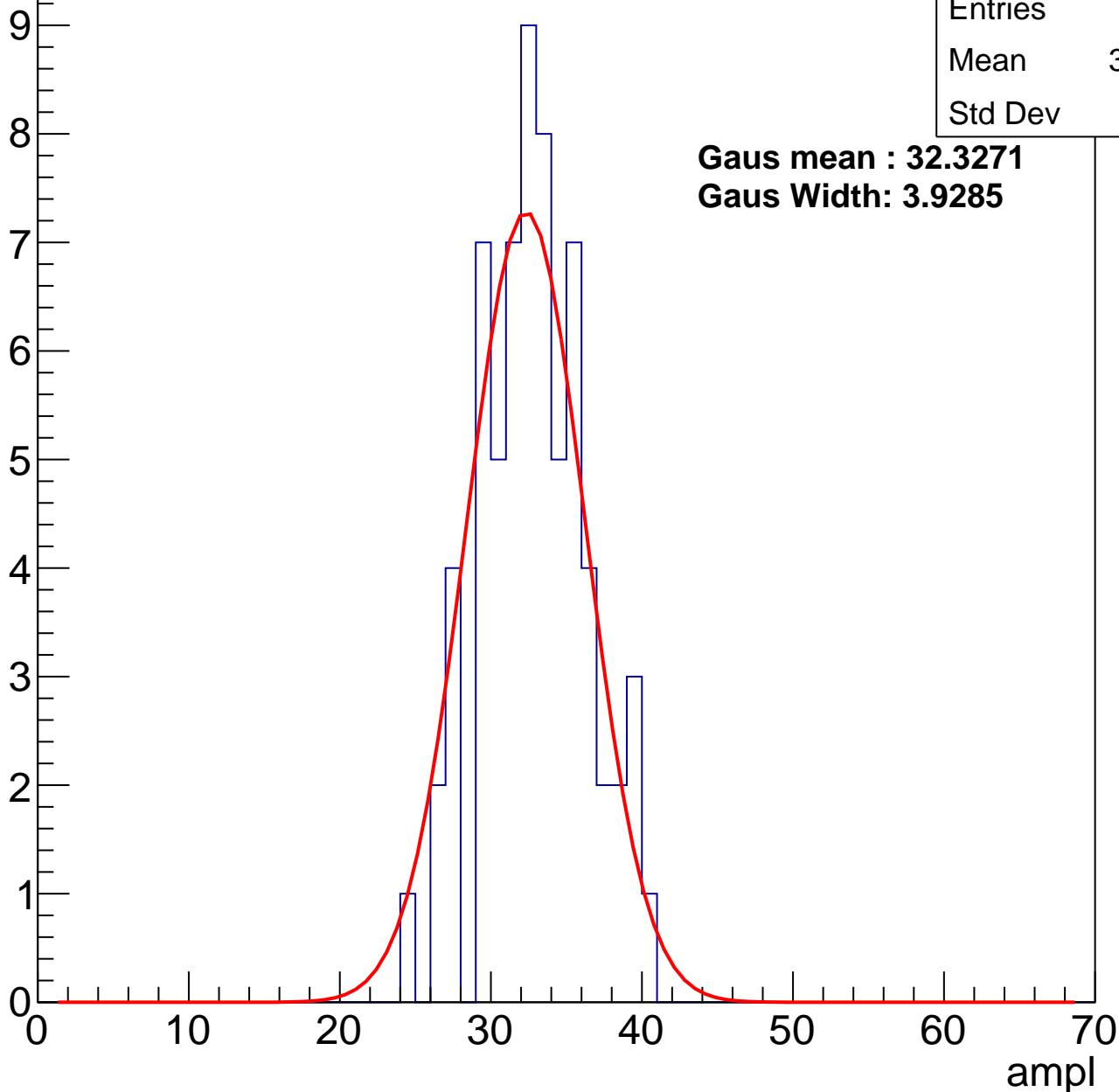
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	67
Mean	32.42
Std Dev	3.46

**Gaus mean : 32.3271**

**Gaus Width: 3.9285**



# B0L002S, U2-ch71, adc1

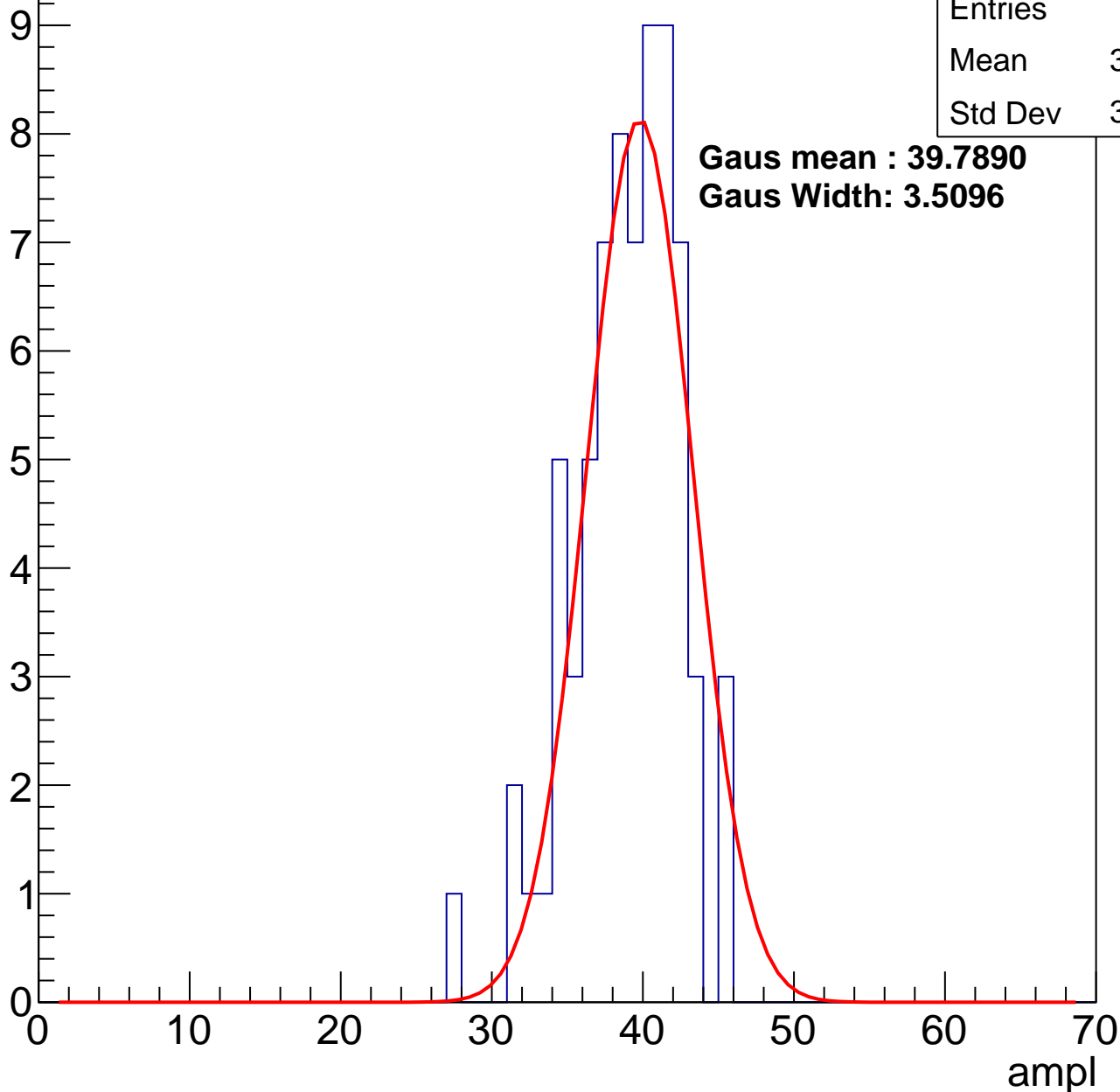
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	71
Mean	38.48
Std Dev	3.472

**Gaus mean : 39.7890**

**Gaus Width: 3.5096**



# B0L002S, U2-ch71, adc2

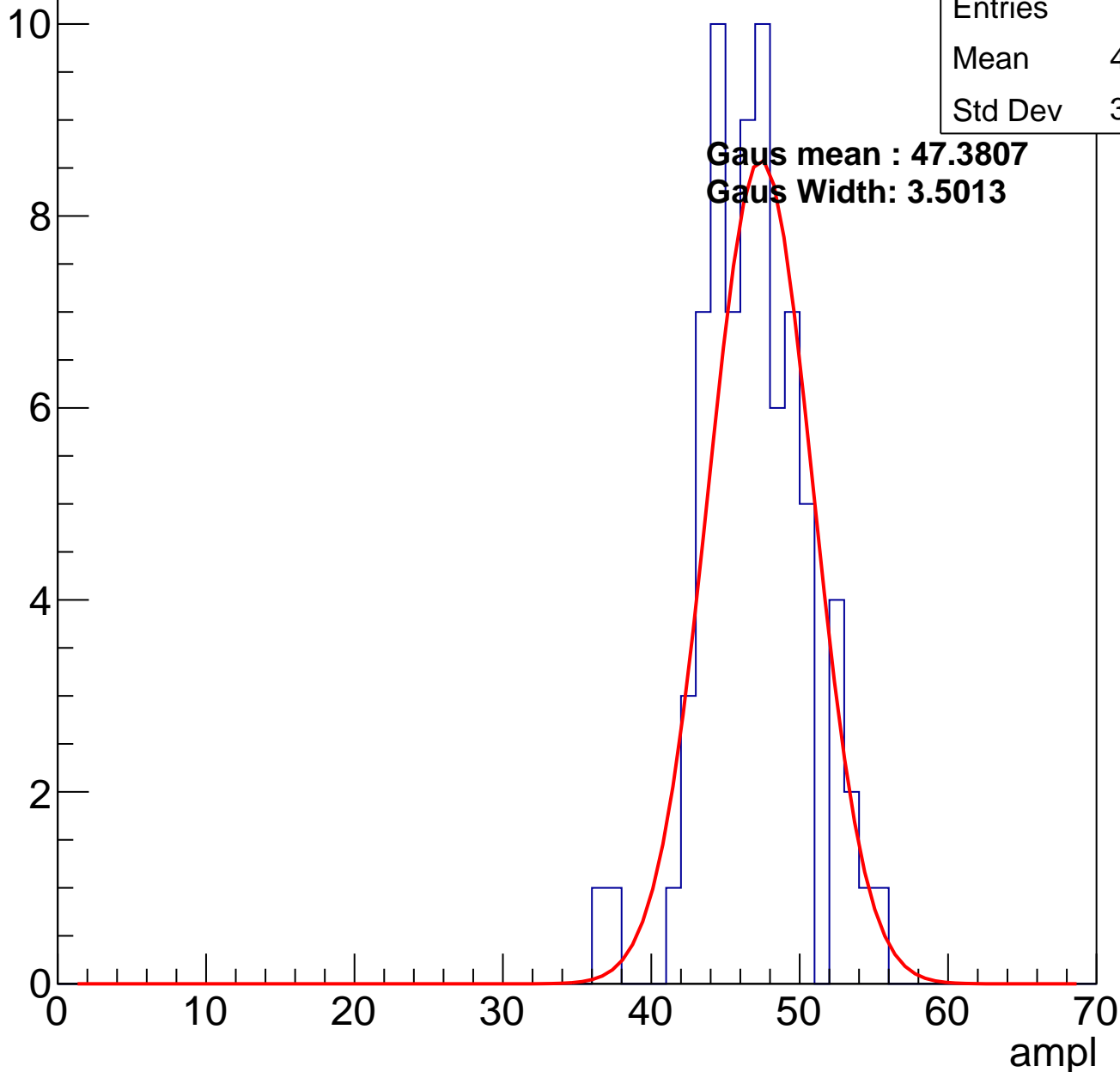
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entries	75
Mean	46.45
Std Dev	3.488

**Gaus mean : 47.3807**

**Gaus Width: 3.5013**

Entry

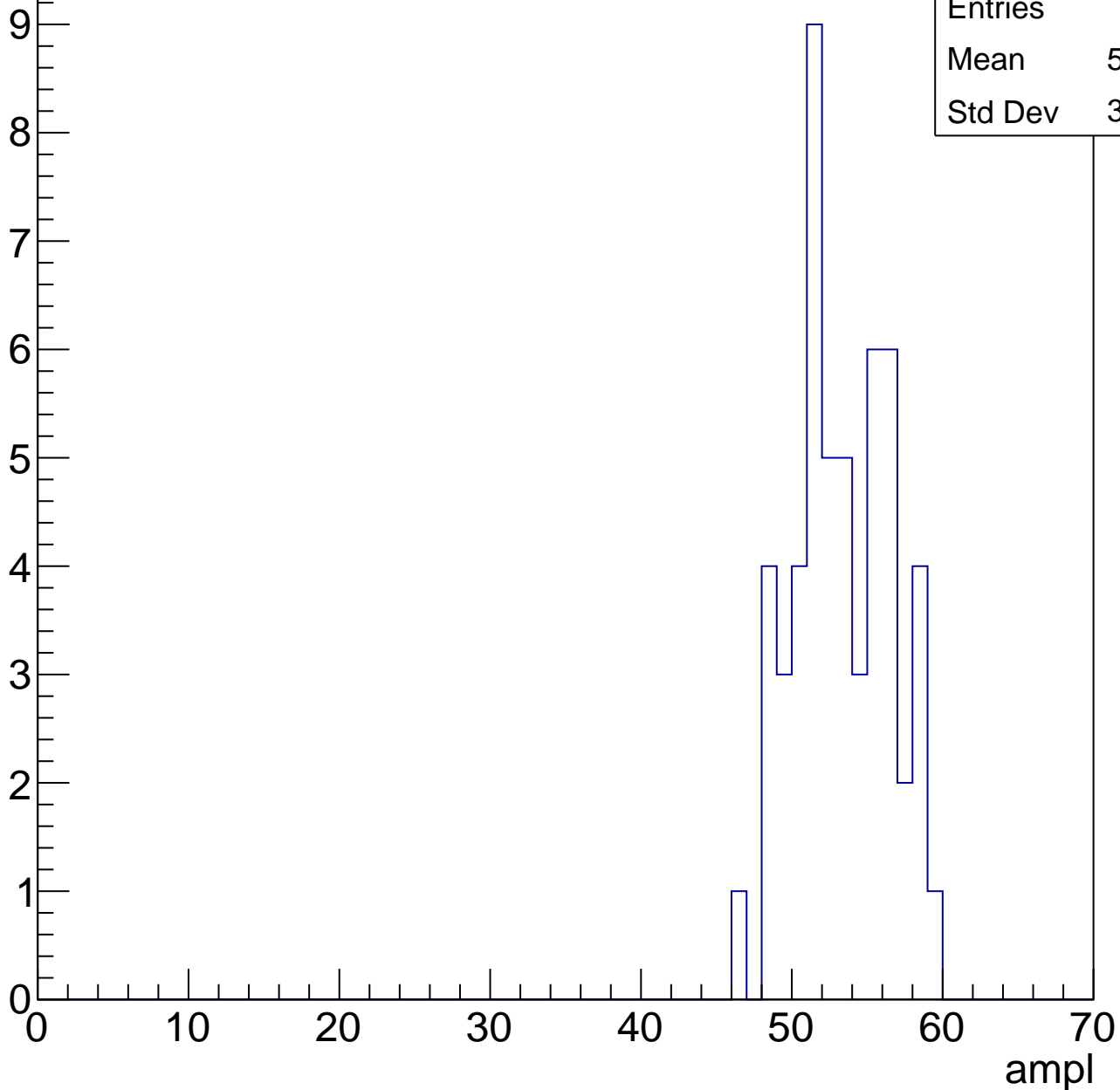


# B0L002S, U2-ch71, adc3

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	53
Mean	52.87
Std Dev	3.139

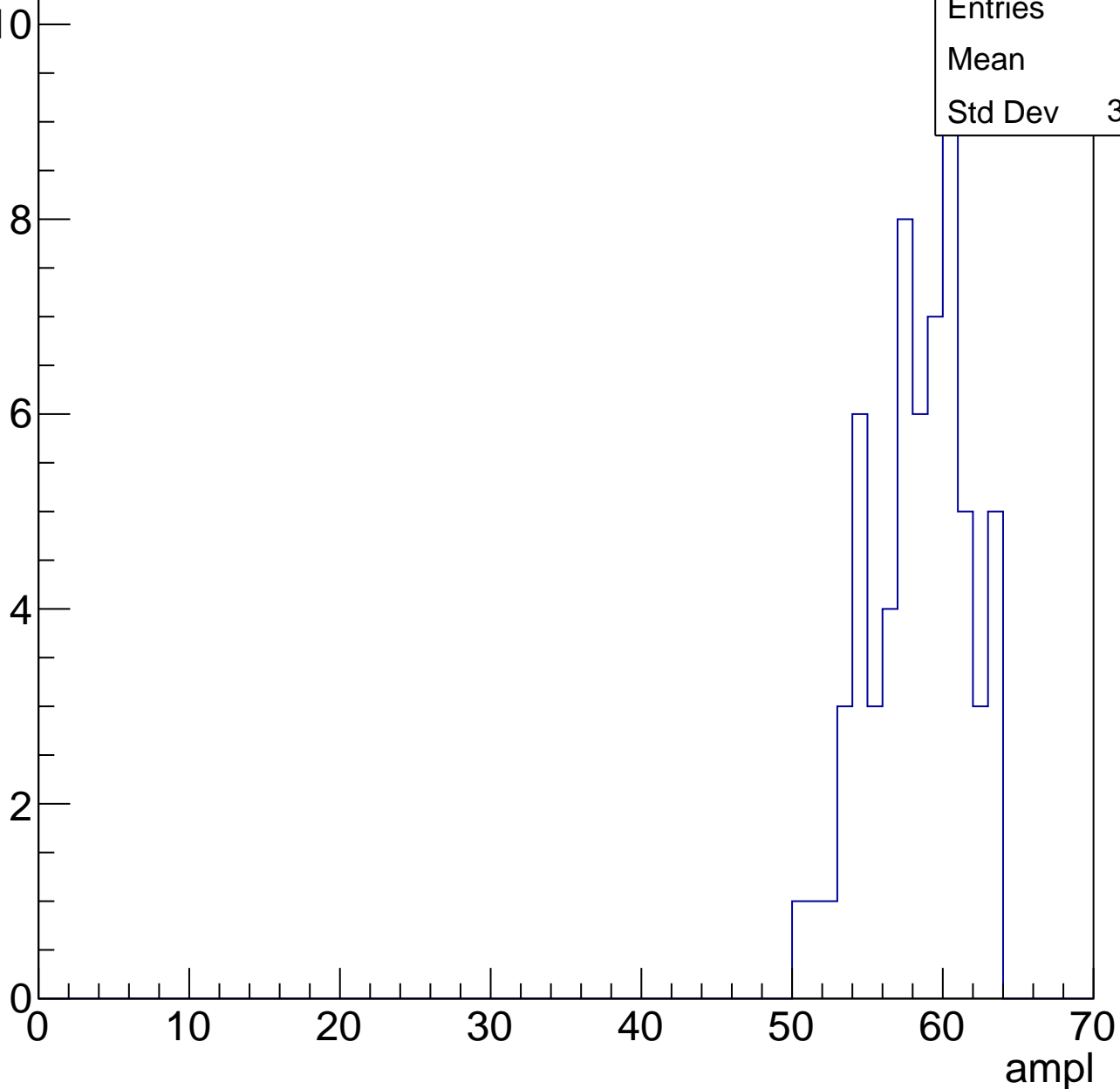


# B0L002S, U2-ch71, adc4

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	63
Mean	57.9
Std Dev	3.176

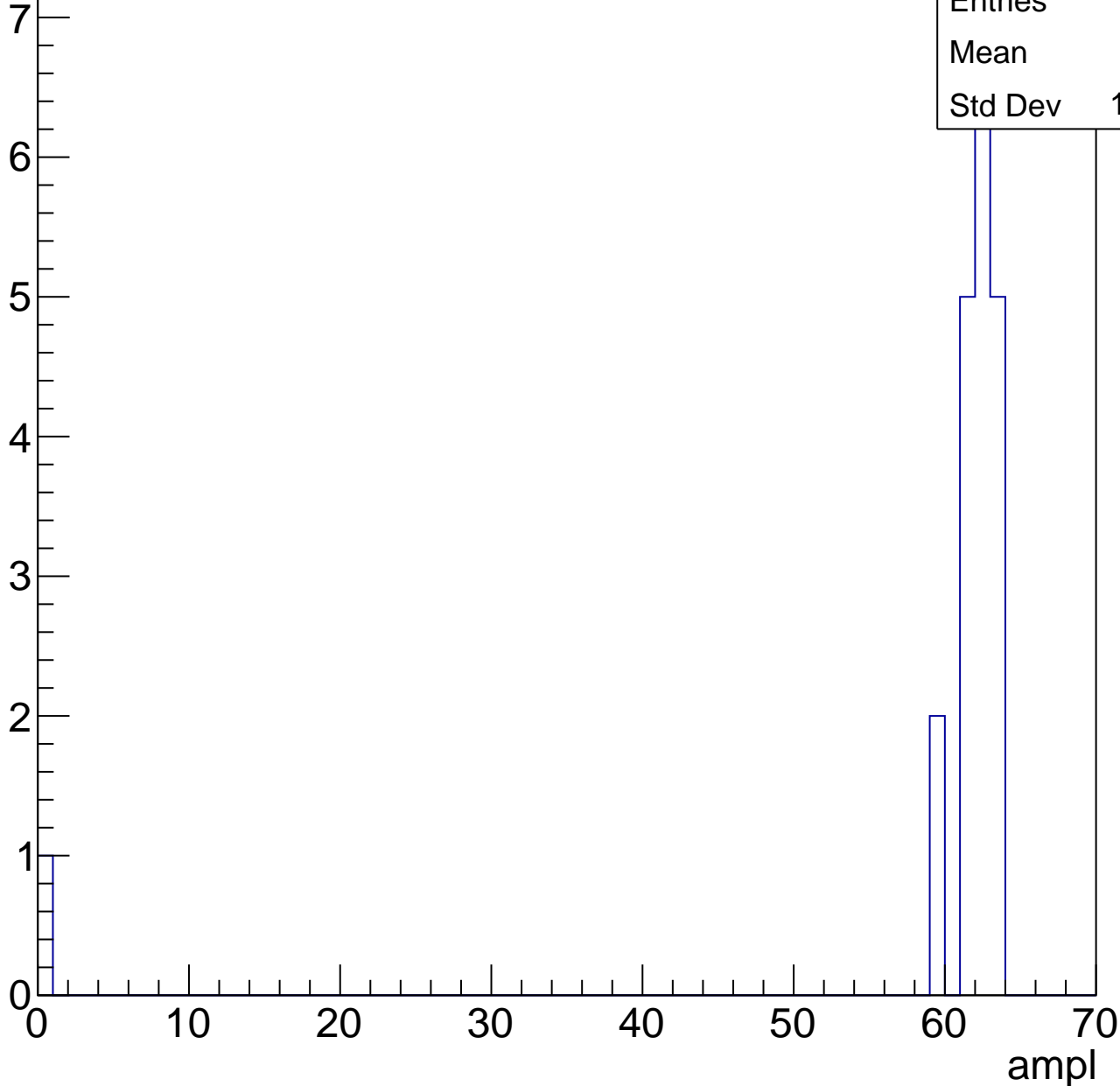


# B0L002S, U2-ch71, adc5

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	20
Mean	58.6
Std Dev	13.49



# B0L002S, U2-ch71, adc6

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



Entries	0
Mean	0
Std Dev	0



# B0L002S, U2-ch71, adc7

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



Entries	3
Mean	0
Std Dev	0

# B0L002S, U2-ch72, adc0

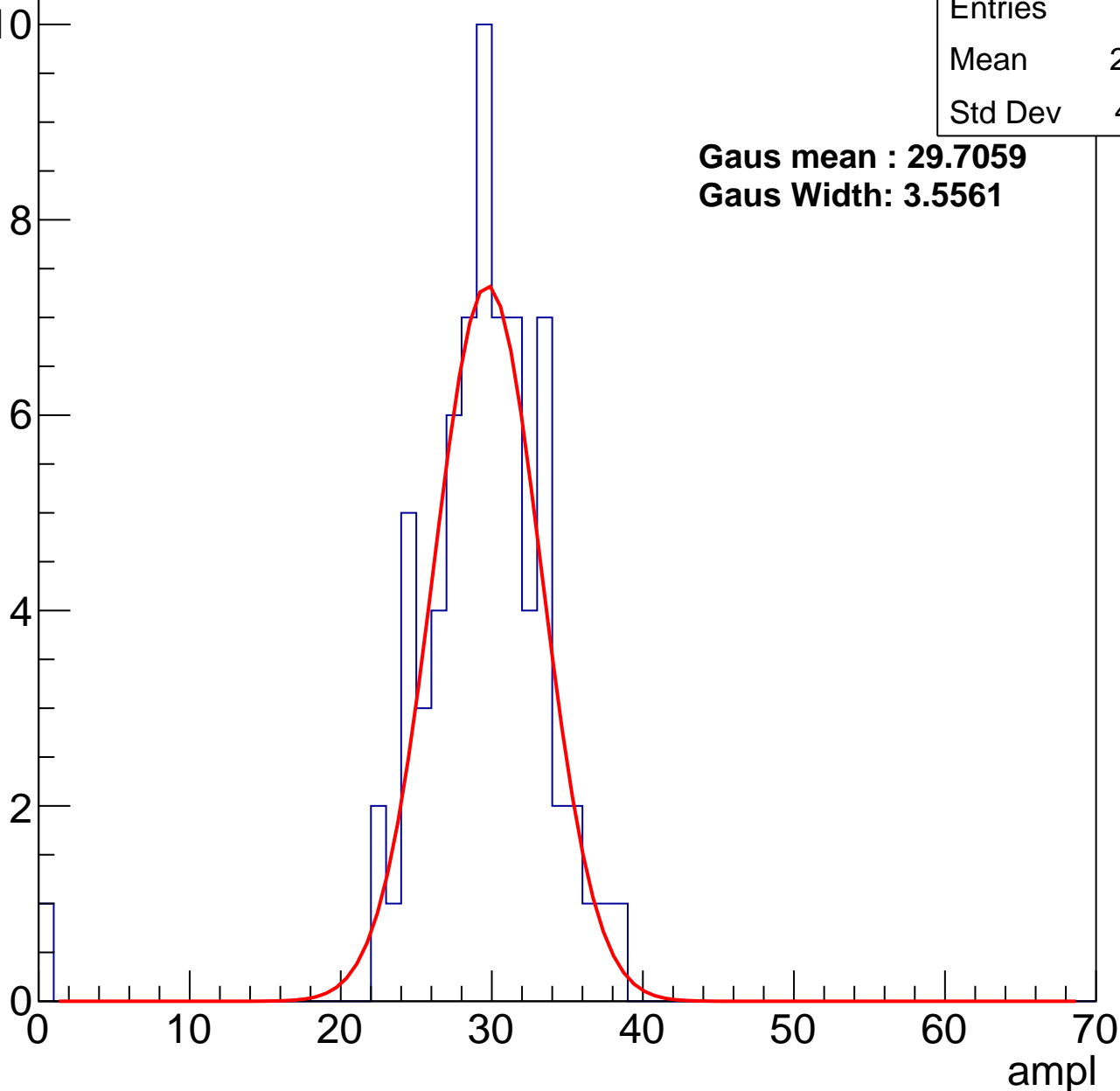
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	71
Mean	28.86
Std Dev	4.911

**Gaus mean : 29.7059**

**Gaus Width: 3.5561**



# B0L002S, U2-ch72, adc1

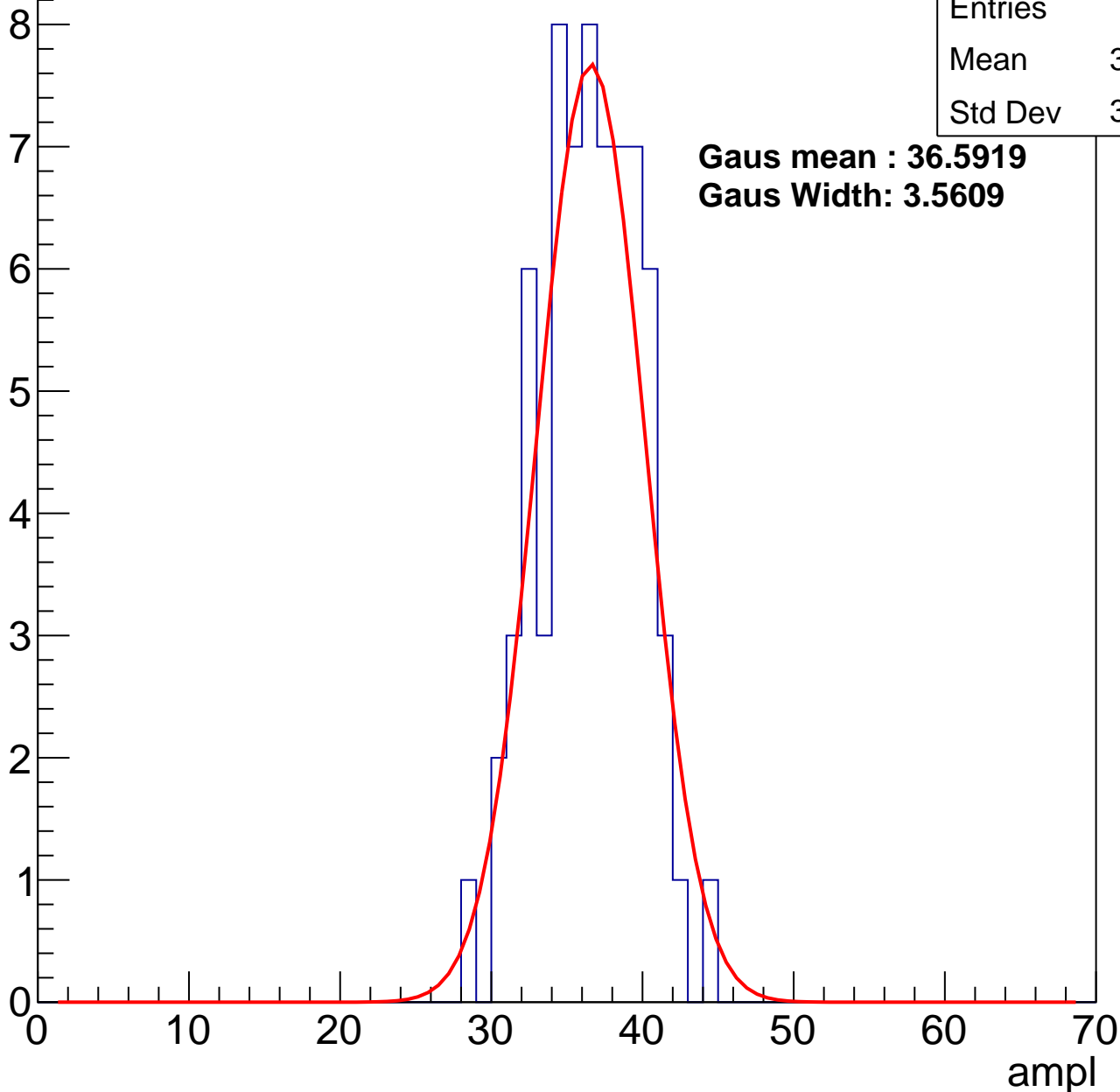
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	70
Mean	36.06
Std Dev	3.255

**Gaus mean : 36.5919**

**Gaus Width: 3.5609**



# B0L002S, U2-ch72, adc2

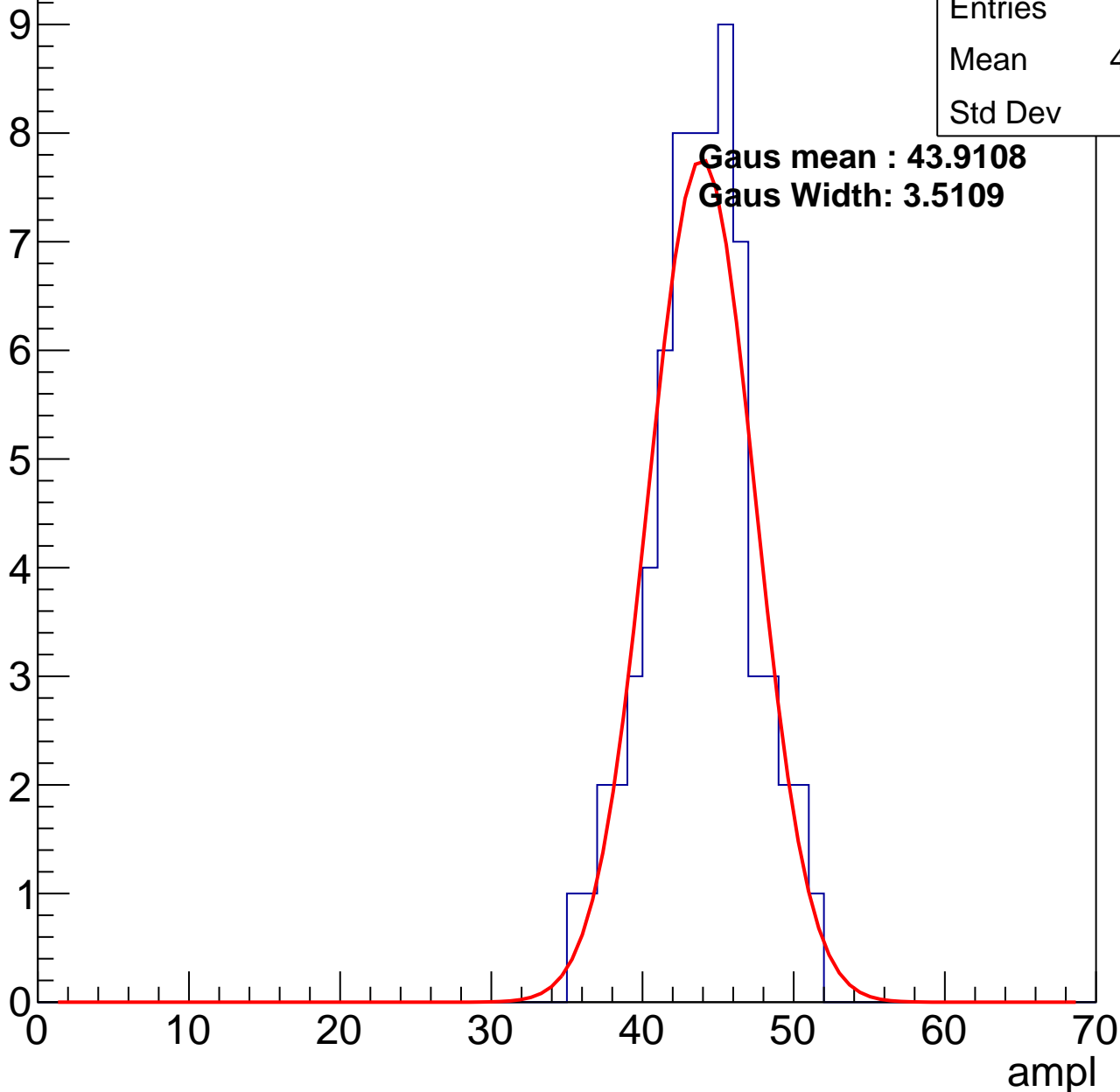
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	70
Mean	43.39
Std Dev	3.39

**Gaus mean : 43.9108**

**Gaus Width: 3.5109**

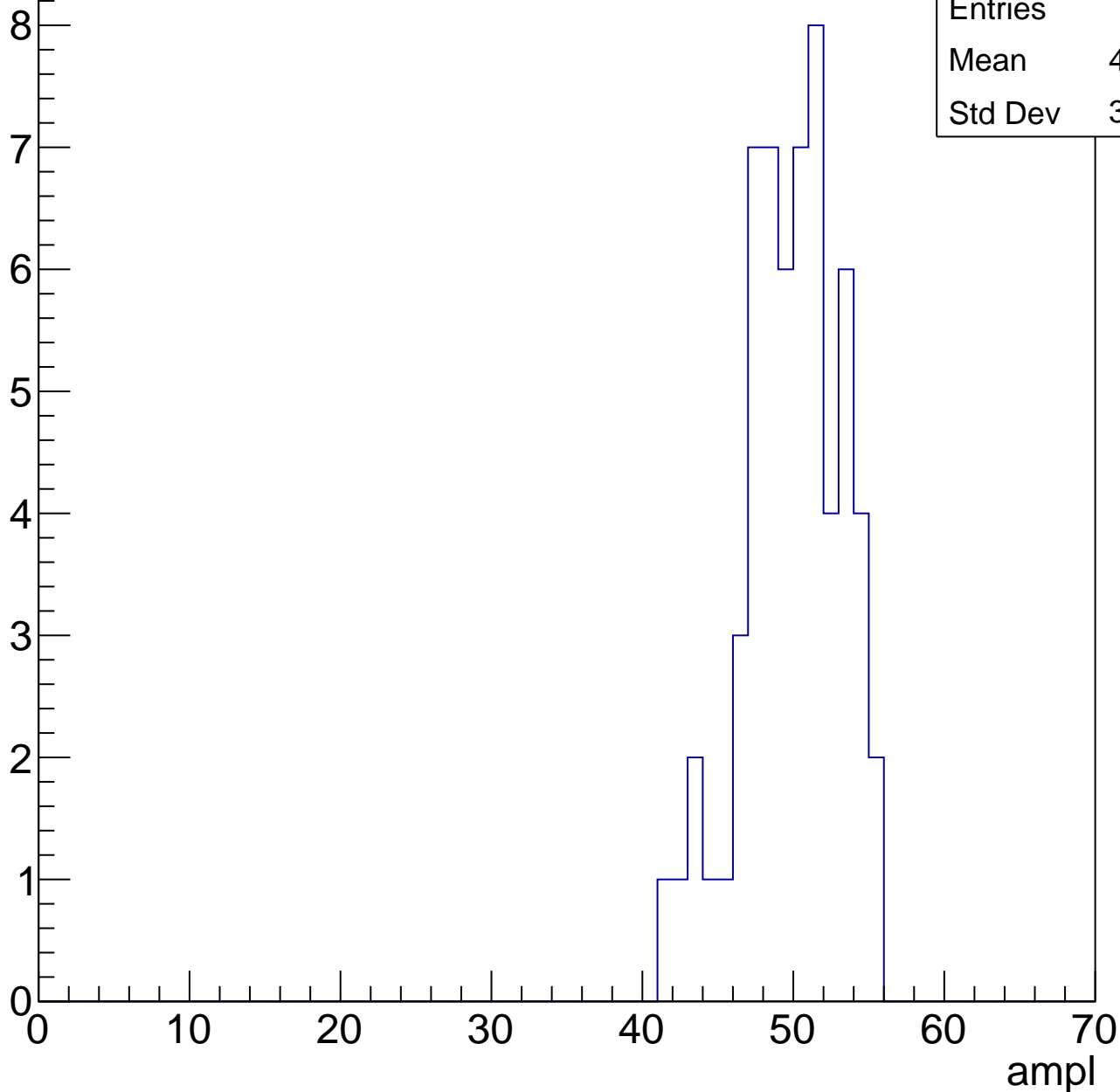


# B0L002S, U2-ch72, adc3

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	60
Mean	49.42
Std Dev	3.216

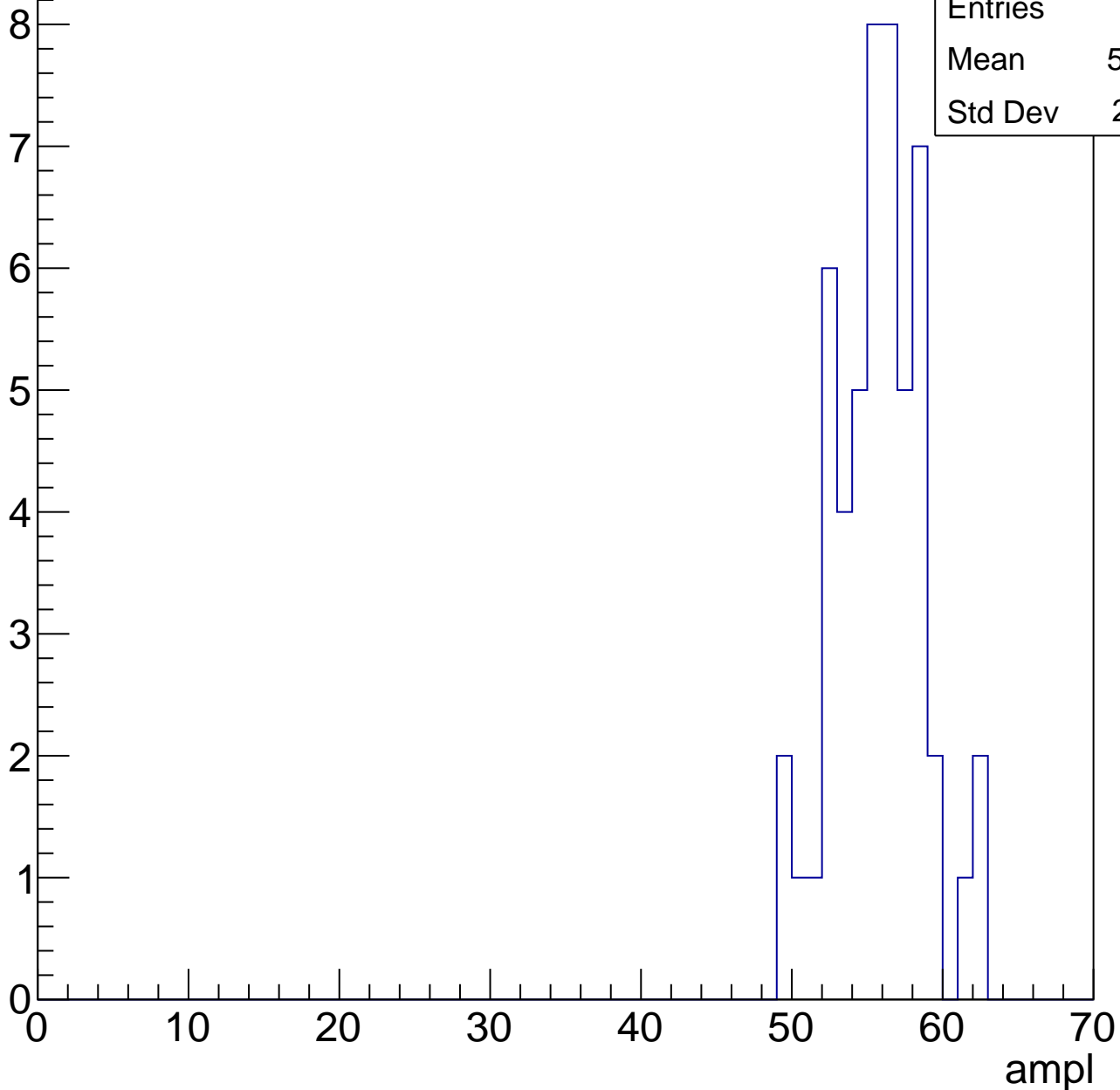


# B0L002S, U2-ch72, adc4

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	52
Mean	55.29
Std Dev	2.911



# B0L002S, U2-ch72, adc5

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

10

Entries 53

Mean 58.91

Std Dev 8.439

8

6

4

2

0

0

10

20

30

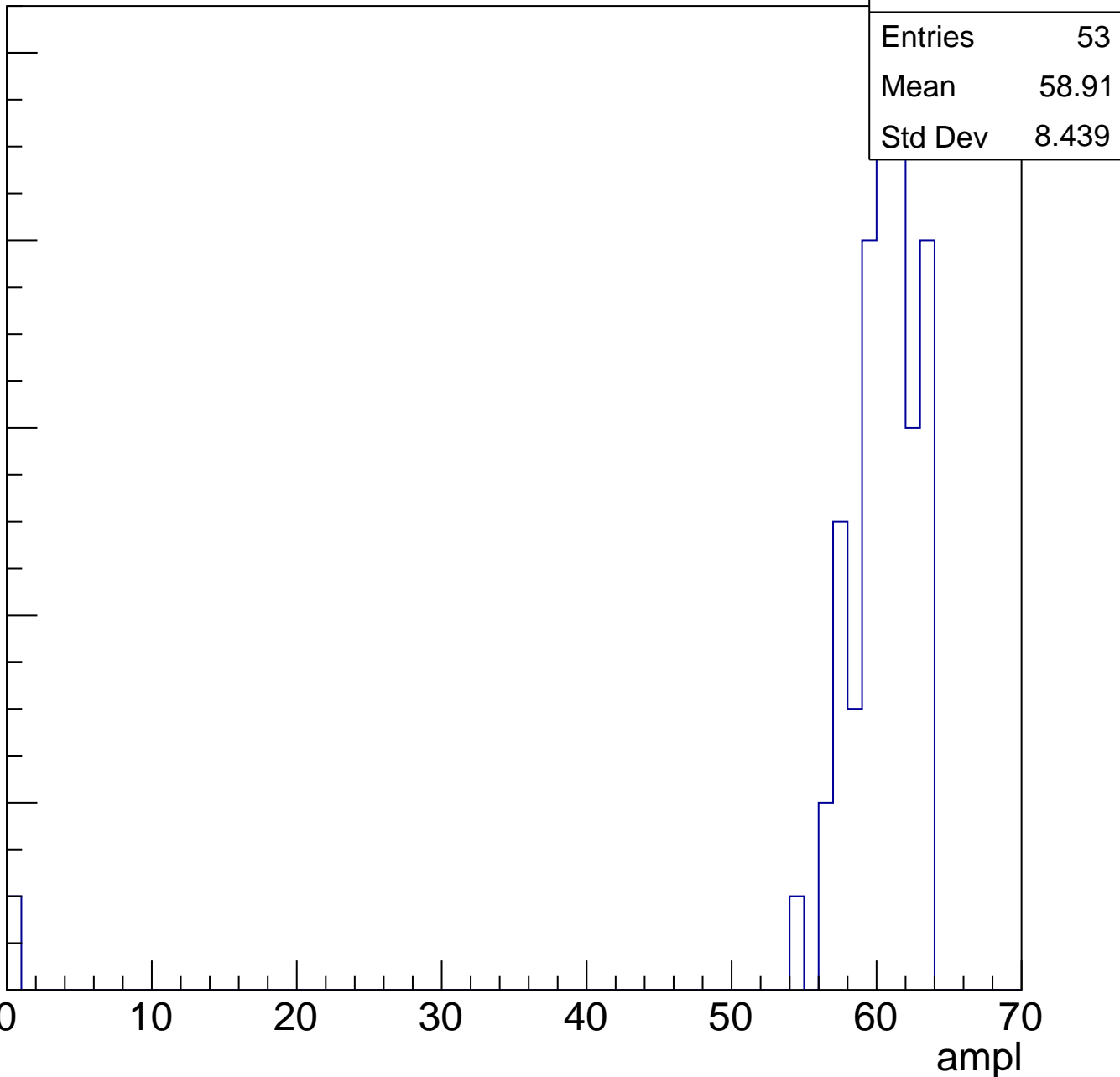
40

50

60

70

ampl



# B0L002S, U2-ch72, adc6

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	4
Mean	62.5
Std Dev	0.5

0 10 20 30 40 50 60 70

ampl



# B0L002S, U2-ch72, adc7

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L002S, U2-ch73, adc0

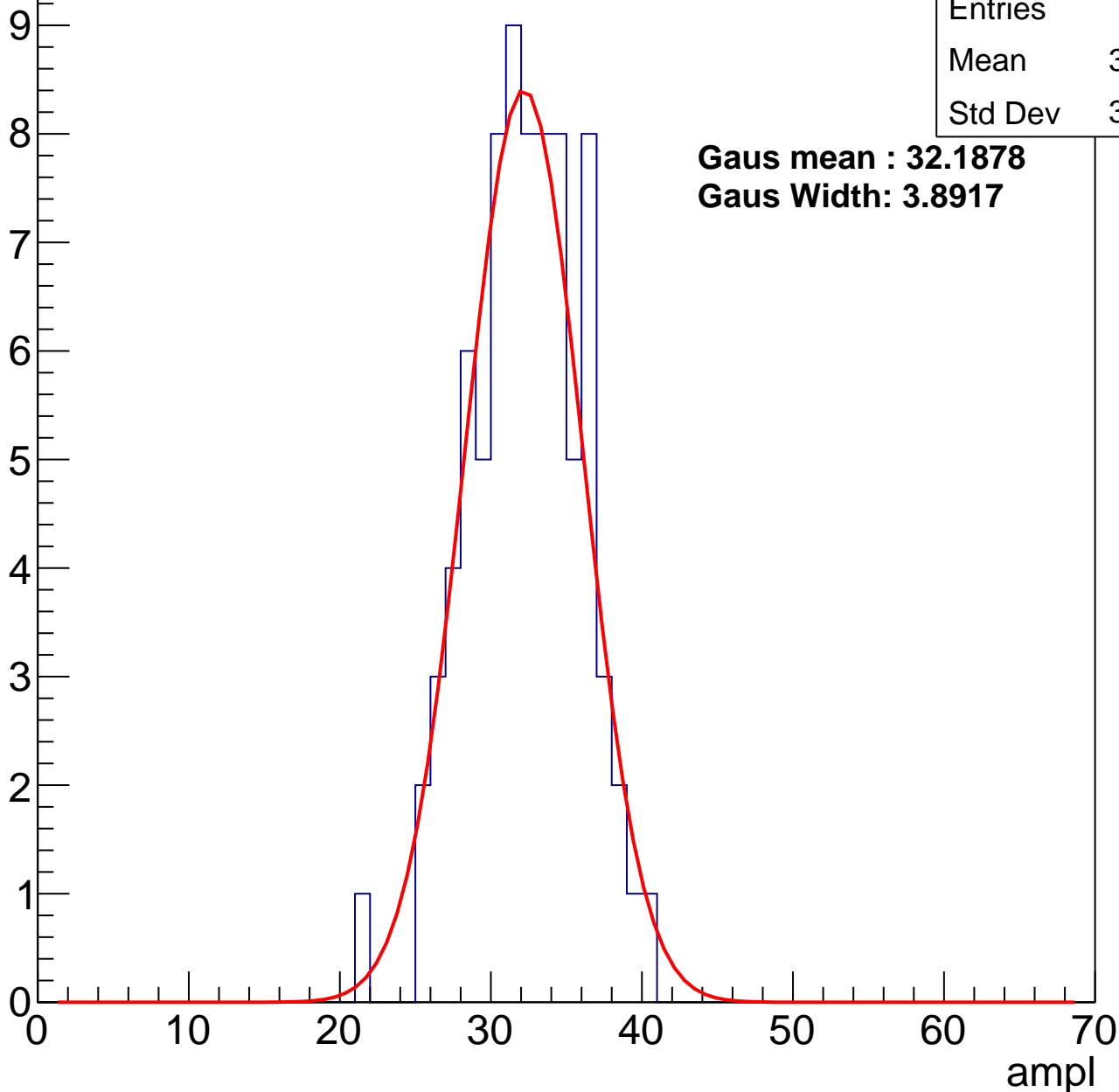
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	82
Mean	31.83
Std Dev	3.628

**Gaus mean : 32.1878**

**Gaus Width: 3.8917**



# B0L002S, U2-ch73, adc1

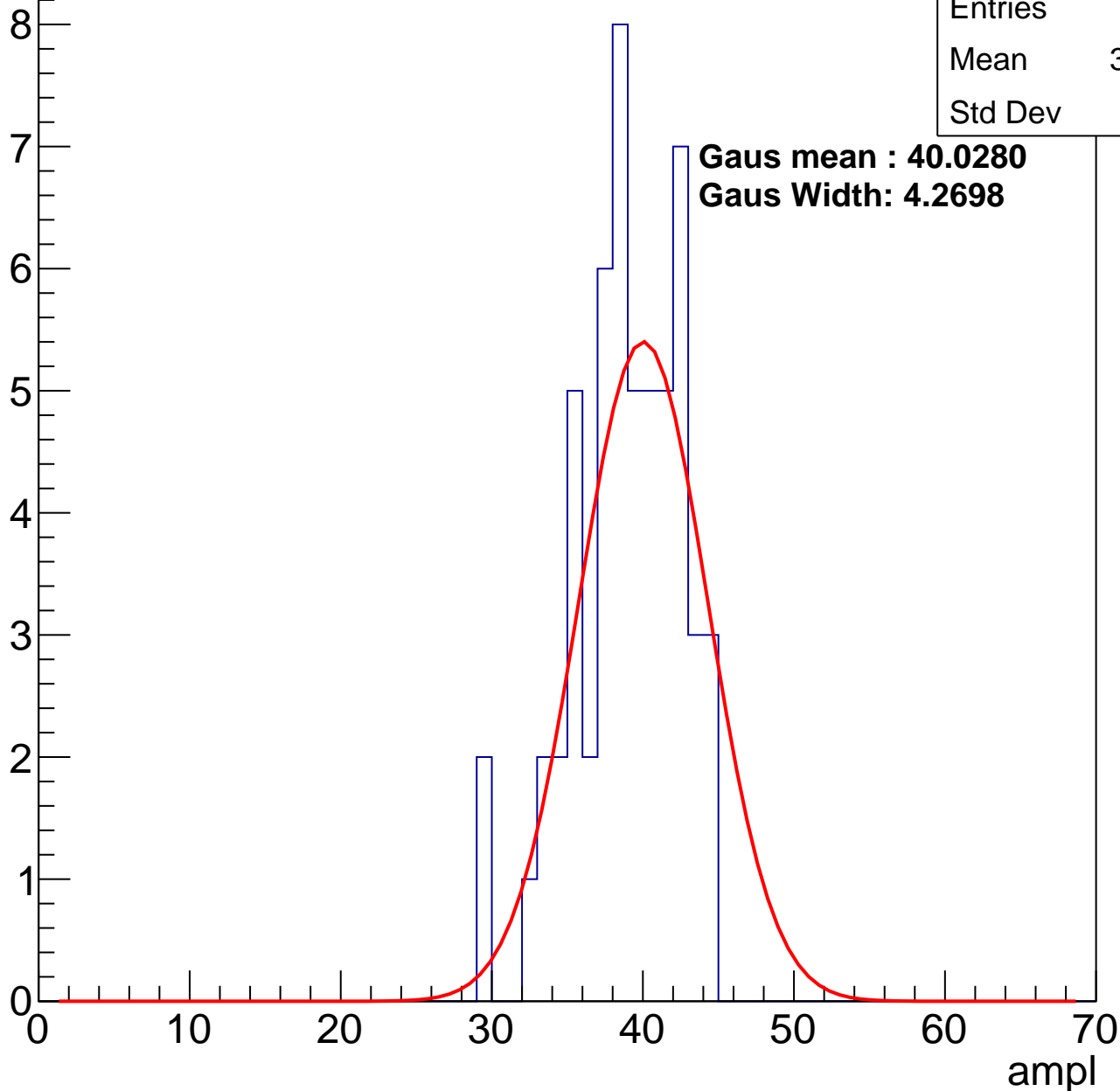
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	56
Mean	38.43
Std Dev	3.52

**Gaus mean : 40.0280**

**Gaus Width: 4.2698**



# B0L002S, U2-ch73, adc2

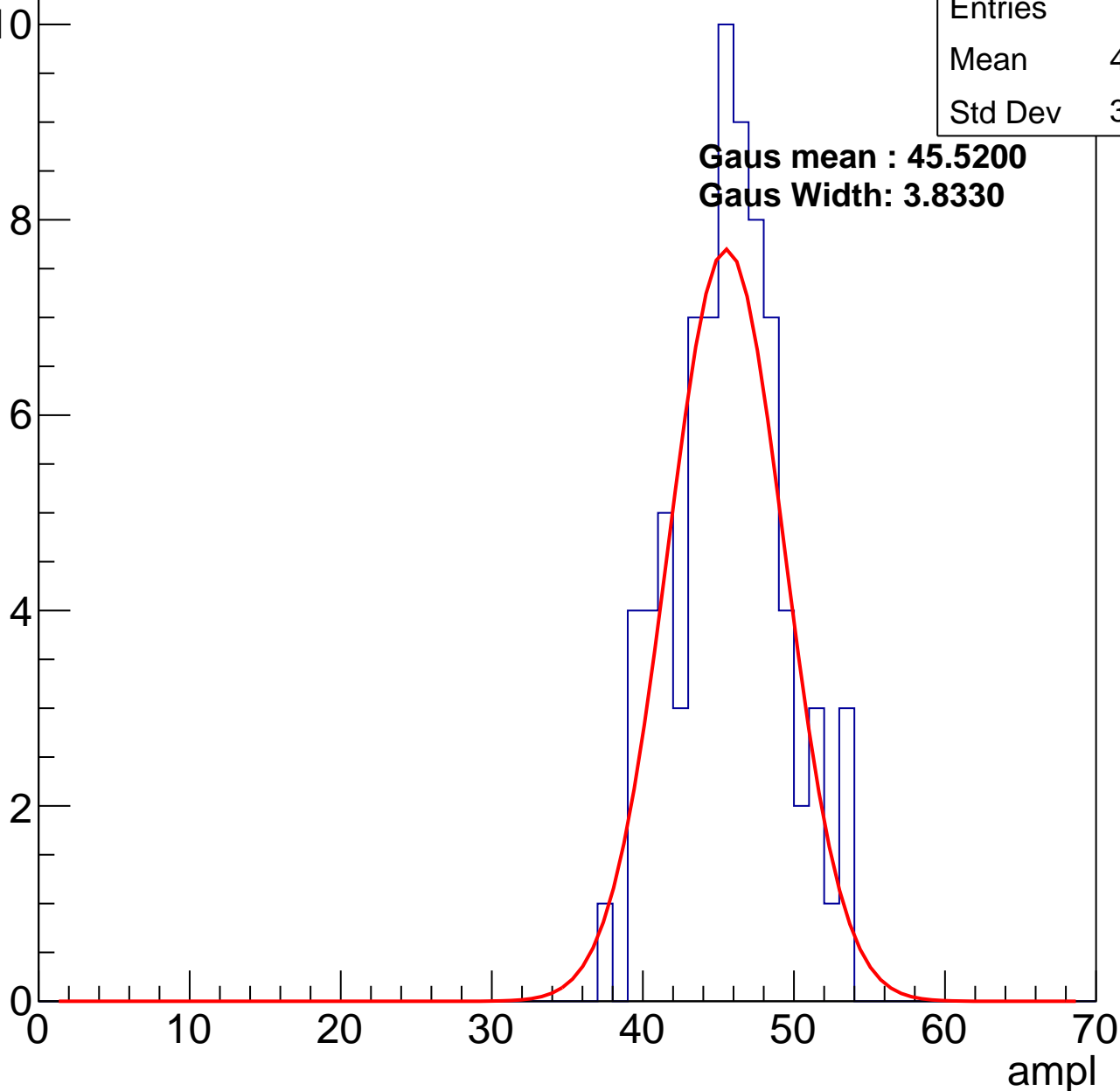
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	78
Mean	45.24
Std Dev	3.603

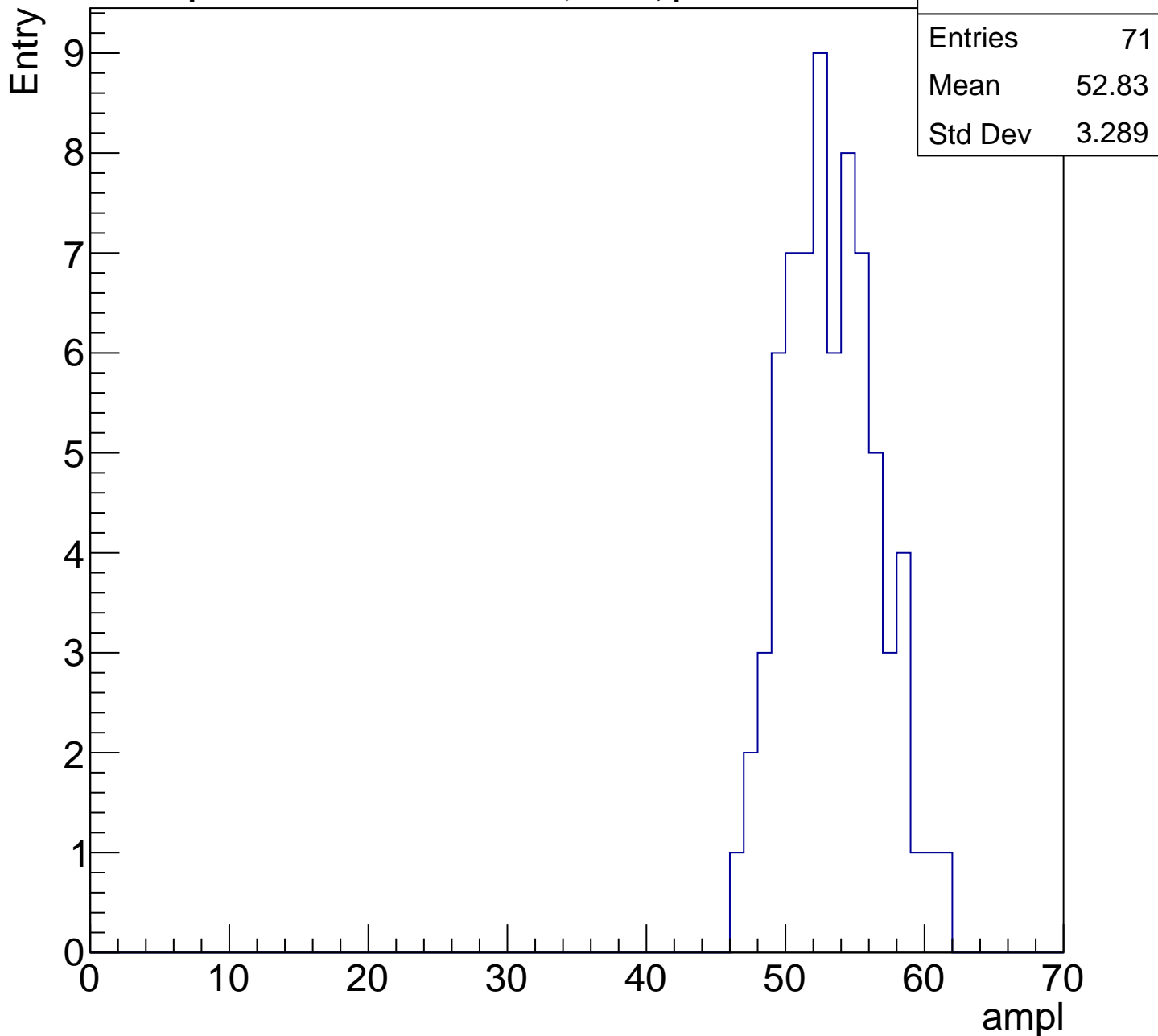
**Gaus mean : 45.5200**

**Gaus Width: 3.8330**



# B0L002S, U2-ch73, adc3

calib\_packv5\_042523\_0143.root, FC#8, port C1



# B0L002S, U2-ch73, adc4

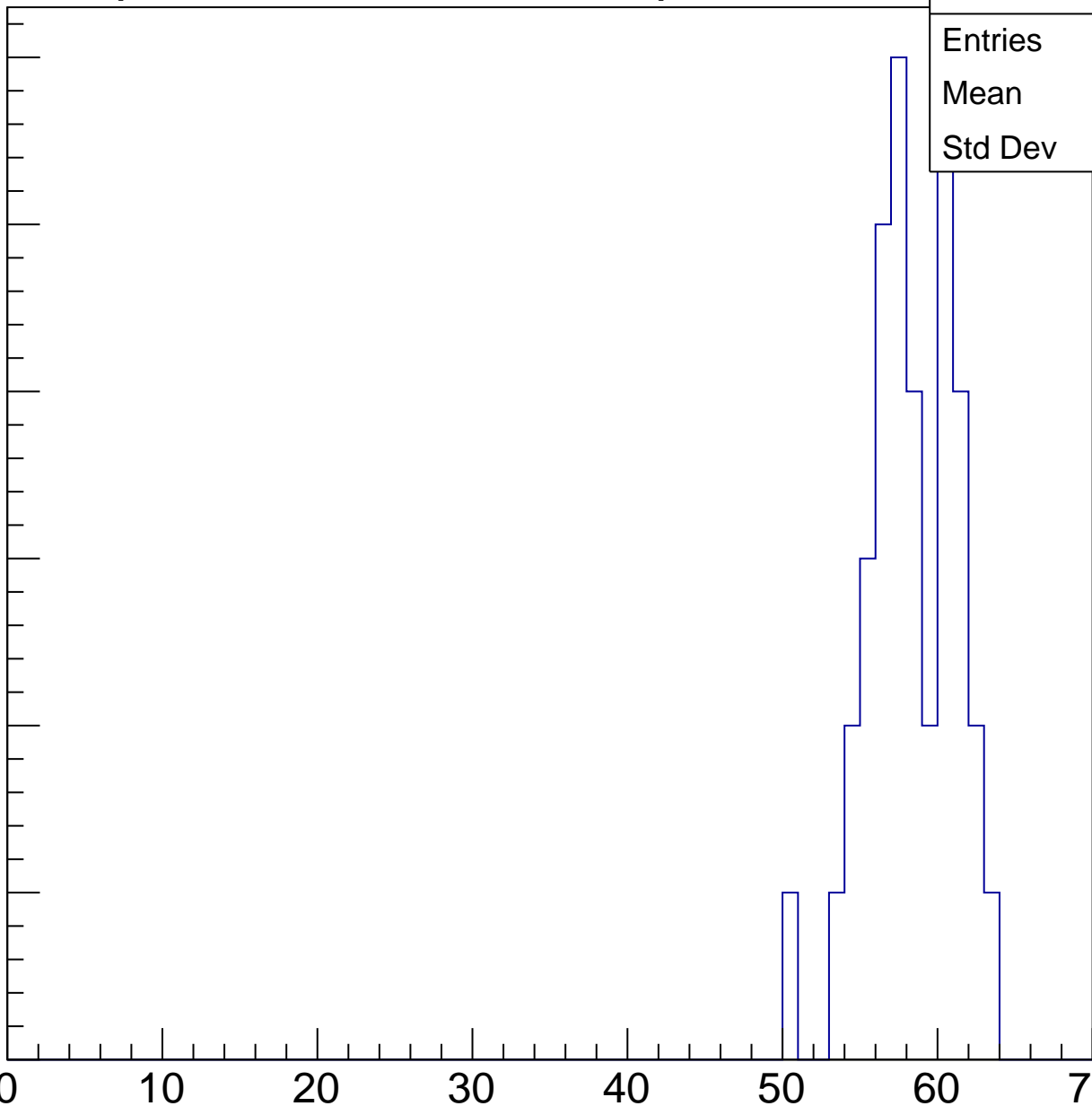
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

6  
5  
4  
3  
2  
1  
0

Entries	37
Mean	57.81
Std Dev	2.808

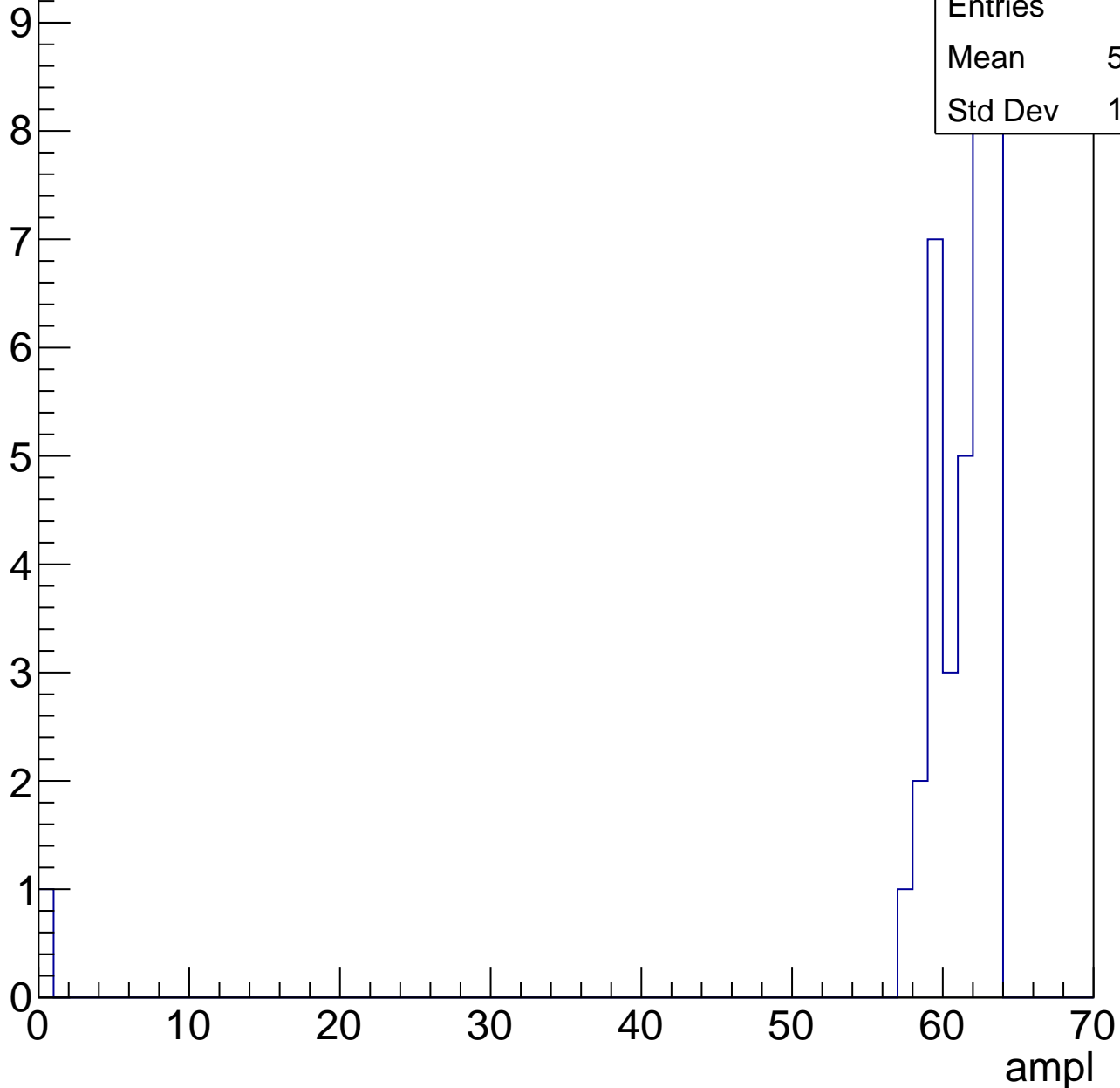
ampl



# B0L002S, U2-ch73, adc5

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



# B0L002S, U2-ch73, adc6

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry





# B0L002S, U2-ch73, adc7

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L002S, U2-ch74, adc0

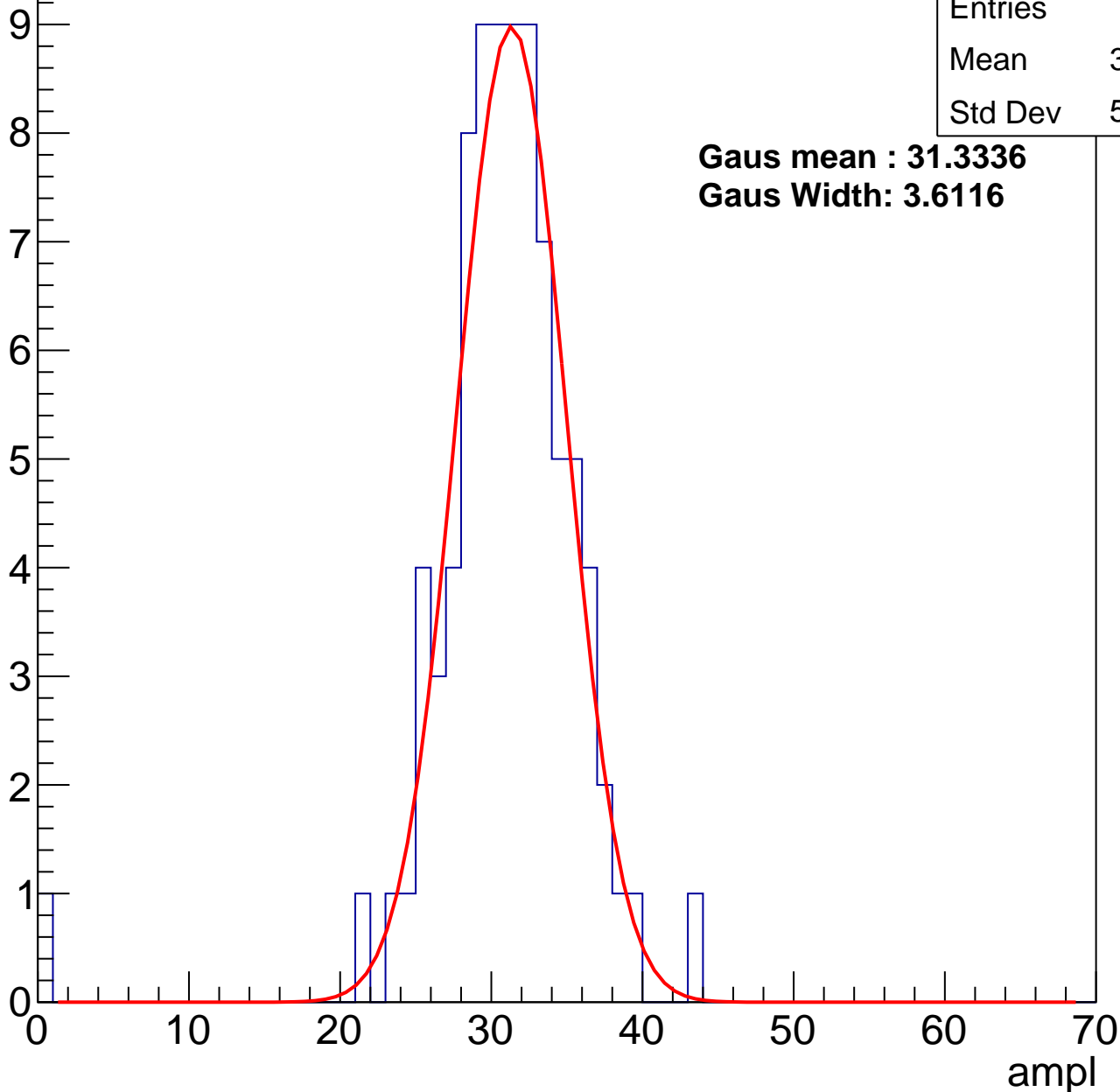
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	85
Mean	30.47
Std Dev	5.019

**Gaus mean : 31.3336**

**Gaus Width: 3.6116**



# B0L002S, U2-ch74, adc1

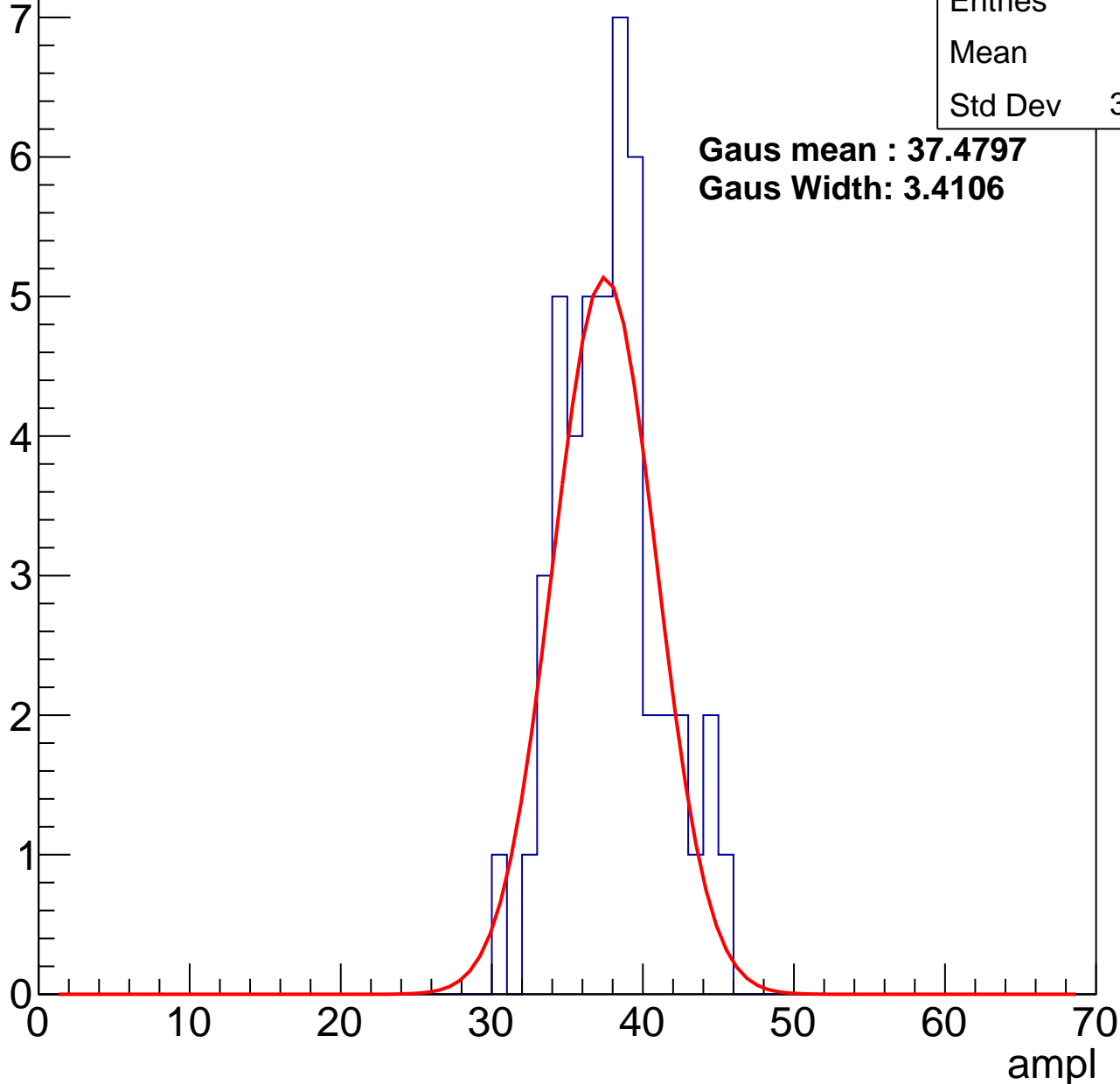
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	47
Mean	37.4
Std Dev	3.292

**Gaus mean : 37.4797**

**Gaus Width: 3.4106**



# B0L002S, U2-ch74, adc2

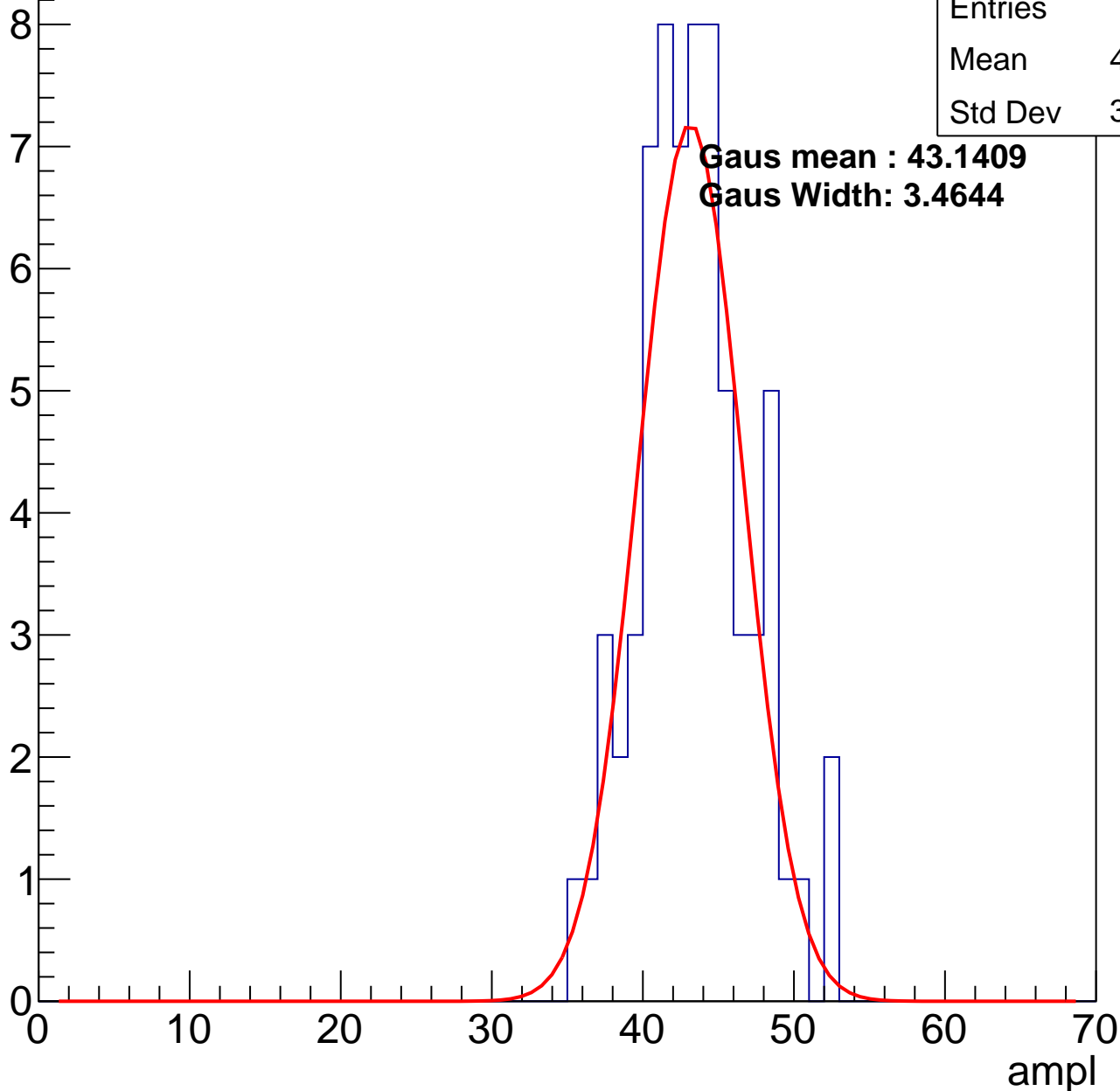
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	68
Mean	42.94
Std Dev	3.629

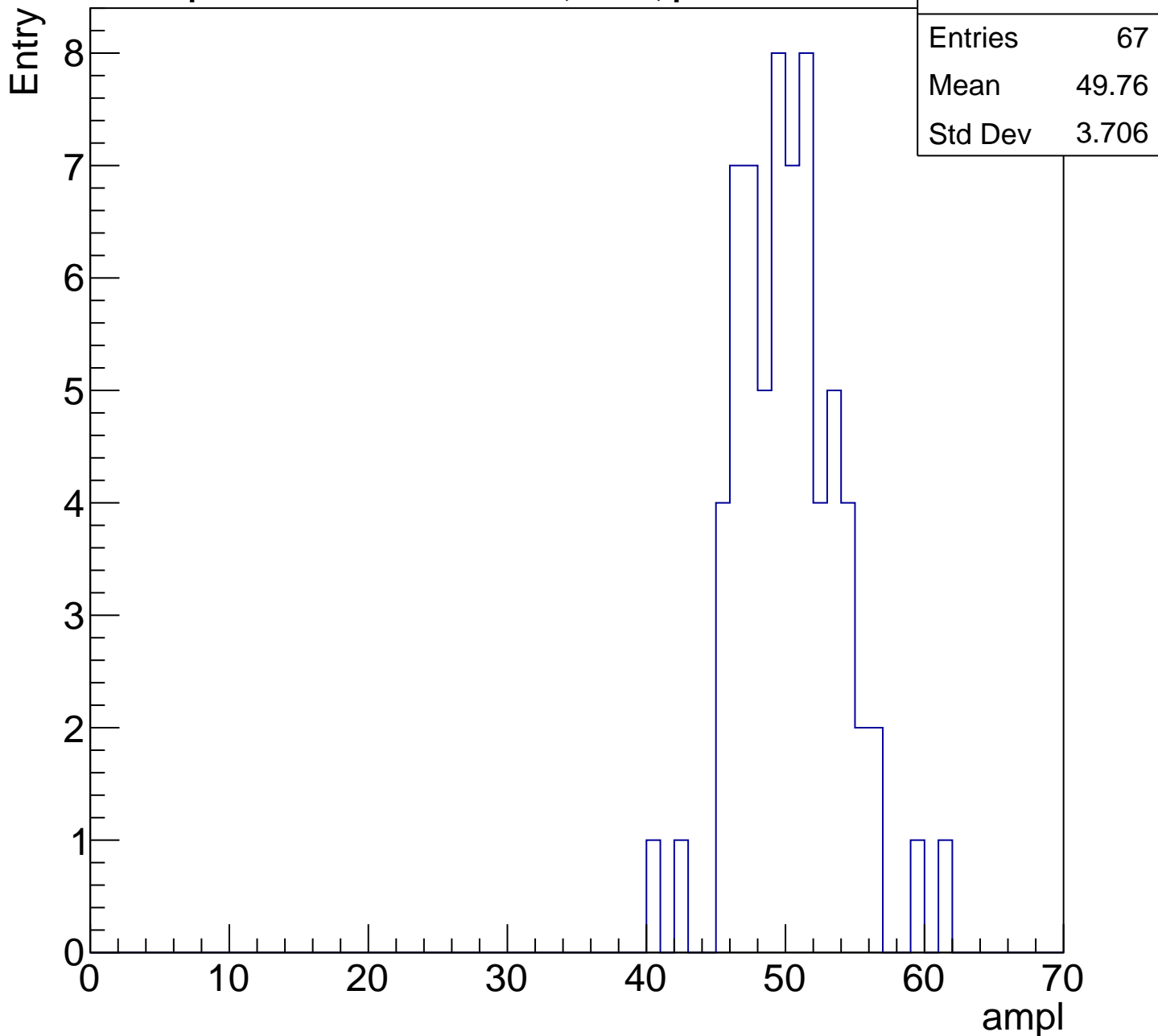
**Gaus mean : 43.1409**

**Gaus Width: 3.4644**



# B0L002S, U2-ch74, adc3

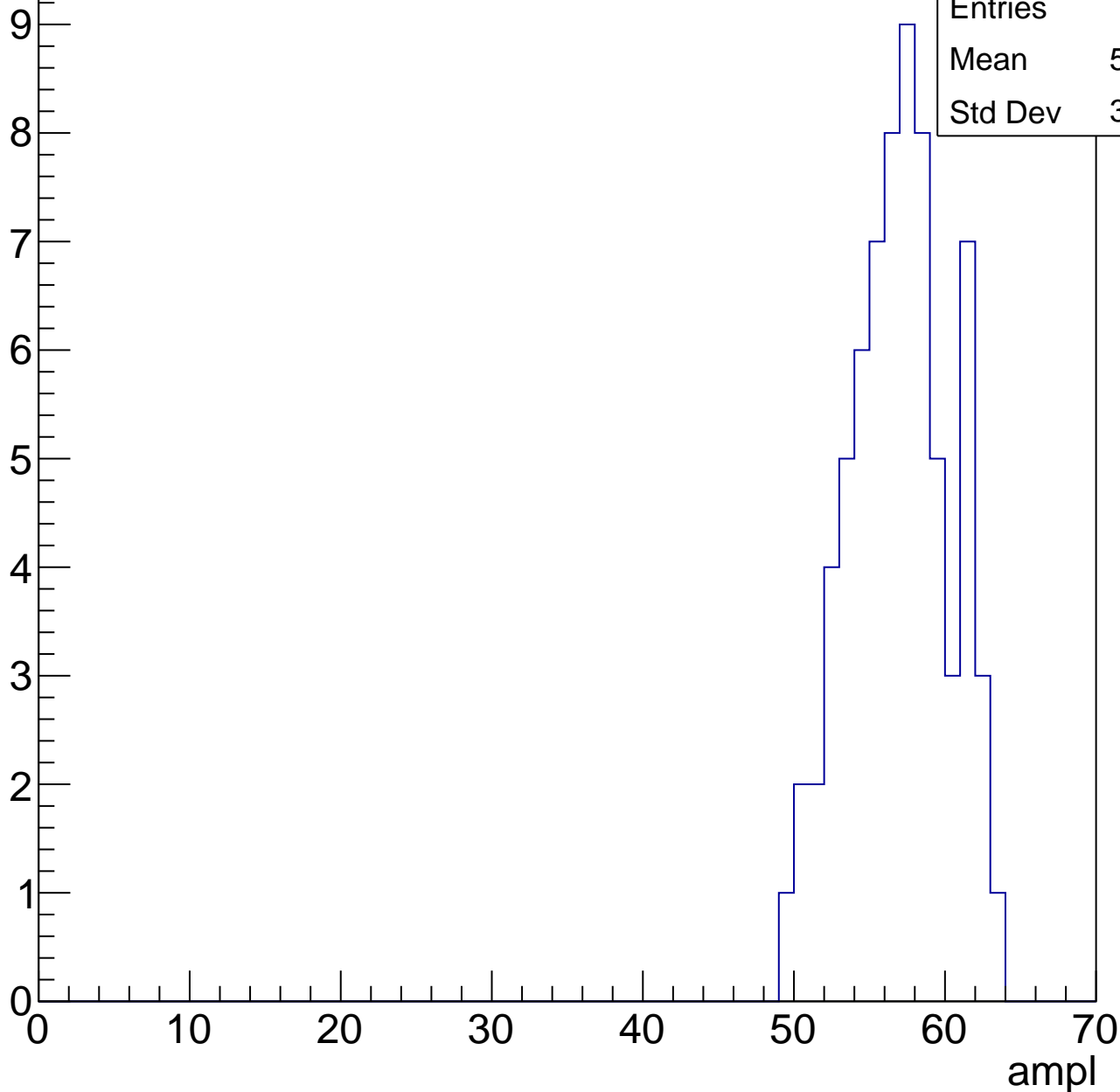
calib\_packv5\_042523\_0143.root, FC#8, port C1



# B0L002S, U2-ch74, adc4

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



# B0L002S, U2-ch74, adc5

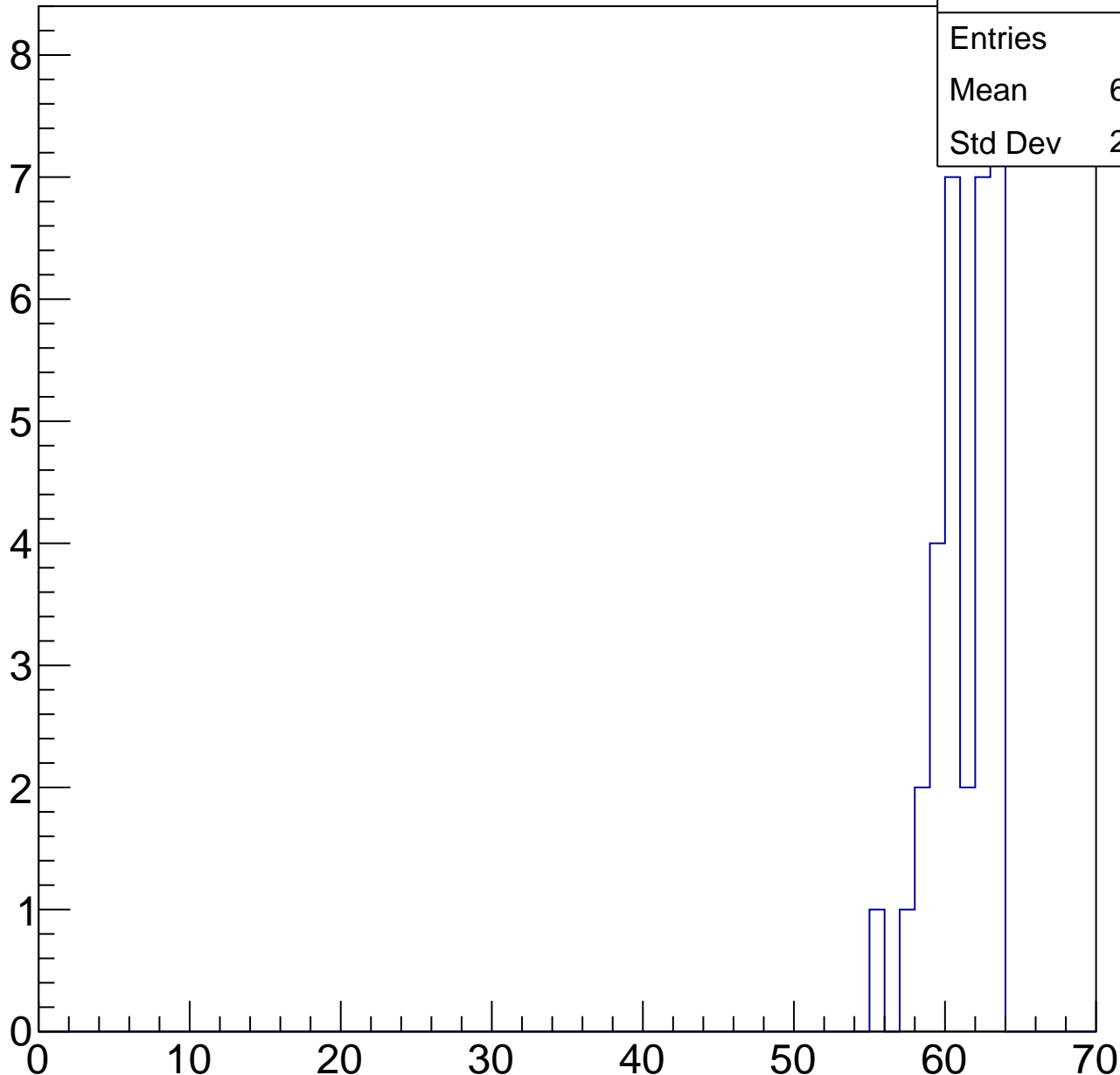
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	32
Mean	60.75
Std Dev	2.016

ampl



# B0L002S, U2-ch74, adc6

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry





# B0L002S, U2-ch74, adc7

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



# B0L002S, U2-ch75, adc0

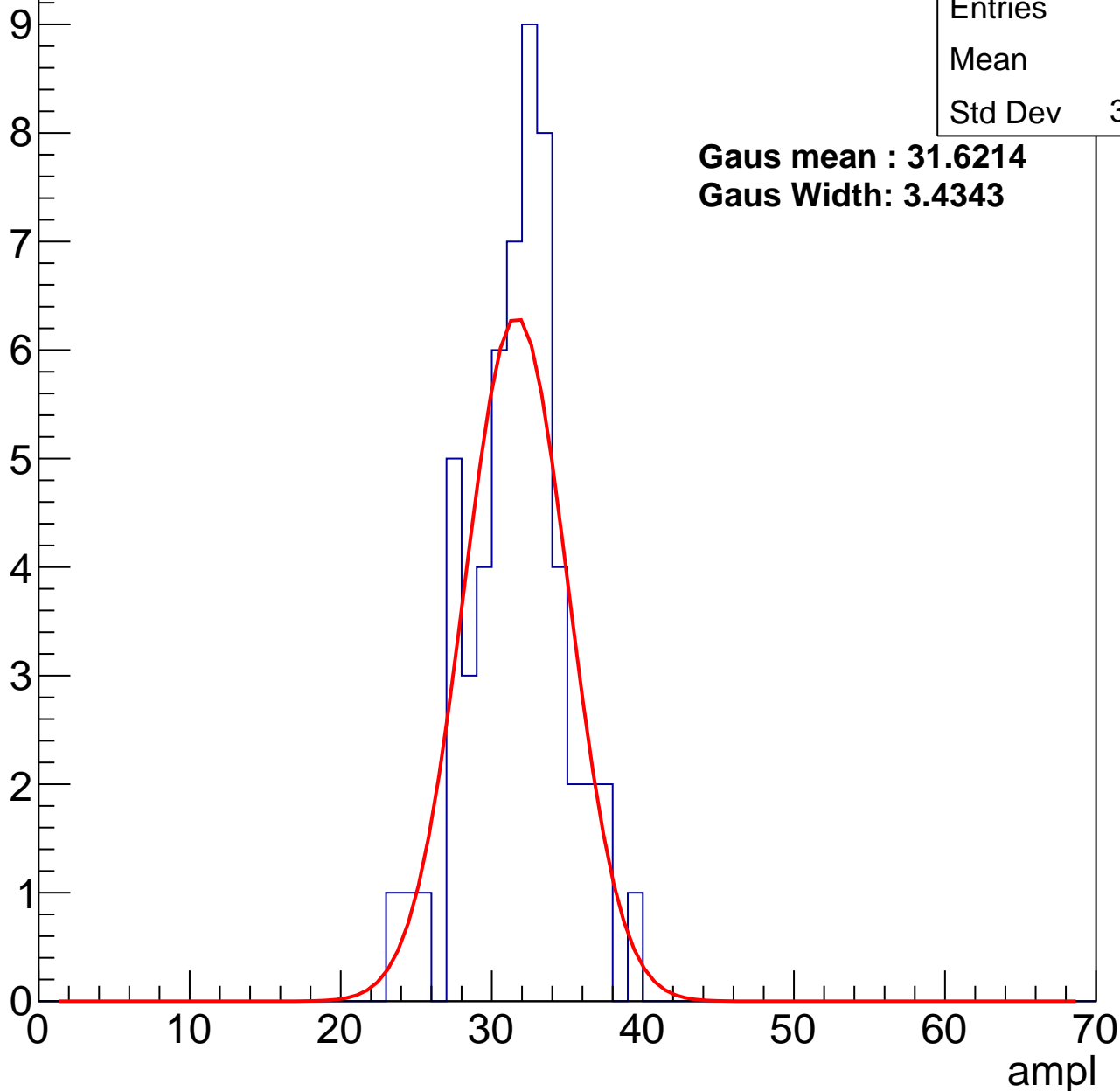
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	56
Mean	31.2
Std Dev	3.193

**Gaus mean : 31.6214**

**Gaus Width: 3.4343**



# B0L002S, U2-ch75, adc1

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	76
Mean	37.92
Std Dev	3.523

**Gaus mean : 38.5671**

**Gaus Width: 3.2810**

10

8

6

4

2

0

0

10

20

30

40

50

60

70

ampl



# B0L002S, U2-ch75, adc2

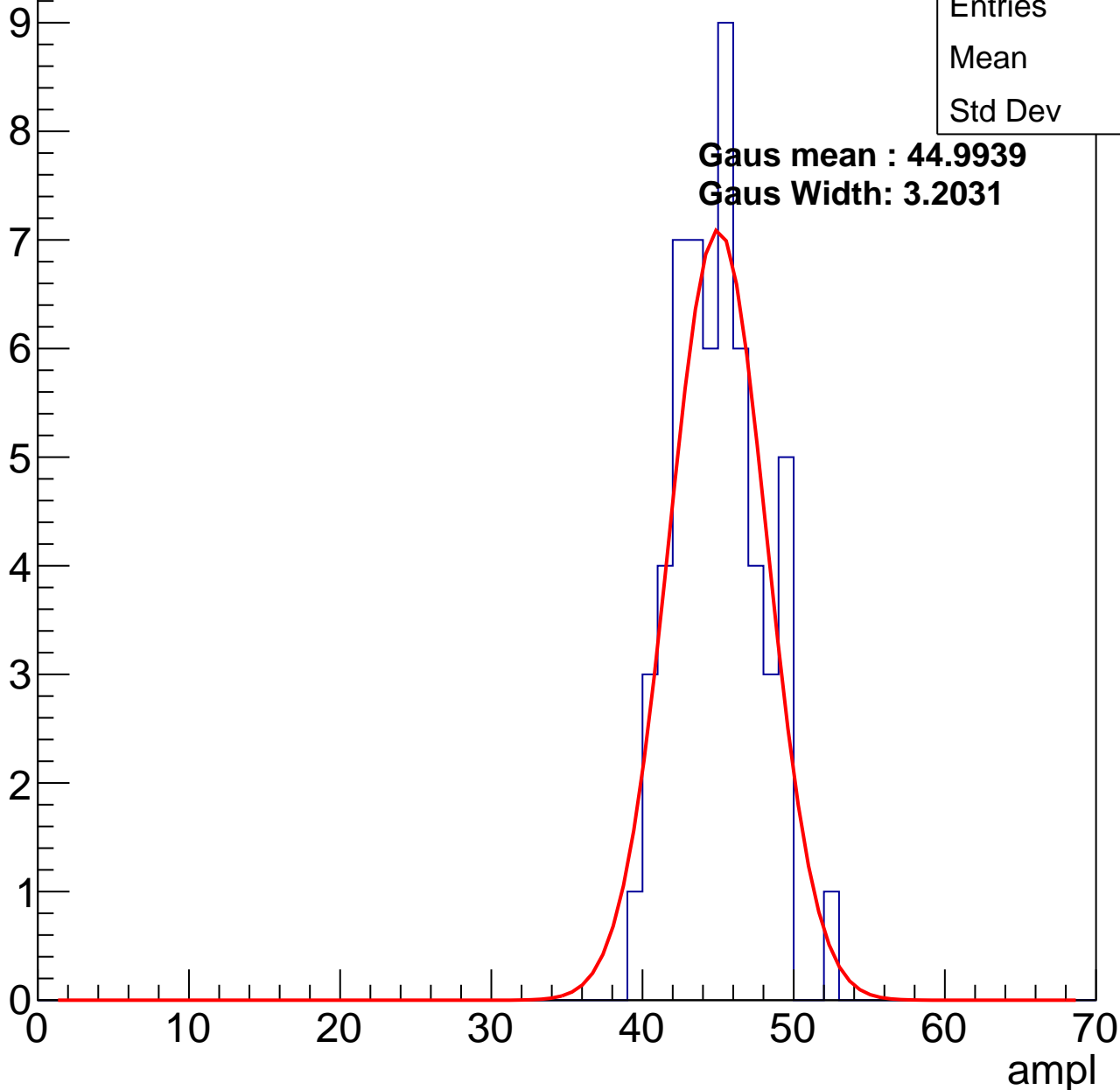
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	56
Mean	44.5
Std Dev	2.79

**Gaus mean : 44.9939**

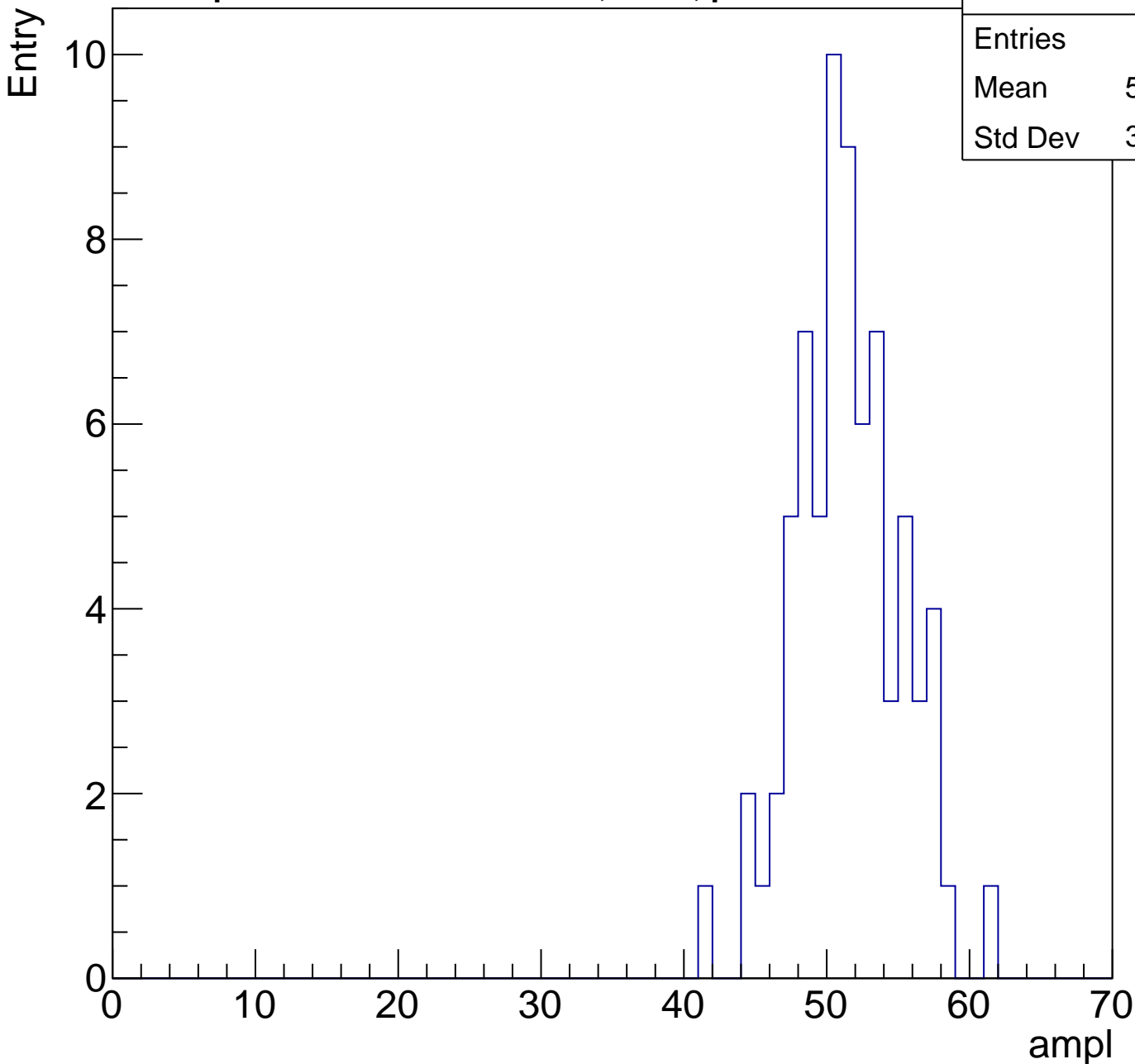
**Gaus Width: 3.2031**



# B0L002S, U2-ch75, adc3

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entries	72
Mean	51.06
Std Dev	3.662



# B0L002S, U2-ch75, adc4

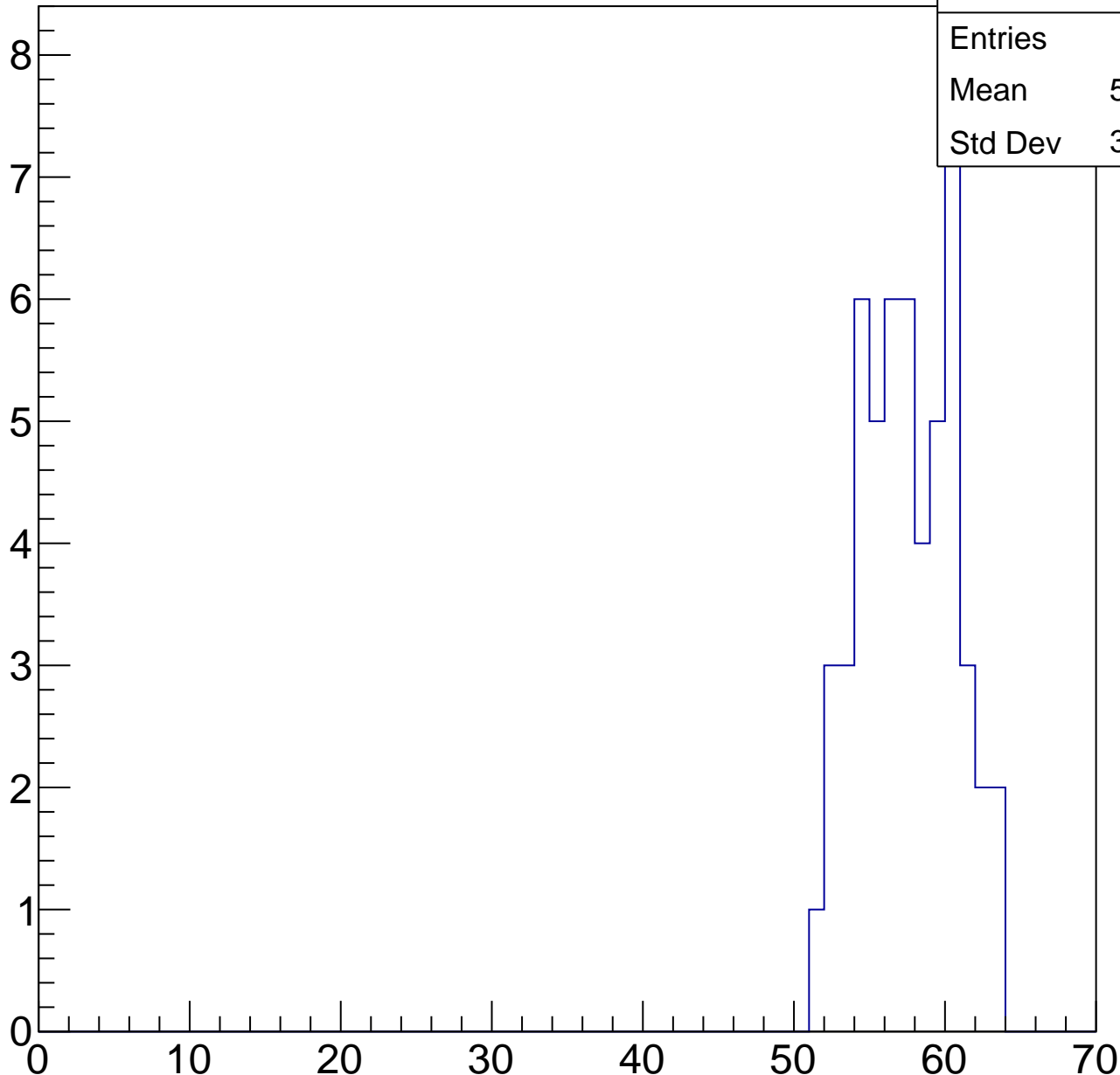
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	54
Mean	57.09
Std Dev	3.057

ampl

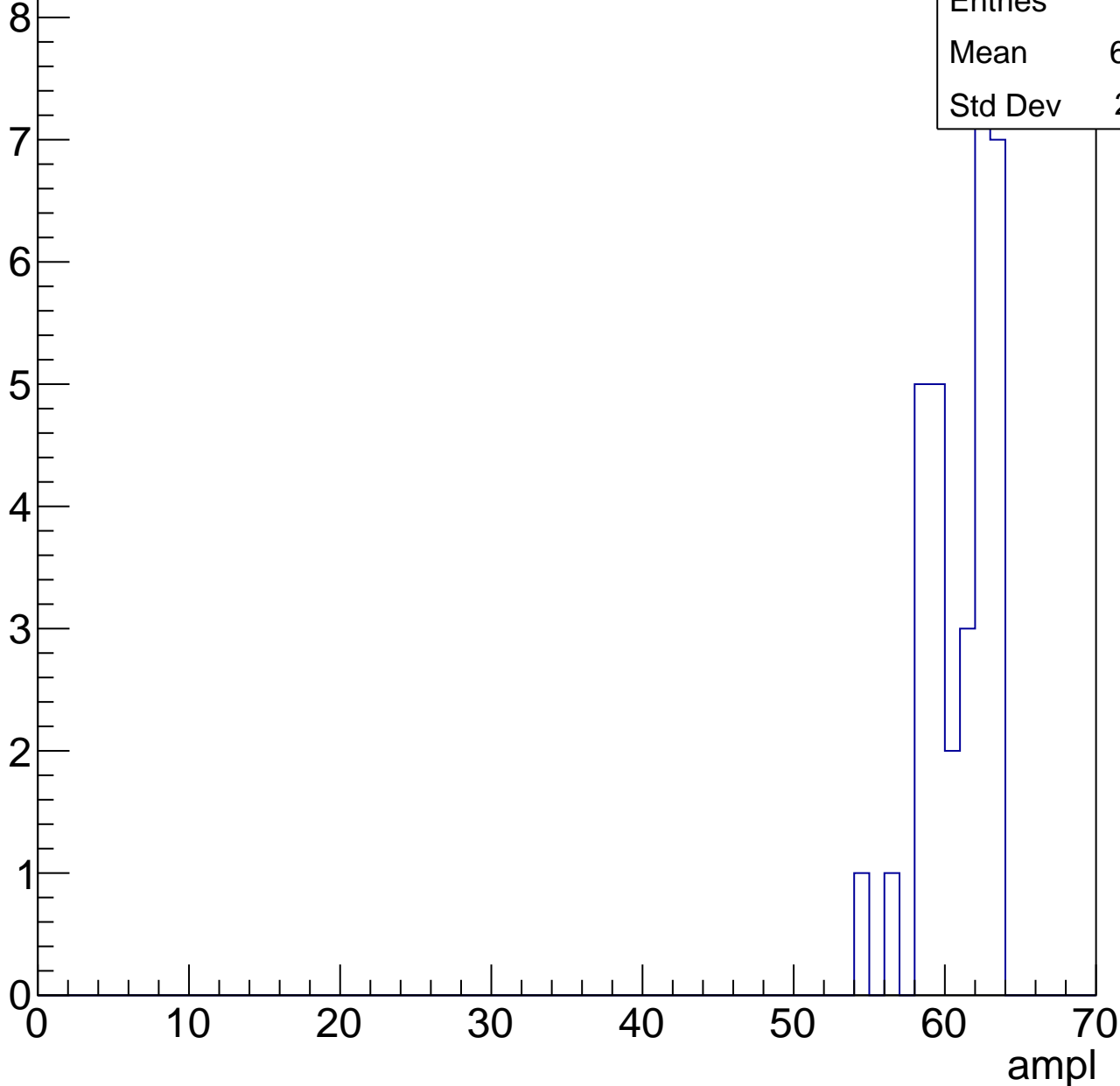


# B0L002S, U2-ch75, adc5

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

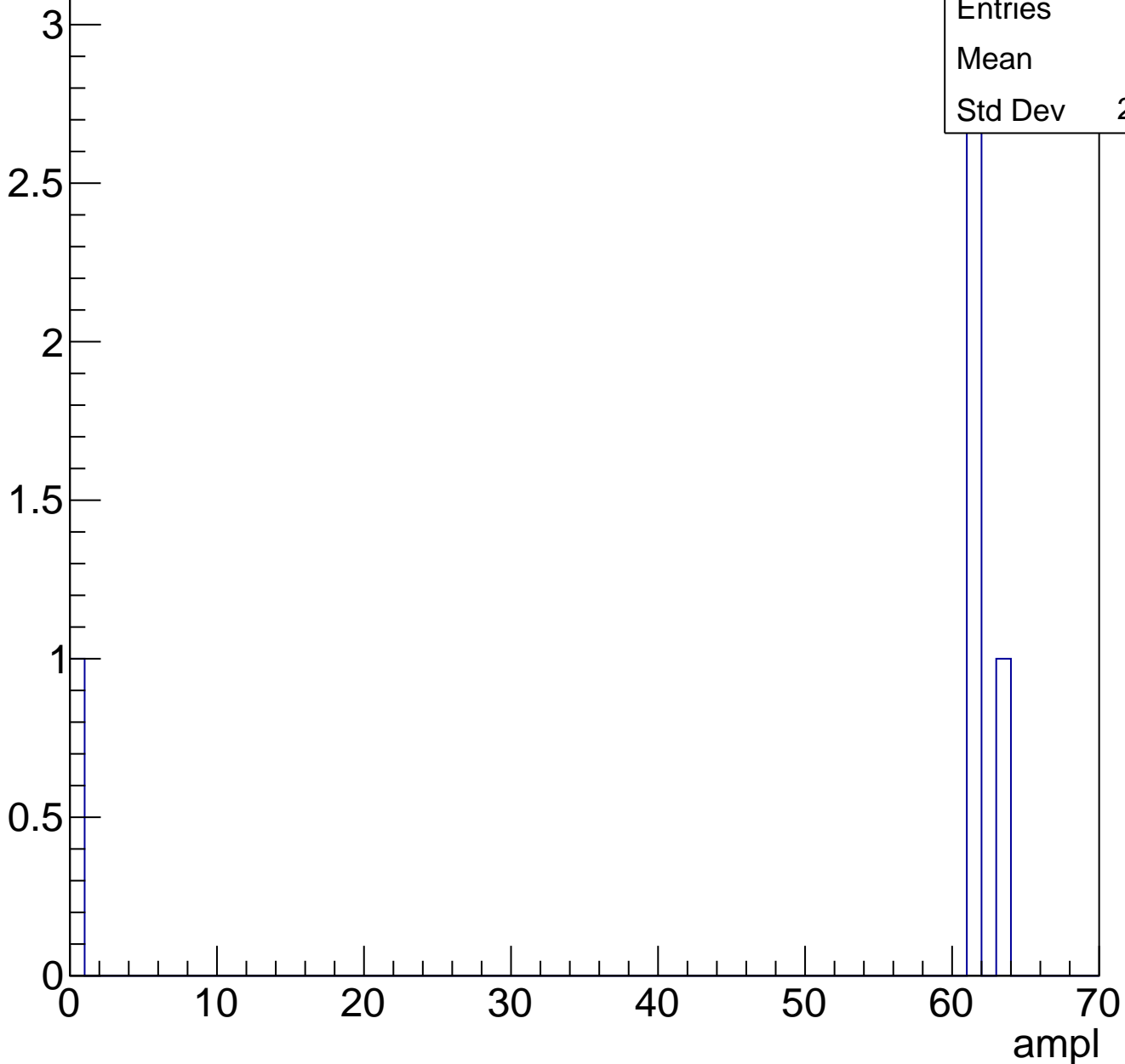
Entries	32
Mean	60.47
Std Dev	2.291



# B0L002S, U2-ch75, adc6

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry





# B0L002S, U2-ch75, adc7

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



# B0L002S, U2-ch76, adc0

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entries	68
Mean	30.25
Std Dev	4.906

**Gaus mean : 31.4702**

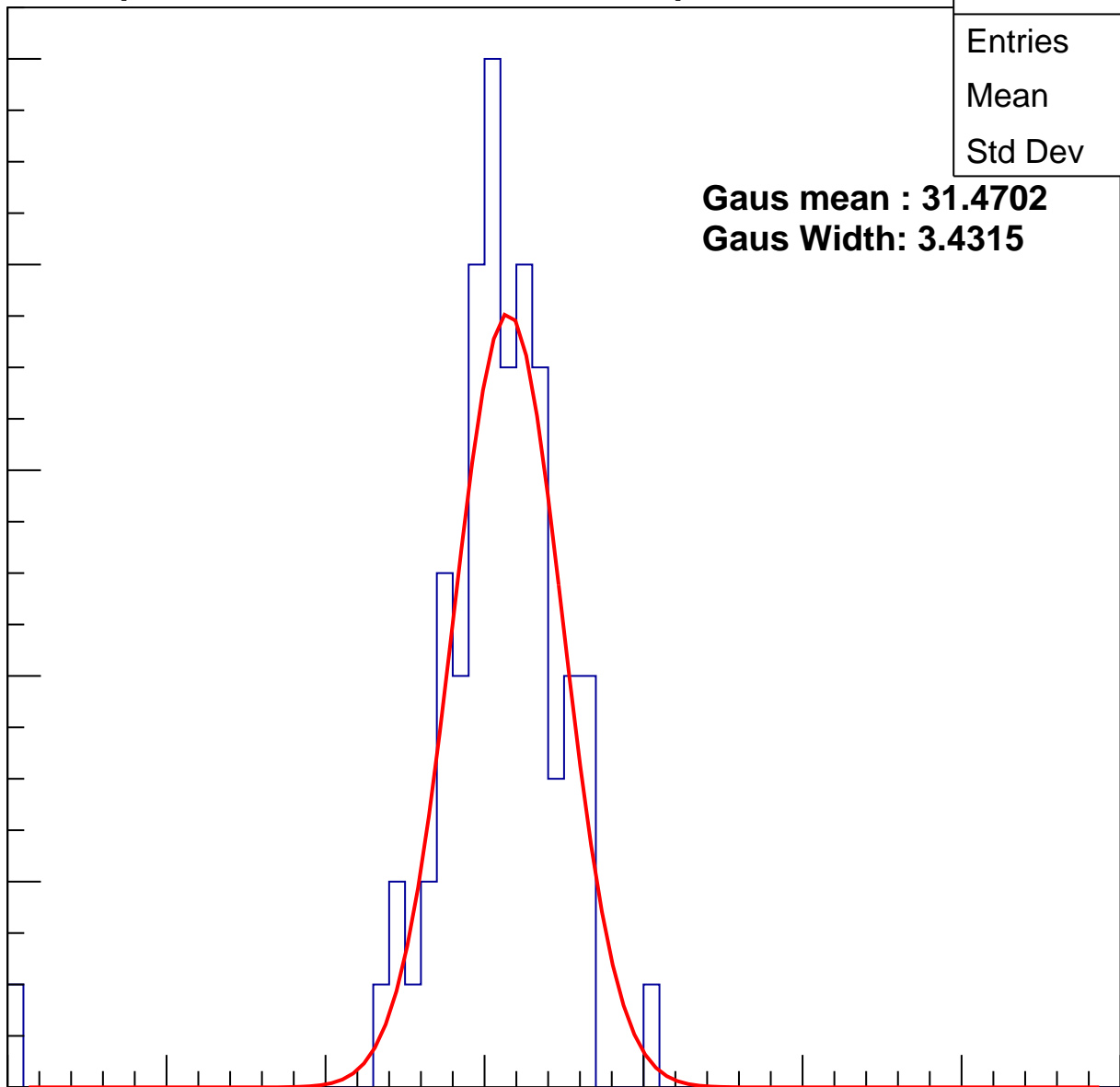
**Gaus Width: 3.4315**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L002S, U2-ch76, adc1

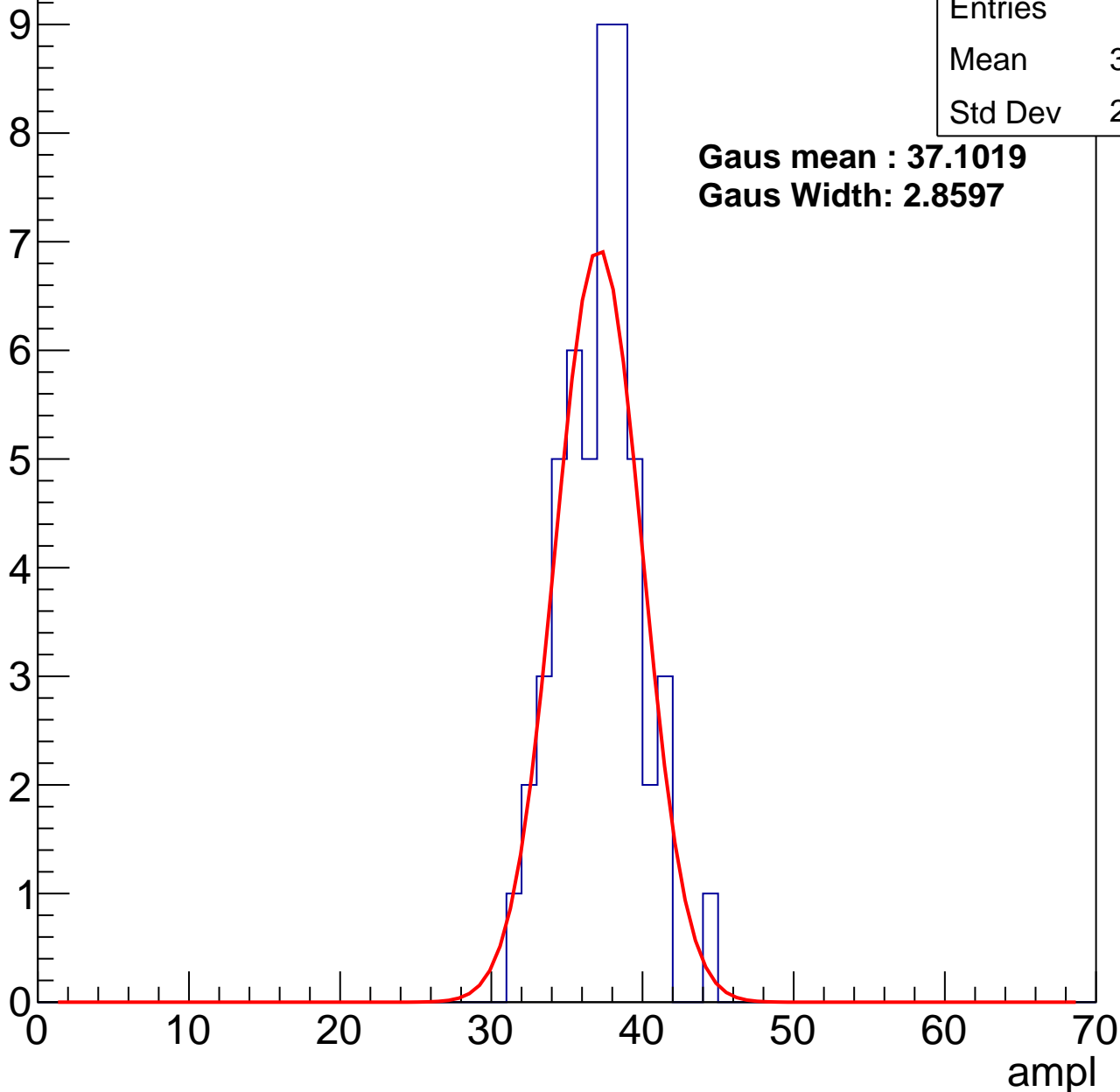
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	51
Mean	36.69
Std Dev	2.608

**Gaus mean : 37.1019**

**Gaus Width: 2.8597**



# B0L002S, U2-ch76, adc2

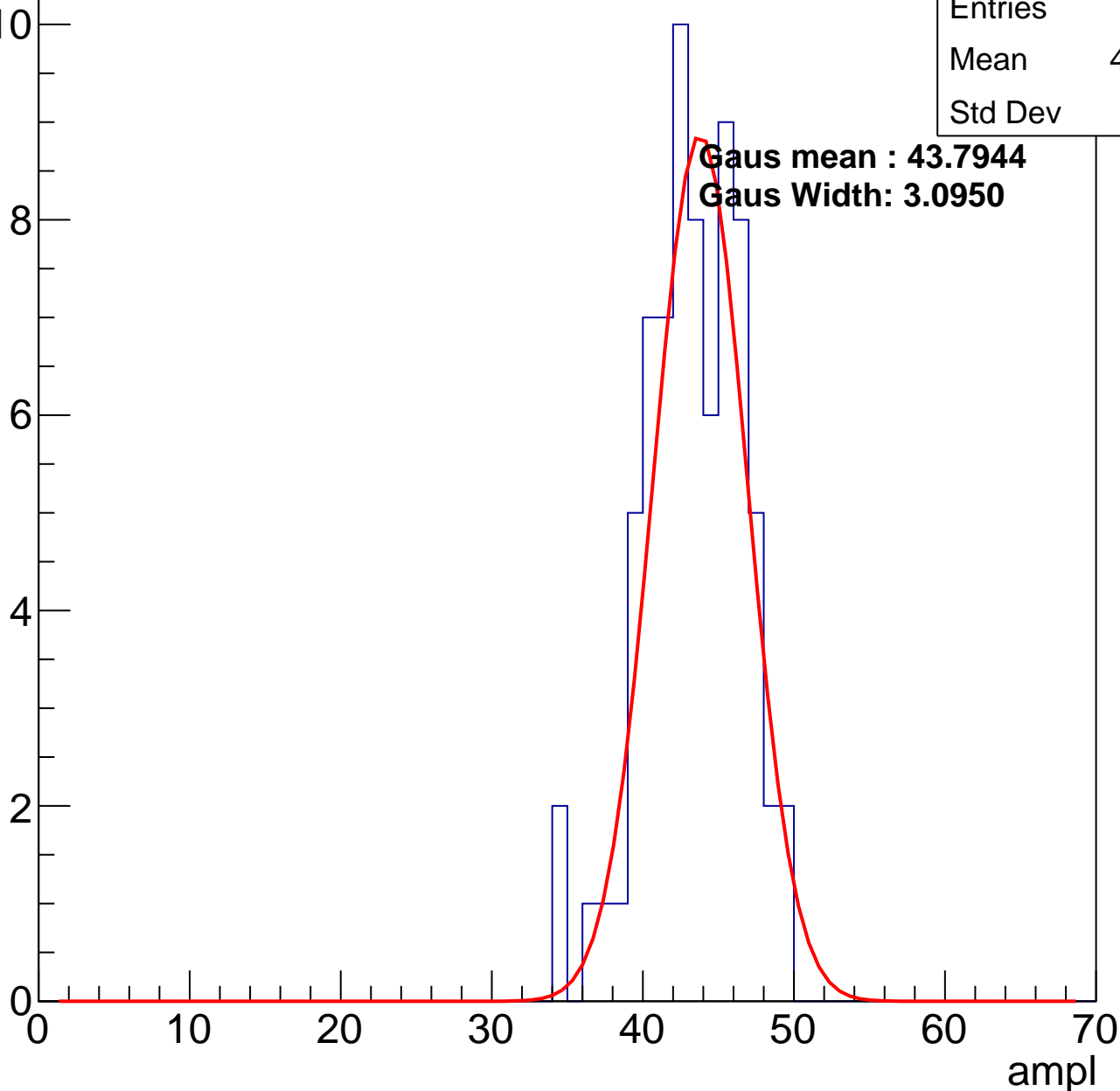
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	74
Mean	42.85
Std Dev	3.22

**Gaus mean : 43.7944**

**Gaus Width: 3.0950**

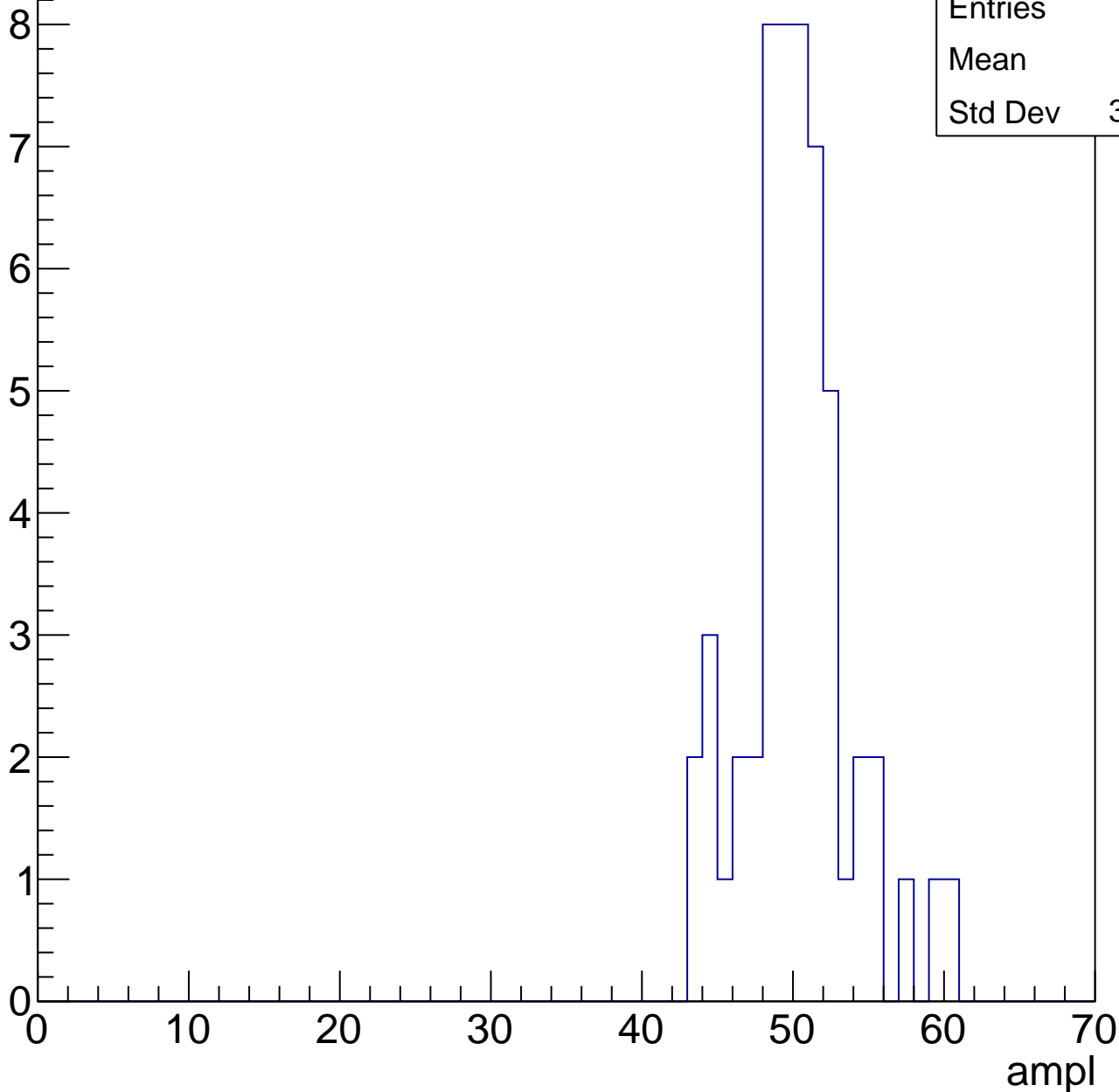


# B0L002S, U2-ch76, adc3

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	54
Mean	49.8
Std Dev	3.514

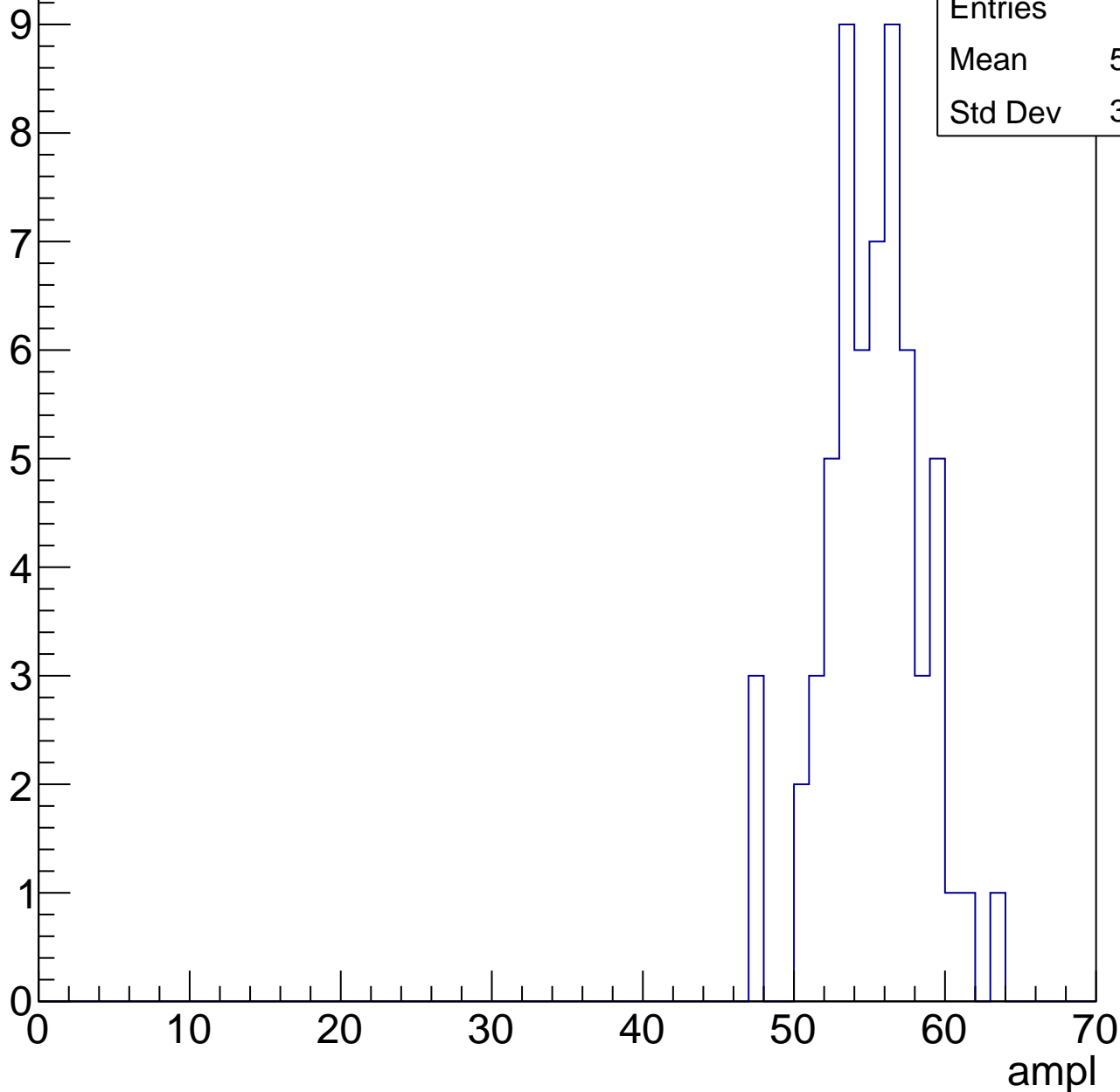


# B0L002S, U2-ch76, adc4

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	61
Mean	54.74
Std Dev	3.234

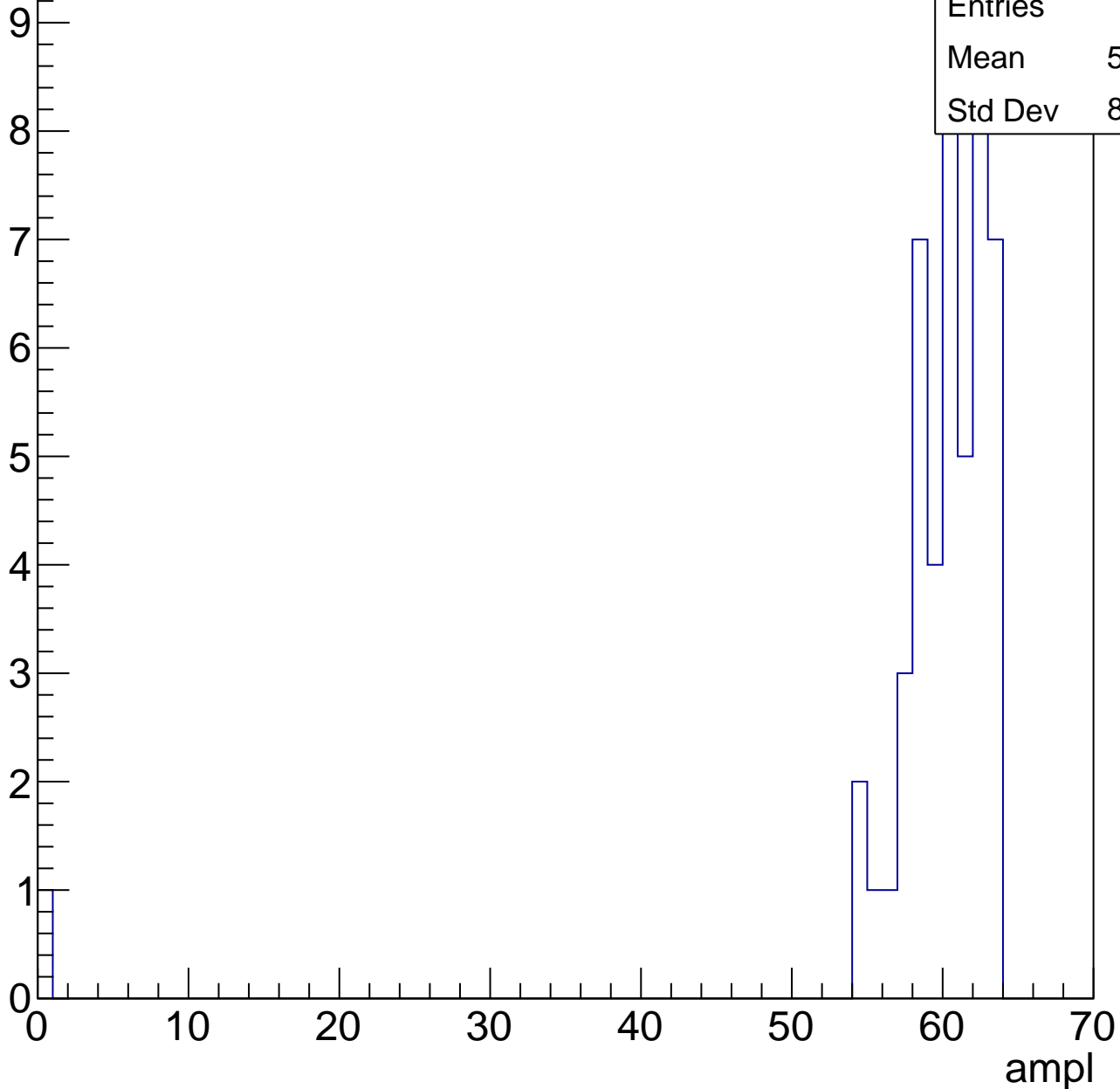


# B0L002S, U2-ch76, adc5

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

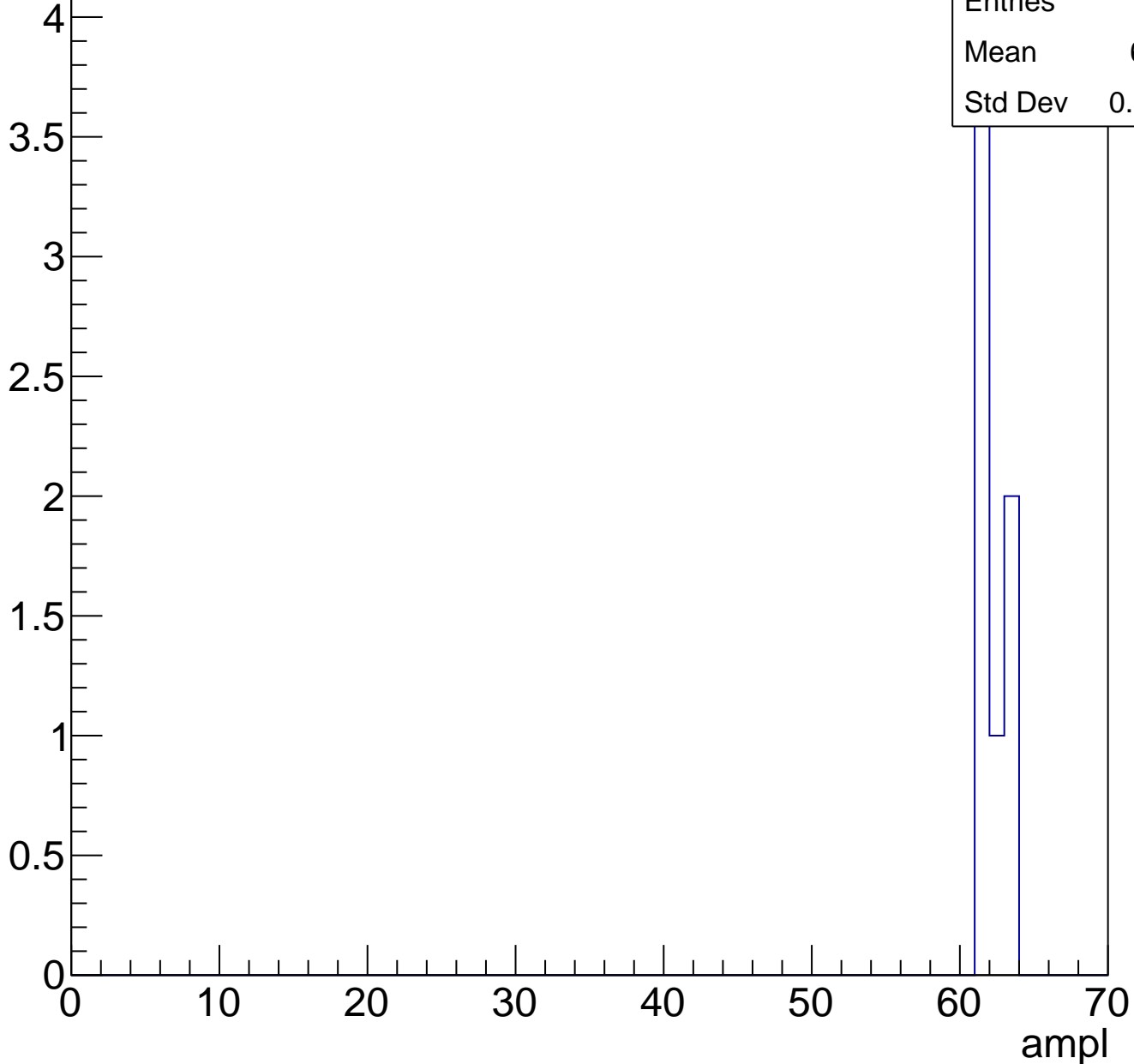
Entries	48
Mean	58.67
Std Dev	8.887



# B0L002S, U2-ch76, adc6

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry





# B0L002S, U2-ch76, adc7

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L002S, U2-ch77, adc0

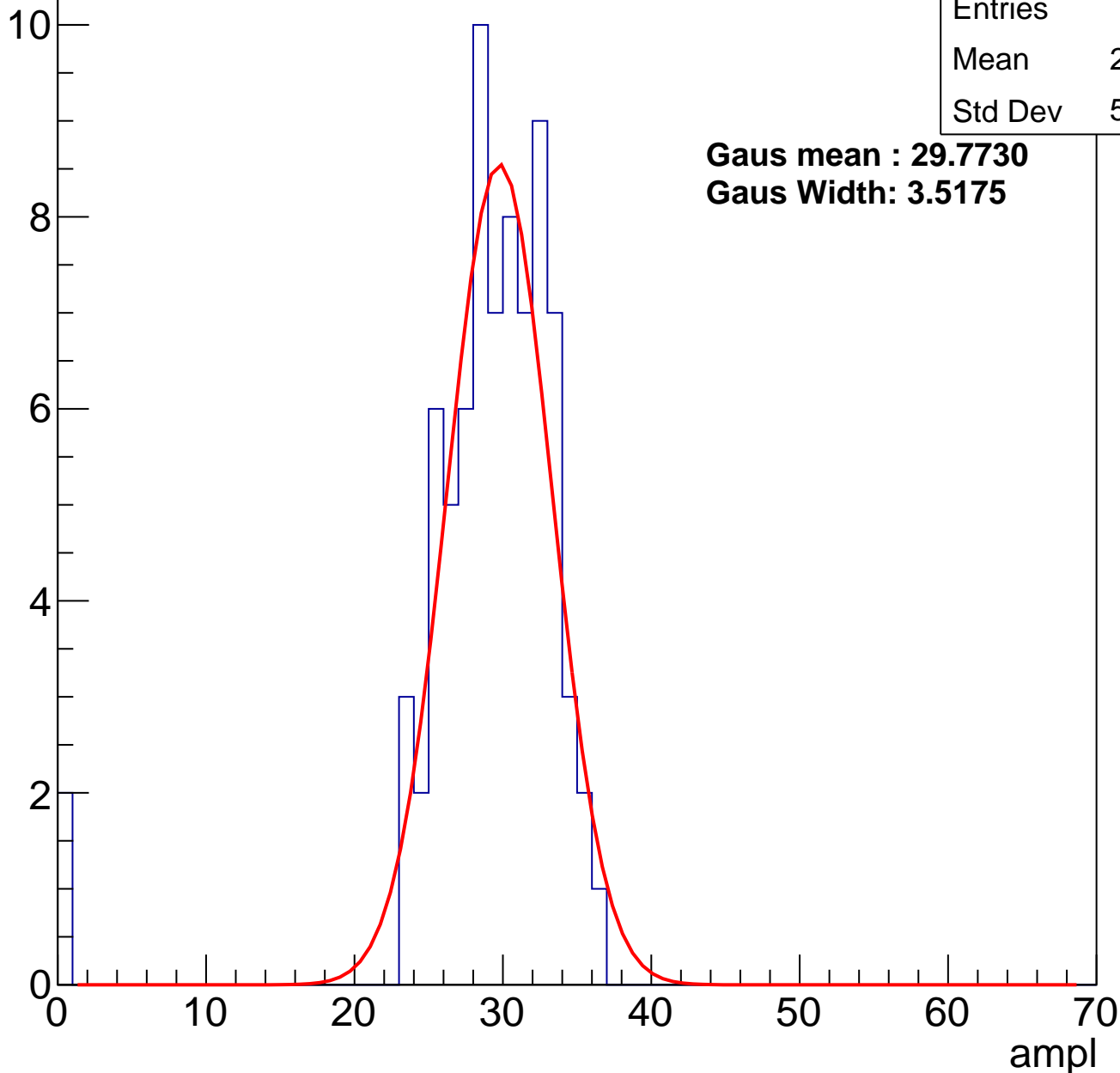
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entries	78
Mean	28.54
Std Dev	5.574

**Gaus mean : 29.7730**

**Gaus Width: 3.5175**

Entry



# B0L002S, U2-ch77, adc1

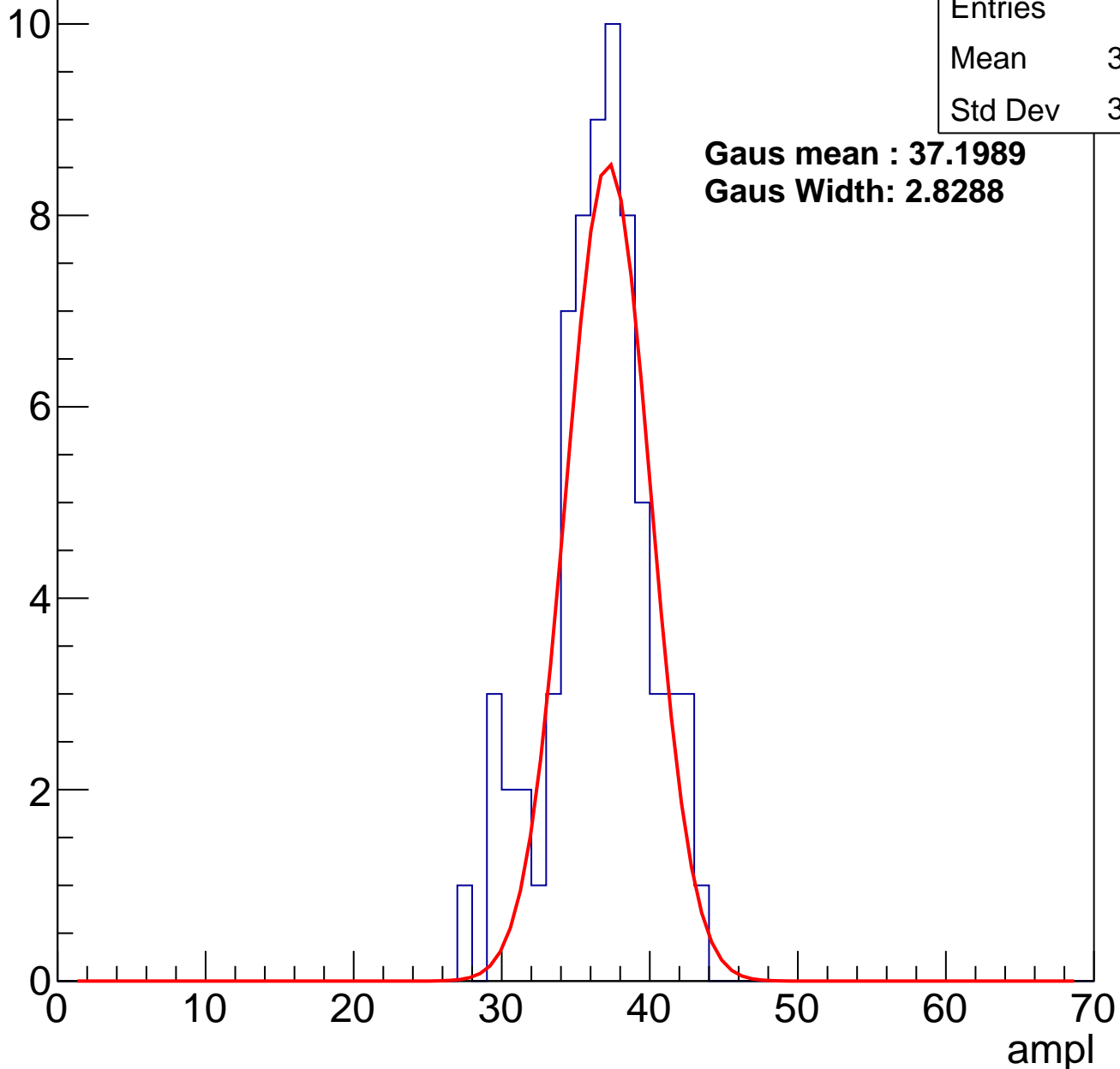
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entries	69
Mean	36.09
Std Dev	3.395

**Gaus mean : 37.1989**

**Gaus Width: 2.8288**

Entry



# B0L002S, U2-ch77, adc2

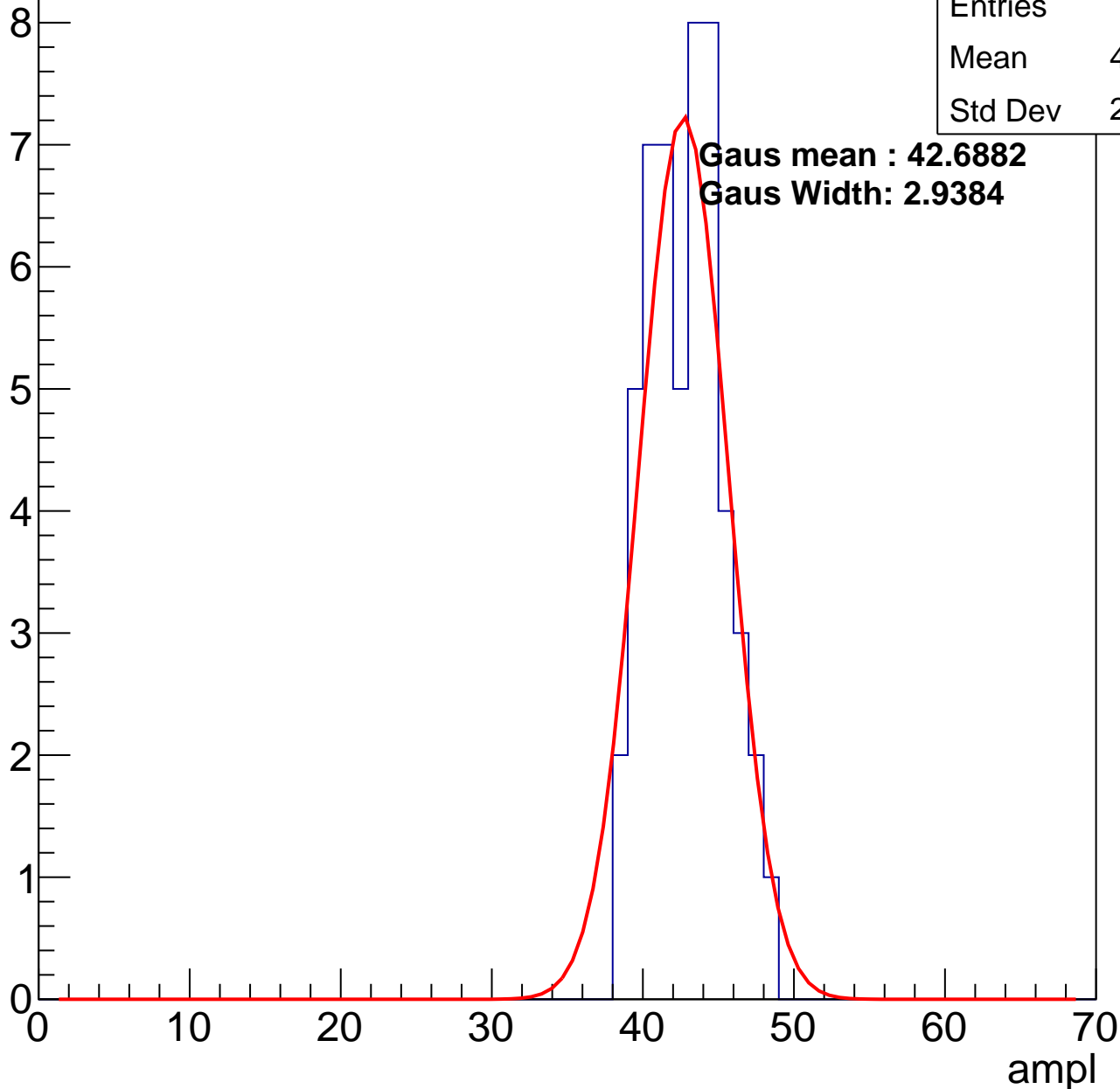
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	52
Mean	42.38
Std Dev	2.459

**Gaus mean : 42.6882**

**Gaus Width: 2.9384**

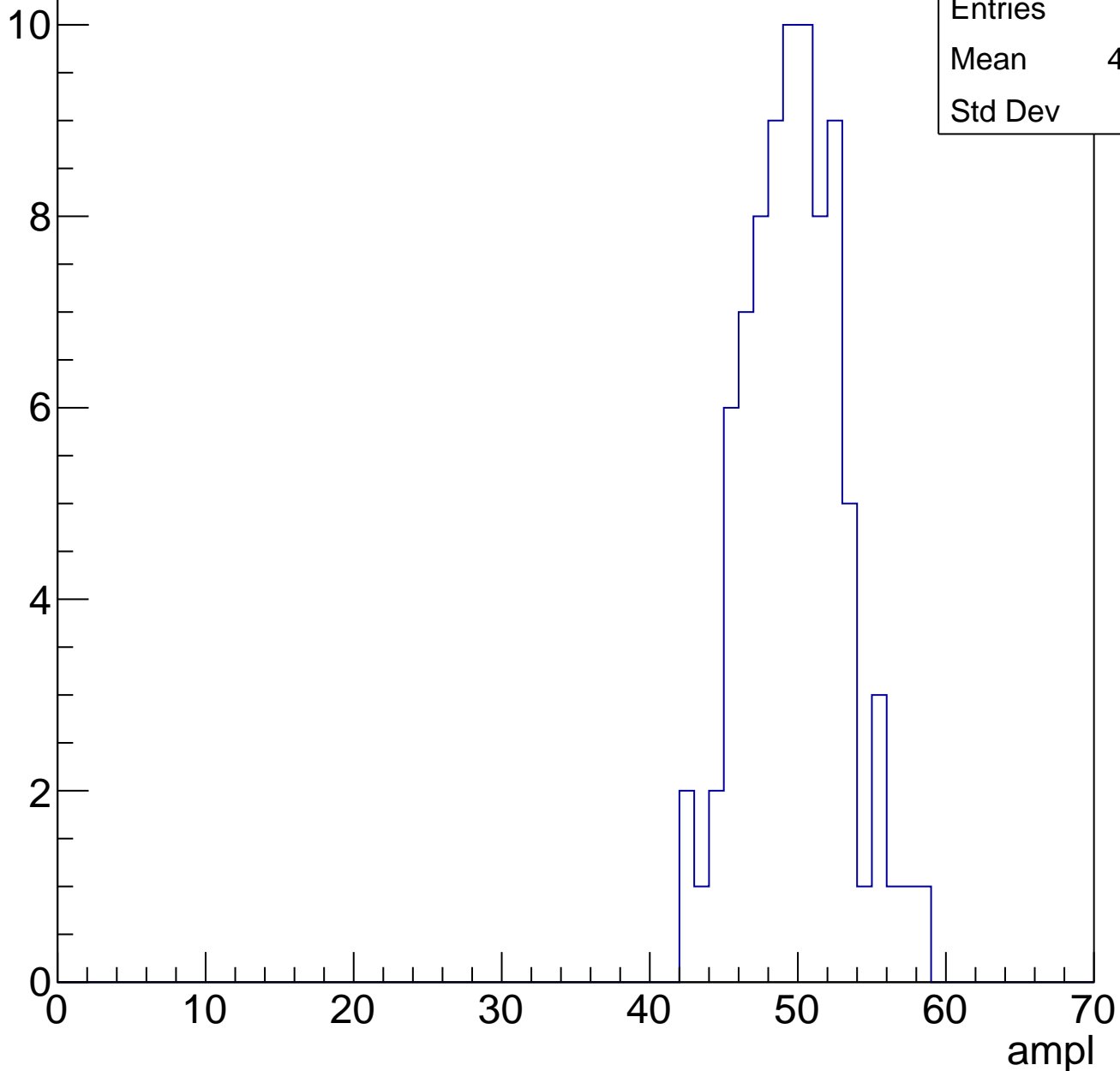


# B0L002S, U2-ch77, adc3

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entries	84
Mean	49.24
Std Dev	3.29

Entry

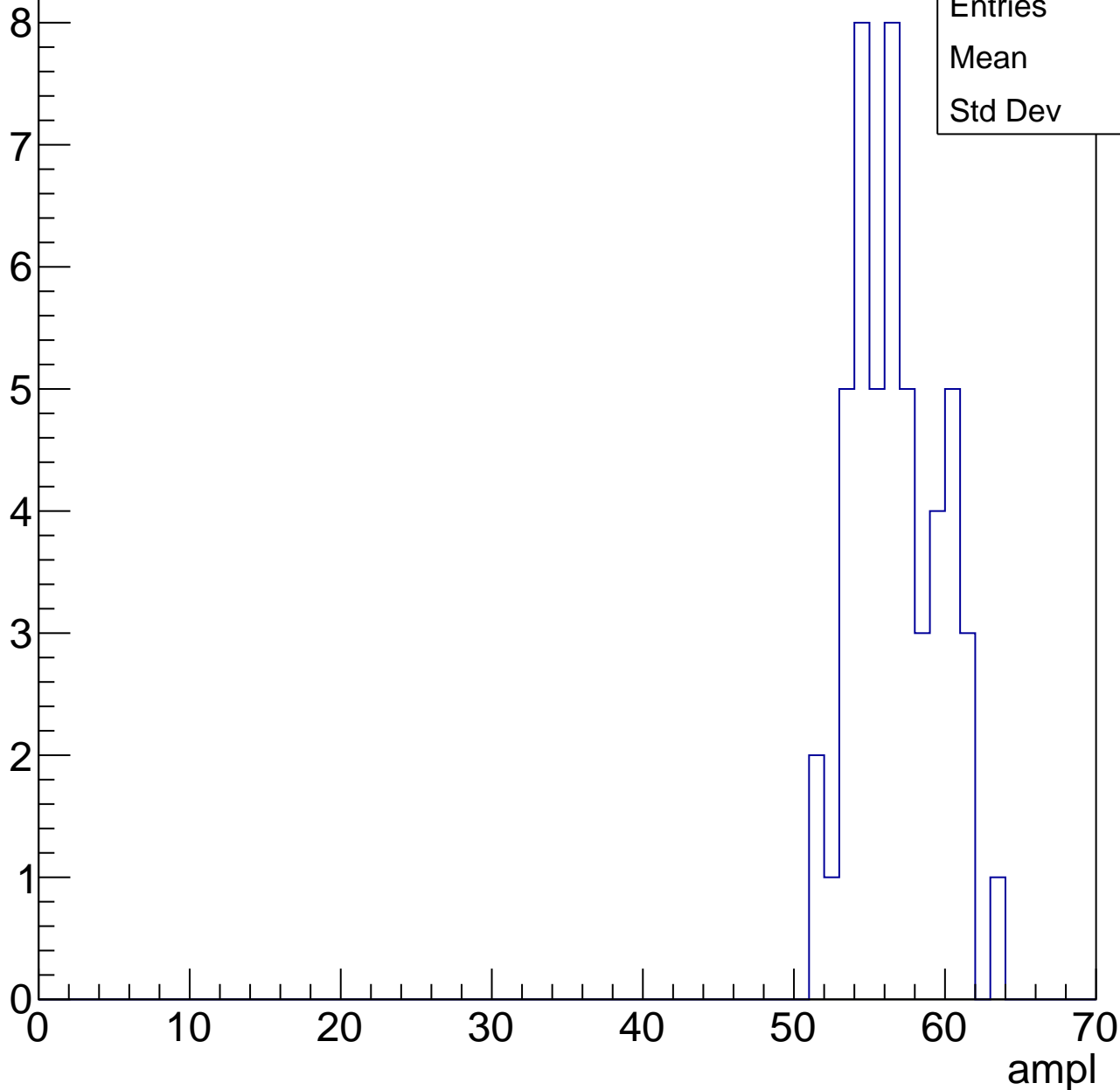


# B0L002S, U2-ch77, adc4

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	50
Mean	56.3
Std Dev	2.83

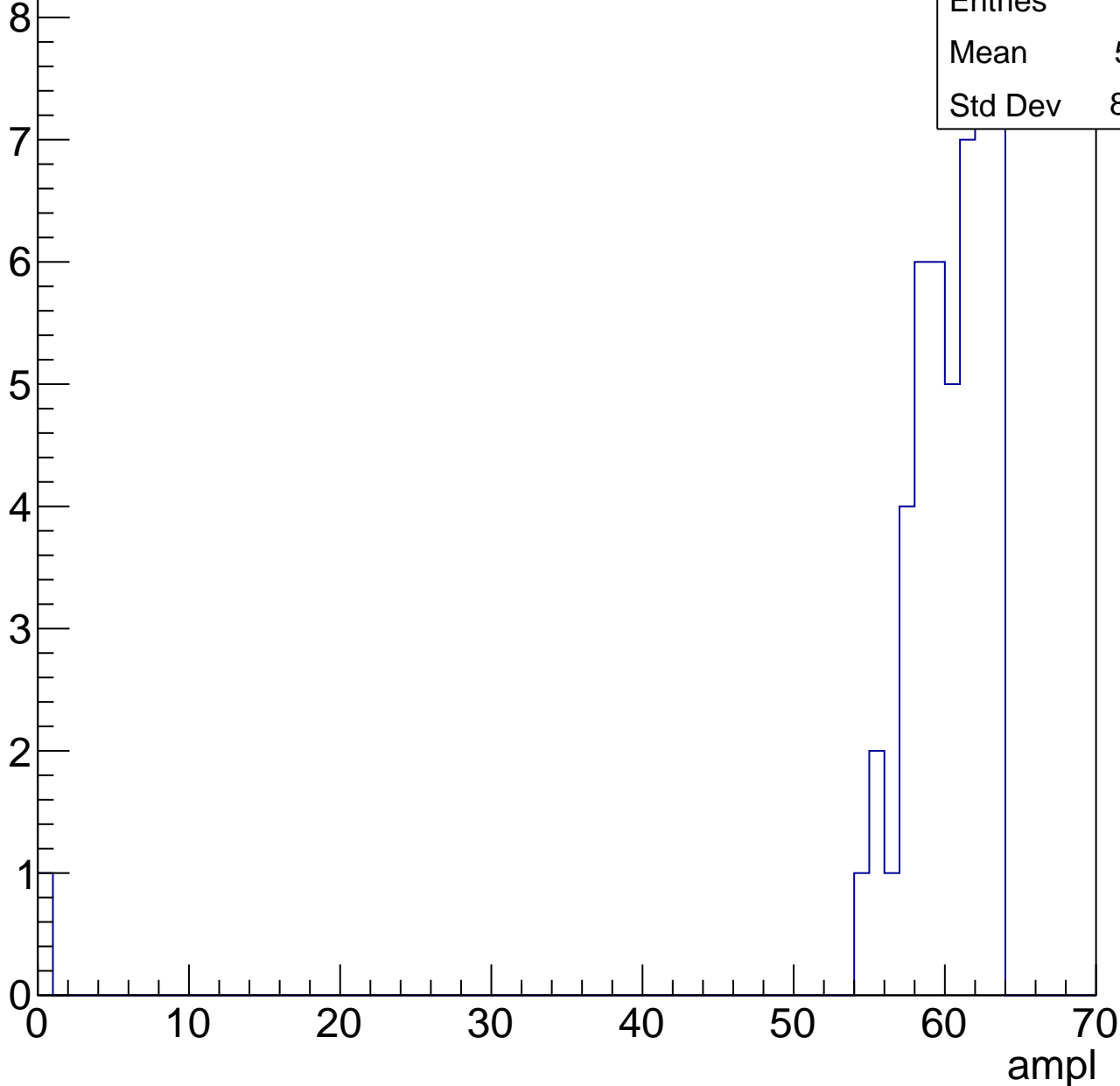


# B0L002S, U2-ch77, adc5

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	49
Mean	58.71
Std Dev	8.804



# B0L002S, U2-ch77, adc6

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	3
Mean	62.33
Std Dev	0.4714

ampl

0 10 20 30 40 50 60 70



# B0L002S, U2-ch77, adc7

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



# B0L002S, U2-ch78, adc0

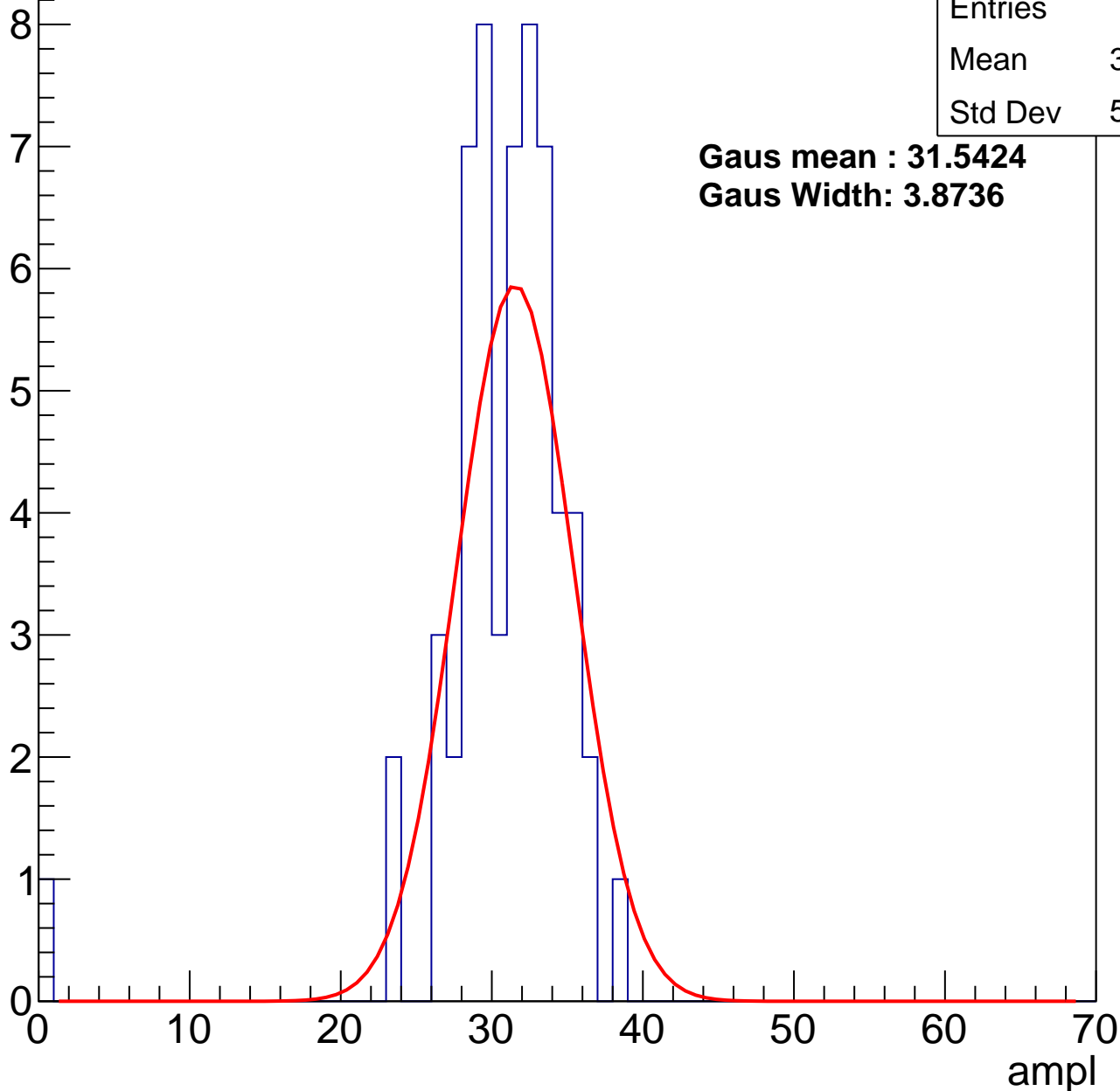
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	59
Mean	30.27
Std Dev	5.038

**Gaus mean : 31.5424**

**Gaus Width: 3.8736**



# B0L002S, U2-ch78, adc1

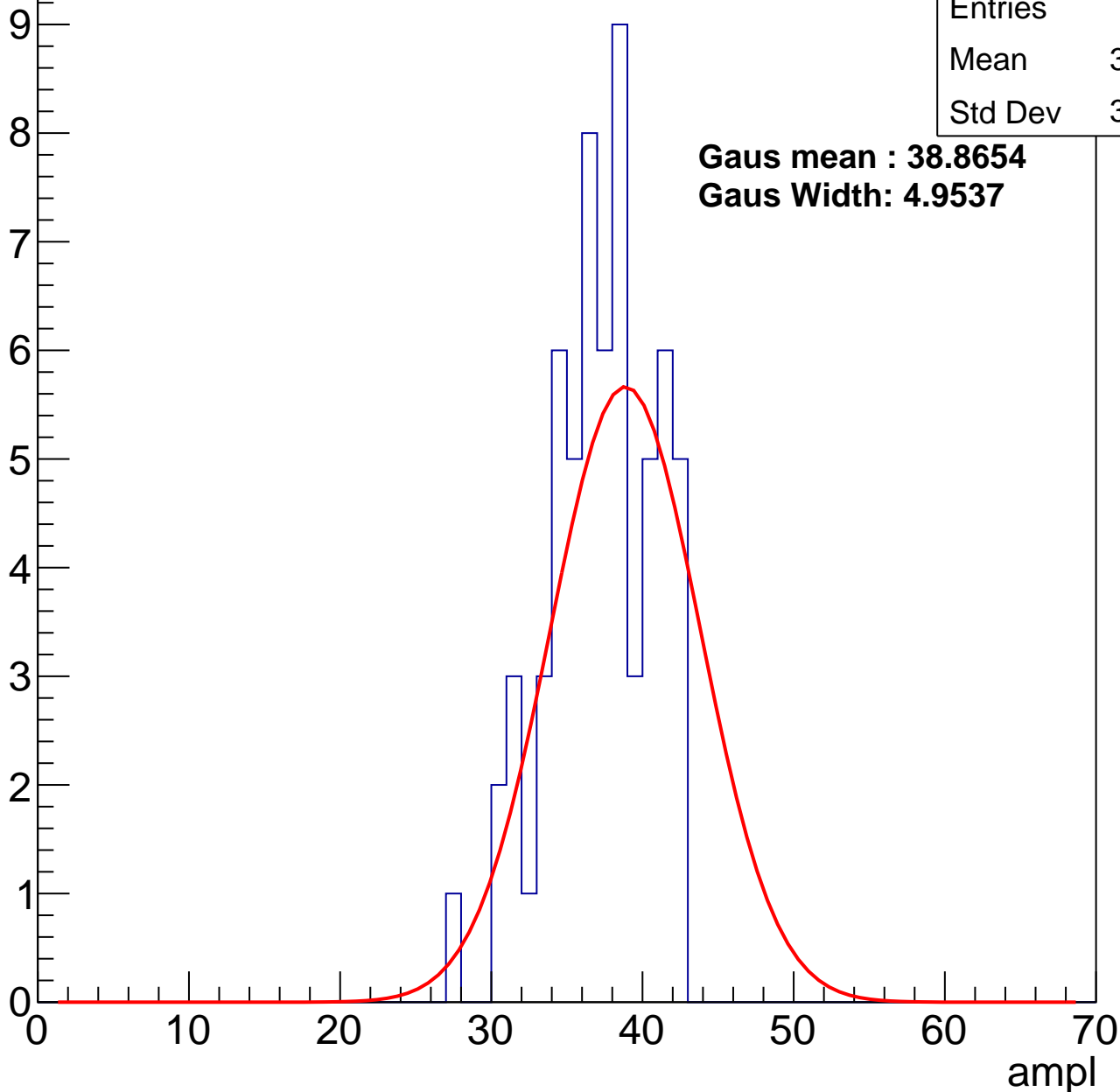
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	63
Mean	36.75
Std Dev	3.436

**Gaus mean : 38.8654**

**Gaus Width: 4.9537**



# B0L002S, U2-ch78, adc2

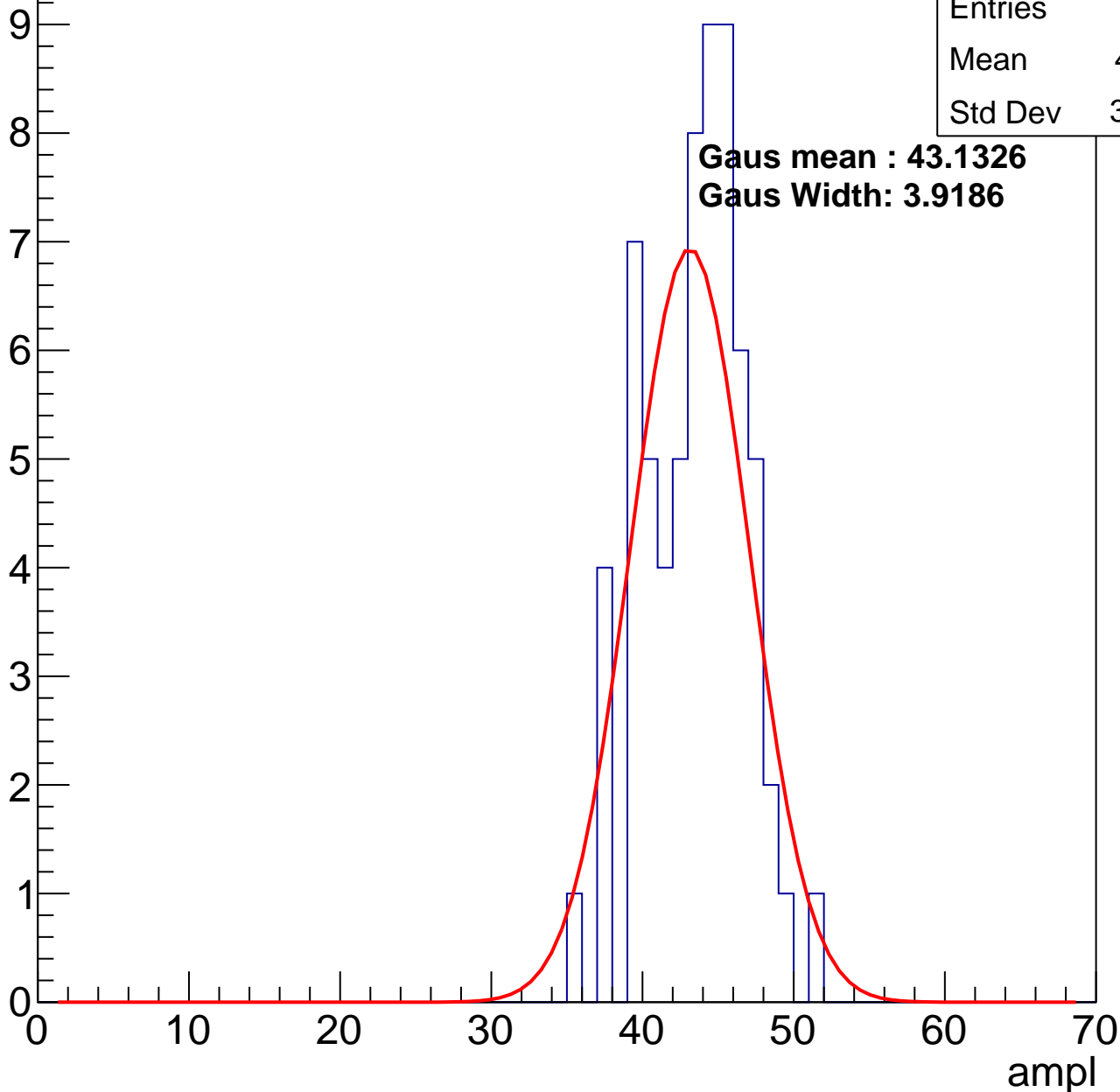
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	67
Mean	43.01
Std Dev	3.267

**Gaus mean : 43.1326**

**Gaus Width: 3.9186**

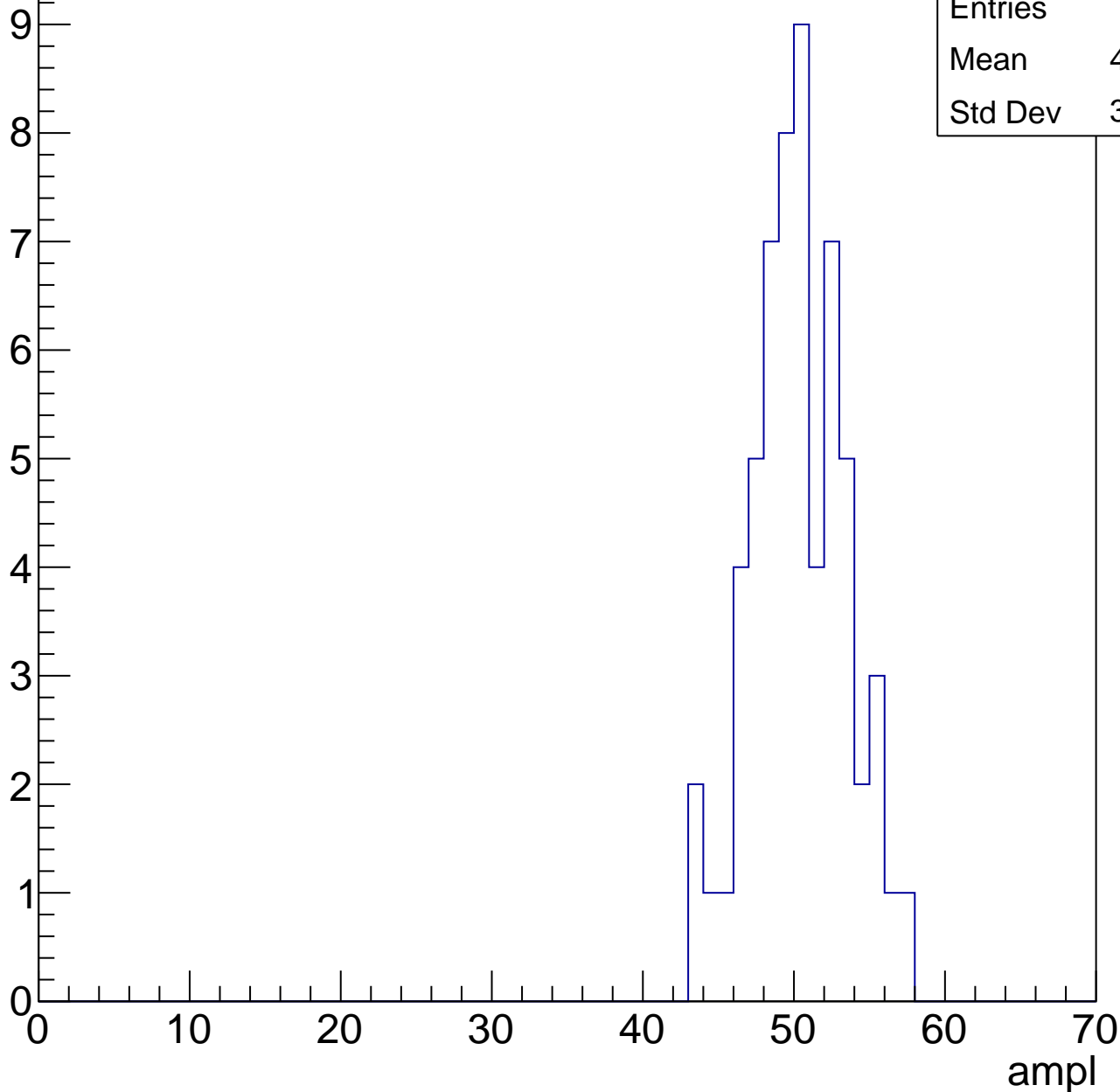


# B0L002S, U2-ch78, adc3

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

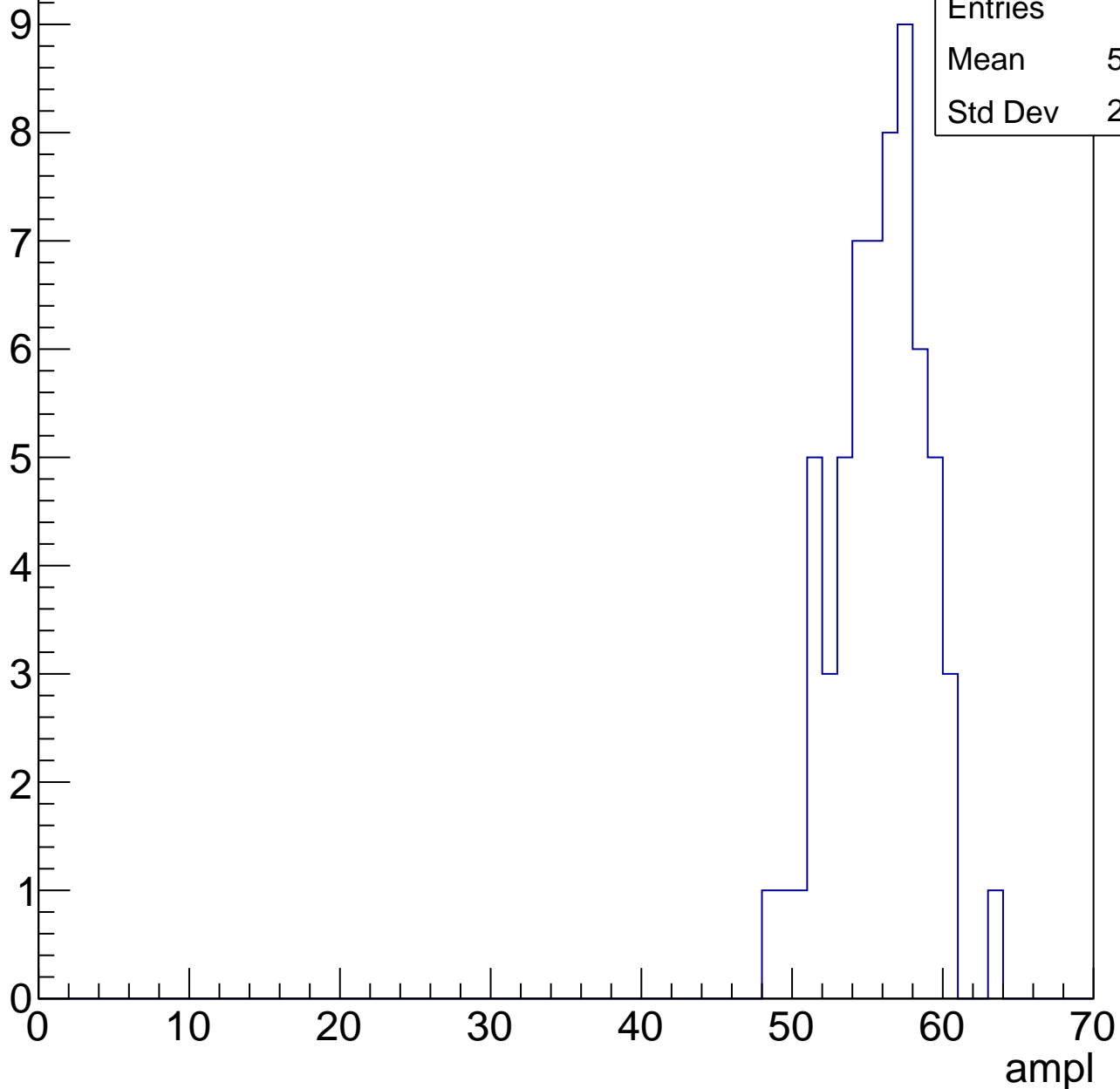
Entries	60
Mean	49.85
Std Dev	3.087



# B0L002S, U2-ch78, adc4

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

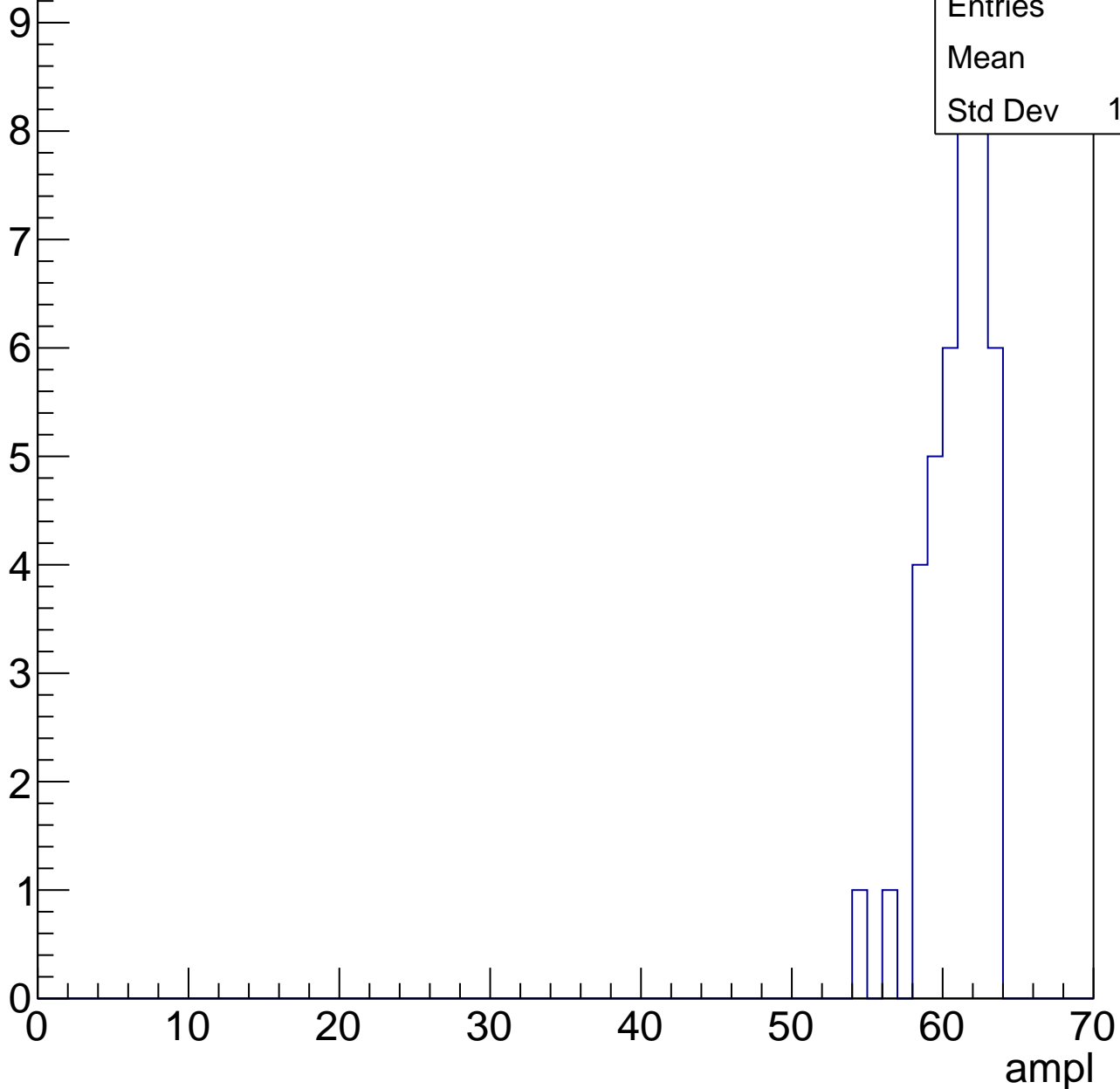


# B0L002S, U2-ch78, adc5

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

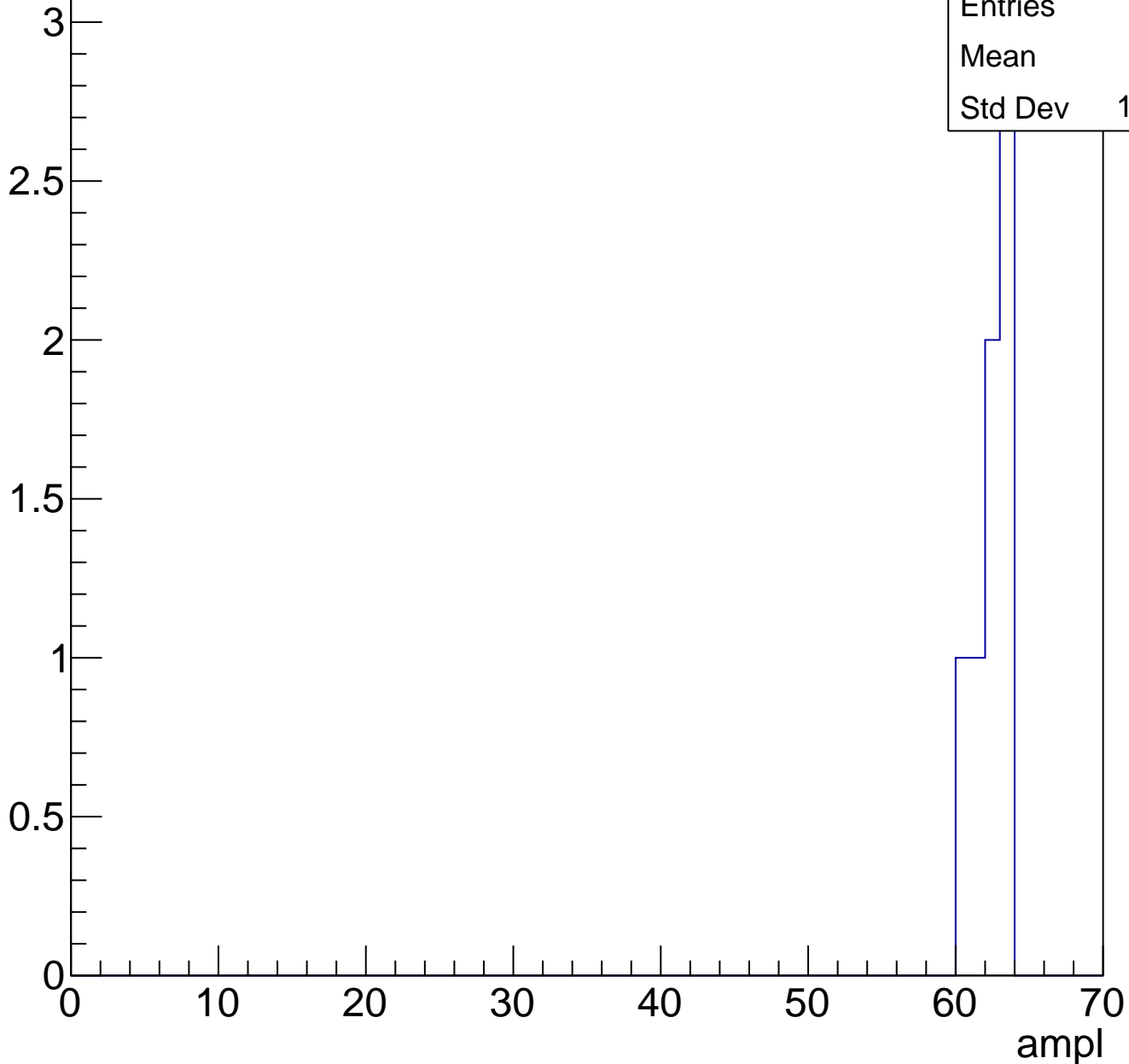
Entries	40
Mean	60.5
Std Dev	1.987



# B0L002S, U2-ch78, adc6

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry





# B0L002S, U2-ch78, adc7

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



# B0L002S, U2-ch79, adc0

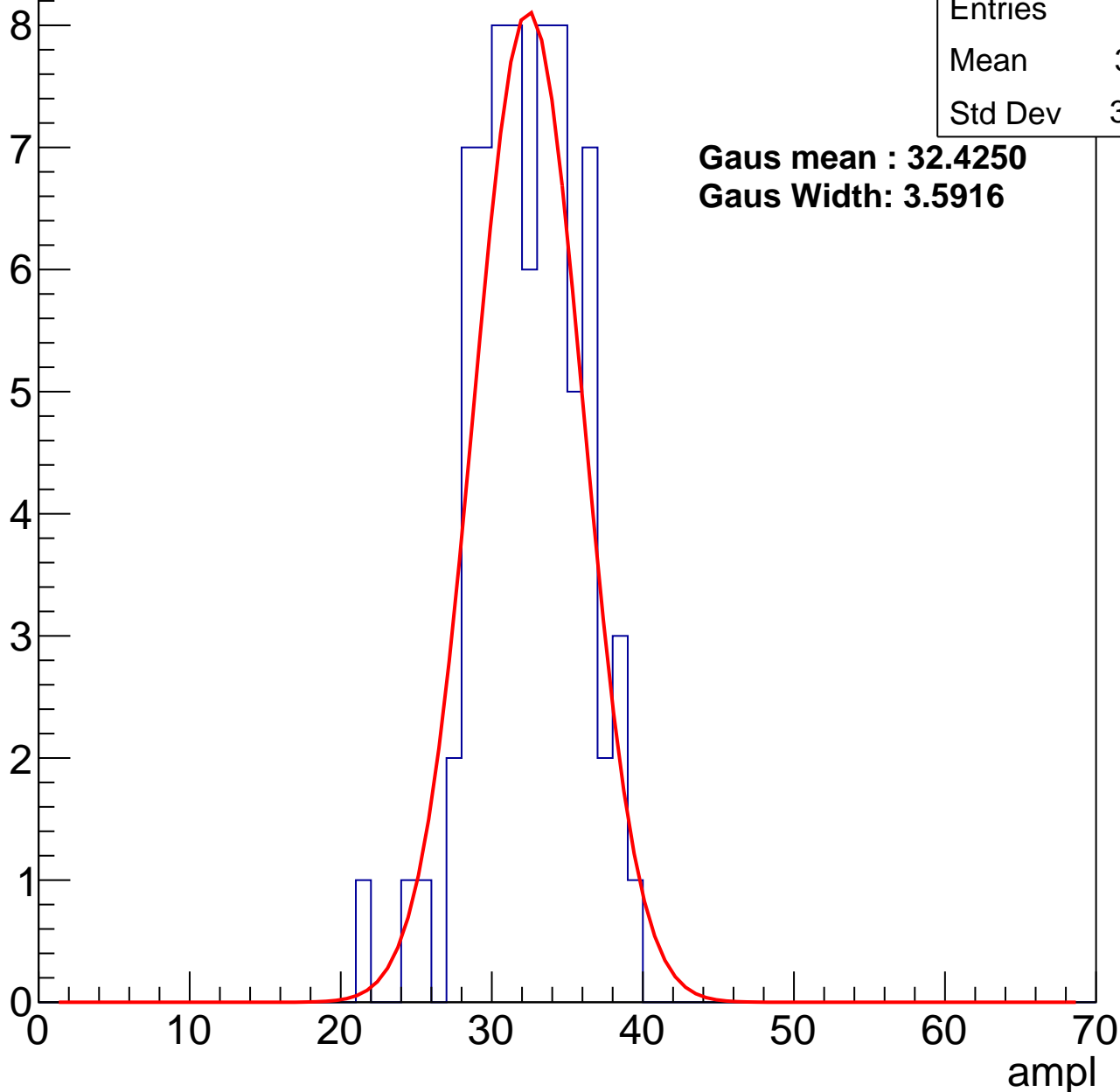
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	75
Mean	31.91
Std Dev	3.469

**Gaus mean : 32.4250**

**Gaus Width: 3.5916**



# B0L002S, U2-ch79, adc1

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	72
Mean	38.76
Std Dev	3.569

**Gaus mean : 39.4115**

**Gaus Width: 3.5474**

10

8

6

4

2

0

0

10

20

30

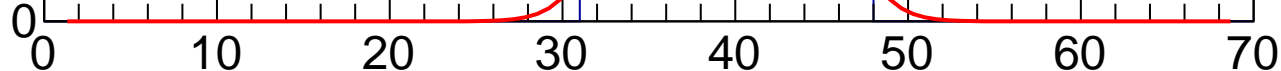
40

50

60

70

ampl



# B0L002S, U2-ch79, adc2

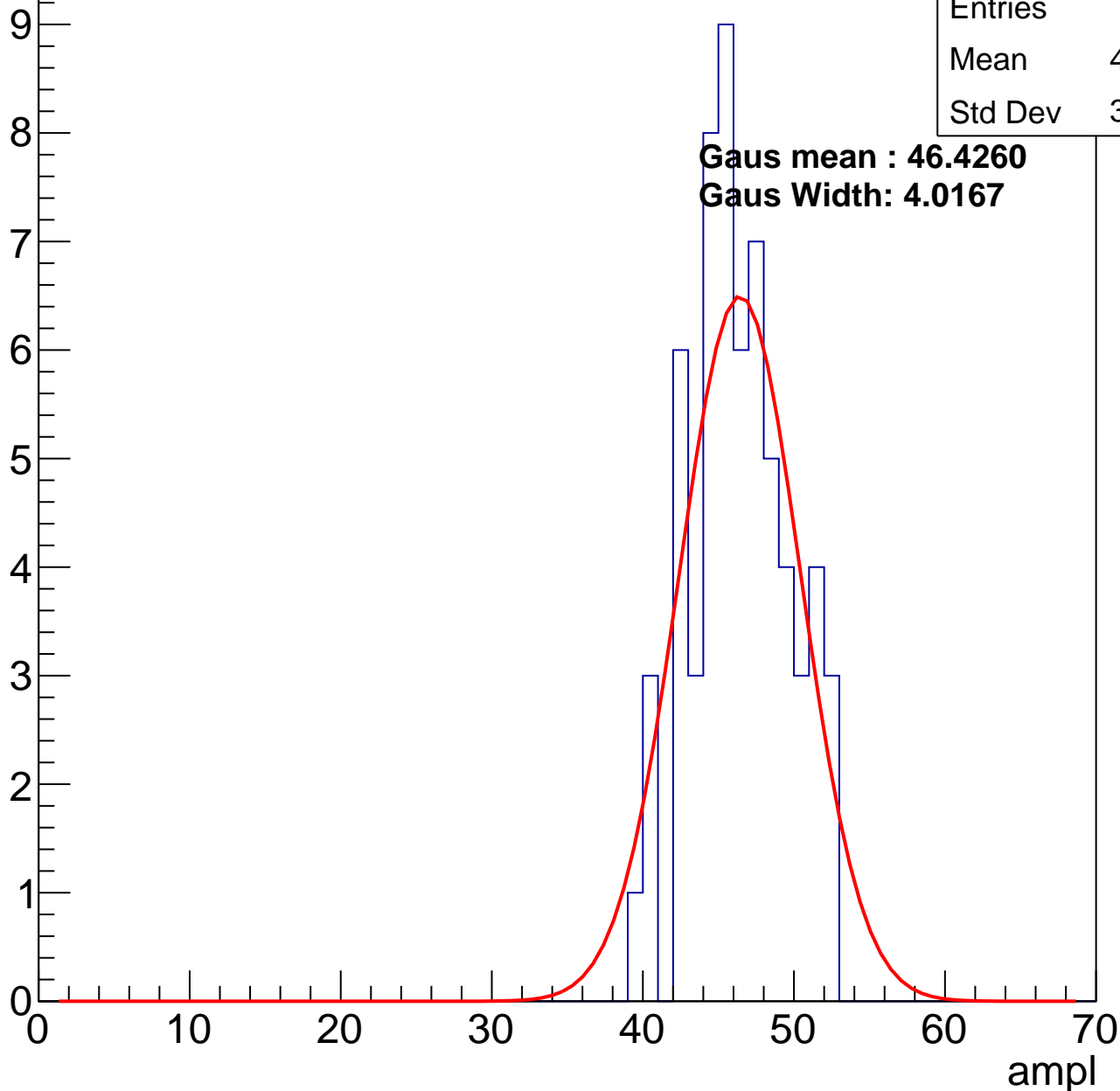
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	62
Mean	45.94
Std Dev	3.212

**Gaus mean : 46.4260**

**Gaus Width: 4.0167**

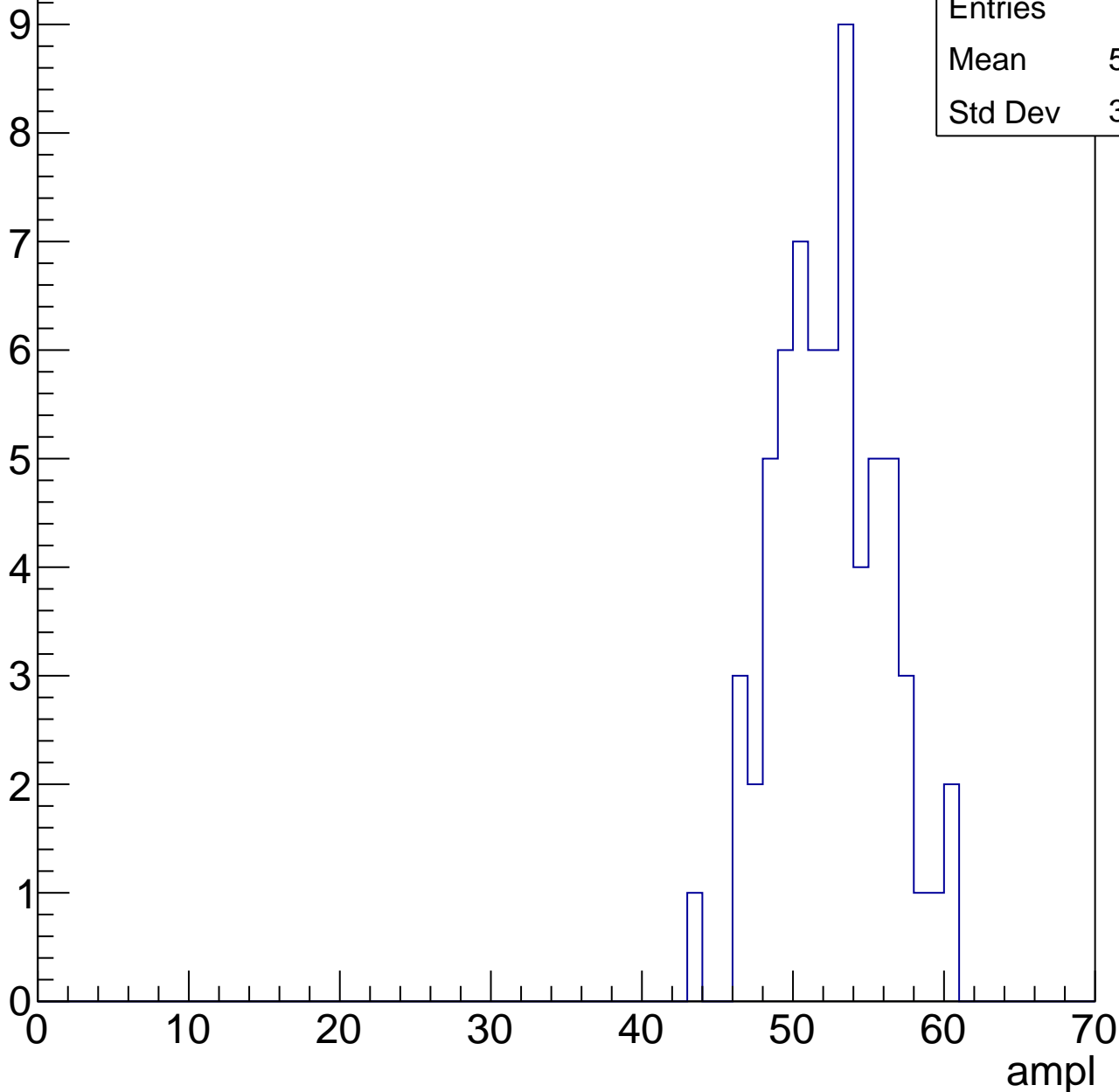


# B0L002S, U2-ch79, adc3

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

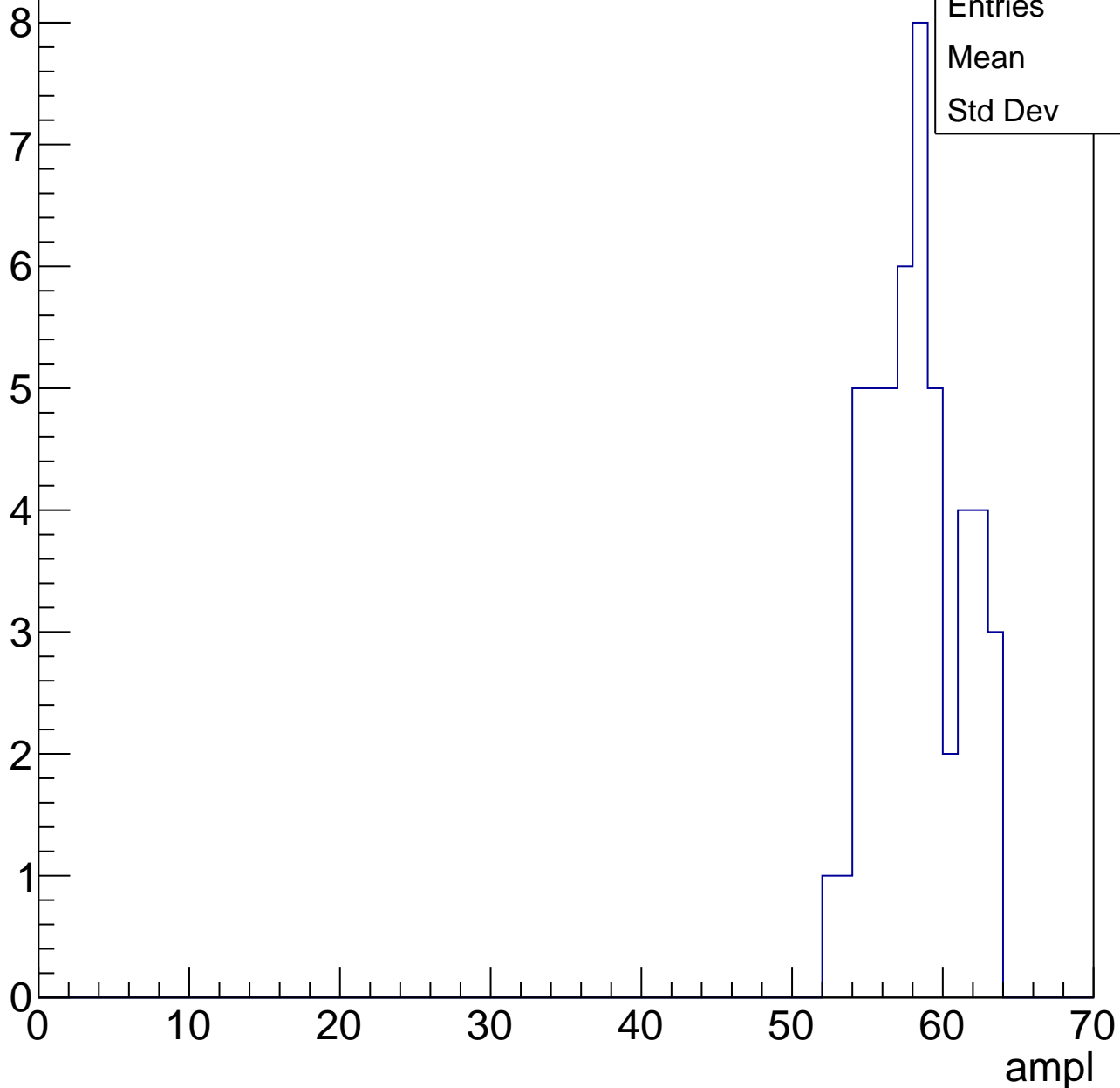
Entries	66
Mean	52.02
Std Dev	3.578



# B0L002S, U2-ch79, adc4

calib\_packv5\_042523\_0143.root, FC#8, port C1

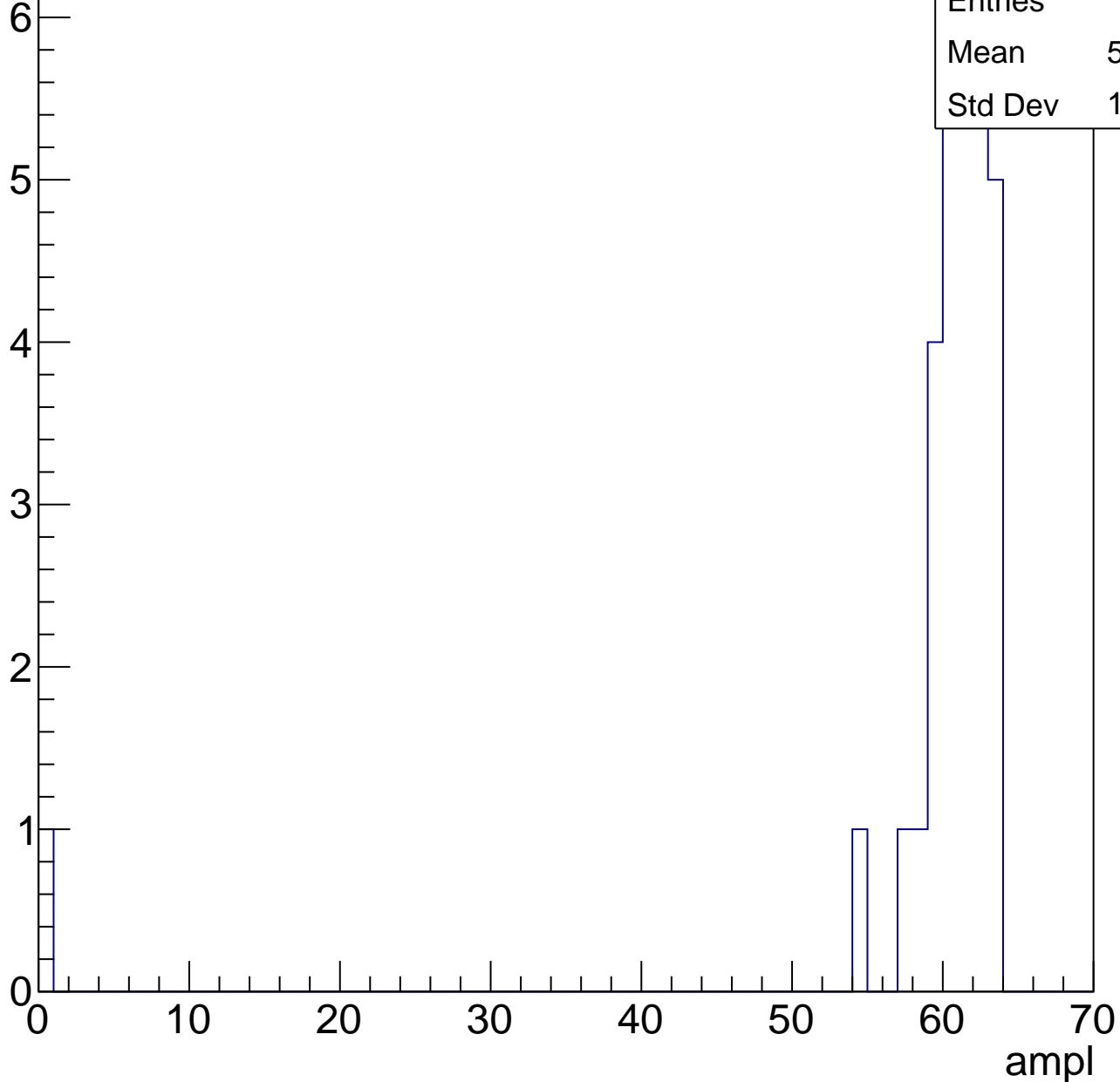
Entry



# B0L002S, U2-ch79, adc5

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



# B0L002S, U2-ch79, adc6

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



Entries	2
Mean	63
Std Dev	0



# B0L002S, U2-ch79, adc7

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L002S, U2-ch80, adc0

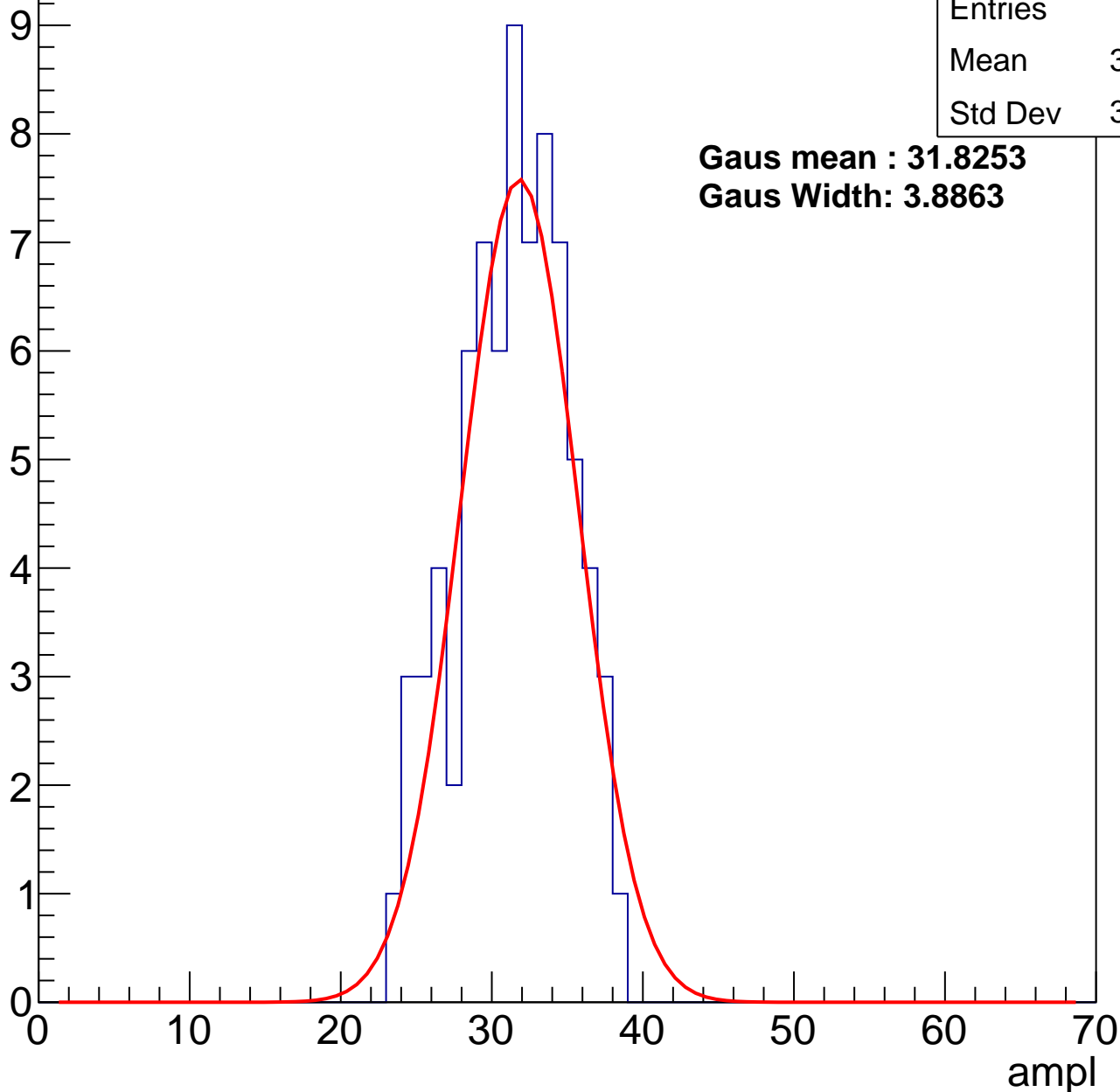
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	76
Mean	30.95
Std Dev	3.587

**Gaus mean : 31.8253**

**Gaus Width: 3.8863**



# B0L002S, U2-ch80, adc1

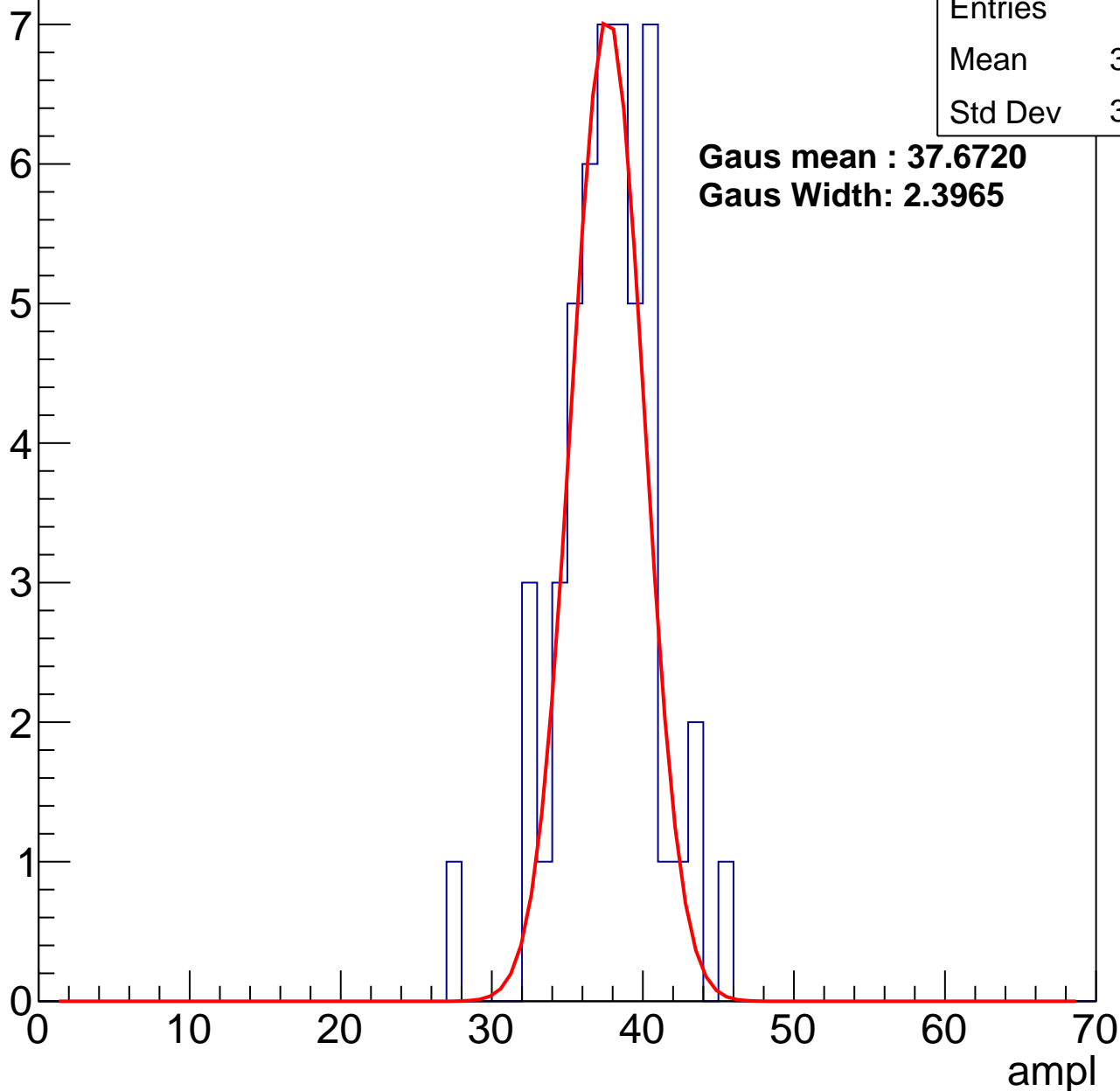
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	50
Mean	37.26
Std Dev	3.186

**Gaus mean : 37.6720**

**Gaus Width: 2.3965**



# B0L002S, U2-ch80, adc2

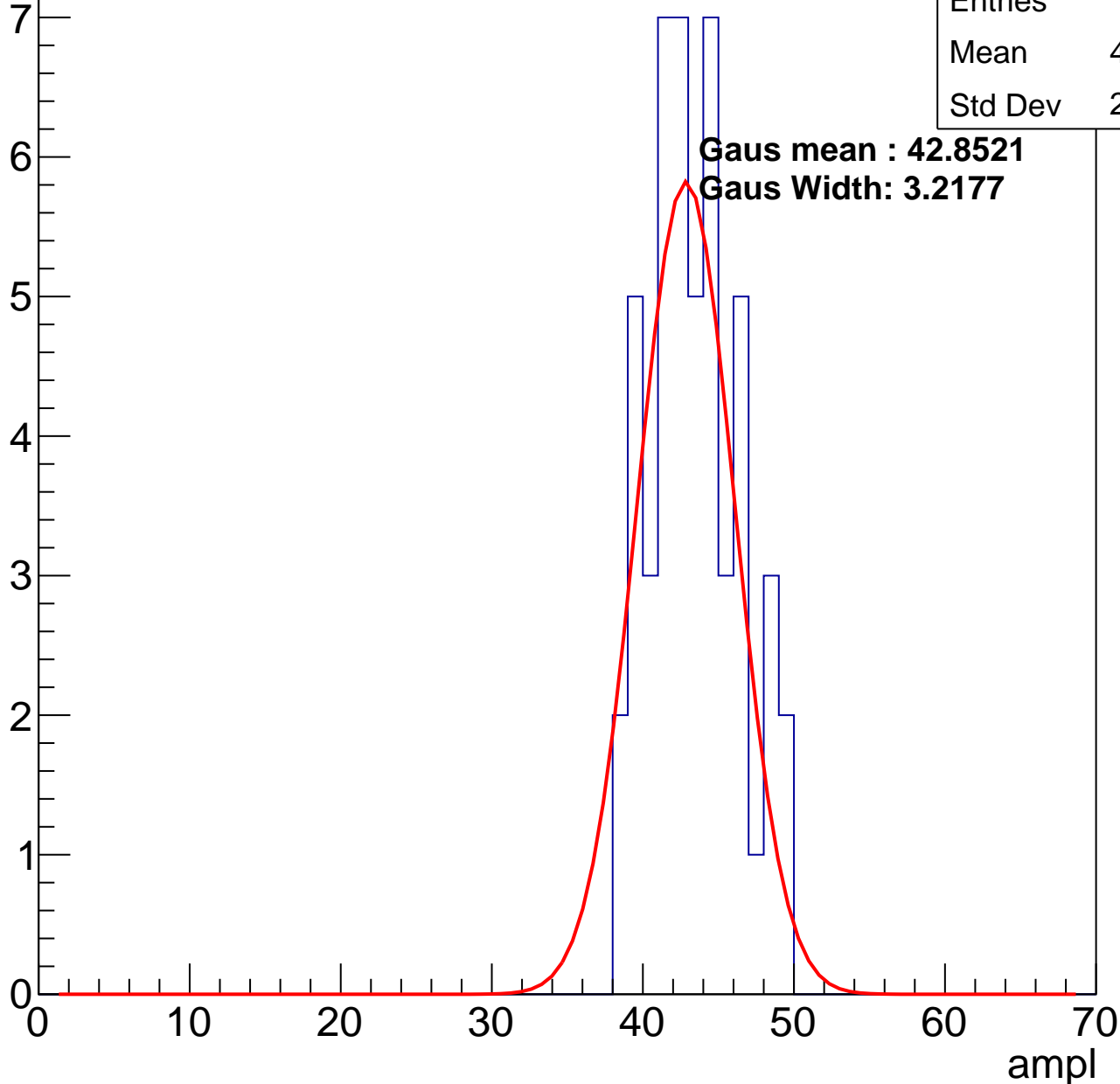
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	50
Mean	42.98
Std Dev	2.895

**Gaus mean : 42.8521**

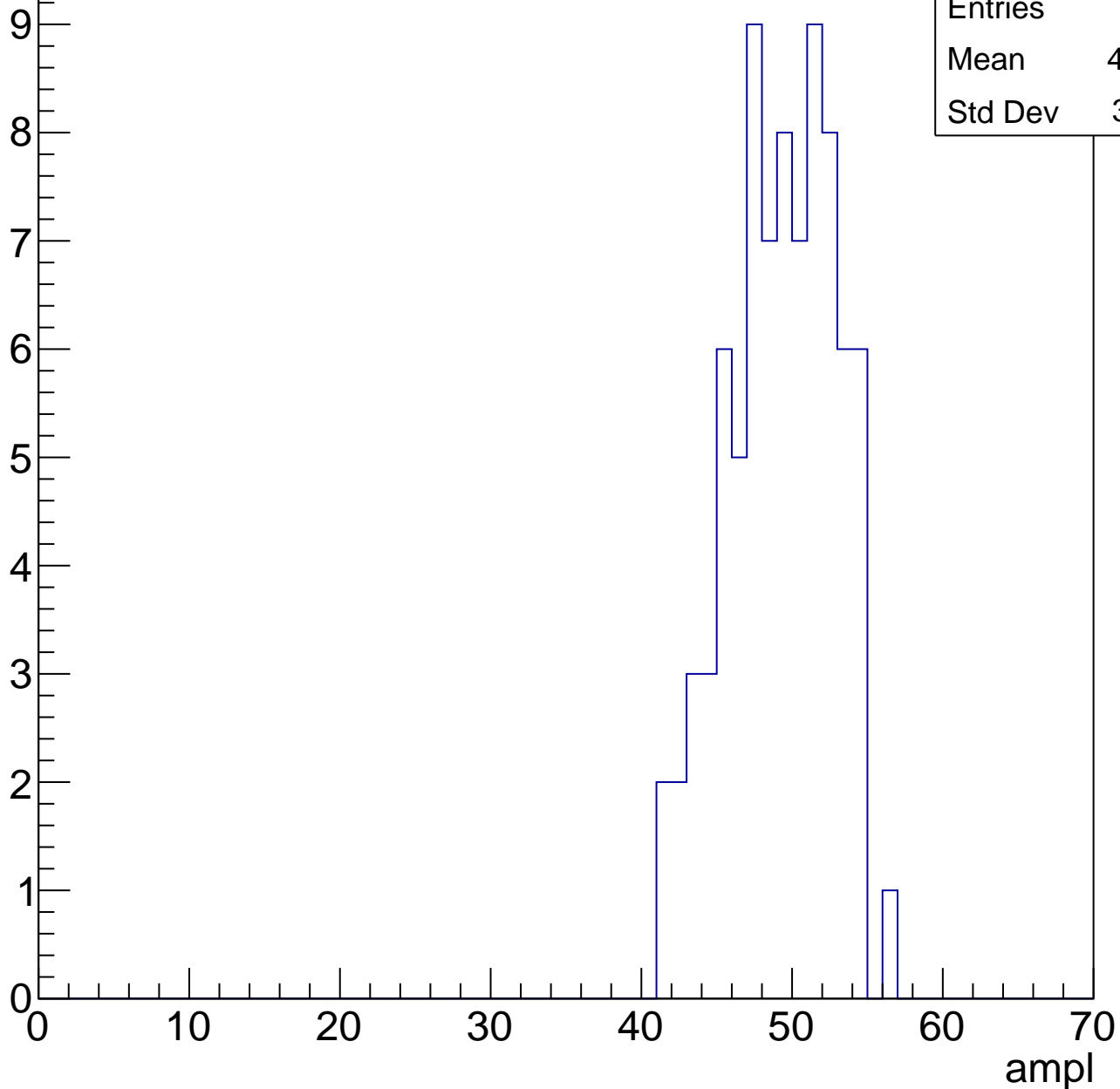
**Gaus Width: 3.2177**



# B0L002S, U2-ch80, adc3

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

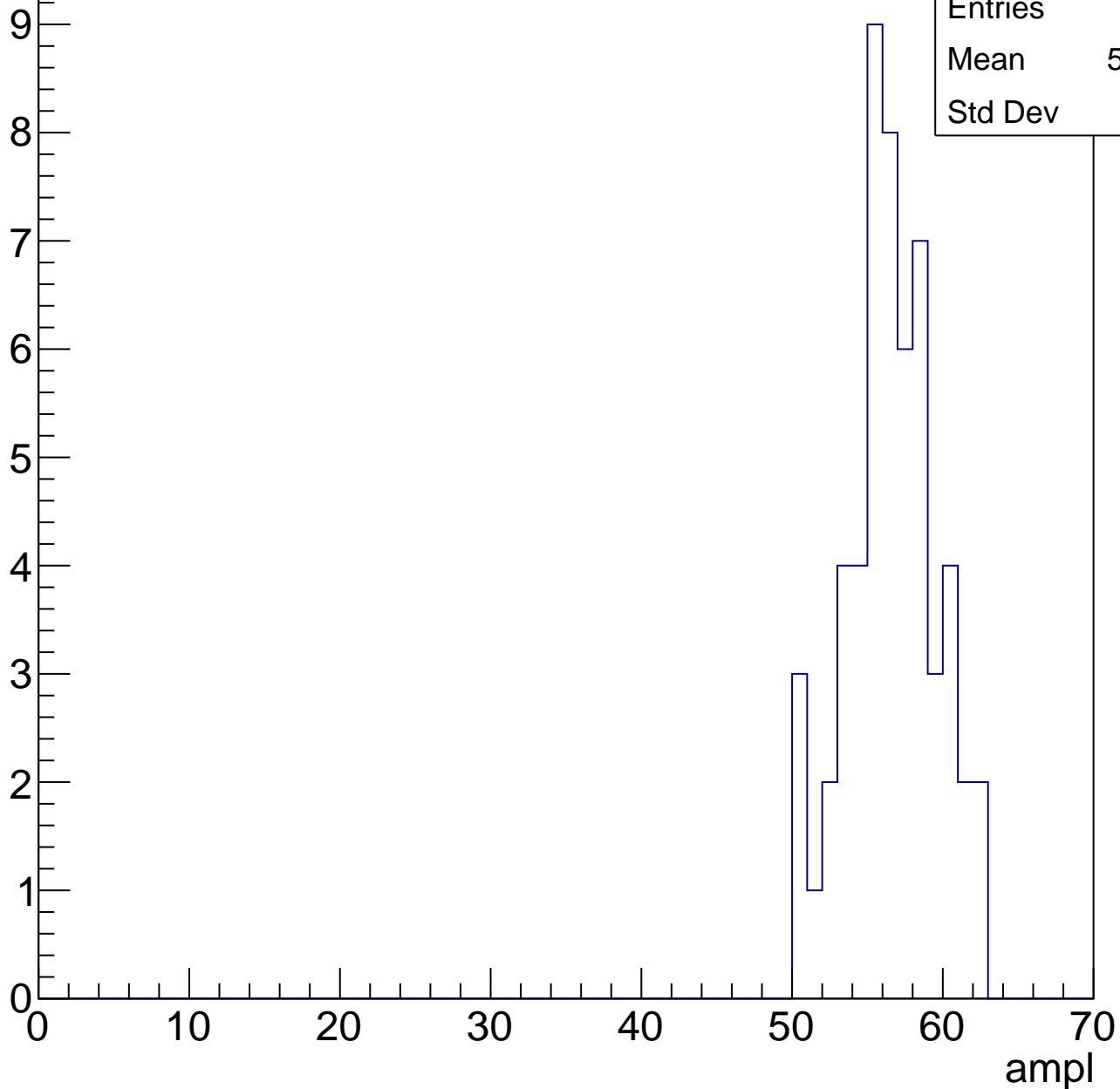


Entries	82
Mean	48.79
Std Dev	3.491

# B0L002S, U2-ch80, adc4

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

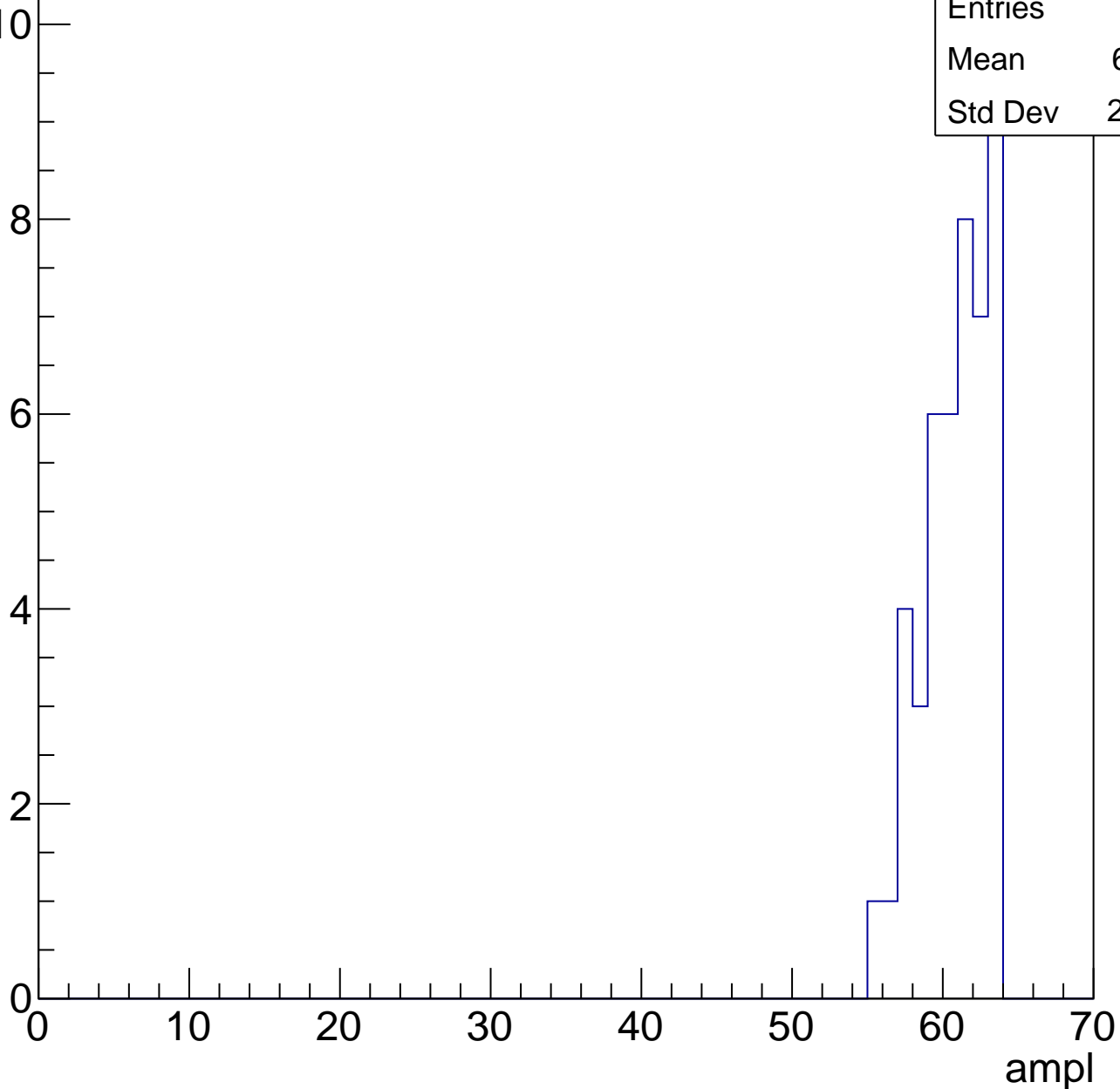


# B0L002S, U2-ch80, adc5

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

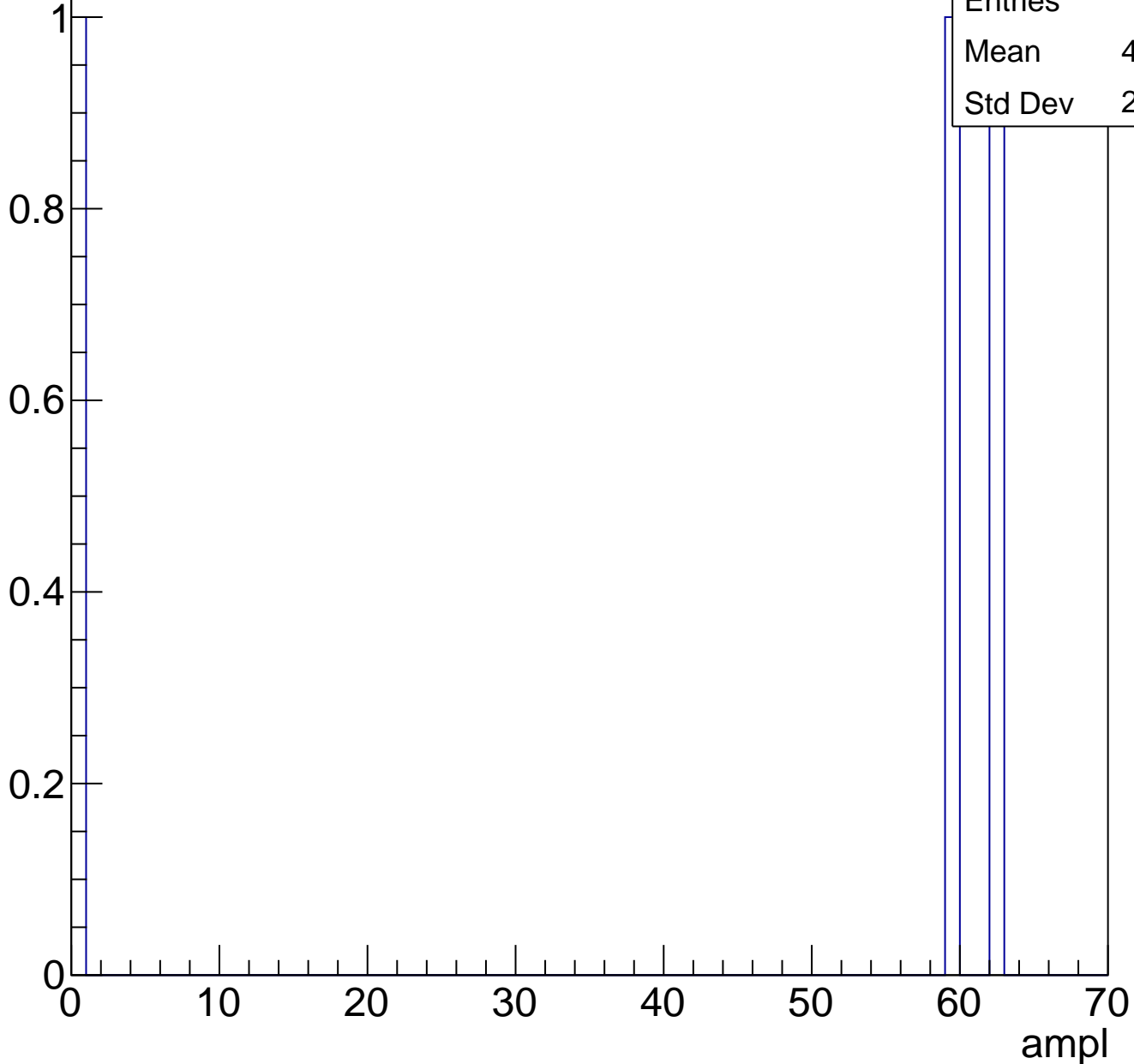
Entries	46
Mean	60.41
Std Dev	2.153



# B0L002S, U2-ch80, adc6

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry





# B0L002S, U2-ch80, adc7

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L002S, U2-ch81, adc0

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entries	63
Mean	30.41
Std Dev	3.048

**Gaus mean : 30.8092**

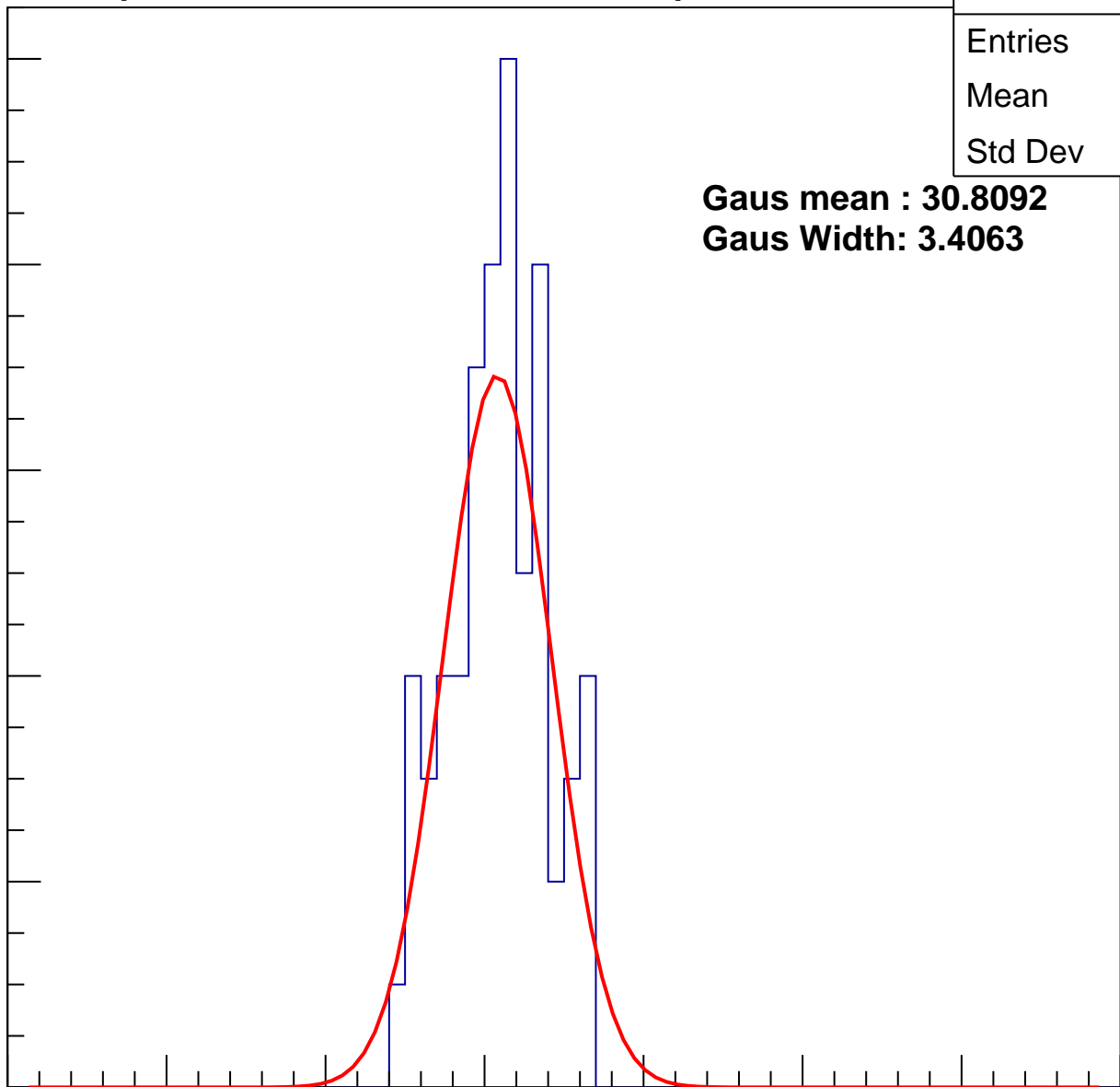
**Gaus Width: 3.4063**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L002S, U2-ch81, adc1

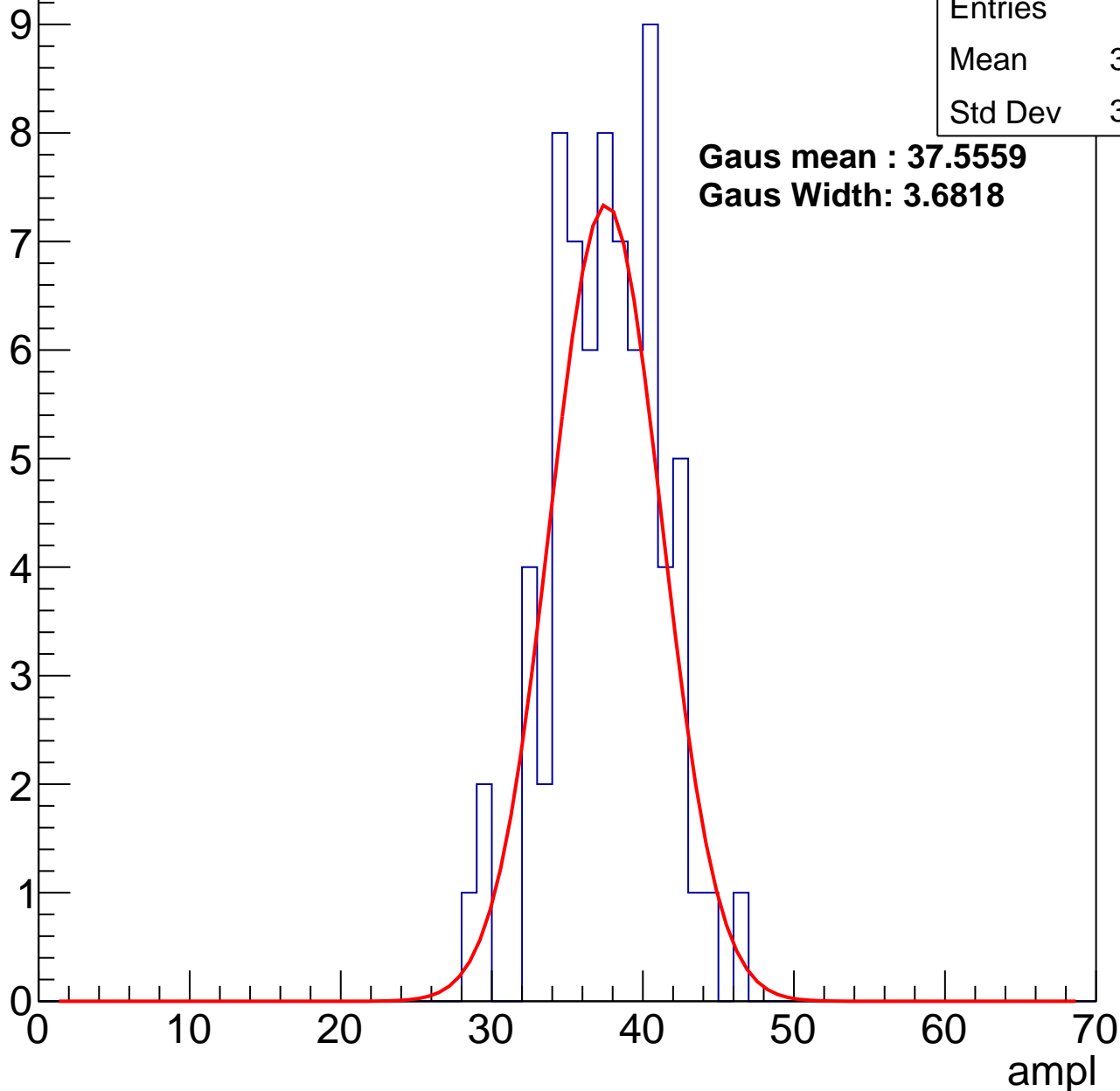
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	72
Mean	37.17
Std Dev	3.559

**Gaus mean : 37.5559**

**Gaus Width: 3.6818**



# B0L002S, U2-ch81, adc2

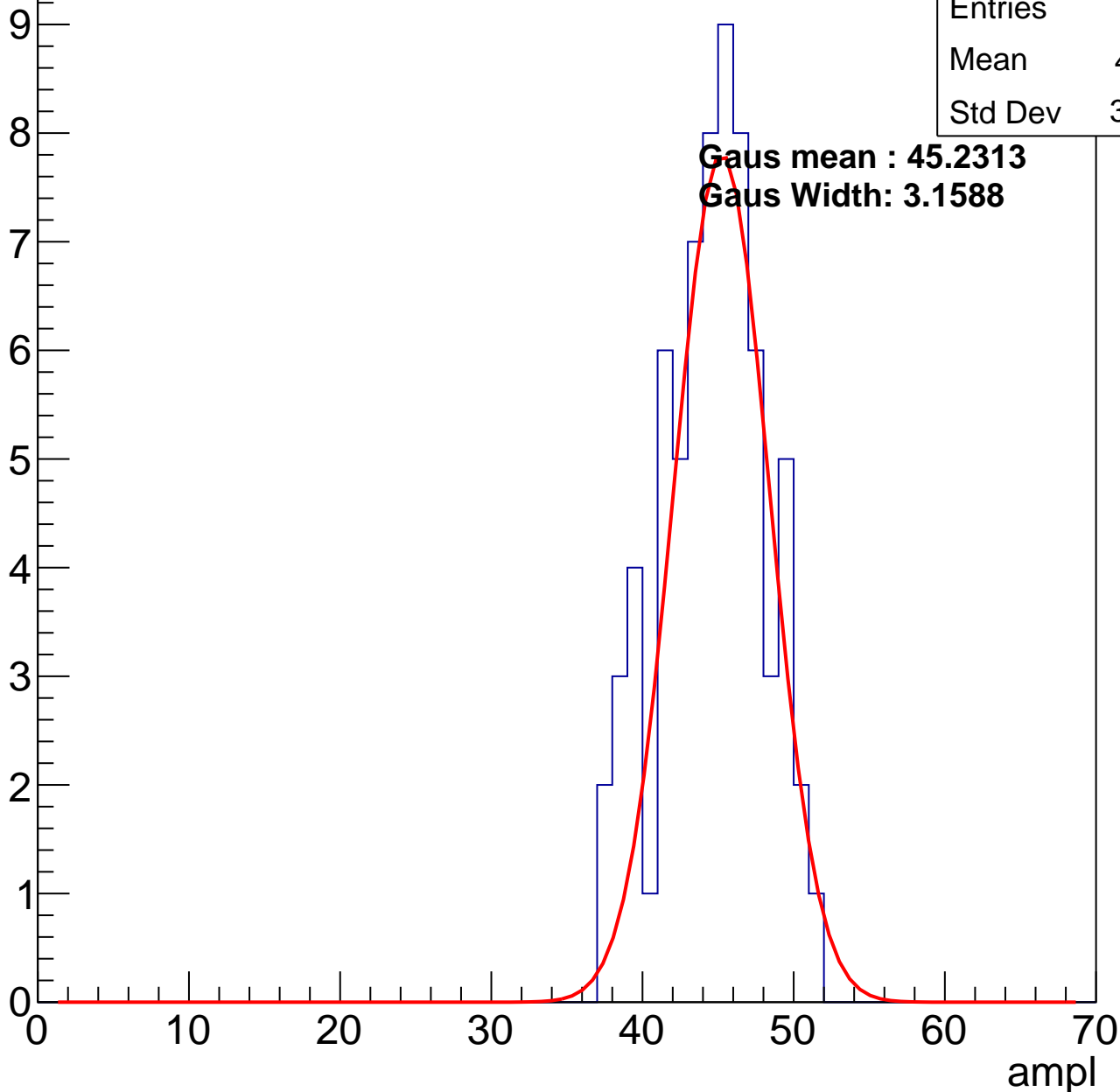
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	70
Mean	44.11
Std Dev	3.362

**Gaus mean : 45.2313**

**Gaus Width: 3.1588**

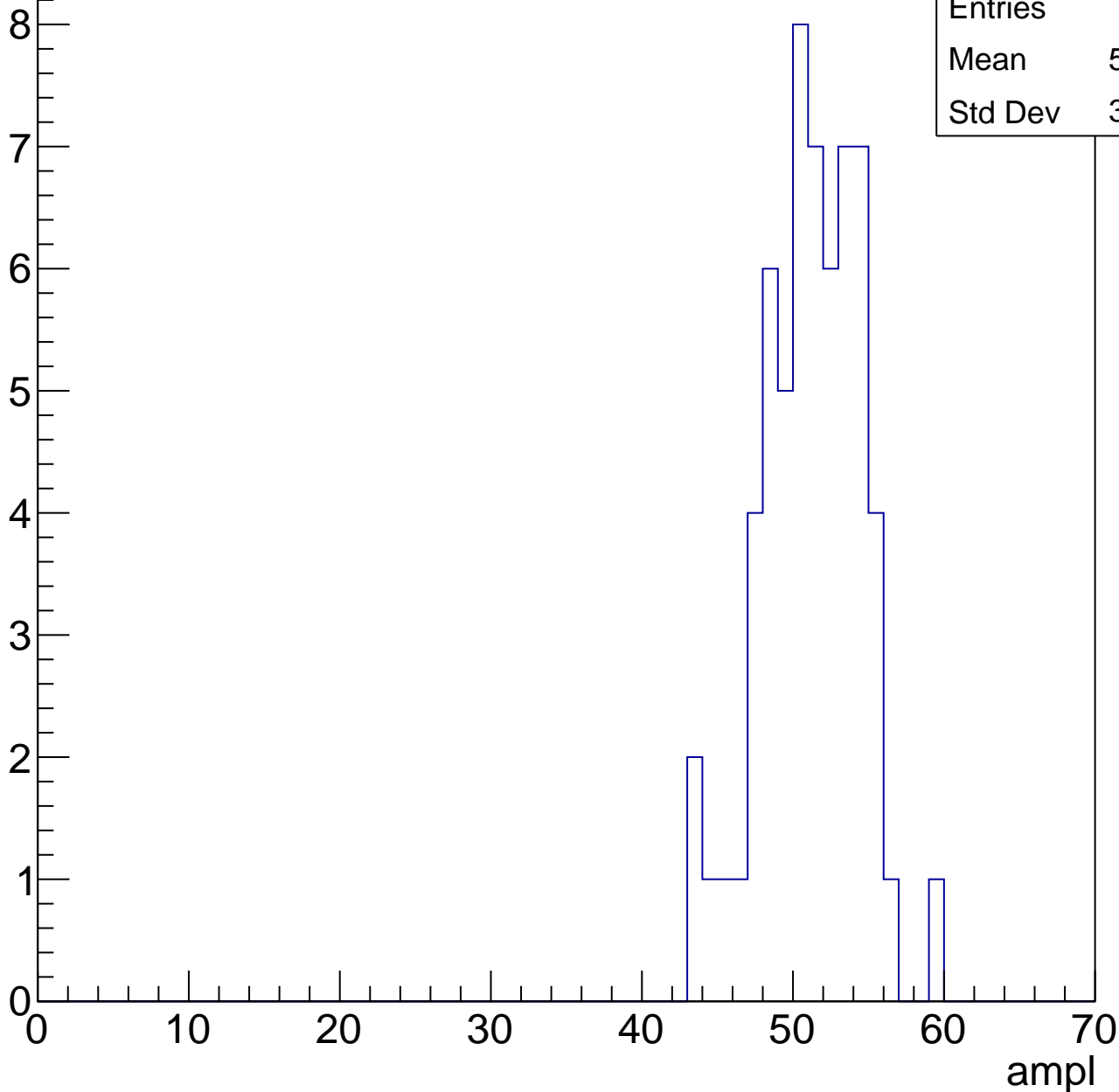


# B0L002S, U2-ch81, adc3

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	61
Mean	50.74
Std Dev	3.213

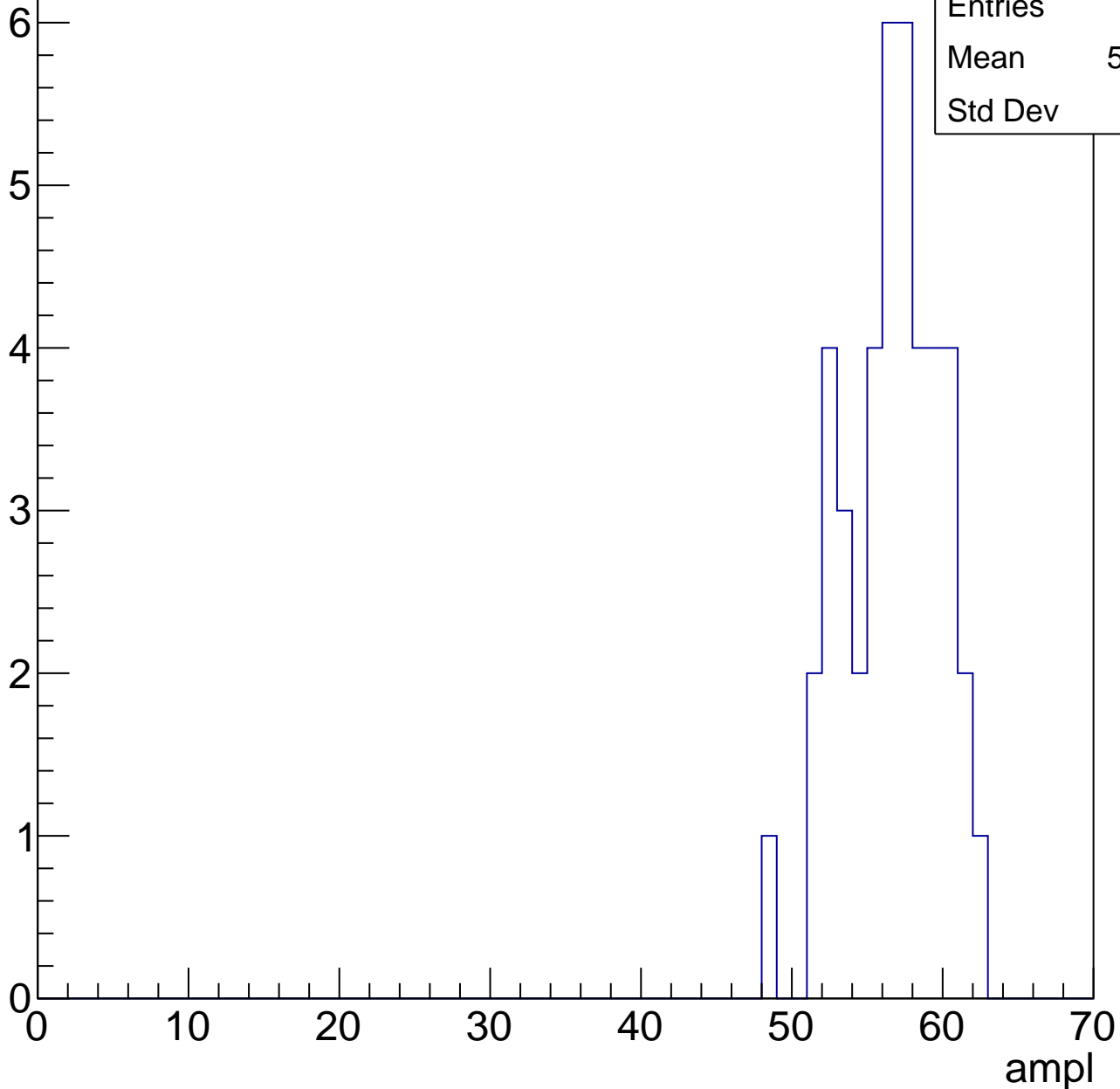


# B0L002S, U2-ch81, adc4

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	43
Mean	56.16
Std Dev	3.14

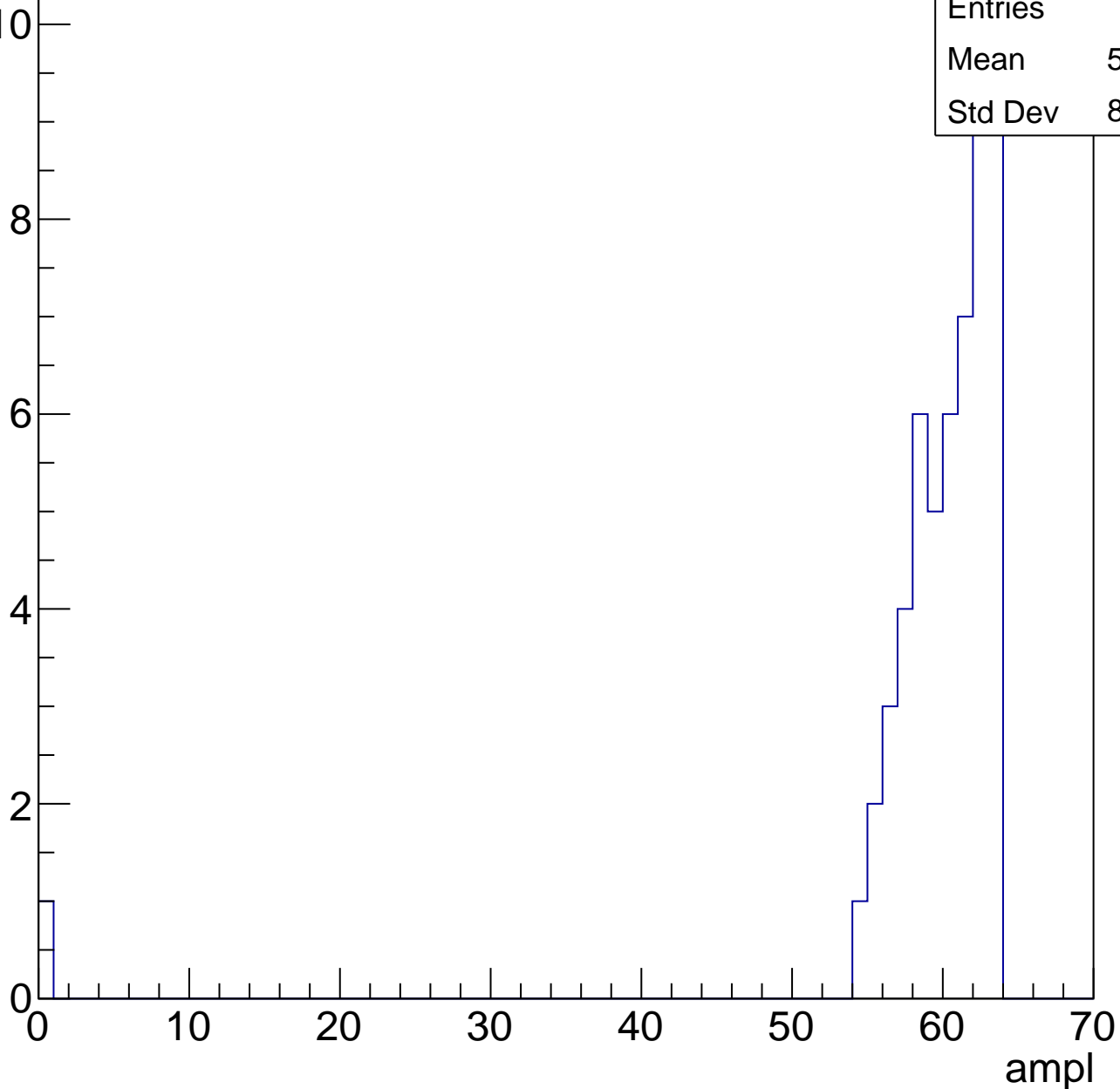


# B0L002S, U2-ch81, adc5

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	54
Mean	58.85
Std Dev	8.456



# B0L002S, U2-ch81, adc6

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry





# B0L002S, U2-ch81, adc7

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



# B0L002S, U2-ch82, adc0

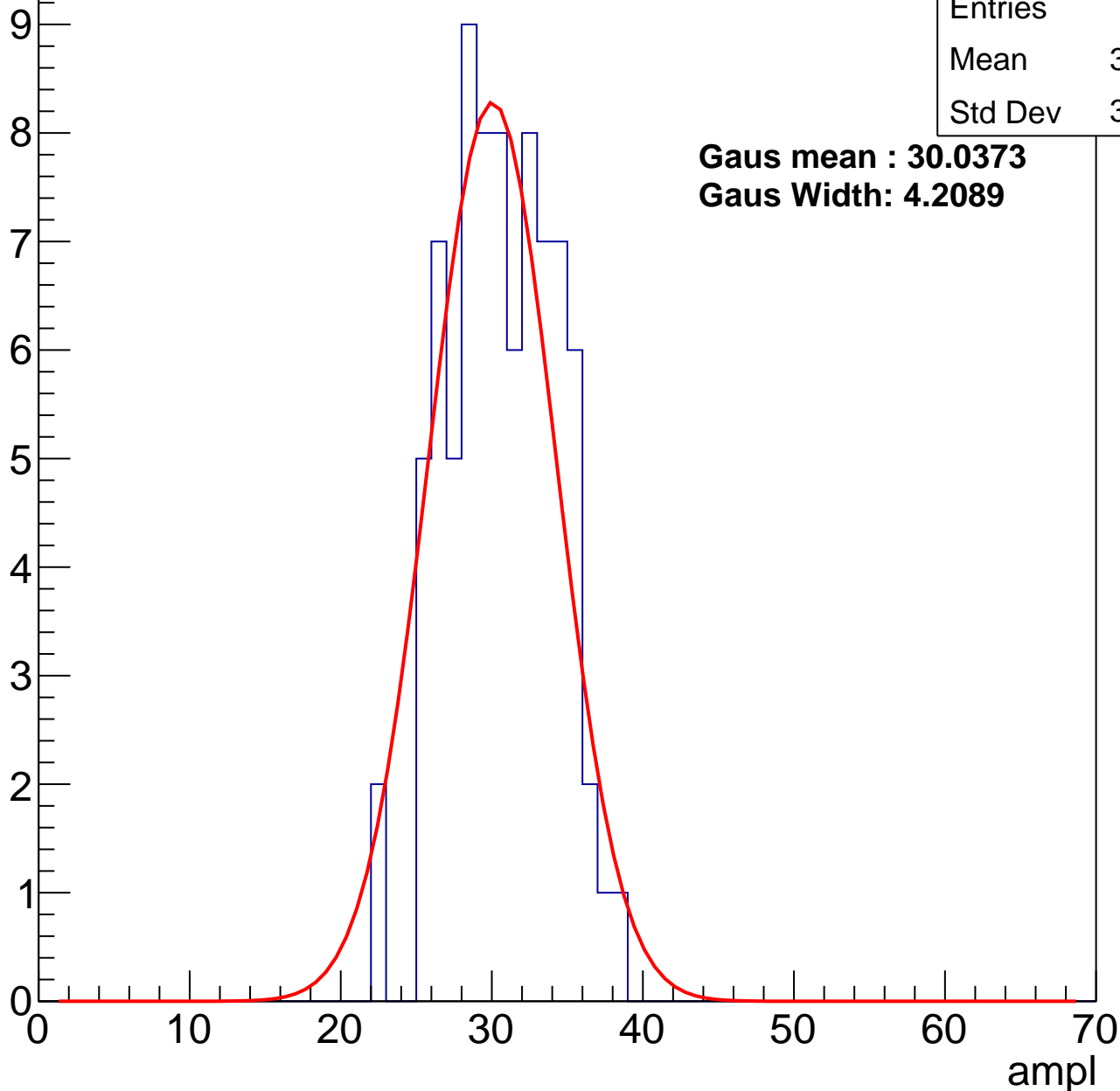
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	82
Mean	30.22
Std Dev	3.489

**Gaus mean : 30.0373**

**Gaus Width: 4.2089**



# B0L002S, U2-ch82, adc1

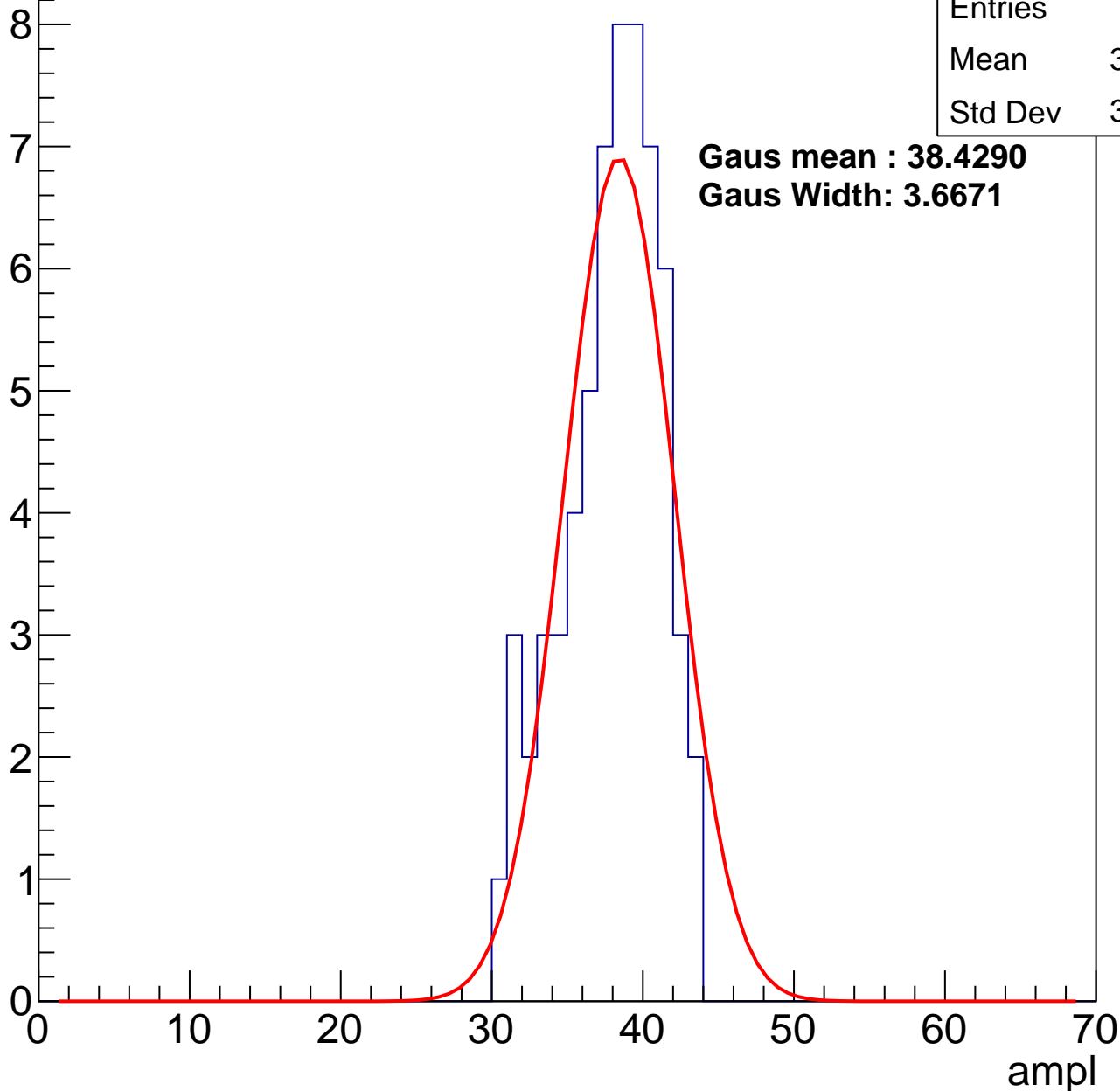
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	62
Mean	37.44
Std Dev	3.206

**Gaus mean : 38.4290**

**Gaus Width: 3.6671**



# B0L002S, U2-ch82, adc2

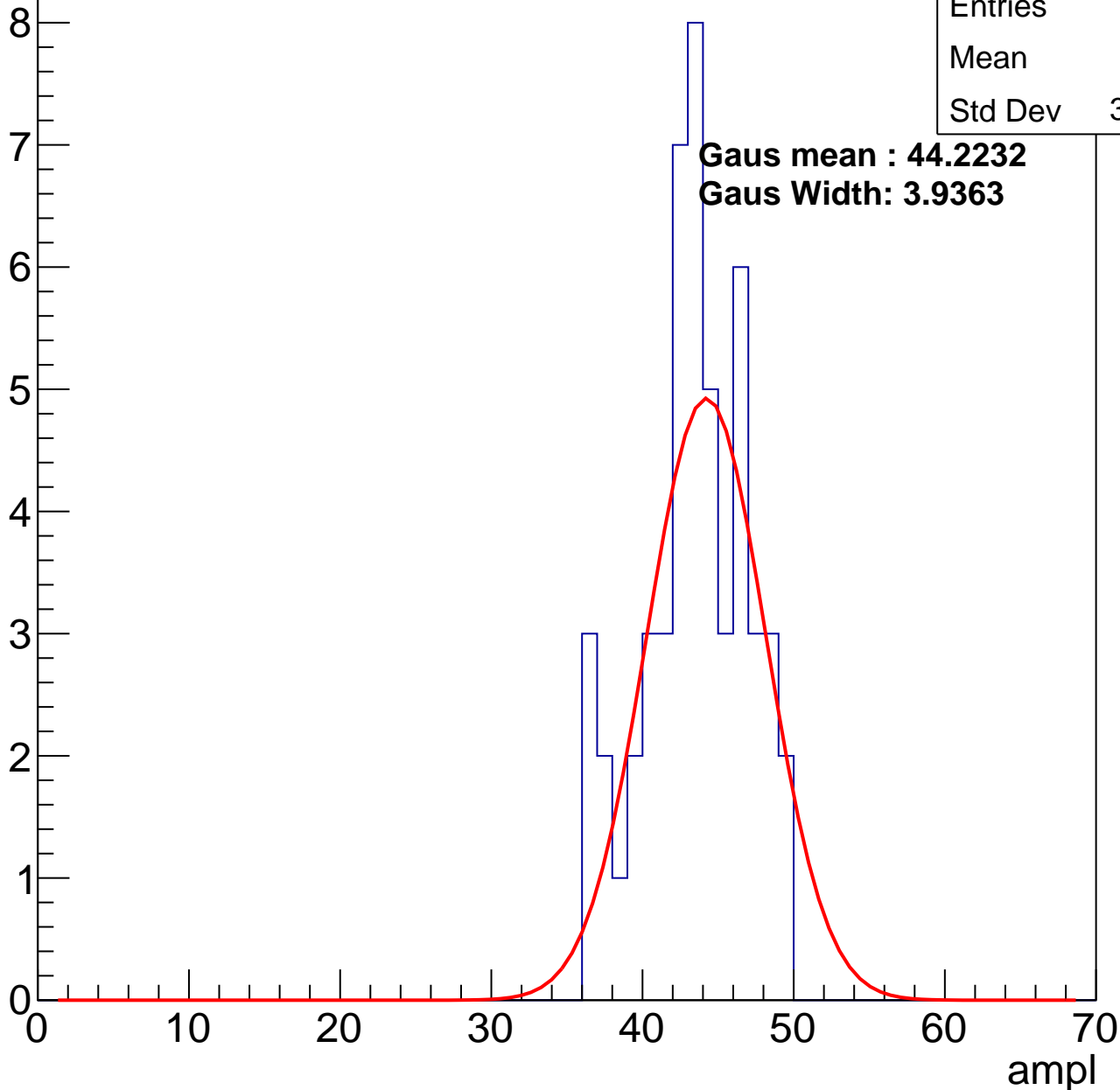
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	51
Mean	43
Std Dev	3.395

**Gaus mean : 44.2232**

**Gaus Width: 3.9363**

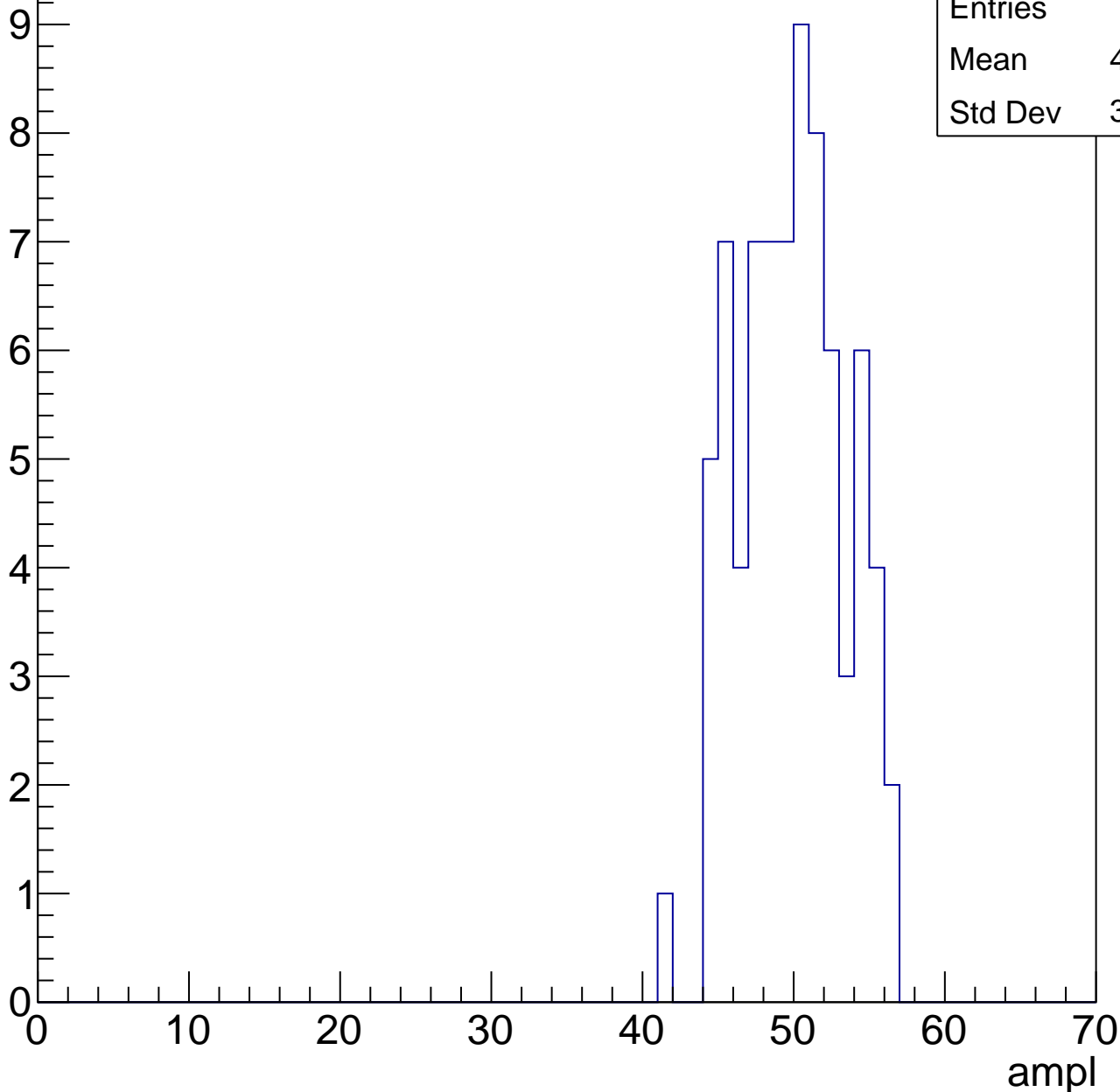


# B0L002S, U2-ch82, adc3

calib\_packv5\_042523\_0143.root, FC#8, port C1

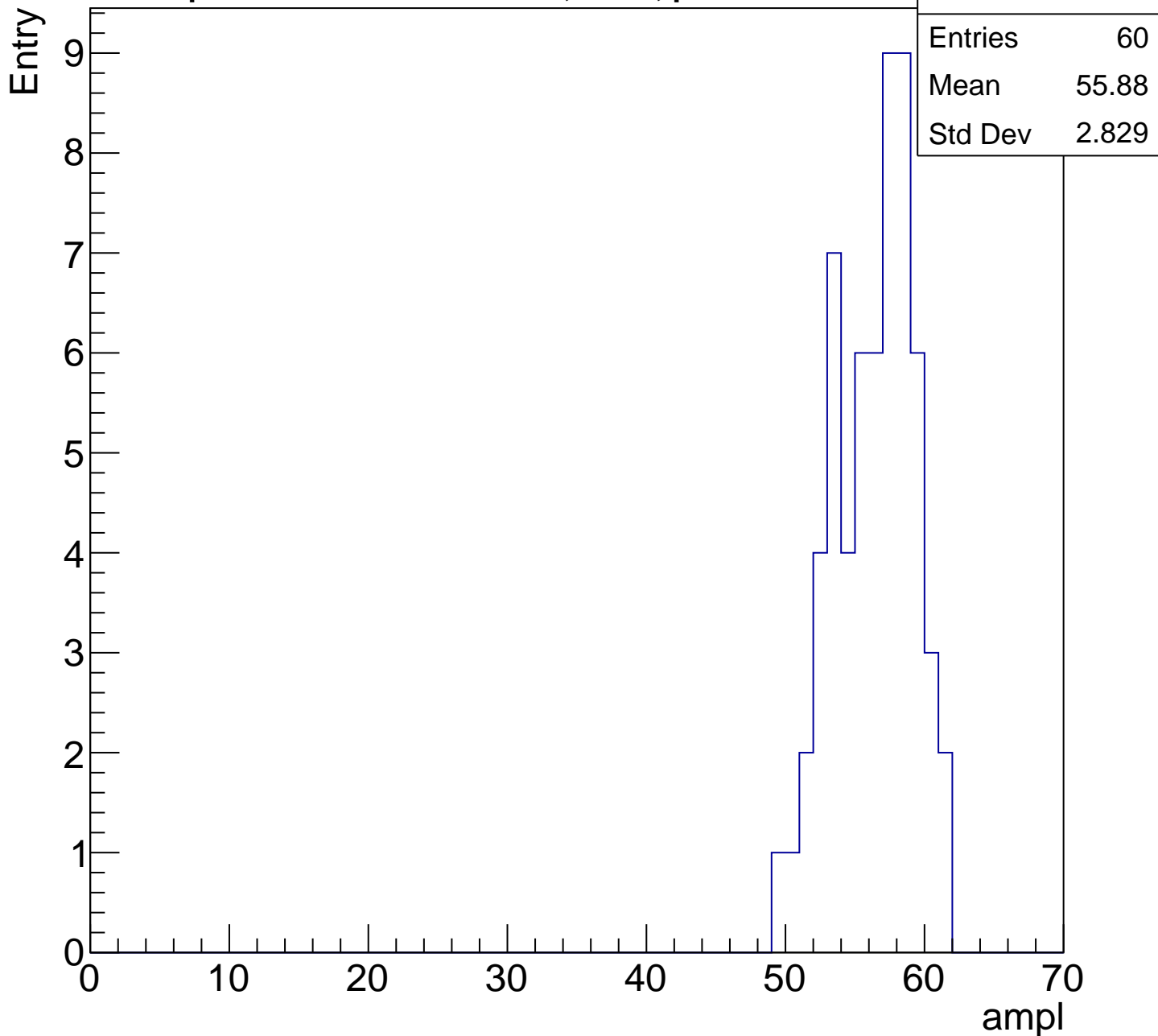
Entry

Entries	76
Mean	49.38
Std Dev	3.433



# B0L002S, U2-ch82, adc4

calib\_packv5\_042523\_0143.root, FC#8, port C1



# B0L002S, U2-ch82, adc5

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	41
Mean	59.37
Std Dev	9.568

ampl

0 10 20 30 40 50 60 70

1

2

3

4

5

6

7

8

9

# B0L002S, U2-ch82, adc6

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry





# B0L002S, U2-ch82, adc7

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L002S, U2-ch83, adc0

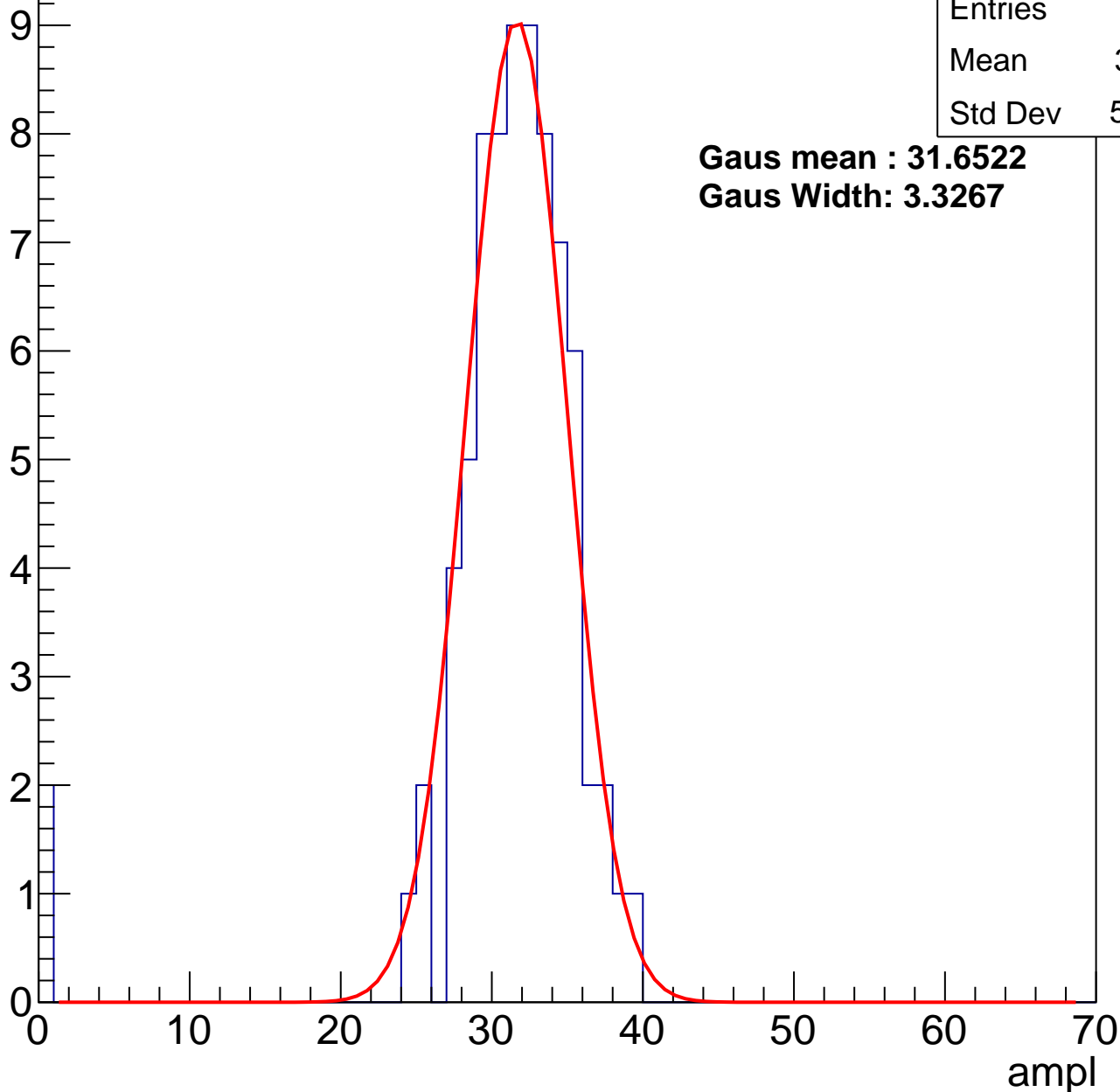
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	75
Mean	30.61
Std Dev	5.906

**Gaus mean : 31.6522**

**Gaus Width: 3.3267**



# B0L002S, U2-ch83, adc1

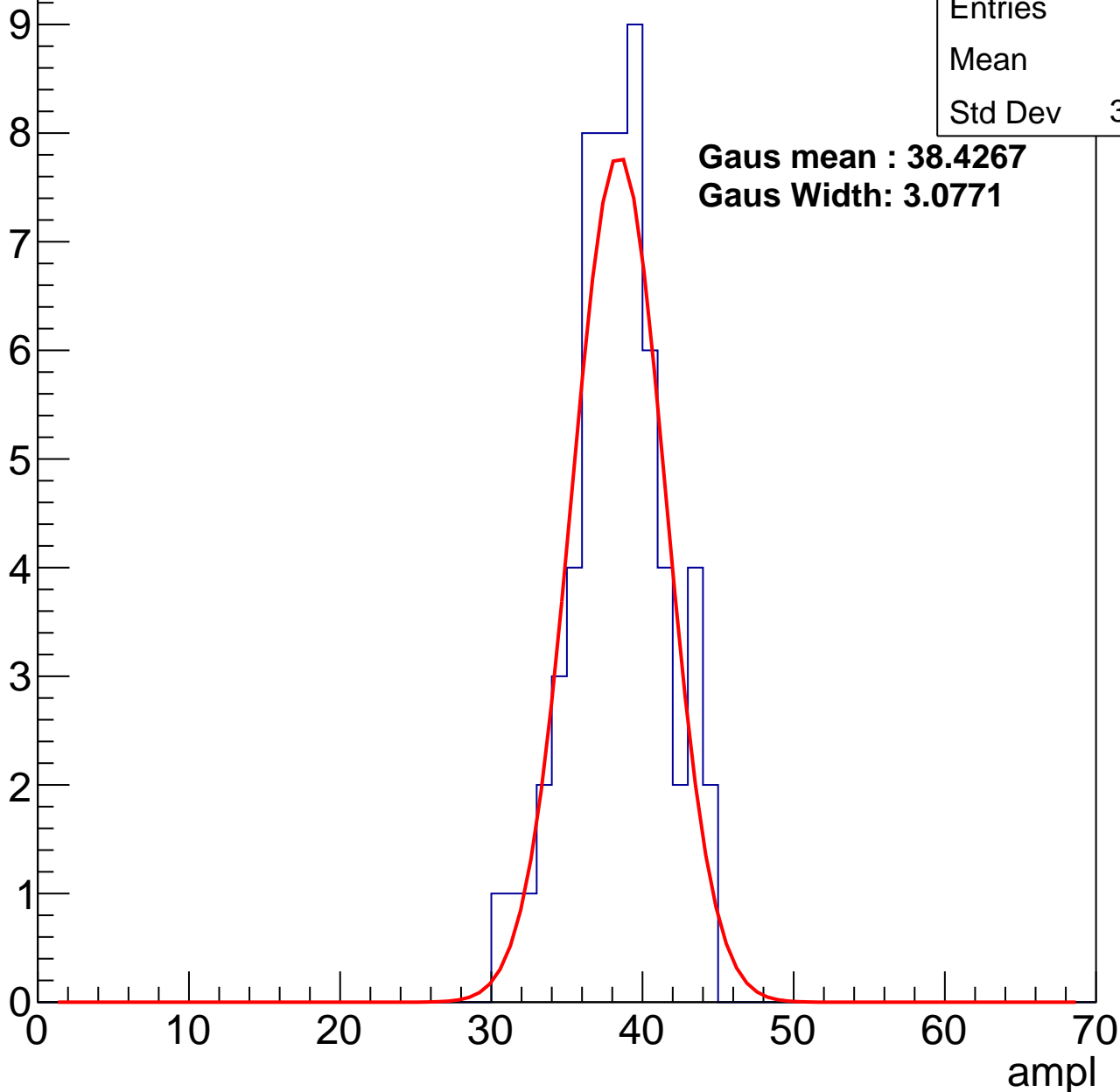
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	63
Mean	37.9
Std Dev	3.074

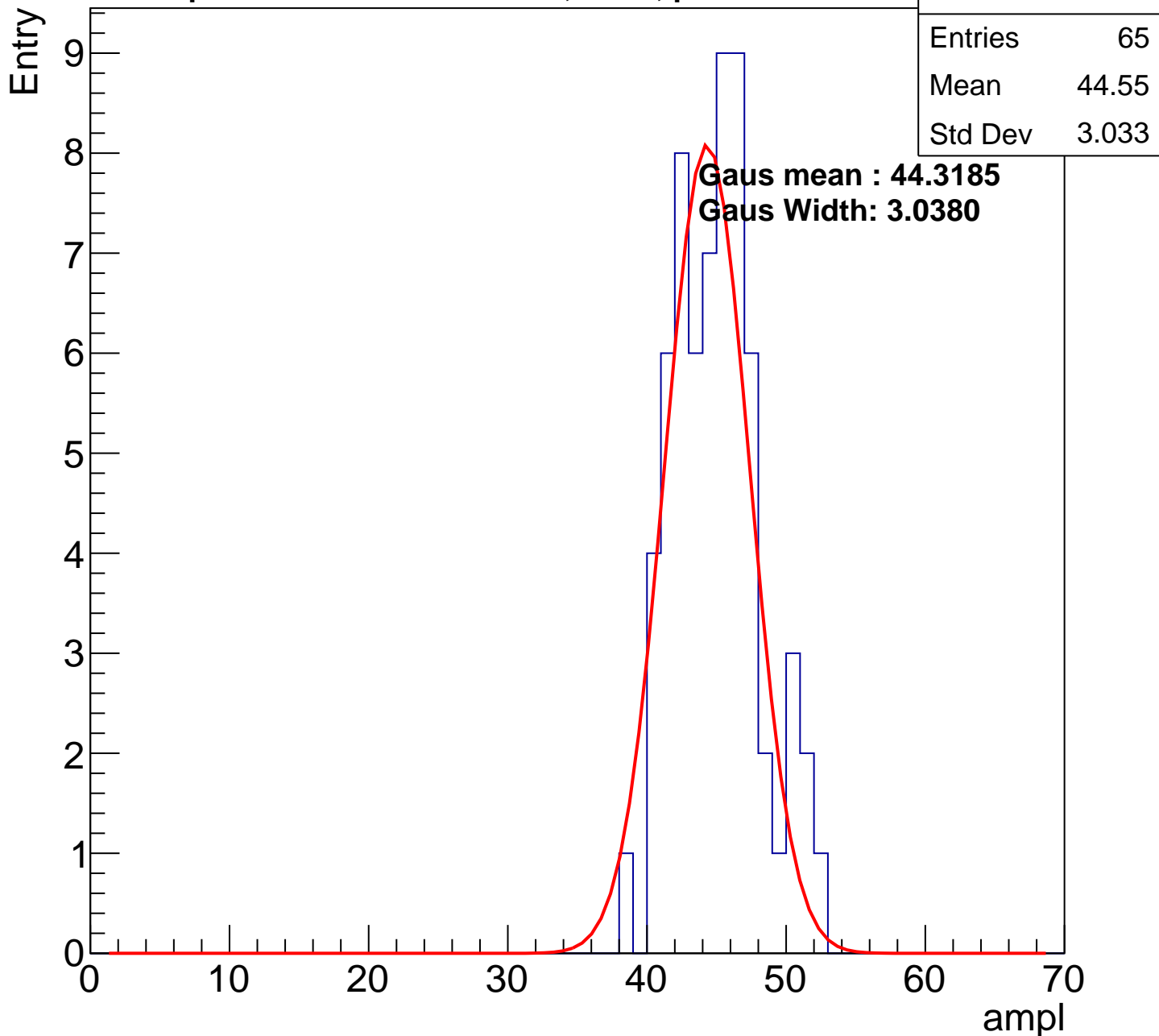
**Gaus mean : 38.4267**

**Gaus Width: 3.0771**



# B0L002S, U2-ch83, adc2

calib\_packv5\_042523\_0143.root, FC#8, port C1

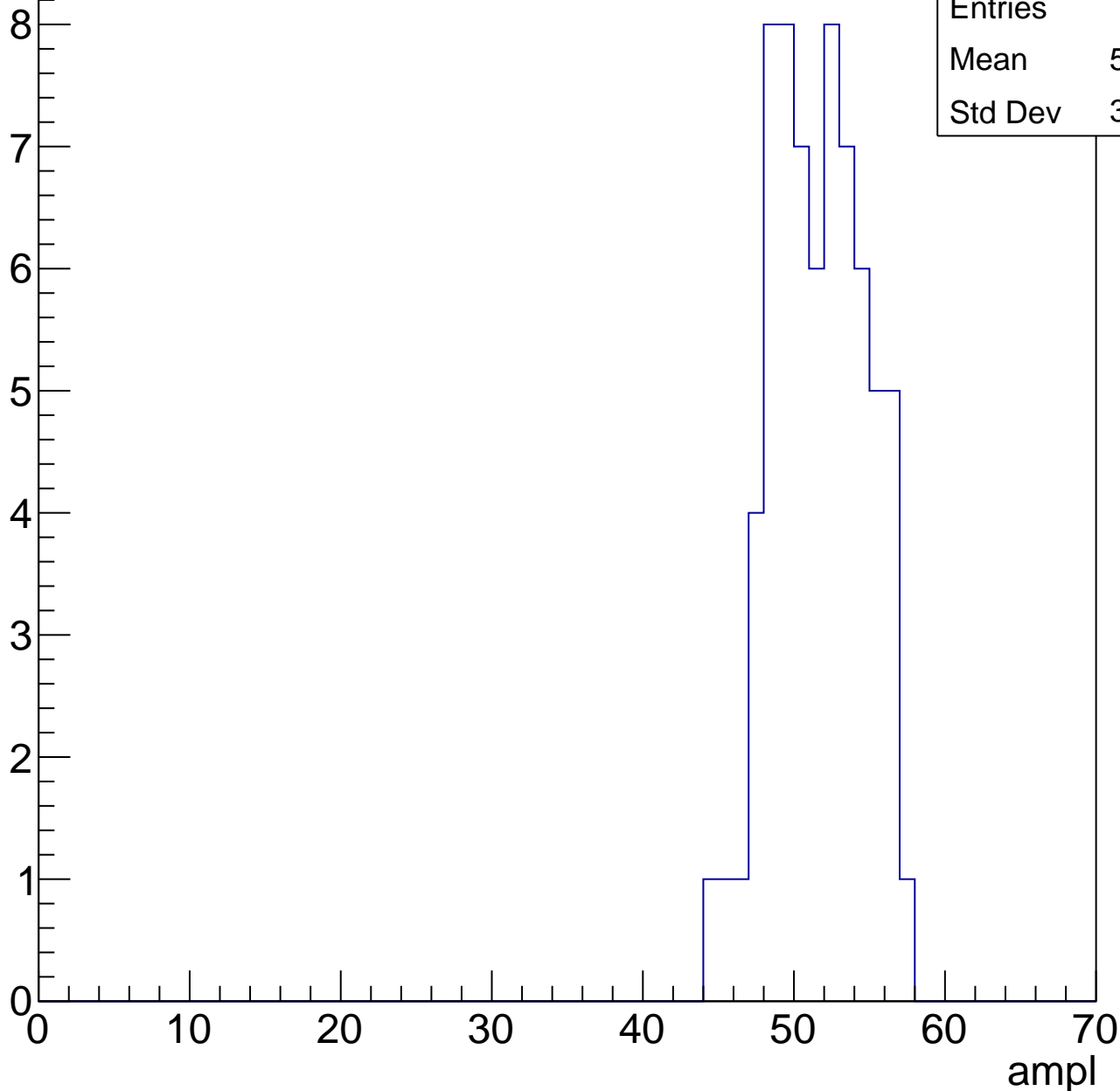


# B0L002S, U2-ch83, adc3

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	68
Mean	51.15
Std Dev	3.006



# B0L002S, U2-ch83, adc4

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entries	53
Mean	56.91
Std Dev	2.756

Entry

10

8

6

4

2

0

0

10

20

30

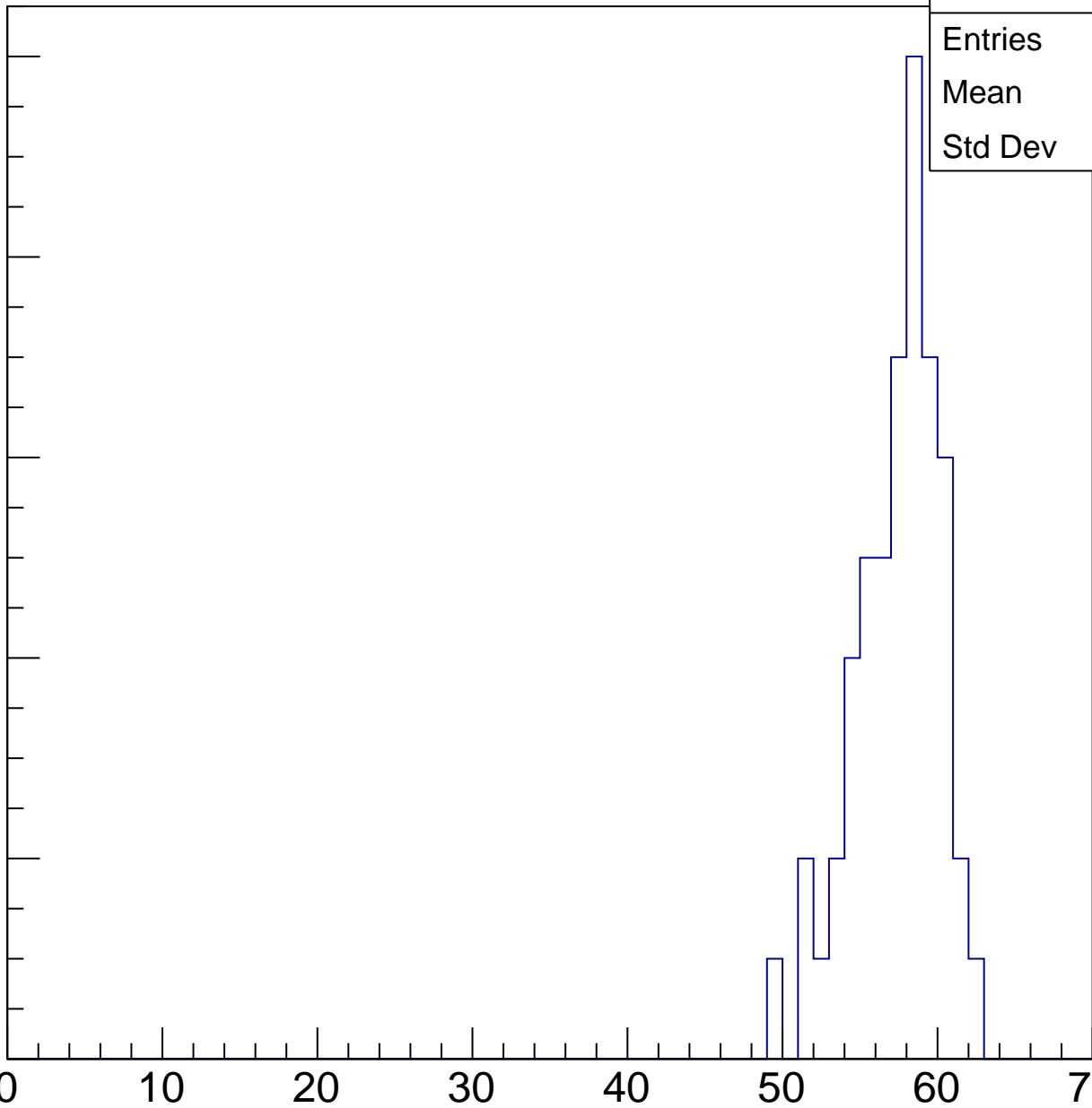
40

50

60

70

ampl

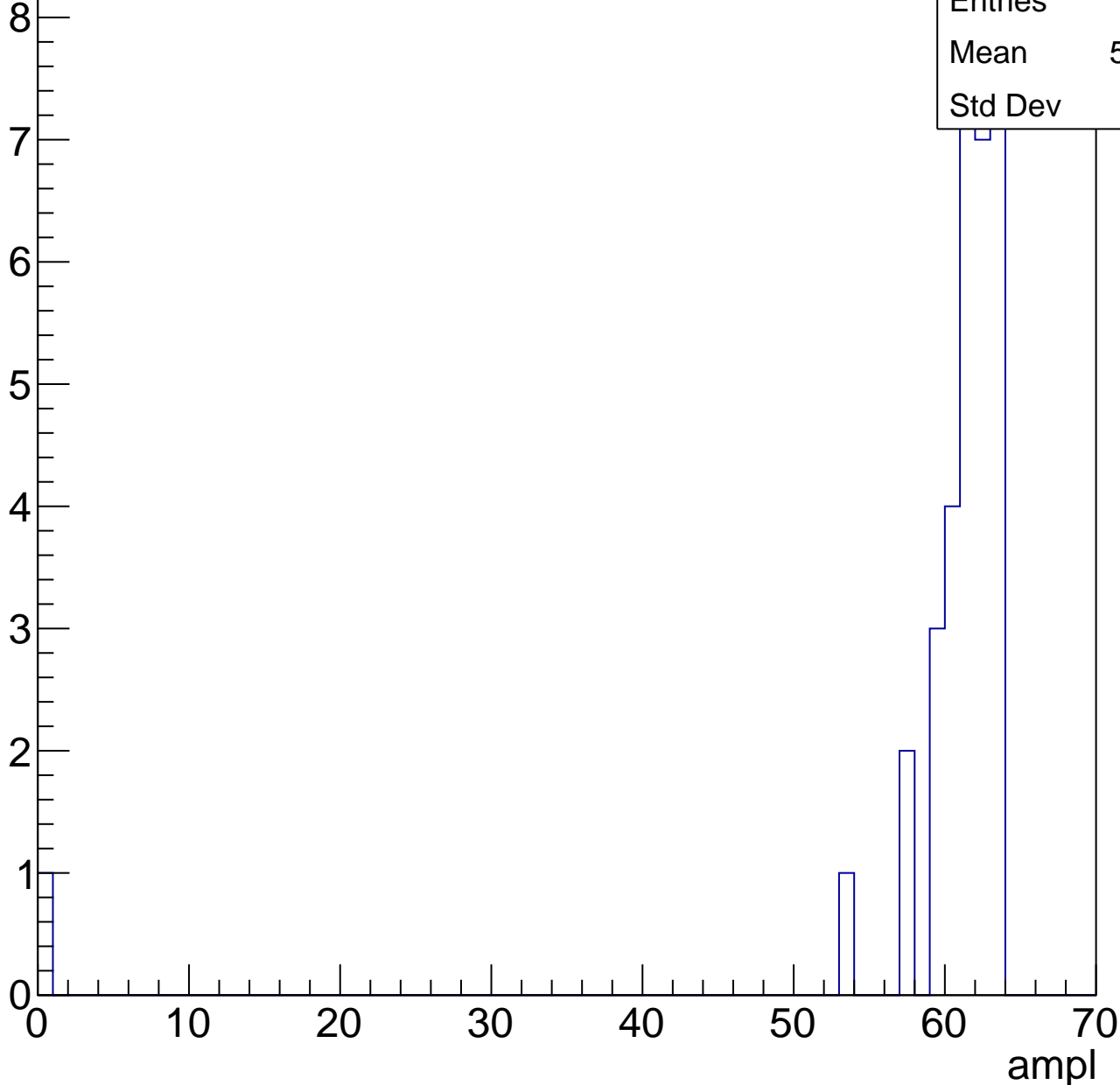


# B0L002S, U2-ch83, adc5

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

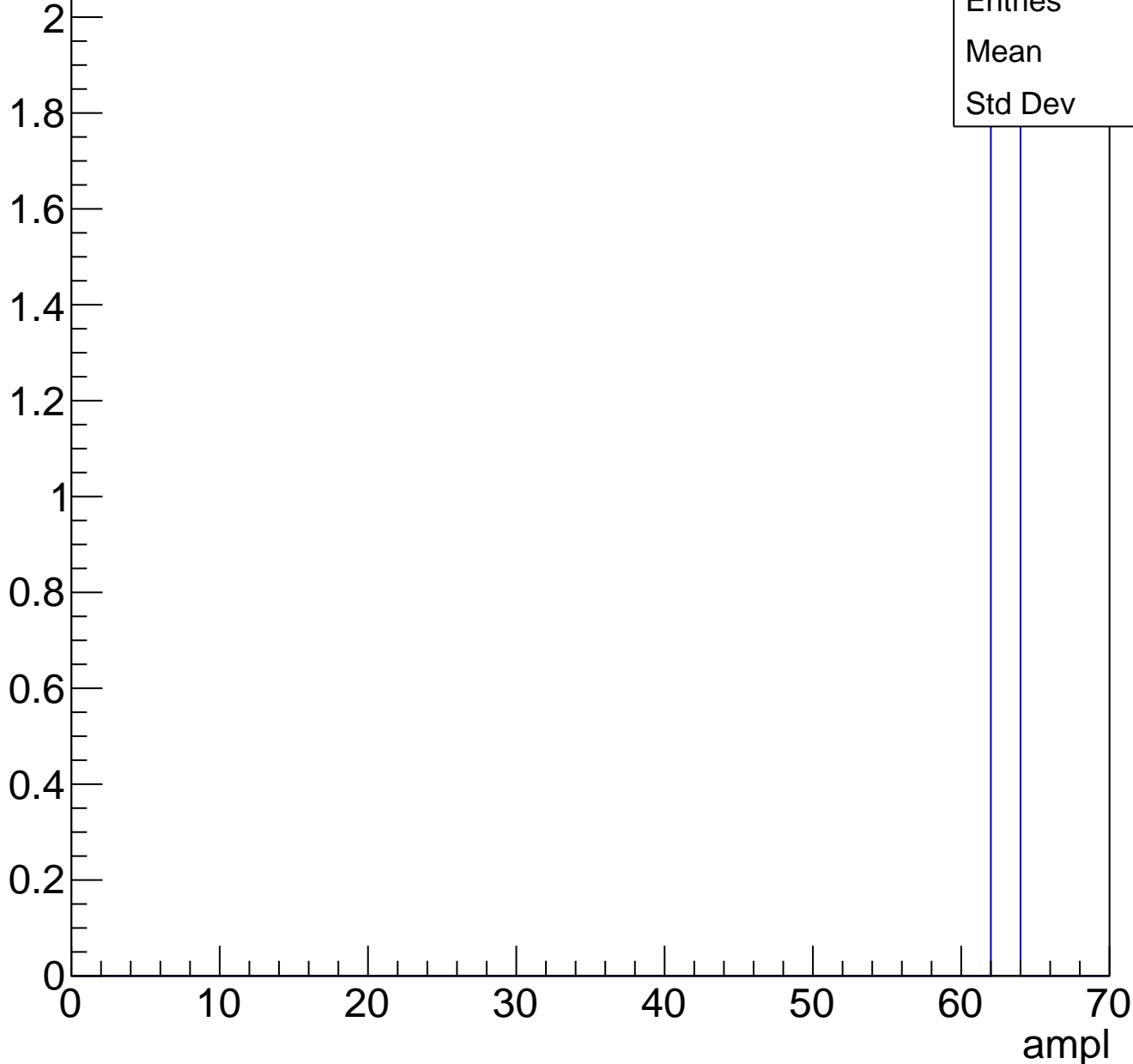
Entries	34
Mean	59.12
Std Dev	10.5



# B0L002S, U2-ch83, adc6

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry





# B0L002S, U2-ch83, adc7

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



# B0L002S, U2-ch84, adc0

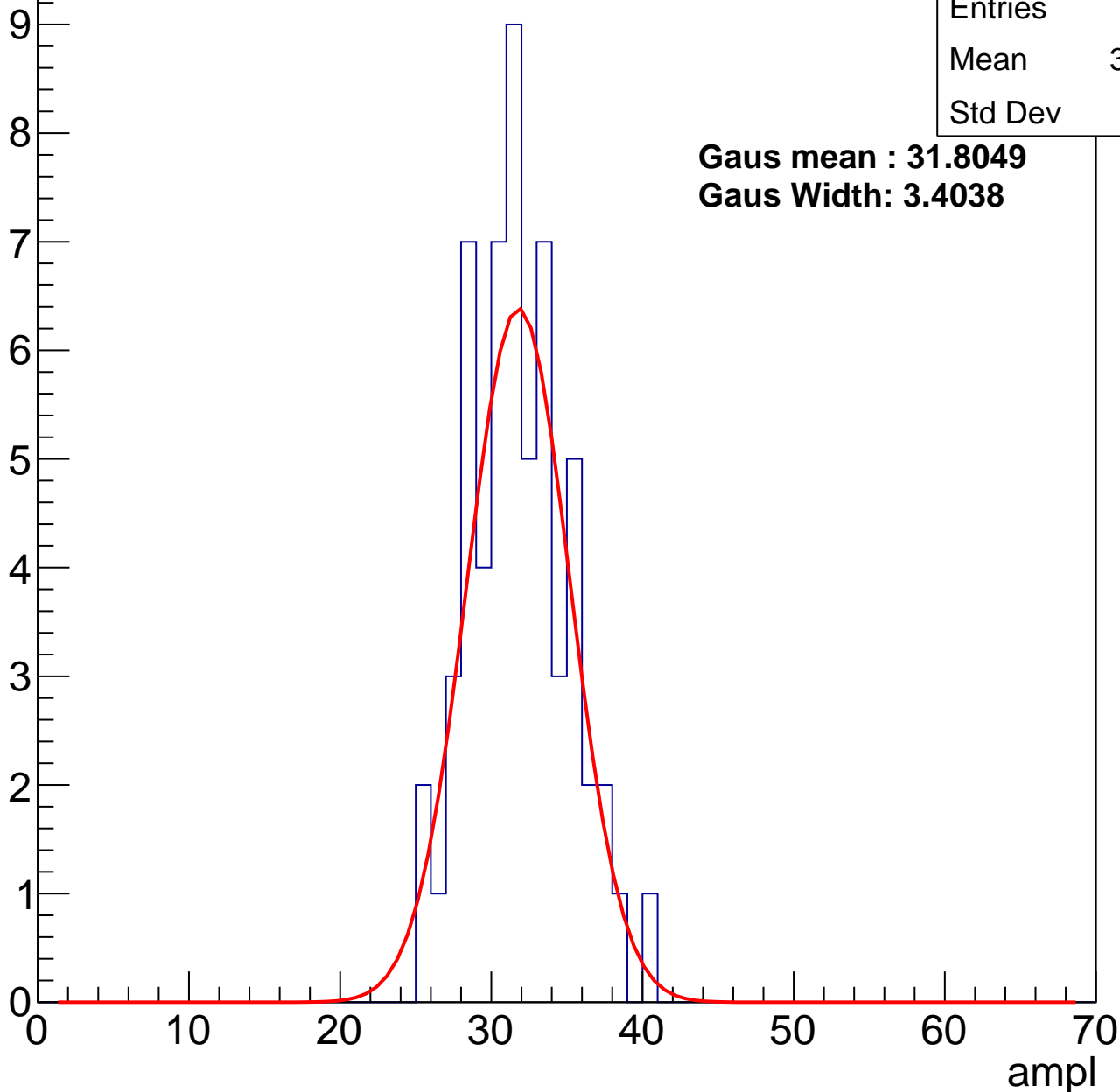
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	59
Mean	31.36
Std Dev	3.23

**Gaus mean : 31.8049**

**Gaus Width: 3.4038**



# B0L002S, U2-ch84, adc1

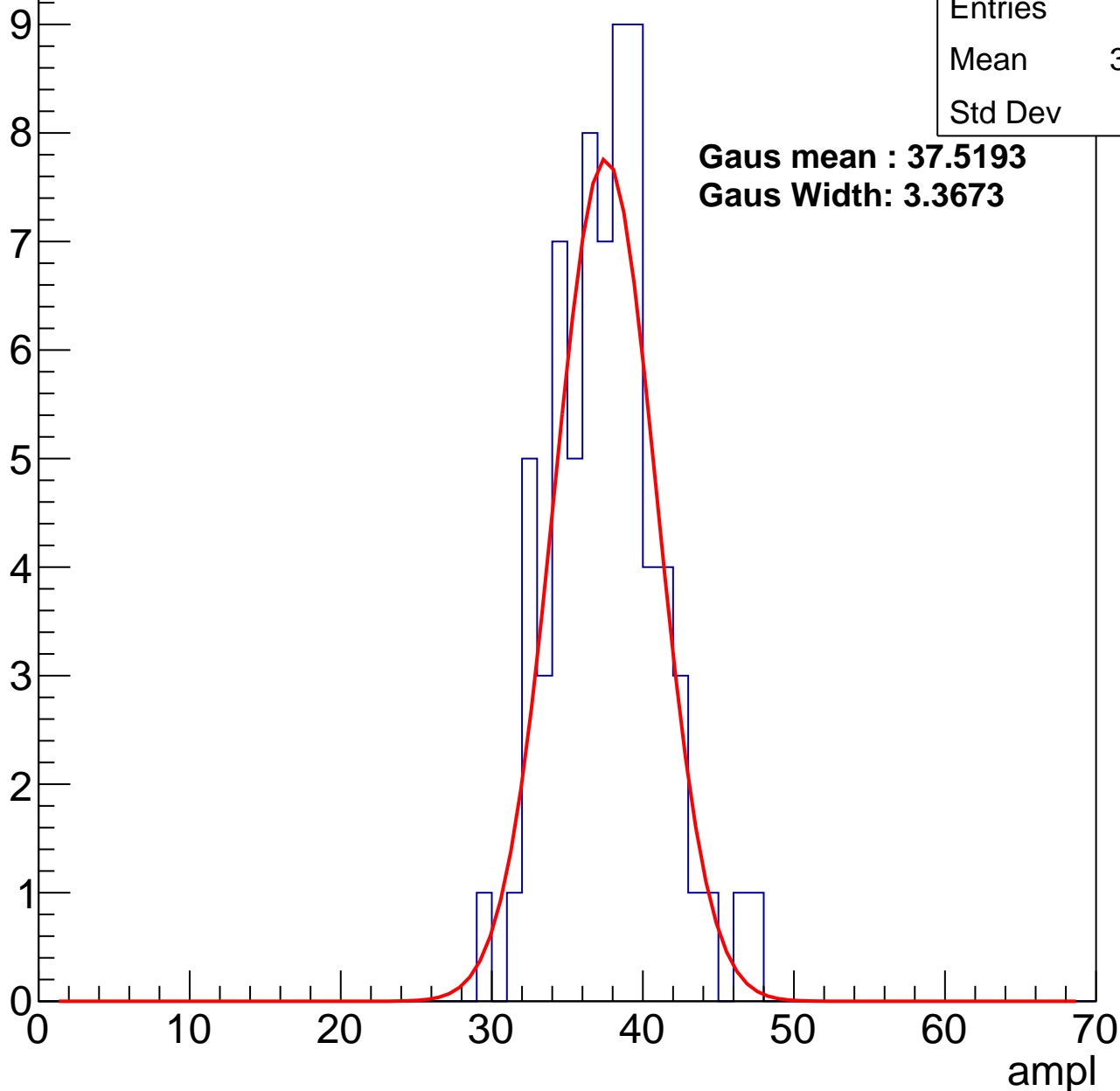
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	70
Mean	37.17
Std Dev	3.48

**Gaus mean : 37.5193**

**Gaus Width: 3.3673**



# B0L002S, U2-ch84, adc2

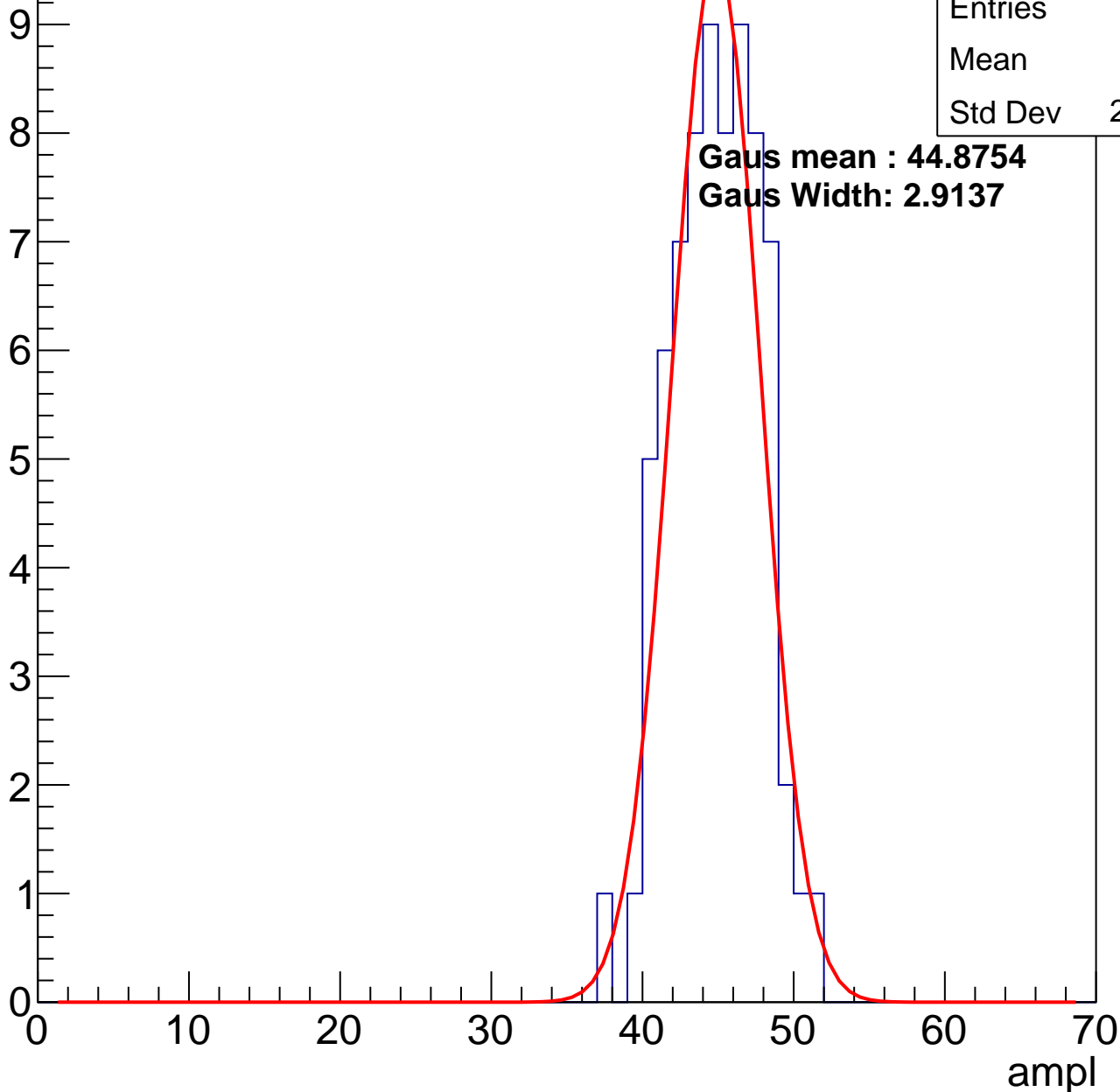
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	73
Mean	44.4
Std Dev	2.856

**Gaus mean : 44.8754**

**Gaus Width: 2.9137**

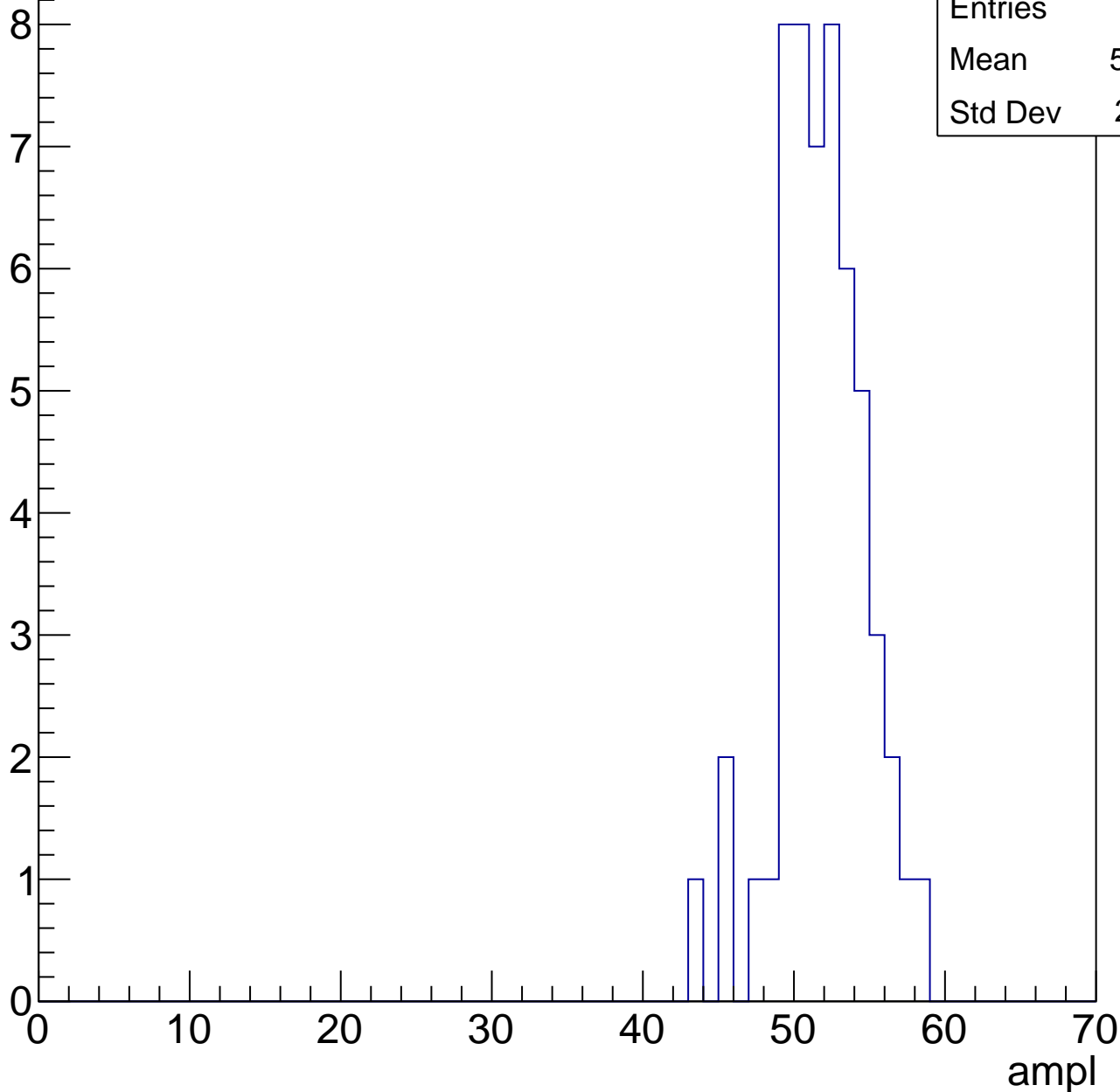


# B0L002S, U2-ch84, adc3

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

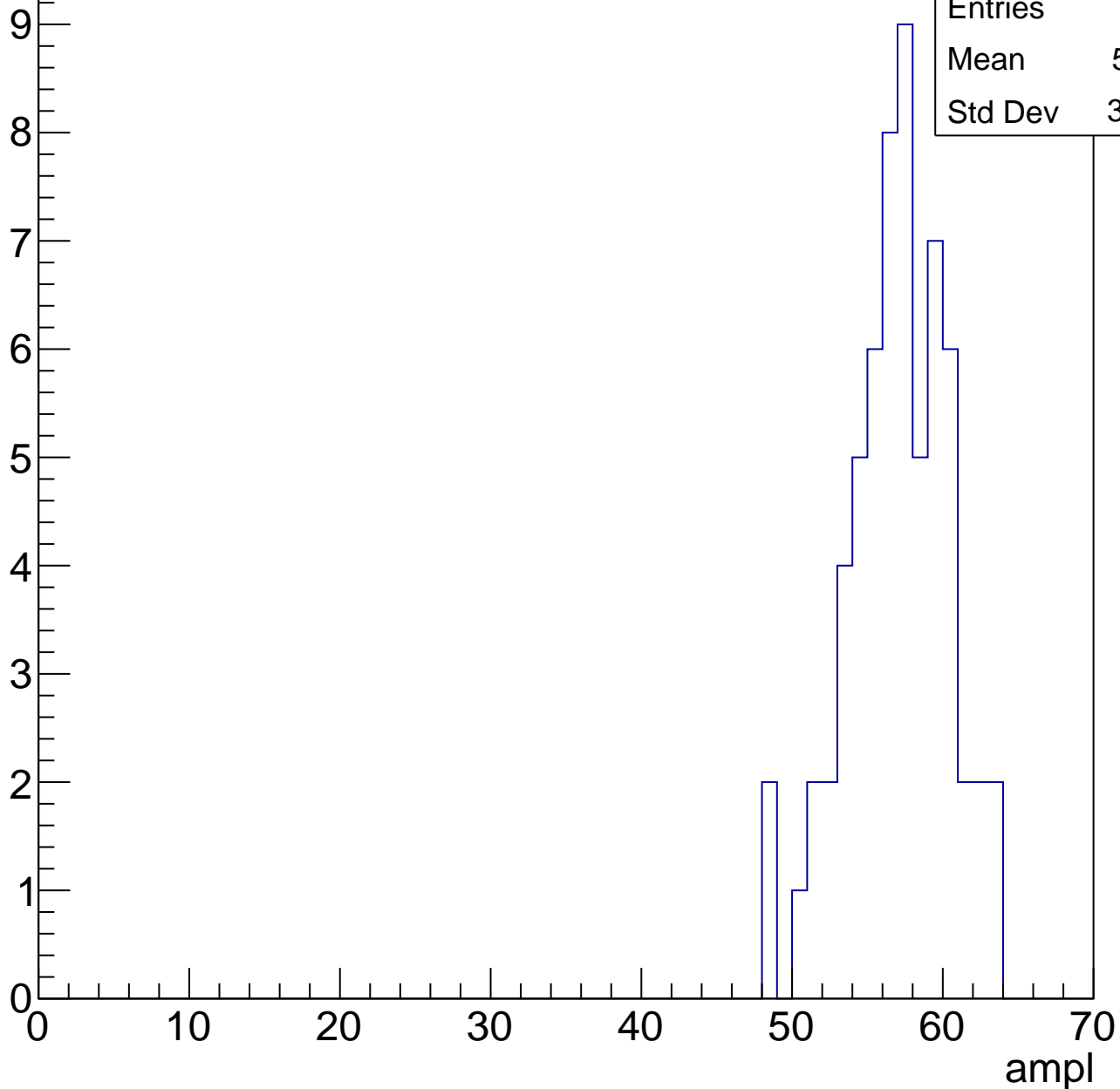
Entries	54
Mean	51.35
Std Dev	2.901



# B0L002S, U2-ch84, adc4

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



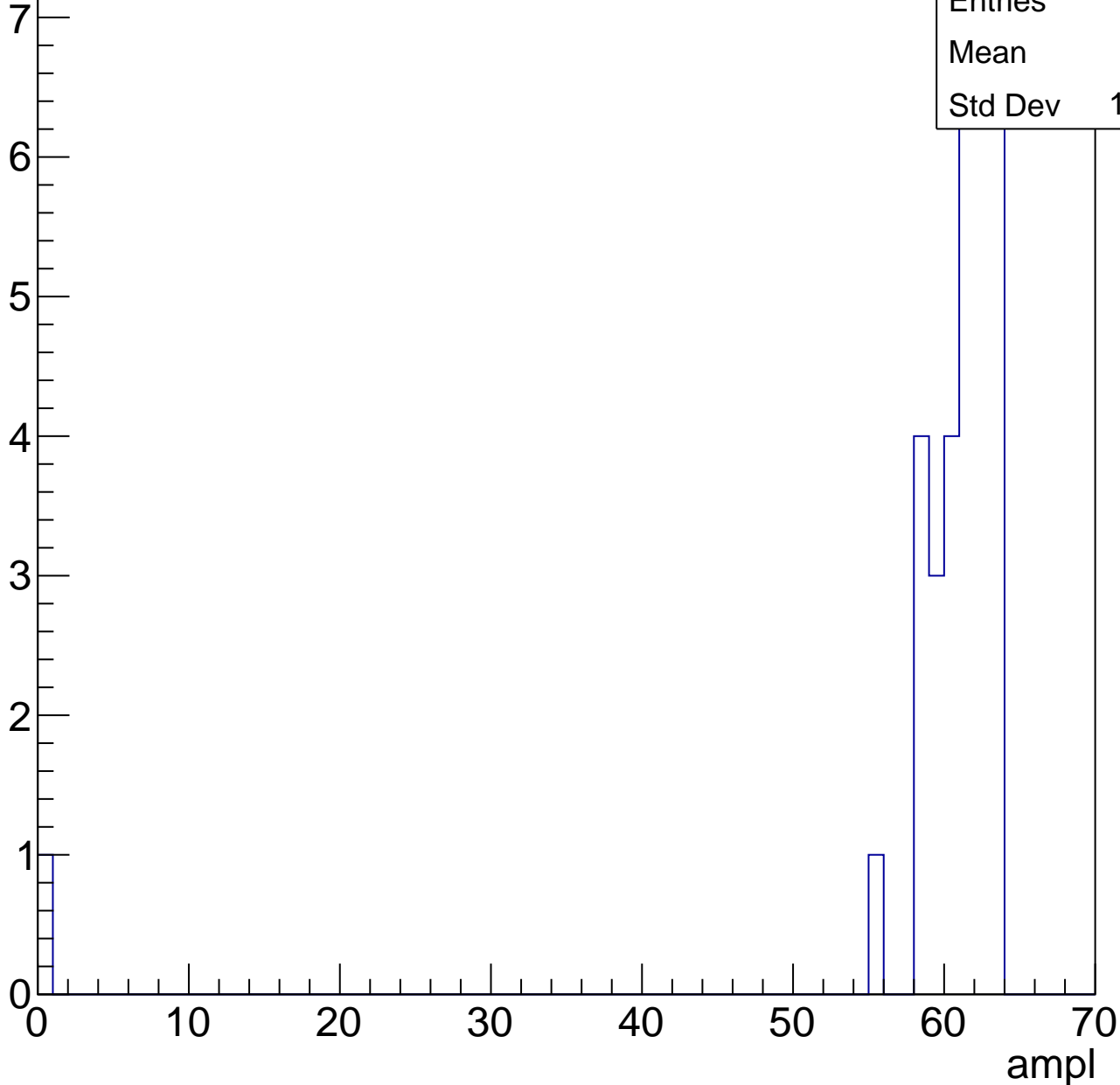
Entries	63
Mean	56.51
Std Dev	3.333

# B0L002S, U2-ch84, adc5

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	34
Mean	59
Std Dev	10.44



# B0L002S, U2-ch84, adc6

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry





# B0L002S, U2-ch84, adc7

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L002S, U2-ch85, adc0

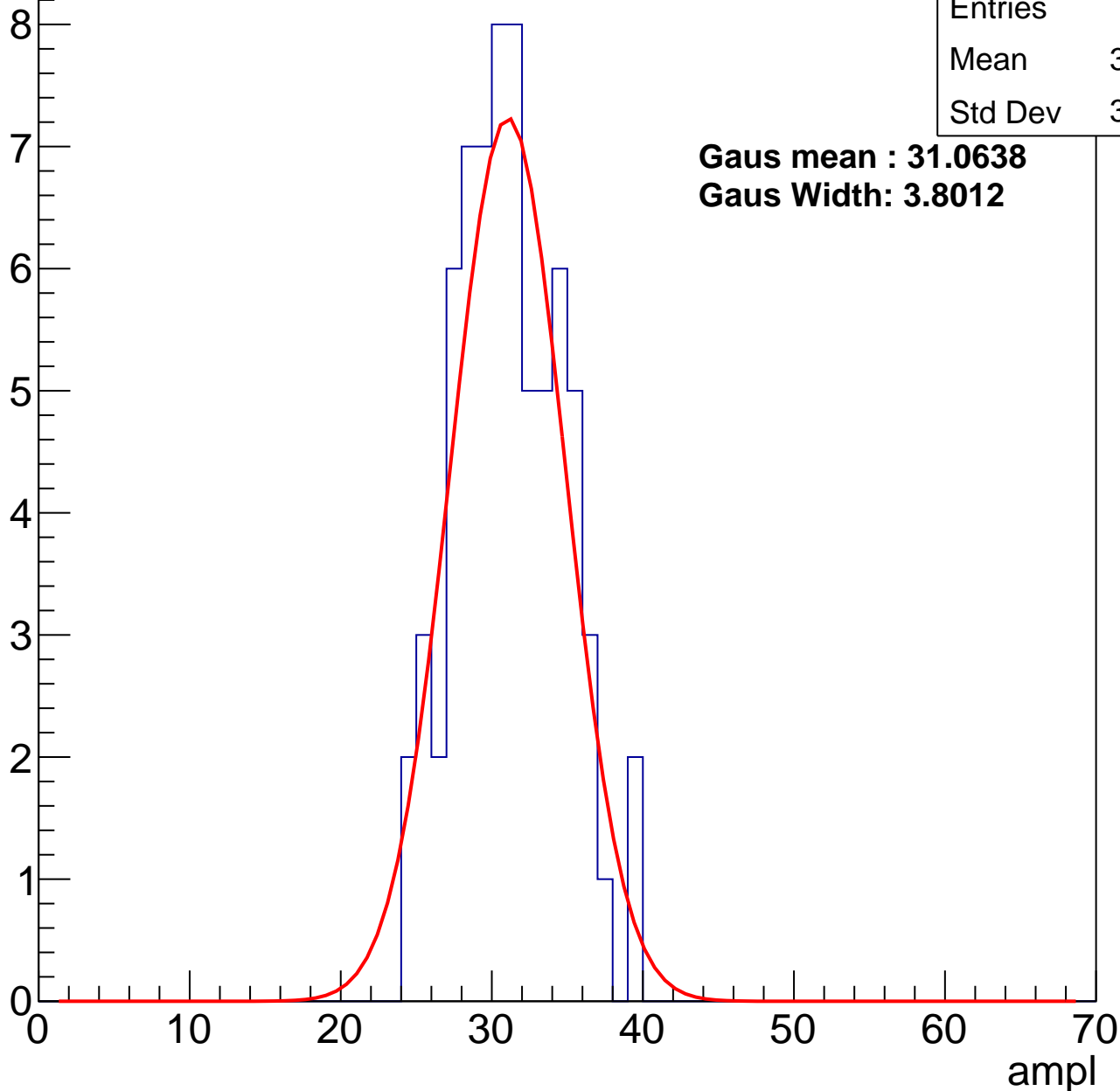
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	70
Mean	30.73
Std Dev	3.472

**Gaus mean : 31.0638**

**Gaus Width: 3.8012**



# B0L002S, U2-ch85, adc1

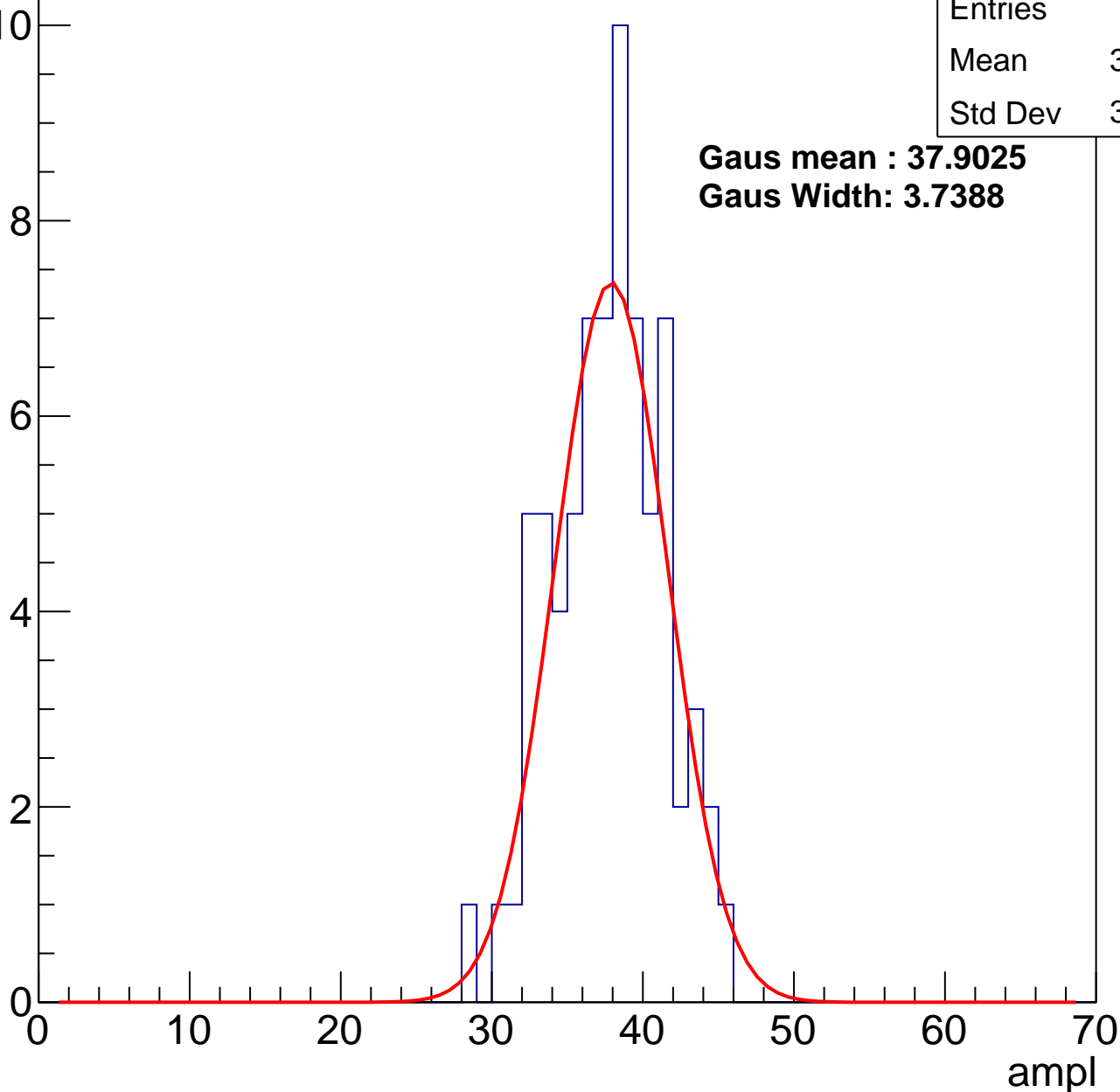
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	73
Mean	37.29
Std Dev	3.594

**Gaus mean : 37.9025**

**Gaus Width: 3.7388**



# B0L002S, U2-ch85, adc2

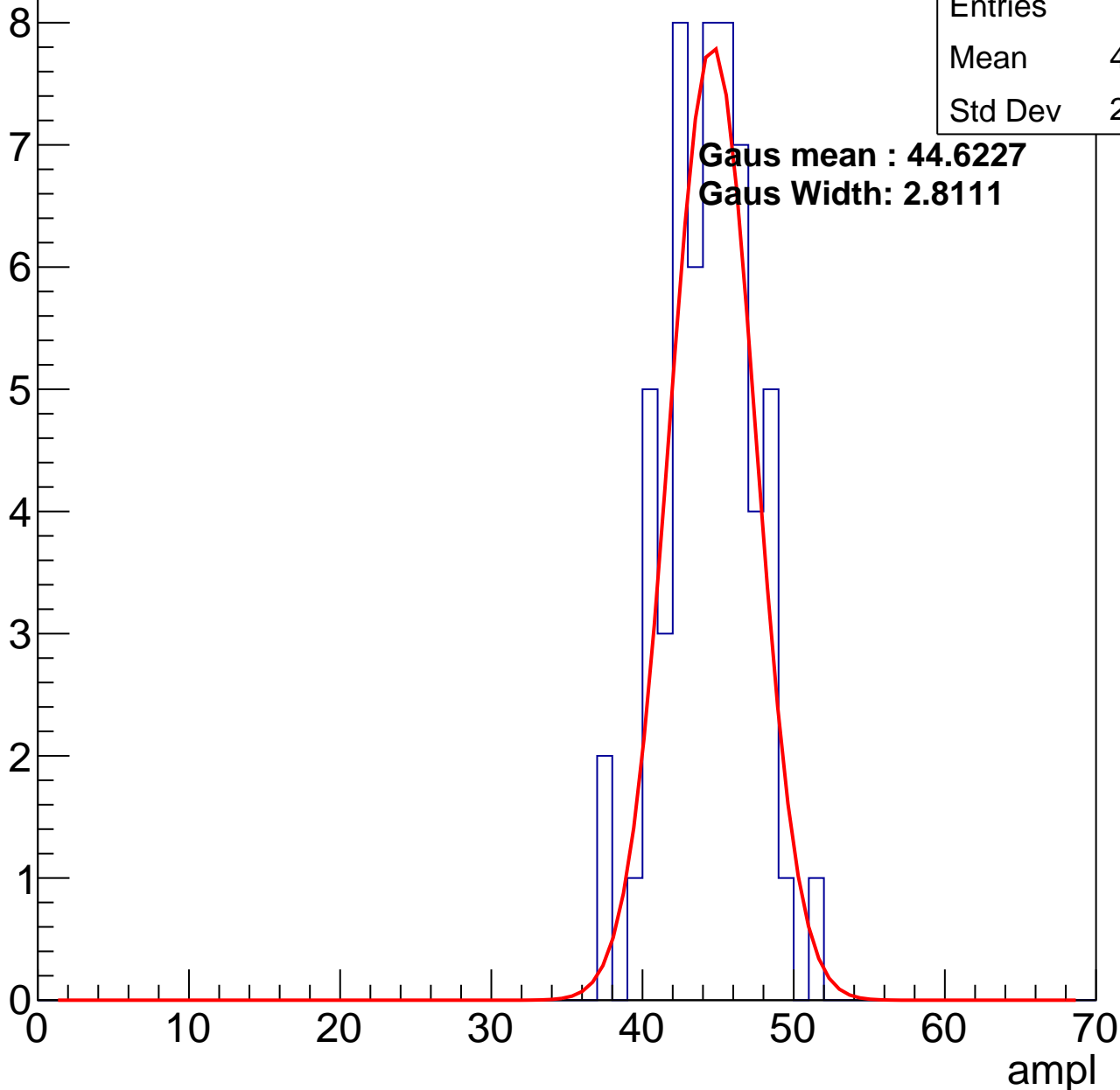
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	59
Mean	43.93
Std Dev	2.893

**Gaus mean : 44.6227**

**Gaus Width: 2.8111**



# B0L002S, U2-ch85, adc3

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entries	71
Mean	50.76
Std Dev	3.033

Entry

10

8

6

4

2

0

0

10

20

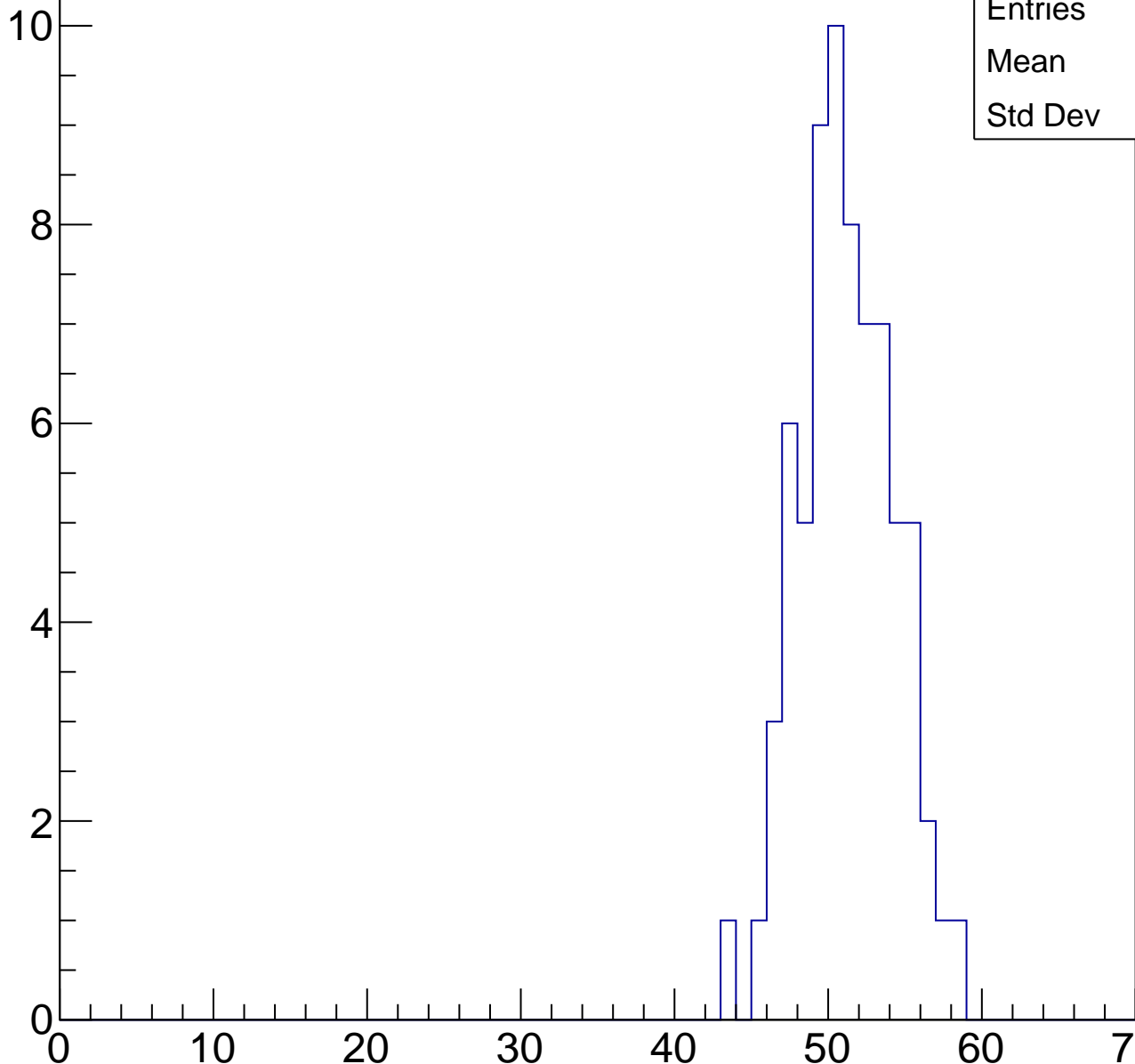
30

40

50

60

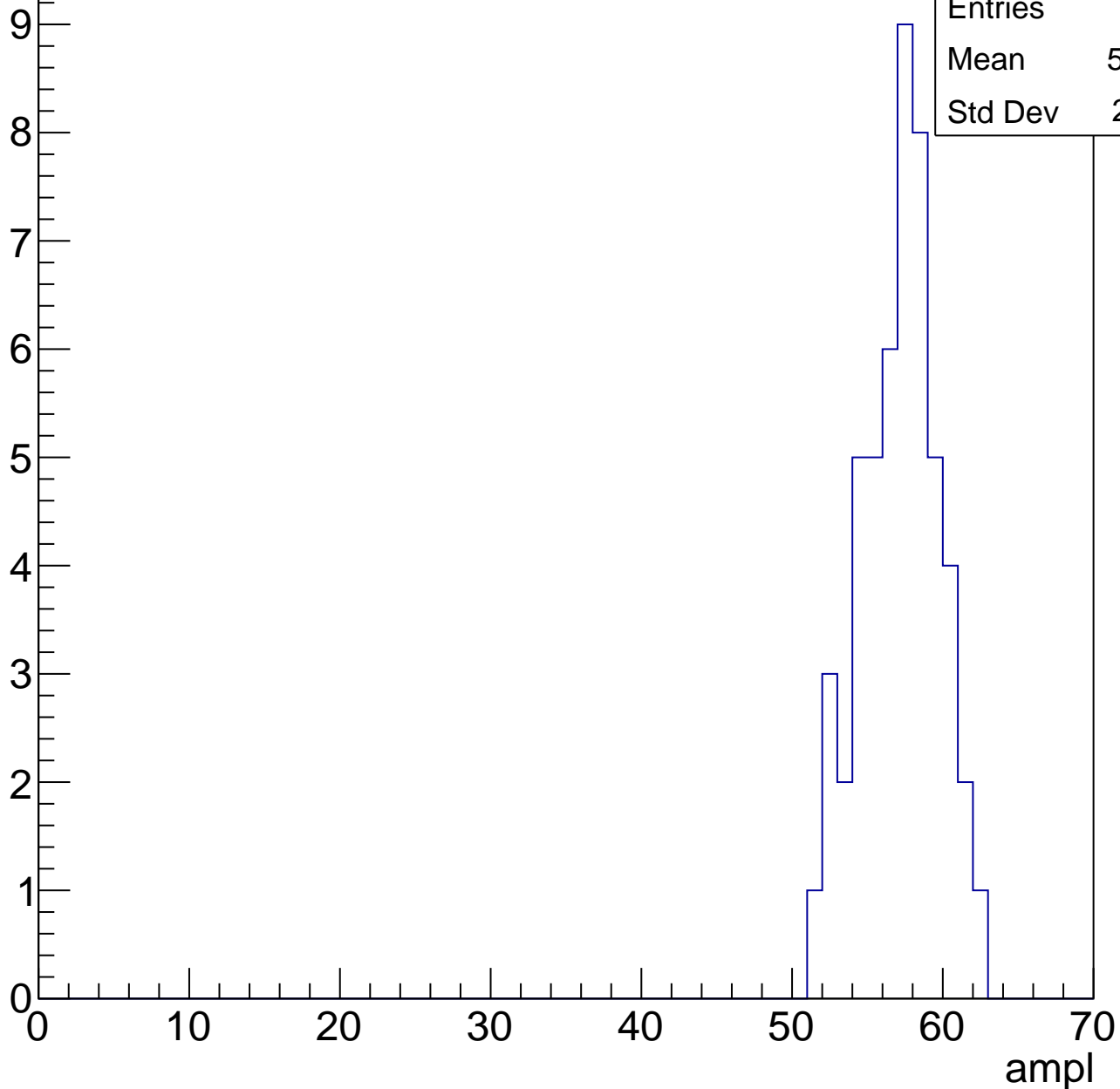
ampl



# B0L002S, U2-ch85, adc4

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



# B0L002S, U2-ch85, adc5

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	41
Mean	59.22
Std Dev	9.603

ampl

0 10 20 30 40 50 60 70

0

1

2

3

4

5

6

7

8

9

# B0L002S, U2-ch85, adc6

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry





# B0L002S, U2-ch85, adc7

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



Entries	2
Mean	11.5
Std Dev	11.5

# B0L002S, U2-ch86, adc0

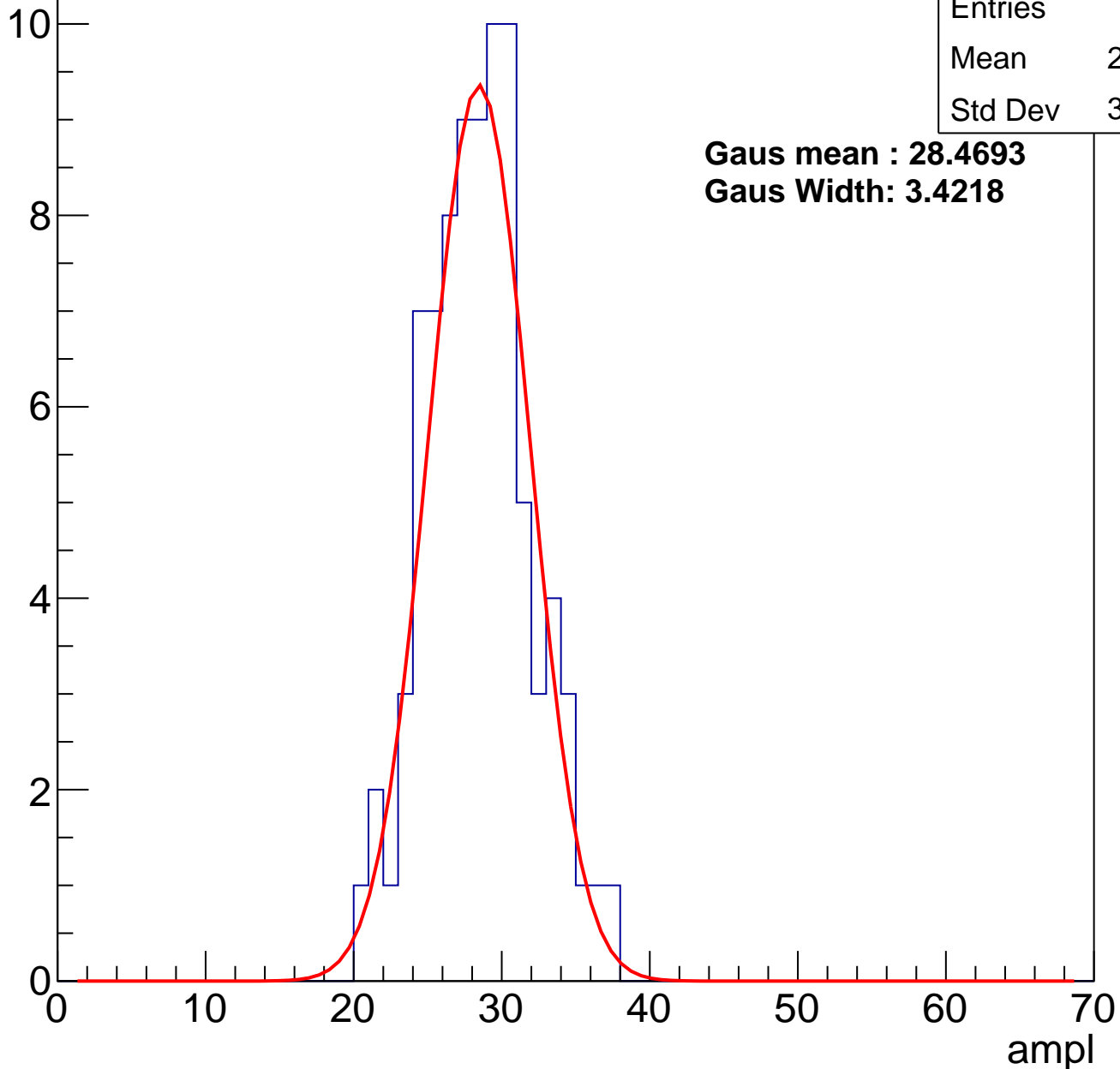
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entries	85
Mean	28.02
Std Dev	3.488

**Gaus mean : 28.4693**

**Gaus Width: 3.4218**

Entry



# B0L002S, U2-ch86, adc1

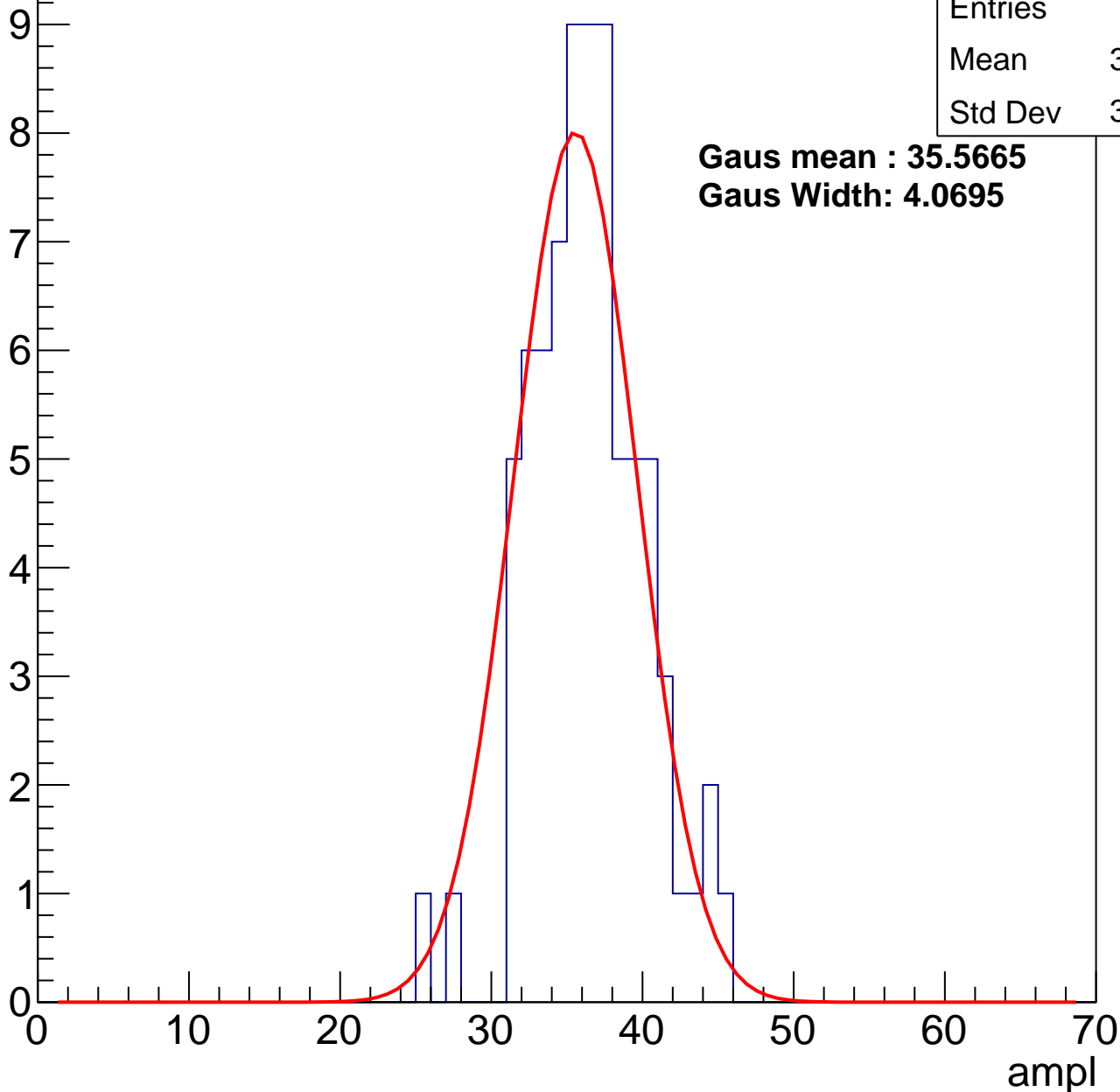
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	76
Mean	35.96
Std Dev	3.694

**Gaus mean : 35.5665**

**Gaus Width: 4.0695**



# B0L002S, U2-ch86, adc2

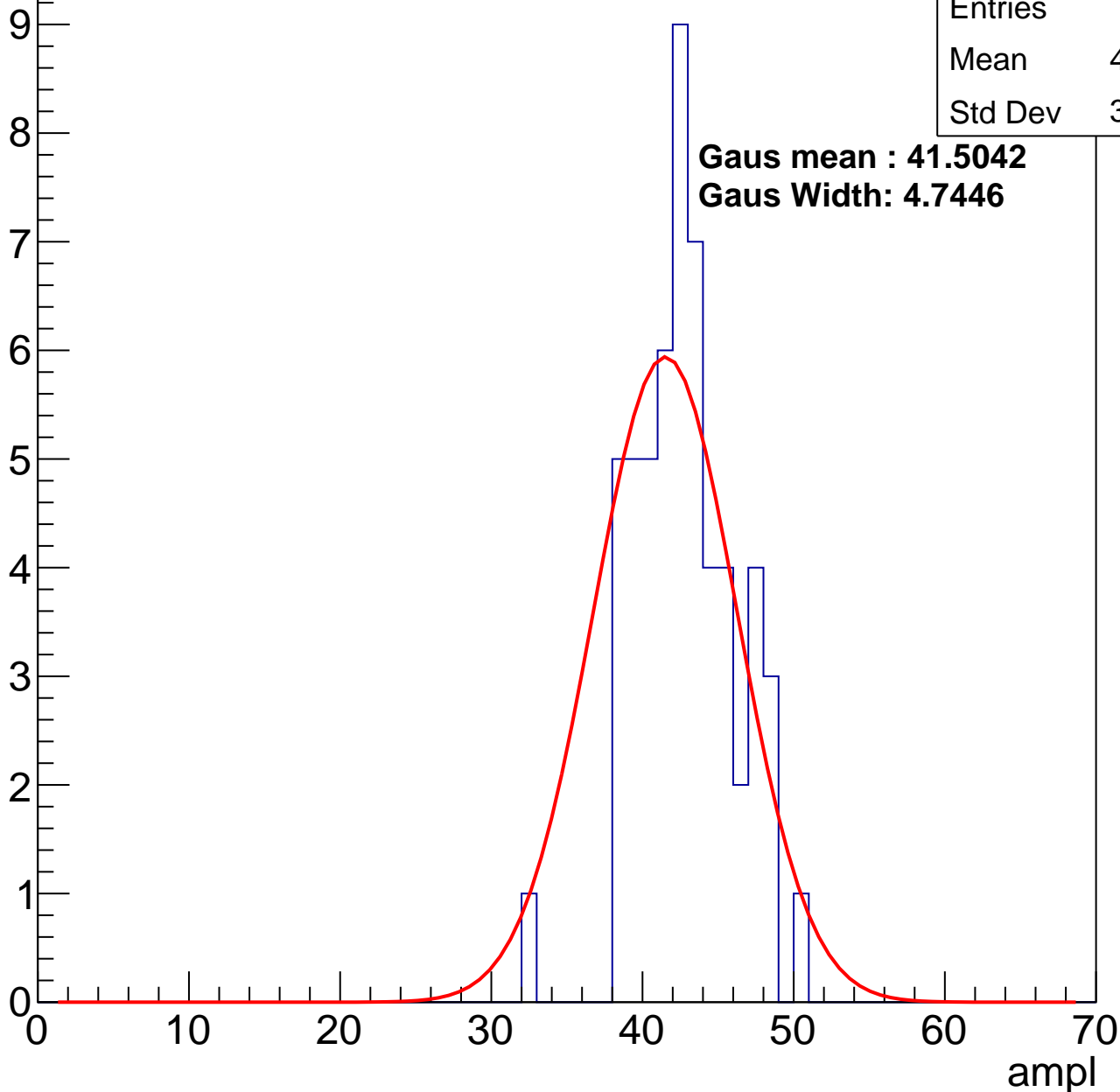
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	56
Mean	42.36
Std Dev	3.292

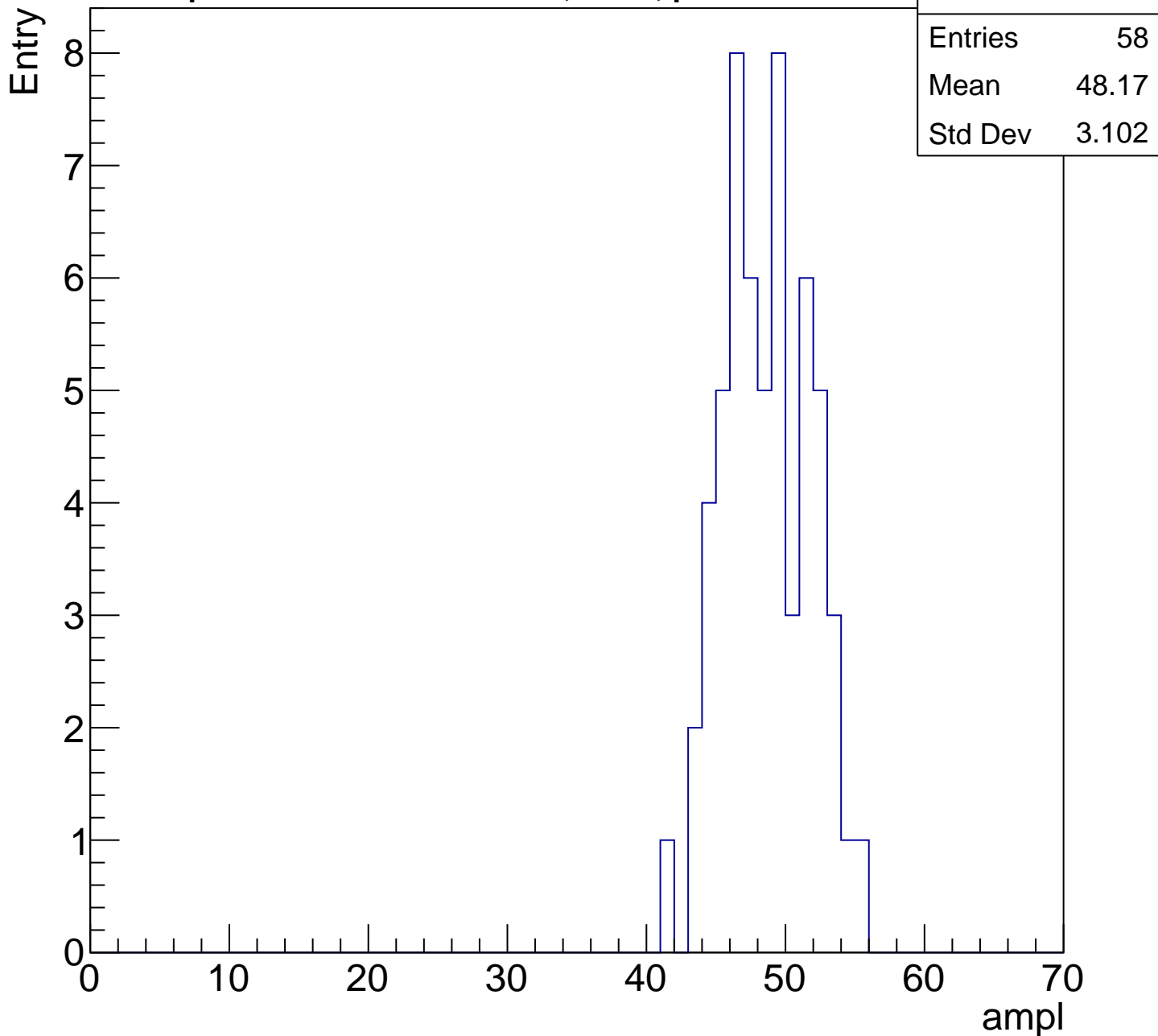
**Gaus mean : 41.5042**

**Gaus Width: 4.7446**



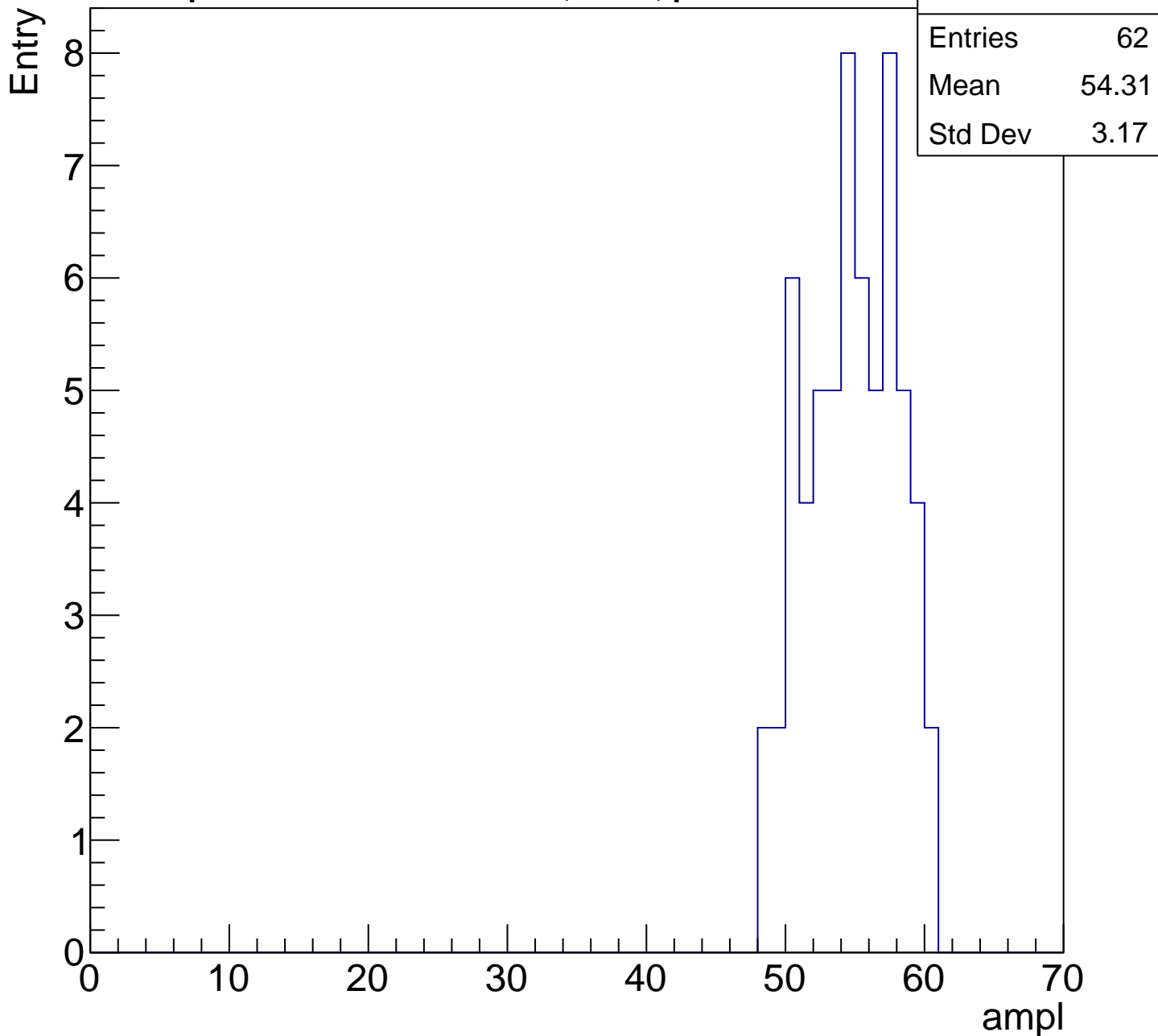
# B0L002S, U2-ch86, adc3

calib\_packv5\_042523\_0143.root, FC#8, port C1



# B0L002S, U2-ch86, adc4

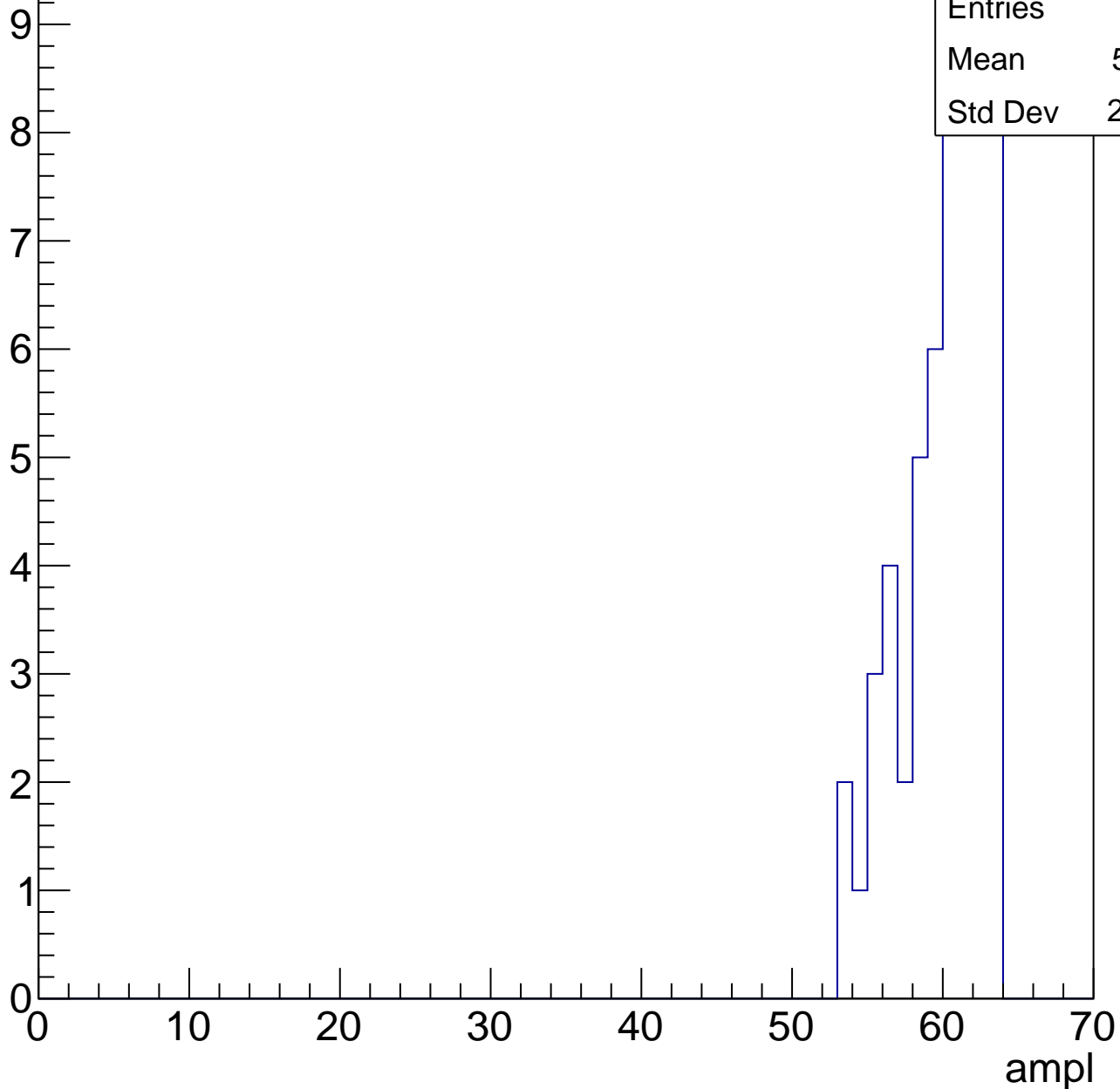
calib\_packv5\_042523\_0143.root, FC#8, port C1



# B0L002S, U2-ch86, adc5

calib\_packv5\_042523\_0143.root, FC#8, port C1

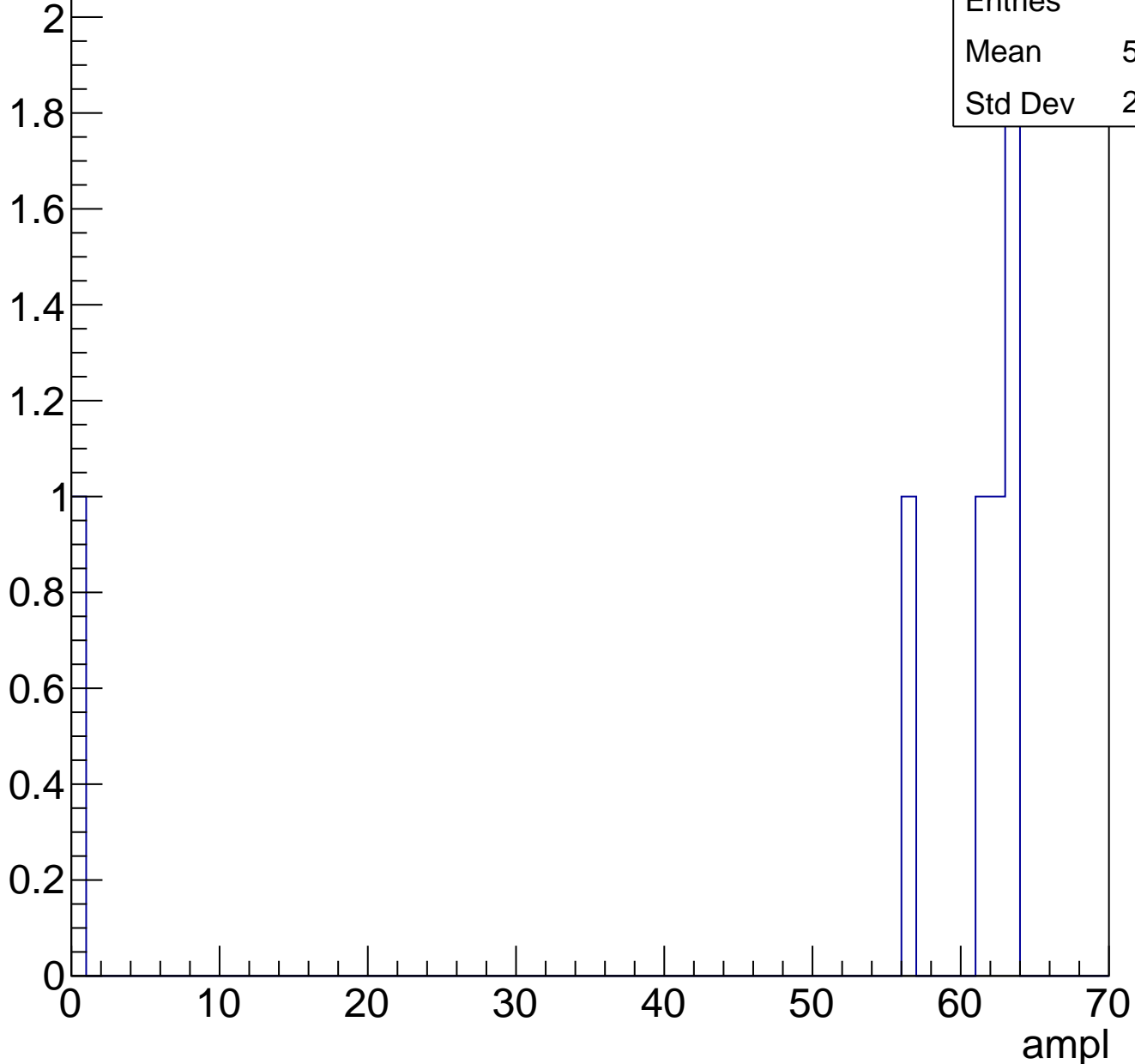
Entry



# B0L002S, U2-ch86, adc6

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry





# B0L002S, U2-ch86, adc7

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L002S, U2-ch87, adc0

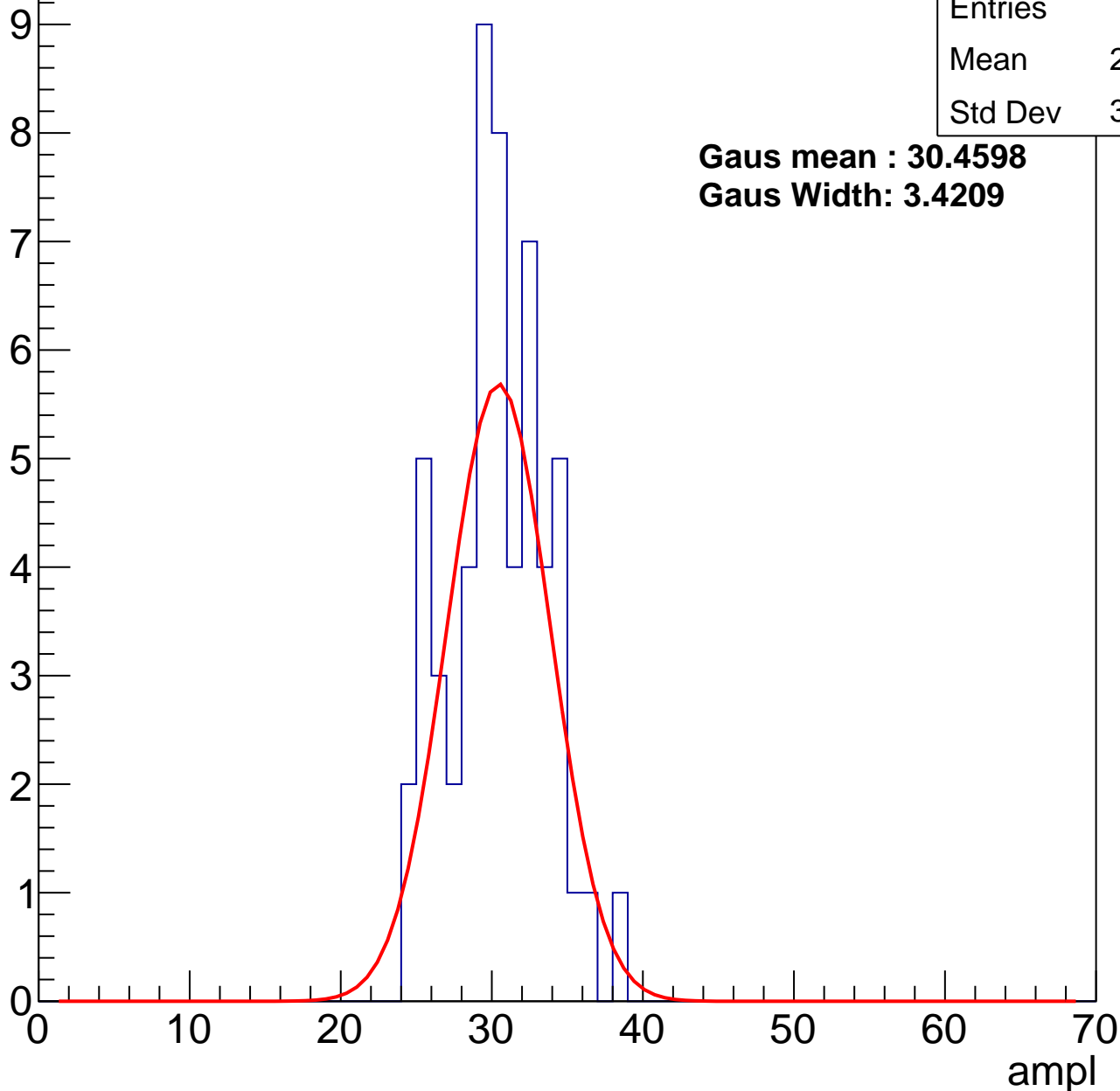
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	56
Mean	29.95
Std Dev	3.165

**Gaus mean : 30.4598**

**Gaus Width: 3.4209**



# B0L002S, U2-ch87, adc1

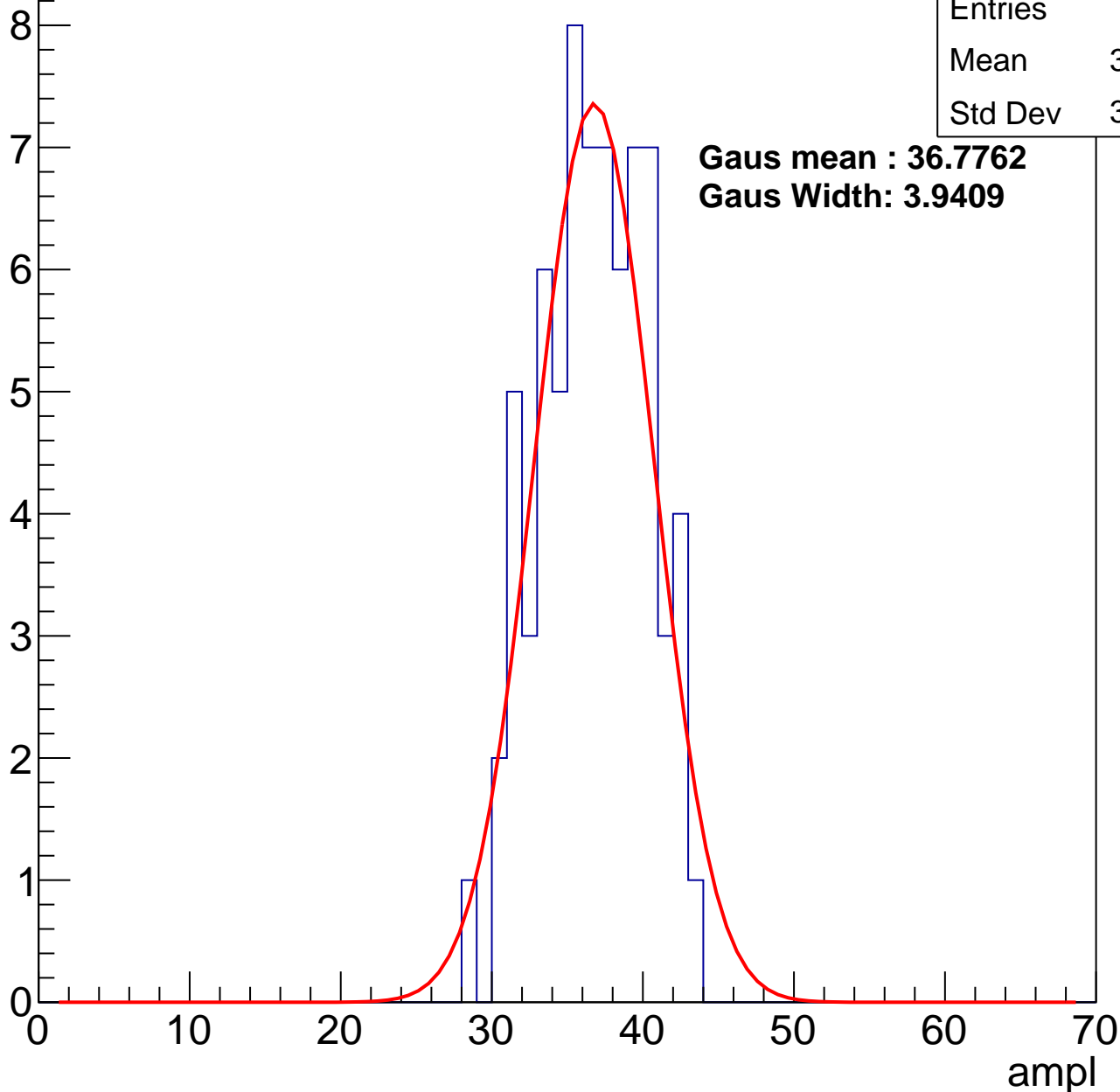
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	72
Mean	36.29
Std Dev	3.454

**Gaus mean : 36.7762**

**Gaus Width: 3.9409**



# B0L002S, U2-ch87, adc2

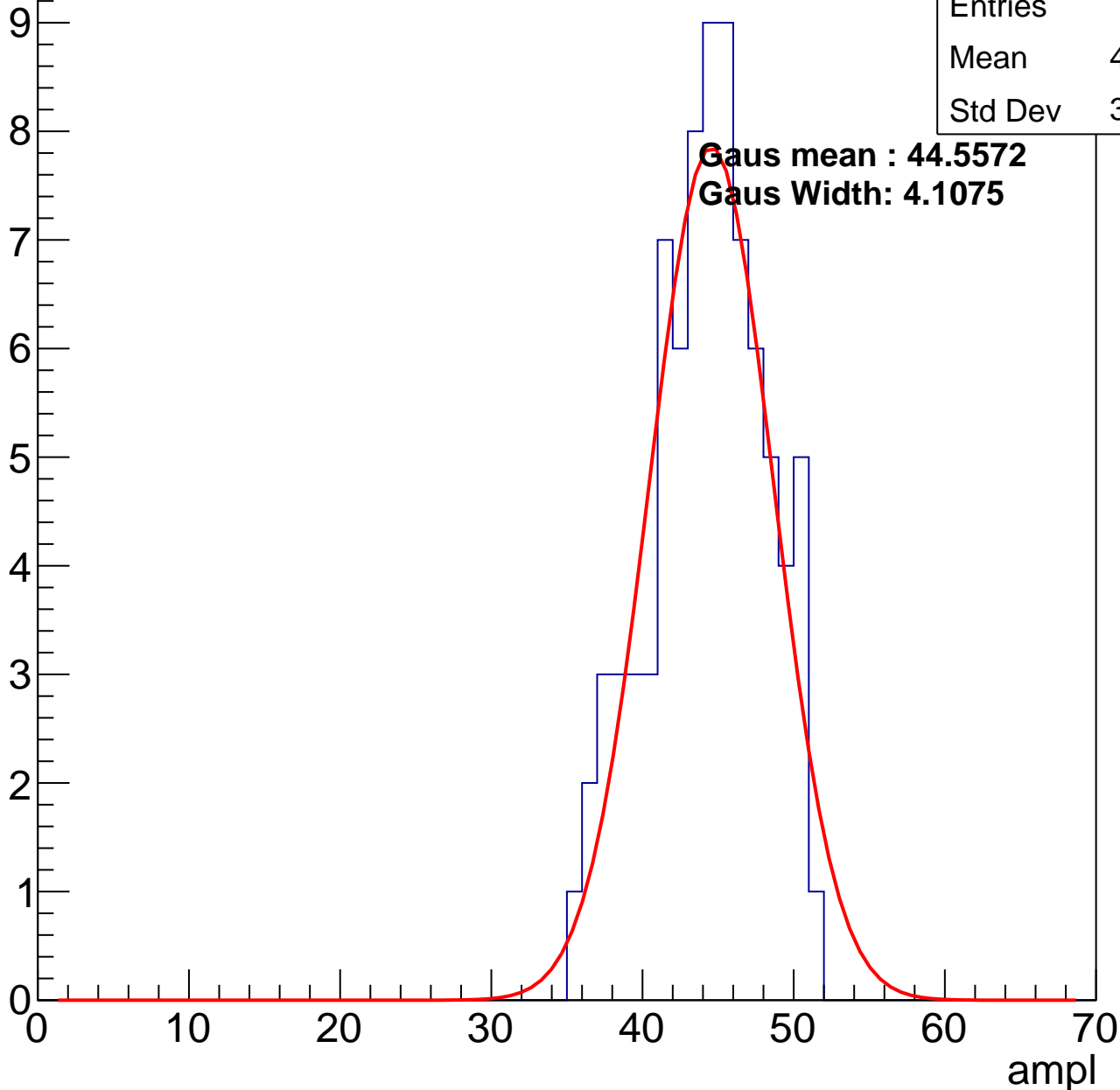
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	82
Mean	43.83
Std Dev	3.793

Gaus mean : 44.5572

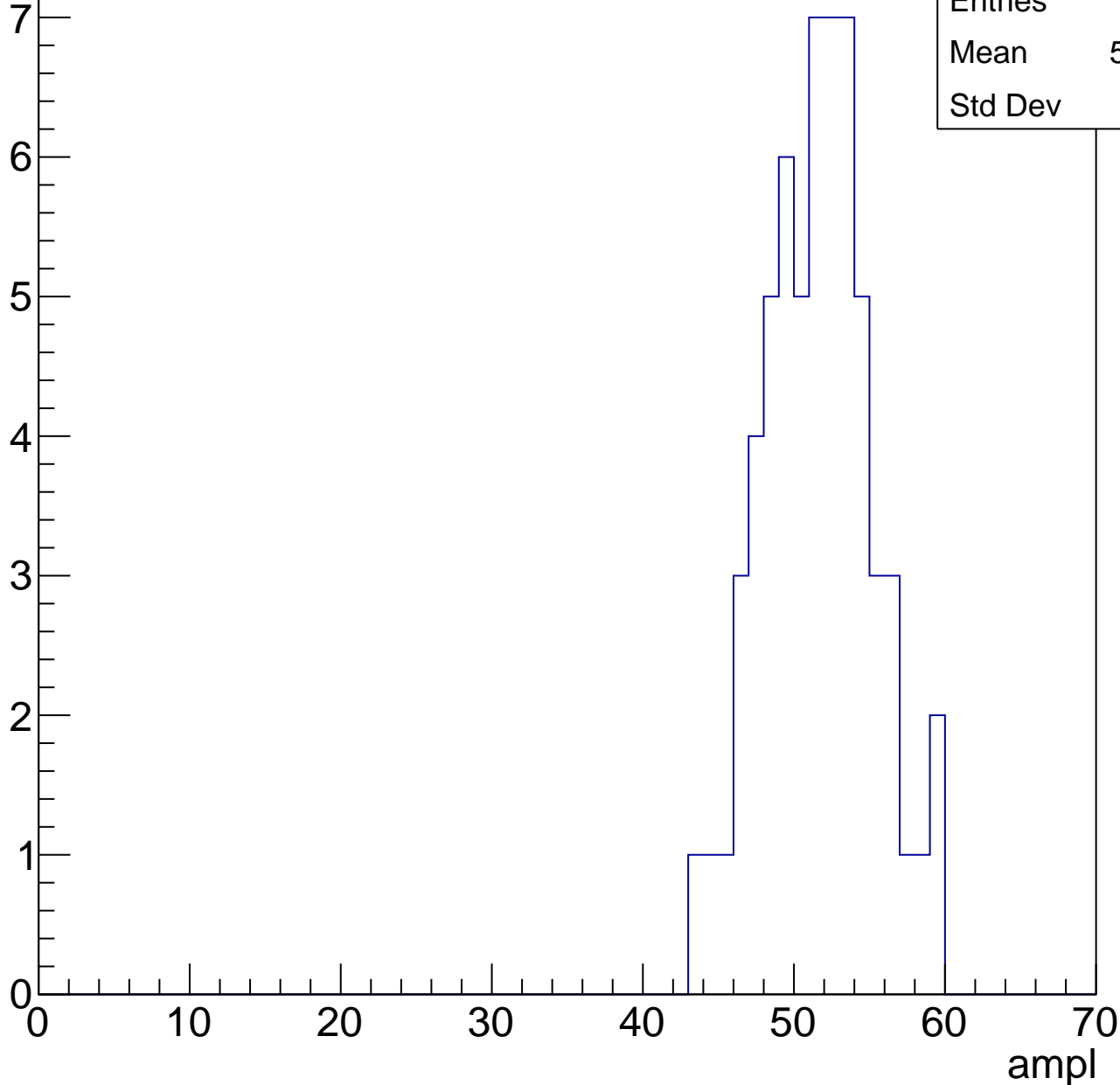
Gaus Width: 4.1075



# B0L002S, U2-ch87, adc3

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

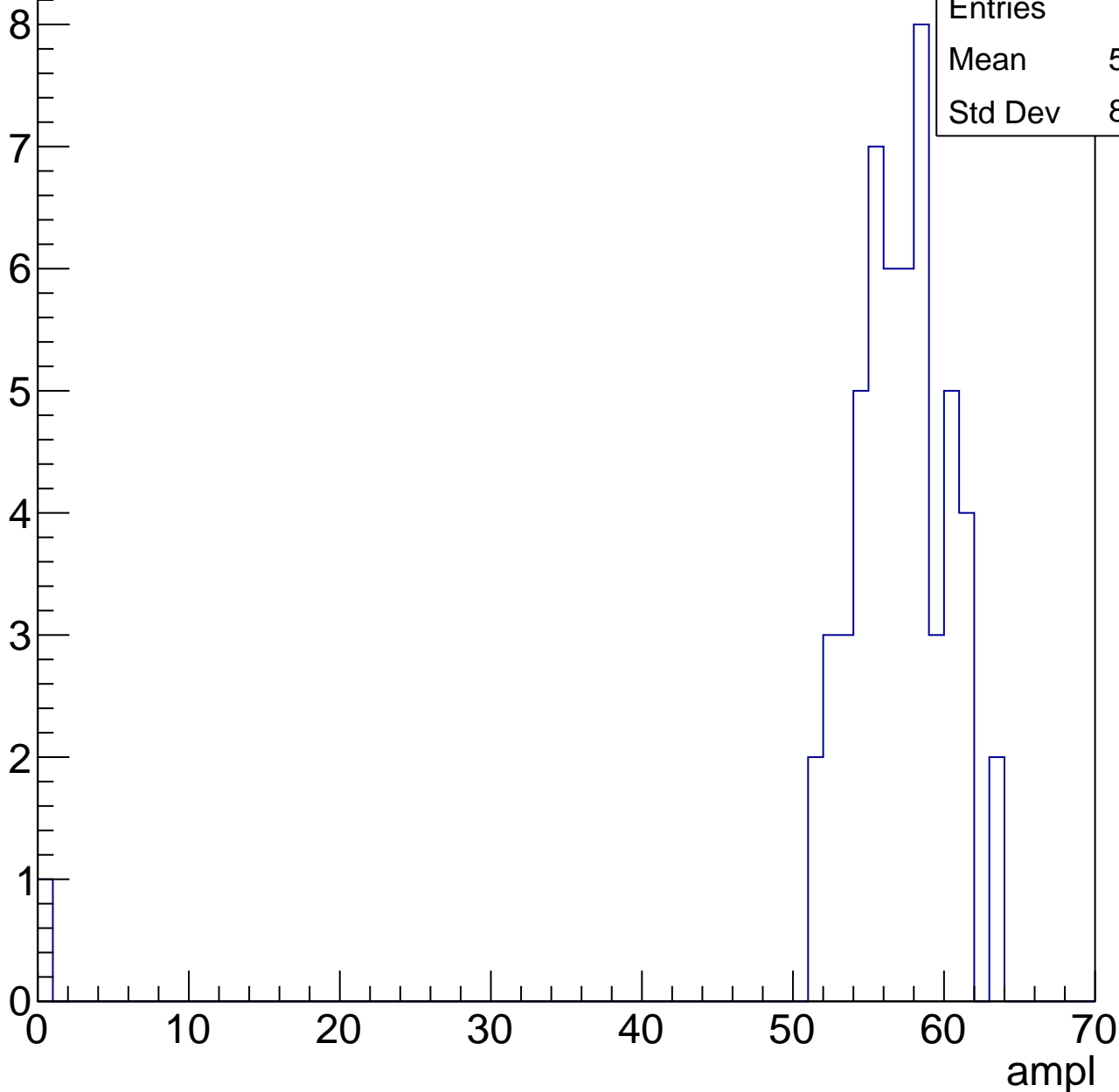


# B0L002S, U2-ch87, adc4

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	55
Mean	55.65
Std Dev	8.118

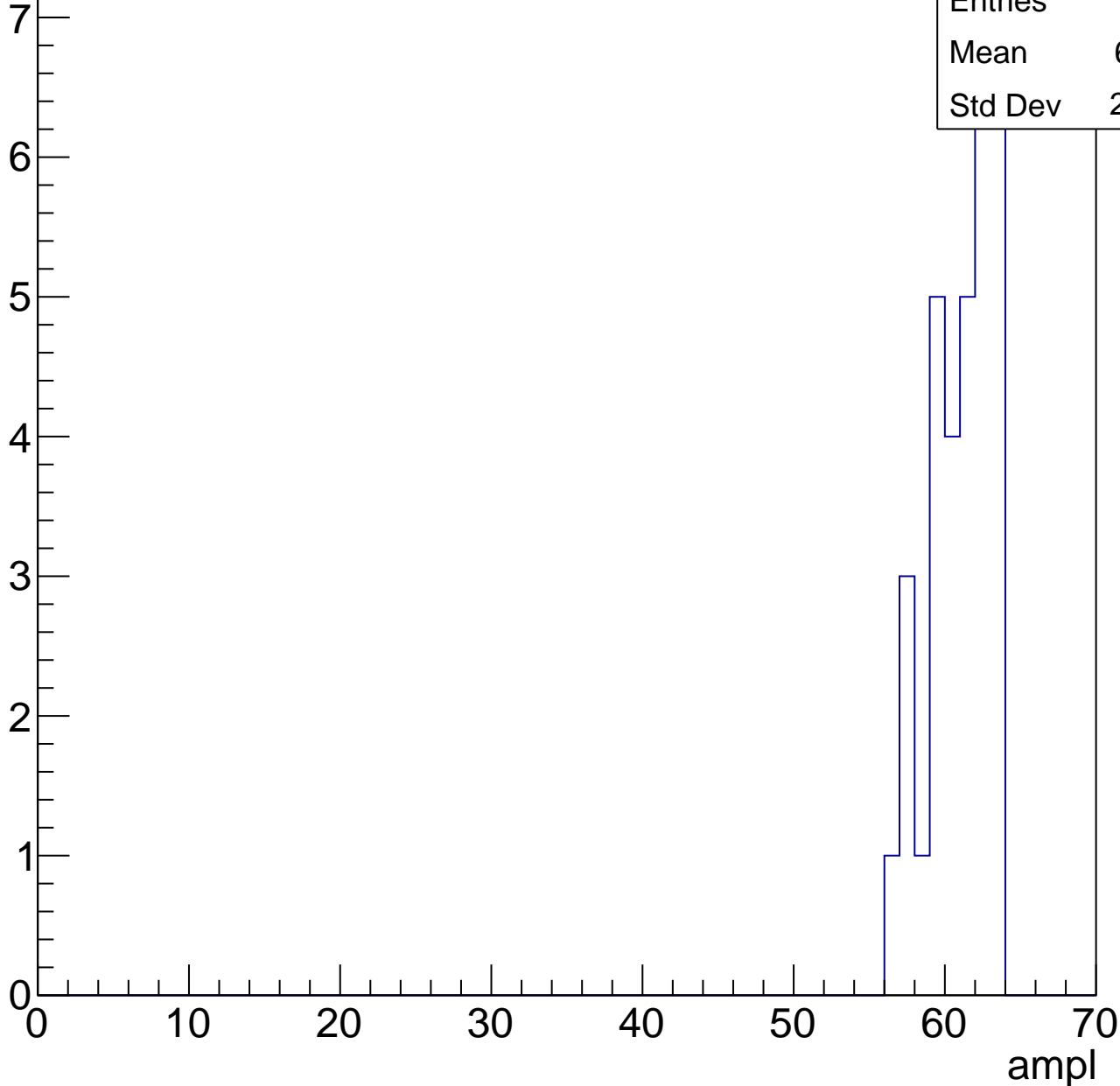


# B0L002S, U2-ch87, adc5

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

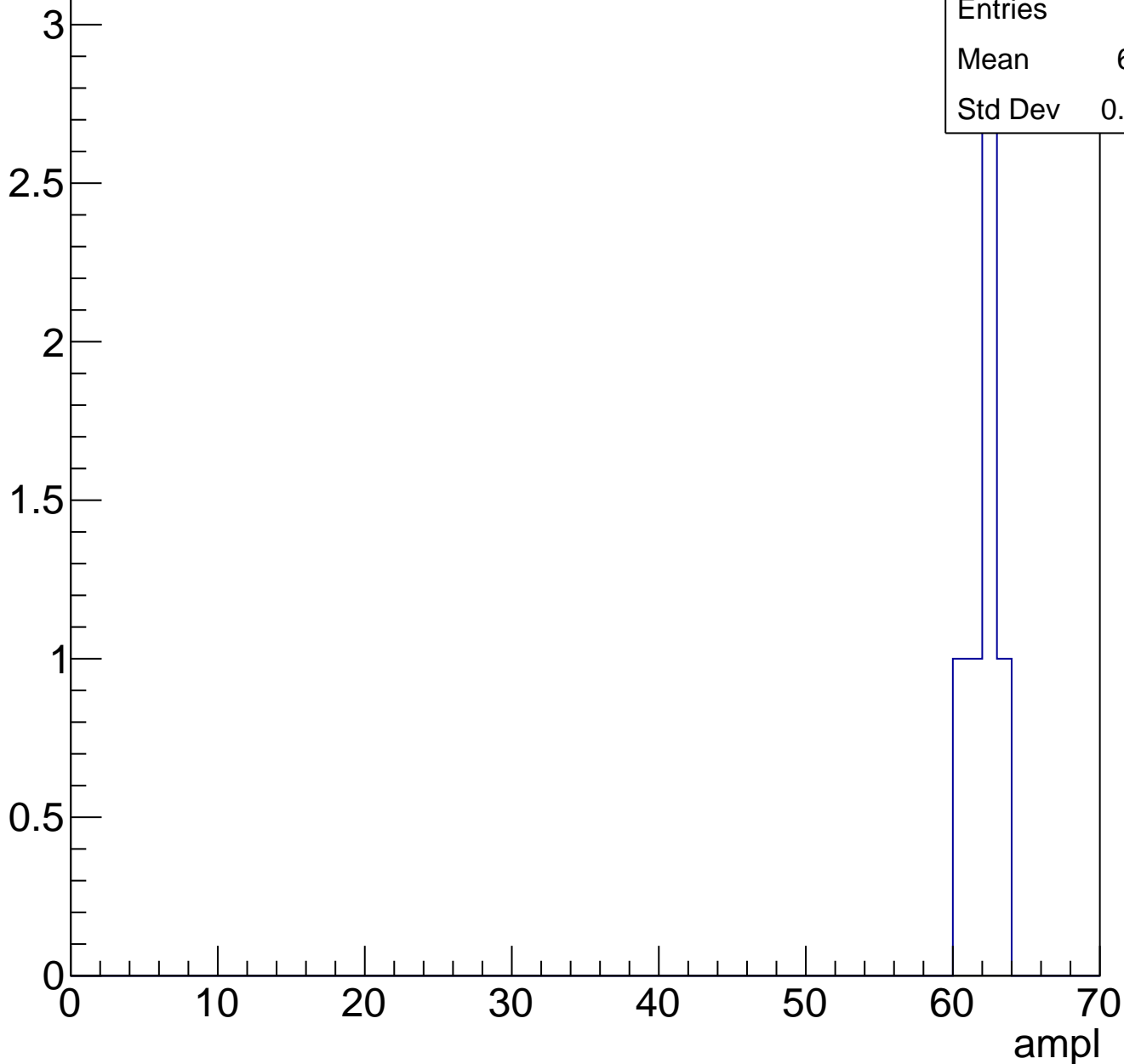
Entries	33
Mean	60.61
Std Dev	2.029



# B0L002S, U2-ch87, adc6

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry





# B0L002S, U2-ch87, adc7

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



# B0L002S, U2-ch88, adc0

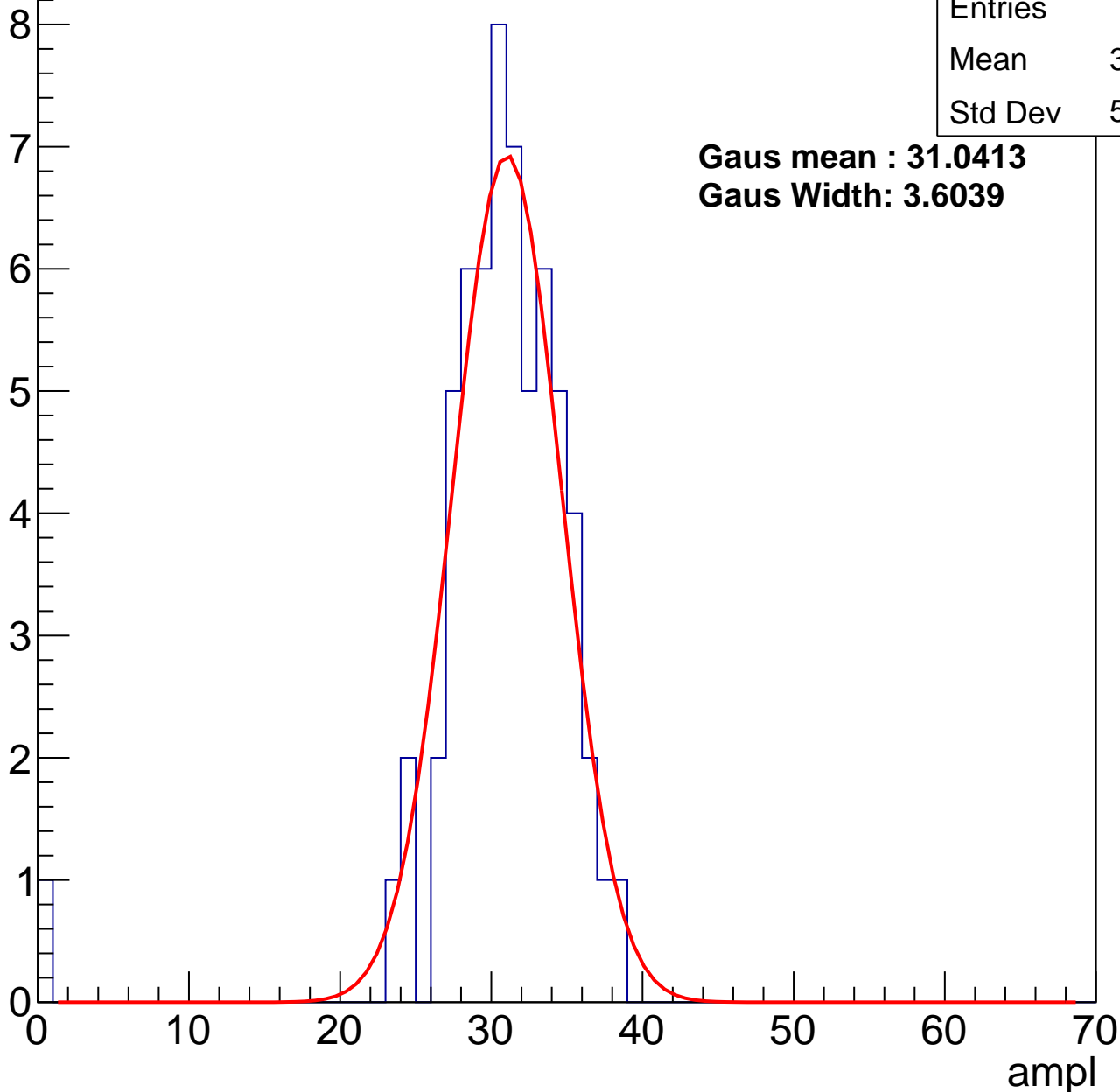
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	62
Mean	30.19
Std Dev	5.035

**Gaus mean : 31.0413**

**Gaus Width: 3.6039**



# B0L002S, U2-ch88, adc1

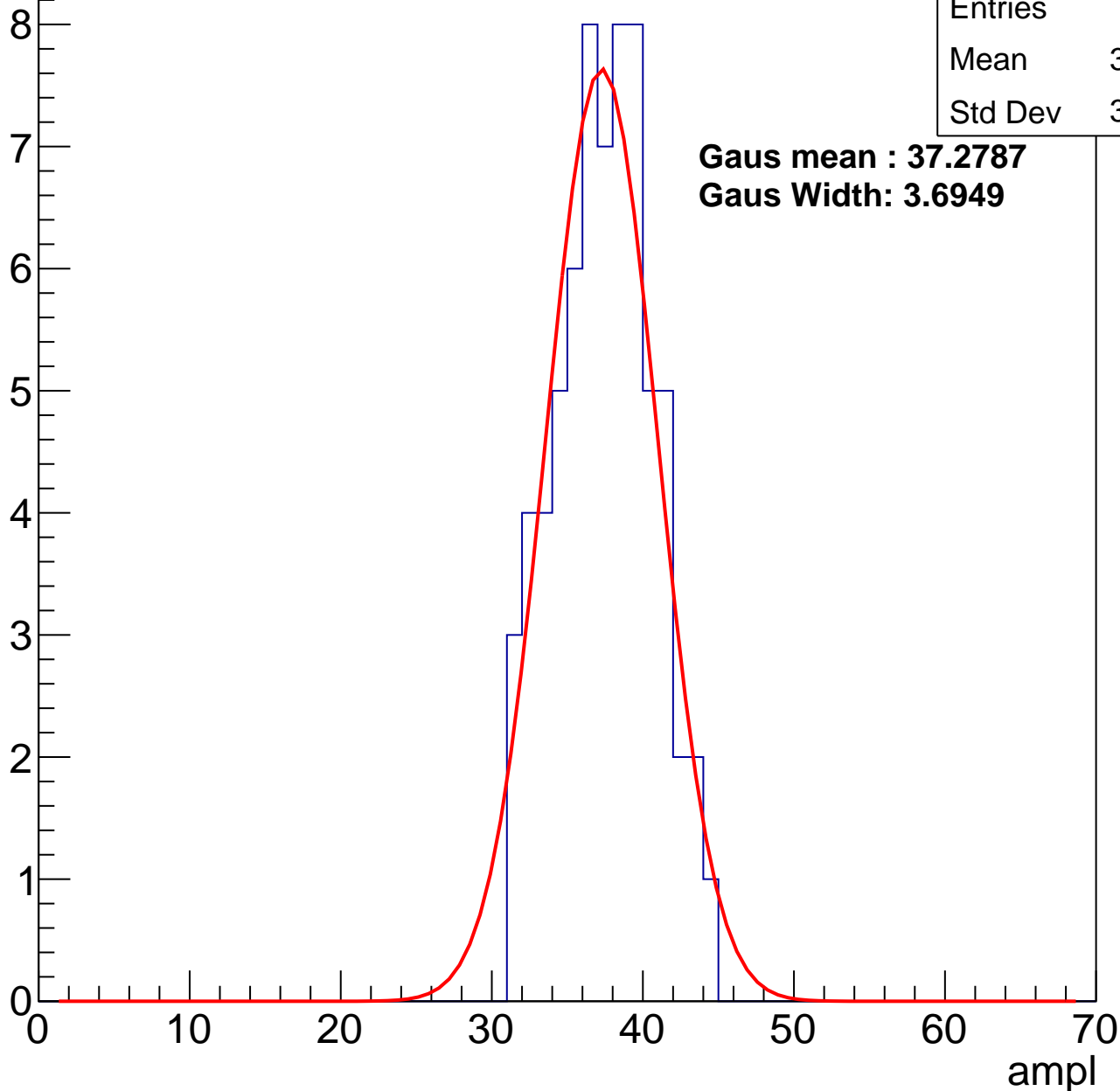
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	68
Mean	36.99
Std Dev	3.174

**Gaus mean : 37.2787**

**Gaus Width: 3.6949**



# B0L002S, U2-ch88, adc2

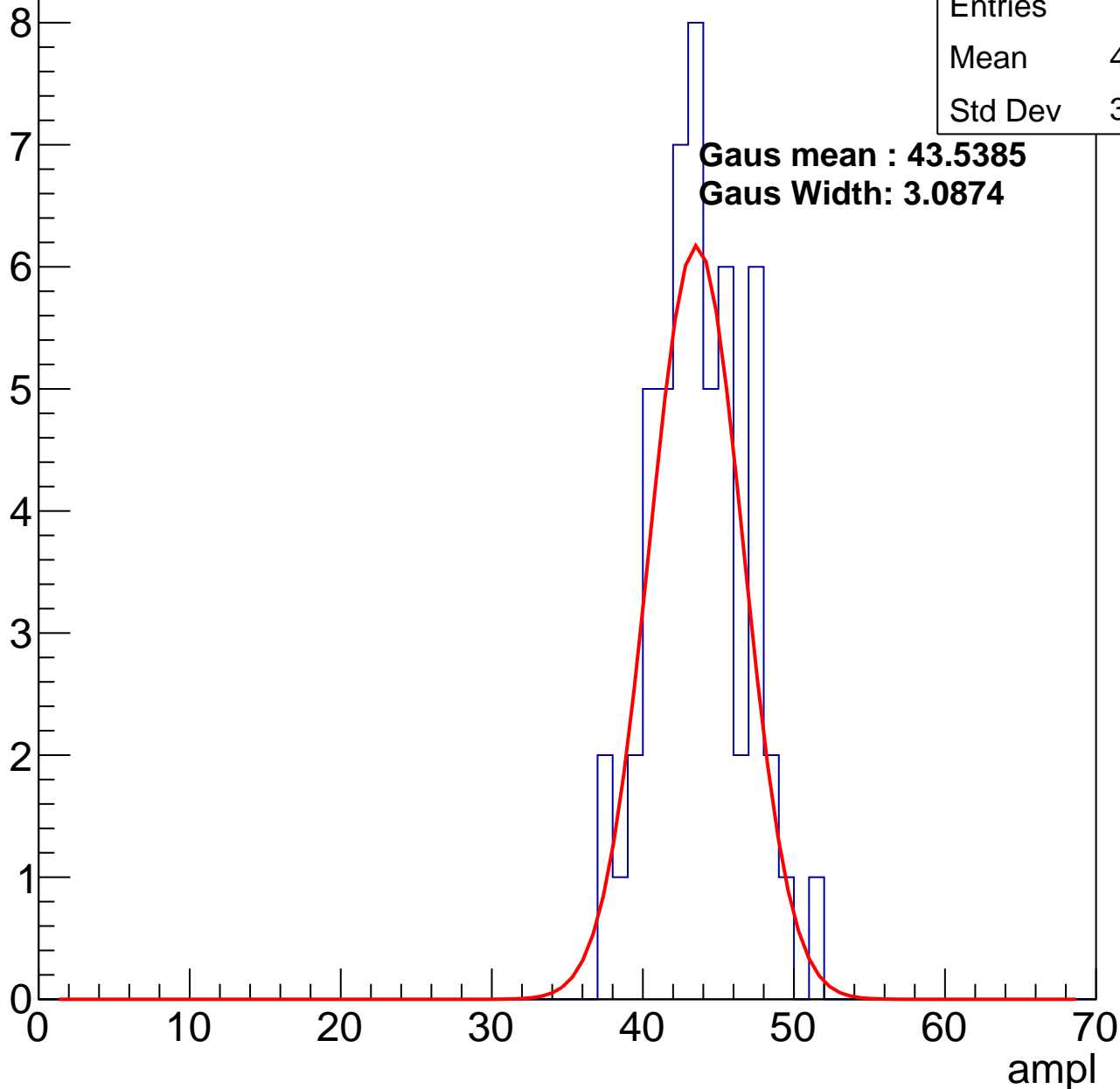
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	53
Mean	43.26
Std Dev	3.042

**Gaus mean : 43.5385**

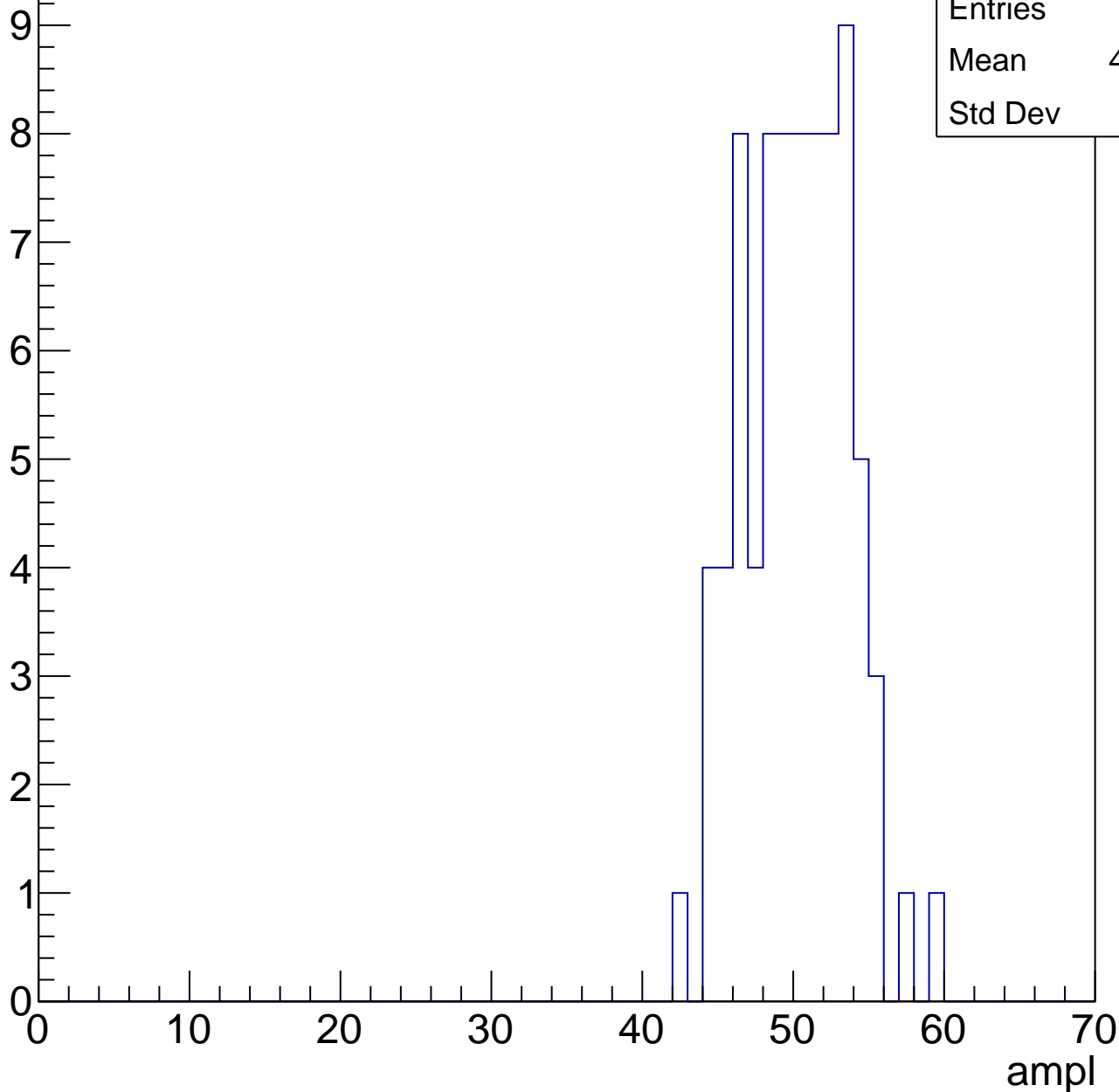
**Gaus Width: 3.0874**



# B0L002S, U2-ch88, adc3

calib\_packv5\_042523\_0143.root, FC#8, port C1

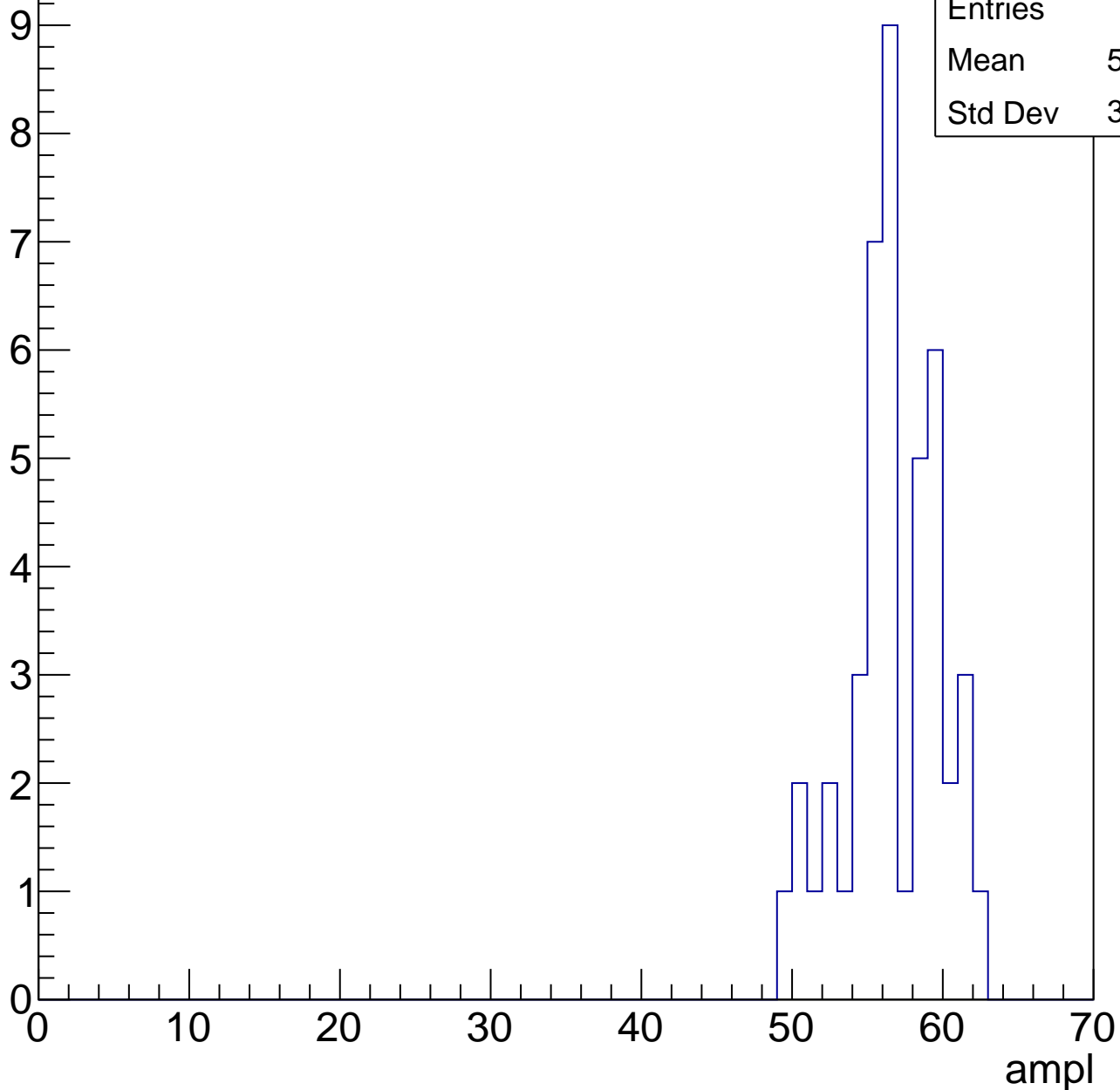
Entry



# B0L002S, U2-ch88, adc4

calib\_packv5\_042523\_0143.root, FC#8, port C1

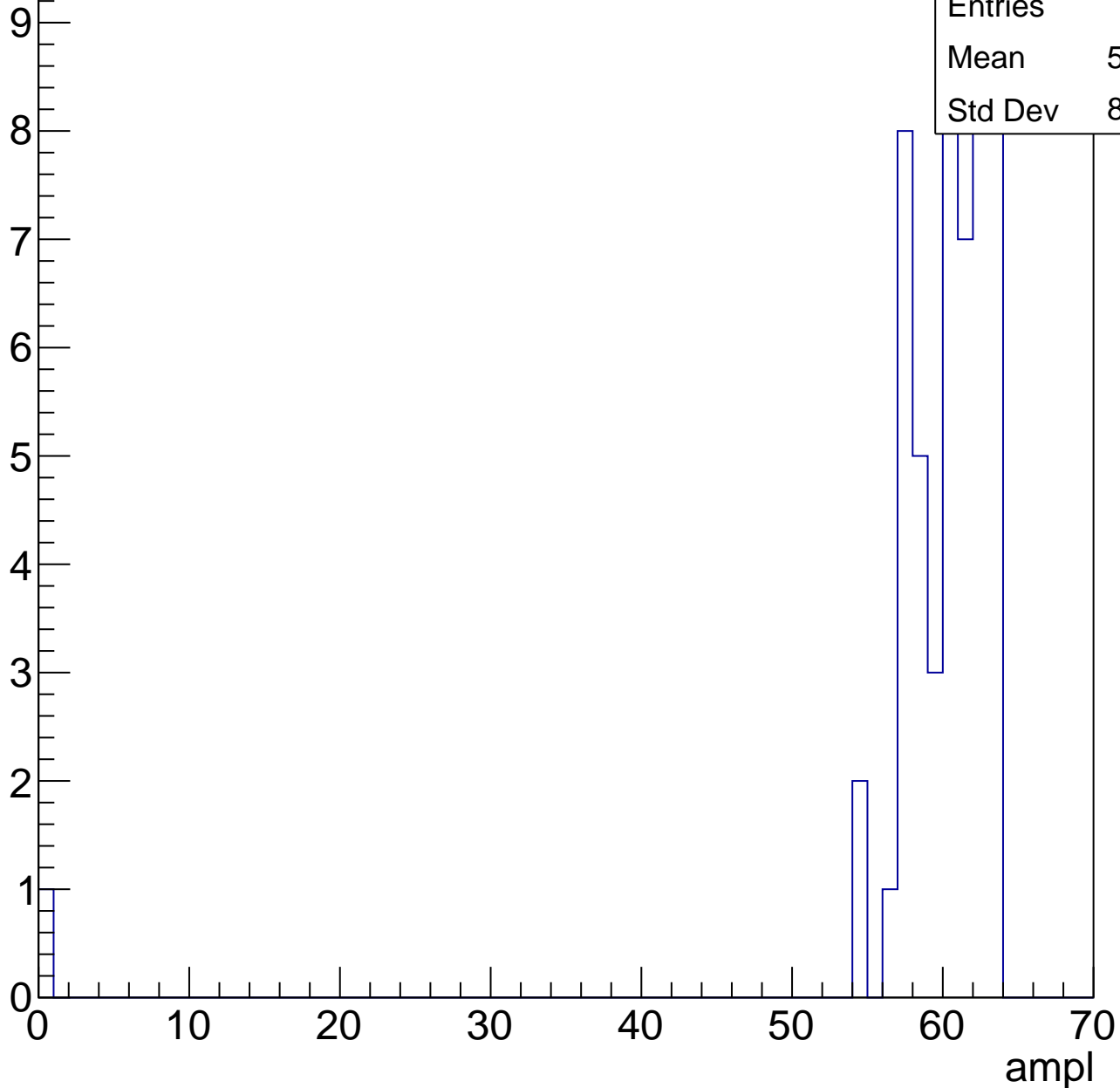
Entry



# B0L002S, U2-ch88, adc5

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



# B0L002S, U2-ch88, adc6

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry





# B0L002S, U2-ch88, adc7

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L002S, U2-ch89, adc0

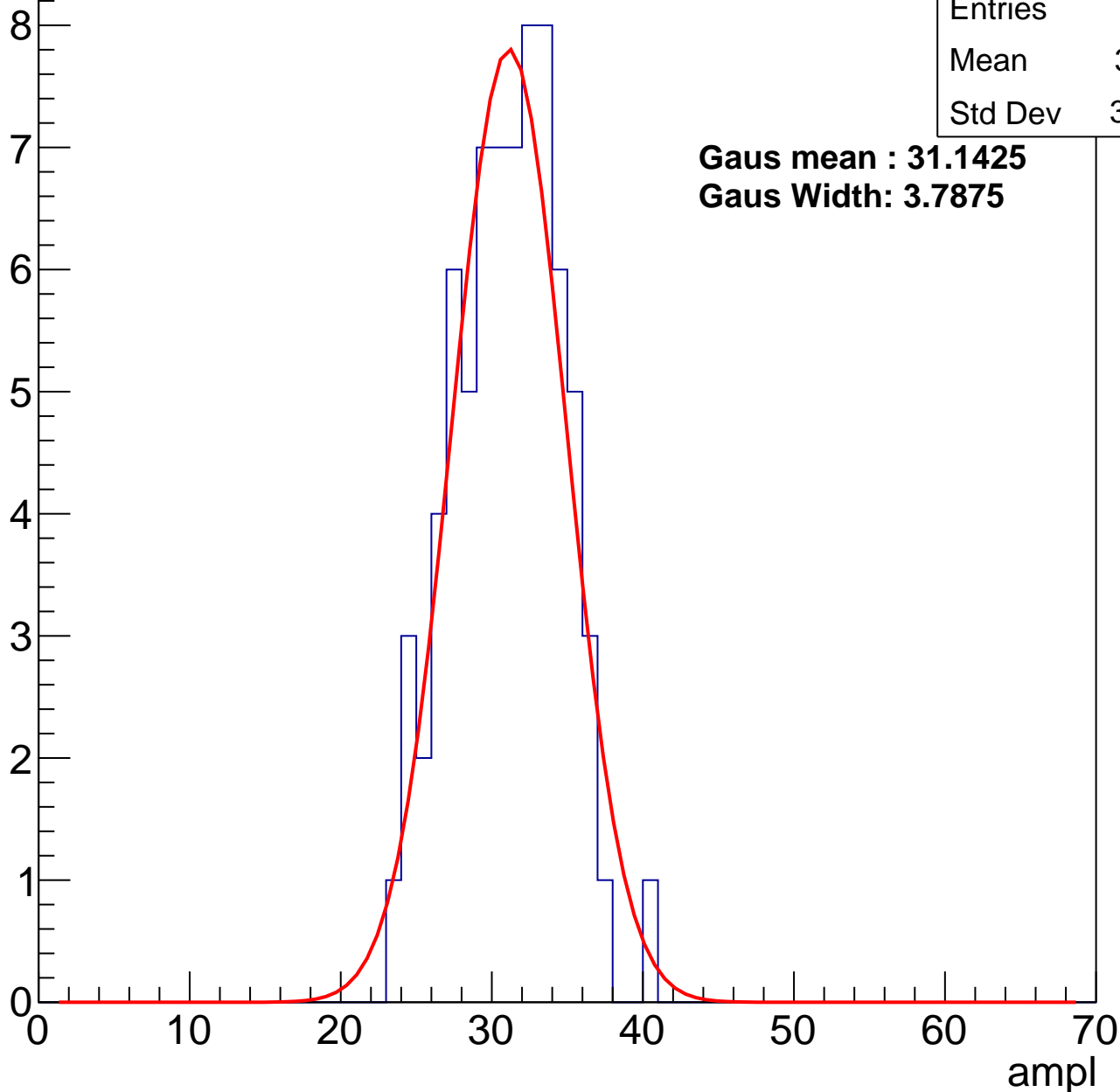
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	74
Mean	30.61
Std Dev	3.514

**Gaus mean : 31.1425**

**Gaus Width: 3.7875**



# B0L002S, U2-ch89, adc1

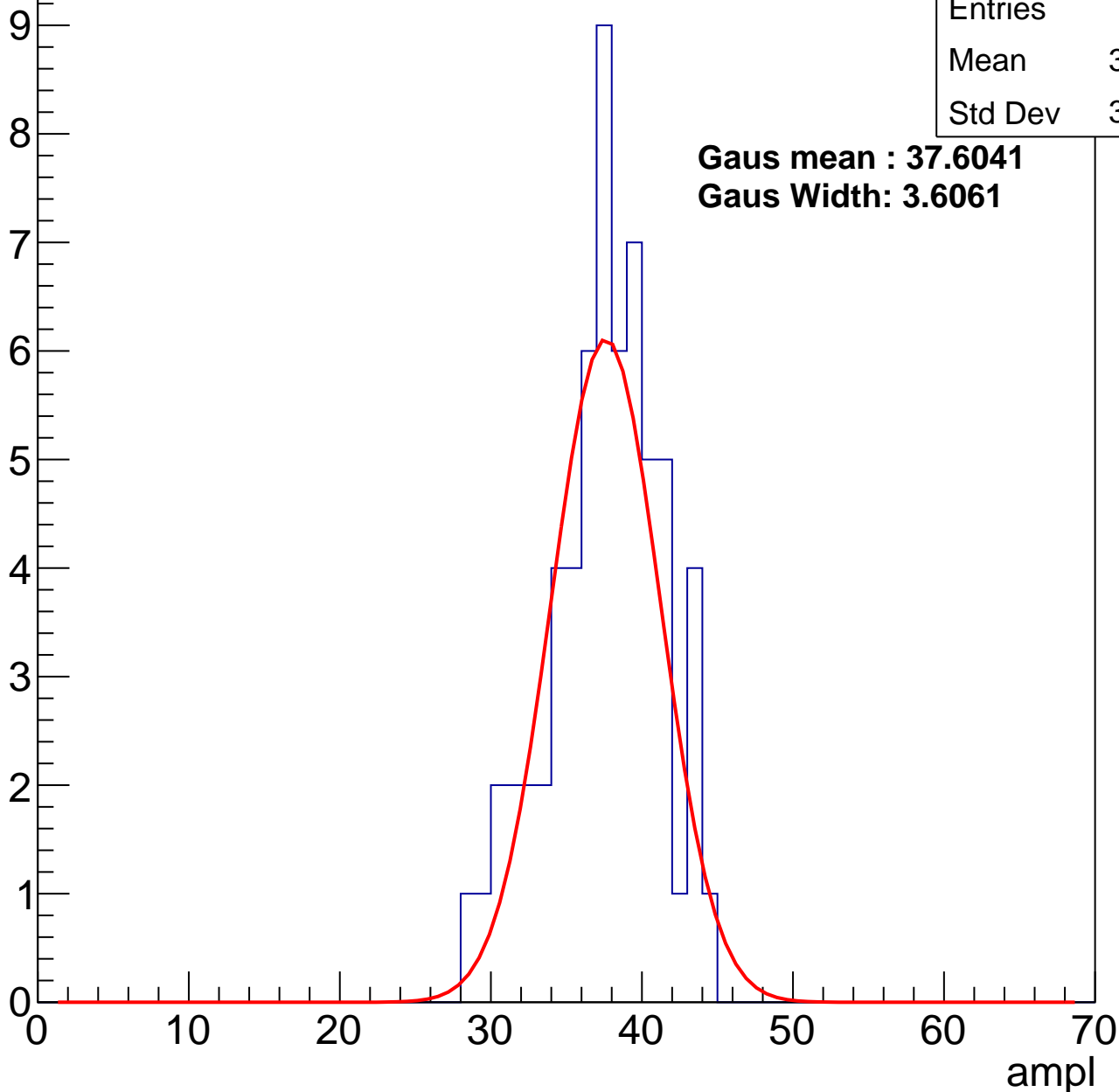
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	62
Mean	37.06
Std Dev	3.663

**Gaus mean : 37.6041**

**Gaus Width: 3.6061**



# B0L002S, U2-ch89, adc2

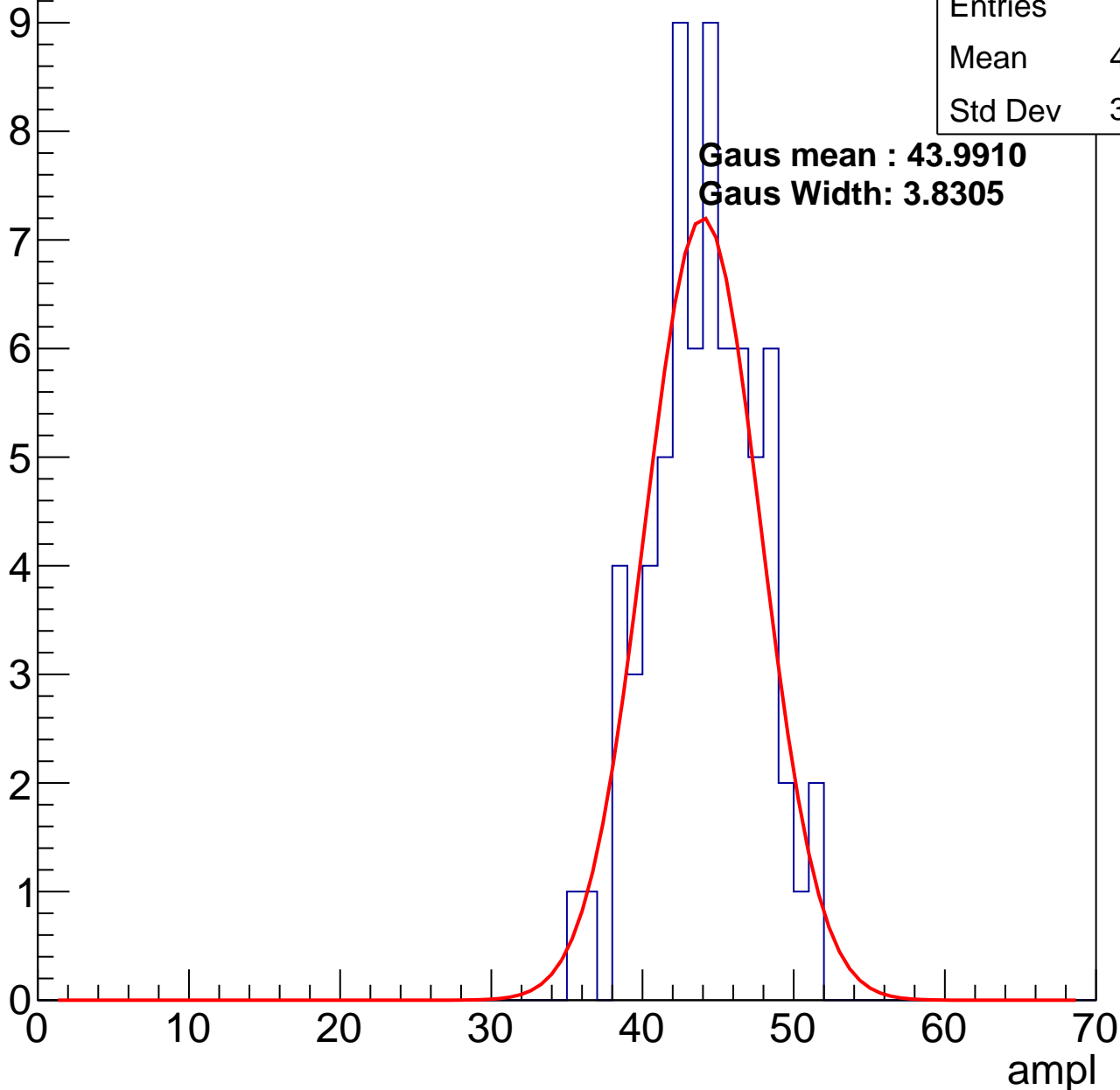
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	70
Mean	43.66
Std Dev	3.509

**Gaus mean : 43.9910**

**Gaus Width: 3.8305**

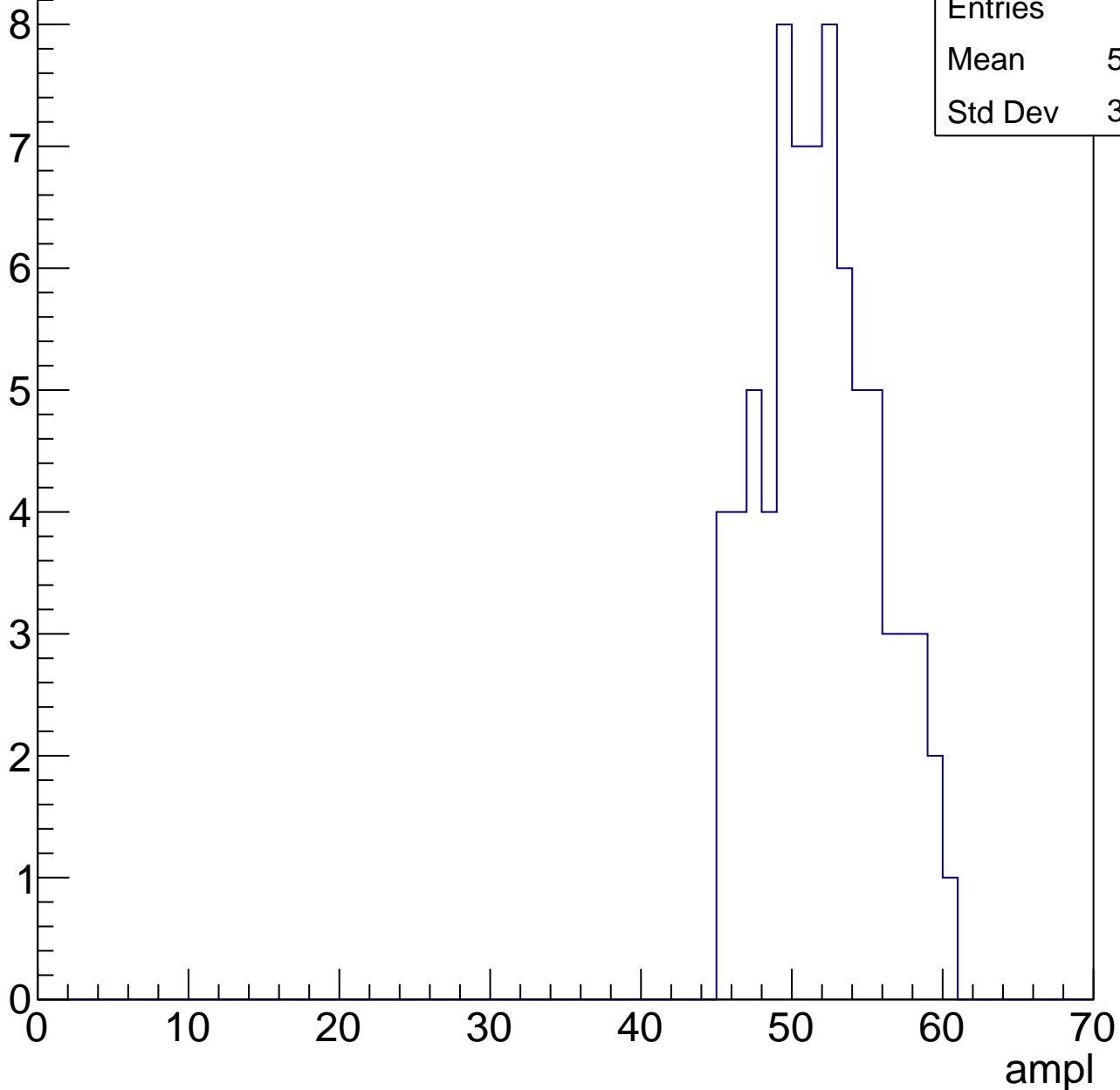


# B0L002S, U2-ch89, adc3

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	75
Mean	51.47
Std Dev	3.792

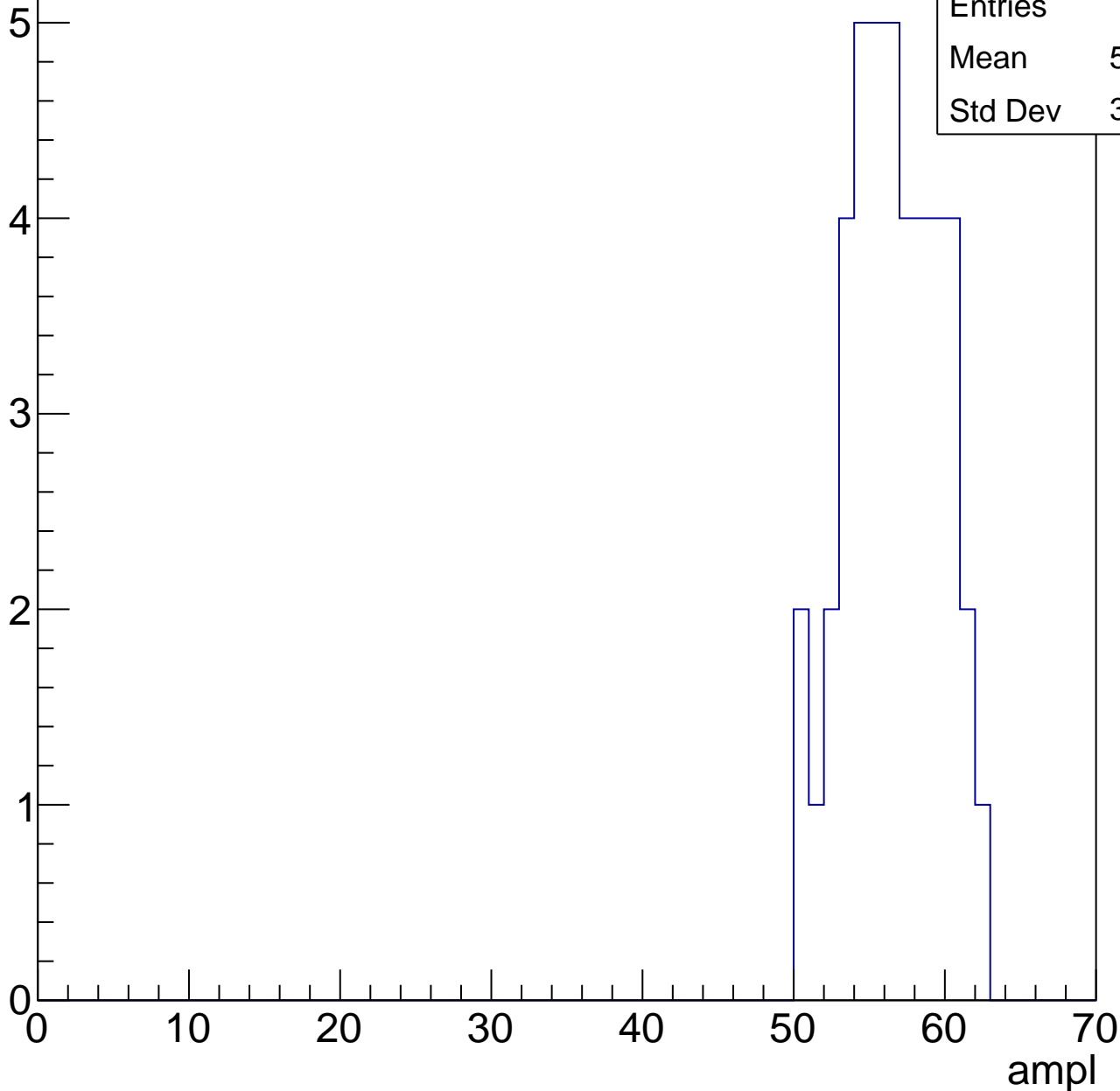


# B0L002S, U2-ch89, adc4

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	43
Mean	56.09
Std Dev	3.033

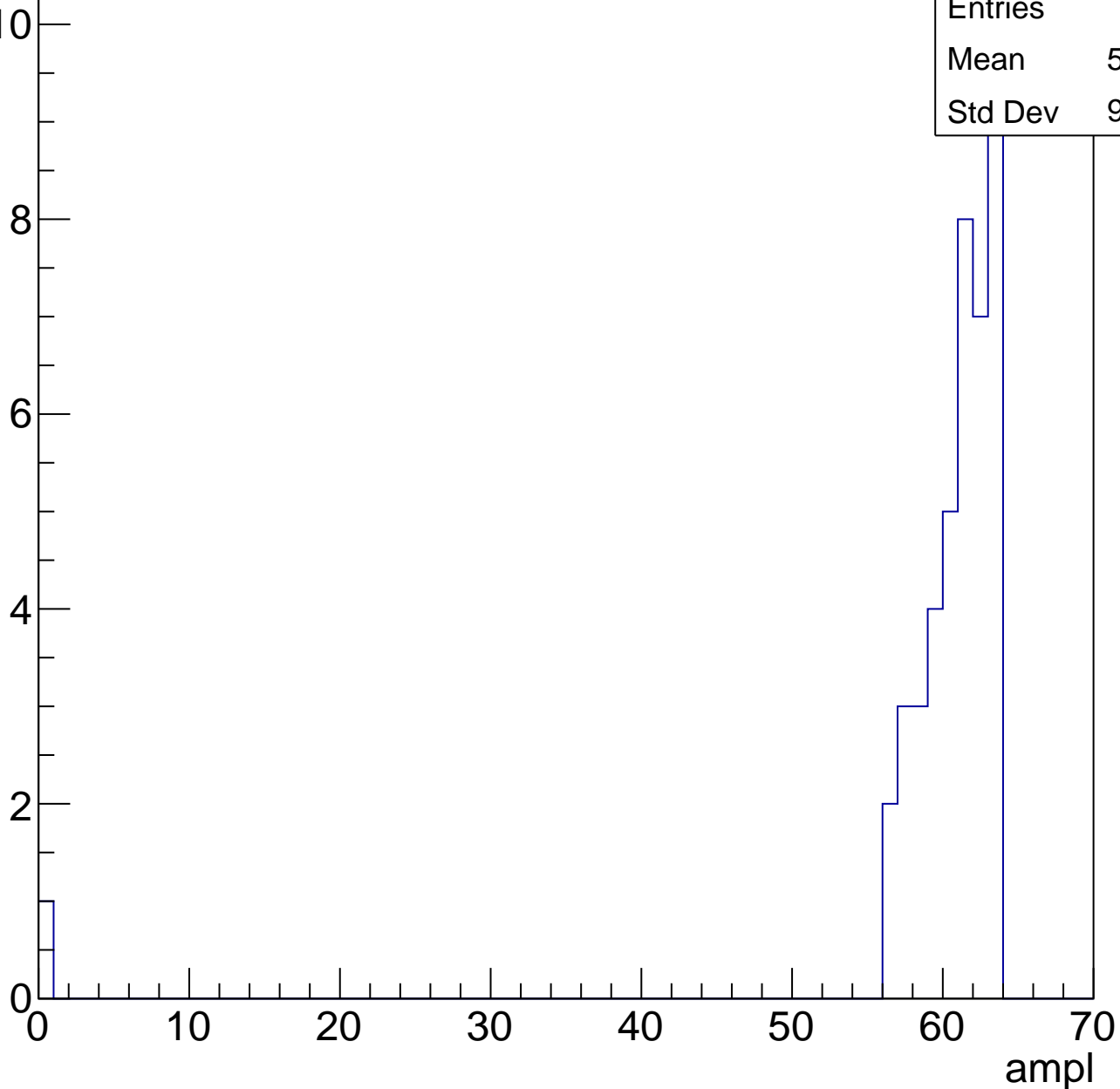


# B0L002S, U2-ch89, adc5

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	43
Mean	59.19
Std Dev	9.367



# B0L002S, U2-ch89, adc6

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry





# B0L002S, U2-ch89, adc7

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L002S, U2-ch90, adc0

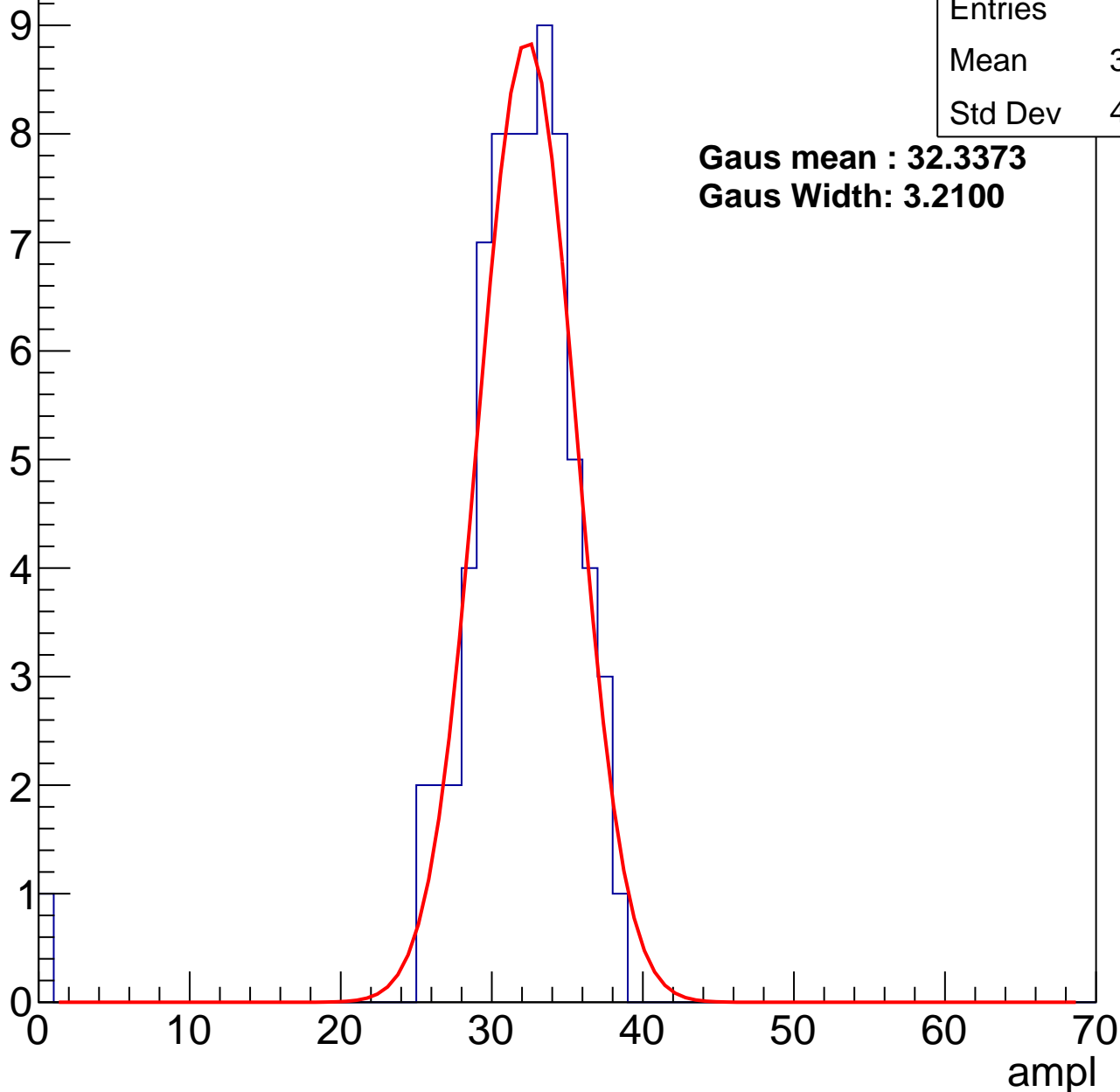
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	72
Mean	31.28
Std Dev	4.765

**Gaus mean : 32.3373**

**Gaus Width: 3.2100**



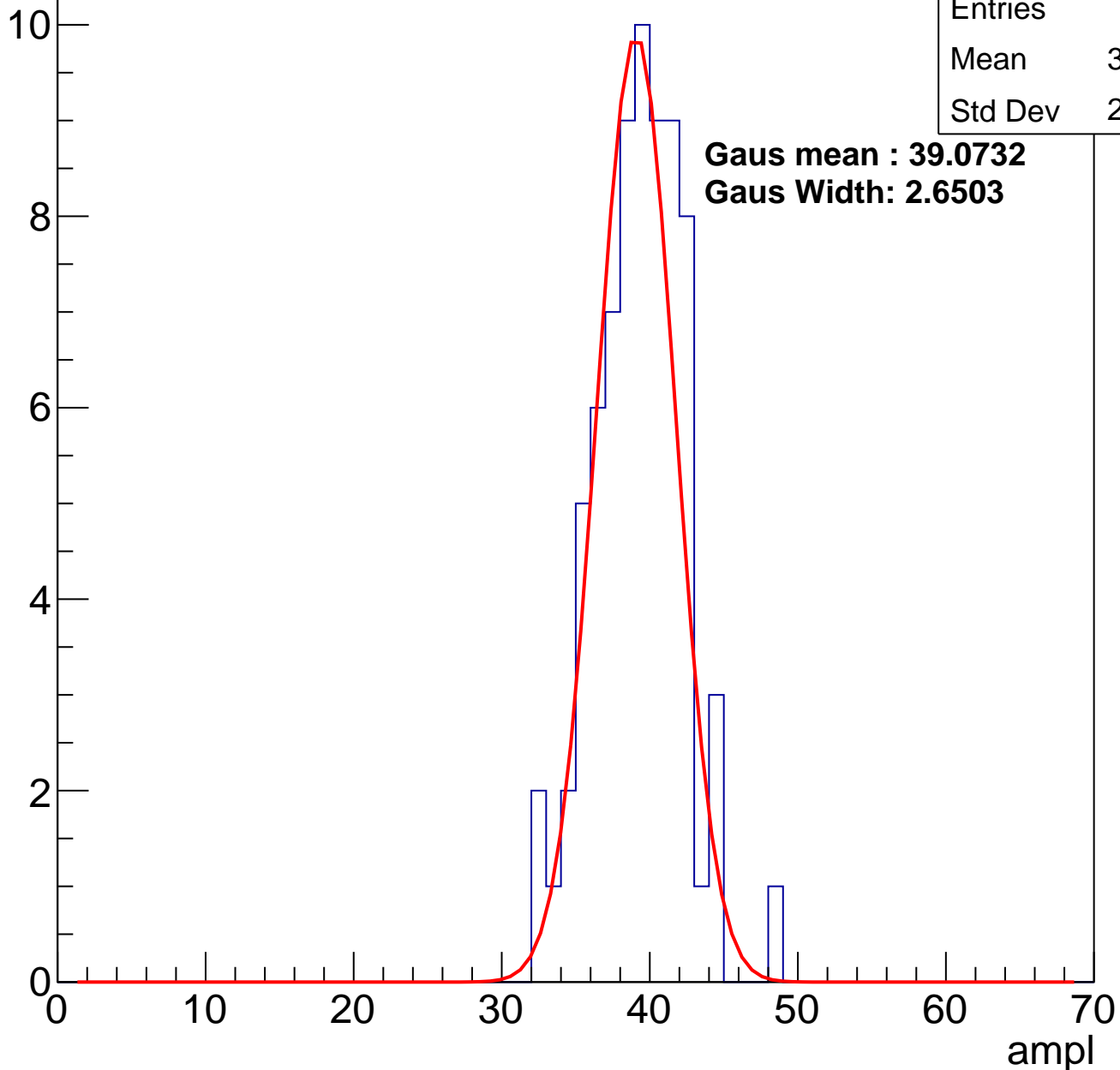
# B0L002S, U2-ch90, adc1

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entries	73
Mean	38.84
Std Dev	2.966

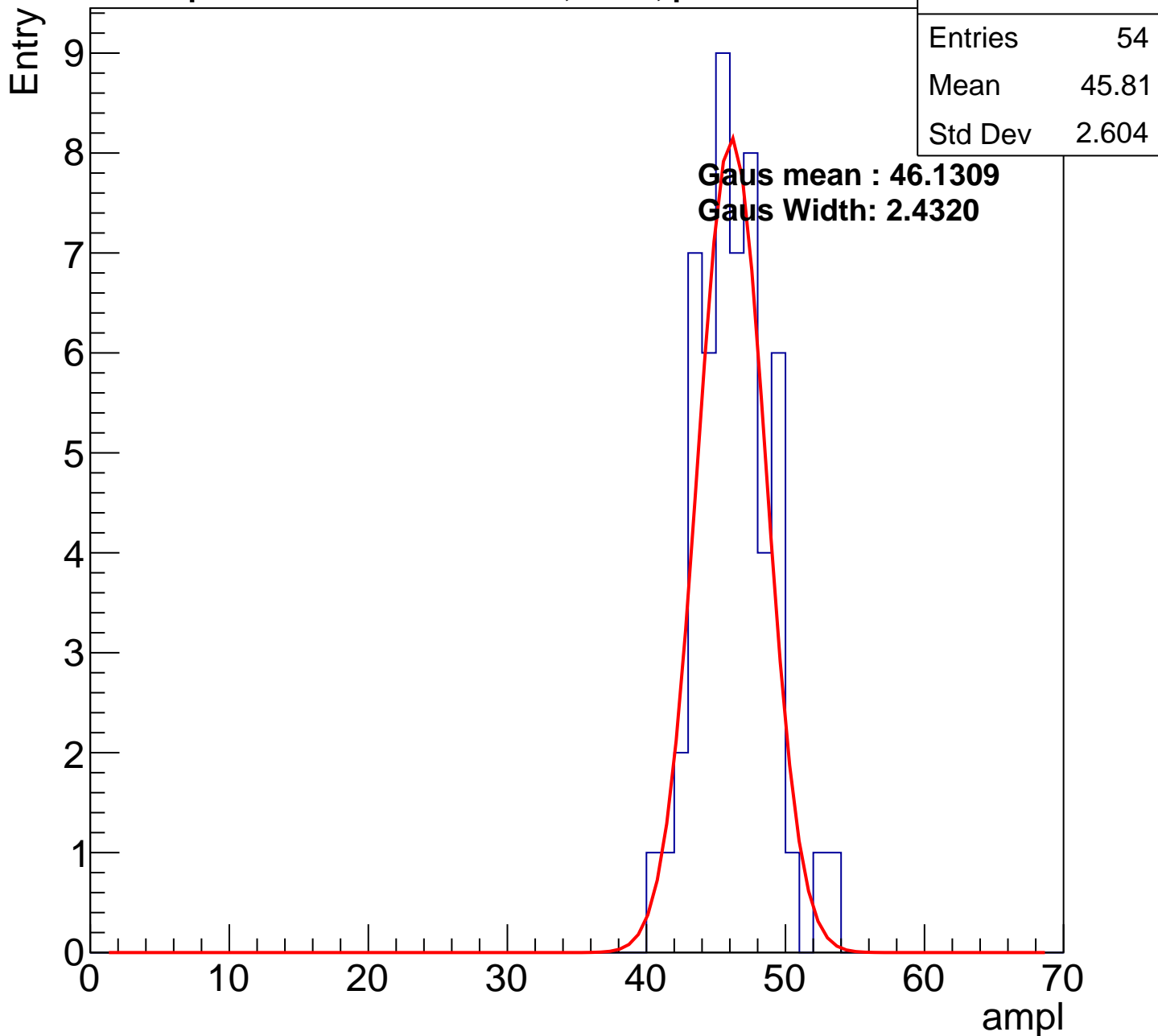
**Gaus mean : 39.0732**  
**Gaus Width: 2.6503**

Entry



# B0L002S, U2-ch90, adc2

calib\_packv5\_042523\_0143.root, FC#8, port C1

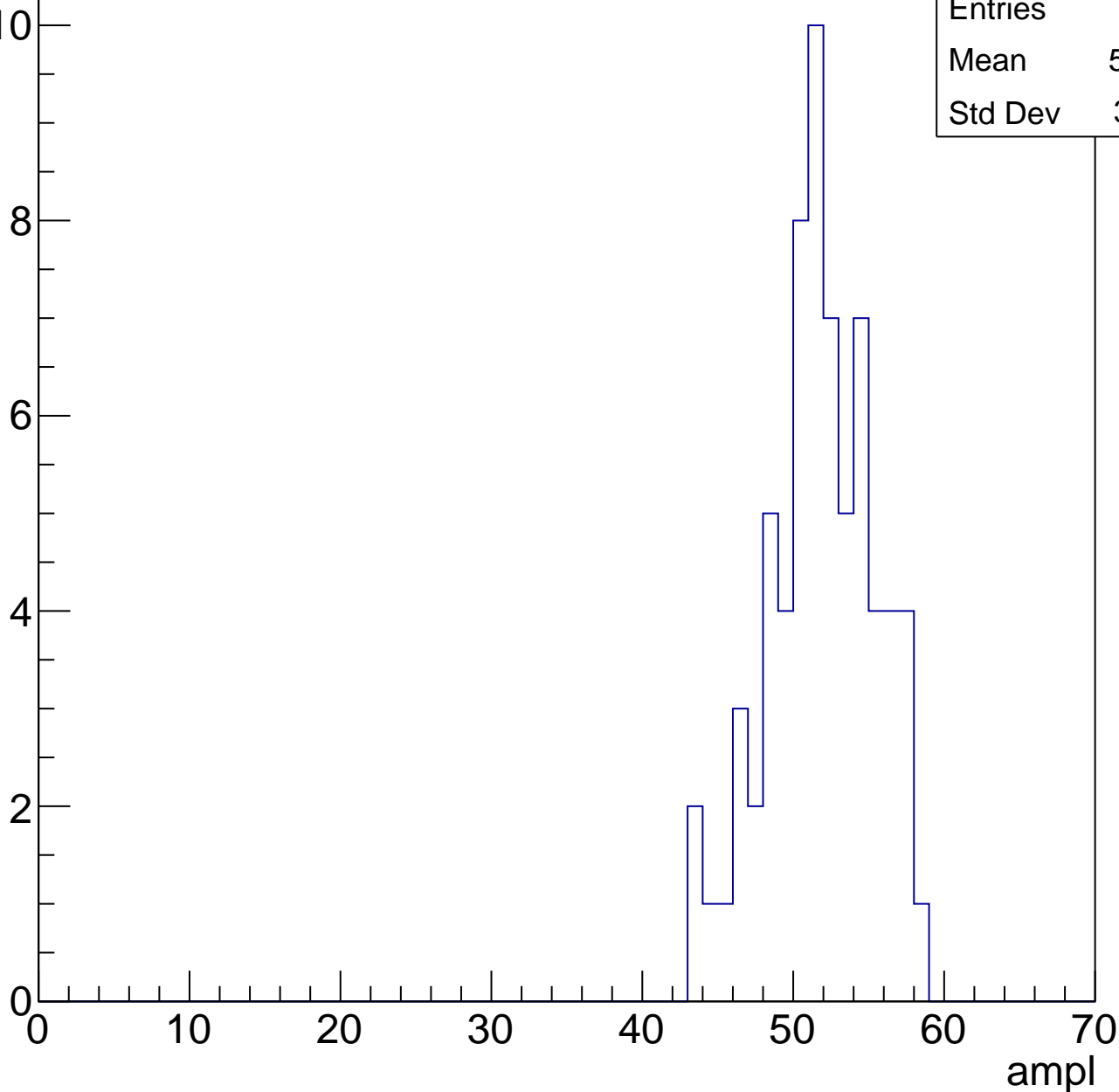


# B0L002S, U2-ch90, adc3

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	68
Mean	51.32
Std Dev	3.491

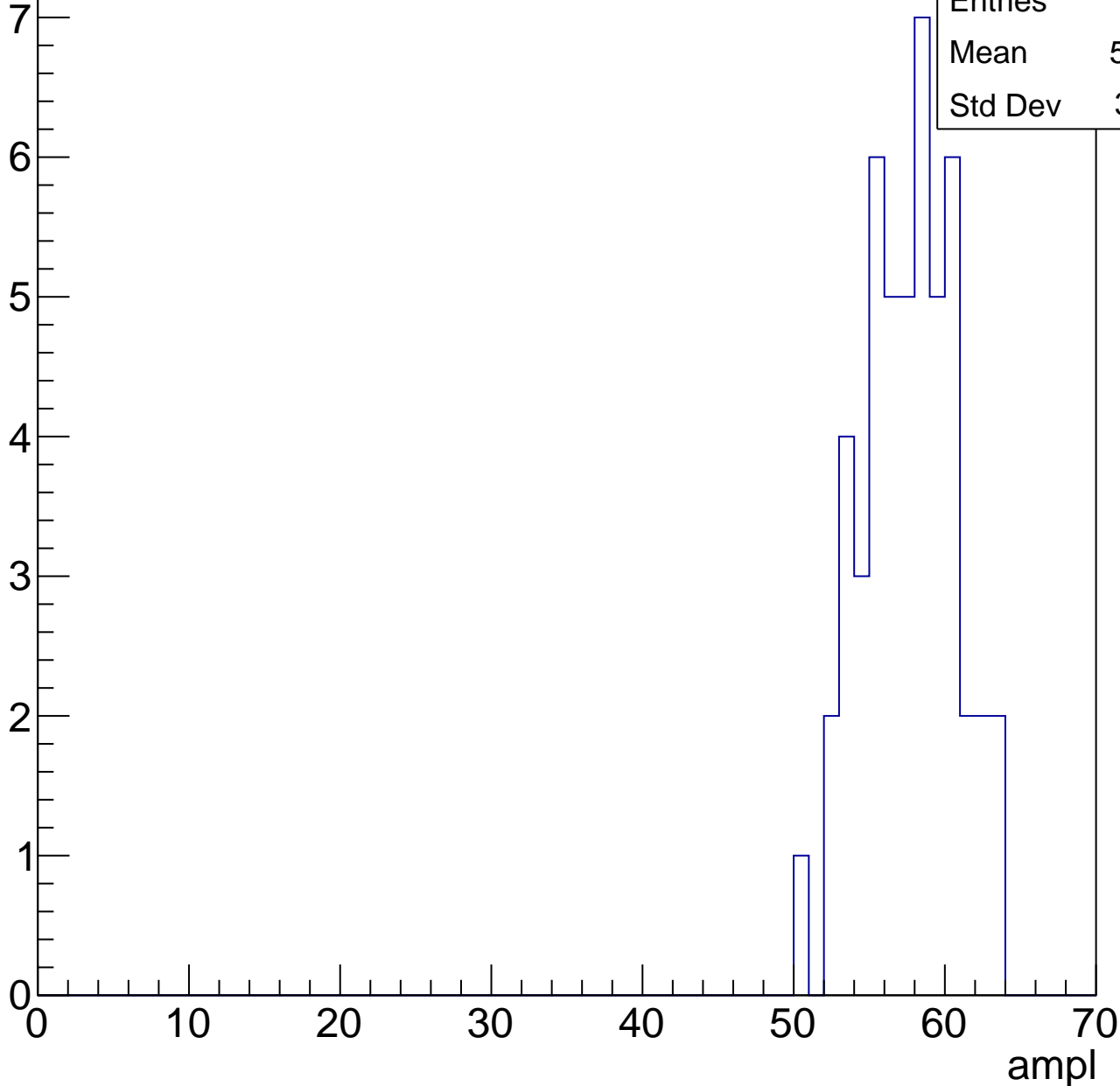


# B0L002S, U2-ch90, adc4

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	50
Mean	57.12
Std Dev	3.011

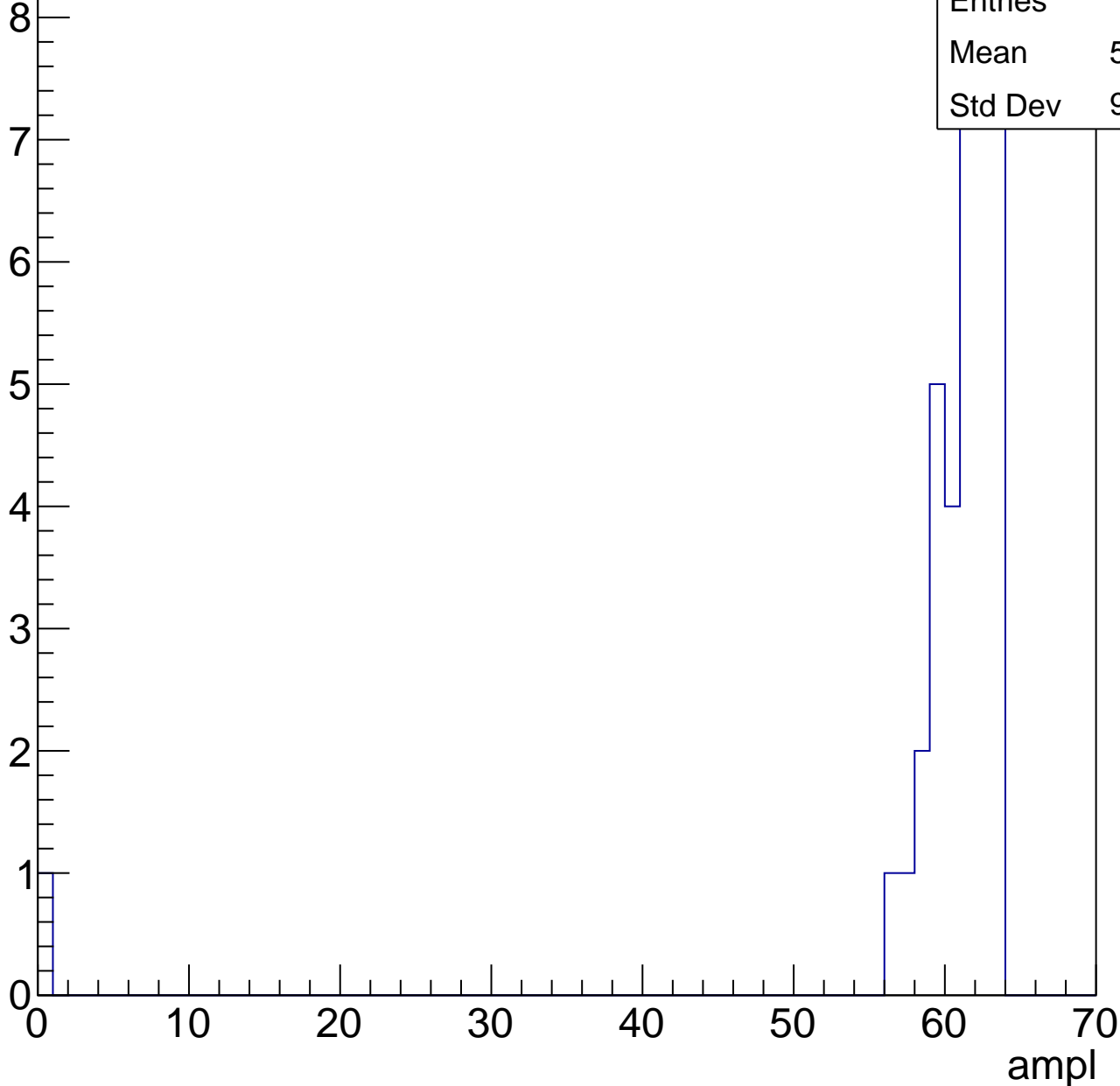


# B0L002S, U2-ch90, adc5

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	38
Mean	59.26
Std Dev	9.907



# B0L002S, U2-ch90, adc6

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



Entries	0
Mean	0
Std Dev	0



# B0L002S, U2-ch90, adc7

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



Entries	3
Mean	0
Std Dev	0

# B0L002S, U2-ch91, adc0

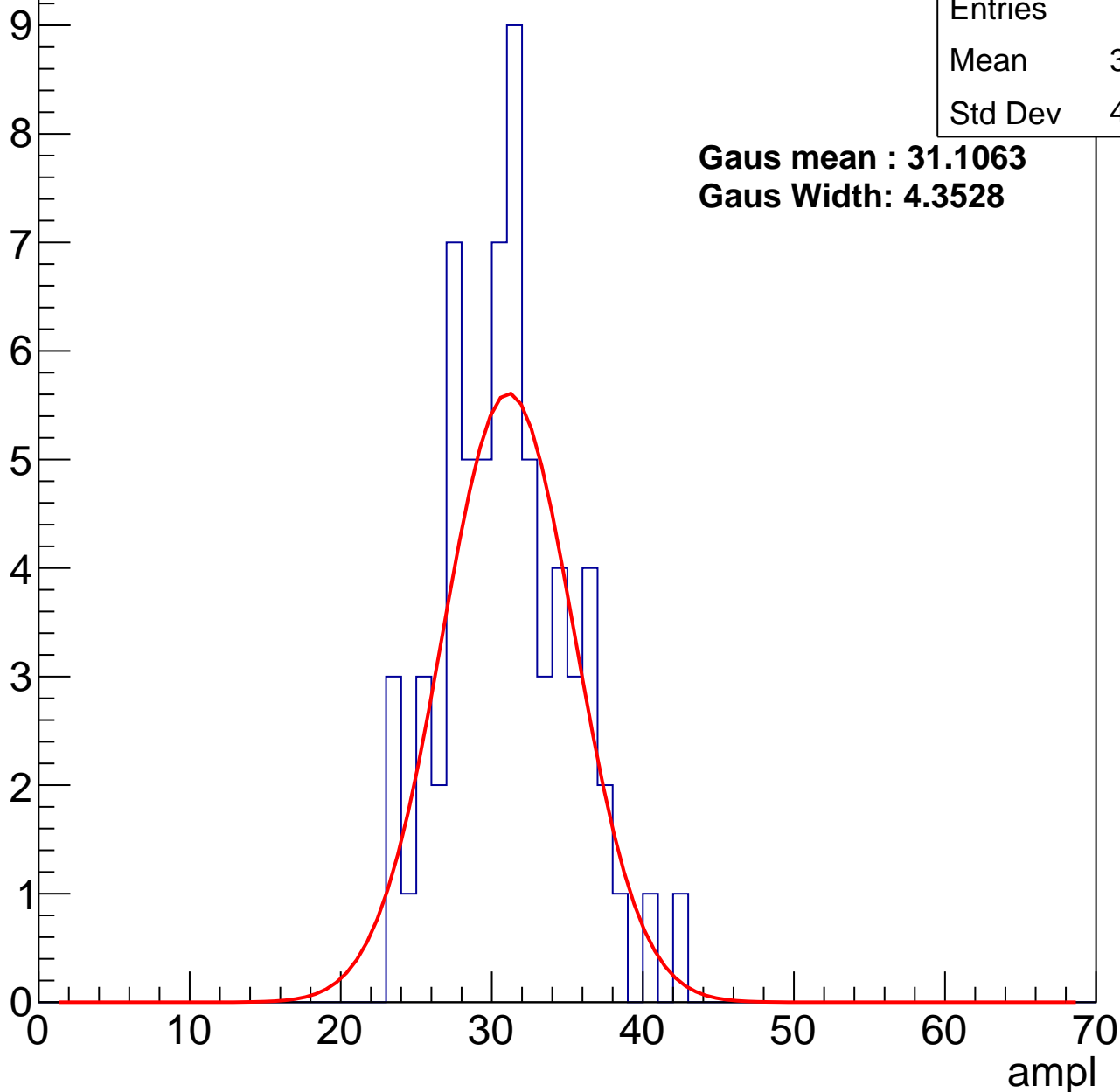
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	66
Mean	30.62
Std Dev	4.078

**Gaus mean : 31.1063**

**Gaus Width: 4.3528**



# B0L002S, U2-ch91, adc1

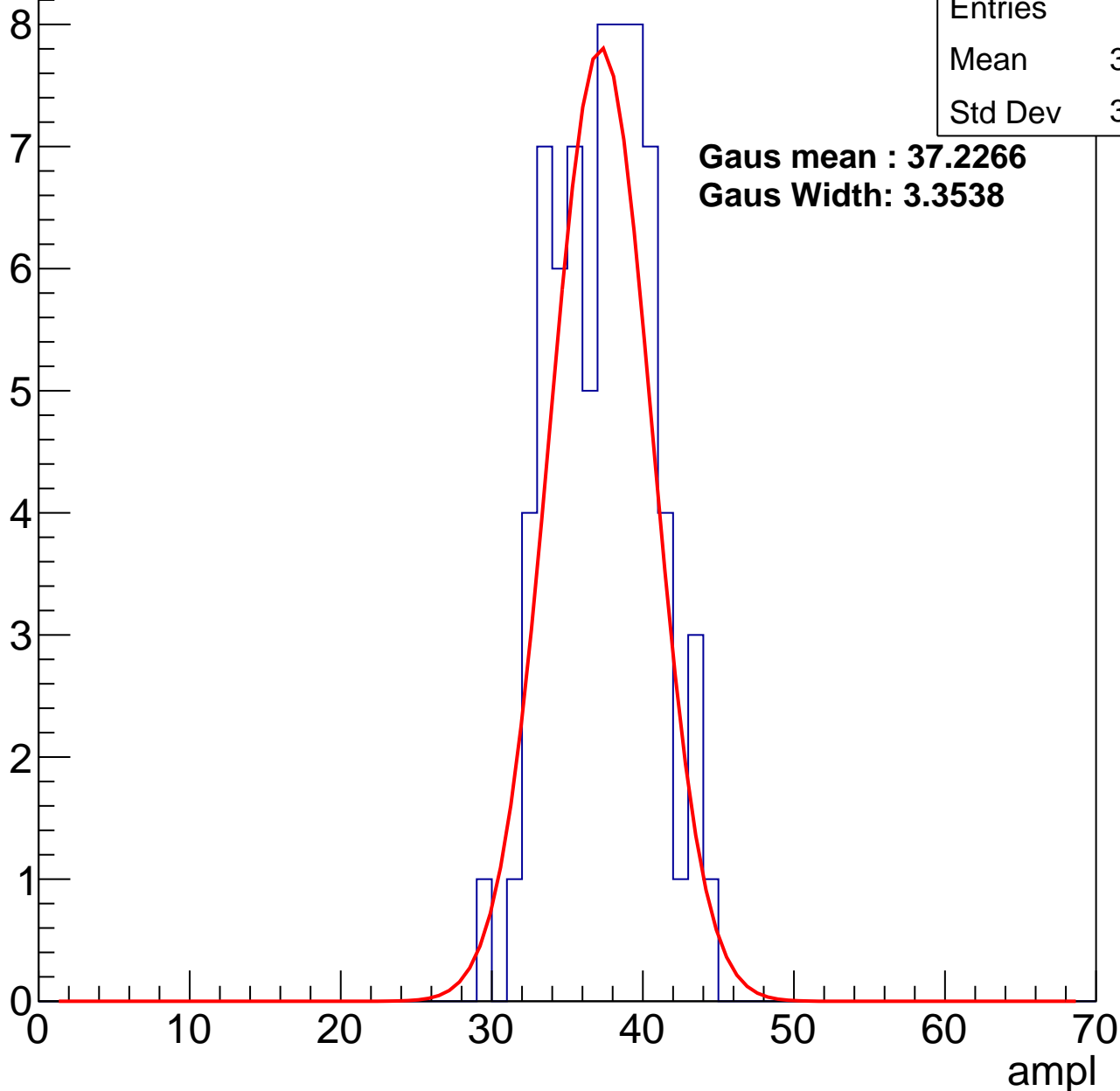
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	71
Mean	36.89
Std Dev	3.244

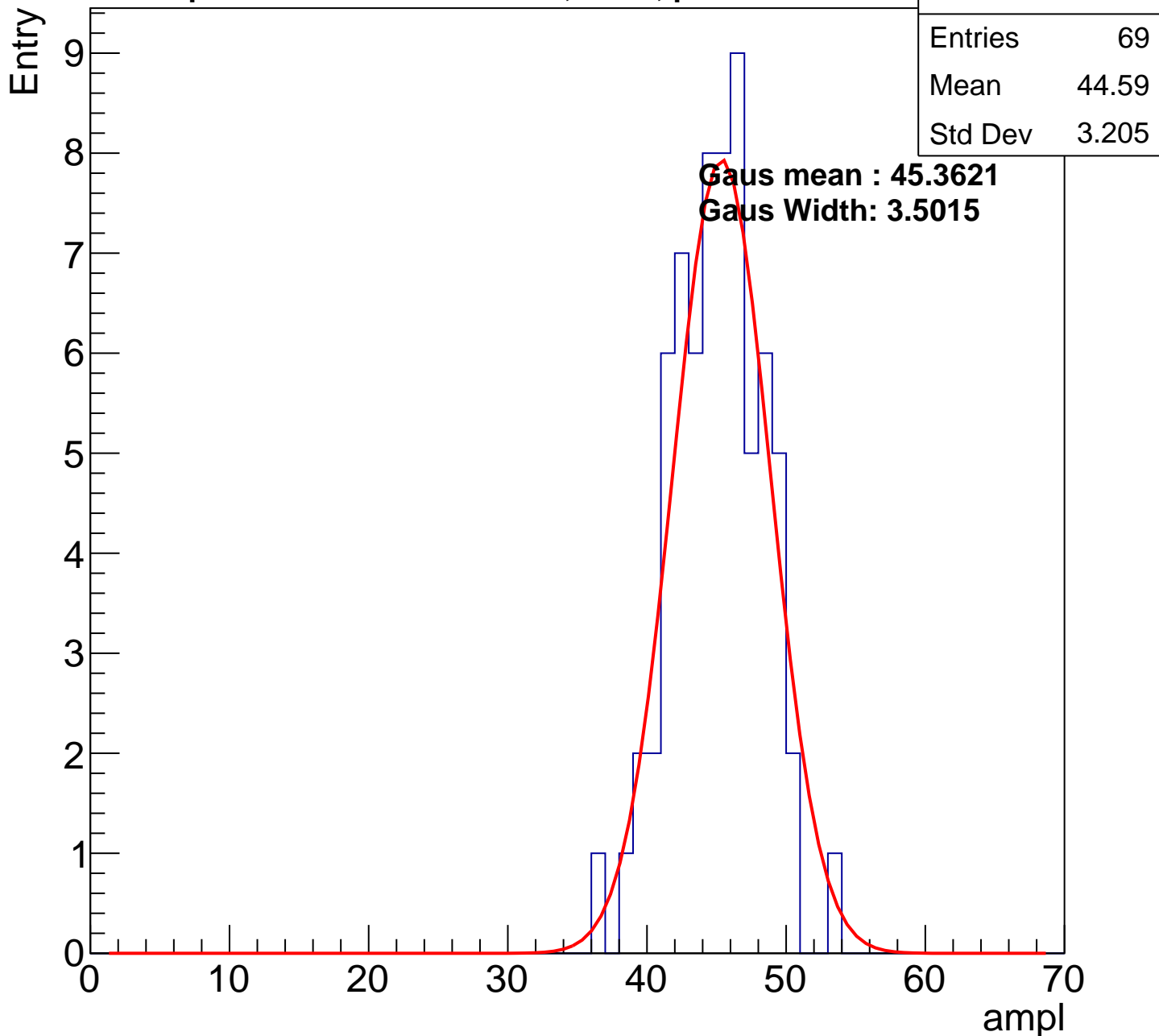
**Gaus mean : 37.2266**

**Gaus Width: 3.3538**



# B0L002S, U2-ch91, adc2

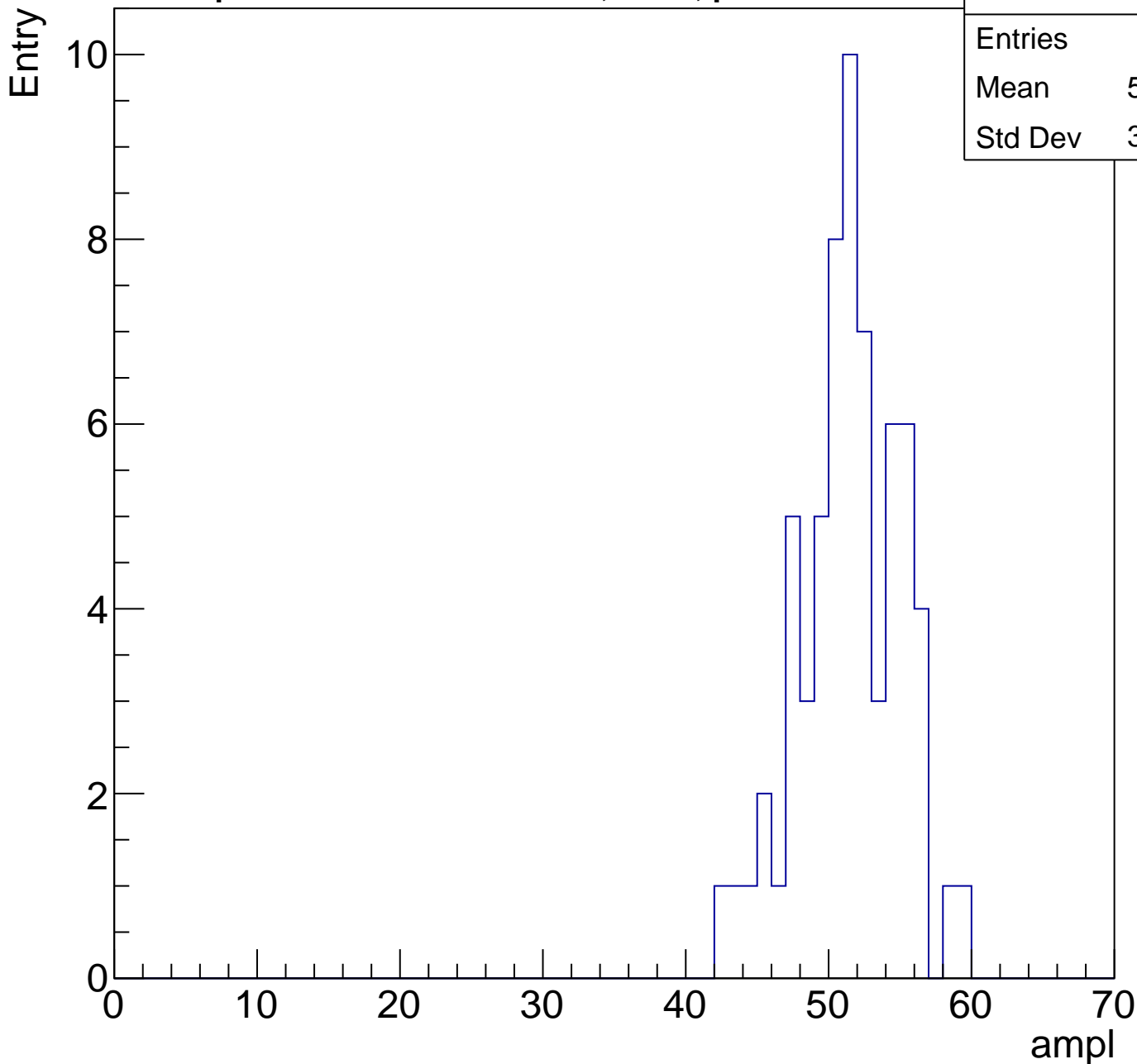
calib\_packv5\_042523\_0143.root, FC#8, port C1



# B0L002S, U2-ch91, adc3

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entries	65
Mean	51.03
Std Dev	3.526

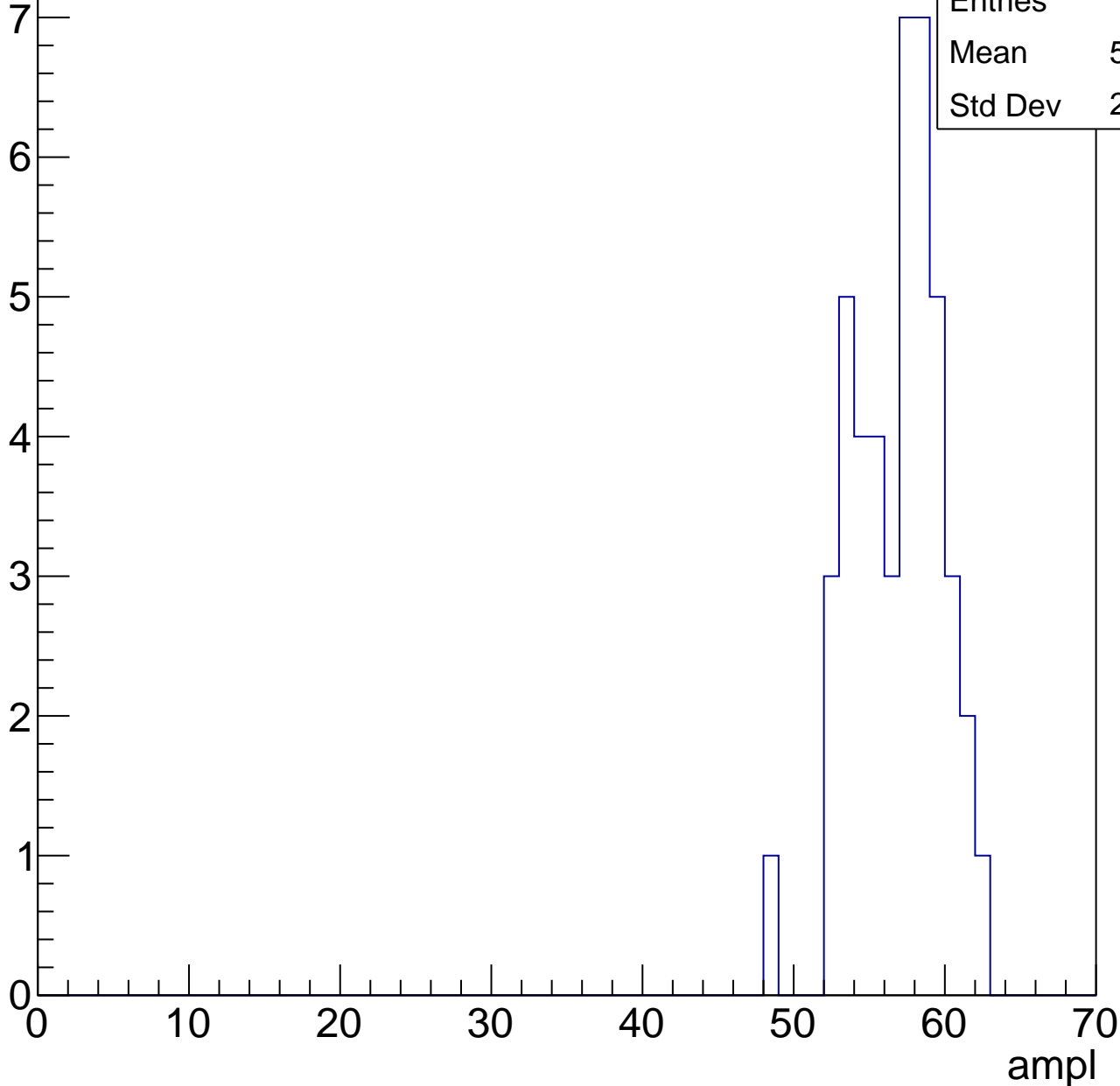


# B0L002S, U2-ch91, adc4

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	45
Mean	56.38
Std Dev	2.923

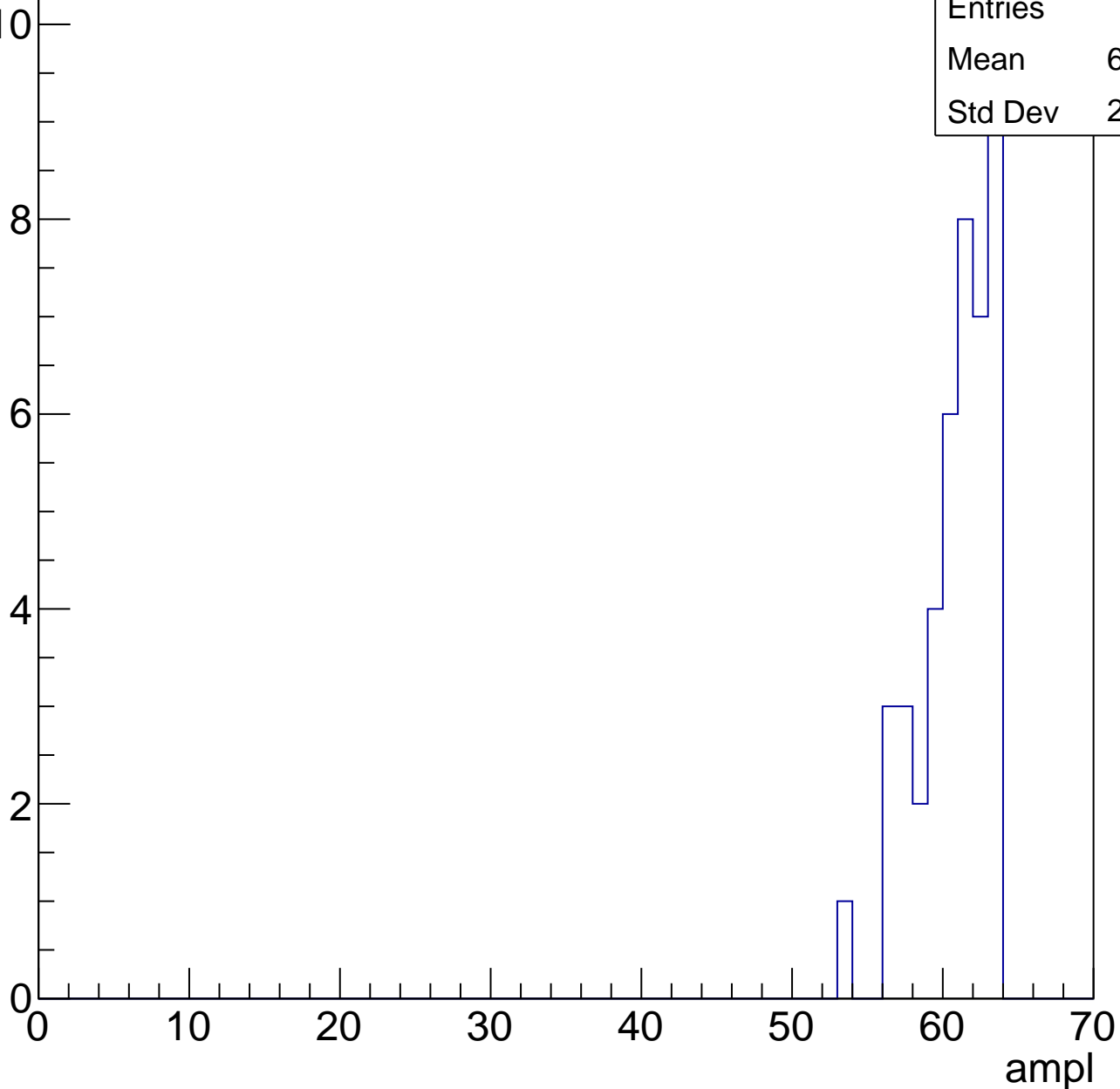


# B0L002S, U2-ch91, adc5

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

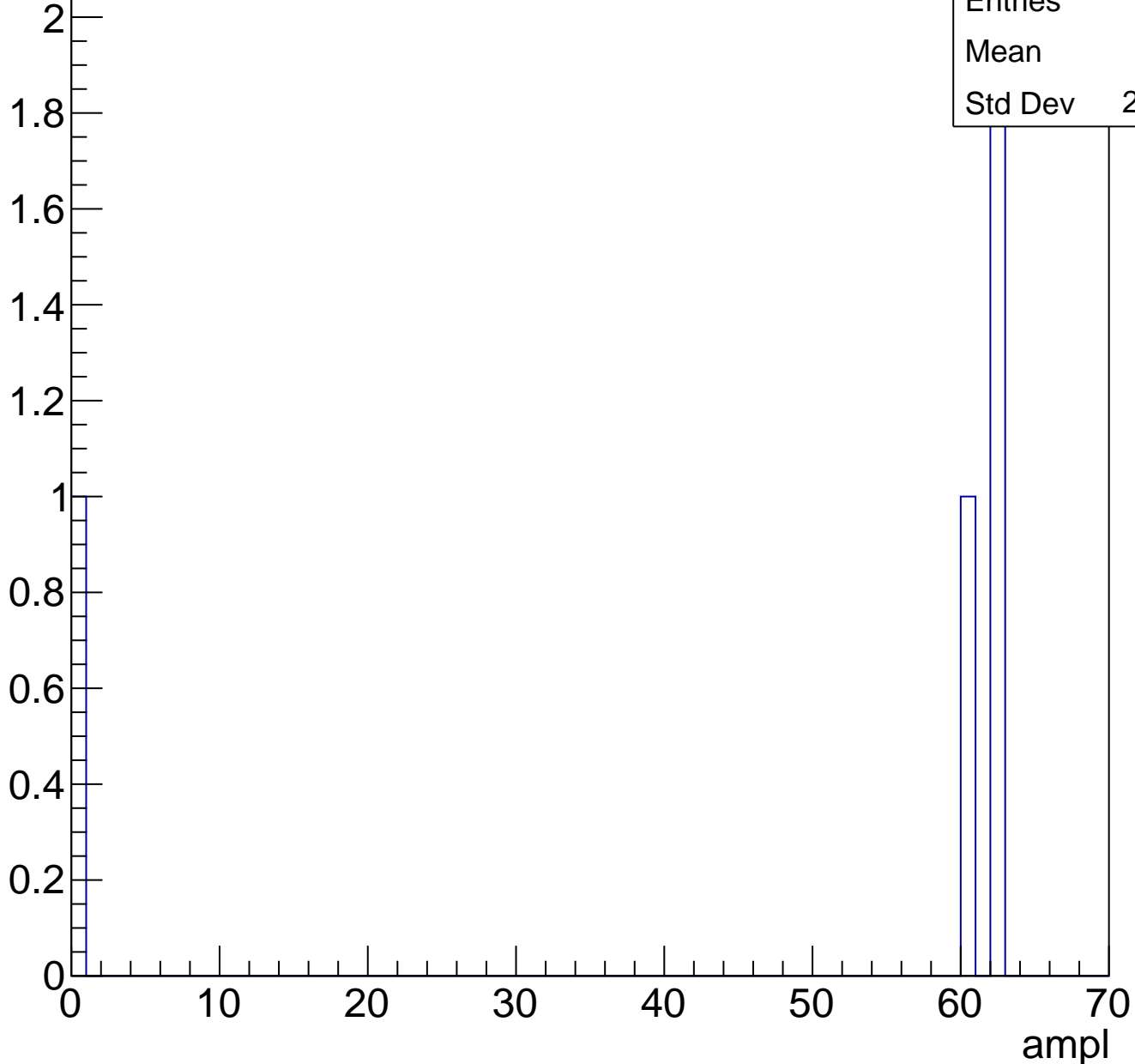
Entries	44
Mean	60.36
Std Dev	2.413



# B0L002S, U2-ch91, adc6

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



Entries	4
Mean	46
Std Dev	26.57



# B0L002S, U2-ch91, adc7

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L002S, U2-ch92, adc0

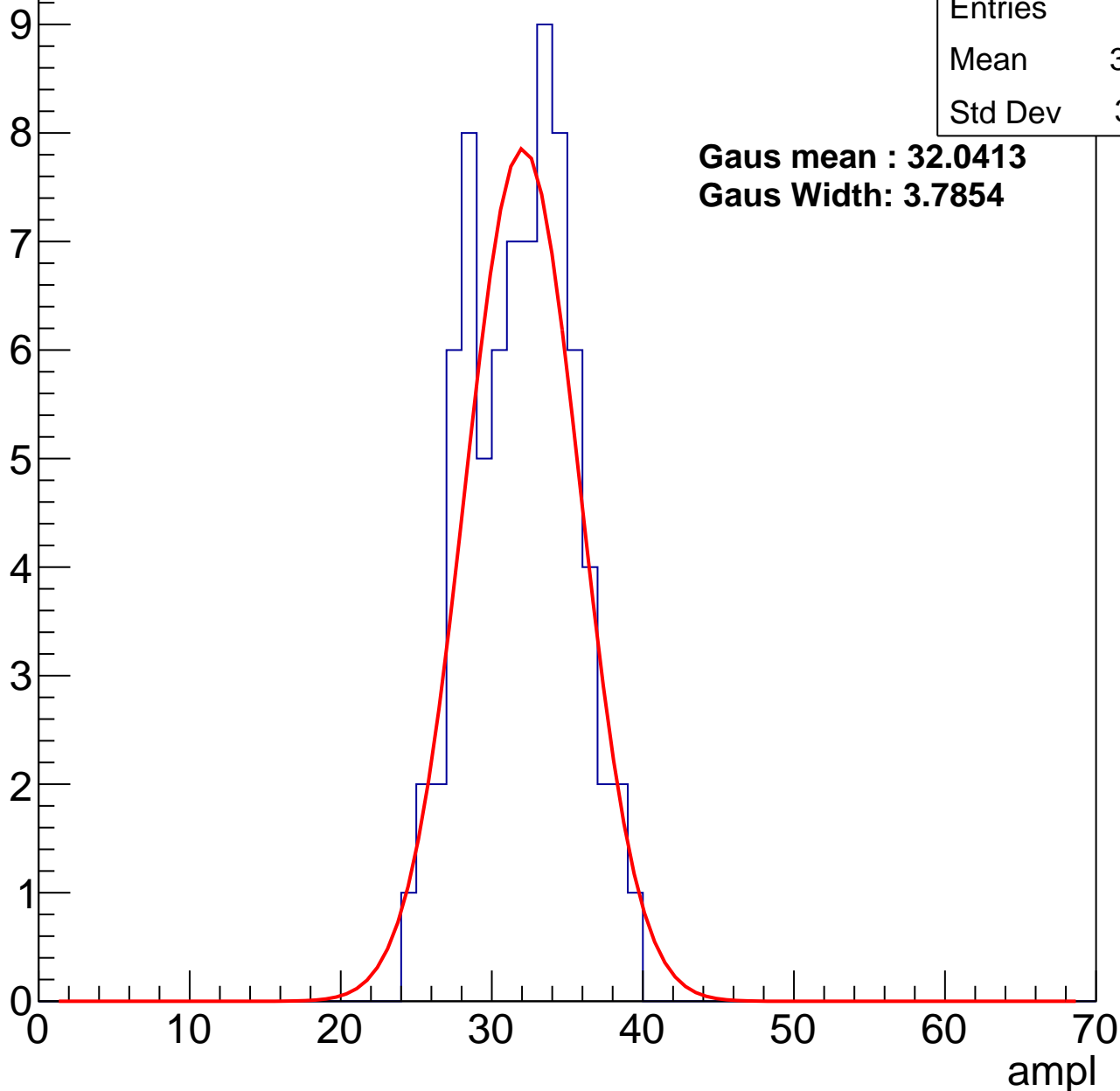
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	76
Mean	31.45
Std Dev	3.431

**Gaus mean : 32.0413**

**Gaus Width: 3.7854**



# B0L002S, U2-ch92, adc1

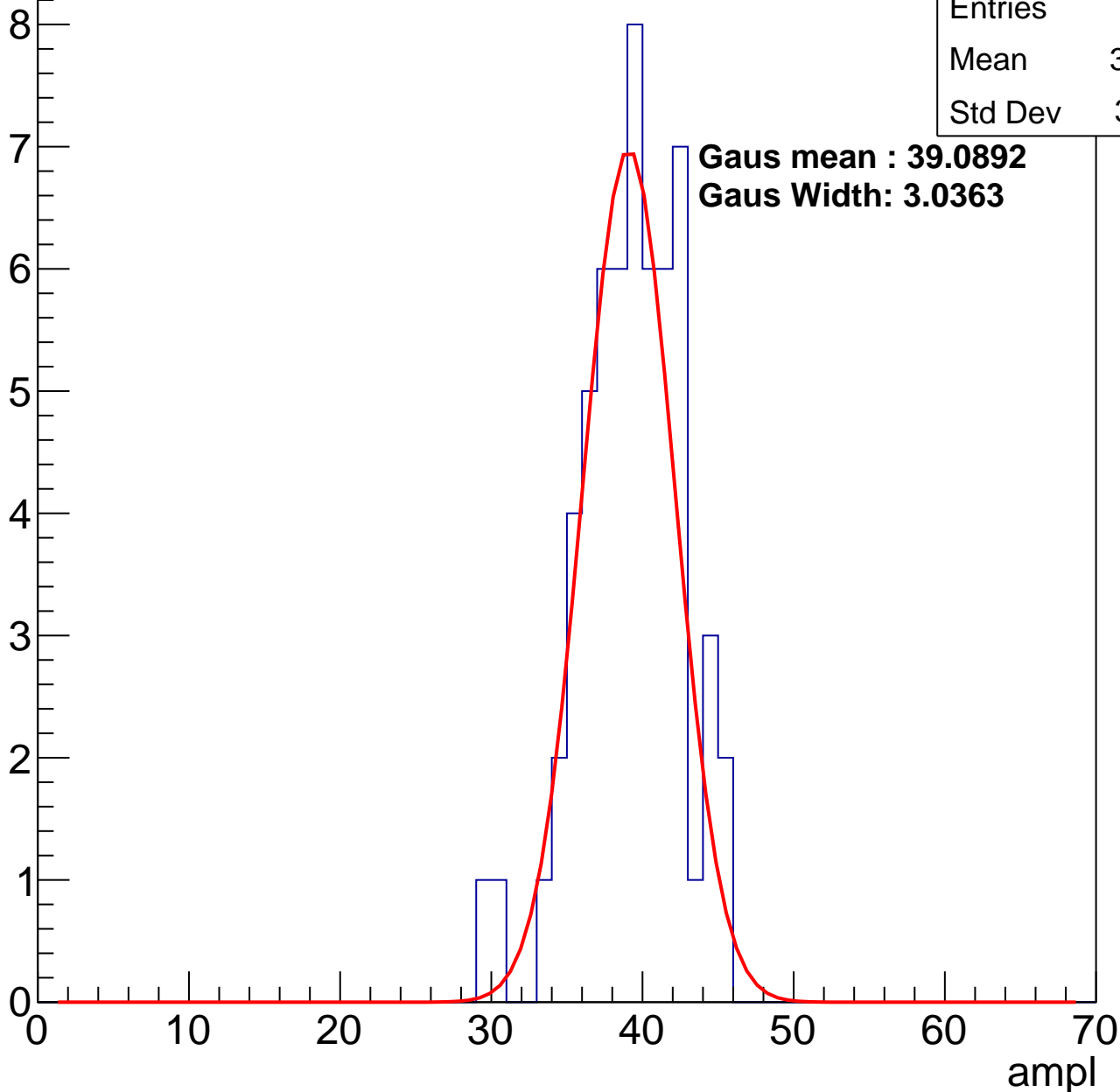
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	59
Mean	38.76
Std Dev	3.341

**Gaus mean : 39.0892**

**Gaus Width: 3.0363**



# B0L002S, U2-ch92, adc2

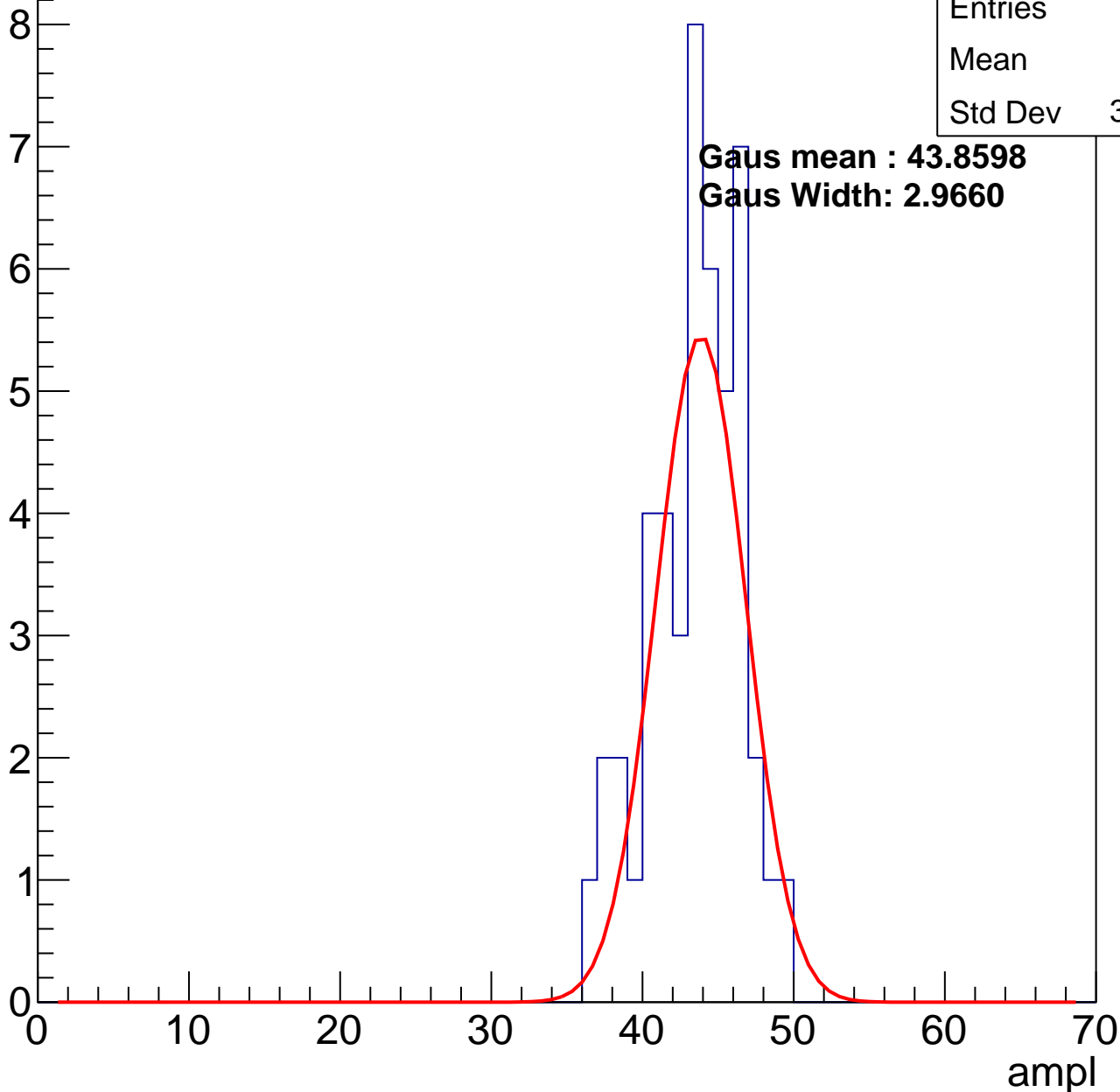
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	47
Mean	43
Std Dev	3.004

**Gaus mean : 43.8598**

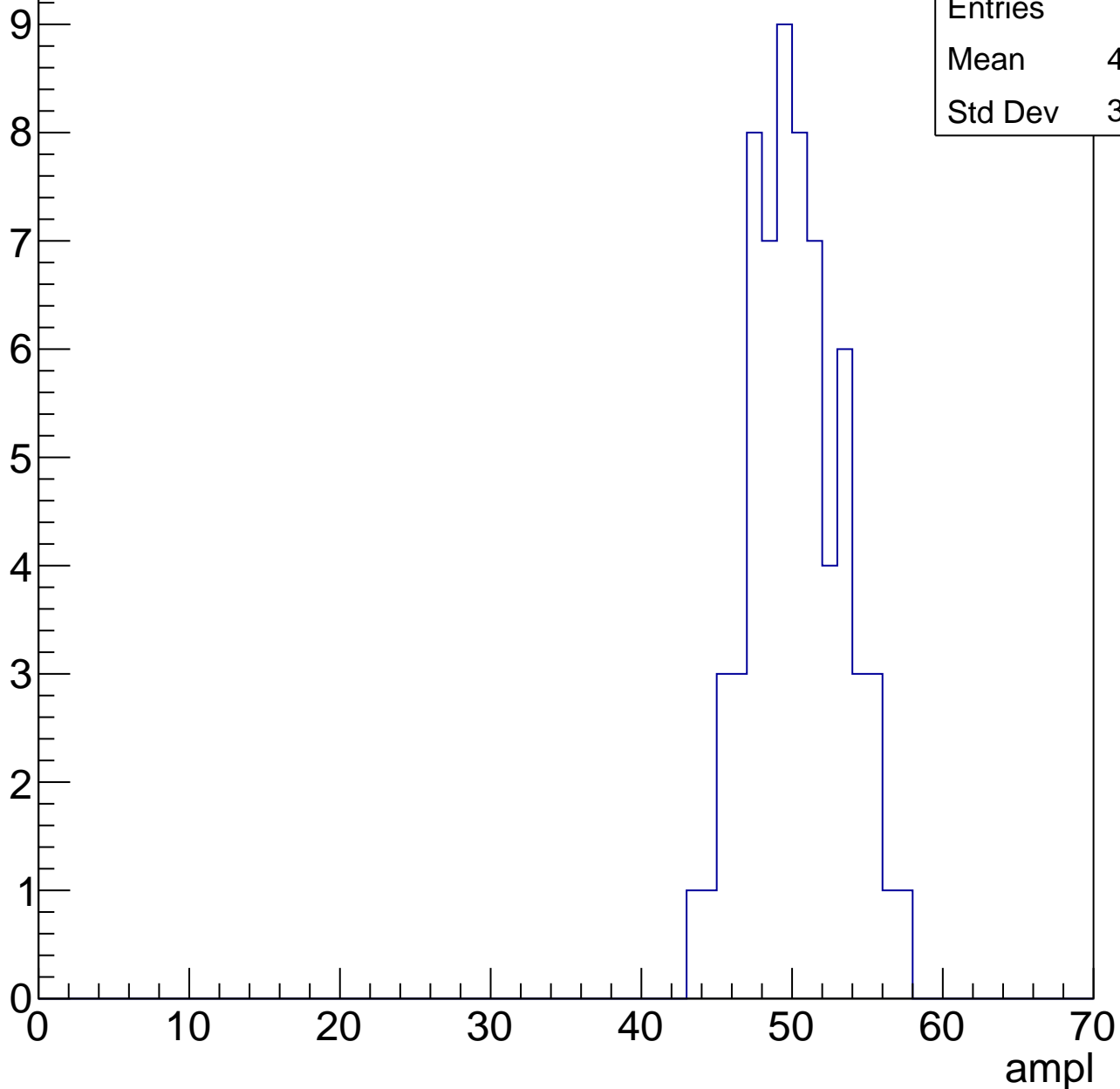
**Gaus Width: 2.9660**



# B0L002S, U2-ch92, adc3

calib\_packv5\_042523\_0143.root, FC#8, port C1

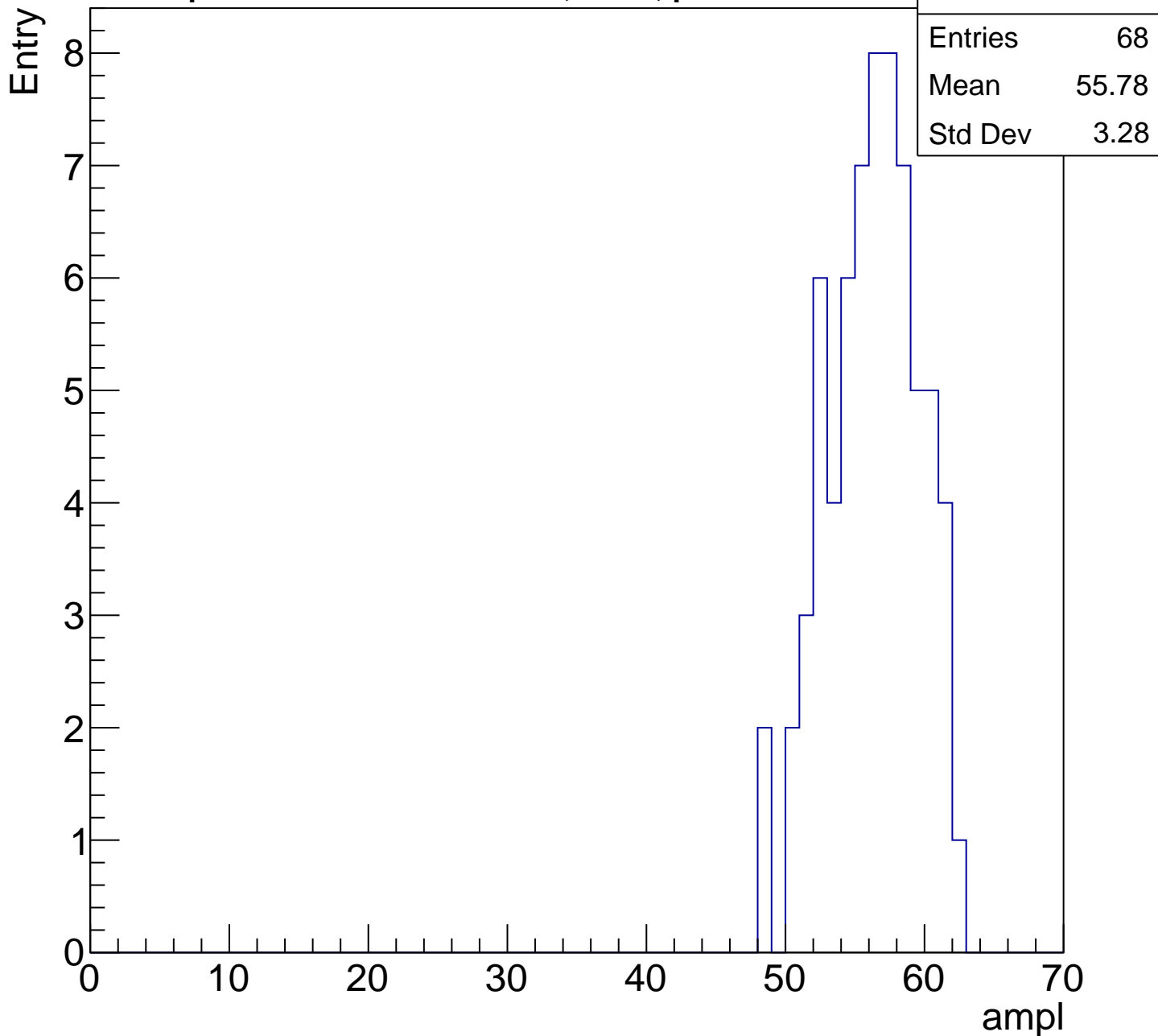
Entry



Entries	65
Mean	49.78
Std Dev	3.036

# B0L002S, U2-ch92, adc4

calib\_packv5\_042523\_0143.root, FC#8, port C1

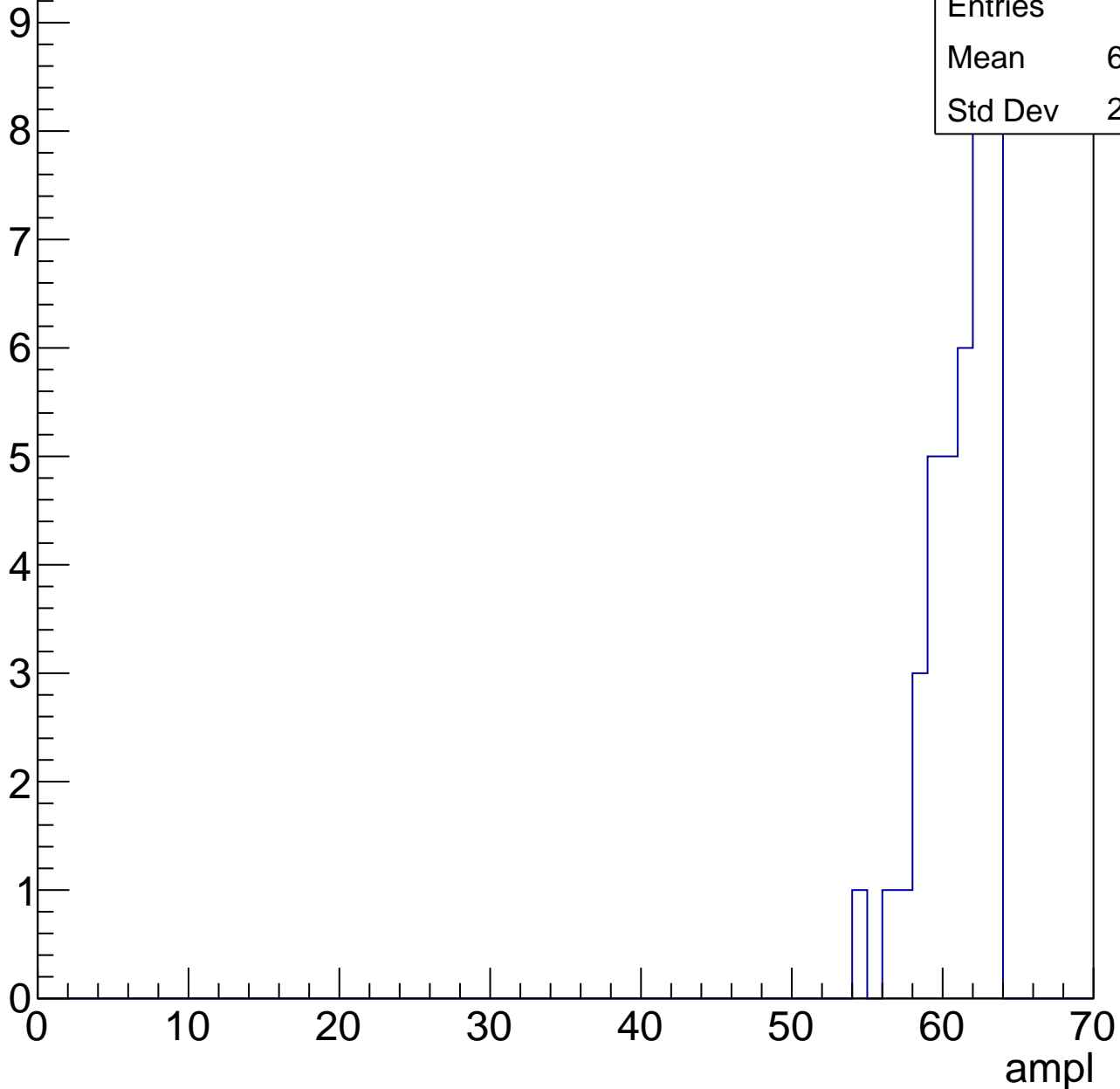


# B0L002S, U2-ch92, adc5

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	39
Mean	60.62
Std Dev	2.132



# B0L002S, U2-ch92, adc6

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry





# B0L002S, U2-ch92, adc7

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L002S, U2-ch93, adc0

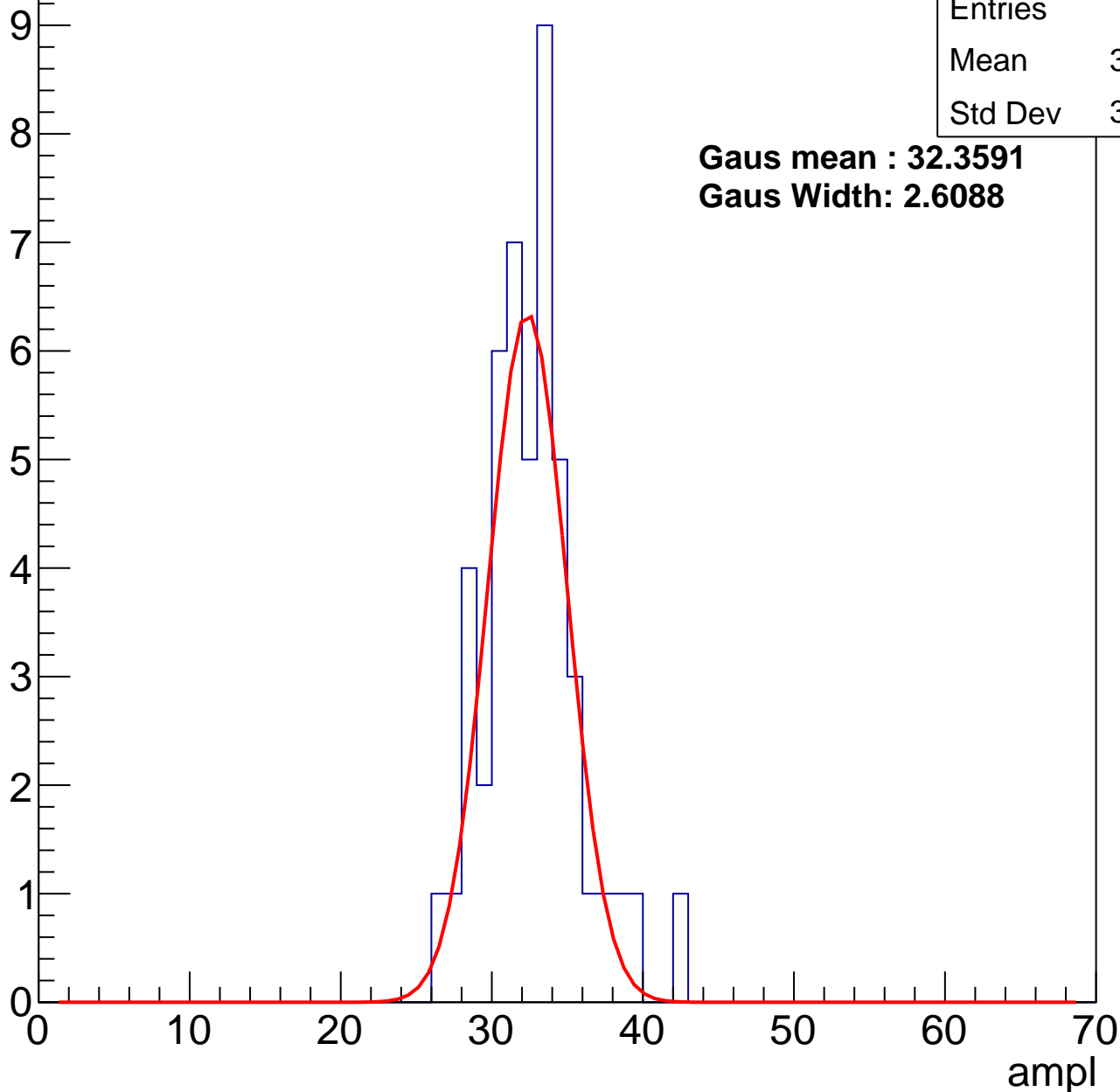
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	48
Mean	32.17
Std Dev	3.078

**Gaus mean : 32.3591**

**Gaus Width: 2.6088**



# B0L002S, U2-ch93, adc1

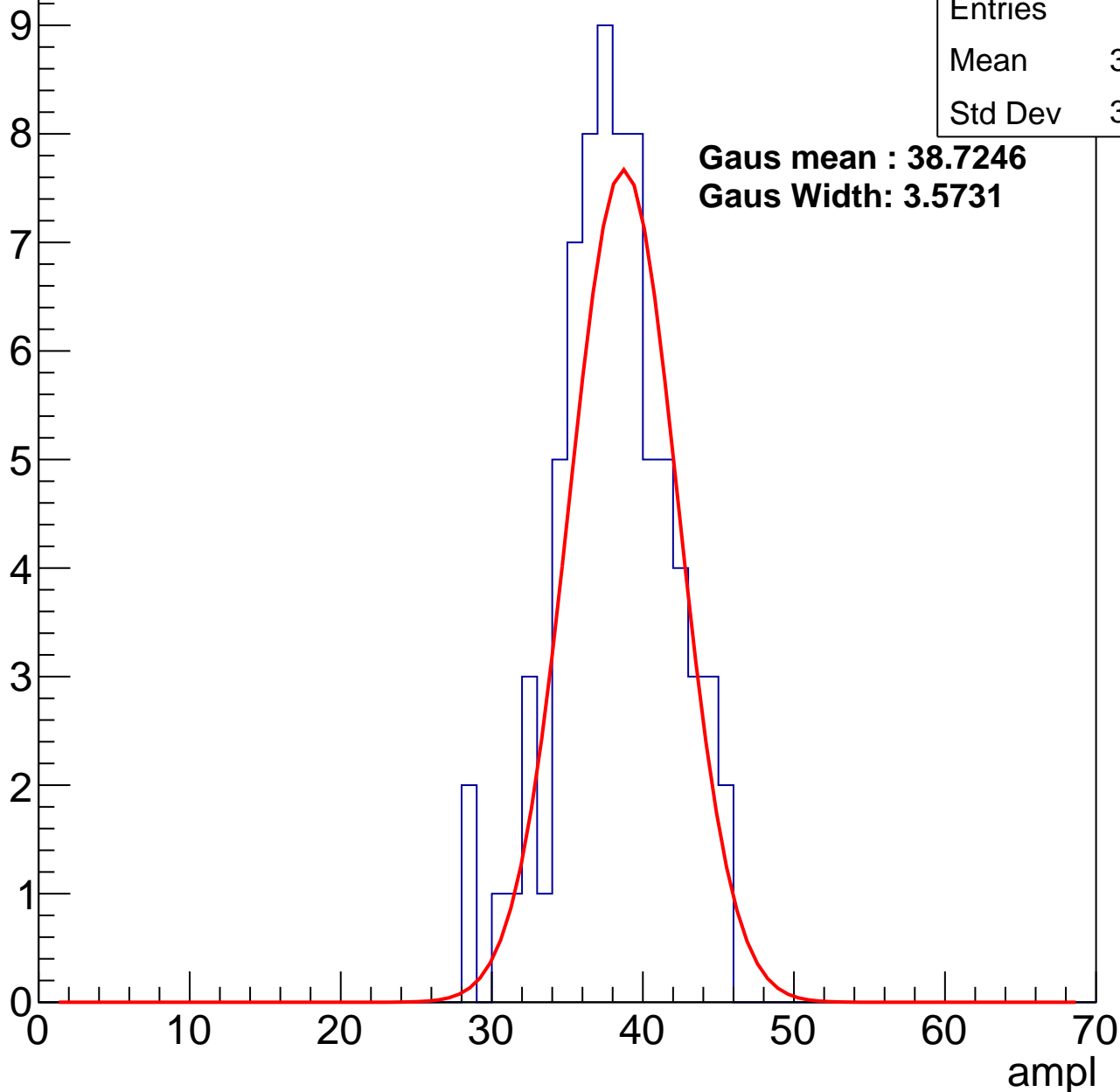
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	75
Mean	37.63
Std Dev	3.719

**Gaus mean : 38.7246**

**Gaus Width: 3.5731**



# B0L002S, U2-ch93, adc2

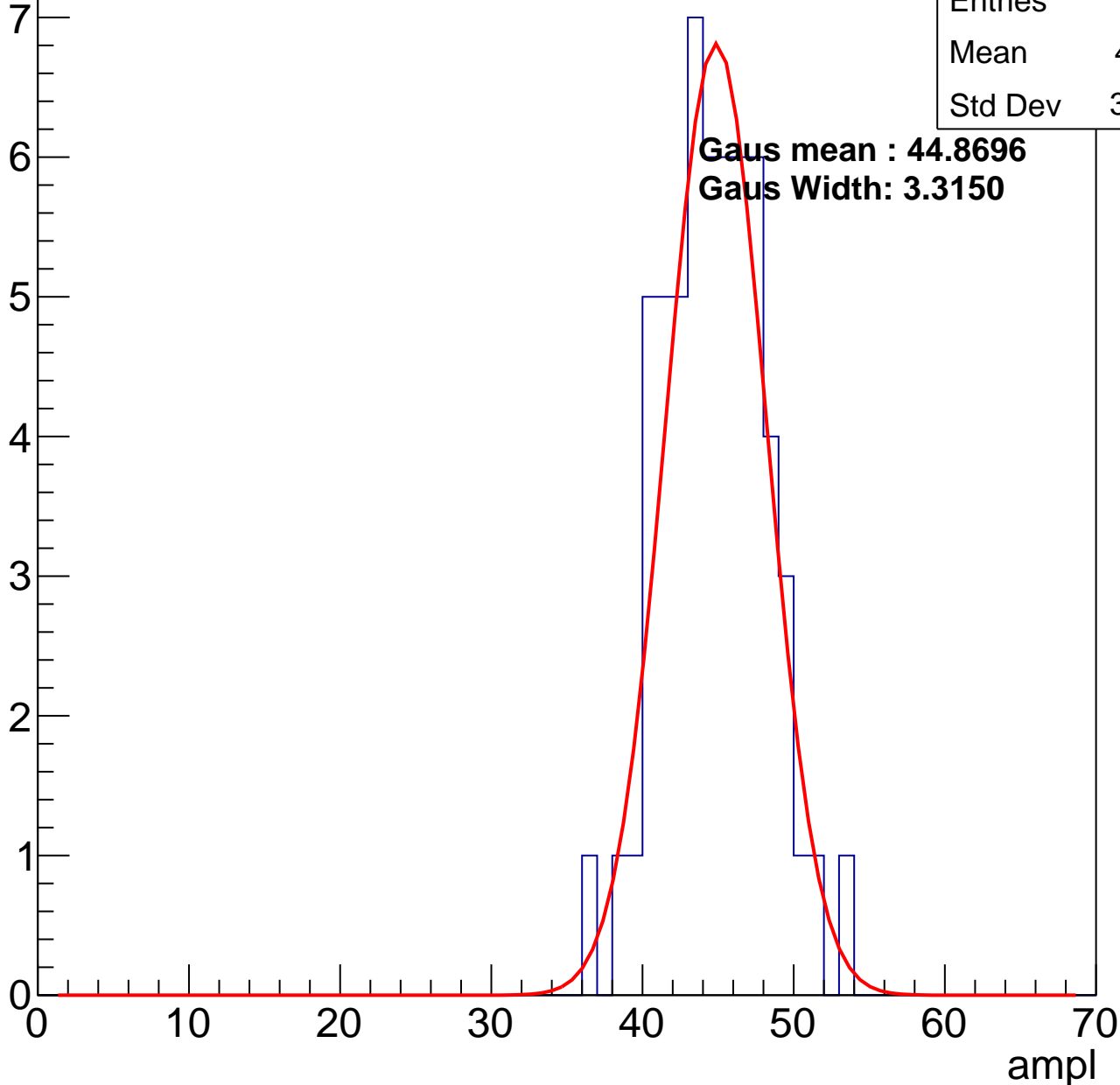
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	59
Mean	44.31
Std Dev	3.346

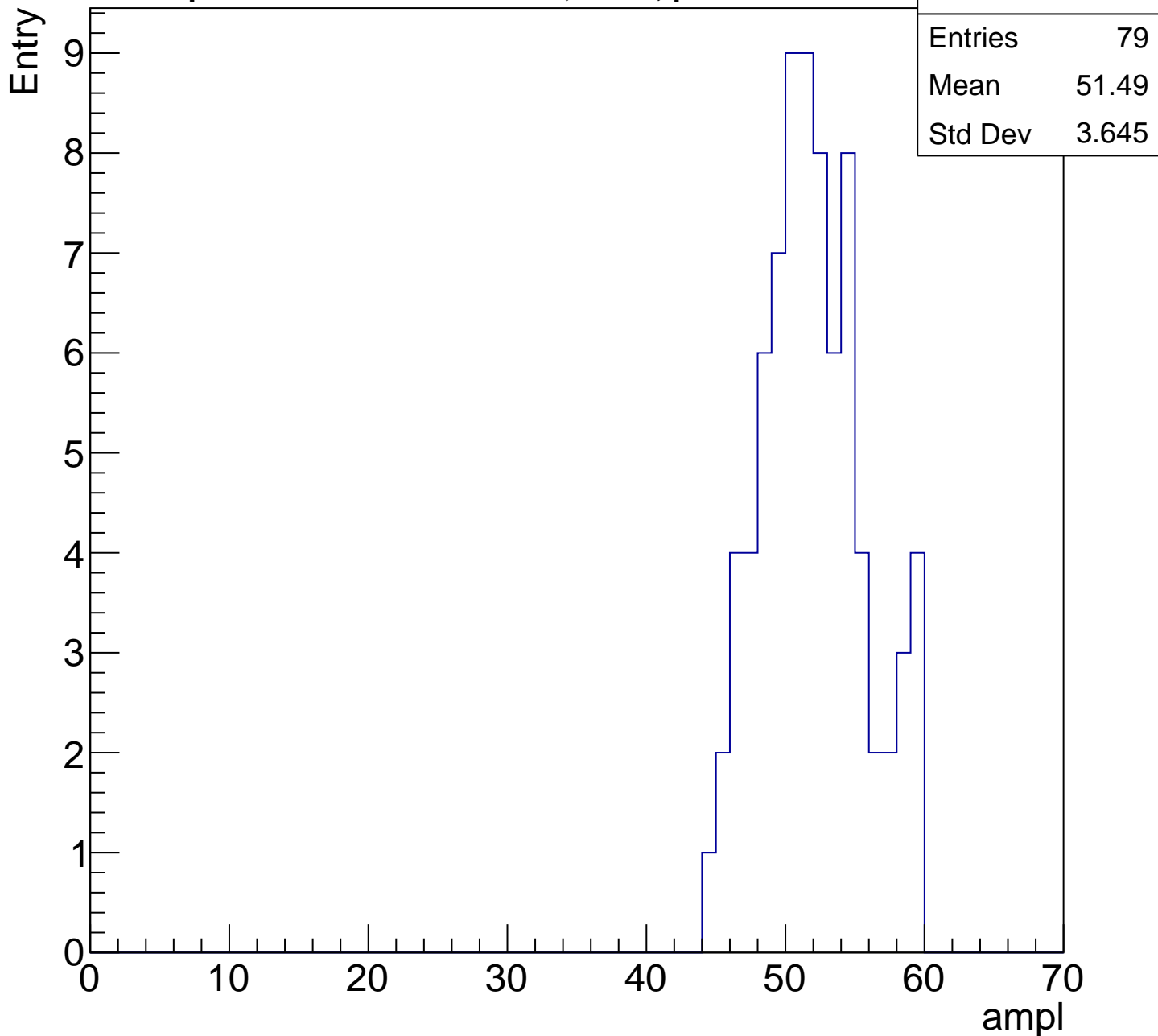
**Gaus mean : 44.8696**

**Gaus Width: 3.3150**



# B0L002S, U2-ch93, adc3

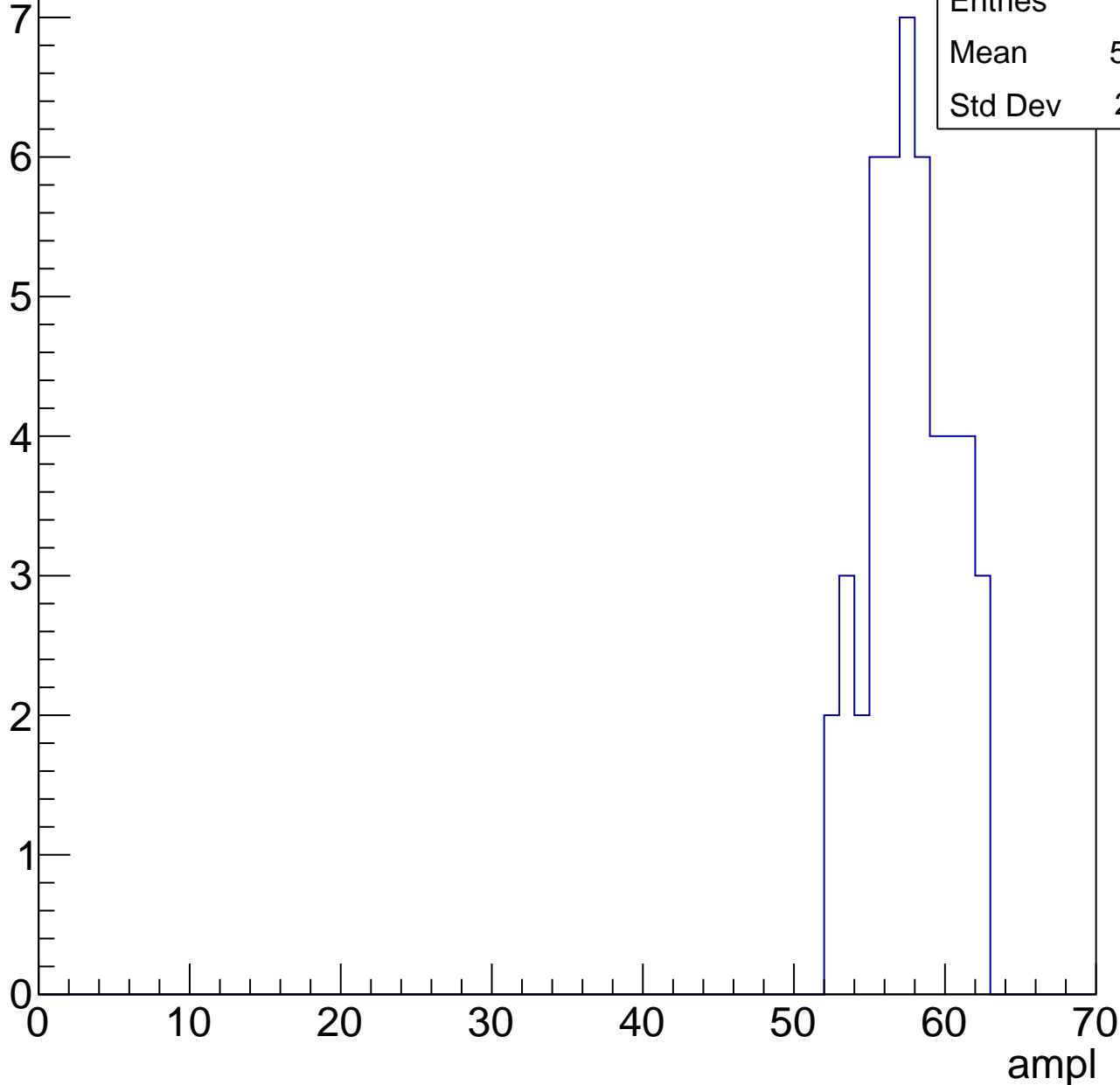
calib\_packv5\_042523\_0143.root, FC#8, port C1



# B0L002S, U2-ch93, adc4

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



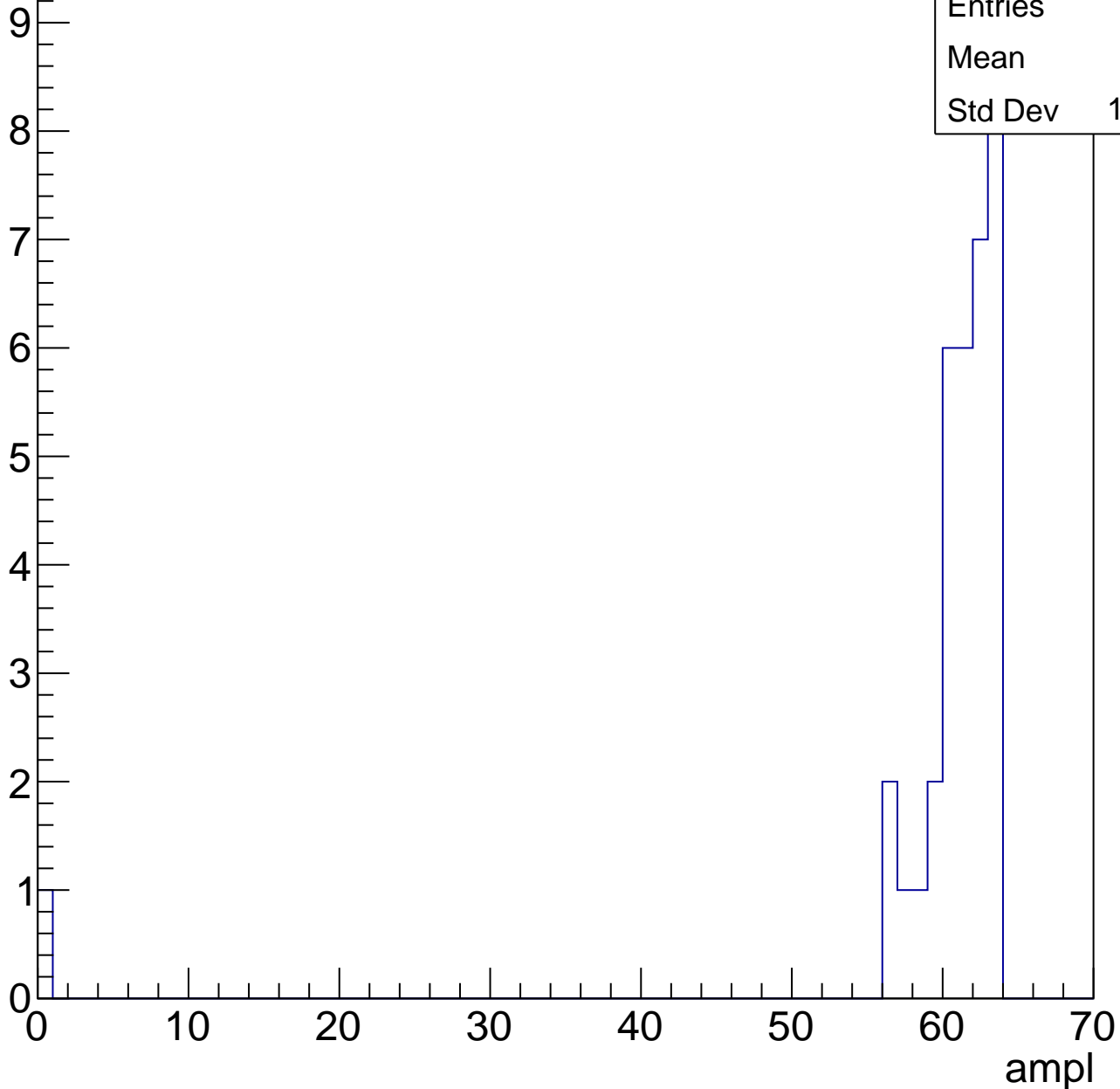
Entries	47
Mean	57.23
Std Dev	2.691

# B0L002S, U2-ch93, adc5

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	35
Mean	59.2
Std Dev	10.34



# B0L002S, U2-ch93, adc6

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry





# B0L002S, U2-ch93, adc7

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



# B0L002S, U2-ch94, adc0

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entries	48
Mean	30.98
Std Dev	2.712

**Gaus mean : 31.3568**

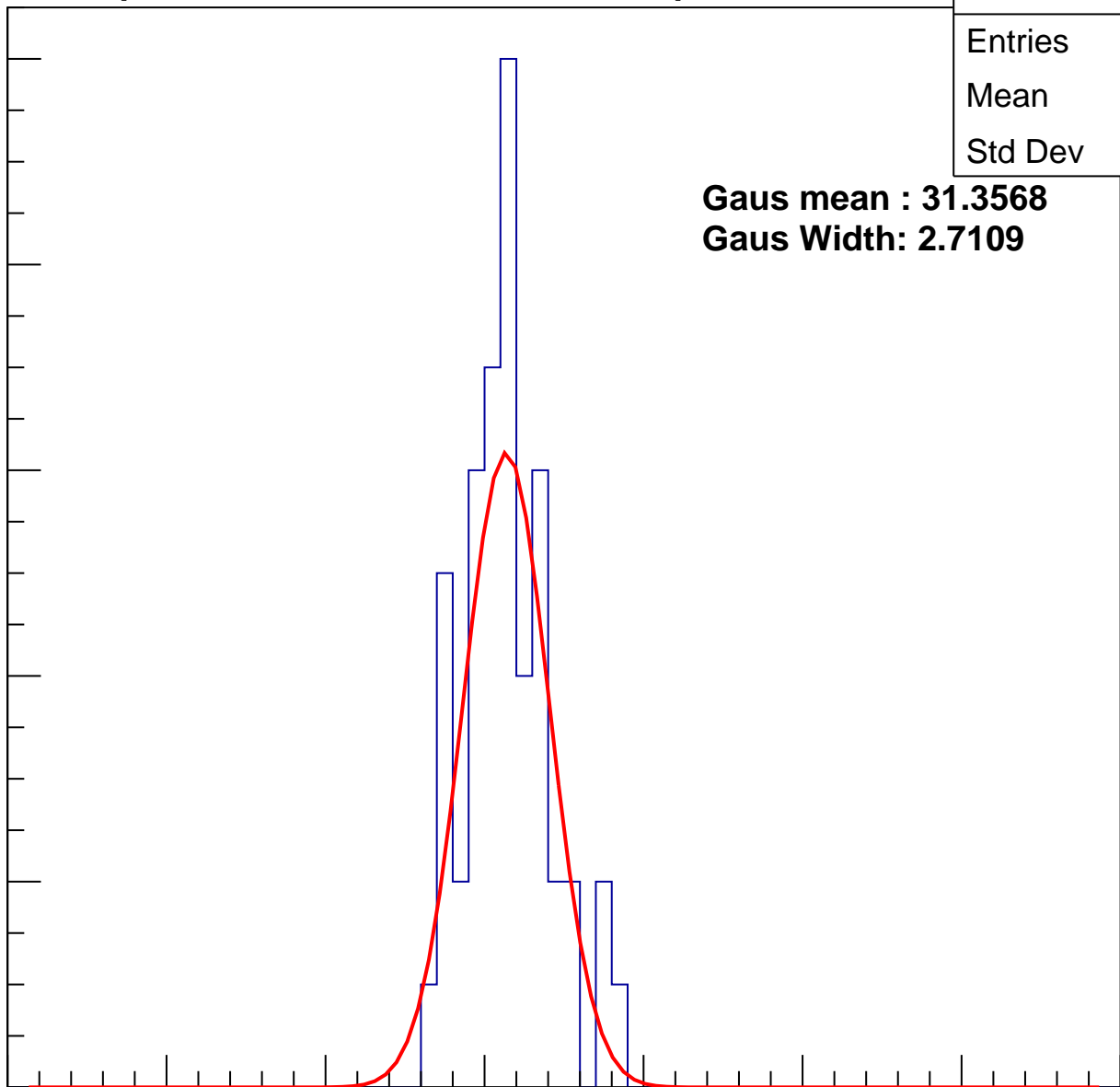
**Gaus Width: 2.7109**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L002S, U2-ch94, adc1

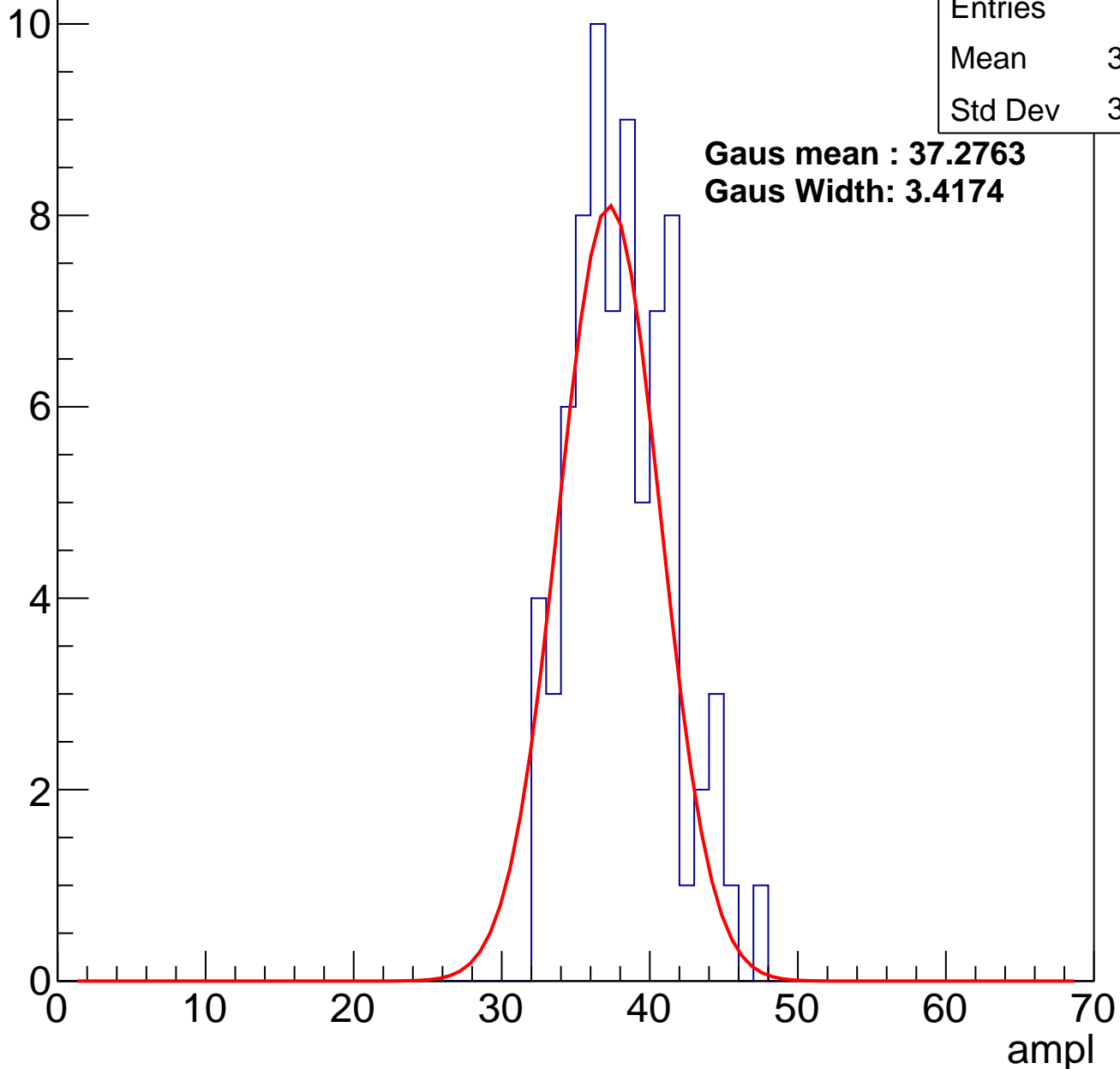
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entries	75
Mean	37.69
Std Dev	3.339

**Gaus mean : 37.2763**

**Gaus Width: 3.4174**

Entry



# B0L002S, U2-ch94, adc2

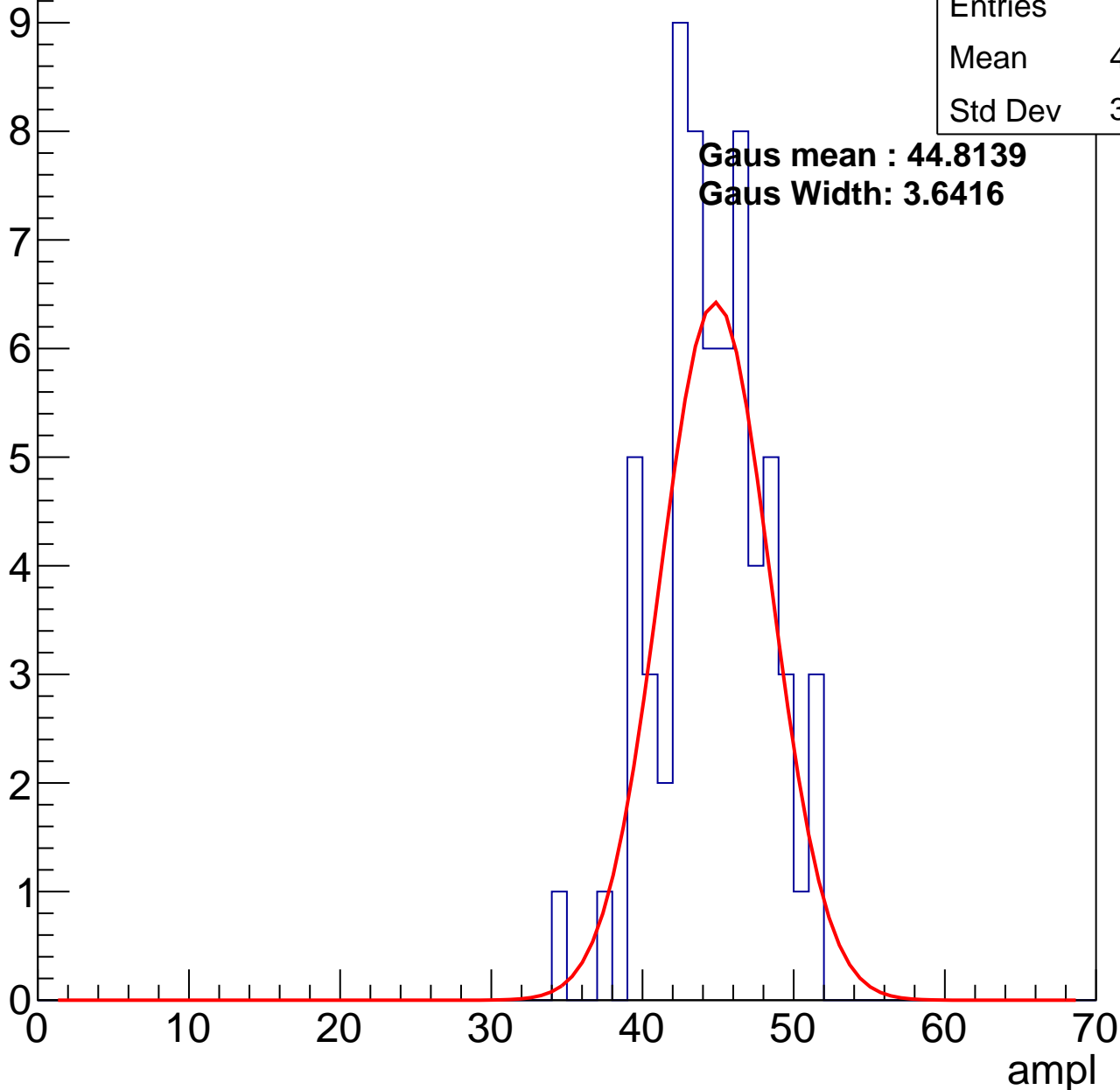
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	65
Mean	44.15
Std Dev	3.496

**Gaus mean : 44.8139**

**Gaus Width: 3.6416**

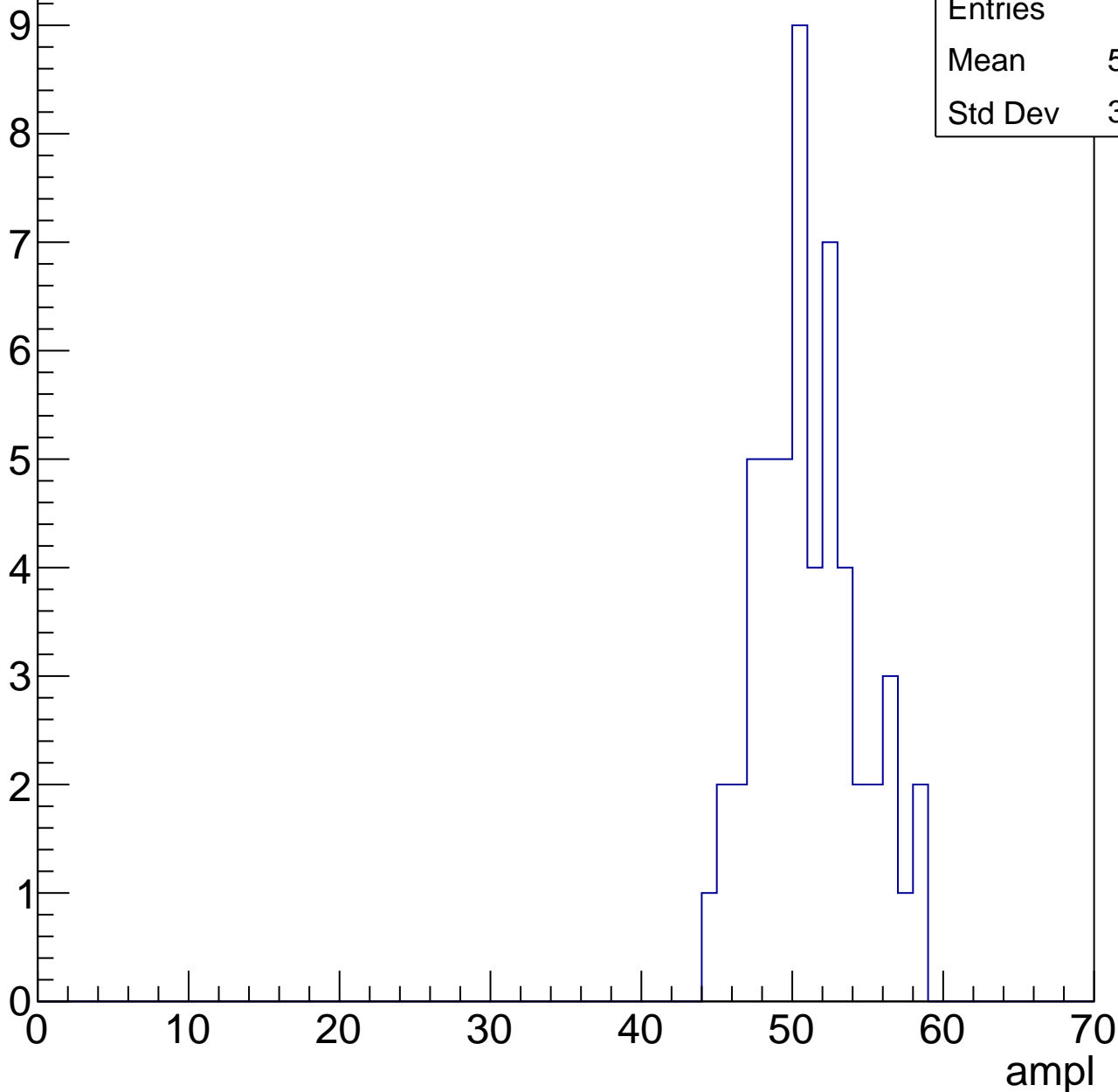


# B0L002S, U2-ch94, adc3

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	54
Mean	50.65
Std Dev	3.334

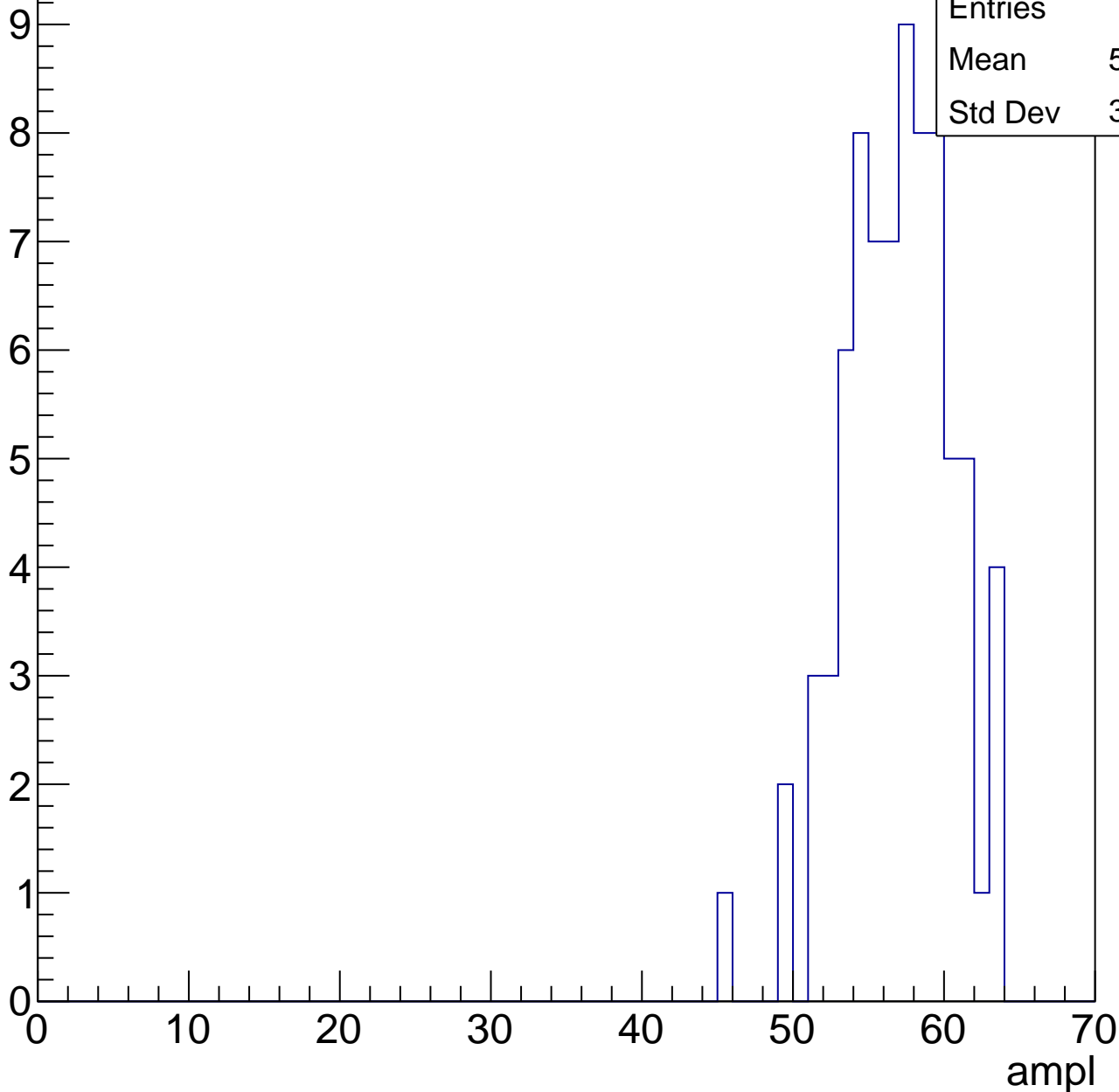


# B0L002S, U2-ch94, adc4

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	77
Mean	56.45
Std Dev	3.548

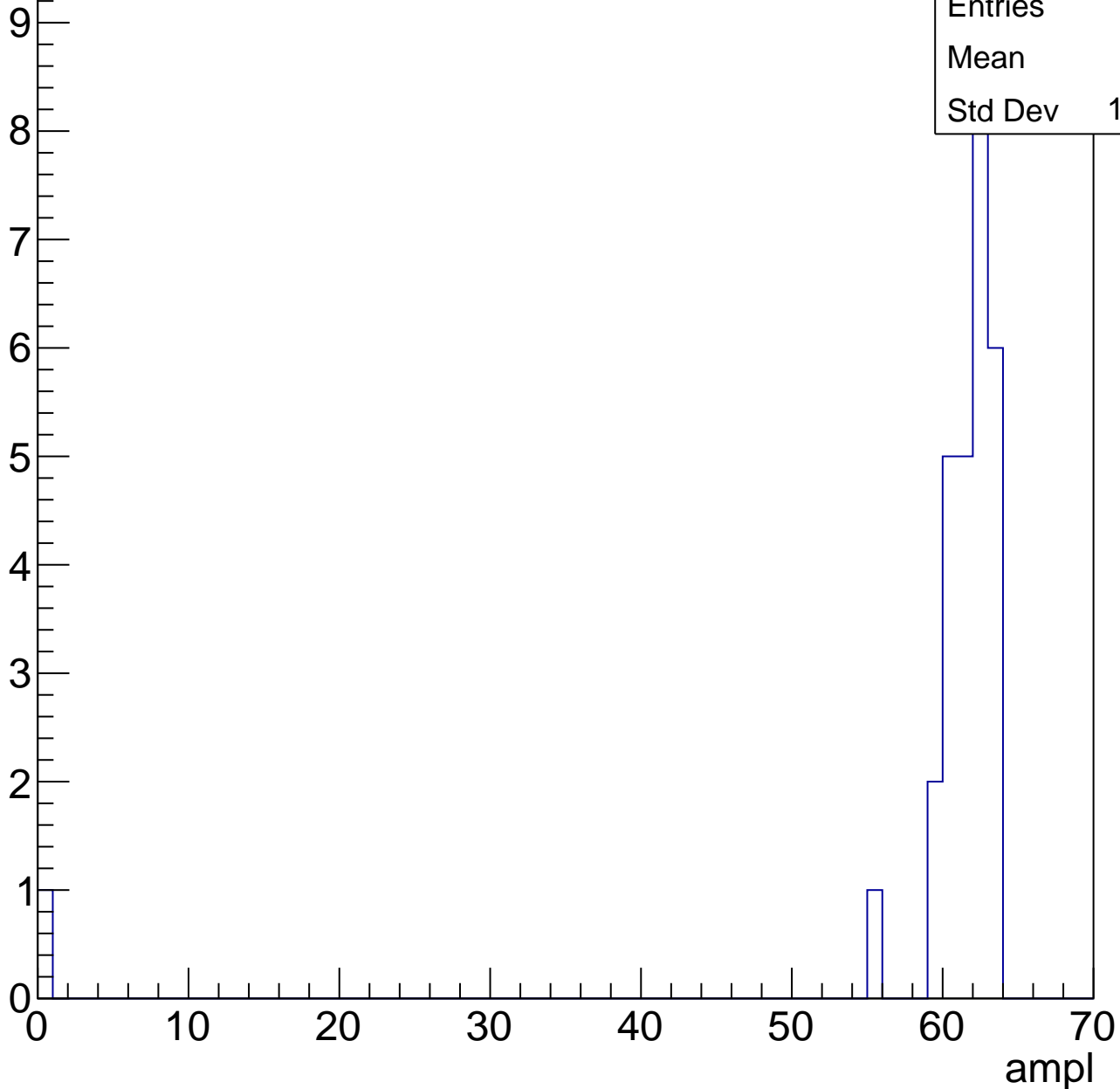


# B0L002S, U2-ch94, adc5

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	29
Mean	59.1
Std Dev	11.29



# B0L002S, U2-ch94, adc6

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



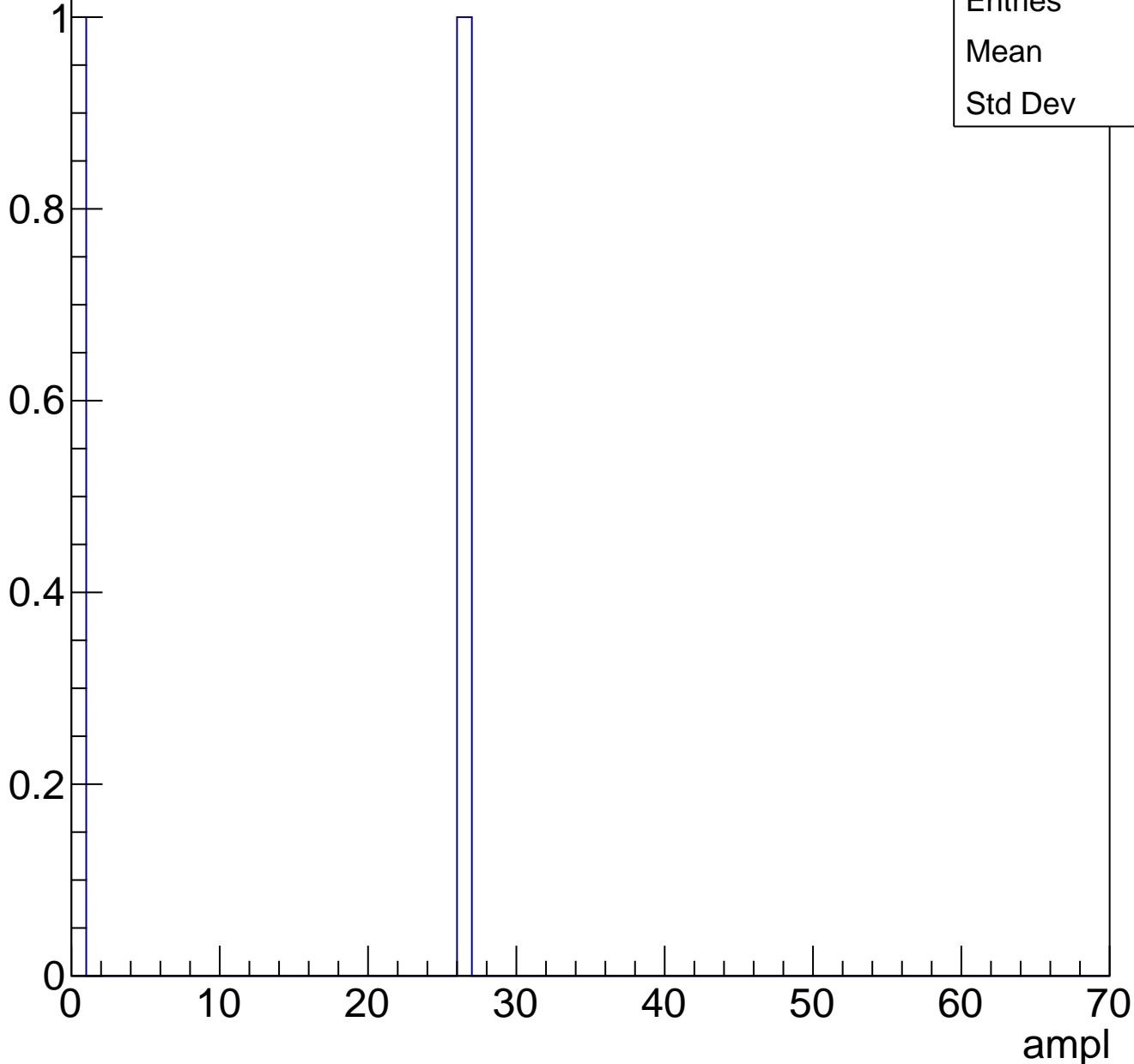
Entries	0
Mean	0
Std Dev	0



# B0L002S, U2-ch94, adc7

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



Entries	2
Mean	13
Std Dev	13

# B0L002S, U2-ch95, adc0

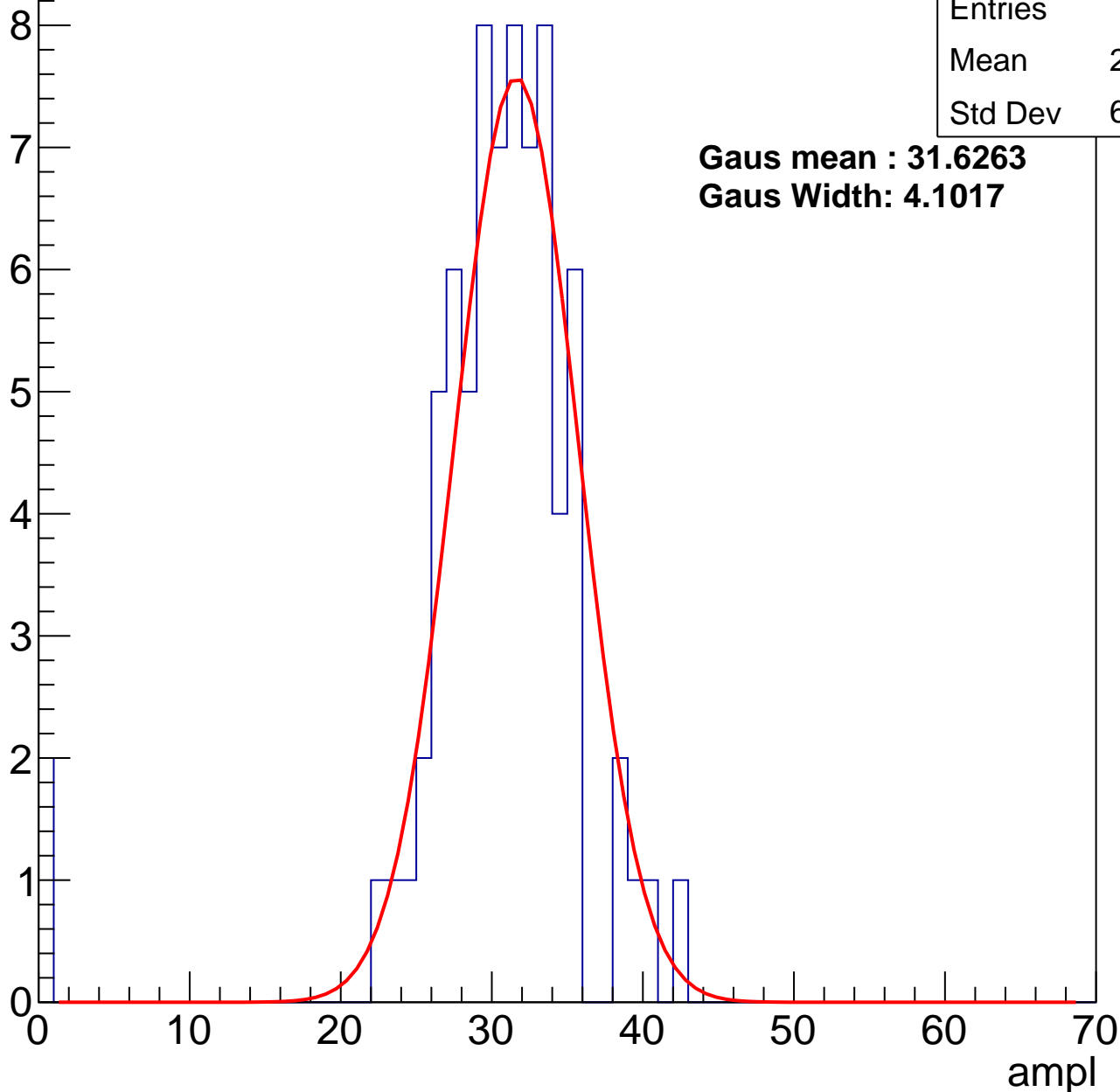
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	76
Mean	29.89
Std Dev	6.215

**Gaus mean : 31.6263**

**Gaus Width: 4.1017**



# B0L002S, U2-ch95, adc1

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entries	68
Mean	37.04
Std Dev	3.367

**Gaus mean : 37.9112**

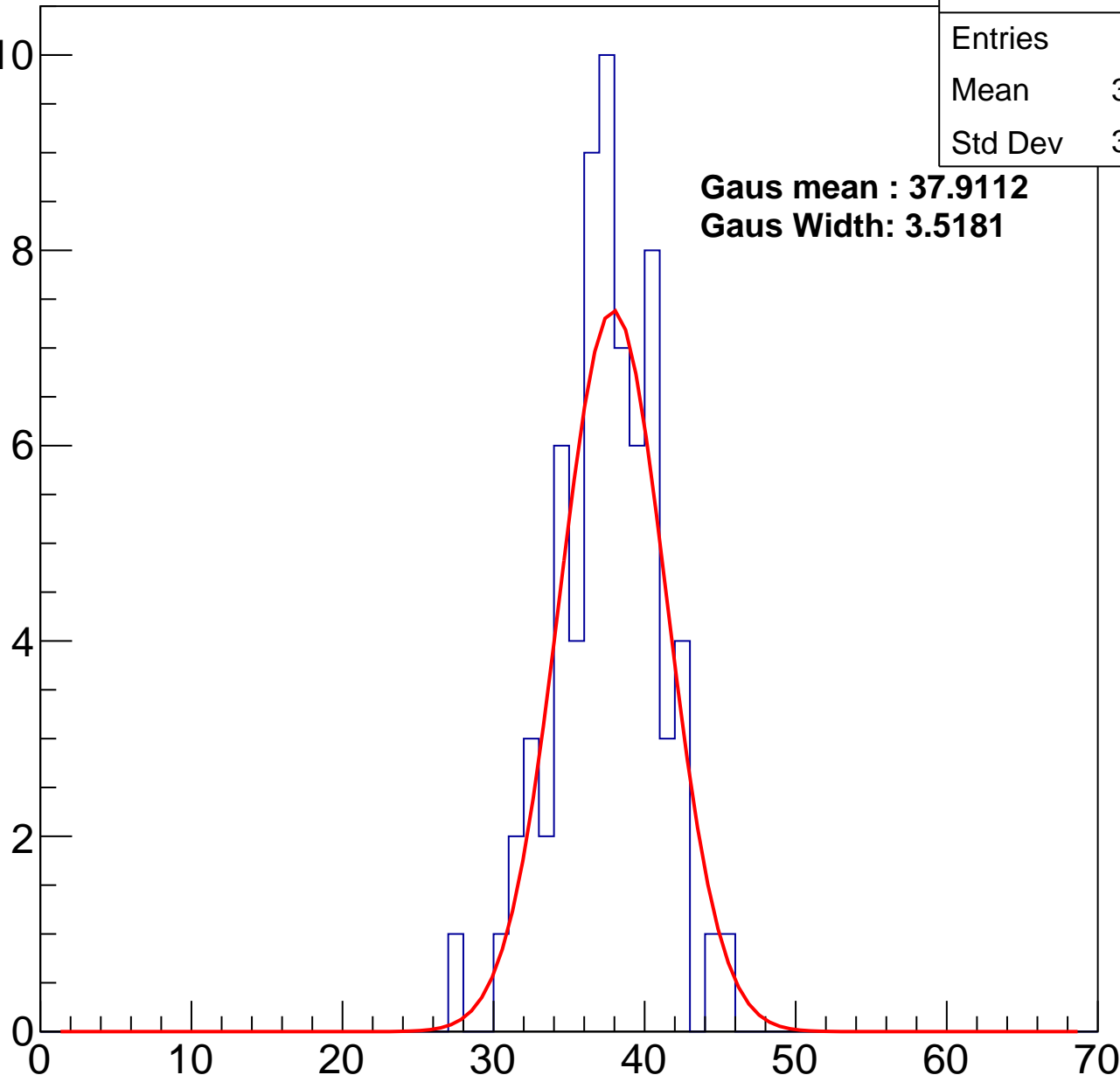
**Gaus Width: 3.5181**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B0L002S, U2-ch95, adc2

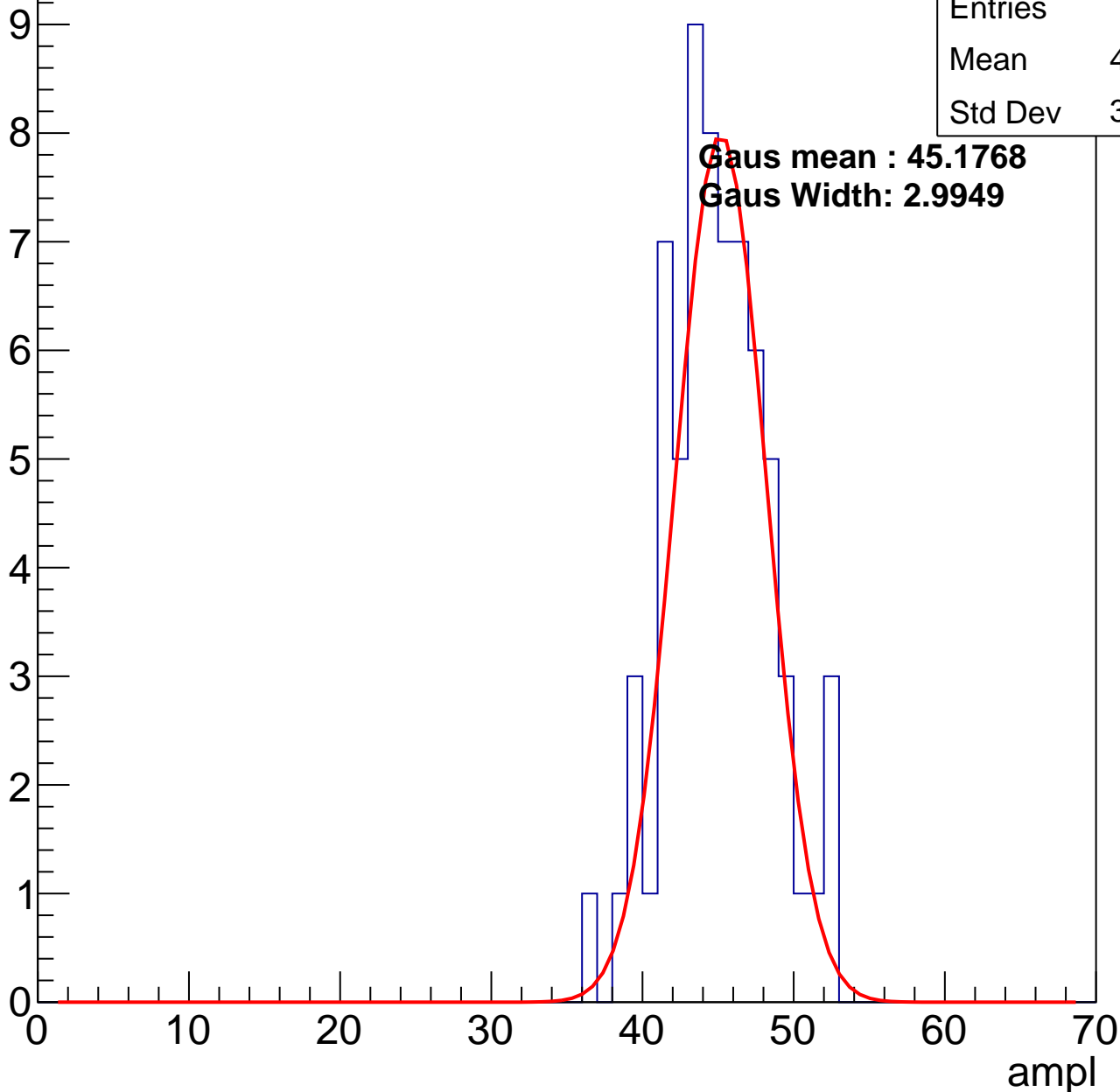
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	68
Mean	44.56
Std Dev	3.393

**Gaus mean : 45.1768**

**Gaus Width: 2.9949**

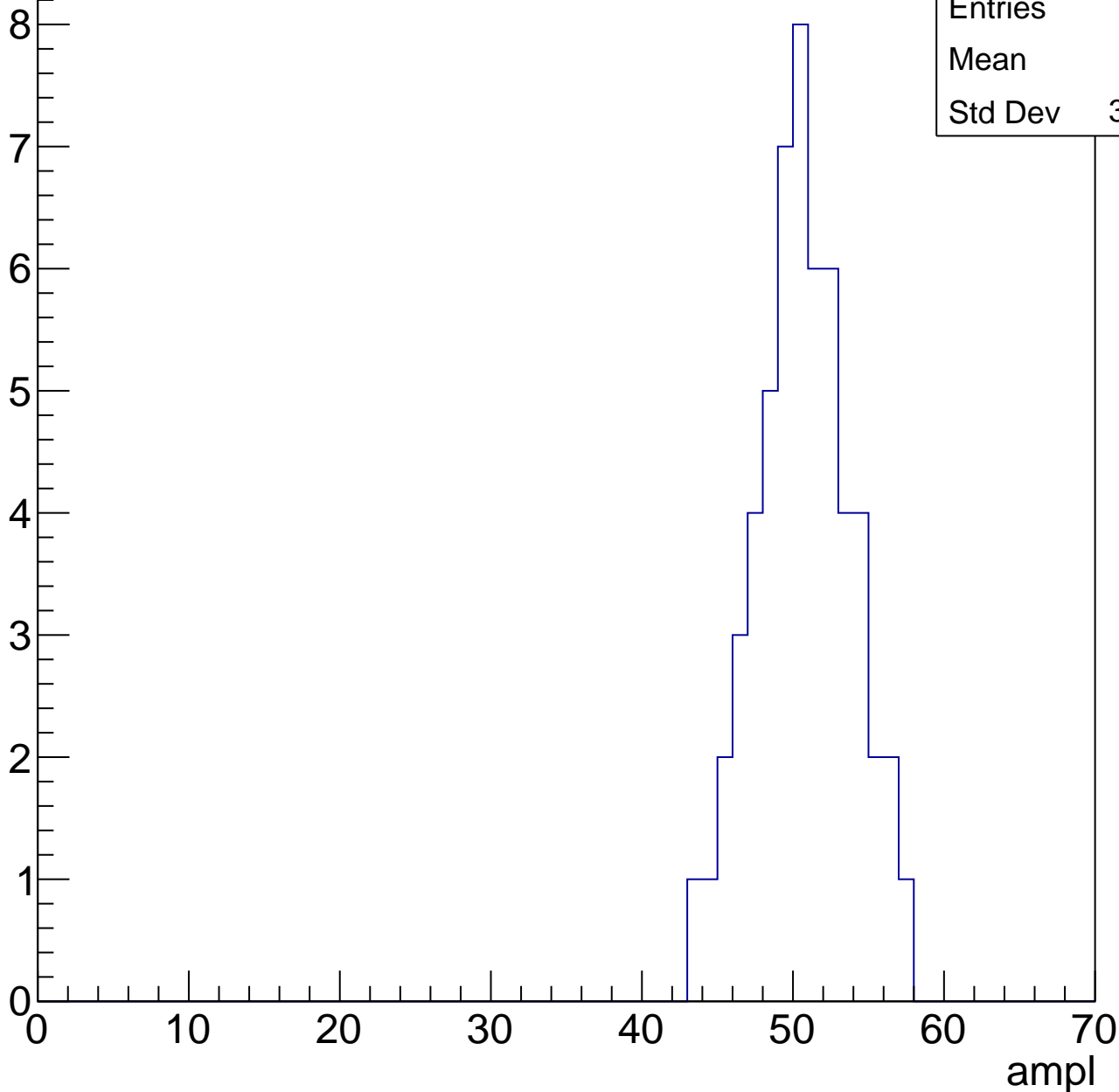


# B0L002S, U2-ch95, adc3

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

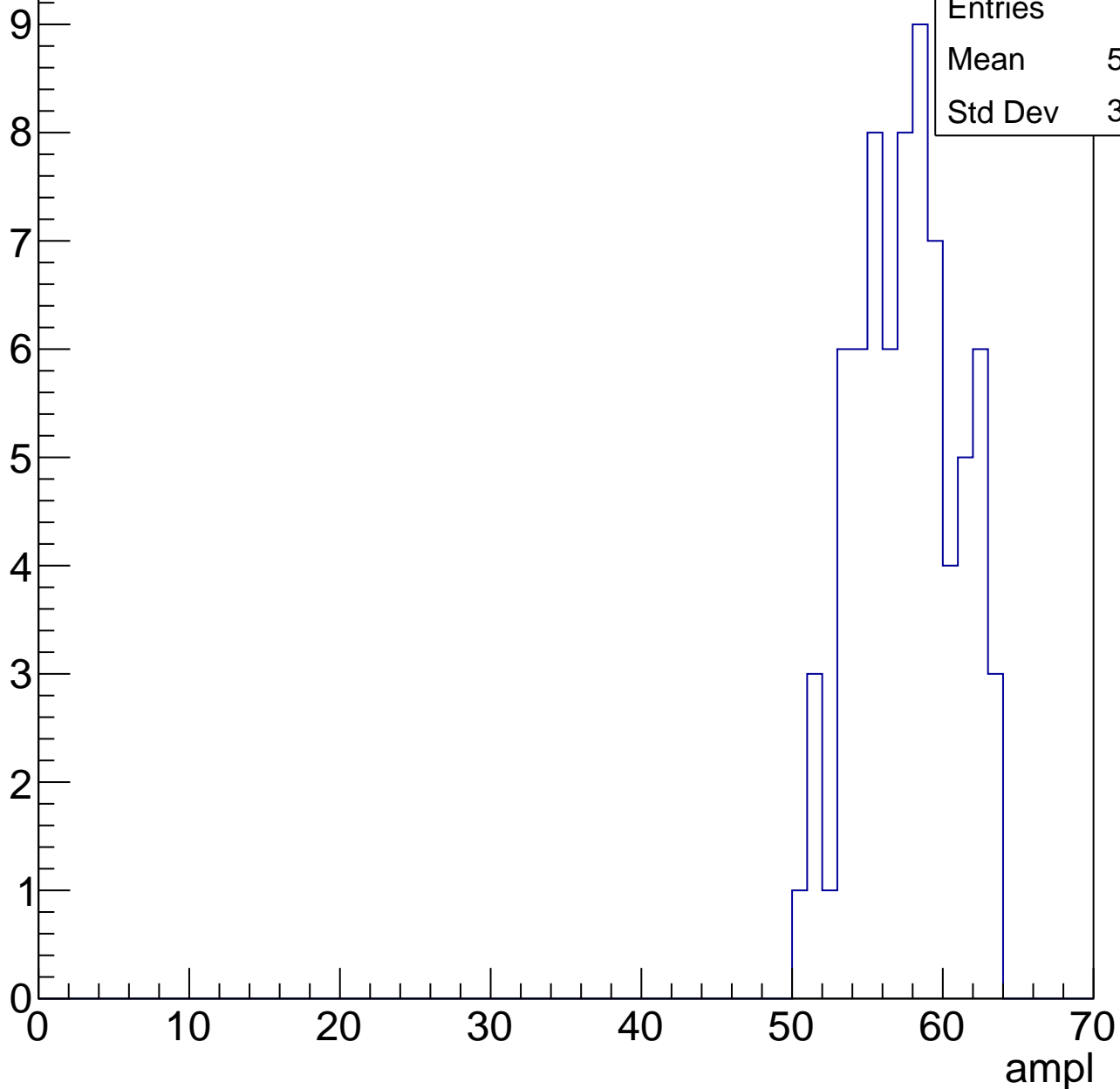
Entries	56
Mean	50.2
Std Dev	3.119



# B0L002S, U2-ch95, adc4

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

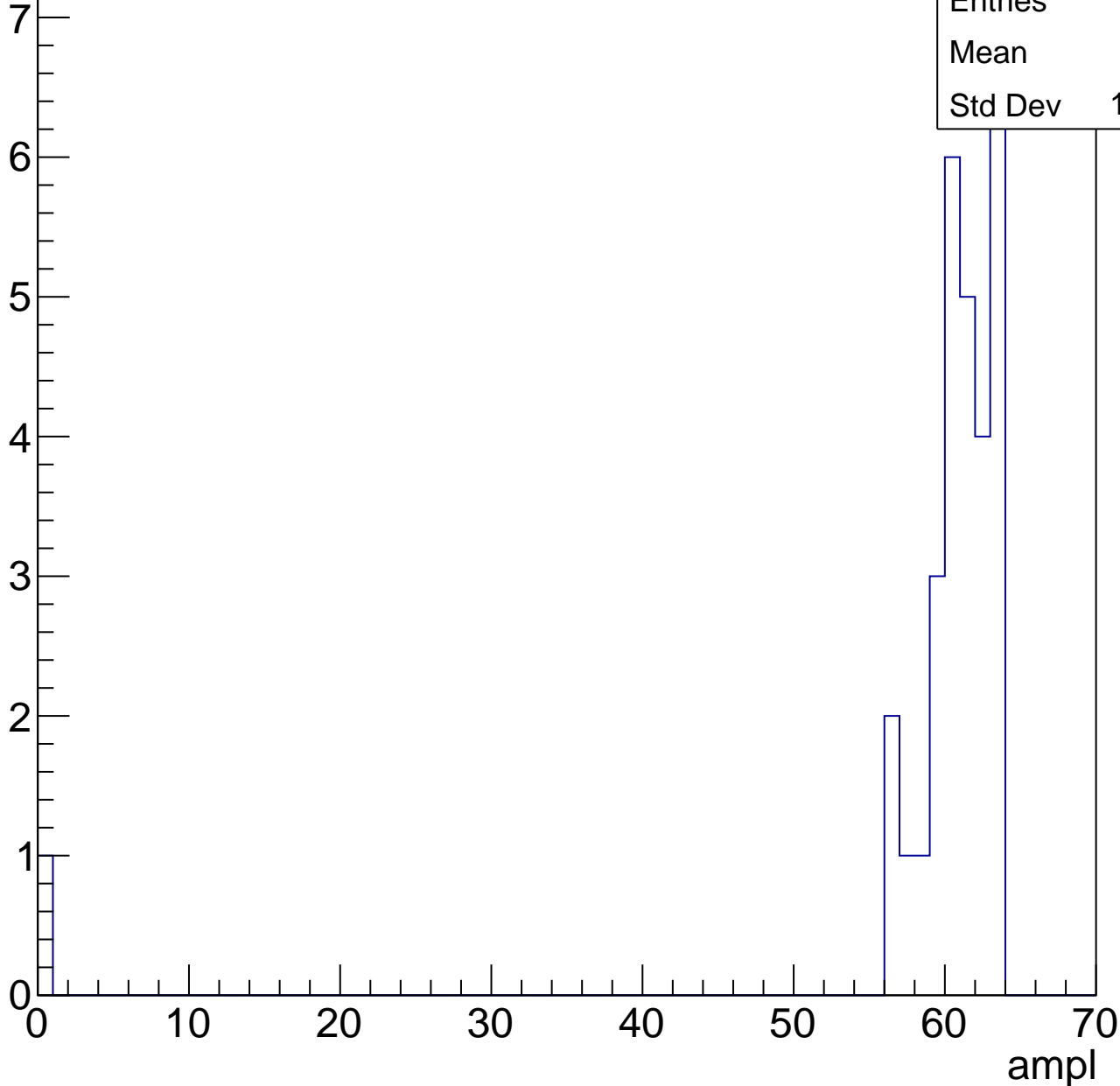


# B0L002S, U2-ch95, adc5

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	30
Mean	58.6
Std Dev	11.07



# B0L002S, U2-ch95, adc6

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



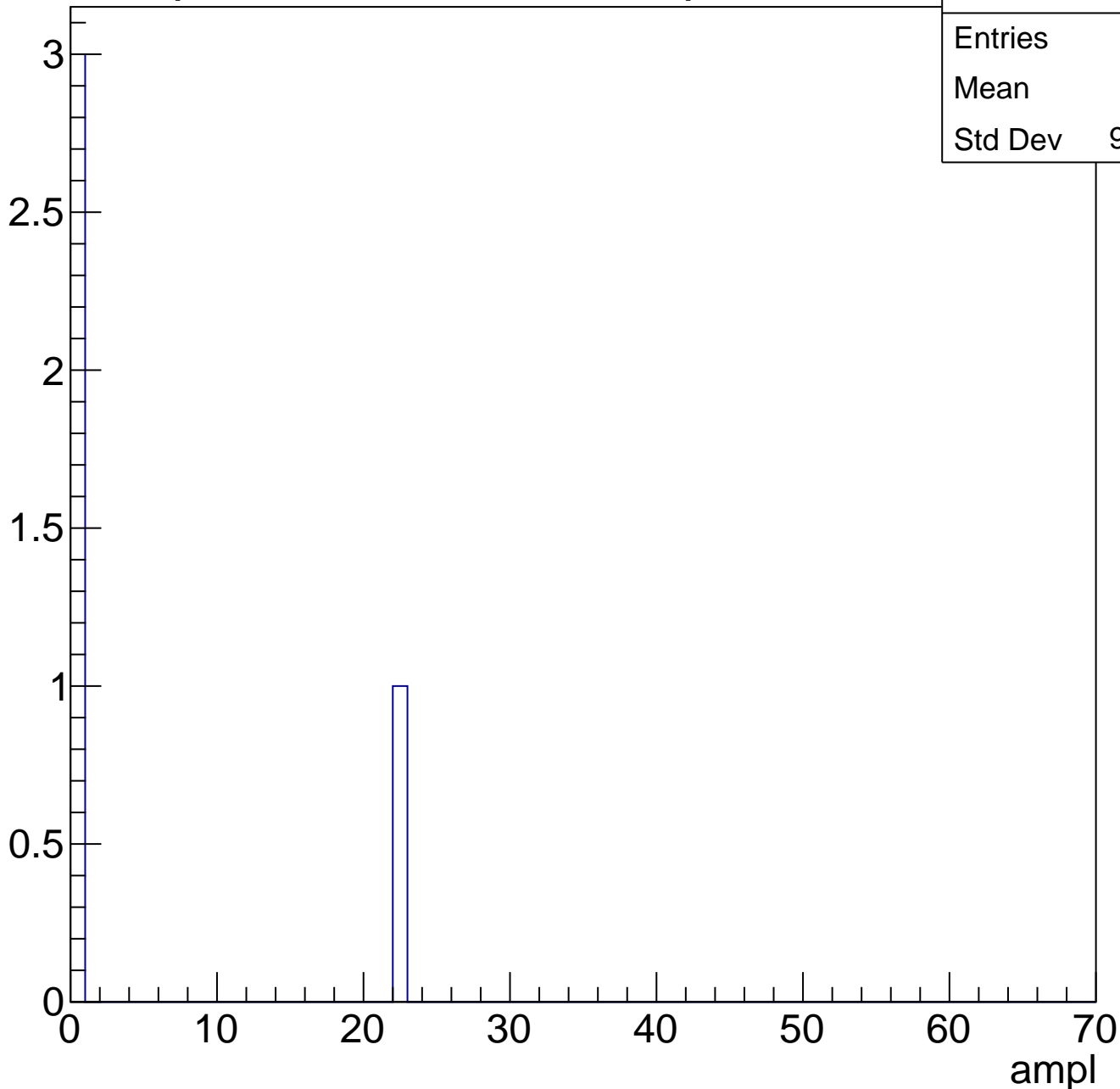
Entries	0
Mean	0
Std Dev	0



# B0L002S, U2-ch95, adc7

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



Entries	4
Mean	5.5
Std Dev	9.526

# B0L002S, U2-ch96, adc0

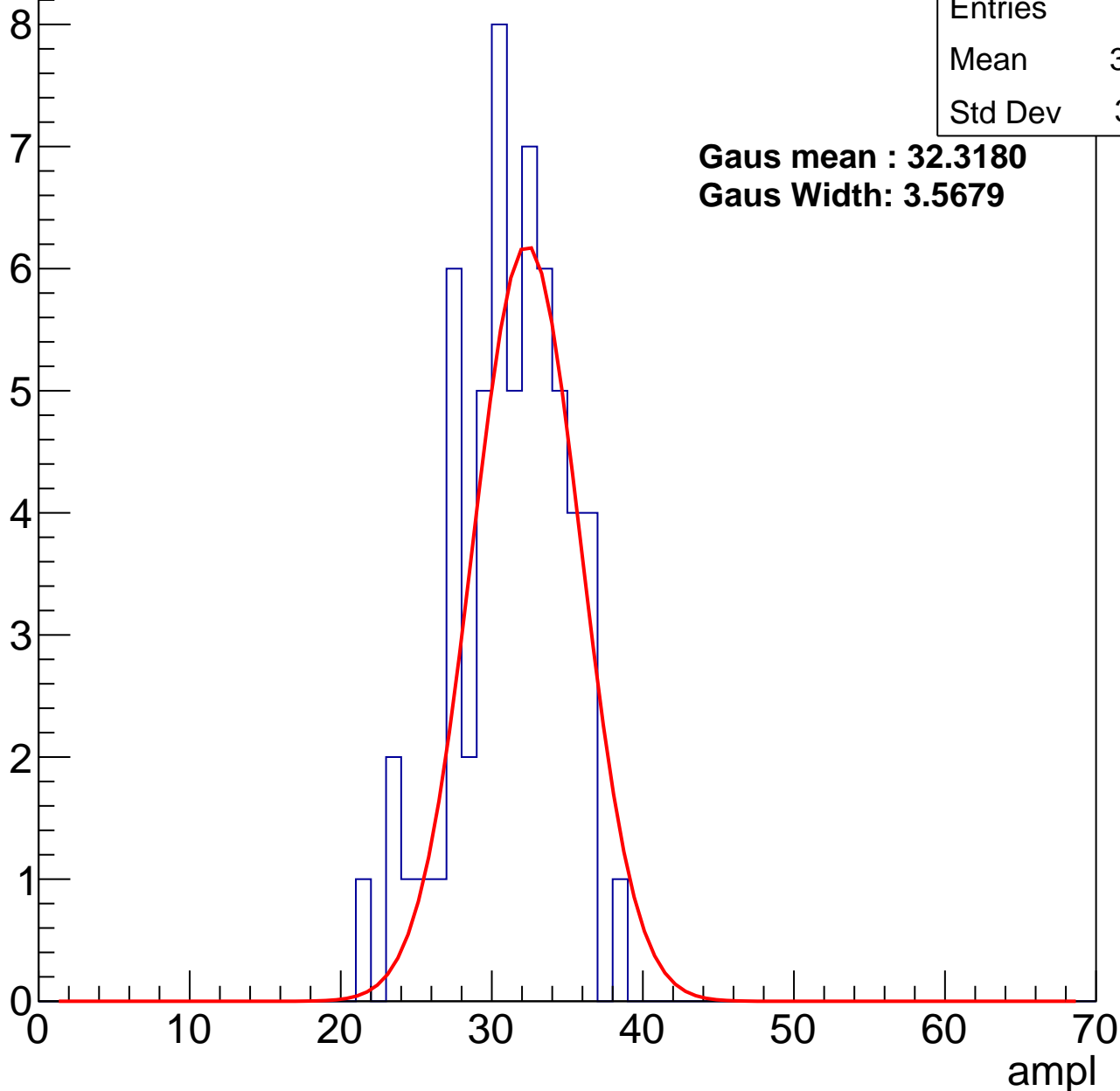
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	59
Mean	30.75
Std Dev	3.601

**Gaus mean : 32.3180**

**Gaus Width: 3.5679**



# B0L002S, U2-ch96, adc1

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entries	54
Mean	36.48
Std Dev	2.955

**Gaus mean : 37.1524**

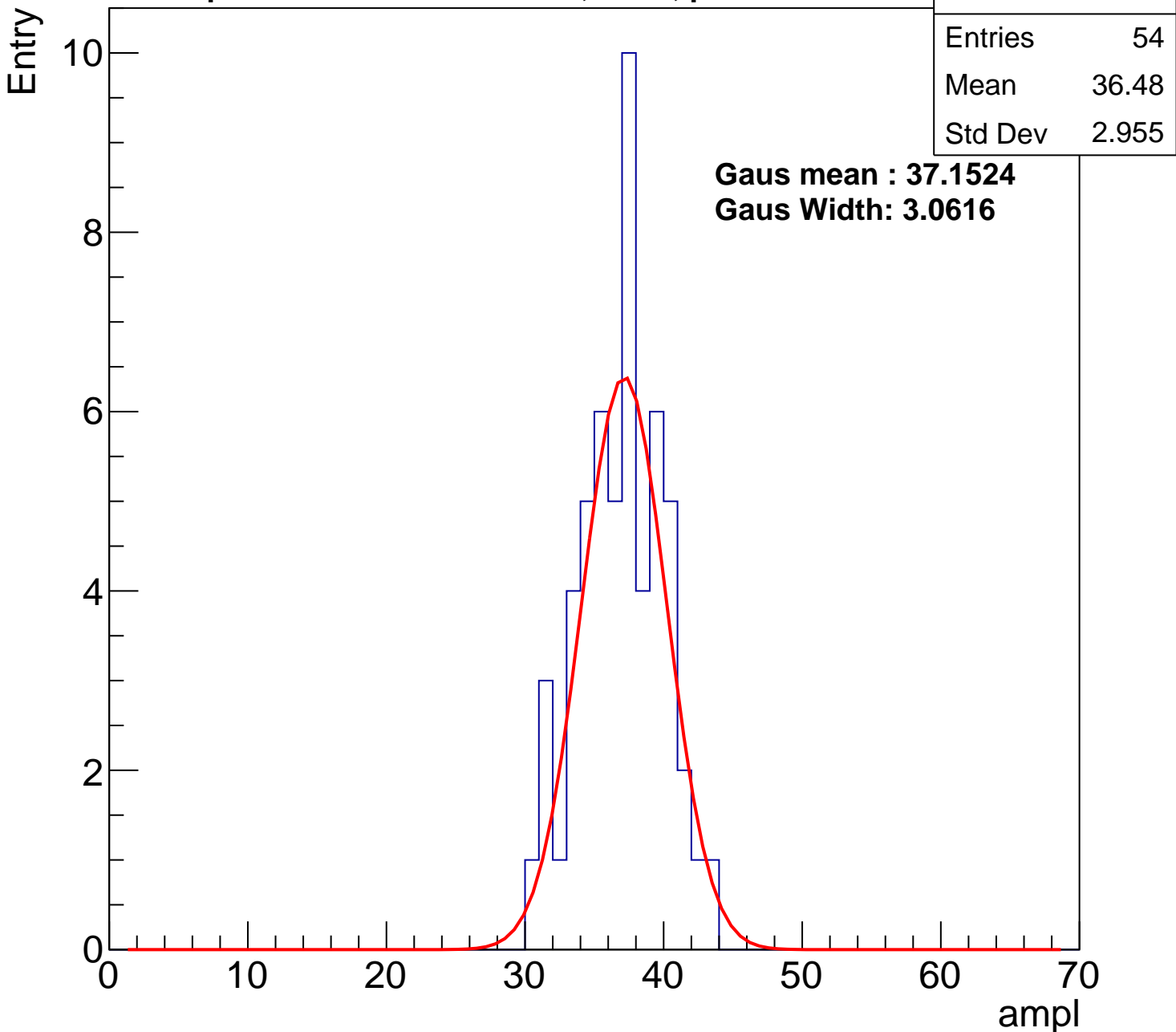
**Gaus Width: 3.0616**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L002S, U2-ch96, adc2

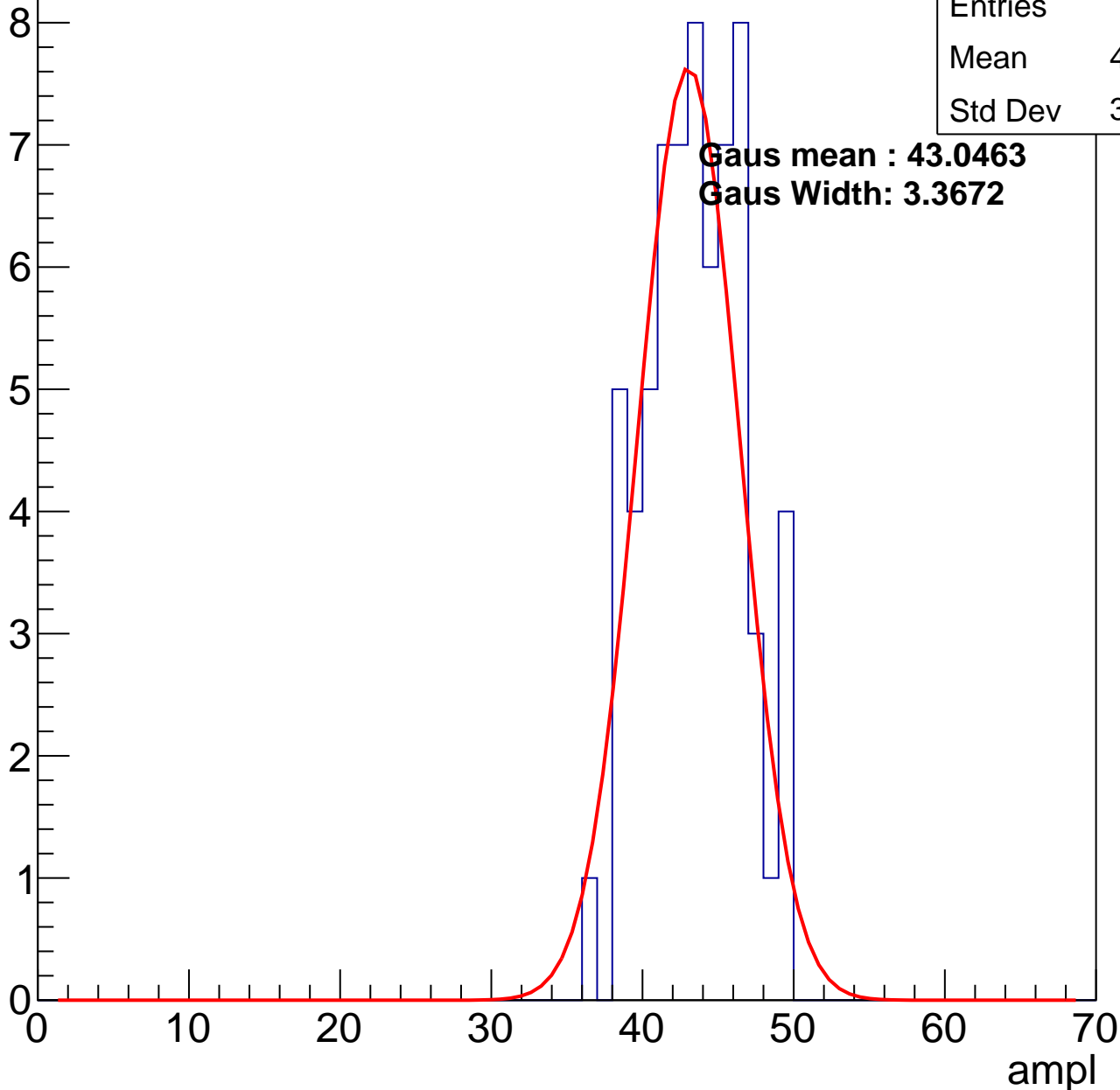
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	66
Mean	43.02
Std Dev	3.116

**Gaus mean : 43.0463**

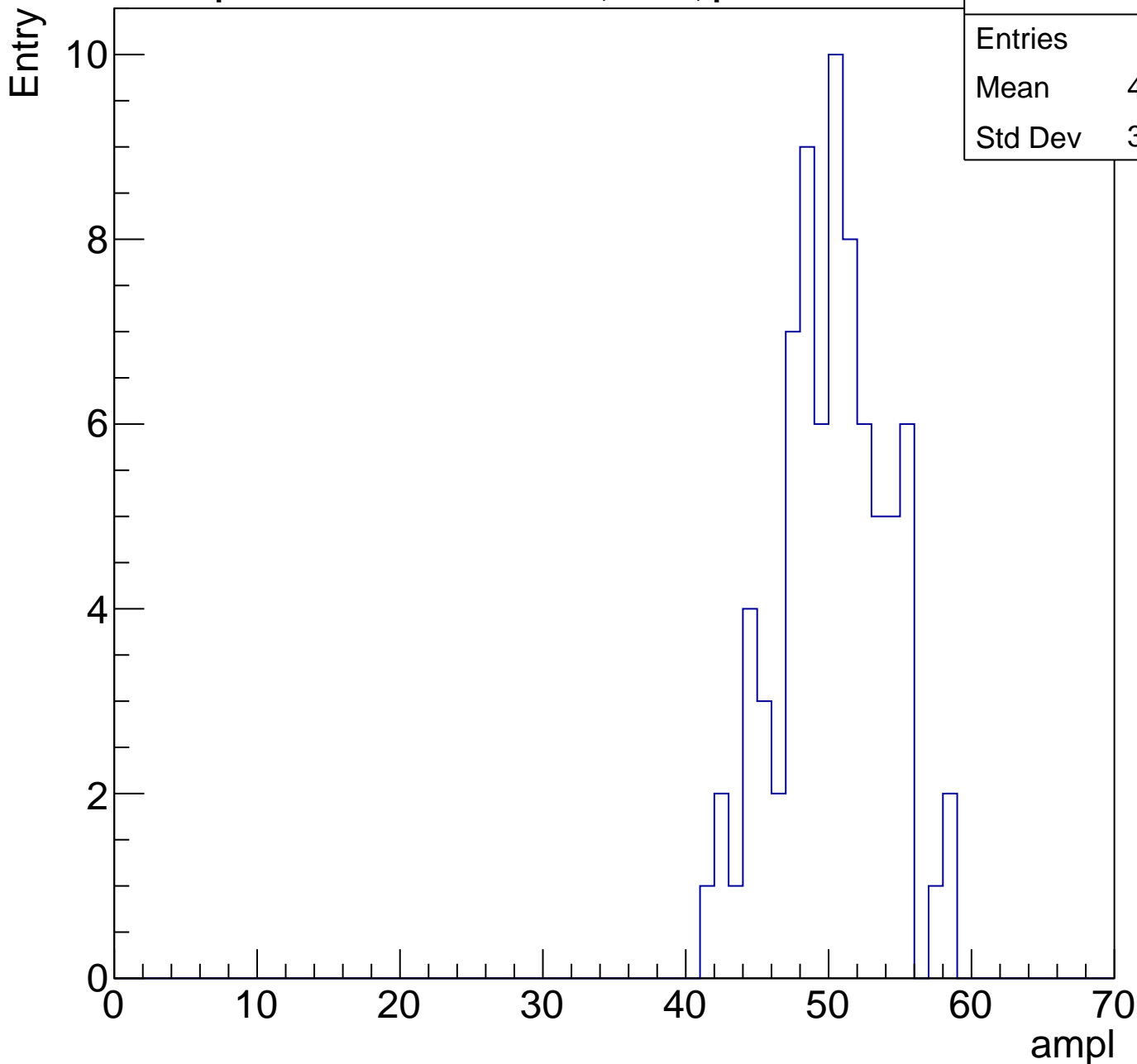
**Gaus Width: 3.3672**



# B0L002S, U2-ch96, adc3

calib\_packv5\_042523\_0143.root, FC#8, port C1

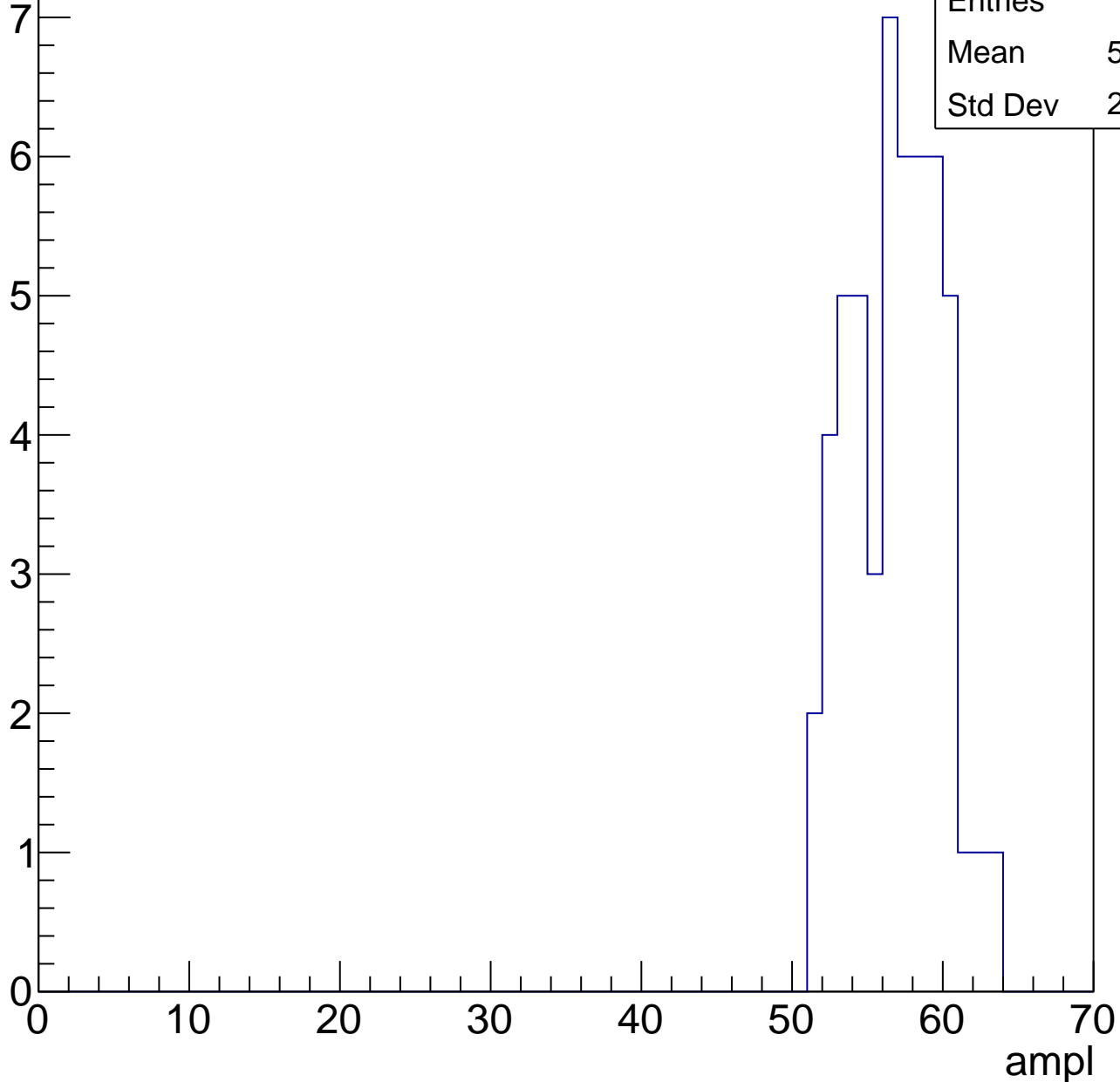
Entries	78
Mean	49.79
Std Dev	3.746



# B0L002S, U2-ch96, adc4

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



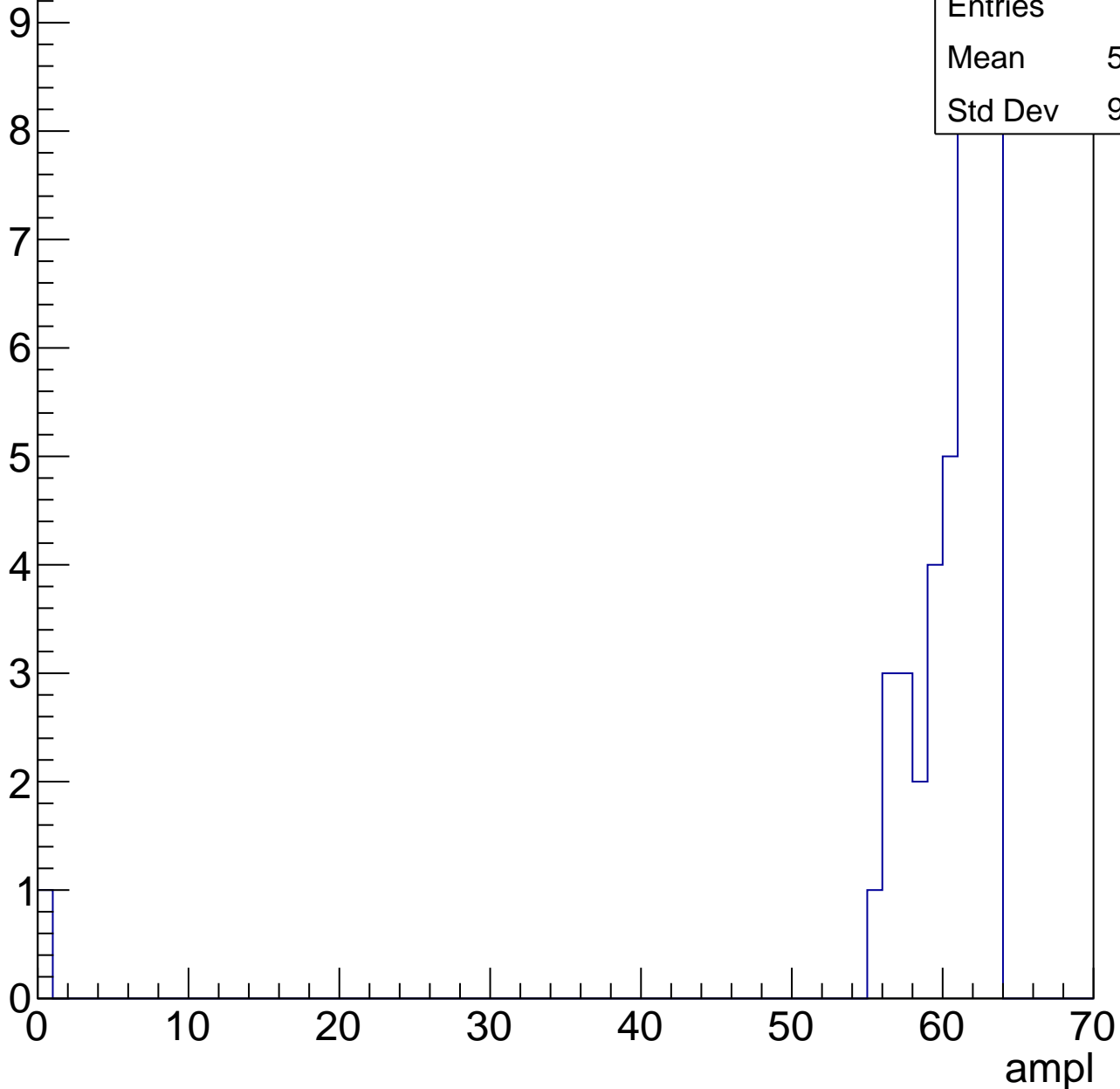
Entries	52
Mean	56.38
Std Dev	2.936

# B0L002S, U2-ch96, adc5

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	45
Mean	59.04
Std Dev	9.175



# B0L002S, U2-ch96, adc6

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry





# B0L002S, U2-ch96, adc7

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L002S, U2-ch97, adc0

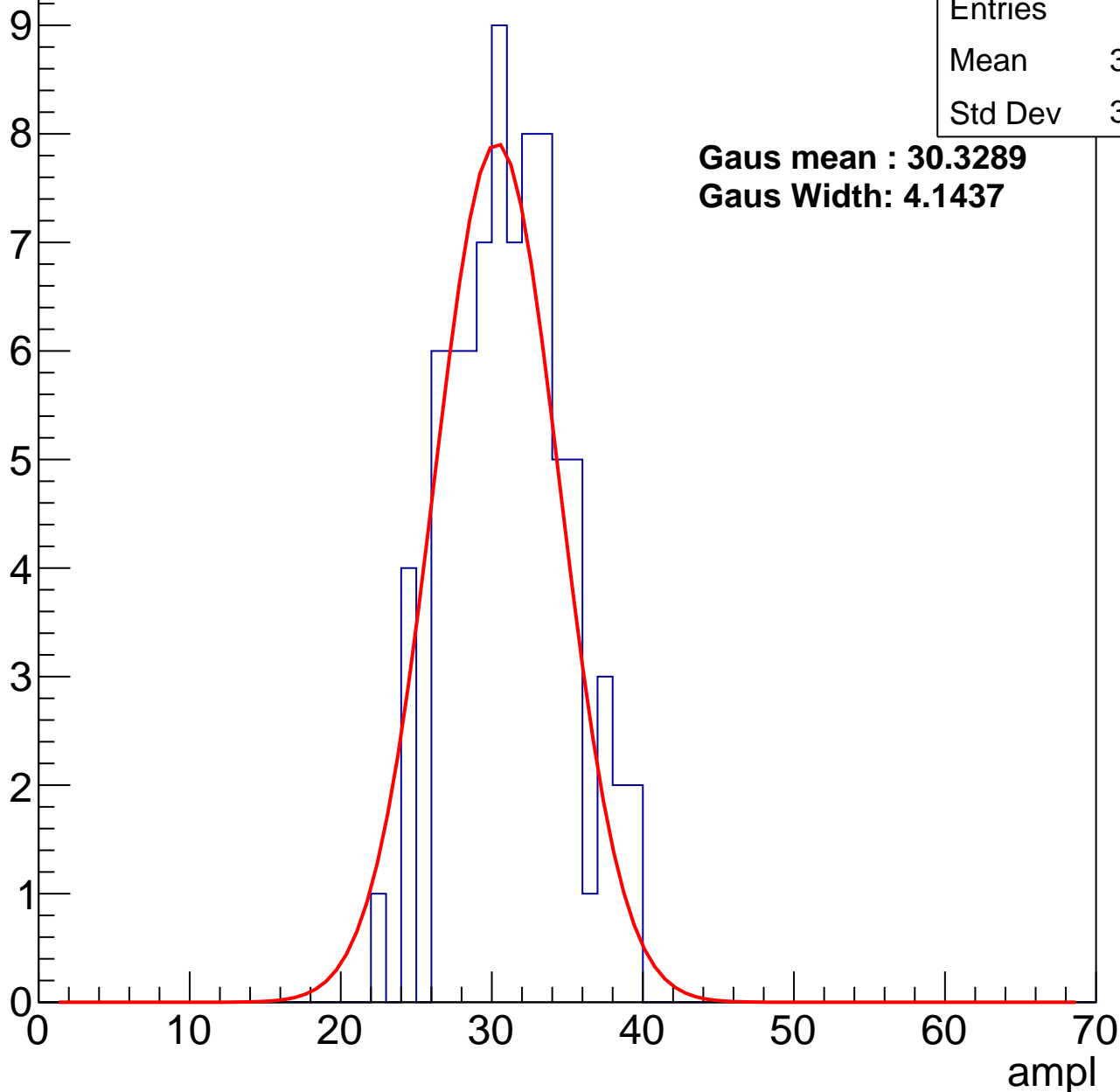
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	80
Mean	30.75
Std Dev	3.763

**Gaus mean : 30.3289**

**Gaus Width: 4.1437**



# B0L002S, U2-ch97, adc1

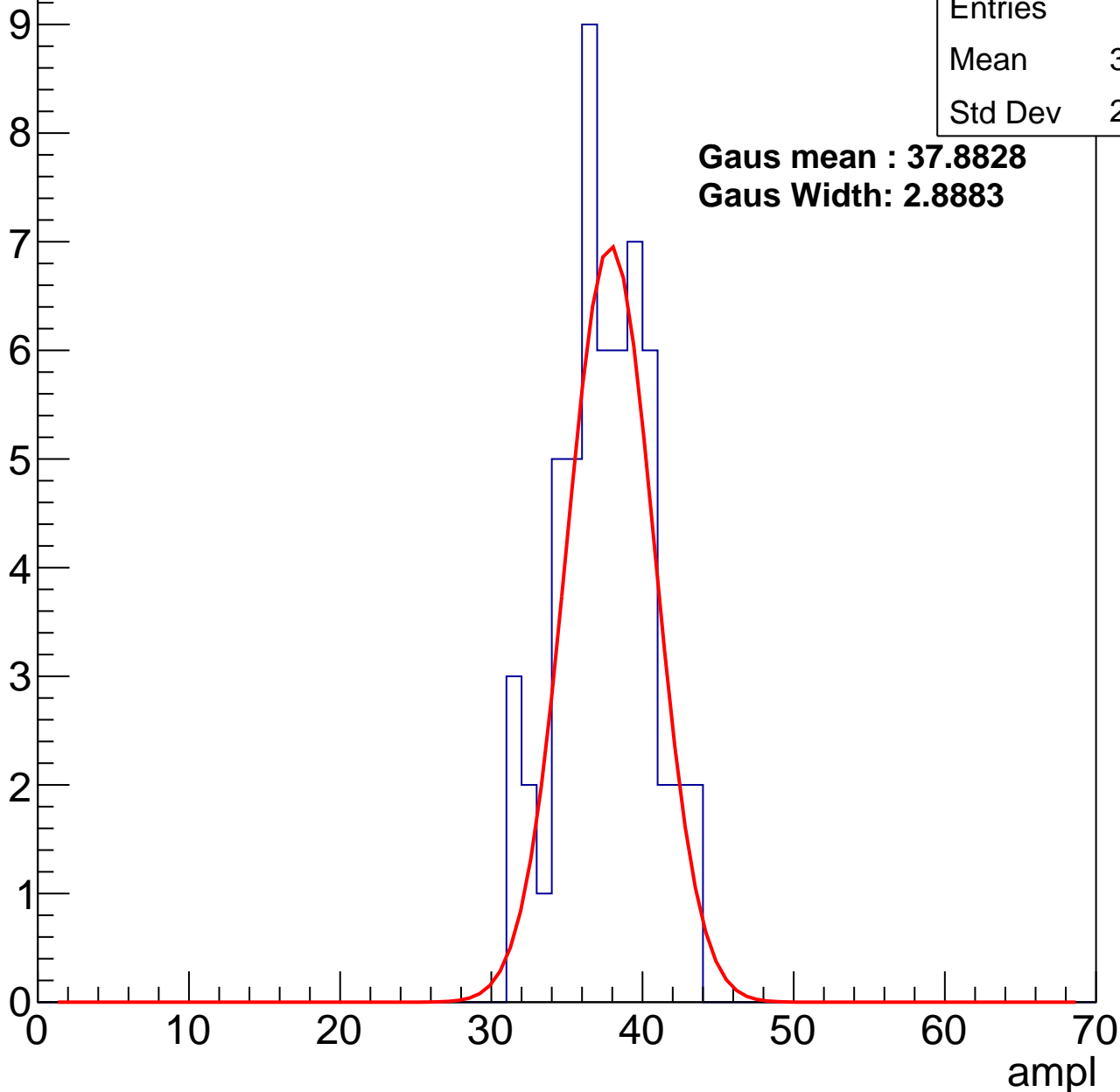
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	56
Mean	37.04
Std Dev	2.958

**Gaus mean : 37.8828**

**Gaus Width: 2.8883**



# B0L002S, U2-ch97, adc2

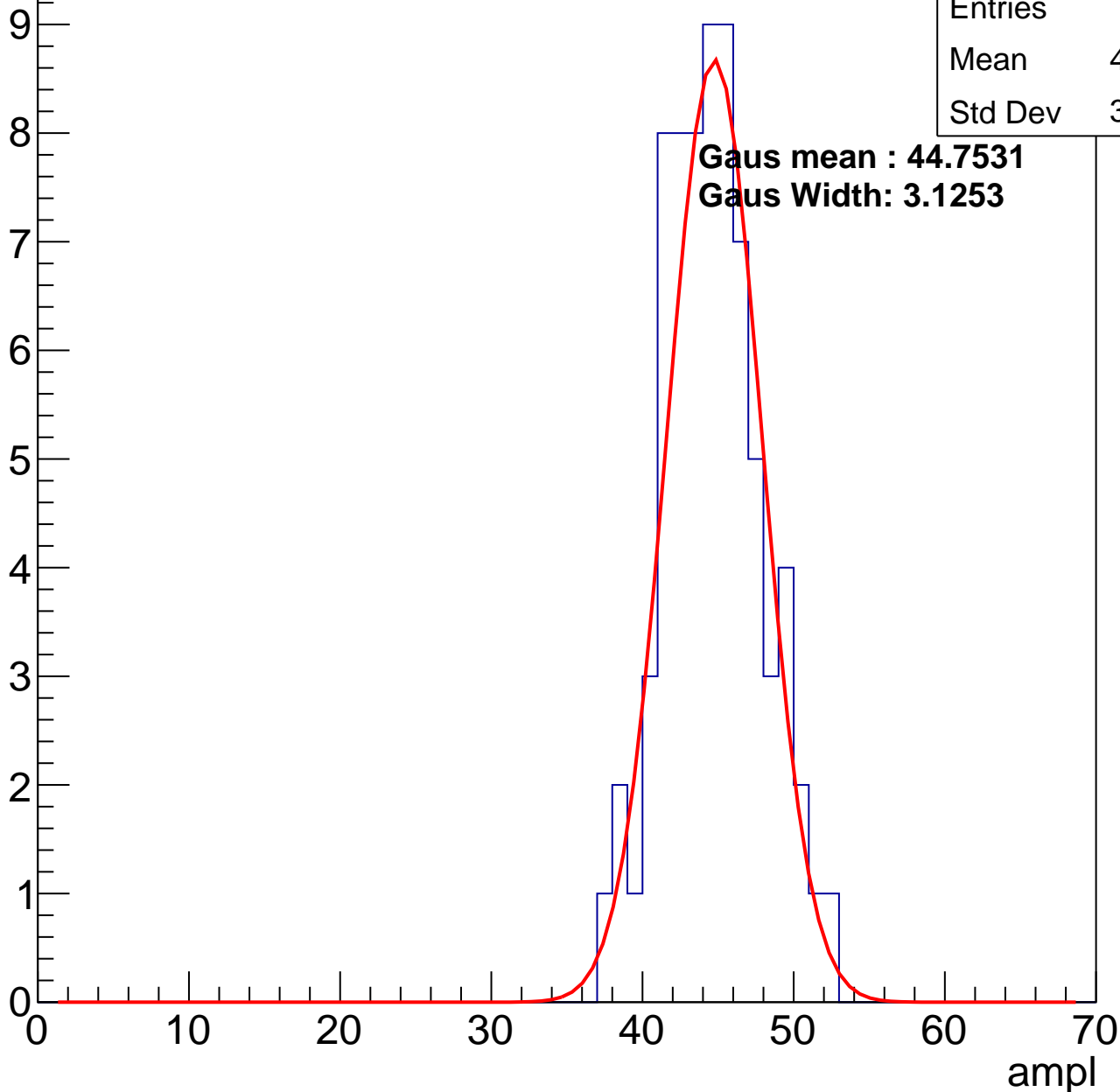
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	72
Mean	44.18
Std Dev	3.159

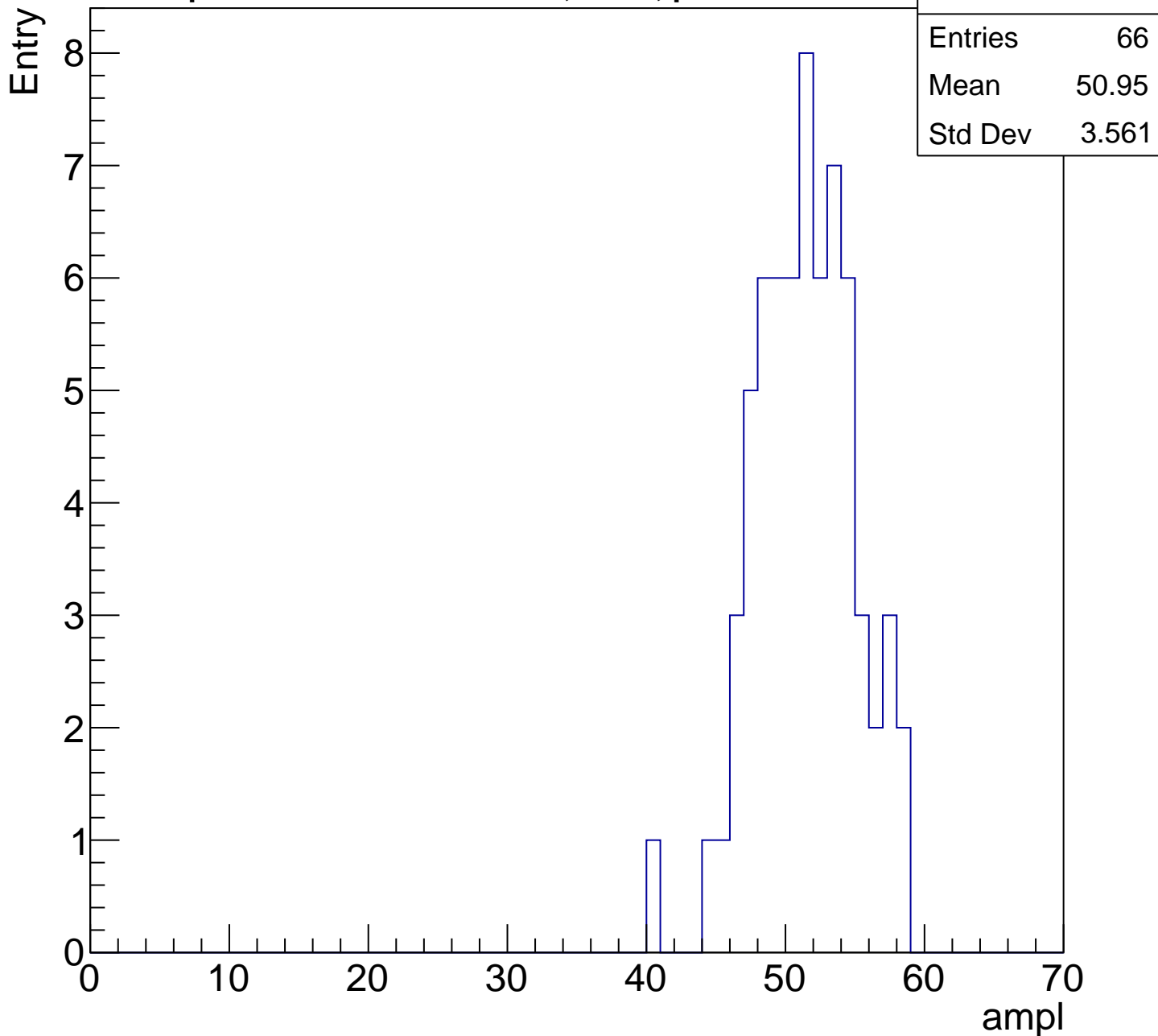
**Gaus mean : 44.7531**

**Gaus Width: 3.1253**



# B0L002S, U2-ch97, adc3

calib\_packv5\_042523\_0143.root, FC#8, port C1

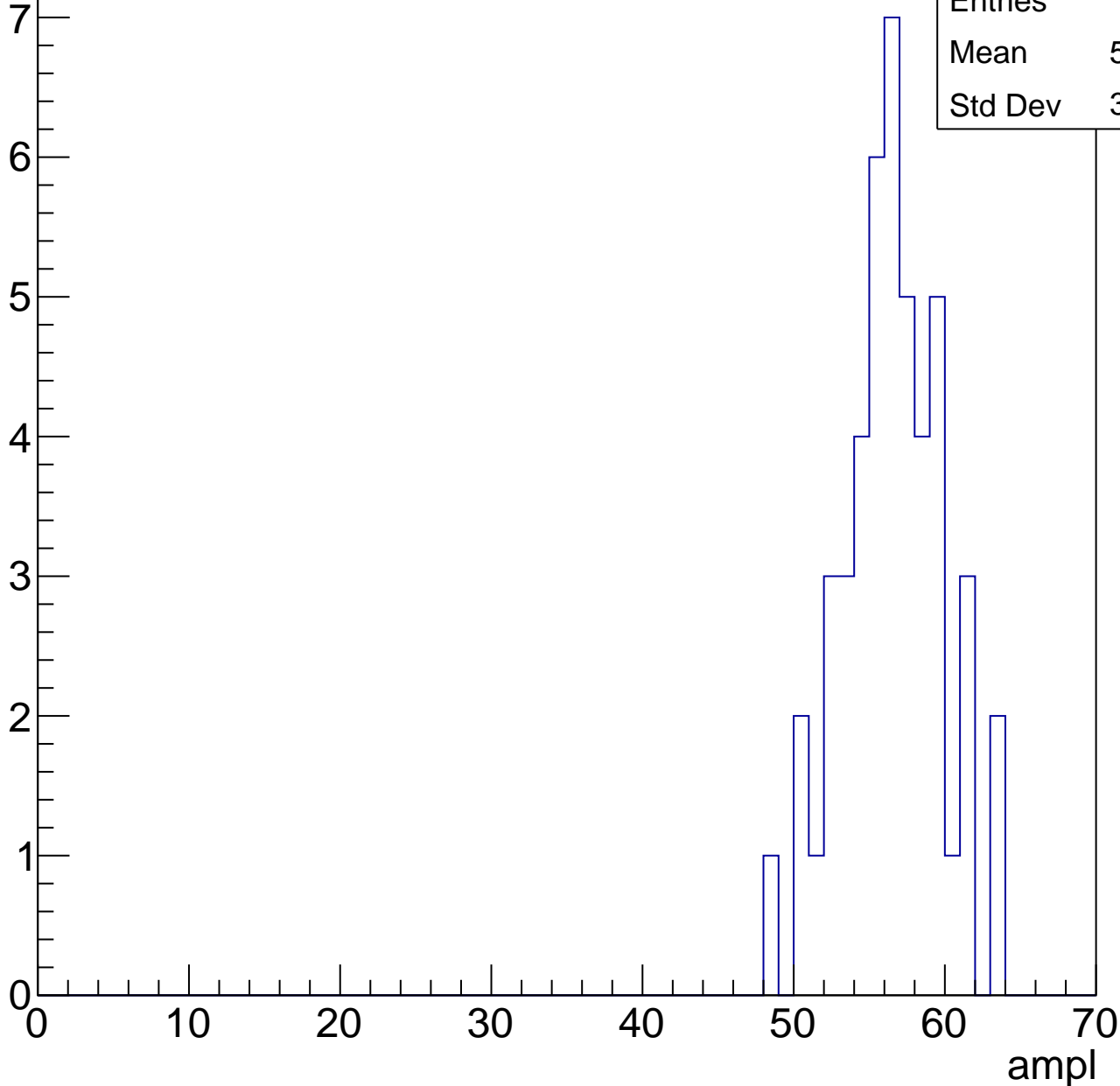


# B0L002S, U2-ch97, adc4

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	47
Mean	56.02
Std Dev	3.304



# B0L002S, U2-ch97, adc5

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

10

Entries 47

Mean 59.19

Std Dev 8.953

8

6

4

2

0

0

10

20

30

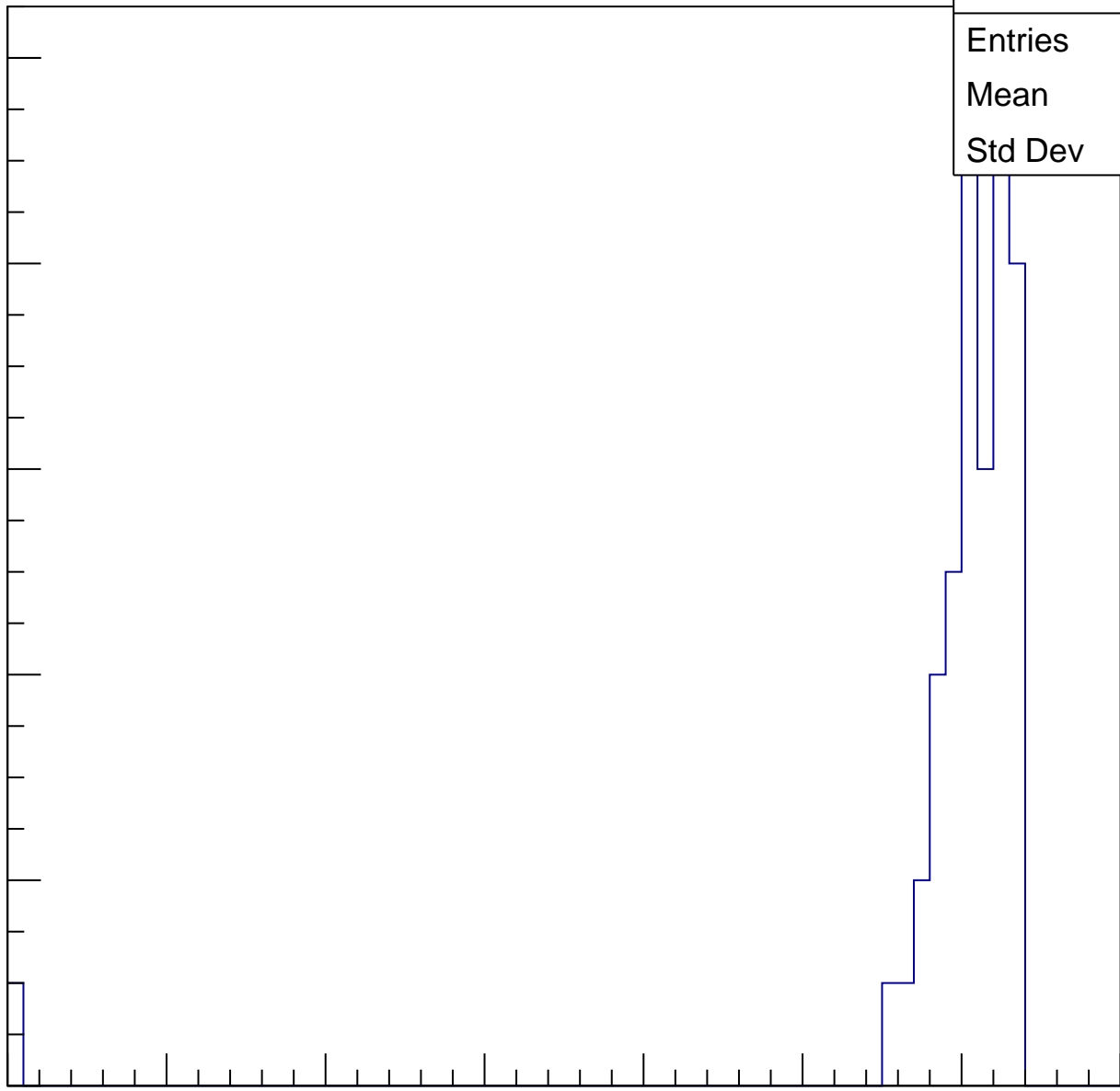
40

50

60

70

ampl



# B0L002S, U2-ch97, adc6

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry





# B0L002S, U2-ch97, adc7

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L002S, U2-ch98, adc0

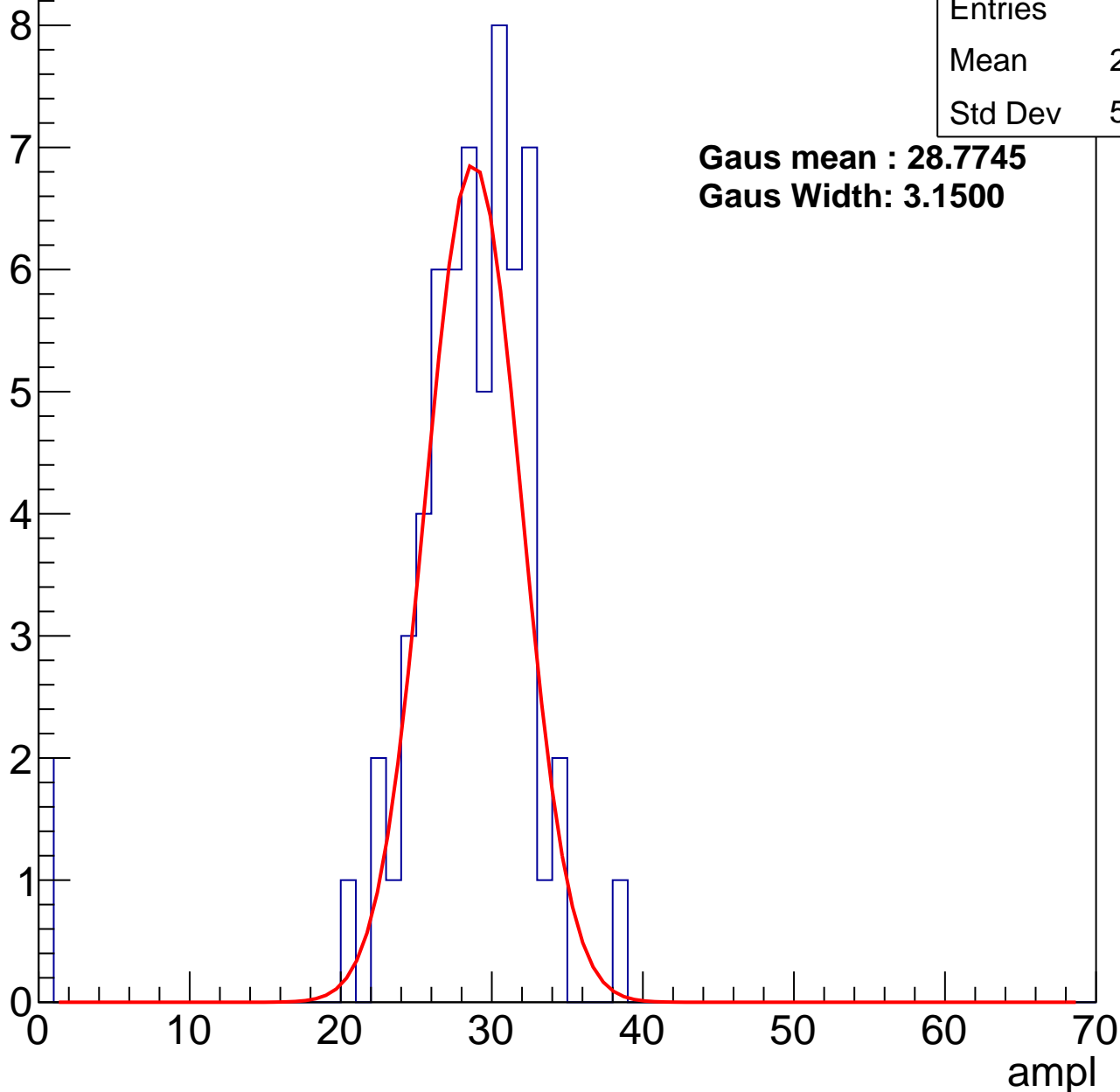
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	62
Mean	27.53
Std Dev	5.997

**Gaus mean : 28.7745**

**Gaus Width: 3.1500**



# B0L002S, U2-ch98, adc1

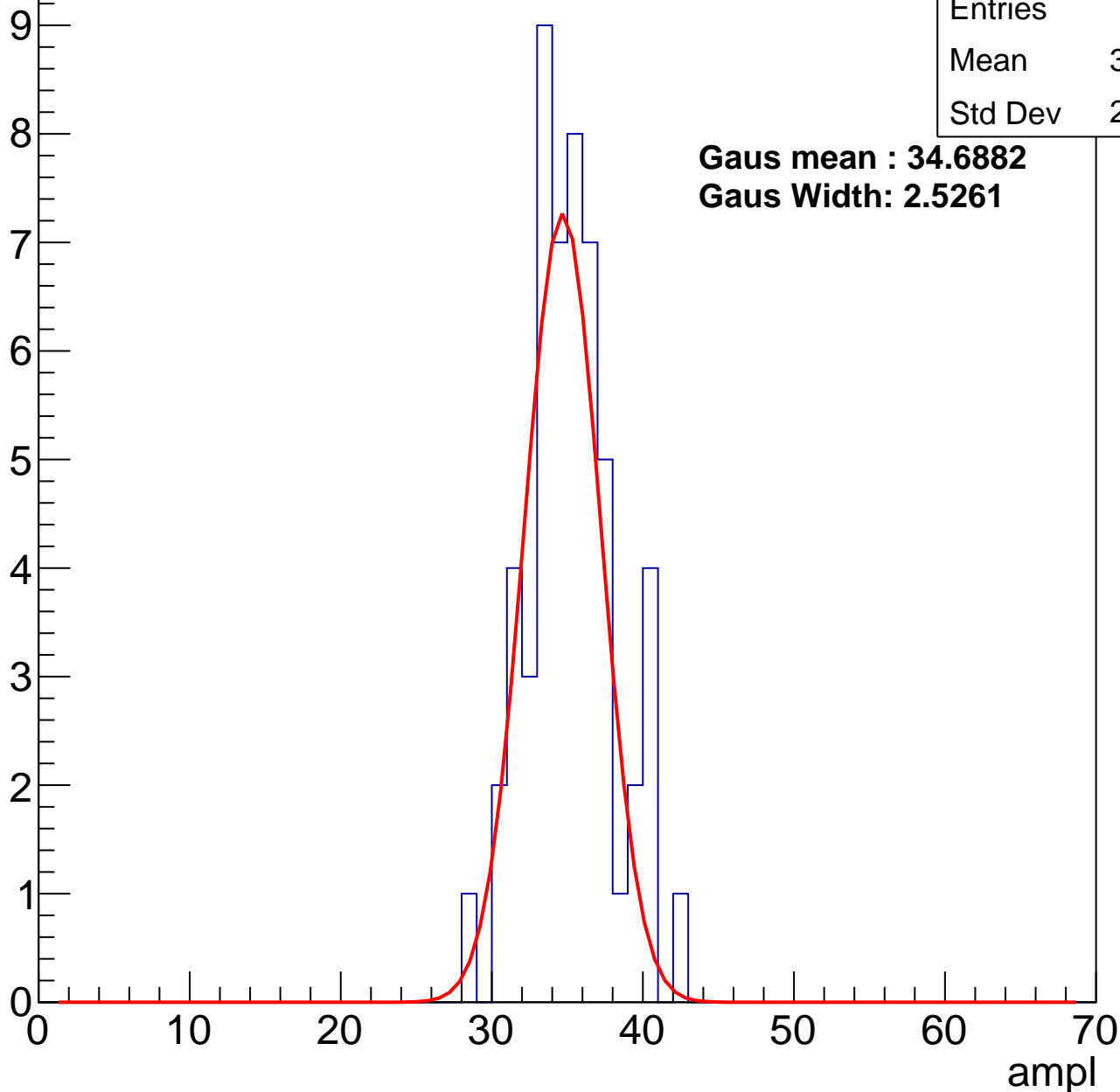
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	54
Mean	34.78
Std Dev	2.878

**Gaus mean : 34.6882**

**Gaus Width: 2.5261**



# B0L002S, U2-ch98, adc2

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entries	76
Mean	41.14
Std Dev	3.452

**Gaus mean : 41.1001**

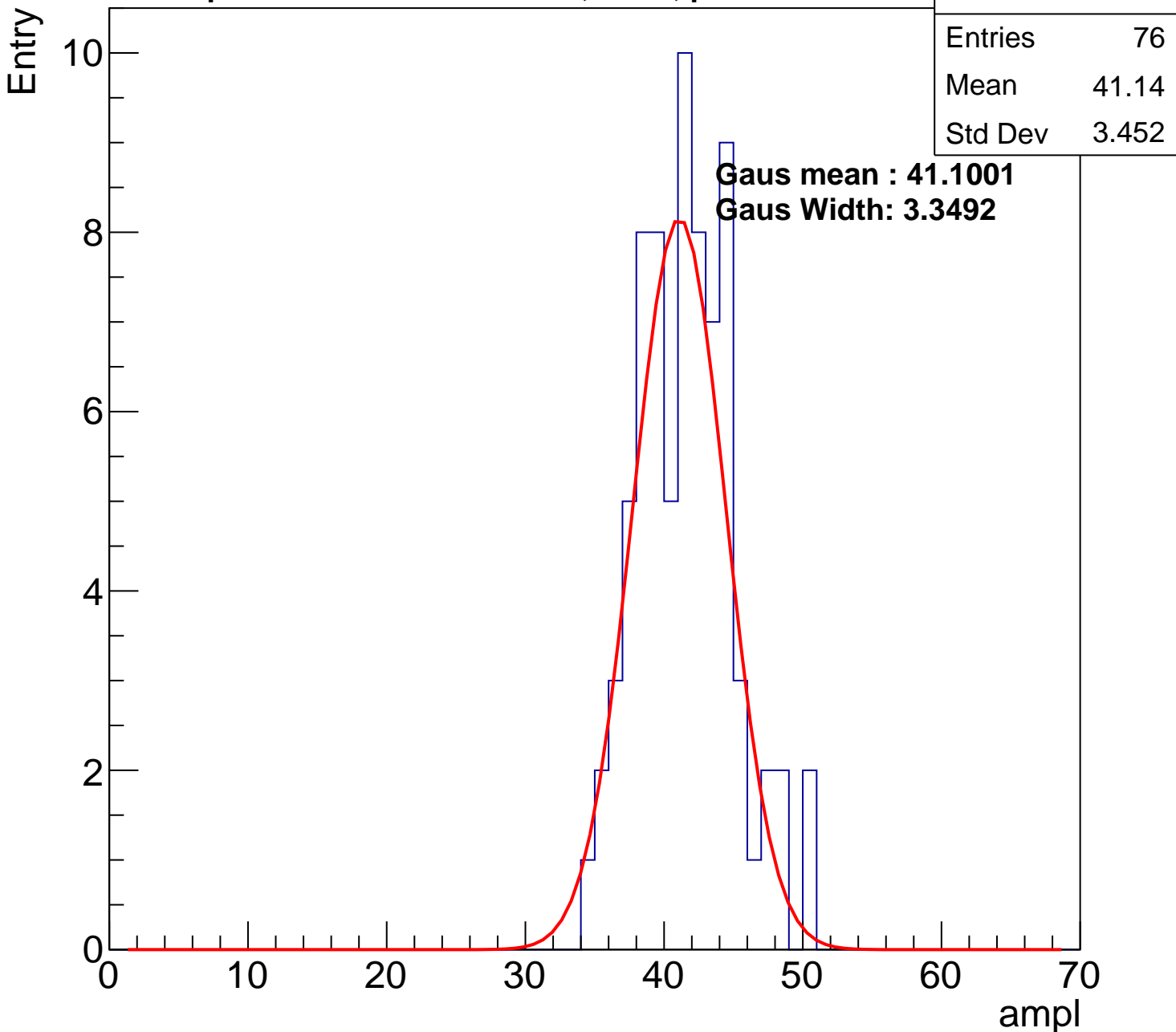
**Gaus Width: 3.3492**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

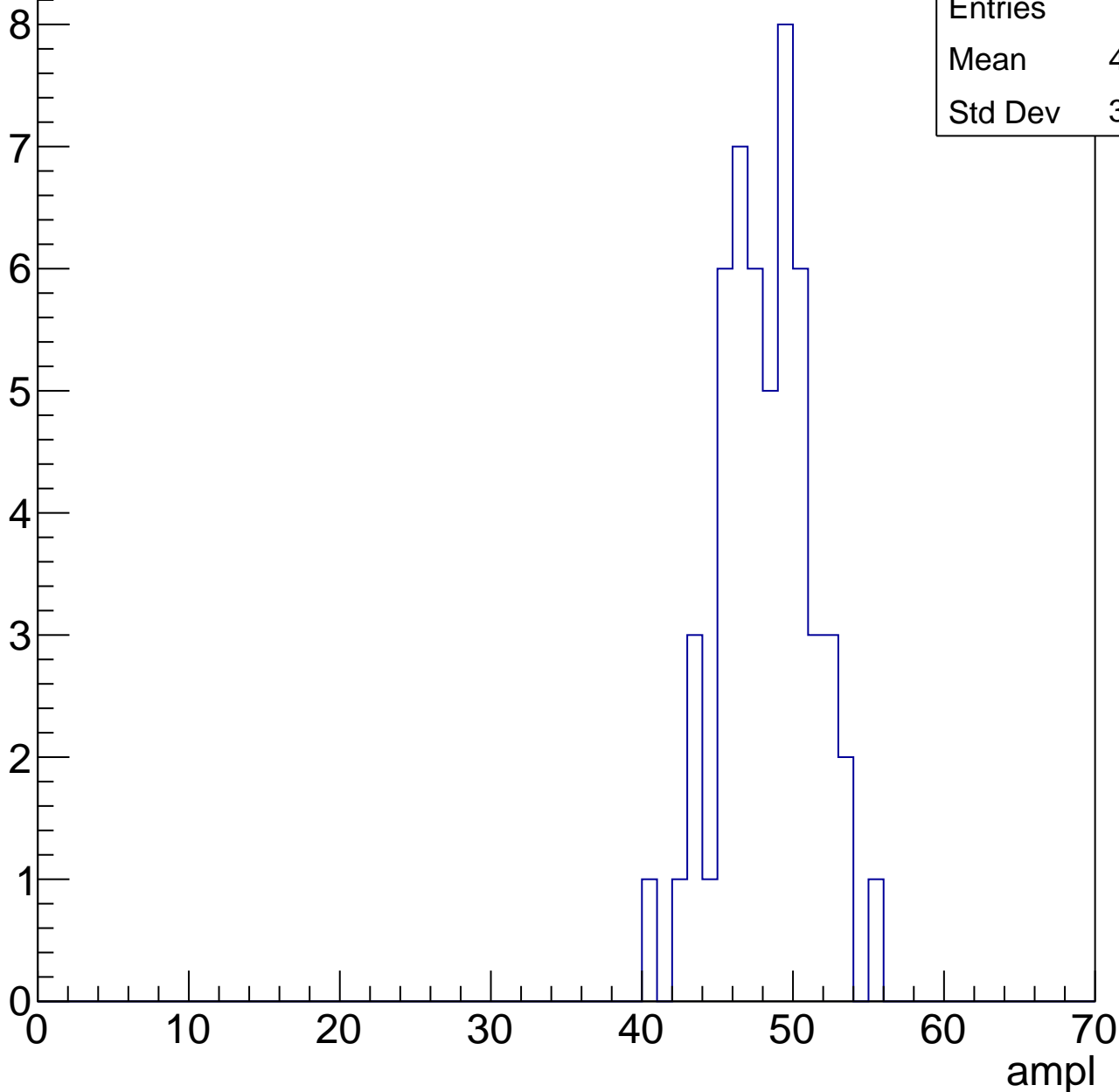


# B0L002S, U2-ch98, adc3

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	53
Mean	47.75
Std Dev	3.015

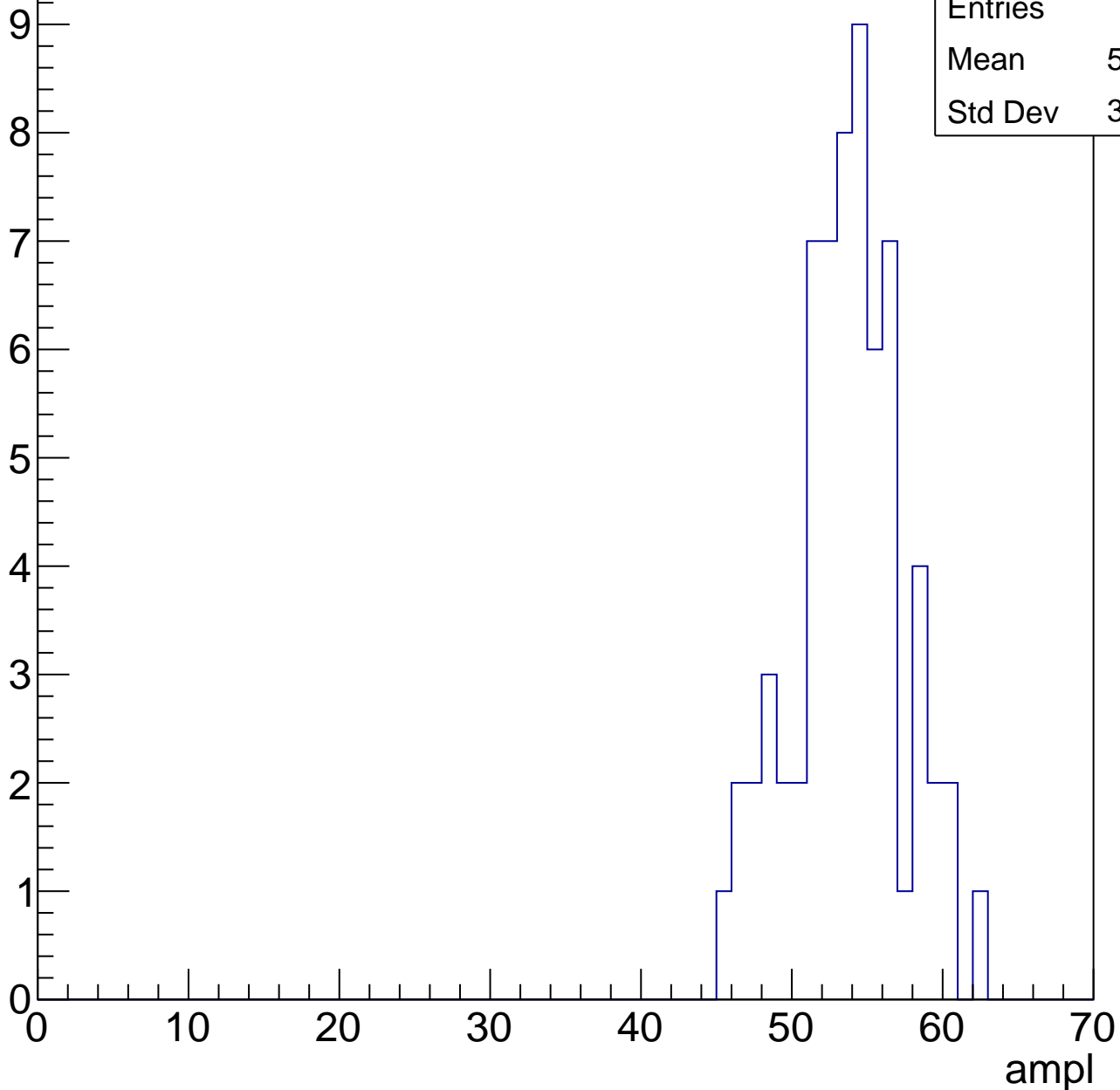


# B0L002S, U2-ch98, adc4

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	66
Mean	53.26
Std Dev	3.594

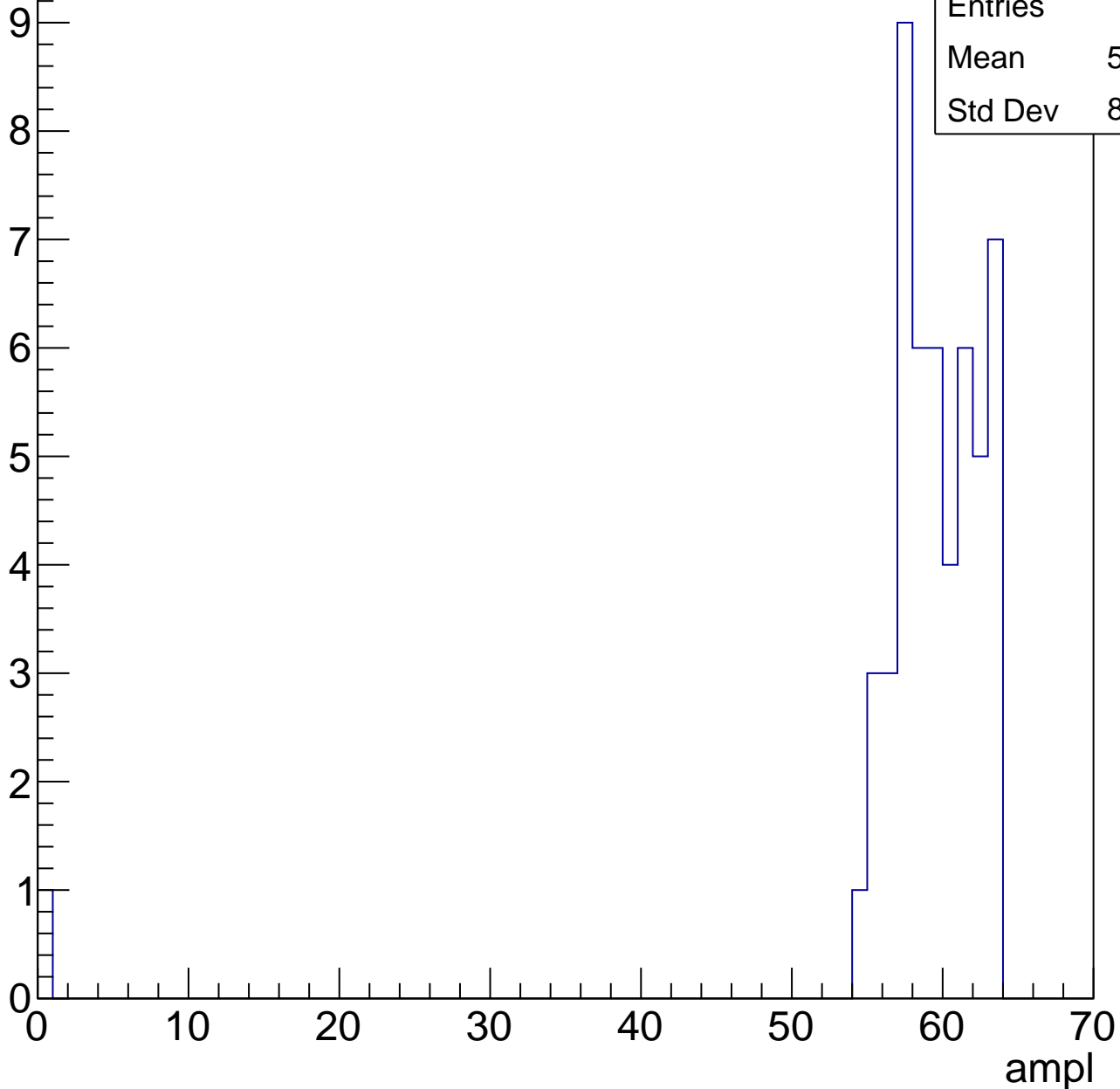


# B0L002S, U2-ch98, adc5

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

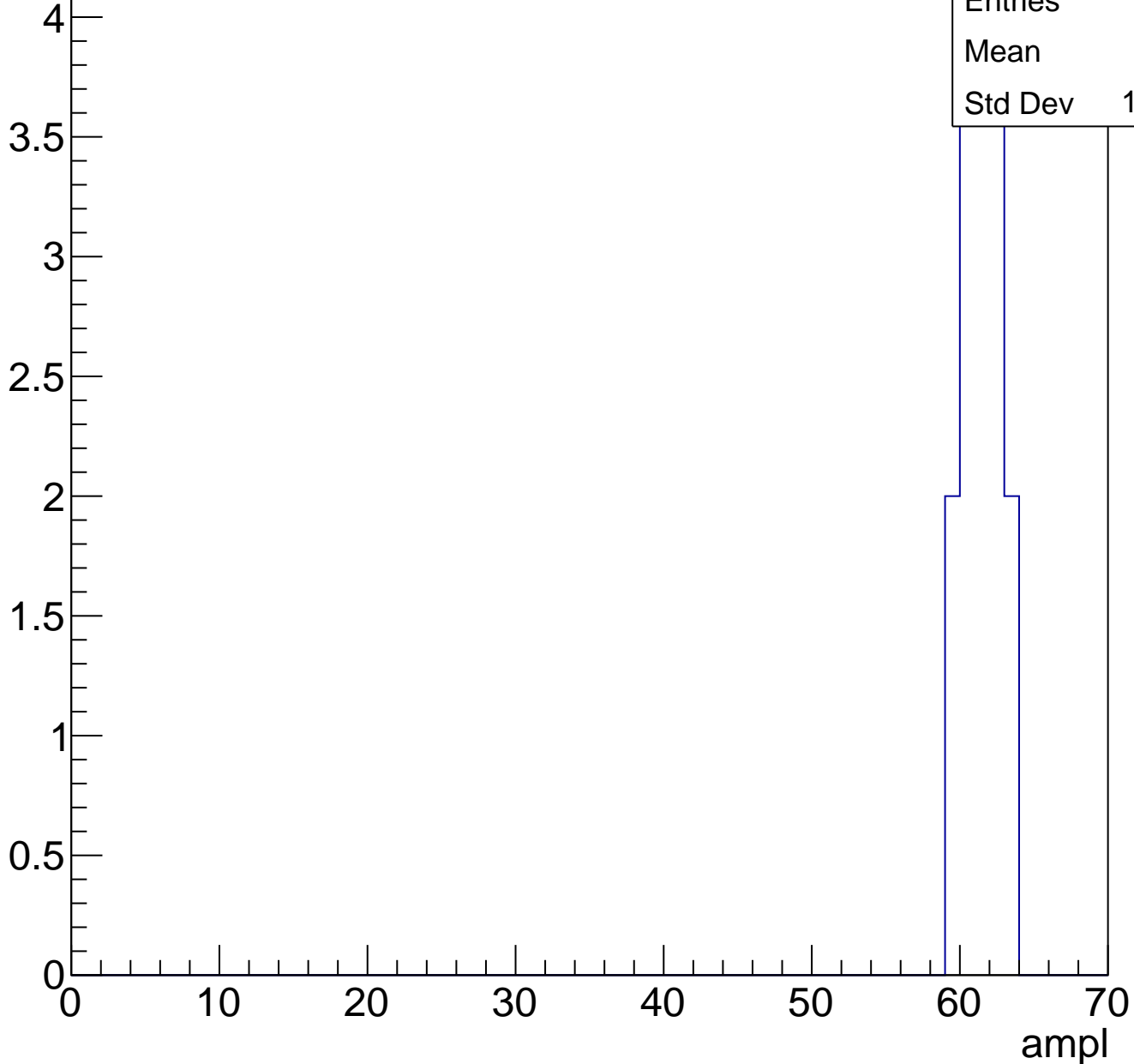
Entries	51
Mean	58.02
Std Dev	8.585



# B0L002S, U2-ch98, adc6

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



Entries	16
Mean	61
Std Dev	1.225



# B0L002S, U2-ch98, adc7

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



# B0L002S, U2-ch99, adc0

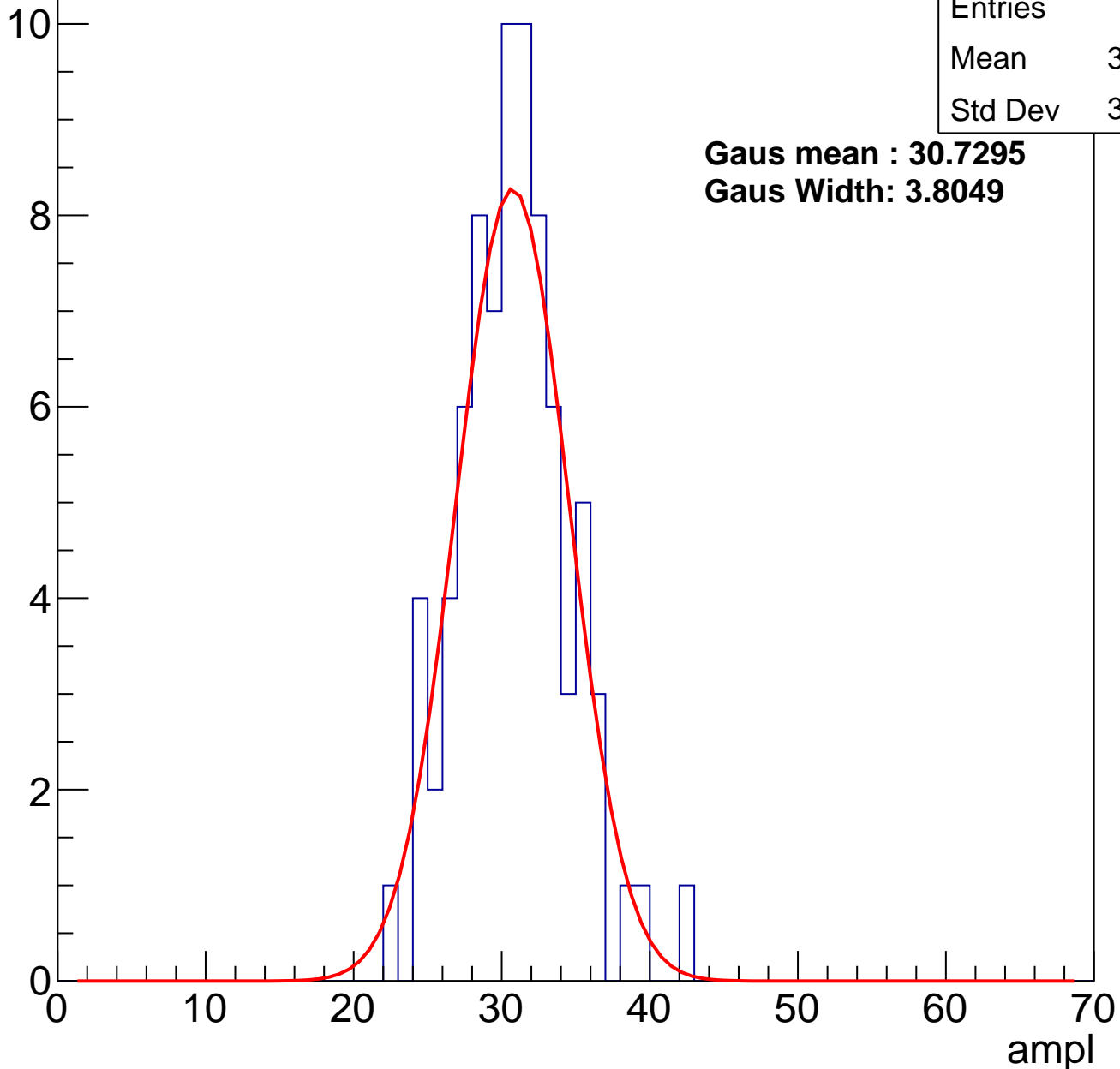
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entries	80
Mean	30.36
Std Dev	3.658

**Gaus mean : 30.7295**

**Gaus Width: 3.8049**

Entry



# B0L002S, U2-ch99, adc1

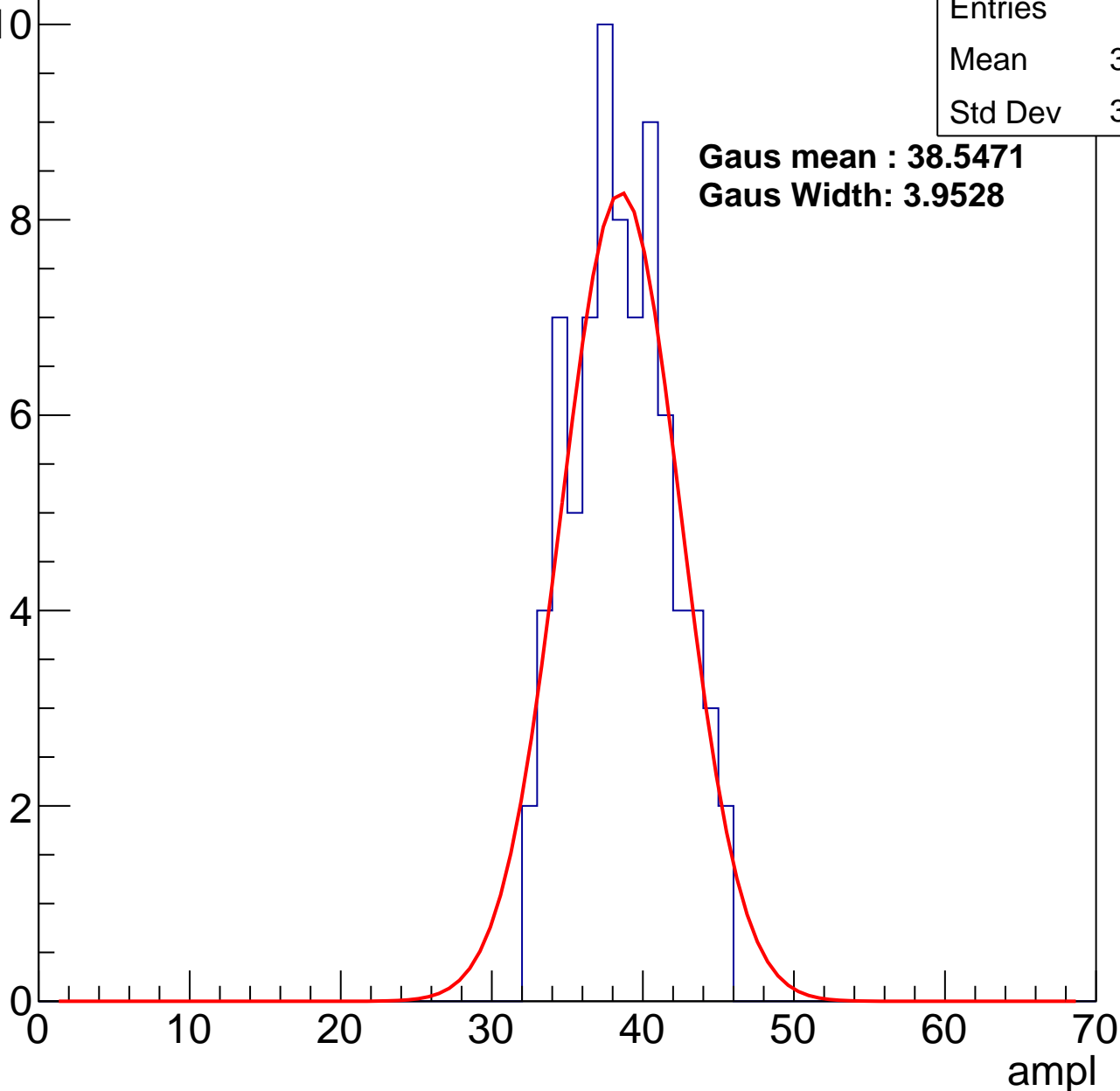
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	78
Mean	38.15
Std Dev	3.266

**Gaus mean : 38.5471**

**Gaus Width: 3.9528**



# B0L002S, U2-ch99, adc2

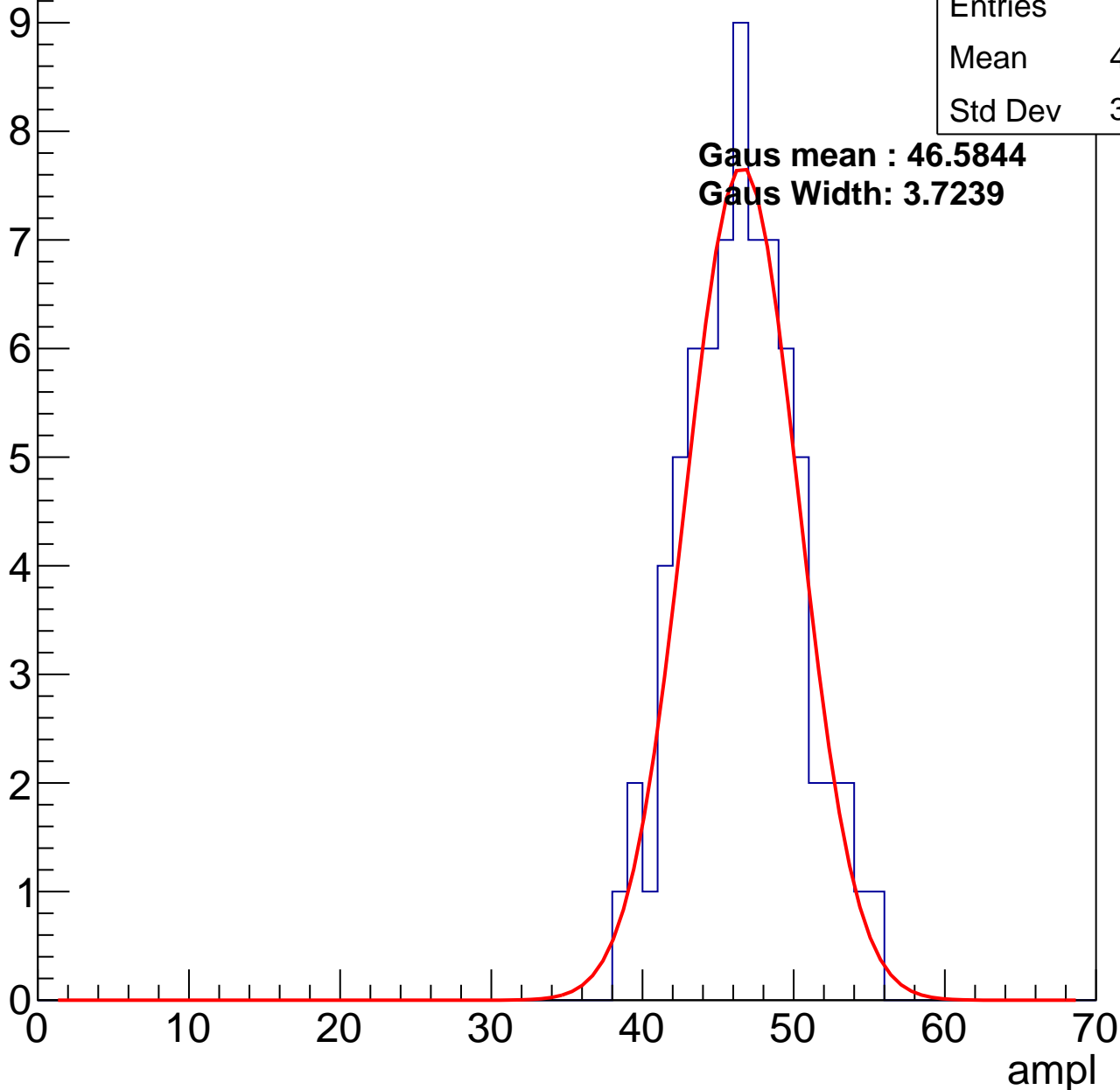
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	74
Mean	46.09
Std Dev	3.669

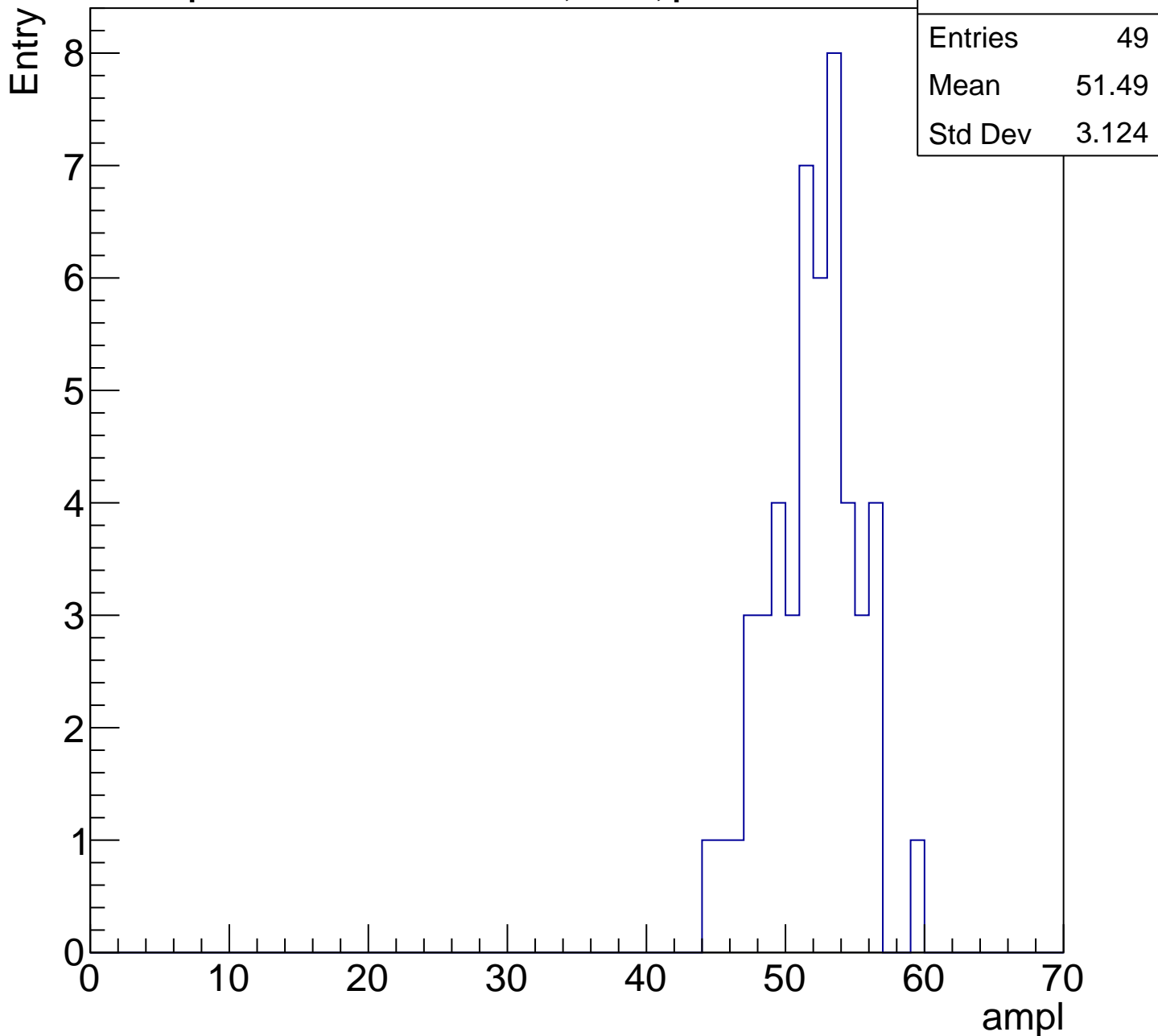
**Gaus mean : 46.5844**

**Gaus Width: 3.7239**



# B0L002S, U2-ch99, adc3

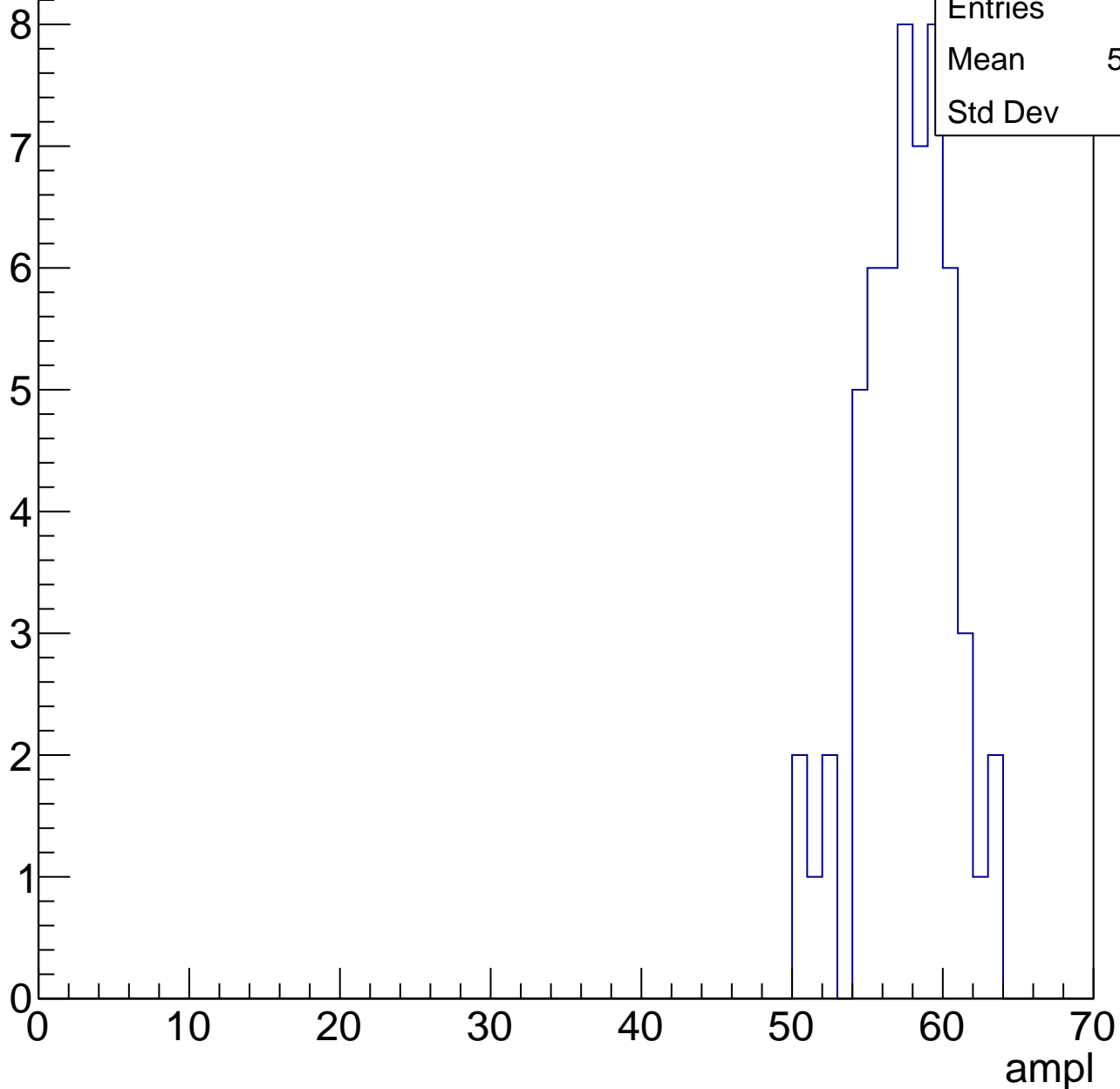
calib\_packv5\_042523\_0143.root, FC#8, port C1



# B0L002S, U2-ch99, adc4

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

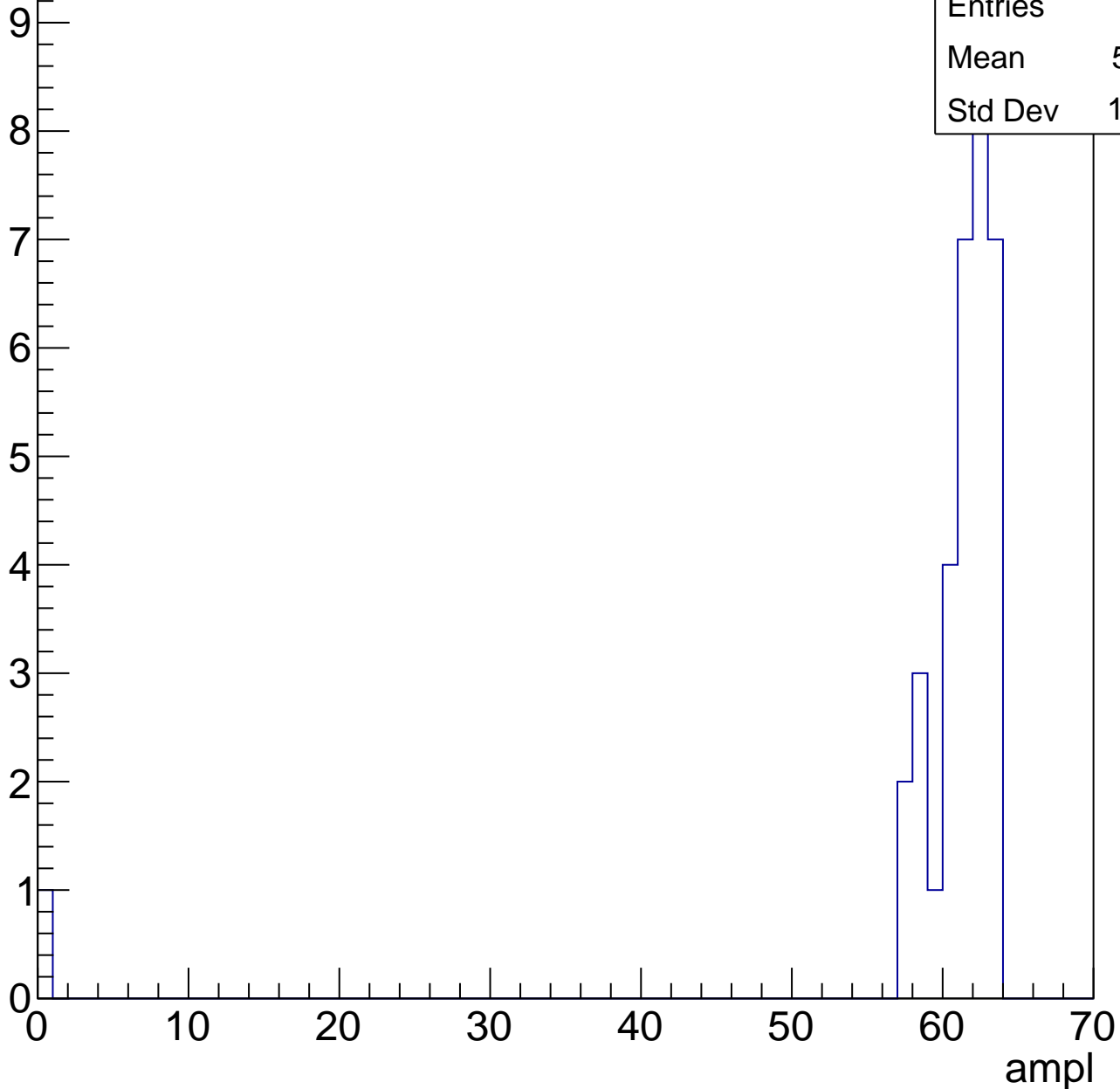


# B0L002S, U2-ch99, adc5

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	34
Mean	59.21
Std Dev	10.45



# B0L002S, U2-ch99, adc6

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry





# B0L002S, U2-ch99, adc7

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L002S, U2-ch100, adc0

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entries	82
Mean	31.27
Std Dev	3.276

**Gaus mean : 31.7316**

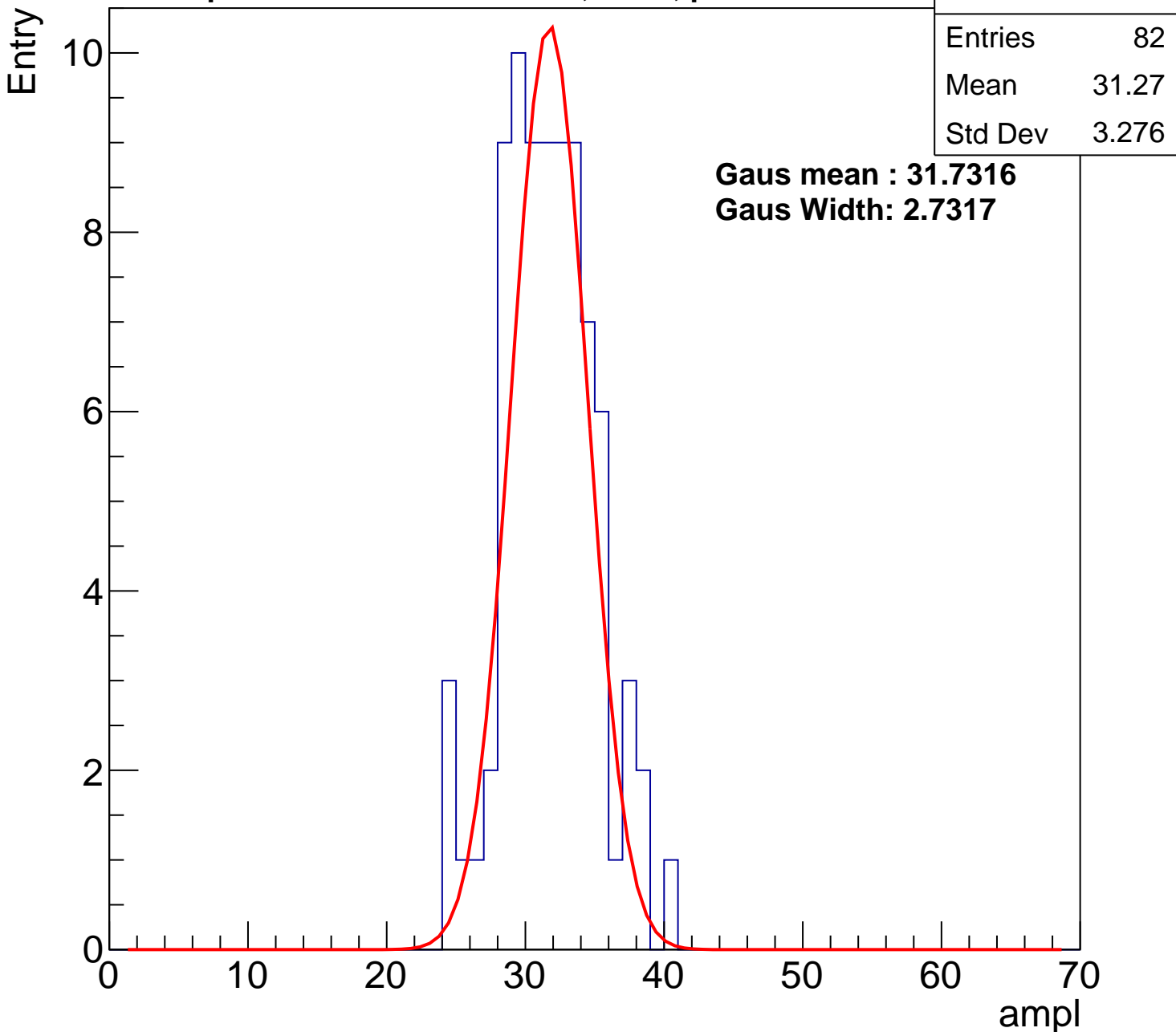
**Gaus Width: 2.7317**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L002S, U2-ch100, adc1

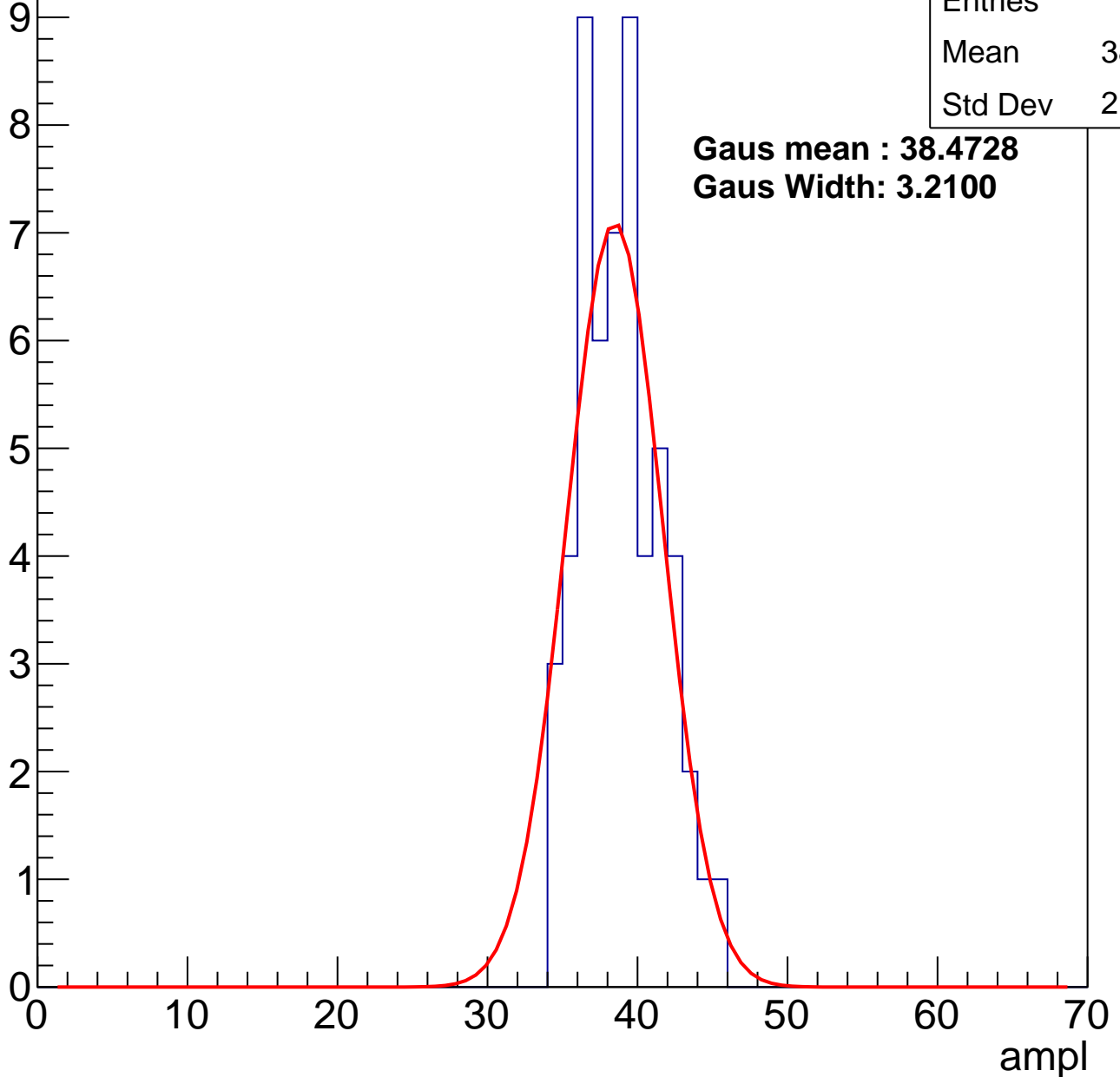
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	55
Mean	38.42
Std Dev	2.647

**Gaus mean : 38.4728**

**Gaus Width: 3.2100**



# B0L002S, U2-ch100, adc2

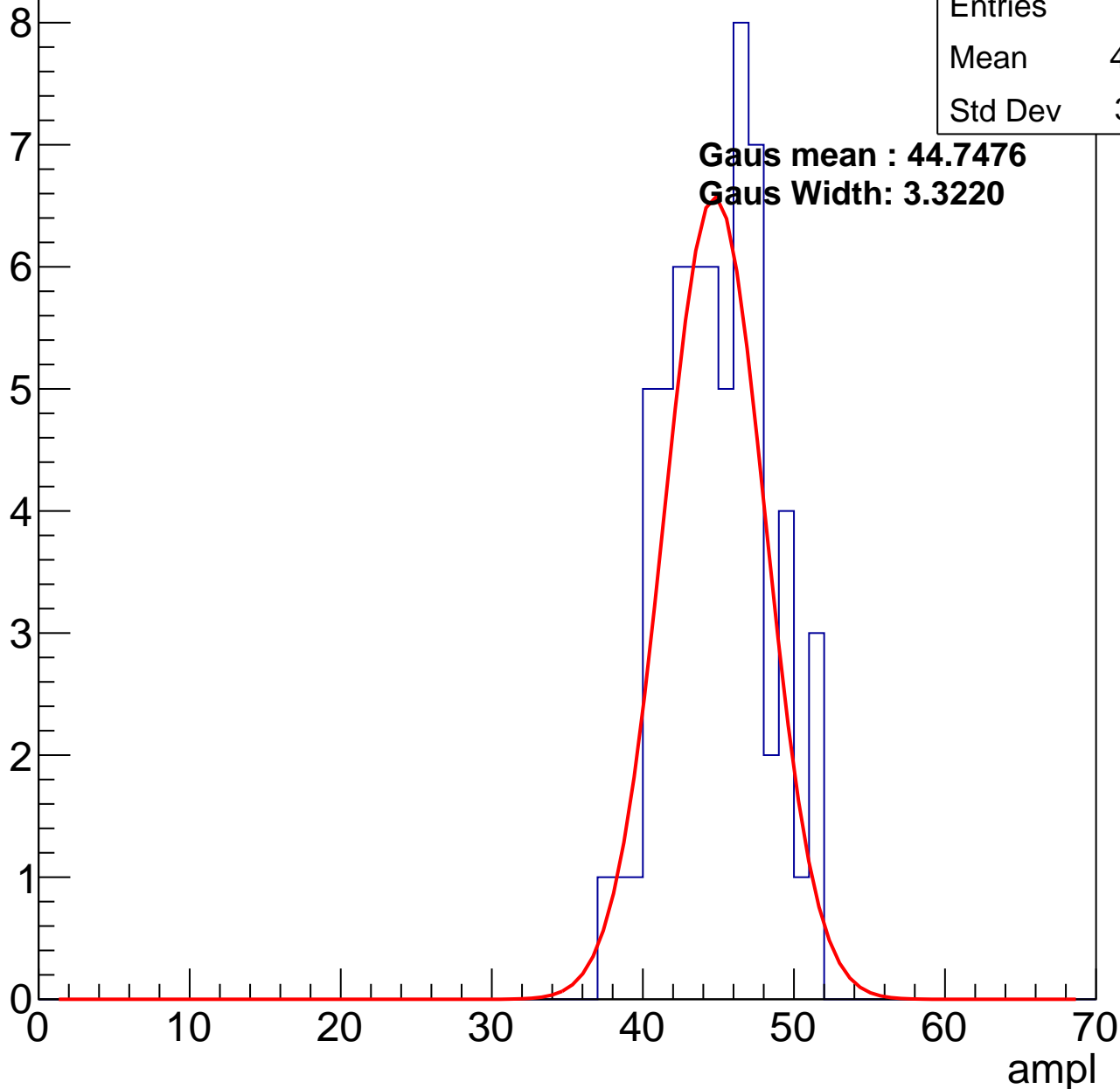
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	61
Mean	44.43
Std Dev	3.311

**Gaus mean : 44.7476**

**Gaus Width: 3.3220**



# B0L002S, U2-ch100, adc3

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entries	88
Mean	51.34
Std Dev	3.89

Entry

10

8

6

4

2

0

0

10

20

30

40

50

60

ampl

0

1

2

3

4

5

6

7

8

9

10

11

12

13

14

15

16

17

18

19

20

21

22

23

24

25

26

27

28

29

30

31

32

33

34

35

36

37

38

39

40

41

42

43

44

45

46

47

48

49

50

51

52

53

54

55

56

57

58

59

60

61

62

63

64

65

66

67

68

69

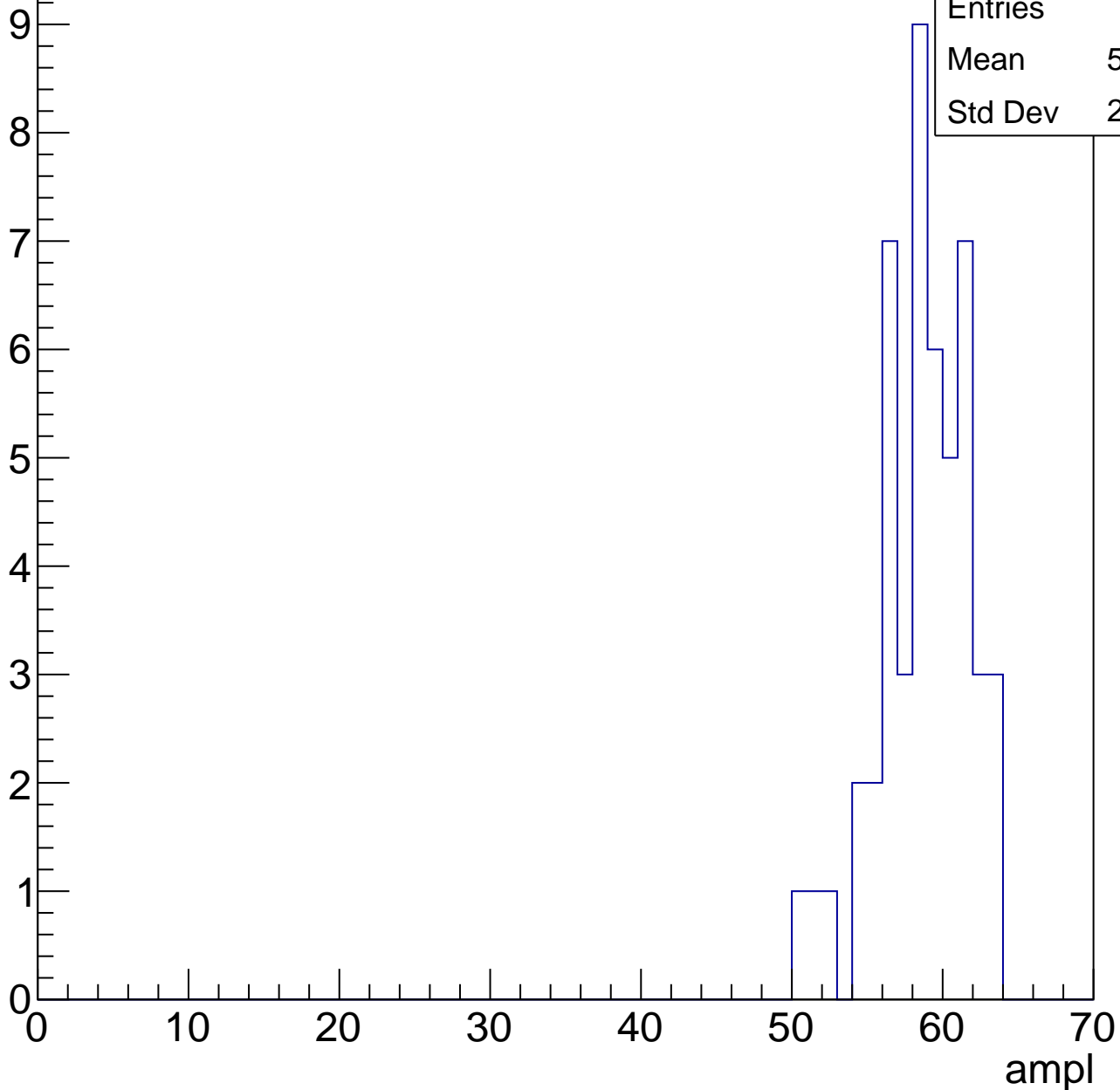
70

# B0L002S, U2-ch100, adc4

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	50
Mean	58.24
Std Dev	2.964

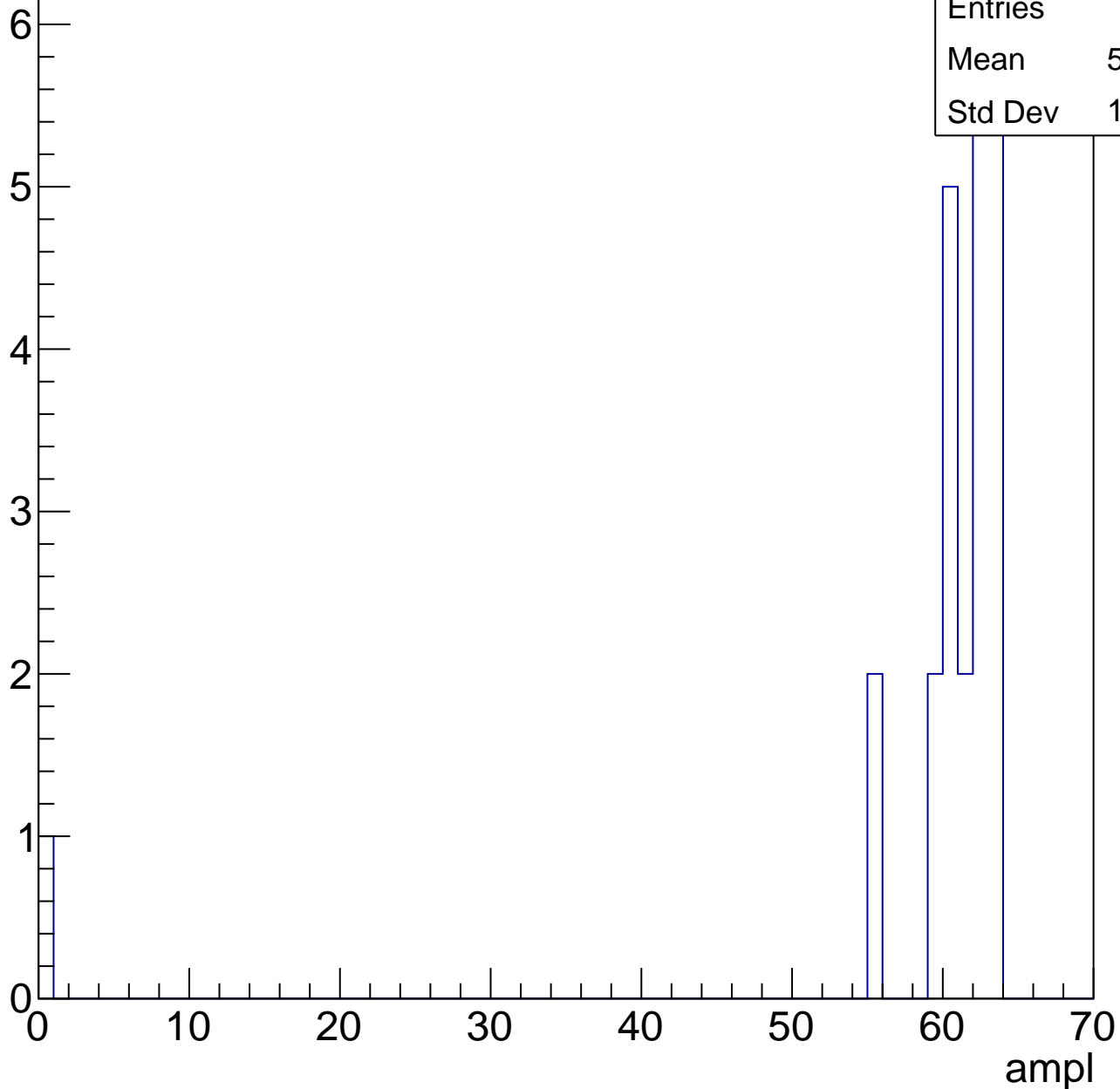


# B0L002S, U2-ch100, adc5

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	24
Mean	58.33
Std Dev	12.36



# B0L002S, U2-ch100, adc6

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry





# B0L002S, U2-ch100, adc7

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



# B0L002S, U2-ch101, adc0

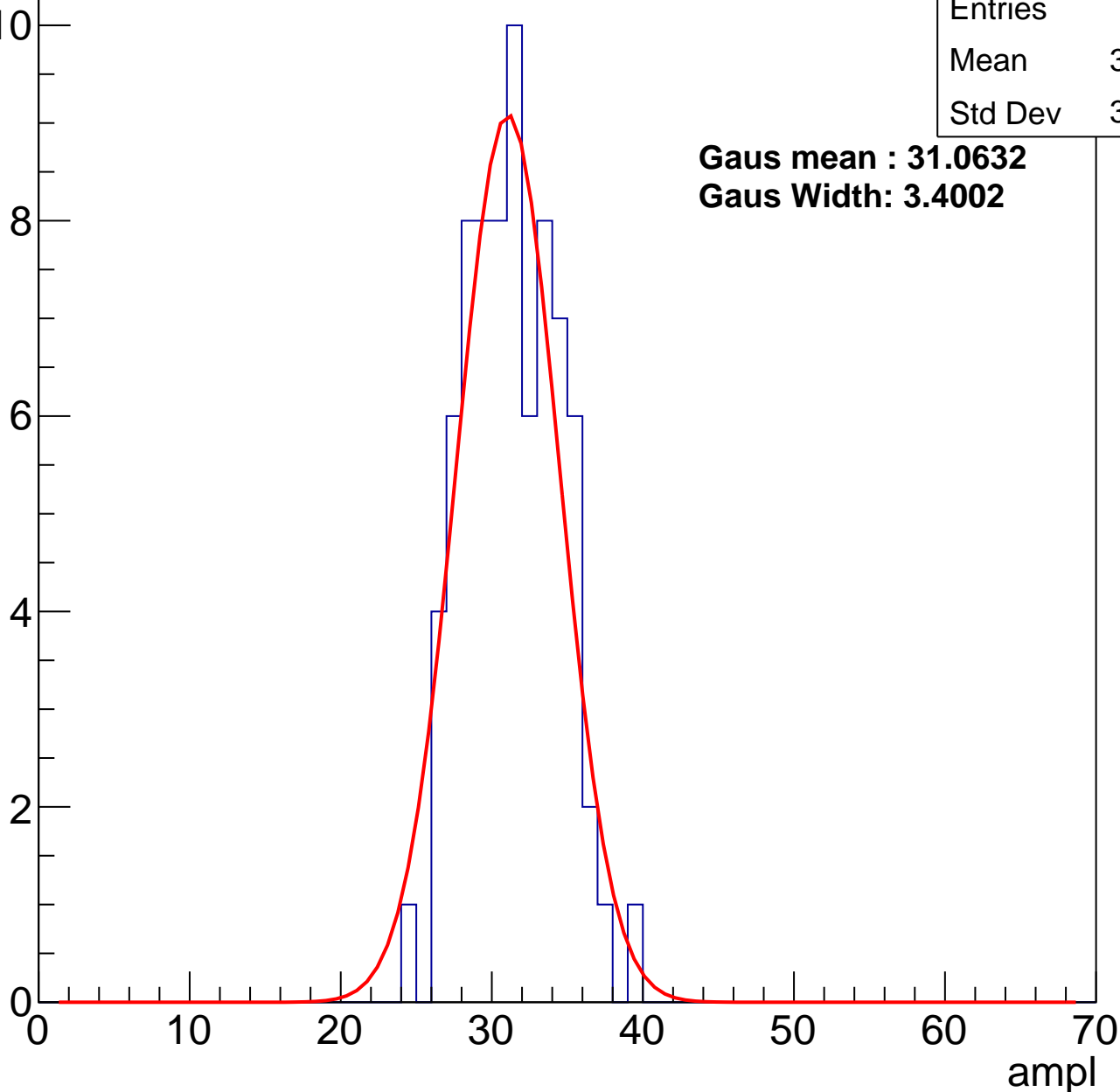
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	76
Mean	30.89
Std Dev	3.042

**Gaus mean : 31.0632**

**Gaus Width: 3.4002**



# B0L002S, U2-ch101, adc1

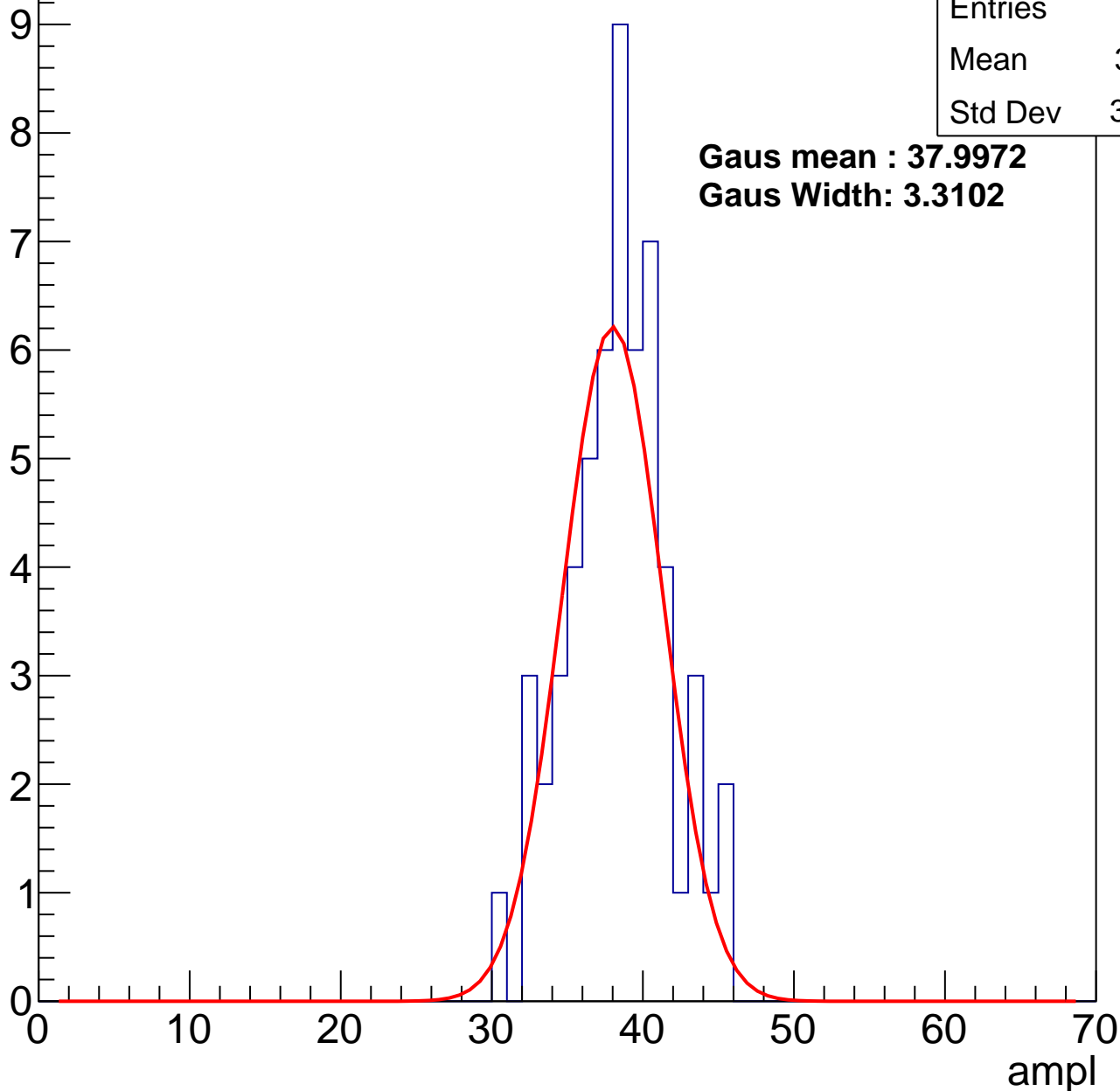
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	57
Mean	37.91
Std Dev	3.315

**Gaus mean : 37.9972**

**Gaus Width: 3.3102**



# B0L002S, U2-ch101, adc2

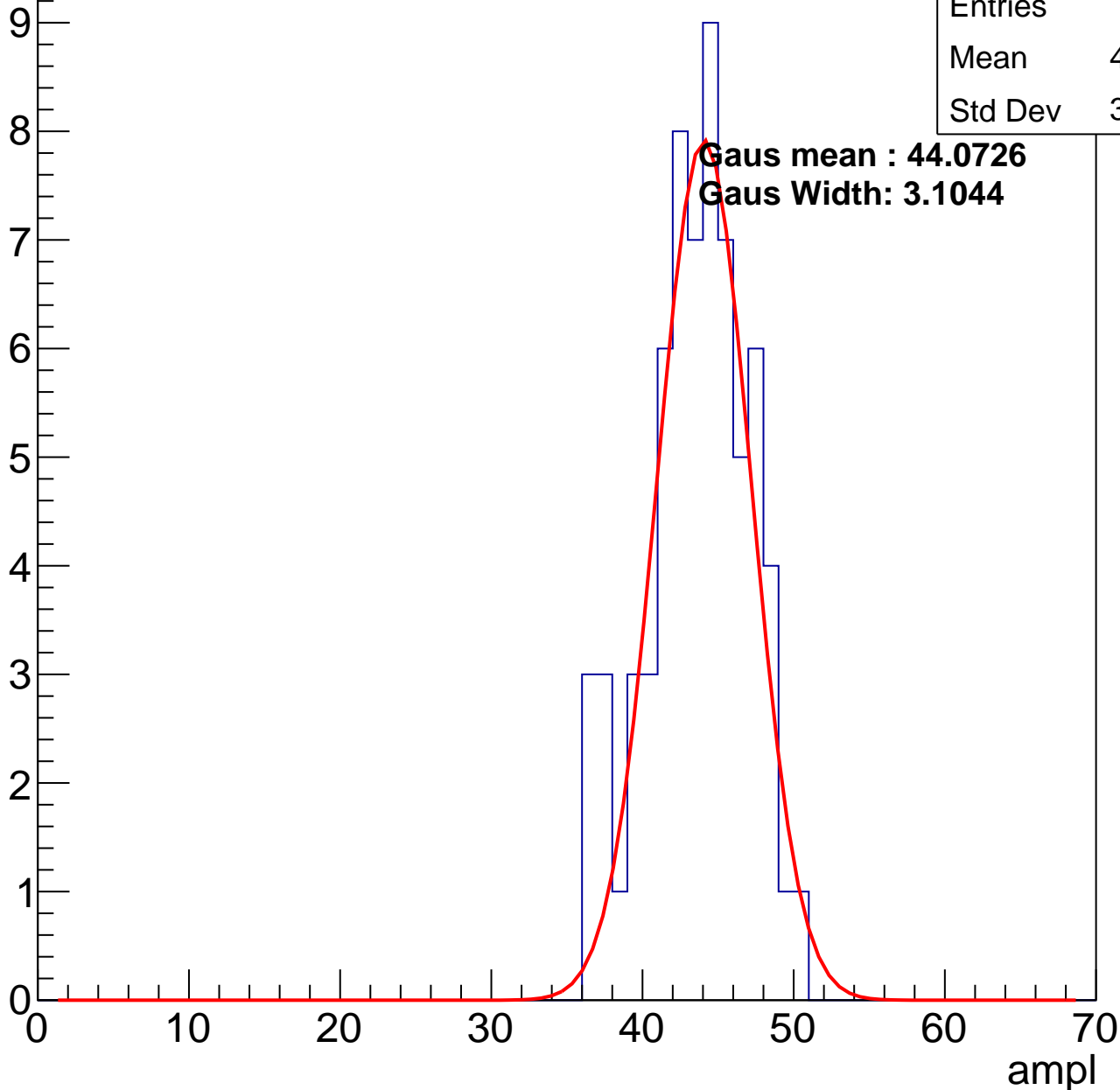
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	67
Mean	43.15
Std Dev	3.342

**Gaus mean : 44.0726**

**Gaus Width: 3.1044**

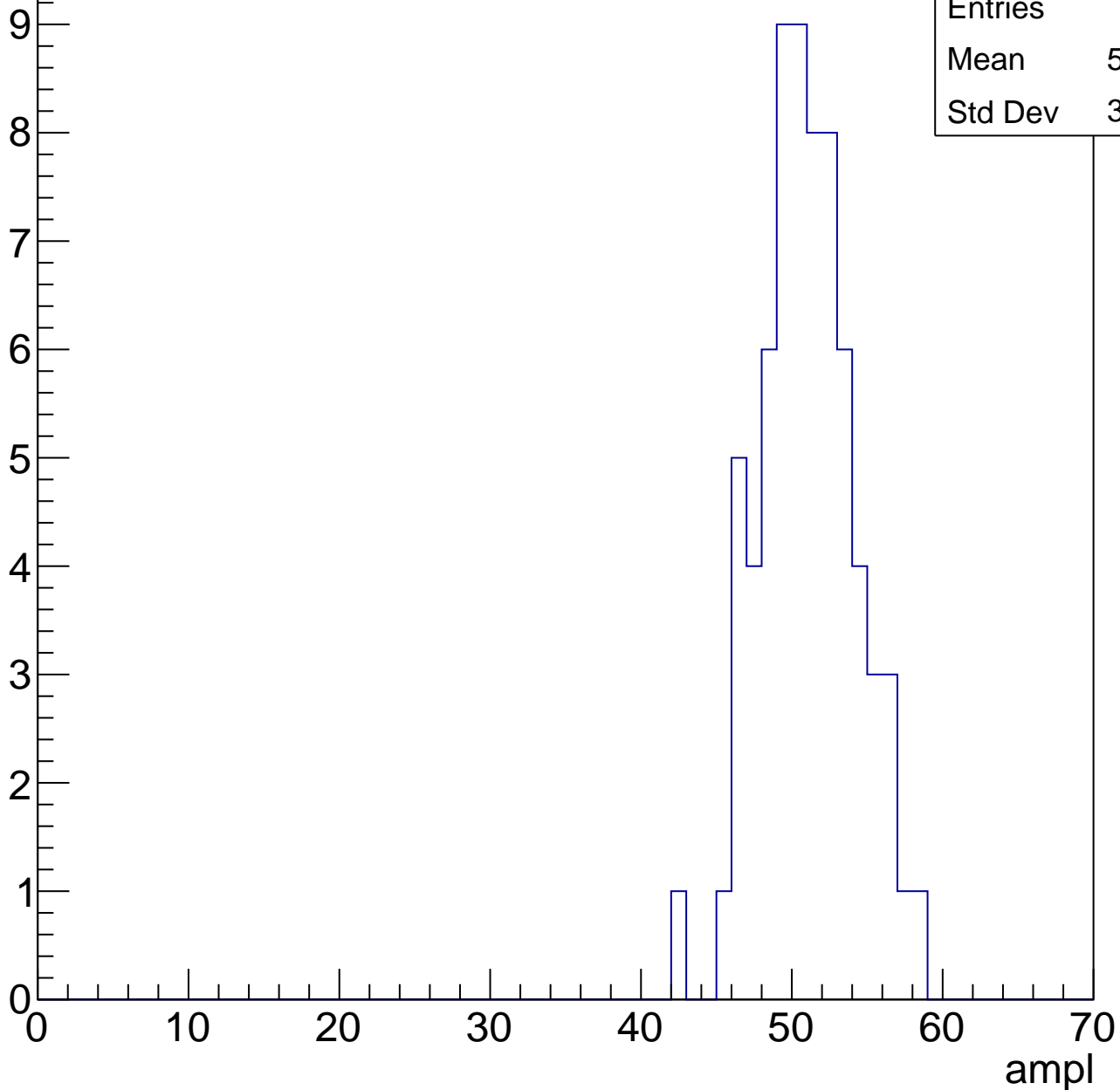


# B0L002S, U2-ch101, adc3

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

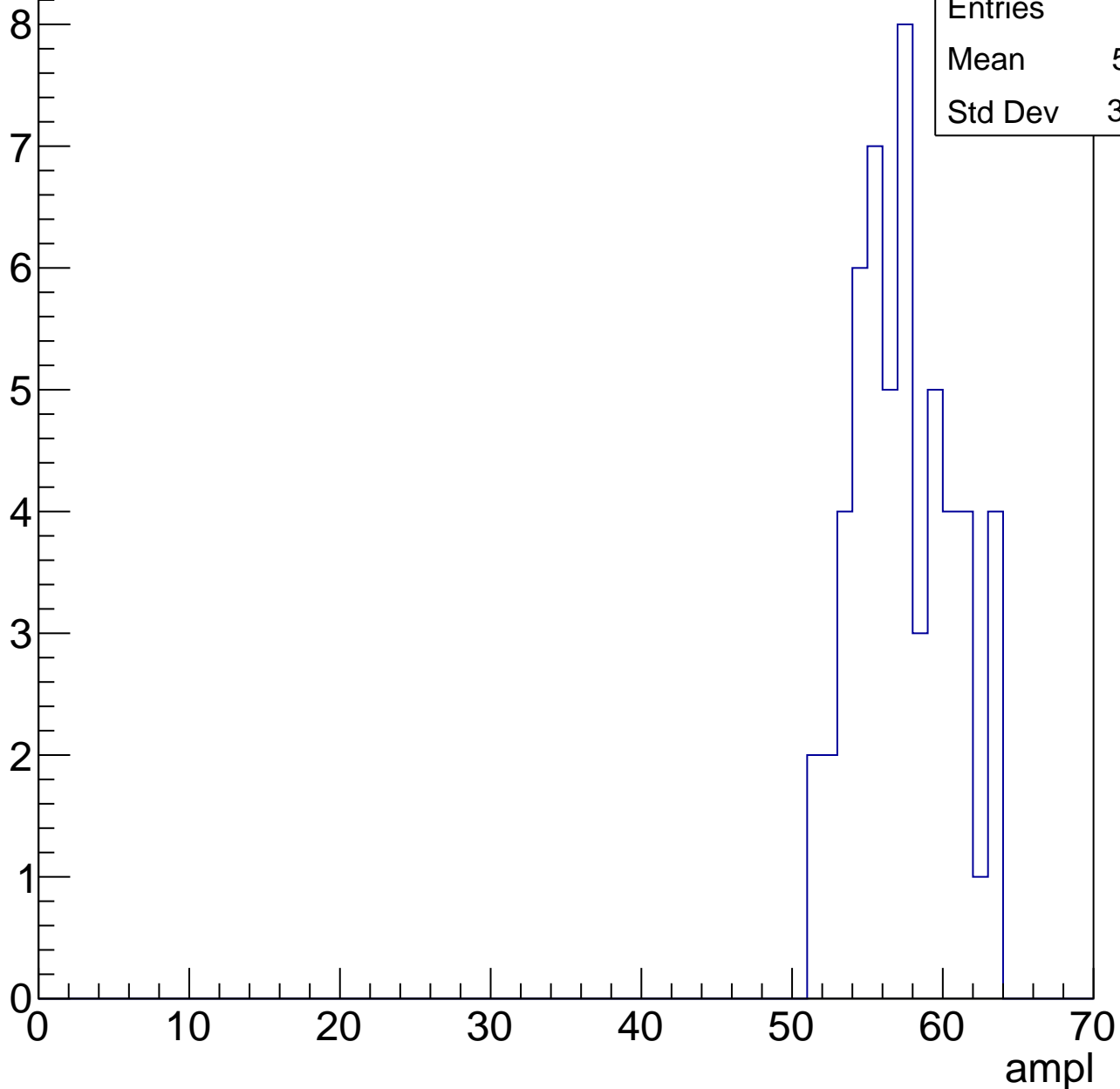
Entries	69
Mean	50.58
Std Dev	3.113



# B0L002S, U2-ch101, adc4

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

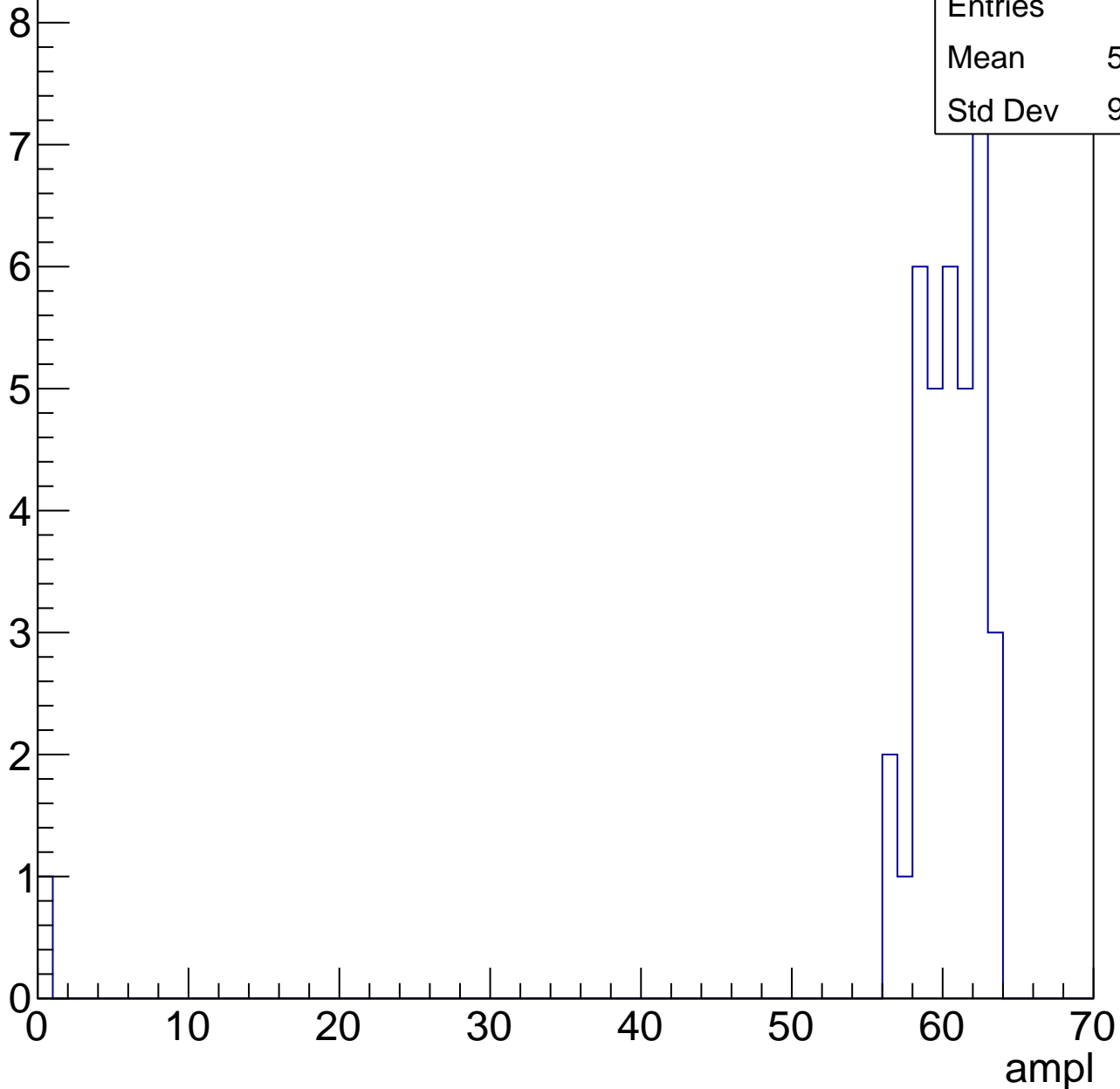


# B0L002S, U2-ch101, adc5

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	37
Mean	58.43
Std Dev	9.923



# B0L002S, U2-ch101, adc6

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

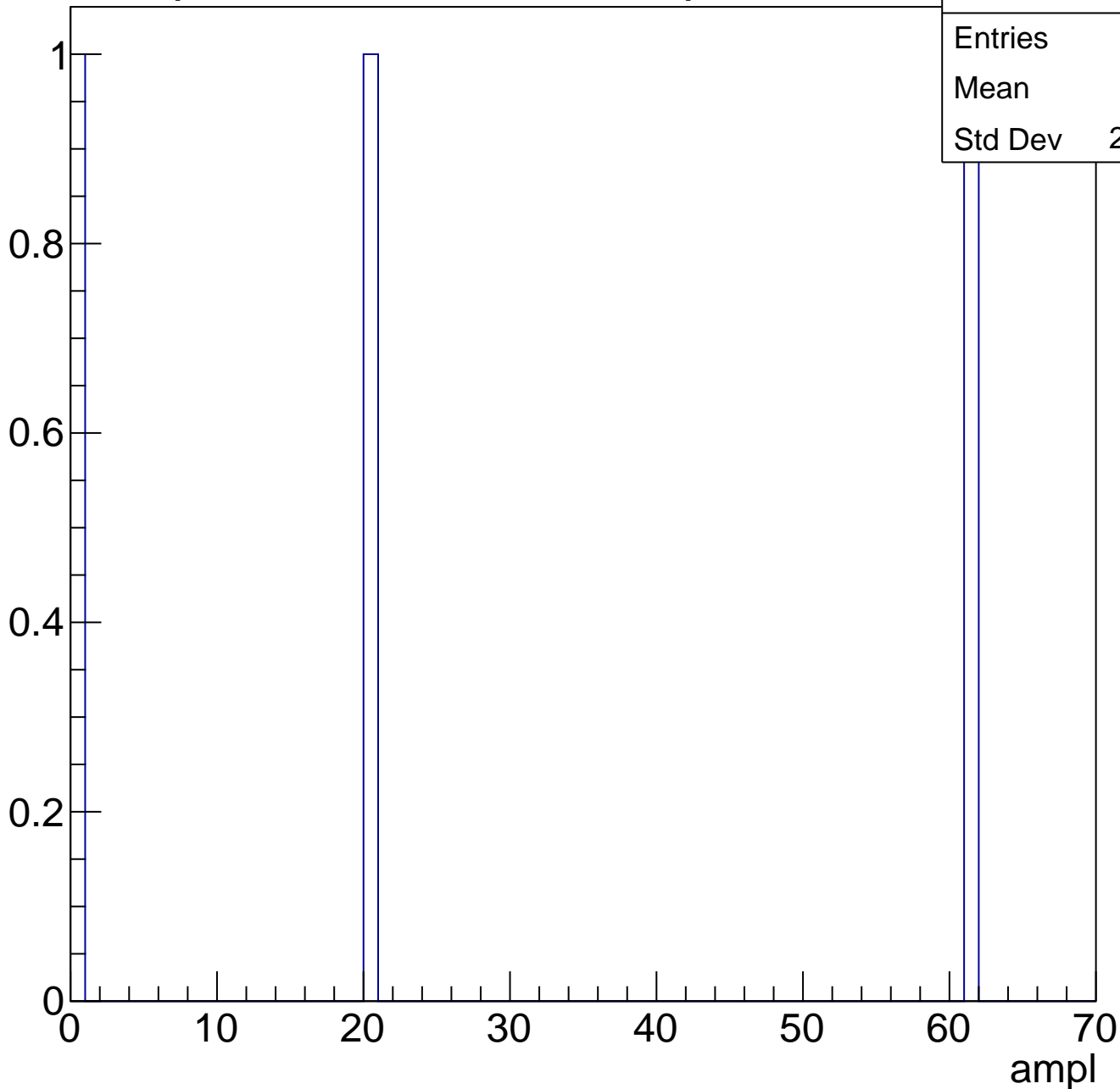




# B0L002S, U2-ch101, adc7

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



Entries	3
Mean	27
Std Dev	25.39

# B0L002S, U2-ch102, adc0

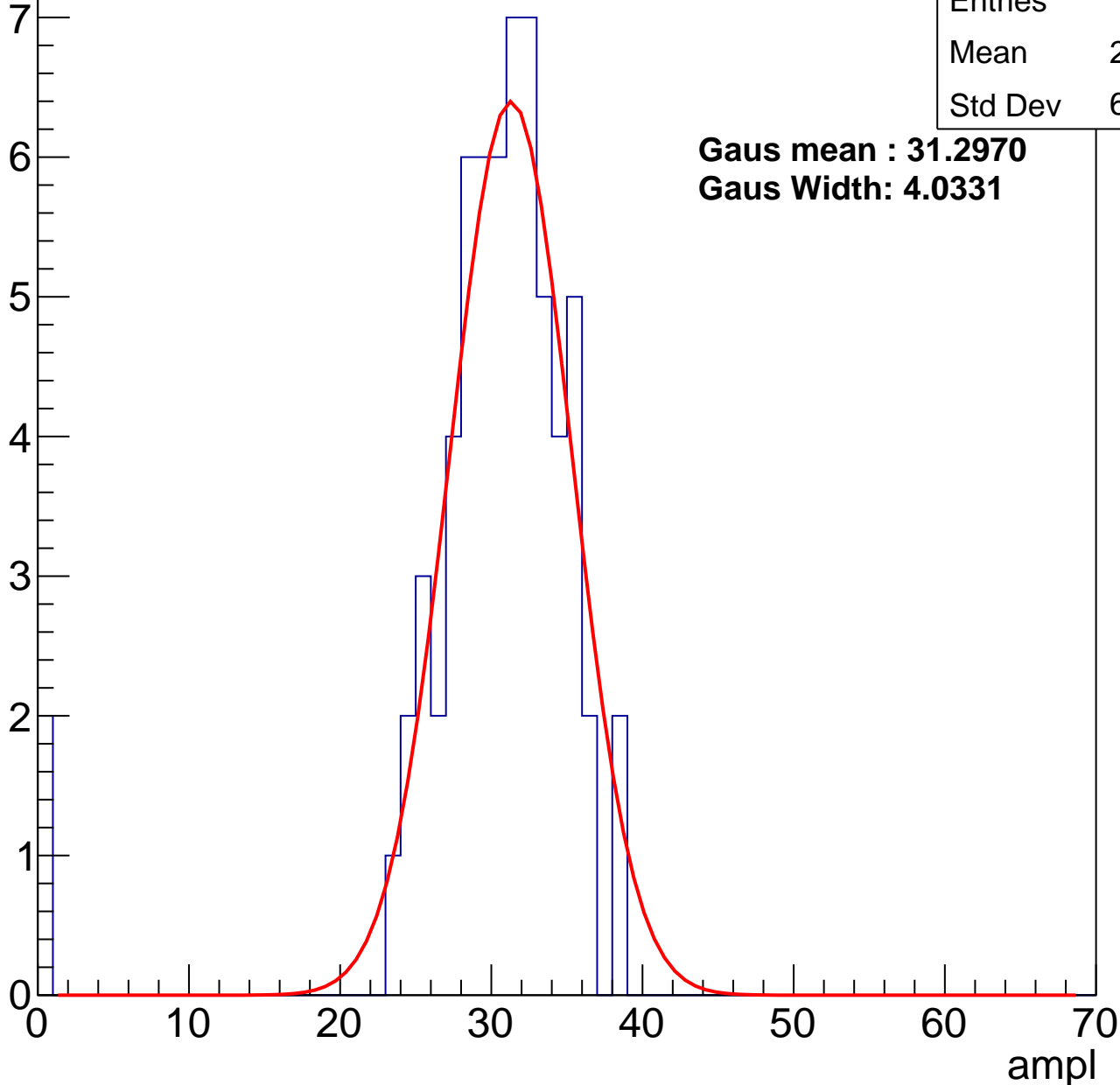
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	64
Mean	29.58
Std Dev	6.314

**Gaus mean : 31.2970**

**Gaus Width: 4.0331**



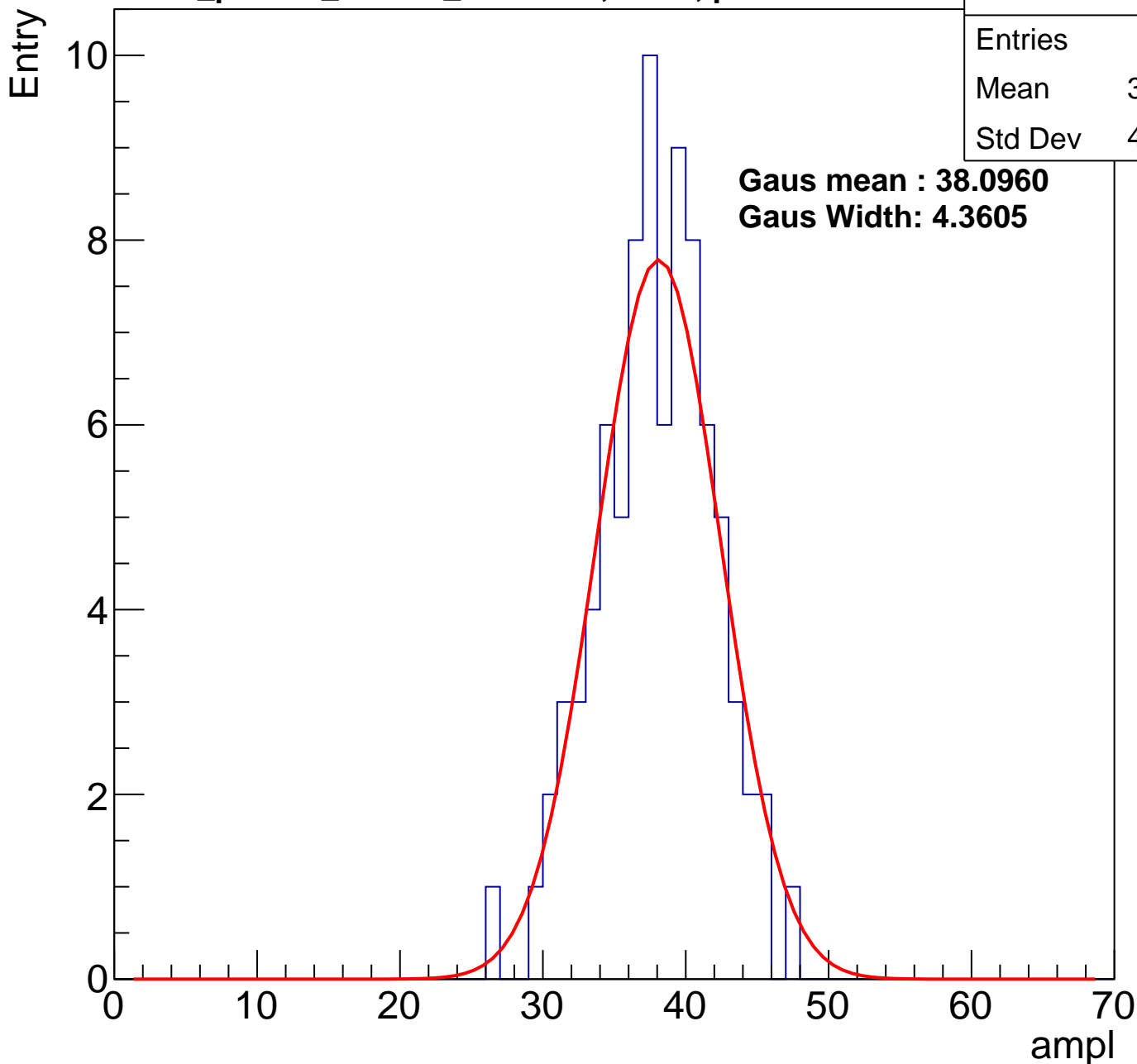
# B0L002S, U2-ch102, adc1

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entries	85
Mean	37.44
Std Dev	4.007

**Gaus mean : 38.0960**

**Gaus Width: 4.3605**



# B0L002S, U2-ch102, adc2

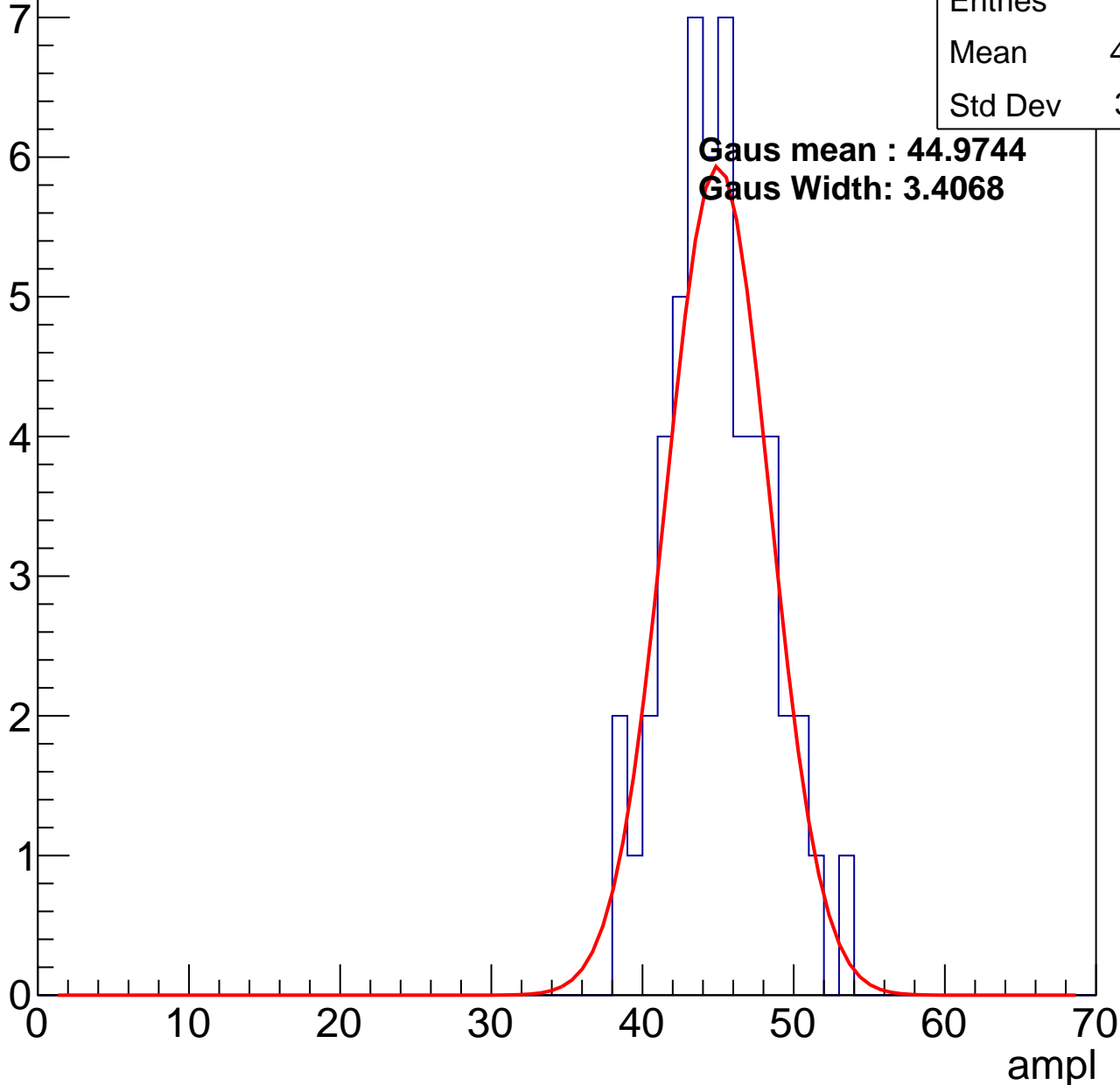
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	52
Mean	44.52
Std Dev	3.261

**Gaus mean : 44.9744**

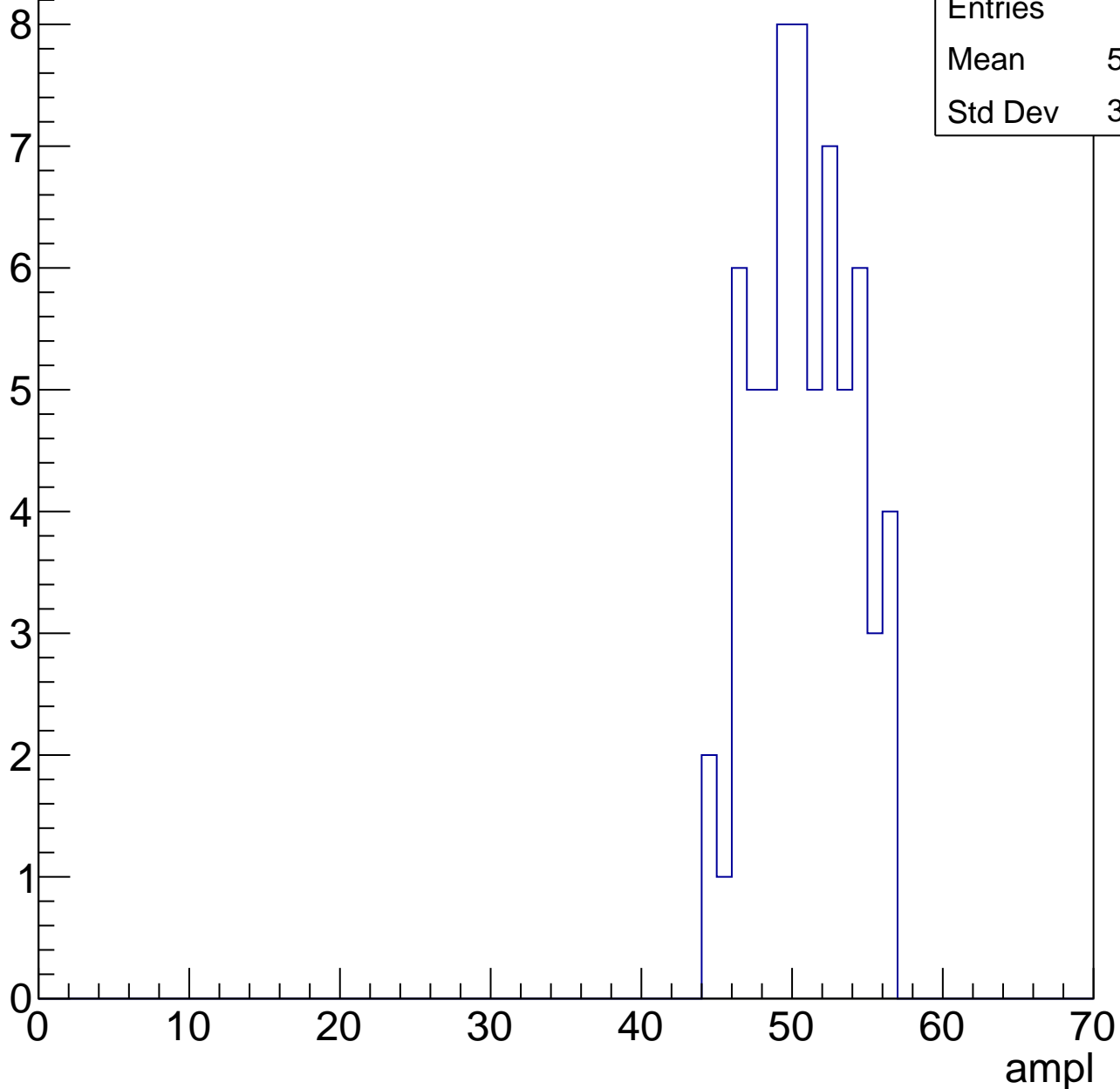
**Gaus Width: 3.4068**



# B0L002S, U2-ch102, adc3

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



Entries	65
Mean	50.35
Std Dev	3.164

# B0L002S, U2-ch102, adc4

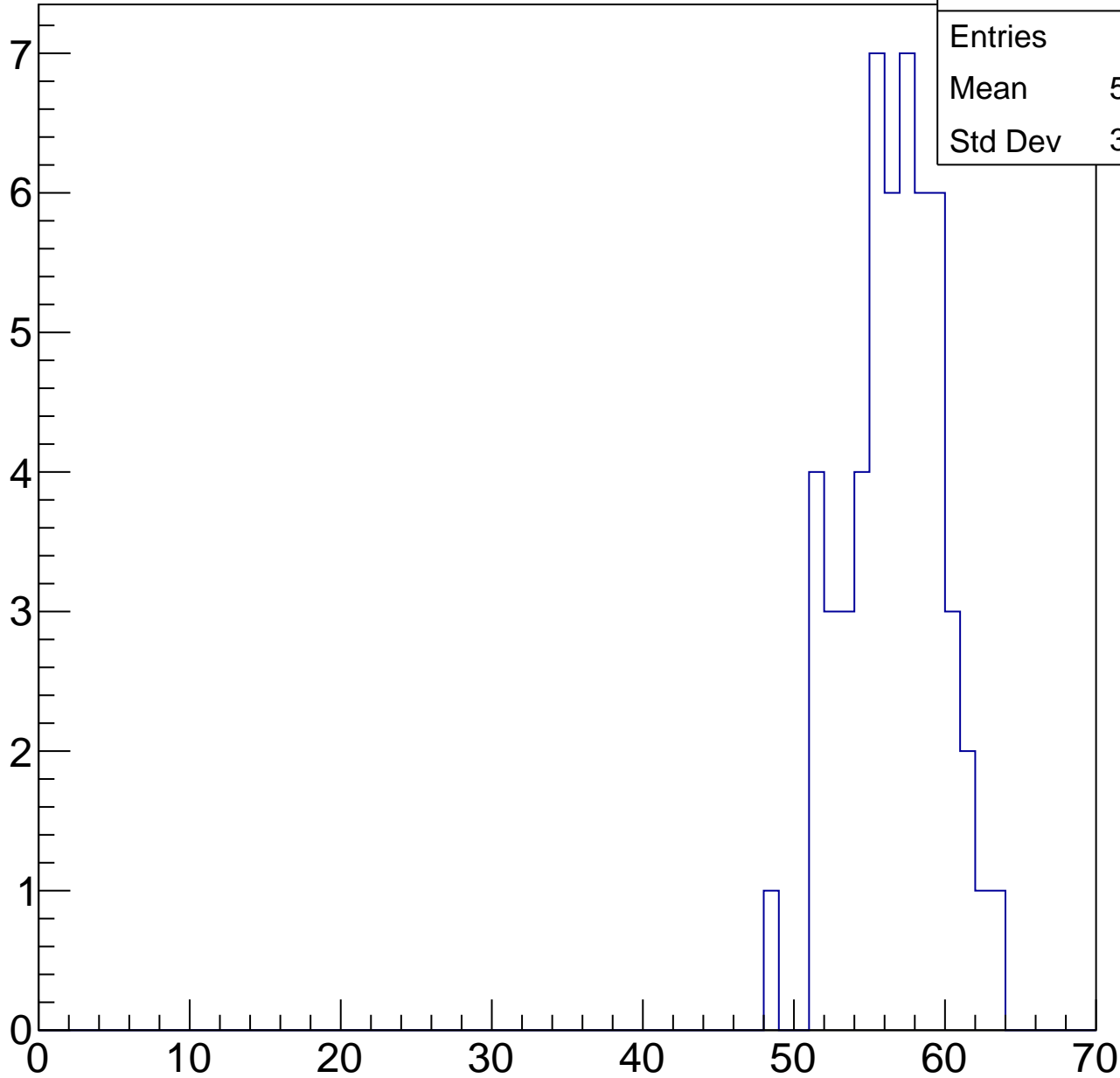
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

7  
6  
5  
4  
3  
2  
1  
0

Entries	54
Mean	56.15
Std Dev	3.129

ampl

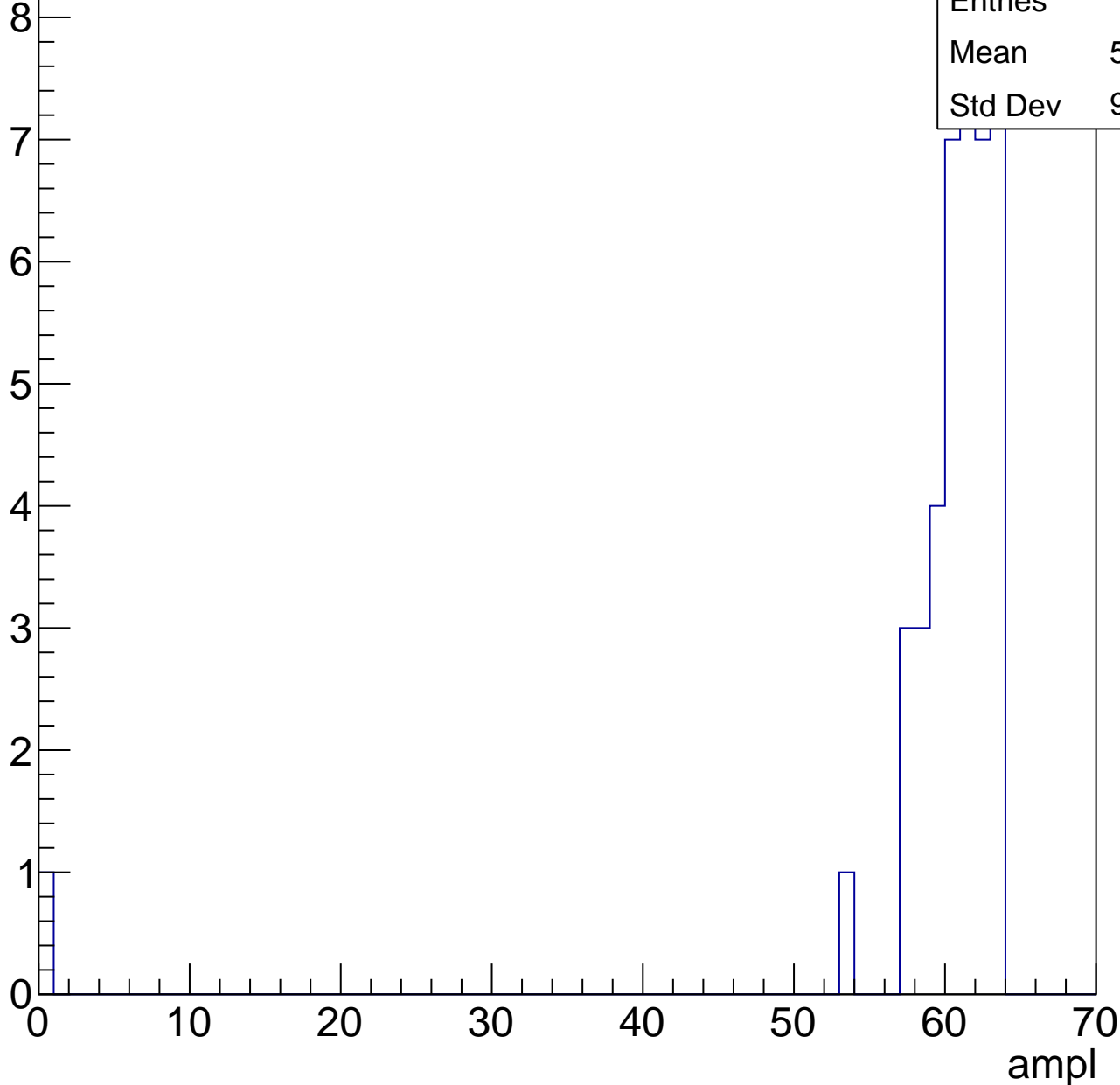


# B0L002S, U2-ch102, adc5

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

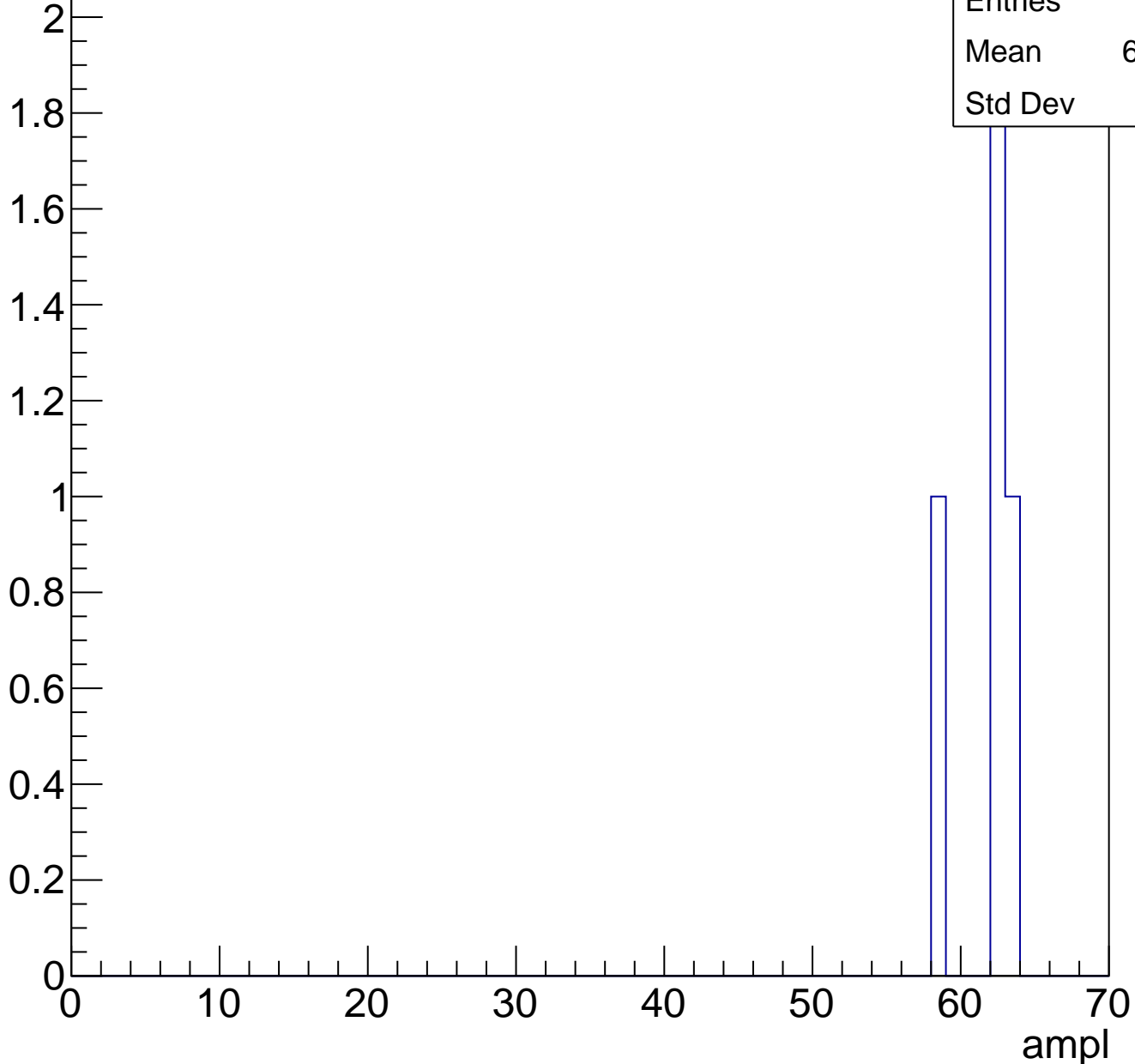
Entries	42
Mean	59.05
Std Dev	9.464



# B0L002S, U2-ch102, adc6

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry





# B0L002S, U2-ch102, adc7

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



Entries	3
Mean	0
Std Dev	0

# B0L002S, U2-ch103, adc0

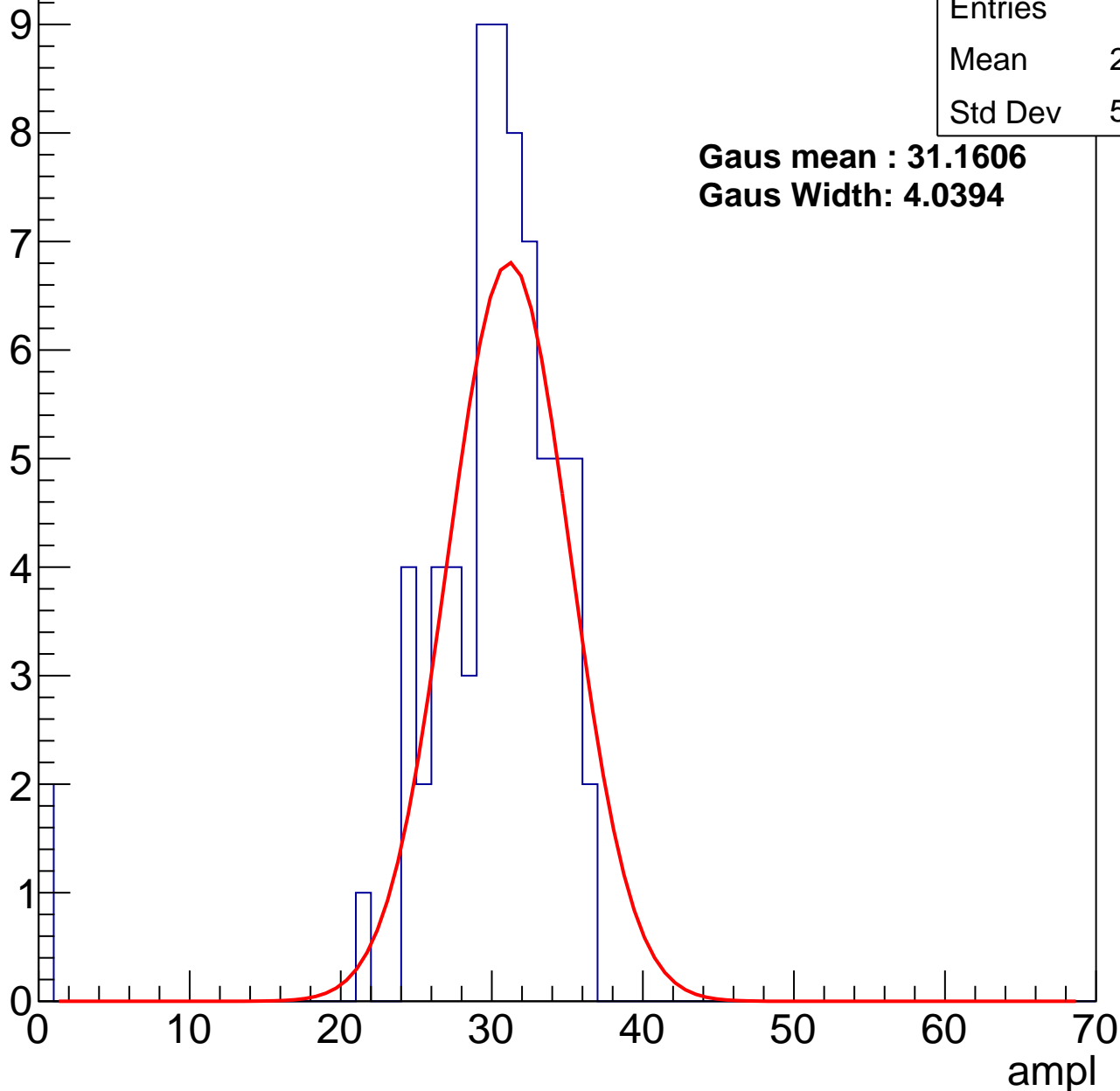
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	70
Mean	29.26
Std Dev	5.994

**Gaus mean : 31.1606**

**Gaus Width: 4.0394**



# B0L002S, U2-ch103, adc1

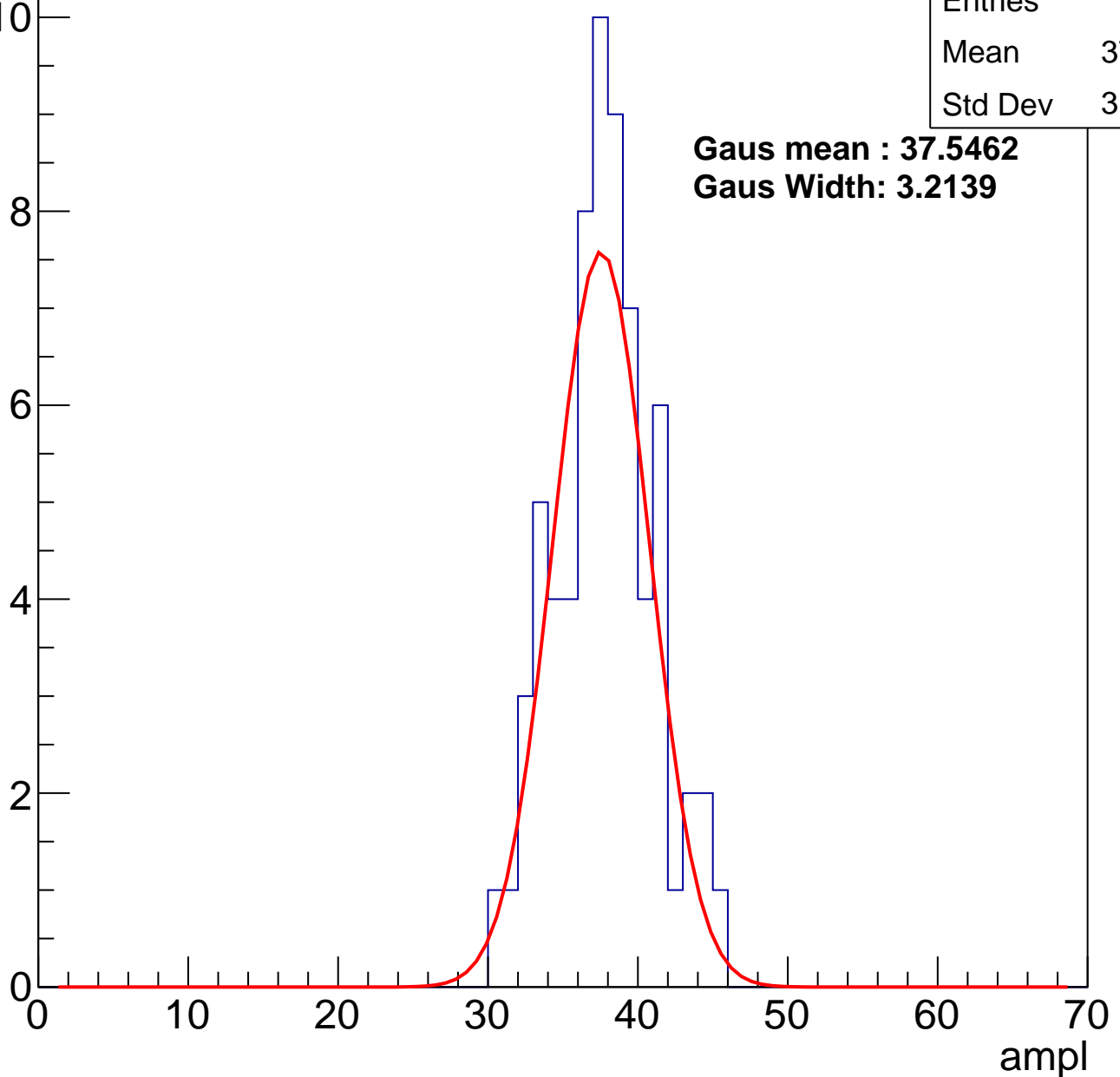
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	68
Mean	37.32
Std Dev	3.256

**Gaus mean : 37.5462**

**Gaus Width: 3.2139**



# B0L002S, U2-ch103, adc2

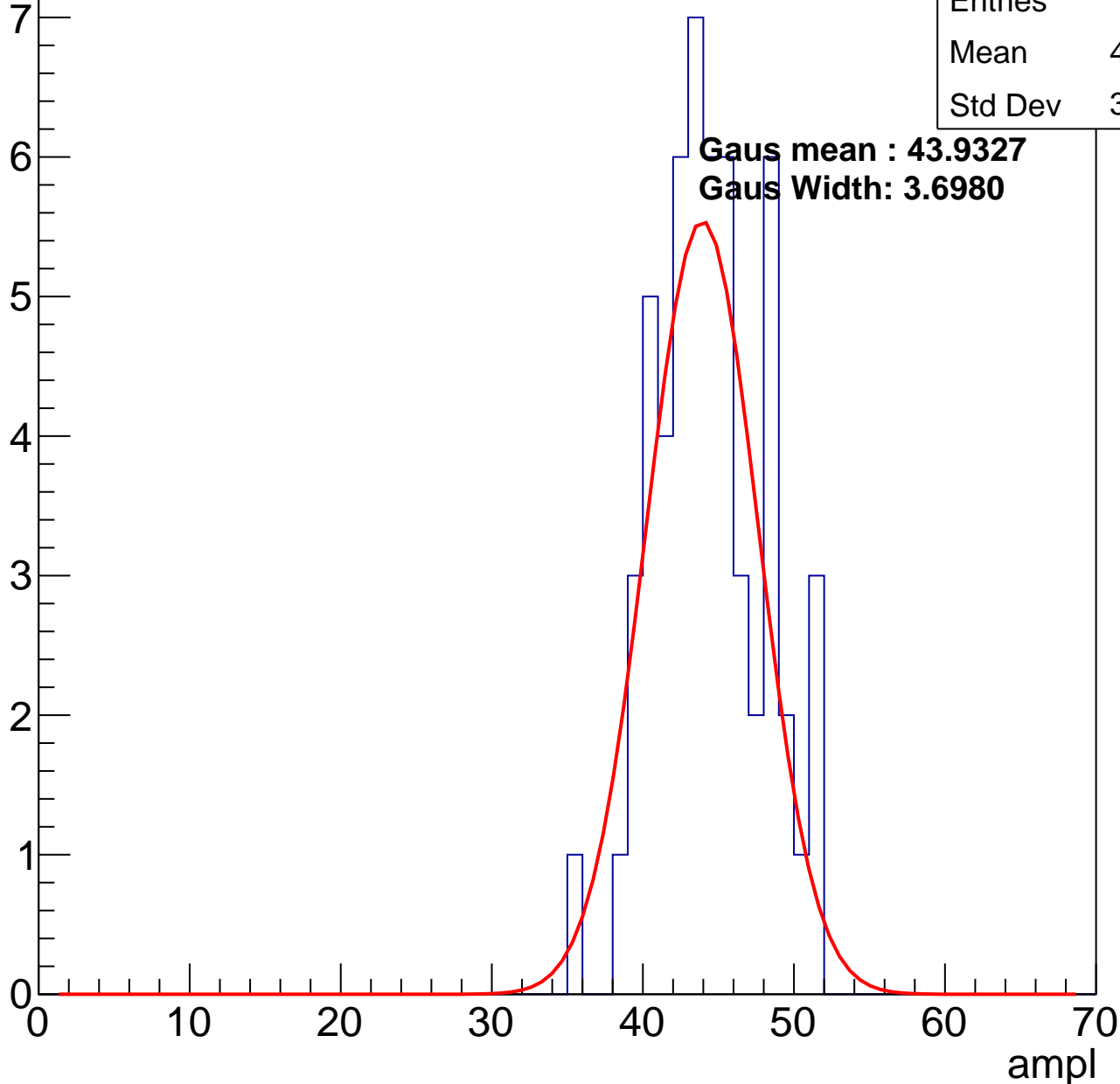
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	56
Mean	43.96
Std Dev	3.545

**Gaus mean : 43.9327**

**Gaus Width: 3.6980**

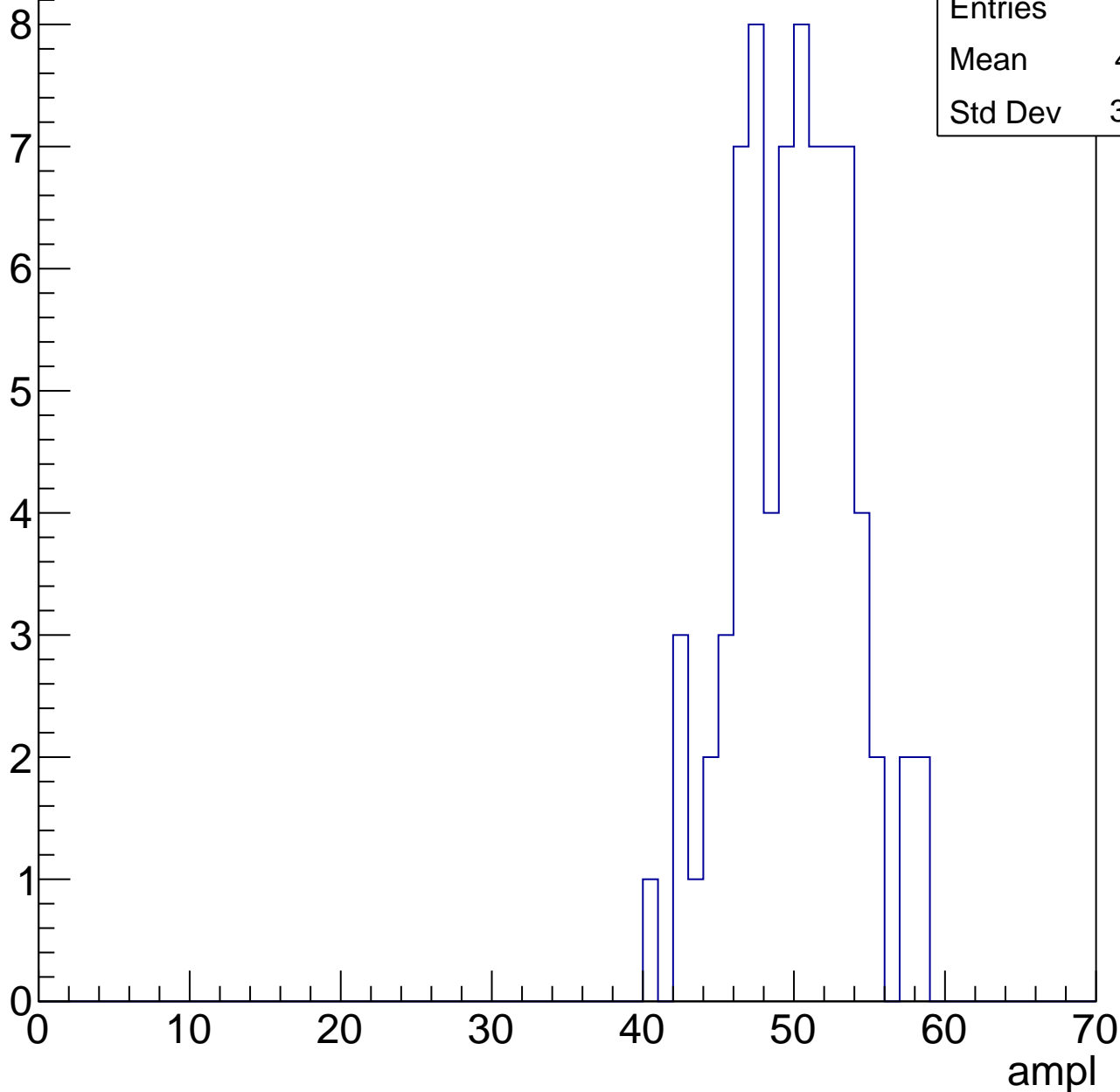


# B0L002S, U2-ch103, adc3

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	75
Mean	49.51
Std Dev	3.855

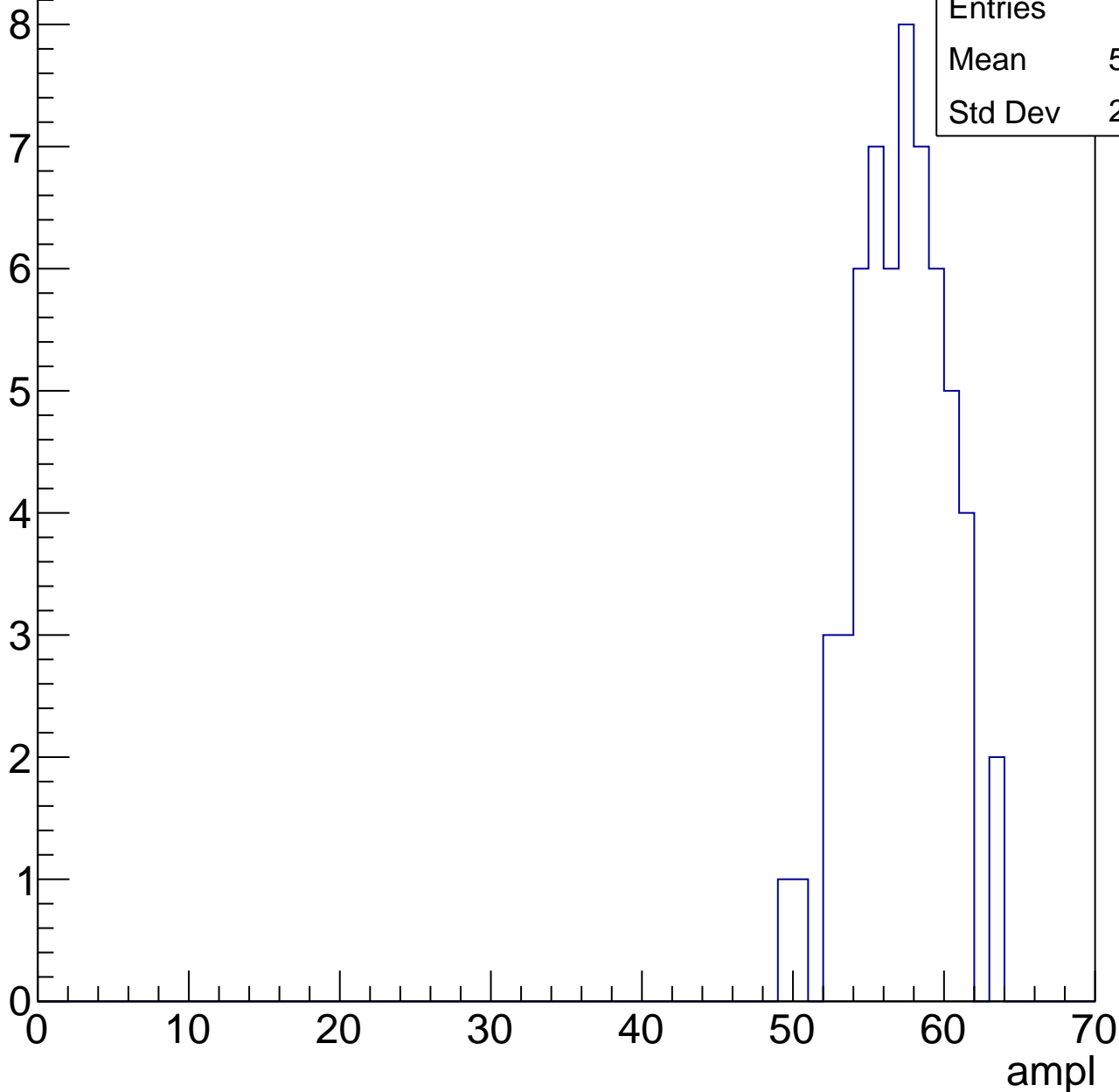


# B0L002S, U2-ch103, adc4

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	59
Mean	56.69
Std Dev	2.999

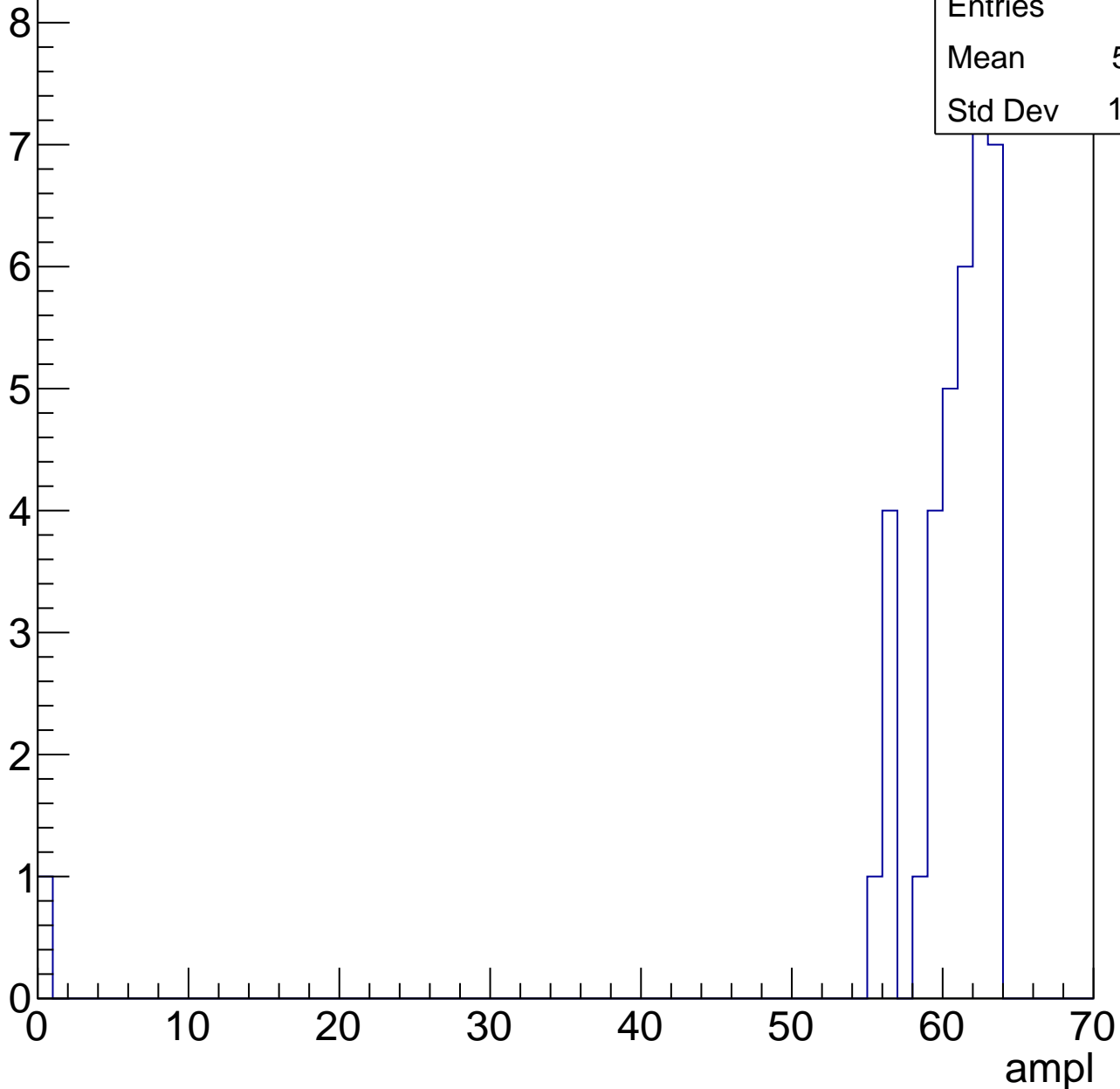


# B0L002S, U2-ch103, adc5

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	37
Mean	58.81
Std Dev	10.06



# B0L002S, U2-ch103, adc6

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	3
Mean	62.33
Std Dev	0.4714

ampl

0 10 20 30 40 50 60 70



# B0L002S, U2-ch103, adc7

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L002S, U2-ch104, adc0

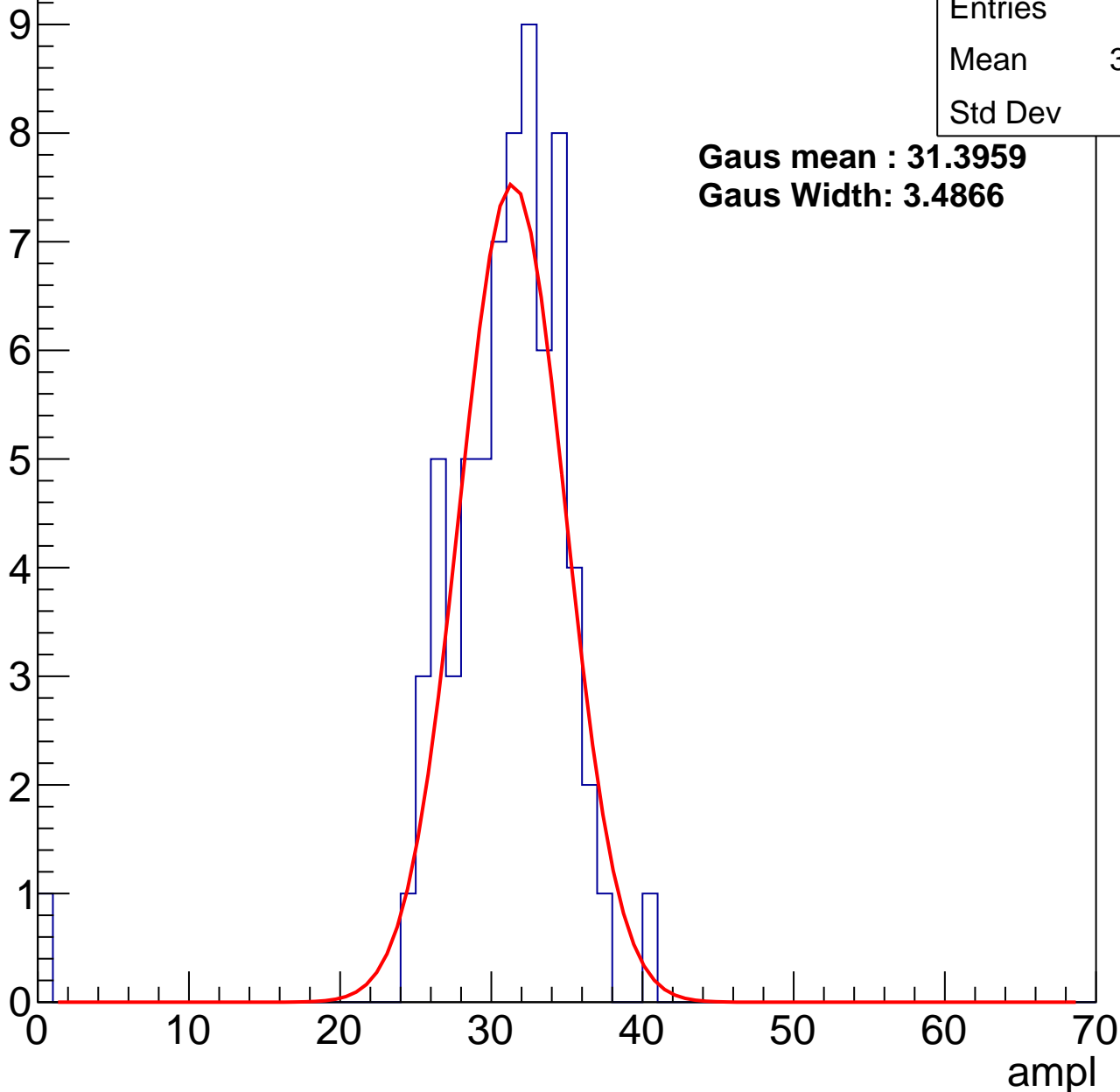
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	69
Mean	30.43
Std Dev	4.93

**Gaus mean : 31.3959**

**Gaus Width: 3.4866**



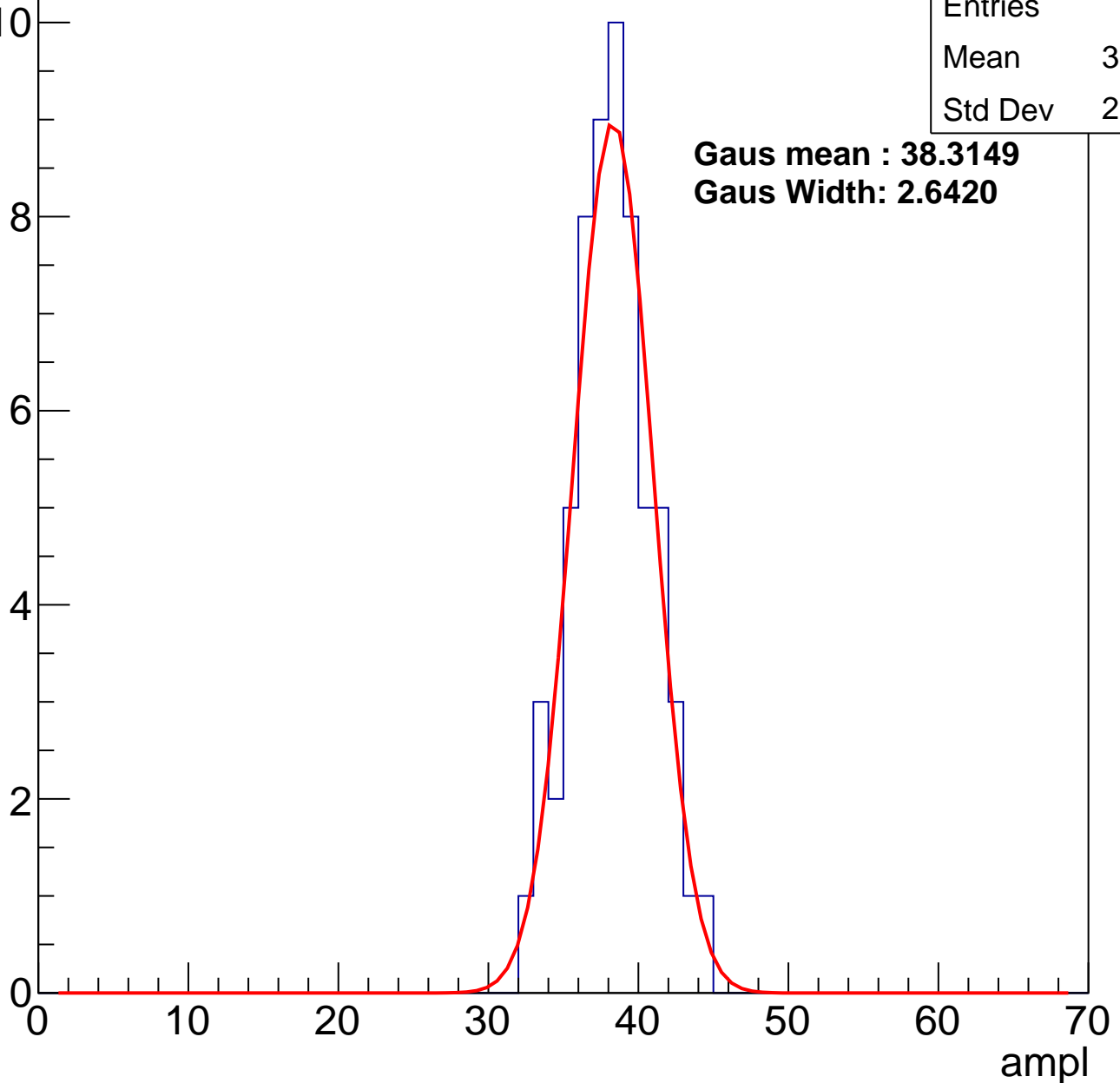
# B0L002S, U2-ch104, adc1

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	61
Mean	37.79
Std Dev	2.587

**Gaus mean : 38.3149**  
**Gaus Width: 2.6420**



# B0L002S, U2-ch104, adc2

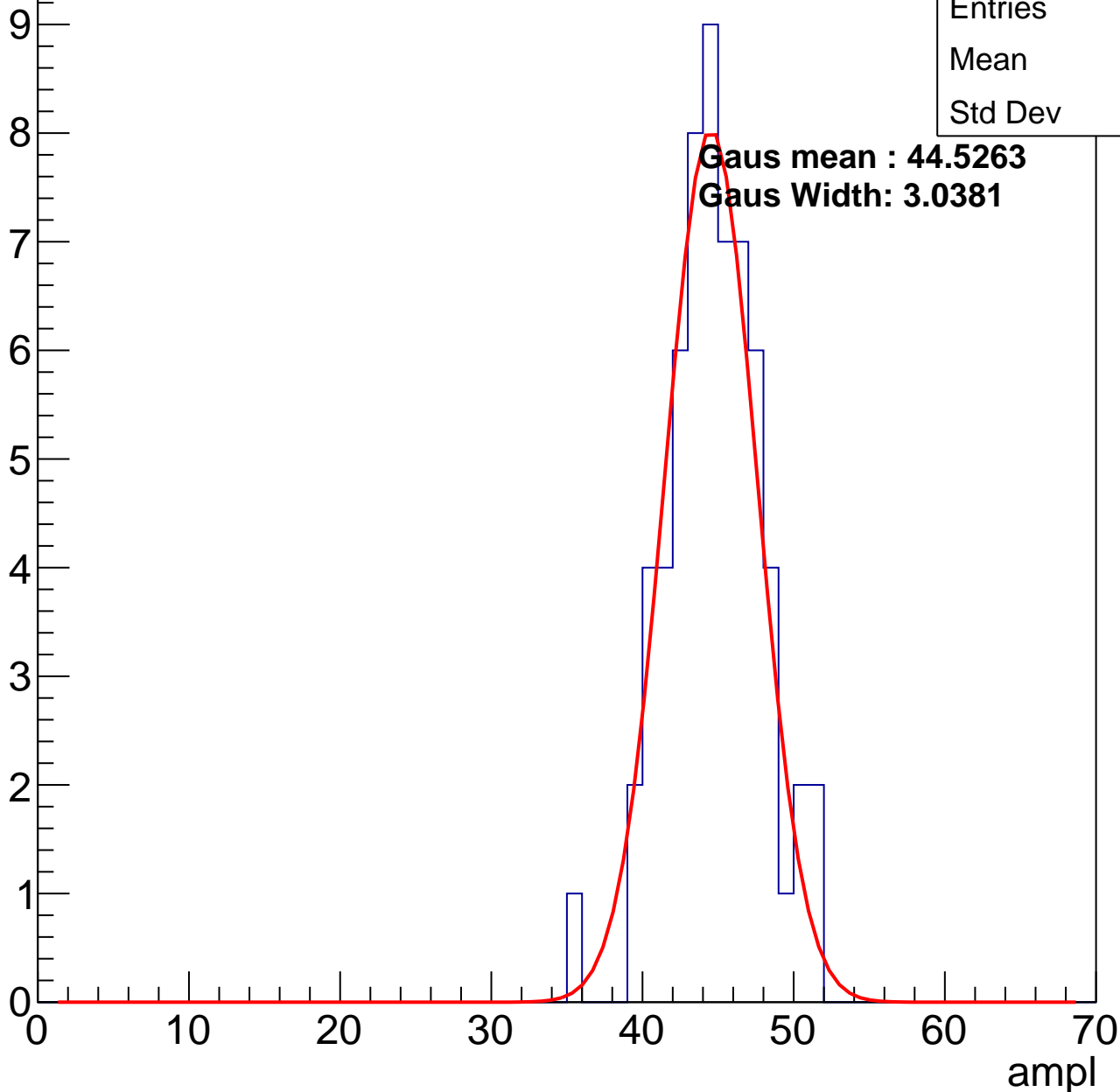
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	63
Mean	44.3
Std Dev	3.1

**Gaus mean : 44.5263**

**Gaus Width: 3.0381**

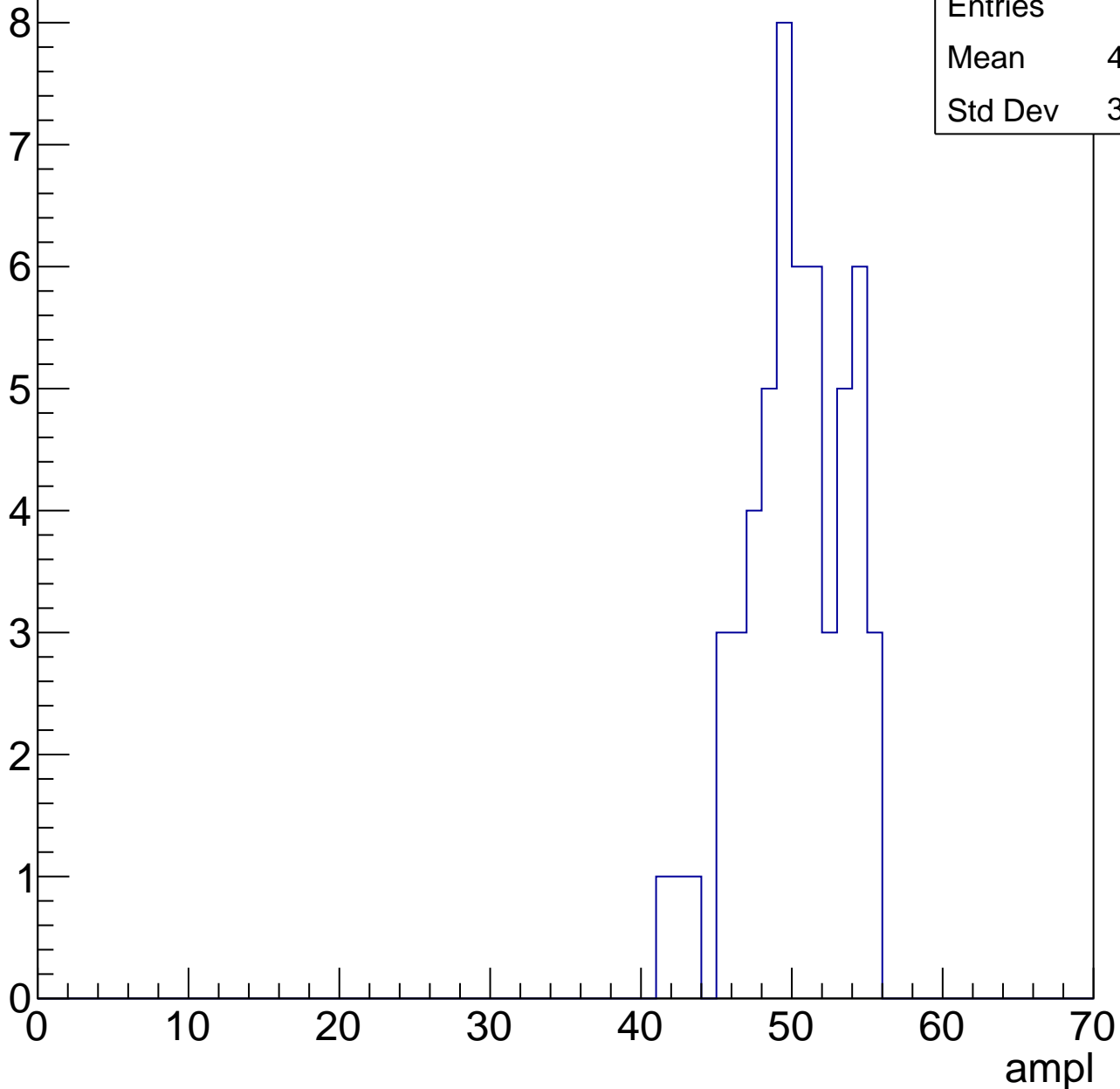


# B0L002S, U2-ch104, adc3

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	55
Mean	49.73
Std Dev	3.333



# B0L002S, U2-ch104, adc4

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entries	67
Mean	55.96
Std Dev	3.436

Entry

10

8

6

4

2

0

0

10

20

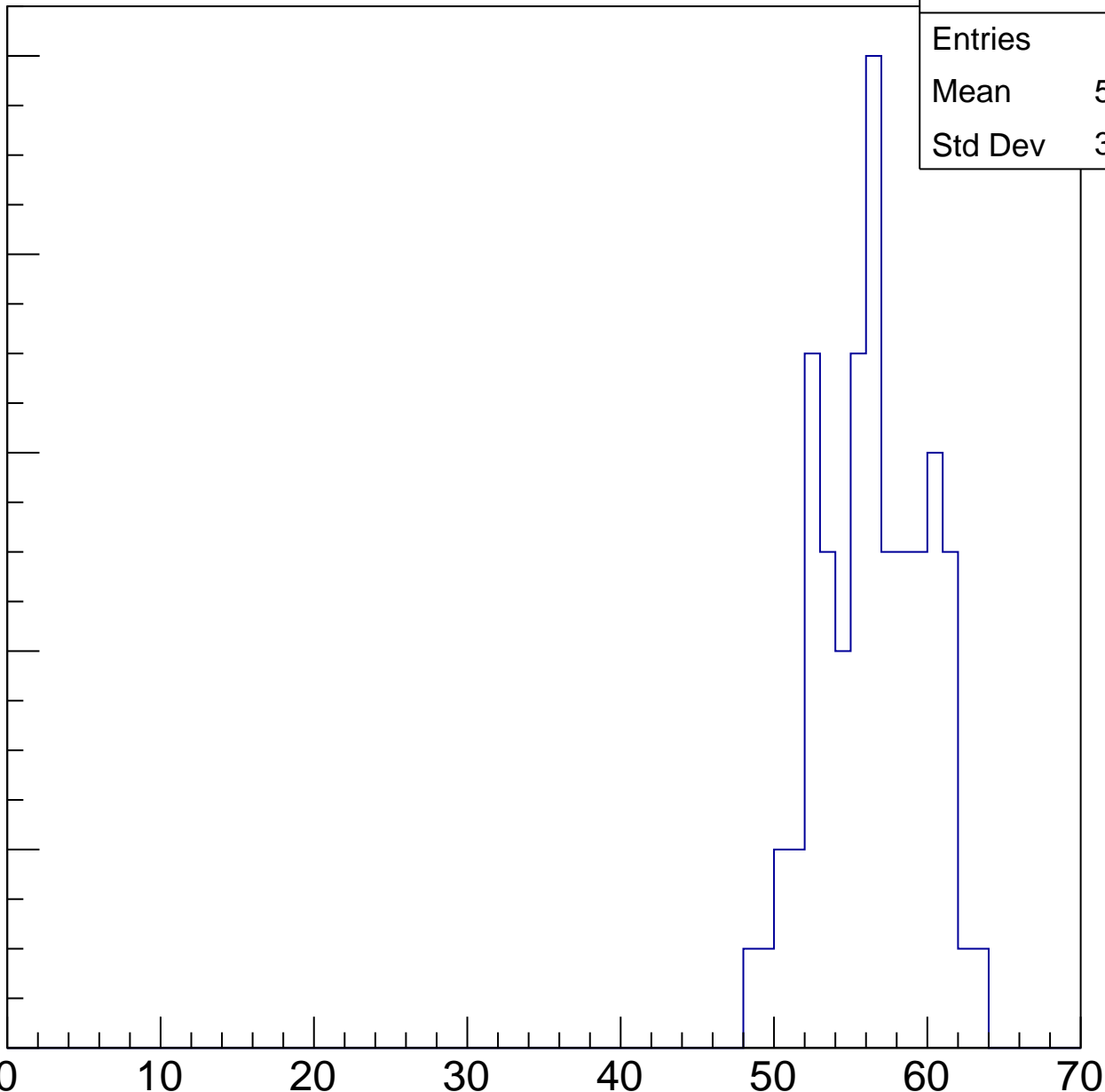
30

40

50

60

ampl

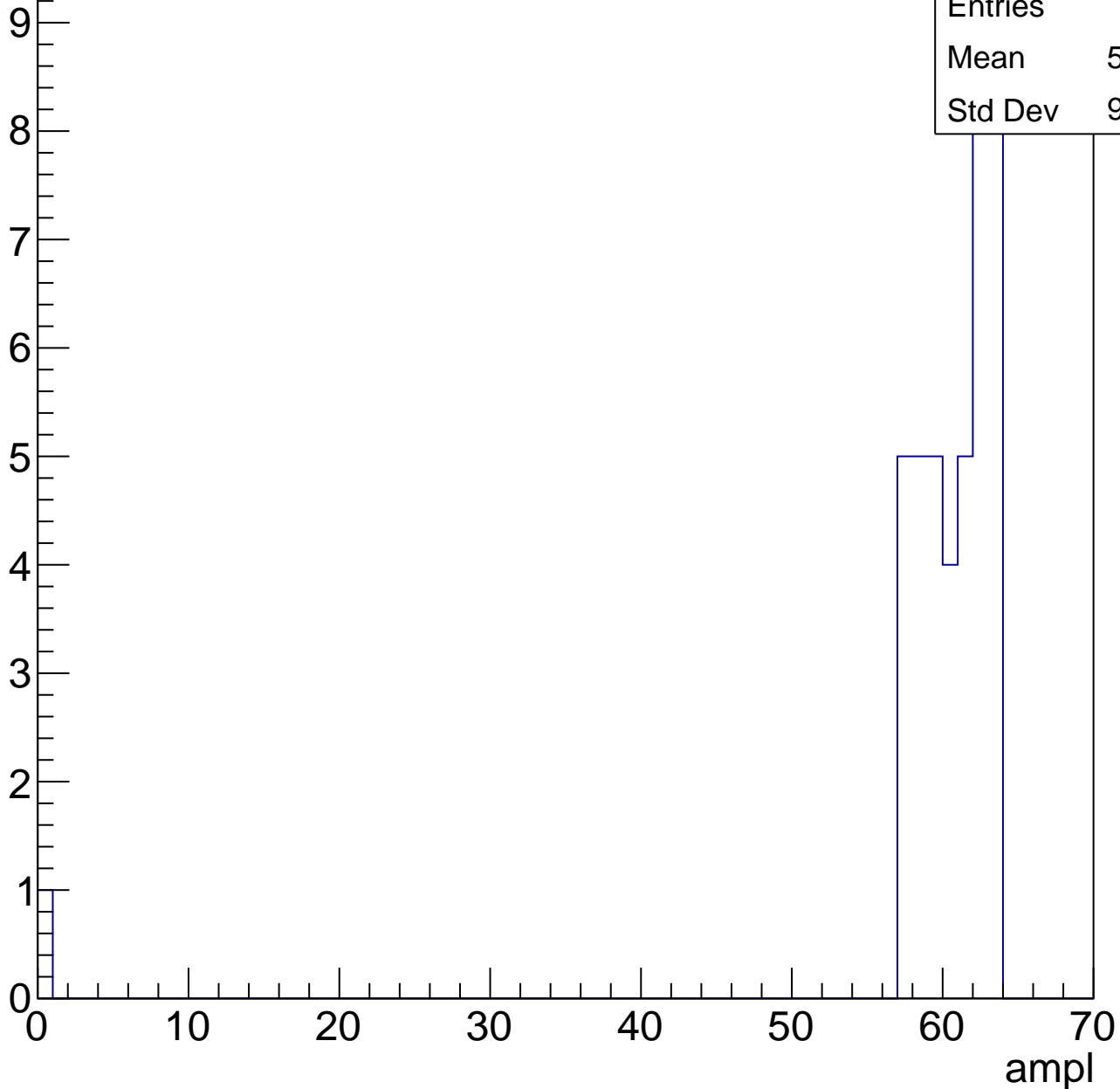


# B0L002S, U2-ch104, adc5

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	43
Mean	59.07
Std Dev	9.345



# B0L002S, U2-ch104, adc6

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



Entries	0
Mean	0
Std Dev	0



# B0L002S, U2-ch104, adc7

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



Entries	3
Mean	0
Std Dev	0

# B0L002S, U2-ch105, adc0

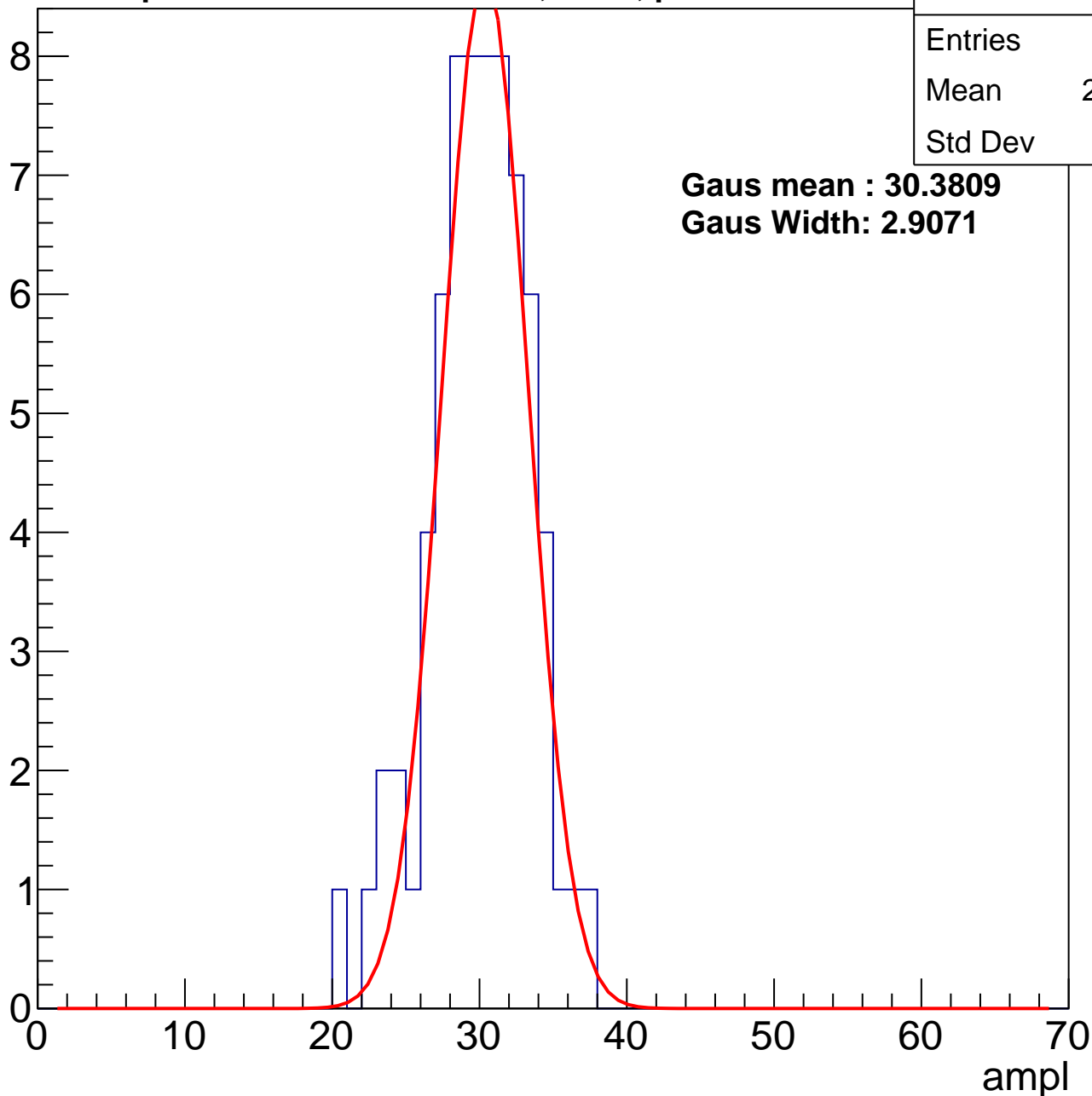
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	69
Mean	29.52
Std Dev	3.33

**Gaus mean : 30.3809**

**Gaus Width: 2.9071**



# B0L002S, U2-ch105, adc1

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entries	72
Mean	37.21
Std Dev	3.337

**Gaus mean : 37.7679**

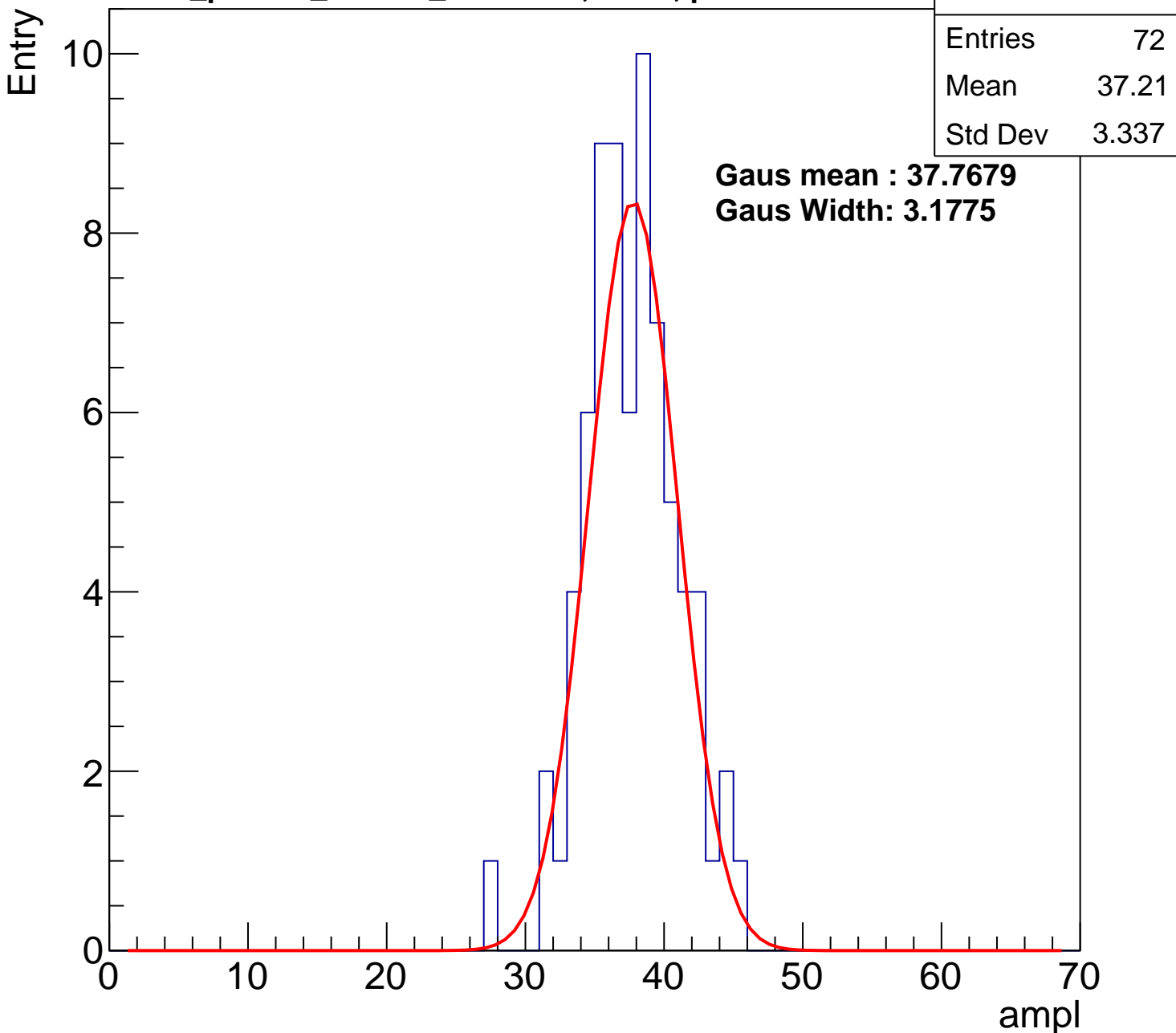
**Gaus Width: 3.1775**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L002S, U2-ch105, adc2

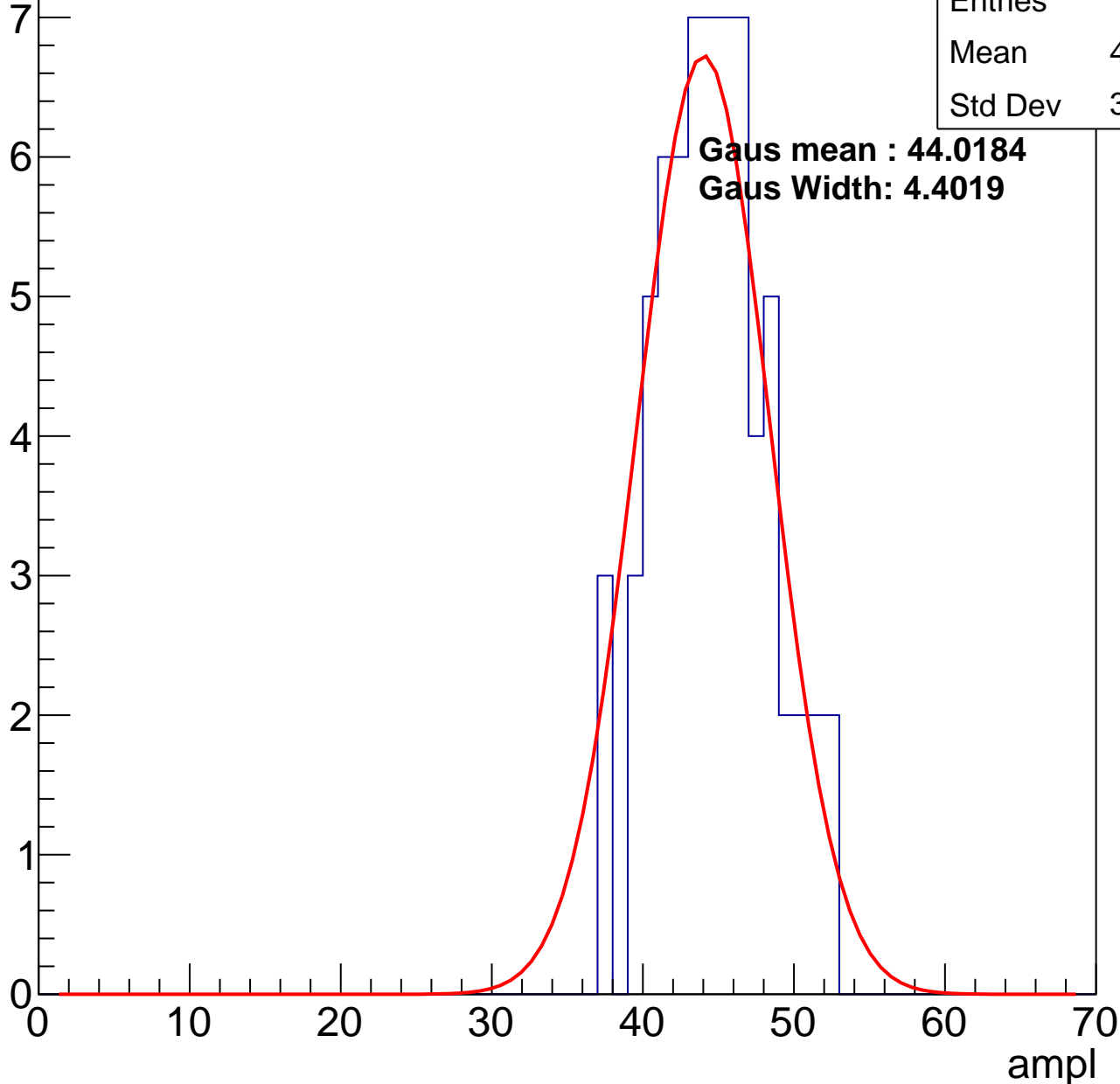
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	68
Mean	44.18
Std Dev	3.605

**Gaus mean : 44.0184**

**Gaus Width: 4.4019**

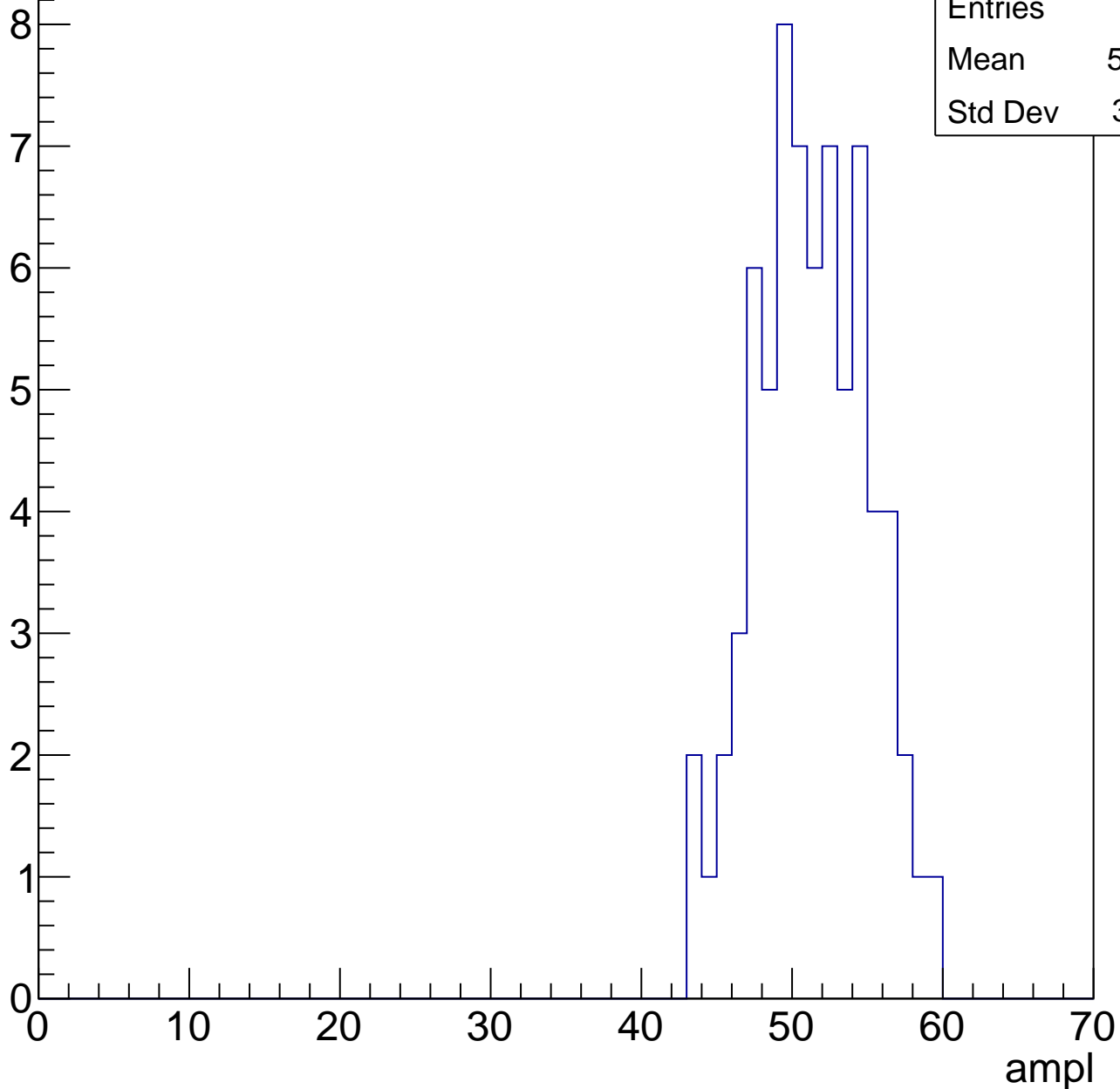


# B0L002S, U2-ch105, adc3

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	71
Mean	50.85
Std Dev	3.641

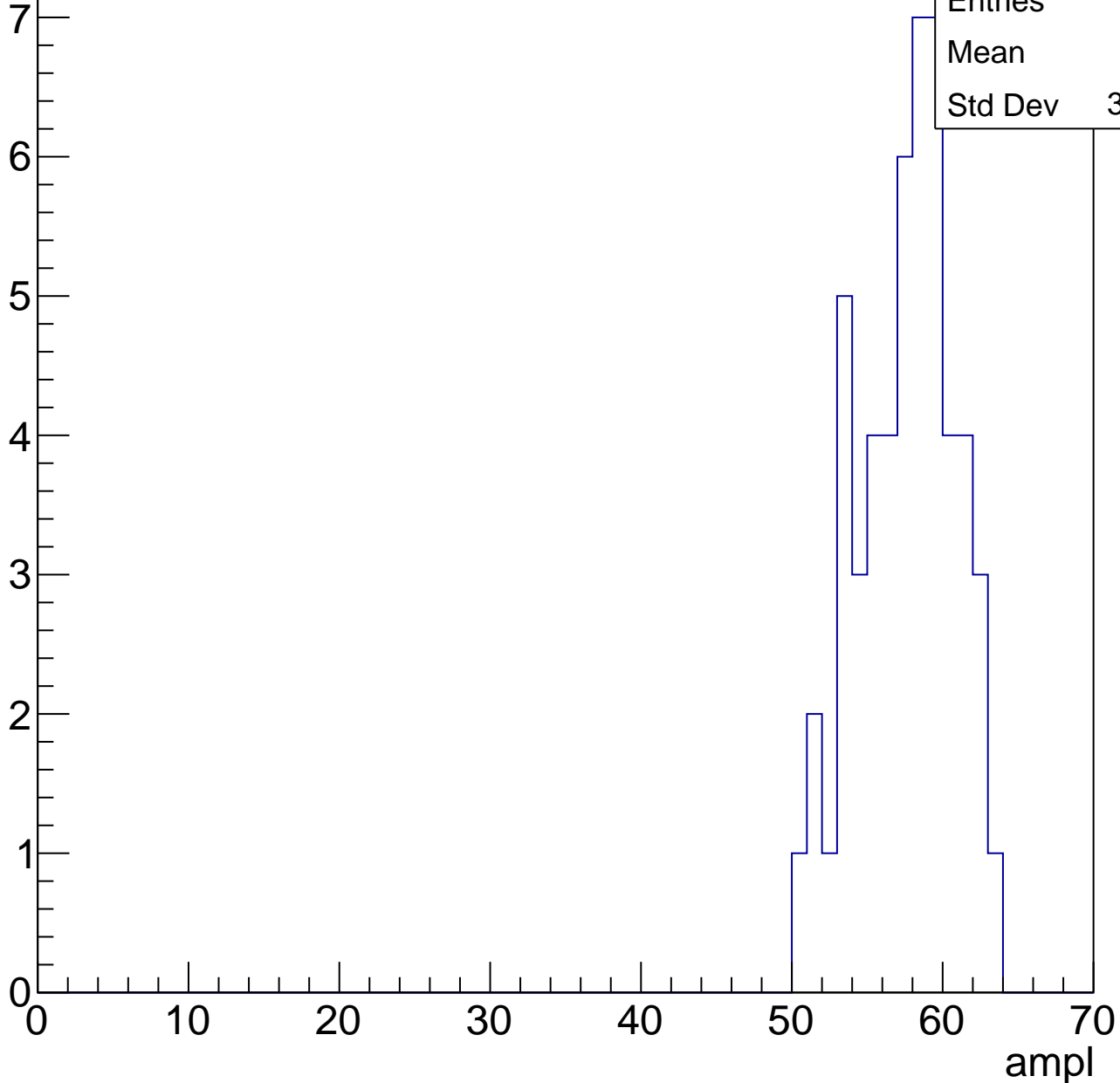


# B0L002S, U2-ch105, adc4

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	52
Mean	57.1
Std Dev	3.158

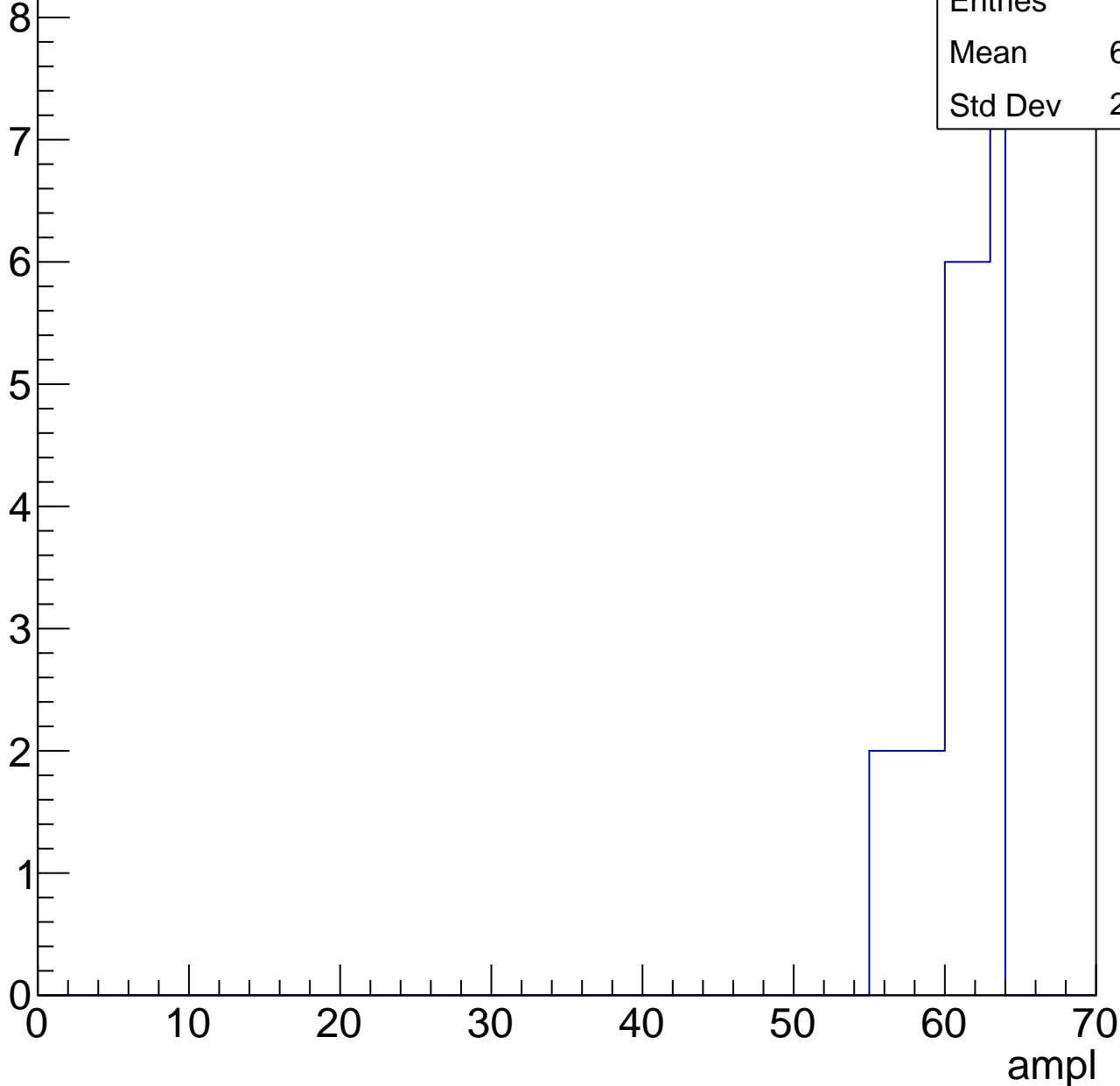


# B0L002S, U2-ch105, adc5

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

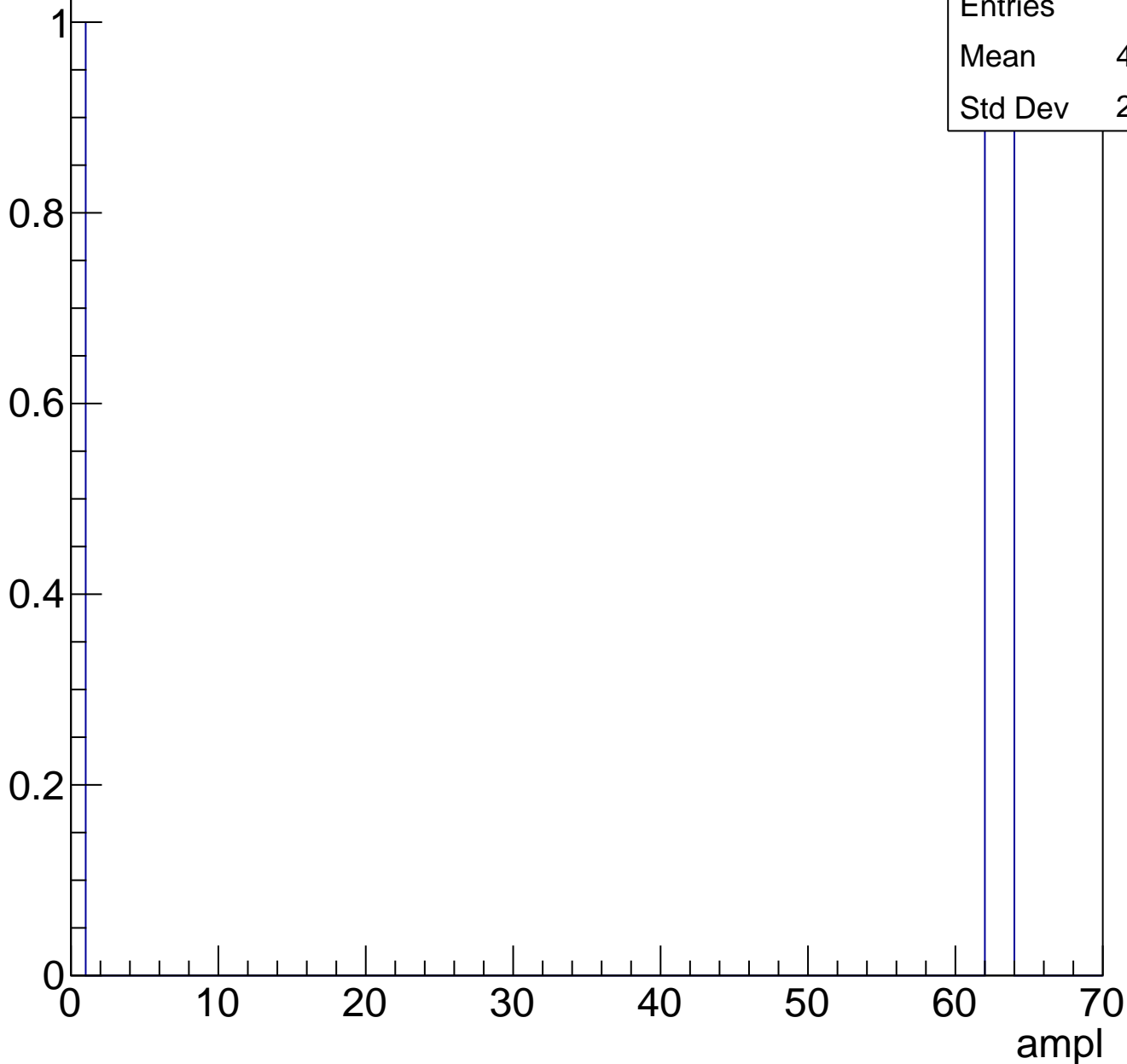
Entries	36
Mean	60.33
Std Dev	2.404



# B0L002S, U2-ch105, adc6

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry





# B0L002S, U2-ch105, adc7

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L002S, U2-ch106, adc0

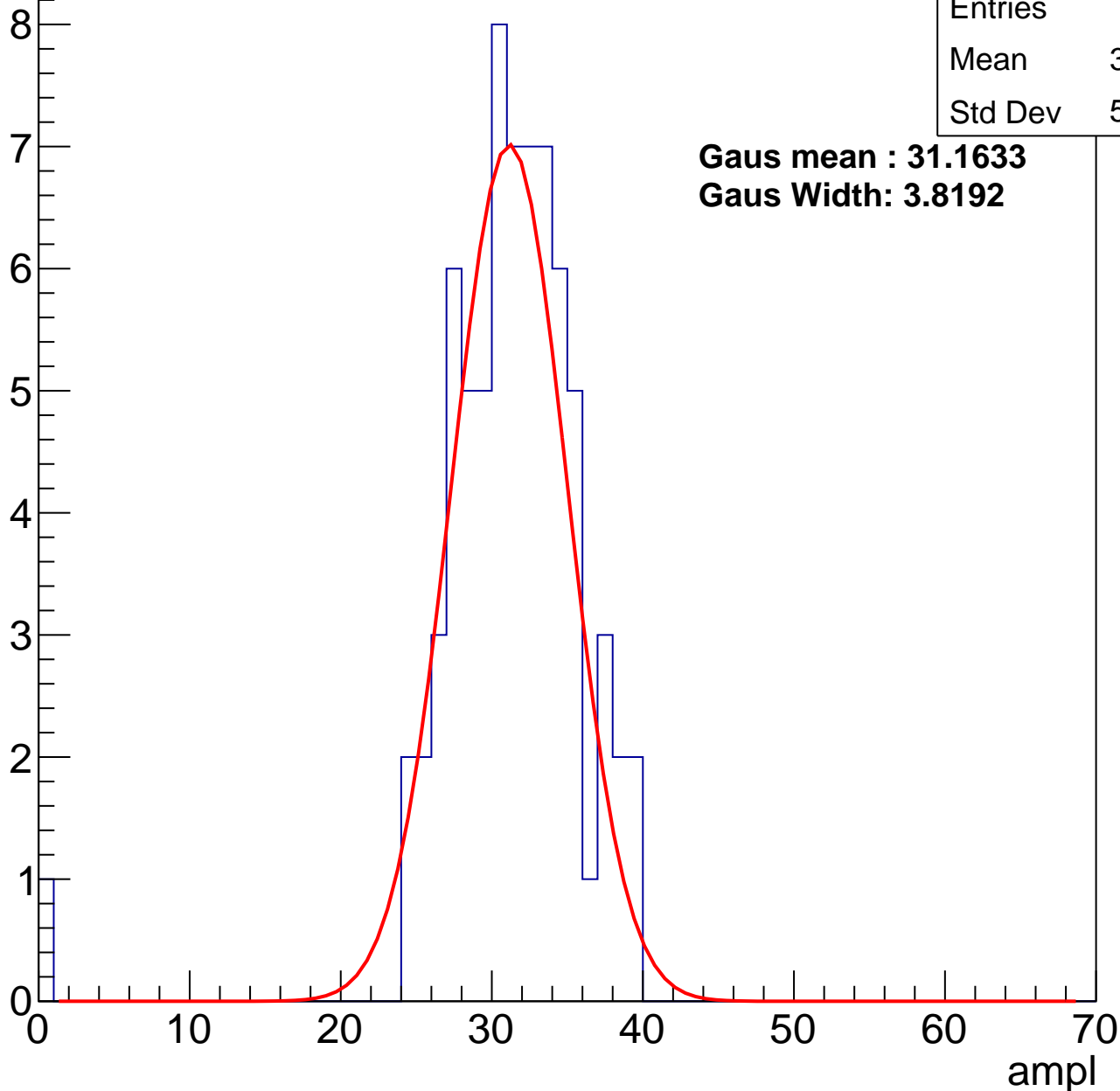
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	72
Mean	30.76
Std Dev	5.136

**Gaus mean : 31.1633**

**Gaus Width: 3.8192**



# B0L002S, U2-ch106, adc1

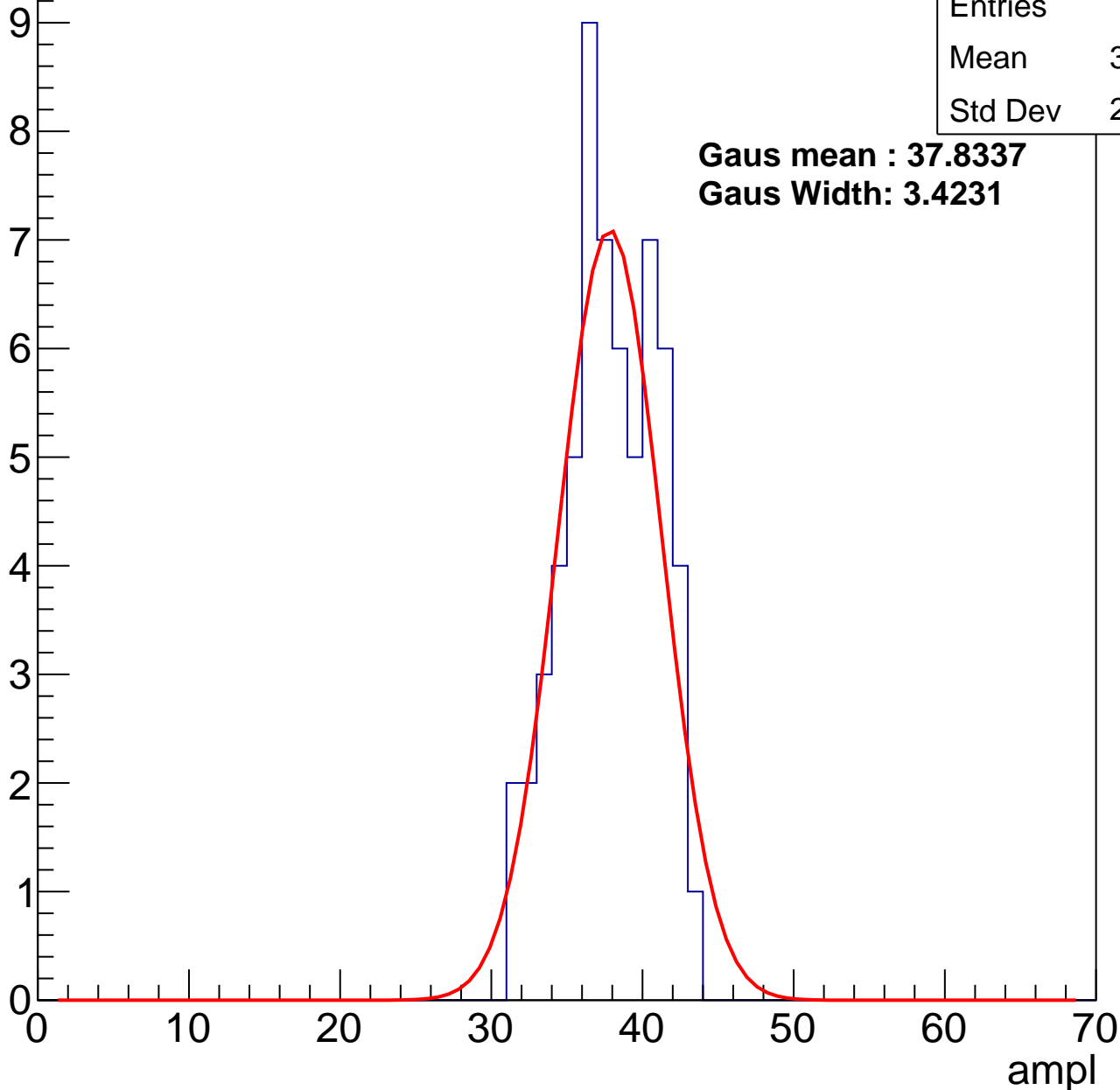
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	61
Mean	37.36
Std Dev	2.997

**Gaus mean : 37.8337**

**Gaus Width: 3.4231**



# B0L002S, U2-ch106, adc2

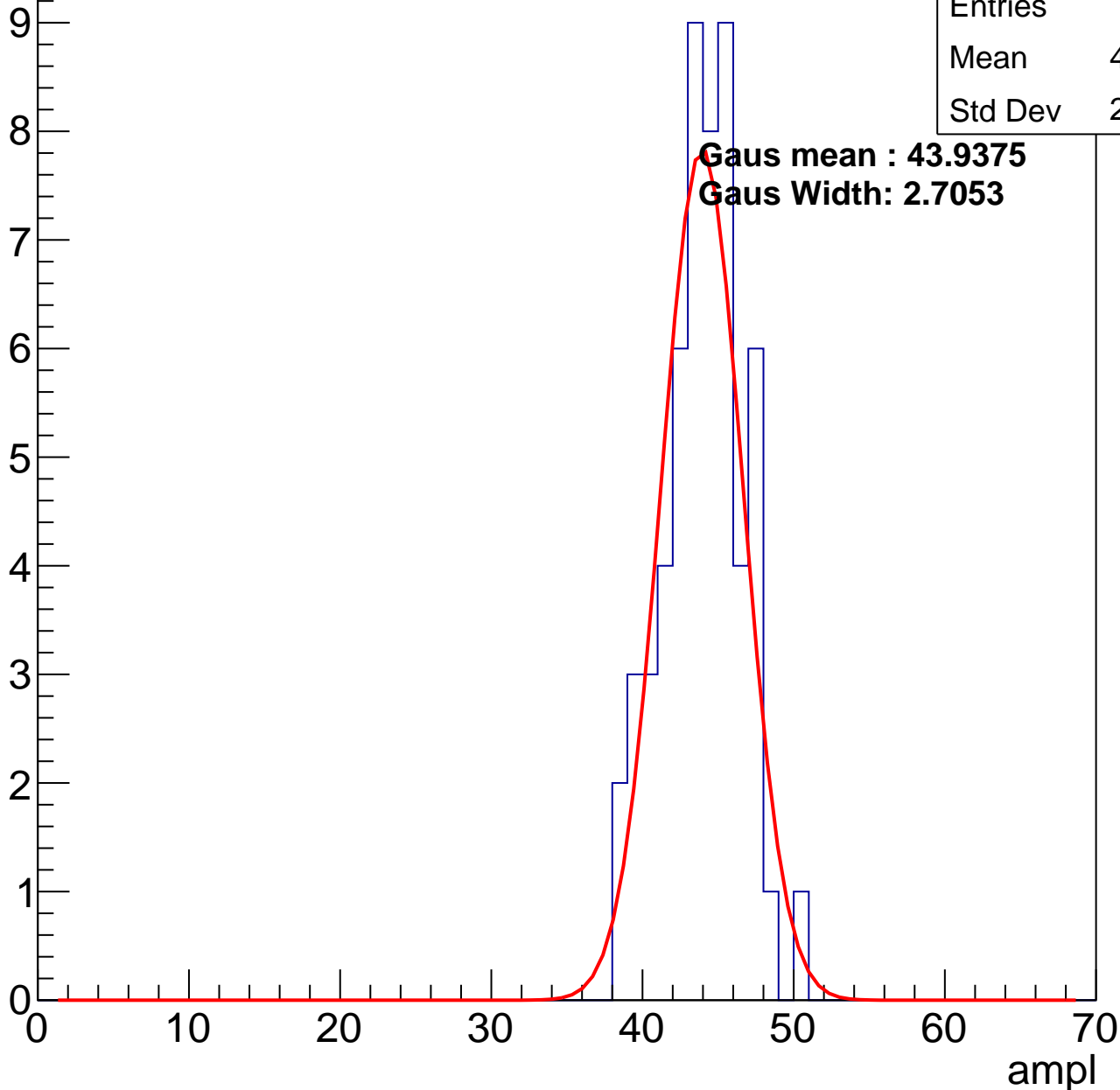
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	56
Mean	43.52
Std Dev	2.612

**Gaus mean : 43.9375**

**Gaus Width: 2.7053**



# B0L002S, U2-ch106, adc3

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entries	81
Mean	50.81
Std Dev	3.244

Entry

10

8

6

4

2

0

0

10

20

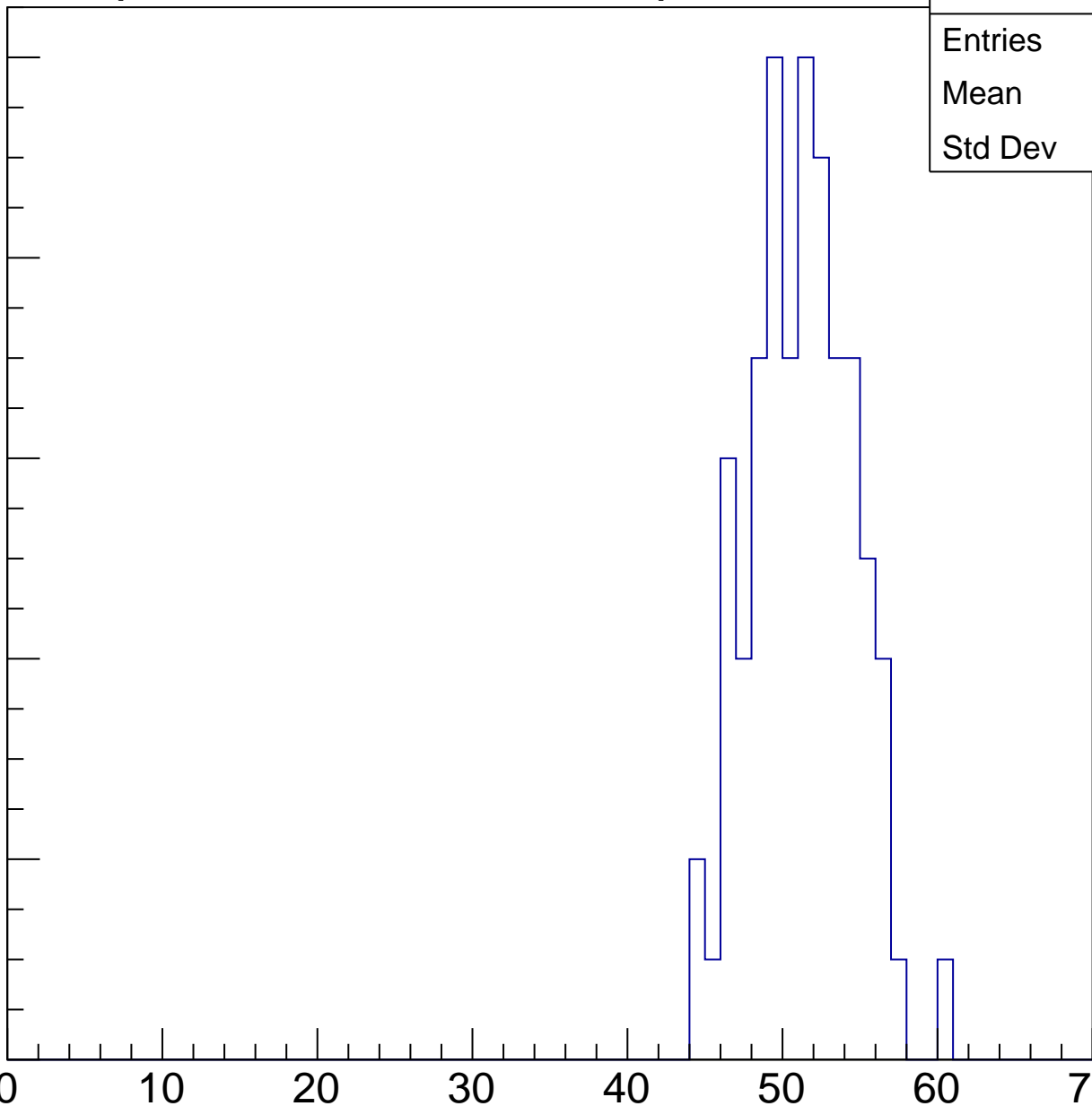
30

40

50

60

ampl

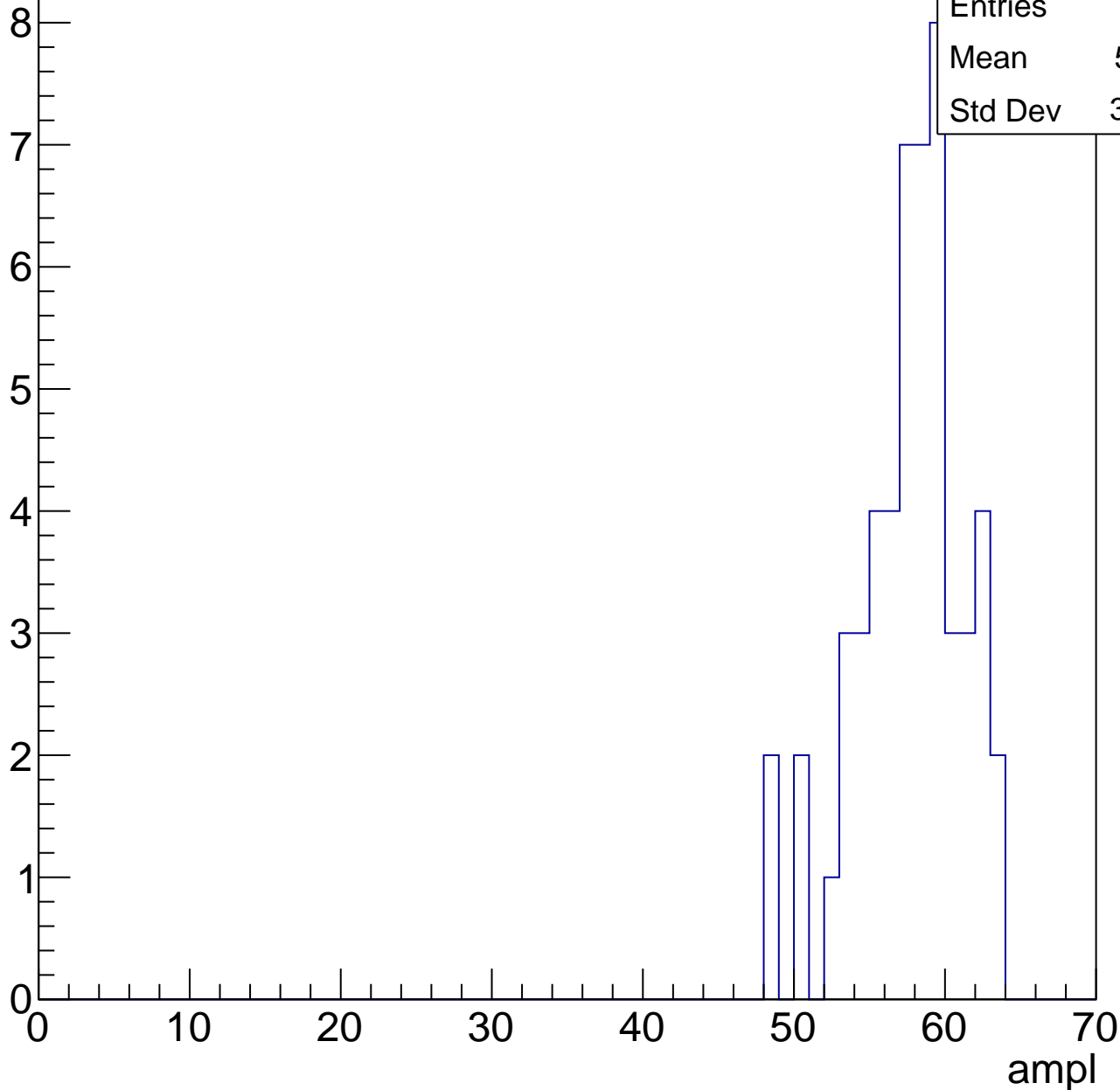


# B0L002S, U2-ch106, adc4

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	53
Mean	57.11
Std Dev	3.543

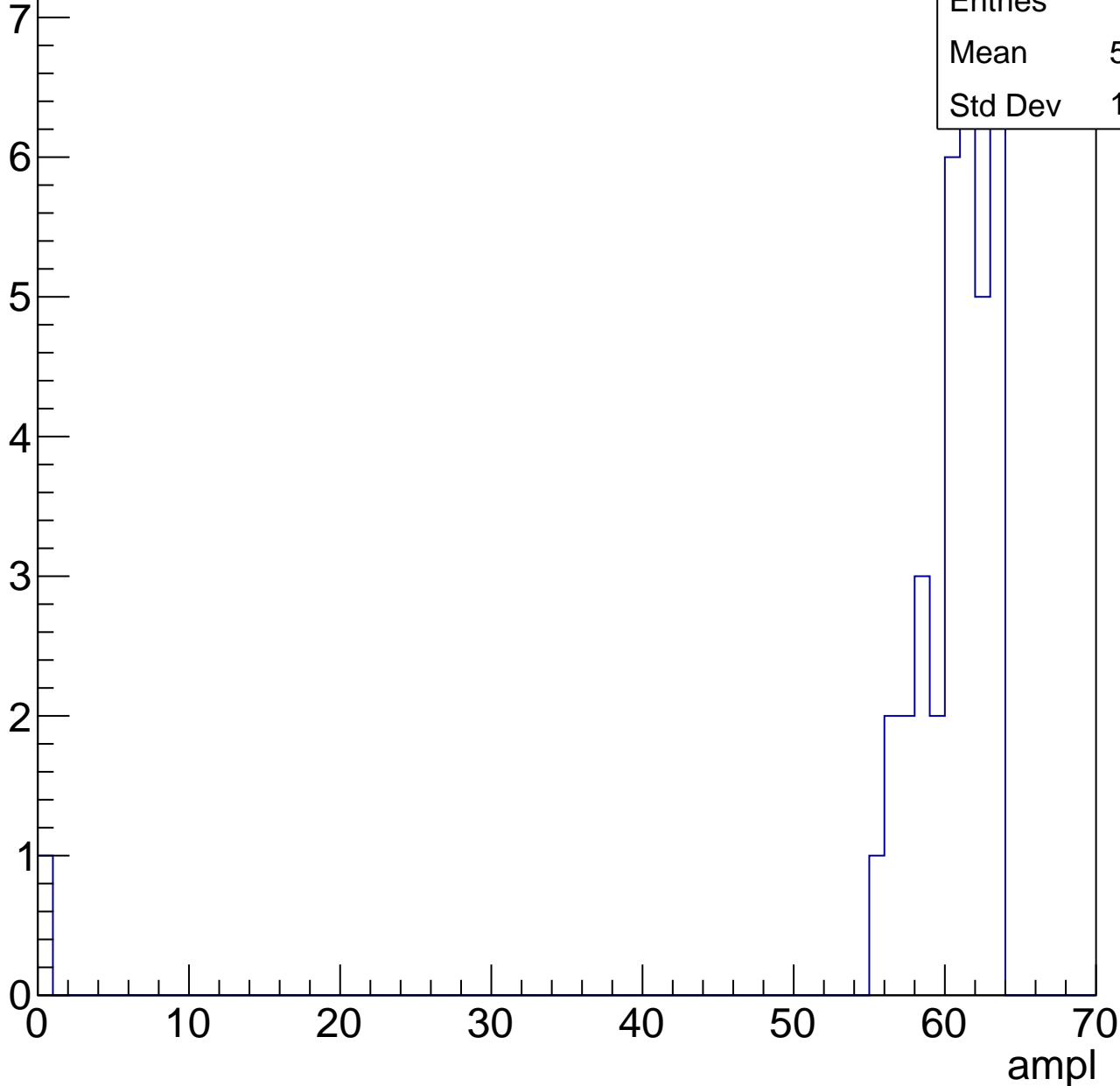


# B0L002S, U2-ch106, adc5

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	36
Mean	58.64
Std Dev	10.15



# B0L002S, U2-ch106, adc6

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry





# B0L002S, U2-ch106, adc7

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



Entries	3
Mean	0
Std Dev	0

# B0L002S, U2-ch107, adc0

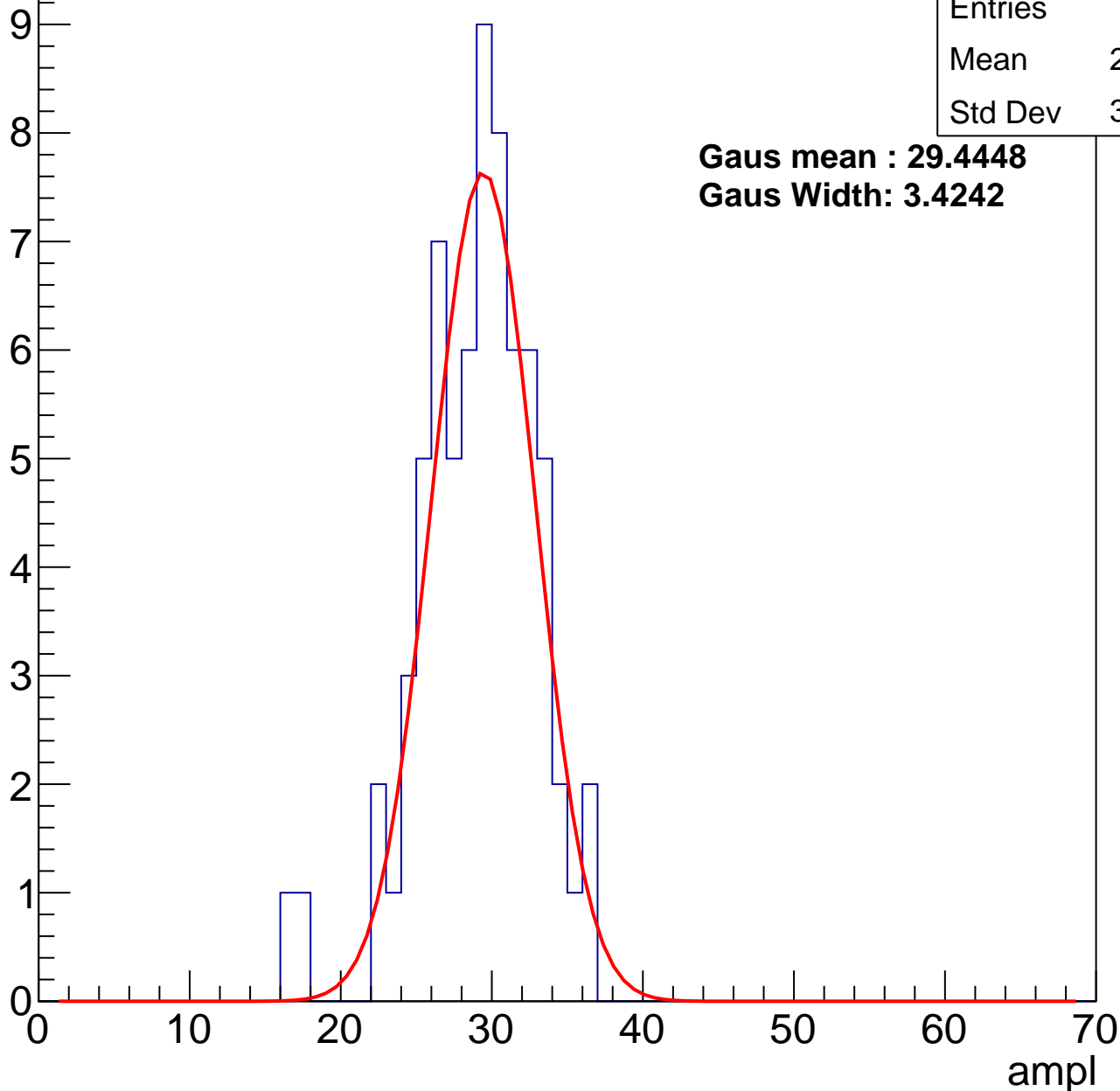
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	70
Mean	28.59
Std Dev	3.834

**Gaus mean : 29.4448**

**Gaus Width: 3.4242**



# B0L002S, U2-ch107, adc1

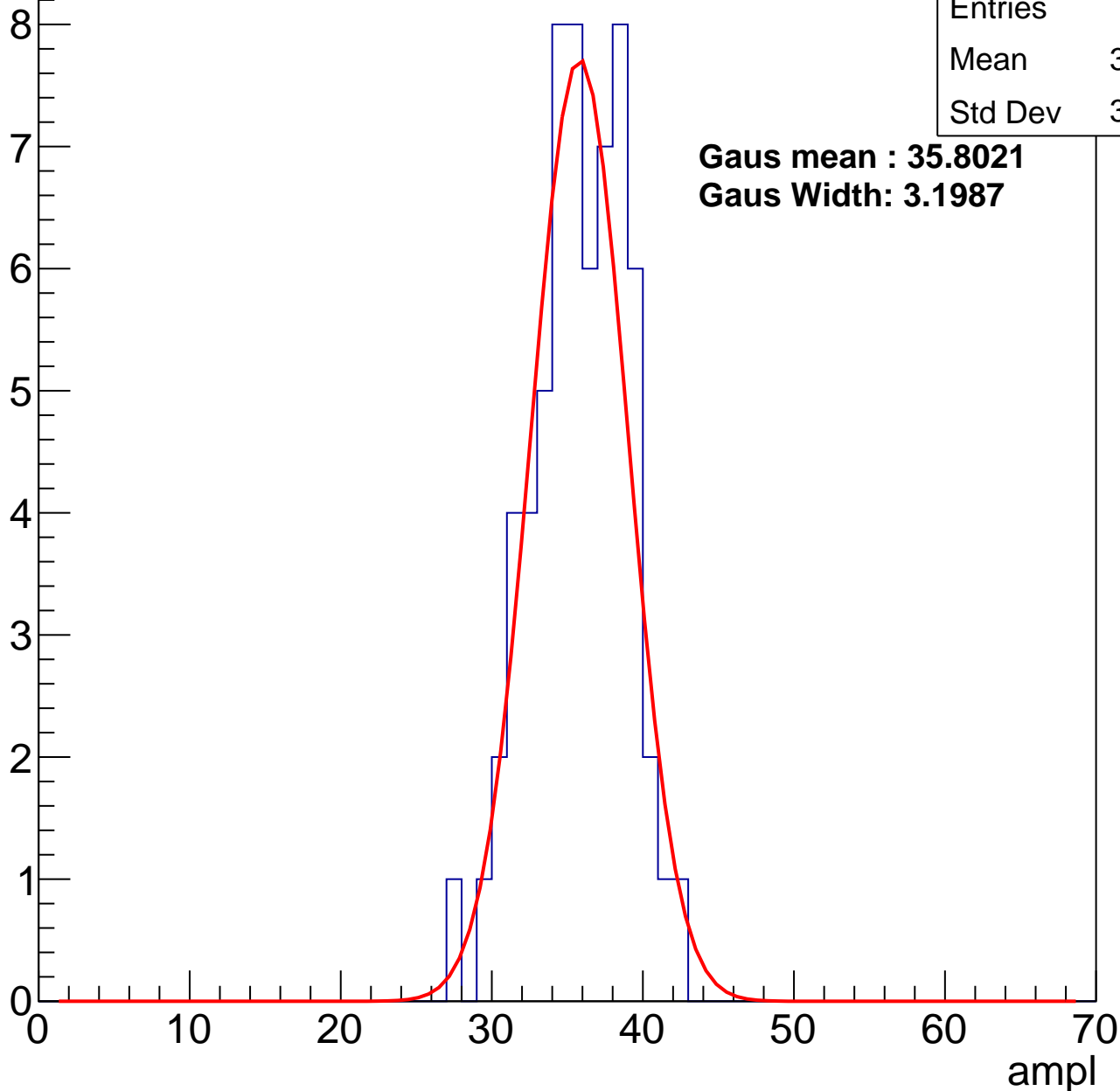
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	64
Mean	35.33
Std Dev	3.082

**Gaus mean : 35.8021**

**Gaus Width: 3.1987**



# B0L002S, U2-ch107, adc2

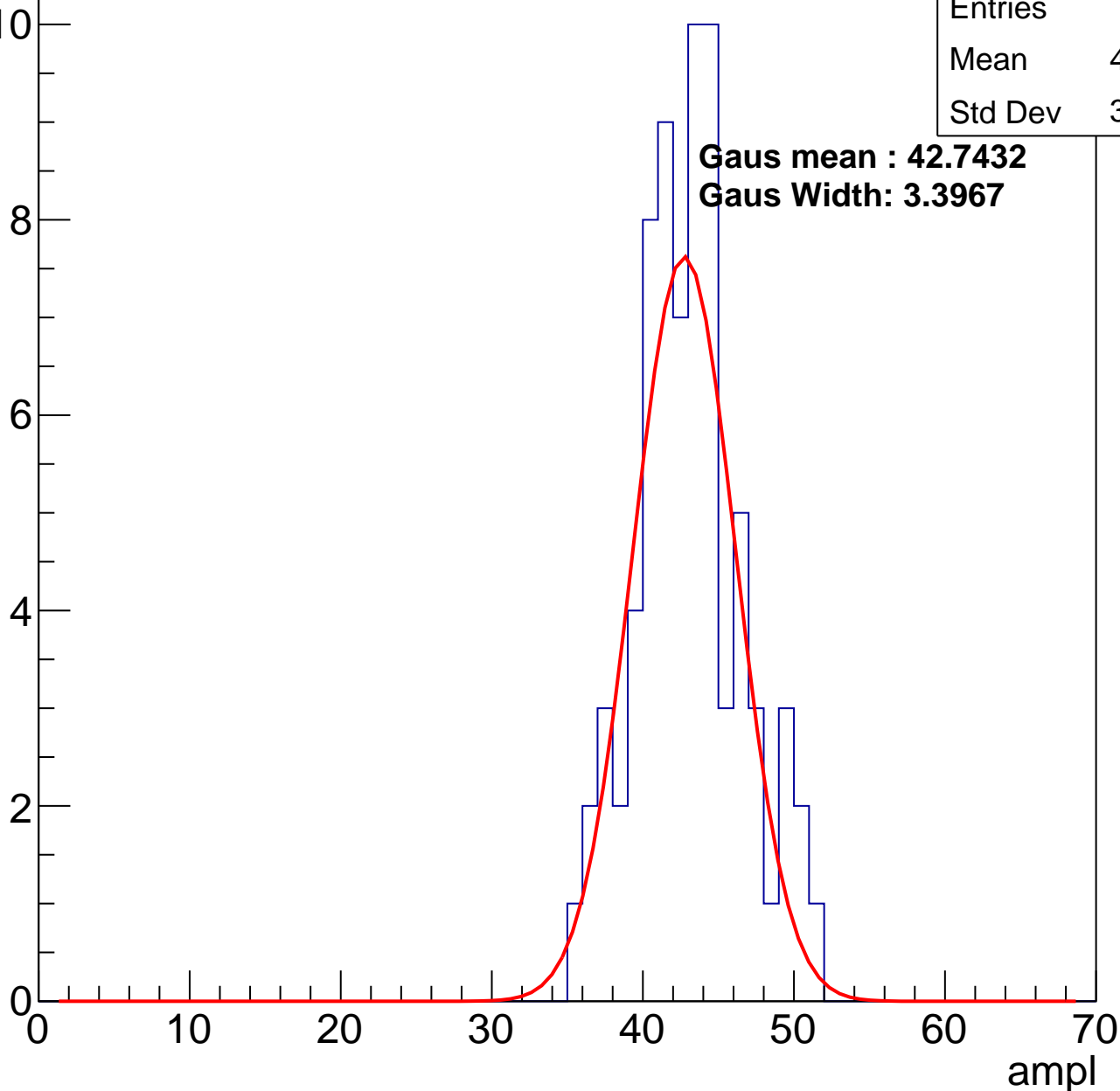
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	74
Mean	42.64
Std Dev	3.486

**Gaus mean : 42.7432**

**Gaus Width: 3.3967**

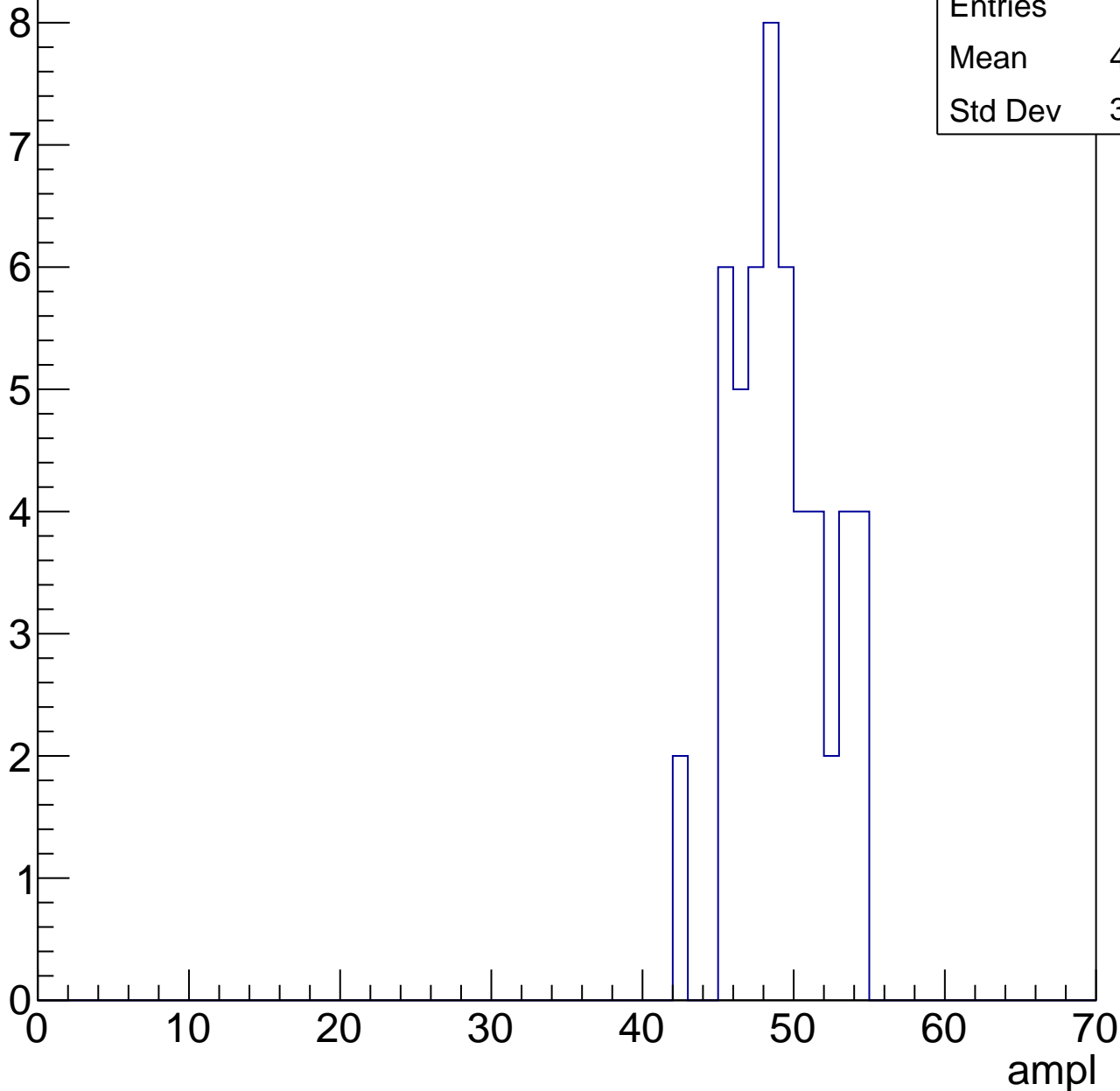


# B0L002S, U2-ch107, adc3

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	51
Mean	48.63
Std Dev	3.023

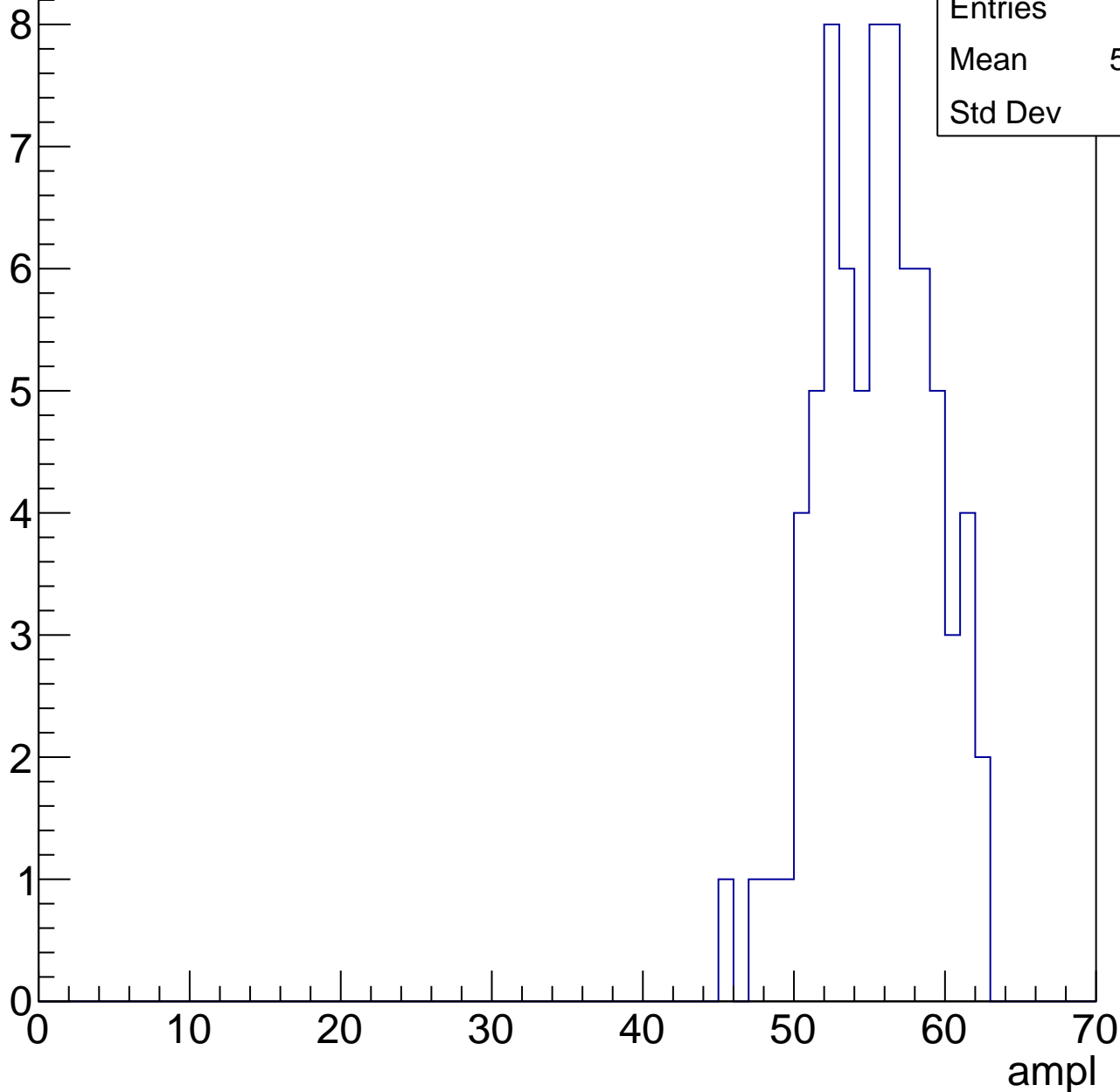


# B0L002S, U2-ch107, adc4

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	74
Mean	54.99
Std Dev	3.7

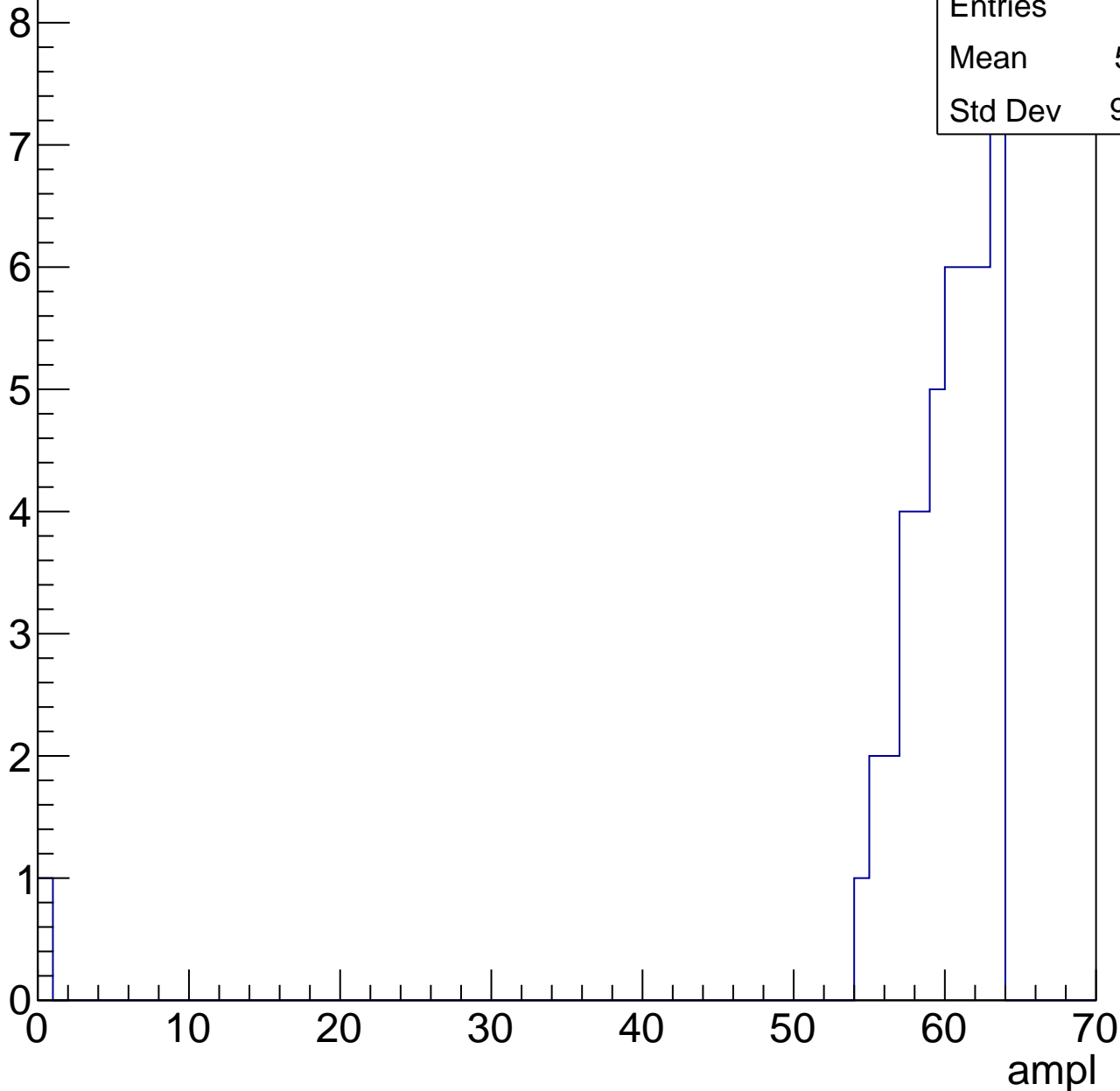


# B0L002S, U2-ch107, adc5

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

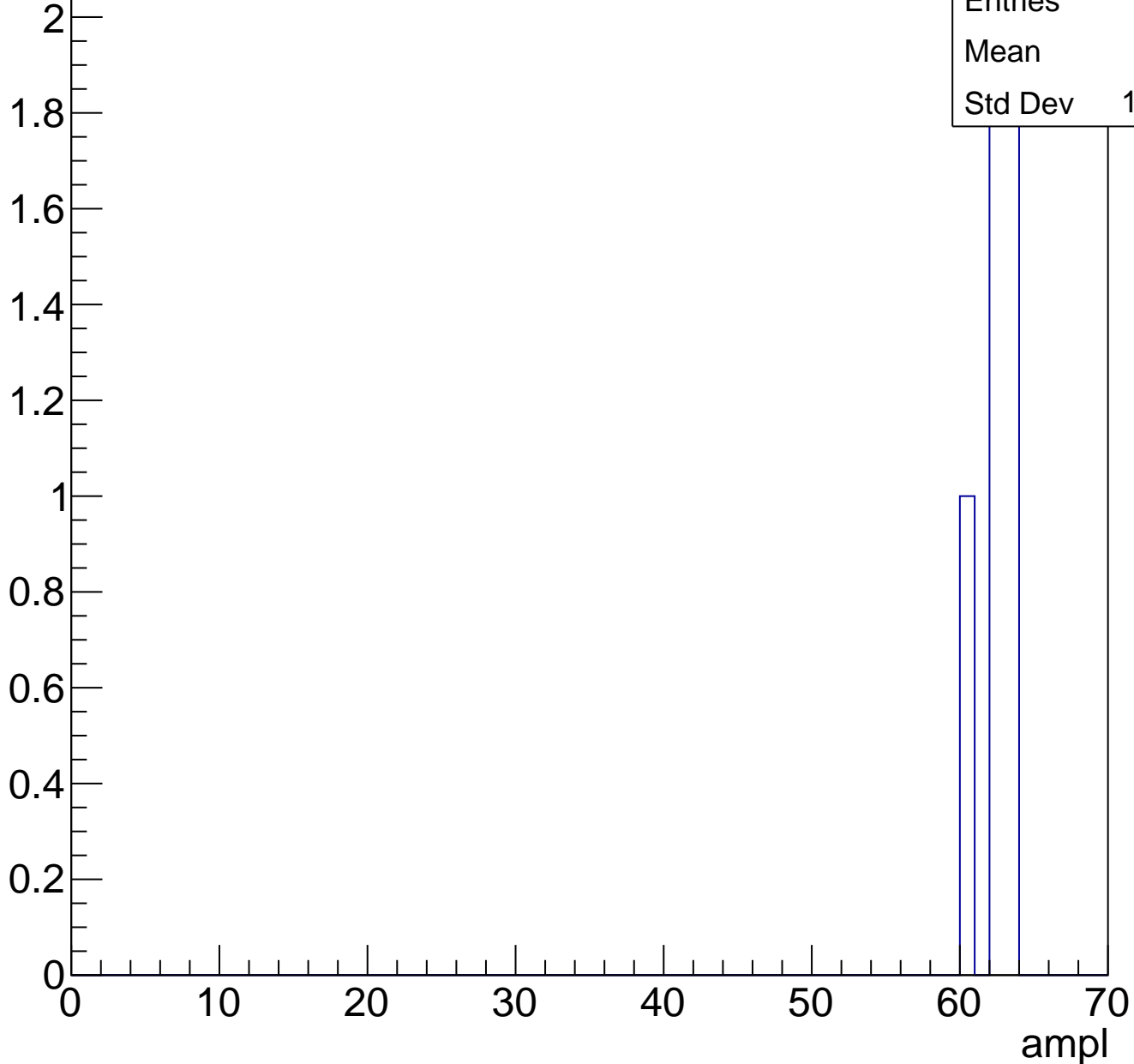
Entries	45
Mean	58.51
Std Dev	9.162



# B0L002S, U2-ch107, adc6

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry





# B0L002S, U2-ch107, adc7

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



# B0L002S, U2-ch108, adc0

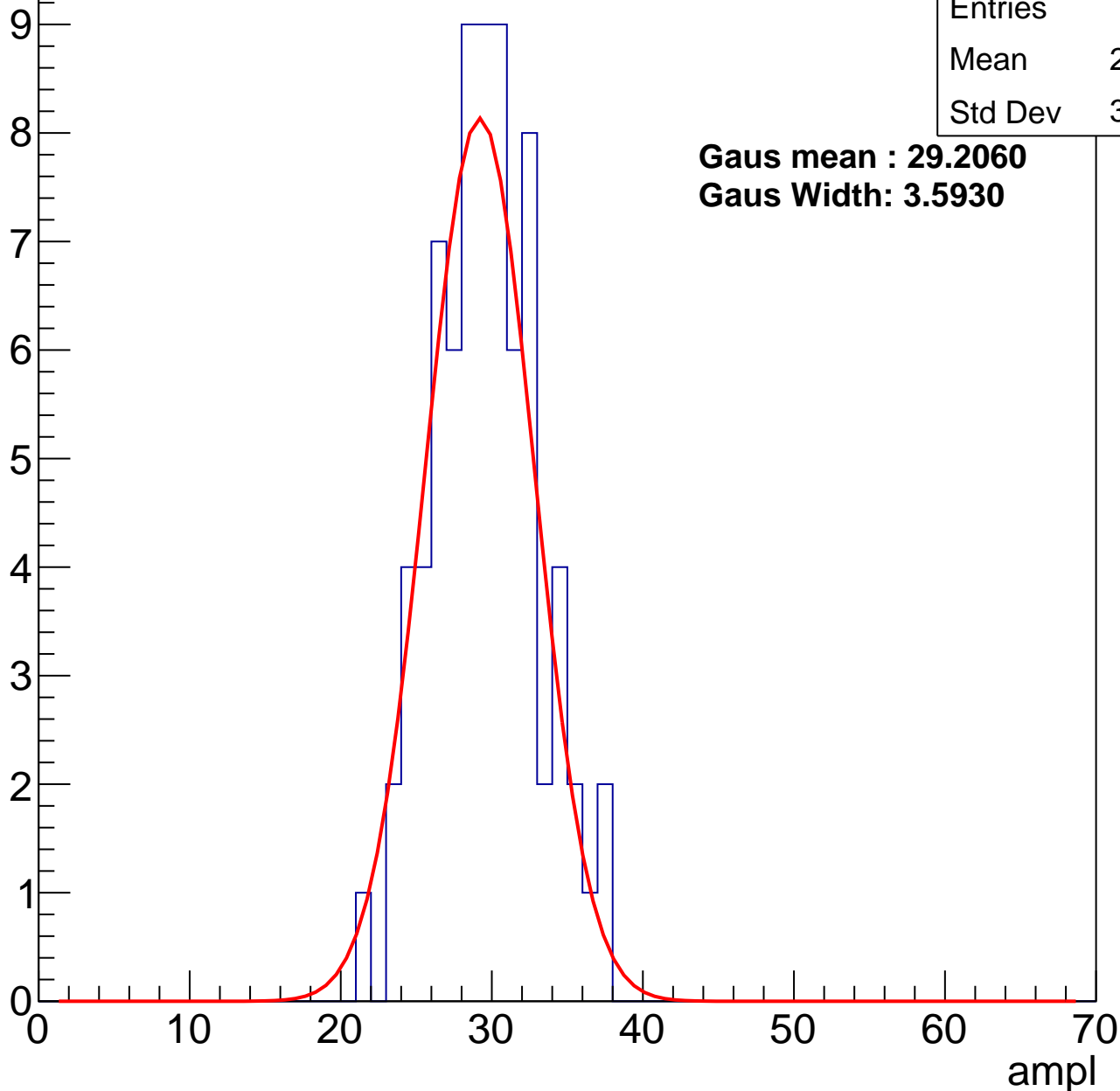
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	76
Mean	29.13
Std Dev	3.404

**Gaus mean : 29.2060**

**Gaus Width: 3.5930**



# B0L002S, U2-ch108, adc1

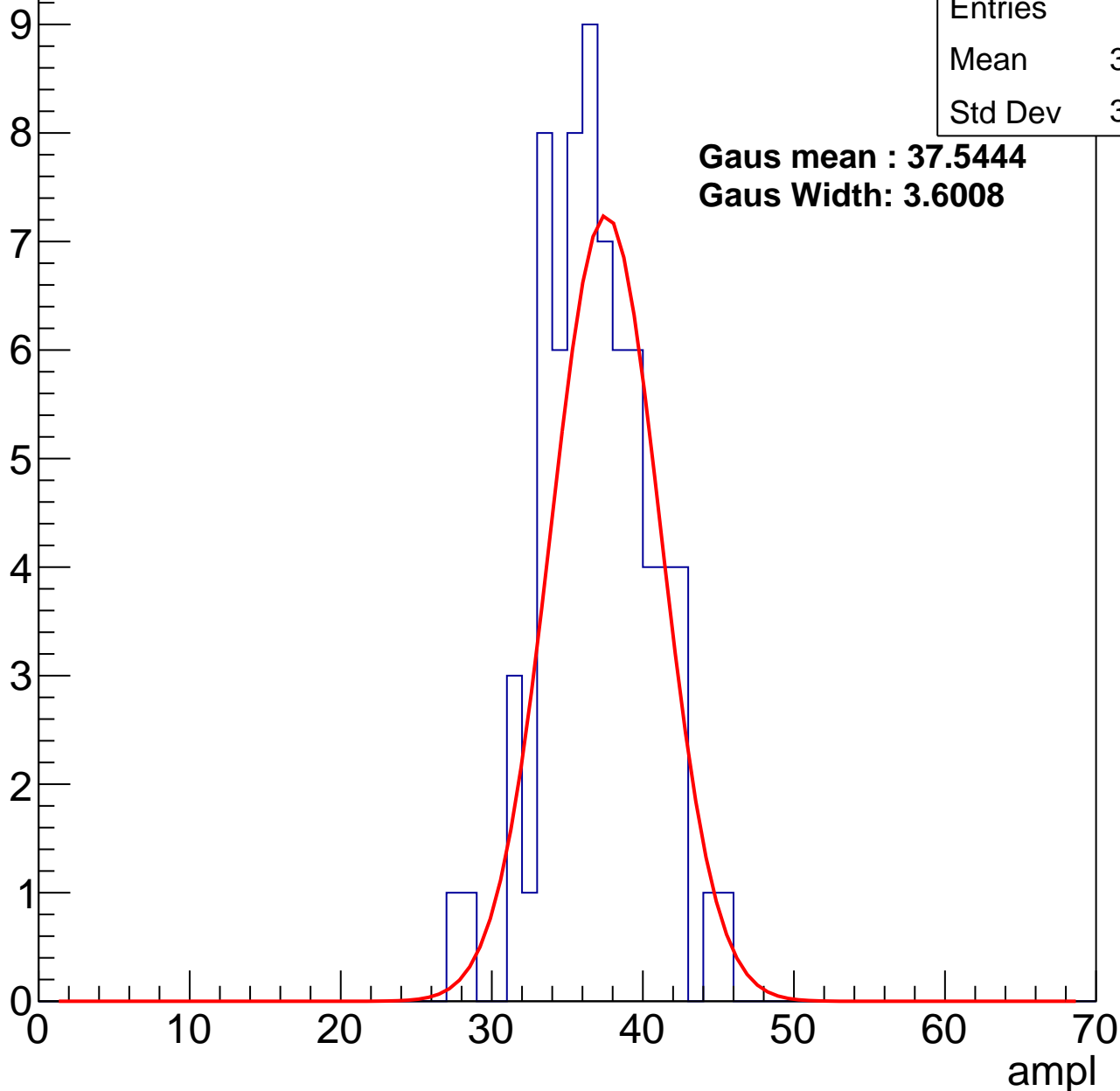
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	70
Mean	36.49
Std Dev	3.508

**Gaus mean : 37.5444**

**Gaus Width: 3.6008**



# B0L002S, U2-ch108, adc2

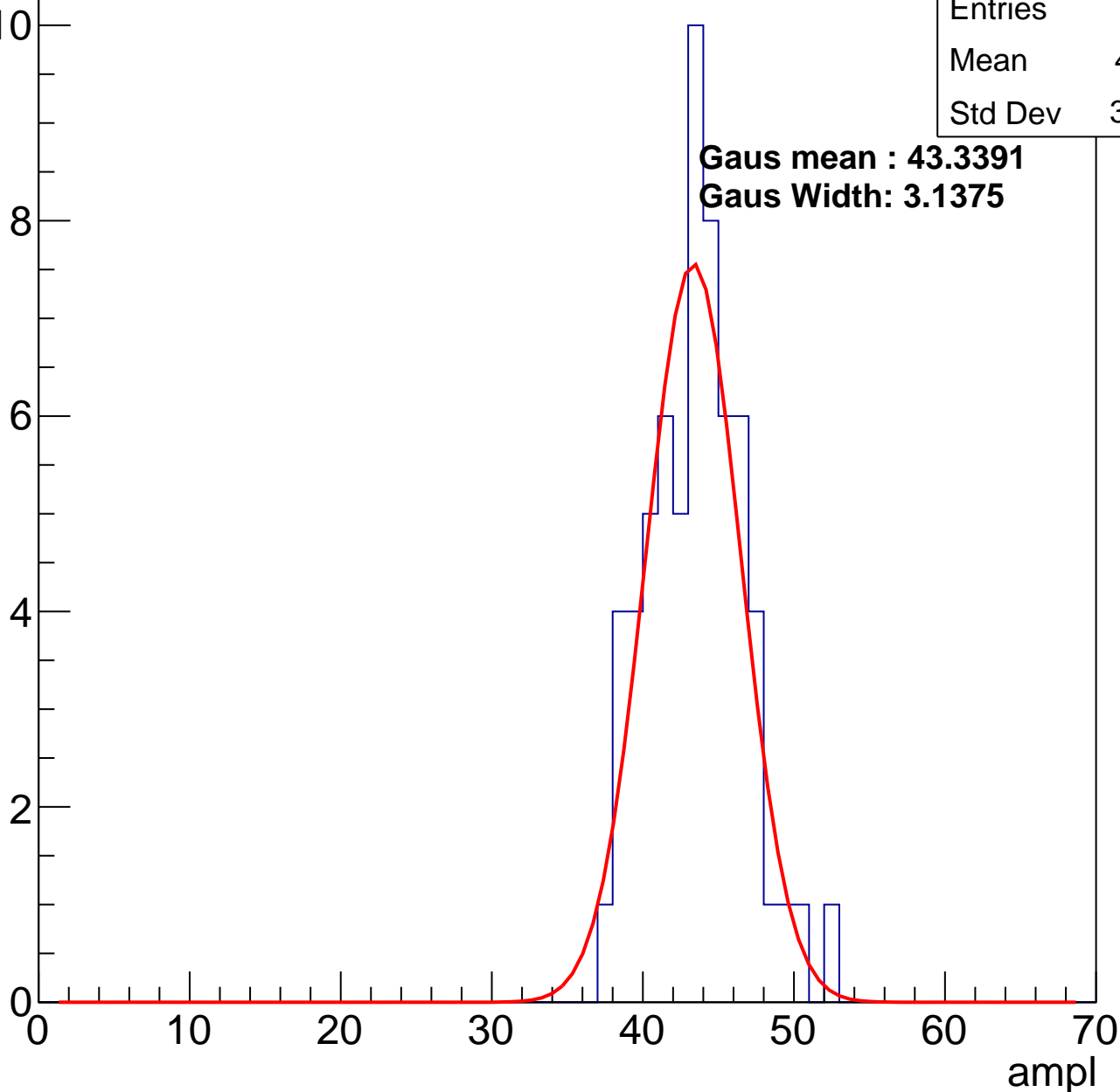
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	63
Mean	43.11
Std Dev	3.122

**Gaus mean : 43.3391**

**Gaus Width: 3.1375**

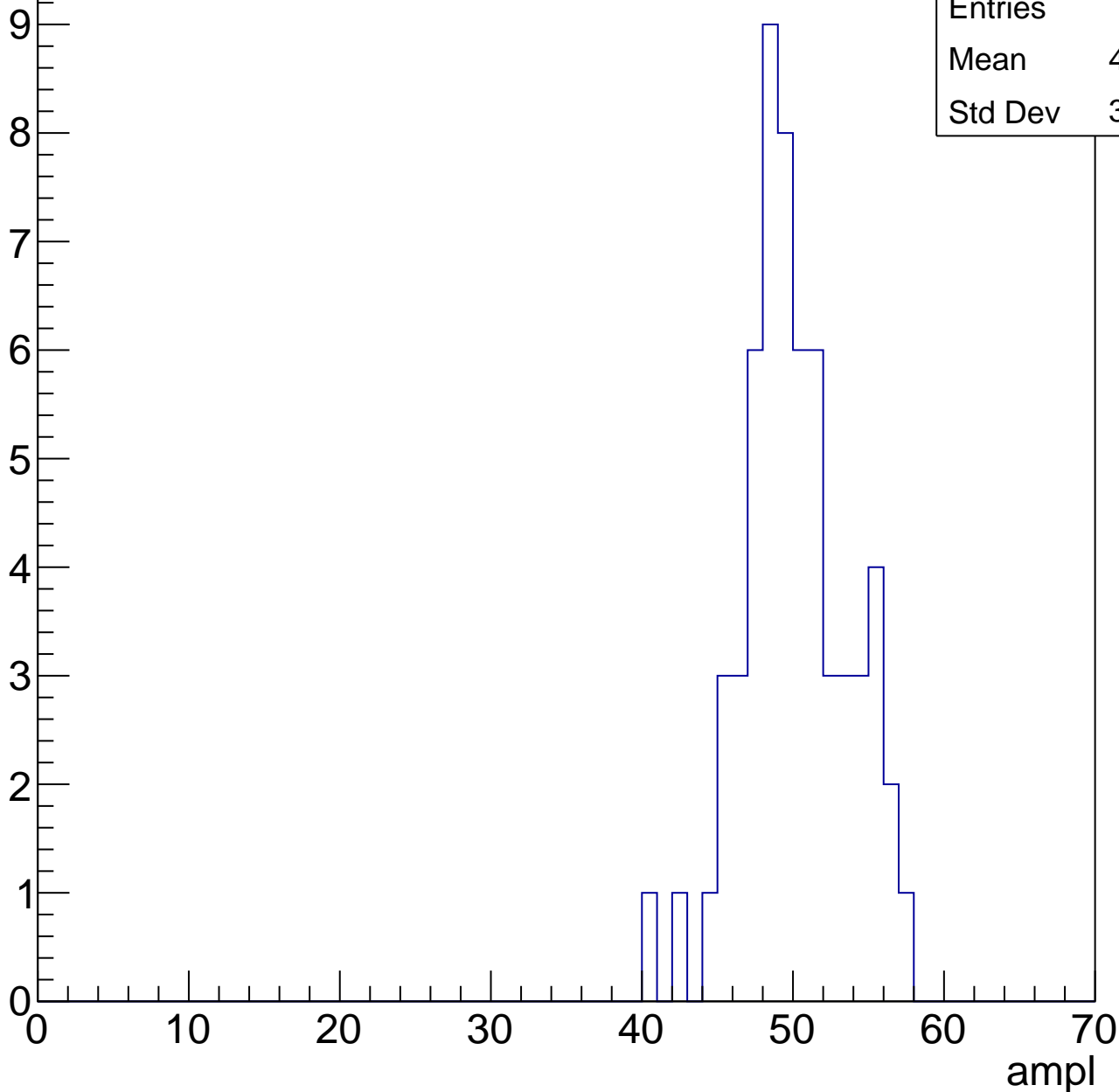


# B0L002S, U2-ch108, adc3

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	60
Mean	49.62
Std Dev	3.479

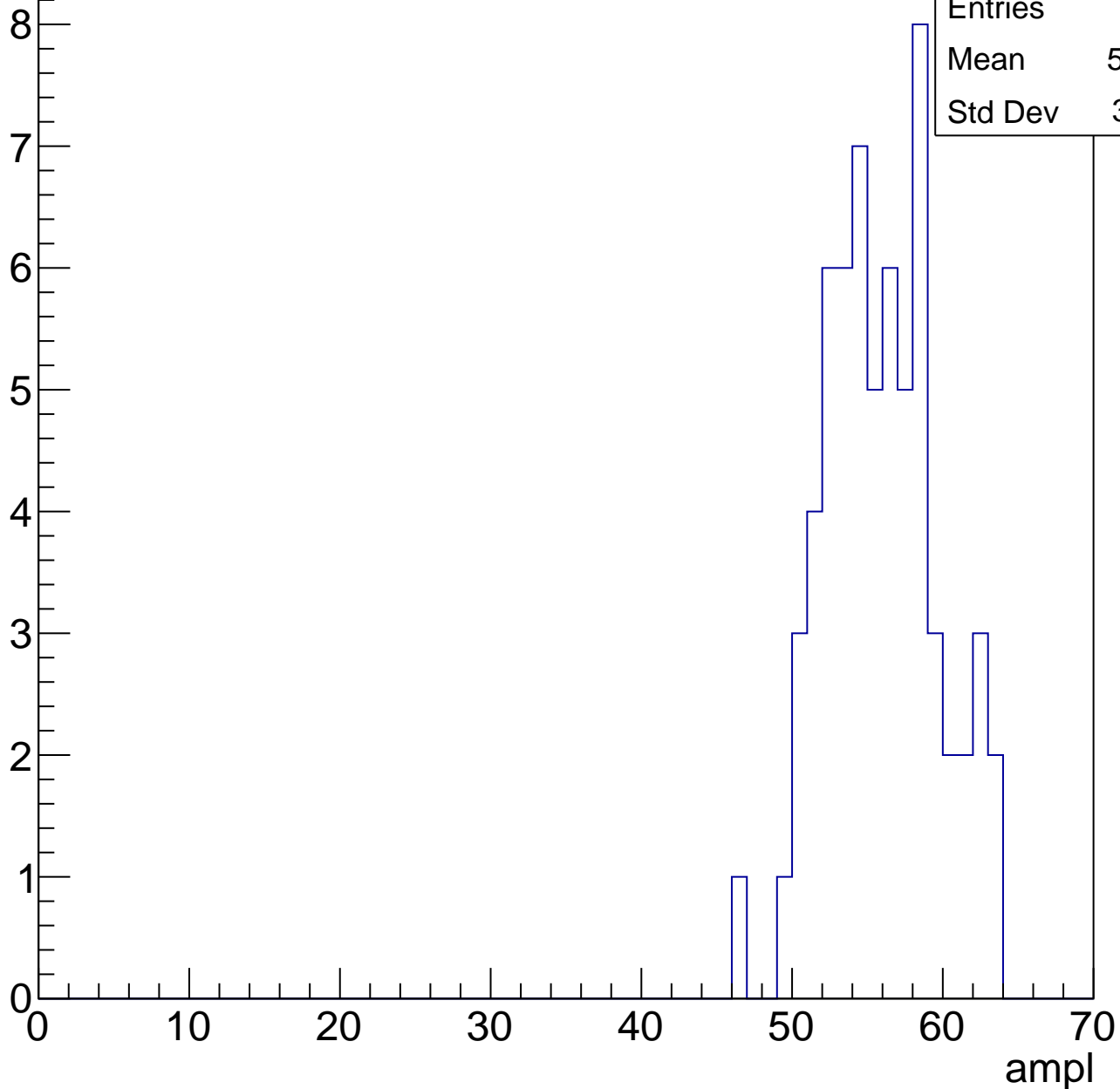


# B0L002S, U2-ch108, adc4

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	64
Mean	55.44
Std Dev	3.691

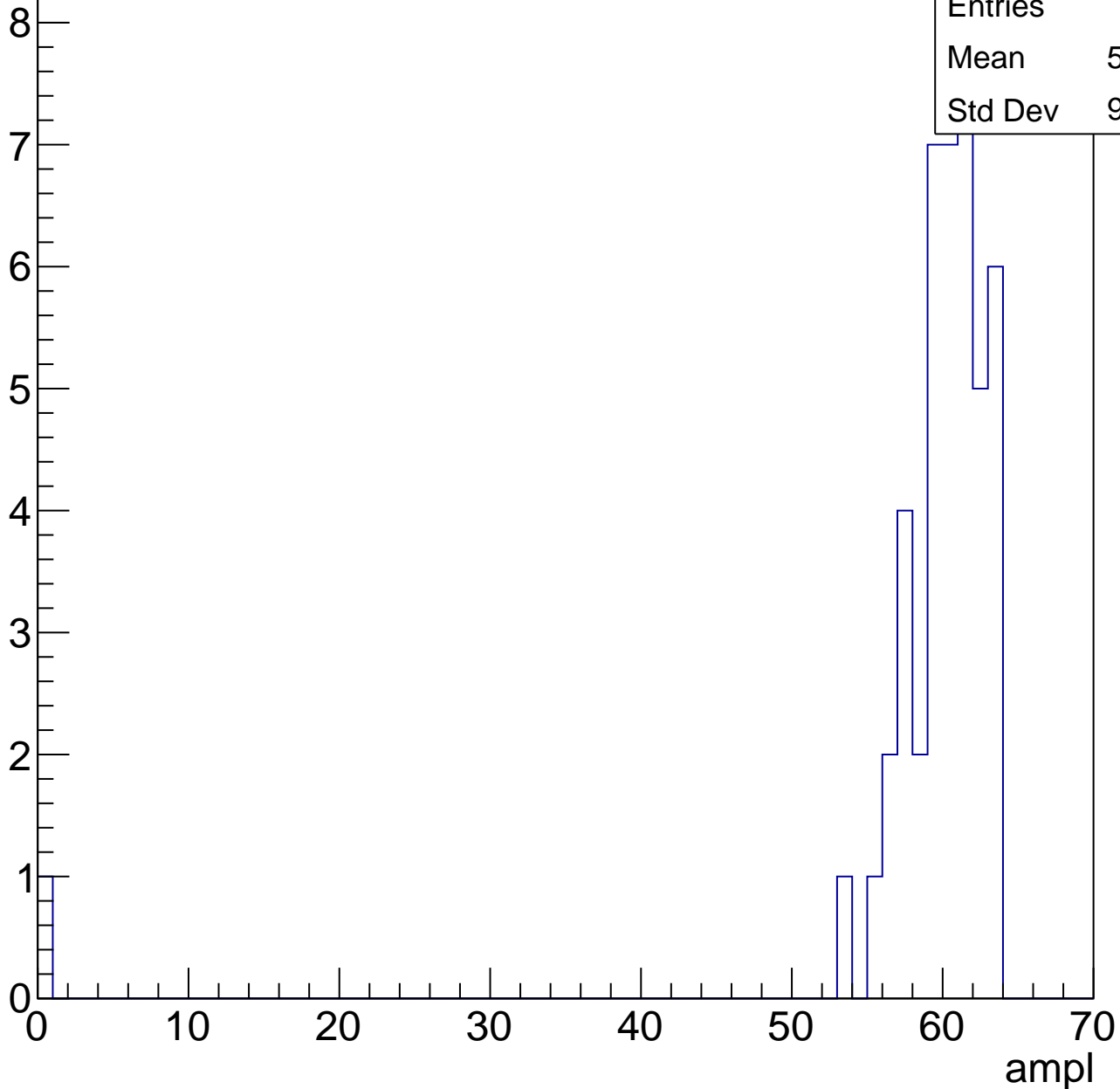


# B0L002S, U2-ch108, adc5

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

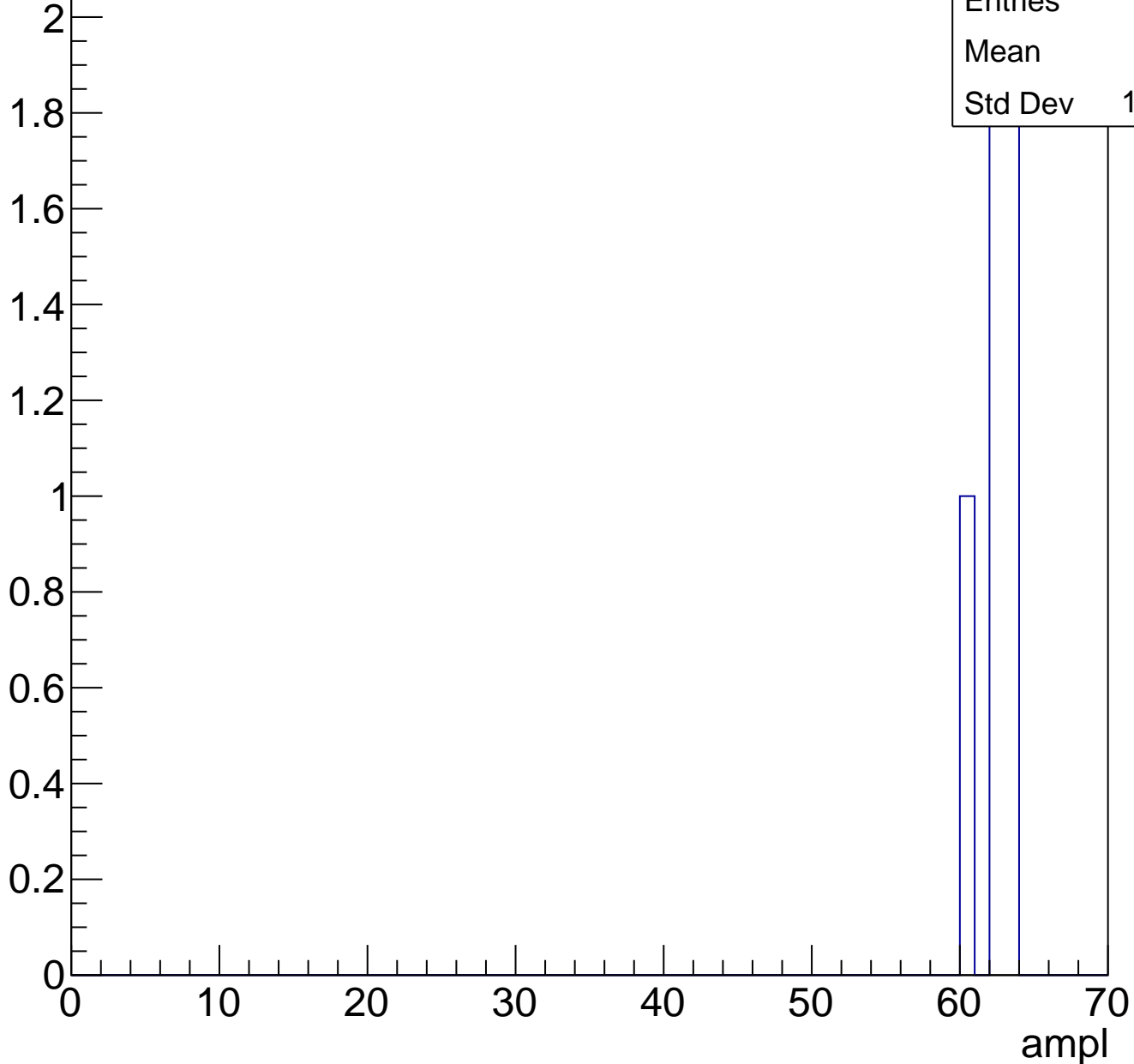
Entries	44
Mean	58.48
Std Dev	9.216



# B0L002S, U2-ch108, adc6

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry





# B0L002S, U2-ch108, adc7

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L002S, U2-ch109, adc0

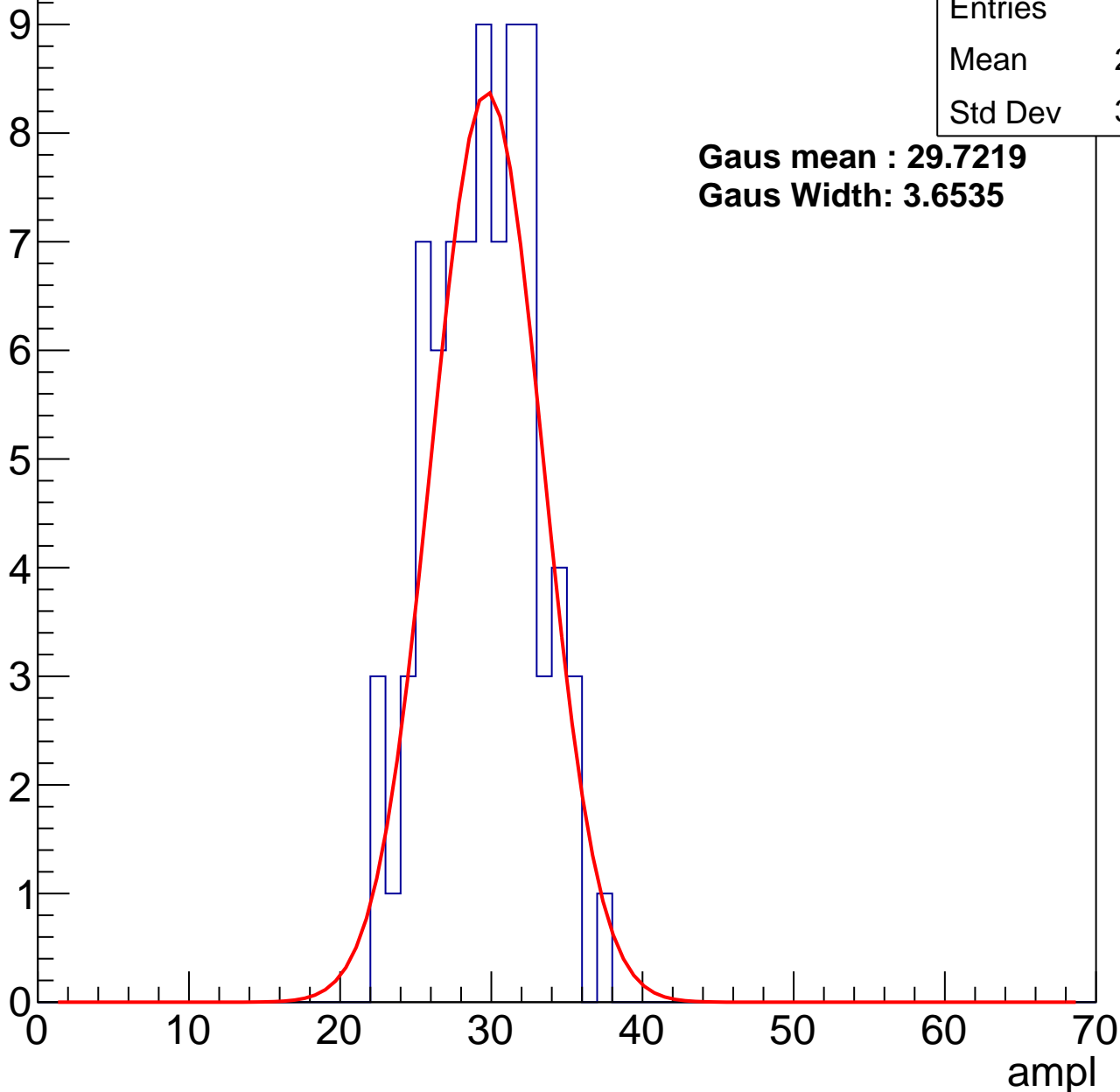
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	79
Mean	29.01
Std Dev	3.381

**Gaus mean : 29.7219**

**Gaus Width: 3.6535**



# B0L002S, U2-ch109, adc1

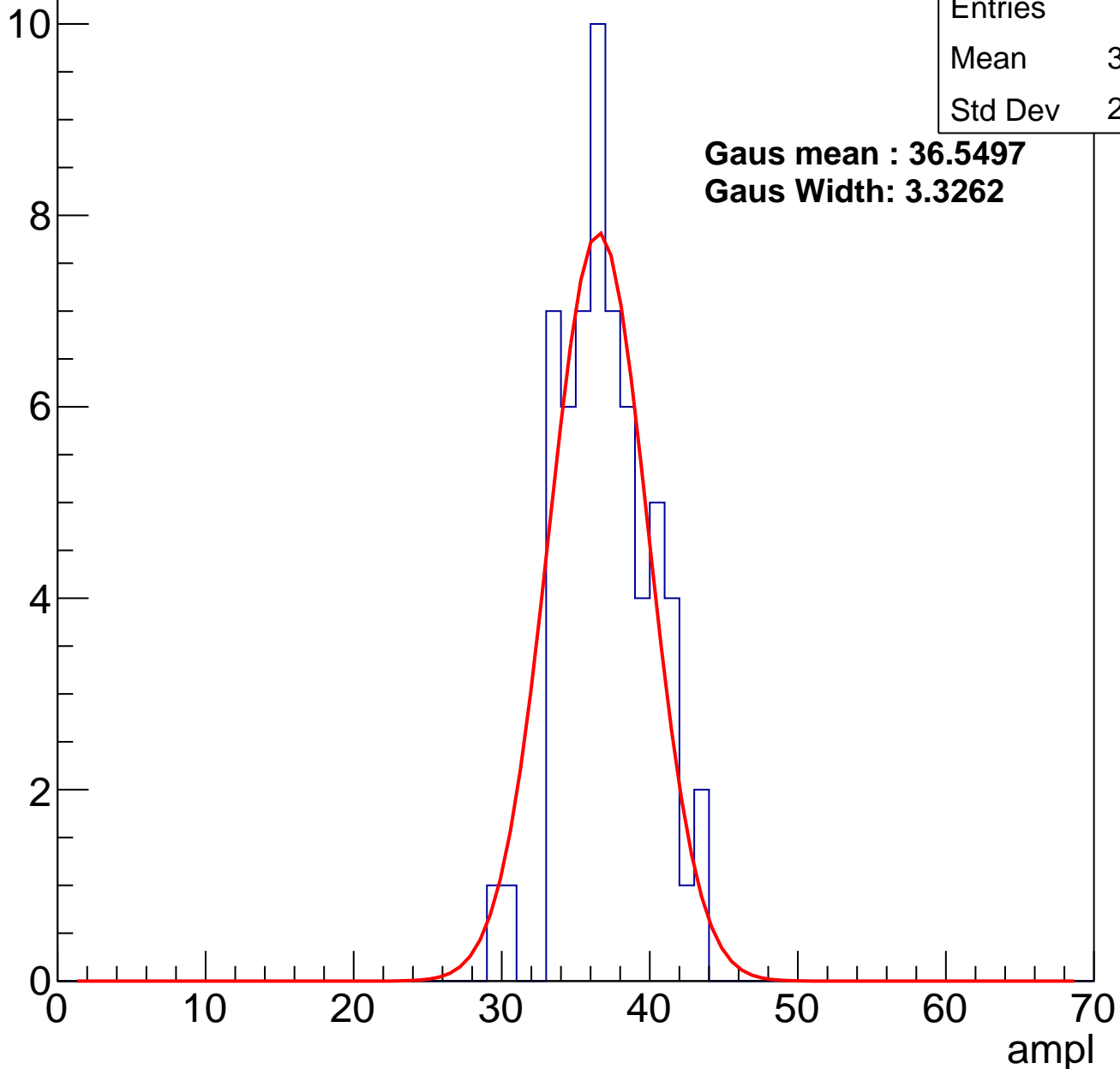
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entries	61
Mean	36.62
Std Dev	2.965

**Gaus mean : 36.5497**

**Gaus Width: 3.3262**

Entry



# B0L002S, U2-ch109, adc2

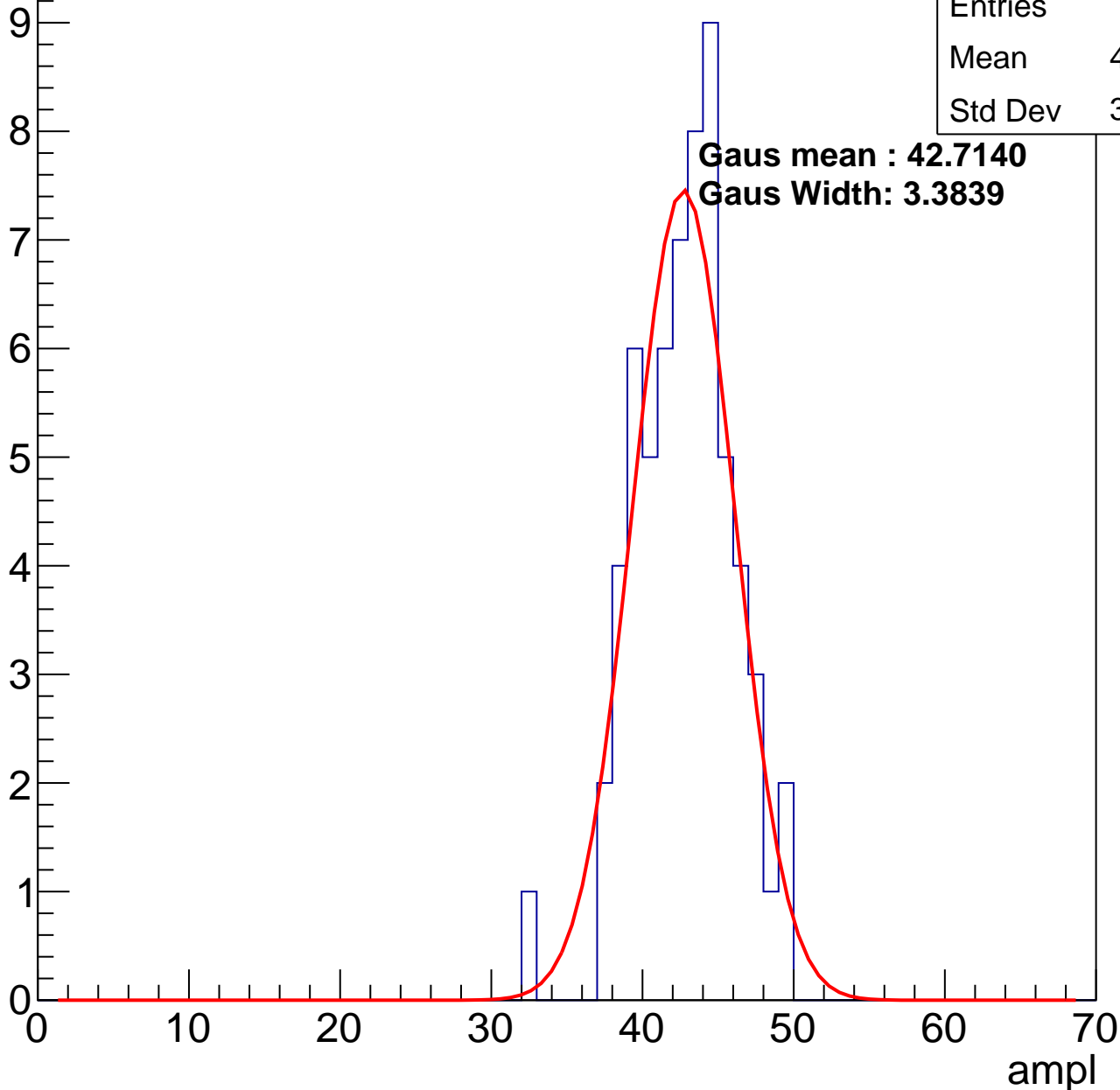
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	63
Mean	42.35
Std Dev	3.208

**Gaus mean : 42.7140**

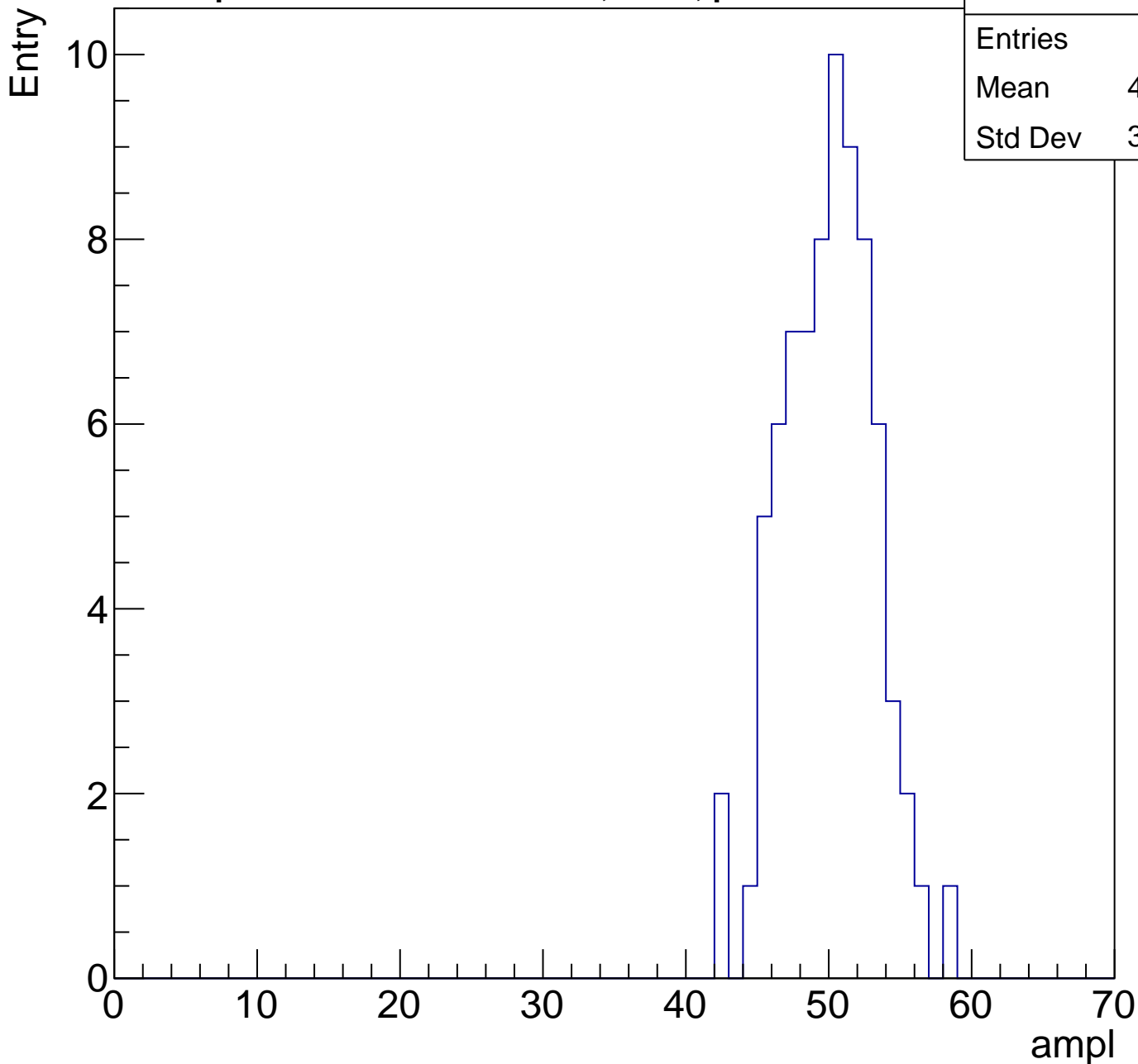
**Gaus Width: 3.3839**



# B0L002S, U2-ch109, adc3

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entries	76
Mean	49.54
Std Dev	3.164

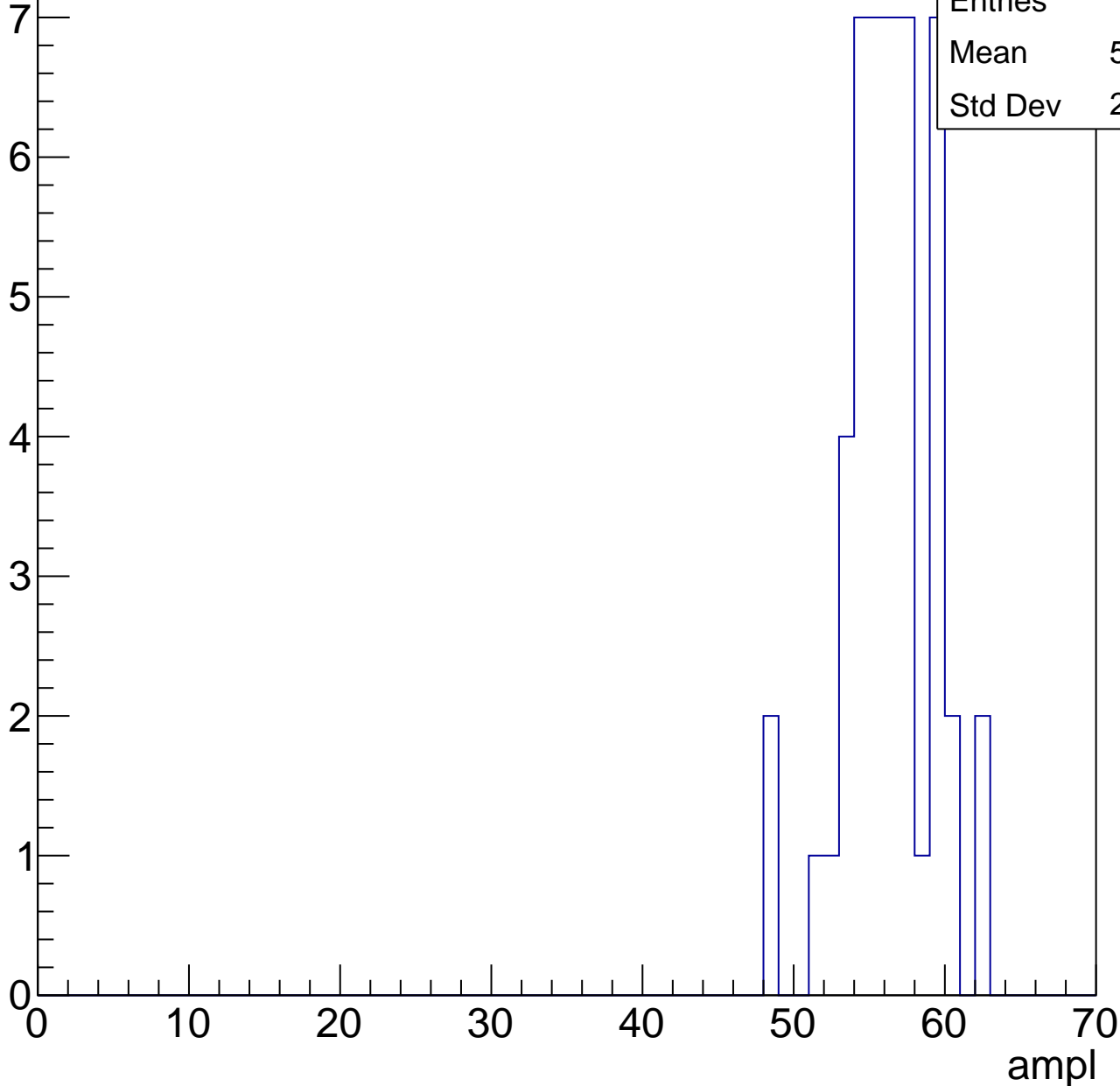


# B0L002S, U2-ch109, adc4

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	48
Mean	55.83
Std Dev	2.946

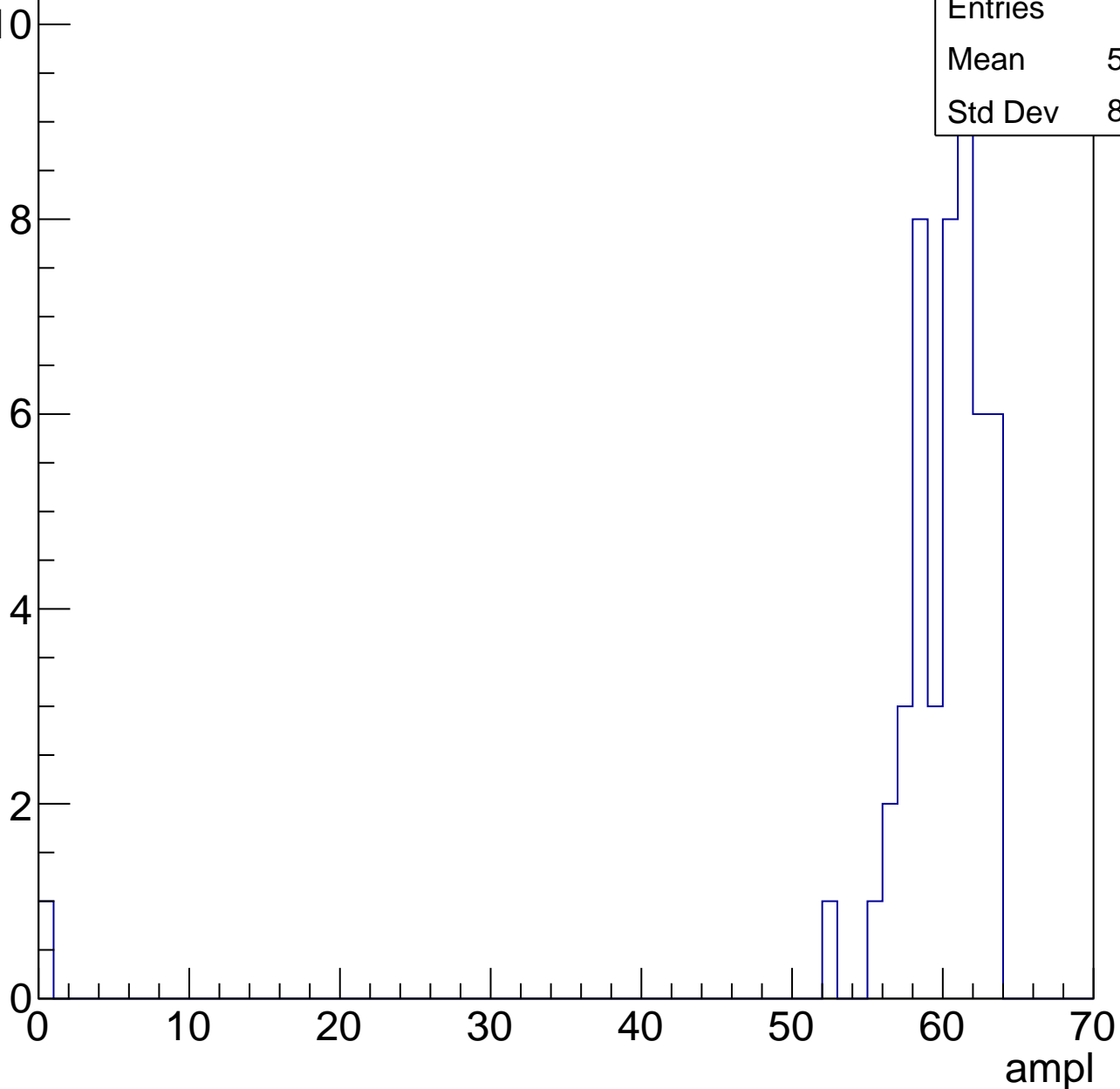


# B0L002S, U2-ch109, adc5

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	49
Mean	58.59
Std Dev	8.776



# B0L002S, U2-ch109, adc6

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry





# B0L002S, U2-ch109, adc7

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L002S, U2-ch110, adc0

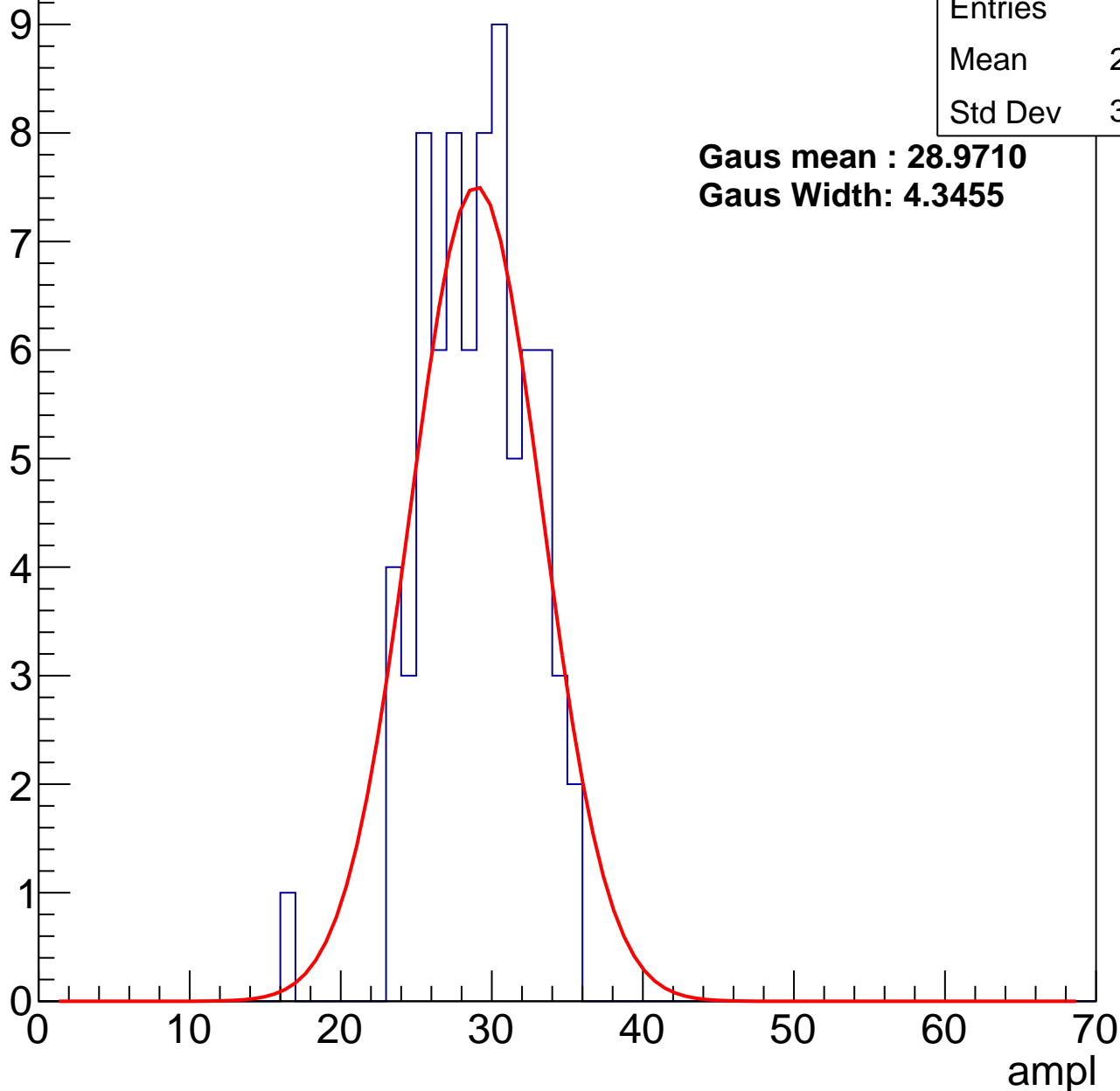
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	75
Mean	28.52
Std Dev	3.496

**Gaus mean : 28.9710**

**Gaus Width: 4.3455**



# B0L002S, U2-ch110, adc1

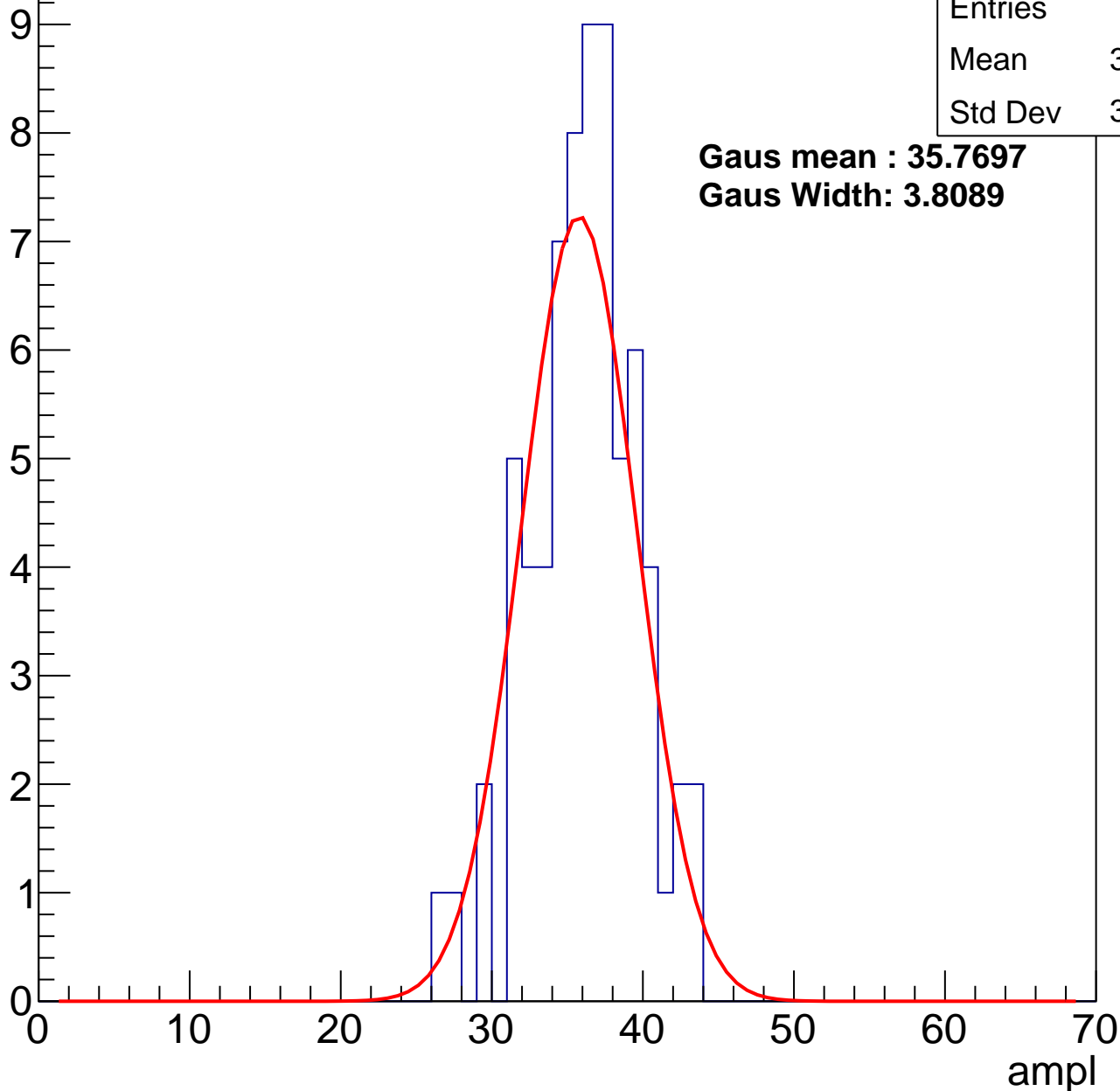
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	70
Mean	35.66
Std Dev	3.533

**Gaus mean : 35.7697**

**Gaus Width: 3.8089**



# B0L002S, U2-ch110, adc2

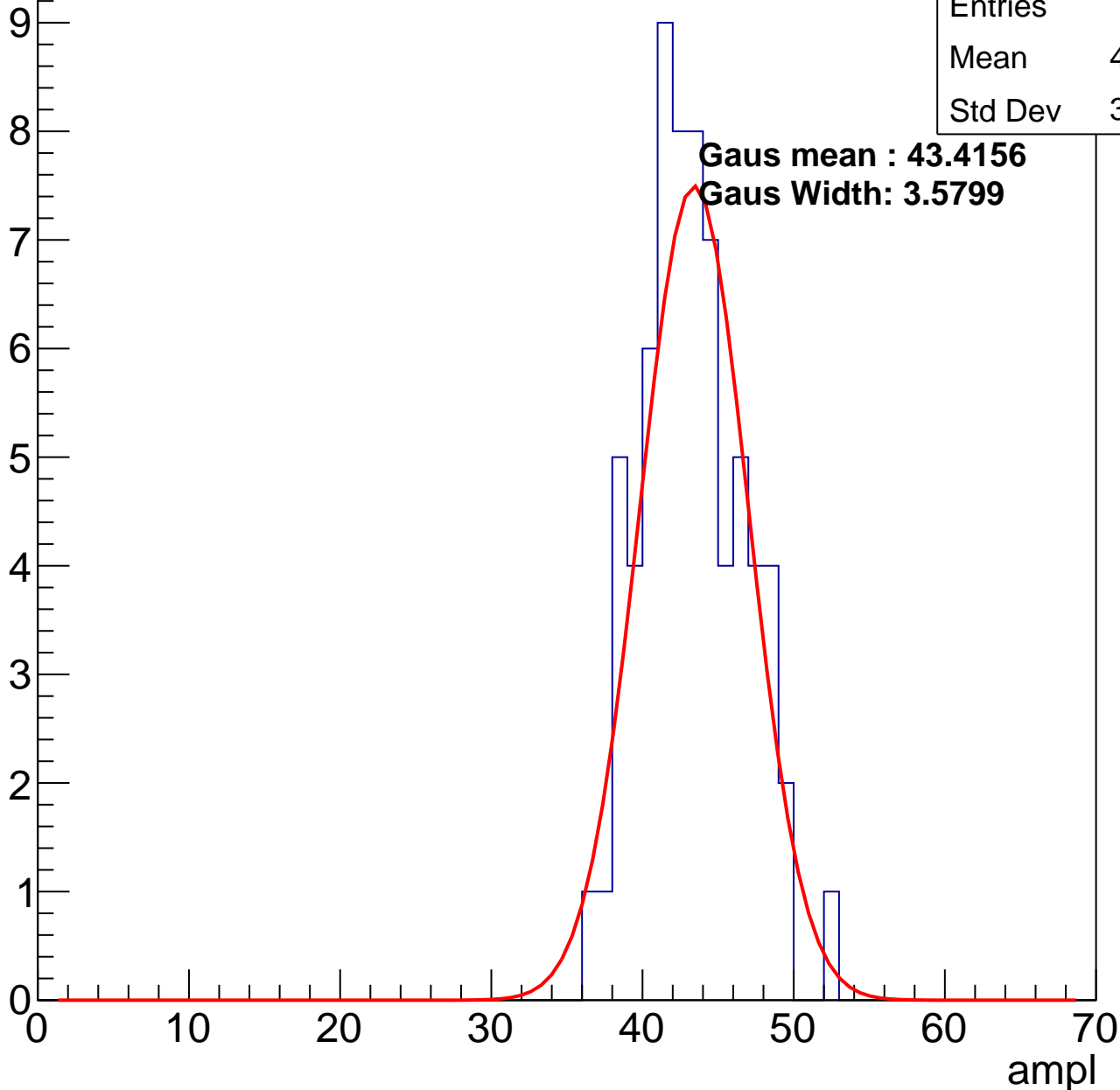
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	69
Mean	42.84
Std Dev	3.308

**Gaus mean : 43.4156**

**Gaus Width: 3.5799**



# B0L002S, U2-ch110, adc3

calib\_packv5\_042523\_0143.root, FC#8, port C1

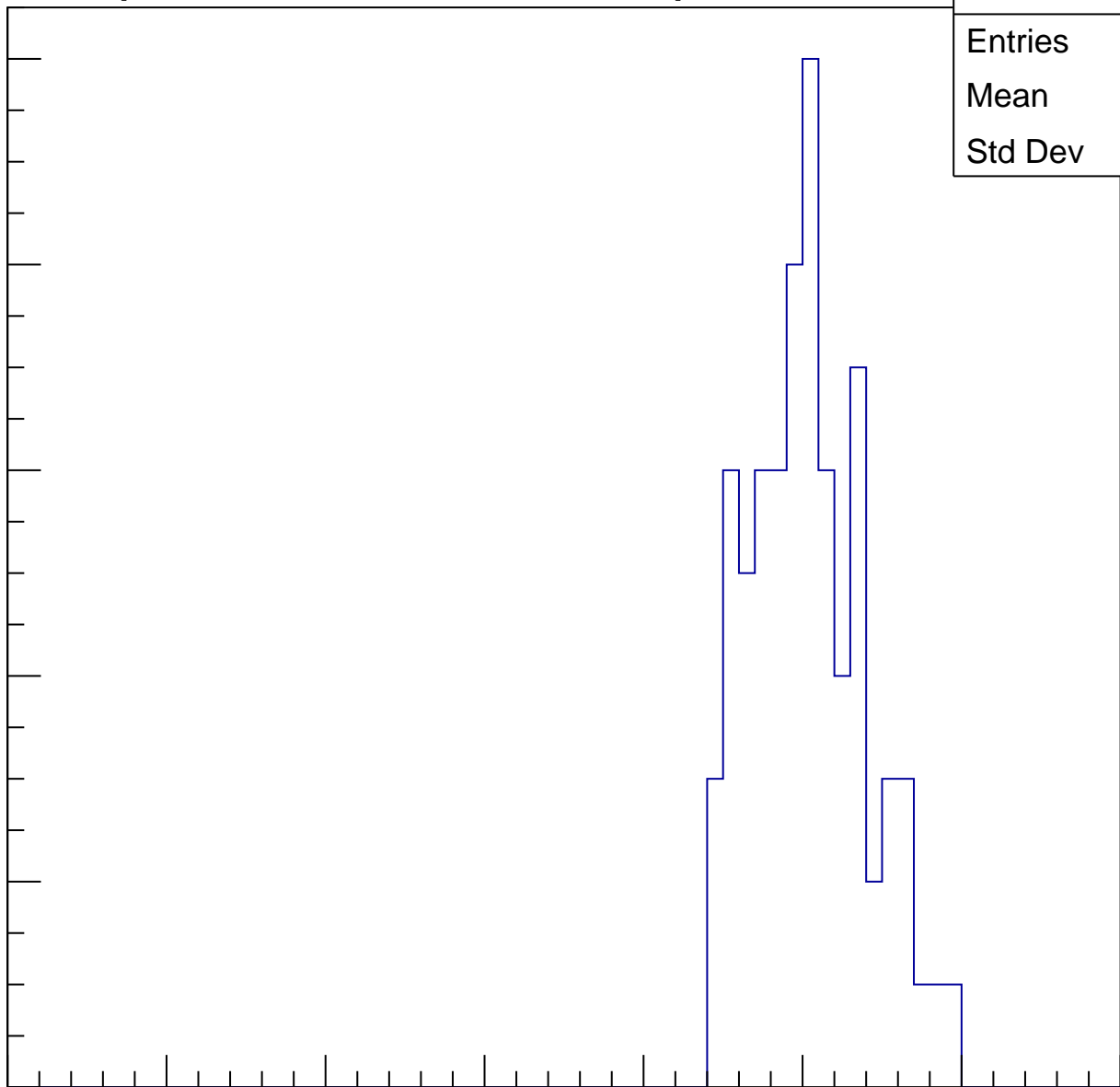
Entries	72
Mean	49.92
Std Dev	3.57

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

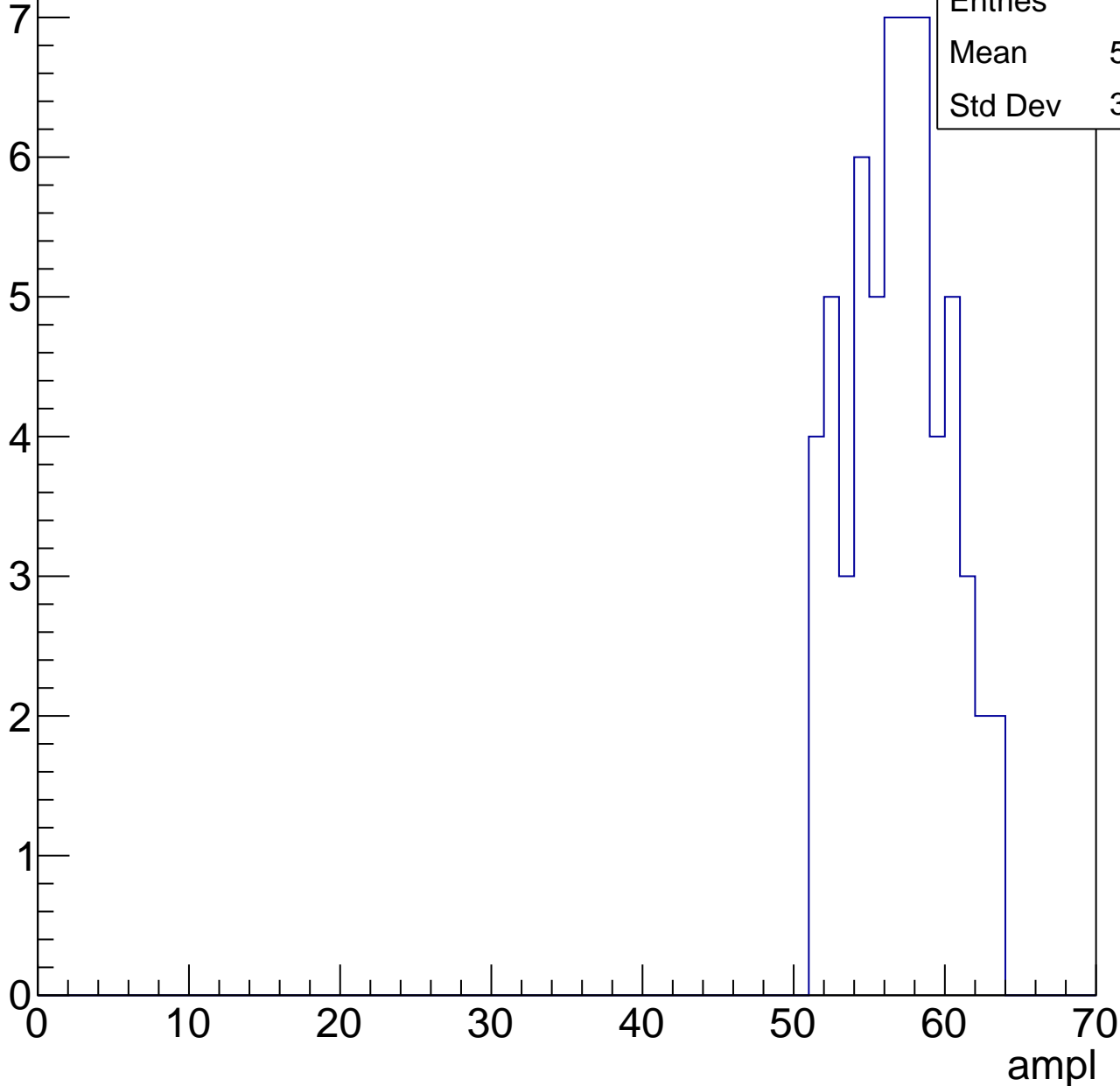


# B0L002S, U2-ch110, adc4

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	60
Mean	56.47
Std Dev	3.212

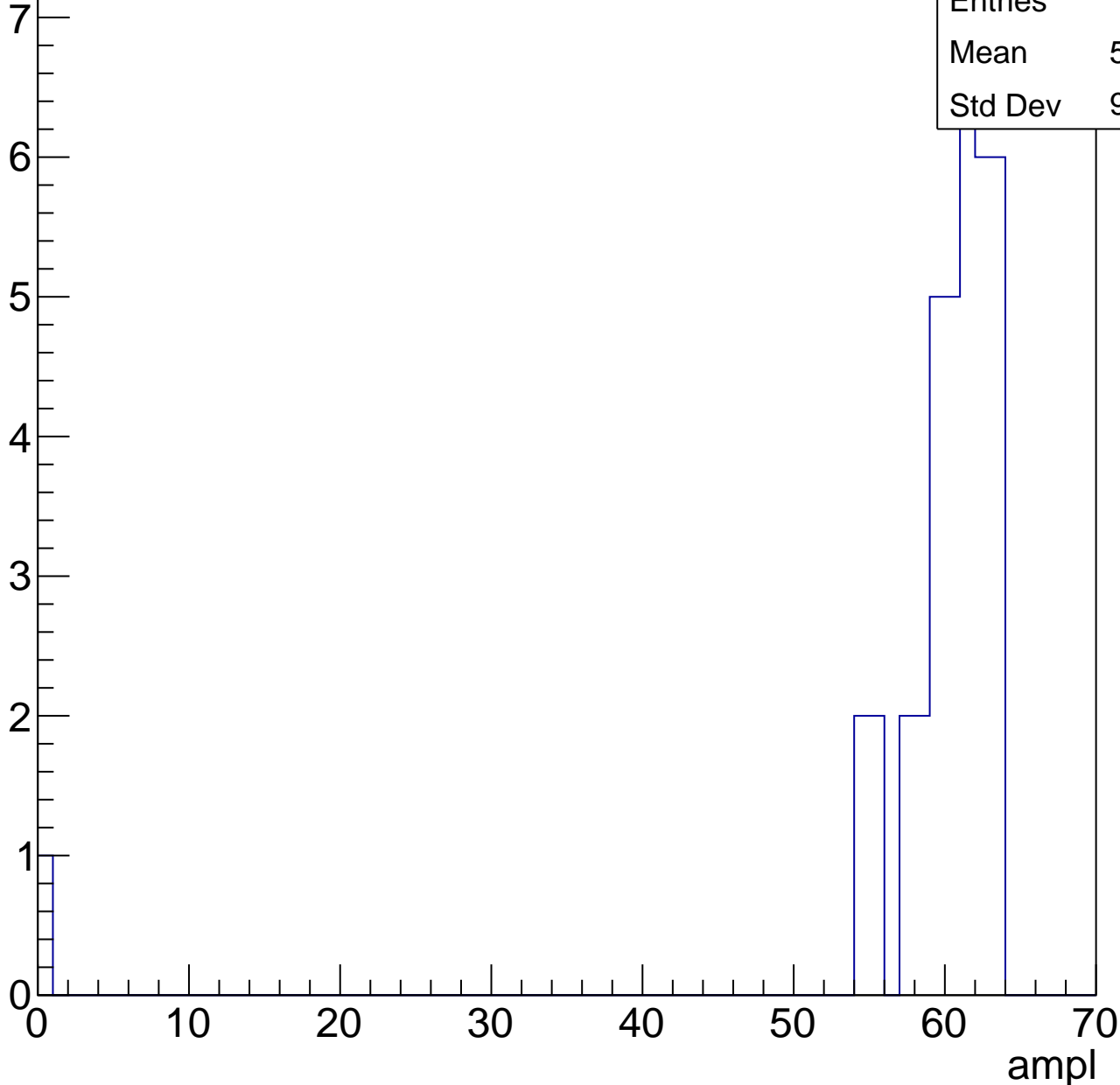


# B0L002S, U2-ch110, adc5

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	38
Mean	58.42
Std Dev	9.925



# B0L002S, U2-ch110, adc6

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry





# B0L002S, U2-ch110, adc7

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L002S, U2-ch111, adc0

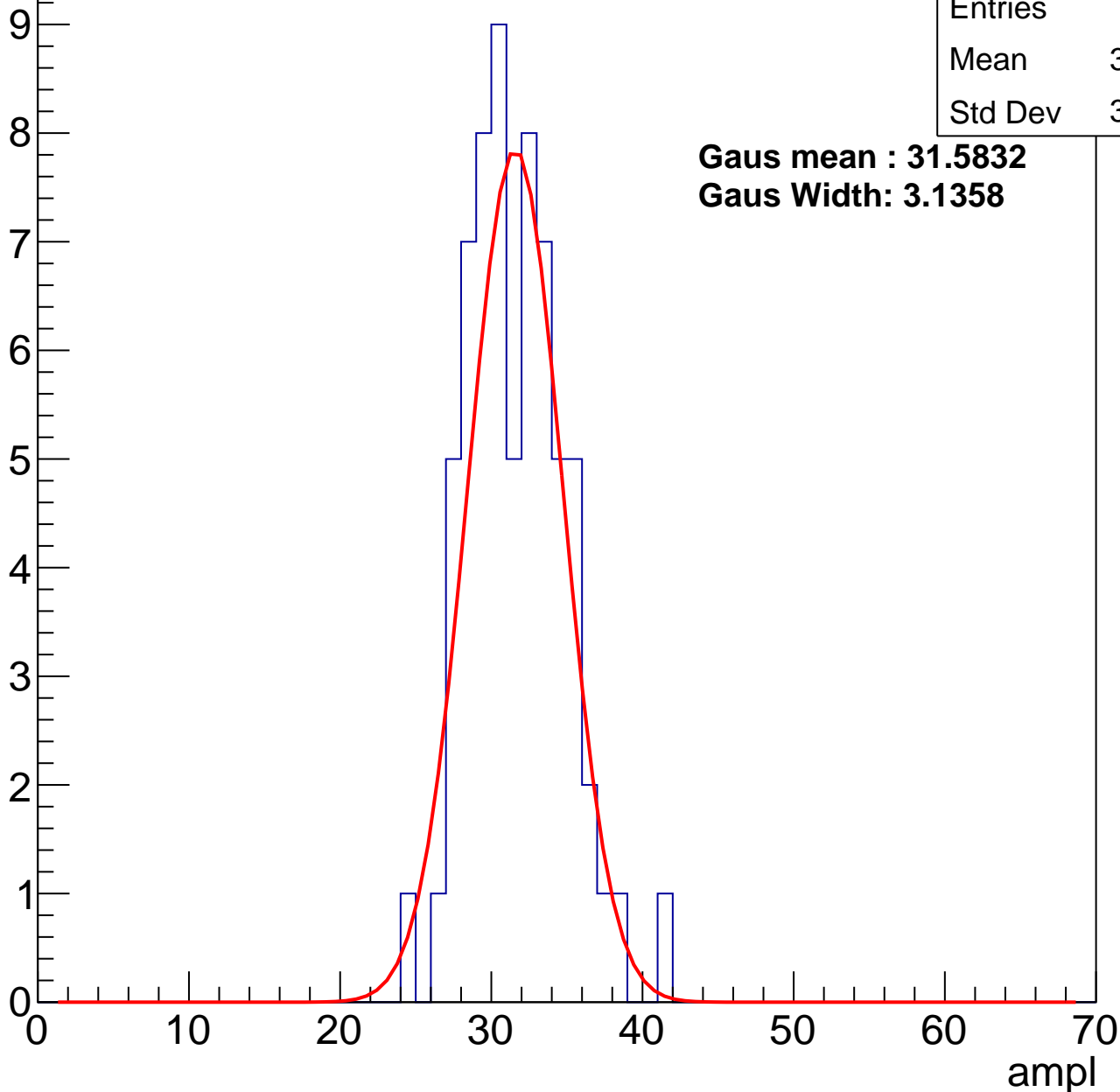
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	66
Mean	31.18
Std Dev	3.143

**Gaus mean : 31.5832**

**Gaus Width: 3.1358**



# B0L002S, U2-ch111, adc1

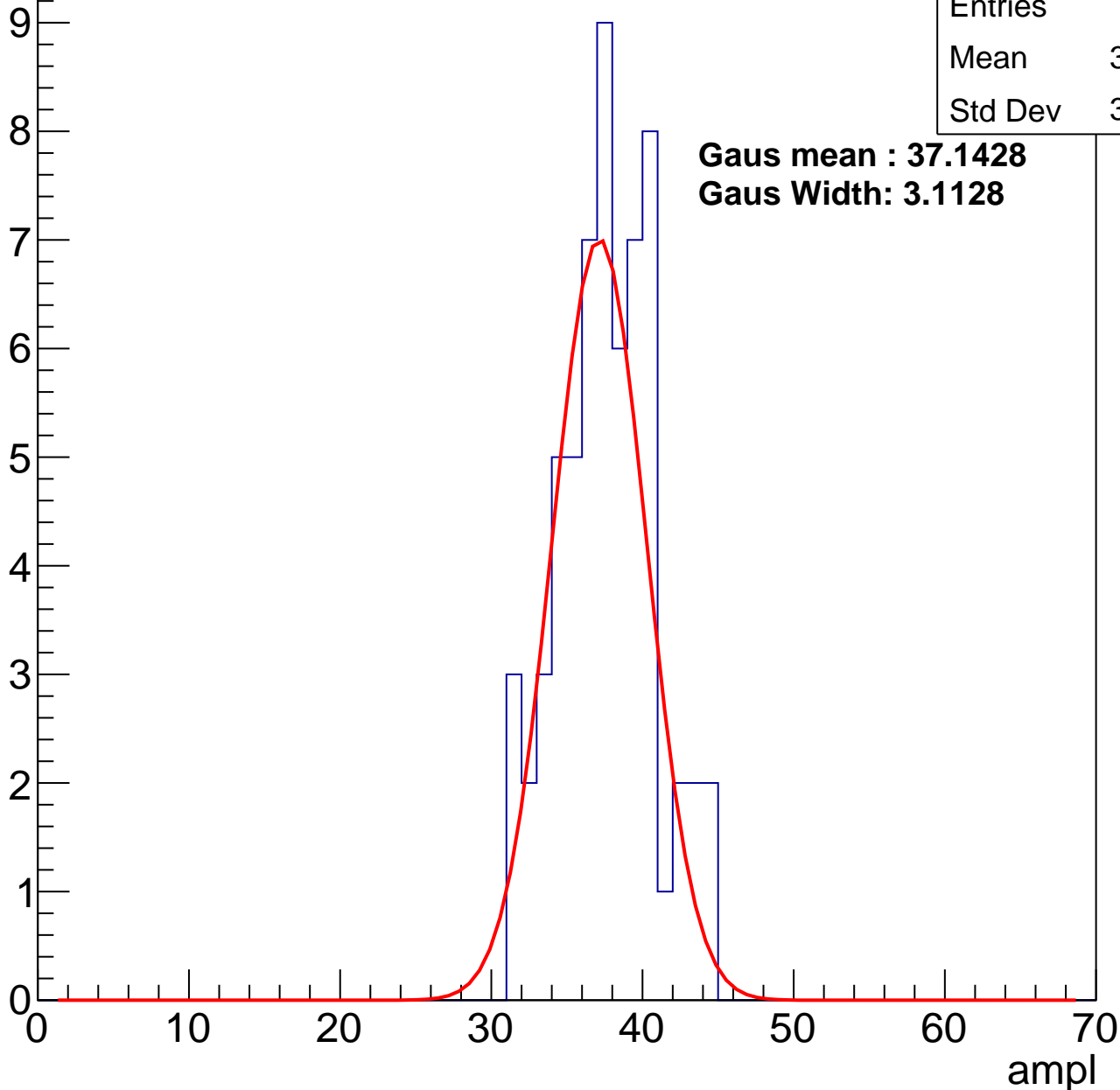
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	62
Mean	37.19
Std Dev	3.156

**Gaus mean : 37.1428**

**Gaus Width: 3.1128**



# B0L002S, U2-ch111, adc2

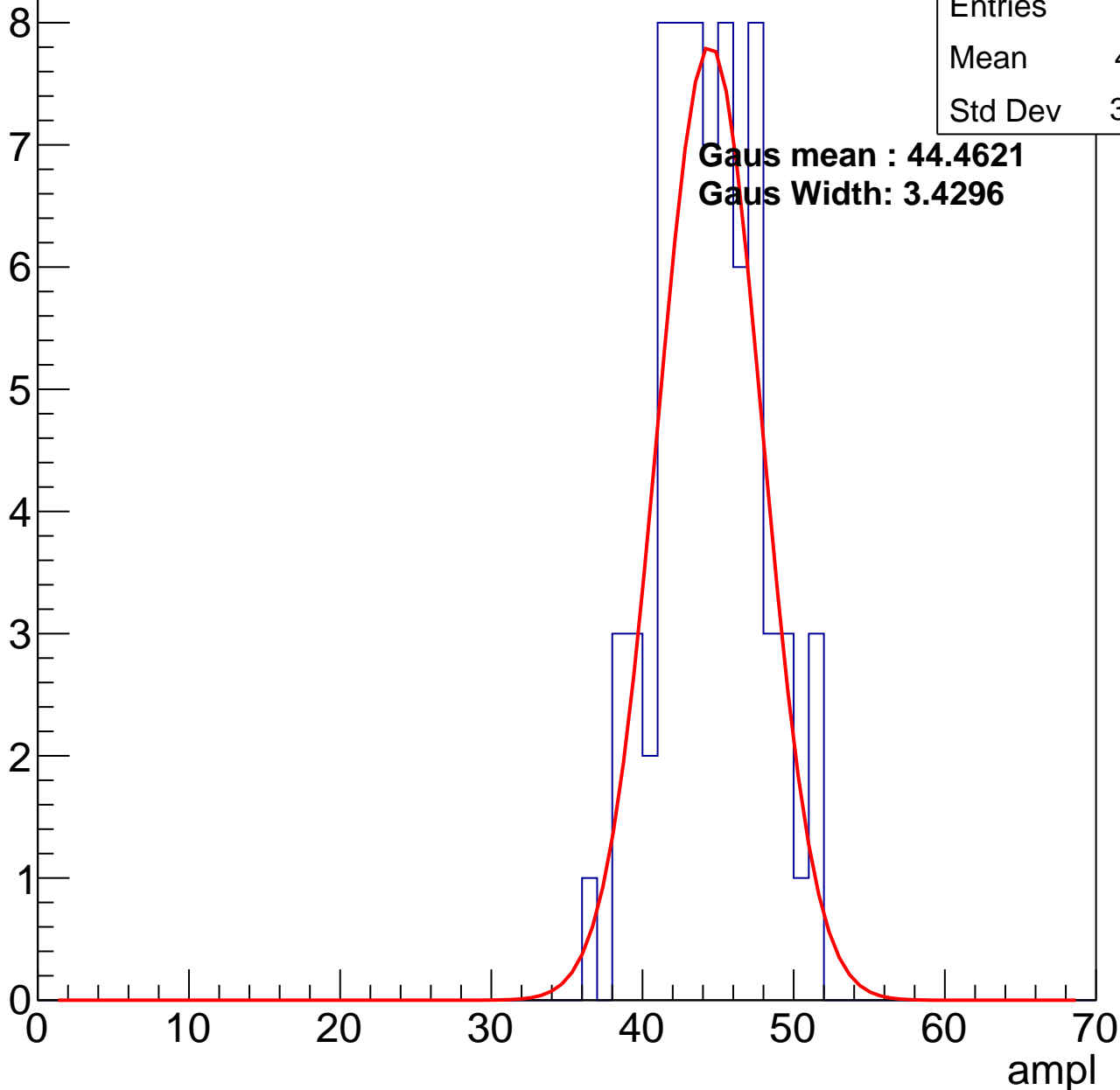
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	72
Mean	44.01
Std Dev	3.335

**Gaus mean : 44.4621**

**Gaus Width: 3.4296**

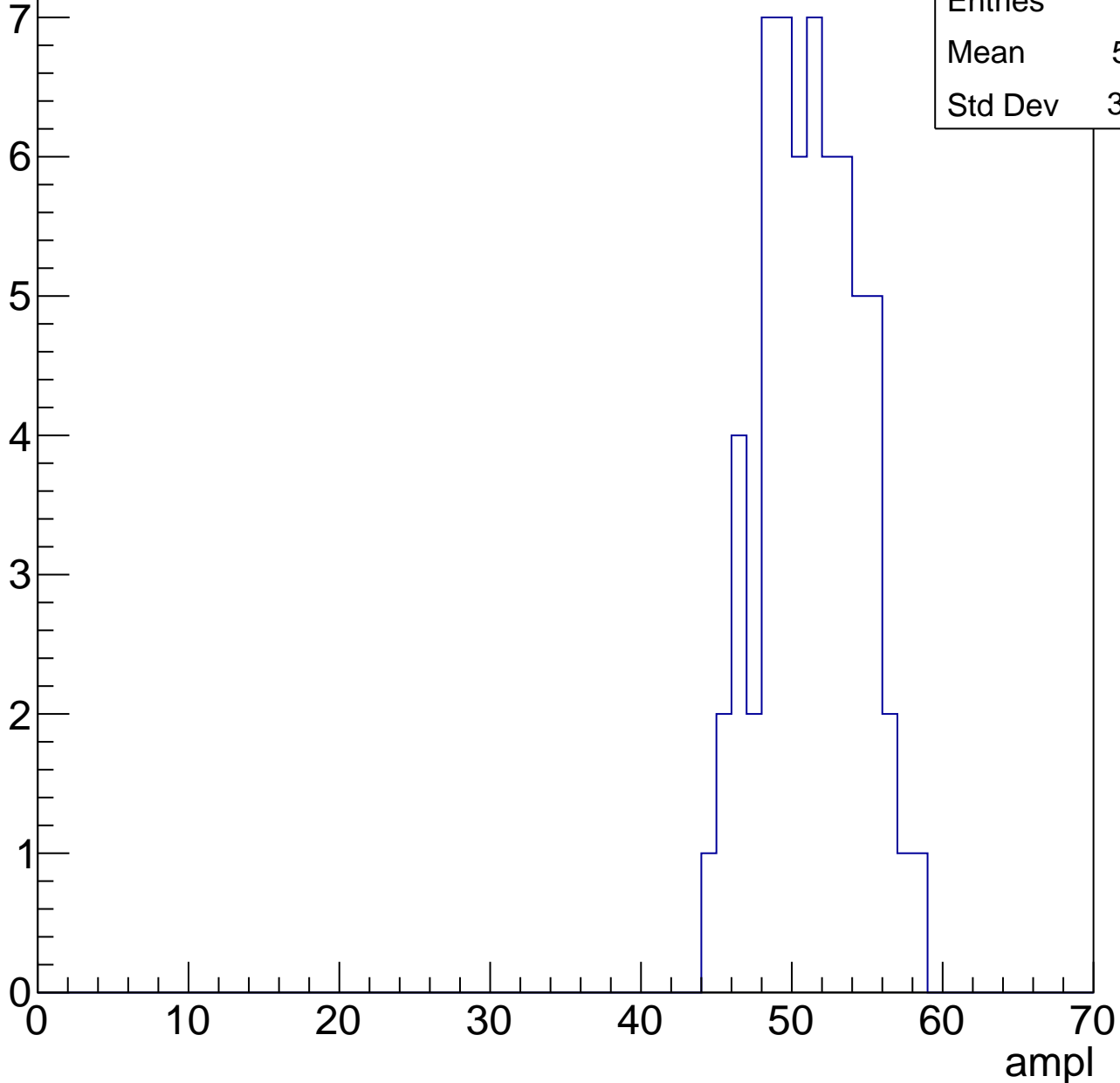


# B0L002S, U2-ch111, adc3

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

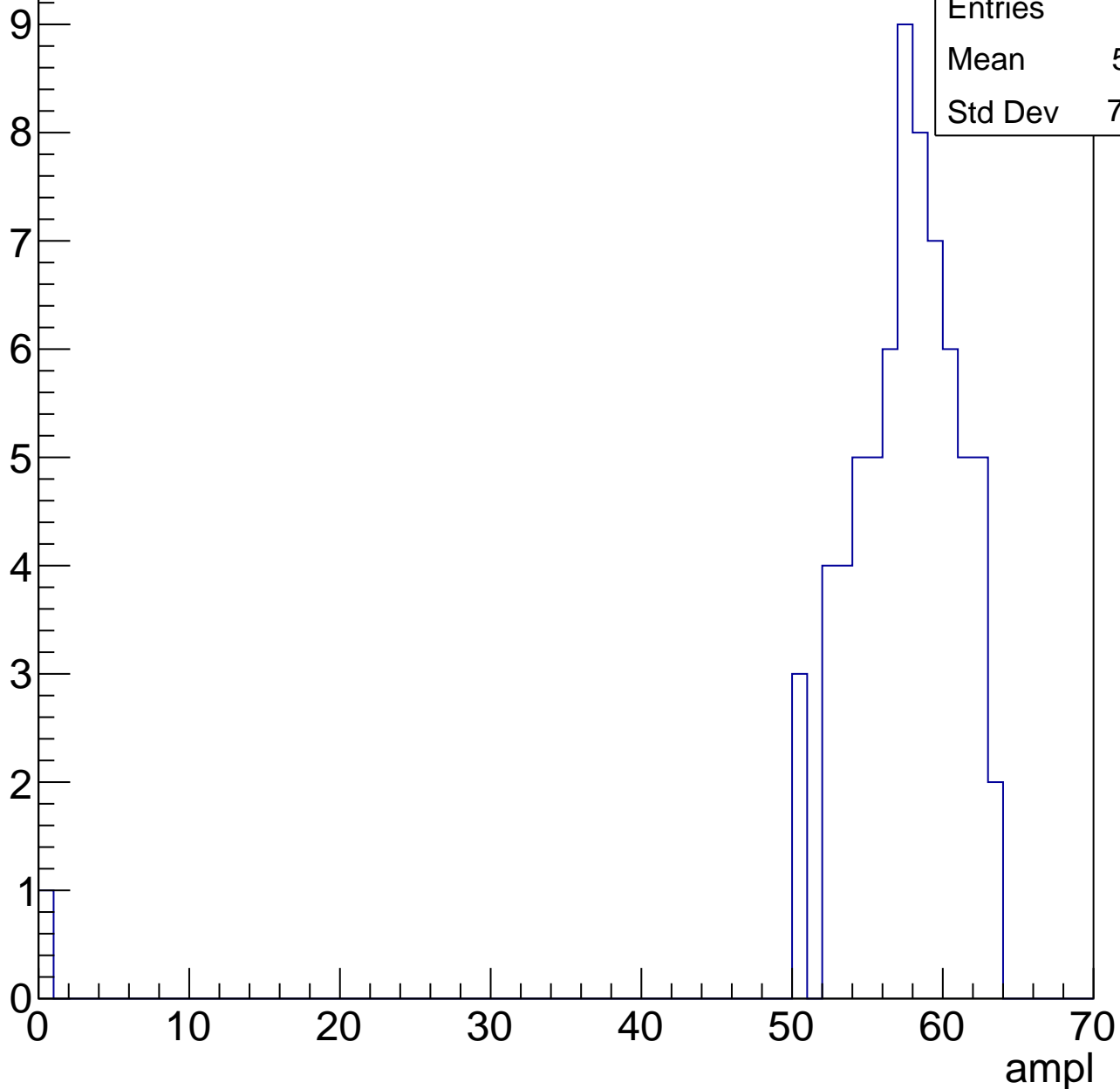
Entries	62
Mean	50.81
Std Dev	3.207



# B0L002S, U2-ch111, adc4

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

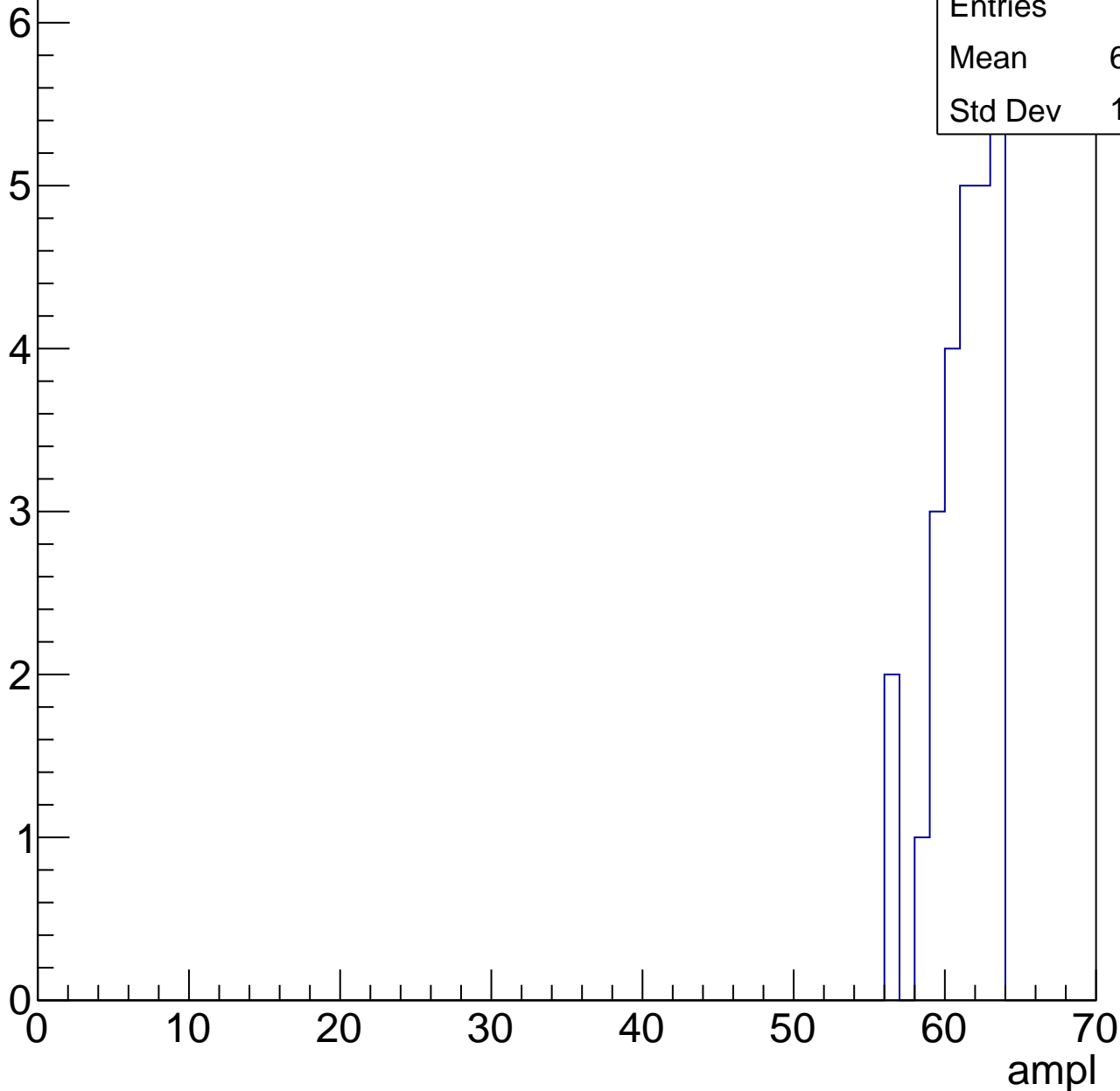


# B0L002S, U2-ch111, adc5

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	26
Mean	60.77
Std Dev	1.987



# B0L002S, U2-ch111, adc6

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry





# B0L002S, U2-ch111, adc7

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



# B0L002S, U2-ch112, adc0

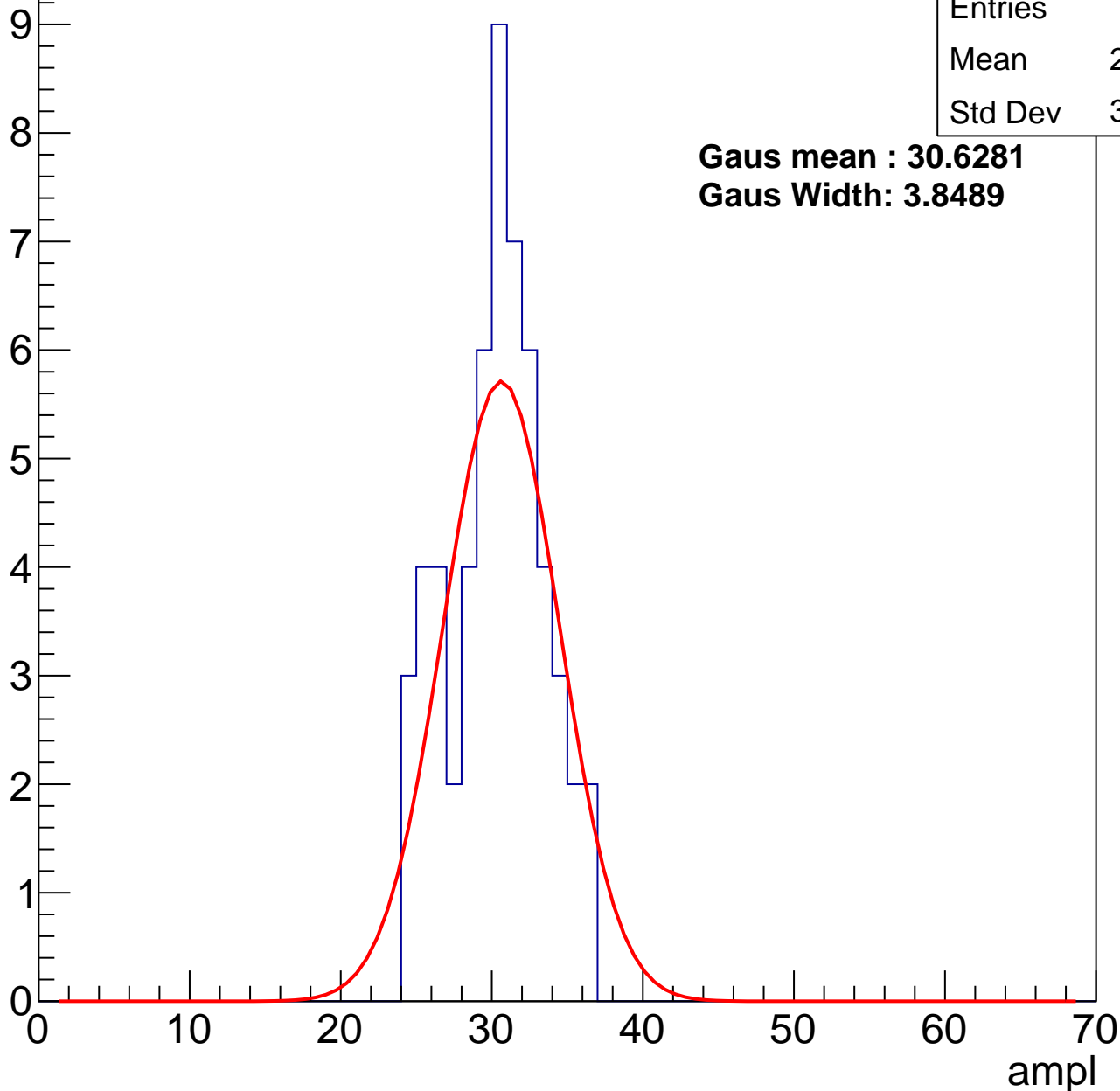
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	56
Mean	29.84
Std Dev	3.127

**Gaus mean : 30.6281**

**Gaus Width: 3.8489**



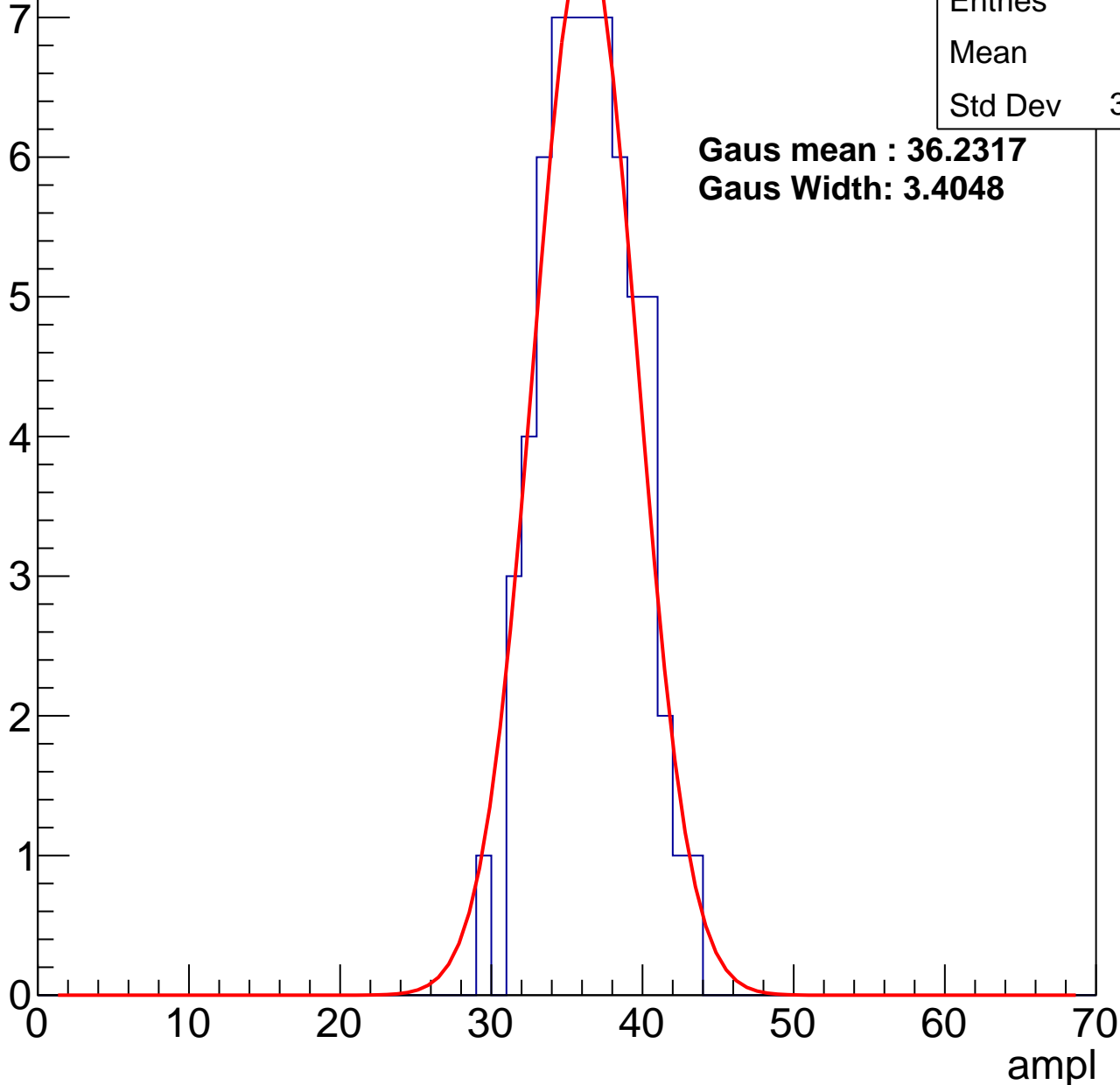
# B0L002S, U2-ch112, adc1

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	62
Mean	36
Std Dev	3.027

**Gaus mean : 36.2317**  
**Gaus Width: 3.4048**



# B0L002S, U2-ch112, adc2

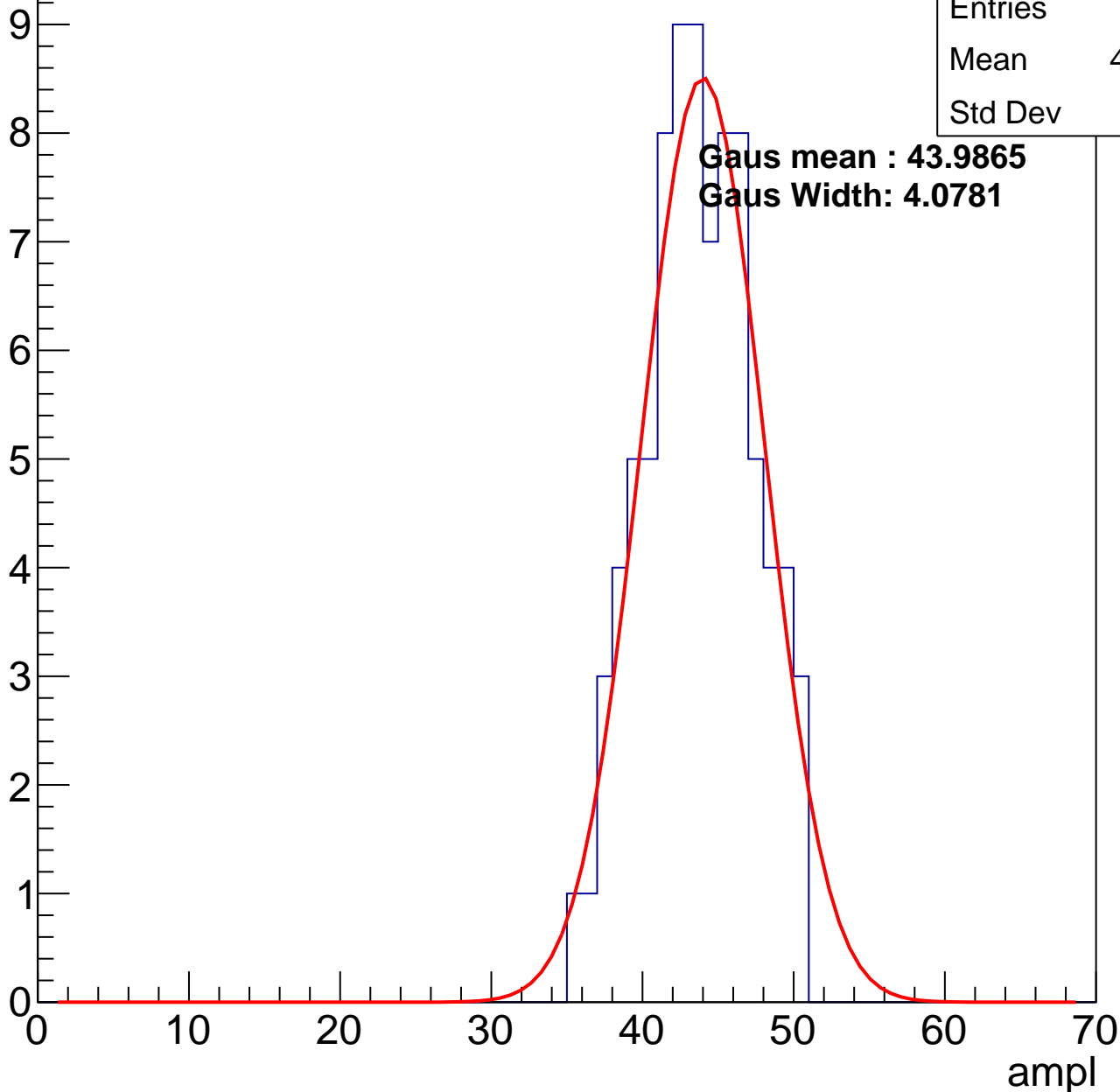
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	84
Mean	43.23
Std Dev	3.56

**Gaus mean : 43.9865**

**Gaus Width: 4.0781**

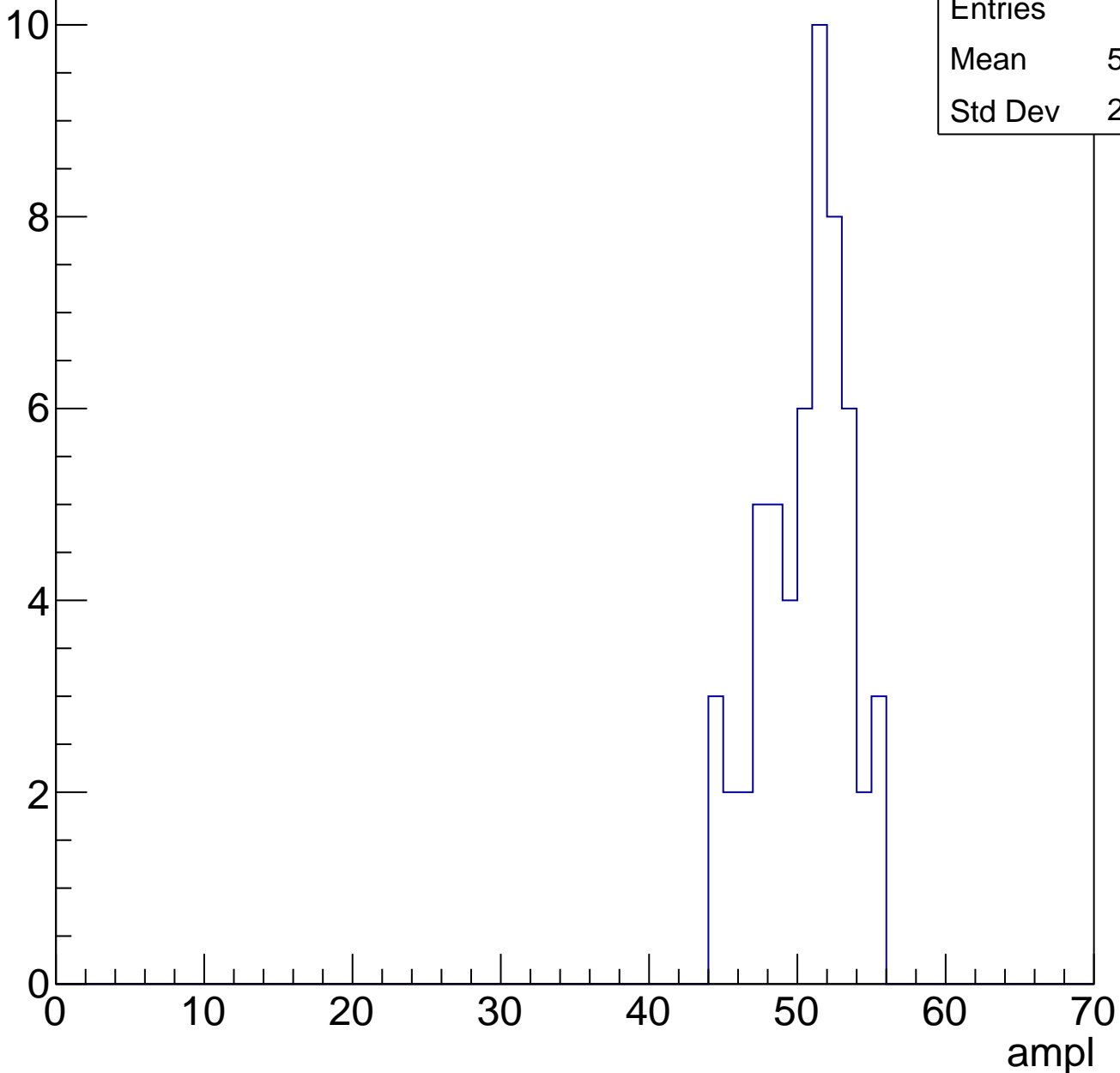


# B0L002S, U2-ch112, adc3

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	56
Mean	50.04
Std Dev	2.872

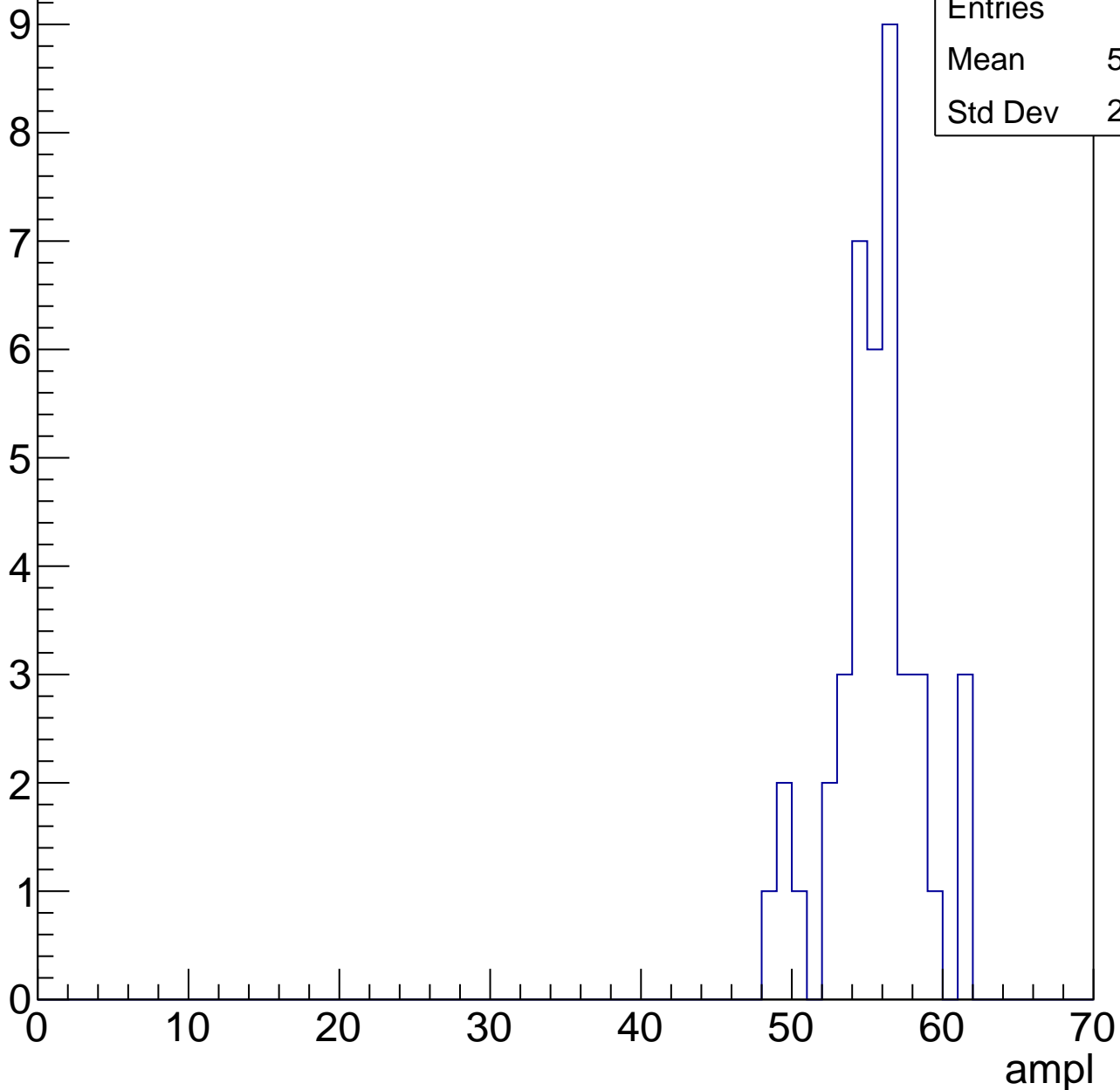


# B0L002S, U2-ch112, adc4

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	41
Mean	55.07
Std Dev	2.942

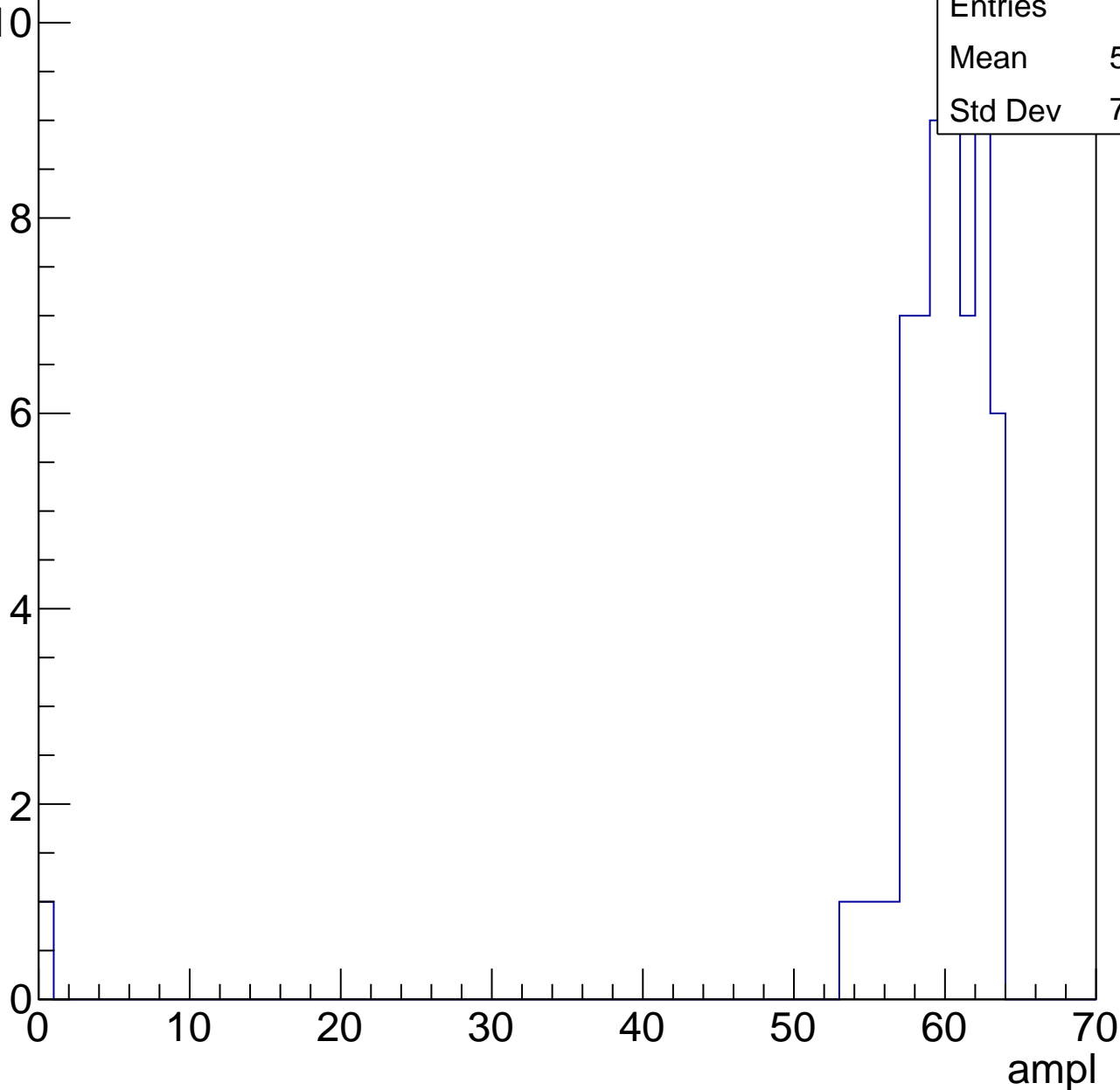


# B0L002S, U2-ch112, adc5

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

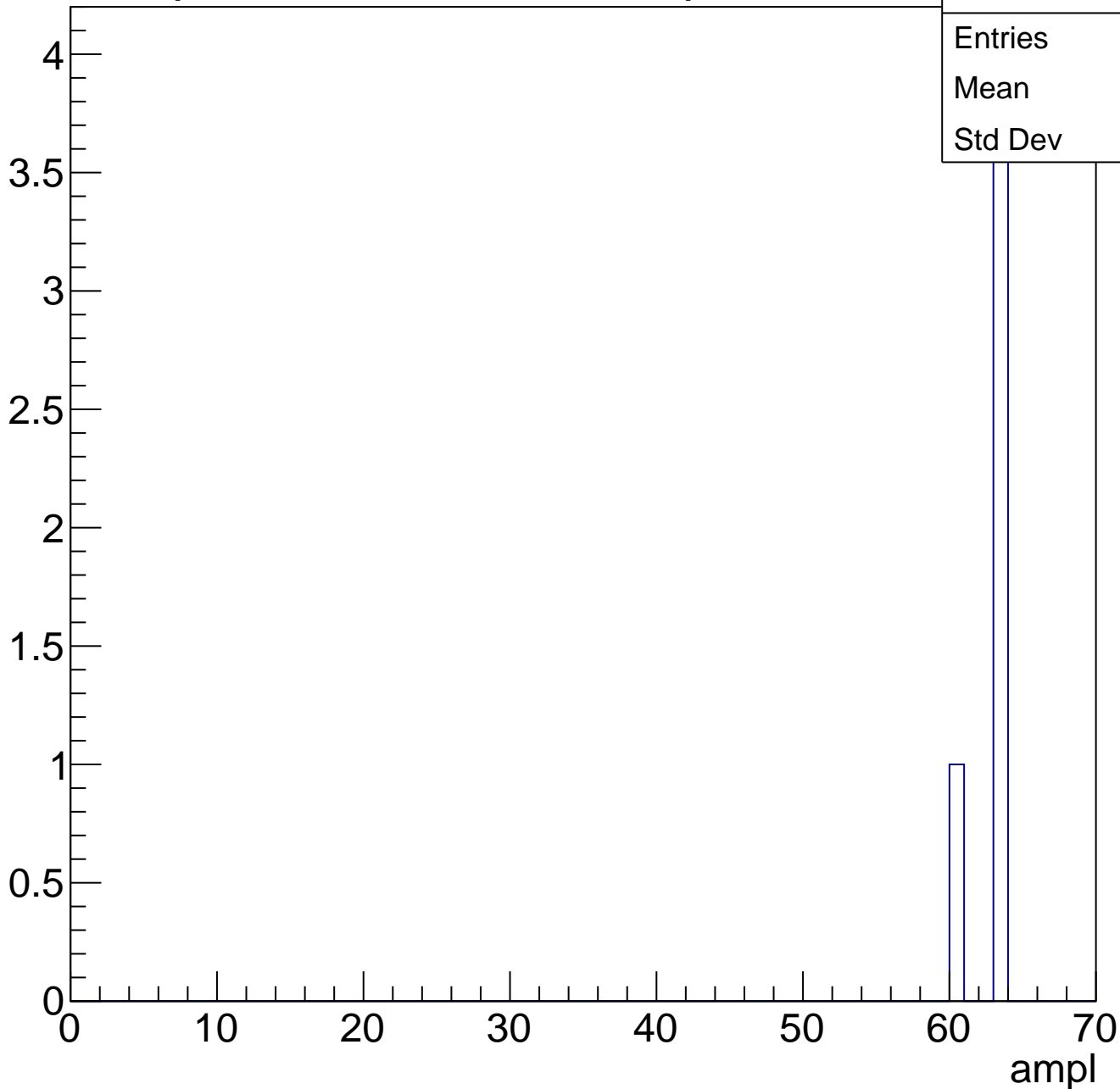
Entries	60
Mean	58.65
Std Dev	7.977



# B0L002S, U2-ch112, adc6

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry





# B0L002S, U2-ch112, adc7

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



Entries	1
Mean	23
Std Dev	0

# B0L002S, U2-ch113, adc0

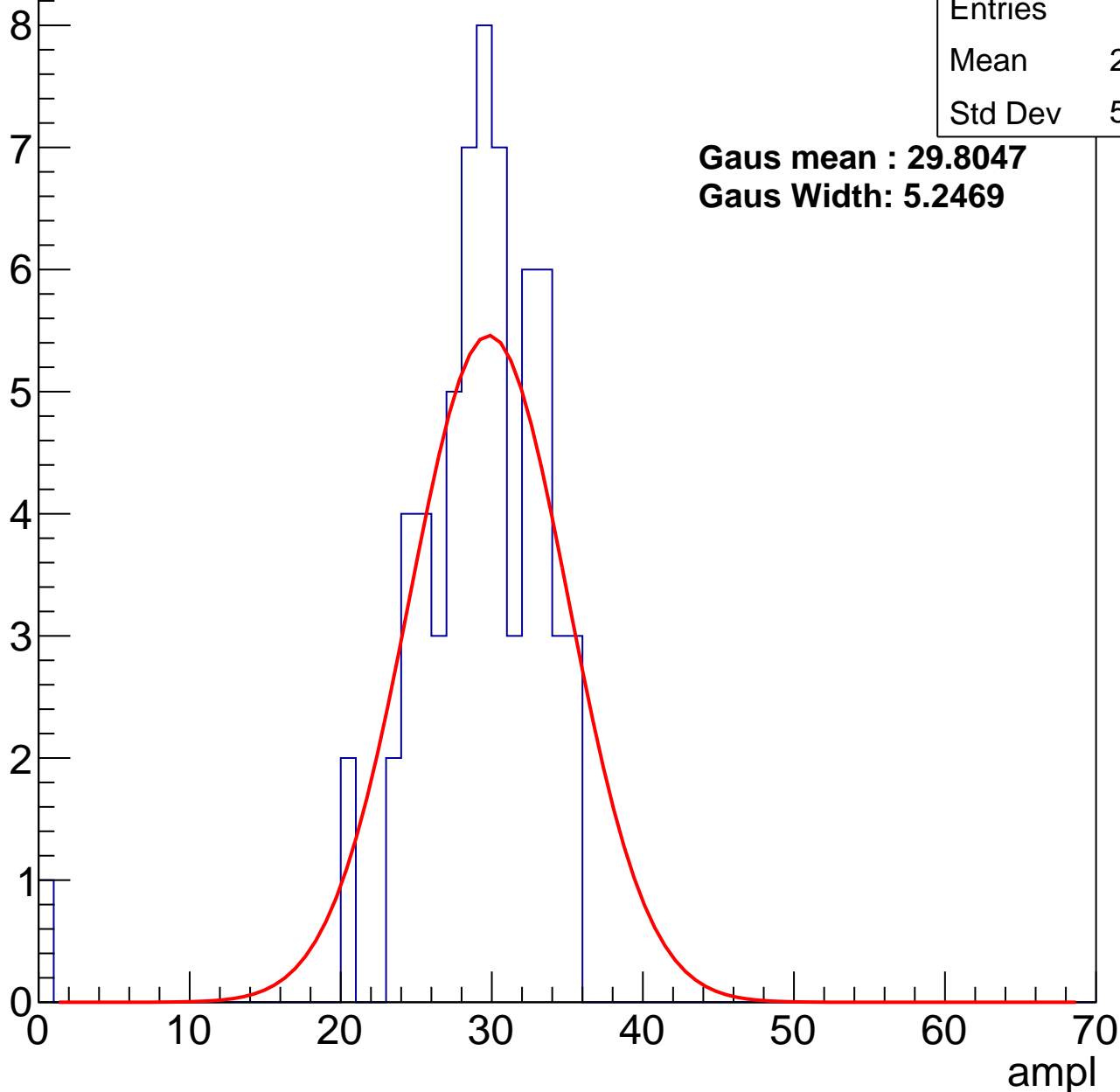
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	64
Mean	28.48
Std Dev	5.044

**Gaus mean : 29.8047**

**Gaus Width: 5.2469**



# B0L002S, U2-ch113, adc1

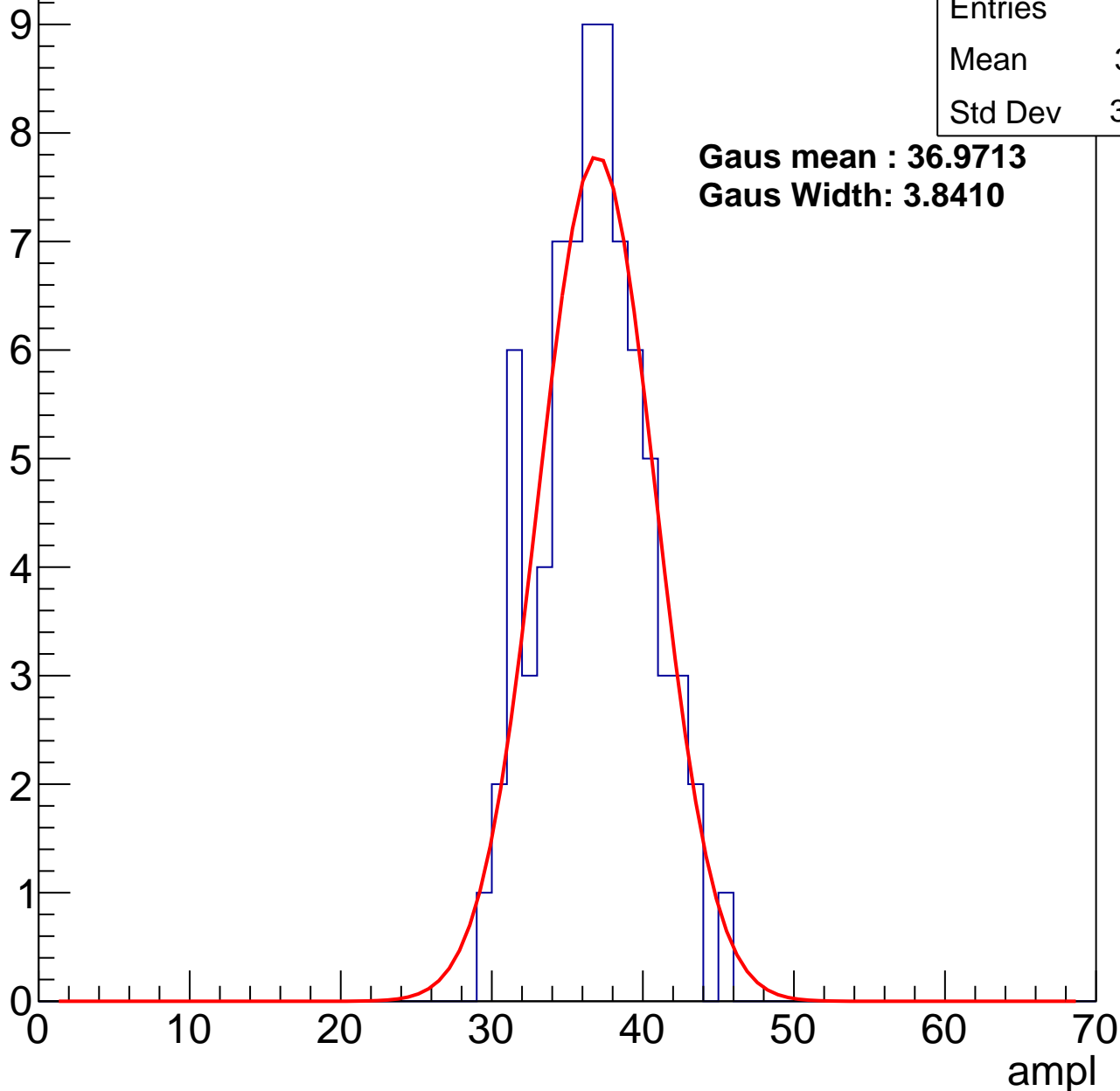
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	75
Mean	36.31
Std Dev	3.495

**Gaus mean : 36.9713**

**Gaus Width: 3.8410**



# B0L002S, U2-ch113, adc2

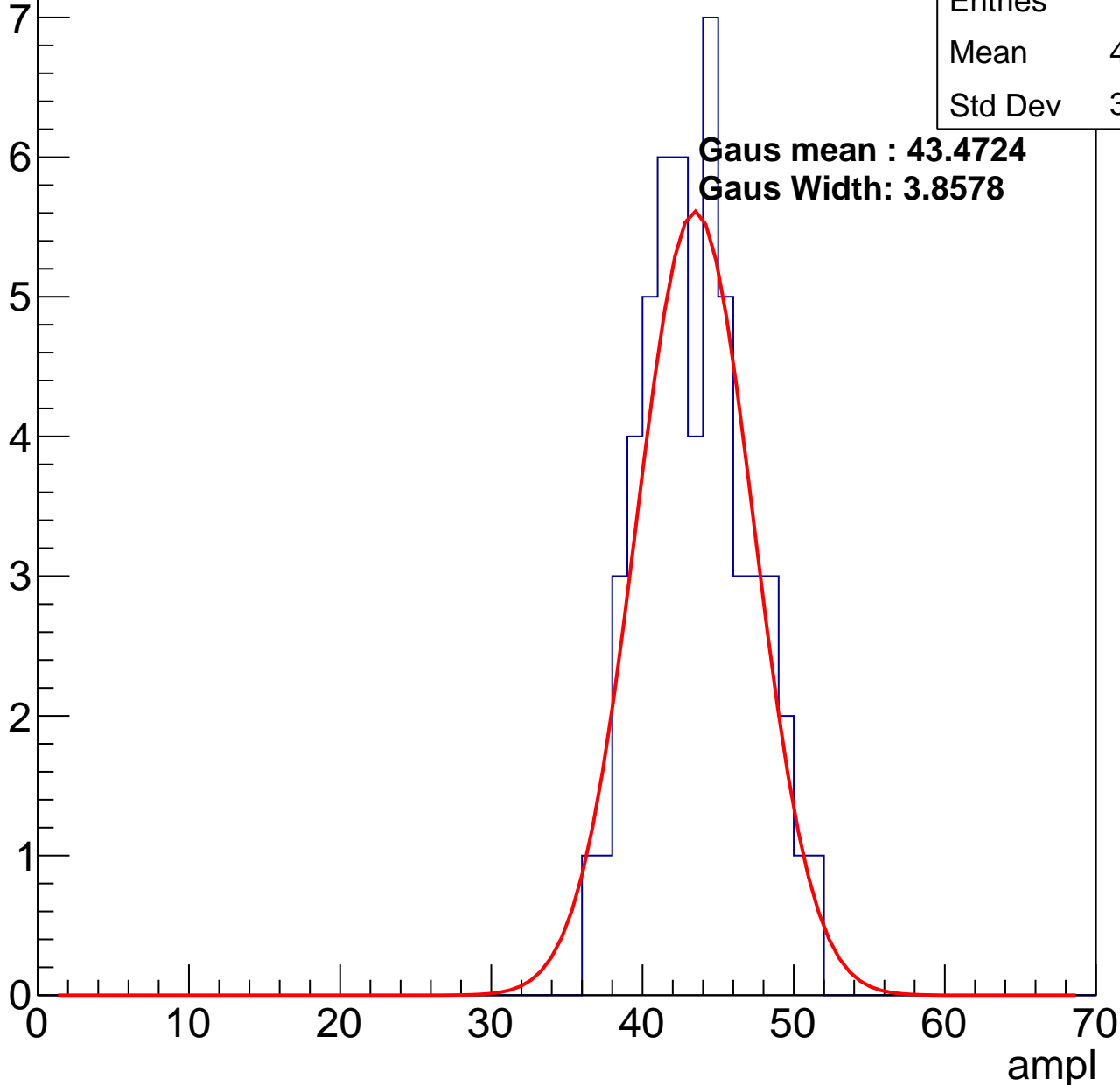
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	55
Mean	43.05
Std Dev	3.466

**Gaus mean : 43.4724**

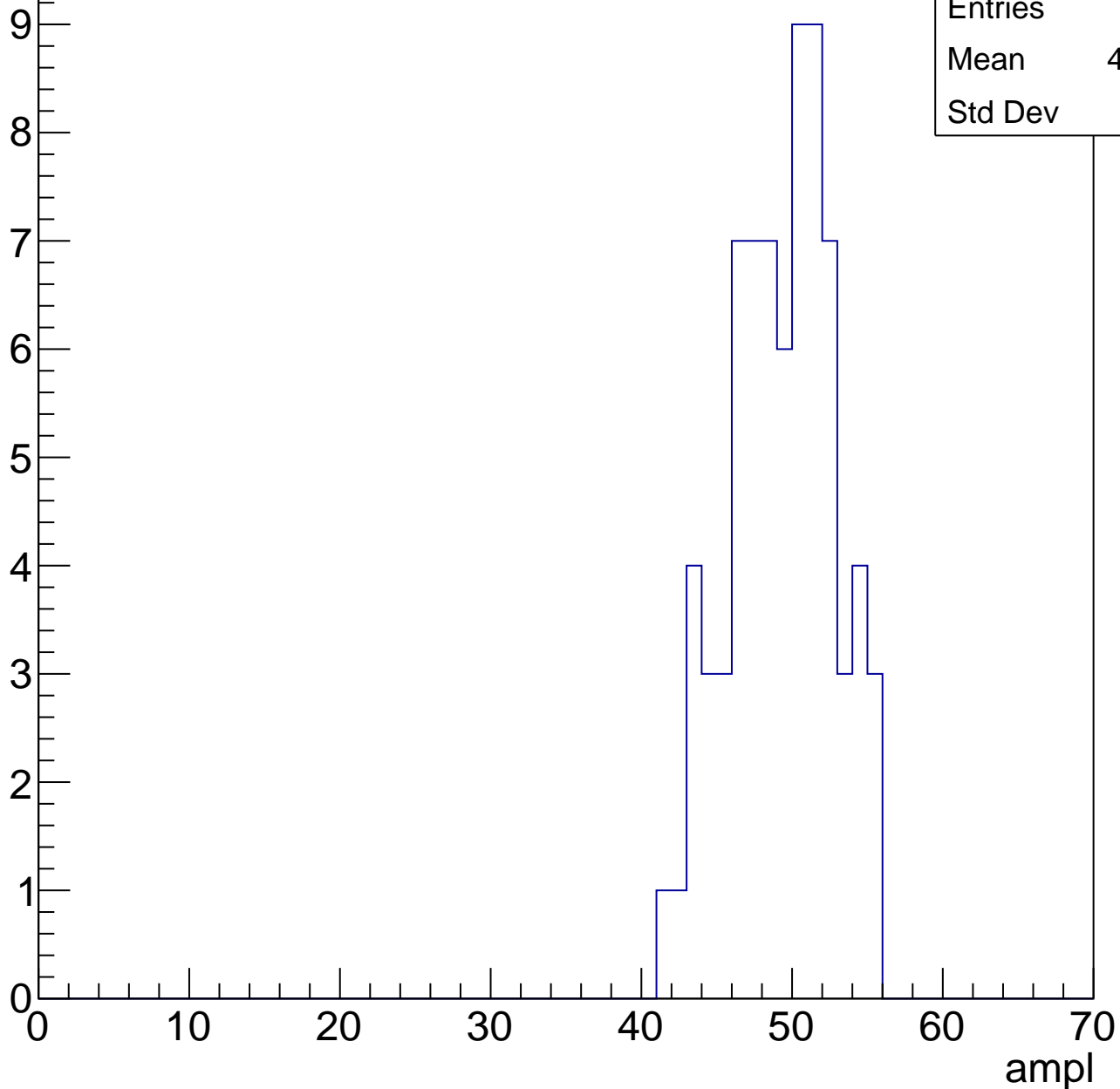
**Gaus Width: 3.8578**



# B0L002S, U2-ch113, adc3

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

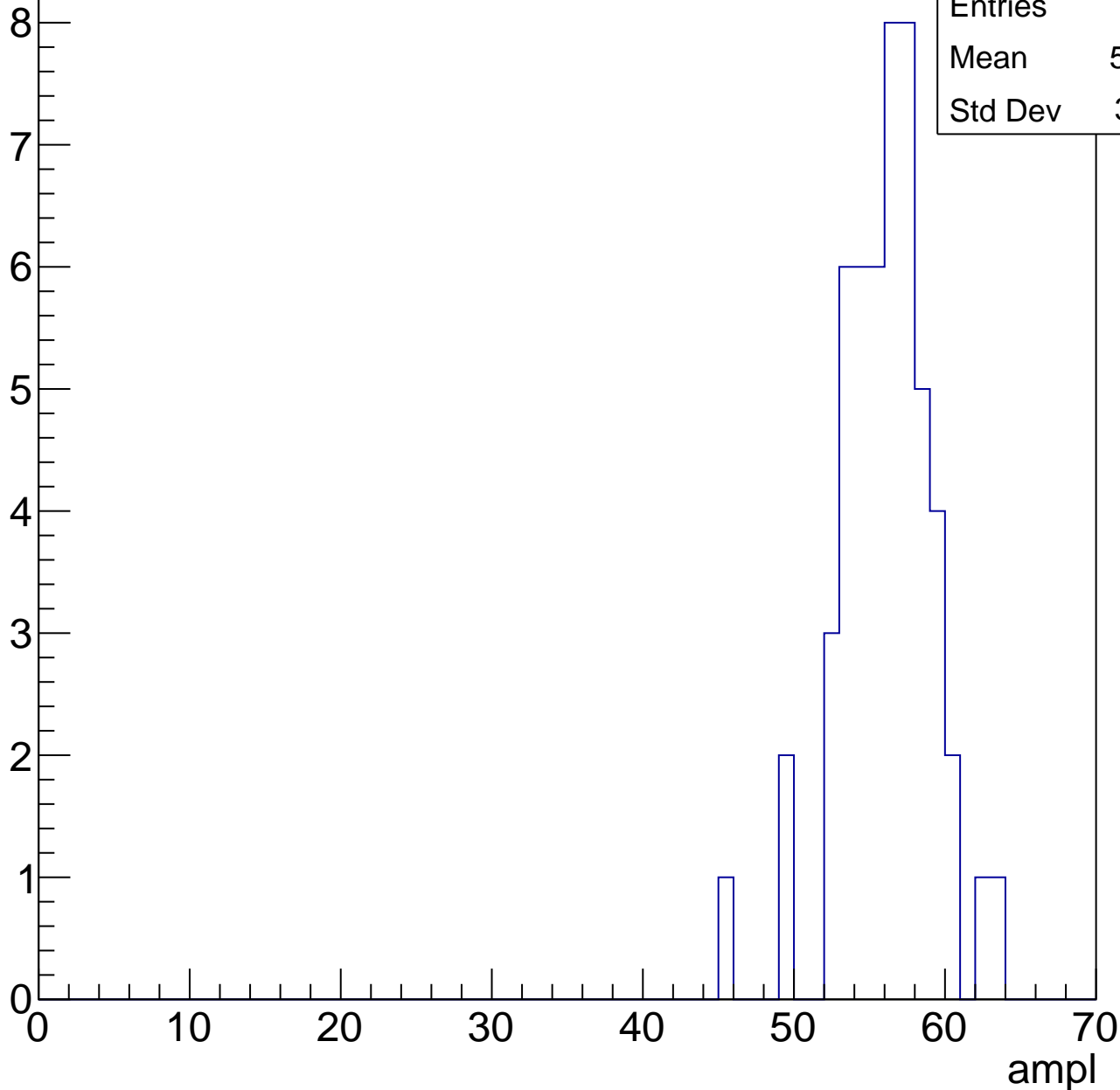


# B0L002S, U2-ch113, adc4

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	53
Mean	55.58
Std Dev	3.141

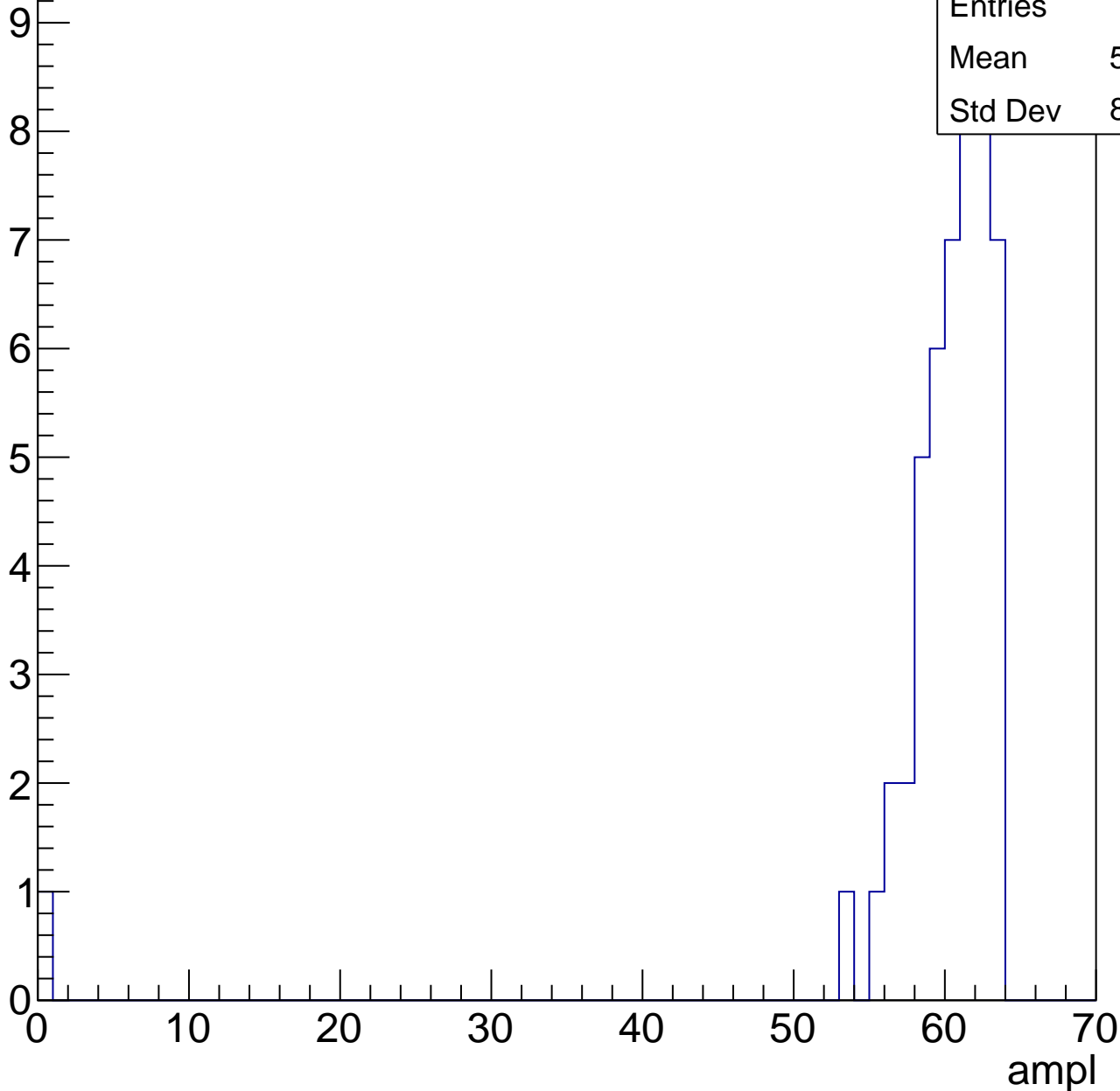


# B0L002S, U2-ch113, adc5

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	50
Mean	58.92
Std Dev	8.717



# B0L002S, U2-ch113, adc6

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry





# B0L002S, U2-ch113, adc7

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L002S, U2-ch114, adc0

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entries	93
Mean	29.98
Std Dev	6.625

**Gaus mean : 31.7204**

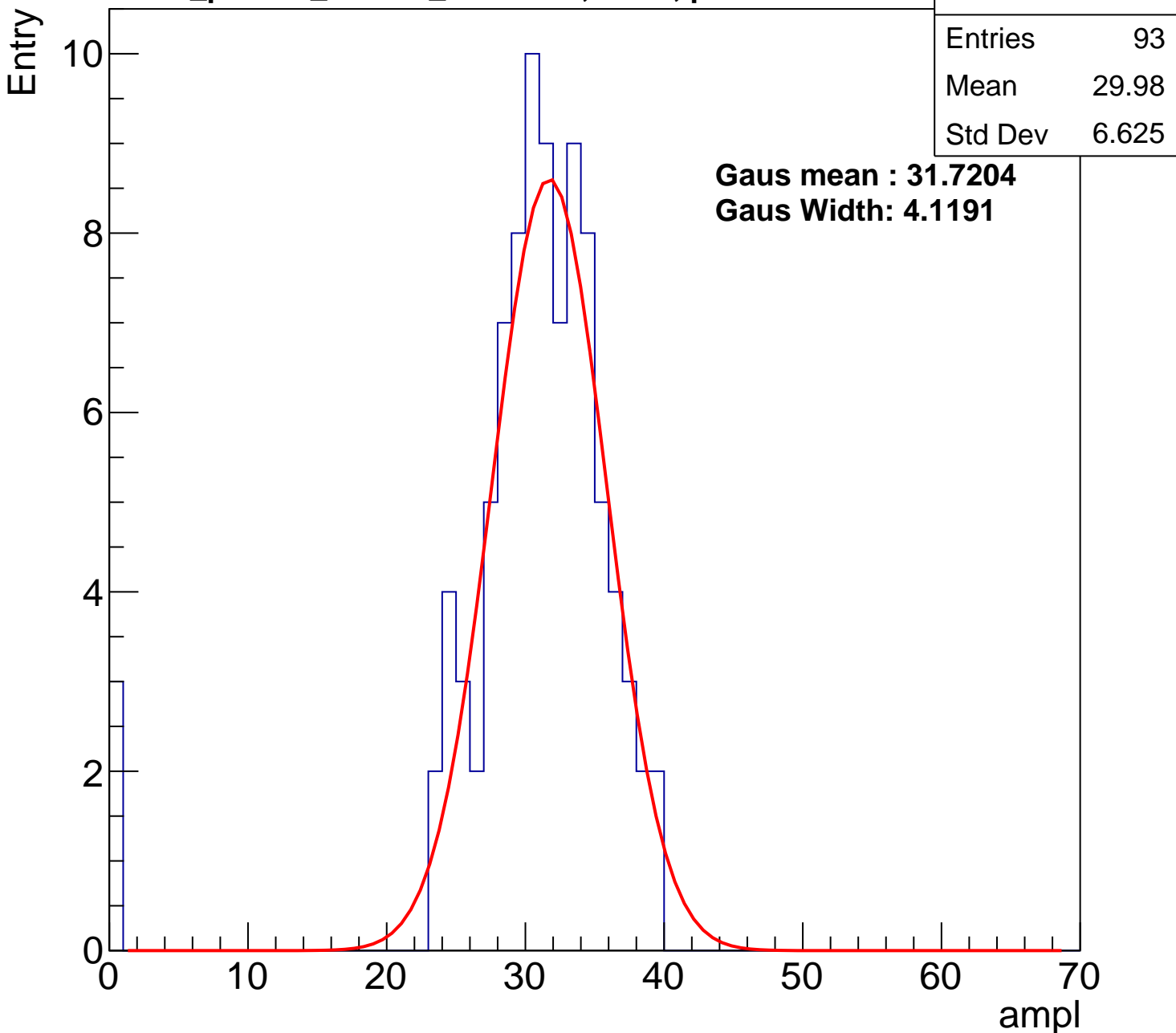
**Gaus Width: 4.1191**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



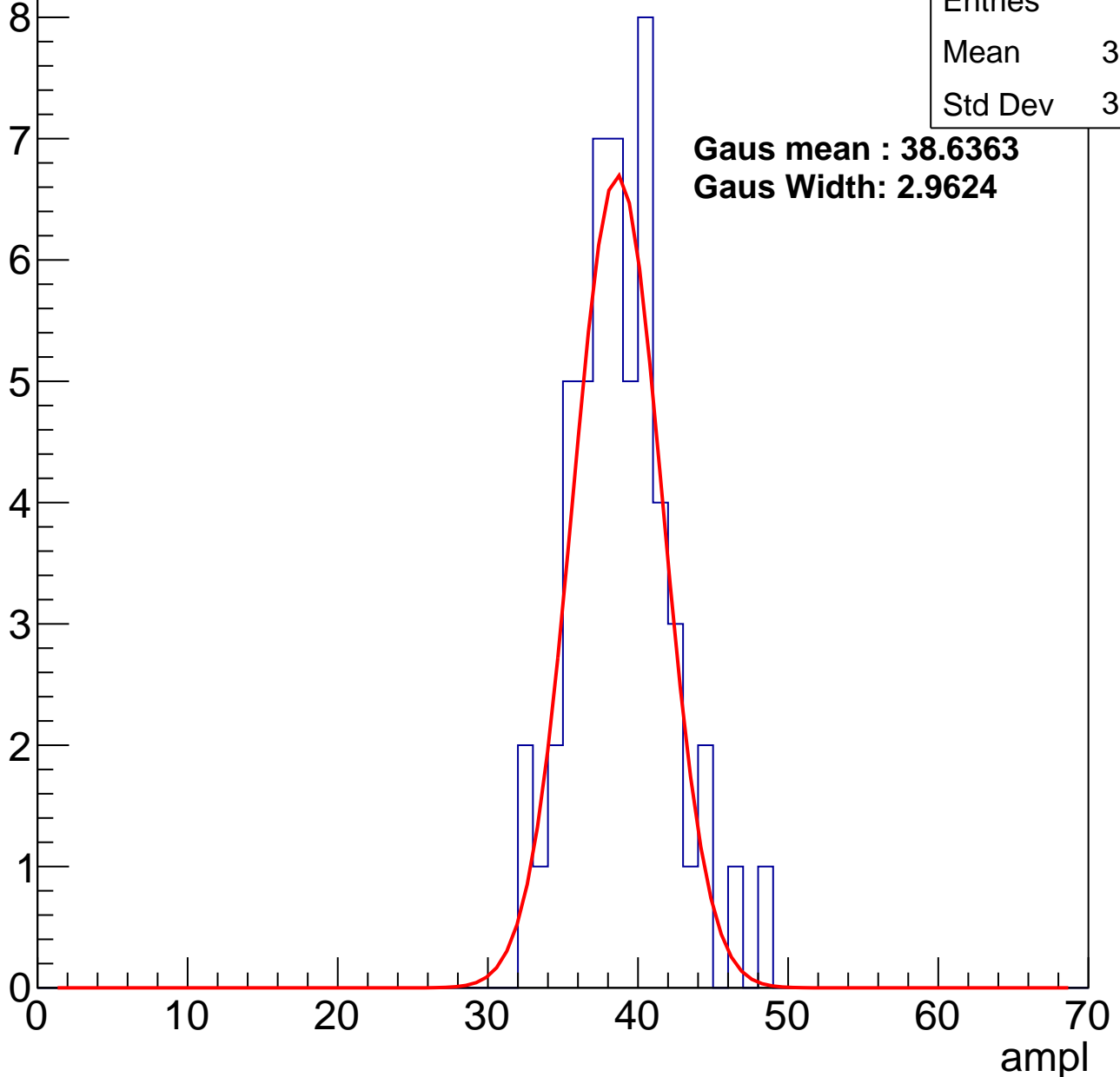
# B0L002S, U2-ch114, adc1

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

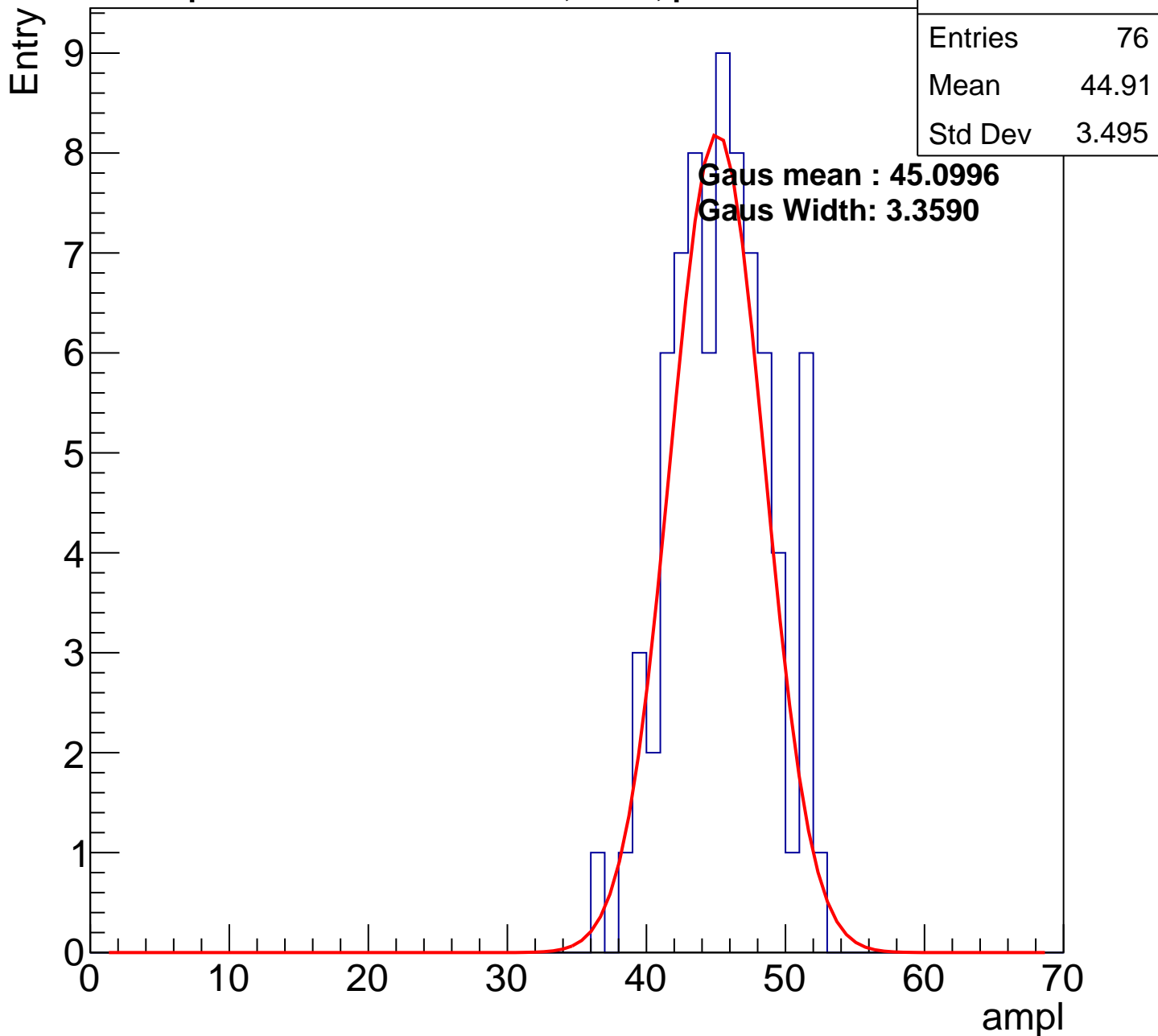
Entries	54
Mean	38.43
Std Dev	3.258

**Gaus mean : 38.6363**  
**Gaus Width: 2.9624**



# B0L002S, U2-ch114, adc2

calib\_packv5\_042523\_0143.root, FC#8, port C1

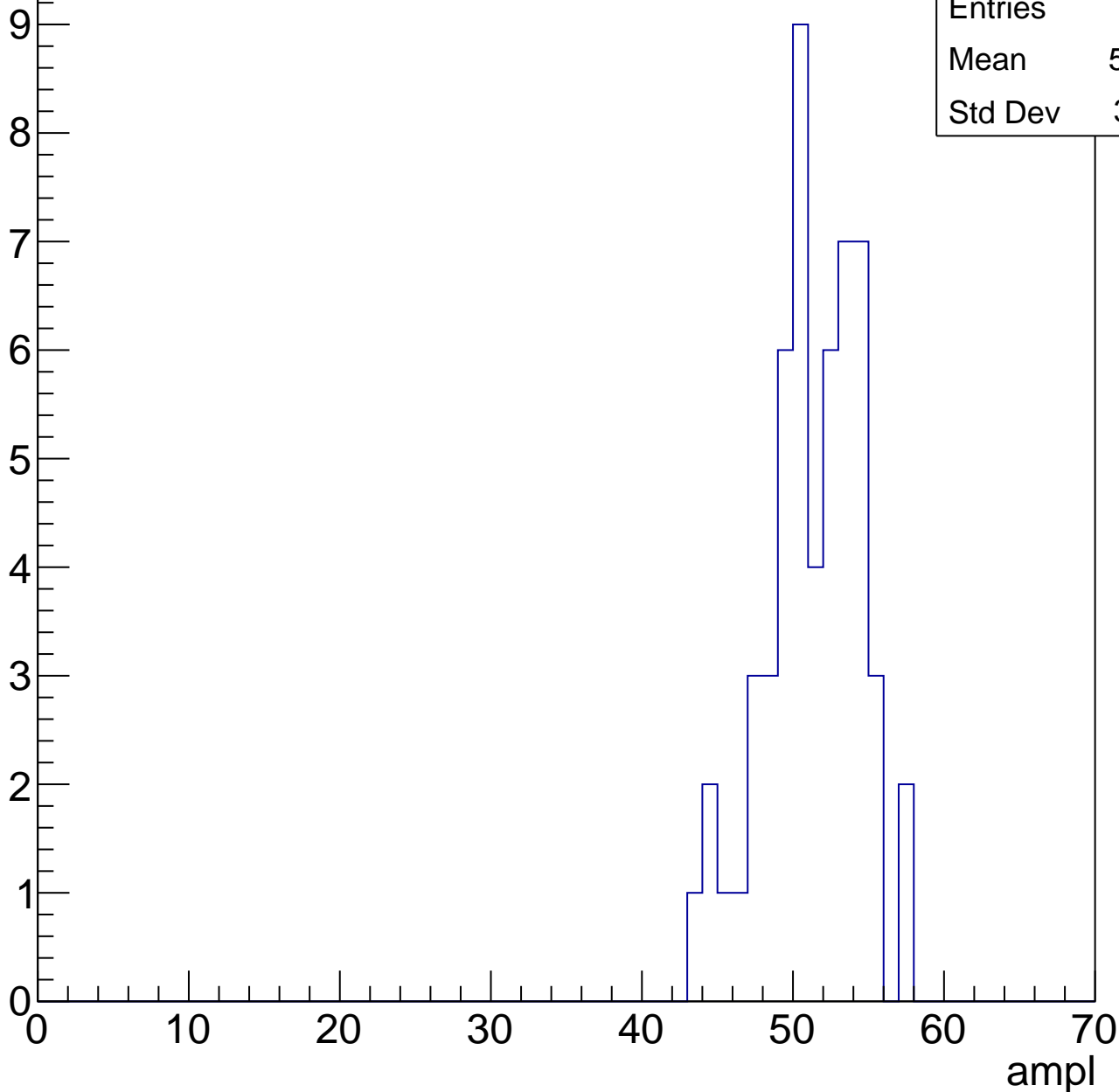


# B0L002S, U2-ch114, adc3

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

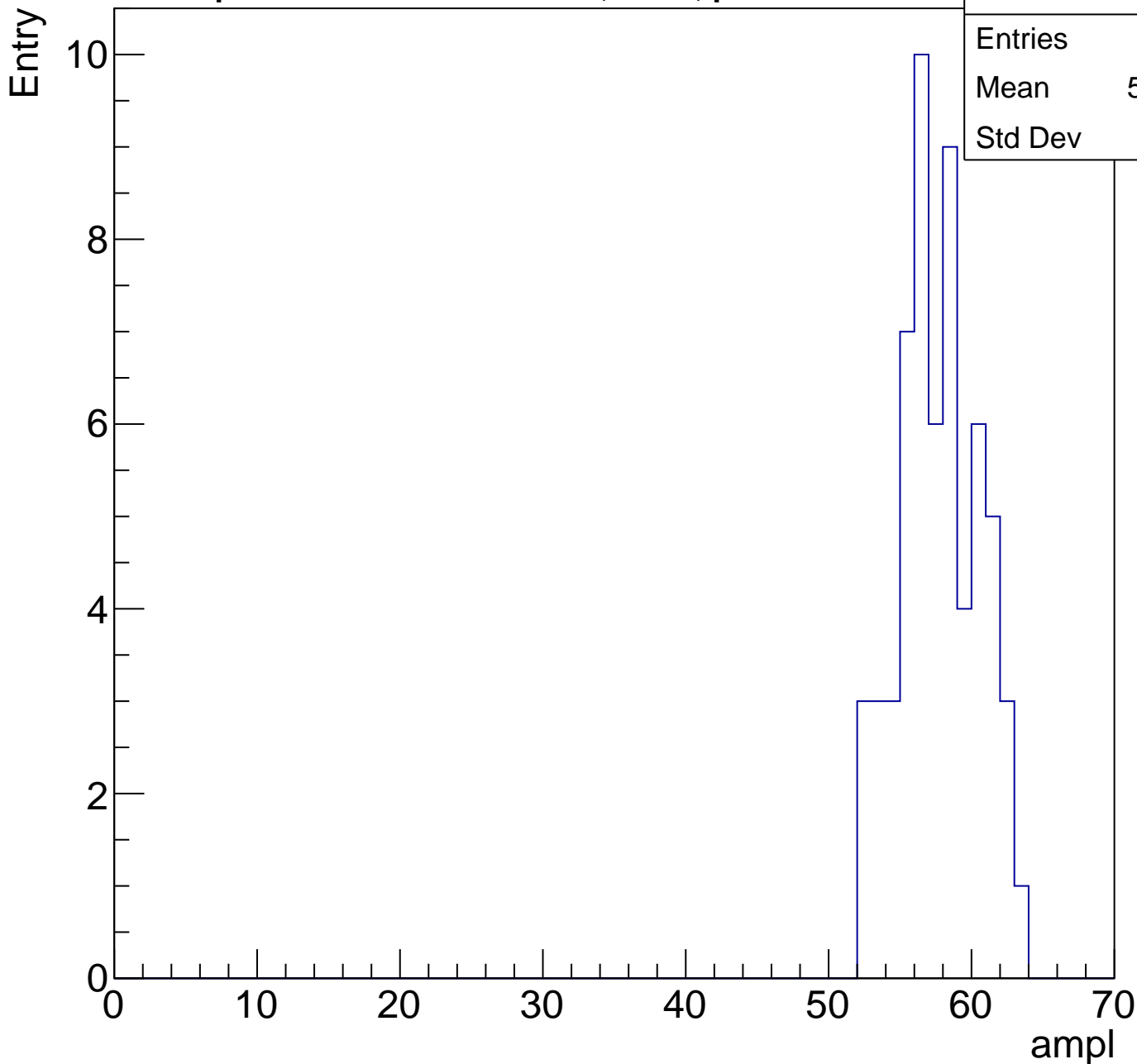
Entries	55
Mean	50.82
Std Dev	3.151



# B0L002S, U2-ch114, adc4

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entries	60
Mean	57.27
Std Dev	2.75

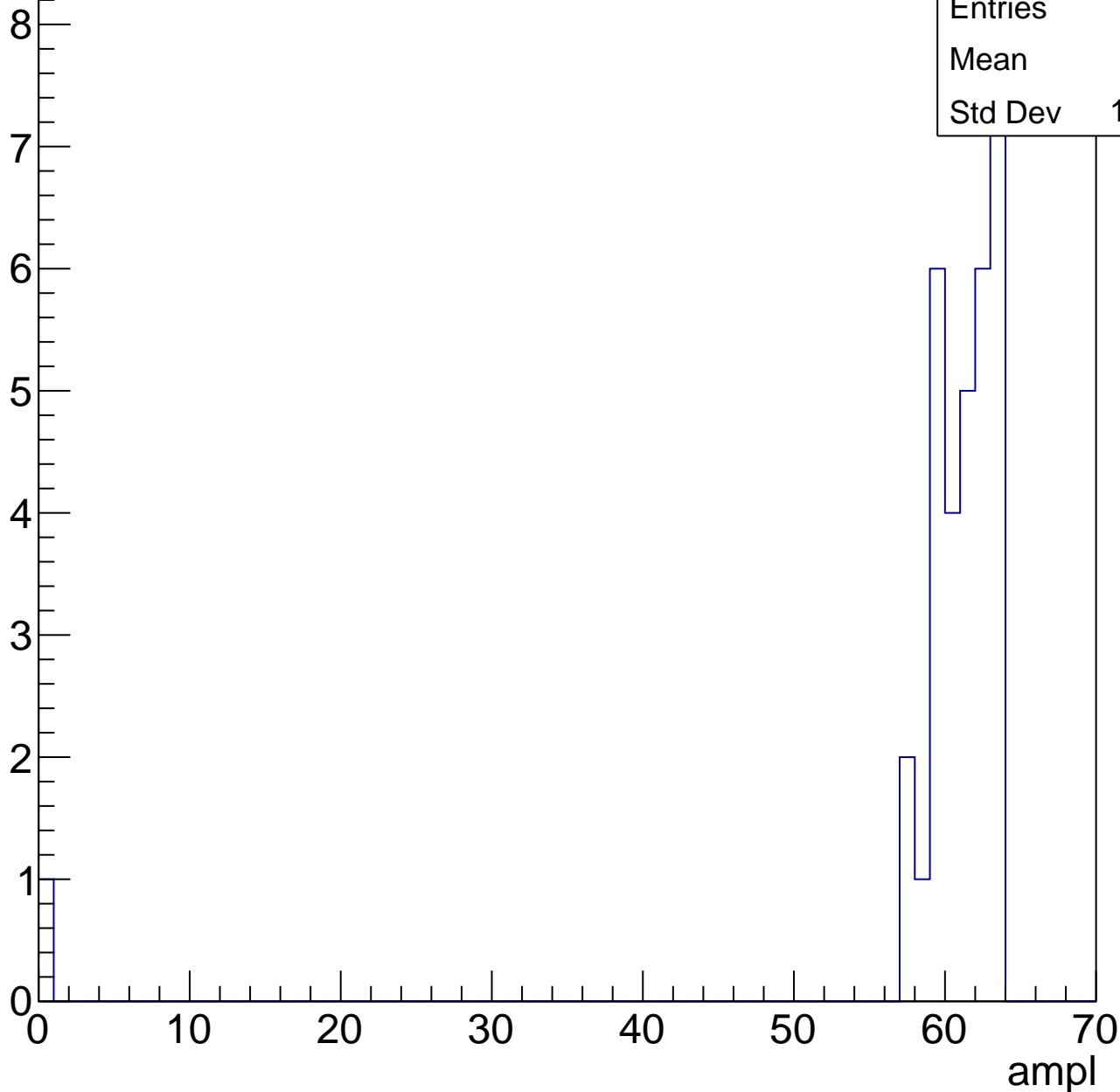


# B0L002S, U2-ch114, adc5

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	33
Mean	59
Std Dev	10.58



# B0L002S, U2-ch114, adc6

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry





# B0L002S, U2-ch114, adc7

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L002S, U2-ch115, adc0

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entries	85
Mean	31.58
Std Dev	4.95

**Gaus mean : 32.5484**

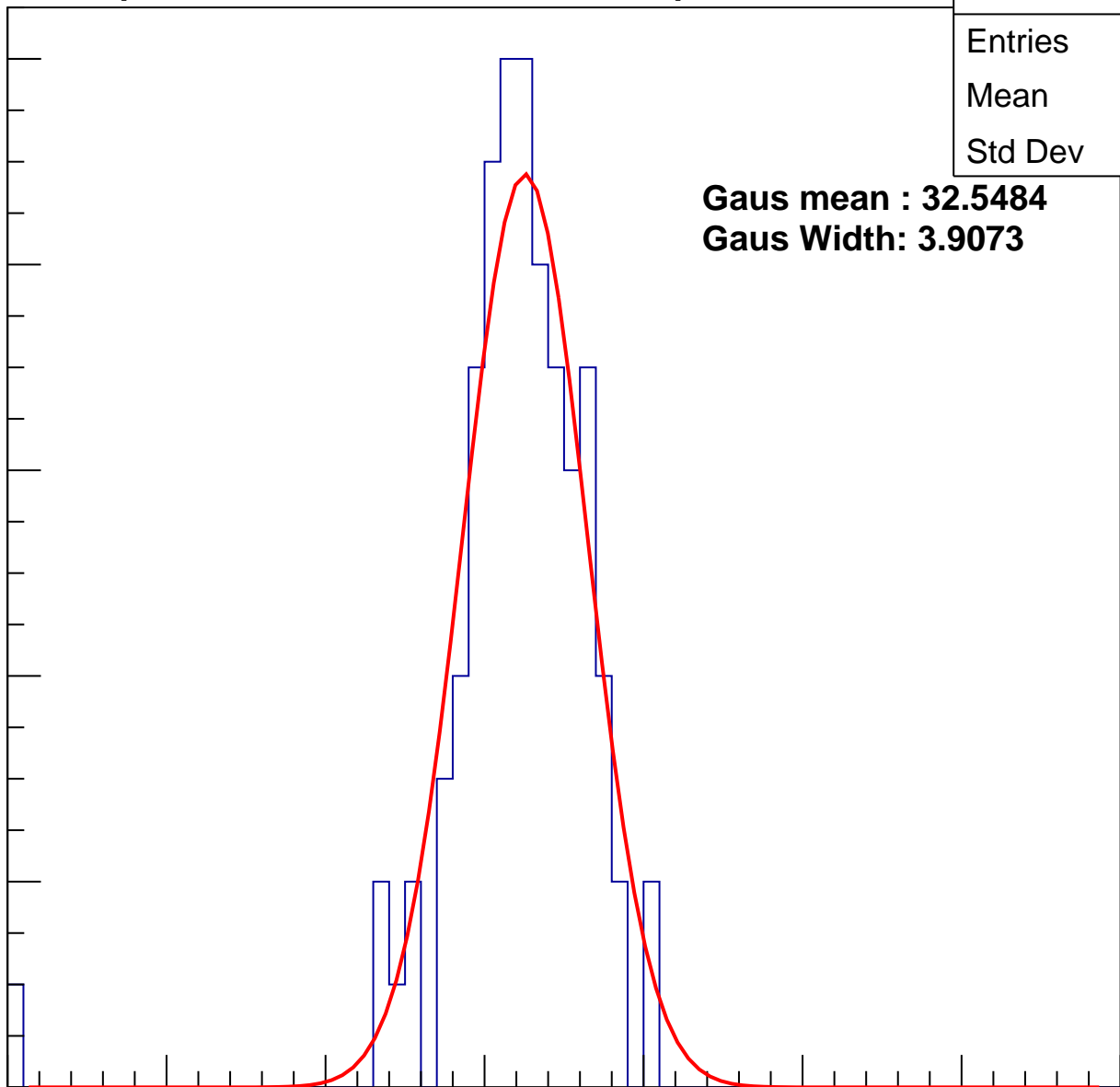
**Gaus Width: 3.9073**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L002S, U2-ch115, adc1

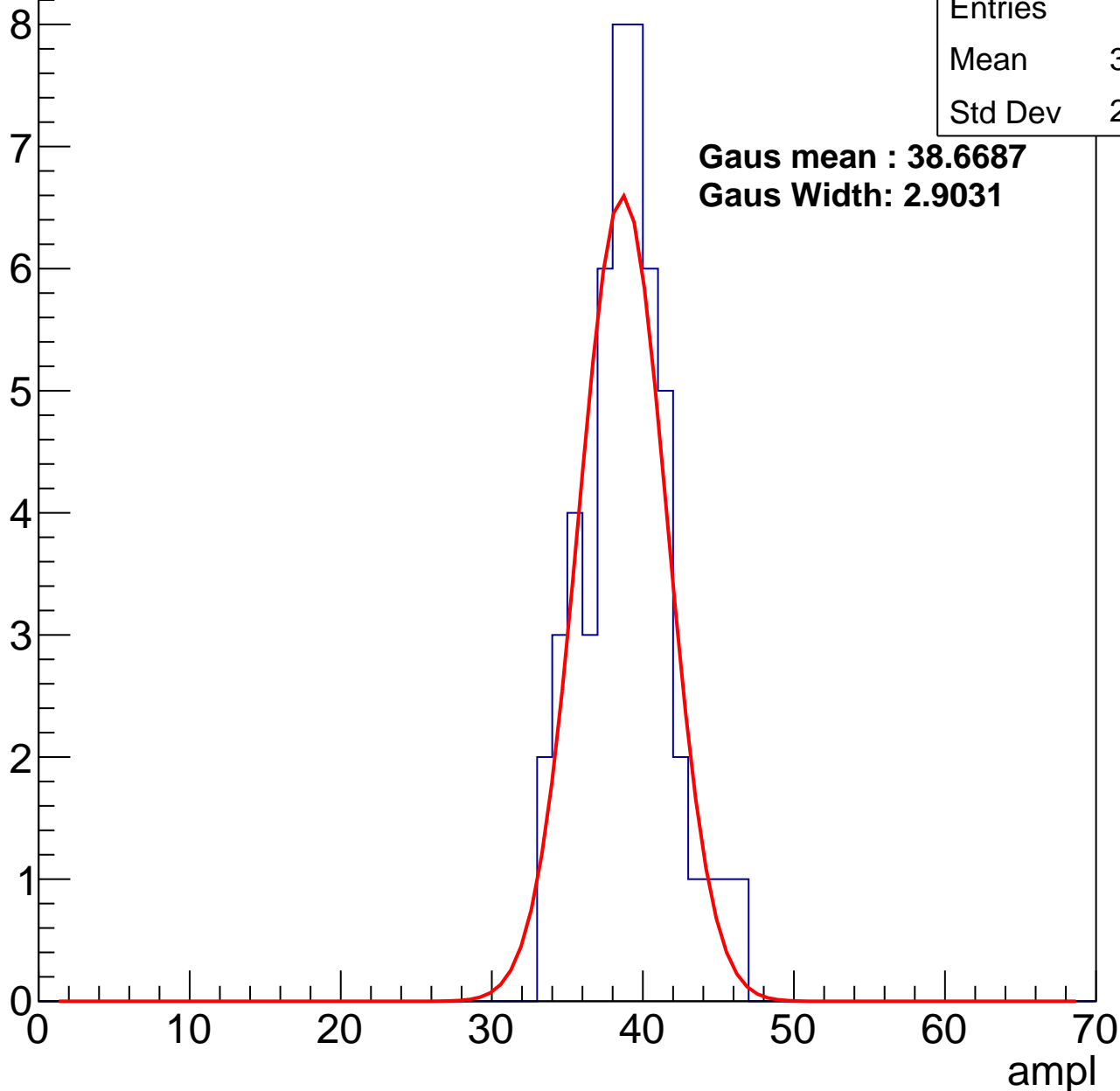
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	51
Mean	38.45
Std Dev	2.885

**Gaus mean : 38.6687**

**Gaus Width: 2.9031**



# B0L002S, U2-ch115, adc2

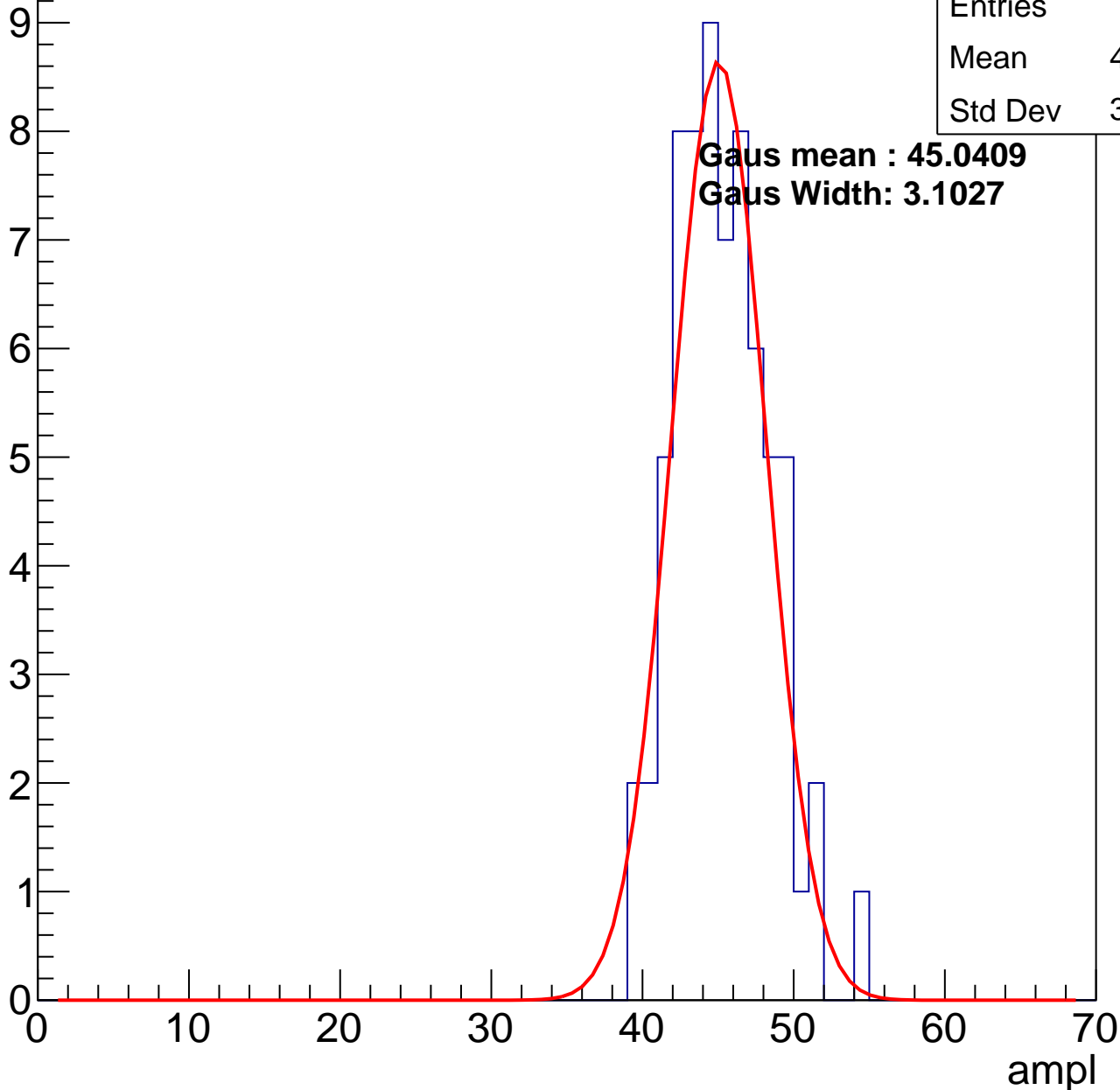
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	69
Mean	44.86
Std Dev	3.066

**Gaus mean : 45.0409**

**Gaus Width: 3.1027**

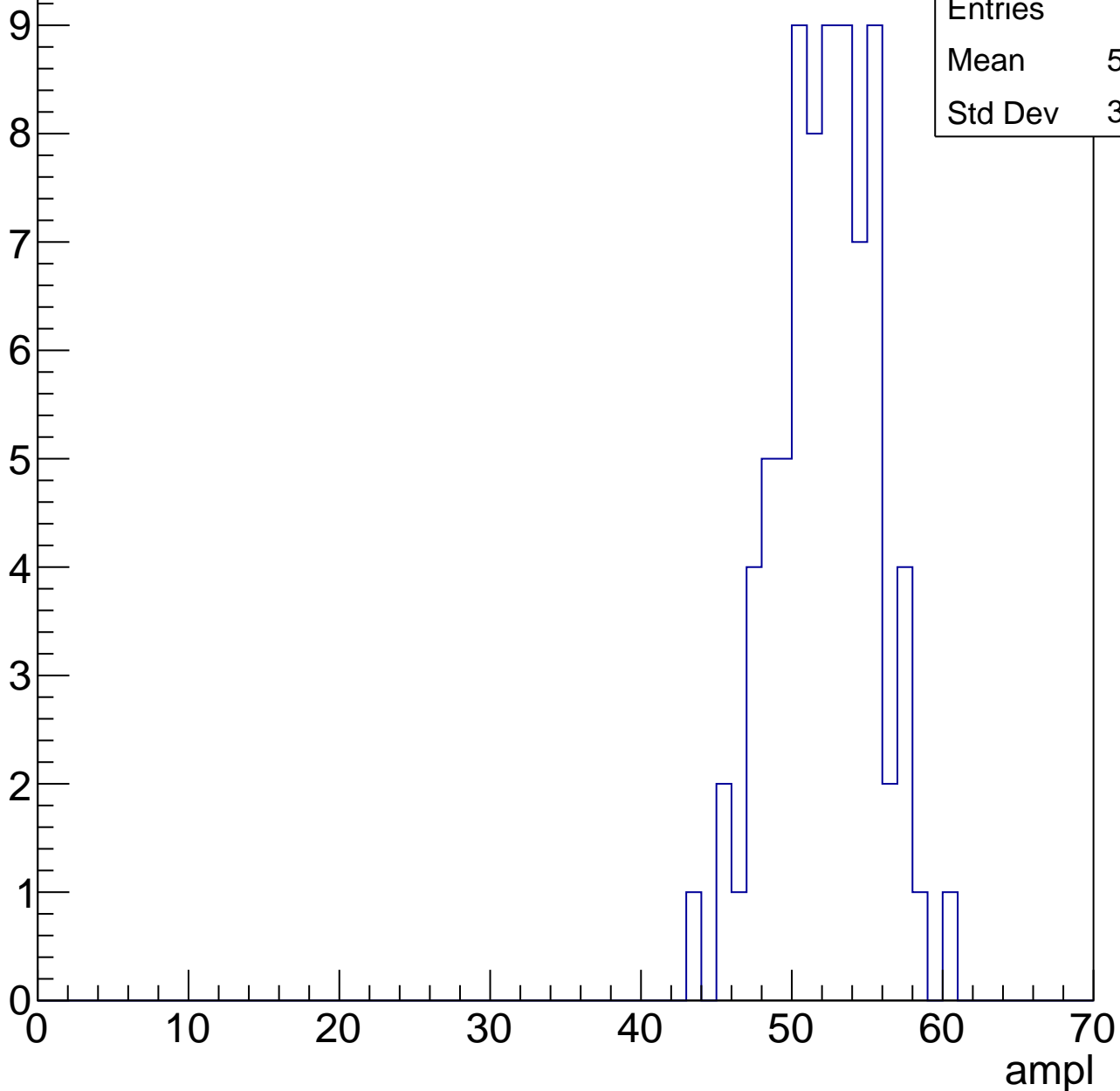


# B0L002S, U2-ch115, adc3

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

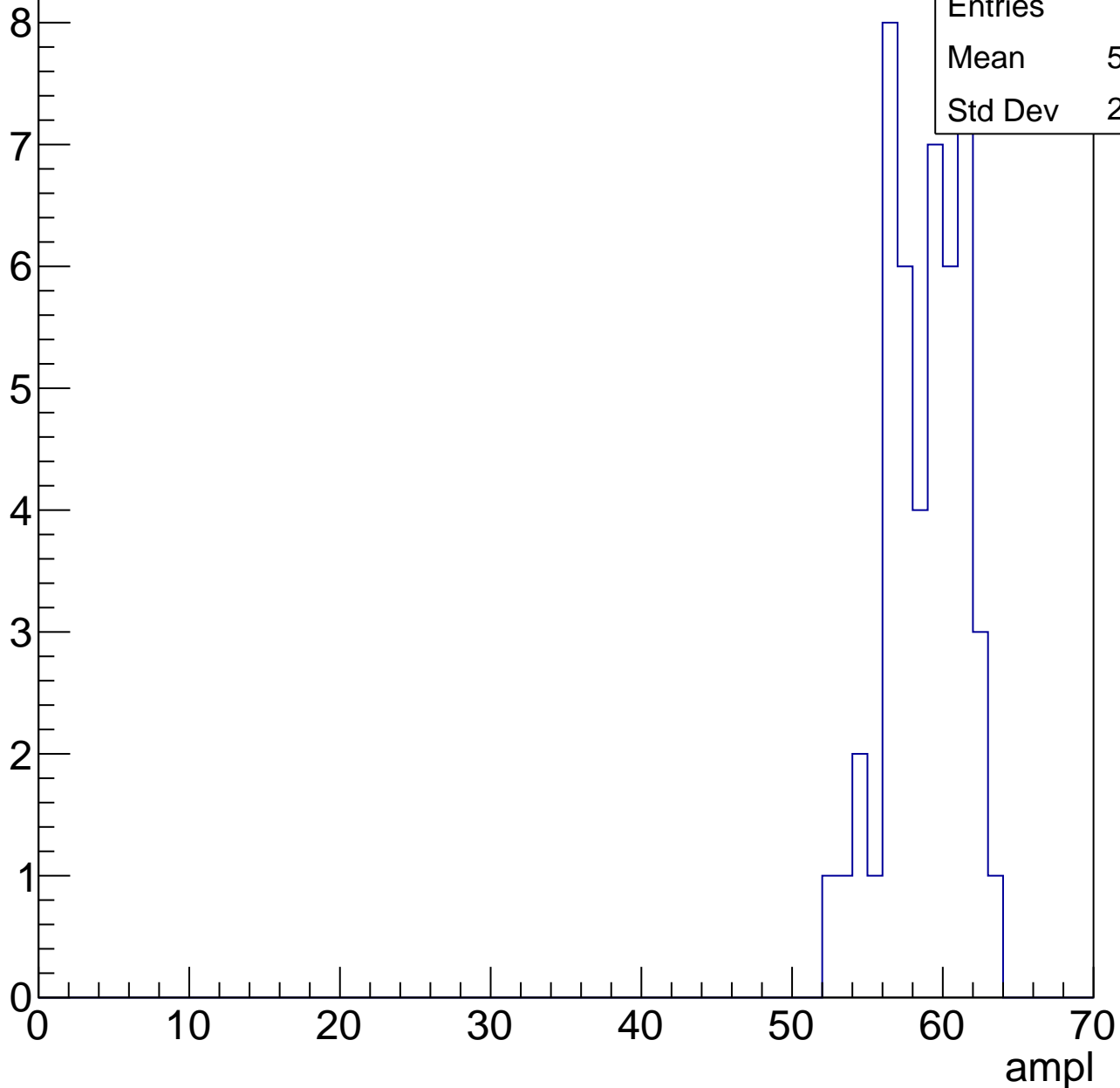
Entries	77
Mean	51.77
Std Dev	3.283



# B0L002S, U2-ch115, adc4

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

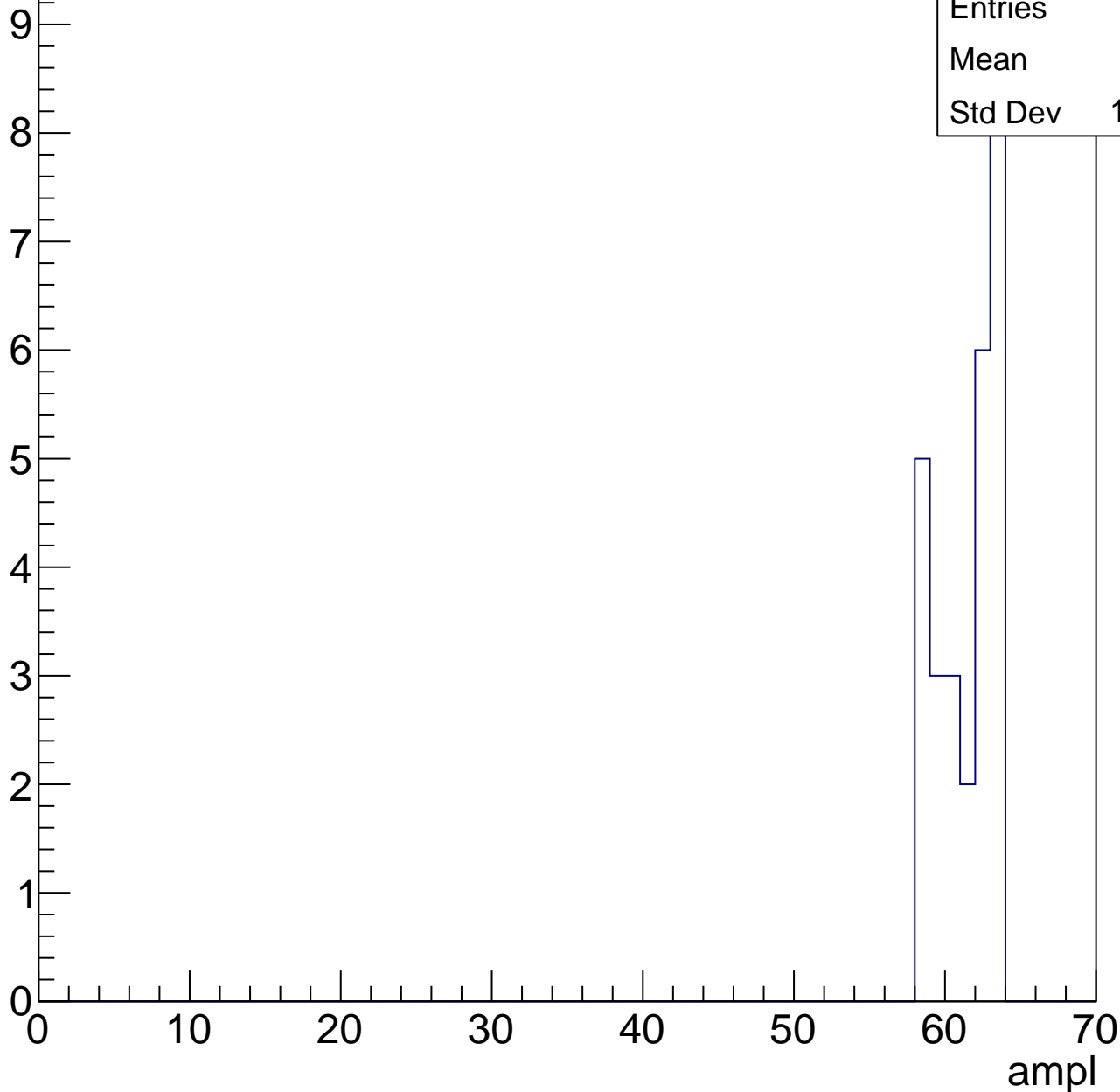


# B0L002S, U2-ch115, adc5

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

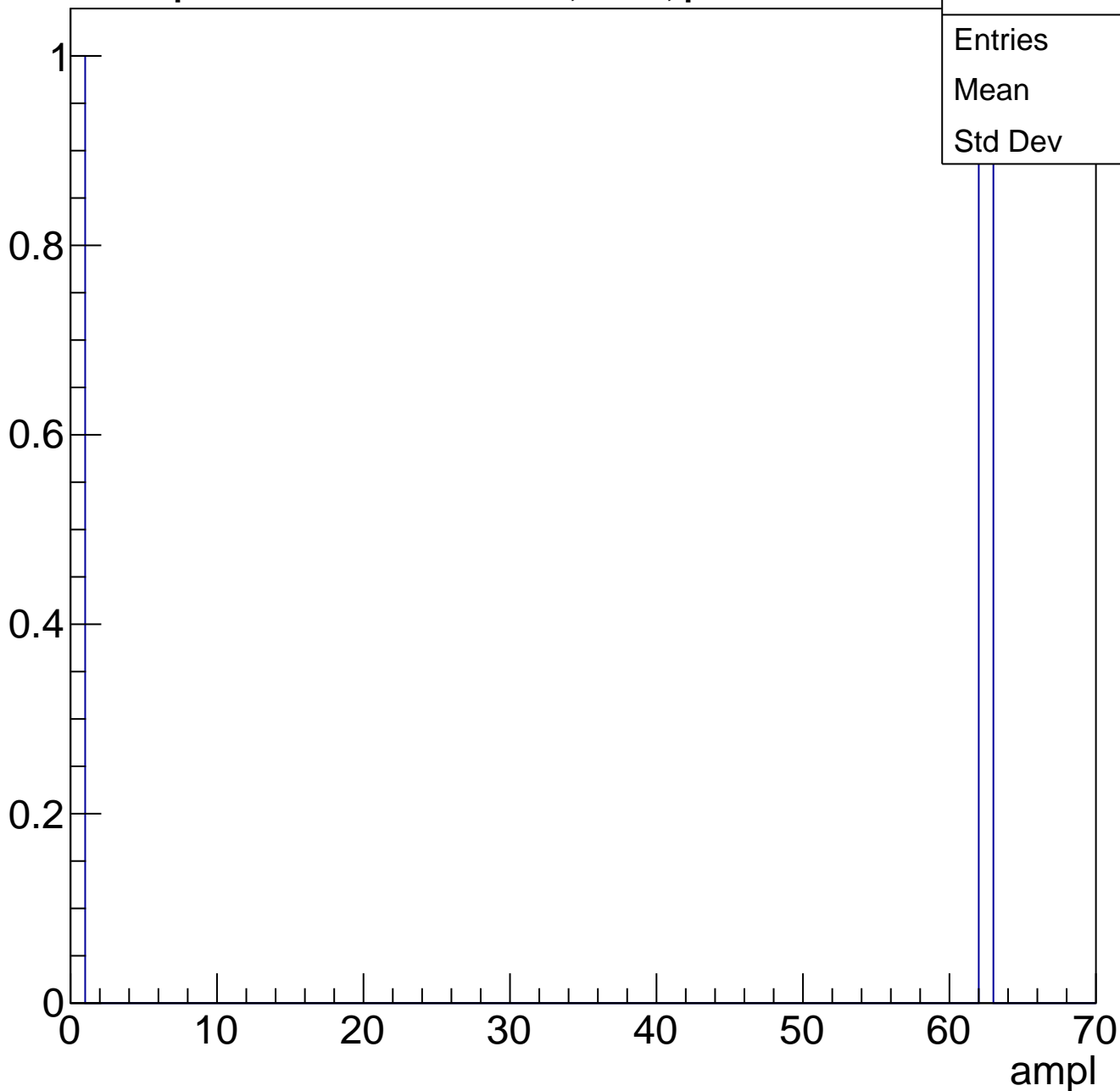
Entries	28
Mean	61
Std Dev	1.909



# B0L002S, U2-ch115, adc6

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry





# B0L002S, U2-ch115, adc7

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



# B0L002S, U2-ch116, adc0

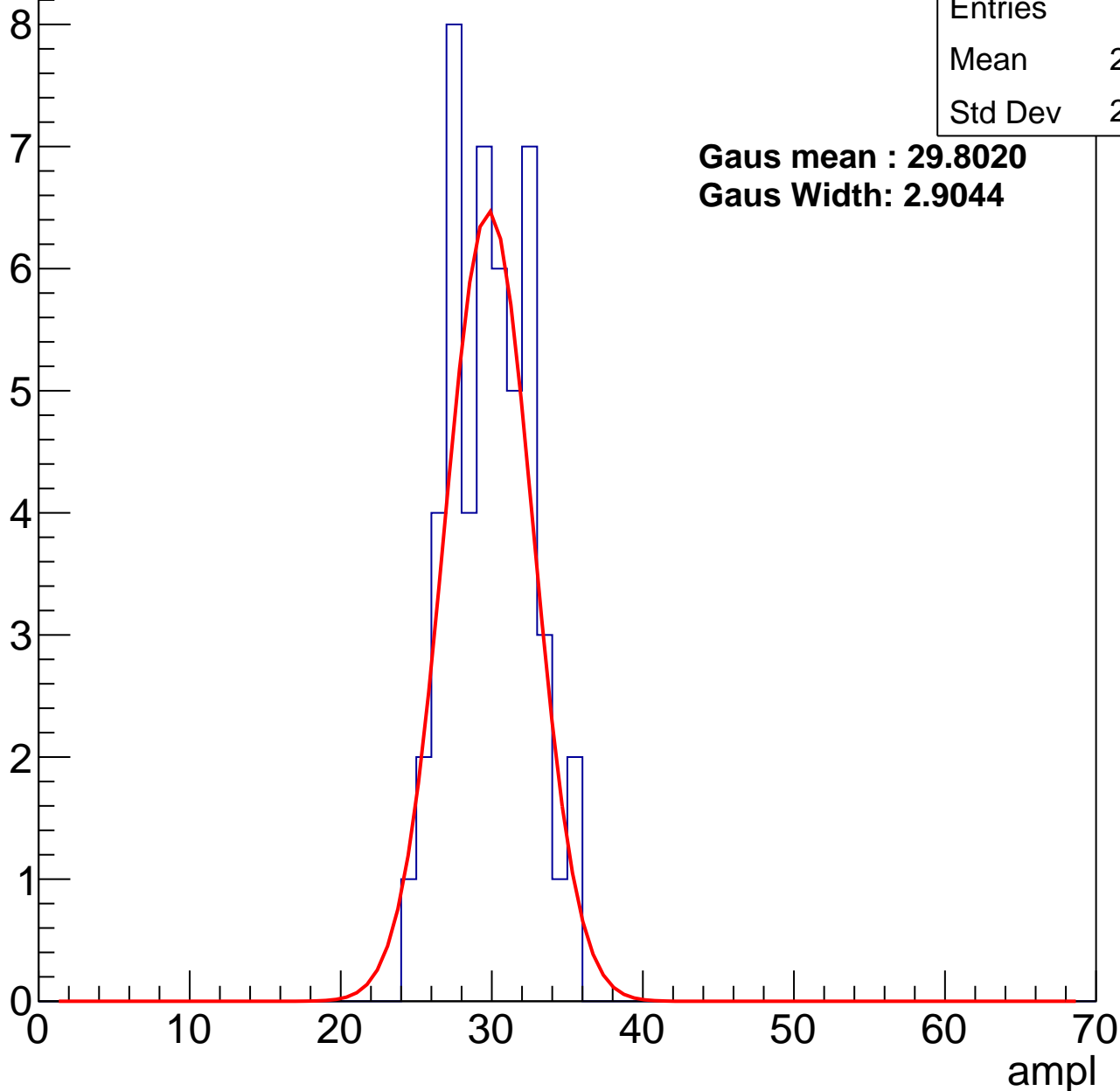
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	50
Mean	29.42
Std Dev	2.662

**Gaus mean : 29.8020**

**Gaus Width: 2.9044**

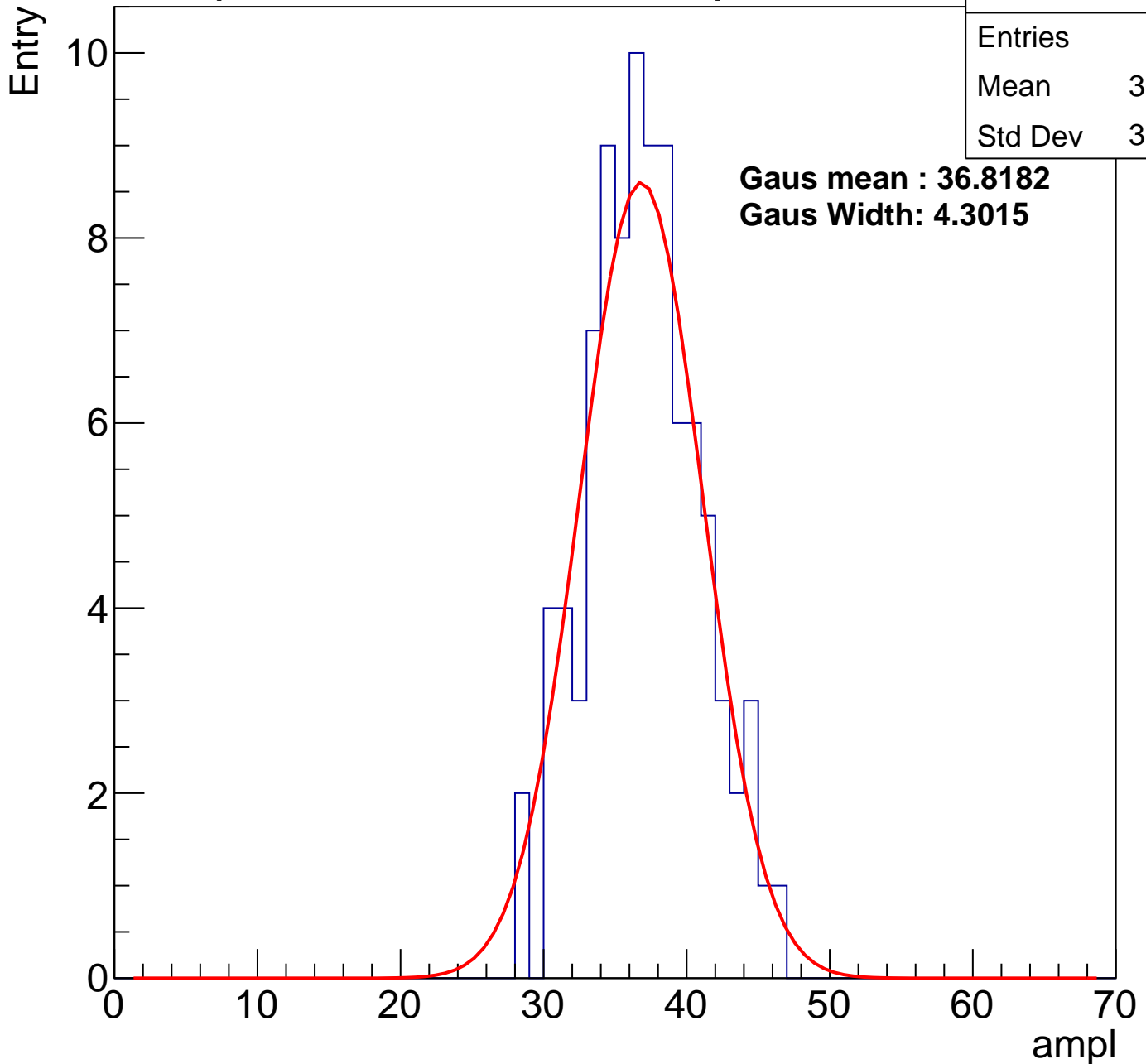


# B0L002S, U2-ch116, adc1

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entries	92
Mean	36.54
Std Dev	3.899

**Gaus mean : 36.8182**  
**Gaus Width: 4.3015**



# B0L002S, U2-ch116, adc2

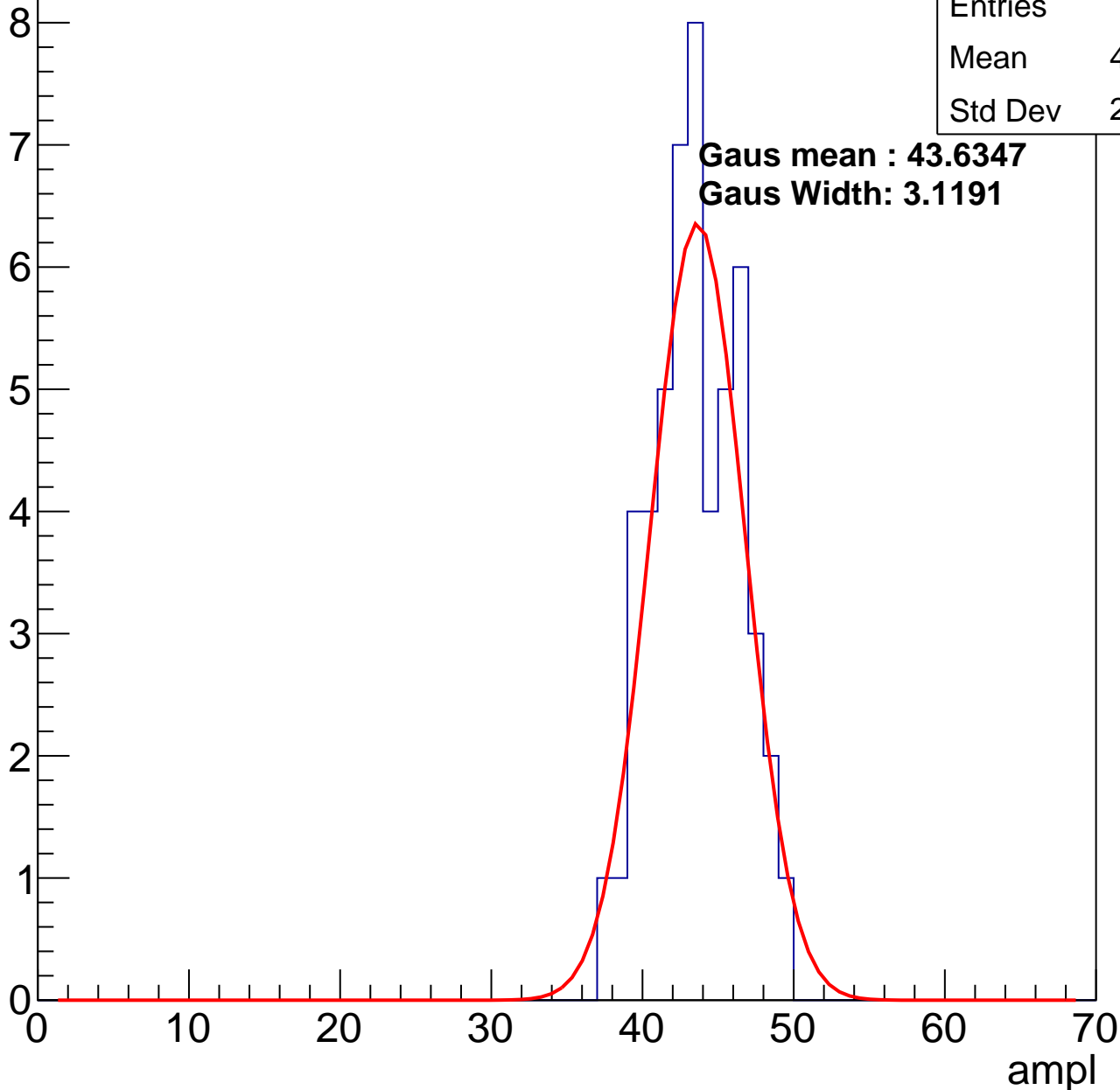
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	51
Mean	43.08
Std Dev	2.799

**Gaus mean : 43.6347**

**Gaus Width: 3.1191**

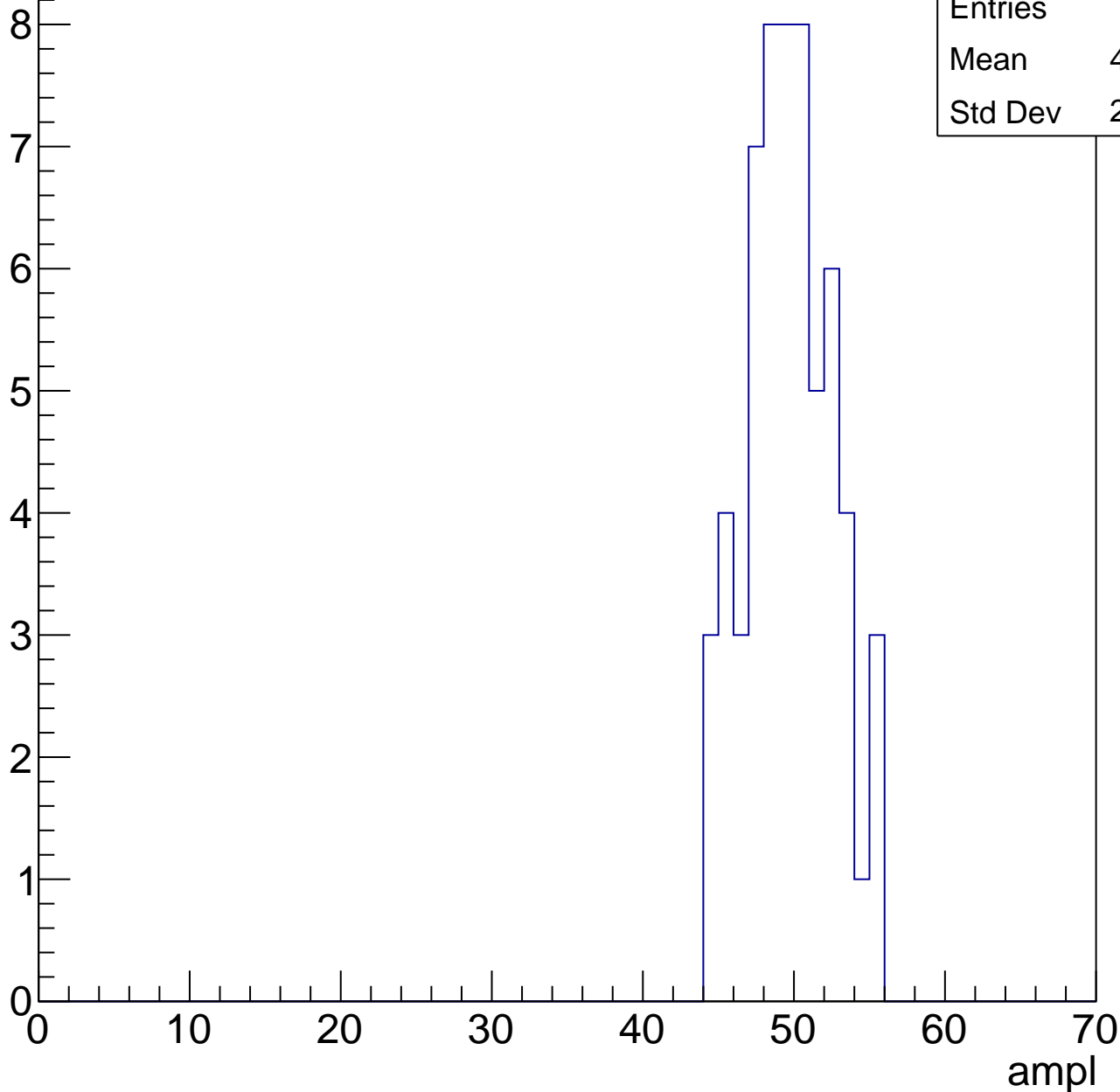


# B0L002S, U2-ch116, adc3

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	60
Mean	49.22
Std Dev	2.823

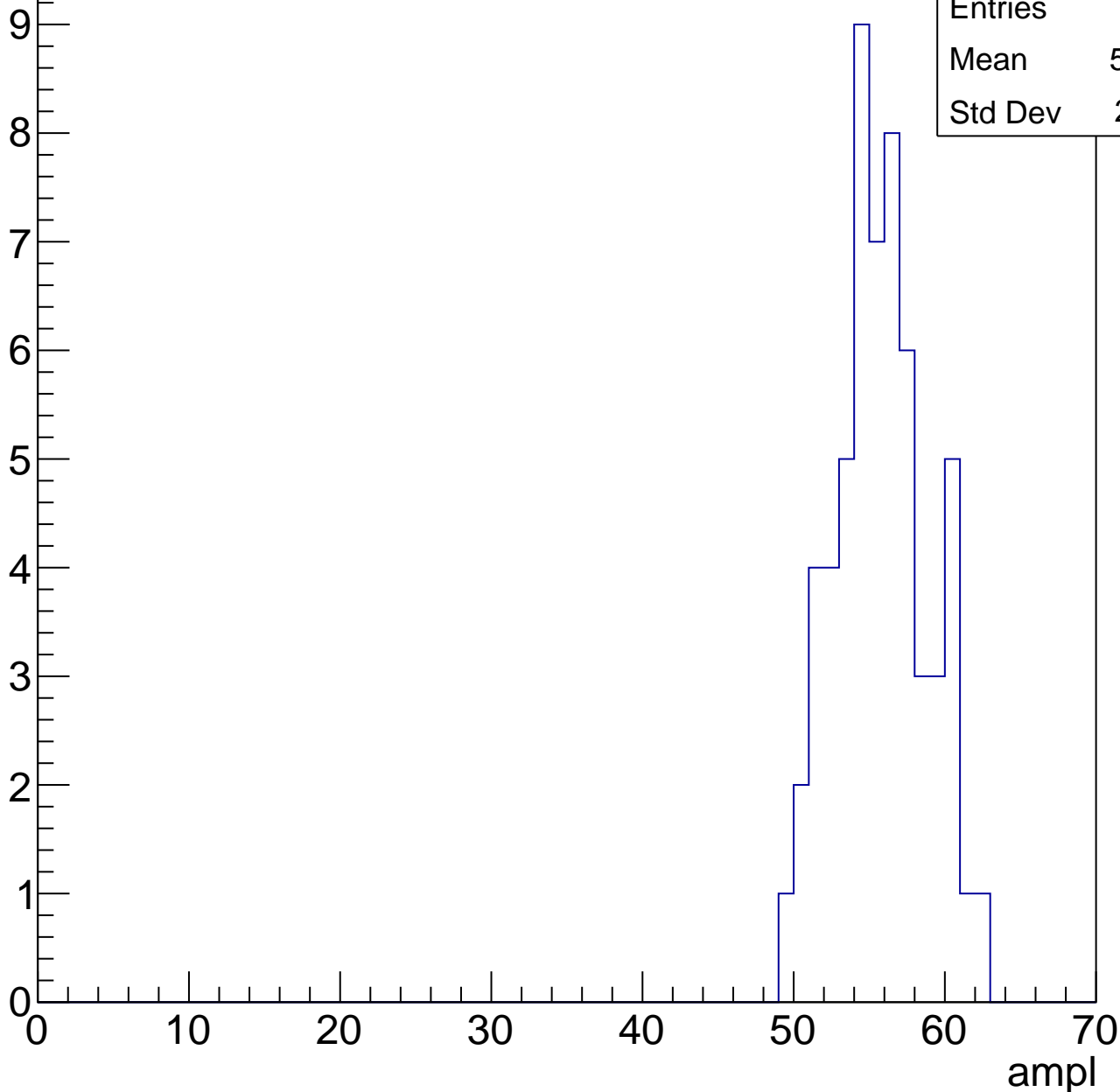


# B0L002S, U2-ch116, adc4

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	59
Mean	55.27
Std Dev	2.991

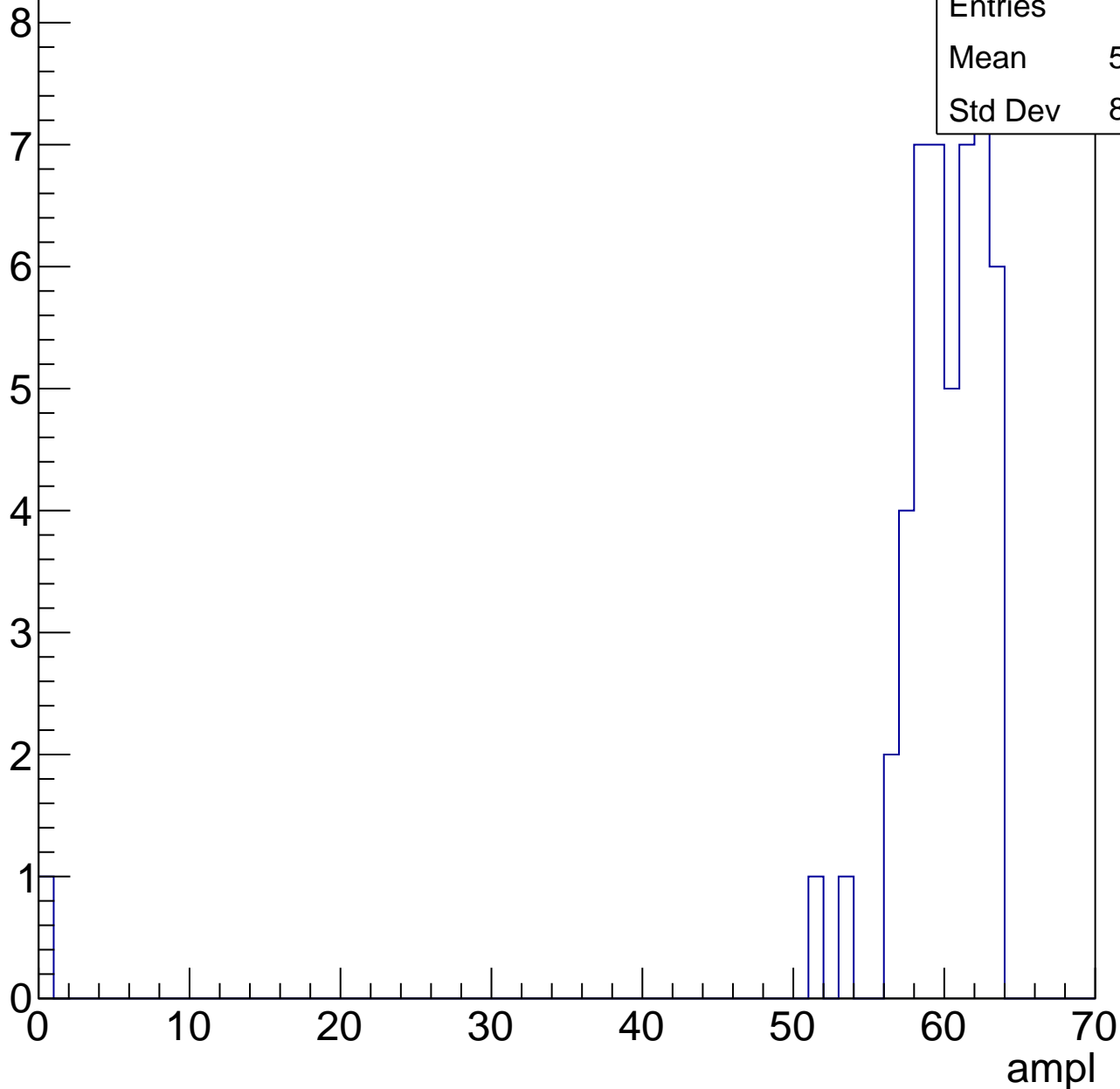


# B0L002S, U2-ch116, adc5

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

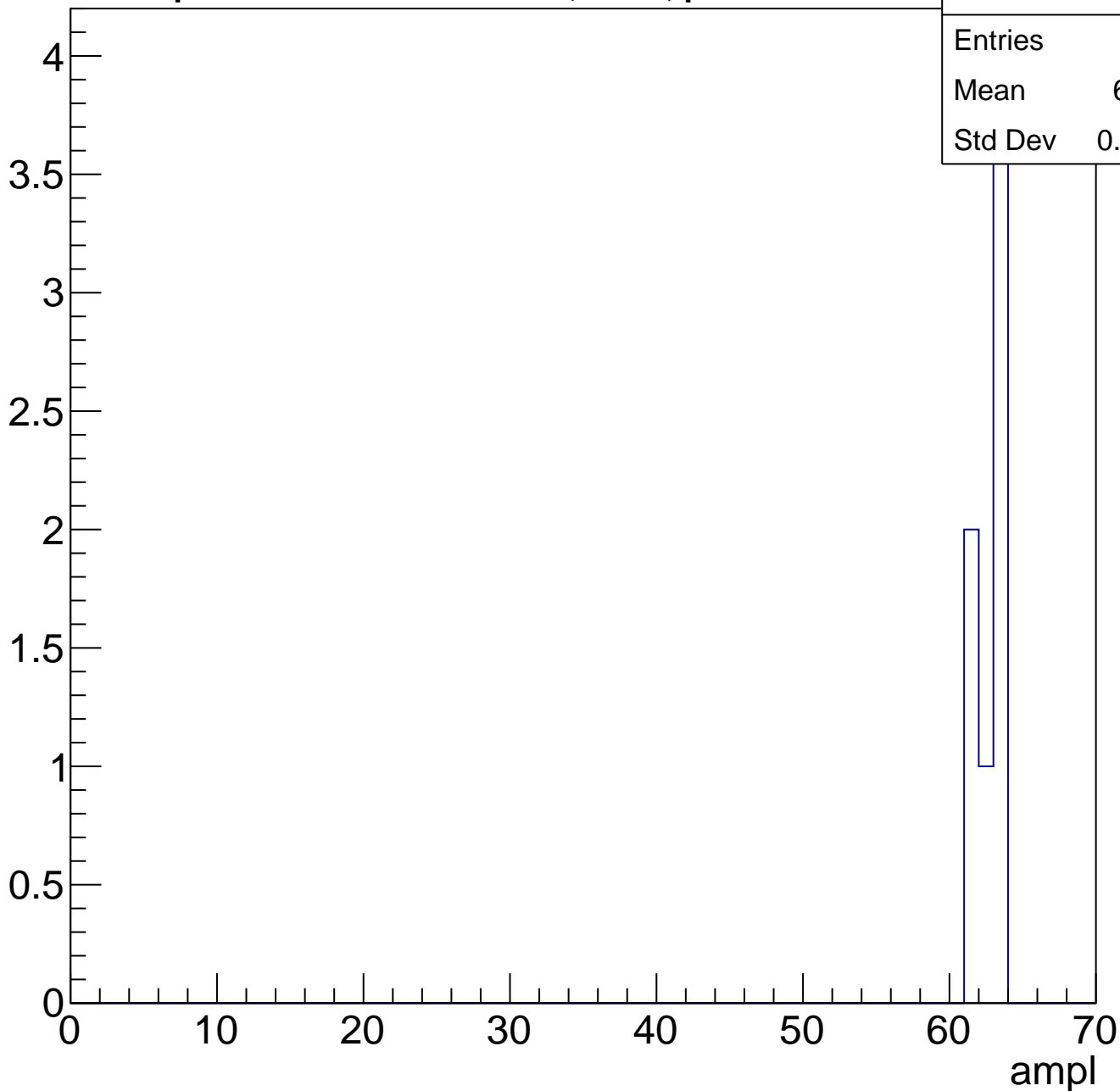
Entries	49
Mean	58.45
Std Dev	8.816



# B0L002S, U2-ch116, adc6

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry





# B0L002S, U2-ch116, adc7

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



Entries	2
Mean	0
Std Dev	0

# B0L002S, U2-ch117, adc0

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entries	91
Mean	31.88
Std Dev	5.027

**Gaus mean : 32.7316**

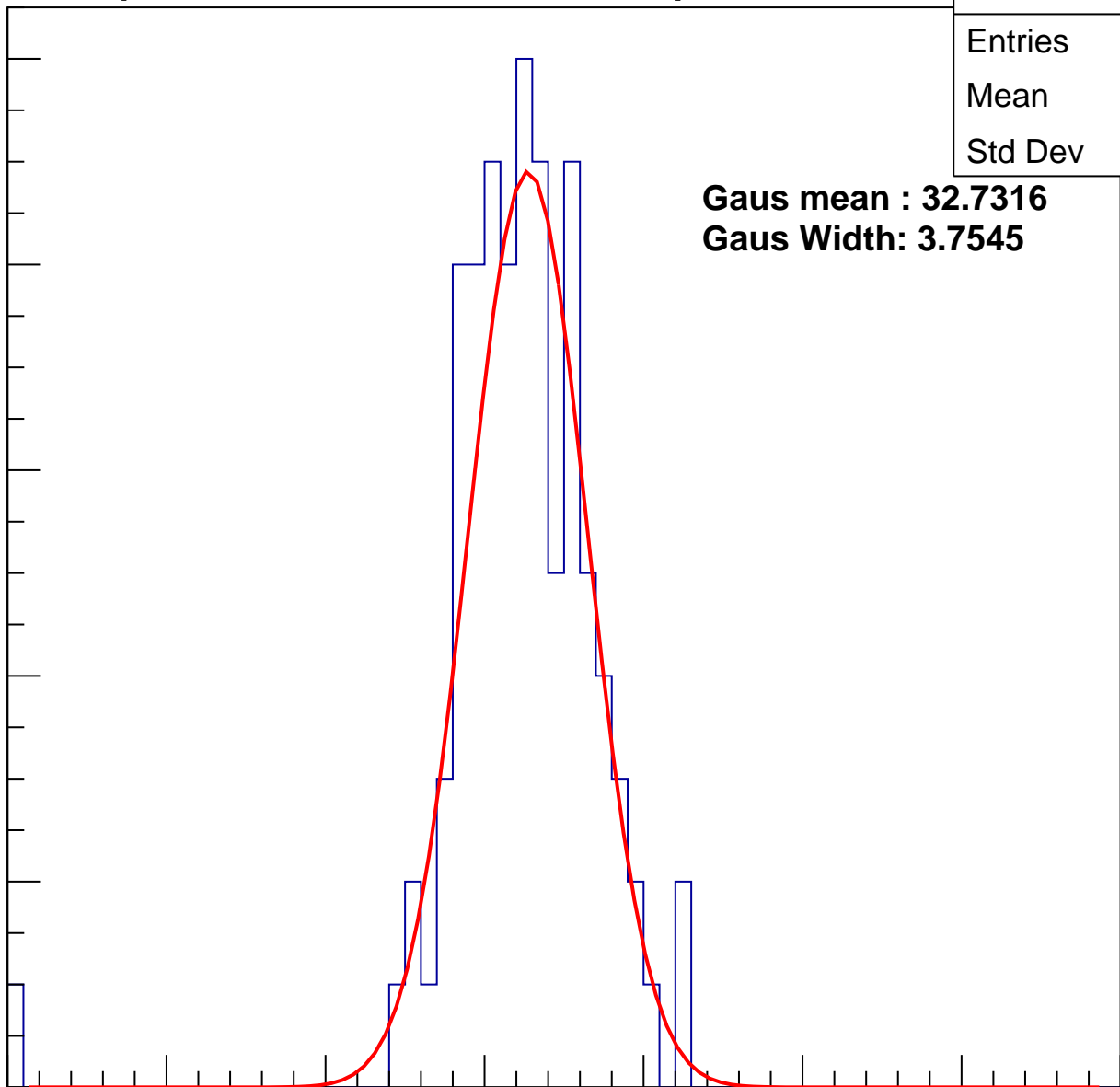
**Gaus Width: 3.7545**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L002S, U2-ch117, adc1

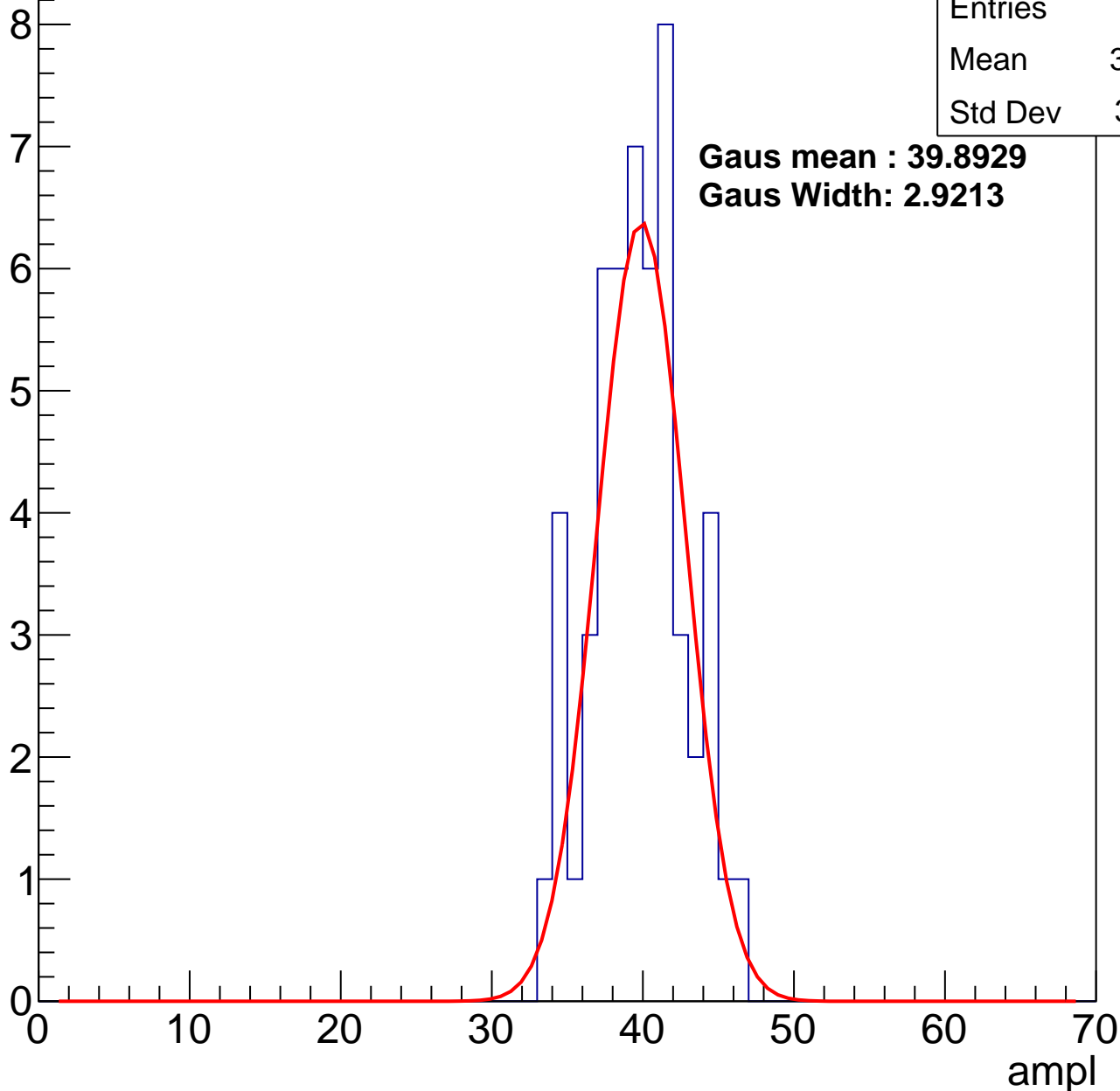
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	53
Mean	39.28
Std Dev	3.031

**Gaus mean : 39.8929**

**Gaus Width: 2.9213**



# B0L002S, U2-ch117, adc2

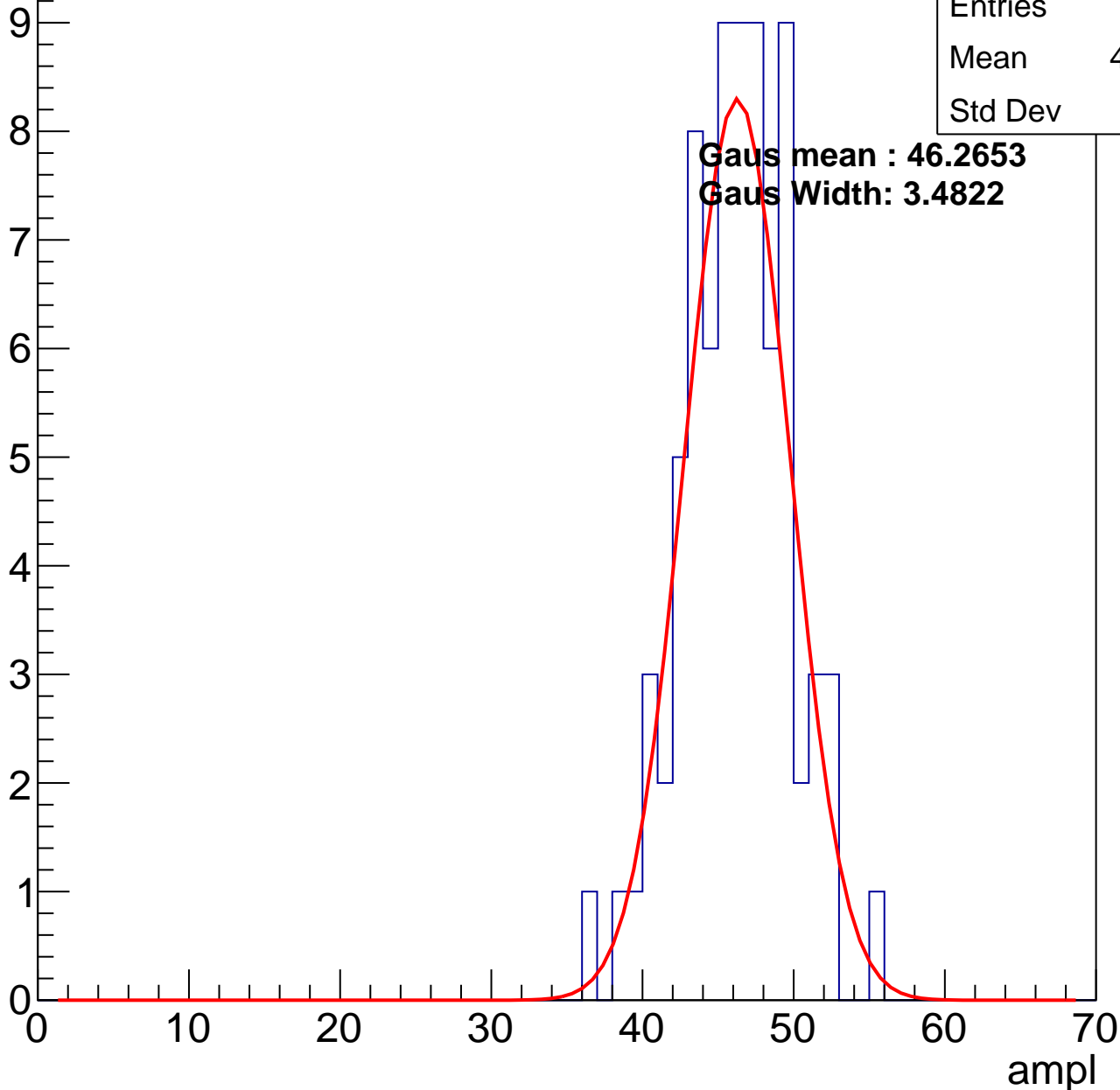
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	78
Mean	45.74
Std Dev	3.51

**Gaus mean : 46.2653**

**Gaus Width: 3.4822**

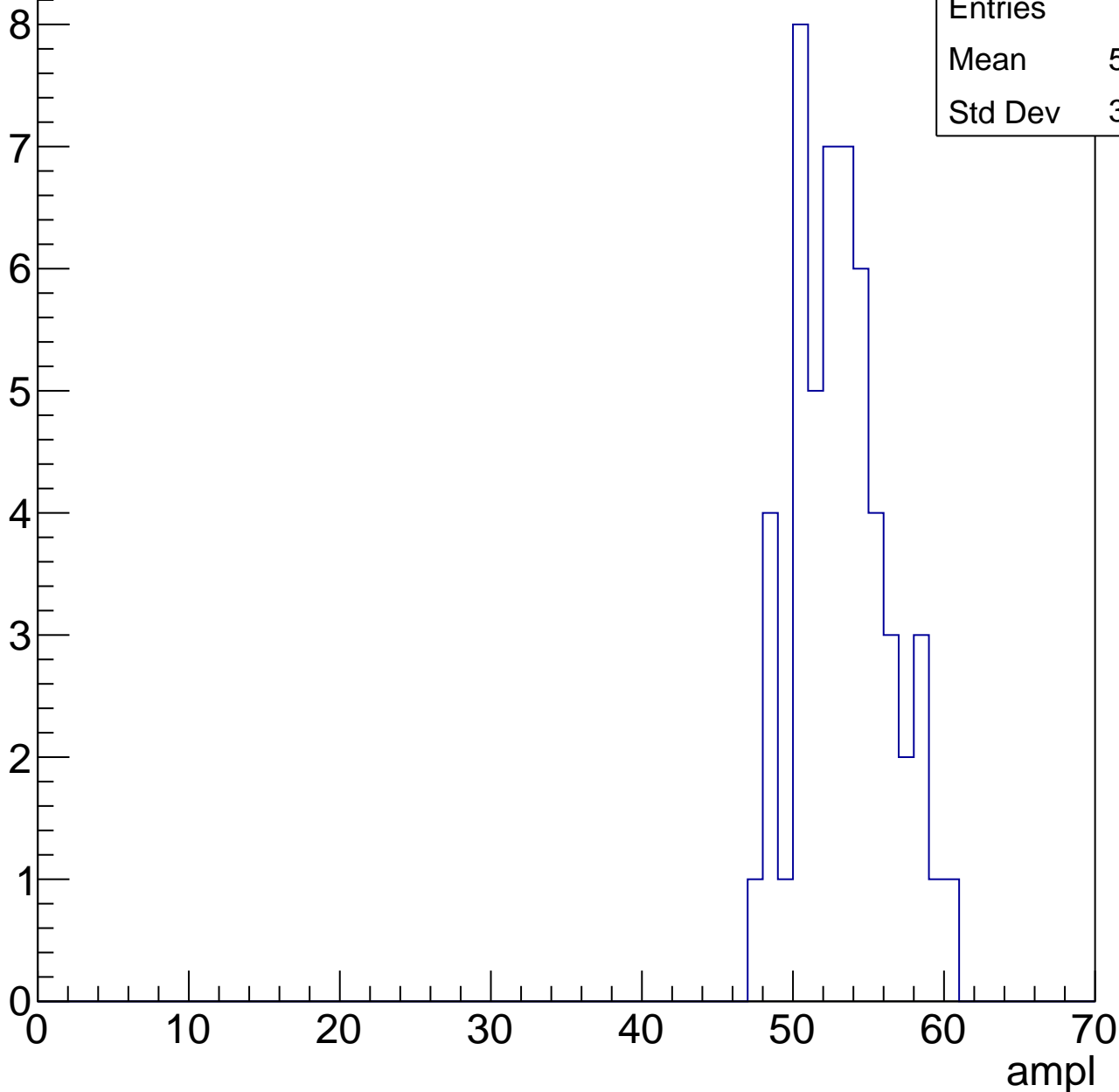


# B0L002S, U2-ch117, adc3

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	53
Mean	52.77
Std Dev	3.038

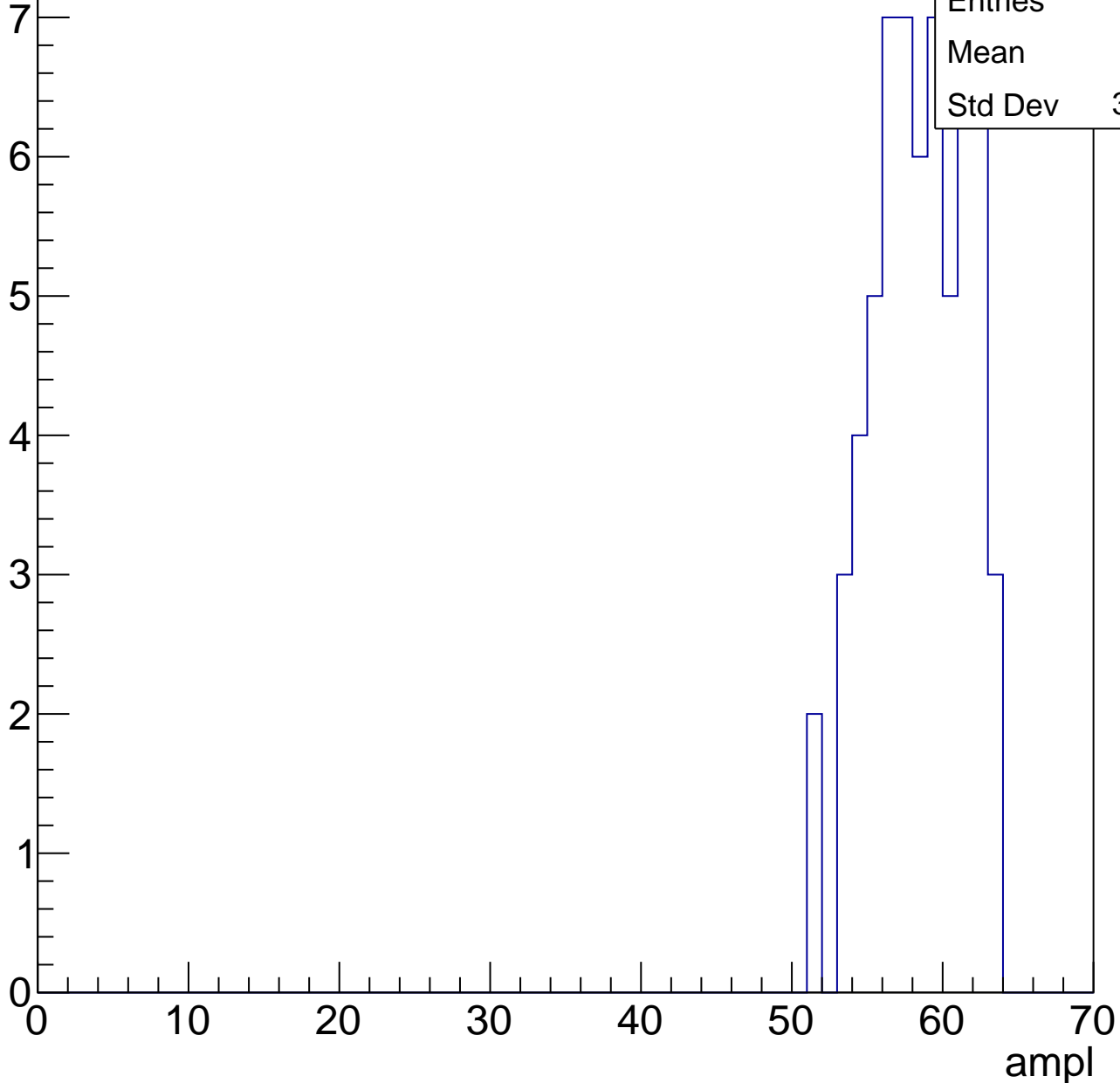


# B0L002S, U2-ch117, adc4

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	63
Mean	58
Std Dev	3.071

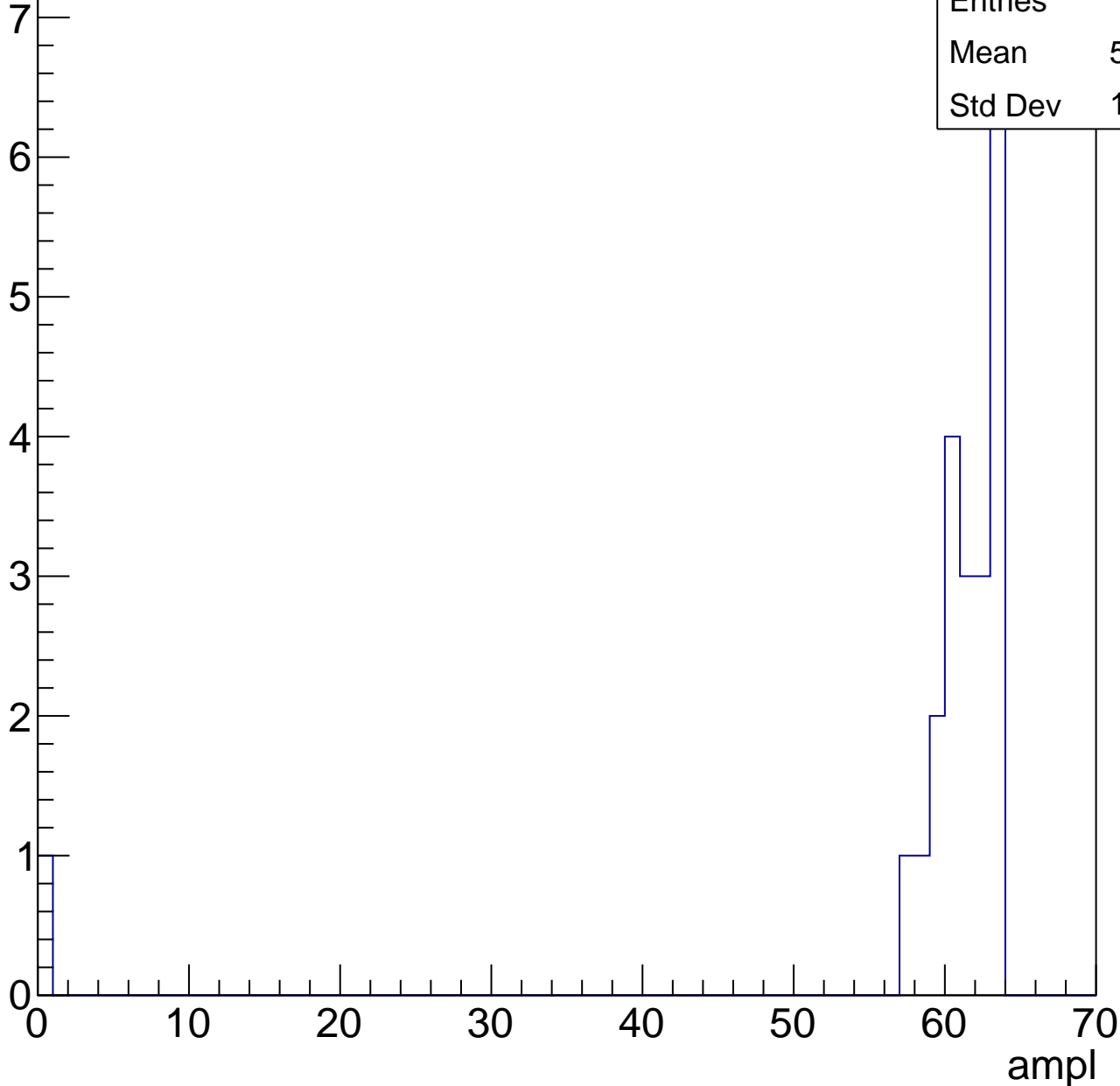


# B0L002S, U2-ch117, adc5

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	22
Mean	58.32
Std Dev	12.85



# B0L002S, U2-ch117, adc6

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



Entries	0
Mean	0
Std Dev	0



# B0L002S, U2-ch117, adc7

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L002S, U2-ch118, adc0

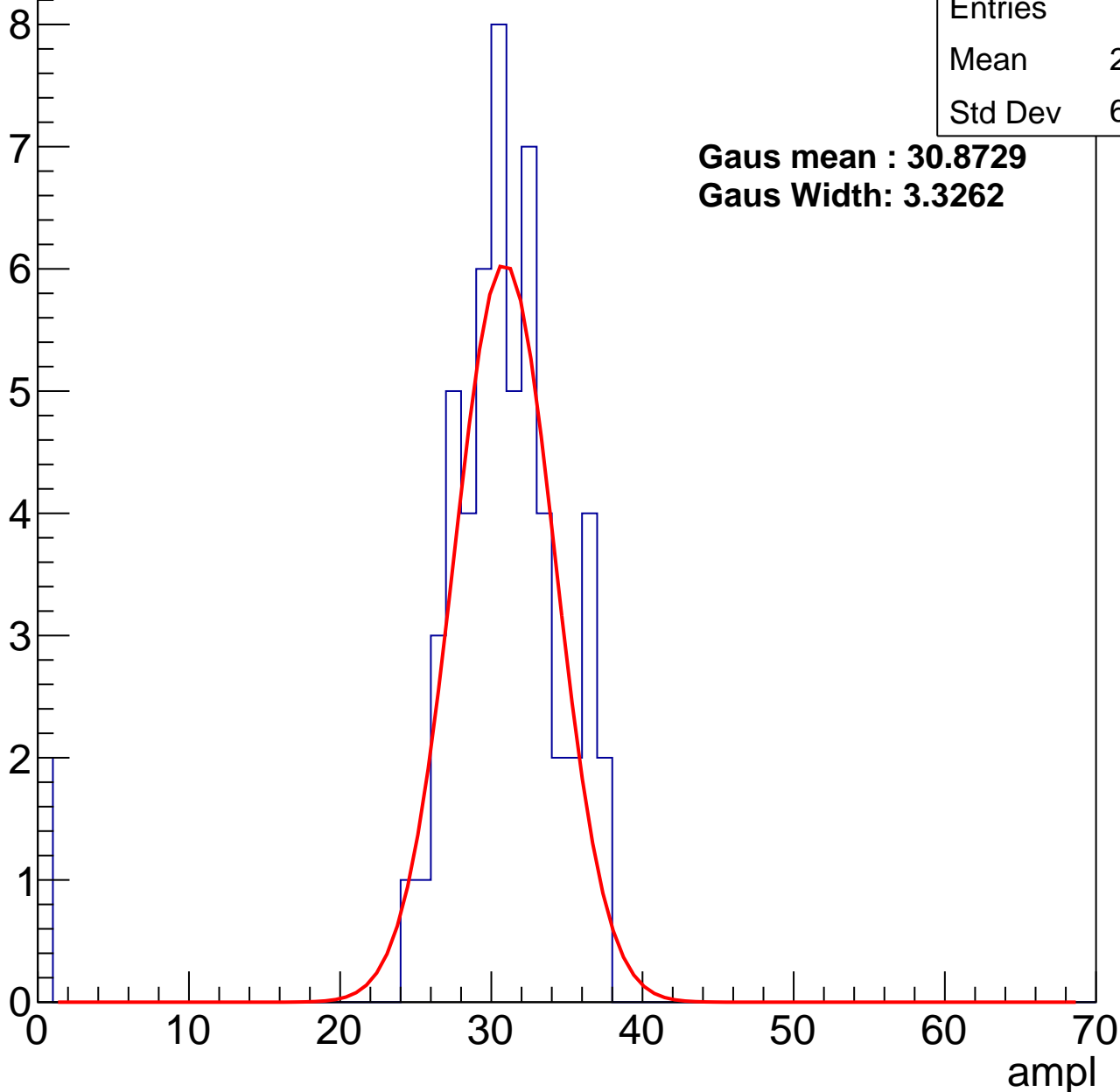
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	56
Mean	29.55
Std Dev	6.489

**Gaus mean : 30.8729**

**Gaus Width: 3.3262**



# B0L002S, U2-ch118, adc1

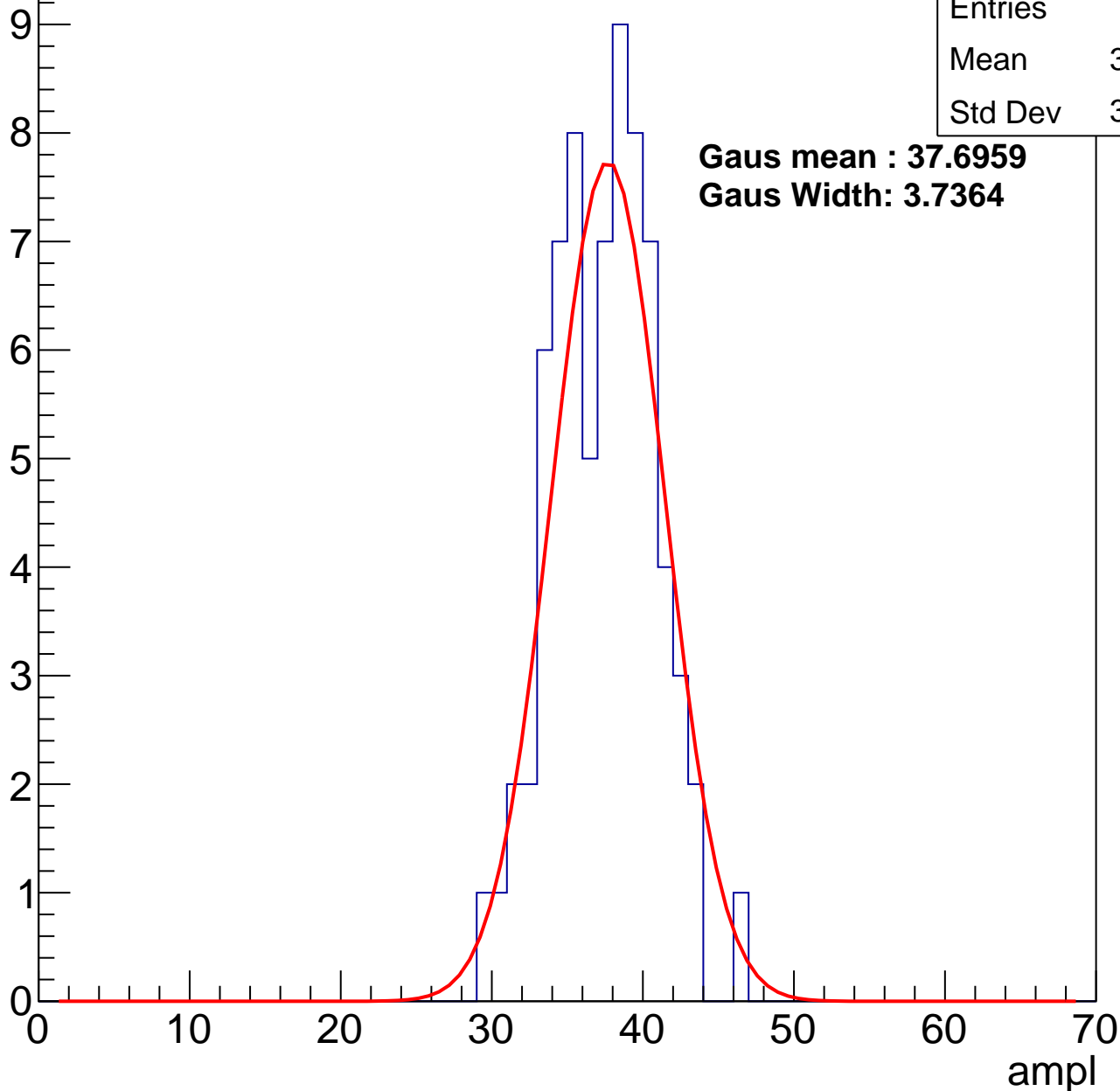
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	73
Mean	36.93
Std Dev	3.365

**Gaus mean : 37.6959**

**Gaus Width: 3.7364**



# B0L002S, U2-ch118, adc2

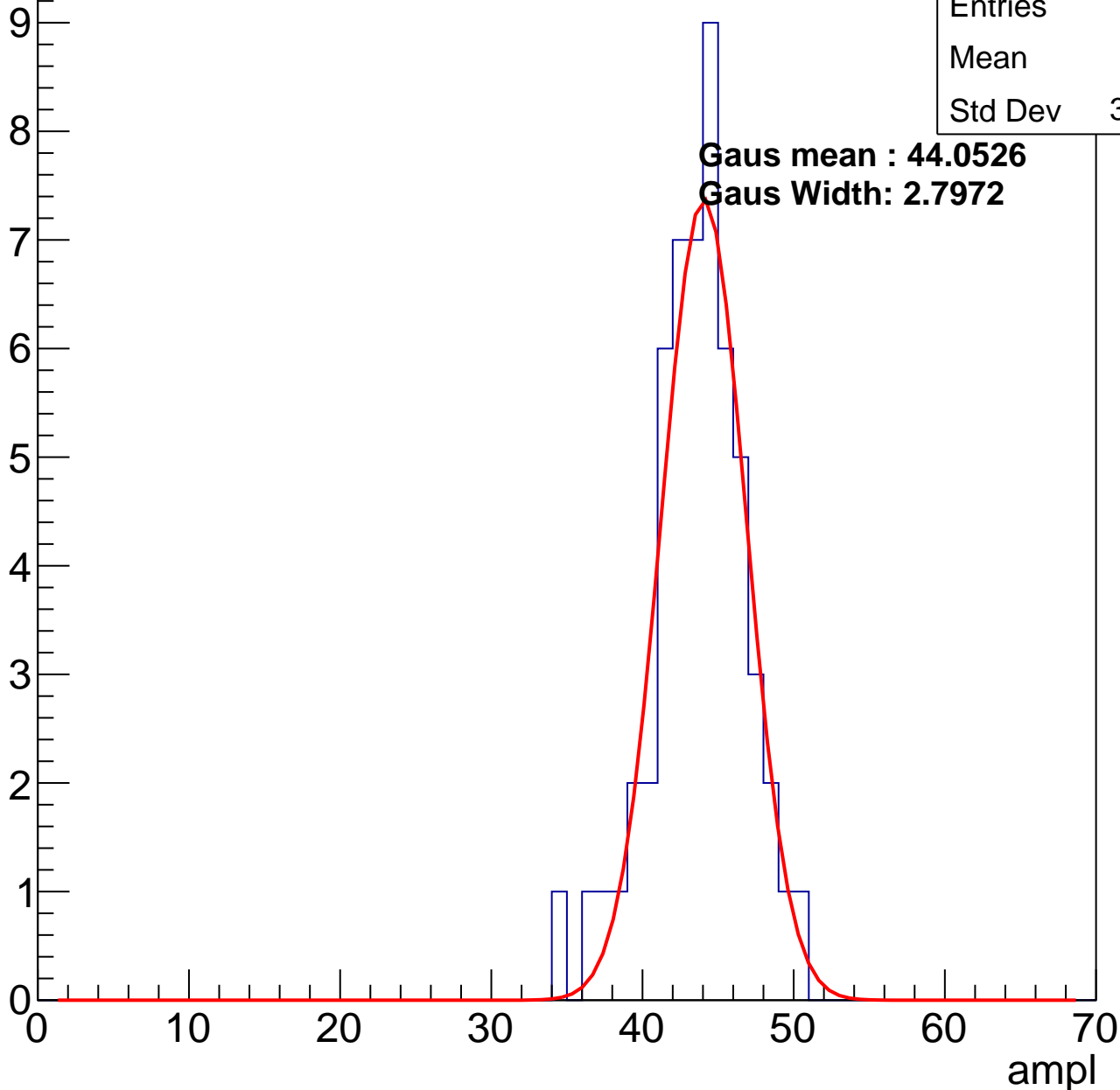
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	55
Mean	43.2
Std Dev	3.107

**Gaus mean : 44.0526**

**Gaus Width: 2.7972**

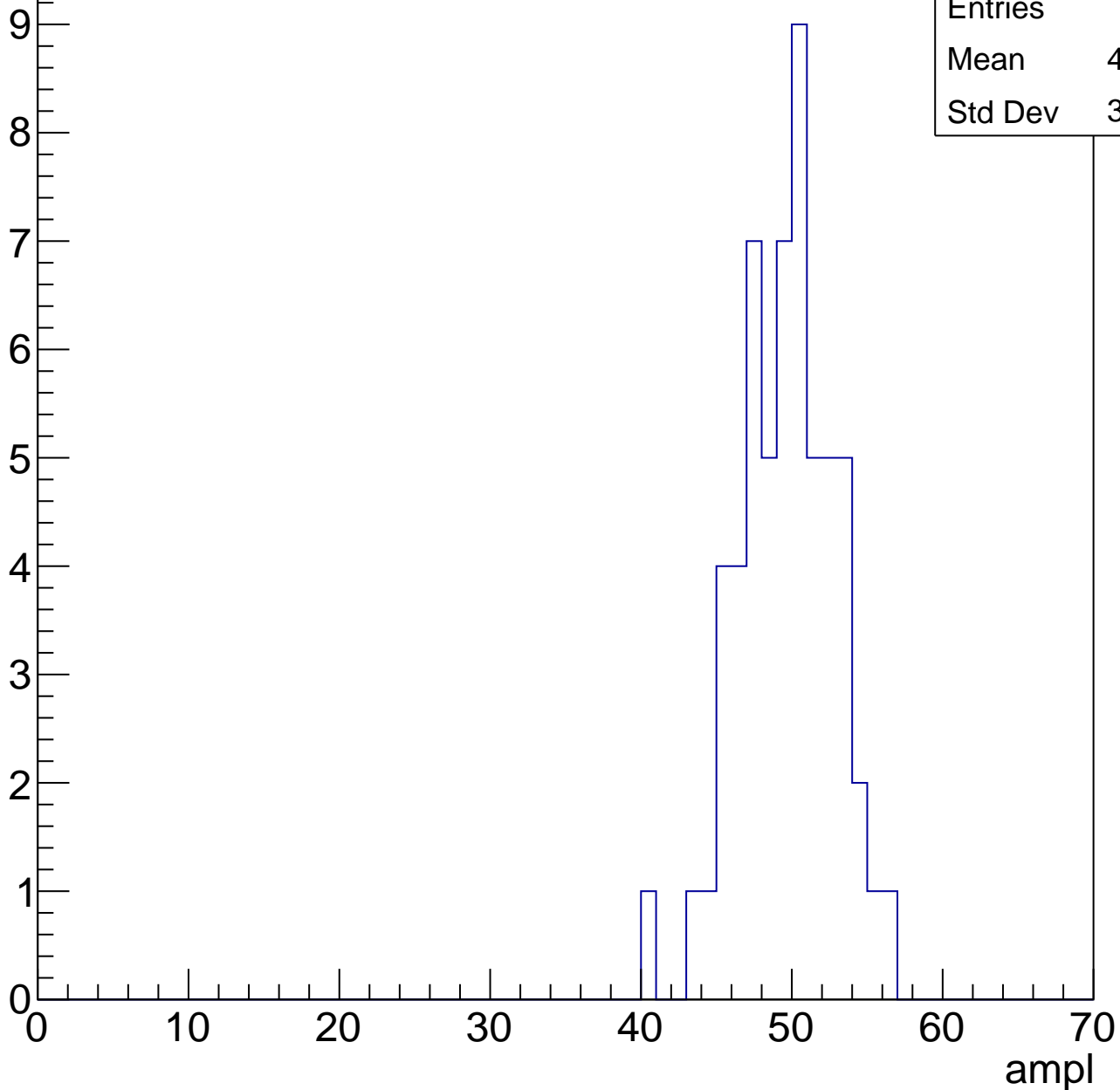


# B0L002S, U2-ch118, adc3

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	58
Mean	49.17
Std Dev	3.114

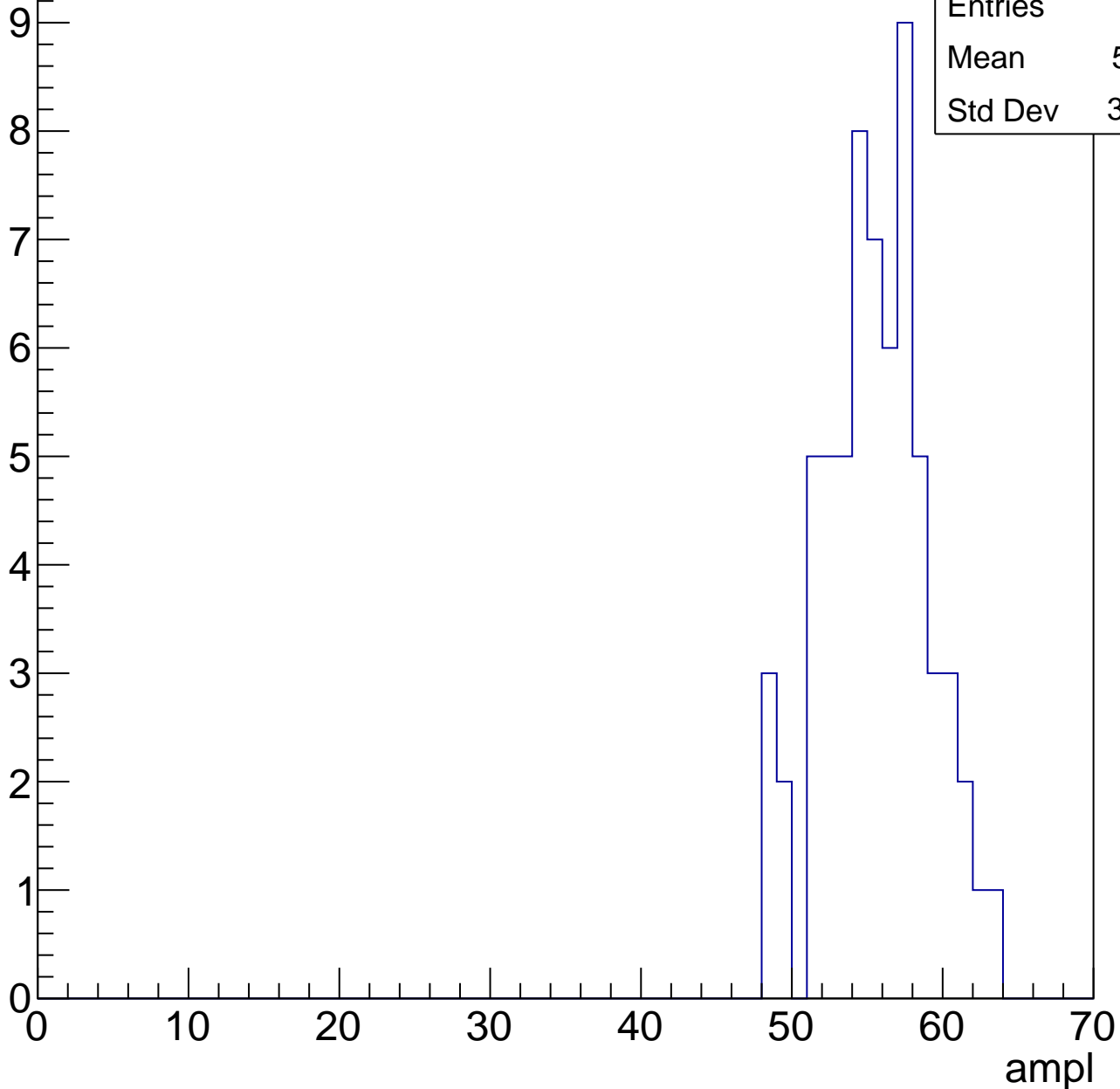


# B0L002S, U2-ch118, adc4

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	65
Mean	55.11
Std Dev	3.433



# B0L002S, U2-ch118, adc5

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

7

6

5

4

3

2

1

0

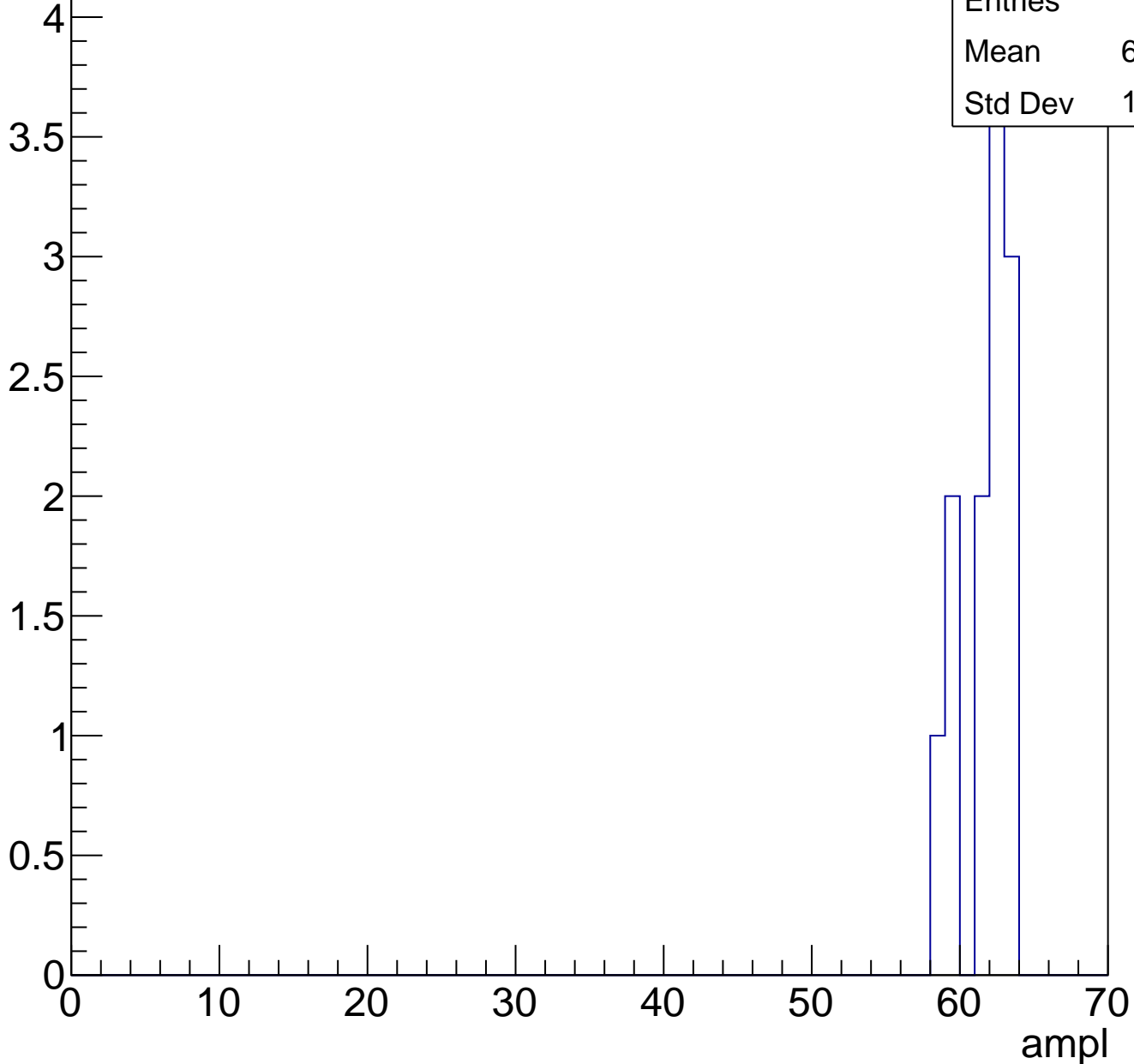
Entries	40
Mean	58.4
Std Dev	9.625

ampl

# B0L002S, U2-ch118, adc6

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry





# B0L002S, U2-ch118, adc7

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L002S, U2-ch119, adc0

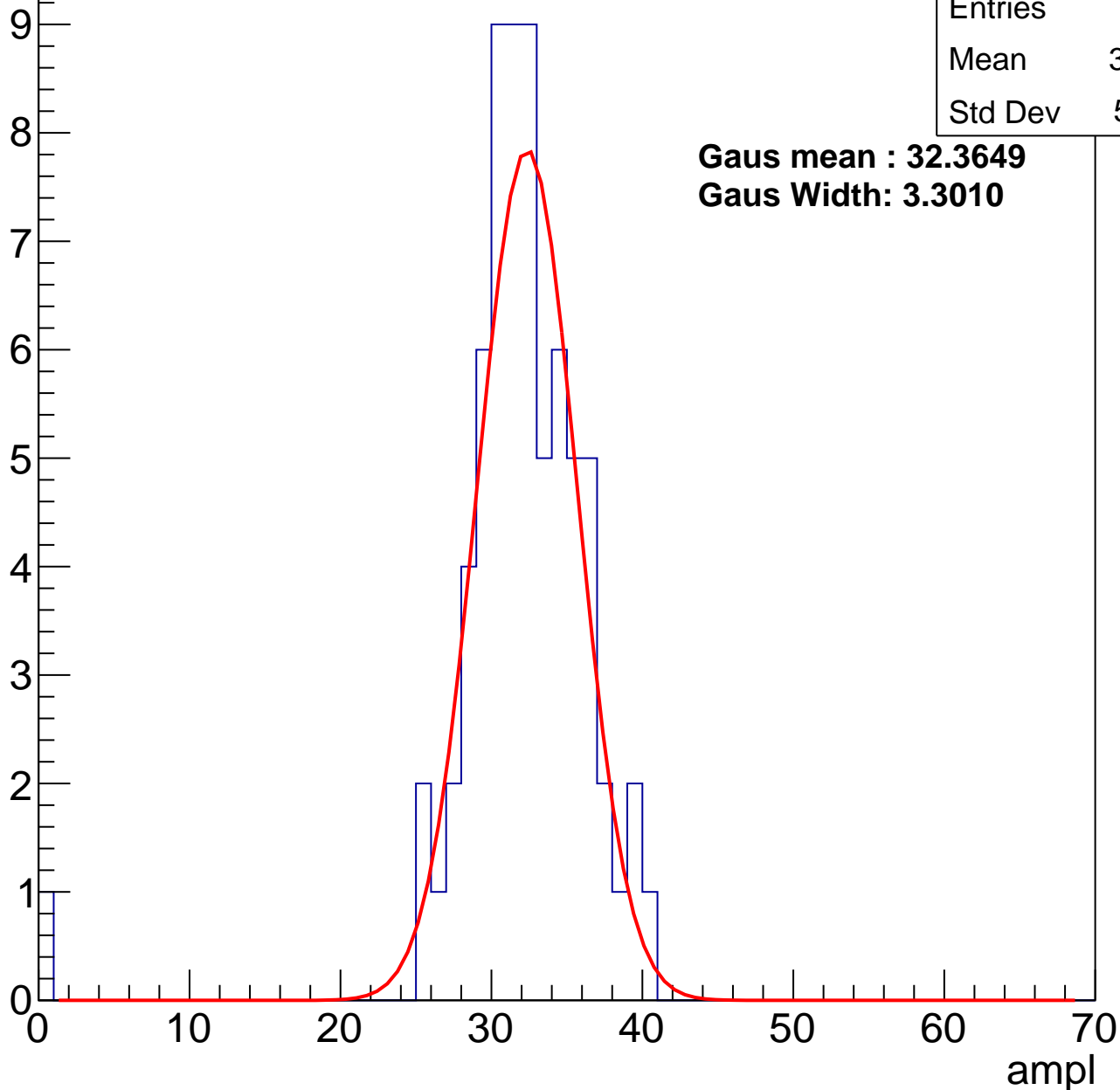
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	70
Mean	31.53
Std Dev	5.011

**Gaus mean : 32.3649**

**Gaus Width: 3.3010**



# B0L002S, U2-ch119, adc1

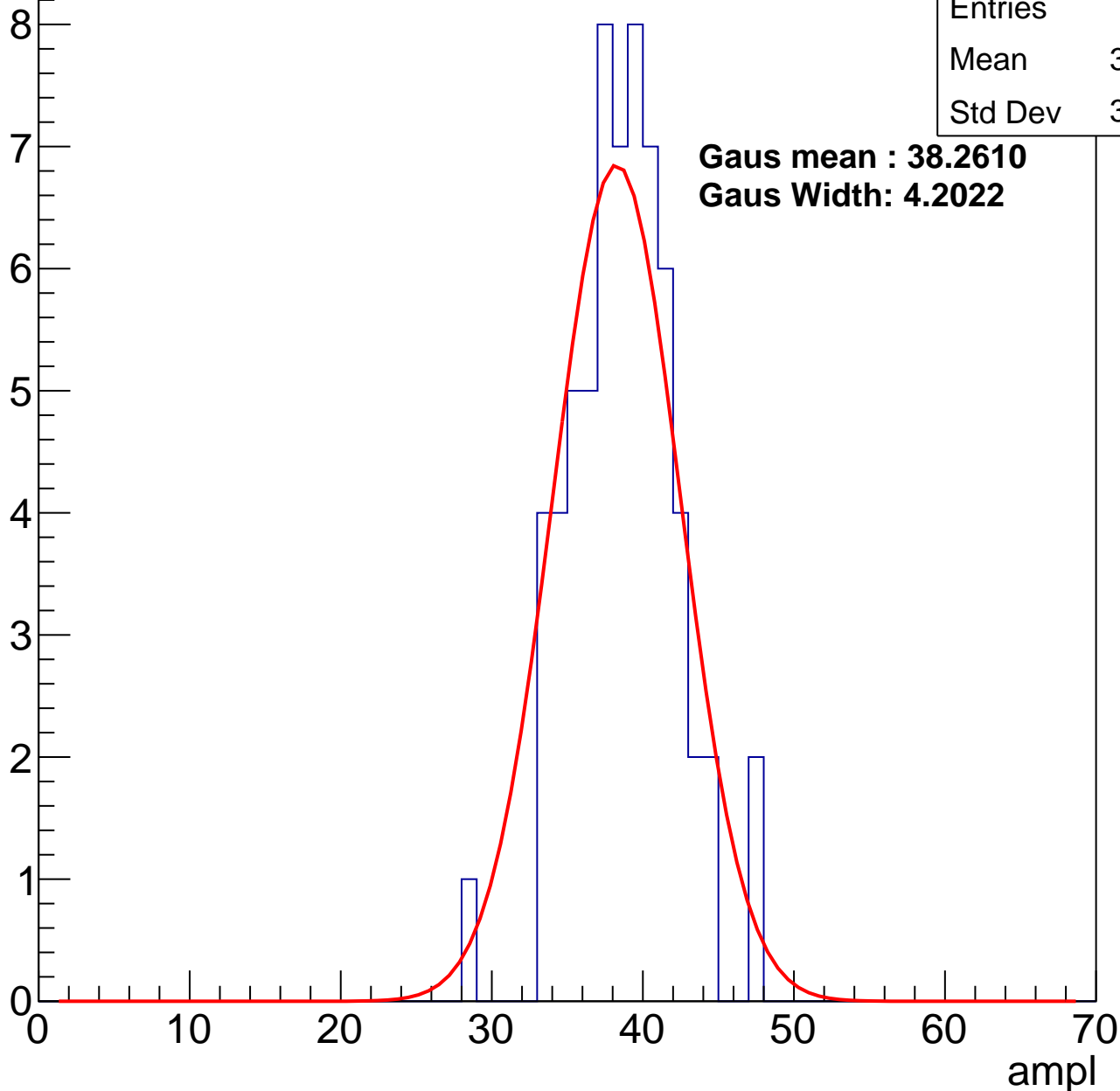
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	65
Mean	38.26
Std Dev	3.443

**Gaus mean : 38.2610**

**Gaus Width: 4.2022**



# B0L002S, U2-ch119, adc2

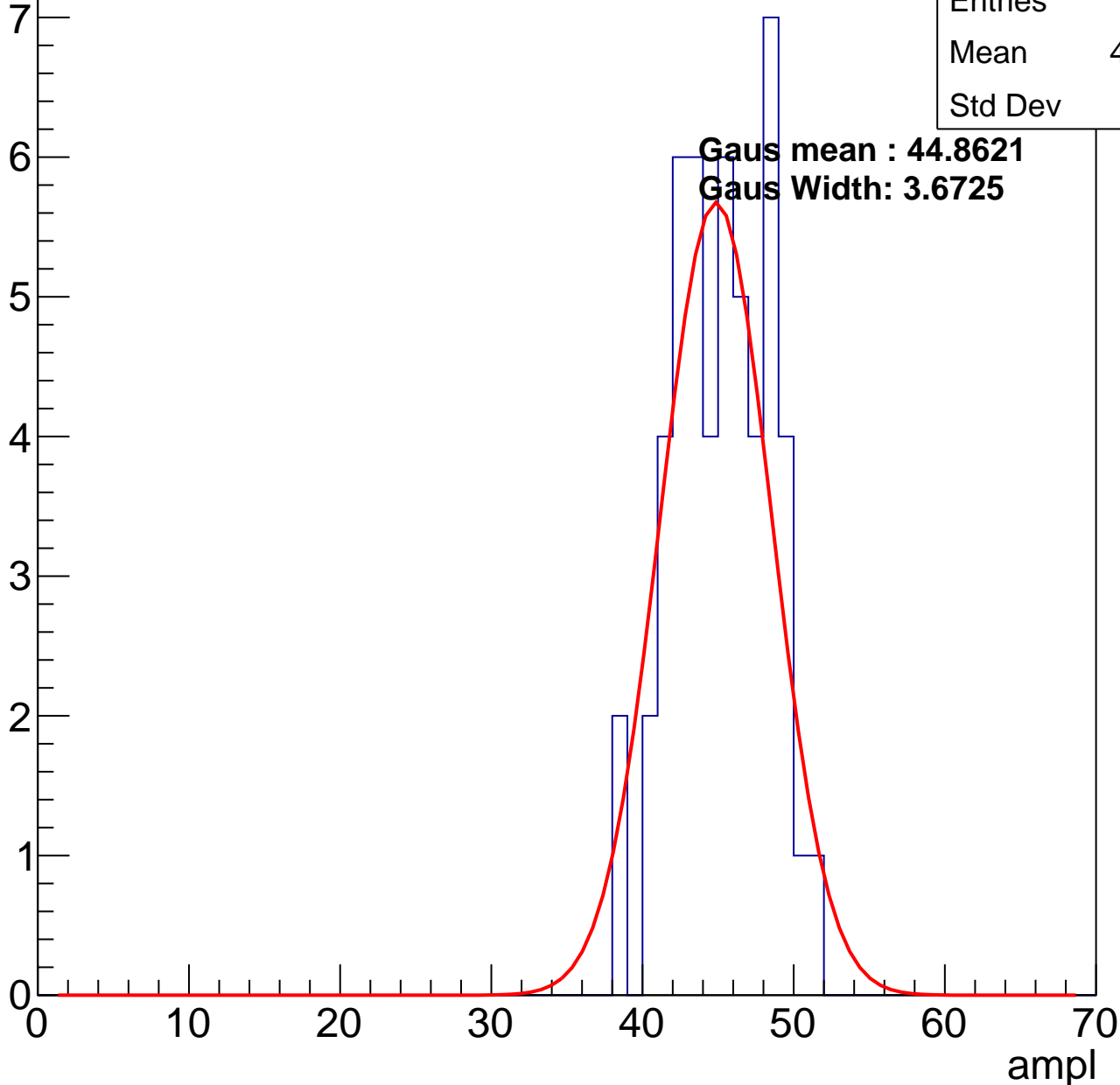
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	52
Mean	44.75
Std Dev	3.1

**Gaus mean : 44.8621**

**Gaus Width: 3.6725**

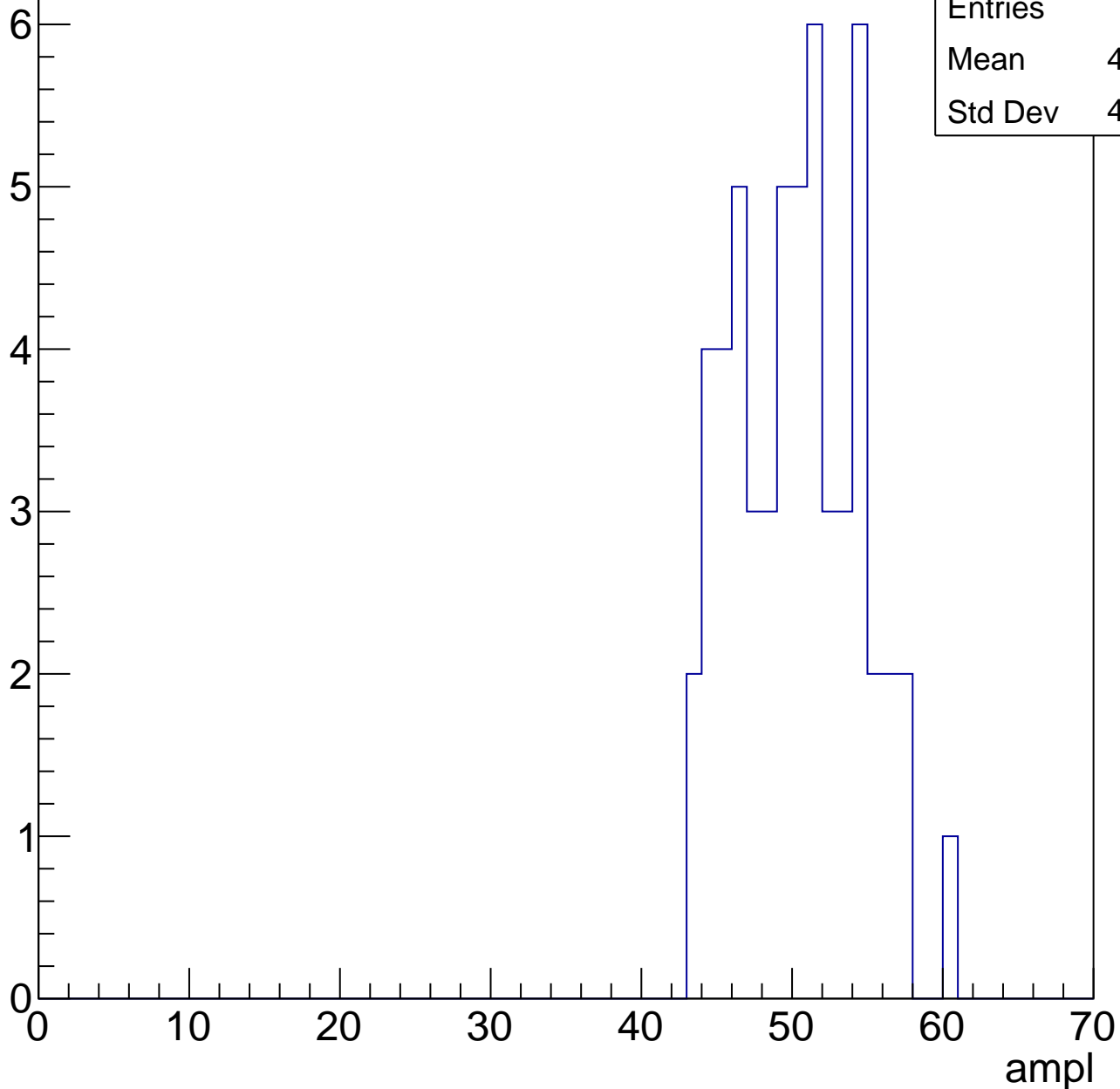


# B0L002S, U2-ch119, adc3

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	56
Mean	49.88
Std Dev	4.067

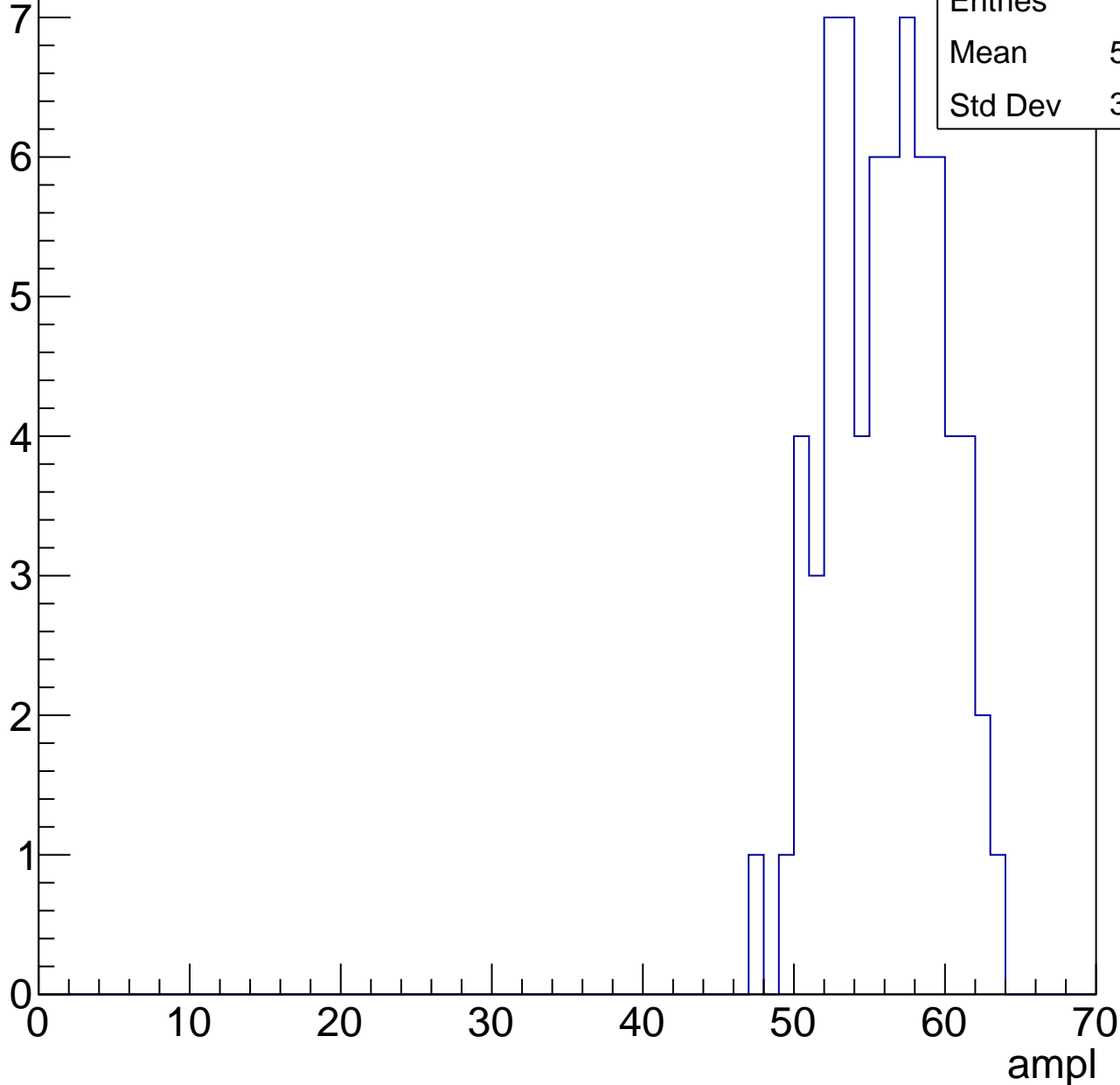


# B0L002S, U2-ch119, adc4

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	69
Mean	55.62
Std Dev	3.624

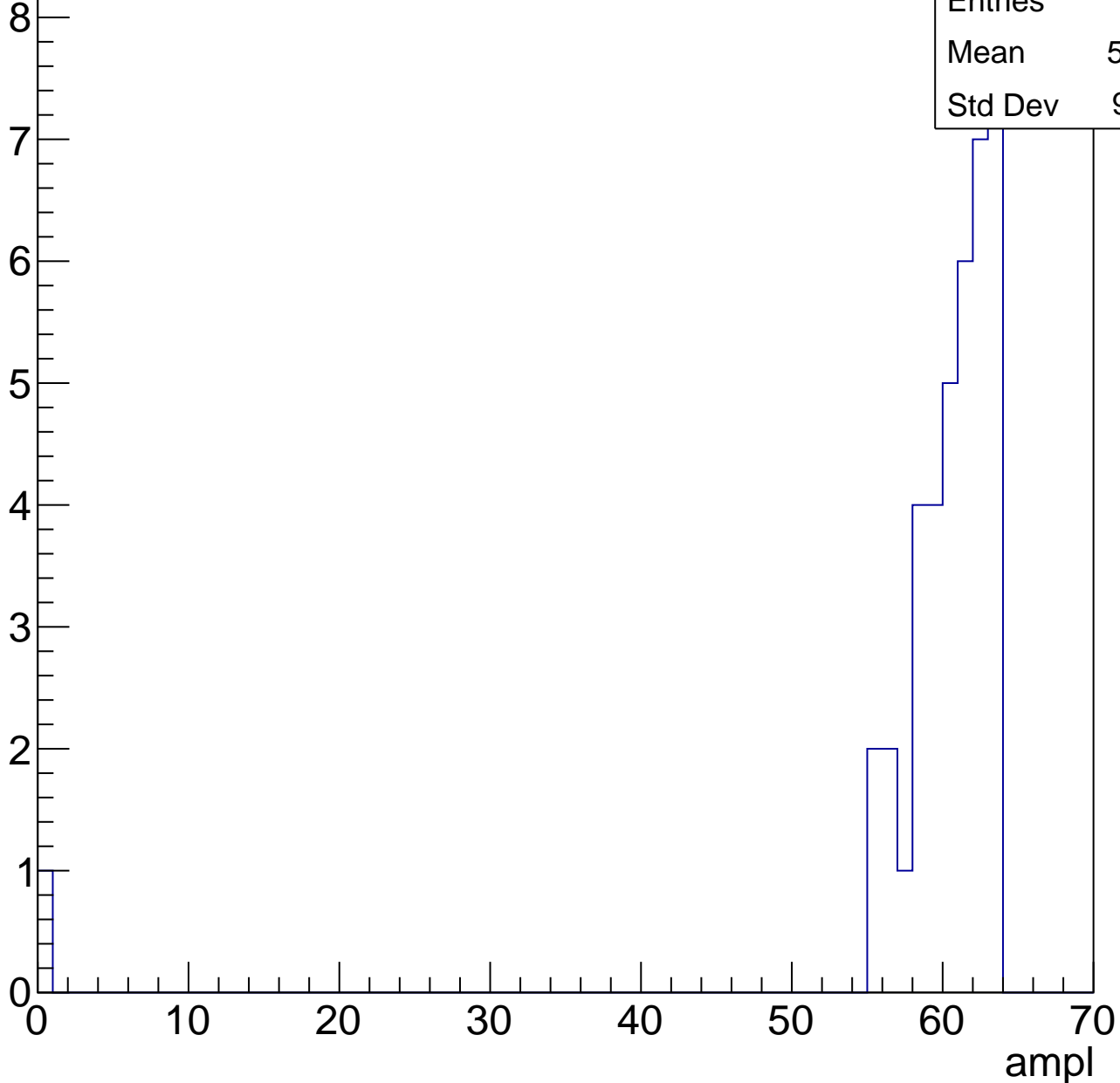


# B0L002S, U2-ch119, adc5

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	40
Mean	58.77
Std Dev	9.691



# B0L002S, U2-ch119, adc6

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry





# B0L002S, U2-ch119, adc7

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L002S, U2-ch120, adc0

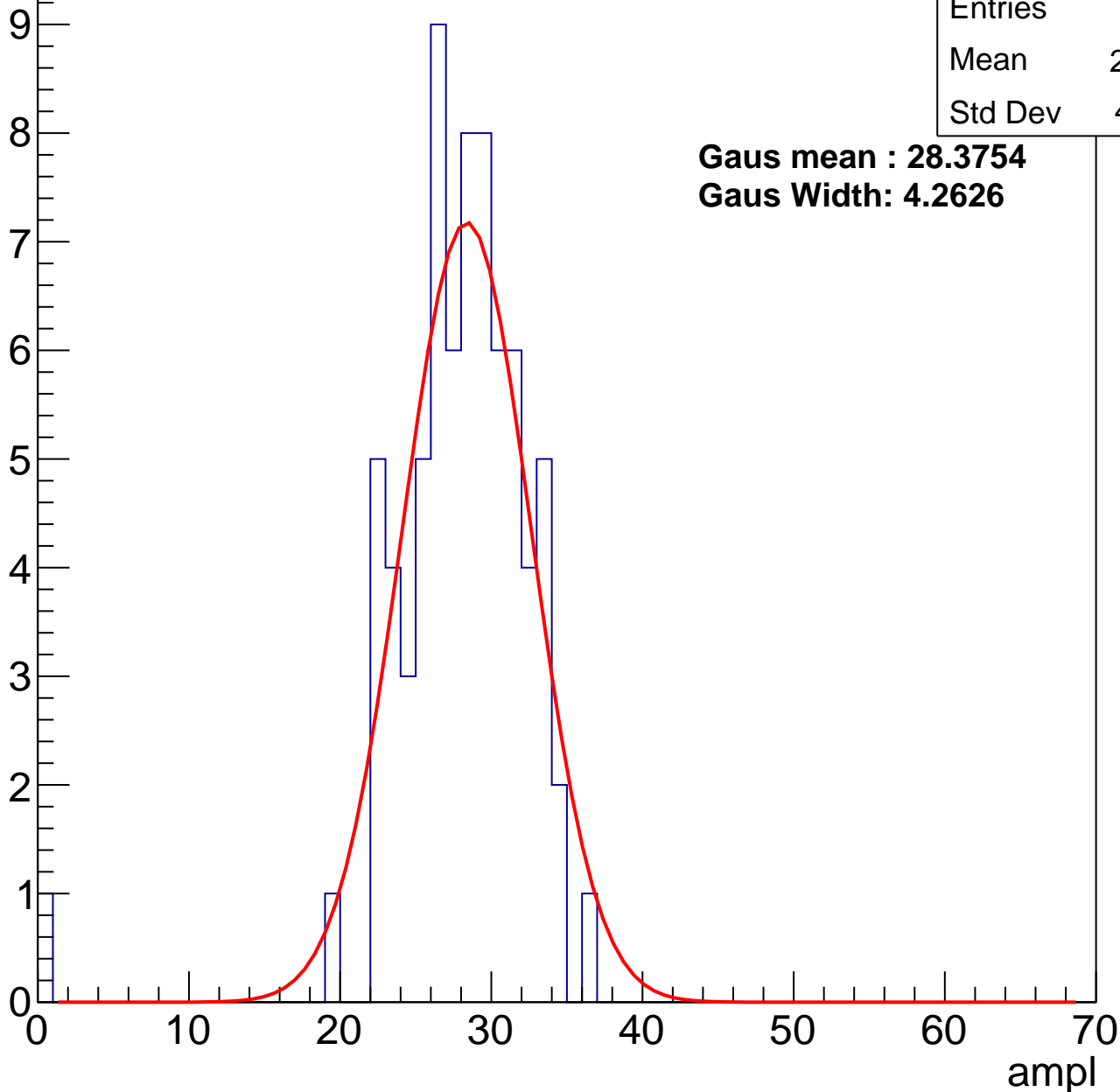
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	74
Mean	27.47
Std Dev	4.751

**Gaus mean : 28.3754**

**Gaus Width: 4.2626**



# B0L002S, U2-ch120, adc1

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entries	73
Mean	35.52
Std Dev	3.197

**Gaus mean : 35.8107**

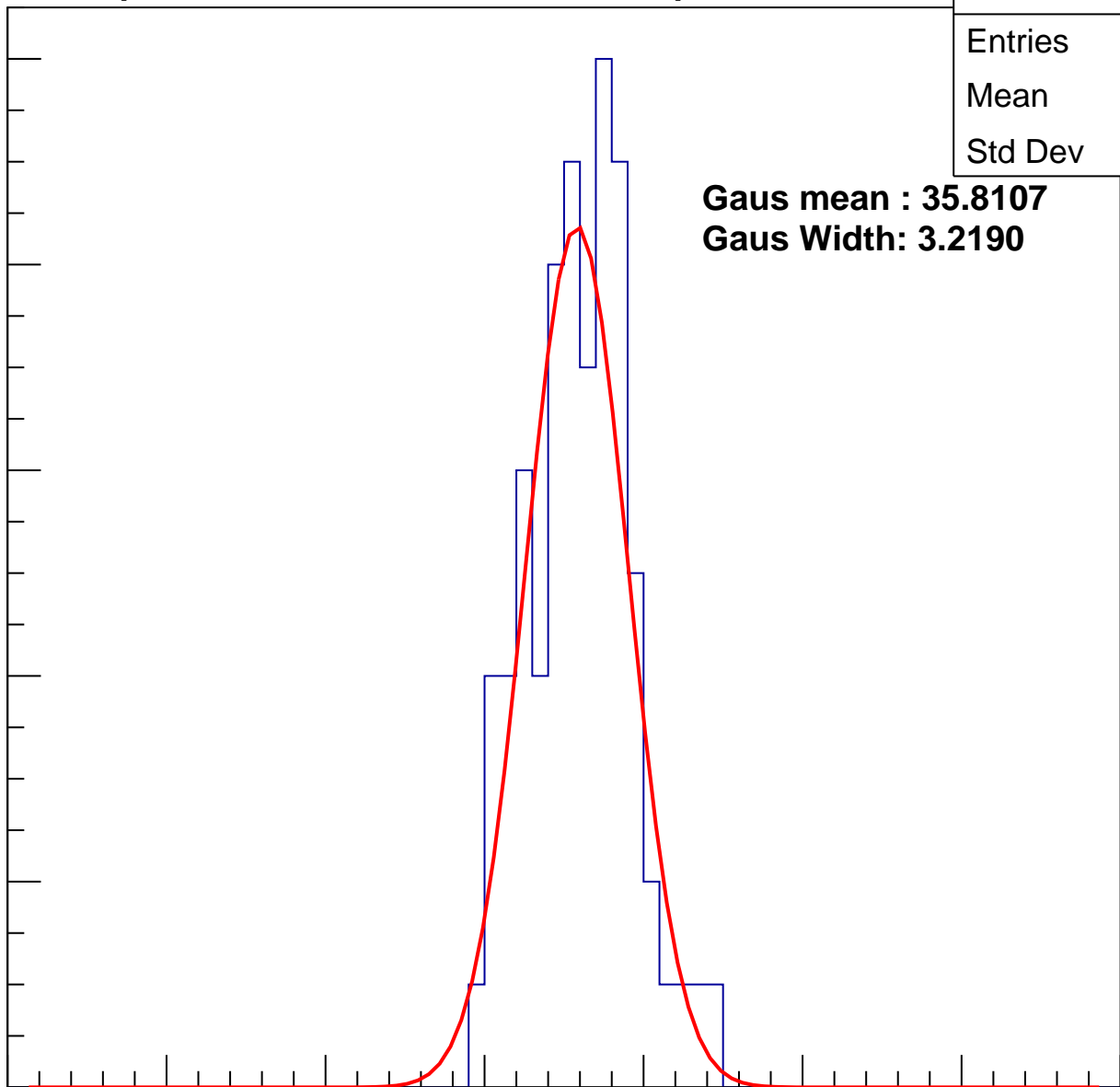
**Gaus Width: 3.2190**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L002S, U2-ch120, adc2

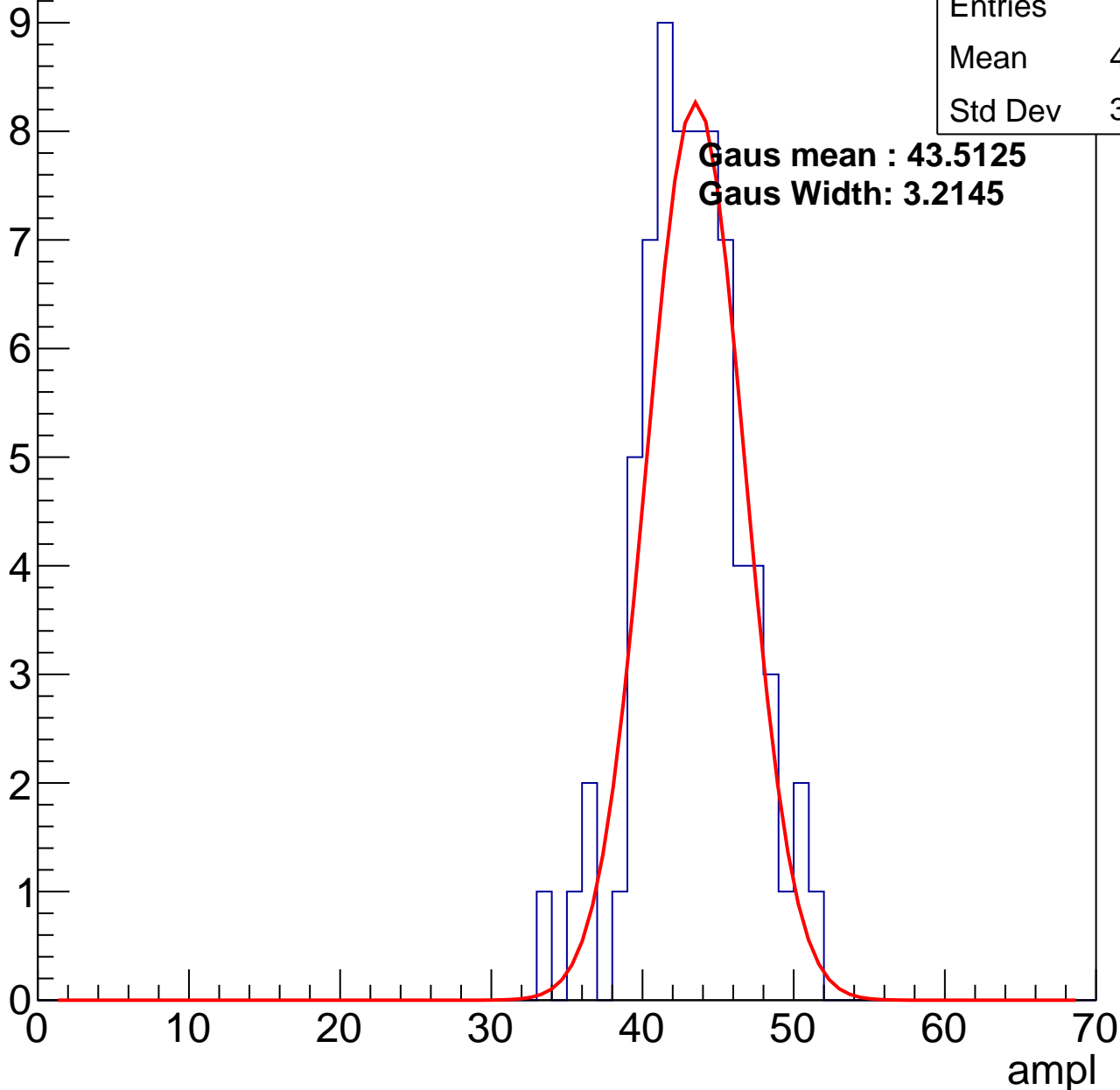
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	72
Mean	42.85
Std Dev	3.499

**Gaus mean : 43.5125**

**Gaus Width: 3.2145**

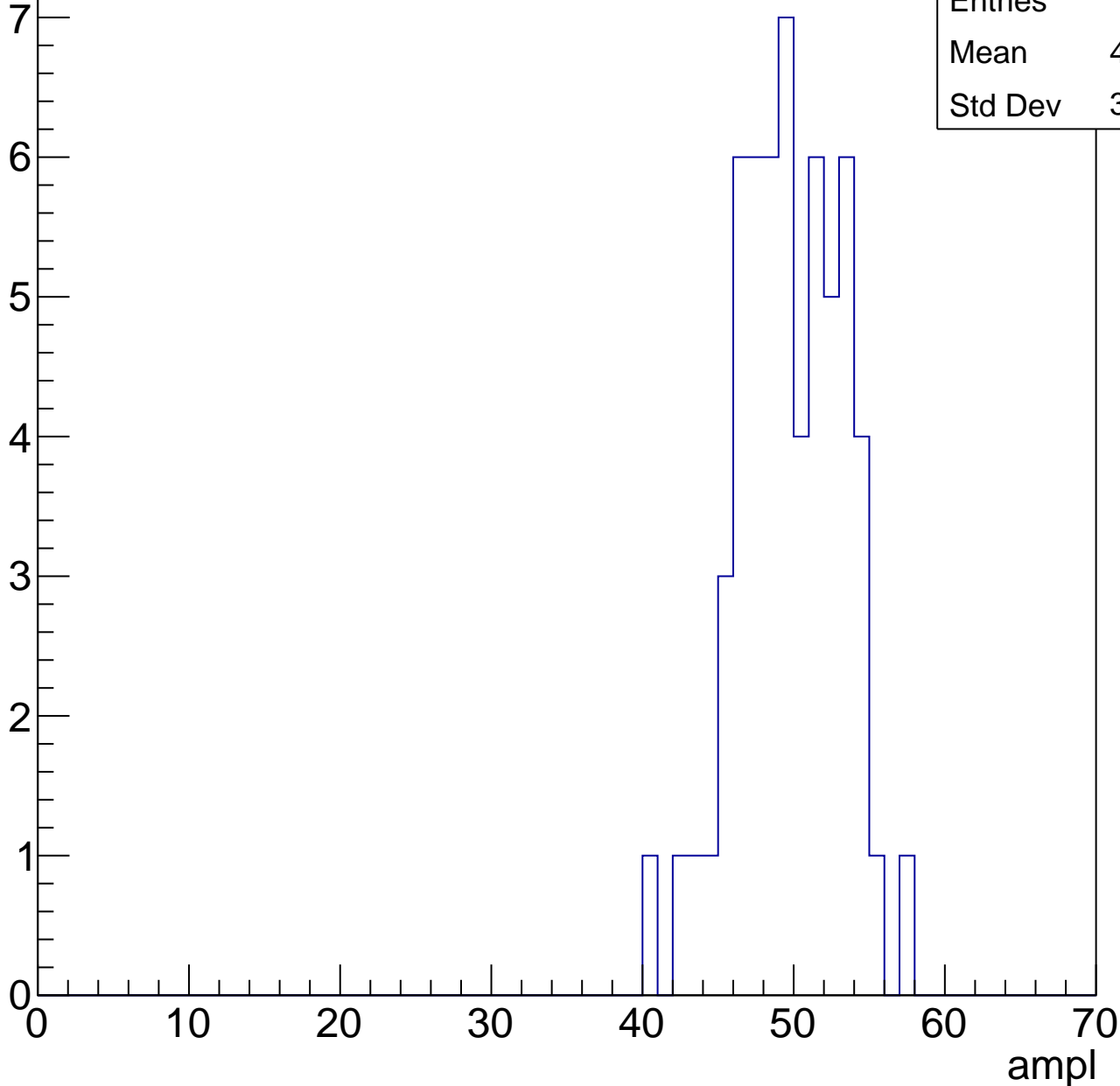


# B0L002S, U2-ch120, adc3

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	59
Mean	49.24
Std Dev	3.417

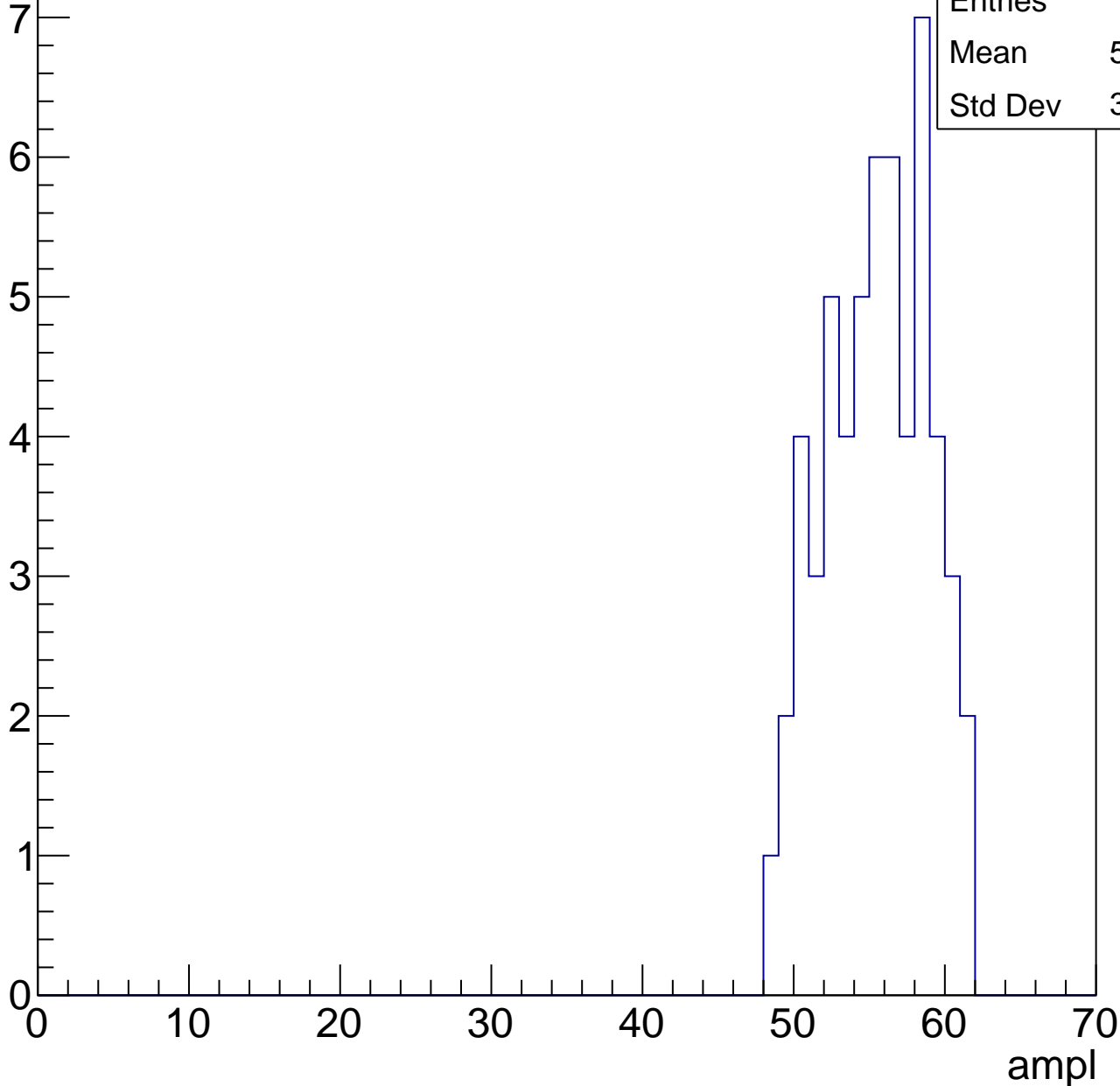


# B0L002S, U2-ch120, adc4

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	56
Mean	54.98
Std Dev	3.357

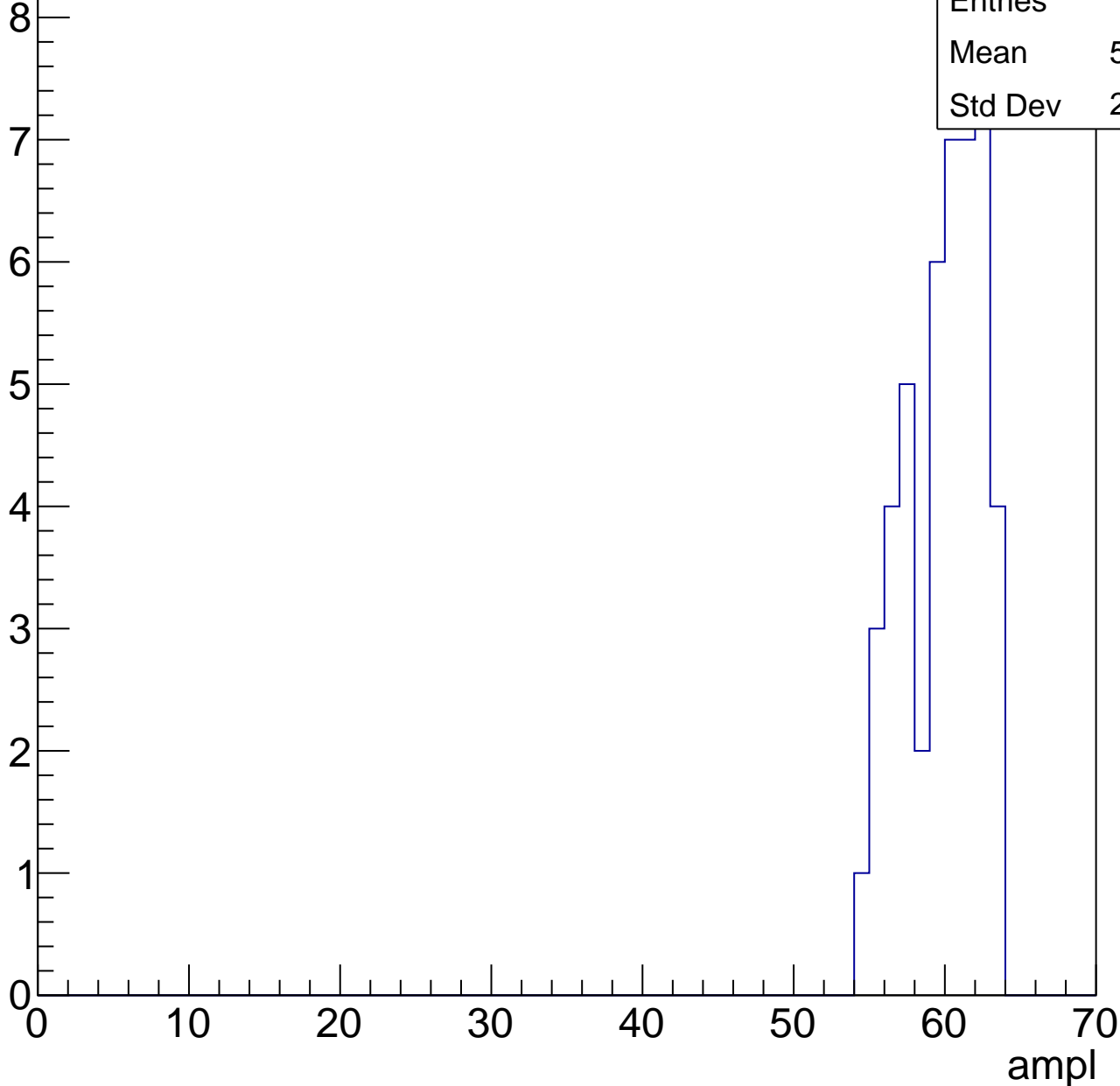


# B0L002S, U2-ch120, adc5

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	47
Mean	59.43
Std Dev	2.499

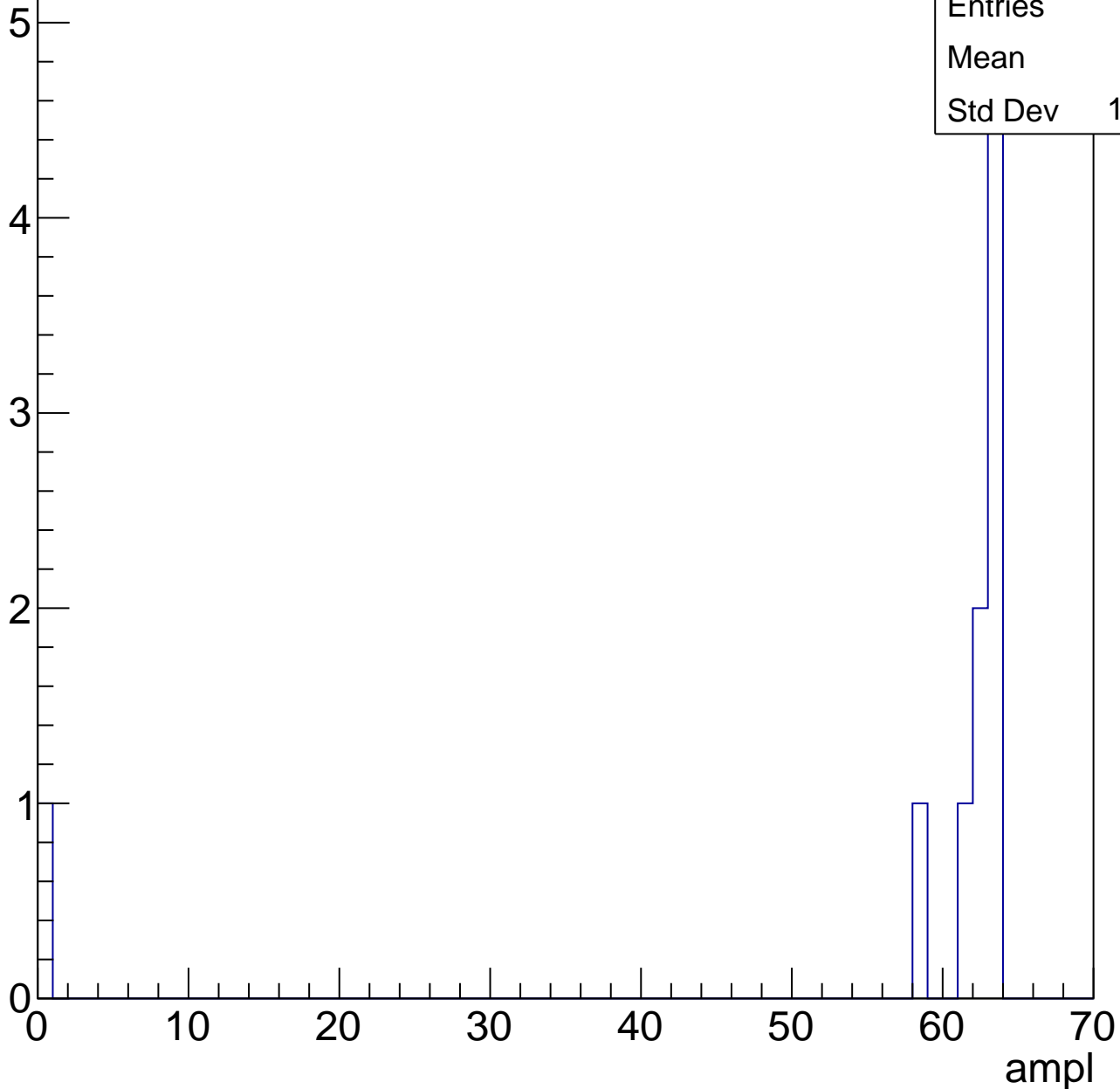


# B0L002S, U2-ch120, adc6

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	10
Mean	55.8
Std Dev	18.66





# B0L002S, U2-ch120, adc7

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



# B0L002S, U2-ch121, adc0

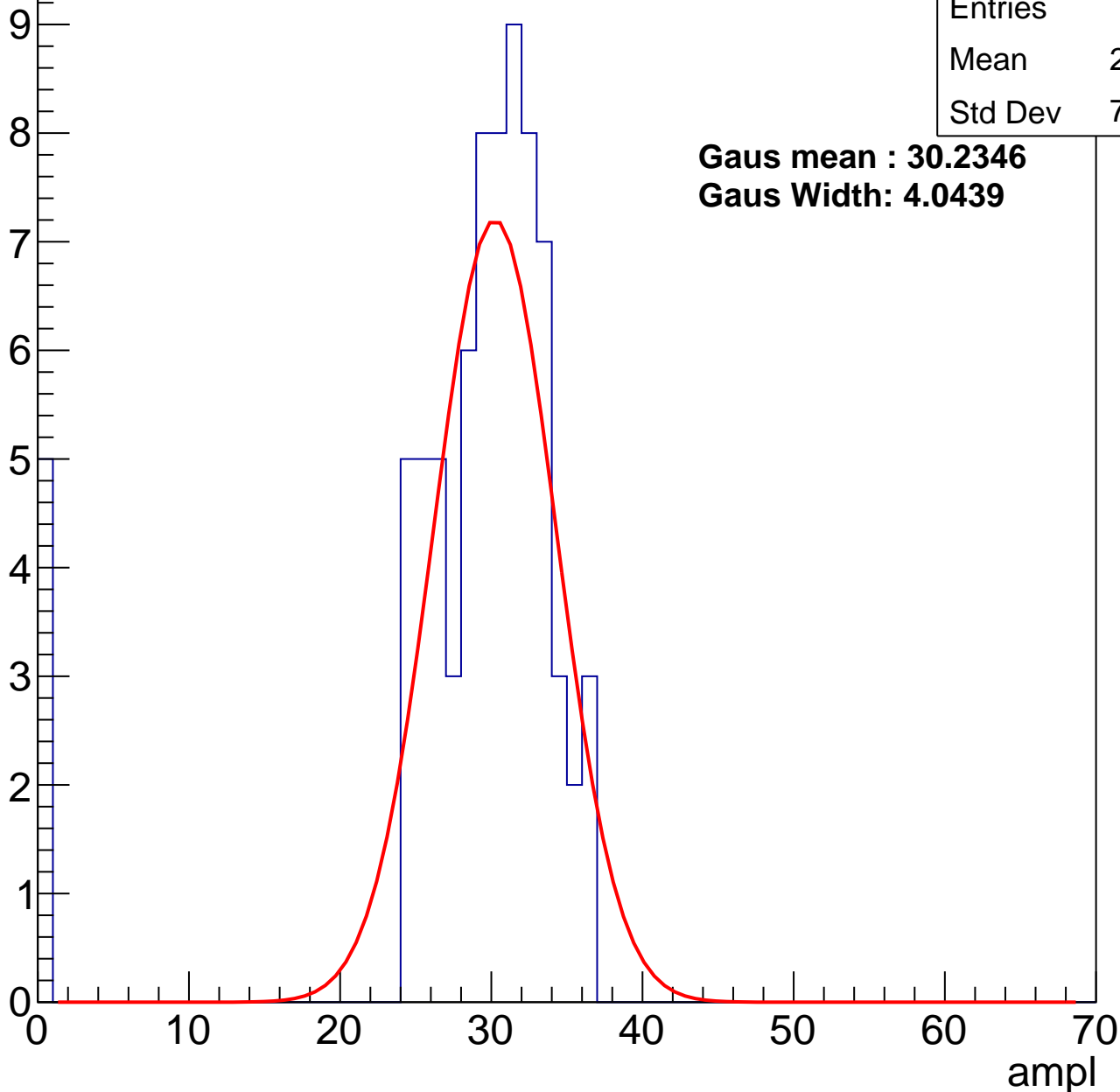
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	77
Mean	27.82
Std Dev	7.967

**Gaus mean : 30.2346**

**Gaus Width: 4.0439**



# B0L002S, U2-ch121, adc1

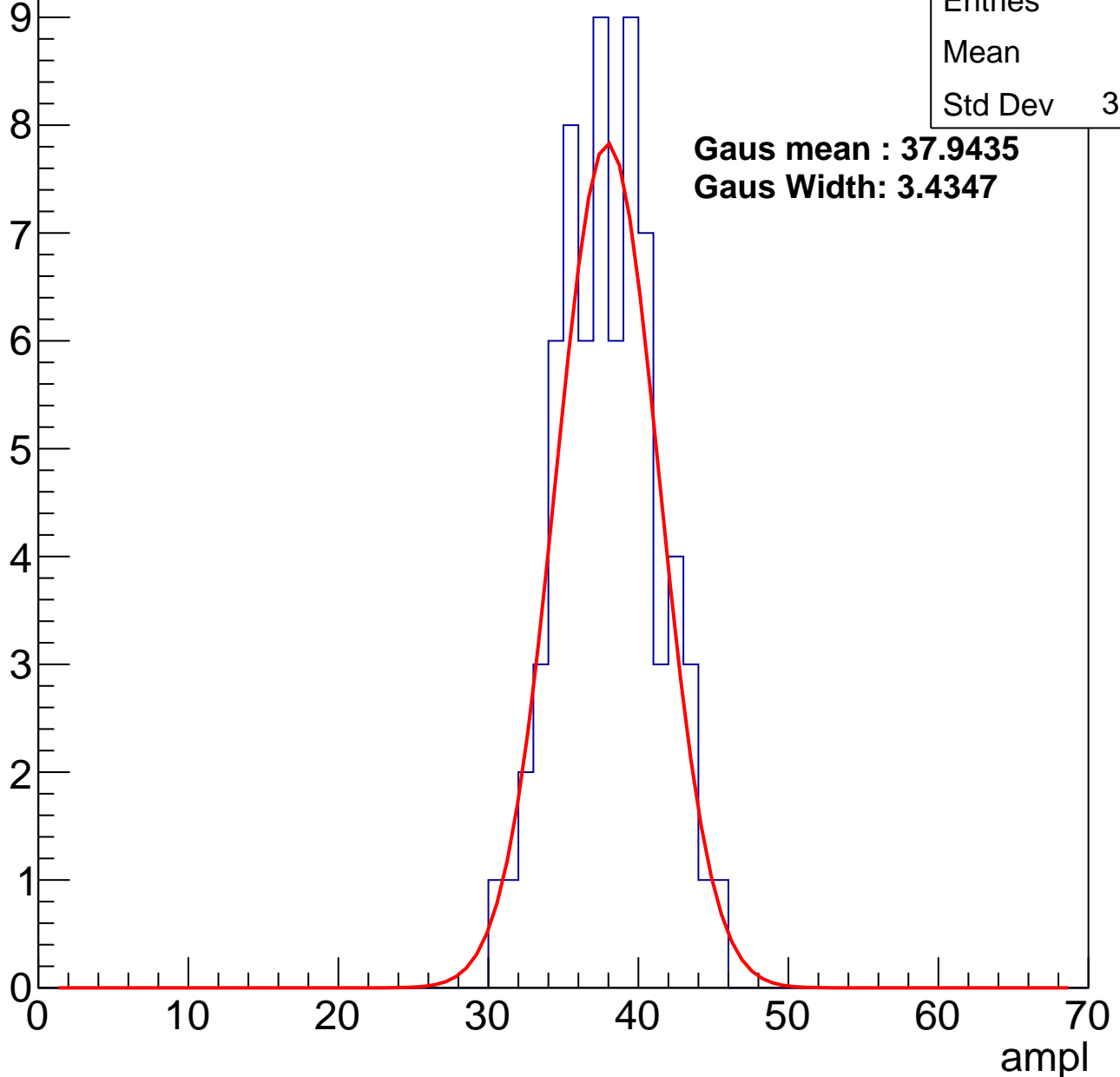
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	70
Mean	37.5
Std Dev	3.233

**Gaus mean : 37.9435**

**Gaus Width: 3.4347**



# B0L002S, U2-ch121, adc2

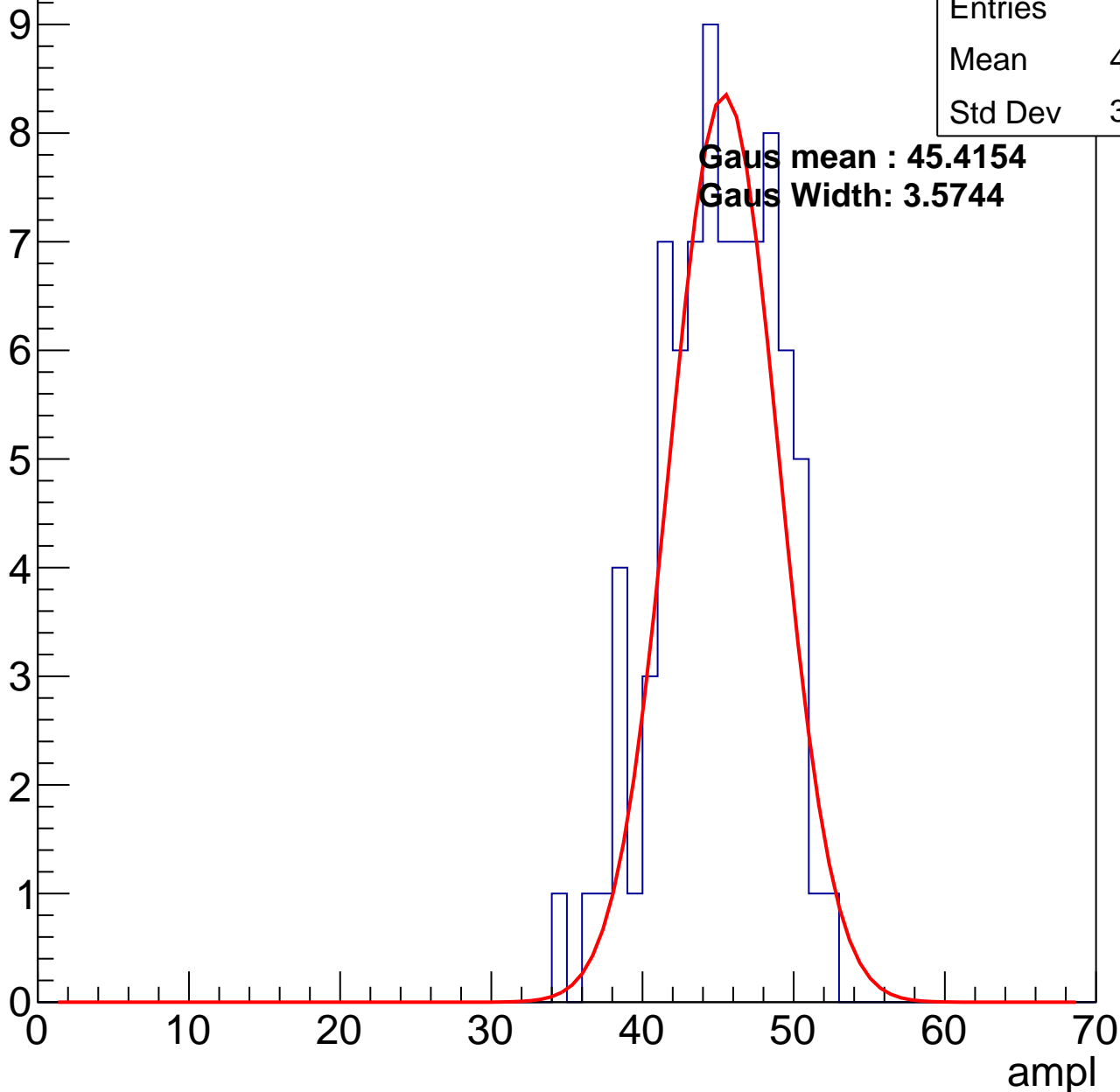
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	82
Mean	44.52
Std Dev	3.778

**Gaus mean : 45.4154**

**Gaus Width: 3.5744**



# B0L002S, U2-ch121, adc3

calib\_packv5\_042523\_0143.root, FC#8, port C1

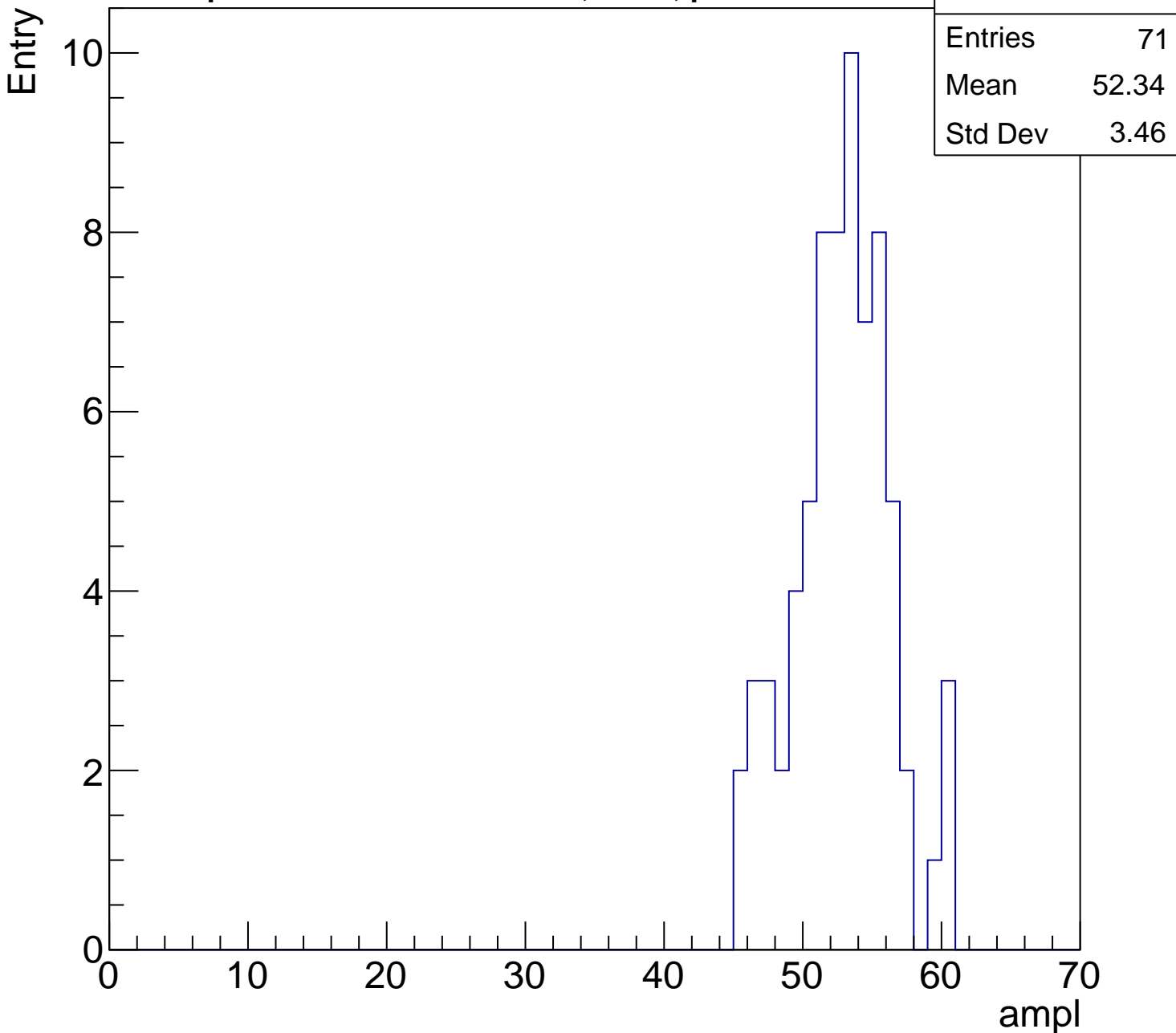
Entries	71
Mean	52.34
Std Dev	3.46

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

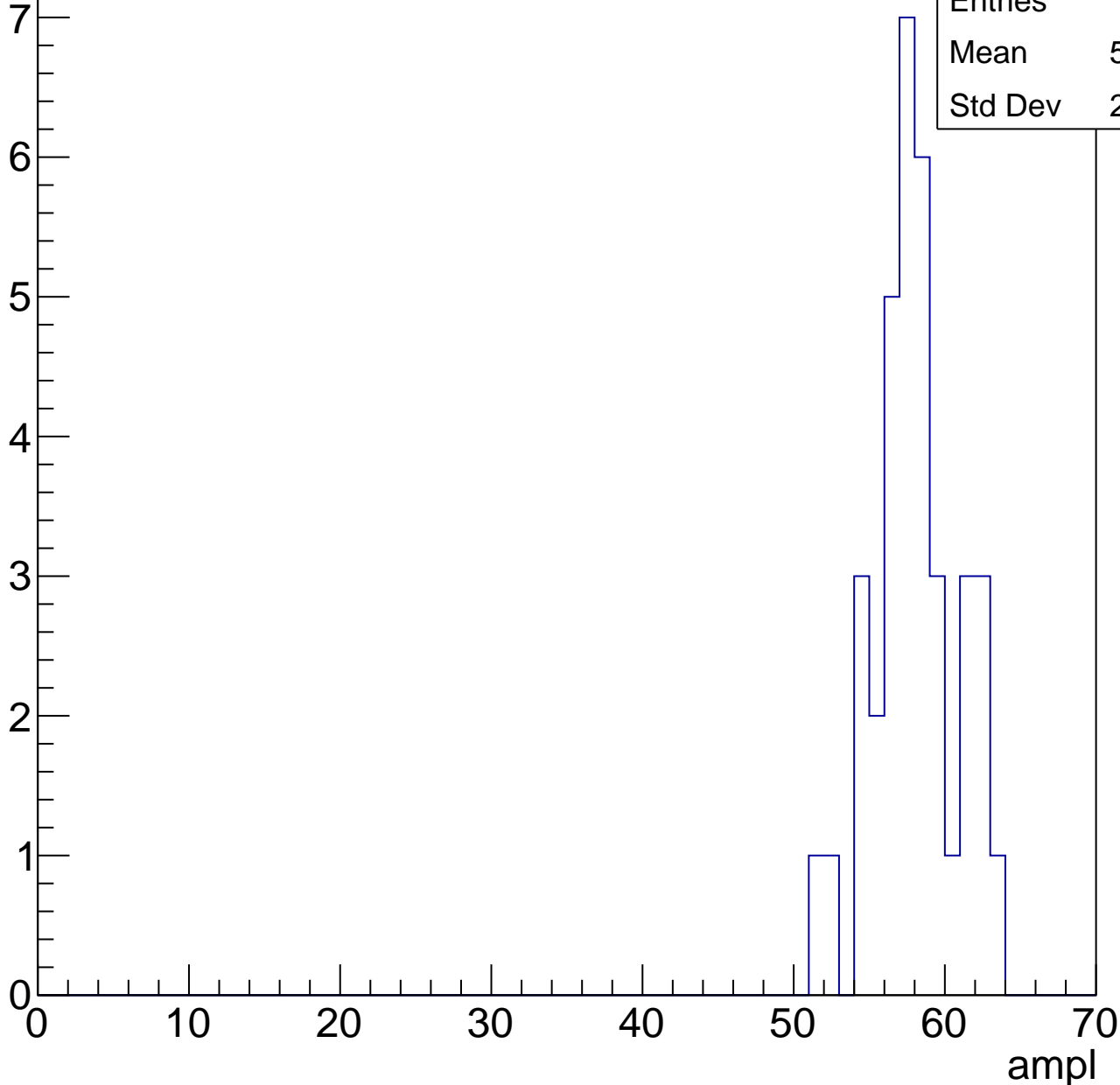


# B0L002S, U2-ch121, adc4

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	36
Mean	57.53
Std Dev	2.774

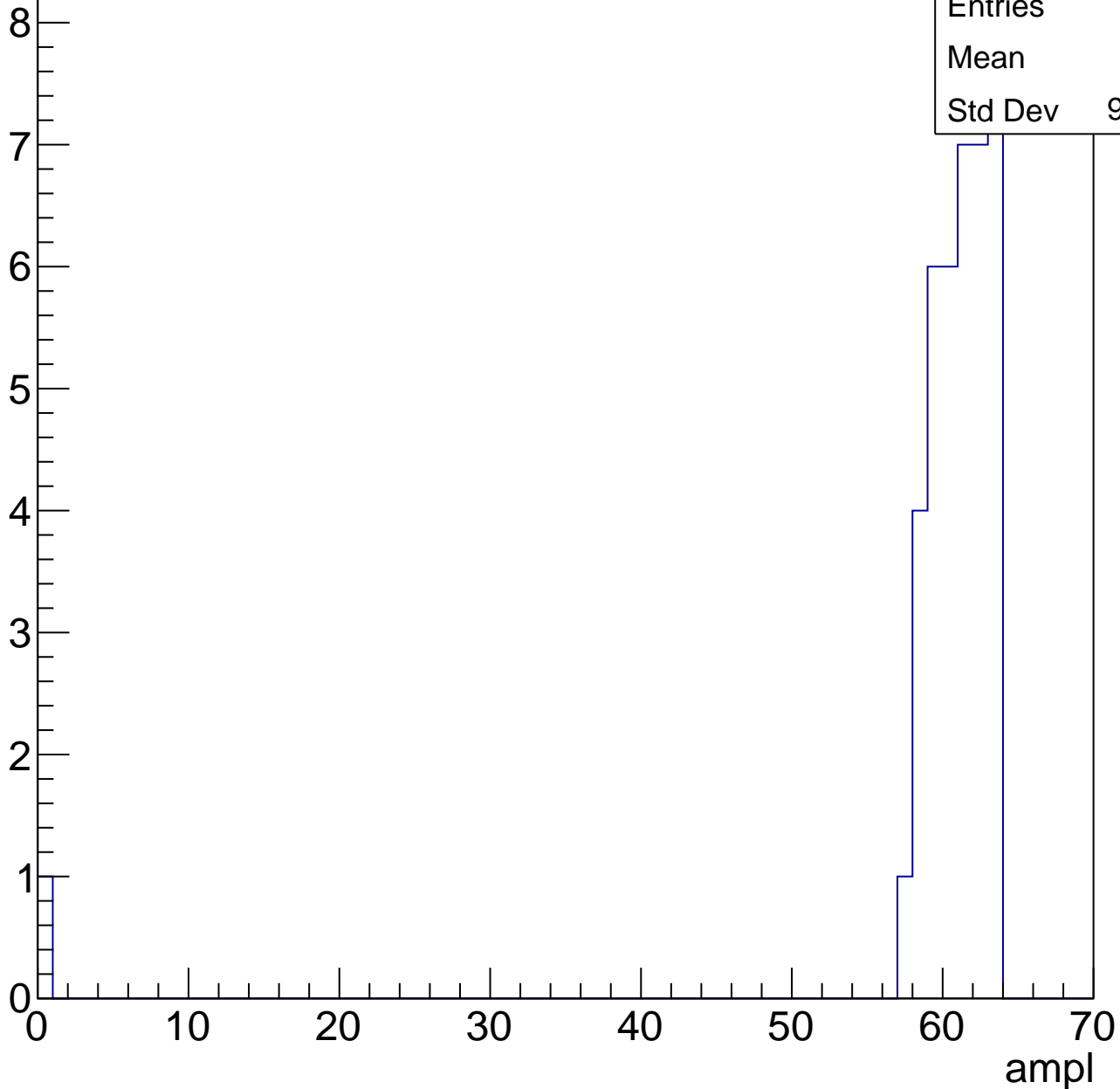


# B0L002S, U2-ch121, adc5

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	40
Mean	59.2
Std Dev	9.634



# B0L002S, U2-ch121, adc6

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry





# B0L002S, U2-ch121, adc7

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



# B0L002S, U2-ch122, adc0

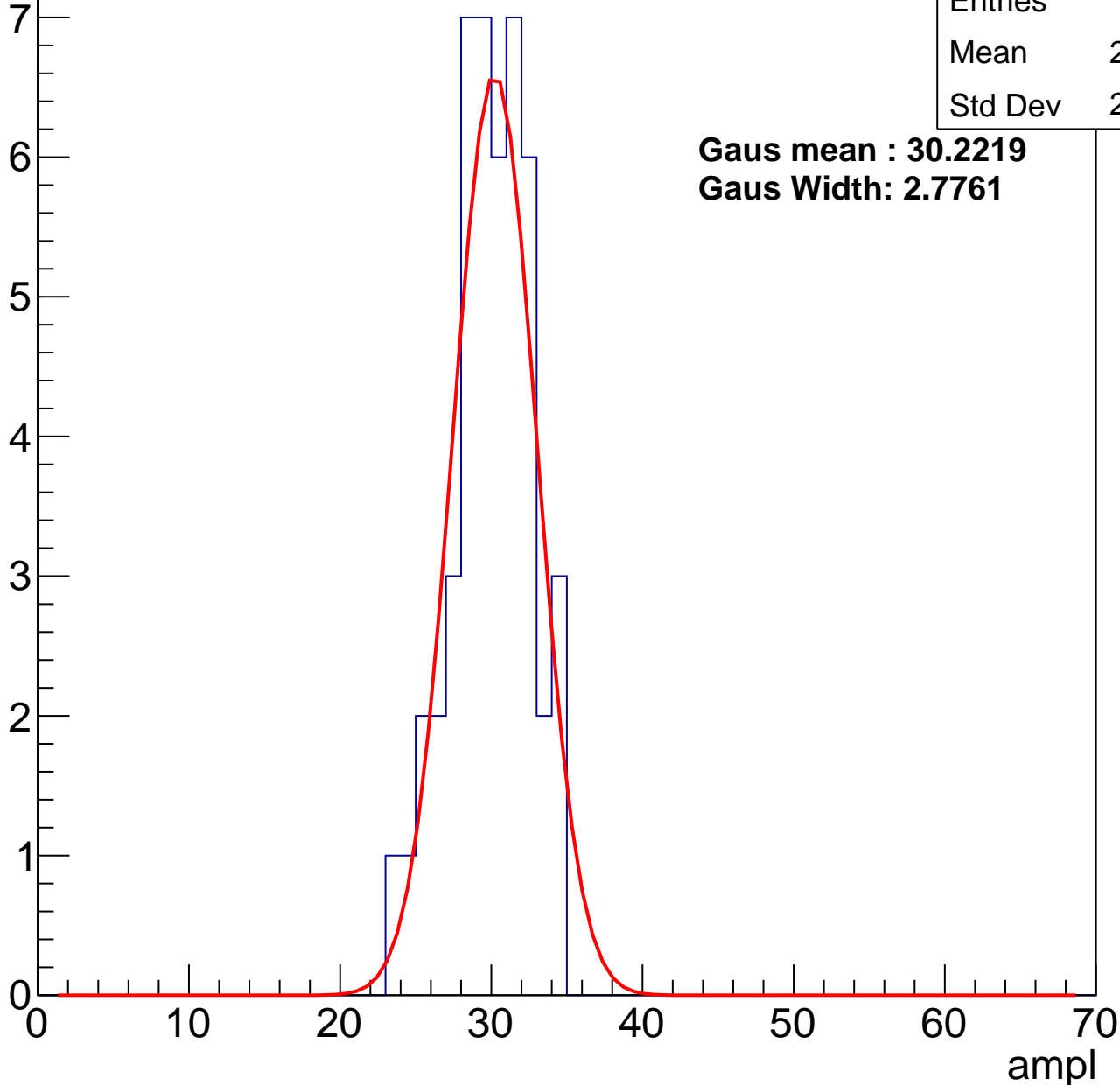
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	47
Mean	29.49
Std Dev	2.584

**Gaus mean : 30.2219**

**Gaus Width: 2.7761**



# B0L002S, U2-ch122, adc1

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

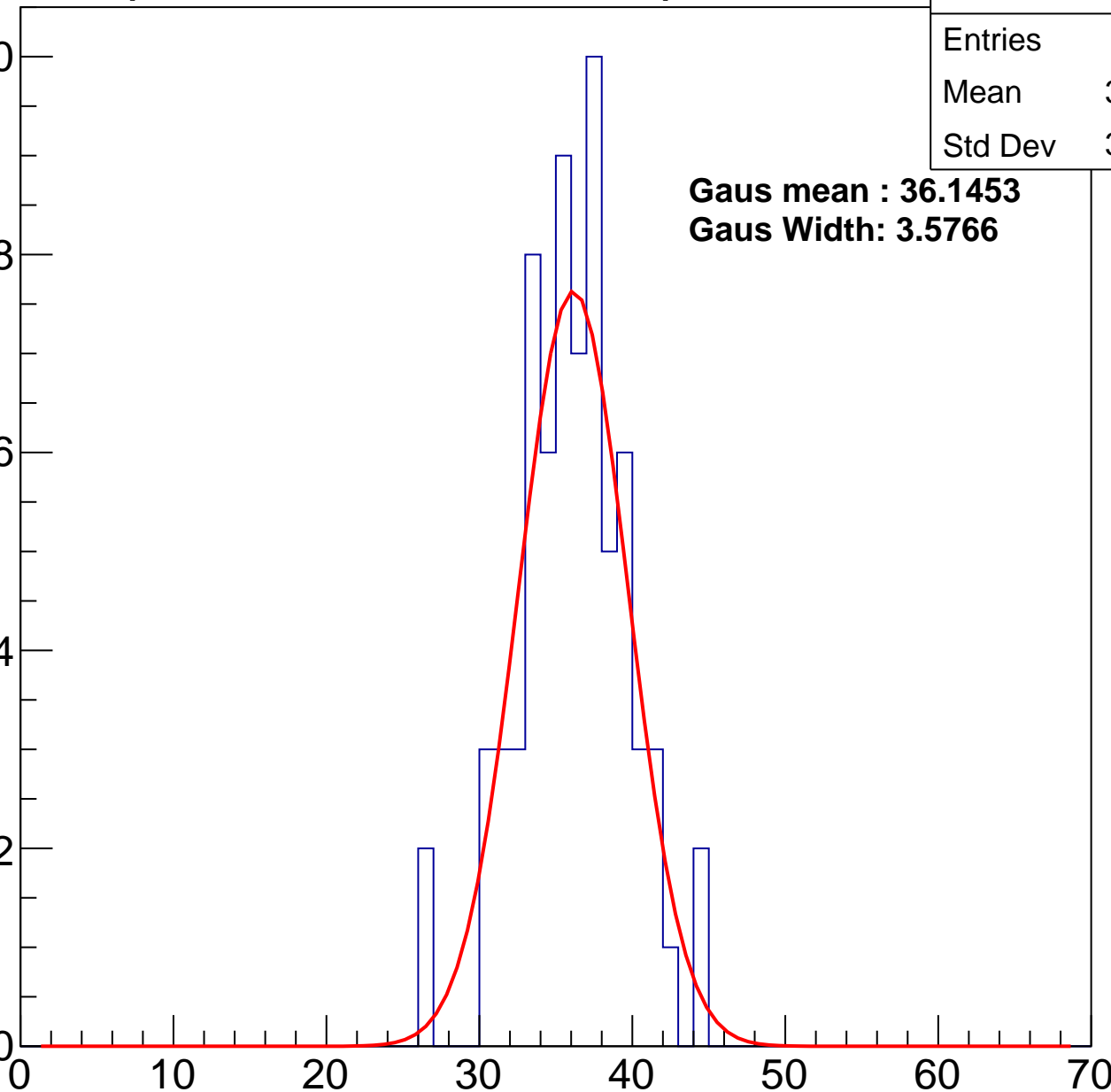
Entries	71
Mean	35.68
Std Dev	3.559

**Gaus mean : 36.1453**

**Gaus Width: 3.5766**

10  
8  
6  
4  
2  
0

ampl



# B0L002S, U2-ch122, adc2

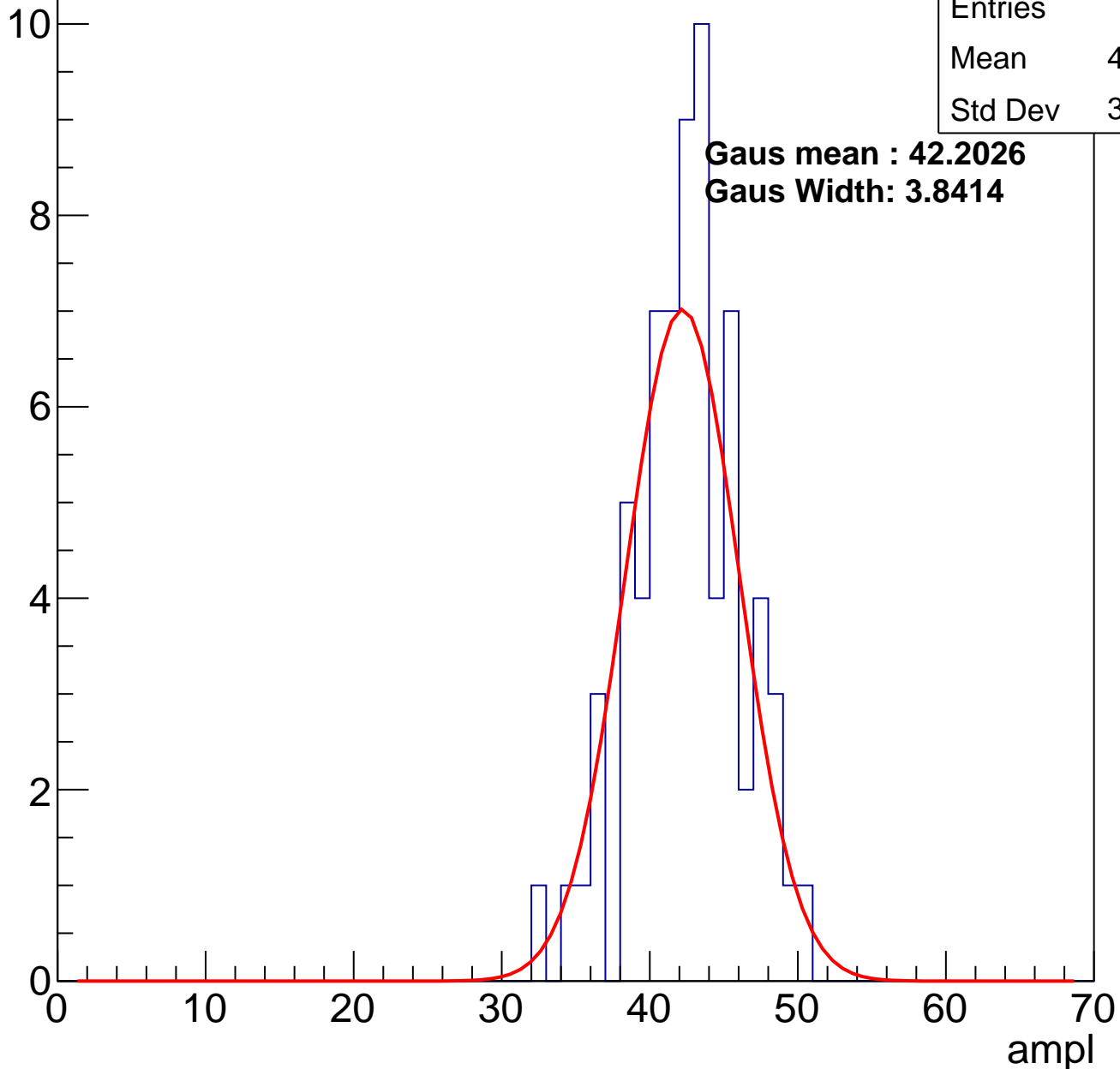
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entries	70
Mean	42.06
Std Dev	3.613

**Gaus mean : 42.2026**

**Gaus Width: 3.8414**

Entry

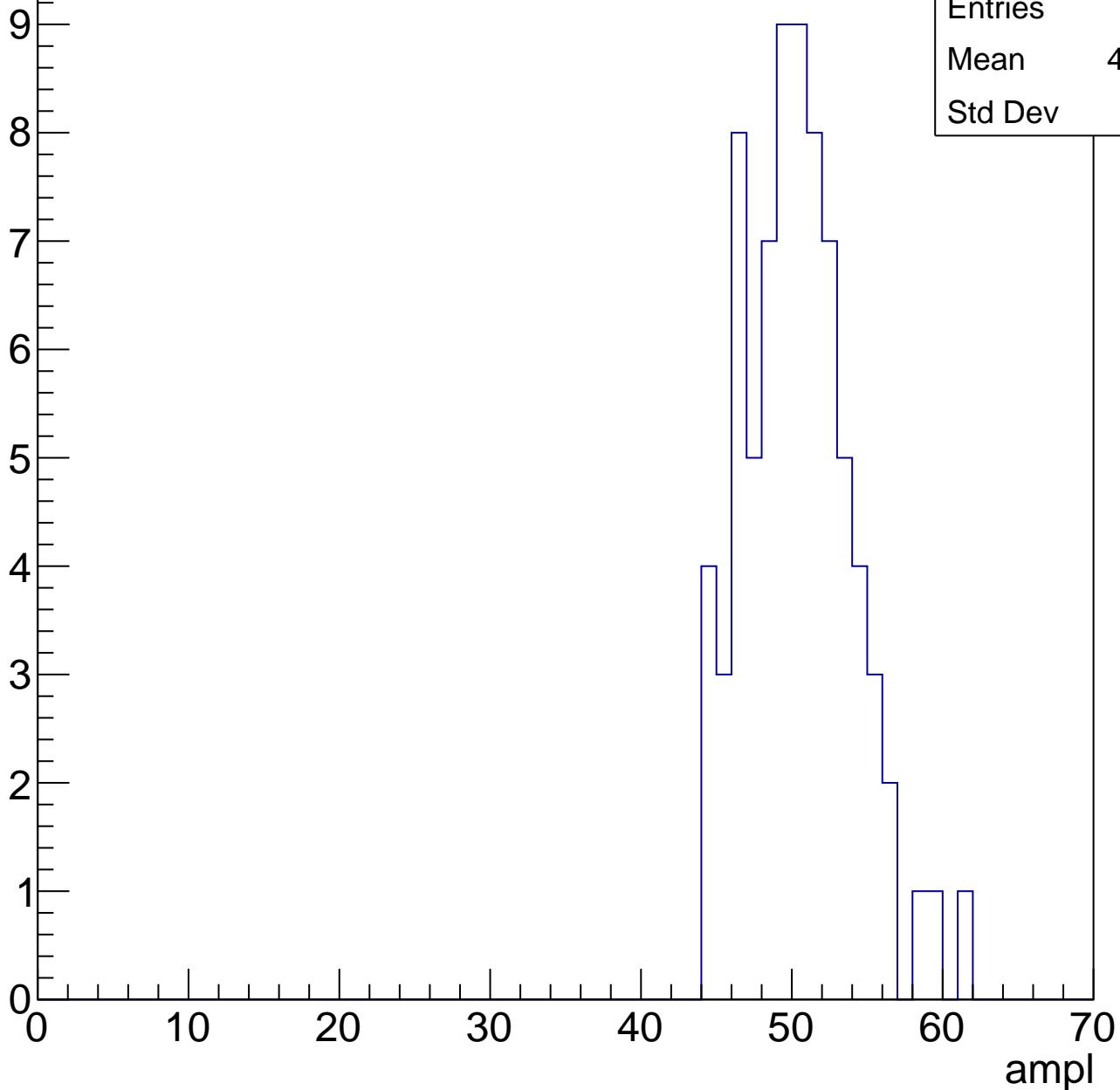


# B0L002S, U2-ch122, adc3

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	77
Mean	49.99
Std Dev	3.58

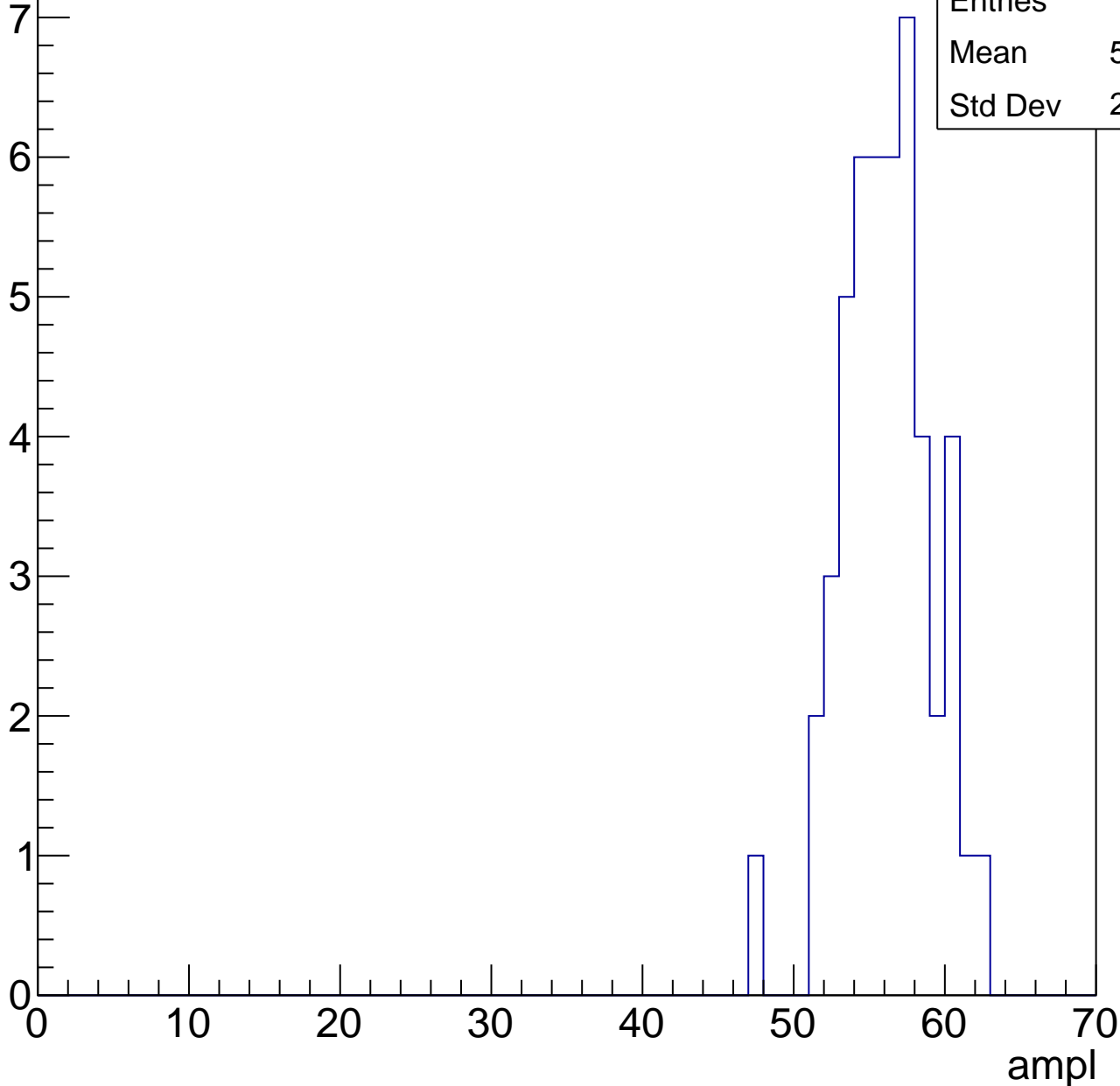


# B0L002S, U2-ch122, adc4

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	48
Mean	55.67
Std Dev	2.939

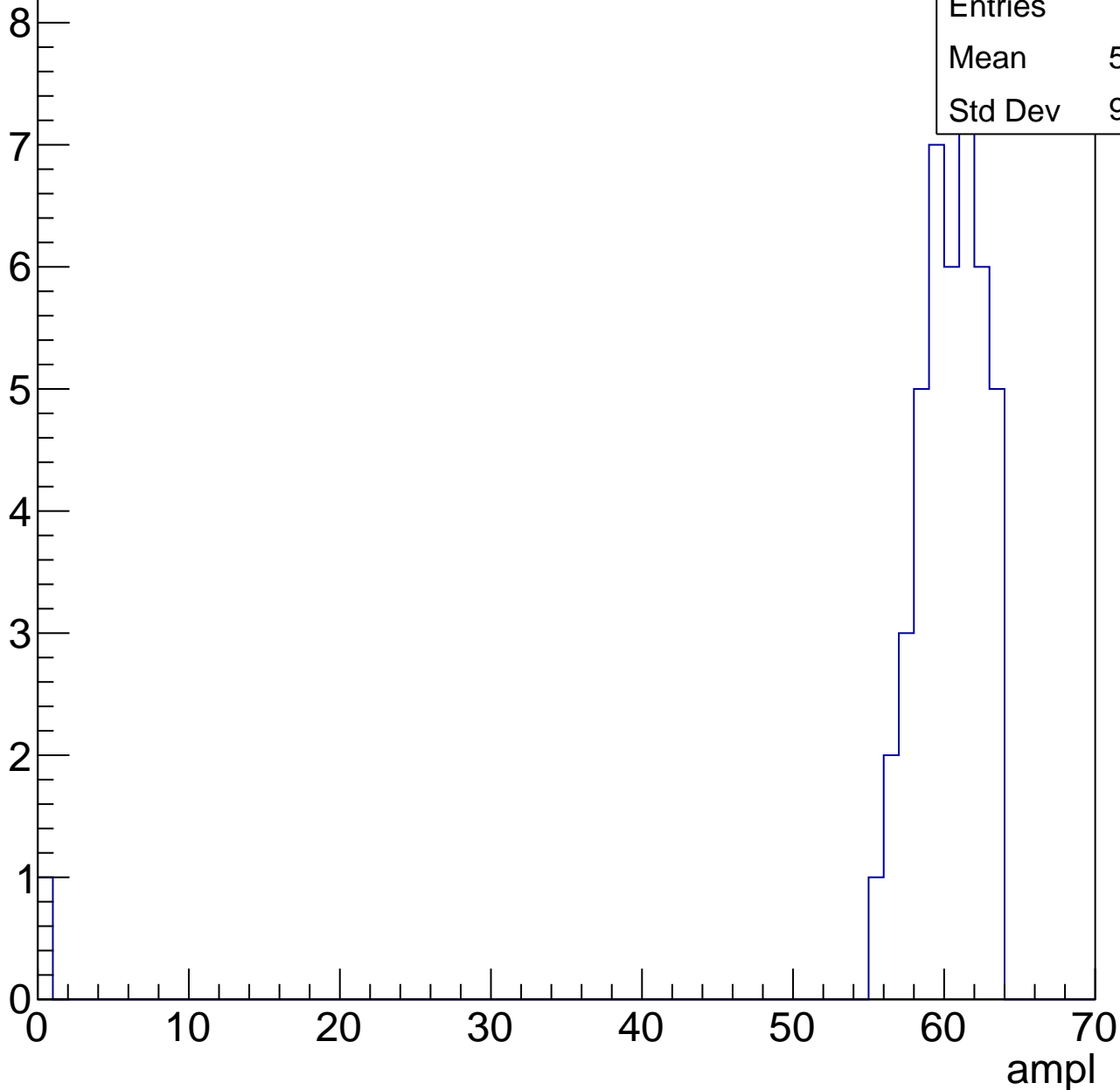


# B0L002S, U2-ch122, adc5

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	44
Mean	58.55
Std Dev	9.164

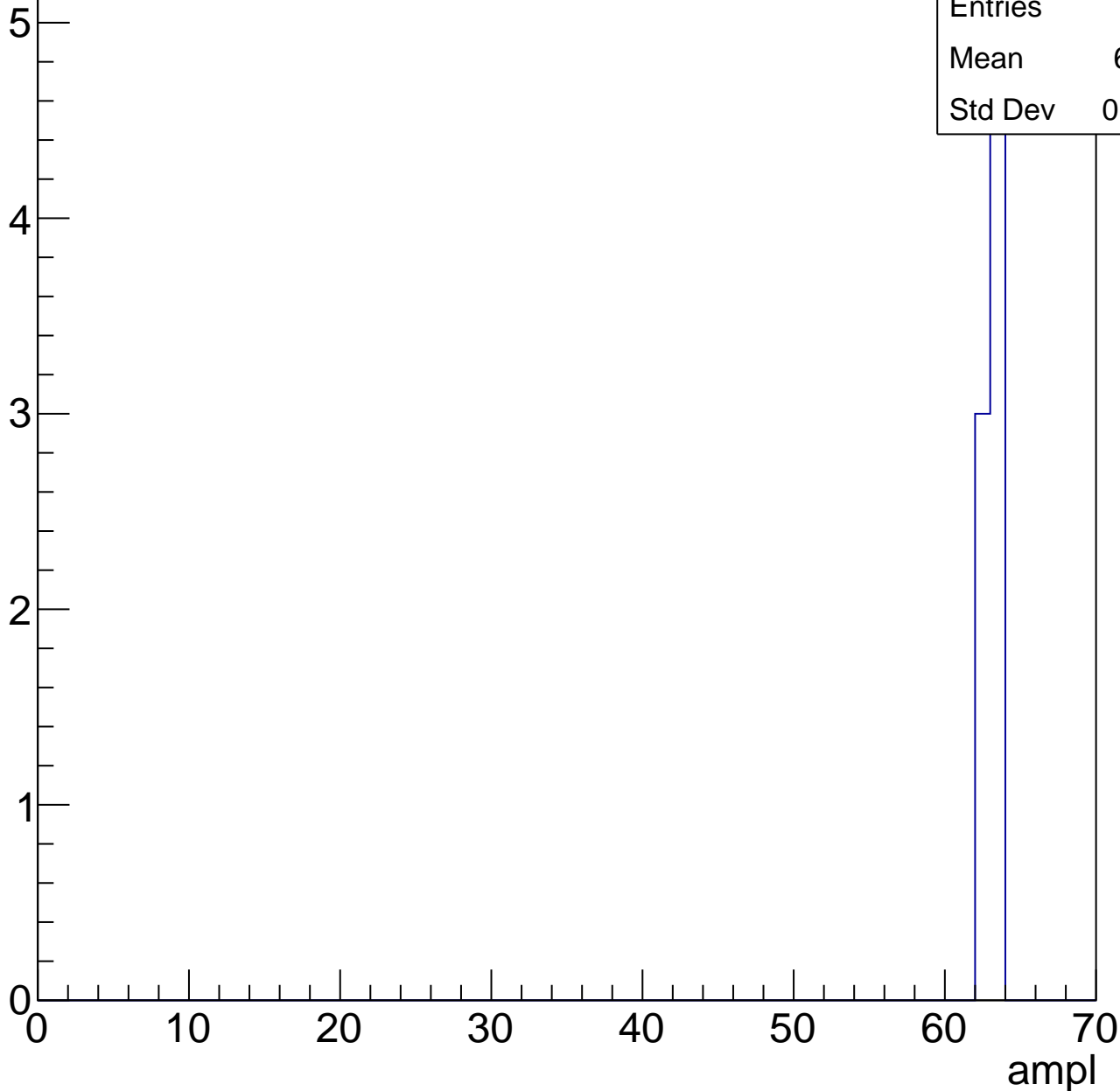


# B0L002S, U2-ch122, adc6

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	8
Mean	62.62
Std Dev	0.4841





# B0L002S, U2-ch122, adc7

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



# B0L002S, U2-ch123, adc0

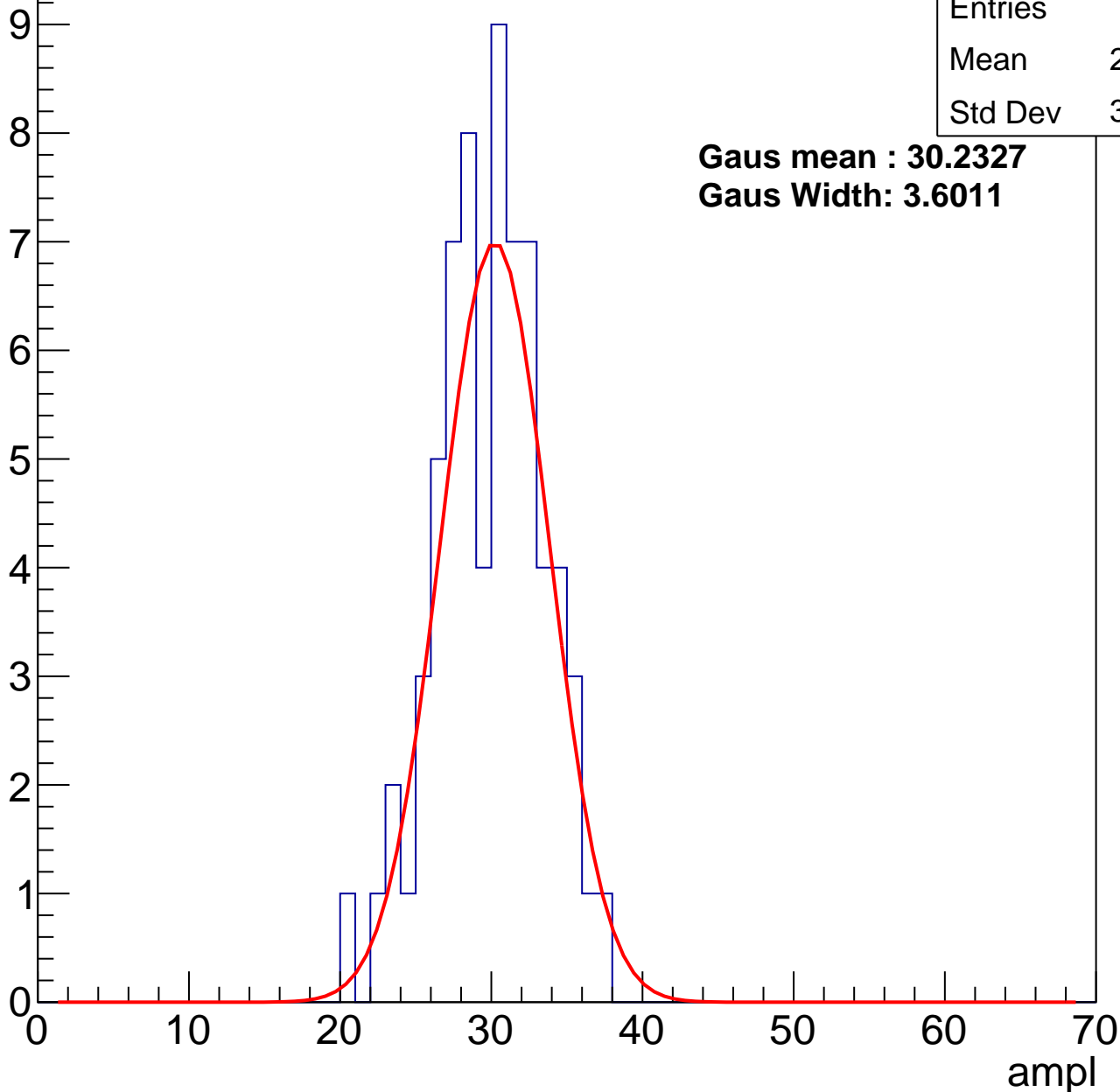
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	68
Mean	29.46
Std Dev	3.487

**Gaus mean : 30.2327**

**Gaus Width: 3.6011**



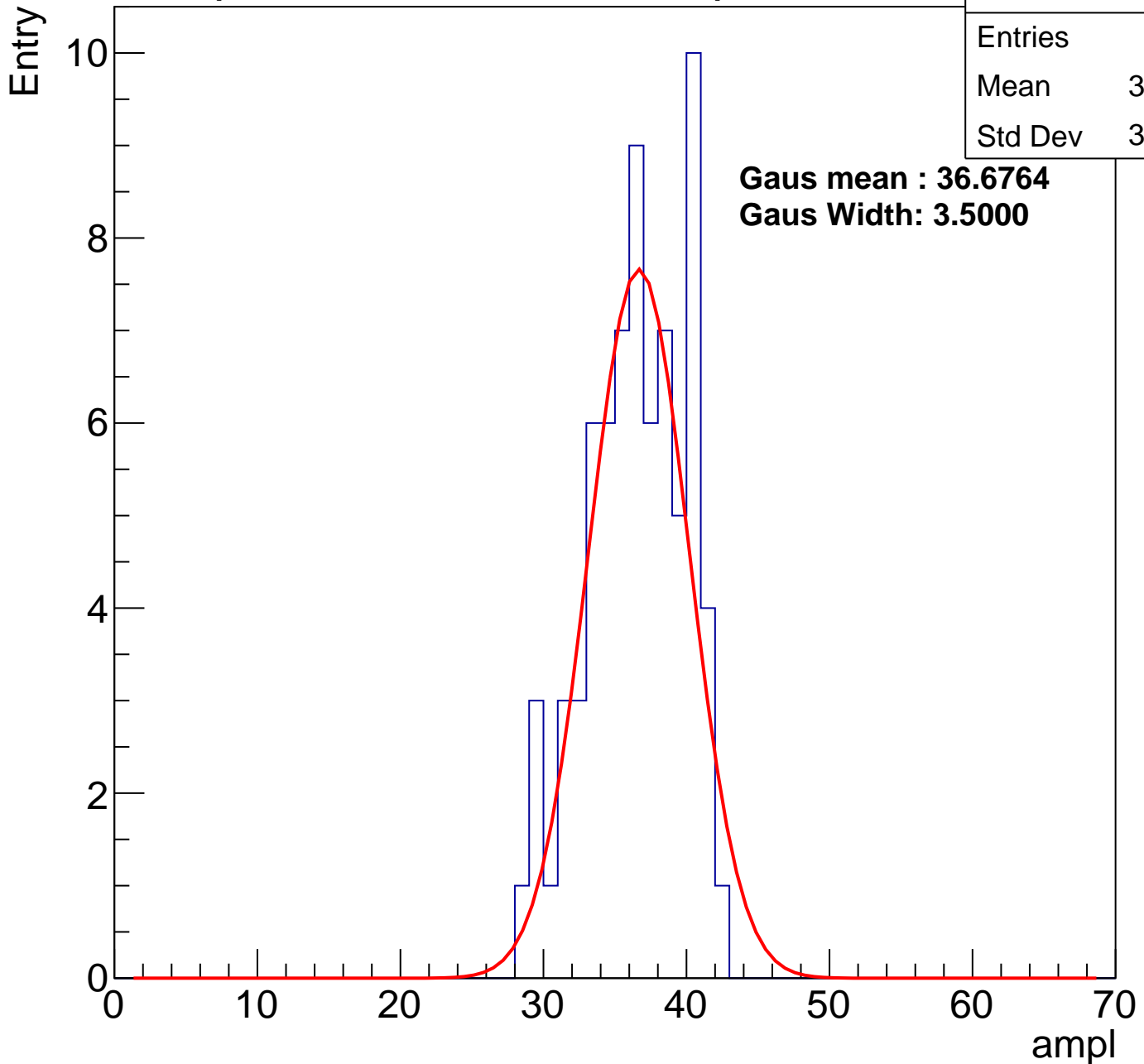
# B0L002S, U2-ch123, adc1

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entries	72
Mean	36.03
Std Dev	3.395

**Gaus mean : 36.6764**

**Gaus Width: 3.5000**



# B0L002S, U2-ch123, adc2

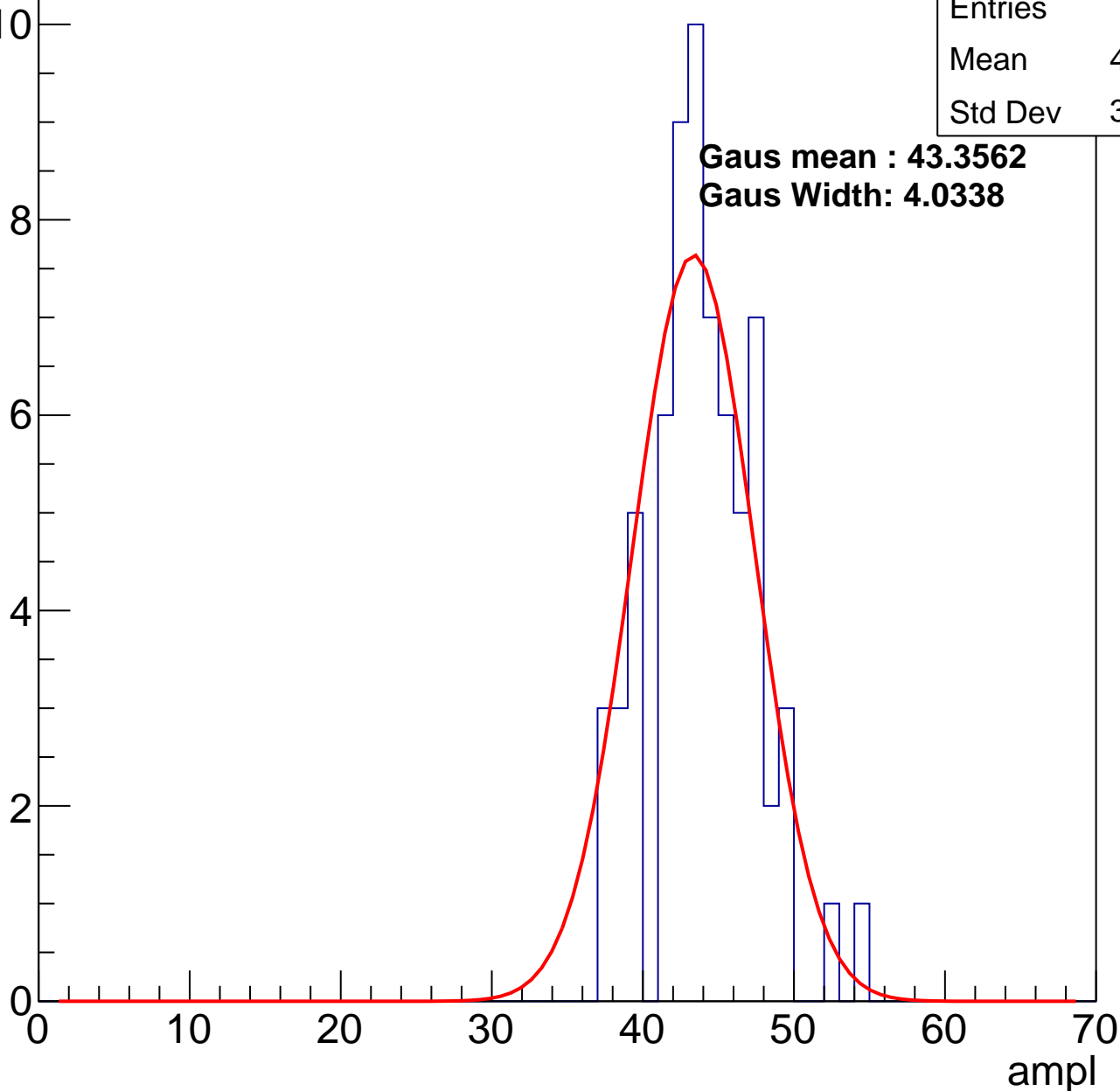
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	68
Mean	43.53
Std Dev	3.483

**Gaus mean : 43.3562**

**Gaus Width: 4.0338**



# B0L002S, U2-ch123, adc3

calib\_packv5\_042523\_0143.root, FC#8, port C1

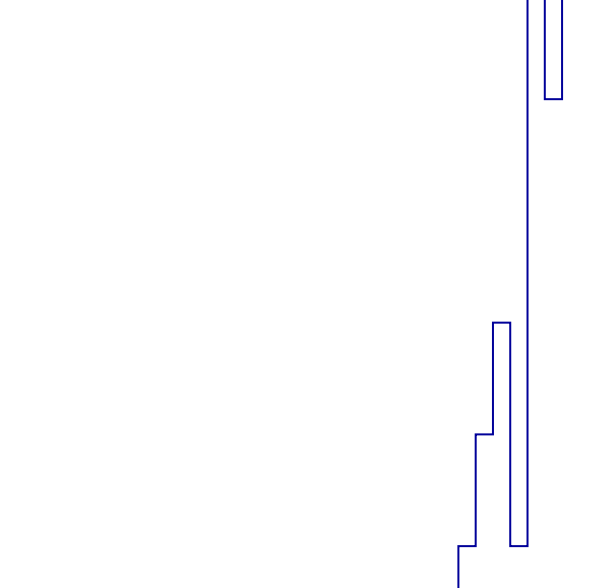
Entries	80
Mean	50.54
Std Dev	3.398

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

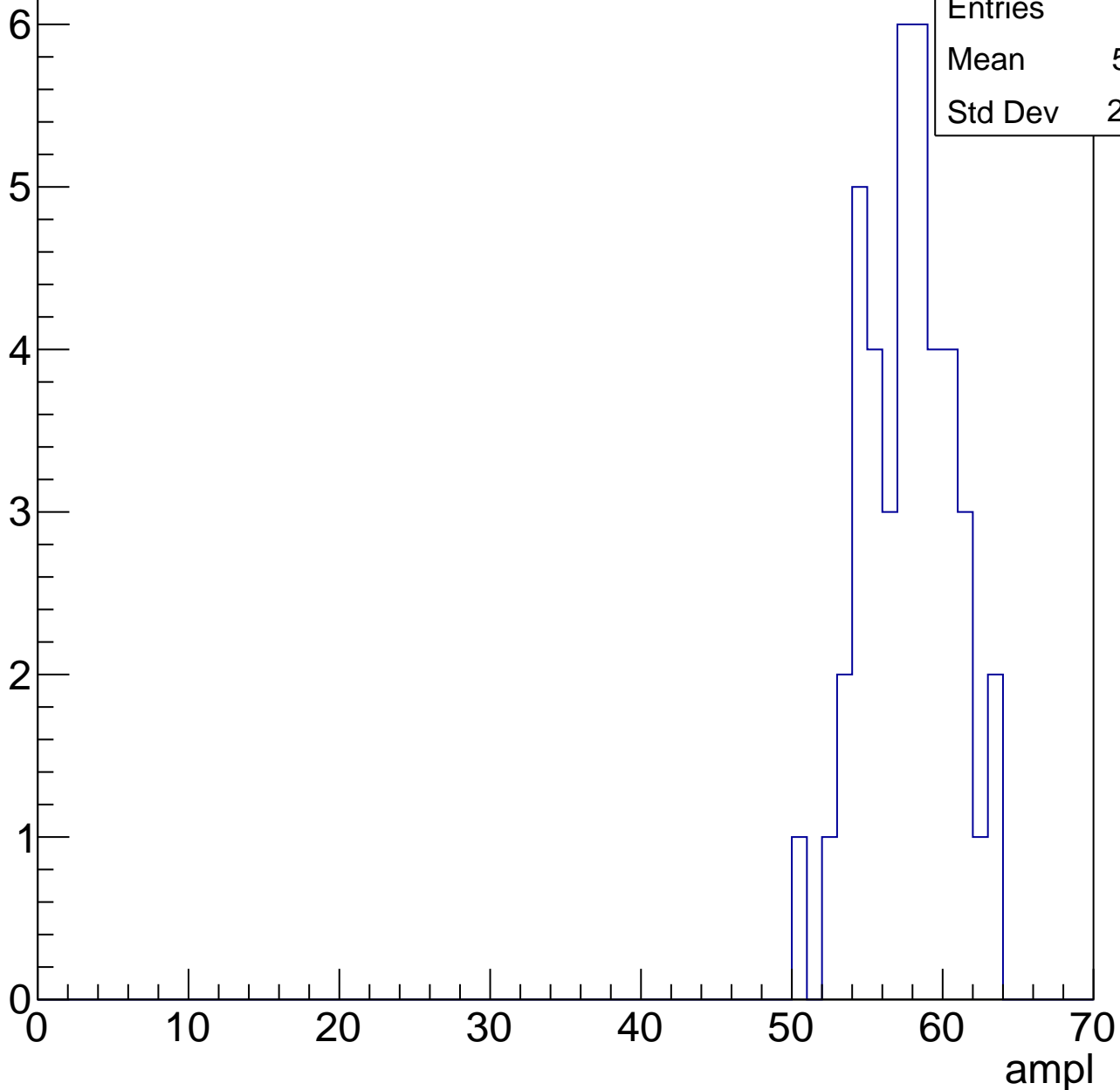


# B0L002S, U2-ch123, adc4

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	42
Mean	57.21
Std Dev	2.972

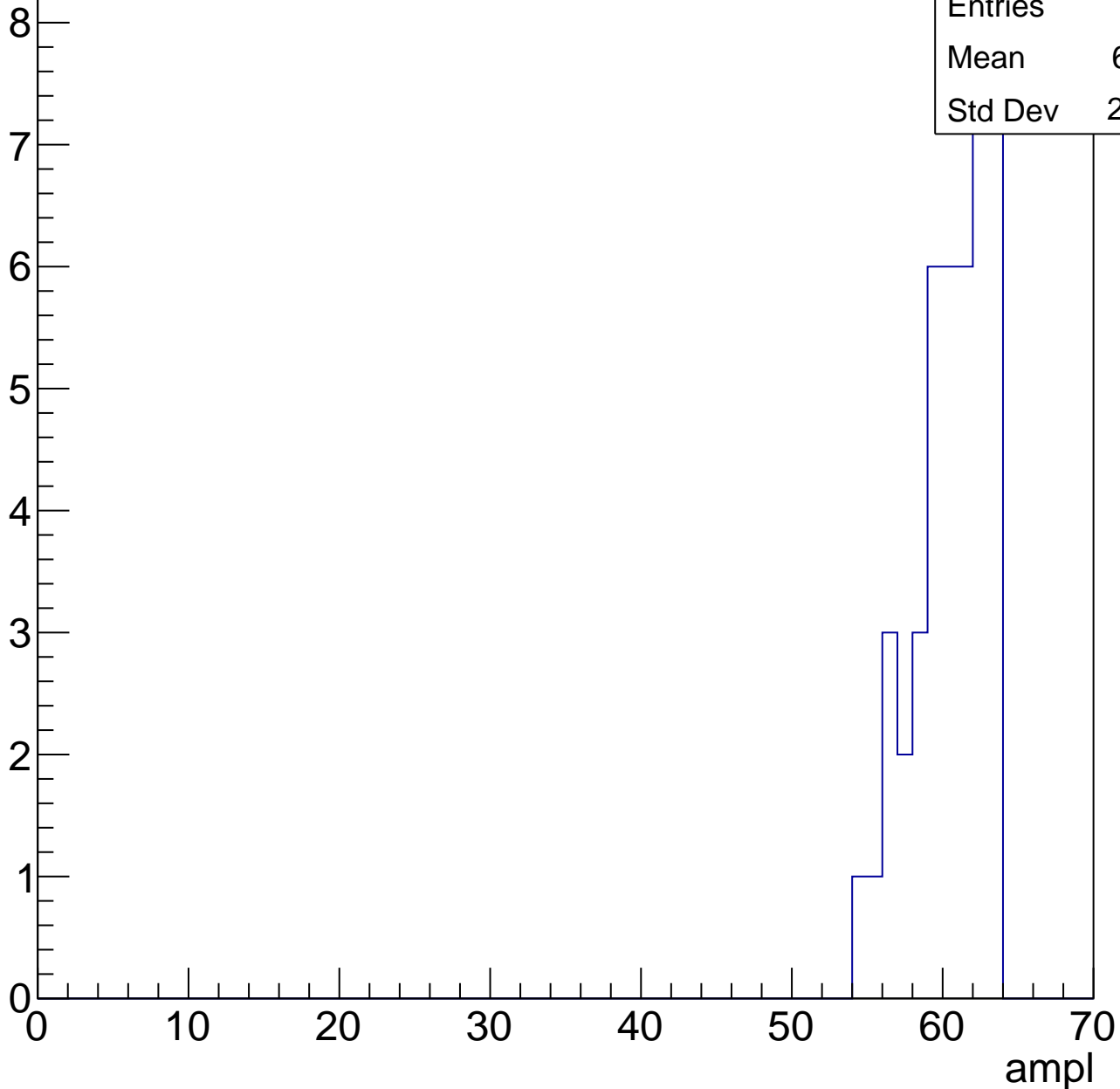


# B0L002S, U2-ch123, adc5

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	44
Mean	60.11
Std Dev	2.405



# B0L002S, U2-ch123, adc6

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

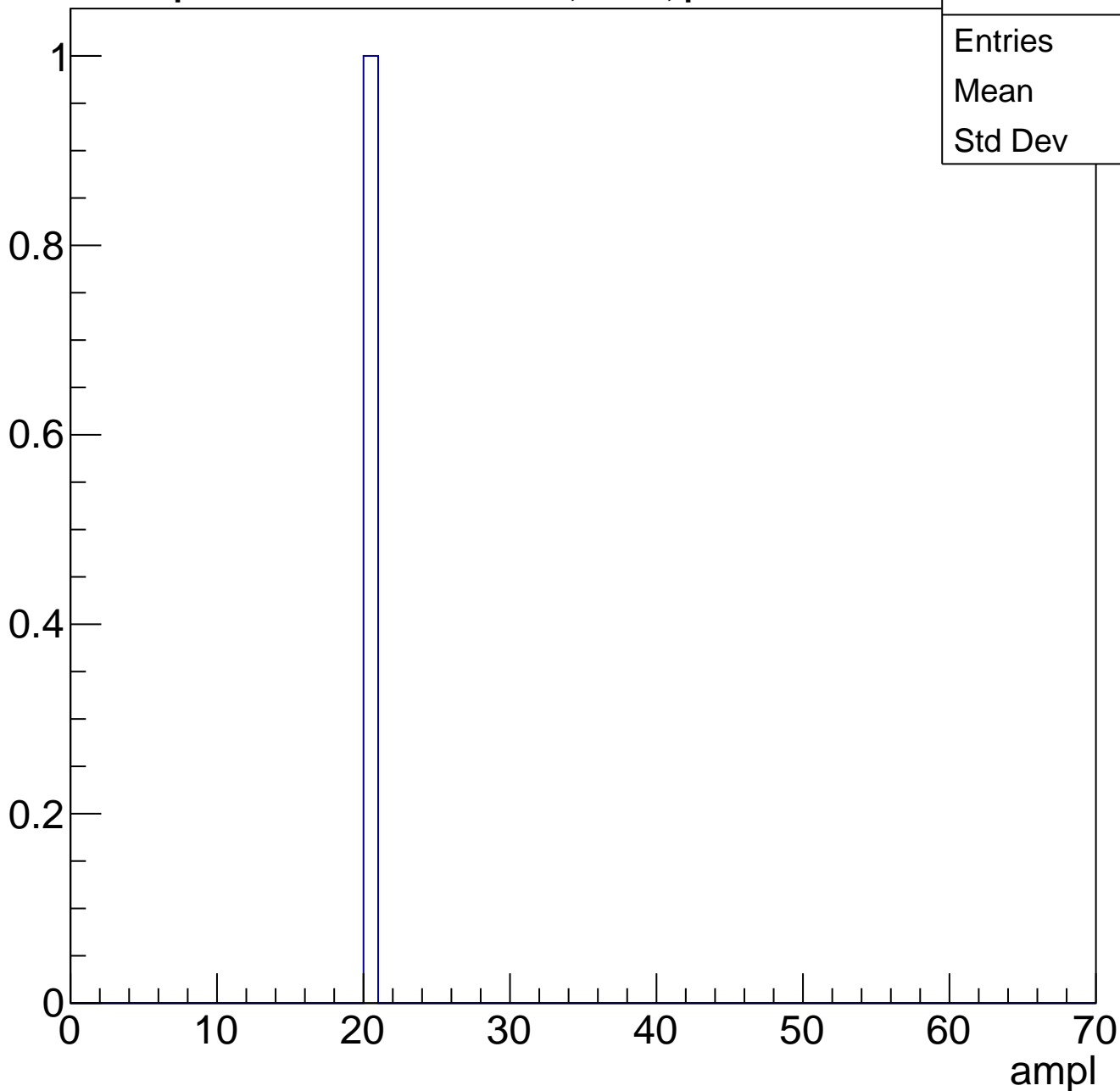




# B0L002S, U2-ch123, adc7

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



Entries	1
Mean	20
Std Dev	0

# B0L002S, U2-ch124, adc0

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entries	73
Mean	29.36
Std Dev	4.866

**Gaus mean : 30.5433**

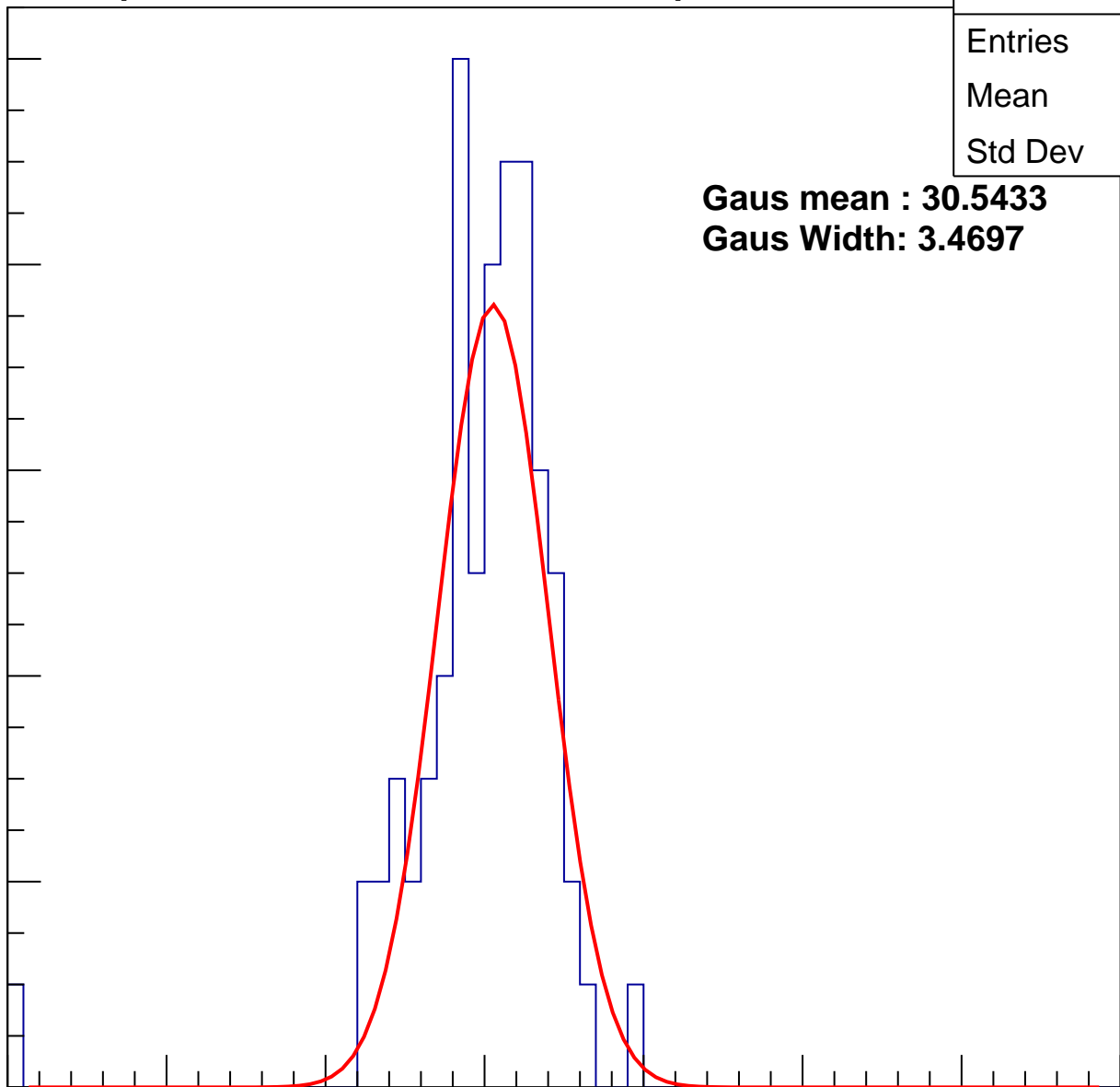
**Gaus Width: 3.4697**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L002S, U2-ch124, adc1

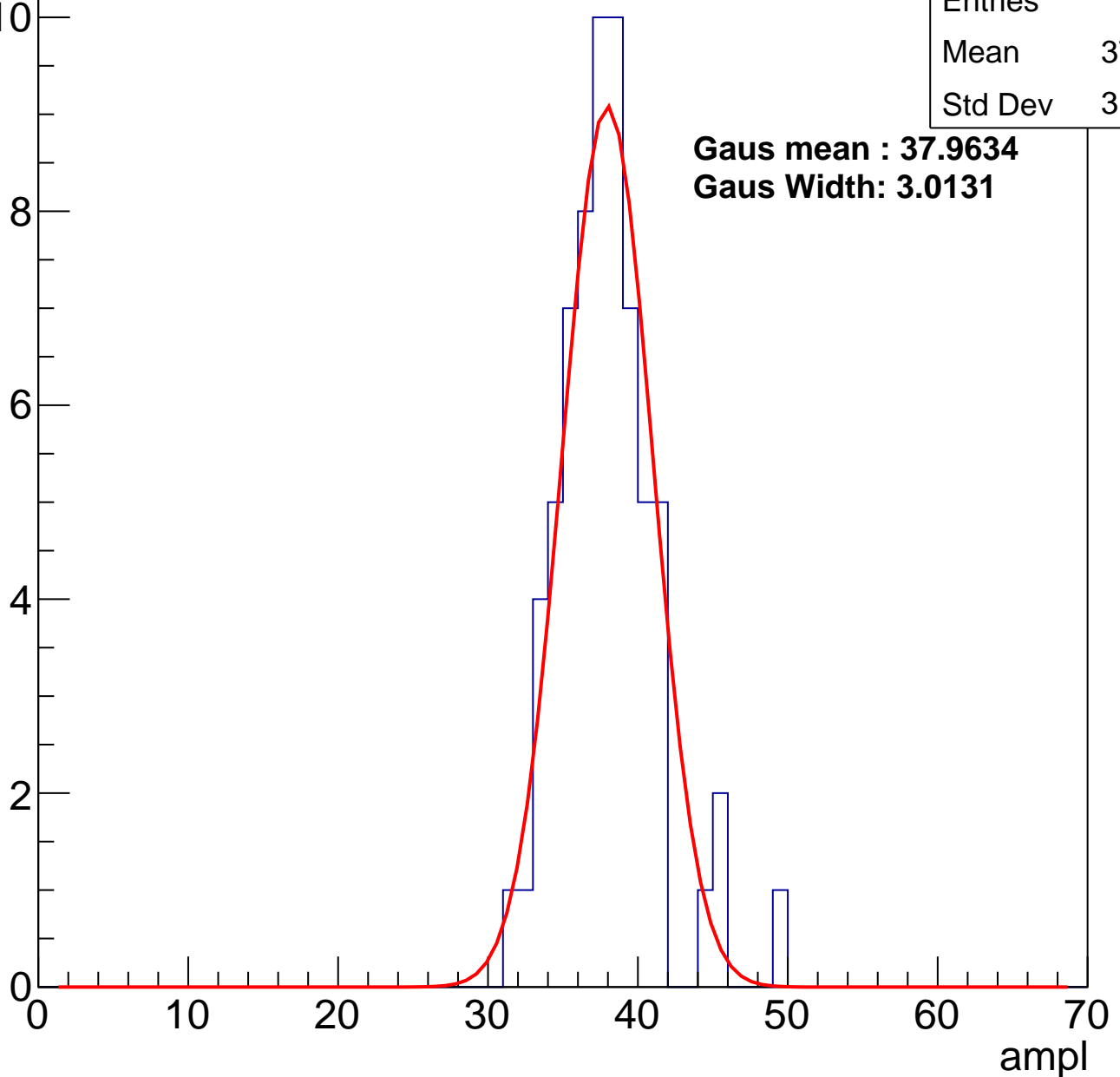
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	67
Mean	37.45
Std Dev	3.178

**Gaus mean : 37.9634**

**Gaus Width: 3.0131**



# B0L002S, U2-ch124, adc2

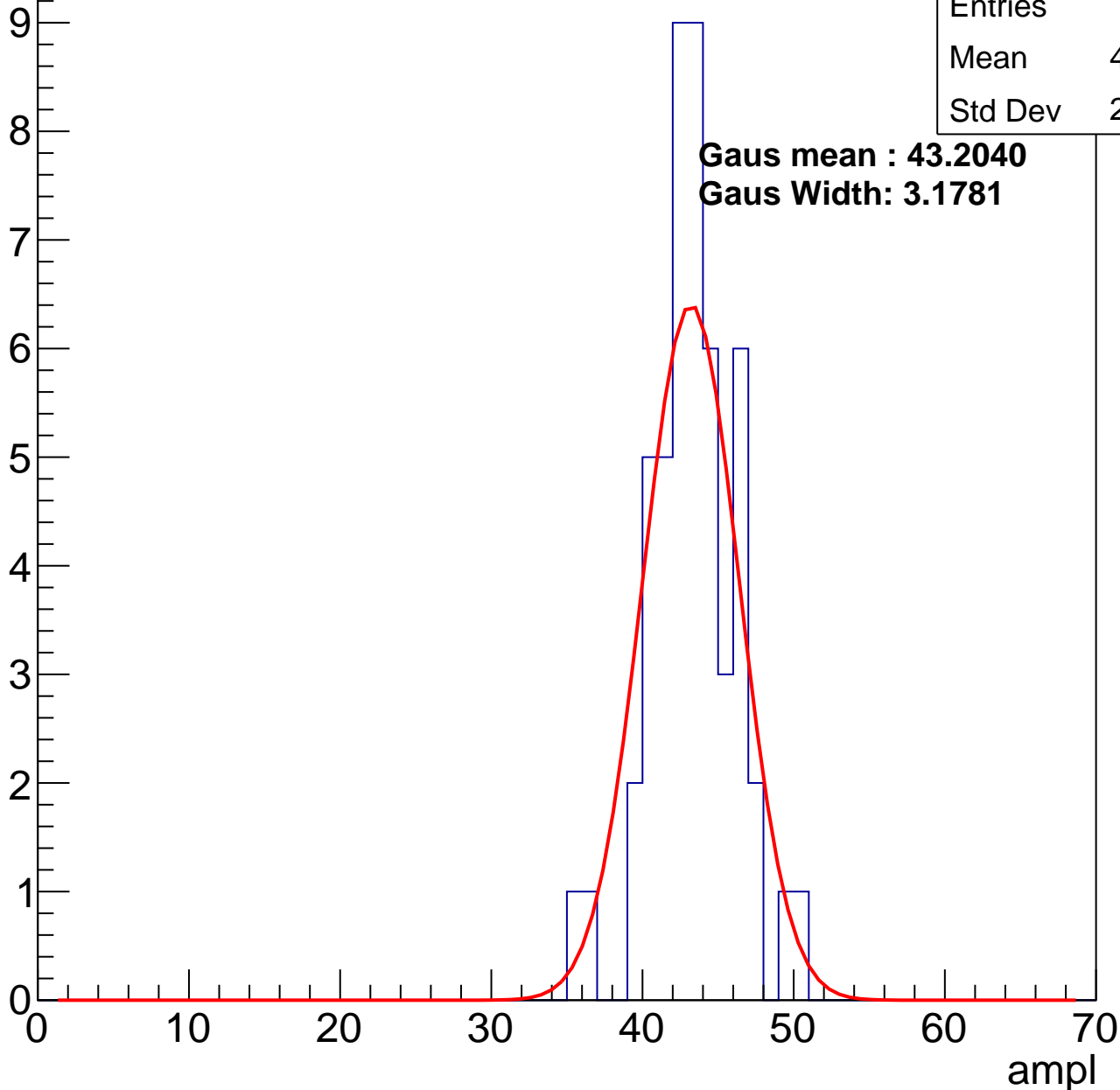
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	51
Mean	42.88
Std Dev	2.826

**Gaus mean : 43.2040**

**Gaus Width: 3.1781**



# B0L002S, U2-ch124, adc3

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entries	78
Mean	49.68
Std Dev	3.572

Entry

10

8

6

4

2

0

0

10

20

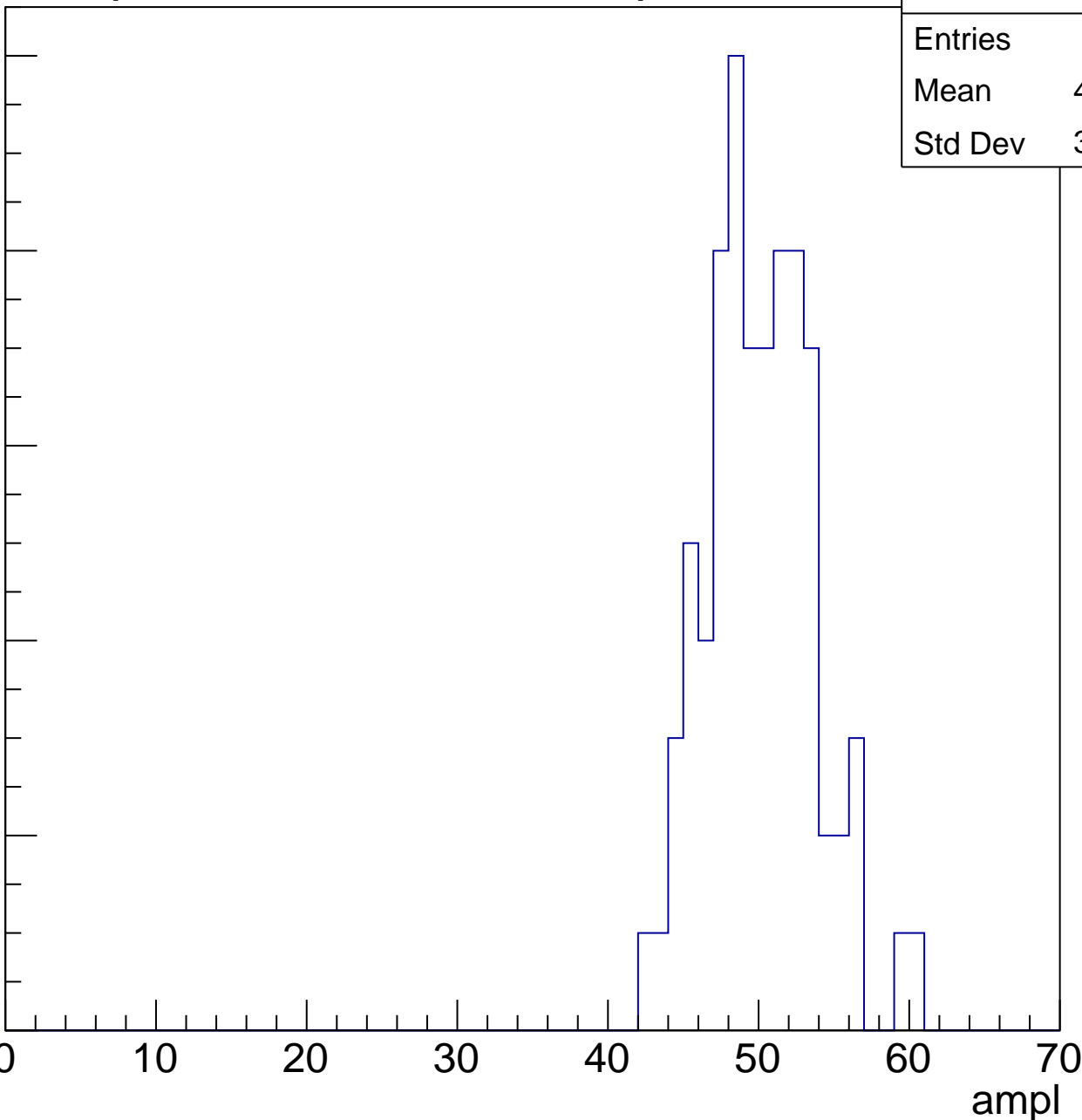
30

40

50

60

ampl

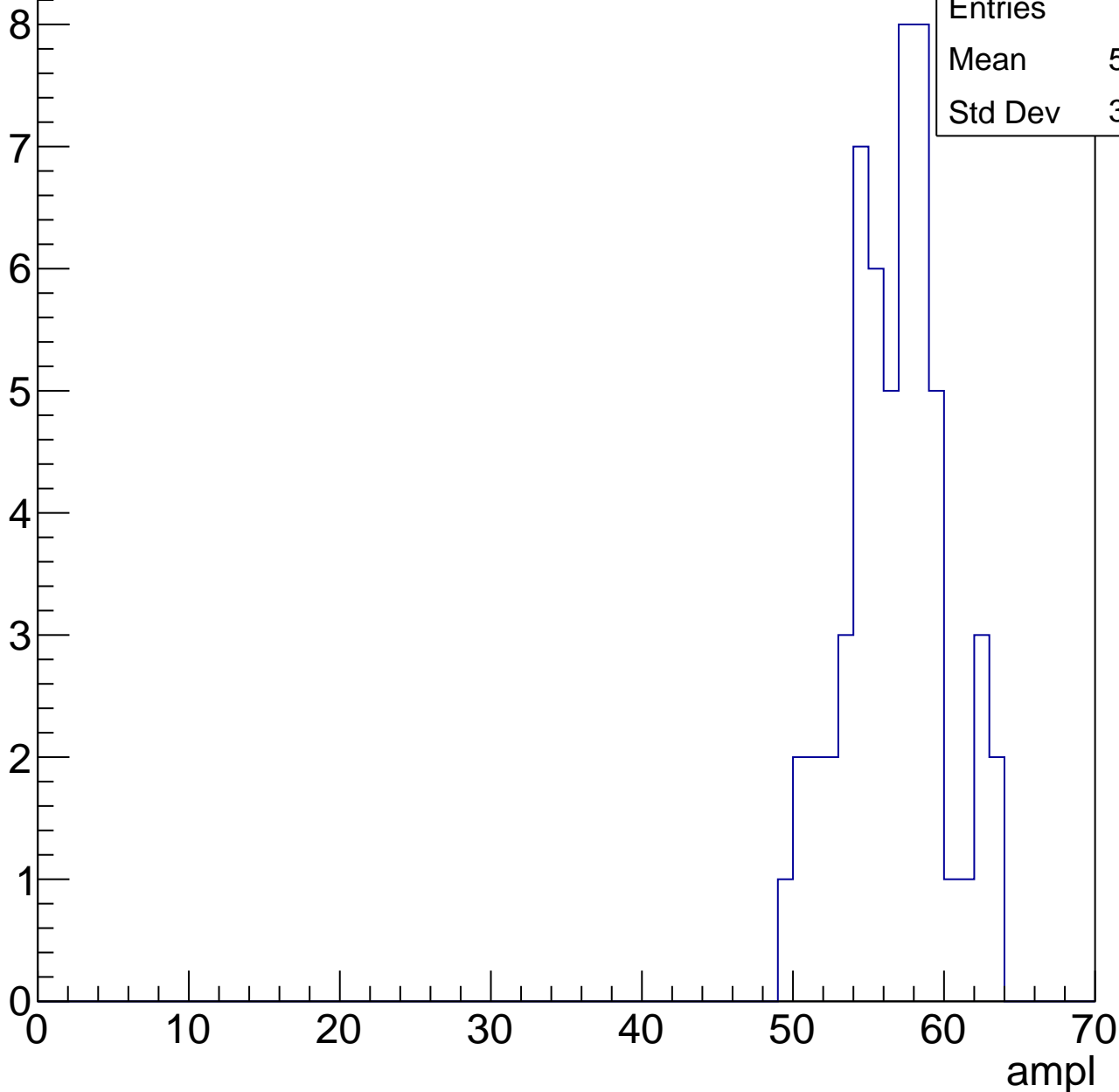


# B0L002S, U2-ch124, adc4

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	56
Mean	56.25
Std Dev	3.253



# B0L002S, U2-ch124, adc5

calib\_packv5\_042523\_0143.root, FC#8, port C1

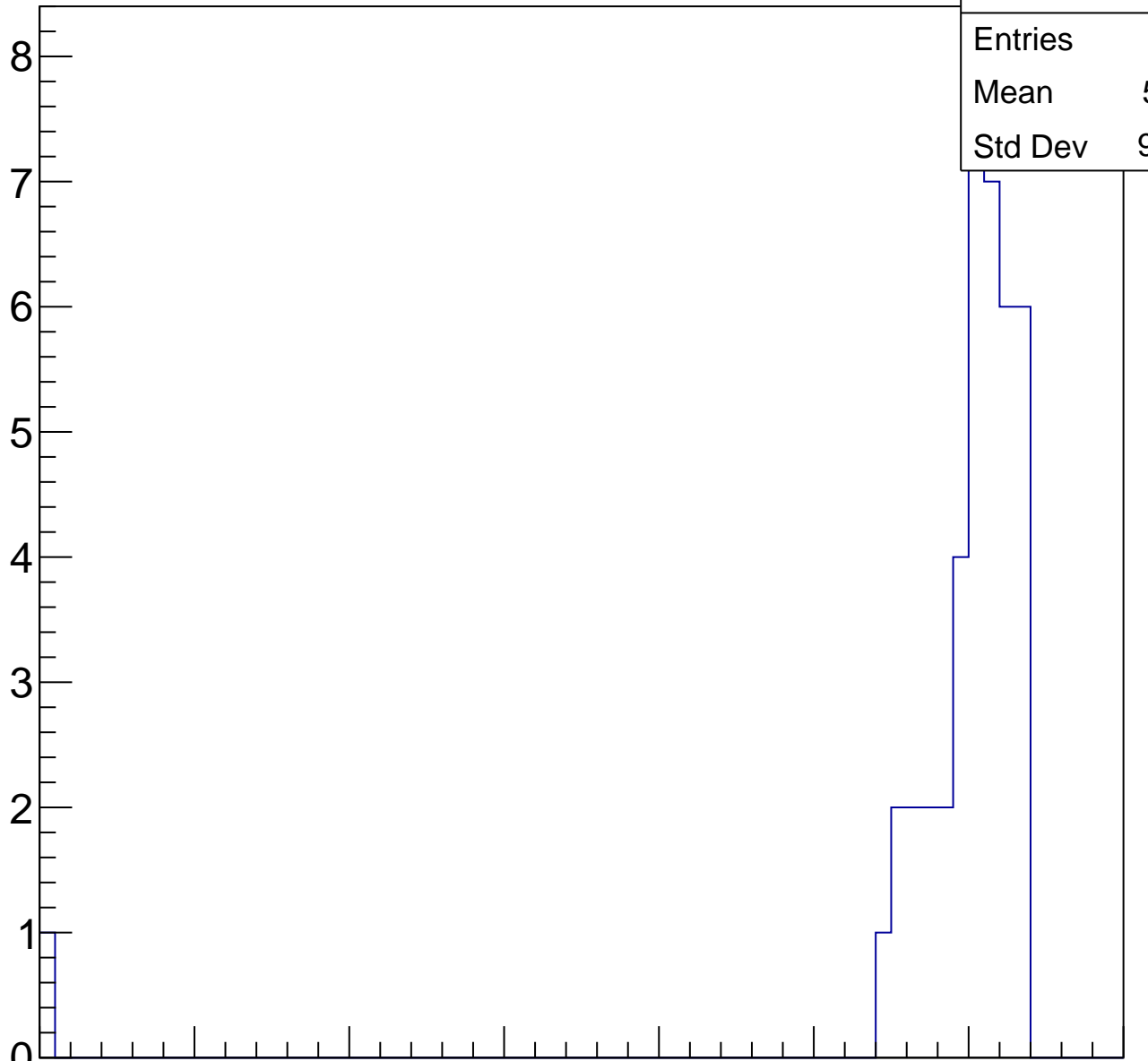
Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	41
Mean	58.51
Std Dev	9.554

ampl

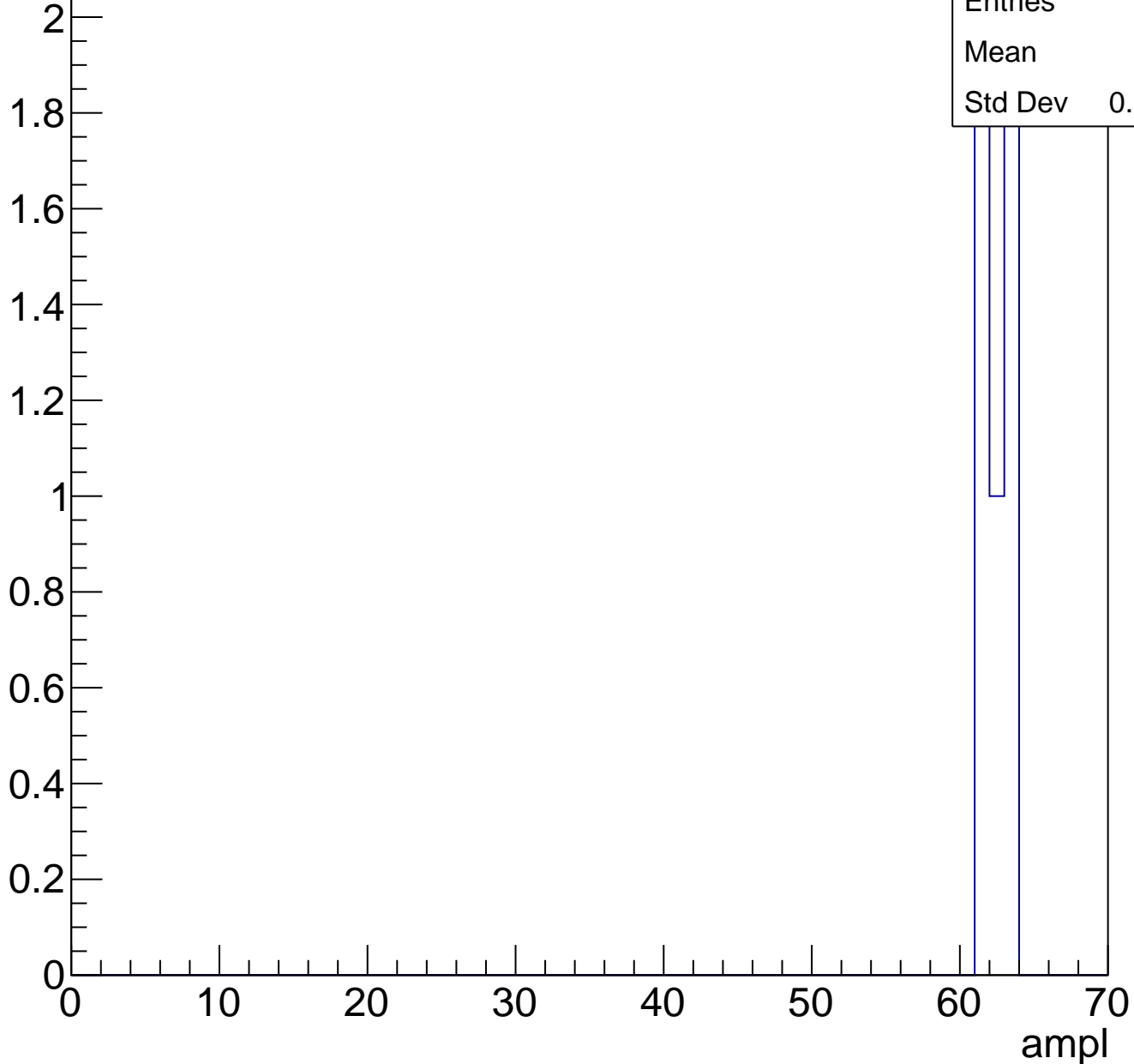
0 10 20 30 40 50 60 70



# B0L002S, U2-ch124, adc6

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry





# B0L002S, U2-ch124, adc7

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



# B0L002S, U2-ch125, adc0

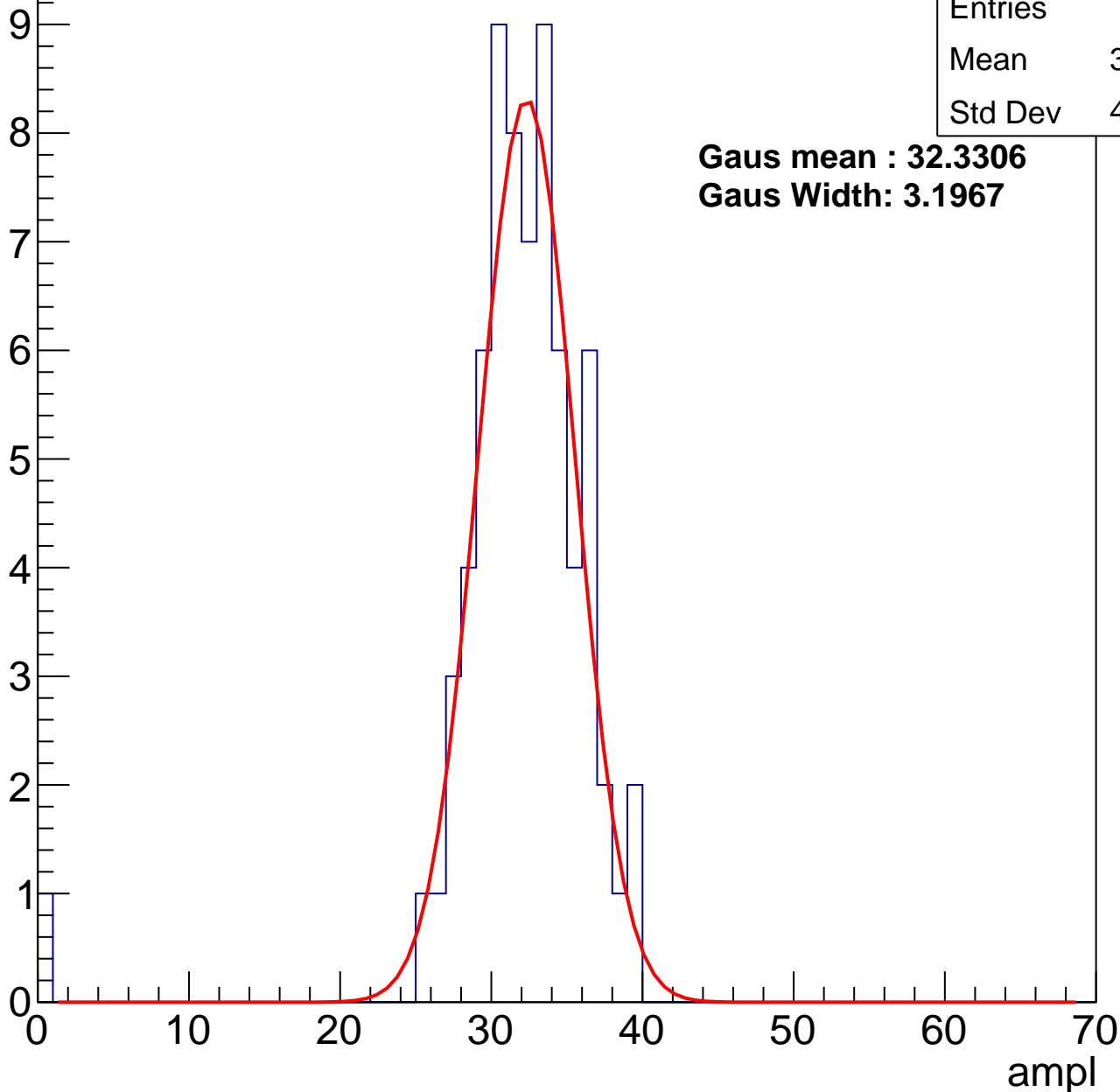
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	70
Mean	31.53
Std Dev	4.898

**Gaus mean : 32.3306**

**Gaus Width: 3.1967**



# B0L002S, U2-ch125, adc1

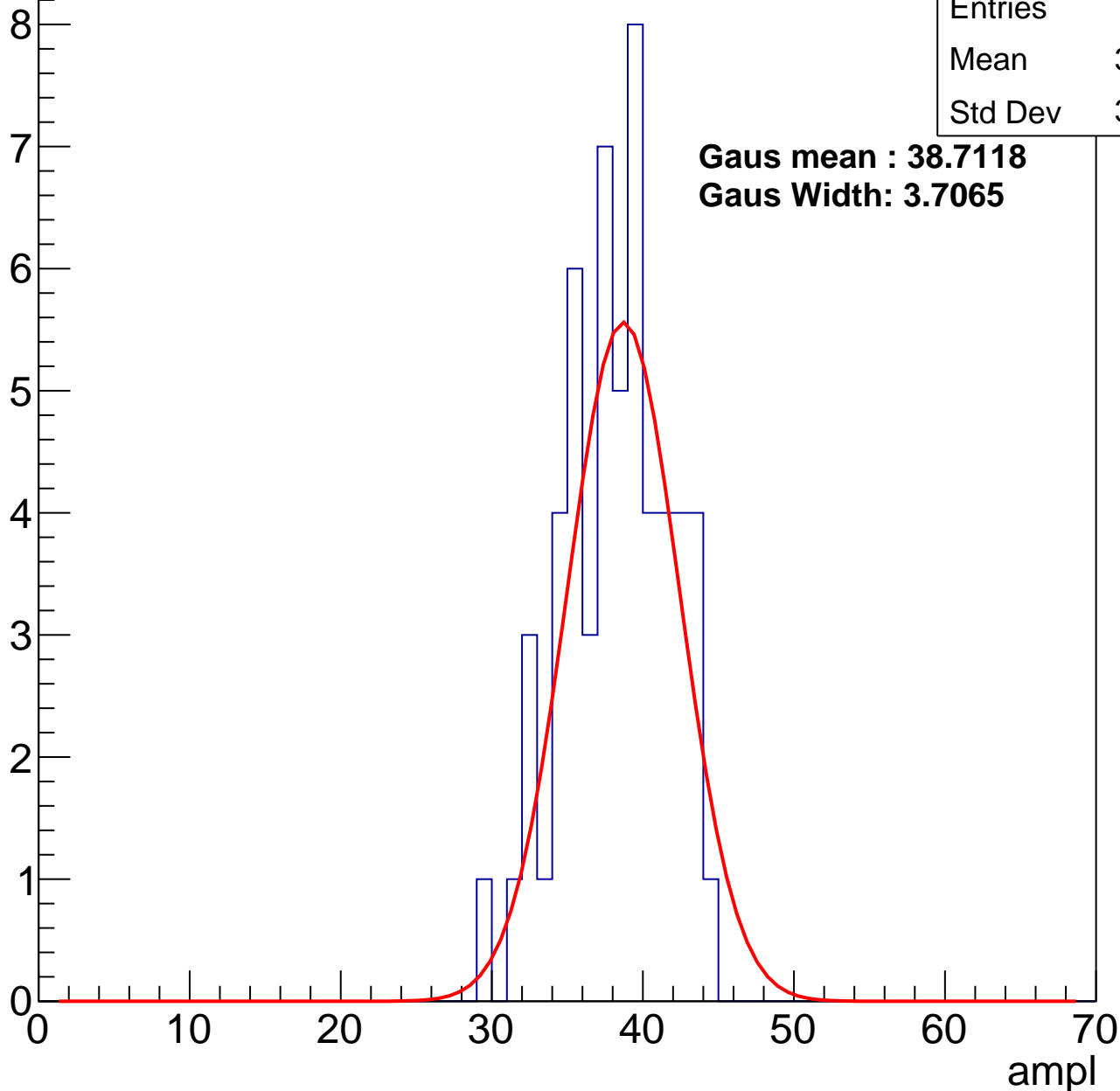
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	56
Mean	37.71
Std Dev	3.421

**Gaus mean : 38.7118**

**Gaus Width: 3.7065**



# B0L002S, U2-ch125, adc2

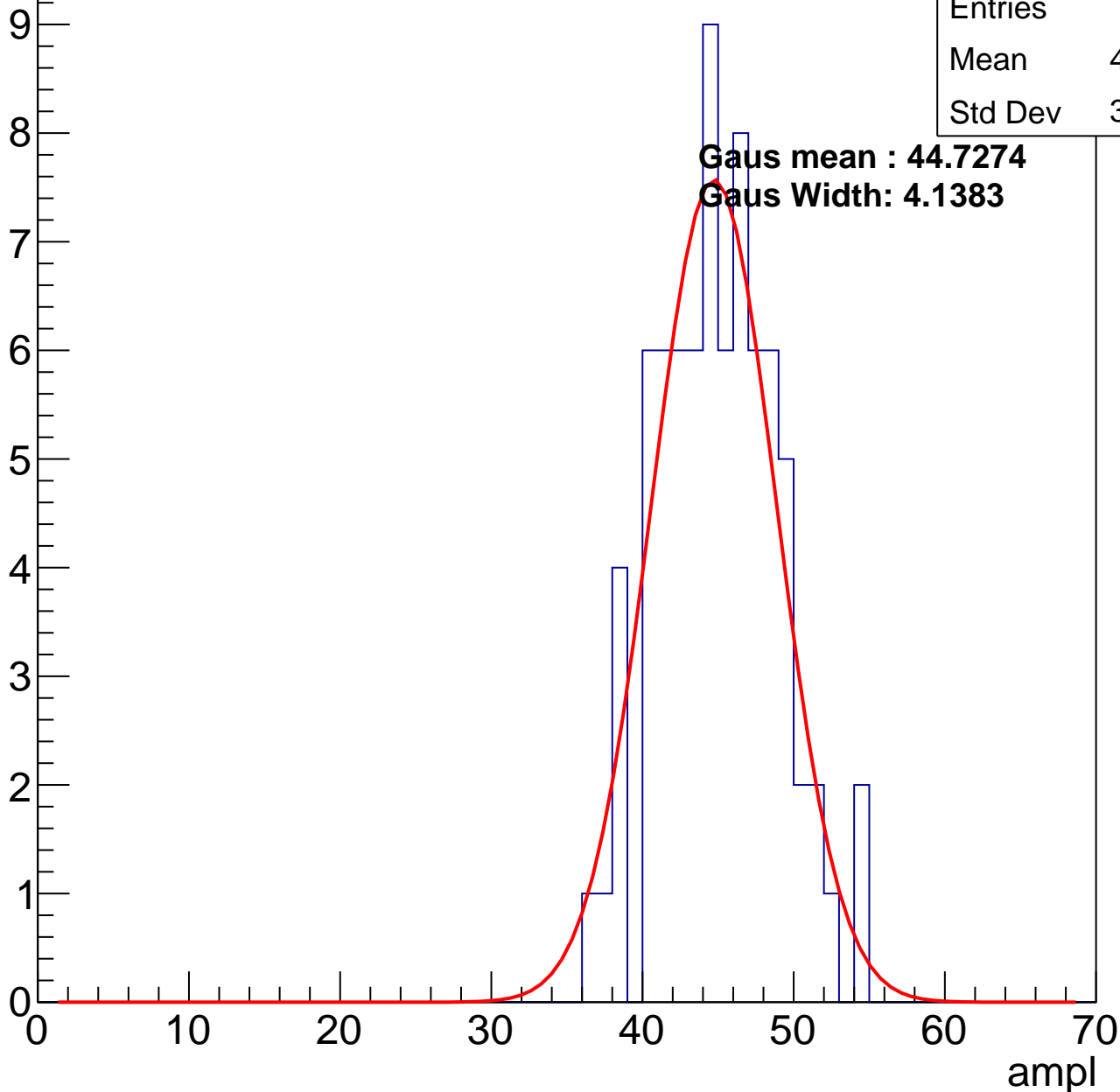
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	77
Mean	44.57
Std Dev	3.879

**Gaus mean : 44.7274**

**Gaus Width: 4.1383**

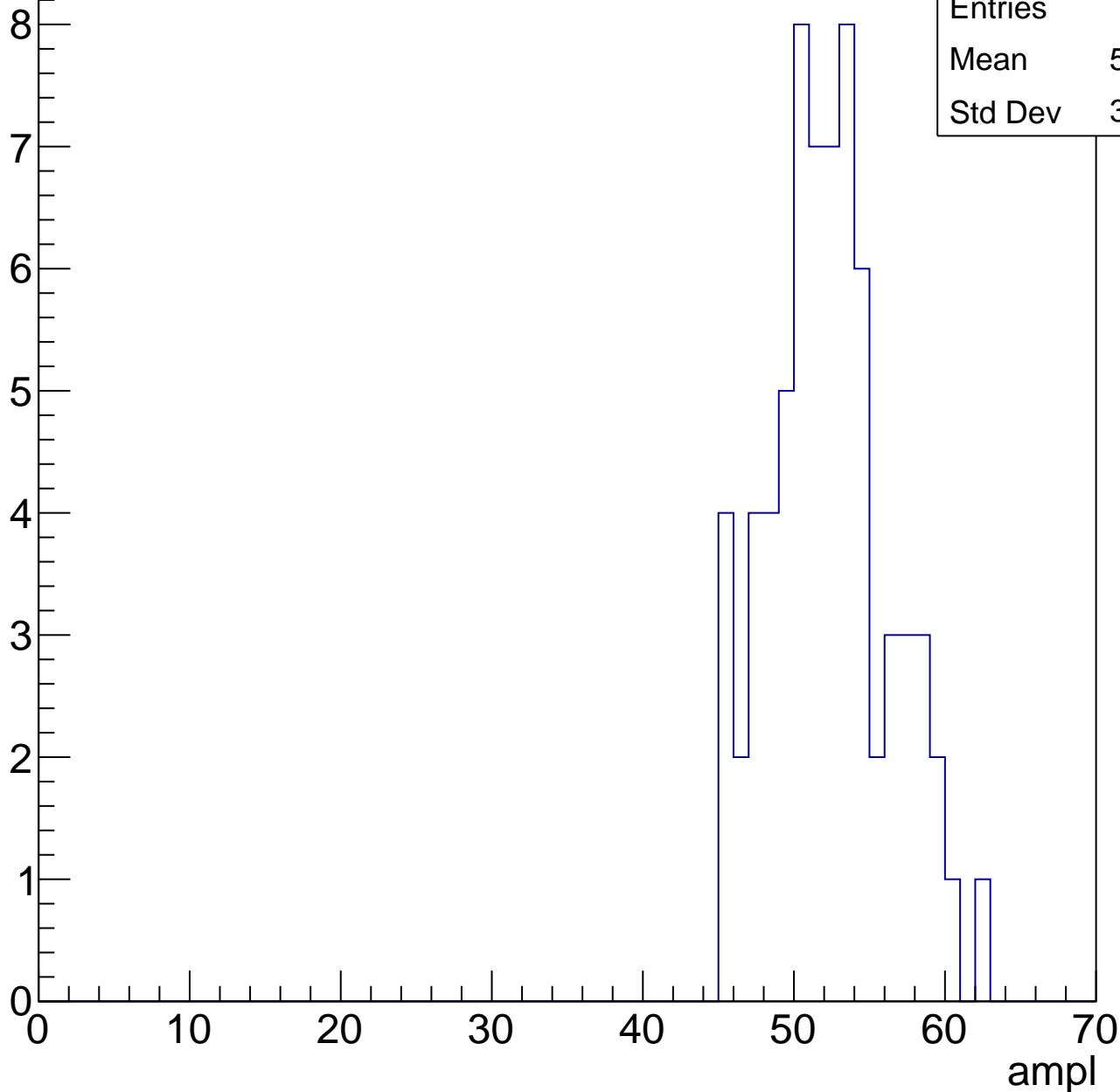


# B0L002S, U2-ch125, adc3

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

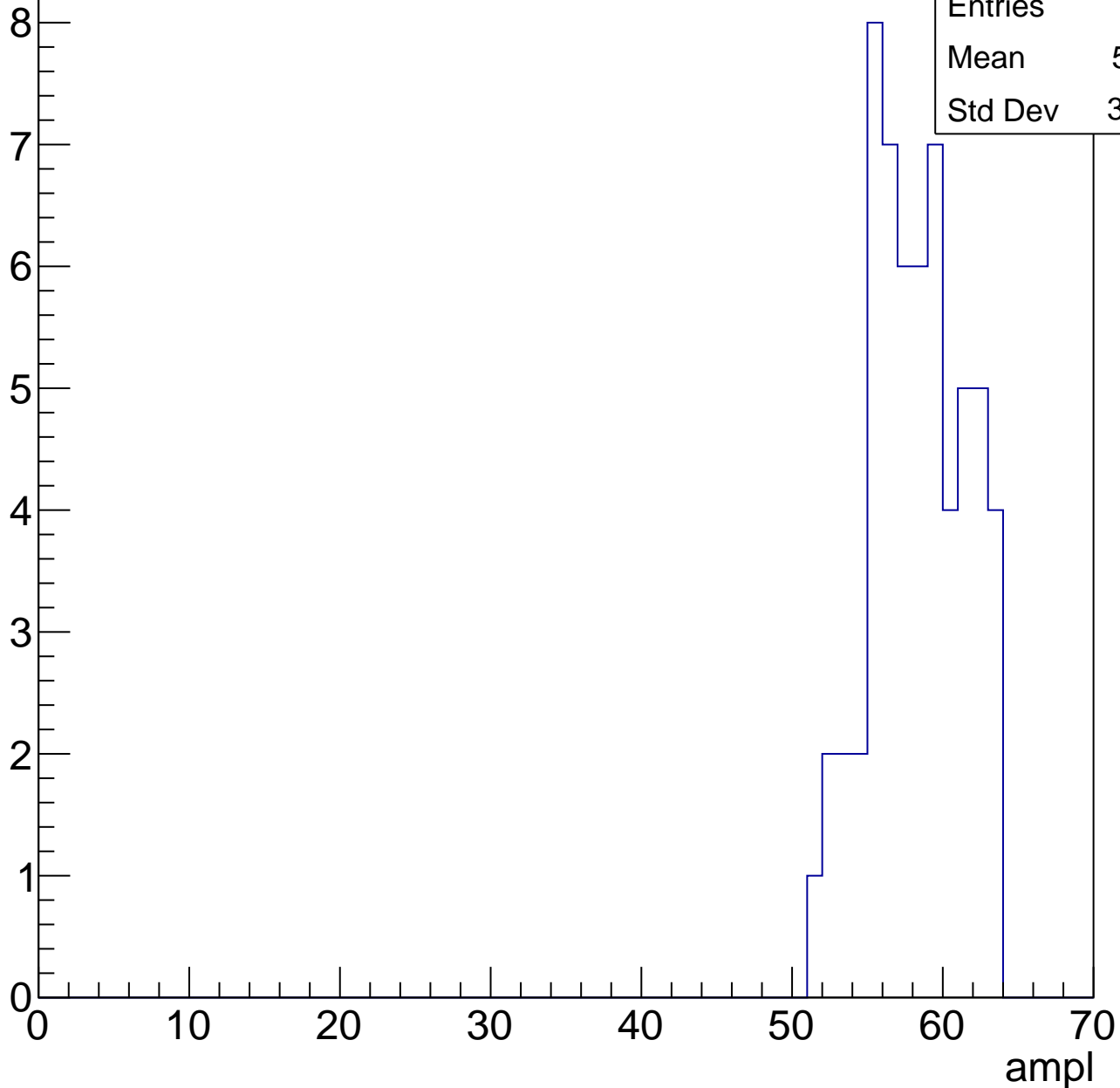
Entries	70
Mean	51.84
Std Dev	3.886



# B0L002S, U2-ch125, adc4

calib\_packv5\_042523\_0143.root, FC#8, port C1

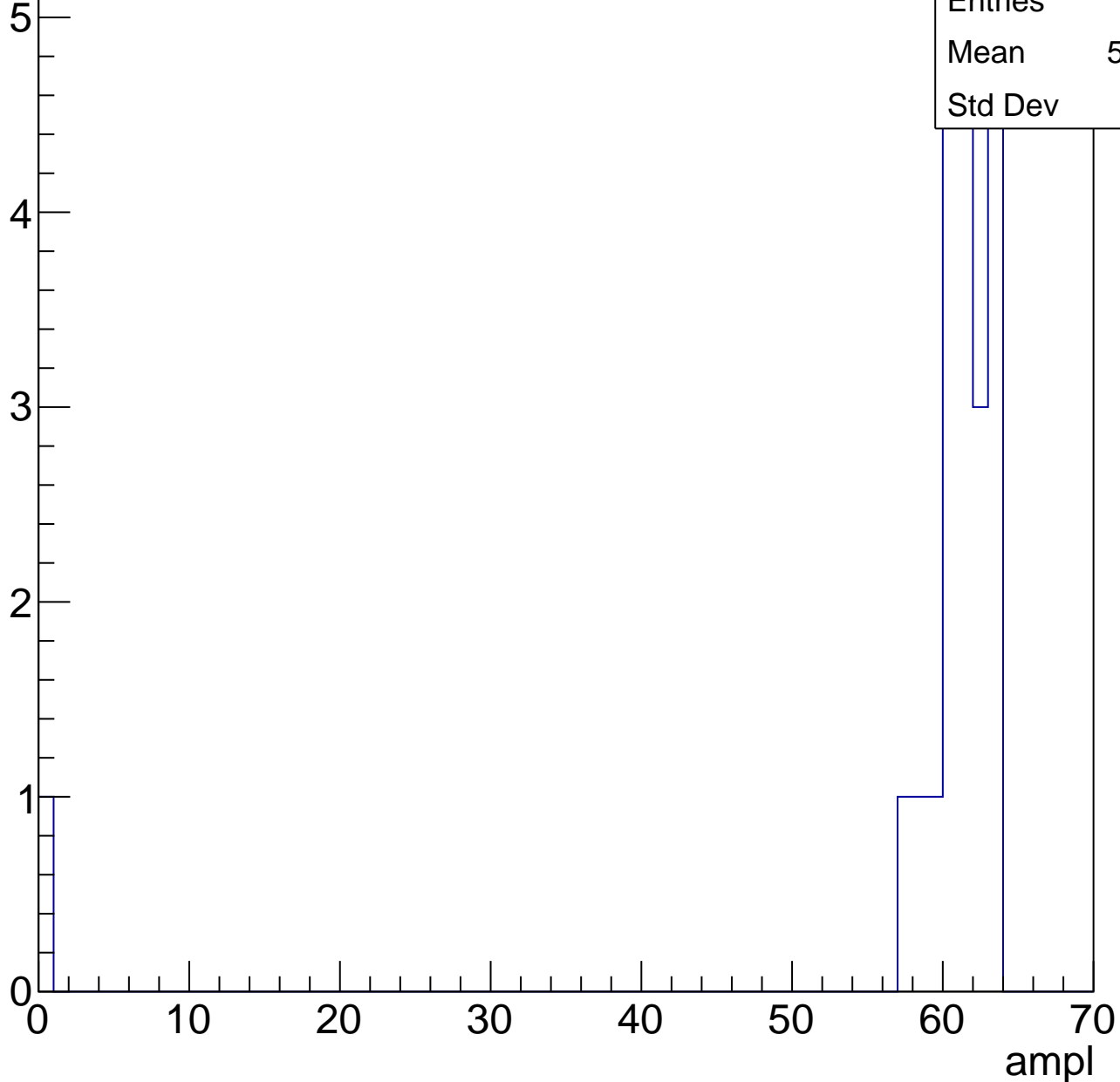
Entry



# B0L002S, U2-ch125, adc5

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



# B0L002S, U2-ch125, adc6

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry





# B0L002S, U2-ch125, adc7

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



# B0L002S, U2-ch126, adc0

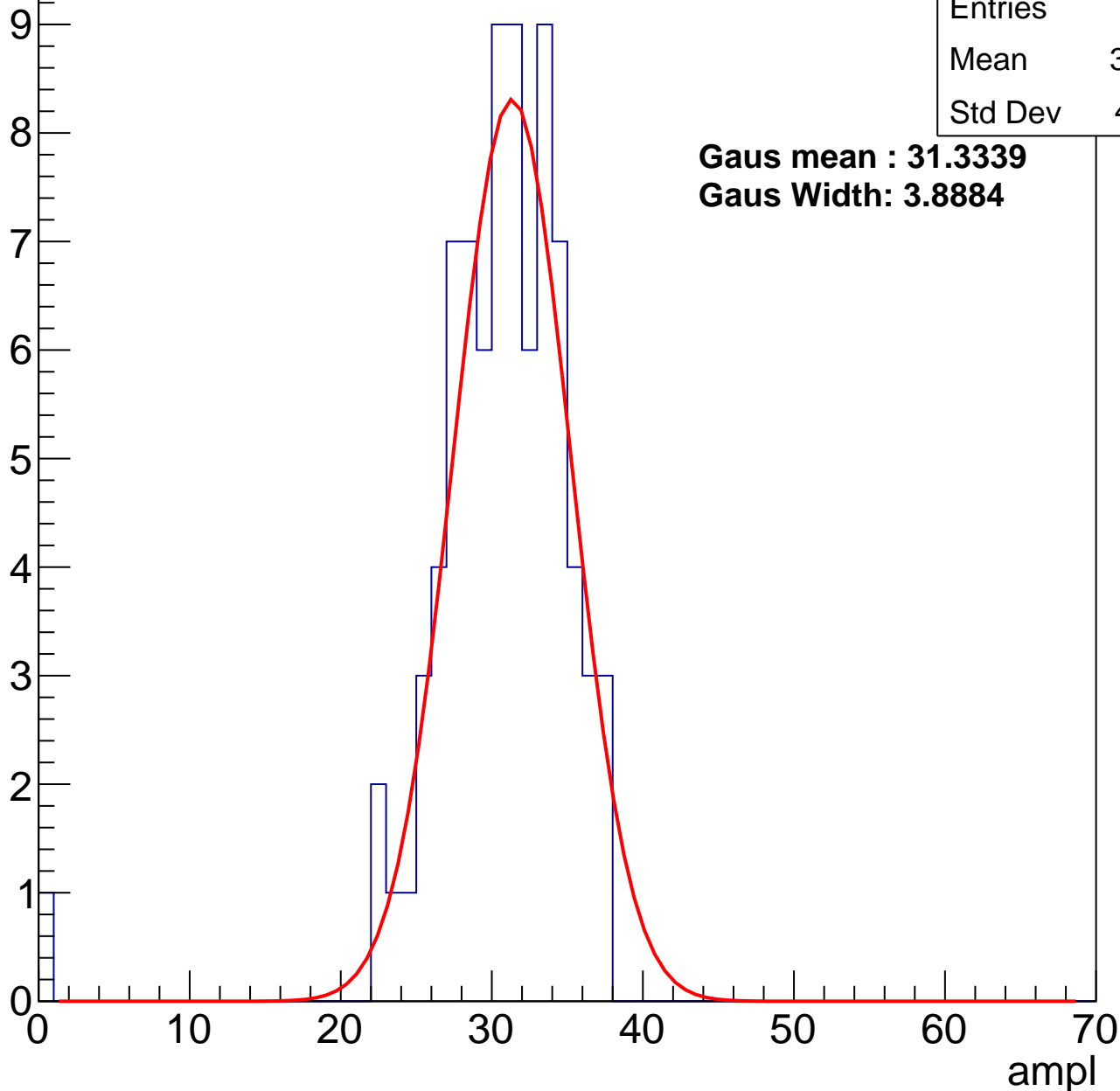
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	82
Mean	30.05
Std Dev	4.851

**Gaus mean : 31.3339**

**Gaus Width: 3.8884**



# B0L002S, U2-ch126, adc1

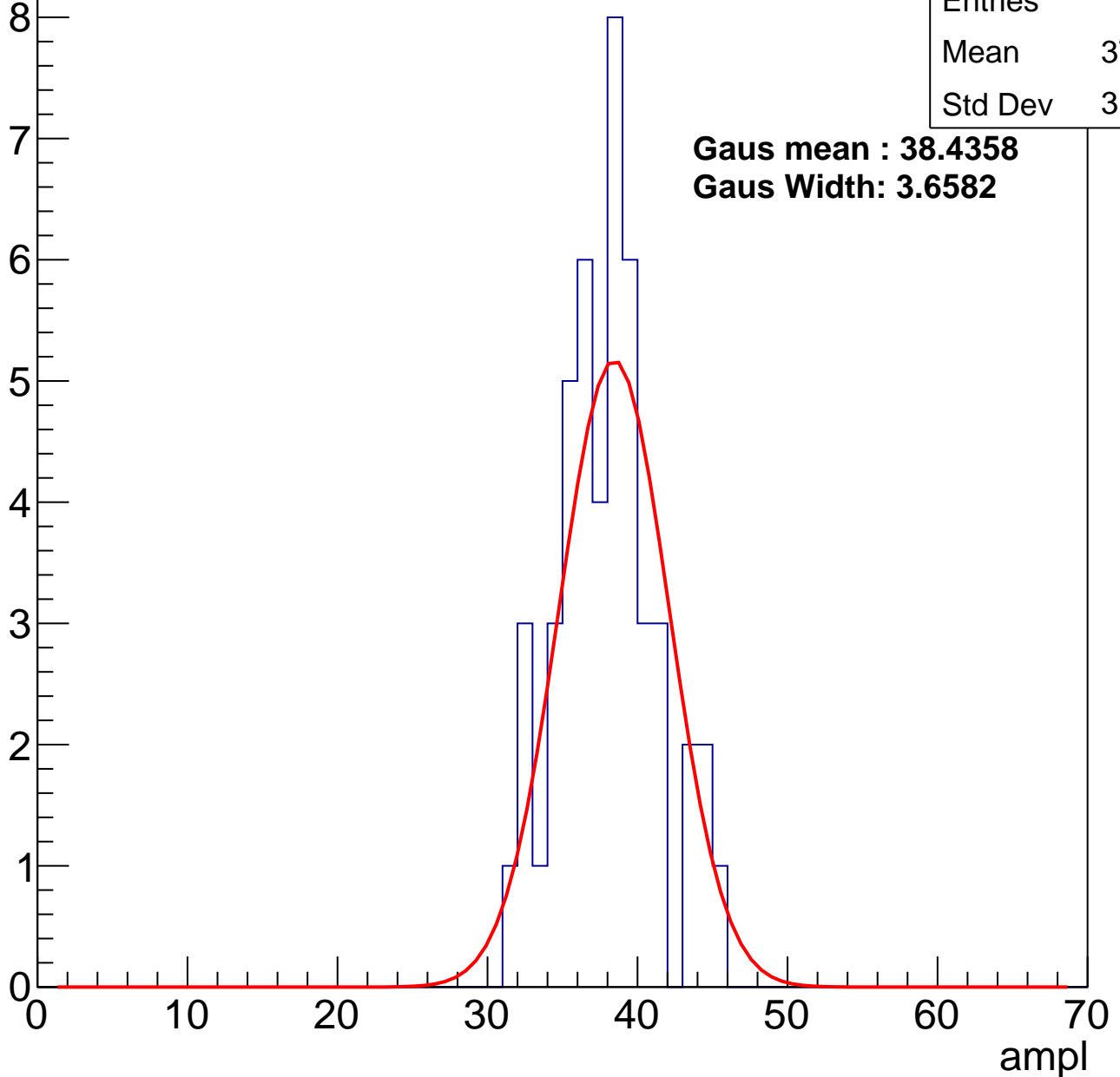
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	48
Mean	37.52
Std Dev	3.253

**Gaus mean : 38.4358**

**Gaus Width: 3.6582**



# B0L002S, U2-ch126, adc2

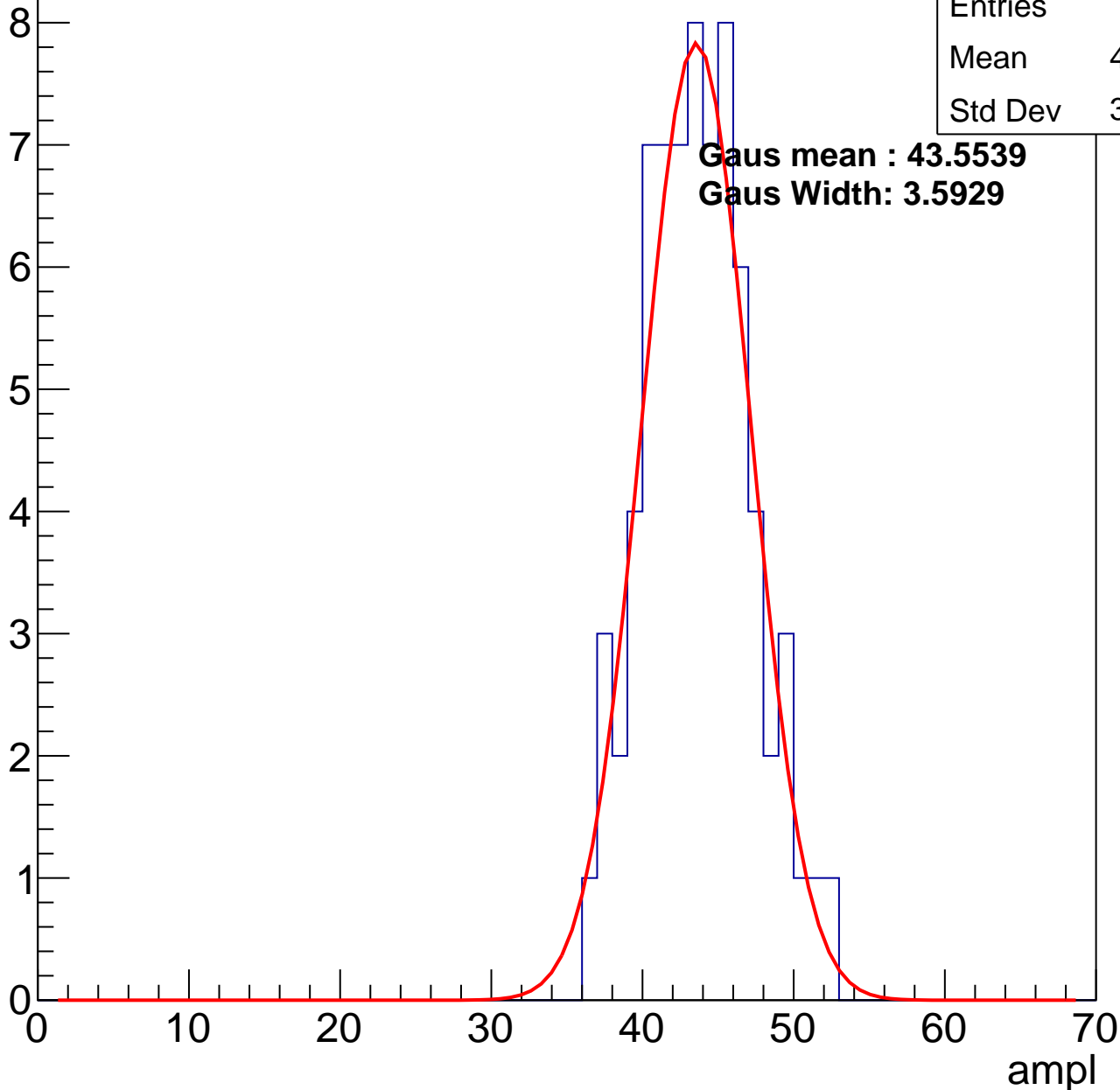
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	72
Mean	43.22
Std Dev	3.485

**Gaus mean : 43.5539**

**Gaus Width: 3.5929**

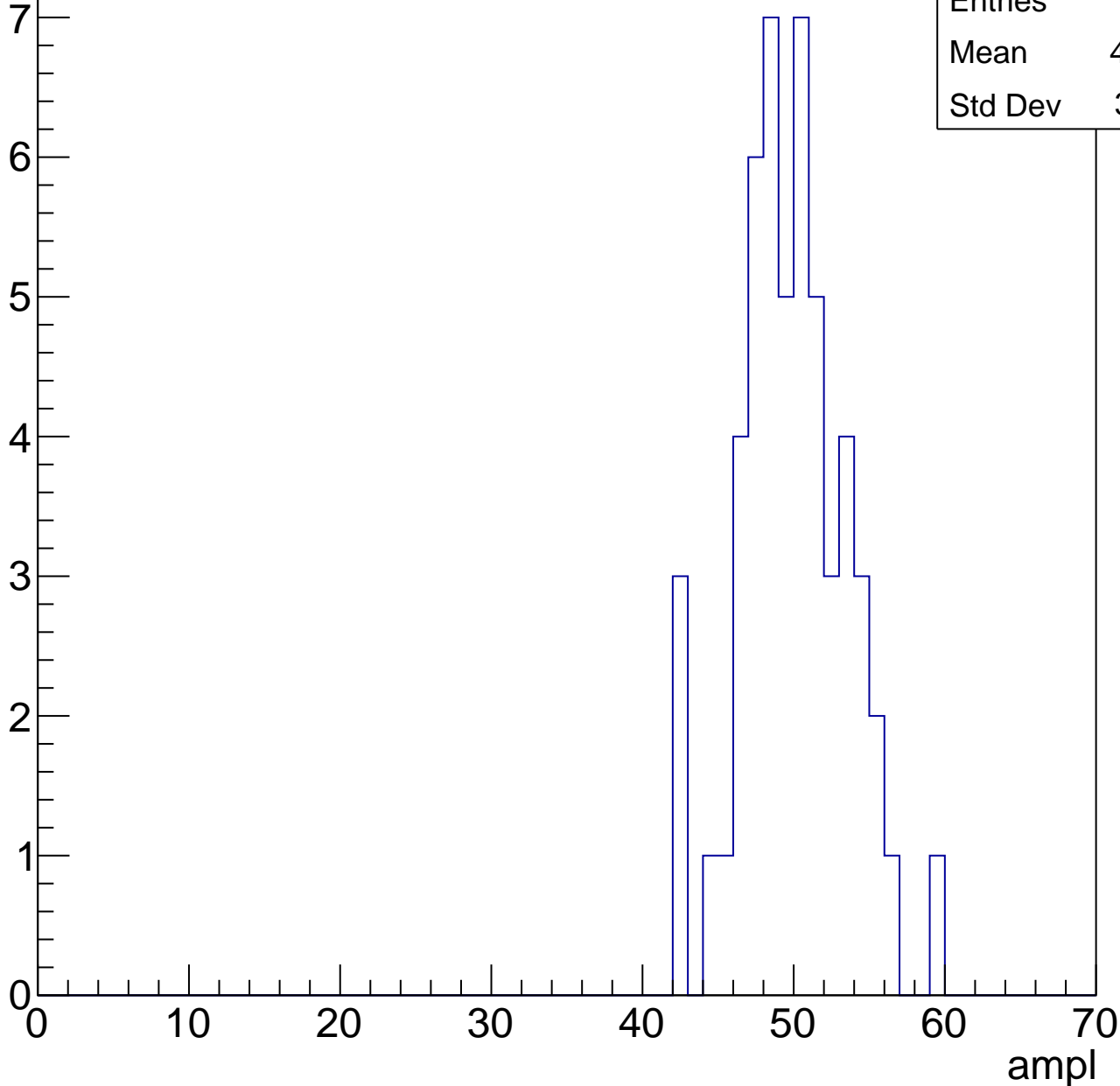


# B0L002S, U2-ch126, adc3

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

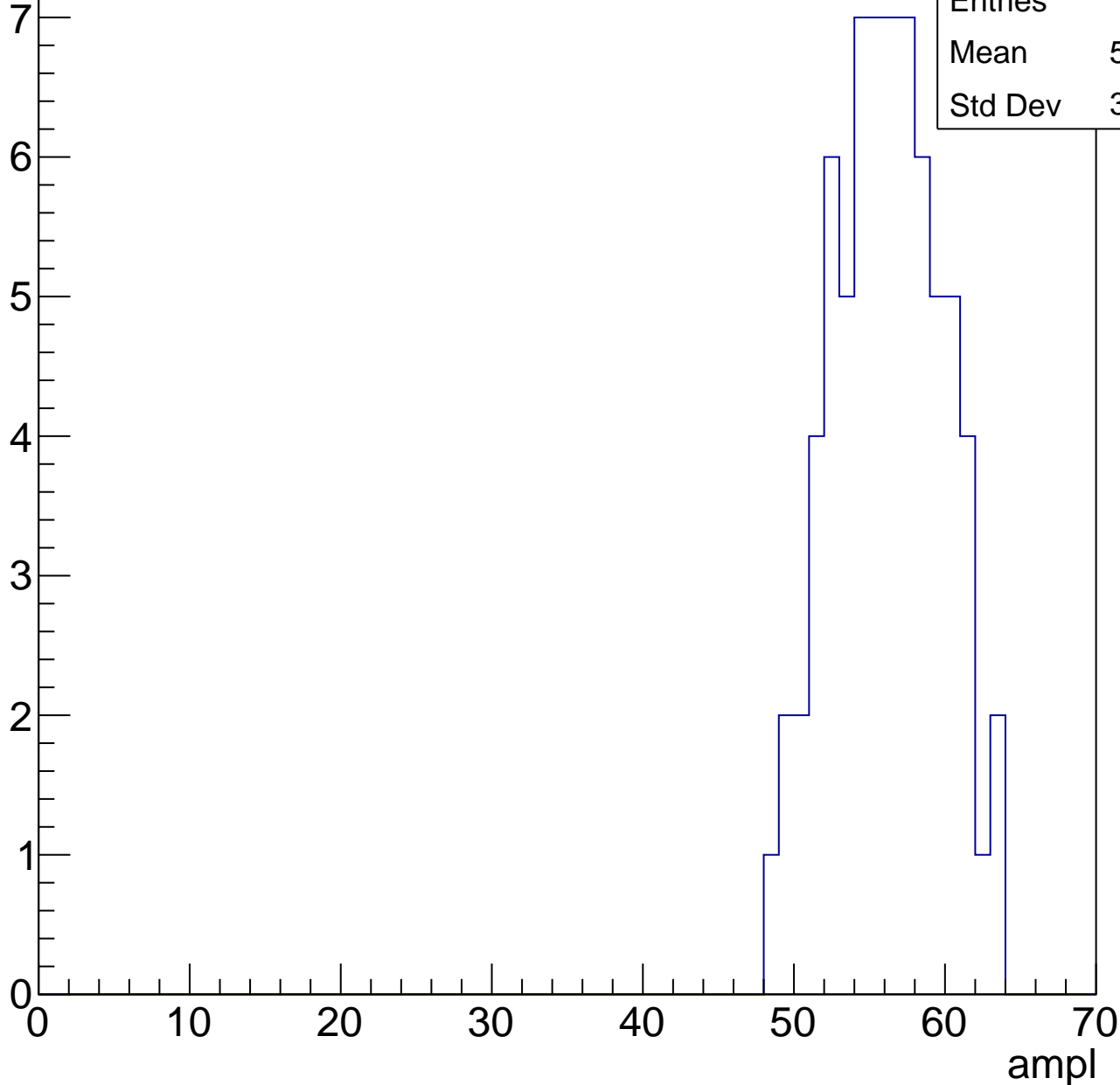
Entries	53
Mean	49.47
Std Dev	3.521



# B0L002S, U2-ch126, adc4

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



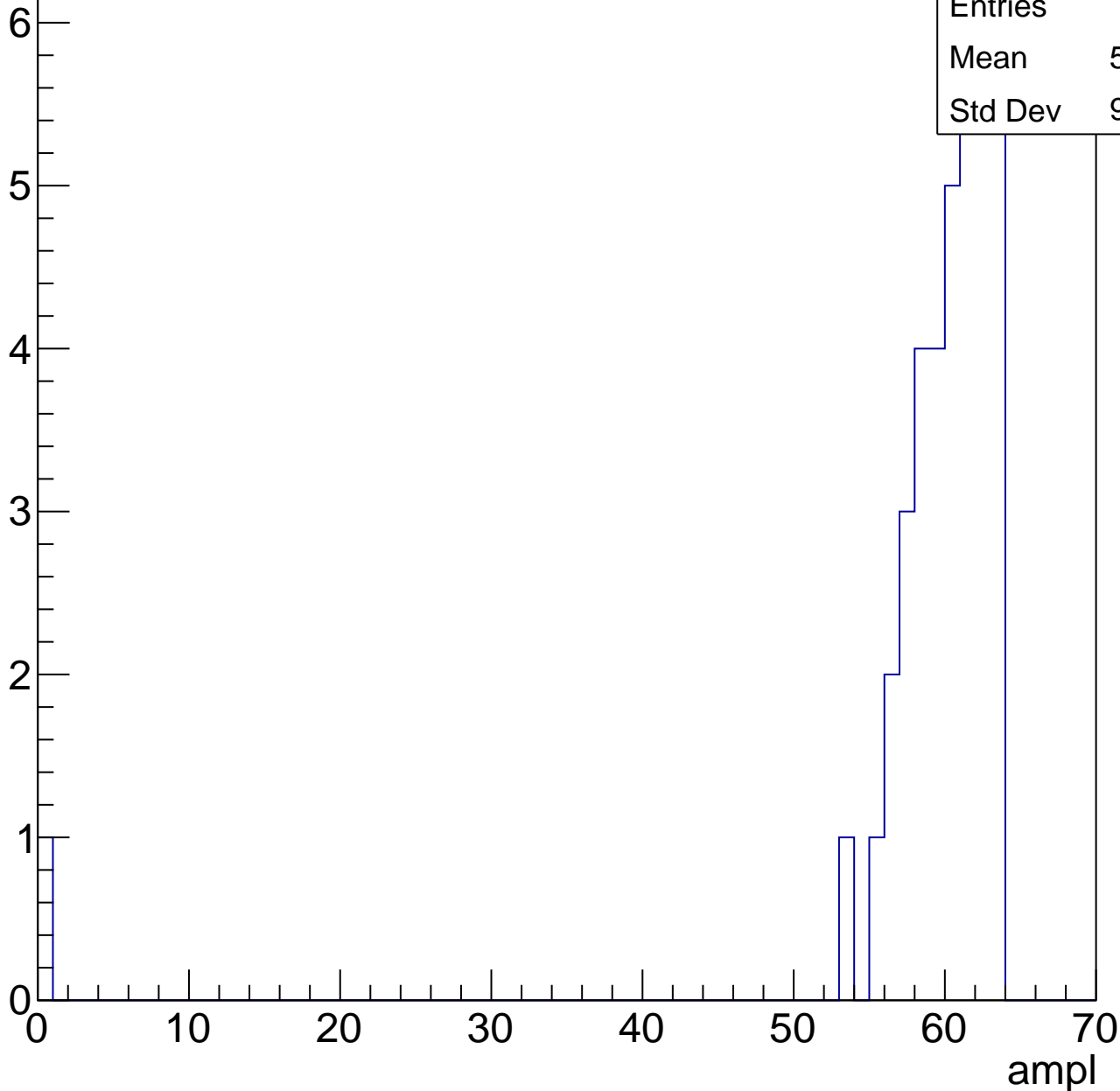
Entries	71
Mean	55.72
Std Dev	3.549

# B0L002S, U2-ch126, adc5

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	39
Mean	58.33
Std Dev	9.778



# B0L002S, U2-ch126, adc6

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry





# B0L002S, U2-ch126, adc7

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



# B0L002S, U2-ch127, adc0

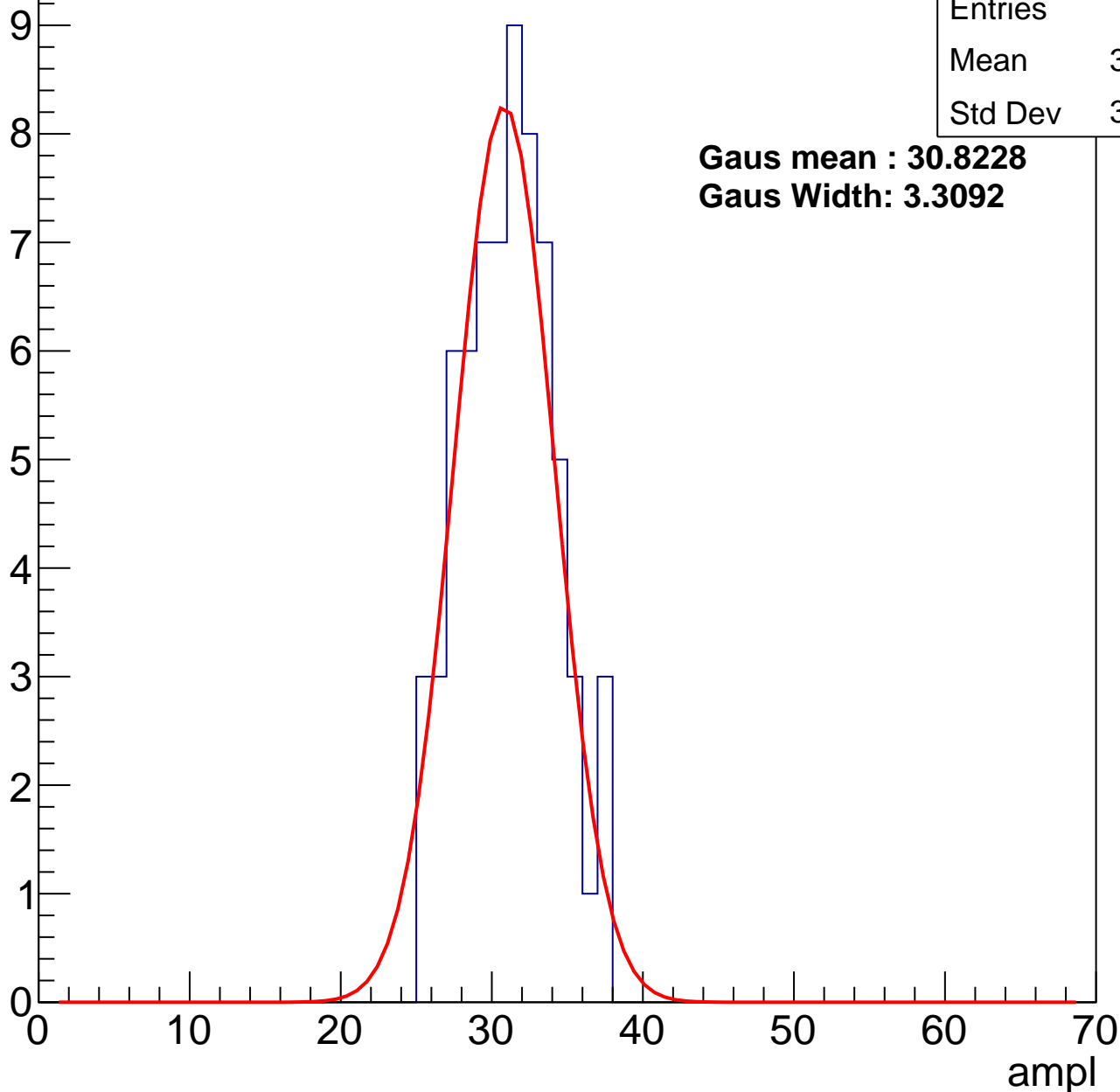
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	68
Mean	30.65
Std Dev	3.023

**Gaus mean : 30.8228**

**Gaus Width: 3.3092**



# B0L002S, U2-ch127, adc1

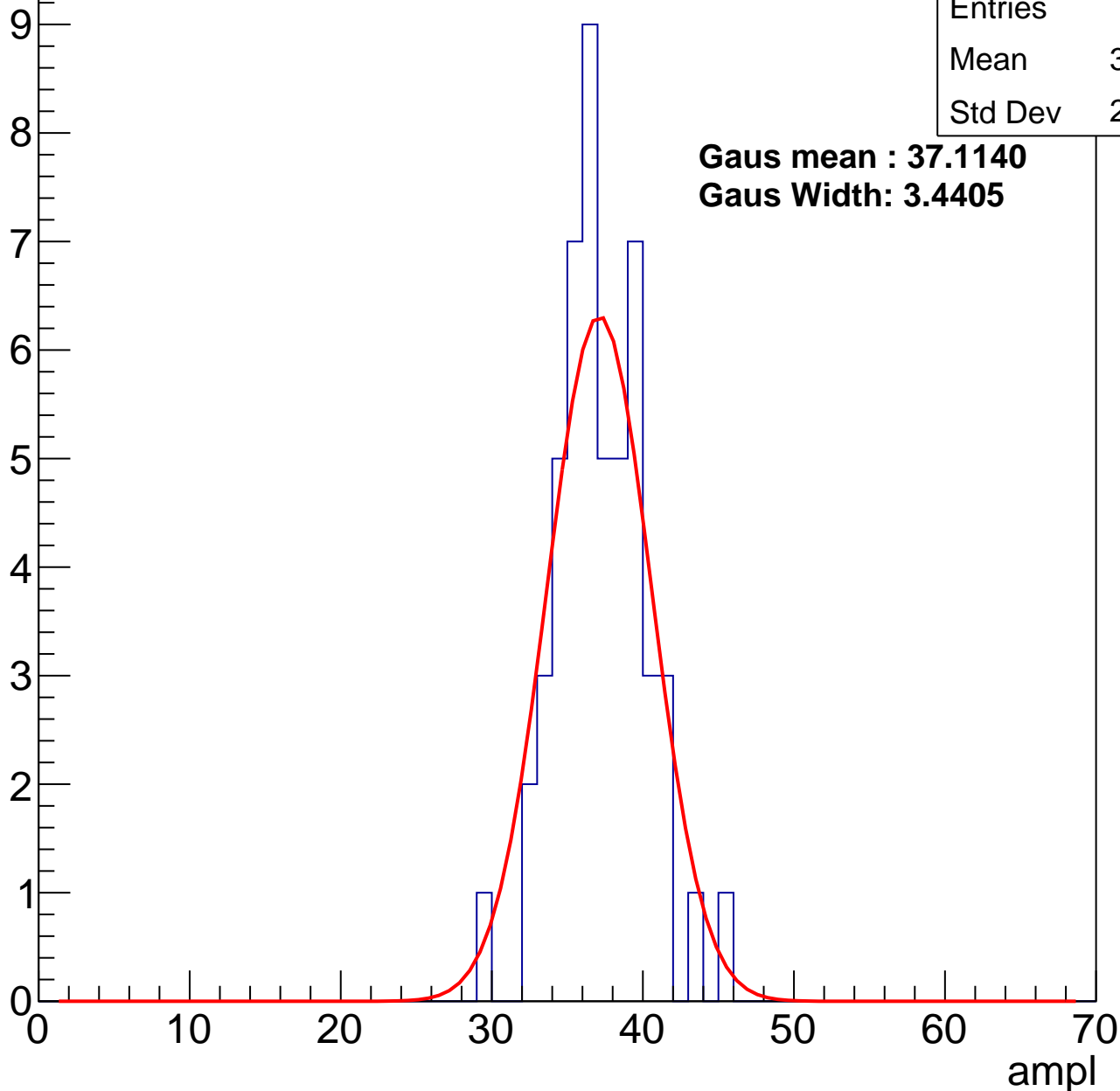
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	52
Mean	36.73
Std Dev	2.936

**Gaus mean : 37.1140**

**Gaus Width: 3.4405**



# B0L002S, U2-ch127, adc2

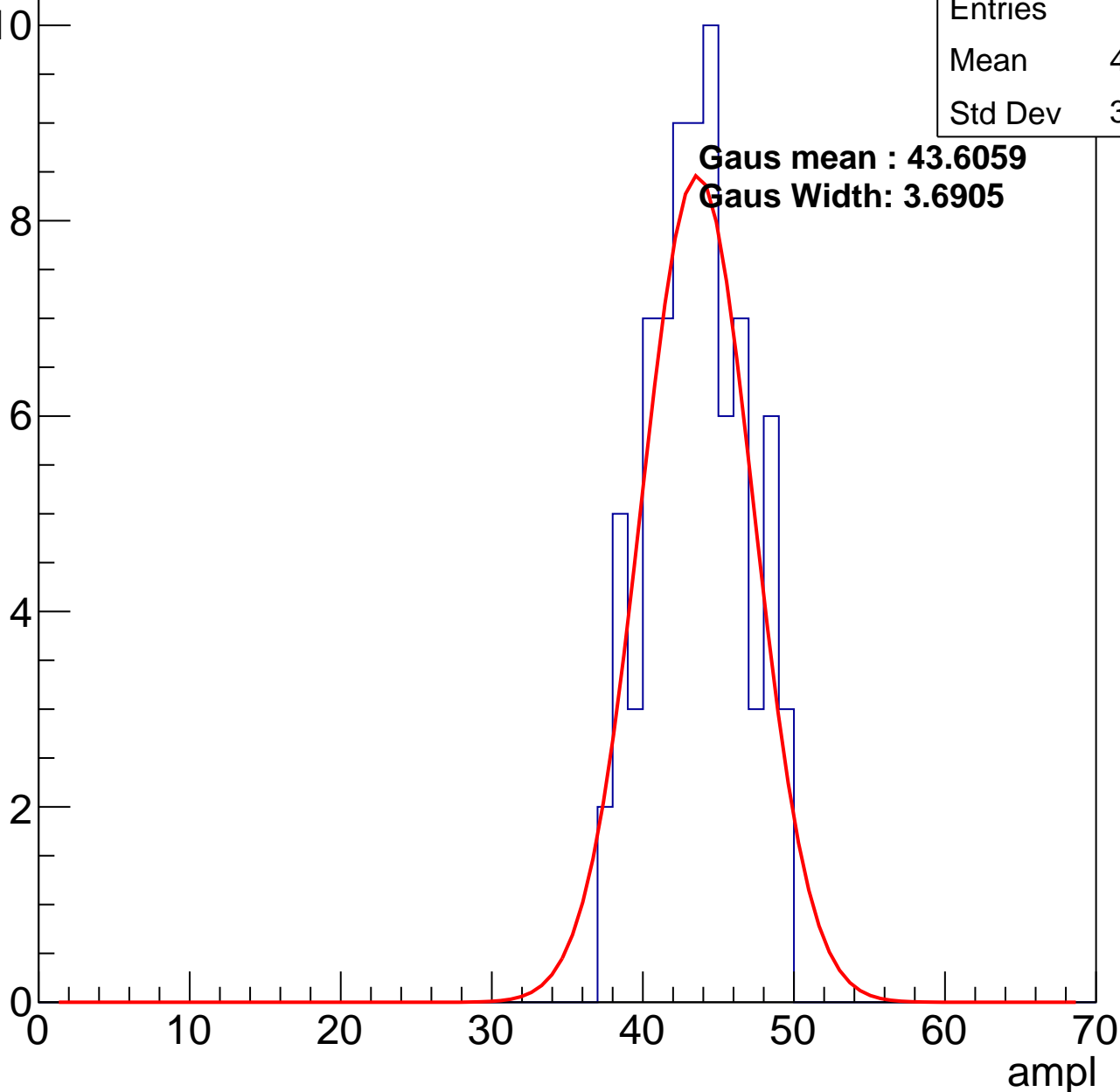
calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	77
Mean	43.13
Std Dev	3.114

**Gaus mean : 43.6059**

**Gaus Width: 3.6905**

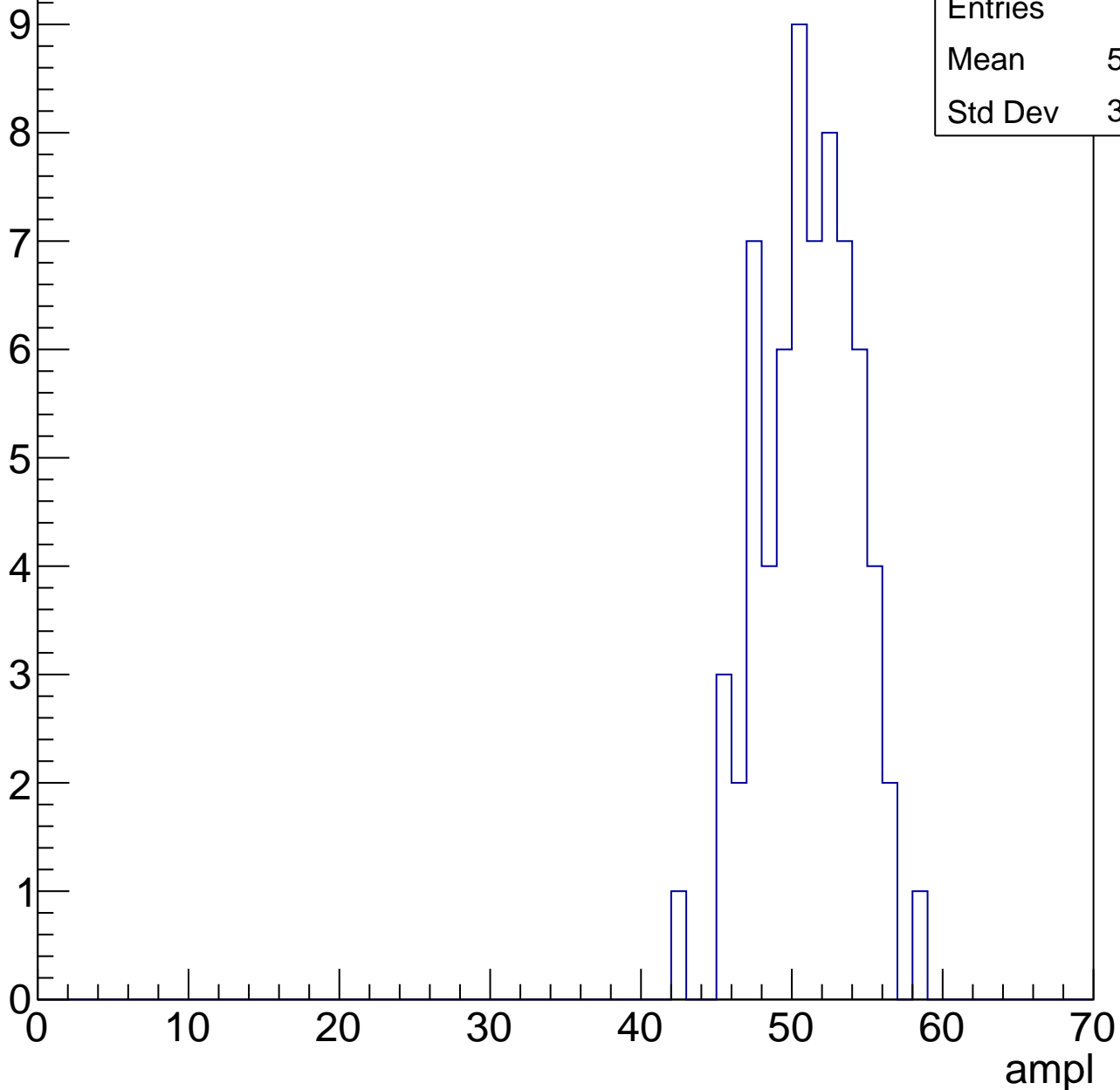


# B0L002S, U2-ch127, adc3

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	67
Mean	50.63
Std Dev	3.147

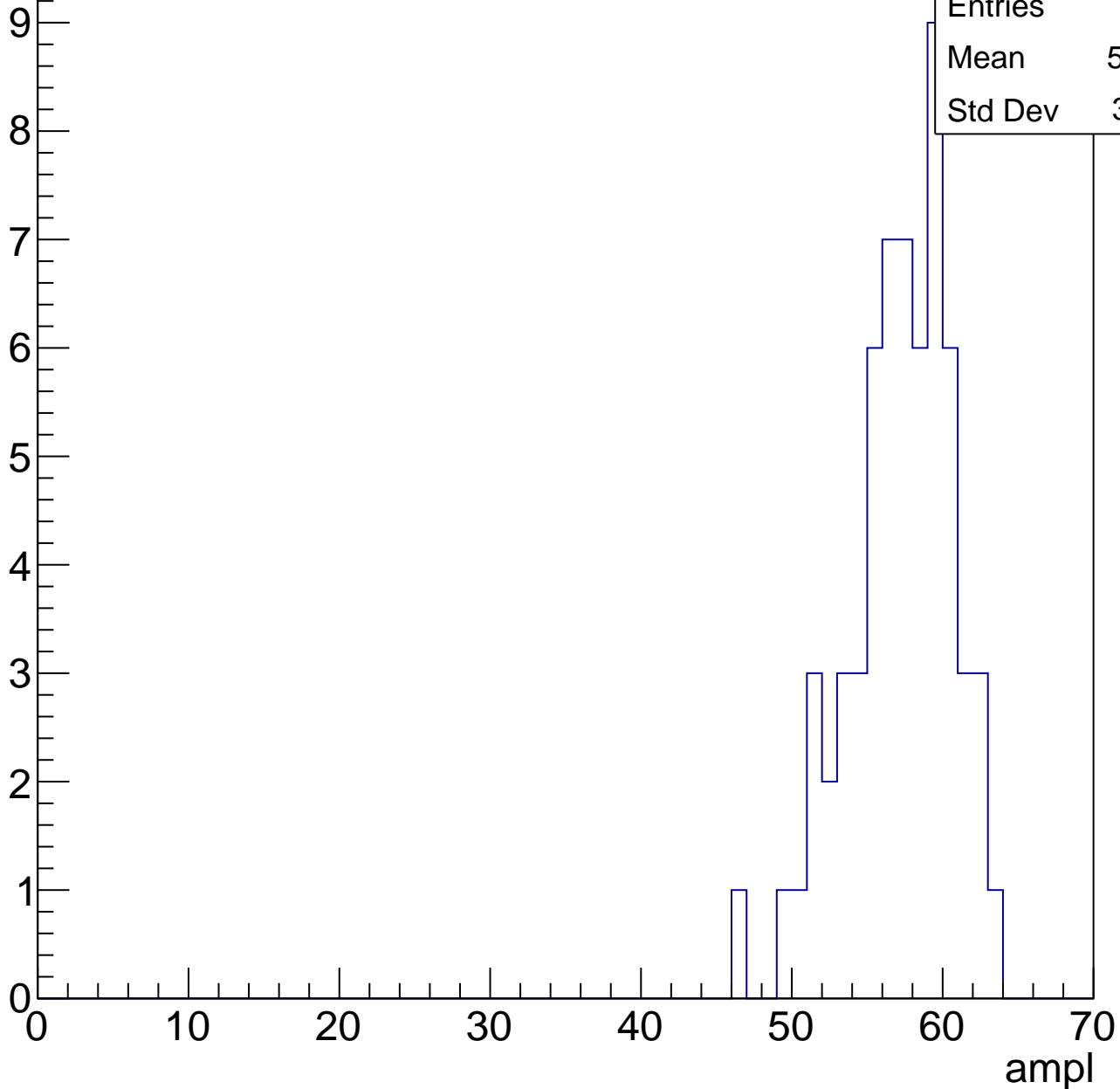


# B0L002S, U2-ch127, adc4

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	62
Mean	56.69
Std Dev	3.471

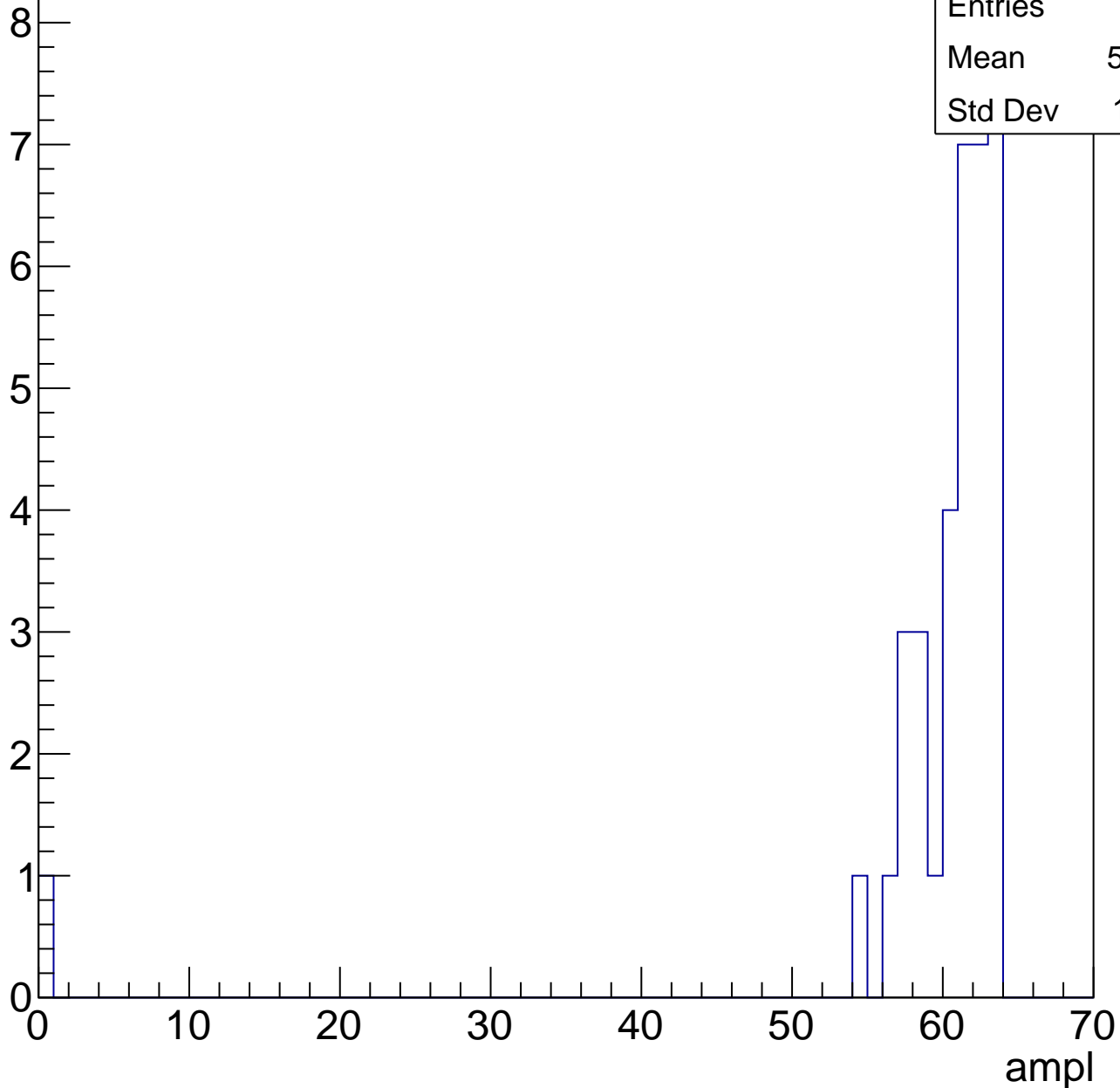


# B0L002S, U2-ch127, adc5

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry

Entries	36
Mean	58.86
Std Dev	10.21



# B0L002S, U2-ch127, adc6

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



Entries	1
Mean	63
Std Dev	0



# B0L002S, U2-ch127, adc7

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L002S, U2-ch127, adc7

calib\_packv5\_042523\_0143.root, FC#8, port C1

Entry



Entries	0
Mean	0
Std Dev	0