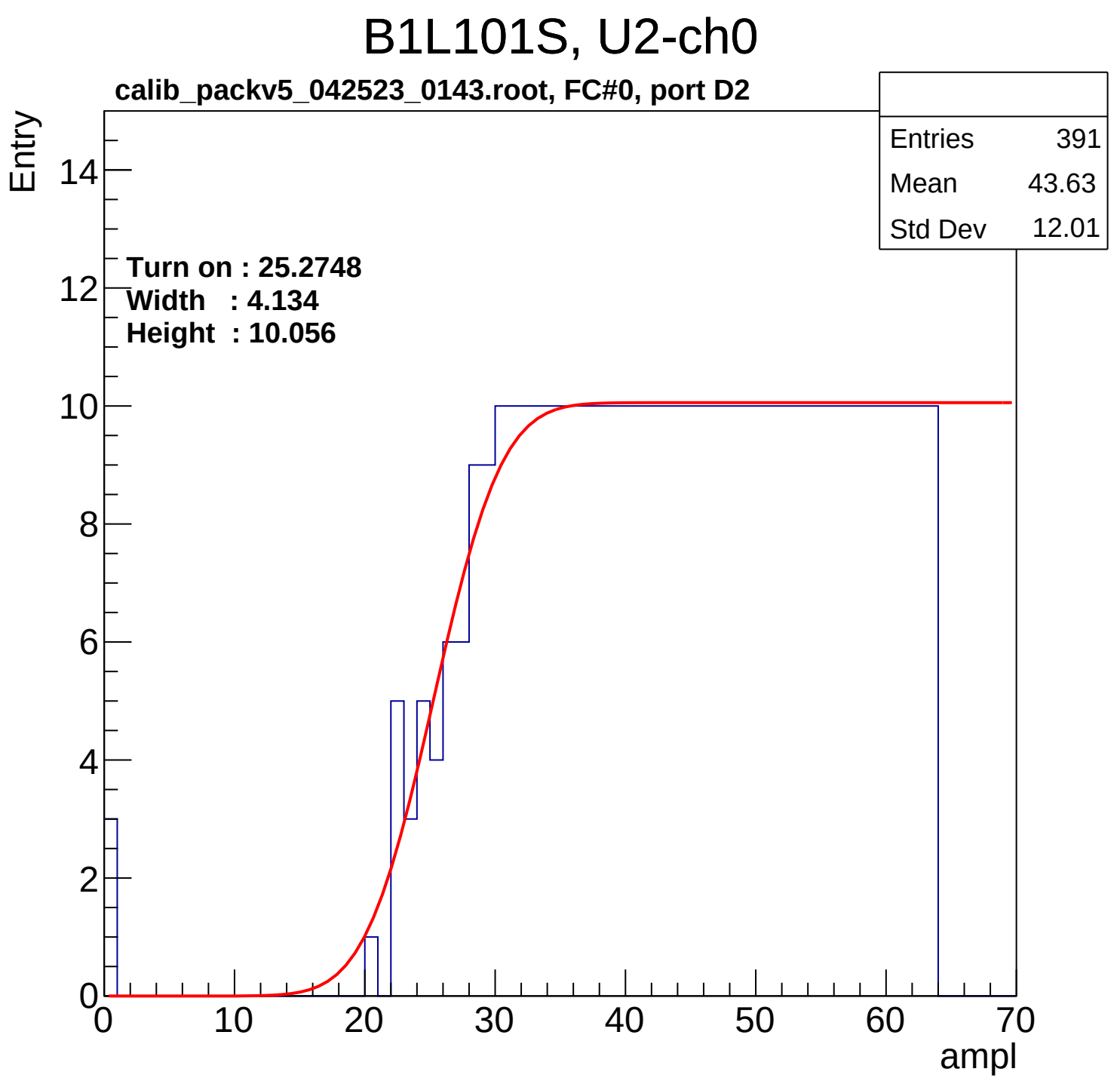
B1L101S, U2-ch0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 391
Mean 43.63
Std Dev 12.01
Turn on : 25.2748
Width : 4.134
Height : 10.056
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ampl
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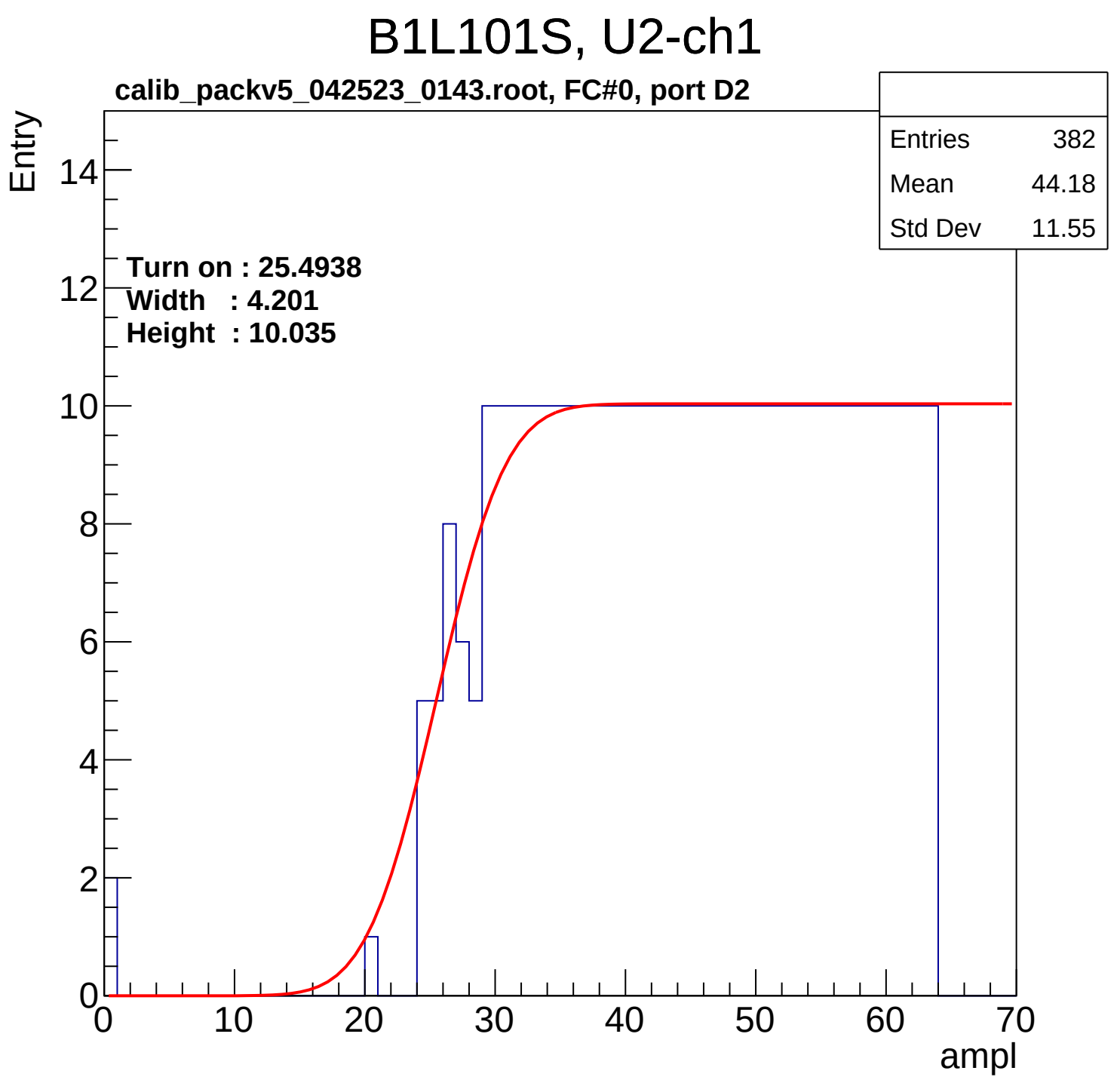
B1L101S, U2-ch1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 382
Mean 44.18
Std Dev 11.55
Turn on : 25.4938
Width : 4.201
Height : 10.035
Entry
ampl
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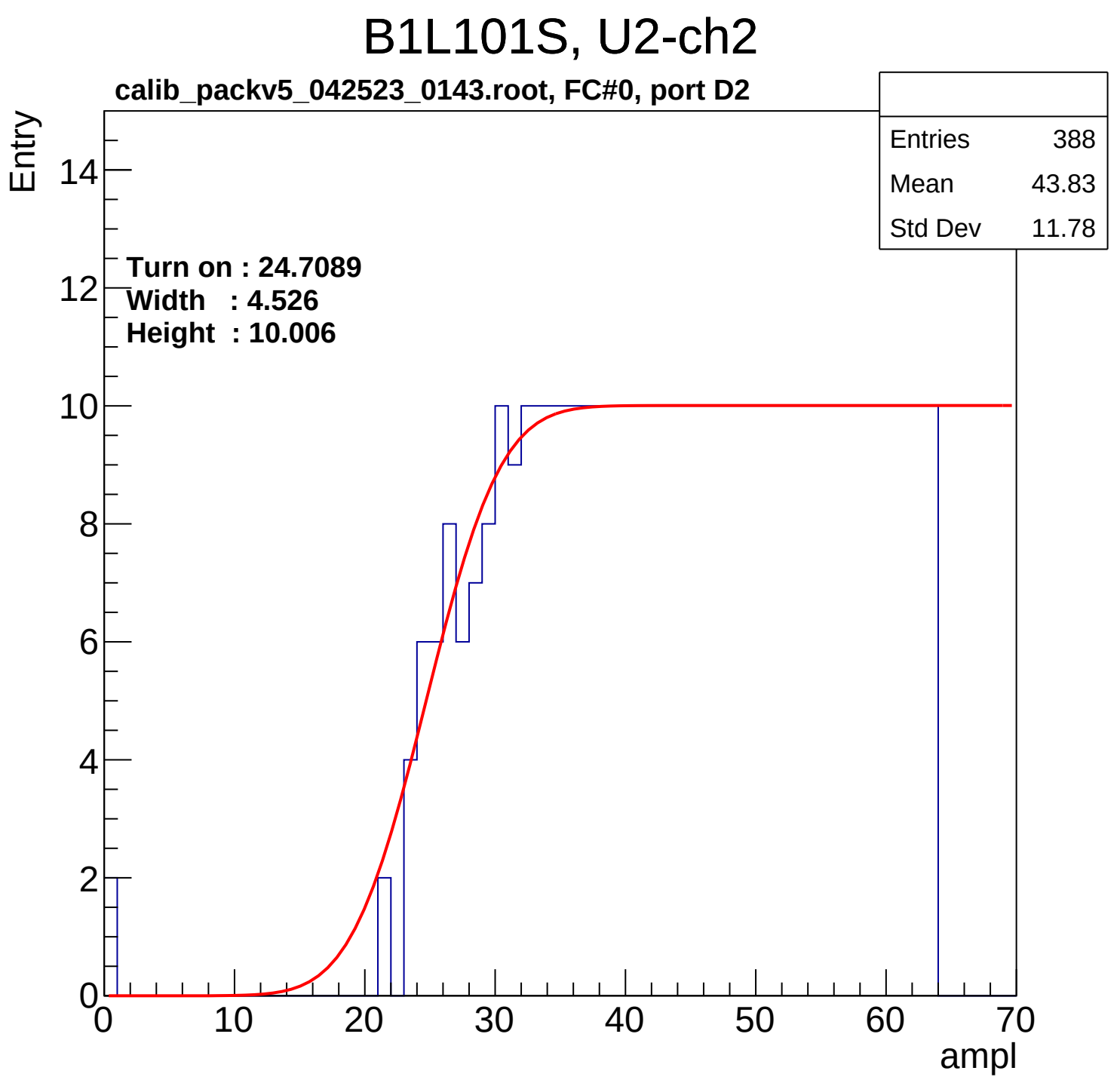
B1L101S, U2-ch2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 388
Mean 43.83
Std Dev 11.78
Turn on : 24.7089
Width : 4.526
Height : 10.006
Entry
ampl
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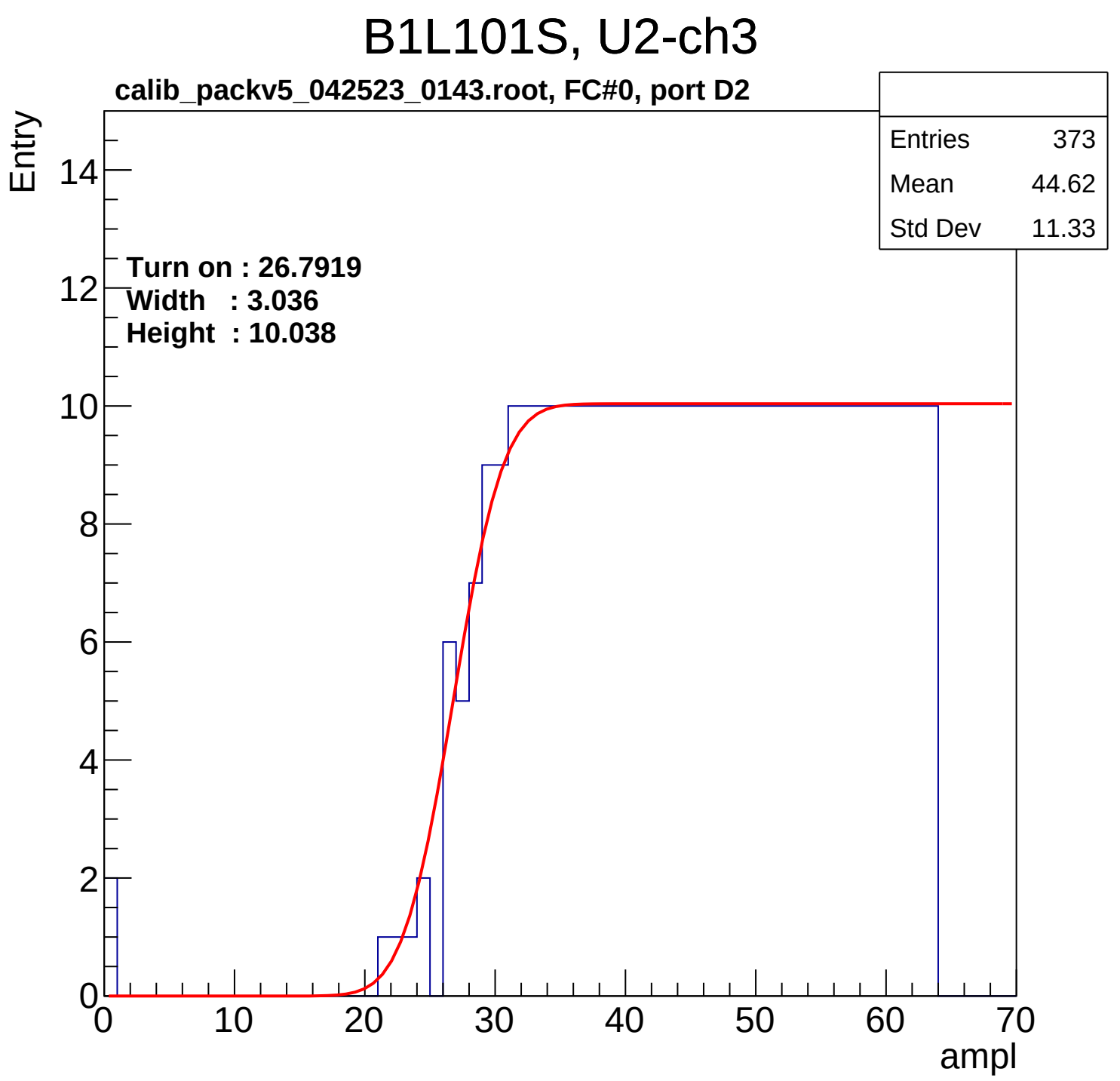
B1L101S, U2-ch3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 373
Mean 44.62
Std Dev 11.33
Turn on : 26.7919
Width : 3.036
Height : 10.038
Entry
ampl
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6
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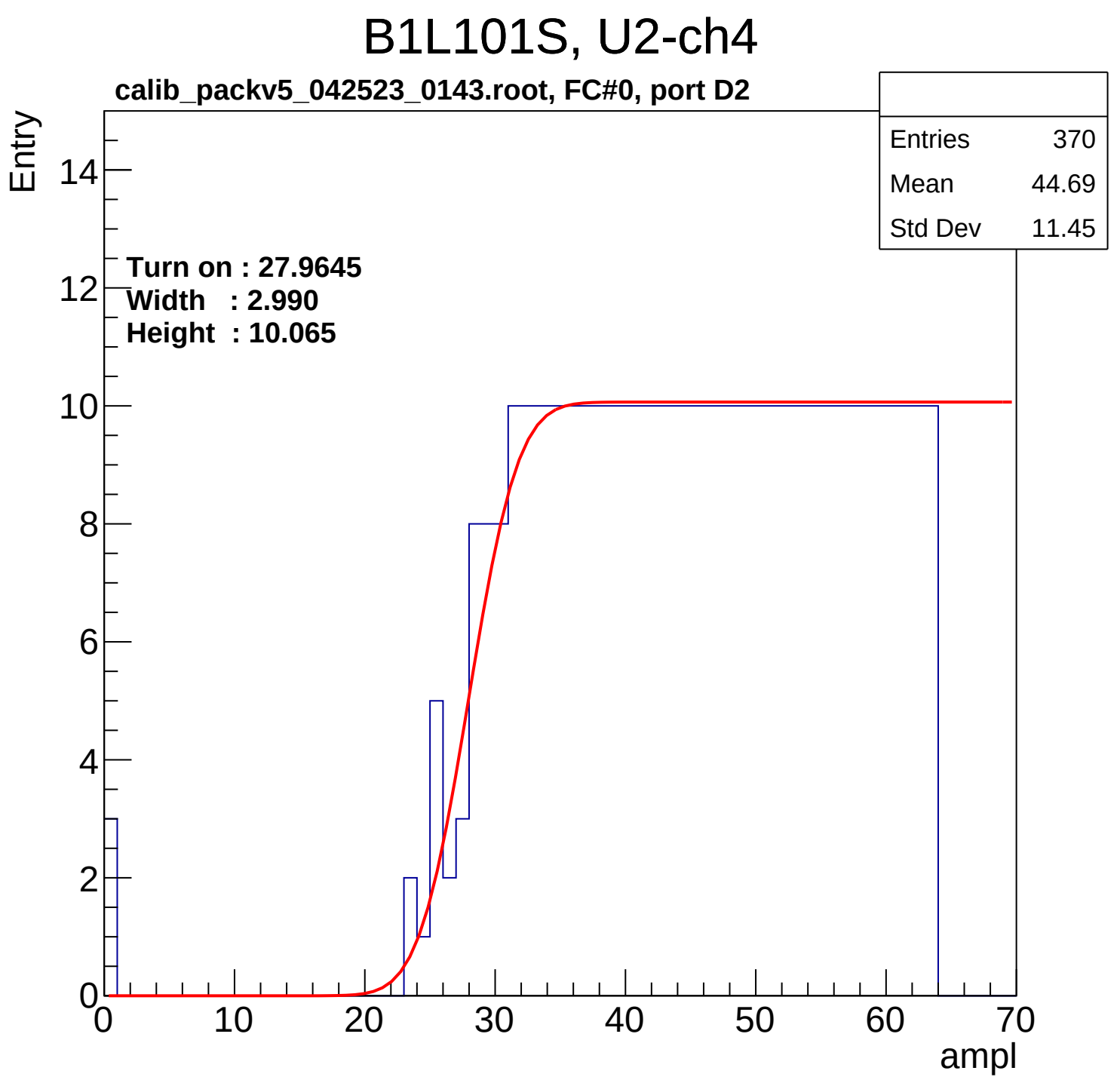
B1L101S, U2-ch4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 370
Mean 44.69
Std Dev 11.45
Turn on : 27.9645
Width : 2.990
Height : 10.065
Entry
ampl
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2
4
6
8
10
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0
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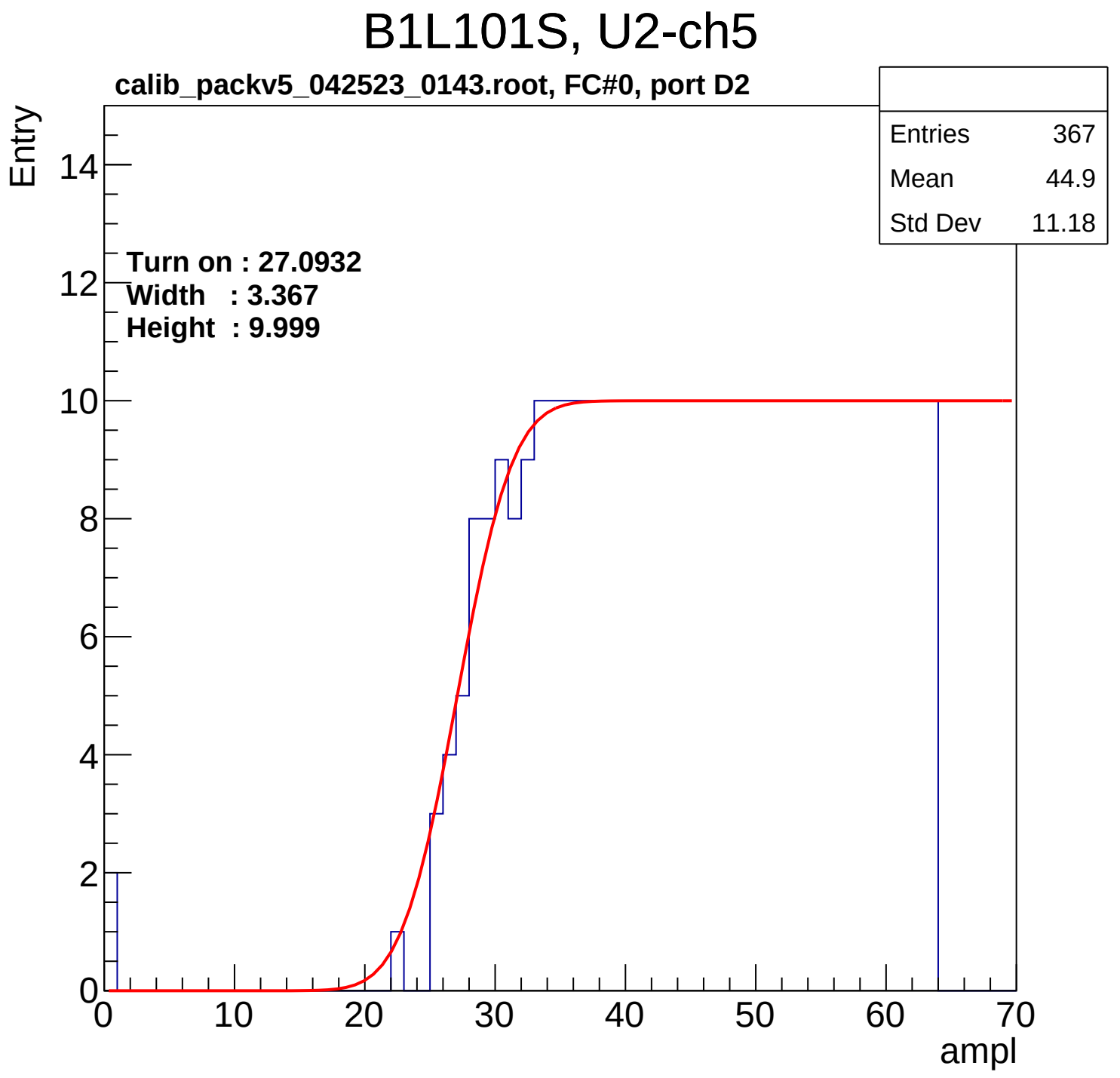
B1L101S, U2-ch5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 367
Mean 44.9
Std Dev 11.18
Turn on : 27.0932
Width : 3.367
Height : 9.999
Entry
ampl
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8
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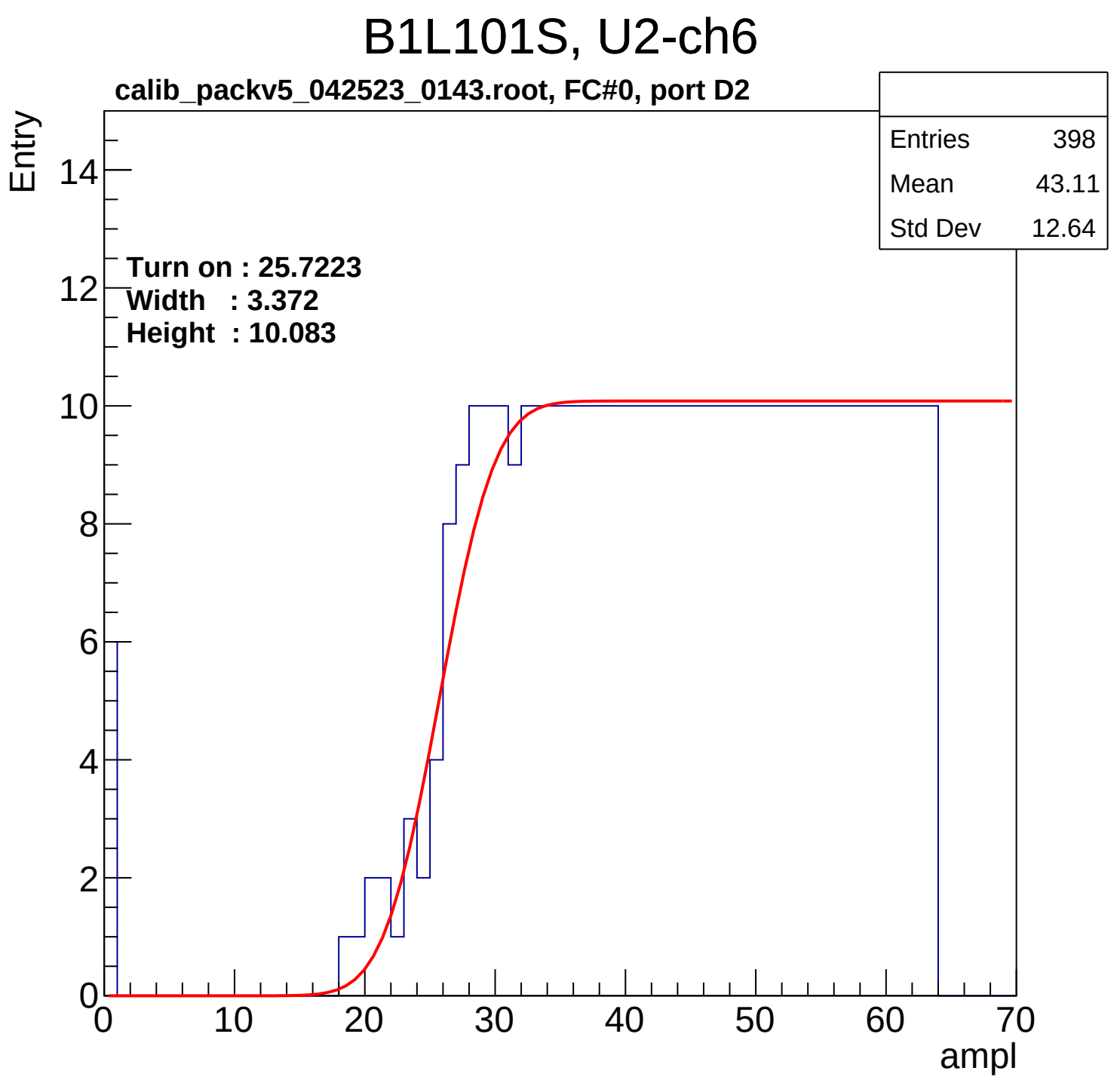
B1L101S, U2-ch6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 398
Mean 43.11
Std Dev 12.64
Turn on : 25.7223
Width : 3.372
Height : 10.083
Entry
ampl
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6
8
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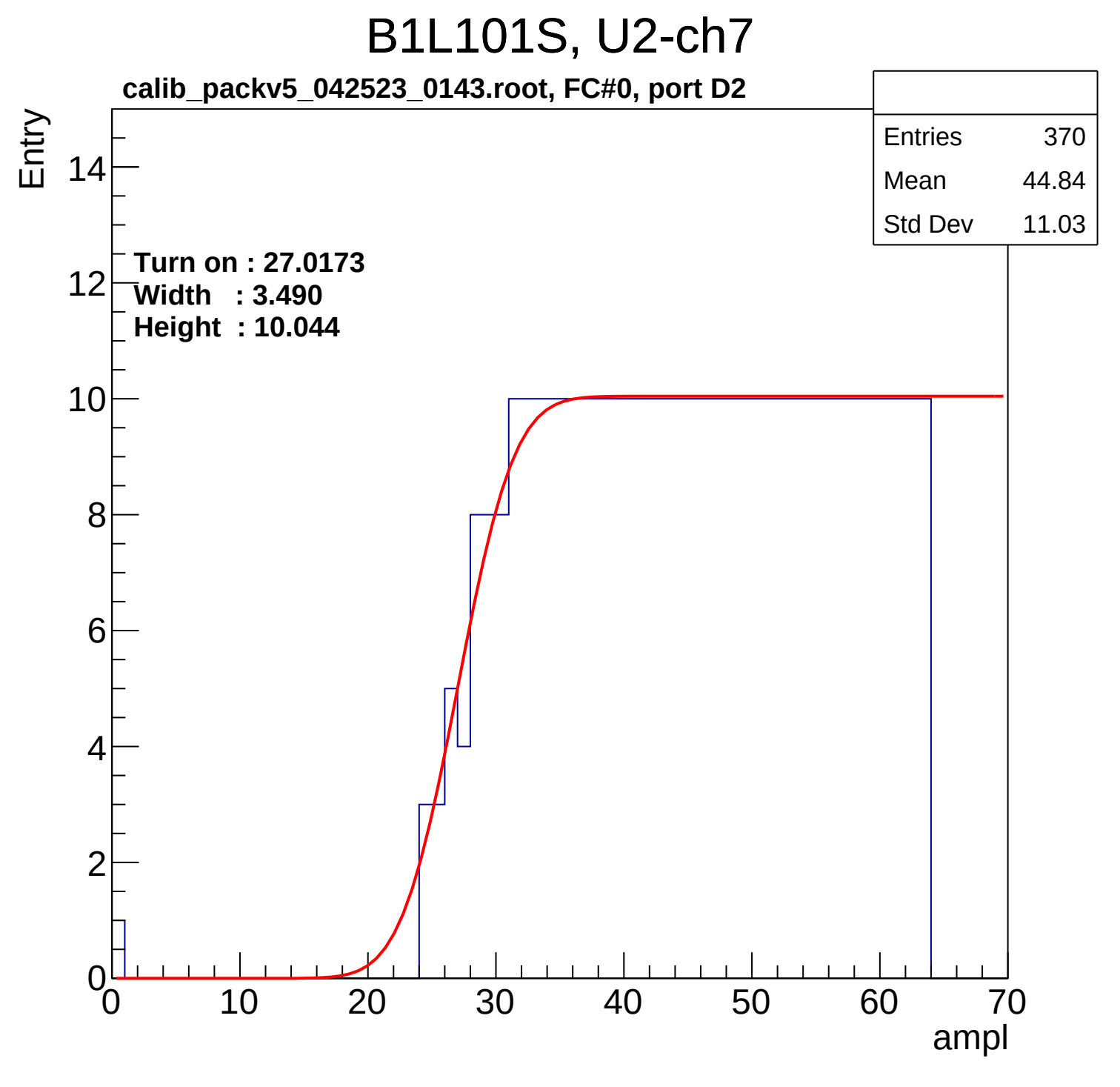
B1L101S, U2-ch7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 370
Mean 44.84
Std Dev 11.03
Turn on : 27.0173
Width : 3.490
Height : 10.044
Entry
ampl
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4
6
8
10
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0
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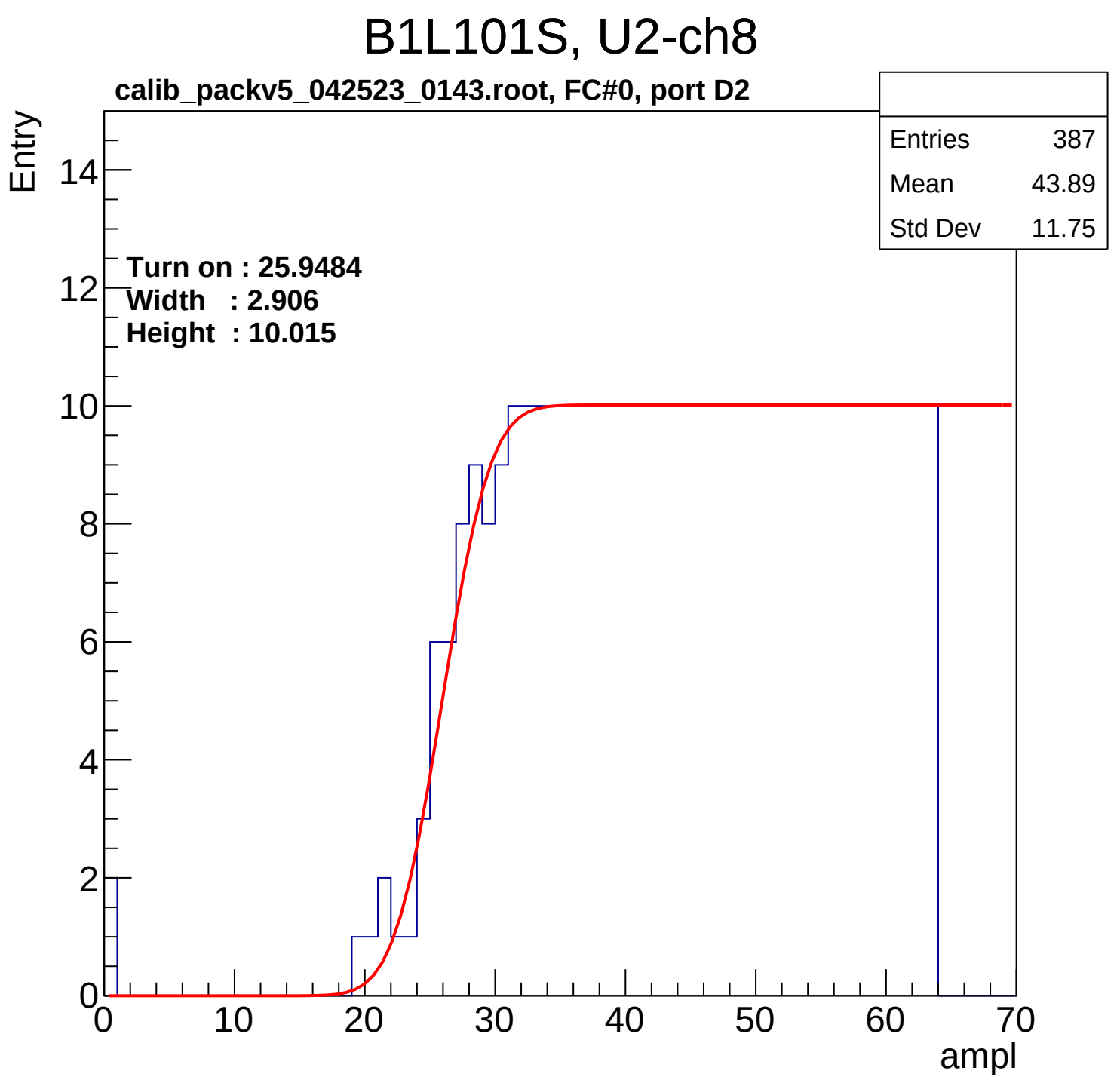
B1L101S, U2-ch8
calib_packv5_042523_0143.root, FC#0, port D2
Entries 387
Mean 43.89
Std Dev 11.75
Turn on : 25.9484
Width : 2.906
Height : 10.015
Entry
ampl
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2
4
6
8
10
12
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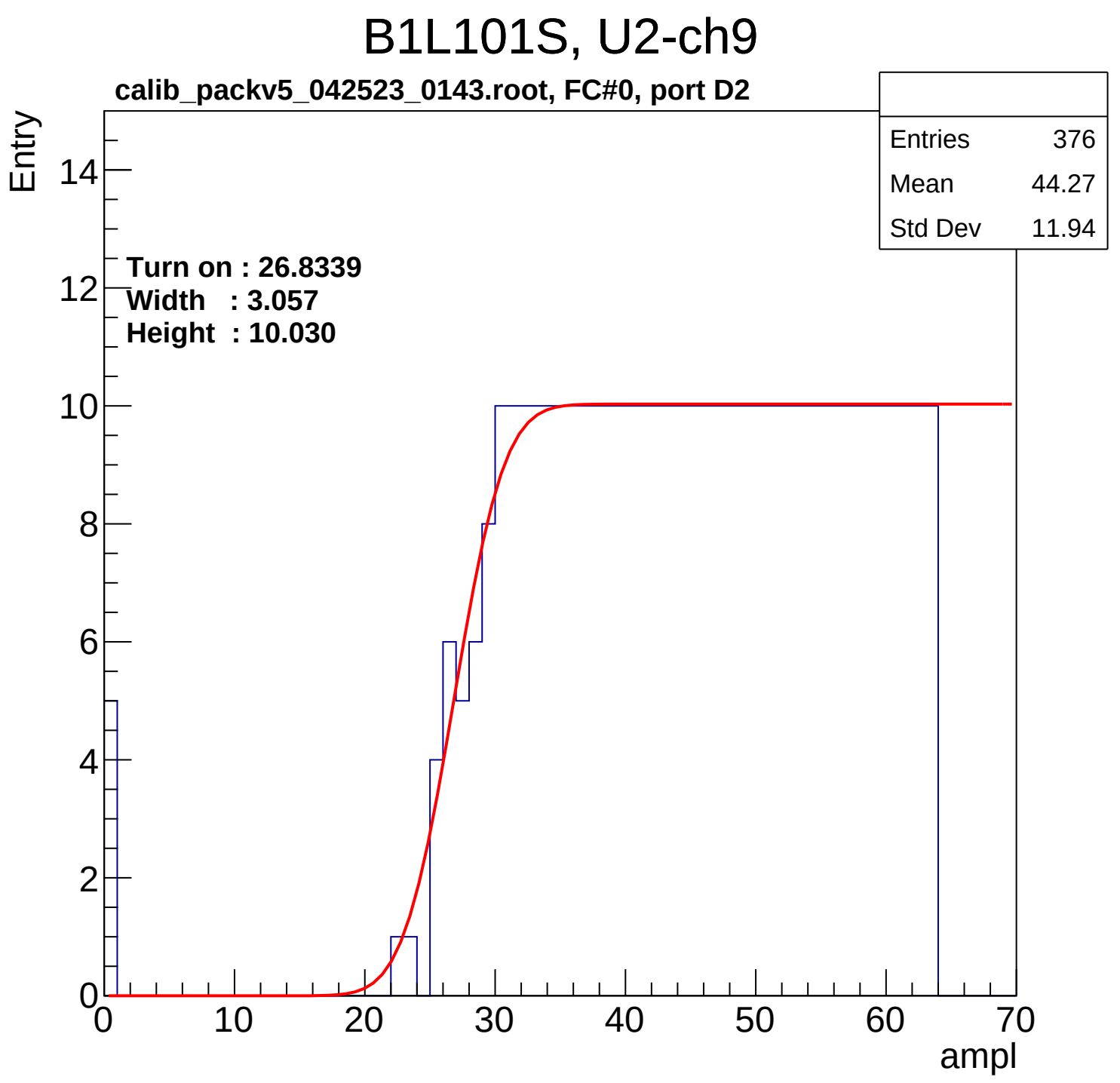
B1L101S, U2-ch9
calib_packv5_042523_0143.root, FC#0, port D2
Entries 376
Mean 44.27
Std Dev 11.94
Turn on : 26.8339
Width : 3.057
Height : 10.030
Entry
ampl
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2
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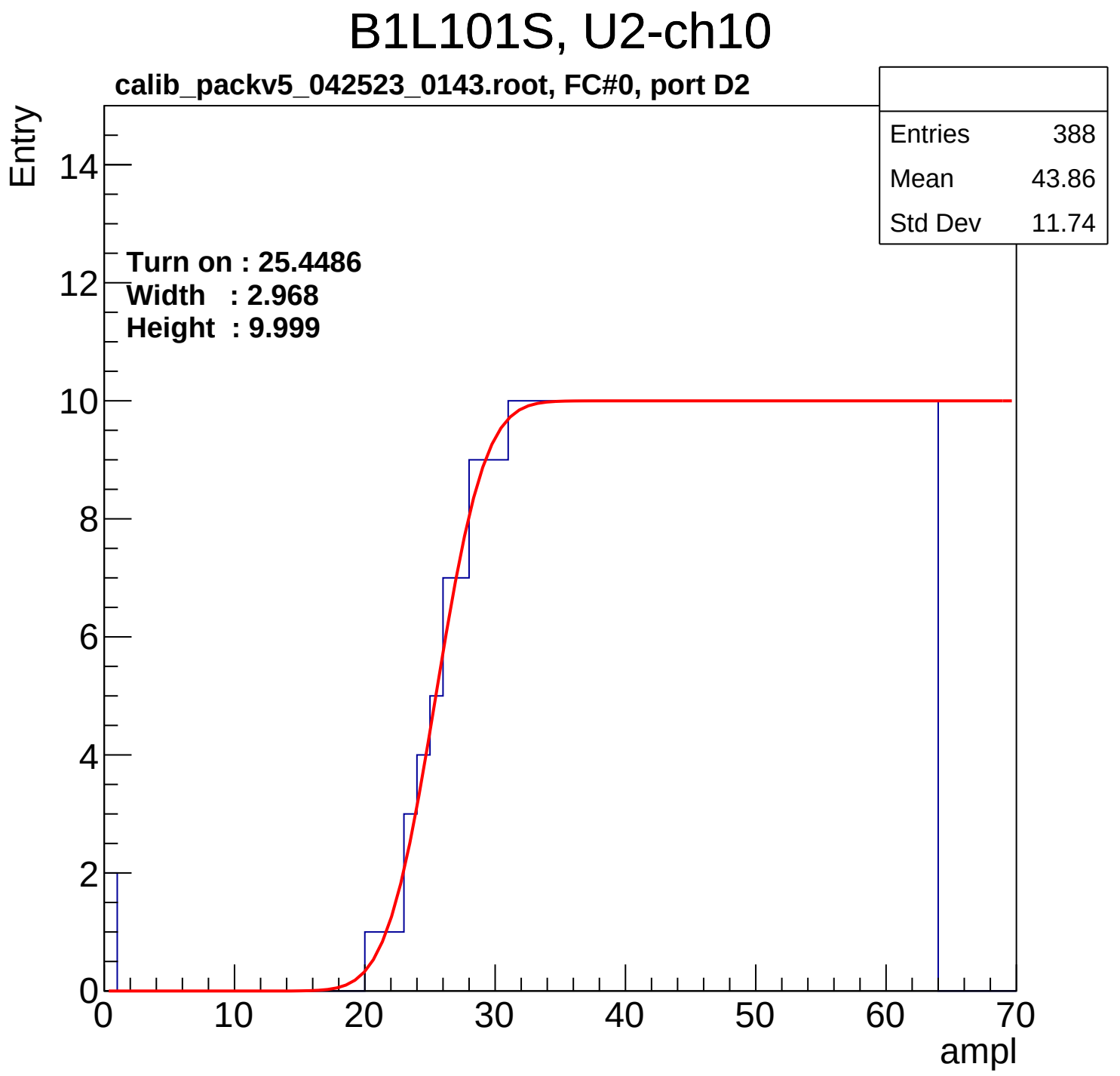
B1L101S, U2-ch10
calib_packv5_042523_0143.root, FC#0, port D2
Entries 388
Mean 43.86
Std Dev 11.74
Turn on : 25.4486
Width : 2.968
Height : 9.999
Entry
ampl
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6
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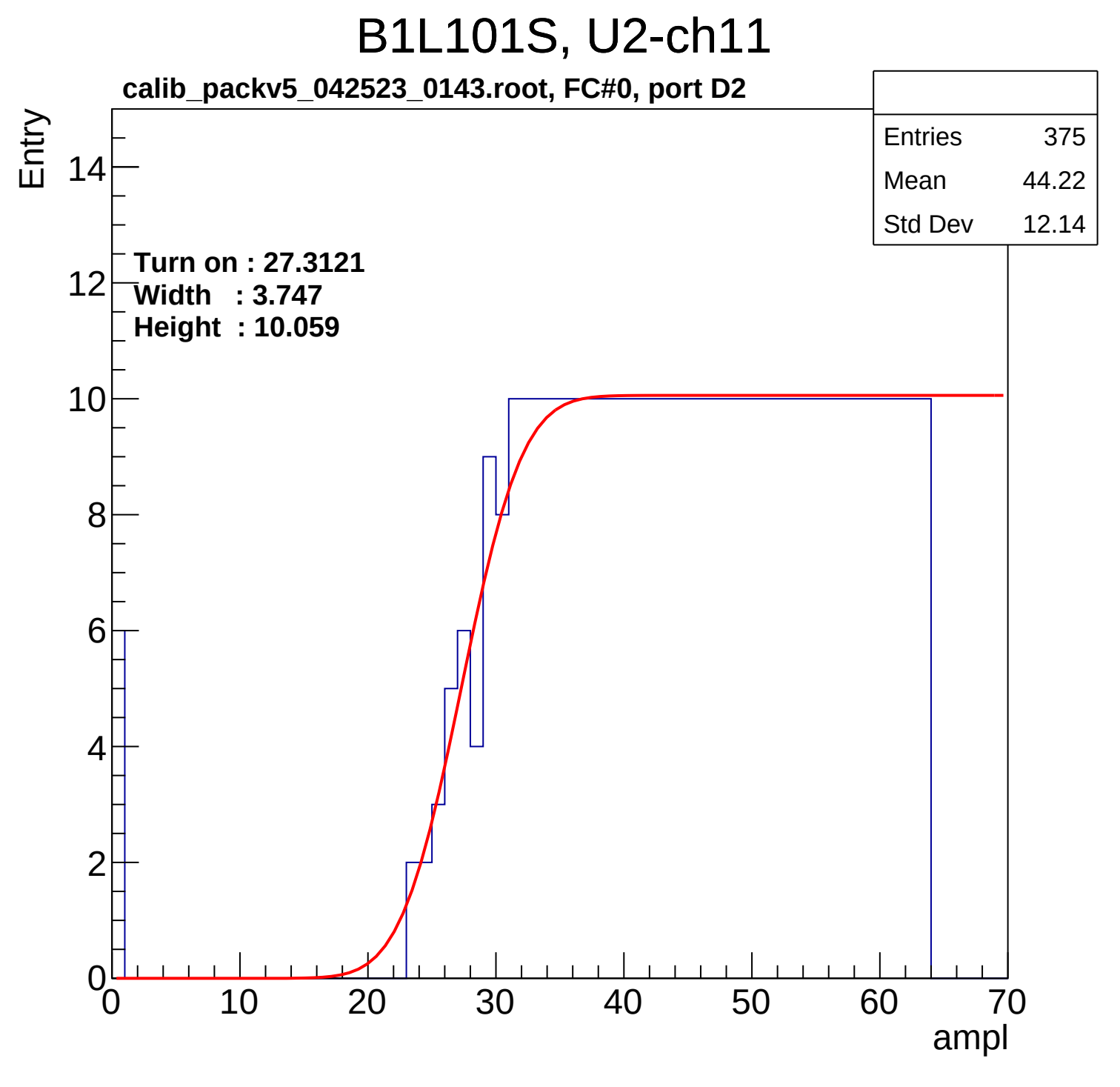
B1L101S, U2-ch11
calib_packv5_042523_0143.root, FC#0, port D2
Entries 375
Mean 44.22
Std Dev 12.14
Turn on : 27.3121
Width : 3.747
Height : 10.059
Entry
ampl
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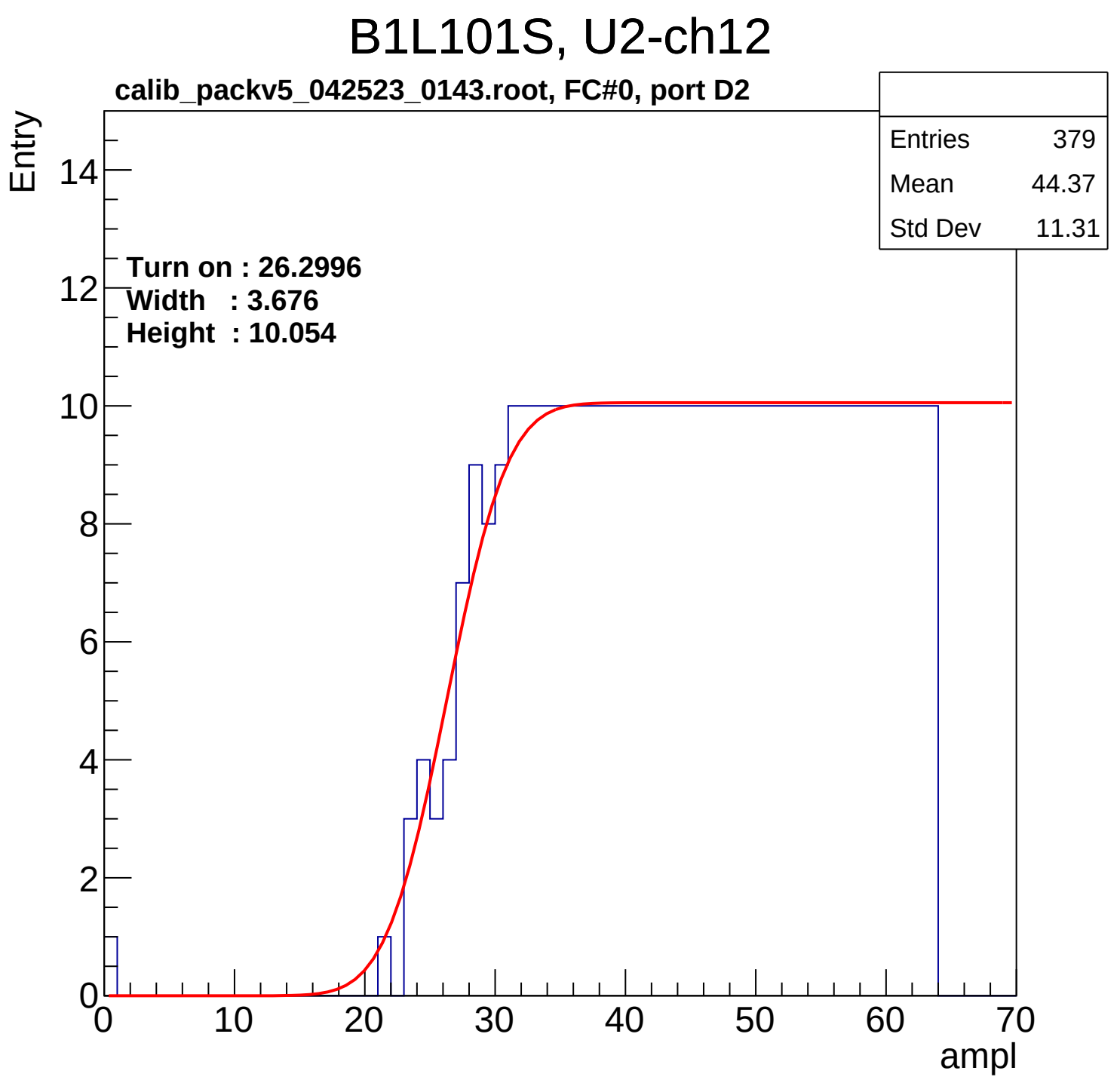
B1L101S, U2-ch12
calib_packv5_042523_0143.root, FC#0, port D2
Entries 379
Mean 44.37
Std Dev 11.31
Turn on : 26.2996
Width : 3.676
Height : 10.054
Entry
ampl
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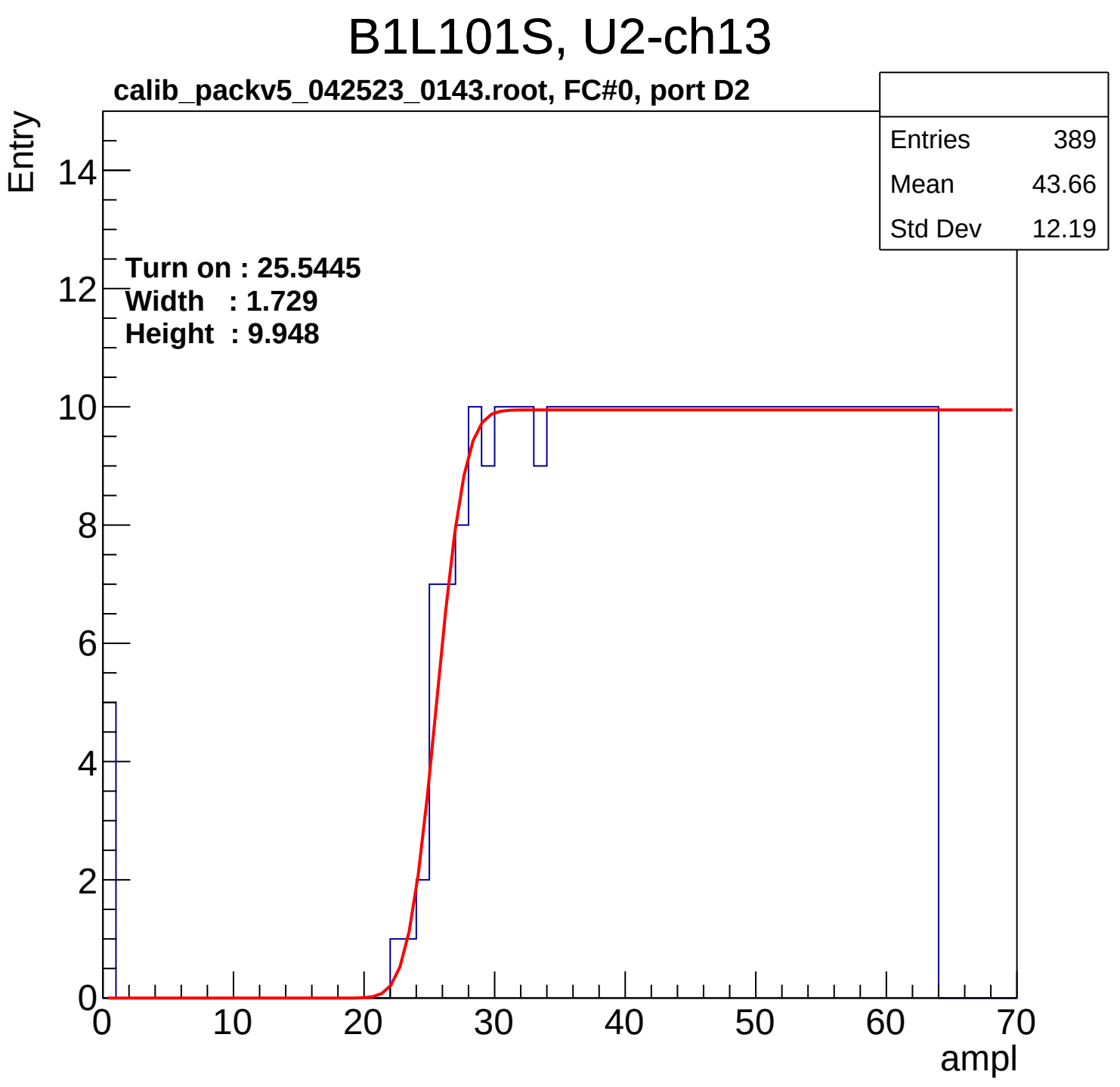
B1L101S, U2-ch13
calib_packv5_042523_0143.root, FC#0, port D2
Entries 389
Mean 43.66
Std Dev 12.19
Turn on : 25.5445
Width : 1.729
Height : 9.948
Entry
ampl
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4
6
8
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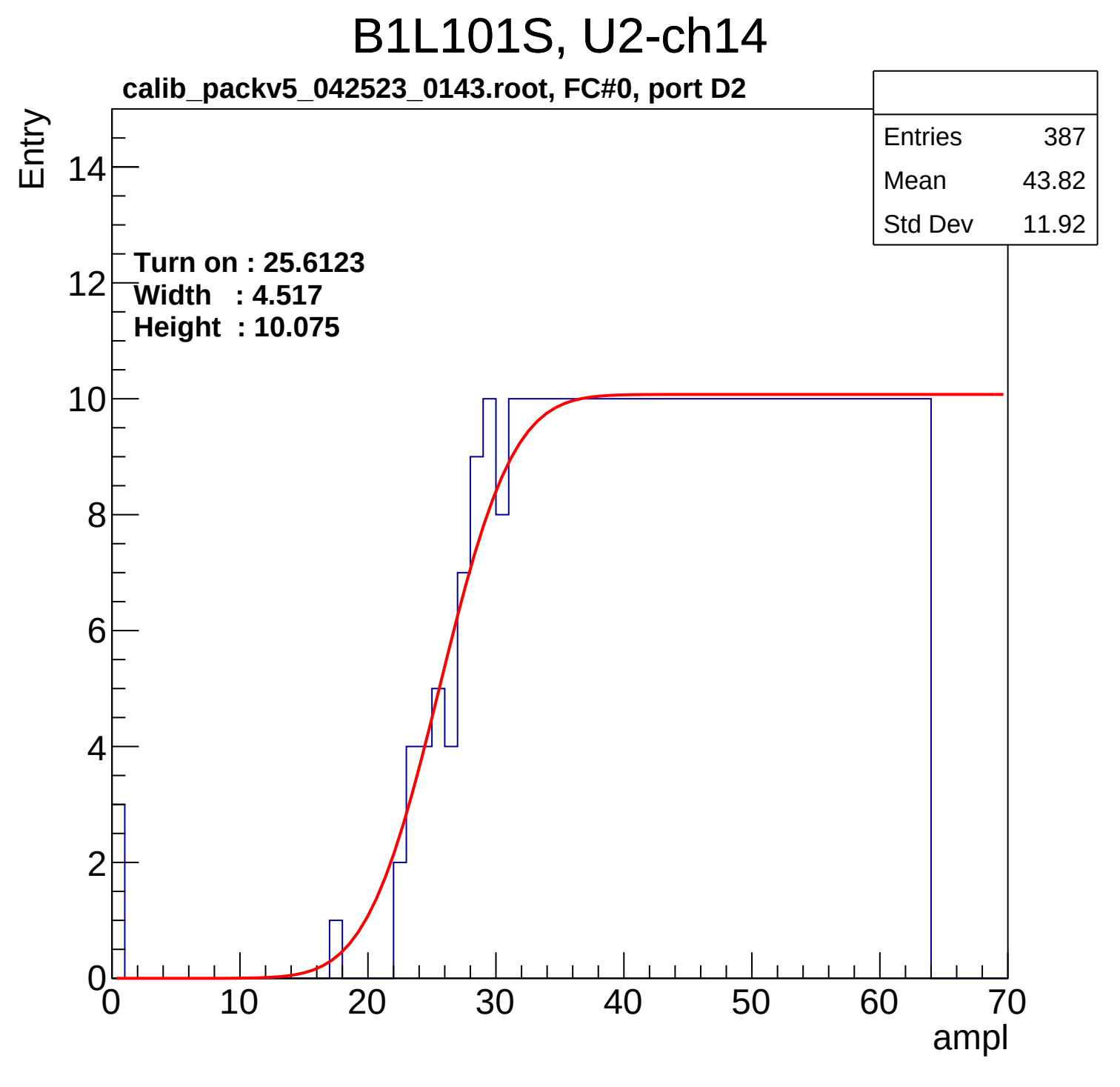
B1L101S, U2-ch14
calib_packv5_042523_0143.root, FC#0, port D2
Entries 387
Mean 43.82
Std Dev 11.92
Turn on : 25.6123
Width : 4.517
Height : 10.075
Entry
ampl
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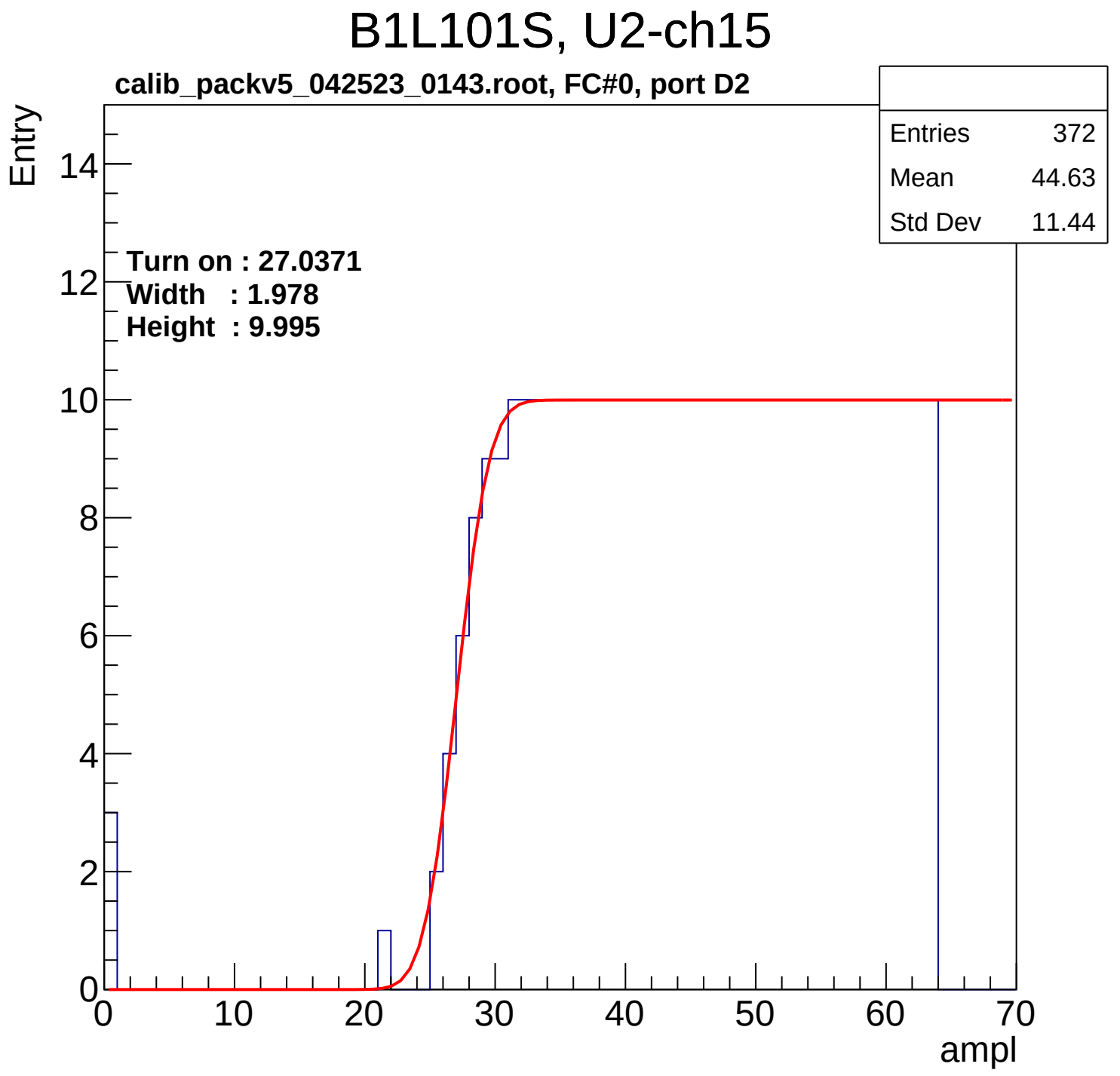
B1L101S, U2-ch15
calib_packv5_042523_0143.root, FC#0, port D2
Entries 372
Mean 44.63
Std Dev 11.44
Turn on : 27.0371
Width : 1.978
Height : 9.995
Entry
ampl
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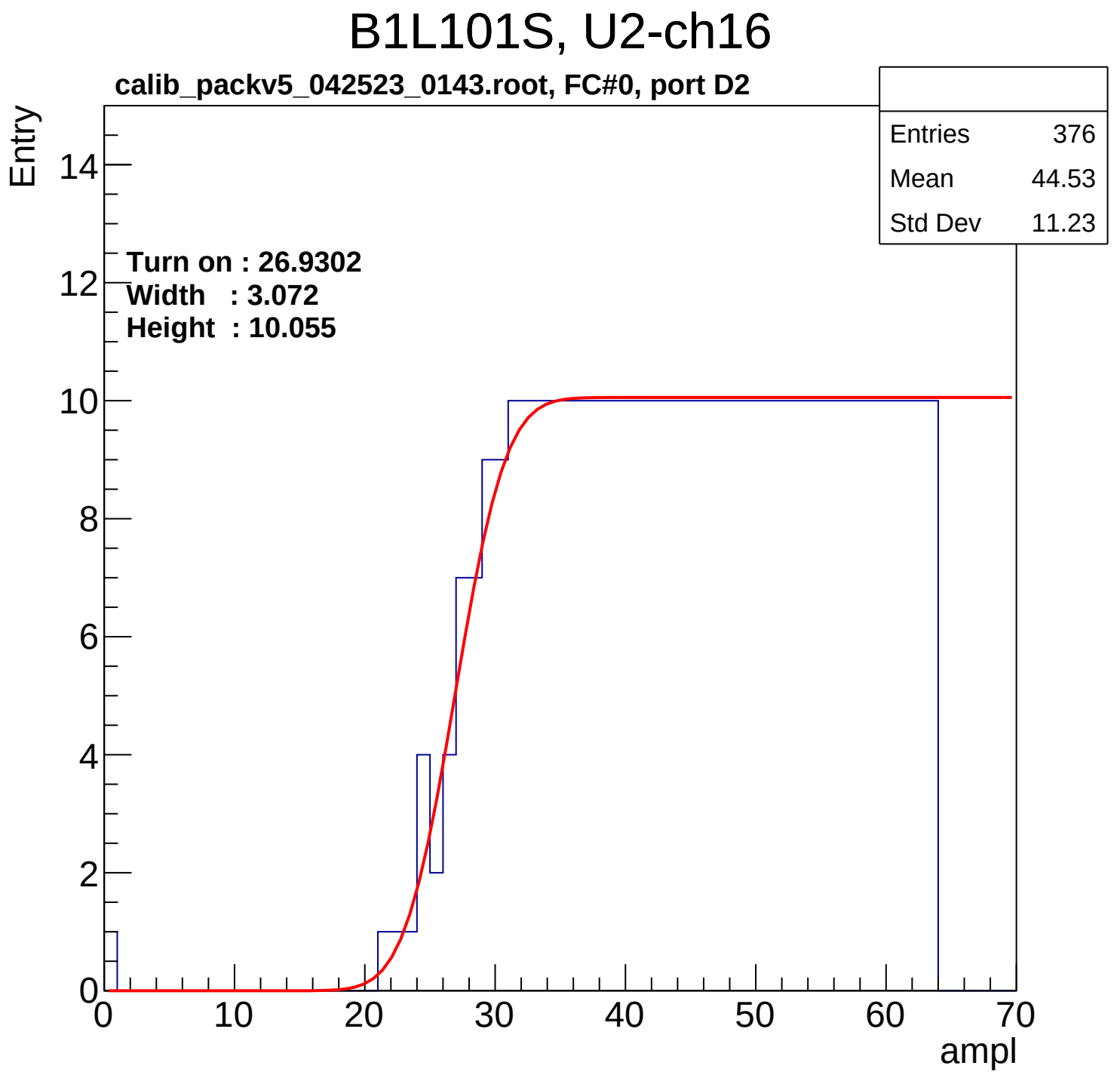
B1L101S, U2-ch16
calib_packv5_042523_0143.root, FC#0, port D2
Entries 376
Mean 44.53
Std Dev 11.23
Turn on : 26.9302
Width : 3.072
Height : 10.055
Entry
ampl
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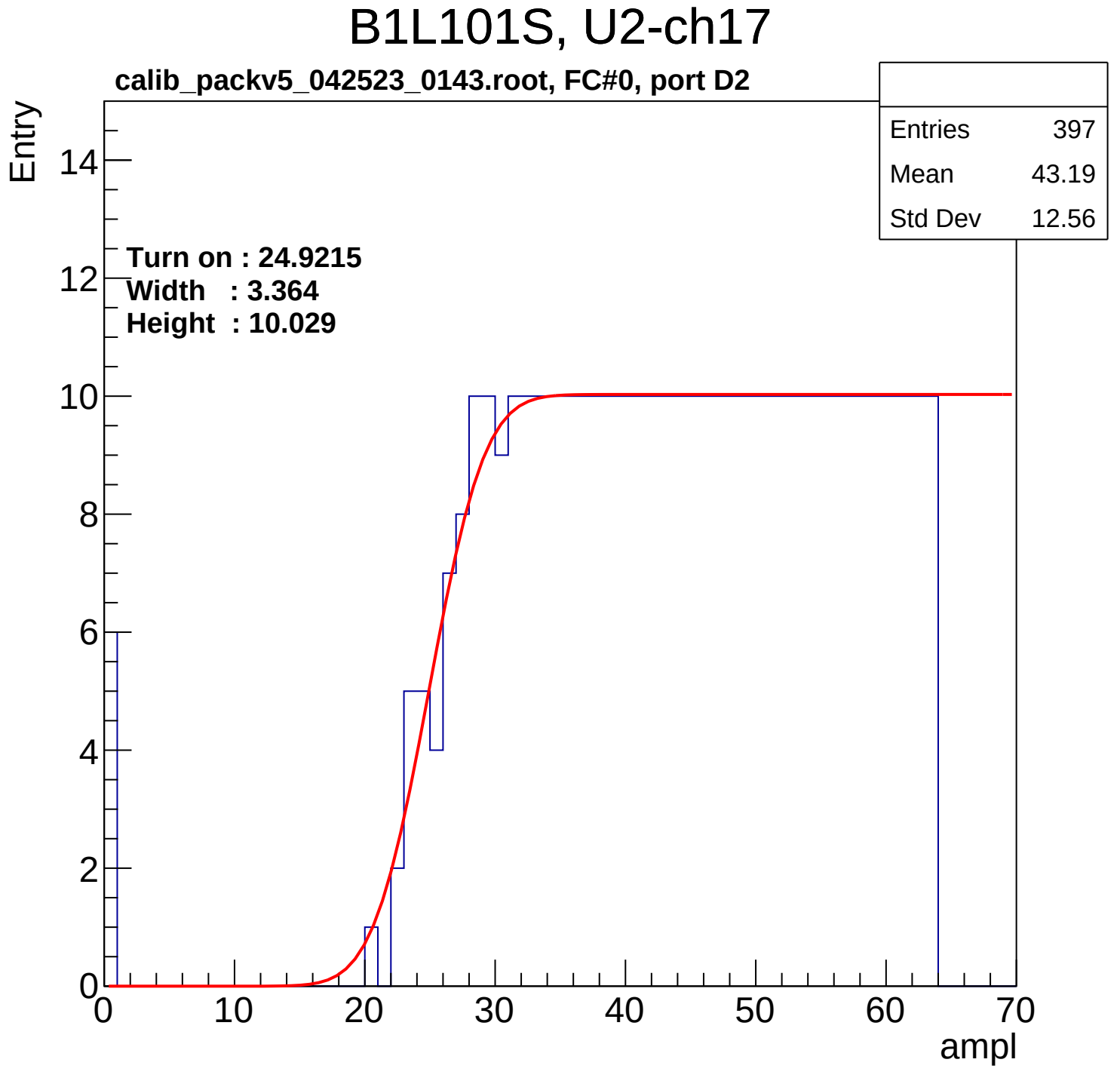
B1L101S, U2-ch17
calib_packv5_042523_0143.root, FC#0, port D2
Entries 397
Mean 43.19
Std Dev 12.56
Turn on : 24.9215
Width : 3.364
Height : 10.029
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ampl
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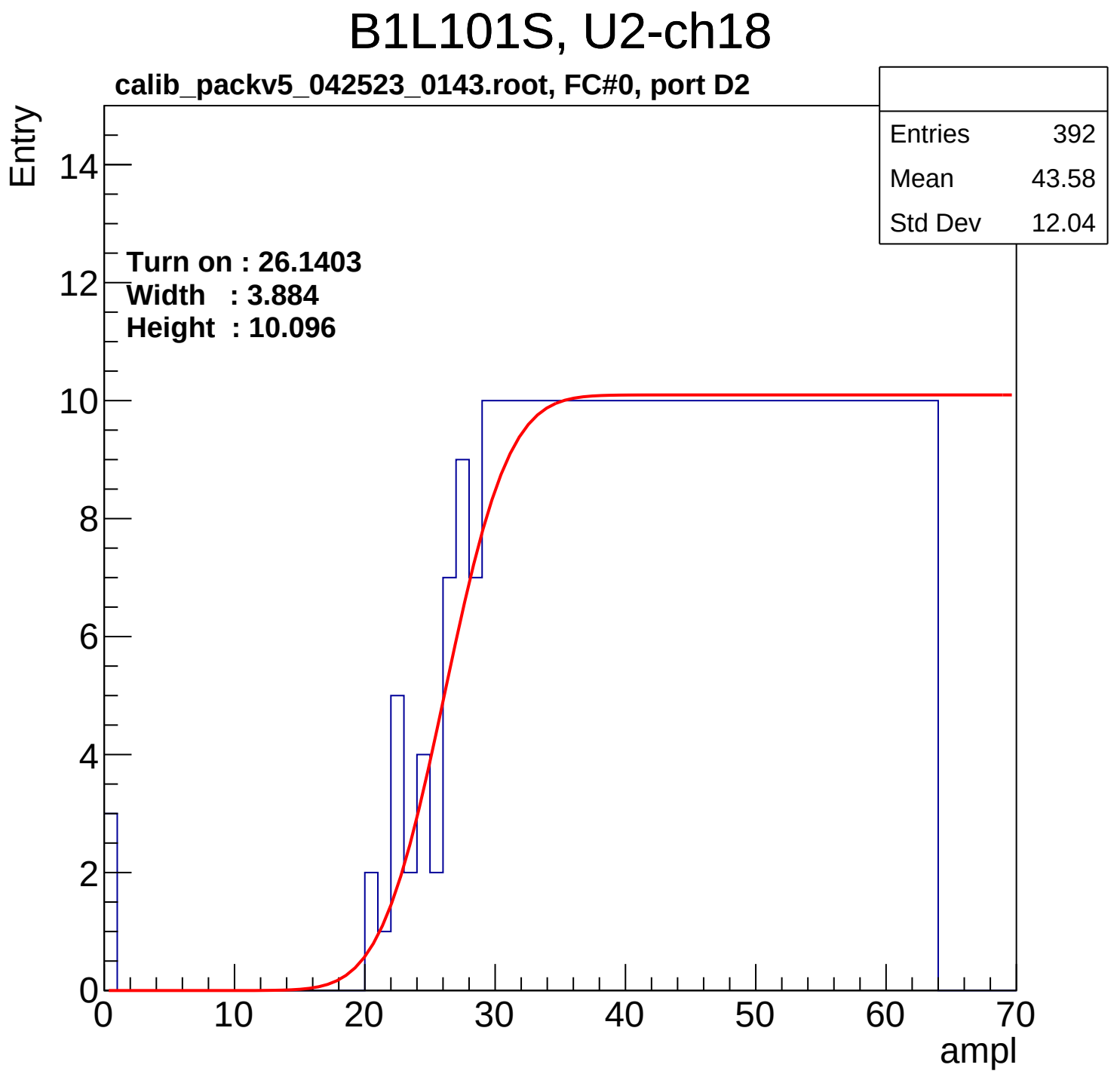
B1L101S, U2-ch18
calib_packv5_042523_0143.root, FC#0, port D2
Entries 392
Mean 43.58
Std Dev 12.04
Turn on : 26.1403
Width : 3.884
Height : 10.096
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ampl
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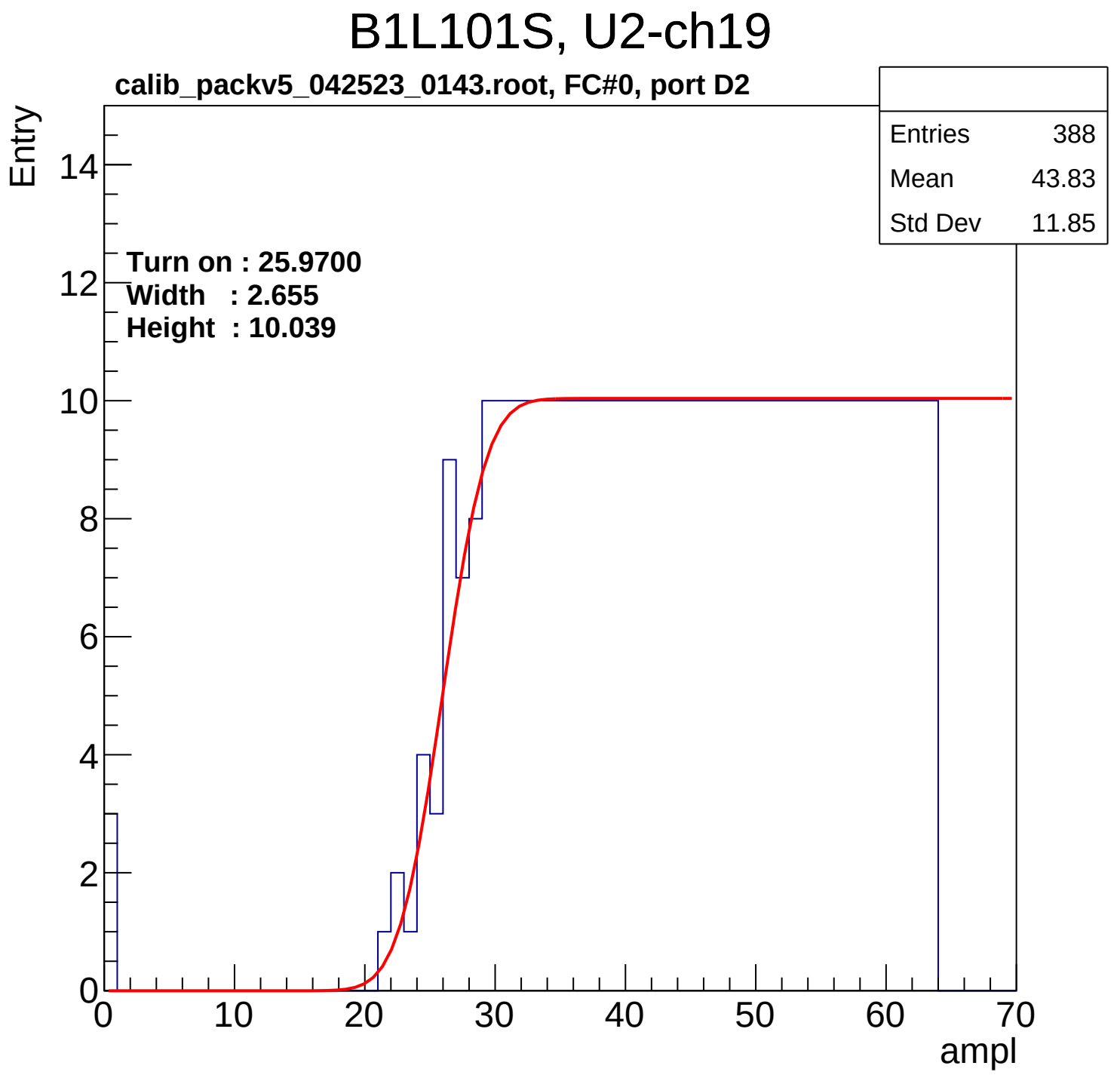
B1L101S, U2-ch19
calib_packv5_042523_0143.root, FC#0, port D2
Entries 388
Mean 43.83
Std Dev 11.85
Turn on : 25.9700
Width : 2.655
Height : 10.039
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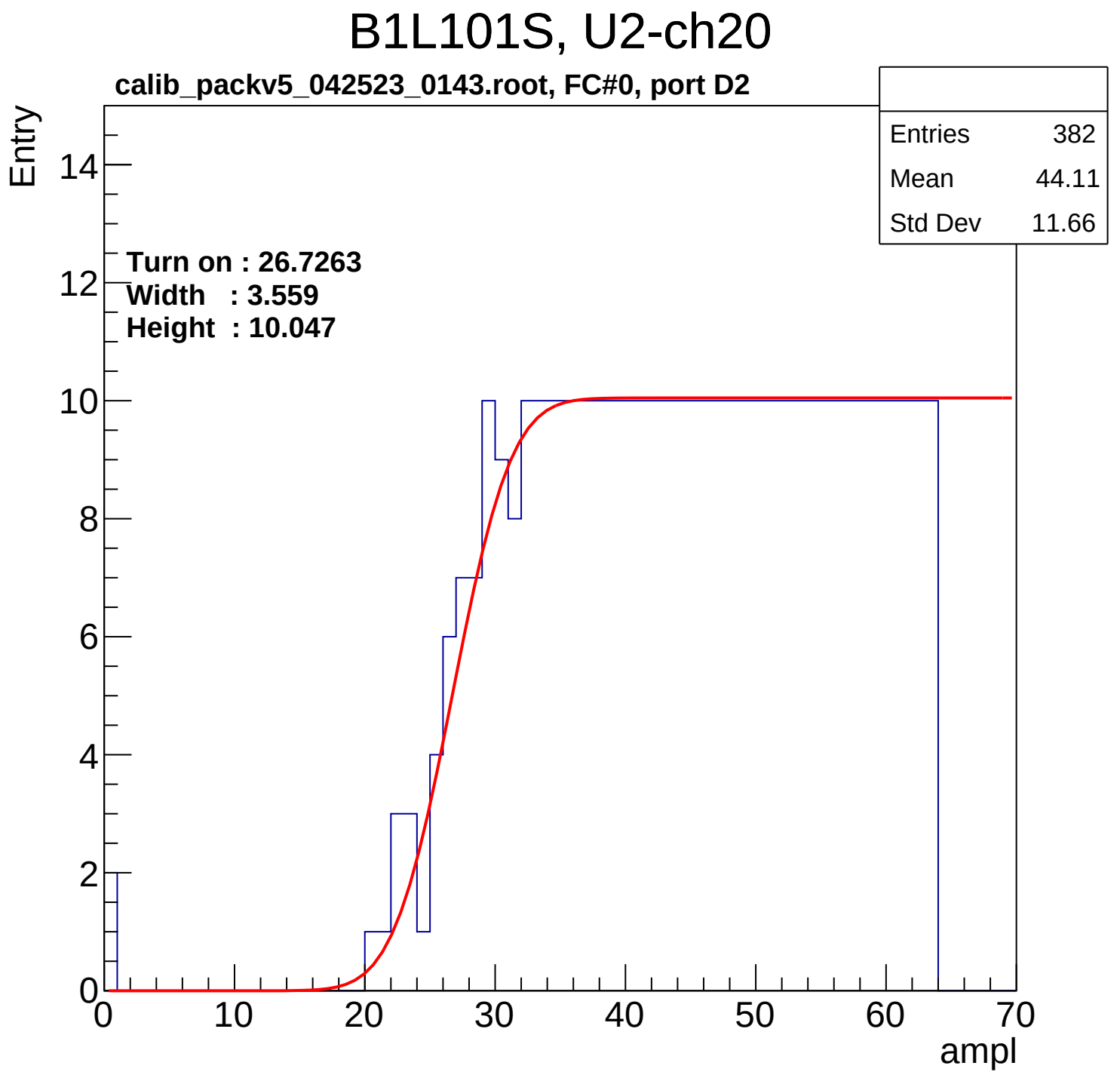
B1L101S, U2-ch20
calib_packv5_042523_0143.root, FC#0, port D2
Entries 382
Mean 44.11
Std Dev 11.66
Turn on : 26.7263
Width : 3.559
Height : 10.047
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ampl
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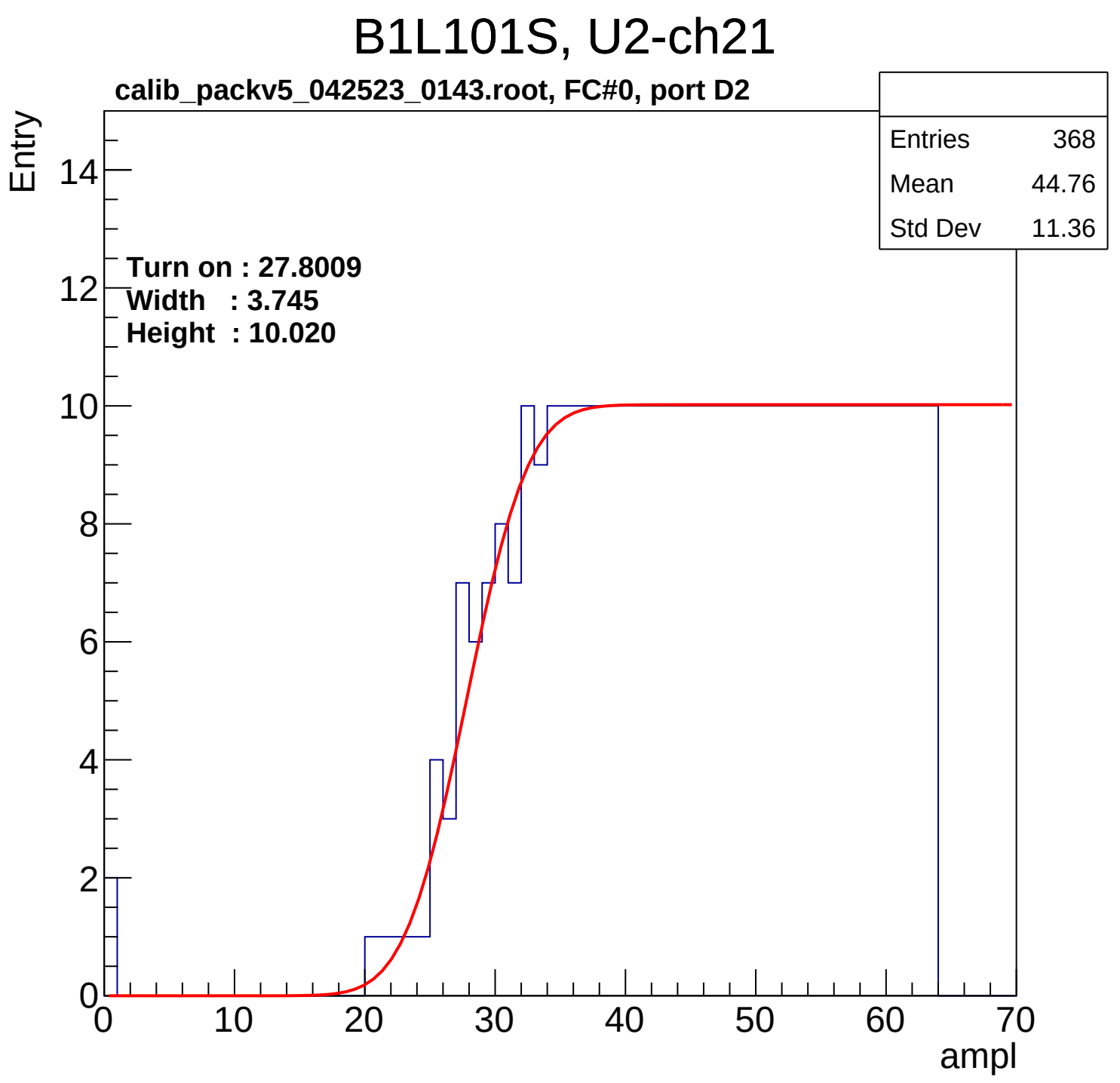
B1L101S, U2-ch21
calib_packv5_042523_0143.root, FC#0, port D2
Entries 368
Mean 44.76
Std Dev 11.36
Turn on : 27.8009
Width : 3.745
Height : 10.020
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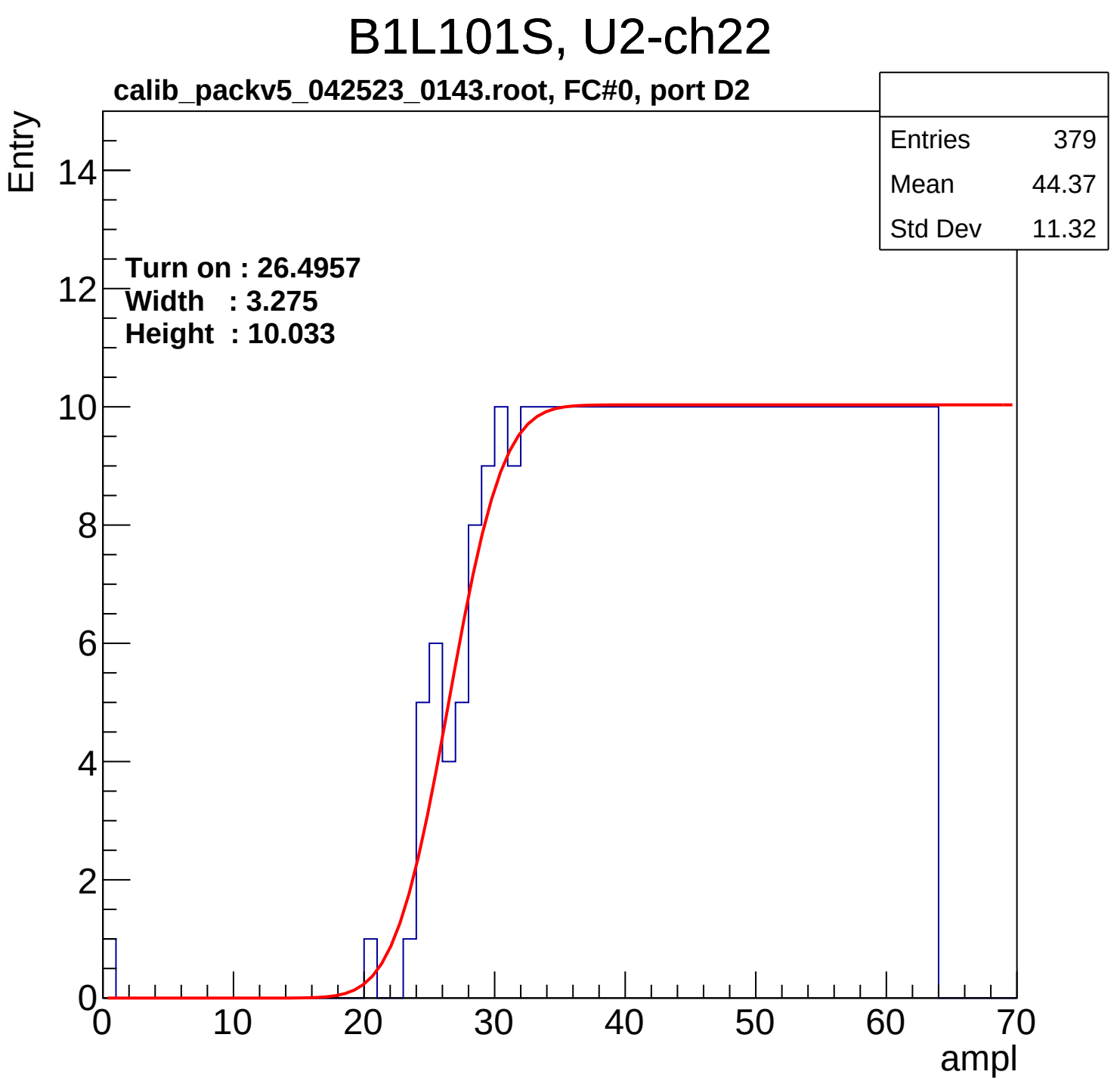
B1L101S, U2-ch22
calib_packv5_042523_0143.root, FC#0, port D2
Entries 379
Mean 44.37
Std Dev 11.32
Turn on : 26.4957
Width : 3.275
Height : 10.033
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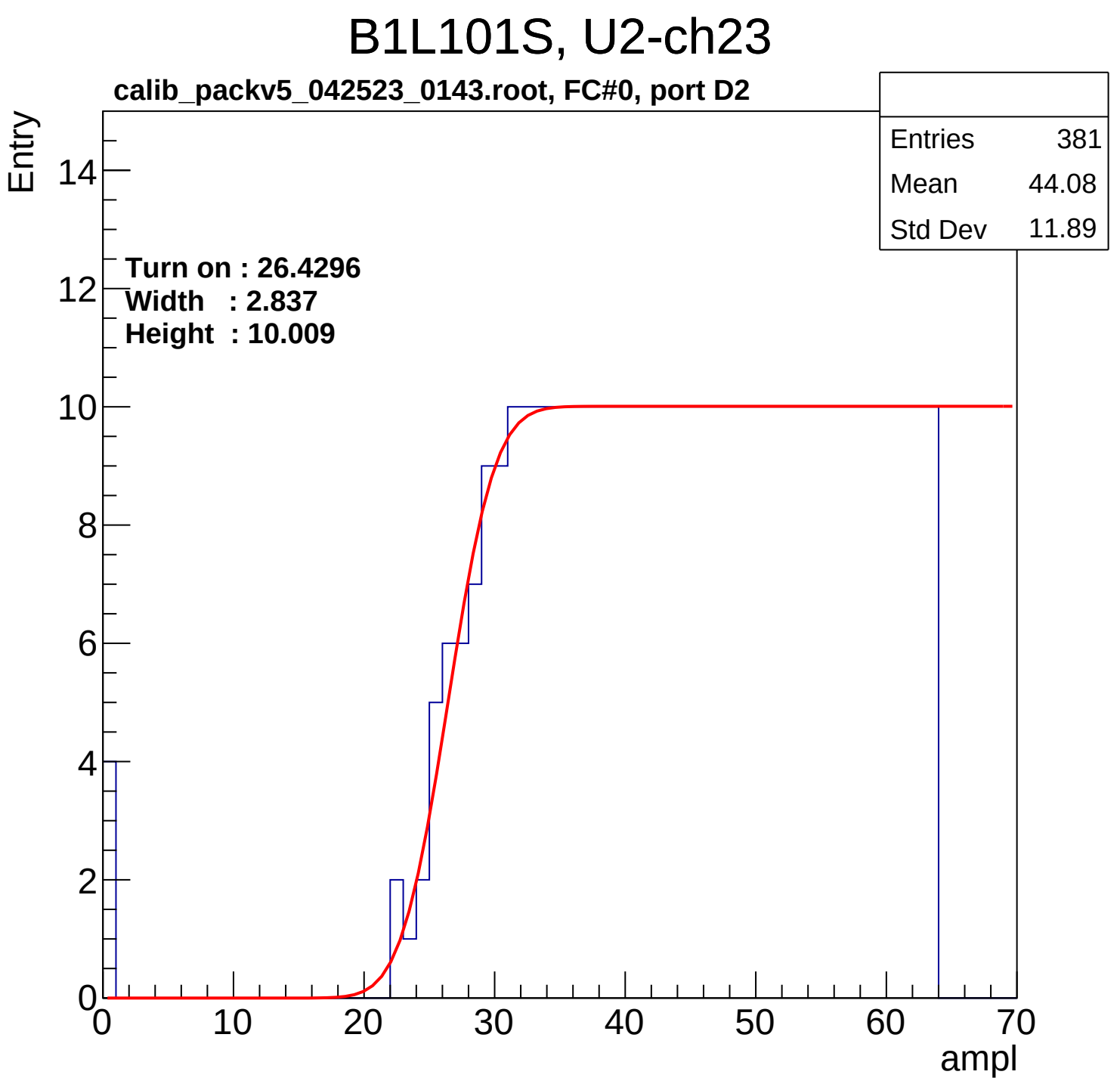
B1L101S, U2-ch23
calib_packv5_042523_0143.root, FC#0, port D2
Entries 381
Mean 44.08
Std Dev 11.89
Turn on : 26.4296
Width : 2.837
Height : 10.009
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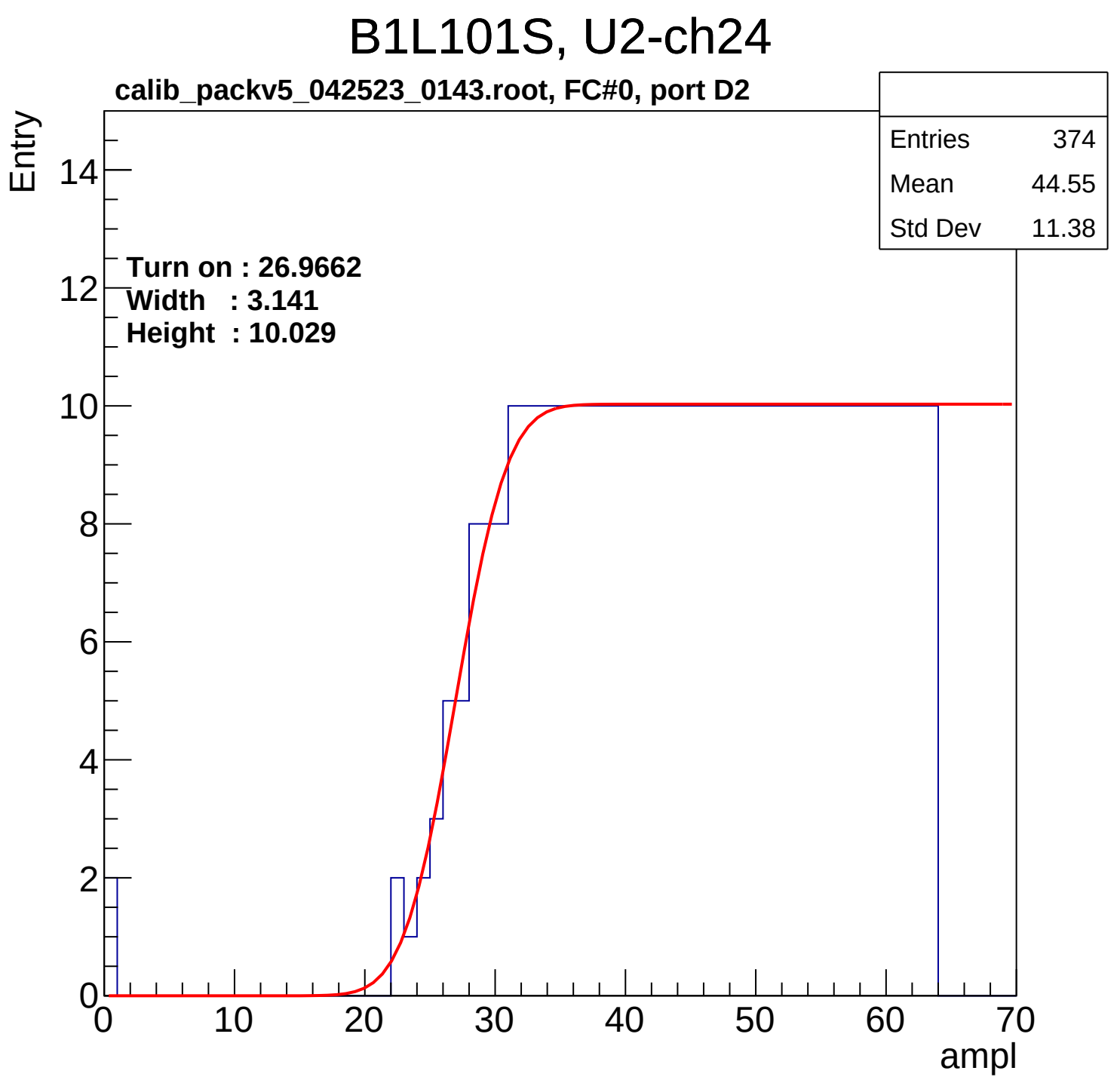
B1L101S, U2-ch24
calib_packv5_042523_0143.root, FC#0, port D2
Entries 374
Mean 44.55
Std Dev 11.38
Turn on : 26.9662
Width : 3.141
Height : 10.029
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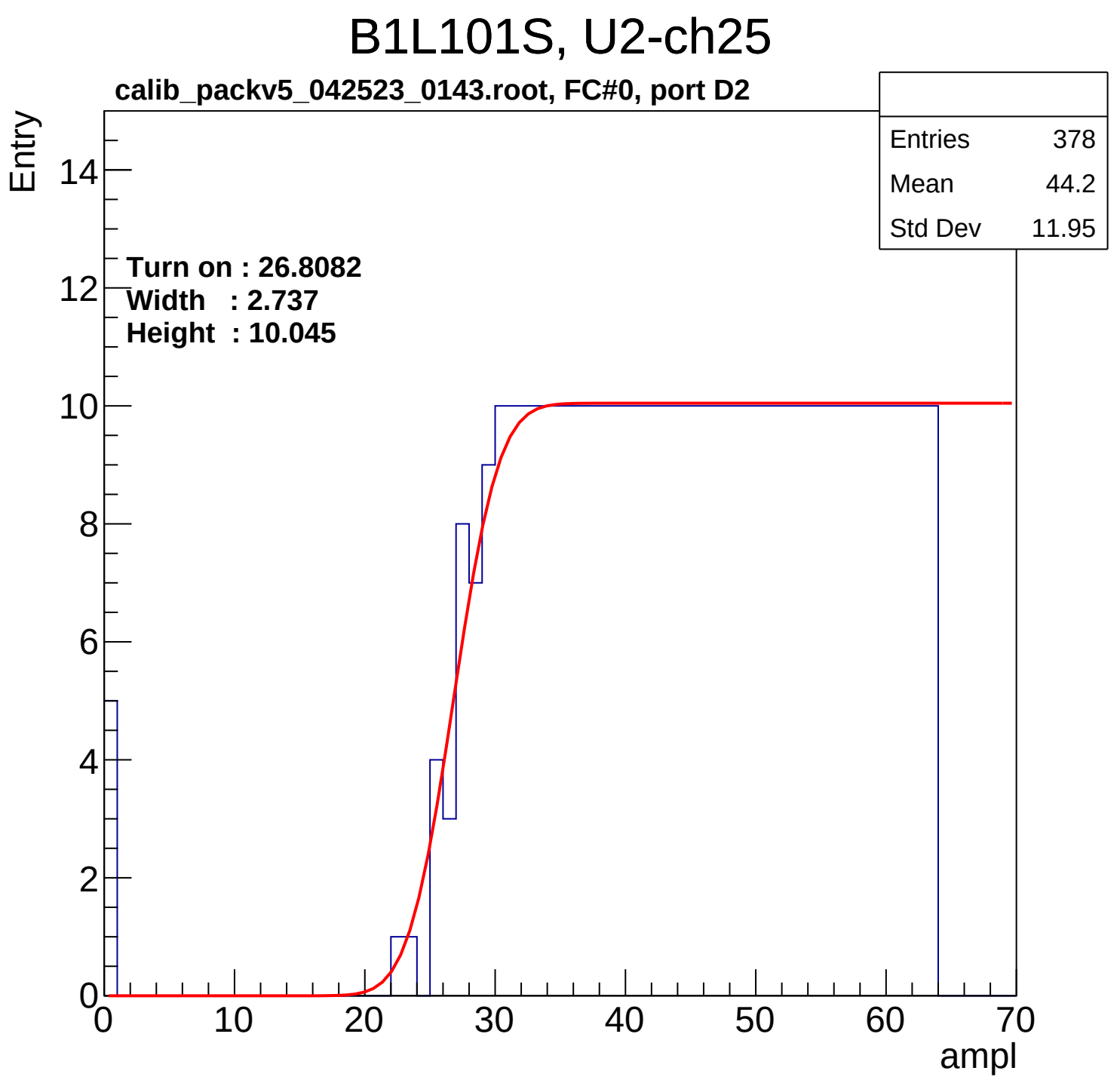
B1L101S, U2-ch25
calib_packv5_042523_0143.root, FC#0, port D2
Entries 378
Mean 44.2
Std Dev 11.95
Turn on : 26.8082
Width : 2.737
Height : 10.045
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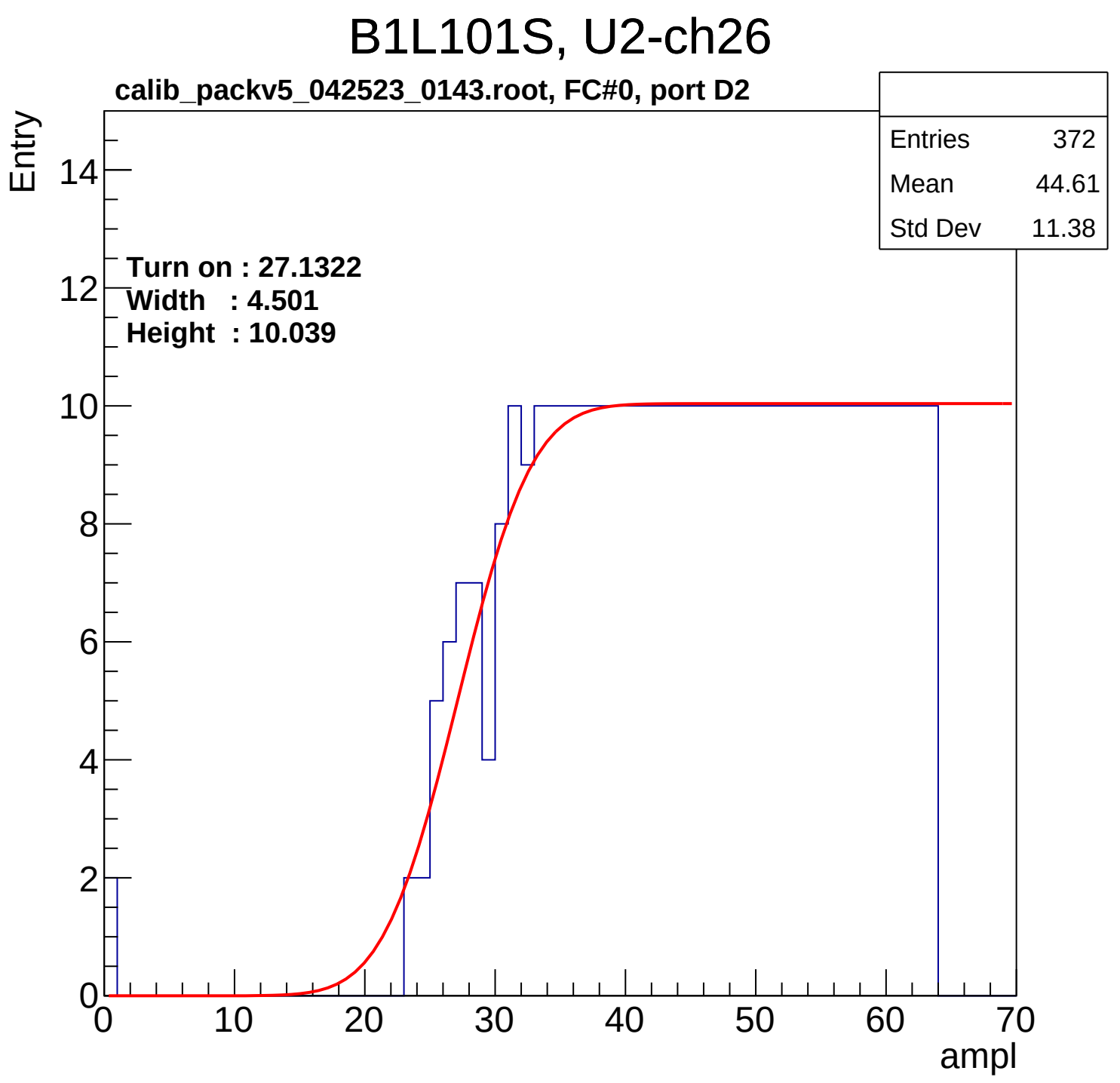
B1L101S, U2-ch26
calib_packv5_042523_0143.root, FC#0, port D2
Entries 372
Mean 44.61
Std Dev 11.38
Turn on : 27.1322
Width : 4.501
Height : 10.039
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ampl
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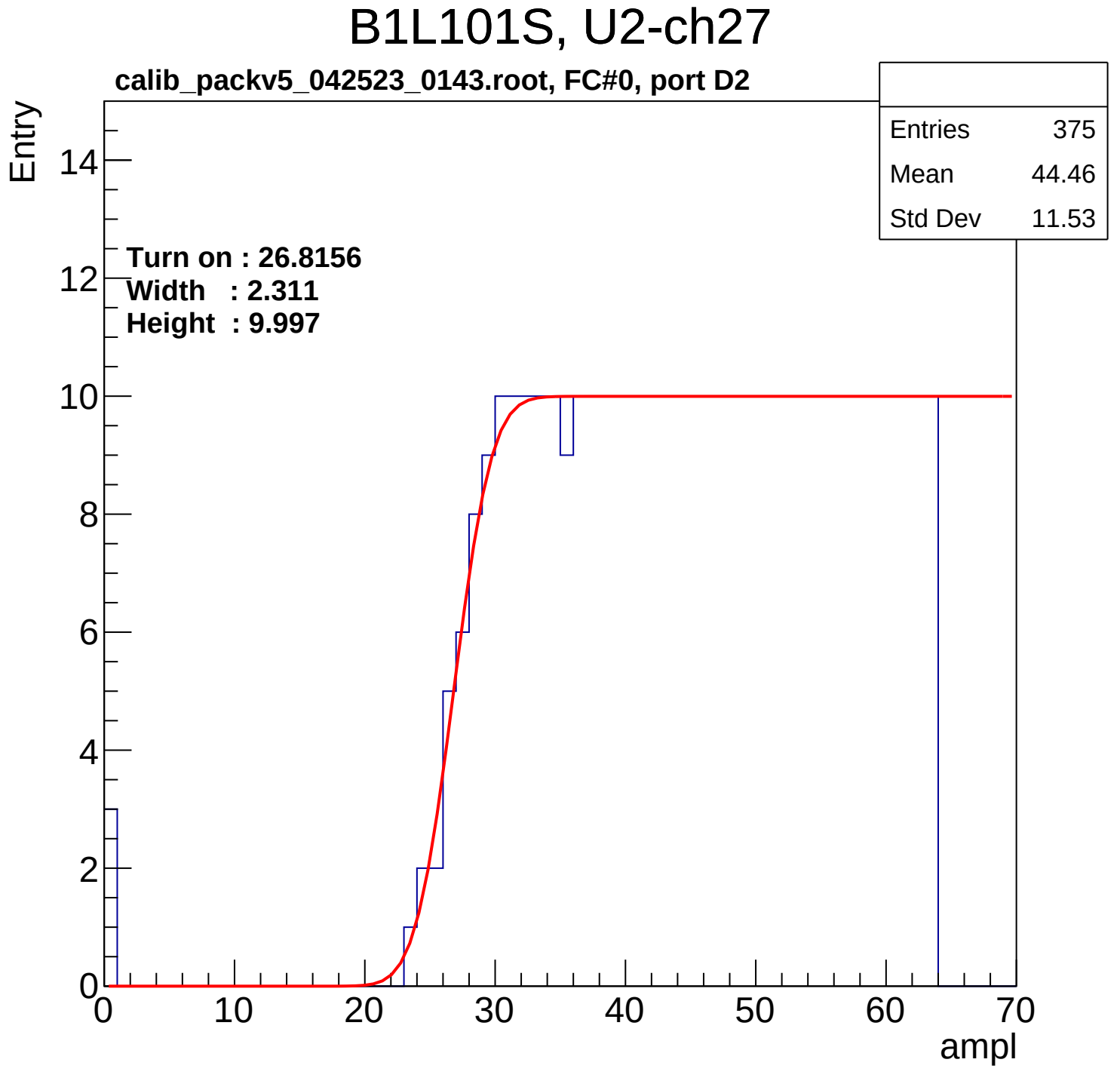
B1L101S, U2-ch27
calib_packv5_042523_0143.root, FC#0, port D2
Entries 375
Mean 44.46
Std Dev 11.53
Turn on : 26.8156
Width : 2.311
Height : 9.997
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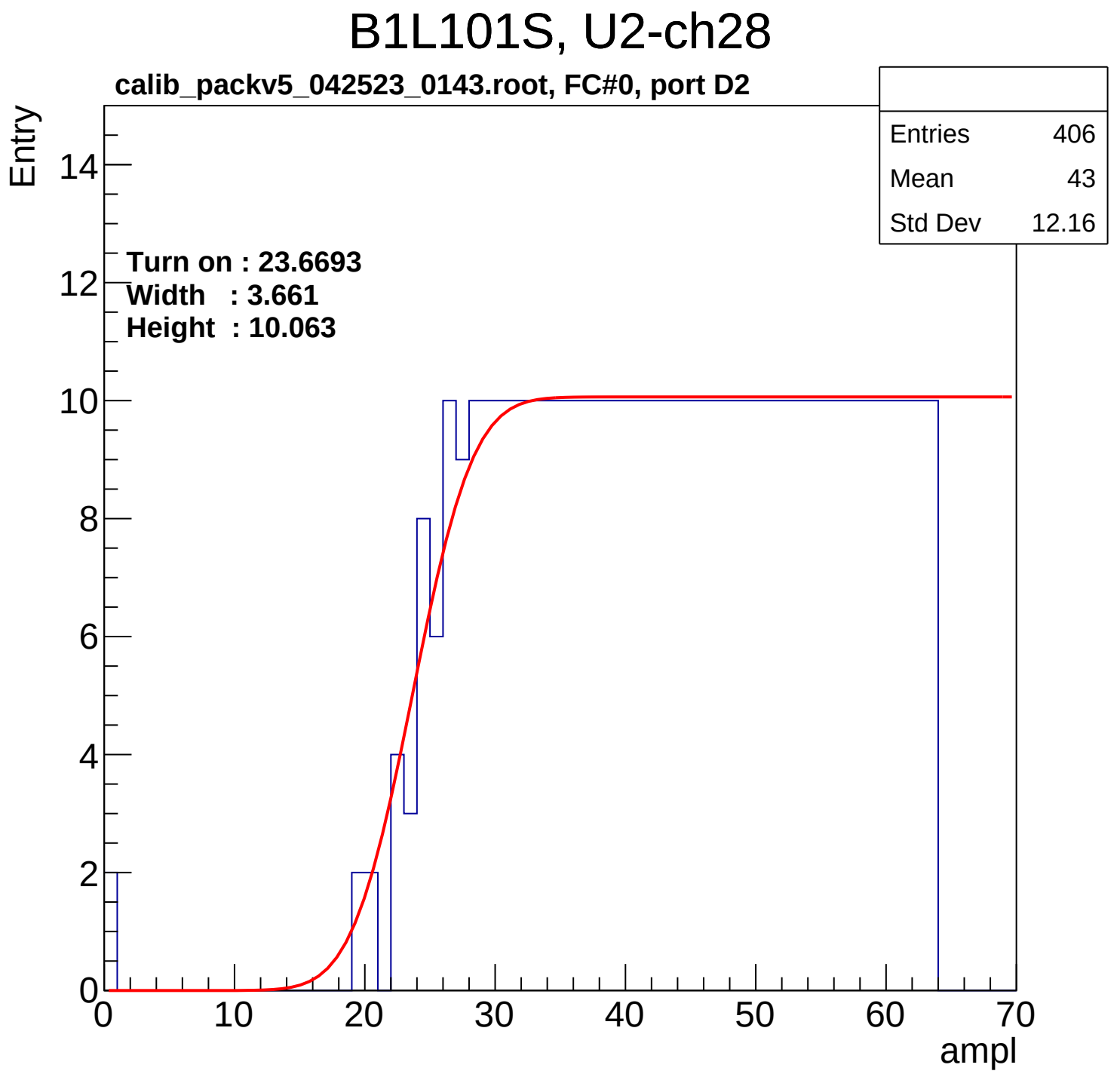
B1L101S, U2-ch28
calib_packv5_042523_0143.root, FC#0, port D2
Entries 406
Mean 43
Std Dev 12.16
Turn on : 23.6693
Width : 3.661
Height : 10.063
Entry
ampl
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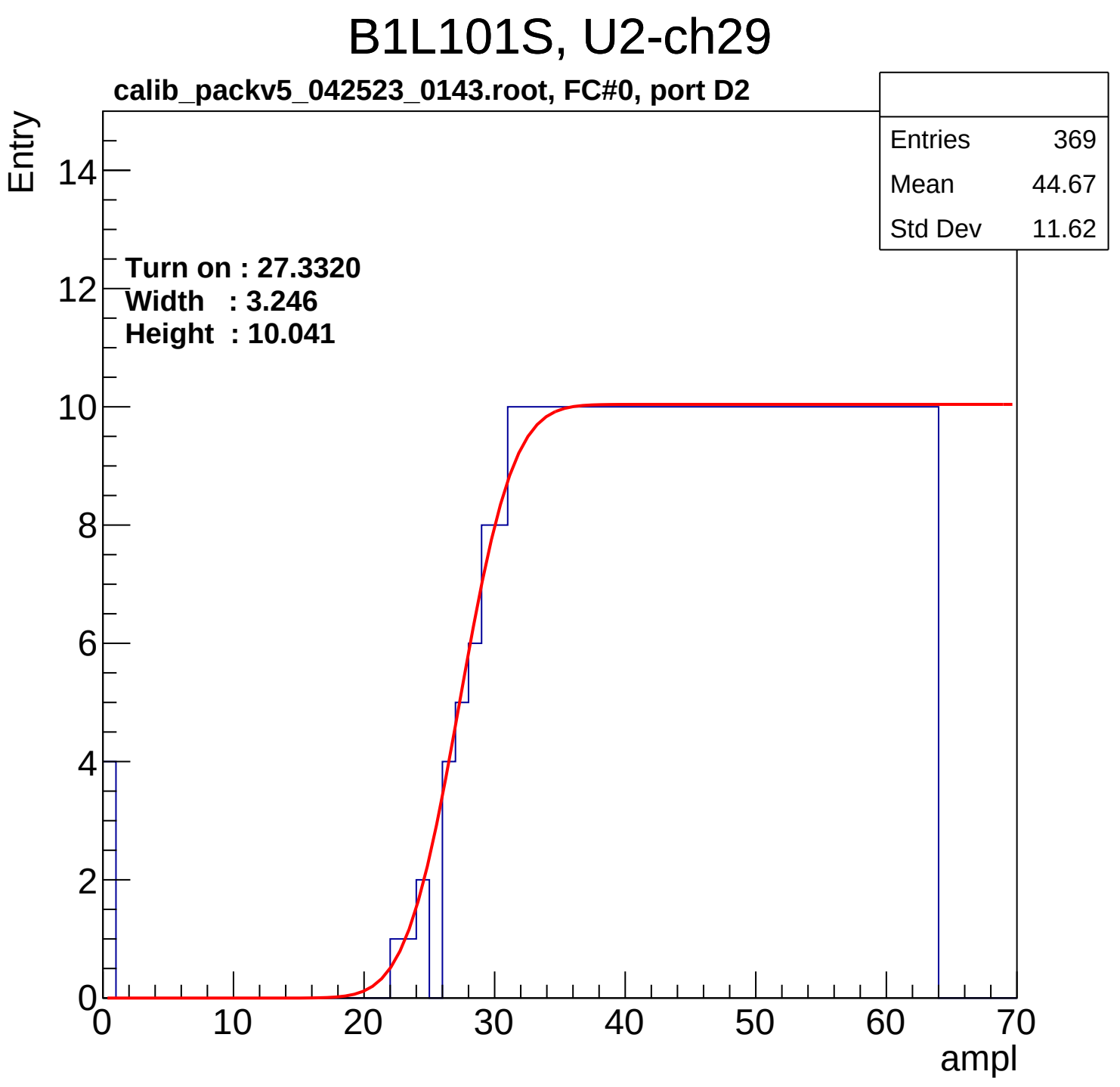
B1L101S, U2-ch29
calib_packv5_042523_0143.root, FC#0, port D2
Entries 369
Mean 44.67
Std Dev 11.62
Turn on : 27.3320
Width : 3.246
Height : 10.041
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ampl
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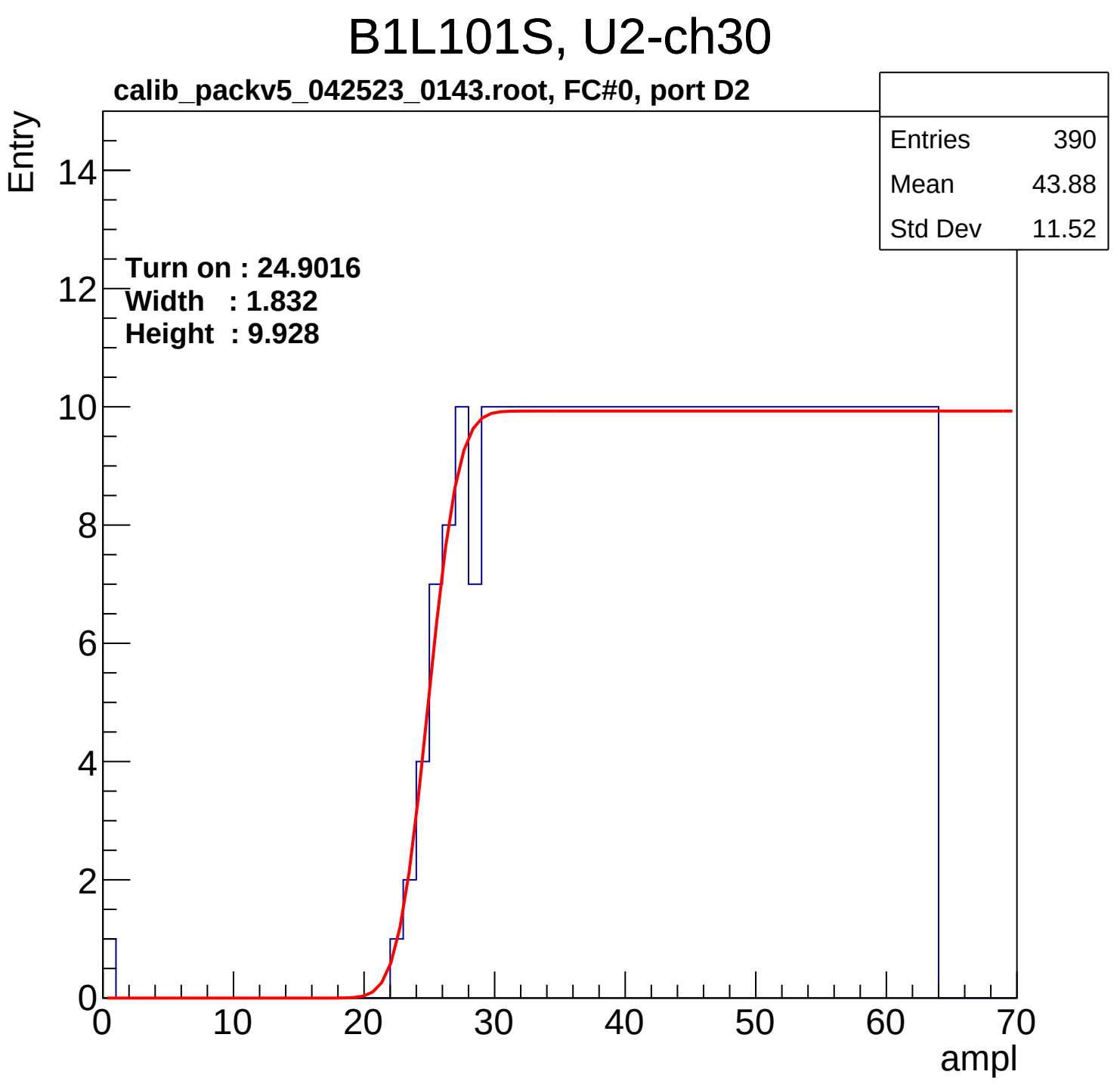
B1L101S, U2-ch30
calib_packv5_042523_0143.root, FC#0, port D2
Entries 390
Mean 43.88
Std Dev 11.52
Turn on : 24.9016
Width : 1.832
Height : 9.928
Entry
ampl
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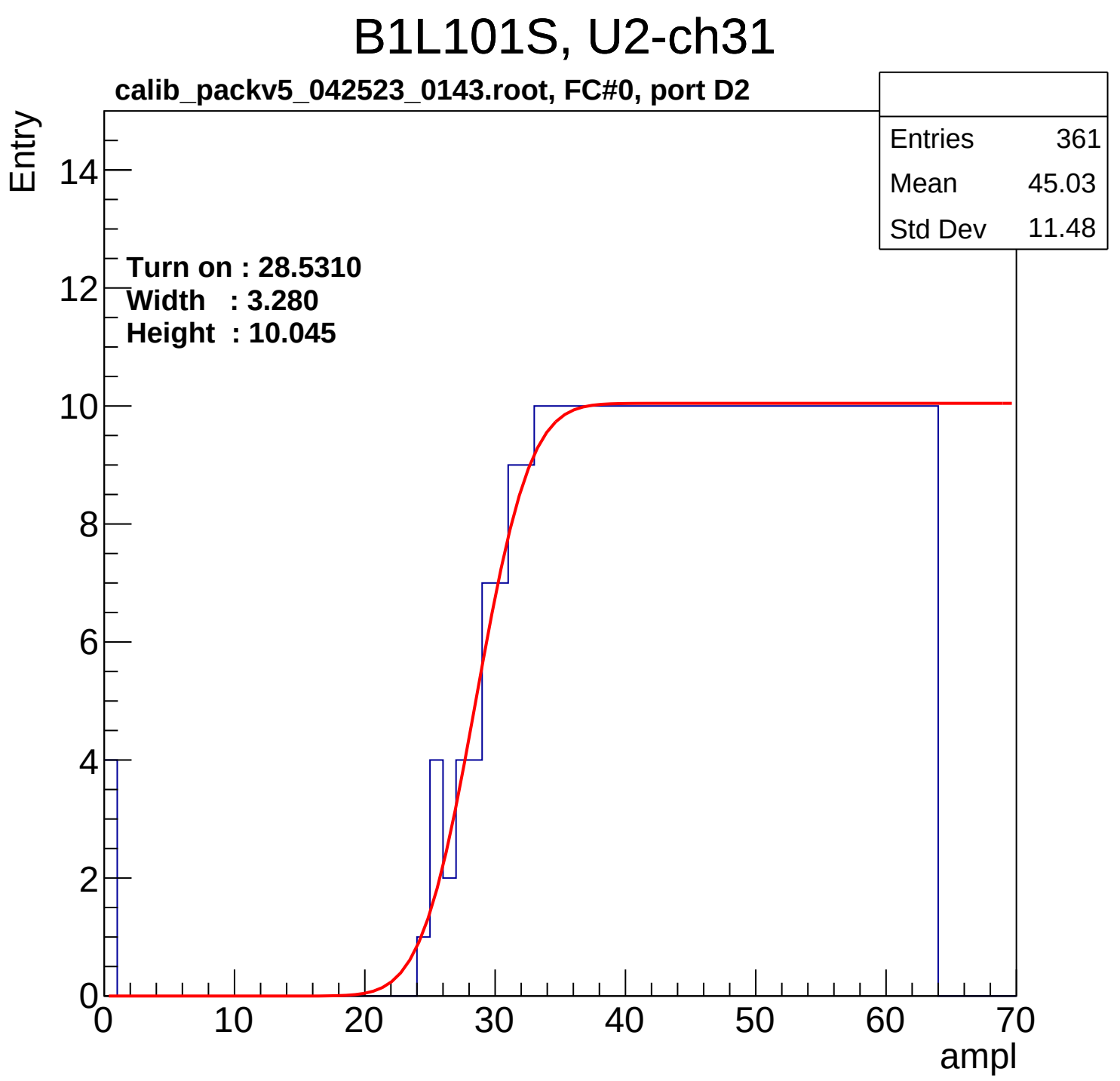
B1L101S, U2-ch31
calib_packv5_042523_0143.root, FC#0, port D2
Entries 361
Mean 45.03
Std Dev 11.48
Turn on : 28.5310
Width : 3.280
Height : 10.045
Entry
ampl
0
2
4
6
8
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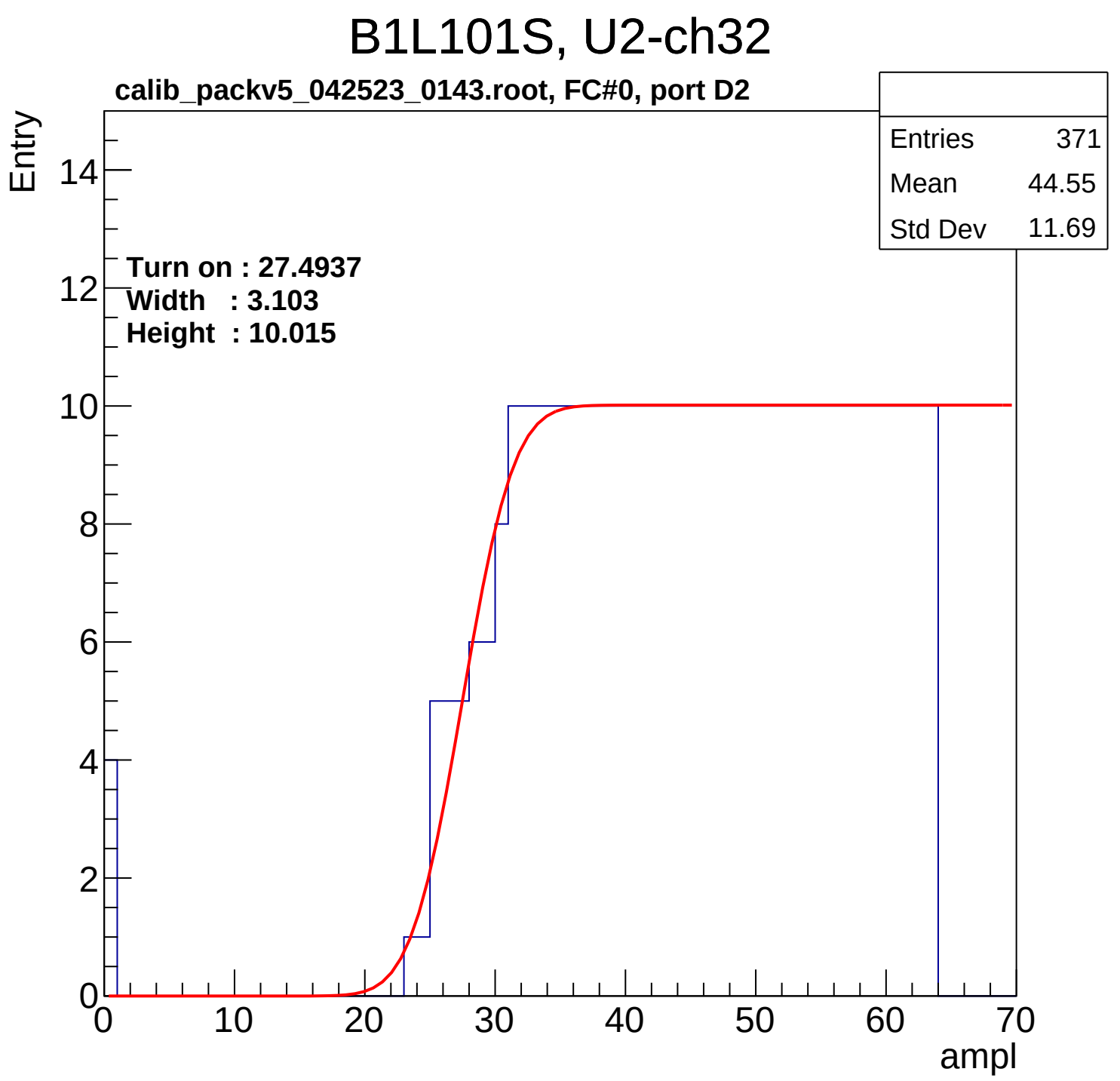
B1L101S, U2-ch32
calib_packv5_042523_0143.root, FC#0, port D2
Entries 371
Mean 44.55
Std Dev 11.69
Turn on : 27.4937
Width : 3.103
Height : 10.015
Entry
ampl
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2
4
6
8
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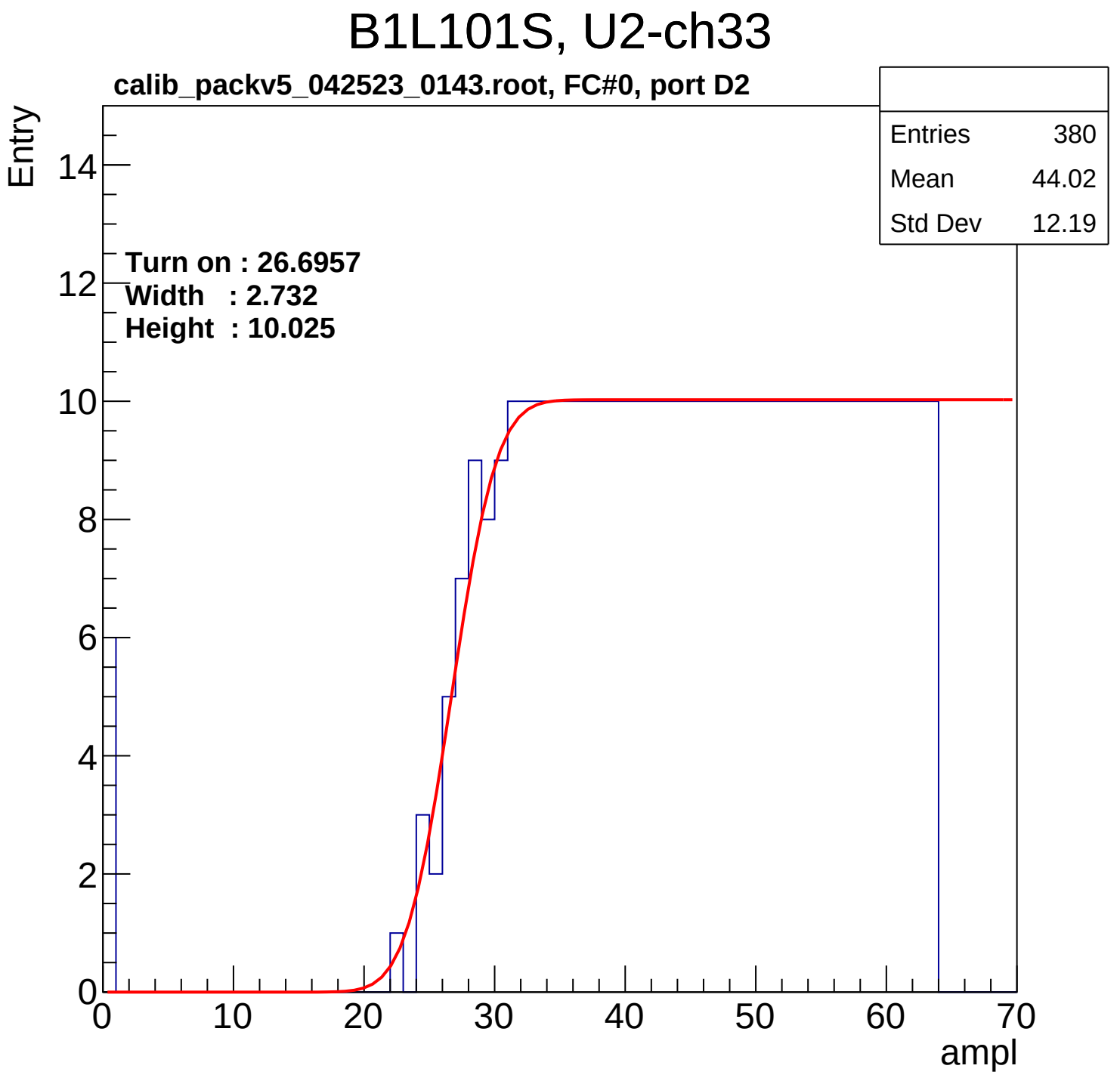
B1L101S, U2-ch33
calib_packv5_042523_0143.root, FC#0, port D2
Entries 380
Mean 44.02
Std Dev 12.19
Turn on : 26.6957
Width : 2.732
Height : 10.025
Entry
ampl
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2
4
6
8
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12
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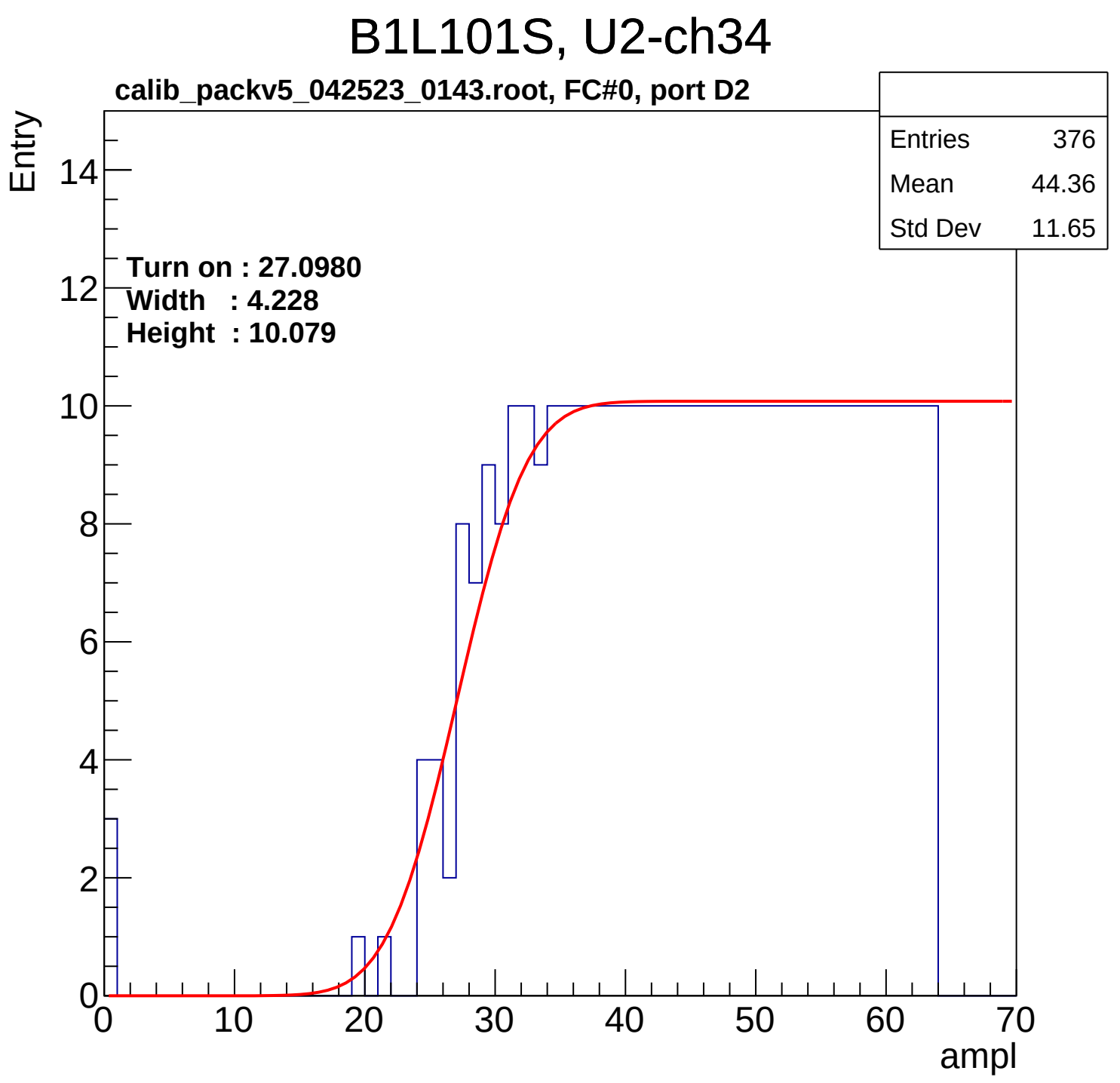
B1L101S, U2-ch34
calib_packv5_042523_0143.root, FC#0, port D2
Entries 376
Mean 44.36
Std Dev 11.65
Turn on : 27.0980
Width : 4.228
Height : 10.079
Entry
ampl
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2
4
6
8
10
12
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0
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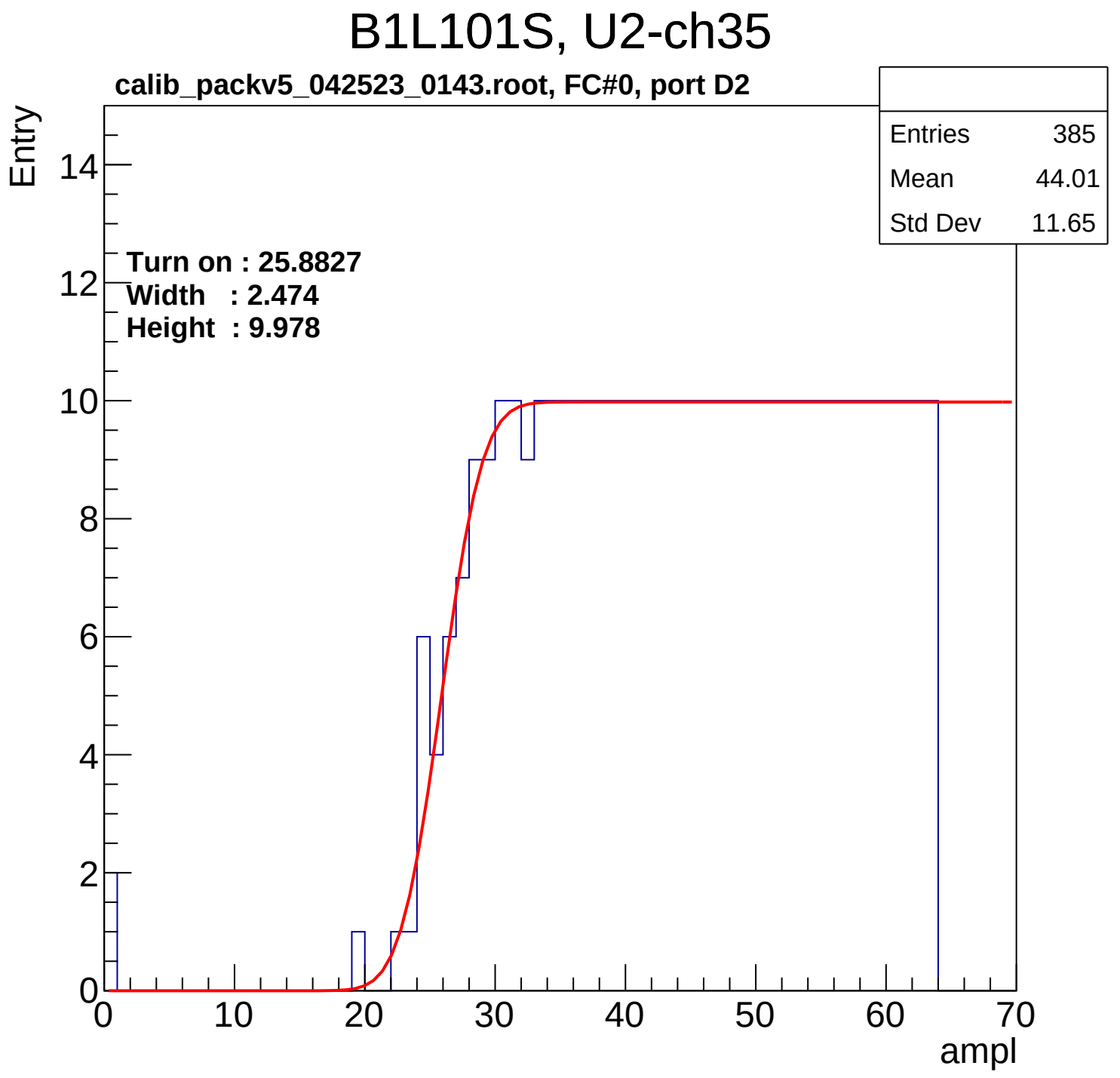
B1L101S, U2-ch35
calib_packv5_042523_0143.root, FC#0, port D2
Entries 385
Mean 44.01
Std Dev 11.65
Turn on : 25.8827
Width : 2.474
Height : 9.978
Entry
ampl
0
2
4
6
8
10
12
14
0
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60
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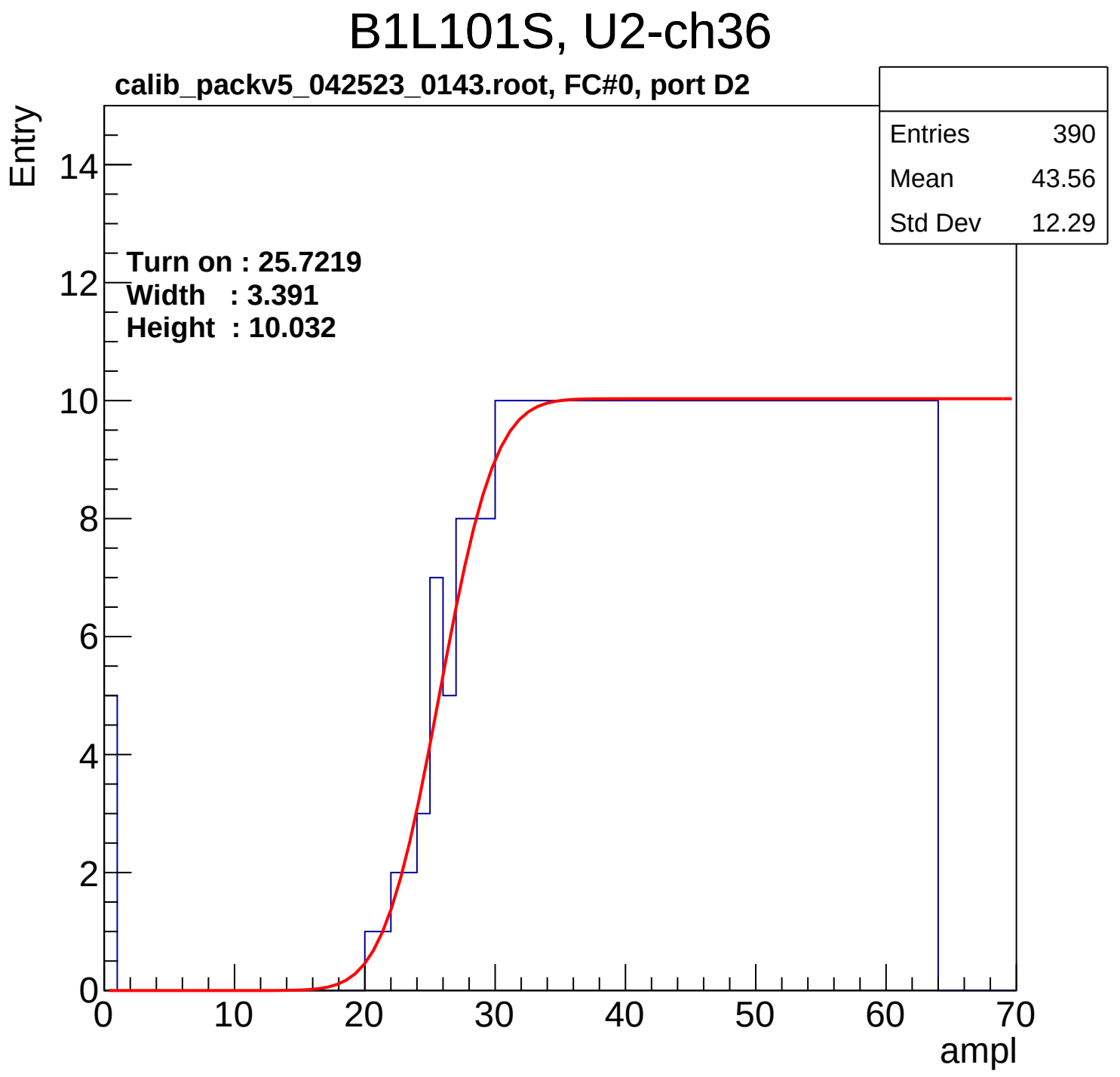
B1L101S, U2-ch36
calib_packv5_042523_0143.root, FC#0, port D2
Entries 390
Mean 43.56
Std Dev 12.29
Turn on : 25.7219
Width : 3.391
Height : 10.032
Entry
ampl
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2
4
6
8
10
12
14
0
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60
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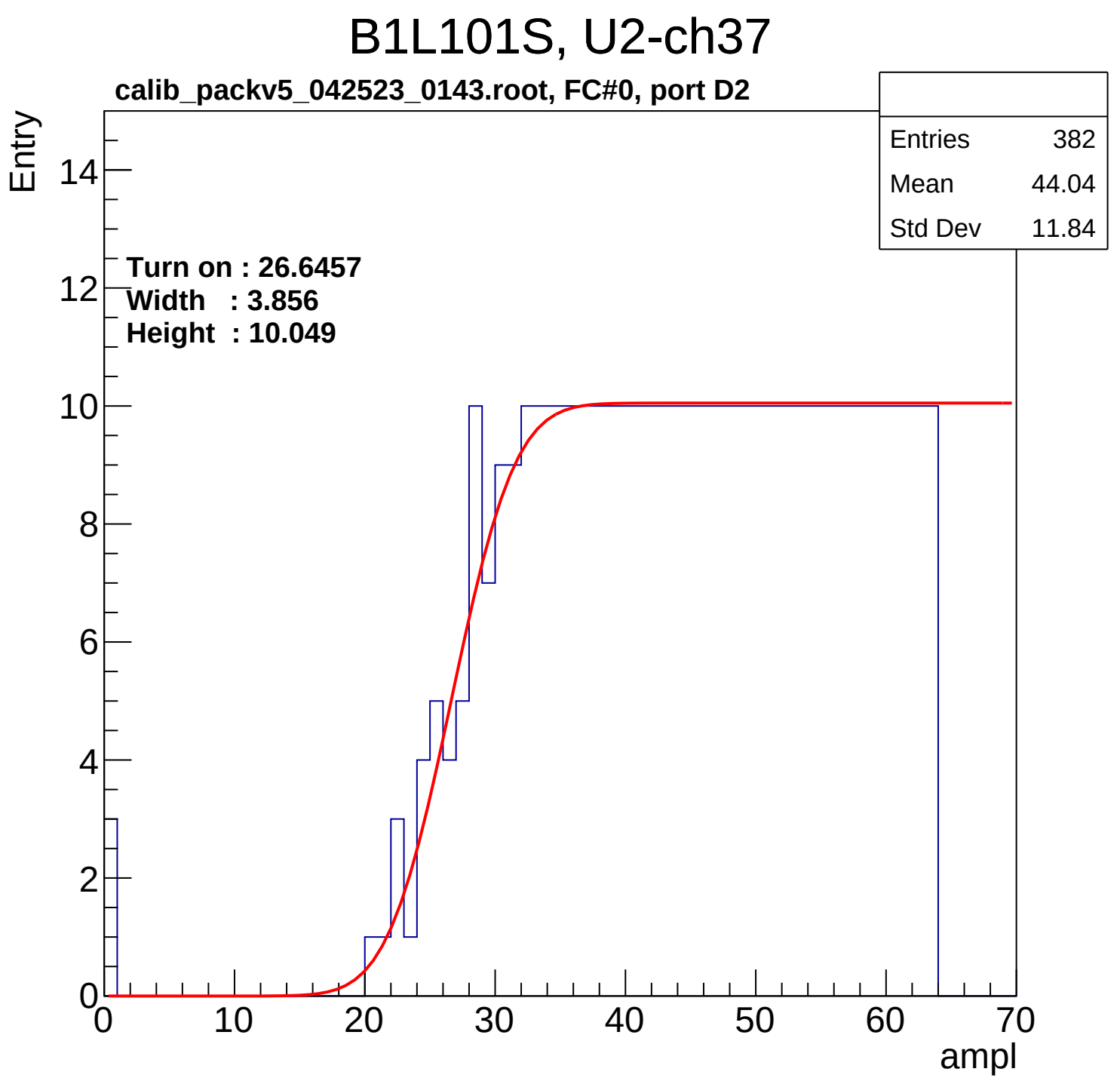
B1L101S, U2-ch37
calib_packv5_042523_0143.root, FC#0, port D2
Entries 382
Mean 44.04
Std Dev 11.84
Turn on : 26.6457
Width : 3.856
Height : 10.049
Entry
ampl
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4
6
8
10
12
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0
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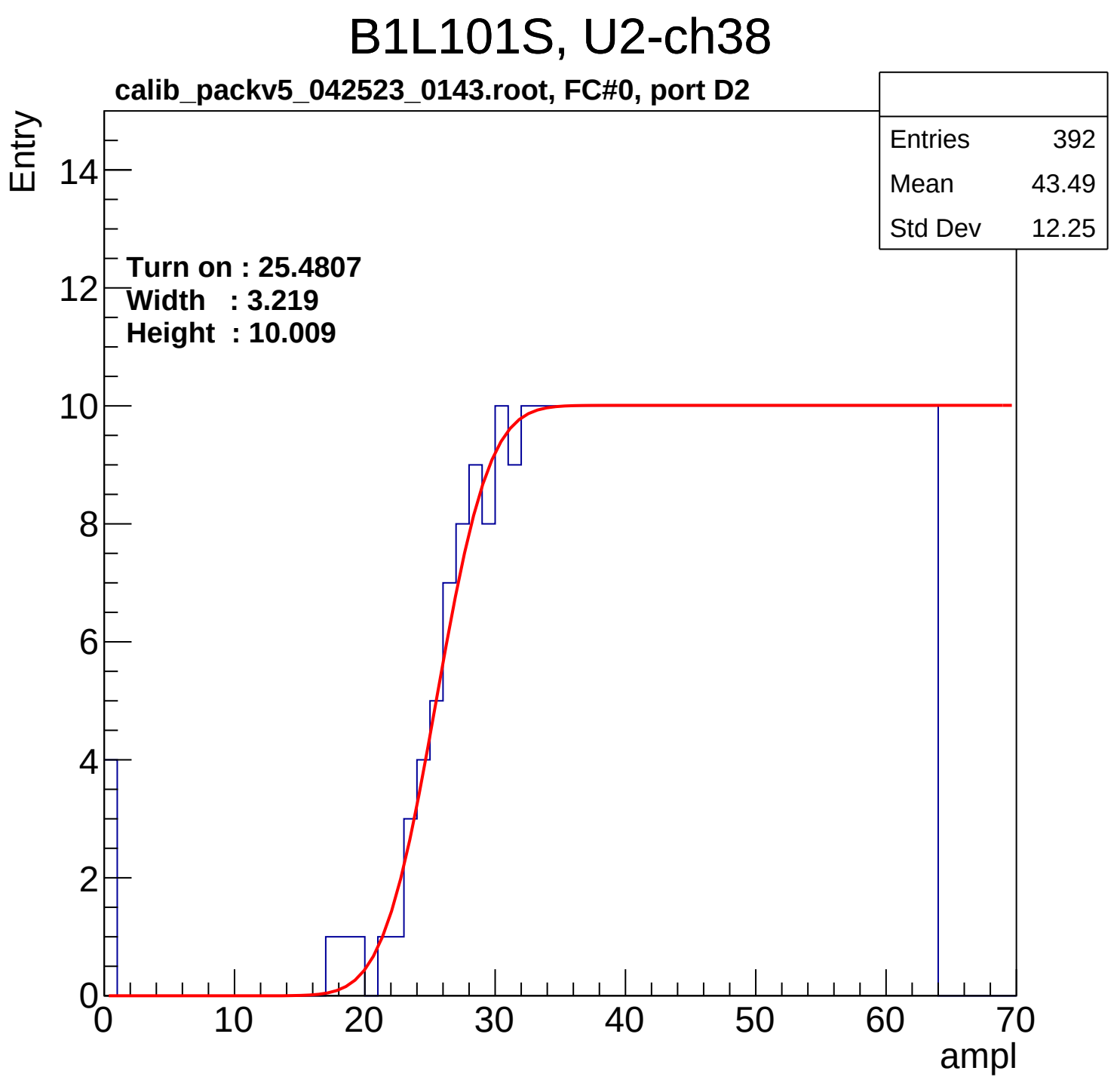
B1L101S, U2-ch38
calib_packv5_042523_0143.root, FC#0, port D2
Entries 392
Mean 43.49
Std Dev 12.25
Turn on : 25.4807
Width : 3.219
Height : 10.009
Entry
ampl
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6
8
10
12
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0
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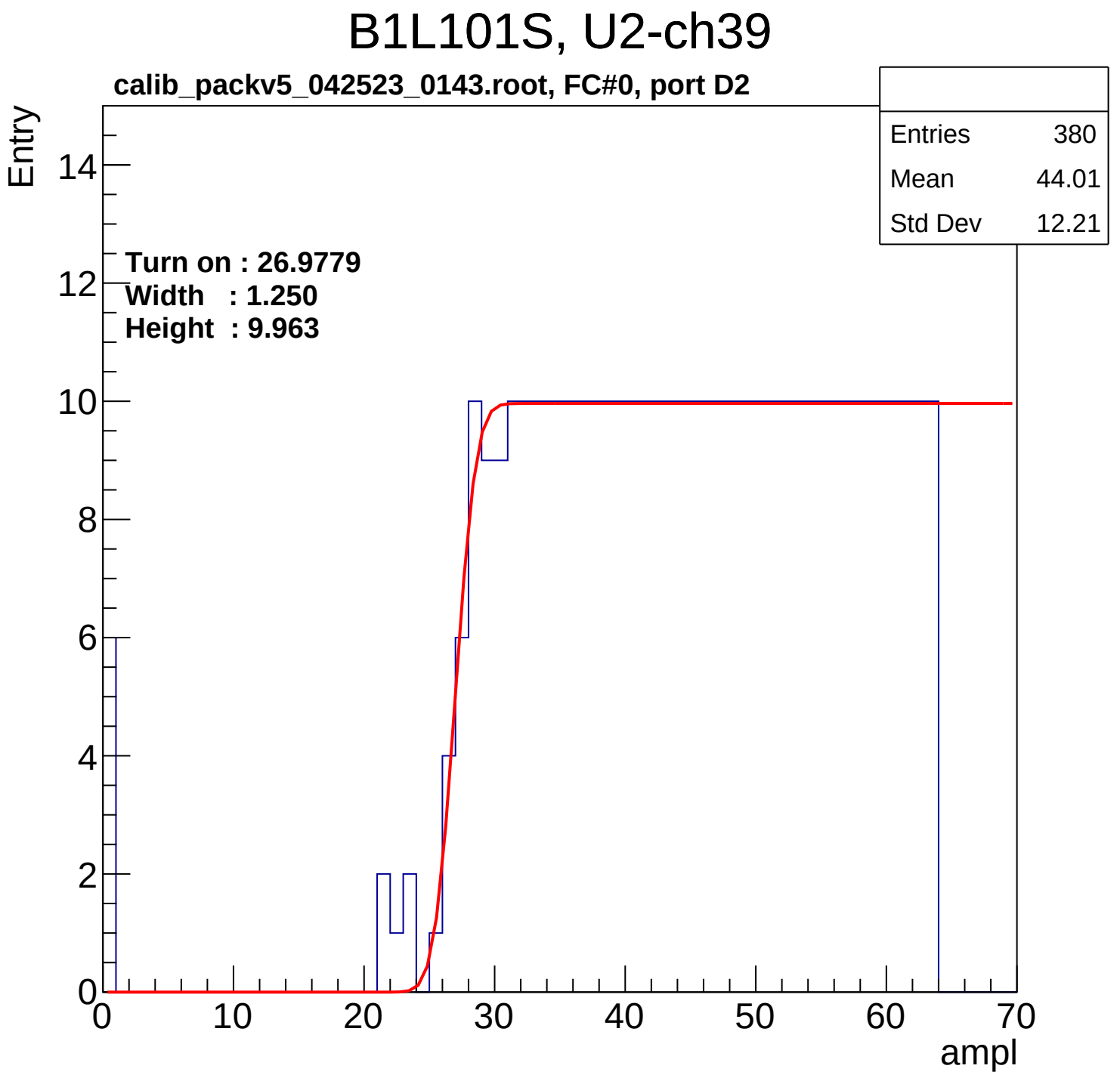
B1L101S, U2-ch39
calib_packv5_042523_0143.root, FC#0, port D2
Entries 380
Mean 44.01
Std Dev 12.21
Turn on : 26.9779
Width : 1.250
Height : 9.963
Entry
ampl
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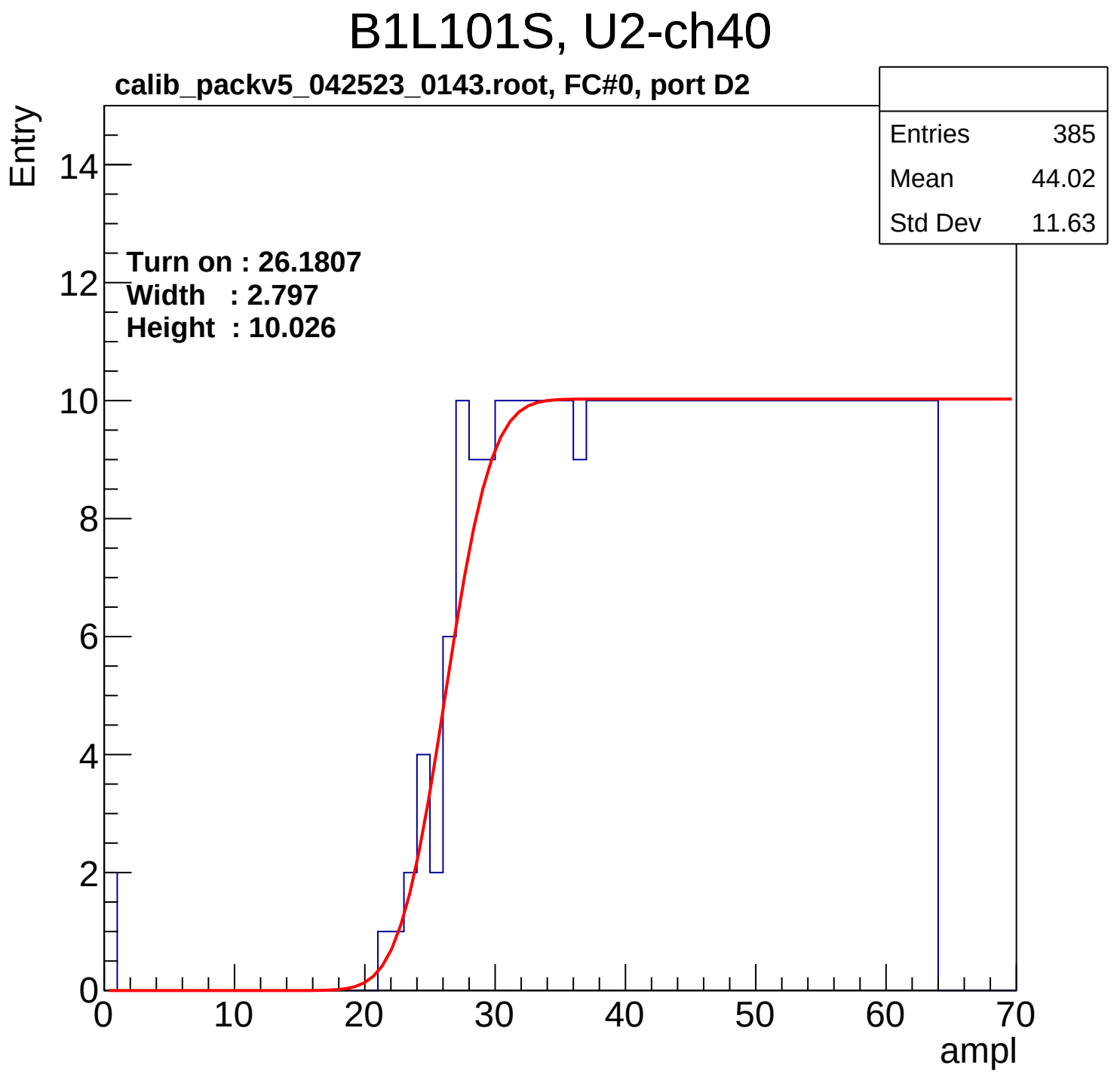
B1L101S, U2-ch40
calib_packv5_042523_0143.root, FC#0, port D2
Entries 385
Mean 44.02
Std Dev 11.63
Turn on : 26.1807
Width : 2.797
Height : 10.026
Entry
ampl
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6
8
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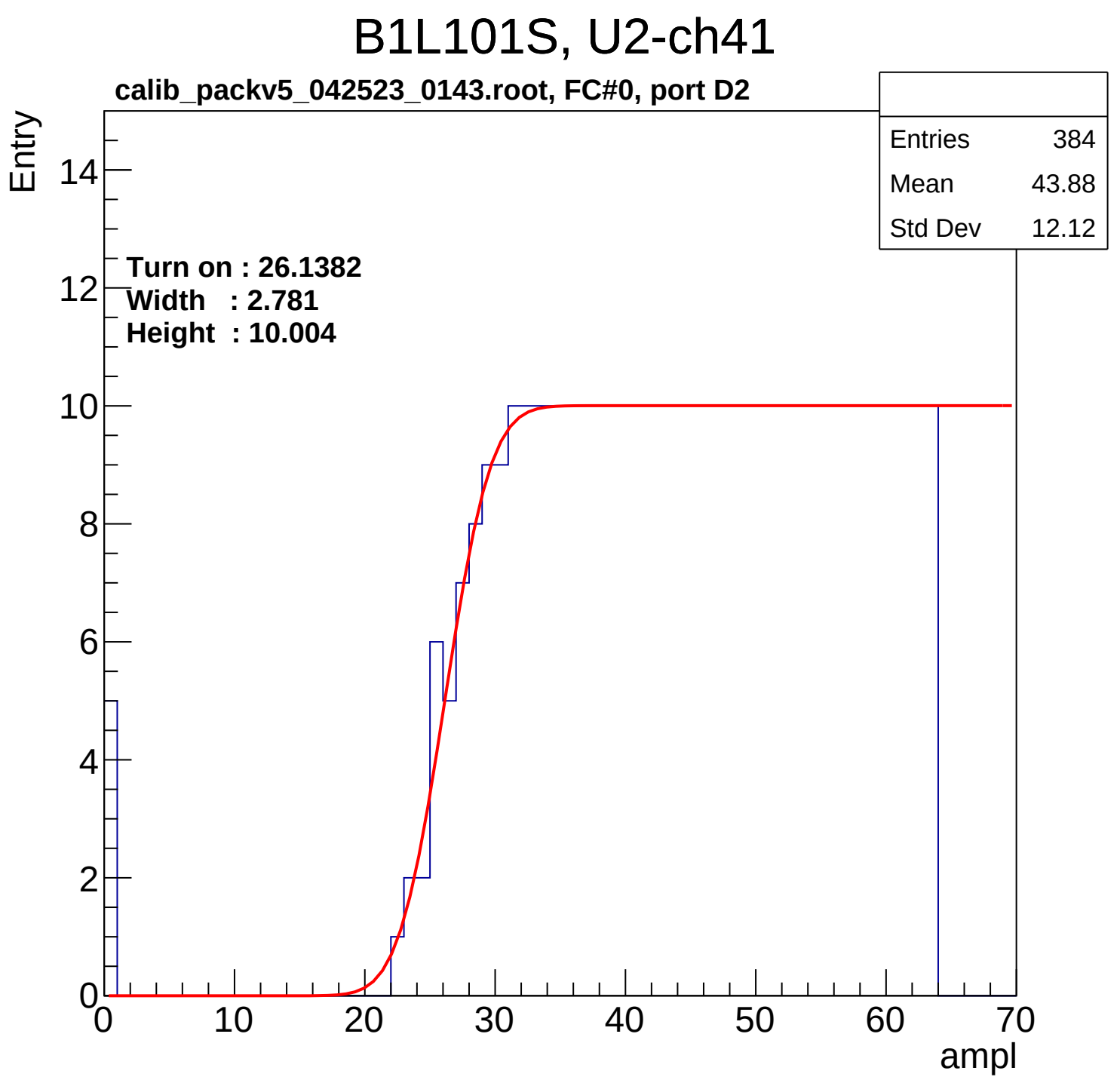
B1L101S, U2-ch41
calib_packv5_042523_0143.root, FC#0, port D2
Entries 384
Mean 43.88
Std Dev 12.12
Turn on : 26.1382
Width : 2.781
Height : 10.004
Entry
ampl
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4
6
8
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12
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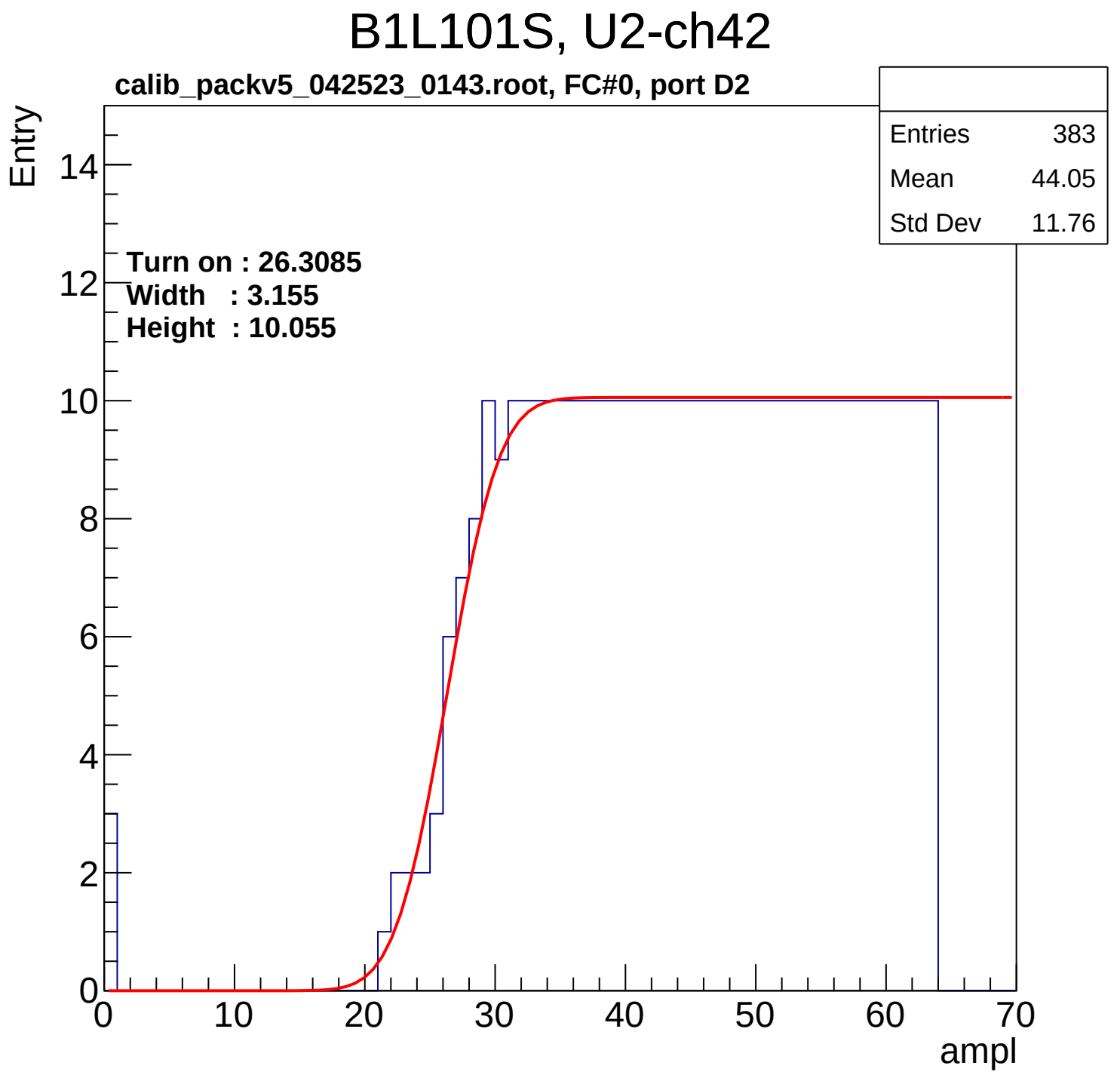
B1L101S, U2-ch42
calib_packv5_042523_0143.root, FC#0, port D2
Entries 383
Mean 44.05
Std Dev 11.76
Turn on : 26.3085
Width : 3.155
Height : 10.055
Entry
ampl
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4
6
8
10
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0
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20
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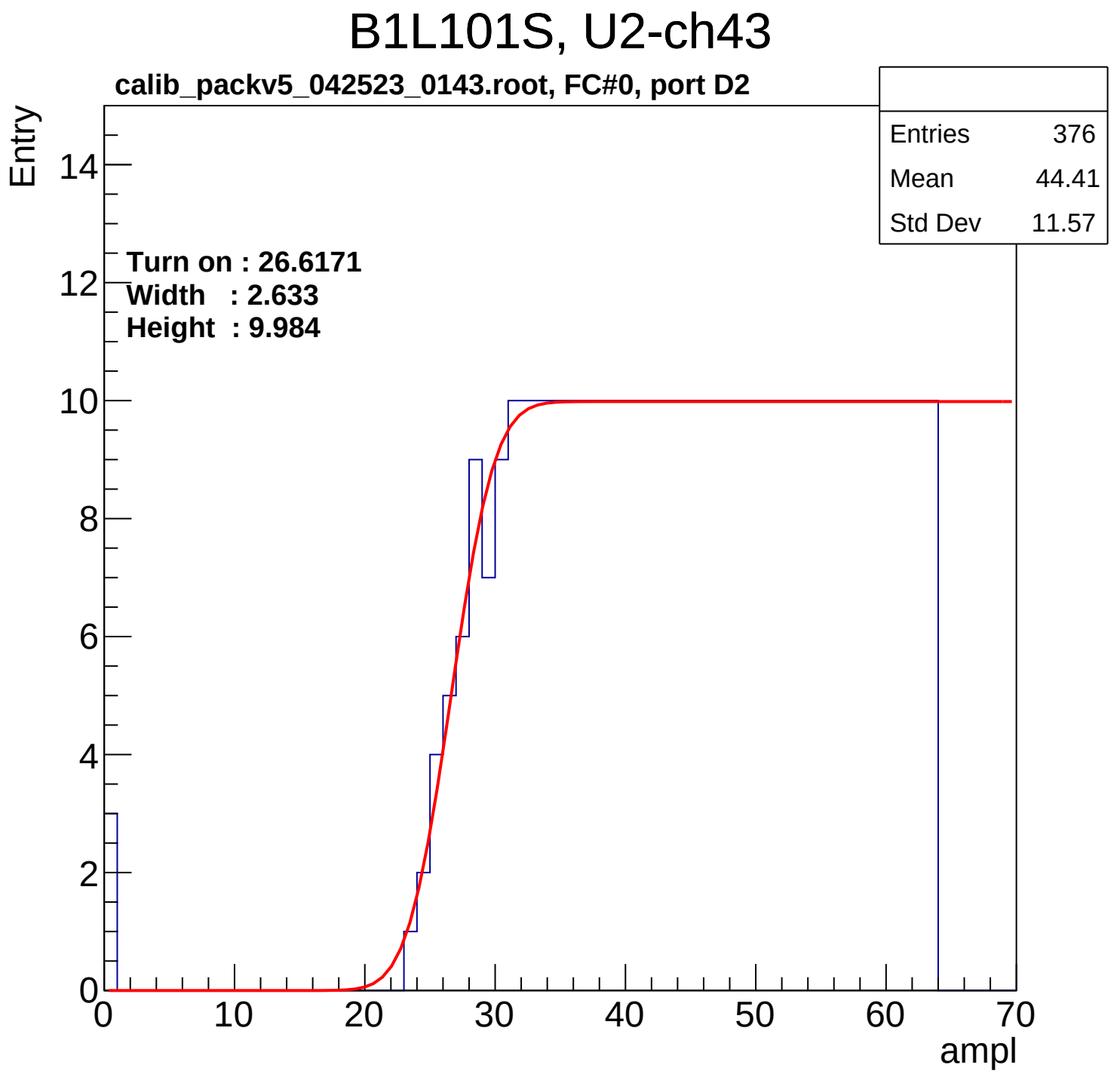
B1L101S, U2-ch43
calib_packv5_042523_0143.root, FC#0, port D2
Entries 376
Mean 44.41
Std Dev 11.57
Turn on : 26.6171
Width : 2.633
Height : 9.984
Entry
ampl
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6
8
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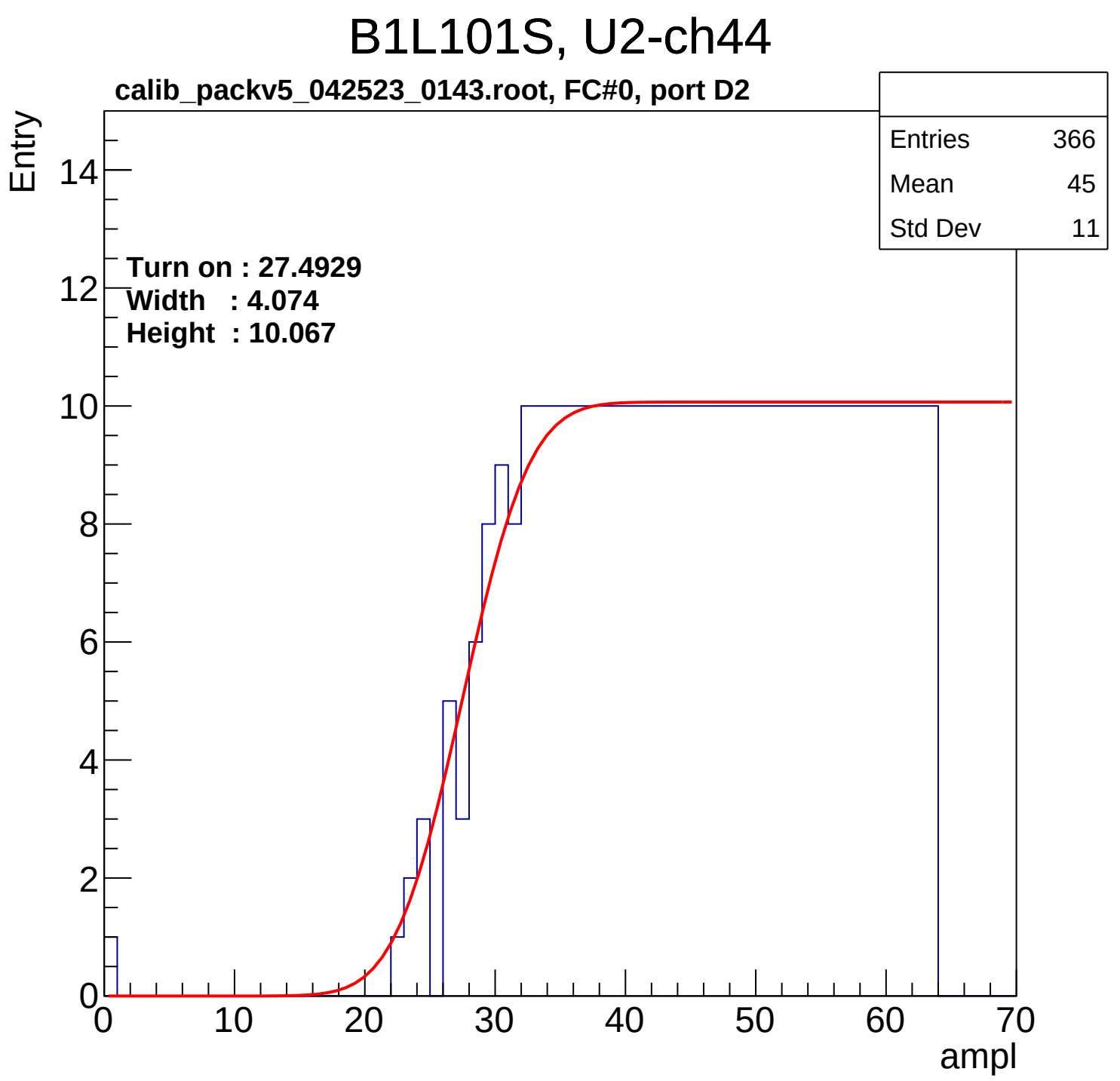
B1L101S, U2-ch44
calib_packv5_042523_0143.root, FC#0, port D2
Entries 366
Mean 45
Std Dev 11
Turn on : 27.4929
Width : 4.074
Height : 10.067
Entry
ampl
0
2
4
6
8
10
12
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0
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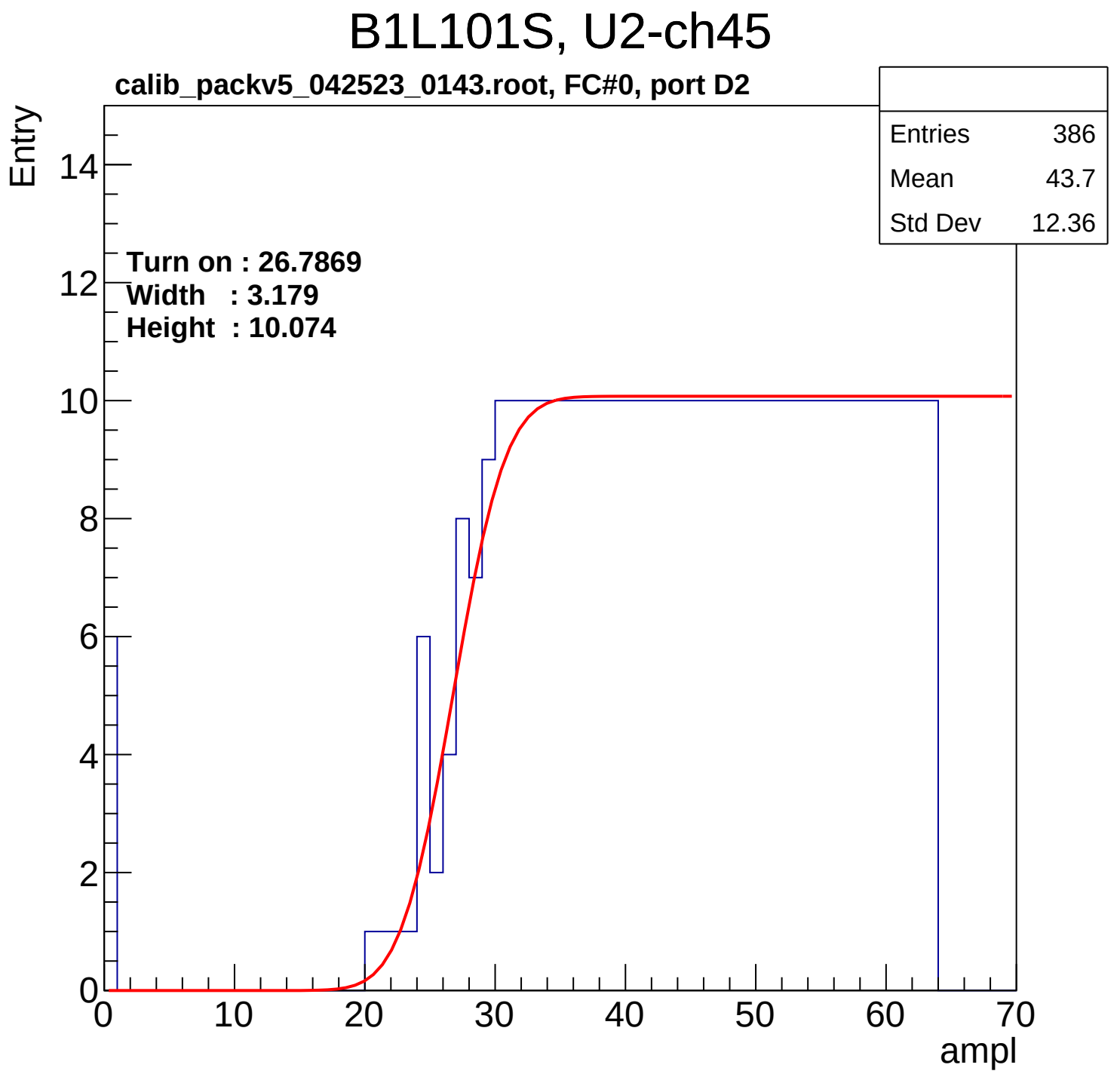
B1L101S, U2-ch45
calib_packv5_042523_0143.root, FC#0, port D2
Entries 386
Mean 43.7
Std Dev 12.36
Turn on : 26.7869
Width : 3.179
Height : 10.074
Entry
ampl
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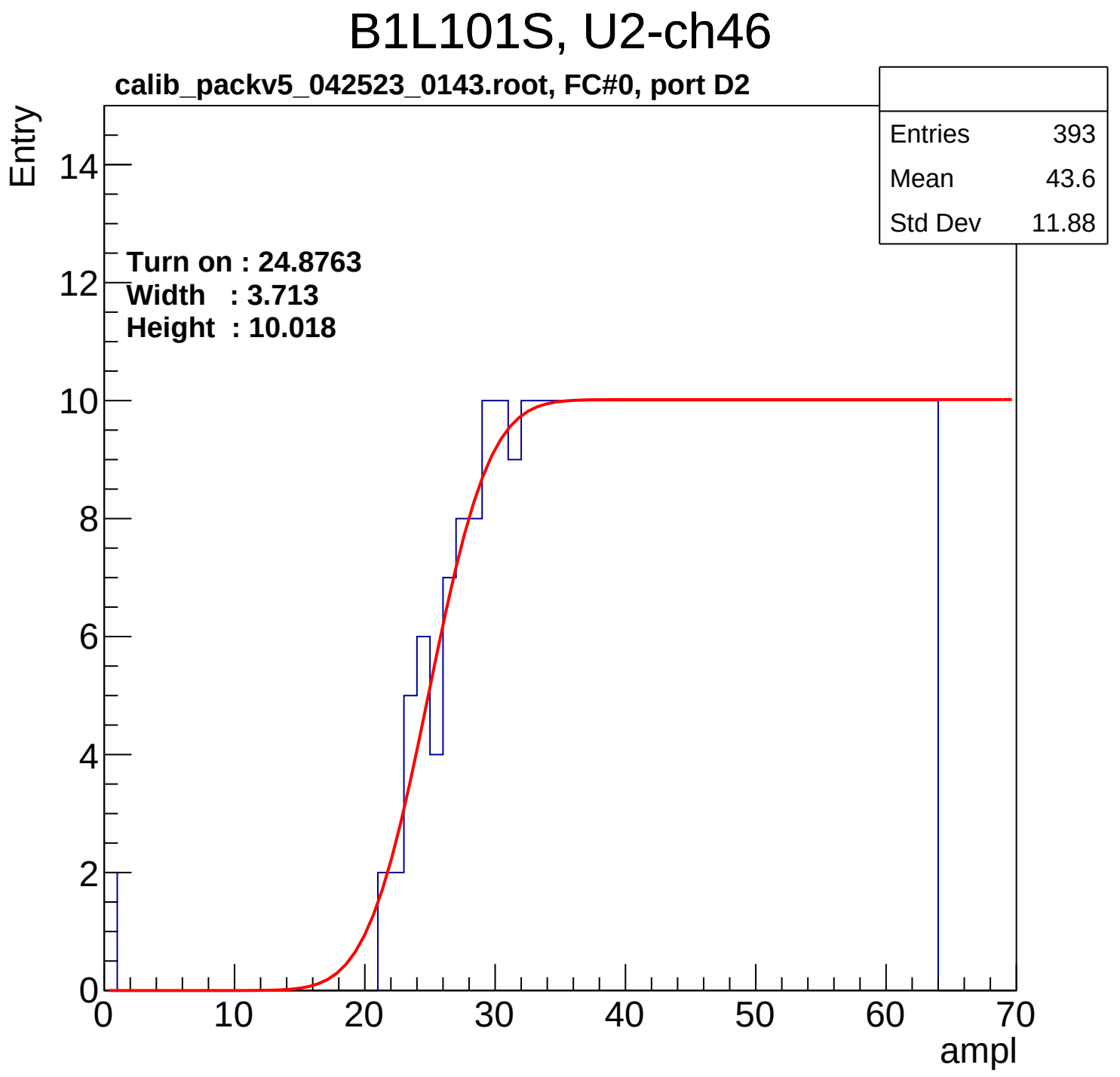
B1L101S, U2-ch46
calib_packv5_042523_0143.root, FC#0, port D2
Entries 393
Mean 43.6
Std Dev 11.88
Turn on : 24.8763
Width : 3.713
Height : 10.018
Entry
ampl
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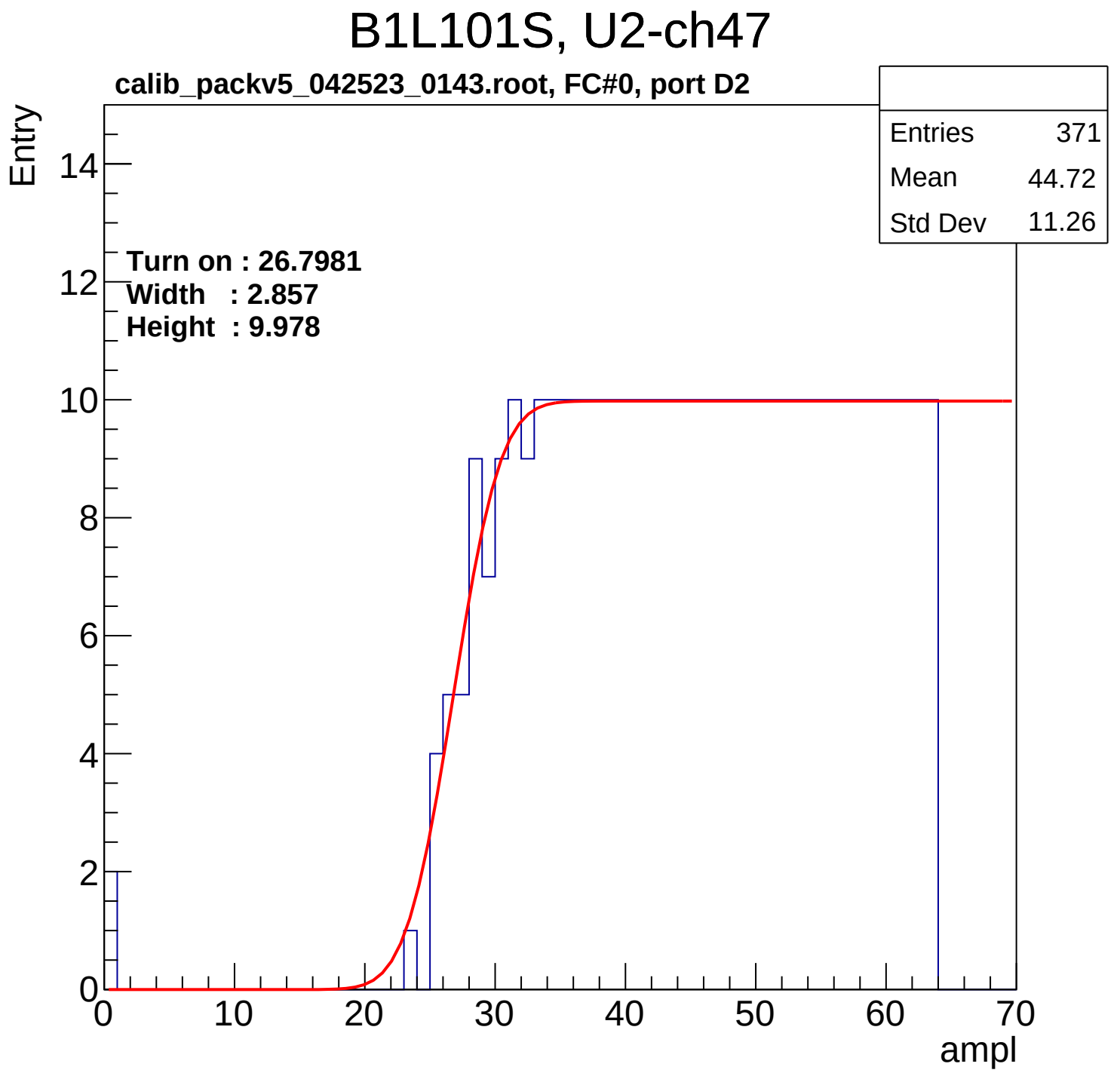
B1L101S, U2-ch47
calib_packv5_042523_0143.root, FC#0, port D2
Entries 371
Mean 44.72
Std Dev 11.26
Turn on : 26.7981
Width : 2.857
Height : 9.978
Entry
ampl
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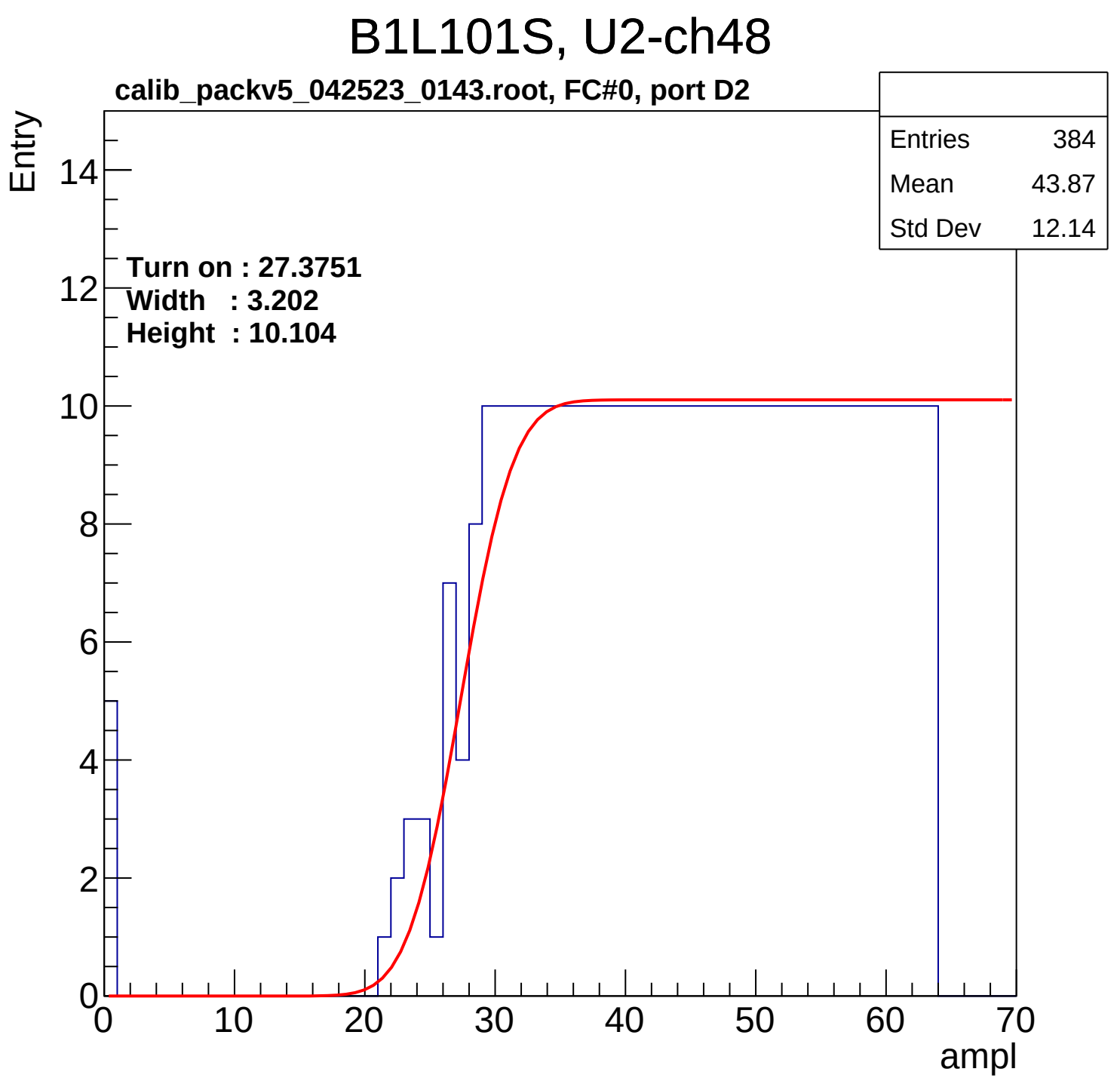
B1L101S, U2-ch48
calib_packv5_042523_0143.root, FC#0, port D2
Entries 384
Mean 43.87
Std Dev 12.14
Turn on : 27.3751
Width : 3.202
Height : 10.104
Entry
ampl
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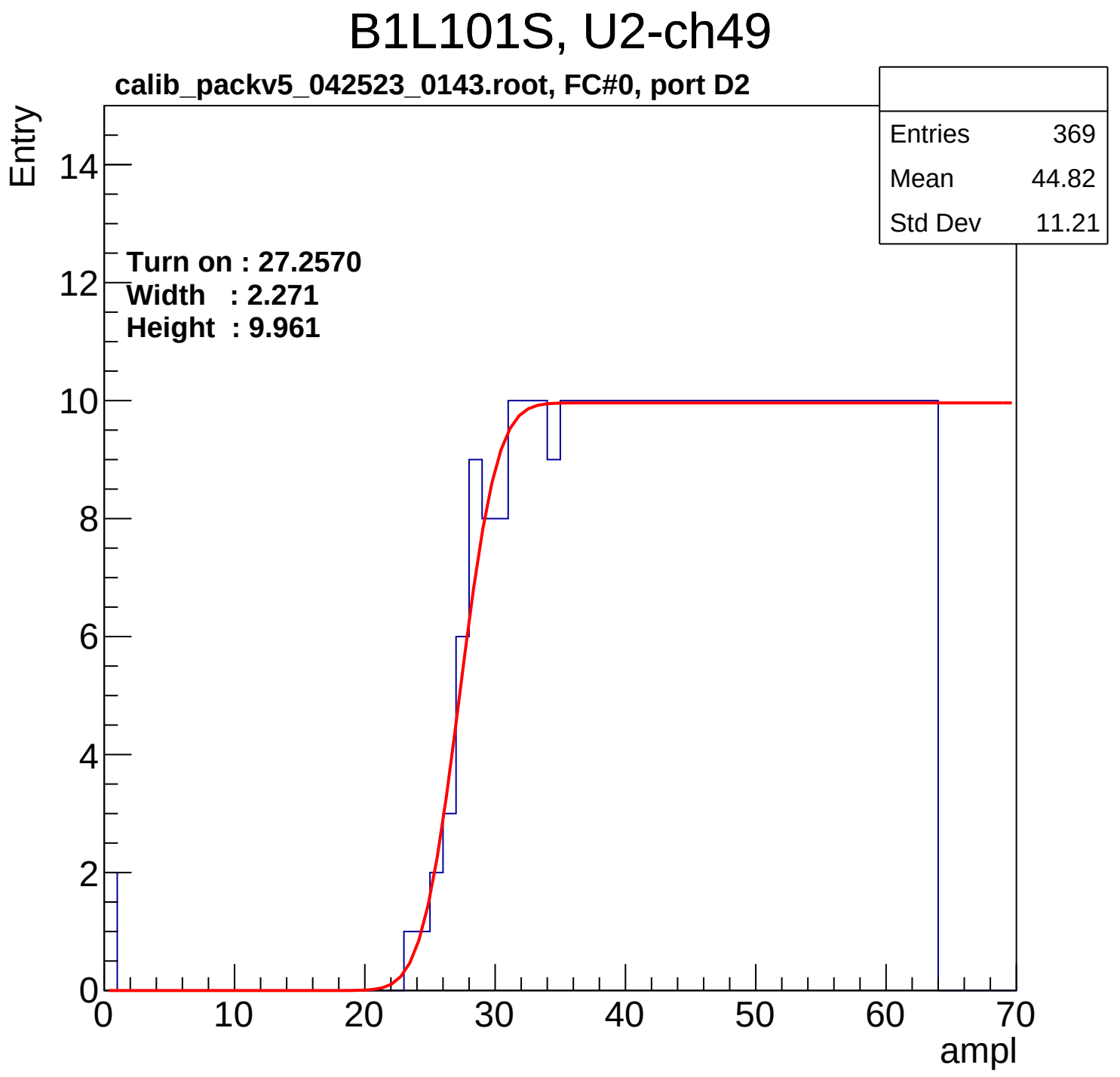
B1L101S, U2-ch49
calib_packv5_042523_0143.root, FC#0, port D2
Entries 369
Mean 44.82
Std Dev 11.21
Turn on : 27.2570
Width : 2.271
Height : 9.961
Entry
ampl
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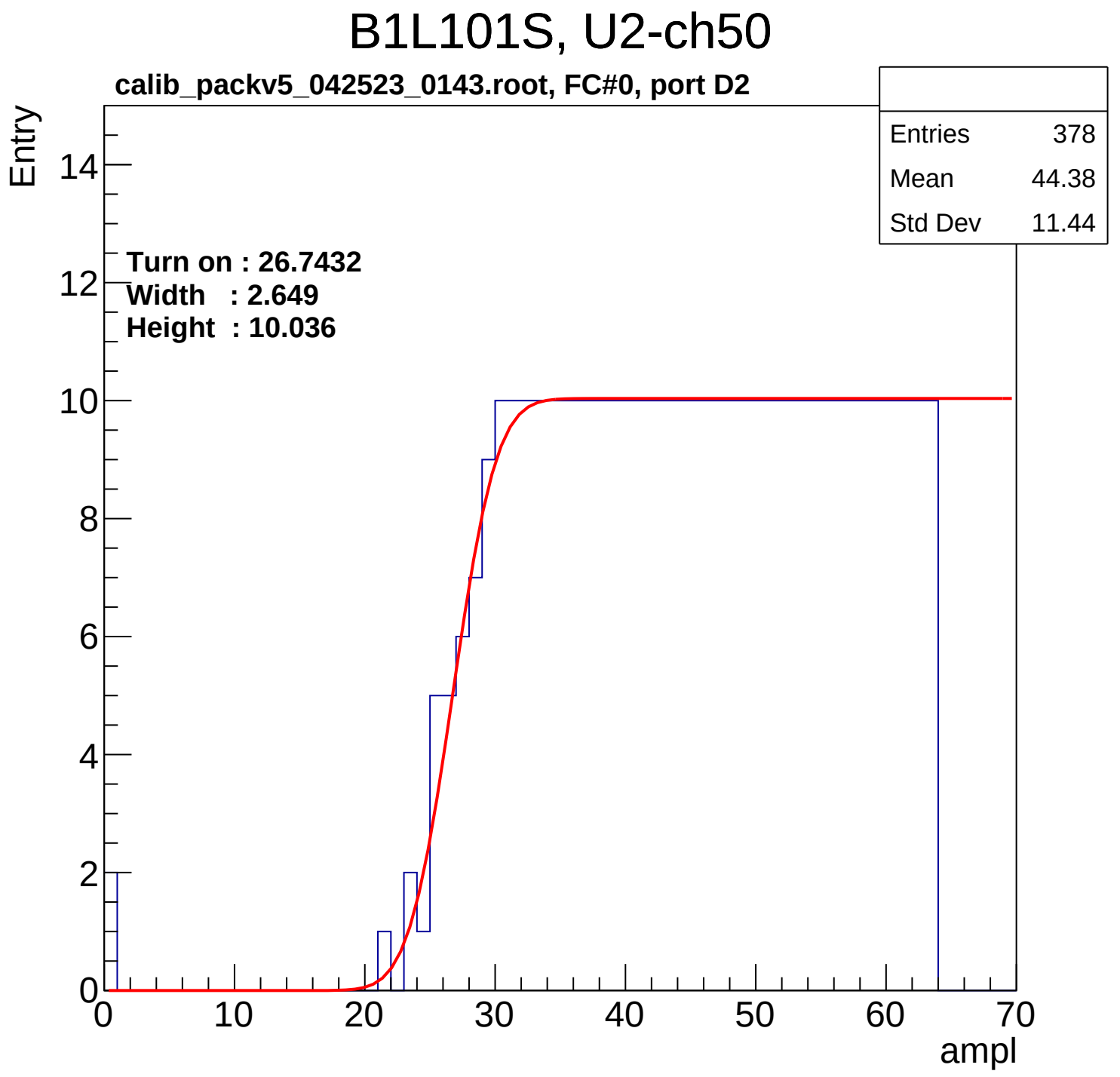
B1L101S, U2-ch50
calib_packv5_042523_0143.root, FC#0, port D2
Entries 378
Mean 44.38
Std Dev 11.44
Turn on : 26.7432
Width : 2.649
Height : 10.036
Entry
ampl
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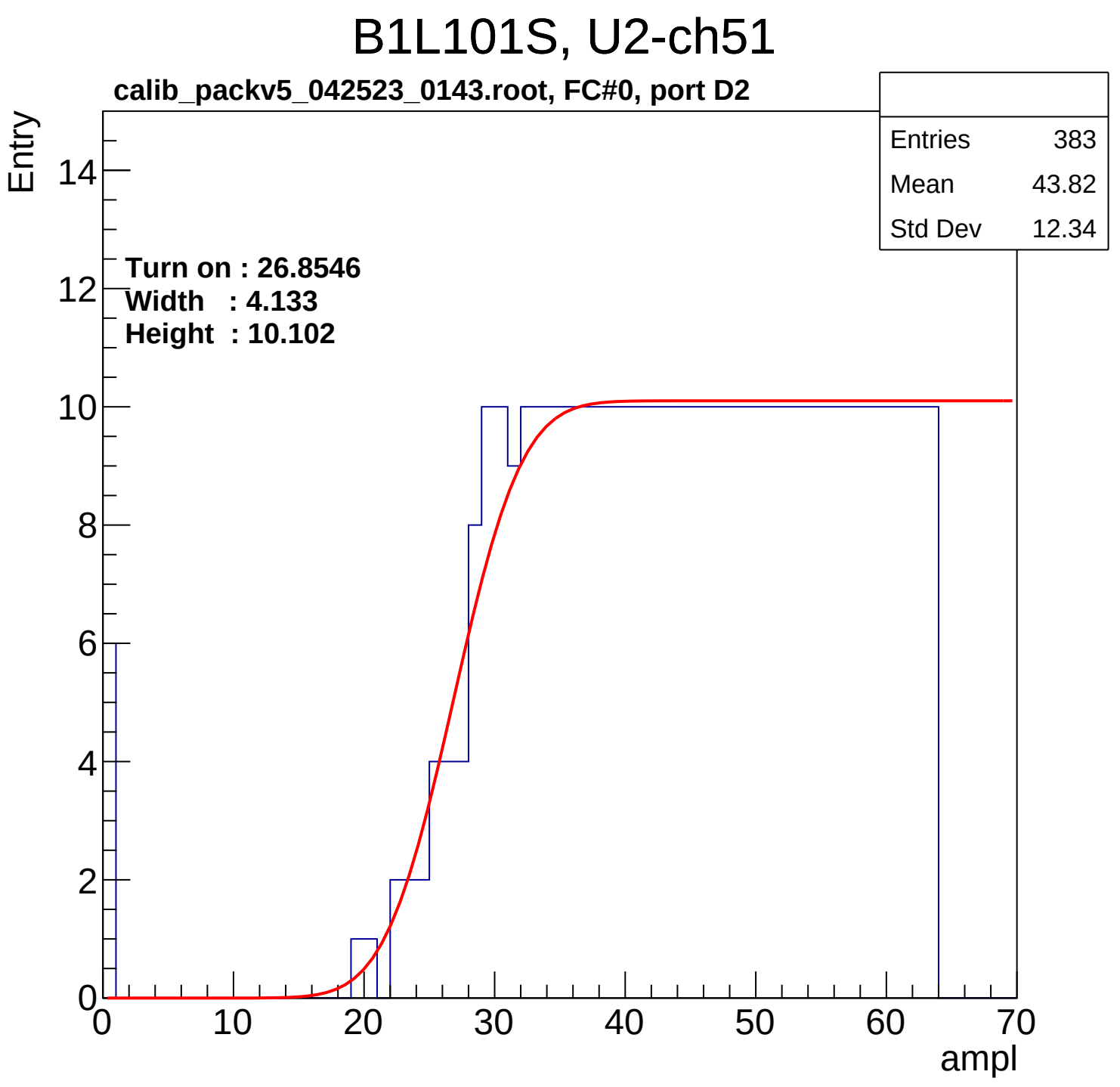
B1L101S, U2-ch51
calib_packv5_042523_0143.root, FC#0, port D2
Entries 383
Mean 43.82
Std Dev 12.34
Turn on : 26.8546
Width : 4.133
Height : 10.102
Entry
ampl
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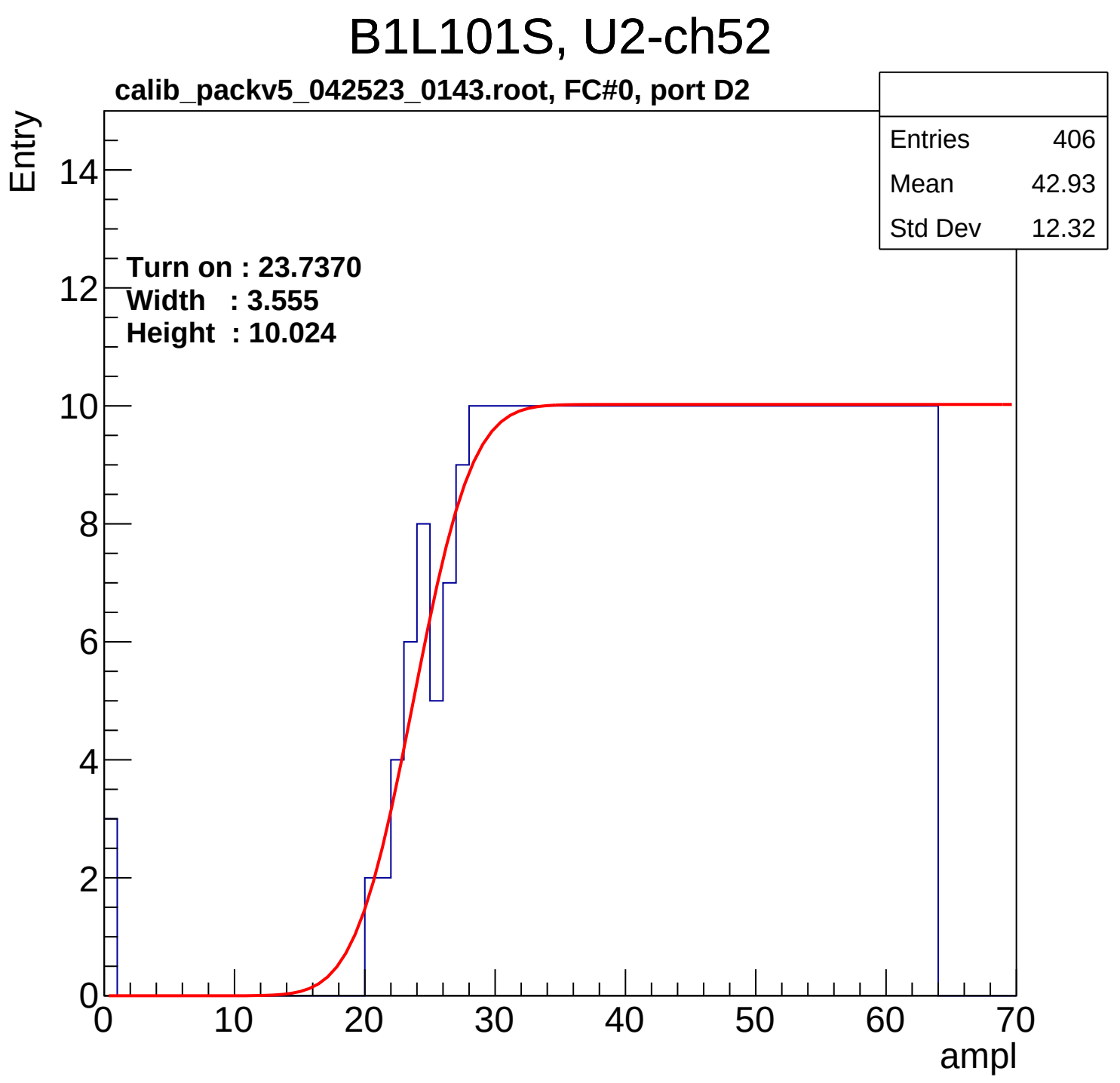
B1L101S, U2-ch52
calib_packv5_042523_0143.root, FC#0, port D2
Entries 406
Mean 42.93
Std Dev 12.32
Turn on : 23.7370
Width : 3.555
Height : 10.024
Entry
ampl
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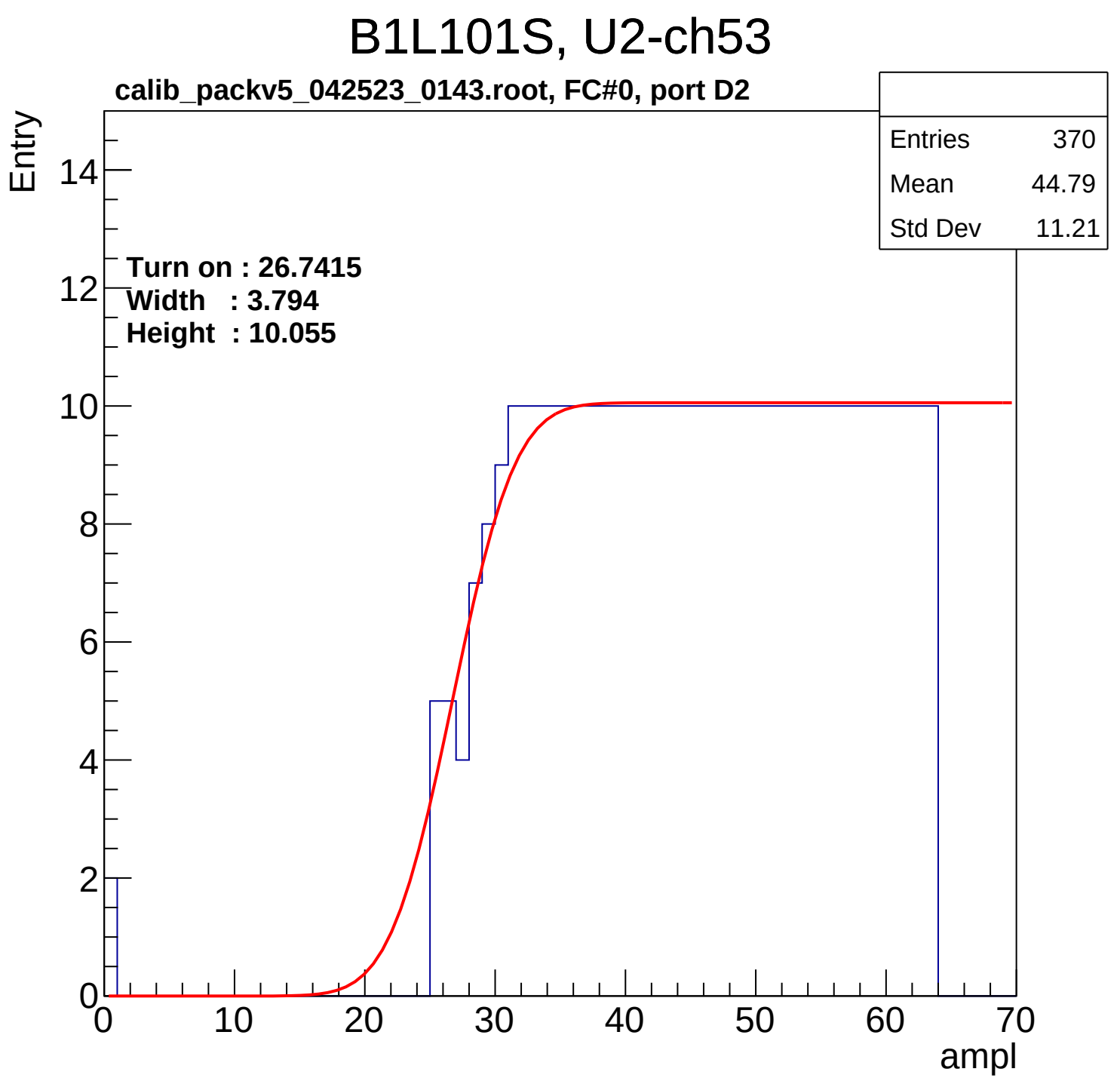
B1L101S, U2-ch53
calib_packv5_042523_0143.root, FC#0, port D2
Entries 370
Mean 44.79
Std Dev 11.21
Turn on : 26.7415
Width : 3.794
Height : 10.055
Entry
ampl
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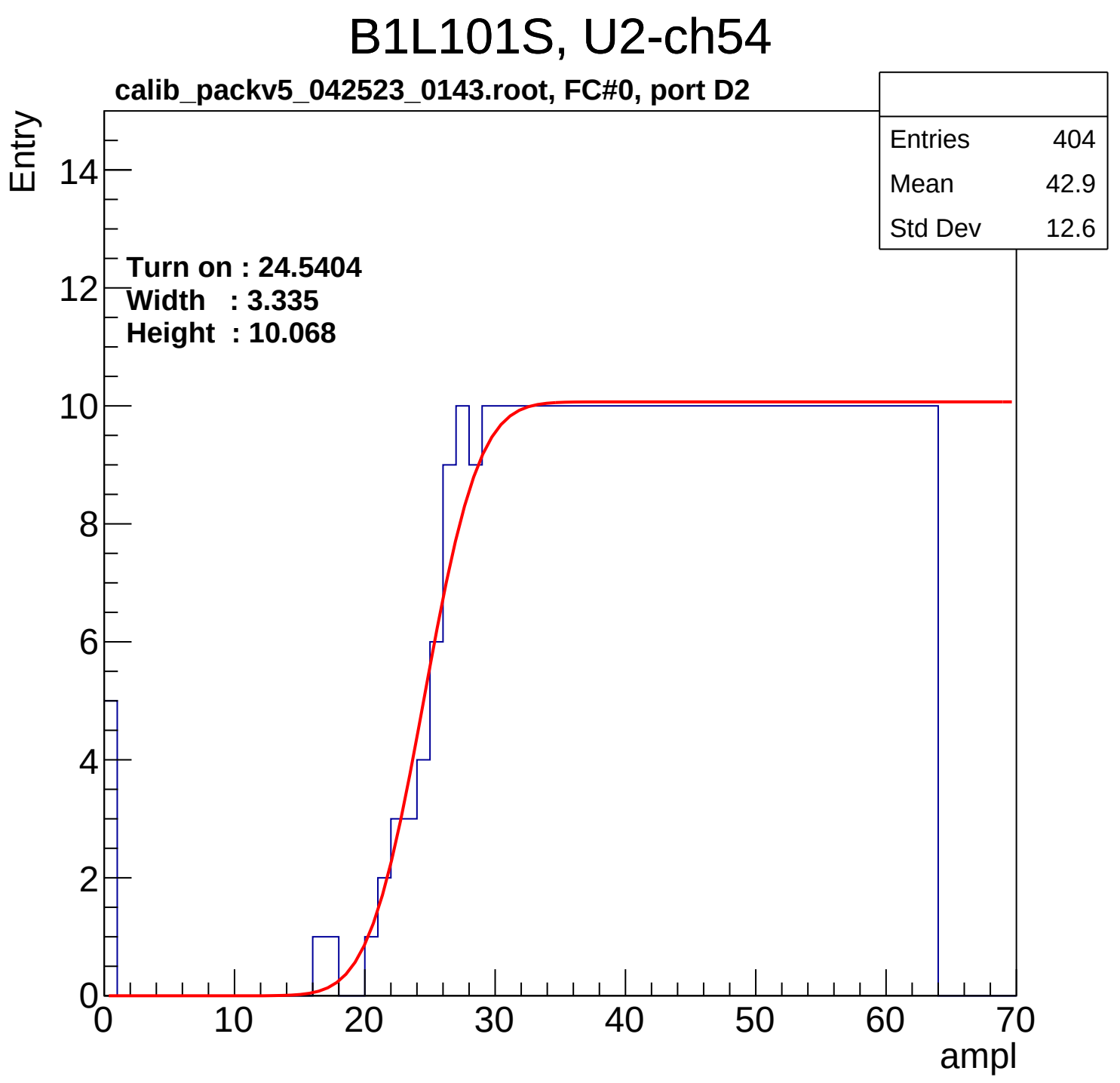
B1L101S, U2-ch54
calib_packv5_042523_0143.root, FC#0, port D2
Entries 404
Mean 42.9
Std Dev 12.6
Turn on : 24.5404
Width : 3.335
Height : 10.068
Entry
ampl
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6
8
10
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60
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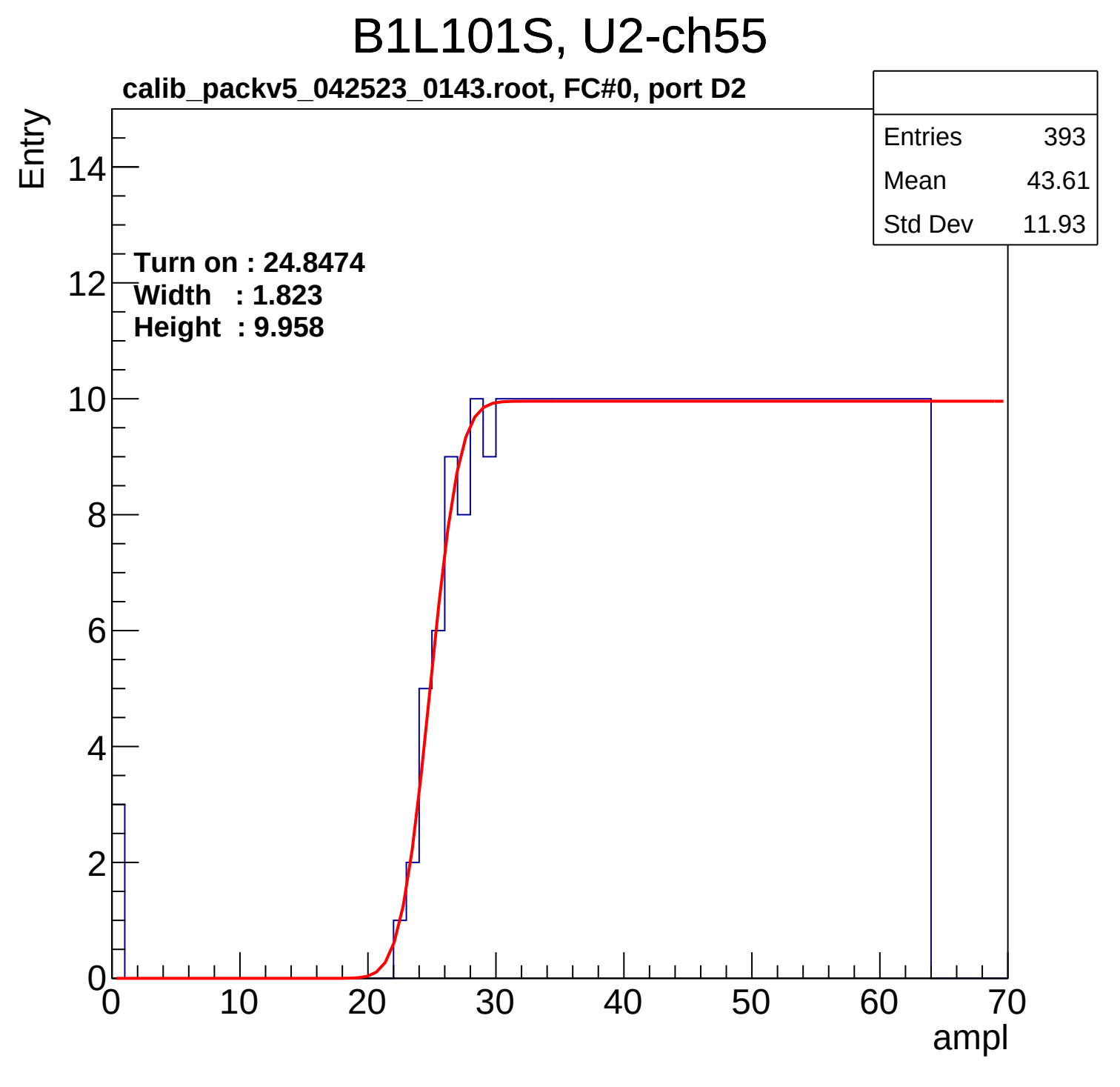
B1L101S, U2-ch55
calib_packv5_042523_0143.root, FC#0, port D2
Entries 393
Mean 43.61
Std Dev 11.93
Turn on : 24.8474
Width : 1.823
Height : 9.958
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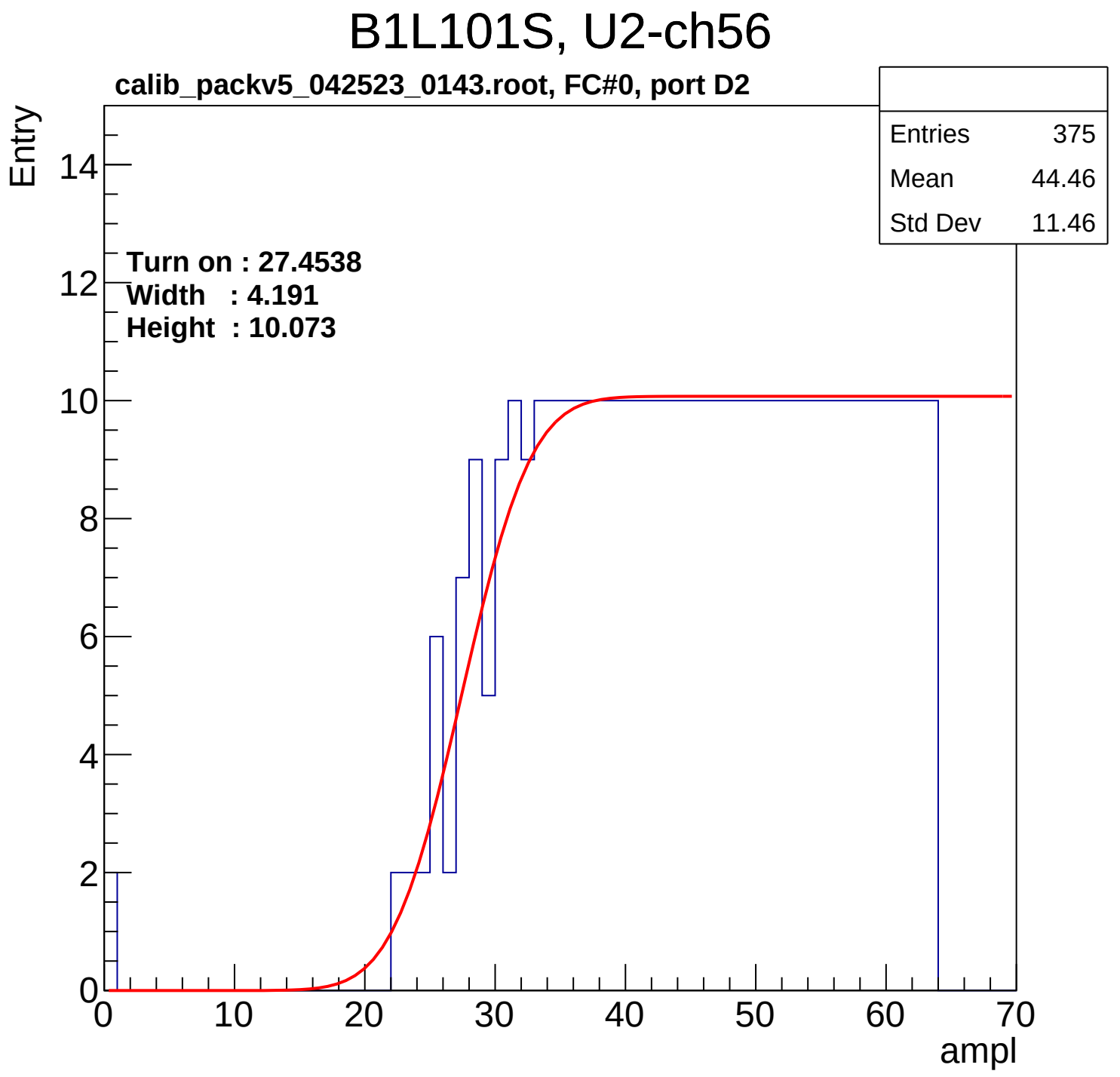
B1L101S, U2-ch56
calib_packv5_042523_0143.root, FC#0, port D2
Entries 375
Mean 44.46
Std Dev 11.46
Turn on : 27.4538
Width : 4.191
Height : 10.073
Entry
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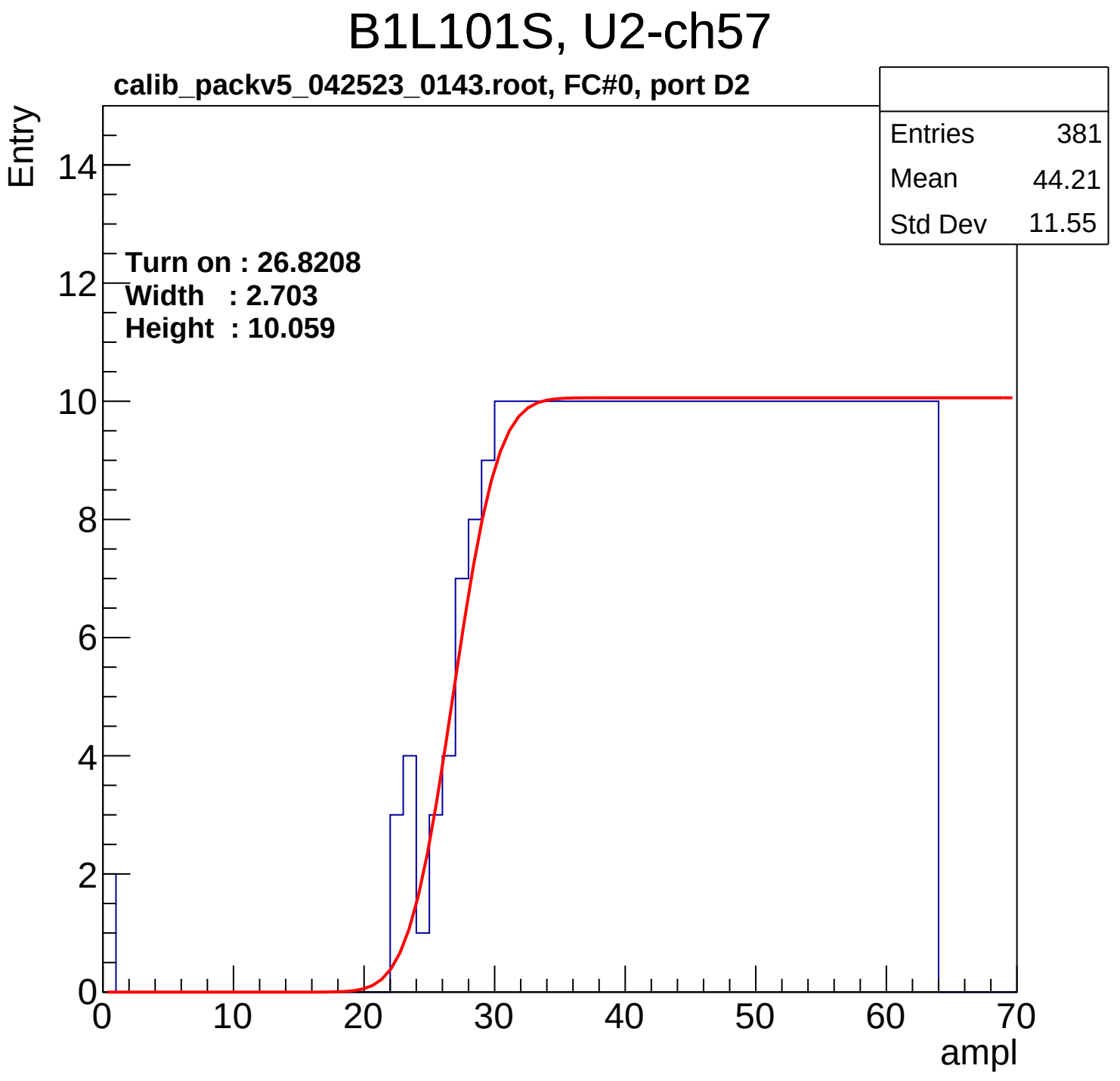
B1L101S, U2-ch57
calib_packv5_042523_0143.root, FC#0, port D2
Entries 381
Mean 44.21
Std Dev 11.55
Turn on : 26.8208
Width : 2.703
Height : 10.059
Entry
ampl
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2
4
6
8
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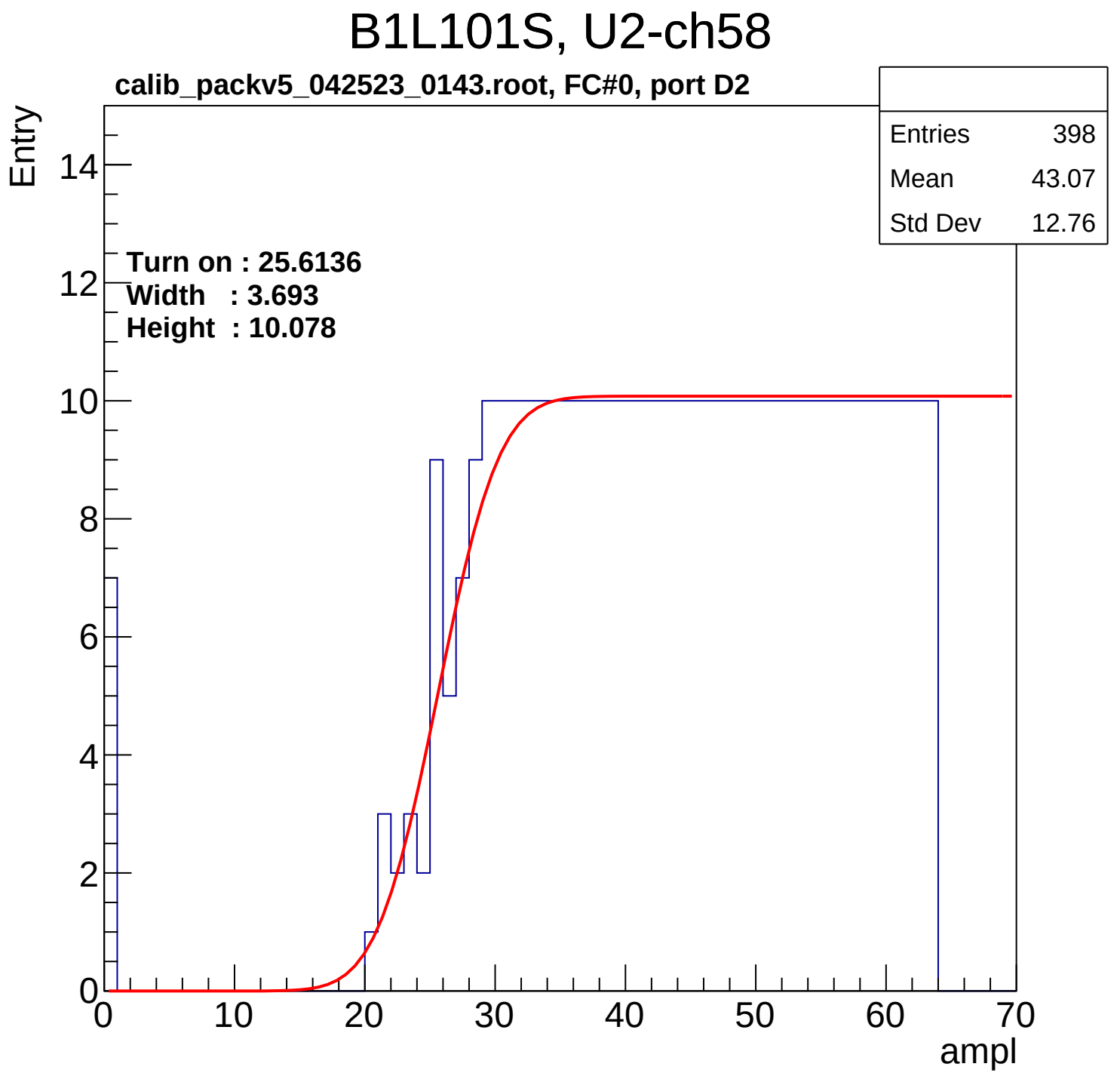
B1L101S, U2-ch58
calib_packv5_042523_0143.root, FC#0, port D2
Entries 398
Mean 43.07
Std Dev 12.76
Turn on : 25.6136
Width : 3.693
Height : 10.078
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ampl
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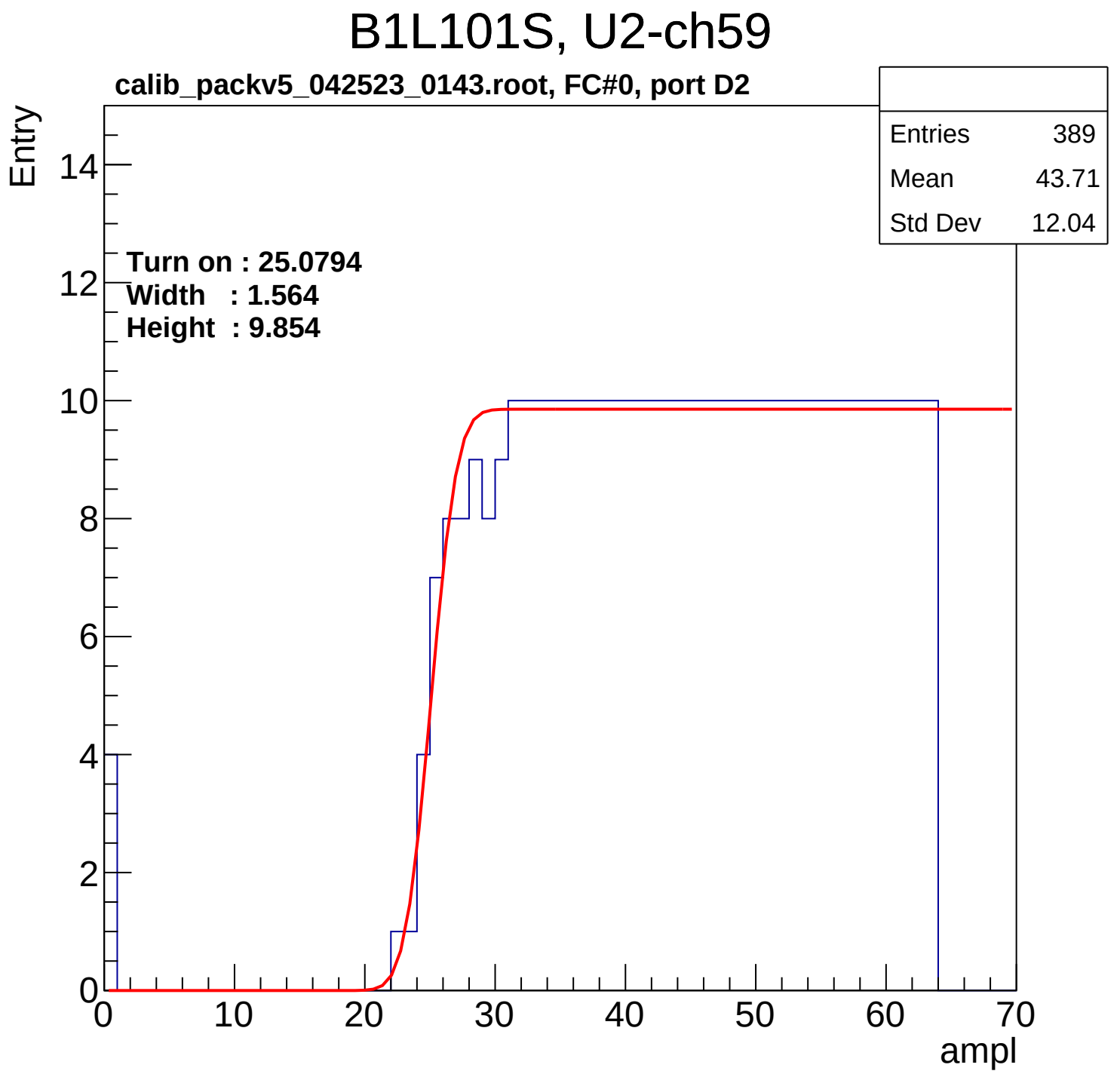
B1L101S, U2-ch59
calib_packv5_042523_0143.root, FC#0, port D2
Entries 389
Mean 43.71
Std Dev 12.04
Turn on : 25.0794
Width : 1.564
Height : 9.854
Entry
ampl
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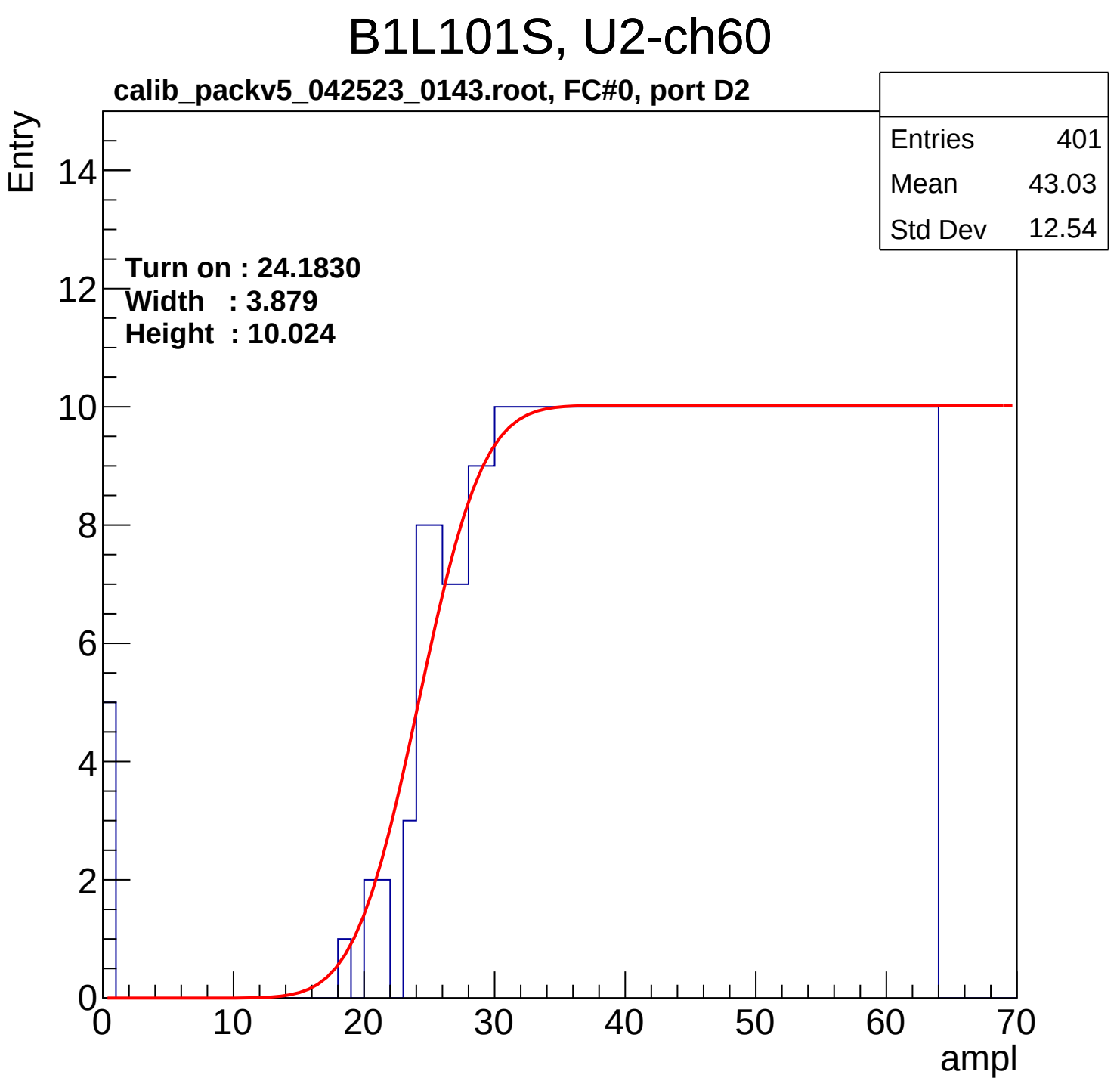
B1L101S, U2-ch60
calib_packv5_042523_0143.root, FC#0, port D2
Entries 401
Mean 43.03
Std Dev 12.54
Turn on : 24.1830
Width : 3.879
Height : 10.024
Entry
ampl
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2
4
6
8
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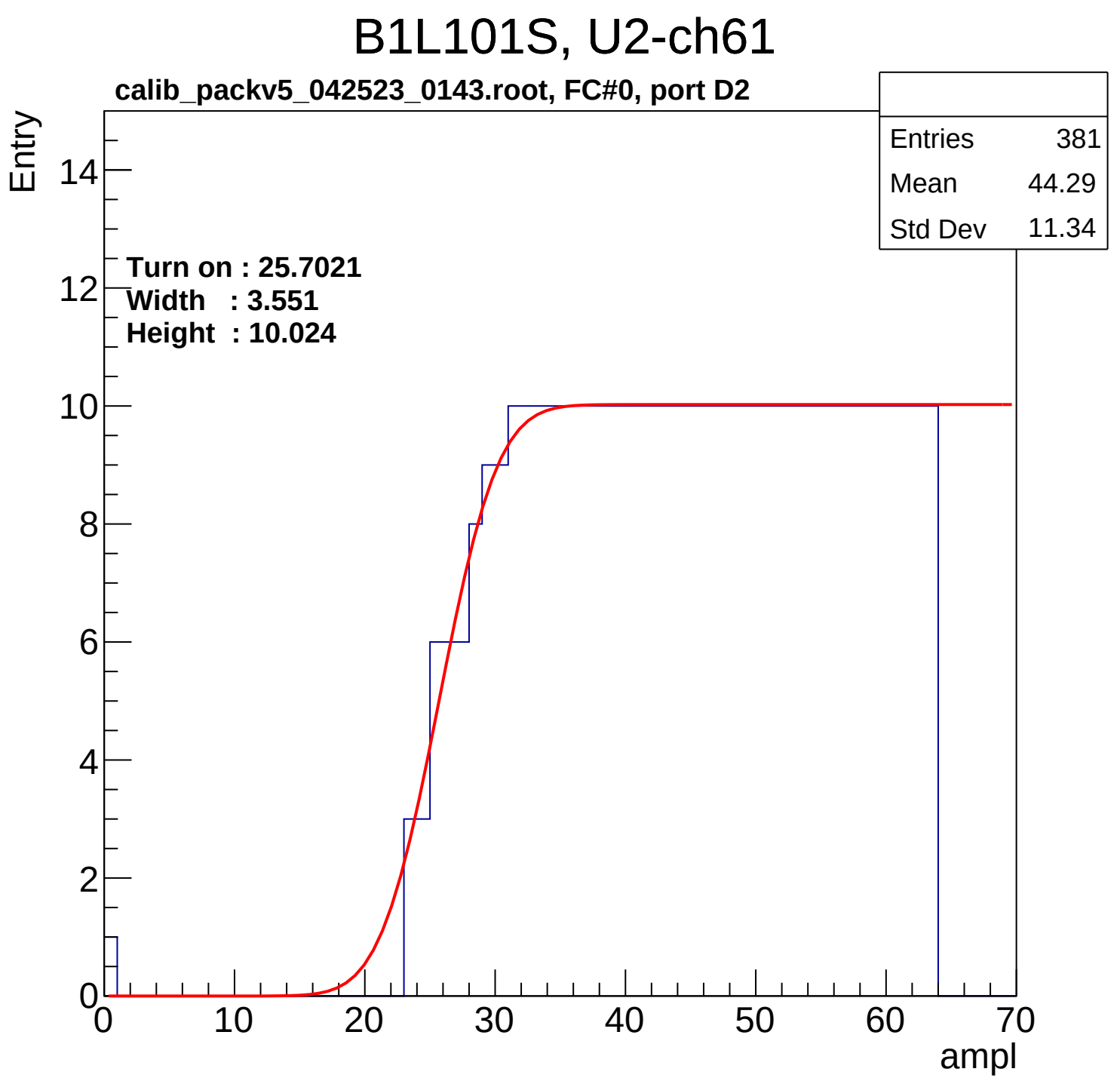
B1L101S, U2-ch61
calib_packv5_042523_0143.root, FC#0, port D2
Entries 381
Mean 44.29
Std Dev 11.34
Turn on : 25.7021
Width : 3.551
Height : 10.024
Entry
ampl
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4
6
8
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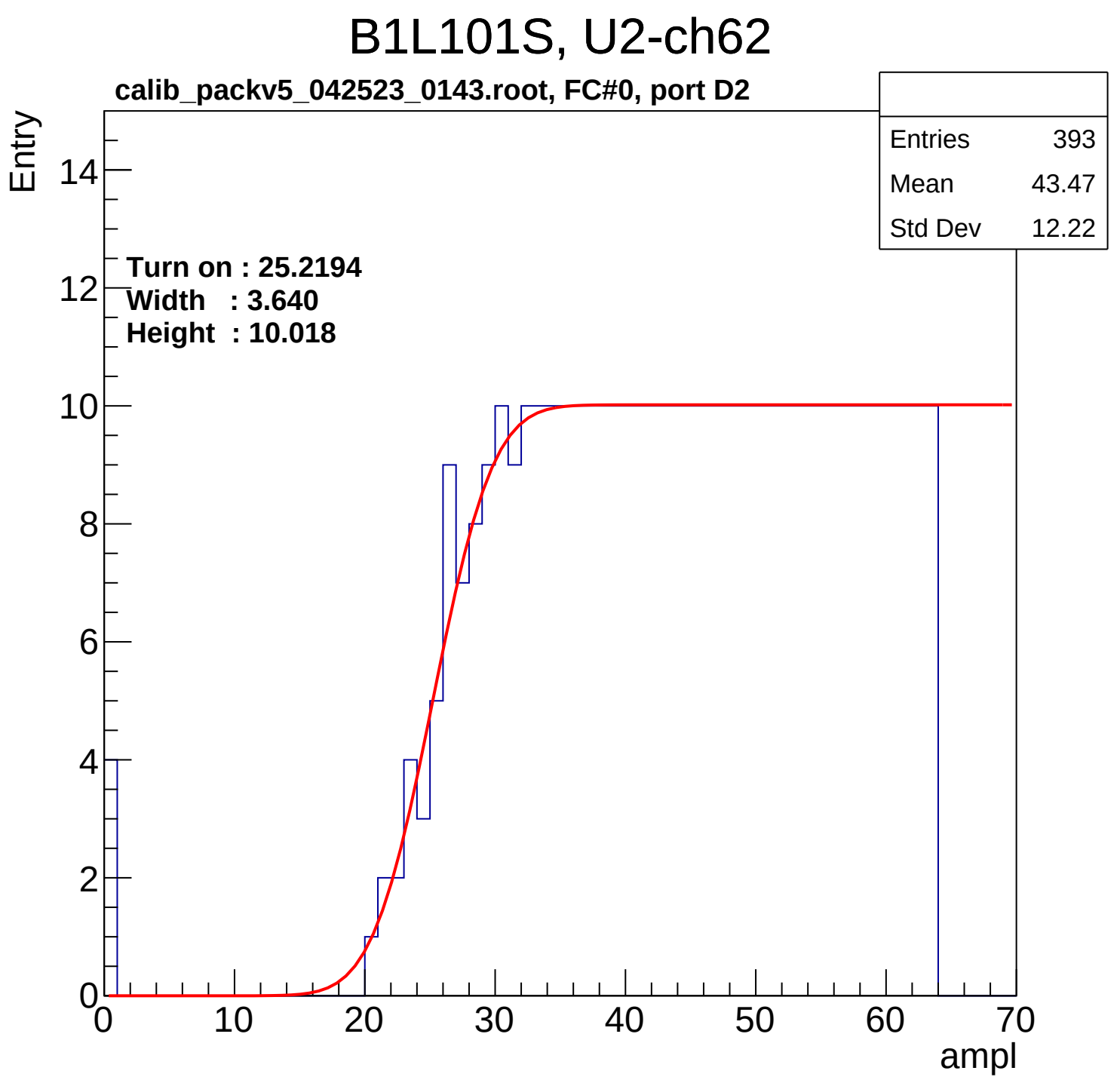
B1L101S, U2-ch62
calib_packv5_042523_0143.root, FC#0, port D2
Entries 393
Mean 43.47
Std Dev 12.22
Turn on : 25.2194
Width : 3.640
Height : 10.018
Entry
ampl
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6
8
10
12
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0
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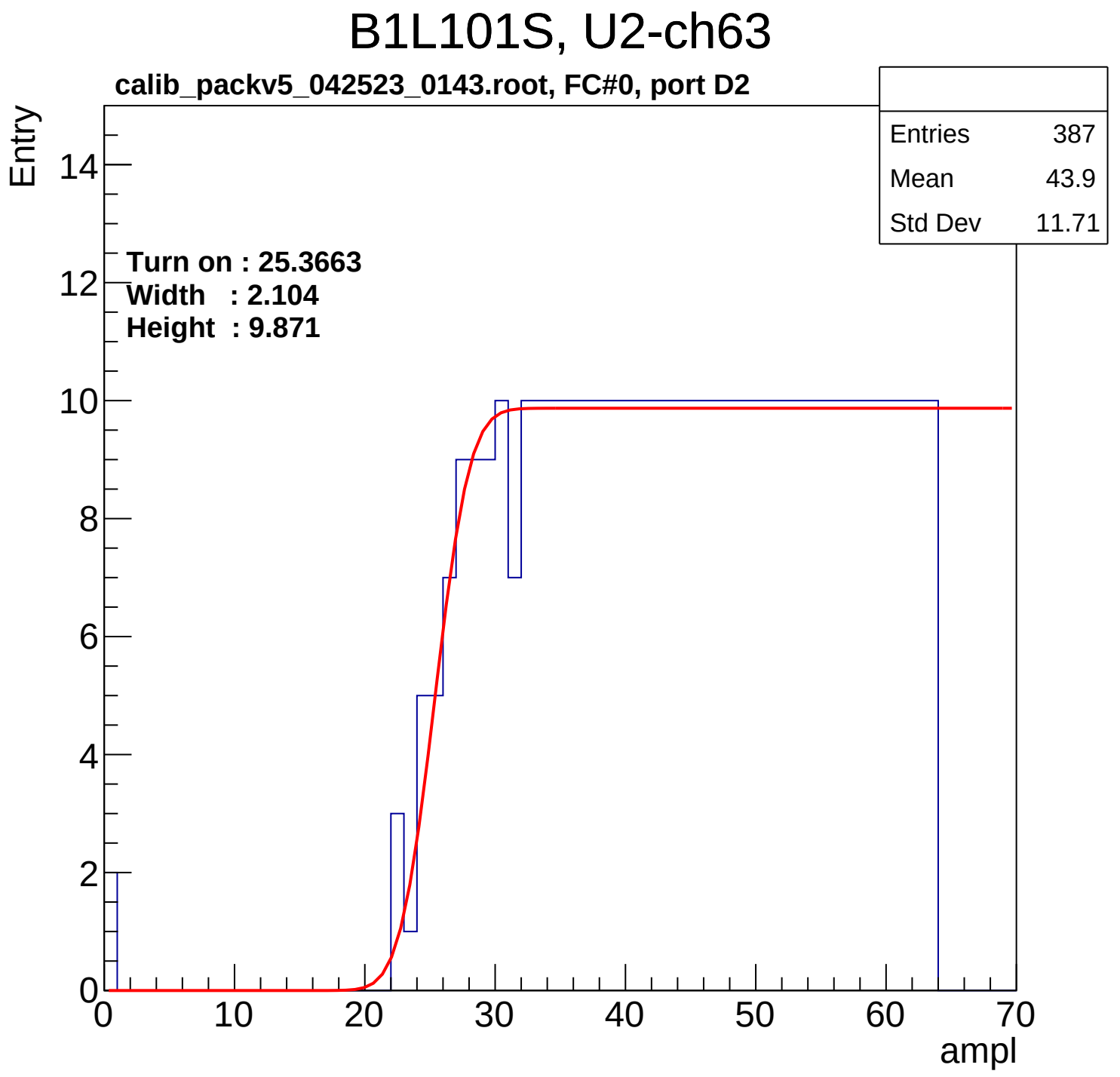
B1L101S, U2-ch63
calib_packv5_042523_0143.root, FC#0, port D2
Entries 387
Mean 43.9
Std Dev 11.71
Turn on : 25.3663
Width : 2.104
Height : 9.871
Entry
ampl
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2
4
6
8
10
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60
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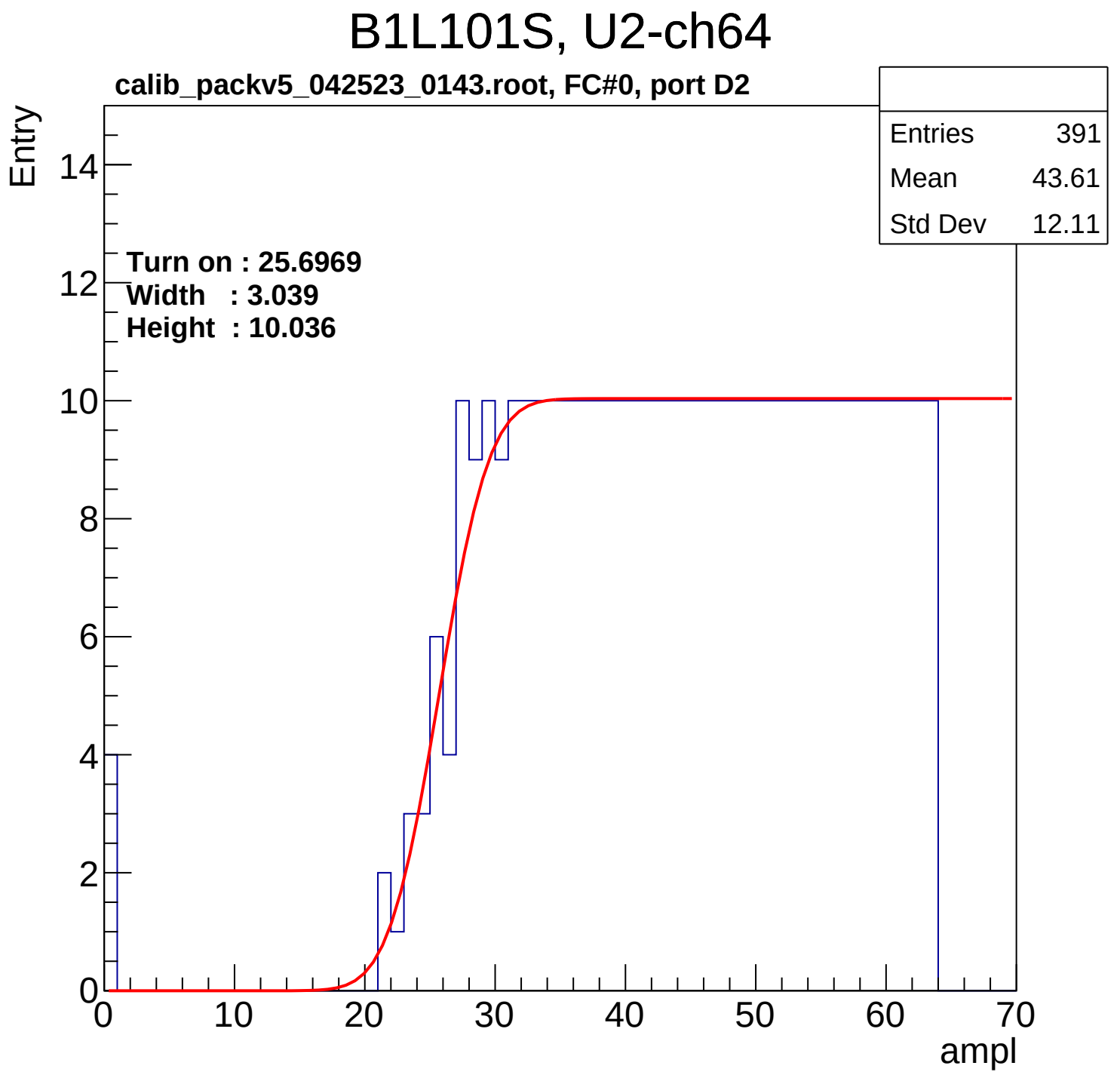
B1L101S, U2-ch64
calib_packv5_042523_0143.root, FC#0, port D2
Entries 391
Mean 43.61
Std Dev 12.11
Turn on : 25.6969
Width : 3.039
Height : 10.036
Entry
ampl
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2
4
6
8
10
12
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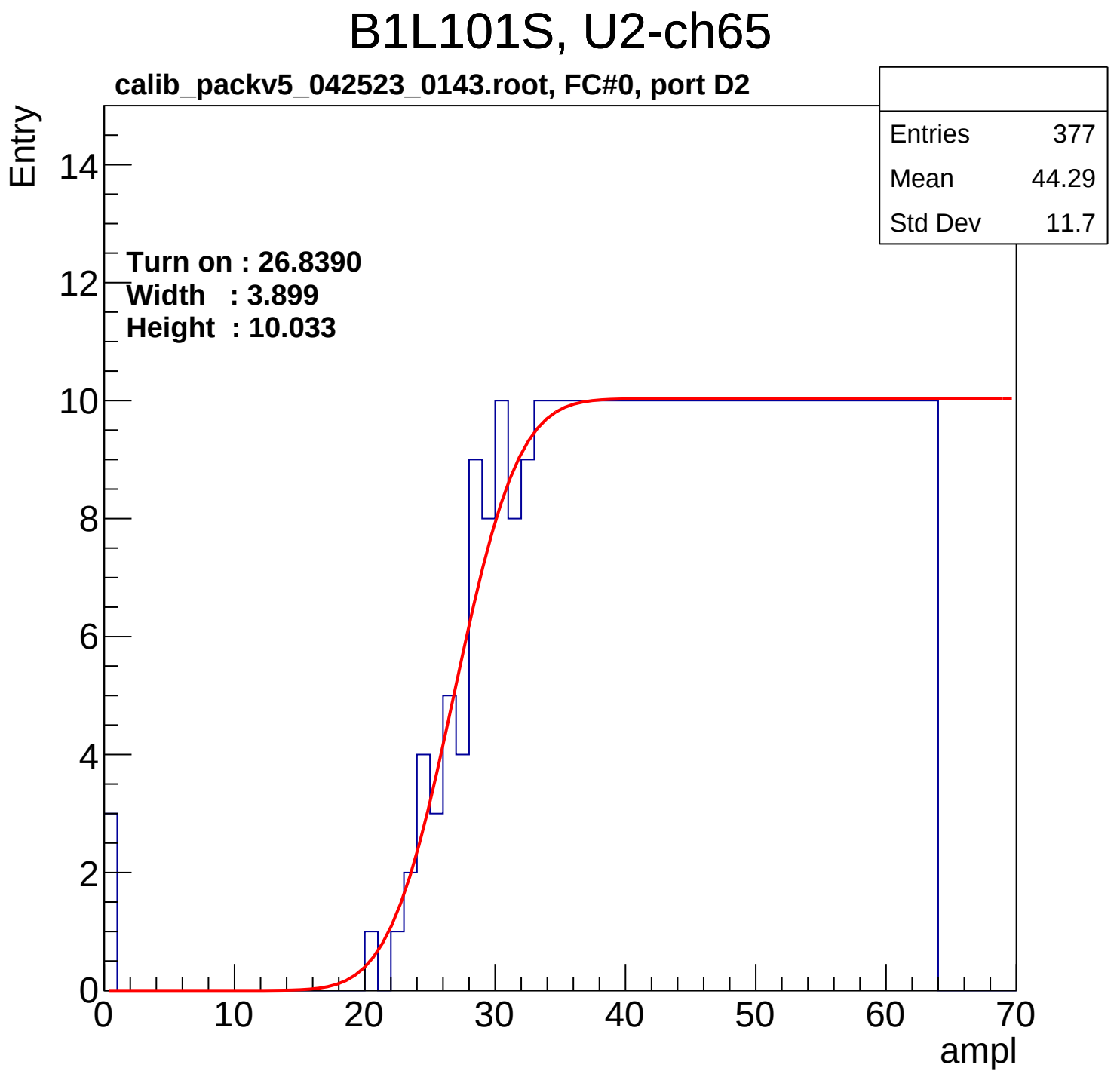
B1L101S, U2-ch65
calib_packv5_042523_0143.root, FC#0, port D2
Entries 377
Mean 44.29
Std Dev 11.7
Turn on : 26.8390
Width : 3.899
Height : 10.033
Entry
ampl
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2
4
6
8
10
12
14
0
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20
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40
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60
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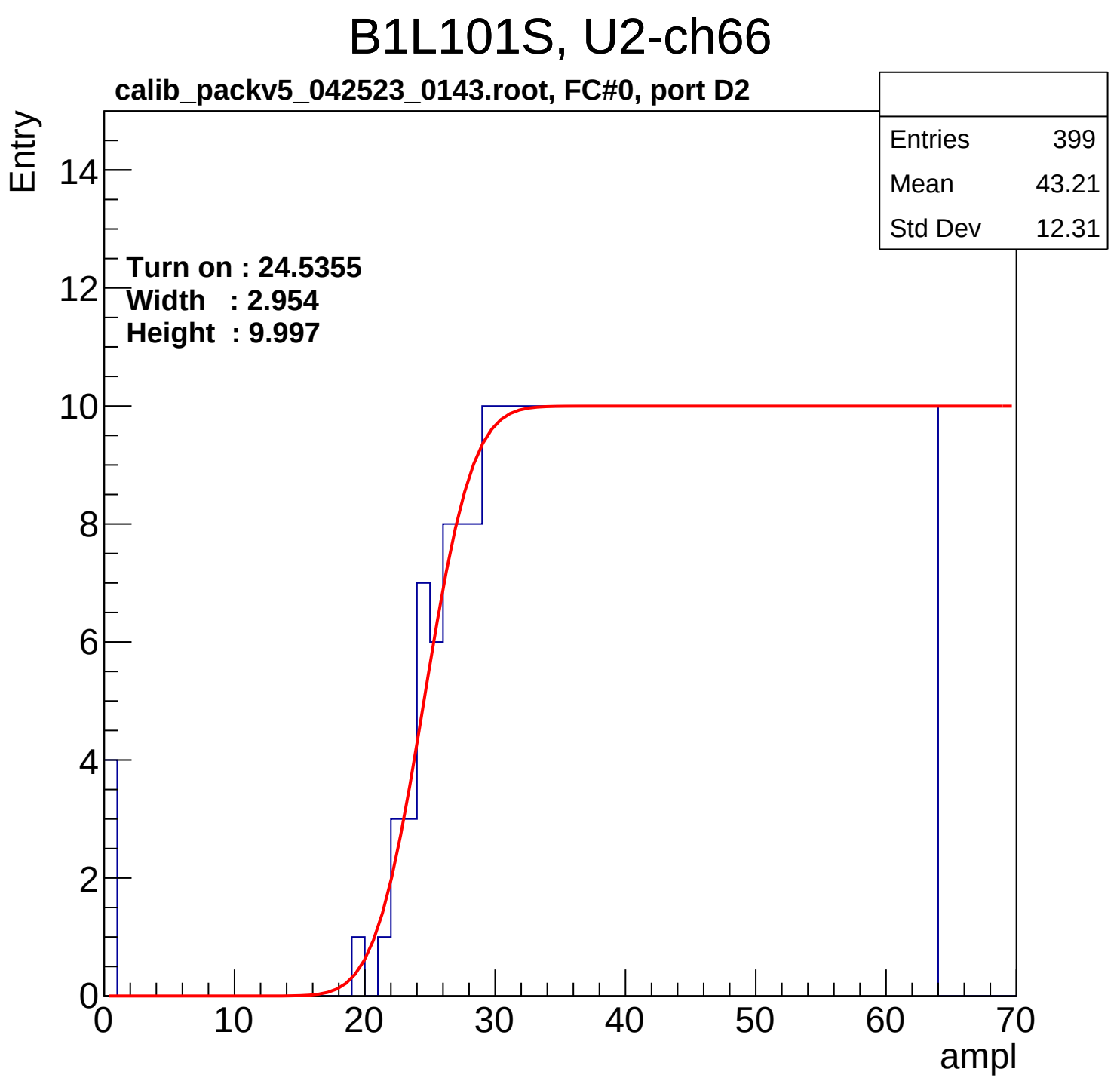
B1L101S, U2-ch66
calib_packv5_042523_0143.root, FC#0, port D2
Entries 399
Mean 43.21
Std Dev 12.31
Turn on : 24.5355
Width : 2.954
Height : 9.997
Entry
ampl
0
2
4
6
8
10
12
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0
10
20
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40
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60
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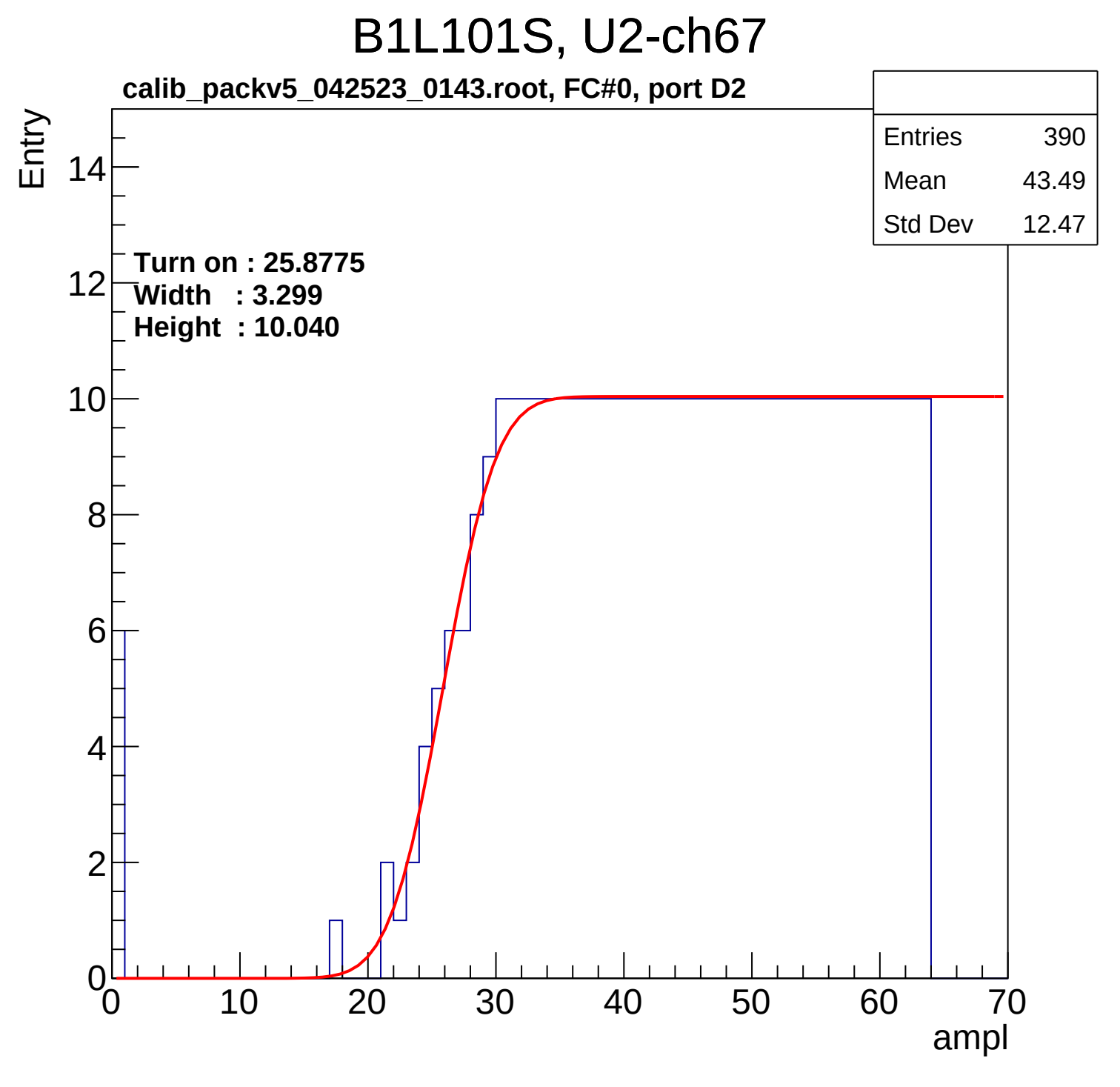
B1L101S, U2-ch67
calib_packv5_042523_0143.root, FC#0, port D2
Entries 390
Mean 43.49
Std Dev 12.47
Turn on : 25.8775
Width : 3.299
Height : 10.040
Entry
ampl
0
2
4
6
8
10
12
14
0
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60
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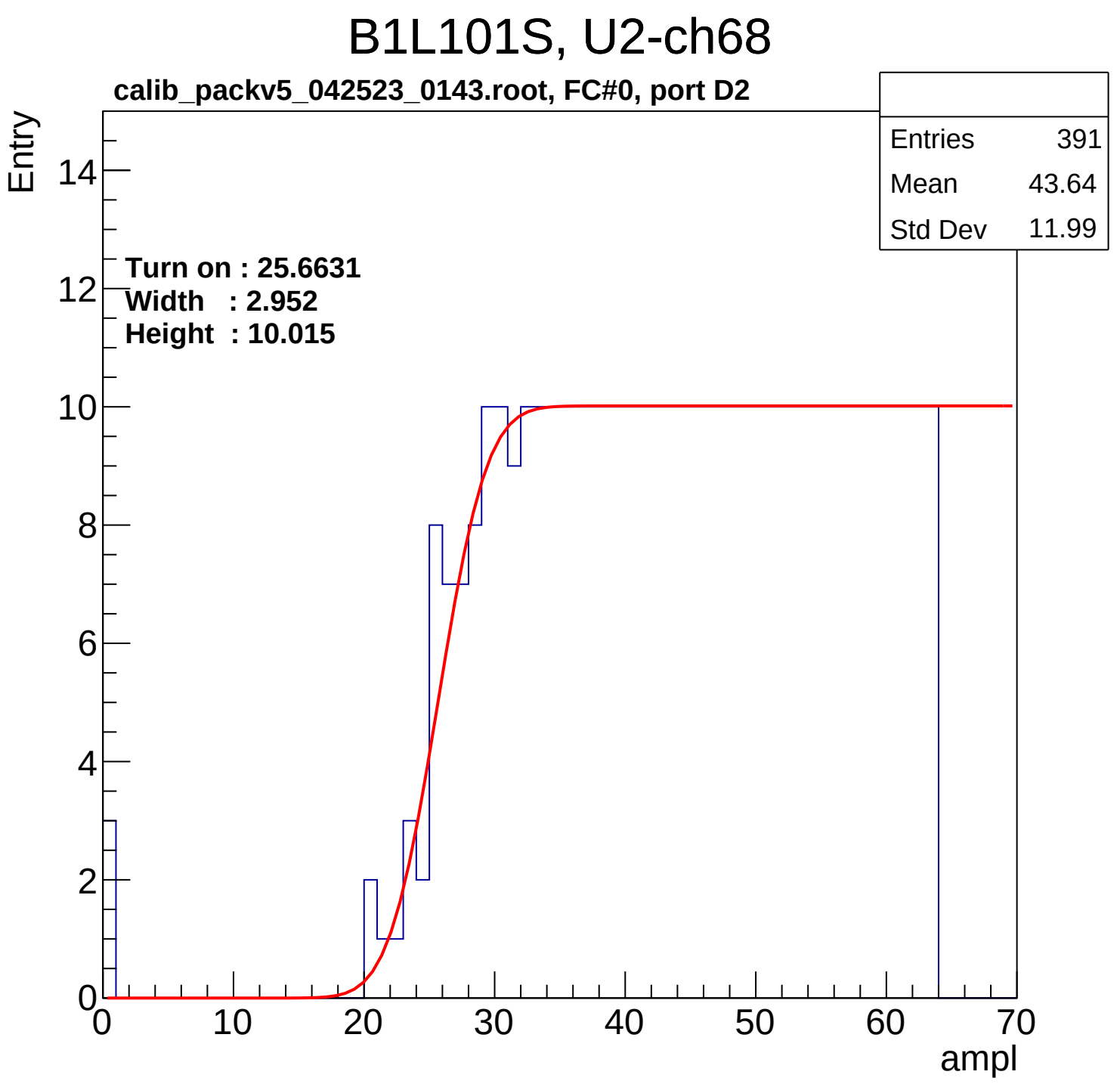
B1L101S, U2-ch68
calib_packv5_042523_0143.root, FC#0, port D2
Entries 391
Mean 43.64
Std Dev 11.99
Turn on : 25.6631
Width : 2.952
Height : 10.015
Entry
ampl
0
2
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6
8
10
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0
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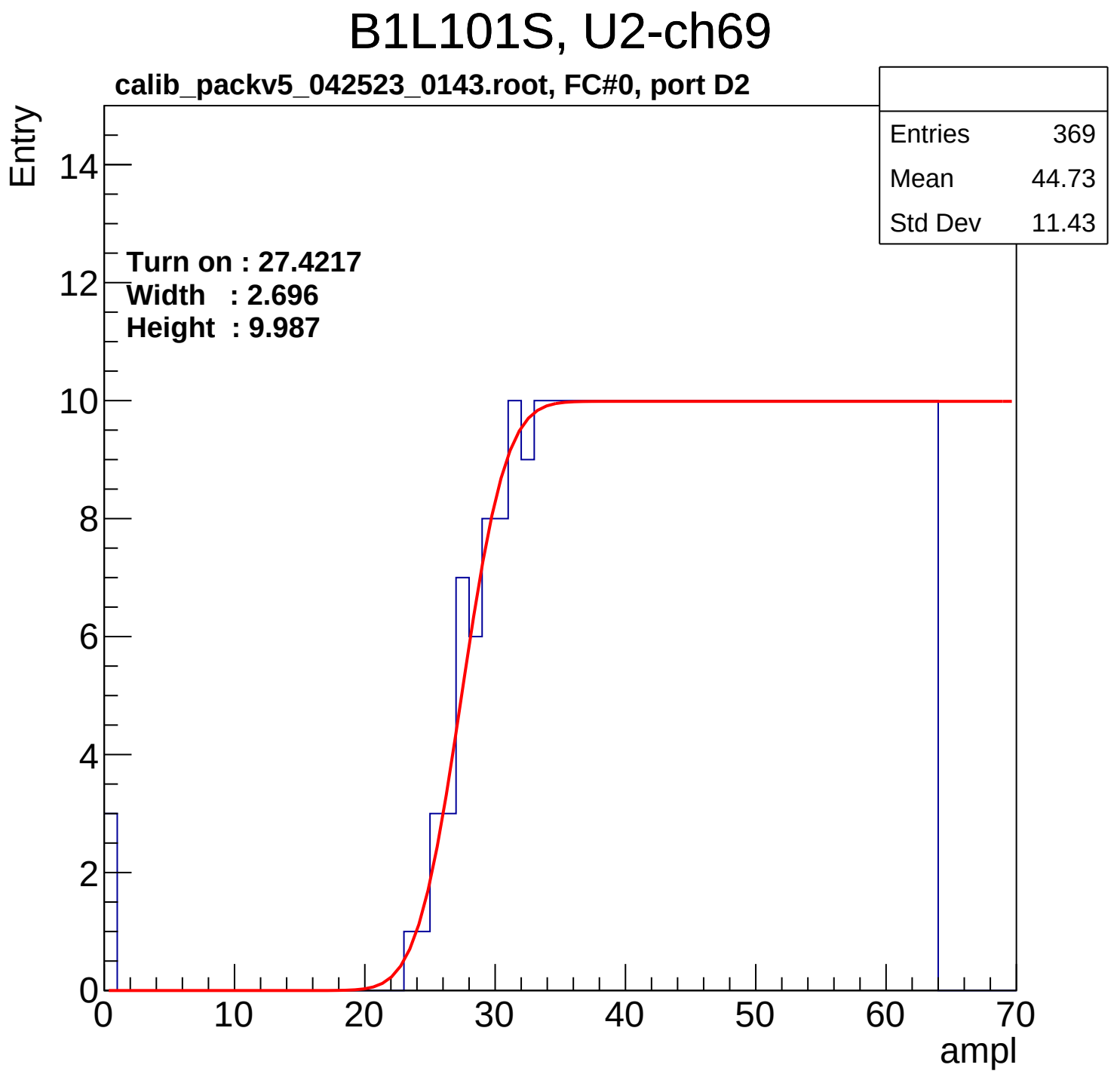
B1L101S, U2-ch69
calib_packv5_042523_0143.root, FC#0, port D2
Entries 369
Mean 44.73
Std Dev 11.43
Turn on : 27.4217
Width : 2.696
Height : 9.987
Entry
ampl
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2
4
6
8
10
12
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0
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20
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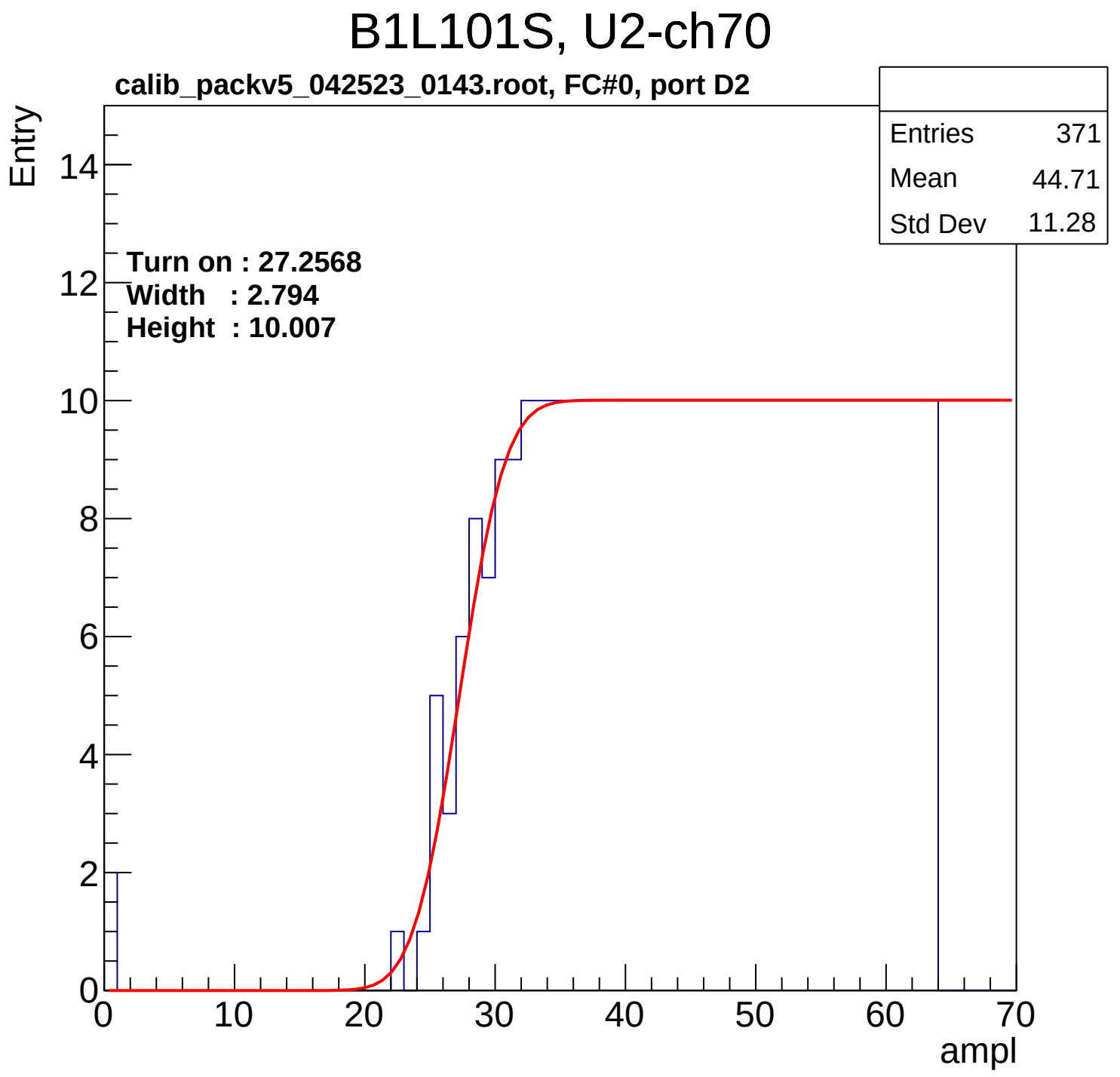
B1L101S, U2-ch70
calib_packv5_042523_0143.root, FC#0, port D2
Entries 371
Mean 44.71
Std Dev 11.28
Turn on : 27.2568
Width : 2.794
Height : 10.007
Entry
ampl
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2
4
6
8
10
12
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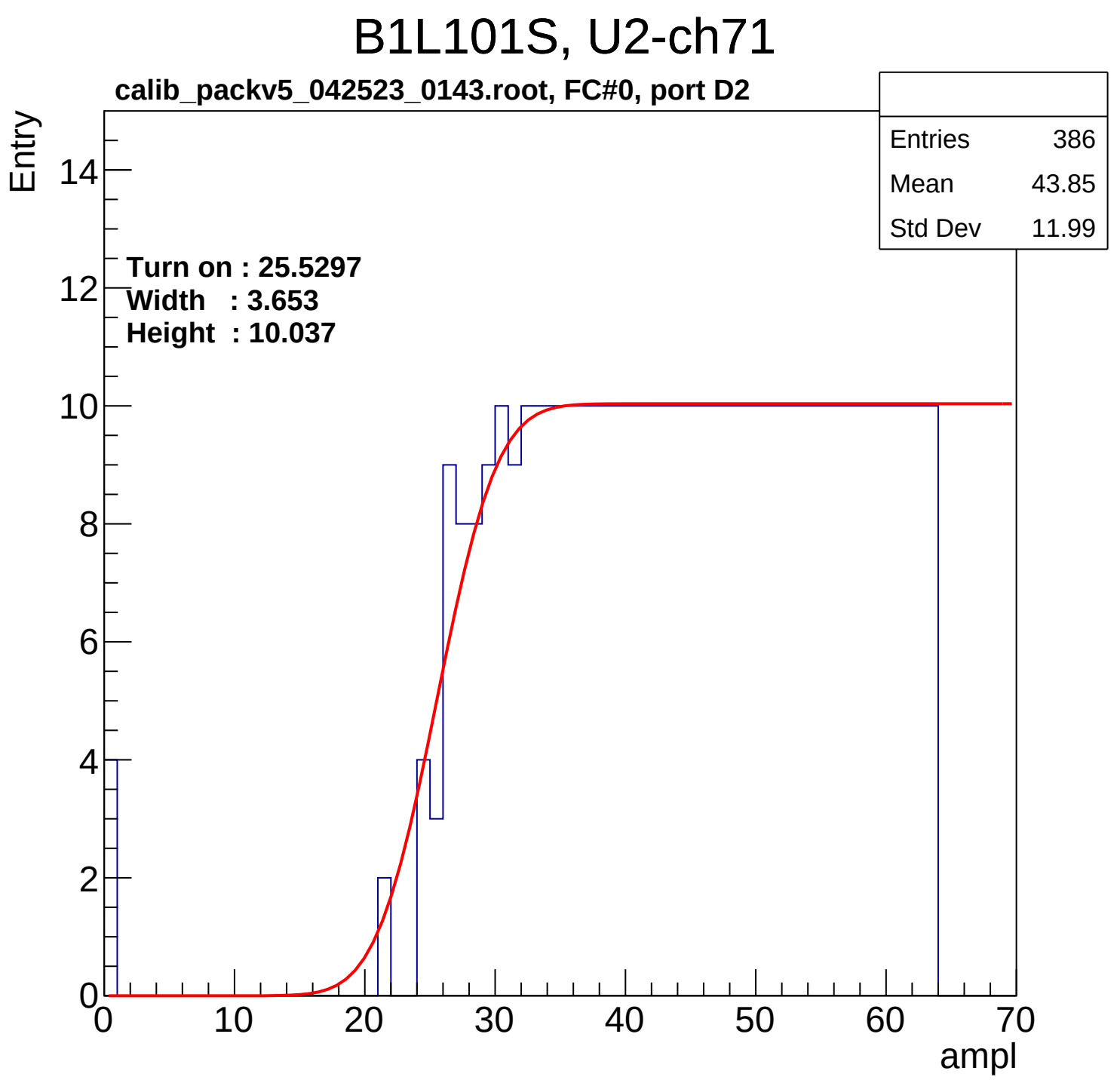
B1L101S, U2-ch71
calib_packv5_042523_0143.root, FC#0, port D2
Entries 386
Mean 43.85
Std Dev 11.99
Turn on : 25.5297
Width : 3.653
Height : 10.037
Entry
ampl
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6
8
10
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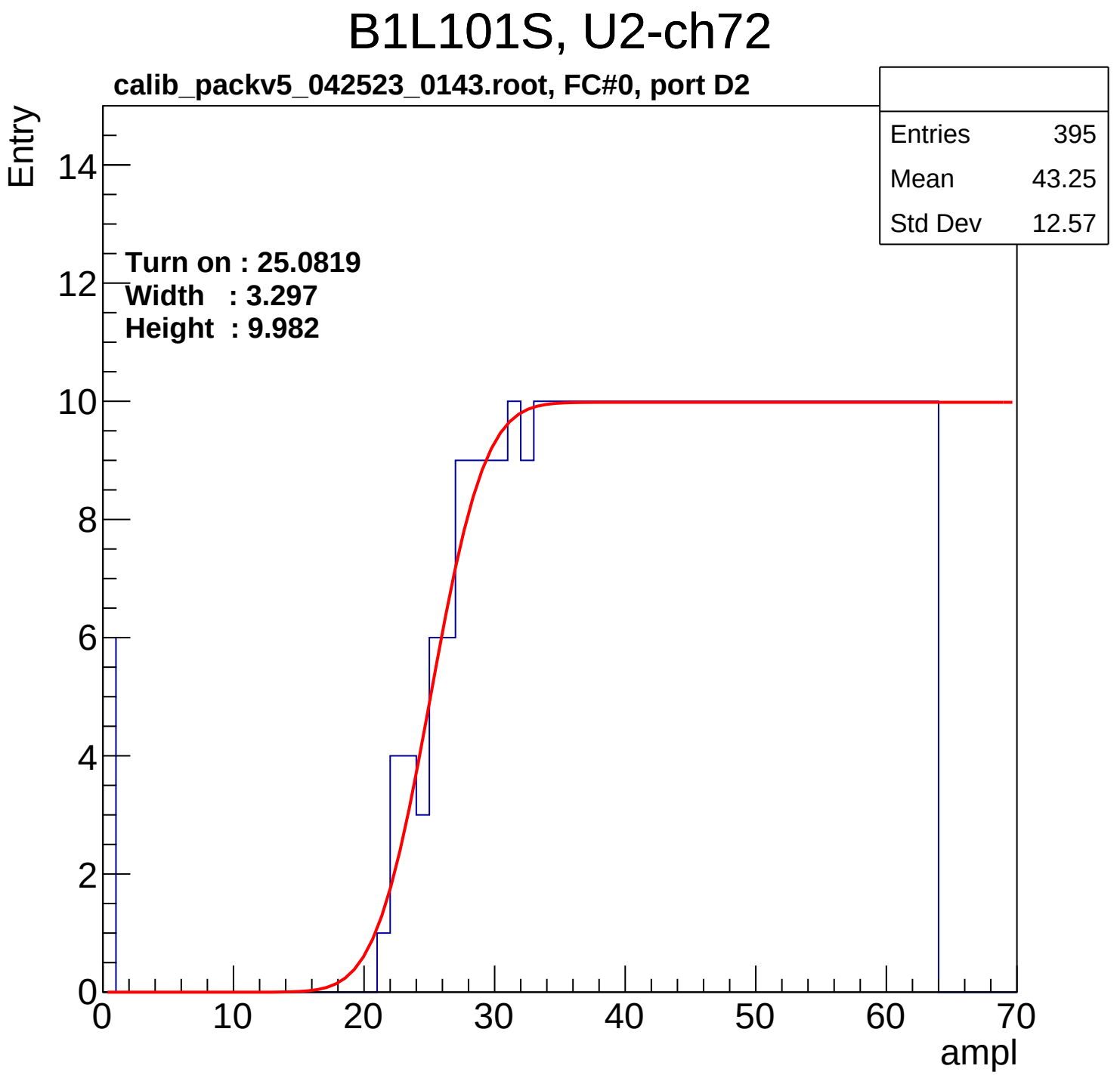
B1L101S, U2-ch72
calib_packv5_042523_0143.root, FC#0, port D2
Entries 395
Mean 43.25
Std Dev 12.57
Turn on : 25.0819
Width : 3.297
Height : 9.982
Entry
ampl
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6
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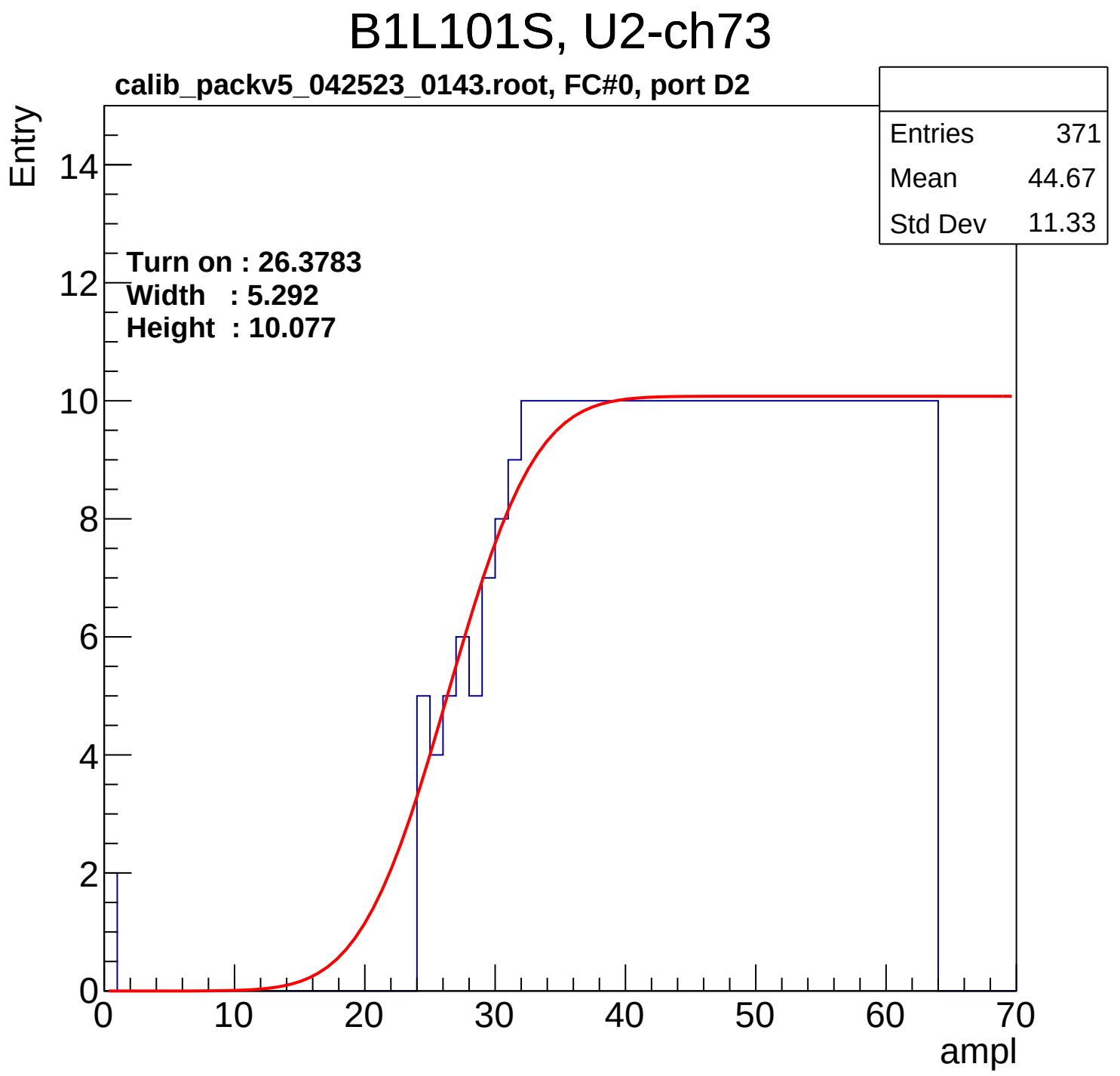
B1L101S, U2-ch73
calib_packv5_042523_0143.root, FC#0, port D2
Entries 371
Mean 44.67
Std Dev 11.33
Turn on : 26.3783
Width : 5.292
Height : 10.077
Entry
ampl
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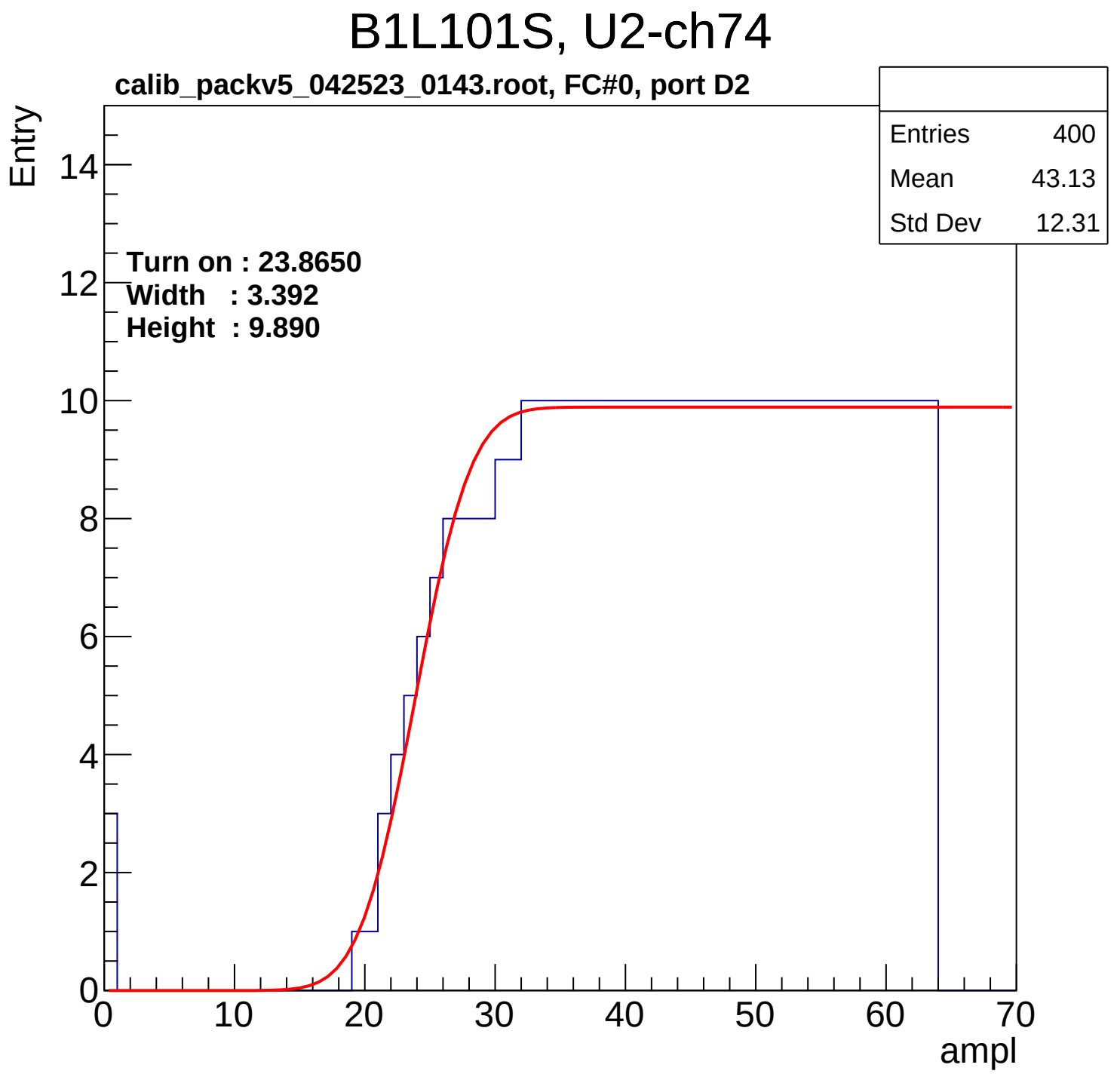
B1L101S, U2-ch74
calib_packv5_042523_0143.root, FC#0, port D2
Entries 400
Mean 43.13
Std Dev 12.31
Turn on : 23.8650
Width : 3.392
Height : 9.890
Entry
ampl
0
2
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8
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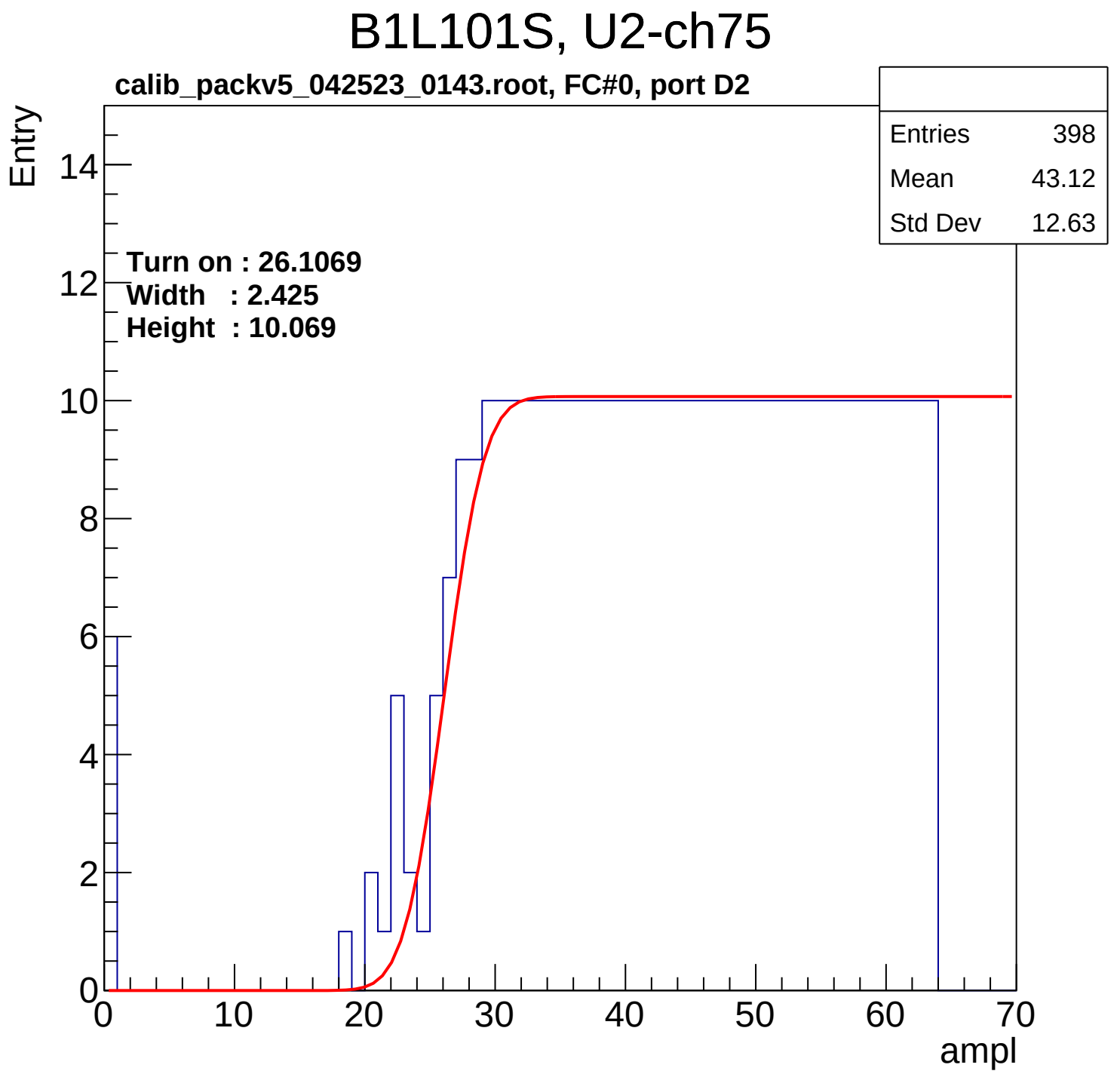
B1L101S, U2-ch75
calib_packv5_042523_0143.root, FC#0, port D2
Entries 398
Mean 43.12
Std Dev 12.63
Turn on : 26.1069
Width : 2.425
Height : 10.069
Entry
ampl
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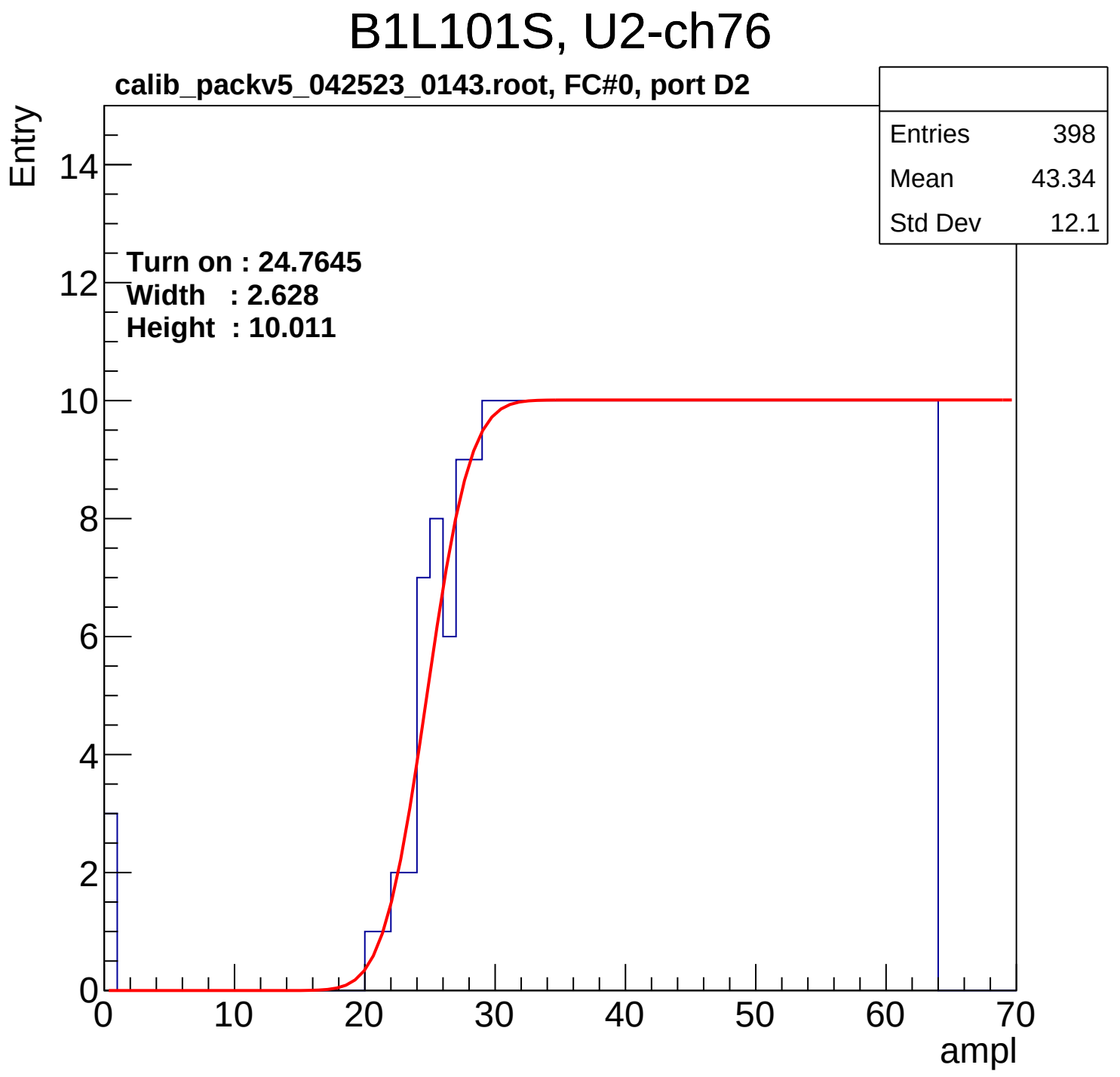
B1L101S, U2-ch76
calib_packv5_042523_0143.root, FC#0, port D2
Entries 398
Mean 43.34
Std Dev 12.1
Turn on : 24.7645
Width : 2.628
Height : 10.011
Entry
ampl
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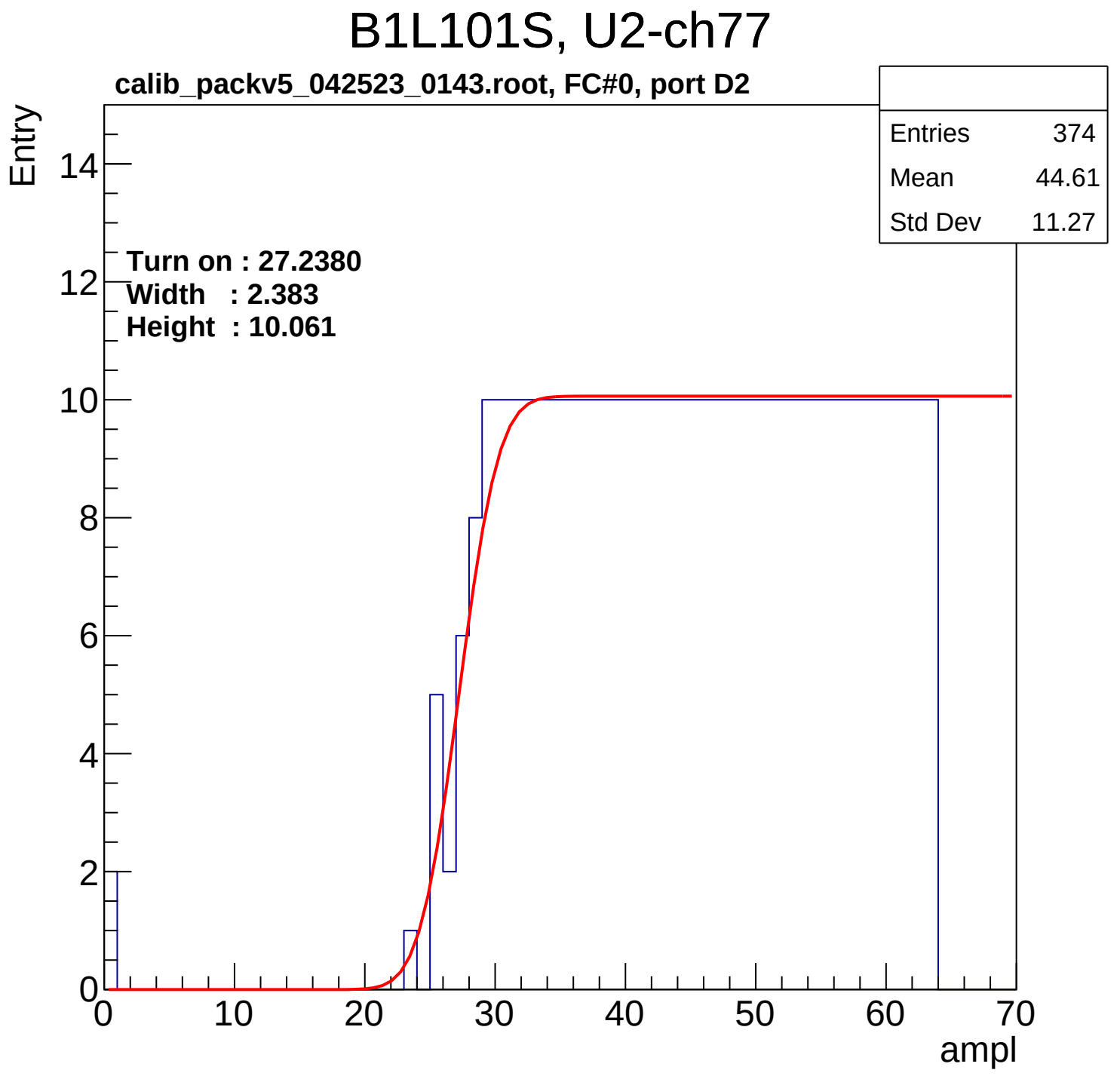
B1L101S, U2-ch77
calib_packv5_042523_0143.root, FC#0, port D2
Entries 374
Mean 44.61
Std Dev 11.27
Turn on : 27.2380
Width : 2.383
Height : 10.061
Entry
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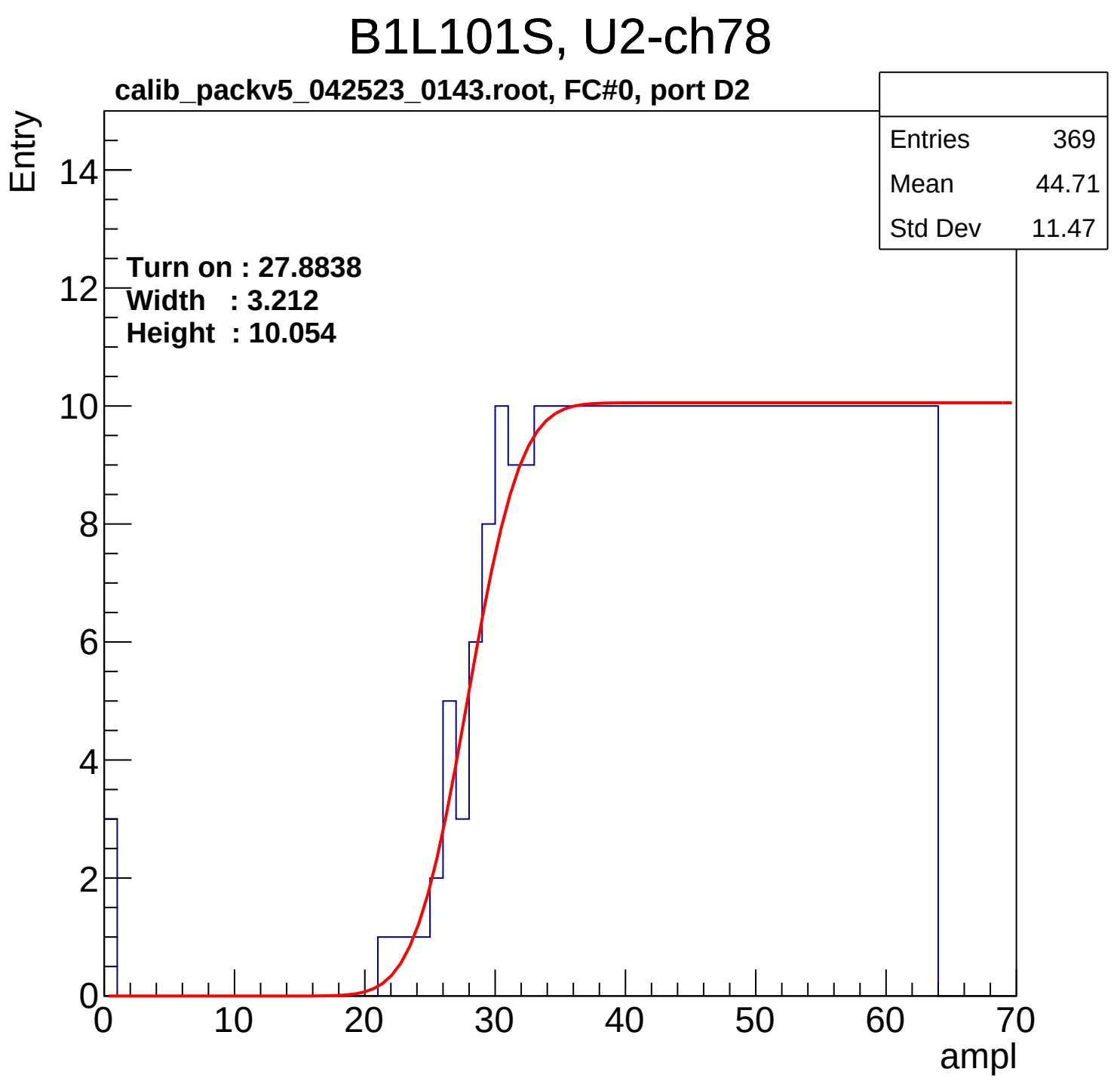
B1L101S, U2-ch78
calib_packv5_042523_0143.root, FC#0, port D2
Entries 369
Mean 44.71
Std Dev 11.47
Turn on : 27.8838
Width : 3.212
Height : 10.054
Entry
ampl
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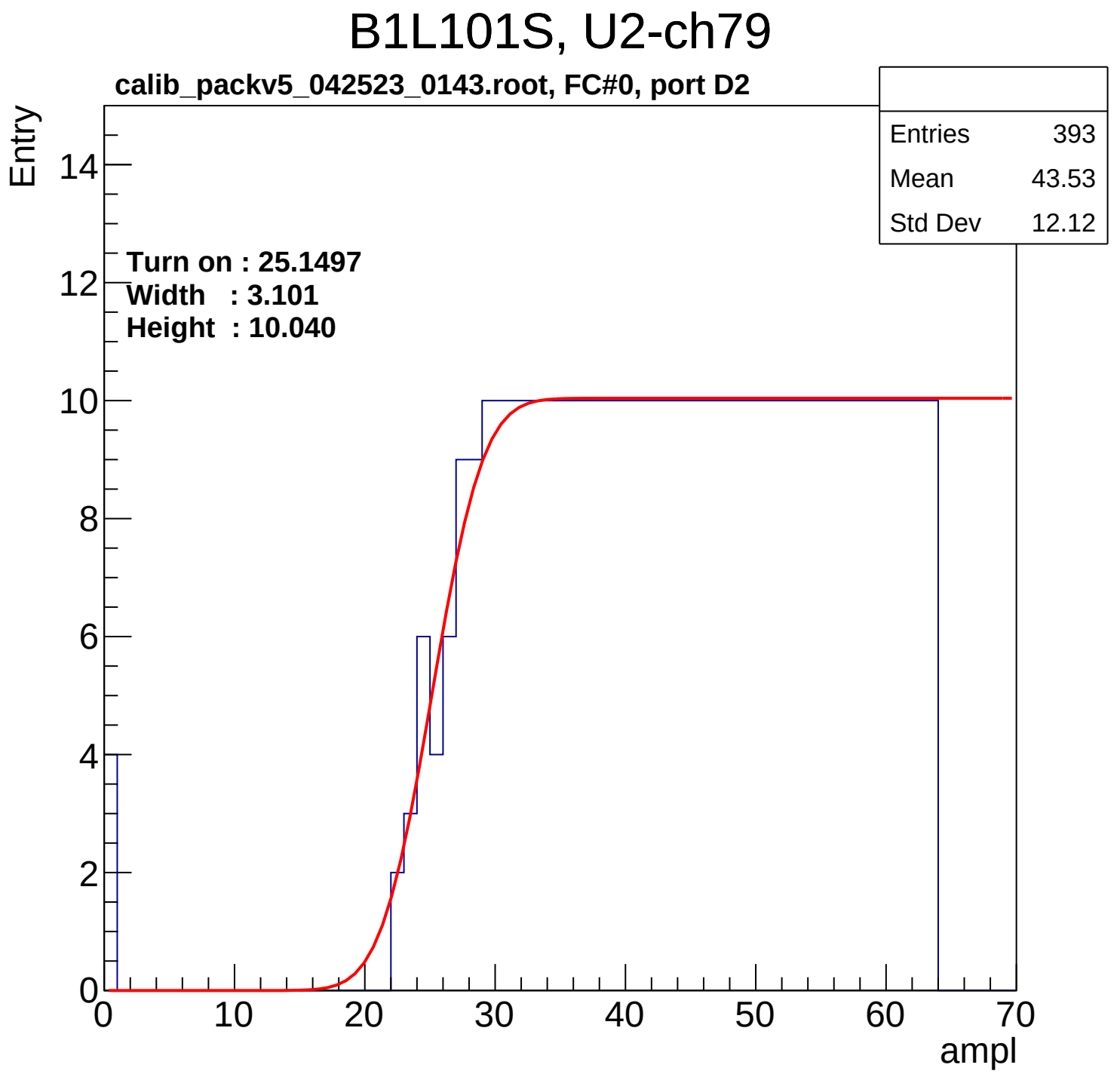
B1L101S, U2-ch79
calib_packv5_042523_0143.root, FC#0, port D2
Entries 393
Mean 43.53
Std Dev 12.12
Turn on : 25.1497
Width : 3.101
Height : 10.040
Entry
ampl
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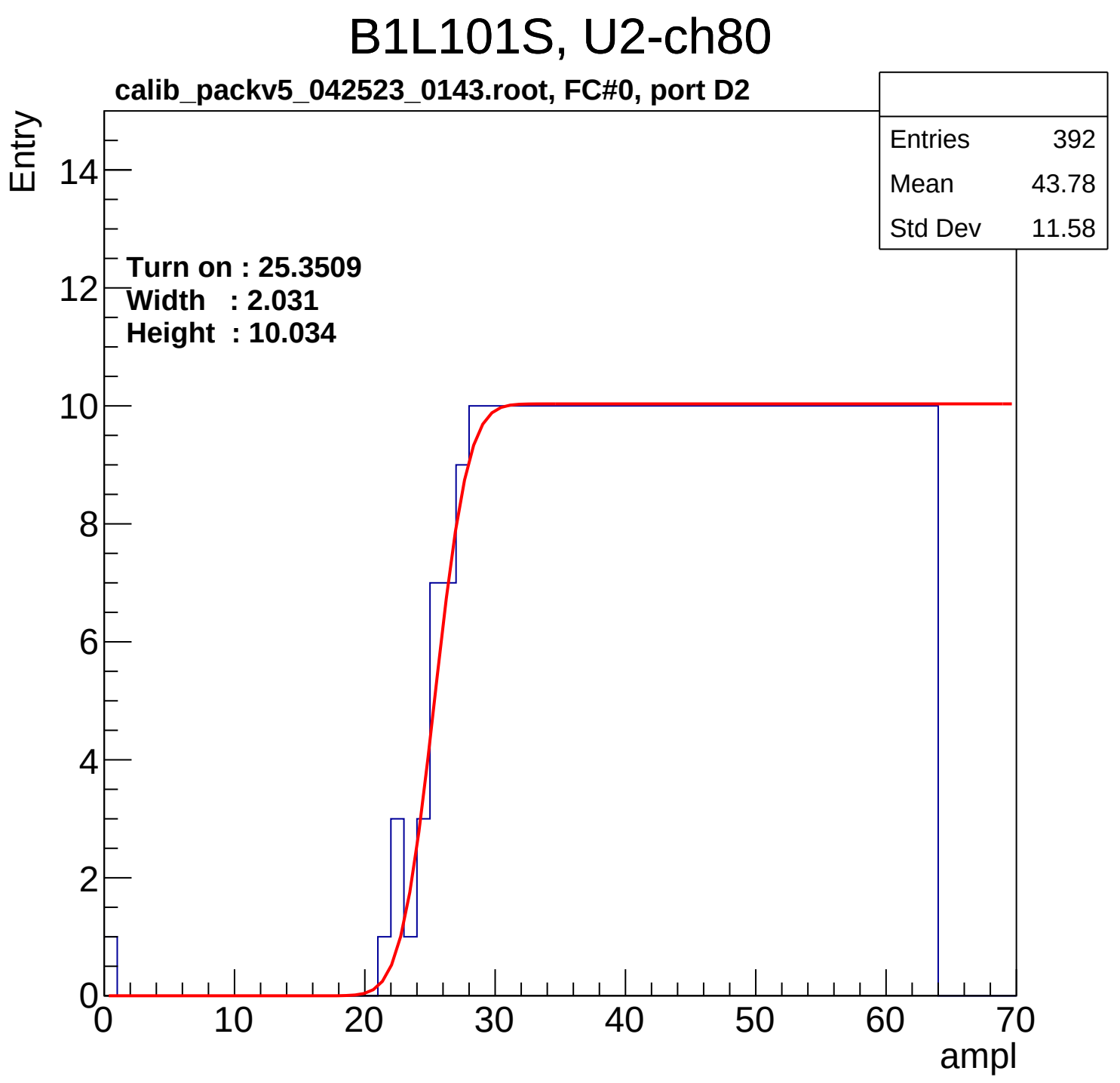
B1L101S, U2-ch80
calib_packv5_042523_0143.root, FC#0, port D2
Entries 392
Mean 43.78
Std Dev 11.58
Turn on : 25.3509
Width : 2.031
Height : 10.034
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ampl
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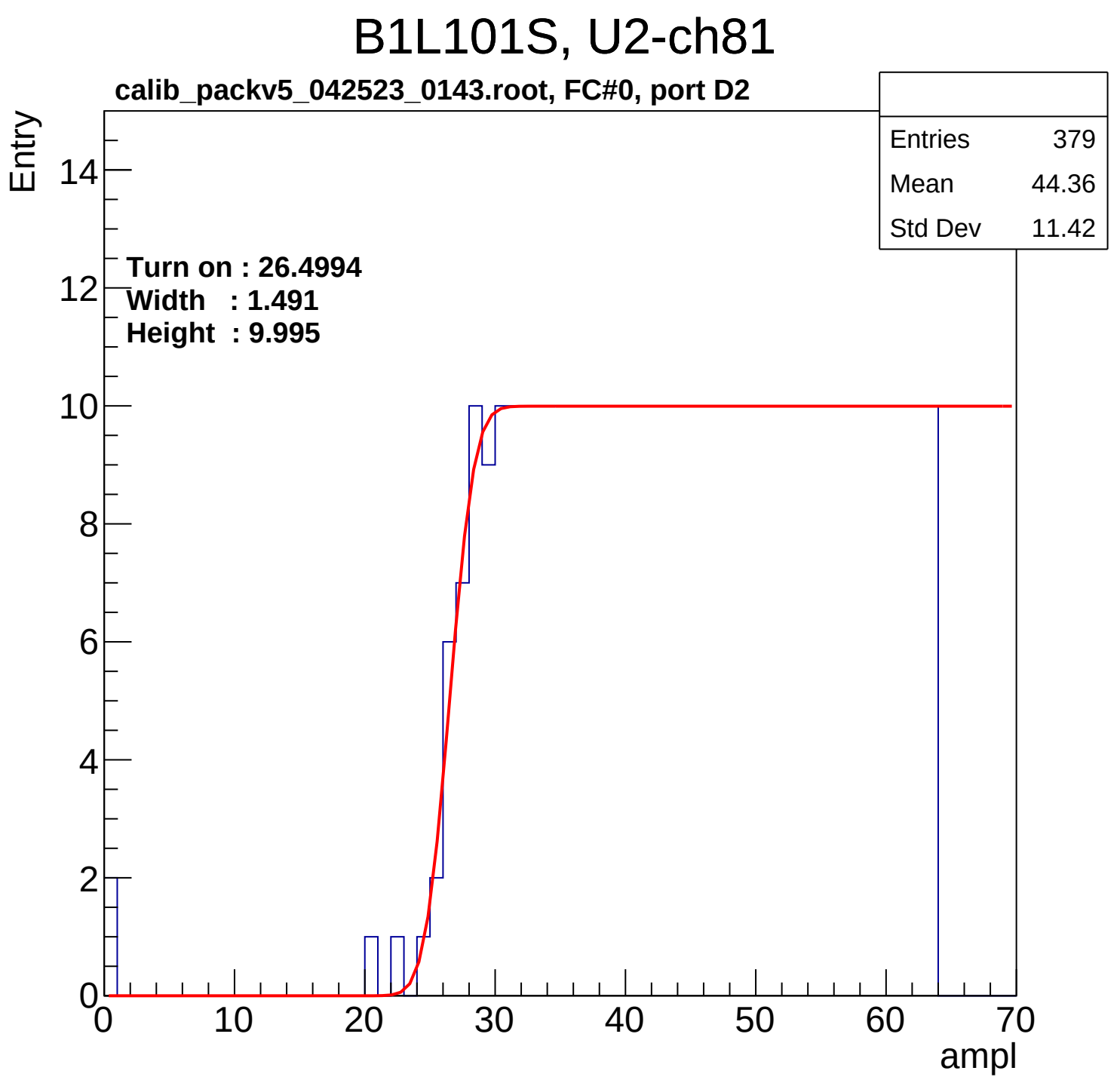
B1L101S, U2-ch81
calib_packv5_042523_0143.root, FC#0, port D2
Entries 379
Mean 44.36
Std Dev 11.42
Turn on : 26.4994
Width : 1.491
Height : 9.995
Entry
ampl
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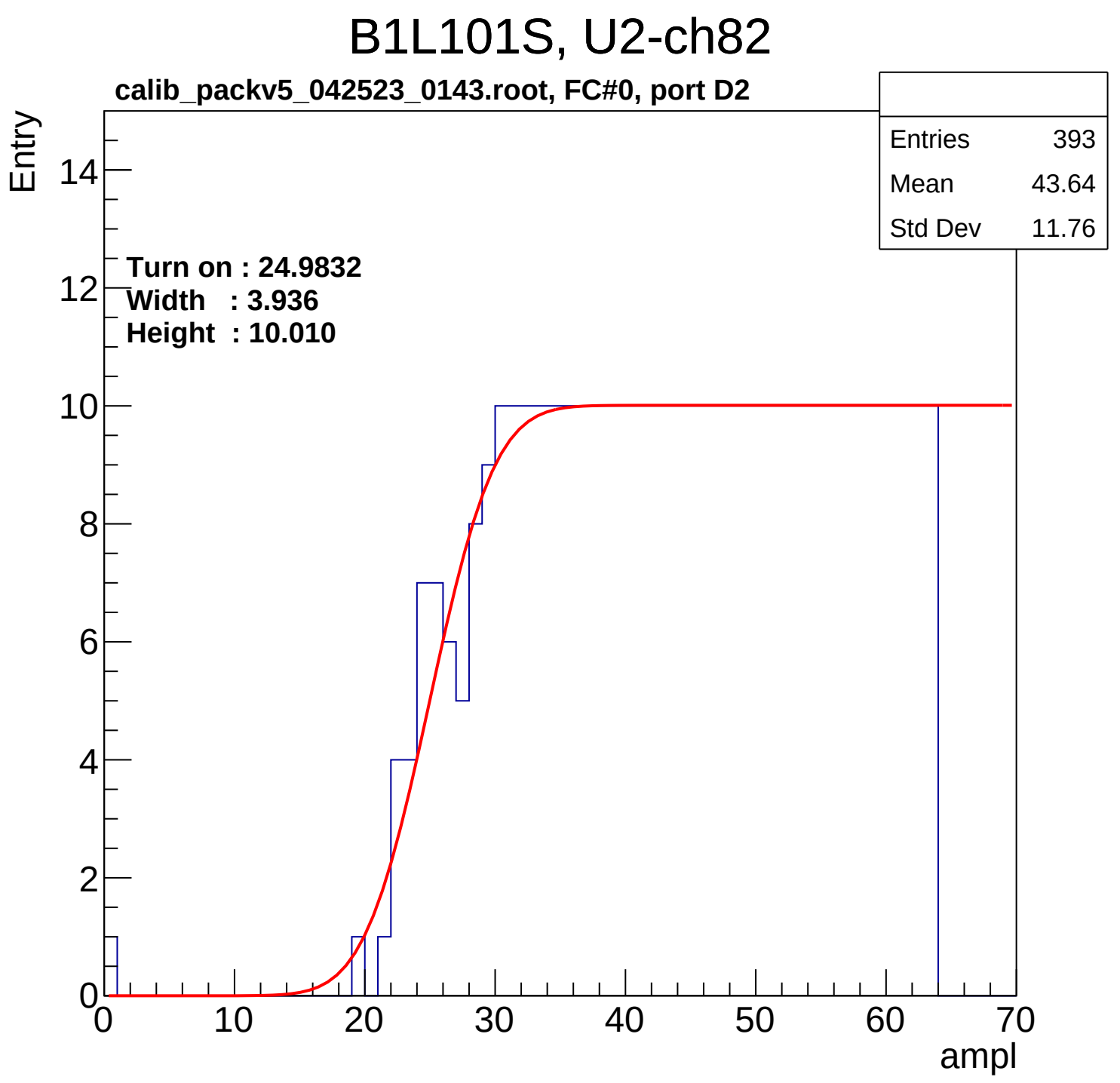
B1L101S, U2-ch82
calib_packv5_042523_0143.root, FC#0, port D2
Entries 393
Mean 43.64
Std Dev 11.76
Turn on : 24.9832
Width : 3.936
Height : 10.010
Entry
ampl
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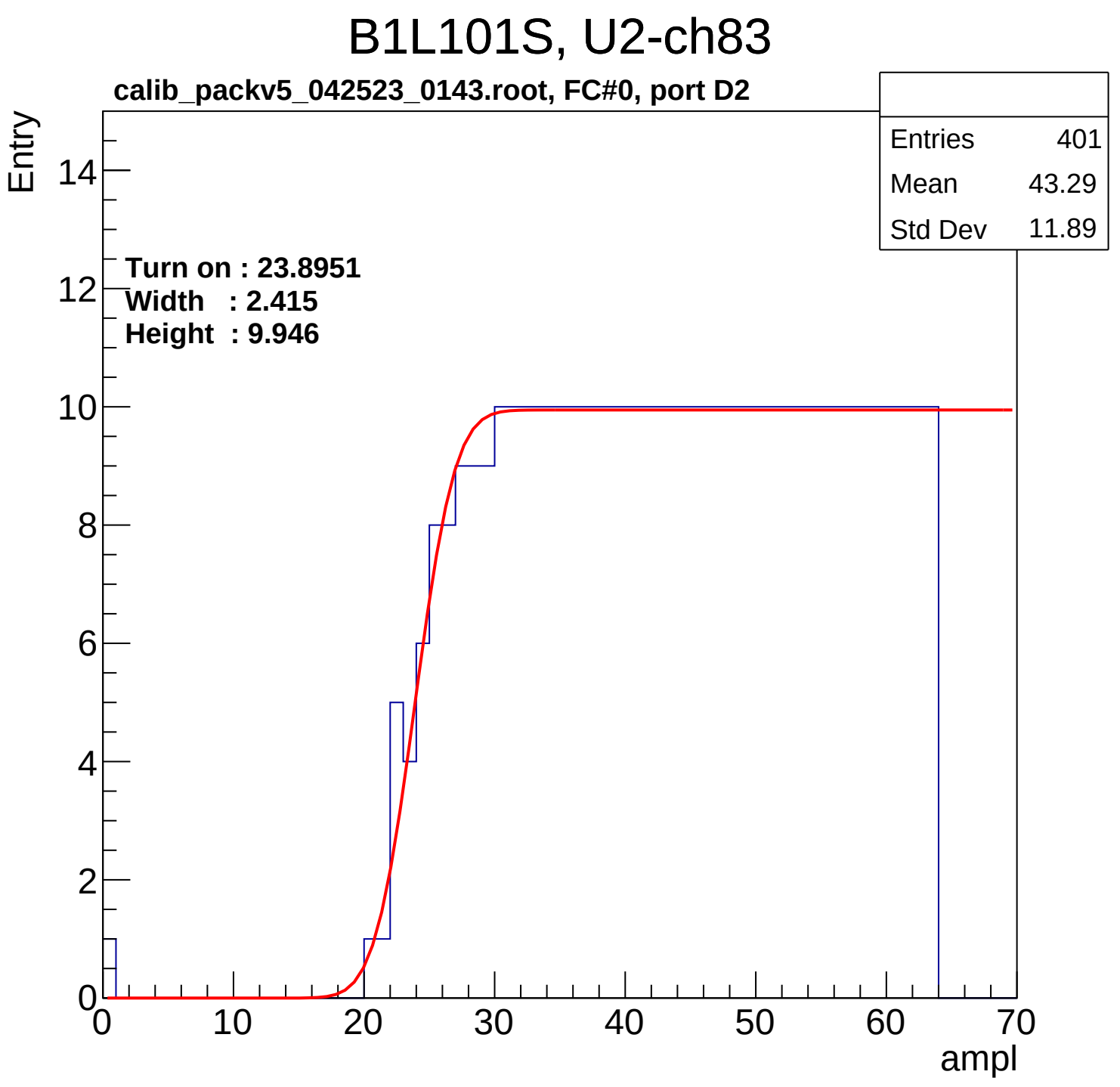
B1L101S, U2-ch83
calib_packv5_042523_0143.root, FC#0, port D2
Entries 401
Mean 43.29
Std Dev 11.89
Turn on : 23.8951
Width : 2.415
Height : 9.946
Entry
ampl
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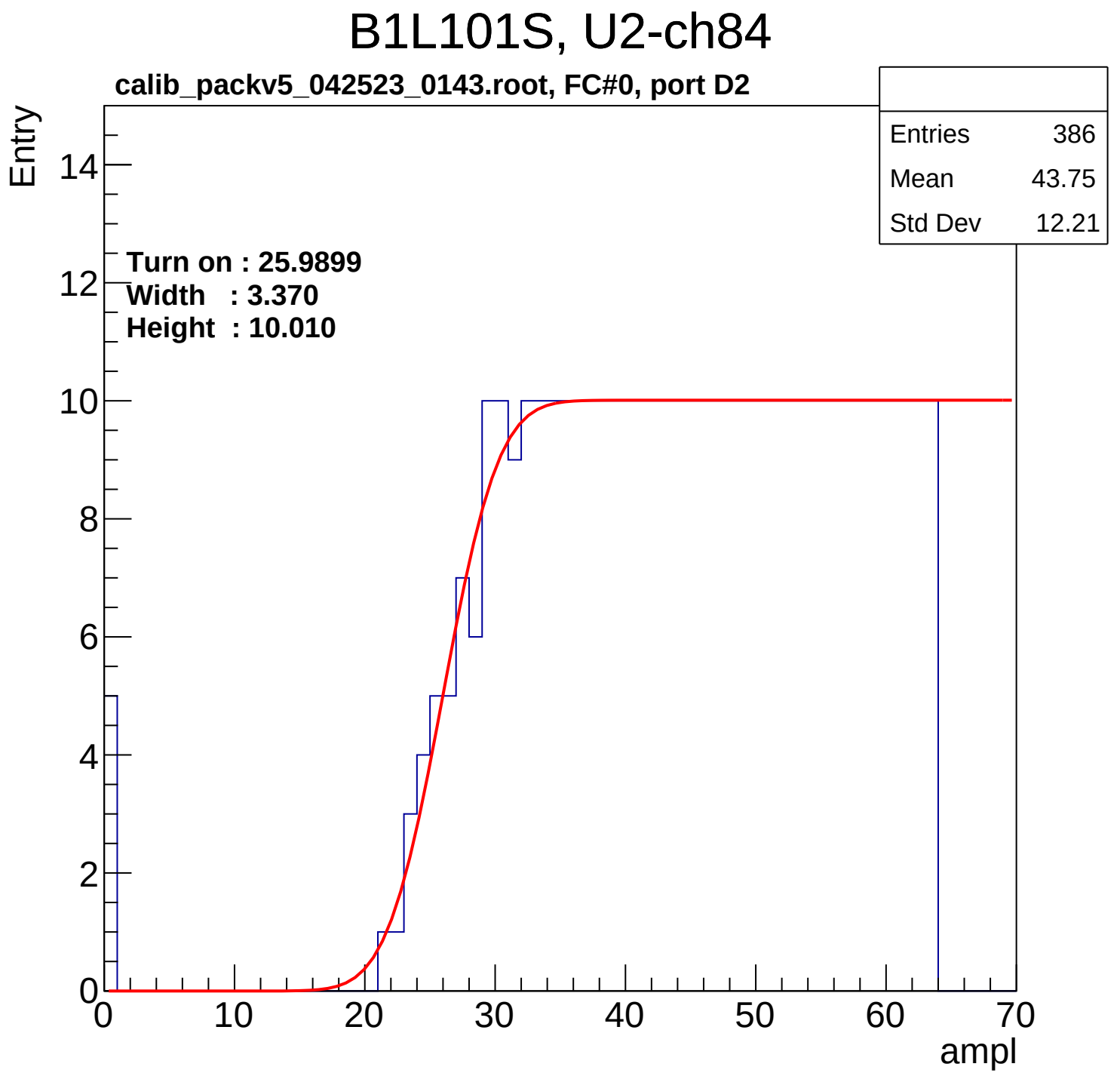
B1L101S, U2-ch84
calib_packv5_042523_0143.root, FC#0, port D2
Entries 386
Mean 43.75
Std Dev 12.21
Turn on : 25.9899
Width : 3.370
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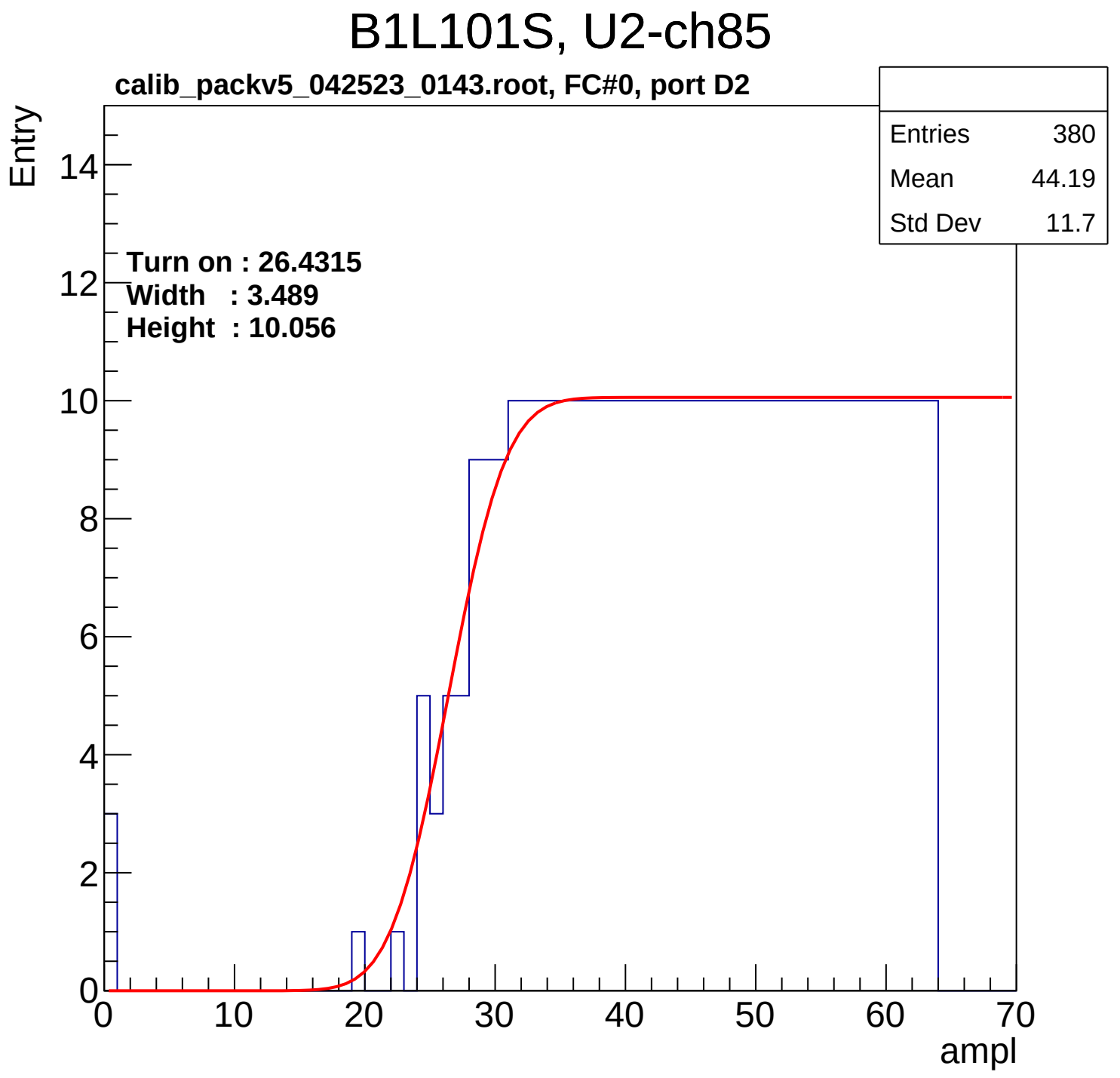
B1L101S, U2-ch85
calib_packv5_042523_0143.root, FC#0, port D2
Entries 380
Mean 44.19
Std Dev 11.7
Turn on : 26.4315
Width : 3.489
Height : 10.056
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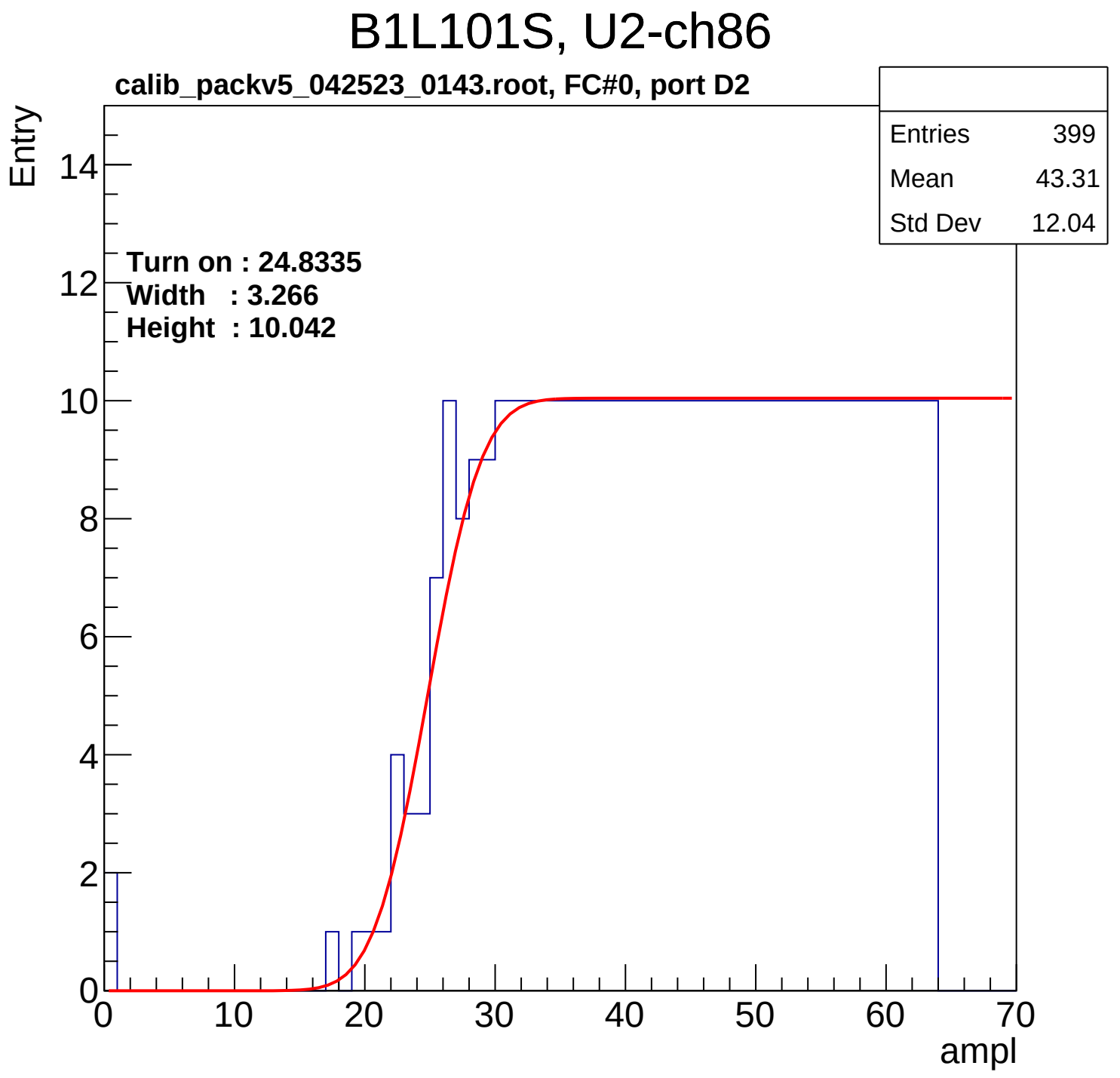
B1L101S, U2-ch86
calib_packv5_042523_0143.root, FC#0, port D2
Entries 399
Mean 43.31
Std Dev 12.04
Turn on : 24.8335
Width : 3.266
Height : 10.042
Entry
ampl
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4
6
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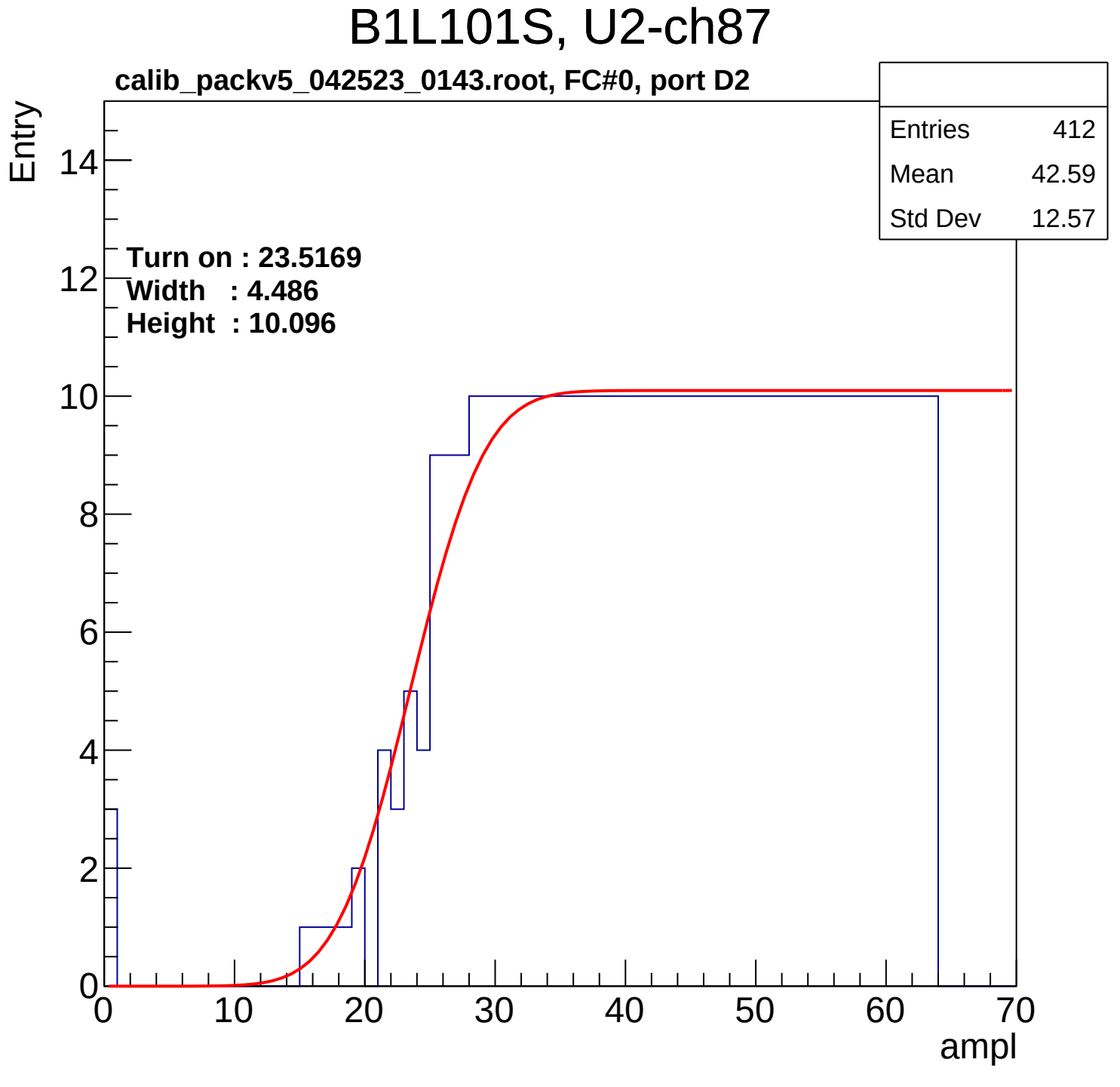
B1L101S, U2-ch87
calib_packv5_042523_0143.root, FC#0, port D2
Entries 412
Mean 42.59
Std Dev 12.57
Turn on : 23.5169
Width : 4.486
Height : 10.096
Entry
ampl
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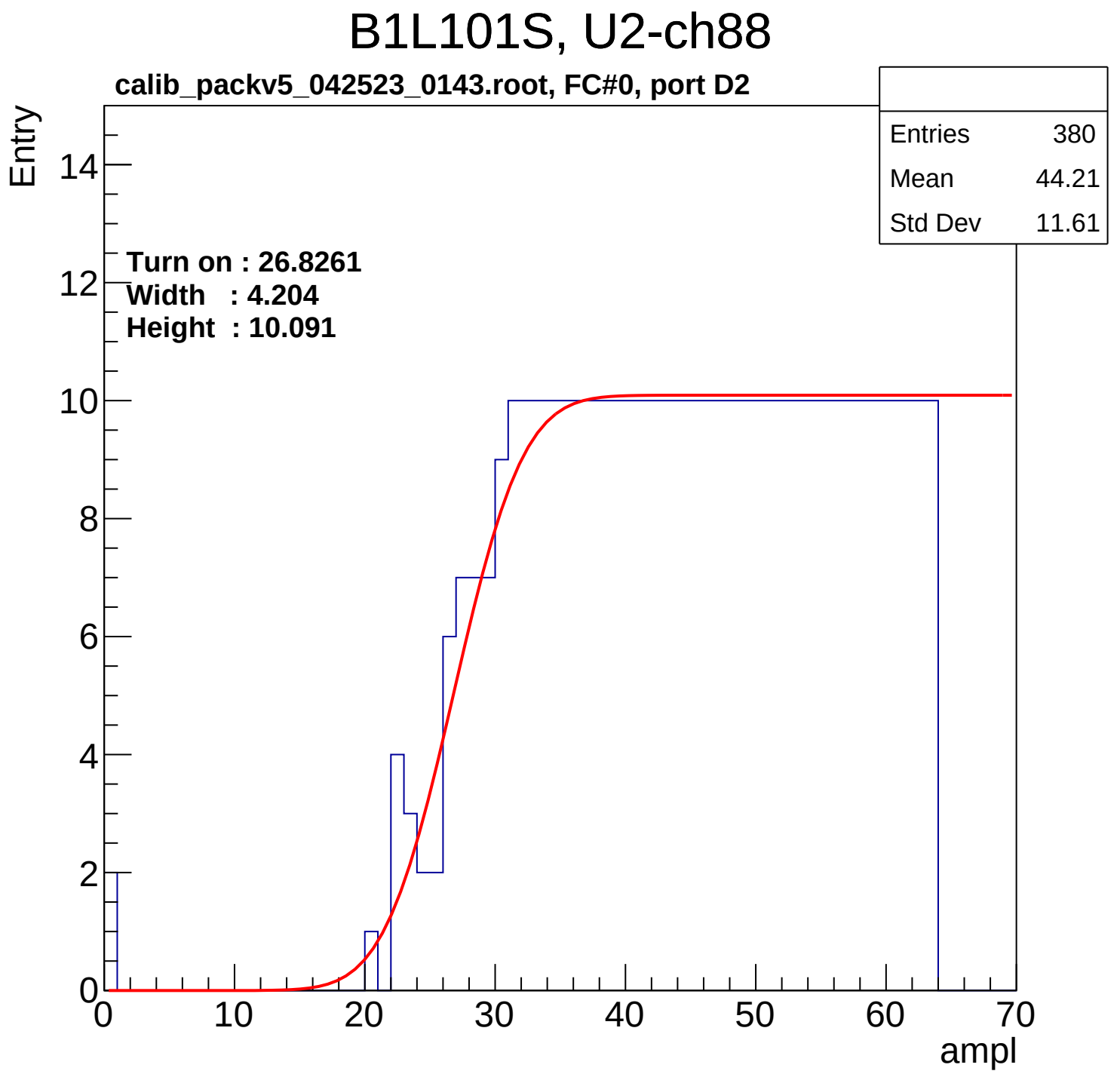
B1L101S, U2-ch88
calib_packv5_042523_0143.root, FC#0, port D2
Entries 380
Mean 44.21
Std Dev 11.61
Turn on : 26.8261
Width : 4.204
Height : 10.091
Entry
ampl
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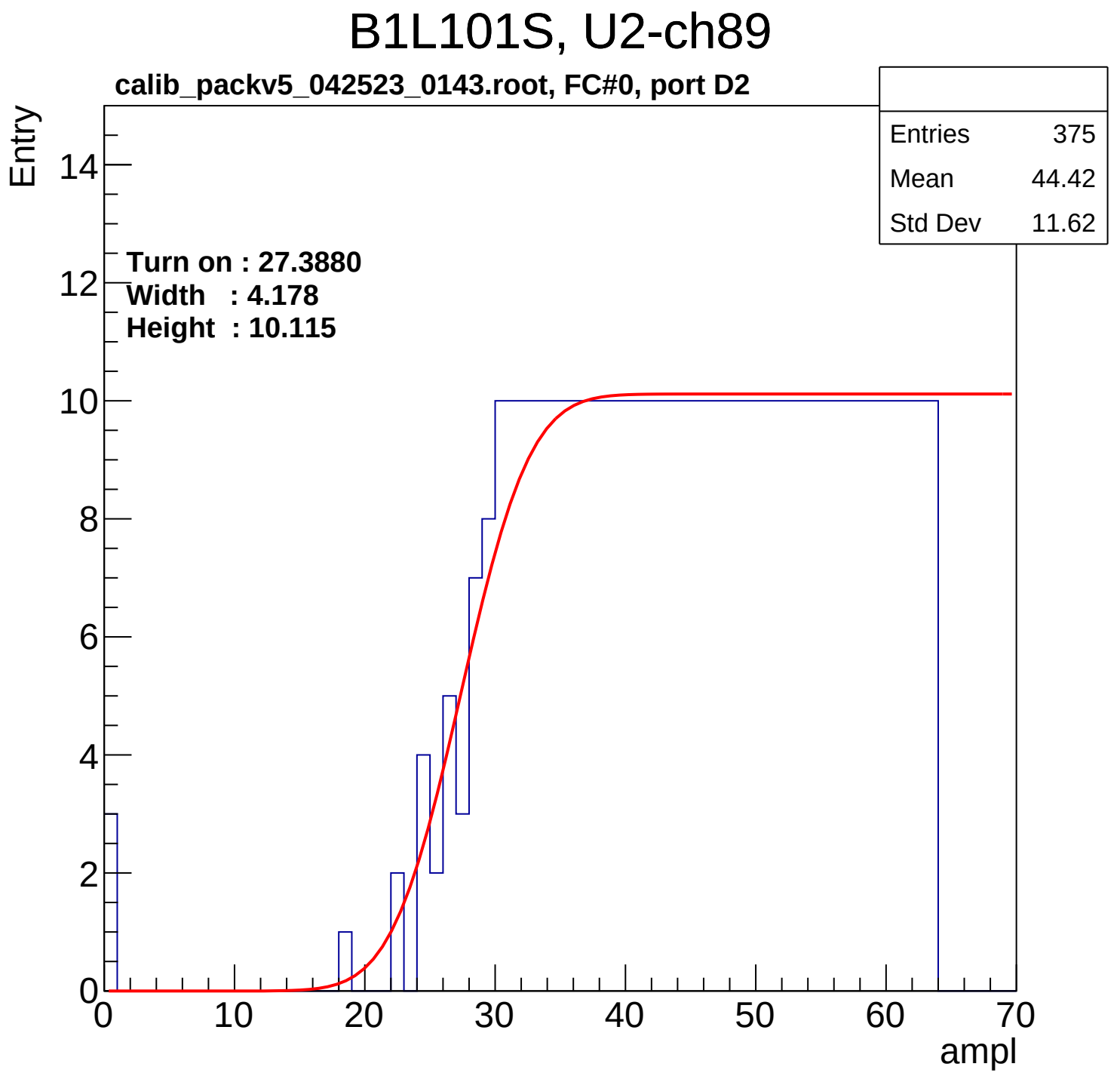
B1L101S, U2-ch89
calib_packv5_042523_0143.root, FC#0, port D2
Entries 375
Mean 44.42
Std Dev 11.62
Turn on : 27.3880
Width : 4.178
Height : 10.115
Entry
ampl
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4
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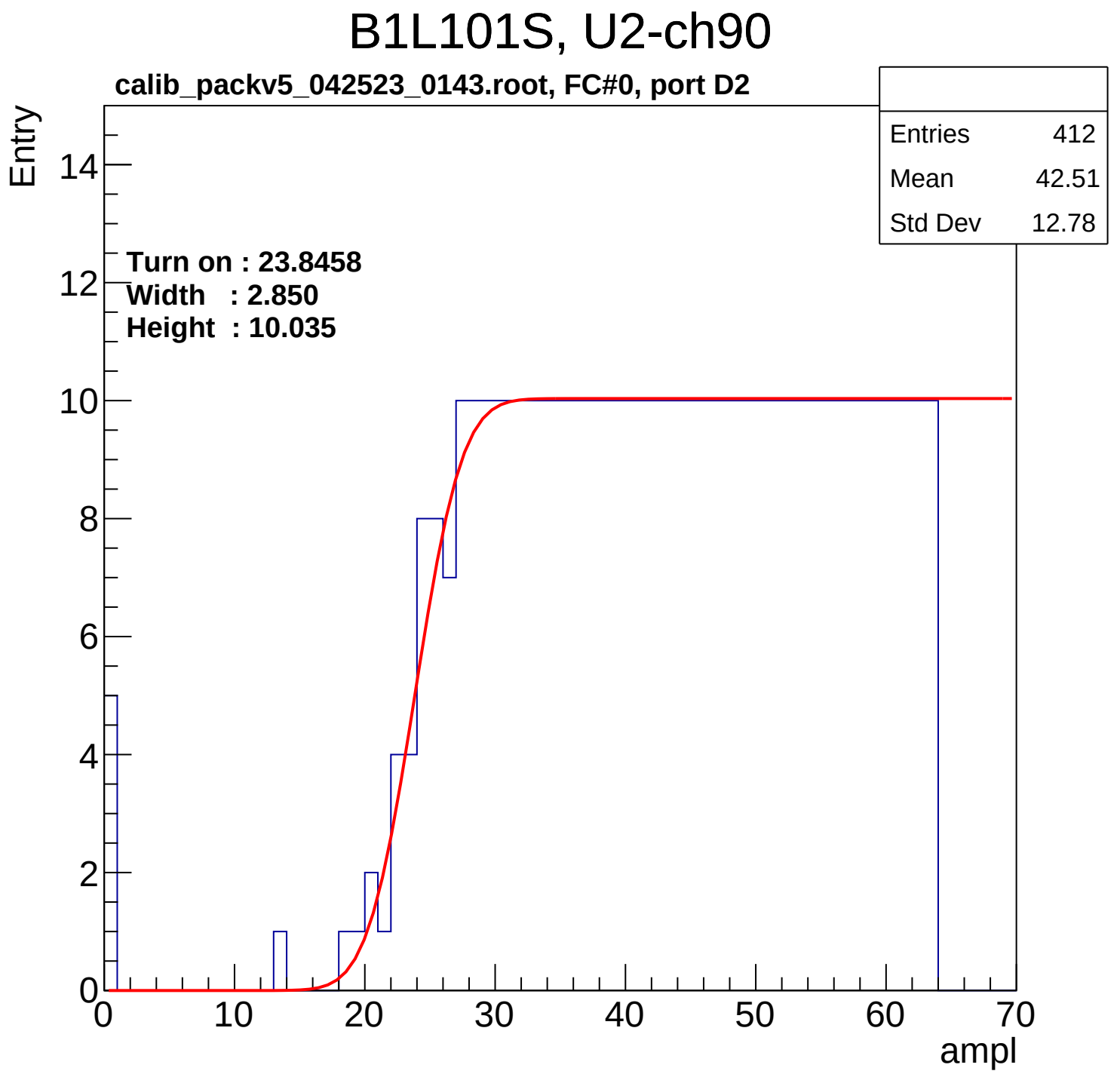
B1L101S, U2-ch90
calib_packv5_042523_0143.root, FC#0, port D2
Entries 412
Mean 42.51
Std Dev 12.78
Turn on : 23.8458
Width : 2.850
Height : 10.035
Entry
ampl
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2
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8
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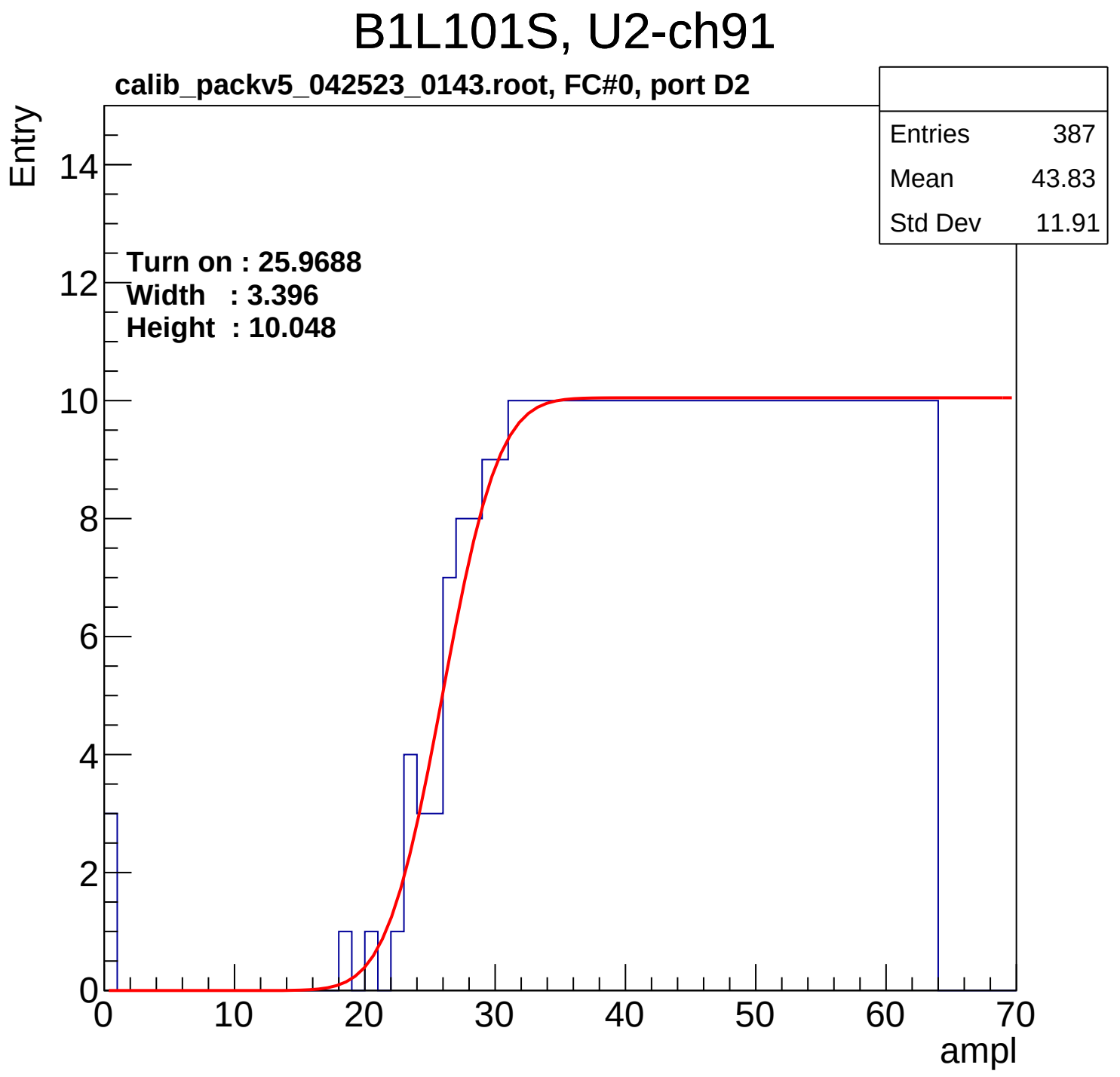
B1L101S, U2-ch91
calib_packv5_042523_0143.root, FC#0, port D2
Entries 387
Mean 43.83
Std Dev 11.91
Turn on : 25.9688
Width : 3.396
Height : 10.048
Entry
ampl
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4
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8
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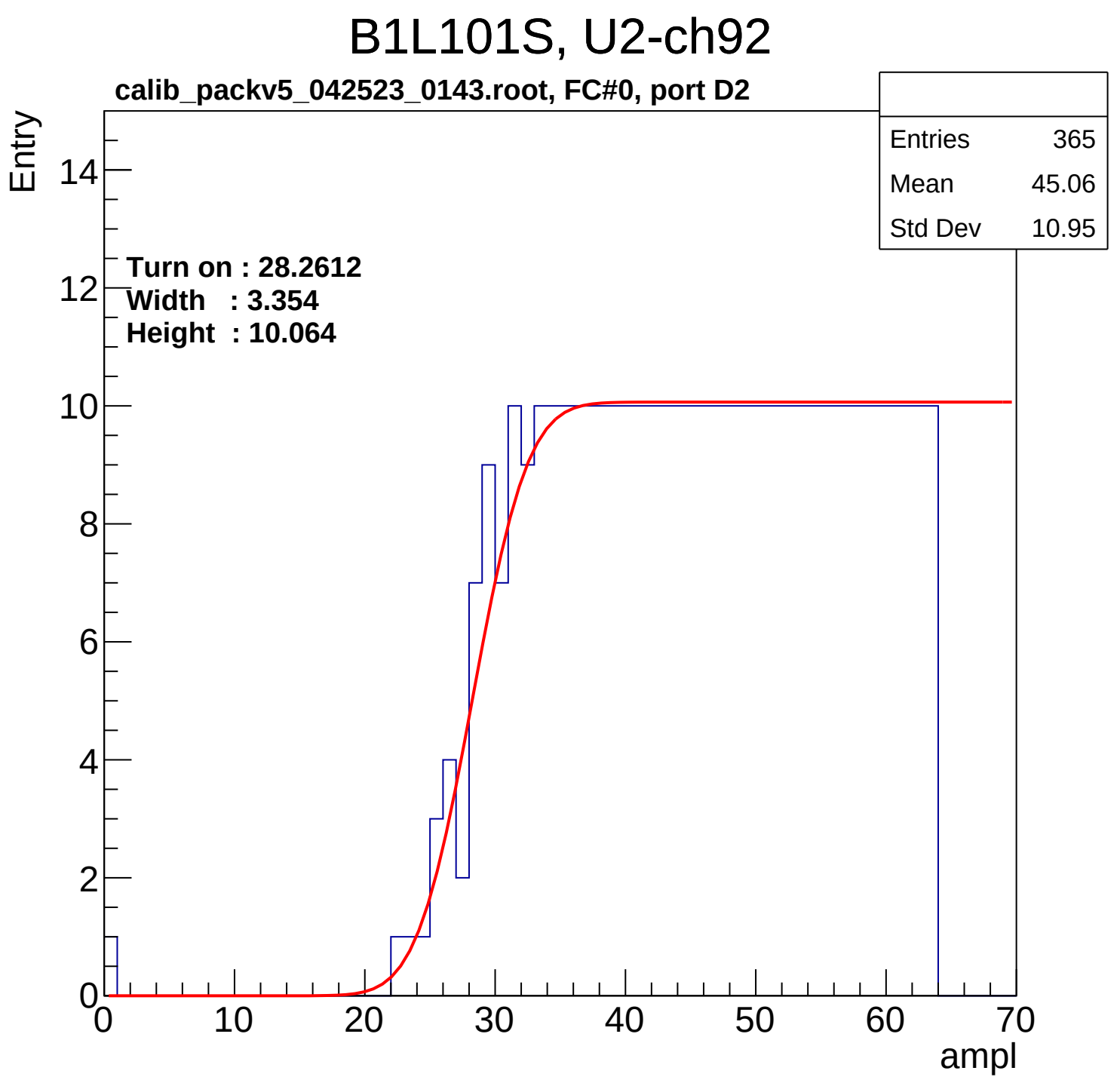
B1L101S, U2-ch92
calib_packv5_042523_0143.root, FC#0, port D2
Entries 365
Mean 45.06
Std Dev 10.95
Turn on : 28.2612
Width : 3.354
Height : 10.064
Entry
ampl
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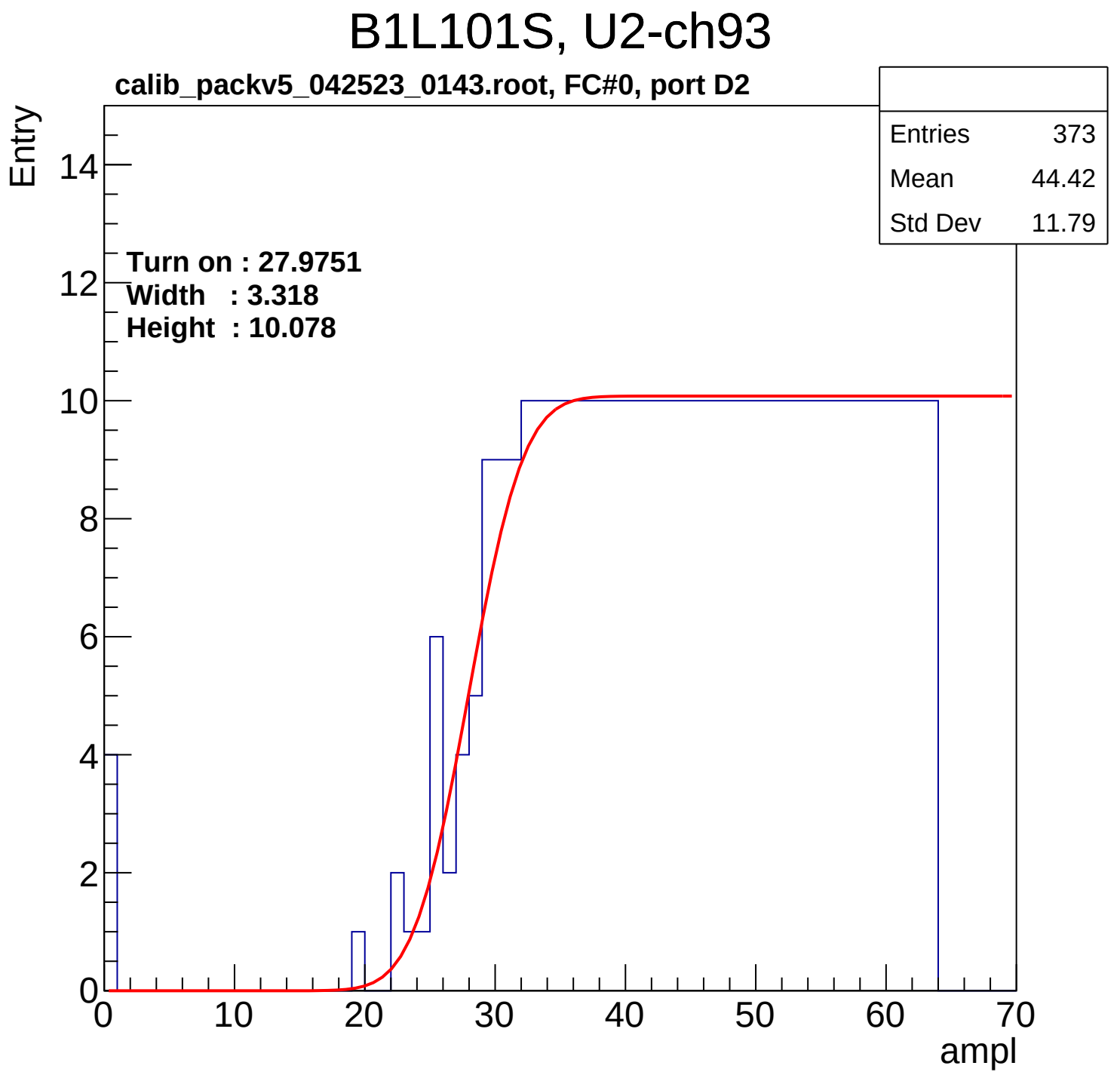
B1L101S, U2-ch93
calib_packv5_042523_0143.root, FC#0, port D2
Entries 373
Mean 44.42
Std Dev 11.79
Turn on : 27.9751
Width : 3.318
Height : 10.078
Entry
ampl
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8
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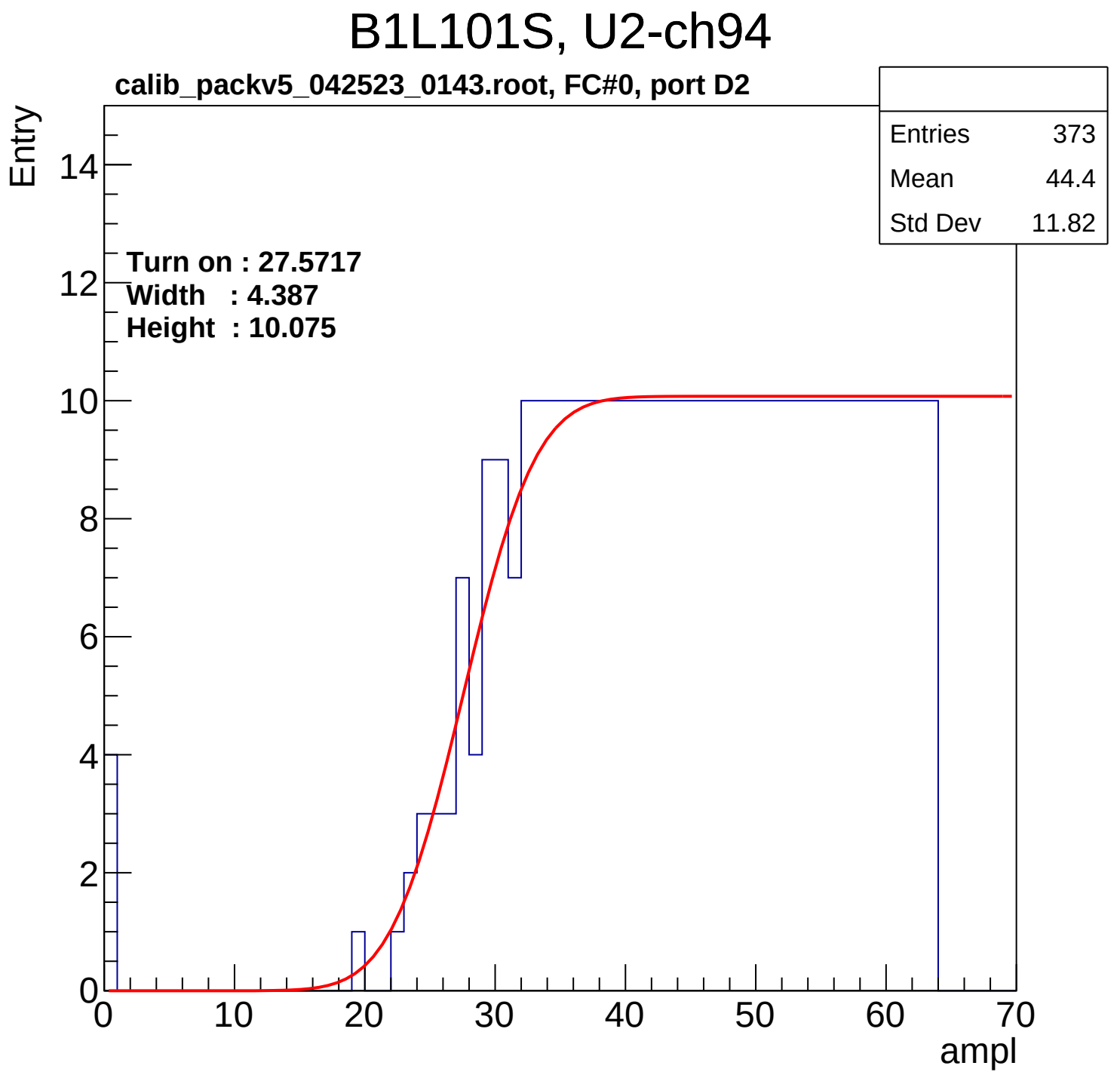
B1L101S, U2-ch94
calib_packv5_042523_0143.root, FC#0, port D2
Entries 373
Mean 44.4
Std Dev 11.82
Turn on : 27.5717
Width : 4.387
Height : 10.075
Entry
ampl
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8
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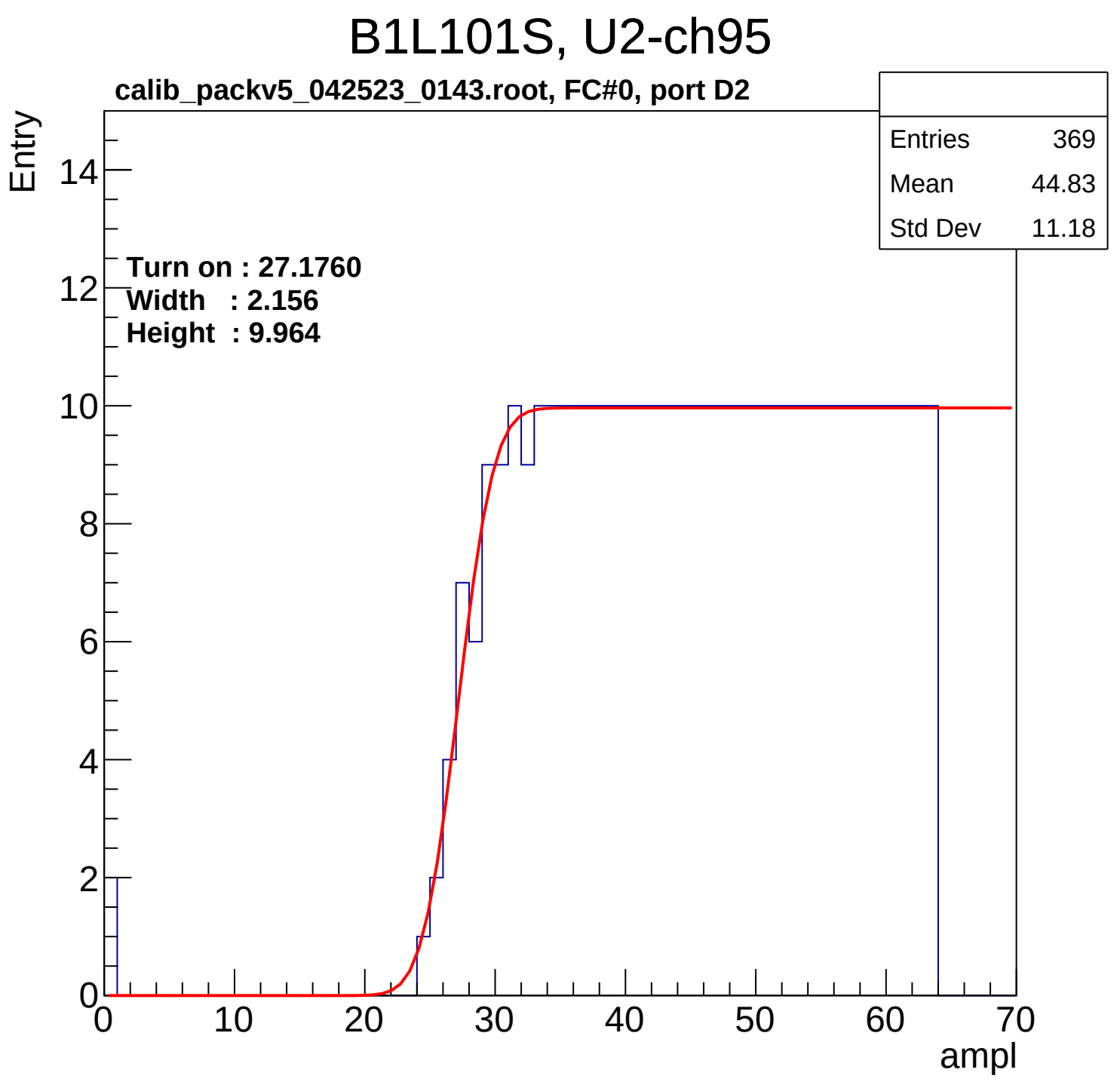
B1L101S, U2-ch95
calib_packv5_042523_0143.root, FC#0, port D2
Entries 369
Mean 44.83
Std Dev 11.18
Turn on : 27.1760
Width : 2.156
Height : 9.964
Entry
ampl
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6
8
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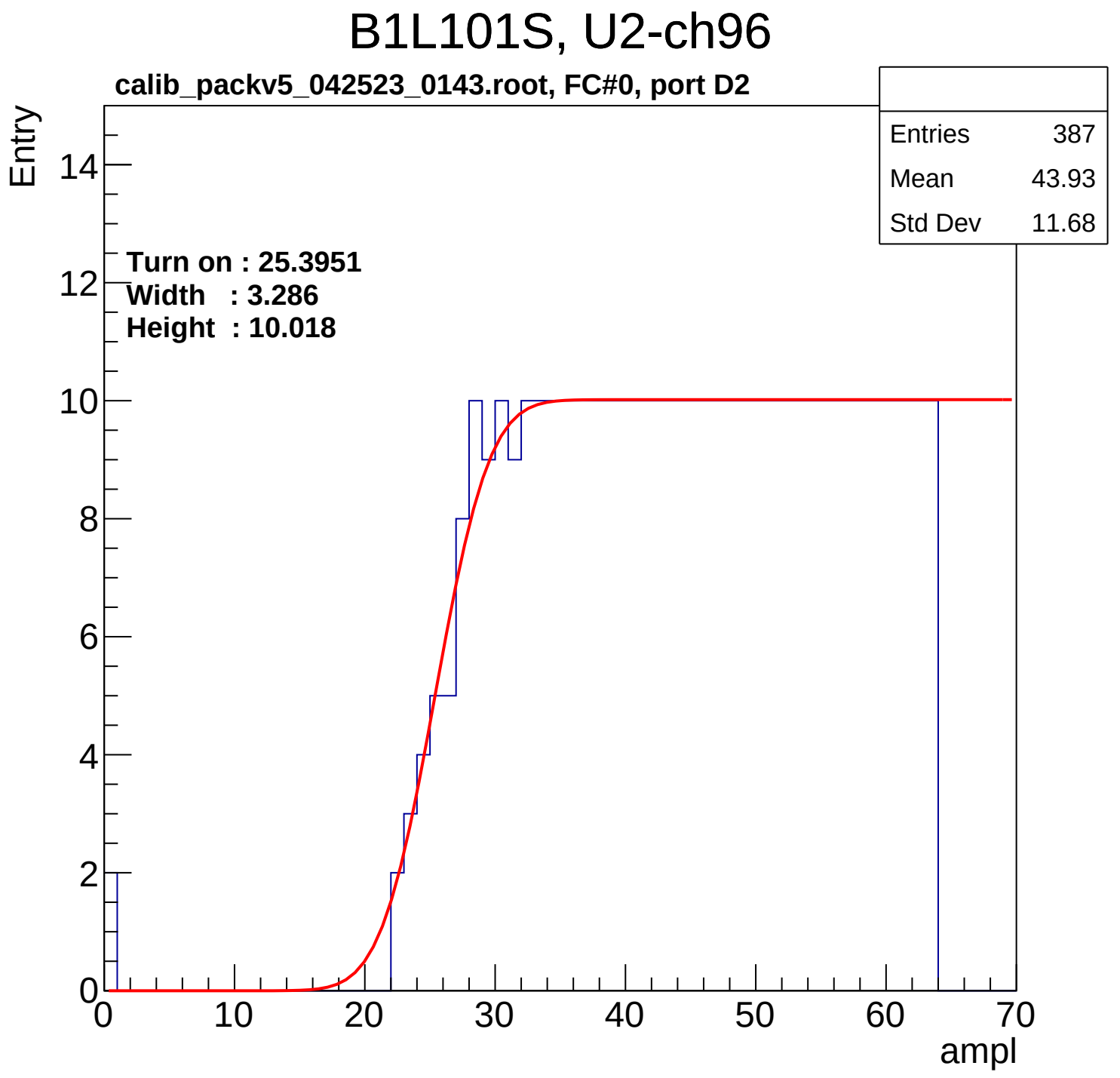
B1L101S, U2-ch96
calib_packv5_042523_0143.root, FC#0, port D2
Entries 387
Mean 43.93
Std Dev 11.68
Turn on : 25.3951
Width : 3.286
Height : 10.018
Entry
ampl
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6
8
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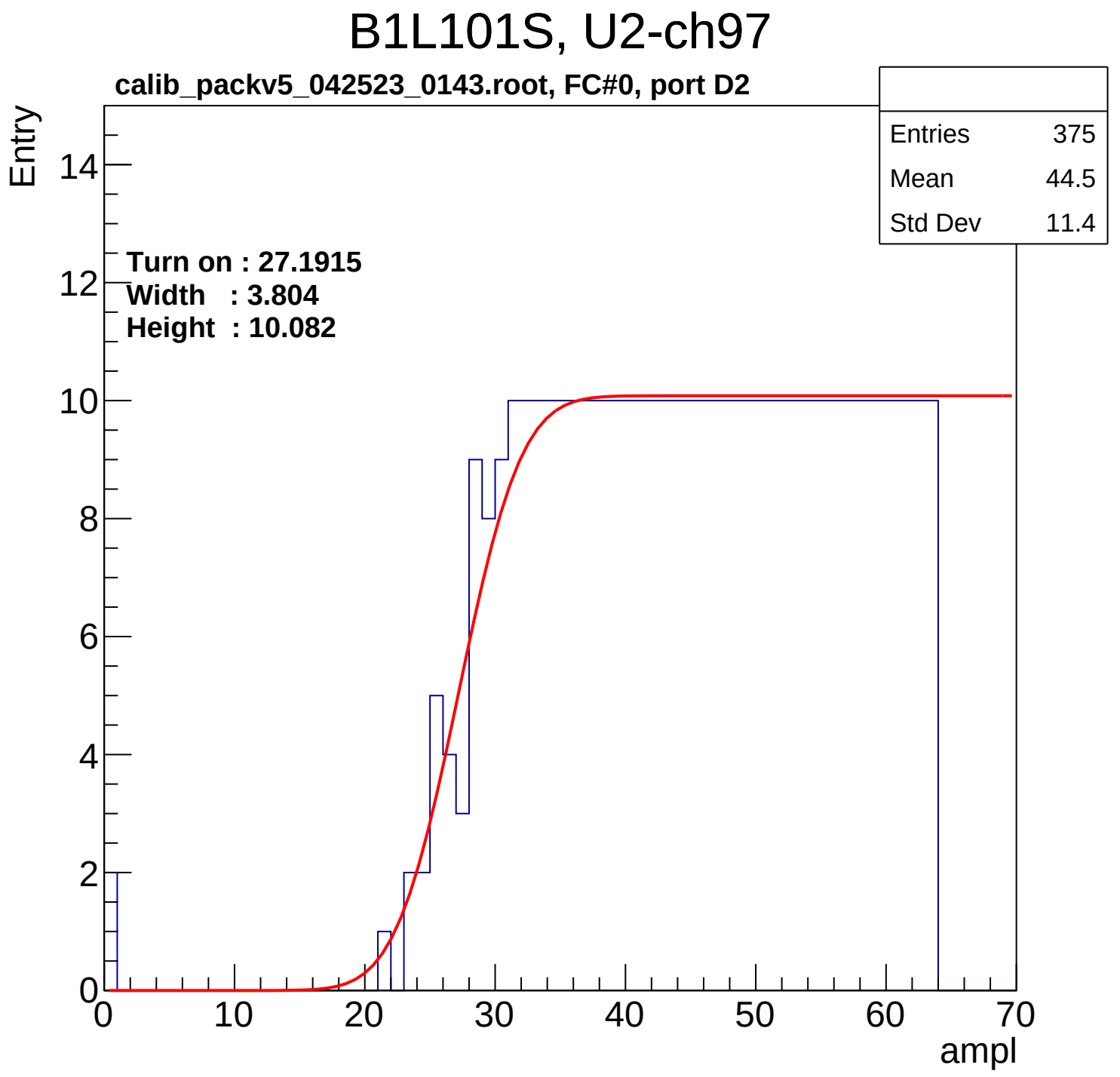
B1L101S, U2-ch97
calib_packv5_042523_0143.root, FC#0, port D2
Entries 375
Mean 44.5
Std Dev 11.4
Turn on : 27.1915
Width : 3.804
Height : 10.082
Entry
ampl
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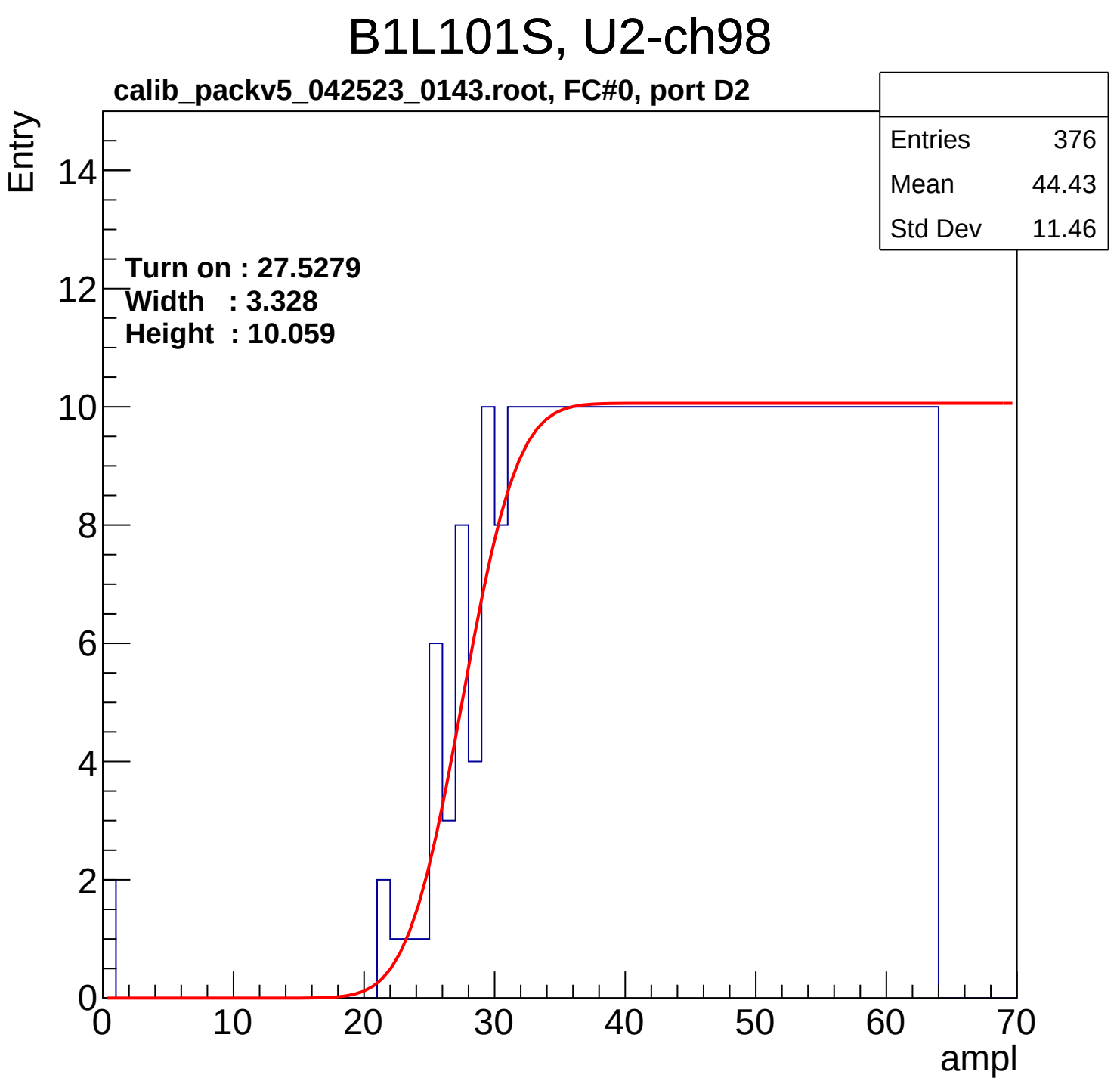
B1L101S, U2-ch98
calib_packv5_042523_0143.root, FC#0, port D2
Entries 376
Mean 44.43
Std Dev 11.46
Turn on : 27.5279
Width : 3.328
Height : 10.059
Entry
ampl
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8
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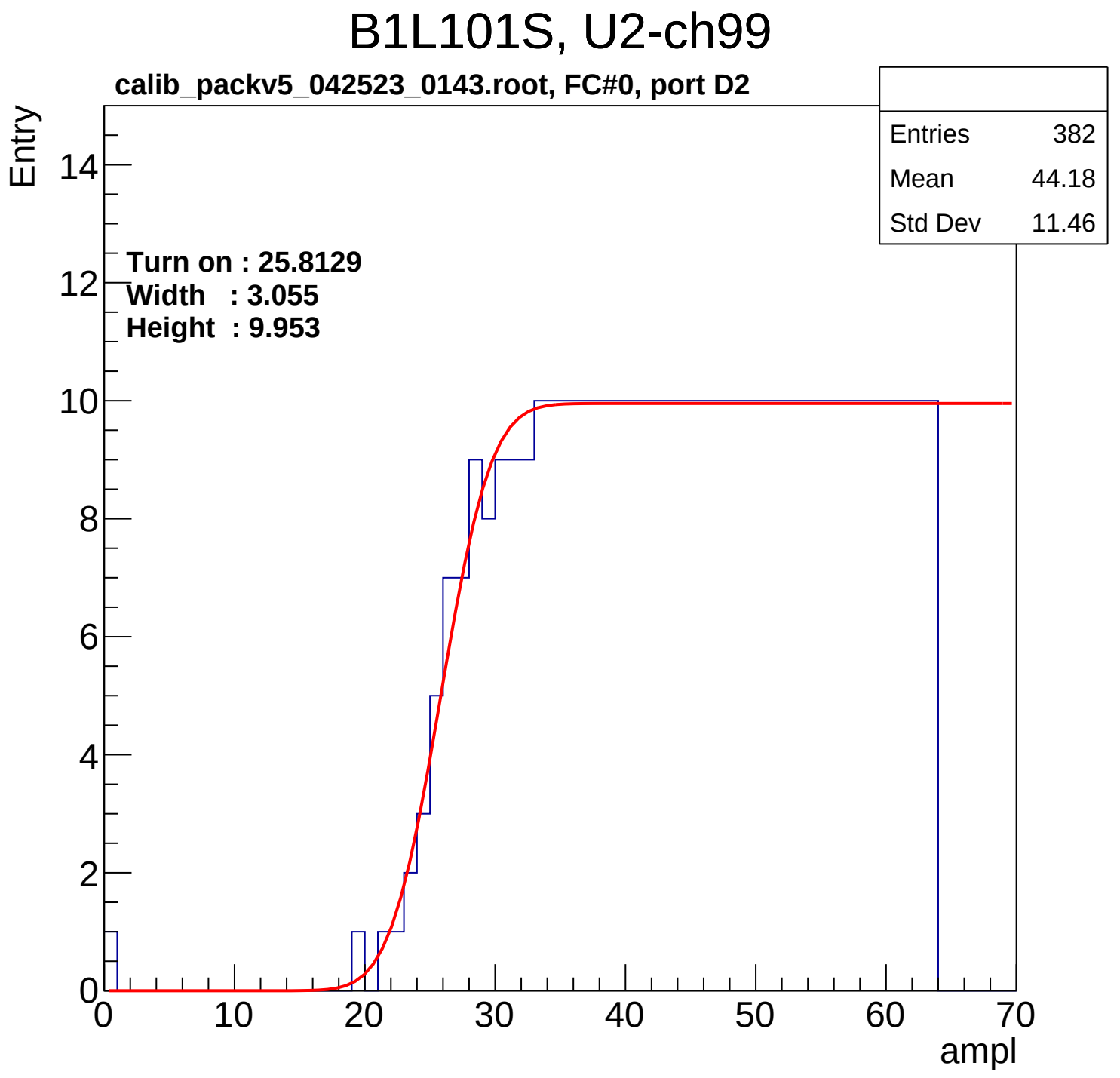
B1L101S, U2-ch99
calib_packv5_042523_0143.root, FC#0, port D2
Entries 382
Mean 44.18
Std Dev 11.46
Turn on : 25.8129
Width : 3.055
Height : 9.953
Entry
ampl
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4
6
8
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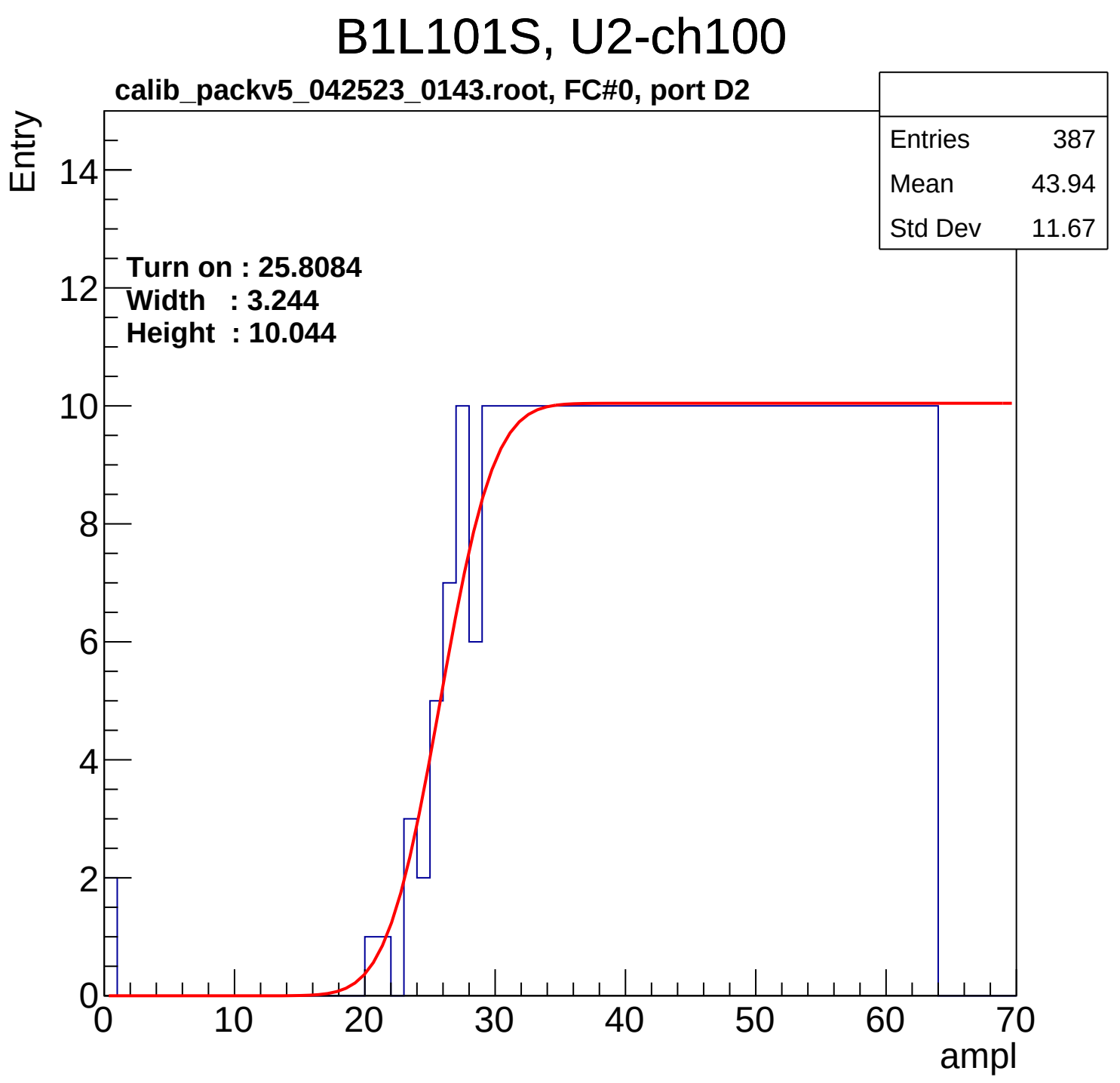
B1L101S, U2-ch100
calib_packv5_042523_0143.root, FC#0, port D2
Entries 387
Mean 43.94
Std Dev 11.67
Turn on : 25.8084
Width : 3.244
Height : 10.044
Entry
ampl
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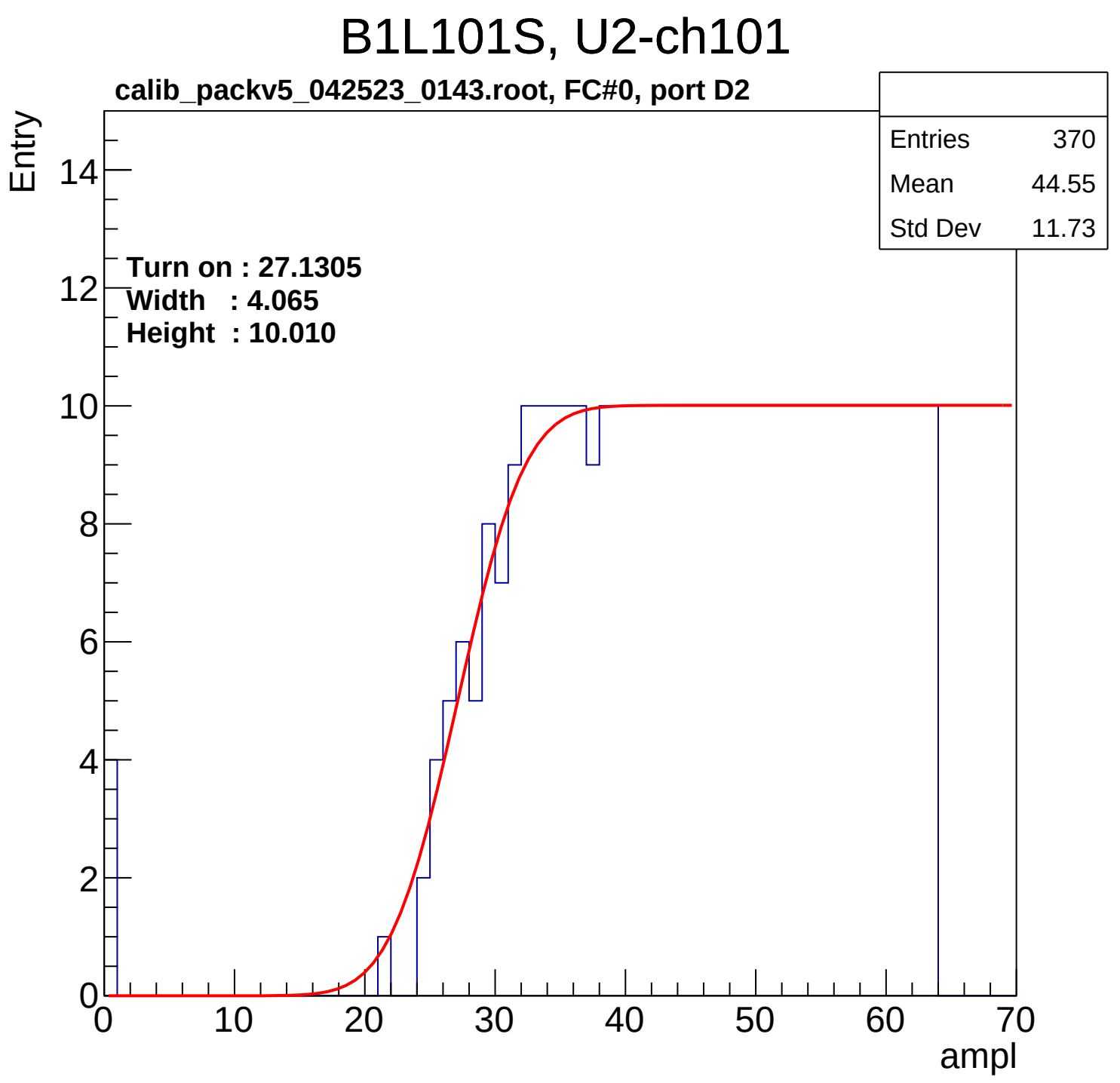
B1L101S, U2-ch101
calib_packv5_042523_0143.root, FC#0, port D2
Entries 370
Mean 44.55
Std Dev 11.73
Turn on : 27.1305
Width : 4.065
Height : 10.010
Entry
ampl
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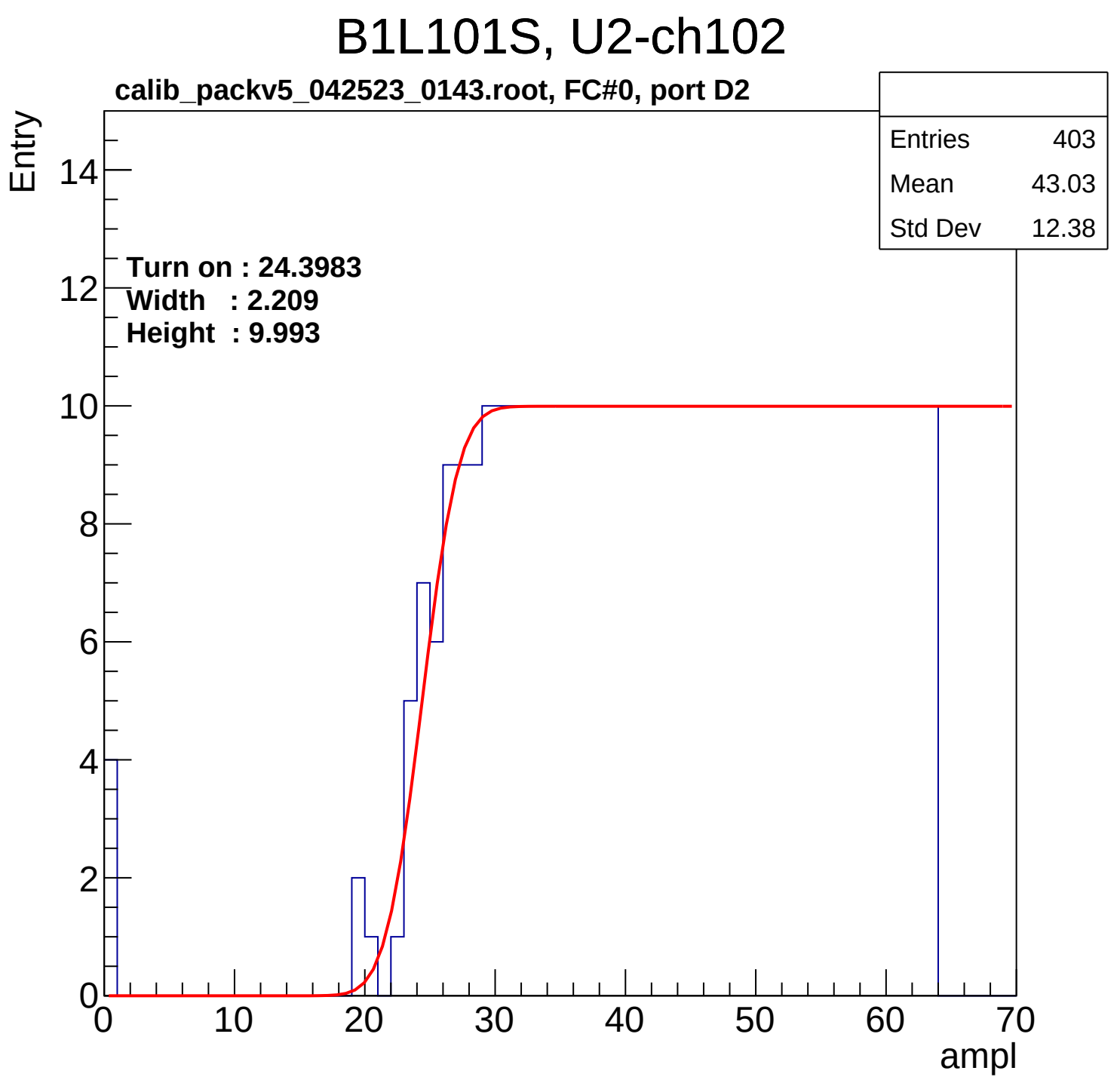
B1L101S, U2-ch102
calib_packv5_042523_0143.root, FC#0, port D2
Entries 403
Mean 43.03
Std Dev 12.38
Turn on : 24.3983
Width : 2.209
Height : 9.993
Entry
ampl
0
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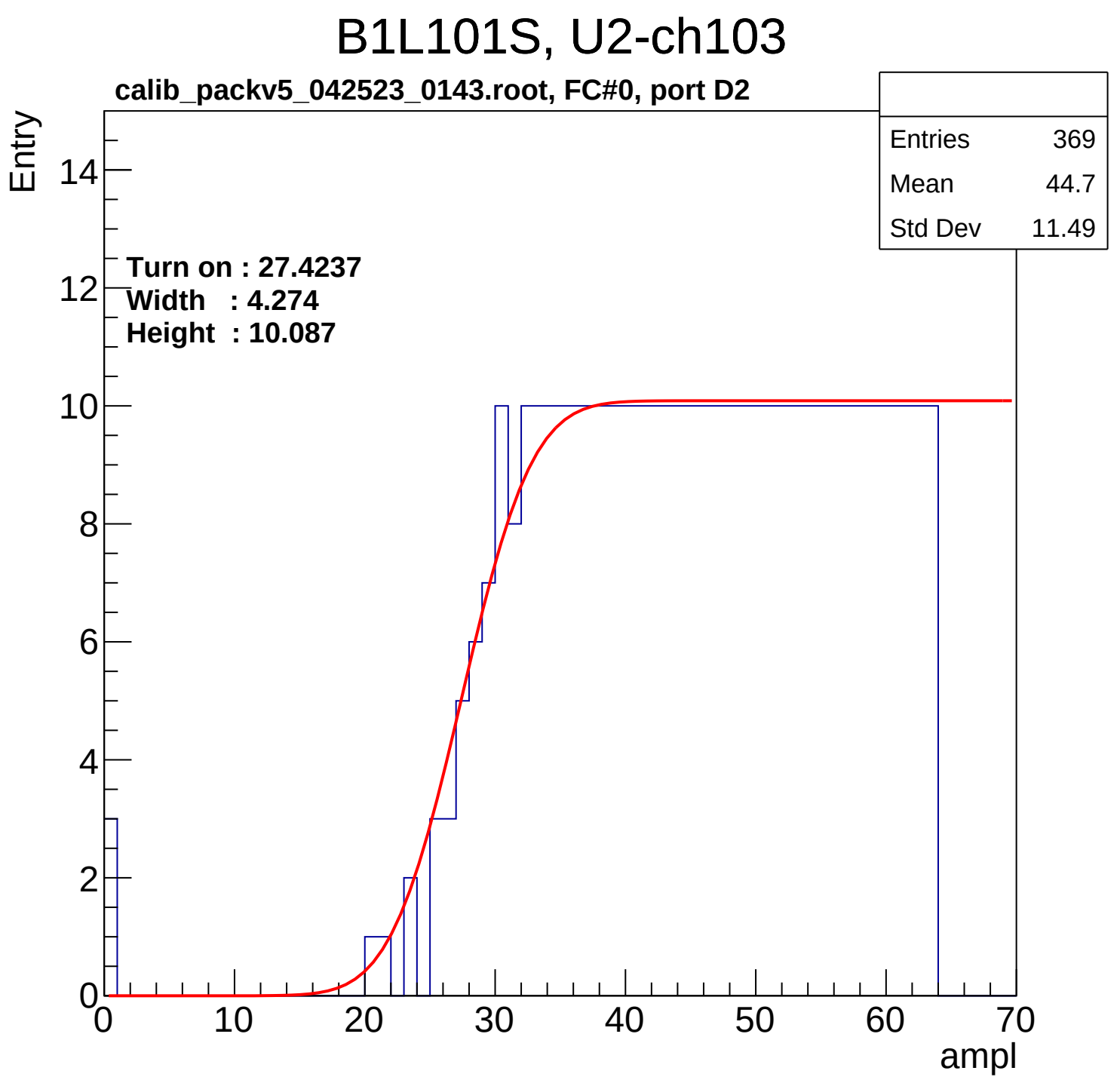
B1L101S, U2-ch103
calib_packv5_042523_0143.root, FC#0, port D2
Entries 369
Mean 44.7
Std Dev 11.49
Turn on : 27.4237
Width : 4.274
Height : 10.087
Entry
ampl
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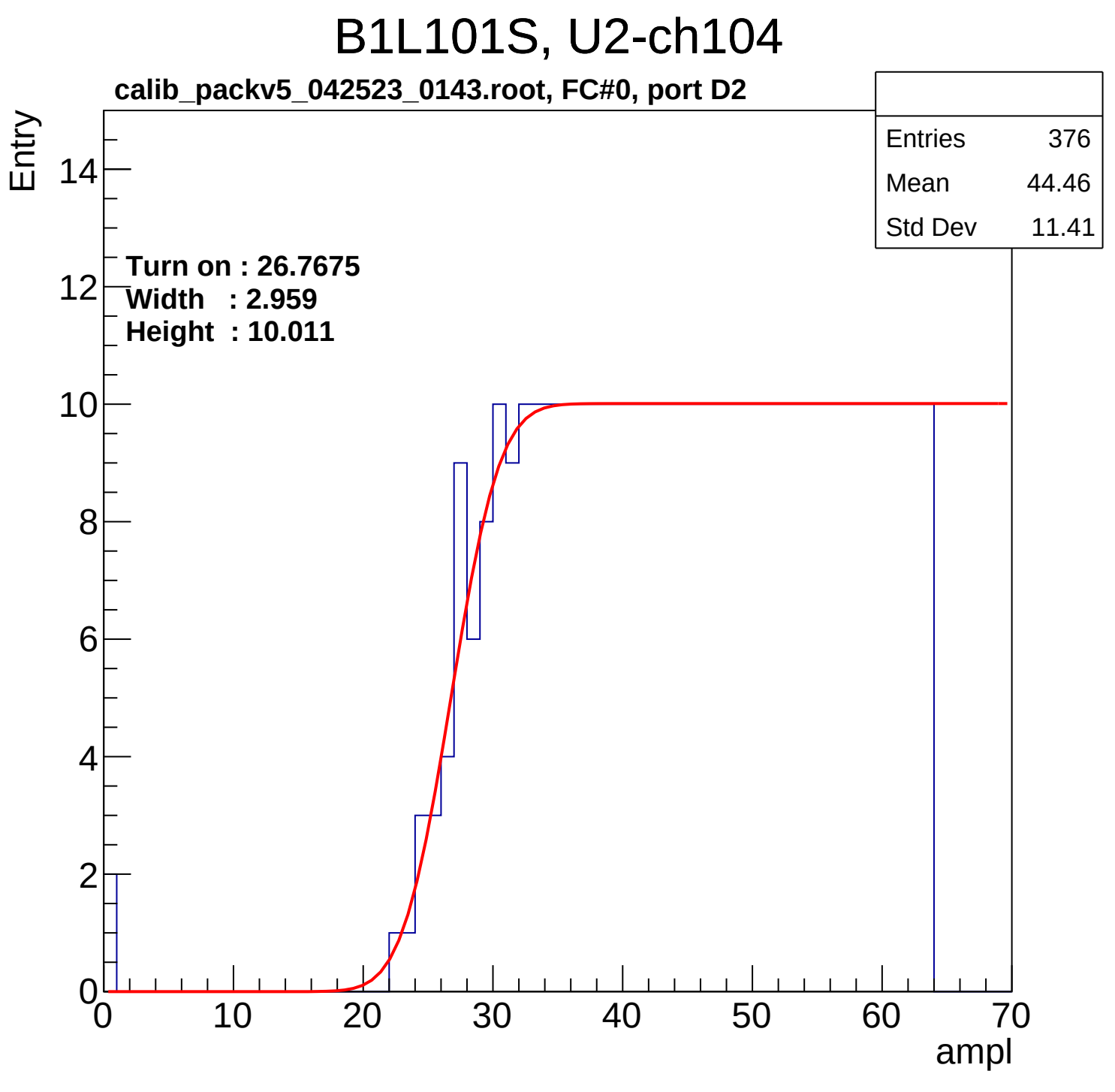
B1L101S, U2-ch104
calib_packv5_042523_0143.root, FC#0, port D2
Entries 376
Mean 44.46
Std Dev 11.41
Turn on : 26.7675
Width : 2.959
Height : 10.011
Entry
ampl
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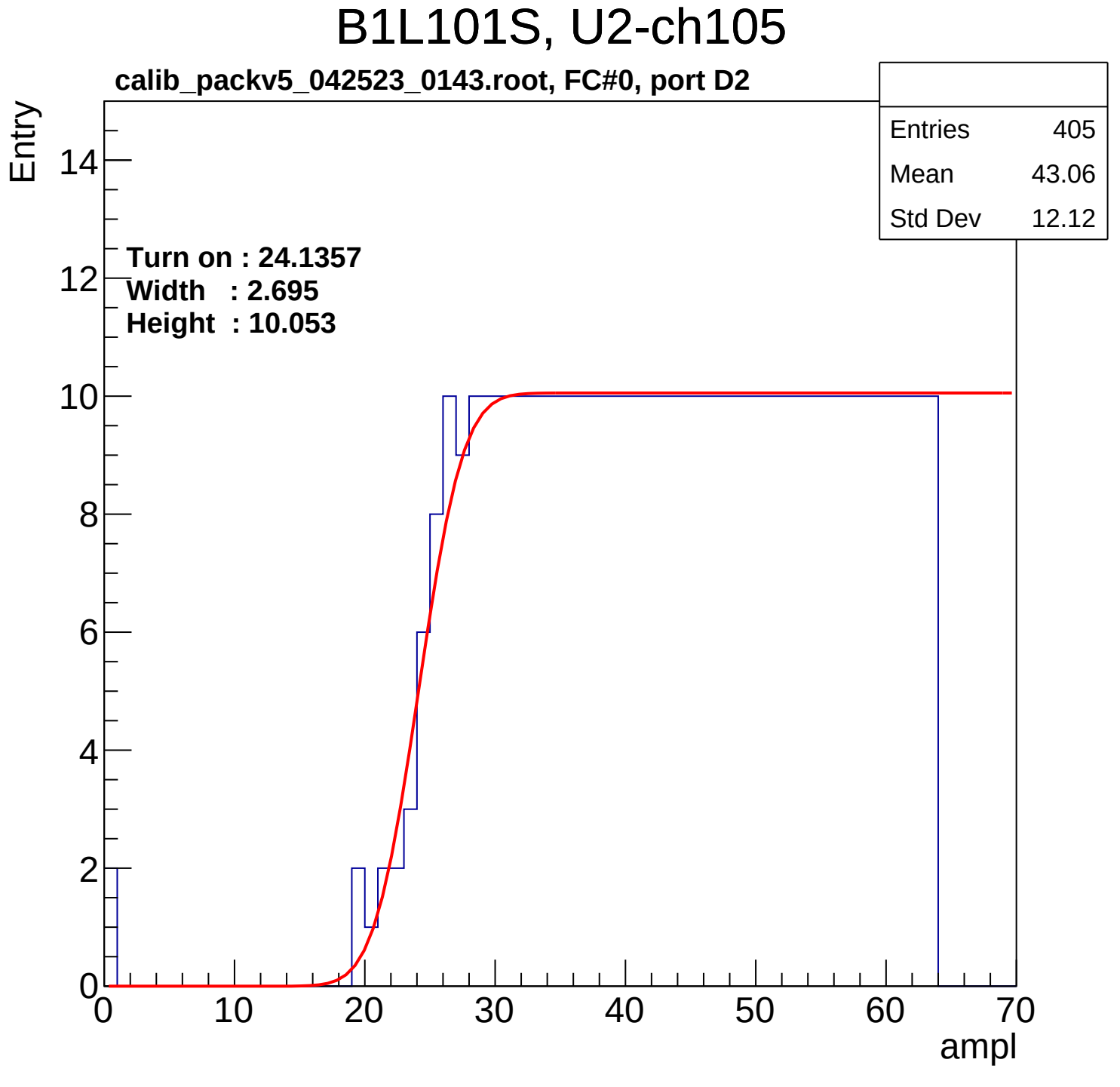
B1L101S, U2-ch105
calib_packv5_042523_0143.root, FC#0, port D2
Entries 405
Mean 43.06
Std Dev 12.12
Turn on : 24.1357
Width : 2.695
Height : 10.053
Entry
ampl
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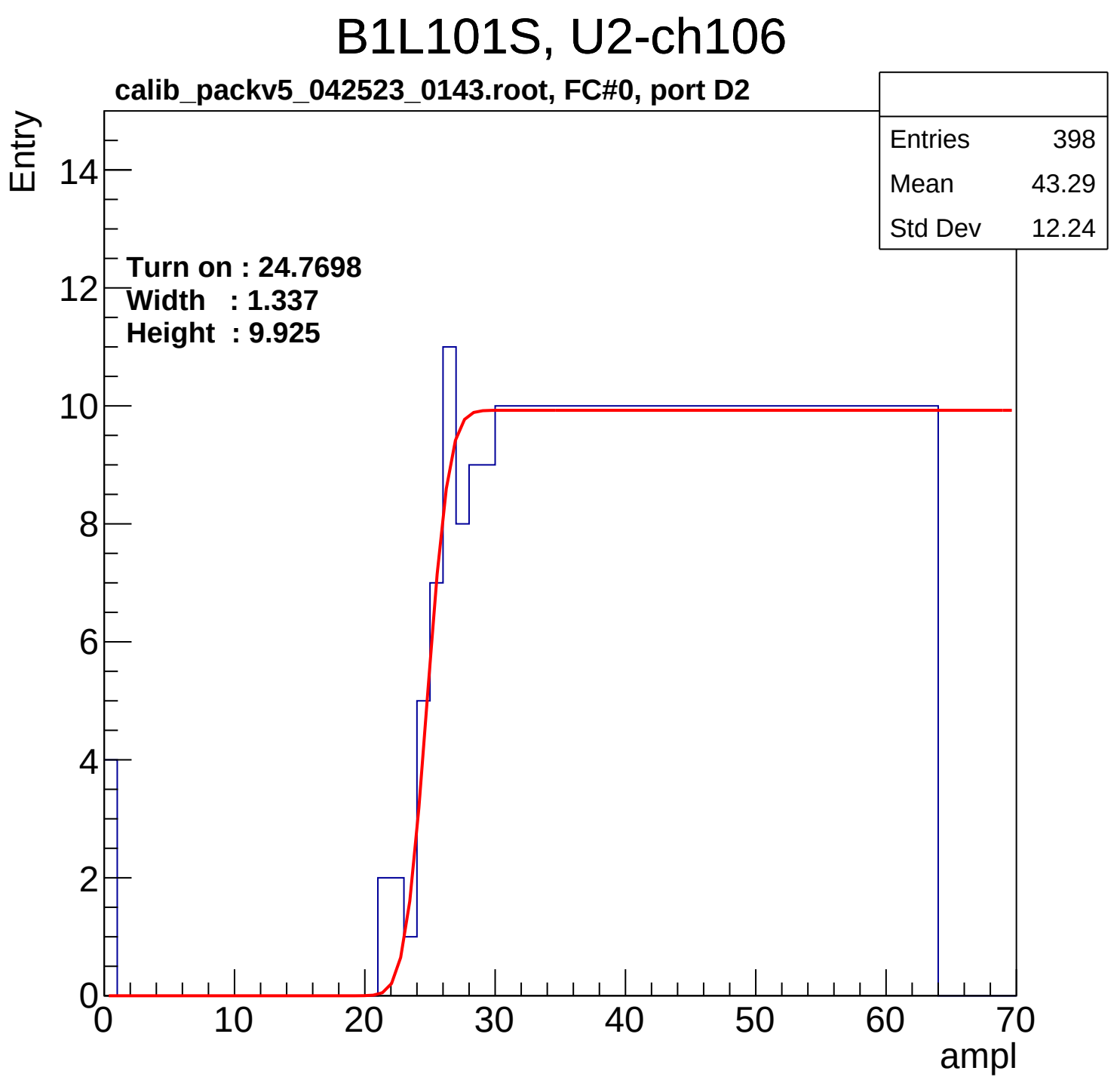
B1L101S, U2-ch106
calib_packv5_042523_0143.root, FC#0, port D2
Entries 398
Mean 43.29
Std Dev 12.24
Turn on : 24.7698
Width : 1.337
Height : 9.925
Entry
ampl
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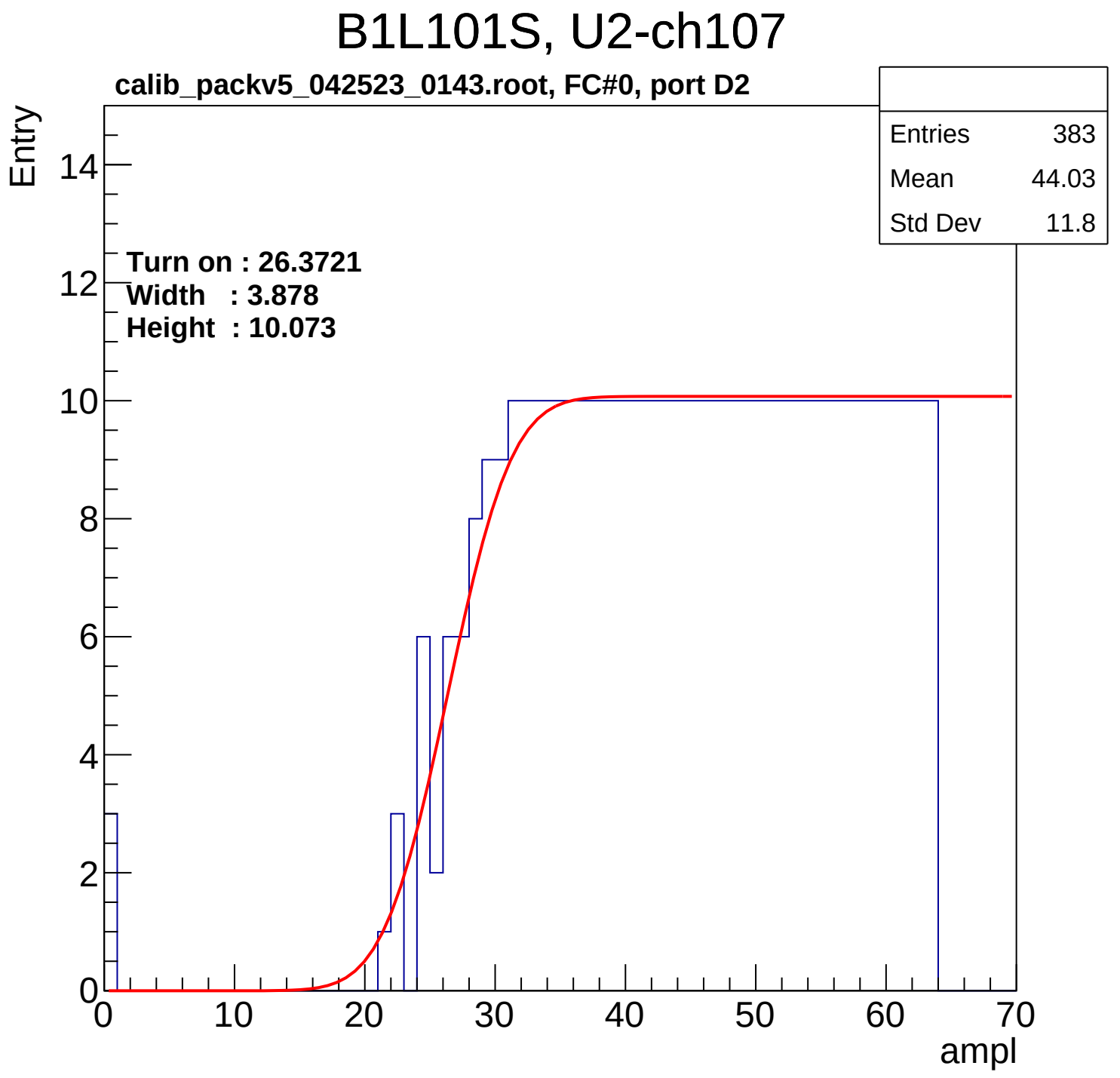
B1L101S, U2-ch107
calib_packv5_042523_0143.root, FC#0, port D2
Entries 383
Mean 44.03
Std Dev 11.8
Turn on : 26.3721
Width : 3.878
Height : 10.073
Entry
ampl
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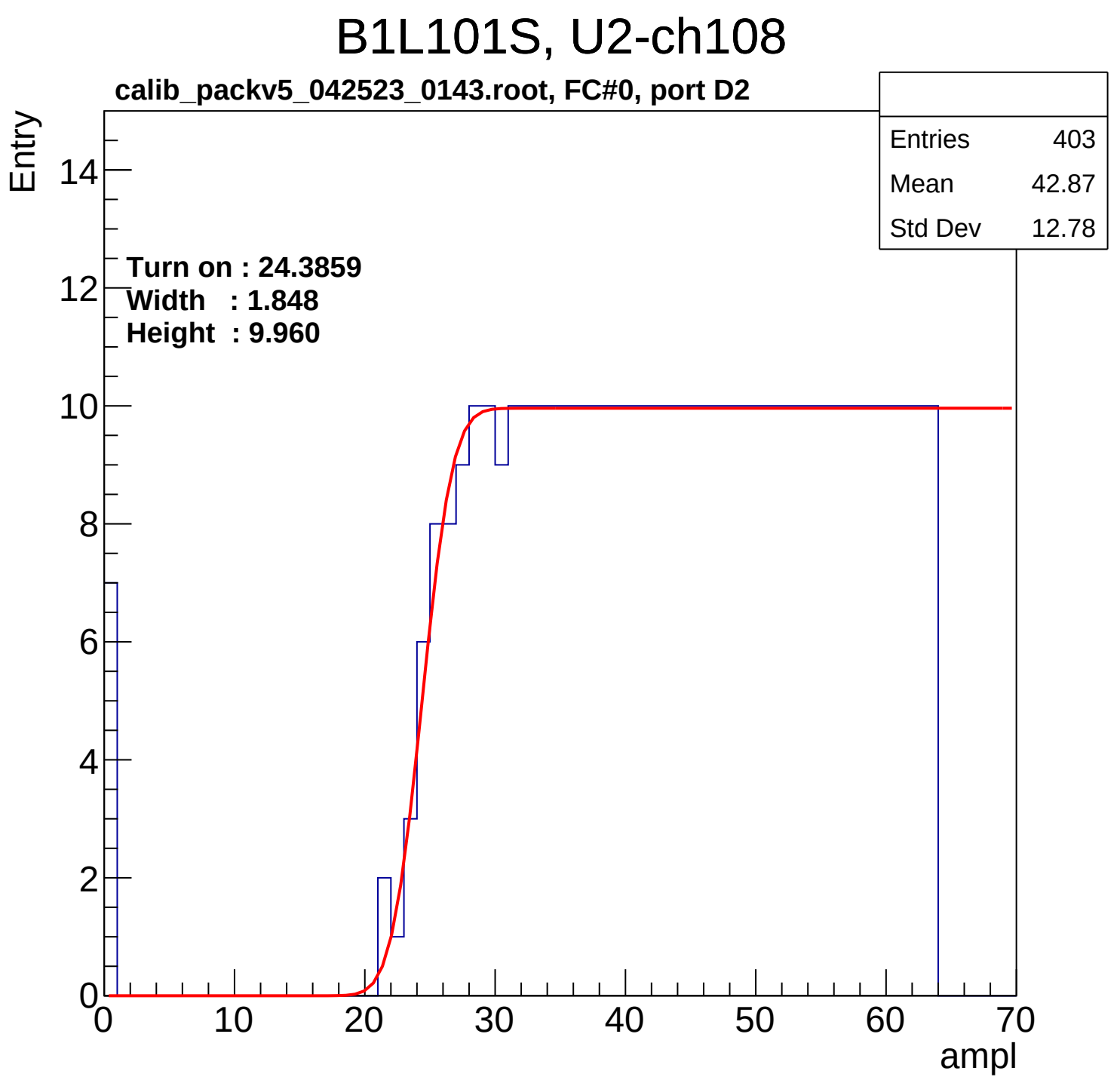
B1L101S, U2-ch108
calib_packv5_042523_0143.root, FC#0, port D2
Entries 403
Mean 42.87
Std Dev 12.78
Turn on : 24.3859
Width : 1.848
Height : 9.960
Entry
ampl
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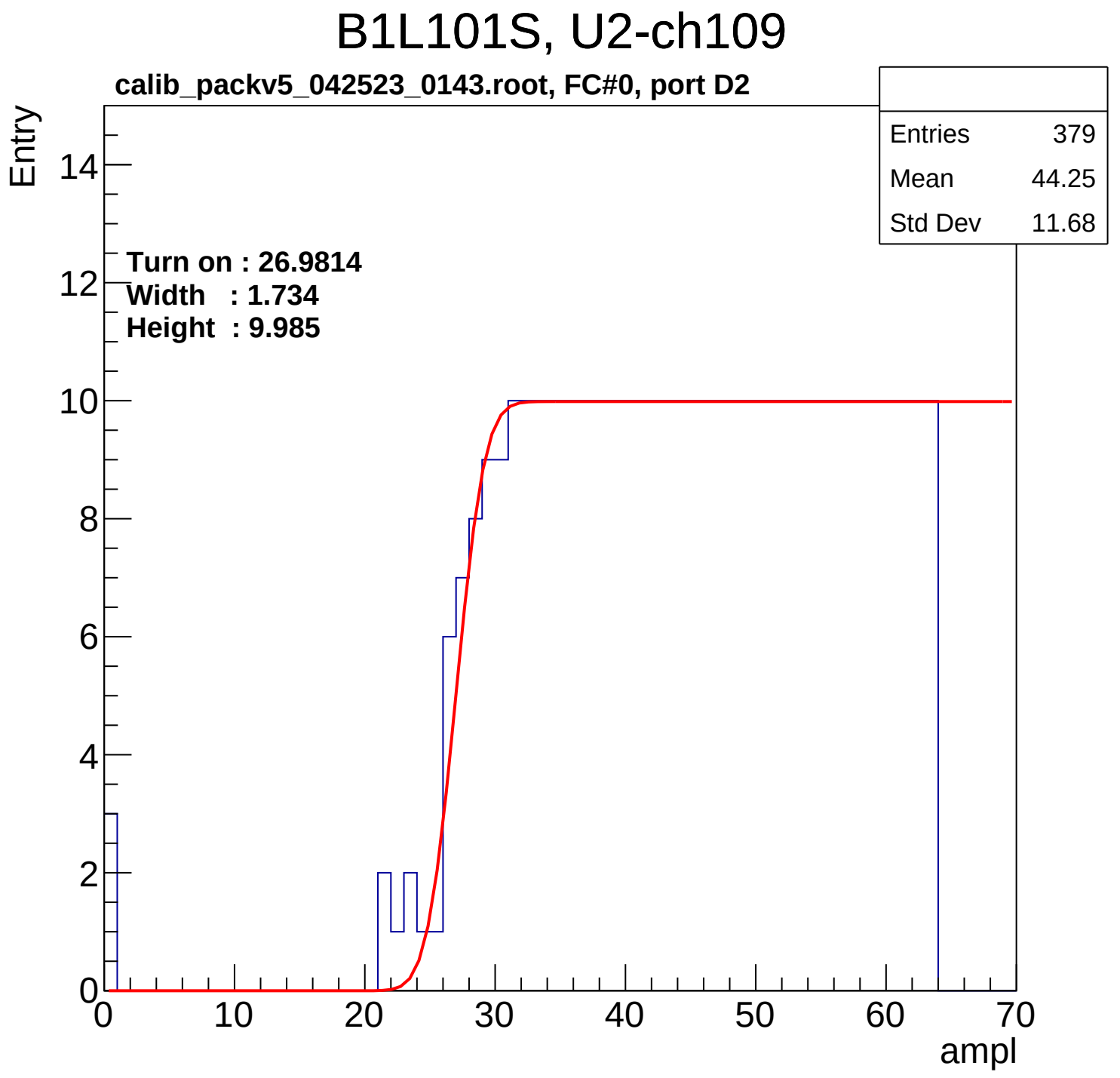
B1L101S, U2-ch109
calib_packv5_042523_0143.root, FC#0, port D2
Entries 379
Mean 44.25
Std Dev 11.68
Turn on : 26.9814
Width : 1.734
Height : 9.985
Entry
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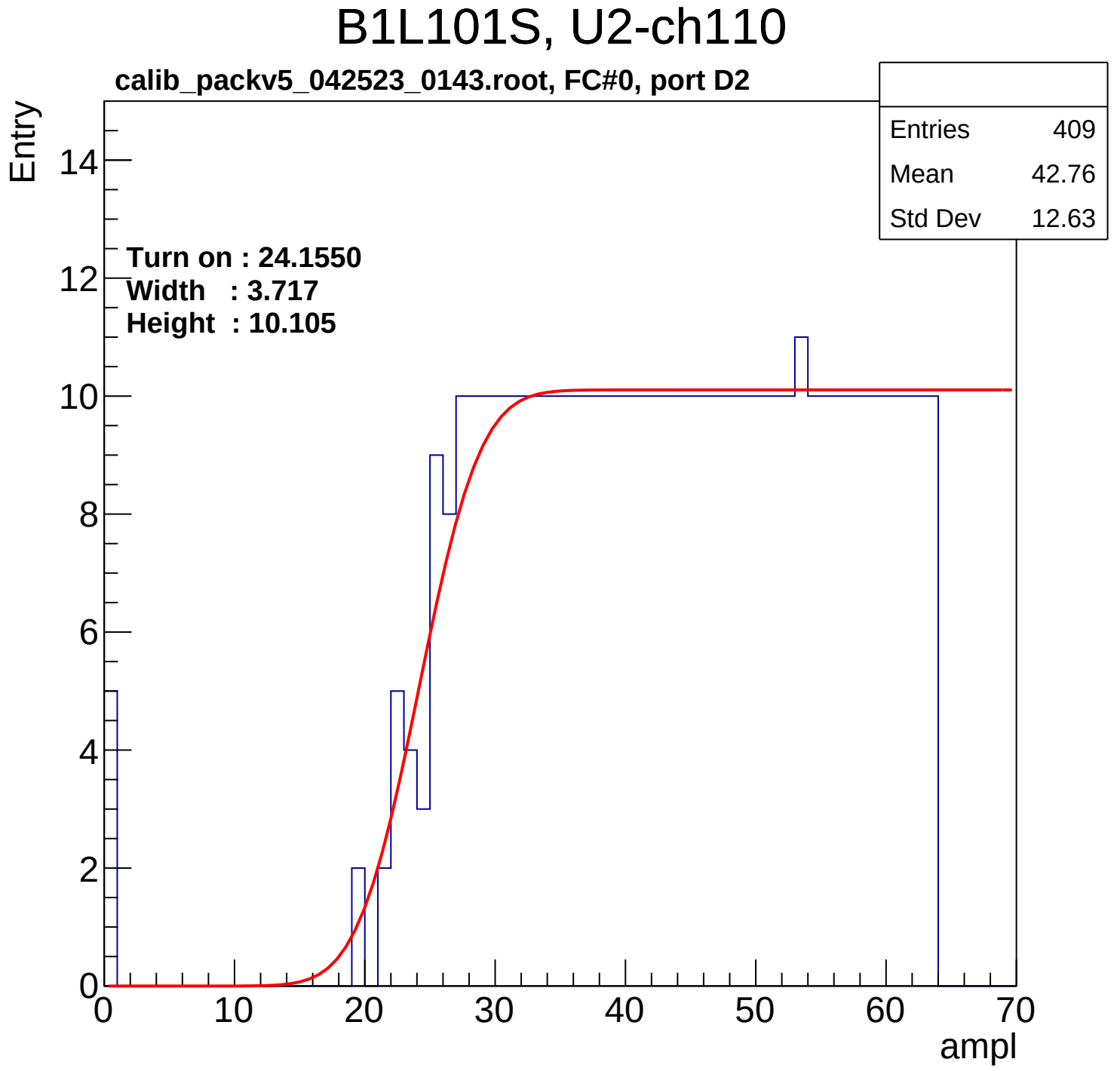
B1L101S, U2-ch110
calib_packv5_042523_0143.root, FC#0, port D2
Entries 409
Mean 42.76
Std Dev 12.63
Turn on : 24.1550
Width : 3.717
Height : 10.105
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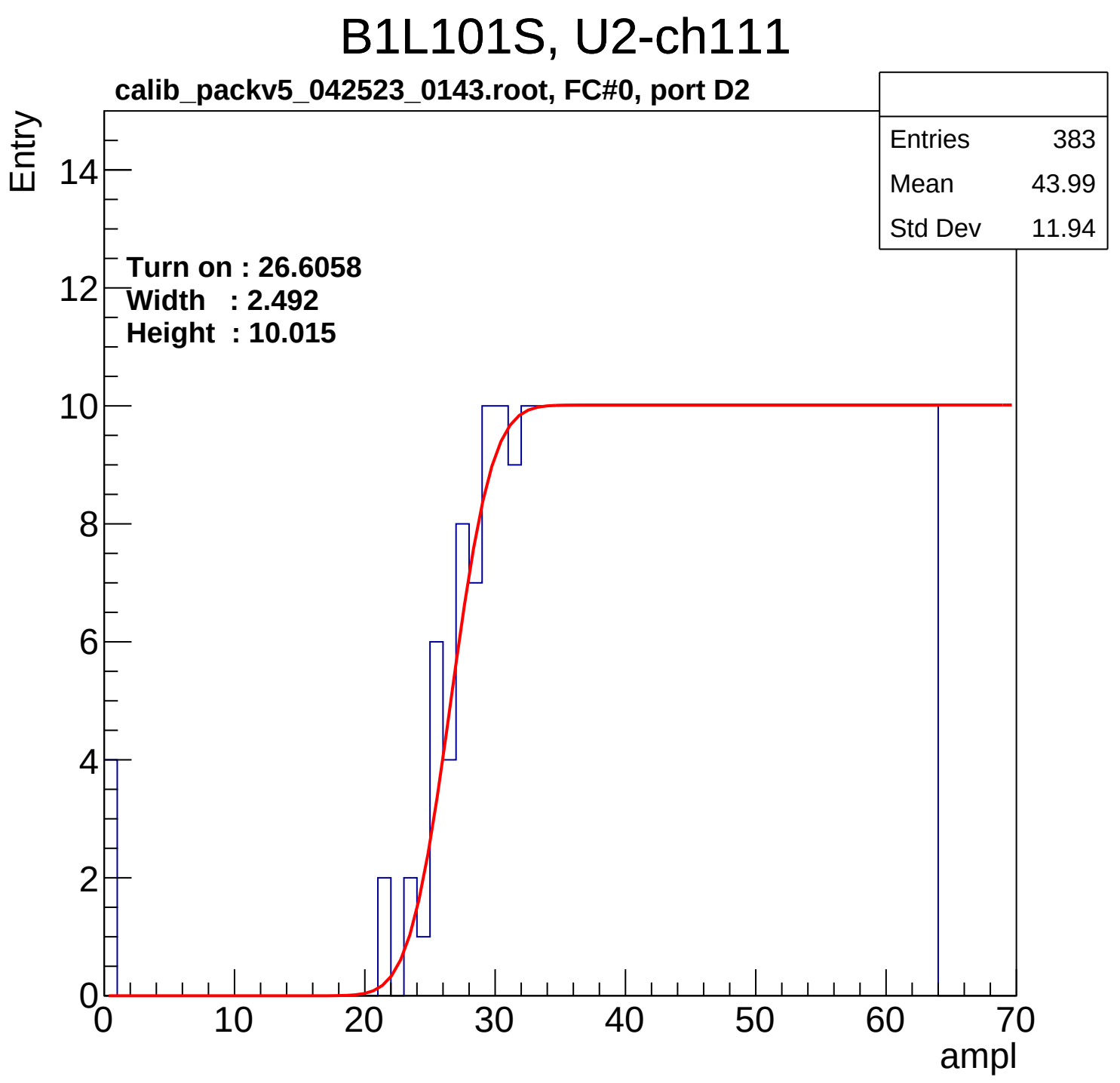
B1L101S, U2-ch111
calib_packv5_042523_0143.root, FC#0, port D2
Entries 383
Mean 43.99
Std Dev 11.94
Turn on : 26.6058
Width : 2.492
Height : 10.015
Entry
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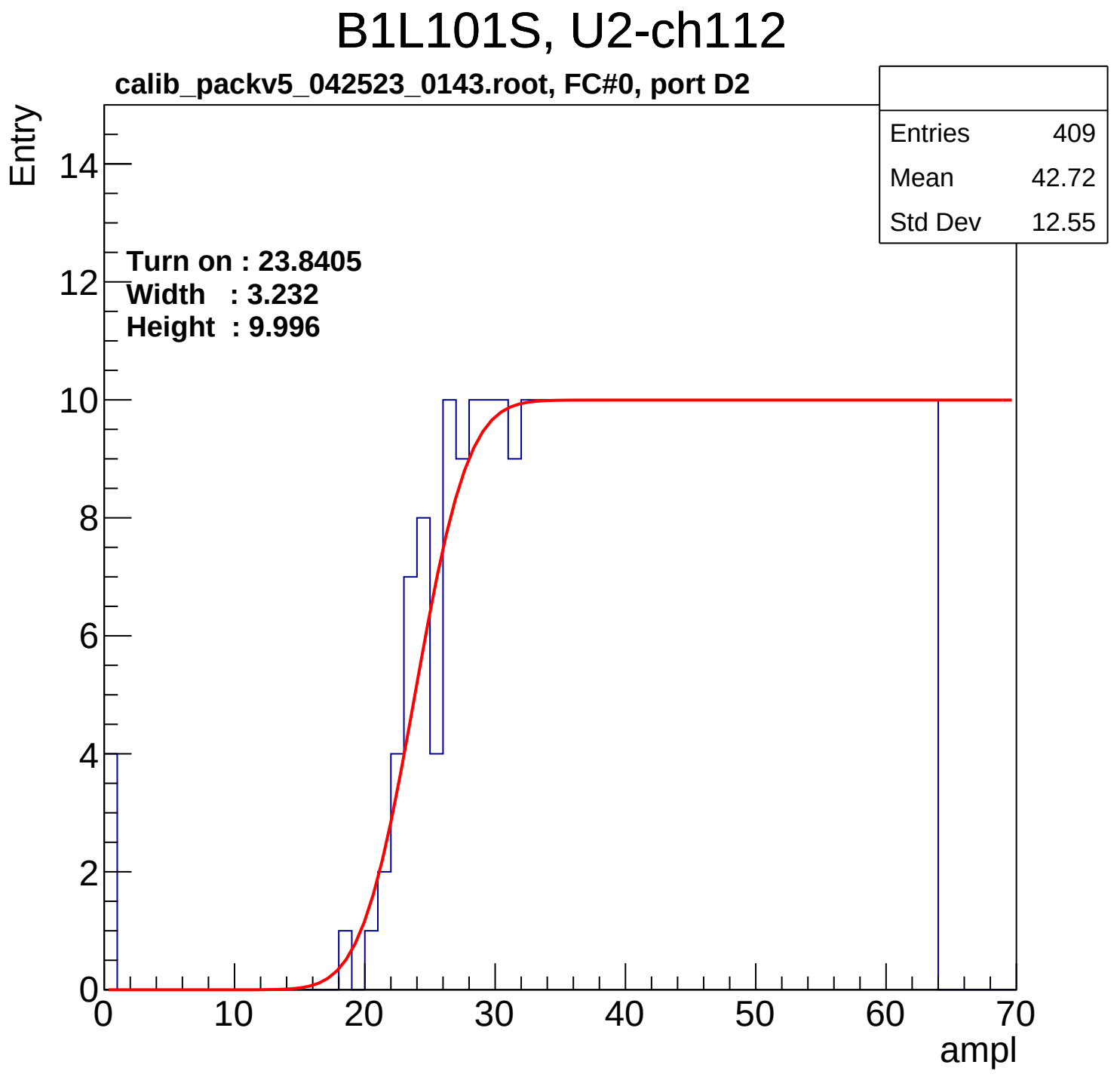
B1L101S, U2-ch112
calib_packv5_042523_0143.root, FC#0, port D2
Entries 409
Mean 42.72
Std Dev 12.55
Turn on : 23.8405
Width : 3.232
Height : 9.996
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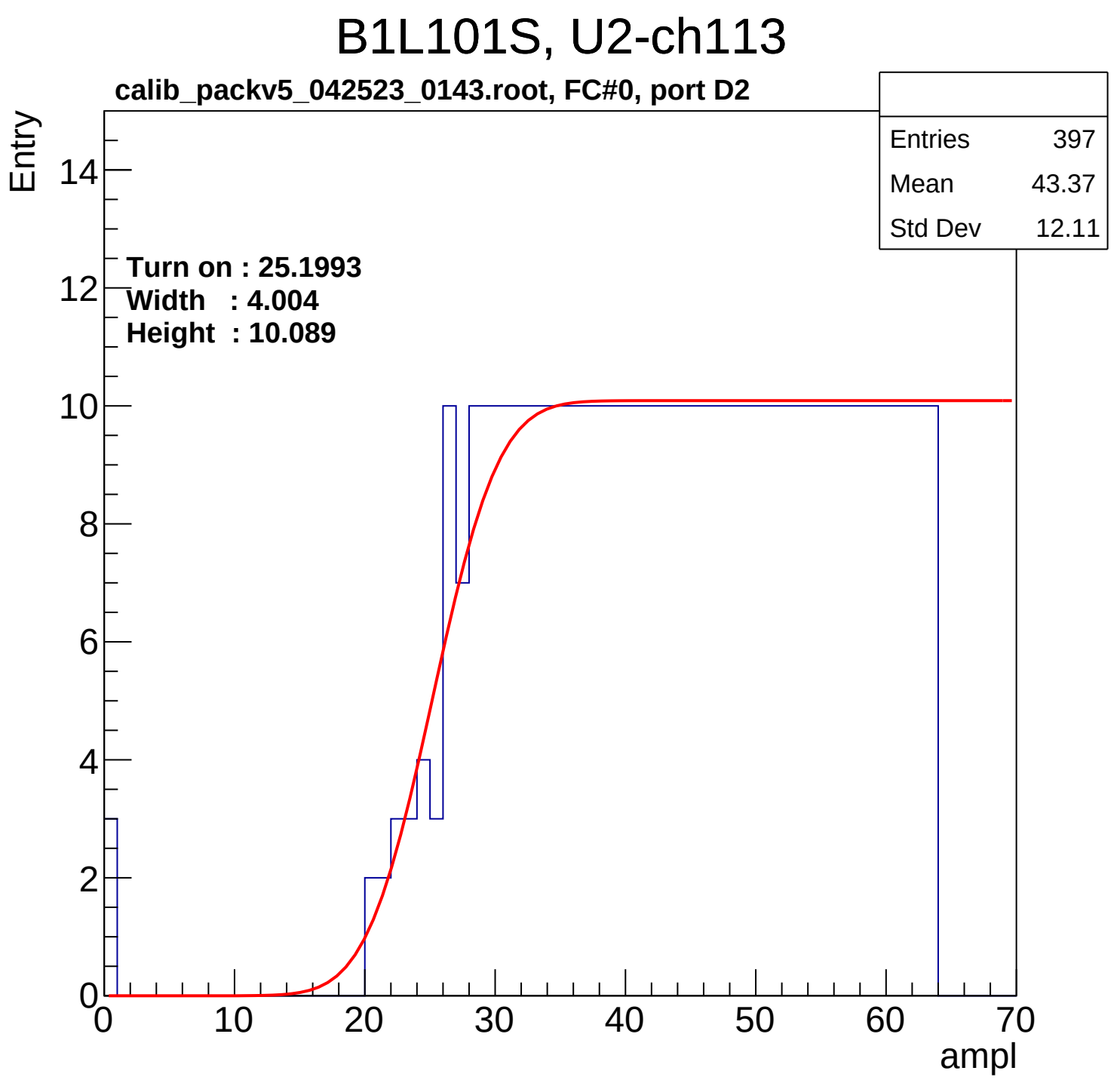
B1L101S, U2-ch113
calib_packv5_042523_0143.root, FC#0, port D2
Entries 397
Mean 43.37
Std Dev 12.11
Turn on : 25.1993
Width : 4.004
Height : 10.089
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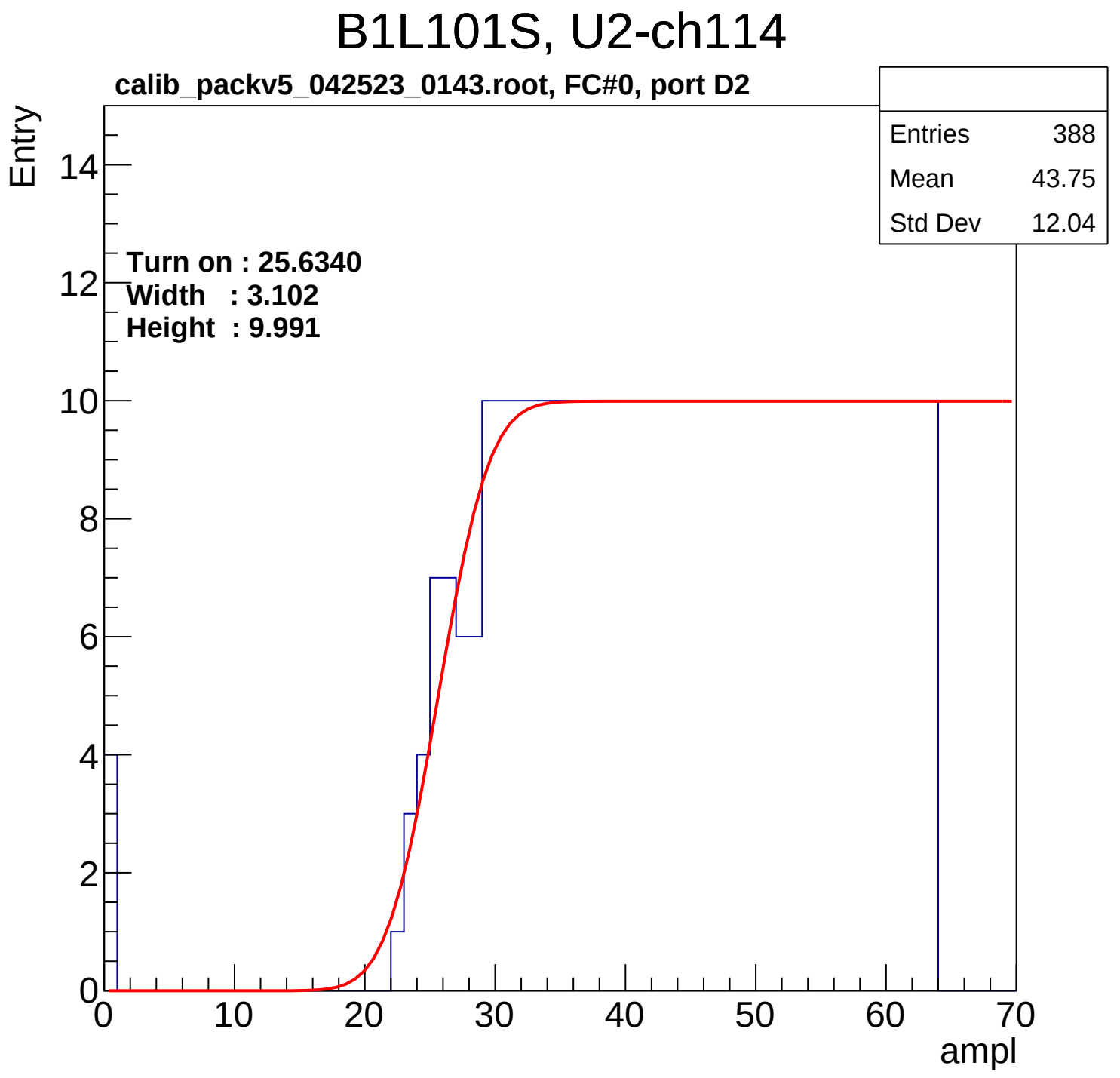
B1L101S, U2-ch114
calib_packv5_042523_0143.root, FC#0, port D2
Entries 388
Mean 43.75
Std Dev 12.04
Turn on : 25.6340
Width : 3.102
Height : 9.991
Entry
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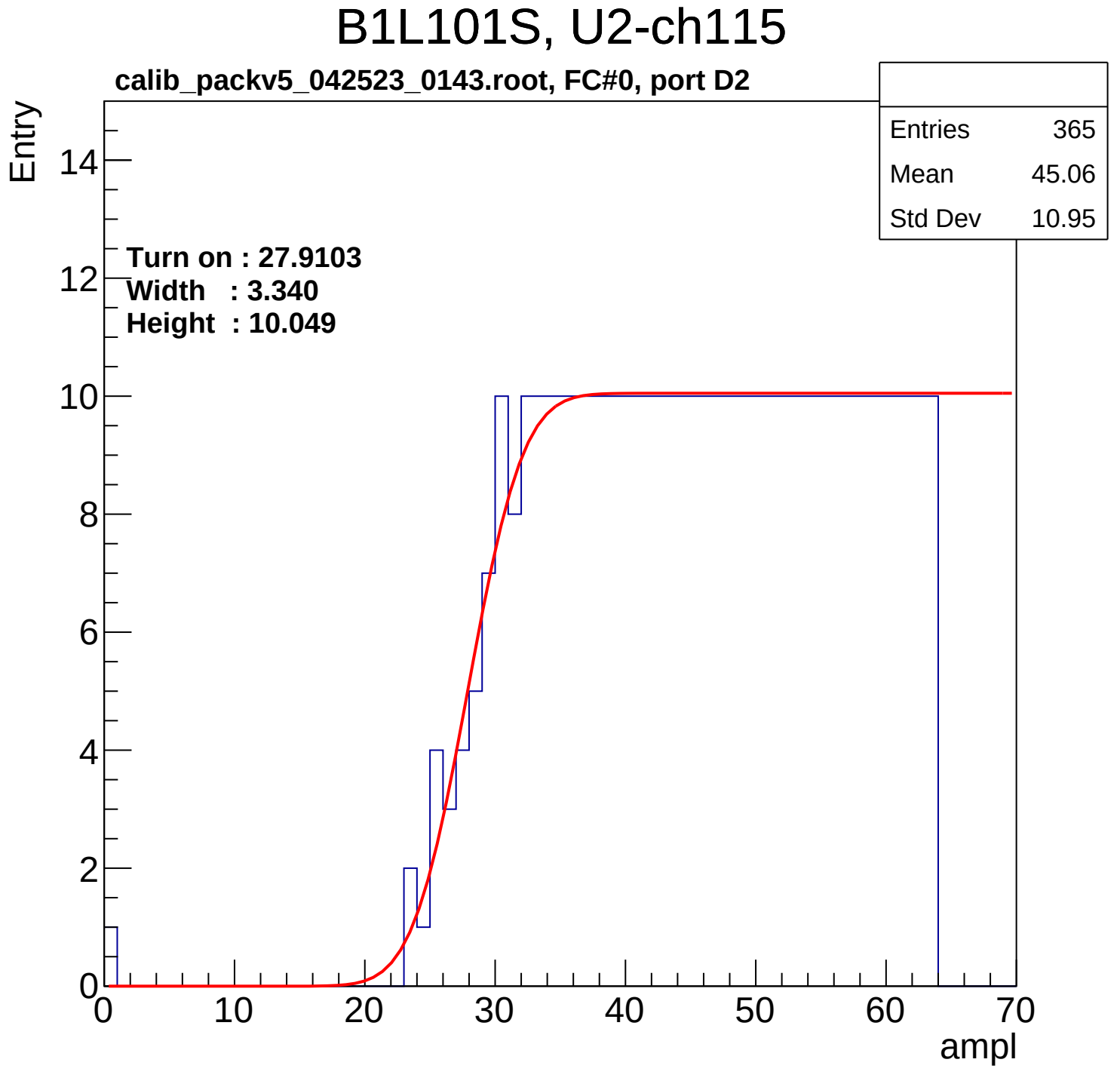
B1L101S, U2-ch115
calib_packv5_042523_0143.root, FC#0, port D2
Entries 365
Mean 45.06
Std Dev 10.95
Turn on : 27.9103
Width : 3.340
Height : 10.049
Entry
ampl
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4
6
8
10
12
14
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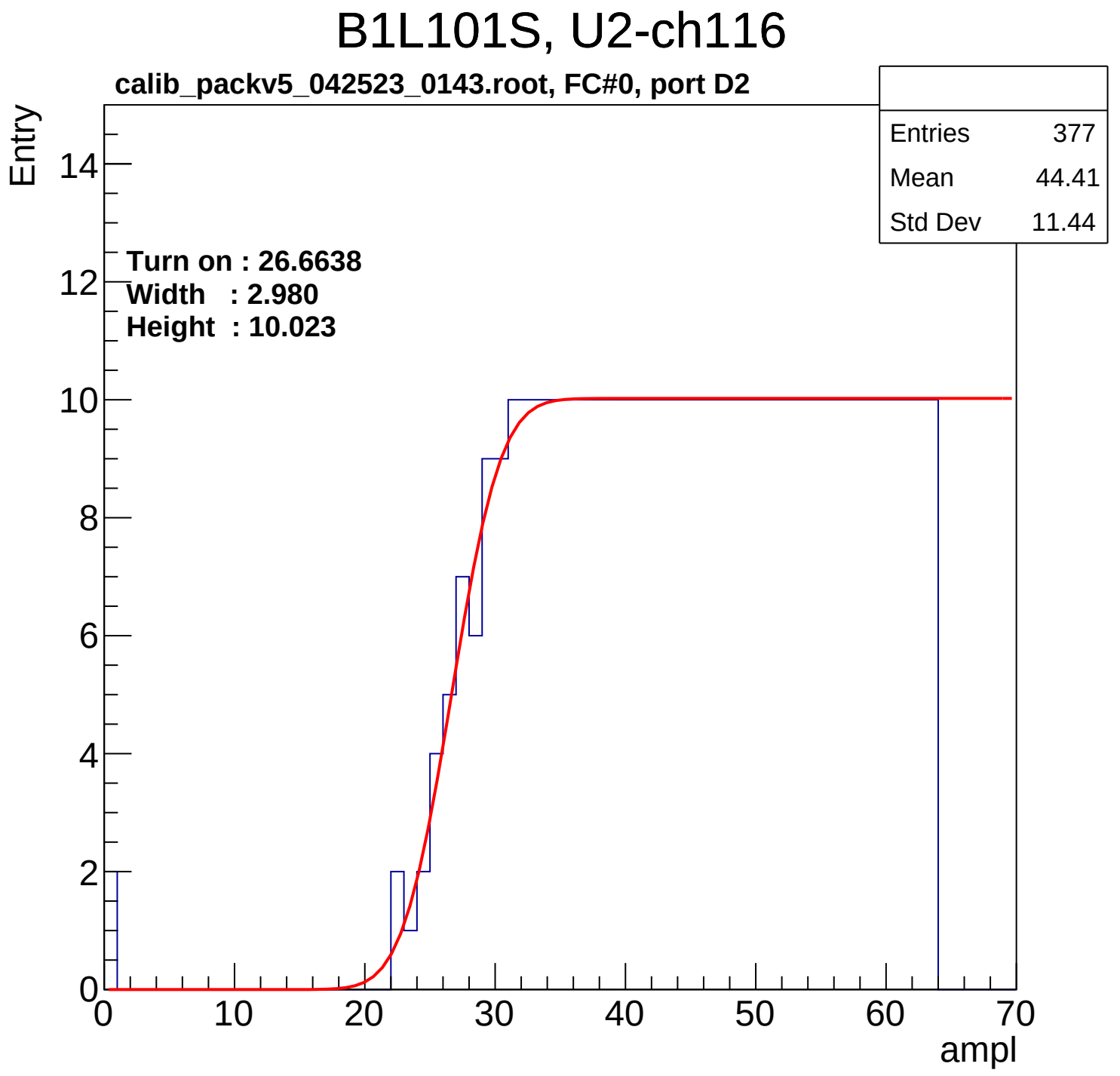
B1L101S, U2-ch116
calib_packv5_042523_0143.root, FC#0, port D2
Entries 377
Mean 44.41
Std Dev 11.44
Turn on : 26.6638
Width : 2.980
Height : 10.023
Entry
ampl
0
2
4
6
8
10
12
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0
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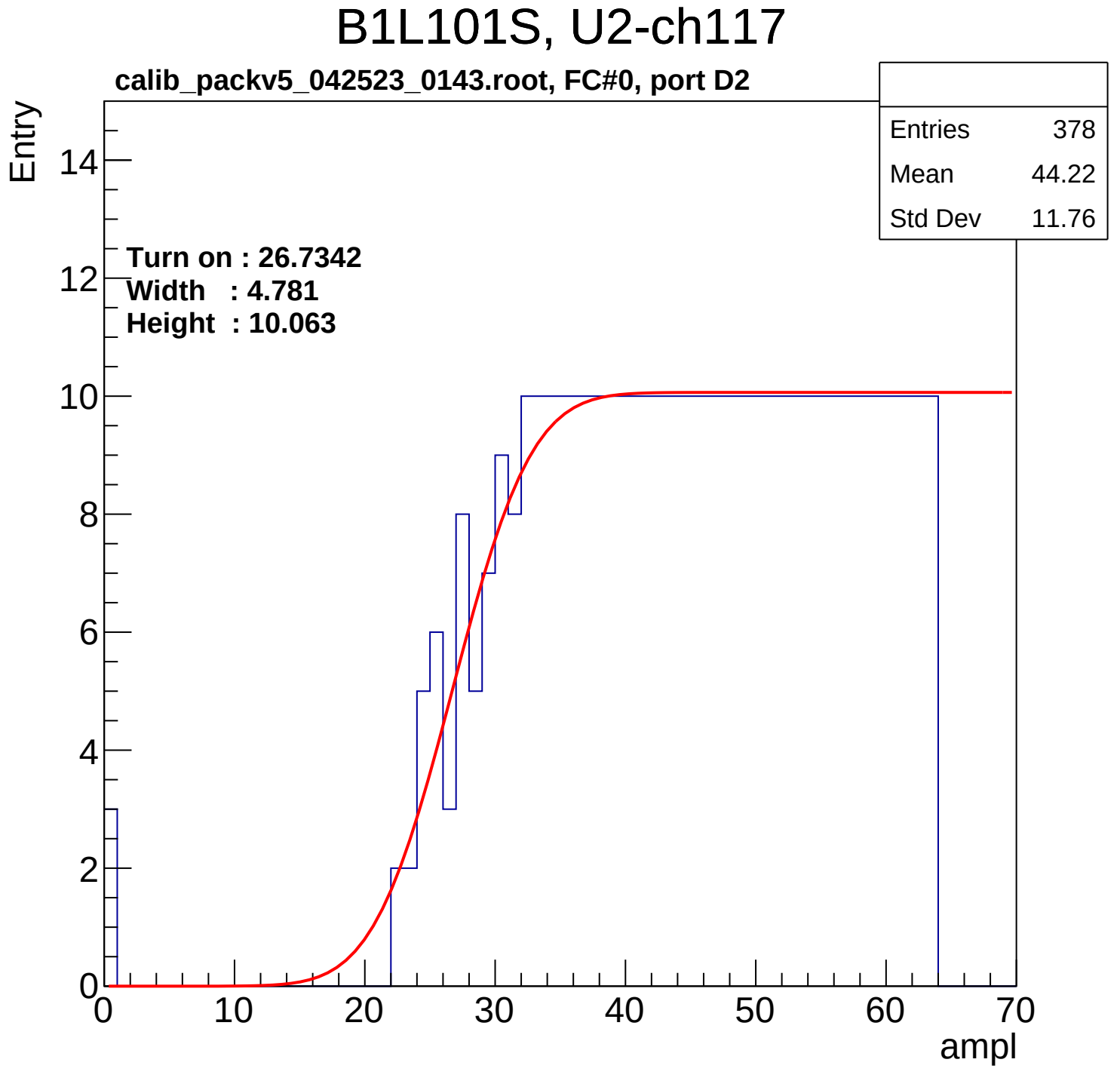
B1L101S, U2-ch117
calib_packv5_042523_0143.root, FC#0, port D2
Entries 378
Mean 44.22
Std Dev 11.76
Turn on : 26.7342
Width : 4.781
Height : 10.063
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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40
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60
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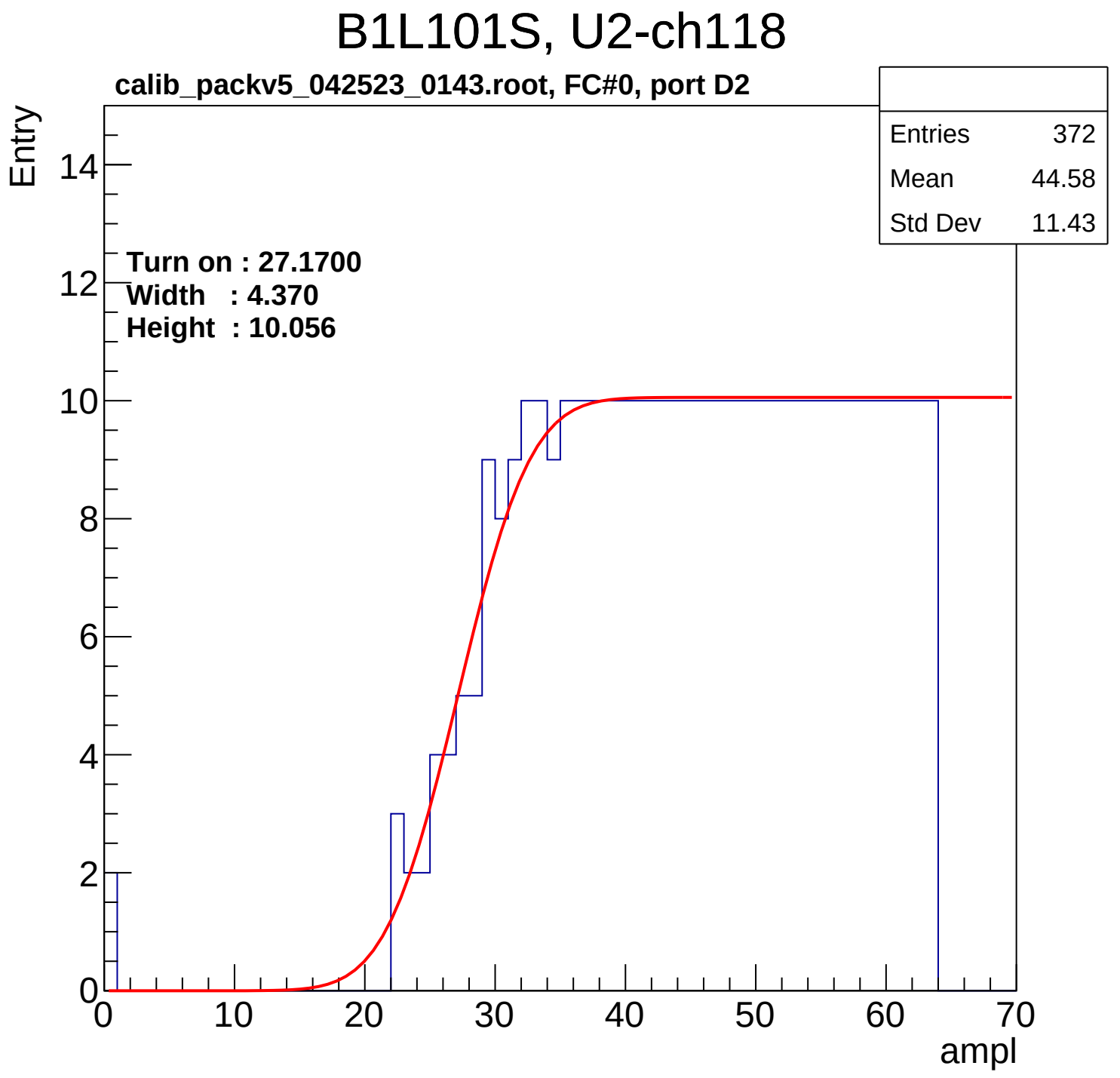
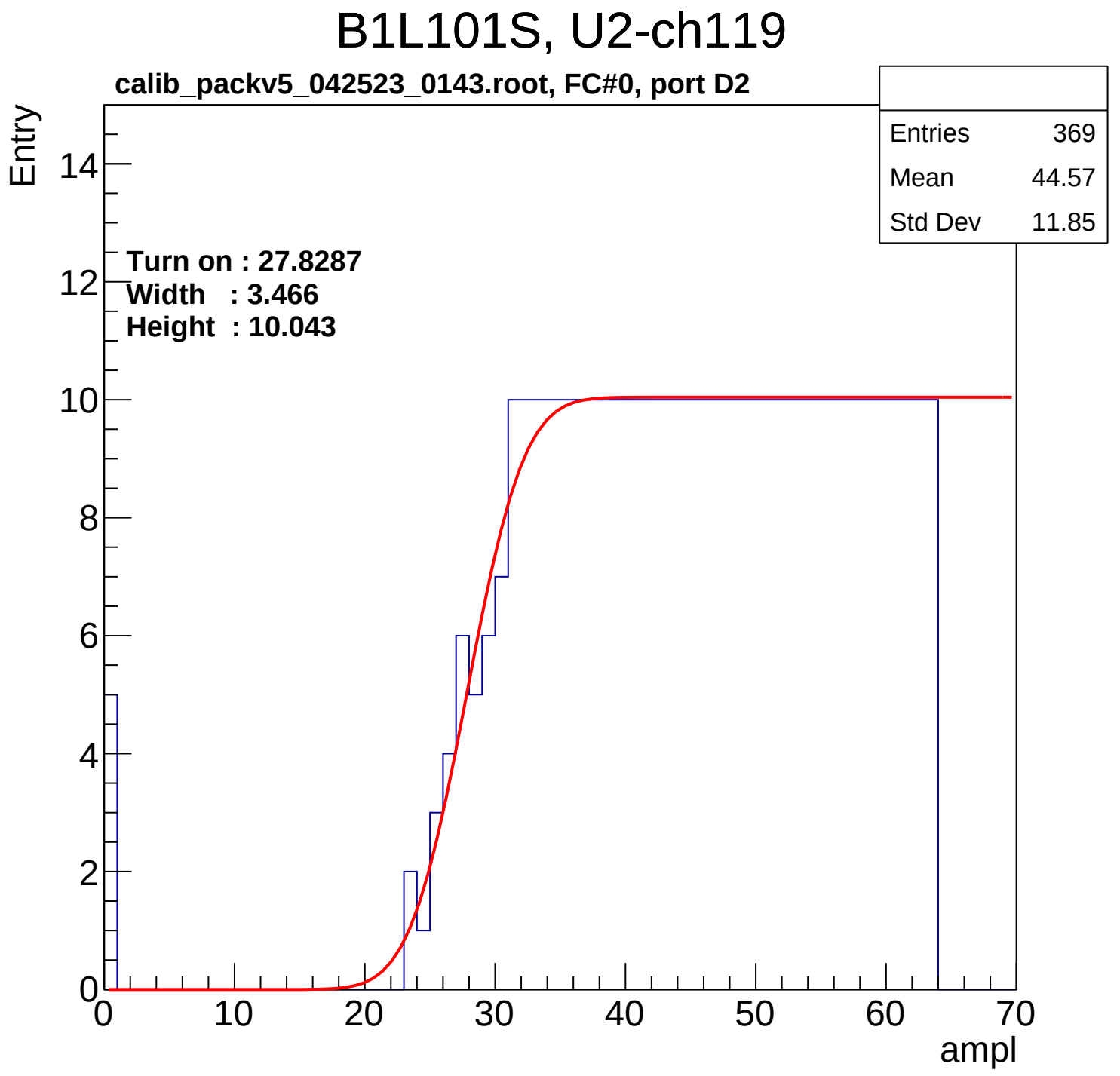
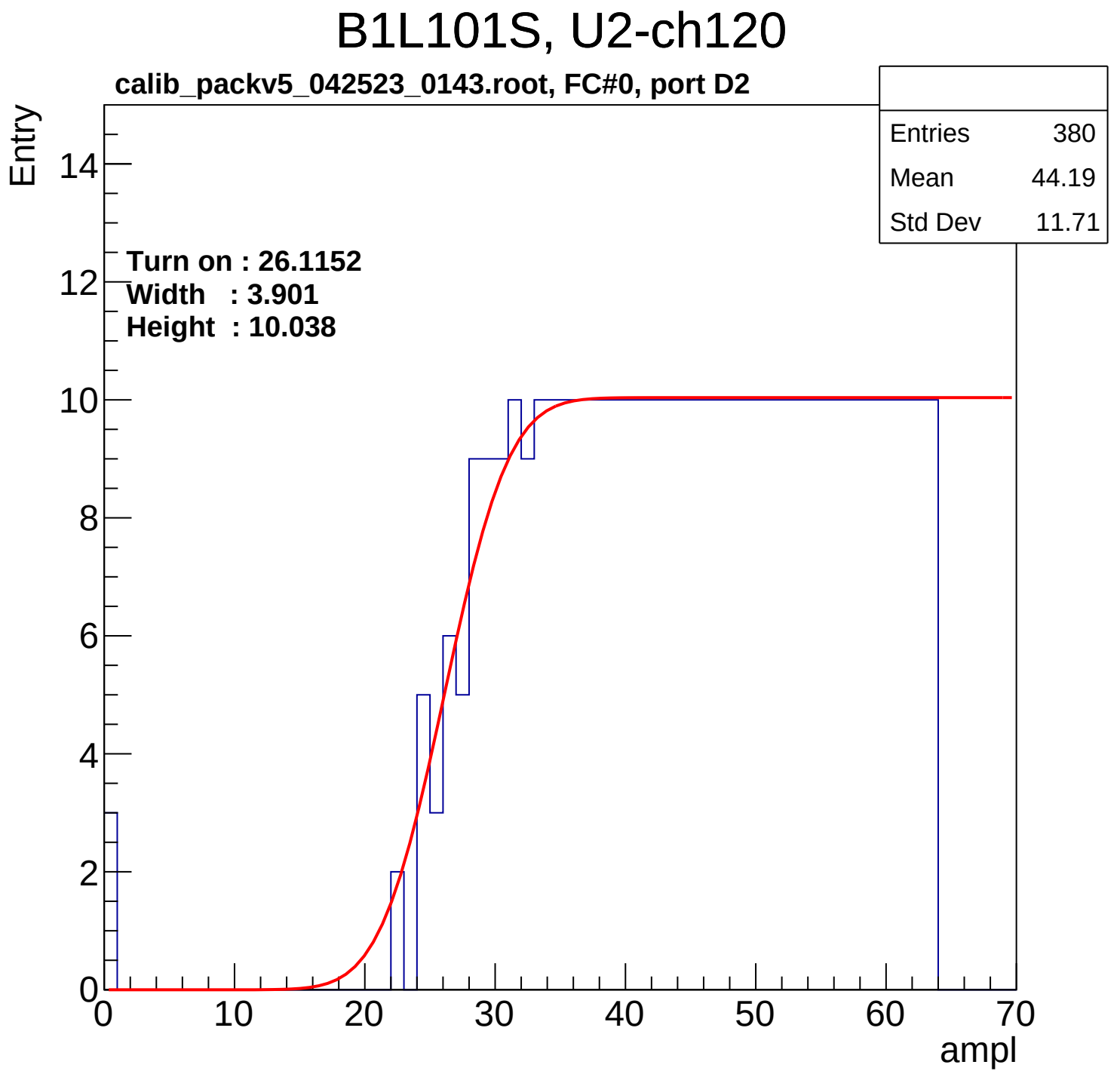

B1L101S, U2-ch118
calib_packv5_042523_0143.root, FC#0, port D2
Entries 372
Mean 44.58
Std Dev 11.43
Turn on : 27.1700
Width : 4.370
Height : 10.056
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L101S, U2-ch119
calib_packv5_042523_0143.root, FC#0, port D2
Entries 369
Mean 44.57
Std Dev 11.85
Turn on : 27.8287
Width : 3.466
Height : 10.043
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L101S, U2-ch120
calib_packv5_042523_0143.root, FC#0, port D2
Entries 380
Mean 44.19
Std Dev 11.71
Turn on : 26.1152
Width : 3.901
Height : 10.038
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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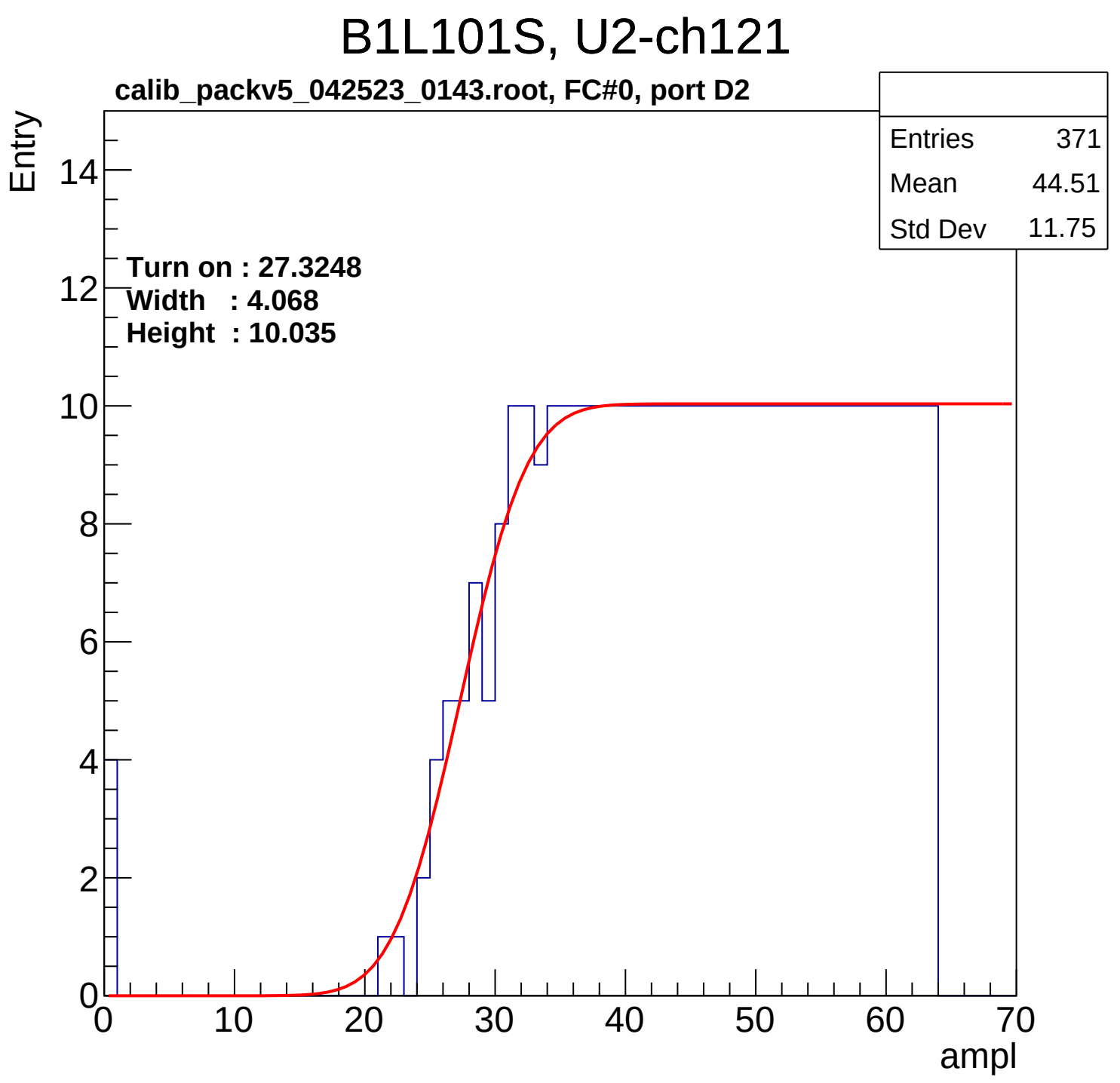
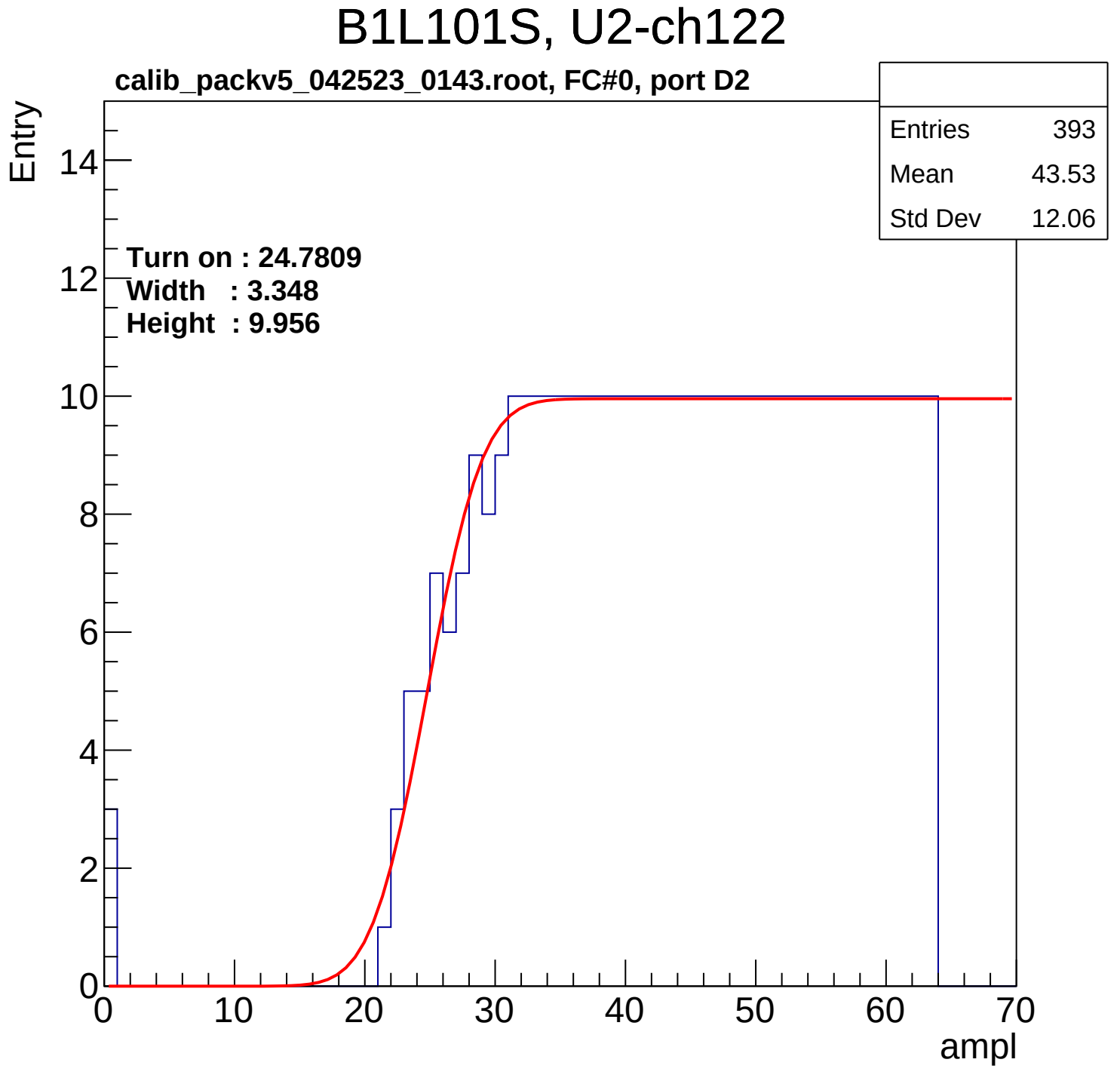

B1L101S, U2-ch121
calib_packv5_042523_0143.root, FC#0, port D2
Entries 371
Mean 44.51
Std Dev 11.75
Turn on : 27.3248
Width : 4.068
Height : 10.035
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L101S, U2-ch122
calib_packv5_042523_0143.root, FC#0, port D2
Entries 393
Mean 43.53
Std Dev 12.06
Turn on : 24.7809
Width : 3.348
Height : 9.956
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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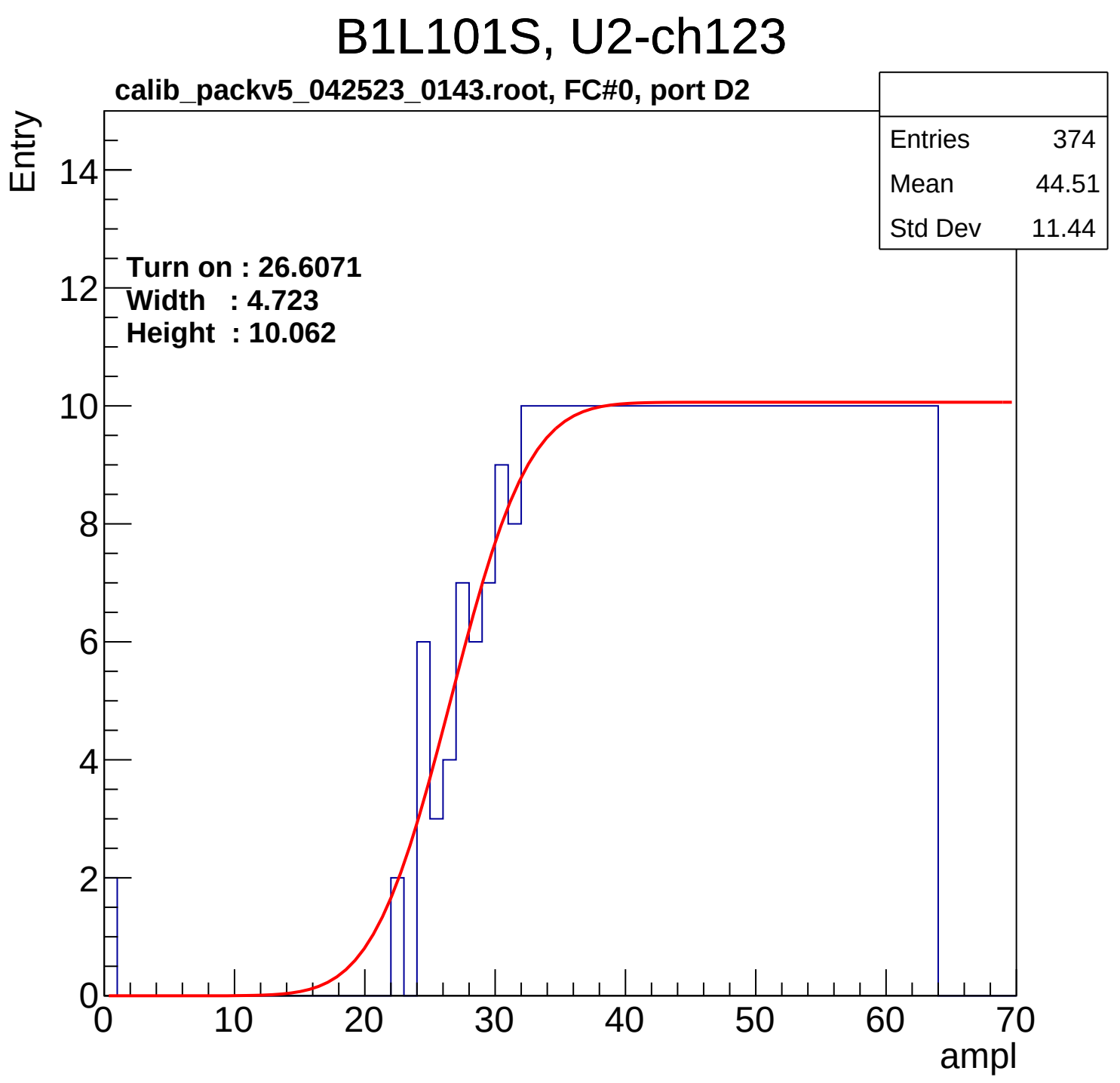
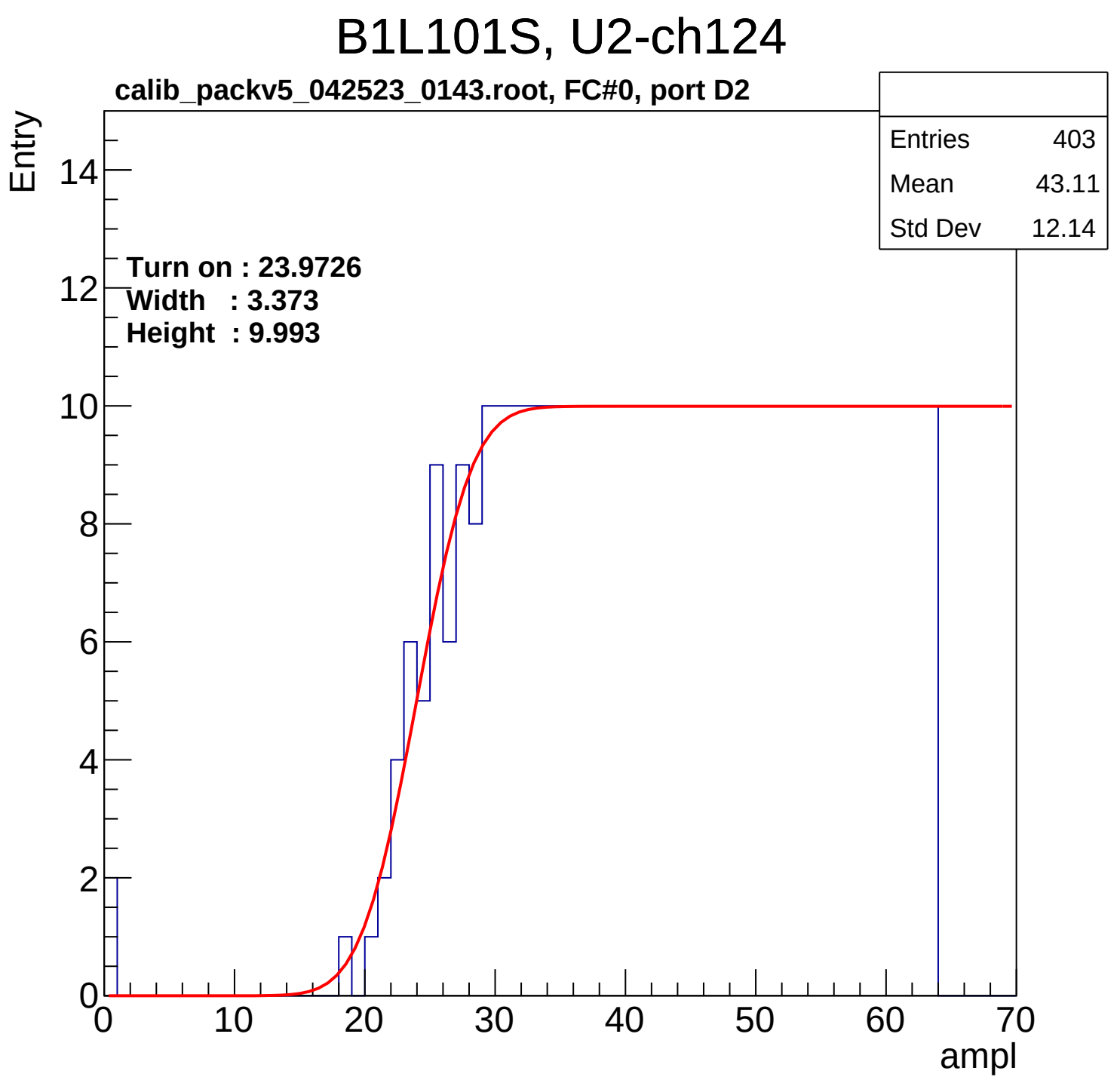
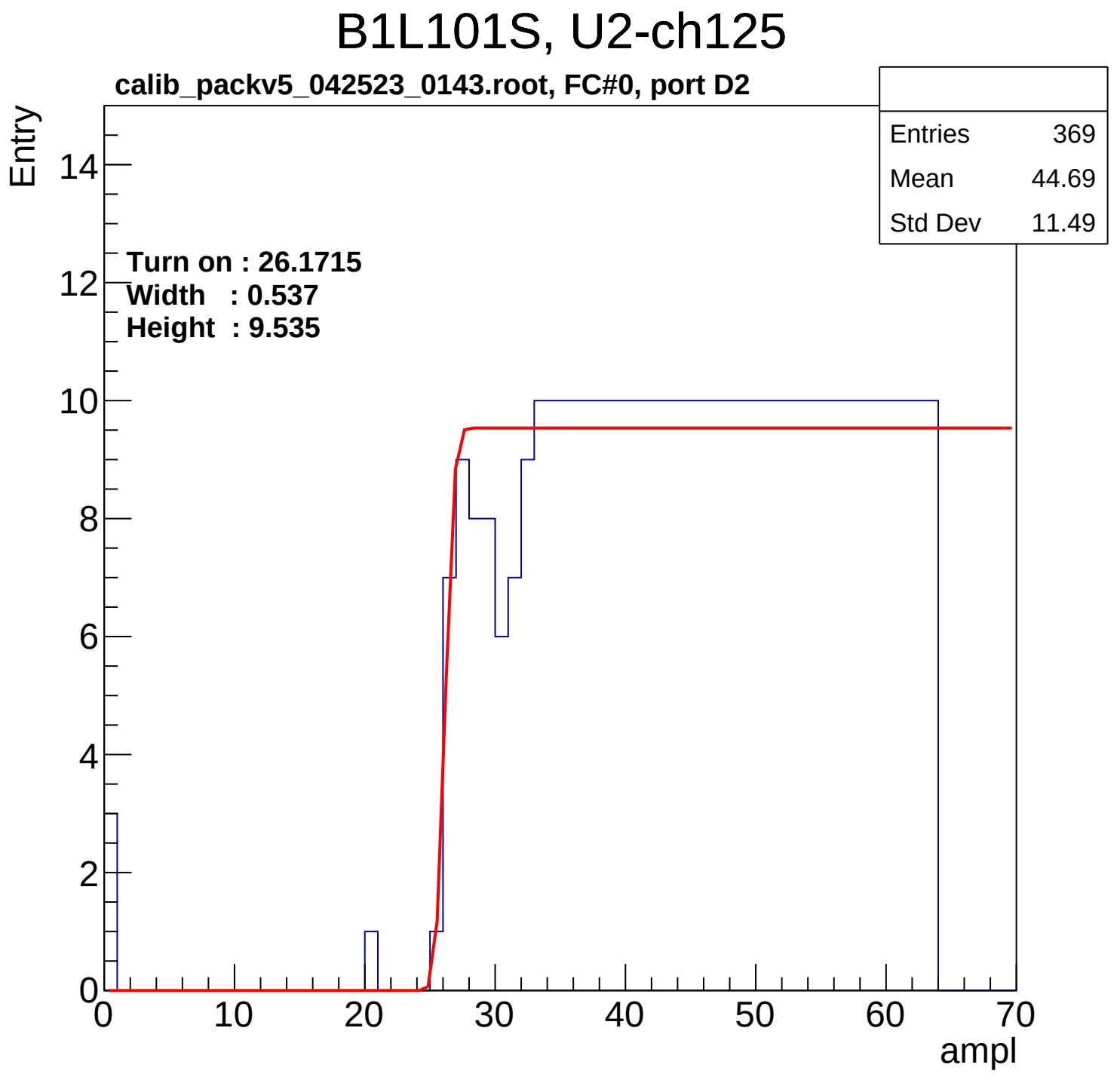
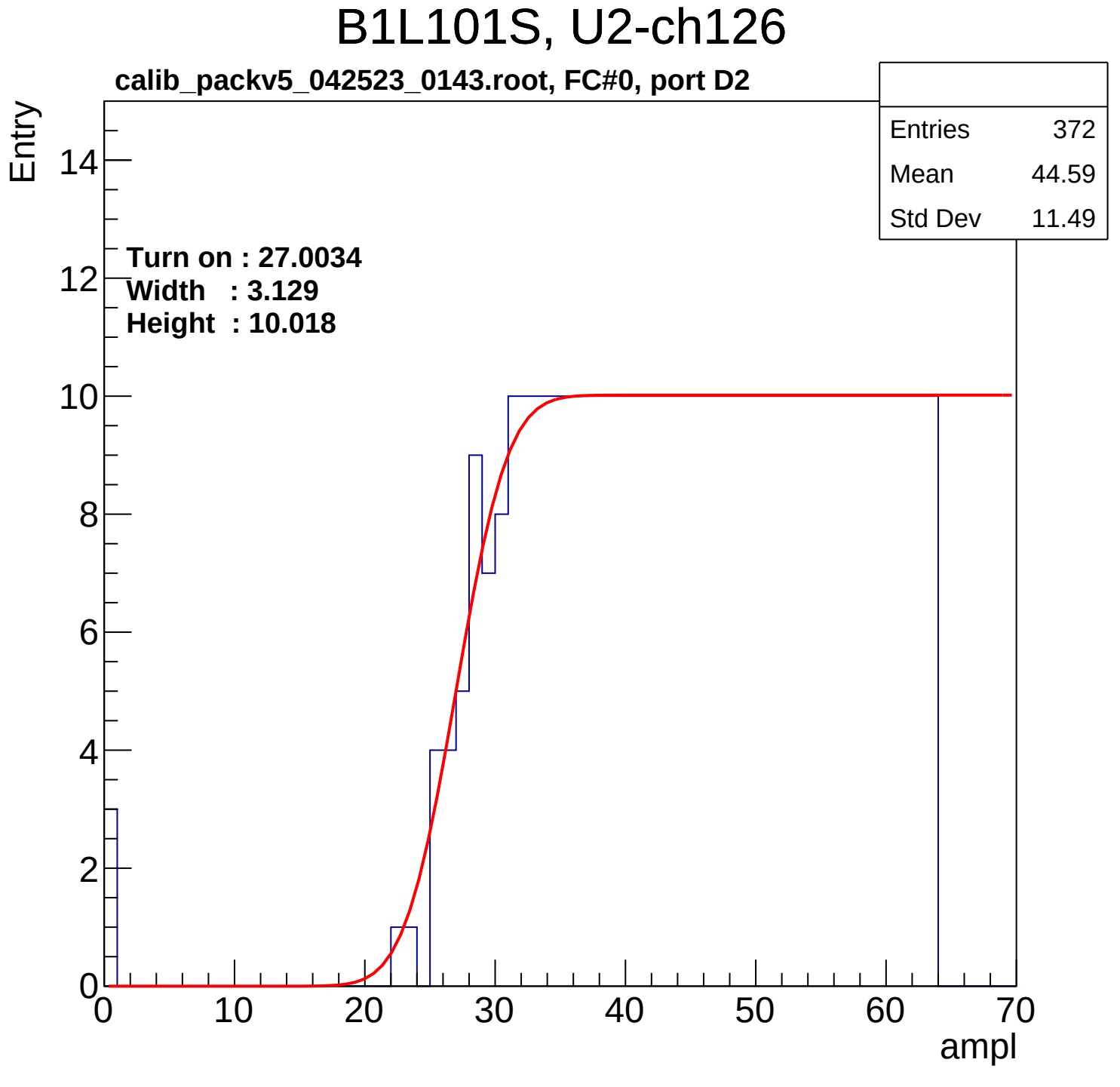

B1L101S, U2-ch123
calib_packv5_042523_0143.root, FC#0, port D2
Entries 374
Mean 44.51
Std Dev 11.44
Turn on : 26.6071
Width : 4.723
Height : 10.062
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L101S, U2-ch124
calib_packv5_042523_0143.root, FC#0, port D2
Entries 403
Mean 43.11
Std Dev 12.14
Turn on : 23.9726
Width : 3.373
Height : 9.993
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L101S, U2-ch125
calib_packv5_042523_0143.root, FC#0, port D2
Entries 369
Mean 44.69
Std Dev 11.49
Turn on : 26.1715
Width : 0.537
Height : 9.535
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L101S, U2-ch126
calib_packv5_042523_0143.root, FC#0, port D2
Entries 372
Mean 44.59
Std Dev 11.49
Turn on : 27.0034
Width : 3.129
Height : 10.018
Entry
ampl
0
2
4
6
8
10
12
14
0
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20
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40
50
60
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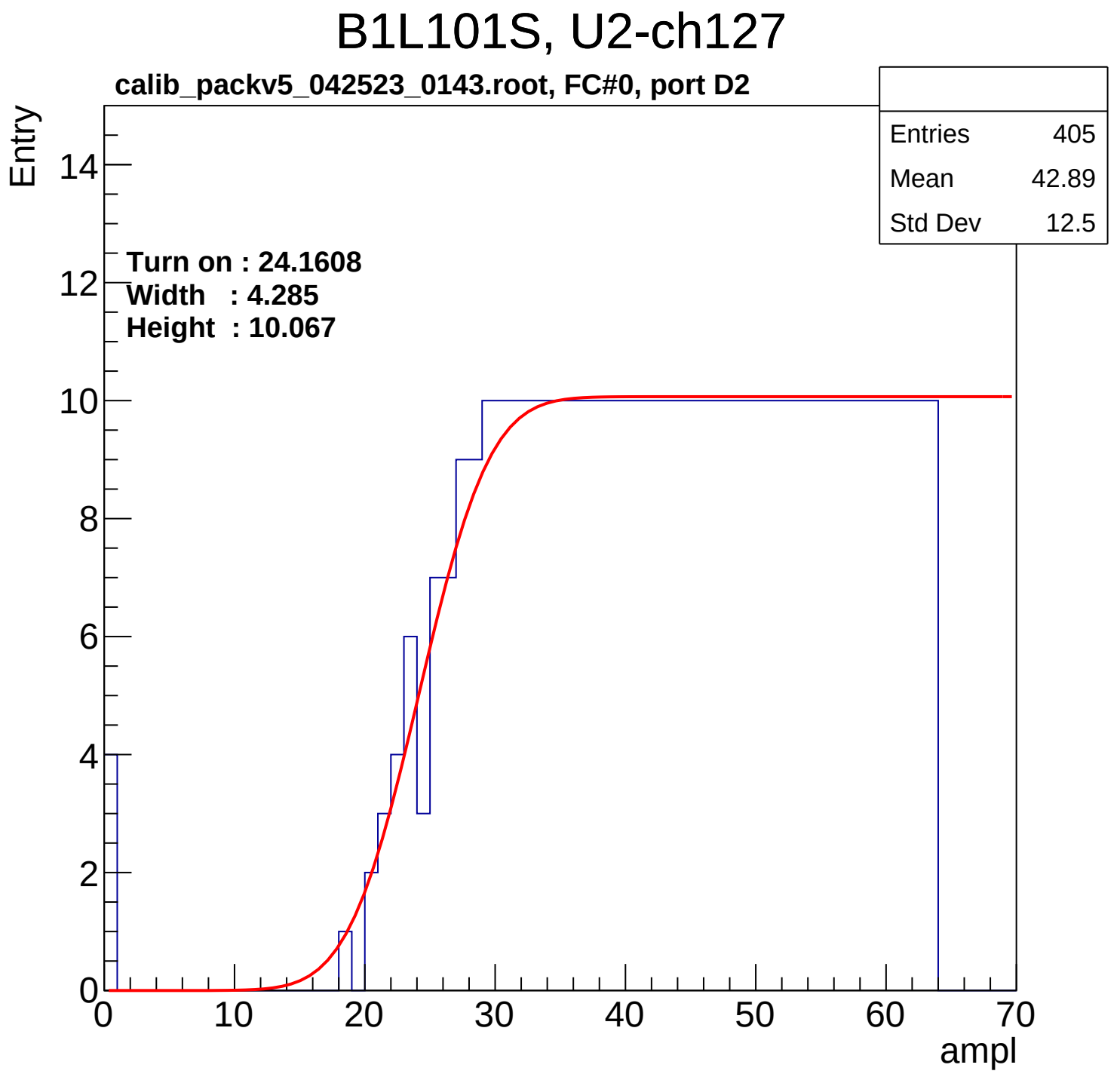
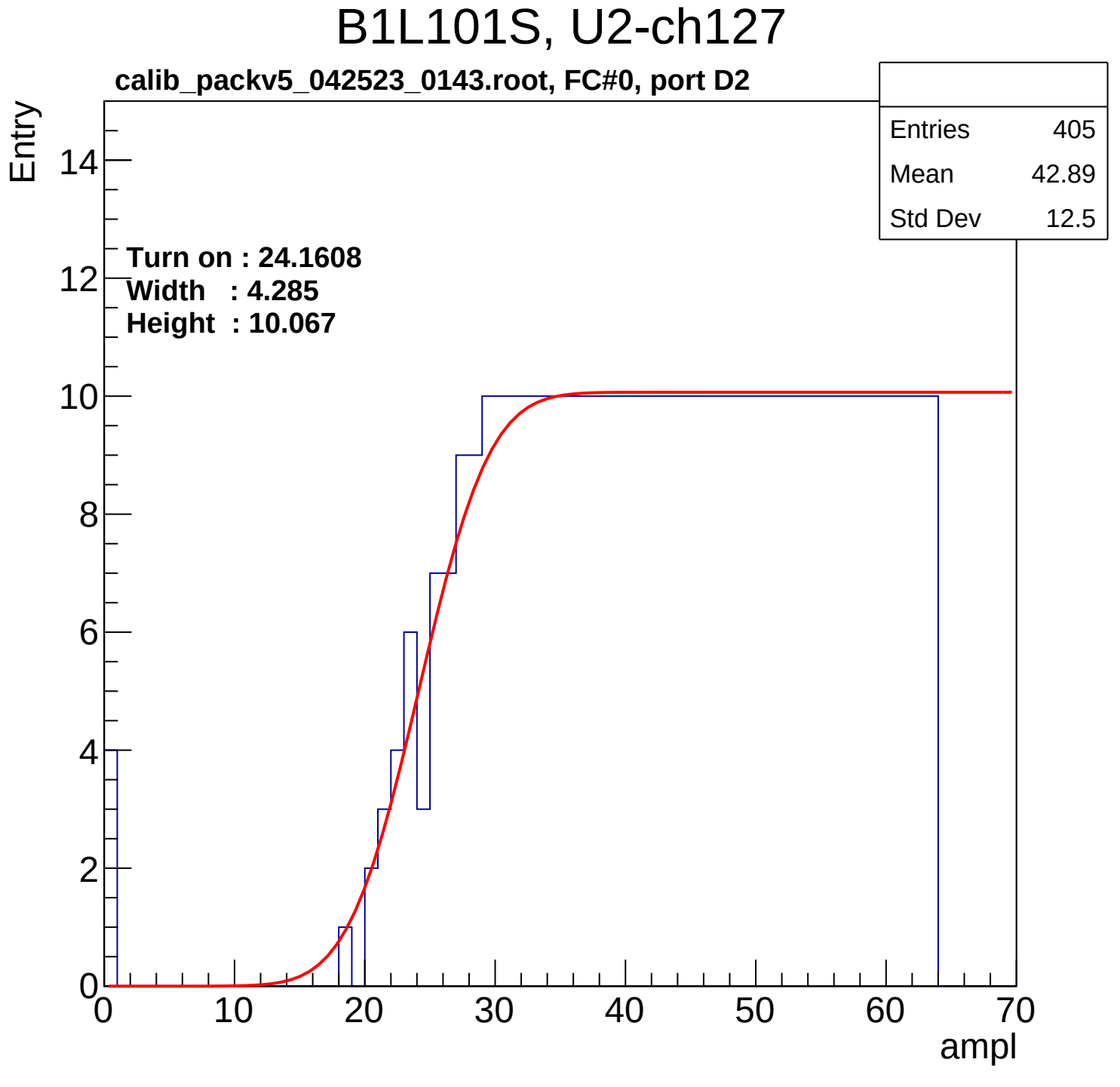

B1L101S, U2-ch127
calib_packv5_042523_0143.root, FC#0, port D2
Entries 405
Mean 42.89
Std Dev 12.5
Turn on : 24.1608
Width : 4.285
Height : 10.067
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L101S, U2-ch127
calib_packv5_042523_0143.root, FC#0, port D2
Entries 405
Mean 42.89
Std Dev 12.5
Turn on : 24.1608
Width : 4.285
Height : 10.067
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70