



# B1L101S, U16-ch0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	374
Mean	44.33
Std Dev	11.94

Turn on : 26.8172

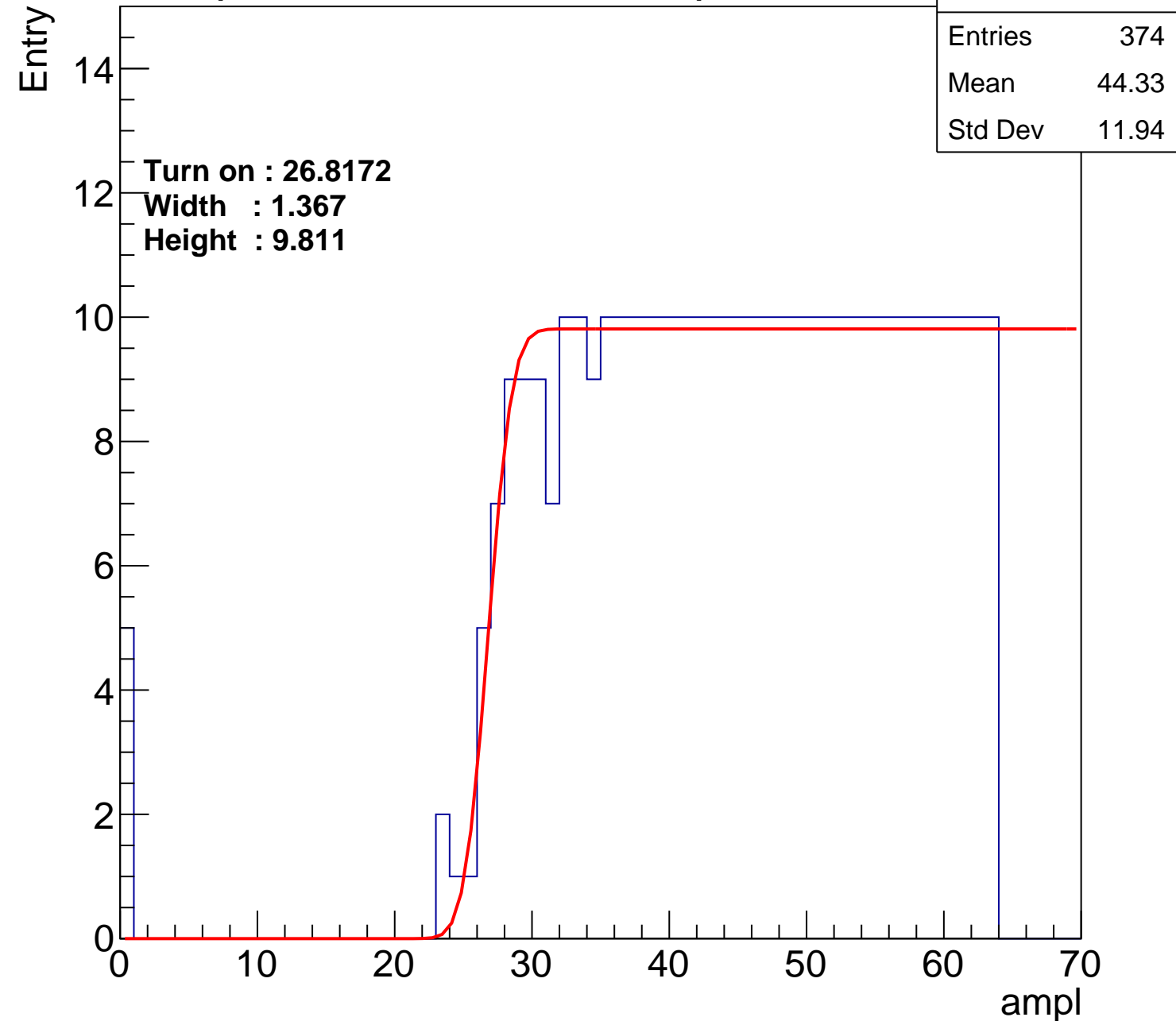
Width : 1.367

Height : 9.811

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U16-ch1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	379
Mean	44.14
Std Dev	11.92

**Turn on : 26.9933**

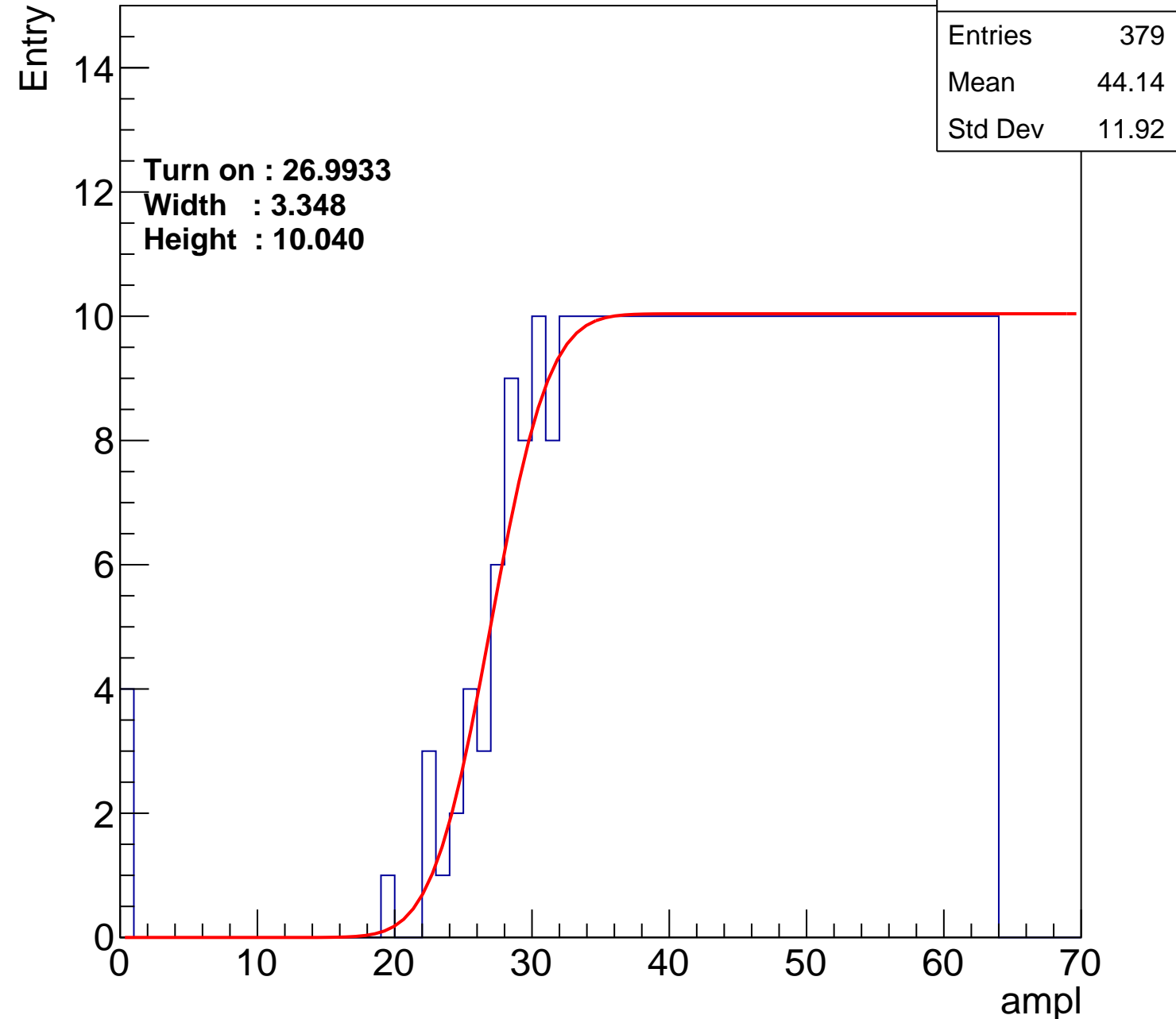
**Width : 3.348**

**Height : 10.040**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U16-ch2

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	382
Mean	44.14
Std Dev	11.6

Turn on : 26.5900

Width : 3.996

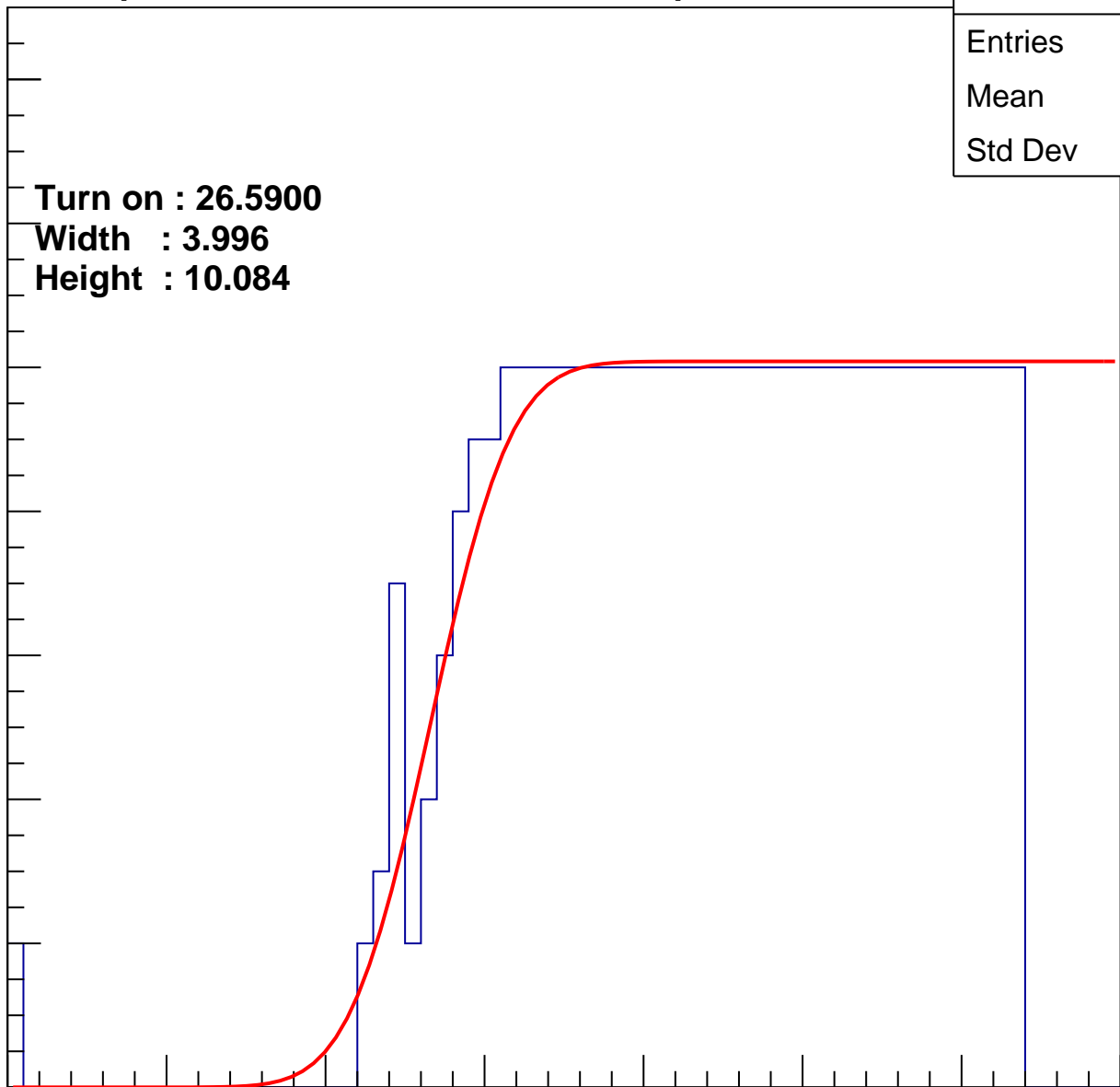
Height : 10.084

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U16-ch3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	361
Mean	45.1
Std Dev	11.27

Turn on : 28.1632

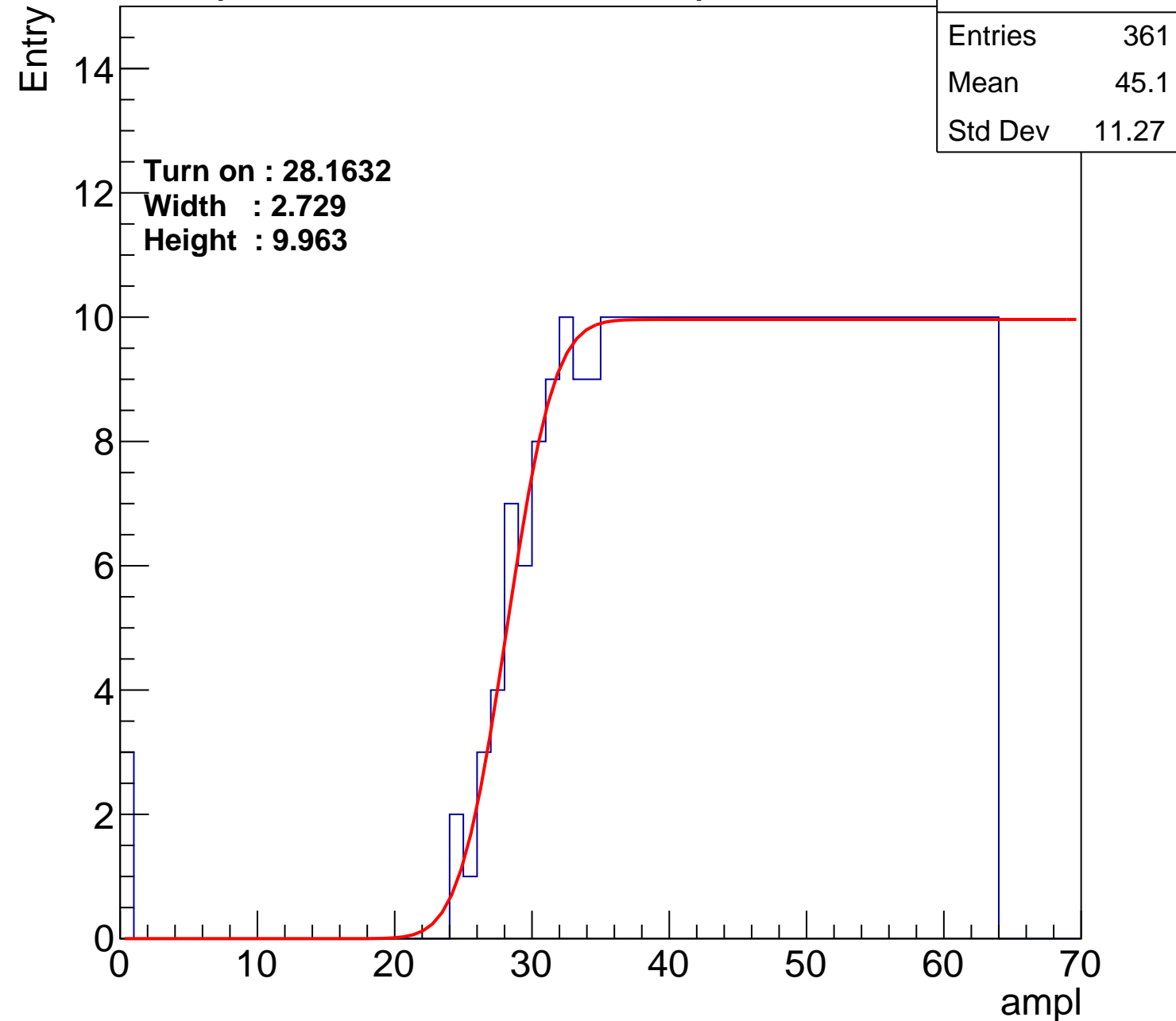
Width : 2.729

Height : 9.963

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U16-ch4

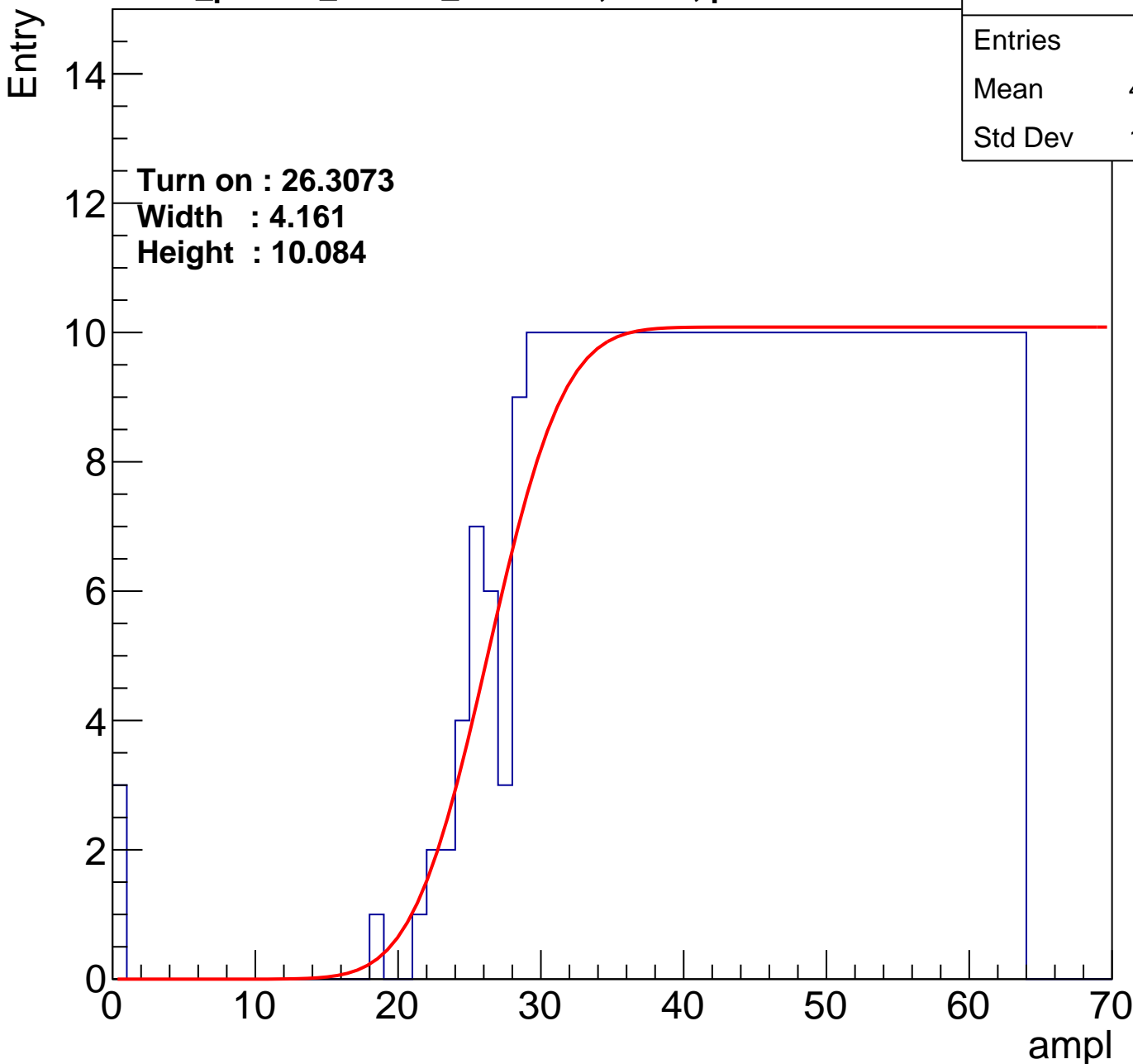
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	388
Mean	43.79
Std Dev	11.93

Turn on : 26.3073

Width : 4.161

Height : 10.084



# B1L101S, U16-ch5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	379
Mean	44.27
Std Dev	11.63

**Turn on : 26.6225**

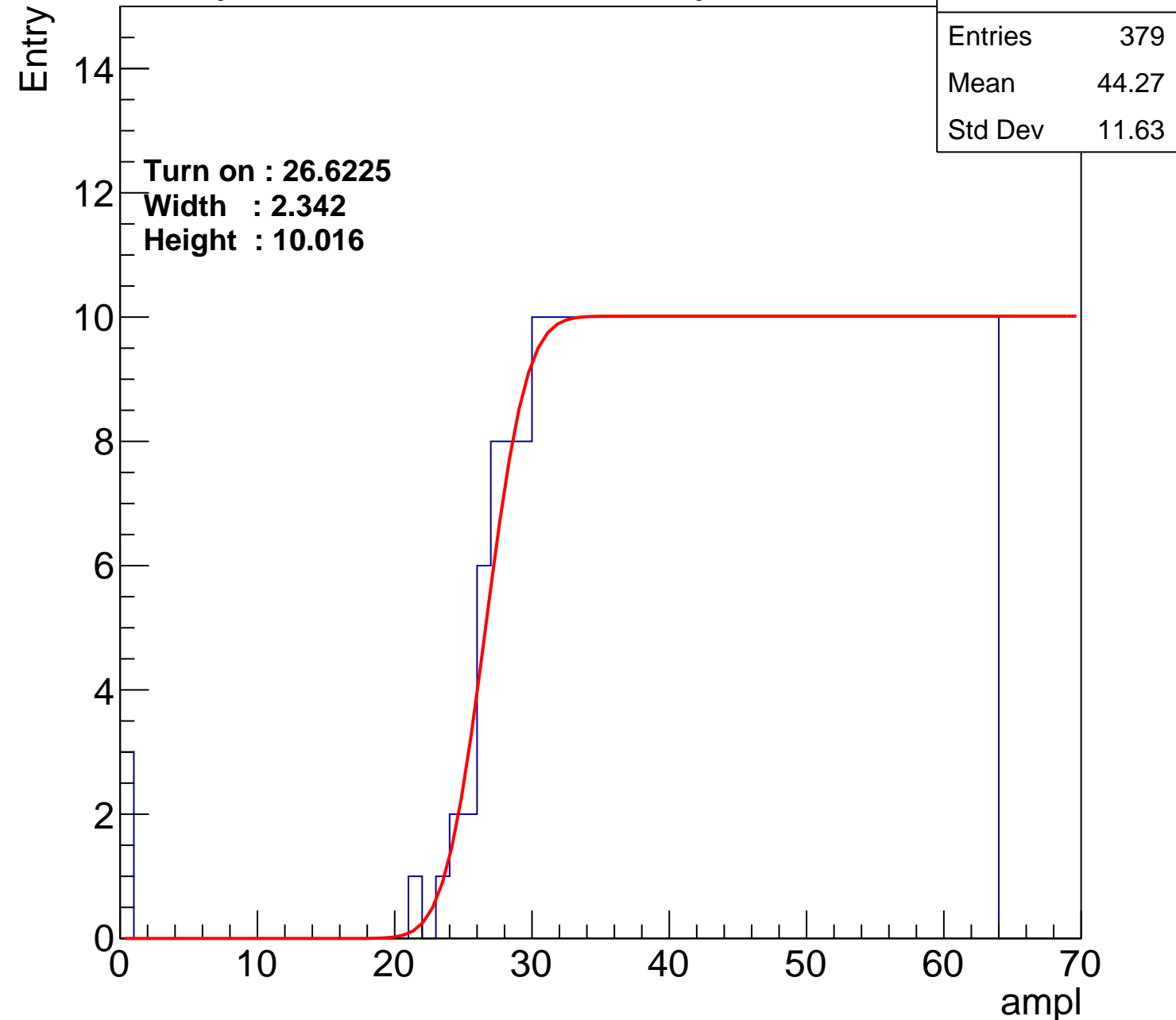
**Width : 2.342**

**Height : 10.016**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U16-ch6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	369
Mean	44.84
Std Dev	11.1

Turn on : 28.1927

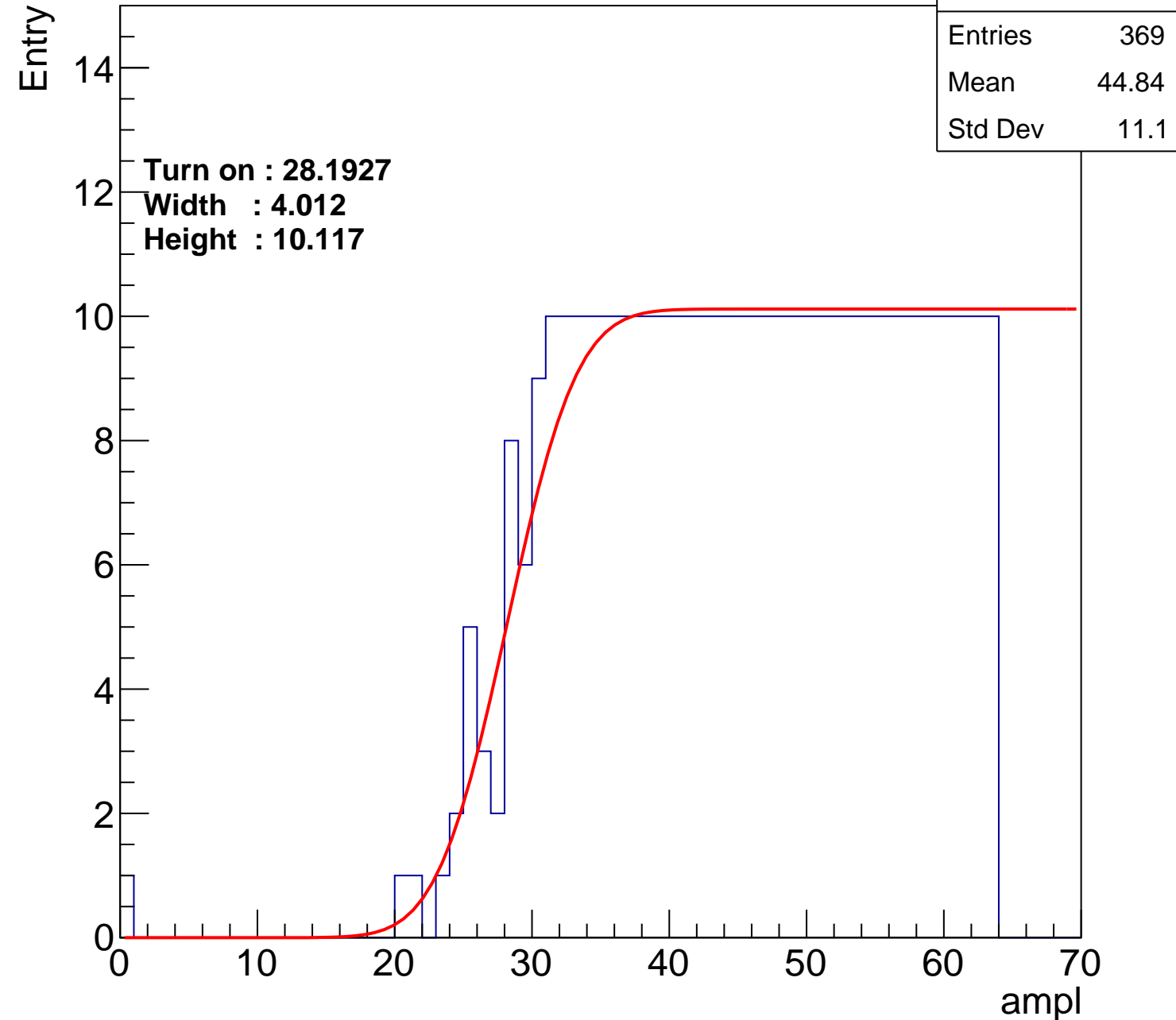
Width : 4.012

Height : 10.117

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L101S, U16-ch7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	392
Mean	43.44
Std Dev	12.38

Turn on : 25.9497

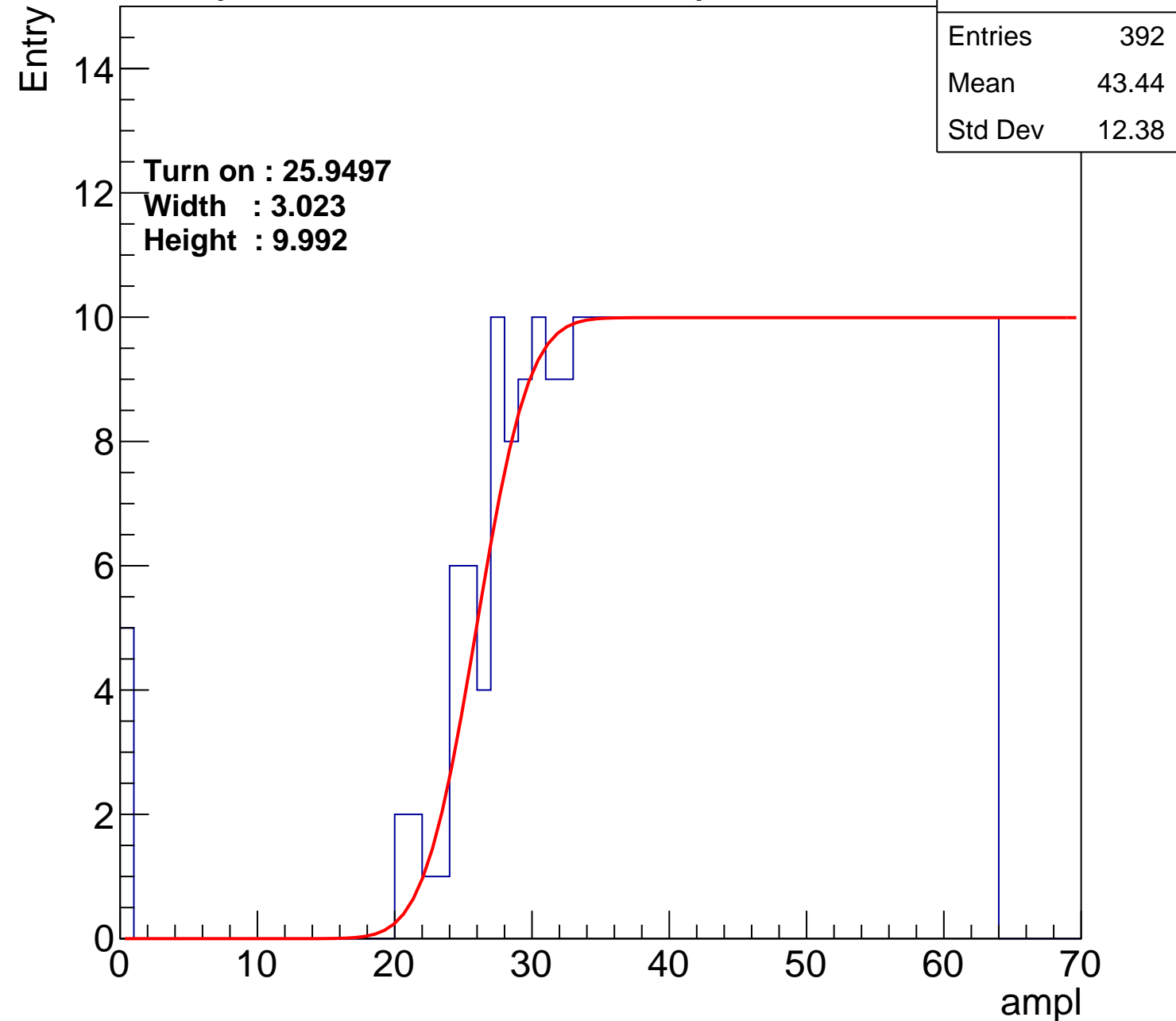
Width : 3.023

Height : 9.992

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U16-ch8

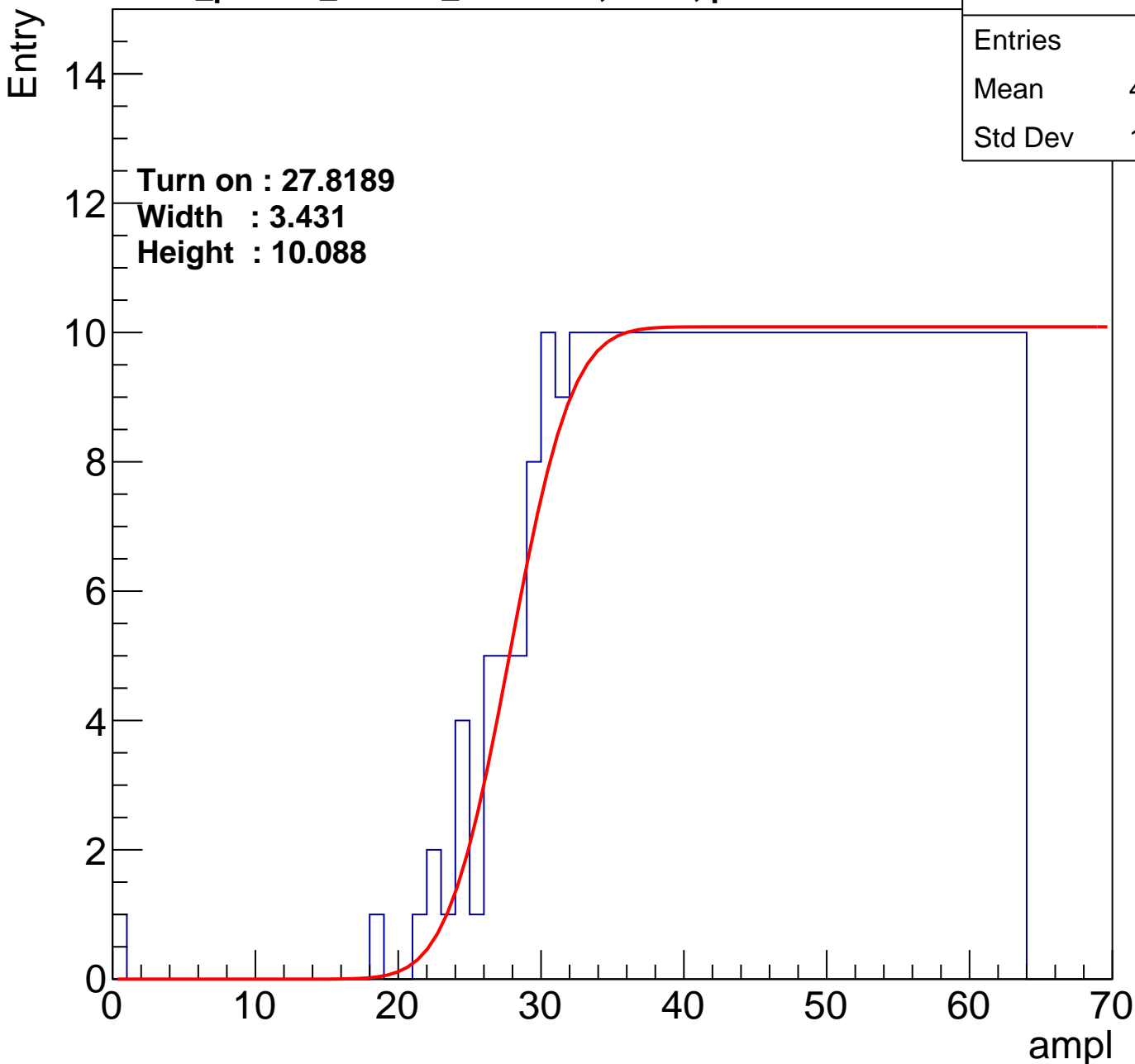
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	373
Mean	44.62
Std Dev	11.25

Turn on : 27.8189

Width : 3.431

Height : 10.088



# B1L101S, U16-ch9

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	394
Mean	43.55
Std Dev	11.98

Turn on : 25.0561

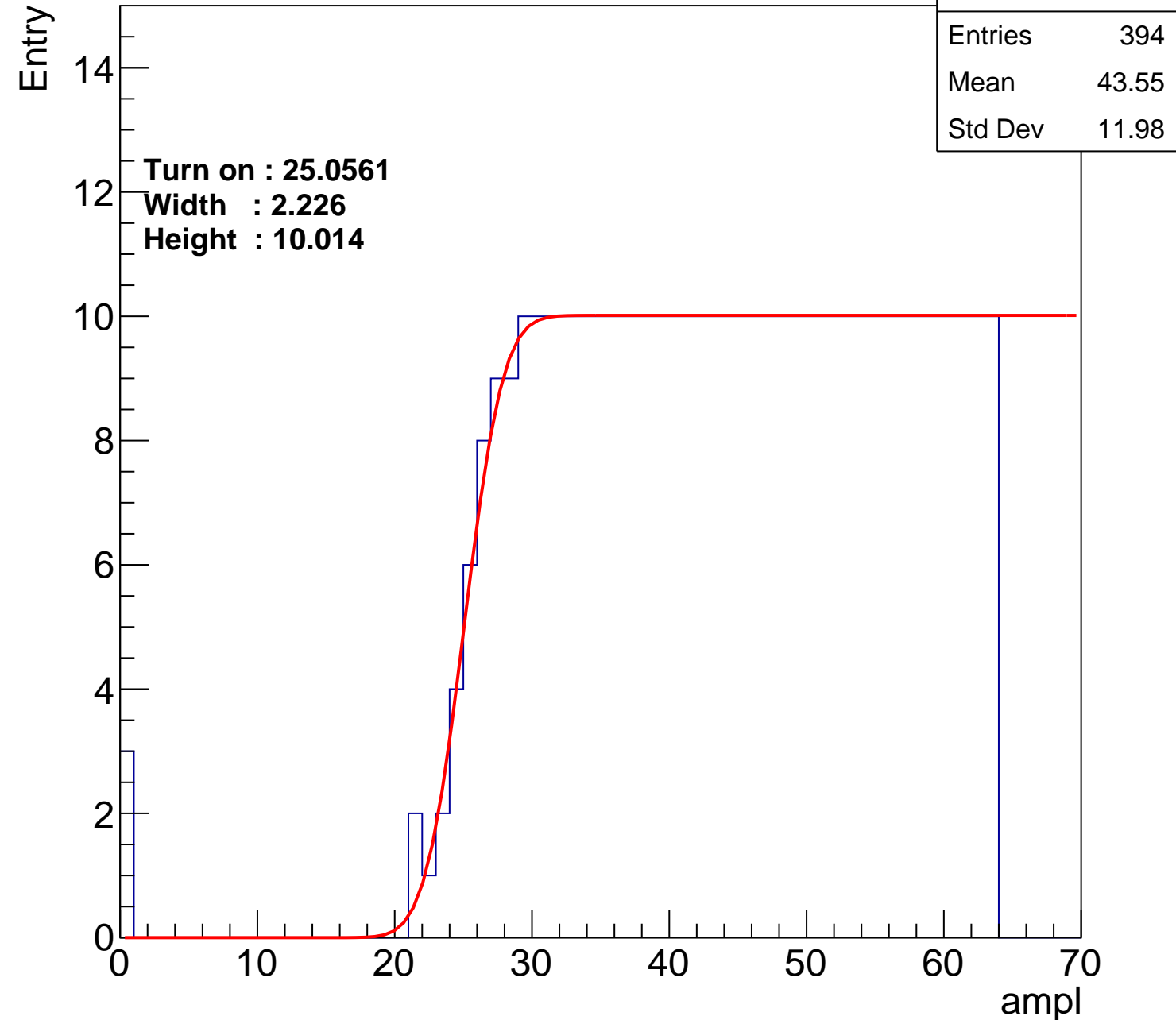
Width : 2.226

Height : 10.014

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U16-ch10

calib\_packv5\_042523\_0143.root, FC#0, port D2

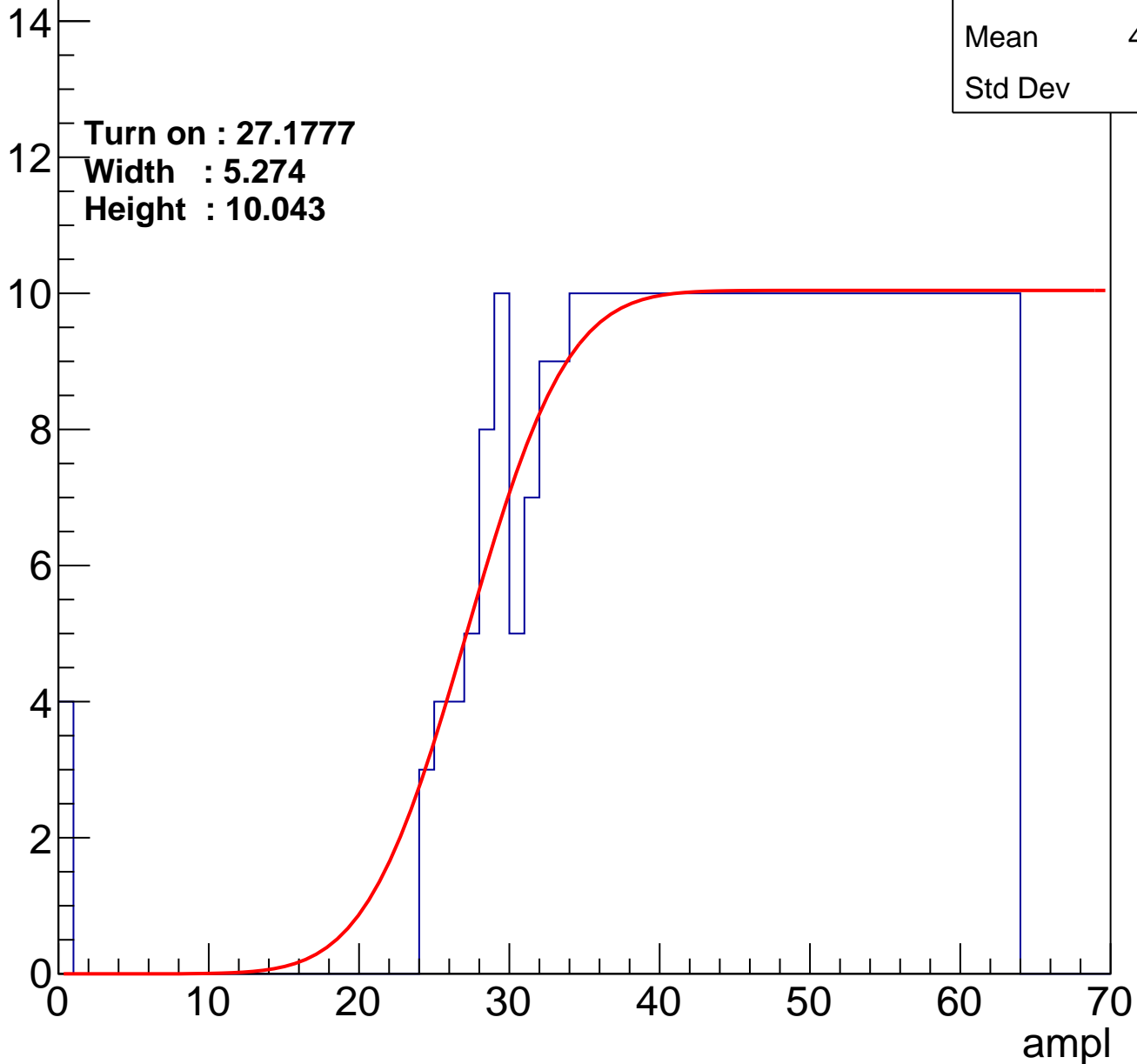
Entries	368
Mean	44.64
Std Dev	11.7

Turn on : 27.1777

Width : 5.274

Height : 10.043

Entry



# B1L101S, U16-ch11

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	373
Mean	44.47
Std Dev	11.71

Turn on : 27.0175

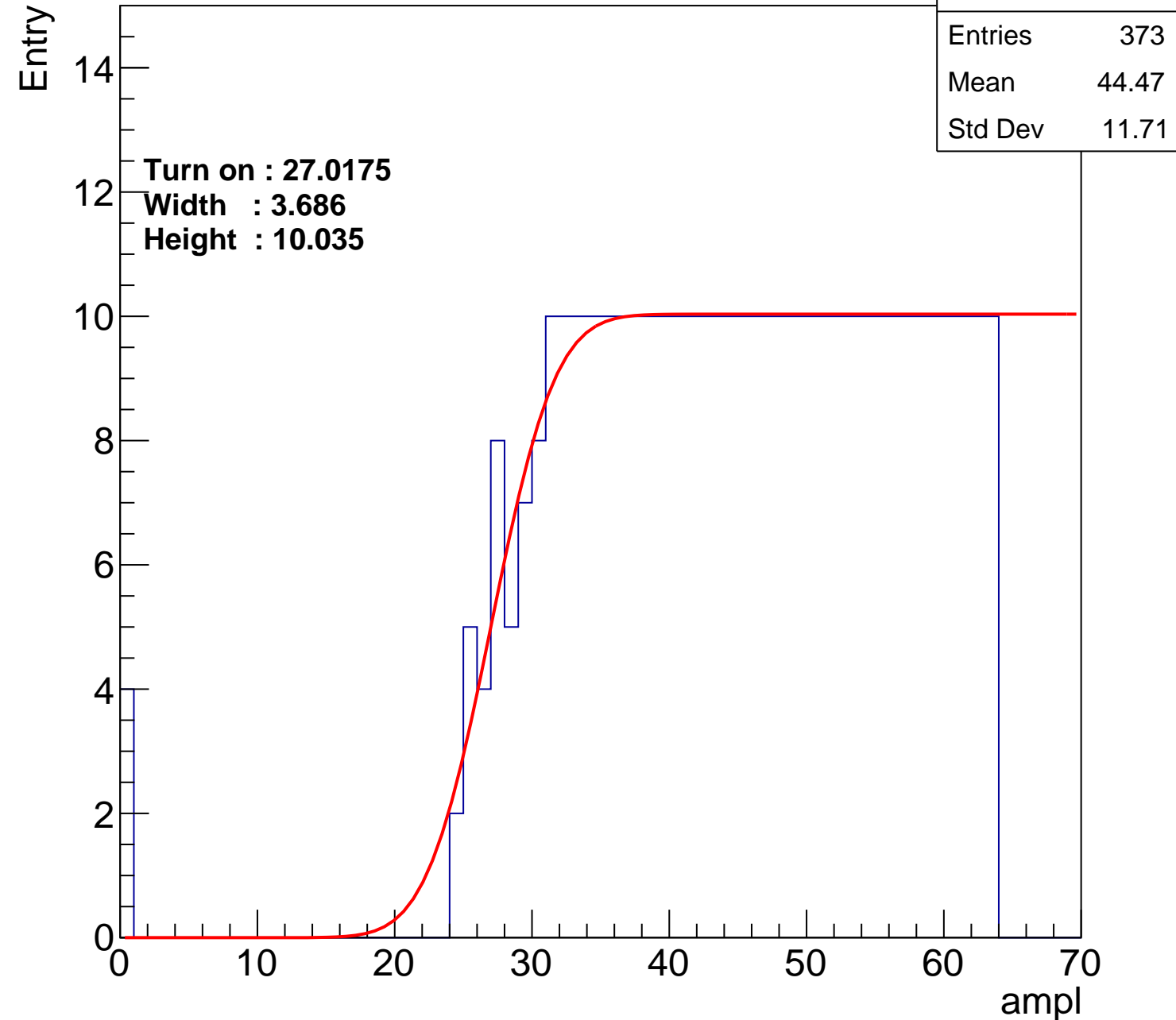
Width : 3.686

Height : 10.035

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U16-ch12

calib\_packv5\_042523\_0143.root, FC#0, port D2

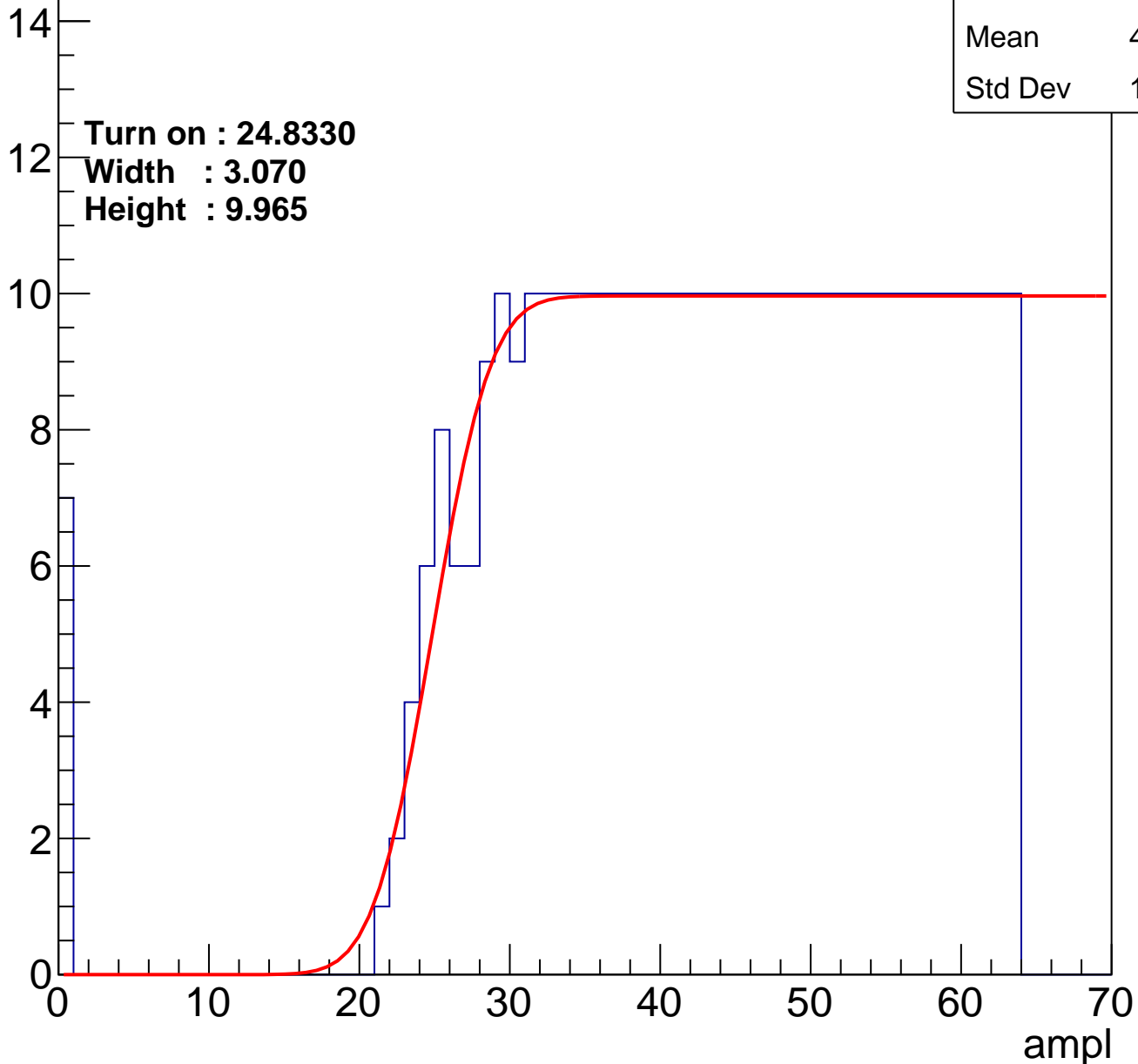
Entries	398
Mean	43.07
Std Dev	12.74

Turn on : 24.8330

Width : 3.070

Height : 9.965

Entry



# B1L101S, U16-ch13

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	367
Mean	44.8
Std Dev	11.35

**Turn on : 27.7795**

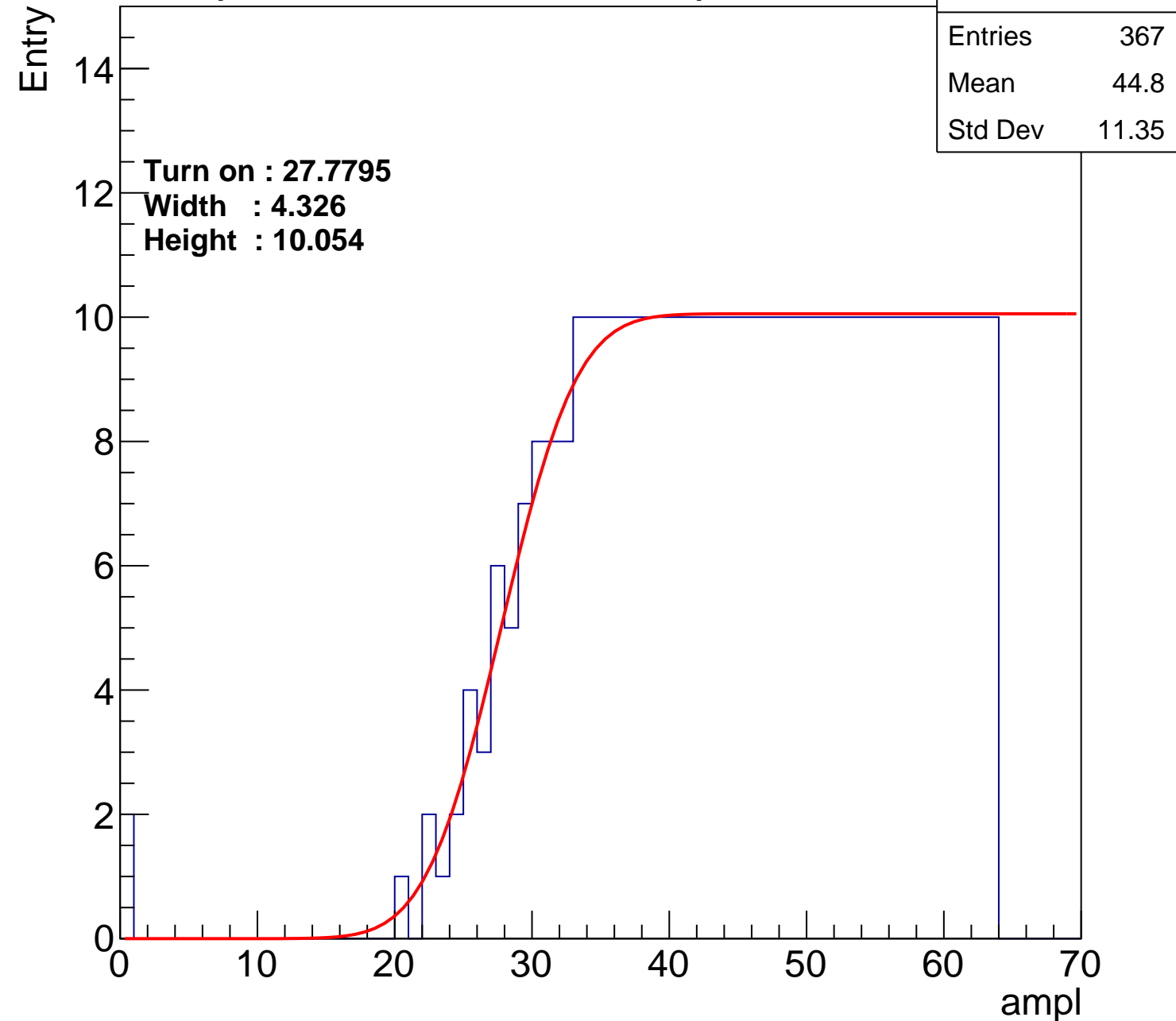
**Width : 4.326**

**Height : 10.054**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U16-ch14

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	361
Mean	45.29
Std Dev	10.78

Turn on : 28.0715

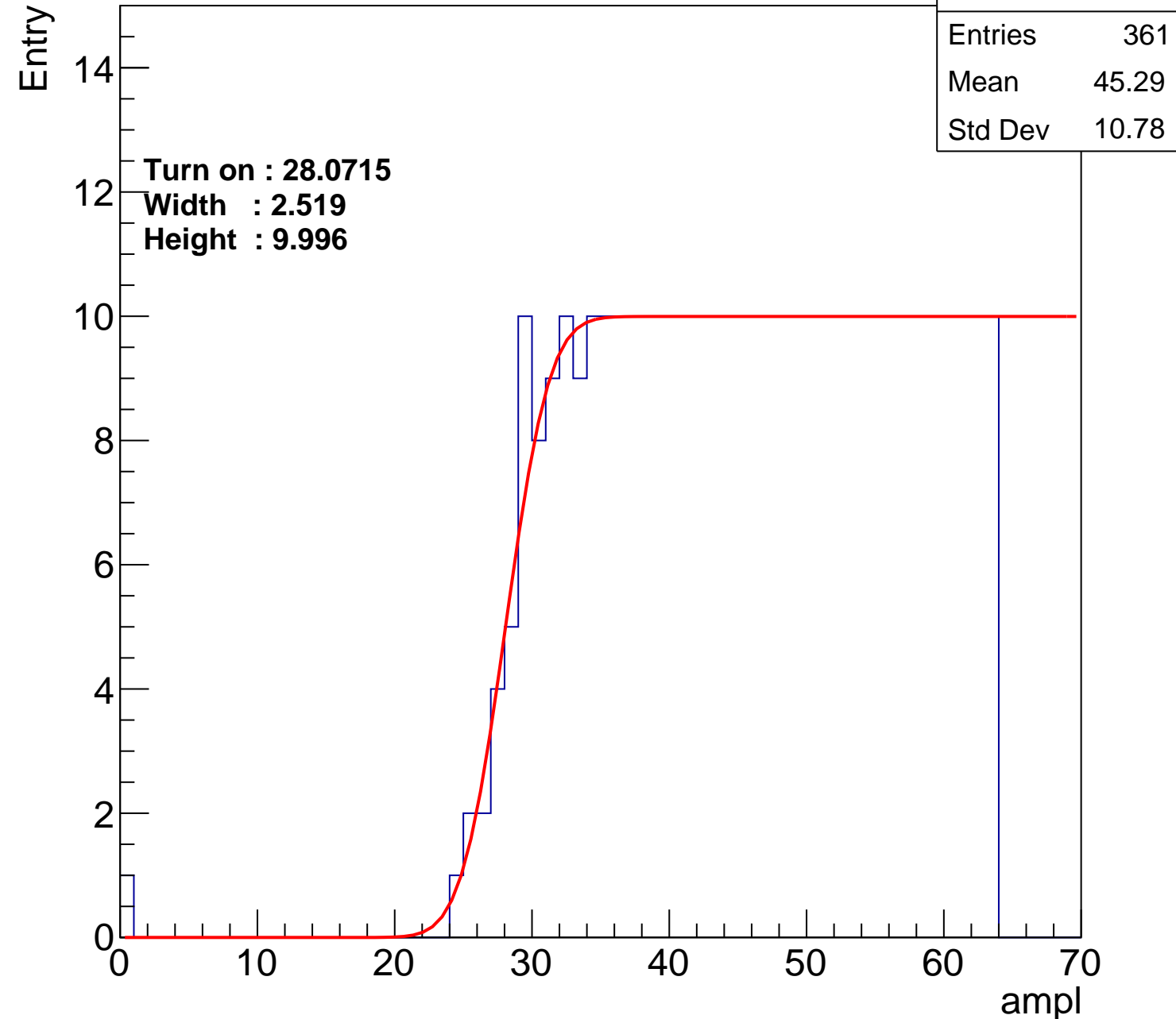
Width : 2.519

Height : 9.996

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L101S, U16-ch15

calib\_packv5\_042523\_0143.root, FC#0, port D2

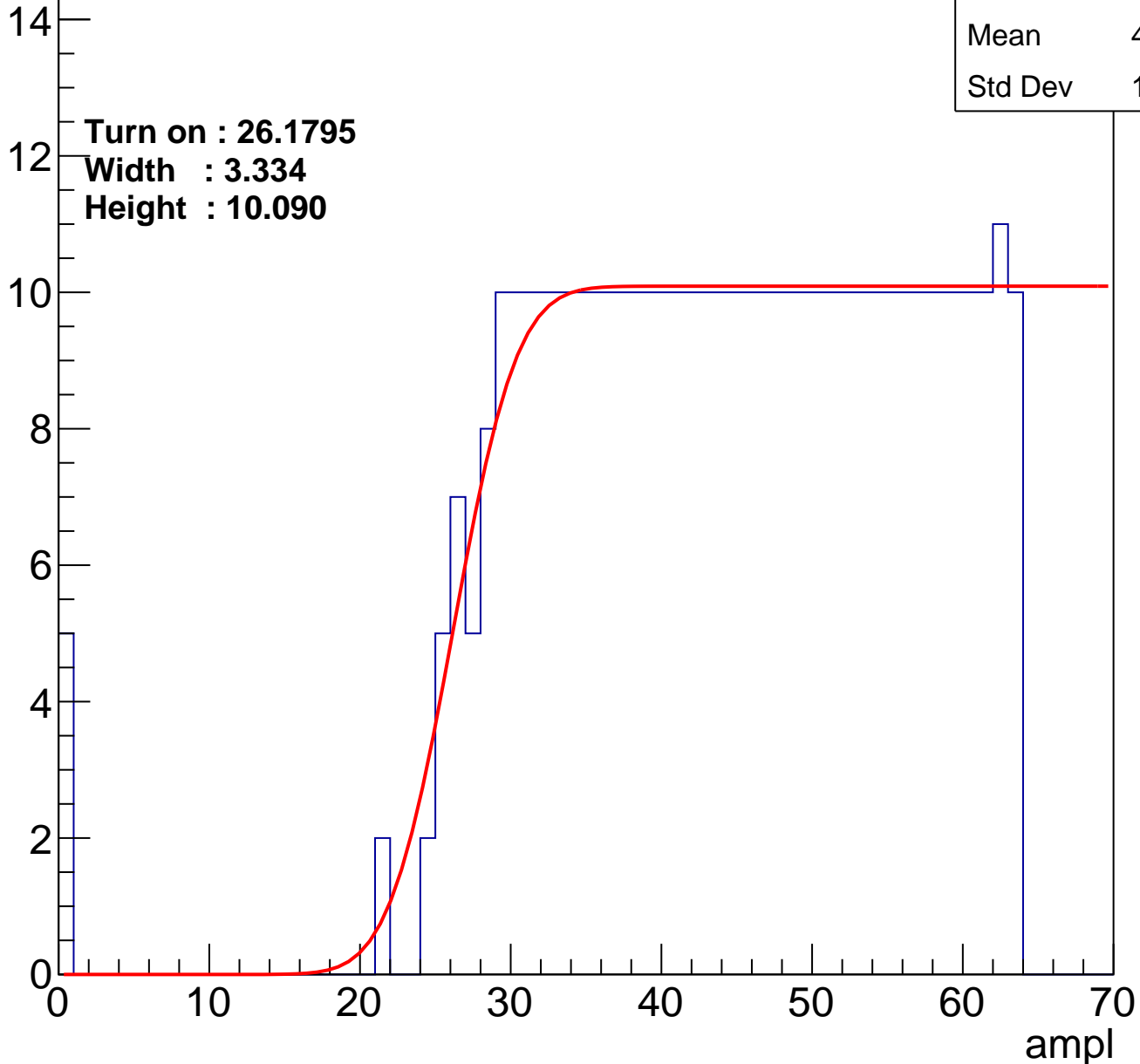
Entries	385
Mean	43.94
Std Dev	12.12

Turn on : 26.1795

Width : 3.334

Height : 10.090

Entry



# B1L101S, U16-ch16

calib\_packv5\_042523\_0143.root, FC#0, port D2

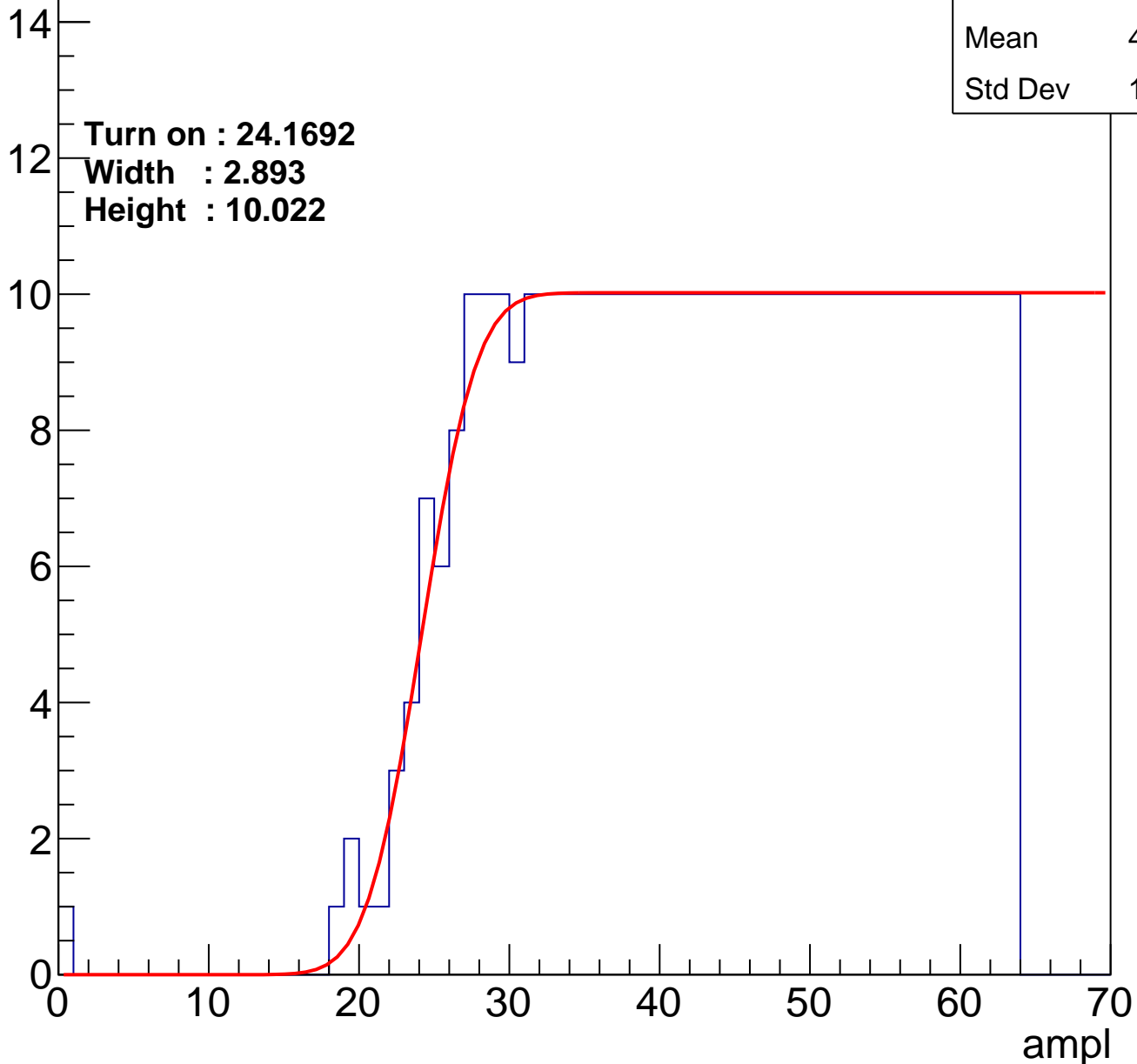
Entries	403
Mean	43.18
Std Dev	11.98

Turn on : 24.1692

Width : 2.893

Height : 10.022

Entry



**calib\_packv5\_042523\_0143.root, FC#0, port D2**

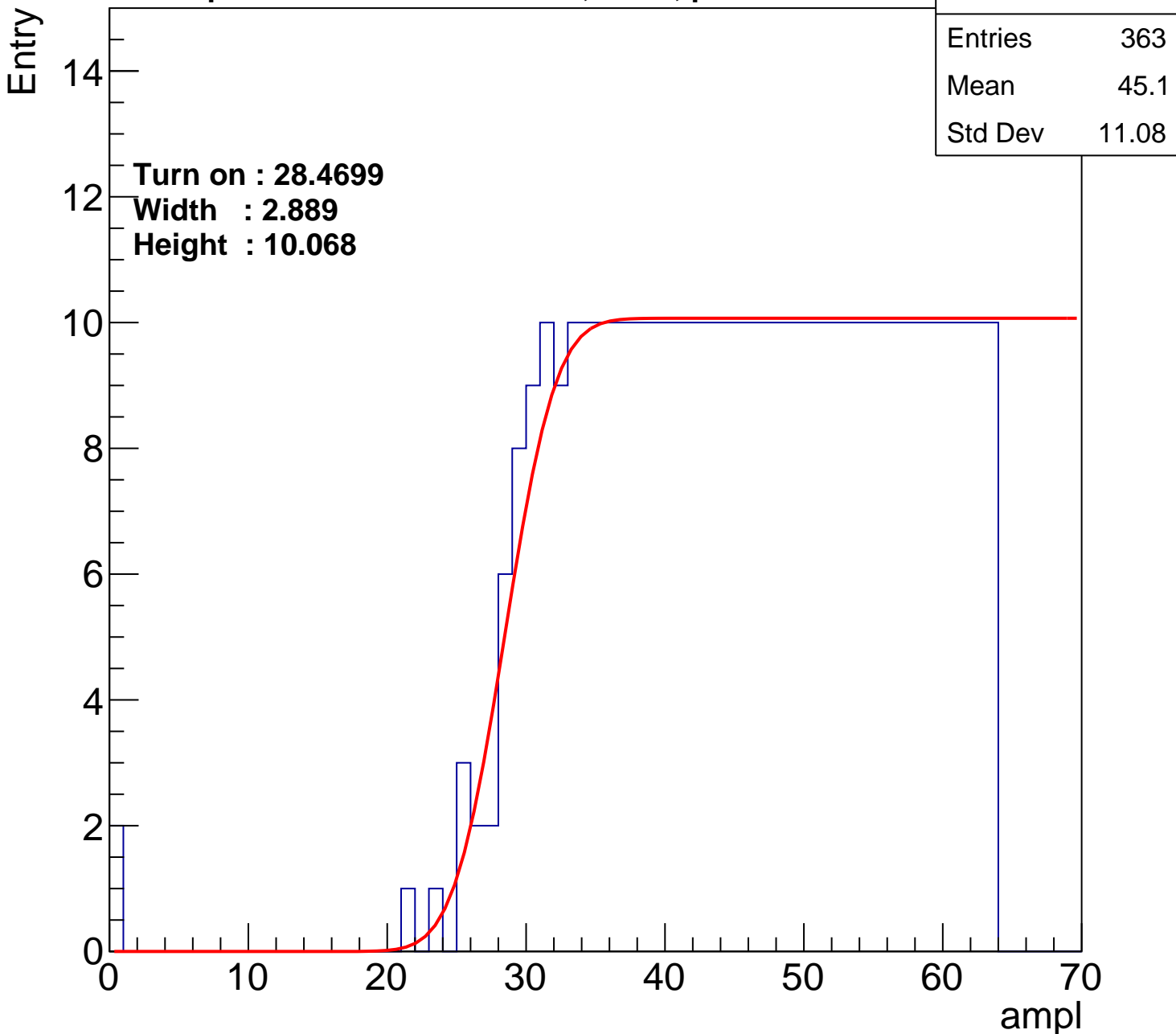
Entries	363
Mean	45.1
Std Dev	11.08

Mean	45.1
------	------

Std Dev	11.08
---------	-------

**Width : 2.889**

**Height : 10.068**



# B1L101S, U16-ch18

calib\_packv5\_042523\_0143.root, FC#0, port D2

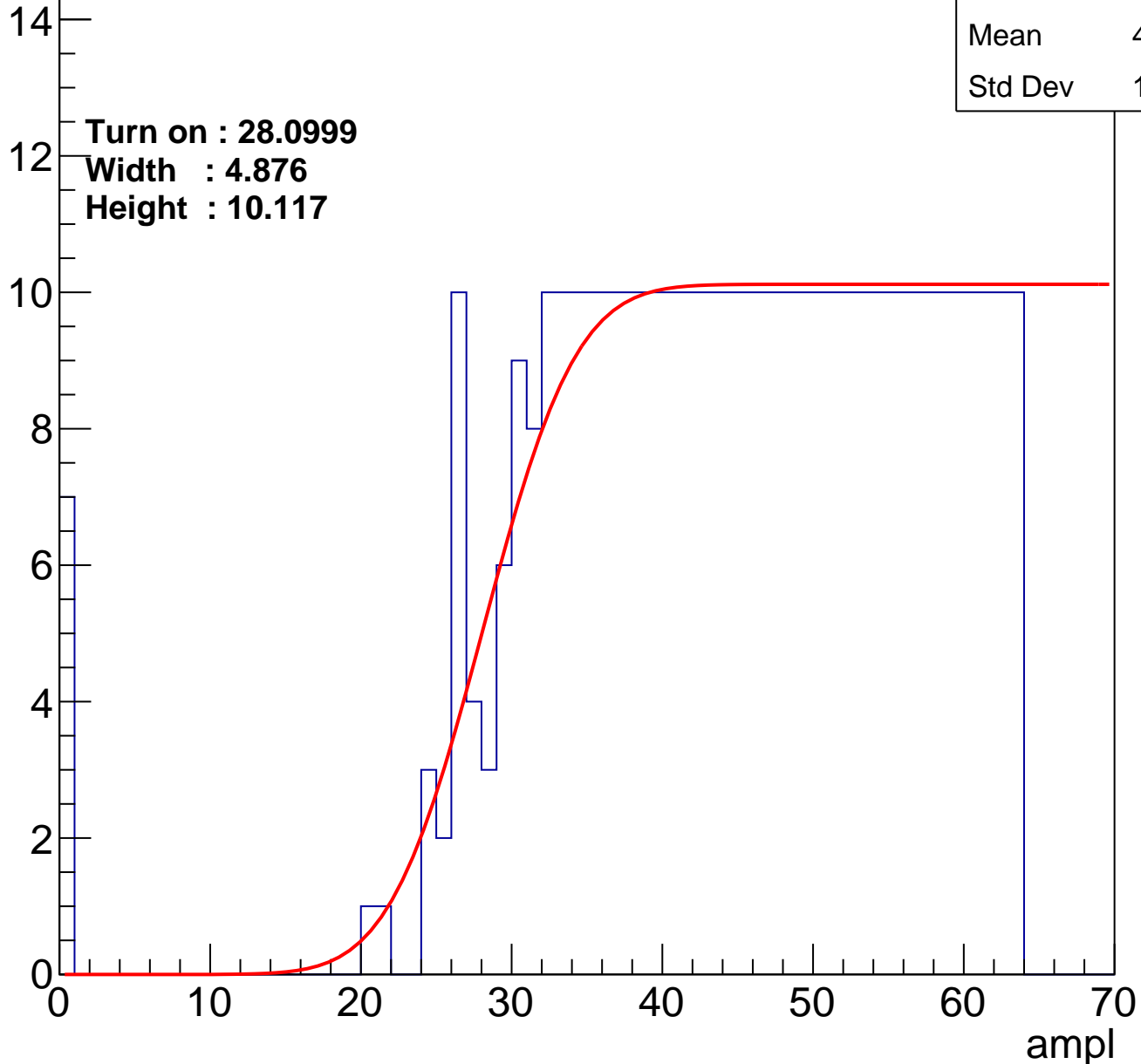
Entries	374
Mean	44.14
Std Dev	12.39

Turn on : 28.0999

Width : 4.876

Height : 10.117

Entry



# B1L101S, U16-ch19

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	371
Mean	44.81
Std Dev	11.04

Turn on : 27.2541

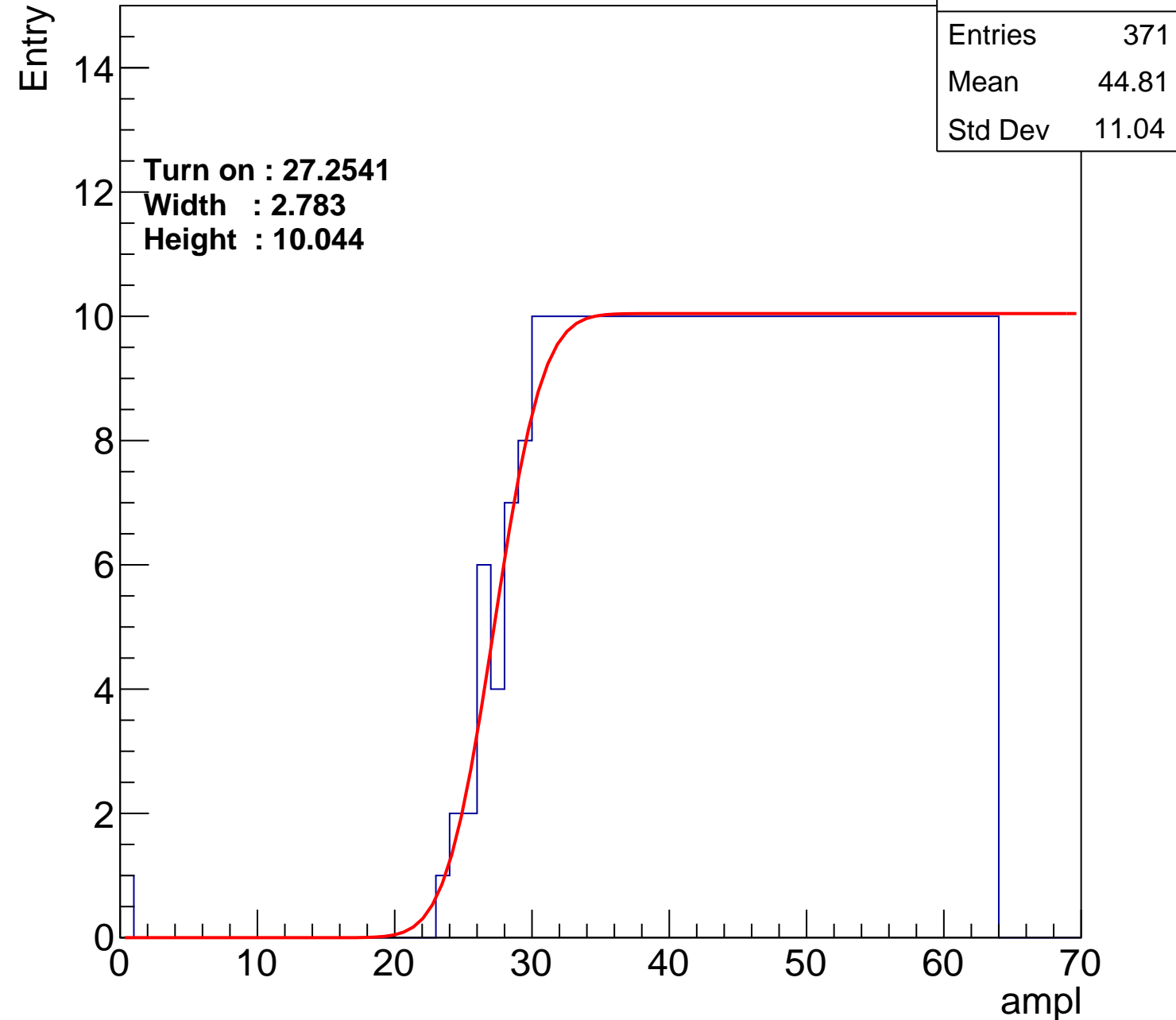
Width : 2.783

Height : 10.044

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U16-ch20

calib\_packv5\_042523\_0143.root, FC#0, port D2

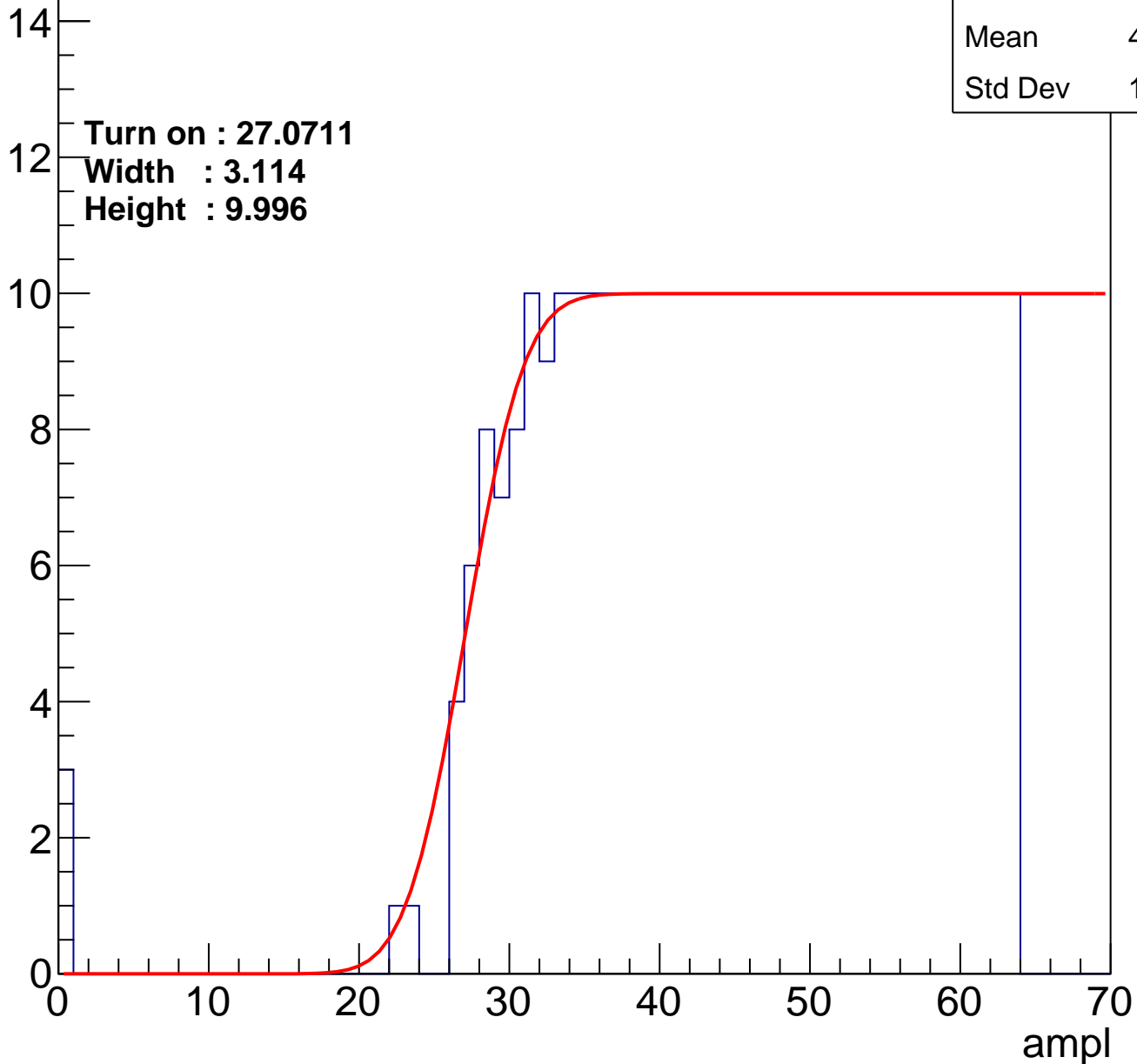
Entries	367
Mean	44.84
Std Dev	11.37

Turn on : 27.0711

Width : 3.114

Height : 9.996

Entry



# B1L101S, U16-ch21

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	386
Mean	43.71
Std Dev	12.34

Turn on : 26.4028

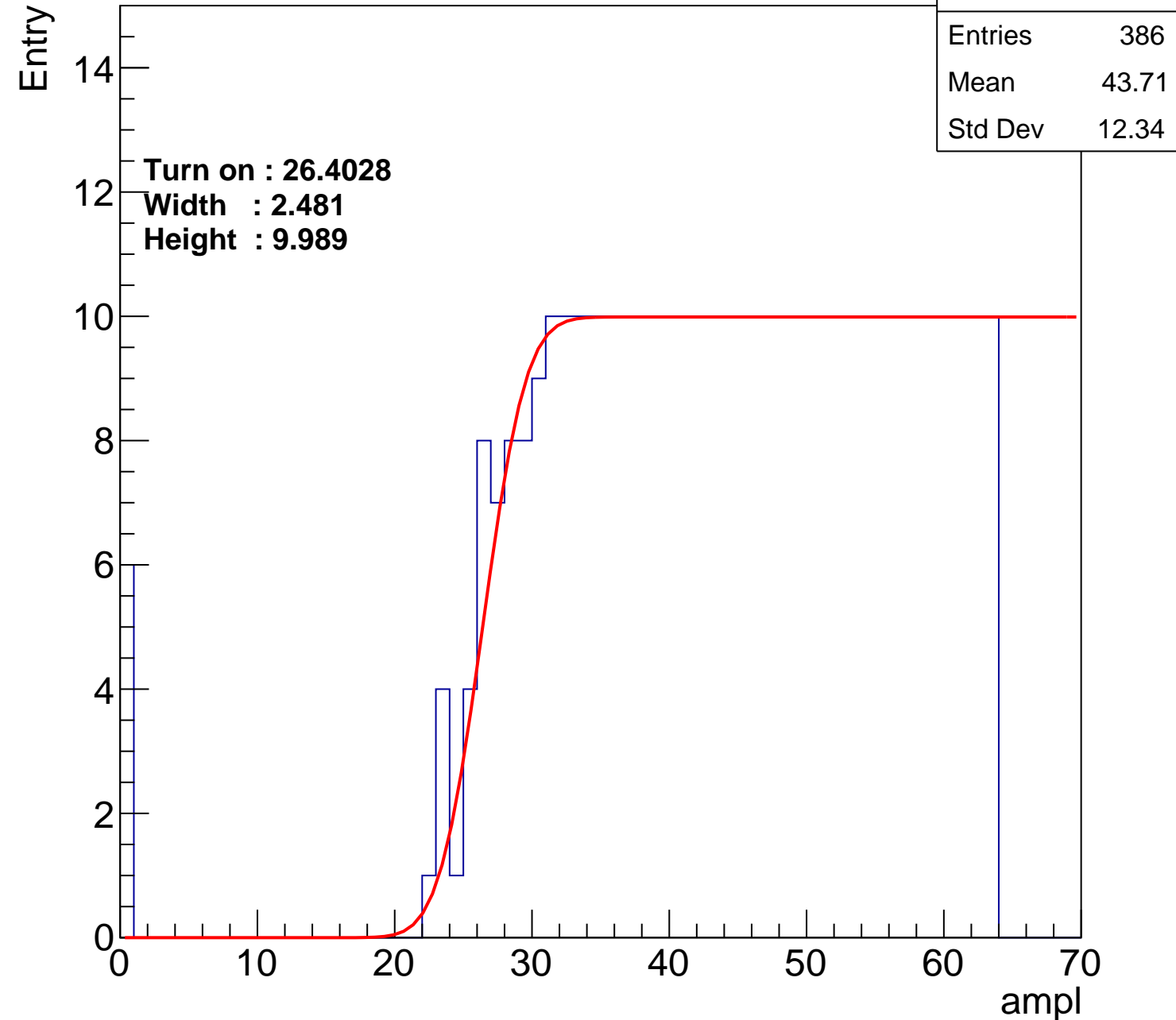
Width : 2.481

Height : 9.989

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U16-ch22

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	382
Mean	44.03
Std Dev	11.92

Turn on : 26.4181

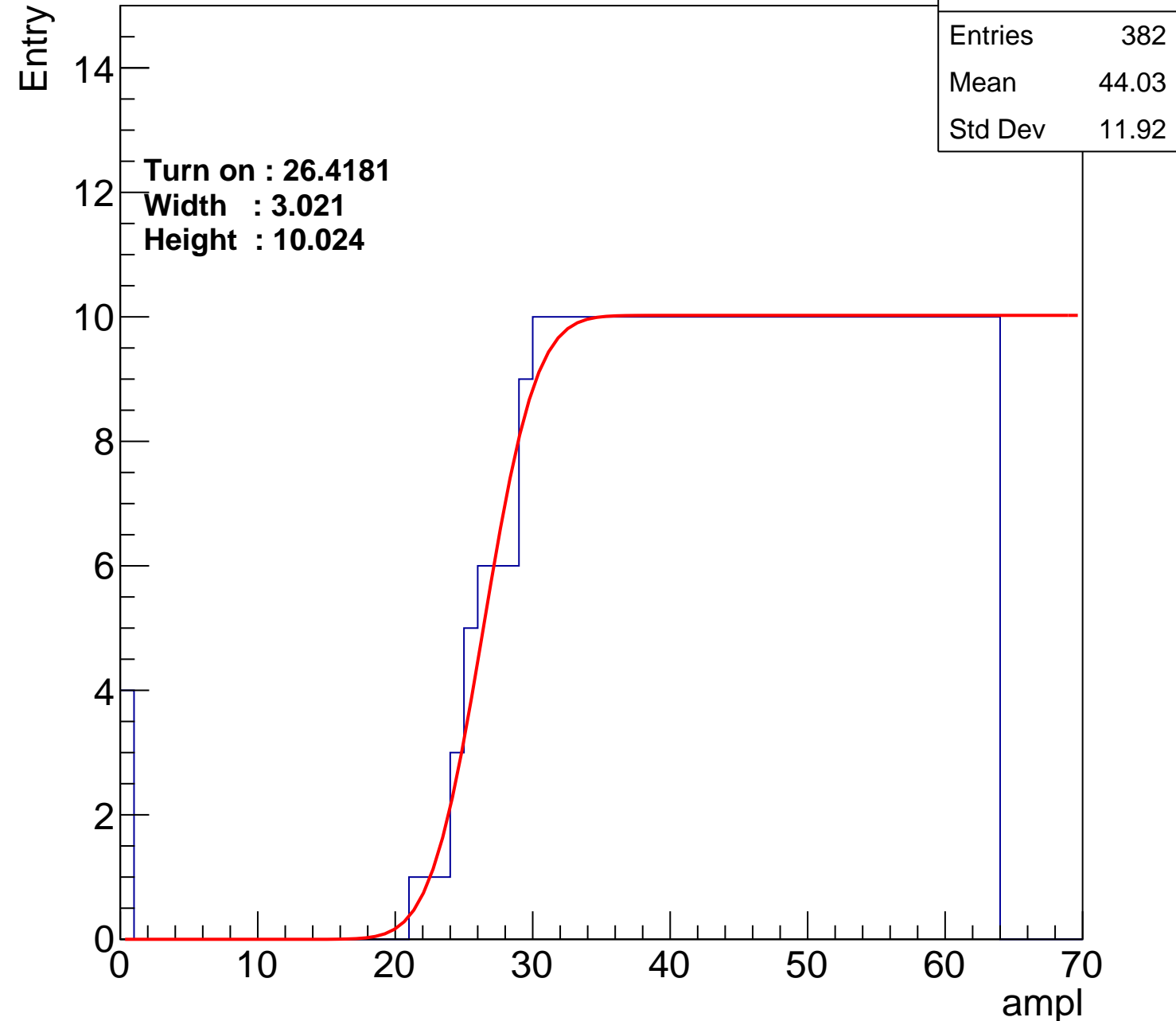
Width : 3.021

Height : 10.024

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L101S, U16-ch23

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	360
Mean	45.01
Std Dev	11.66

Turn on : 28.6211

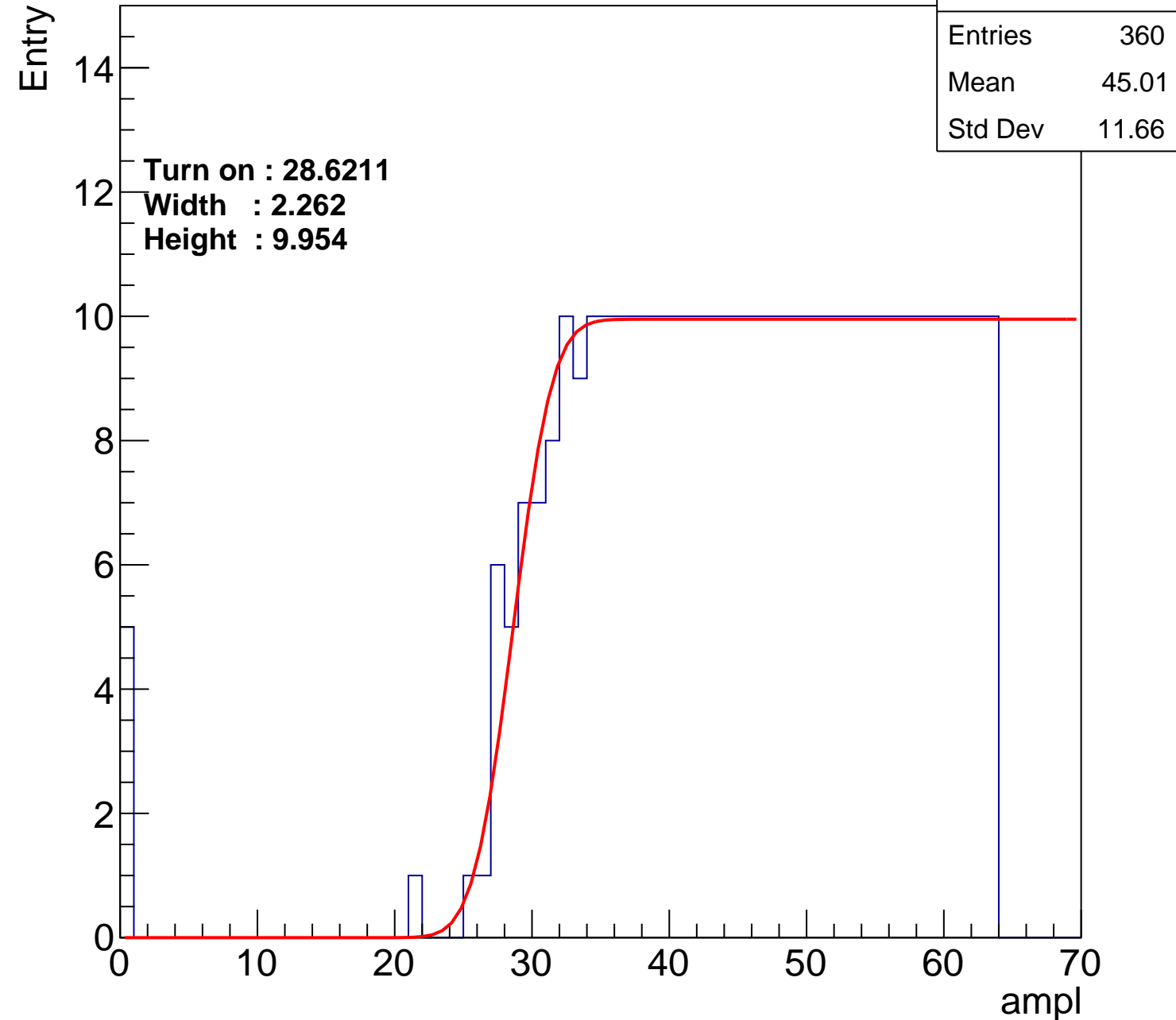
Width : 2.262

Height : 9.954

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U16-ch24

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	374
Mean	44.39
Std Dev	11.79

**Turn on : 27.0289**

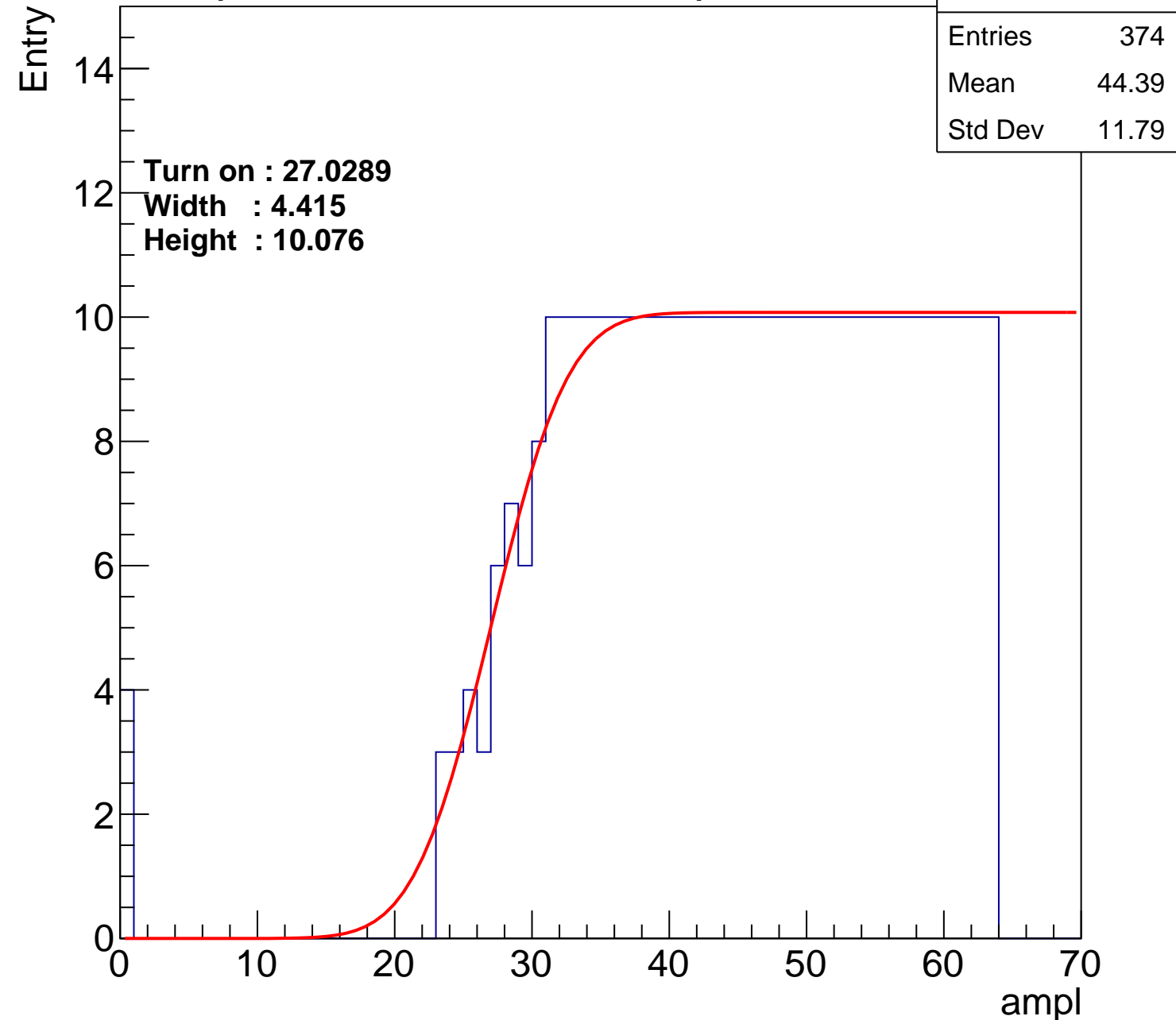
**Width : 4.415**

**Height : 10.076**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U16-ch25

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	356
Mean	45.04
Std Dev	11.99

Turn on : 29.2178

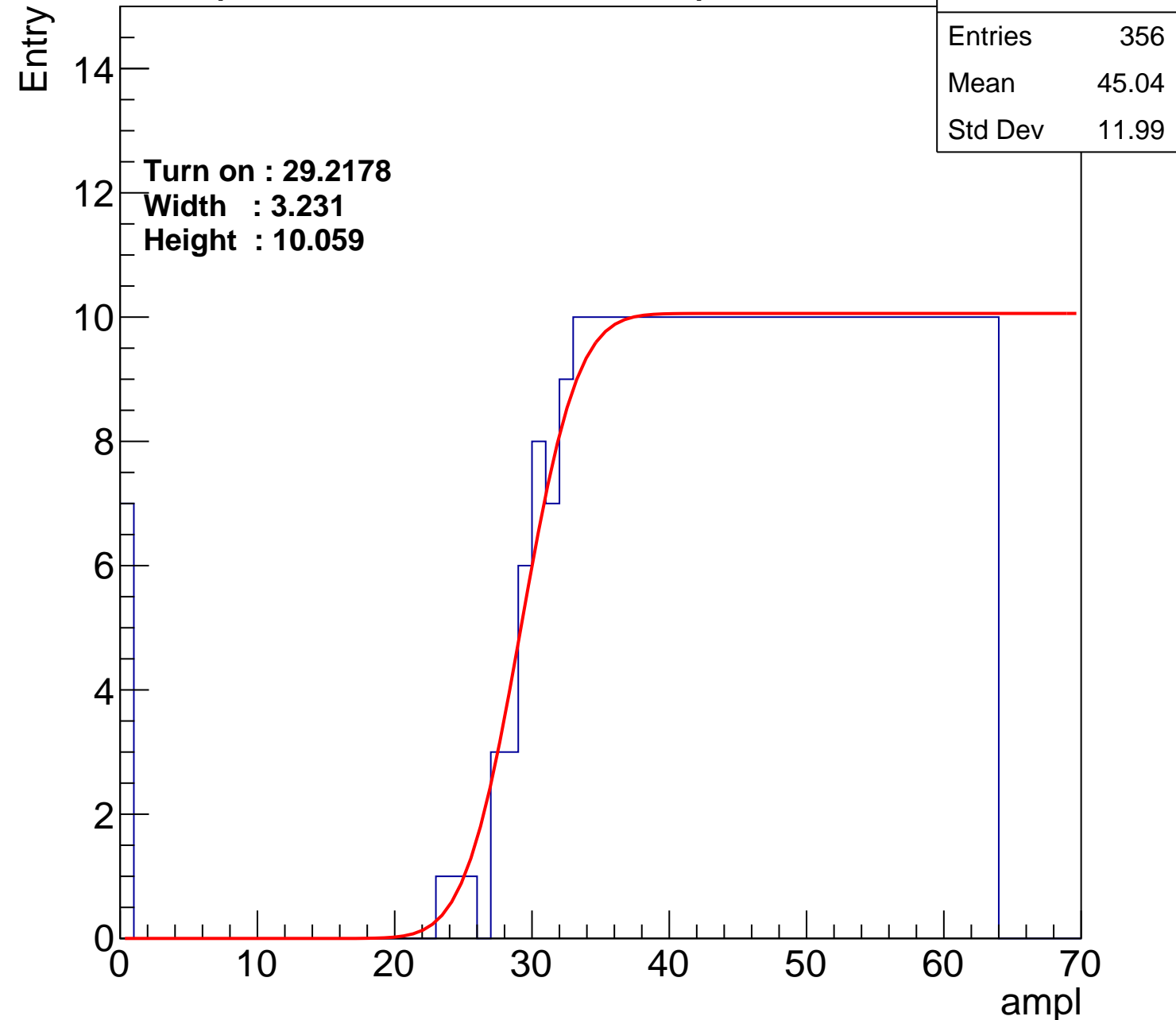
Width : 3.231

Height : 10.059

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U16-ch26

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	373
Mean	44.48
Std Dev	11.62

Turn on : 27.1307

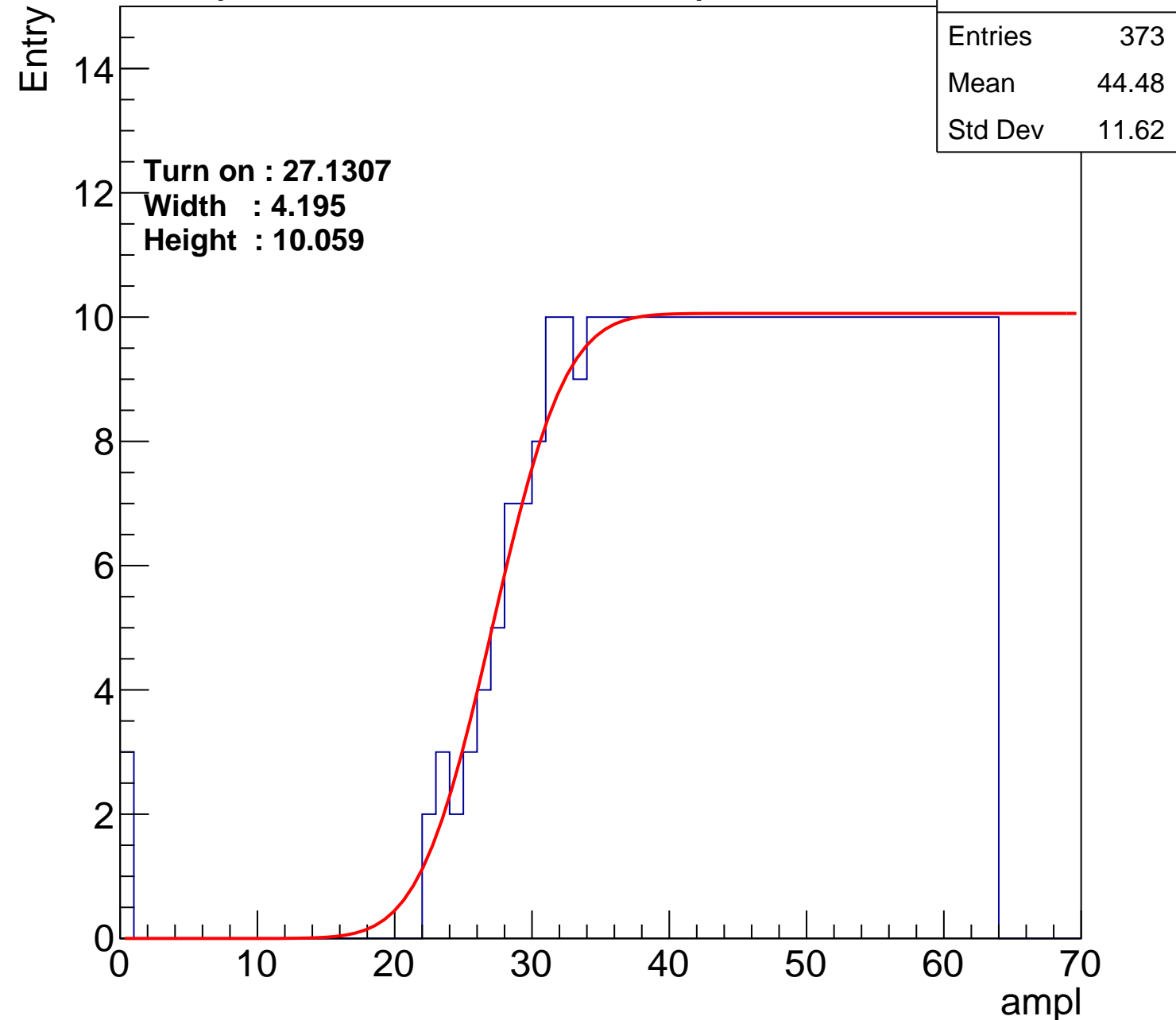
Width : 4.195

Height : 10.059

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U16-ch27

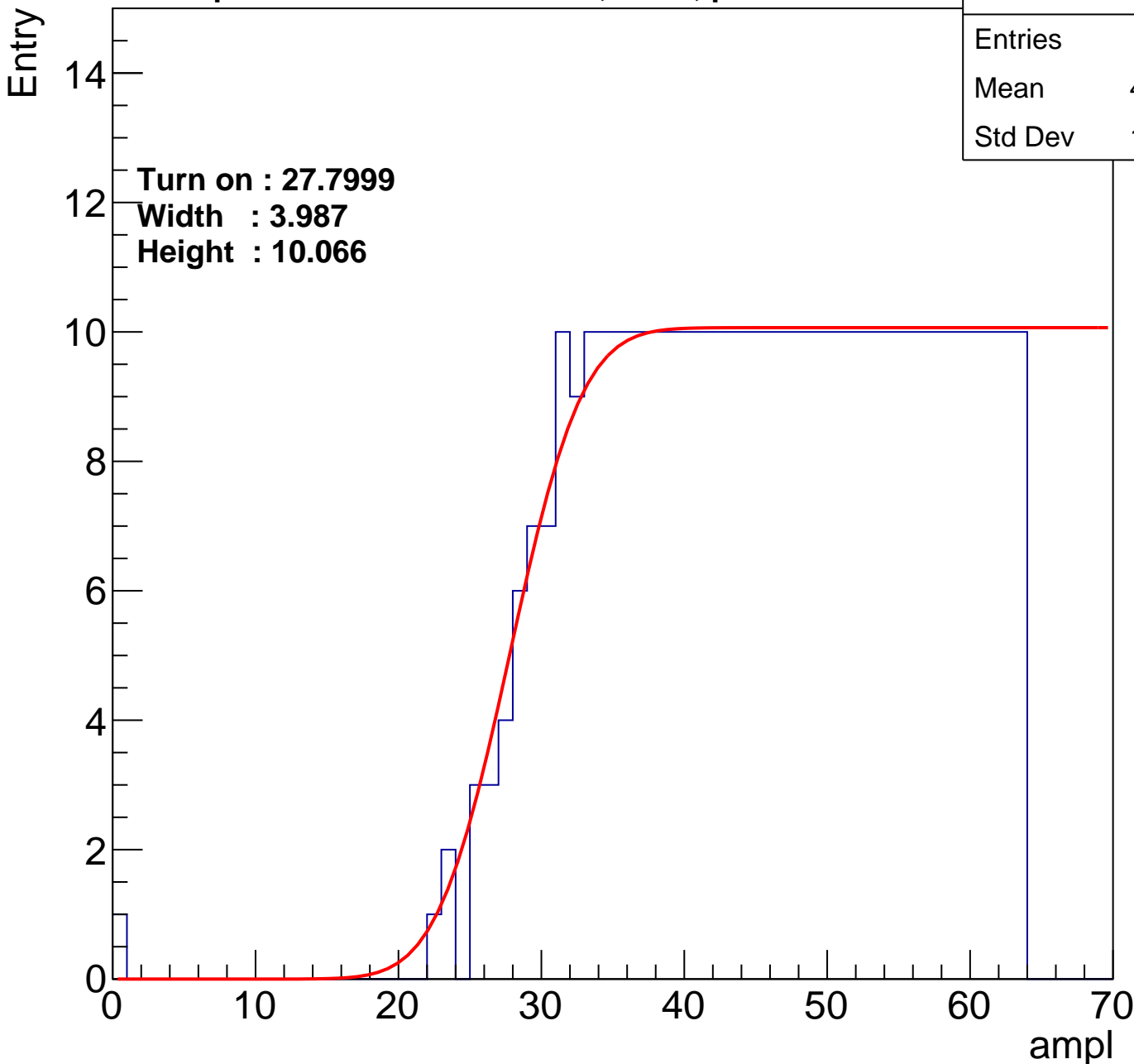
**calib\_packv5\_042523\_0143.root, FC#0, port D2**

Entries	363
Mean	45.15
Std Dev	10.92

**Turn on : 27.7999**

**Width : 3.987**

**Height : 10.066**



# B1L101S, U16-ch28

calib\_packv5\_042523\_0143.root, FC#0, port D2

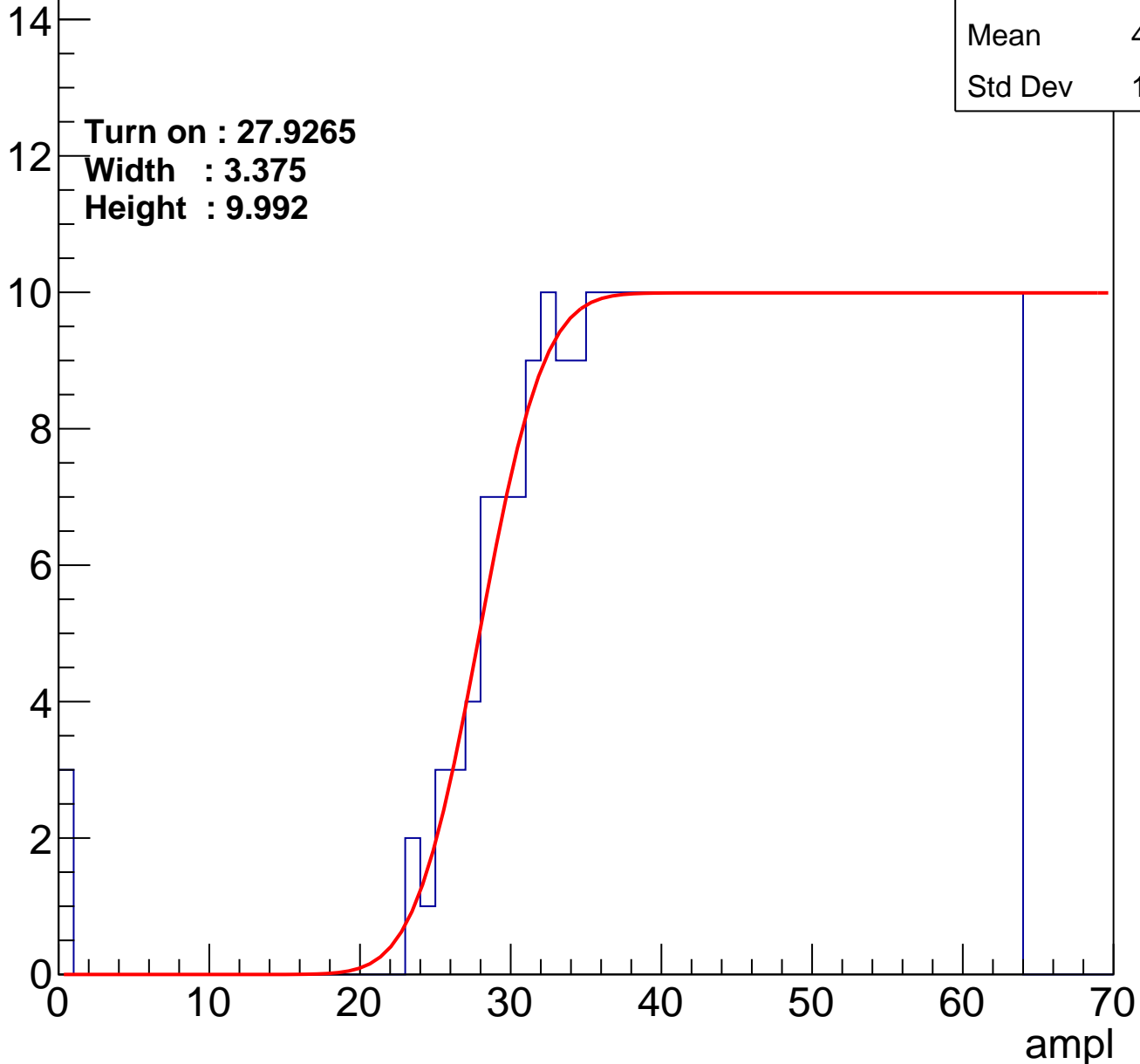
Entries	364
Mean	44.92
Std Dev	11.39

Turn on : 27.9265

Width : 3.375

Height : 9.992

Entry



# B1L101S, U16-ch29

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	369
Mean	44.68
Std Dev	11.59

Turn on : 24.7593

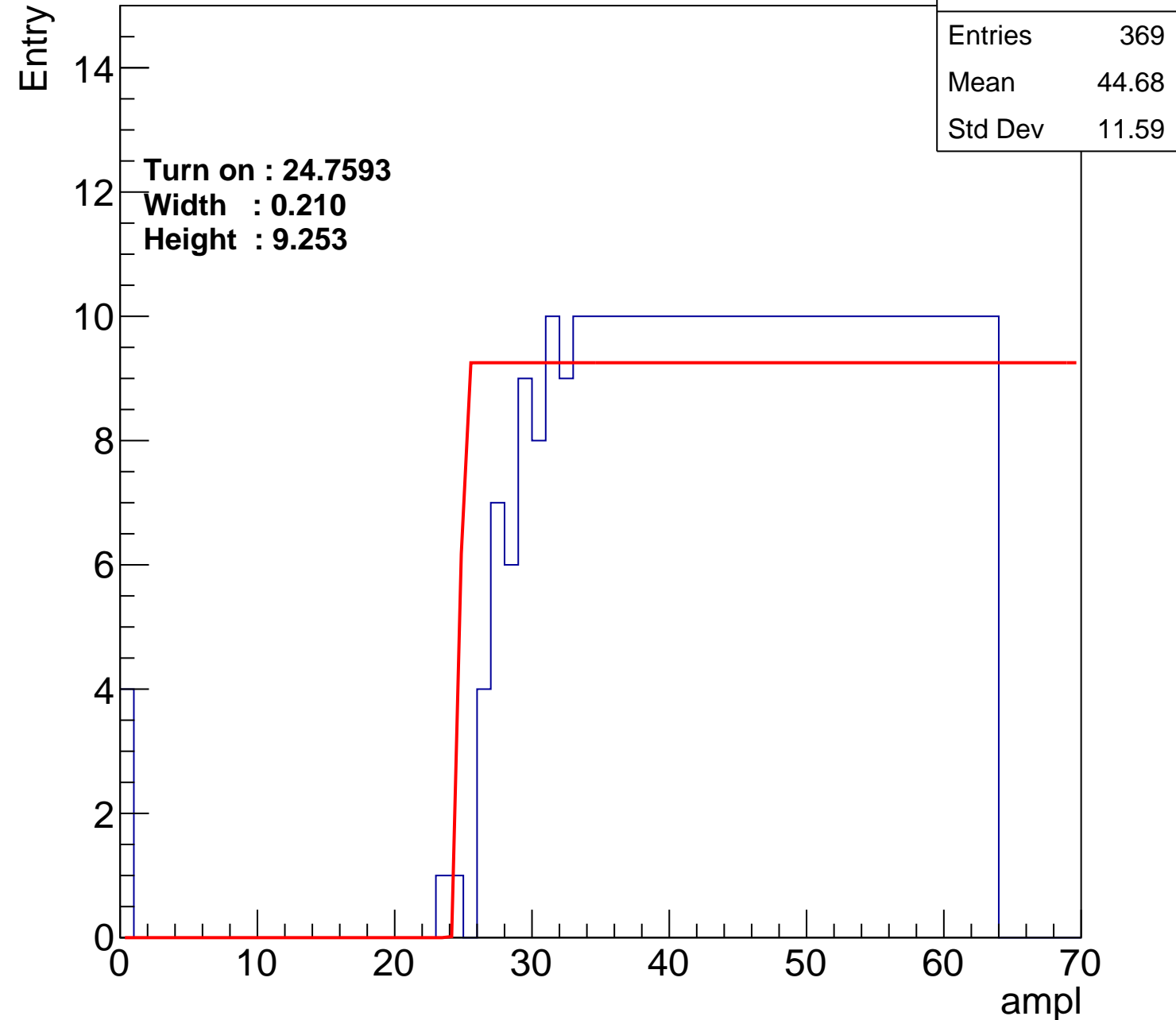
Width : 0.210

Height : 9.253

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U16-ch30

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	371
Mean	44.76
Std Dev	11.11

**Turn on : 26.9607**

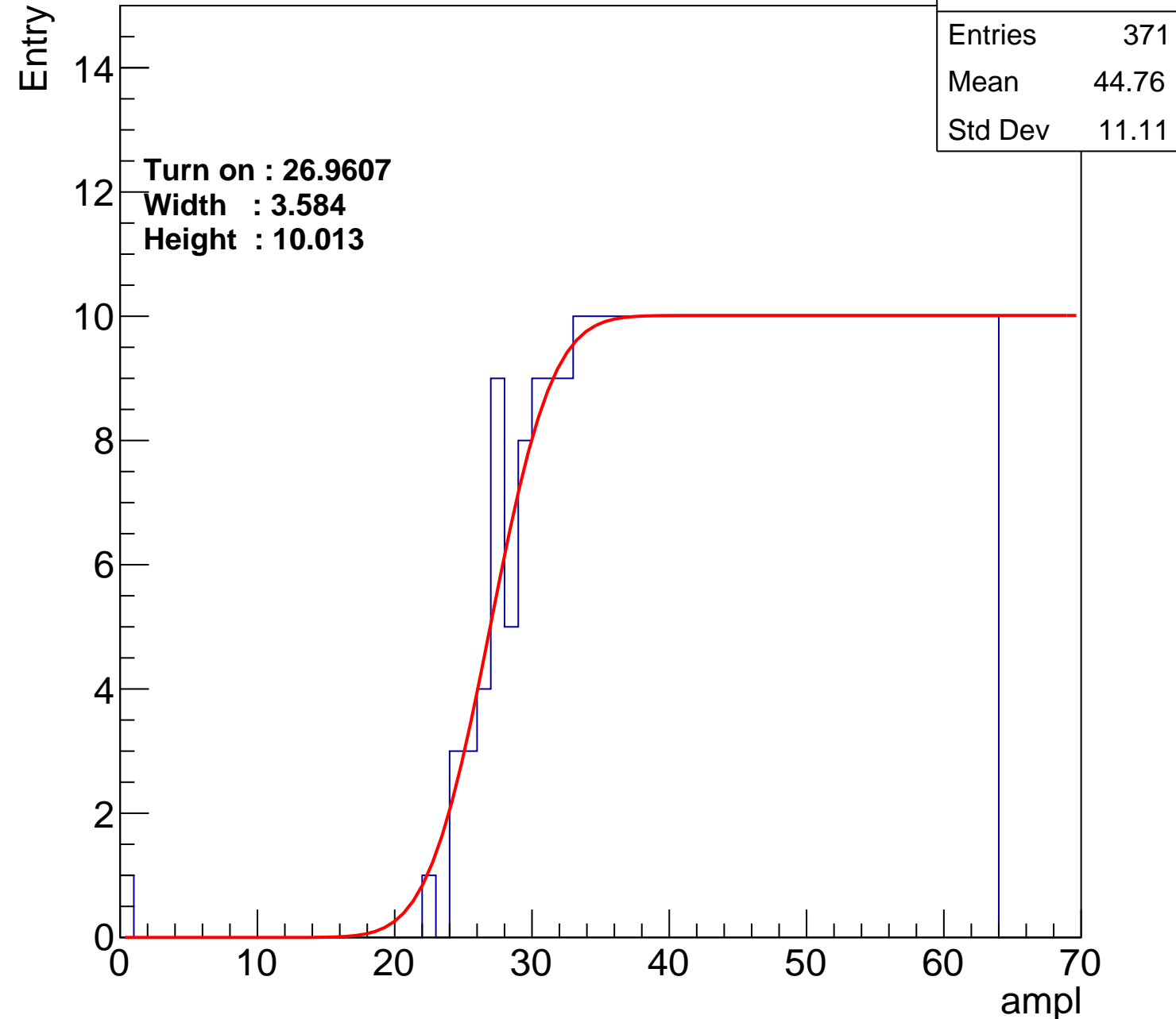
**Width : 3.584**

**Height : 10.013**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L101S, U16-ch31

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	371
Mean	44.71
Std Dev	11.28

Turn on : 26.7234

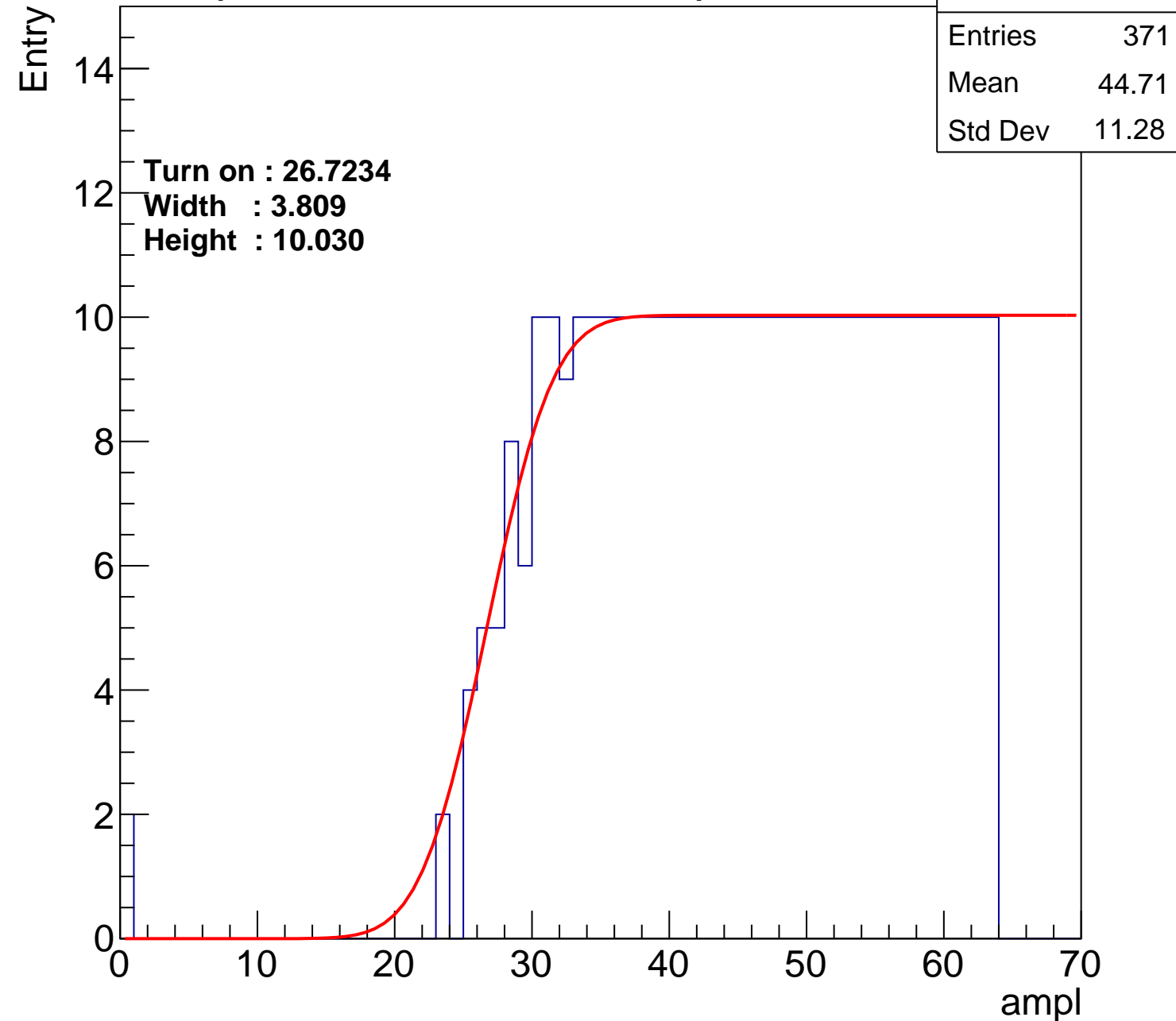
Width : 3.809

Height : 10.030

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U16-ch32

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	393
Mean	43.3
Std Dev	12.59

Turn on : 26.3369

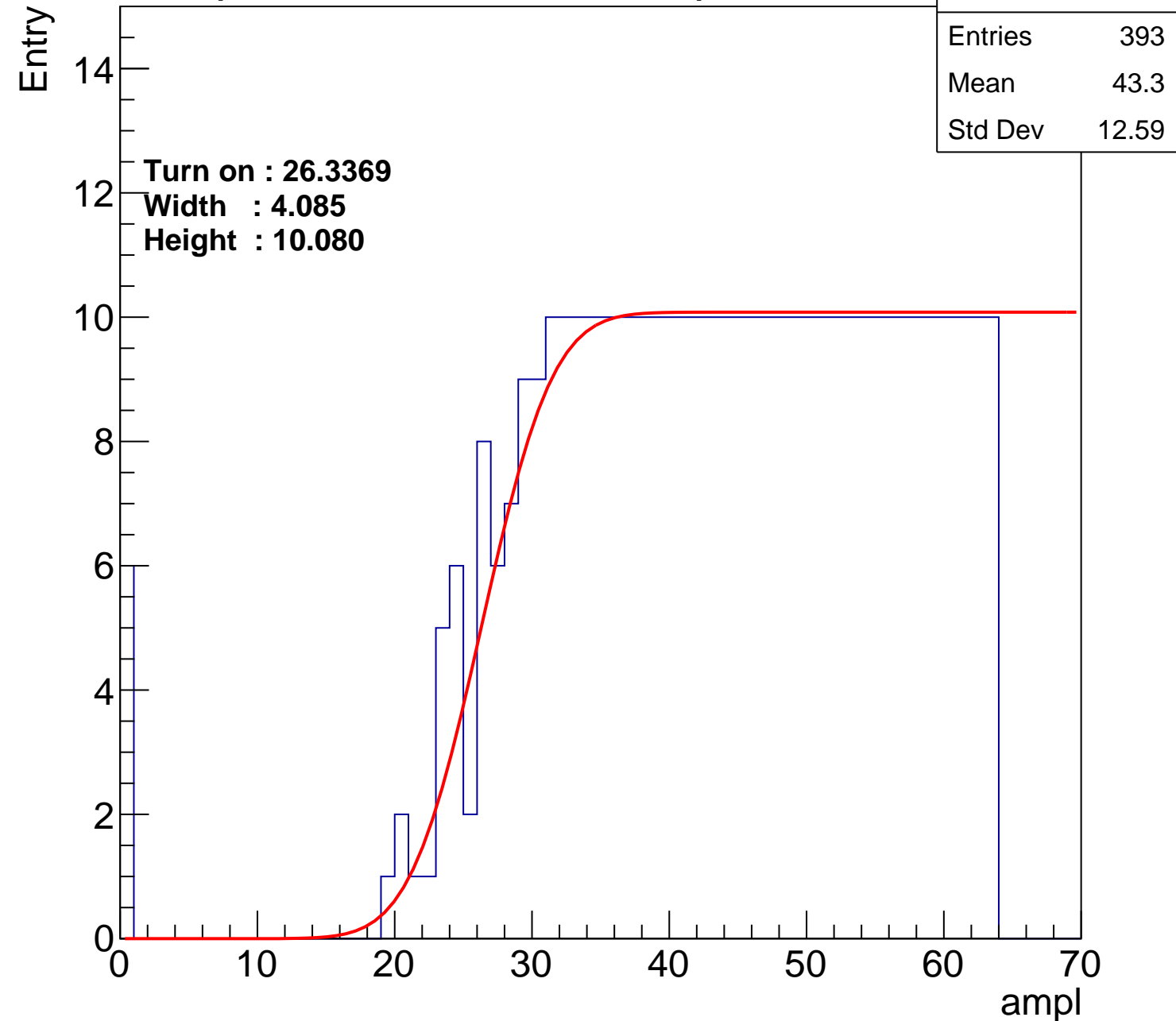
Width : 4.085

Height : 10.080

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U16-ch33

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	369
Mean	44.73
Std Dev	11.43

Turn on : 28.0831

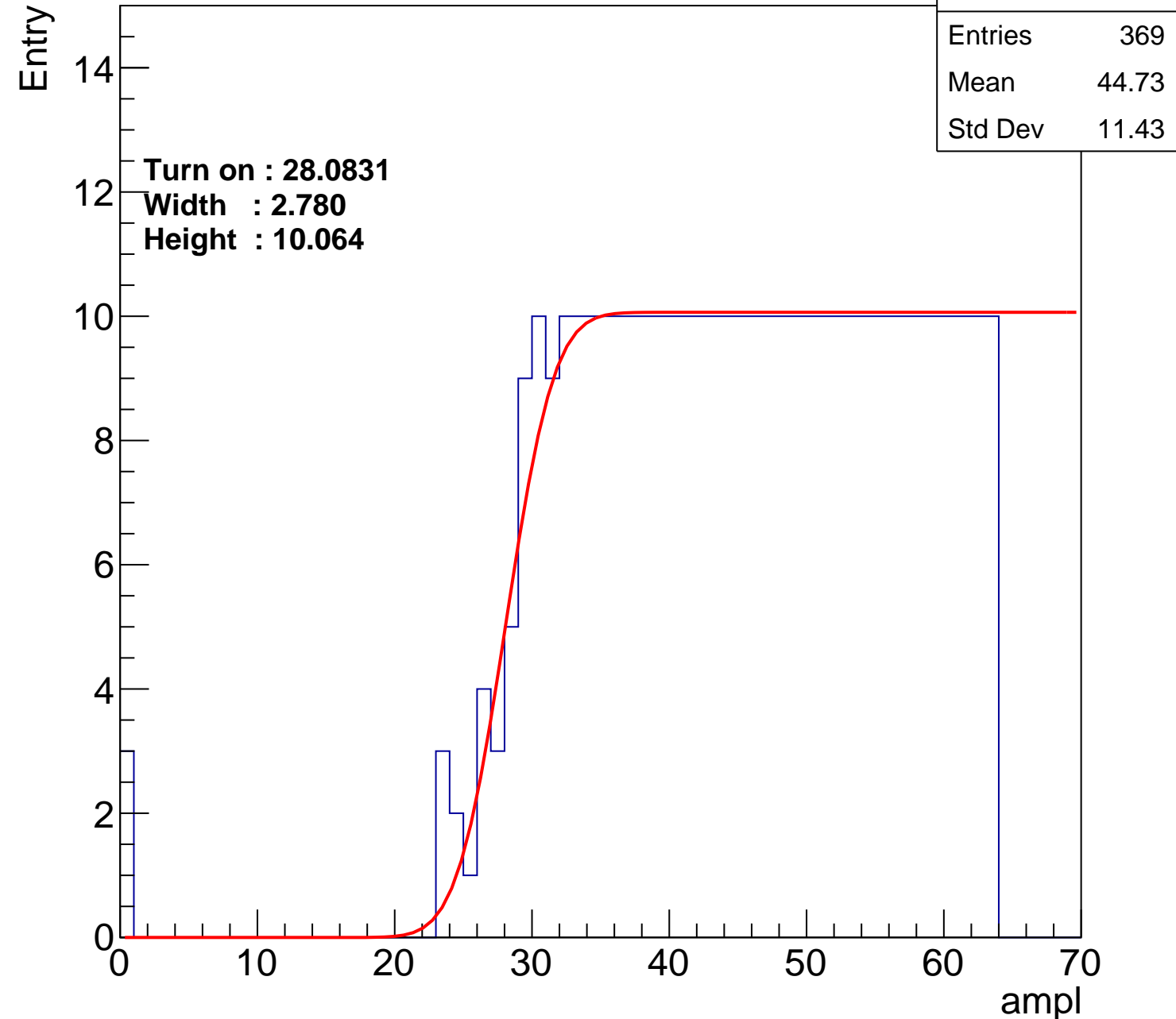
Width : 2.780

Height : 10.064

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U16-ch34

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	378
Mean	44.39
Std Dev	11.34

Turn on : 26.8749

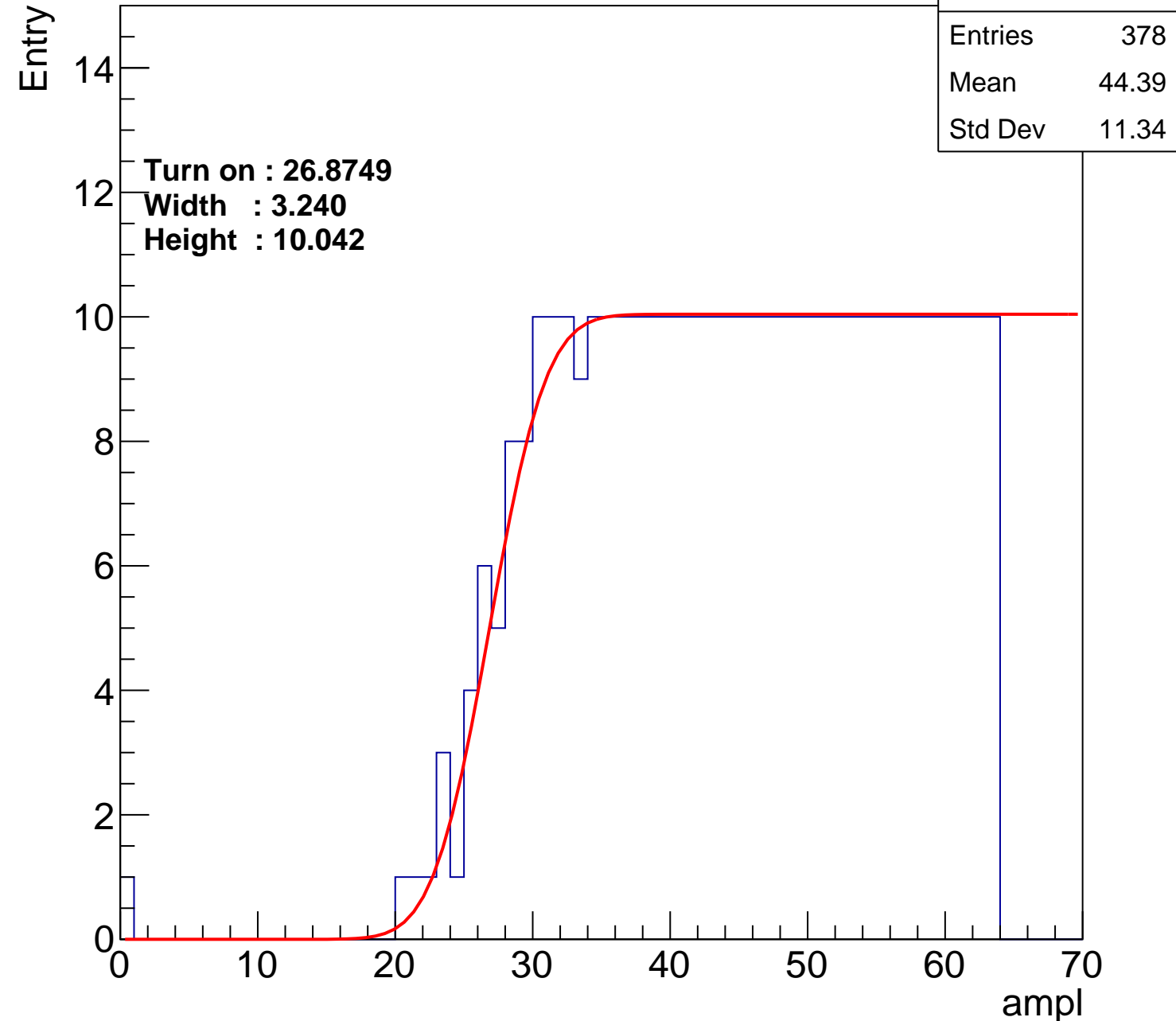
Width : 3.240

Height : 10.042

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U16-ch35

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	364
Mean	44.8
Std Dev	11.76

Turn on : 28.7831

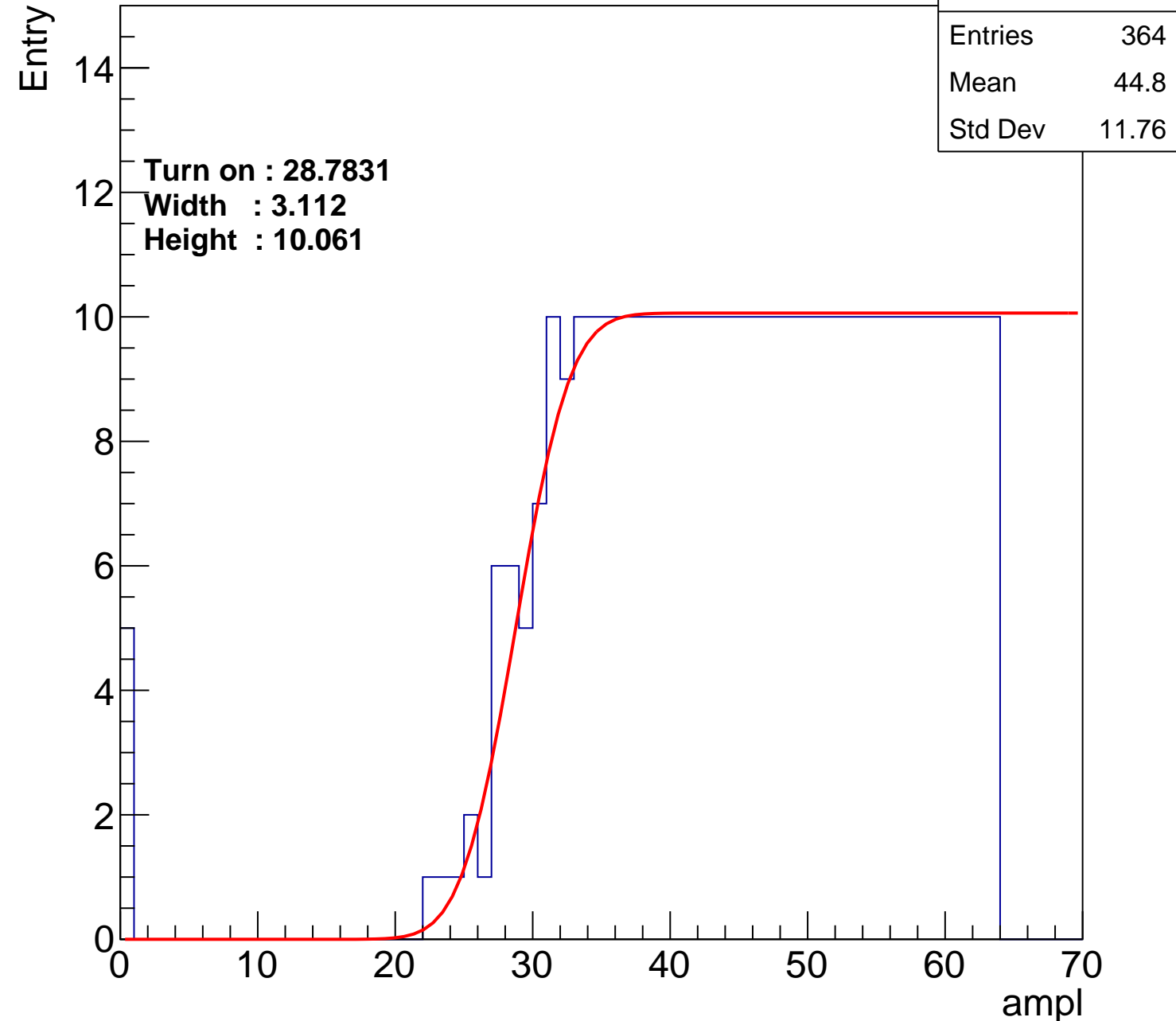
Width : 3.112

Height : 10.061

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U16-ch36

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	361
Mean	45.12
Std Dev	11.25

**Turn on : 28.6230**

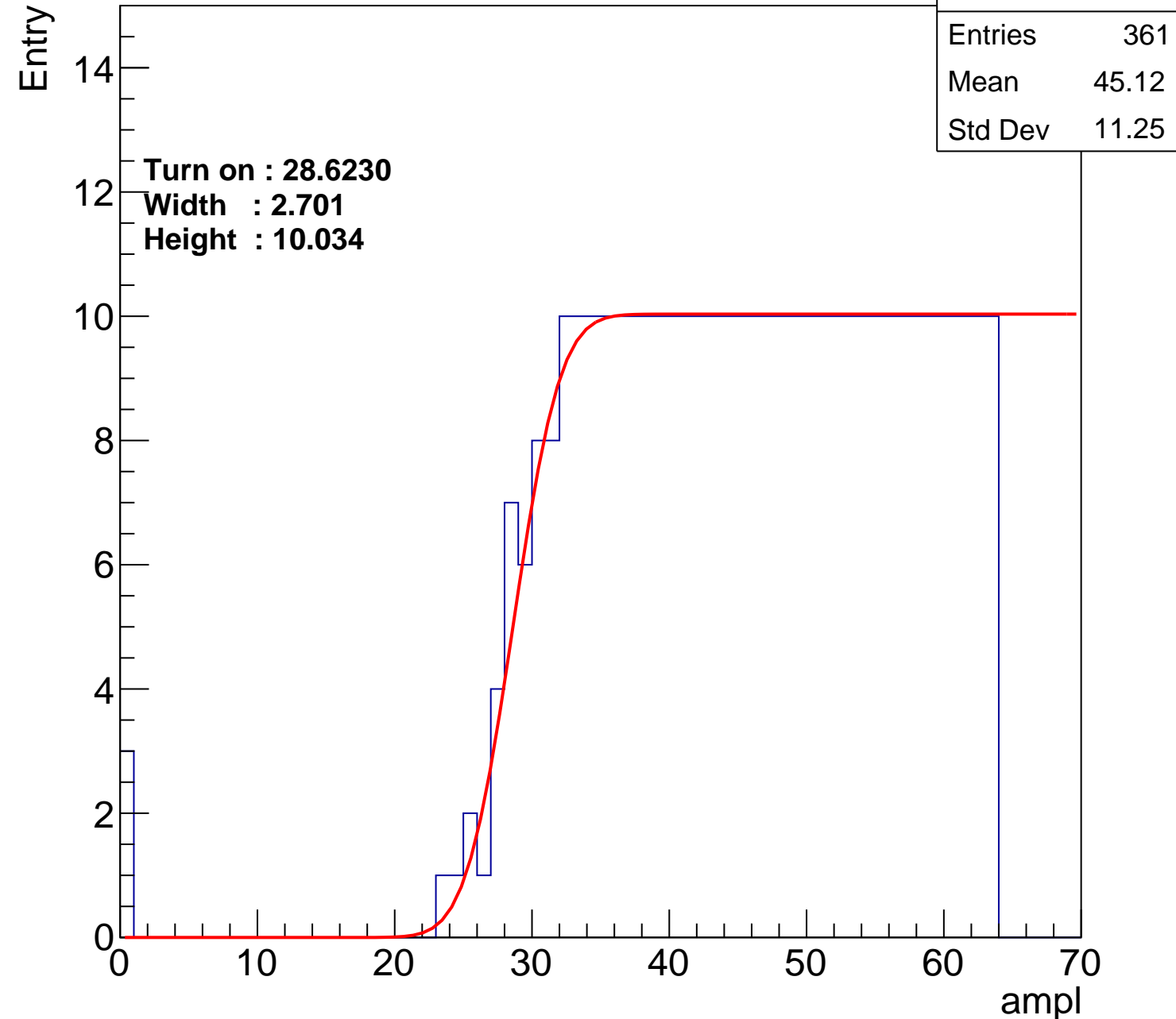
**Width : 2.701**

**Height : 10.034**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U16-ch37

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	348
Mean	45.75
Std Dev	10.95

**Turn on : 29.7743**

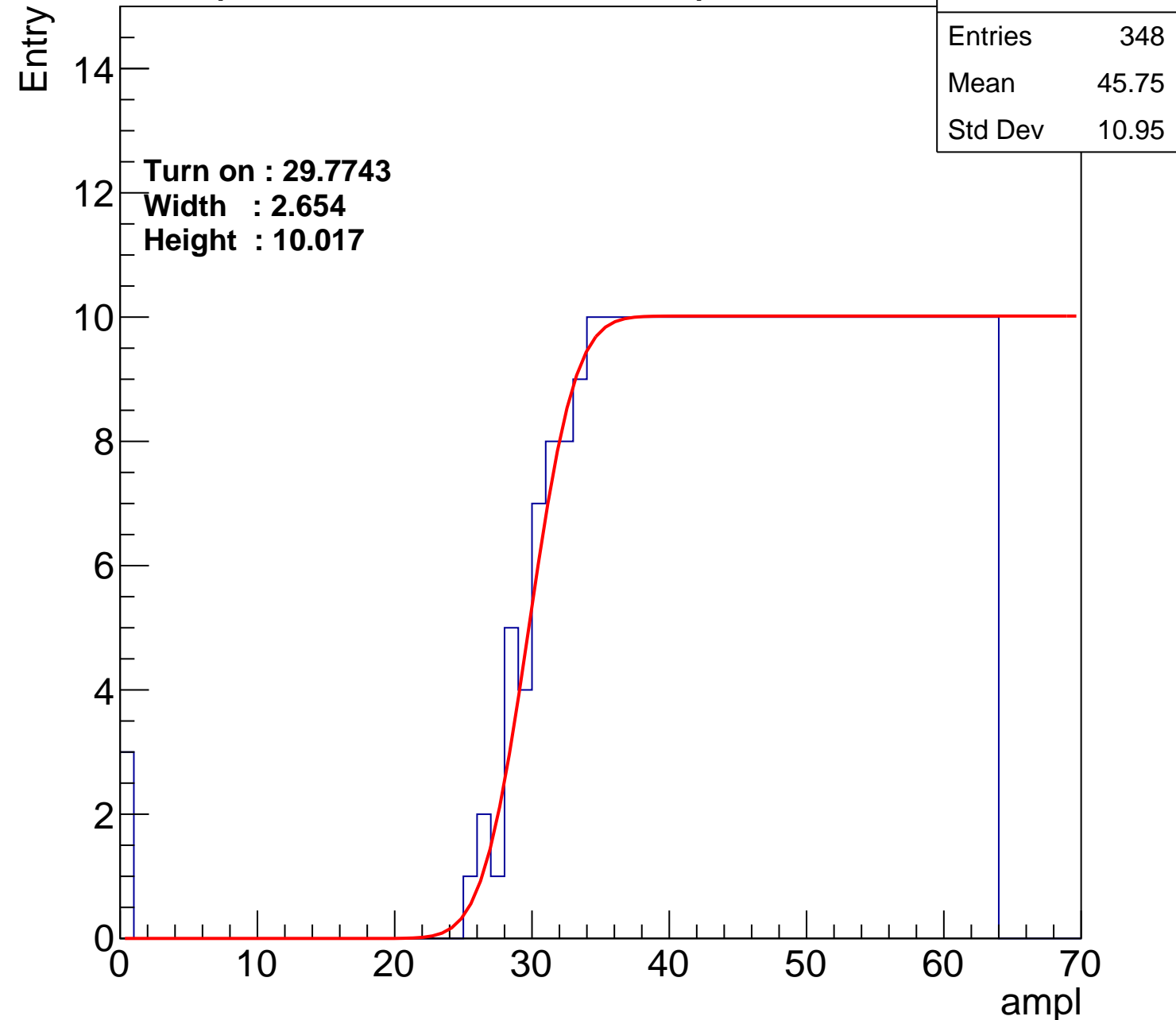
**Width : 2.654**

**Height : 10.017**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U16-ch38

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	394
Mean	43.52
Std Dev	12.03

Turn on : 25.5602

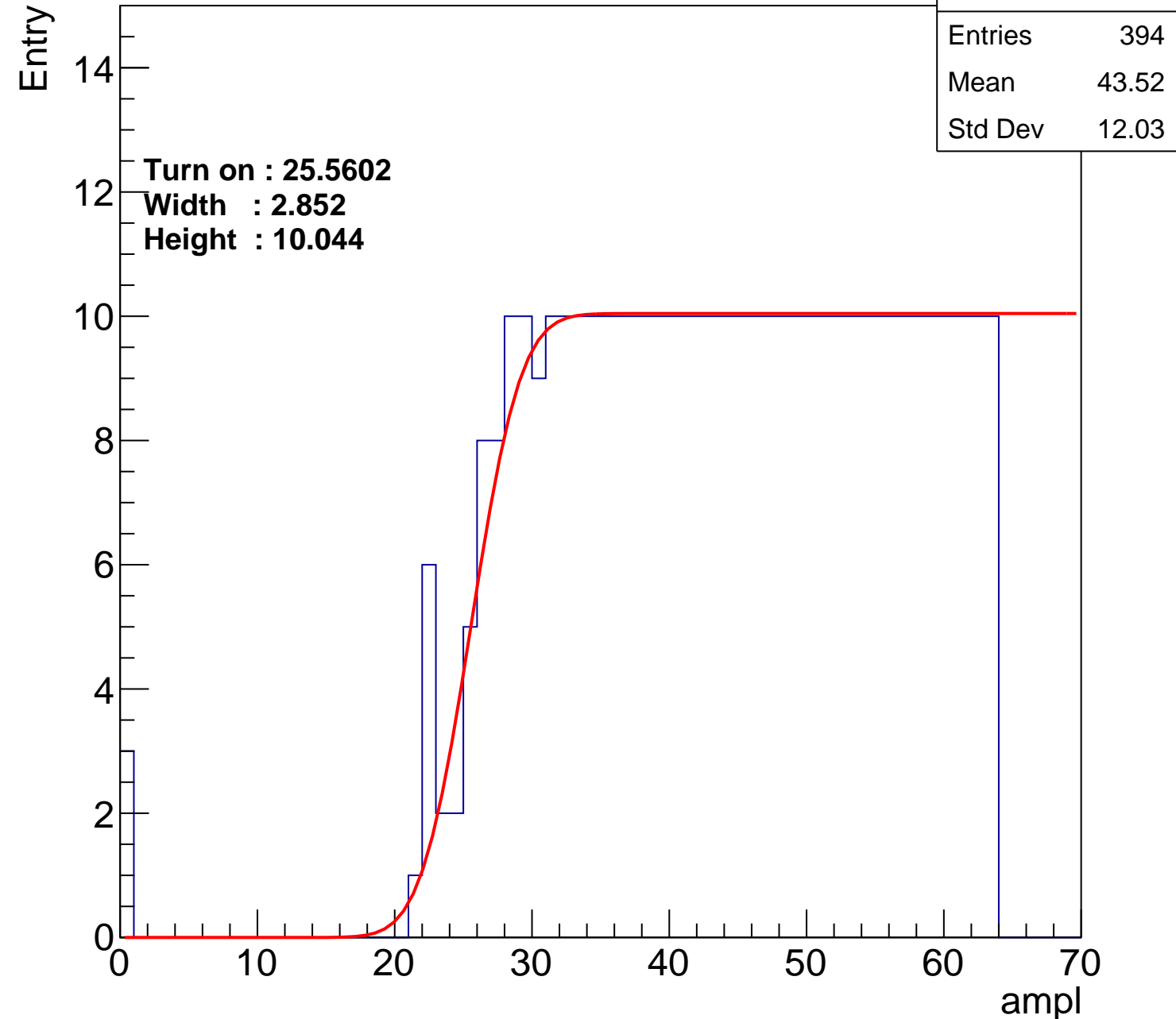
Width : 2.852

Height : 10.044

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L101S, U16-ch39

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	371
Mean	44.71
Std Dev	11.27

Turn on : 27.1891

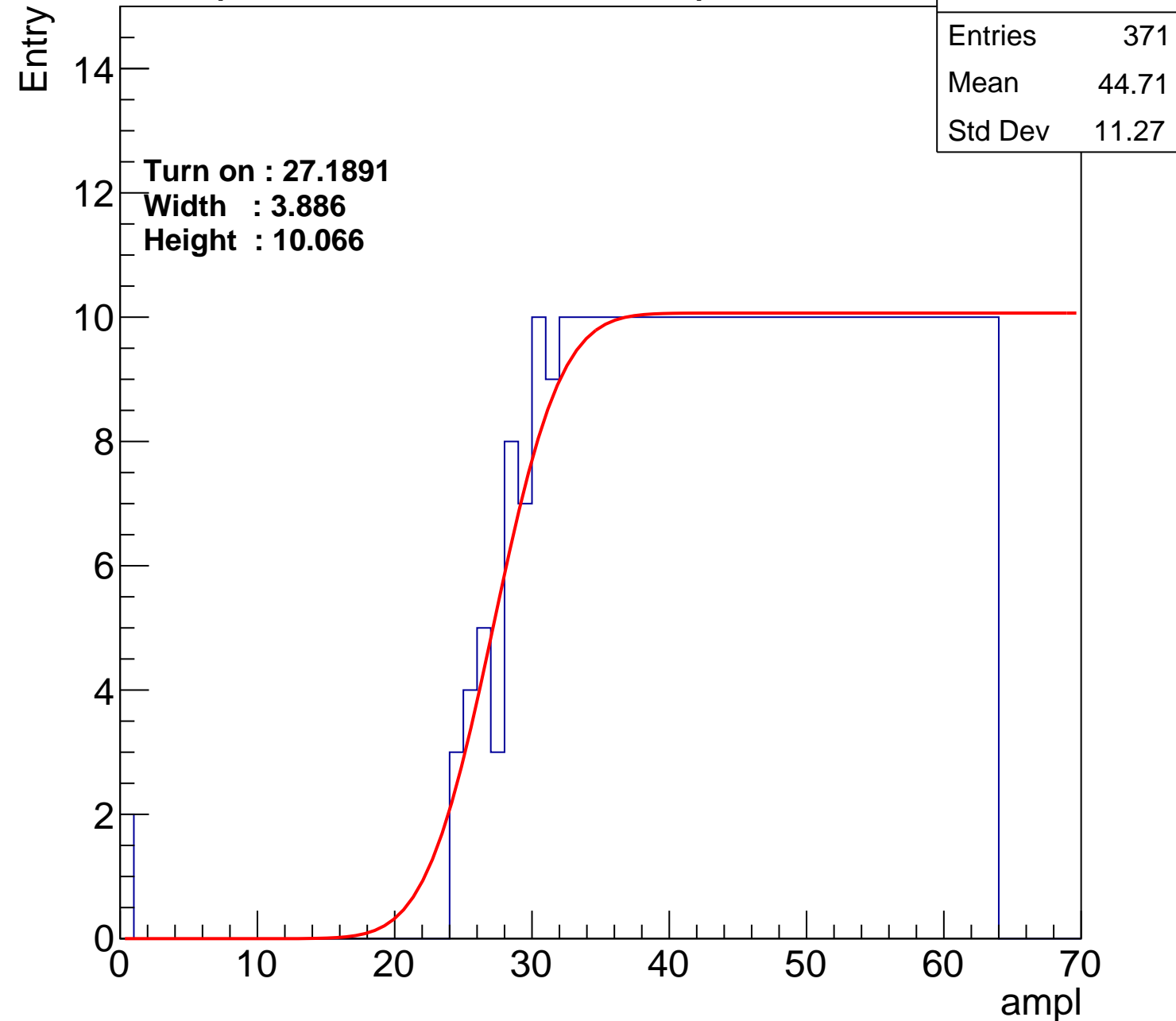
Width : 3.886

Height : 10.066

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U16-ch40

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	390
Mean	43.84
Std Dev	11.6

**Turn on : 25.2882**

**Width : 3.729**

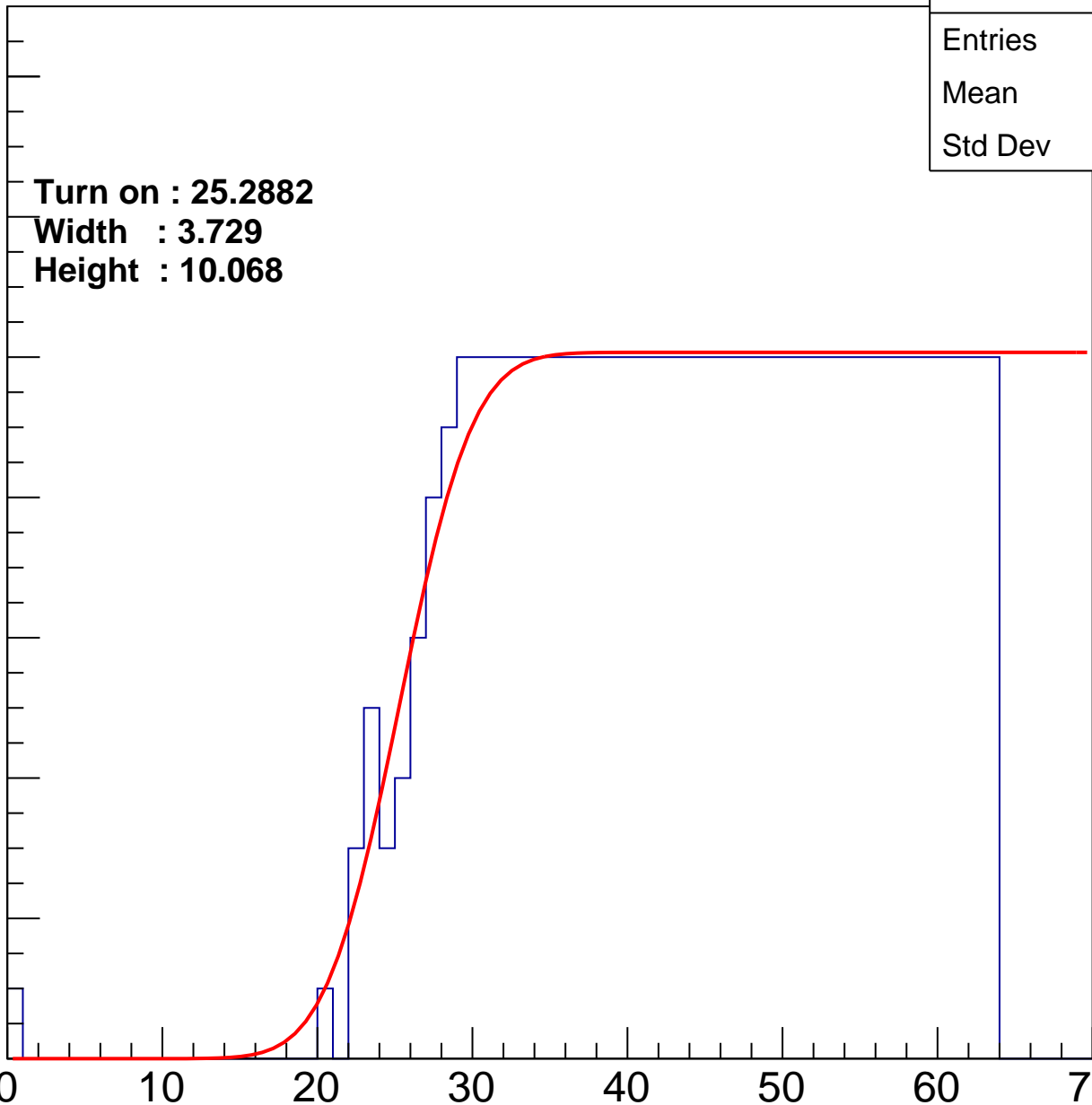
**Height : 10.068**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U16-ch41

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	378
Mean	44.28
Std Dev	11.68

**Turn on : 26.5963**

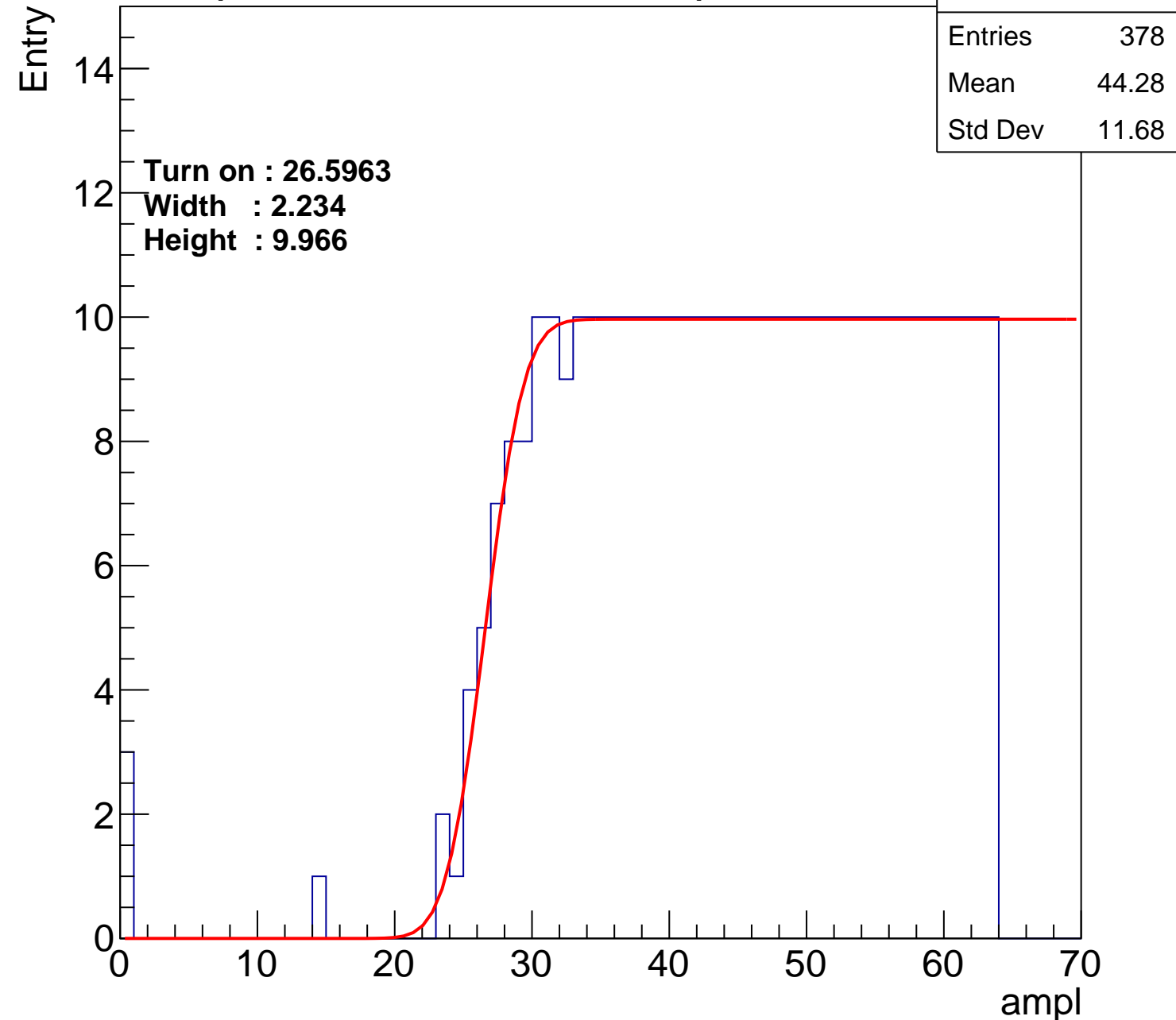
**Width : 2.234**

**Height : 9.966**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U16-ch42

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	356
Mean	45.32
Std Dev	11.19

Turn on : 28.3333

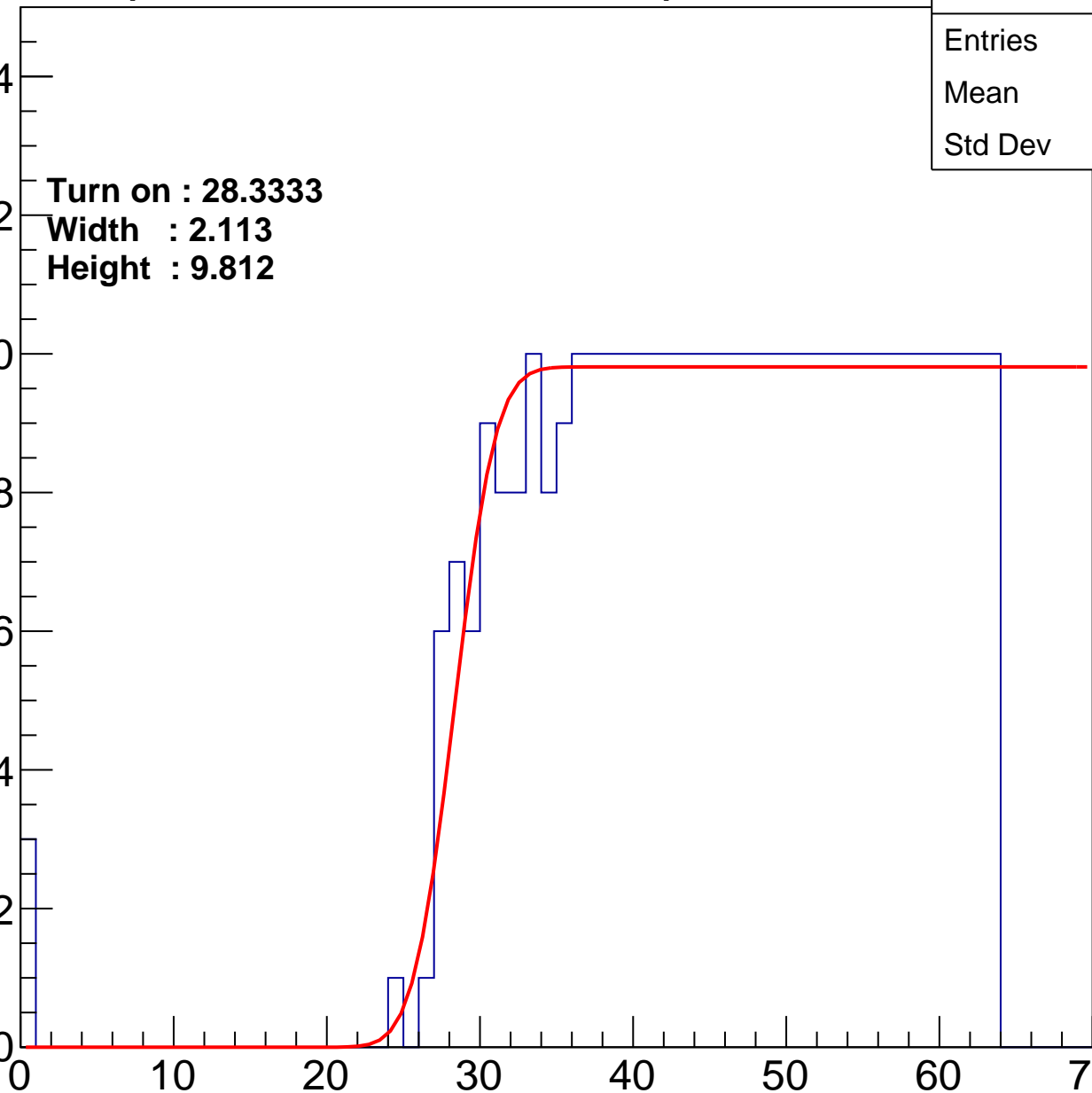
Width : 2.113

Height : 9.812

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U16-ch43

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	341
Mean	46.03
Std Dev	10.76

**Turn on : 29.9737**

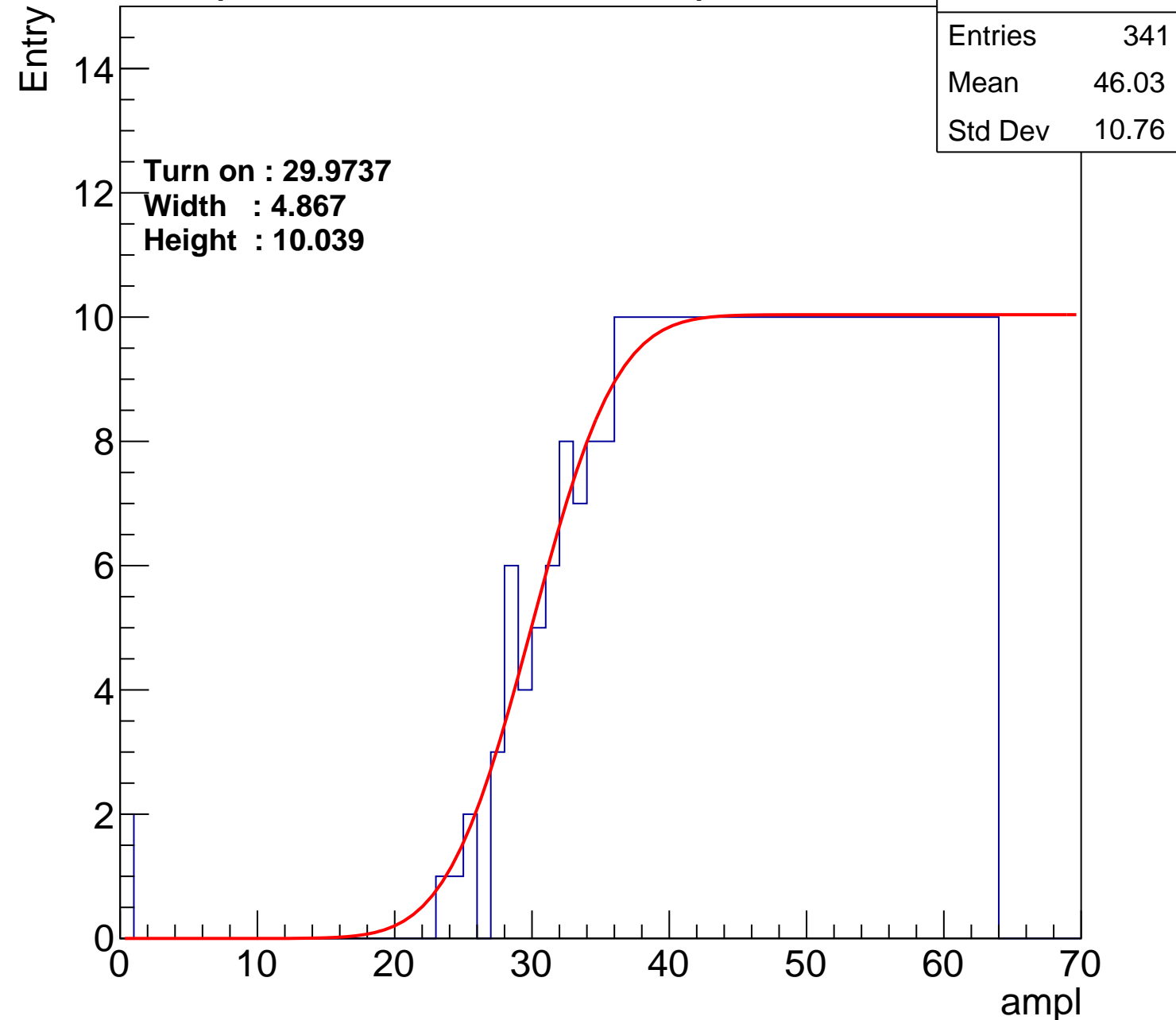
**Width : 4.867**

**Height : 10.039**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U16-ch44

calib\_packv5\_042523\_0143.root, FC#0, port D2

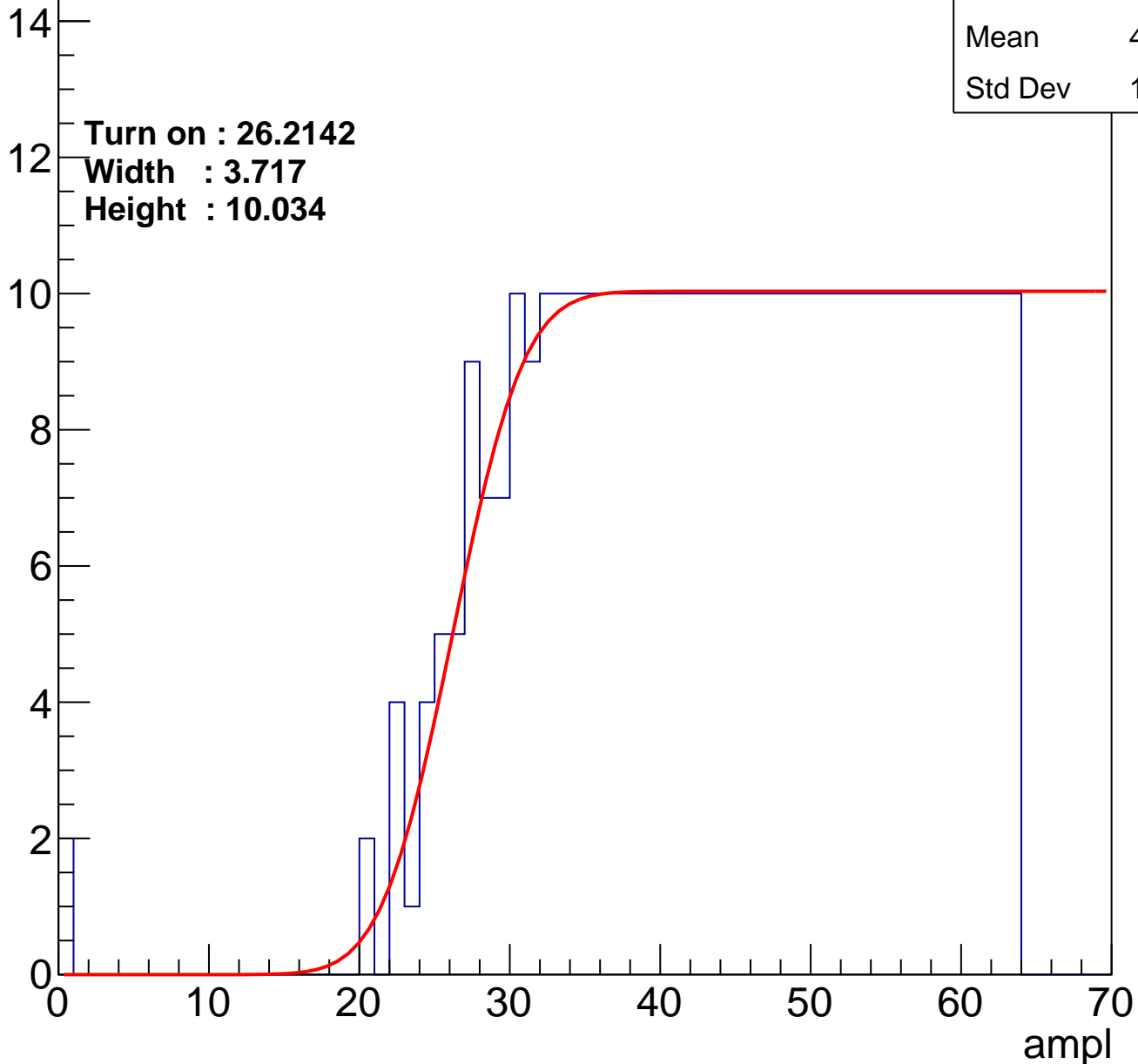
Entries	385
Mean	43.96
Std Dev	11.74

Turn on : 26.2142

Width : 3.717

Height : 10.034

Entry



# B1L101S, U16-ch45

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	384
Mean	43.99
Std Dev	11.88

Turn on : 26.0019

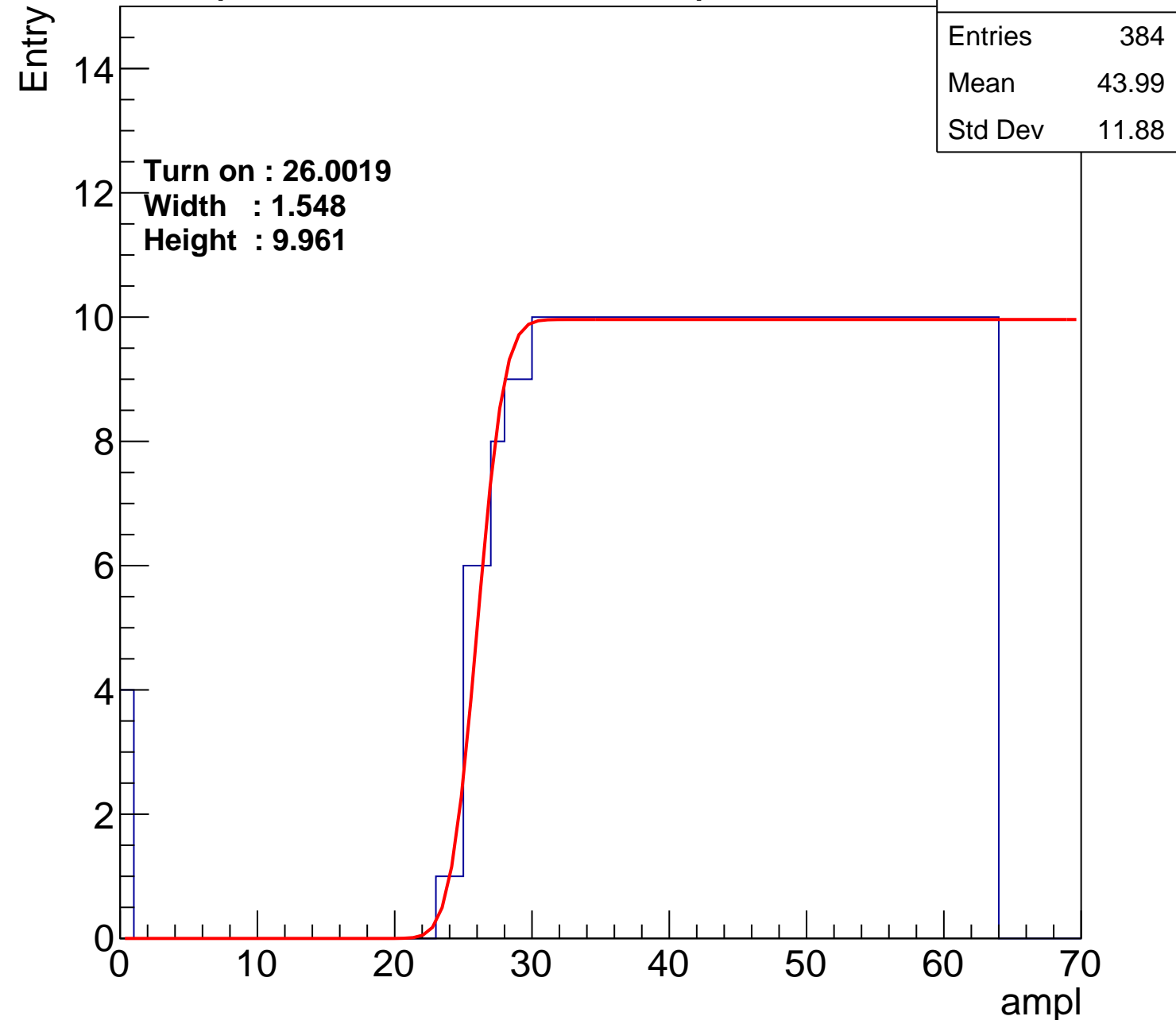
Width : 1.548

Height : 9.961

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U16-ch46

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	375
Mean	44.35
Std Dev	11.79

Turn on : 26.9230

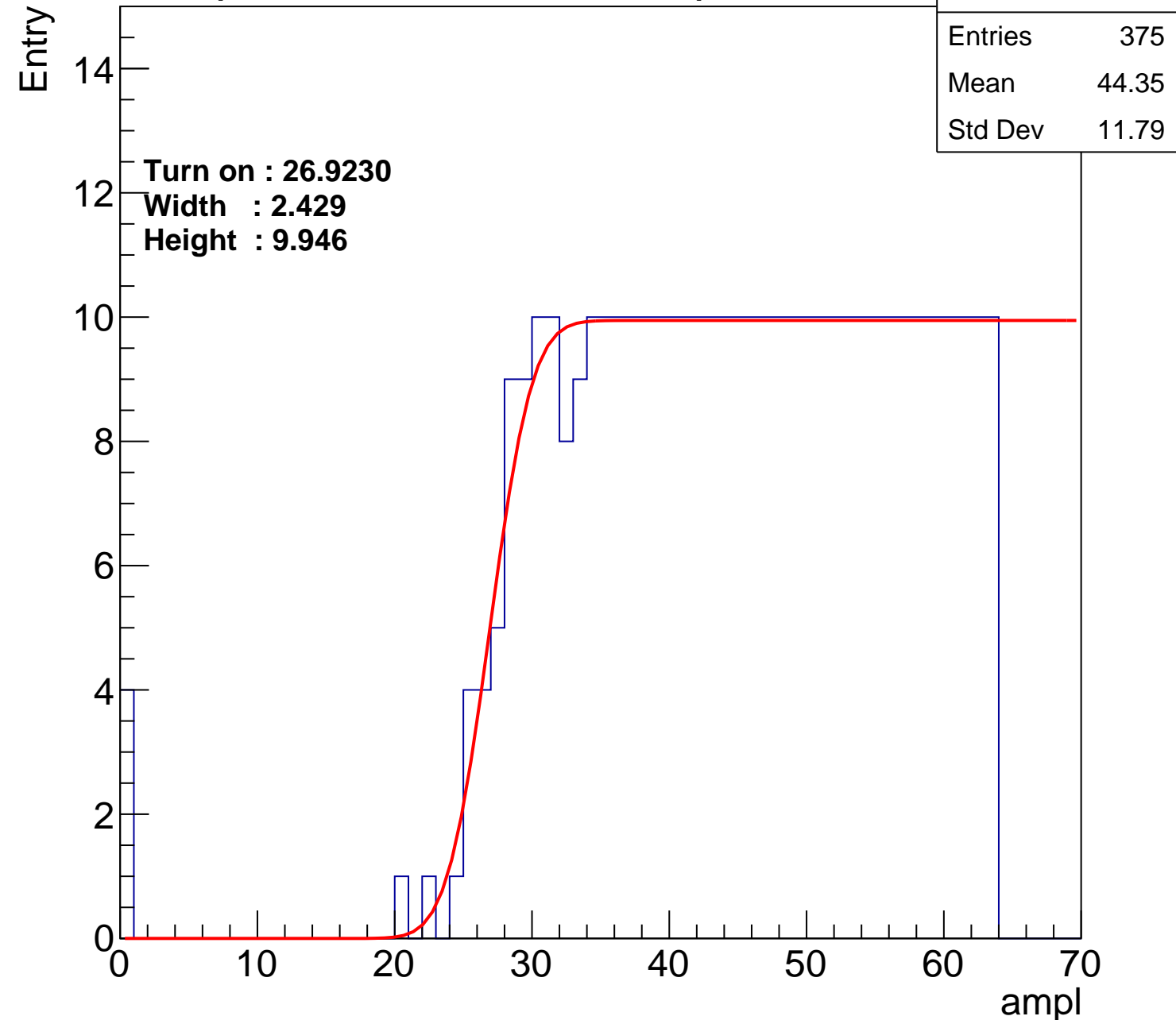
Width : 2.429

Height : 9.946

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L101S, U16-ch47

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	370
Mean	44.6
Std Dev	11.67

Turn on : 27.5808

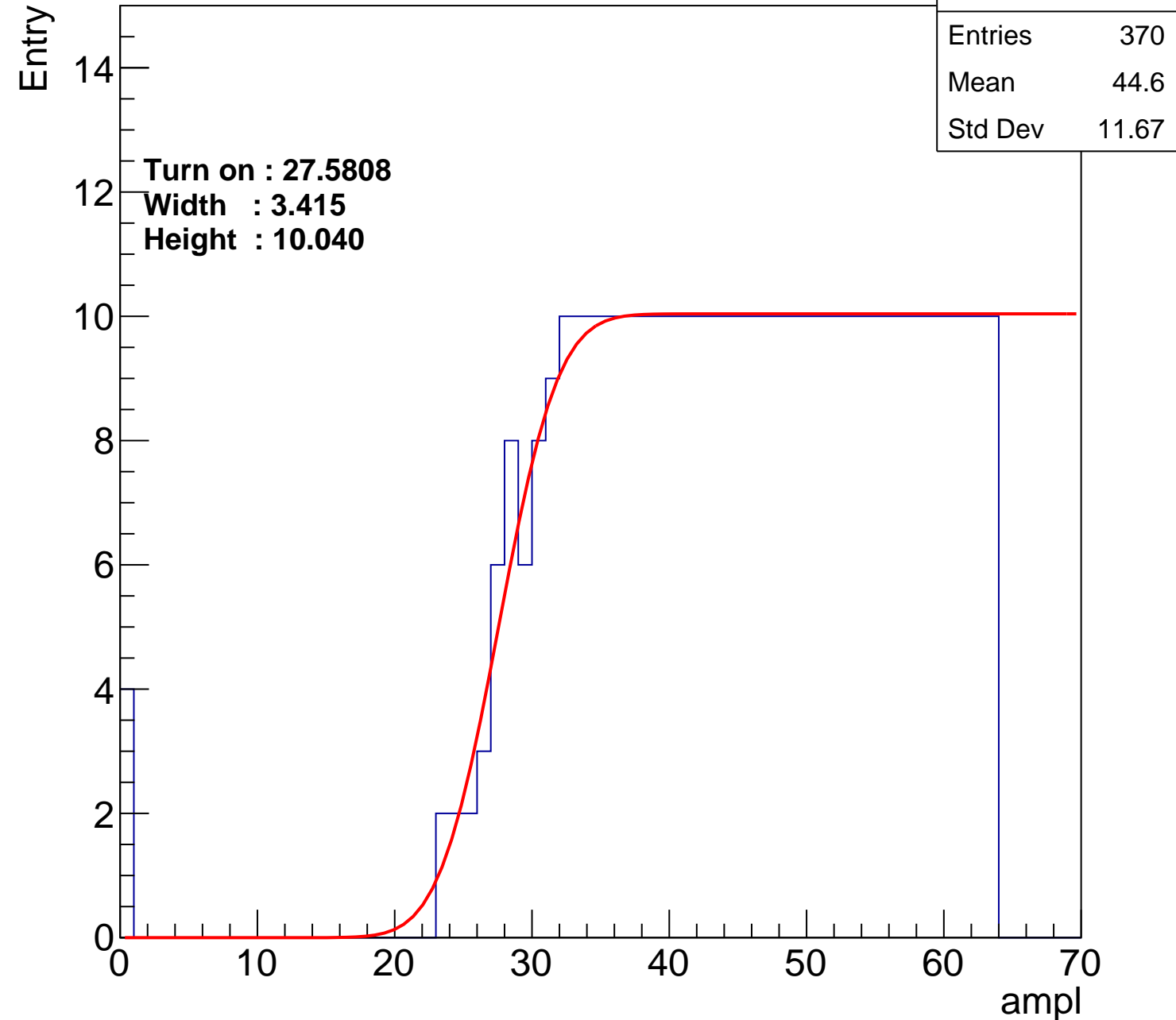
Width : 3.415

Height : 10.040

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U16-ch48

calib\_packv5\_042523\_0143.root, FC#0, port D2

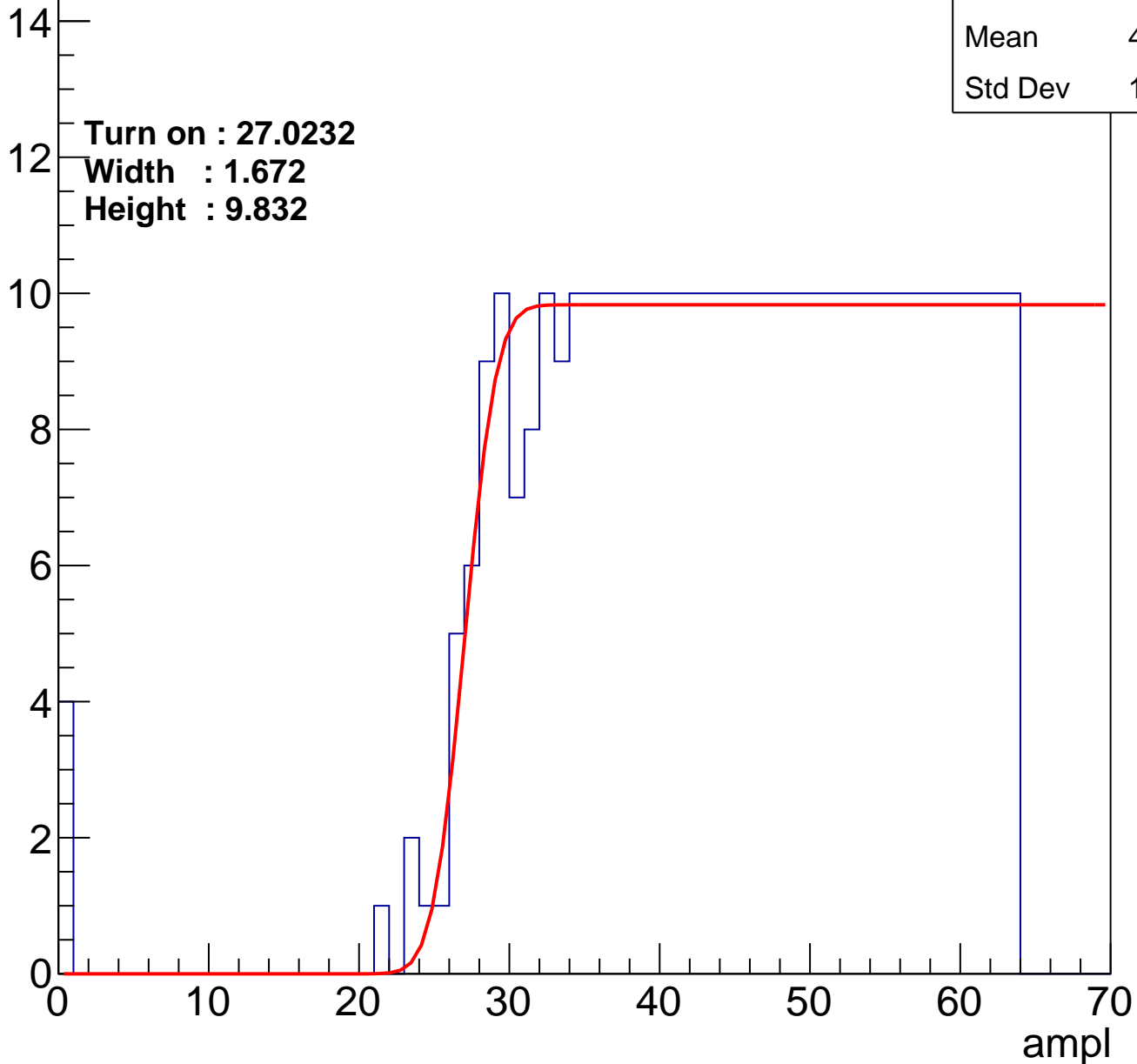
Entries	373
Mean	44.44
Std Dev	11.76

Turn on : 27.0232

Width : 1.672

Height : 9.832

Entry



# B1L101S, U16-ch49

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	369
Mean	44.53
Std Dev	11.99

Turn on : 28.0436

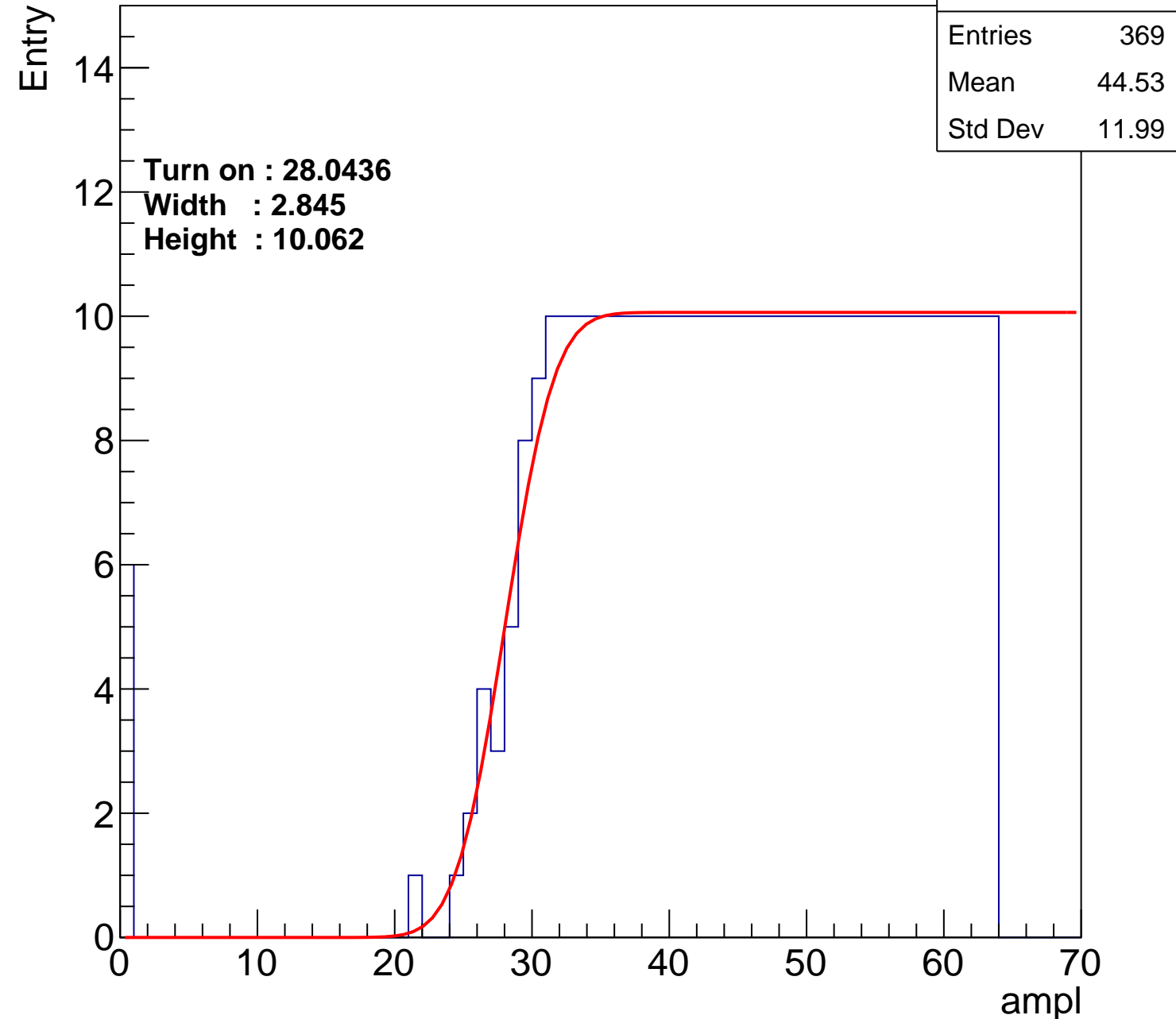
Width : 2.845

Height : 10.062

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U16-ch50

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	379
Mean	44.32
Std Dev	11.41

Turn on : 26.7300

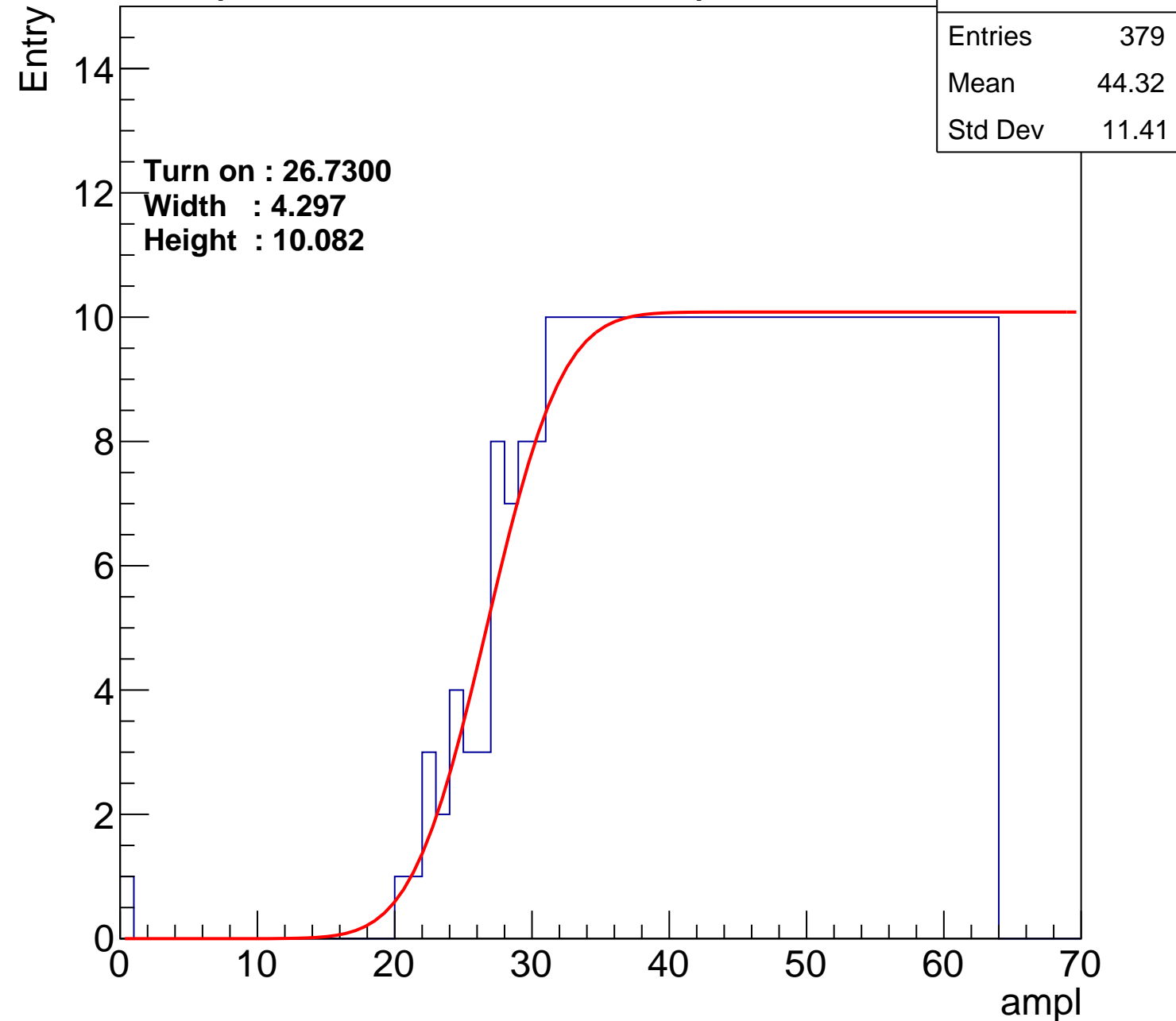
Width : 4.297

Height : 10.082

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U16-ch51

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	386
Mean	43.89
Std Dev	11.87

Turn on : 26.3244

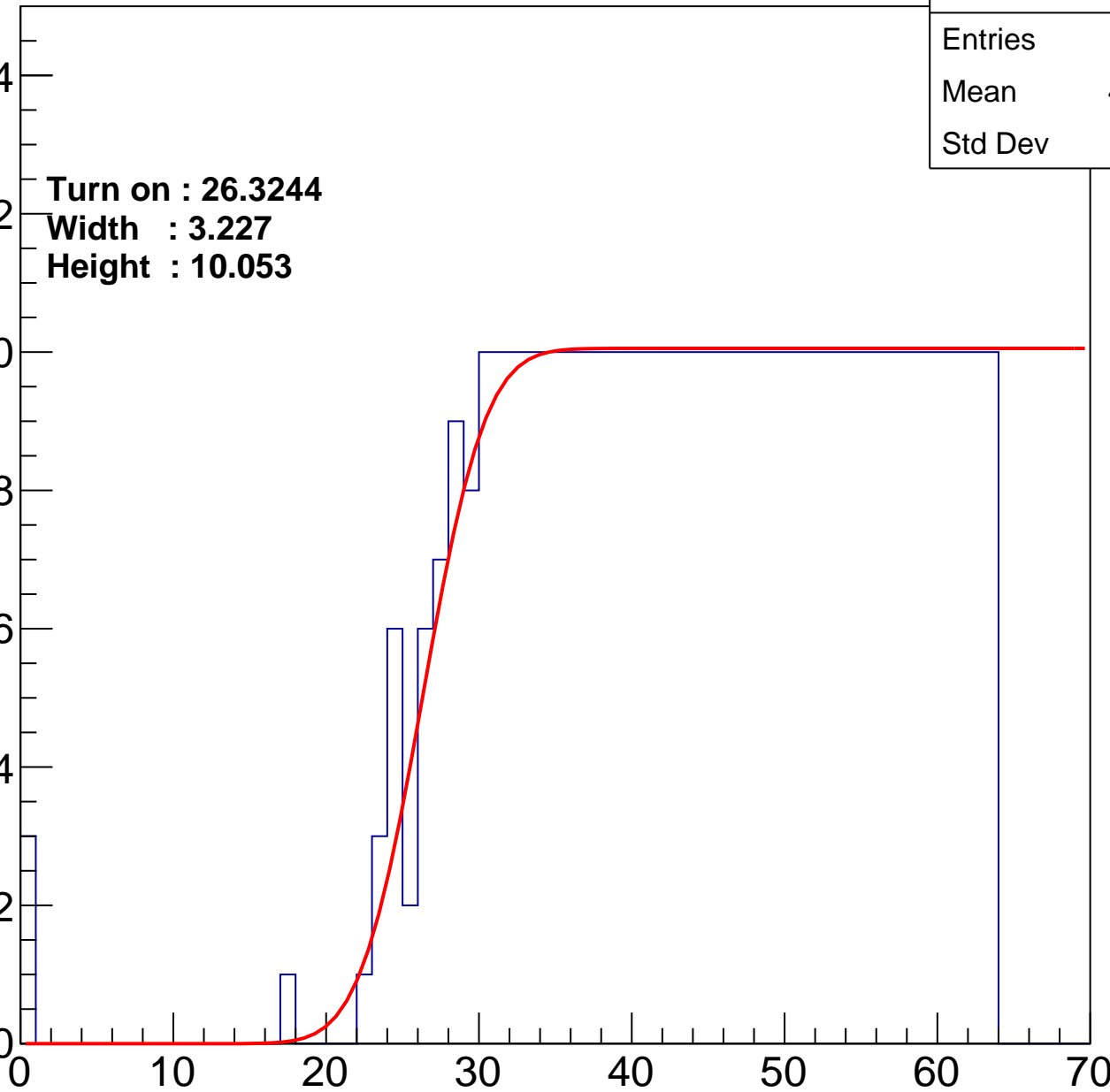
Width : 3.227

Height : 10.053

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U16-ch52

calib\_packv5\_042523\_0143.root, FC#0, port D2

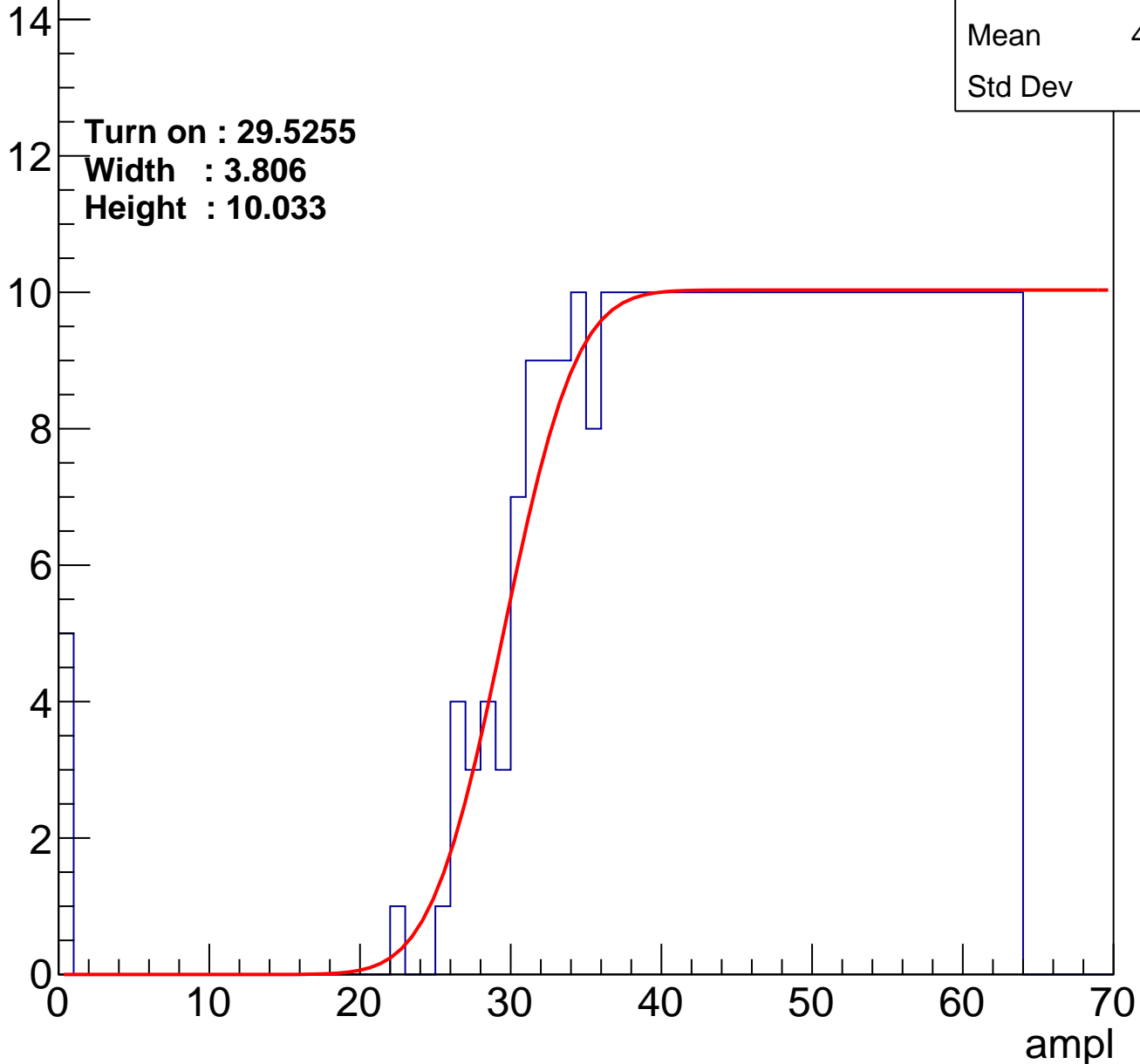
Entries	353
Mean	45.28
Std Dev	11.6

Turn on : 29.5255

Width : 3.806

Height : 10.033

Entry

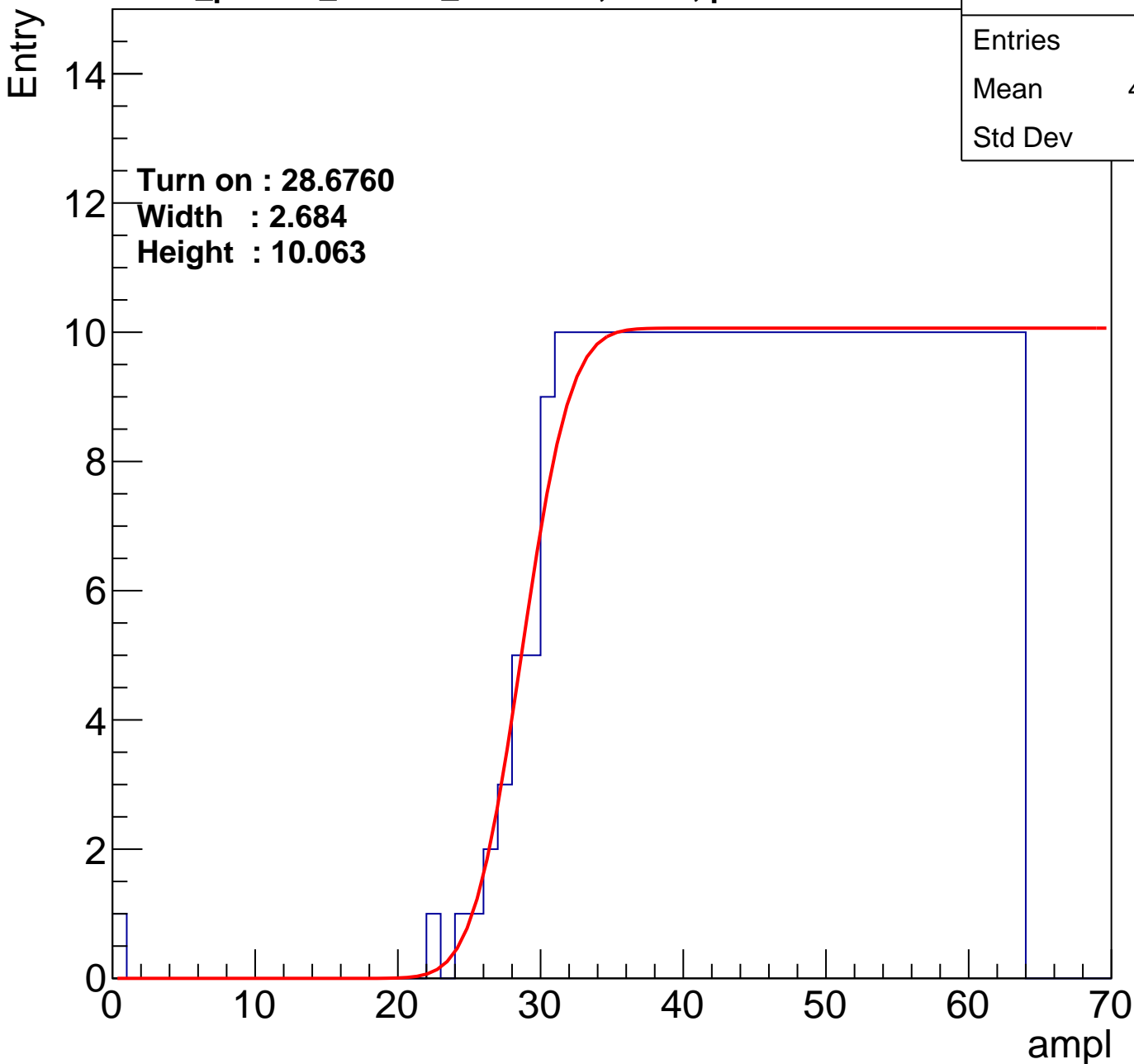


**calib\_packv5\_042523\_0143.root, FC#0, port D2**

**calib\_packv5\_042523\_0143.root, FC#0, port D2**

Entries	358
Mean	45.44
Std Dev	10.7

**Height : 10.063**



# B1L101S, U16-ch54

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	387
Mean	43.63
Std Dev	12.4

Turn on : 26.0136

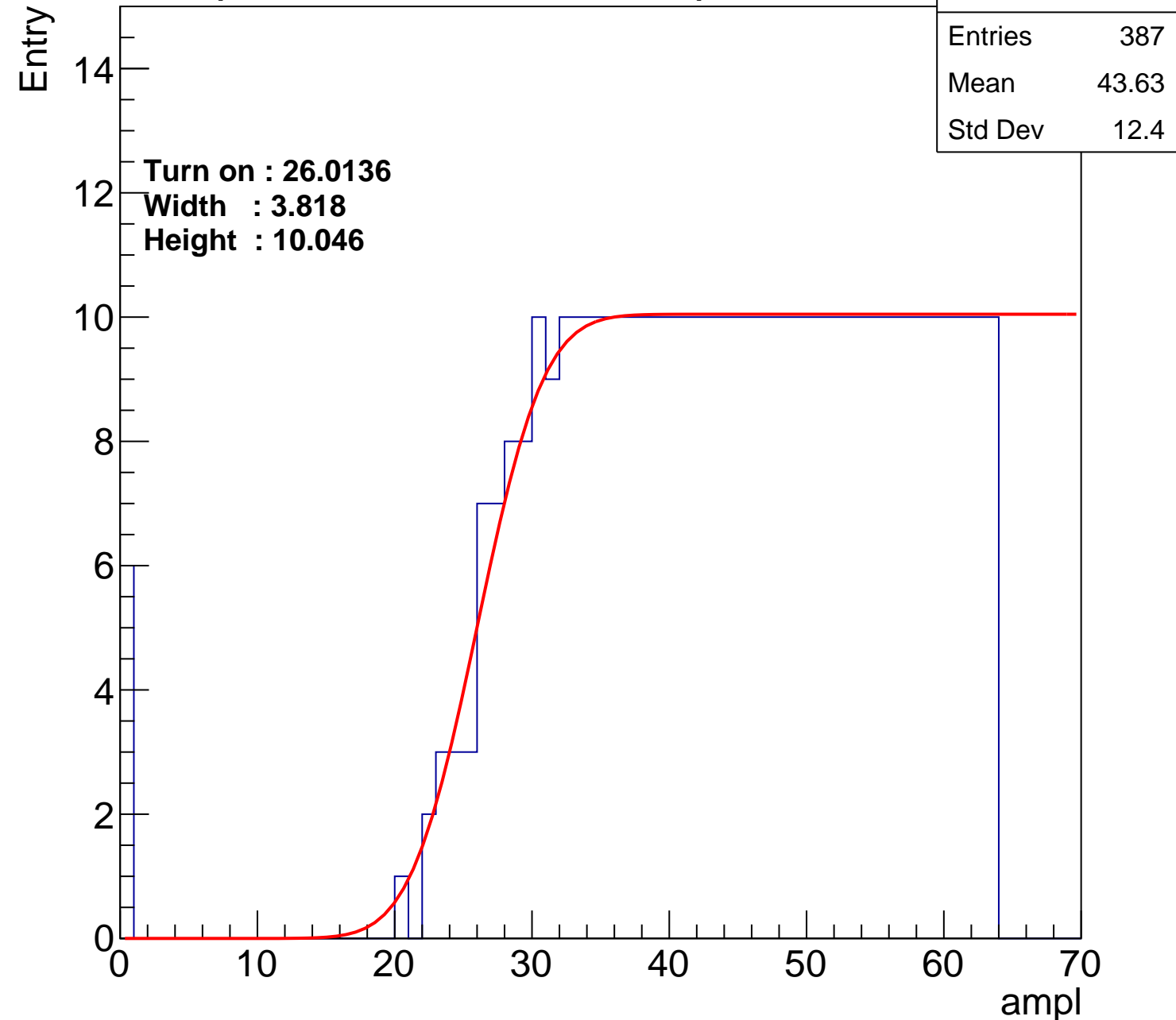
Width : 3.818

Height : 10.046

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L101S, U16-ch55

calib\_packv5\_042523\_0143.root, FC#0, port D2

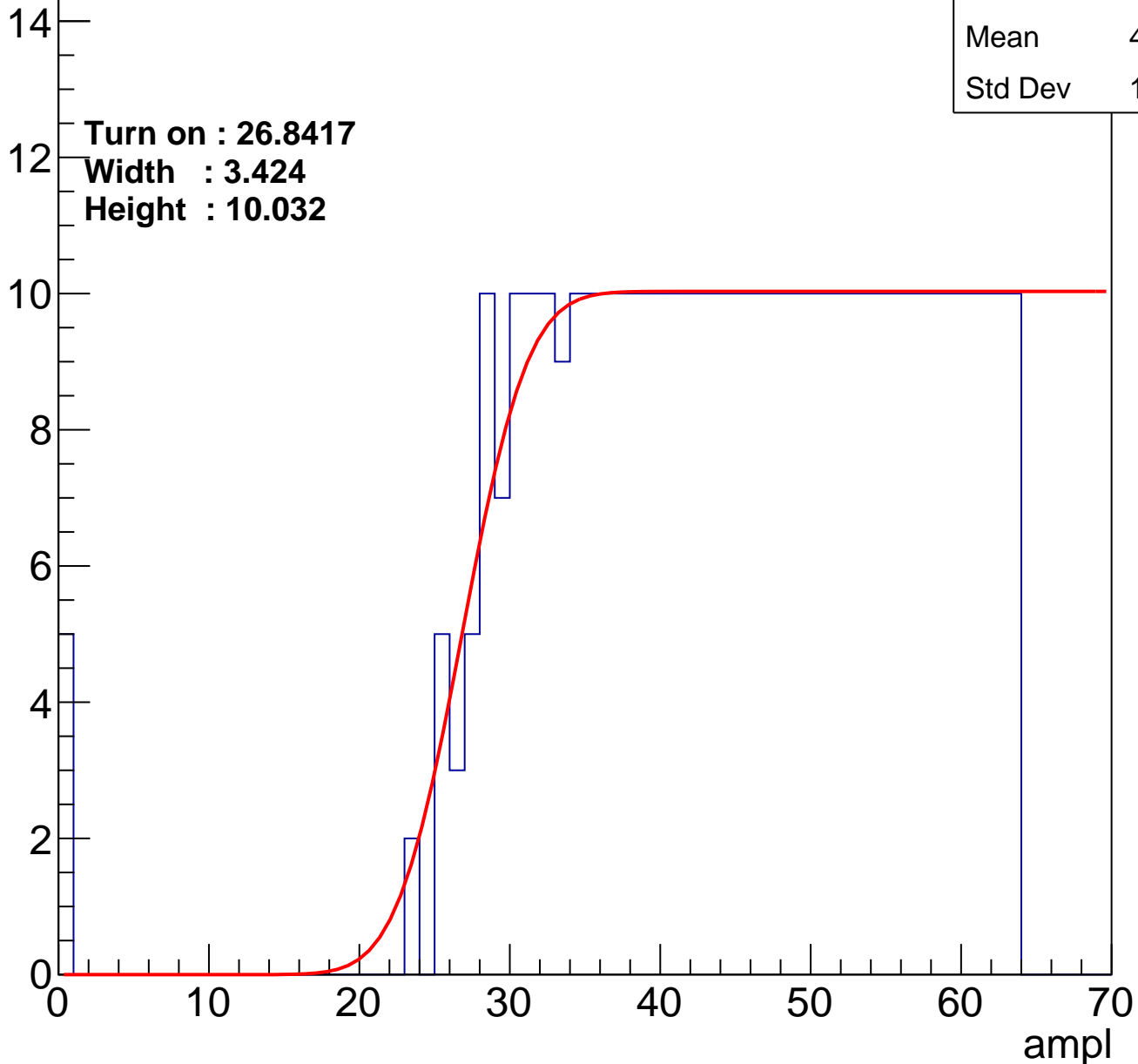
Entries	376
Mean	44.27
Std Dev	11.94

Turn on : 26.8417

Width : 3.424

Height : 10.032

Entry



# B1L101S, U16-ch56

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	385
Mean	44.03
Std Dev	11.56

Turn on : 26.0634

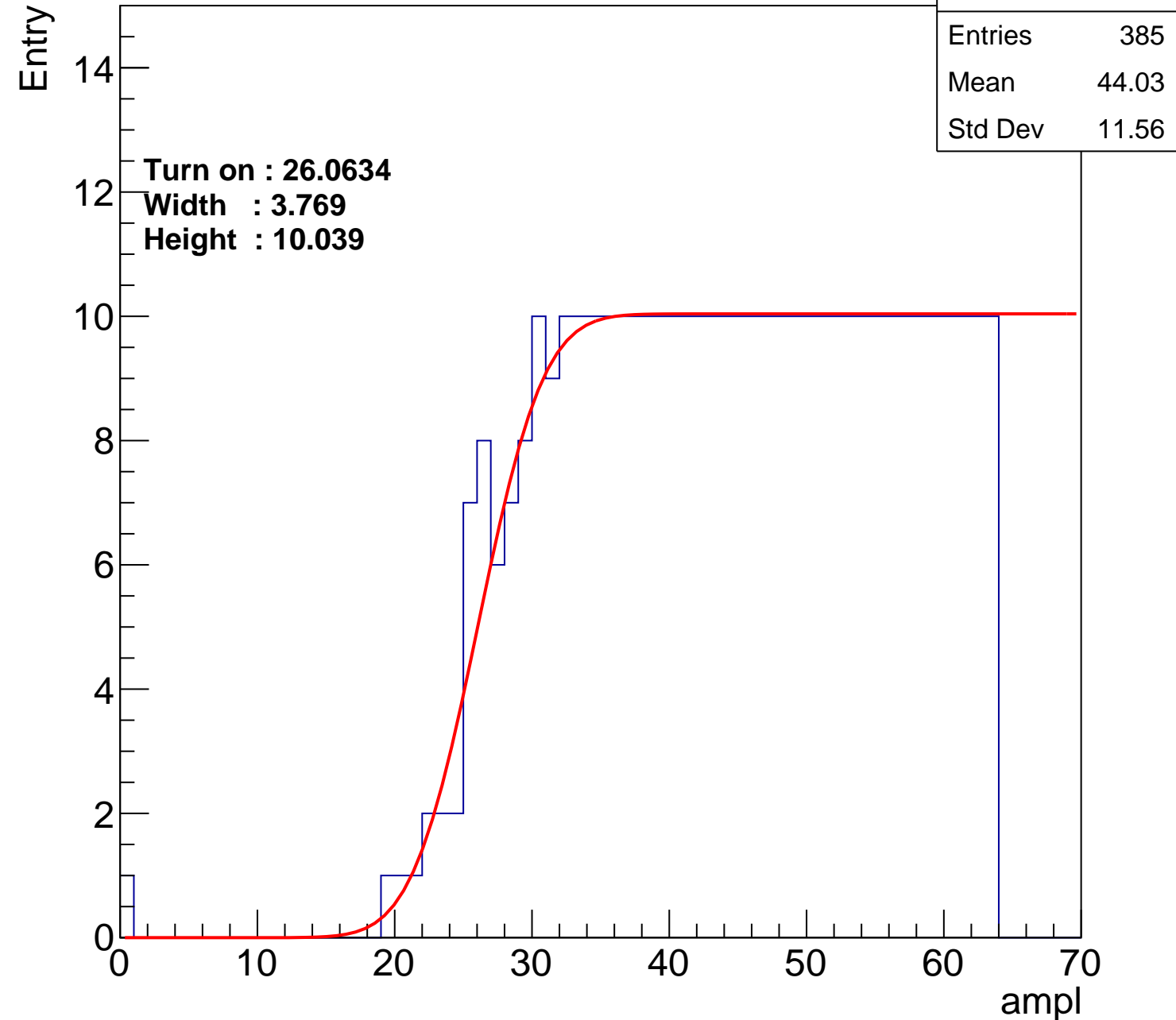
Width : 3.769

Height : 10.039

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U16-ch57

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	373
Mean	44.4
Std Dev	11.82

Turn on : 27.6597

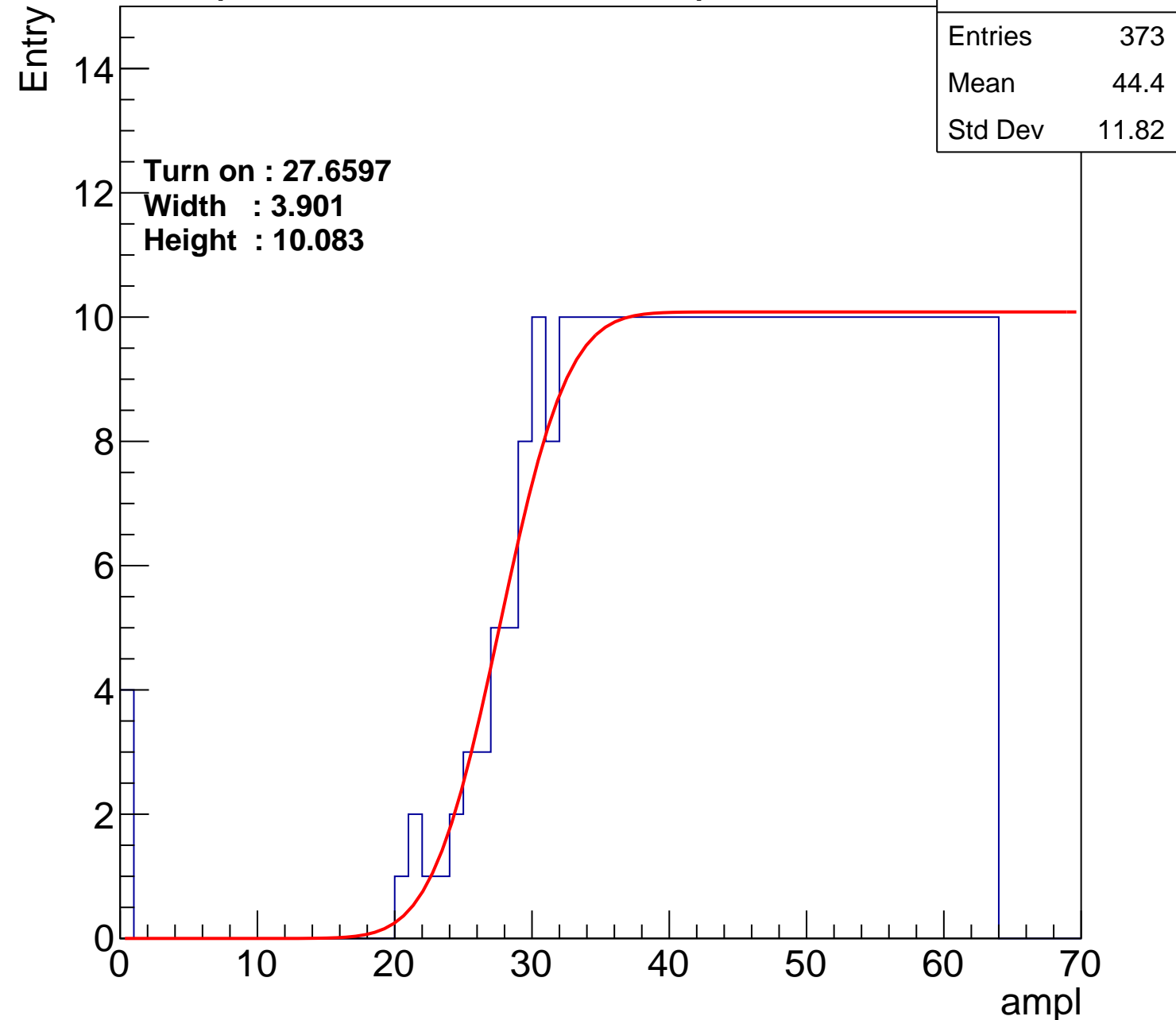
Width : 3.901

Height : 10.083

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U16-ch58

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	395
Mean	43.53
Std Dev	11.85

**Turn on : 25.8037**

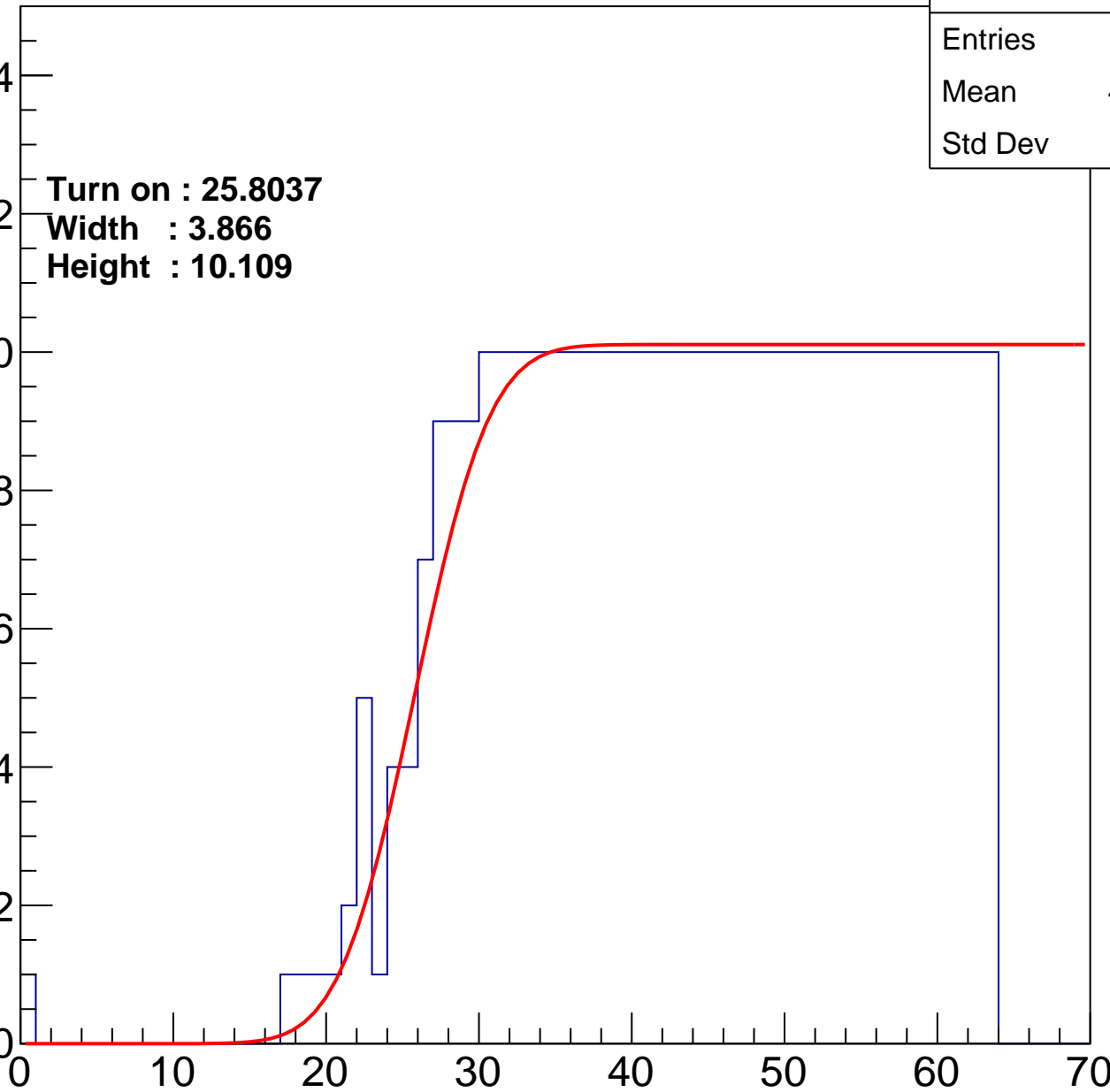
**Width : 3.866**

**Height : 10.109**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U16-ch59

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	365
Mean	44.96
Std Dev	11.29

Turn on : 28.0041

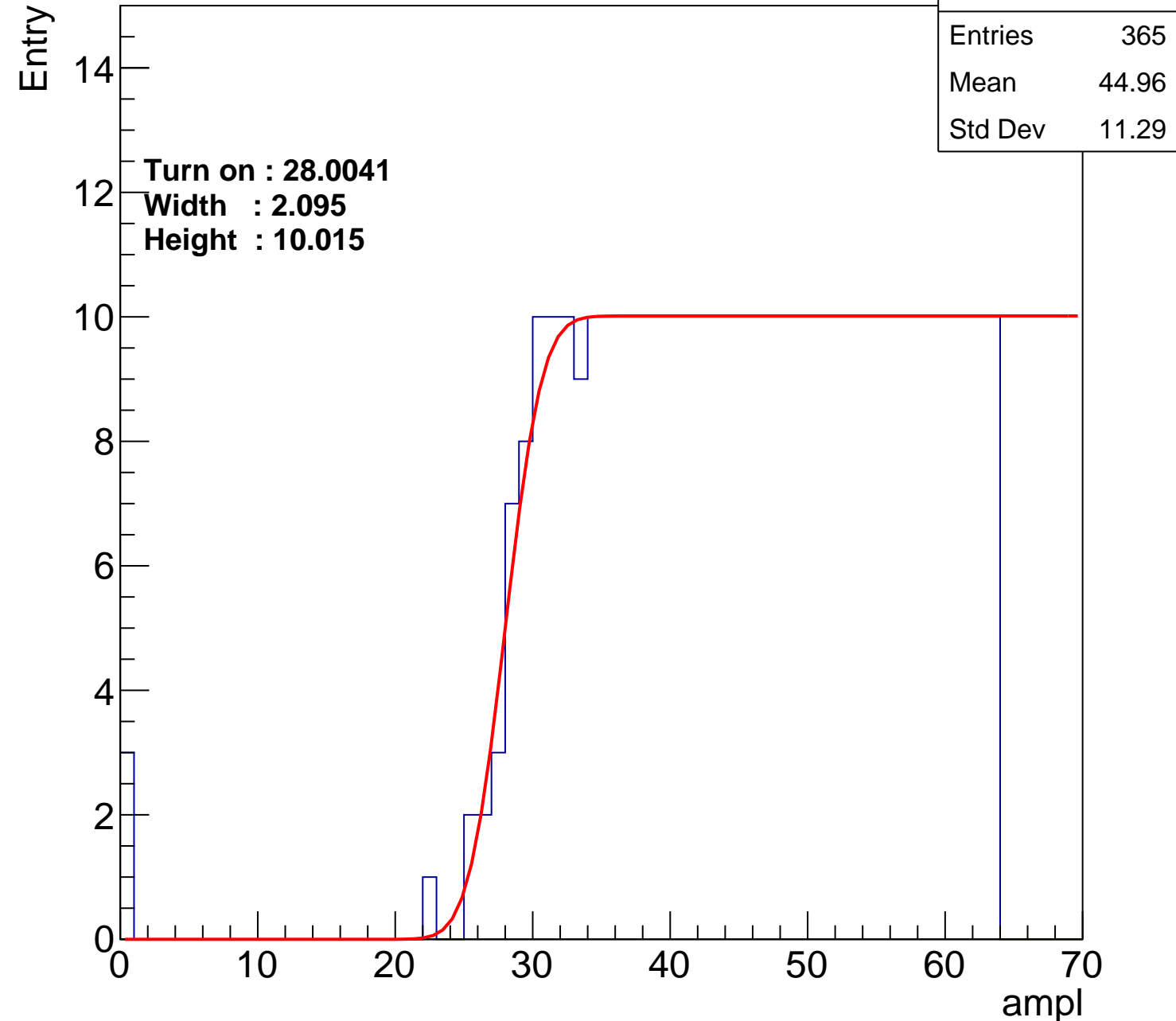
Width : 2.095

Height : 10.015

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U16-ch60

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	406
Mean	42.81
Std Dev	12.63

Turn on : 24.3214

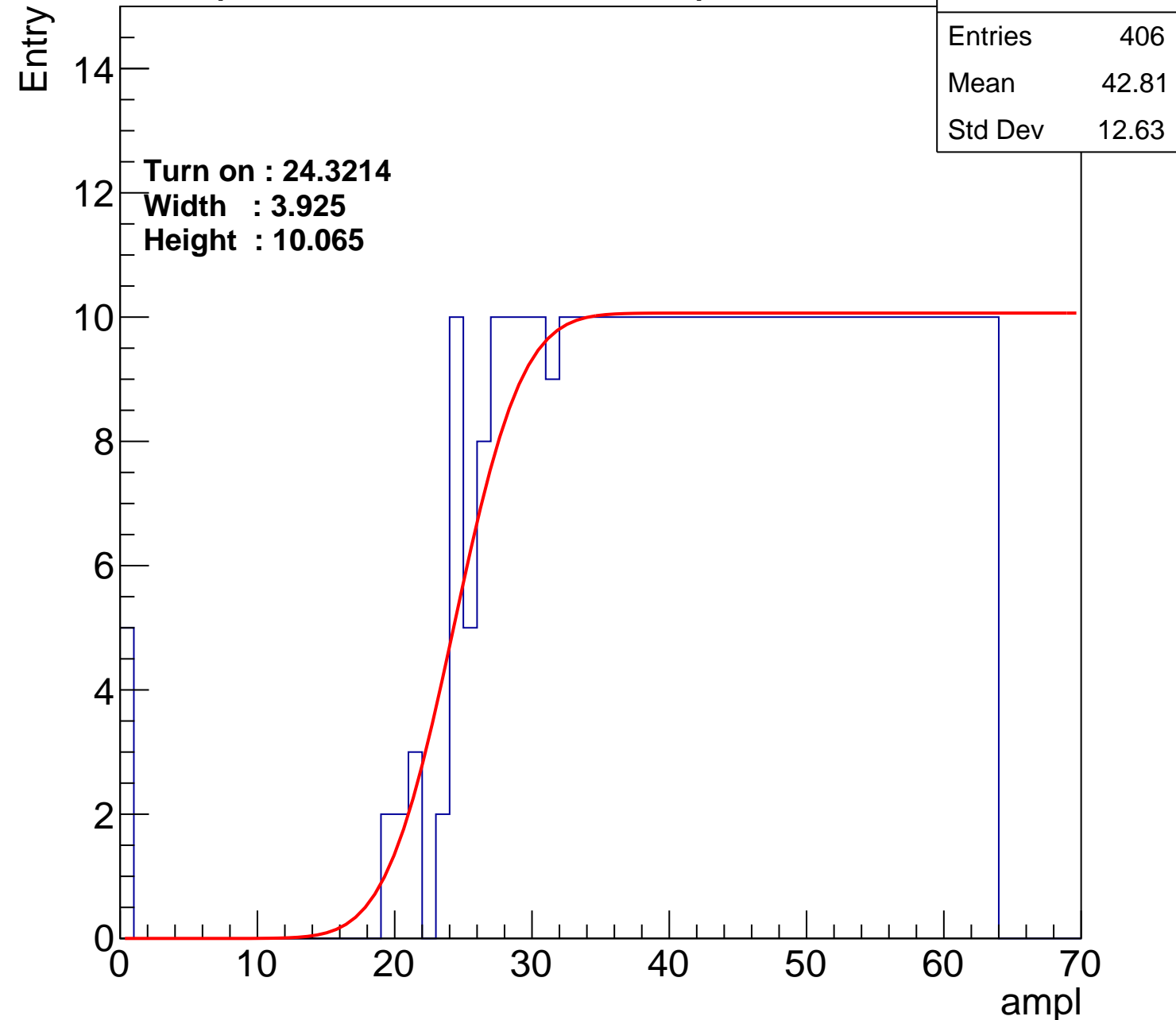
Width : 3.925

Height : 10.065

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U16-ch61

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	365
Mean	44.98
Std Dev	11.16

Turn on : 27.7091

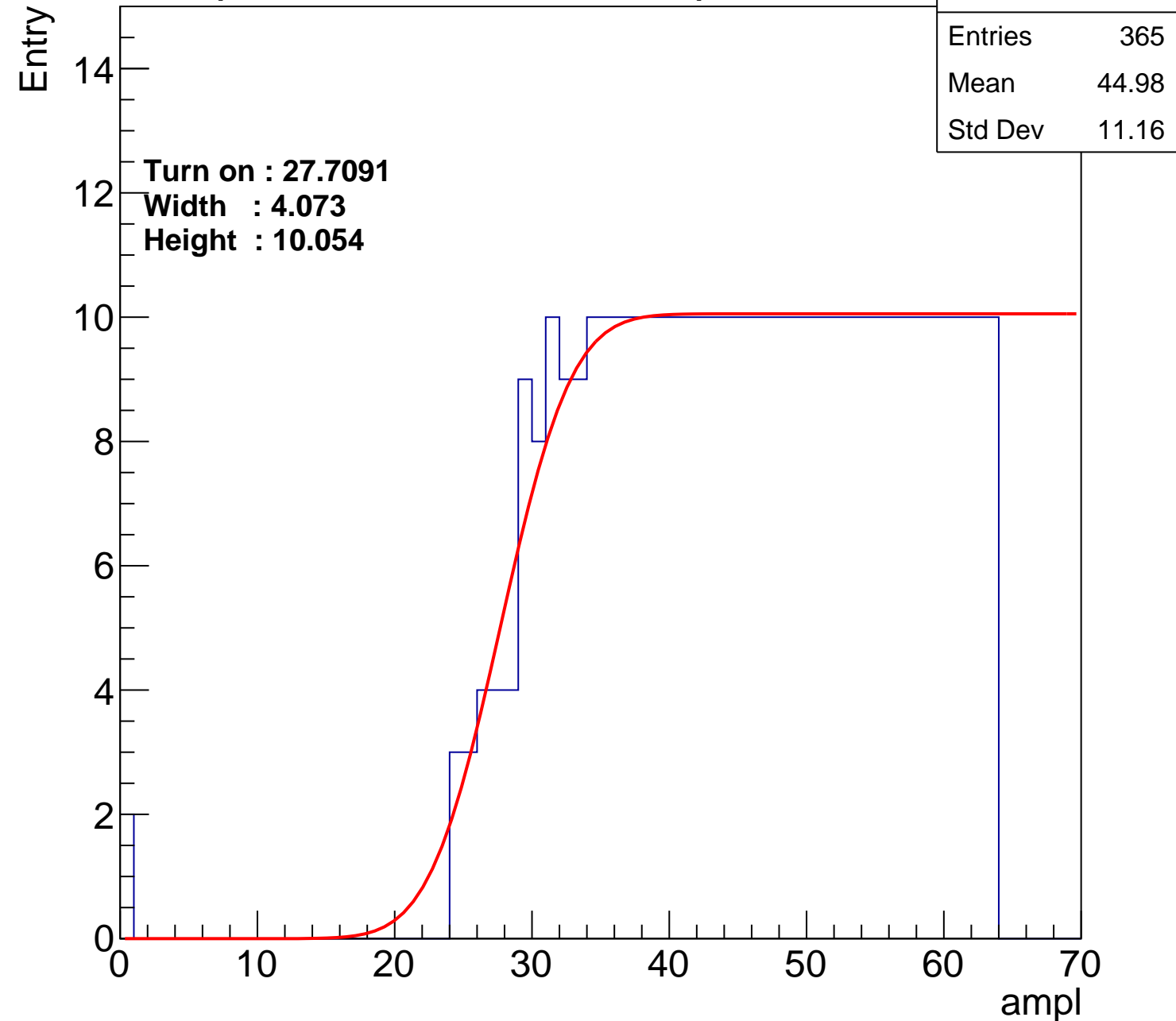
Width : 4.073

Height : 10.054

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U16-ch62

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	384
Mean	43.95
Std Dev	11.88

Turn on : 26.9721

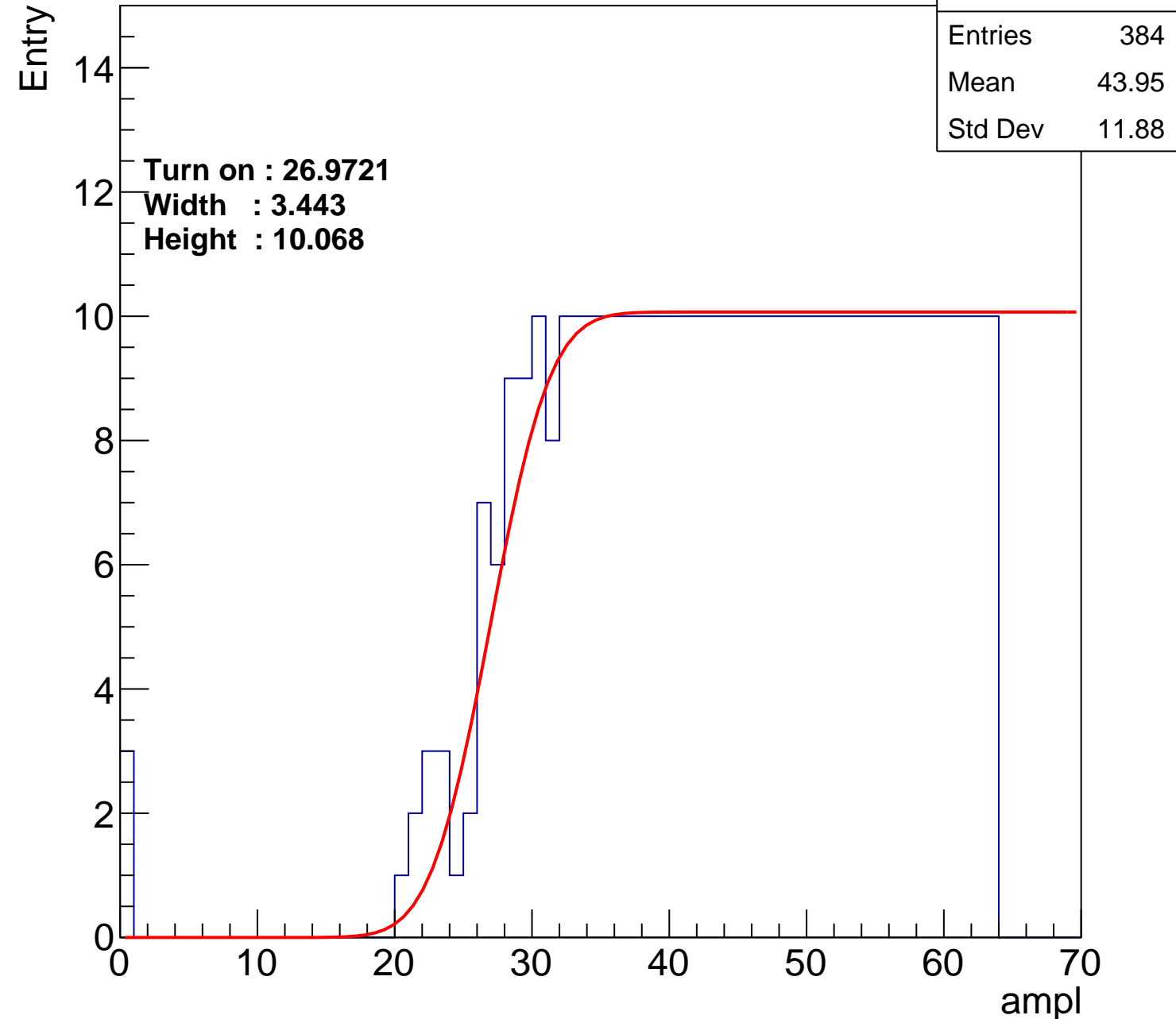
Width : 3.443

Height : 10.068

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L101S, U16-ch63

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	359
Mean	45.25
Std Dev	11.07

**Turn on : 28.8797**

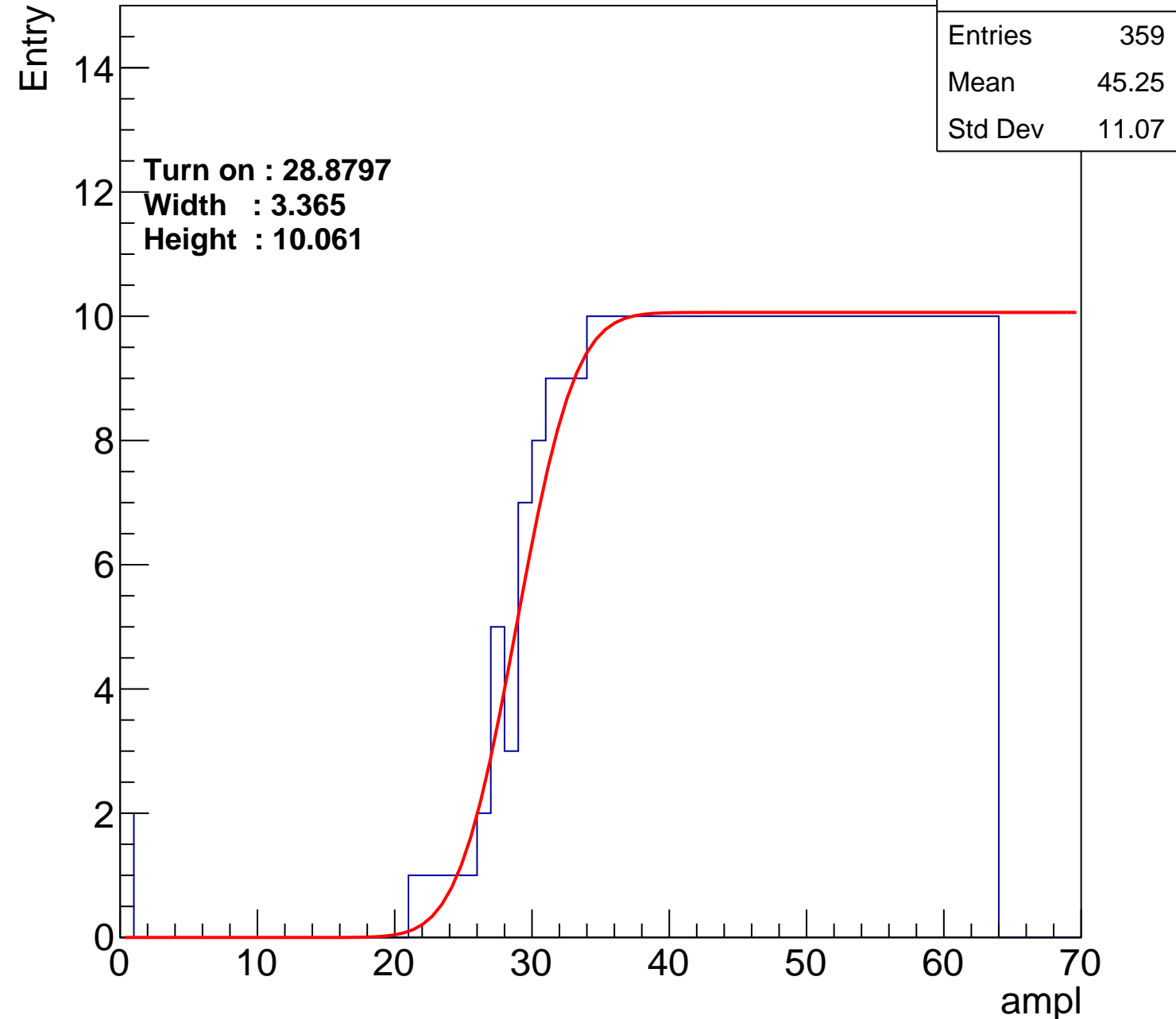
**Width : 3.365**

**Height : 10.061**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U16-ch64

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	358
Mean	45.11
Std Dev	11.51

Turn on : 29.0927

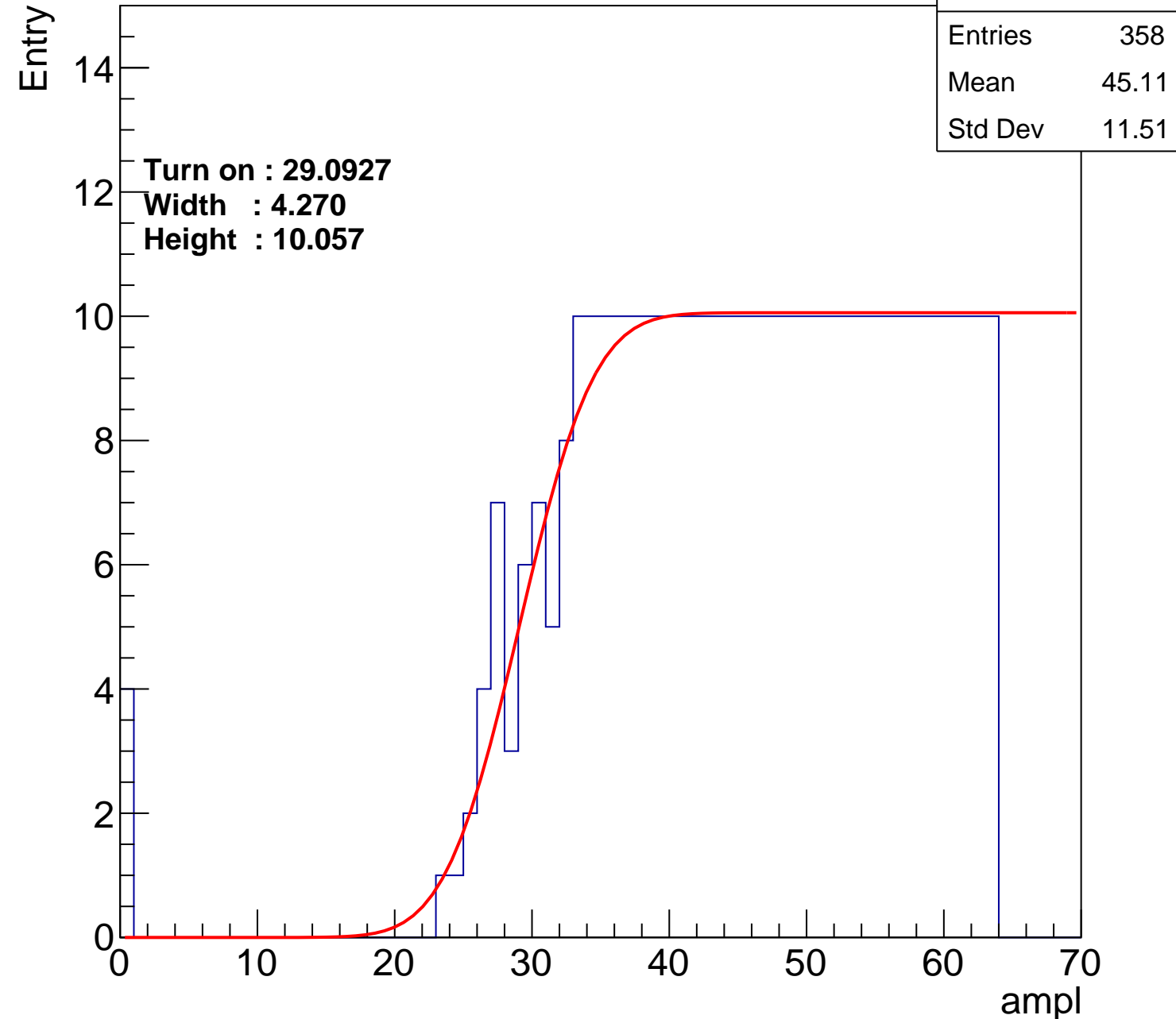
Width : 4.270

Height : 10.057

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U16-ch65

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	367
Mean	44.9
Std Dev	11.18

Turn on : 27.6327

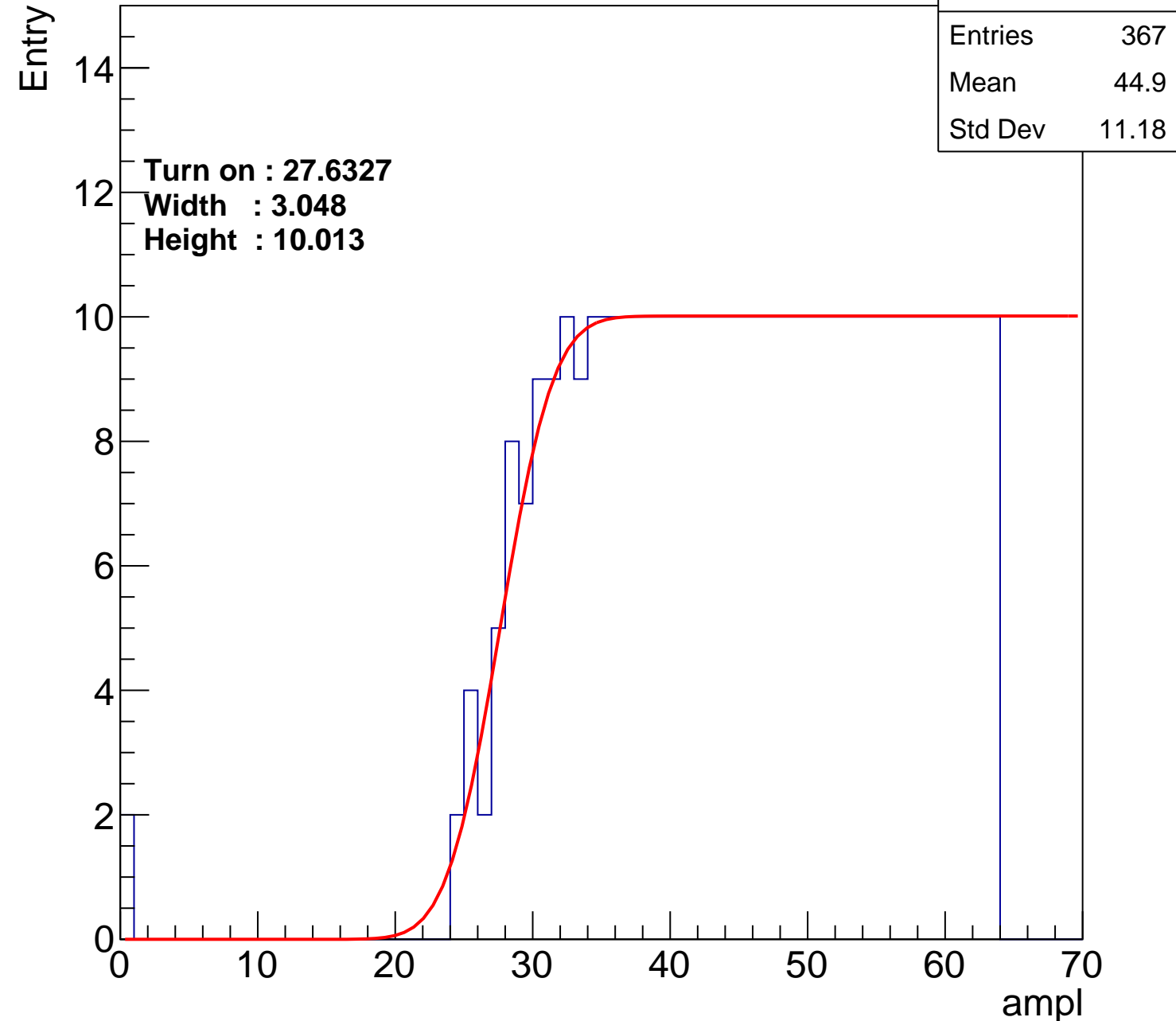
Width : 3.048

Height : 10.013

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U16-ch66

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	349
Mean	45.78
Std Dev	10.75

**Turn on : 29.5169**

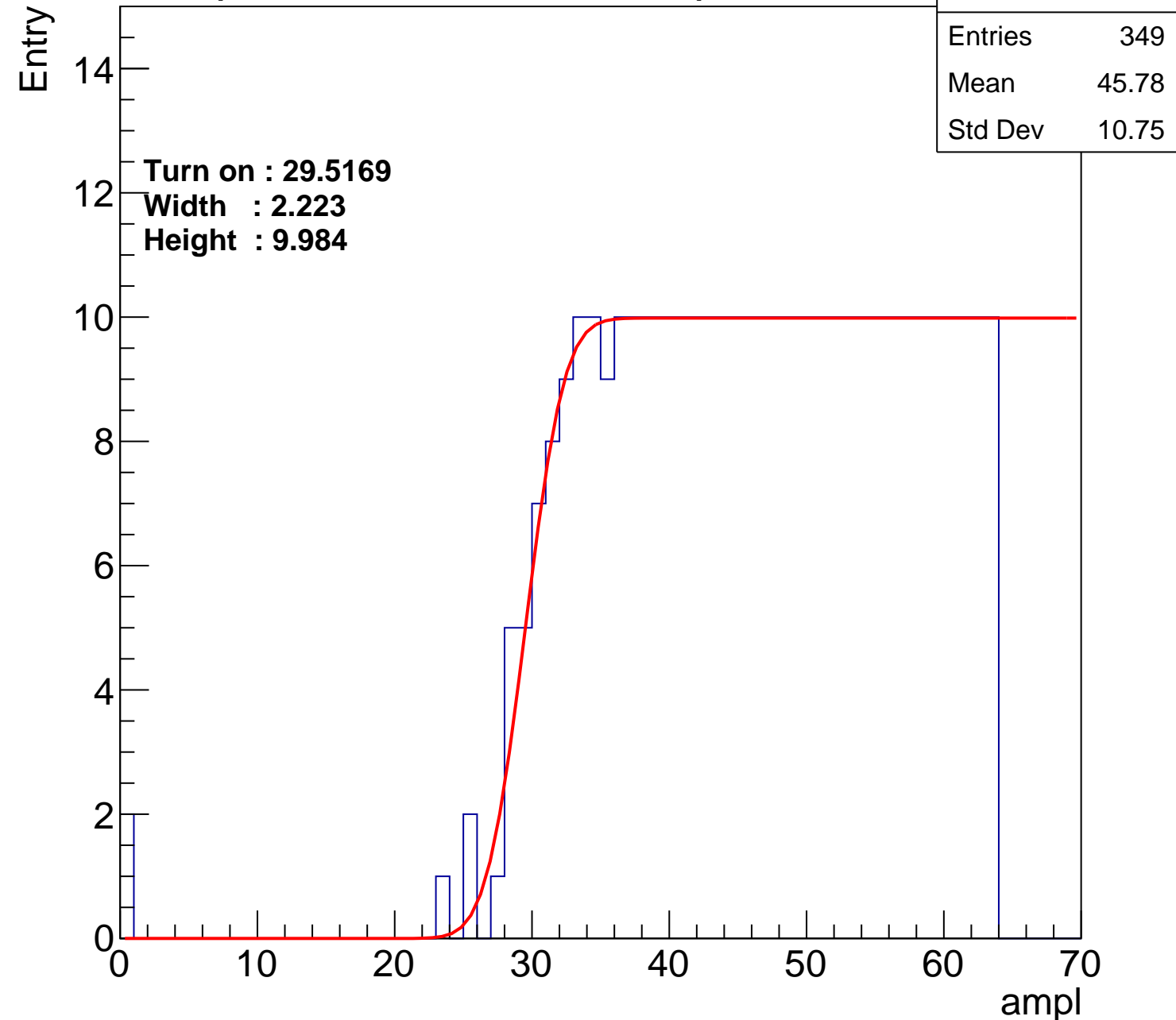
**Width : 2.223**

**Height : 9.984**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U16-ch67

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	378
Mean	44.33
Std Dev	11.51

Turn on : 26.4612

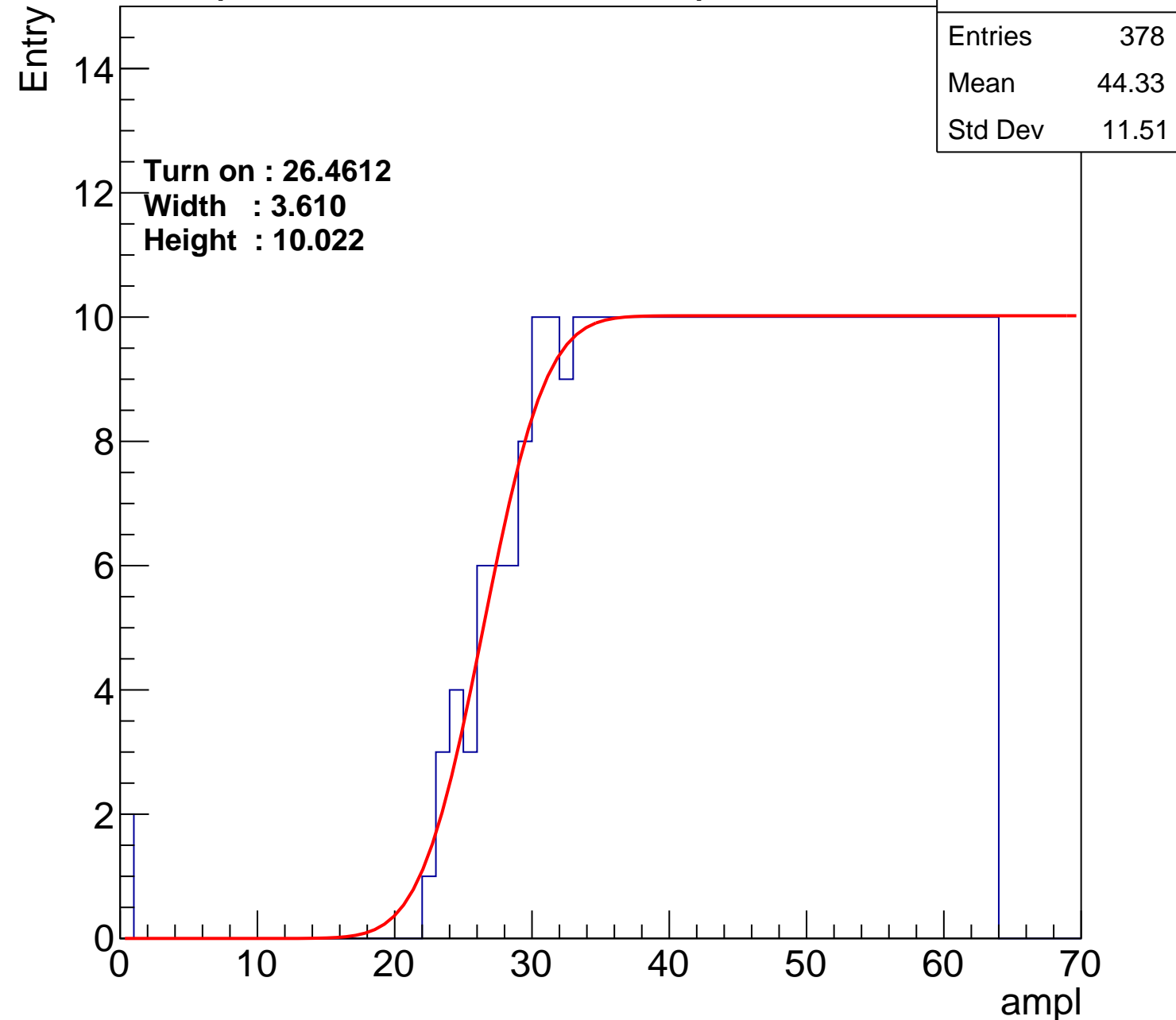
Width : 3.610

Height : 10.022

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U16-ch68

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	364
Mean	45.04
Std Dev	11.03

Turn on : 27.1649

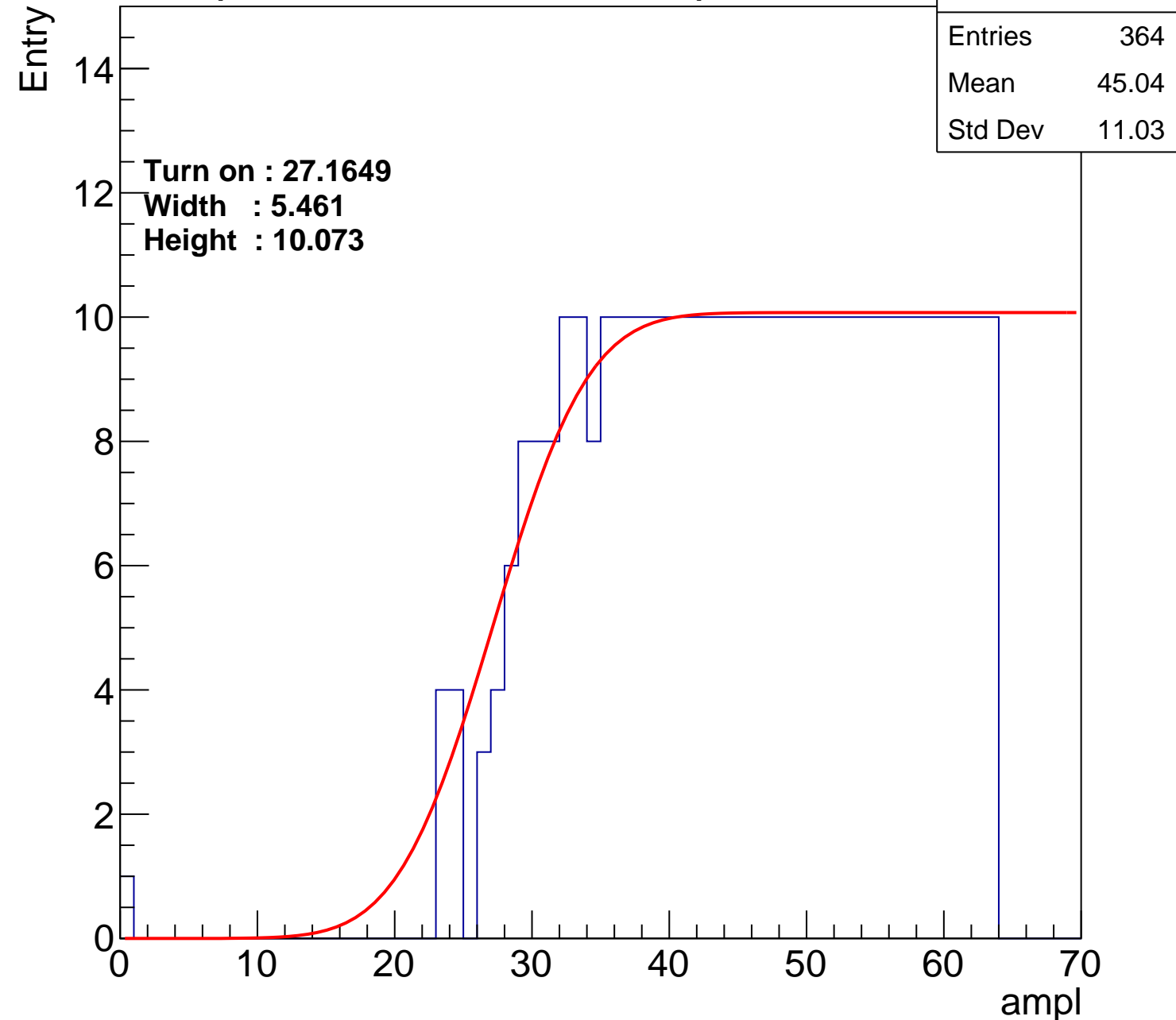
Width : 5.461

Height : 10.073

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U16-ch69

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	373
Mean	44.35
Std Dev	11.97

**Turn on : 27.2287**

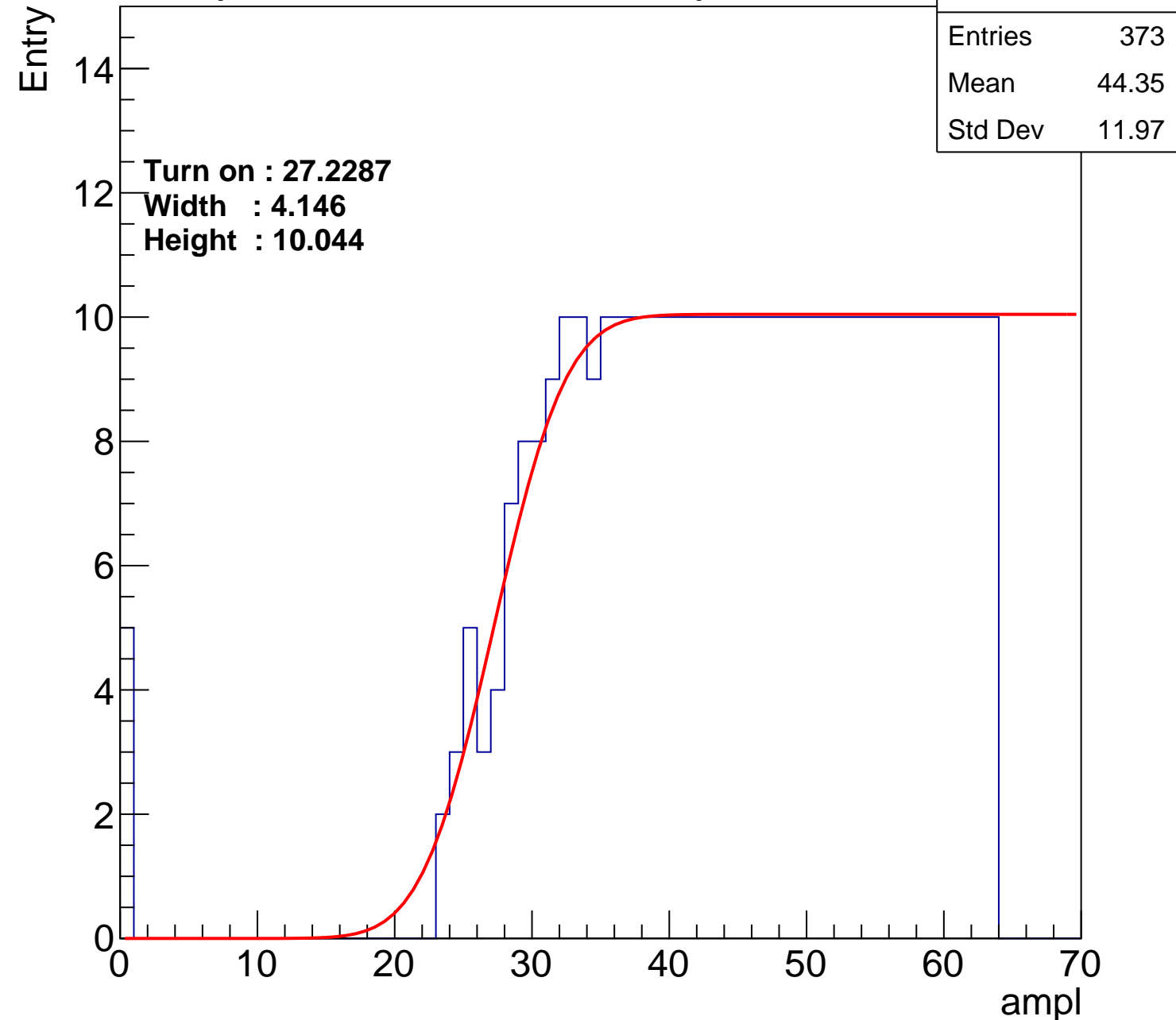
**Width : 4.146**

**Height : 10.044**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U16-ch70

calib\_packv5\_042523\_0143.root, FC#0, port D2

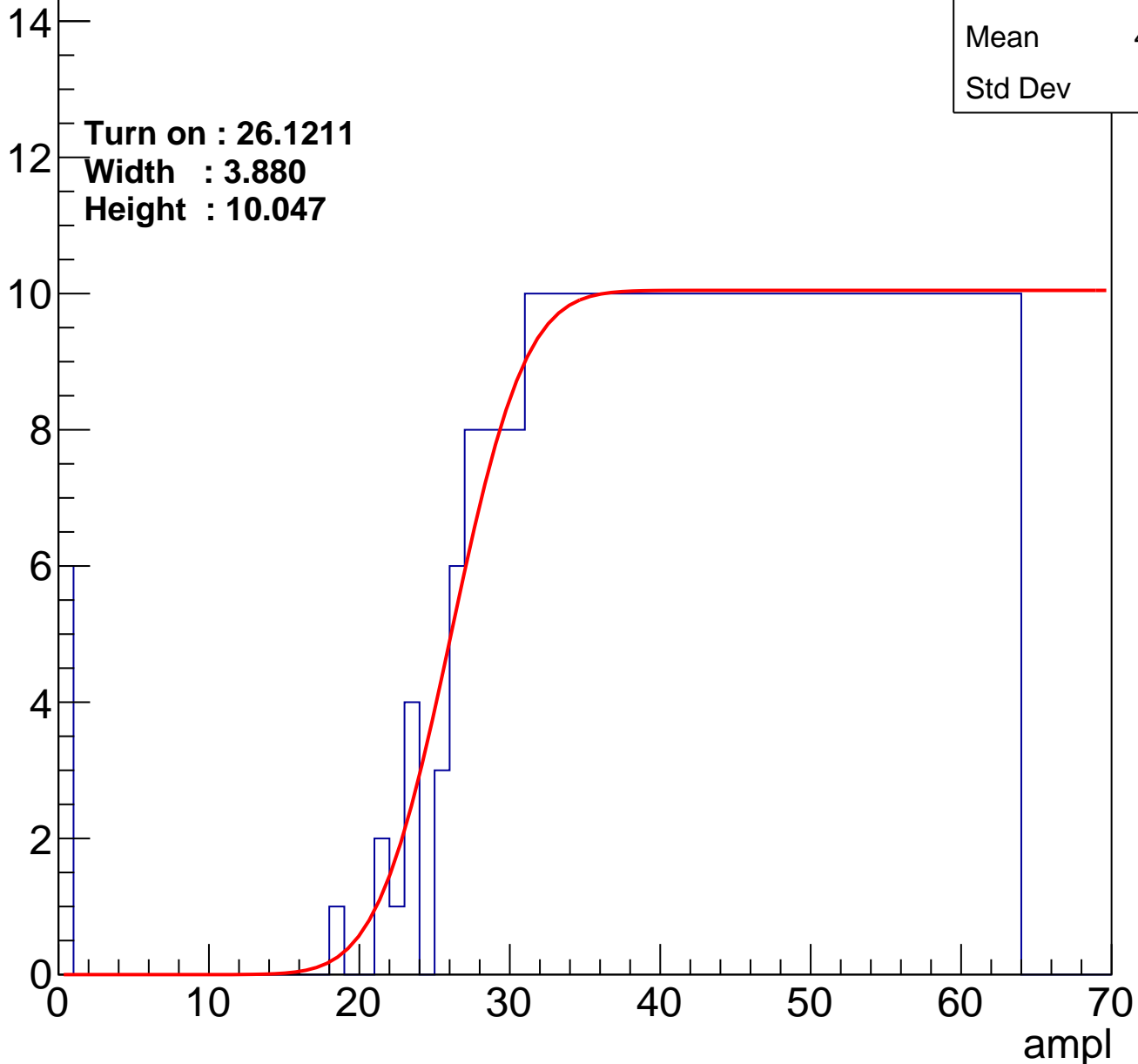
Entries	385
Mean	43.71
Std Dev	12.4

Turn on : 26.1211

Width : 3.880

Height : 10.047

Entry





# B1L101S, U16-ch71

calib\_packv5\_042523\_0143.root, FC#0, port D2

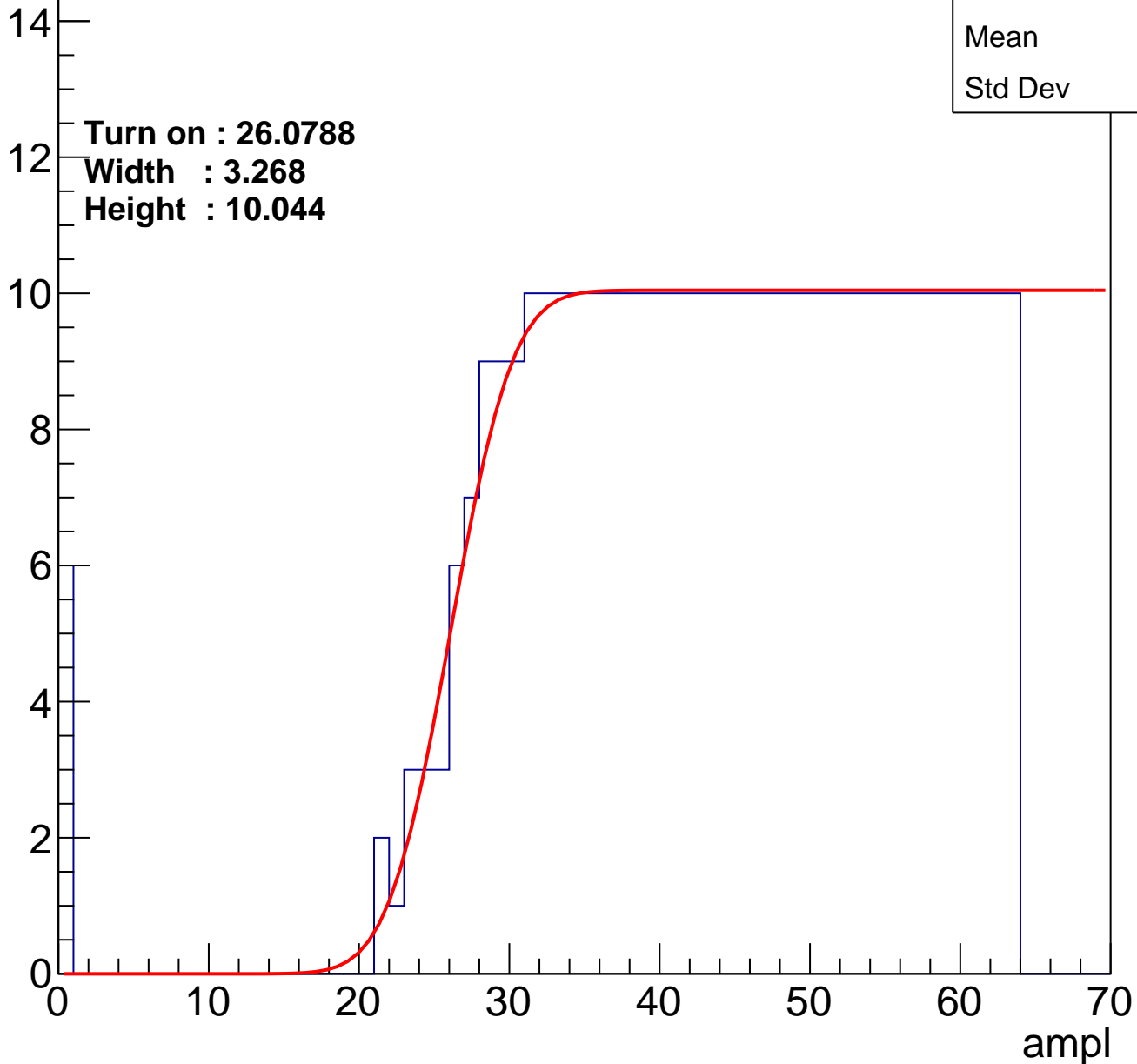
Entries	388
Mean	43.6
Std Dev	12.4

Turn on : 26.0788

Width : 3.268

Height : 10.044

Entry



# B1L101S, U16-ch72

calib\_packv5\_042523\_0143.root, FC#0, port D2

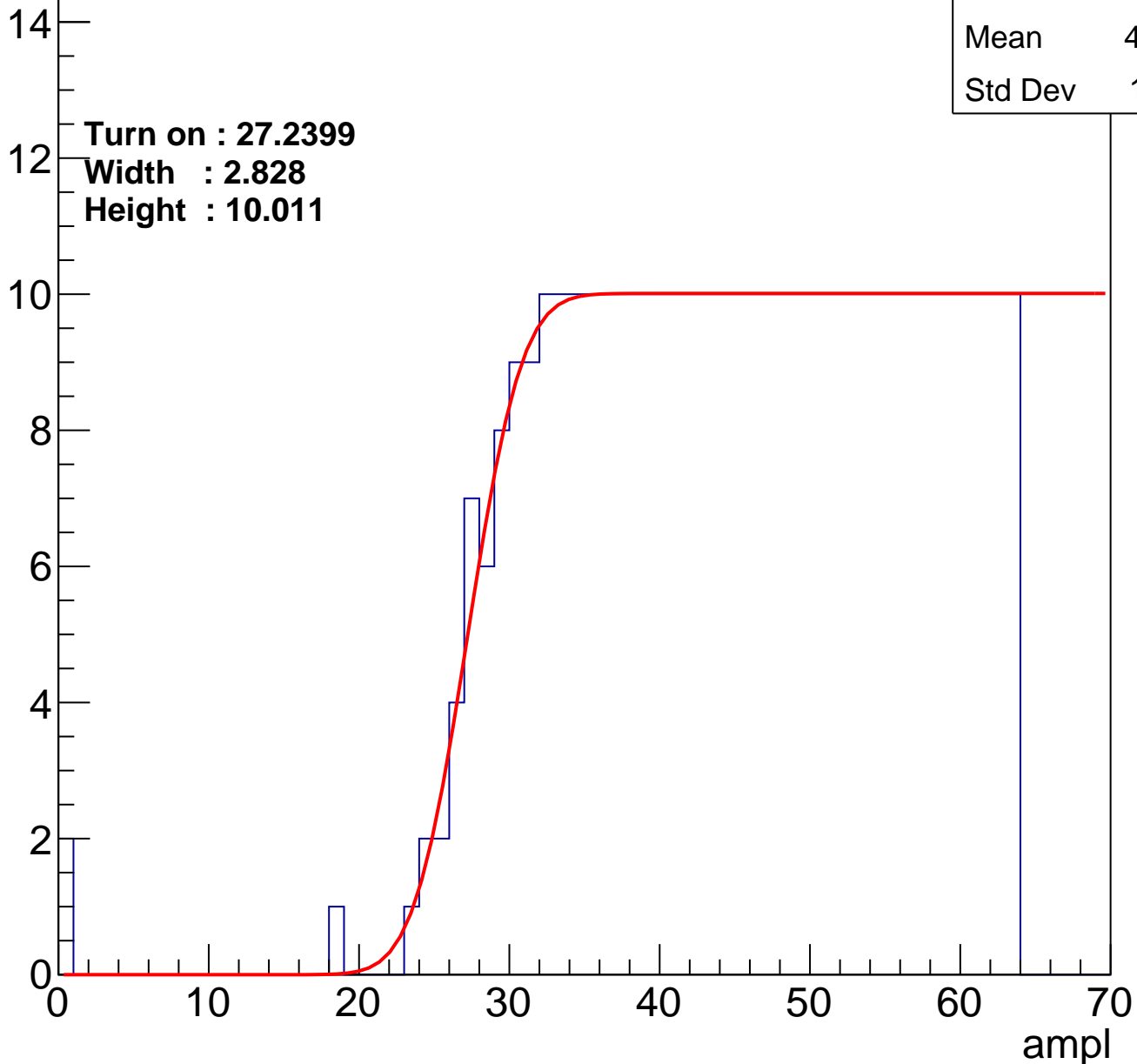
Entries	371
Mean	44.69
Std Dev	11.31

Turn on : 27.2399

Width : 2.828

Height : 10.011

Entry



# B1L101S, U16-ch73

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	355
Mean	45.48
Std Dev	10.9

Turn on : 28.8772

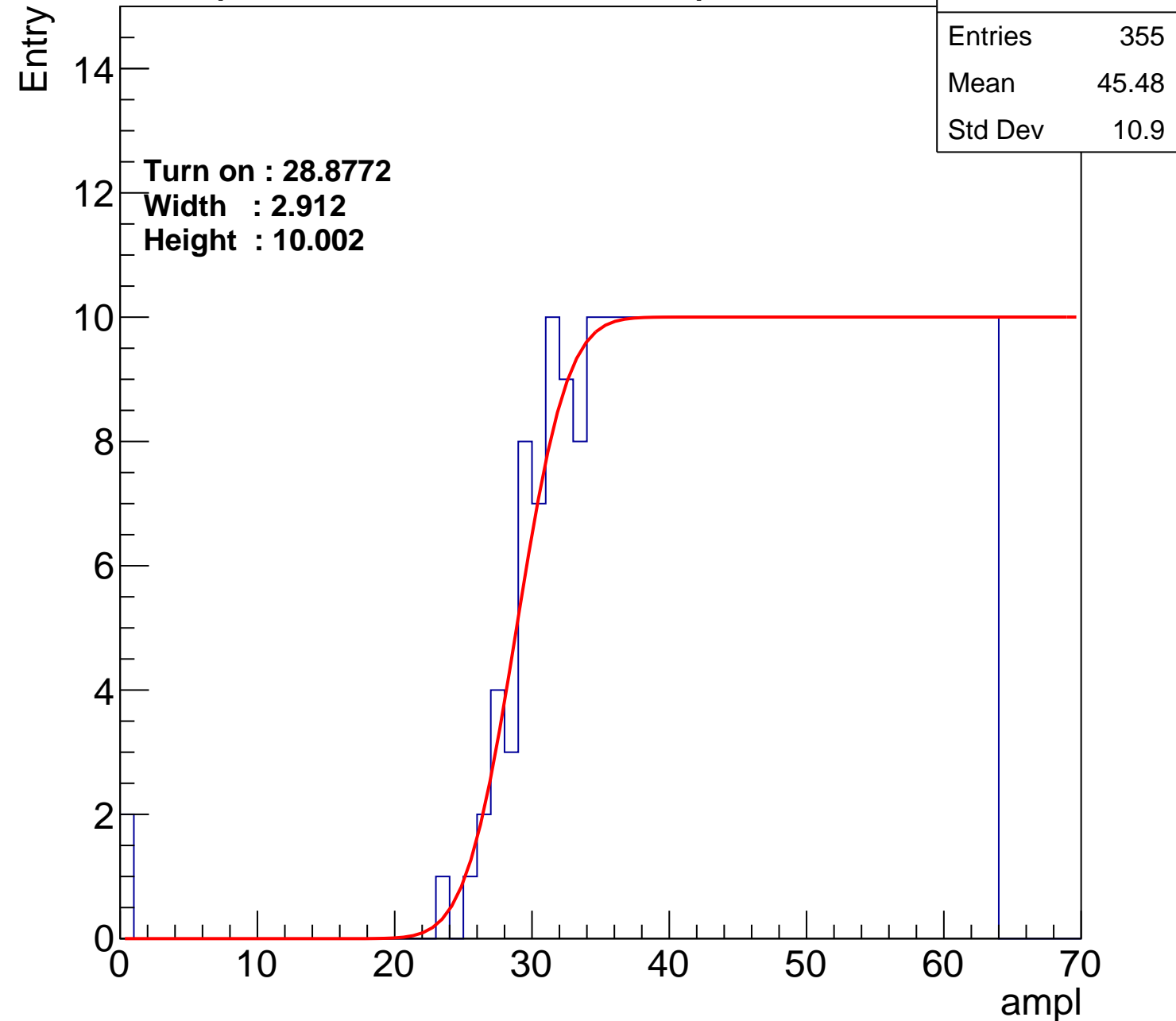
Width : 2.912

Height : 10.002

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U16-ch74

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	377
Mean	44.25
Std Dev	11.84

Turn on : 26.6807

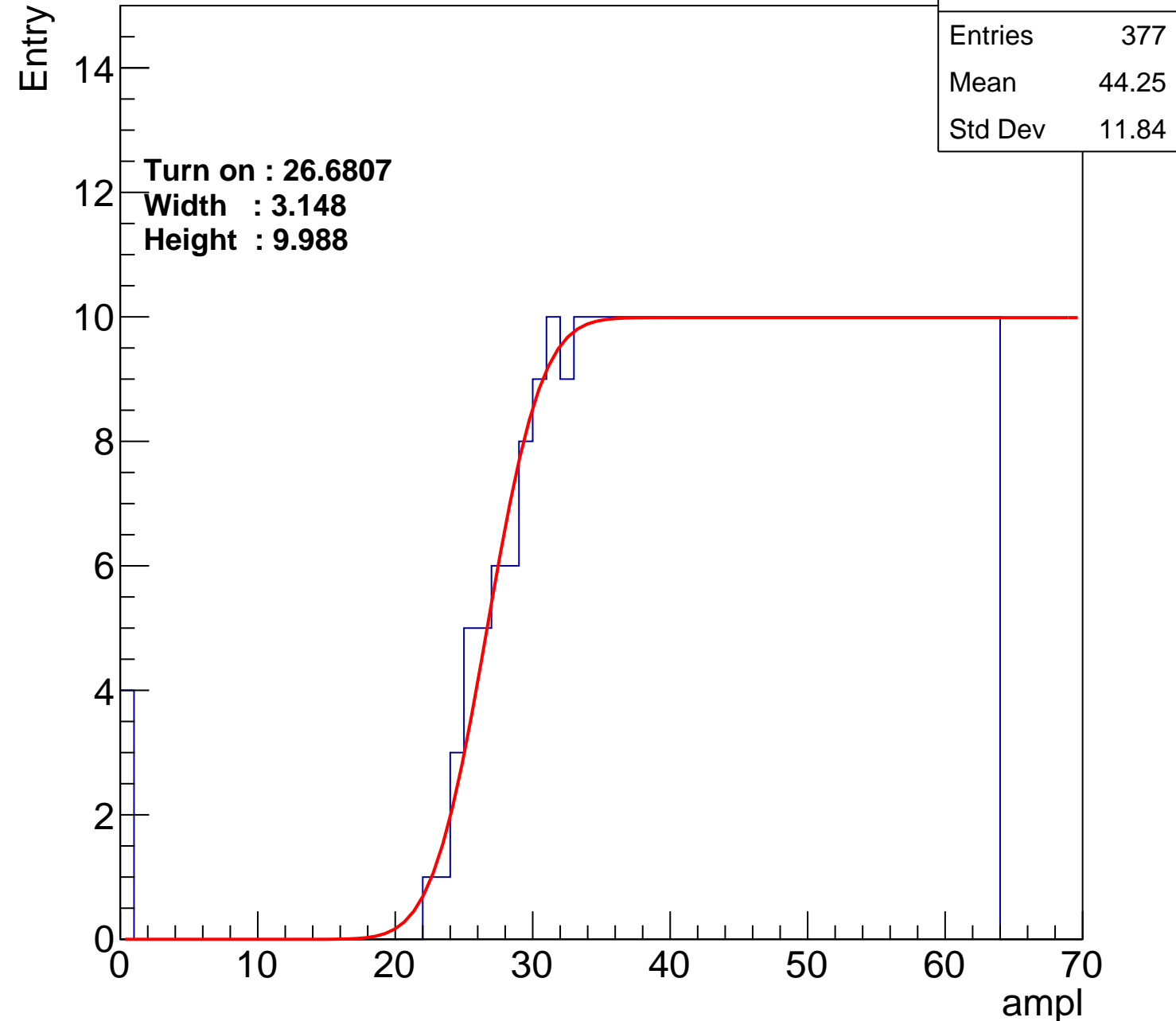
Width : 3.148

Height : 9.988

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U16-ch75

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	369
Mean	44.87
Std Dev	11.04

Turn on : 27.4686

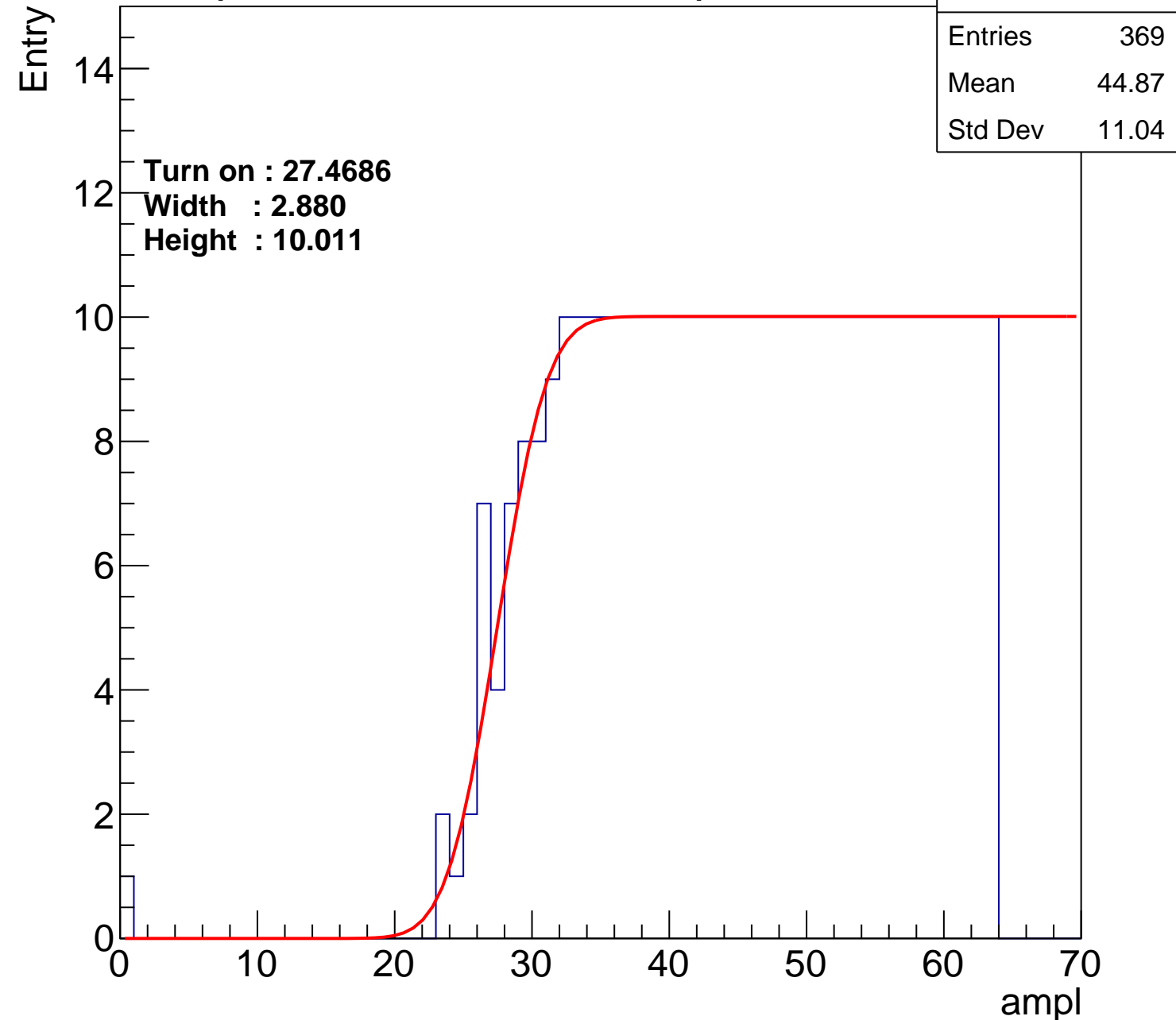
Width : 2.880

Height : 10.011

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U16-ch76

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	386
Mean	43.92
Std Dev	11.76

**Turn on : 25.9794**

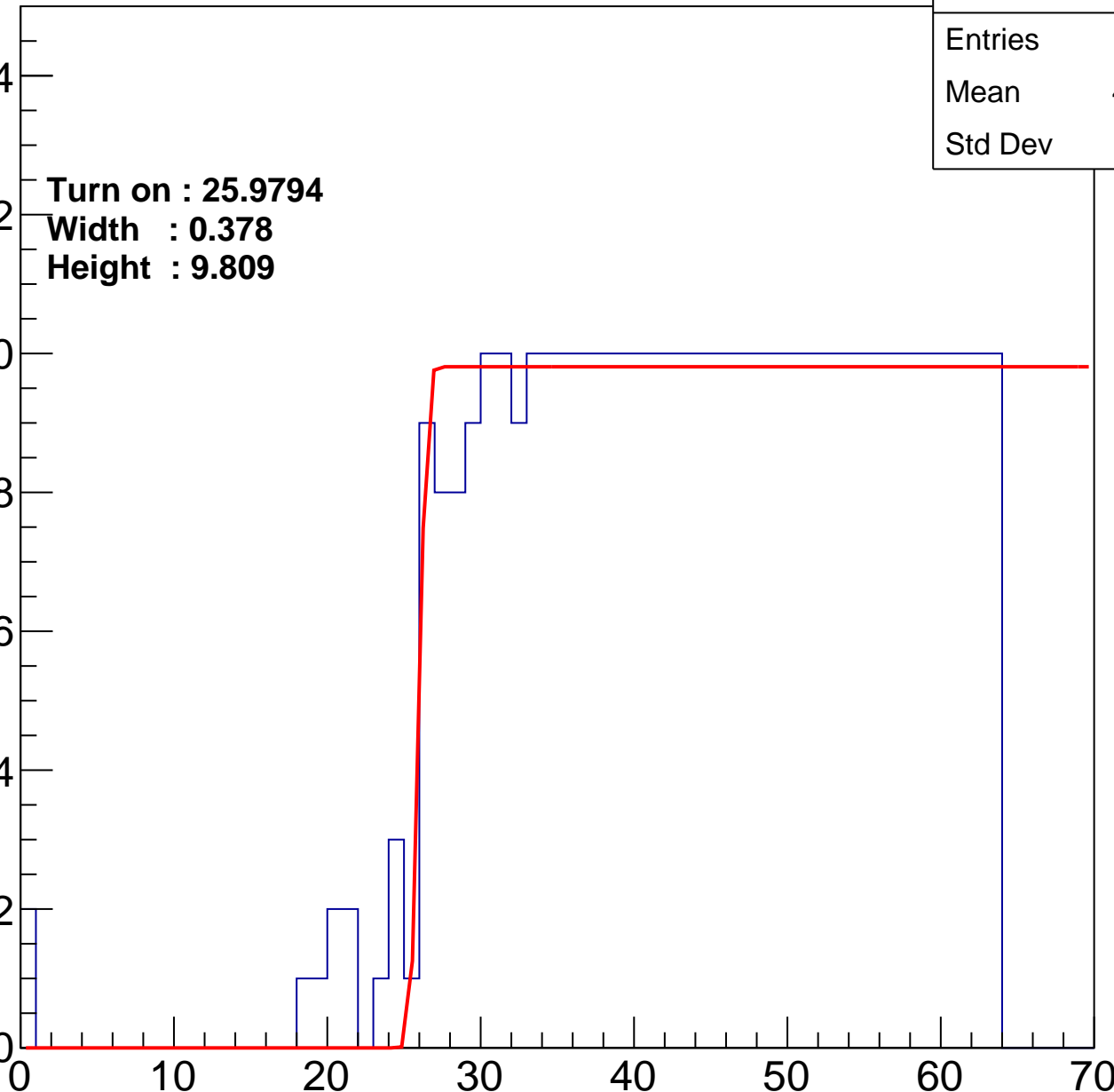
**Width : 0.378**

**Height : 9.809**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U16-ch77

calib\_packv5\_042523\_0143.root, FC#0, port D2

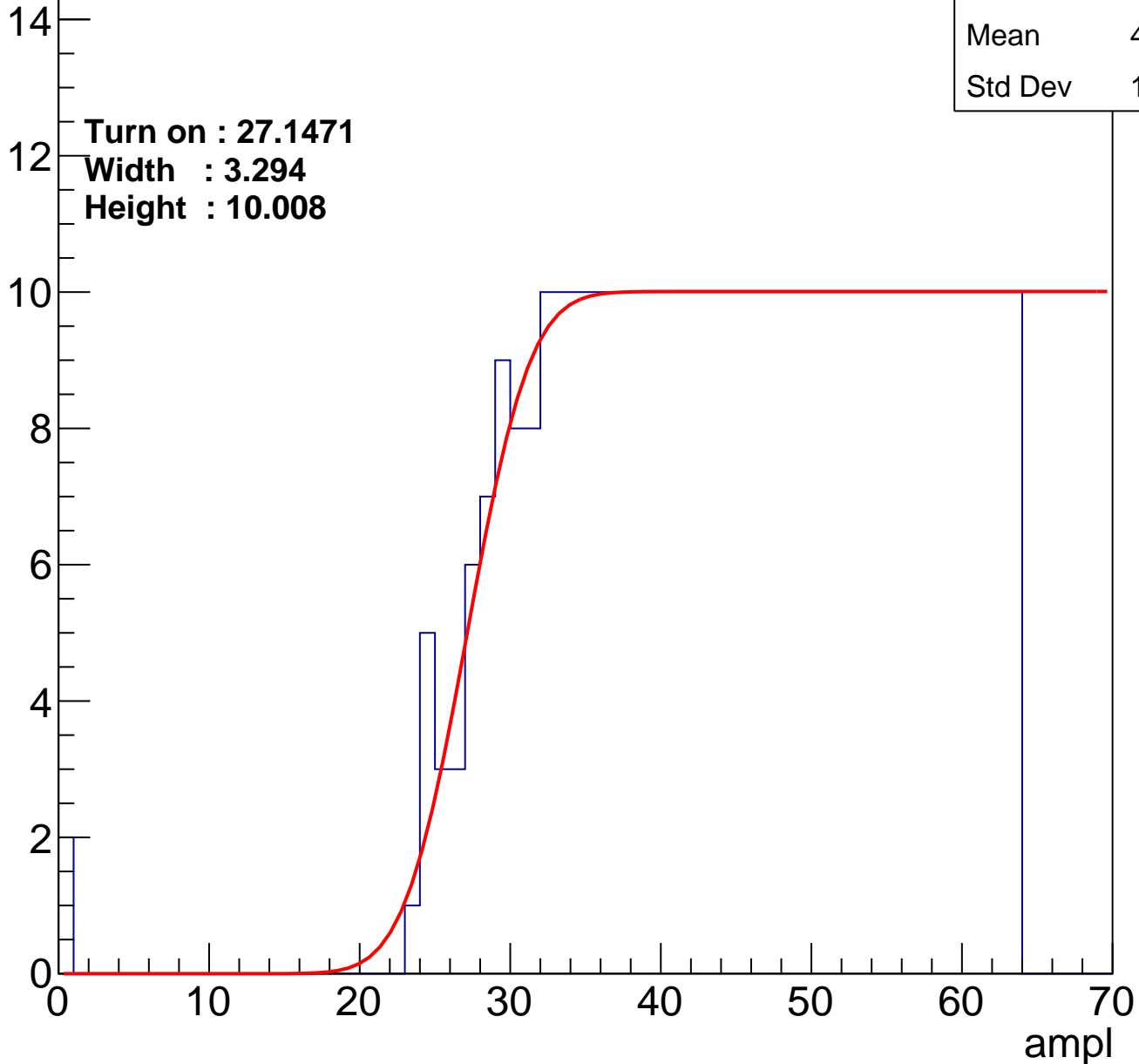
Entries	372
Mean	44.63
Std Dev	11.35

Turn on : 27.1471

Width : 3.294

Height : 10.008

Entry



# B1L101S, U16-ch78

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	374
Mean	44.6
Std Dev	11.3

Turn on : 27.1013

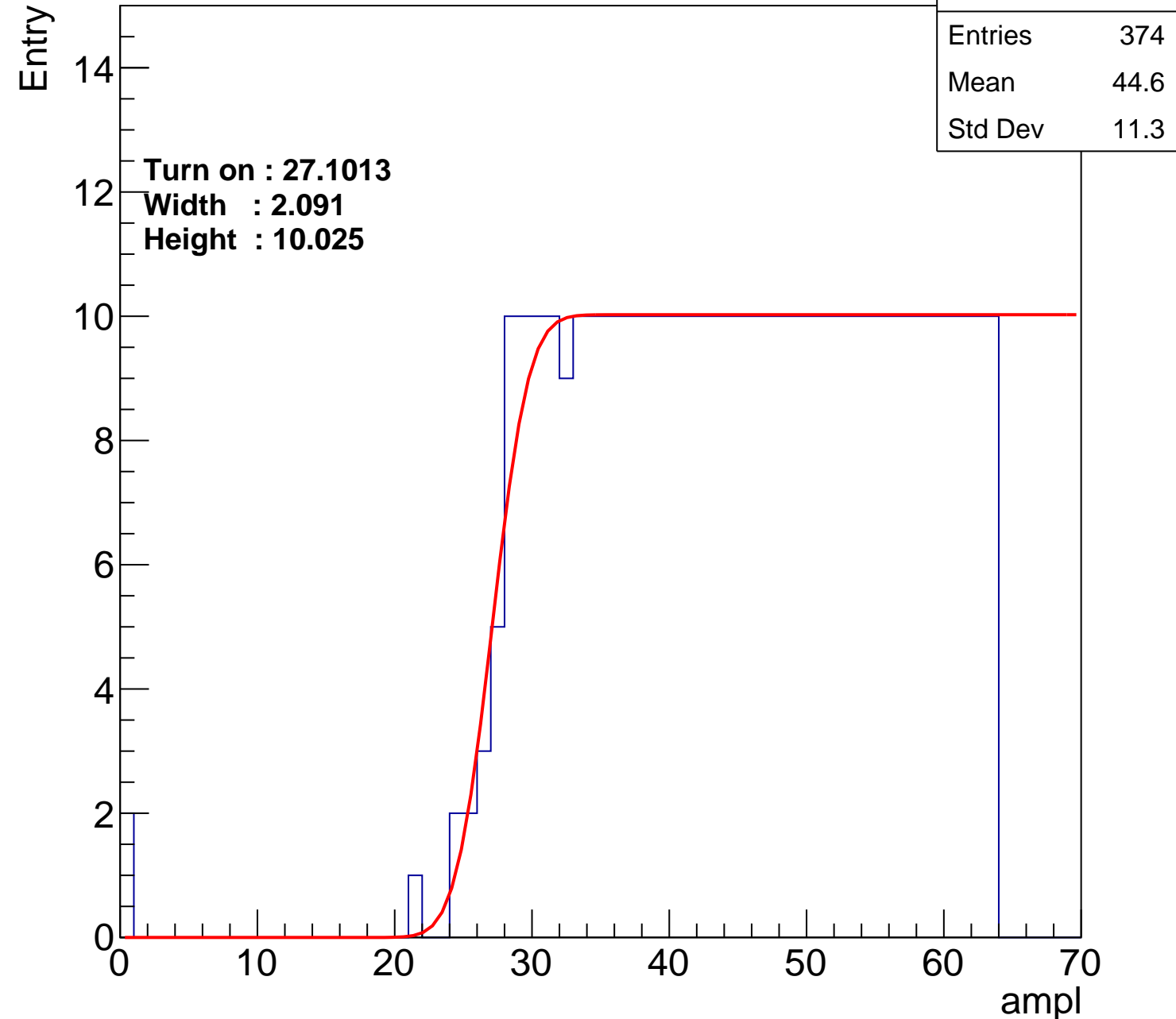
Width : 2.091

Height : 10.025

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L101S, U16-ch79

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	384
Mean	44.01
Std Dev	11.71

Turn on : 26.1936

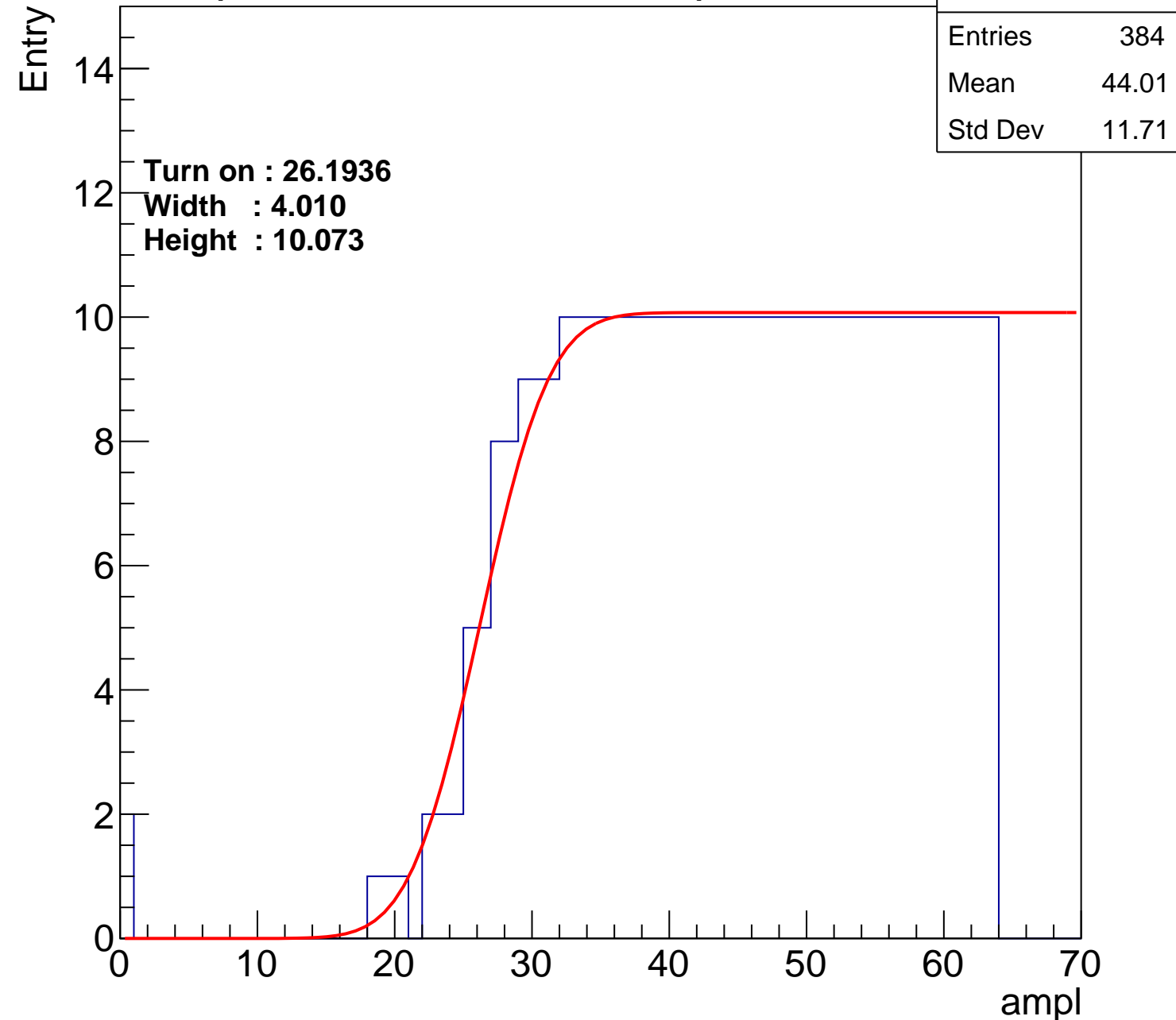
Width : 4.010

Height : 10.073

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U16-ch80

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	383
Mean	43.89
Std Dev	12.16

Turn on : 26.6445

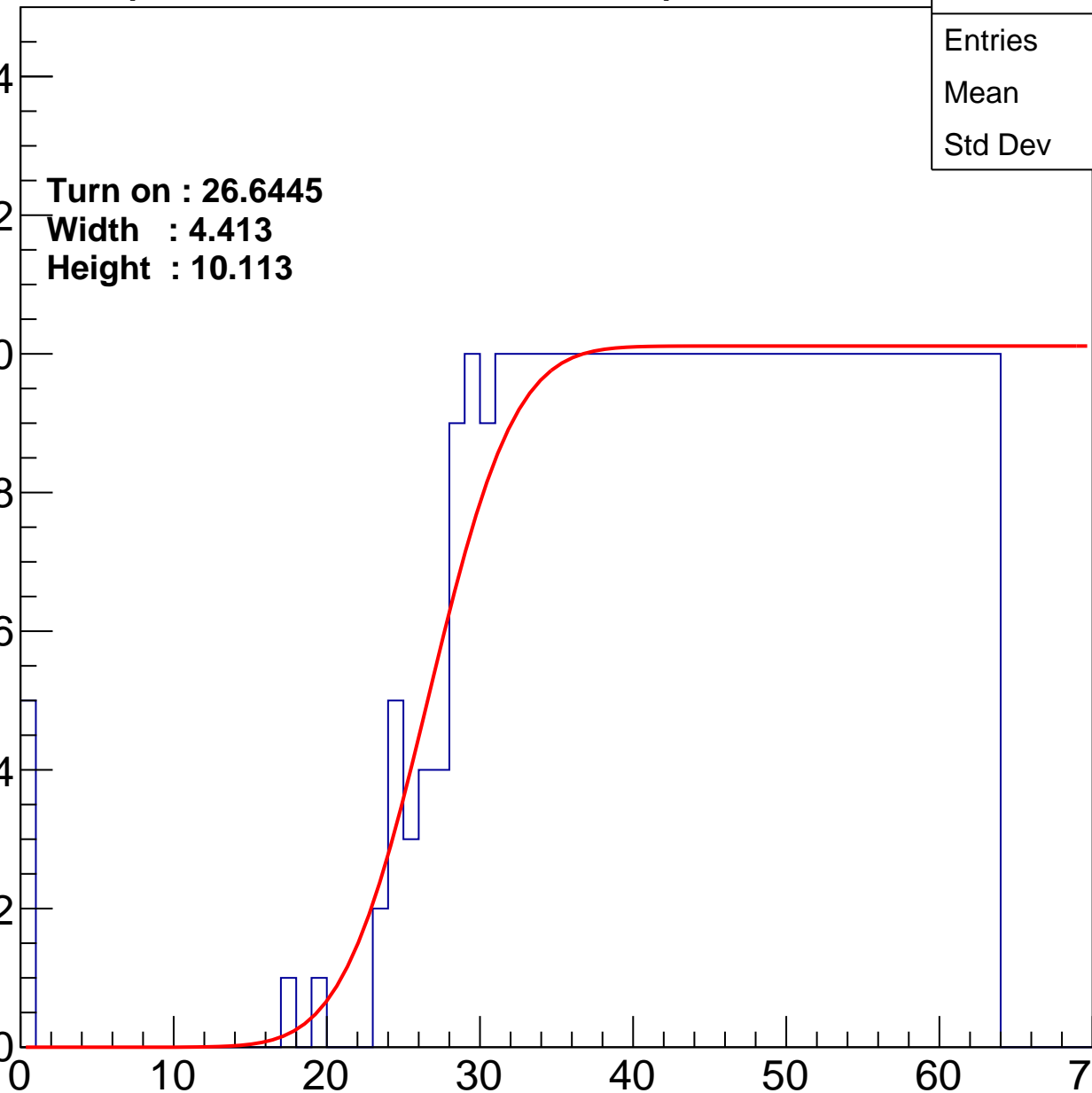
Width : 4.413

Height : 10.113

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U16-ch81

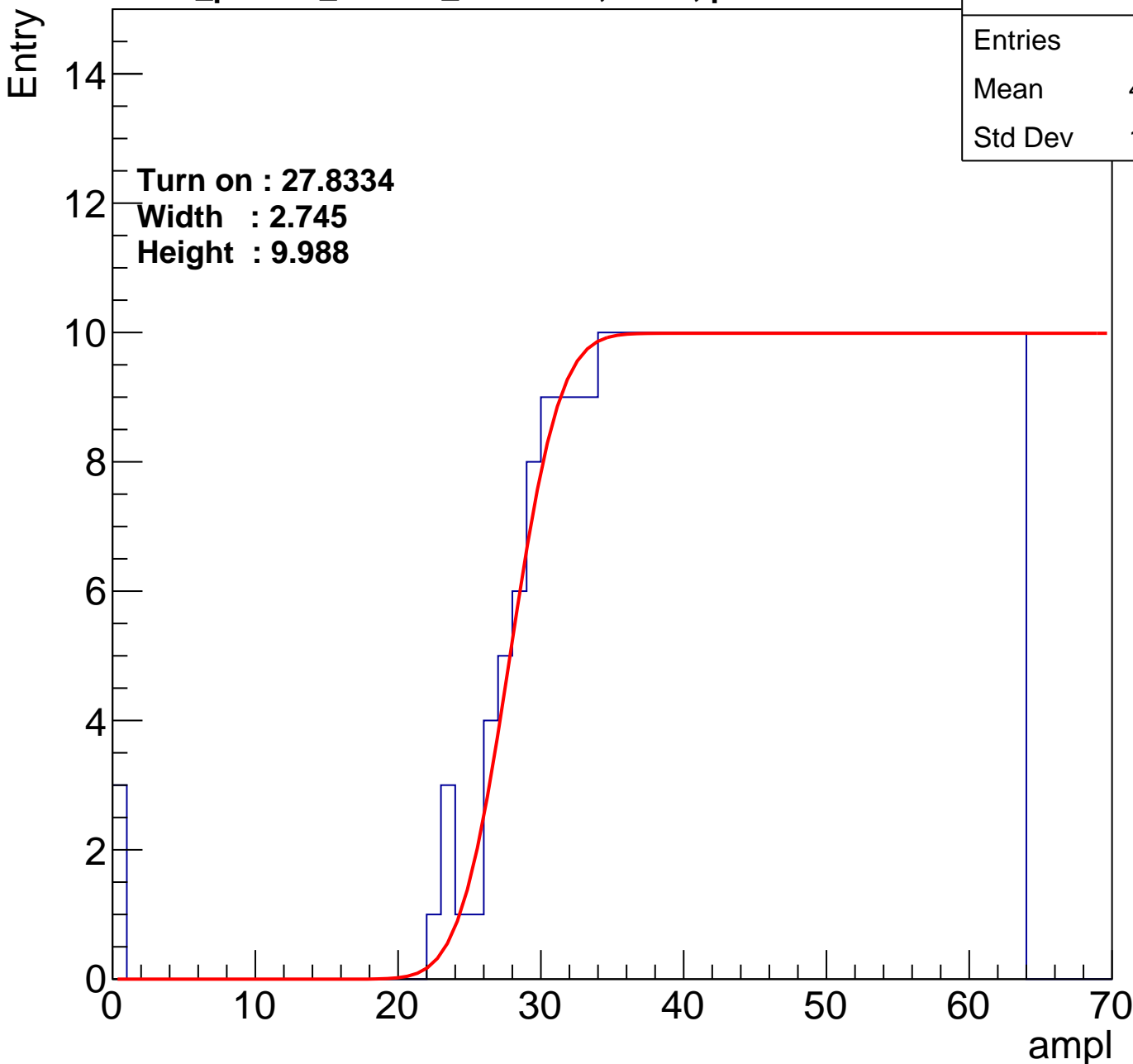
**calib\_packv5\_042523\_0143.root, FC#0, port D2**

Entries	368
Mean	44.74
Std Dev	11.48

**Turn on : 27.8334**

**Width : 2.745**

**Height : 9.988**



# B1L101S, U16-ch82

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	389
Mean	43.69
Std Dev	12.08

Turn on : 25.3310

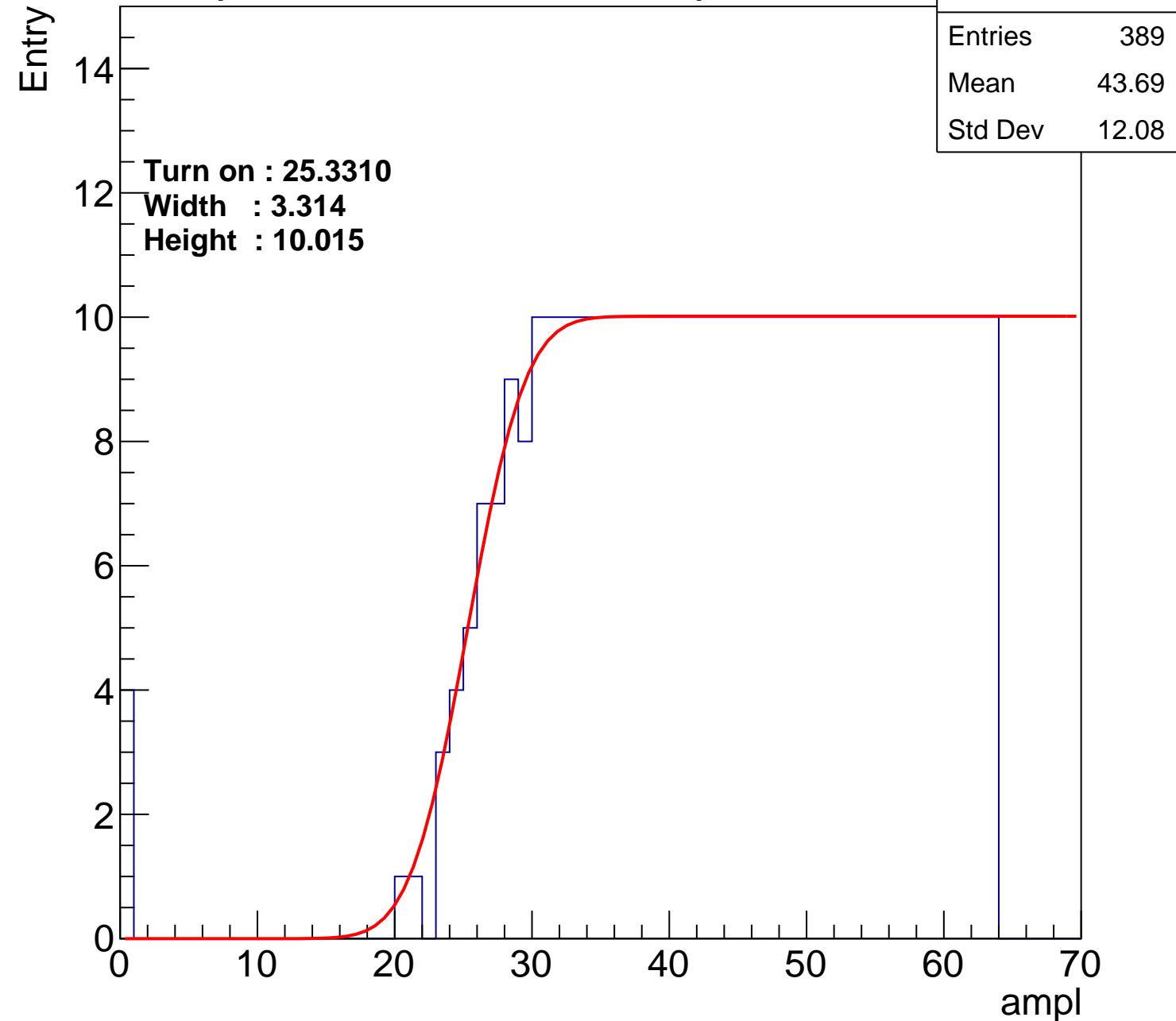
Width : 3.314

Height : 10.015

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U16-ch83

calib\_packv5\_042523\_0143.root, FC#0, port D2

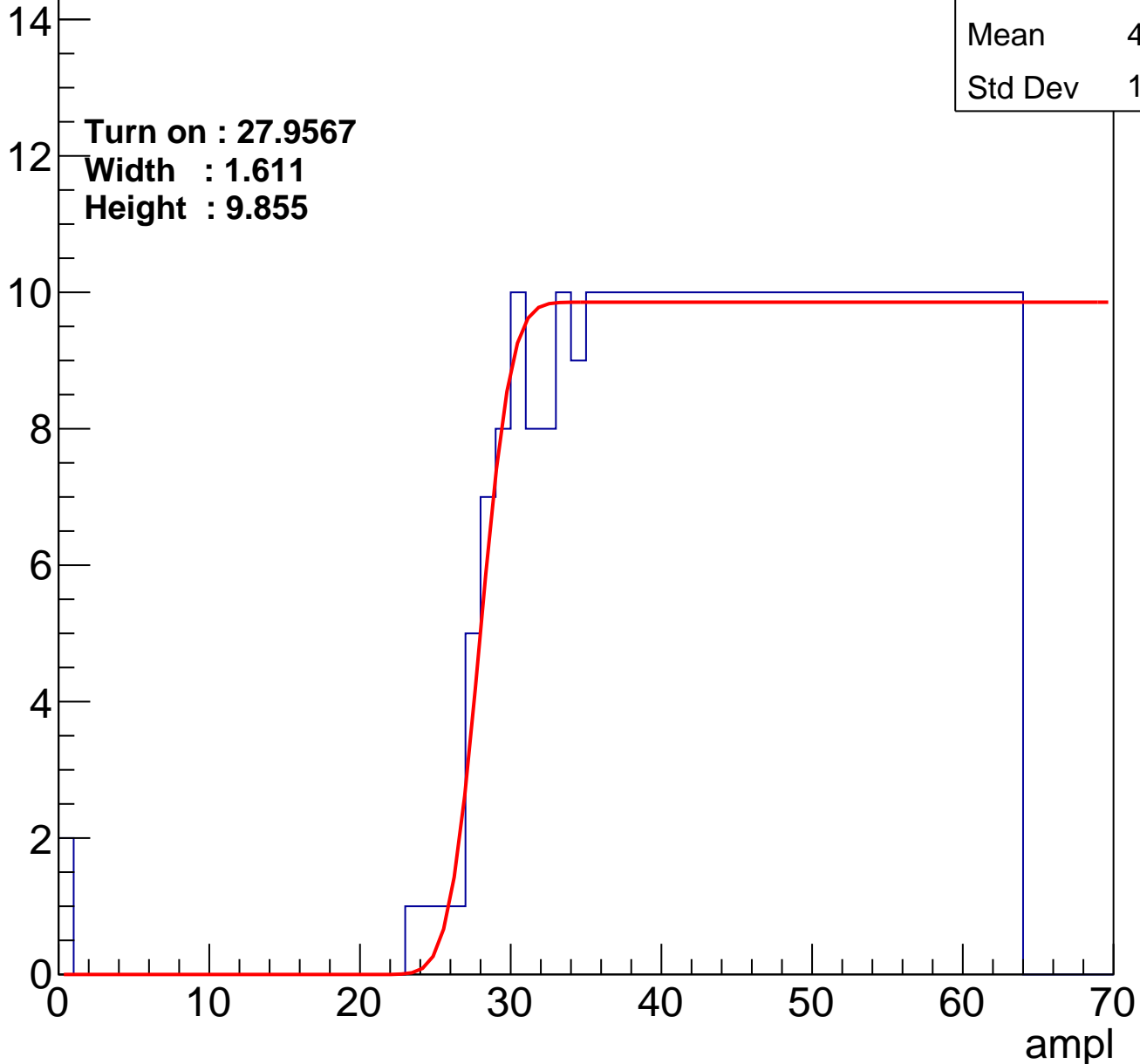
Entries	361
Mean	45.18
Std Dev	11.05

**Turn on : 27.9567**

**Width : 1.611**

**Height : 9.855**

Entry



# B1L101S, U16-ch84

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

14

12

10

8

6

4

2

0

Turn on : 26.5787

Width : 3.022

Height : 9.944

Entries	374
Mean	44.59
Std Dev	11.21

ampl

0

10

20

30

40

50

60

70

# B1L101S, U16-ch85

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	360
Mean	45.1
Std Dev	11.32

Turn on : 28.3443

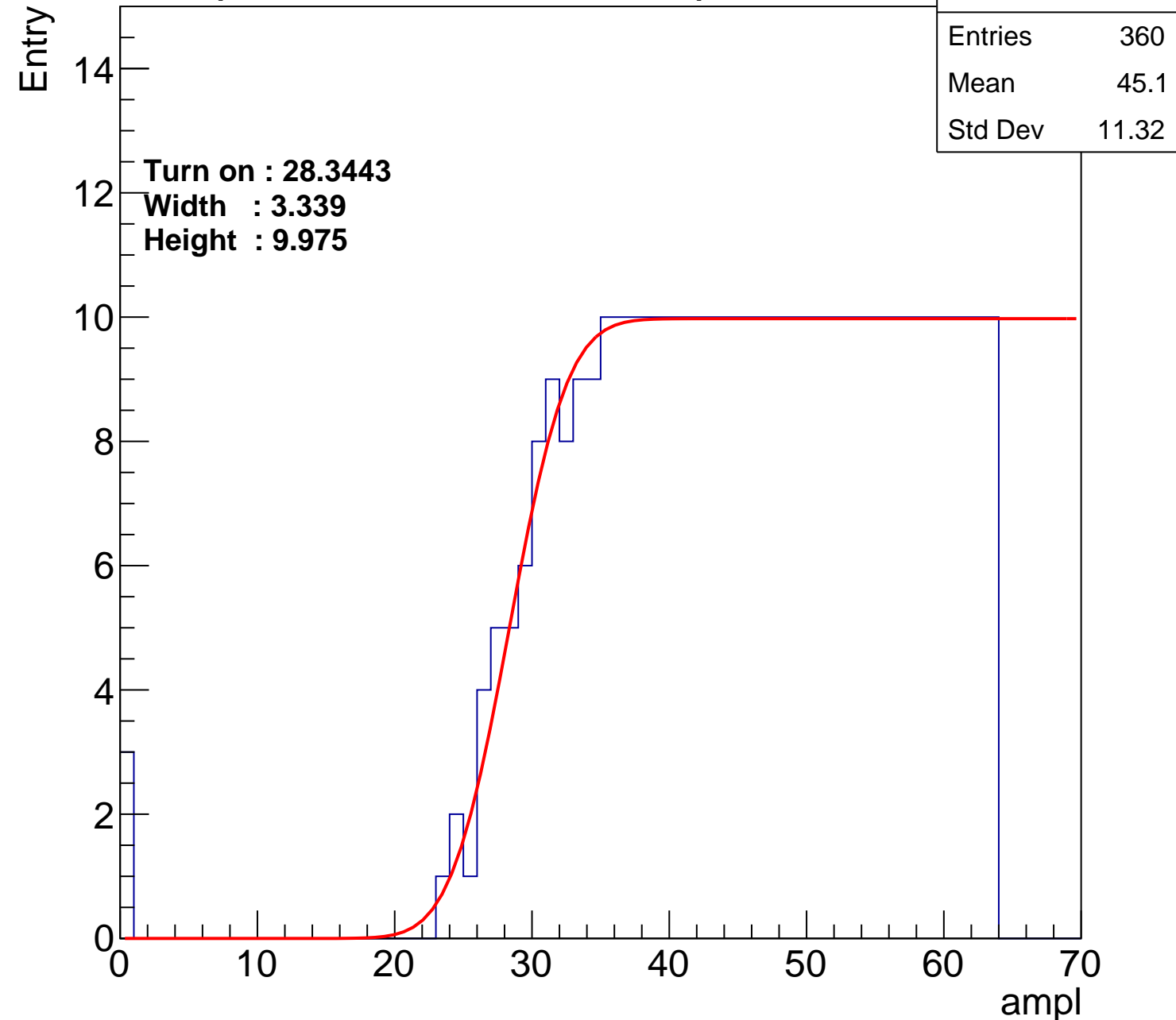
Width : 3.339

Height : 9.975

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U16-ch86

calib\_packv5\_042523\_0143.root, FC#0, port D2

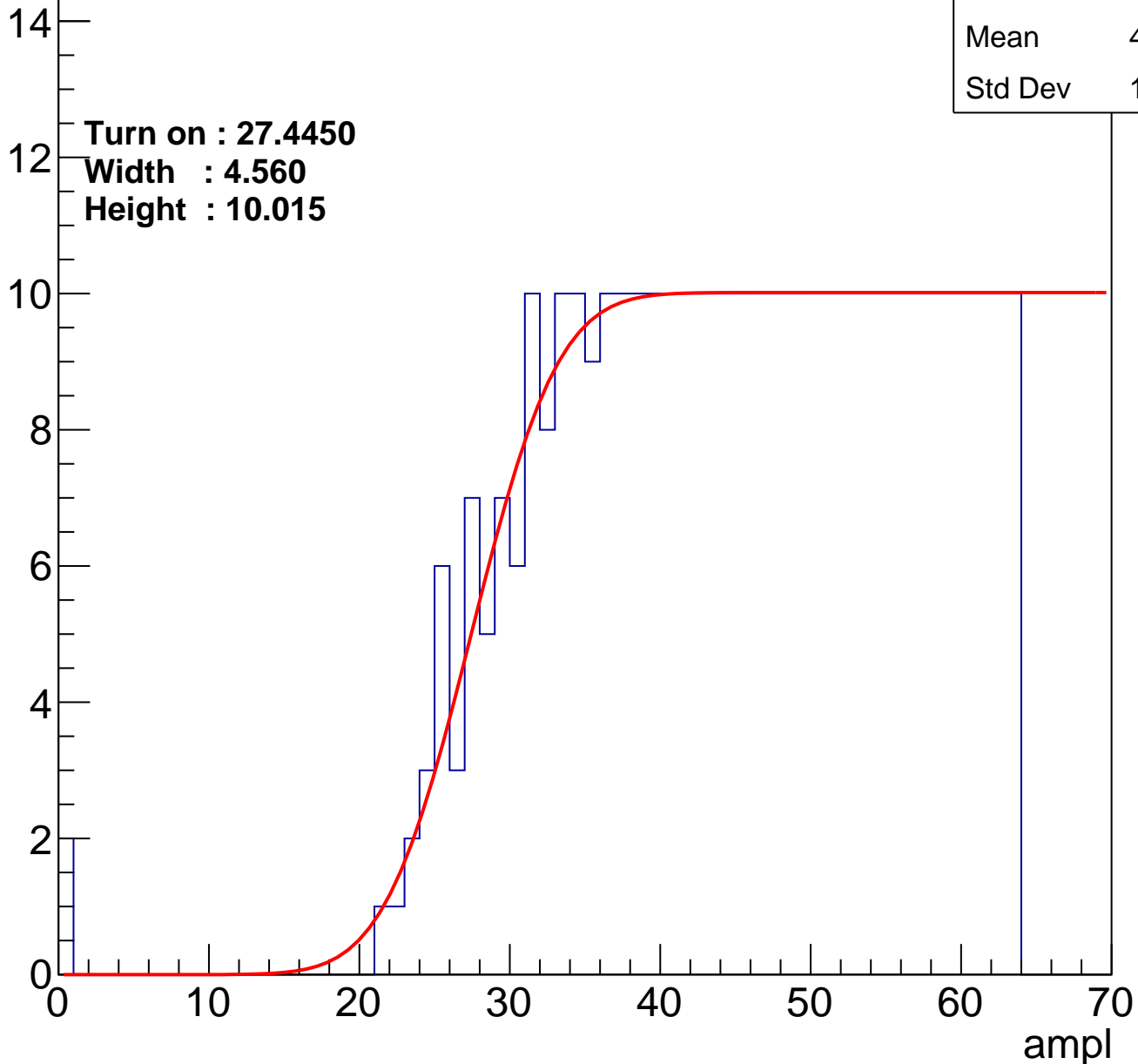
Entries	370
Mean	44.63
Std Dev	11.45

Turn on : 27.4450

Width : 4.560

Height : 10.015

Entry





# B1L101S, U16-ch87

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	355
Mean	45.25
Std Dev	11.55

Turn on : 29.0821

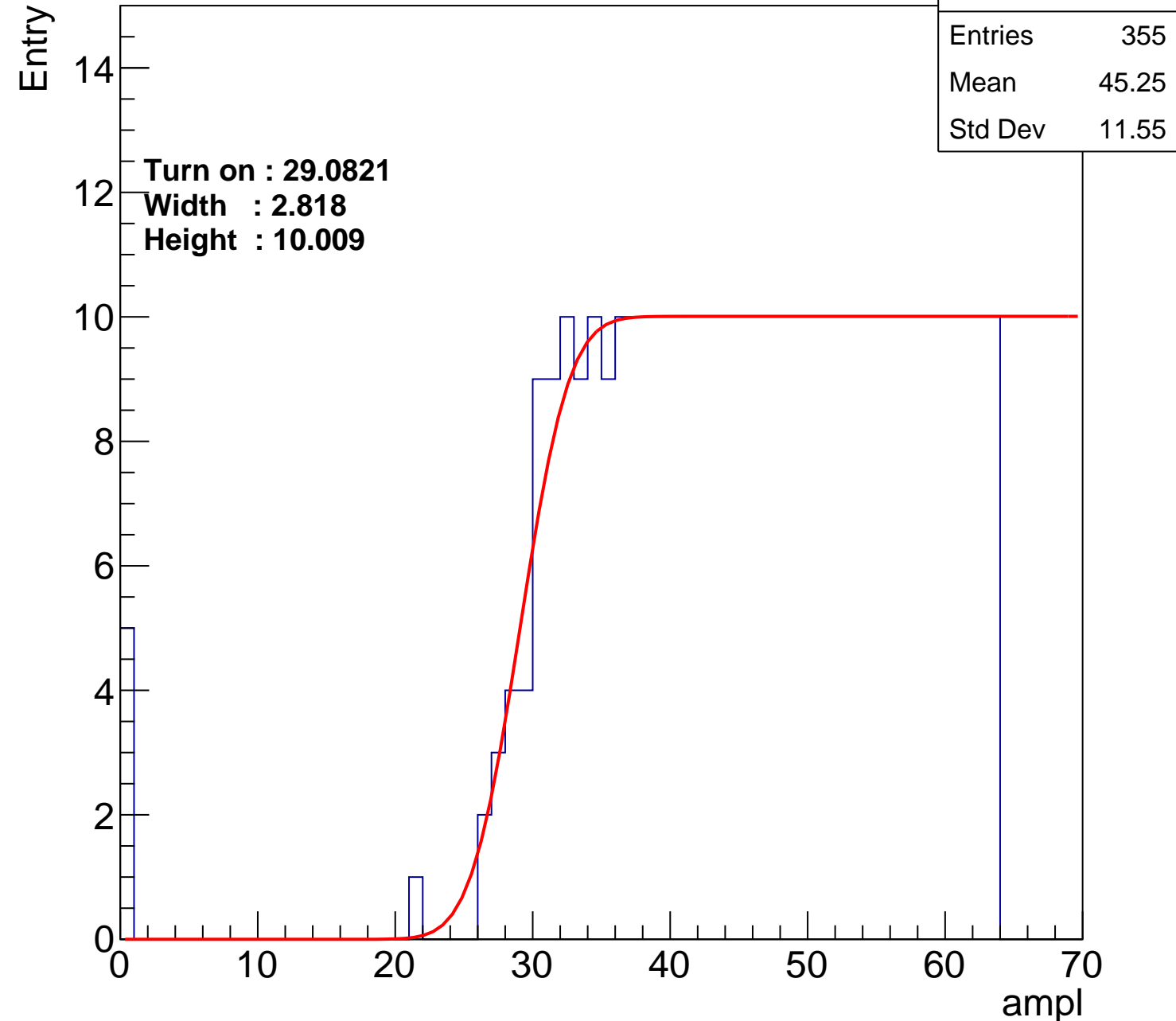
Width : 2.818

Height : 10.009

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U16-ch88

calib\_packv5\_042523\_0143.root, FC#0, port D2

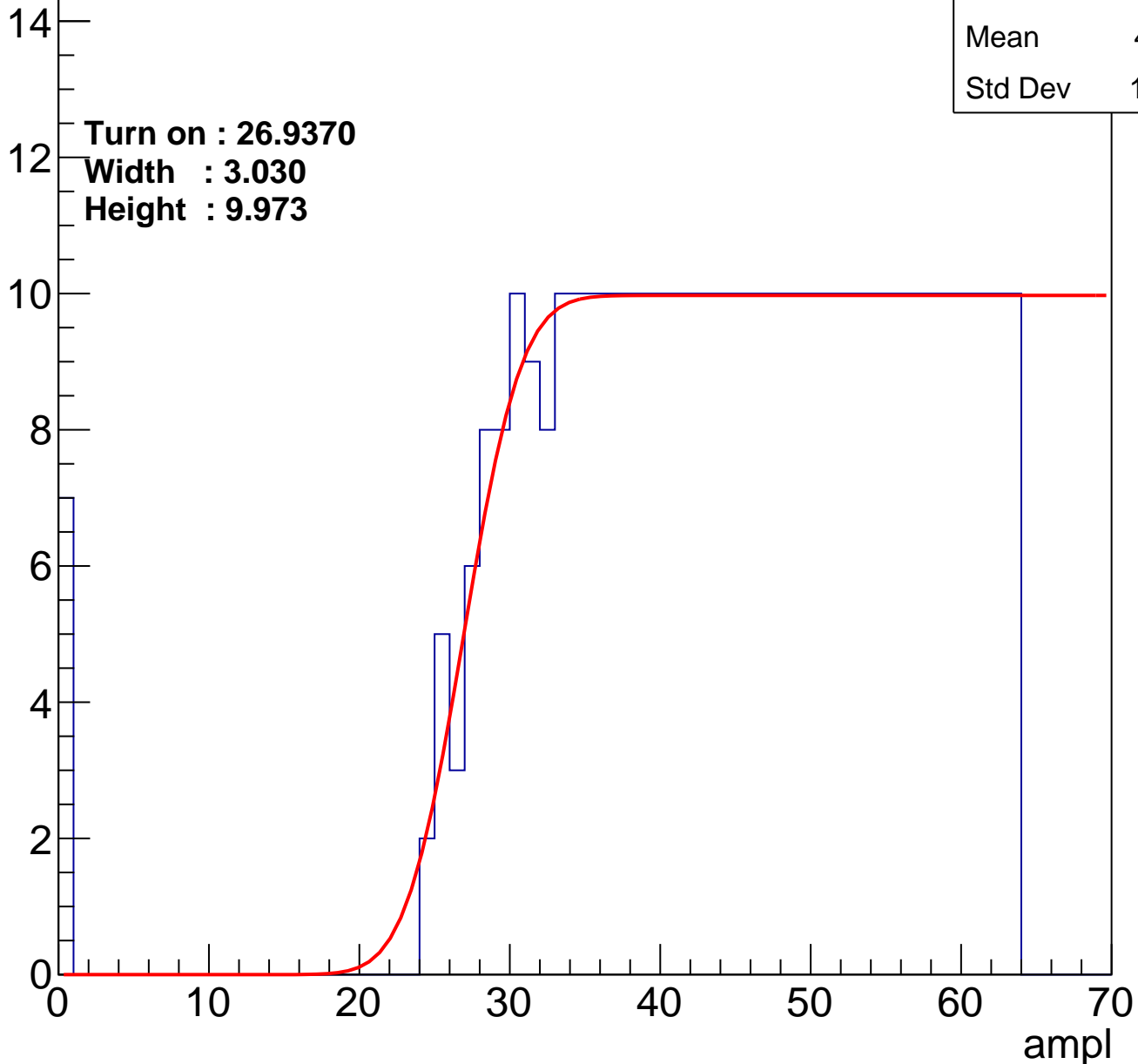
Entries	376
Mean	44.11
Std Dev	12.32

Turn on : 26.9370

Width : 3.030

Height : 9.973

Entry



# B1L101S, U16-ch89

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	384
Mean	43.97
Std Dev	11.84

Turn on : 26.1614

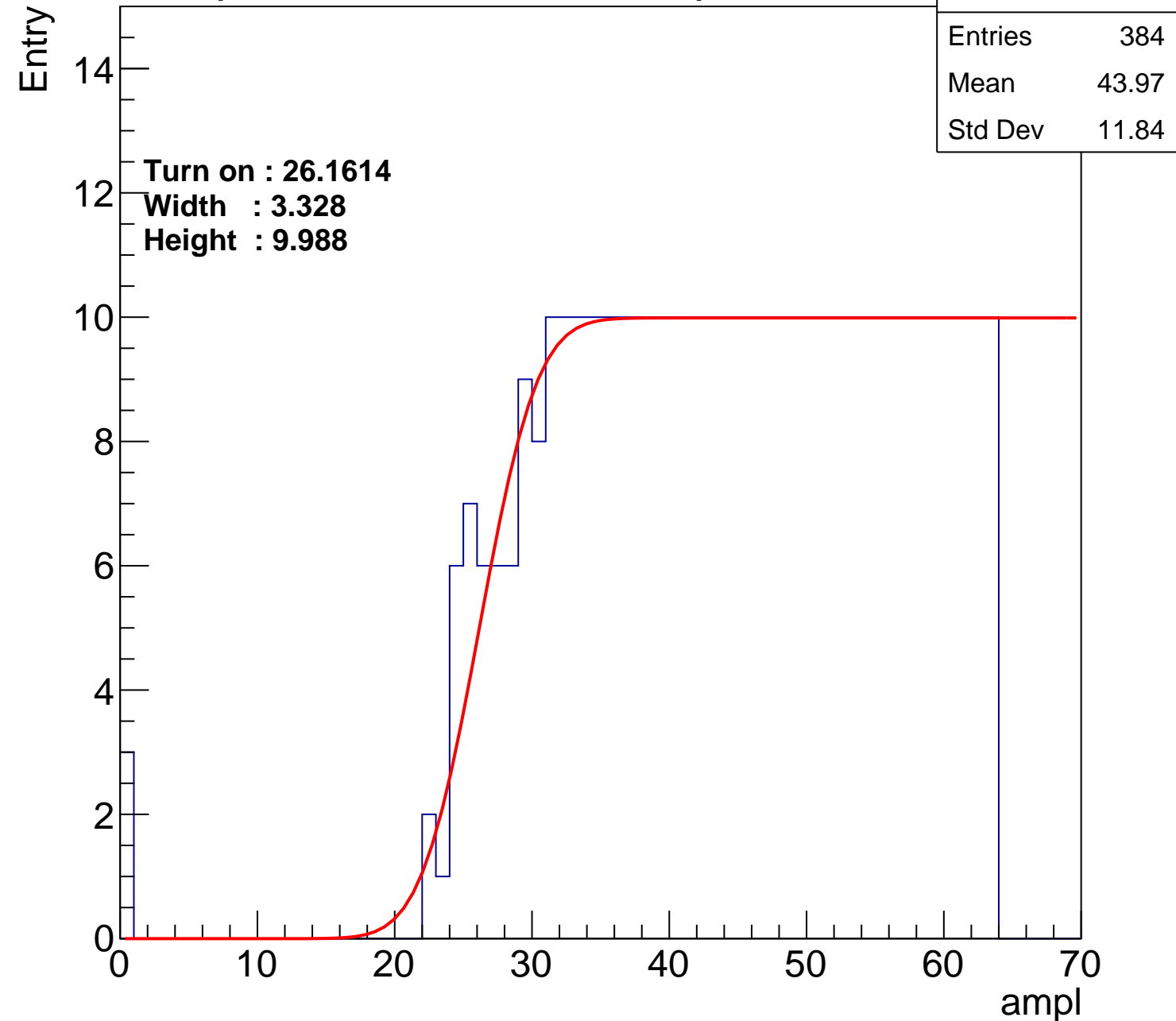
Width : 3.328

Height : 9.988

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U16-ch90

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	359
Mean	45.29
Std Dev	11

Turn on : 28.7622

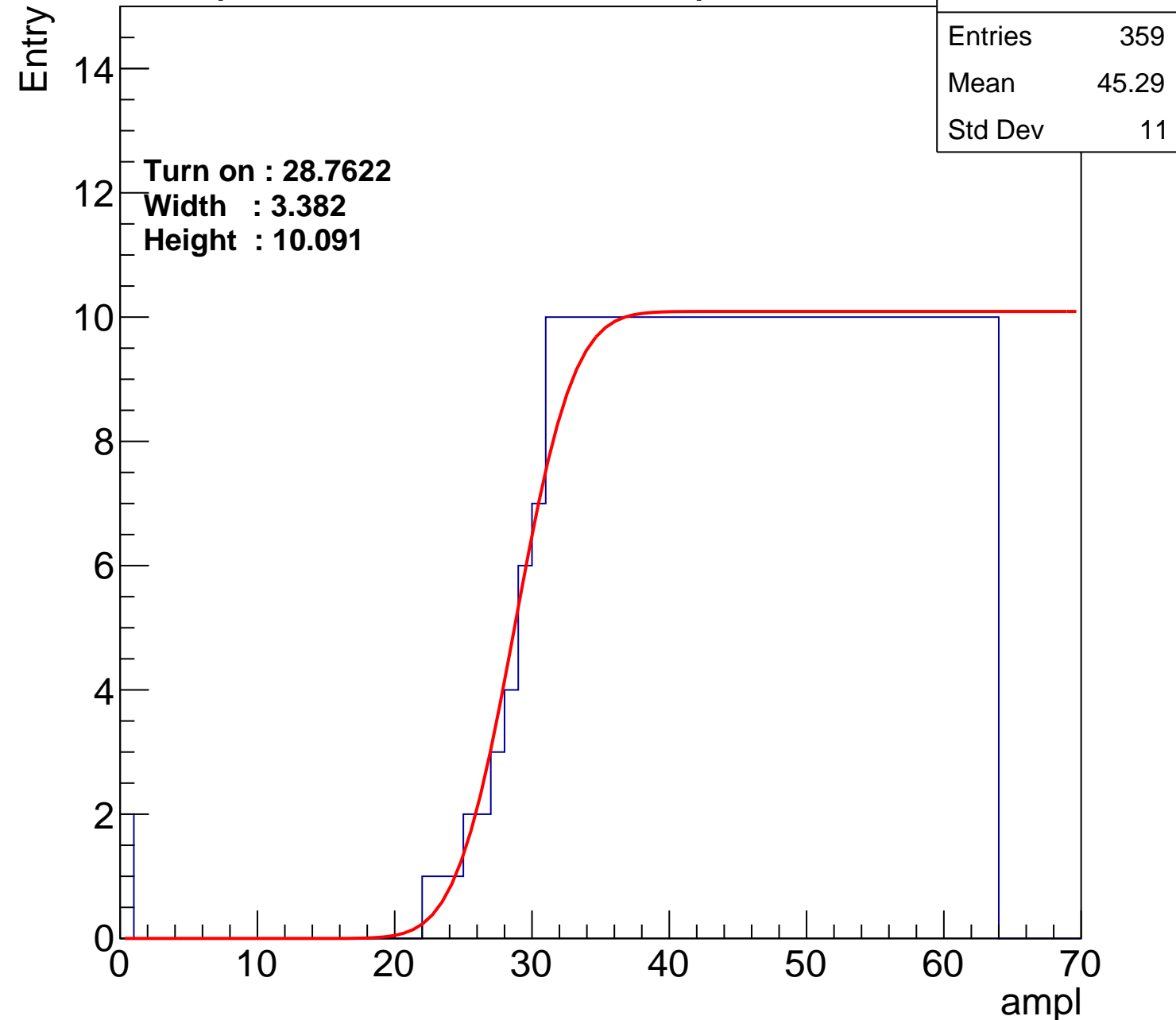
Width : 3.382

Height : 10.091

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U16-ch91

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	388
Mean	43.79
Std Dev	11.91

Turn on : 25.7335

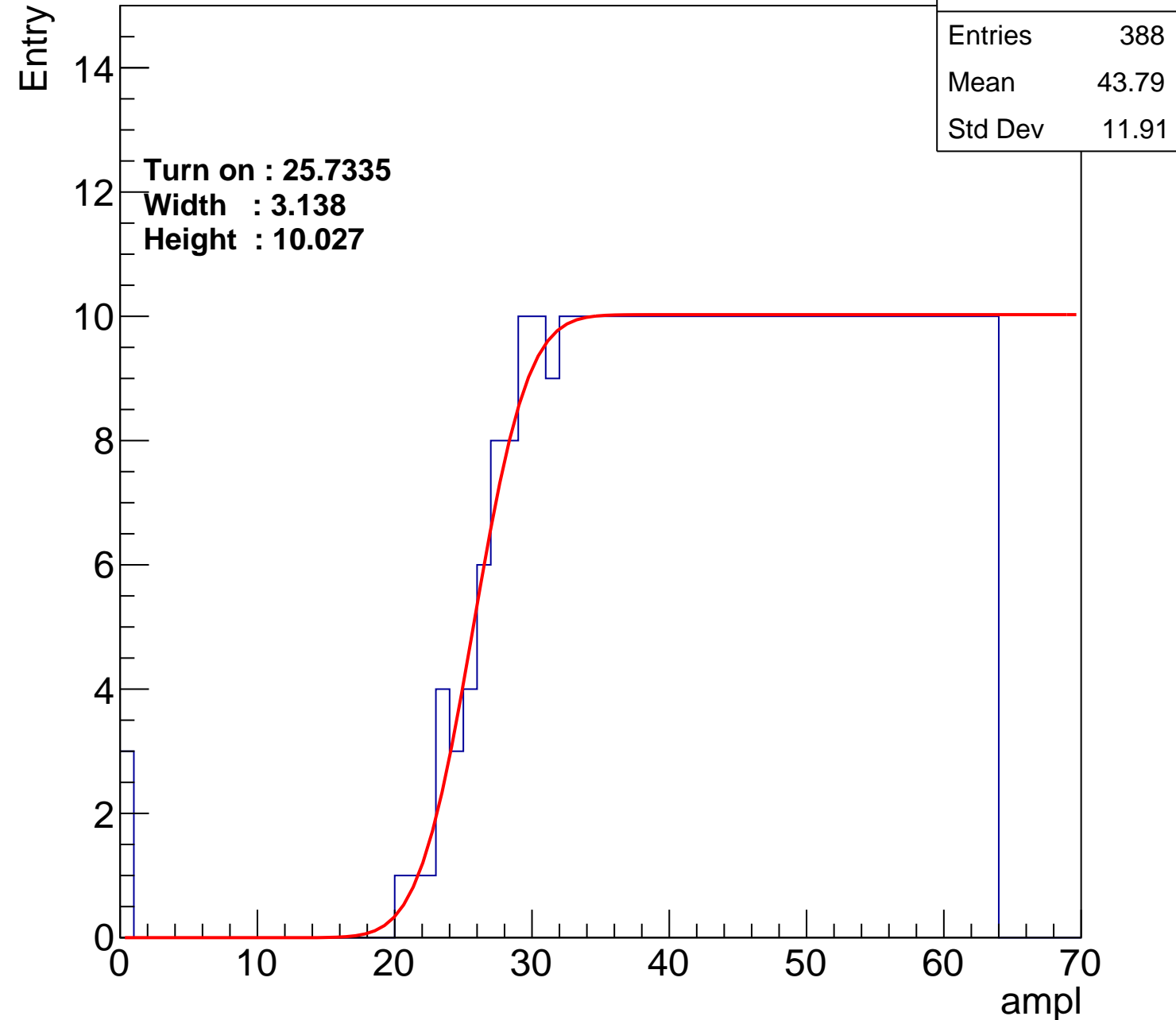
Width : 3.138

Height : 10.027

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



**calib\_packv5\_042523\_0143.root, FC#0, port D2**

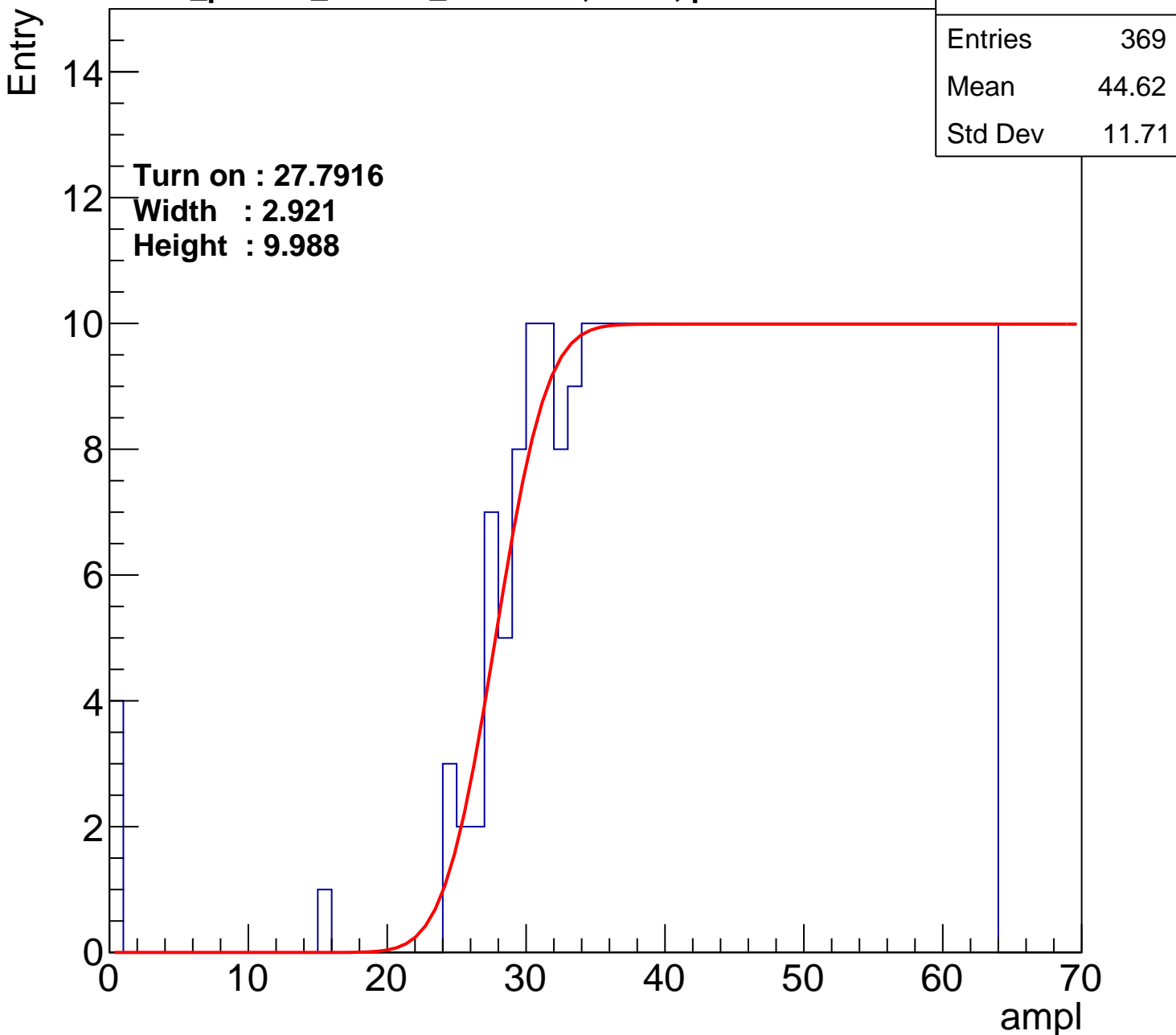
Entries	369
Mean	44.62
Std Dev	11.71

Mean	44.62
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Std Dev	11.71
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**Width : 2.921**

**Height : 9.988**



# B1L101S, U16-ch93

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	370
Mean	44.6
Std Dev	11.67

Turn on : 27.9855

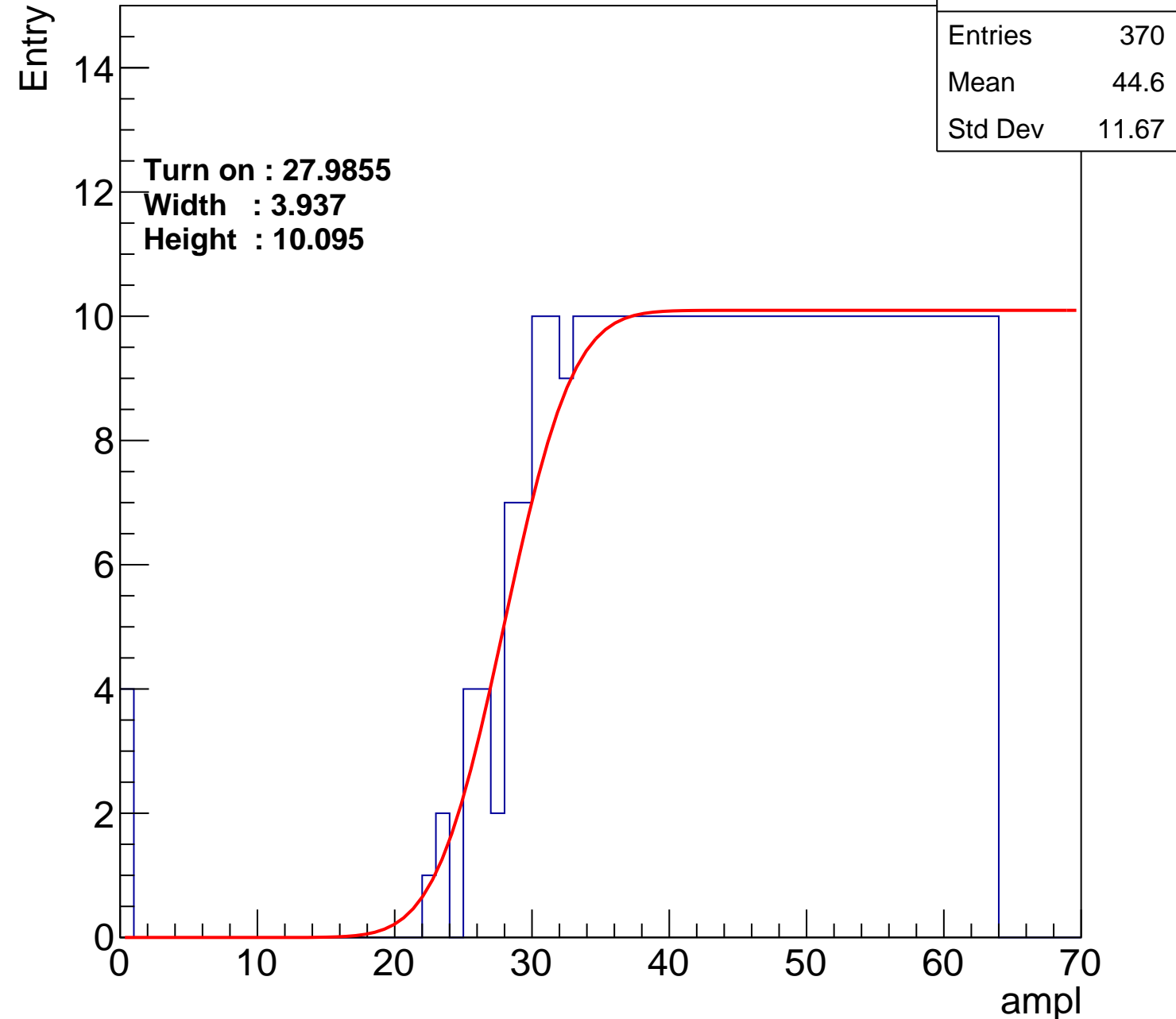
Width : 3.937

Height : 10.095

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U16-ch94

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	372
Mean	44.57
Std Dev	11.53

Turn on : 27.5348

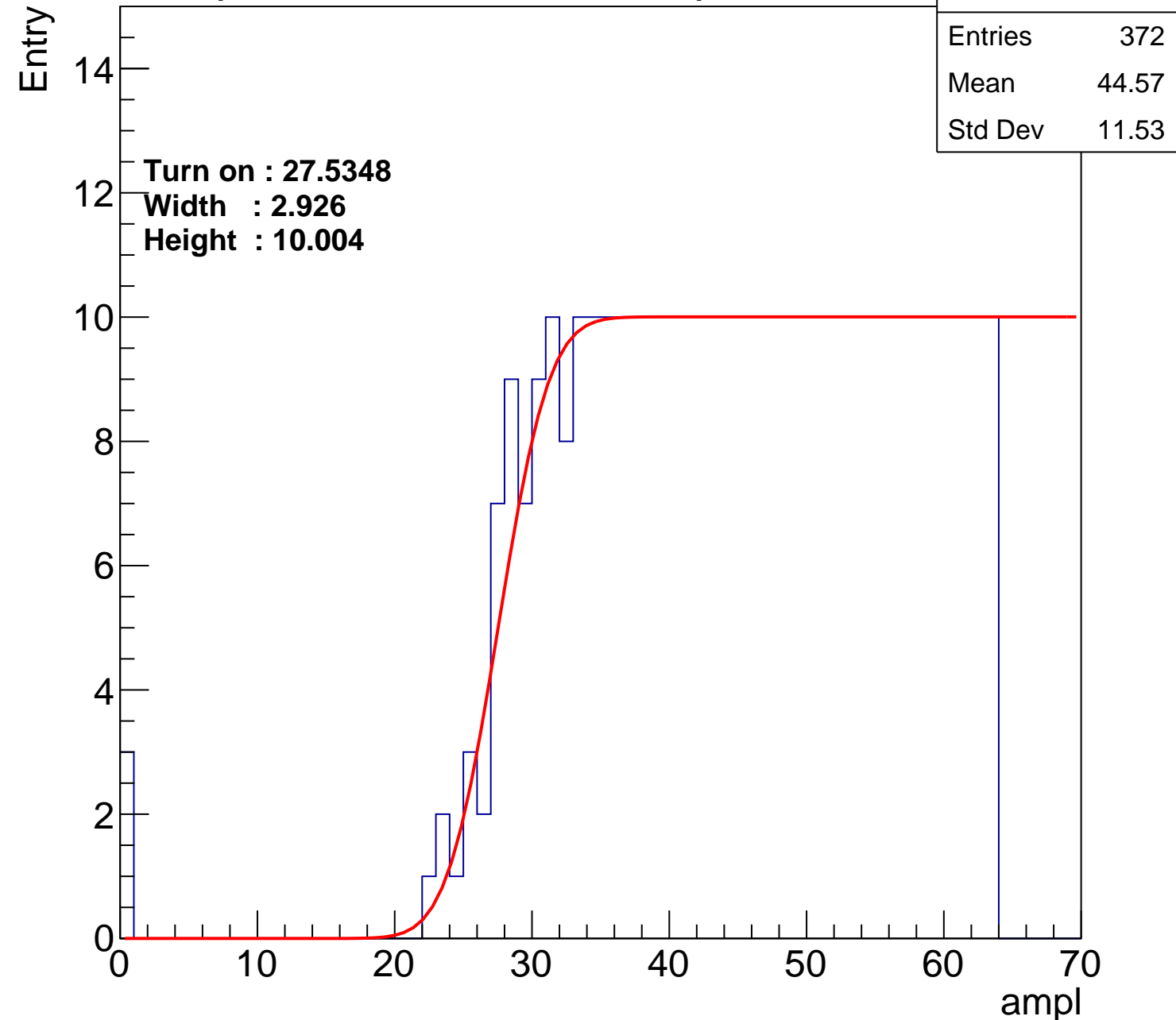
Width : 2.926

Height : 10.004

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L101S, U16-ch95

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	379
Mean	44.16
Std Dev	11.87

Turn on : 26.6810

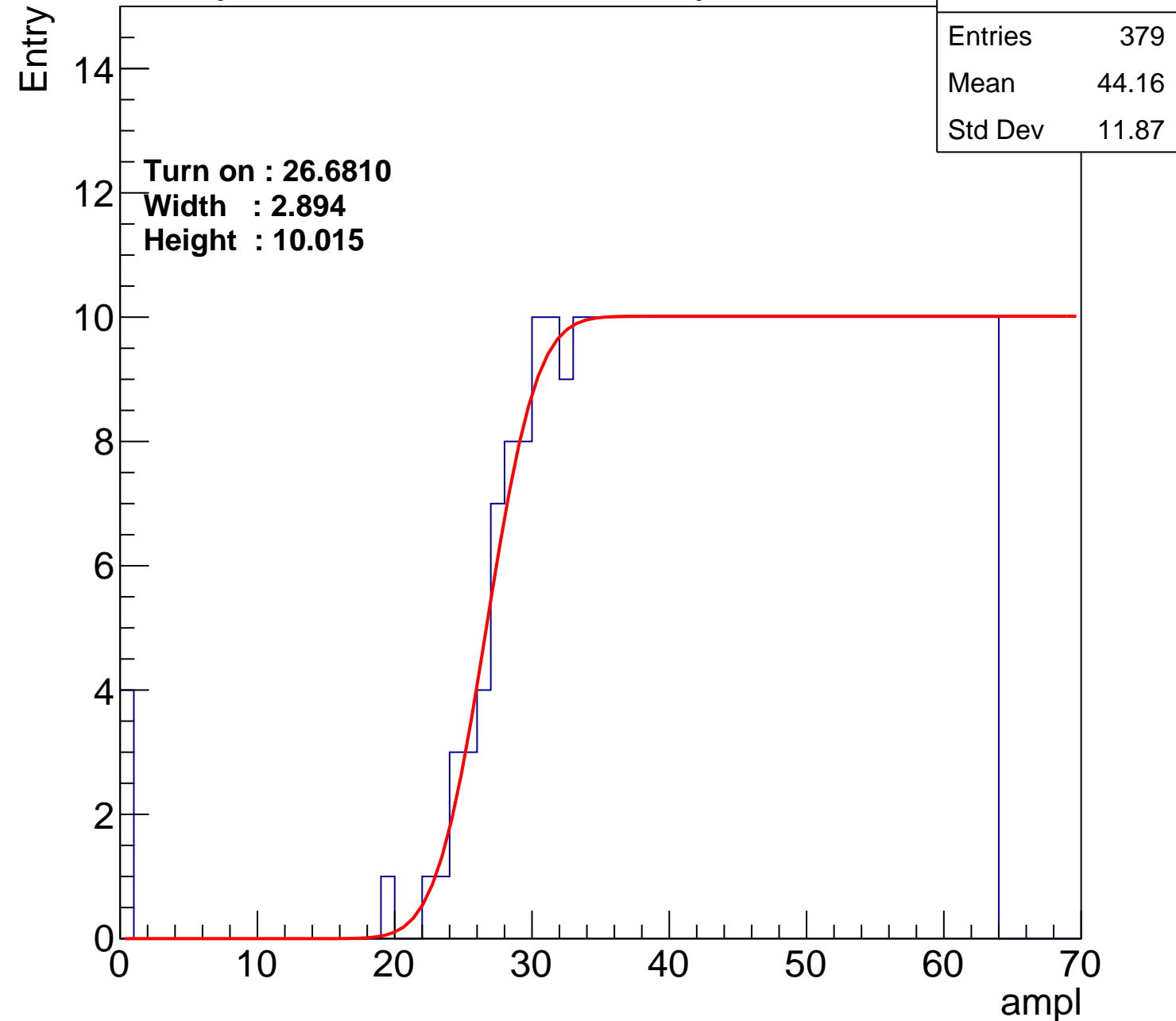
Width : 2.894

Height : 10.015

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U16-ch96

calib\_packv5\_042523\_0143.root, FC#0, port D2

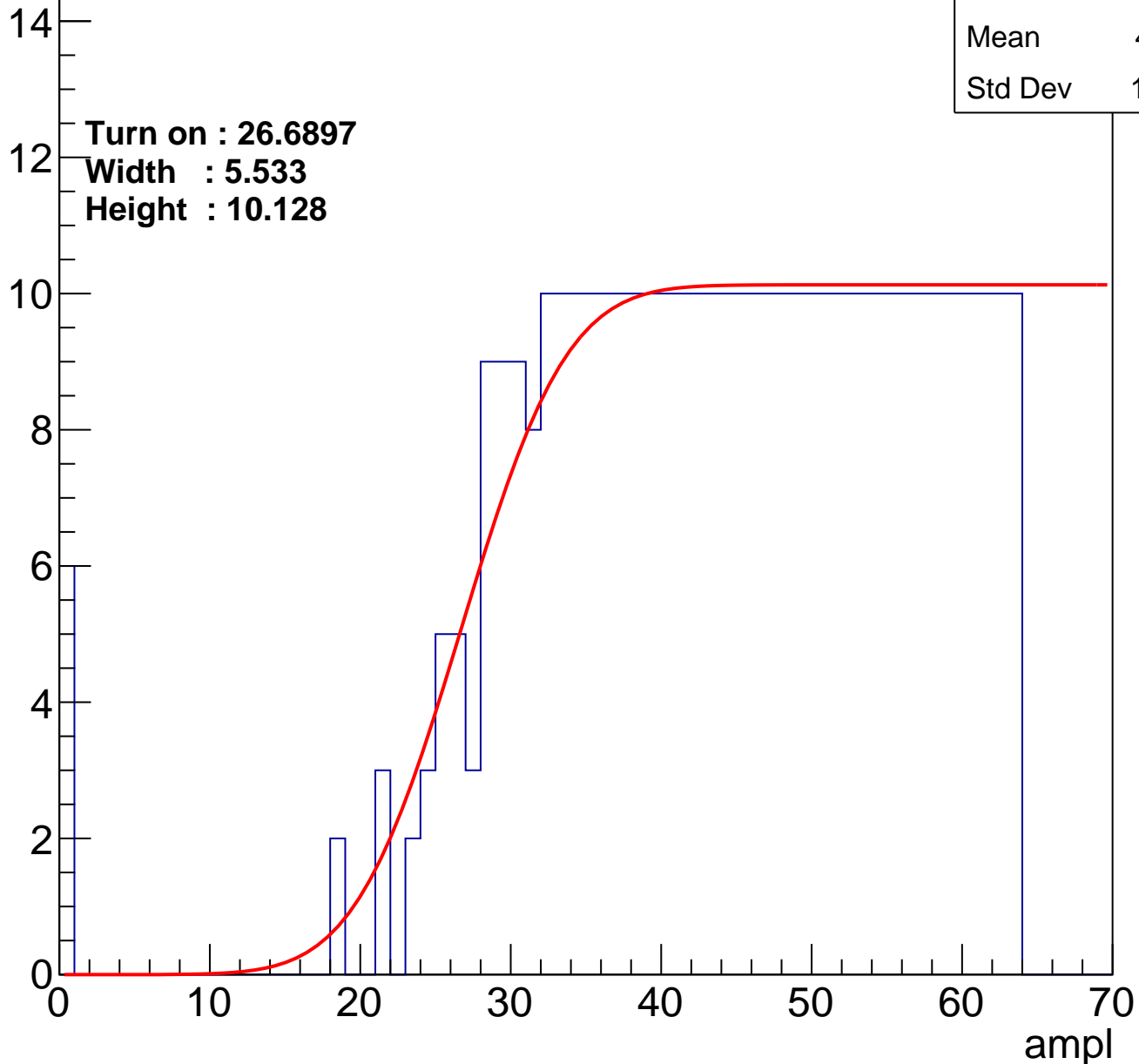
Entries	384
Mean	43.71
Std Dev	12.45

**Turn on : 26.6897**

**Width : 5.533**

**Height : 10.128**

Entry



# B1L101S, U16-ch97

calib\_packv5\_042523\_0143.root, FC#0, port D2

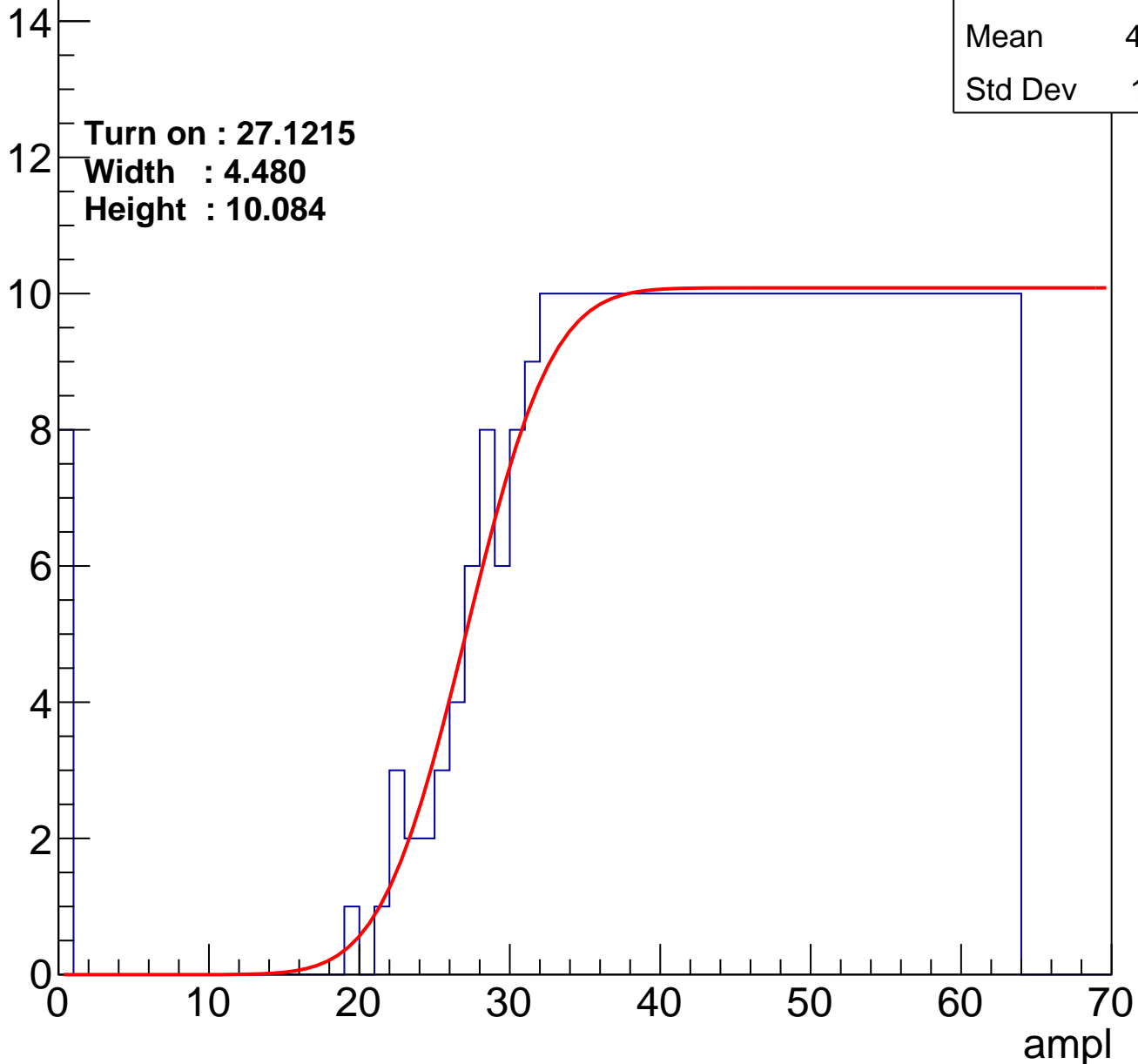
Entries	381
Mean	43.72
Std Dev	12.71

Turn on : 27.1215

Width : 4.480

Height : 10.084

Entry



# B1L101S, U16-ch98

calib\_packv5\_042523\_0143.root, FC#0, port D2

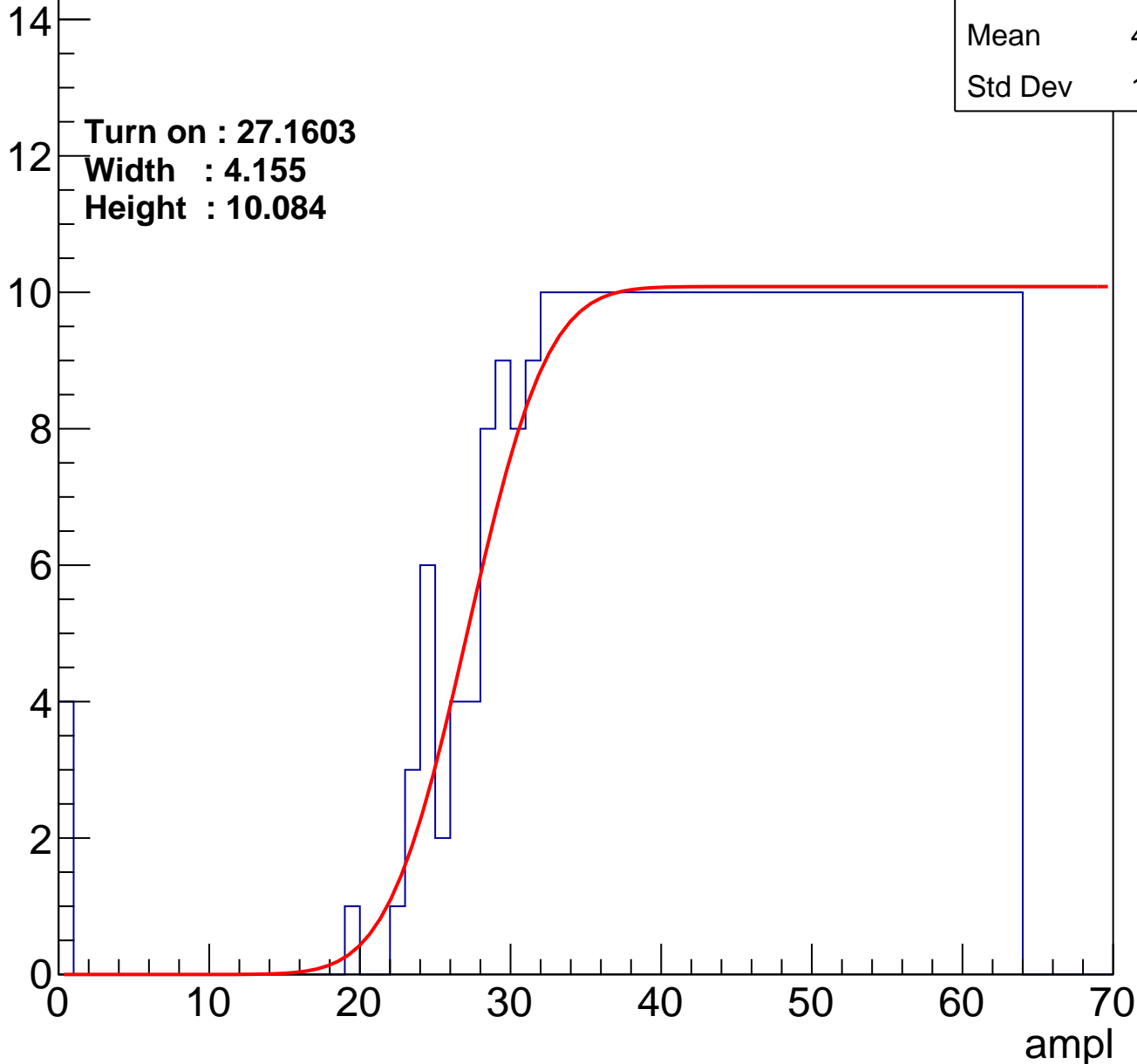
Entries	379
Mean	44.12
Std Dev	11.95

Turn on : 27.1603

Width : 4.155

Height : 10.084

Entry



# B1L101S, U16-ch99

calib\_packv5\_042523\_0143.root, FC#0, port D2

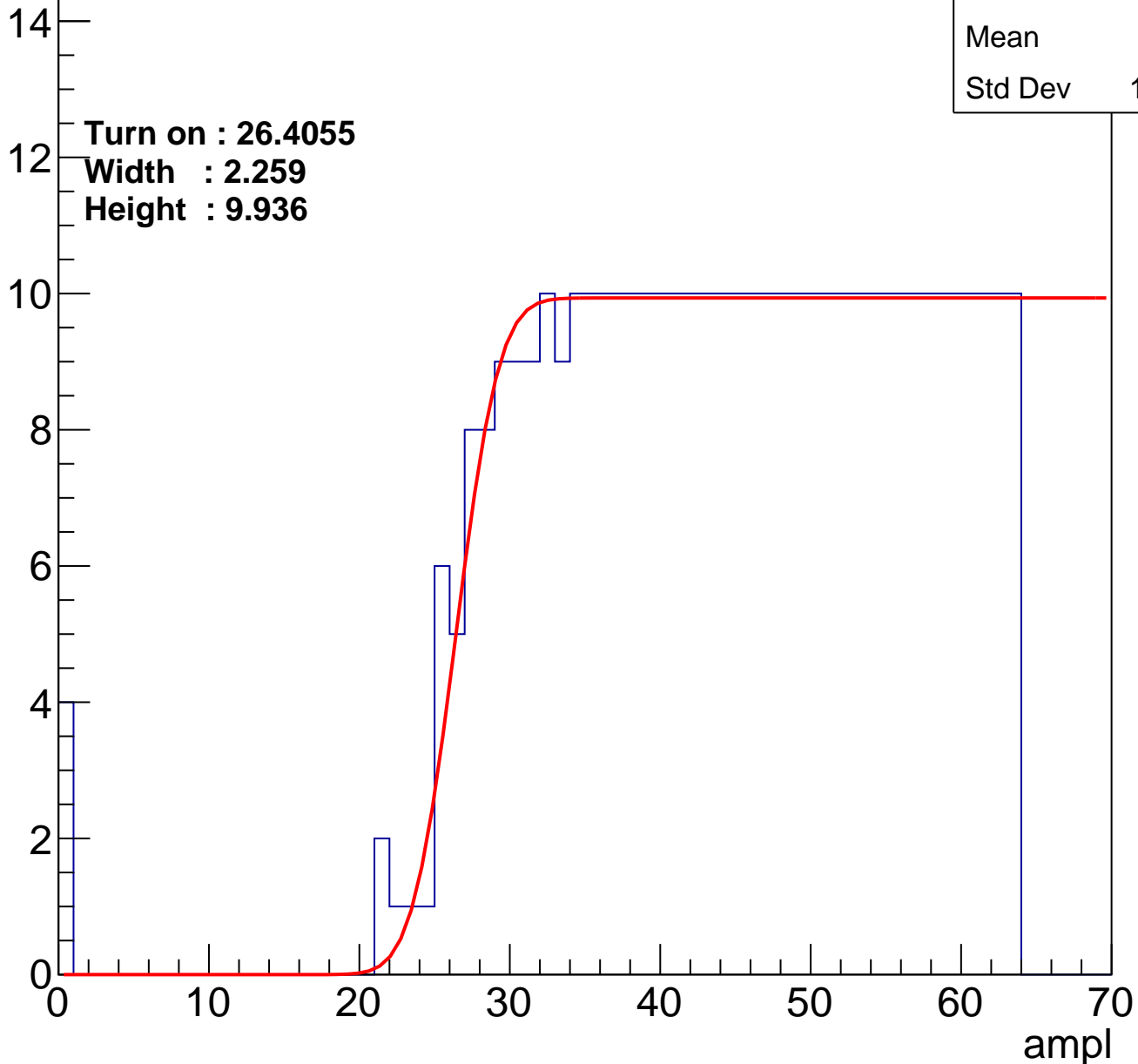
Entries	382
Mean	44
Std Dev	11.96

Turn on : 26.4055

Width : 2.259

Height : 9.936

Entry



# B1L101S, U16-ch100

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	375
Mean	44.23
Std Dev	12.13

Turn on : 27.1337

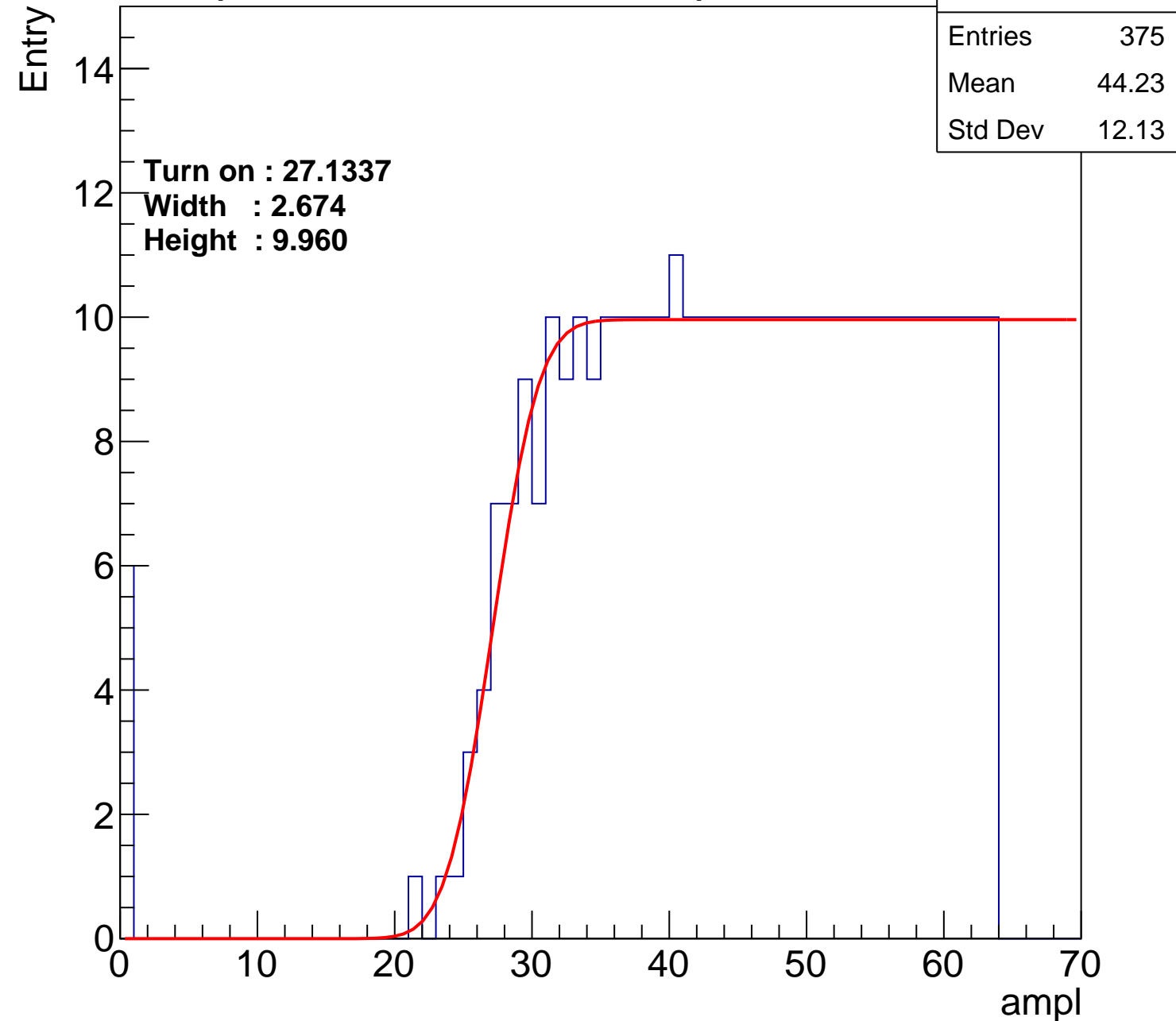
Width : 2.674

Height : 9.960

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U16-ch101

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	394
Mean	43.38
Std Dev	12.31

Turn on : 25.9082

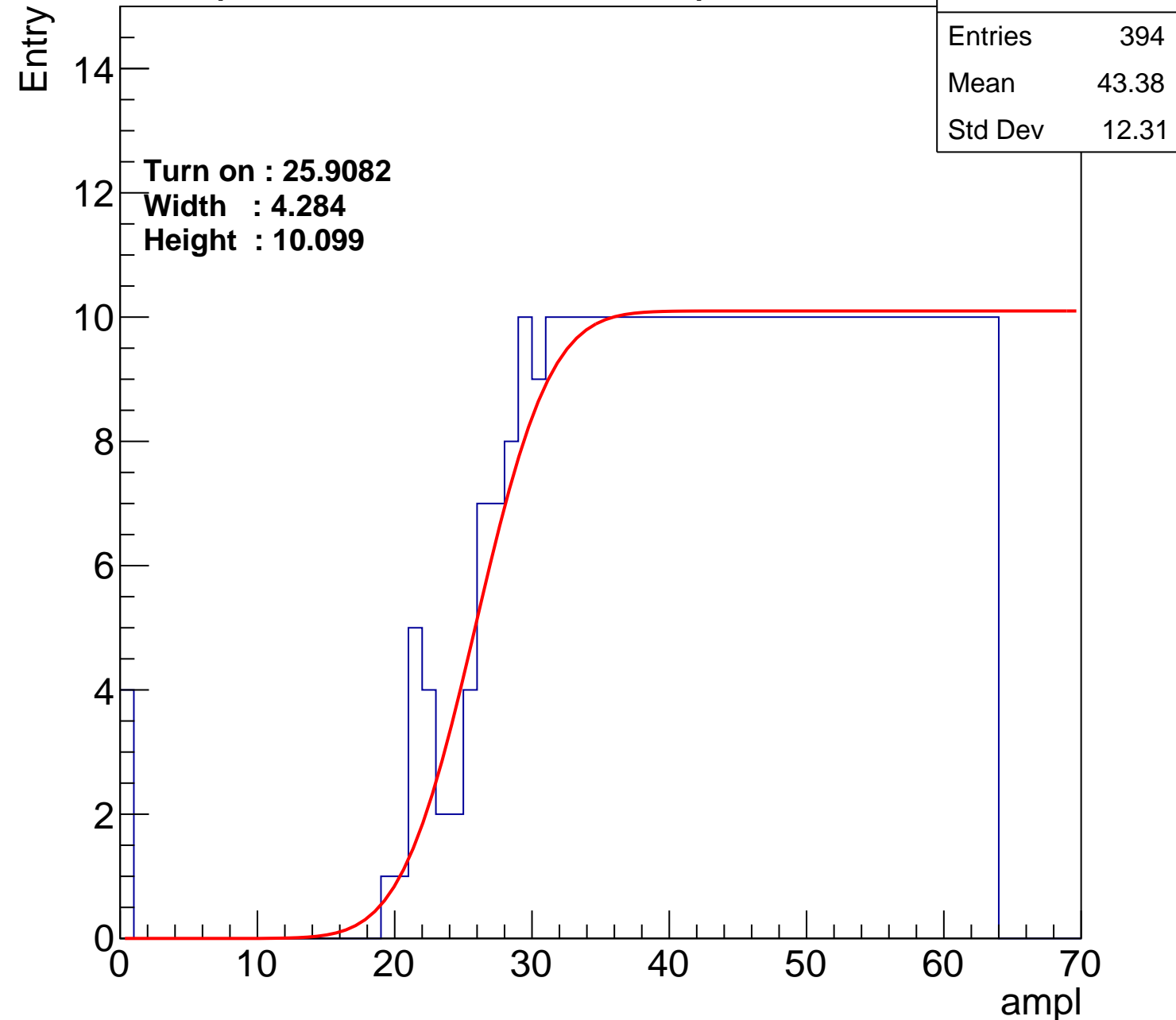
Width : 4.284

Height : 10.099

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U16-ch102

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	377
Mean	44.29
Std Dev	11.72

Turn on : 27.0020

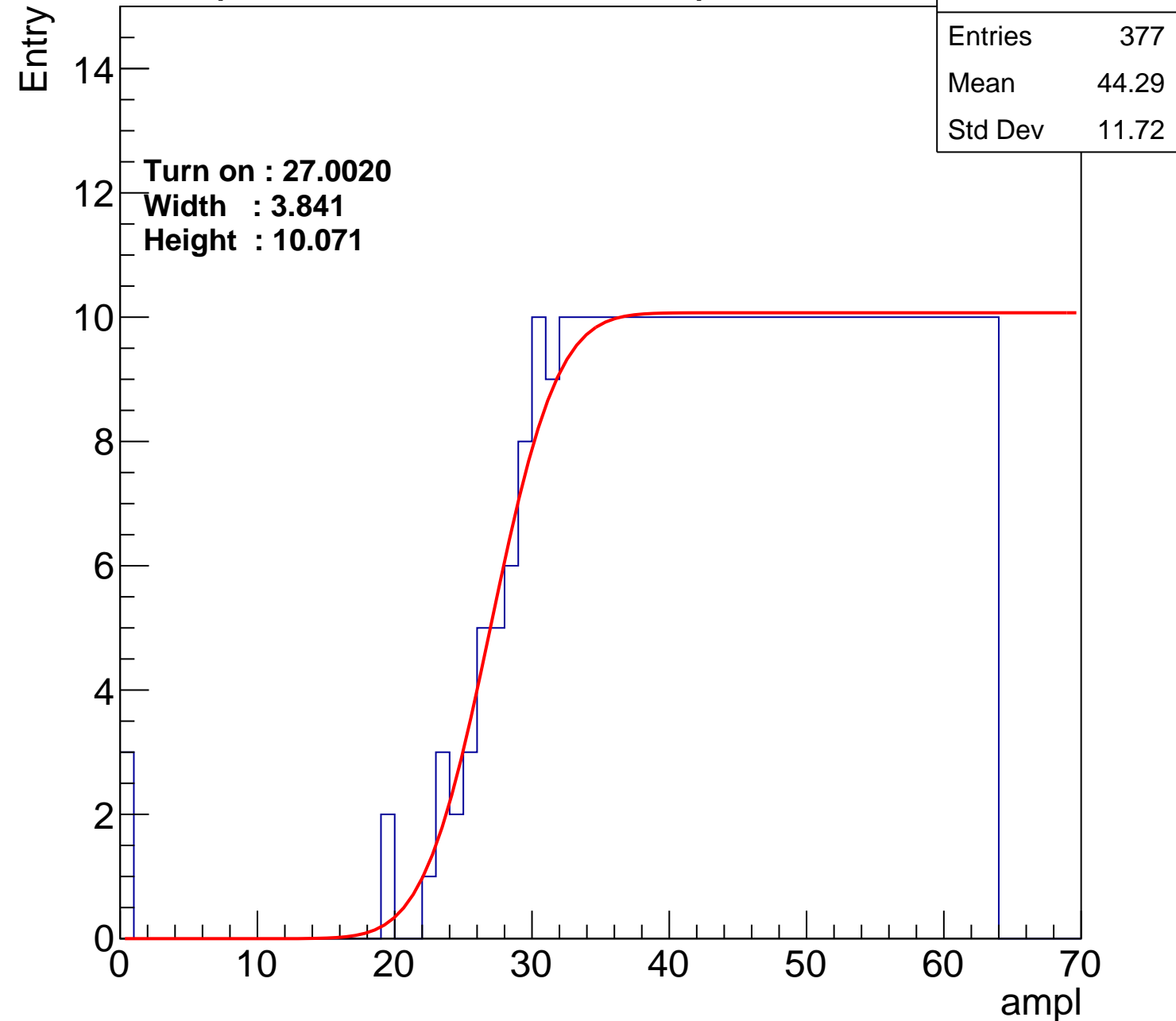
Width : 3.841

Height : 10.071

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L101S, U16-ch103

calib\_packv5\_042523\_0143.root, FC#0, port D2

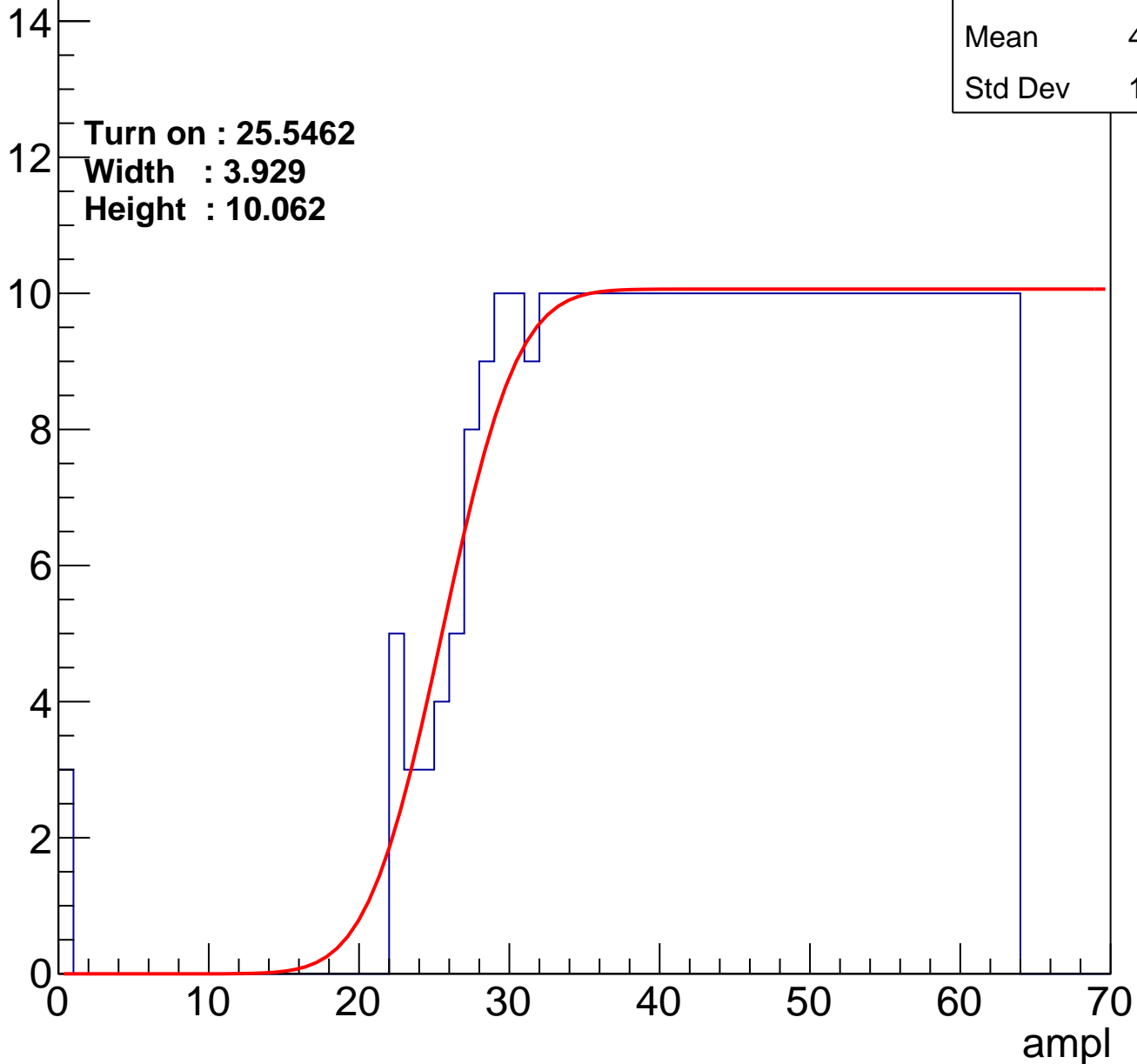
Entries	389
Mean	43.75
Std Dev	11.93

Turn on : 25.5462

Width : 3.929

Height : 10.062

Entry



# B1L101S, U16-ch104

calib\_packv5\_042523\_0143.root, FC#0, port D2

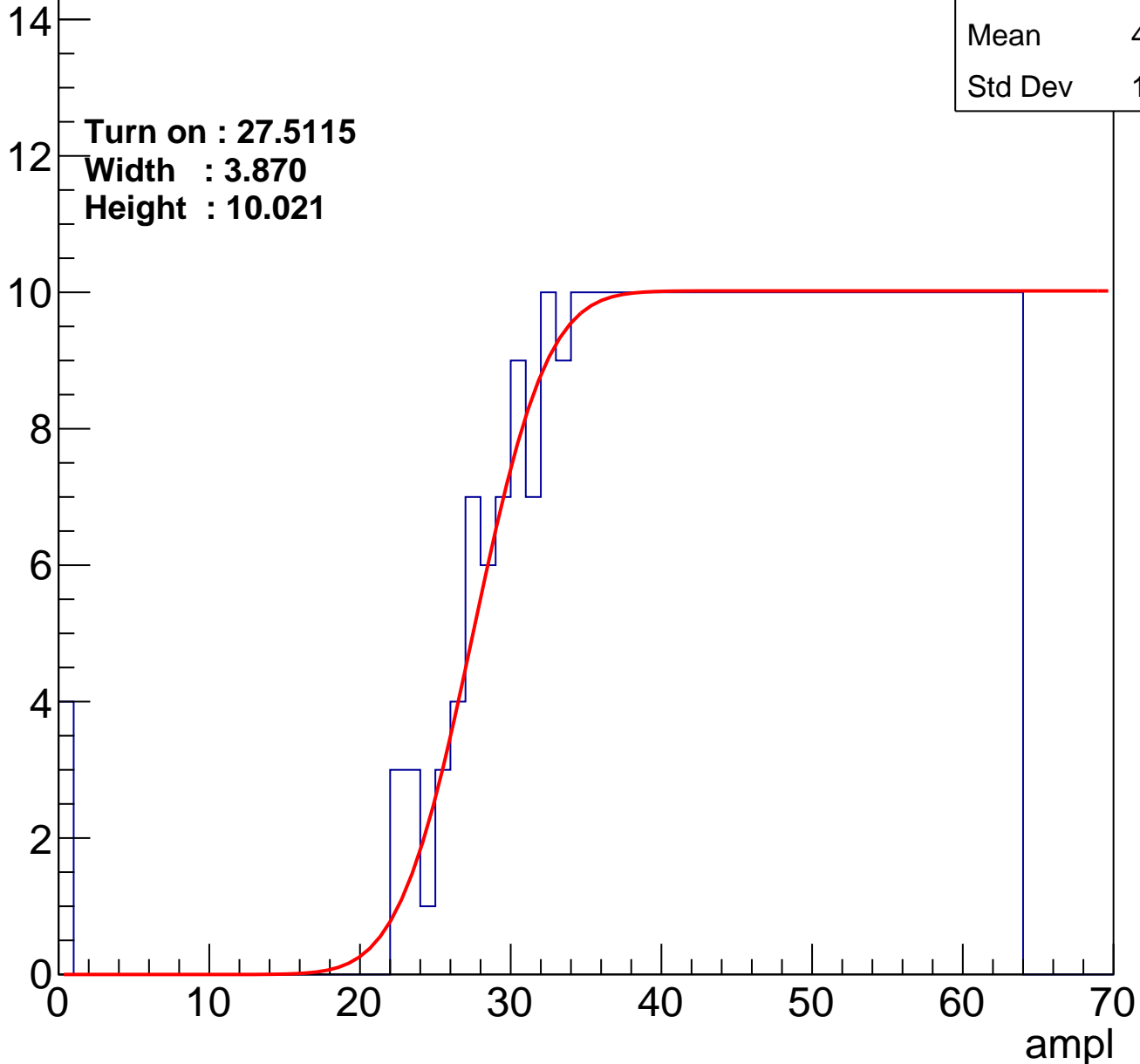
Entries	373
Mean	44.38
Std Dev	11.85

Turn on : 27.5115

Width : 3.870

Height : 10.021

Entry



# B1L101S, U16-ch105

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	380
Mean	44.11
Std Dev	11.9

**Turn on : 26.6194**

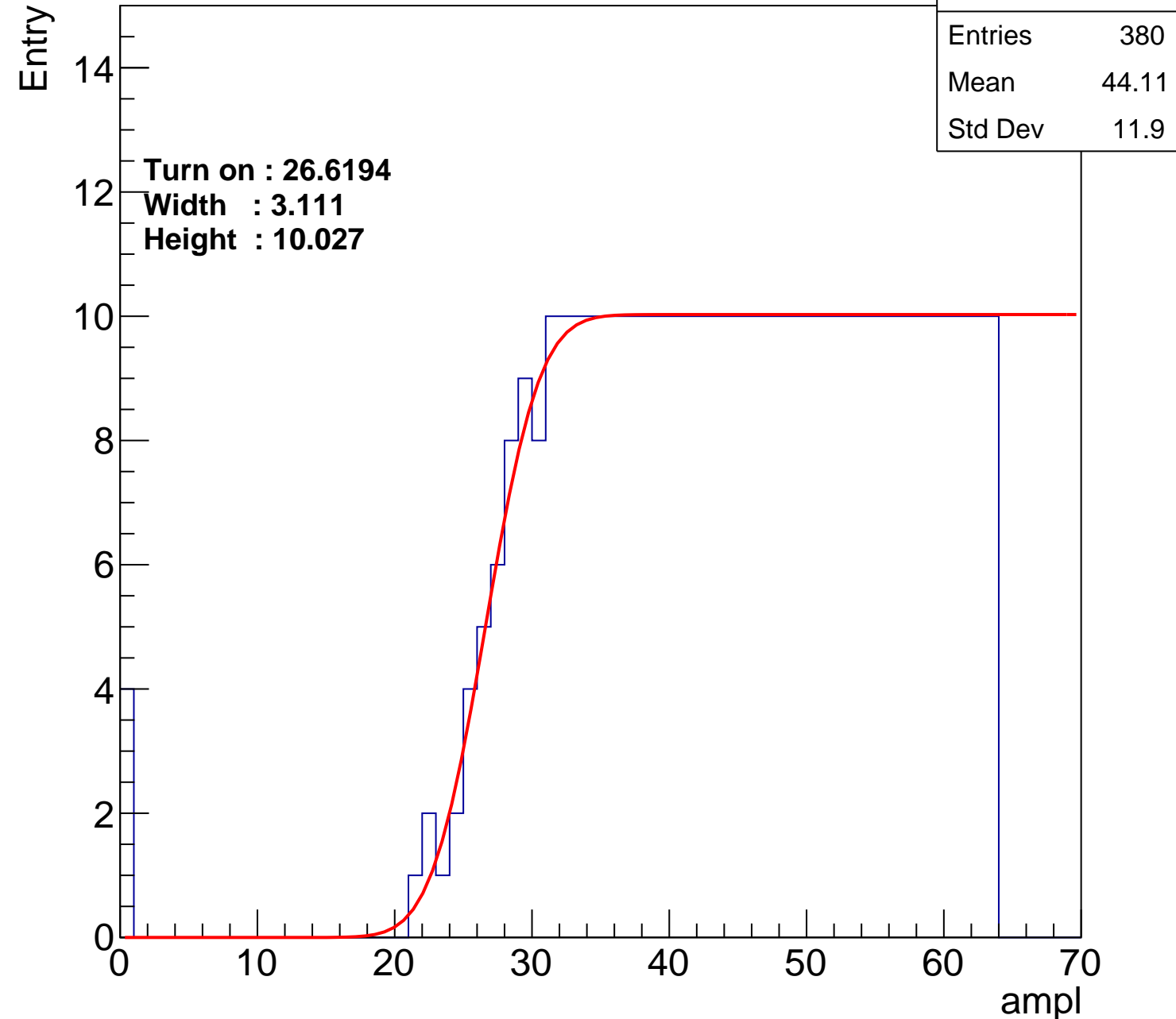
**Width : 3.111**

**Height : 10.027**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U16-ch106

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	383
Mean	43.92
Std Dev	12.04

**Turn on : 26.3188**

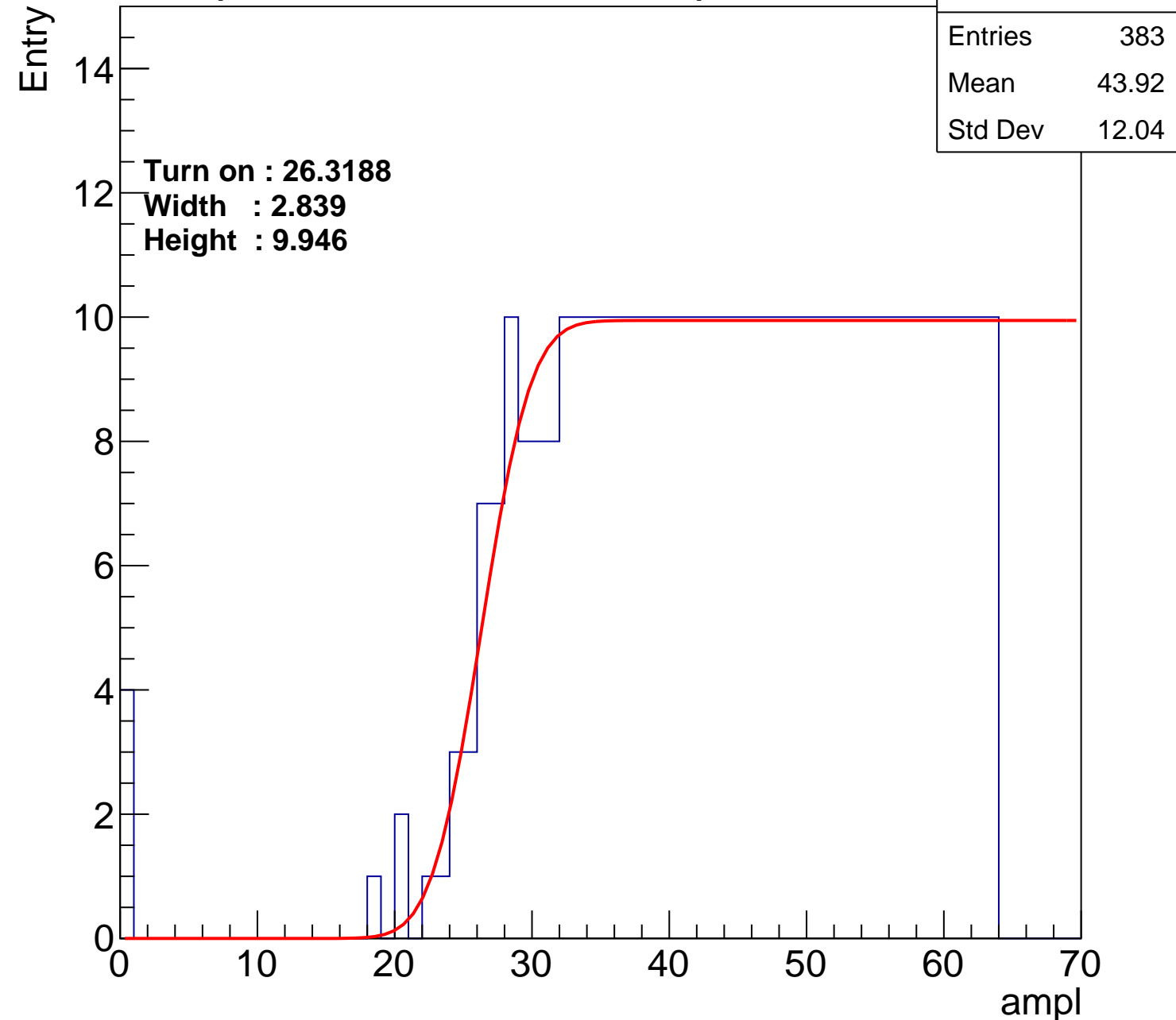
**Width : 2.839**

**Height : 9.946**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U16-ch107

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	380
Mean	44.13
Std Dev	11.81

Turn on : 27.5306

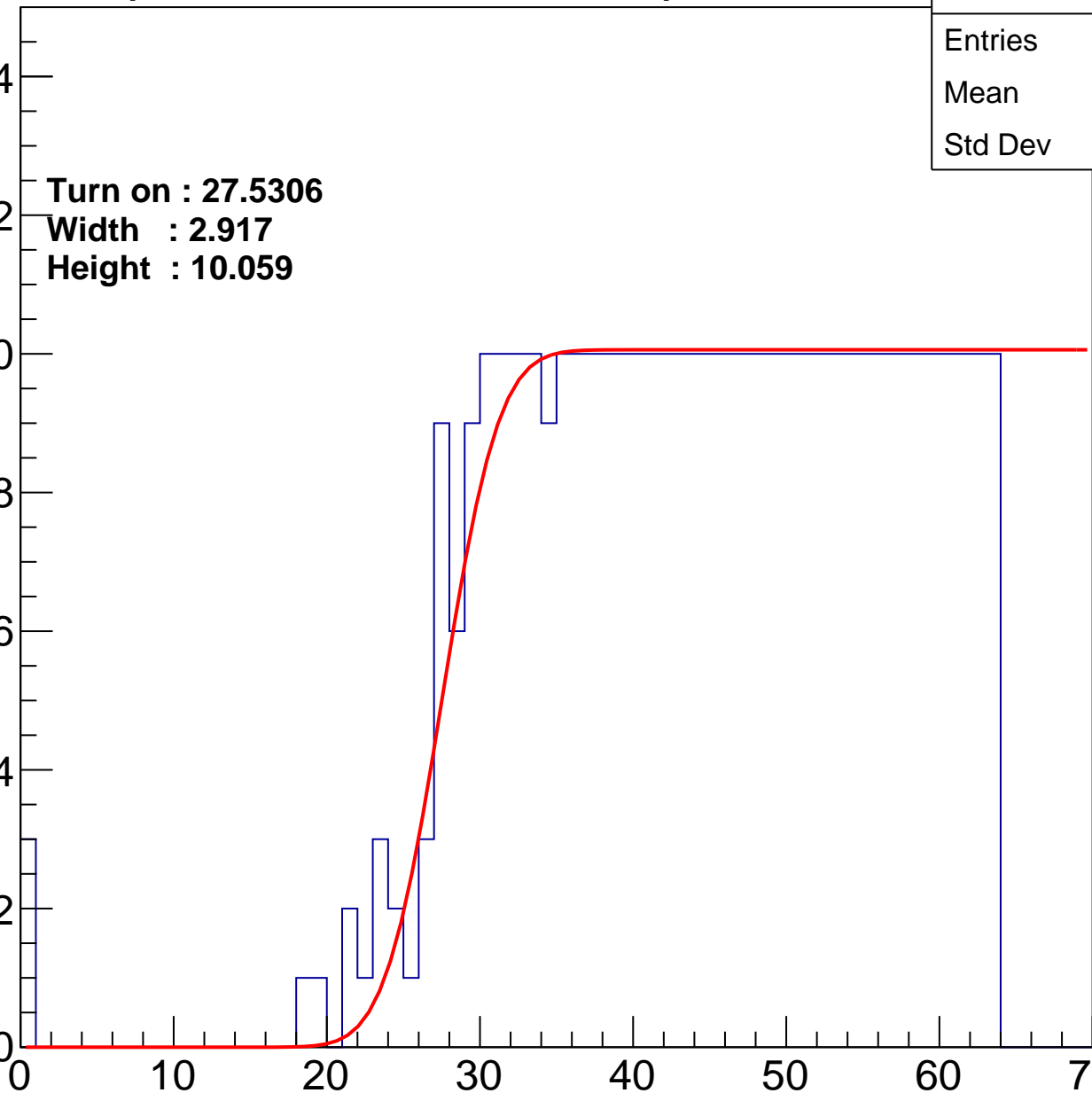
Width : 2.917

Height : 10.059

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U16-ch108

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	372
Mean	44.29
Std Dev	12.26

Turn on : 27.7389

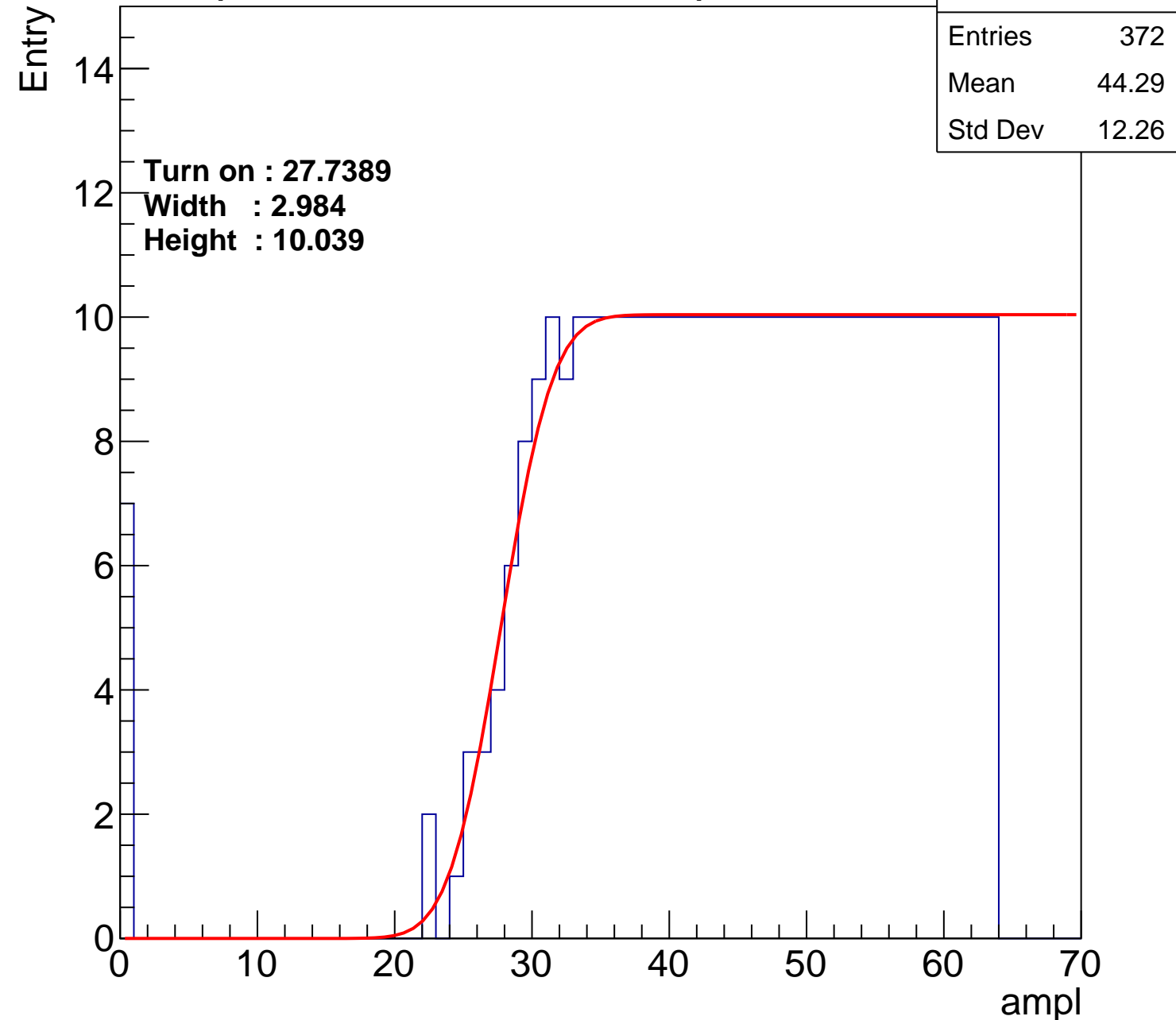
Width : 2.984

Height : 10.039

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U16-ch109

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	348
Mean	45.89
Std Dev	10.5

Turn on : 29.1335

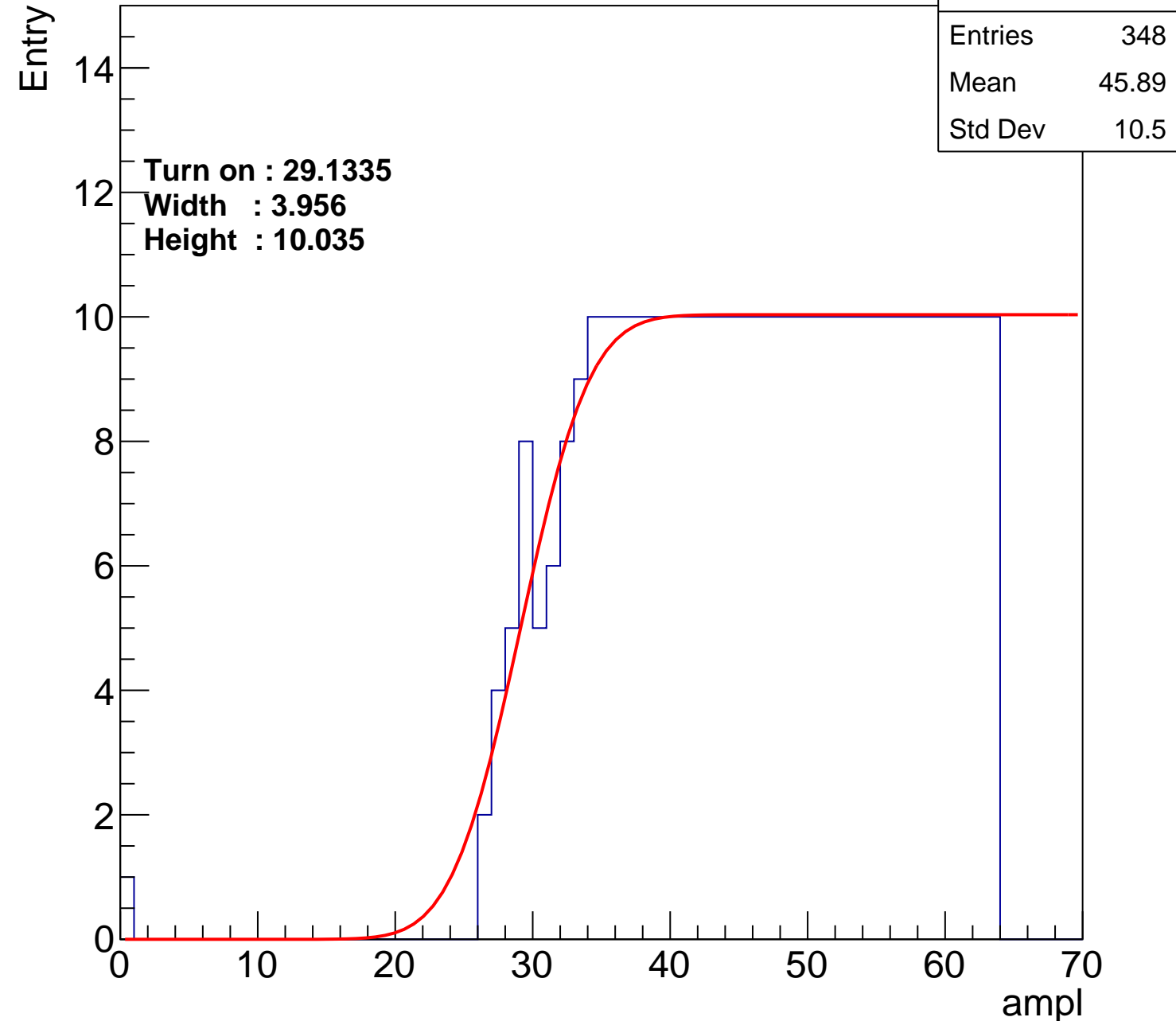
Width : 3.956

Height : 10.035

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U16-ch110

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	372
Mean	44.55
Std Dev	11.48

Turn on : 27.3348

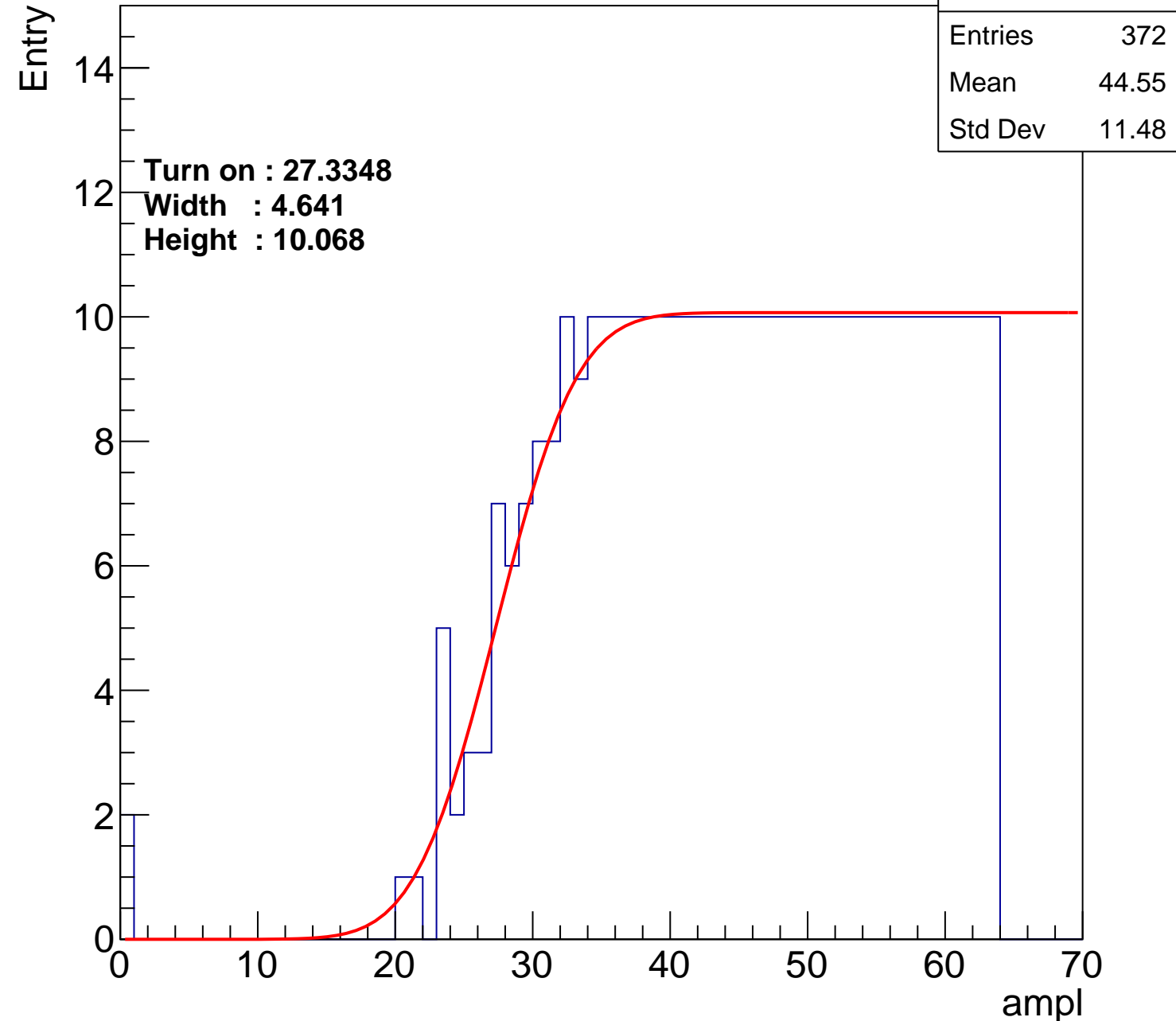
Width : 4.641

Height : 10.068

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L101S, U16-ch111

**calib\_packv5\_042523\_0143.root, FC#0, port D2**

Entries	371
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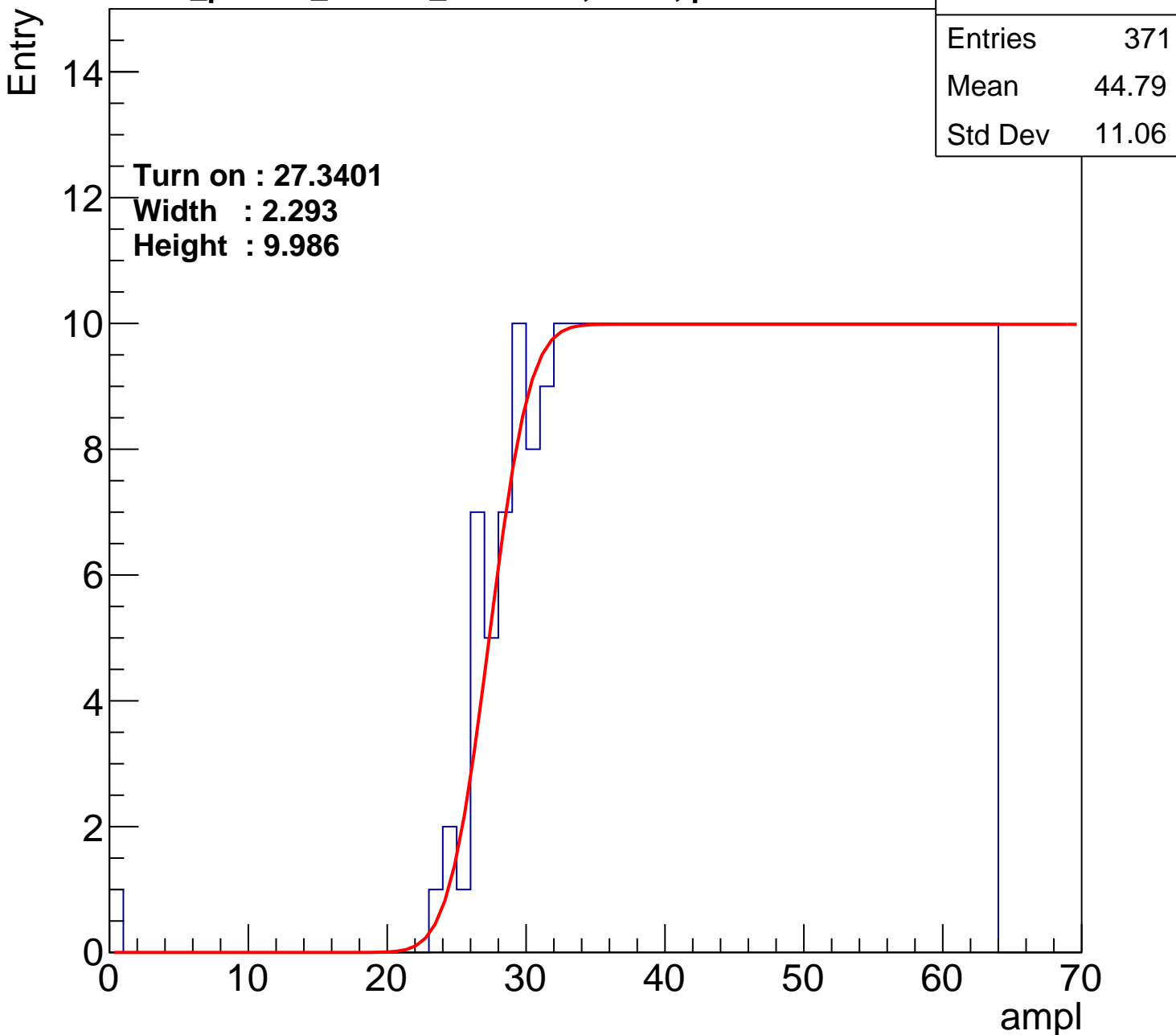
Mean	44.79
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Std Dev	11.06
---------	-------

**Turn on : 27.3401**

**Width : 2.293**

**Height : 9.986**



# B1L101S, U16-ch112

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	366
Mean	44.88
Std Dev	11.28

Turn on : 28.4085

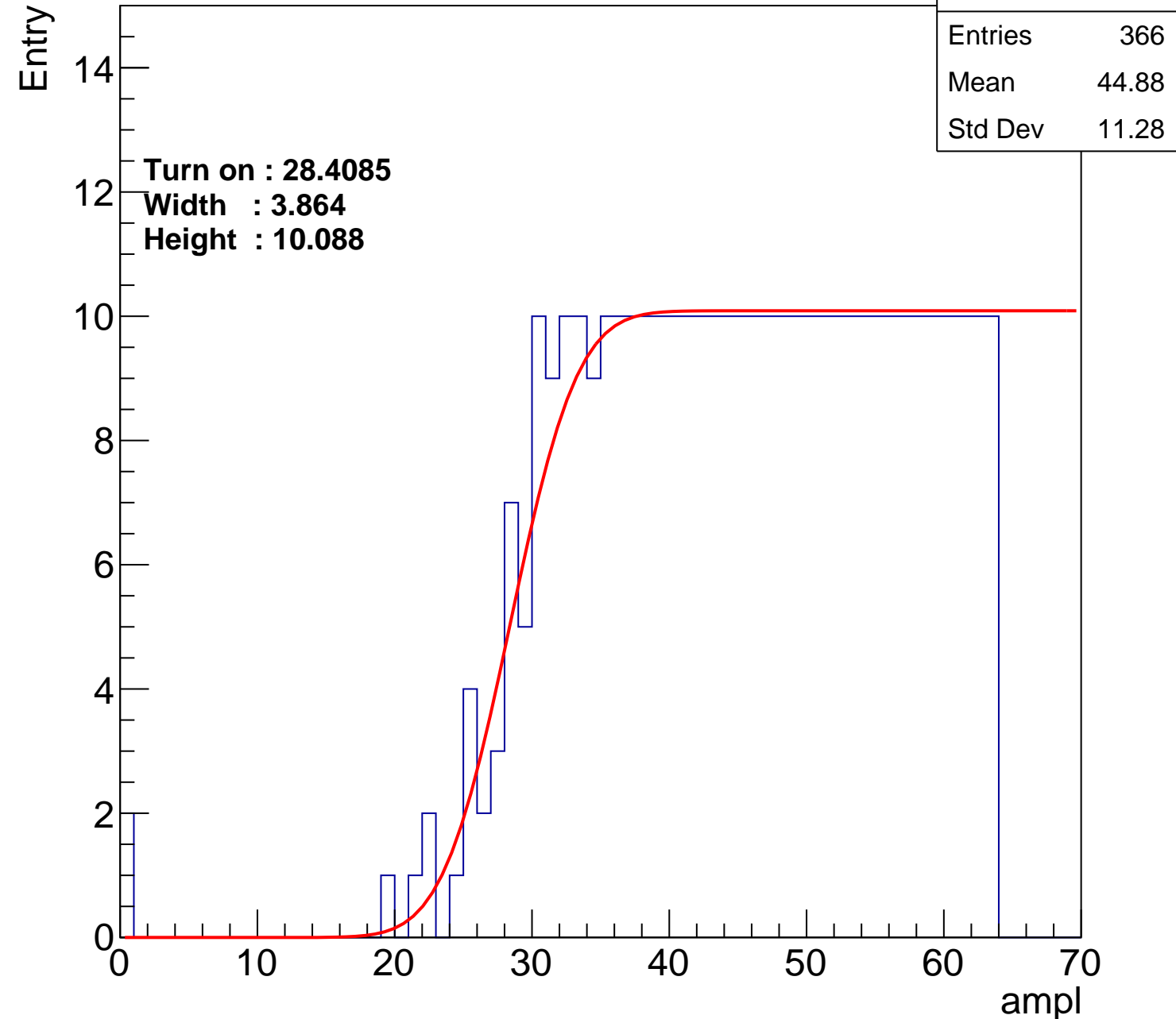
Width : 3.864

Height : 10.088

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U16-ch113

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	364
Mean	45.13
Std Dev	10.89

Turn on : 28.1433

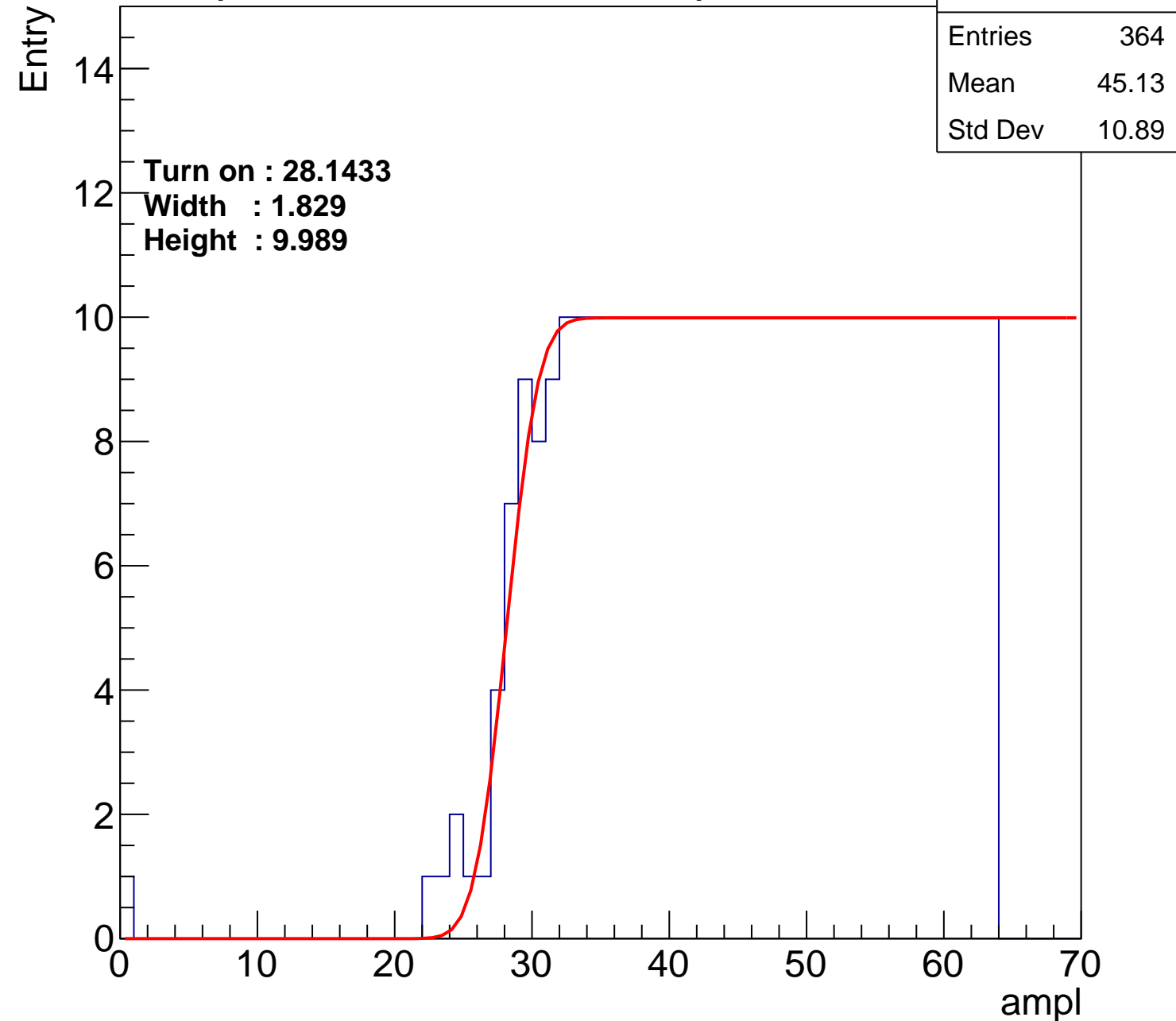
Width : 1.829

Height : 9.989

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U16-ch114

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	385
Mean	43.76
Std Dev	12.25

Turn on : 26.3464

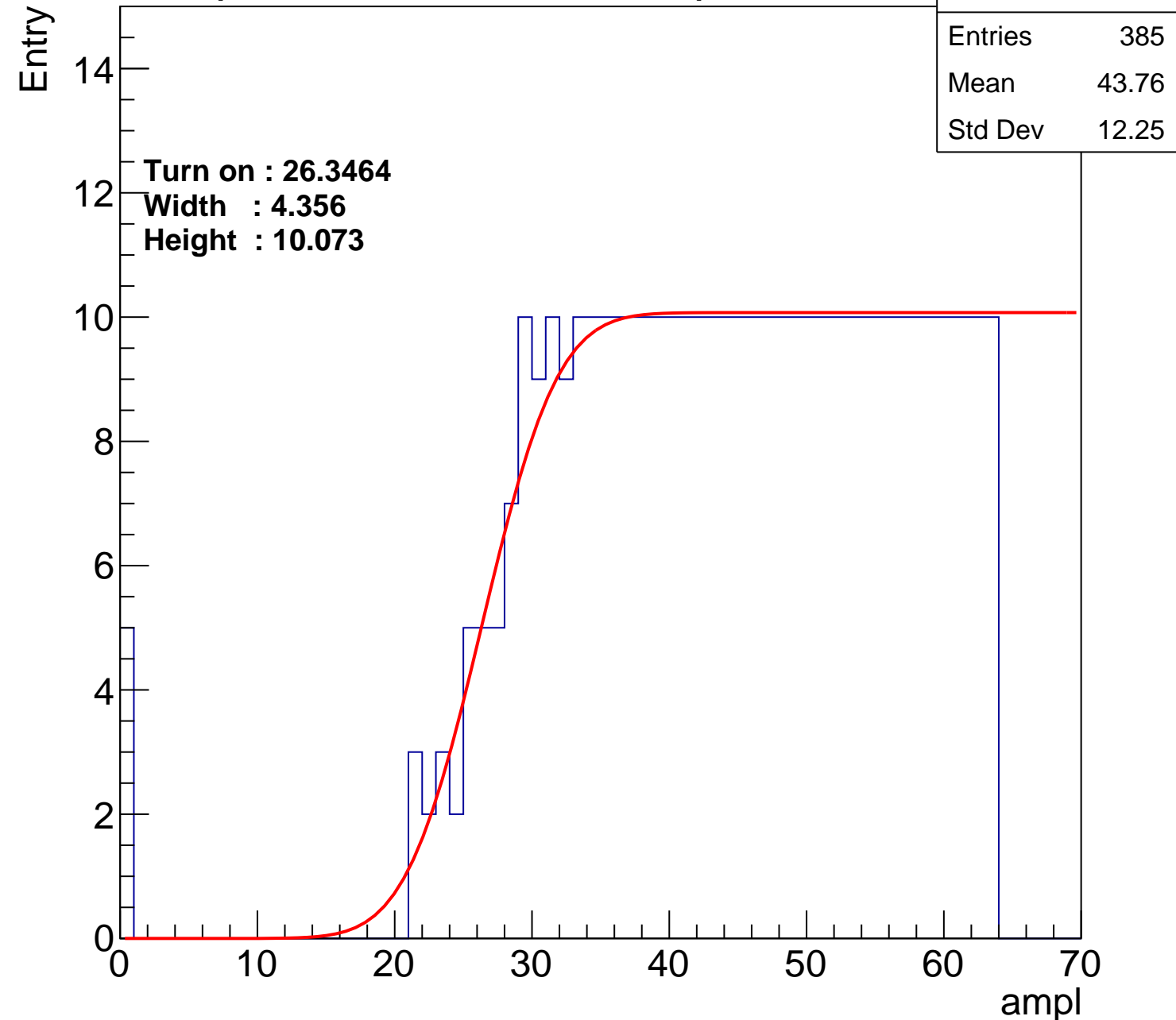
Width : 4.356

Height : 10.073

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U16-ch115

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	362
Mean	44.98
Std Dev	11.5

Turn on : 28.5383

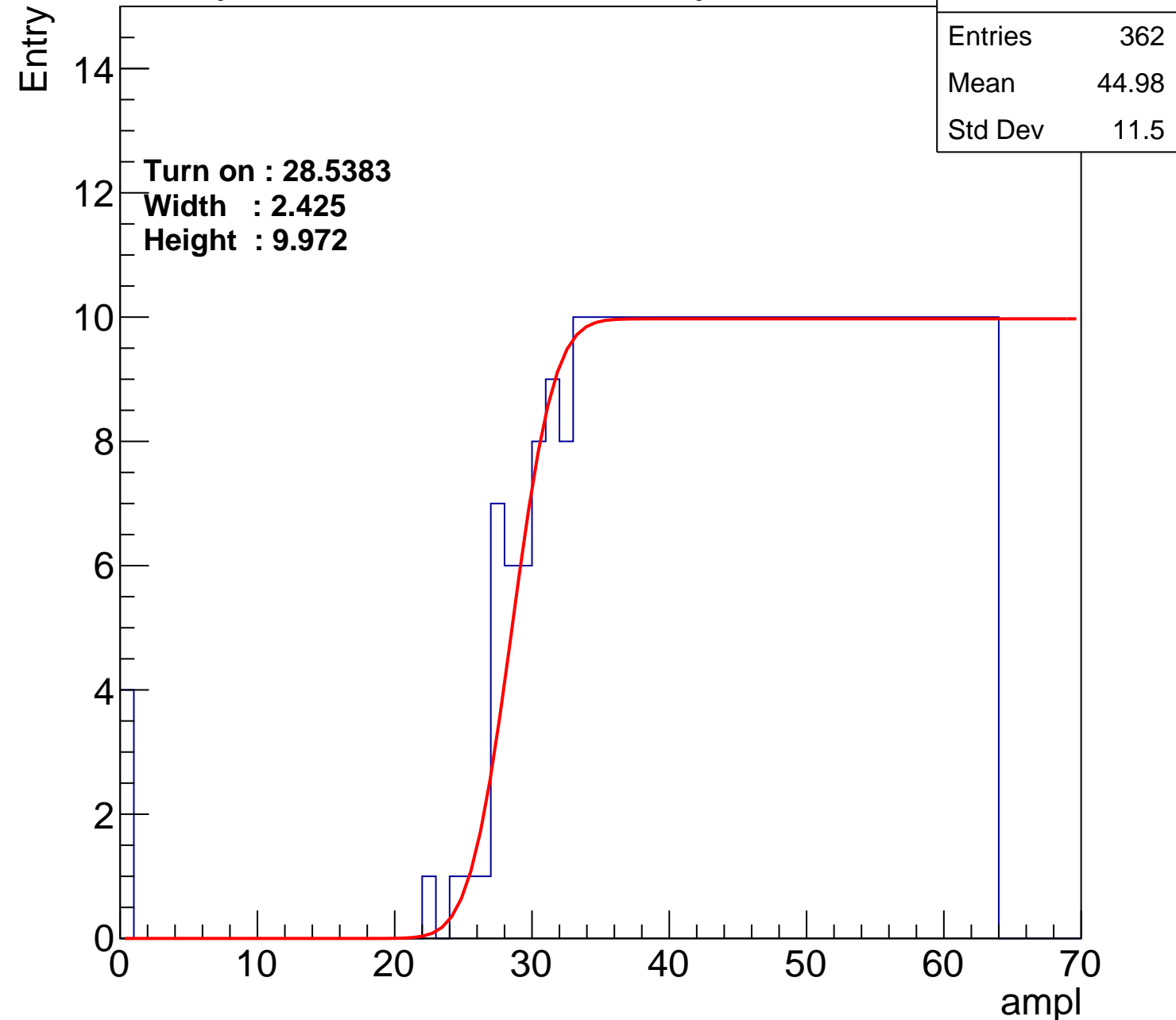
Width : 2.425

Height : 9.972

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U16-ch116

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	382
Mean	43.85
Std Dev	12.33

Turn on : 26.9287

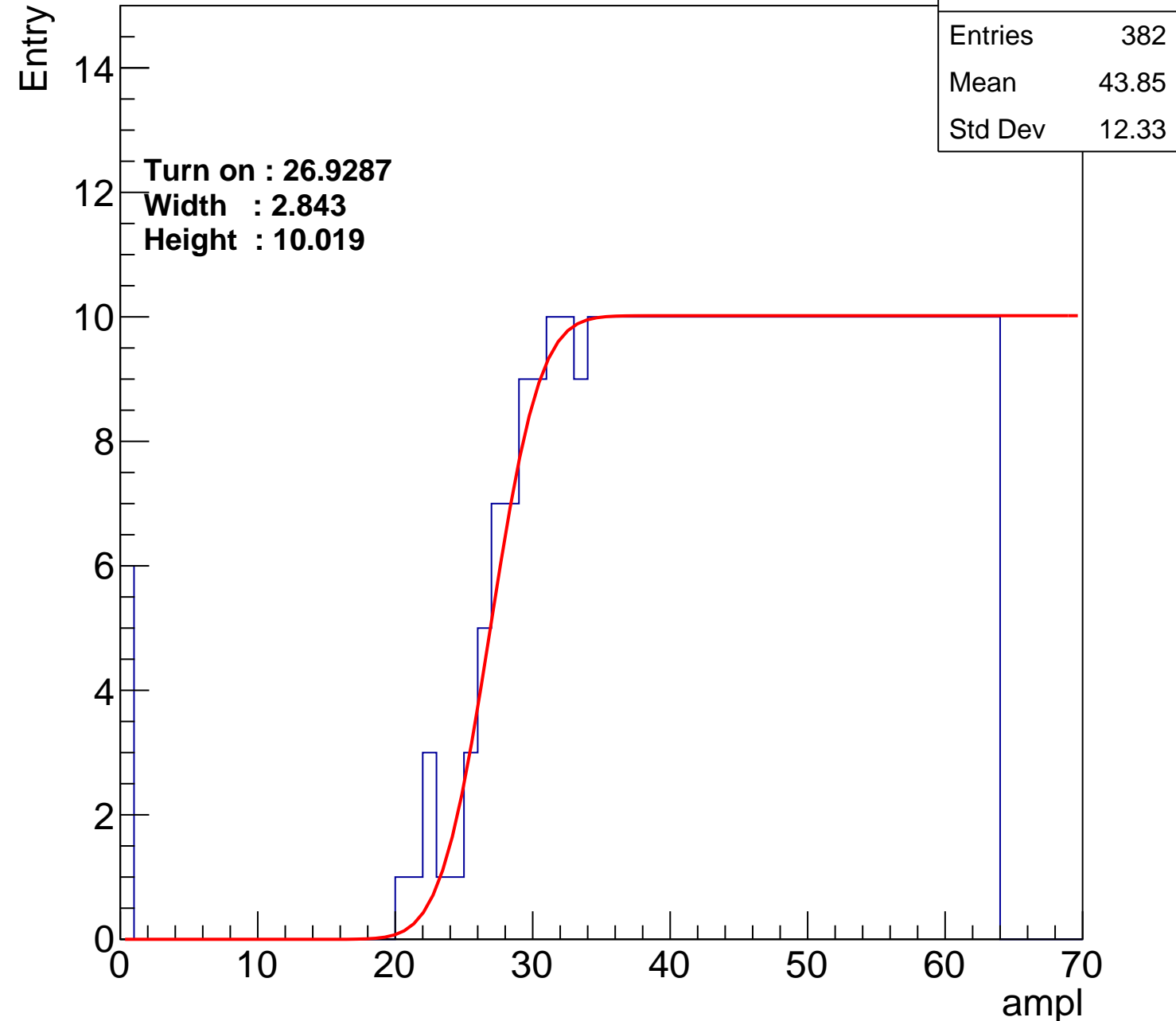
Width : 2.843

Height : 10.019

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U16-ch117

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	372
Mean	44.26
Std Dev	12.31

Turn on : 27.6203

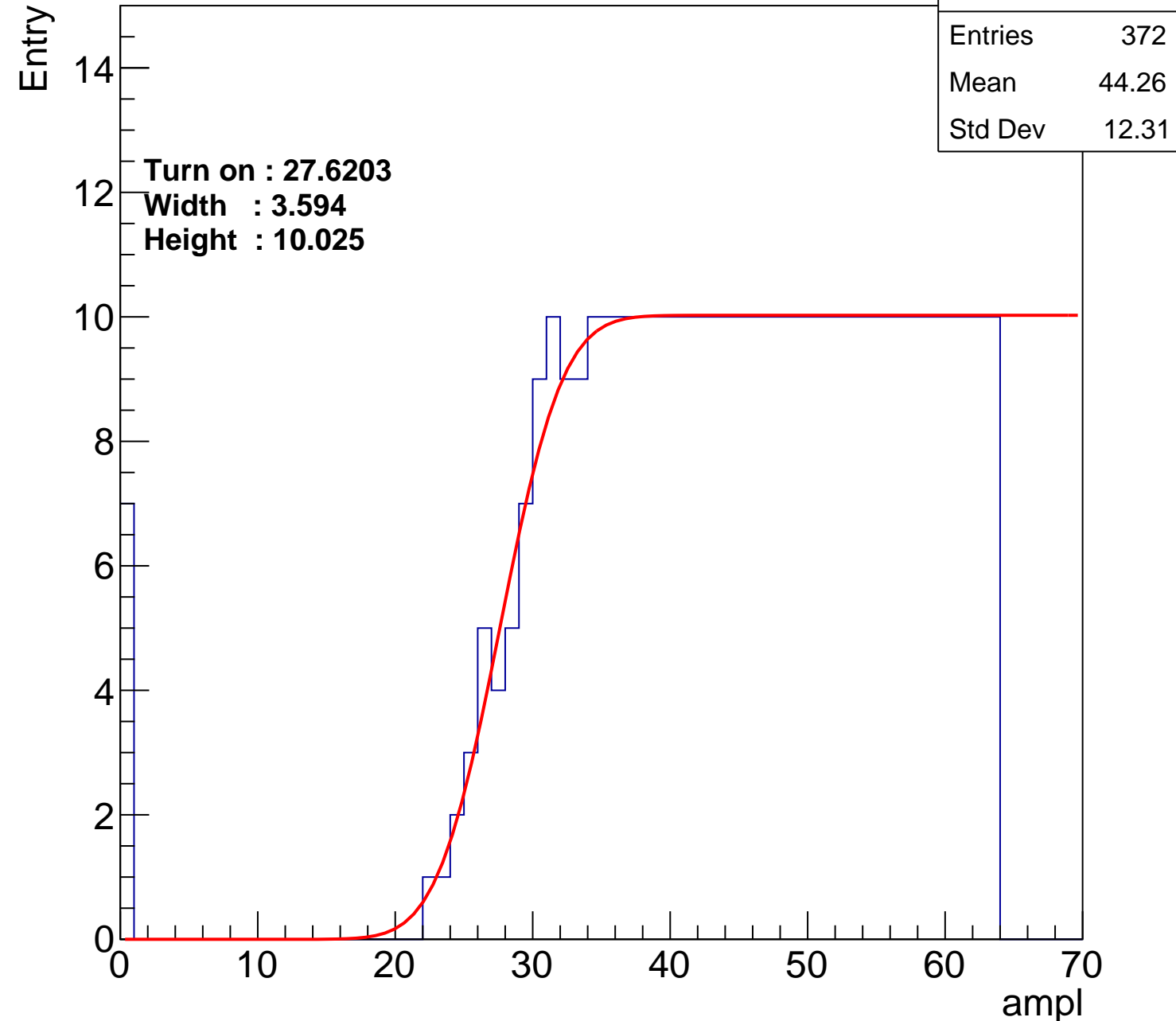
Width : 3.594

Height : 10.025

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U16-ch118

calib\_packv5\_042523\_0143.root, FC#0, port D2

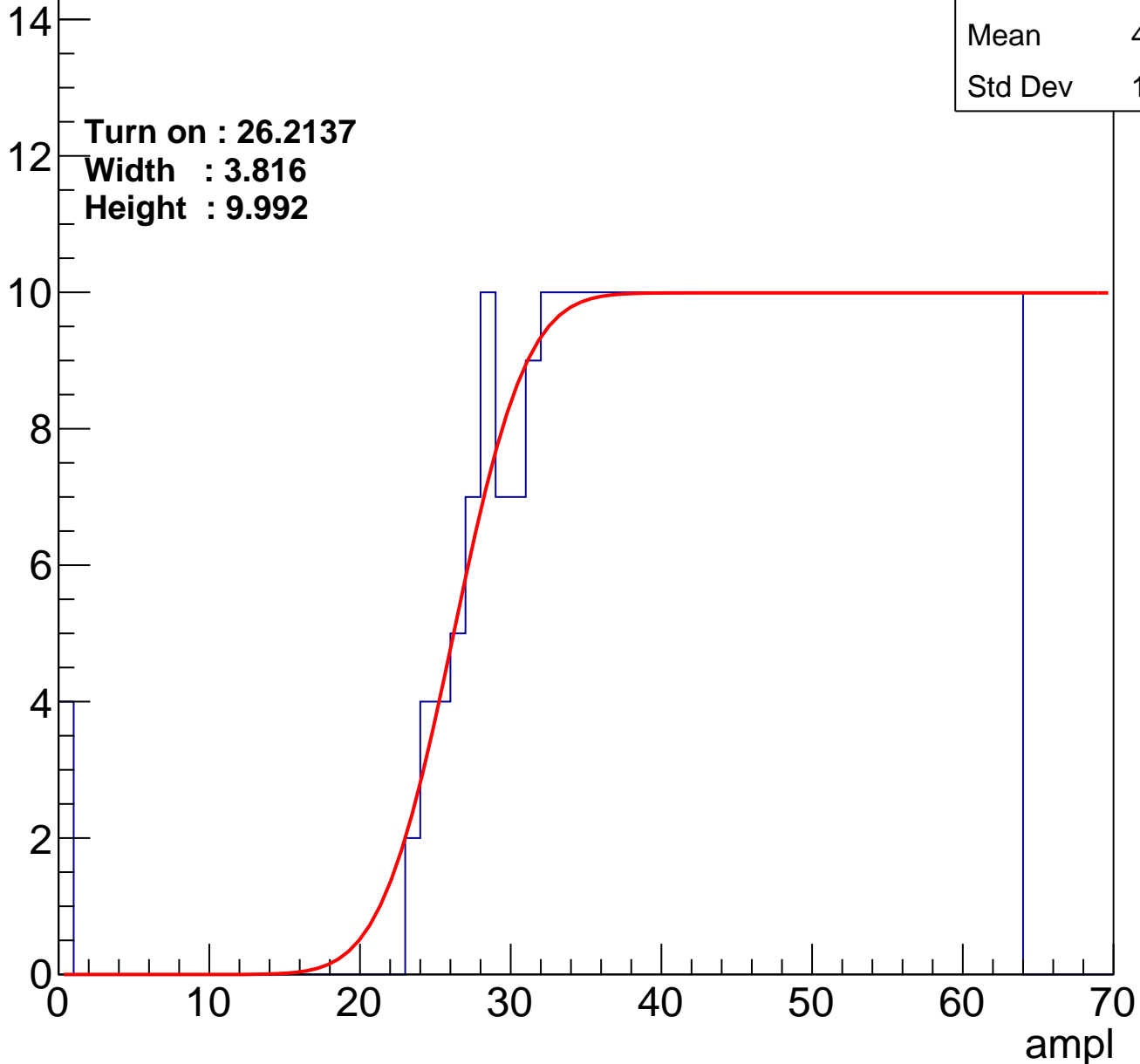
Entries	379
Mean	44.15
Std Dev	11.88

**Turn on : 26.2137**

**Width : 3.816**

**Height : 9.992**

Entry





# B1L101S, U16-ch119

calib\_packv5\_042523\_0143.root, FC#0, port D2

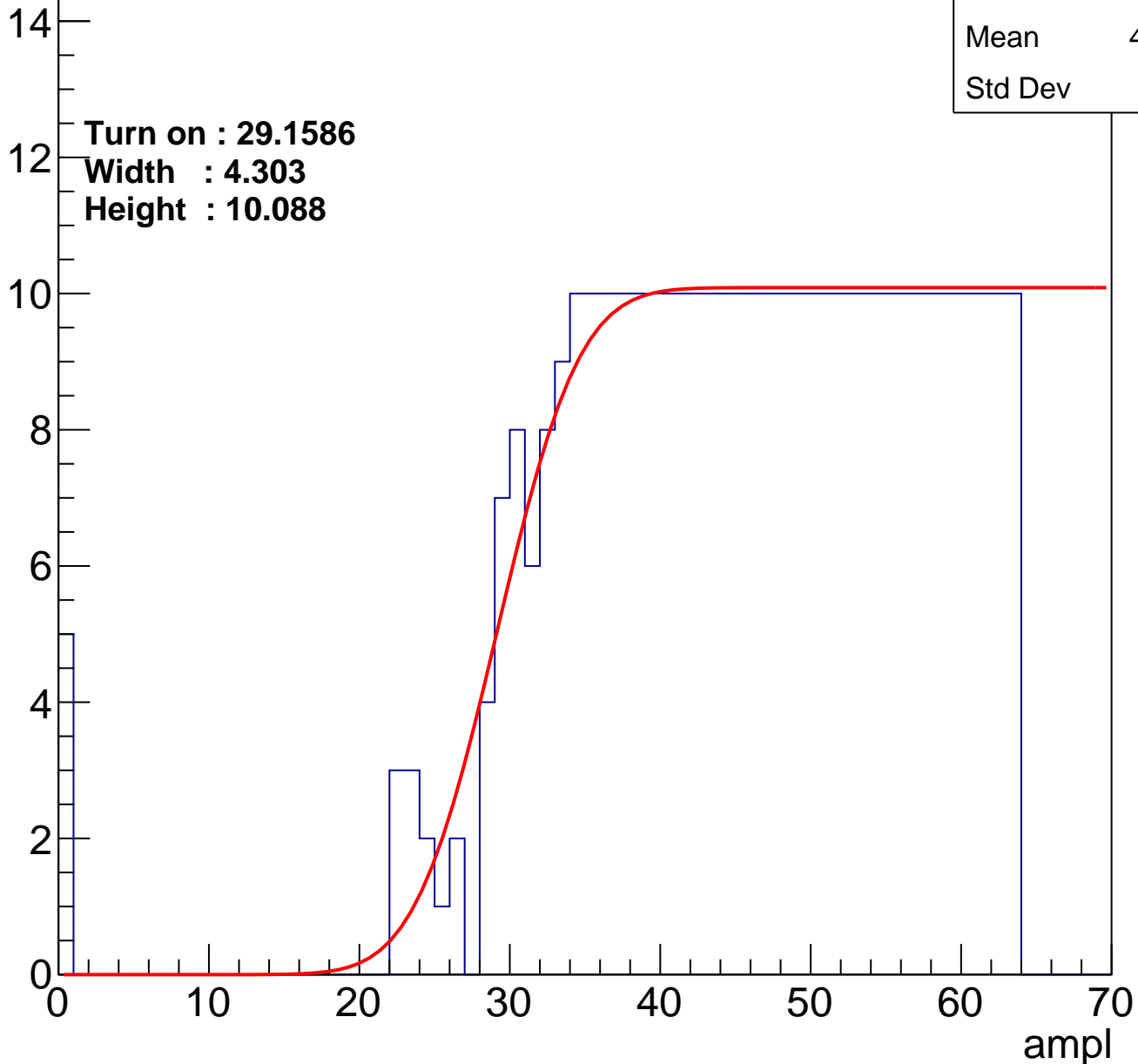
Entries	358
Mean	44.98
Std Dev	11.8

Turn on : 29.1586

Width : 4.303

Height : 10.088

Entry



# B1L101S, U16-ch120

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	398
Mean	43.18
Std Dev	12.47

Turn on : 25.0425

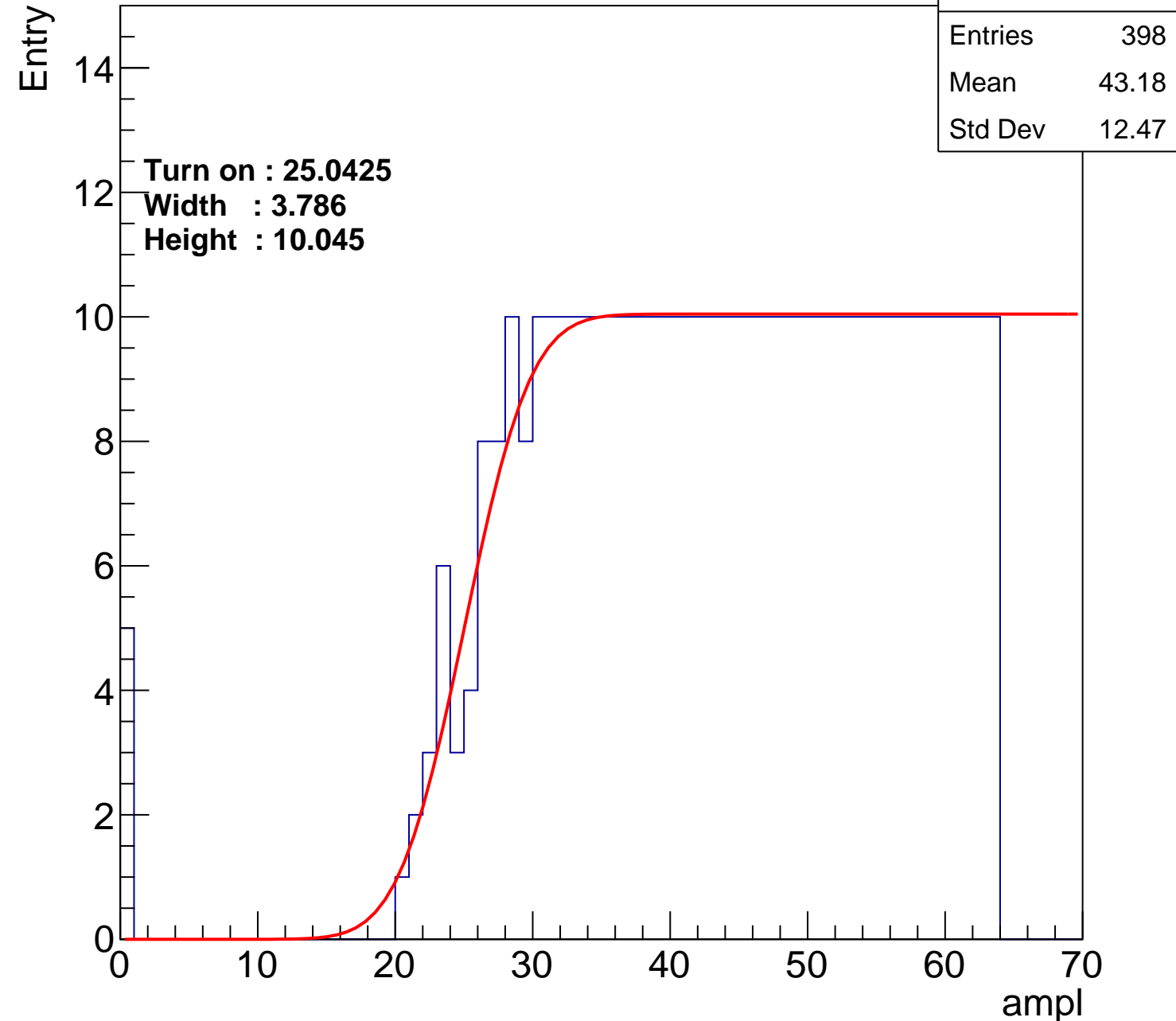
Width : 3.786

Height : 10.045

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U16-ch121

calib\_packv5\_042523\_0143.root, FC#0, port D2

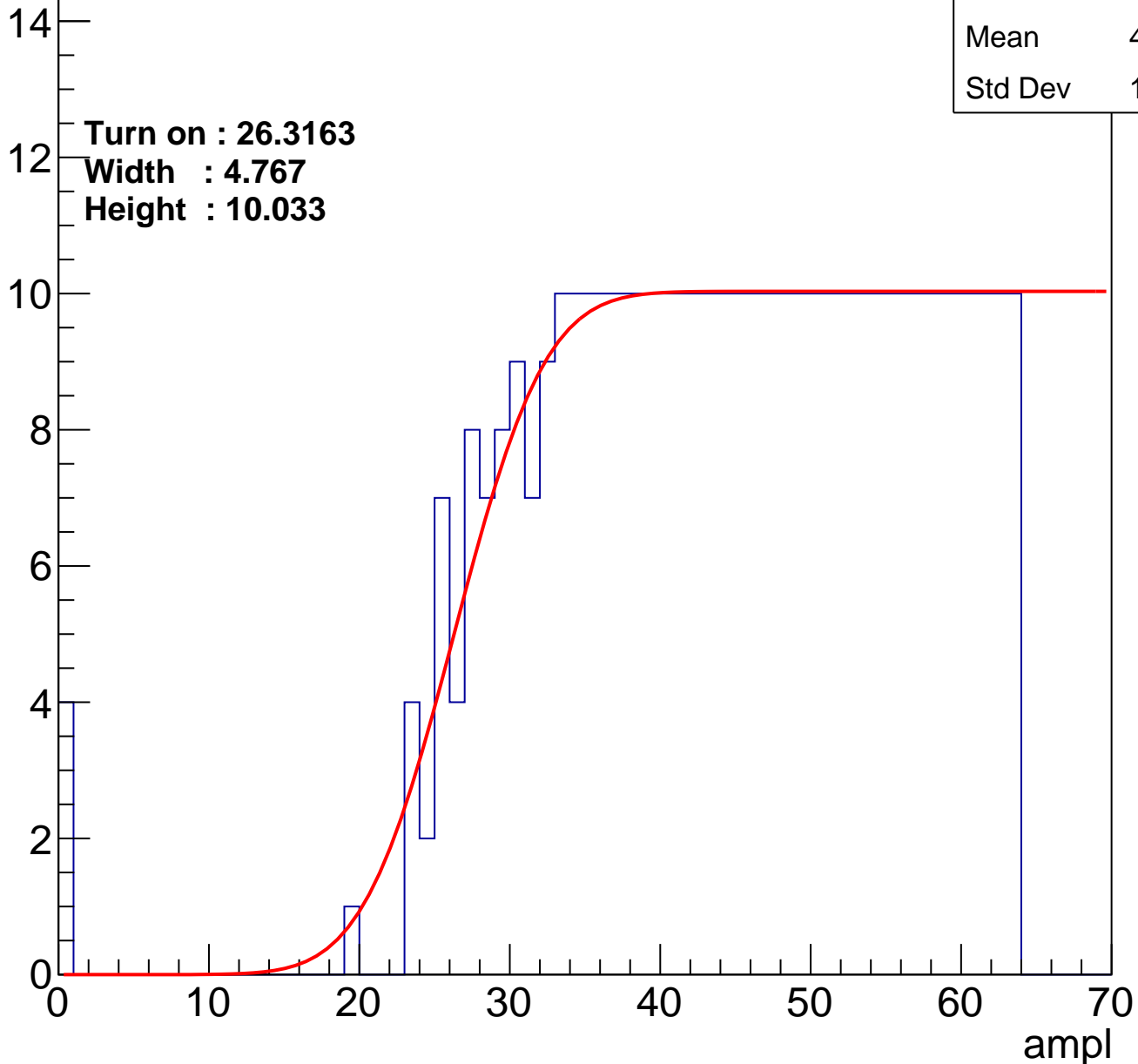
Entries	380
Mean	44.04
Std Dev	11.99

Turn on : 26.3163

Width : 4.767

Height : 10.033

Entry



# B1L101S, U16-ch122

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	371
Mean	44.71
Std Dev	11.18

**Turn on : 26.8760**

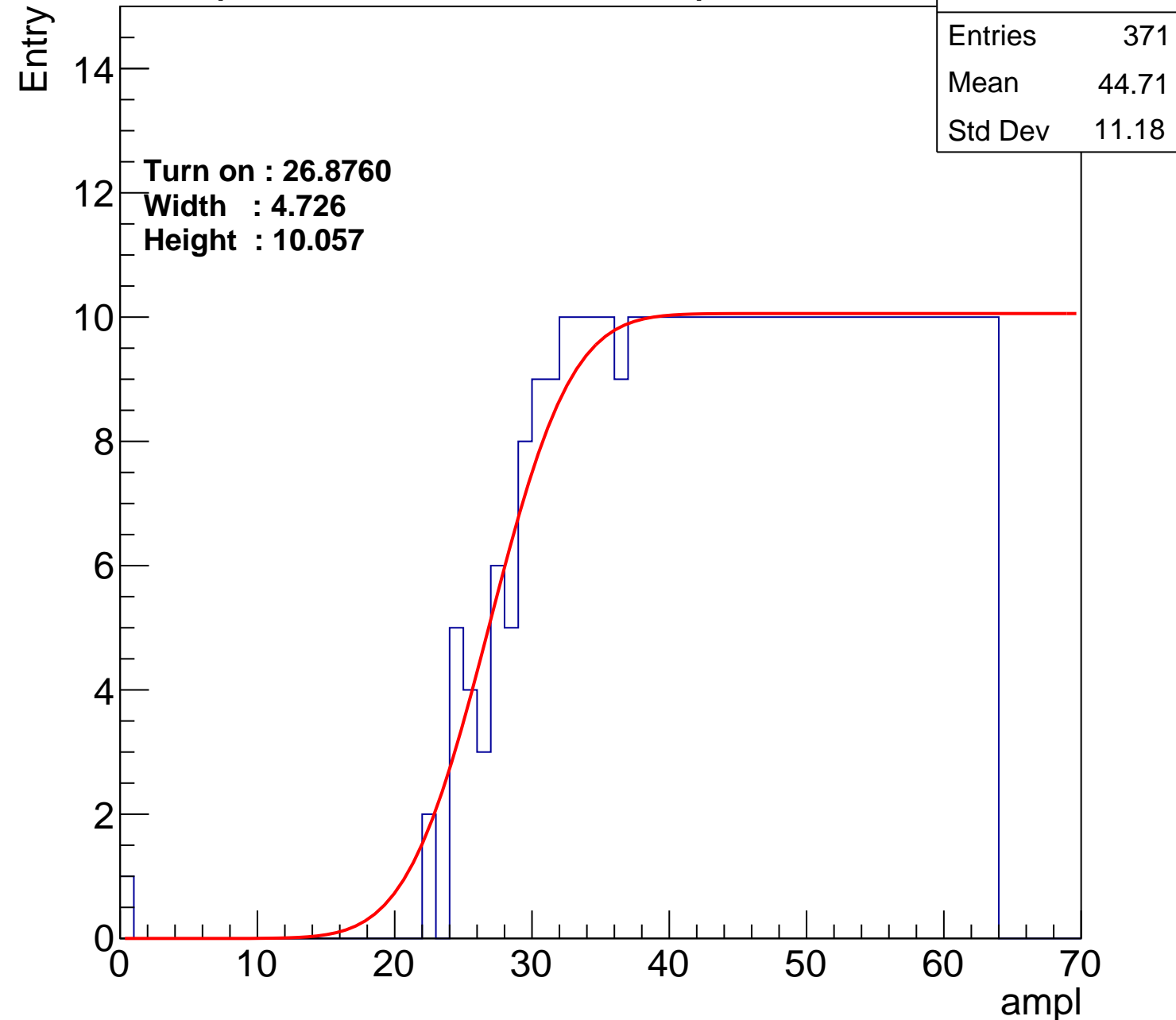
**Width : 4.726**

**Height : 10.057**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U16-ch123

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	377
Mean	44.37
Std Dev	11.59

Turn on : 27.2197

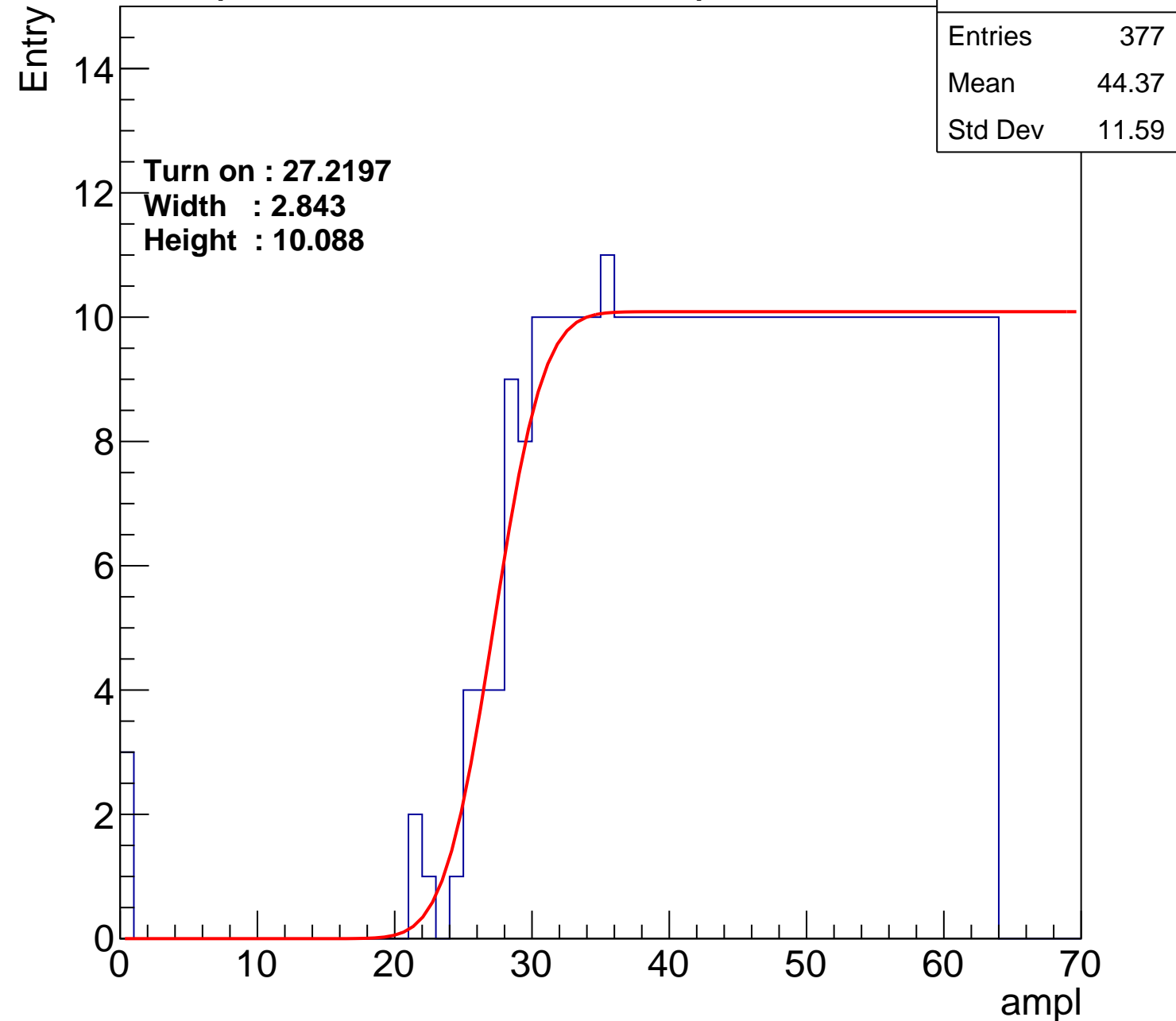
Width : 2.843

Height : 10.088

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U16-ch124

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	400
Mean	43.23
Std Dev	12.17

Turn on : 24.6146

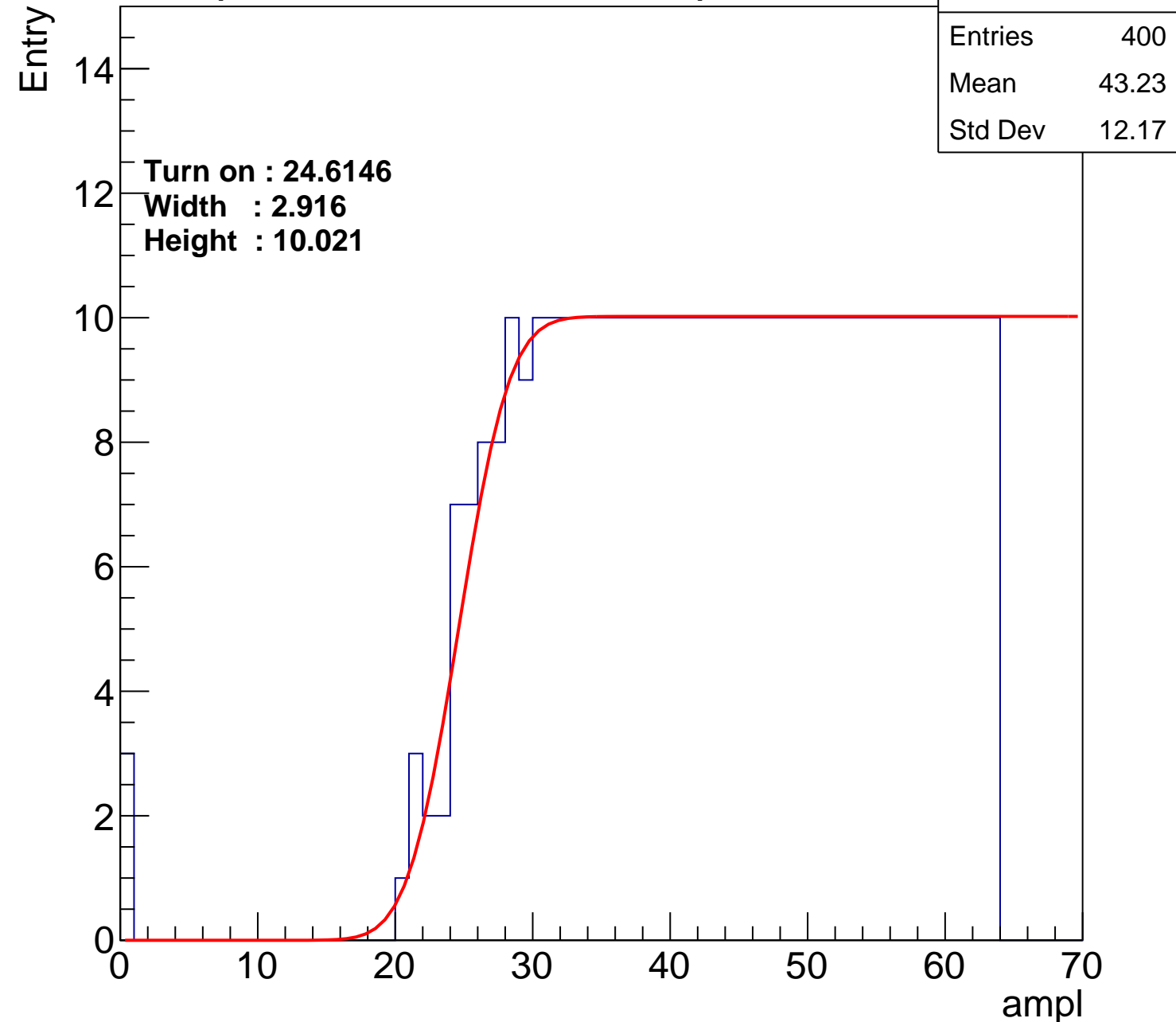
Width : 2.916

Height : 10.021

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U16-ch125

calib\_packv5\_042523\_0143.root, FC#0, port D2

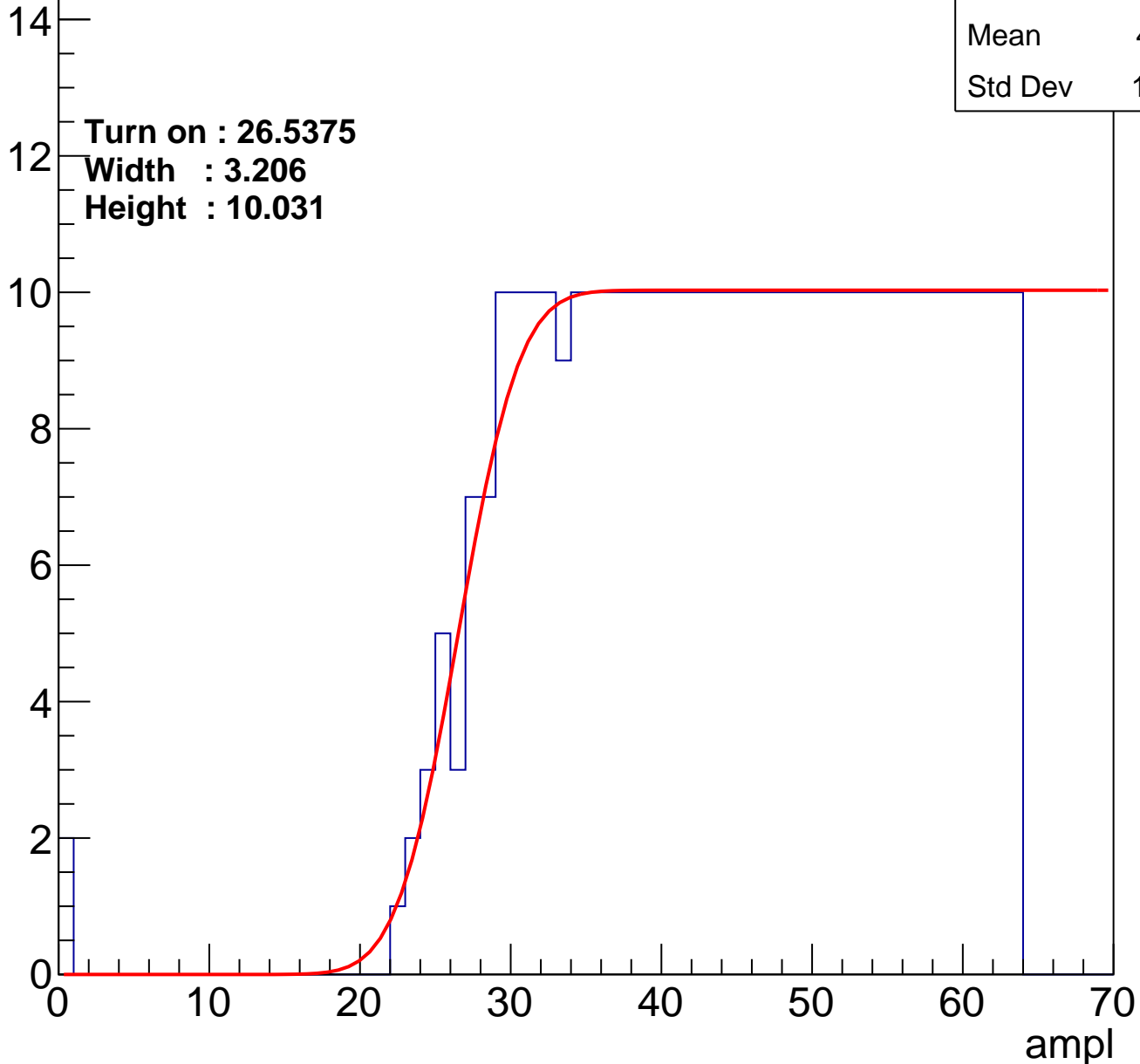
Entries	379
Mean	44.31
Std Dev	11.48

Turn on : 26.5375

Width : 3.206

Height : 10.031

Entry



# B1L101S, U16-ch126

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	394
Mean	43.51
Std Dev	12.08

Turn on : 24.8535

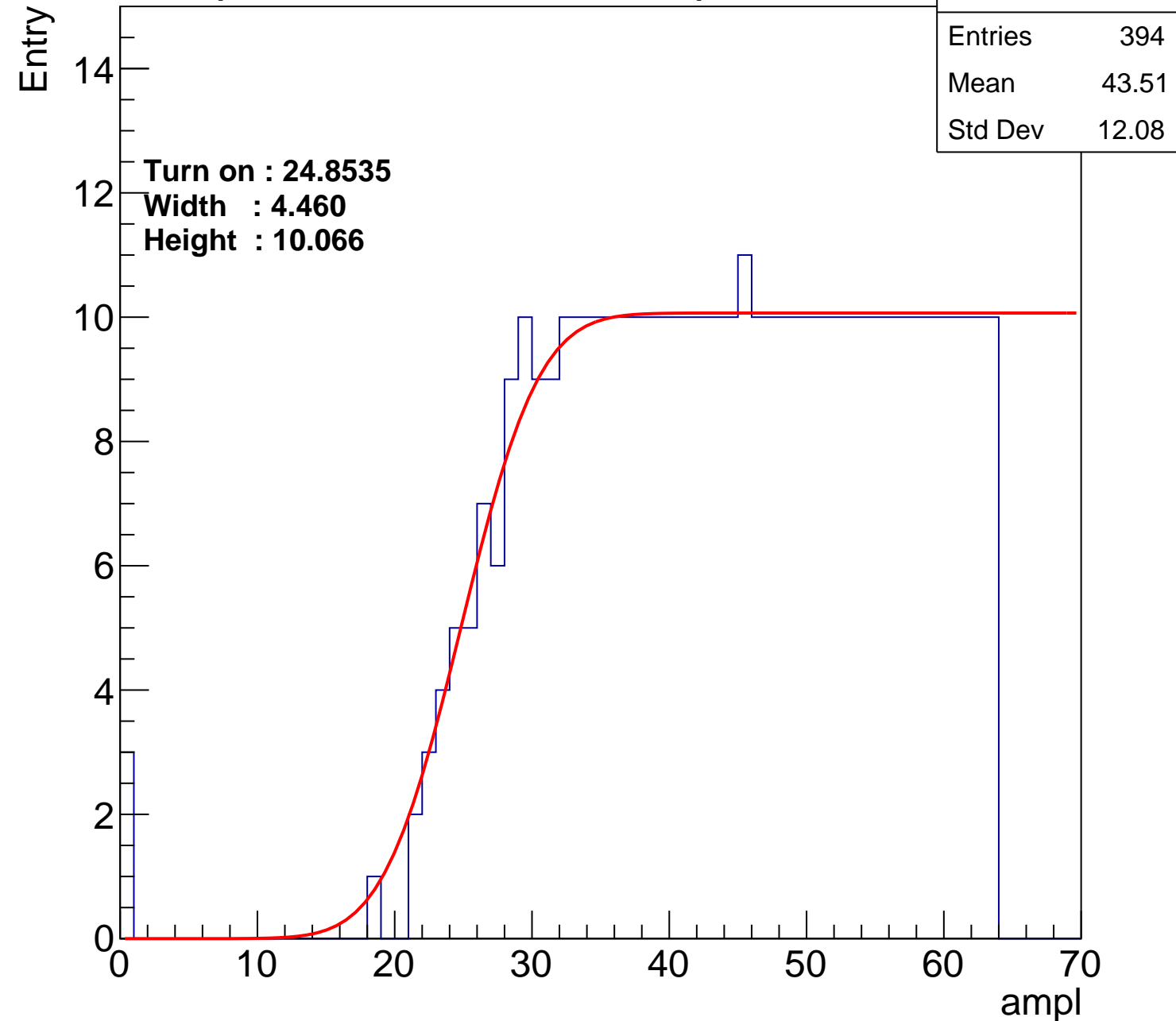
Width : 4.460

Height : 10.066

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L101S, U16-ch127

calib\_packv5\_042523\_0143.root, FC#0, port D2

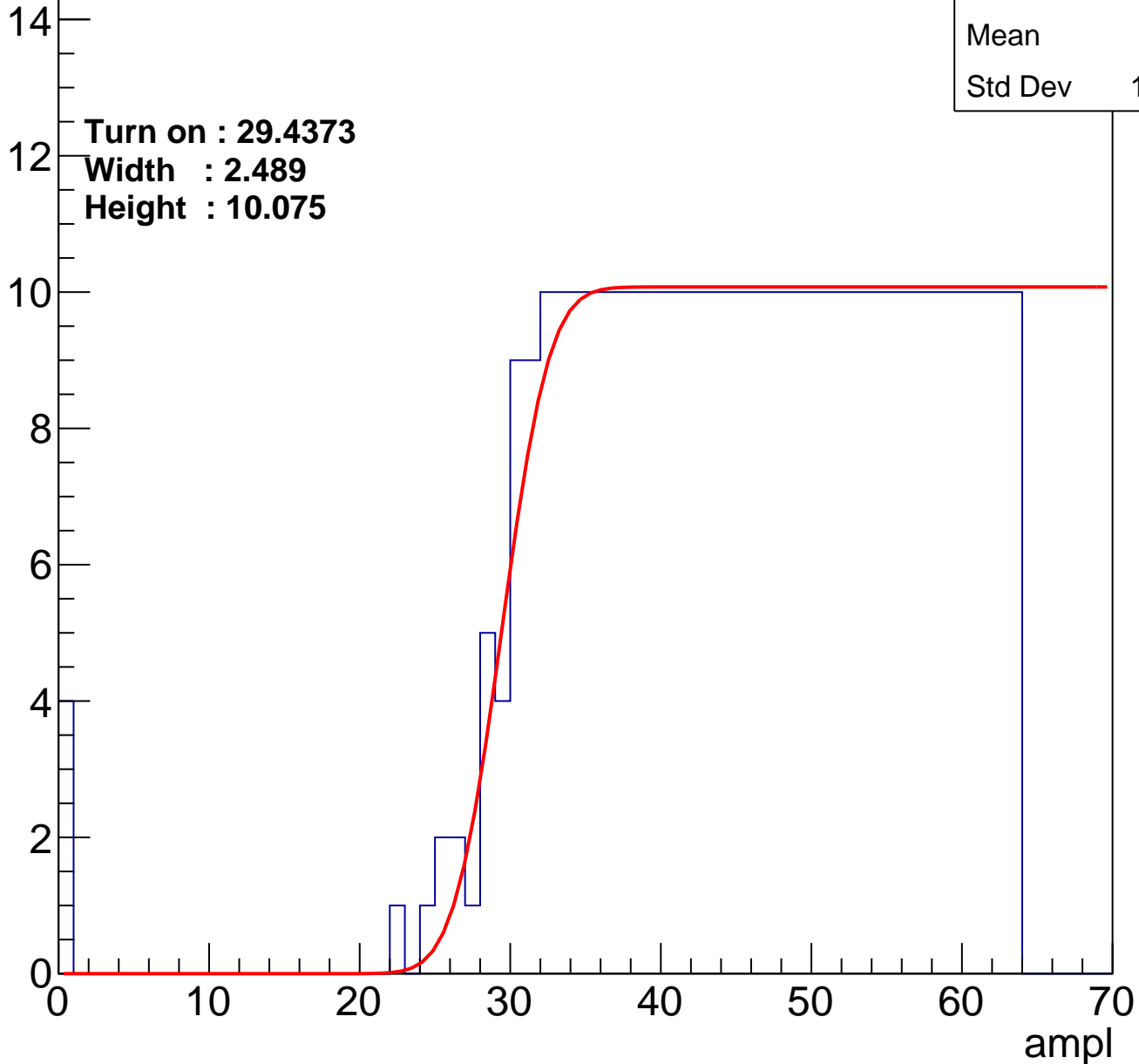
Entries	358
Mean	45.2
Std Dev	11.39

**Turn on : 29.4373**

**Width : 2.489**

**Height : 10.075**

Entry



# B1L101S, U16-ch127

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	358
Mean	45.2
Std Dev	11.39

**Turn on : 29.4373**

**Width : 2.489**

**Height : 10.075**

Entry

