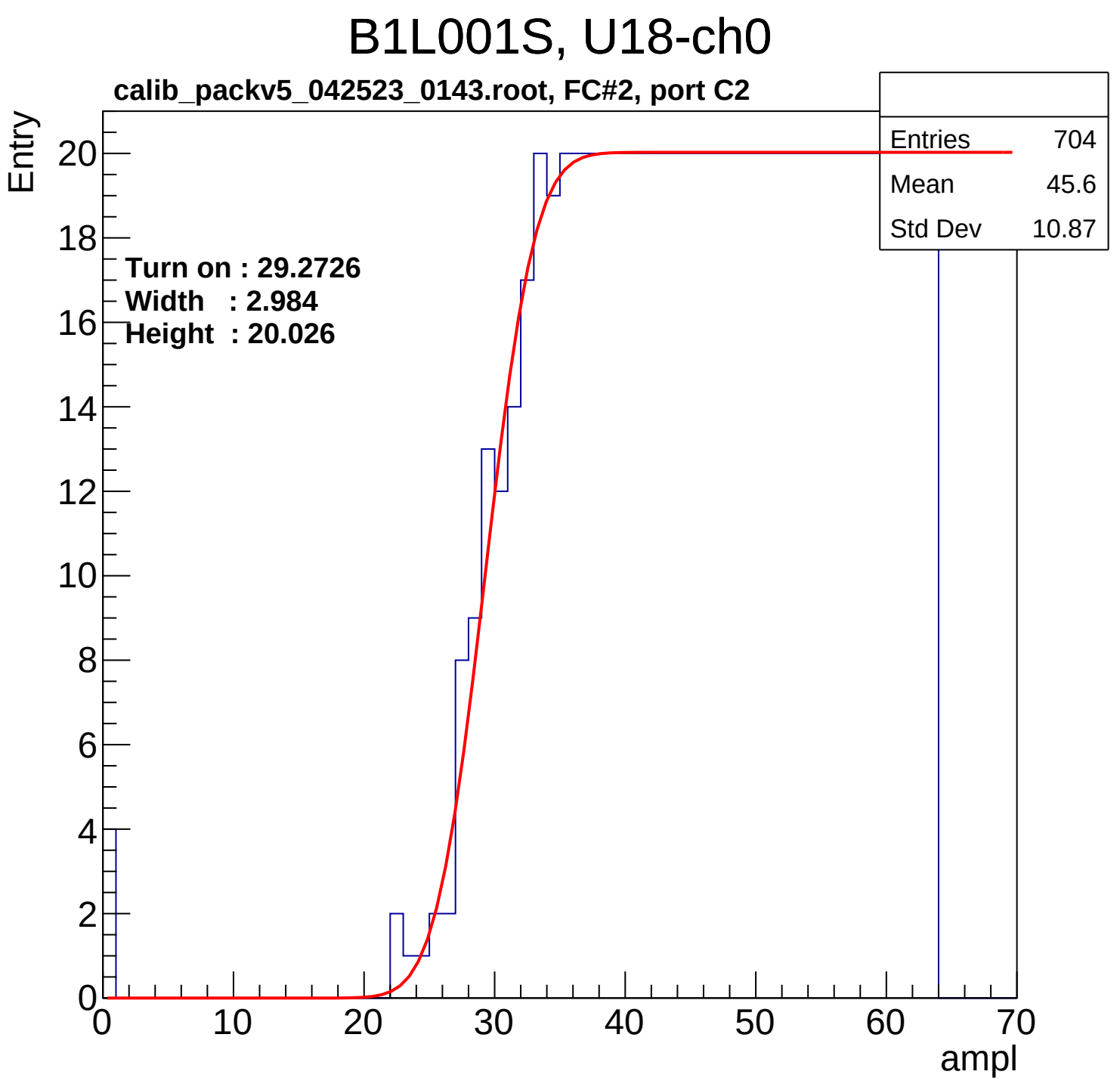
B1L001S, U18-ch0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 704
Mean 45.6
Std Dev 10.87
Turn on : 29.2726
Width : 2.984
Height : 20.026
Entry
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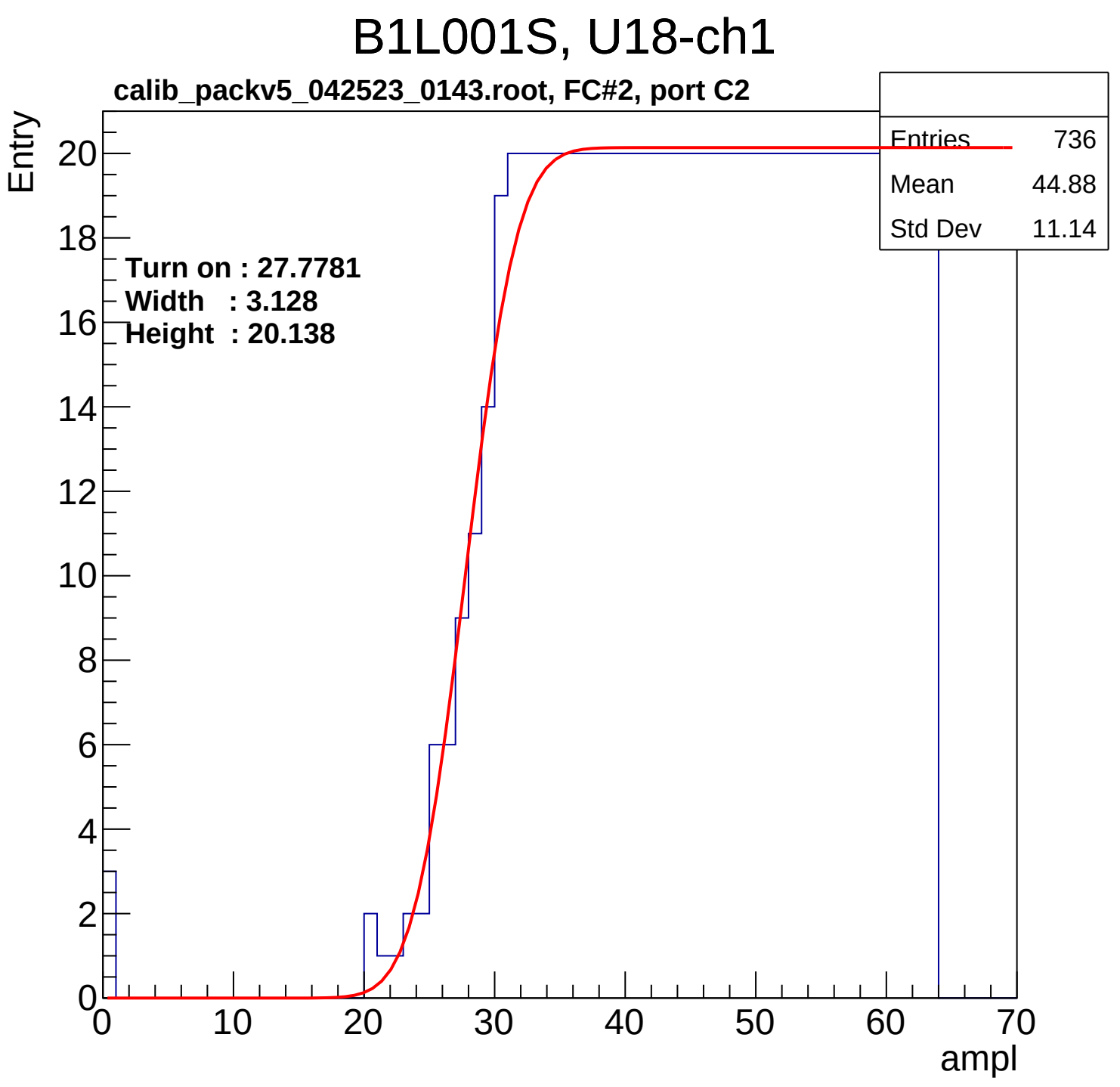
B1L001S, U18-ch1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 736
Mean 44.88
Std Dev 11.14
Turn on : 27.7781
Width : 3.128
Height : 20.138
Entry
ampl
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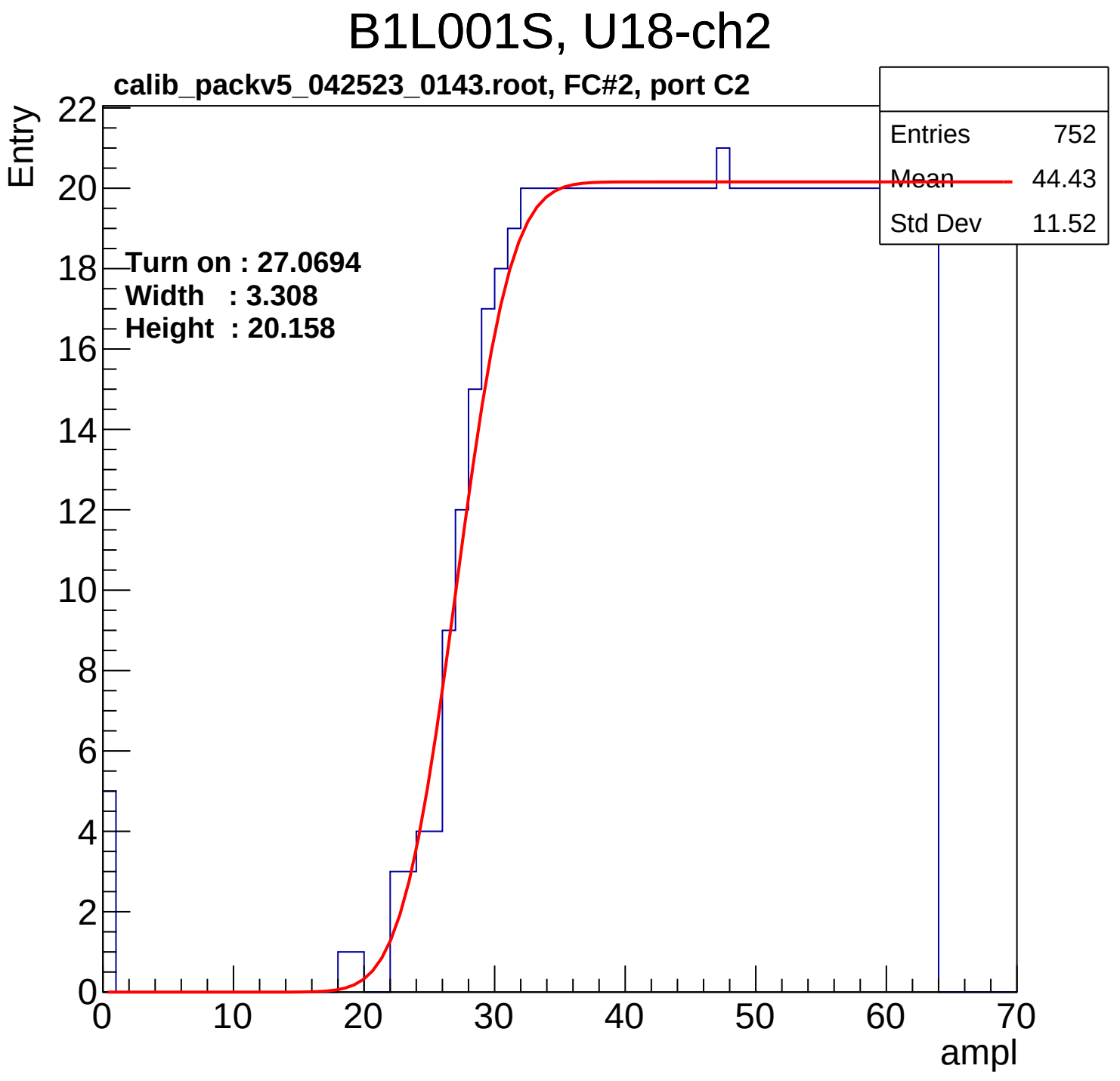
B1L001S, U18-ch2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 752
Mean 44.43
Std Dev 11.52
Turn on : 27.0694
Width : 3.308
Height : 20.158
Entry
ampl
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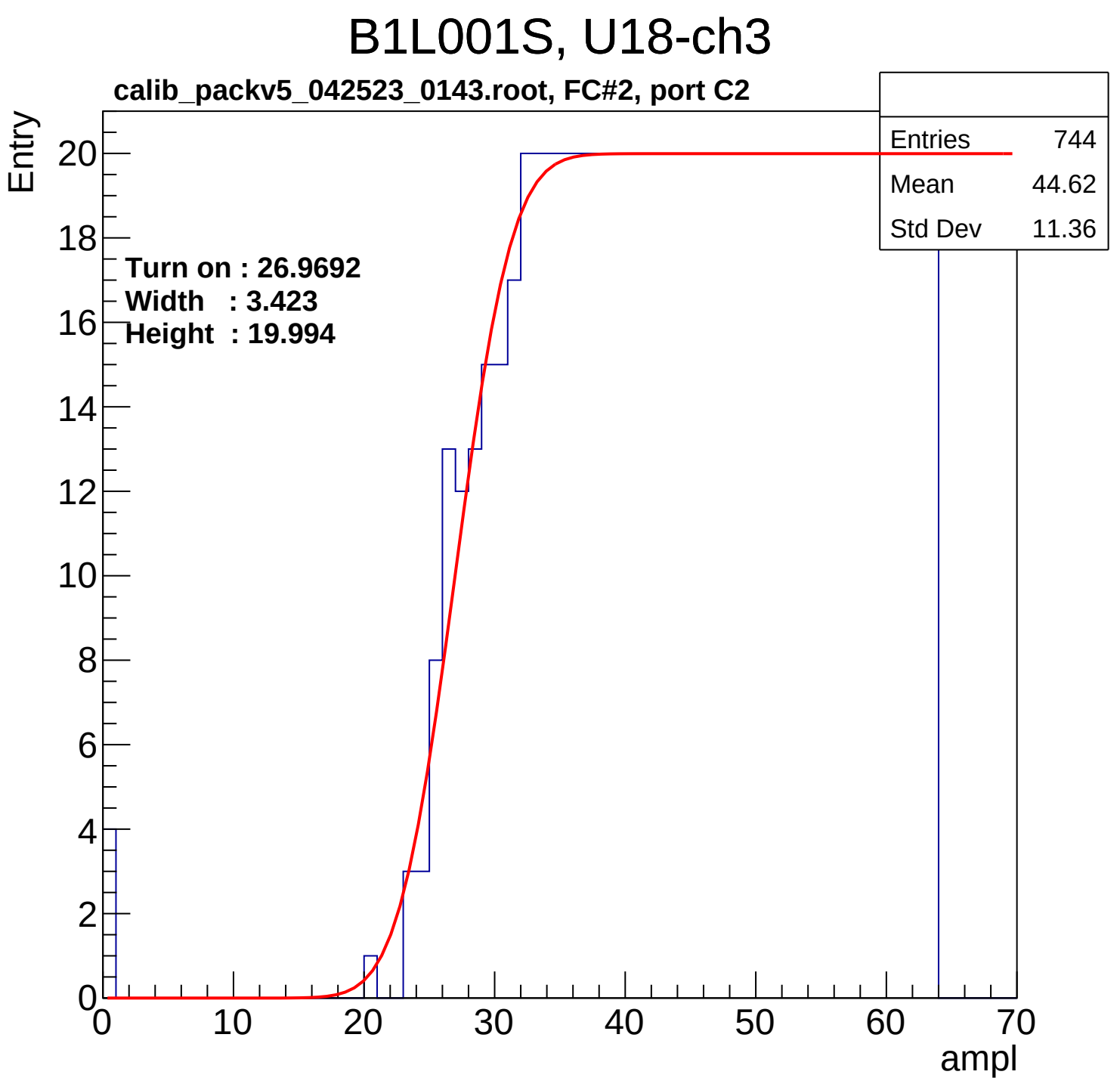
B1L001S, U18-ch3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 744
Mean 44.62
Std Dev 11.36
Turn on : 26.9692
Width : 3.423
Height : 19.994
Entry
ampl
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6
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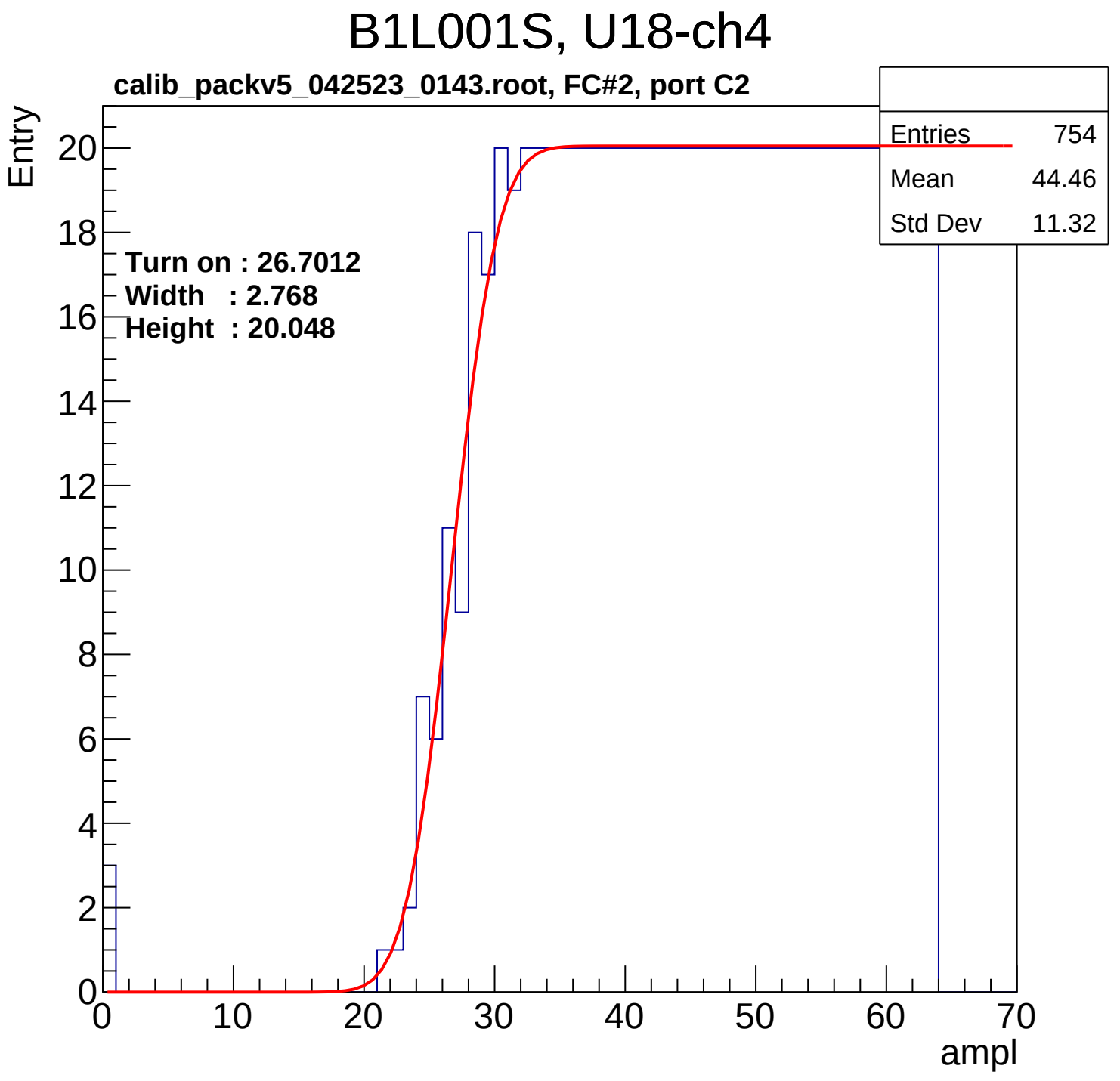
B1L001S, U18-ch4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 754
Mean 44.46
Std Dev 11.32
Turn on : 26.7012
Width : 2.768
Height : 20.048
Entry
ampl
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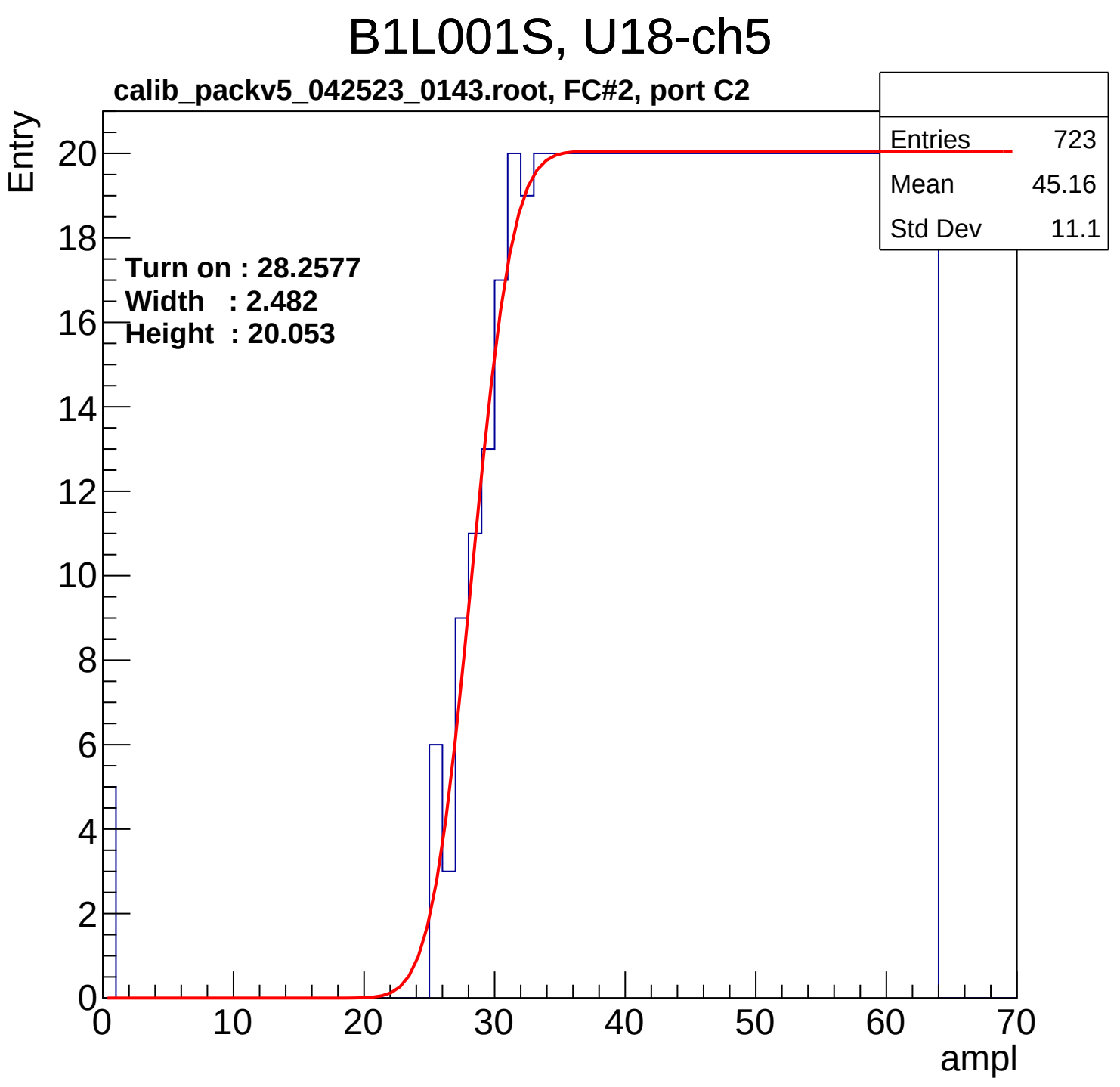
B1L001S, U18-ch5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 723
Mean 45.16
Std Dev 11.1
Turn on : 28.2577
Width : 2.482
Height : 20.053
Entry
ampl
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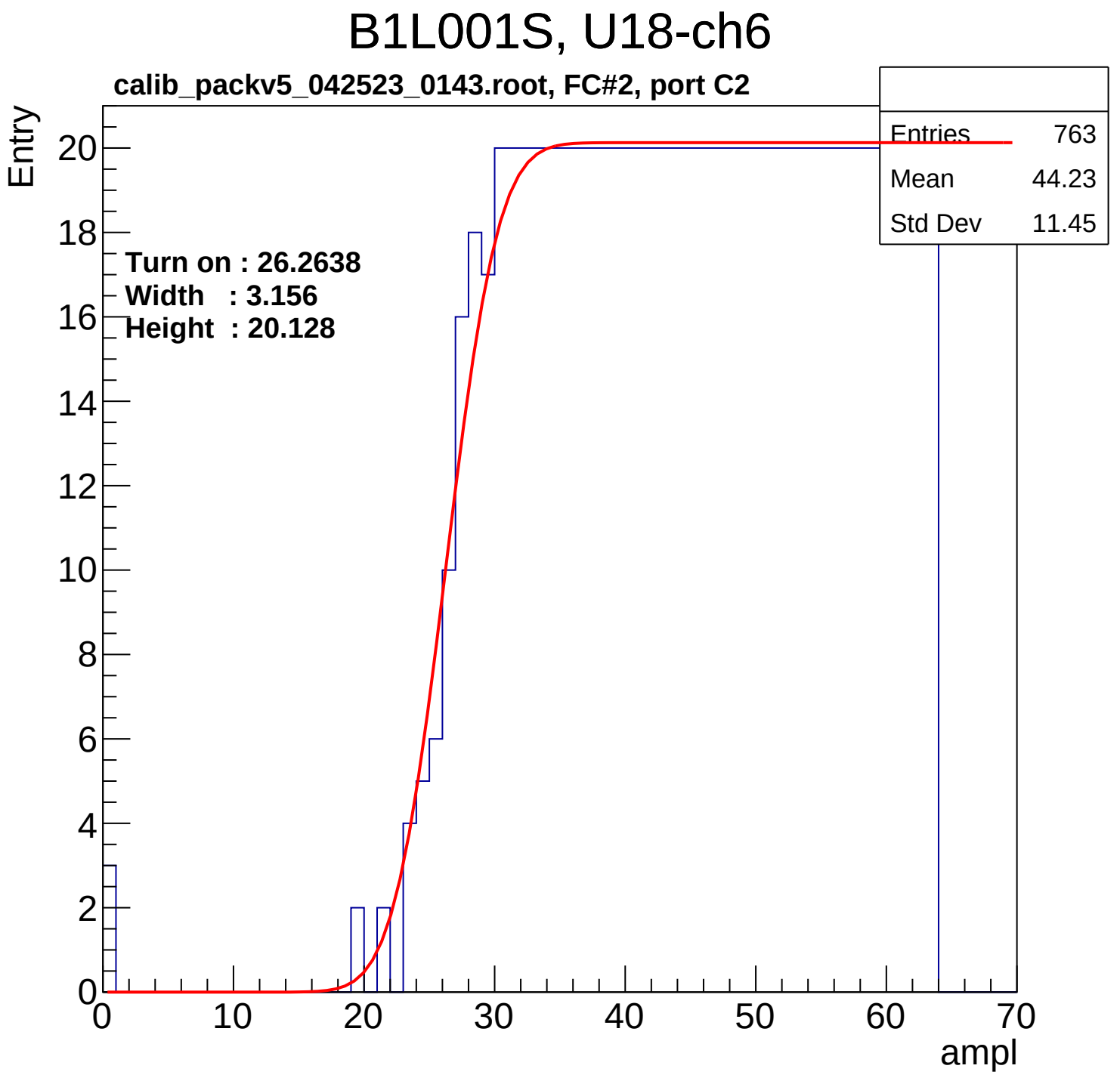
B1L001S, U18-ch6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 763
Mean 44.23
Std Dev 11.45
Turn on : 26.2638
Width : 3.156
Height : 20.128
Entry
ampl
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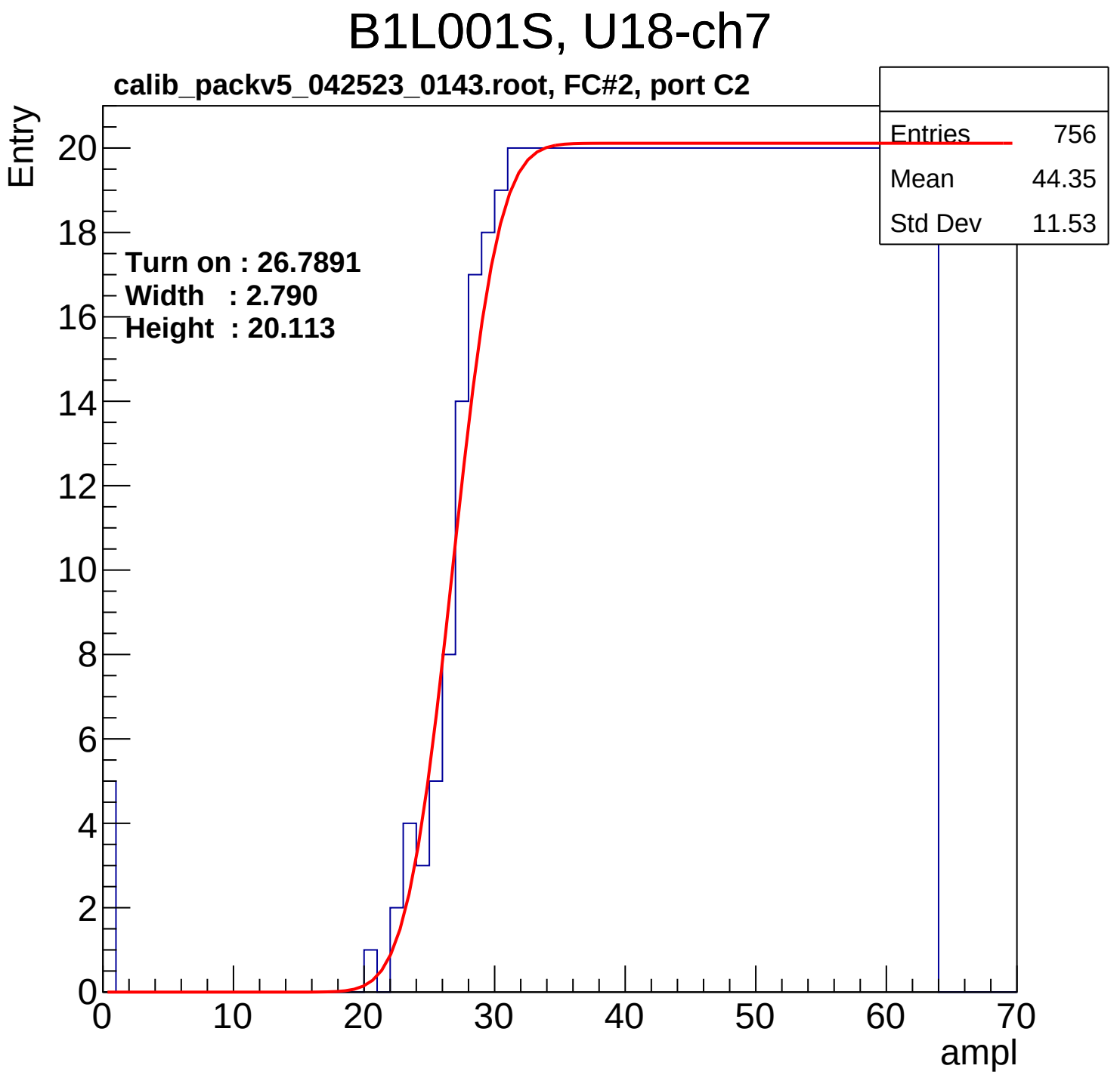
B1L001S, U18-ch7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 756
Mean 44.35
Std Dev 11.53
Turn on : 26.7891
Width : 2.790
Height : 20.113
Entry
ampl
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6
8
10
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14
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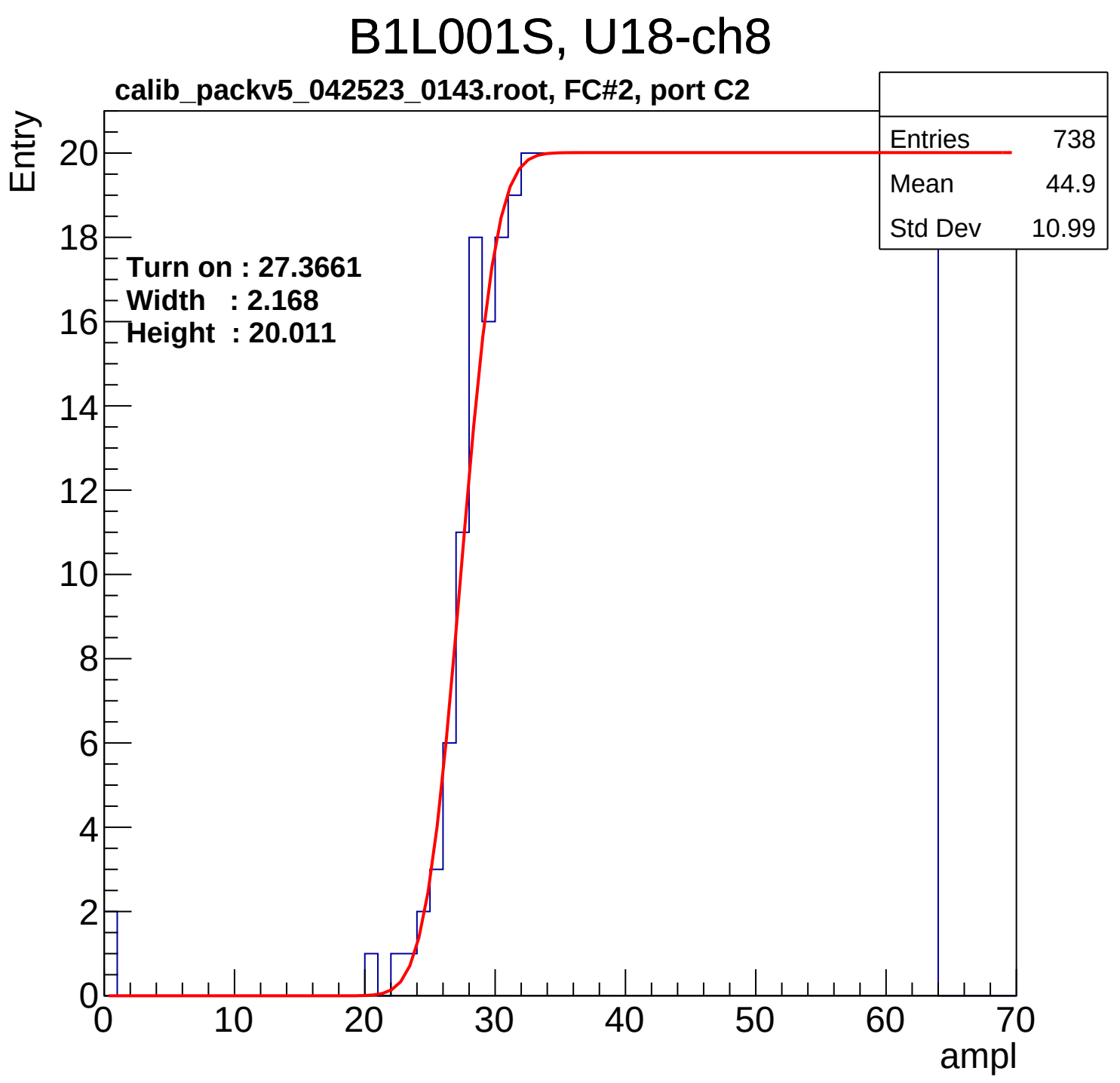
B1L001S, U18-ch8
calib_packv5_042523_0143.root, FC#2, port C2
Entries 738
Mean 44.9
Std Dev 10.99
Turn on : 27.3661
Width : 2.168
Height : 20.011
Entry
ampl
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6
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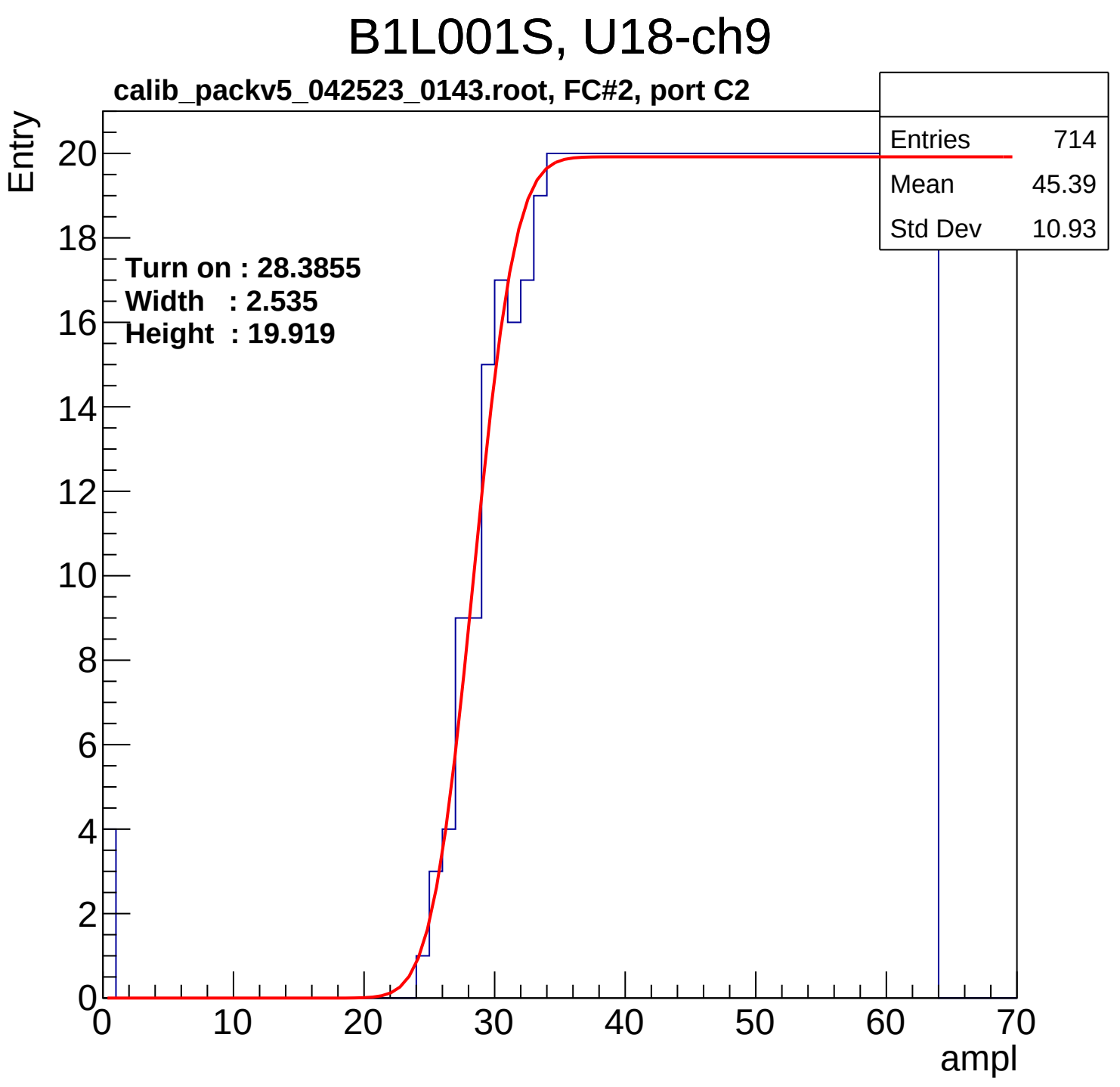
B1L001S, U18-ch9
calib_packv5_042523_0143.root, FC#2, port C2
Entries 714
Mean 45.39
Std Dev 10.93
Turn on : 28.3855
Width : 2.535
Height : 19.919
Entry
ampl
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6
8
10
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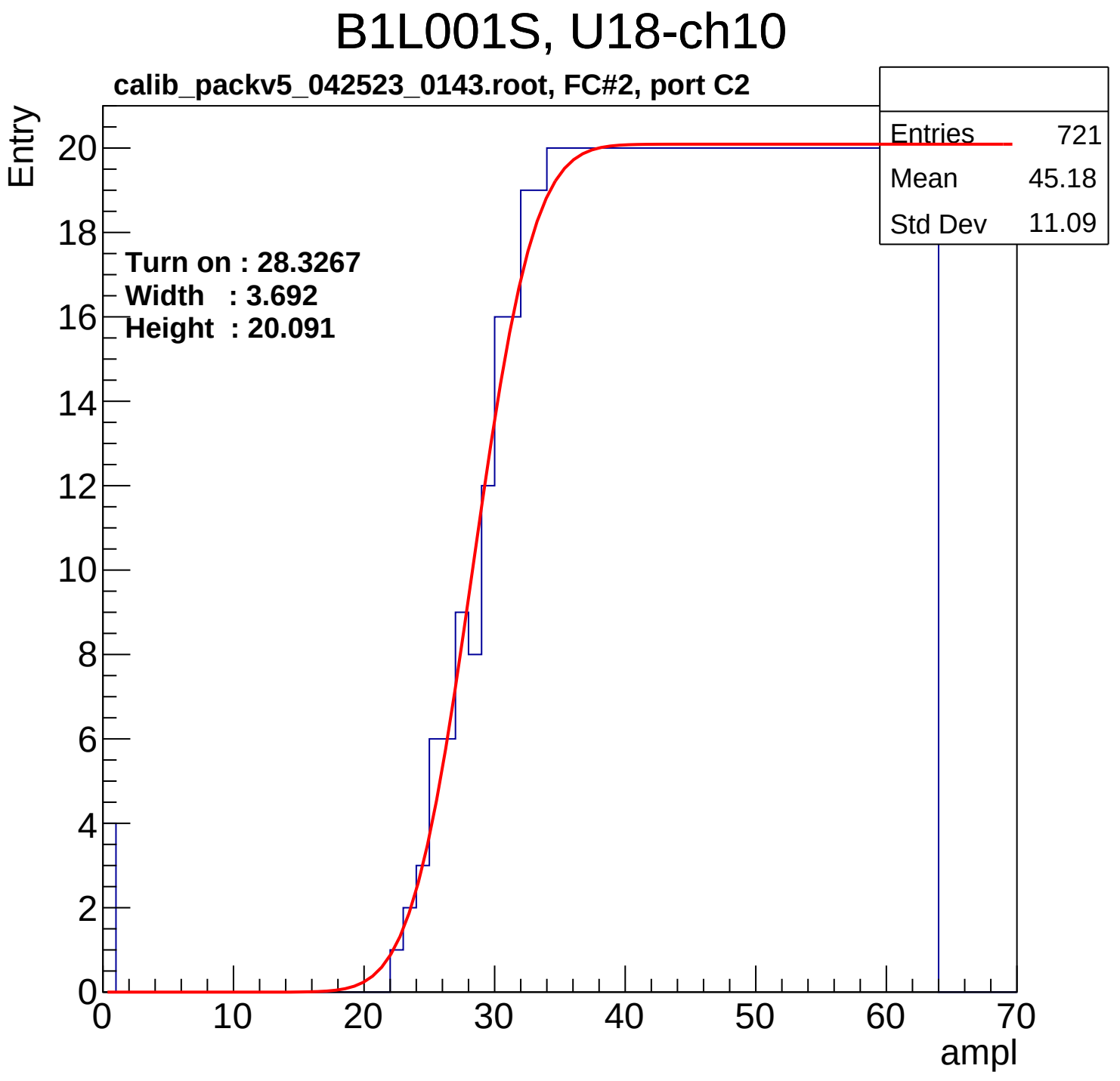
B1L001S, U18-ch10
calib_packv5_042523_0143.root, FC#2, port C2
Entries 721
Mean 45.18
Std Dev 11.09
Turn on : 28.3267
Width : 3.692
Height : 20.091
Entry
ampl
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6
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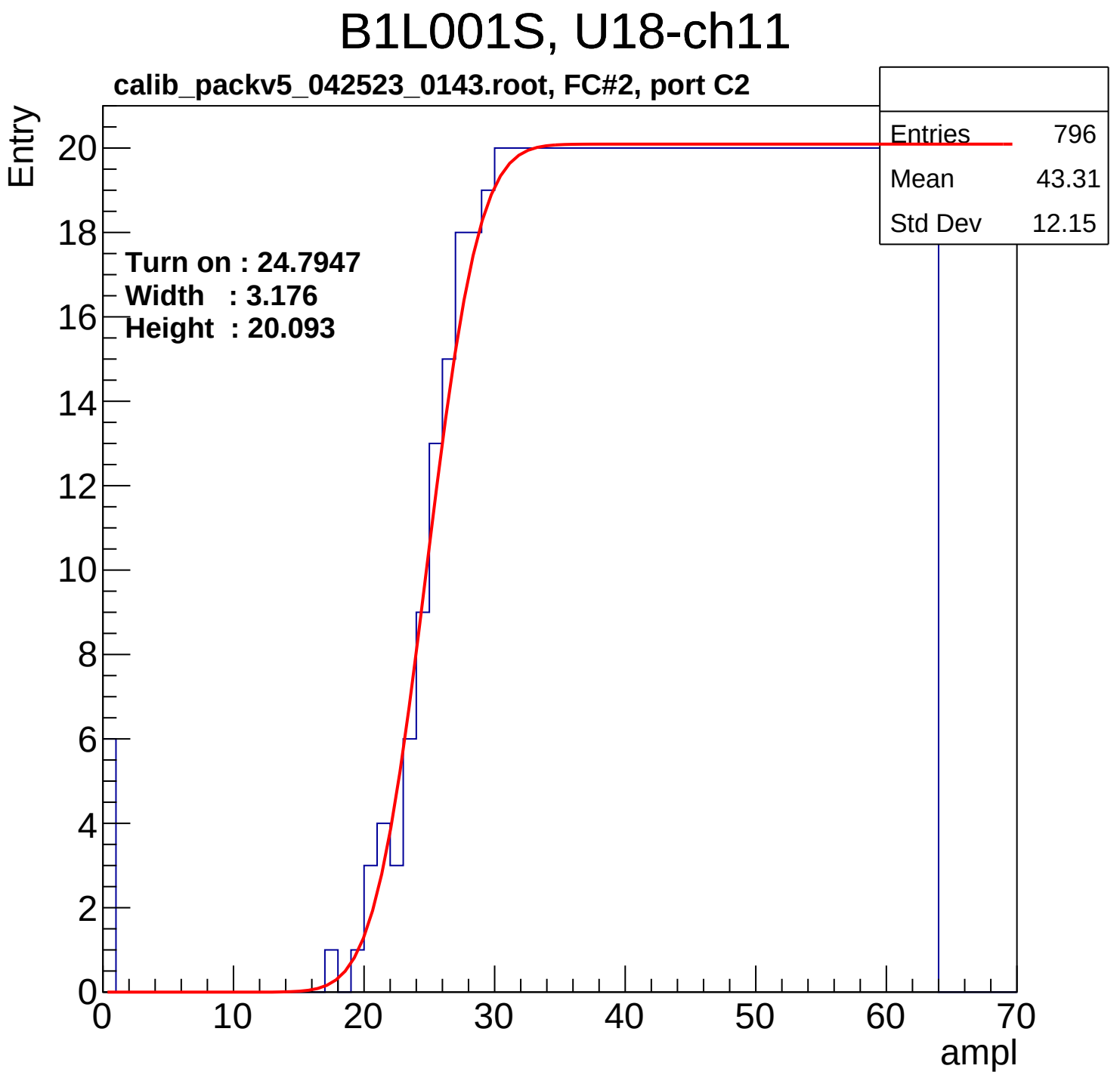
B1L001S, U18-ch11
calib_packv5_042523_0143.root, FC#2, port C2
Entries 796
Mean 43.31
Std Dev 12.15
Turn on : 24.7947
Width : 3.176
Height : 20.093
Entry
ampl
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8
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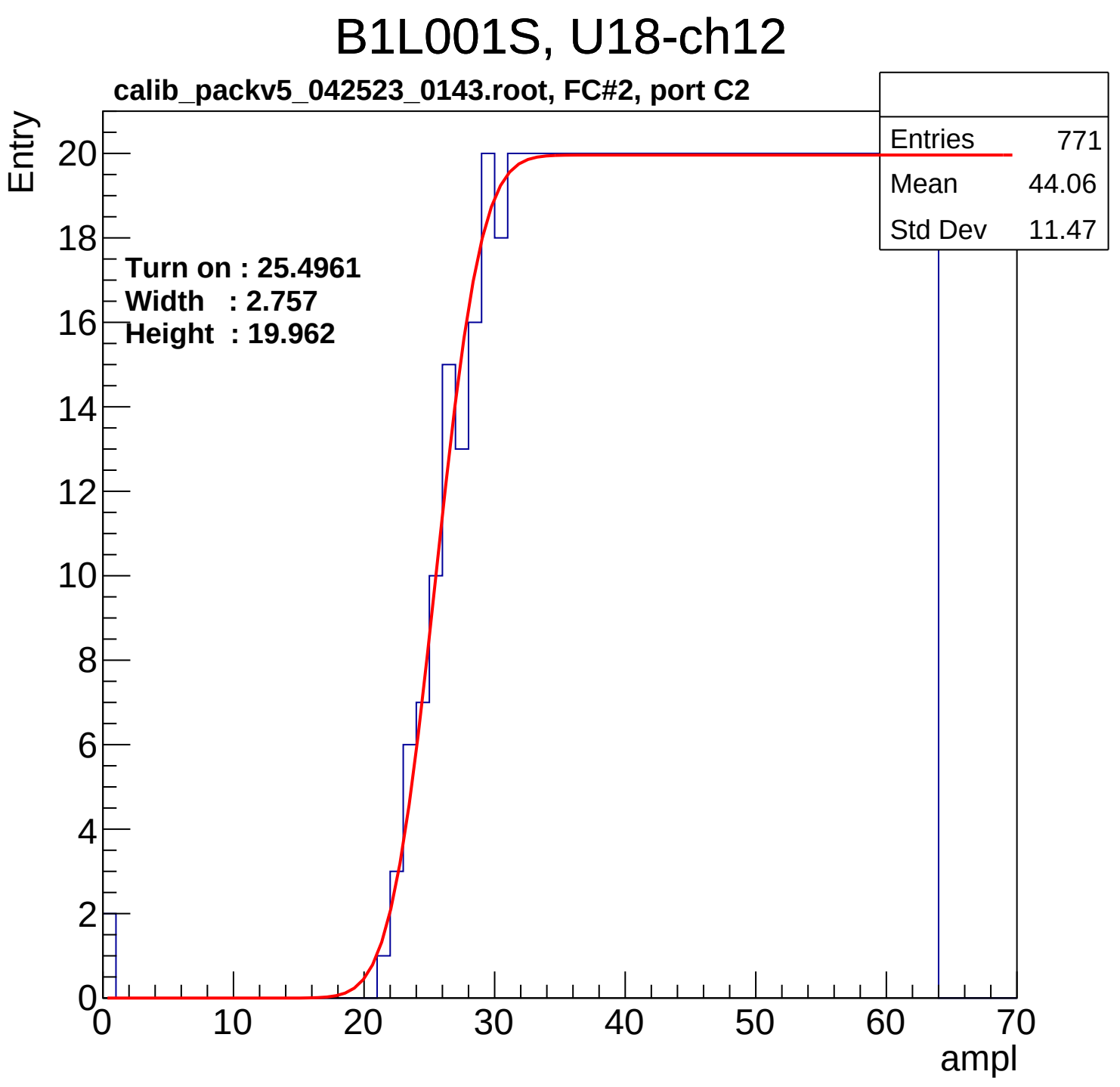
B1L001S, U18-ch12
calib_packv5_042523_0143.root, FC#2, port C2
Entries 771
Mean 44.06
Std Dev 11.47
Turn on : 25.4961
Width : 2.757
Height : 19.962
Entry
ampl
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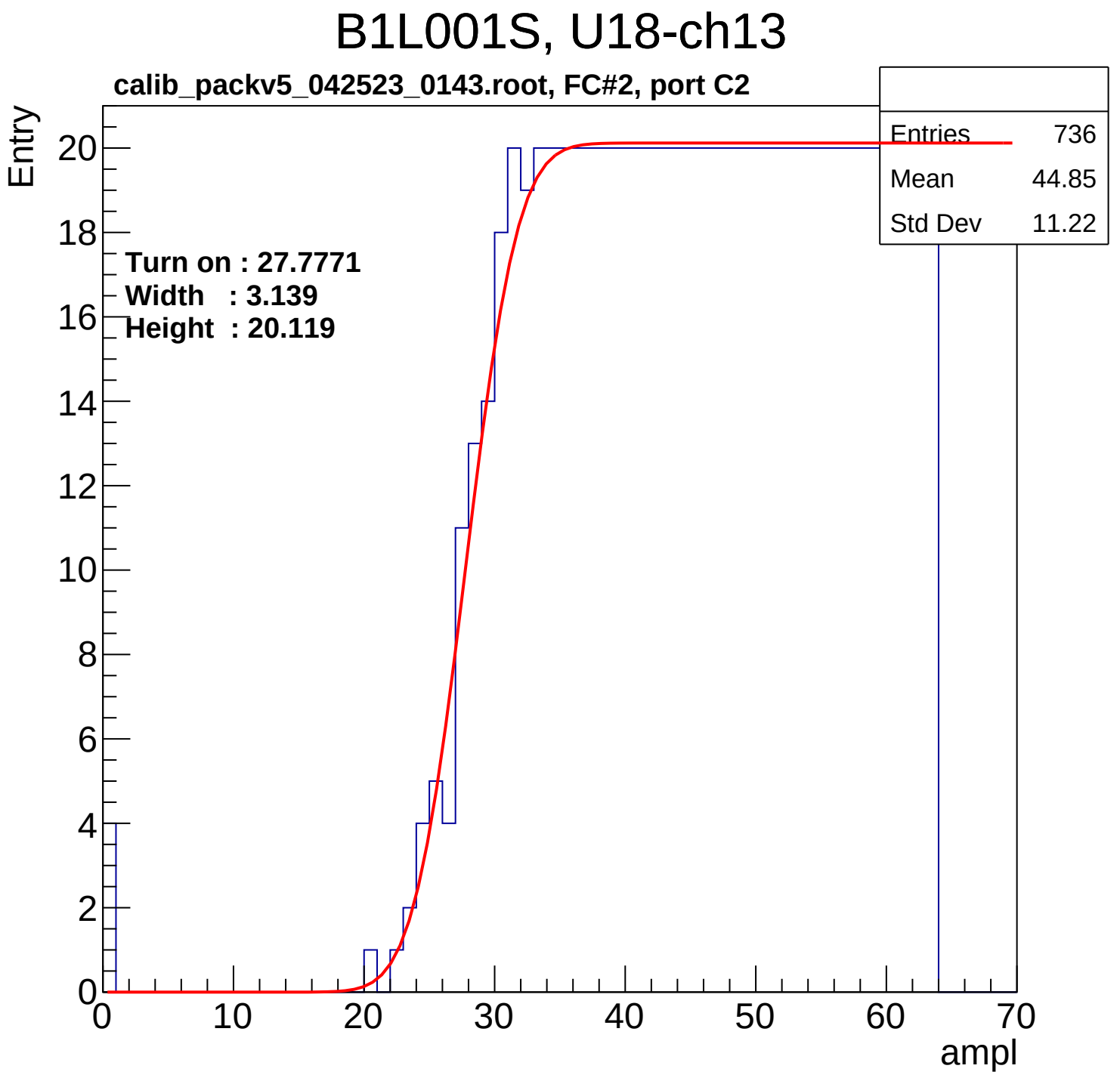
B1L001S, U18-ch13
calib_packv5_042523_0143.root, FC#2, port C2
Entries 736
Mean 44.85
Std Dev 11.22
Turn on : 27.7771
Width : 3.139
Height : 20.119
Entry
ampl
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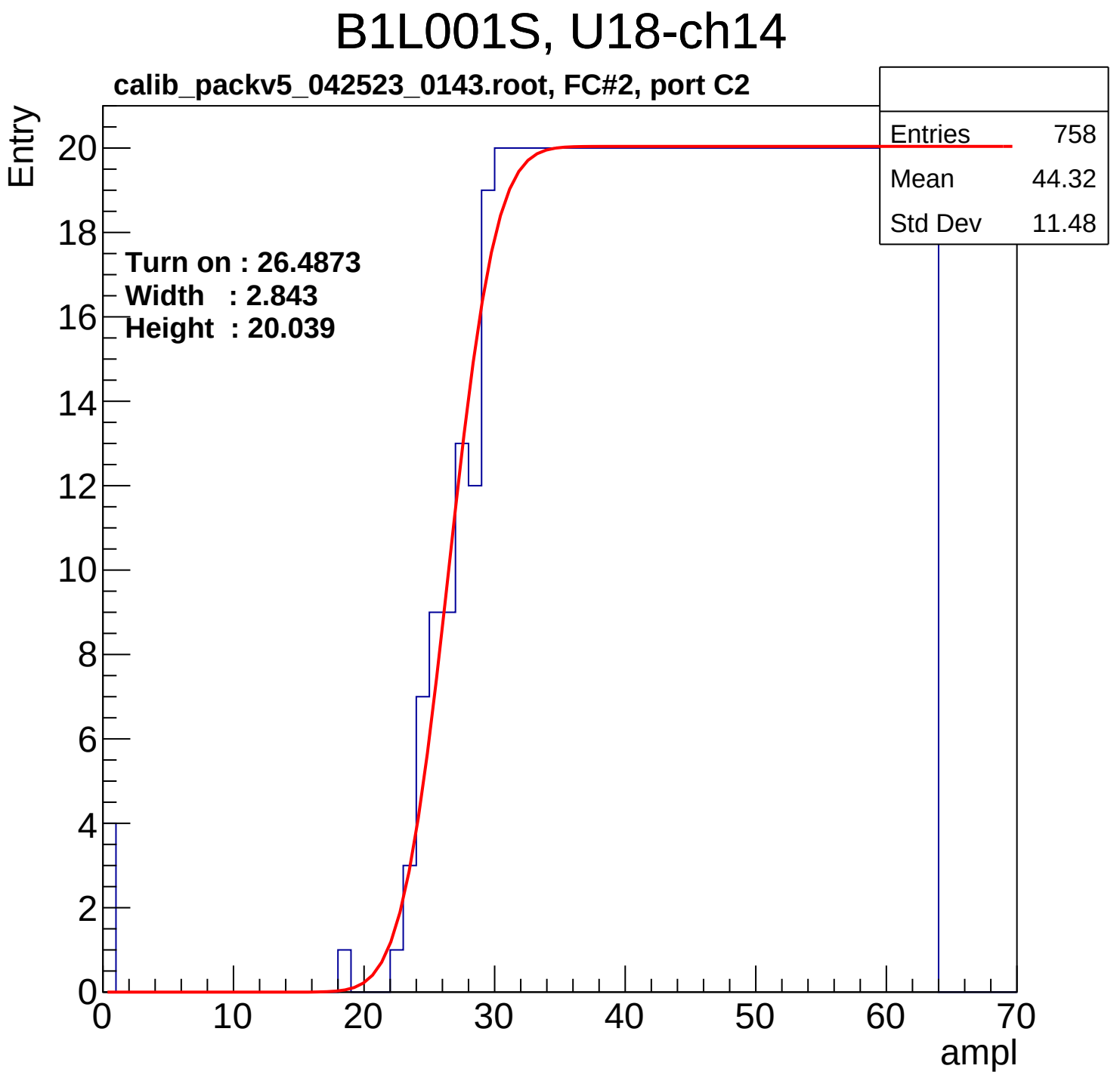
B1L001S, U18-ch14
calib_packv5_042523_0143.root, FC#2, port C2
Entries 758
Mean 44.32
Std Dev 11.48
Turn on : 26.4873
Width : 2.843
Height : 20.039
Entry
ampl
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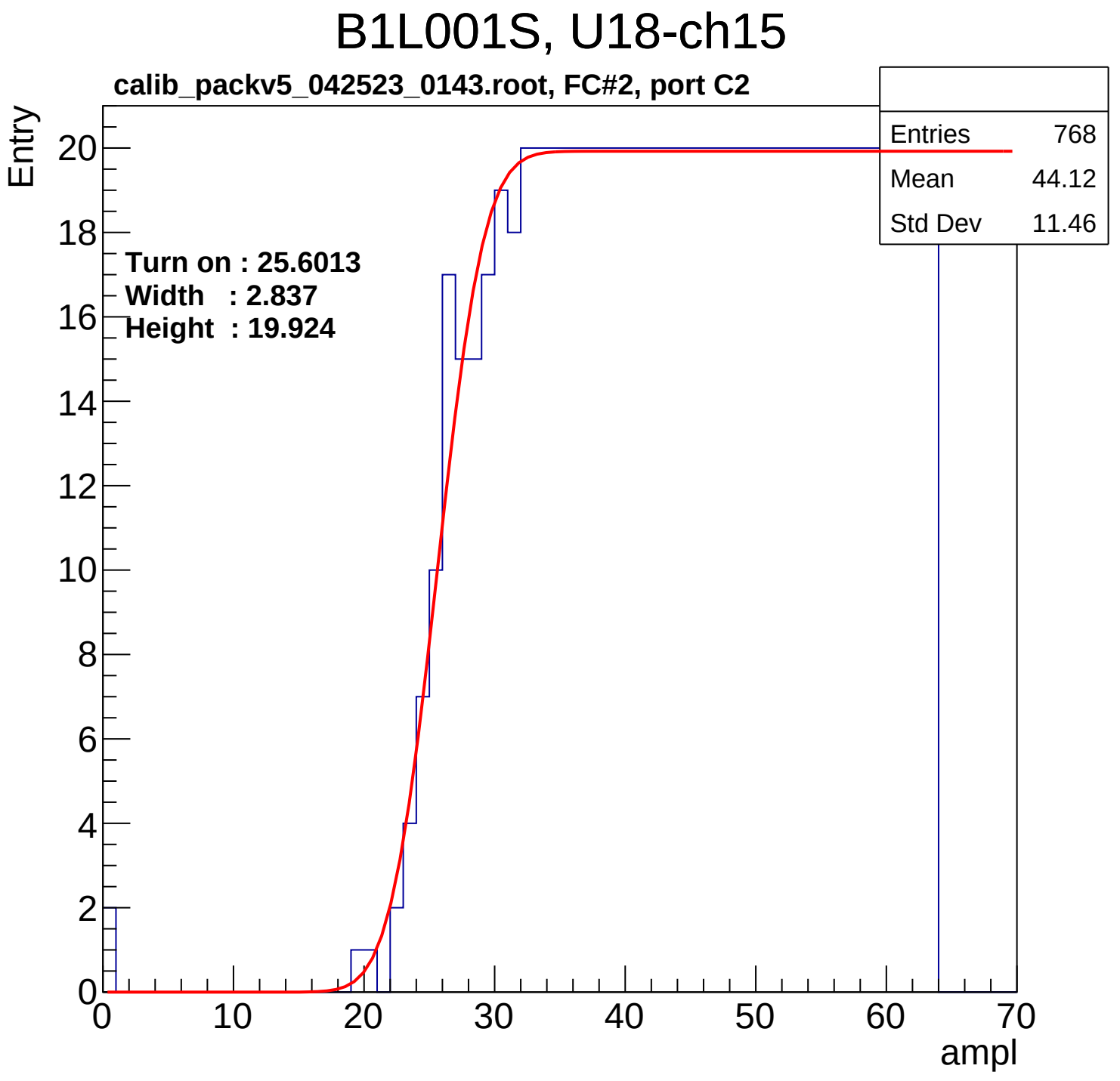
B1L001S, U18-ch15
calib_packv5_042523_0143.root, FC#2, port C2
Entries 768
Mean 44.12
Std Dev 11.46
Turn on : 25.6013
Width : 2.837
Height : 19.924
Entry
ampl
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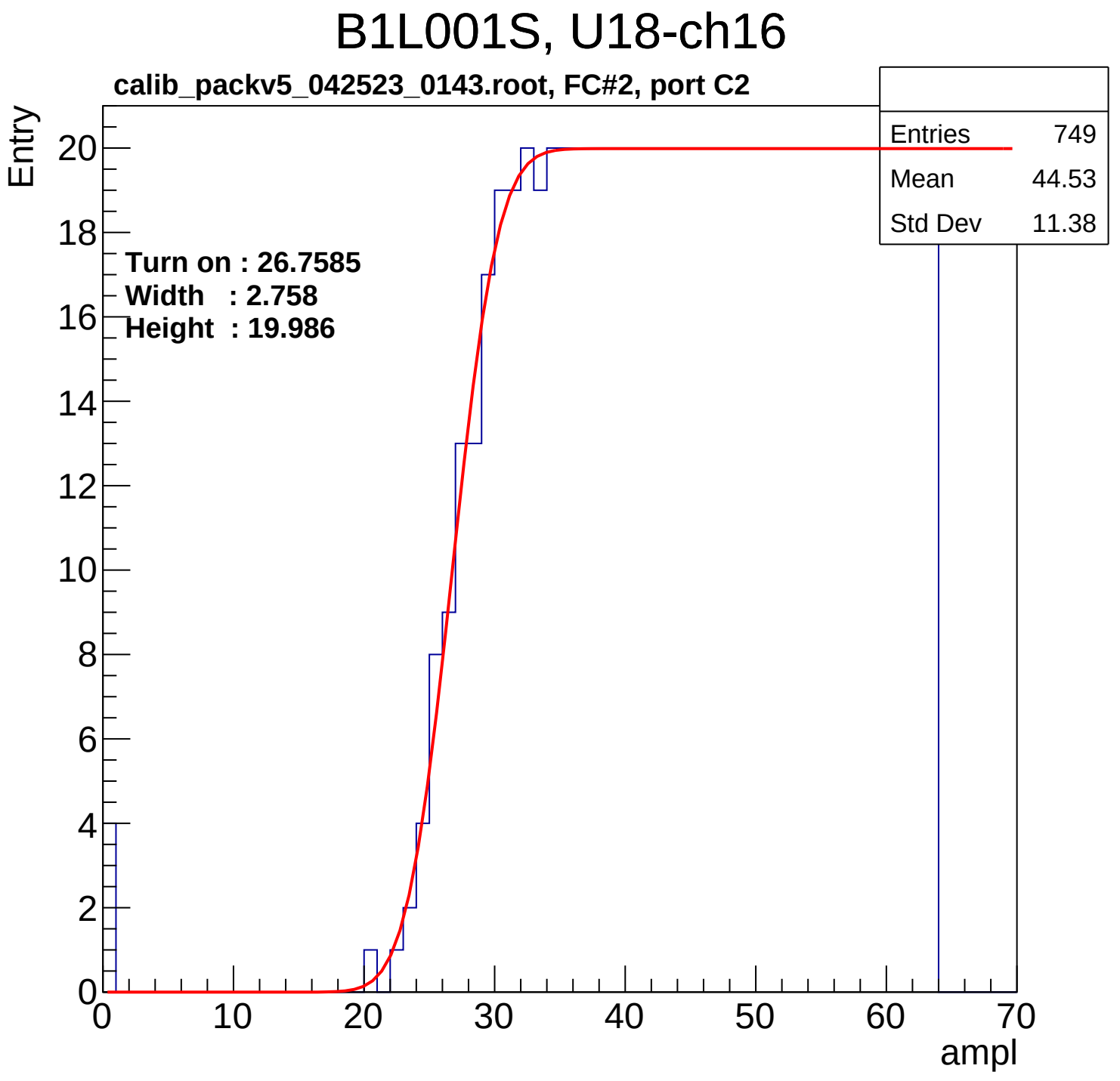
B1L001S, U18-ch16
calib_packv5_042523_0143.root, FC#2, port C2
Entries 749
Mean 44.53
Std Dev 11.38
Turn on : 26.7585
Width : 2.758
Height : 19.986
Entry
ampl
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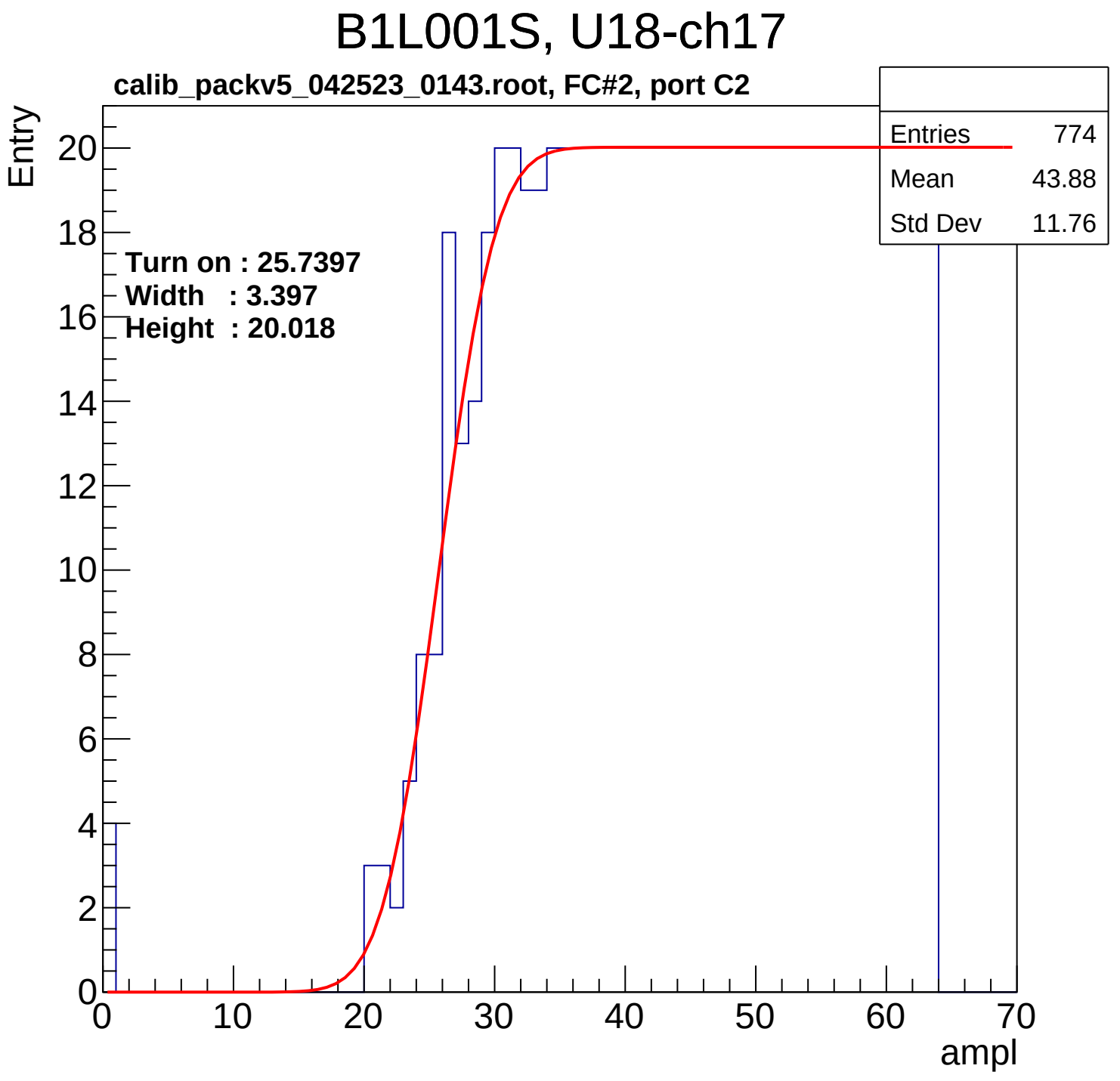
B1L001S, U18-ch17
calib_packv5_042523_0143.root, FC#2, port C2
Entries 774
Mean 43.88
Std Dev 11.76
Turn on : 25.7397
Width : 3.397
Height : 20.018
Entry
ampl
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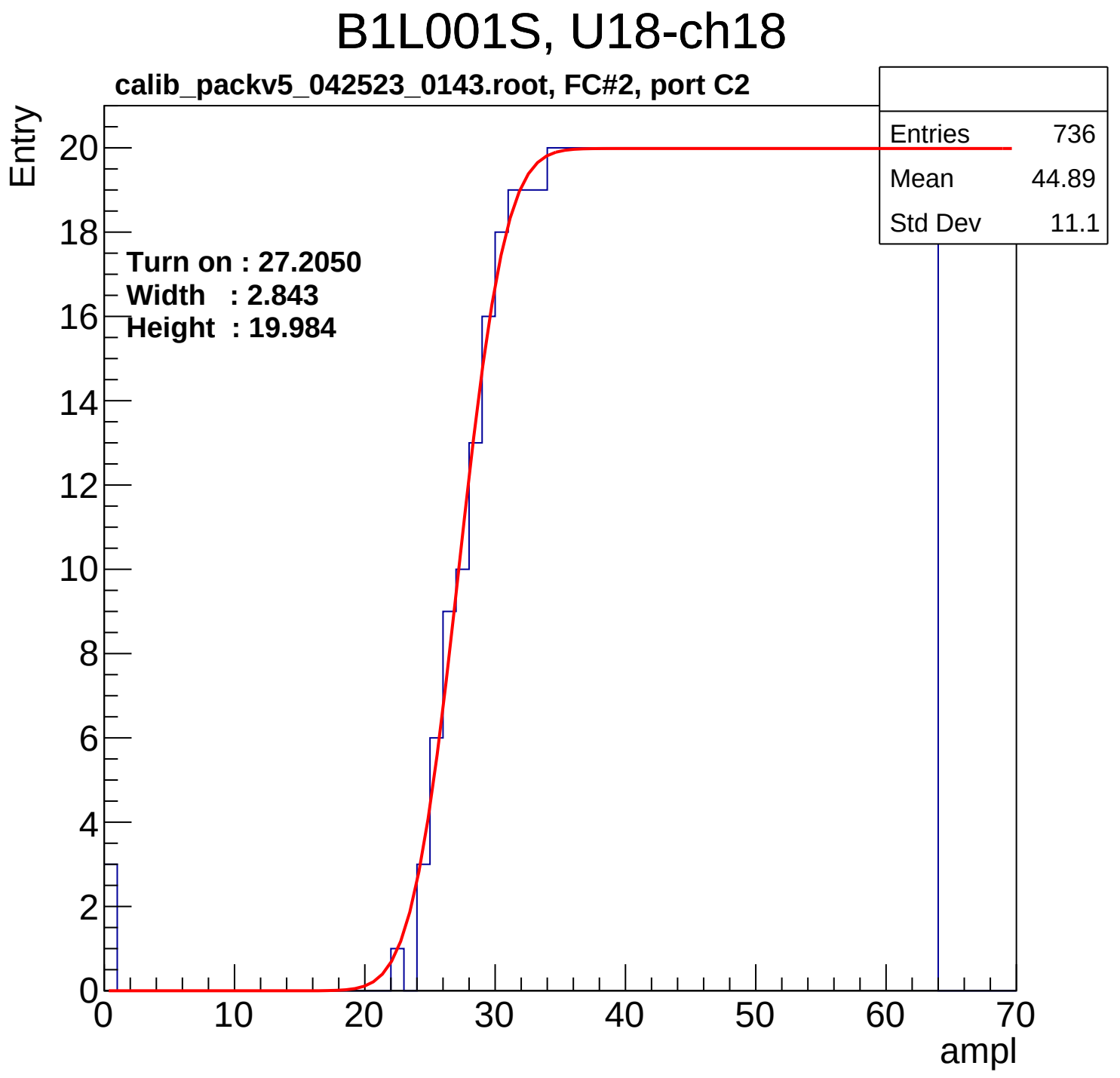
B1L001S, U18-ch18
calib_packv5_042523_0143.root, FC#2, port C2
Entries 736
Mean 44.89
Std Dev 11.1
Turn on : 27.2050
Width : 2.843
Height : 19.984
Entry
ampl
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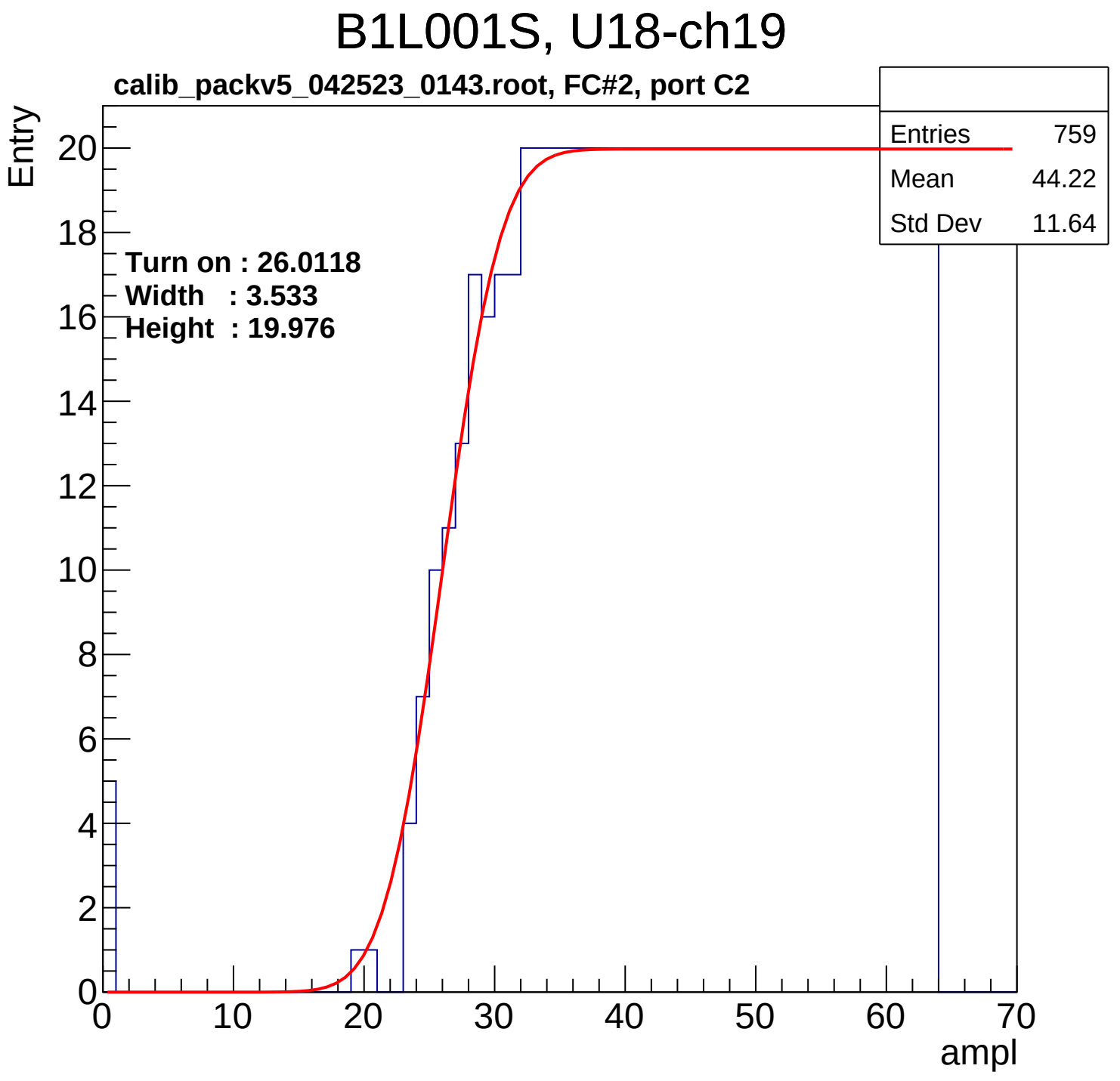
B1L001S, U18-ch19
calib_packv5_042523_0143.root, FC#2, port C2
Entries 759
Mean 44.22
Std Dev 11.64
Turn on : 26.0118
Width : 3.533
Height : 19.976
Entry
ampl
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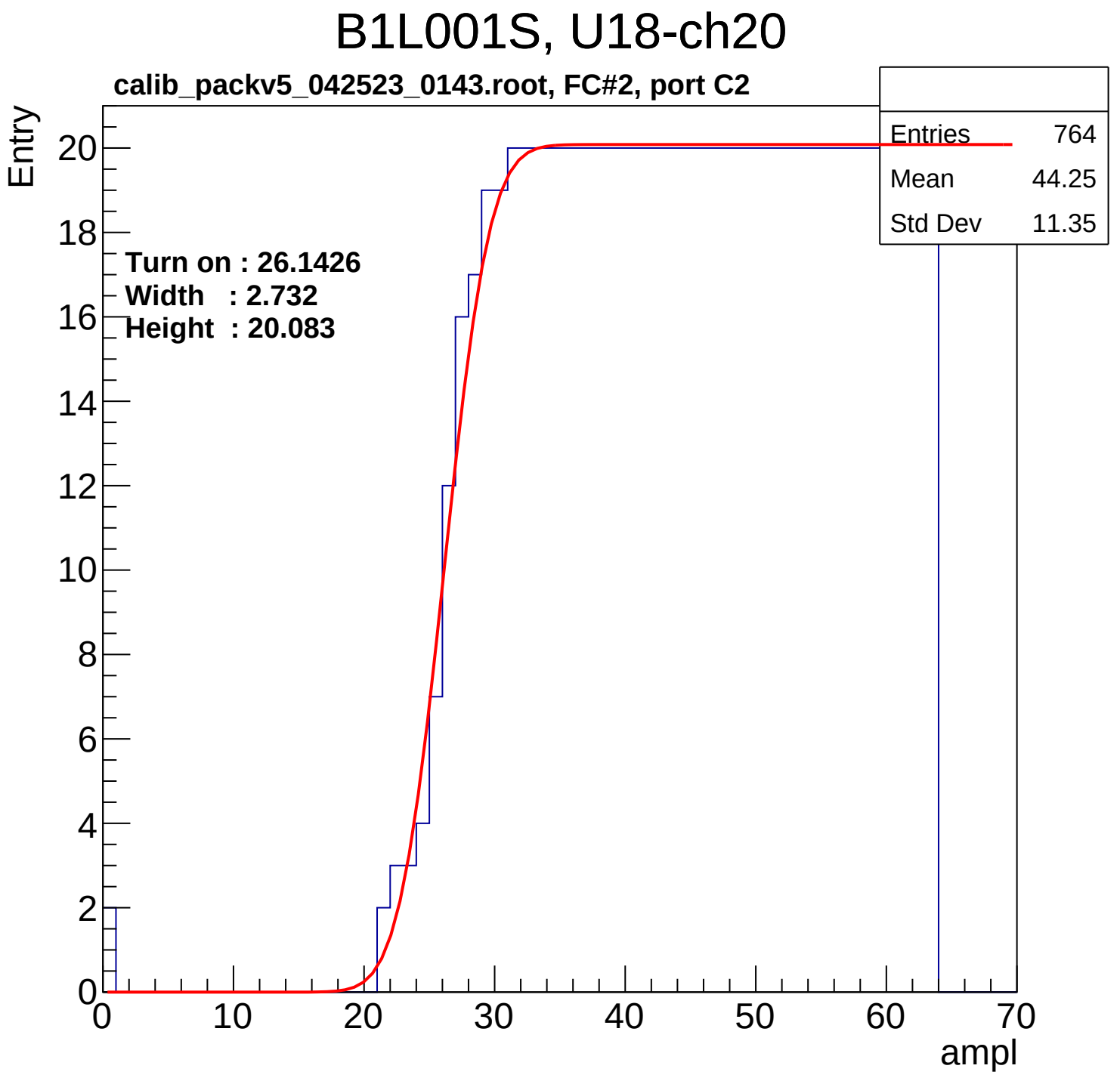
B1L001S, U18-ch20
calib_packv5_042523_0143.root, FC#2, port C2
Entries 764
Mean 44.25
Std Dev 11.35
Turn on : 26.1426
Width : 2.732
Height : 20.083
Entry
ampl
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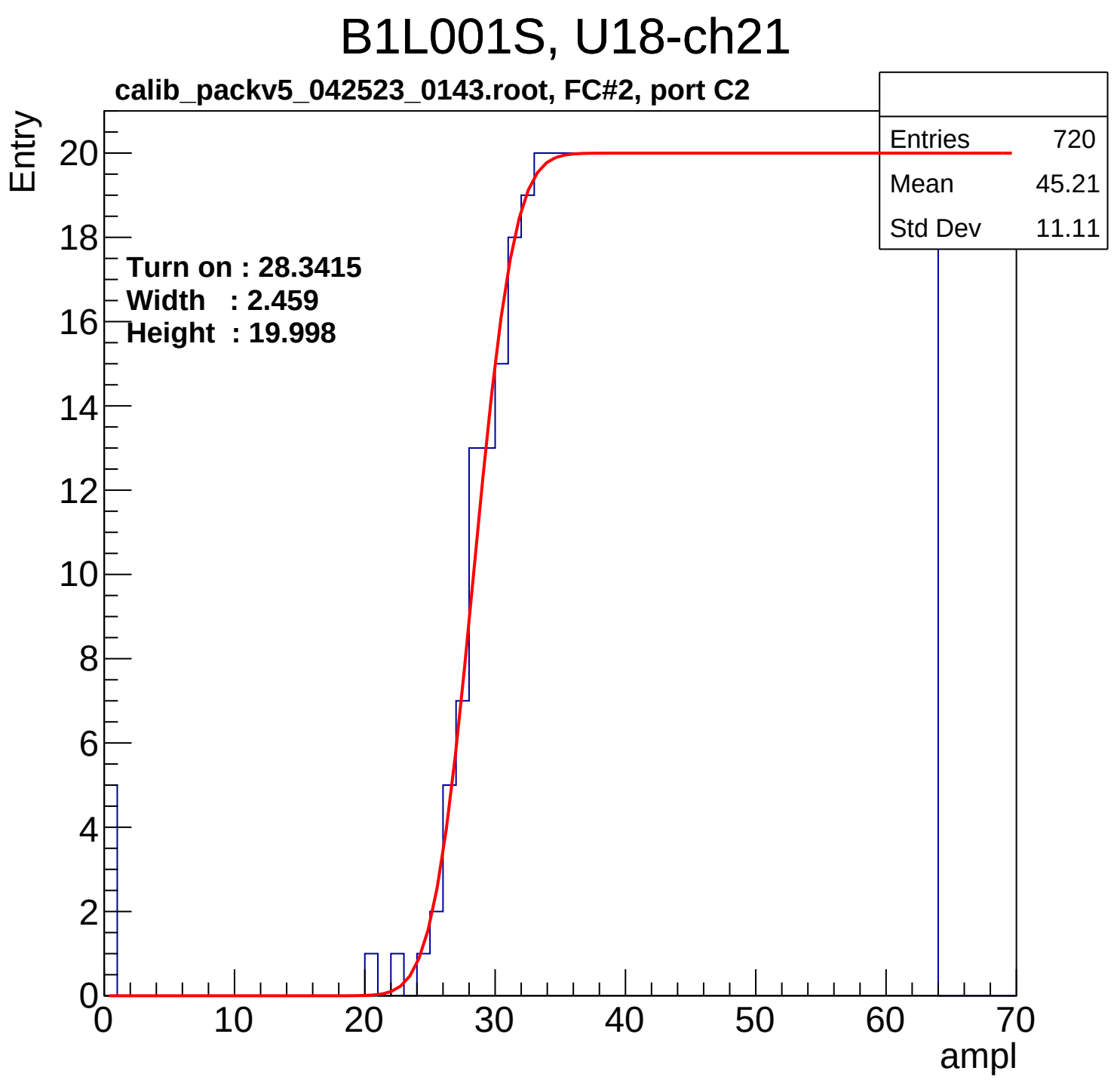
B1L001S, U18-ch21
calib_packv5_042523_0143.root, FC#2, port C2
Entries 720
Mean 45.21
Std Dev 11.11
Turn on : 28.3415
Width : 2.459
Height : 19.998
Entry
ampl
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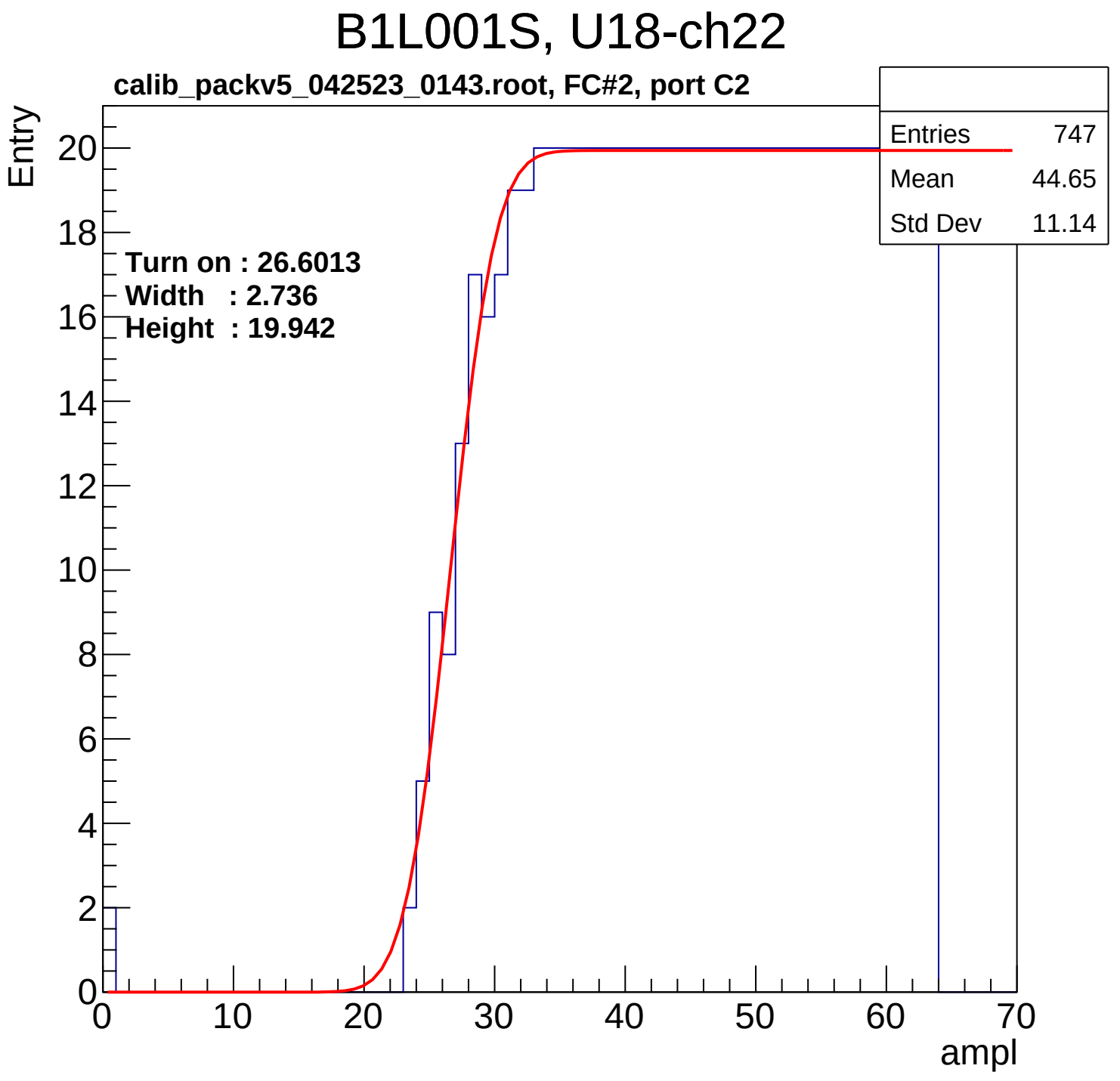
B1L001S, U18-ch22
calib_packv5_042523_0143.root, FC#2, port C2
Entries 747
Mean 44.65
Std Dev 11.14
Turn on : 26.6013
Width : 2.736
Height : 19.942
Entry
ampl
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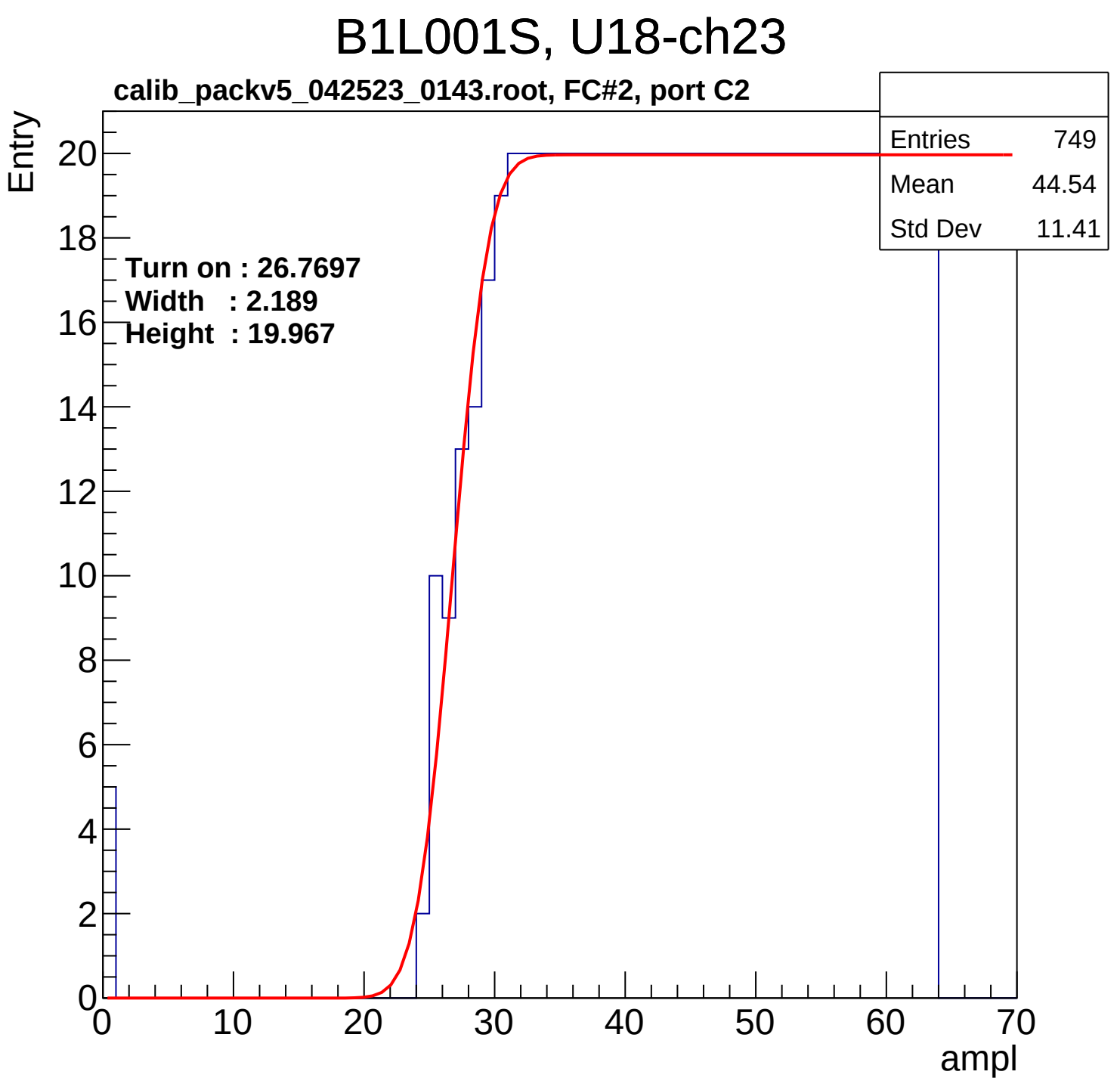
B1L001S, U18-ch23
calib_packv5_042523_0143.root, FC#2, port C2
Entries 749
Mean 44.54
Std Dev 11.41
Turn on : 26.7697
Width : 2.189
Height : 19.967
Entry
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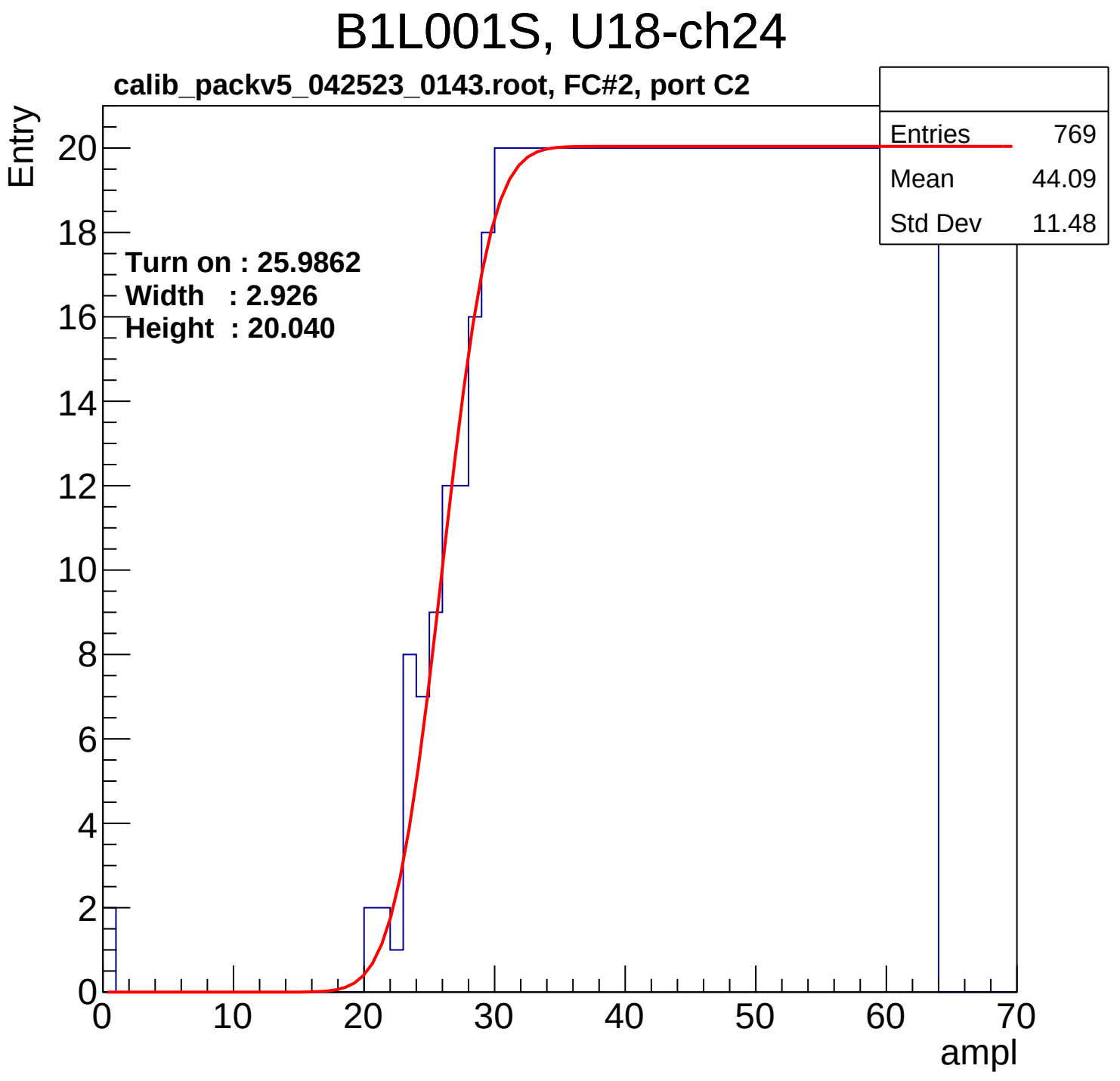
B1L001S, U18-ch24
calib_packv5_042523_0143.root, FC#2, port C2
Entries 769
Mean 44.09
Std Dev 11.48
Turn on : 25.9862
Width : 2.926
Height : 20.040
Entry
ampl
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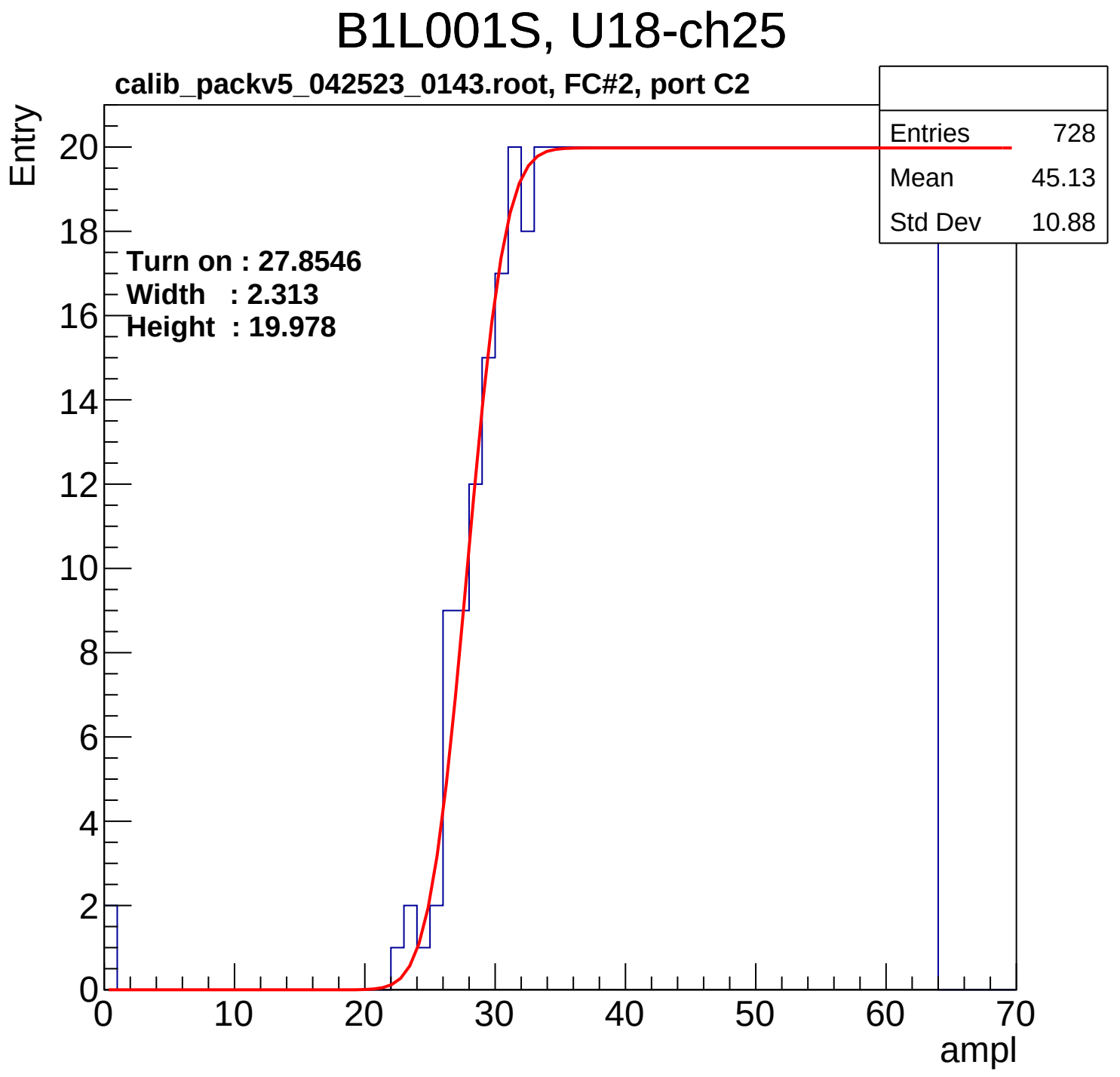
B1L001S, U18-ch25
calib_packv5_042523_0143.root, FC#2, port C2
Entries 728
Mean 45.13
Std Dev 10.88
Turn on : 27.8546
Width : 2.313
Height : 19.978
Entry
ampl
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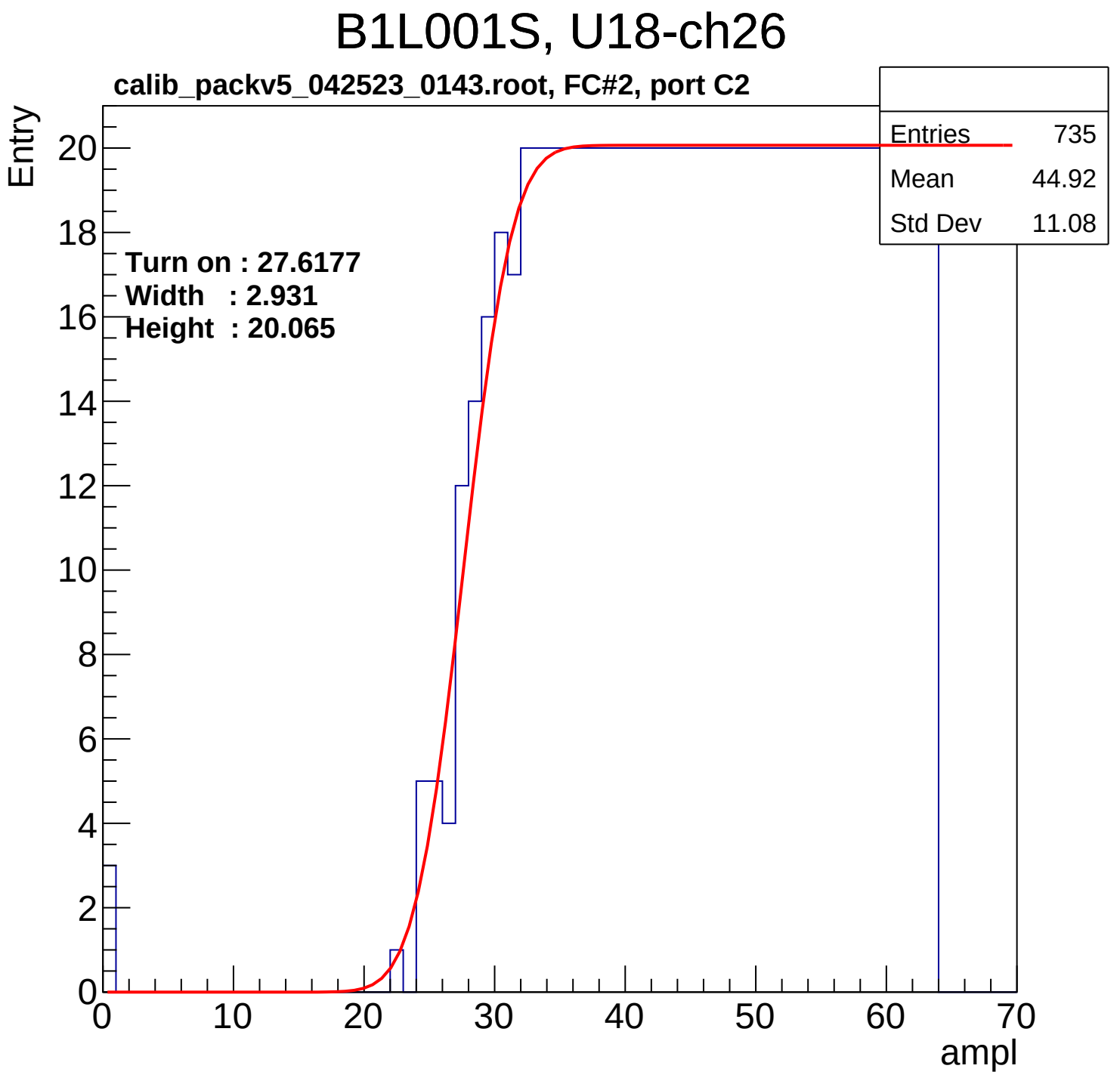
B1L001S, U18-ch26
calib_packv5_042523_0143.root, FC#2, port C2
Entries 735
Mean 44.92
Std Dev 11.08
Turn on : 27.6177
Width : 2.931
Height : 20.065
Entry
ampl
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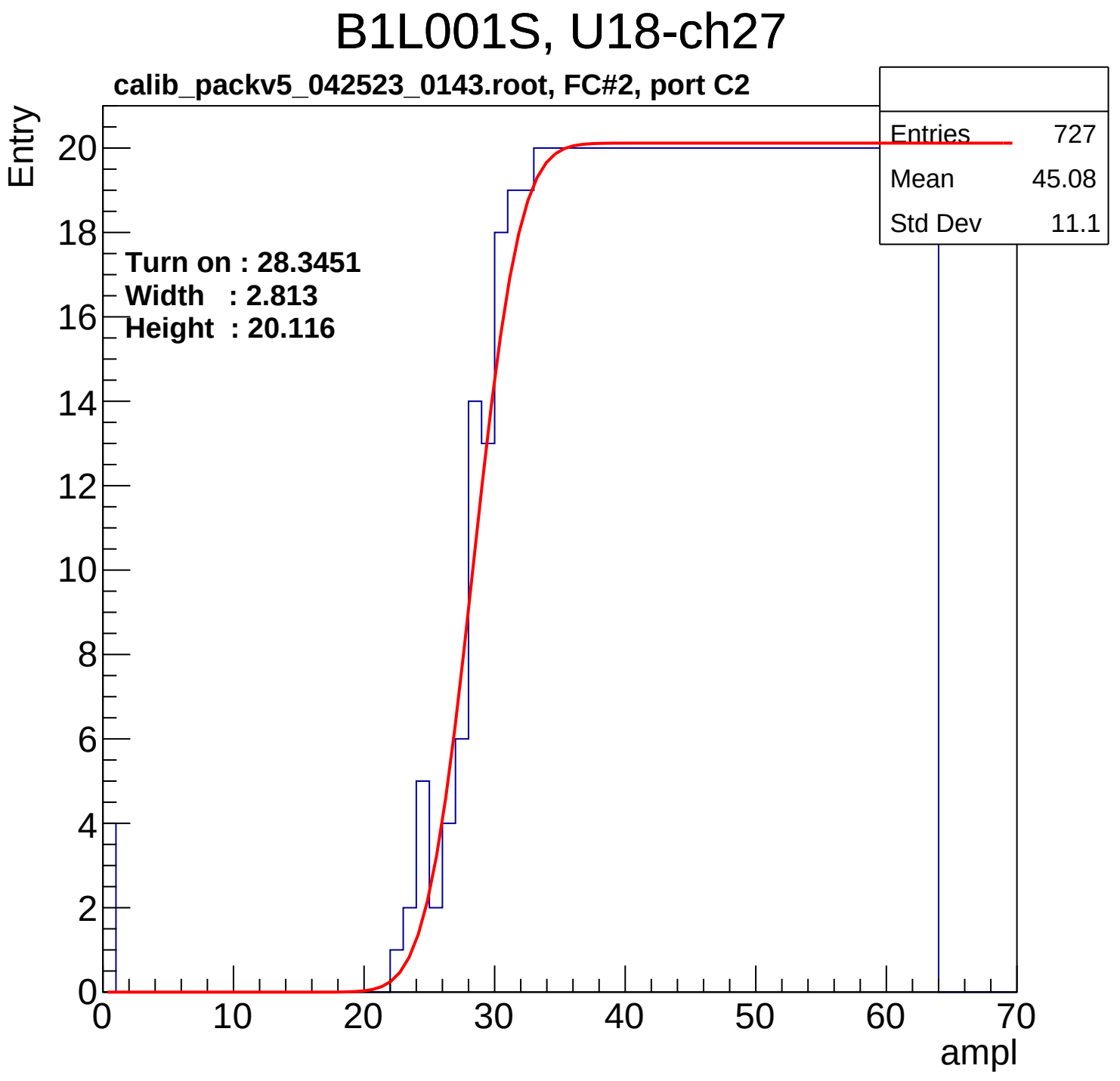
B1L001S, U18-ch27
calib_packv5_042523_0143.root, FC#2, port C2
Entries 727
Mean 45.08
Std Dev 11.1
Turn on : 28.3451
Width : 2.813
Height : 20.116
Entry
ampl
0
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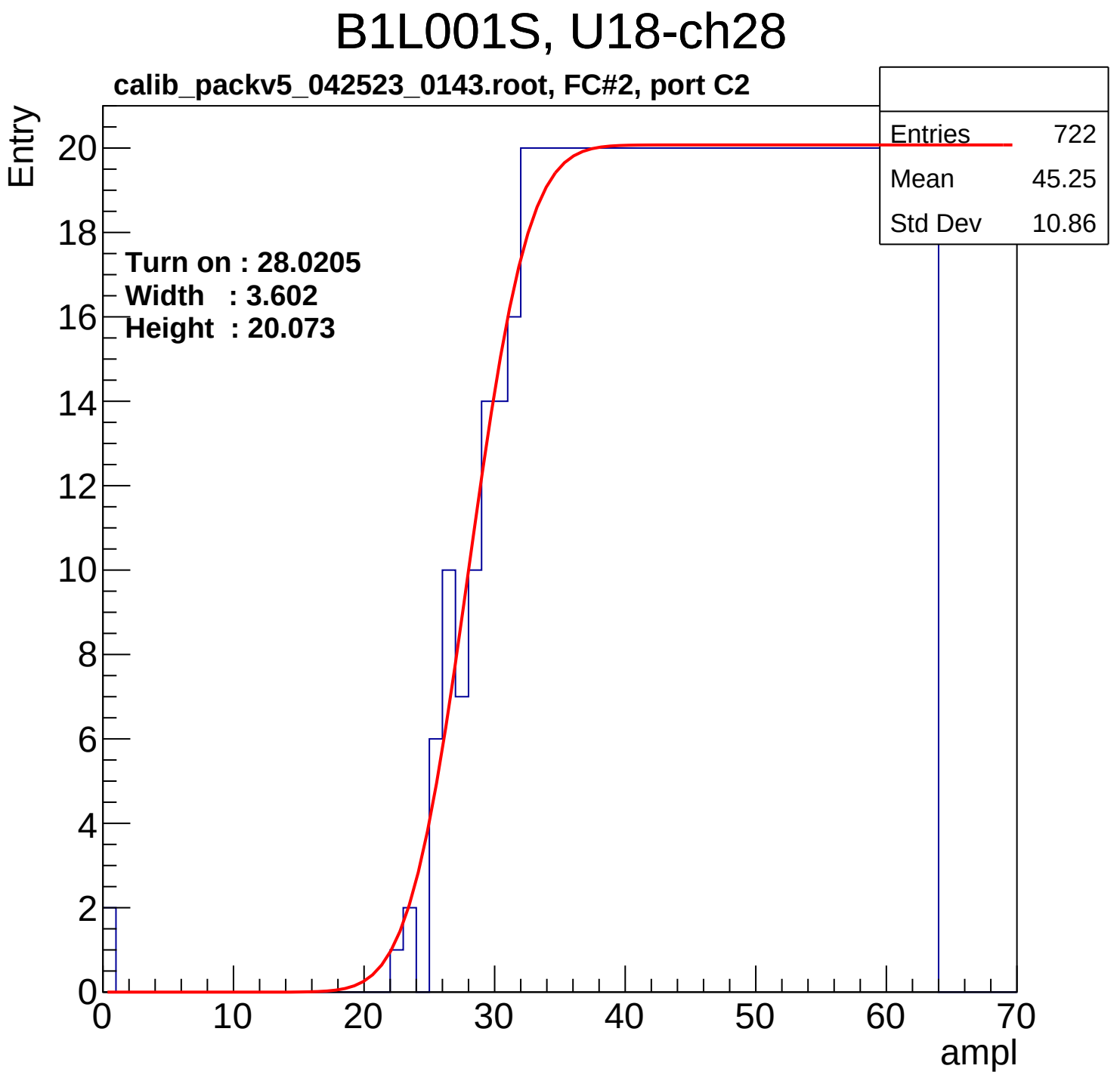
B1L001S, U18-ch28
calib_packv5_042523_0143.root, FC#2, port C2
Entries 722
Mean 45.25
Std Dev 10.86
Turn on : 28.0205
Width : 3.602
Height : 20.073
Entry
ampl
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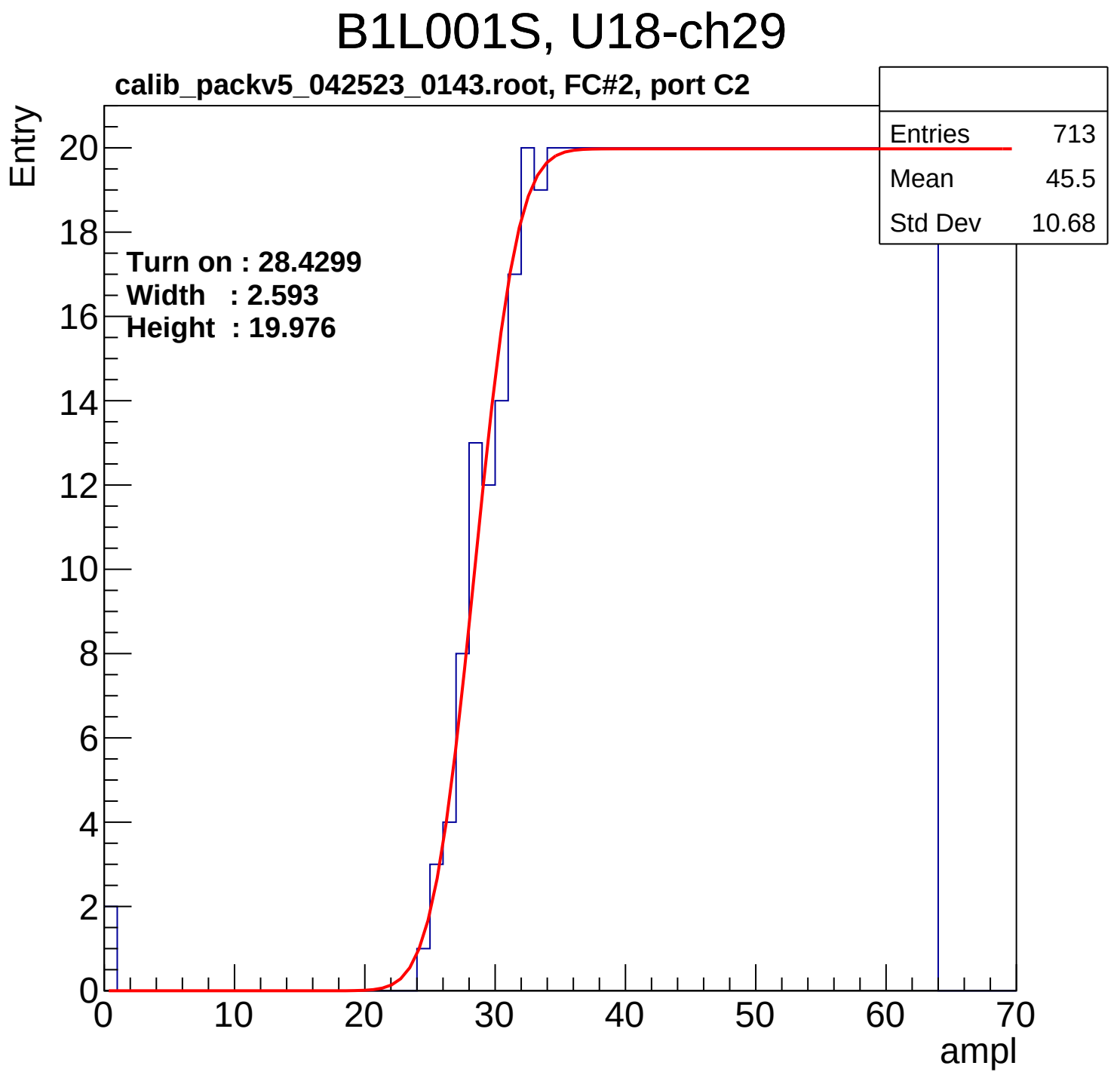
B1L001S, U18-ch29
calib_packv5_042523_0143.root, FC#2, port C2
Entries 713
Mean 45.5
Std Dev 10.68
Turn on : 28.4299
Width : 2.593
Height : 19.976
Entry
ampl
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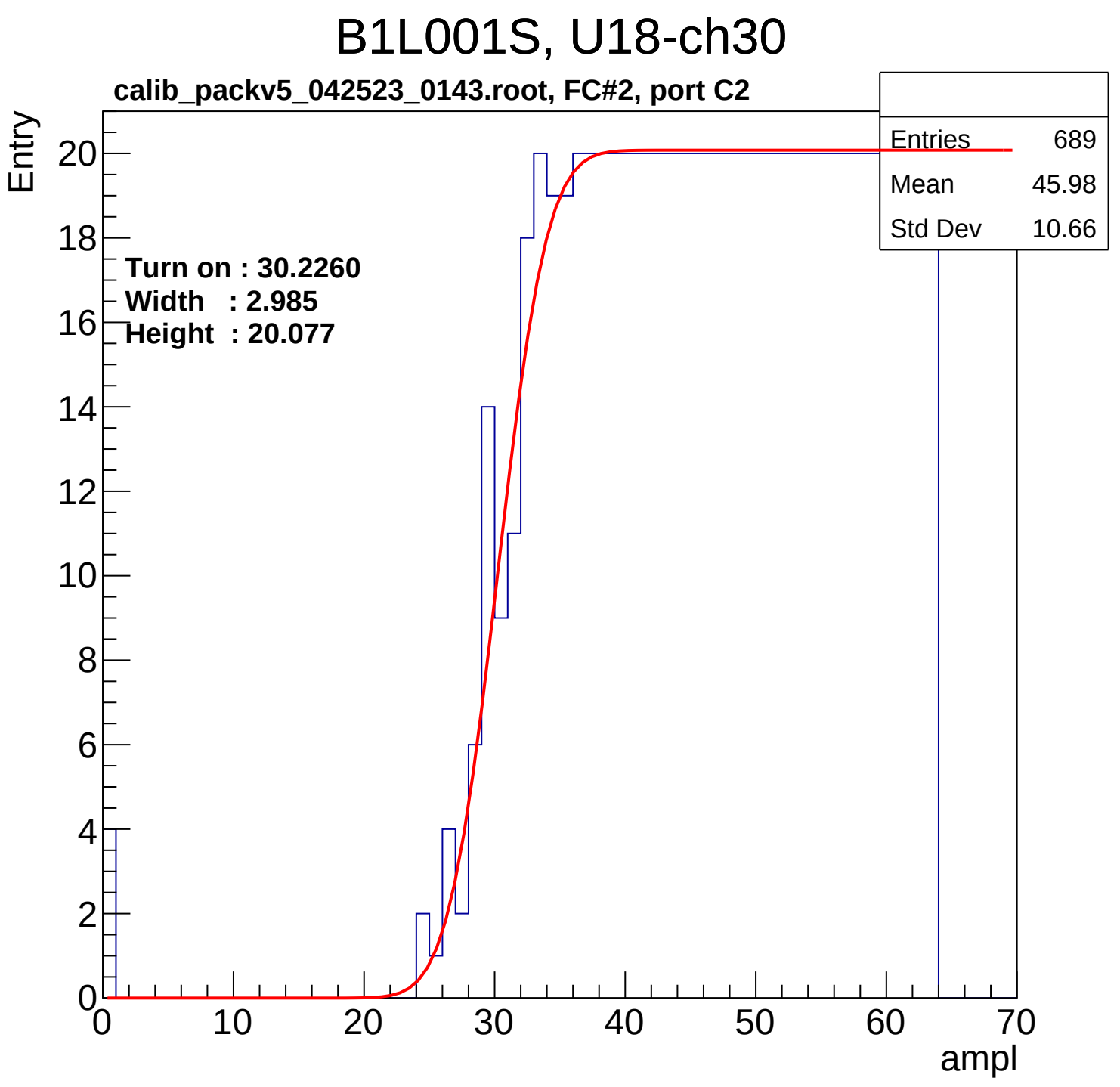
B1L001S, U18-ch30
calib_packv5_042523_0143.root, FC#2, port C2
Entries 689
Mean 45.98
Std Dev 10.66
Turn on : 30.2260
Width : 2.985
Height : 20.077
Entry
ampl
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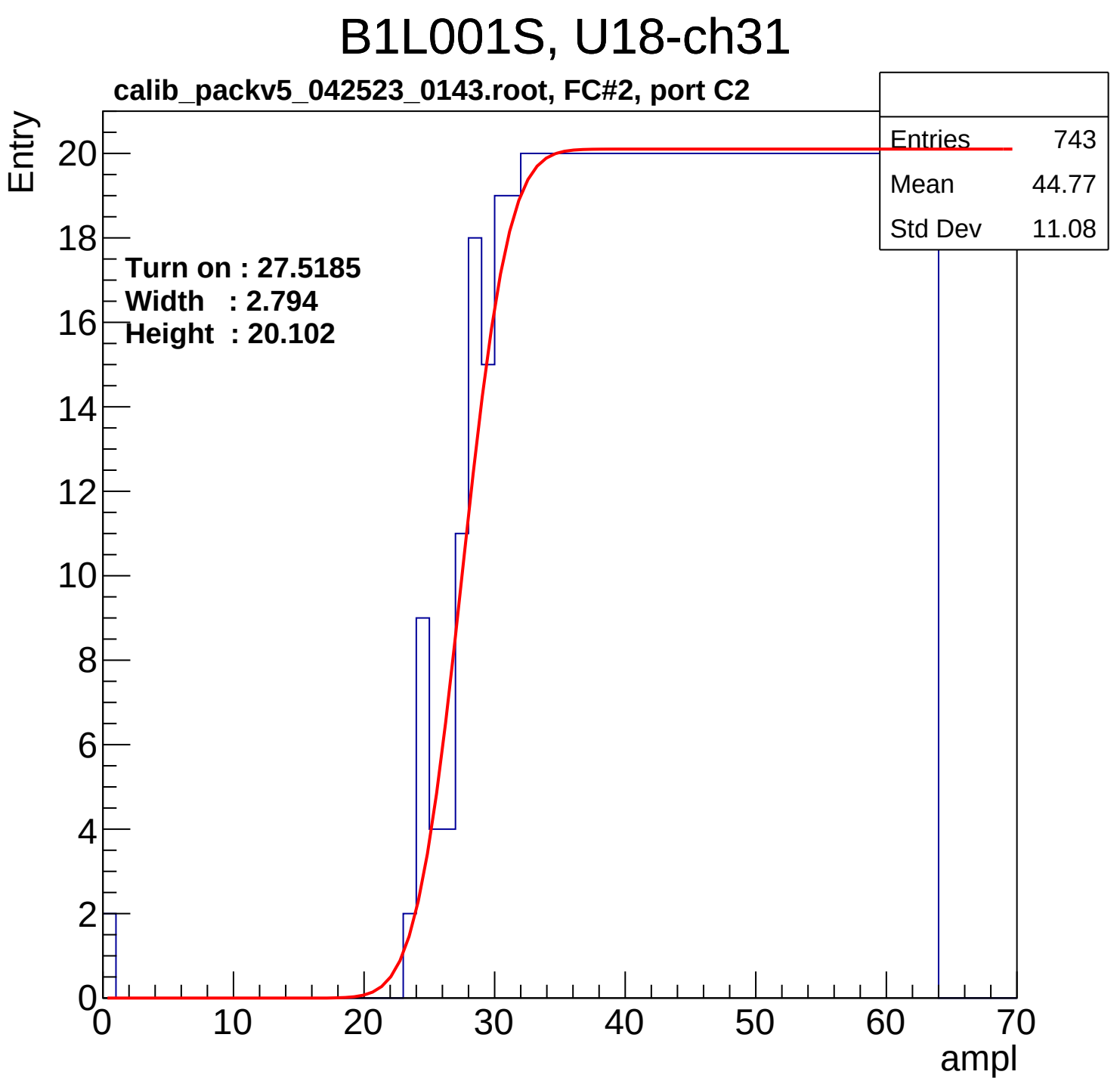
B1L001S, U18-ch31
calib_packv5_042523_0143.root, FC#2, port C2
Entries 743
Mean 44.77
Std Dev 11.08
Turn on : 27.5185
Width : 2.794
Height : 20.102
Entry
ampl
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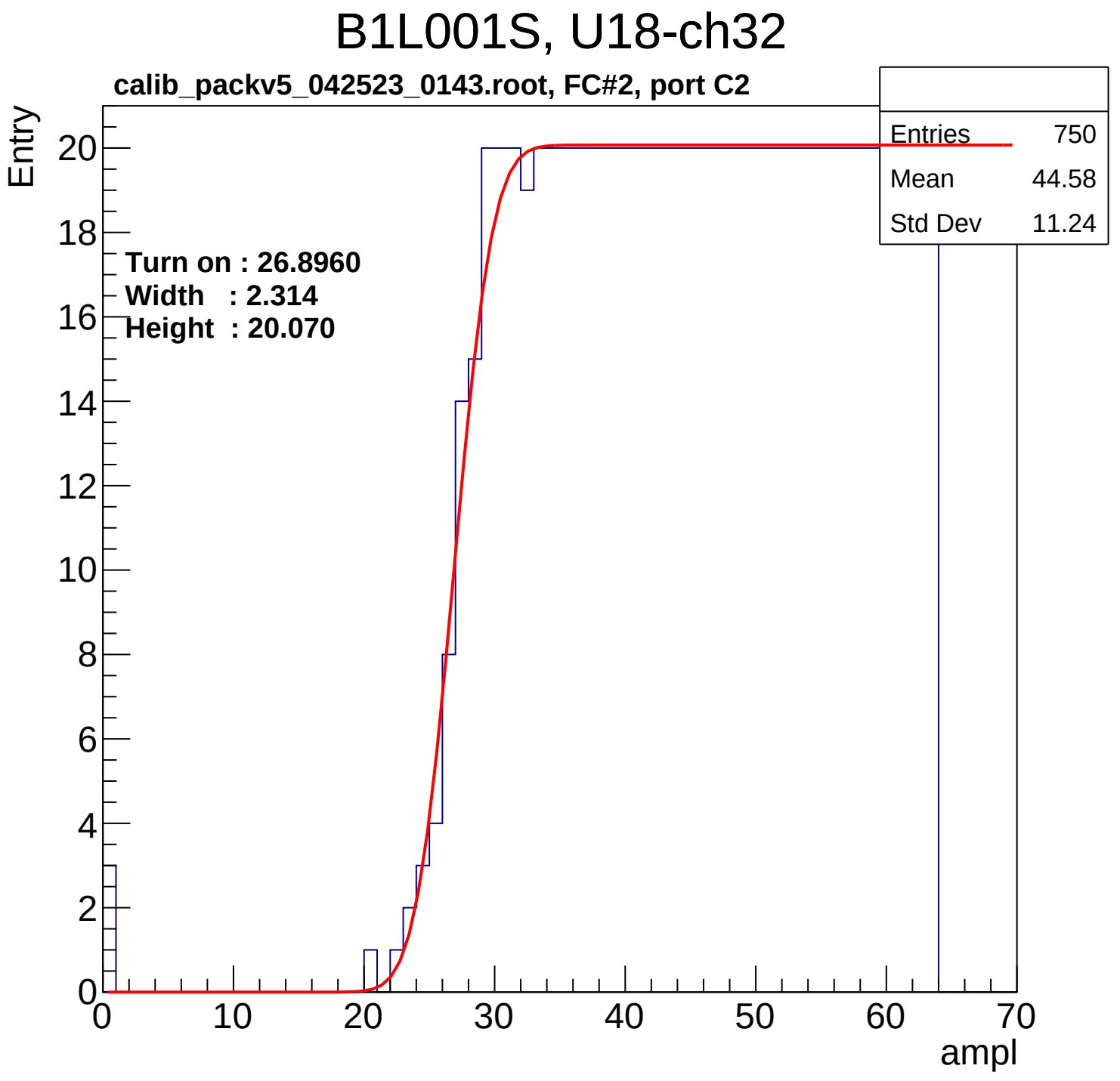
B1L001S, U18-ch32
calib_packv5_042523_0143.root, FC#2, port C2
Entries 750
Mean 44.58
Std Dev 11.24
Turn on : 26.8960
Width : 2.314
Height : 20.070
Entry
ampl
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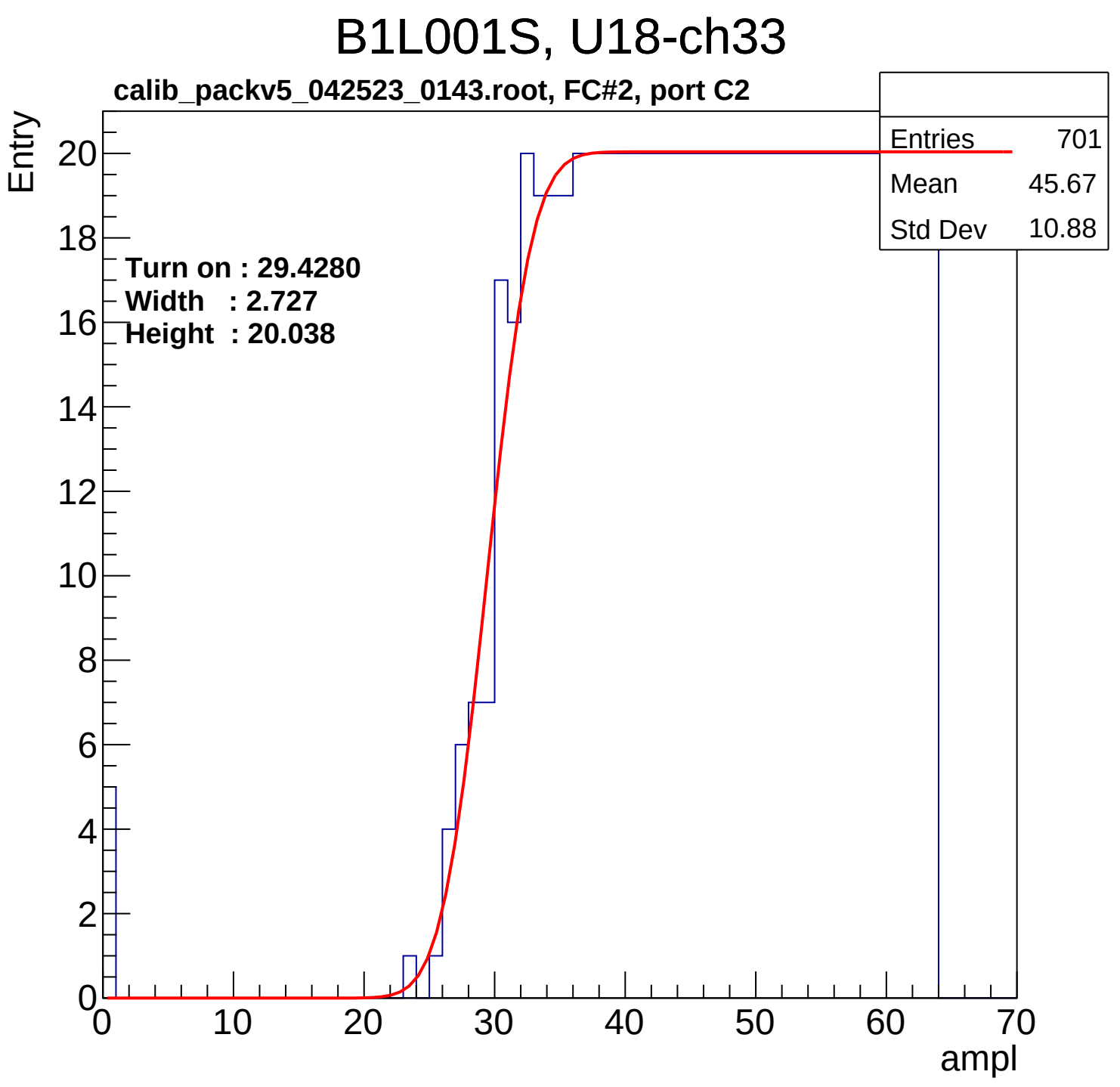
B1L001S, U18-ch33
calib_packv5_042523_0143.root, FC#2, port C2
Entries 701
Mean 45.67
Std Dev 10.88
Turn on : 29.4280
Width : 2.727
Height : 20.038
Entry
ampl
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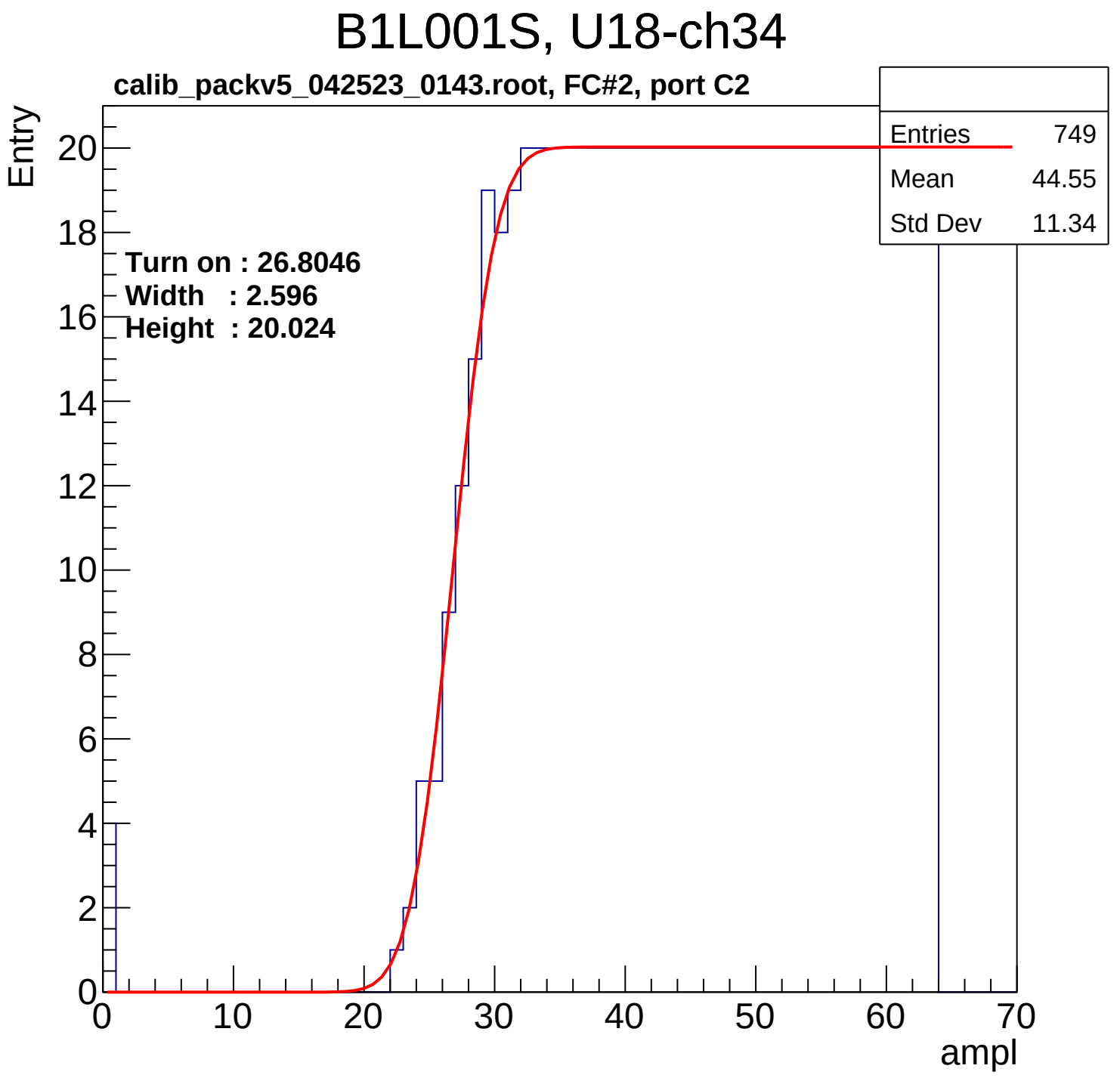
B1L001S, U18-ch34
calib_packv5_042523_0143.root, FC#2, port C2
Entries 749
Mean 44.55
Std Dev 11.34
Turn on : 26.8046
Width : 2.596
Height : 20.024
Entry
ampl
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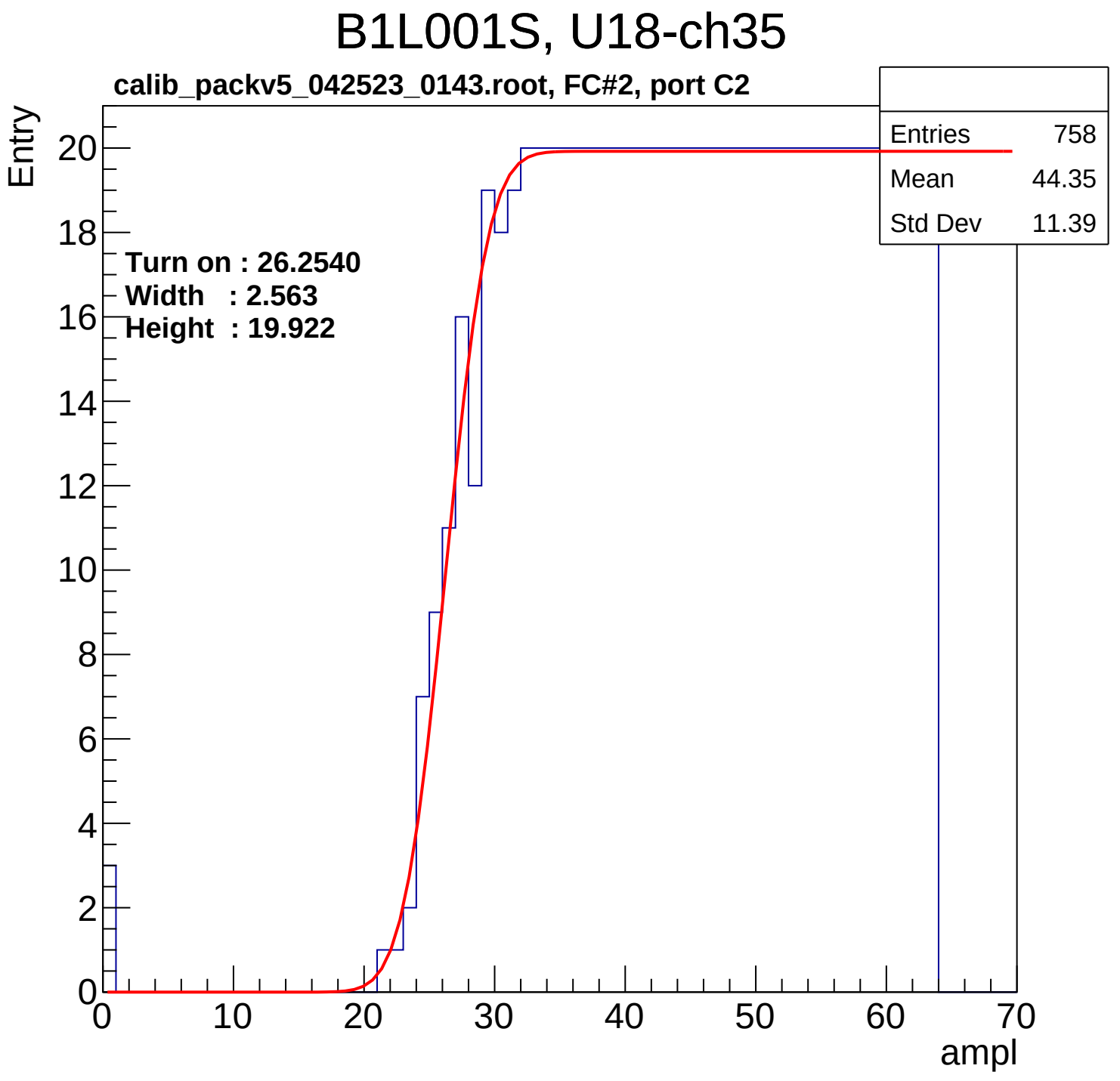
B1L001S, U18-ch35
calib_packv5_042523_0143.root, FC#2, port C2
Entries 758
Mean 44.35
Std Dev 11.39
Turn on : 26.2540
Width : 2.563
Height : 19.922
Entry
ampl
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6
8
10
12
14
16
18
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0
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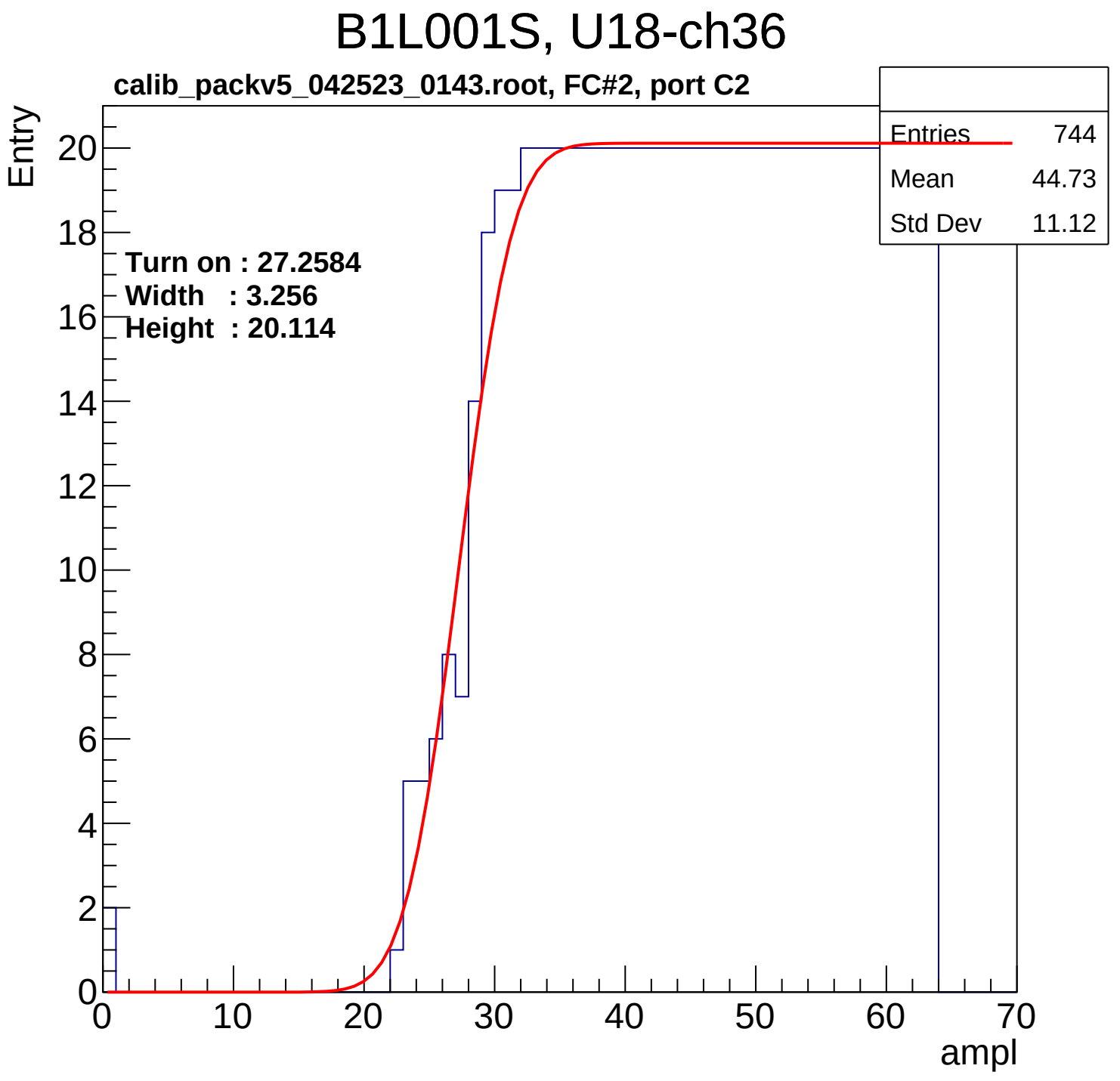
B1L001S, U18-ch36
calib_packv5_042523_0143.root, FC#2, port C2
Entries 744
Mean 44.73
Std Dev 11.12
Turn on : 27.2584
Width : 3.256
Height : 20.114
Entry
ampl
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6
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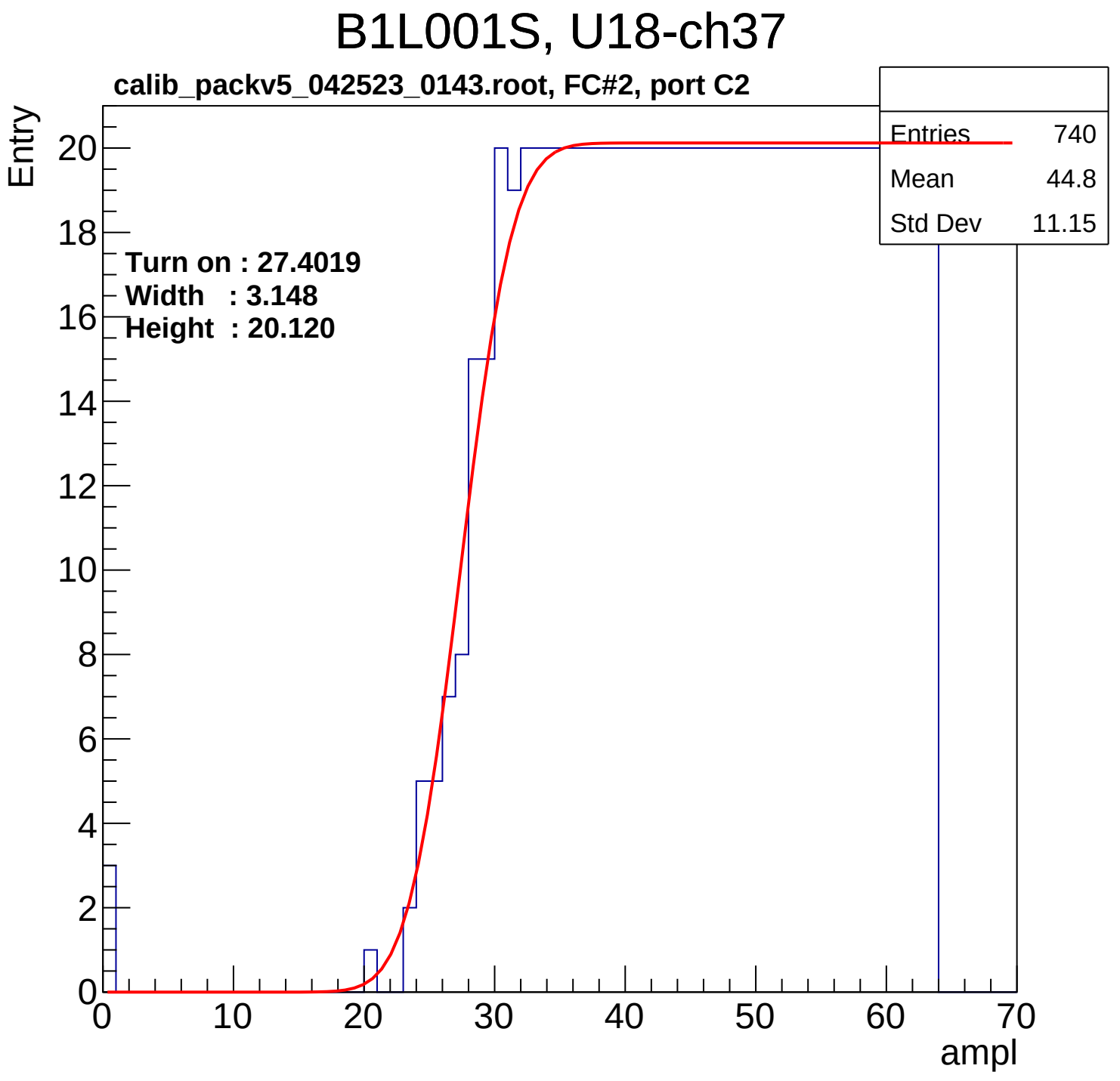
B1L001S, U18-ch37
calib_packv5_042523_0143.root, FC#2, port C2
Entries 740
Mean 44.8
Std Dev 11.15
Turn on : 27.4019
Width : 3.148
Height : 20.120
Entry
ampl
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6
8
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12
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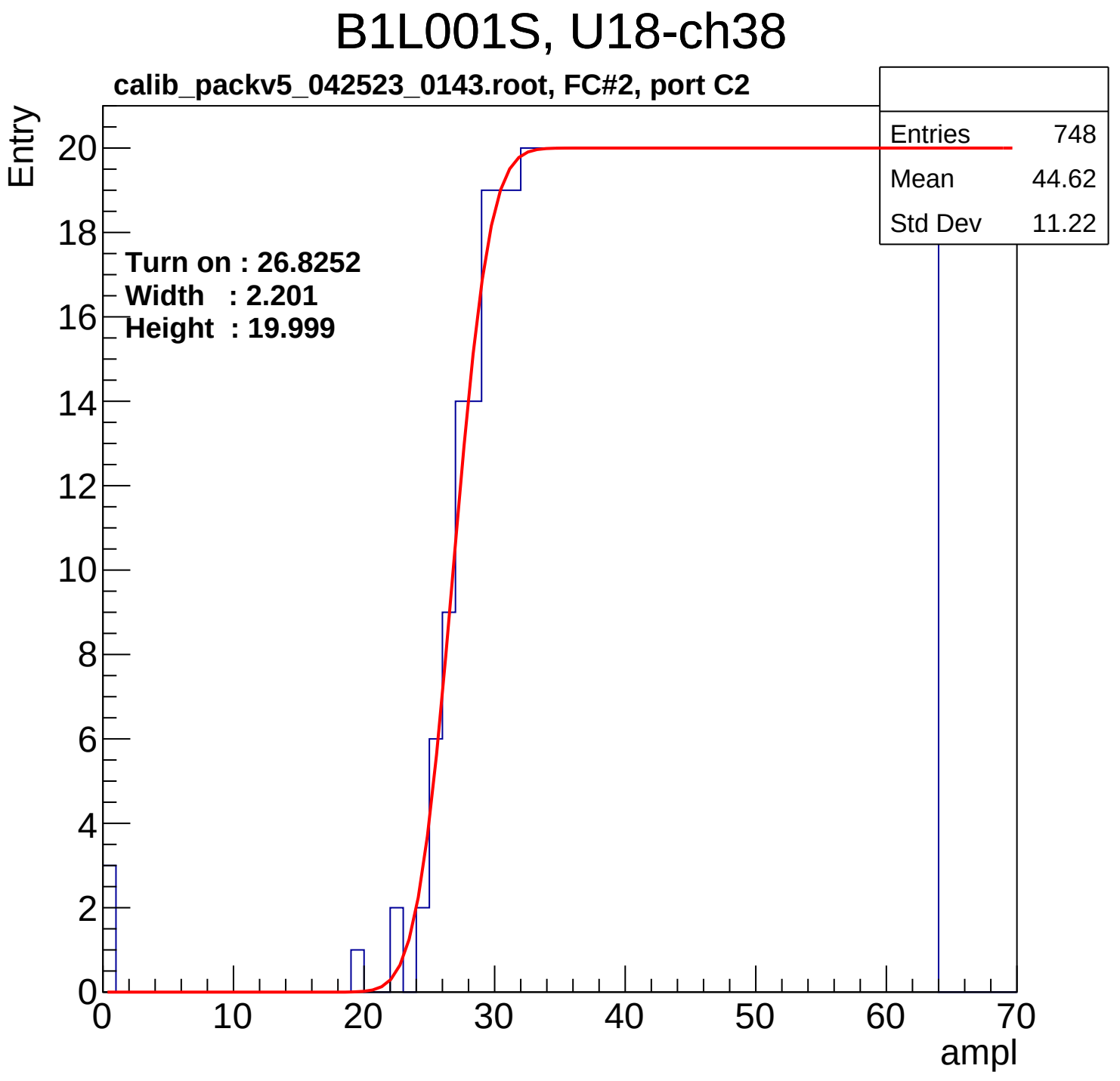
B1L001S, U18-ch38
calib_packv5_042523_0143.root, FC#2, port C2
Entries 748
Mean 44.62
Std Dev 11.22
Turn on : 26.8252
Width : 2.201
Height : 19.999
Entry
ampl
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6
8
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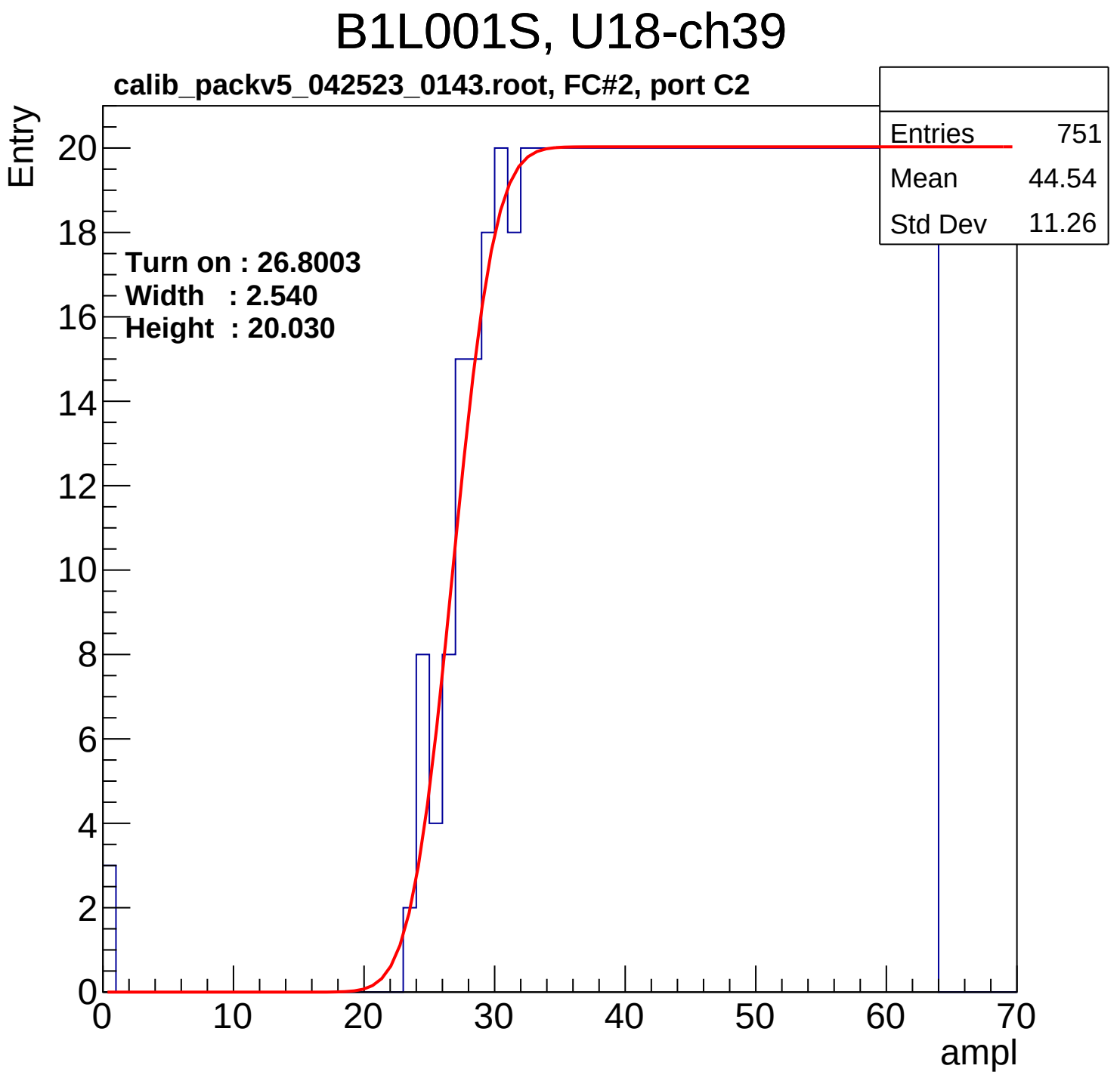
B1L001S, U18-ch39
calib_packv5_042523_0143.root, FC#2, port C2
Entries 751
Mean 44.54
Std Dev 11.26
Turn on : 26.8003
Width : 2.540
Height : 20.030
Entry
ampl
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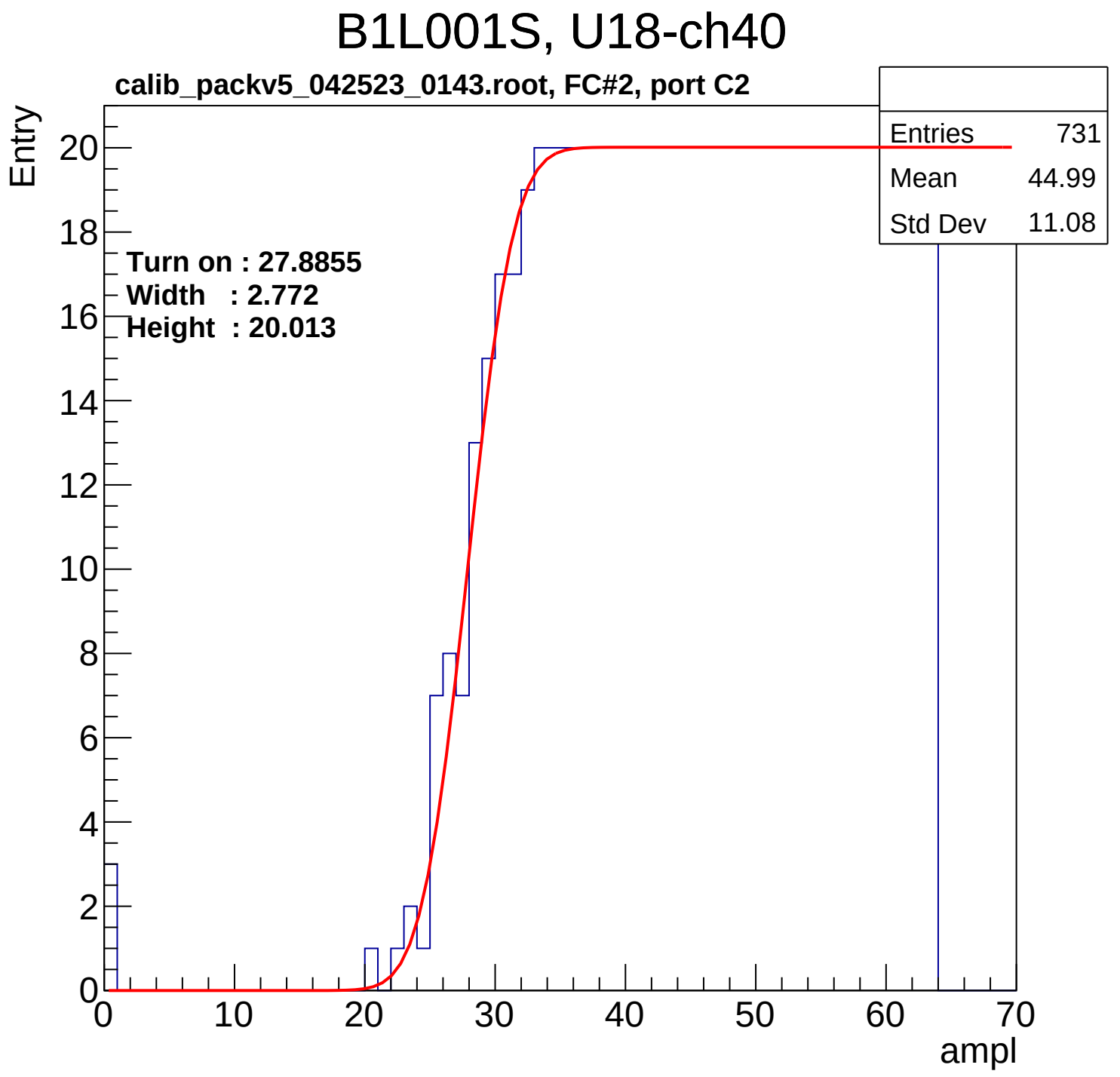
B1L001S, U18-ch40
calib_packv5_042523_0143.root, FC#2, port C2
Entries 731
Mean 44.99
Std Dev 11.08
Turn on : 27.8855
Width : 2.772
Height : 20.013
Entry
ampl
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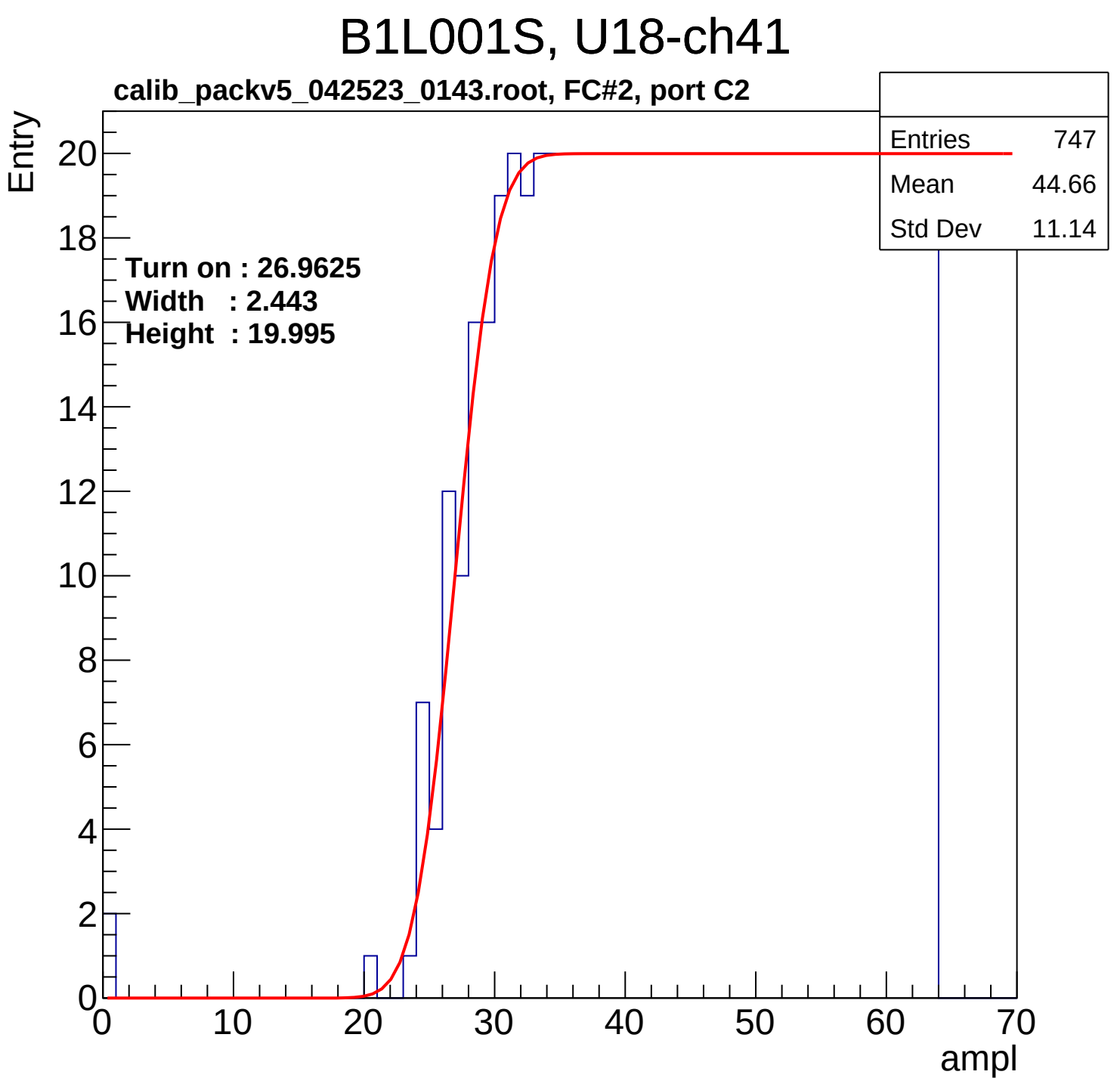
B1L001S, U18-ch41
calib_packv5_042523_0143.root, FC#2, port C2
Entries 747
Mean 44.66
Std Dev 11.14
Turn on : 26.9625
Width : 2.443
Height : 19.995
Entry
ampl
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6
8
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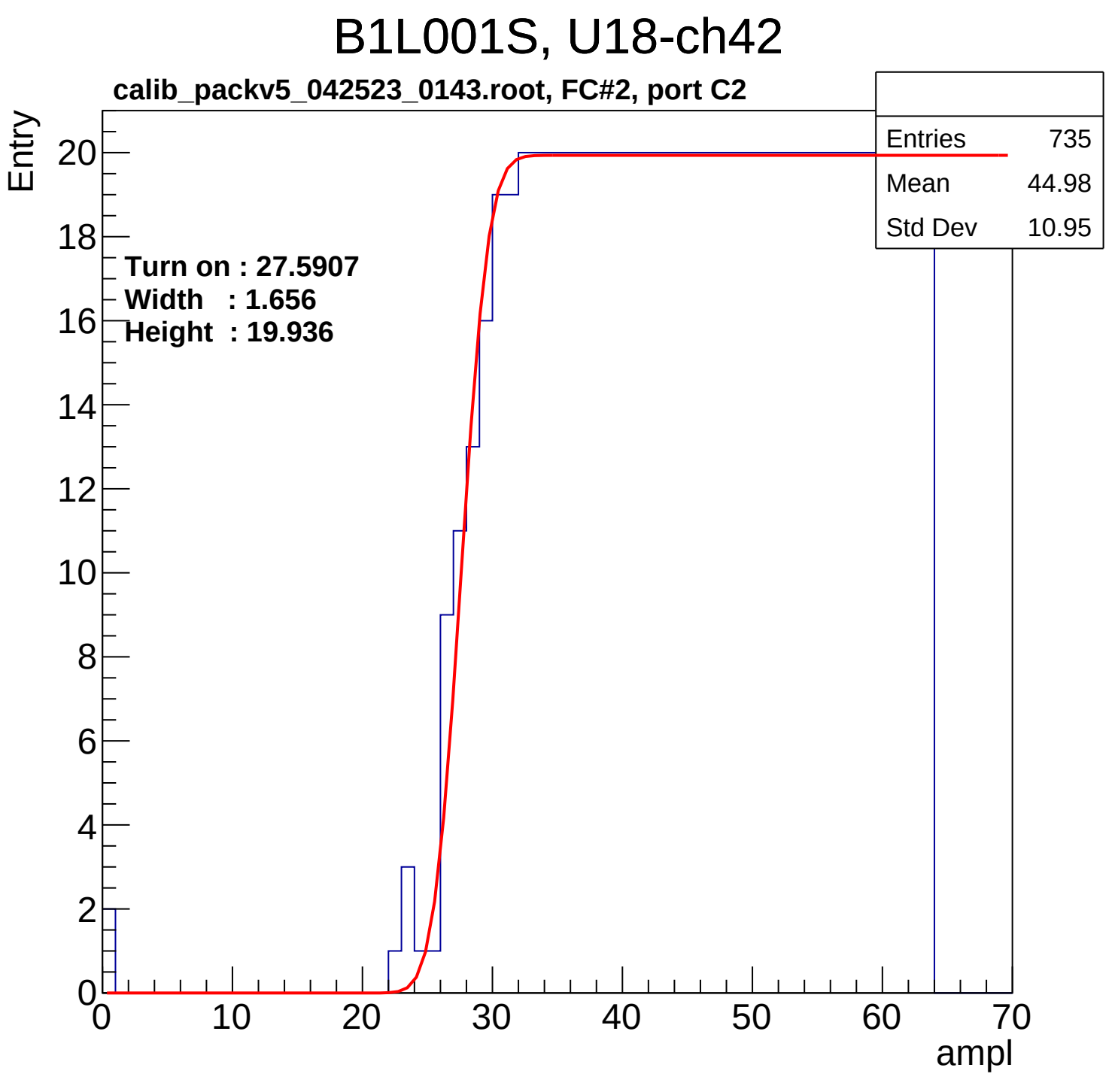
B1L001S, U18-ch42
calib_packv5_042523_0143.root, FC#2, port C2
Entries 735
Mean 44.98
Std Dev 10.95
Turn on : 27.5907
Width : 1.656
Height : 19.936
Entry
ampl
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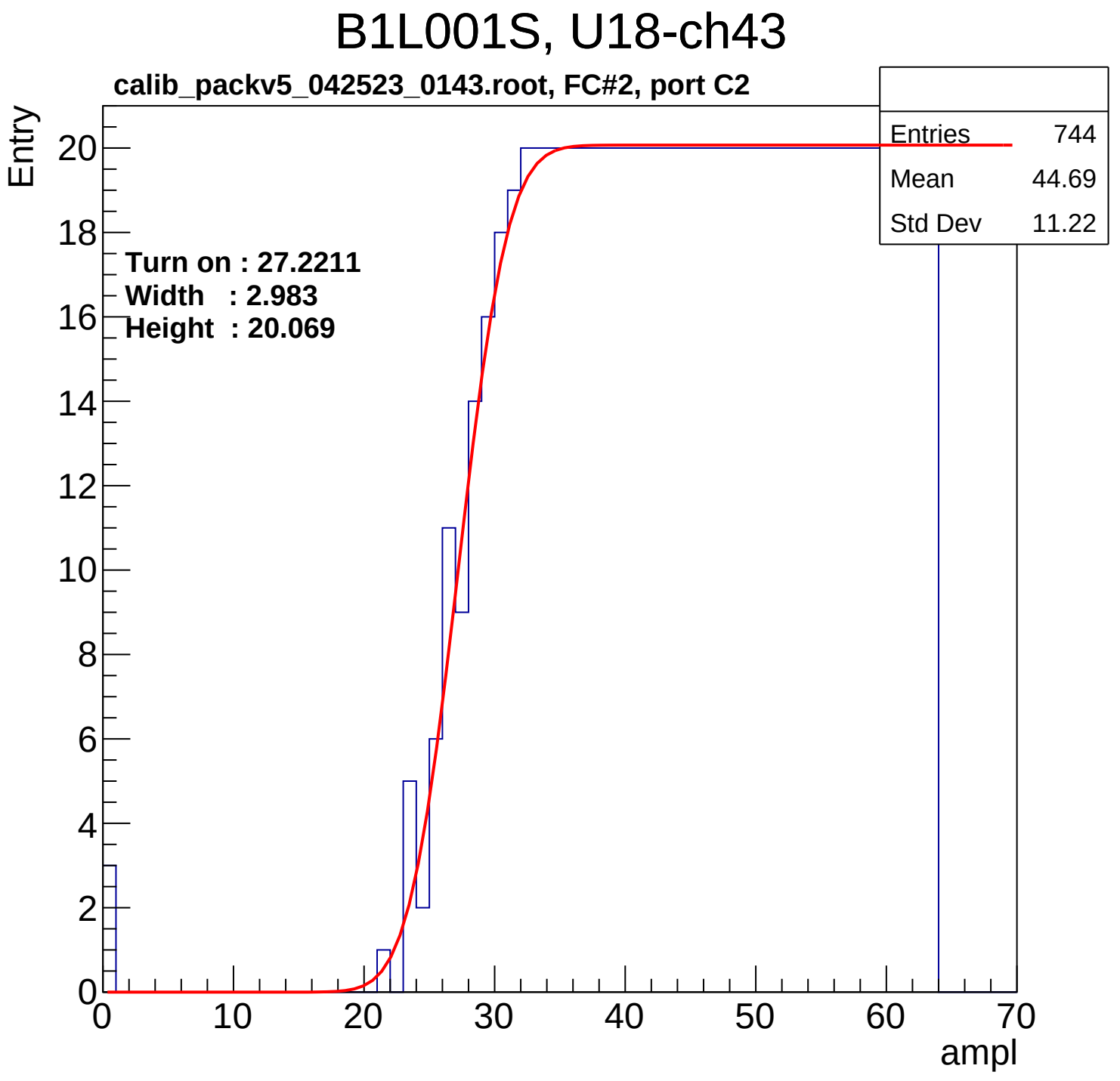
B1L001S, U18-ch43
calib_packv5_042523_0143.root, FC#2, port C2
Entries 744
Mean 44.69
Std Dev 11.22
Turn on : 27.2211
Width : 2.983
Height : 20.069
Entry
ampl
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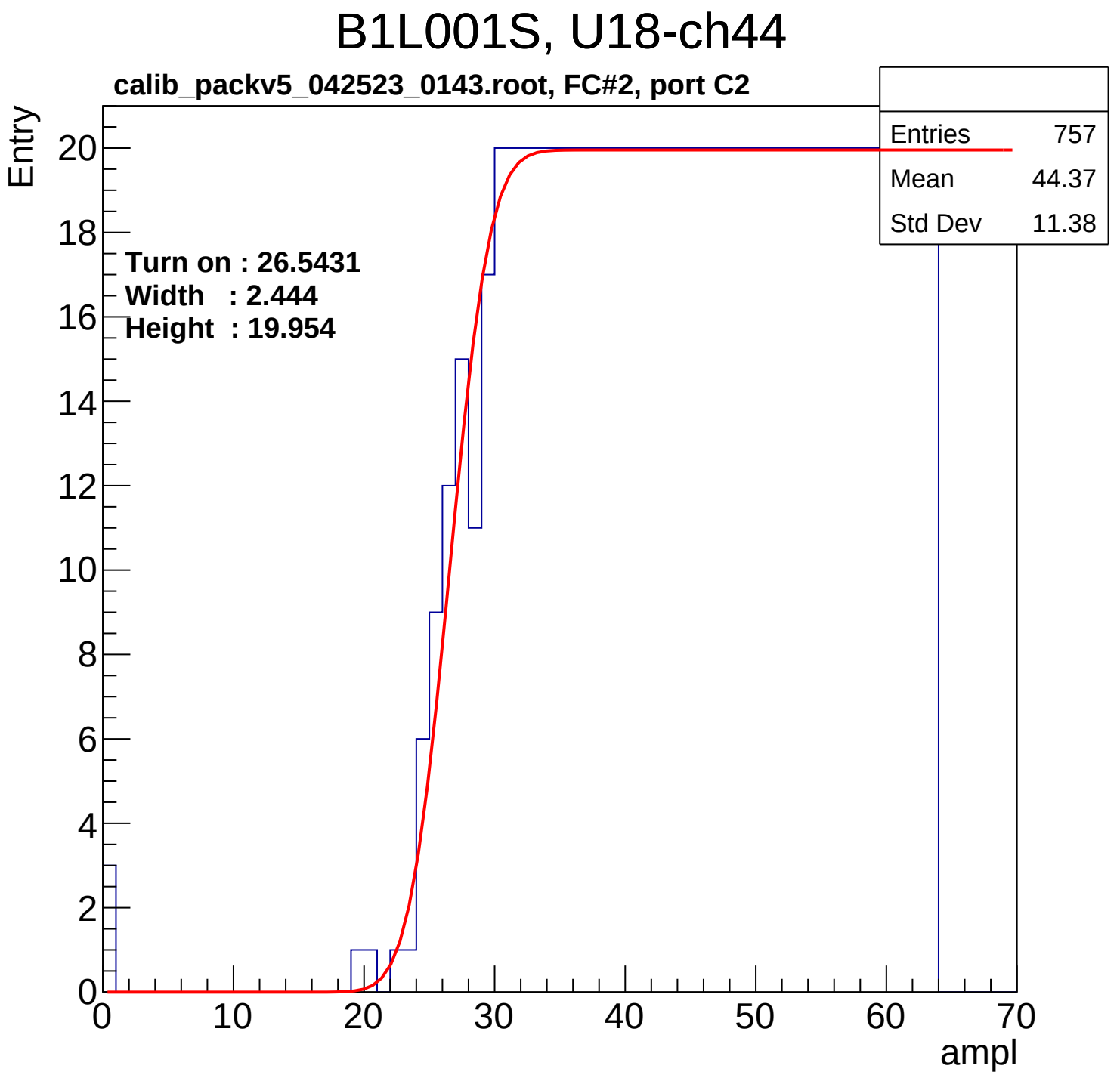
B1L001S, U18-ch44
calib_packv5_042523_0143.root, FC#2, port C2
Entries 757
Mean 44.37
Std Dev 11.38
Turn on : 26.5431
Width : 2.444
Height : 19.954
Entry
ampl
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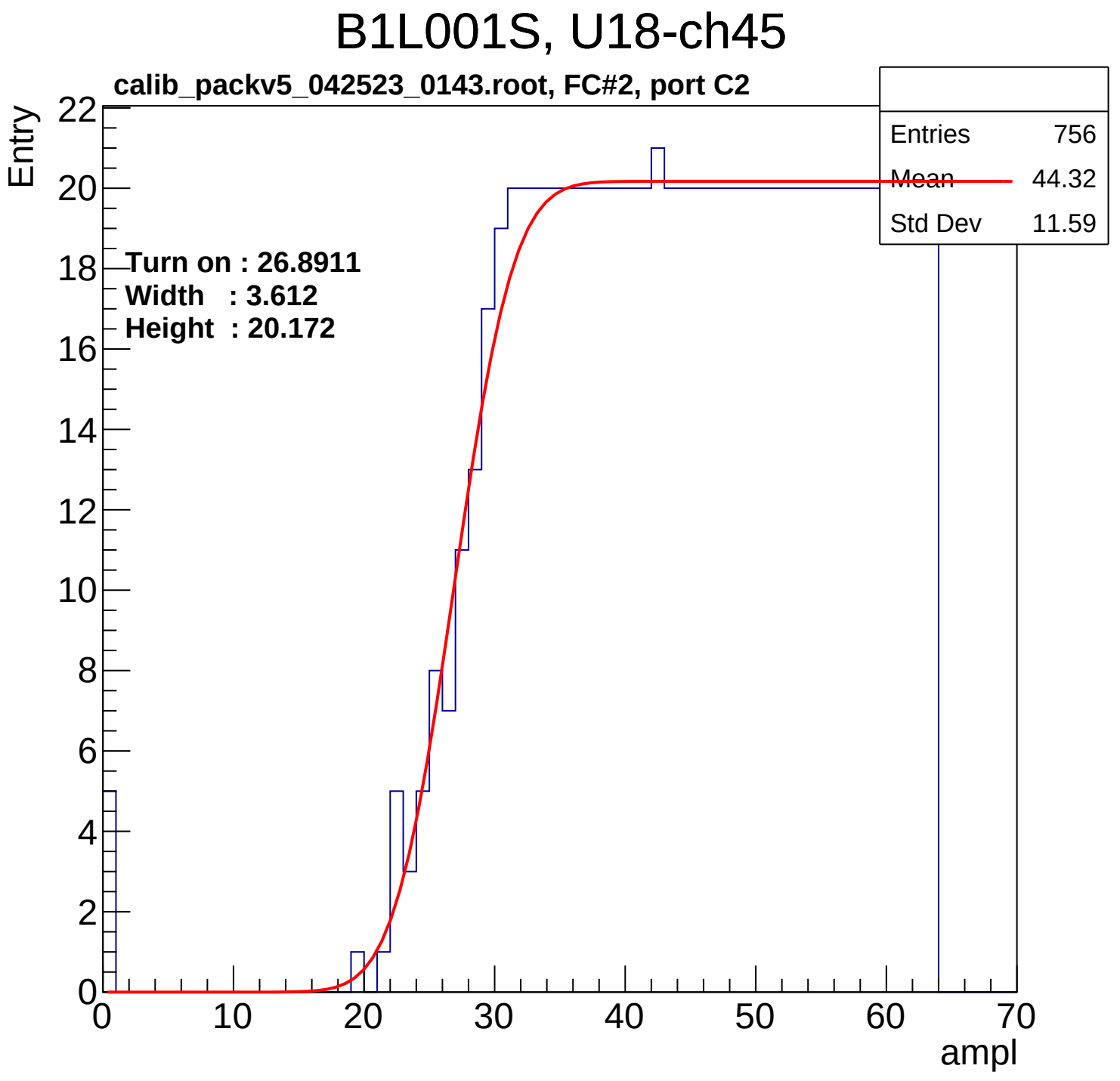
B1L001S, U18-ch45
calib_packv5_042523_0143.root, FC#2, port C2
Entries 756
Mean 44.32
Std Dev 11.59
Turn on : 26.8911
Width : 3.612
Height : 20.172
Entry
ampl
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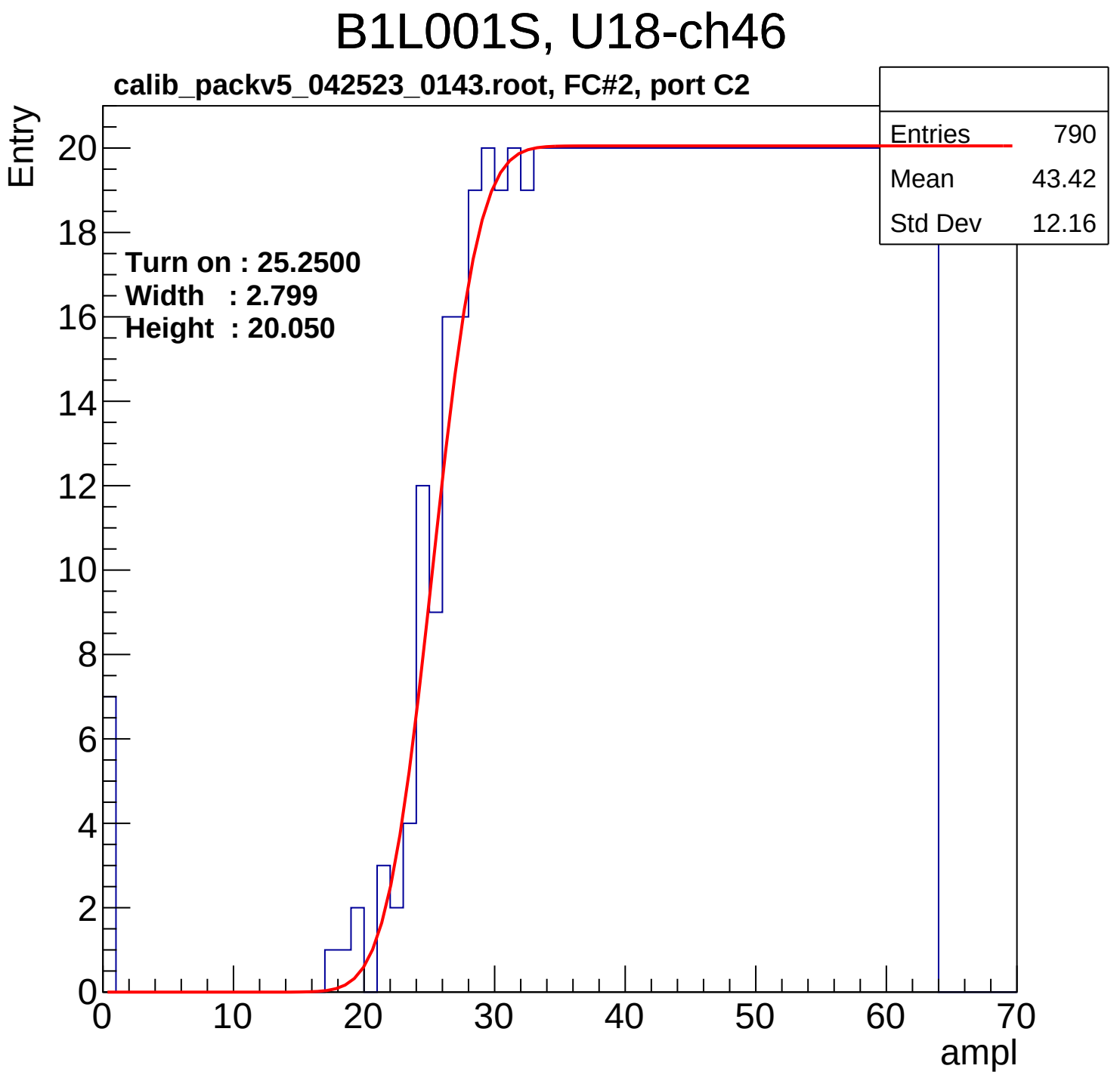
B1L001S, U18-ch46
calib_packv5_042523_0143.root, FC#2, port C2
Entries 790
Mean 43.42
Std Dev 12.16
Turn on : 25.2500
Width : 2.799
Height : 20.050
Entry
ampl
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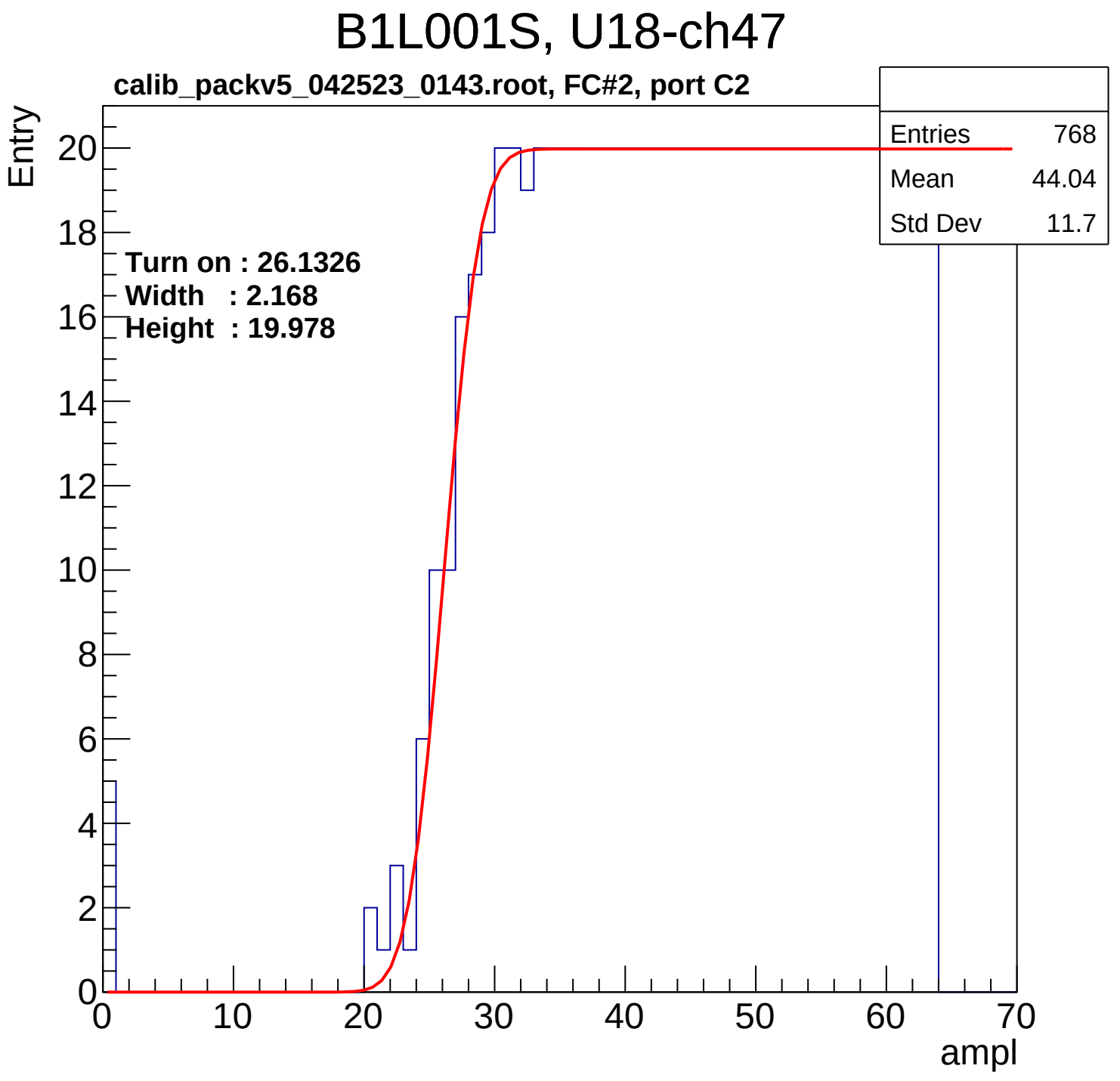
B1L001S, U18-ch47
calib_packv5_042523_0143.root, FC#2, port C2
Entries 768
Mean 44.04
Std Dev 11.7
Turn on : 26.1326
Width : 2.168
Height : 19.978
Entry
ampl
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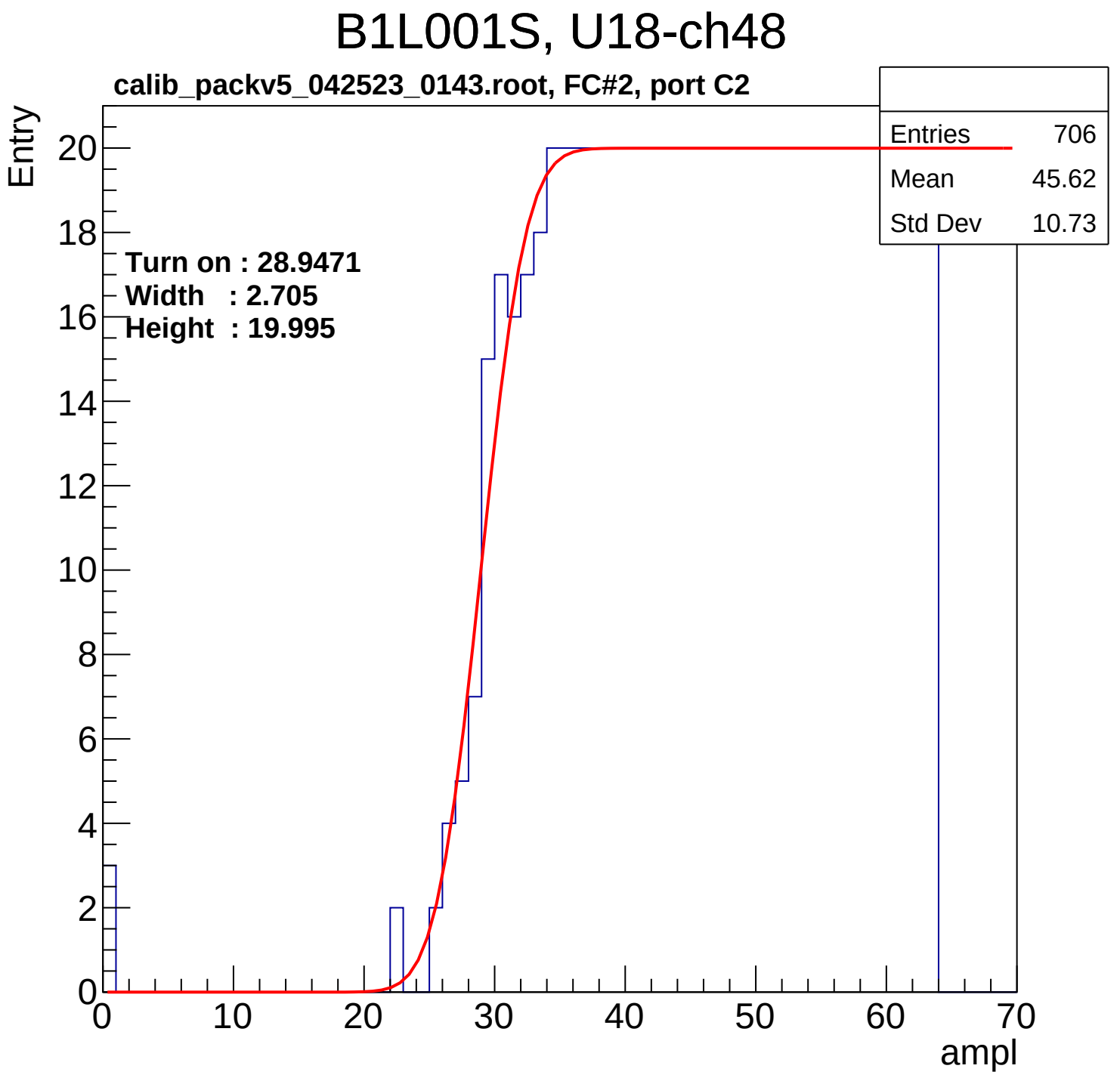
B1L001S, U18-ch48
calib_packv5_042523_0143.root, FC#2, port C2
Entries 706
Mean 45.62
Std Dev 10.73
Turn on : 28.9471
Width : 2.705
Height : 19.995
Entry
ampl
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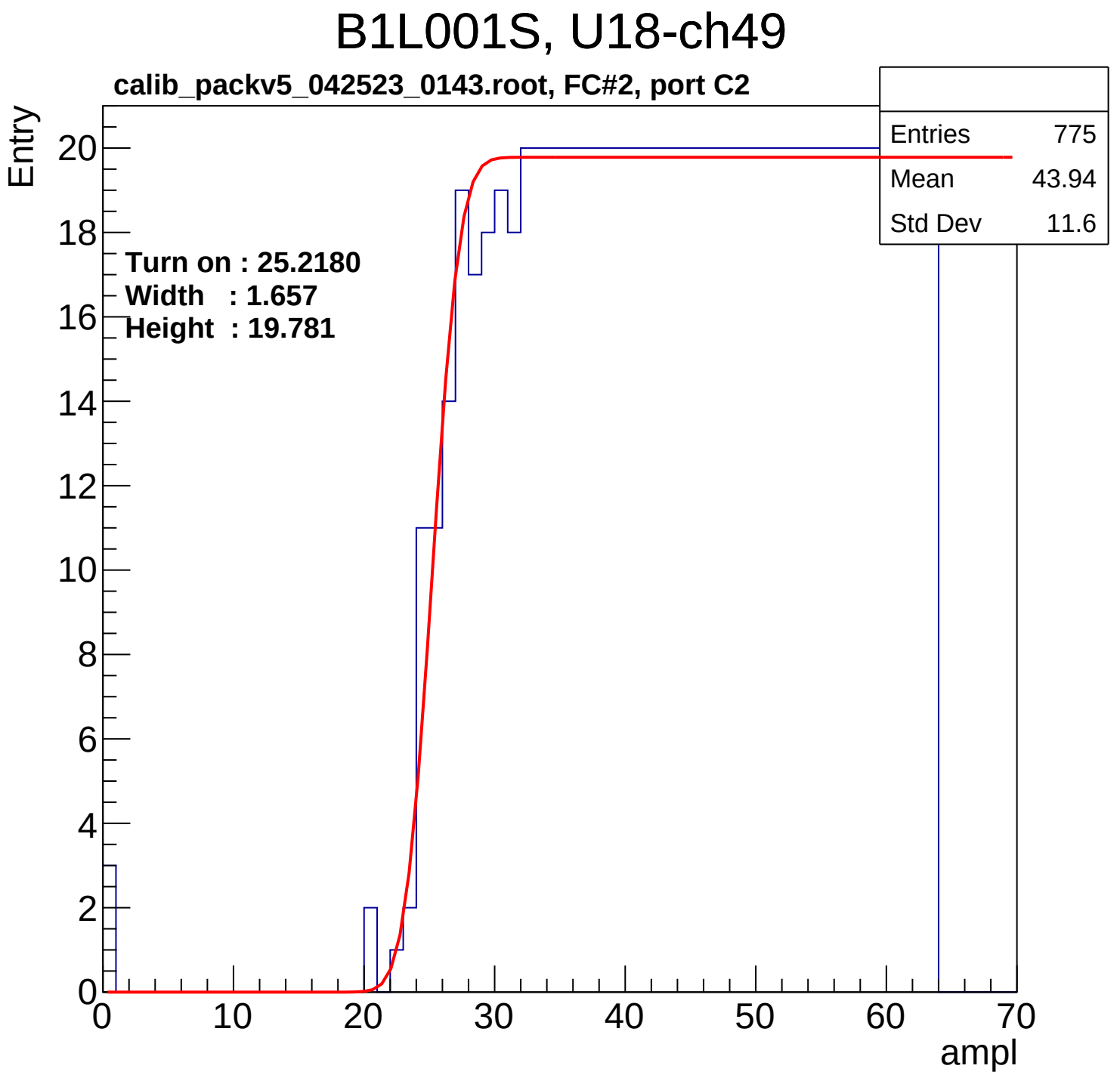
B1L001S, U18-ch49
calib_packv5_042523_0143.root, FC#2, port C2
Entries 775
Mean 43.94
Std Dev 11.6
Turn on : 25.2180
Width : 1.657
Height : 19.781
Entry
ampl
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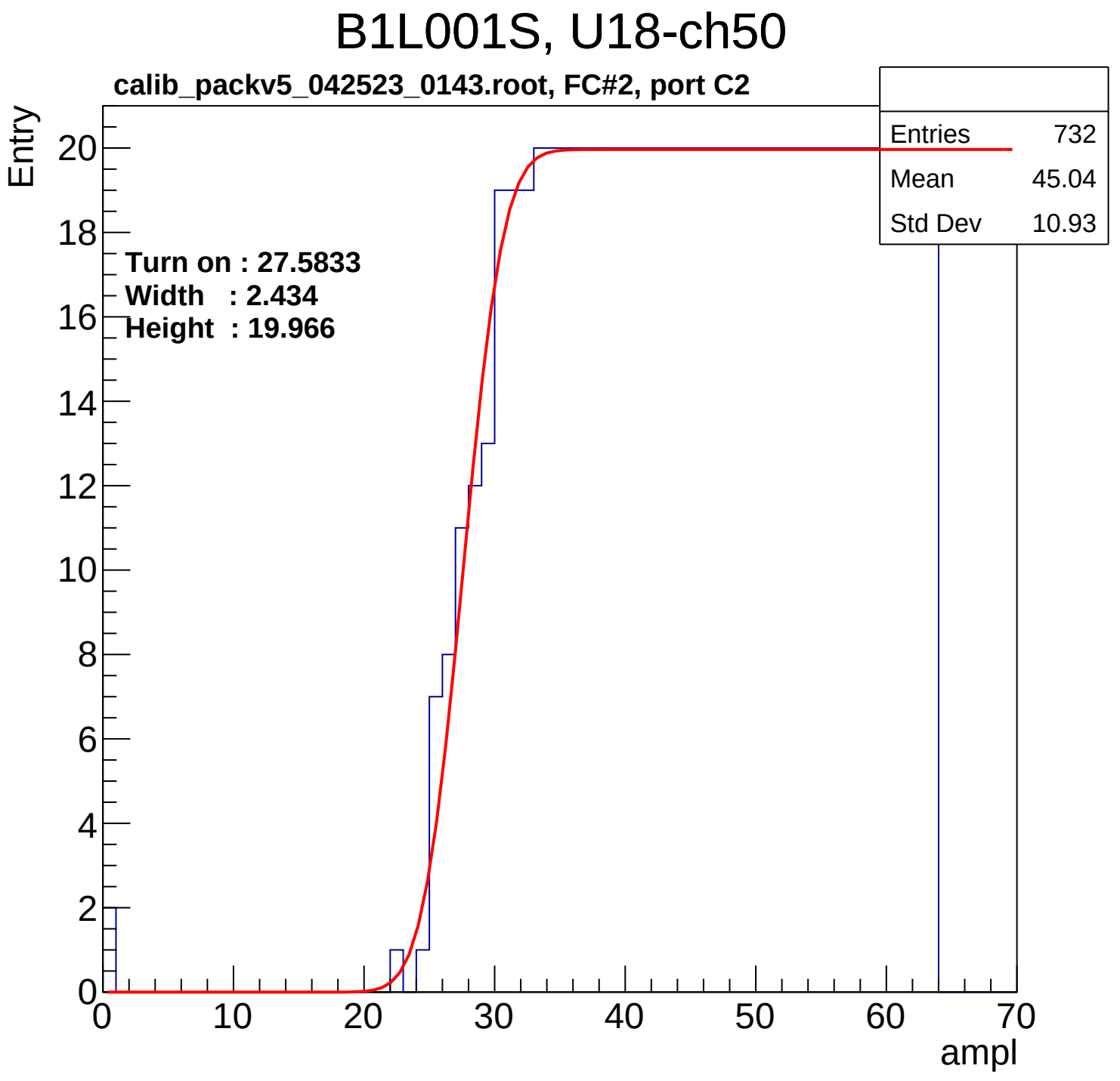
B1L001S, U18-ch50
calib_packv5_042523_0143.root, FC#2, port C2
Entries 732
Mean 45.04
Std Dev 10.93
Turn on : 27.5833
Width : 2.434
Height : 19.966
Entry
ampl
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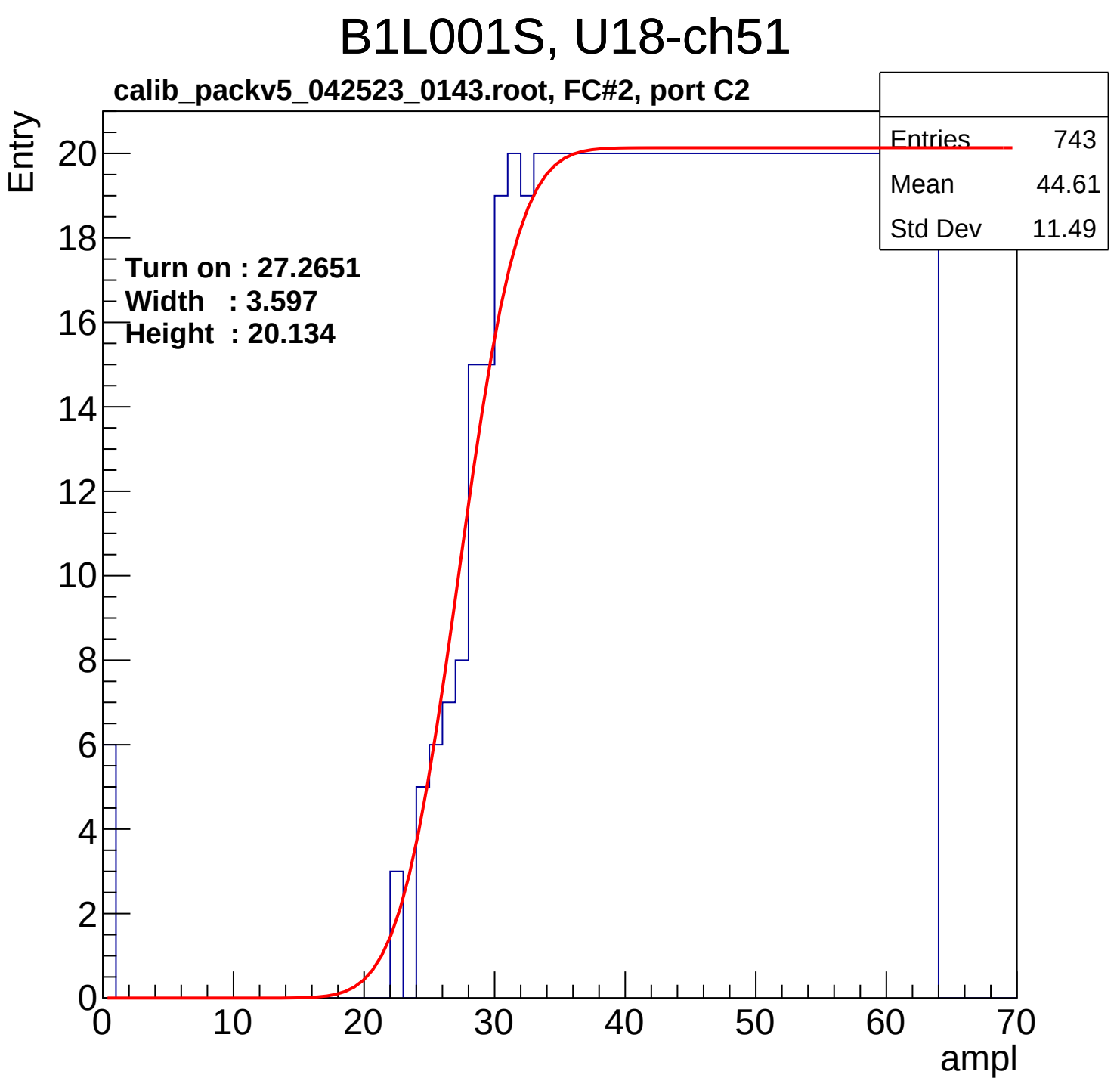
B1L001S, U18-ch51
calib_packv5_042523_0143.root, FC#2, port C2
Entries 743
Mean 44.61
Std Dev 11.49
Turn on : 27.2651
Width : 3.597
Height : 20.134
Entry
ampl
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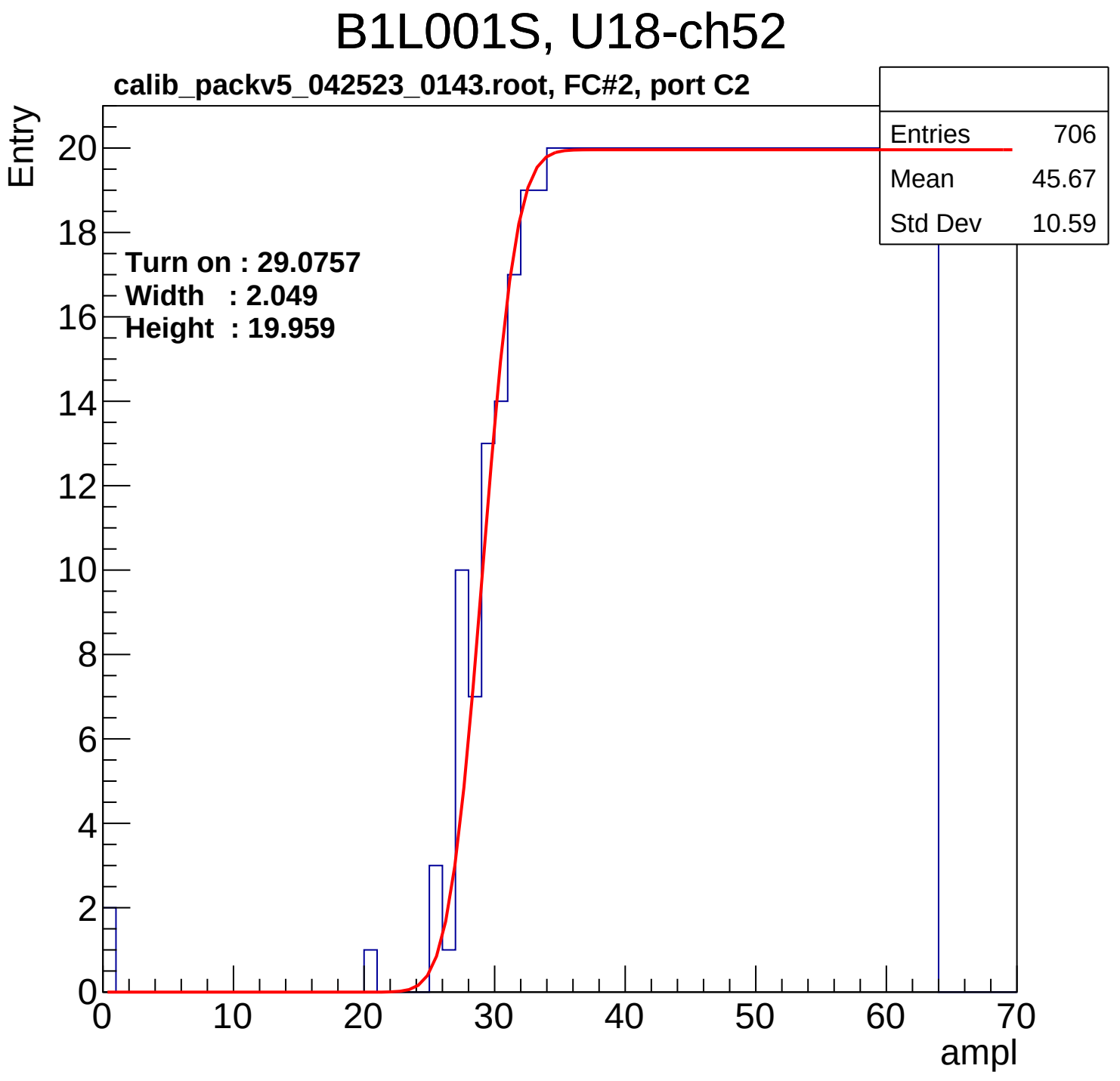
B1L001S, U18-ch52
calib_packv5_042523_0143.root, FC#2, port C2
Entries 706
Mean 45.67
Std Dev 10.59
Turn on : 29.0757
Width : 2.049
Height : 19.959
Entry
ampl
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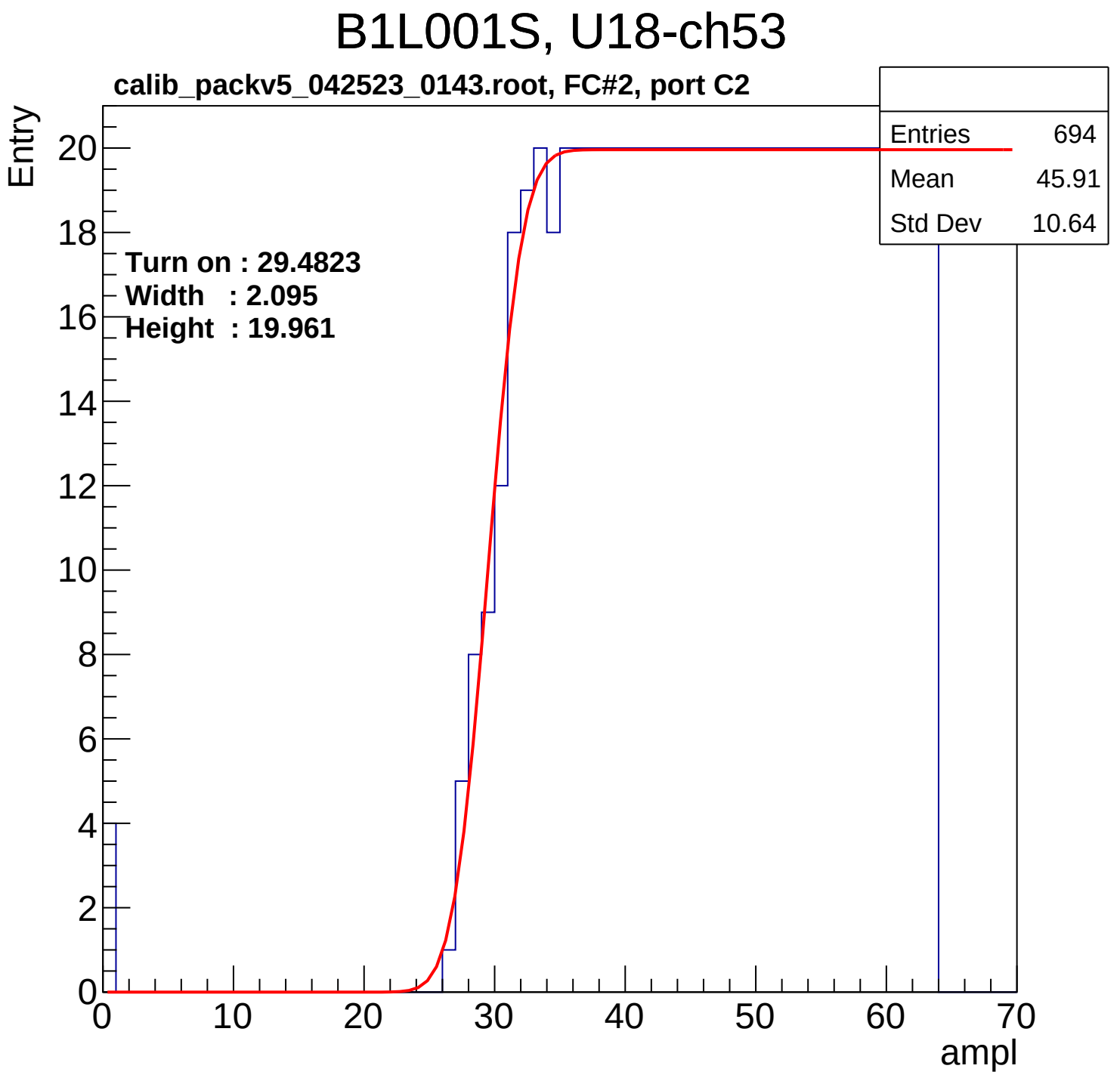
B1L001S, U18-ch53
calib_packv5_042523_0143.root, FC#2, port C2
Entries 694
Mean 45.91
Std Dev 10.64
Turn on : 29.4823
Width : 2.095
Height : 19.961
Entry
ampl
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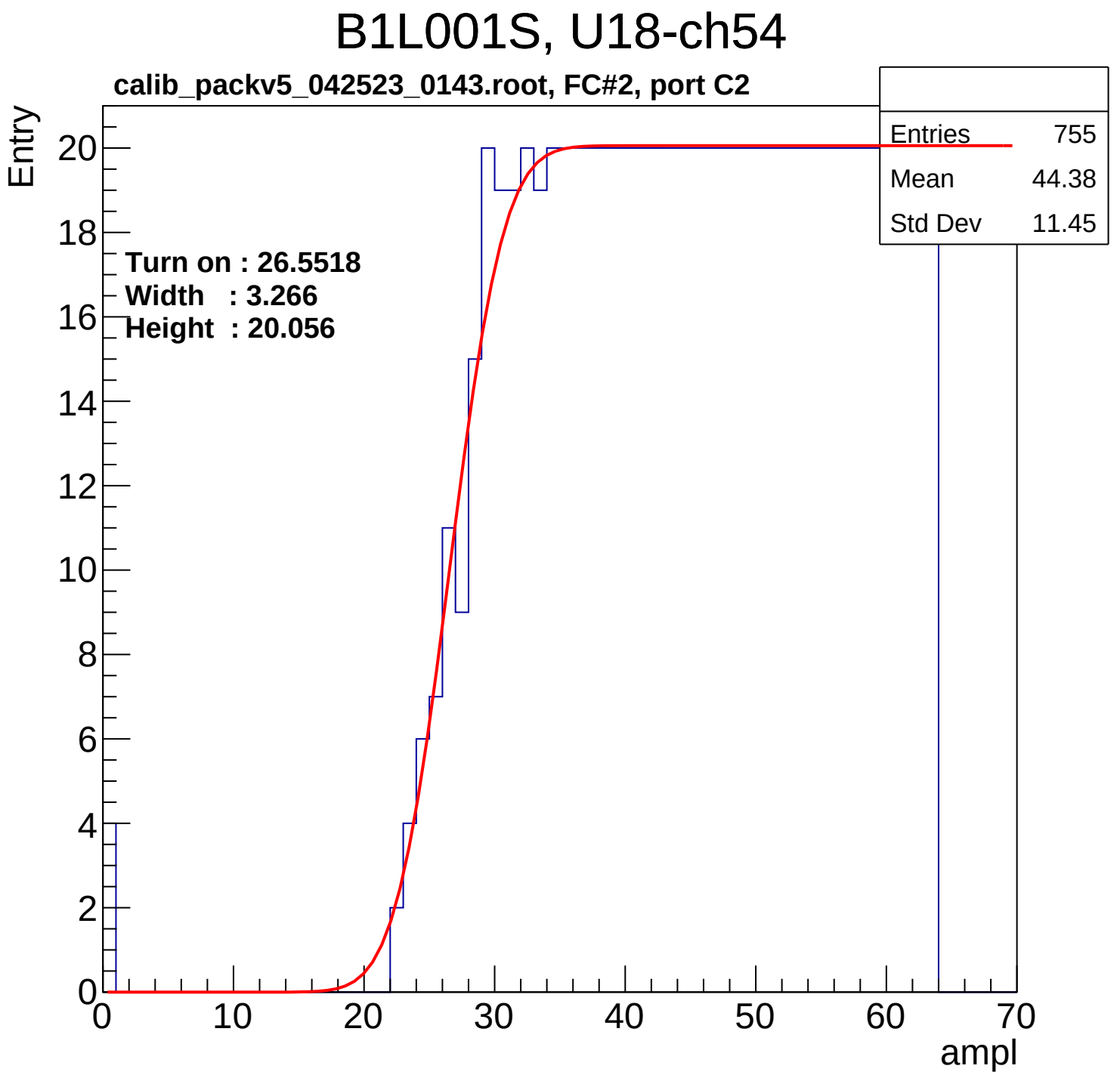
B1L001S, U18-ch54
calib_packv5_042523_0143.root, FC#2, port C2
Entries 755
Mean 44.38
Std Dev 11.45
Turn on : 26.5518
Width : 3.266
Height : 20.056
Entry
ampl
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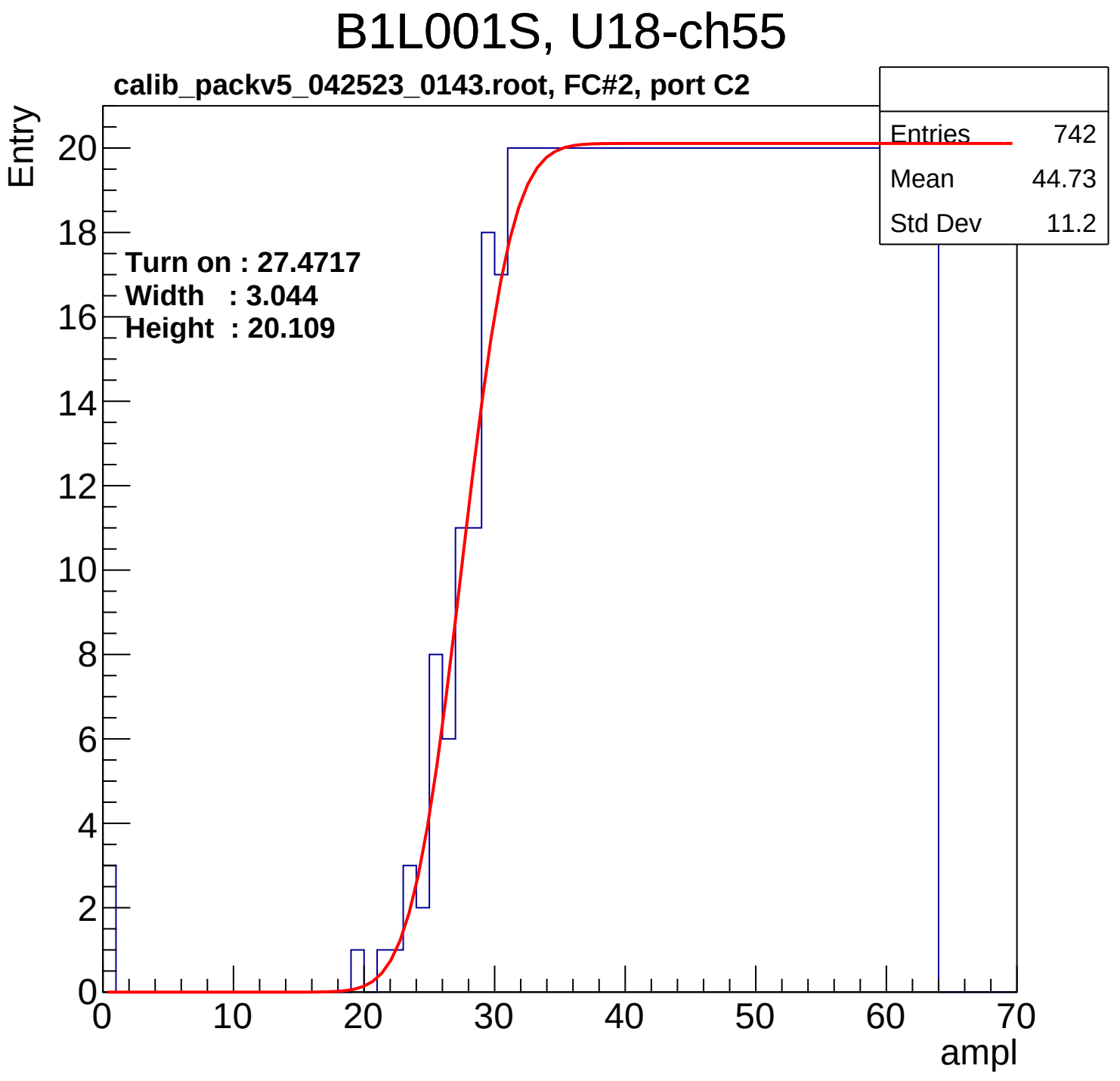
B1L001S, U18-ch55
calib_packv5_042523_0143.root, FC#2, port C2
Entries 742
Mean 44.73
Std Dev 11.2
Turn on : 27.4717
Width : 3.044
Height : 20.109
Entry
ampl
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2
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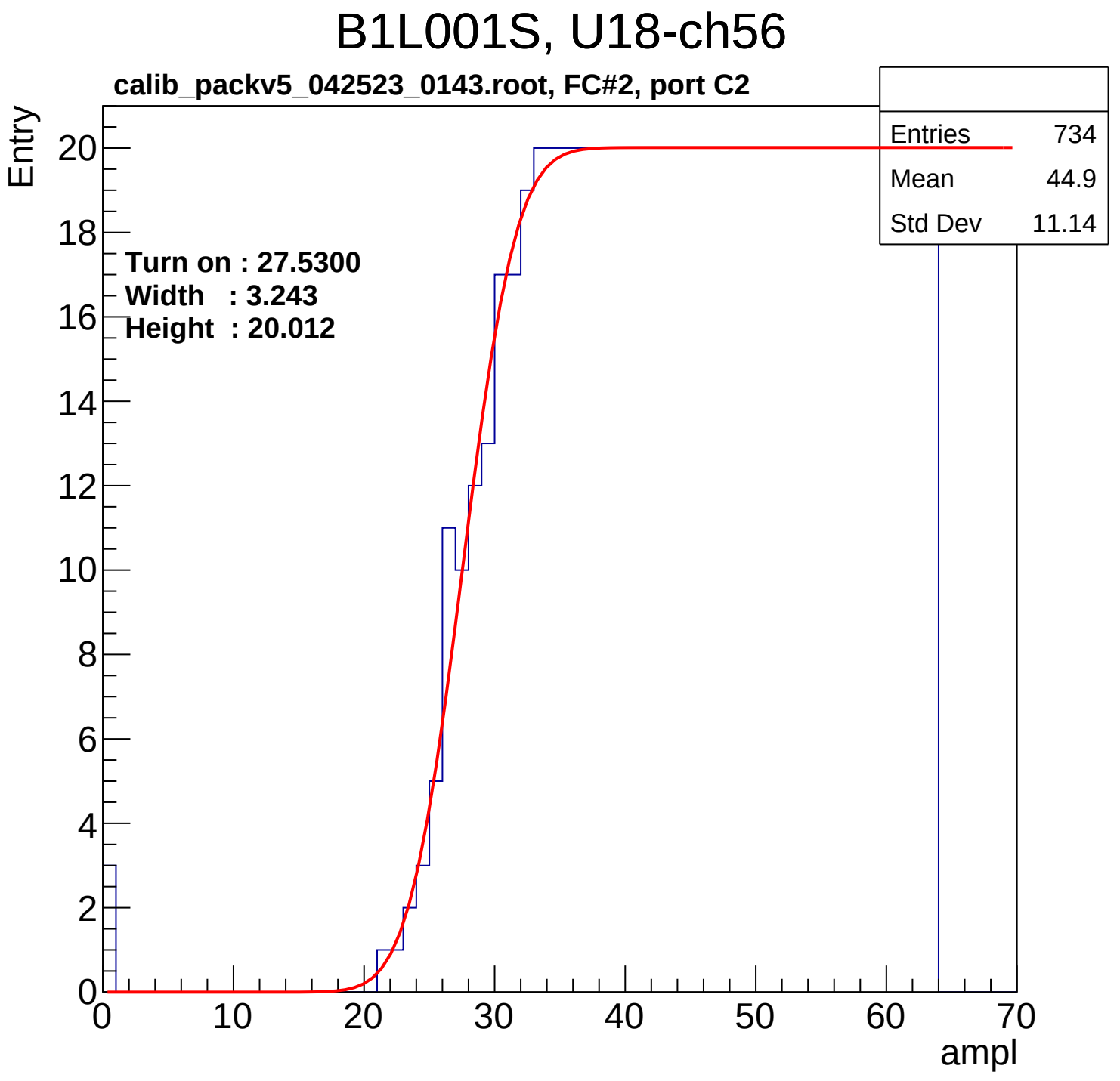
B1L001S, U18-ch56
calib_packv5_042523_0143.root, FC#2, port C2
Entries 734
Mean 44.9
Std Dev 11.14
Turn on : 27.5300
Width : 3.243
Height : 20.012
Entry
ampl
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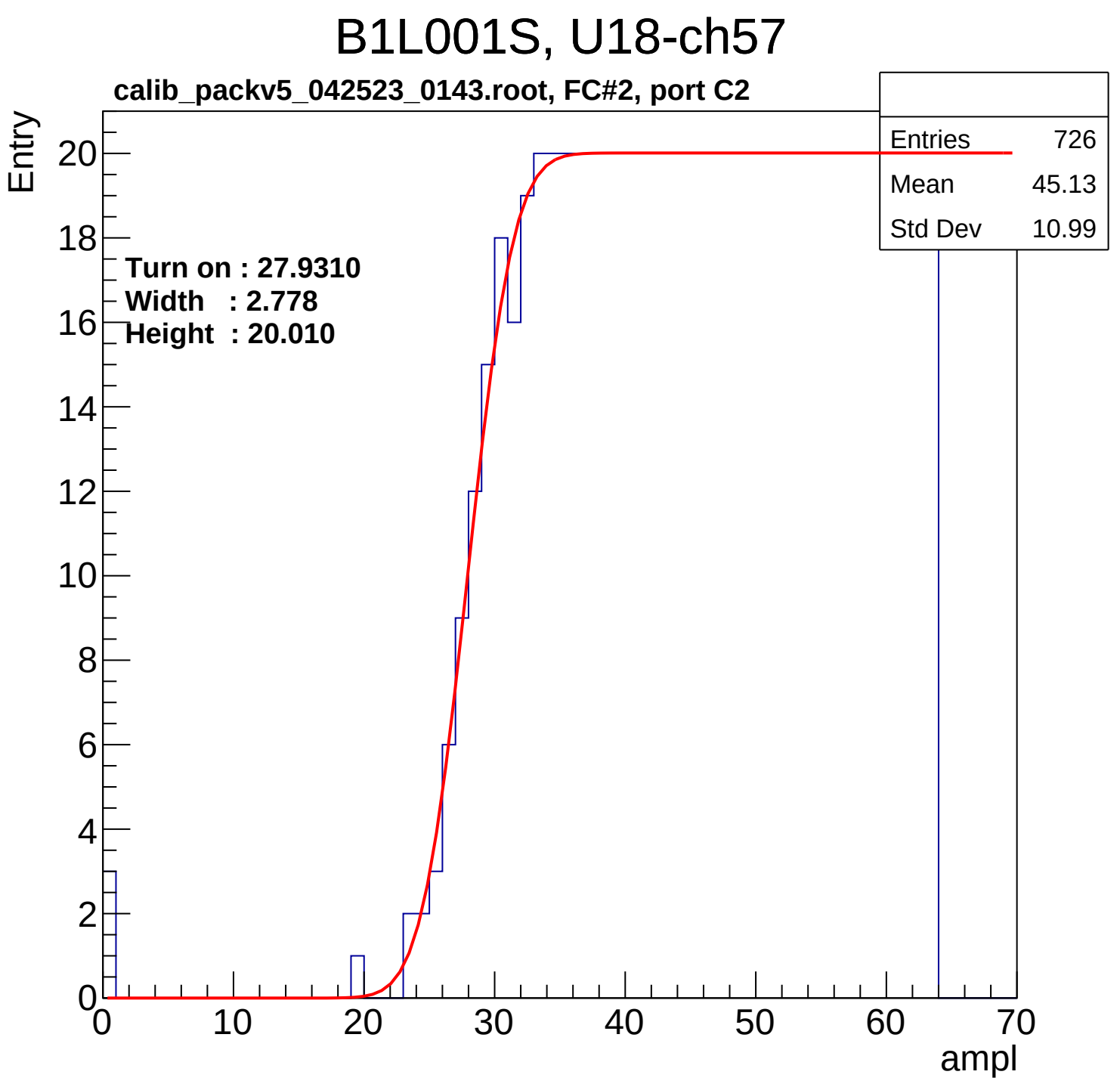
B1L001S, U18-ch57
calib_packv5_042523_0143.root, FC#2, port C2
Entries 726
Mean 45.13
Std Dev 10.99
Turn on : 27.9310
Width : 2.778
Height : 20.010
Entry
ampl
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2
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6
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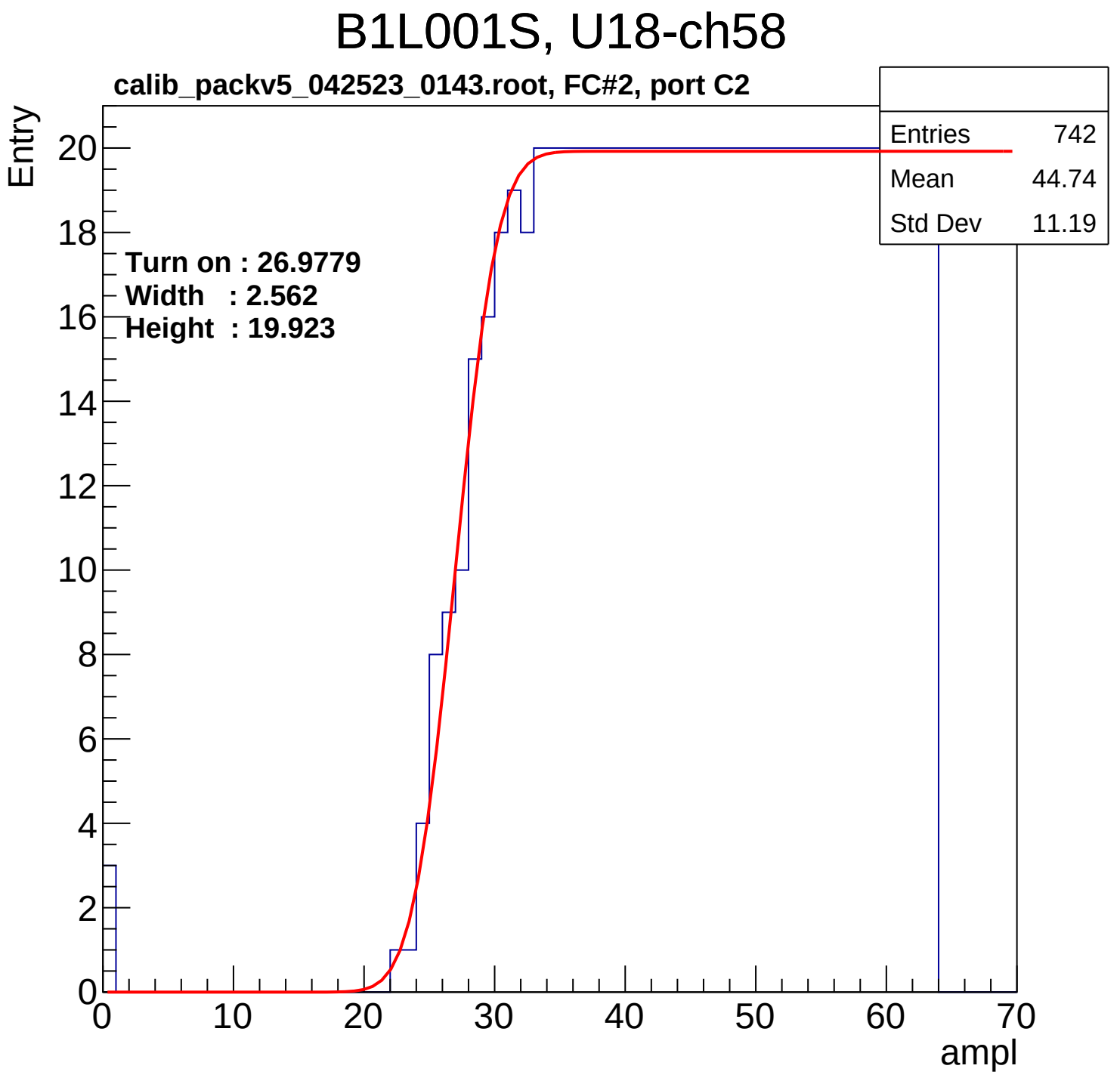
B1L001S, U18-ch58
calib_packv5_042523_0143.root, FC#2, port C2
Entries 742
Mean 44.74
Std Dev 11.19
Turn on : 26.9779
Width : 2.562
Height : 19.923
Entry
ampl
0
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6
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10
12
14
16
18
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0
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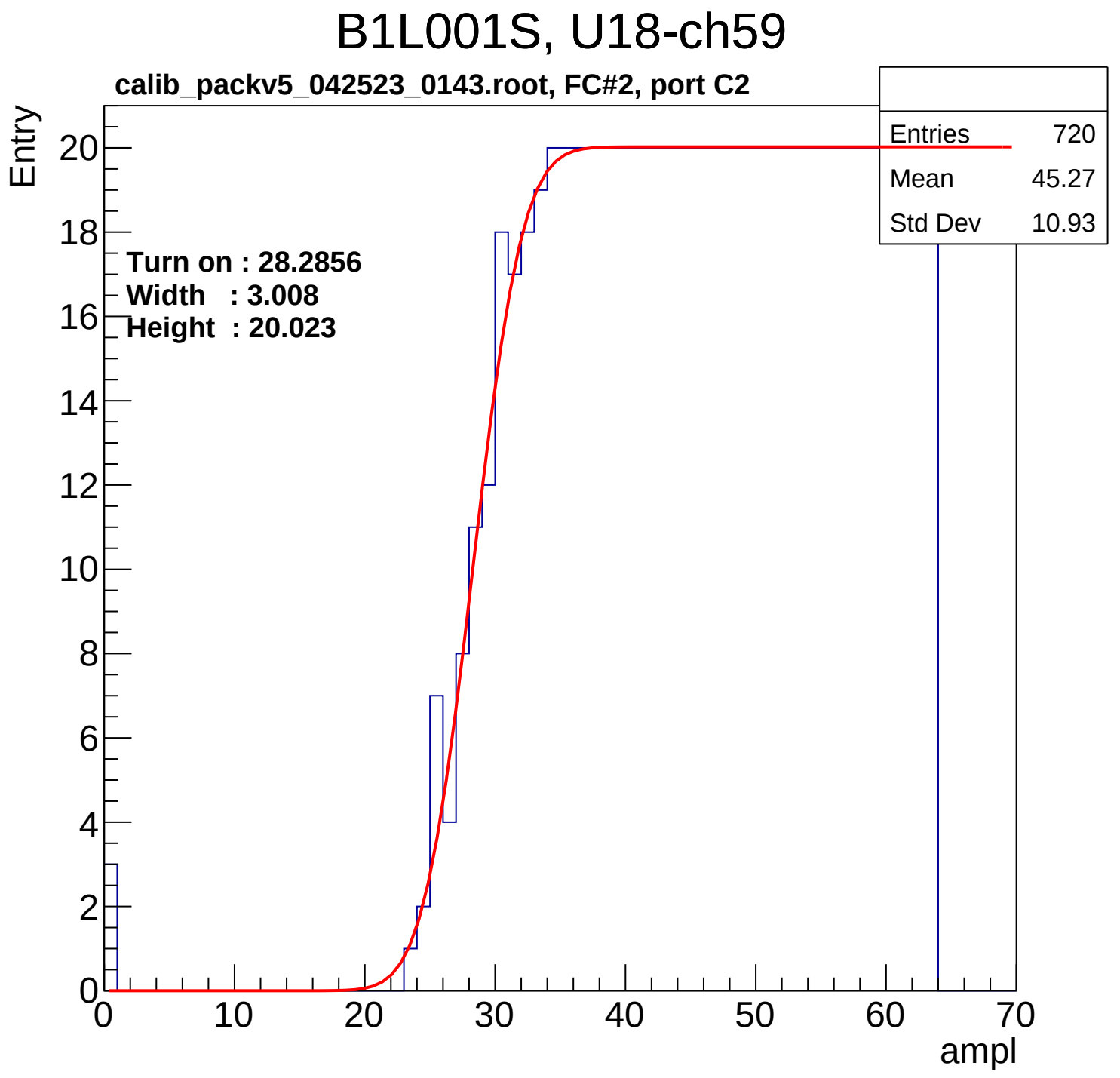
B1L001S, U18-ch59
calib_packv5_042523_0143.root, FC#2, port C2
Entries 720
Mean 45.27
Std Dev 10.93
Turn on : 28.2856
Width : 3.008
Height : 20.023
Entry
ampl
0
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6
8
10
12
14
16
18
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0
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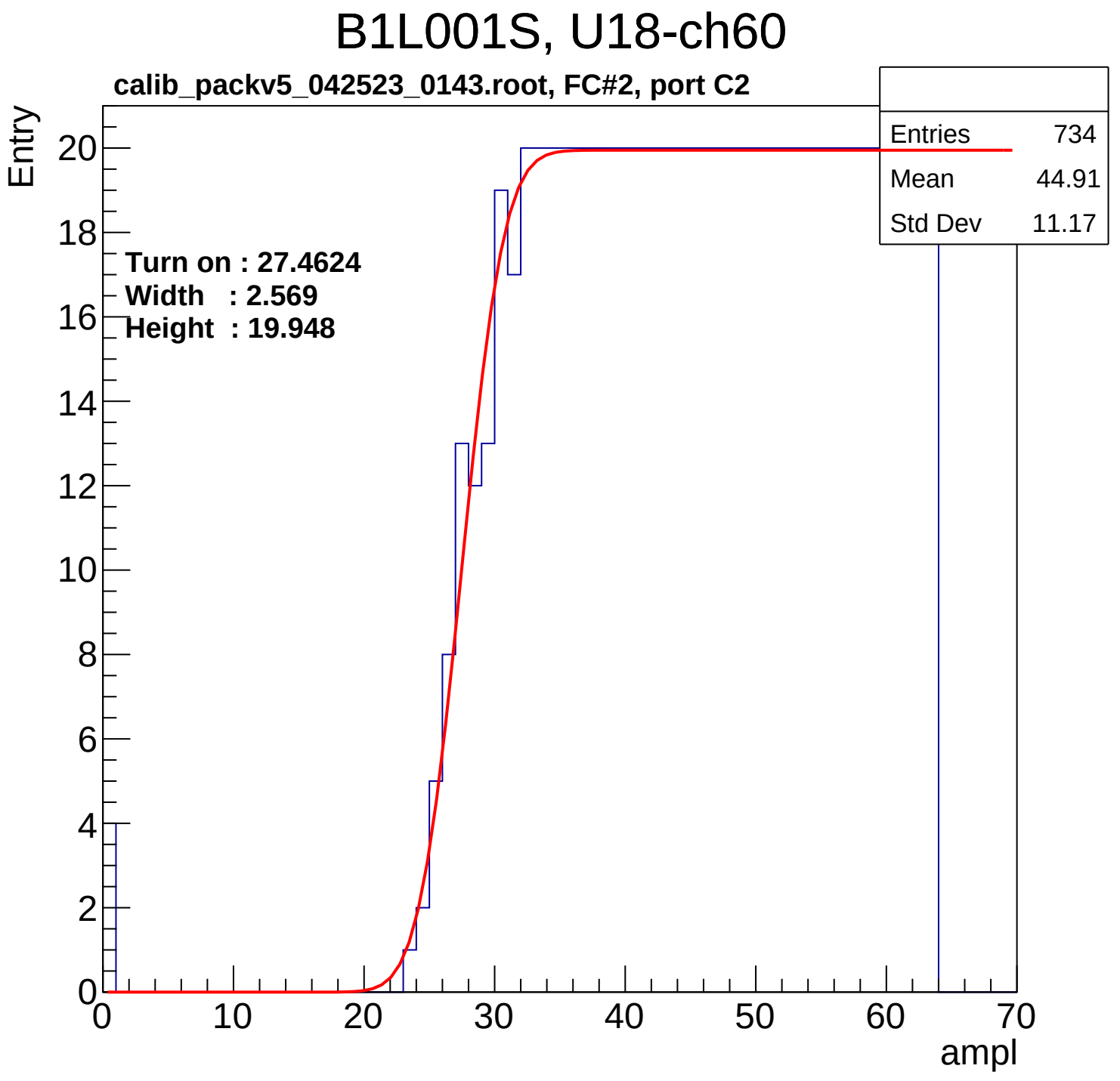
B1L001S, U18-ch60
calib_packv5_042523_0143.root, FC#2, port C2
Entries 734
Mean 44.91
Std Dev 11.17
Turn on : 27.4624
Width : 2.569
Height : 19.948
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
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20
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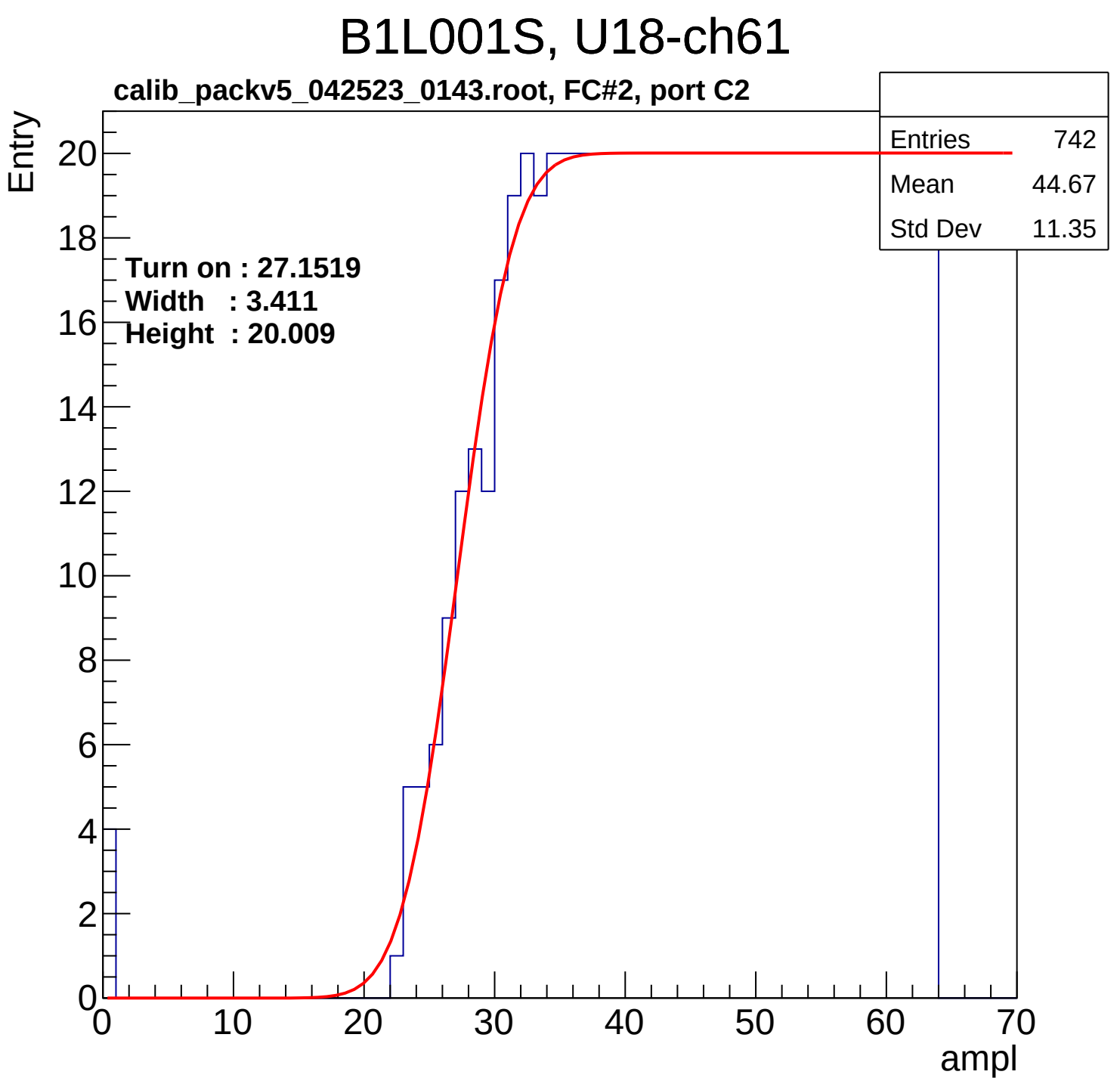
B1L001S, U18-ch61
calib_packv5_042523_0143.root, FC#2, port C2
Entries 742
Mean 44.67
Std Dev 11.35
Turn on : 27.1519
Width : 3.411
Height : 20.009
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
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20
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60
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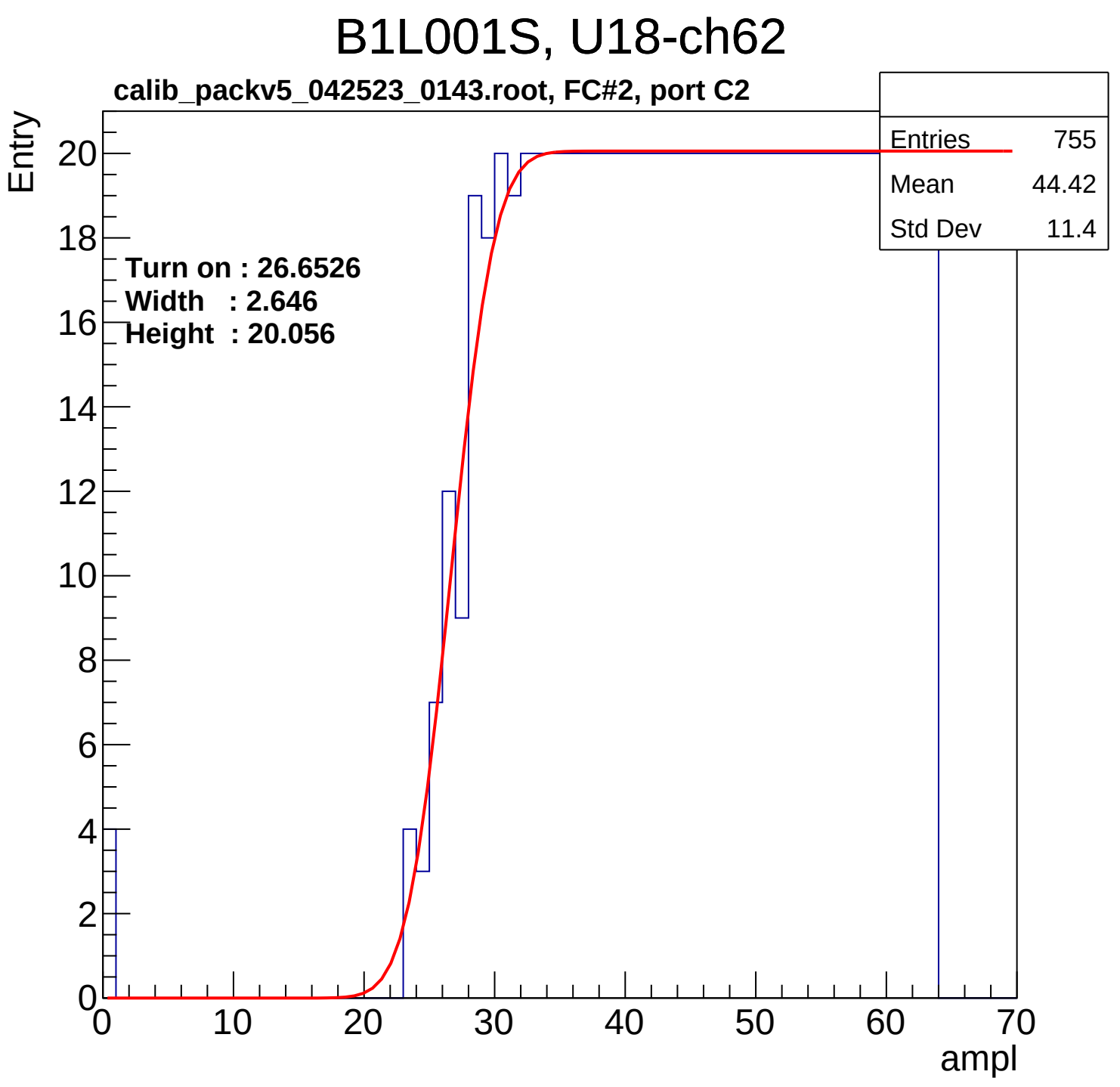
B1L001S, U18-ch62
calib_packv5_042523_0143.root, FC#2, port C2
Entries 755
Mean 44.42
Std Dev 11.4
Turn on : 26.6526
Width : 2.646
Height : 20.056
Entry
ampl
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6
8
10
12
14
16
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60
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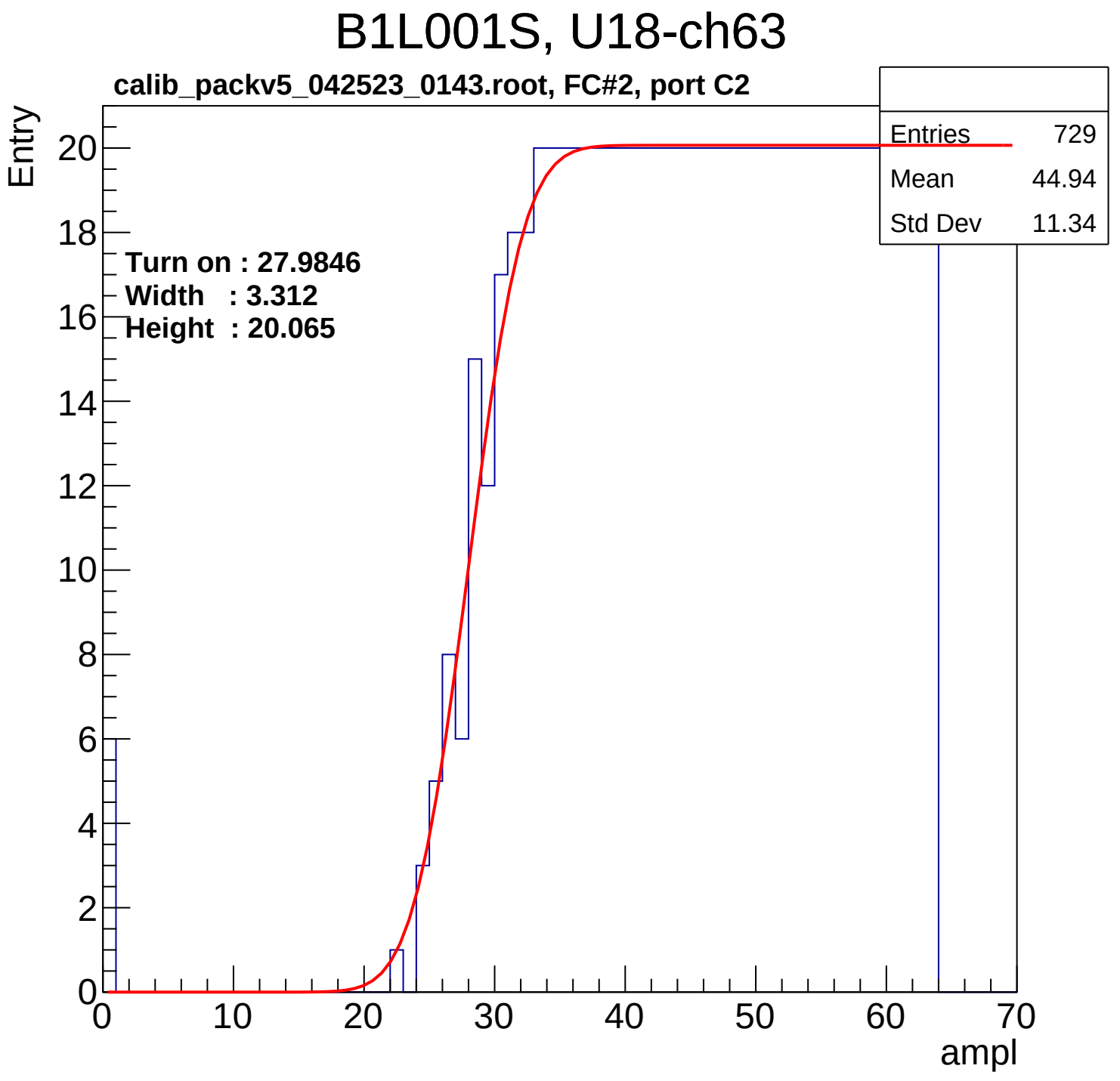
B1L001S, U18-ch63
calib_packv5_042523_0143.root, FC#2, port C2
Entries 729
Mean 44.94
Std Dev 11.34
Turn on : 27.9846
Width : 3.312
Height : 20.065
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
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60
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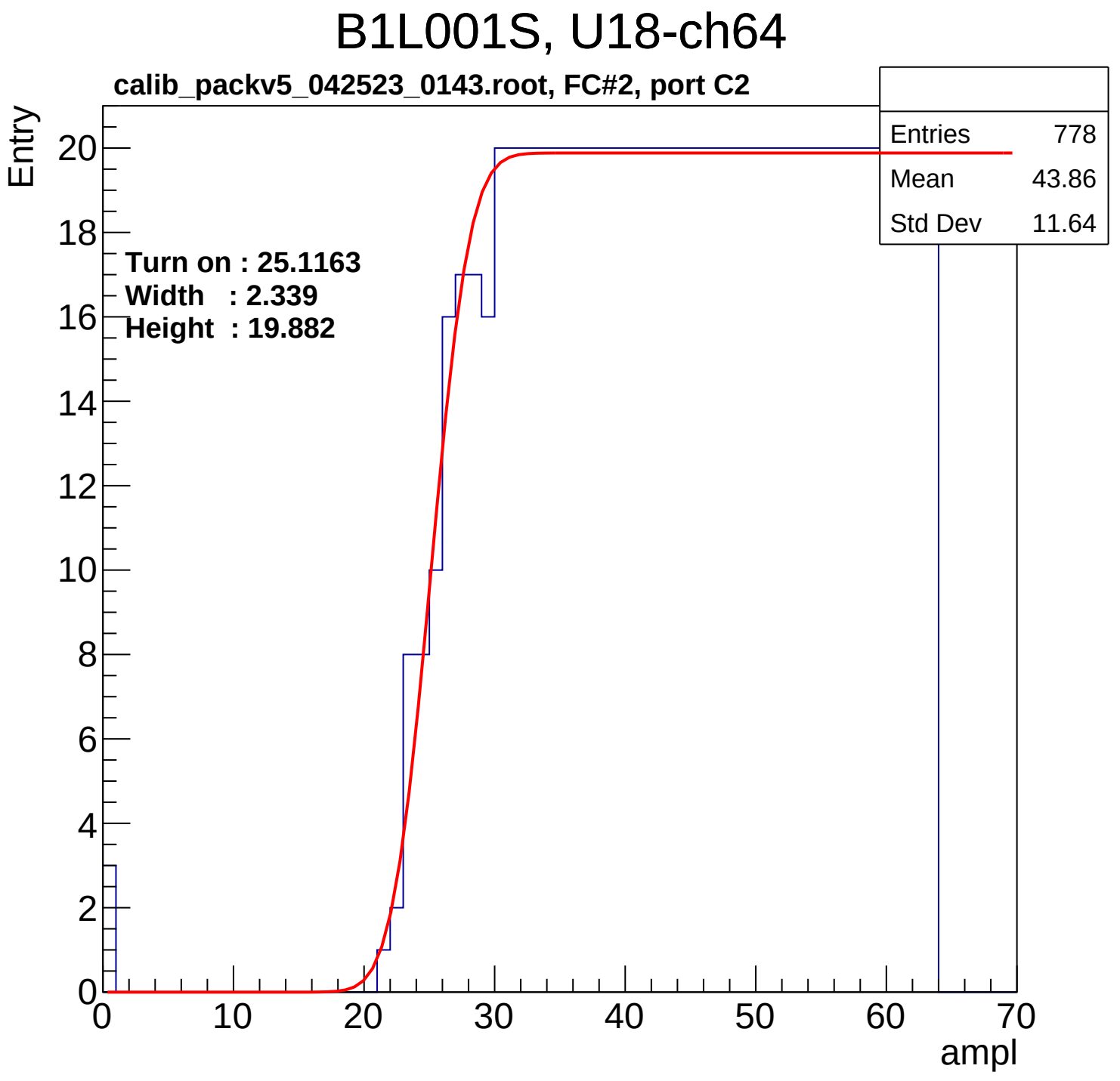
B1L001S, U18-ch64
calib_packv5_042523_0143.root, FC#2, port C2
Entries 778
Mean 43.86
Std Dev 11.64
Turn on : 25.1163
Width : 2.339
Height : 19.882
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
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20
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60
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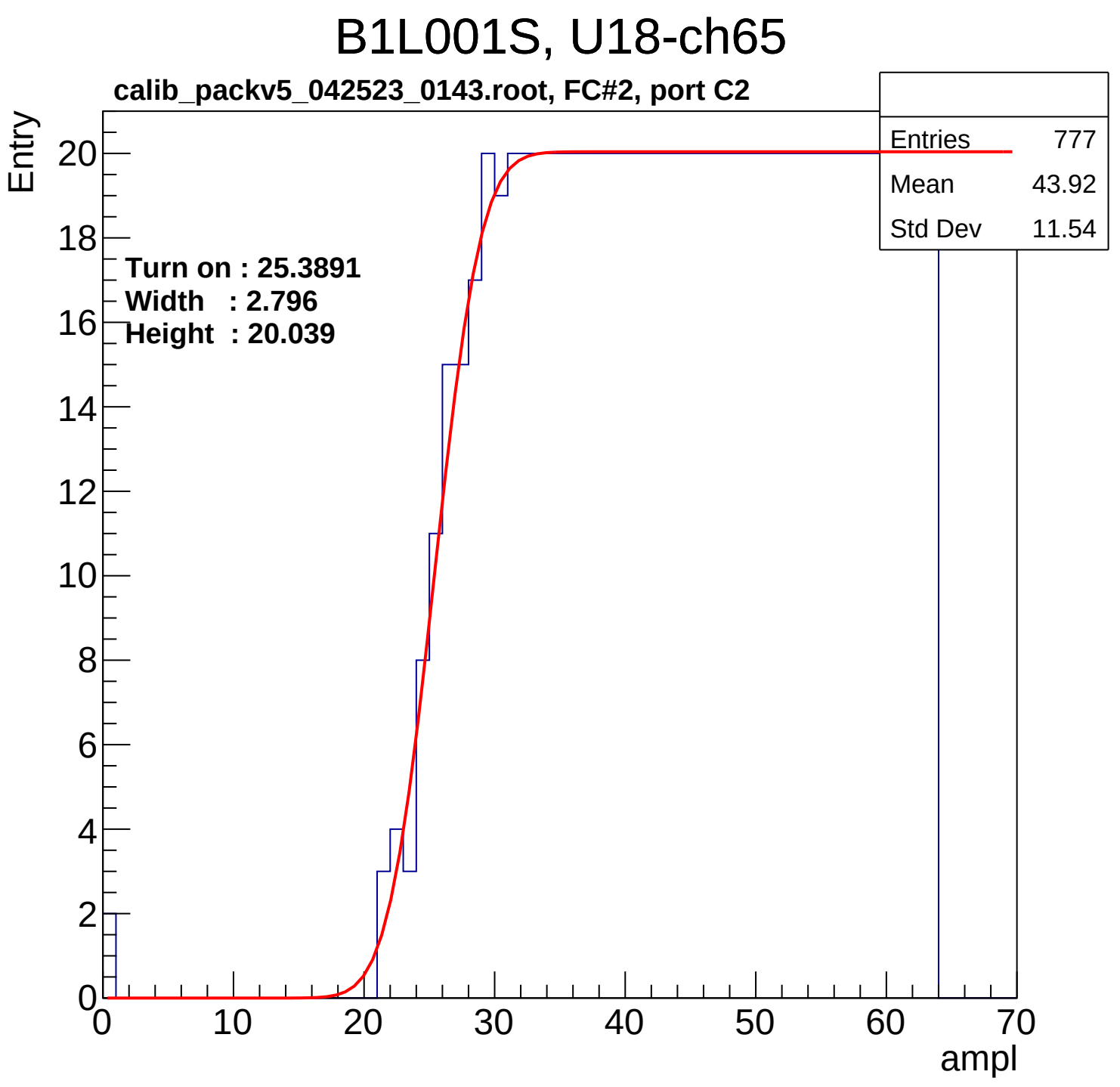
B1L001S, U18-ch65
calib_packv5_042523_0143.root, FC#2, port C2
Entries 777
Mean 43.92
Std Dev 11.54
Turn on : 25.3891
Width : 2.796
Height : 20.039
Entry
ampl
0
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4
6
8
10
12
14
16
18
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0
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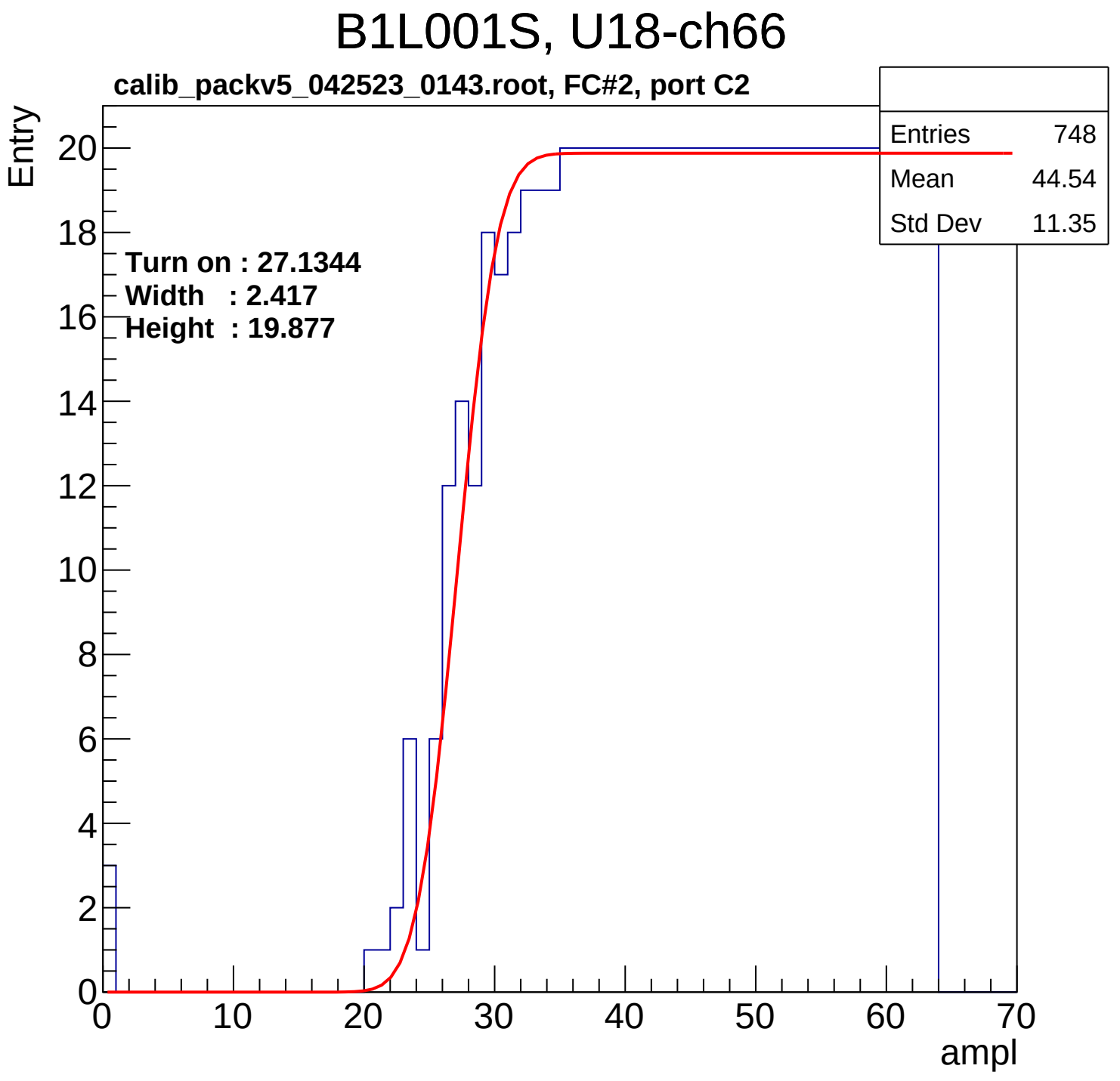
B1L001S, U18-ch66
calib_packv5_042523_0143.root, FC#2, port C2
Entries 748
Mean 44.54
Std Dev 11.35
Turn on : 27.1344
Width : 2.417
Height : 19.877
Entry
ampl
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6
8
10
12
14
16
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0
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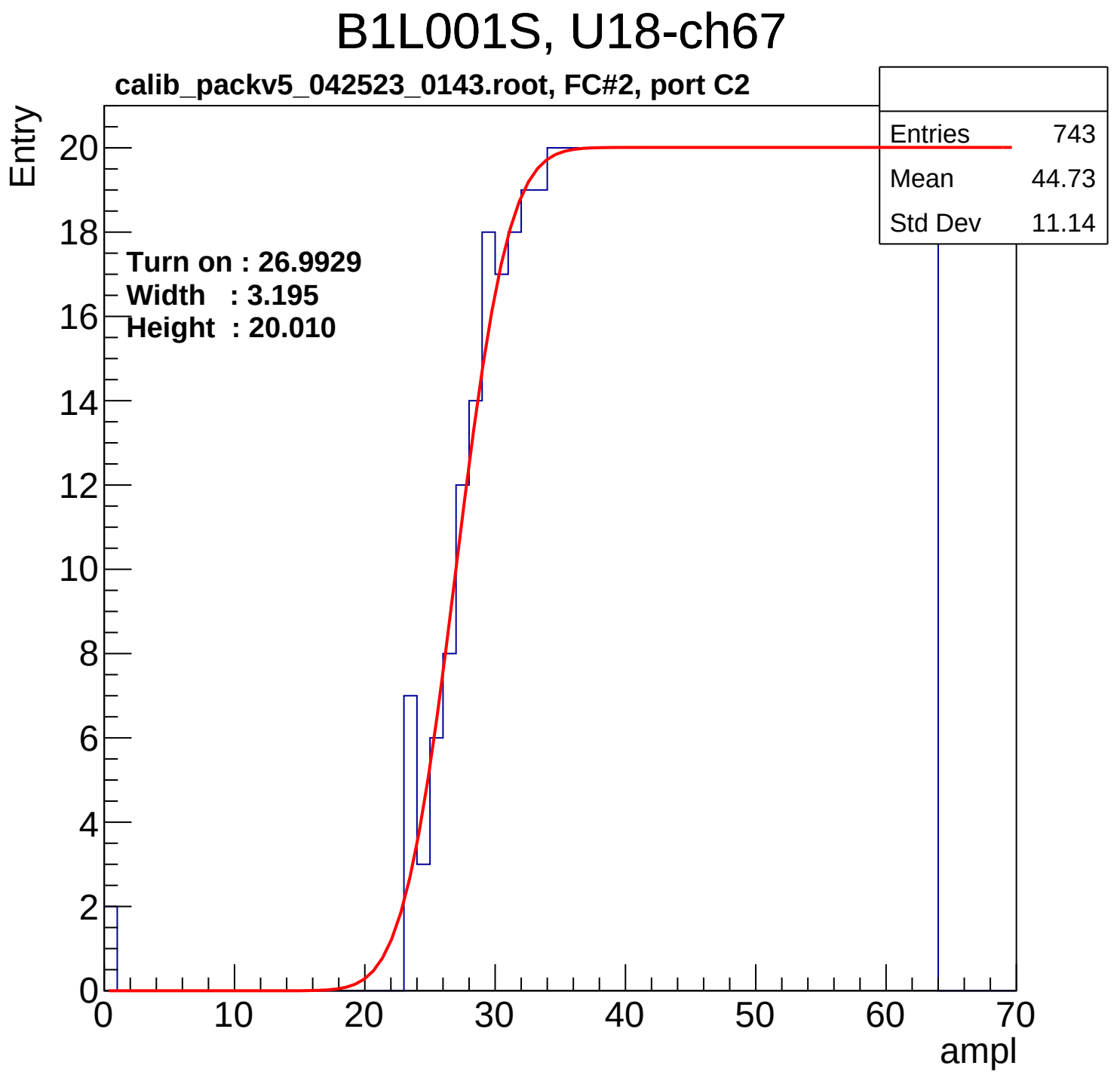
B1L001S, U18-ch67
calib_packv5_042523_0143.root, FC#2, port C2
Entries 743
Mean 44.73
Std Dev 11.14
Turn on : 26.9929
Width : 3.195
Height : 20.010
Entry
ampl
0
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6
8
10
12
14
16
18
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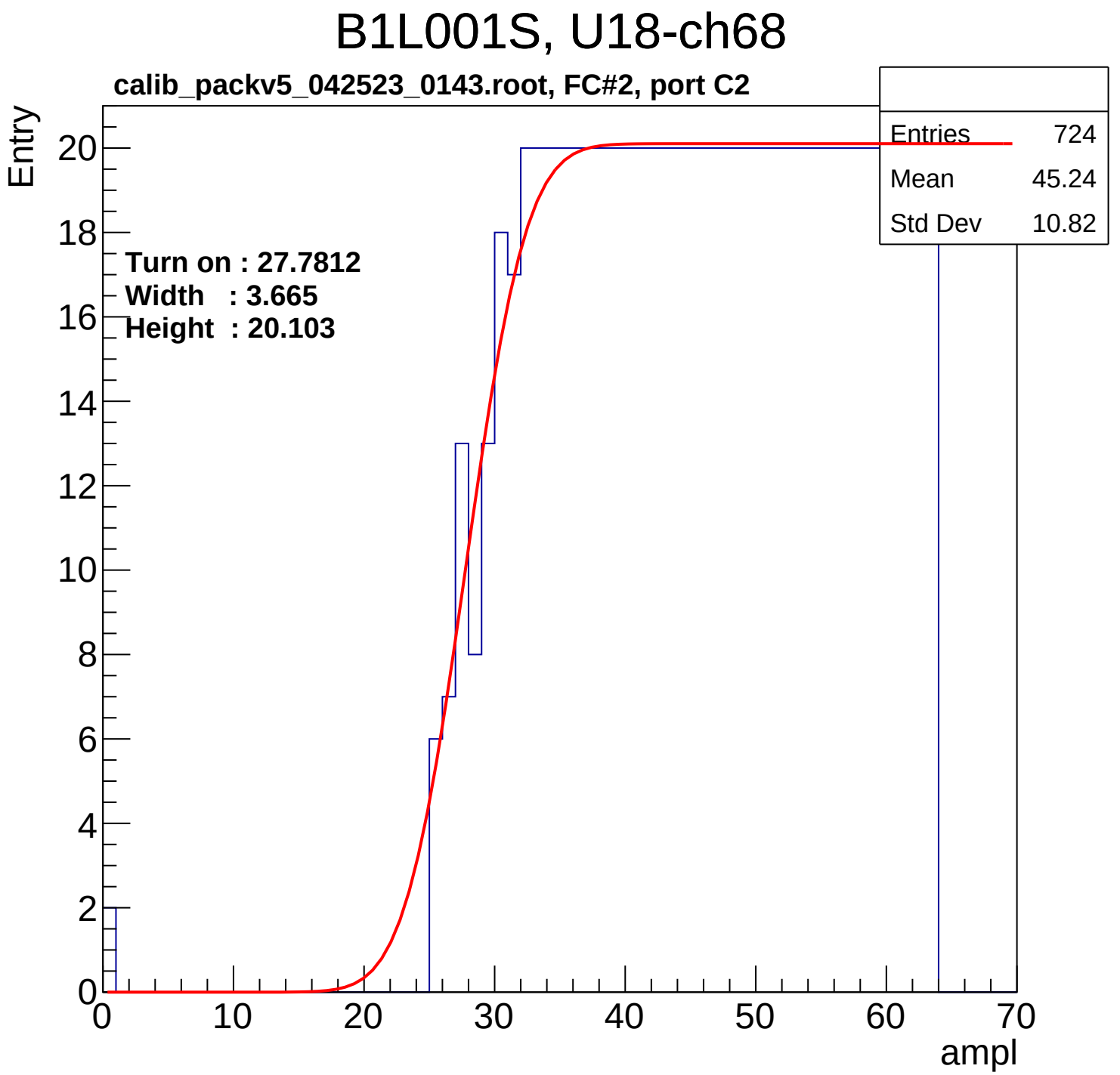
B1L001S, U18-ch68
calib_packv5_042523_0143.root, FC#2, port C2
Entries 724
Mean 45.24
Std Dev 10.82
Turn on : 27.7812
Width : 3.665
Height : 20.103
Entry
ampl
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6
8
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14
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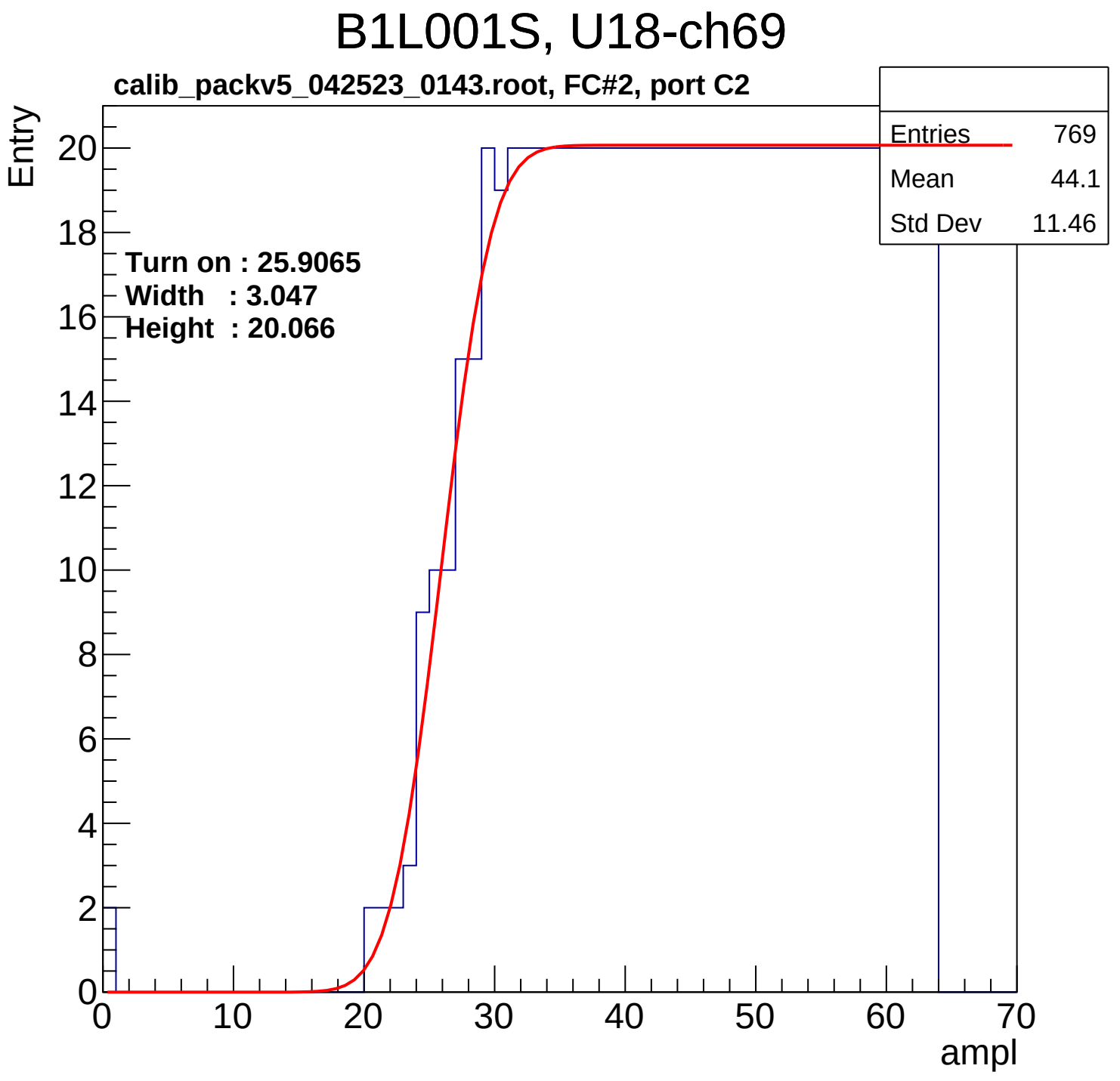
B1L001S, U18-ch69
calib_packv5_042523_0143.root, FC#2, port C2
Entries 769
Mean 44.1
Std Dev 11.46
Turn on : 25.9065
Width : 3.047
Height : 20.066
Entry
ampl
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6
8
10
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0
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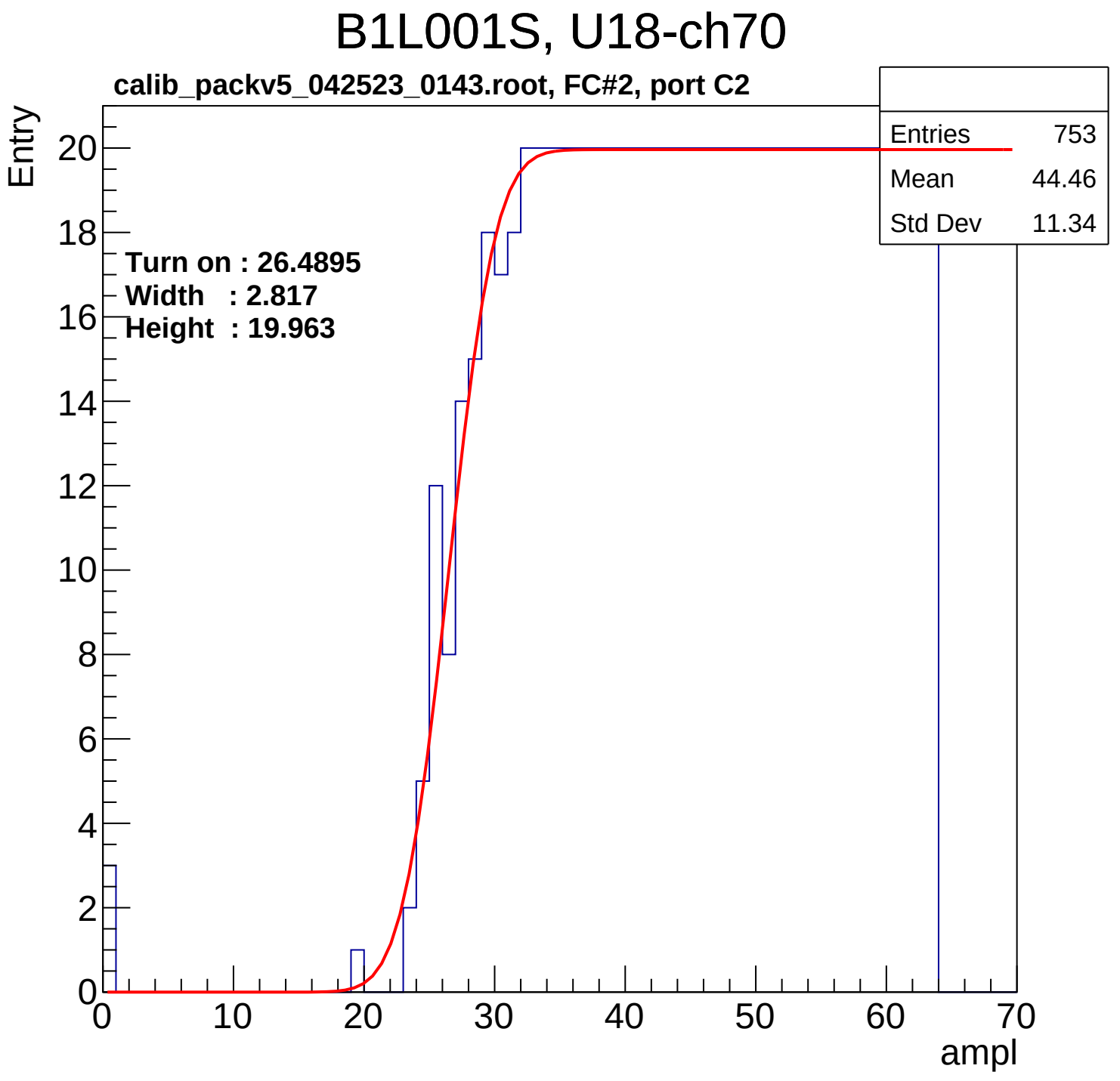
B1L001S, U18-ch70
calib_packv5_042523_0143.root, FC#2, port C2
Entries 753
Mean 44.46
Std Dev 11.34
Turn on : 26.4895
Width : 2.817
Height : 19.963
Entry
ampl
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6
8
10
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14
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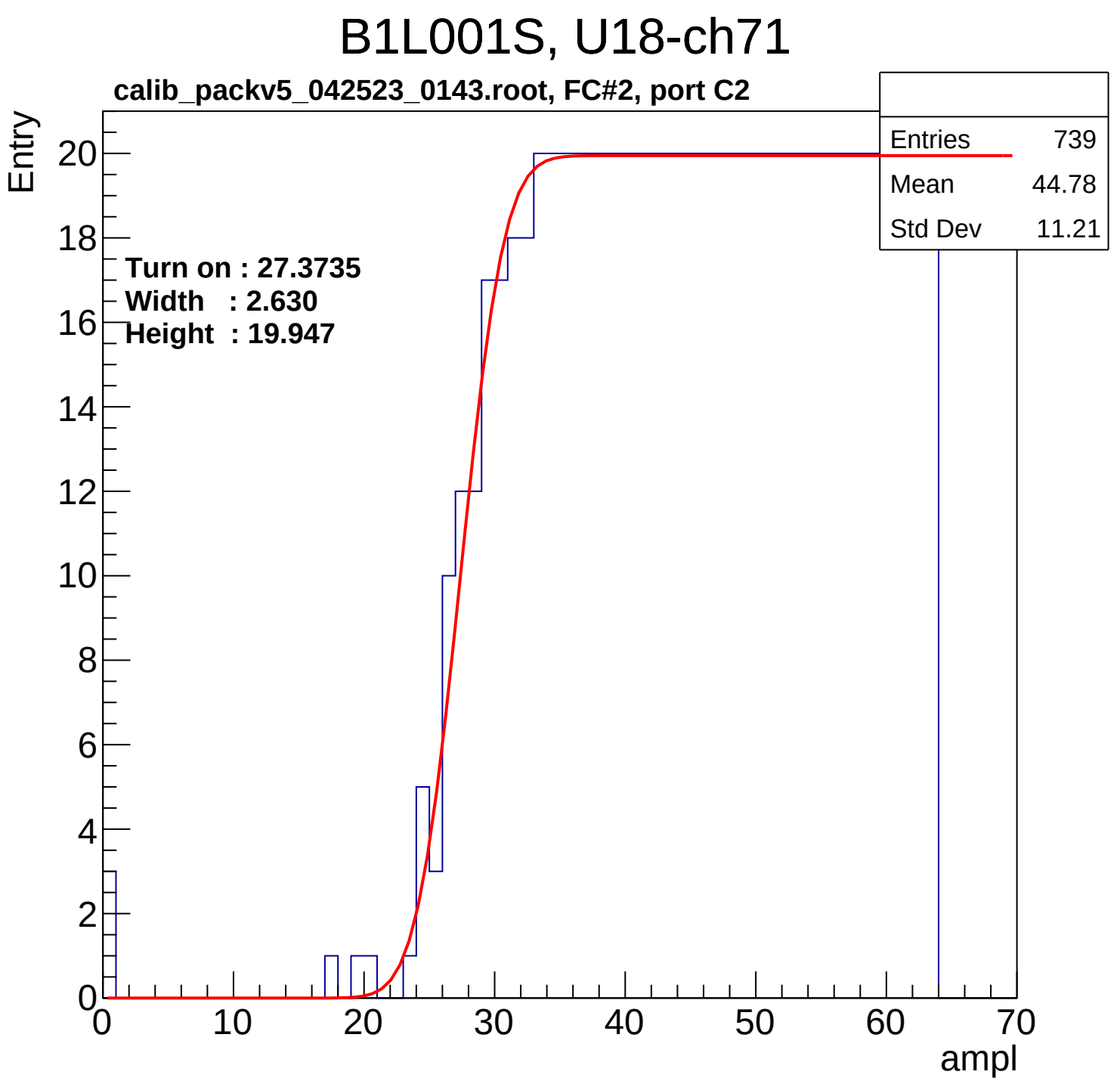
B1L001S, U18-ch71
calib_packv5_042523_0143.root, FC#2, port C2
Entries 739
Mean 44.78
Std Dev 11.21
Turn on : 27.3735
Width : 2.630
Height : 19.947
Entry
ampl
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6
8
10
12
14
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0
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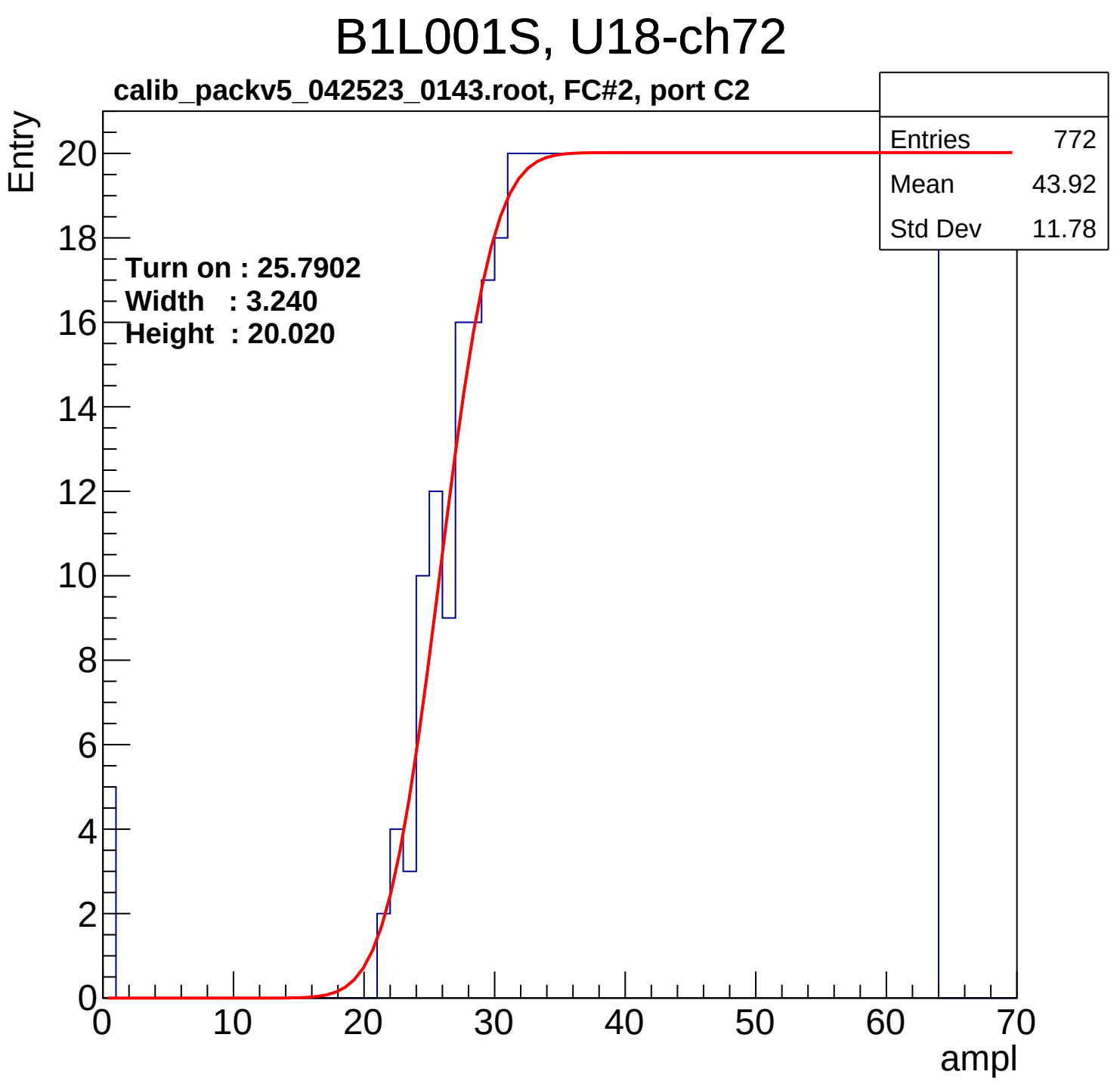
B1L001S, U18-ch72
calib_packv5_042523_0143.root, FC#2, port C2
Entries 772
Mean 43.92
Std Dev 11.78
Turn on : 25.7902
Width : 3.240
Height : 20.020
Entry
ampl
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6
8
10
12
14
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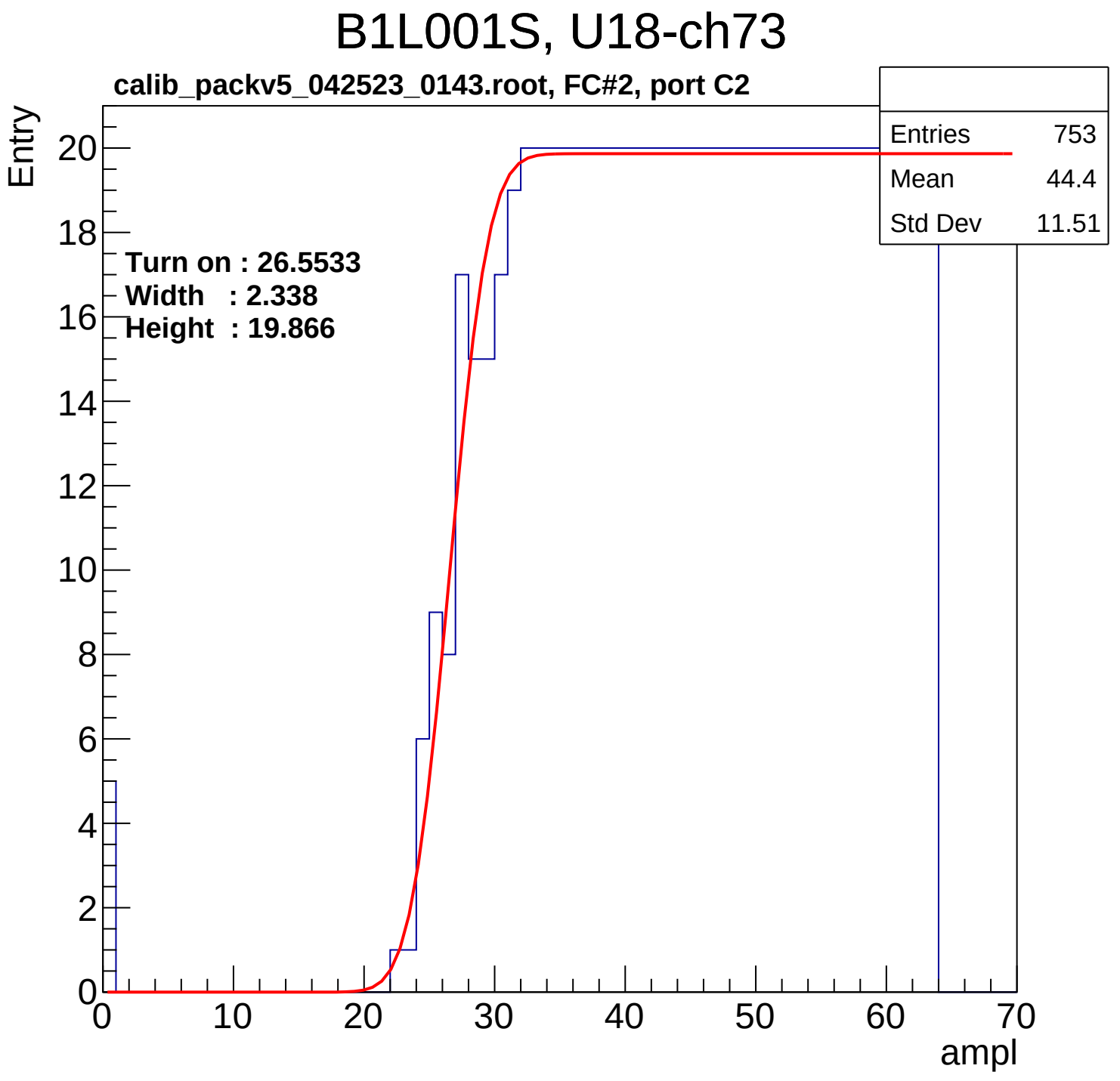
B1L001S, U18-ch73
calib_packv5_042523_0143.root, FC#2, port C2
Entries 753
Mean 44.4
Std Dev 11.51
Turn on : 26.5533
Width : 2.338
Height : 19.866
Entry
ampl
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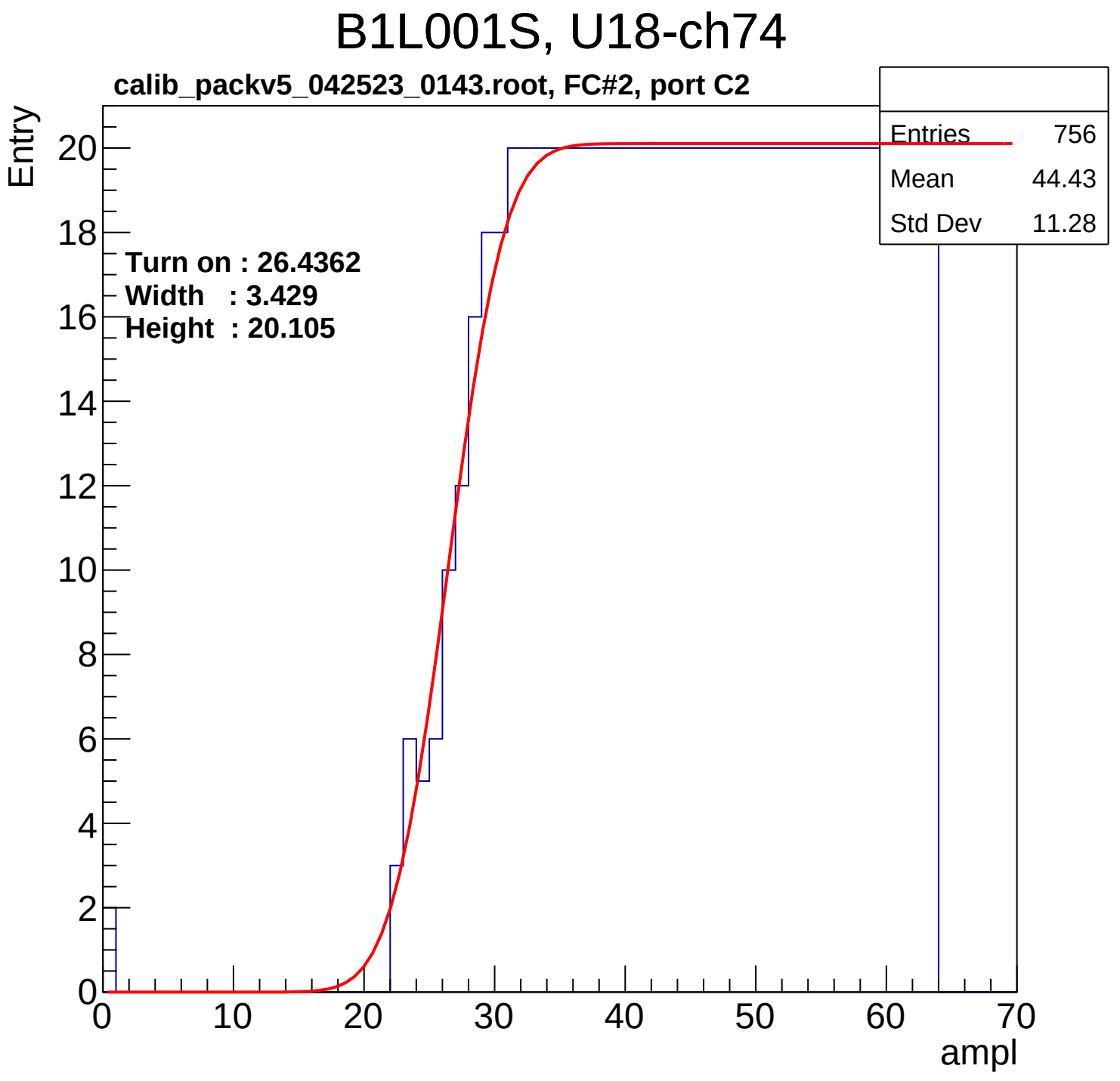
B1L001S, U18-ch74
calib_packv5_042523_0143.root, FC#2, port C2
Entries 756
Mean 44.43
Std Dev 11.28
Turn on : 26.4362
Width : 3.429
Height : 20.105
Entry
ampl
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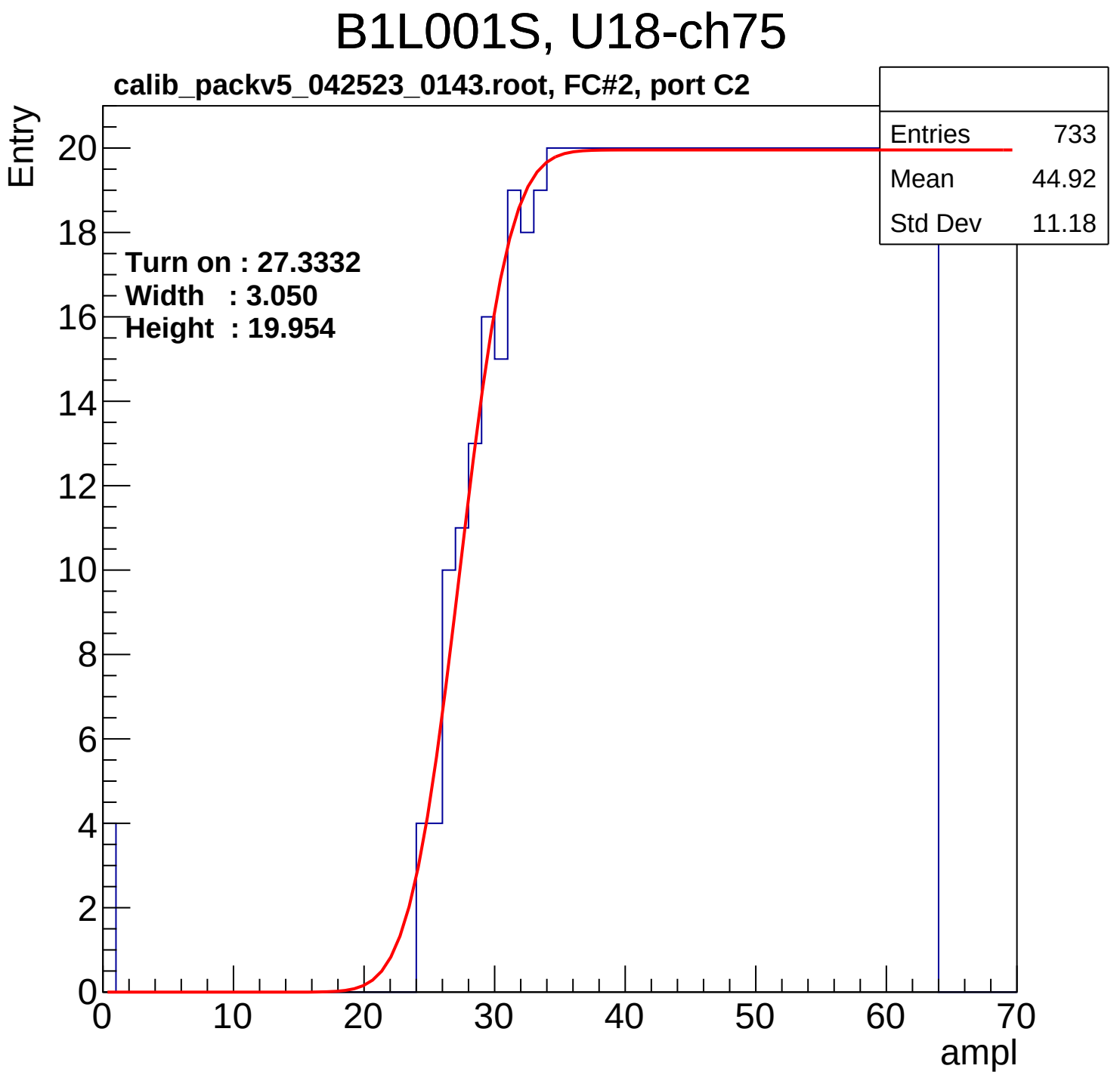
B1L001S, U18-ch75
calib_packv5_042523_0143.root, FC#2, port C2
Entries 733
Mean 44.92
Std Dev 11.18
Turn on : 27.3332
Width : 3.050
Height : 19.954
Entry
ampl
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6
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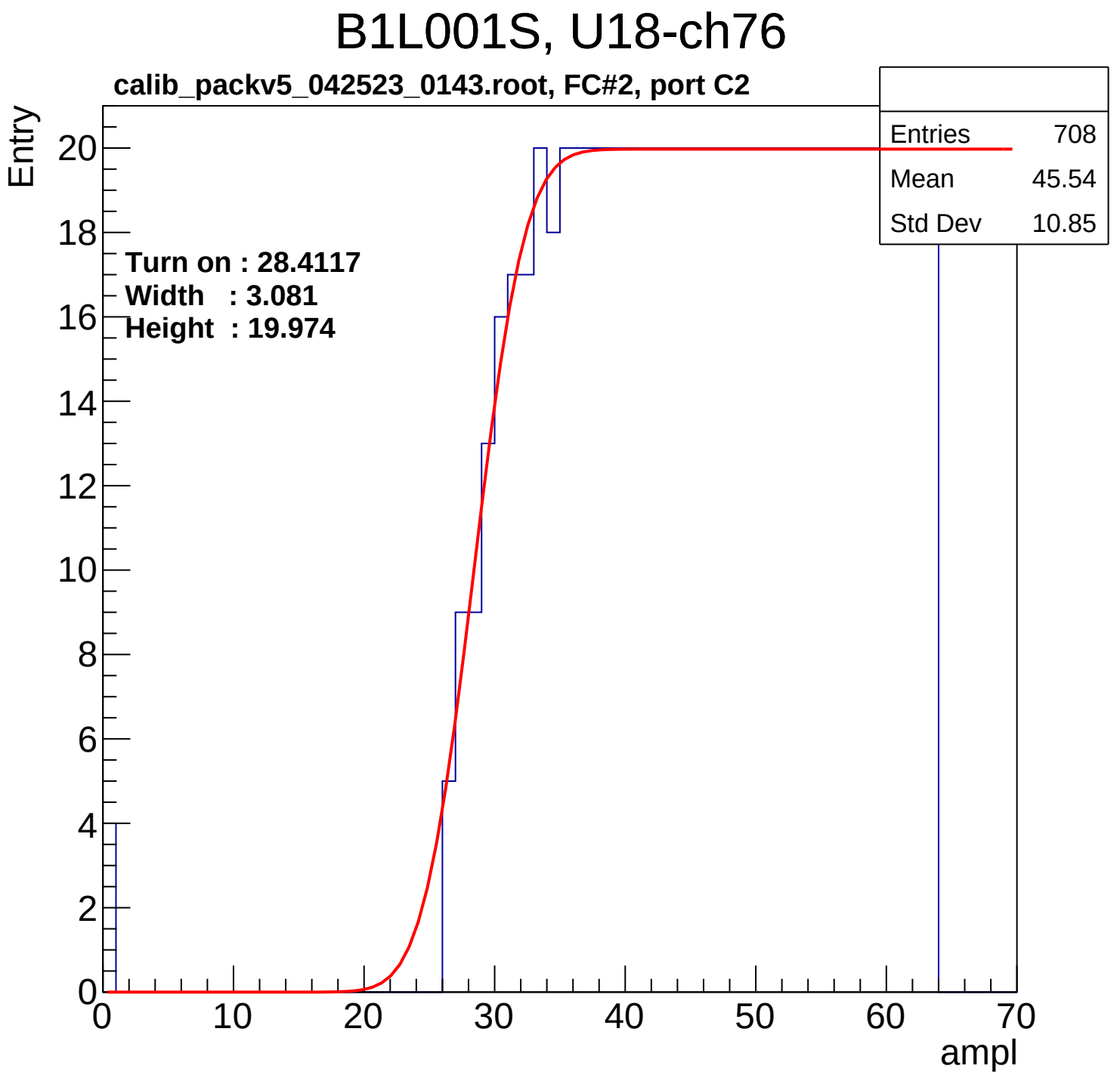
B1L001S, U18-ch76
calib_packv5_042523_0143.root, FC#2, port C2
Entries 708
Mean 45.54
Std Dev 10.85
Turn on : 28.4117
Width : 3.081
Height : 19.974
Entry
ampl
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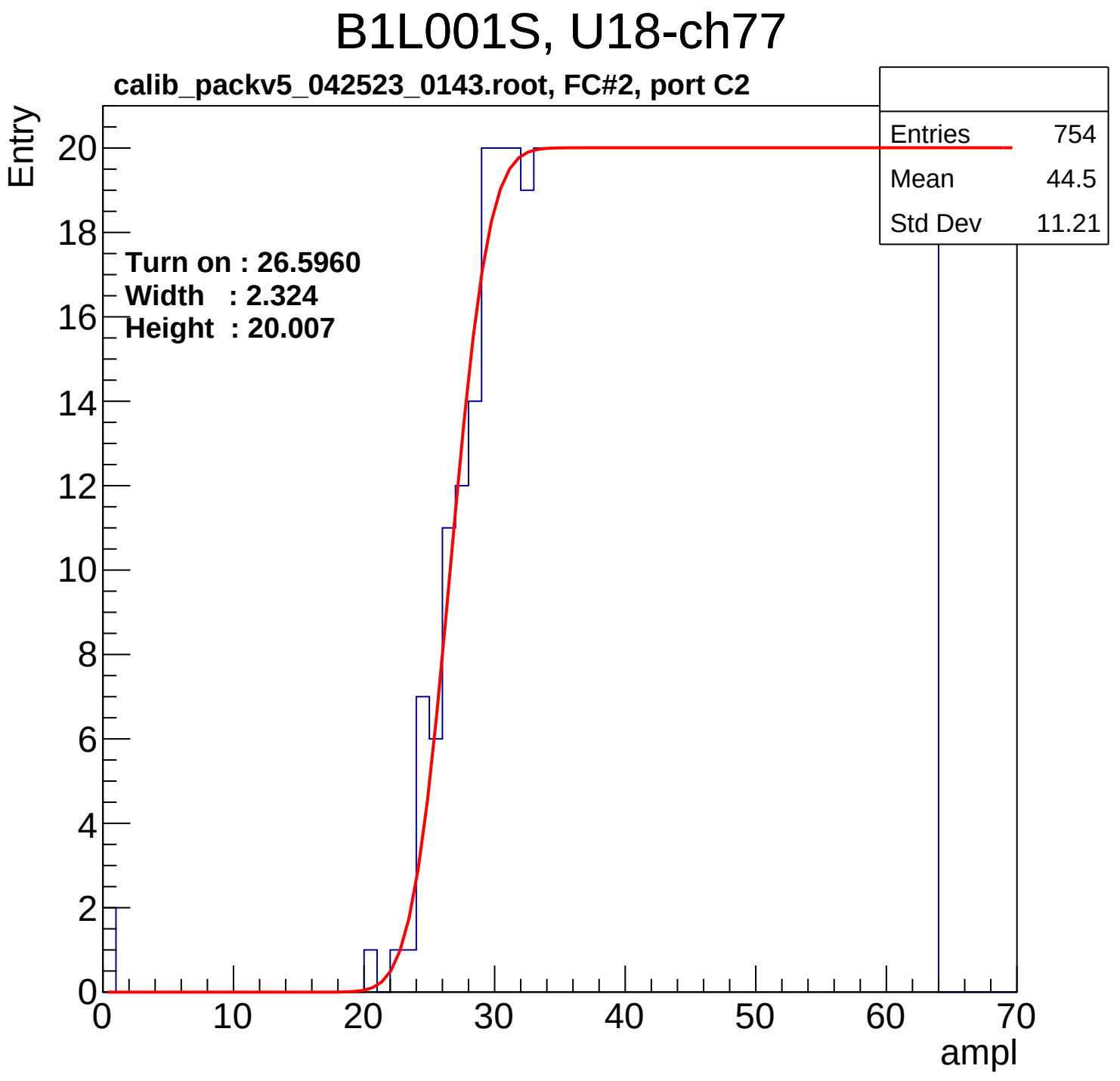
B1L001S, U18-ch77
calib_packv5_042523_0143.root, FC#2, port C2
Entries 754
Mean 44.5
Std Dev 11.21
Turn on : 26.5960
Width : 2.324
Height : 20.007
Entry
ampl
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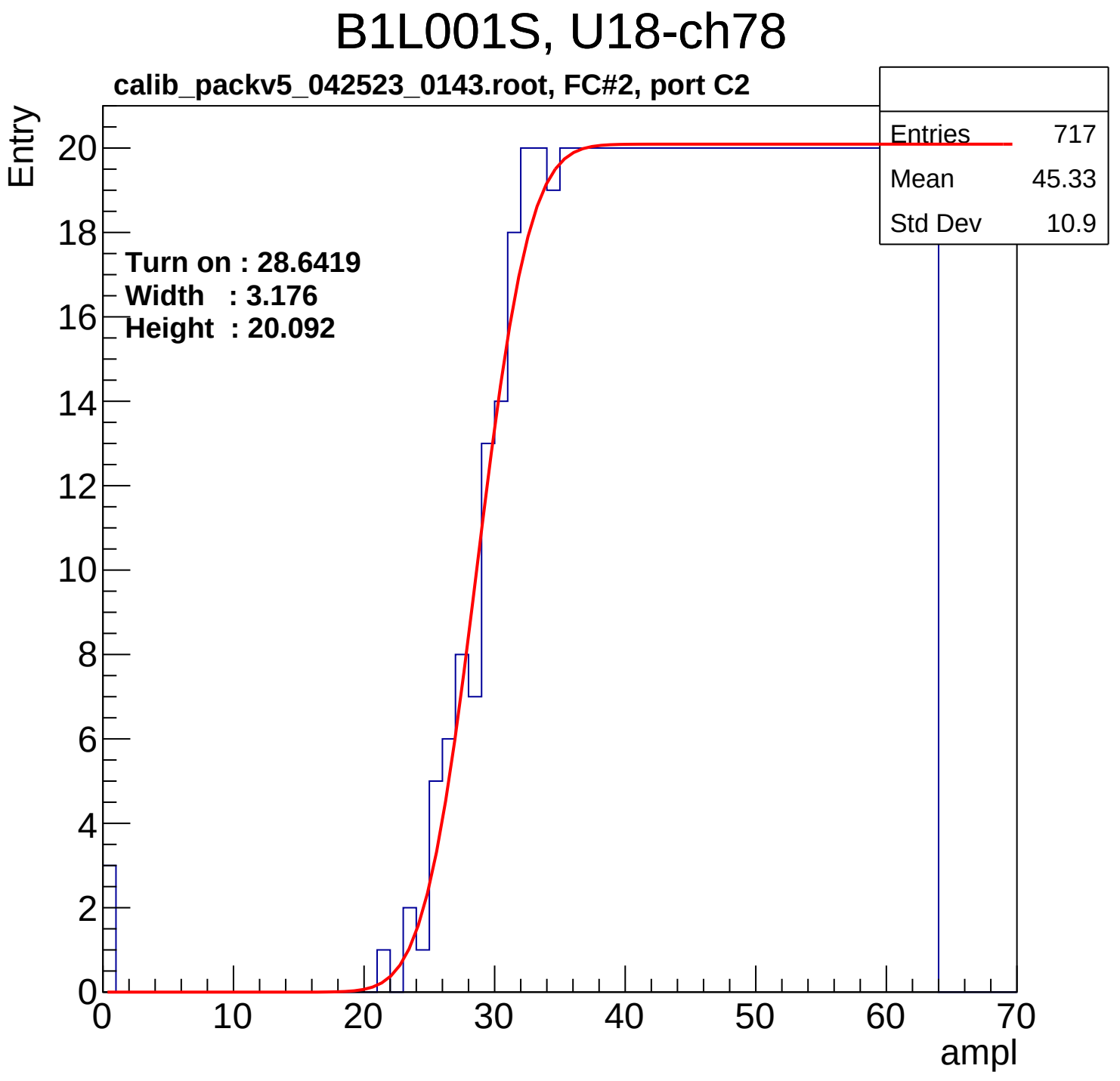
B1L001S, U18-ch78
calib_packv5_042523_0143.root, FC#2, port C2
Entries 717
Mean 45.33
Std Dev 10.9
Turn on : 28.6419
Width : 3.176
Height : 20.092
Entry
ampl
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6
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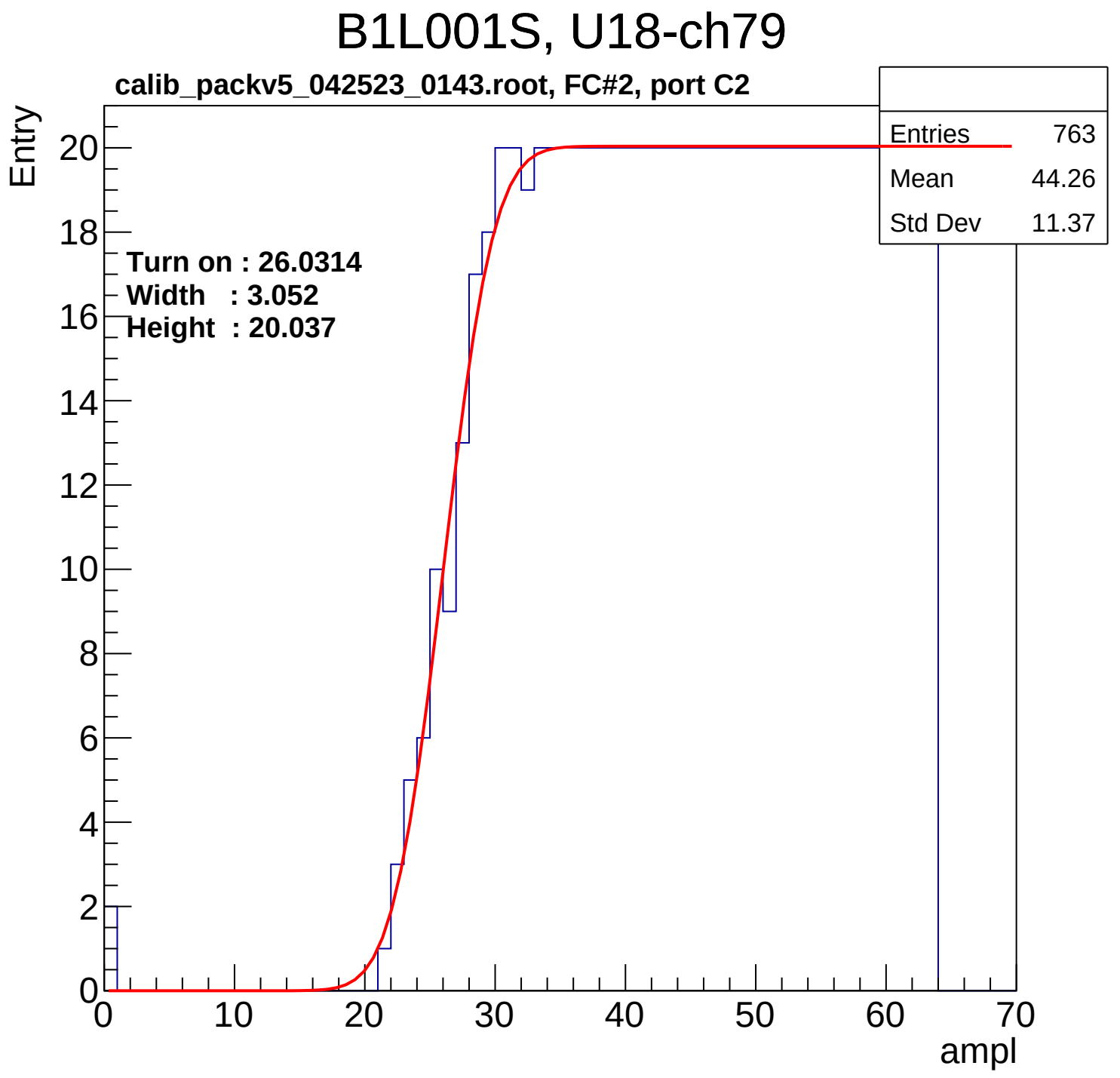
B1L001S, U18-ch79
calib_packv5_042523_0143.root, FC#2, port C2
Entries 763
Mean 44.26
Std Dev 11.37
Turn on : 26.0314
Width : 3.052
Height : 20.037
Entry
ampl
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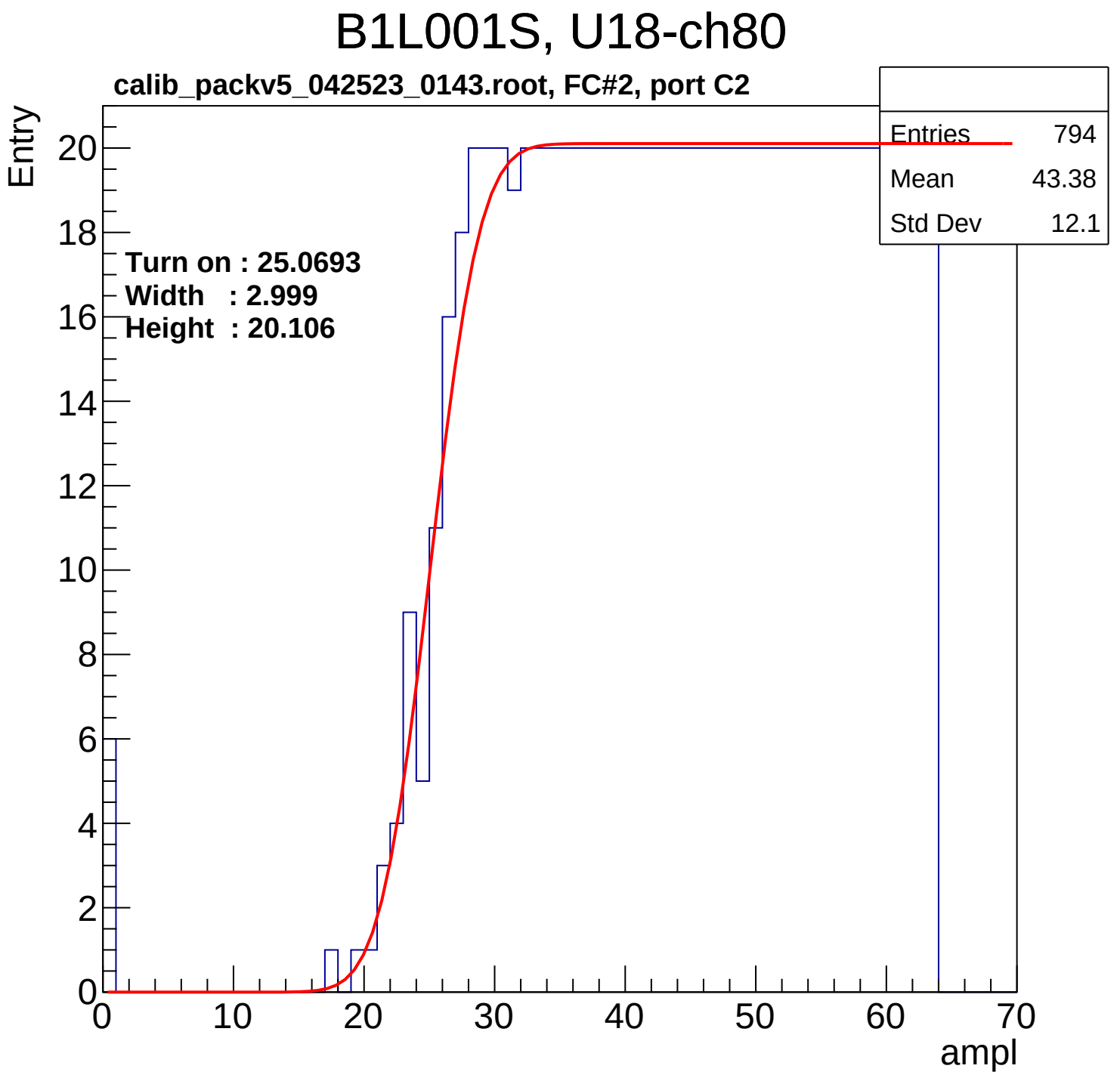
B1L001S, U18-ch80
calib_packv5_042523_0143.root, FC#2, port C2
Entries 794
Mean 43.38
Std Dev 12.1
Turn on : 25.0693
Width : 2.999
Height : 20.106
Entry
ampl
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6
8
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14
16
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0
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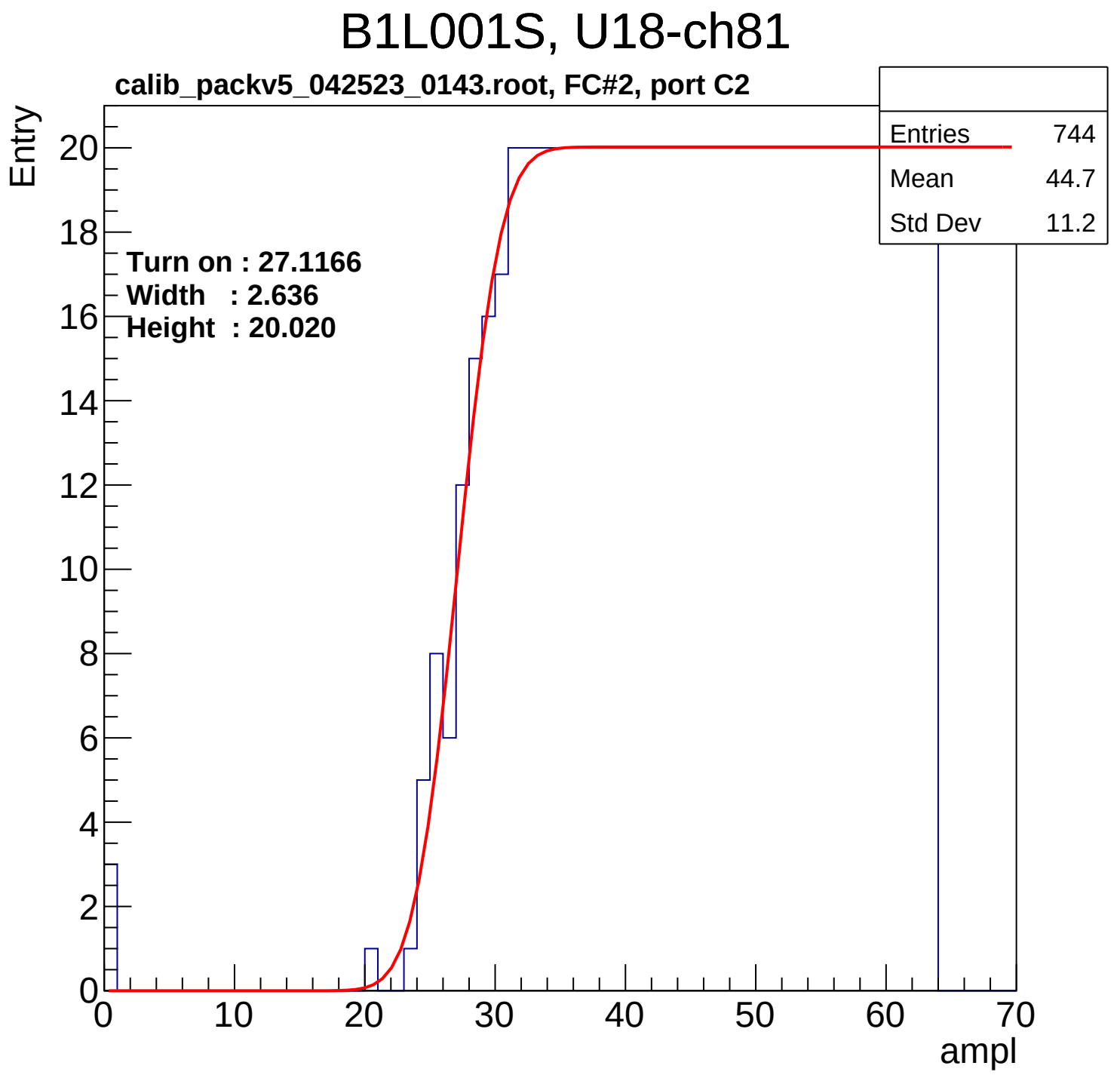
B1L001S, U18-ch81
calib_packv5_042523_0143.root, FC#2, port C2
Entries 744
Mean 44.7
Std Dev 11.2
Turn on : 27.1166
Width : 2.636
Height : 20.020
Entry
ampl
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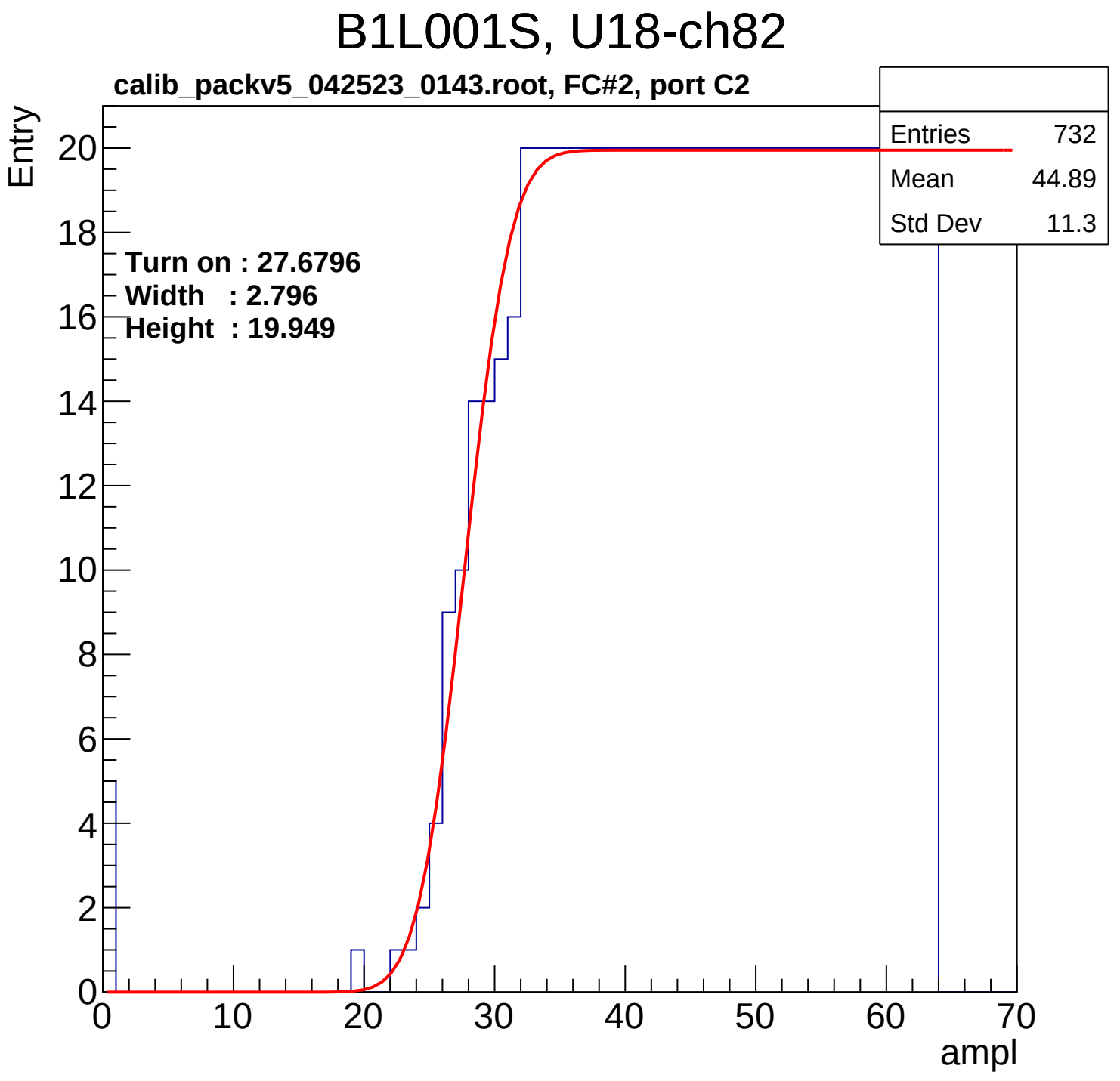
B1L001S, U18-ch82
calib_packv5_042523_0143.root, FC#2, port C2
Entries 732
Mean 44.89
Std Dev 11.3
Turn on : 27.6796
Width : 2.796
Height : 19.949
Entry
ampl
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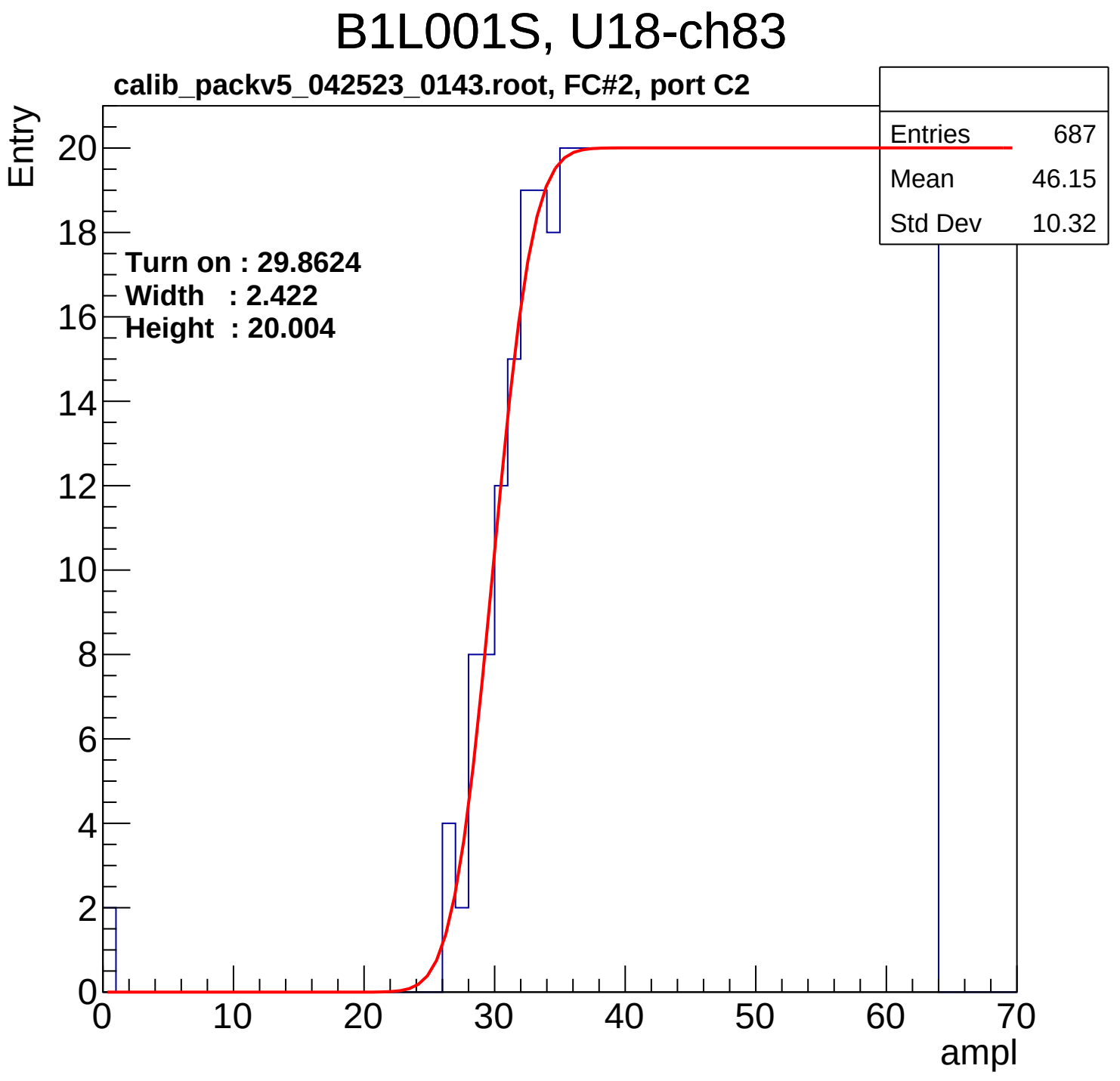
B1L001S, U18-ch83
calib_packv5_042523_0143.root, FC#2, port C2
Entries 687
Mean 46.15
Std Dev 10.32
Turn on : 29.8624
Width : 2.422
Height : 20.004
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
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10
20
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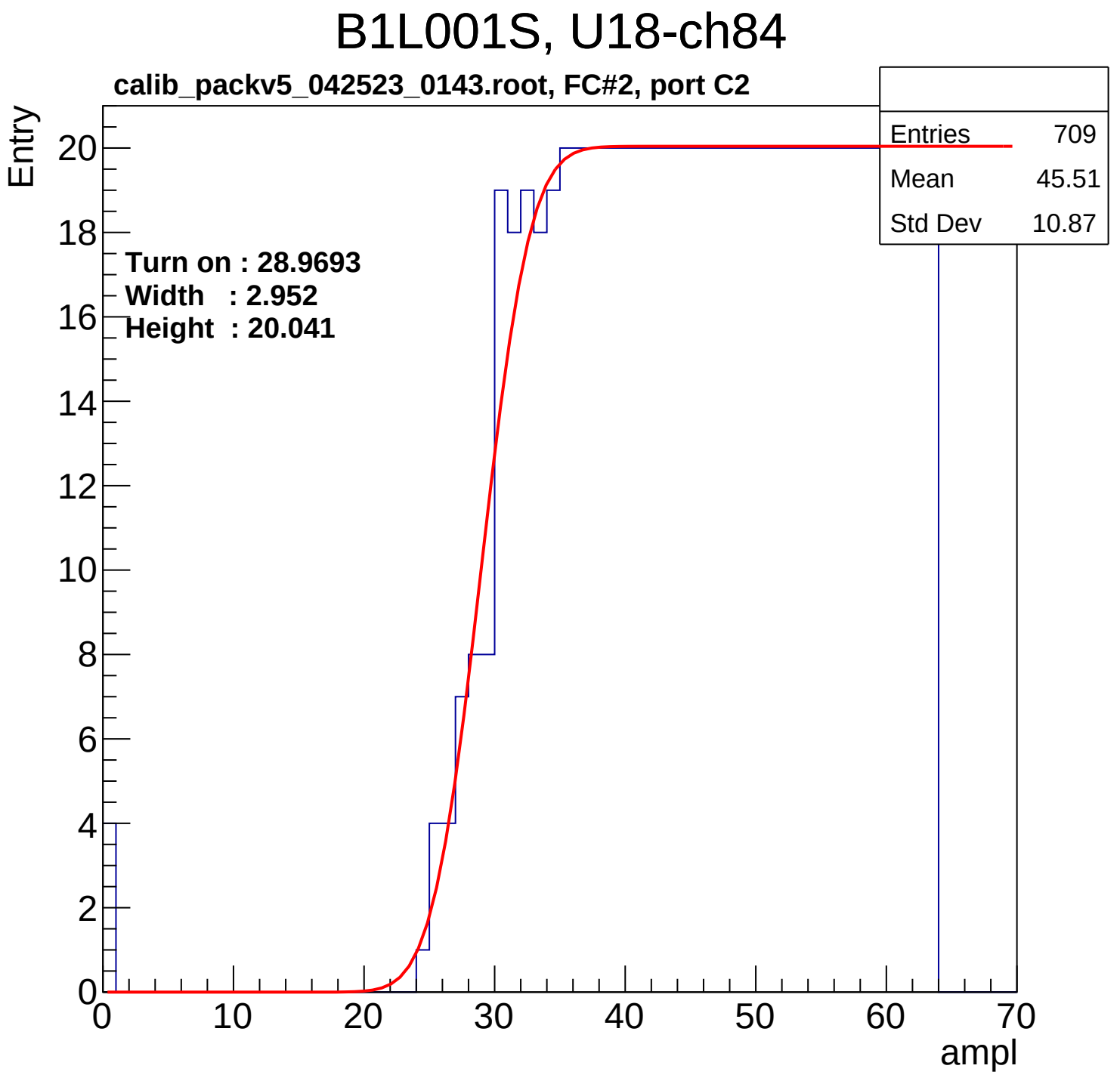
B1L001S, U18-ch84
calib_packv5_042523_0143.root, FC#2, port C2
Entries 709
Mean 45.51
Std Dev 10.87
Turn on : 28.9693
Width : 2.952
Height : 20.041
Entry
ampl
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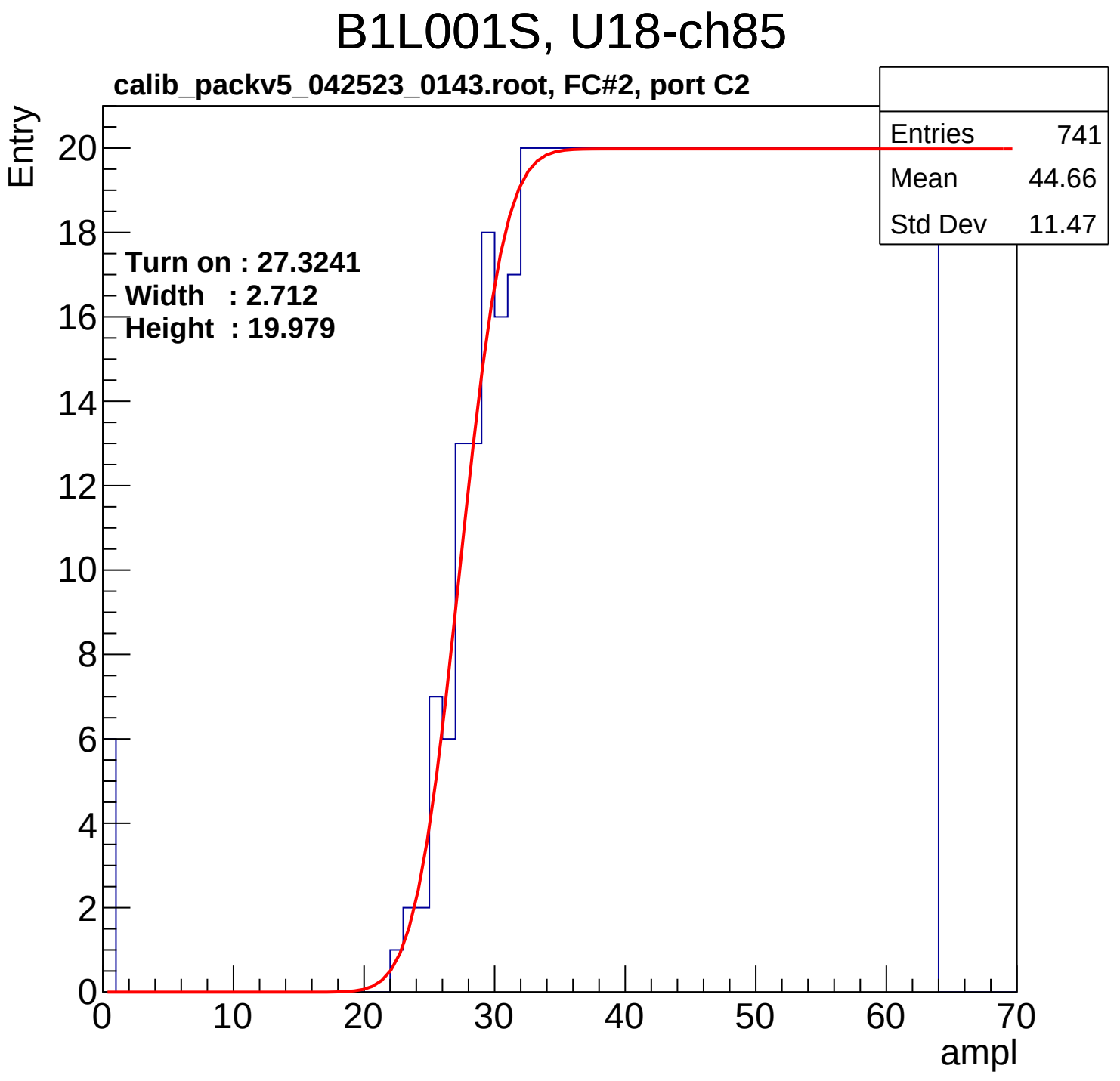
B1L001S, U18-ch85
calib_packv5_042523_0143.root, FC#2, port C2
Entries 741
Mean 44.66
Std Dev 11.47
Turn on : 27.3241
Width : 2.712
Height : 19.979
Entry
ampl
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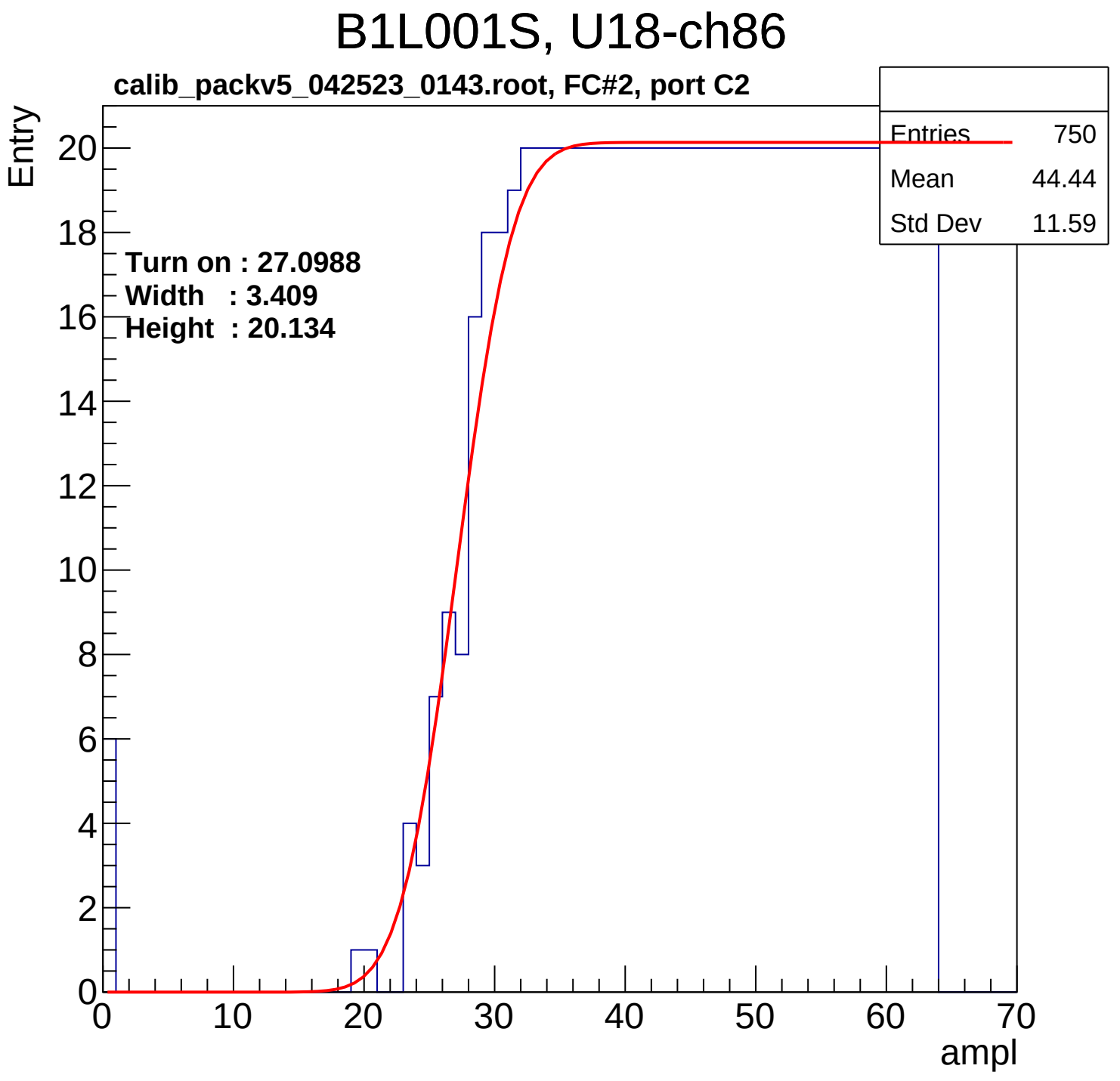
B1L001S, U18-ch86
calib_packv5_042523_0143.root, FC#2, port C2
Entries 750
Mean 44.44
Std Dev 11.59
Turn on : 27.0988
Width : 3.409
Height : 20.134
Entry
ampl
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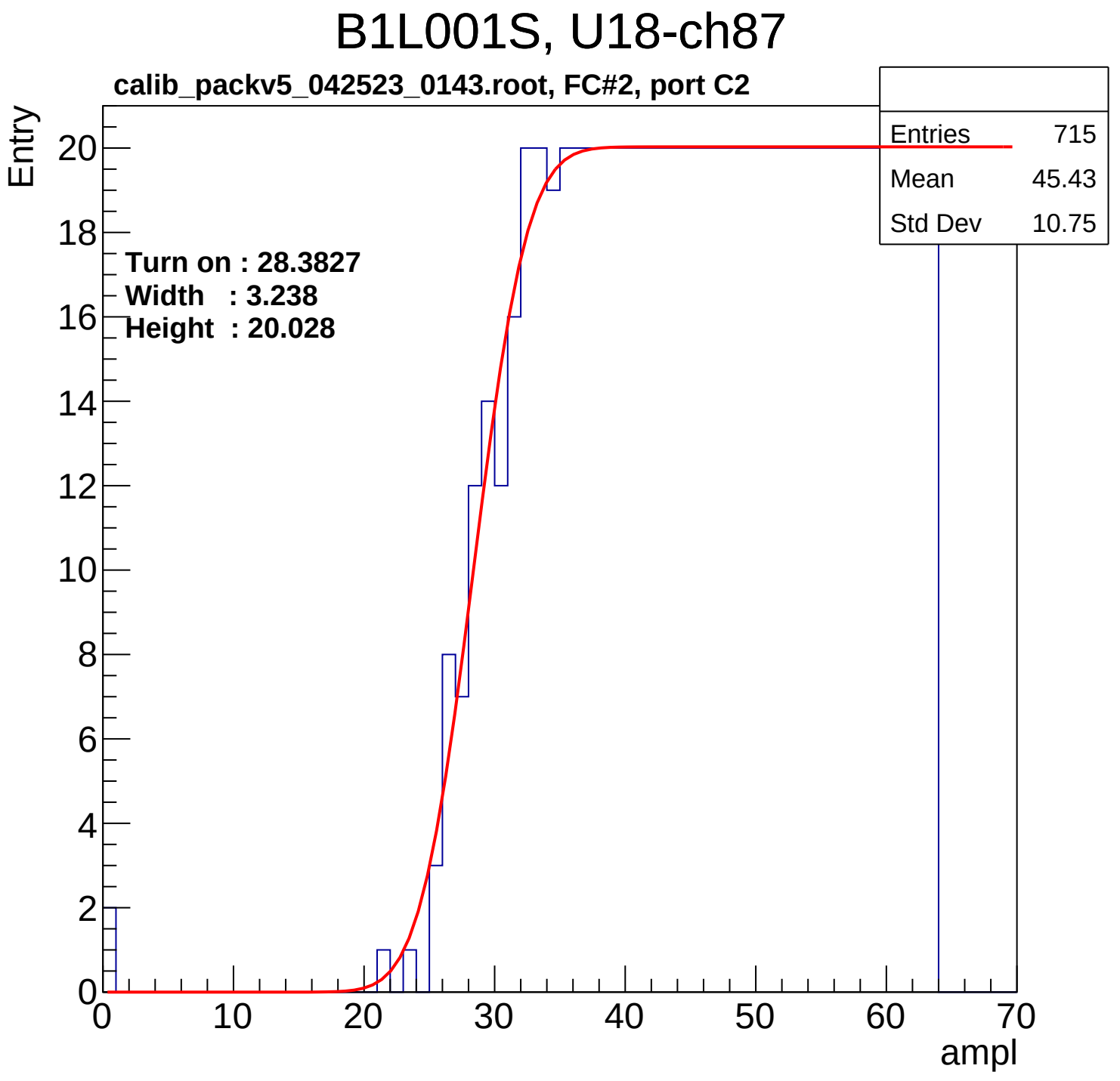
B1L001S, U18-ch87
calib_packv5_042523_0143.root, FC#2, port C2
Entries 715
Mean 45.43
Std Dev 10.75
Turn on : 28.3827
Width : 3.238
Height : 20.028
Entry
ampl
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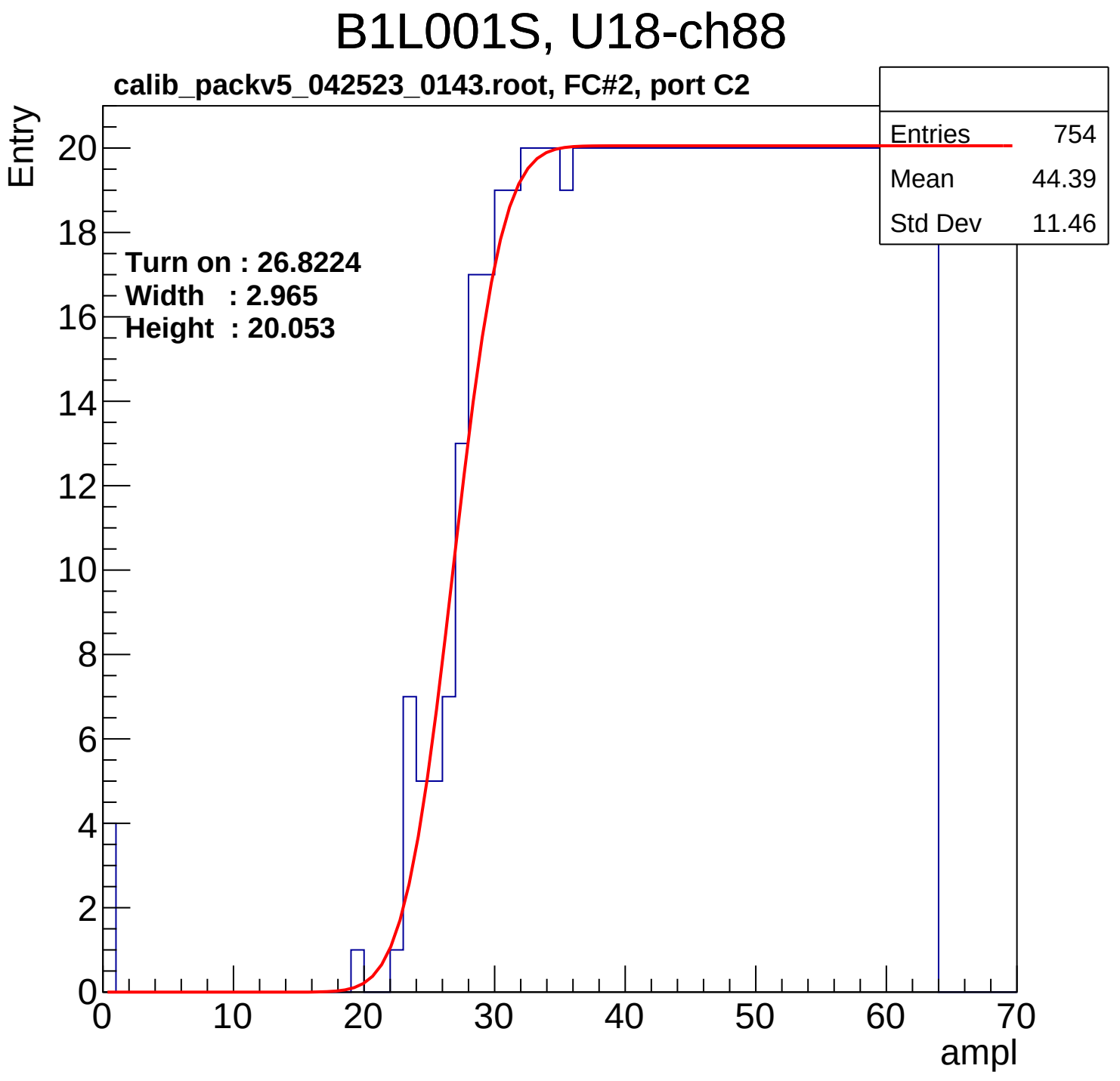
B1L001S, U18-ch88
calib_packv5_042523_0143.root, FC#2, port C2
Entries 754
Mean 44.39
Std Dev 11.46
Turn on : 26.8224
Width : 2.965
Height : 20.053
Entry
ampl
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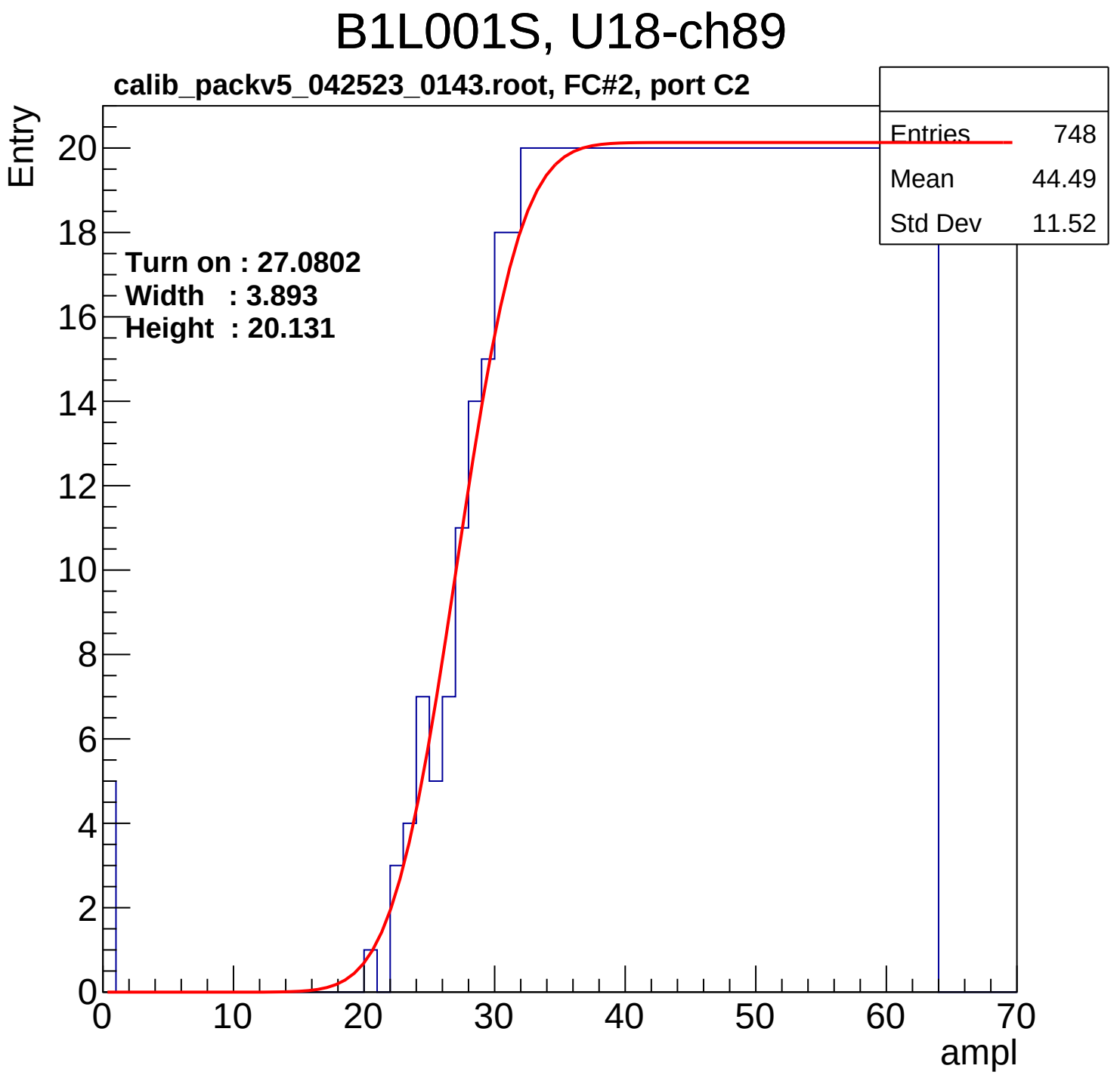
B1L001S, U18-ch89
calib_packv5_042523_0143.root, FC#2, port C2
Entries 748
Mean 44.49
Std Dev 11.52
Turn on : 27.0802
Width : 3.893
Height : 20.131
Entry
ampl
0
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6
8
10
12
14
16
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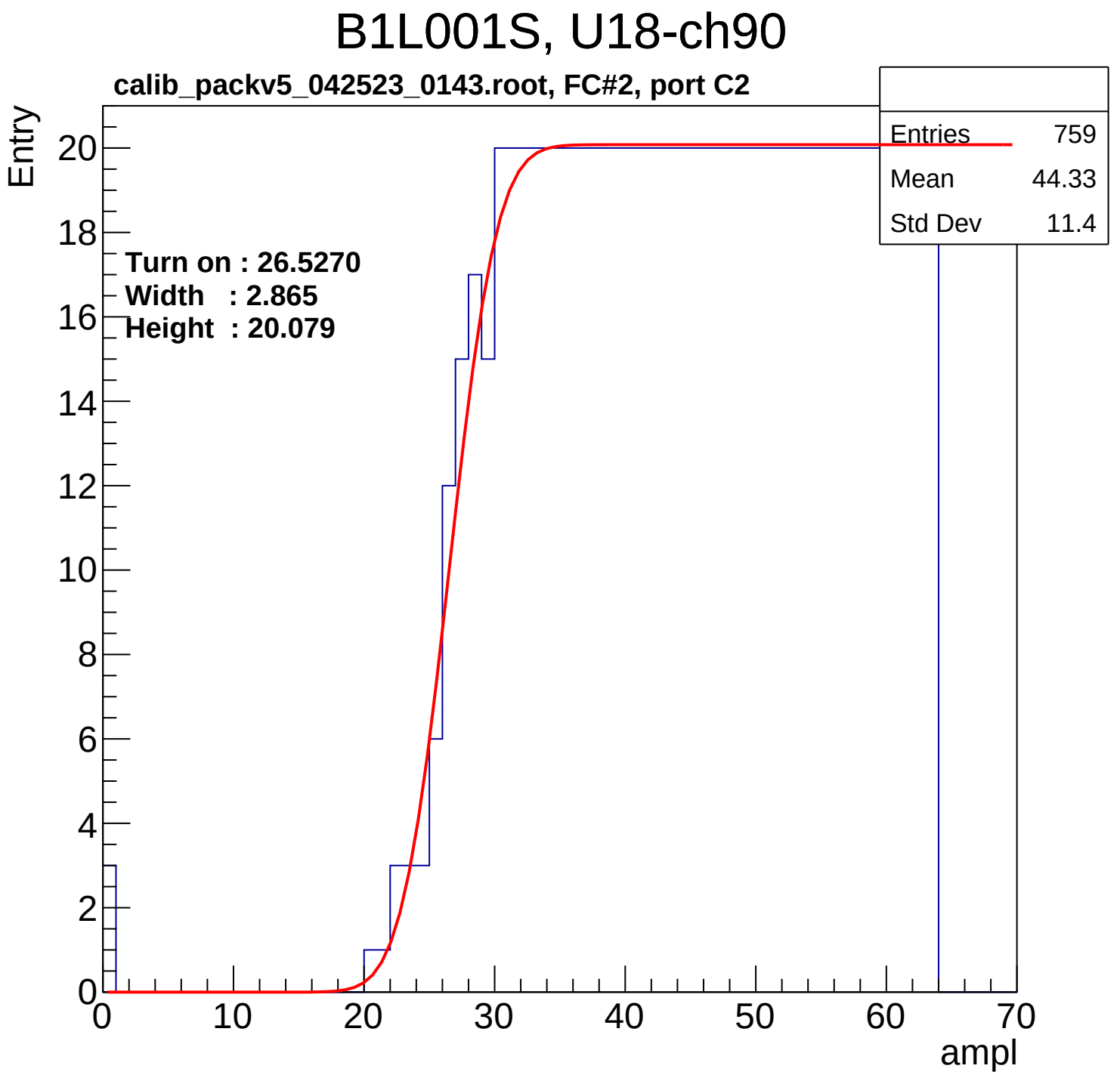
B1L001S, U18-ch90
calib_packv5_042523_0143.root, FC#2, port C2
Entries 759
Mean 44.33
Std Dev 11.4
Turn on : 26.5270
Width : 2.865
Height : 20.079
Entry
ampl
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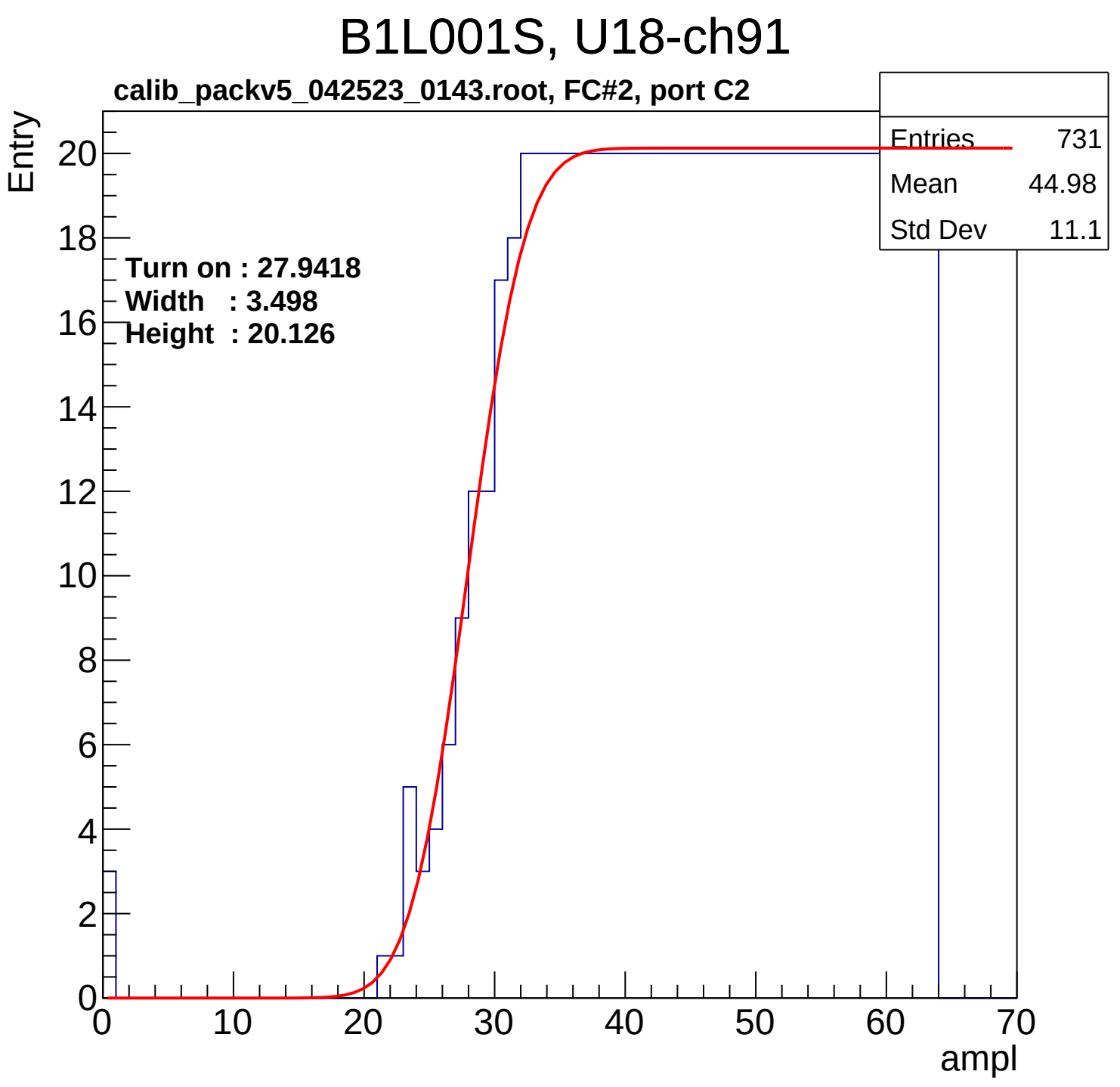
B1L001S, U18-ch91
calib_packv5_042523_0143.root, FC#2, port C2
Entries 731
Mean 44.98
Std Dev 11.1
Turn on : 27.9418
Width : 3.498
Height : 20.126
Entry
ampl
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6
8
10
12
14
16
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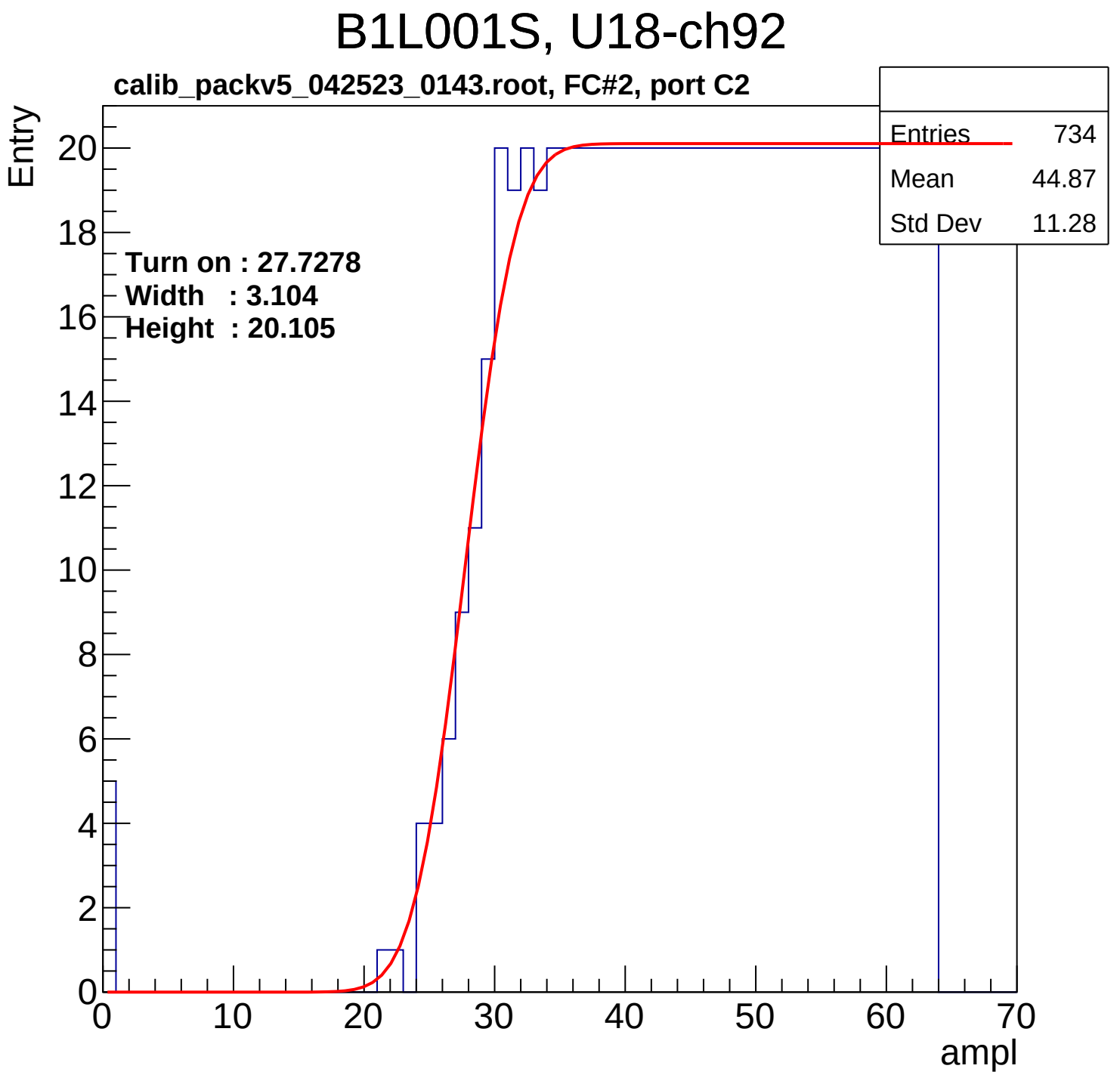
B1L001S, U18-ch92
calib_packv5_042523_0143.root, FC#2, port C2
Entries 734
Mean 44.87
Std Dev 11.28
Turn on : 27.7278
Width : 3.104
Height : 20.105
Entry
ampl
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6
8
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14
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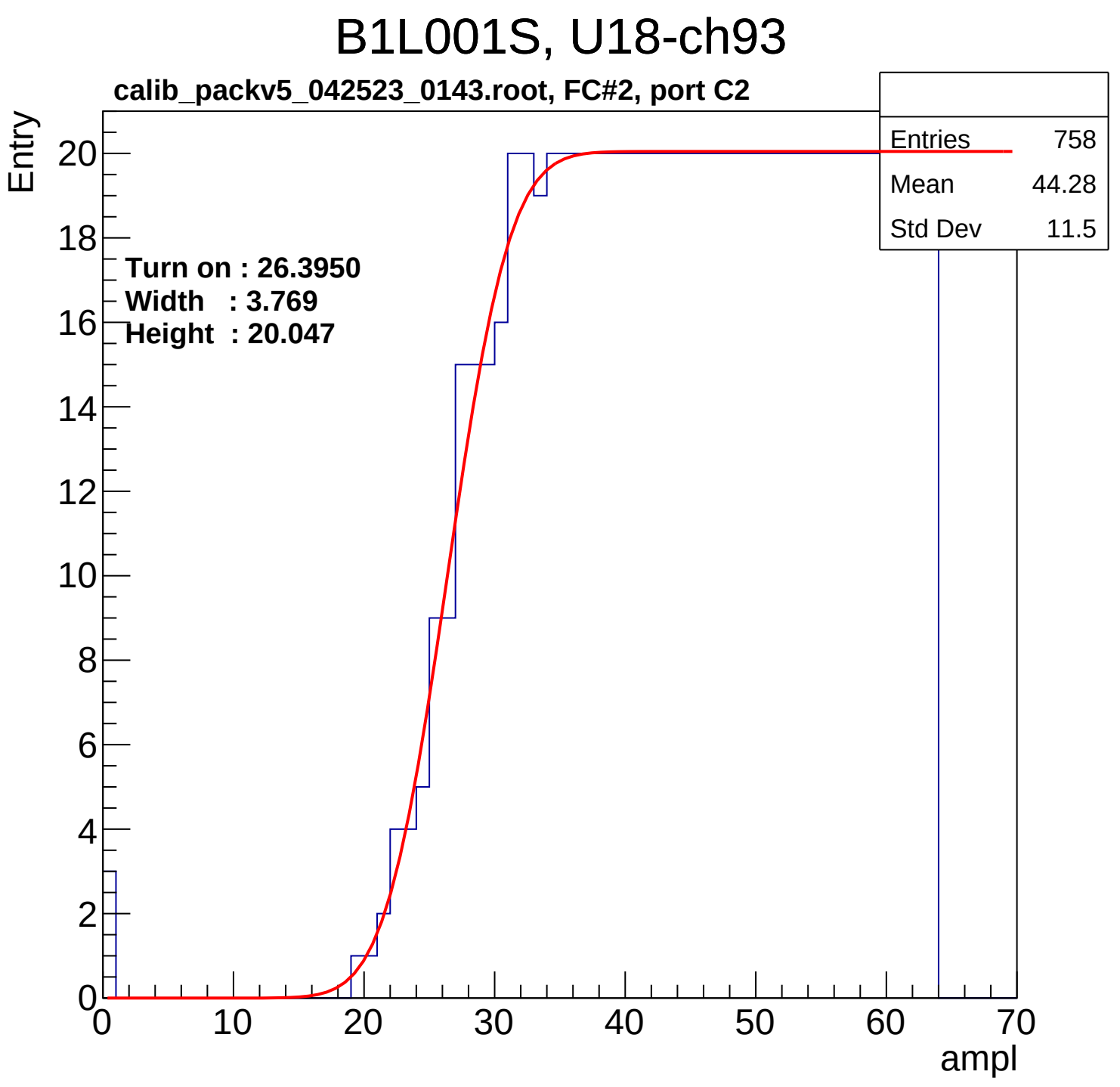
B1L001S, U18-ch93
calib_packv5_042523_0143.root, FC#2, port C2
Entries 758
Mean 44.28
Std Dev 11.5
Turn on : 26.3950
Width : 3.769
Height : 20.047
Entry
ampl
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6
8
10
12
14
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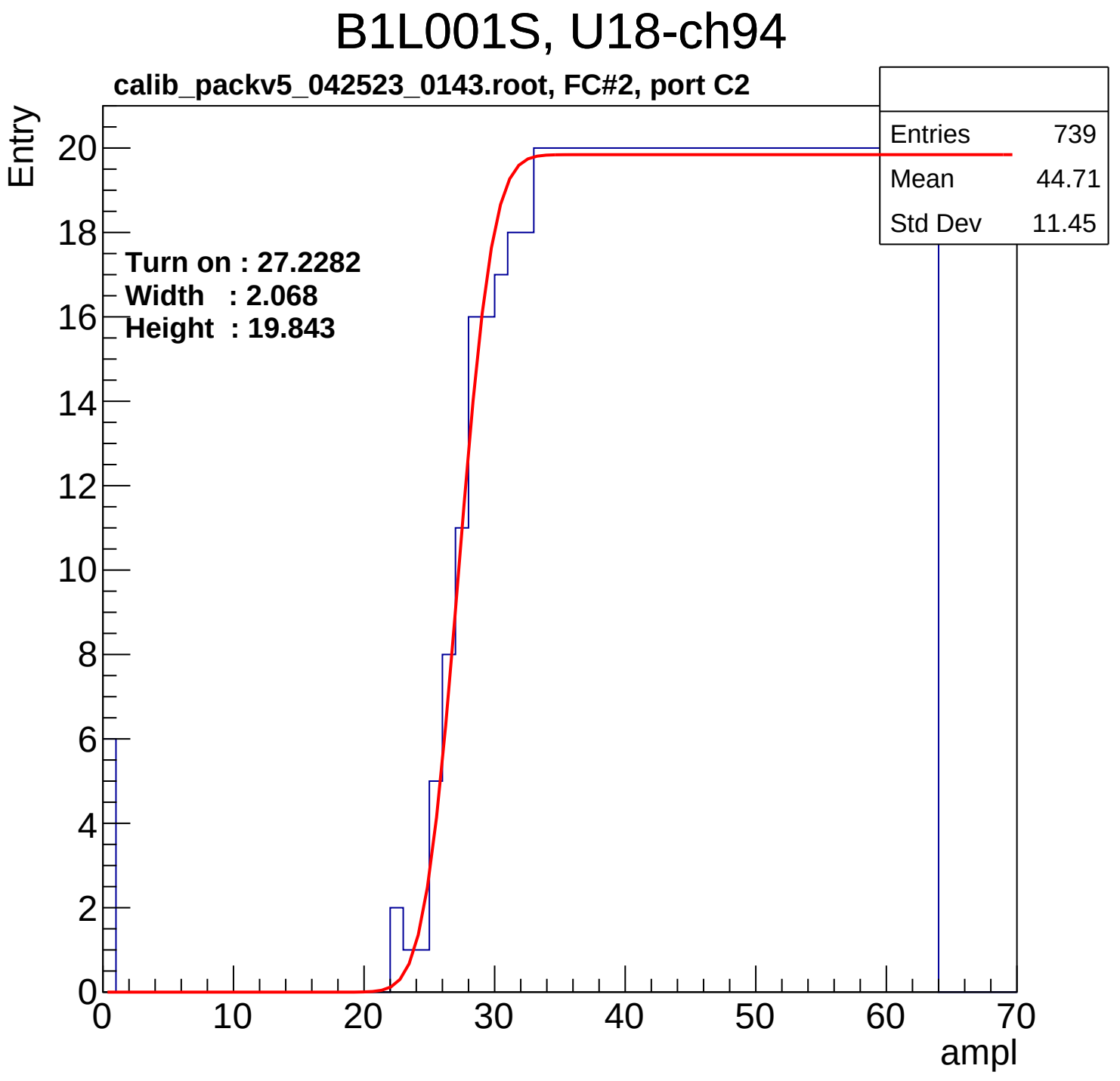
B1L001S, U18-ch94
calib_packv5_042523_0143.root, FC#2, port C2
Entries 739
Mean 44.71
Std Dev 11.45
Turn on : 27.2282
Width : 2.068
Height : 19.843
Entry
ampl
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2
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6
8
10
12
14
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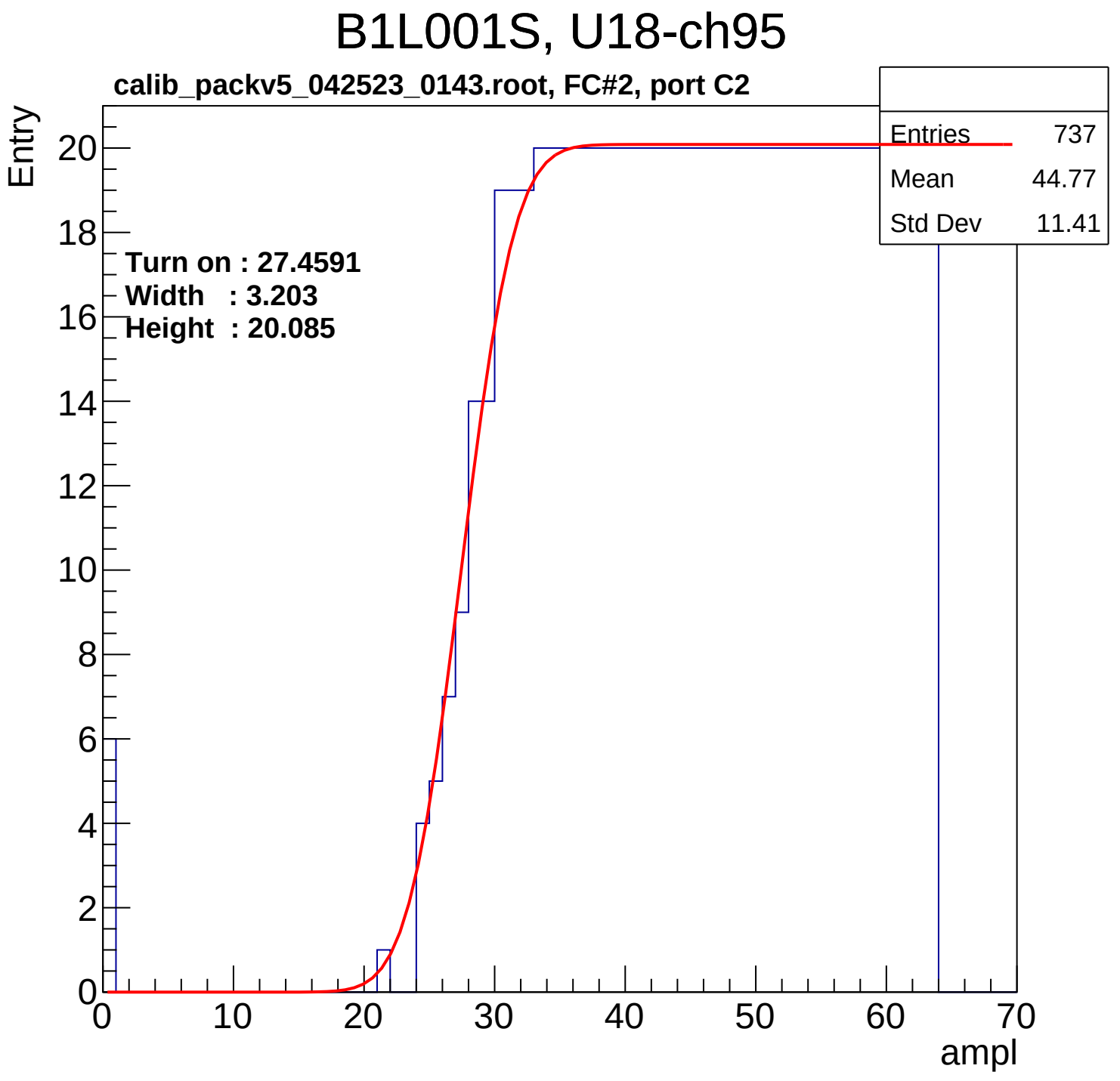
B1L001S, U18-ch95
calib_packv5_042523_0143.root, FC#2, port C2
Entries 737
Mean 44.77
Std Dev 11.41
Turn on : 27.4591
Width : 3.203
Height : 20.085
Entry
ampl
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6
8
10
12
14
16
18
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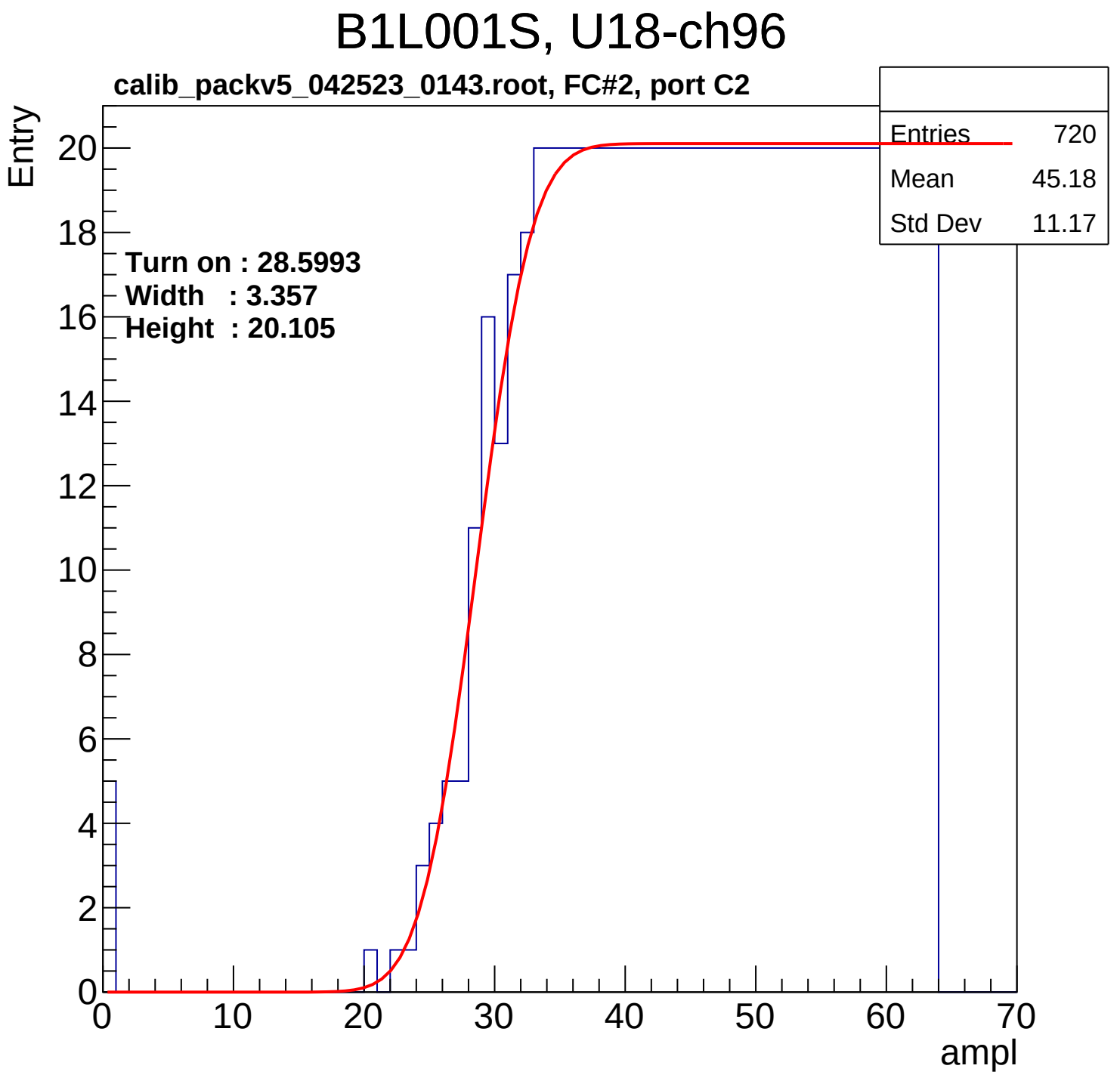
B1L001S, U18-ch96
calib_packv5_042523_0143.root, FC#2, port C2
Entries 720
Mean 45.18
Std Dev 11.17
Turn on : 28.5993
Width : 3.357
Height : 20.105
Entry
ampl
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6
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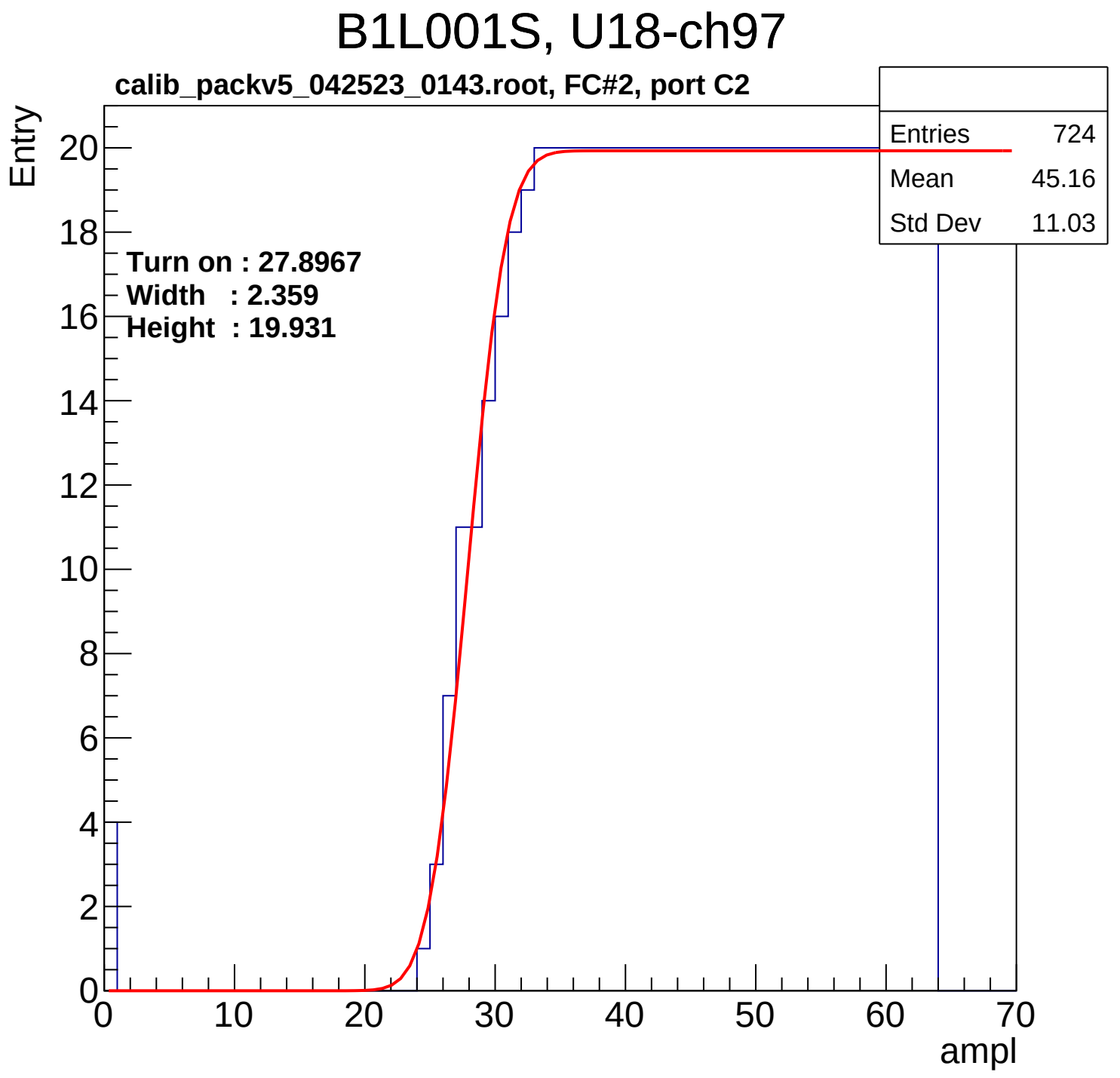
B1L001S, U18-ch97
calib_packv5_042523_0143.root, FC#2, port C2
Entries 724
Mean 45.16
Std Dev 11.03
Turn on : 27.8967
Width : 2.359
Height : 19.931
Entry
ampl
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6
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10
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0
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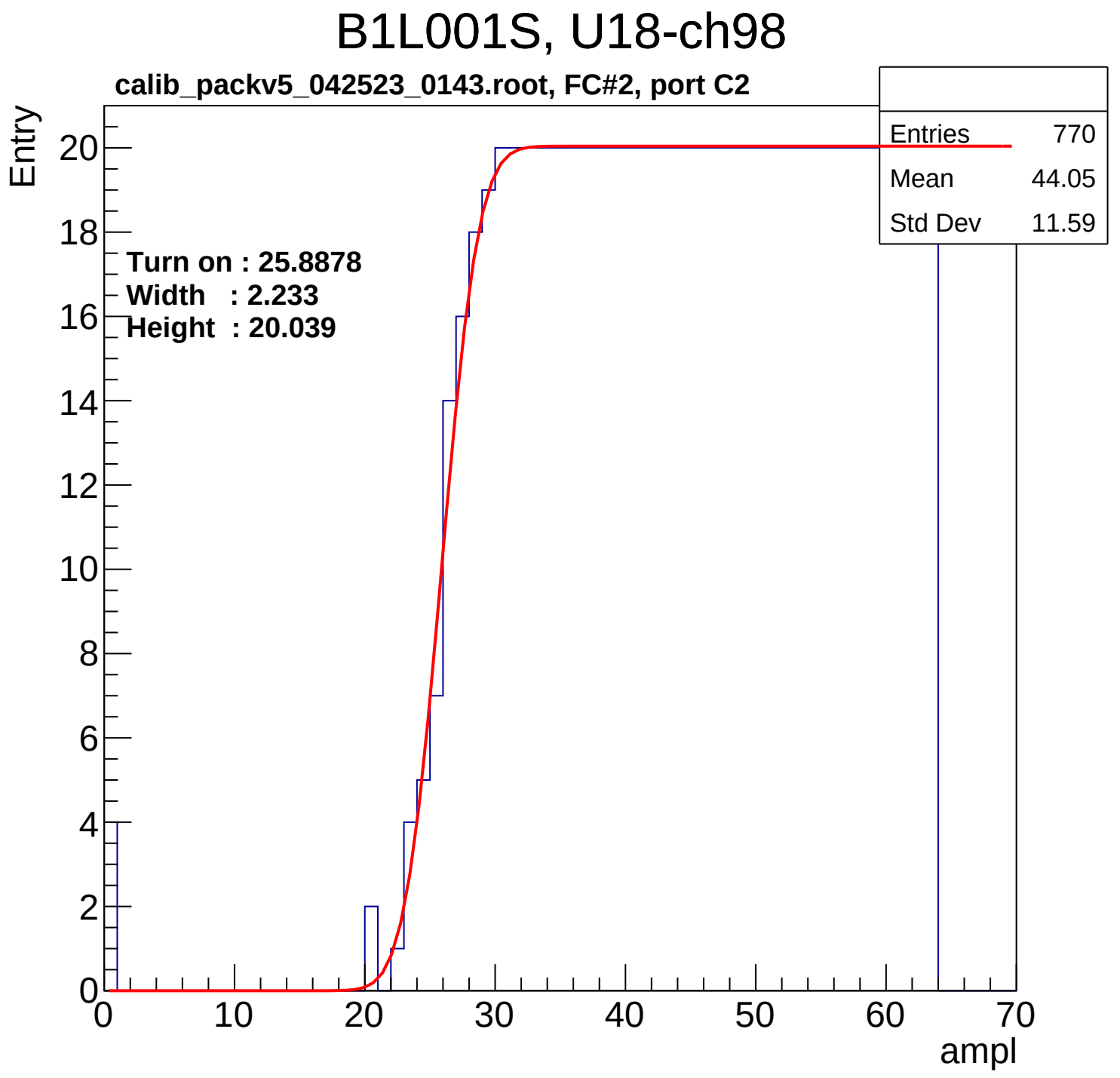
B1L001S, U18-ch98
calib_packv5_042523_0143.root, FC#2, port C2
Entries 770
Mean 44.05
Std Dev 11.59
Turn on : 25.8878
Width : 2.233
Height : 20.039
Entry
ampl
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8
10
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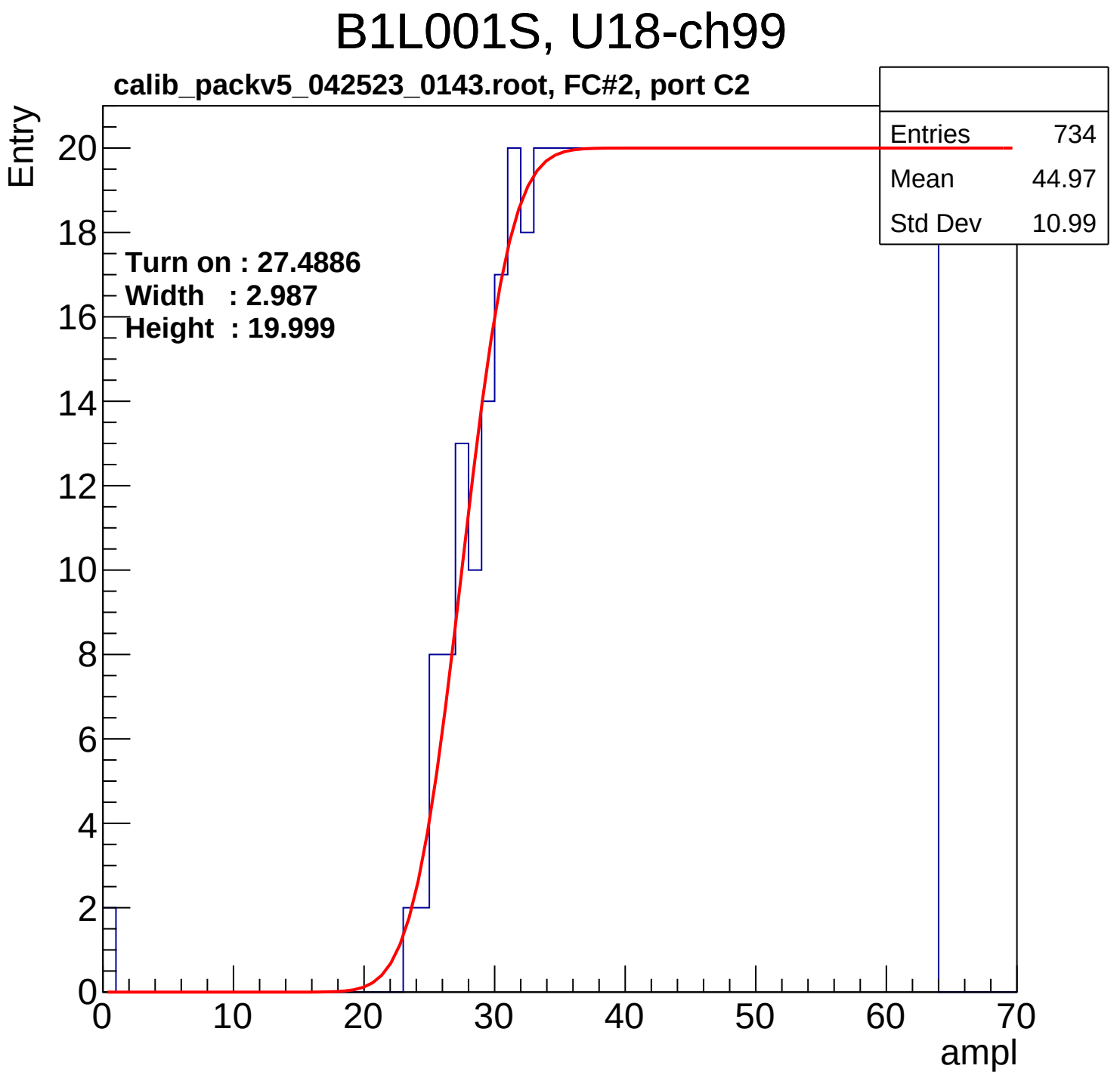
B1L001S, U18-ch99
calib_packv5_042523_0143.root, FC#2, port C2
Entries 734
Mean 44.97
Std Dev 10.99
Turn on : 27.4886
Width : 2.987
Height : 19.999
Entry
ampl
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8
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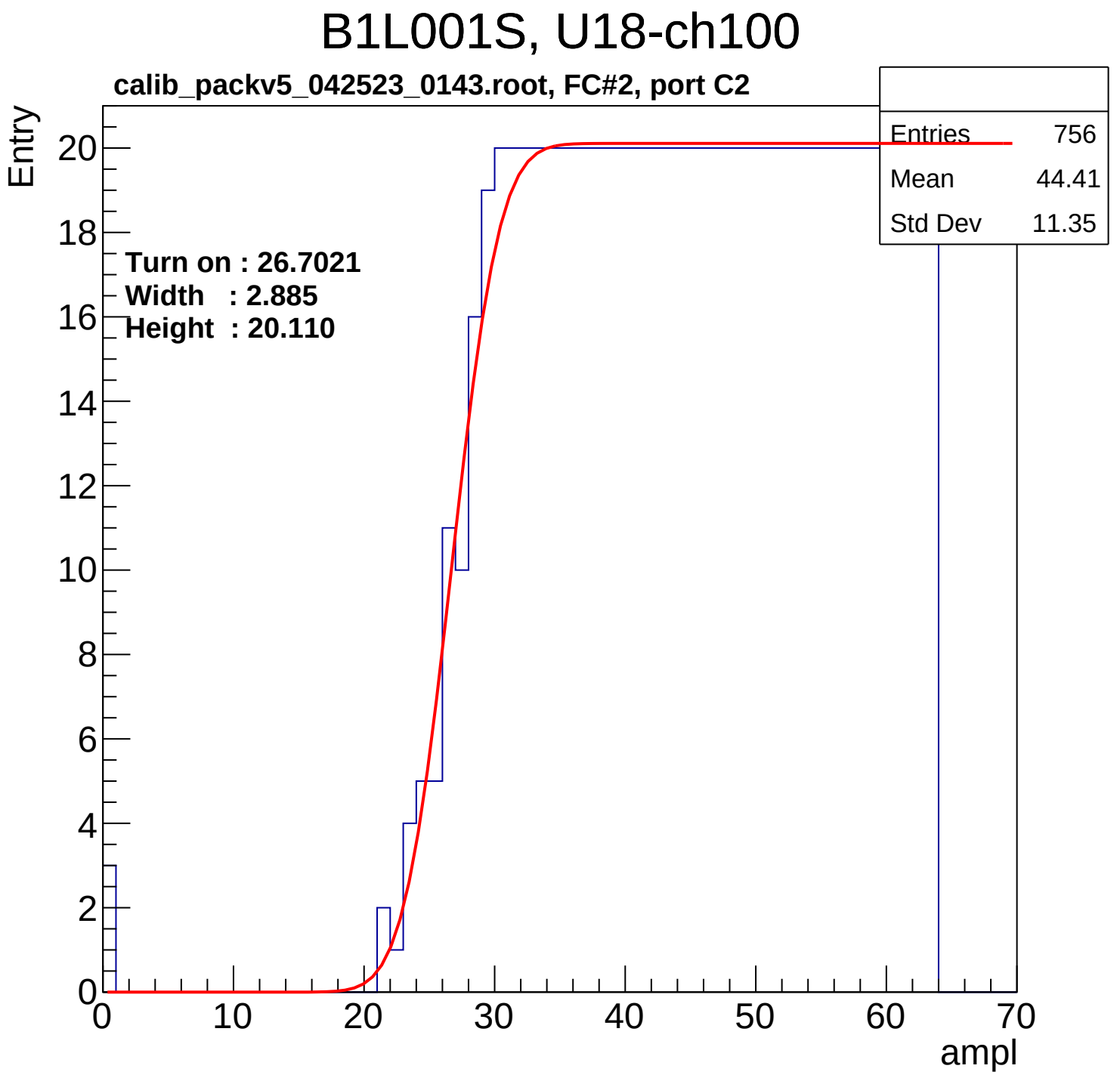
B1L001S, U18-ch100
calib_packv5_042523_0143.root, FC#2, port C2
Entries 756
Mean 44.41
Std Dev 11.35
Turn on : 26.7021
Width : 2.885
Height : 20.110
Entry
ampl
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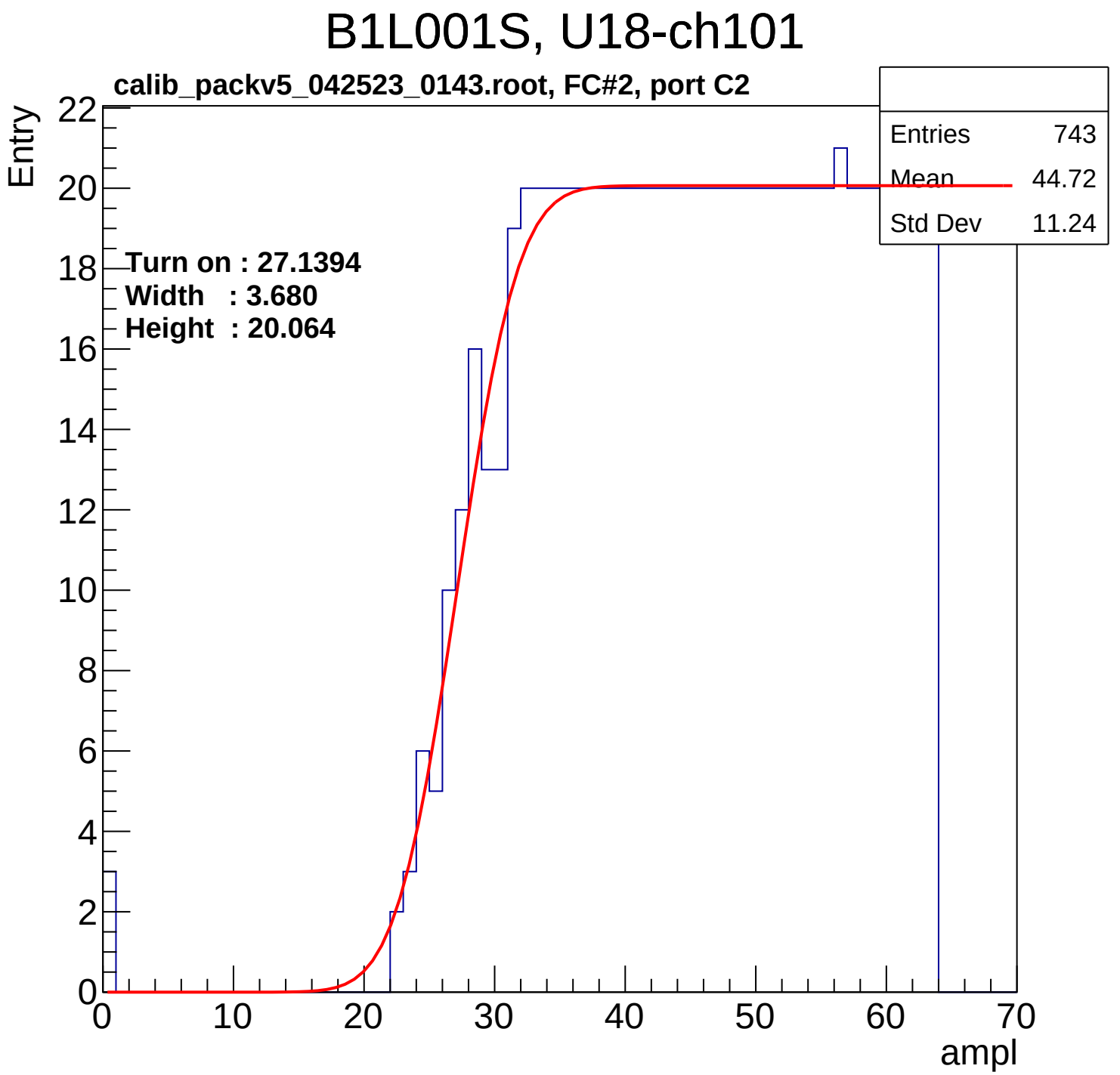
B1L001S, U18-ch101
calib_packv5_042523_0143.root, FC#2, port C2
Entries 743
Mean 44.72
Std Dev 11.24
Turn on : 27.1394
Width : 3.680
Height : 20.064
Entry
ampl
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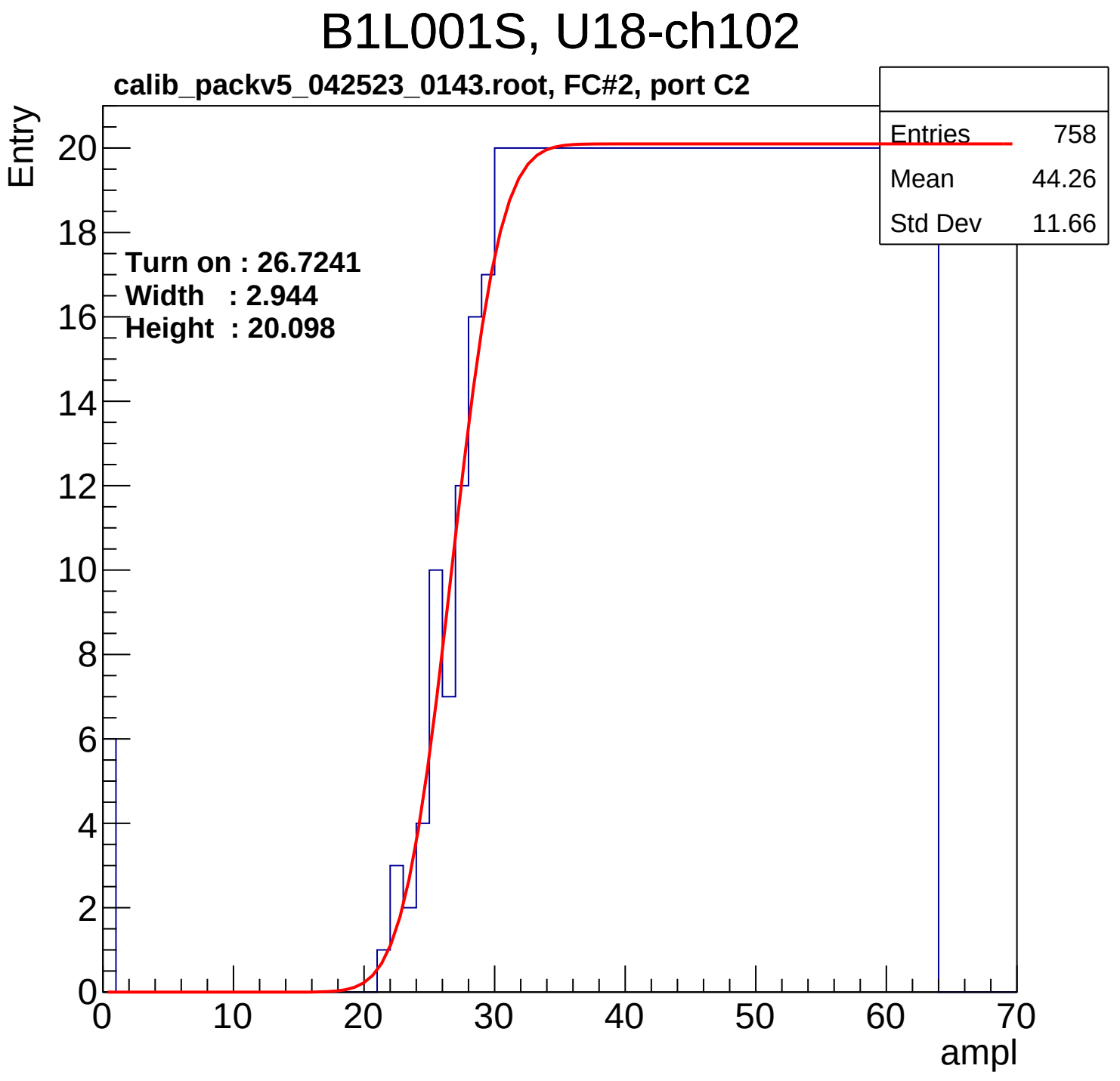
B1L001S, U18-ch102
calib_packv5_042523_0143.root, FC#2, port C2
Entries 758
Mean 44.26
Std Dev 11.66
Turn on : 26.7241
Width : 2.944
Height : 20.098
Entry
ampl
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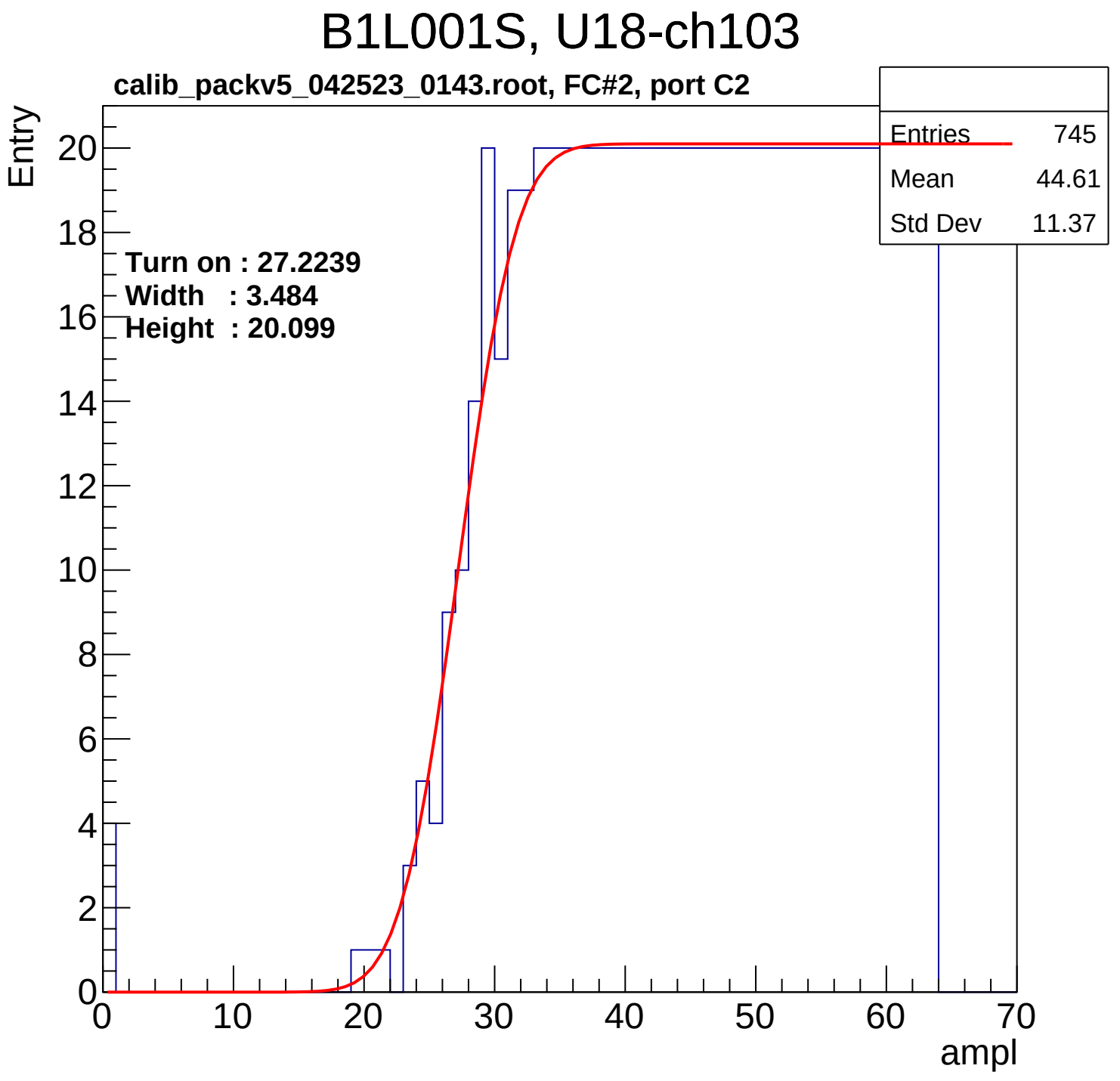
B1L001S, U18-ch103
calib_packv5_042523_0143.root, FC#2, port C2
Entries 745
Mean 44.61
Std Dev 11.37
Turn on : 27.2239
Width : 3.484
Height : 20.099
Entry
ampl
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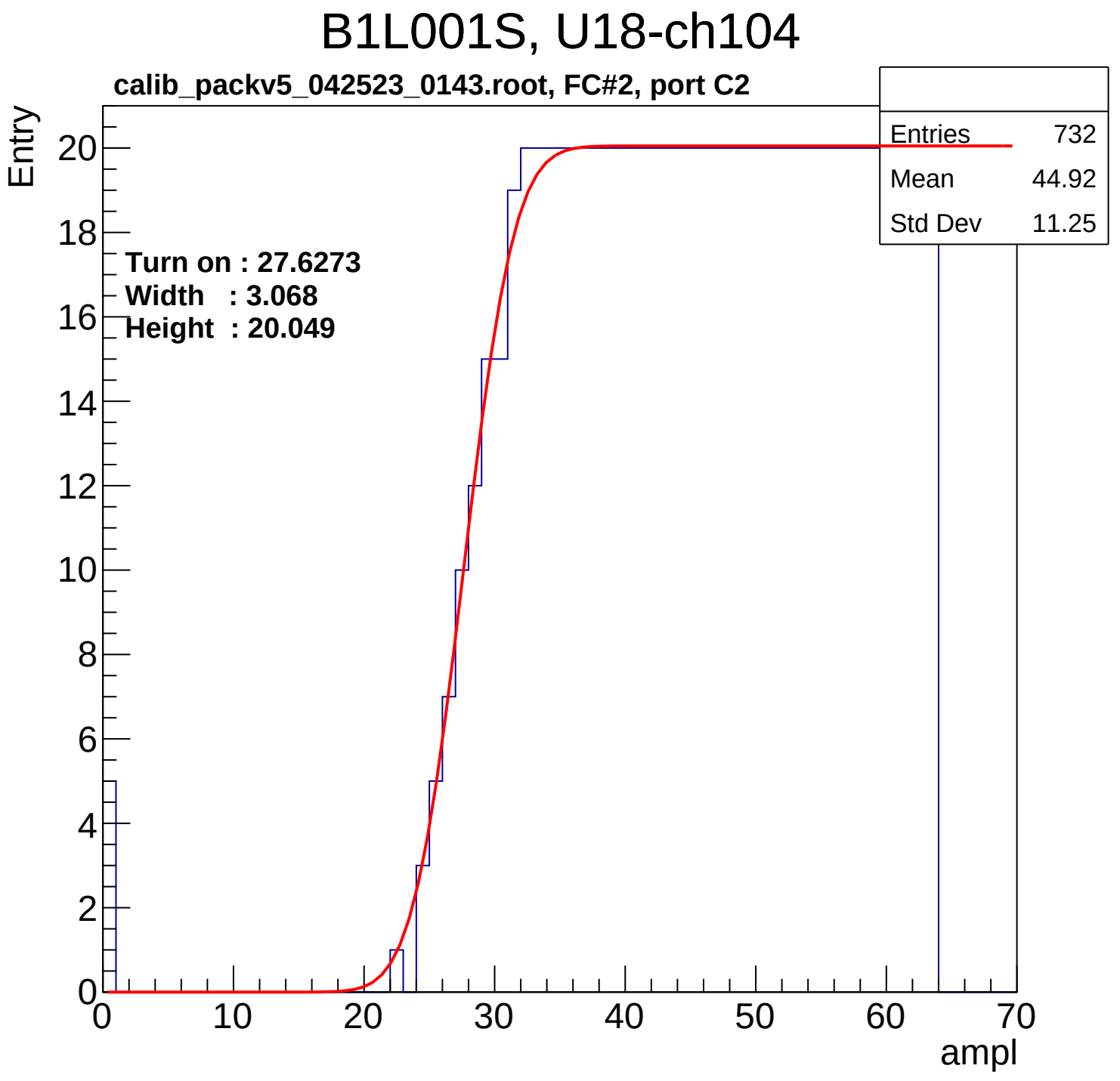
B1L001S, U18-ch104
calib_packv5_042523_0143.root, FC#2, port C2
Entries 732
Mean 44.92
Std Dev 11.25
Turn on : 27.6273
Width : 3.068
Height : 20.049
Entry
ampl
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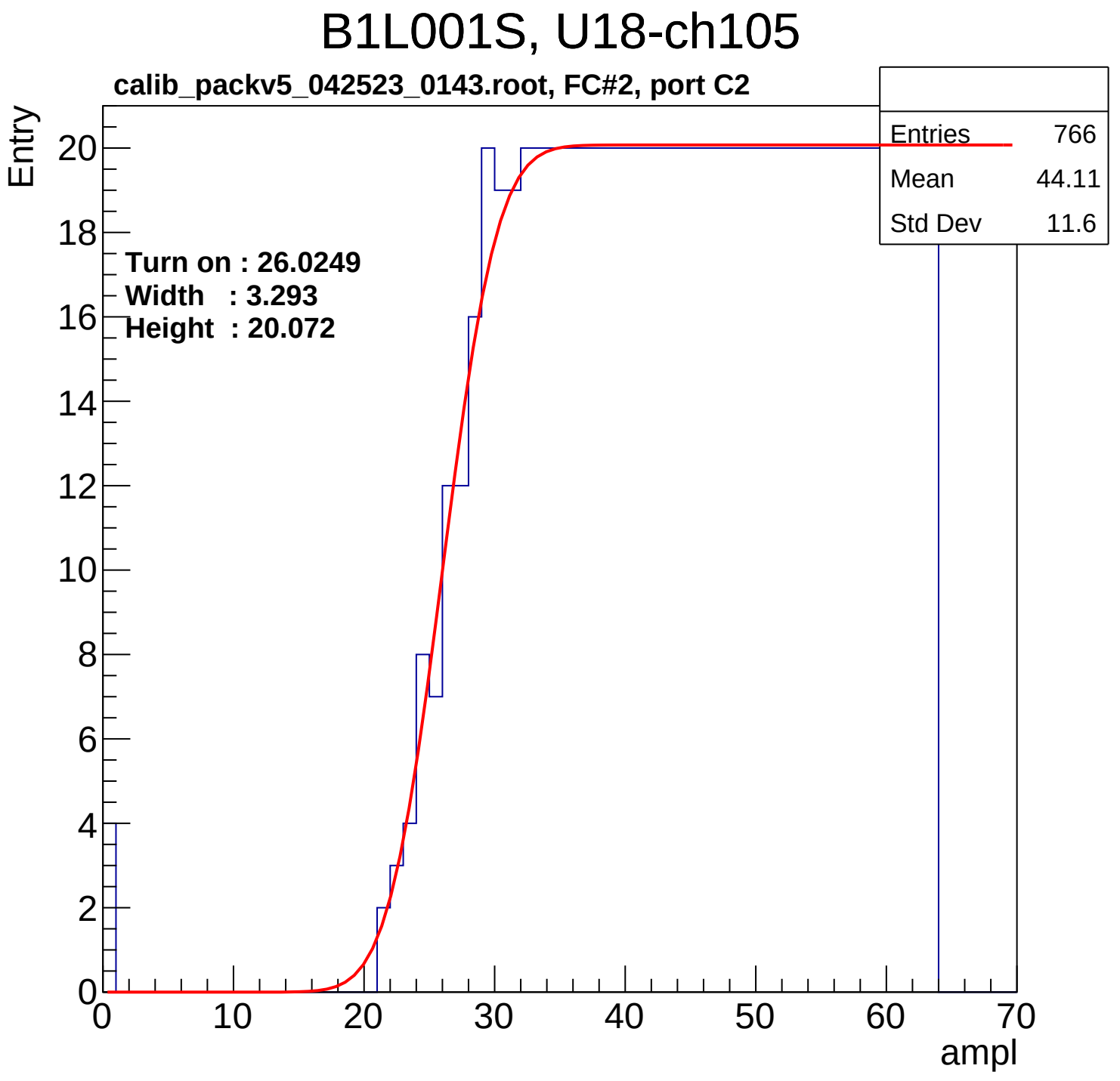
B1L001S, U18-ch105
calib_packv5_042523_0143.root, FC#2, port C2
Entries 766
Mean 44.11
Std Dev 11.6
Turn on : 26.0249
Width : 3.293
Height : 20.072
Entry
ampl
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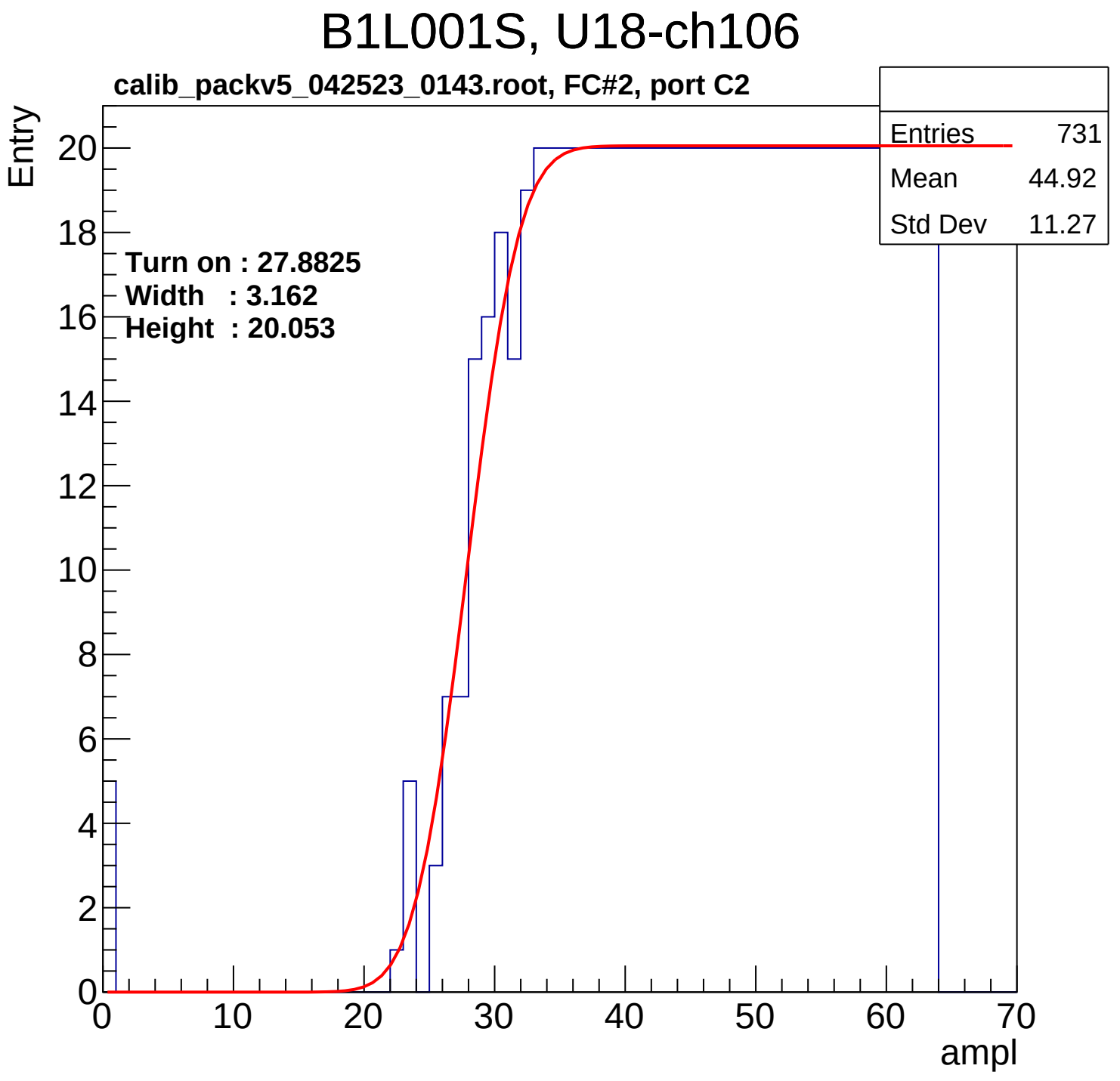
B1L001S, U18-ch106
calib_packv5_042523_0143.root, FC#2, port C2
Entries 731
Mean 44.92
Std Dev 11.27
Turn on : 27.8825
Width : 3.162
Height : 20.053
Entry
ampl
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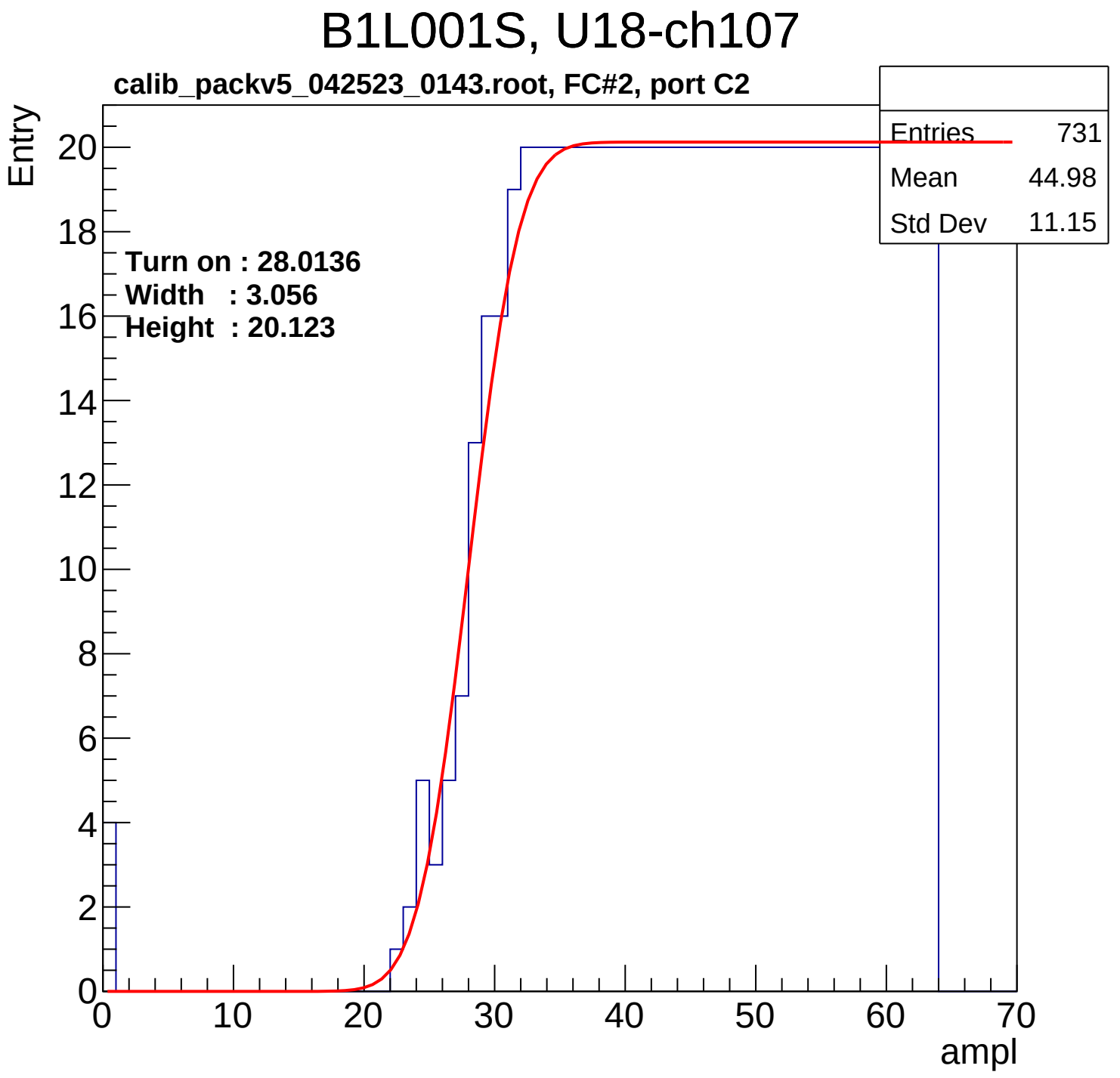
B1L001S, U18-ch107
calib_packv5_042523_0143.root, FC#2, port C2
Entries 731
Mean 44.98
Std Dev 11.15
Turn on : 28.0136
Width : 3.056
Height : 20.123
Entry
ampl
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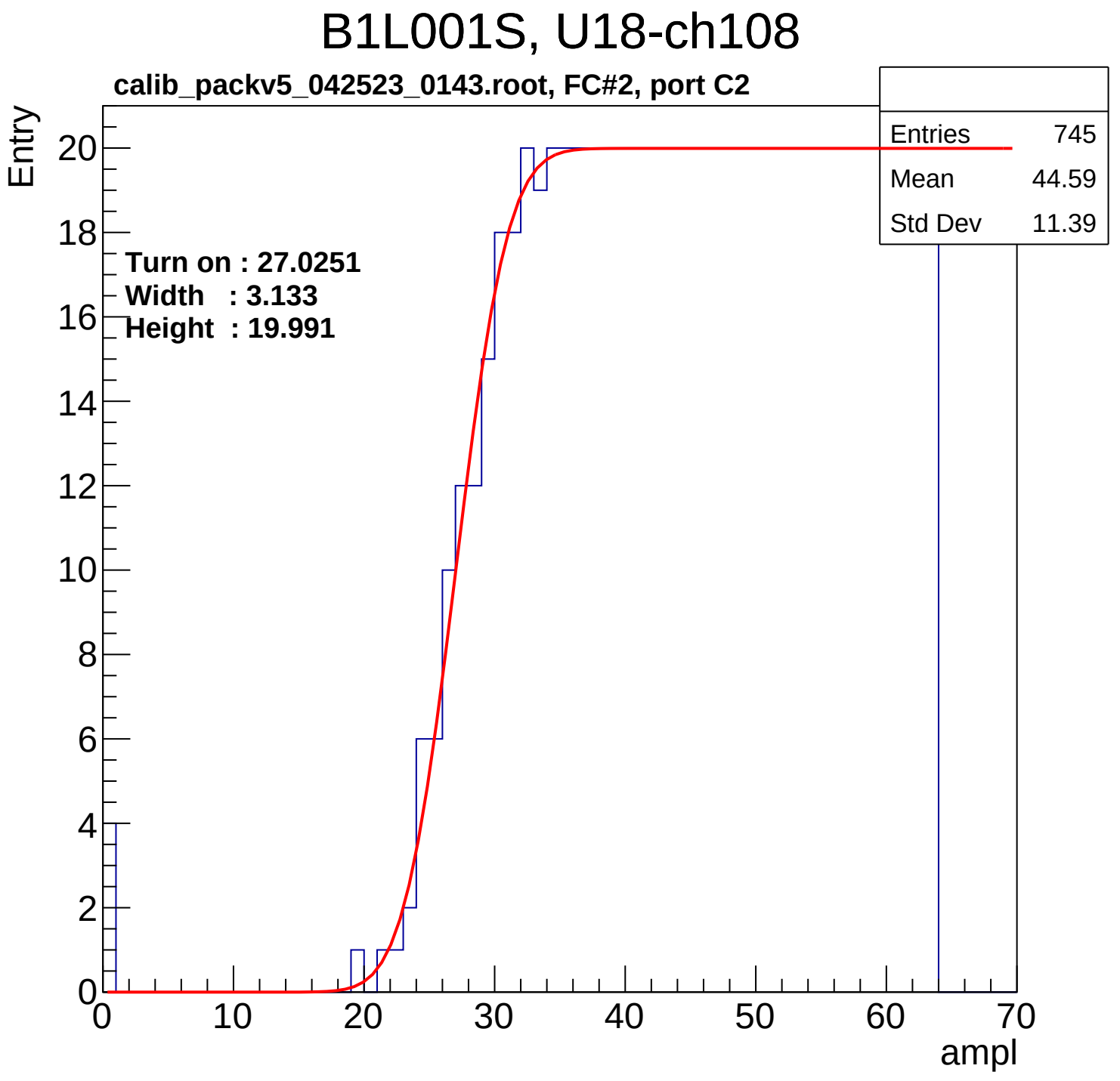
B1L001S, U18-ch108
calib_packv5_042523_0143.root, FC#2, port C2
Entries 745
Mean 44.59
Std Dev 11.39
Turn on : 27.0251
Width : 3.133
Height : 19.991
Entry
ampl
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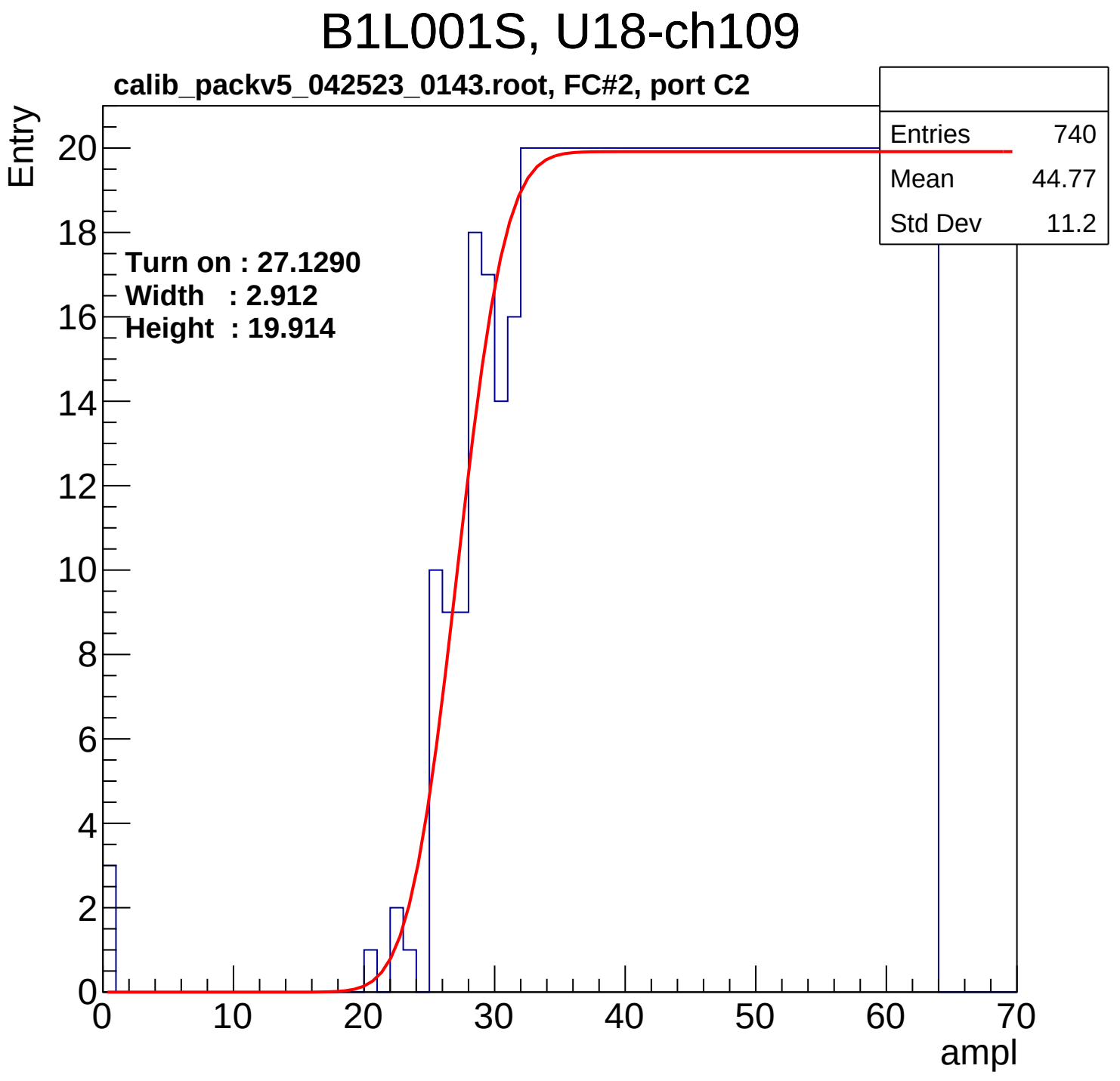
B1L001S, U18-ch109
calib_packv5_042523_0143.root, FC#2, port C2
Entries 740
Mean 44.77
Std Dev 11.2
Turn on : 27.1290
Width : 2.912
Height : 19.914
Entry
ampl
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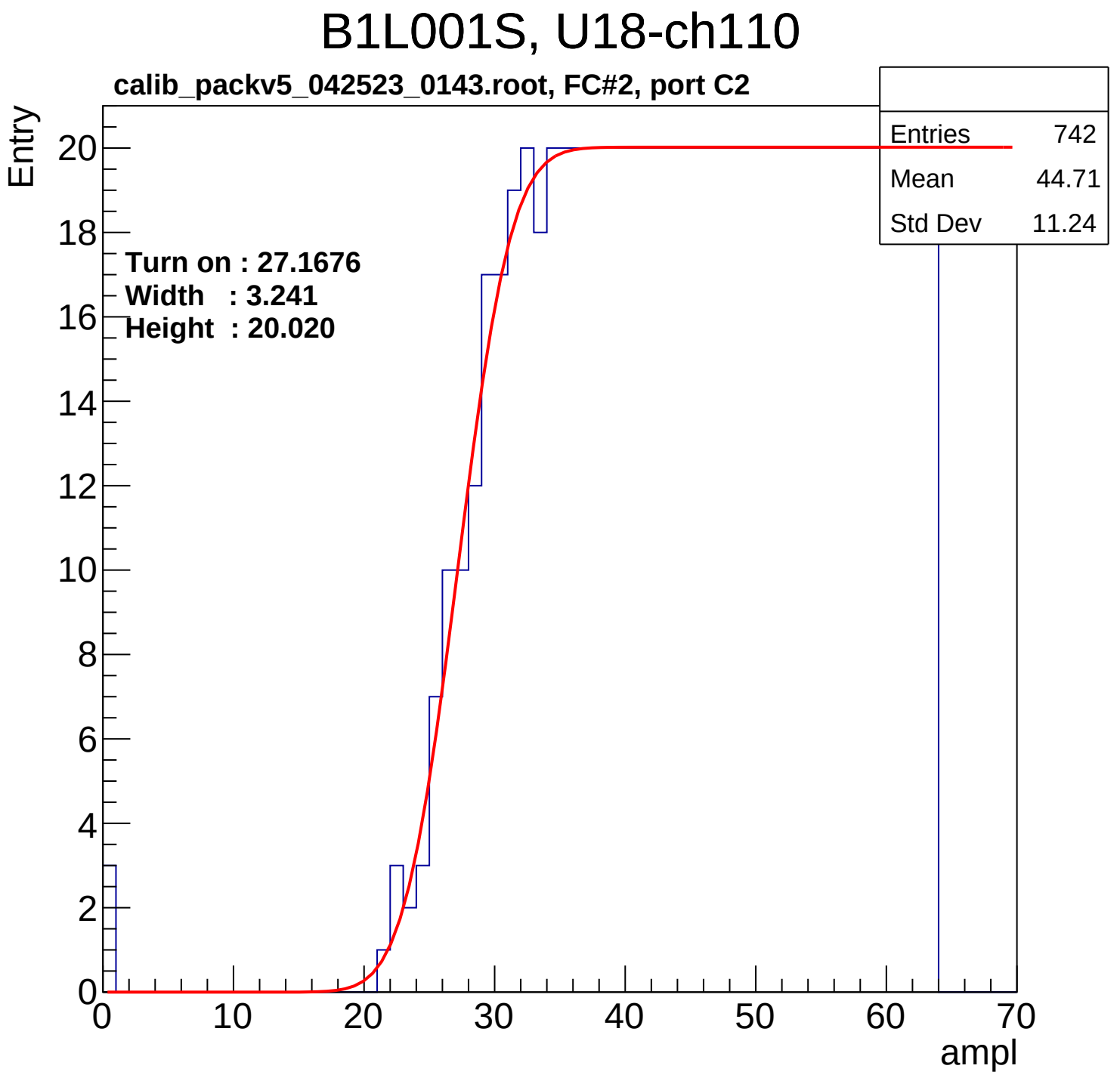
B1L001S, U18-ch110
calib_packv5_042523_0143.root, FC#2, port C2
Entries 742
Mean 44.71
Std Dev 11.24
Turn on : 27.1676
Width : 3.241
Height : 20.020
Entry
ampl
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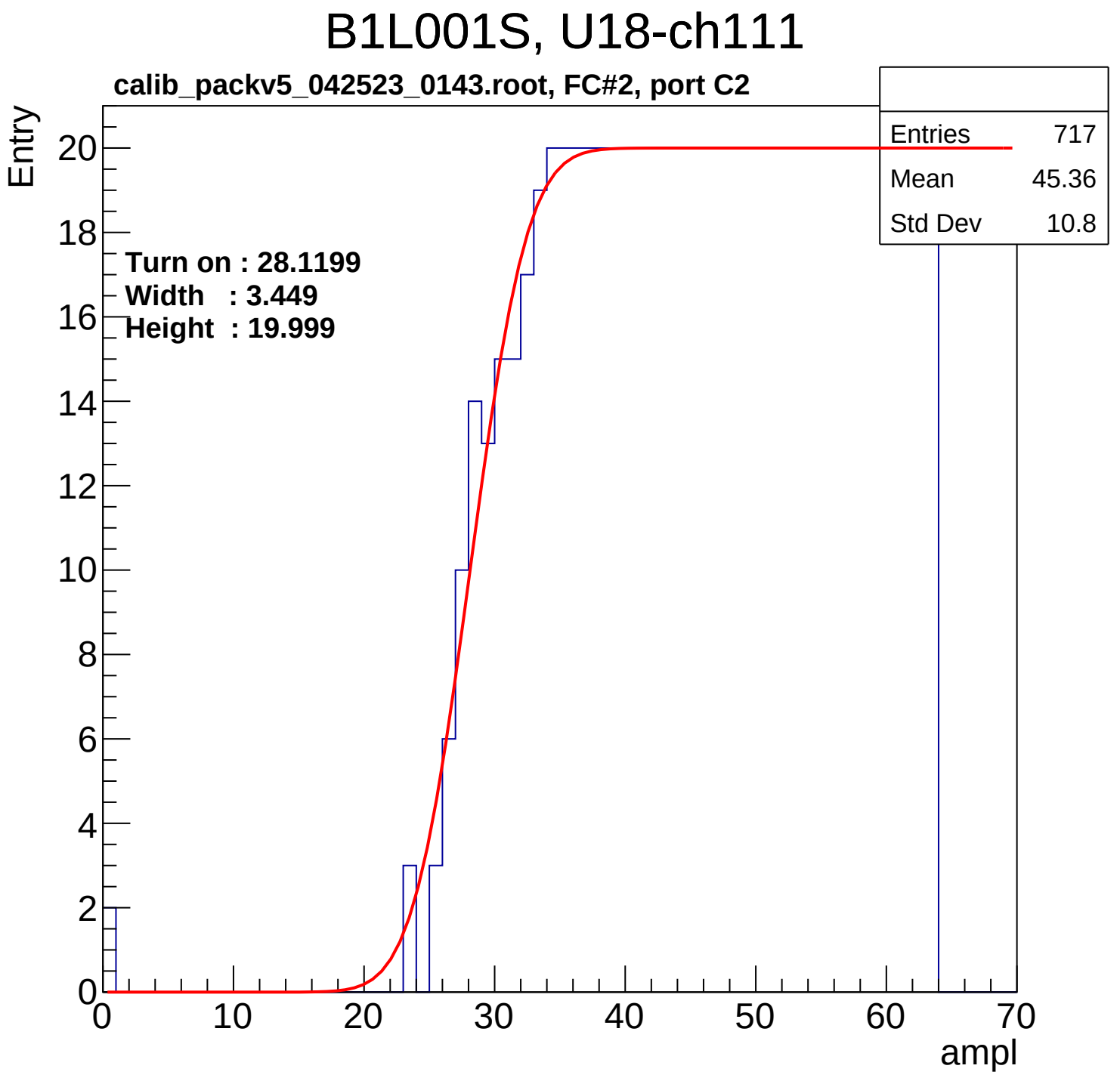
B1L001S, U18-ch111
calib_packv5_042523_0143.root, FC#2, port C2
Entries 717
Mean 45.36
Std Dev 10.8
Turn on : 28.1199
Width : 3.449
Height : 19.999
Entry
ampl
0
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6
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10
12
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18
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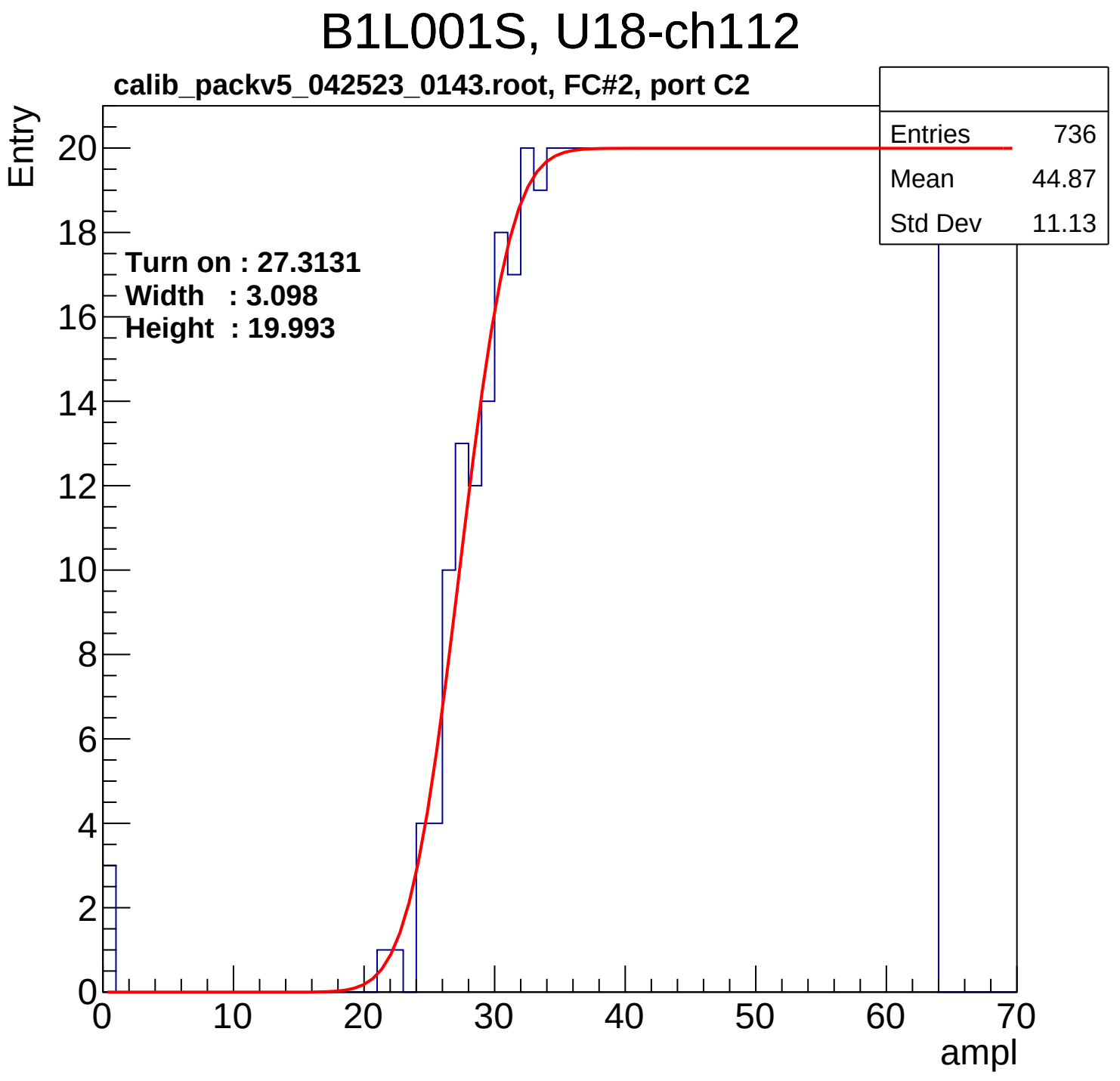
B1L001S, U18-ch112
calib_packv5_042523_0143.root, FC#2, port C2
Entries 736
Mean 44.87
Std Dev 11.13
Turn on : 27.3131
Width : 3.098
Height : 19.993
Entry
ampl
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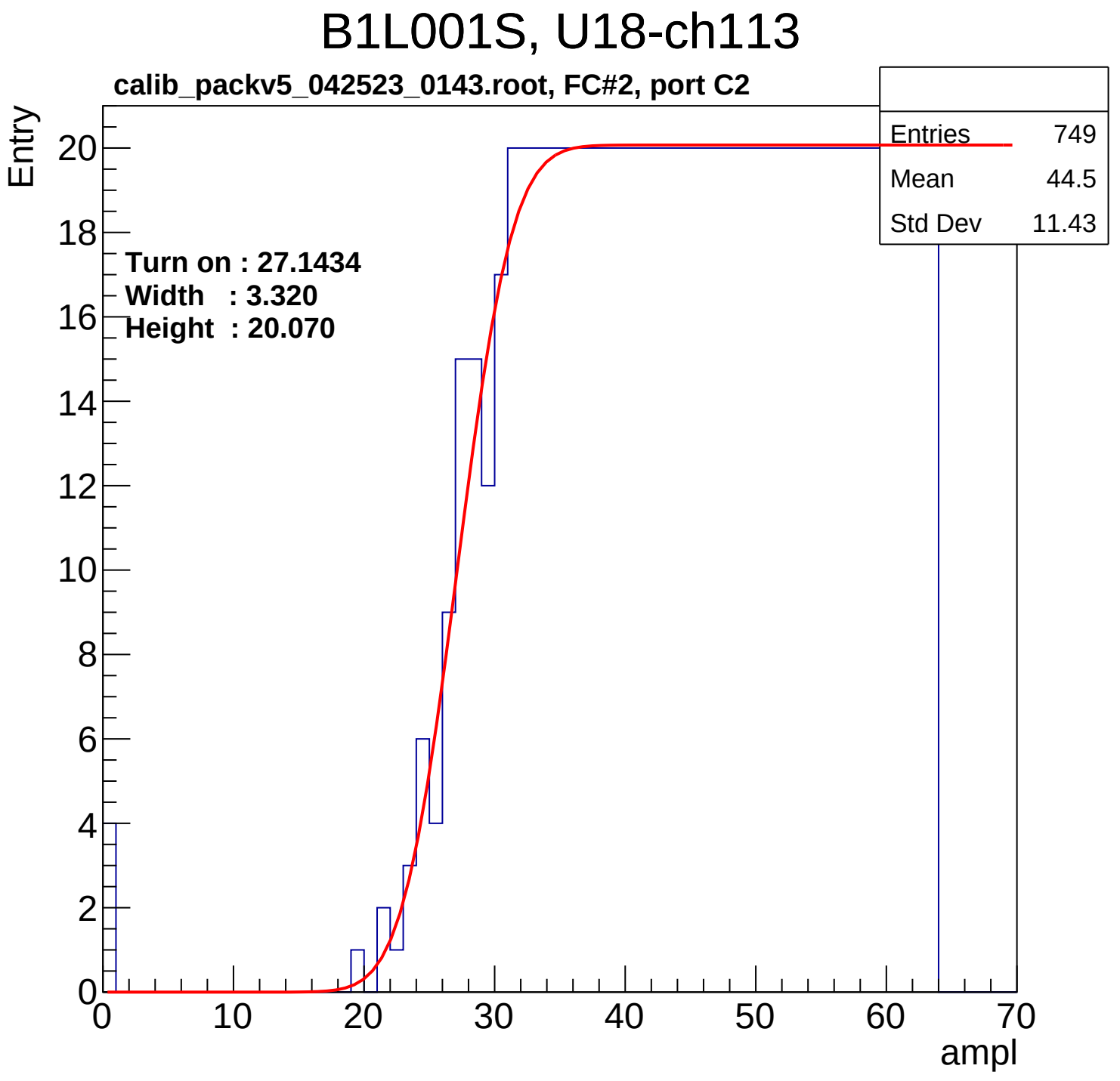
B1L001S, U18-ch113
calib_packv5_042523_0143.root, FC#2, port C2
Entries 749
Mean 44.5
Std Dev 11.43
Turn on : 27.1434
Width : 3.320
Height : 20.070
Entry
ampl
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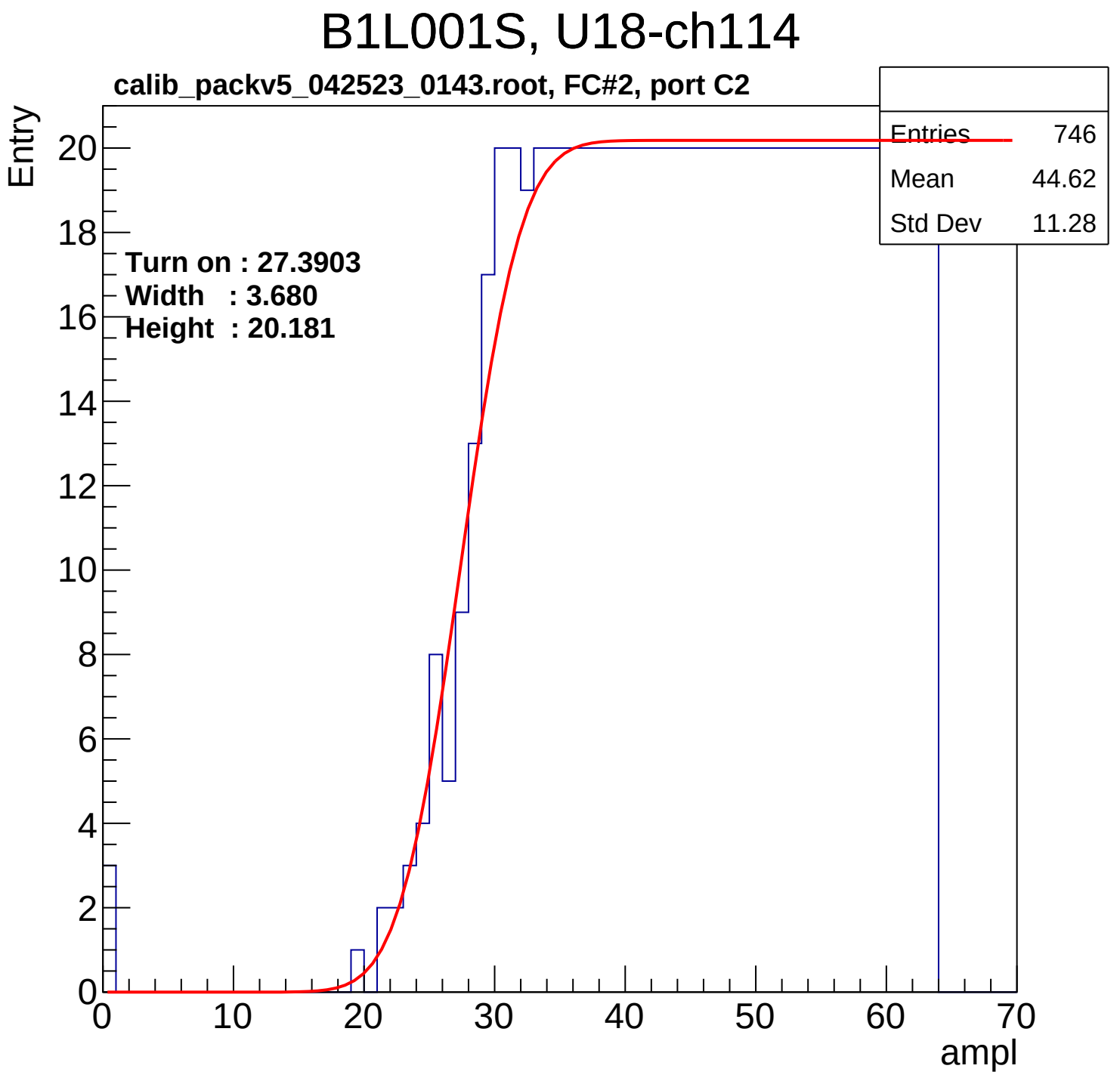
B1L001S, U18-ch114
calib_packv5_042523_0143.root, FC#2, port C2
Entries 746
Mean 44.62
Std Dev 11.28
Turn on : 27.3903
Width : 3.680
Height : 20.181
Entry
ampl
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6
8
10
12
14
16
18
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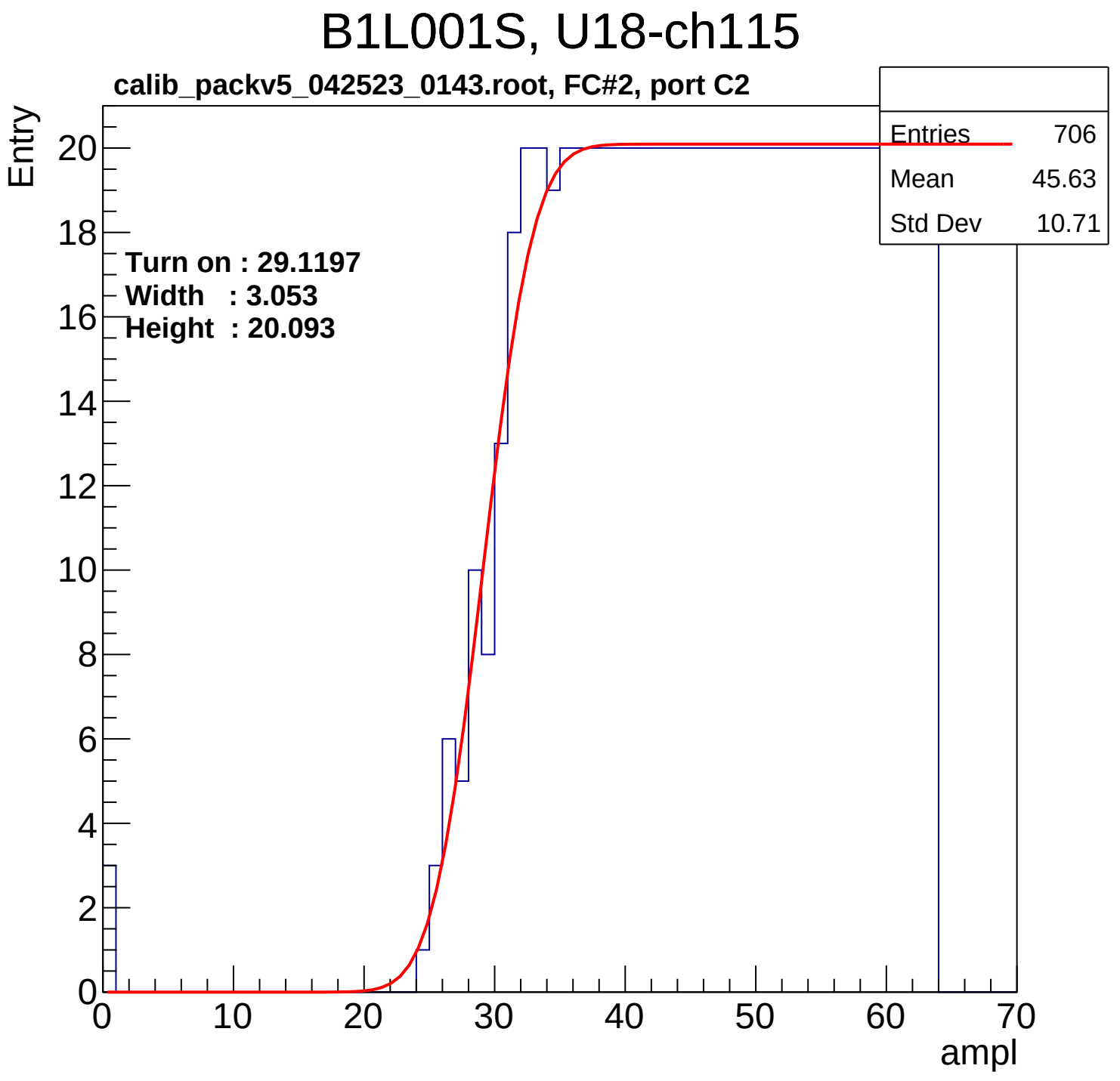
B1L001S, U18-ch115
calib_packv5_042523_0143.root, FC#2, port C2
Entries 706
Mean 45.63
Std Dev 10.71
Turn on : 29.1197
Width : 3.053
Height : 20.093
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
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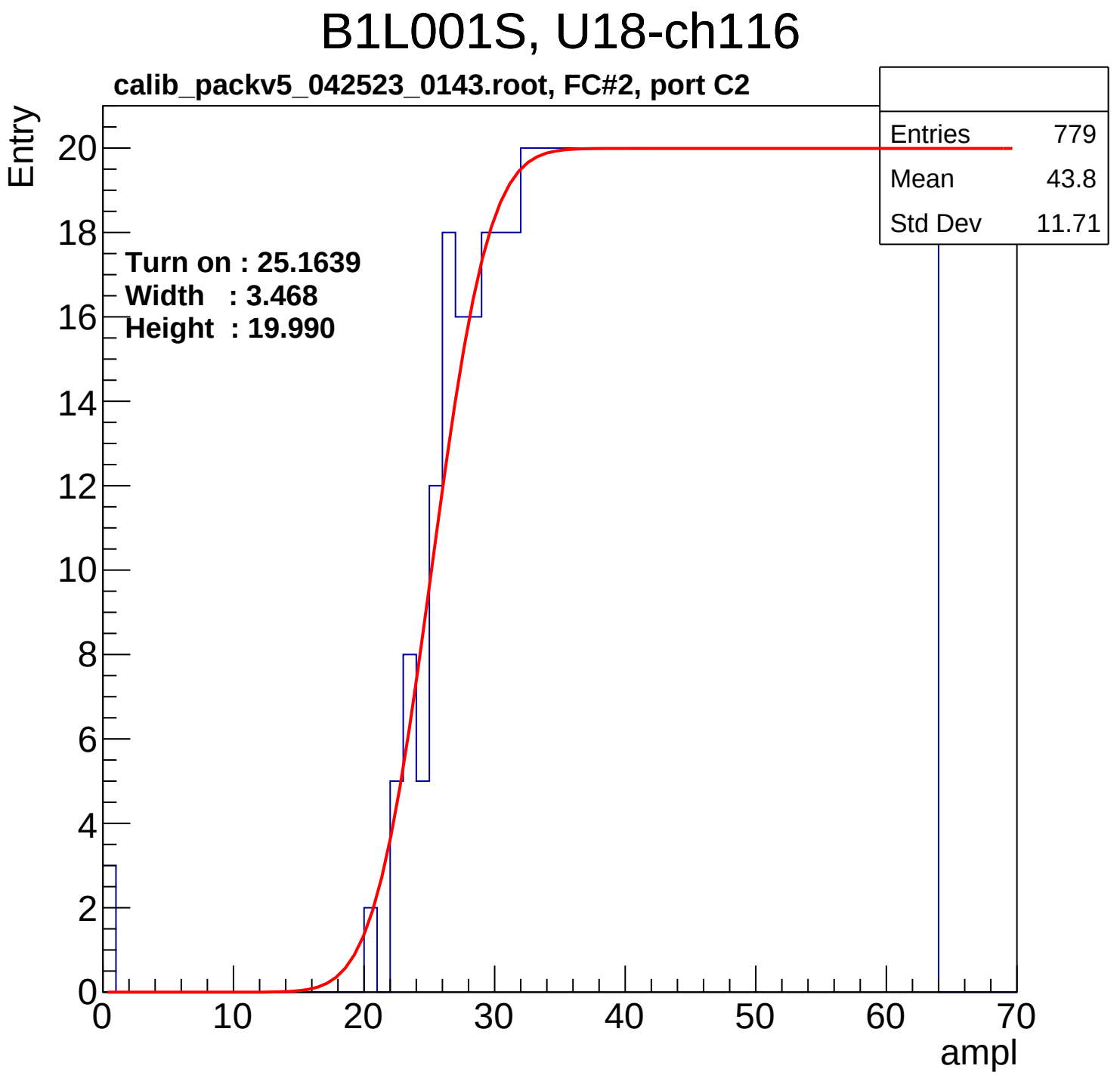
B1L001S, U18-ch116
calib_packv5_042523_0143.root, FC#2, port C2
Entries 779
Mean 43.8
Std Dev 11.71
Turn on : 25.1639
Width : 3.468
Height : 19.990
Entry
ampl
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6
8
10
12
14
16
18
20
0
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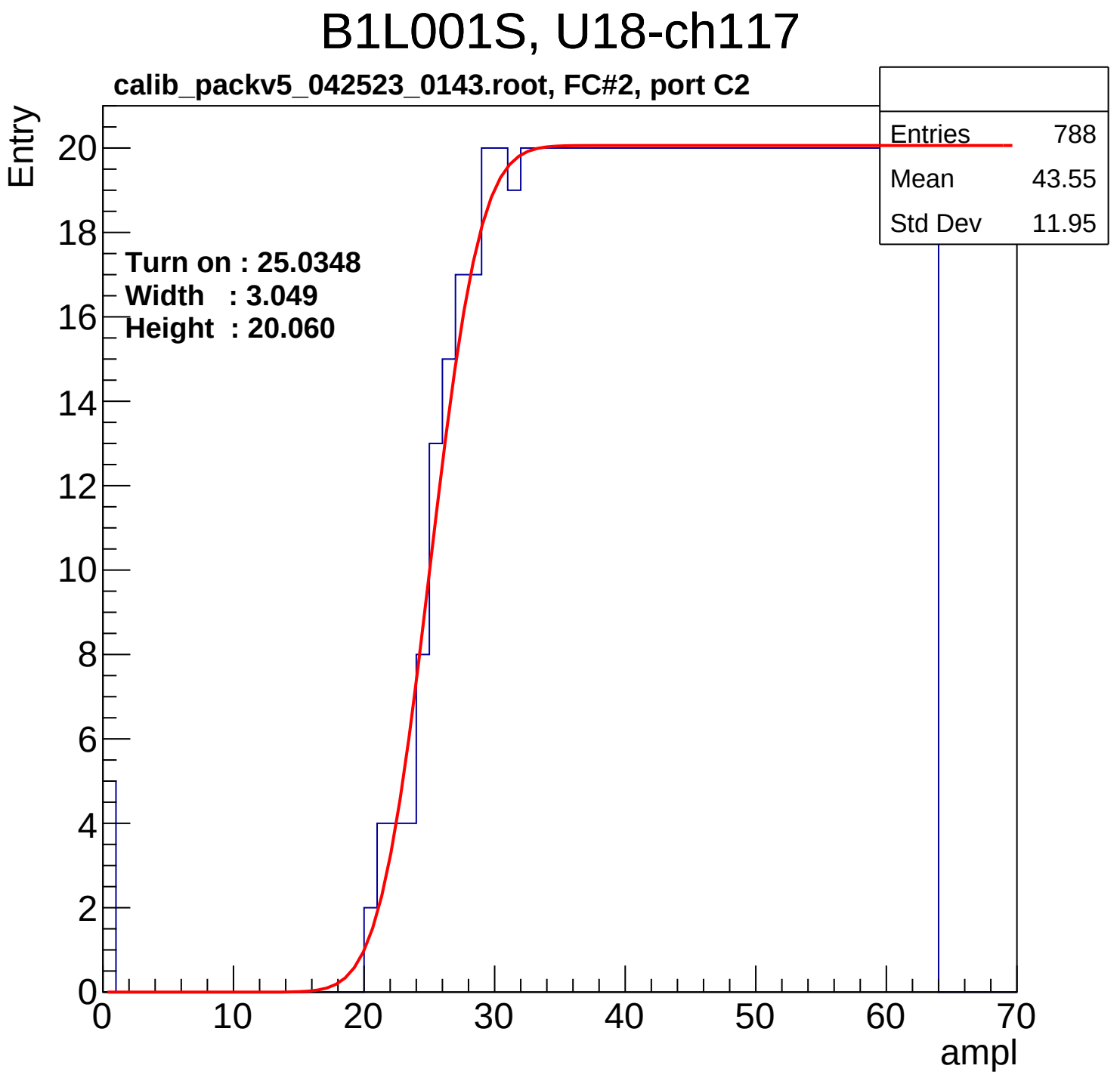
B1L001S, U18-ch117
calib_packv5_042523_0143.root, FC#2, port C2
Entries 788
Mean 43.55
Std Dev 11.95
Turn on : 25.0348
Width : 3.049
Height : 20.060
Entry
ampl
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6
8
10
12
14
16
18
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0
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20
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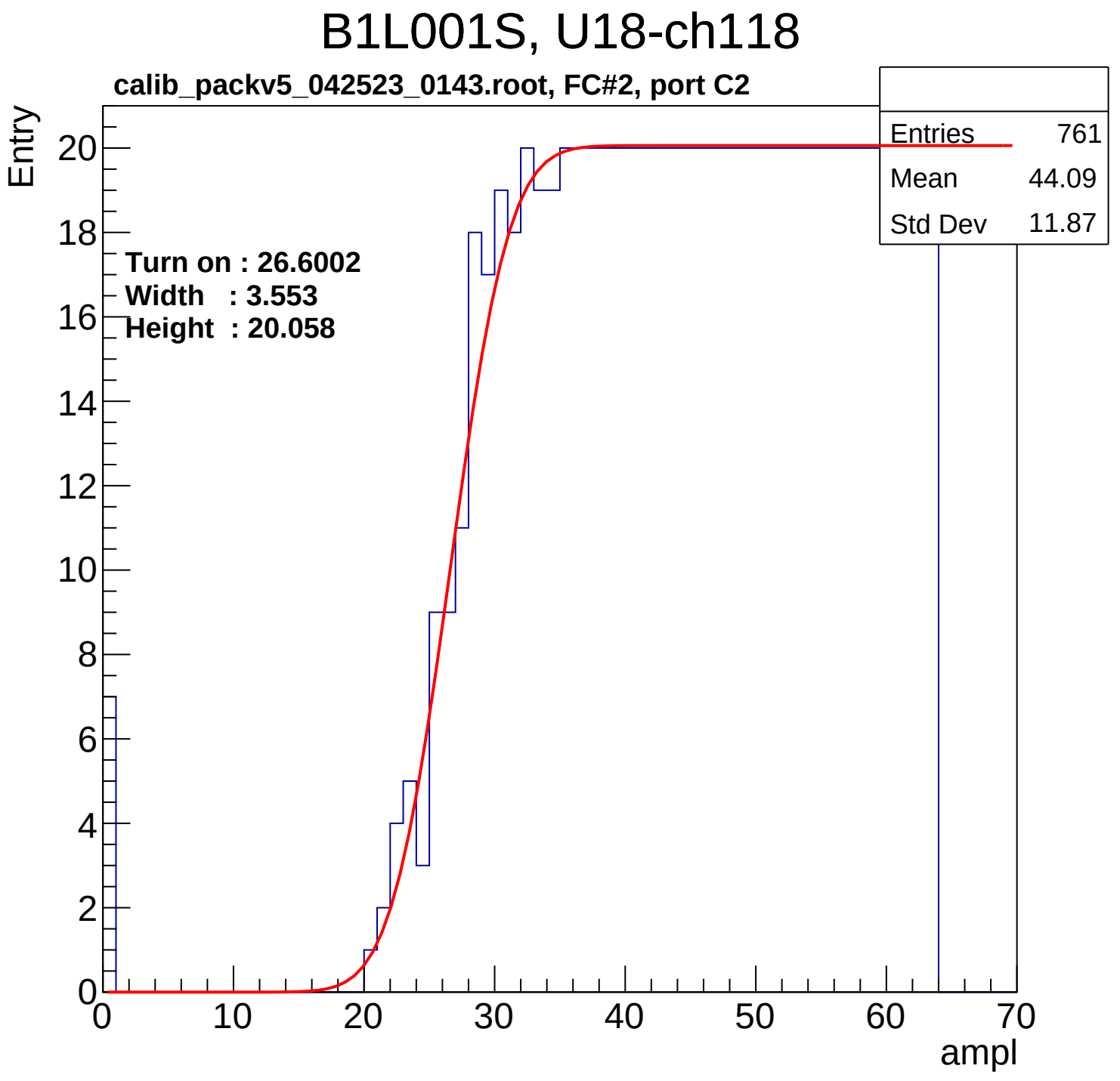
B1L001S, U18-ch118
calib_packv5_042523_0143.root, FC#2, port C2
Entries 761
Mean 44.09
Std Dev 11.87
Turn on : 26.6002
Width : 3.553
Height : 20.058
Entry
ampl
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6
8
10
12
14
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18
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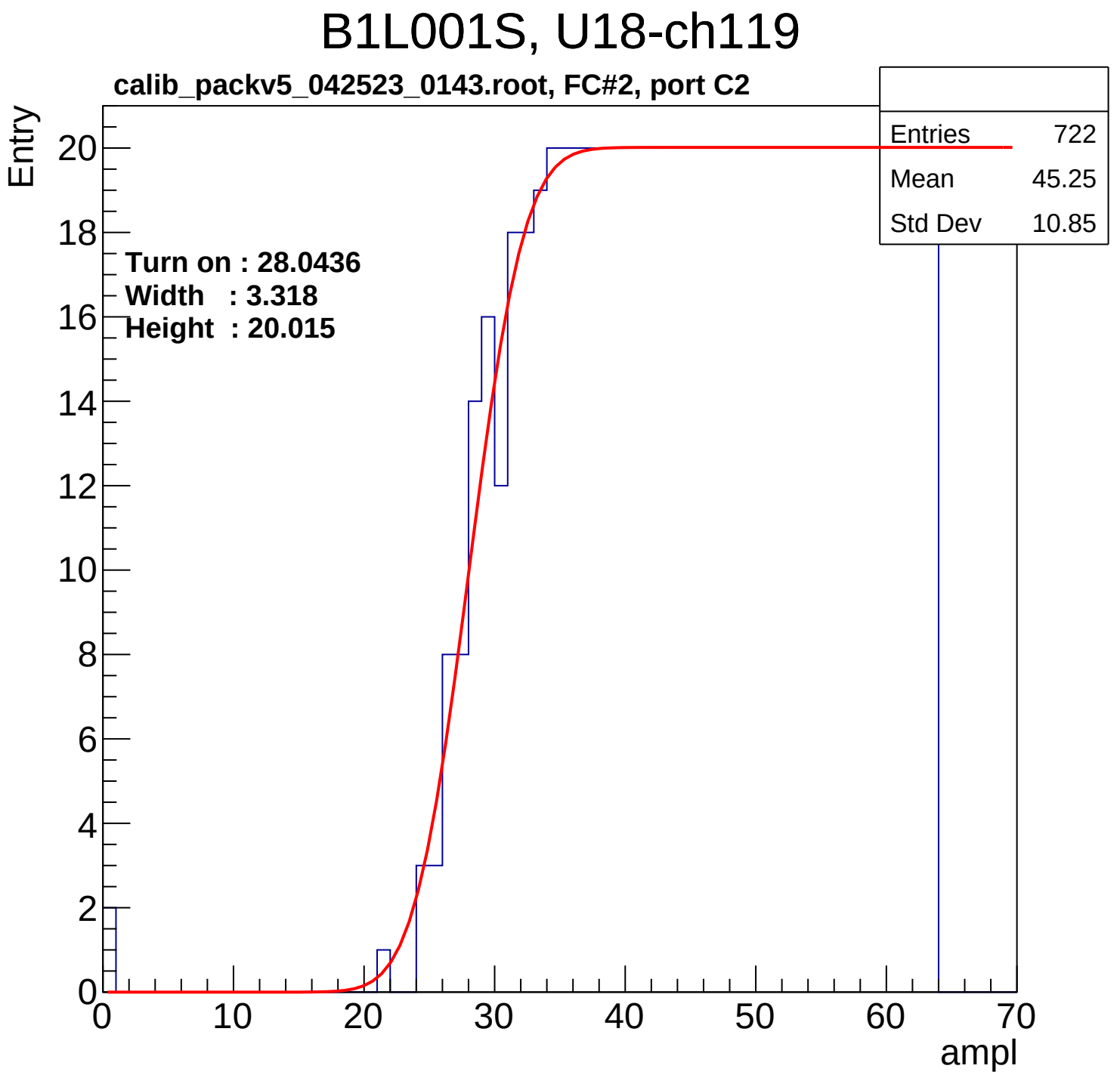
B1L001S, U18-ch119
calib_packv5_042523_0143.root, FC#2, port C2
Entries 722
Mean 45.25
Std Dev 10.85
Turn on : 28.0436
Width : 3.318
Height : 20.015
Entry
ampl
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6
8
10
12
14
16
18
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0
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20
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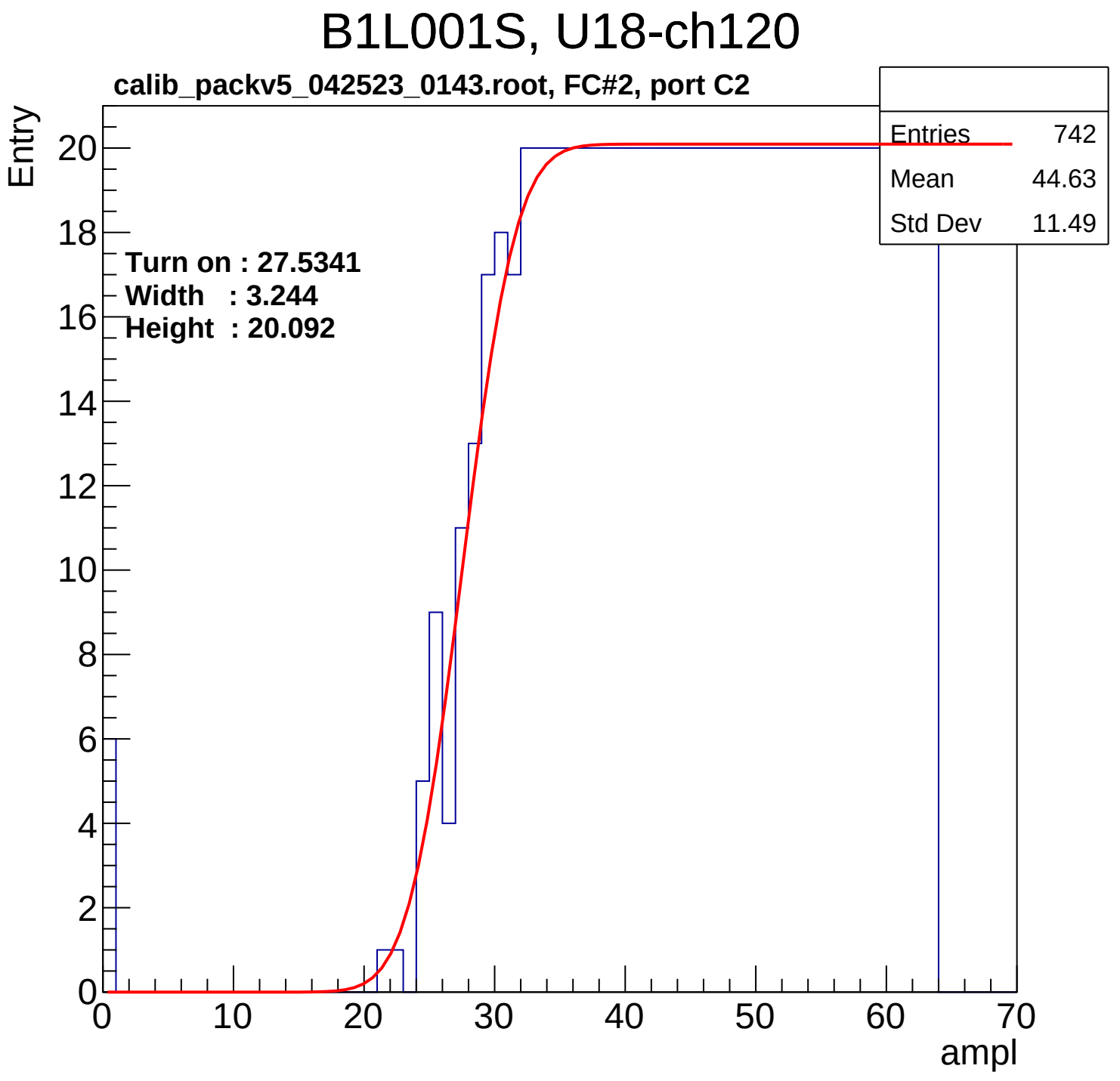
B1L001S, U18-ch120
calib_packv5_042523_0143.root, FC#2, port C2
Entries 742
Mean 44.63
Std Dev 11.49
Turn on : 27.5341
Width : 3.244
Height : 20.092
Entry
ampl
0
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4
6
8
10
12
14
16
18
20
0
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20
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40
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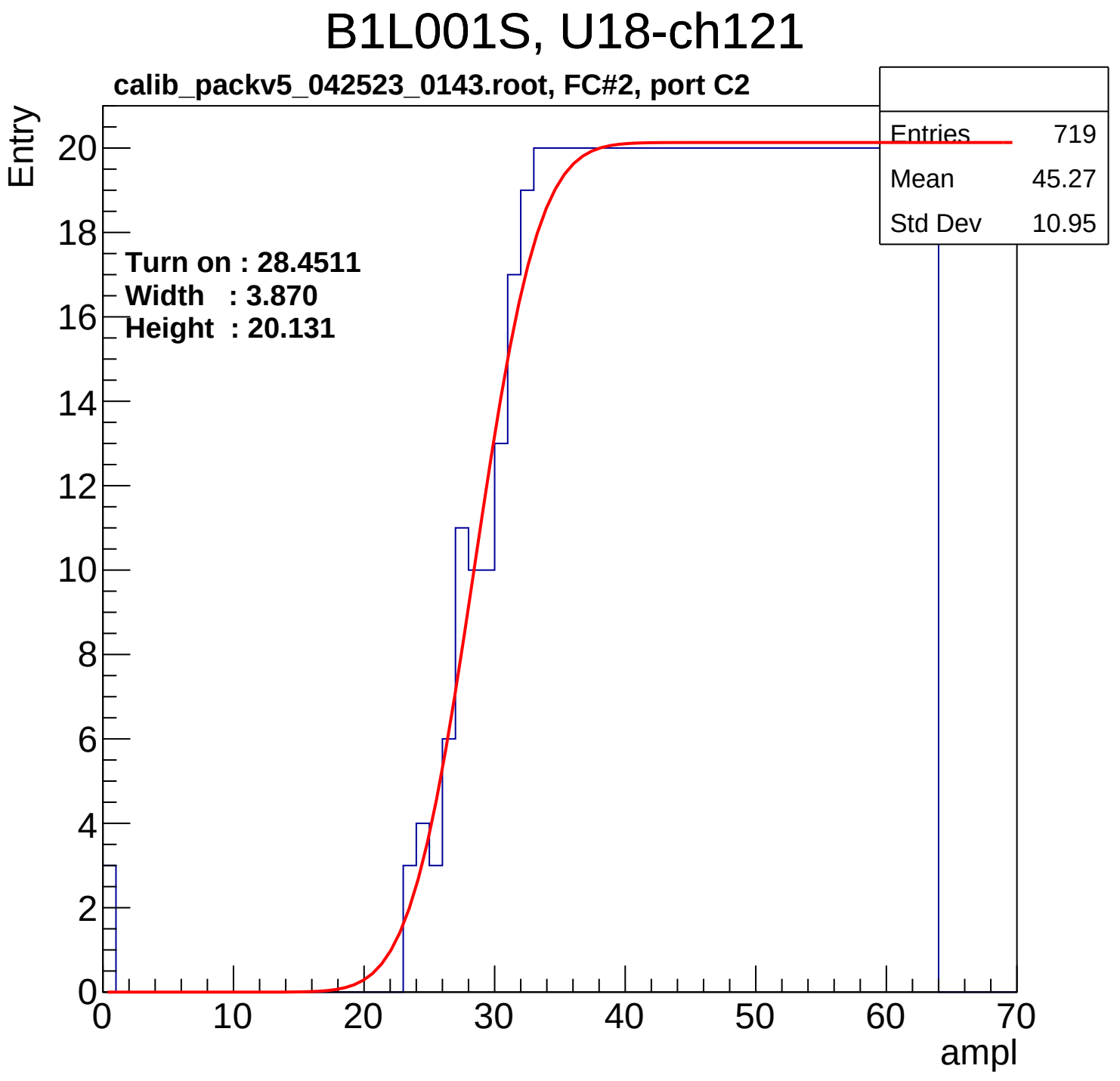
B1L001S, U18-ch121
calib_packv5_042523_0143.root, FC#2, port C2
Entries 719
Mean 45.27
Std Dev 10.95
Turn on : 28.4511
Width : 3.870
Height : 20.131
Entry
ampl
0
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4
6
8
10
12
14
16
18
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0
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20
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40
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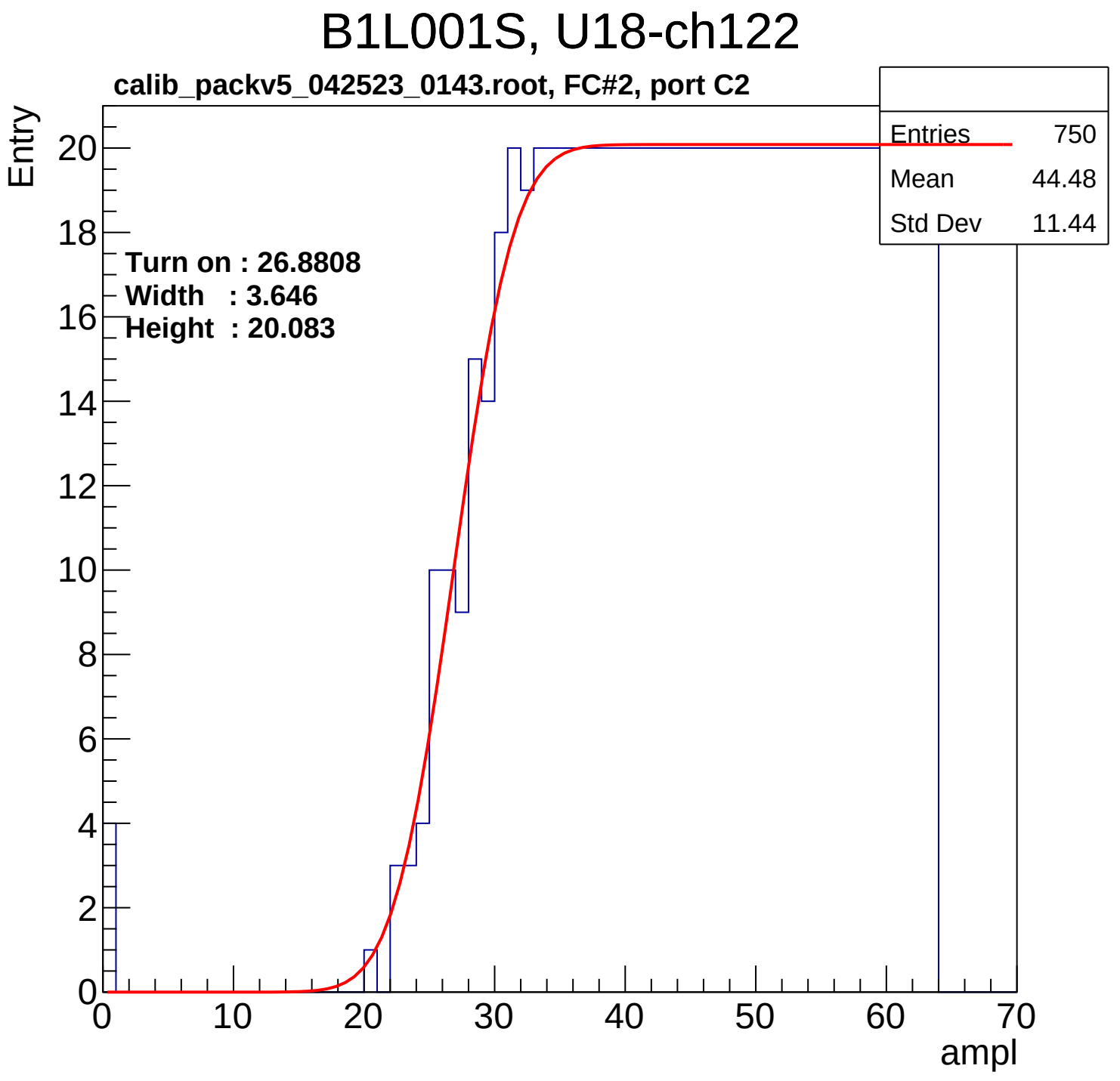
B1L001S, U18-ch122
calib_packv5_042523_0143.root, FC#2, port C2
Entries 750
Mean 44.48
Std Dev 11.44
Turn on : 26.8808
Width : 3.646
Height : 20.083
Entry
ampl
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6
8
10
12
14
16
18
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0
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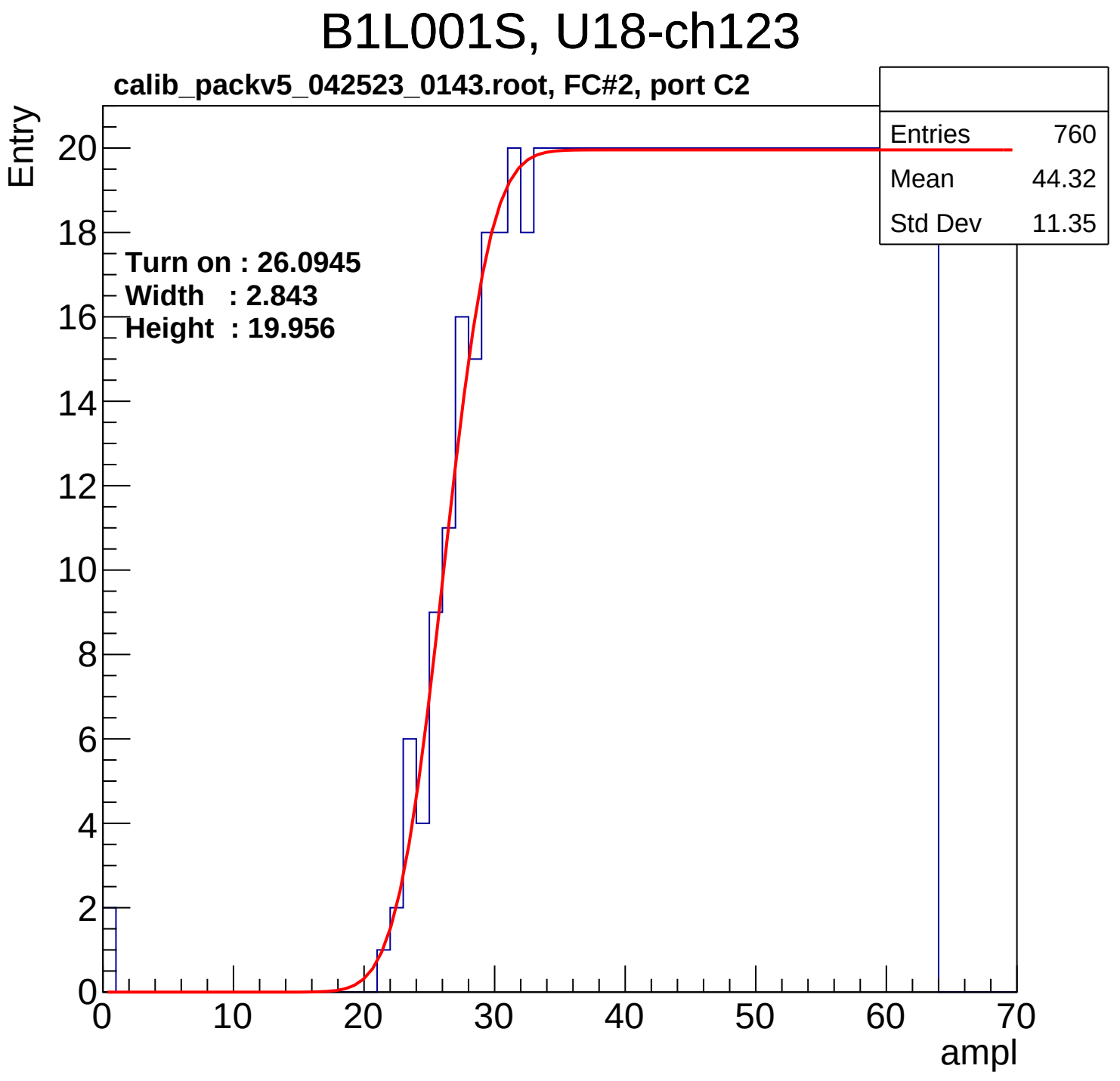
B1L001S, U18-ch123
calib_packv5_042523_0143.root, FC#2, port C2
Entries 760
Mean 44.32
Std Dev 11.35
Turn on : 26.0945
Width : 2.843
Height : 19.956
Entry
ampl
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6
8
10
12
14
16
18
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0
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20
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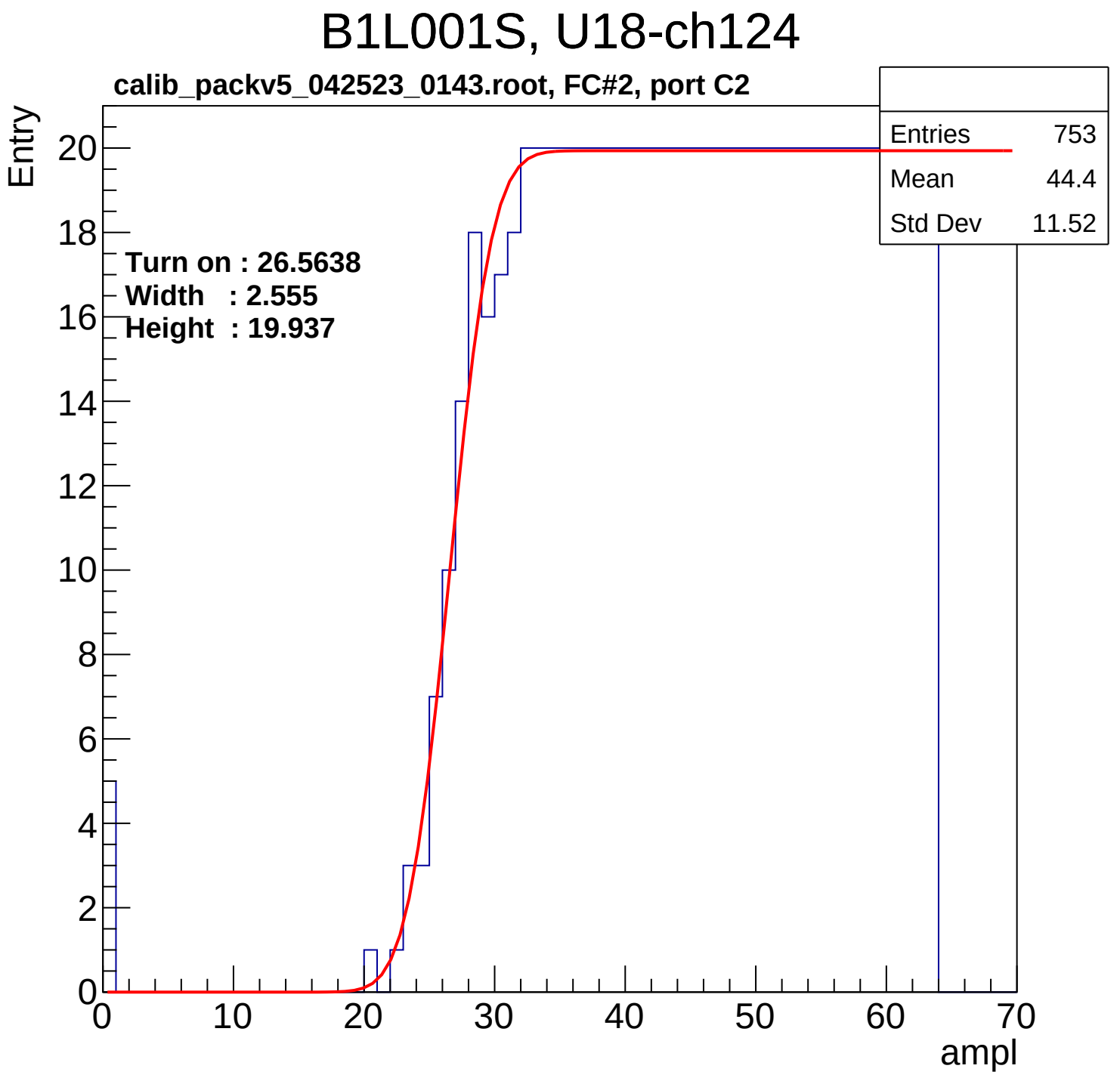
B1L001S, U18-ch124
calib_packv5_042523_0143.root, FC#2, port C2
Entries 753
Mean 44.4
Std Dev 11.52
Turn on : 26.5638
Width : 2.555
Height : 19.937
Entry
ampl
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6
8
10
12
14
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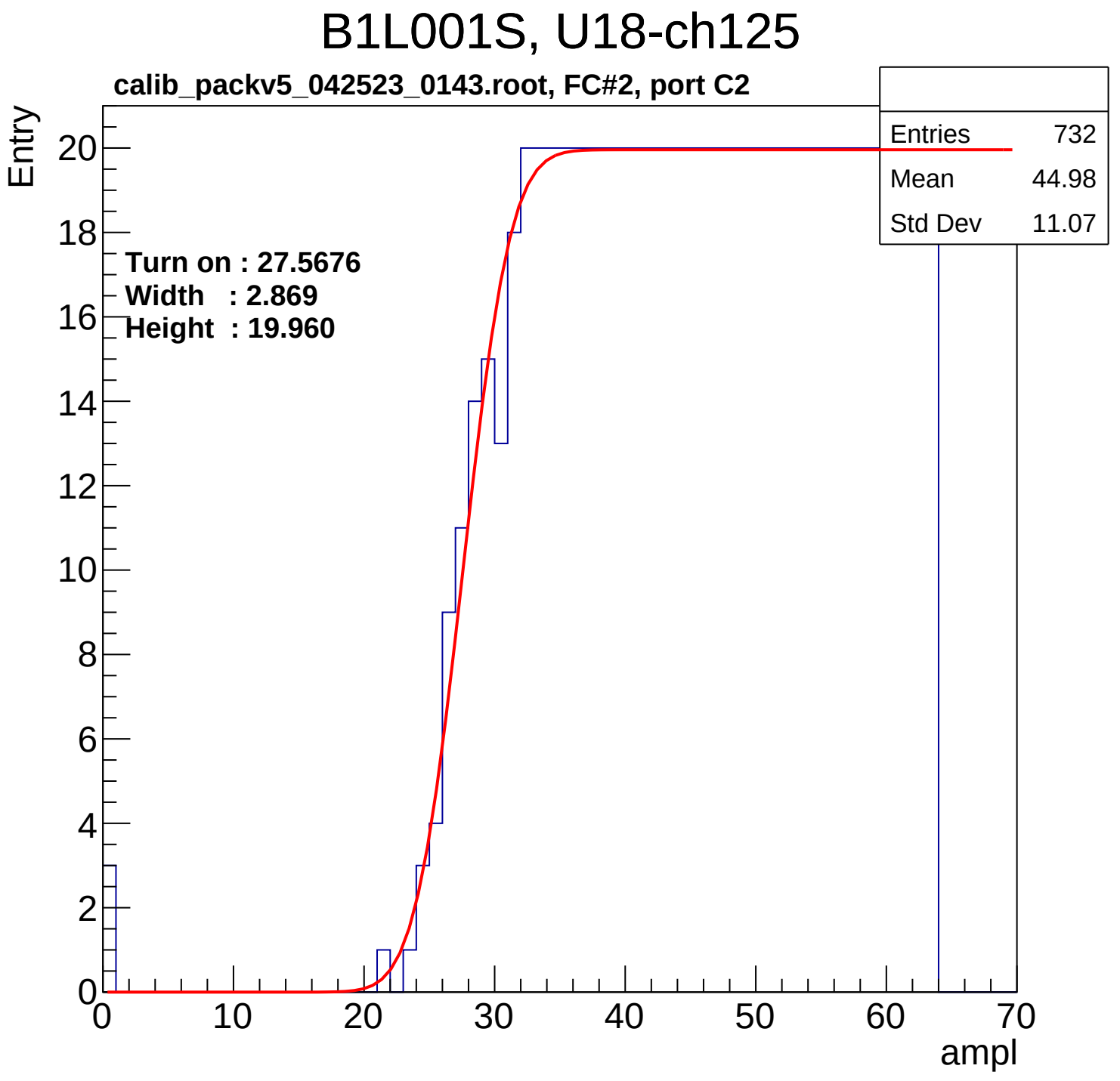
B1L001S, U18-ch125
calib_packv5_042523_0143.root, FC#2, port C2
Entries 732
Mean 44.98
Std Dev 11.07
Turn on : 27.5676
Width : 2.869
Height : 19.960
Entry
ampl
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6
8
10
12
14
16
18
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0
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20
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40
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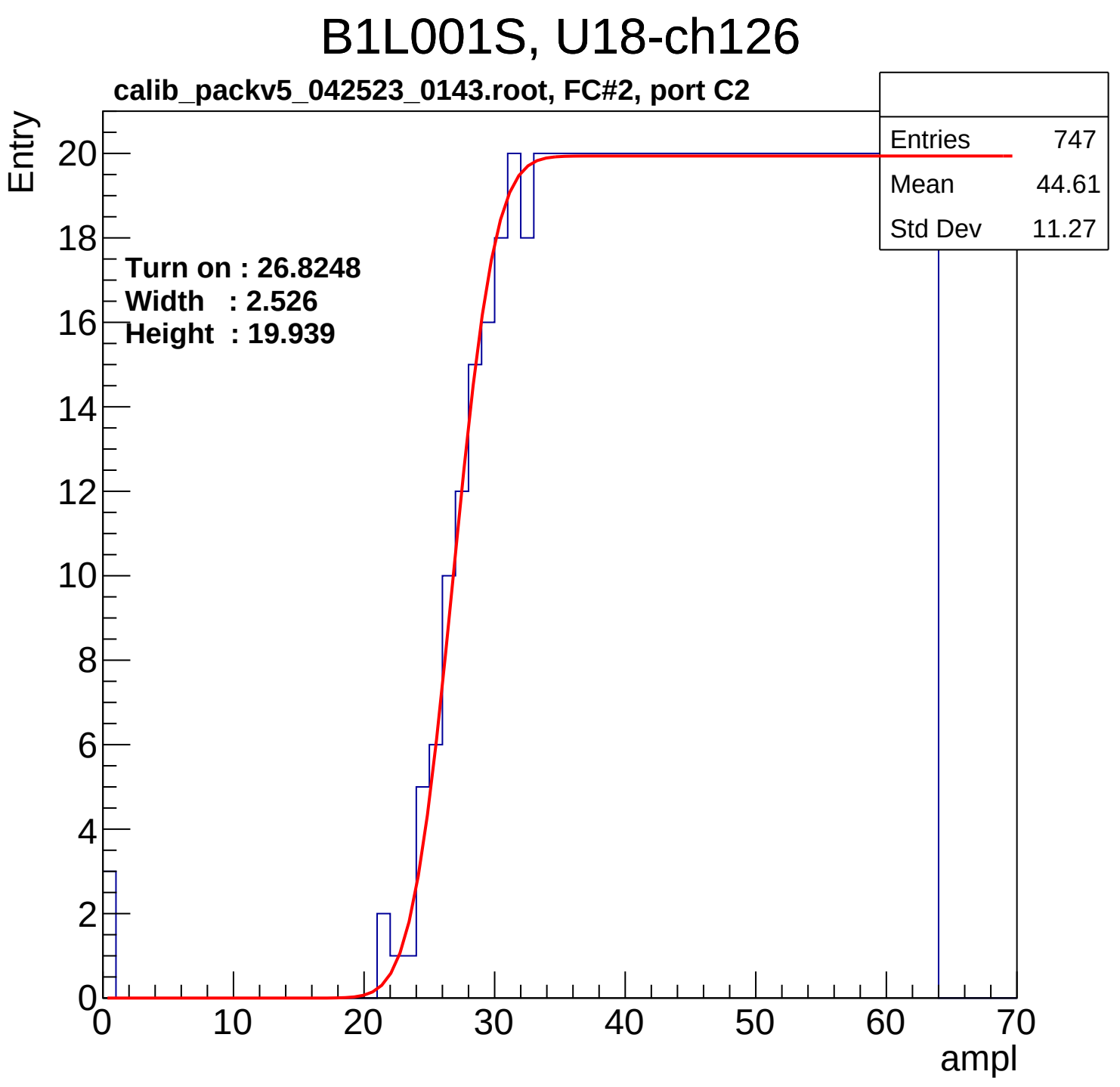
B1L001S, U18-ch126
calib_packv5_042523_0143.root, FC#2, port C2
Entries 747
Mean 44.61
Std Dev 11.27
Turn on : 26.8248
Width : 2.526
Height : 19.939
Entry
ampl
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6
8
10
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14
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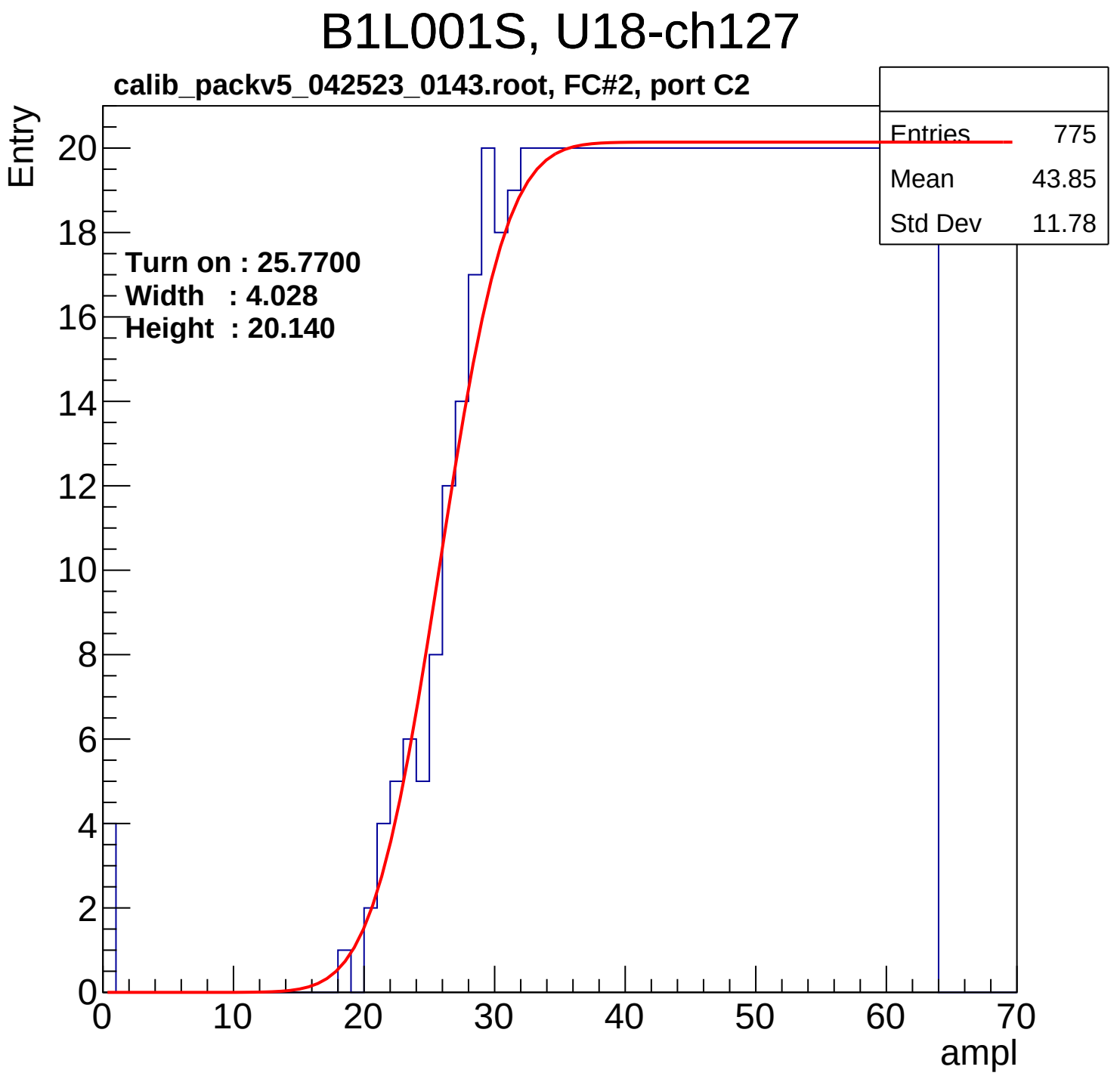
B1L001S, U18-ch127
calib_packv5_042523_0143.root, FC#2, port C2
Entries 775
Mean 43.85
Std Dev 11.78
Turn on : 25.7700
Width : 4.028
Height : 20.140
Entry
ampl
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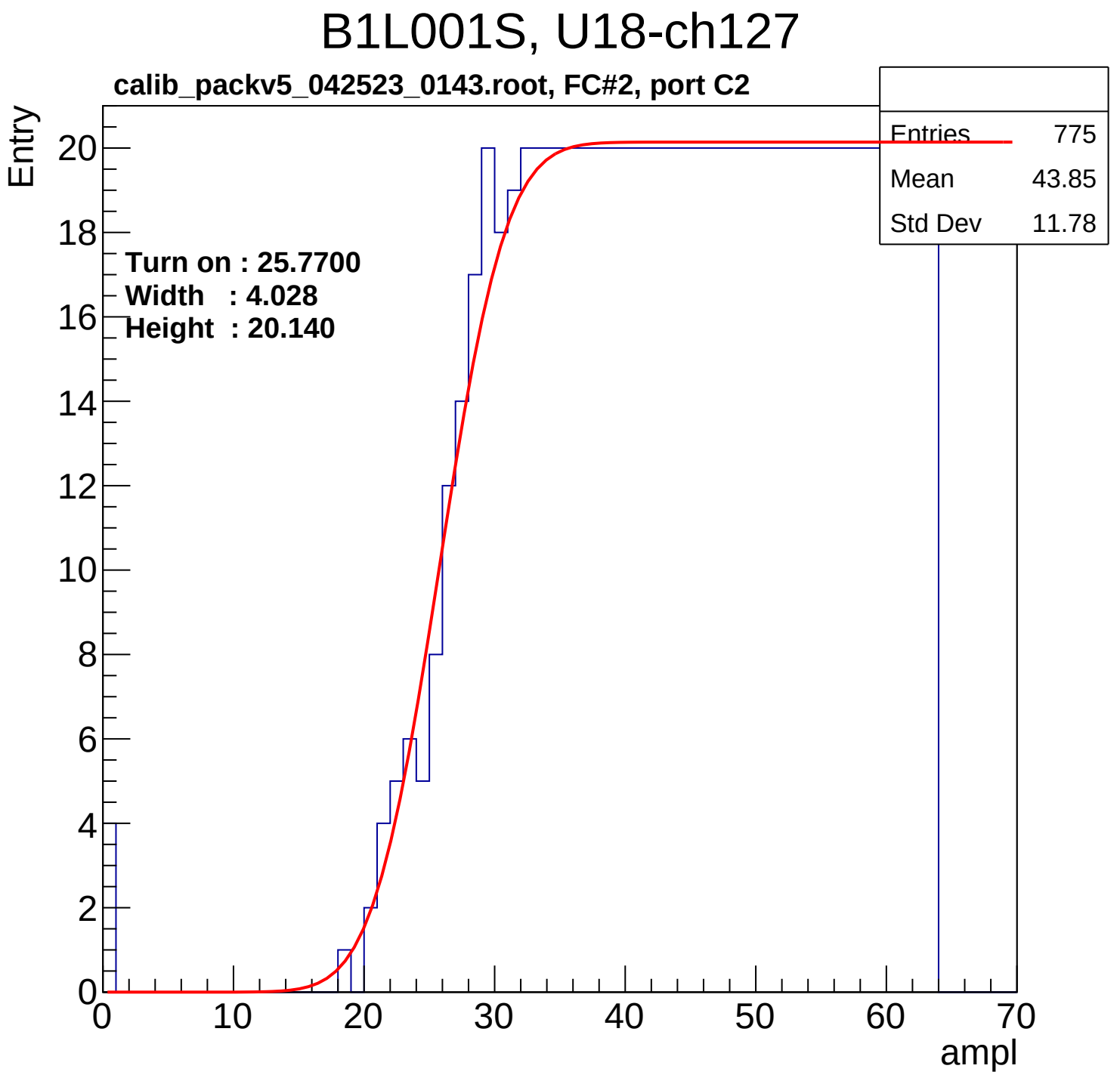
B1L001S, U18-ch127
calib_packv5_042523_0143.root, FC#2, port C2
Entries 775
Mean 43.85
Std Dev 11.78
Turn on : 25.7700
Width : 4.028
Height : 20.140
Entry
ampl
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4
6
8
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