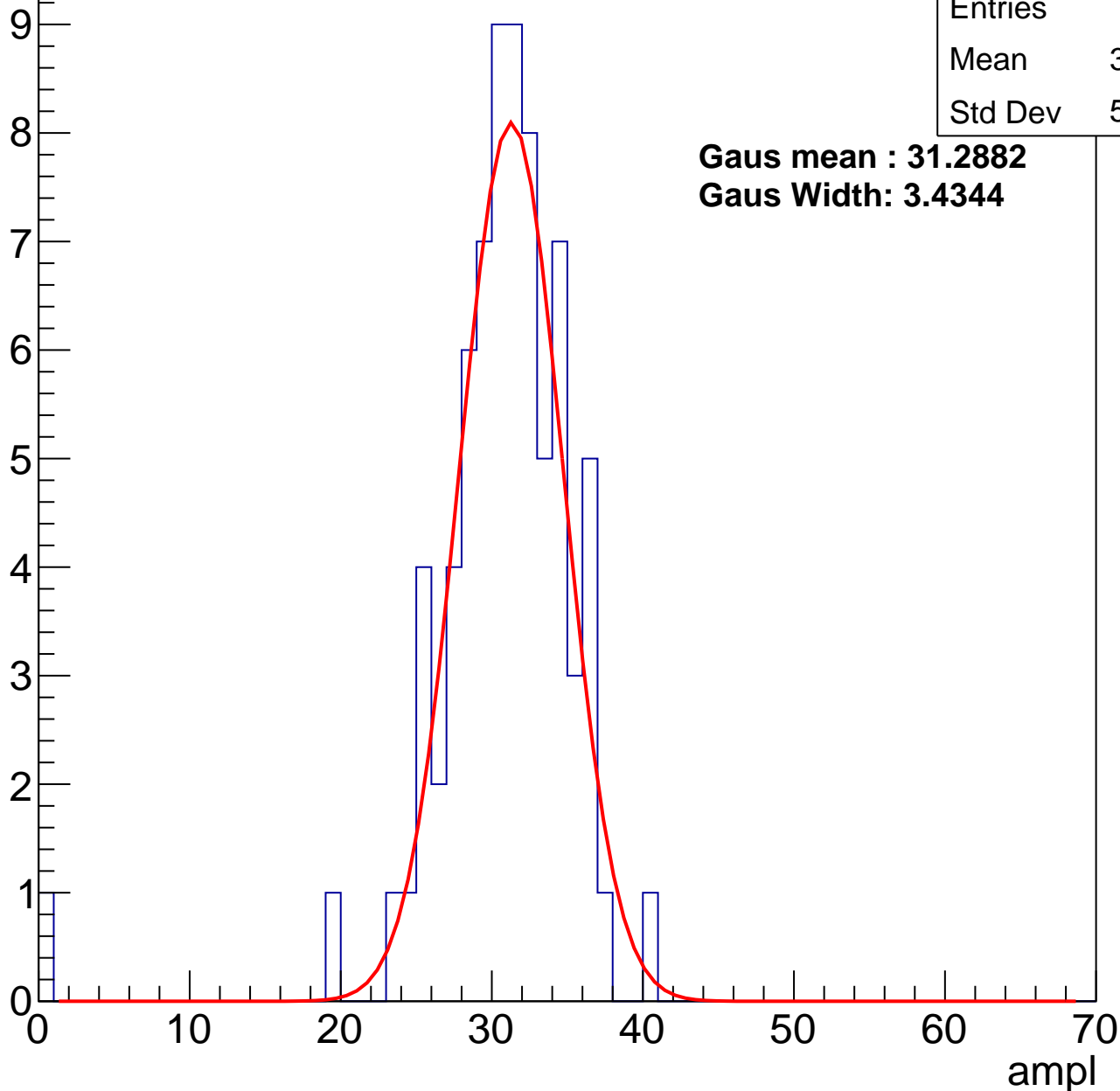




# B1L100S, U6-ch0, adc0

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



# B1L100S, U6-ch0, adc1

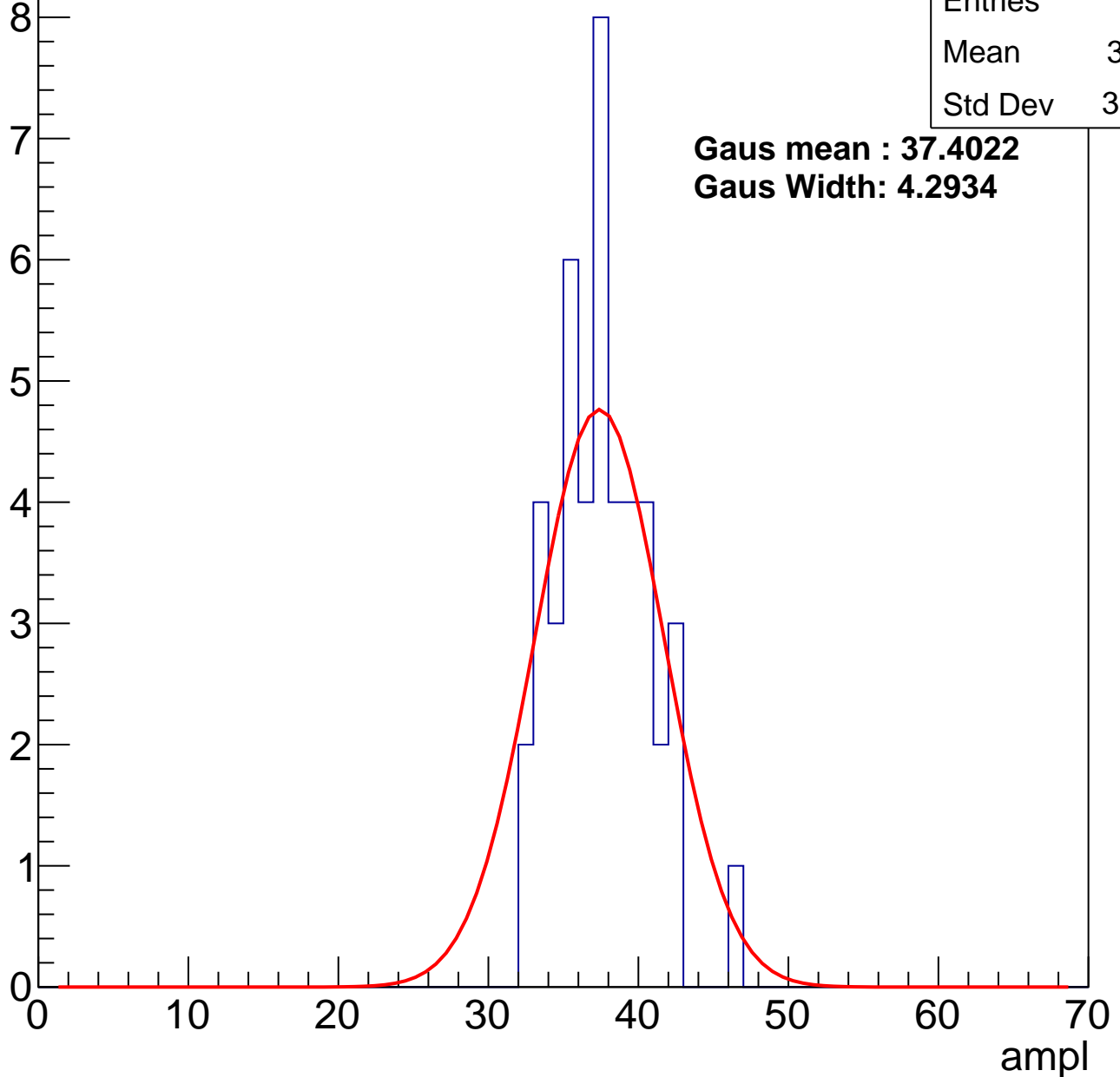
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	45
Mean	37.11
Std Dev	3.027

**Gaus mean : 37.4022**

**Gaus Width: 4.2934**



# B1L100S, U6-ch0, adc2

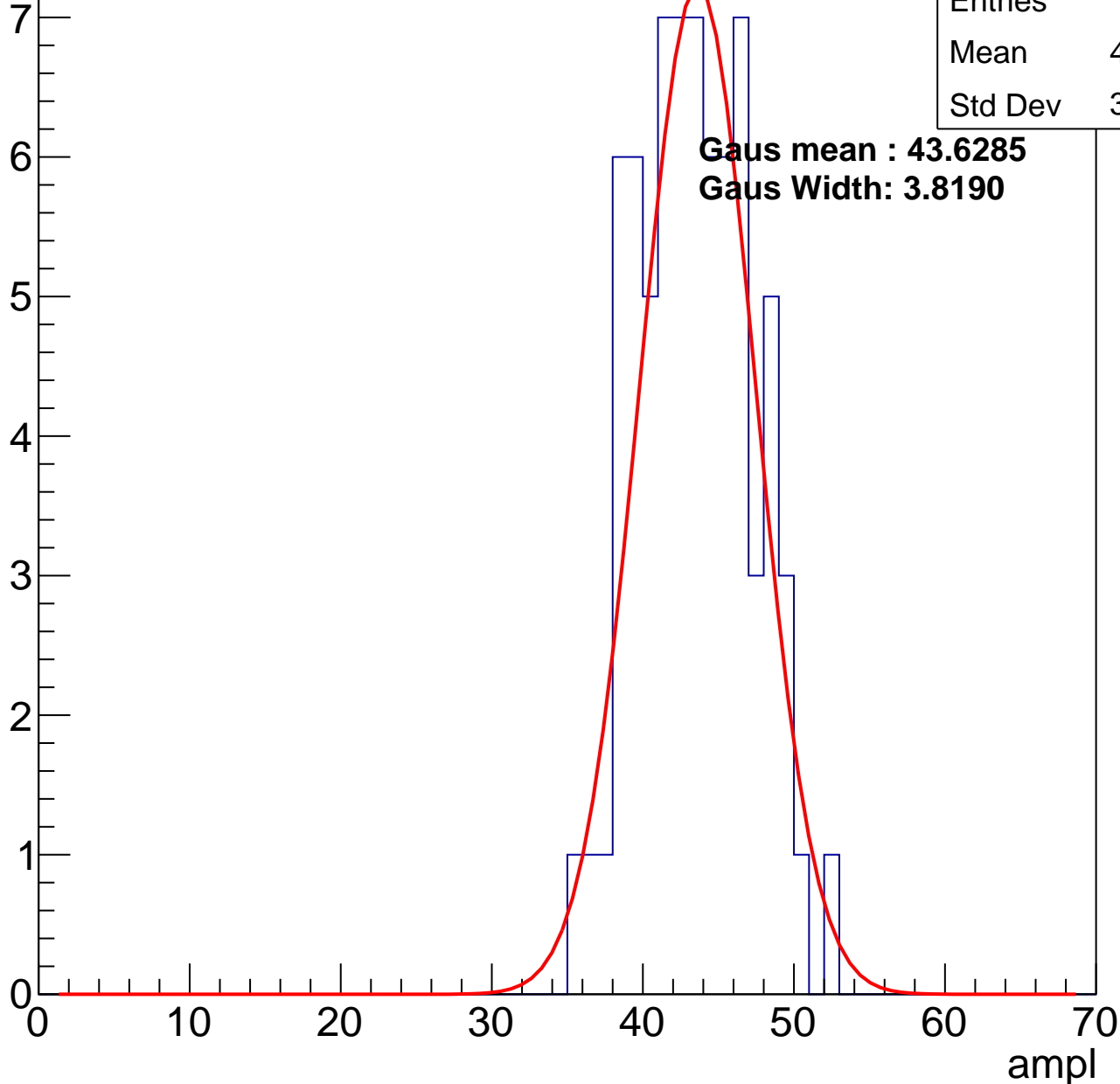
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	73
Mean	42.99
Std Dev	3.662

**Gaus mean : 43.6285**

**Gaus Width: 3.8190**

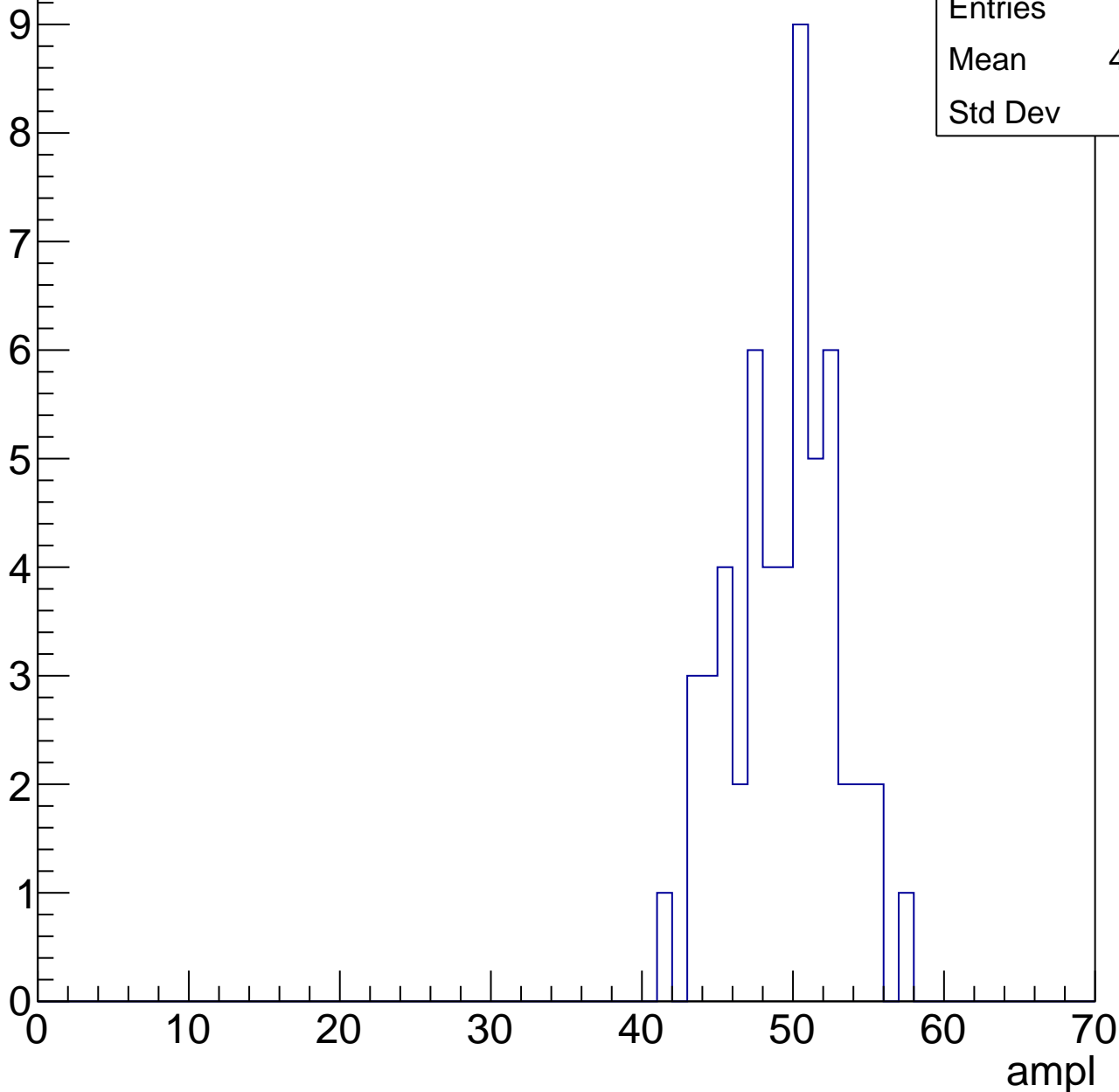


# B1L100S, U6-ch0, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

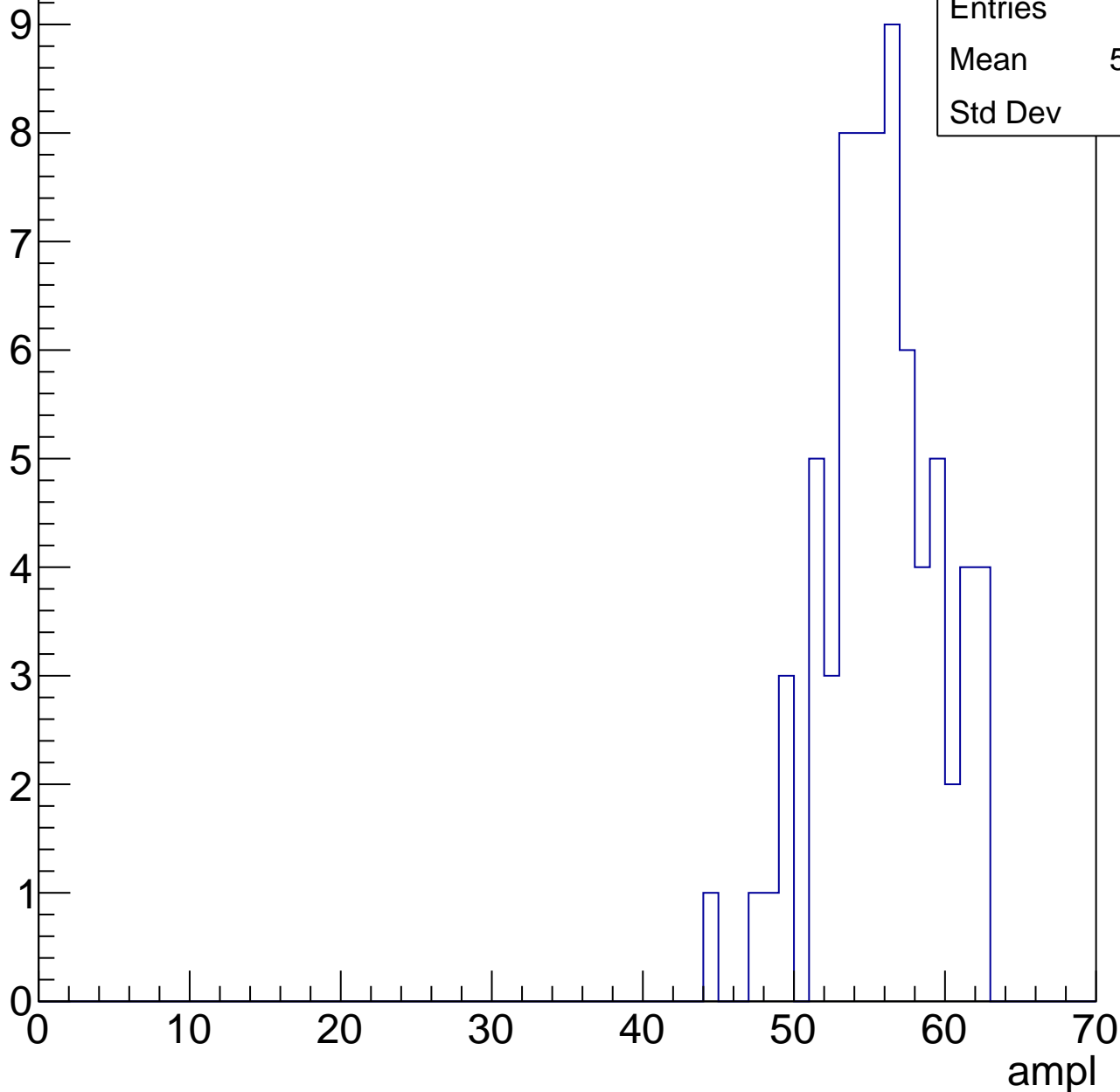
Entries	54
Mean	48.93
Std Dev	3.49



# B1L100S, U6-ch0, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	72
Mean	55.25
Std Dev	3.77

# B1L100S, U6-ch0, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

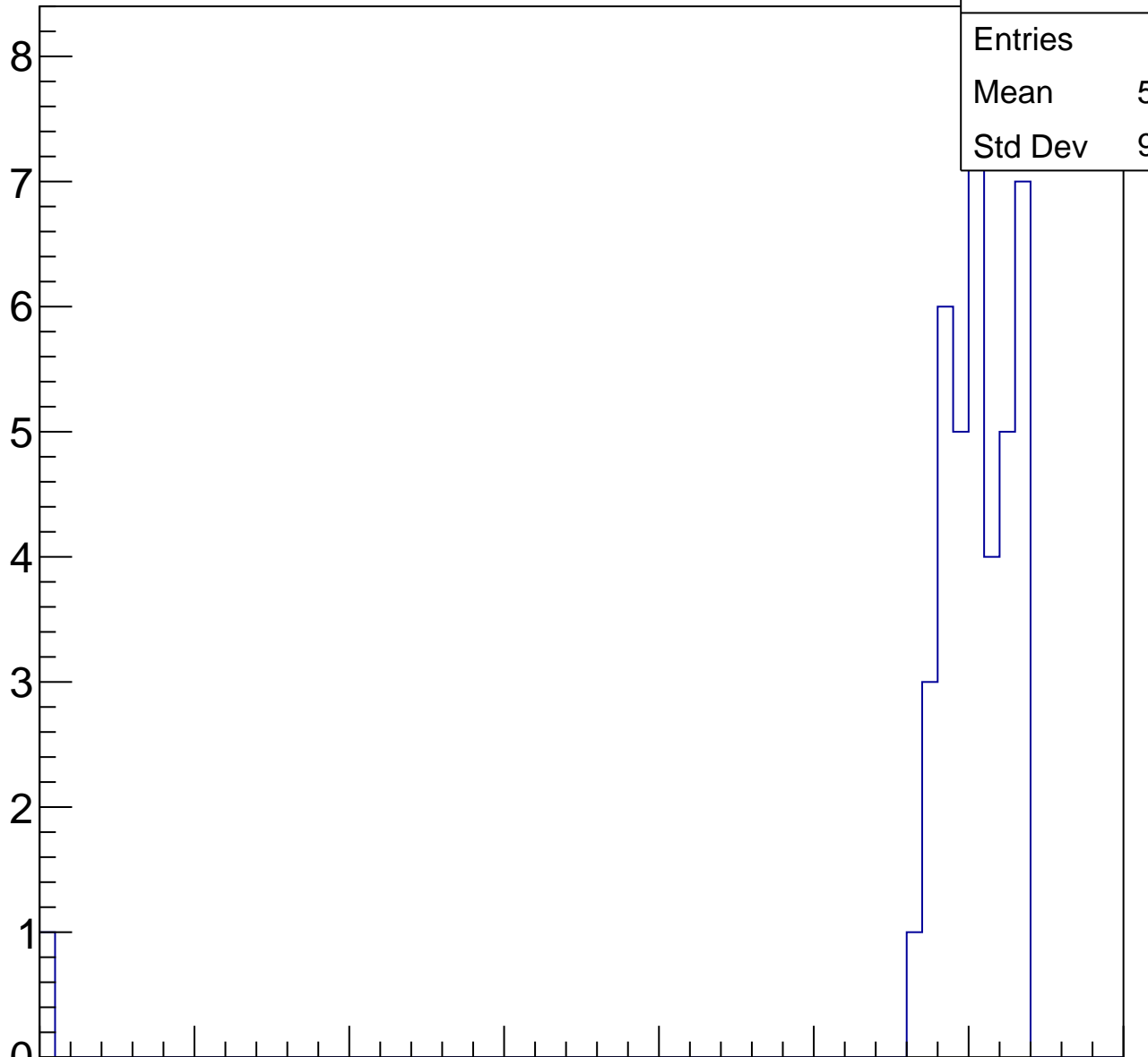
Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	40
Mean	58.62
Std Dev	9.596

ampl

0 10 20 30 40 50 60 70



# B1L100S, U6-ch0, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry





# B1L100S, U6-ch0, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L100S, U6-ch1, adc0

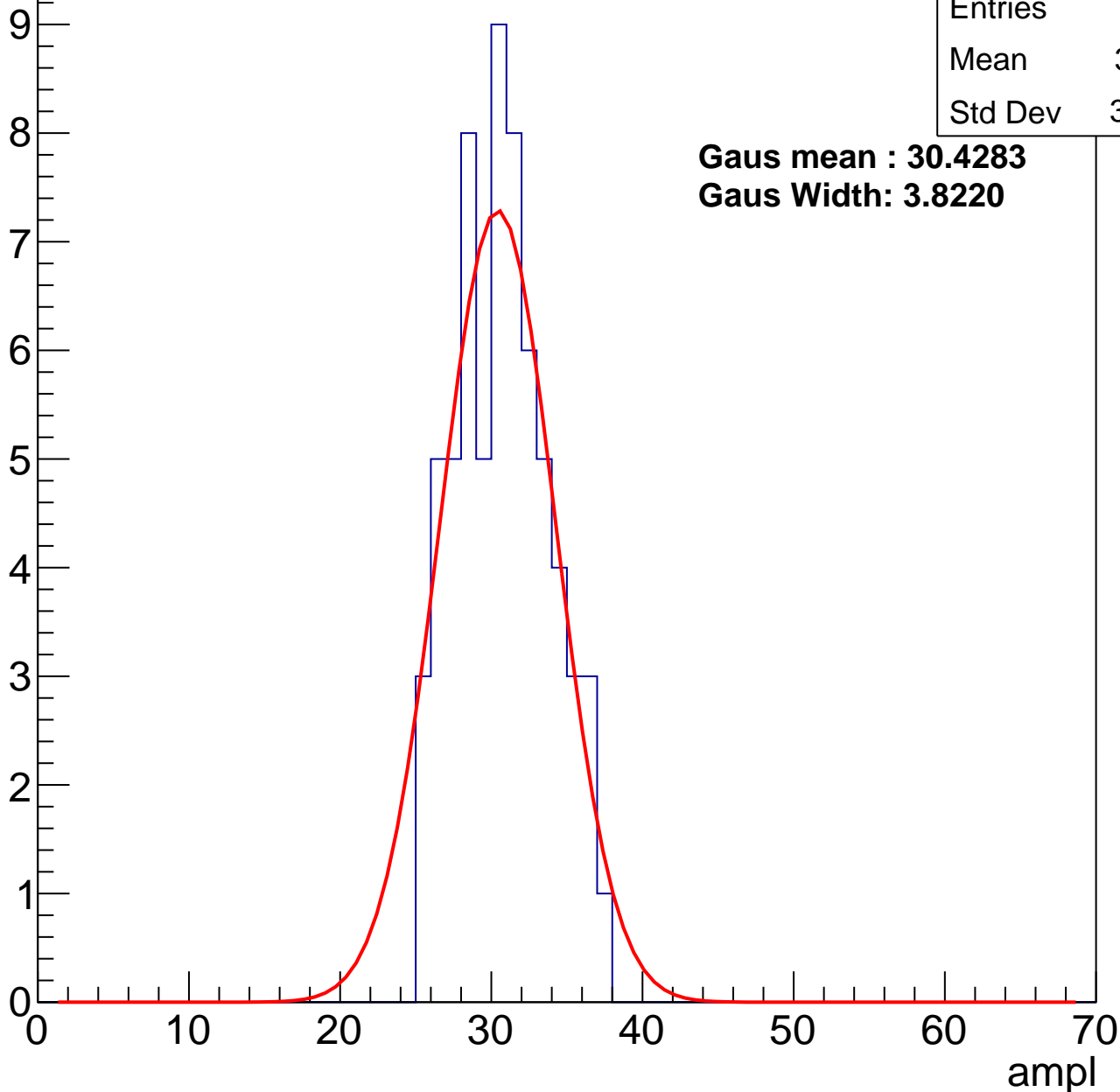
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	65
Mean	30.31
Std Dev	3.048

**Gaus mean : 30.4283**

**Gaus Width: 3.8220**



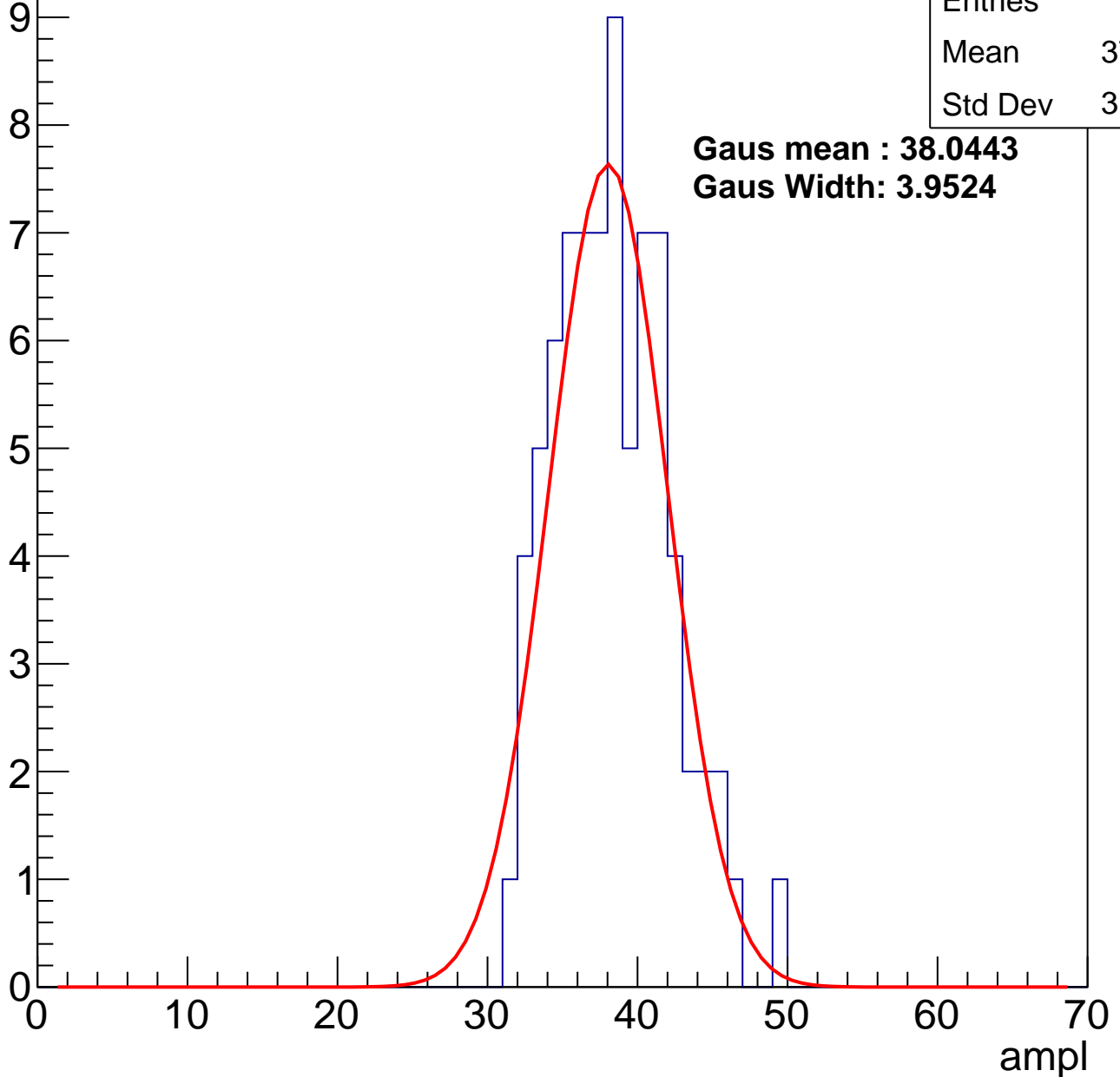
# B1L100S, U6-ch1, adc1

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	77
Mean	37.86
Std Dev	3.737

**Gaus mean : 38.0443**  
**Gaus Width: 3.9524**



# B1L100S, U6-ch1, adc2

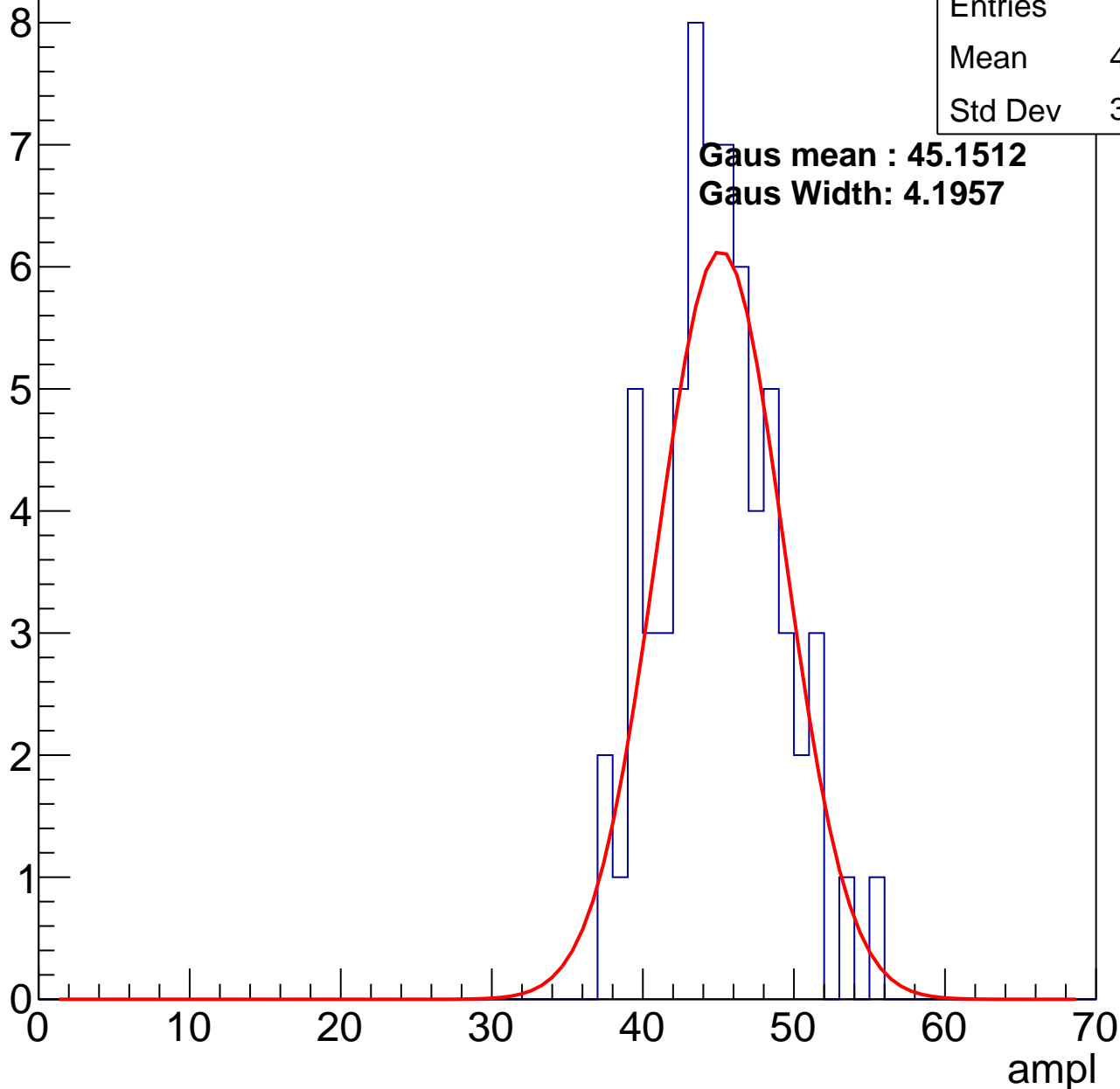
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	66
Mean	44.53
Std Dev	3.866

**Gaus mean : 45.1512**

**Gaus Width: 4.1957**

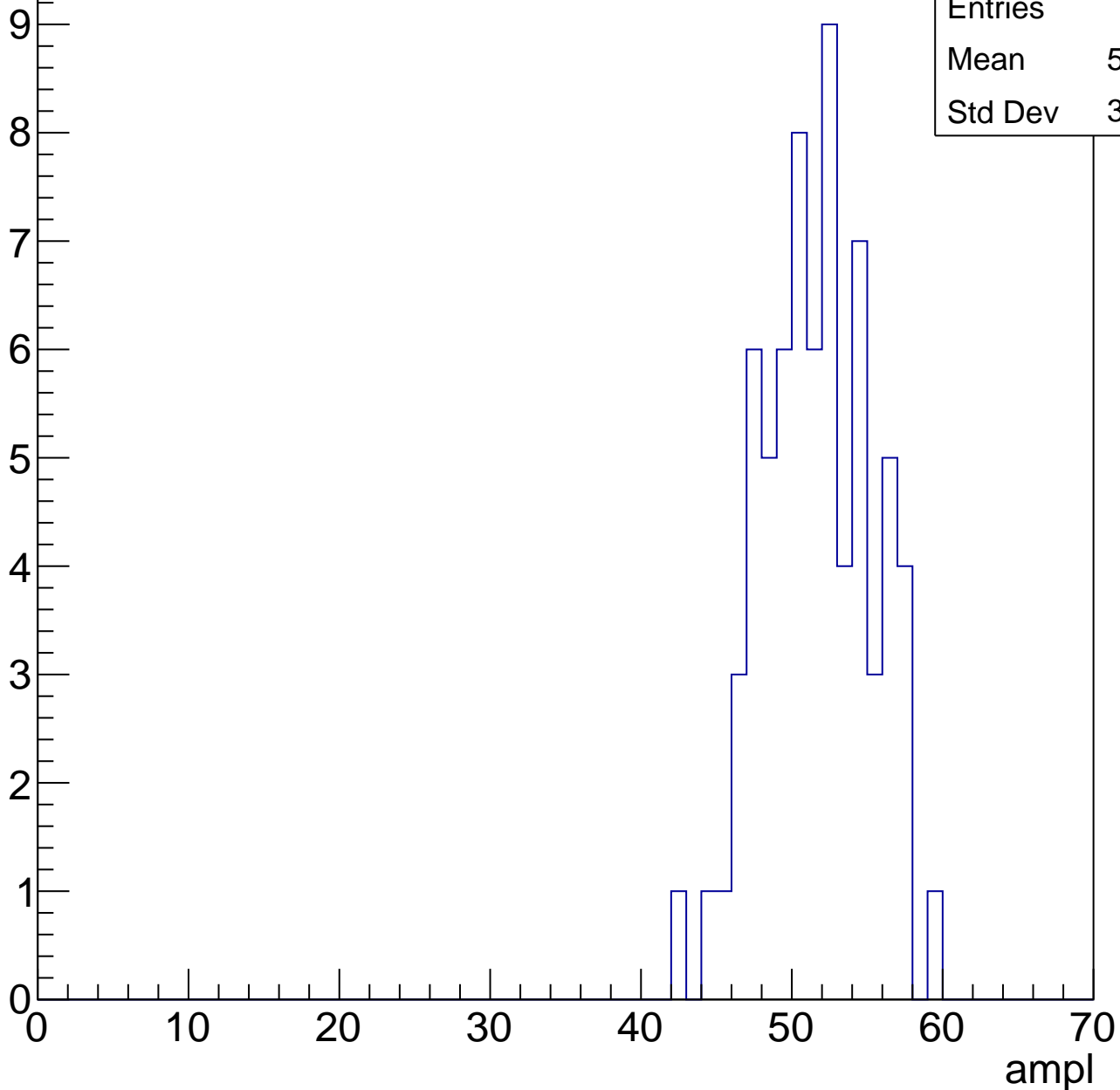


# B1L100S, U6-ch1, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

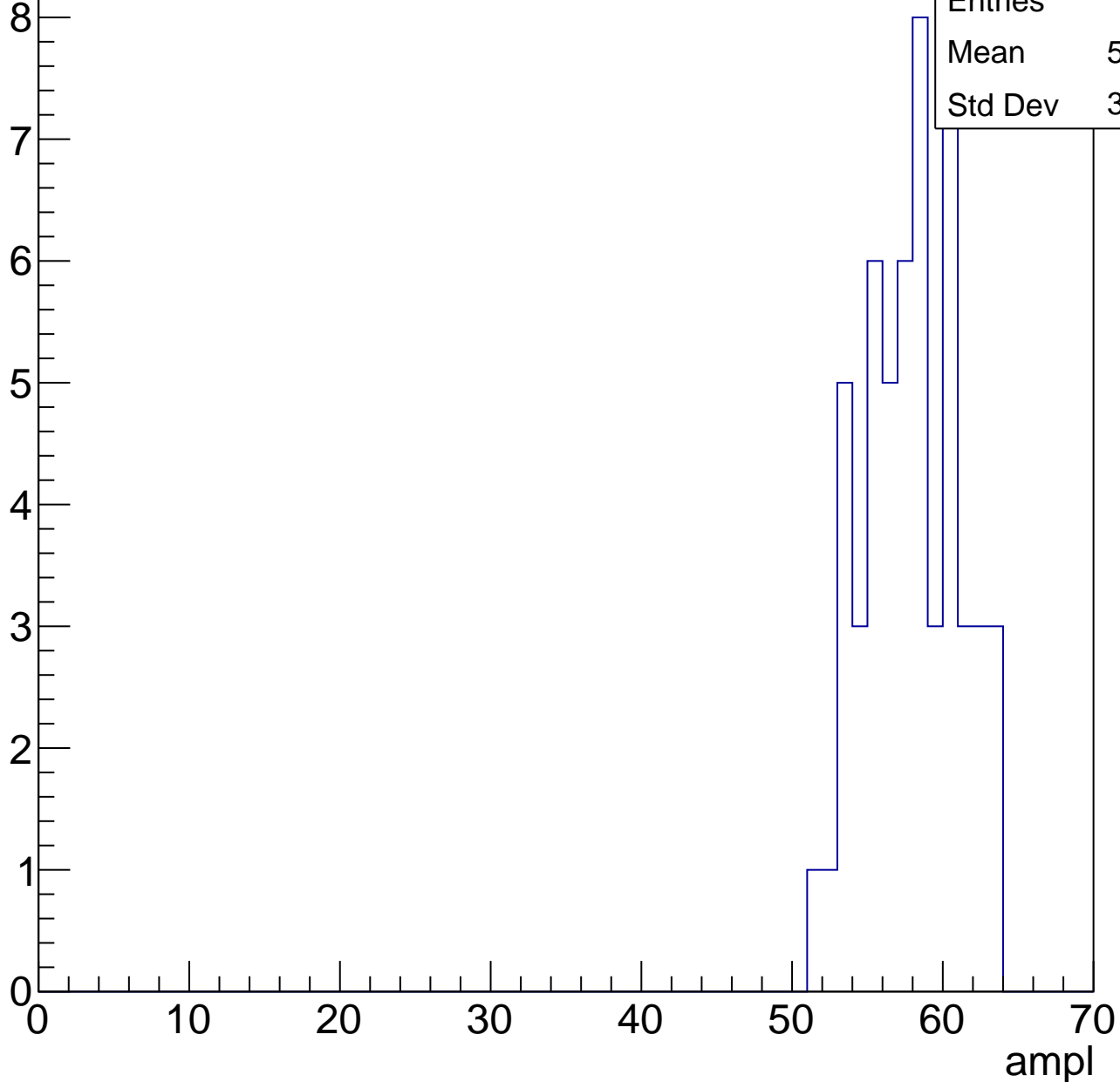
Entries	70
Mean	51.16
Std Dev	3.548



# B1L100S, U6-ch1, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

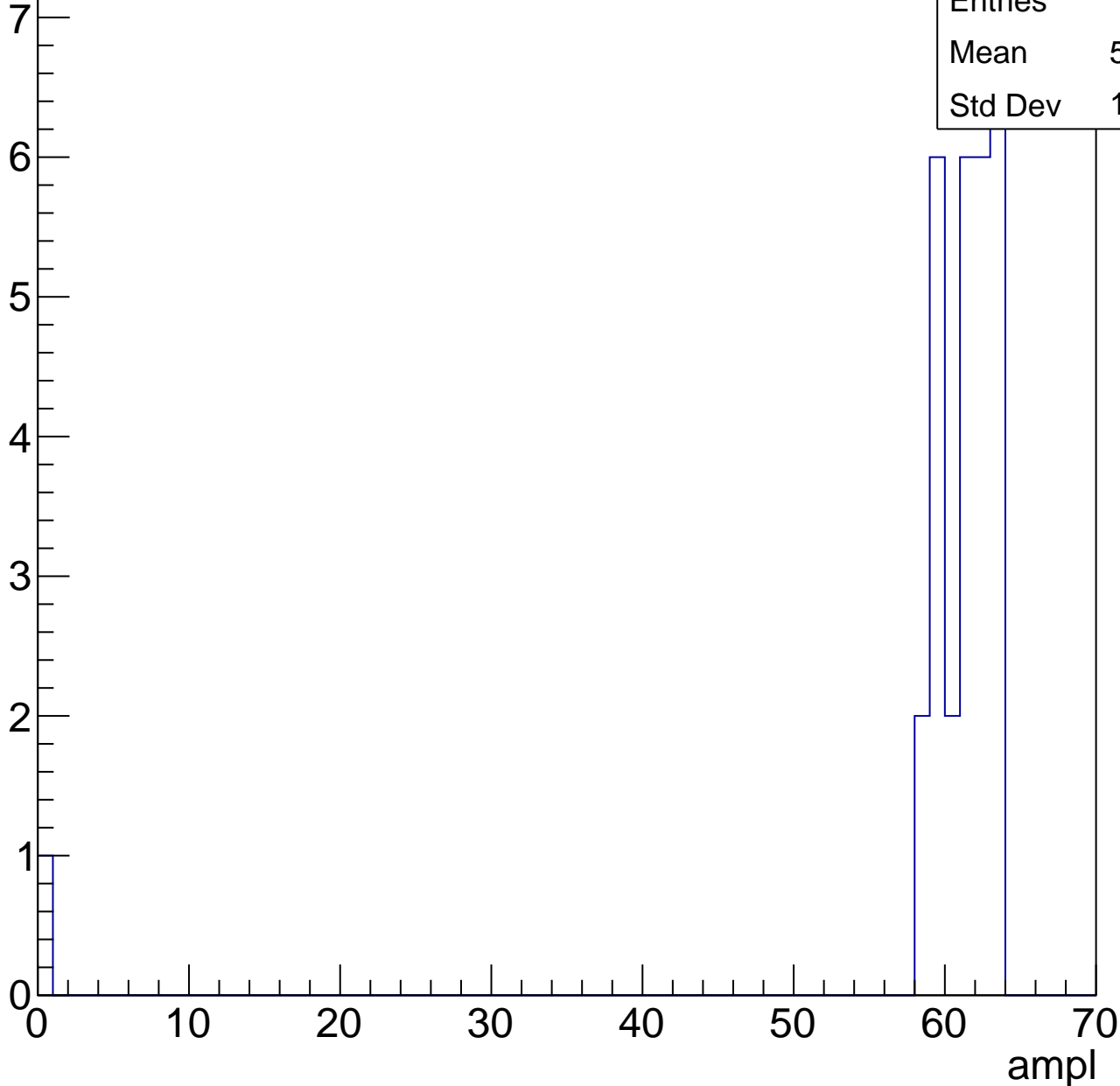


# B1L100S, U6-ch1, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	30
Mean	58.97
Std Dev	11.07



# B1L100S, U6-ch1, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry





# B1L100S, U6-ch1, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

1  
0.8  
0.6  
0.4  
0.2  
0

Entries	1
Mean	21
Std Dev	0

ampl

0 10 20 30 40 50 60 70

# B1L100S, U6-ch2, adc0

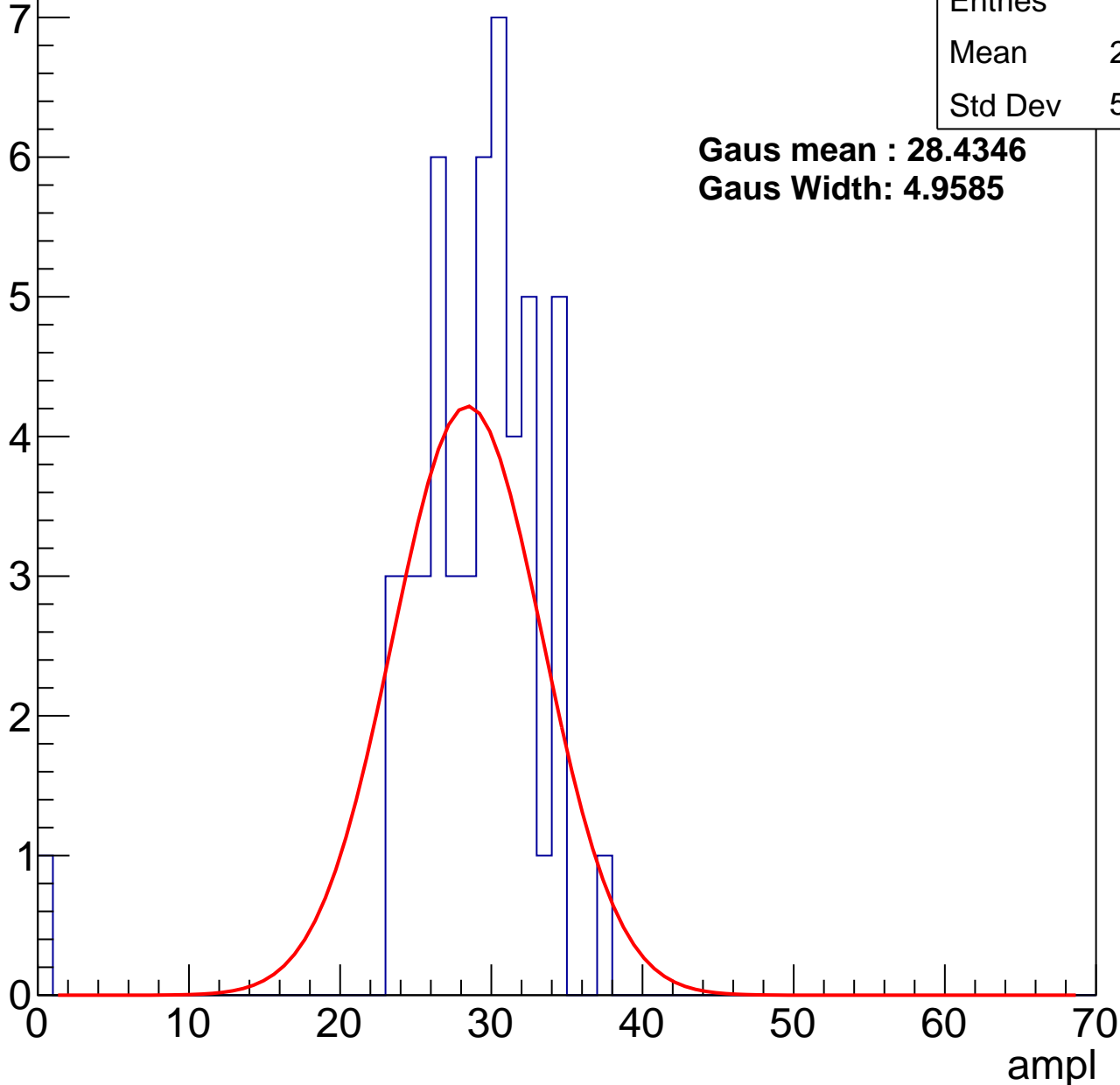
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	51
Mean	28.33
Std Dev	5.223

**Gaus mean : 28.4346**

**Gaus Width: 4.9585**



# B1L100S, U6-ch2, adc1

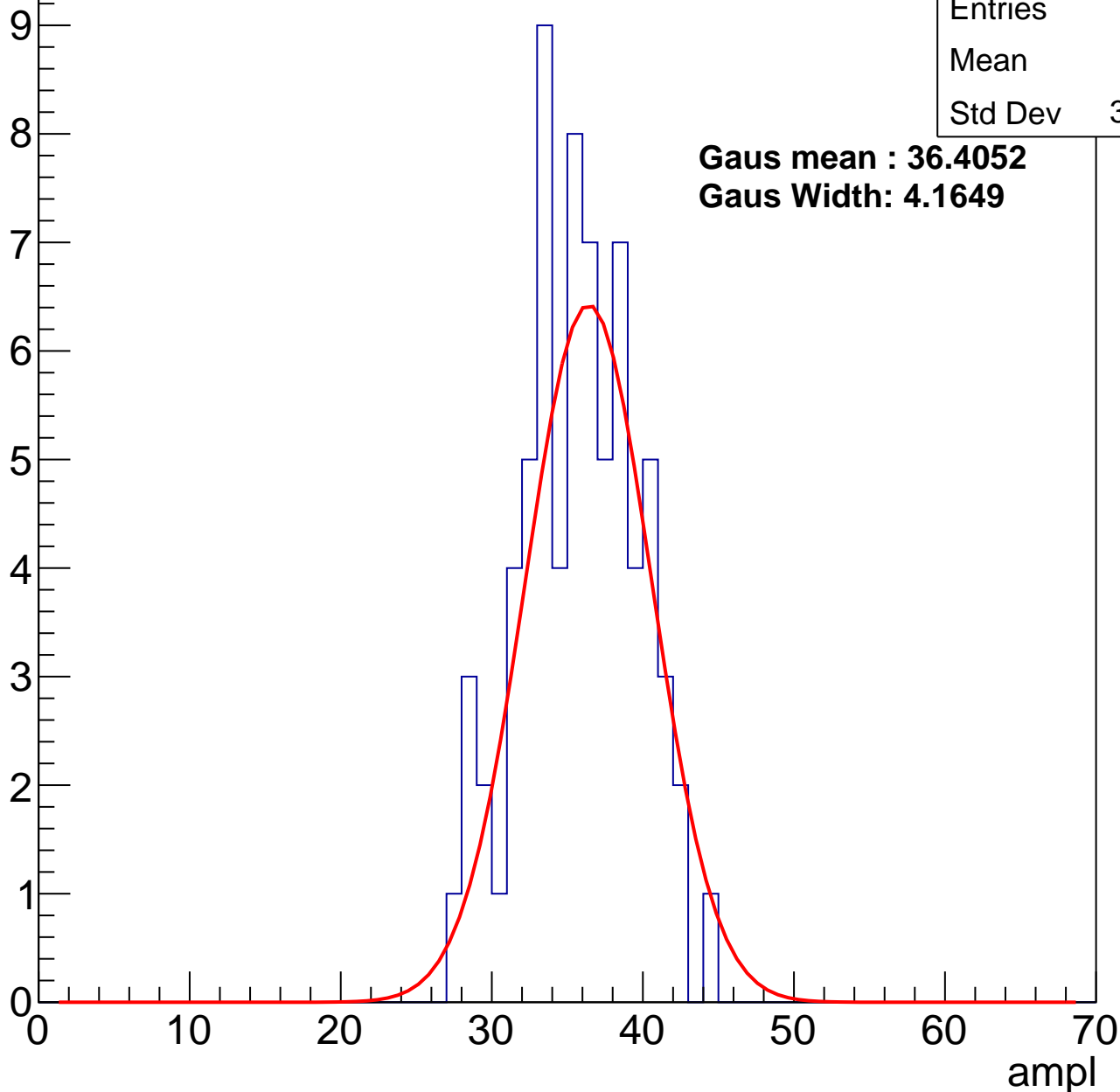
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	71
Mean	35.3
Std Dev	3.784

**Gaus mean : 36.4052**

**Gaus Width: 4.1649**



# B1L100S, U6-ch2, adc2

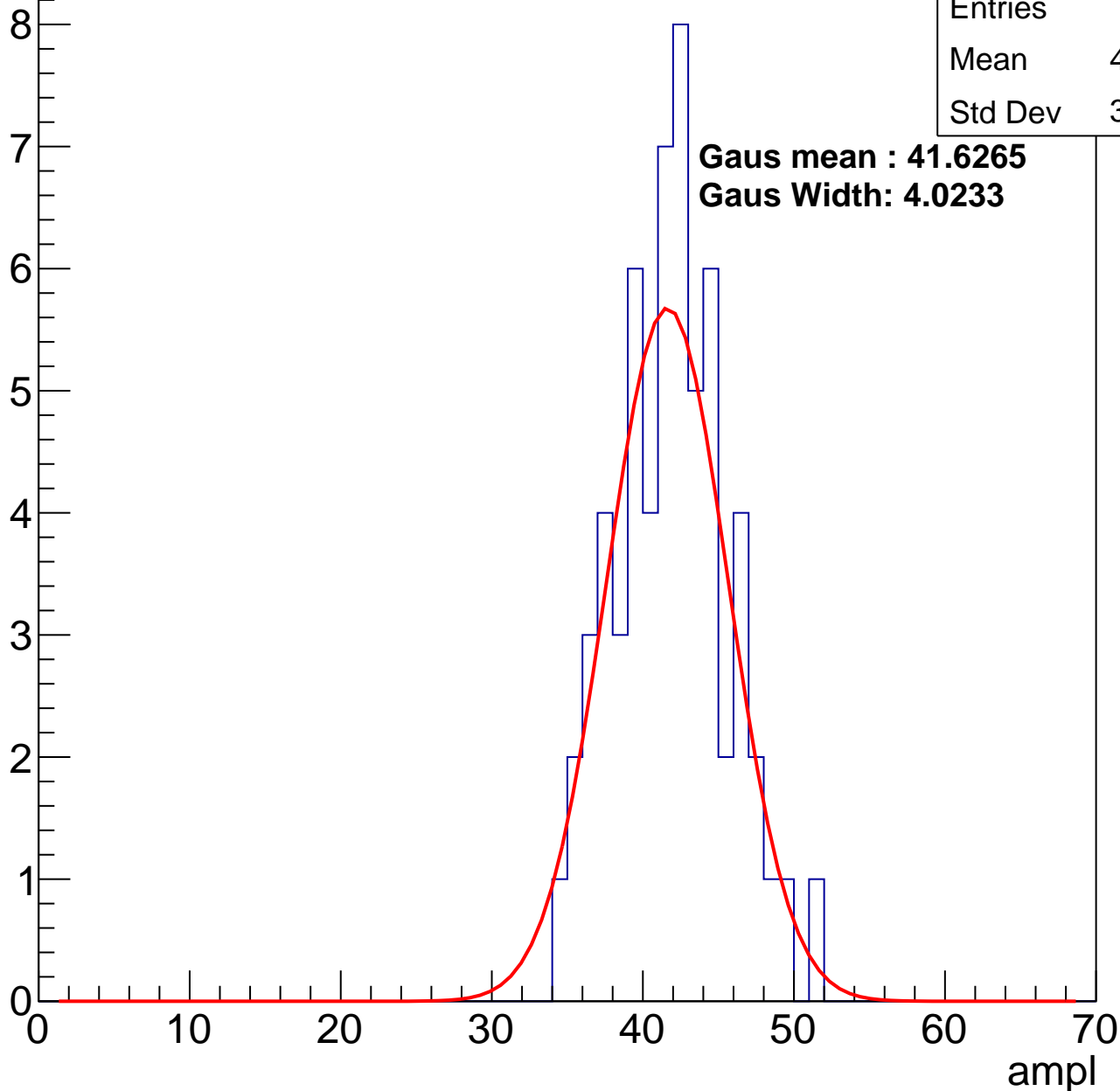
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	60
Mean	41.43
Std Dev	3.658

**Gaus mean : 41.6265**

**Gaus Width: 4.0233**

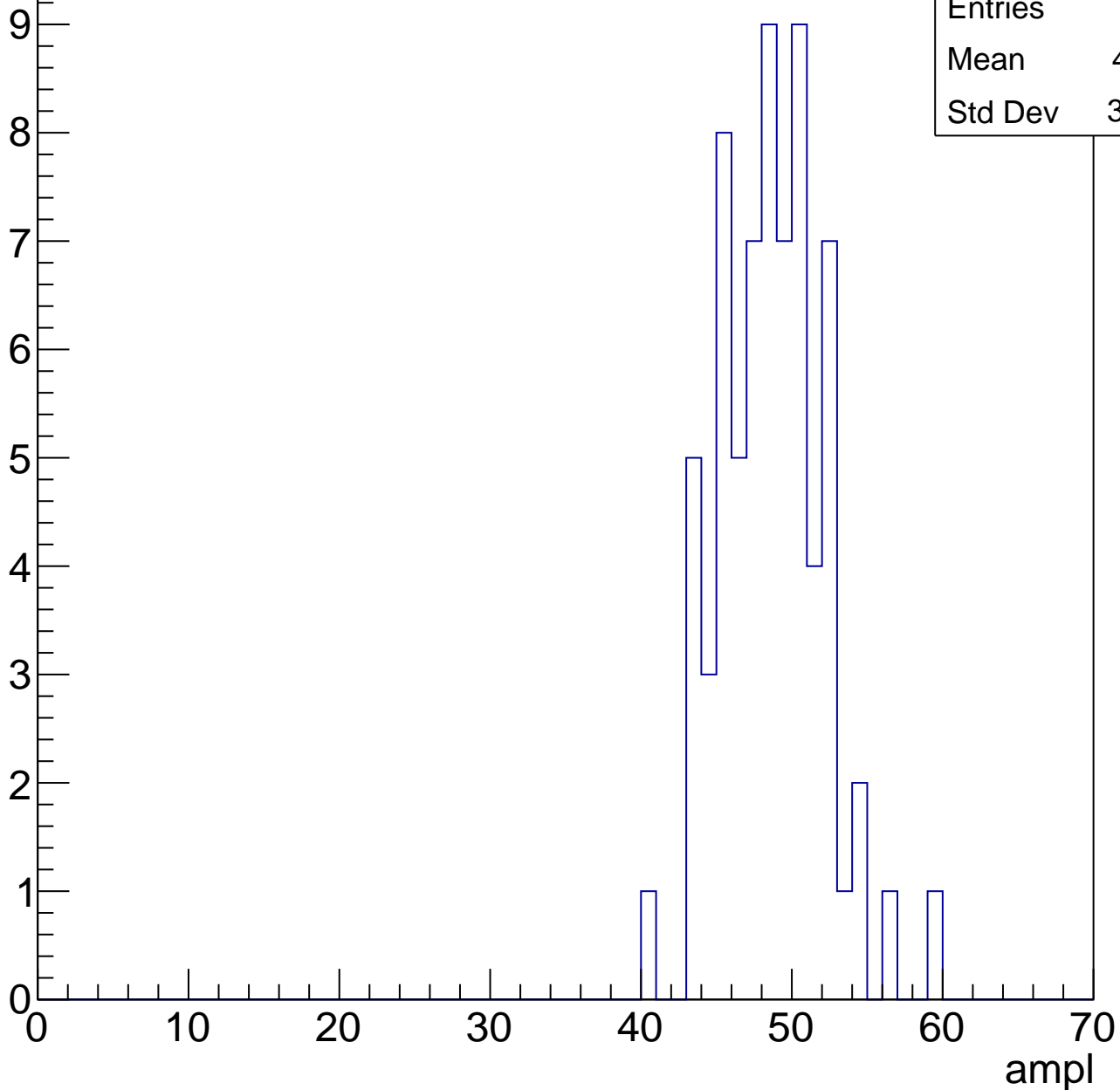


# B1L100S, U6-ch2, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	70
Mean	48.21
Std Dev	3.393

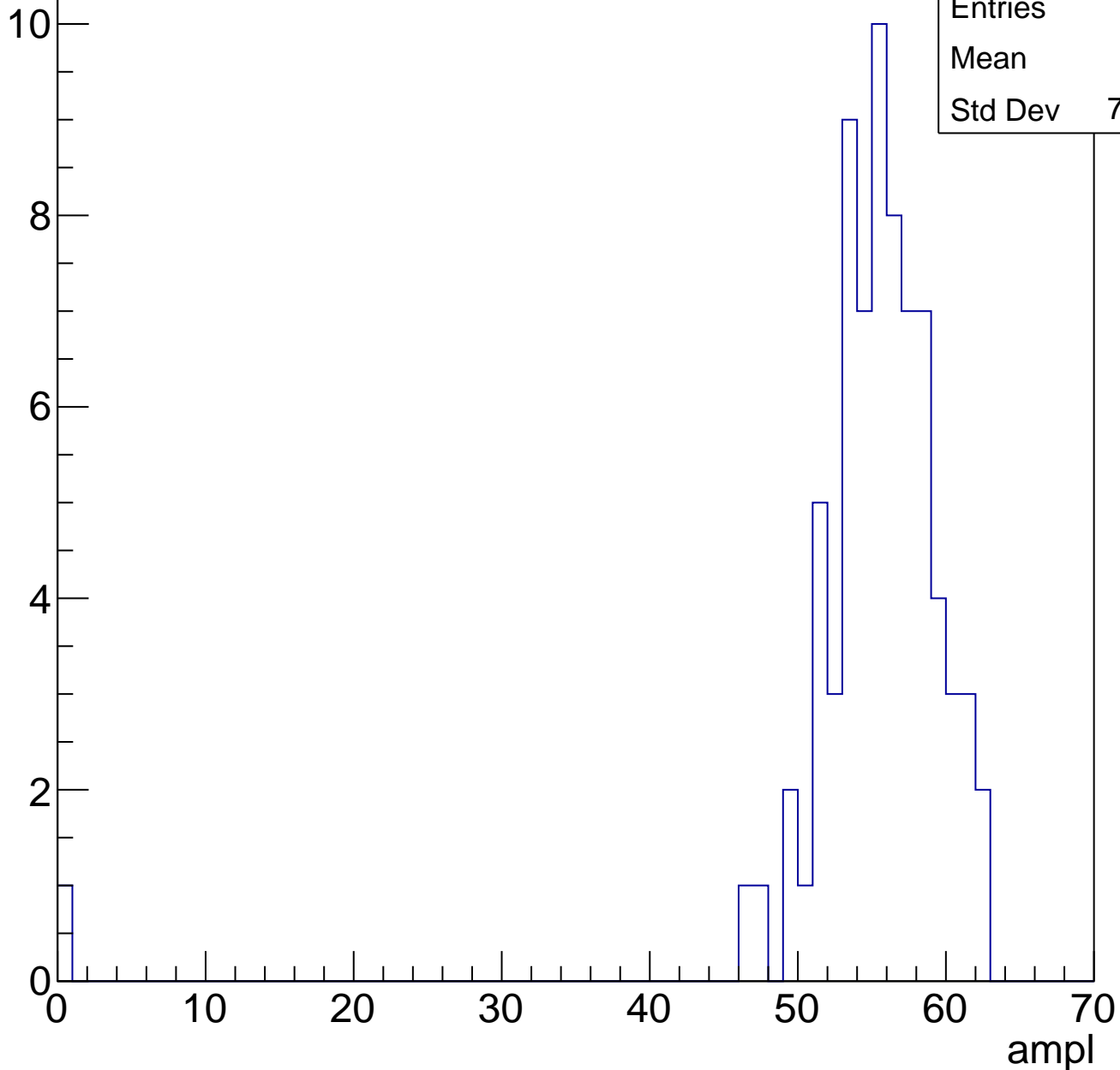


# B1L100S, U6-ch2, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	74
Mean	54.5
Std Dev	7.206

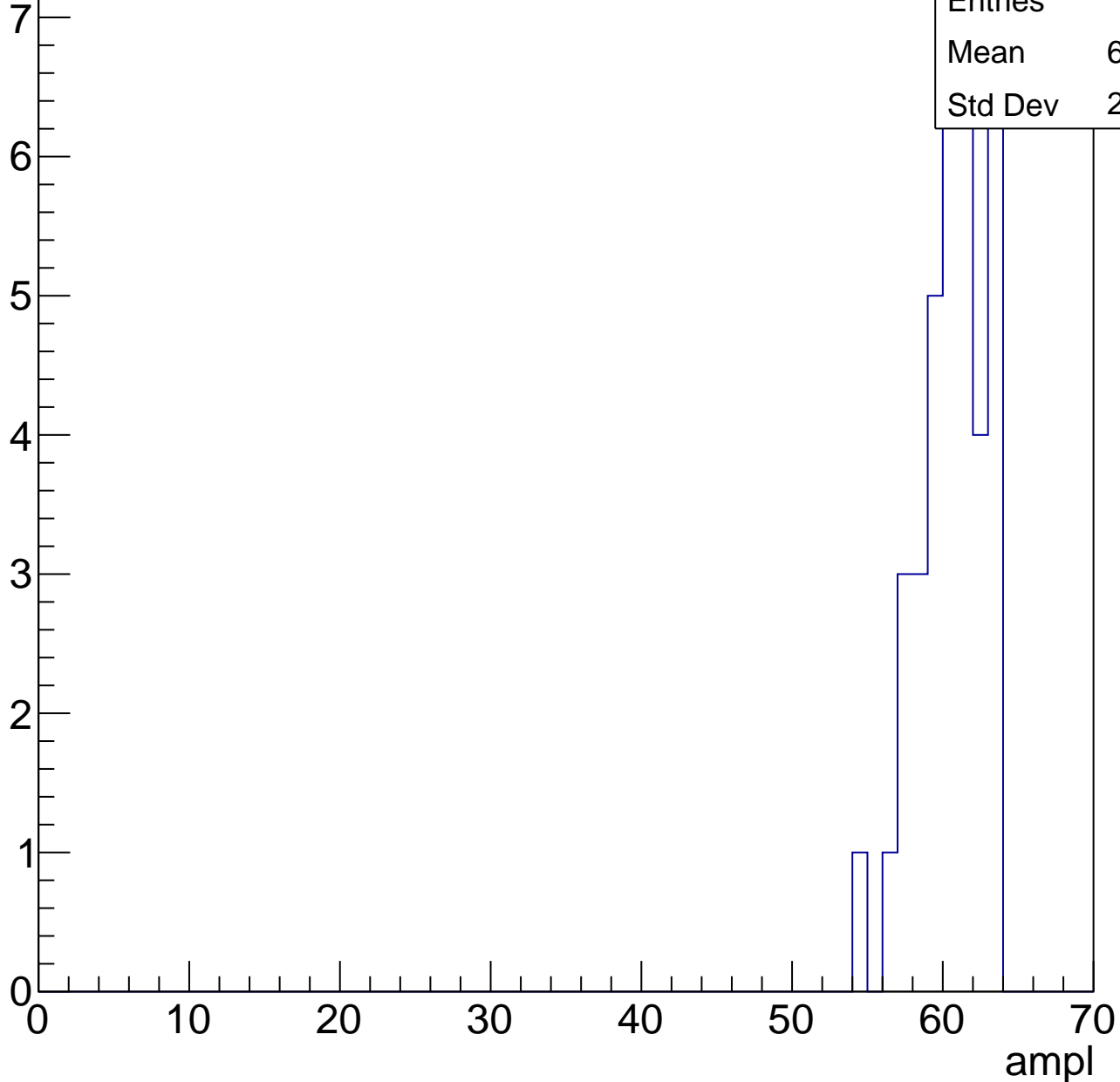
Entry



# B1L100S, U6-ch2, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

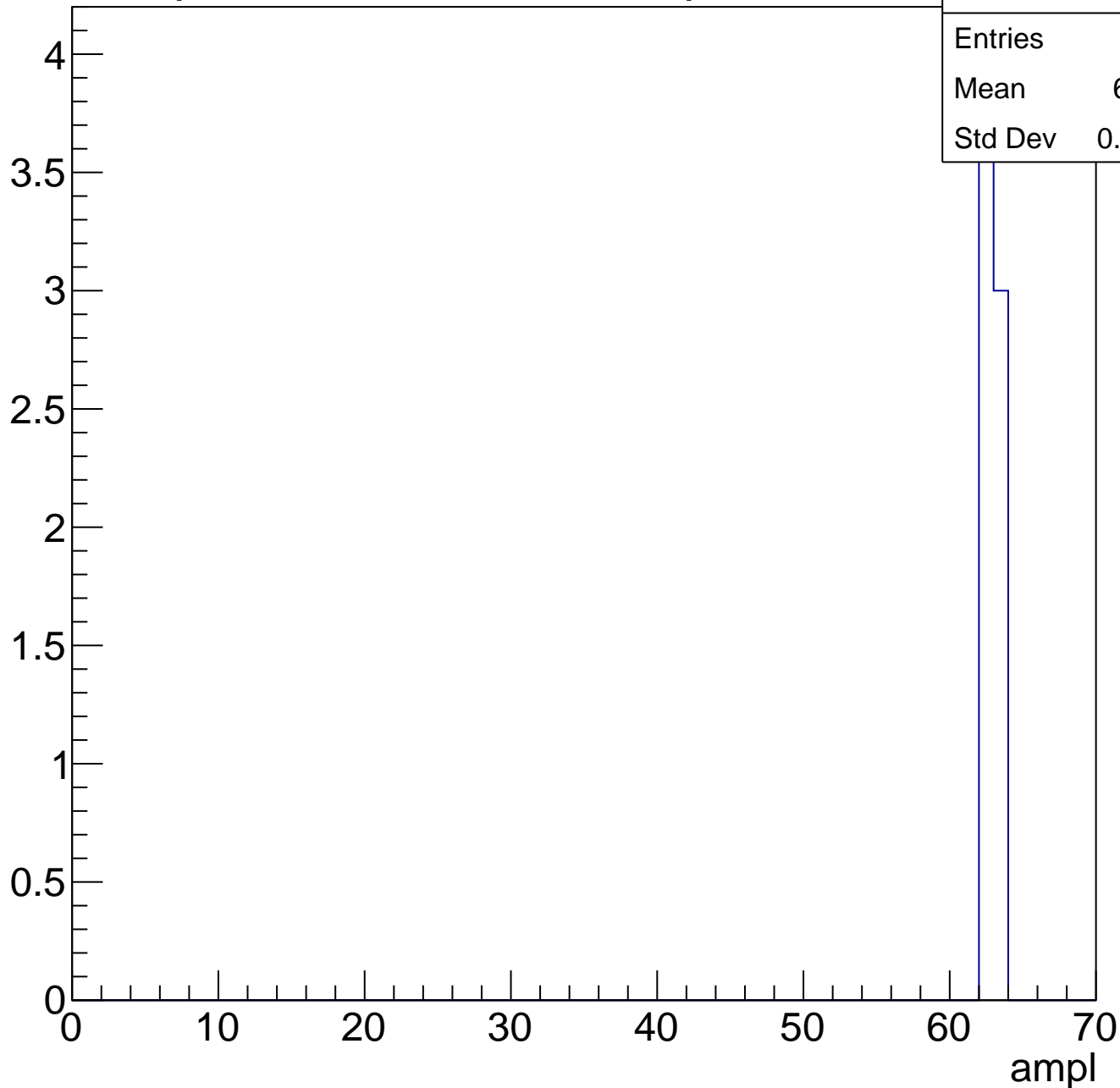
Entry



# B1L100S, U6-ch2, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



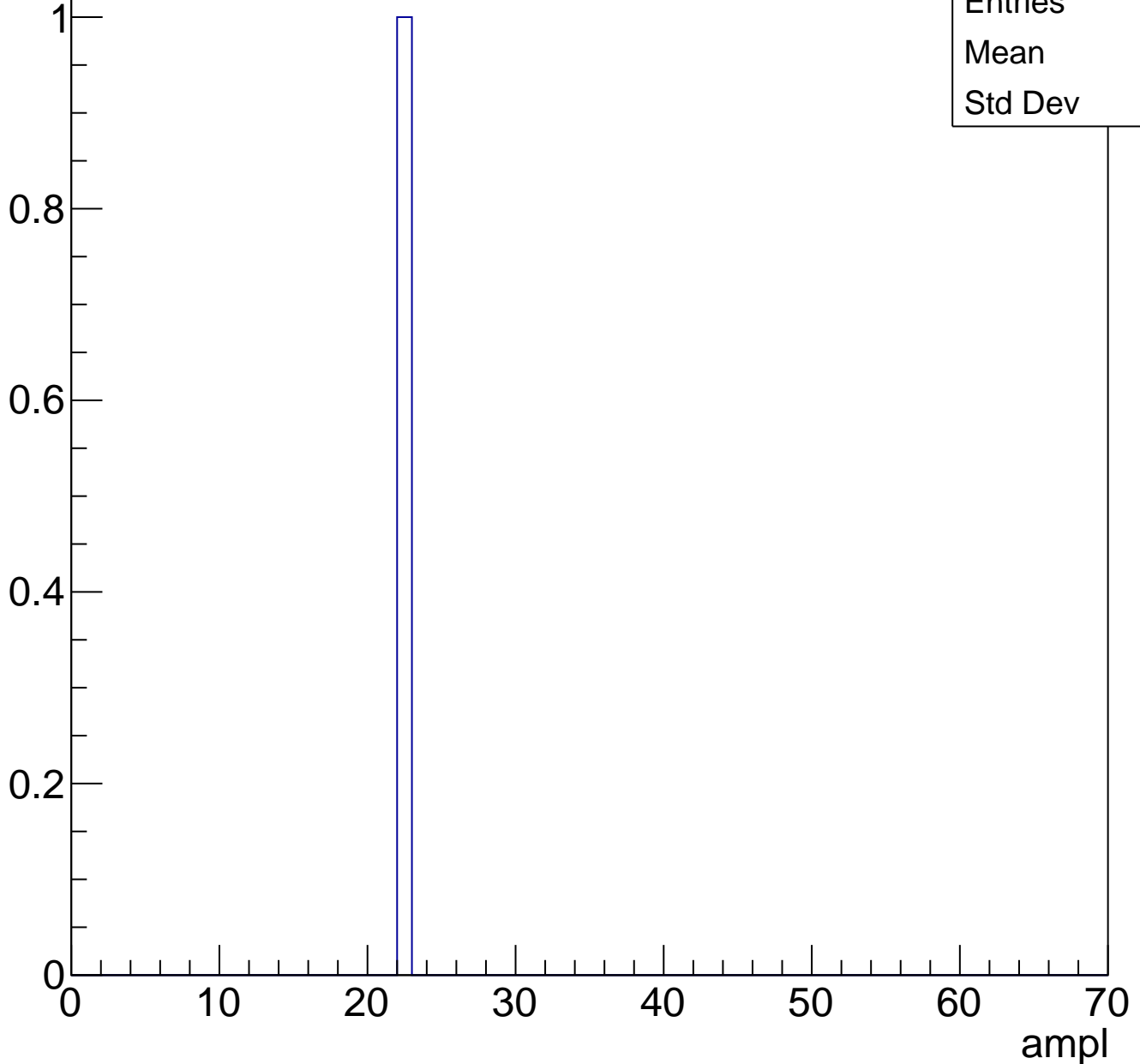
Entries	7
Mean	62.43
Std Dev	0.4949



# B1L100S, U6-ch2, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



# B1L100S, U6-ch3, adc0

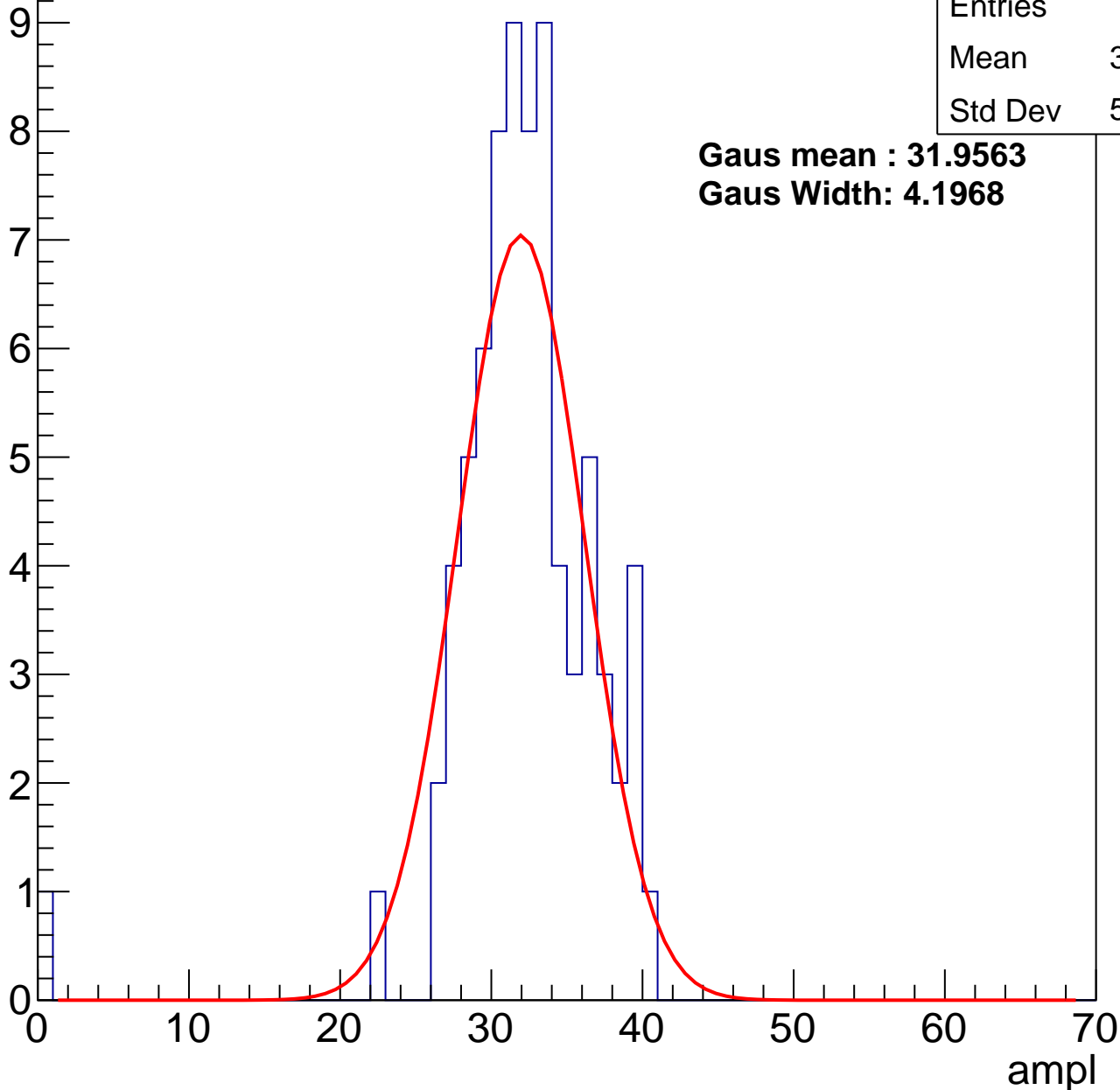
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	75
Mean	31.63
Std Dev	5.163

**Gaus mean : 31.9563**

**Gaus Width: 4.1968**



# B1L100S, U6-ch3, adc1

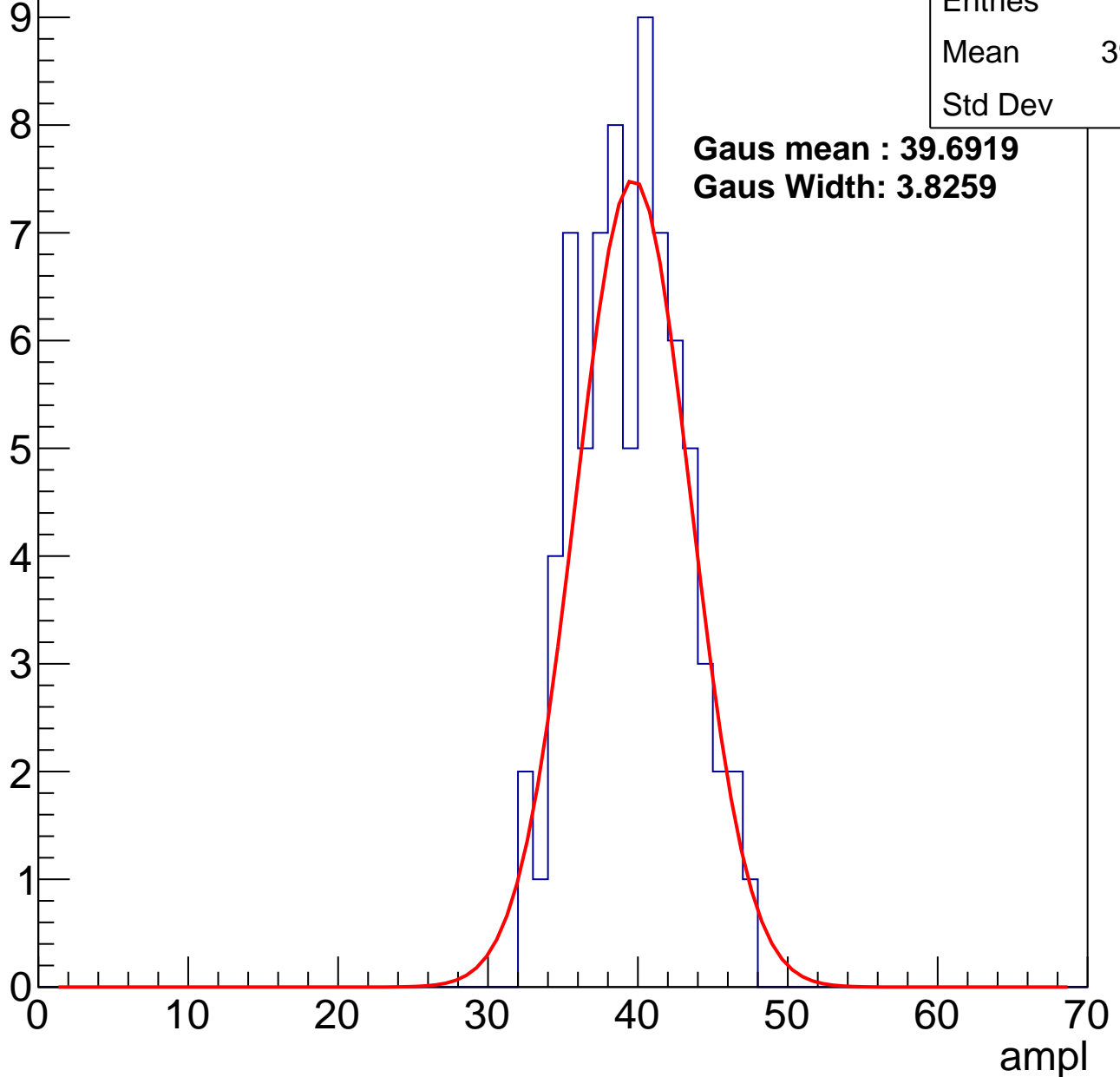
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	74
Mean	39.07
Std Dev	3.5

**Gaus mean : 39.6919**

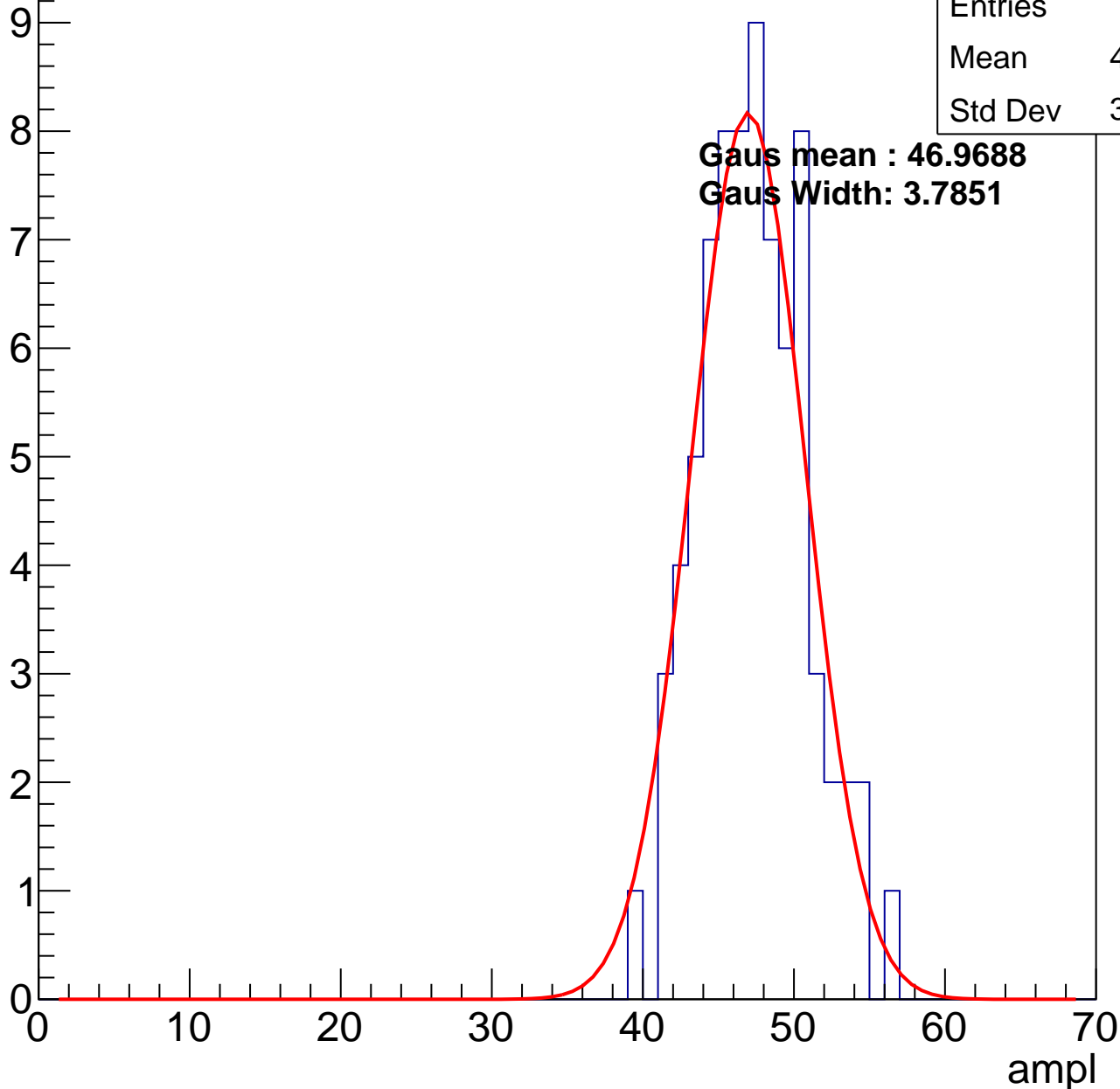
**Gaus Width: 3.8259**



# B1L100S, U6-ch3, adc2

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

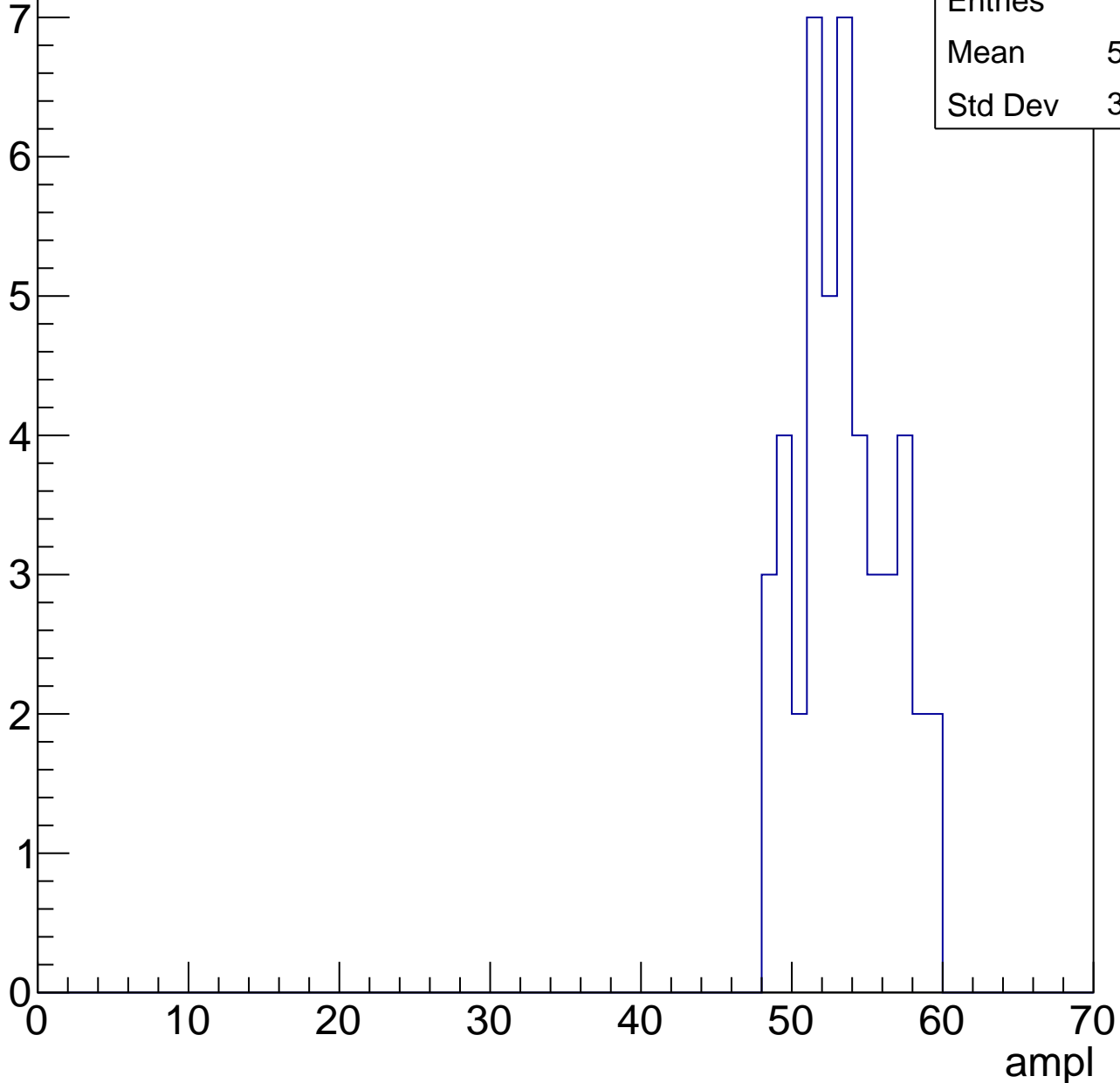


# B1L100S, U6-ch3, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	46
Mean	53.02
Std Dev	3.018



# B1L100S, U6-ch3, adc4

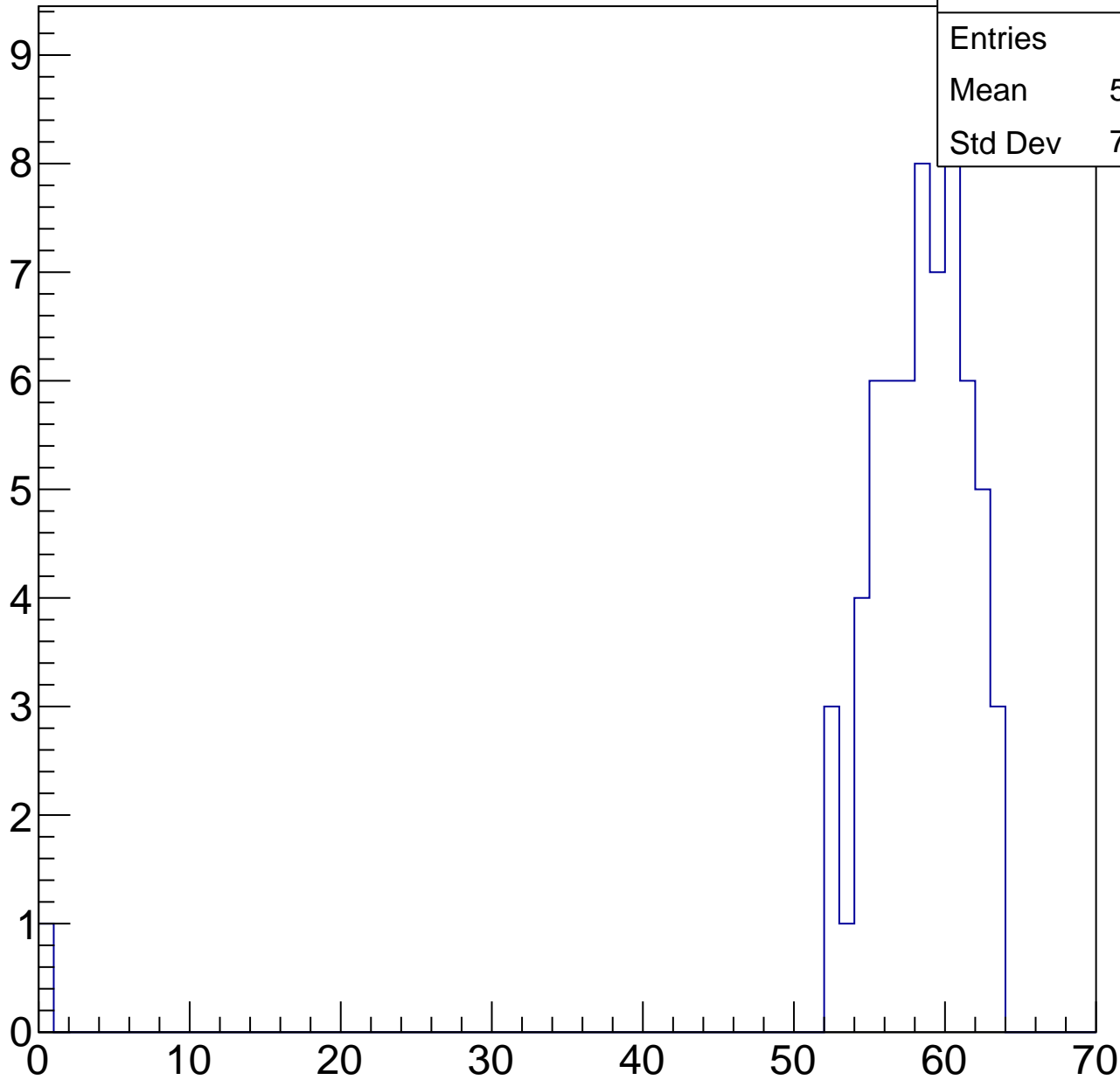
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	65
Mean	57.15
Std Dev	7.697

ampl

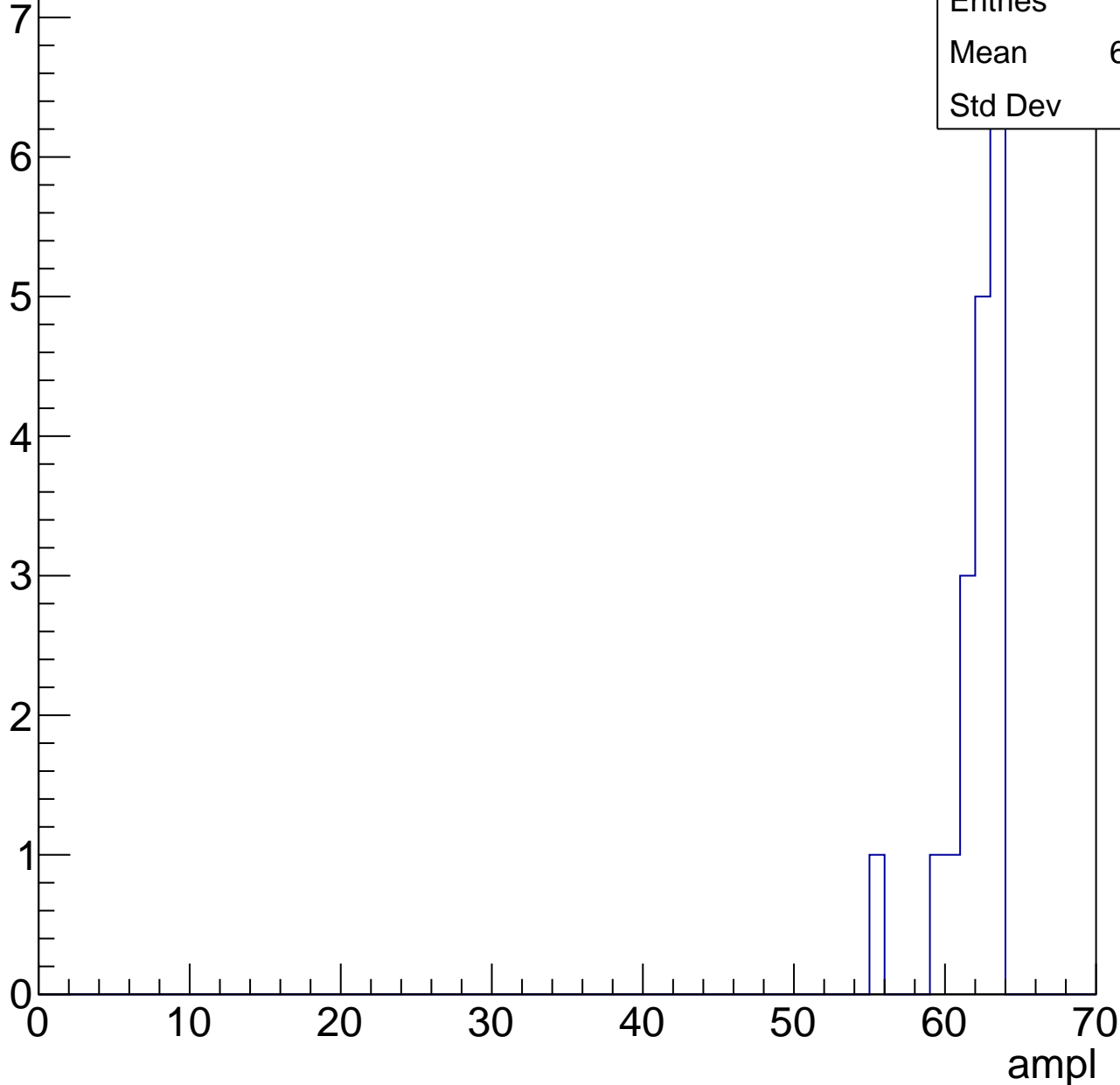


# B1L100S, U6-ch3, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	18
Mean	61.56
Std Dev	1.95



# B1L100S, U6-ch3, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry





# B1L100S, U6-ch3, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L100S, U6-ch4, adc0

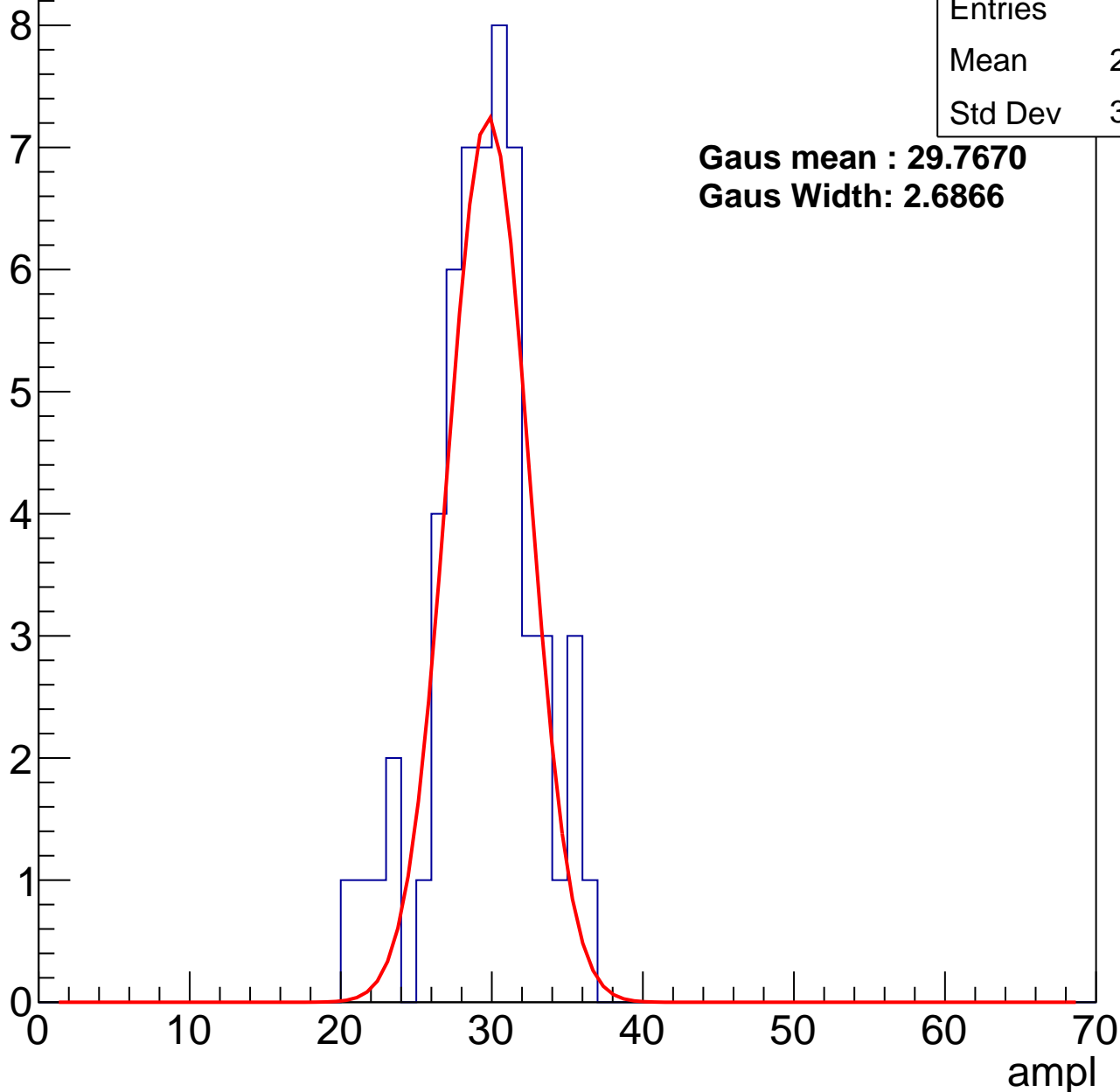
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	56
Mean	29.04
Std Dev	3.386

**Gaus mean : 29.7670**

**Gaus Width: 2.6866**



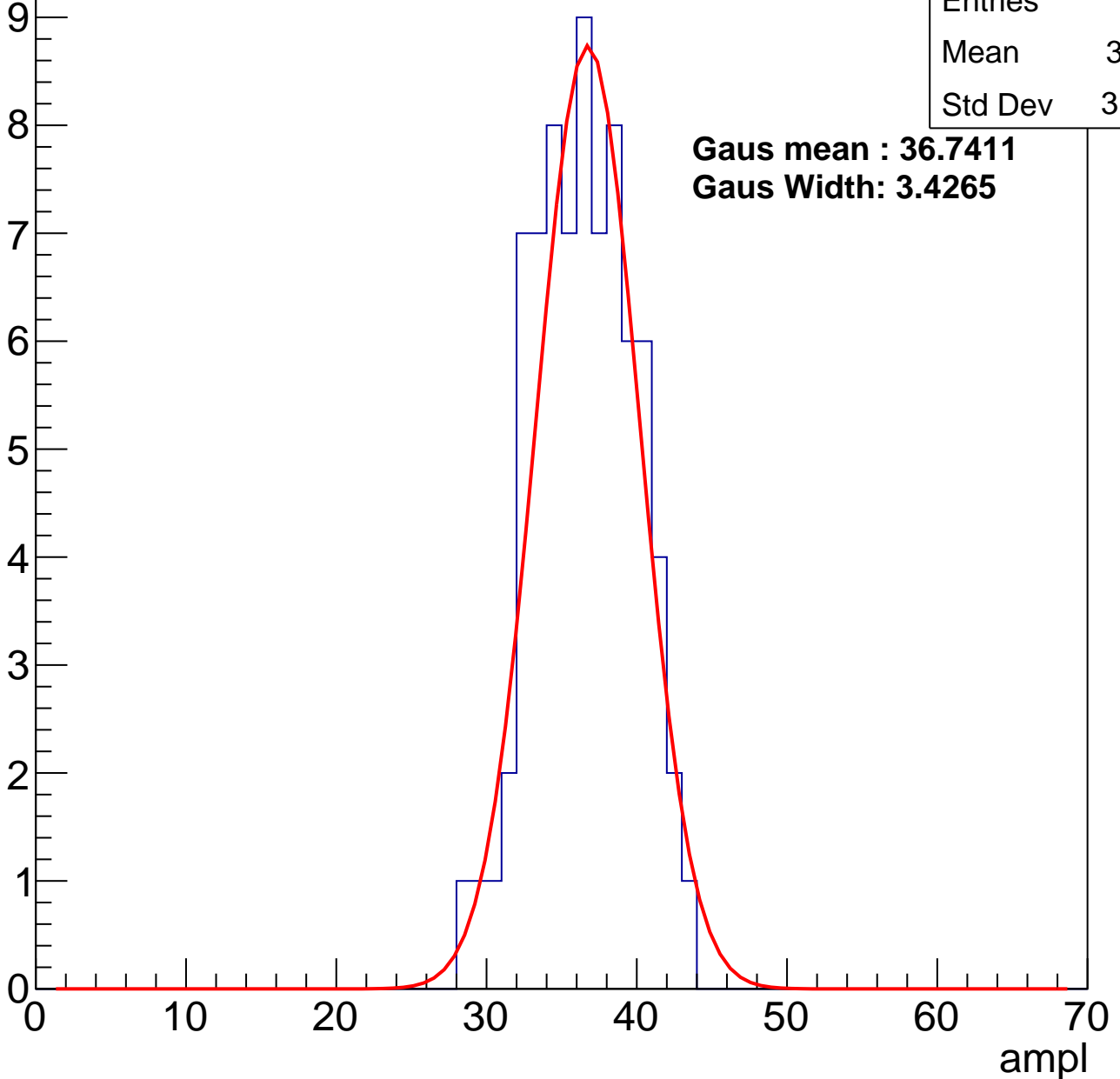
# B1L100S, U6-ch4, adc1

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	77
Mean	36.01
Std Dev	3.269

**Gaus mean : 36.7411**  
**Gaus Width: 3.4265**



# B1L100S, U6-ch4, adc2

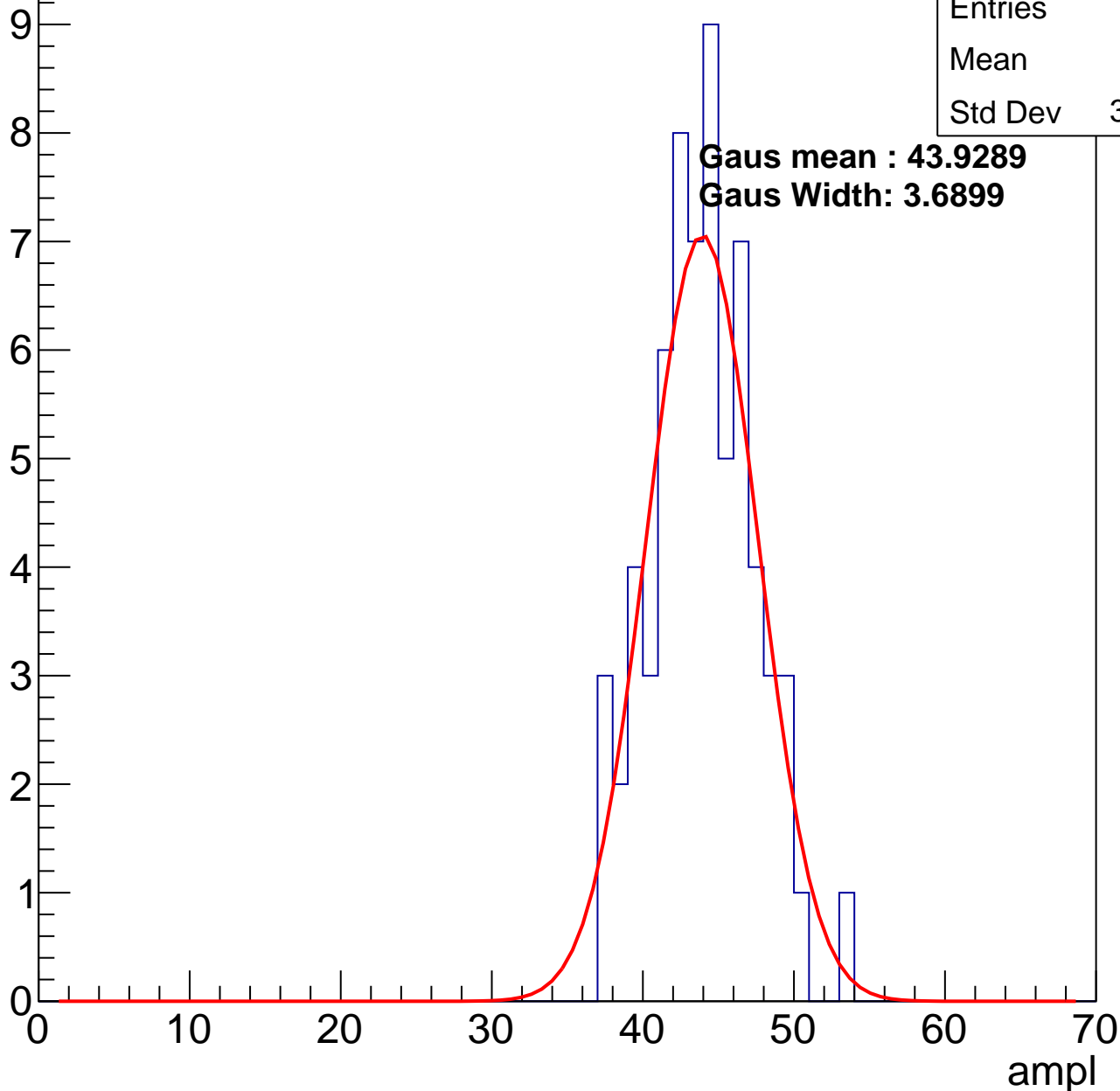
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	66
Mean	43.5
Std Dev	3.377

**Gaus mean : 43.9289**

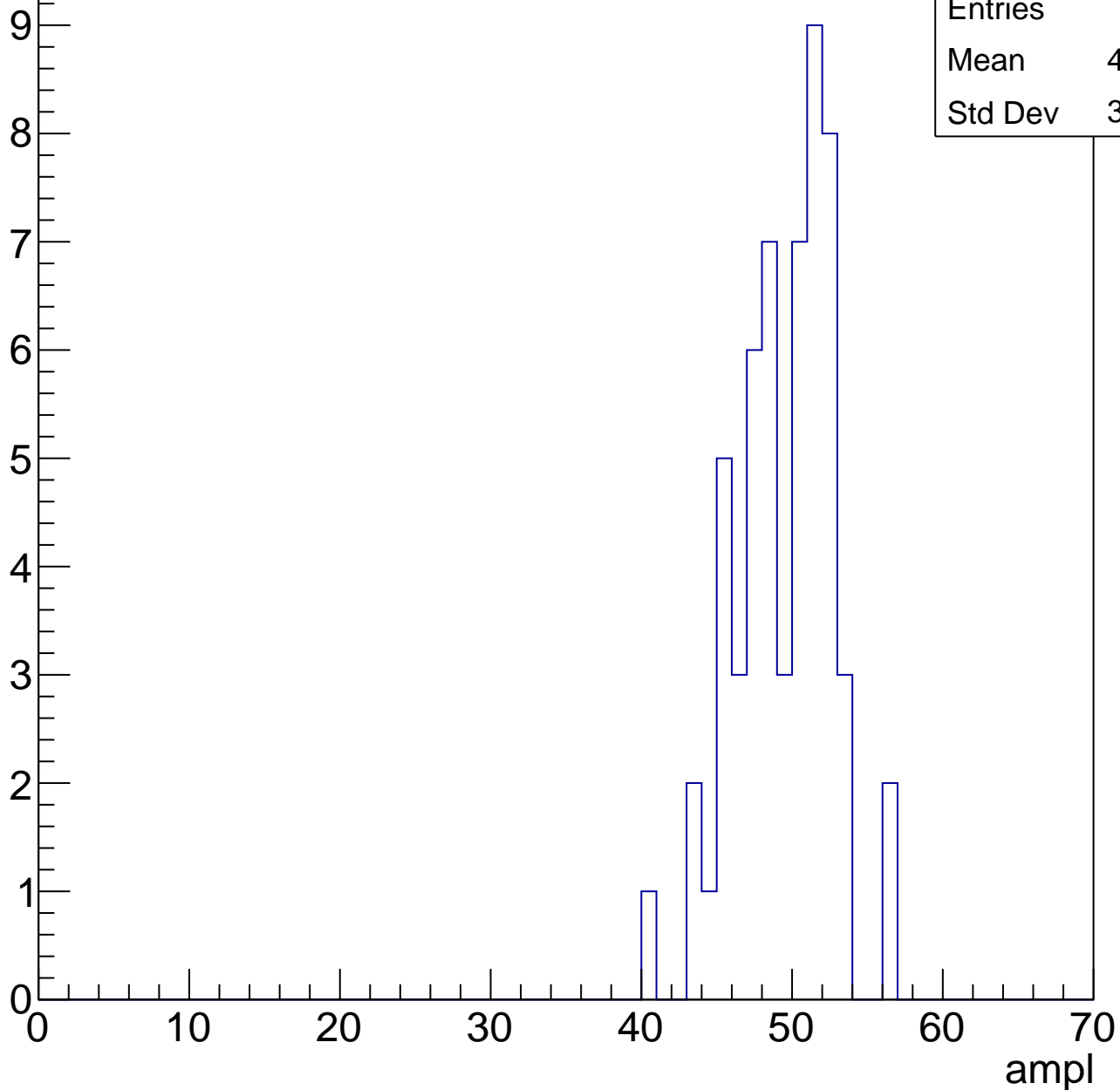
**Gaus Width: 3.6899**



# B1L100S, U6-ch4, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



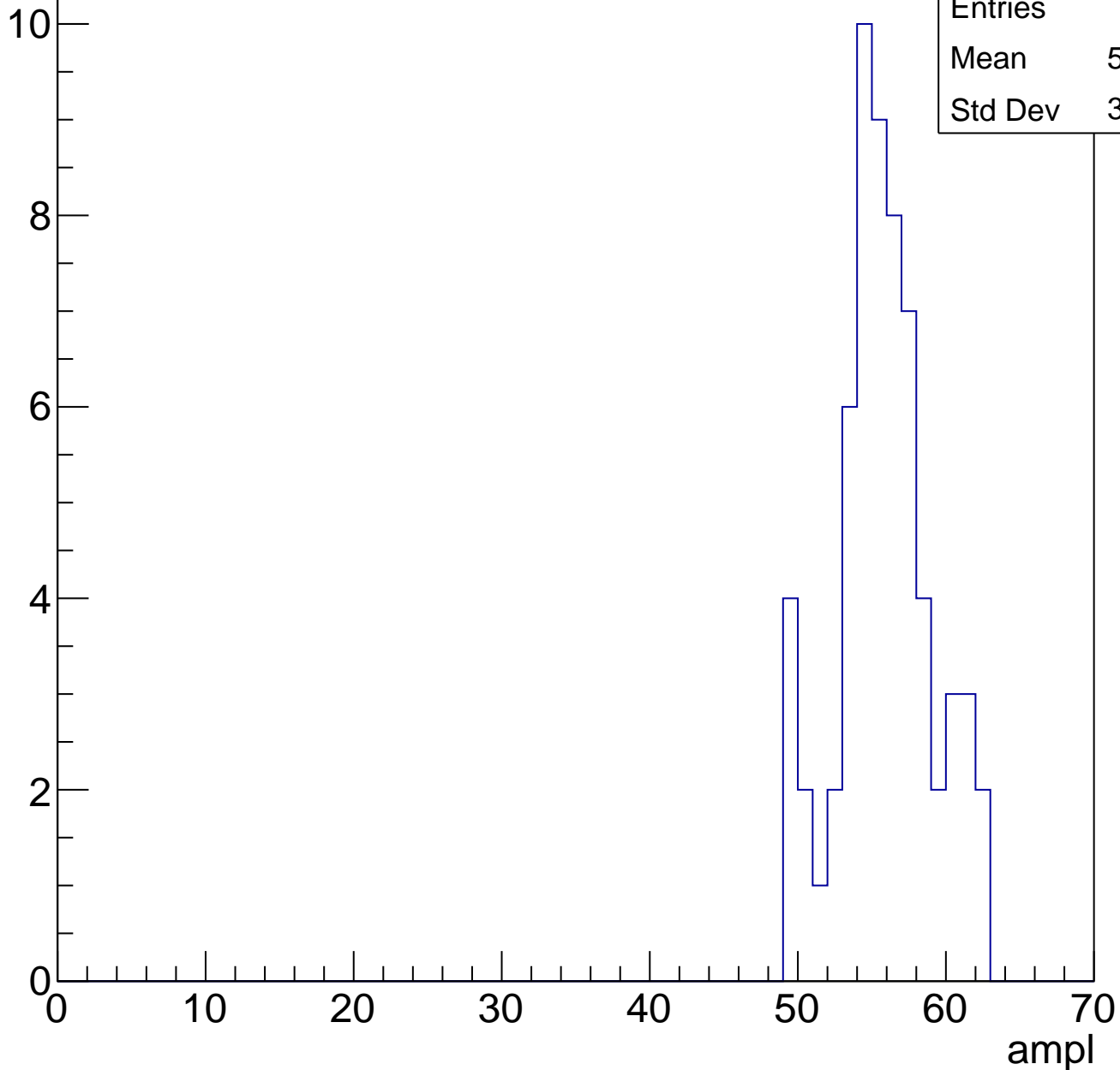
Entries	57
Mean	49.02
Std Dev	3.182

# B1L100S, U6-ch4, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	63
Mean	55.37
Std Dev	3.184

Entry



# B1L100S, U6-ch4, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

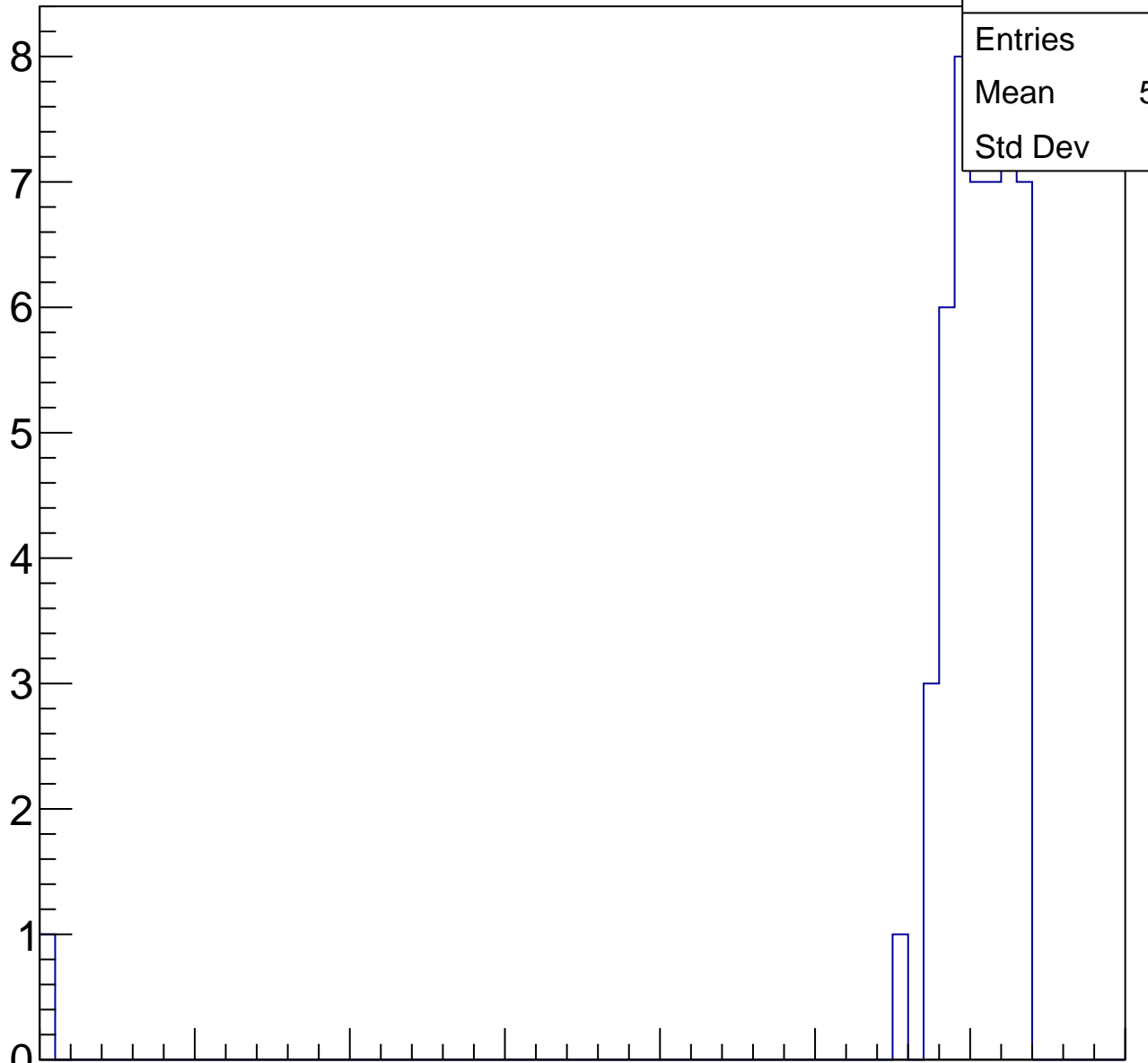
Entry

Entries	48
Mean	58.96
Std Dev	8.82

8  
7  
6  
5  
4  
3  
2  
1  
0

0 10 20 30 40 50 60 70

ampl



# B1L100S, U6-ch4, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry





# B1L100S, U6-ch4, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



# B1L100S, U6-ch5, adc0

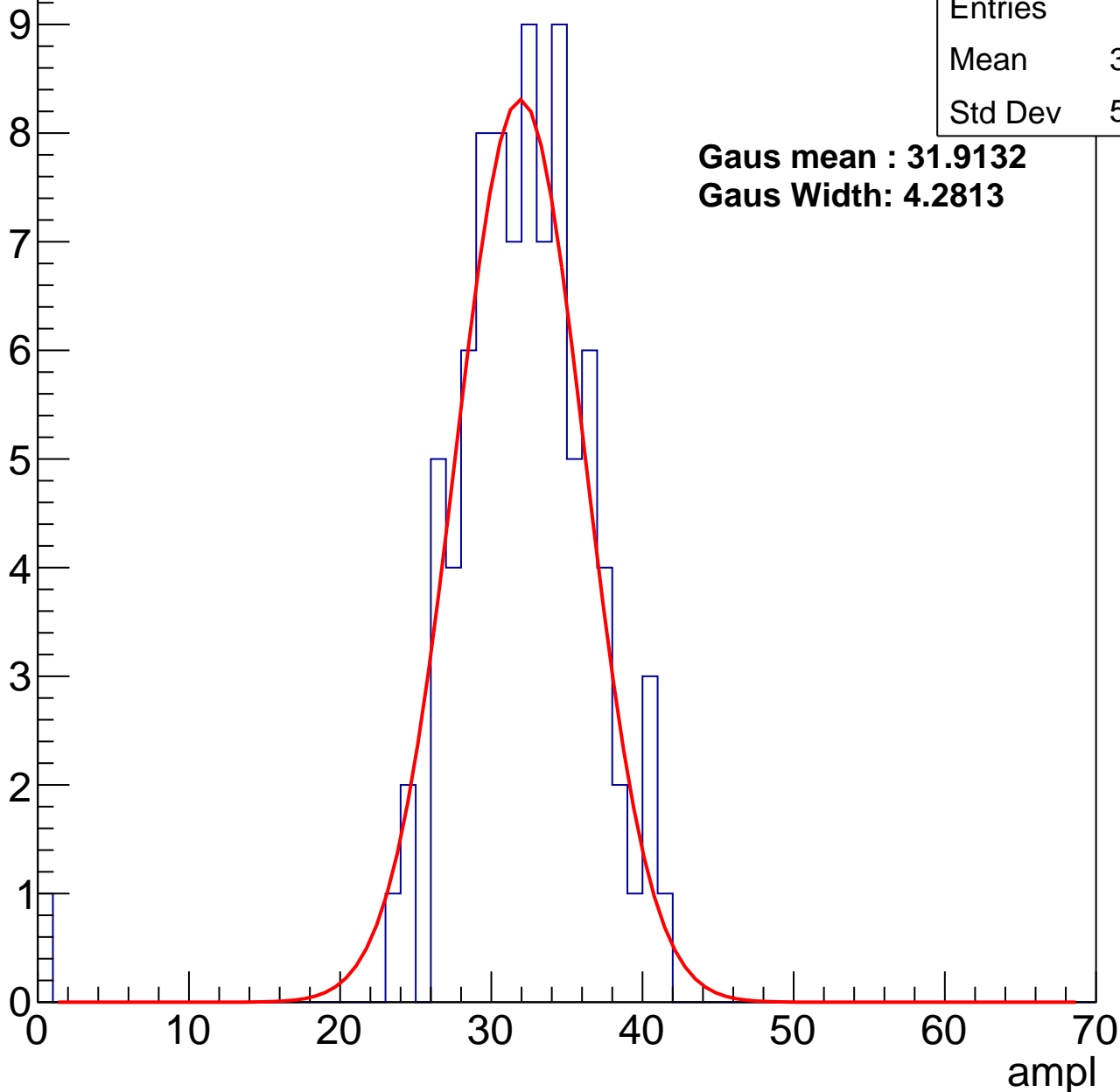
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	89
Mean	31.53
Std Dev	5.169

**Gaus mean : 31.9132**

**Gaus Width: 4.2813**



# B1L100S, U6-ch5, adc1

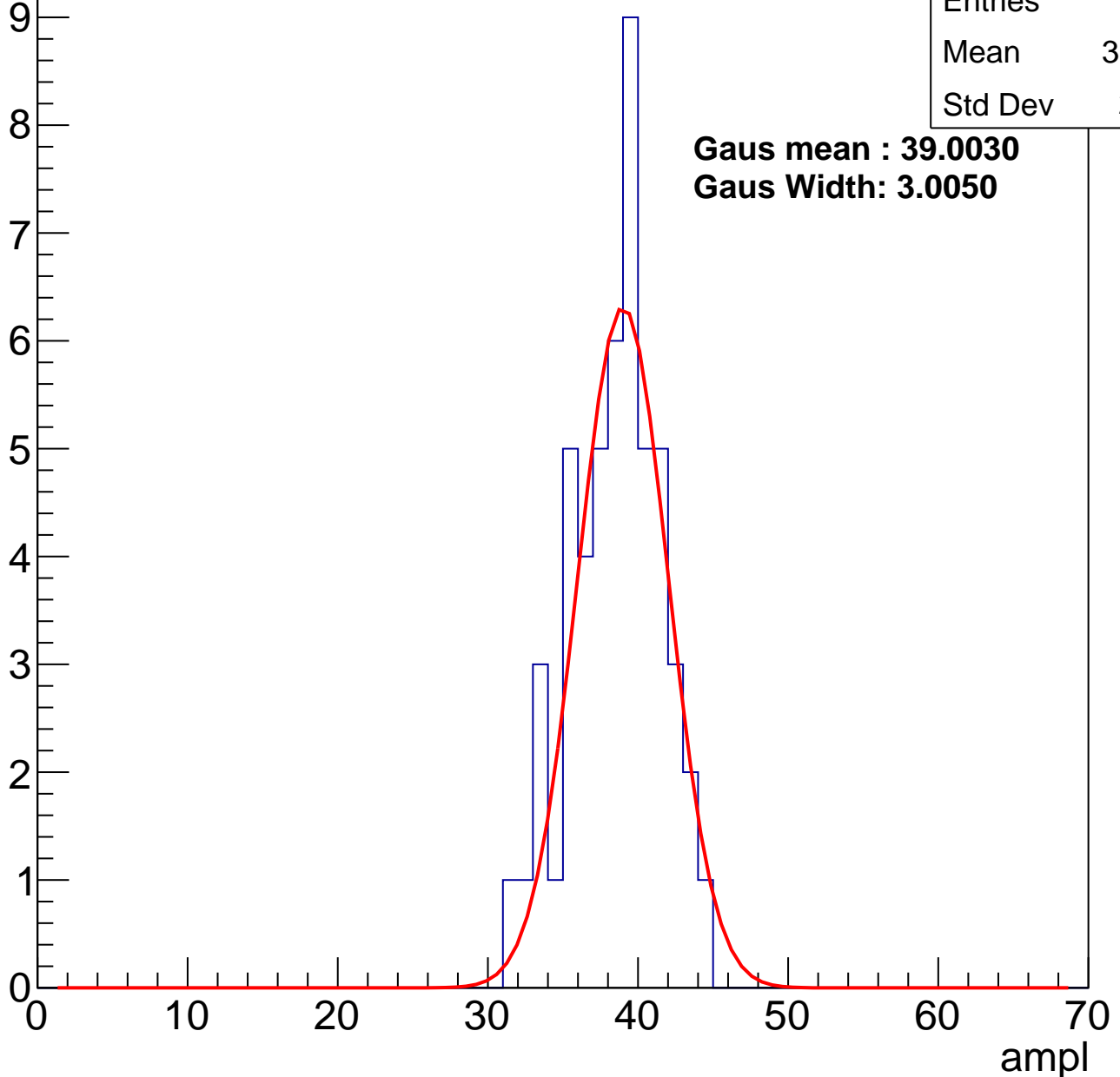
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	51
Mean	38.04
Std Dev	2.97

**Gaus mean : 39.0030**

**Gaus Width: 3.0050**



# B1L100S, U6-ch5, adc2

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	72
Mean	44.99
Std Dev	3.234

**Gaus mean : 45.3614**

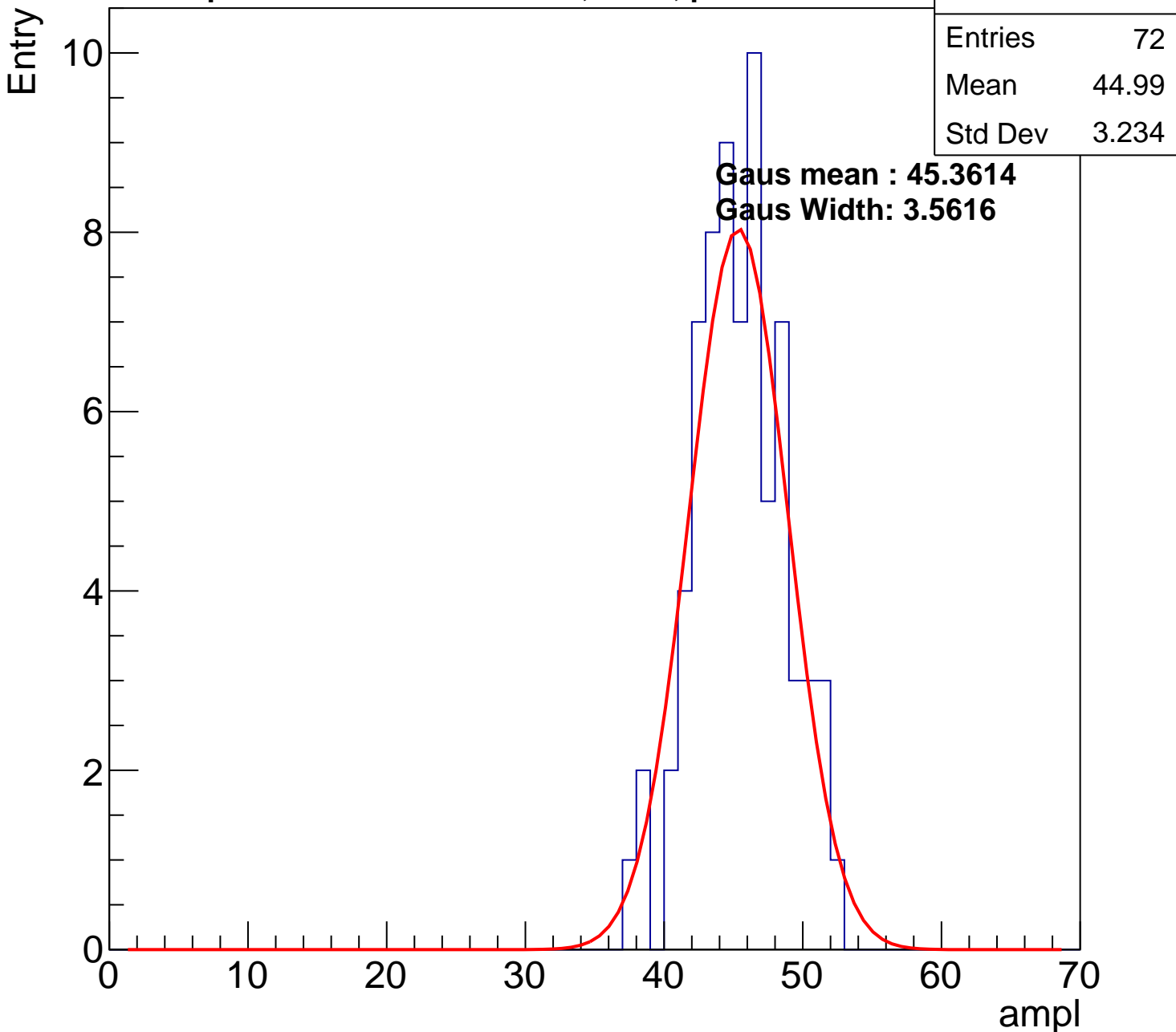
**Gaus Width: 3.5616**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

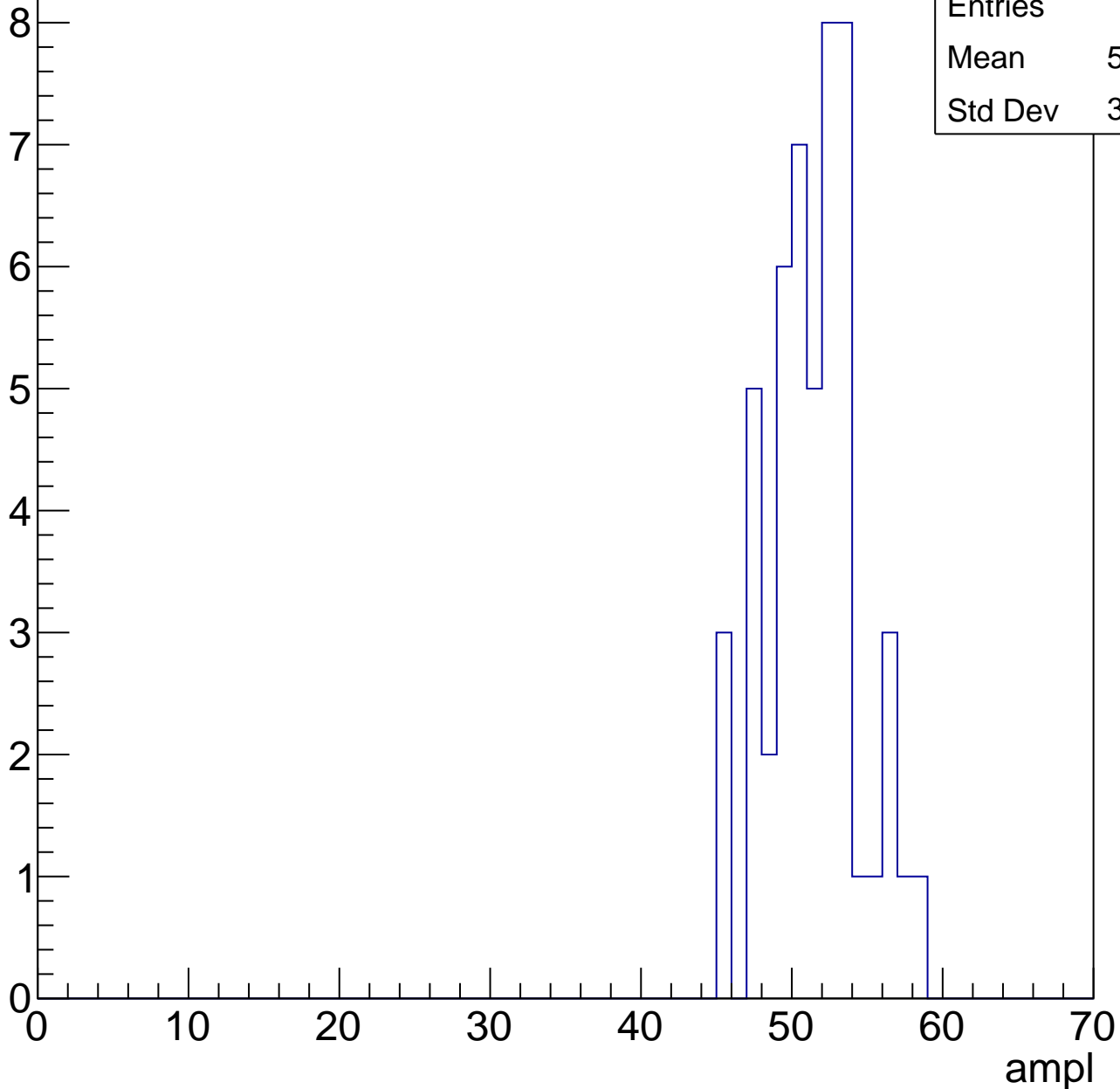


# B1L100S, U6-ch5, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	51
Mean	50.92
Std Dev	3.009

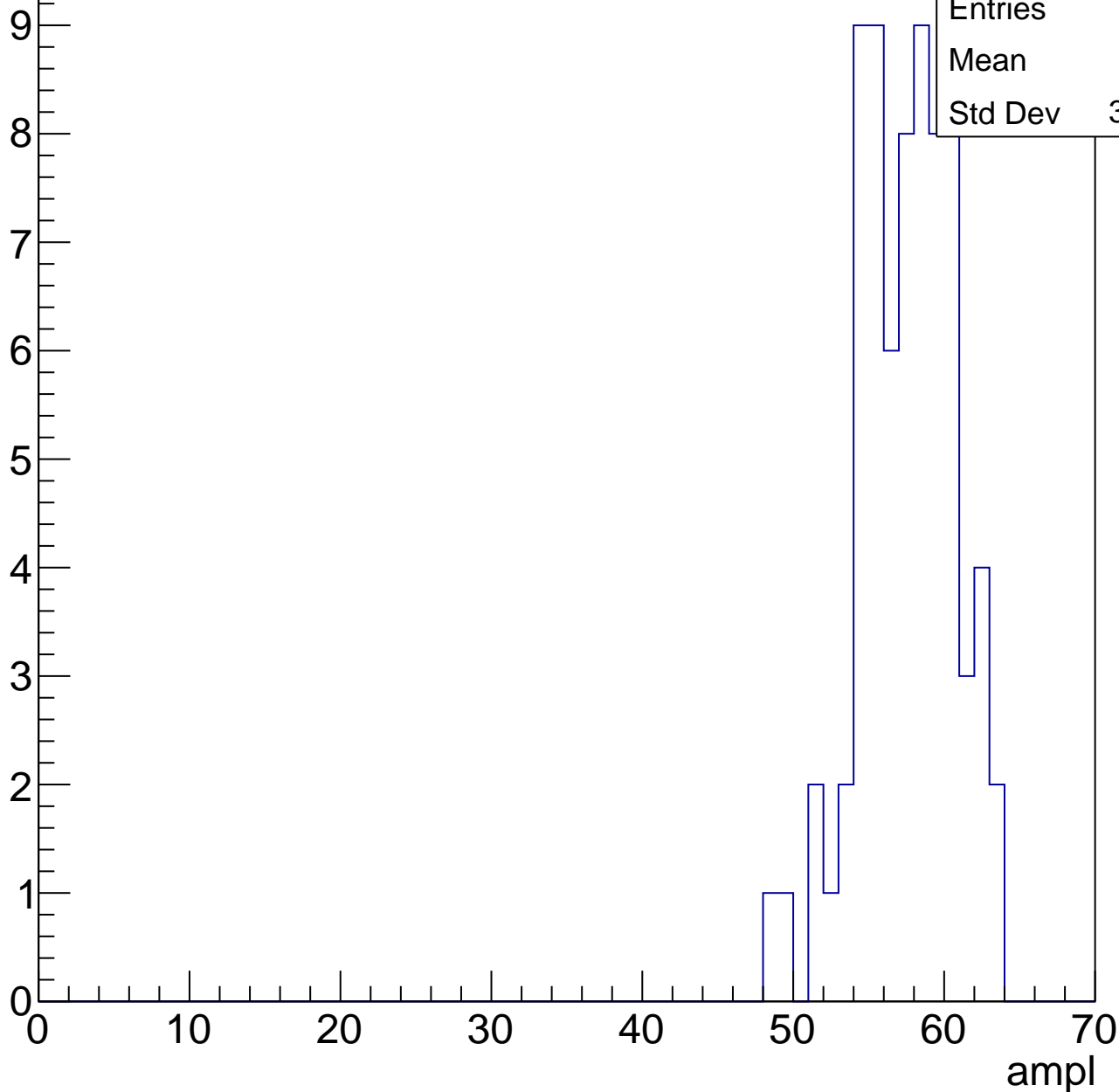


# B1L100S, U6-ch5, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	73
Mean	57
Std Dev	3.162

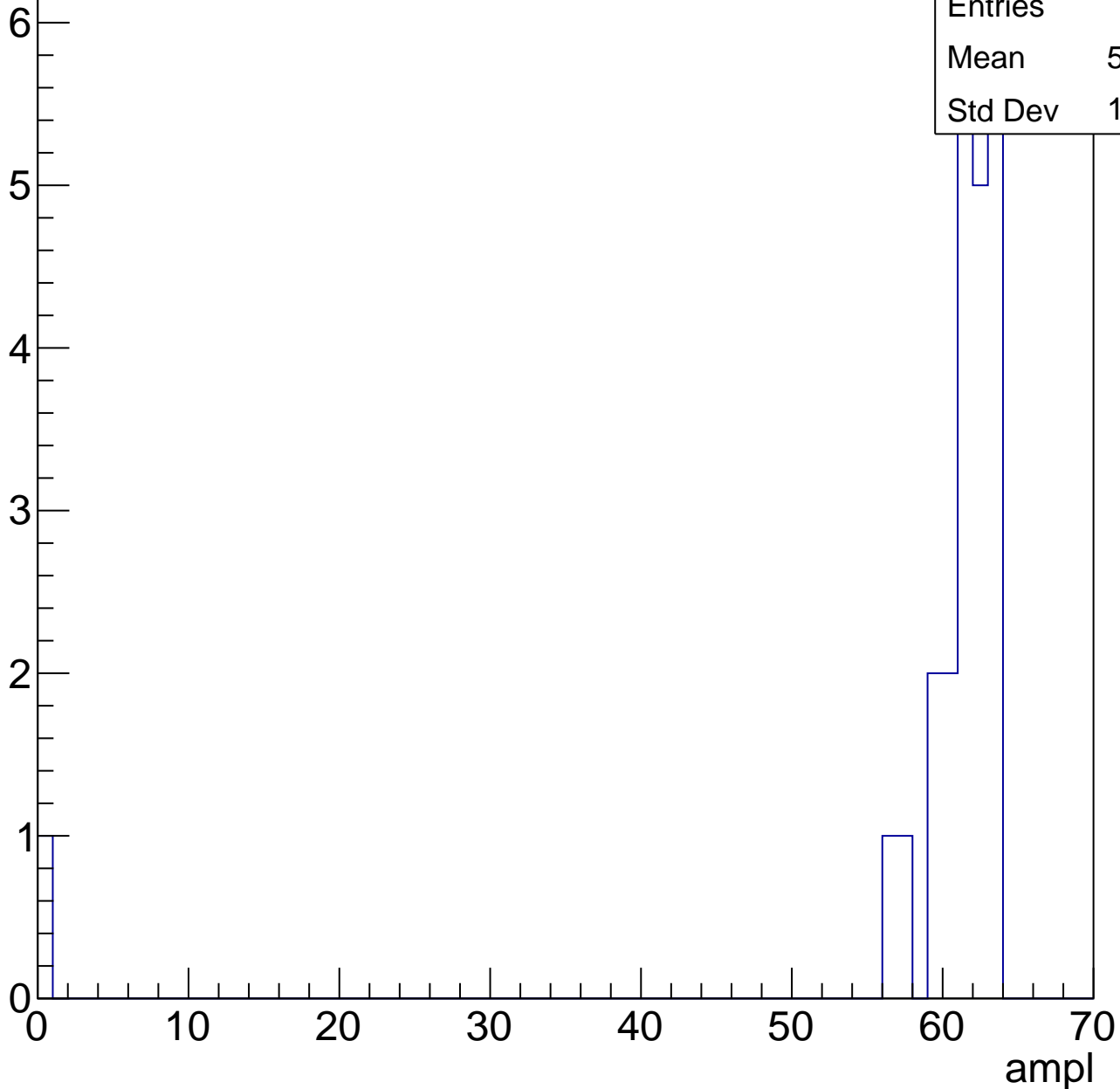


# B1L100S, U6-ch5, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	24
Mean	58.54
Std Dev	12.34



# B1L100S, U6-ch5, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	4
Mean	62.25
Std Dev	0.8292



# B1L100S, U6-ch5, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L100S, U6-ch6, adc0

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	82
Mean	30.21
Std Dev	3.177

**Gaus mean : 30.6345**

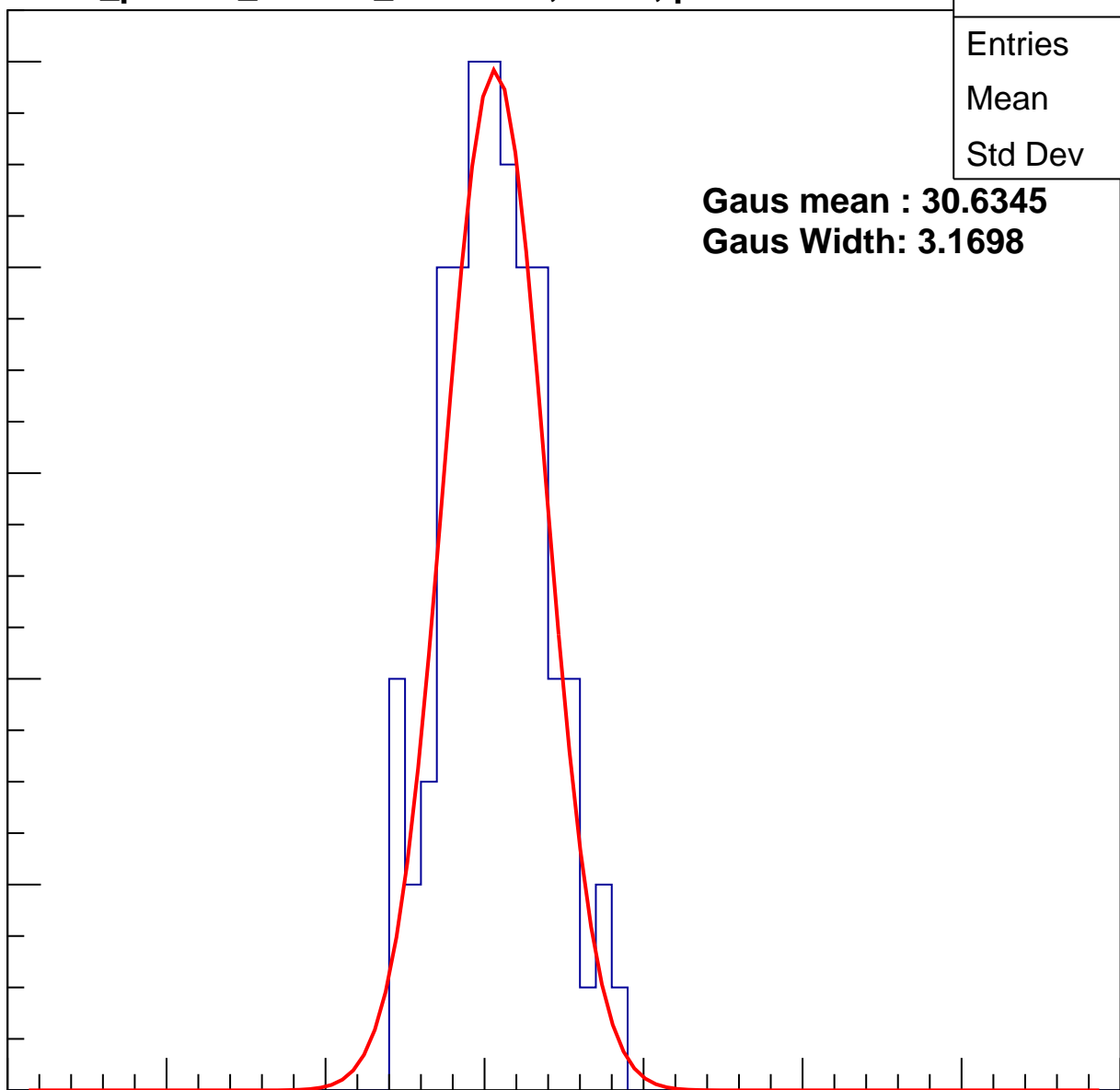
**Gaus Width: 3.1698**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B1L100S, U6-ch6, adc1

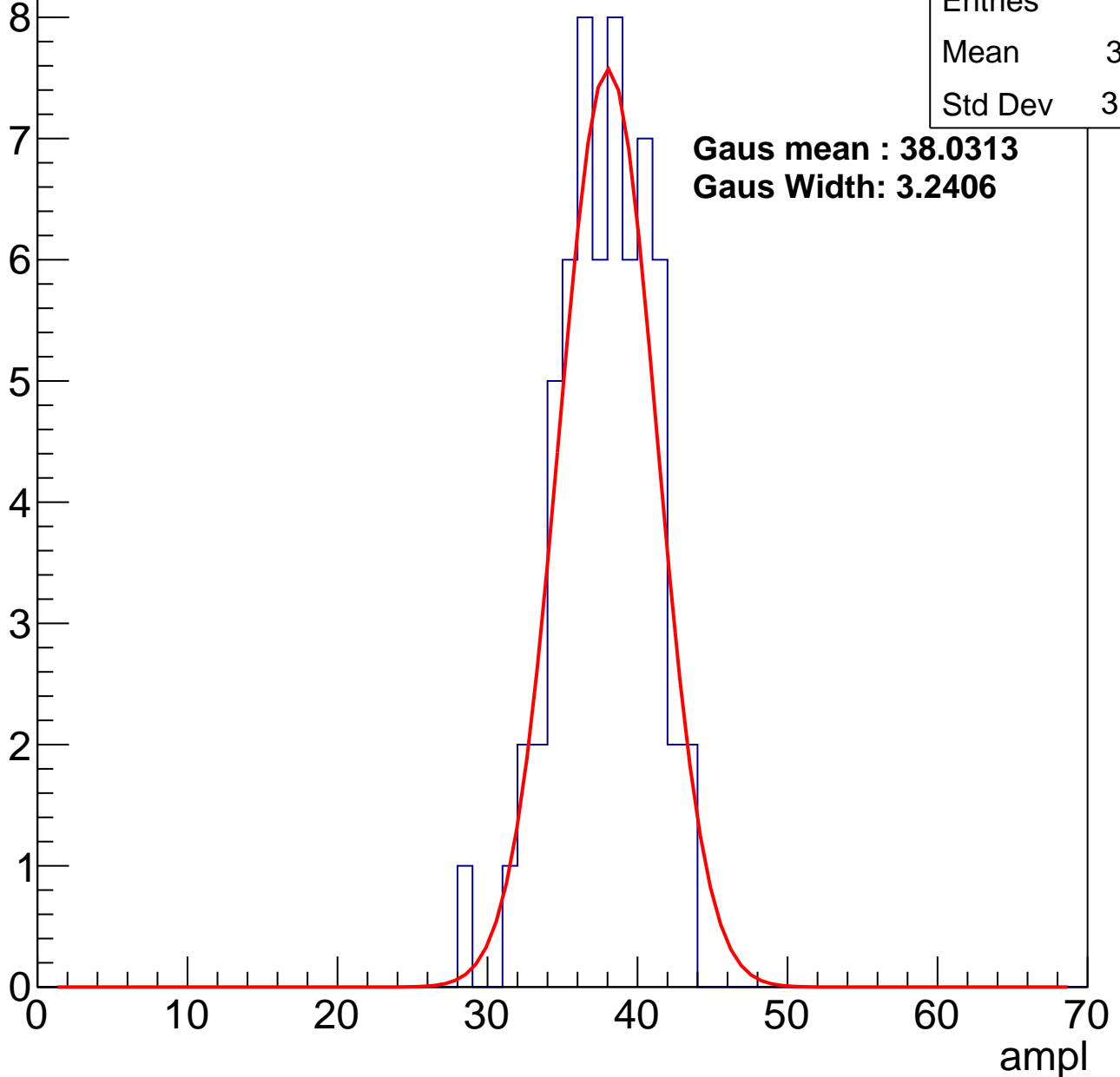
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	62
Mean	37.31
Std Dev	3.067

**Gaus mean : 38.0313**

**Gaus Width: 3.2406**



# B1L100S, U6-ch6, adc2

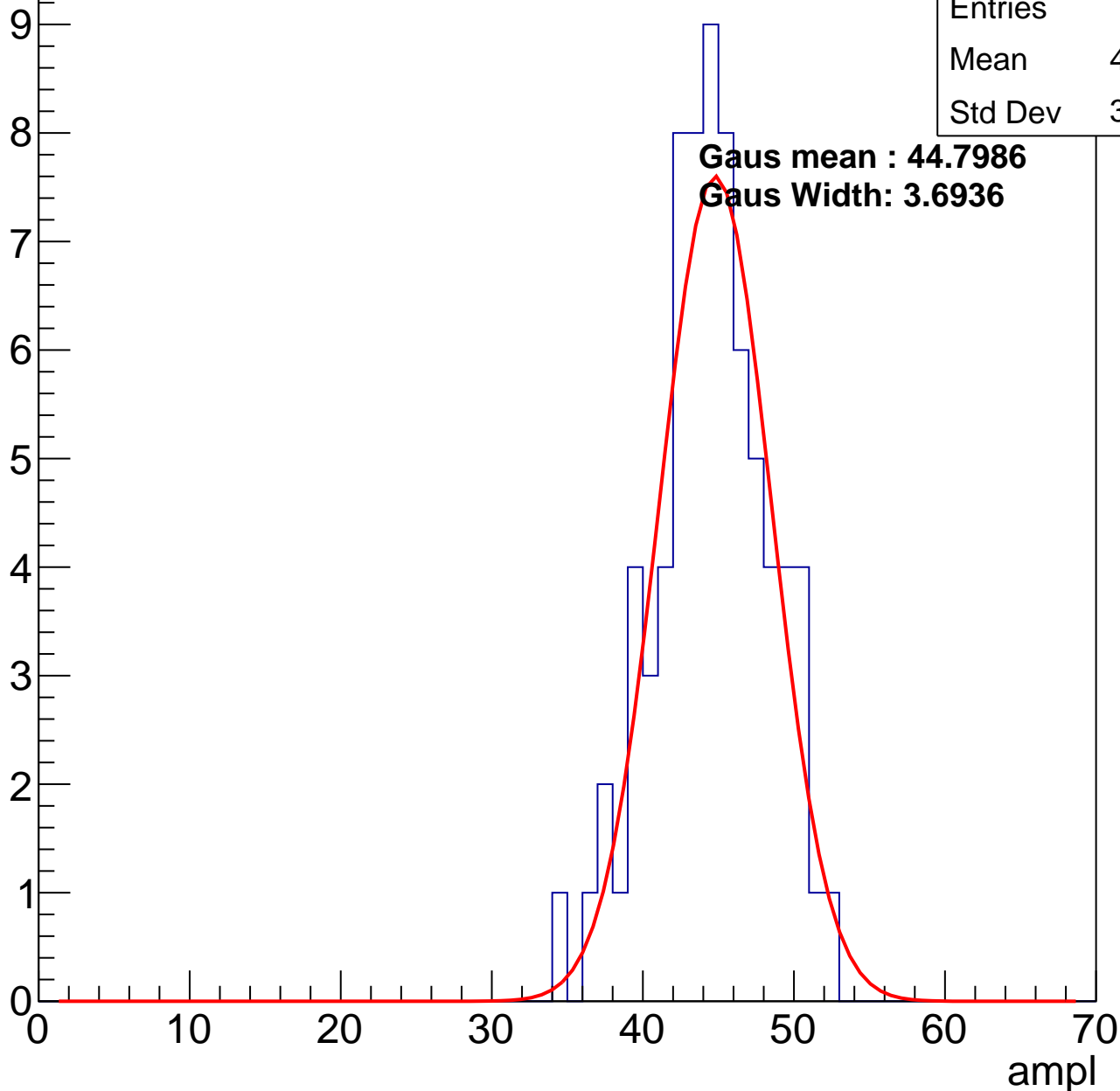
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	74
Mean	44.05
Std Dev	3.712

**Gaus mean : 44.7986**

**Gaus Width: 3.6936**

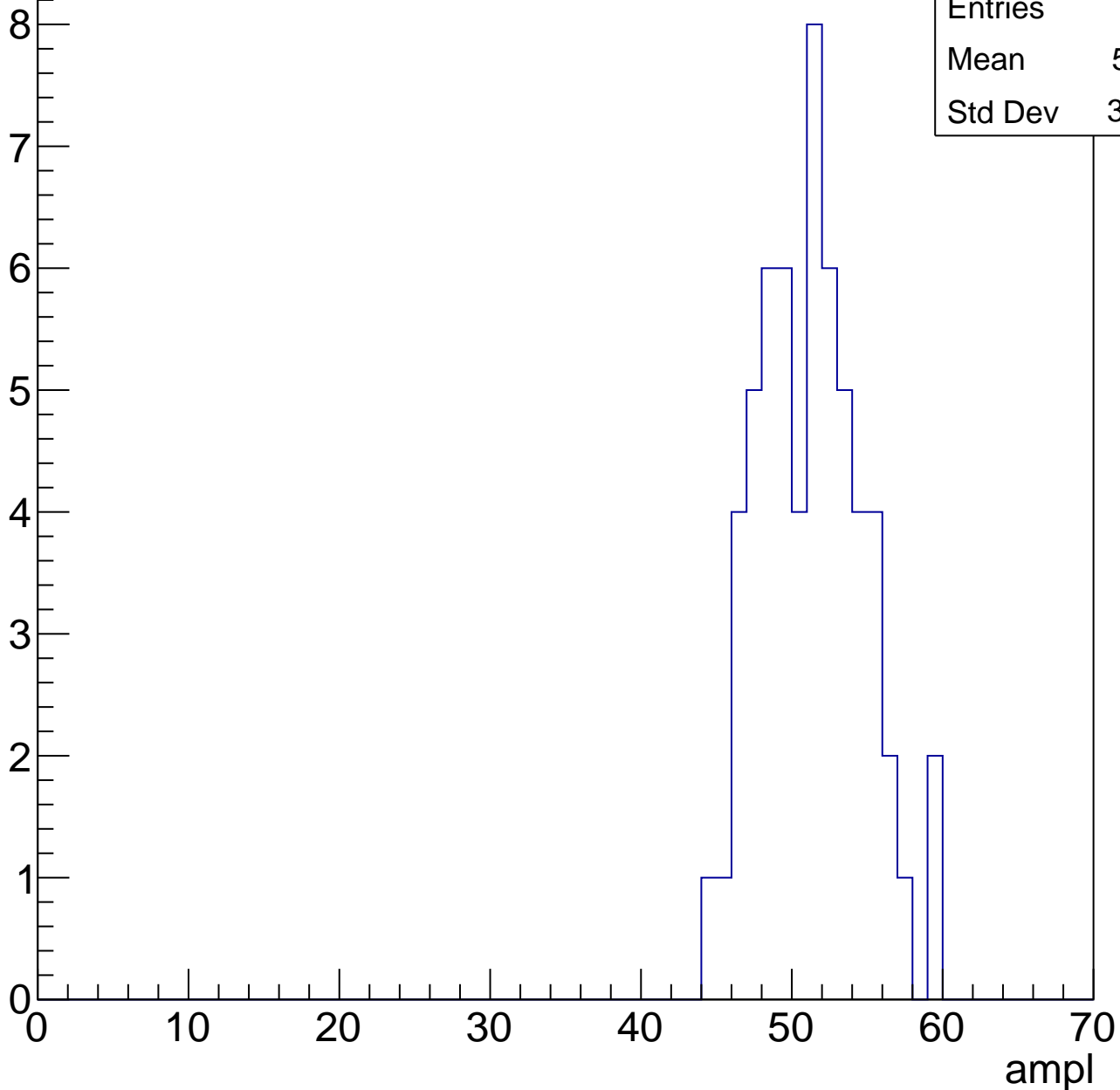


# B1L100S, U6-ch6, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	59
Mean	50.81
Std Dev	3.407

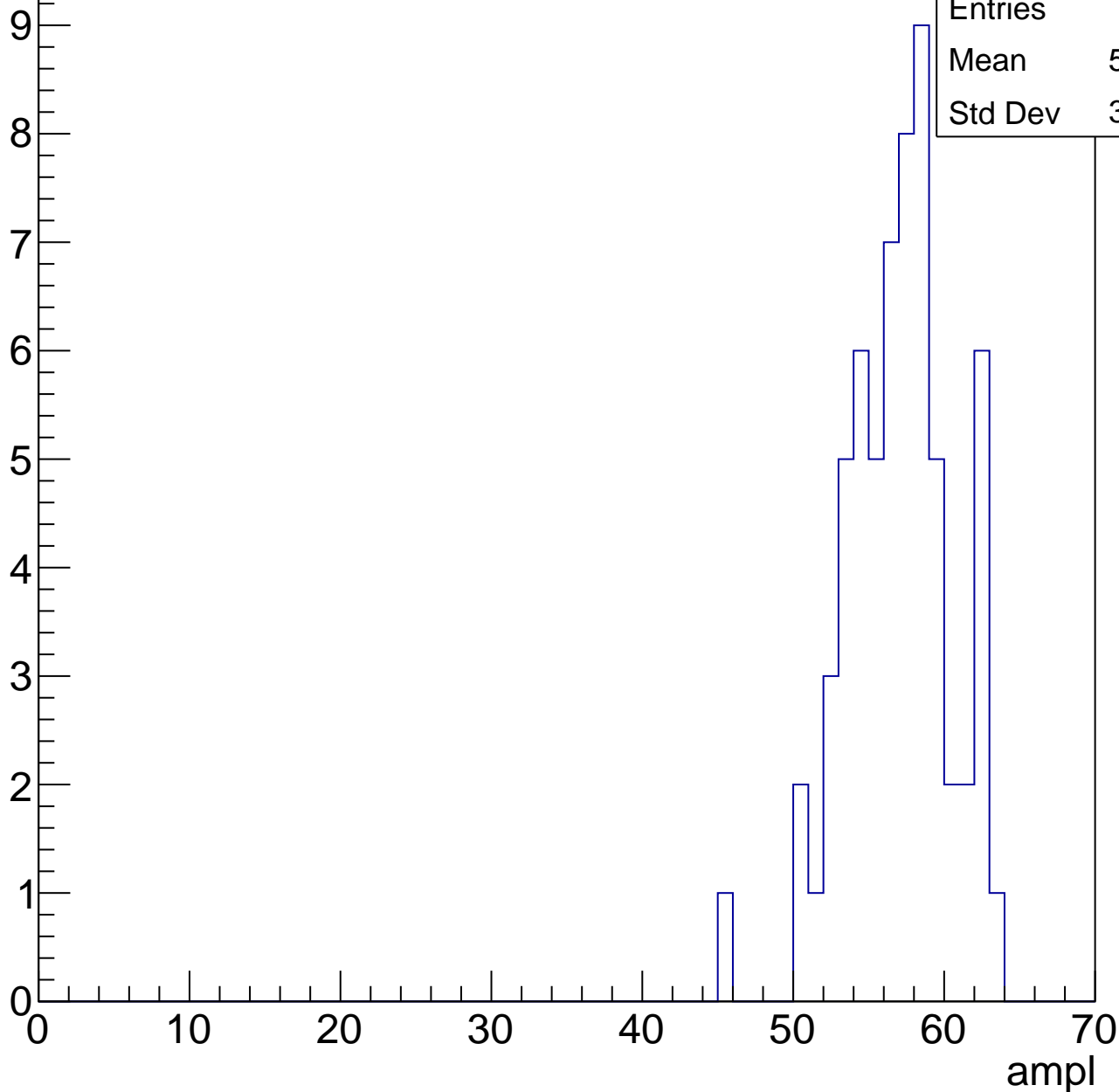


# B1L100S, U6-ch6, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	63
Mean	56.48
Std Dev	3.477



# B1L100S, U6-ch6, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	30
Mean	60.4
Std Dev	1.977

ampl

0 10 20 30 40 50 60 70

0

1

2

3

4

5

6

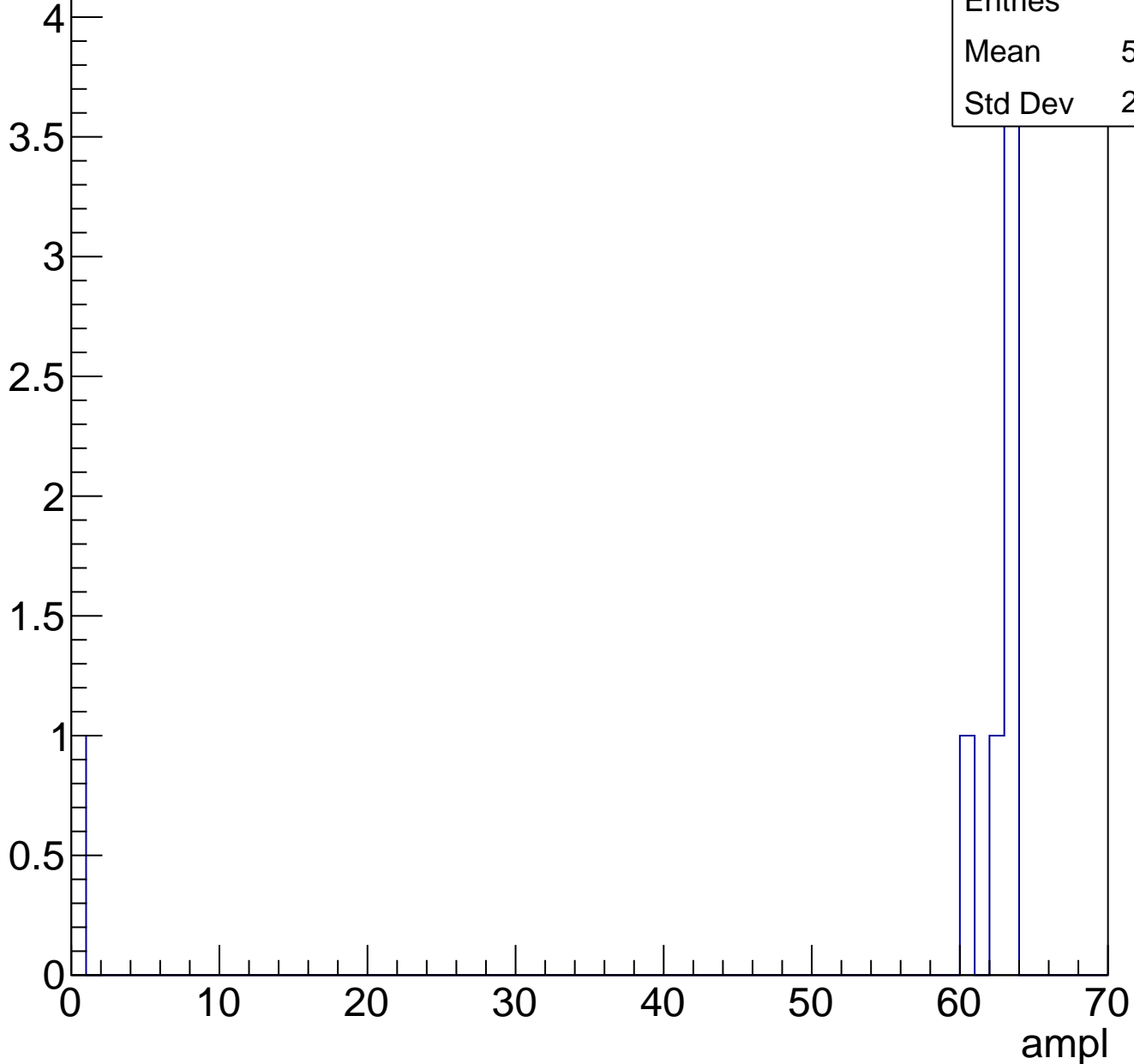
7

8

# B1L100S, U6-ch6, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry





# B1L100S, U6-ch6, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L100S, U6-ch7, adc0

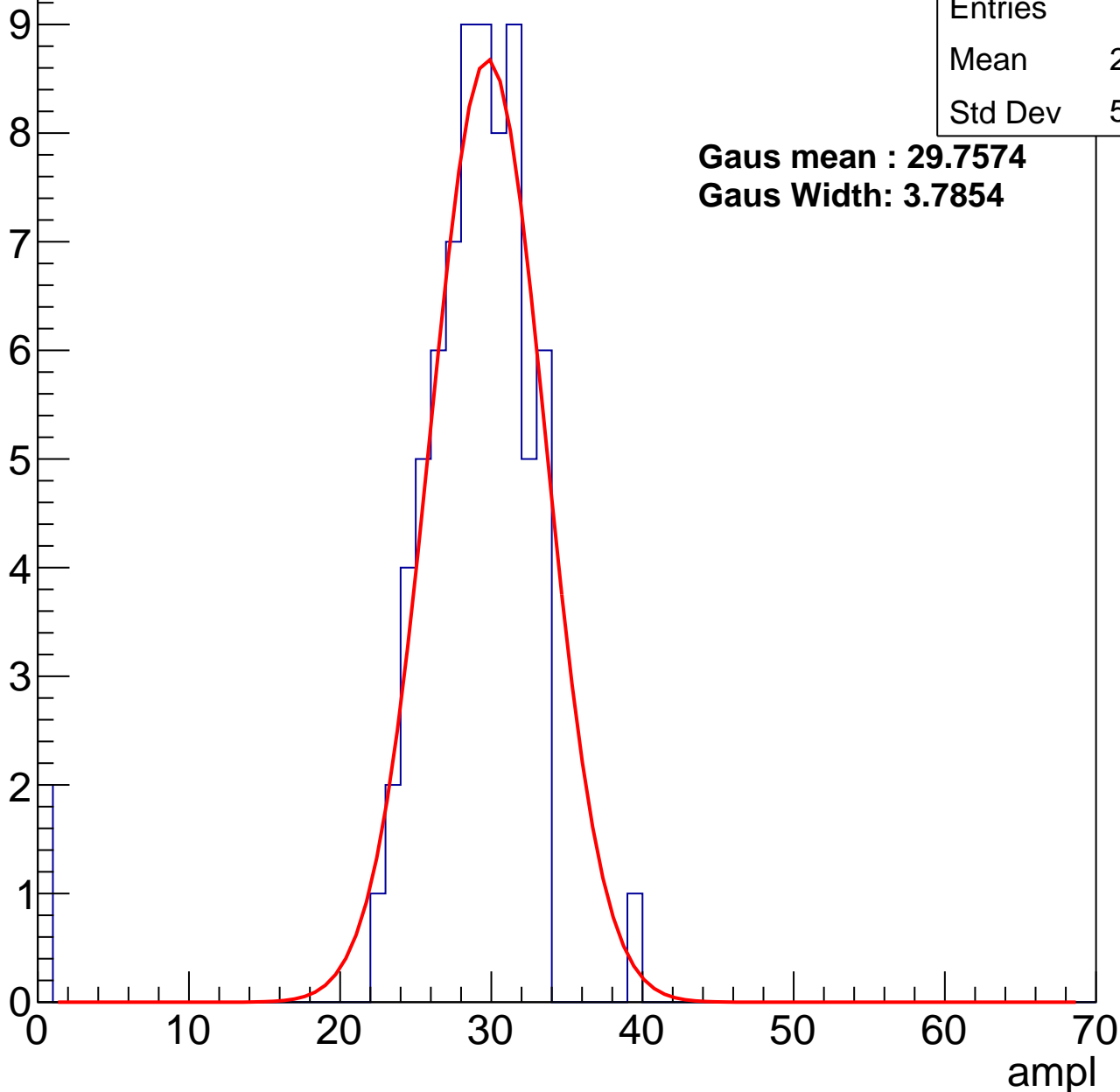
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	74
Mean	27.88
Std Dev	5.534

**Gaus mean : 29.7574**

**Gaus Width: 3.7854**

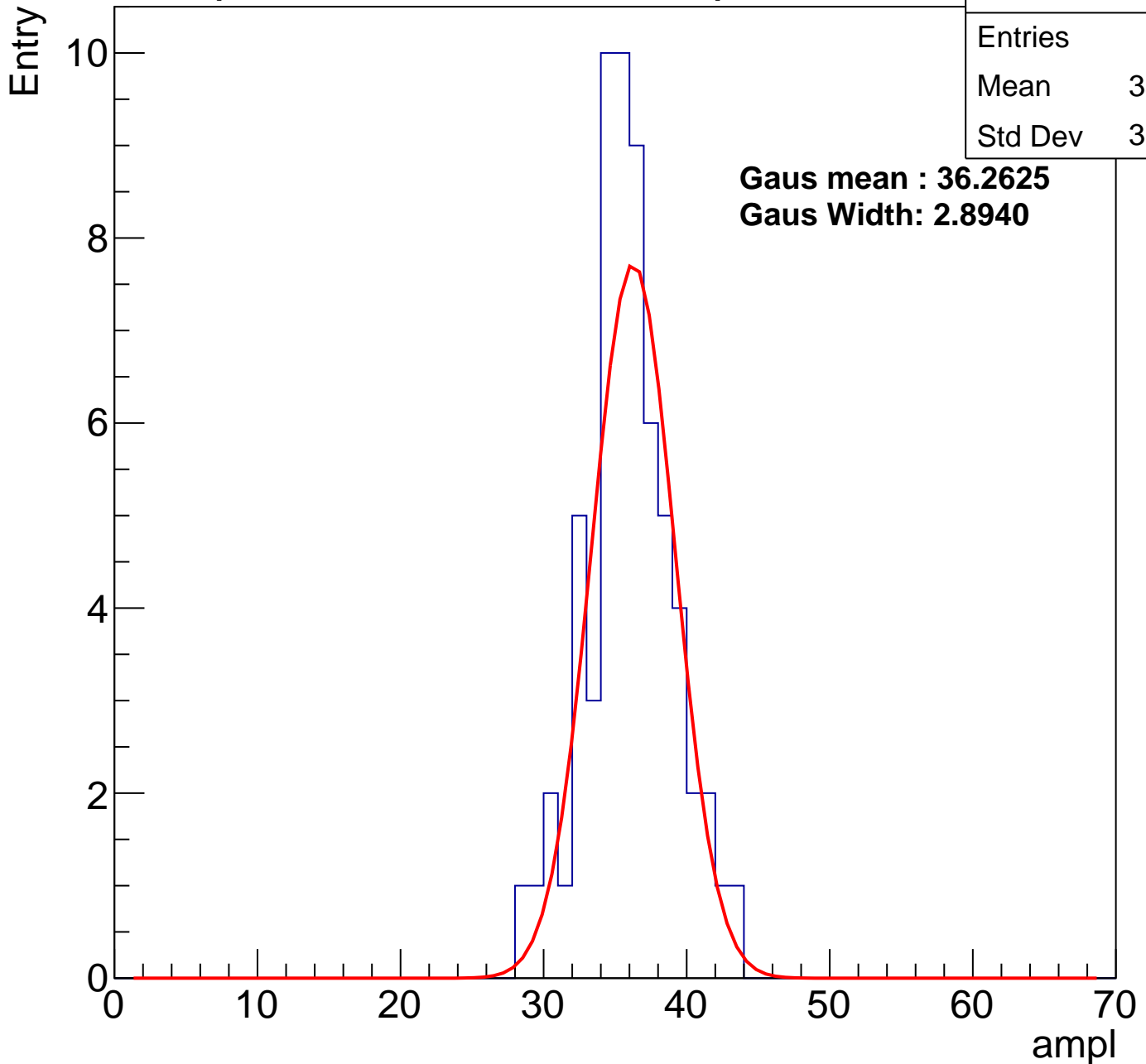


# B1L100S, U6-ch7, adc1

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	63
Mean	35.49
Std Dev	3.034

**Gaus mean : 36.2625**  
**Gaus Width: 2.8940**



# B1L100S, U6-ch7, adc2

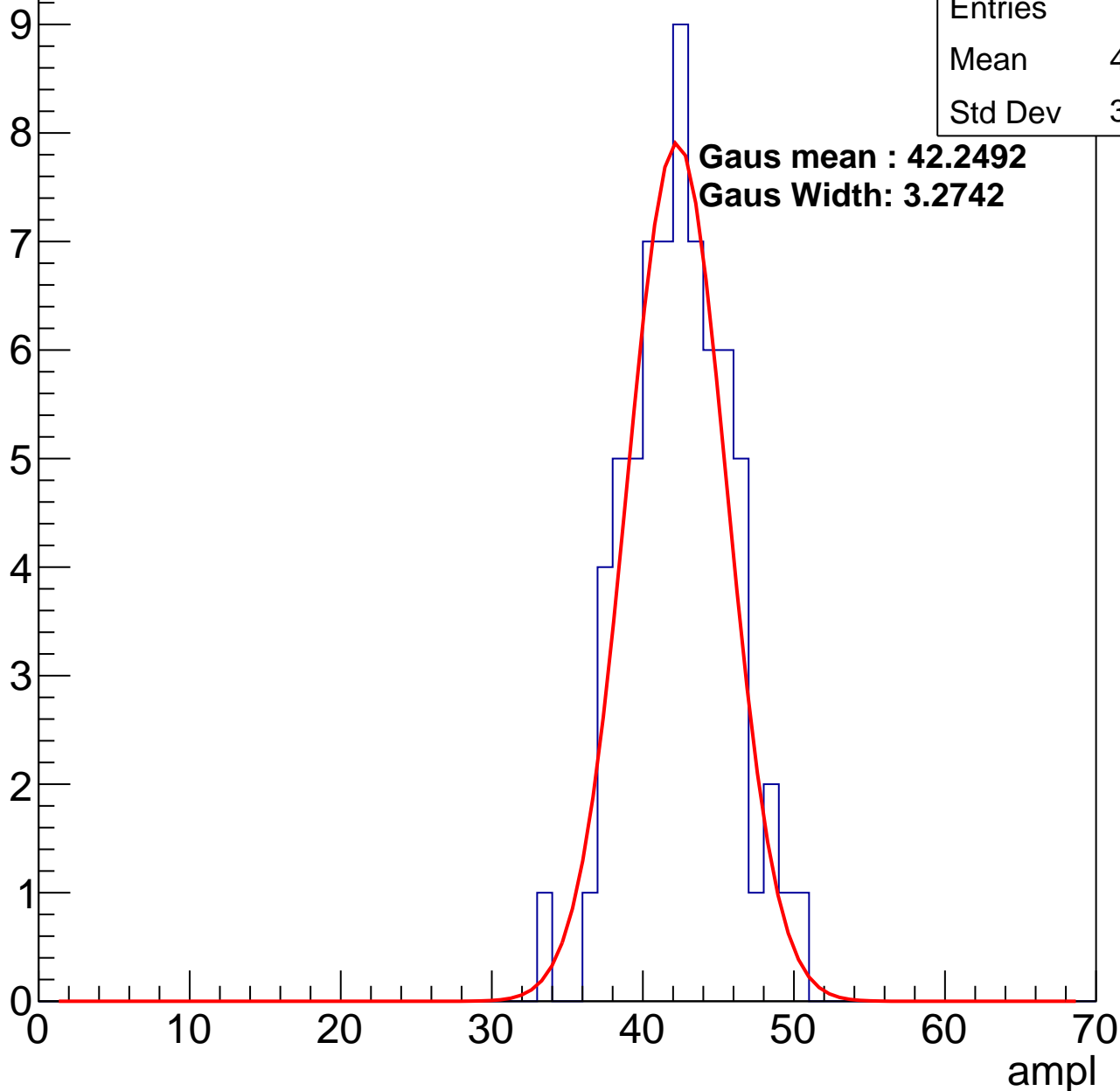
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	68
Mean	41.97
Std Dev	3.325

**Gaus mean : 42.2492**

**Gaus Width: 3.2742**

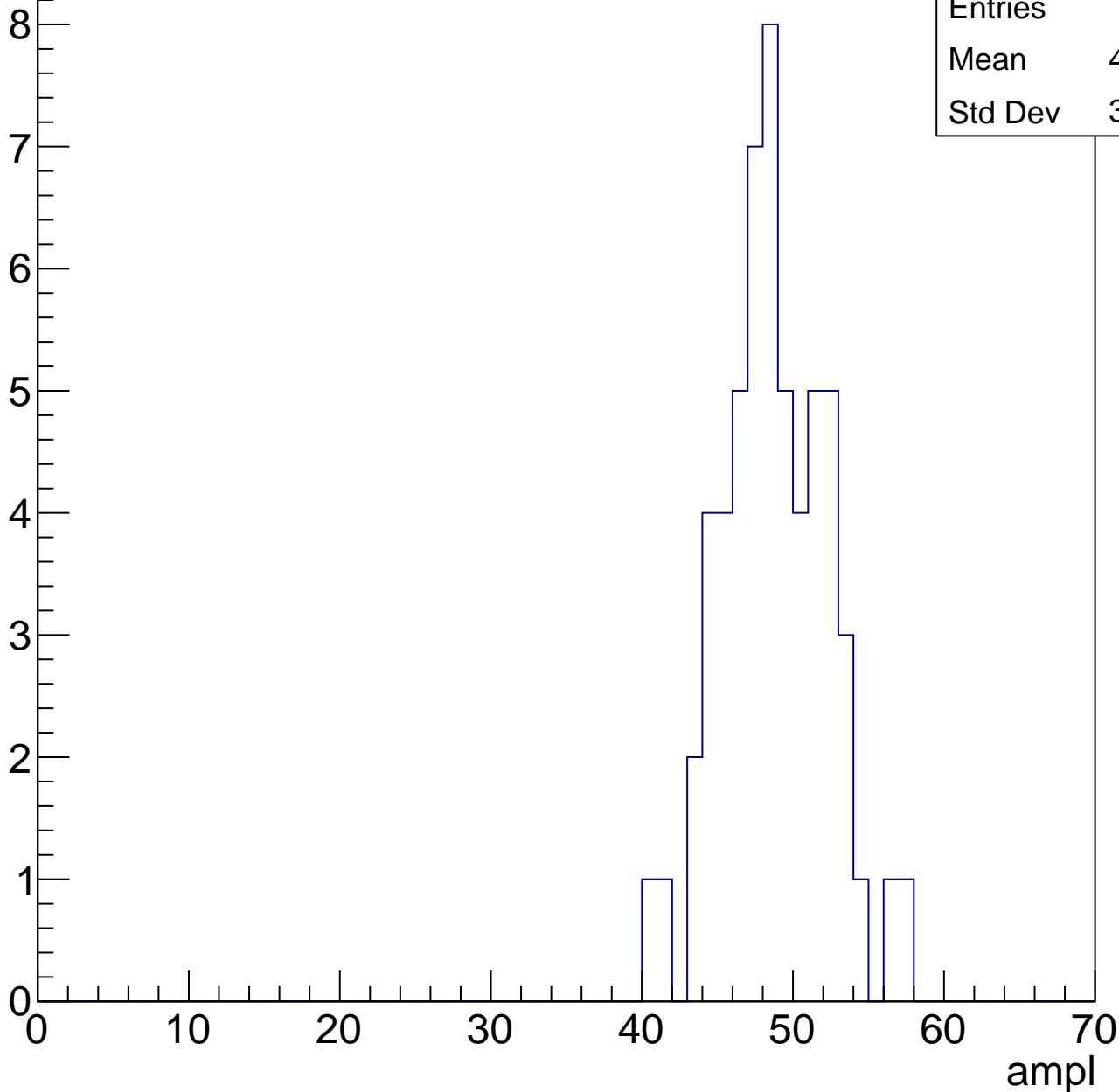


# B1L100S, U6-ch7, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	57
Mean	48.28
Std Dev	3.473

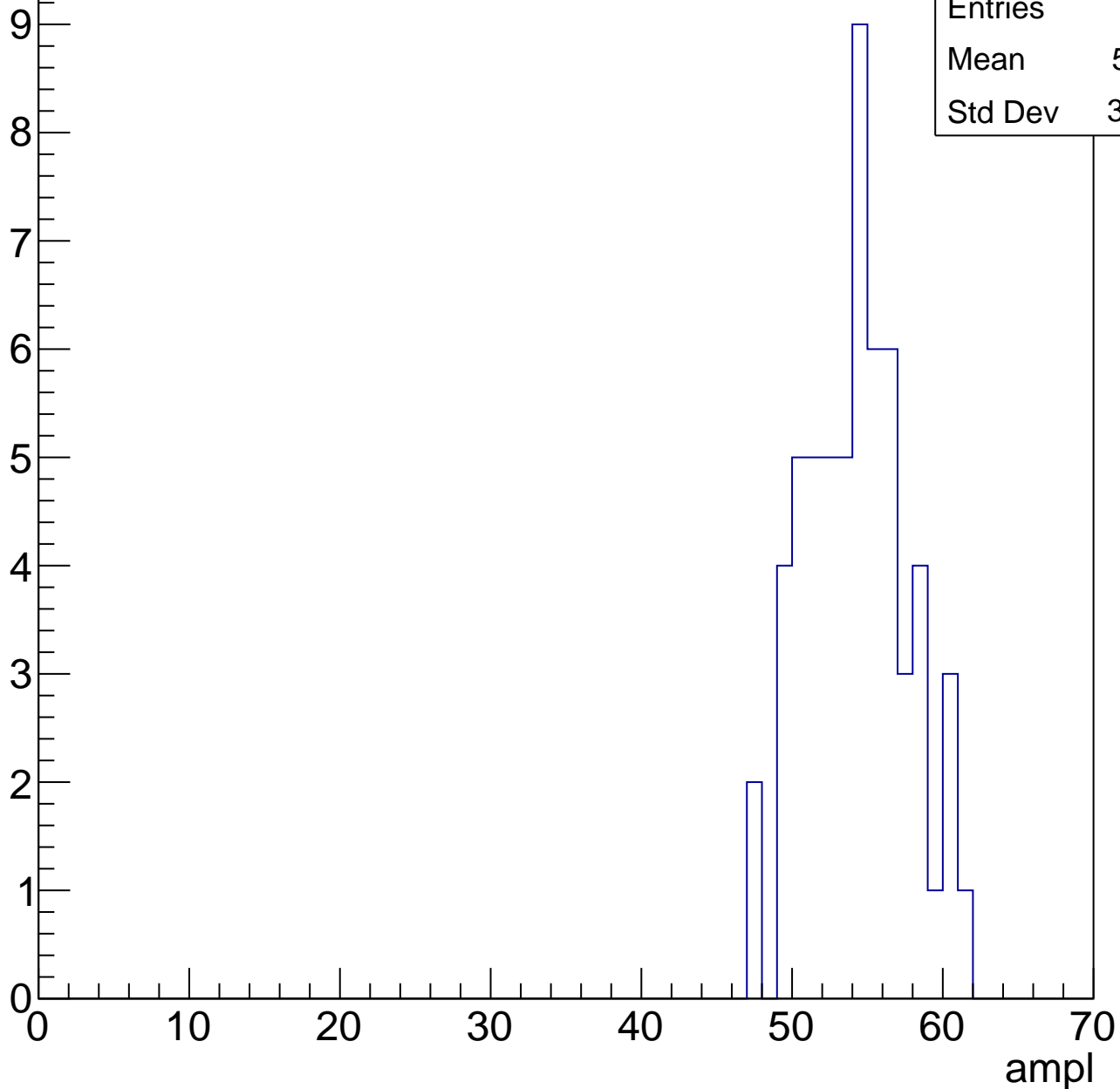


# B1L100S, U6-ch7, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	59
Mean	53.81
Std Dev	3.316

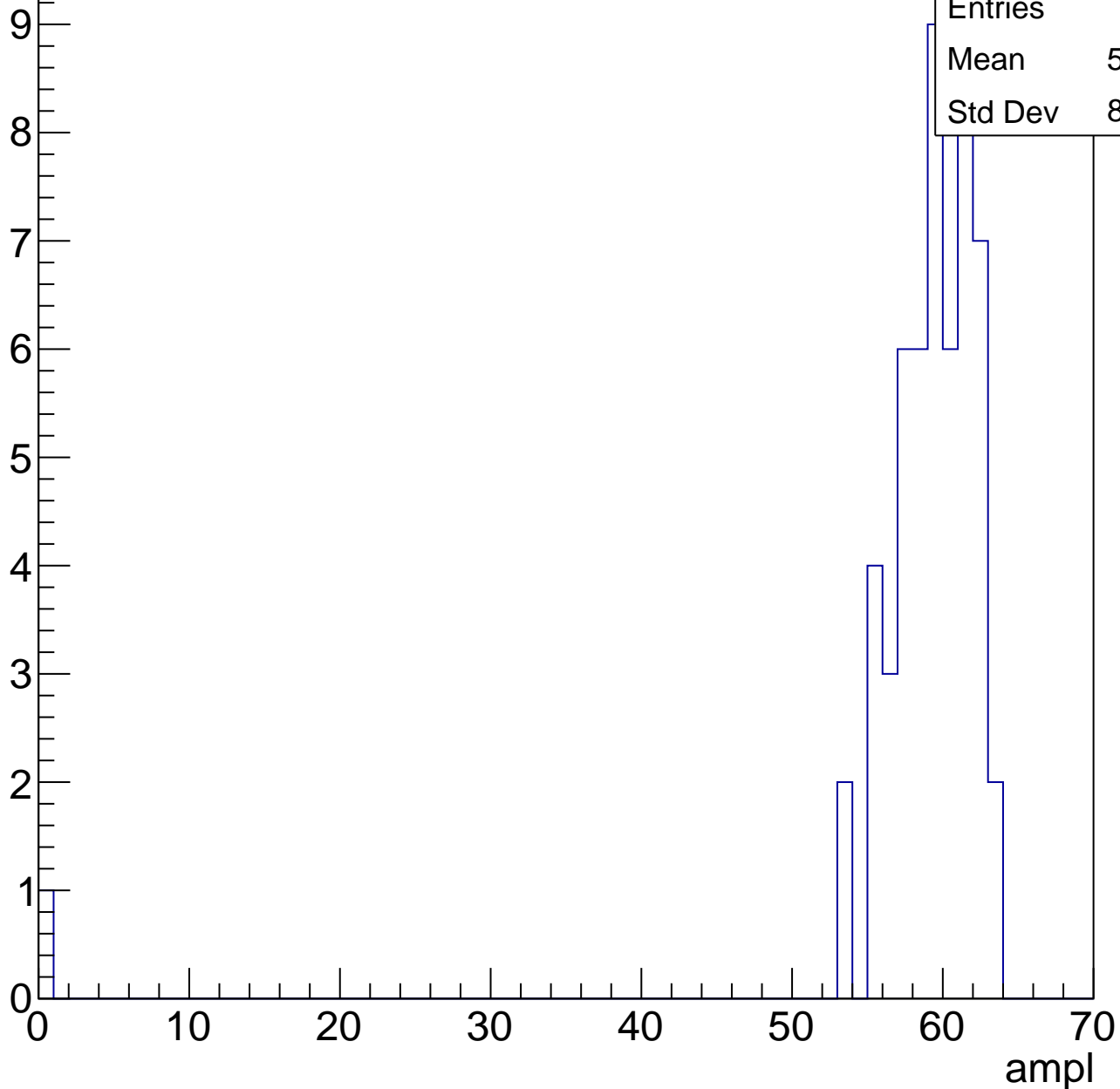


# B1L100S, U6-ch7, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	54
Mean	57.83
Std Dev	8.315

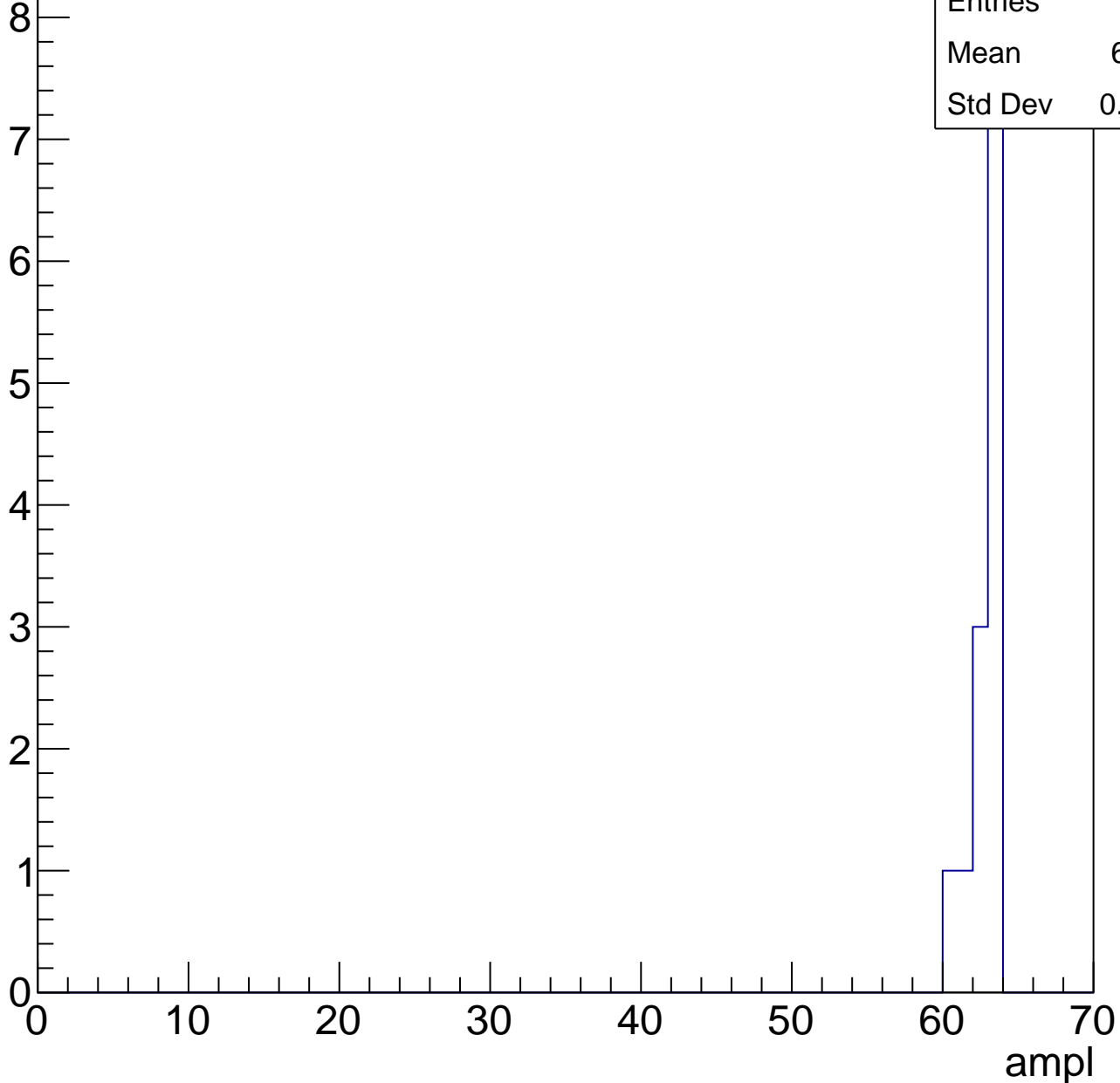


# B1L100S, U6-ch7, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	13
Mean	62.38
Std Dev	0.9231





# B1L100S, U6-ch7, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L100S, U6-ch8, adc0

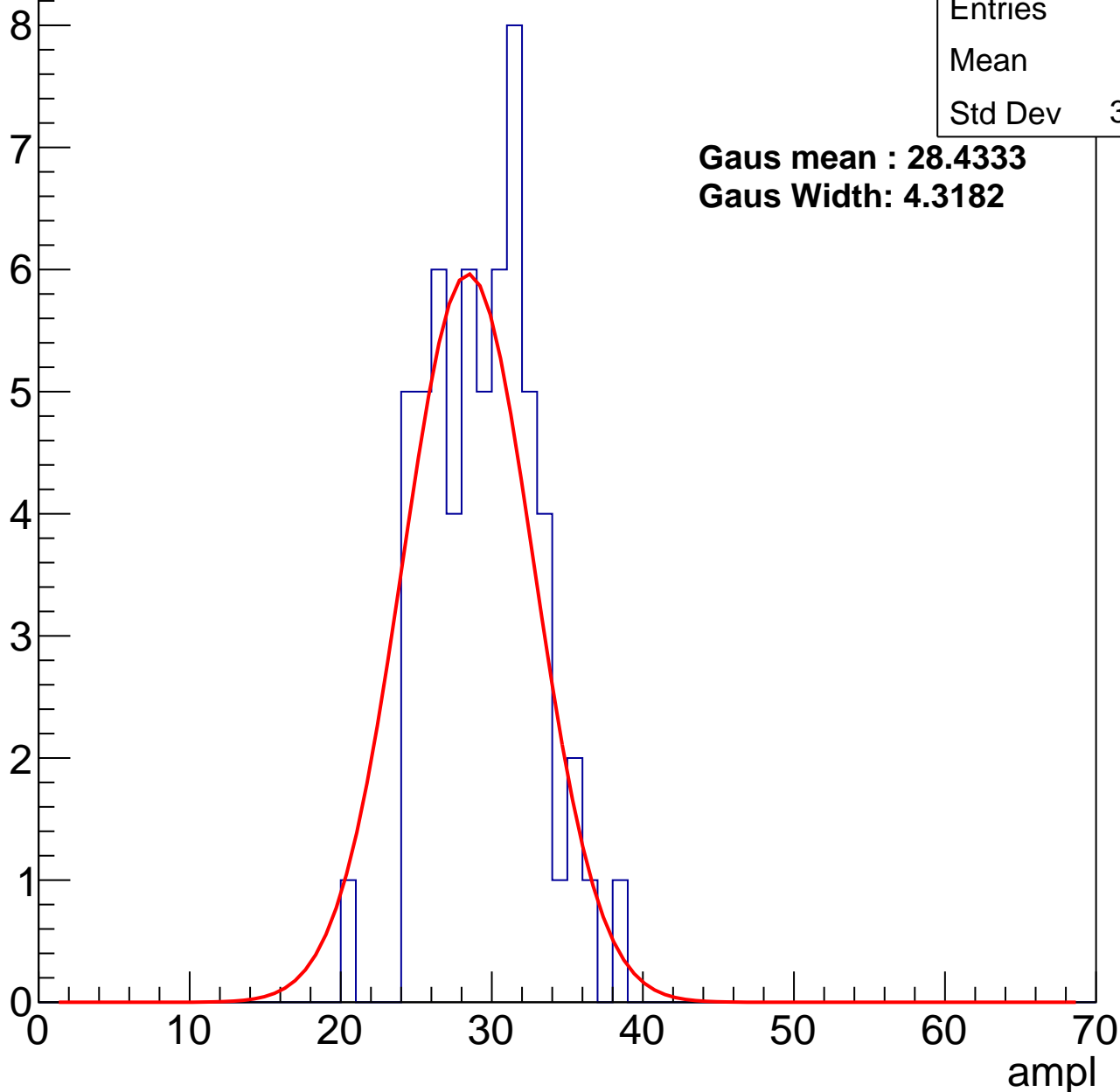
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	60
Mean	29
Std Dev	3.502

**Gaus mean : 28.4333**

**Gaus Width: 4.3182**



# B1L100S, U6-ch8, adc1

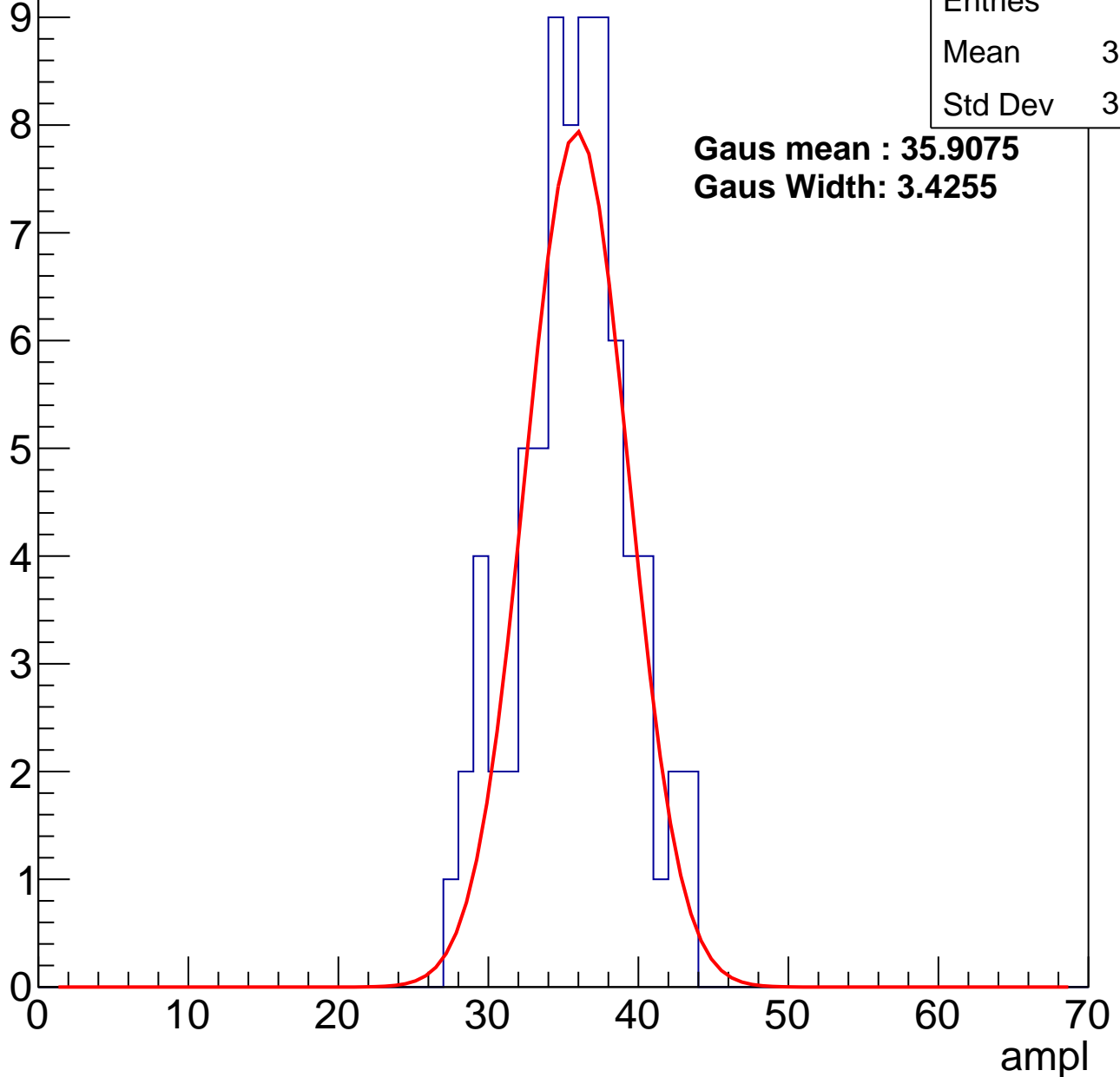
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	75
Mean	35.25
Std Dev	3.619

**Gaus mean : 35.9075**

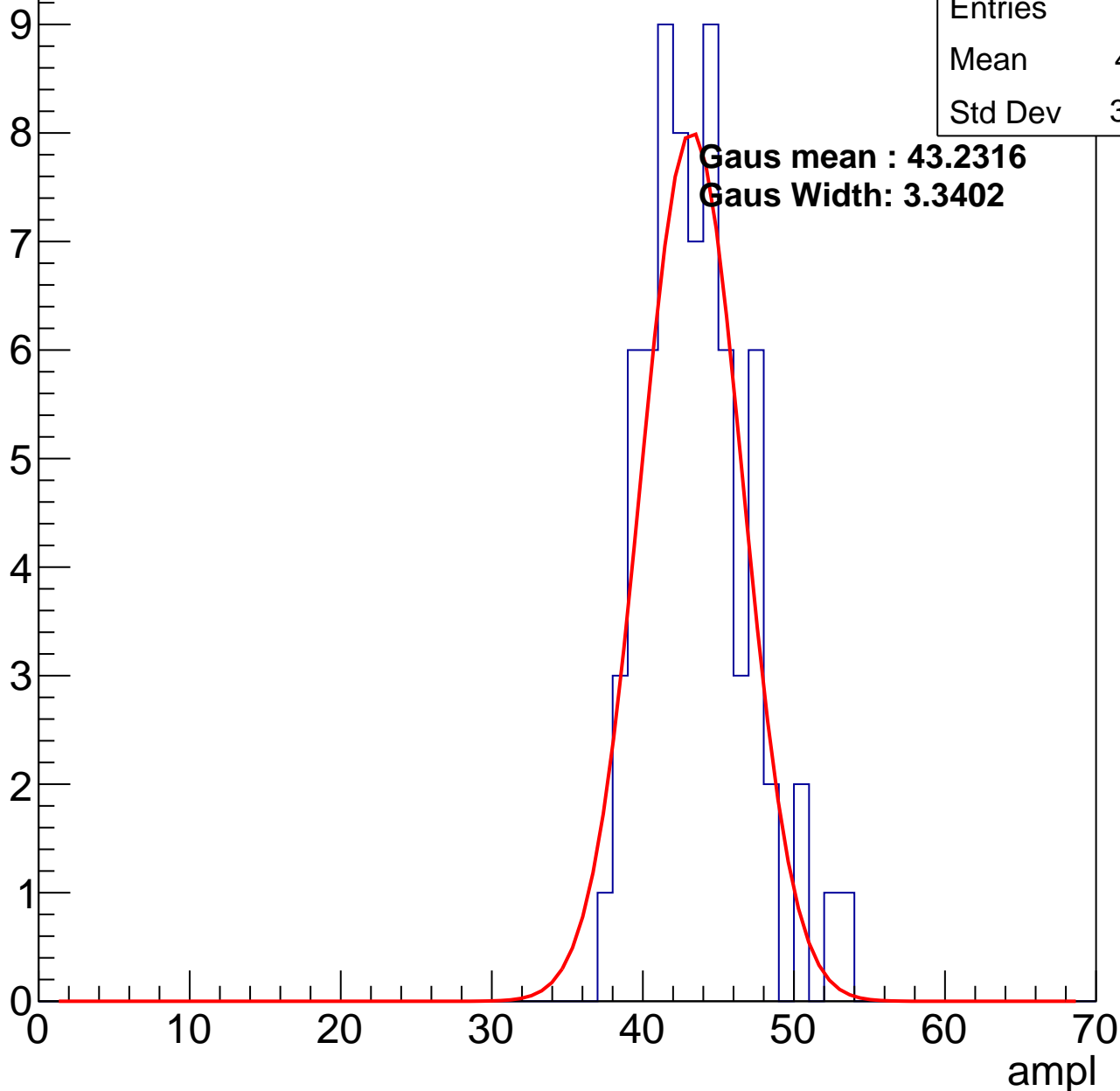
**Gaus Width: 3.4255**



# B1L100S, U6-ch8, adc2

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

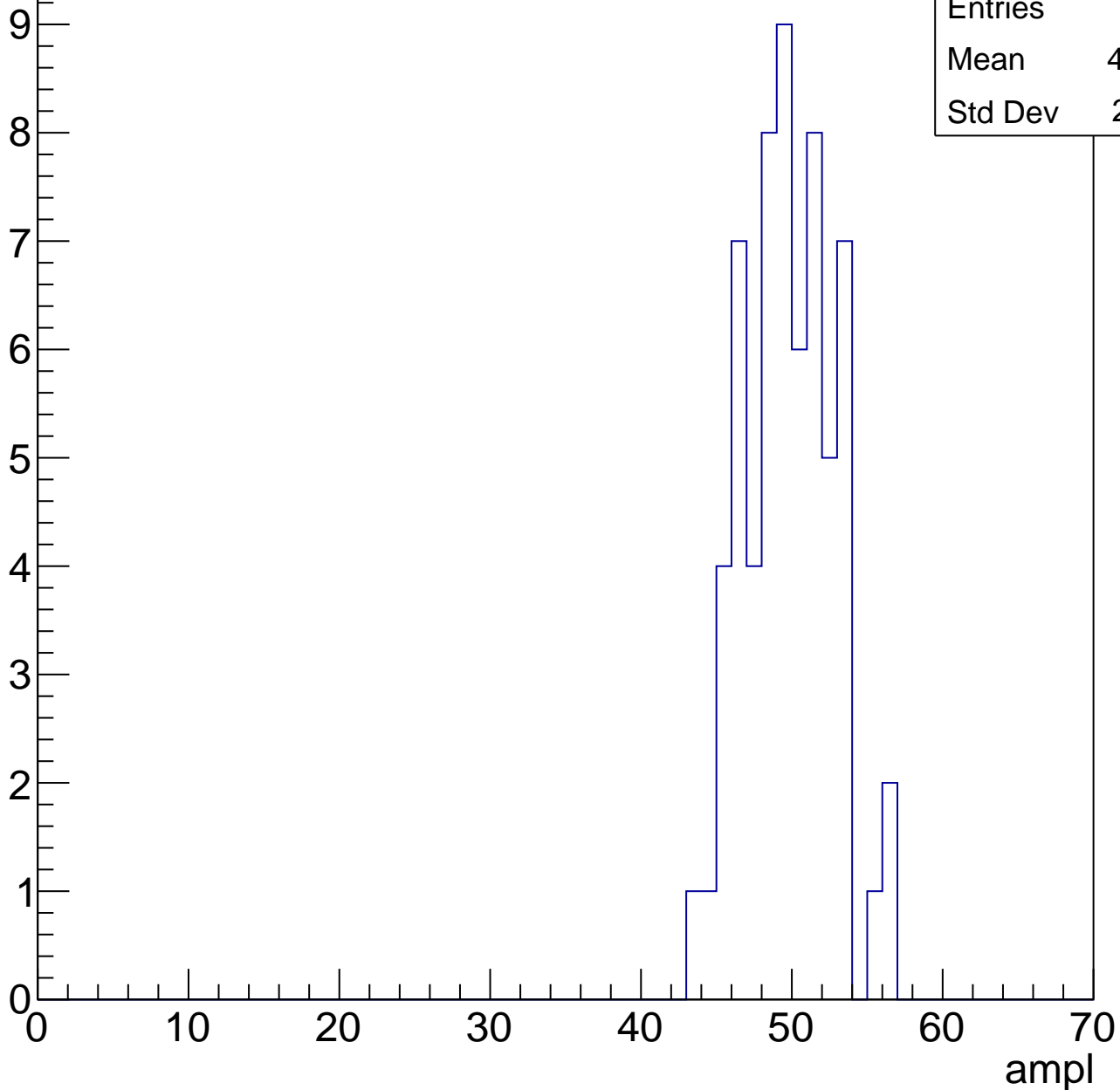


# B1L100S, U6-ch8, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	63
Mean	49.33
Std Dev	2.911

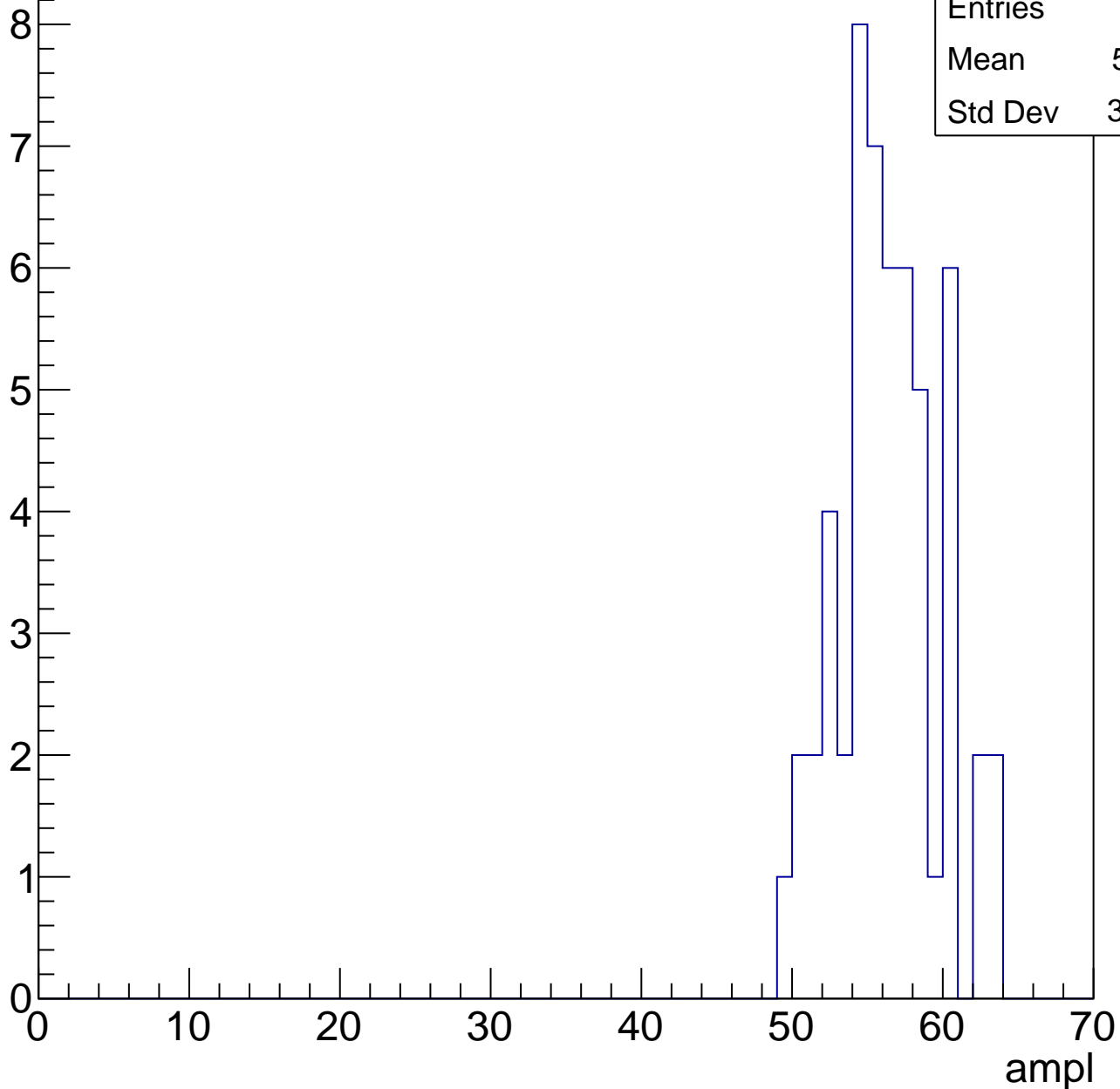


# B1L100S, U6-ch8, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

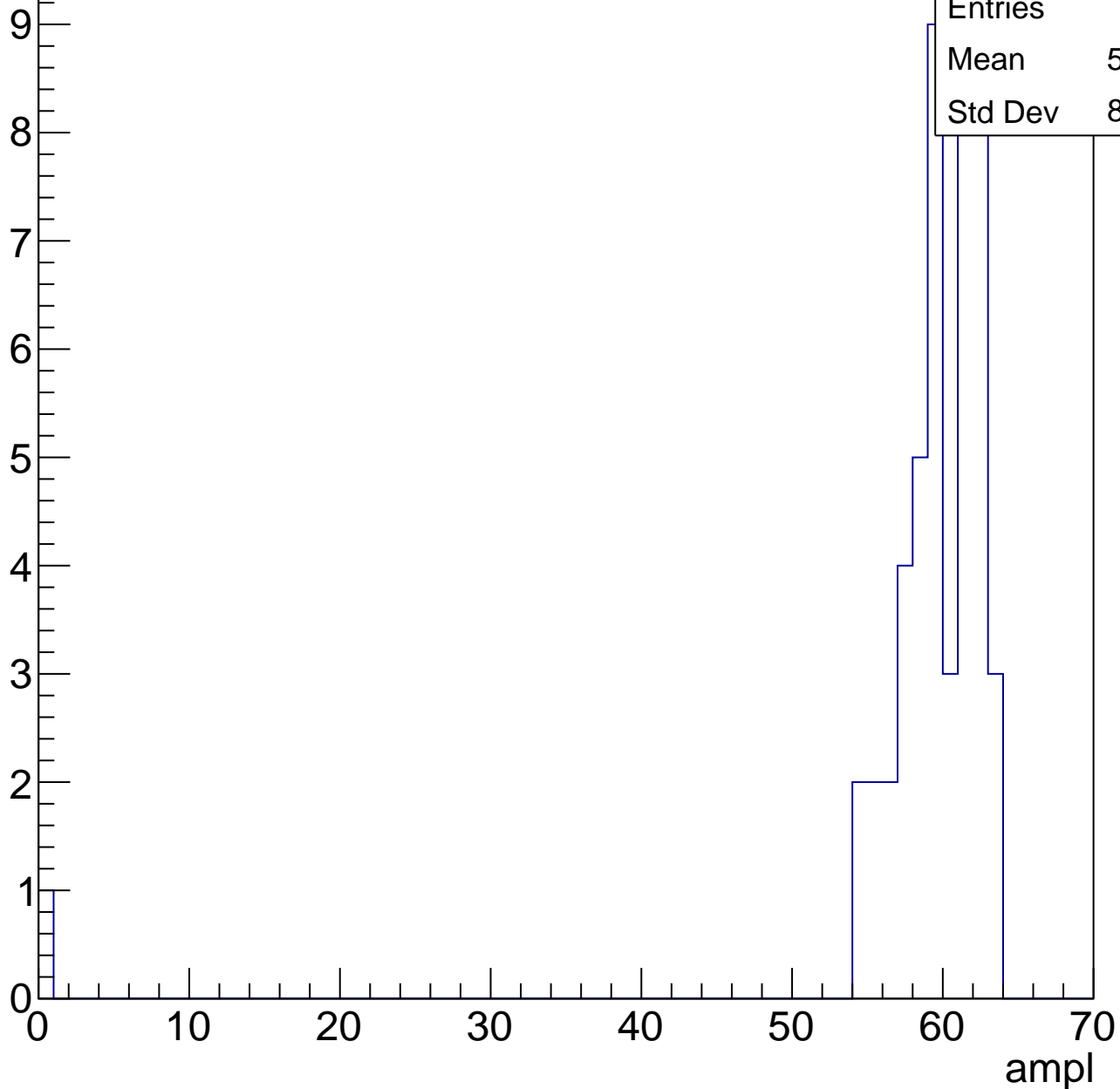
Entries	54
Mean	55.91
Std Dev	3.313



# B1L100S, U6-ch8, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

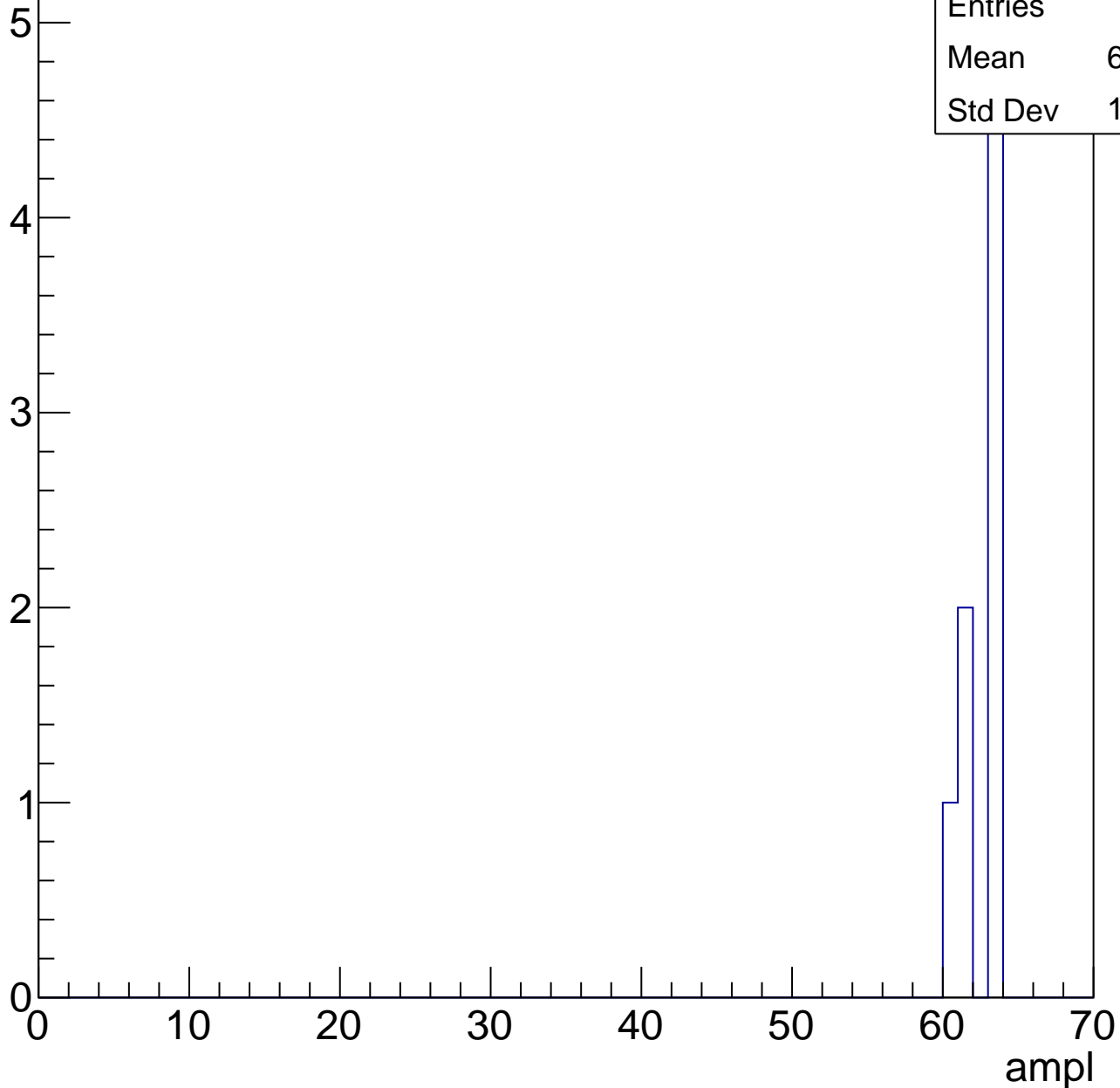


# B1L100S, U6-ch8, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	8
Mean	62.12
Std Dev	1.166





# B1L100S, U6-ch8, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



# B1L100S, U6-ch9, adc0

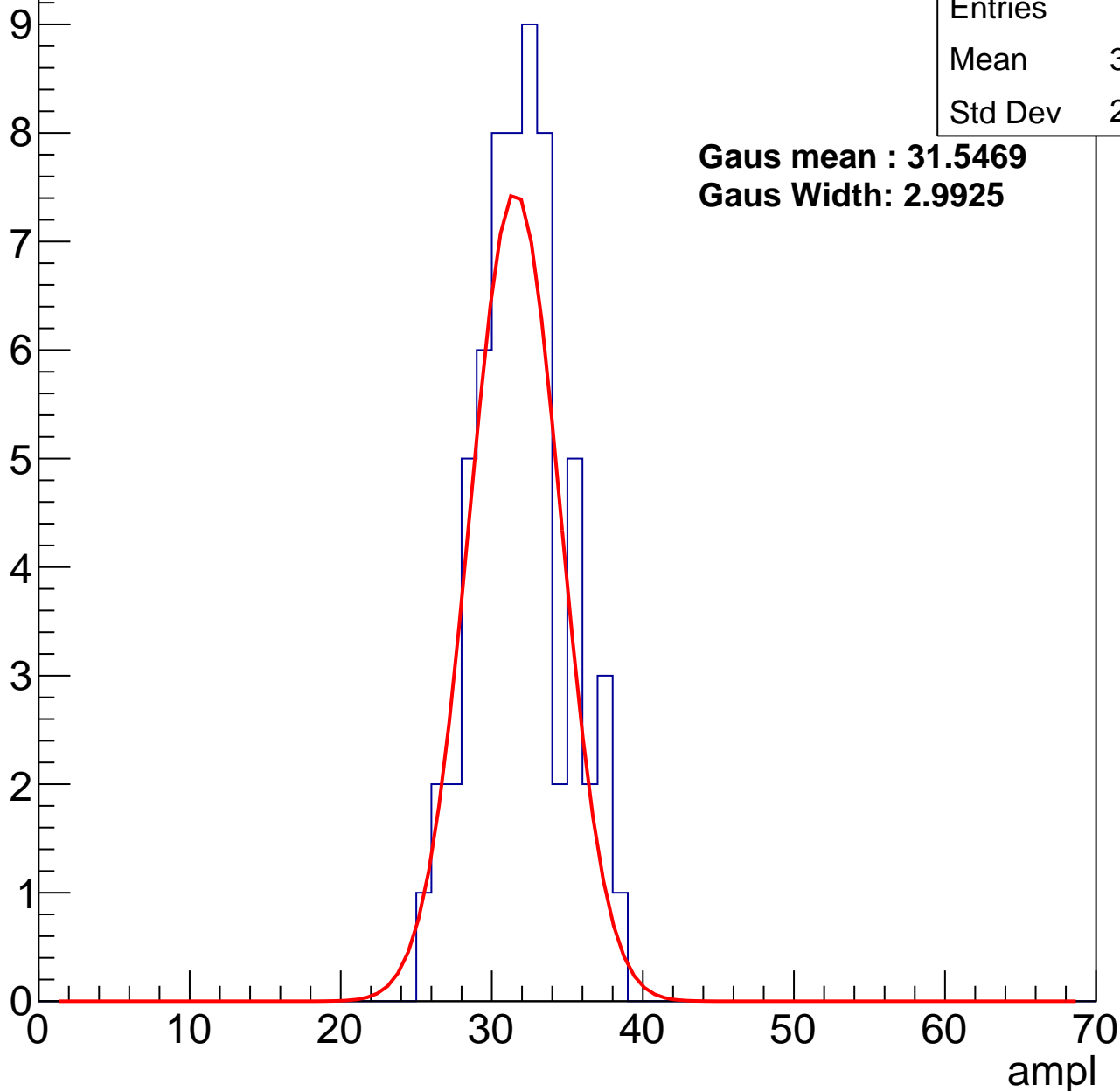
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	62
Mean	31.44
Std Dev	2.922

**Gaus mean : 31.5469**

**Gaus Width: 2.9925**



# B1L100S, U6-ch9, adc1

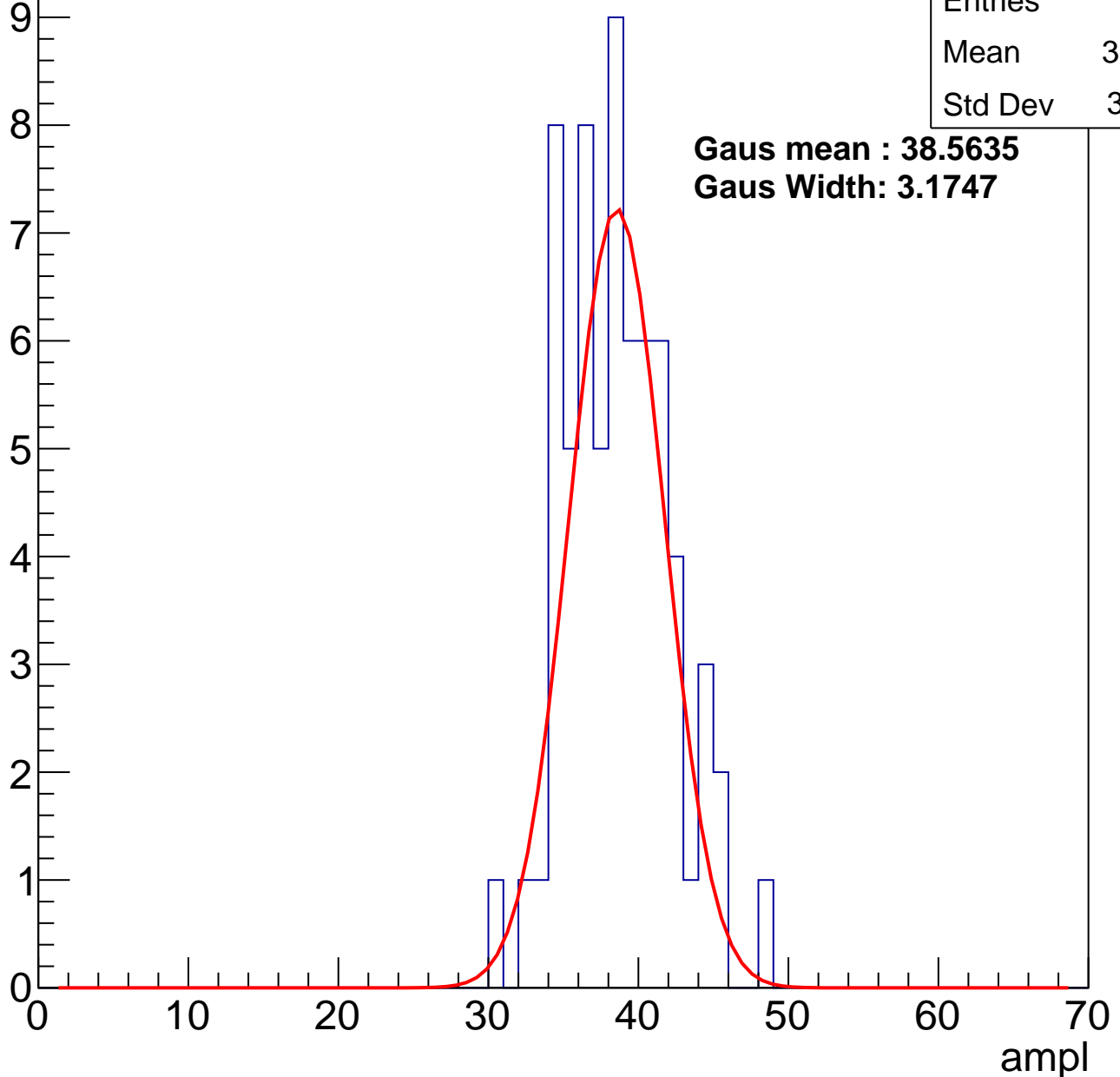
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	67
Mean	38.18
Std Dev	3.481

**Gaus mean : 38.5635**

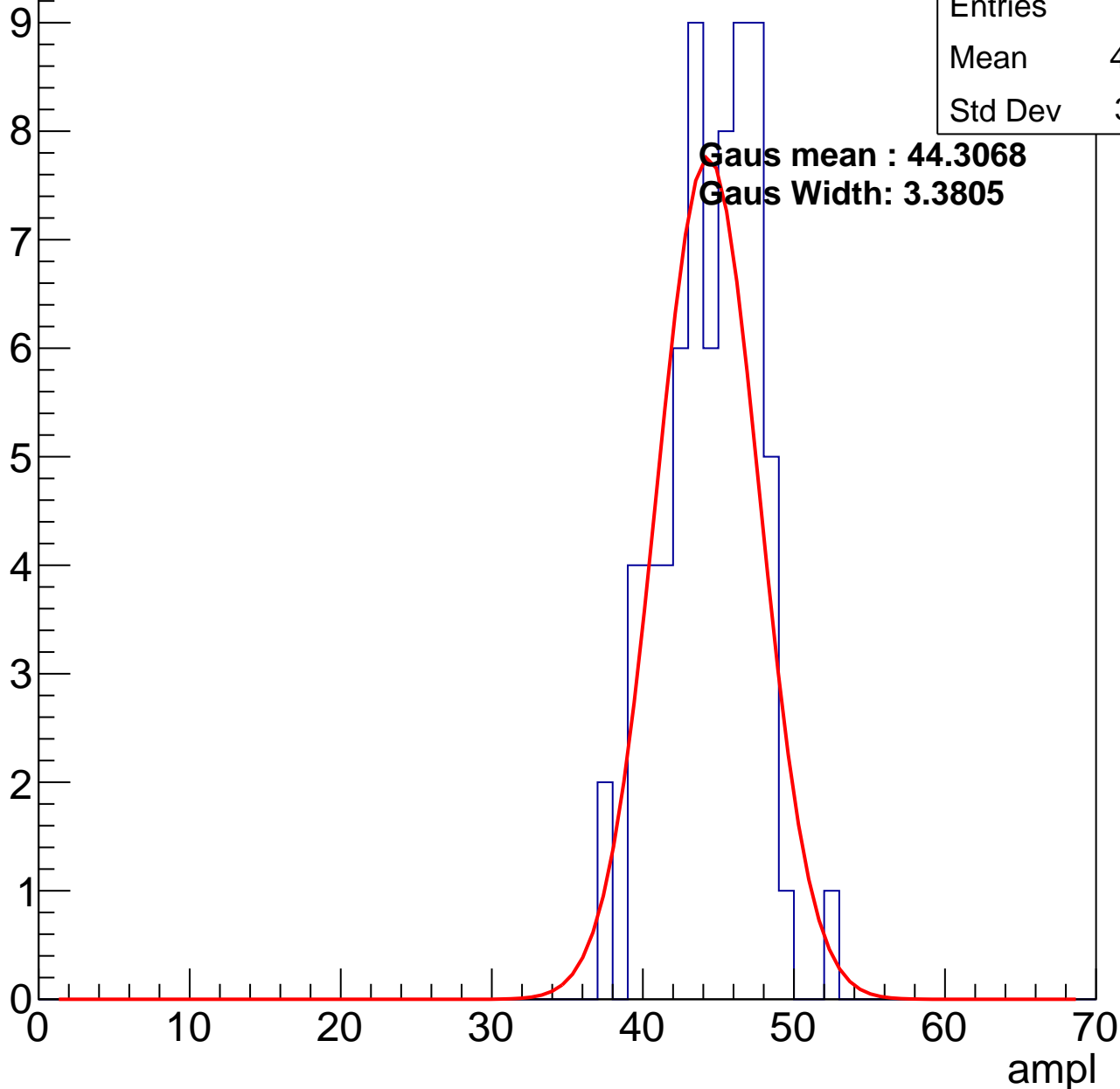
**Gaus Width: 3.1747**



# B1L100S, U6-ch9, adc2

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

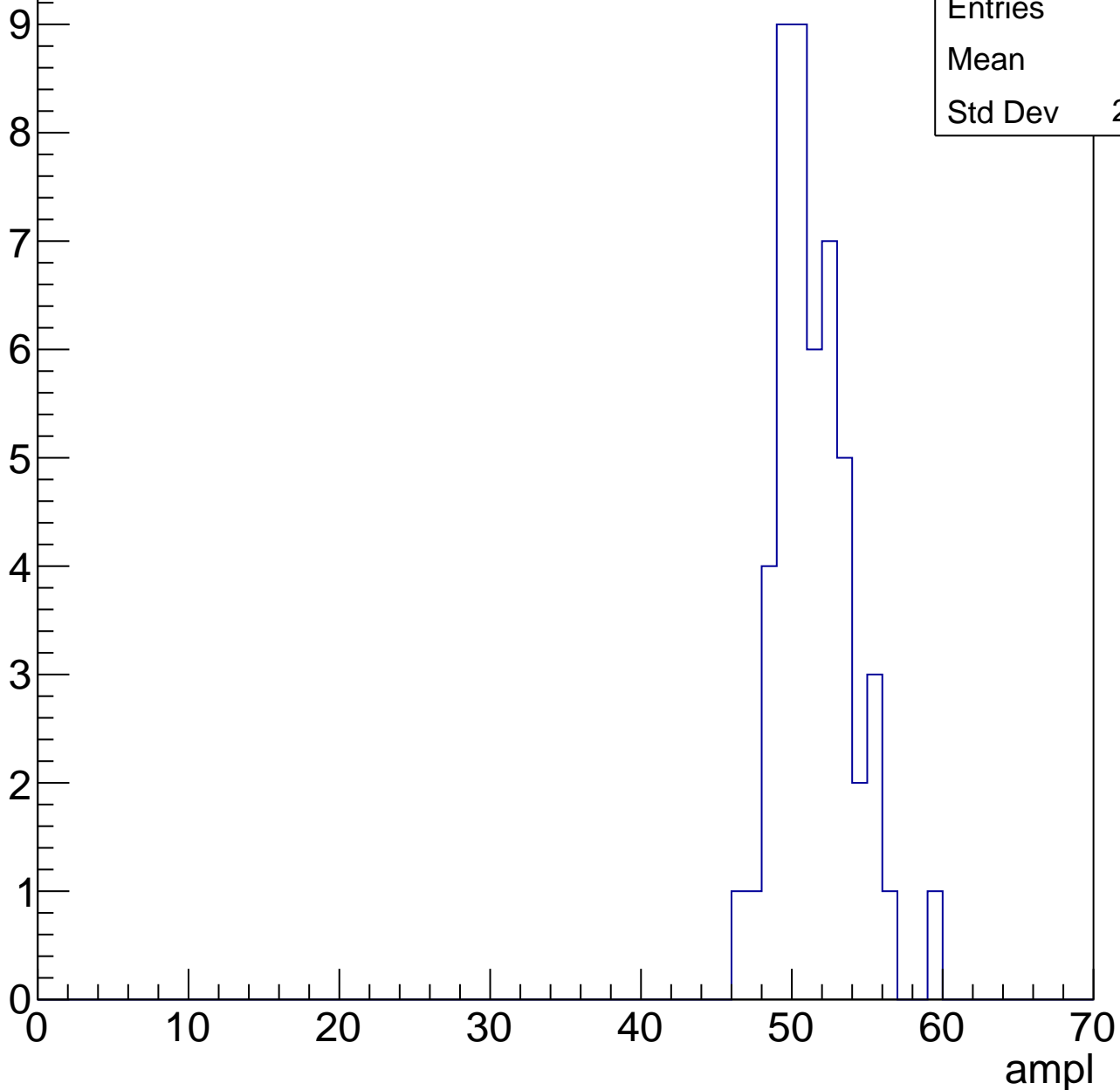


# B1L100S, U6-ch9, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	49
Mean	51
Std Dev	2.491

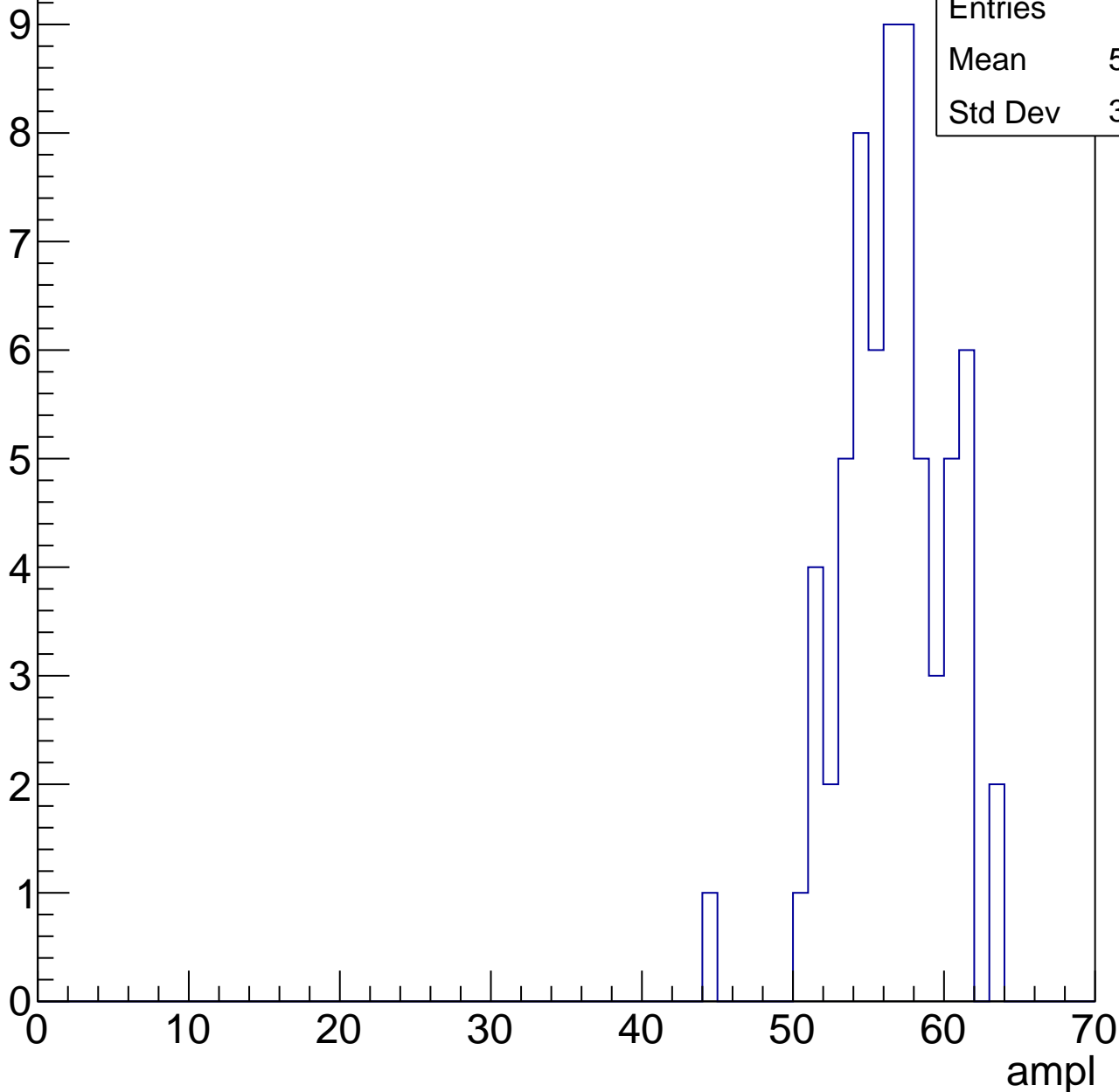


# B1L100S, U6-ch9, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	66
Mean	56.14
Std Dev	3.433

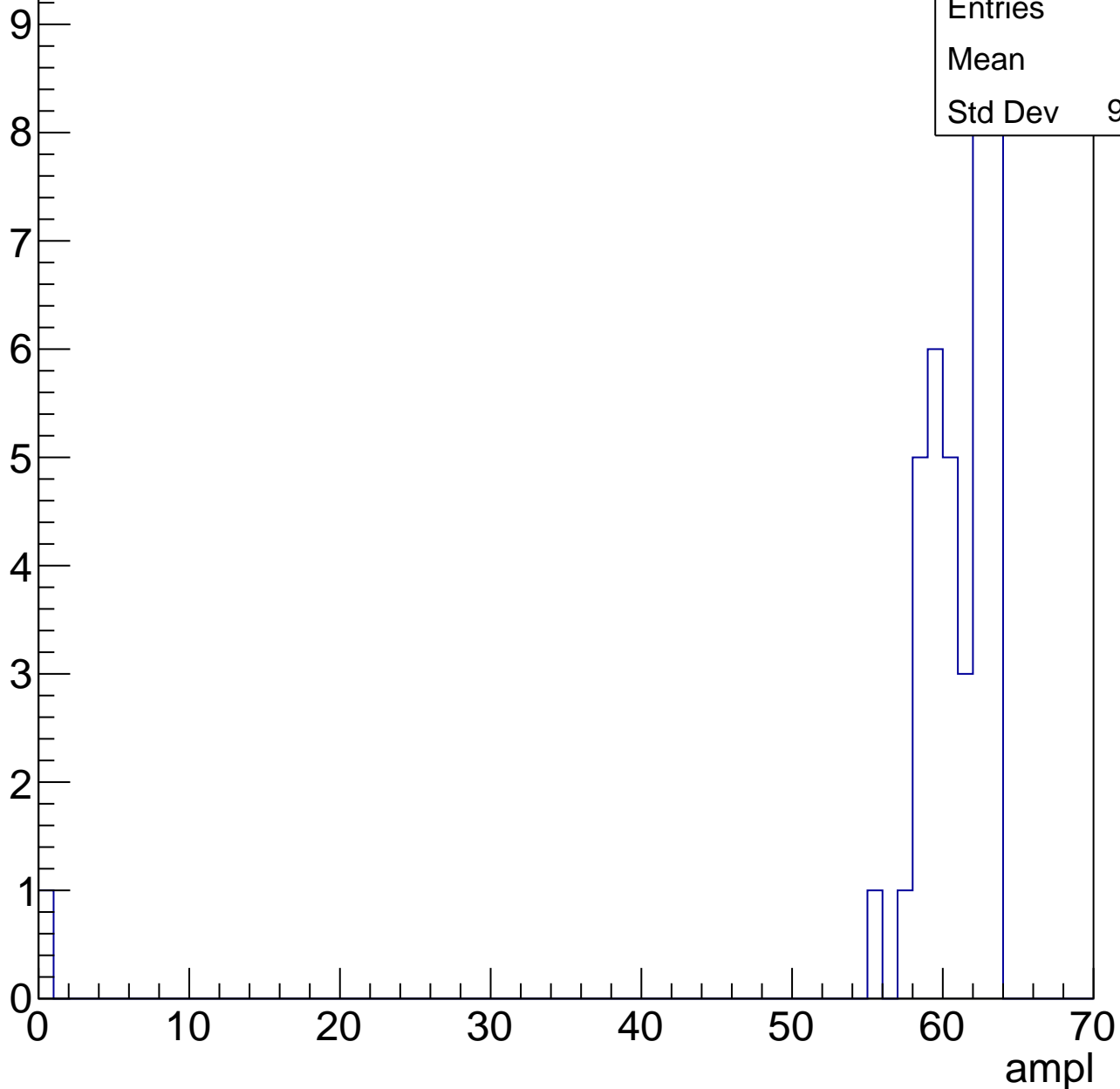


# B1L100S, U6-ch9, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	39
Mean	59
Std Dev	9.782



# B1L100S, U6-ch9, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

1  
0.8  
0.6  
0.4  
0.2  
0

Entries	2
Mean	61.5
Std Dev	0.5

ampl



# B1L100S, U6-ch9, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

1  
0.8  
0.6  
0.4  
0.2  
0

Entries	1
Mean	24
Std Dev	0

ampl

0 10 20 30 40 50 60 70

# B1L100S, U6-ch10, adc0

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	66
Mean	29.83
Std Dev	3.432

**Gaus mean : 30.4968**

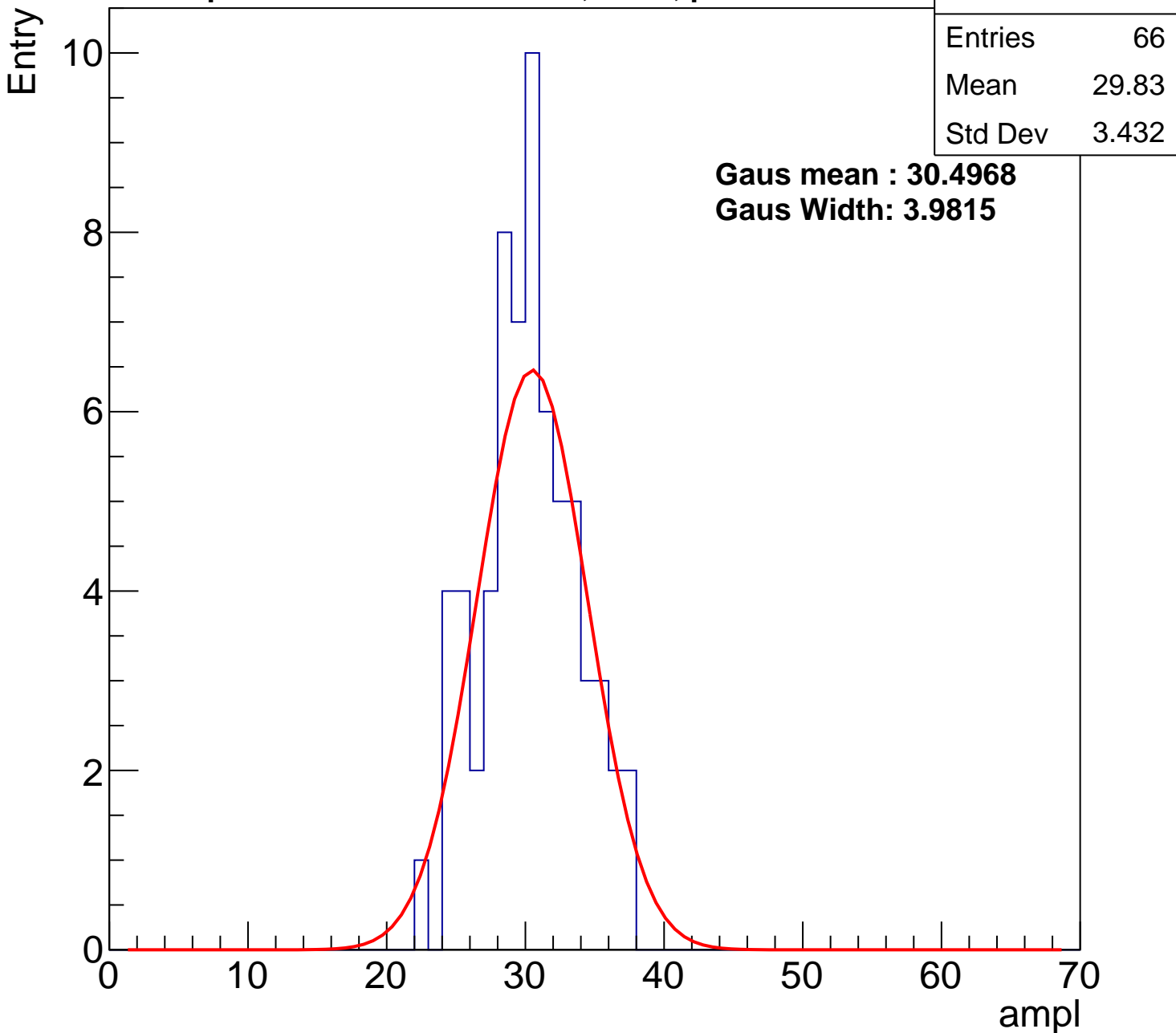
**Gaus Width: 3.9815**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L100S, U6-ch10, adc1

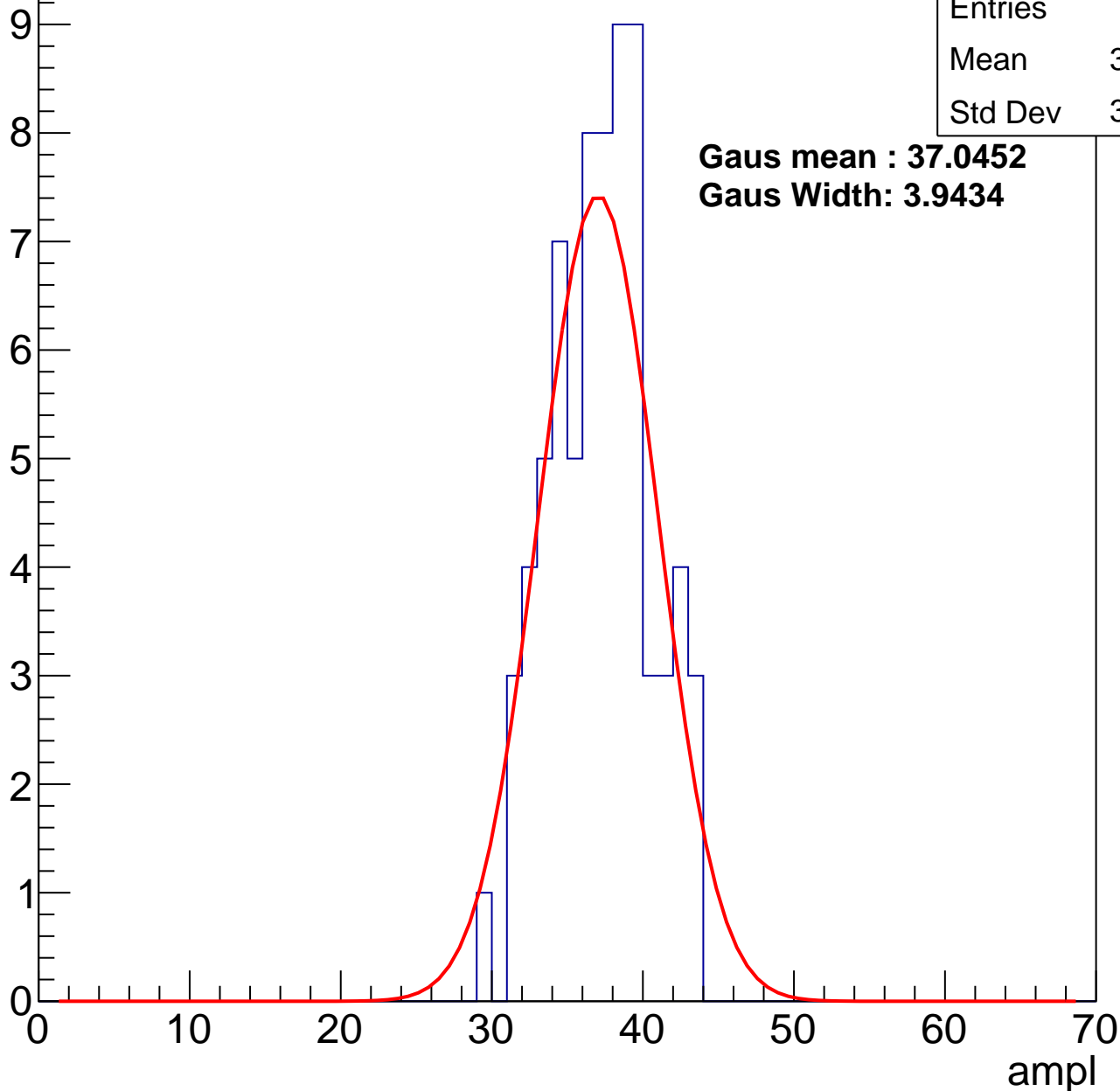
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	72
Mean	36.74
Std Dev	3.262

**Gaus mean : 37.0452**

**Gaus Width: 3.9434**



# B1L100S, U6-ch10, adc2

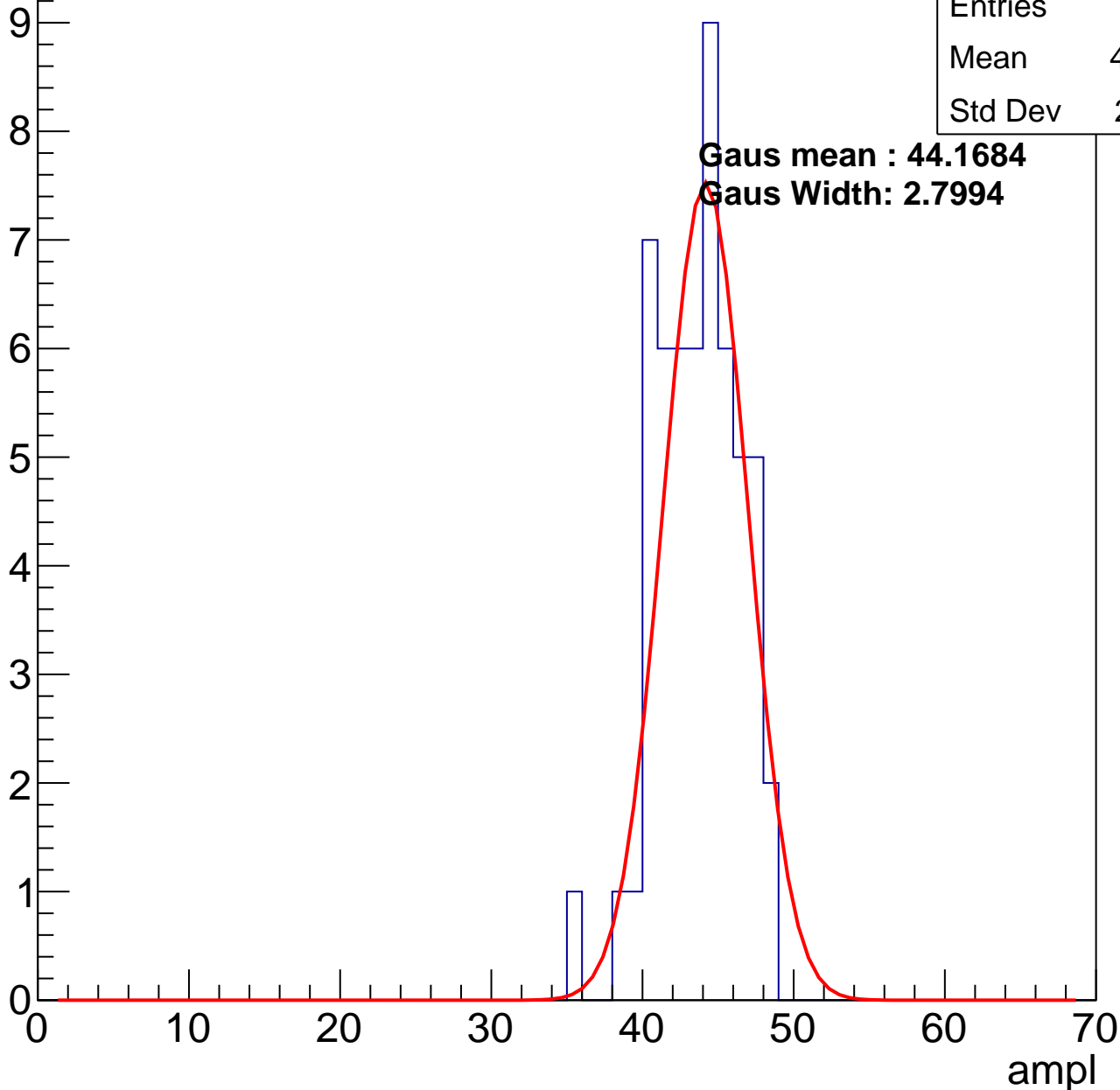
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	55
Mean	43.18
Std Dev	2.711

**Gaus mean : 44.1684**

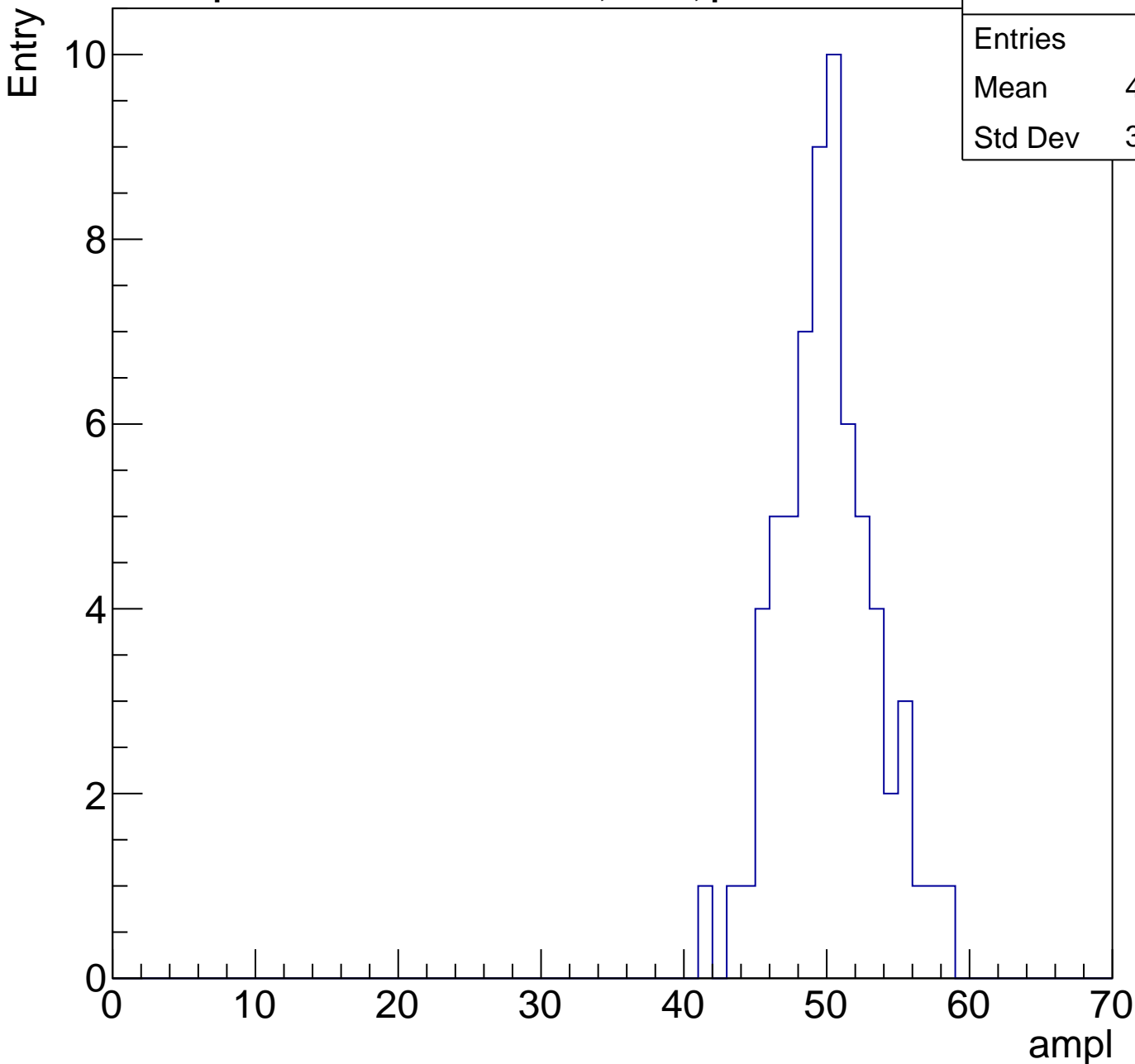
**Gaus Width: 2.7994**



# B1L100S, U6-ch10, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	66
Mean	49.58
Std Dev	3.335

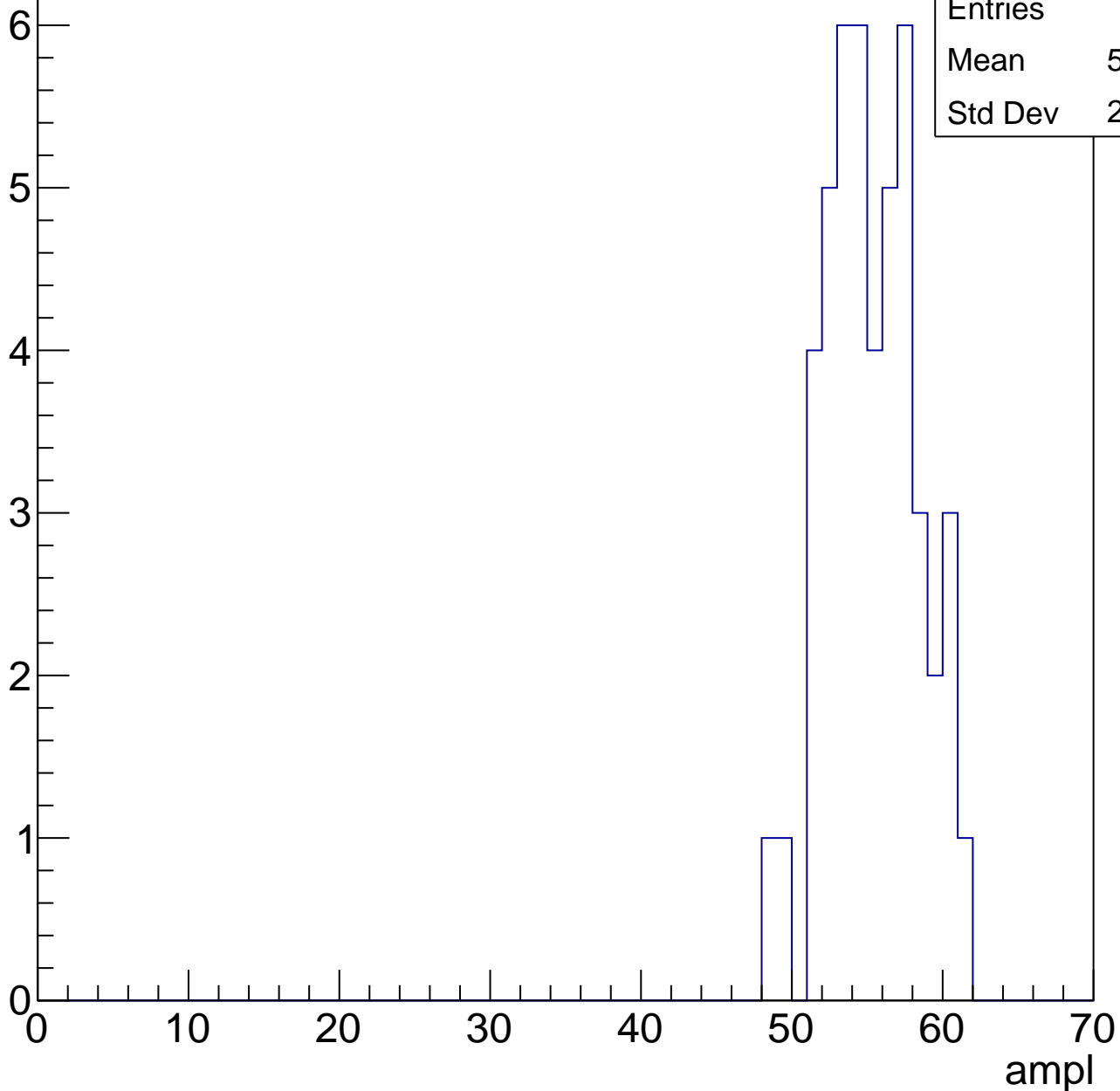


# B1L100S, U6-ch10, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

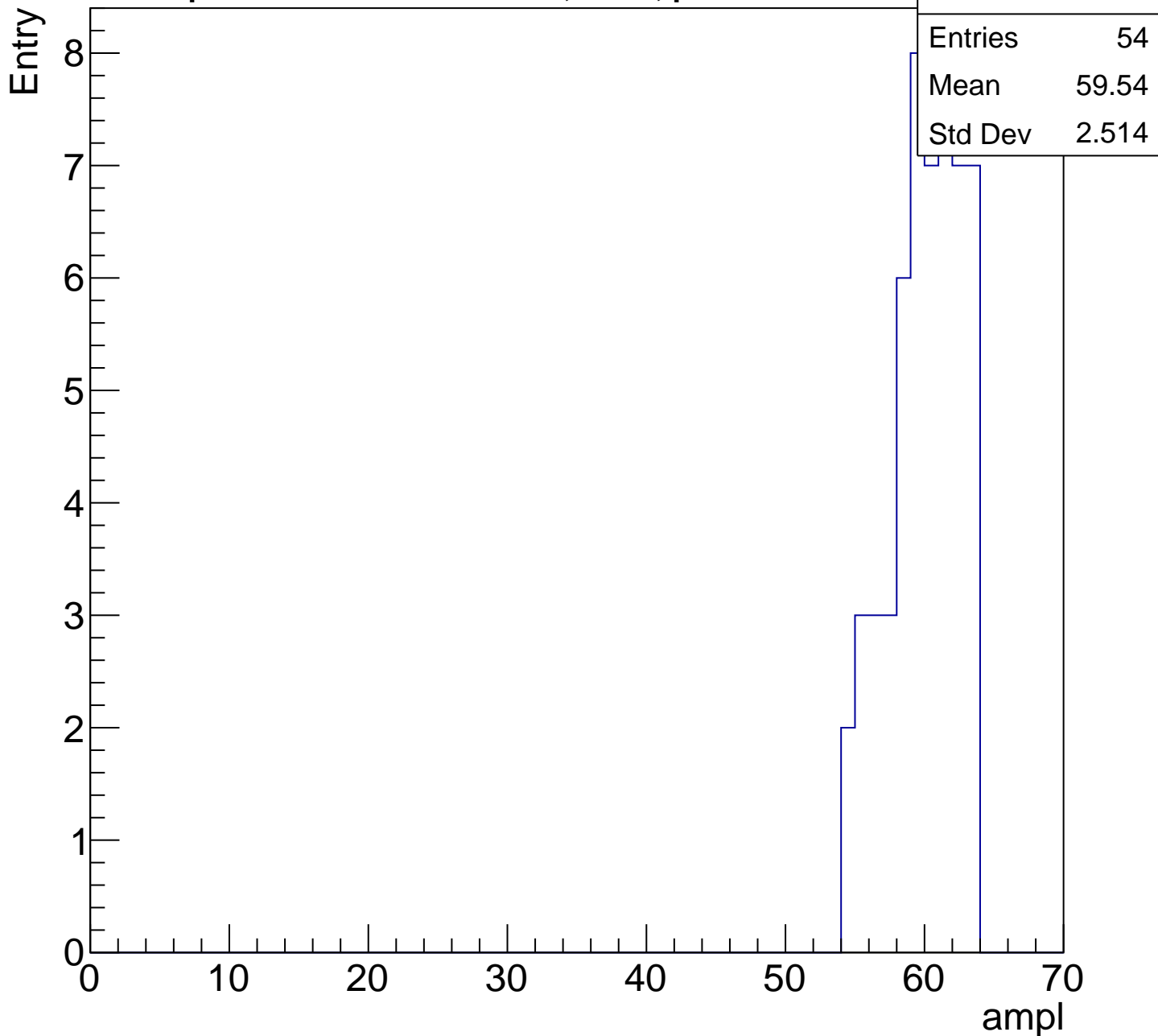
Entry

Entries	47
Mean	54.85
Std Dev	2.996



# B1L100S, U6-ch10, adc5

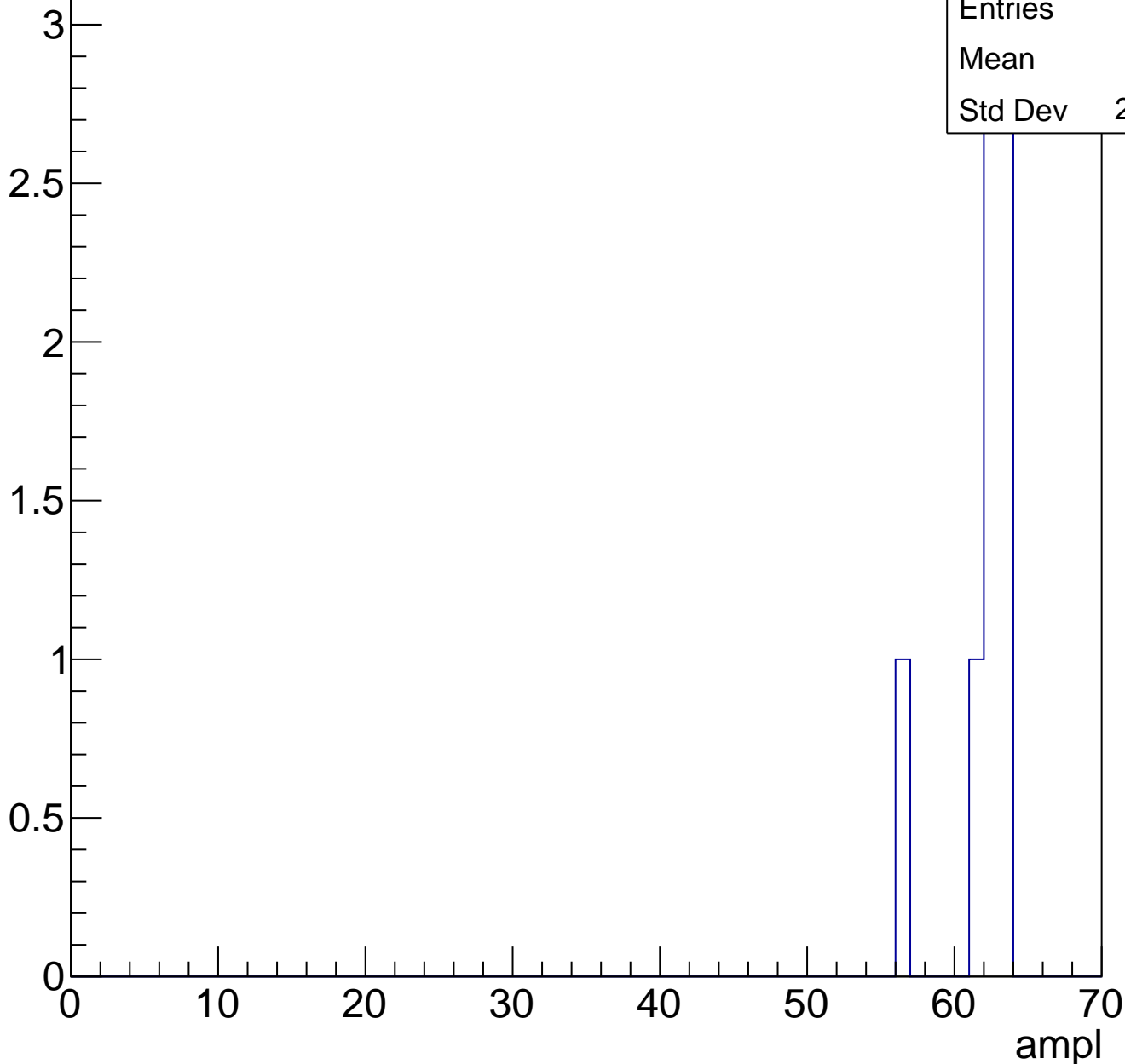
calib\_packv5\_042523\_0143.root, FC#4, port A2



# B1L100S, U6-ch10, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry





# B1L100S, U6-ch10, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



# B1L100S, U6-ch11, adc0

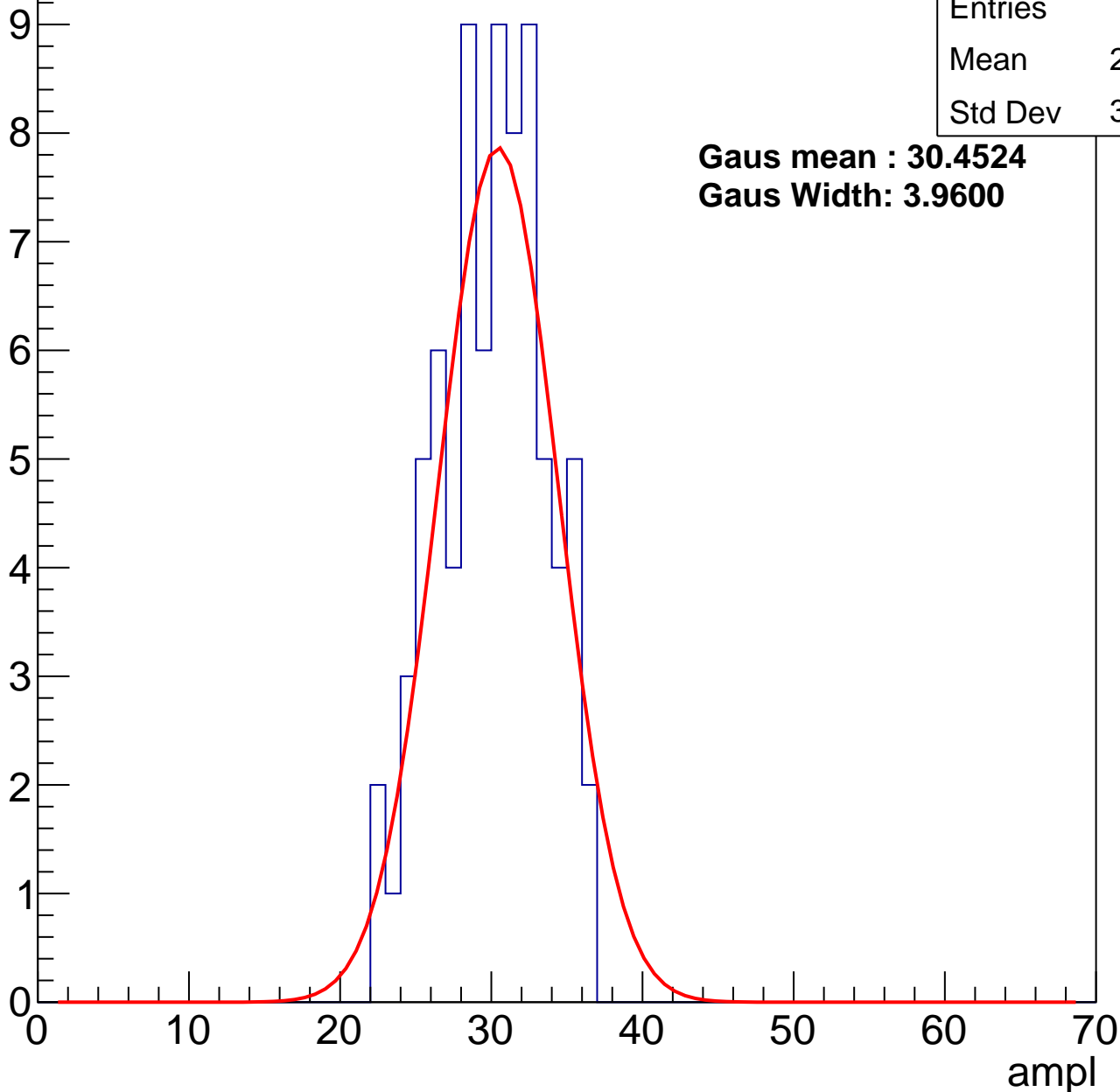
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	78
Mean	29.59
Std Dev	3.436

**Gaus mean : 30.4524**

**Gaus Width: 3.9600**



# B1L100S, U6-ch11, adc1

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	62
Mean	36.82
Std Dev	3.15

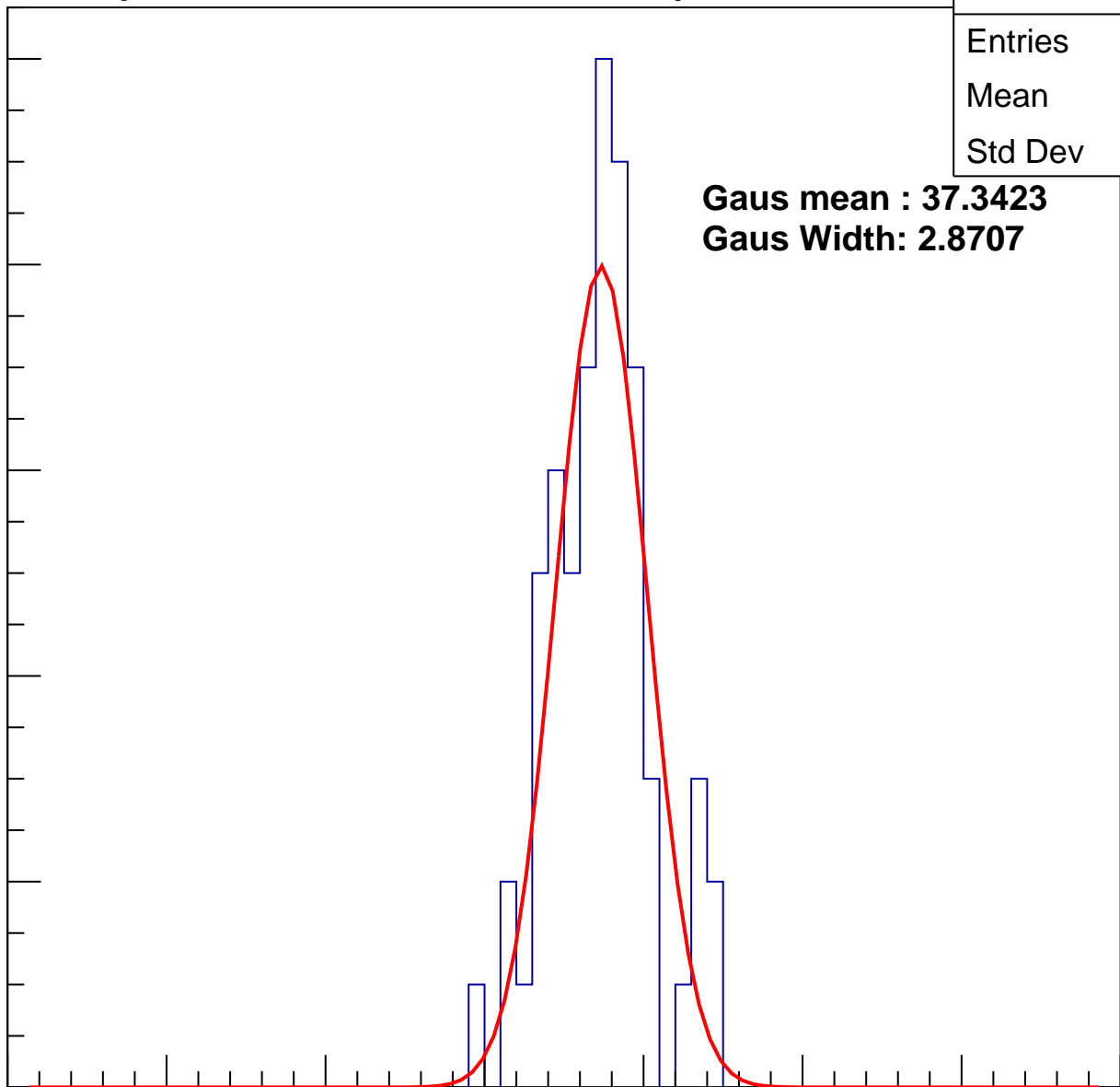
**Gaus mean : 37.3423**  
**Gaus Width: 2.8707**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B1L100S, U6-ch11, adc2

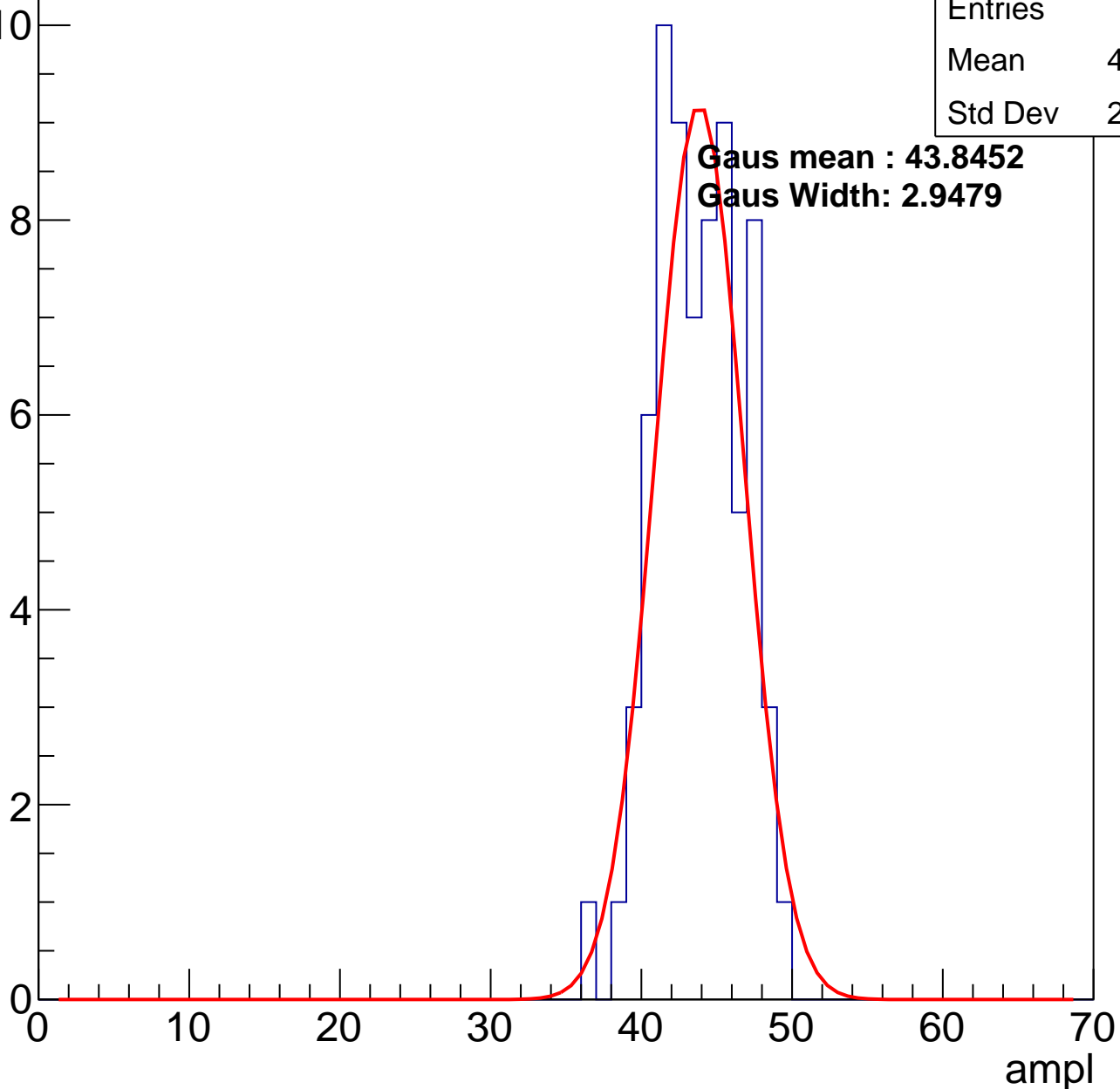
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	71
Mean	43.32
Std Dev	2.772

**Gaus mean : 43.8452**

**Gaus Width: 2.9479**

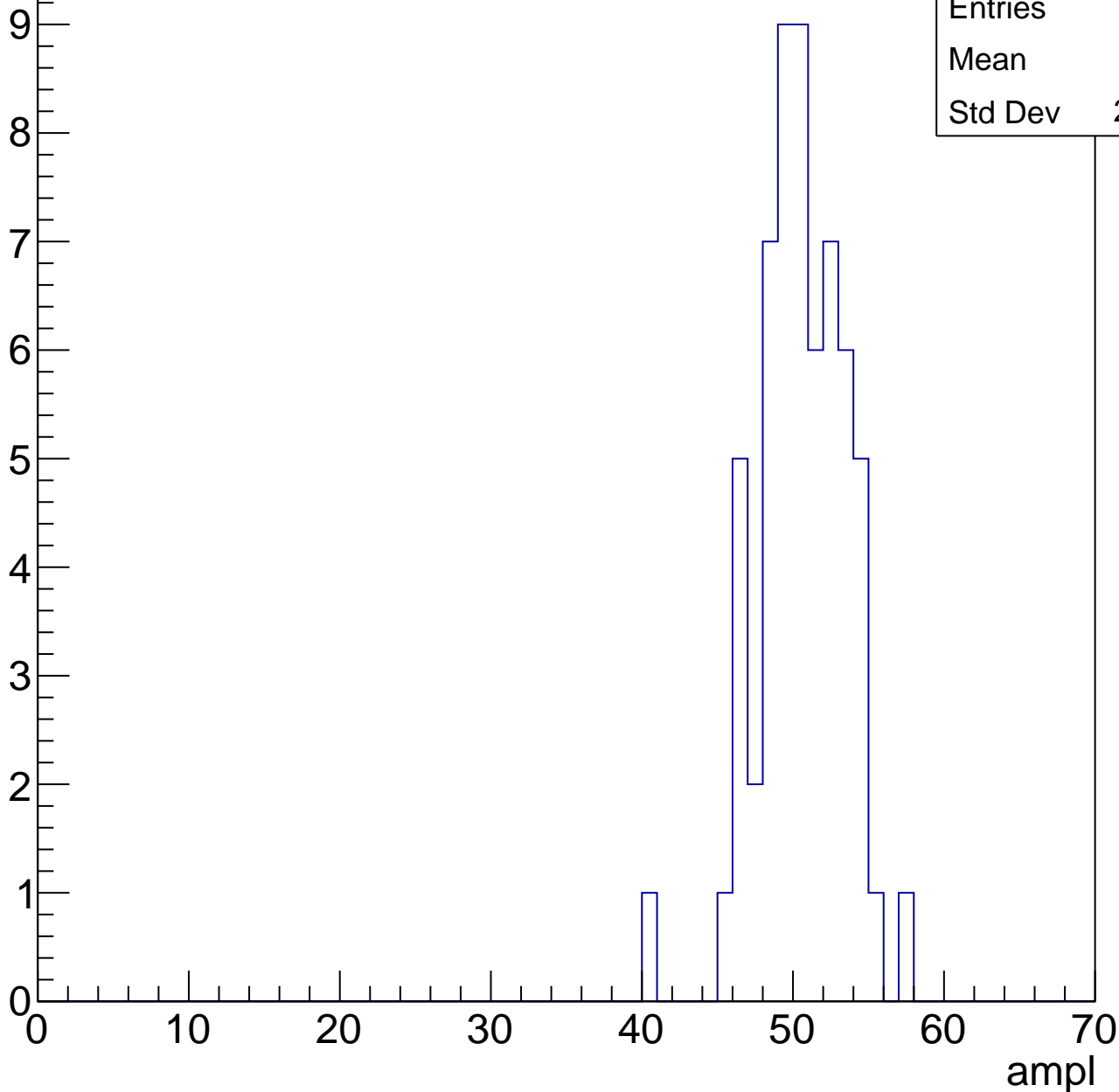


# B1L100S, U6-ch11, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

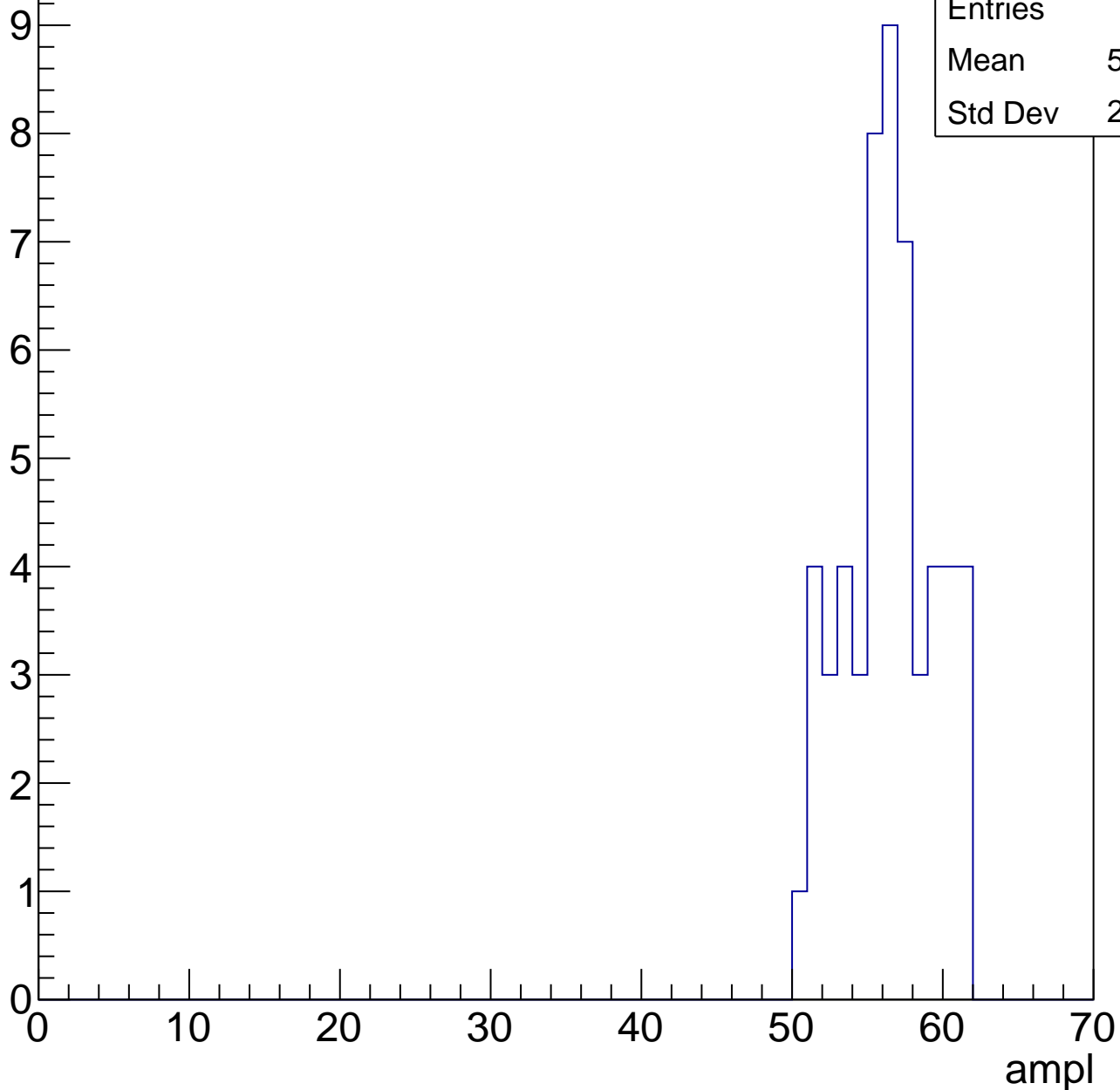
Entries	60
Mean	50.1
Std Dev	2.891



# B1L100S, U6-ch11, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

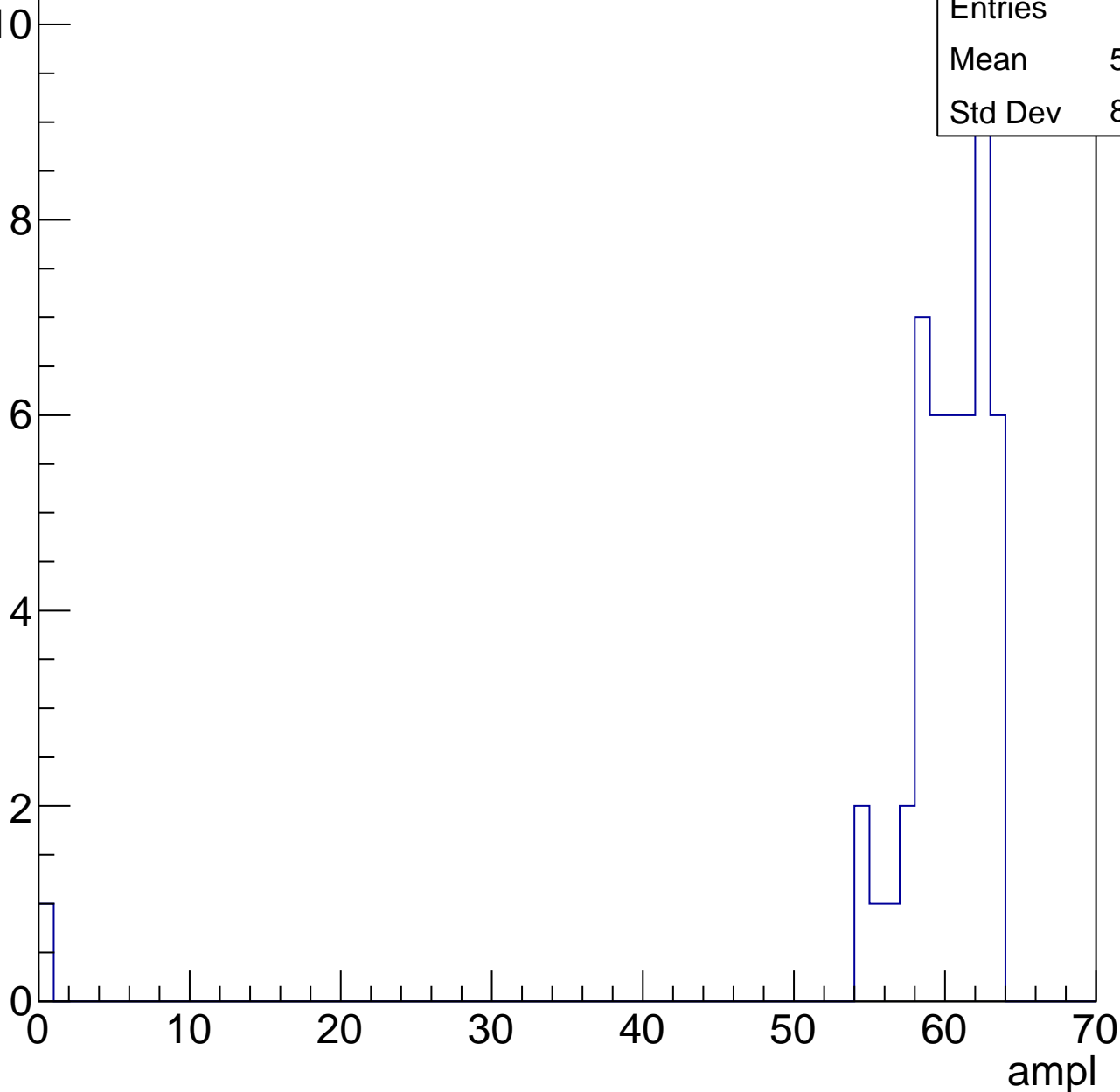


# B1L100S, U6-ch11, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

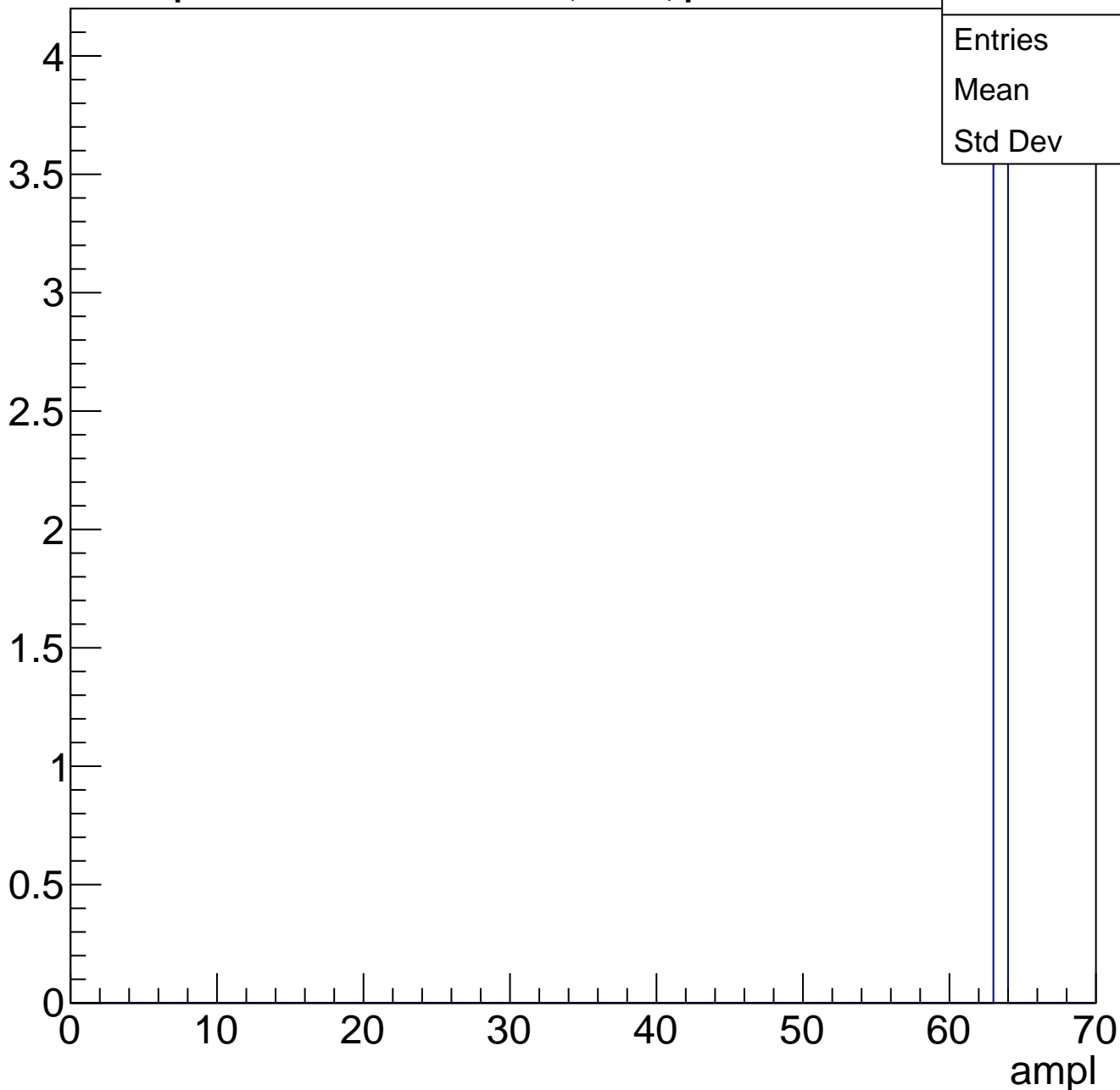
Entries	48
Mean	58.69
Std Dev	8.877



# B1L100S, U6-ch11, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry





# B1L100S, U6-ch11, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L100S, U6-ch12, adc0

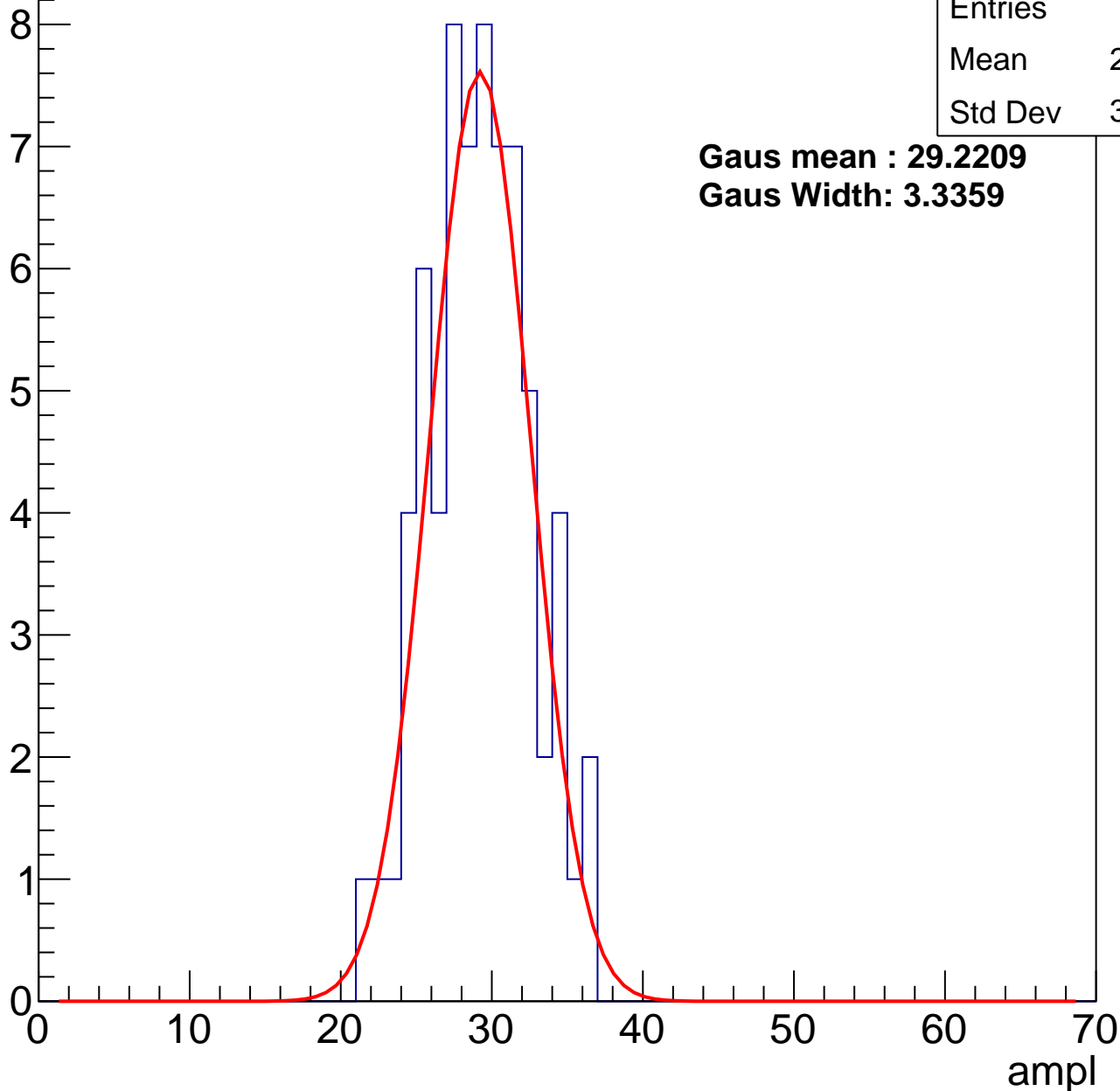
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	68
Mean	28.76
Std Dev	3.348

**Gaus mean : 29.2209**

**Gaus Width: 3.3359**



# B1L100S, U6-ch12, adc1

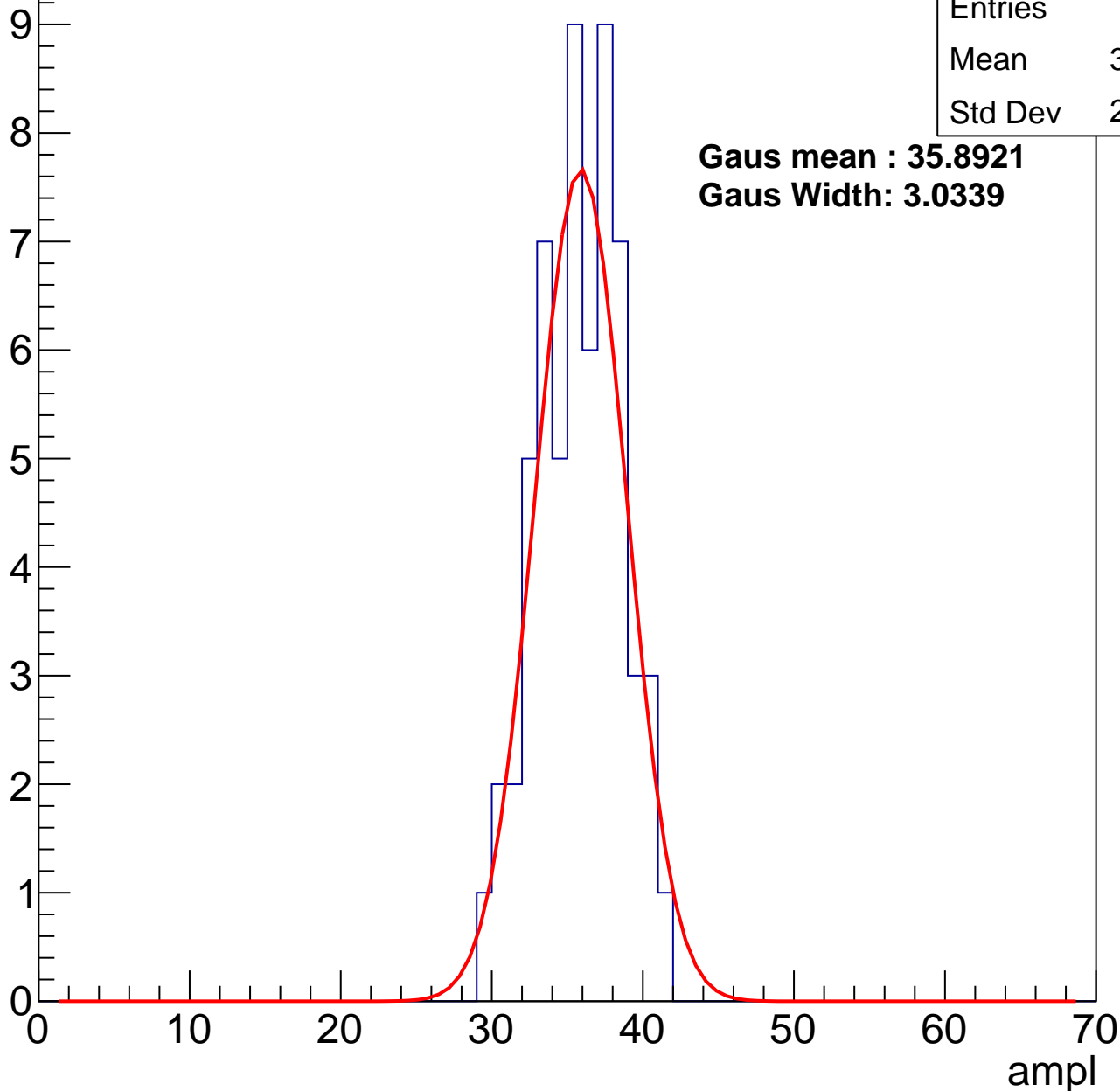
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	60
Mean	35.33
Std Dev	2.749

**Gaus mean : 35.8921**

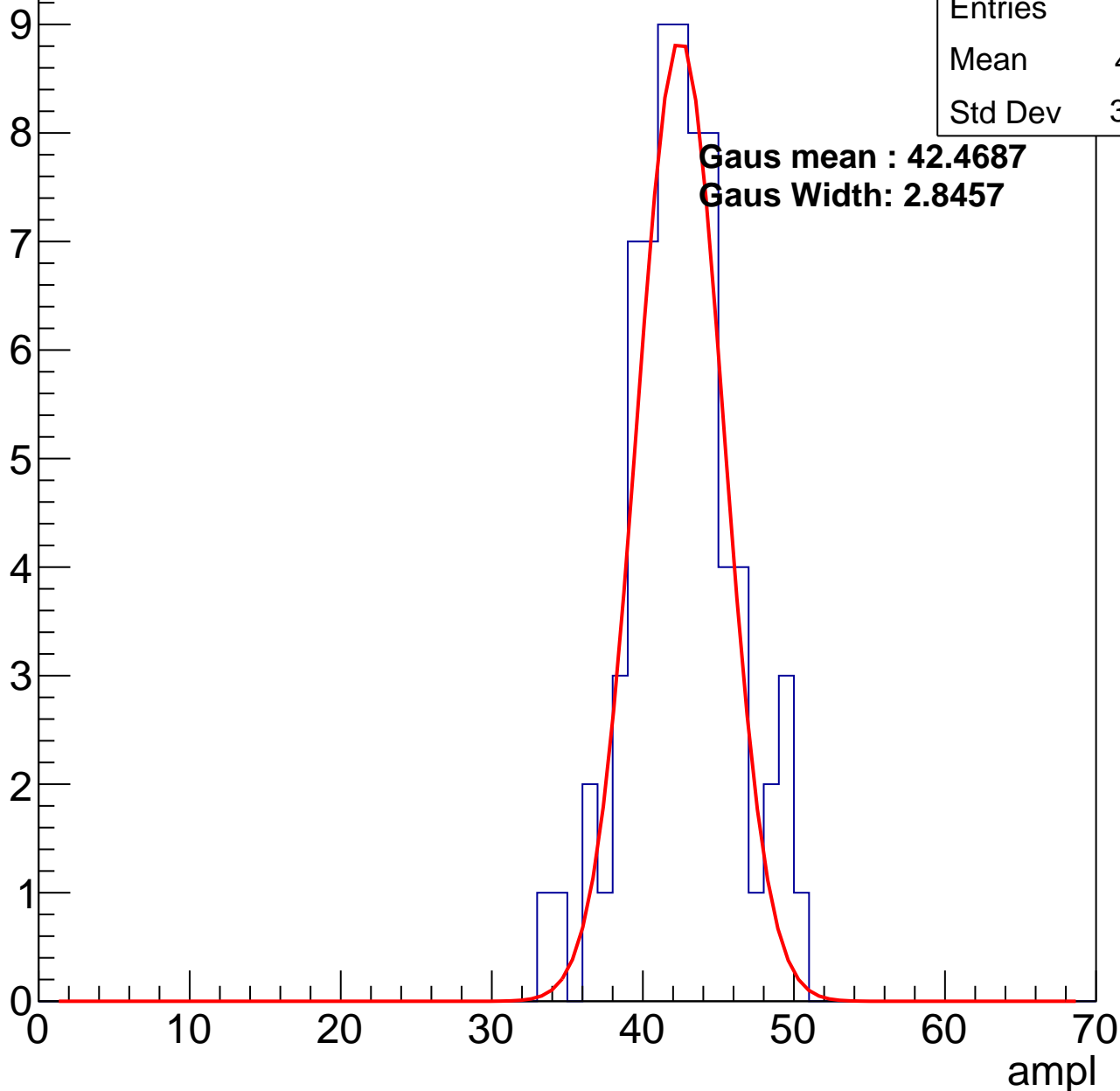
**Gaus Width: 3.0339**



# B1L100S, U6-ch12, adc2

calib\_packv5\_042523\_0143.root, FC#4, port A2

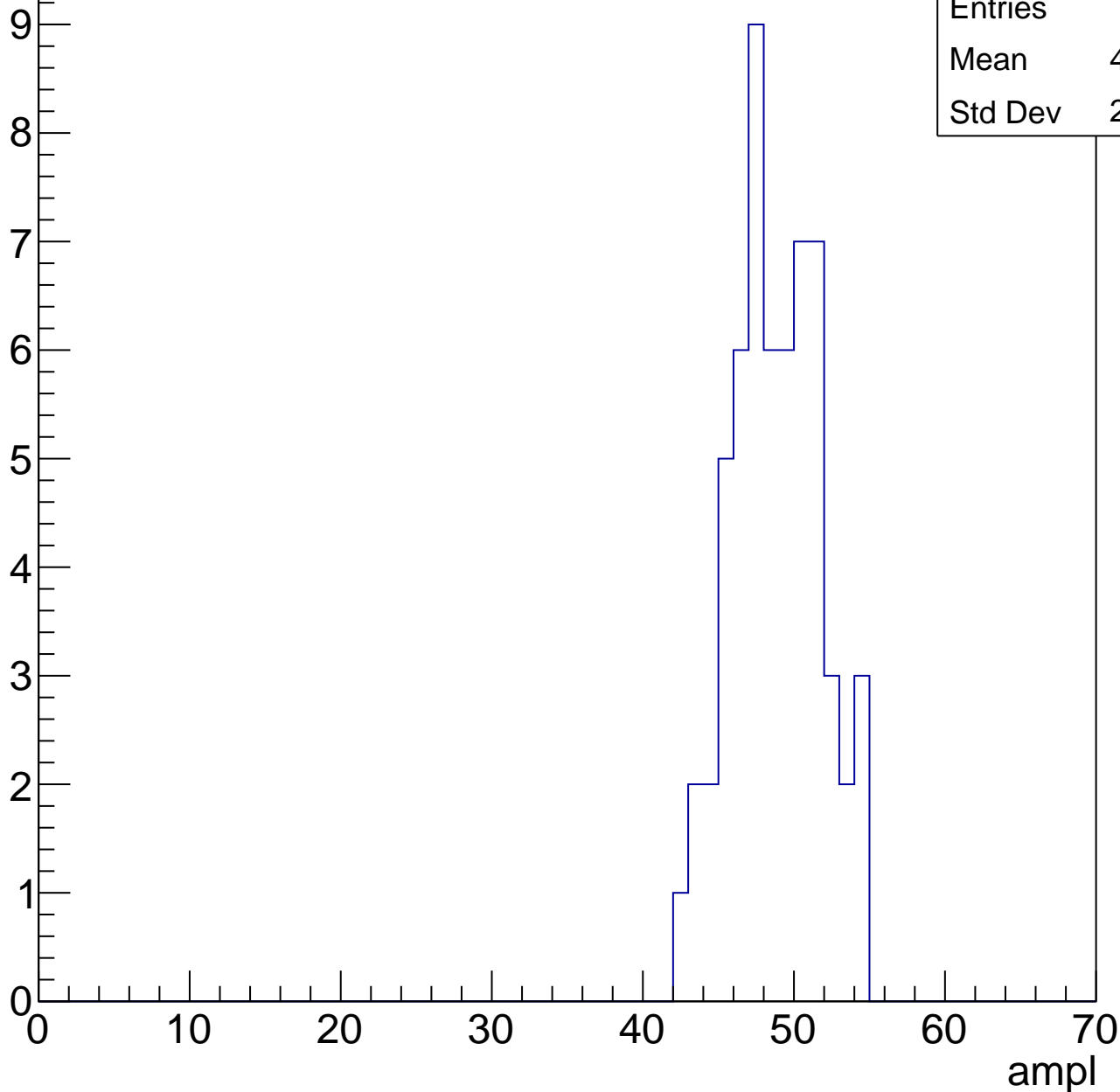
Entry



# B1L100S, U6-ch12, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



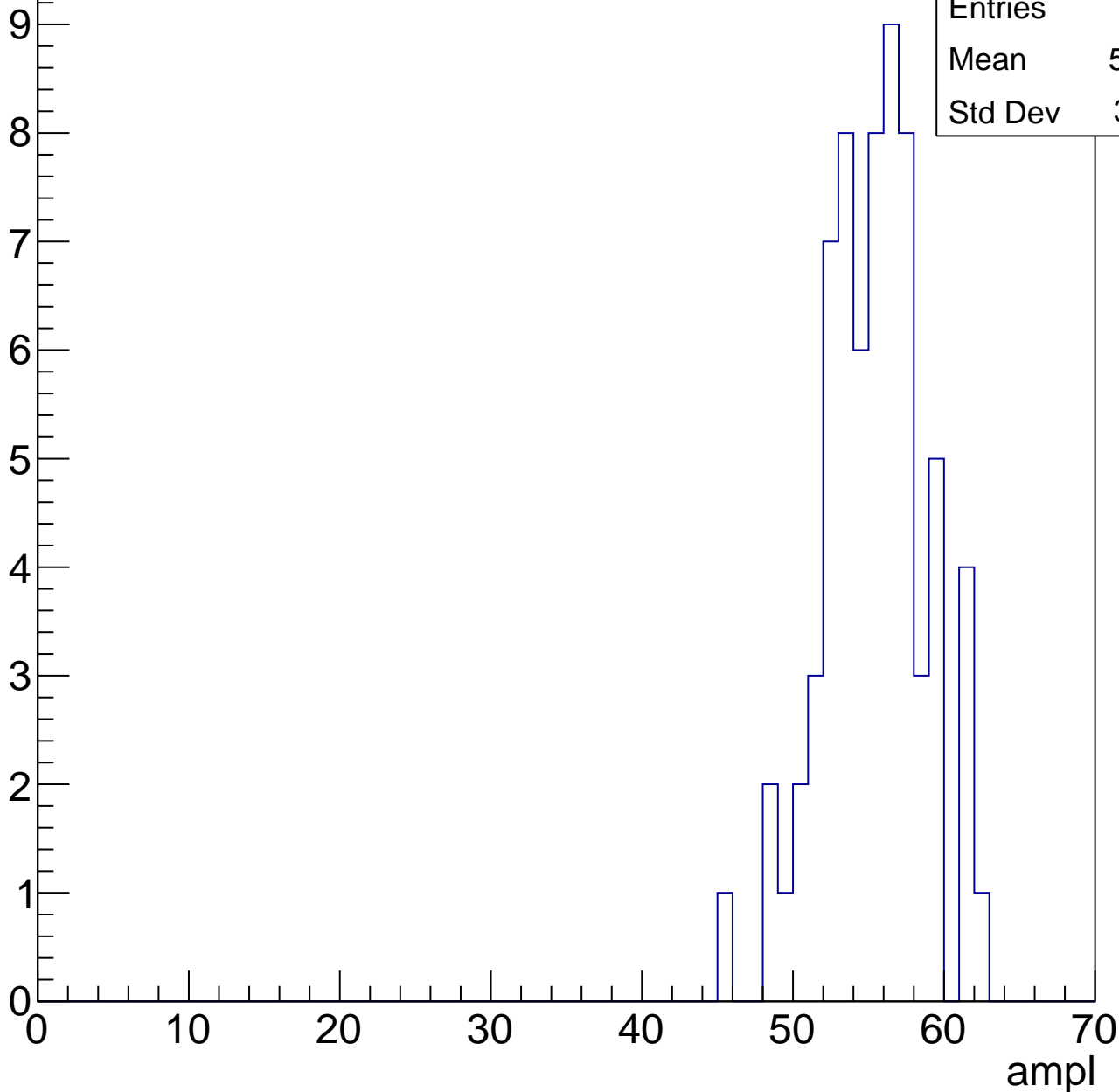
Entries	59
Mean	48.36
Std Dev	2.886

# B1L100S, U6-ch12, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	68
Mean	54.85
Std Dev	3.371



# B1L100S, U6-ch12, adc5

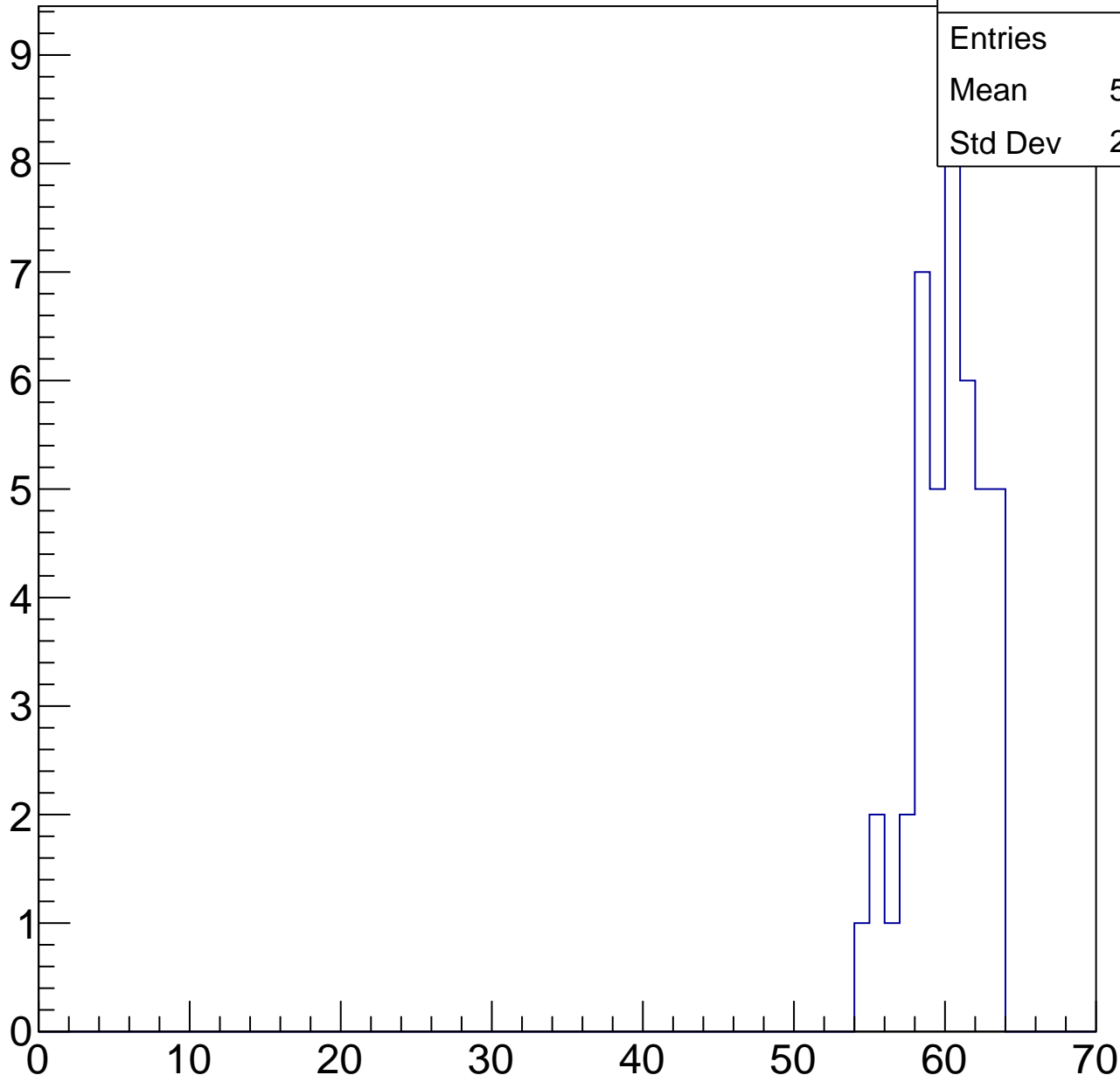
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	43
Mean	59.67
Std Dev	2.259

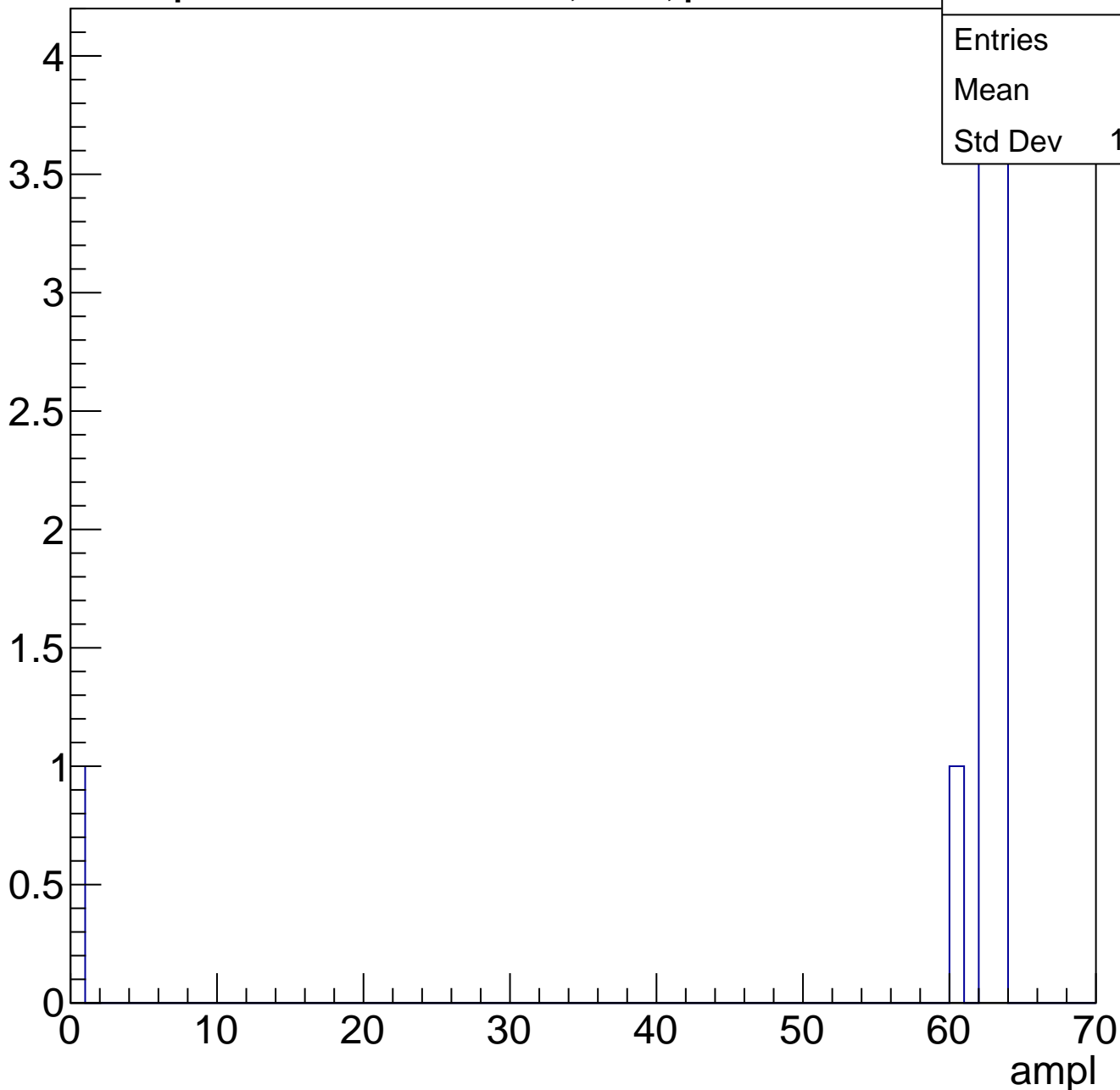
ampl



# B1L100S, U6-ch12, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

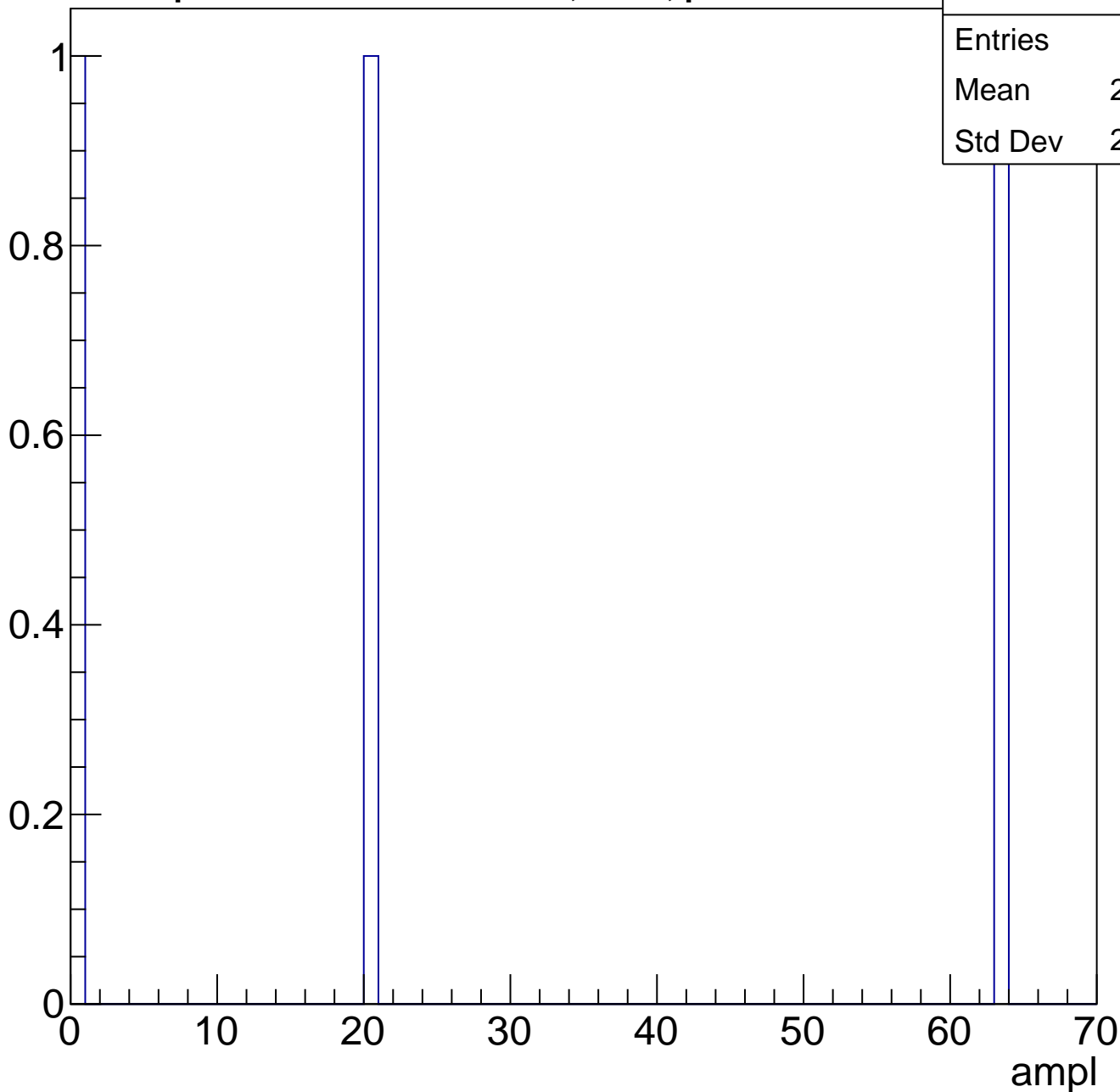




# B1L100S, U6-ch12, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	3
Mean	27.67
Std Dev	26.28

# B1L100S, U6-ch13, adc0

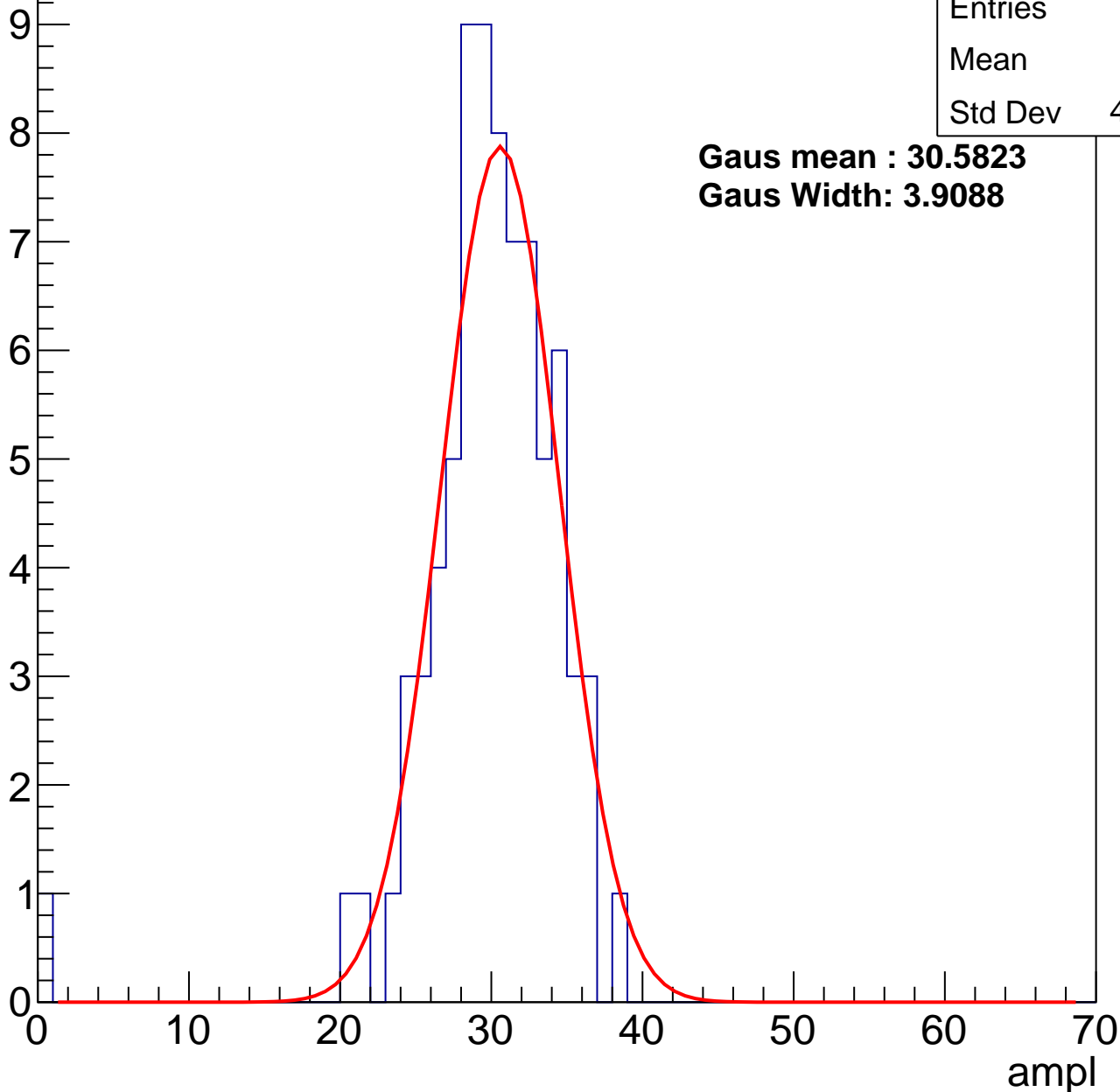
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	77
Mean	29.4
Std Dev	4.918

**Gaus mean : 30.5823**

**Gaus Width: 3.9088**



# B1L100S, U6-ch13, adc1

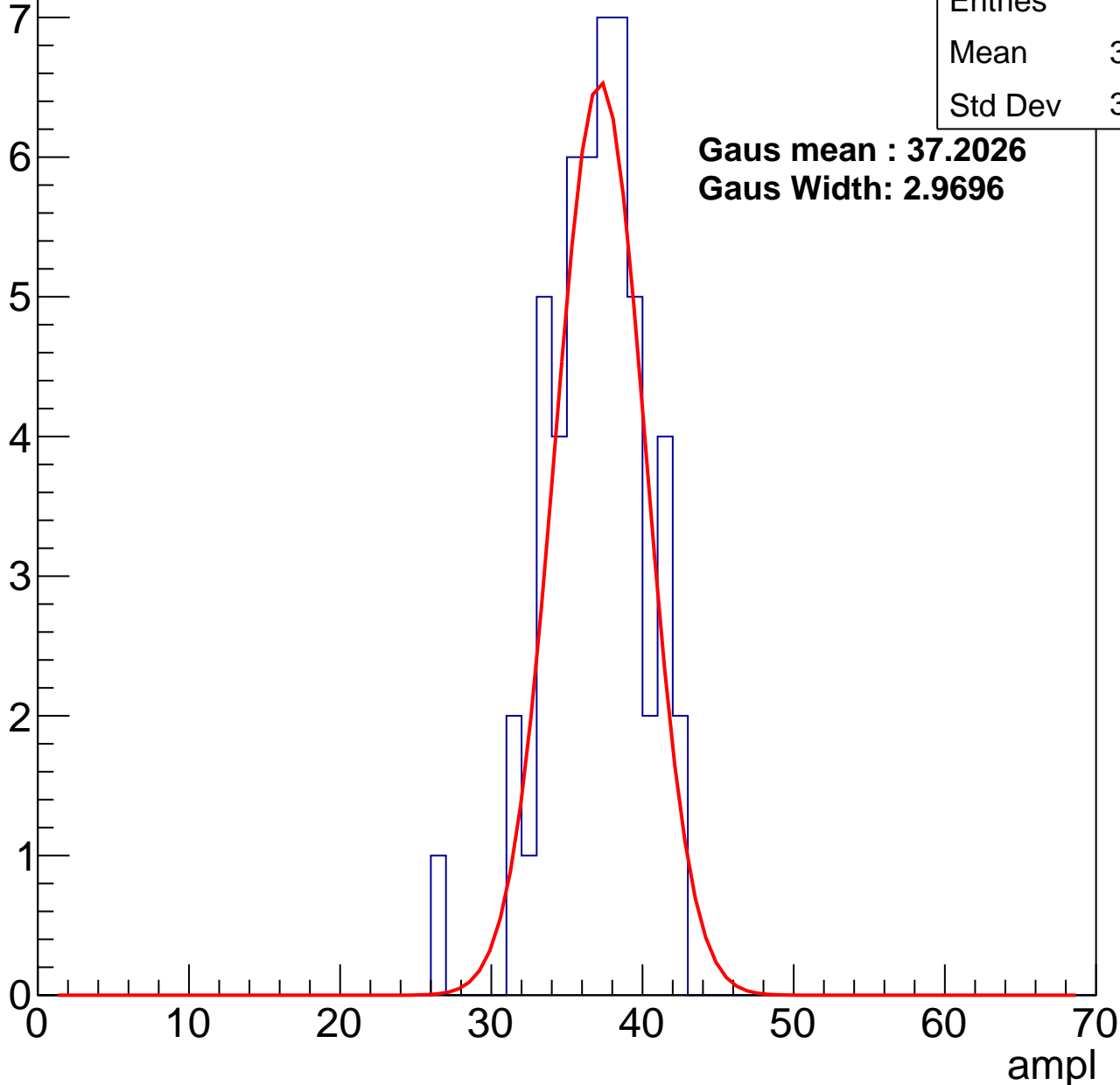
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	52
Mean	36.44
Std Dev	3.122

**Gaus mean : 37.2026**

**Gaus Width: 2.9696**



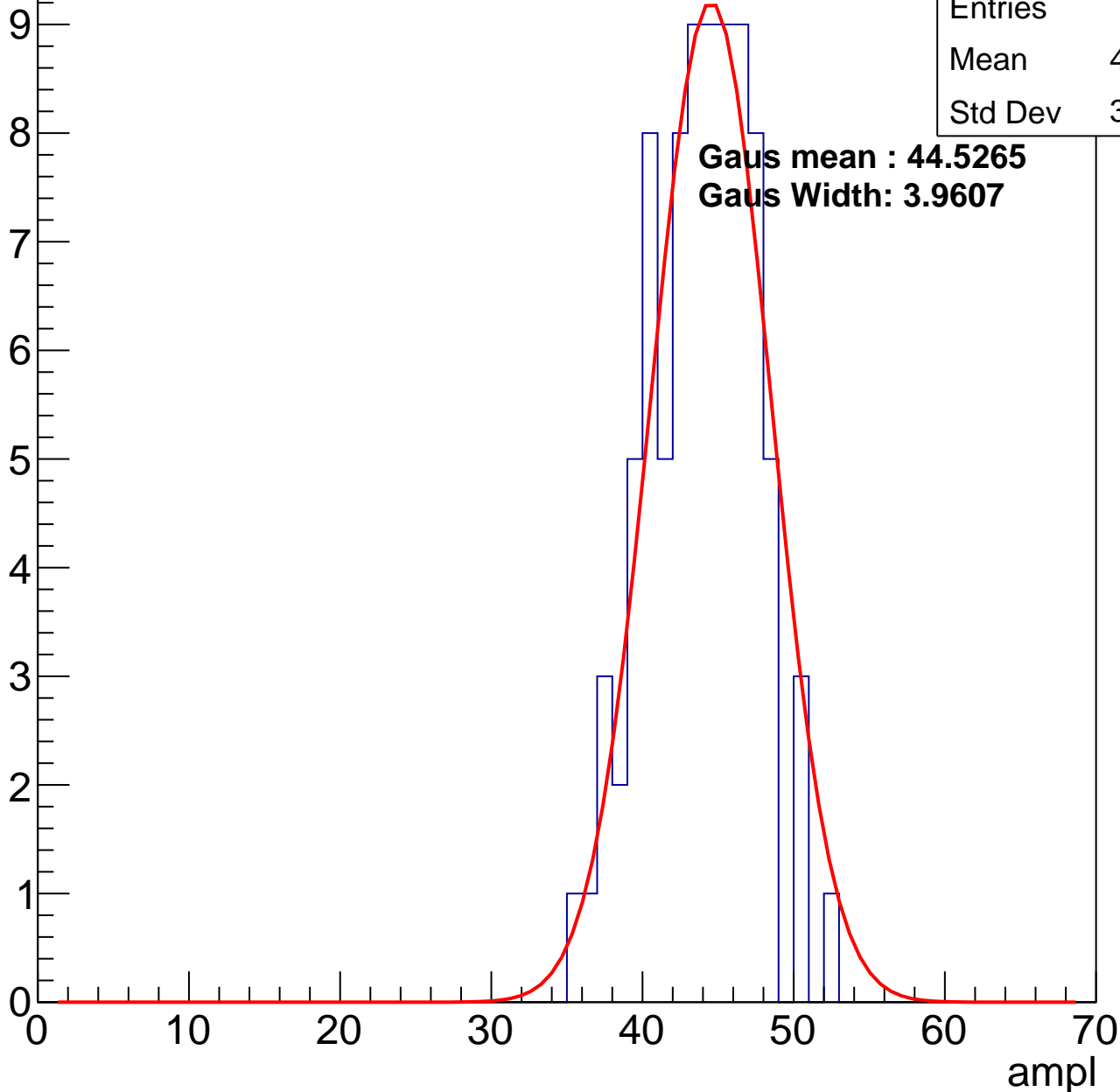
# B1L100S, U6-ch13, adc2

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	86
Mean	43.42
Std Dev	3.482

**Gaus mean : 44.5265**  
**Gaus Width: 3.9607**

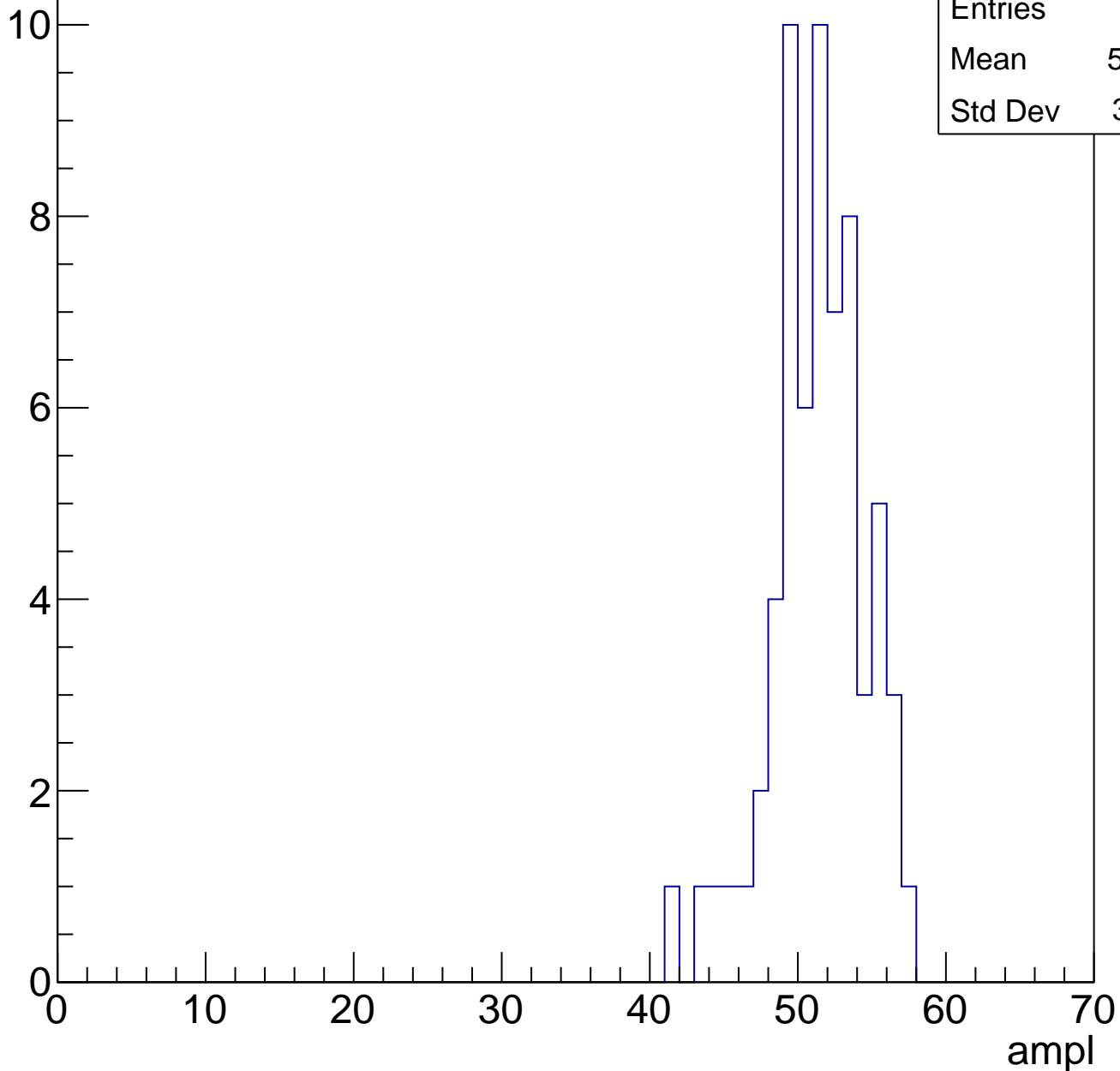


# B1L100S, U6-ch13, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	64
Mean	50.86
Std Dev	3.171

Entry

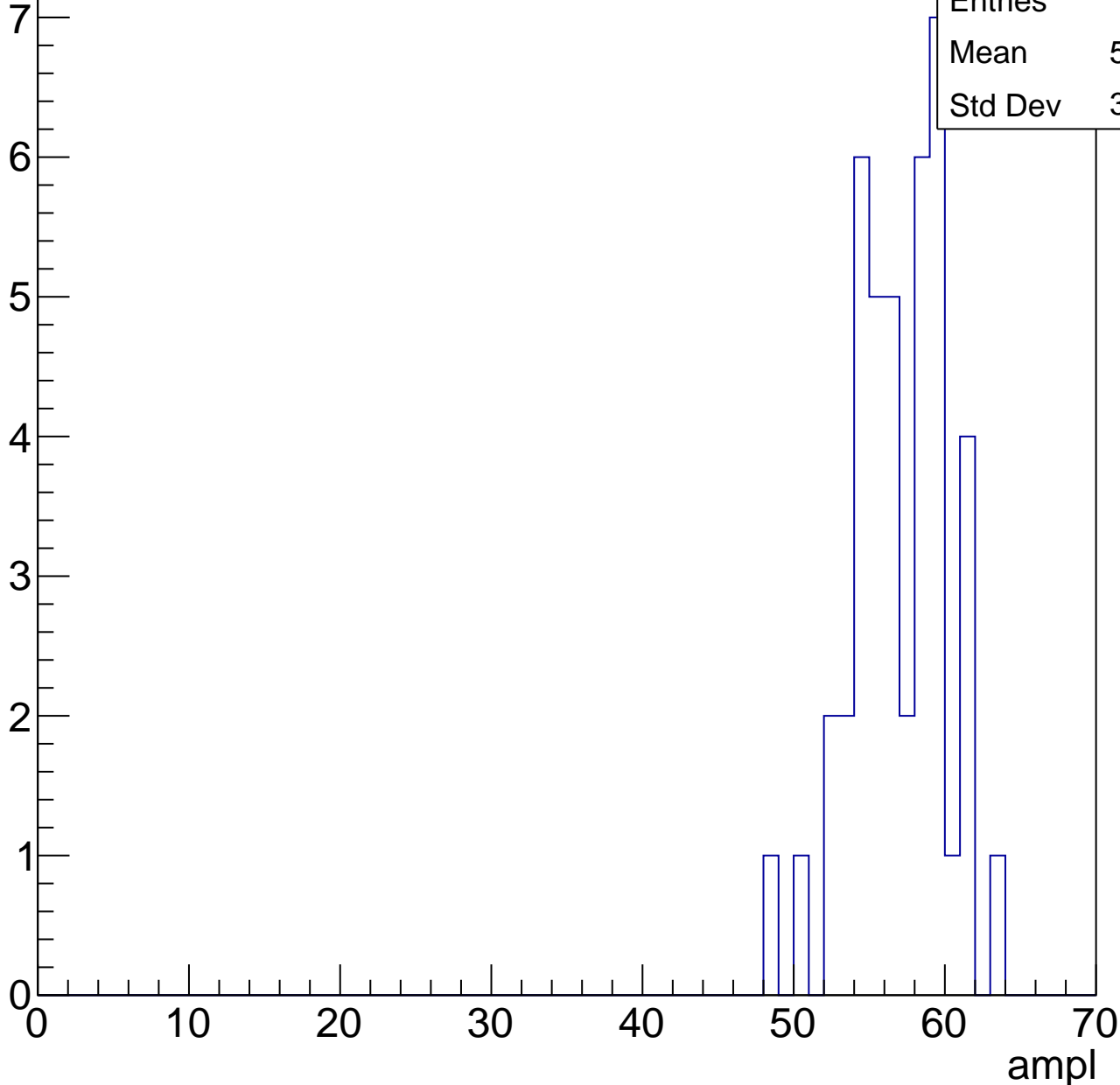


# B1L100S, U6-ch13, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	43
Mean	56.49
Std Dev	3.135



# B1L100S, U6-ch13, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	48
Mean	58.67
Std Dev	8.851

ampl

0 10 20 30 40 50 60 70

0

1

2

3

4

5

6

7

8

9

# B1L100S, U6-ch13, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry





# B1L100S, U6-ch13, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L100S, U6-ch14, adc0

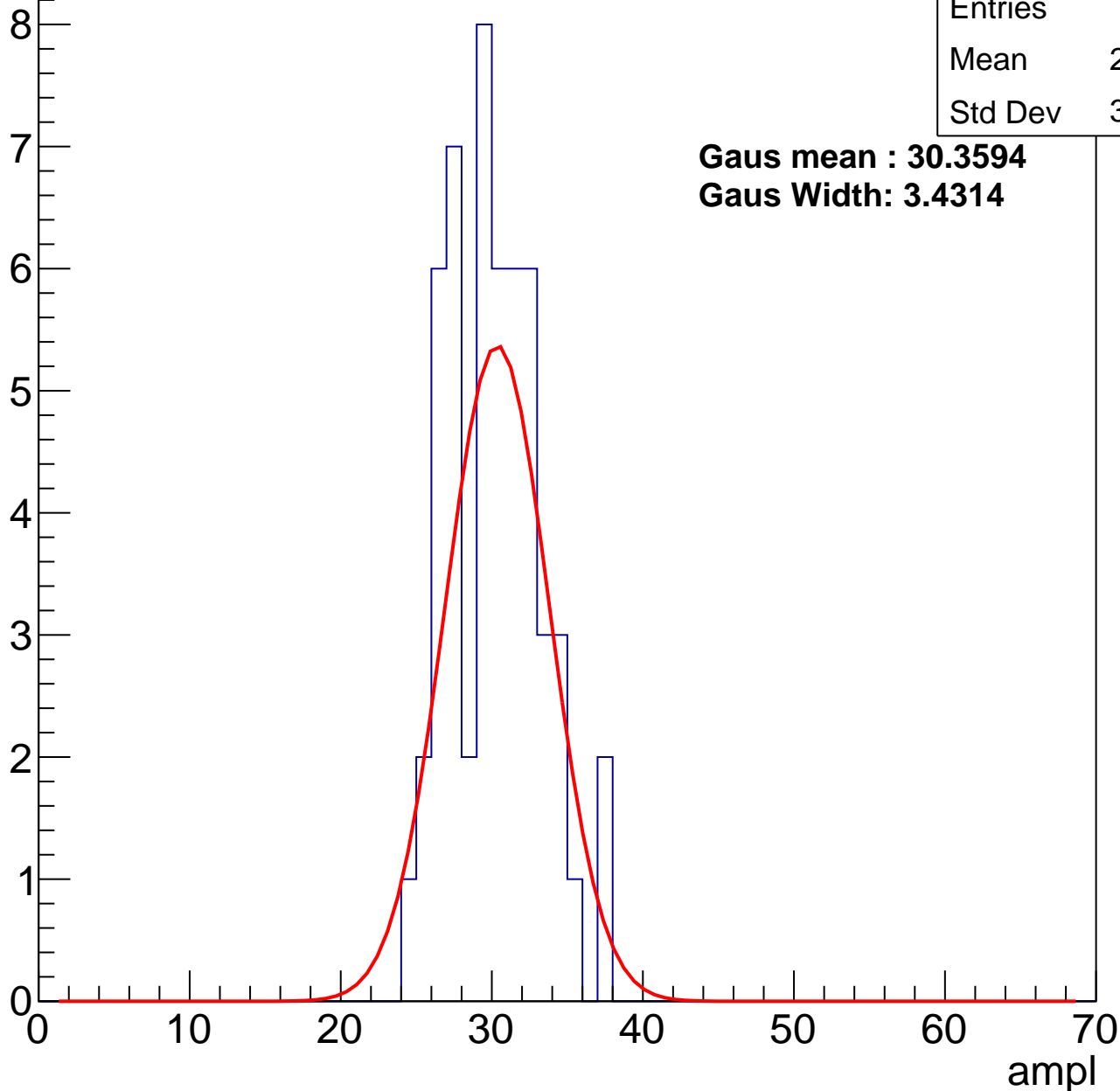
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	53
Mean	29.72
Std Dev	3.024

**Gaus mean : 30.3594**

**Gaus Width: 3.4314**



# B1L100S, U6-ch14, adc1

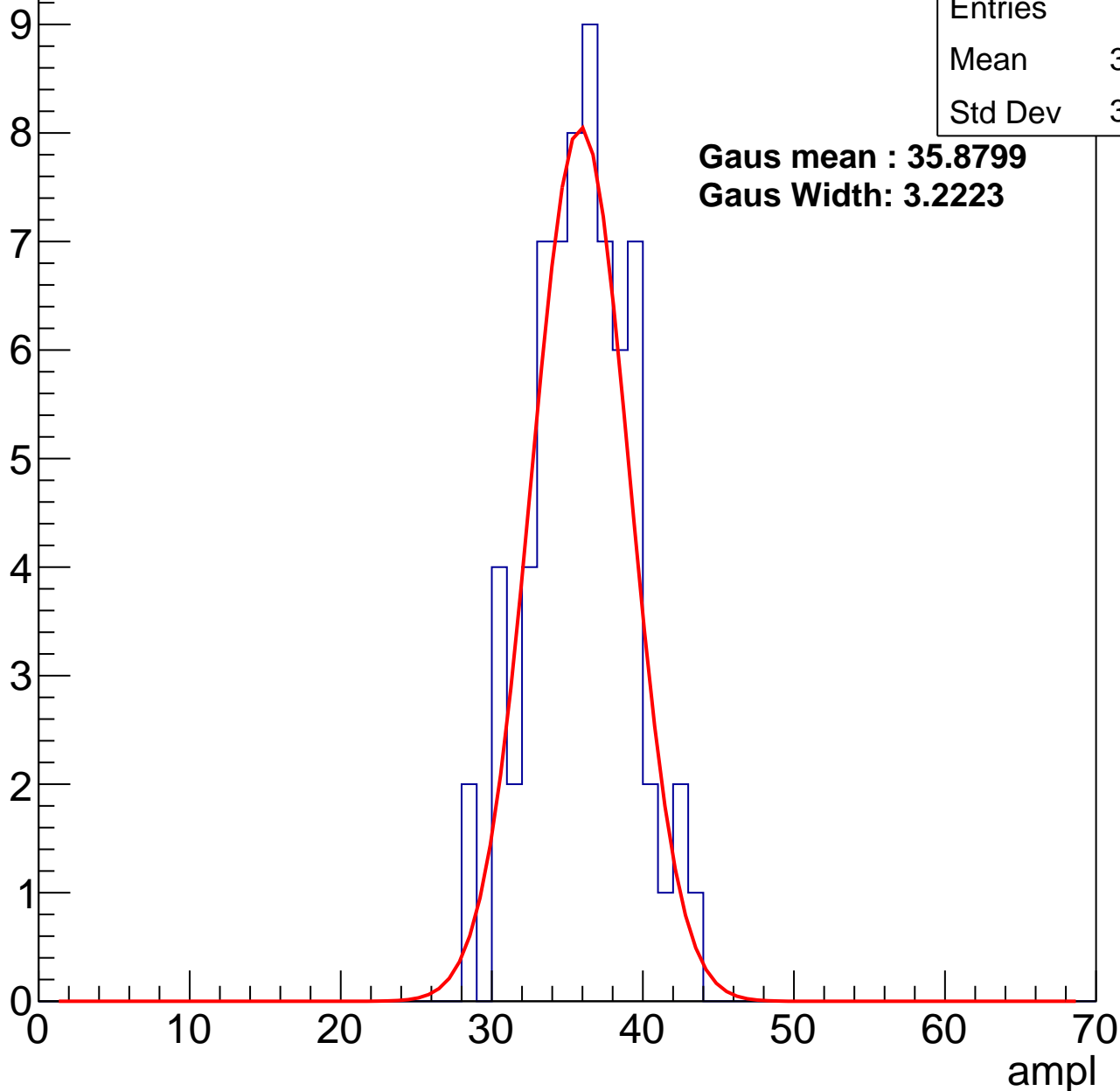
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	69
Mean	35.46
Std Dev	3.269

**Gaus mean : 35.8799**

**Gaus Width: 3.2223**



# B1L100S, U6-ch14, adc2

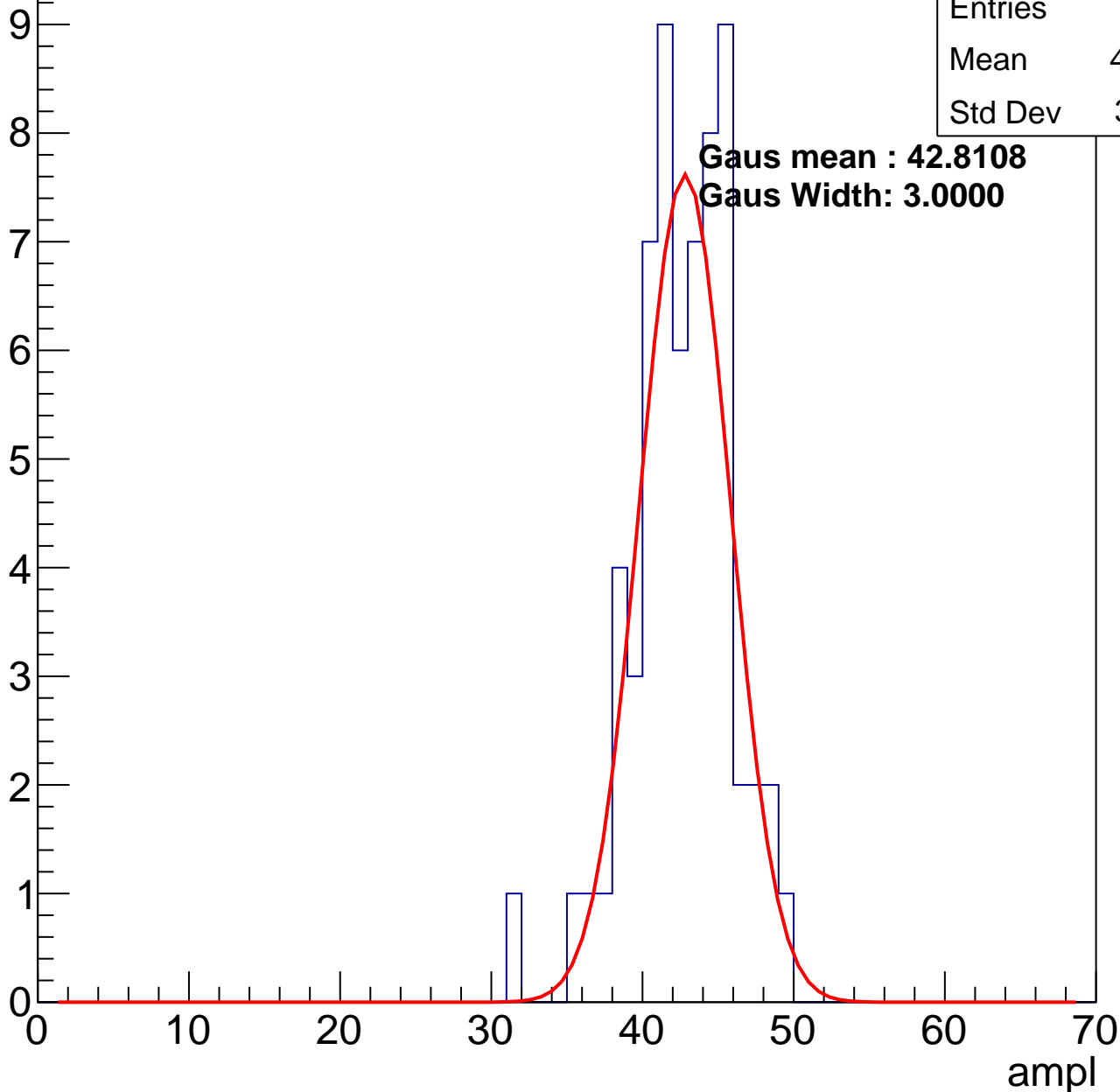
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	64
Mean	42.16
Std Dev	3.261

**Gaus mean : 42.8108**

**Gaus Width: 3.0000**

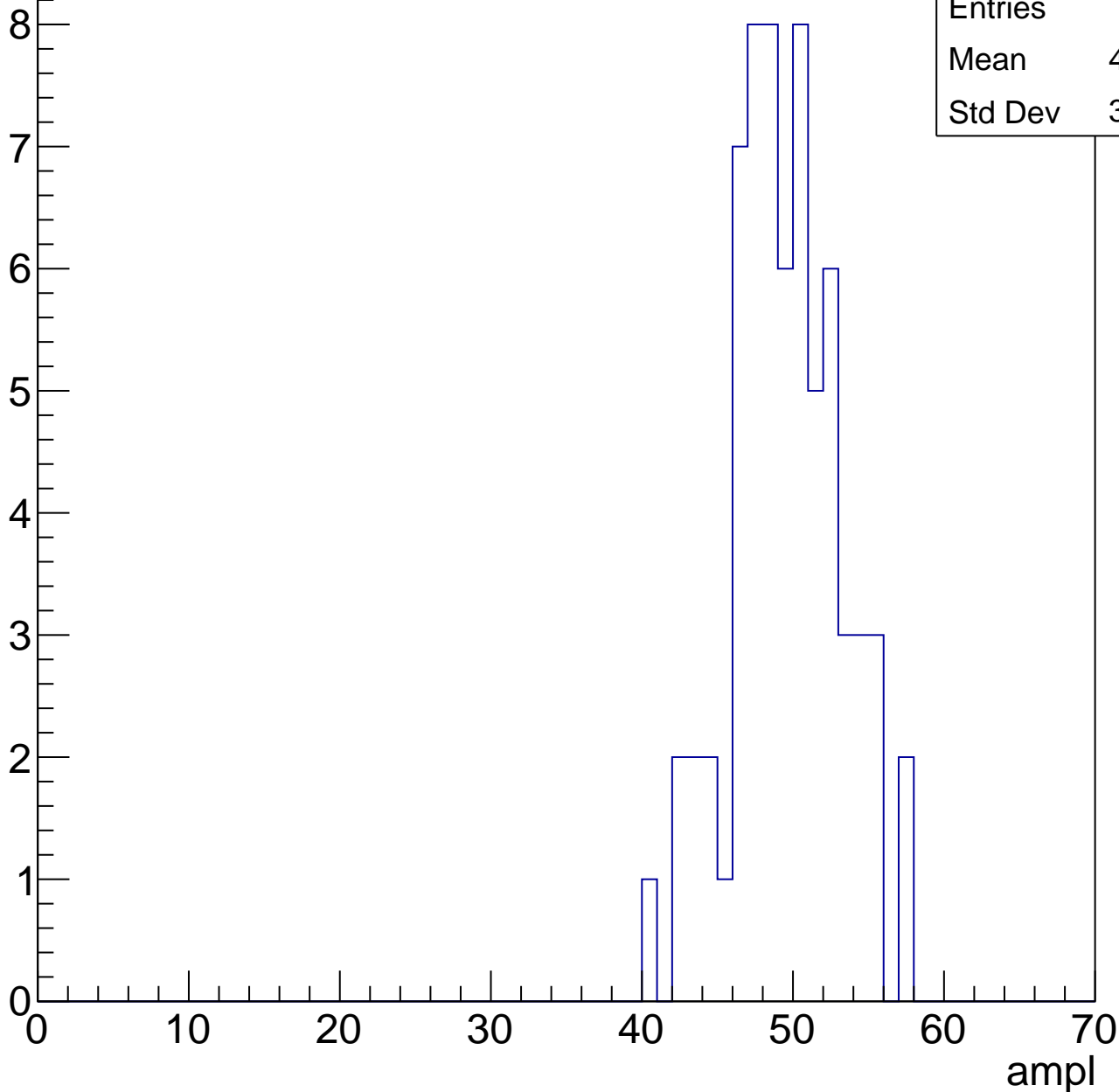


# B1L100S, U6-ch14, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

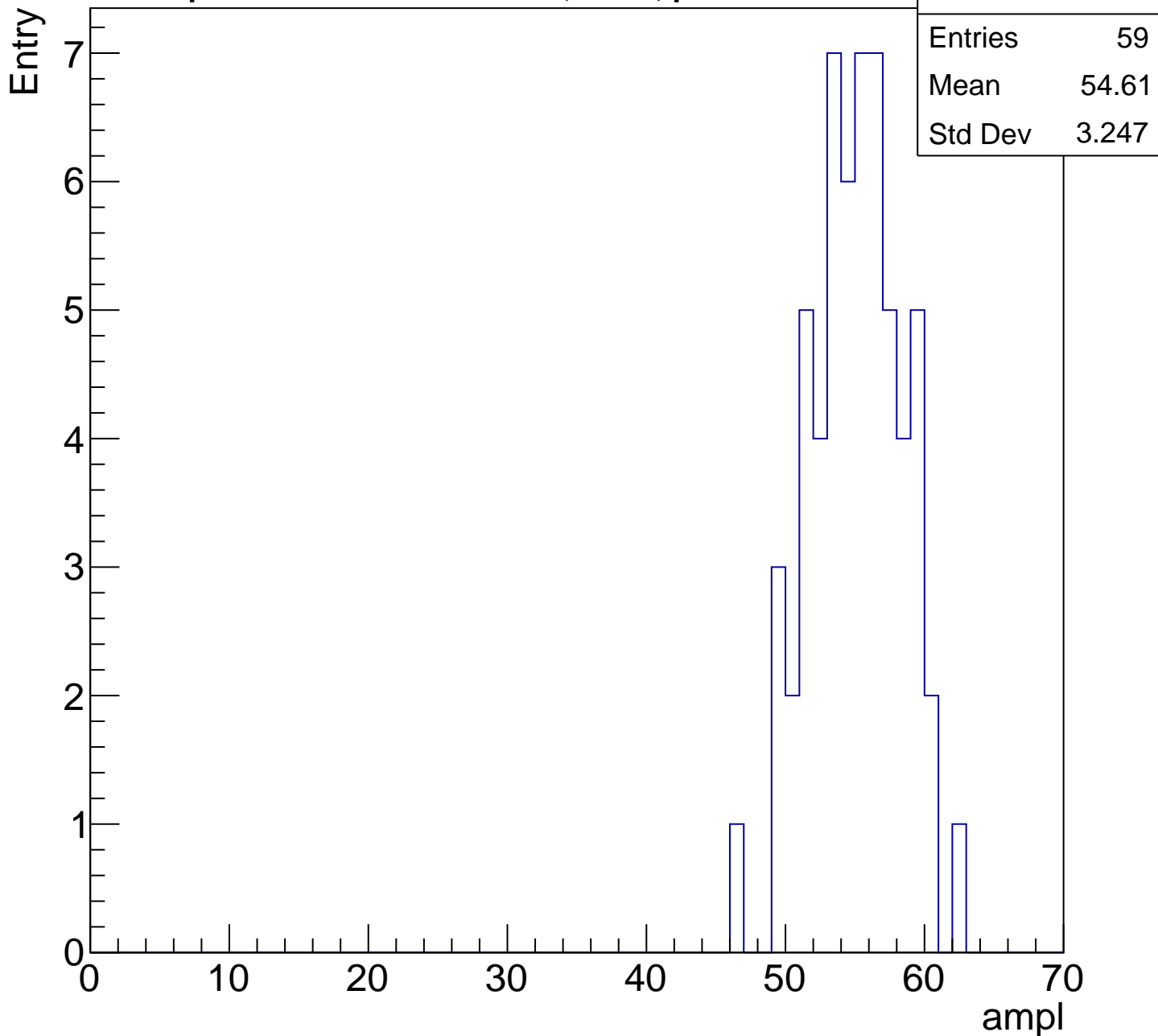
Entry

Entries	67
Mean	49.04
Std Dev	3.585



# B1L100S, U6-ch14, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

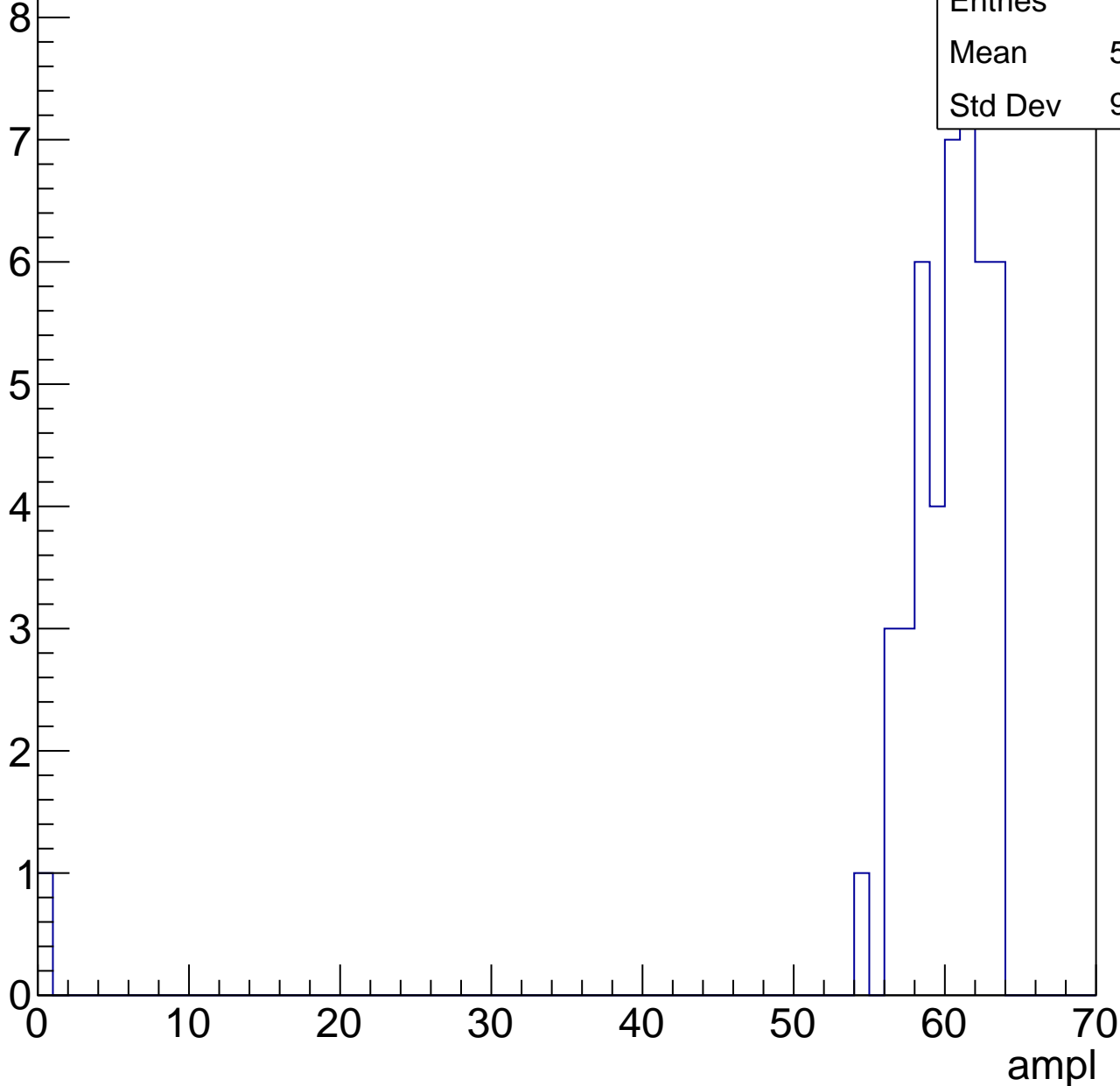


# B1L100S, U6-ch14, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

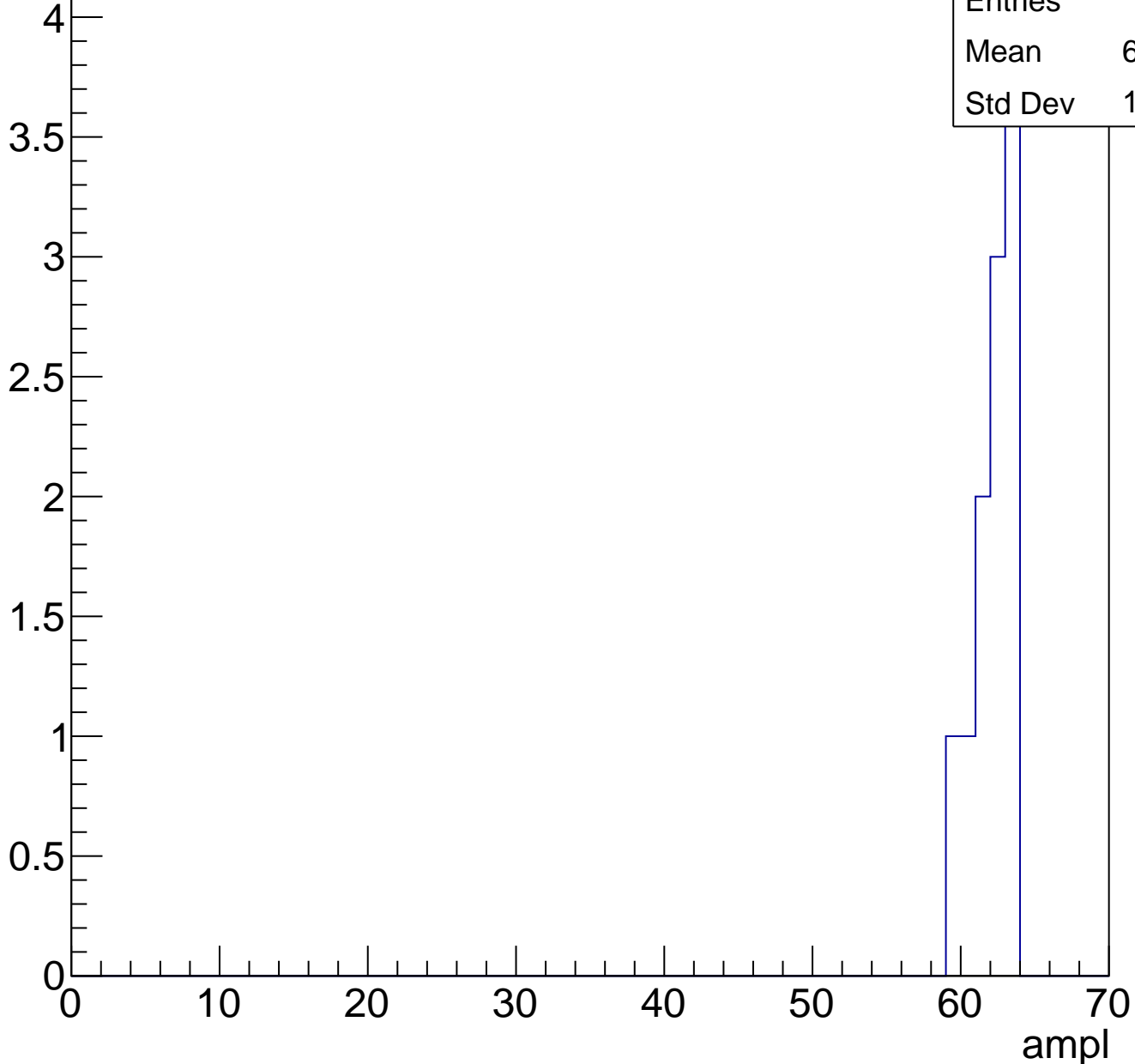
Entries	45
Mean	58.56
Std Dev	9.106



# B1L100S, U6-ch14, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry





# B1L100S, U6-ch14, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	2
Mean	11
Std Dev	11

# B1L100S, U6-ch15, adc0

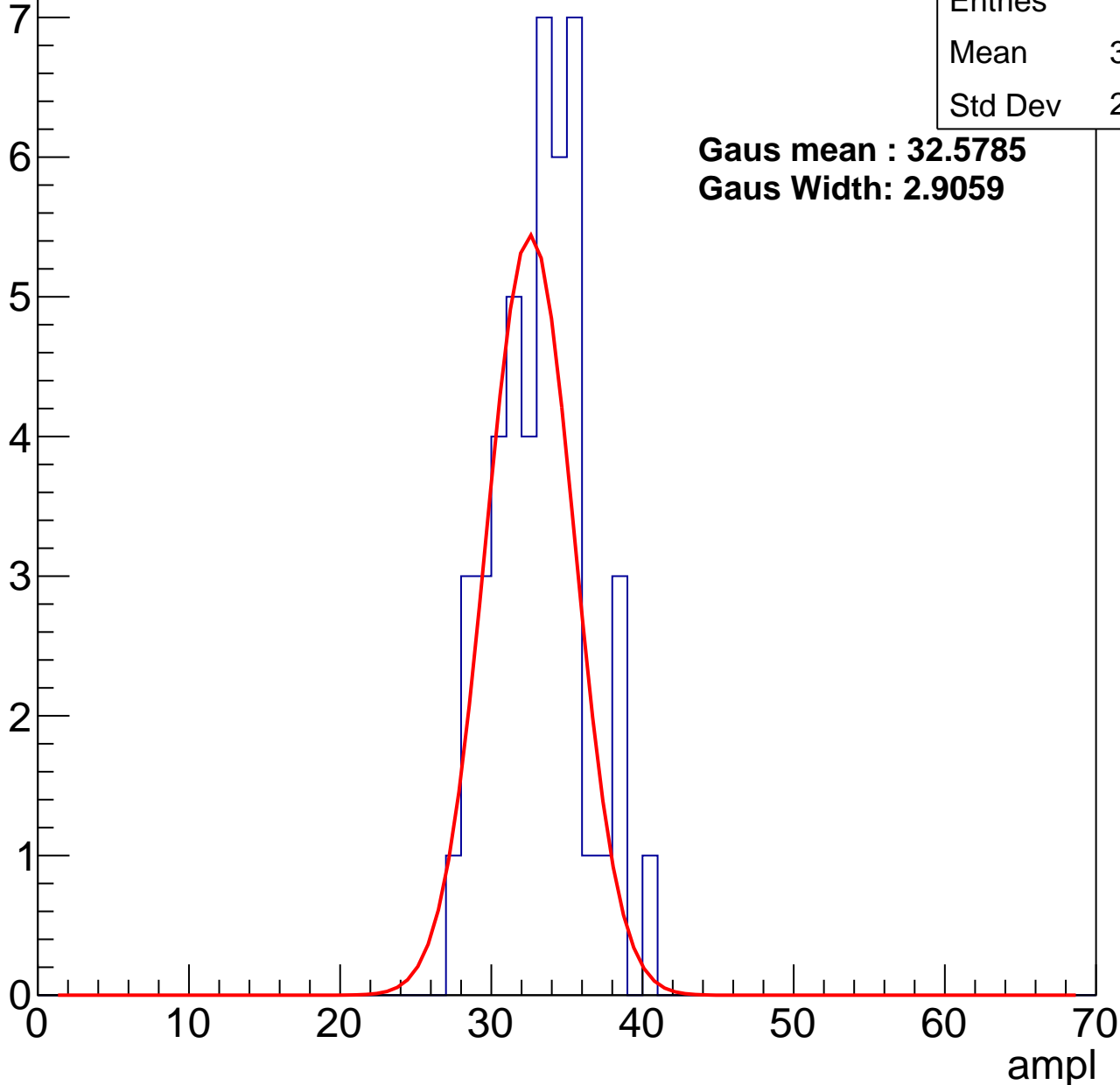
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	46
Mean	32.78
Std Dev	2.948

**Gaus mean : 32.5785**

**Gaus Width: 2.9059**



# B1L100S, U6-ch15, adc1

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	74
Mean	38.32
Std Dev	3.526

**Gaus mean : 38.9779**

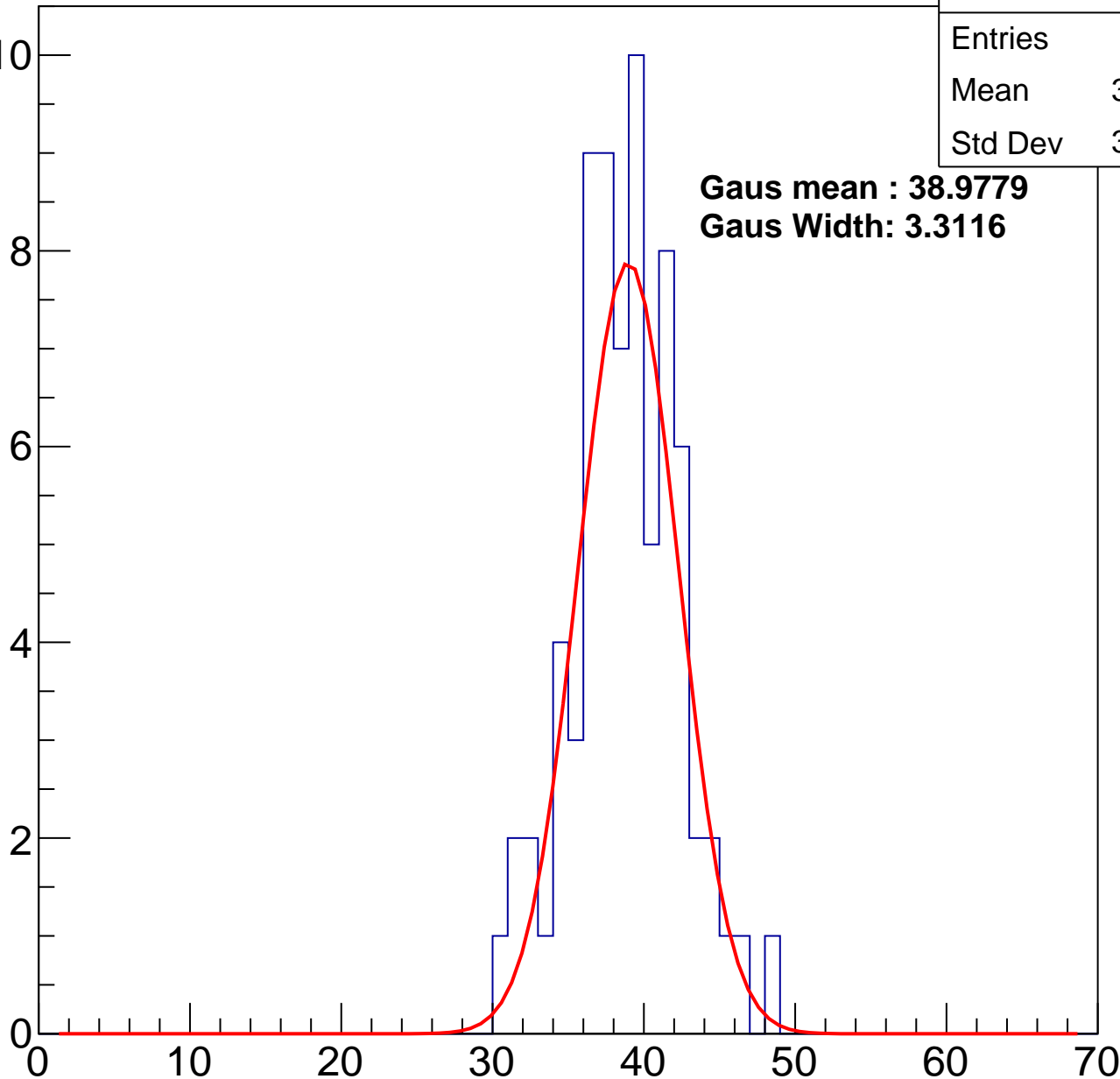
**Gaus Width: 3.3116**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B1L100S, U6-ch15, adc2

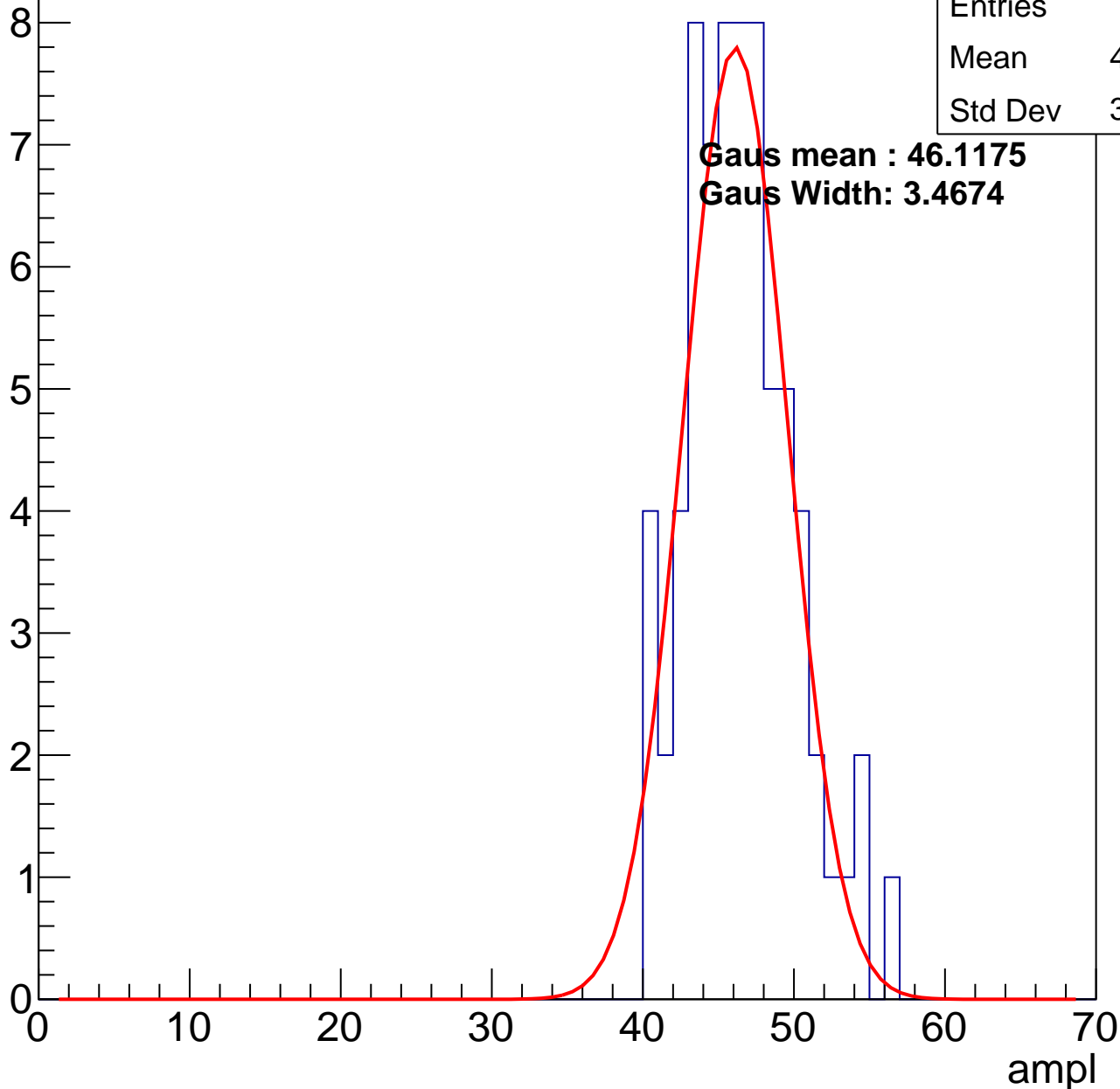
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	70
Mean	46.03
Std Dev	3.517

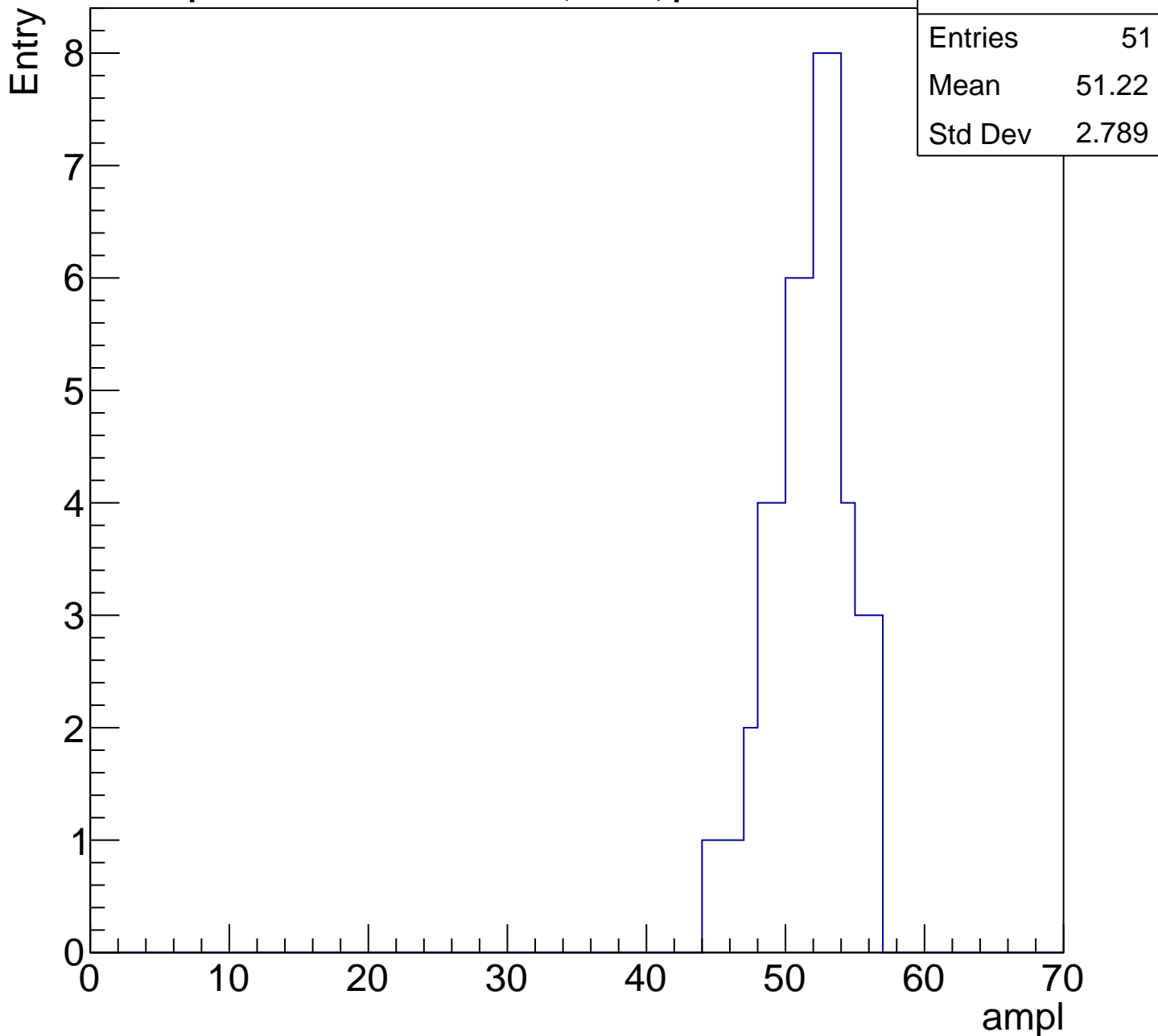
**Gaus mean : 46.1175**

**Gaus Width: 3.4674**



# B1L100S, U6-ch15, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2



# B1L100S, U6-ch15, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	56
Mean	57.62
Std Dev	3.103

Entry

10

8

6

4

2

0

0

10

20

30

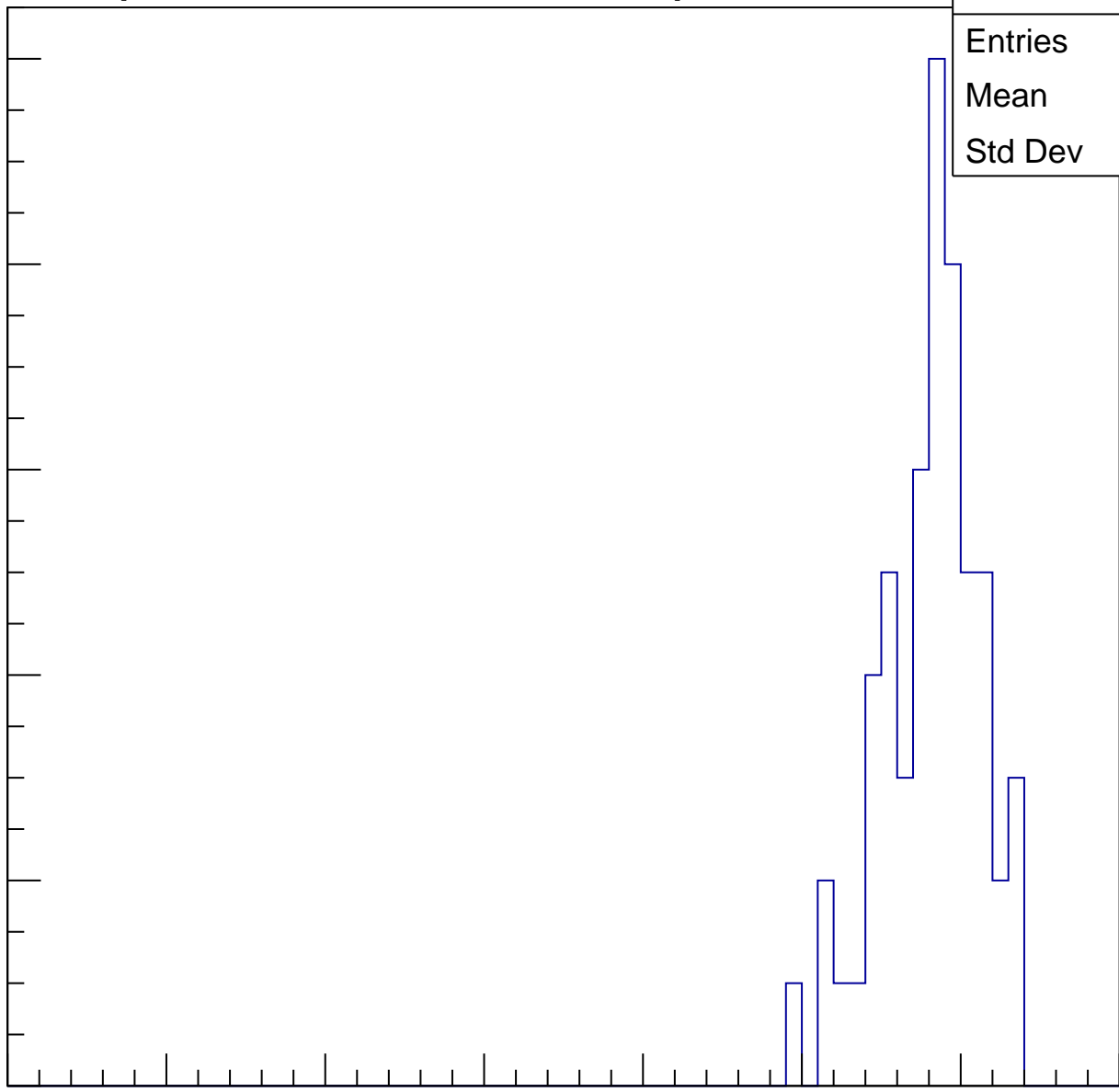
40

50

60

70

ampl

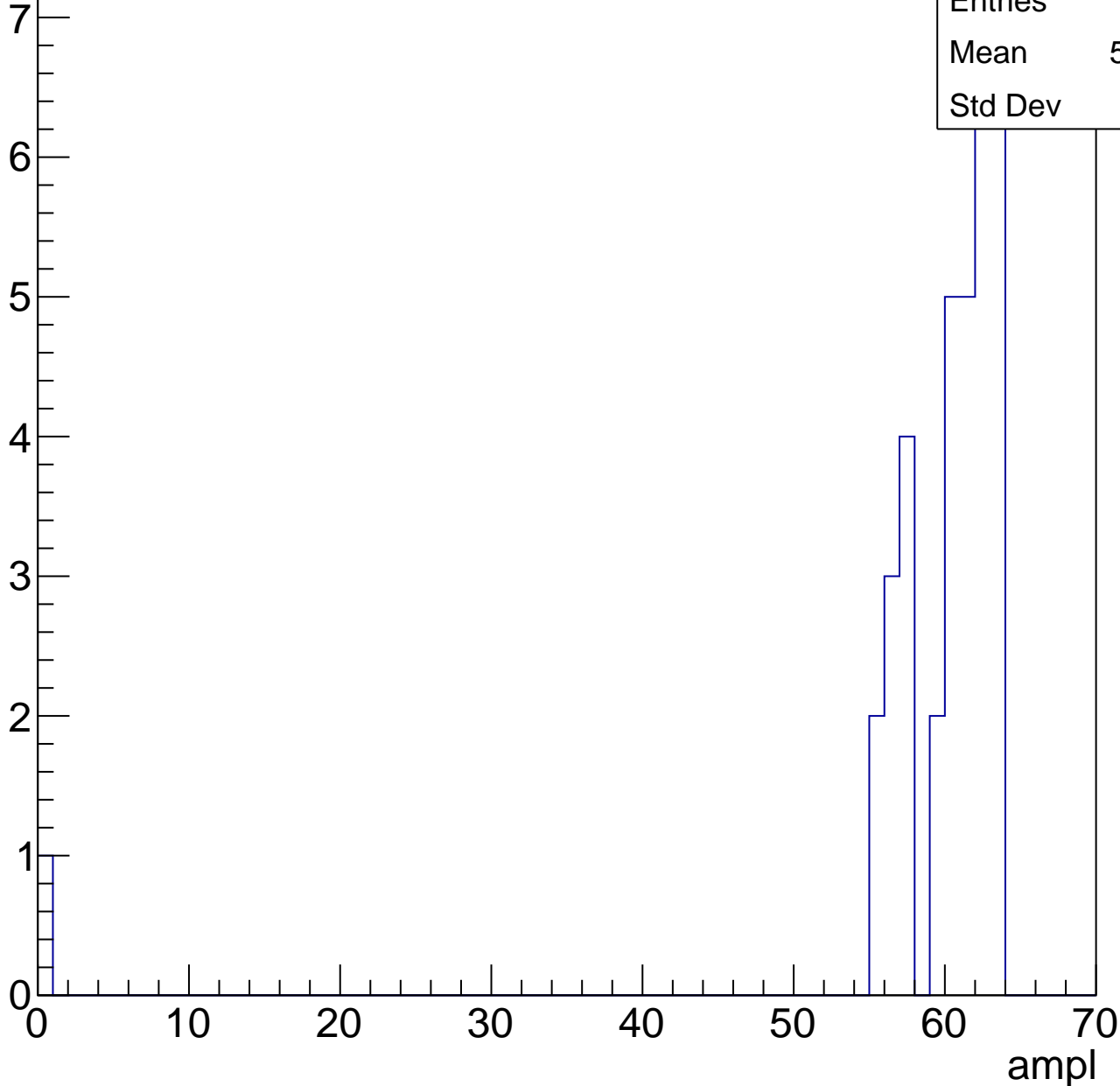


# B1L100S, U6-ch15, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	36
Mean	58.44
Std Dev	10.2



# B1L100S, U6-ch15, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry





# B1L100S, U6-ch15, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L100S, U6-ch16, adc0

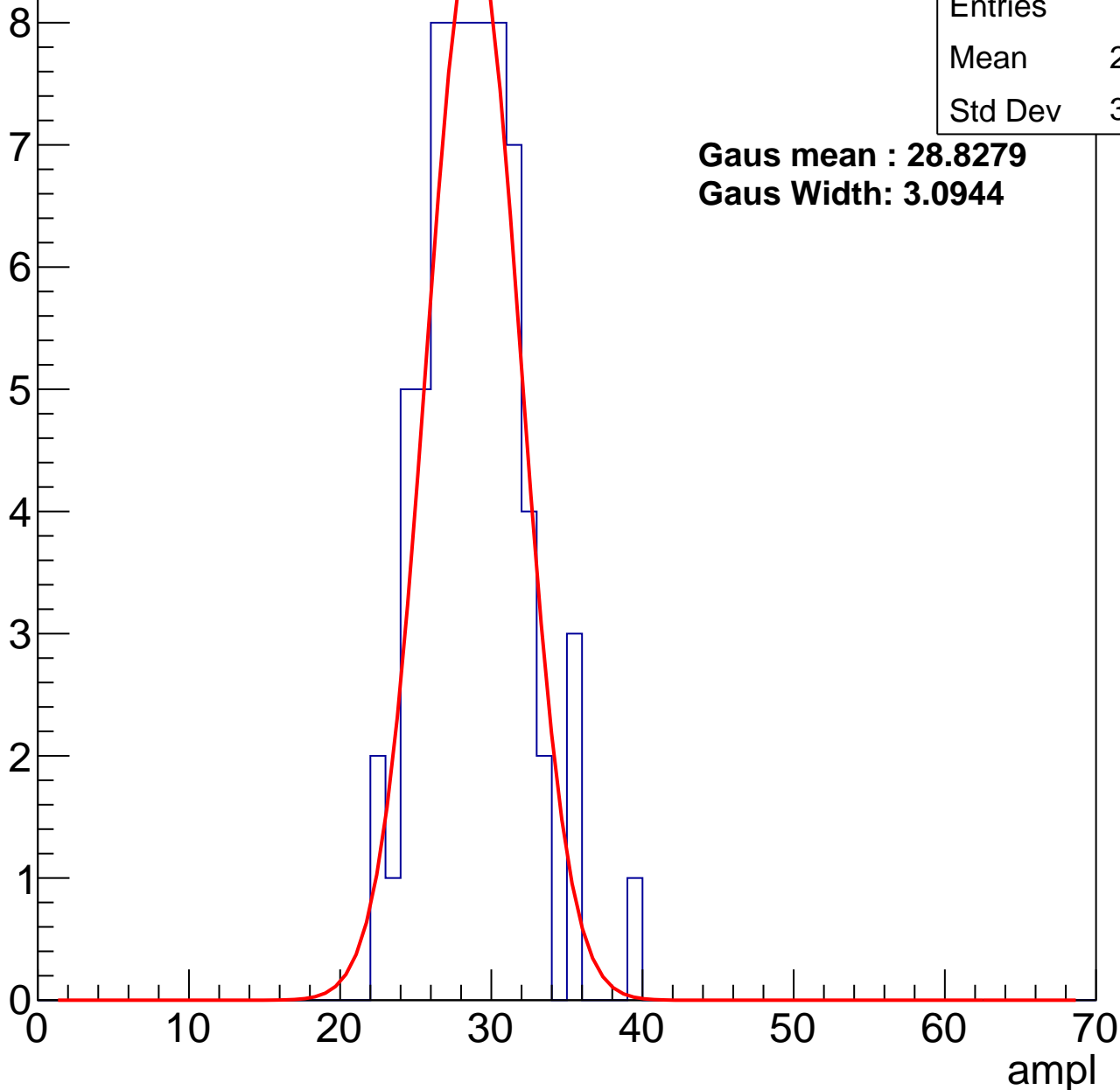
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	70
Mean	28.39
Std Dev	3.244

**Gaus mean : 28.8279**

**Gaus Width: 3.0944**



# B1L100S, U6-ch16, adc1

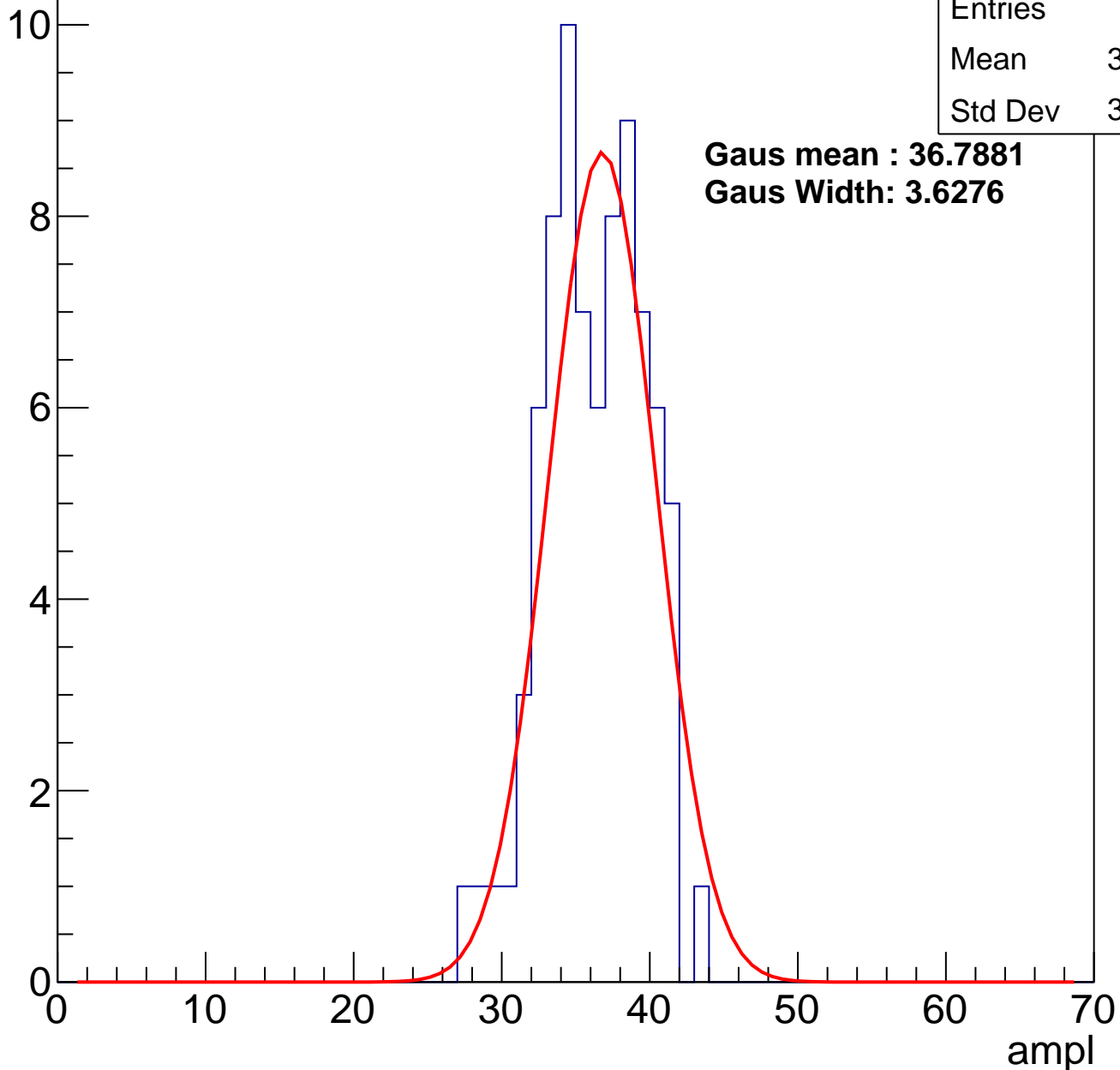
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	80
Mean	35.79
Std Dev	3.342

**Gaus mean : 36.7881**

**Gaus Width: 3.6276**

Entry



# B1L100S, U6-ch16, adc2

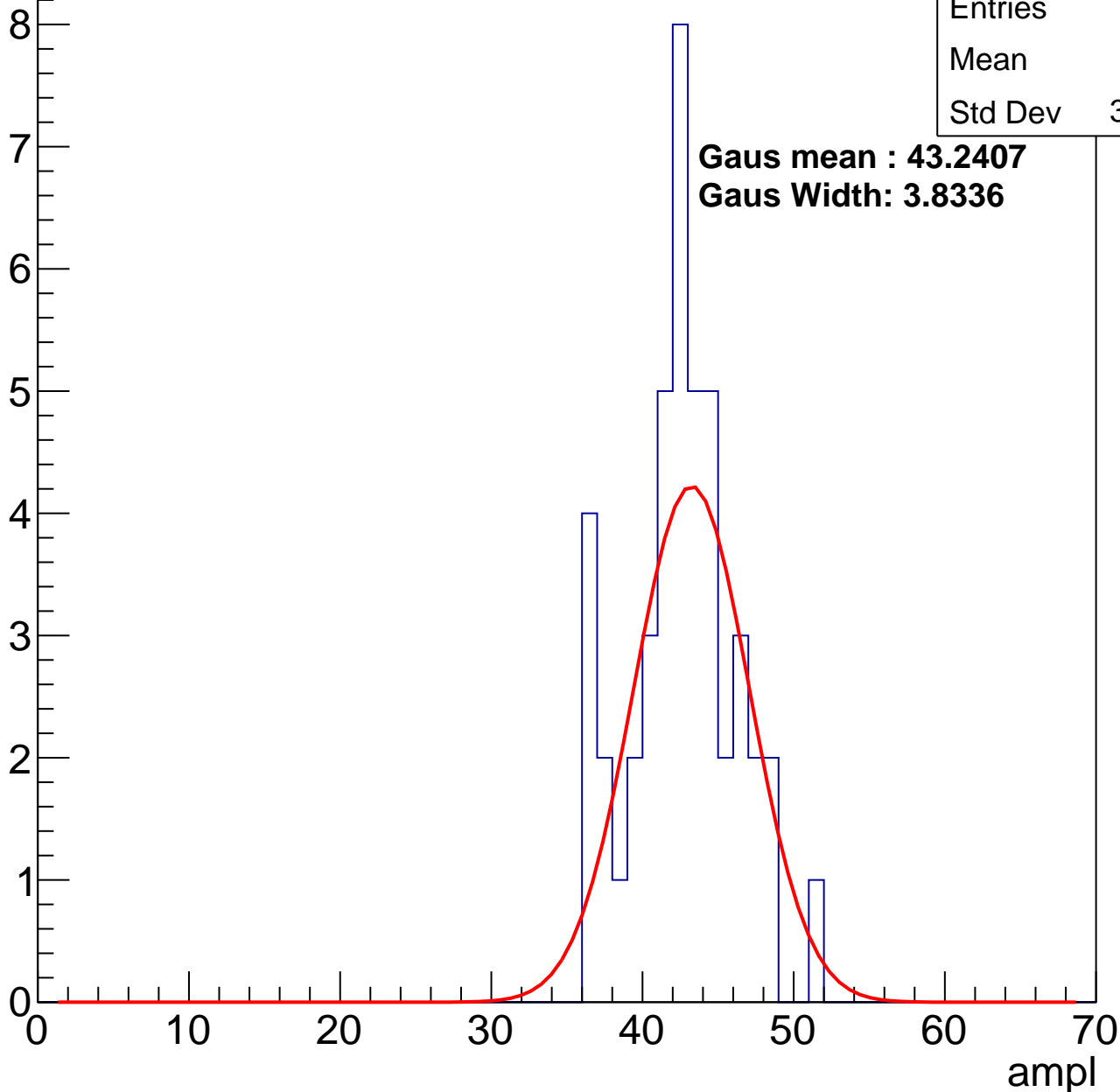
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	45
Mean	42.2
Std Dev	3.455

**Gaus mean : 43.2407**

**Gaus Width: 3.8336**



# B1L100S, U6-ch16, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

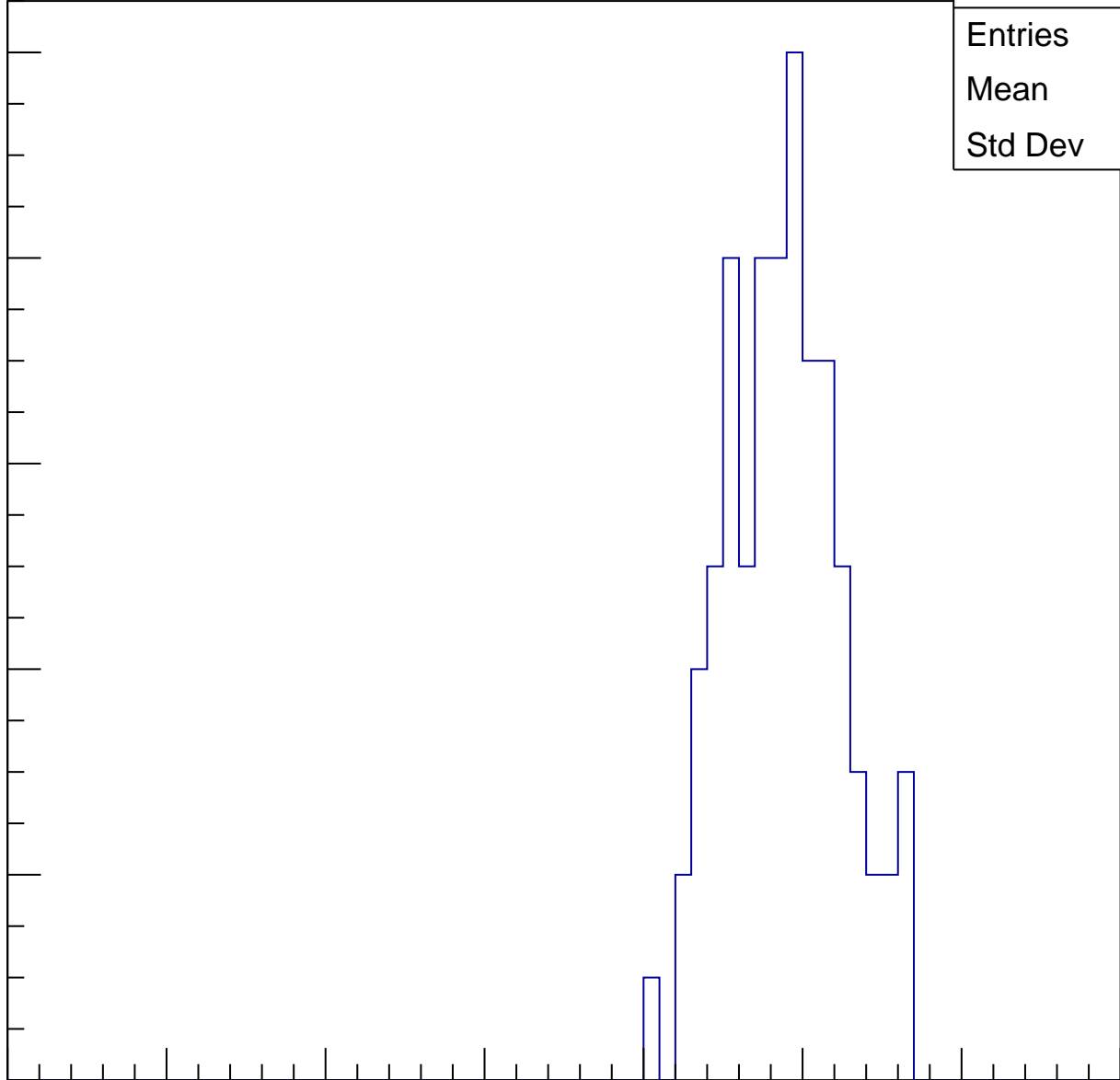
Entries	80
Mean	48.35
Std Dev	3.578

Entry

10  
8  
6  
4  
2  
0

ampl

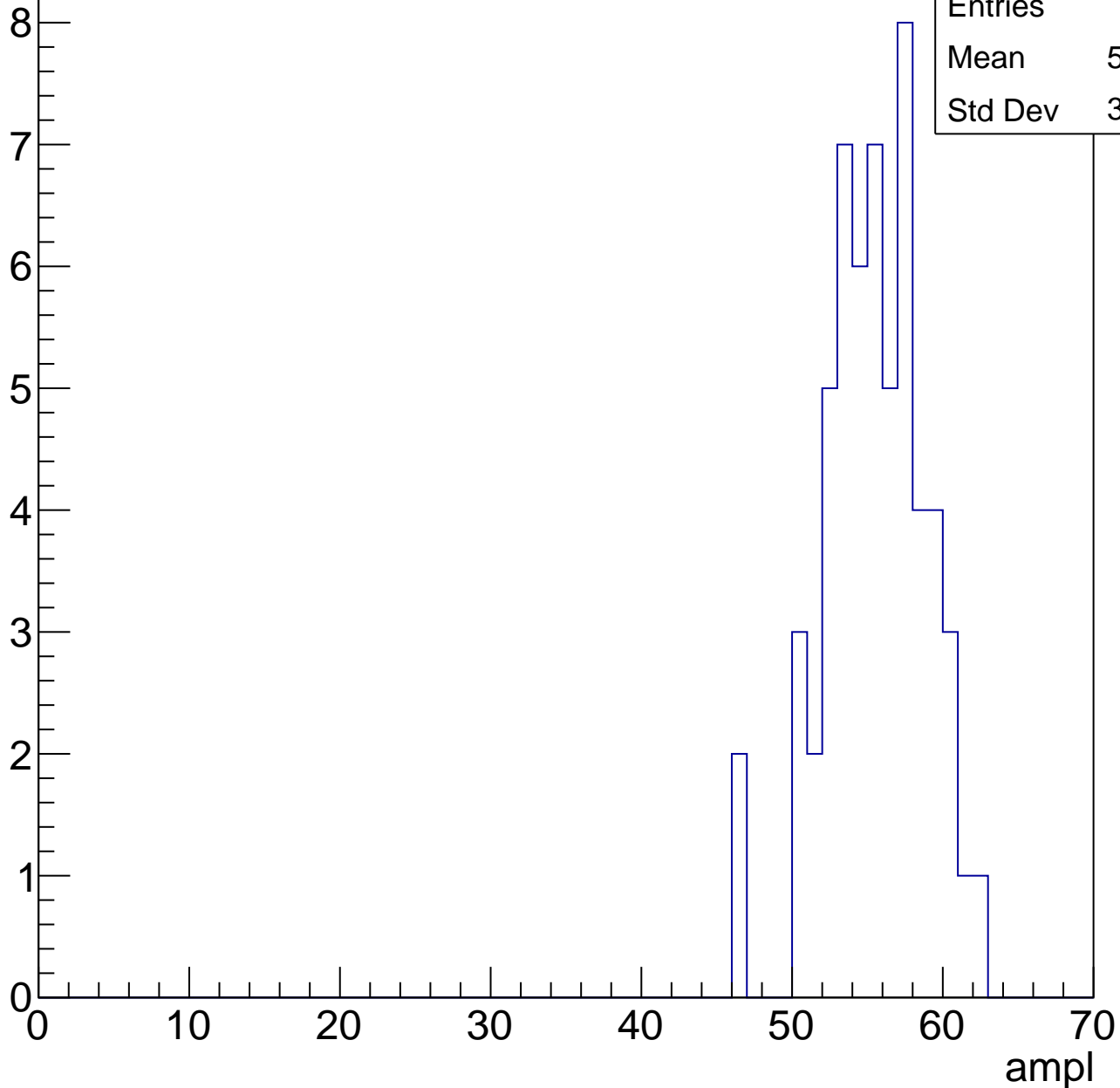
0 10 20 30 40 50 60 70



# B1L100S, U6-ch16, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

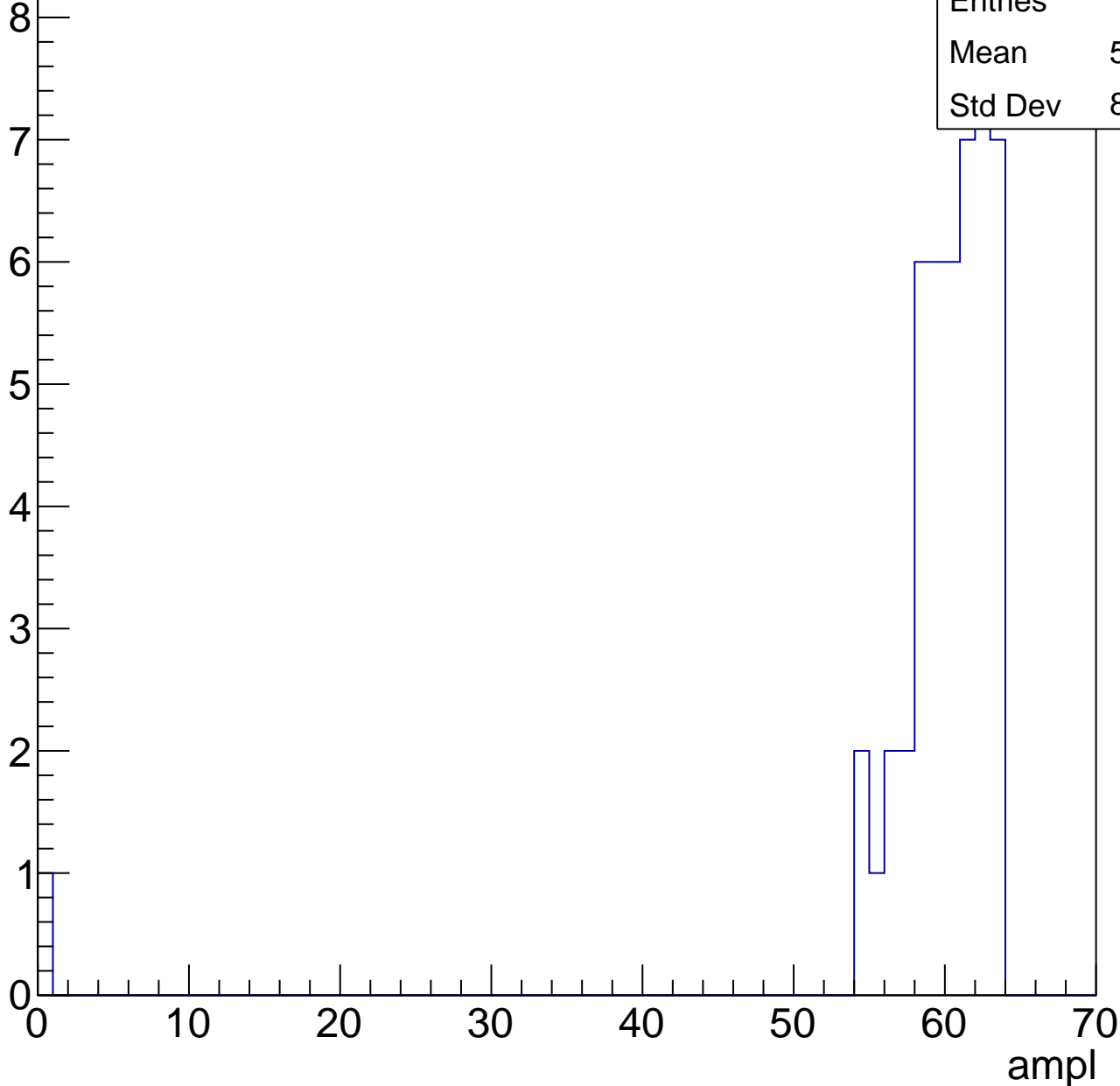


# B1L100S, U6-ch16, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	48
Mean	58.65
Std Dev	8.887



# B1L100S, U6-ch16, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry





# B1L100S, U6-ch16, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



# B1L100S, U6-ch17, adc0

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	70
Mean	29.19
Std Dev	3.011

**Gaus mean : 29.7768**

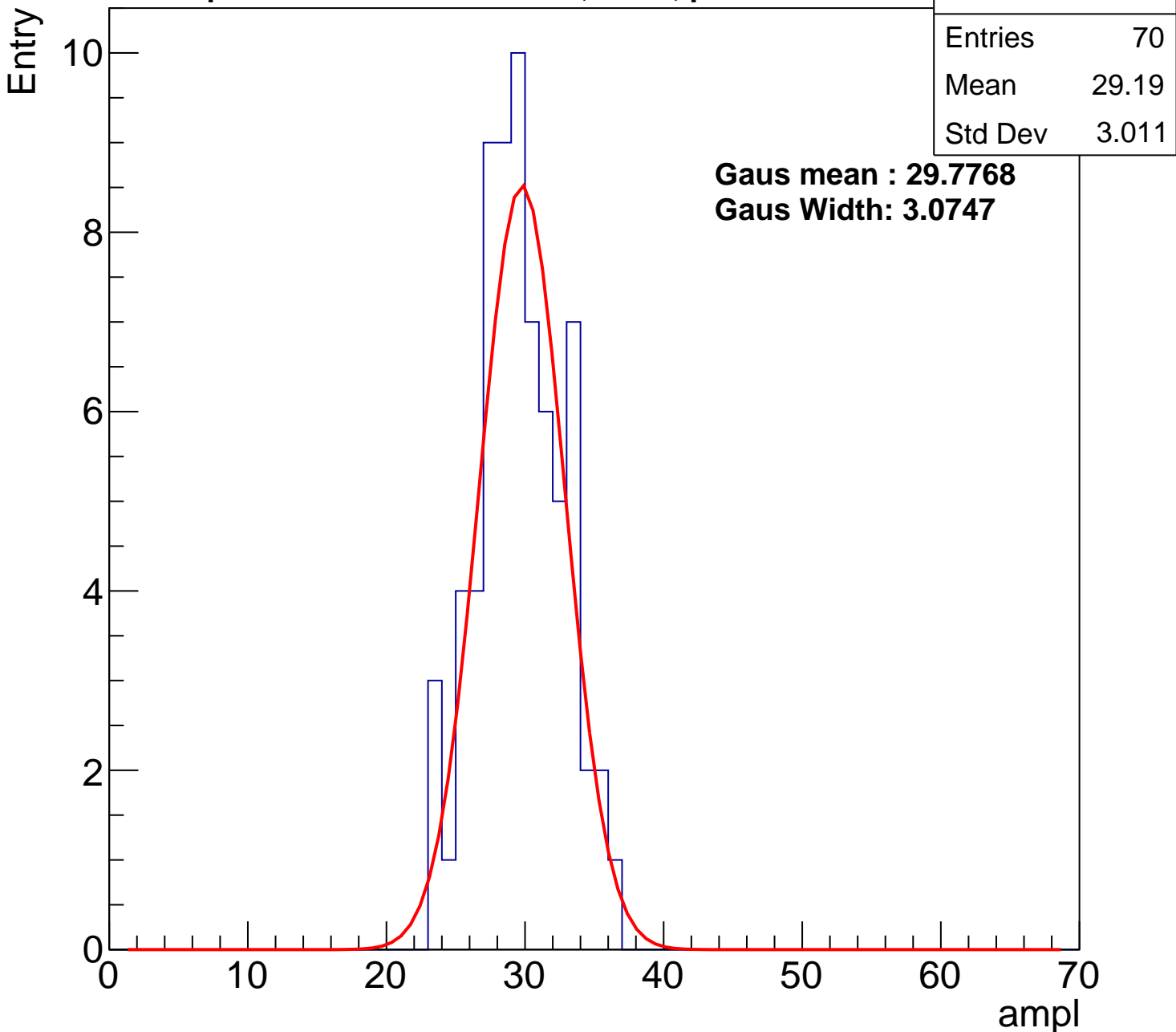
**Gaus Width: 3.0747**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L100S, U6-ch17, adc1

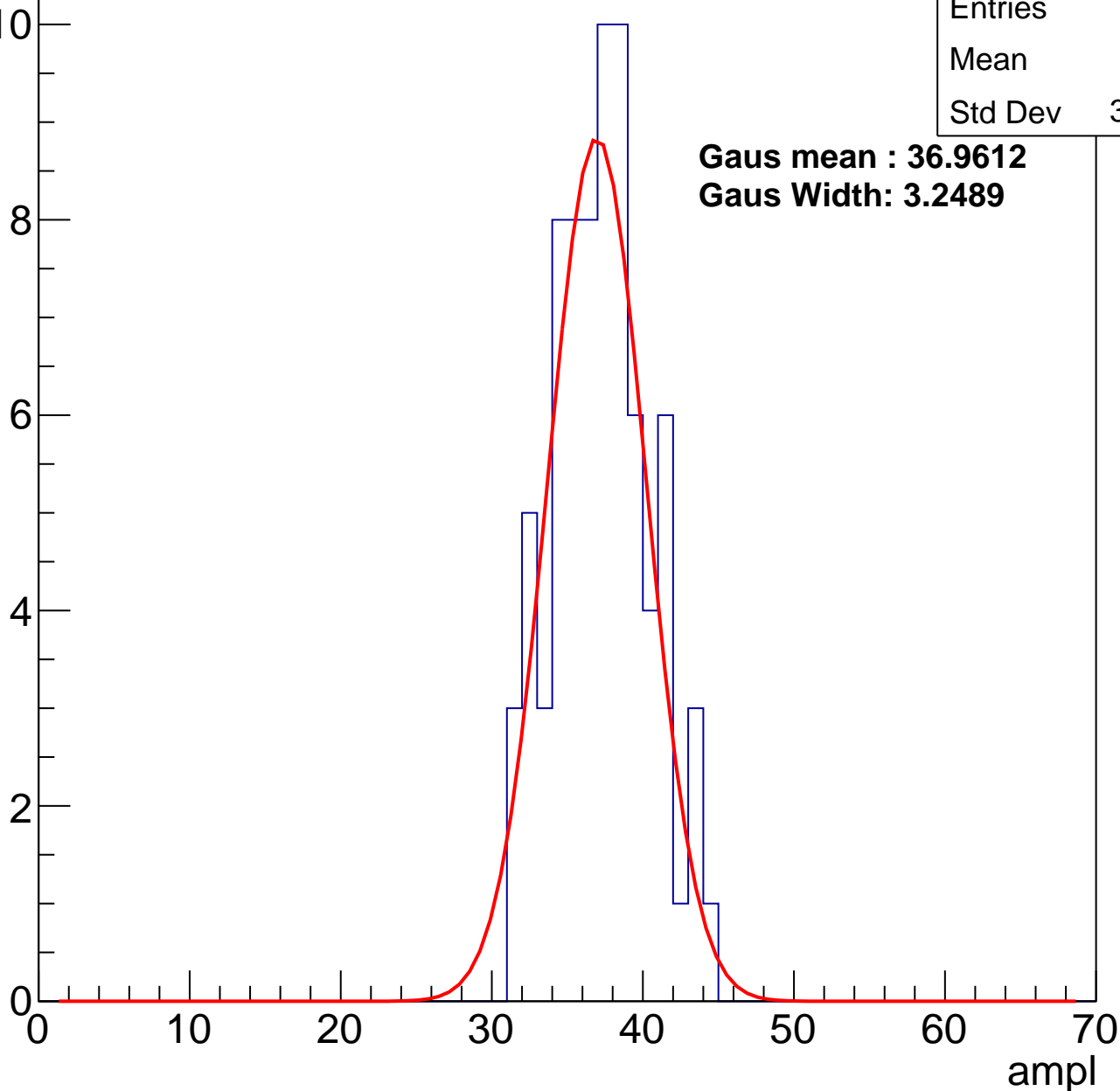
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	76
Mean	36.8
Std Dev	3.116

**Gaus mean : 36.9612**

**Gaus Width: 3.2489**



# B1L100S, U6-ch17, adc2

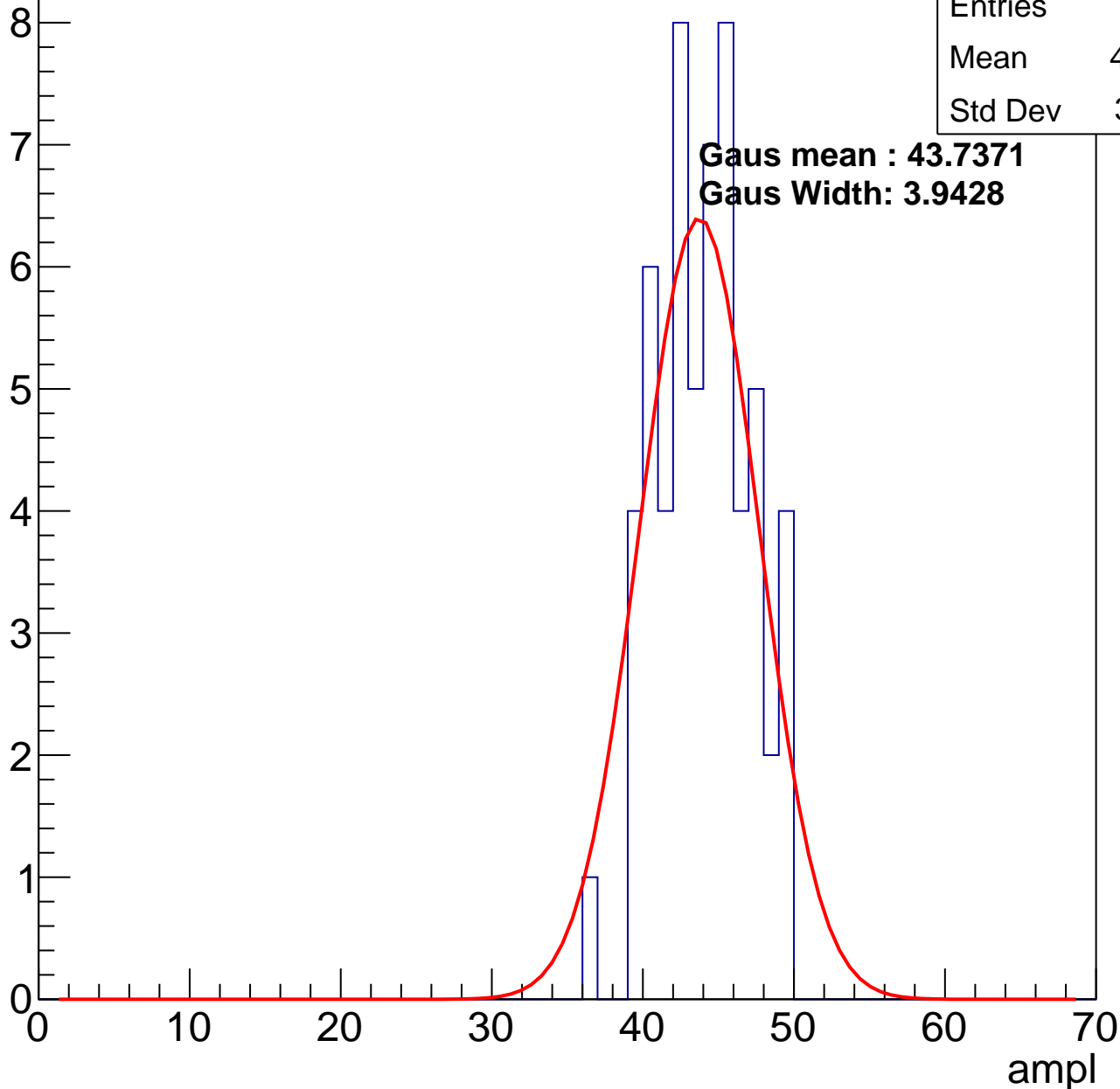
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	58
Mean	43.55
Std Dev	3.001

**Gaus mean : 43.7371**

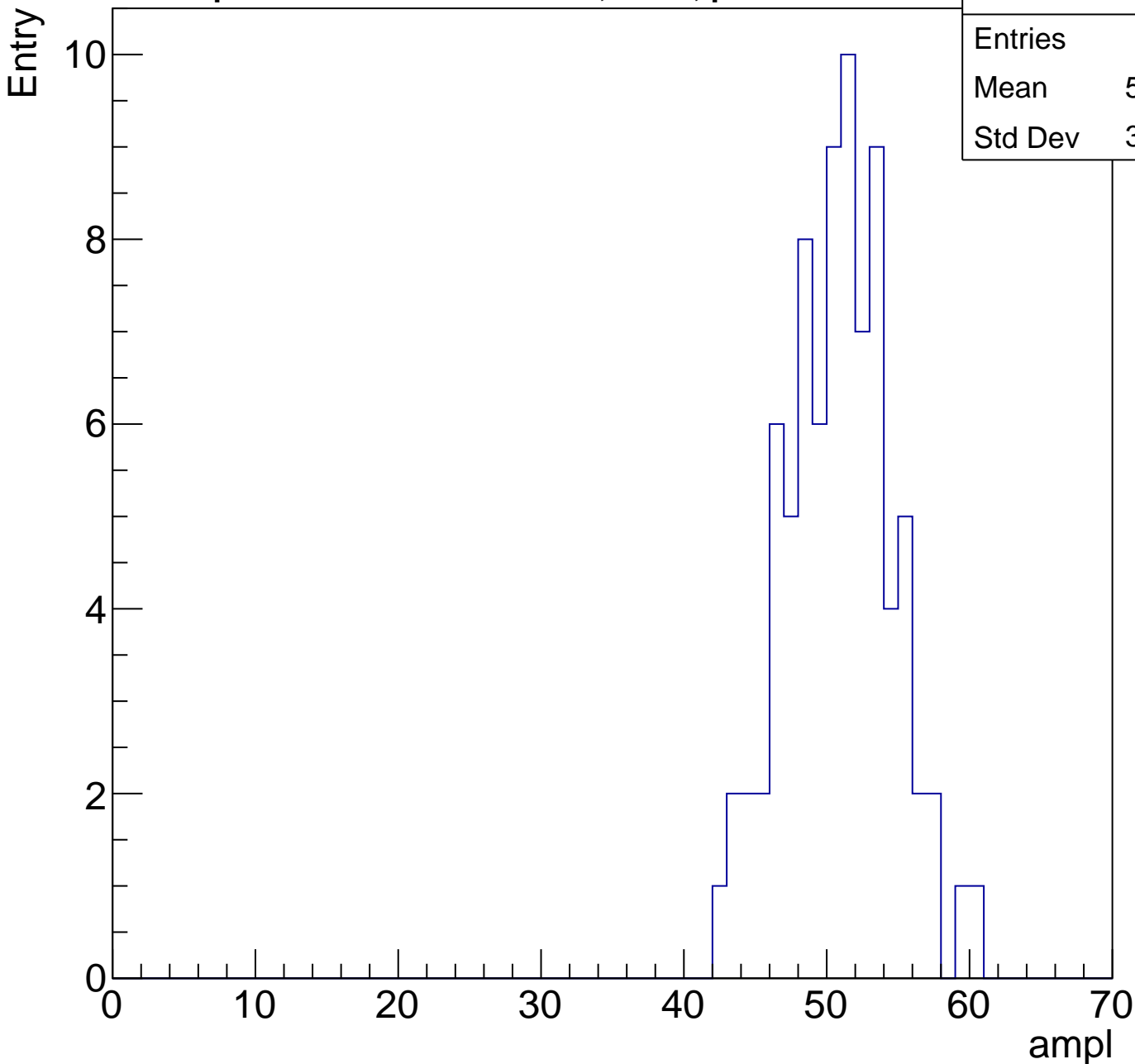
**Gaus Width: 3.9428**



# B1L100S, U6-ch17, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	82
Mean	50.39
Std Dev	3.678

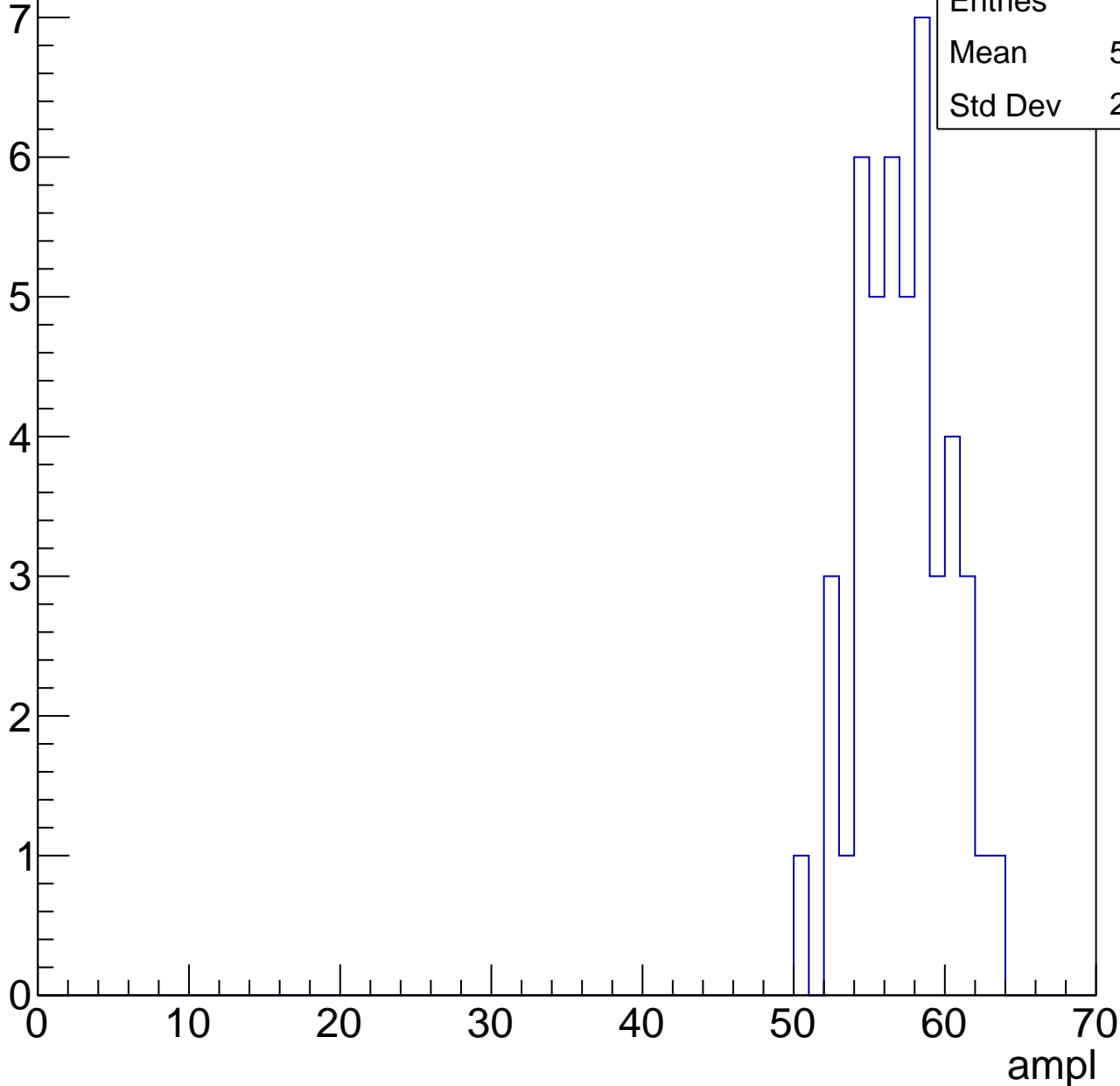


# B1L100S, U6-ch17, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	46
Mean	56.74
Std Dev	2.877



# B1L100S, U6-ch17, adc5

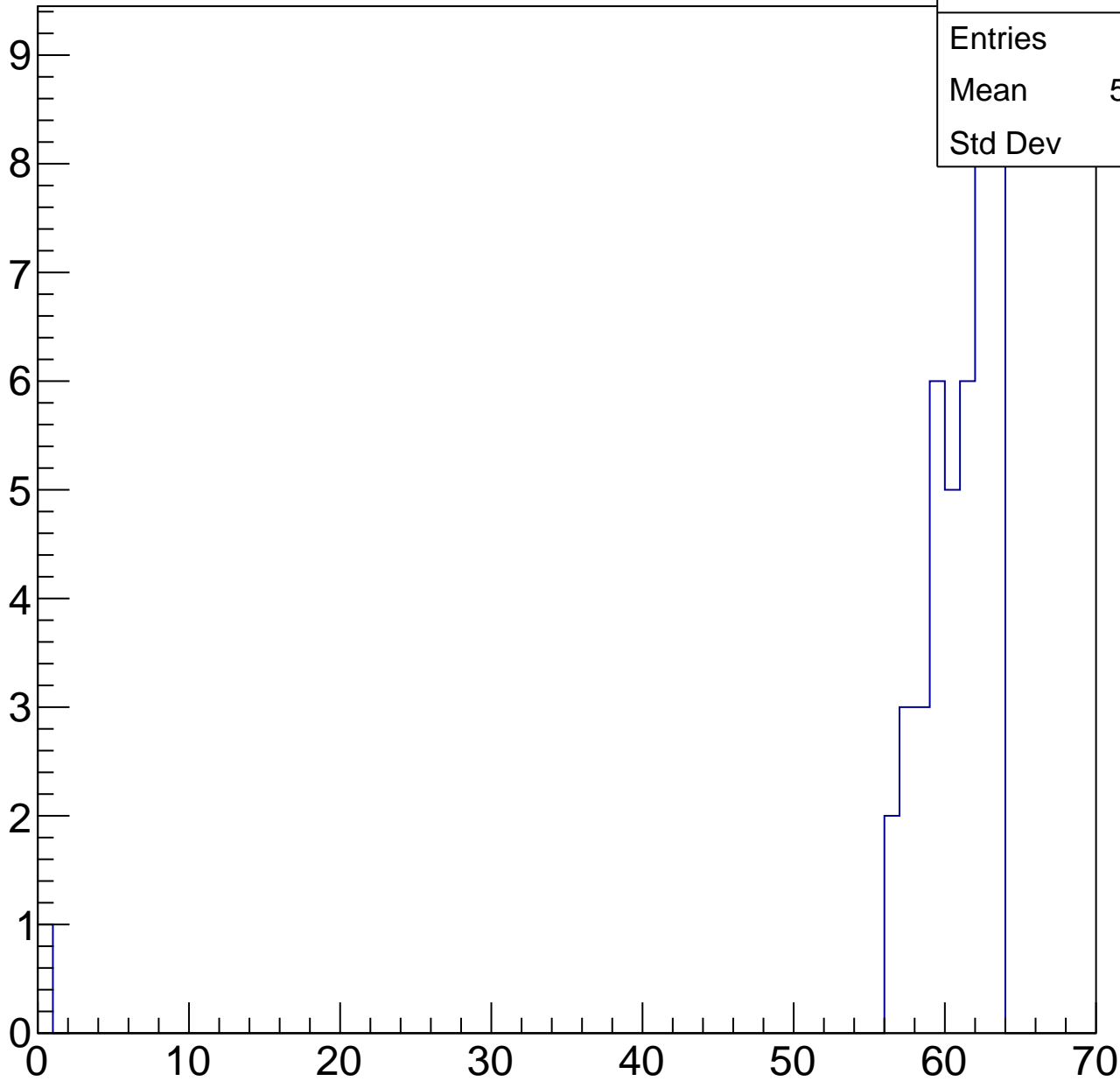
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	43
Mean	59.07
Std Dev	9.35

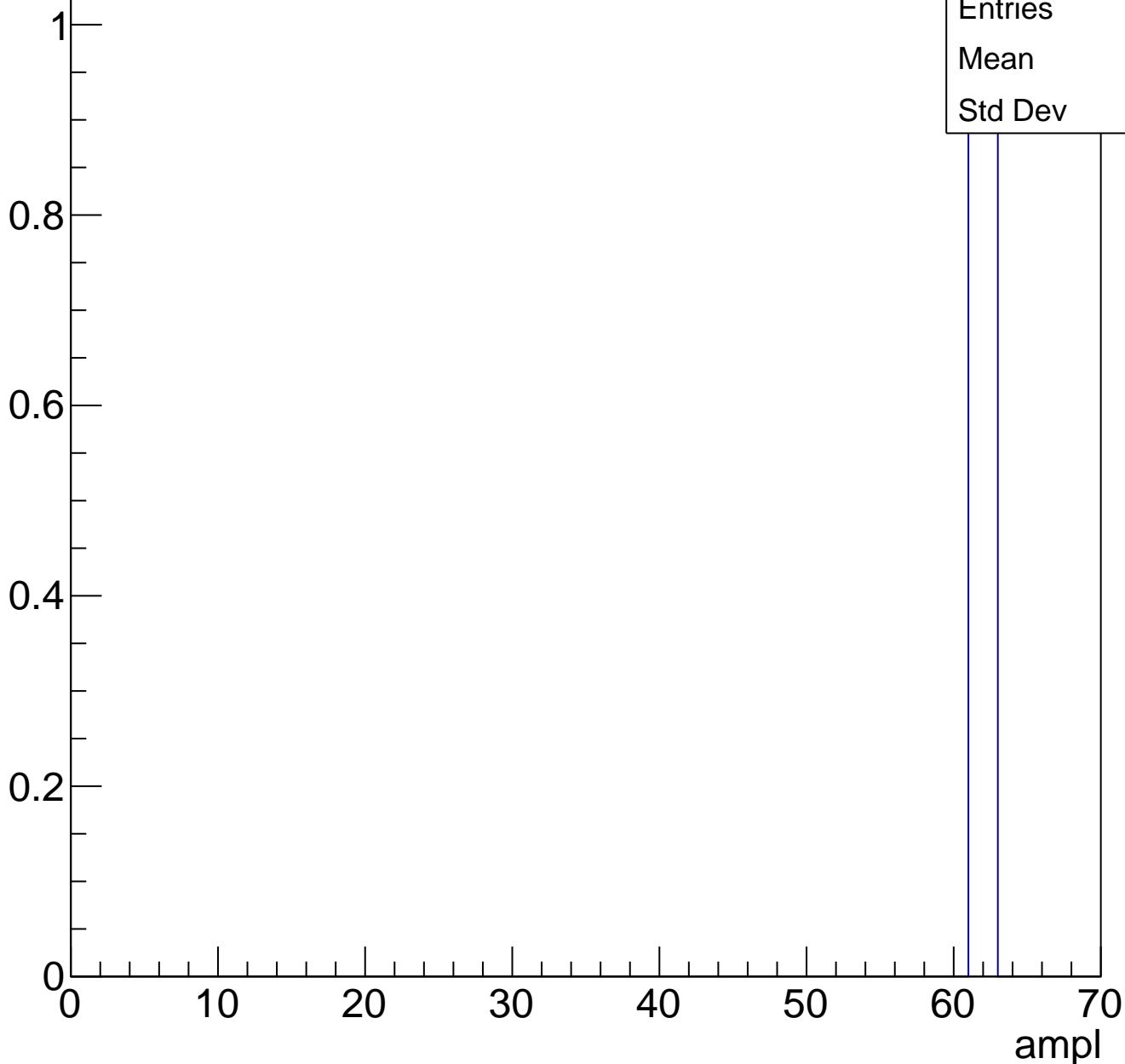
ampl



# B1L100S, U6-ch17, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry





# B1L100S, U6-ch17, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



# B1L100S, U6-ch18, adc0

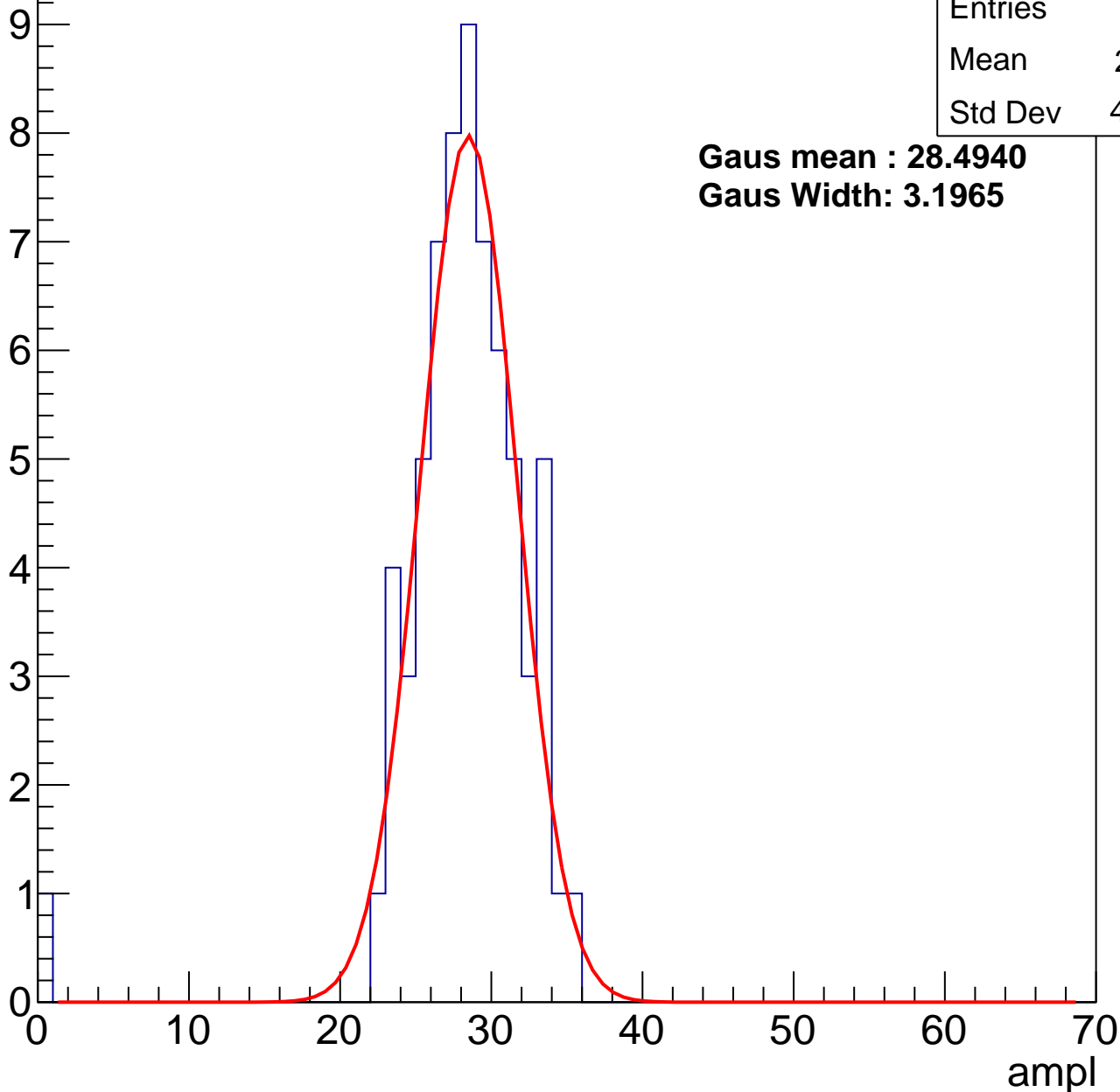
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	66
Mean	27.71
Std Dev	4.569

**Gaus mean : 28.4940**

**Gaus Width: 3.1965**



# B1L100S, U6-ch18, adc1

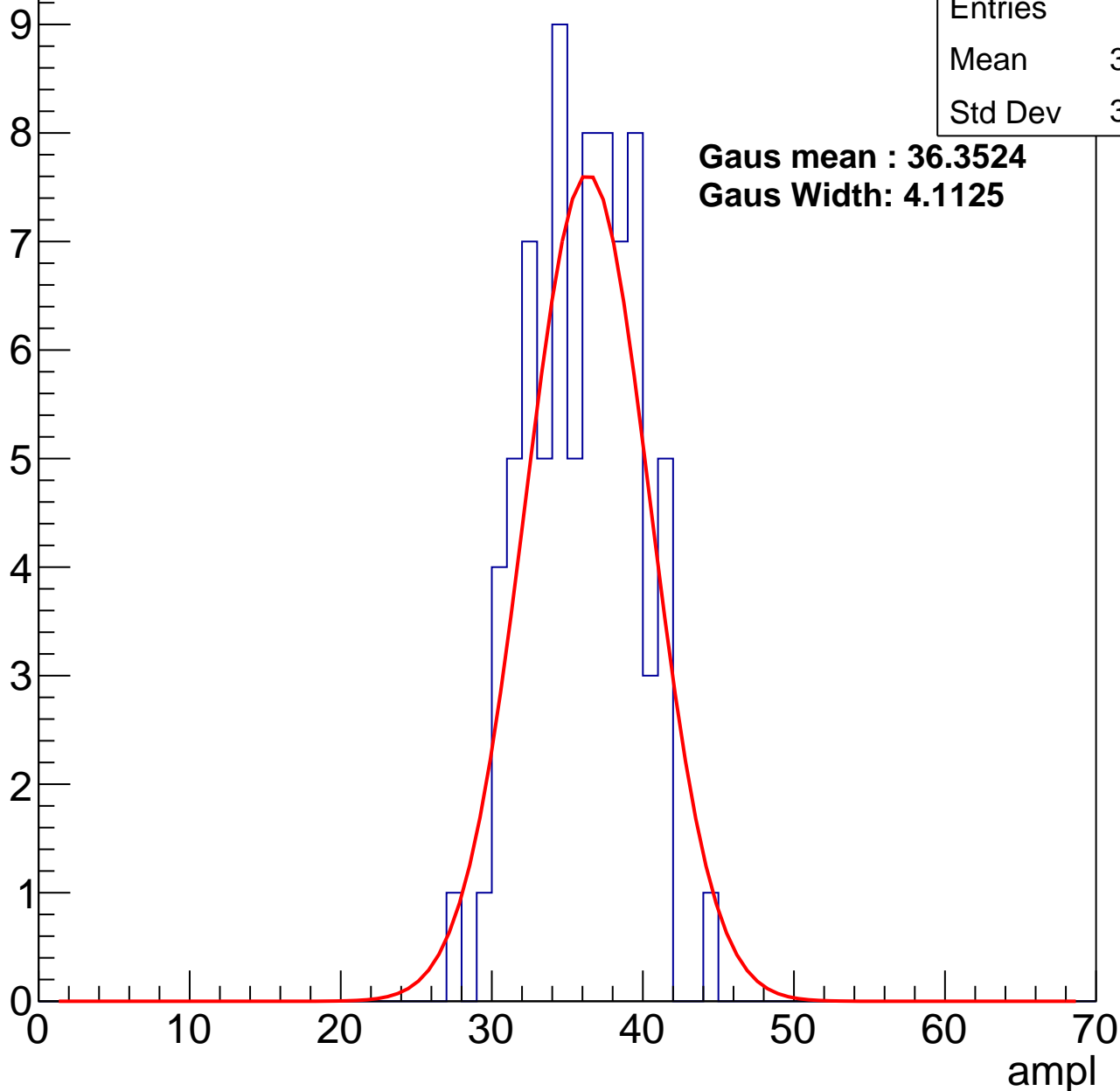
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	77
Mean	35.48
Std Dev	3.459

**Gaus mean : 36.3524**

**Gaus Width: 4.1125**



# B1L100S, U6-ch18, adc2

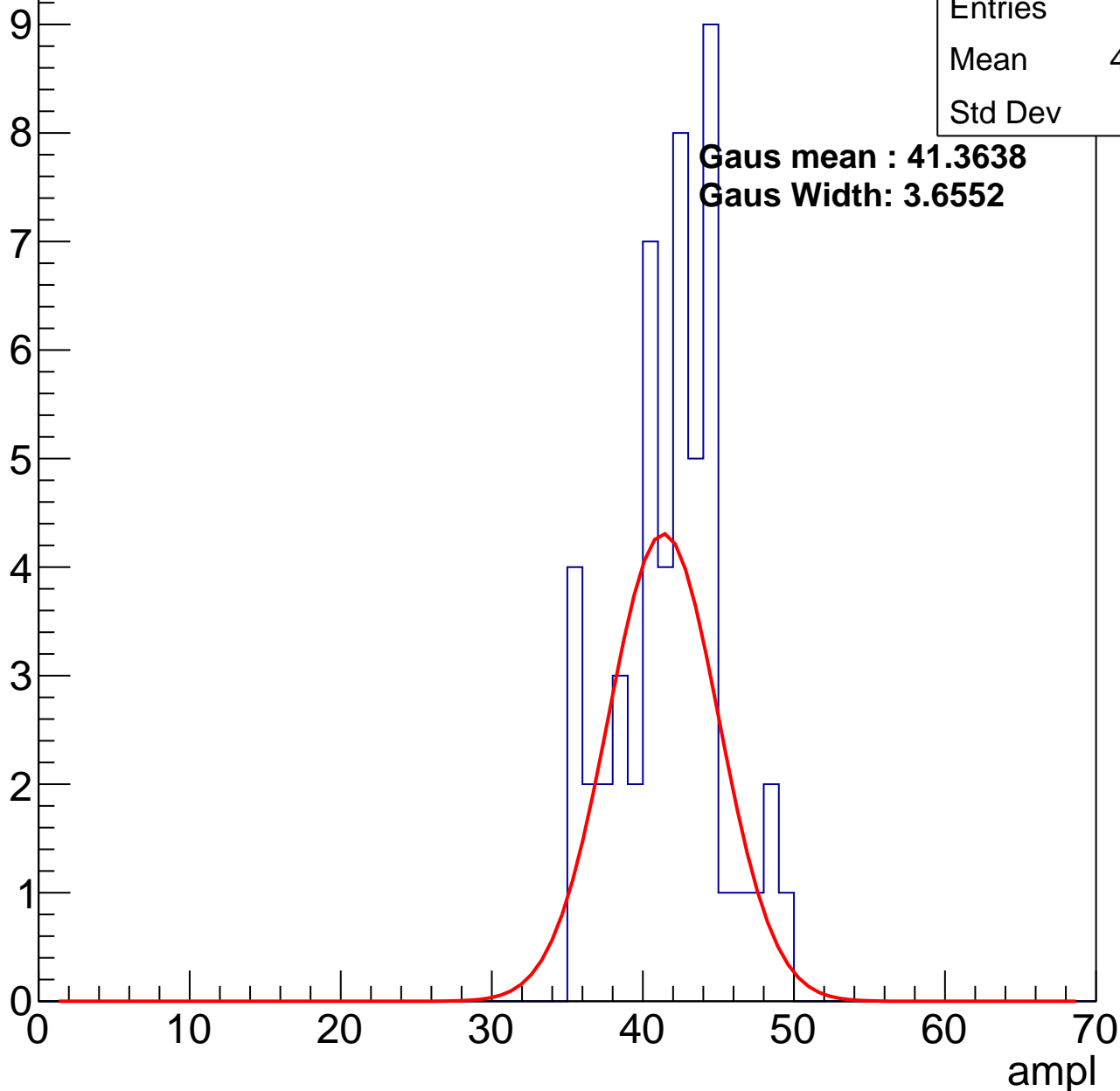
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	52
Mean	41.38
Std Dev	3.42

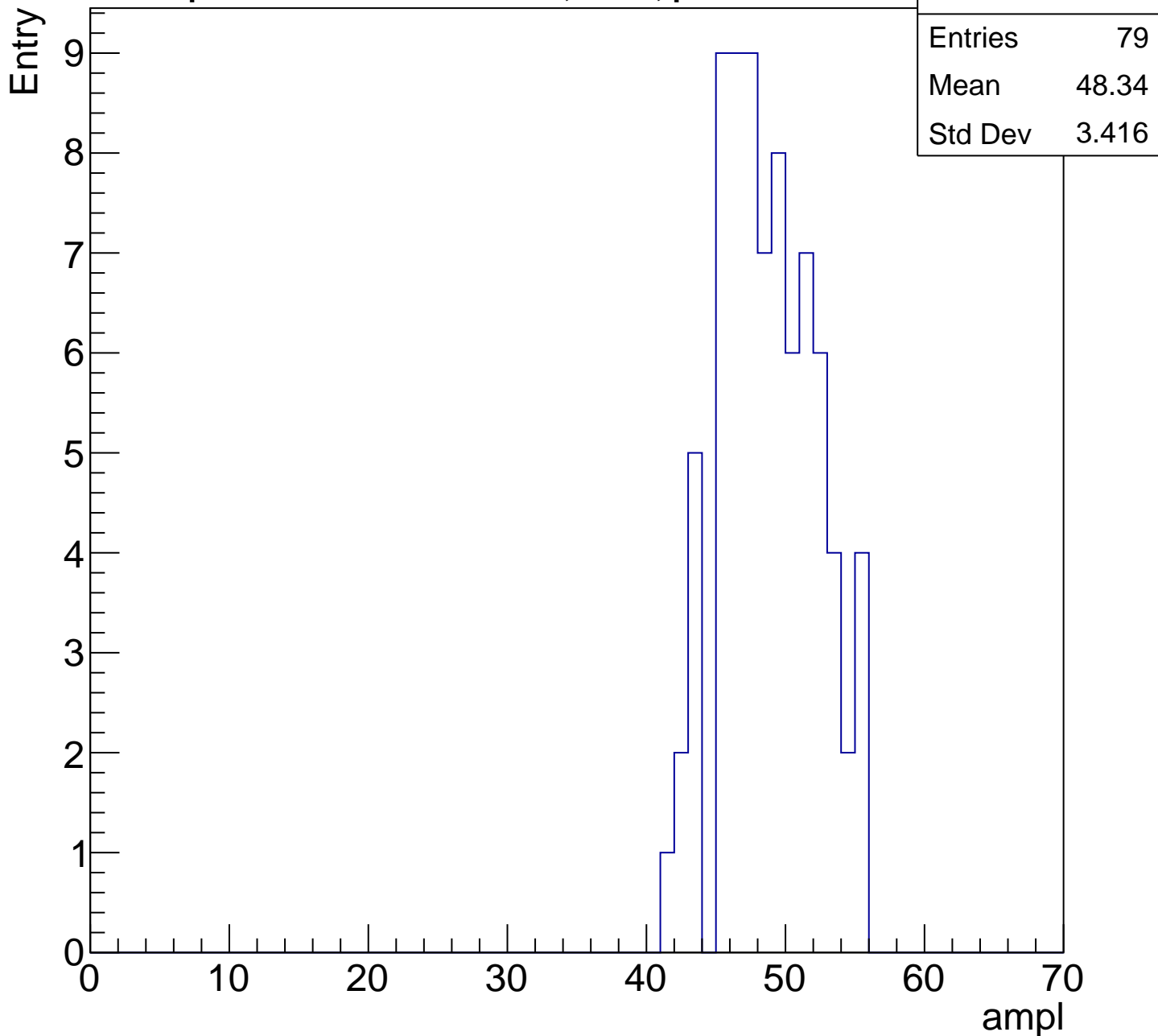
**Gaus mean : 41.3638**

**Gaus Width: 3.6552**



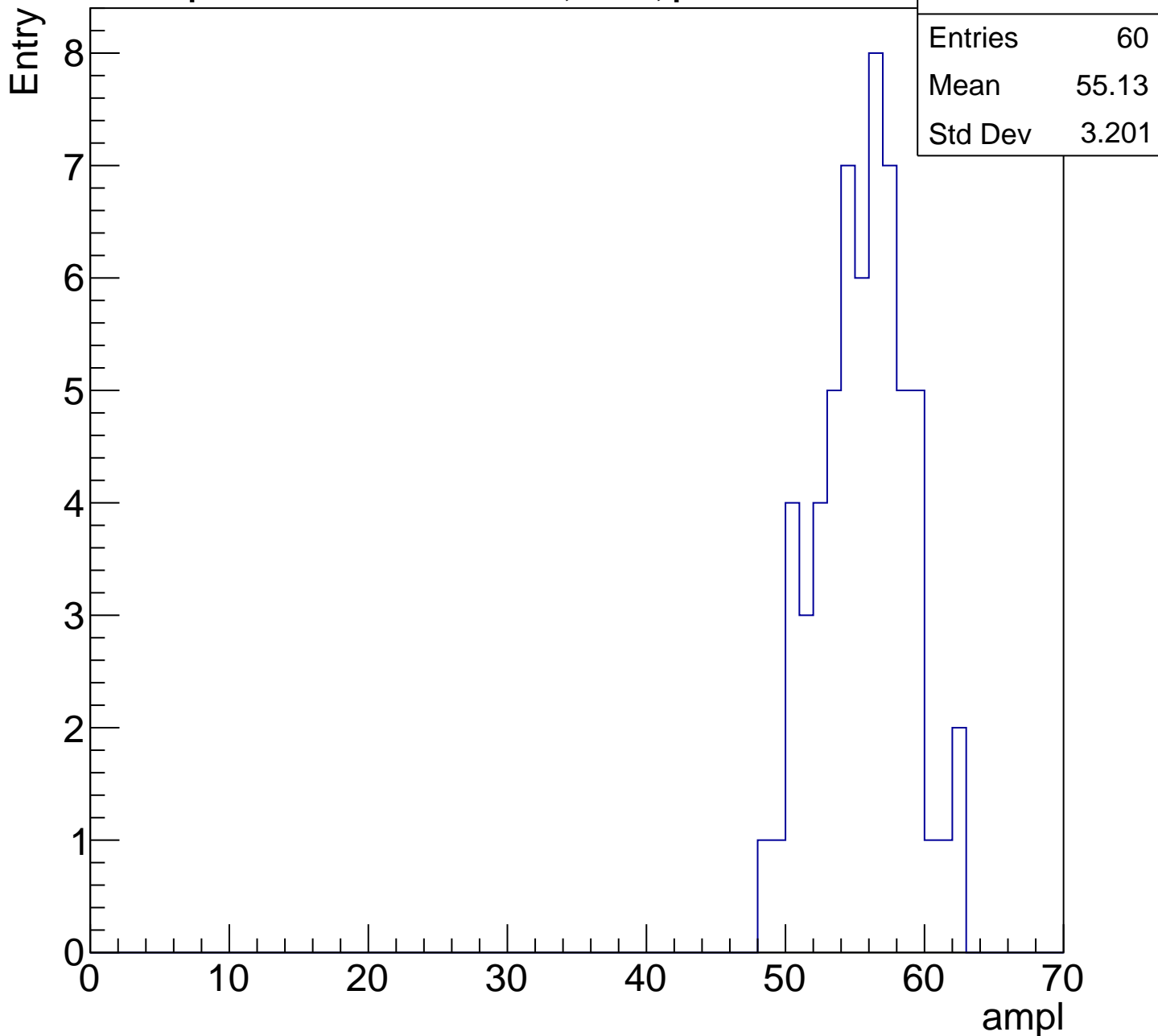
# B1L100S, U6-ch18, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2



# B1L100S, U6-ch18, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2



# B1L100S, U6-ch18, adc5

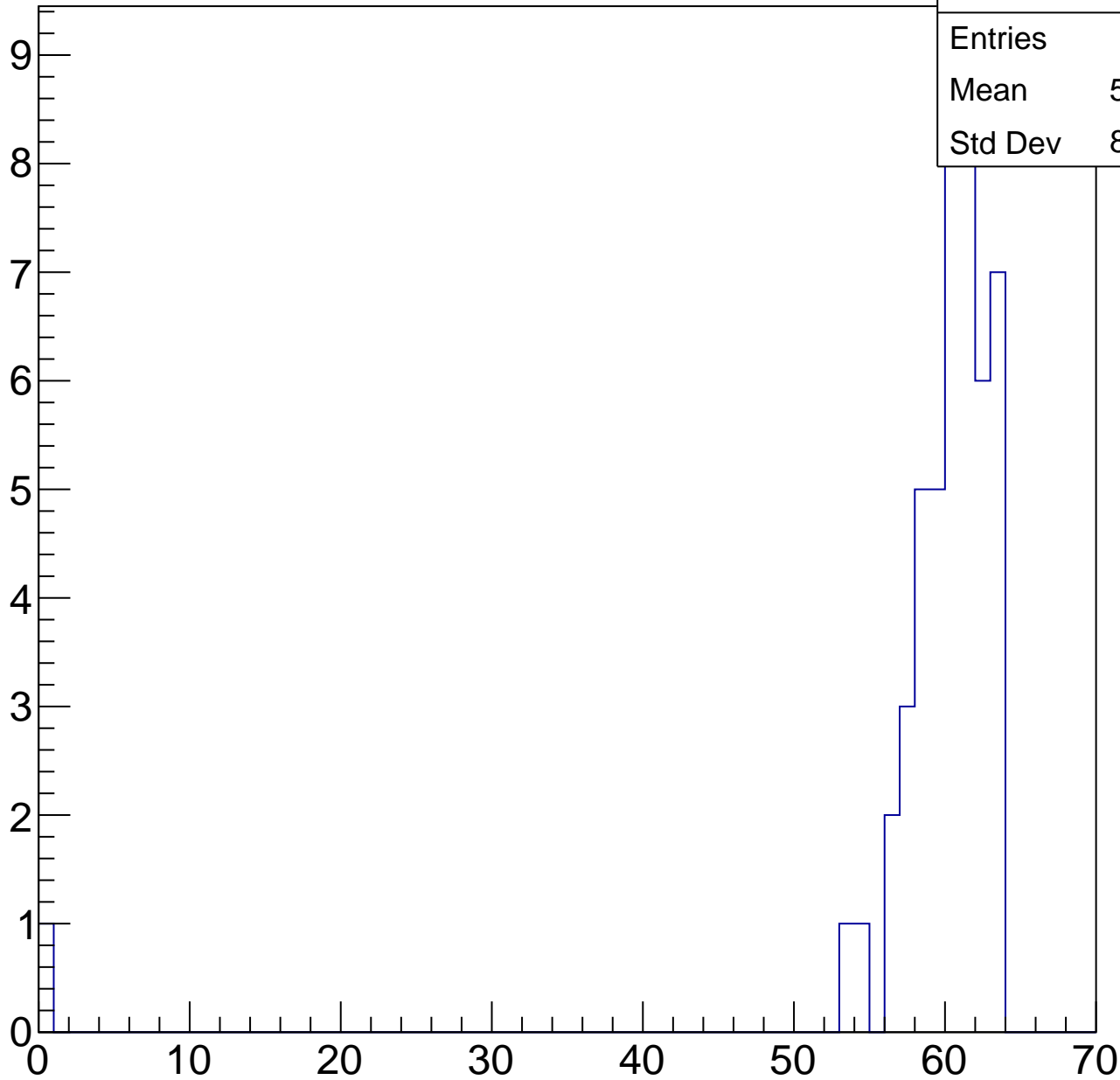
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	48
Mean	58.69
Std Dev	8.877

ampl



# B1L100S, U6-ch18, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry





# B1L100S, U6-ch18, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L100S, U6-ch19, adc0

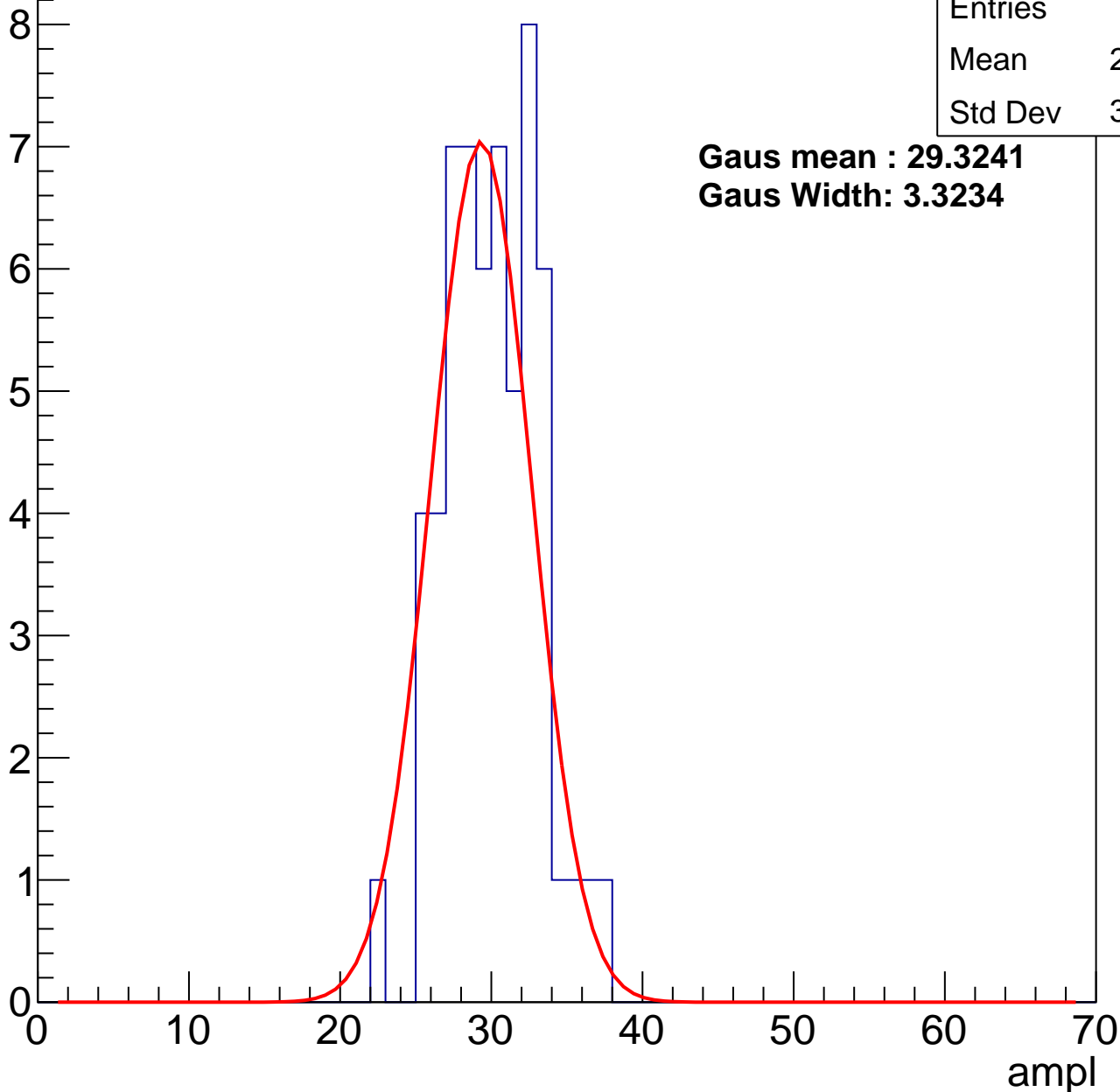
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	59
Mean	29.59
Std Dev	3.003

**Gaus mean : 29.3241**

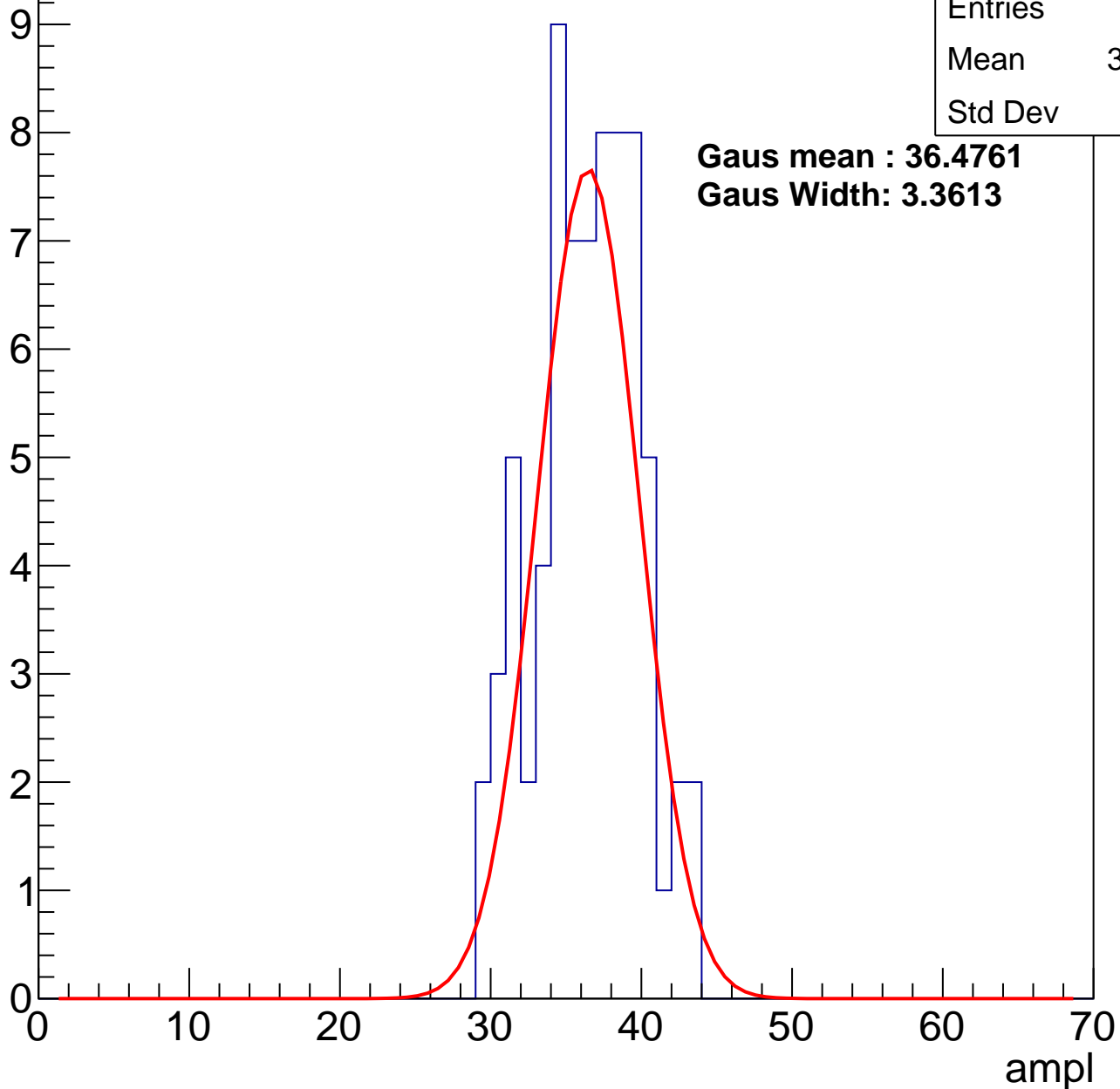
**Gaus Width: 3.3234**



# B1L100S, U6-ch19, adc1

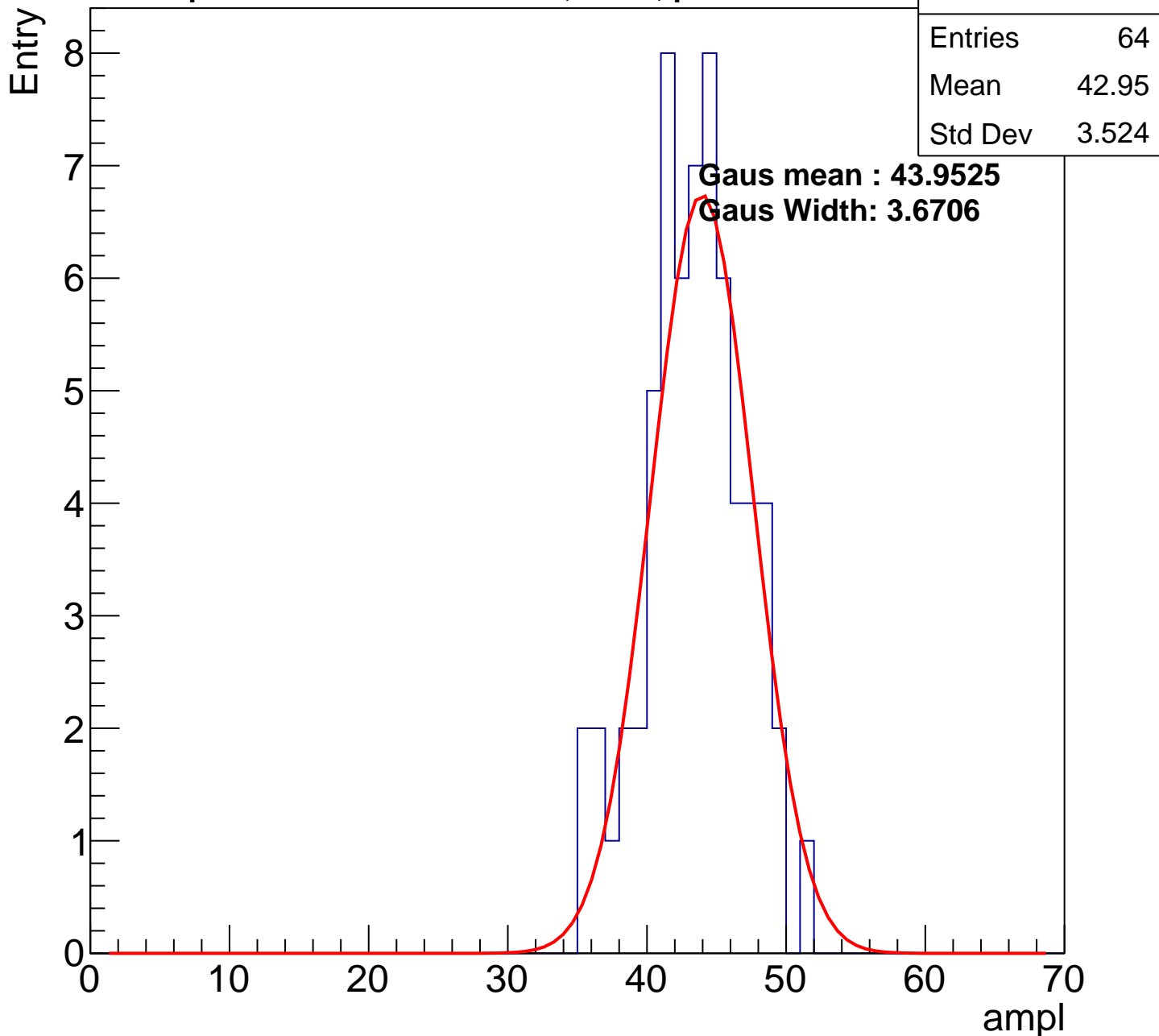
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



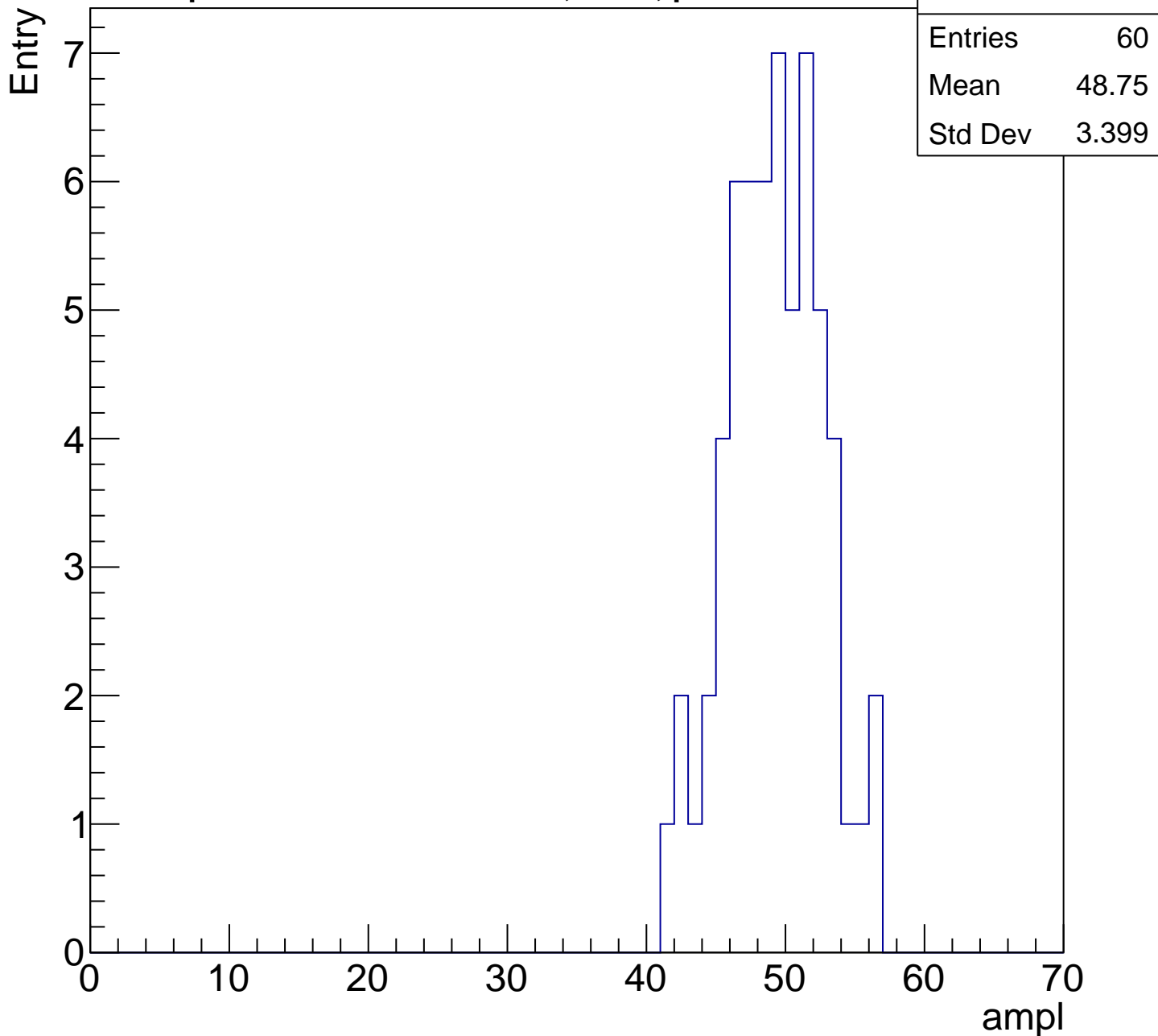
# B1L100S, U6-ch19, adc2

calib\_packv5\_042523\_0143.root, FC#4, port A2



# B1L100S, U6-ch19, adc3

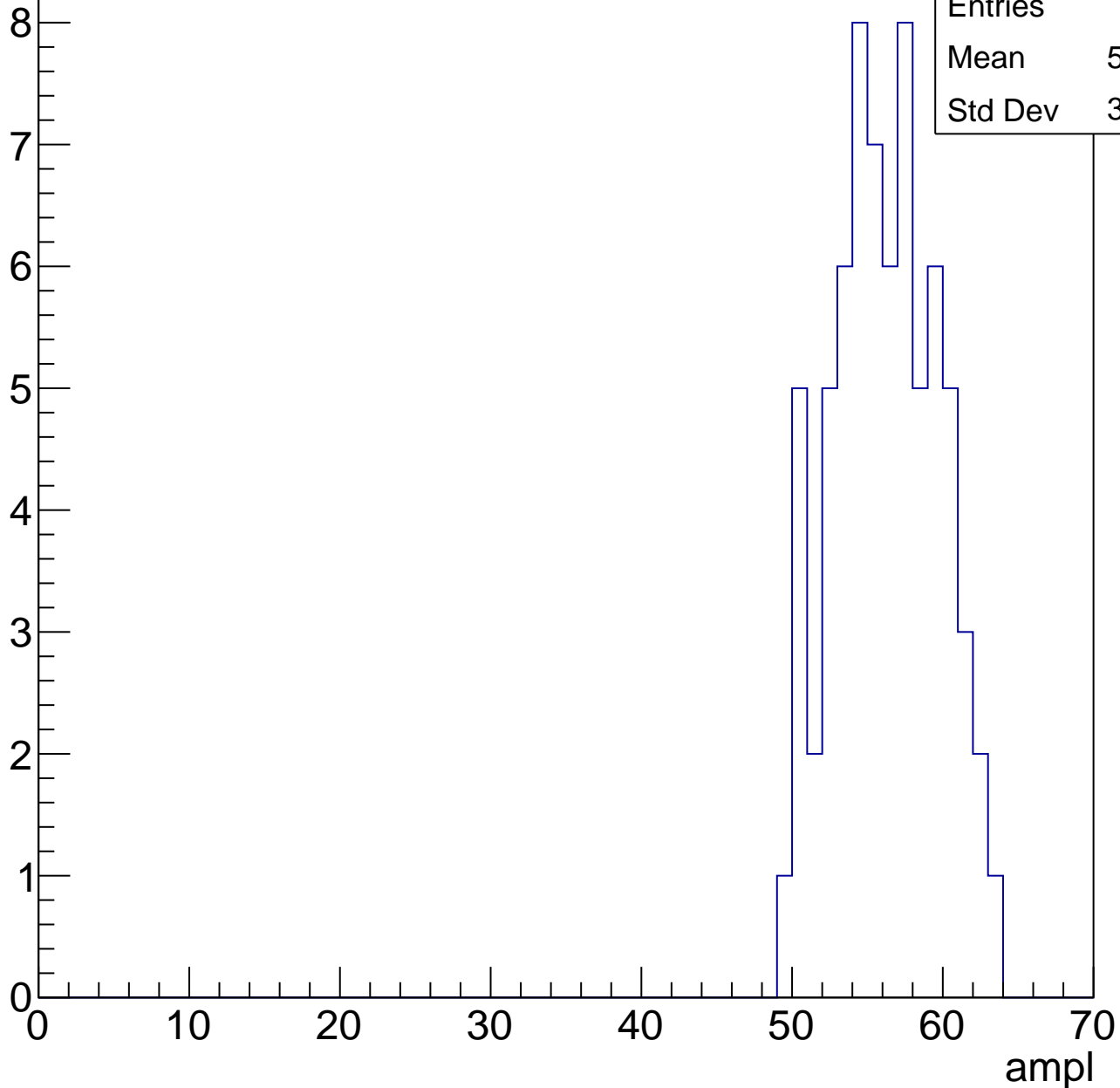
calib\_packv5\_042523\_0143.root, FC#4, port A2



# B1L100S, U6-ch19, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

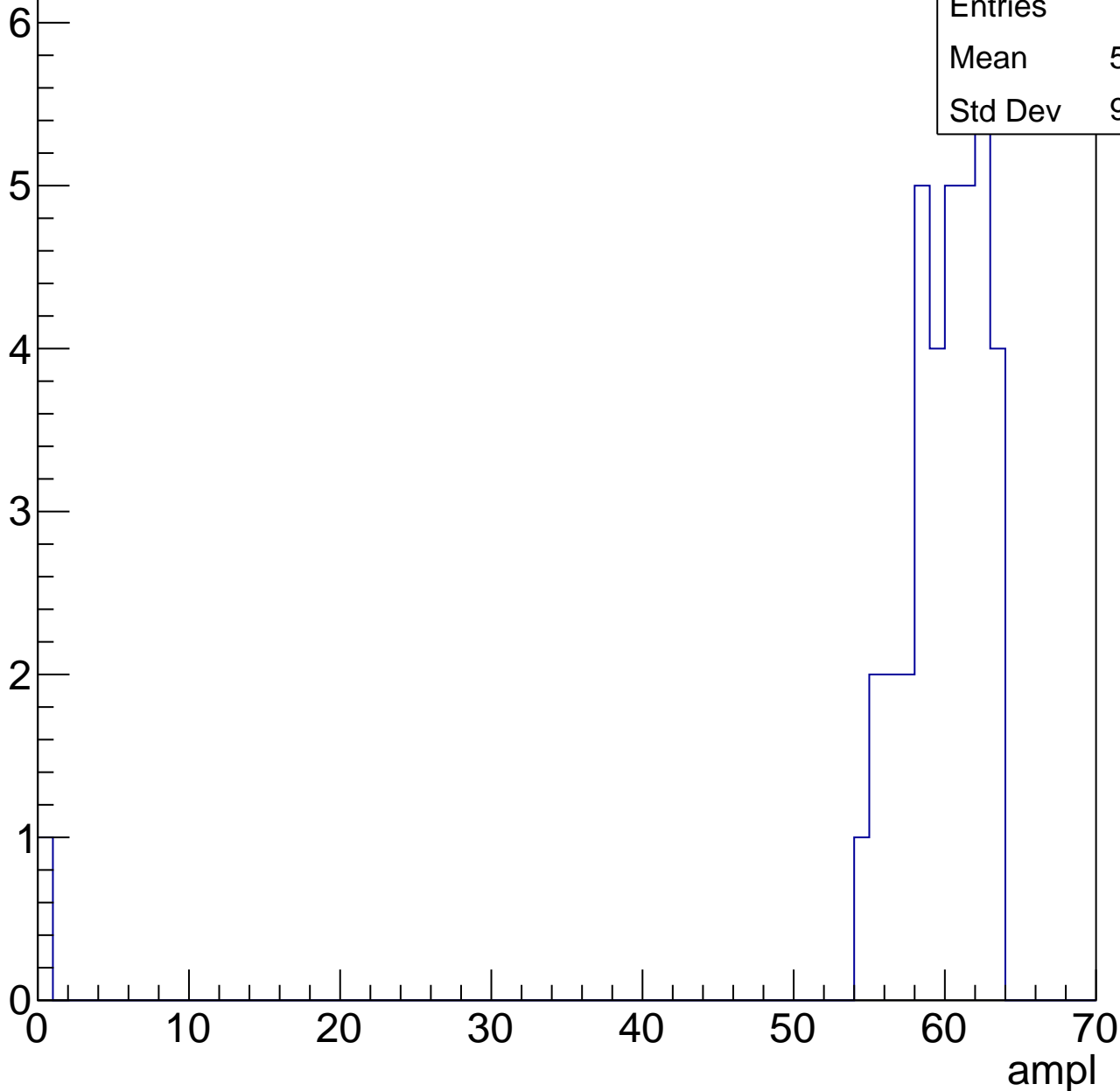


# B1L100S, U6-ch19, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	37
Mean	57.97
Std Dev	9.963

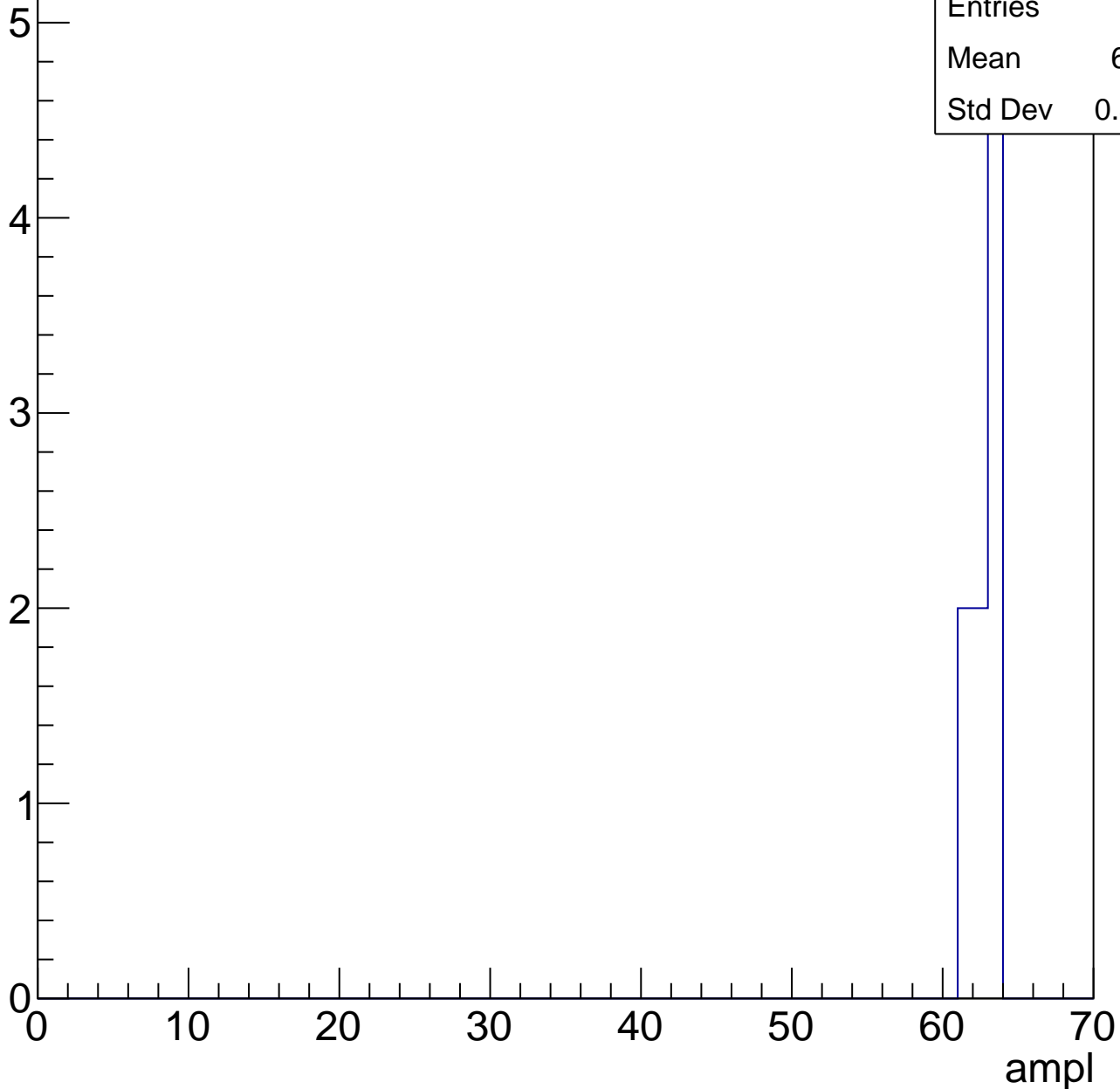


# B1L100S, U6-ch19, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	9
Mean	62.33
Std Dev	0.8165





# B1L100S, U6-ch19, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



# B1L100S, U6-ch20, adc0

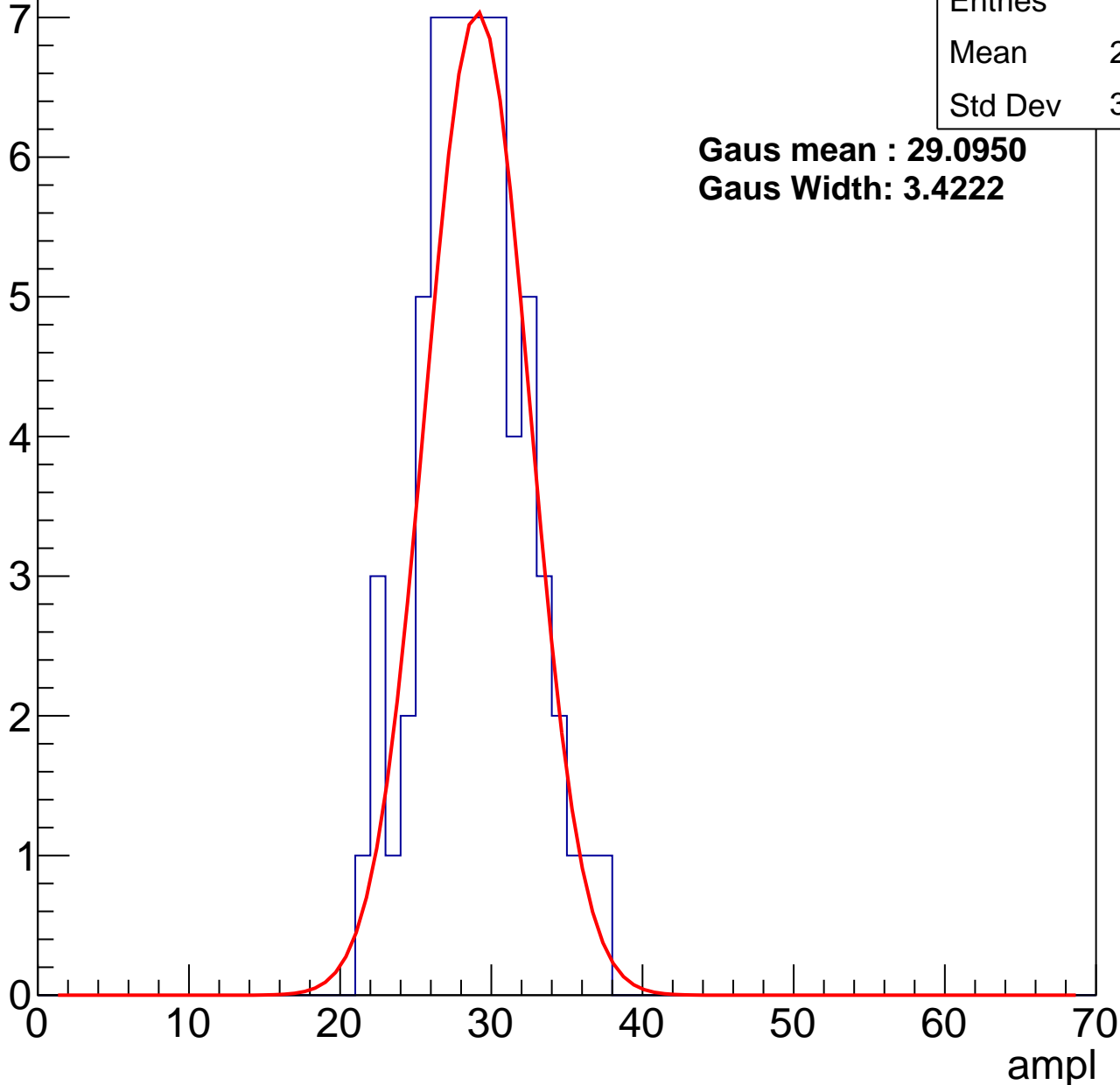
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	64
Mean	28.47
Std Dev	3.473

**Gaus mean : 29.0950**

**Gaus Width: 3.4222**



# B1L100S, U6-ch20, adc1

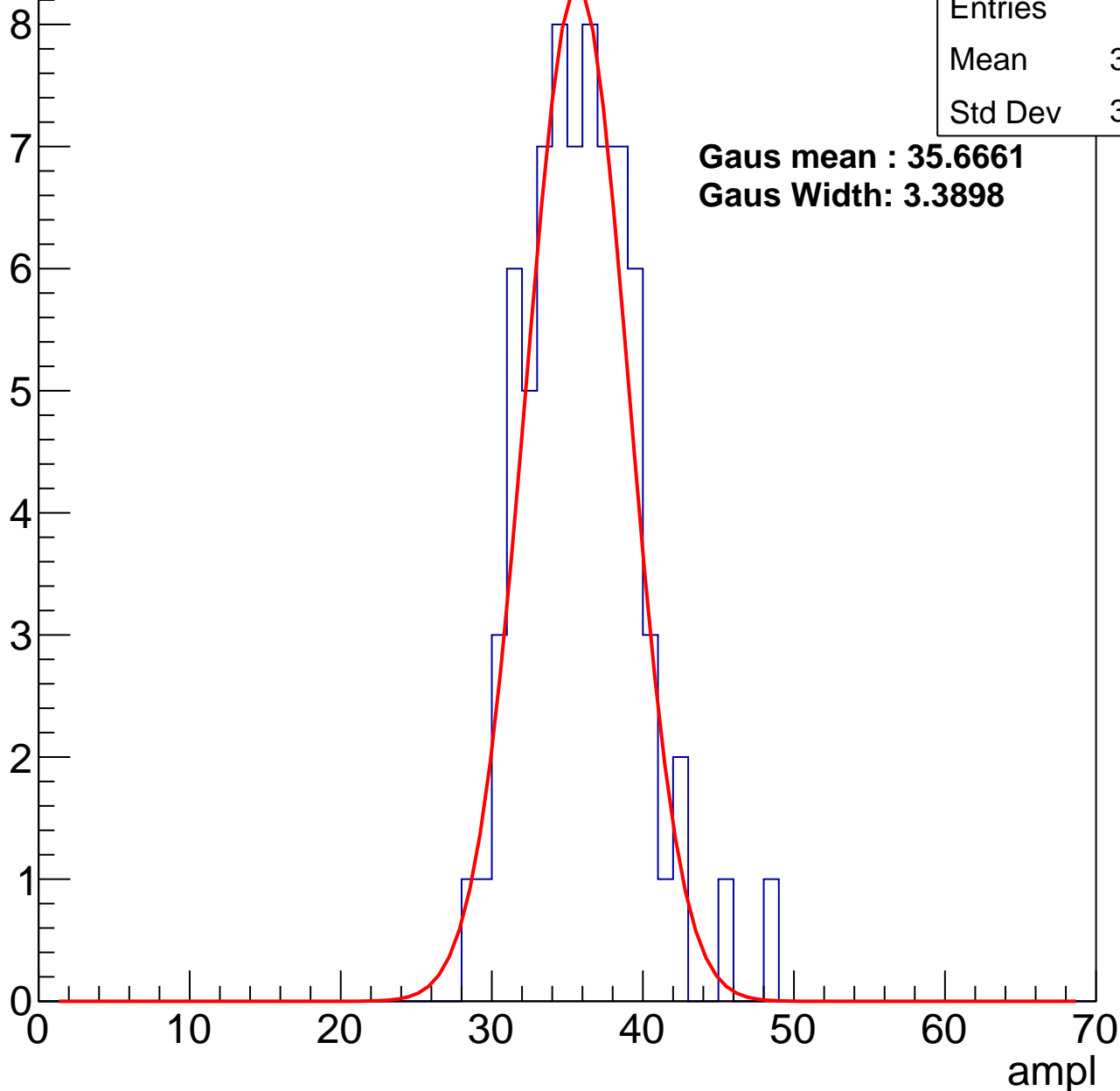
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	74
Mean	35.49
Std Dev	3.662

**Gaus mean : 35.6661**

**Gaus Width: 3.3898**



# B1L100S, U6-ch20, adc2

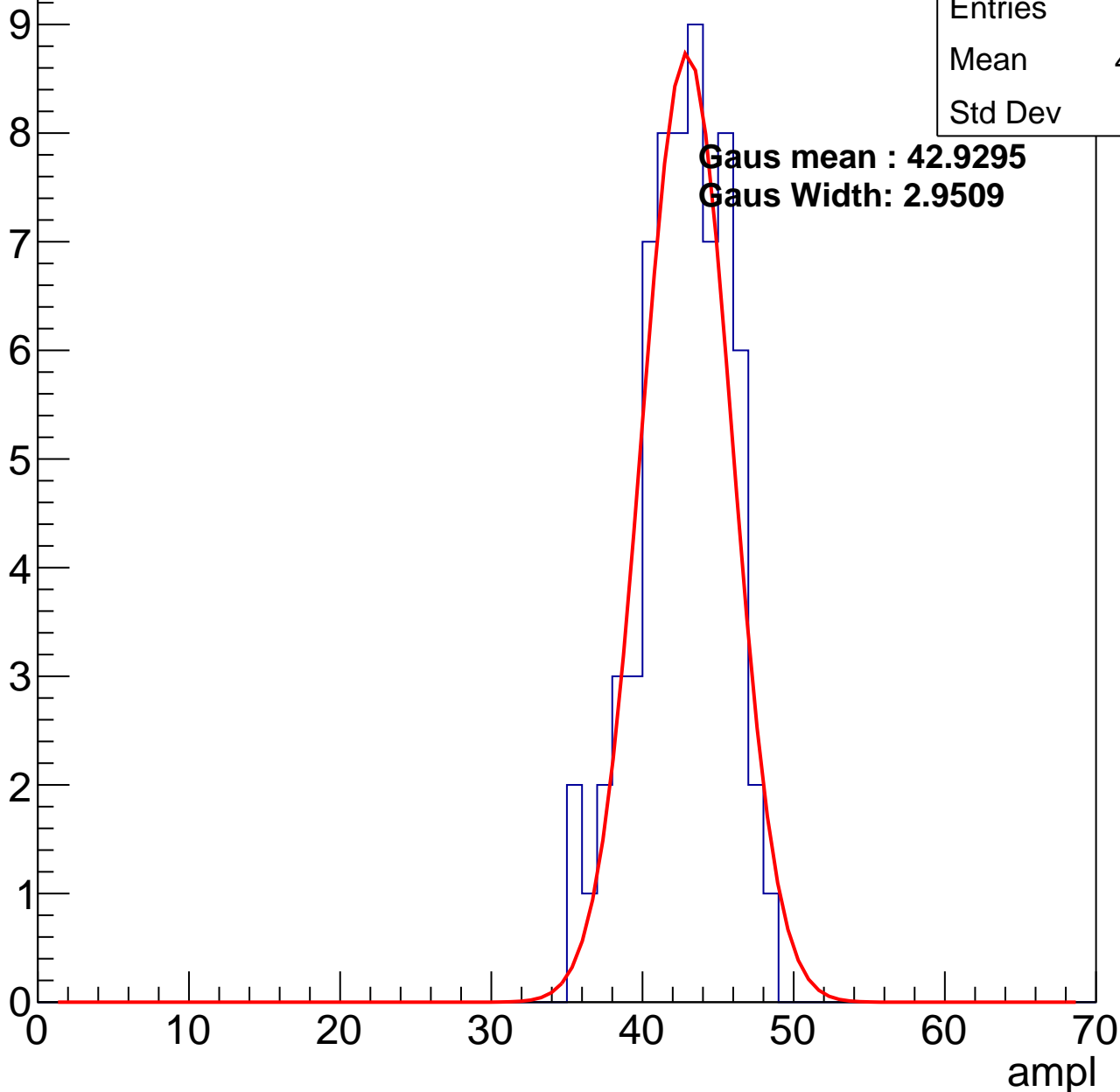
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	67
Mean	42.21
Std Dev	2.95

**Gaus mean : 42.9295**

**Gaus Width: 2.9509**

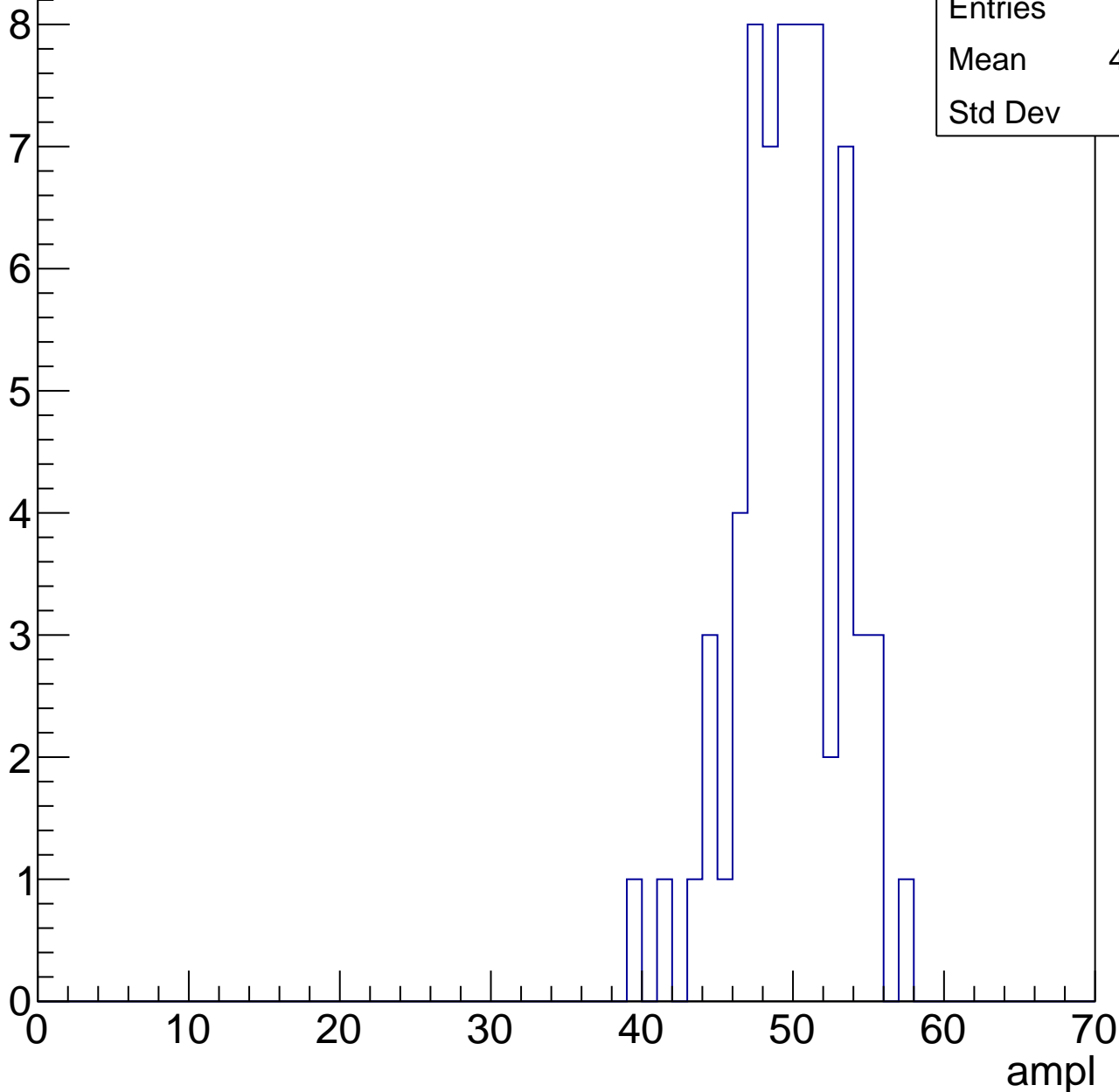


# B1L100S, U6-ch20, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	66
Mean	49.32
Std Dev	3.43

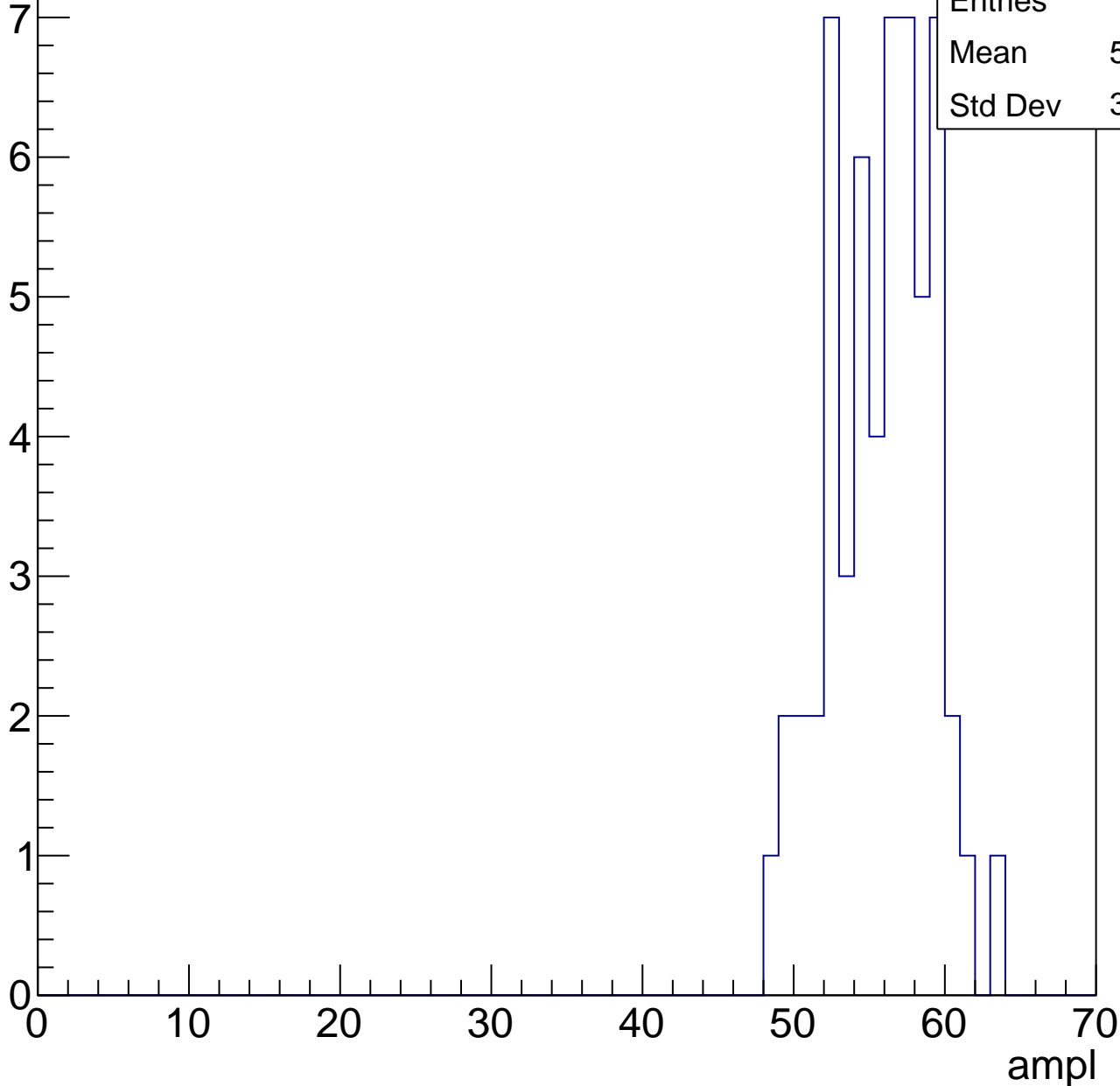


# B1L100S, U6-ch20, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	57
Mean	55.32
Std Dev	3.299



# B1L100S, U6-ch20, adc5

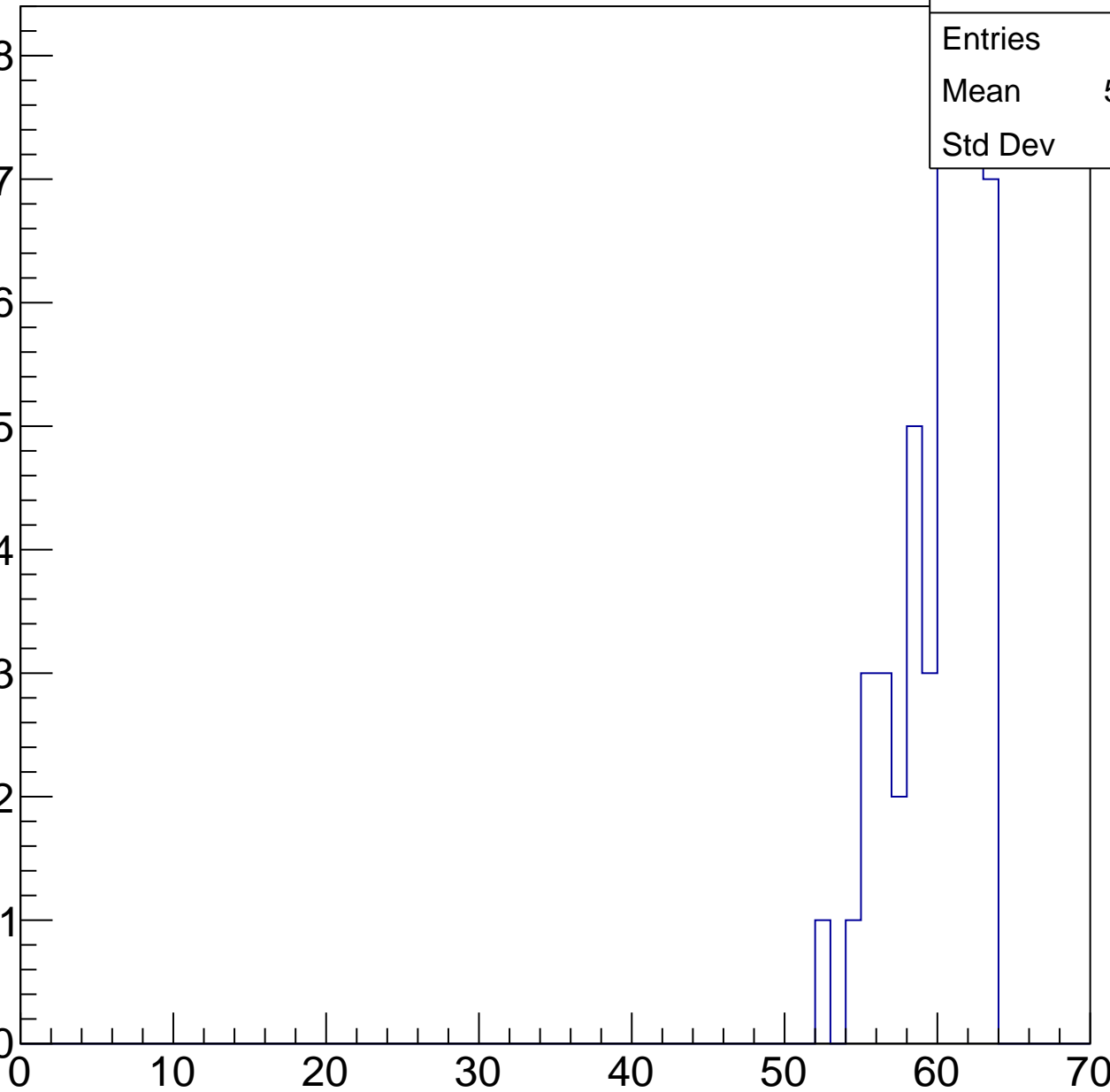
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	49
Mean	59.69
Std Dev	2.72

ampl



# B1L100S, U6-ch20, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry





# B1L100S, U6-ch20, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



# B1L100S, U6-ch21, adc0

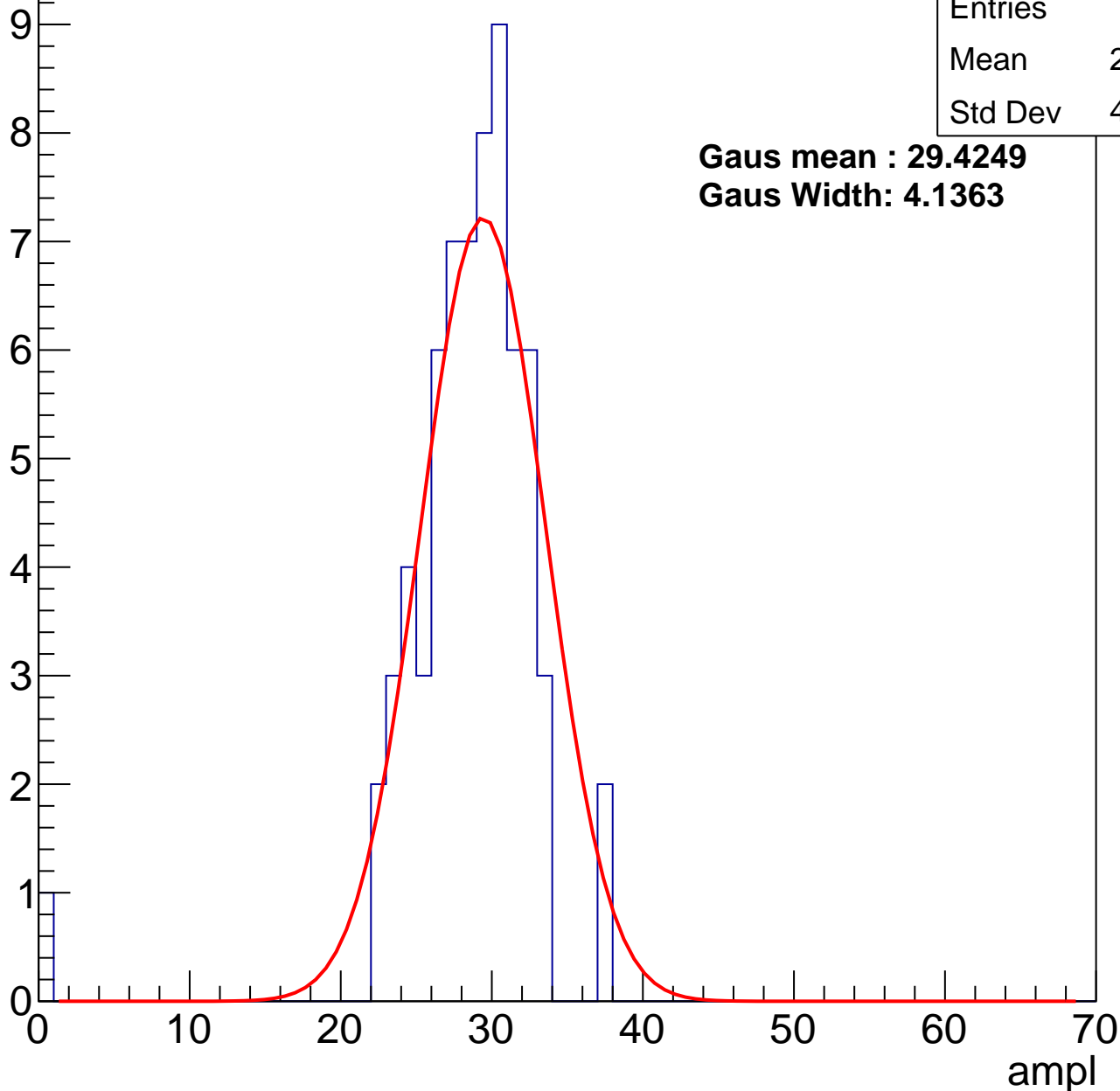
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	67
Mean	28.03
Std Dev	4.706

**Gaus mean : 29.4249**

**Gaus Width: 4.1363**



# B1L100S, U6-ch21, adc1

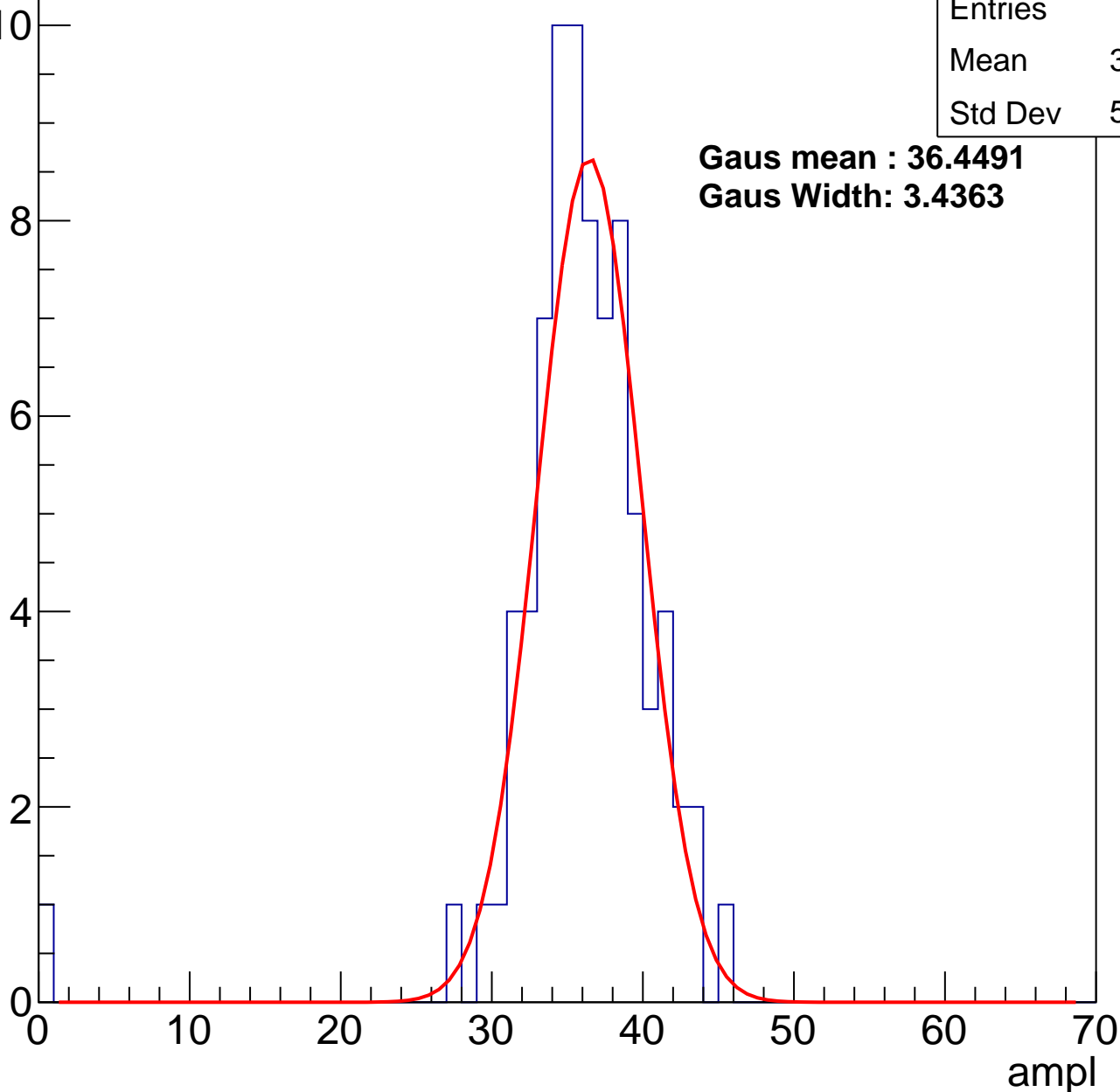
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	79
Mean	35.49
Std Dev	5.279

**Gaus mean : 36.4491**

**Gaus Width: 3.4363**

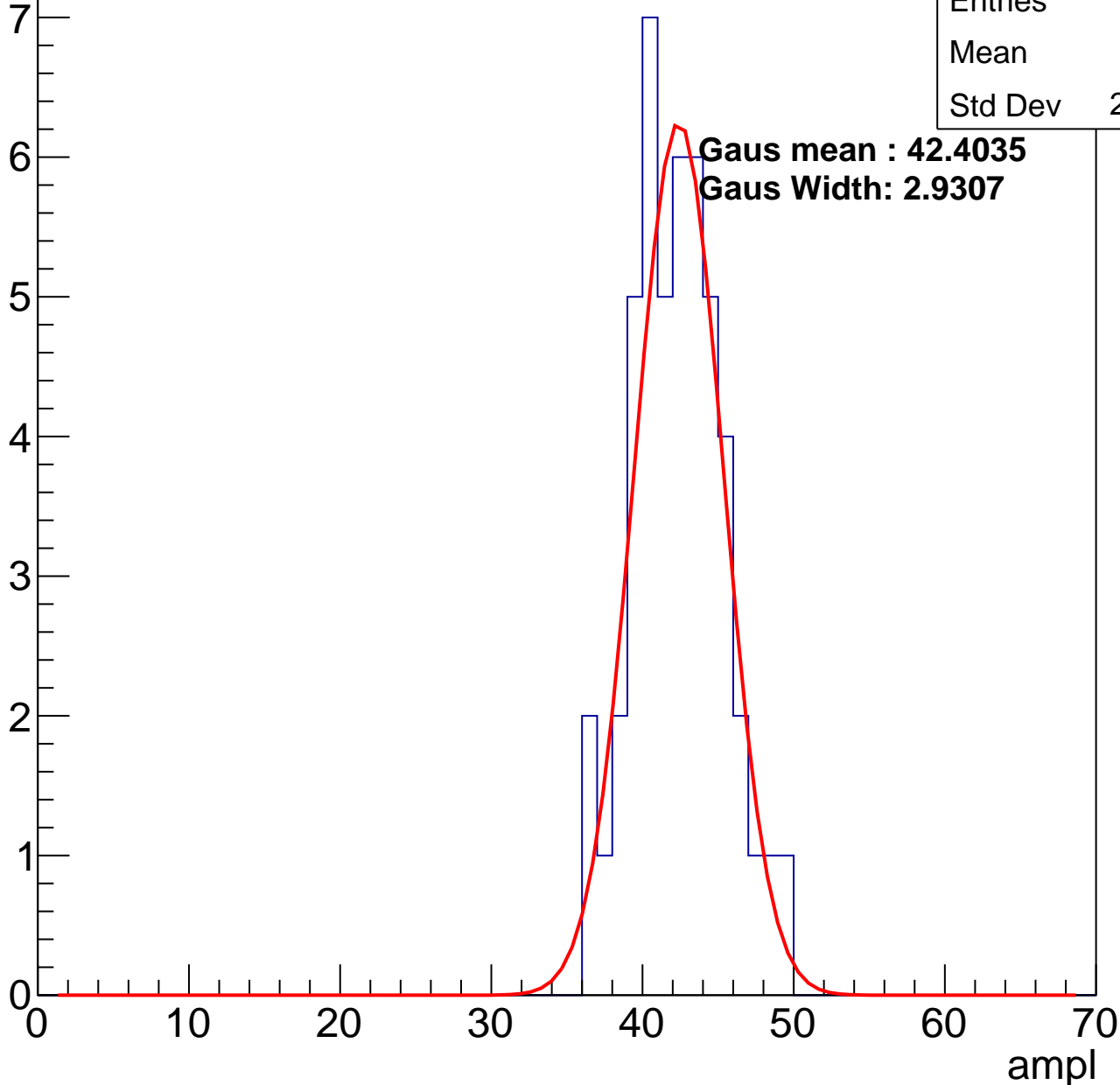


# B1L100S, U6-ch21, adc2

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

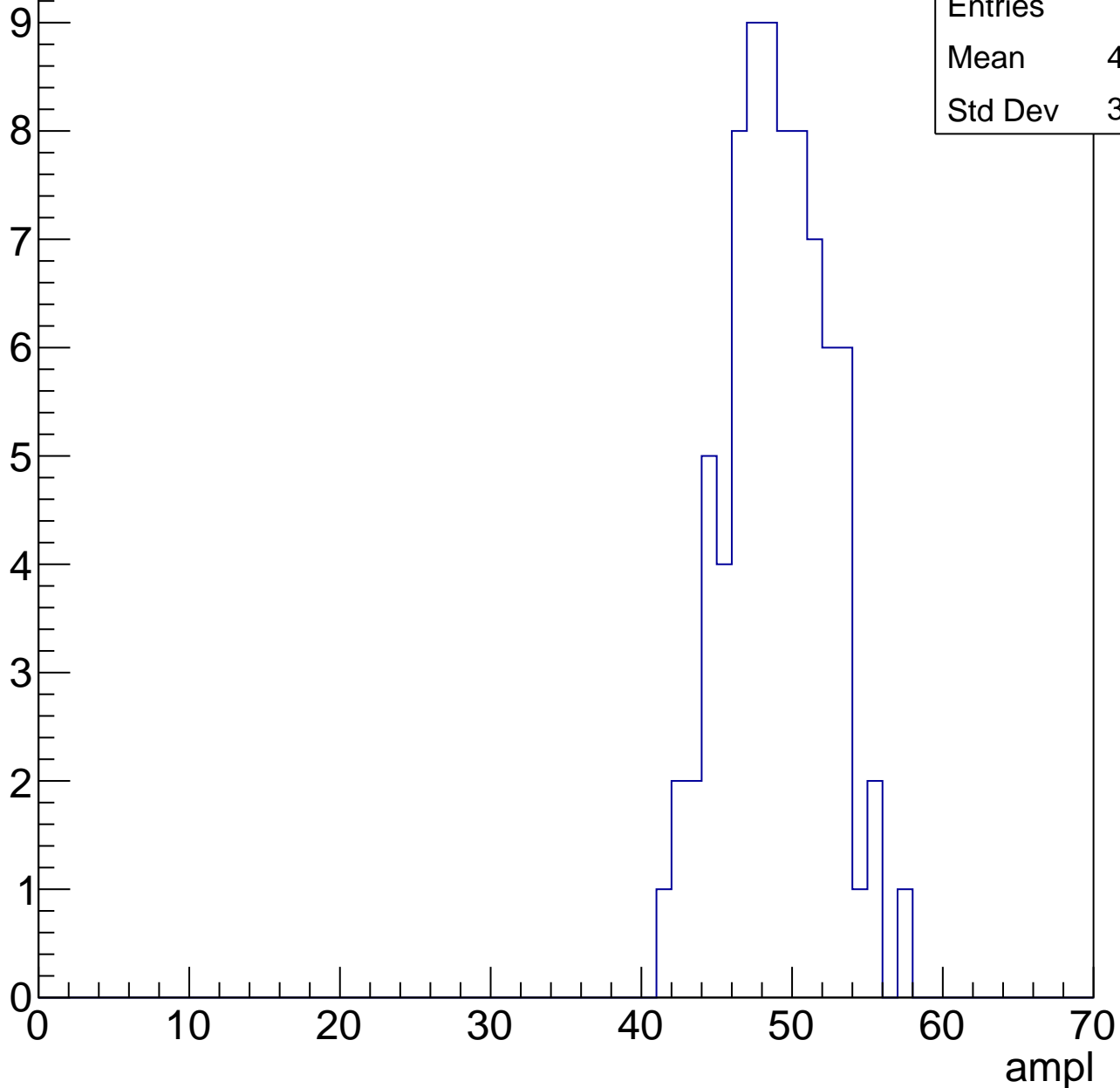
Entries	48
Mean	41.9
Std Dev	2.924



# B1L100S, U6-ch21, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



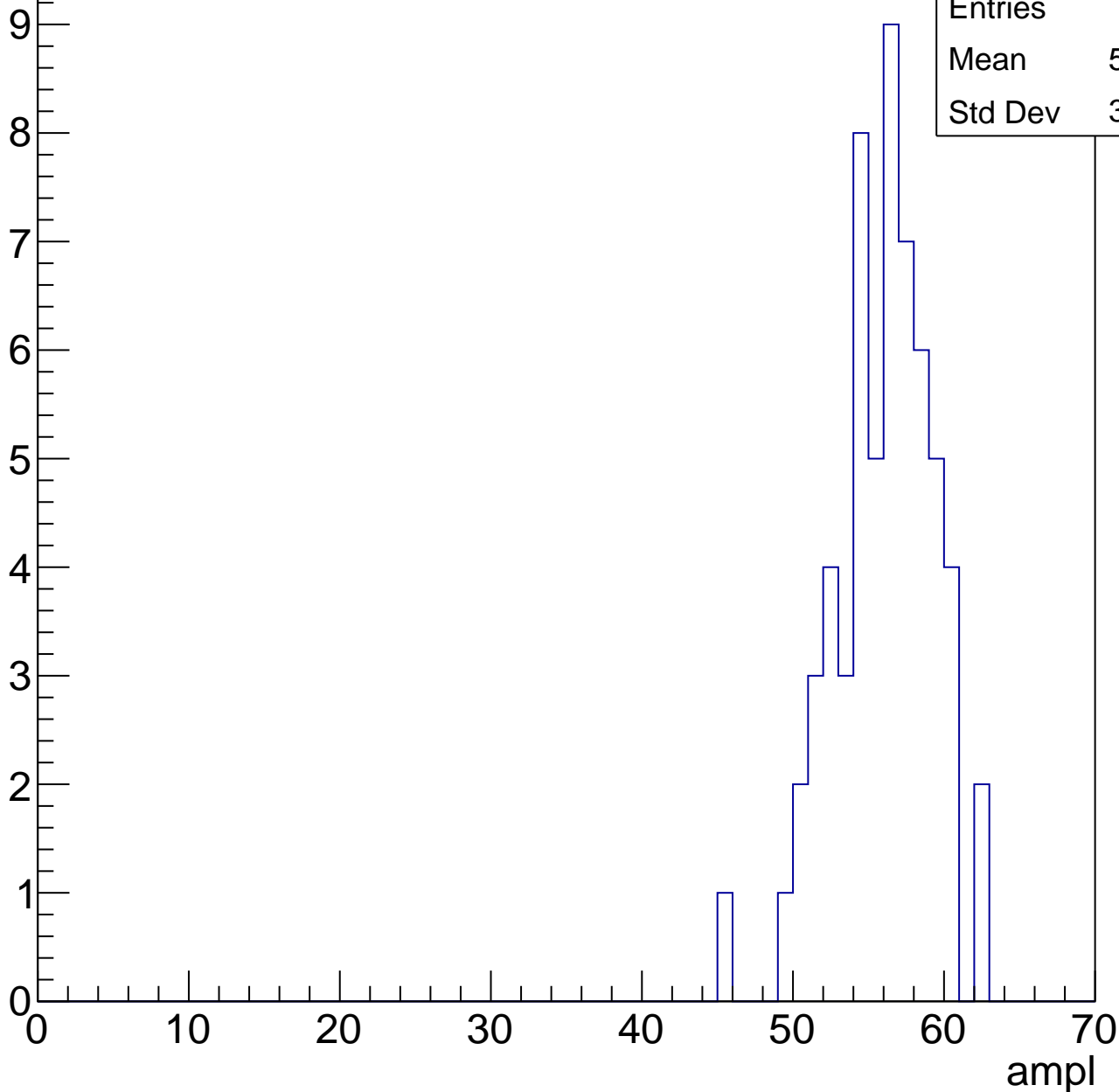
Entries	79
Mean	48.53
Std Dev	3.318

# B1L100S, U6-ch21, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	60
Mean	55.52
Std Dev	3.274



# B1L100S, U6-ch21, adc5

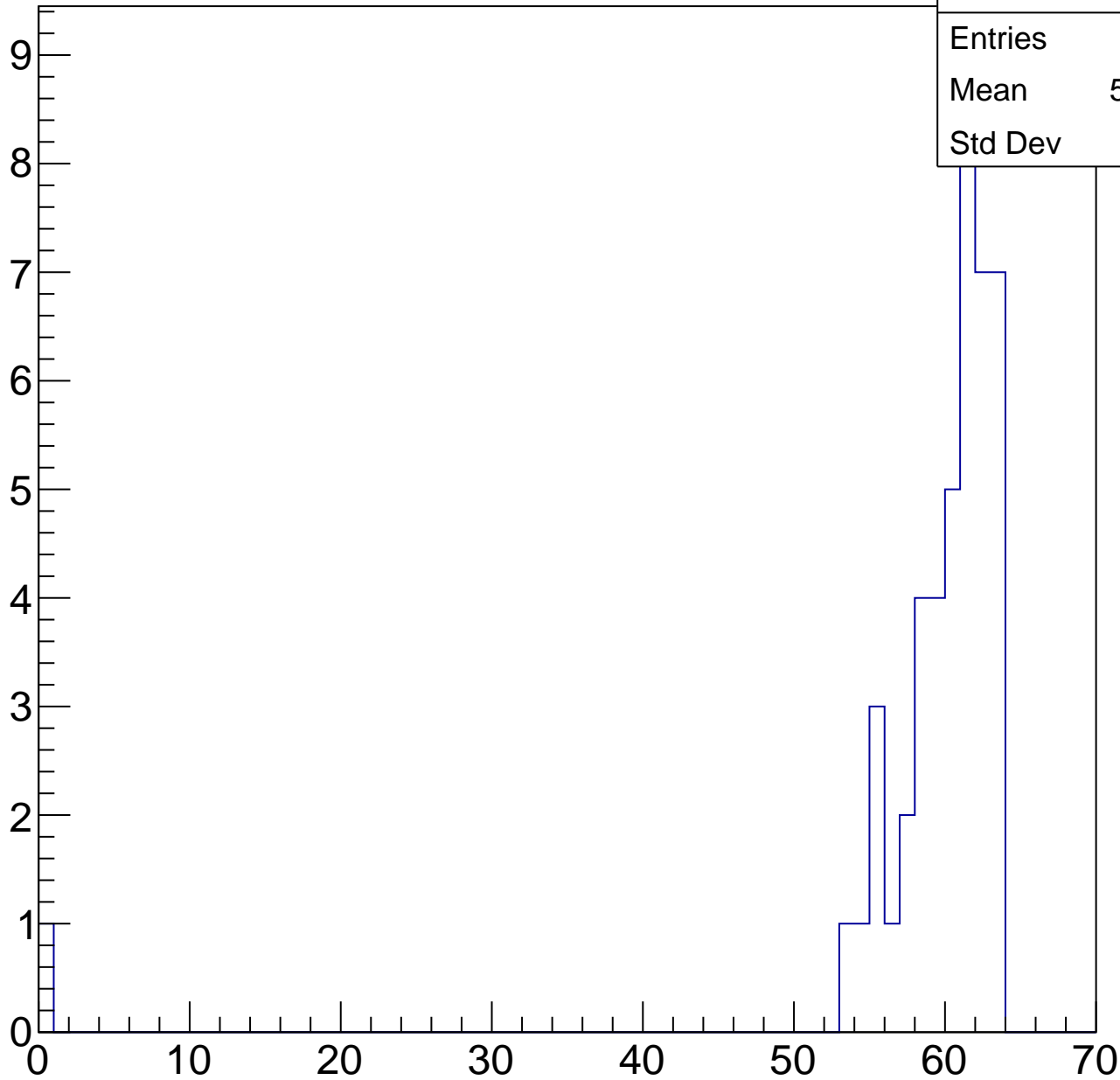
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	45
Mean	58.53
Std Dev	9.21

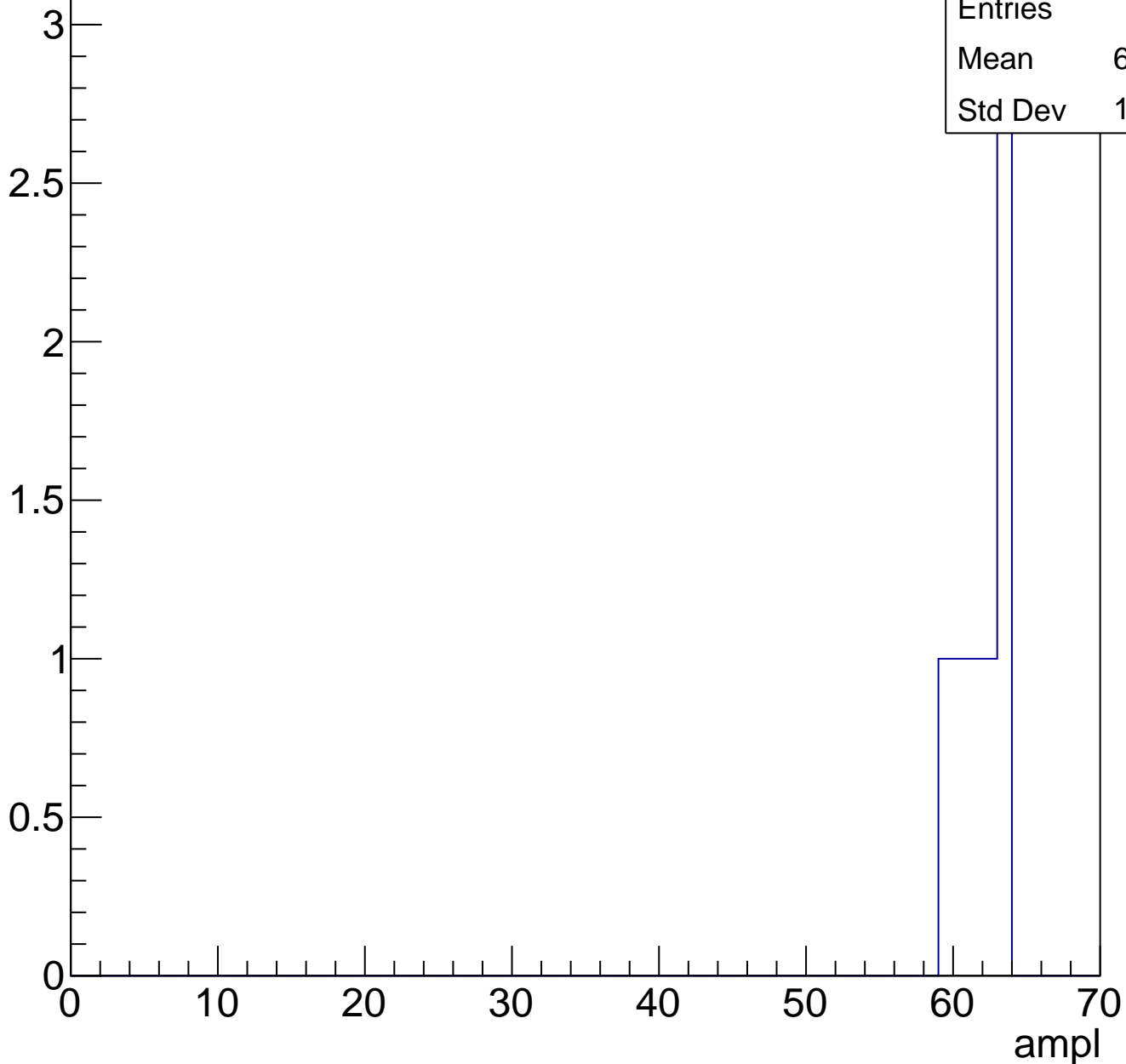
ampl



# B1L100S, U6-ch21, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry





# B1L100S, U6-ch21, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	2
Mean	11
Std Dev	11

# B1L100S, U6-ch22, adc0

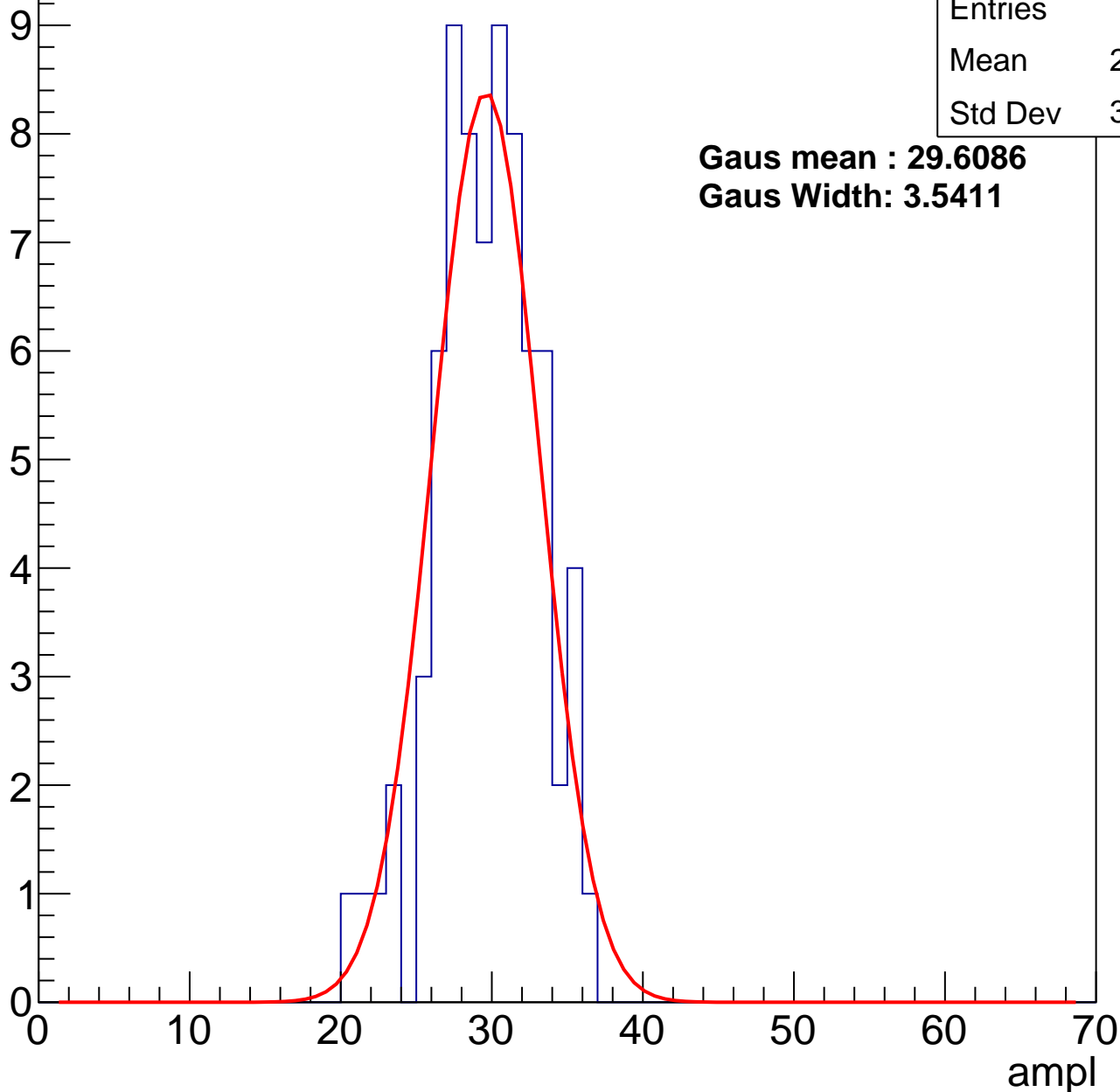
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	74
Mean	29.22
Std Dev	3.374

**Gaus mean : 29.6086**

**Gaus Width: 3.5411**



# B1L100S, U6-ch22, adc1

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	79
Mean	36.99
Std Dev	3.556

**Gaus mean : 37.4514**

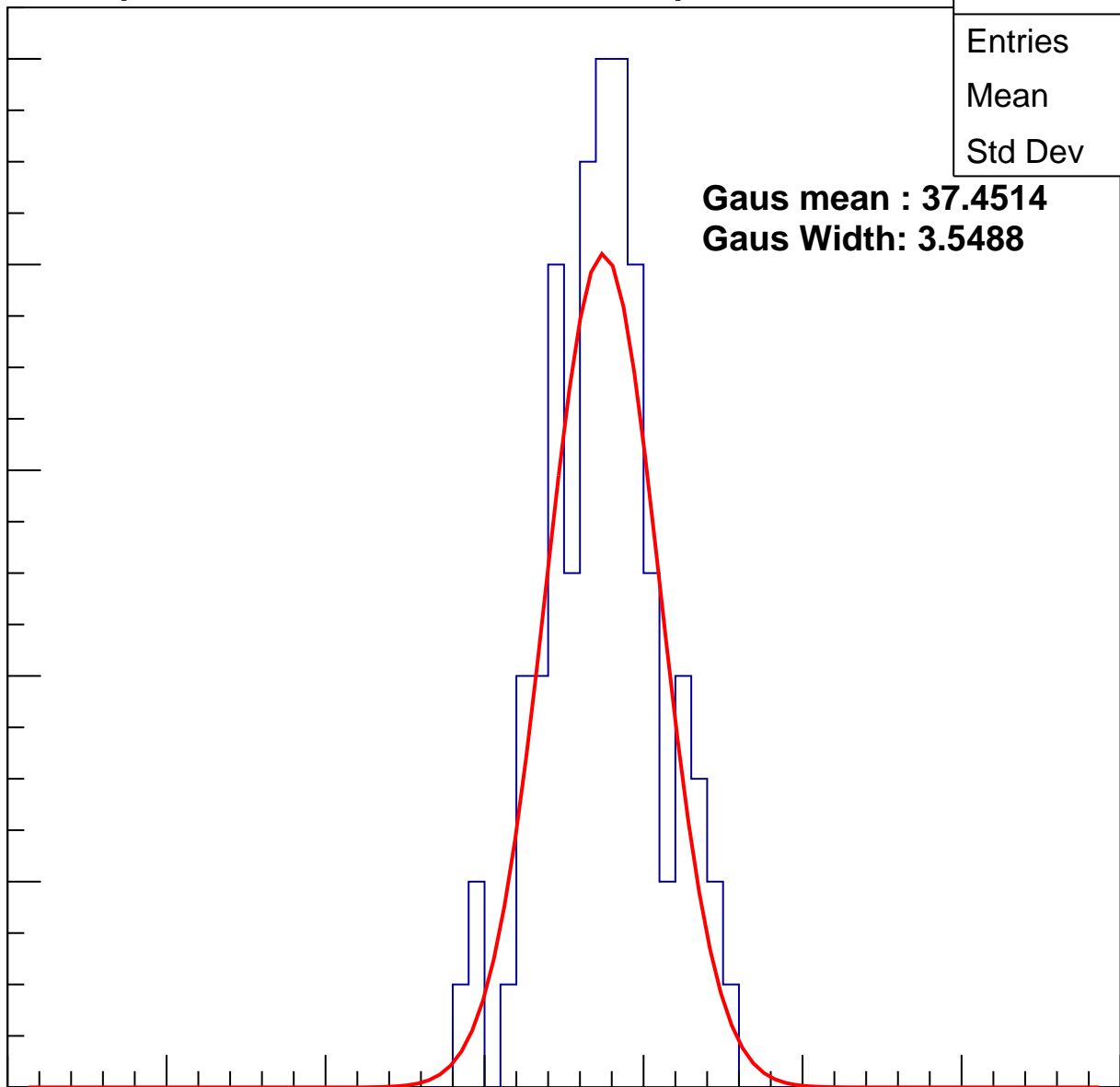
**Gaus Width: 3.5488**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

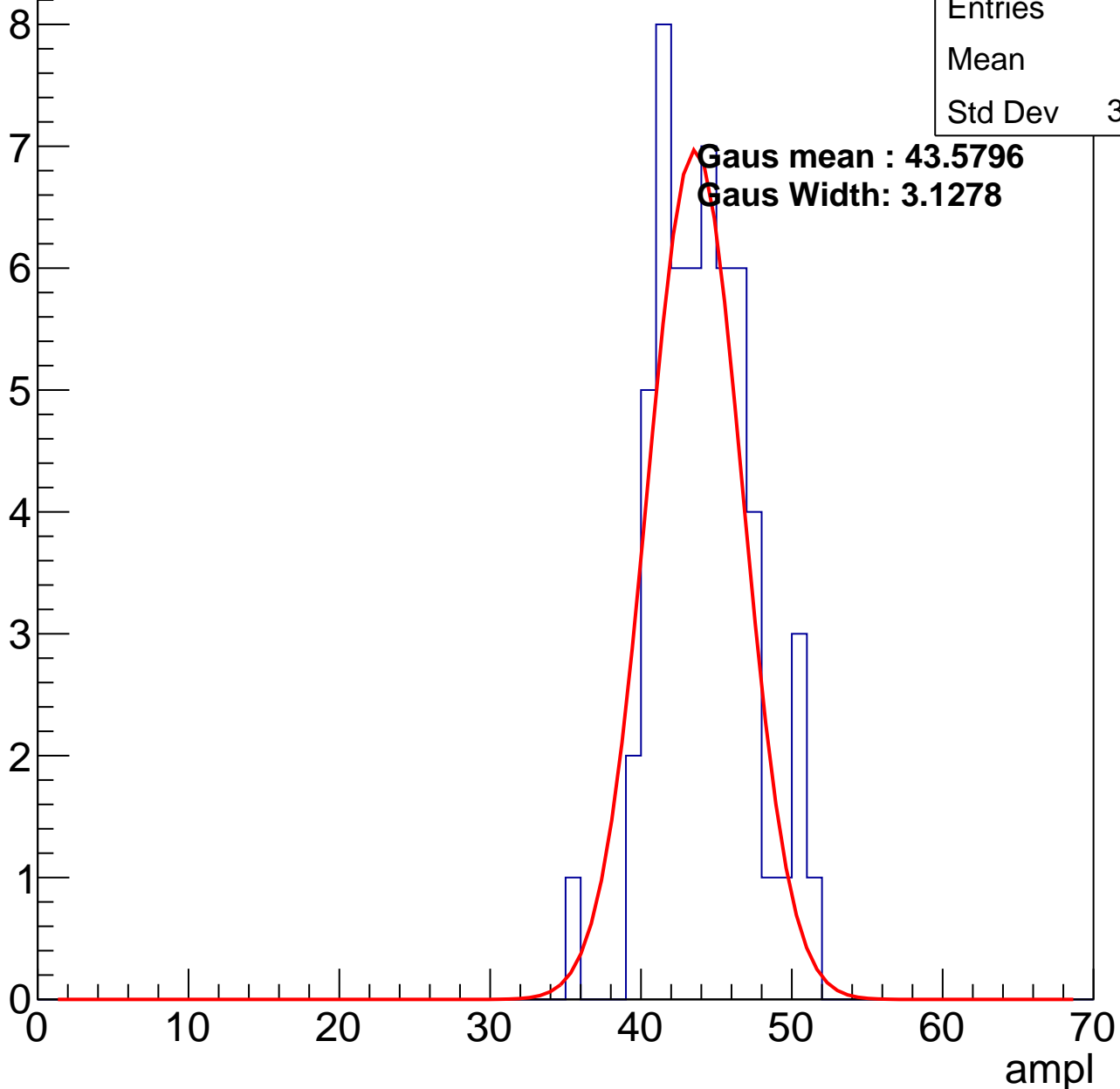


# B1L100S, U6-ch22, adc2

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

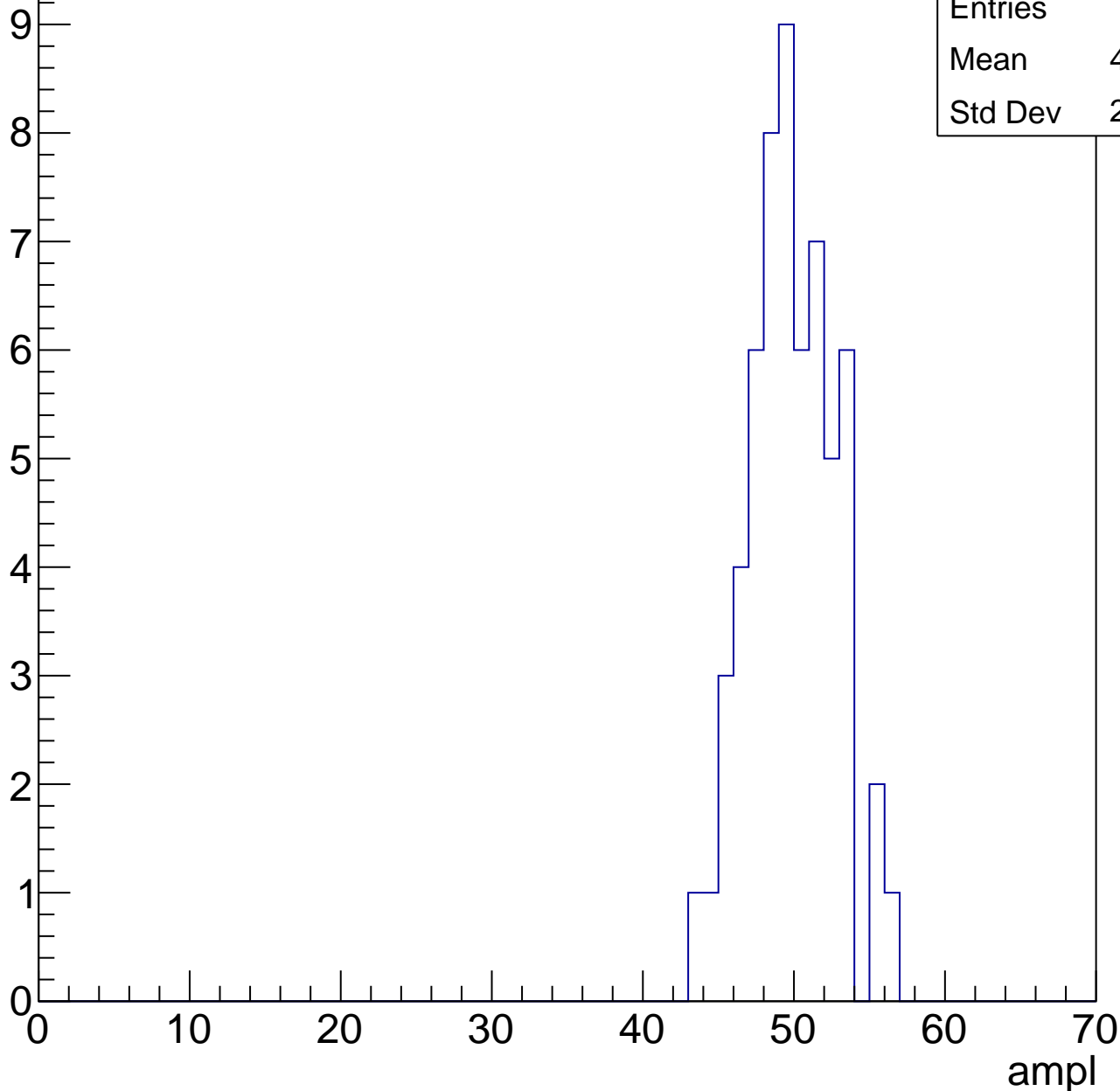
Entries	57
Mean	43.7
Std Dev	3.168



# B1L100S, U6-ch22, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

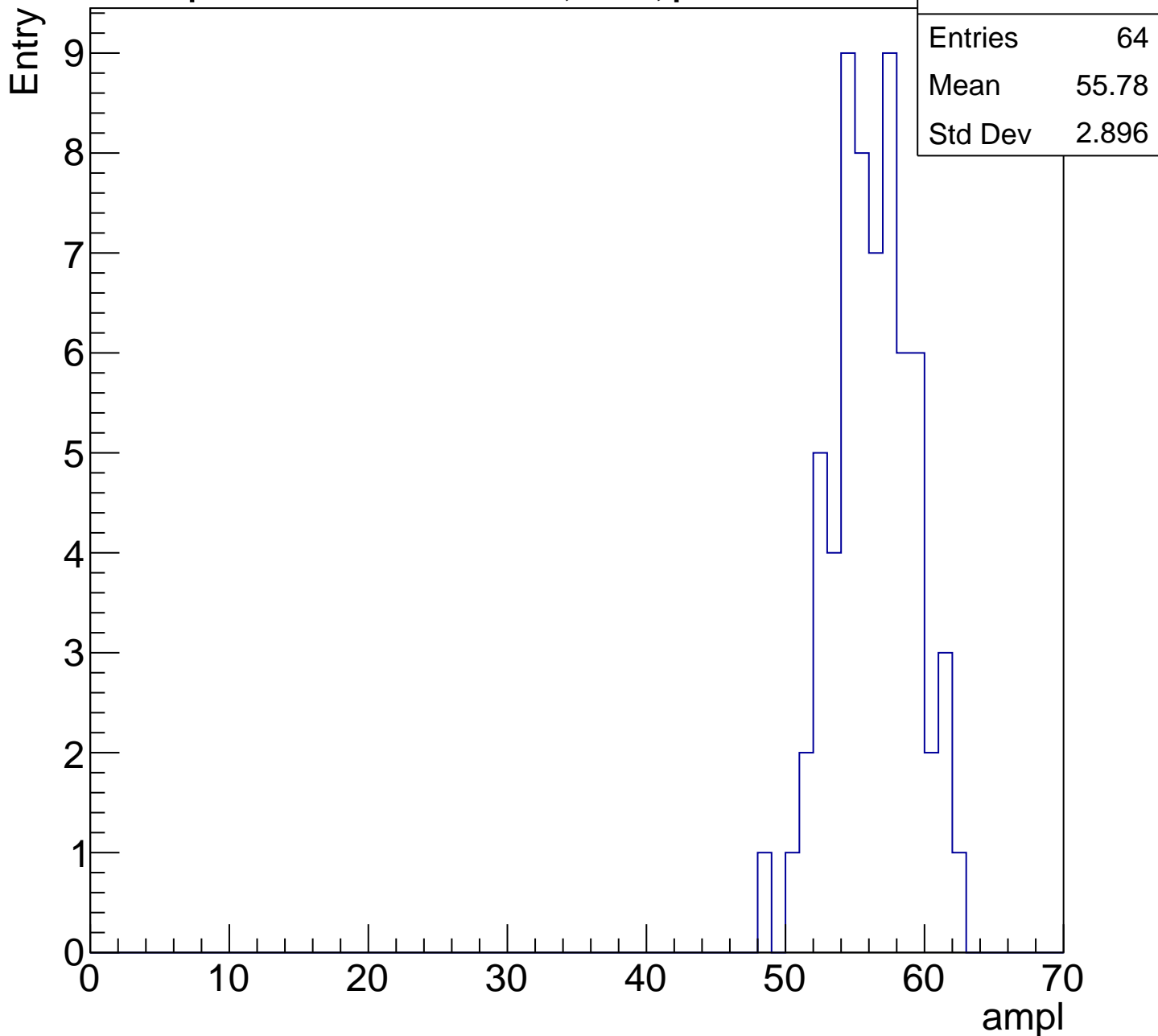
Entry



Entries	59
Mean	49.39
Std Dev	2.804

# B1L100S, U6-ch22, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

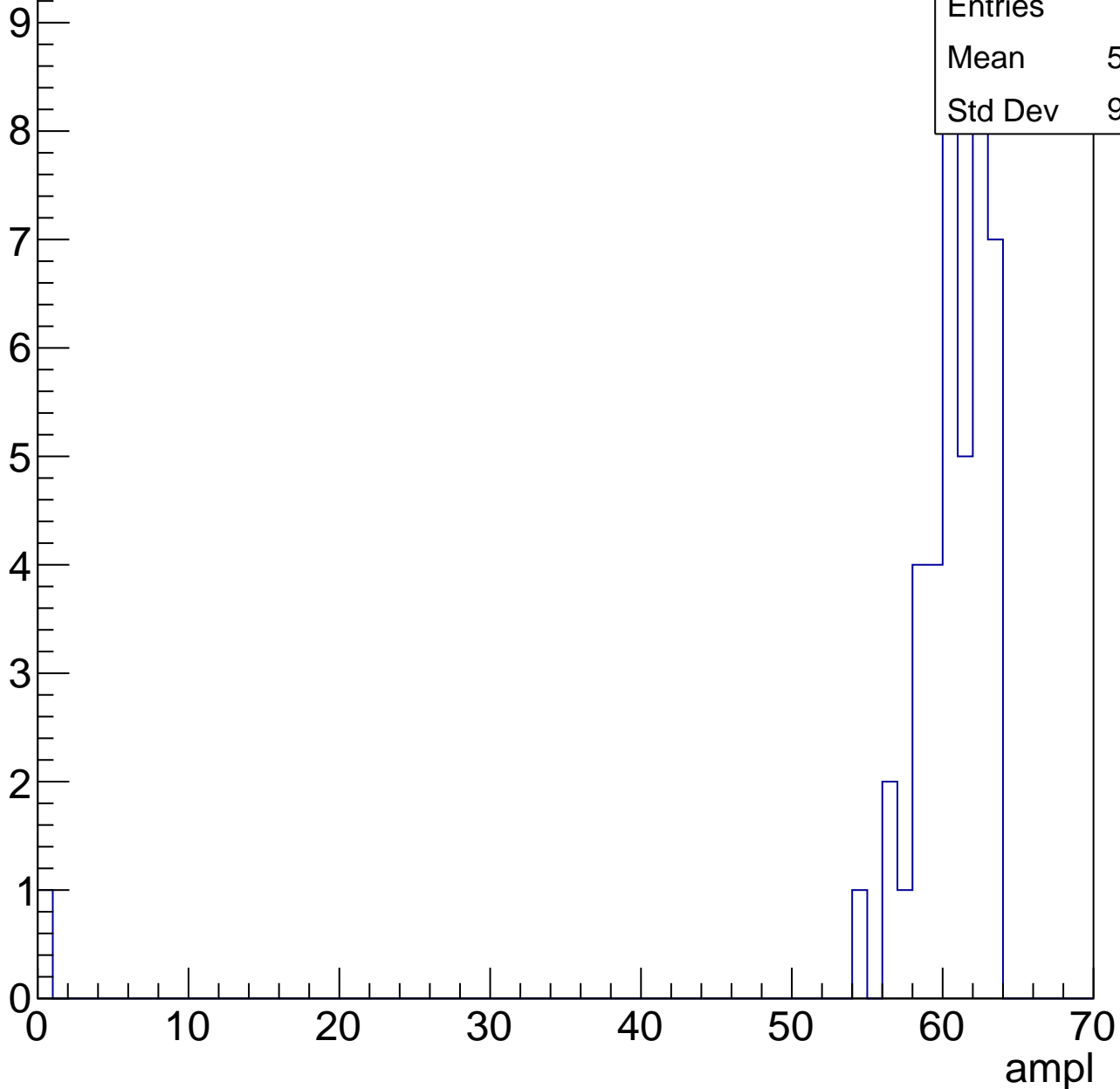


# B1L100S, U6-ch22, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	42
Mean	58.93
Std Dev	9.453



# B1L100S, U6-ch22, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry





# B1L100S, U6-ch22, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



# B1L100S, U6-ch23, adc0

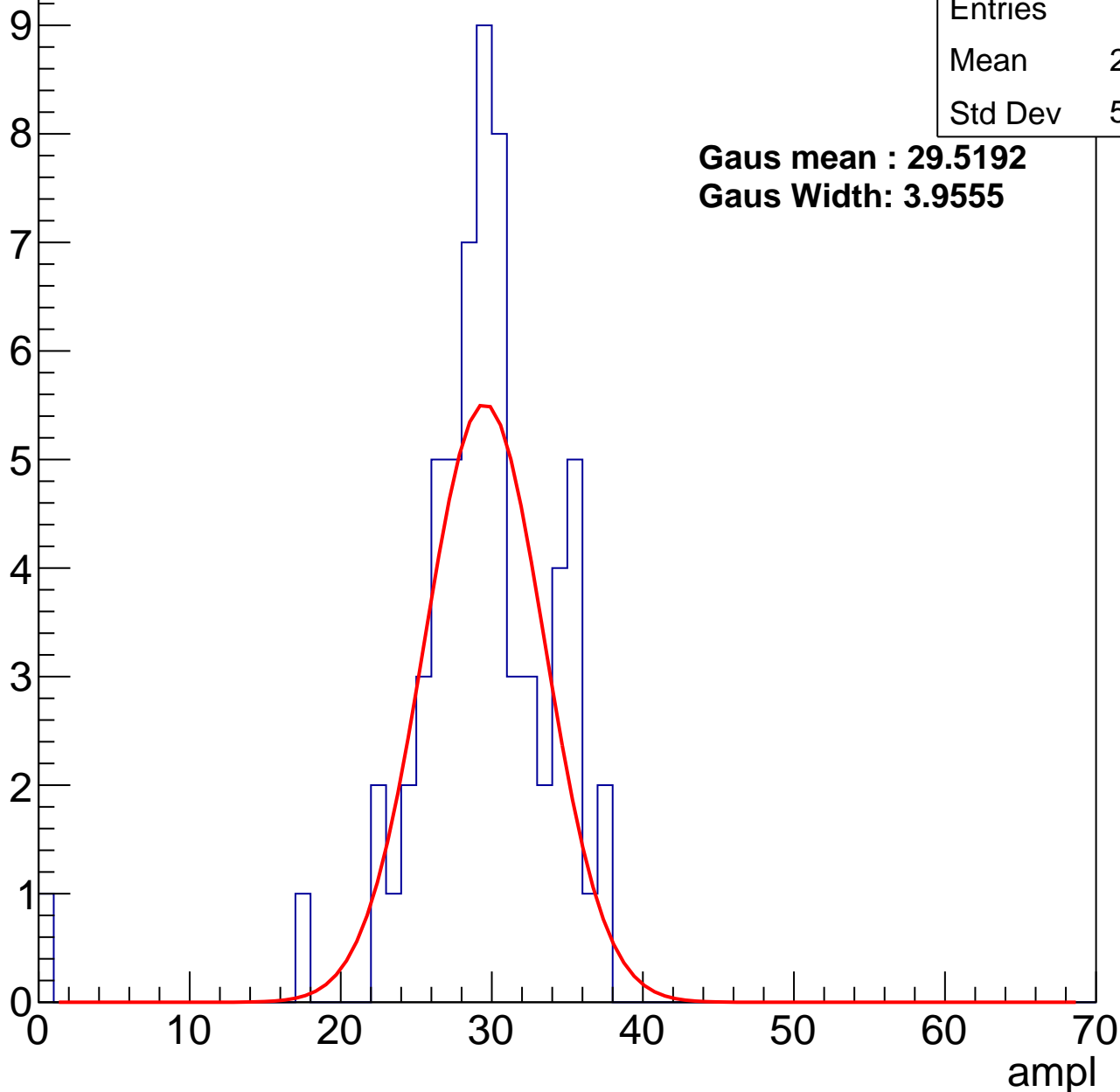
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	64
Mean	28.83
Std Dev	5.337

**Gaus mean : 29.5192**

**Gaus Width: 3.9555**



# B1L100S, U6-ch23, adc1

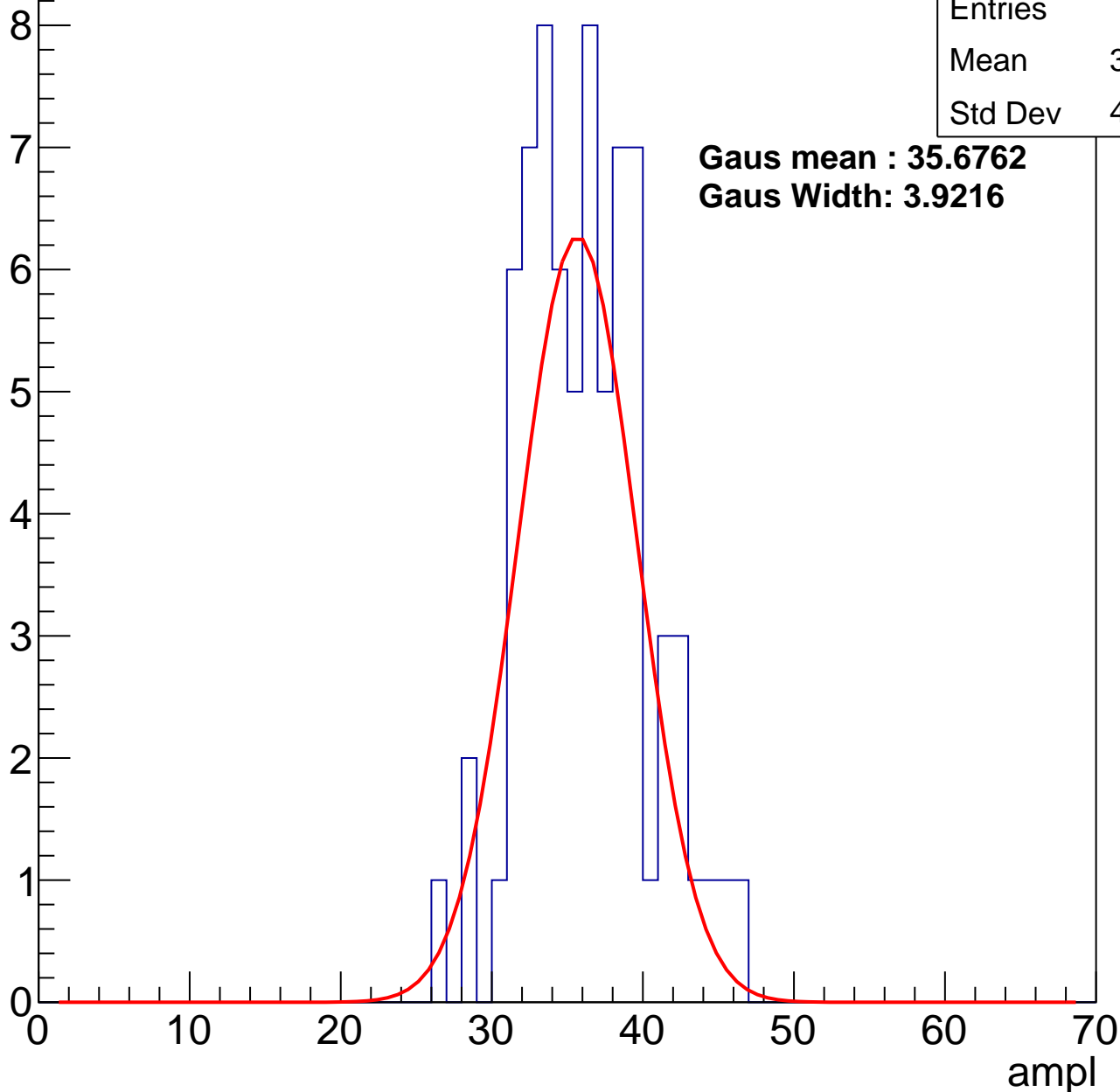
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	74
Mean	35.73
Std Dev	4.045

**Gaus mean : 35.6762**

**Gaus Width: 3.9216**



# B1L100S, U6-ch23, adc2

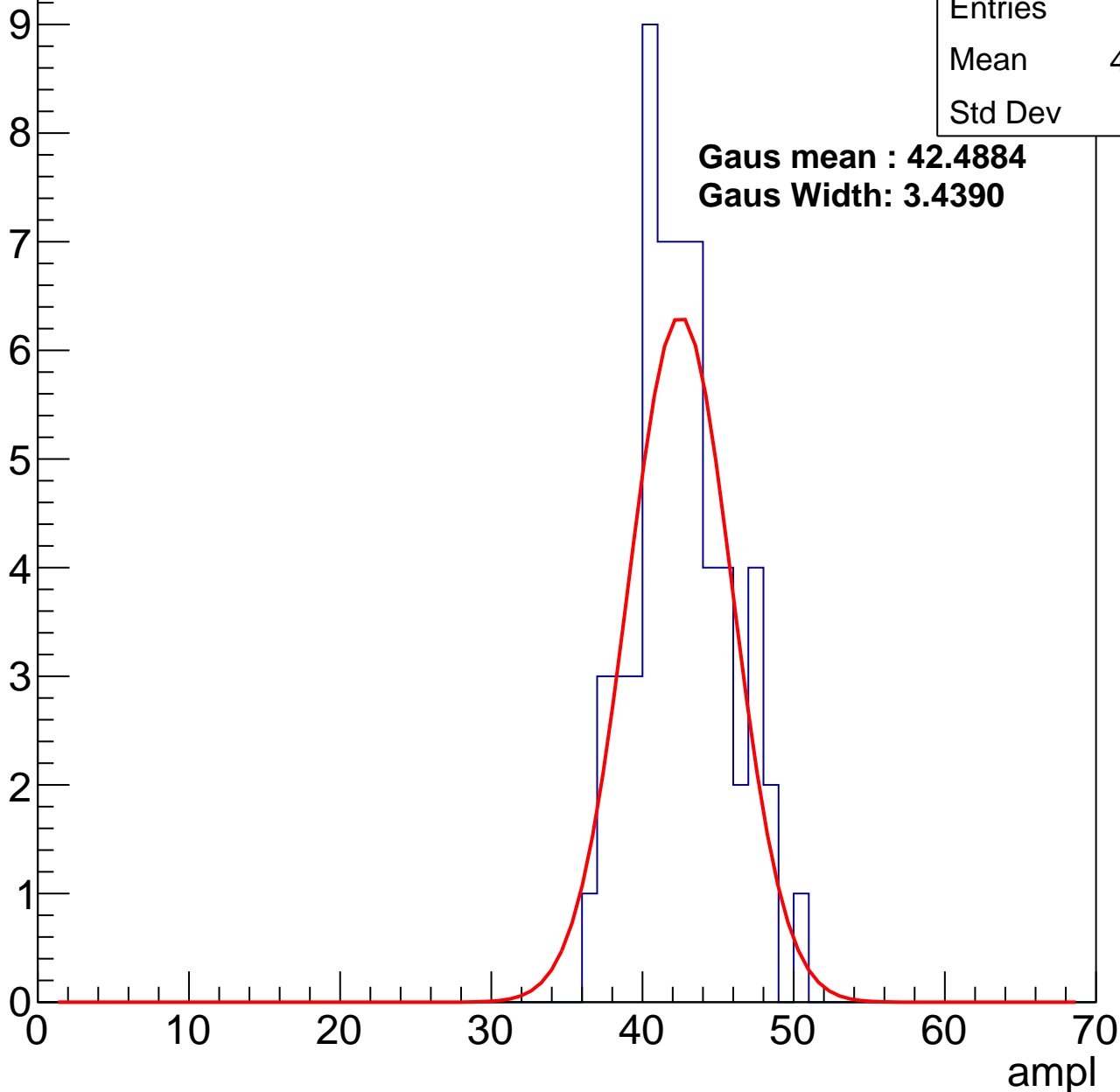
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	57
Mean	42.14
Std Dev	3.12

**Gaus mean : 42.4884**

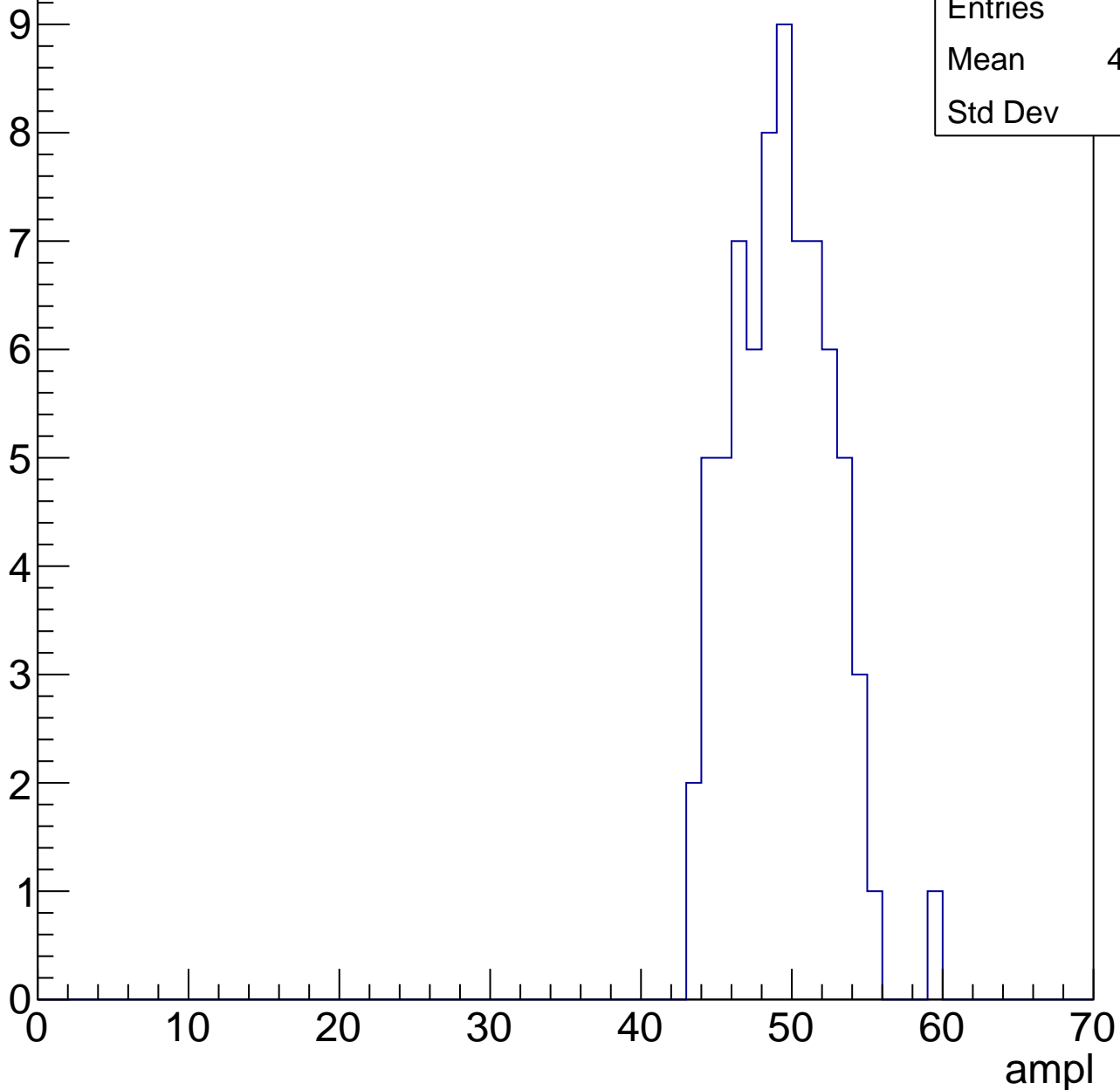
**Gaus Width: 3.4390**



# B1L100S, U6-ch23, adc3

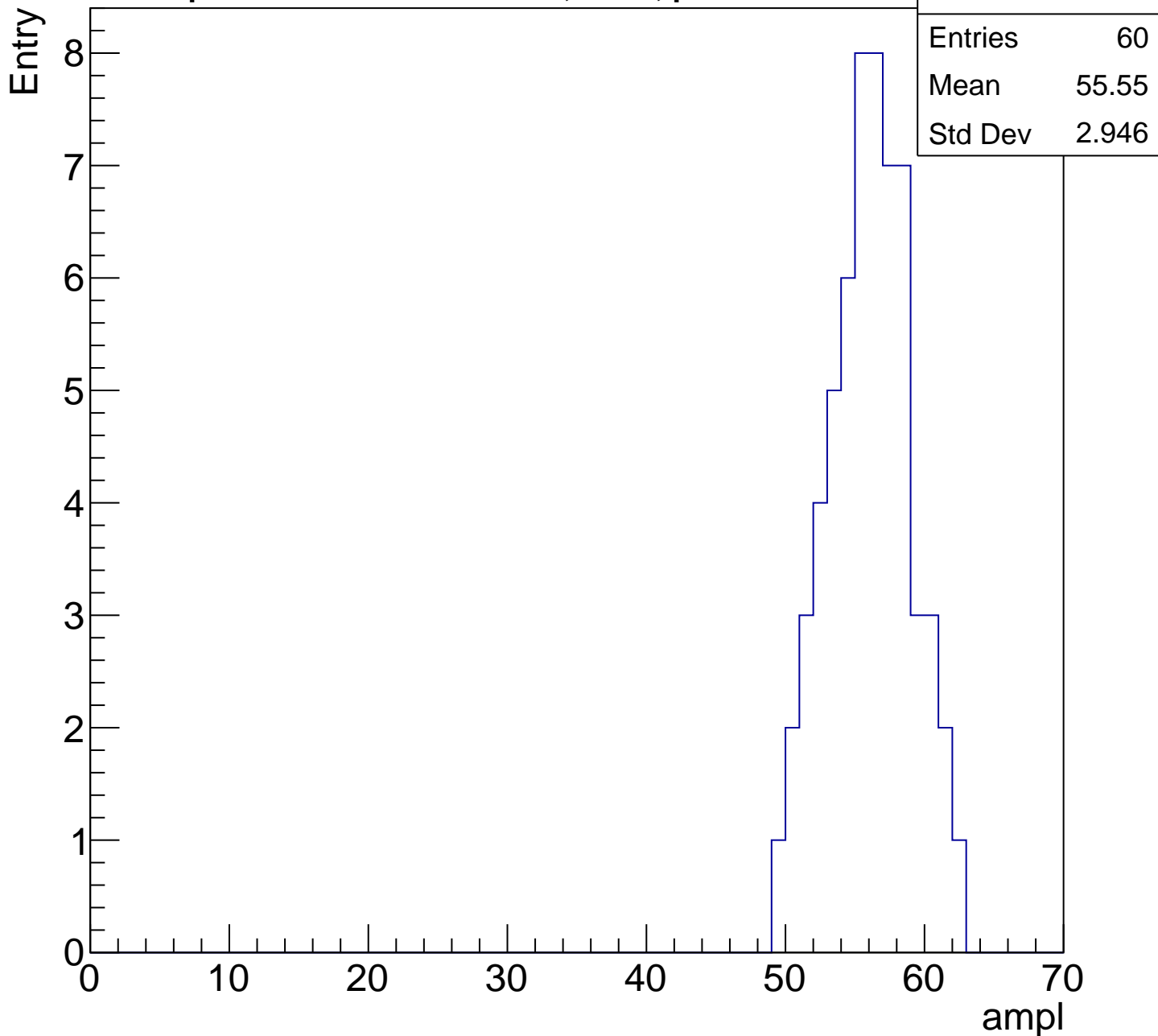
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



# B1L100S, U6-ch23, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2



# B1L100S, U6-ch23, adc5

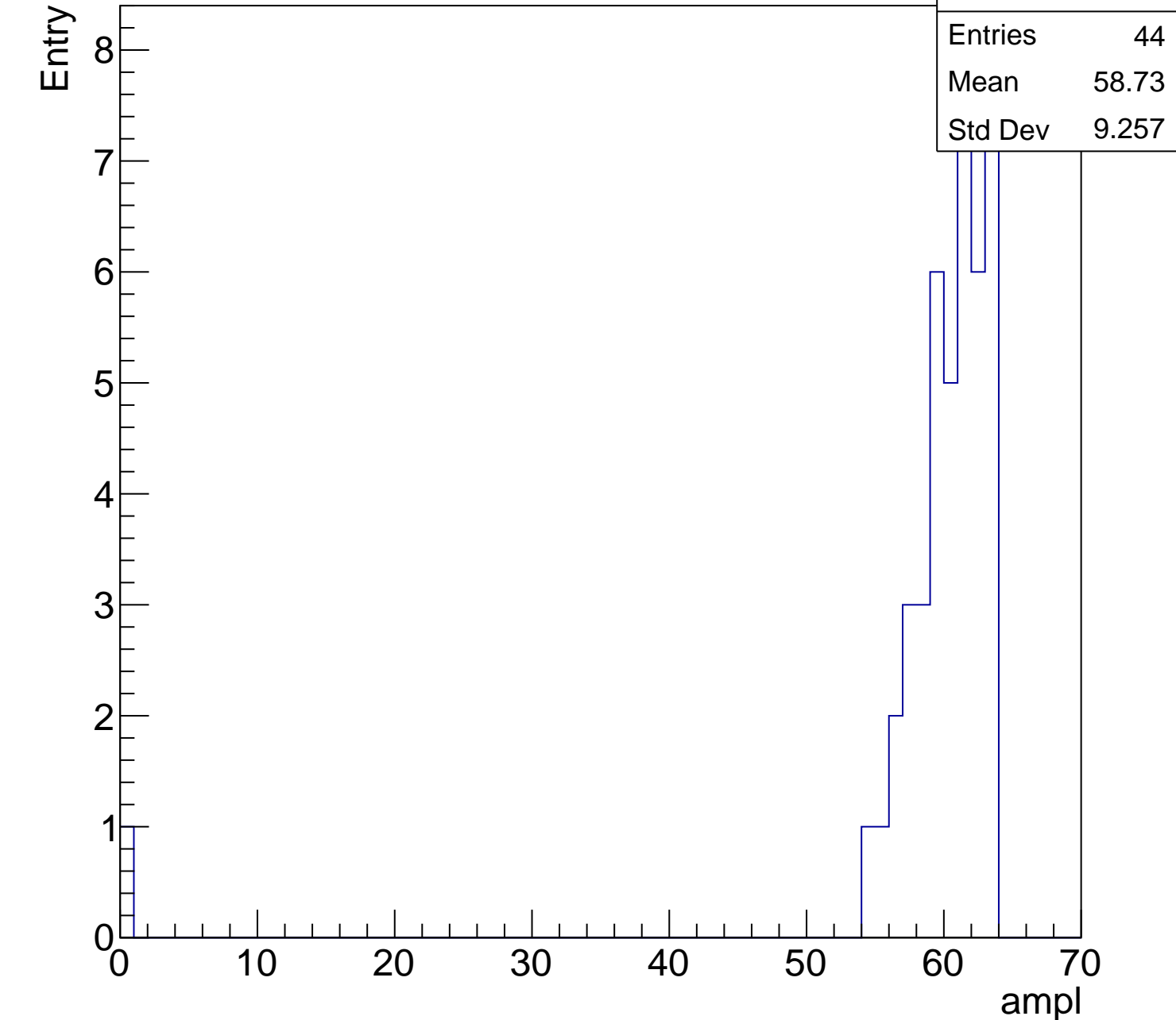
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	44
Mean	58.73
Std Dev	9.257

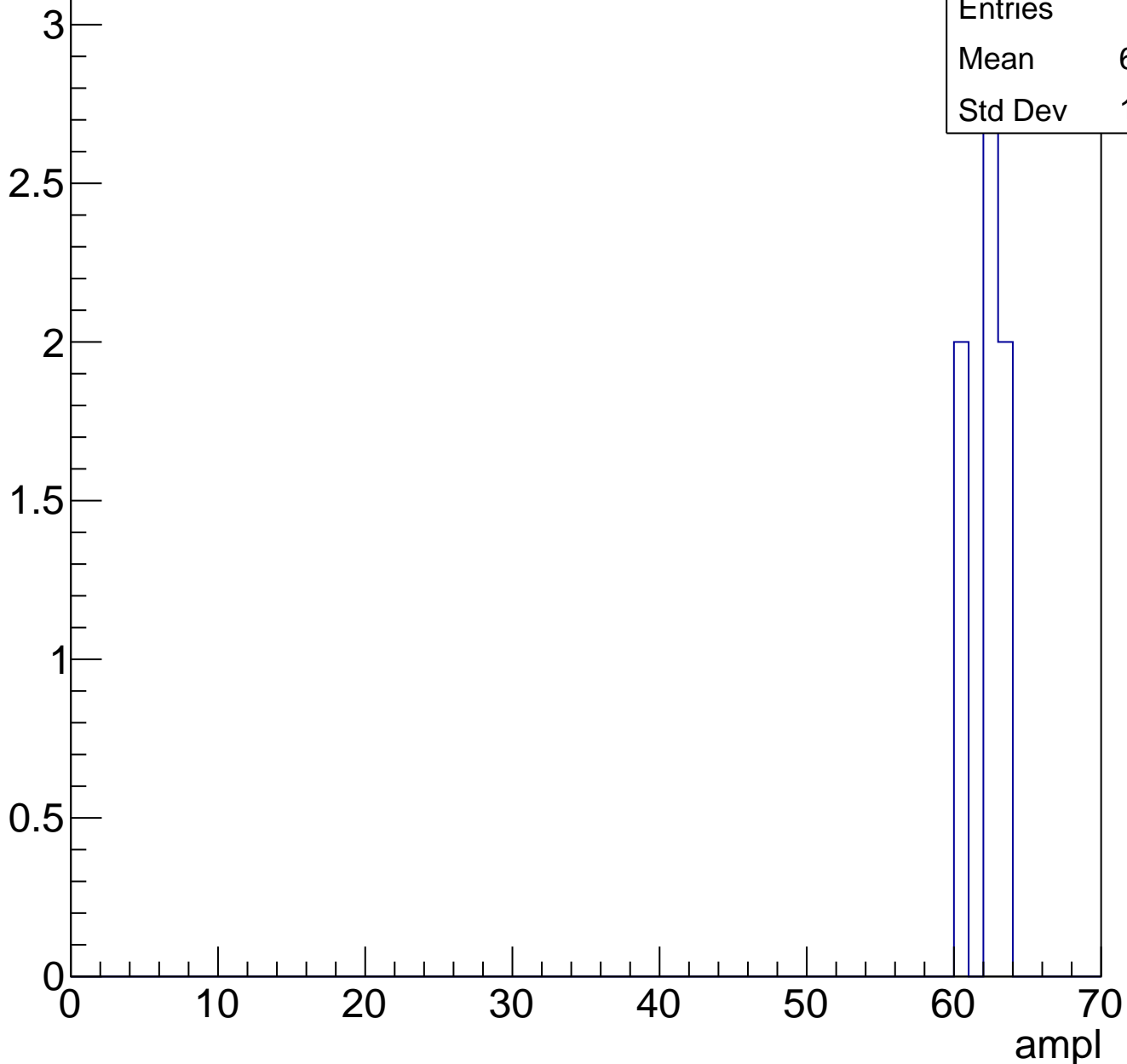
ampl



# B1L100S, U6-ch23, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry





# B1L100S, U6-ch23, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L100S, U6-ch24, adc0

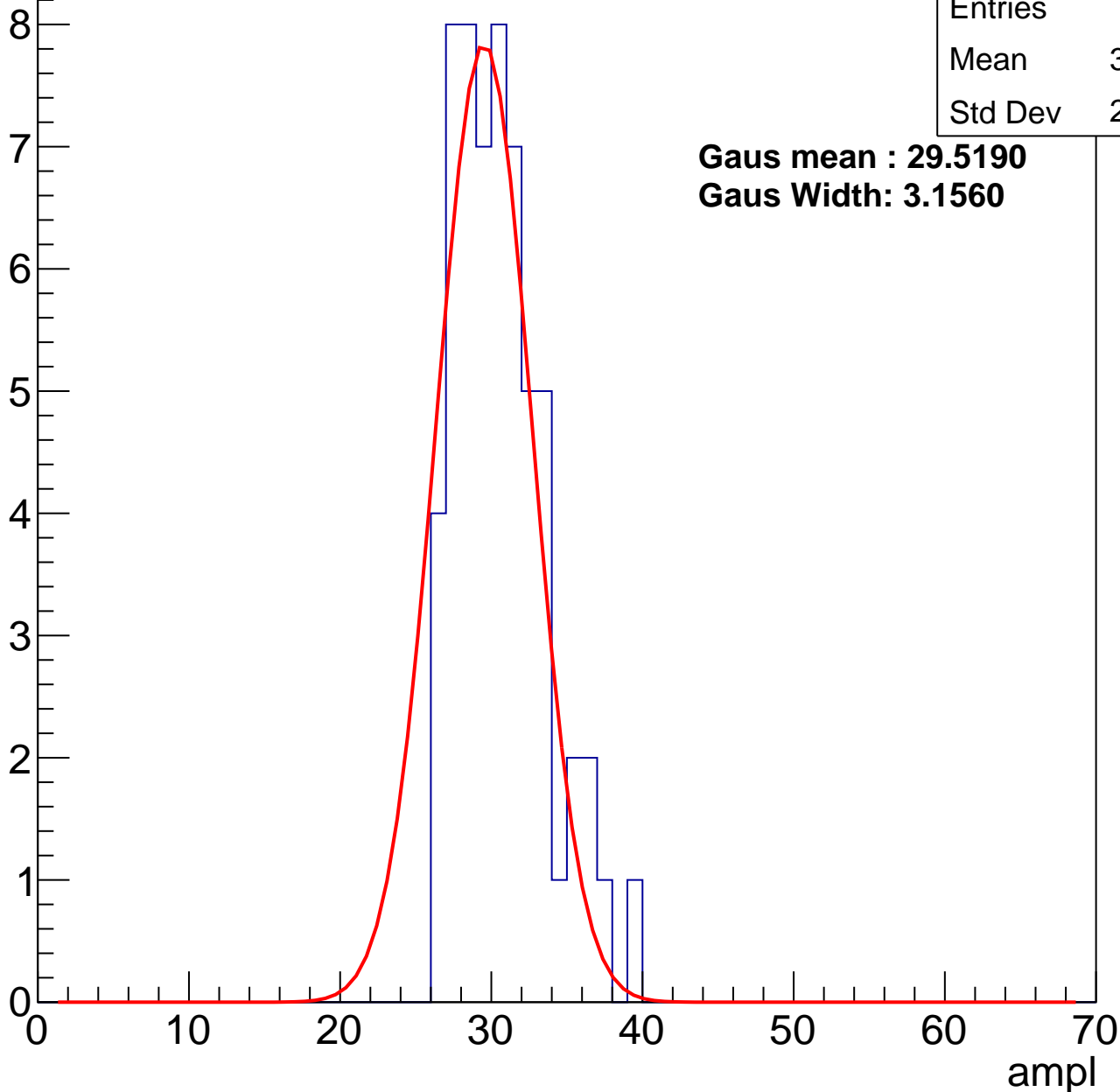
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	59
Mean	30.19
Std Dev	2.949

**Gaus mean : 29.5190**

**Gaus Width: 3.1560**



# B1L100S, U6-ch24, adc1

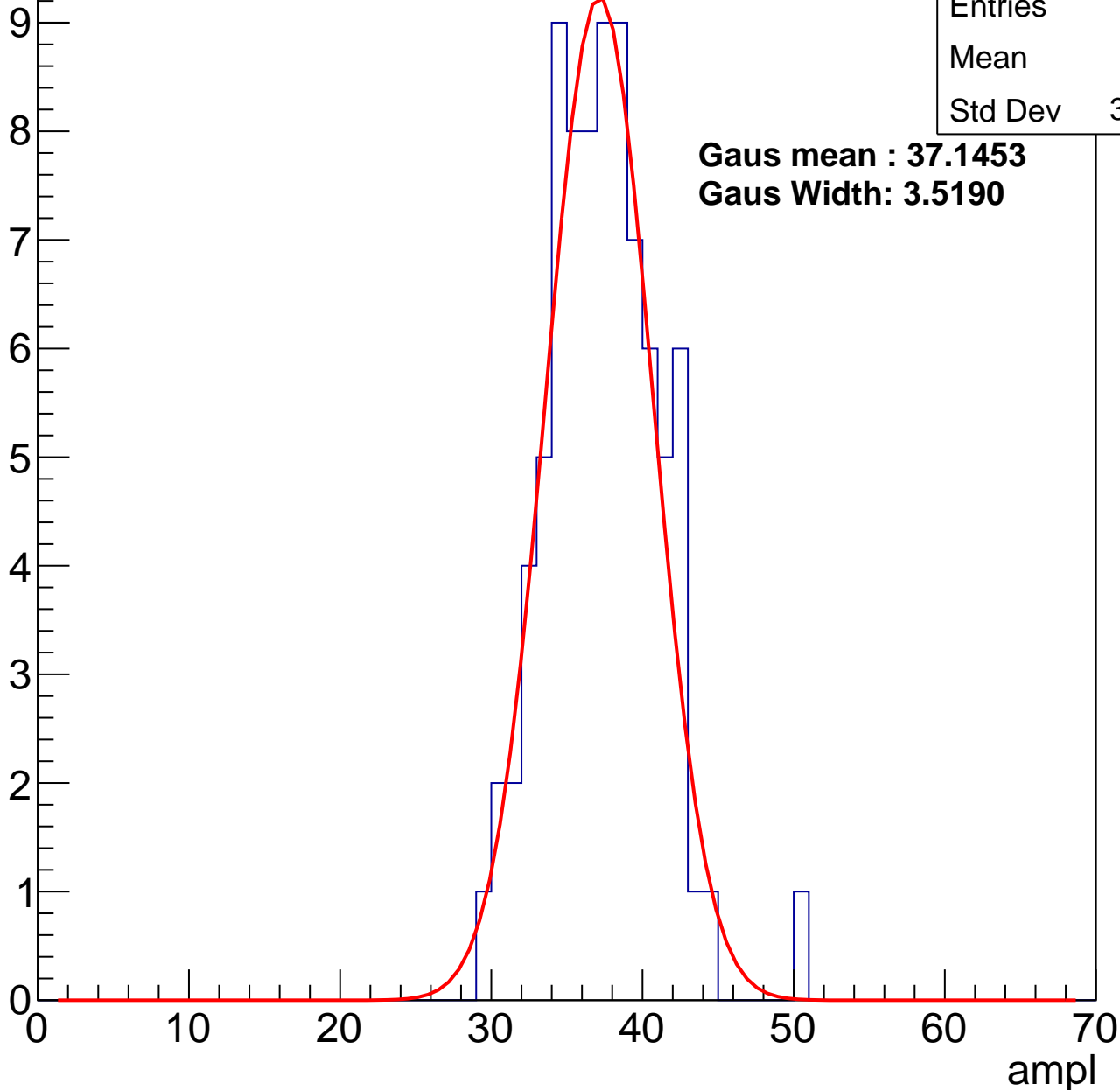
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	84
Mean	36.9
Std Dev	3.634

**Gaus mean : 37.1453**

**Gaus Width: 3.5190**



# B1L100S, U6-ch24, adc2

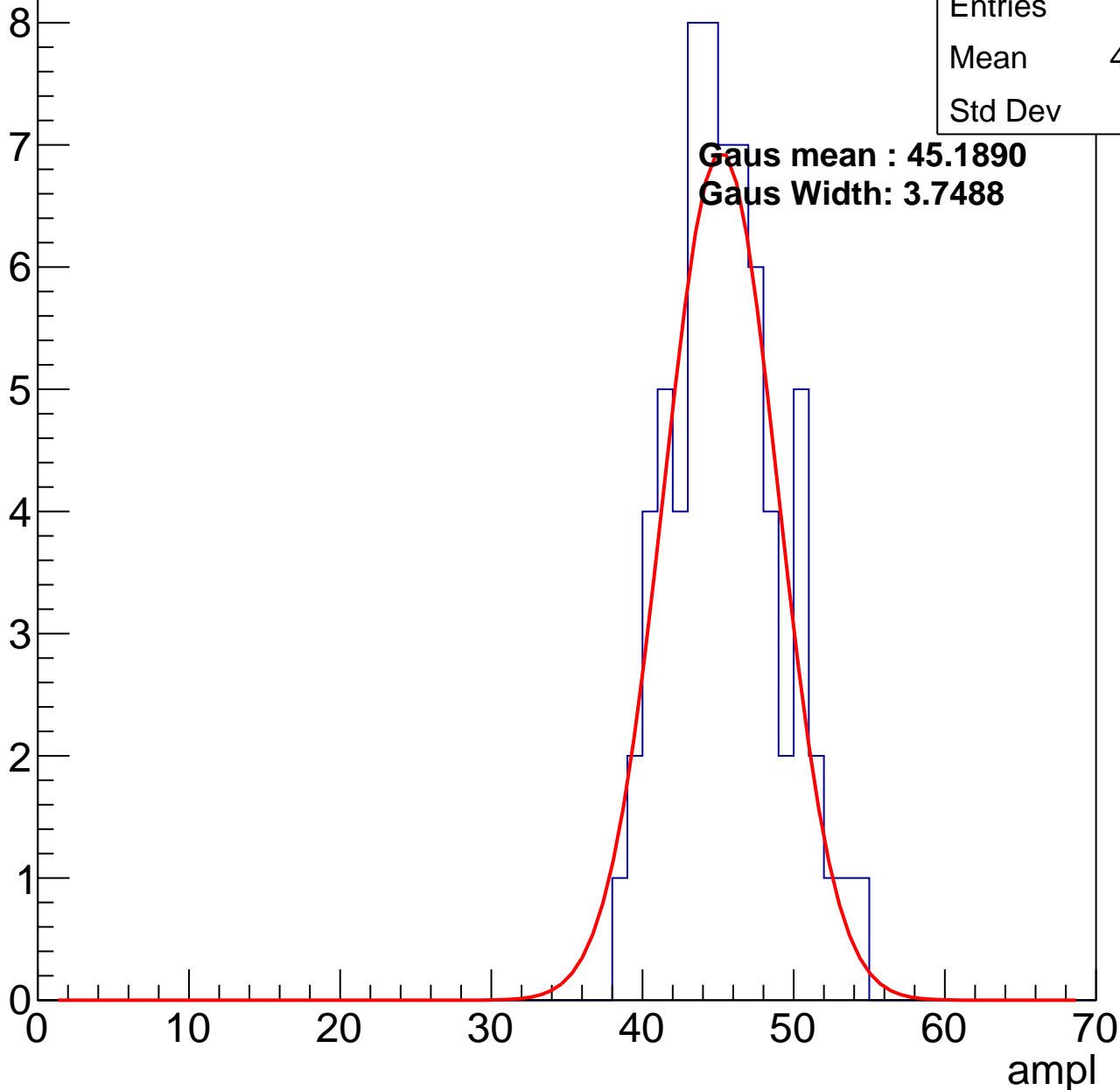
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	68
Mean	45.07
Std Dev	3.57

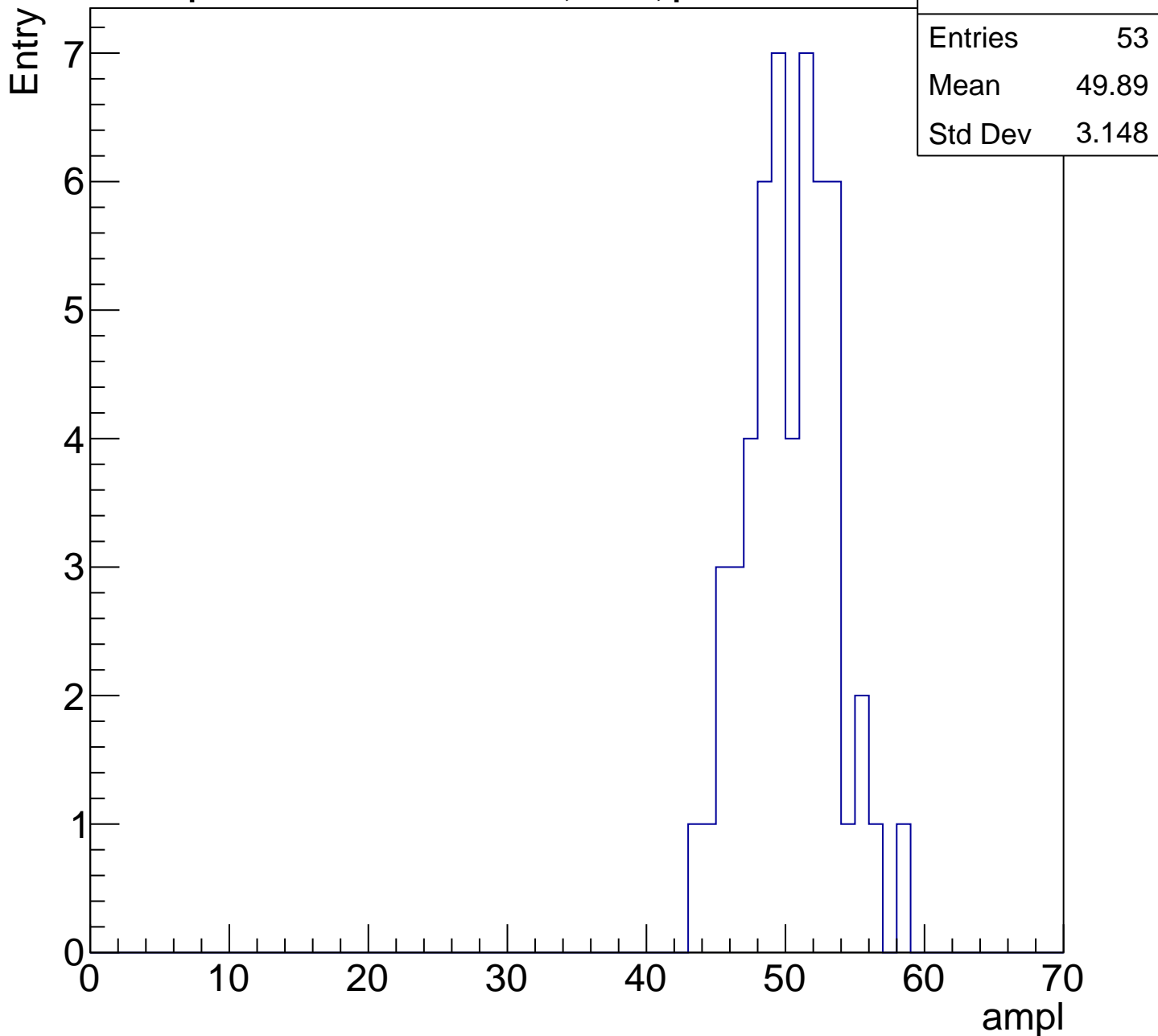
**Gaus mean : 45.1890**

**Gaus Width: 3.7488**



# B1L100S, U6-ch24, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

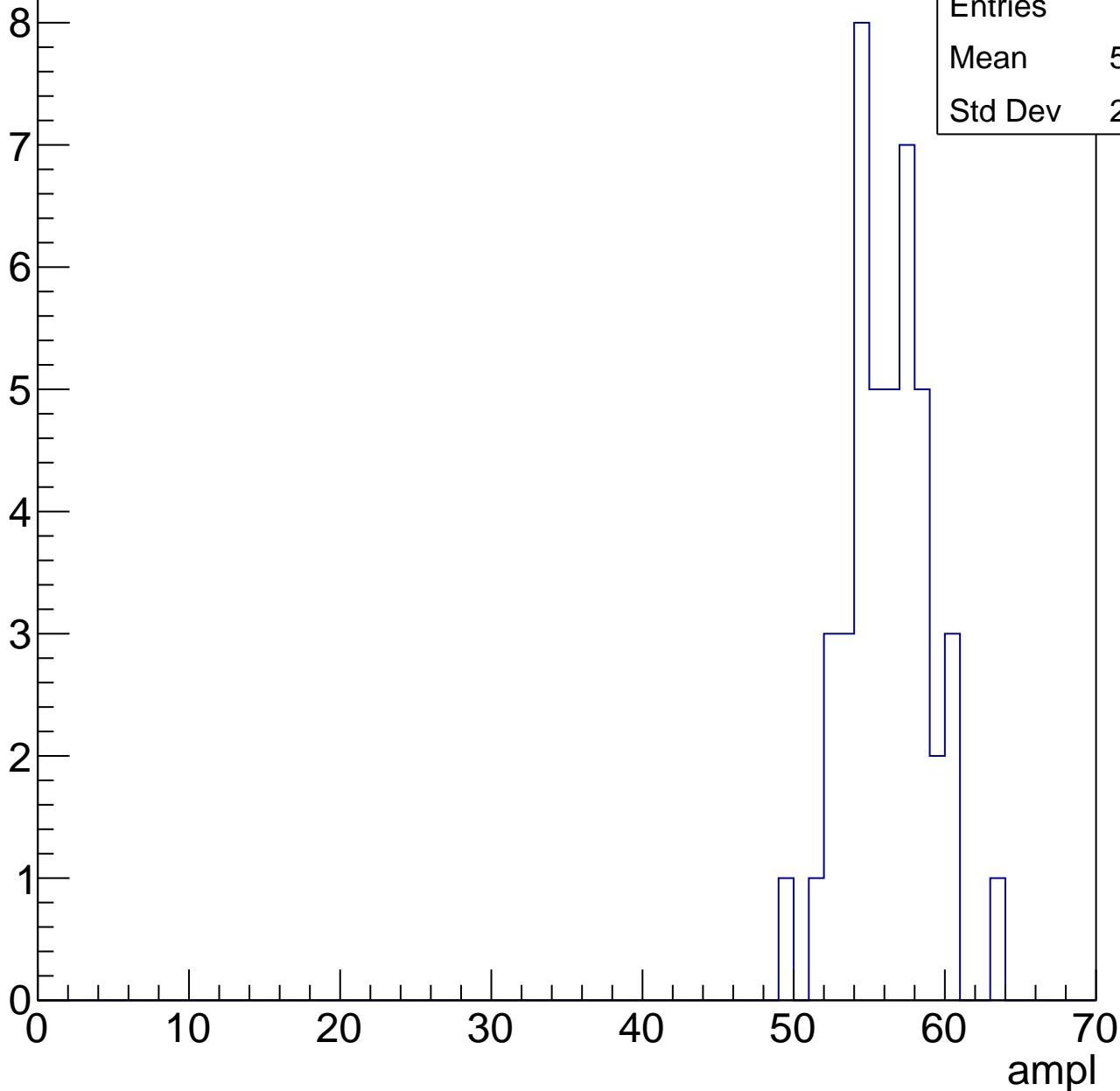


# B1L100S, U6-ch24, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	44
Mean	55.73
Std Dev	2.717



# B1L100S, U6-ch24, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

10

8

6

4

2

0

0

10

20

30

40

50

60

70

ampl

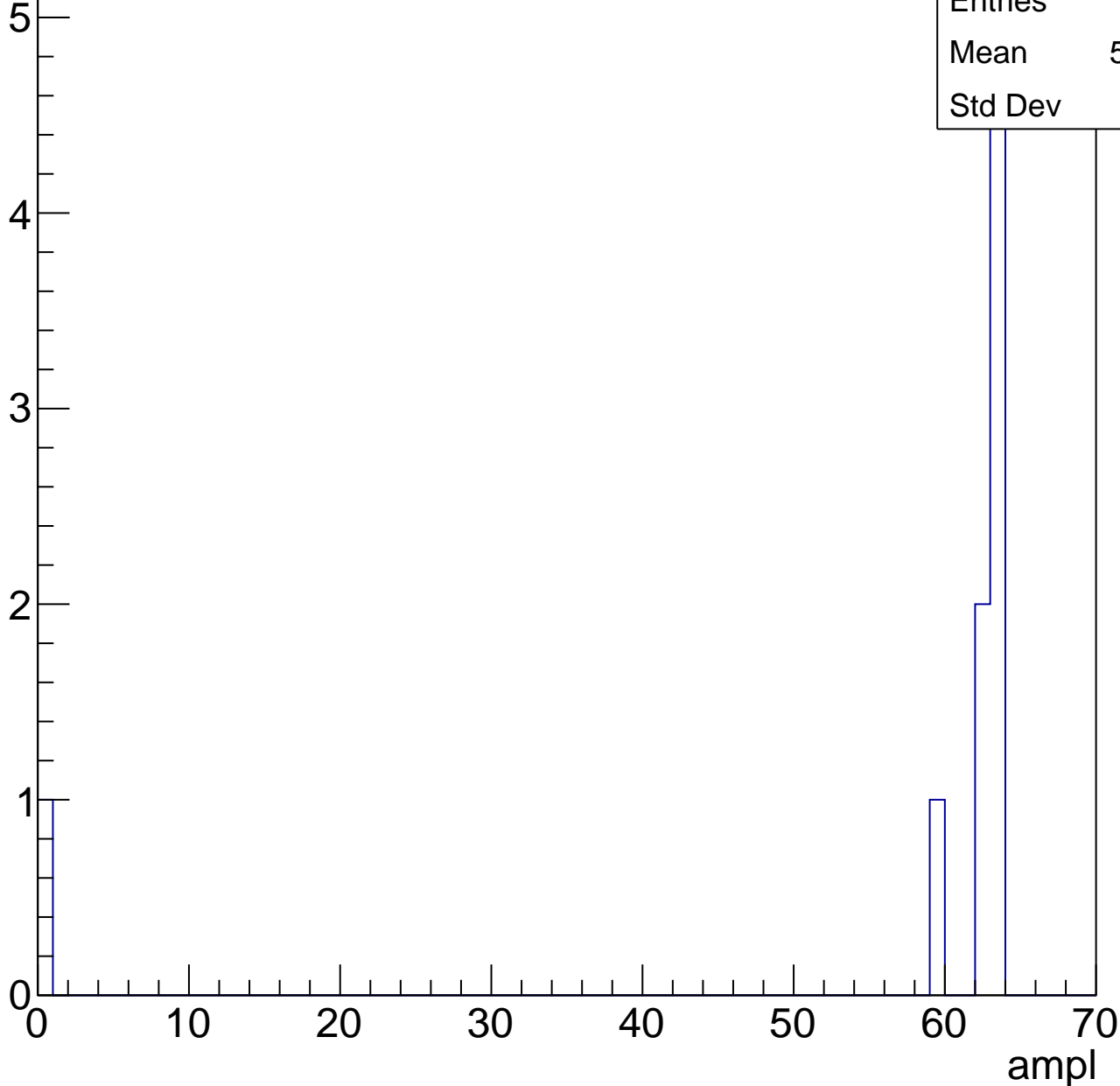
Entries	50
Mean	59.66
Std Dev	2.286

# B1L100S, U6-ch24, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	9
Mean	55.33
Std Dev	19.6





# B1L100S, U6-ch24, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	3
Mean	8.333
Std Dev	11.79

# B1L100S, U6-ch25, adc0

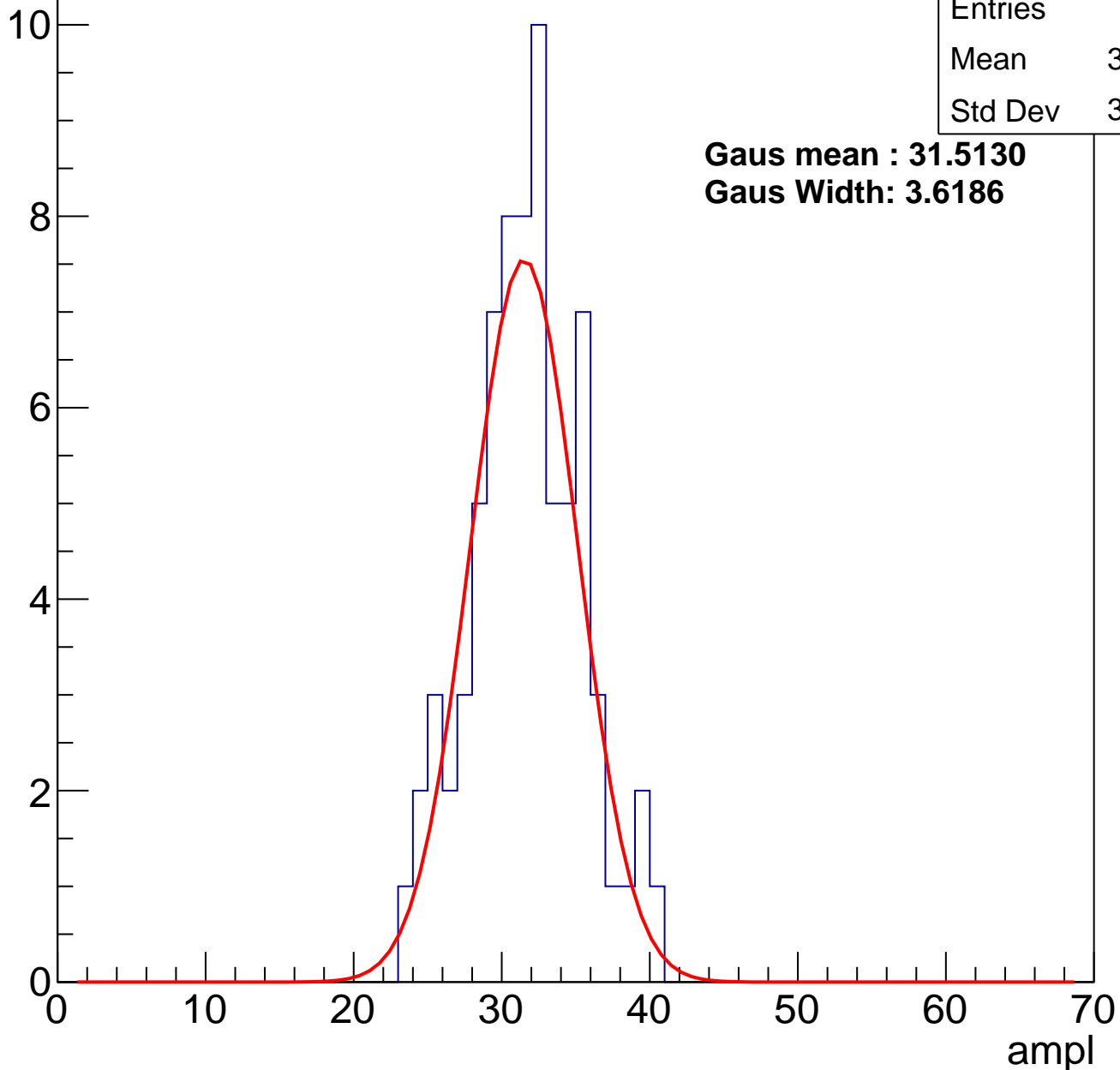
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	74
Mean	31.23
Std Dev	3.678

**Gaus mean : 31.5130**

**Gaus Width: 3.6186**

Entry



# B1L100S, U6-ch25, adc1

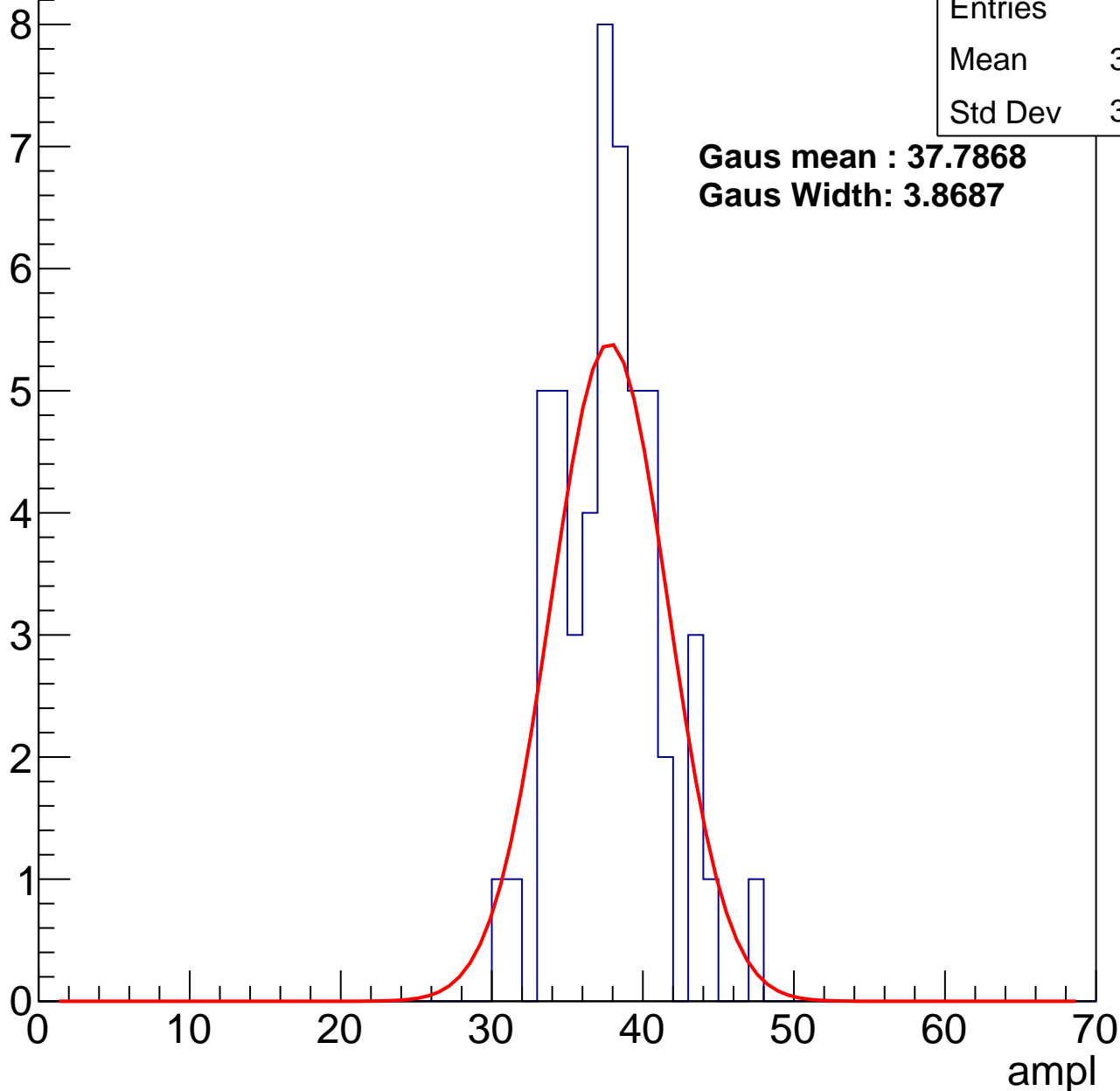
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	51
Mean	37.33
Std Dev	3.376

**Gaus mean : 37.7868**

**Gaus Width: 3.8687**



# B1L100S, U6-ch25, adc2

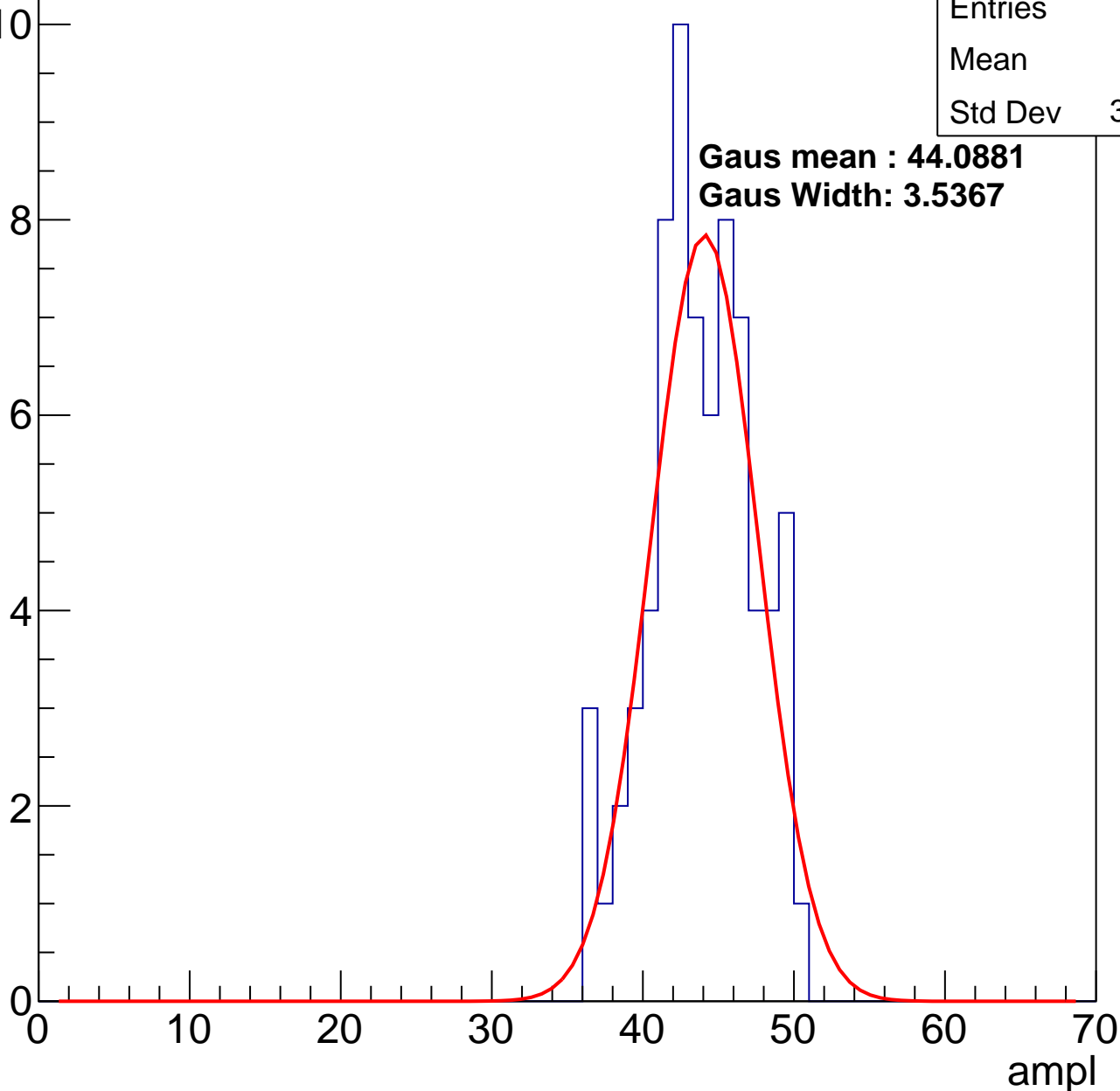
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	73
Mean	43.4
Std Dev	3.395

**Gaus mean : 44.0881**

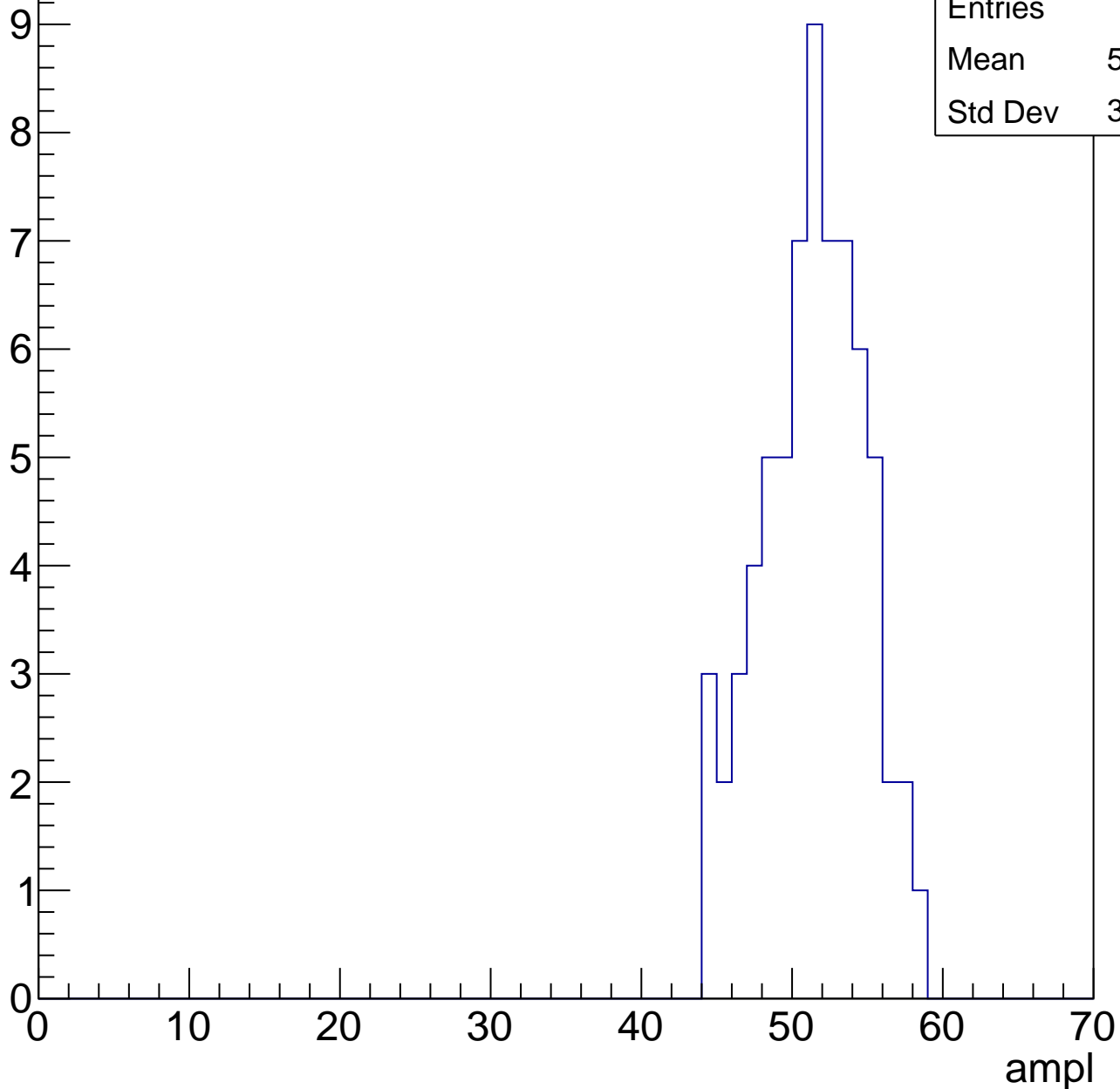
**Gaus Width: 3.5367**



# B1L100S, U6-ch25, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

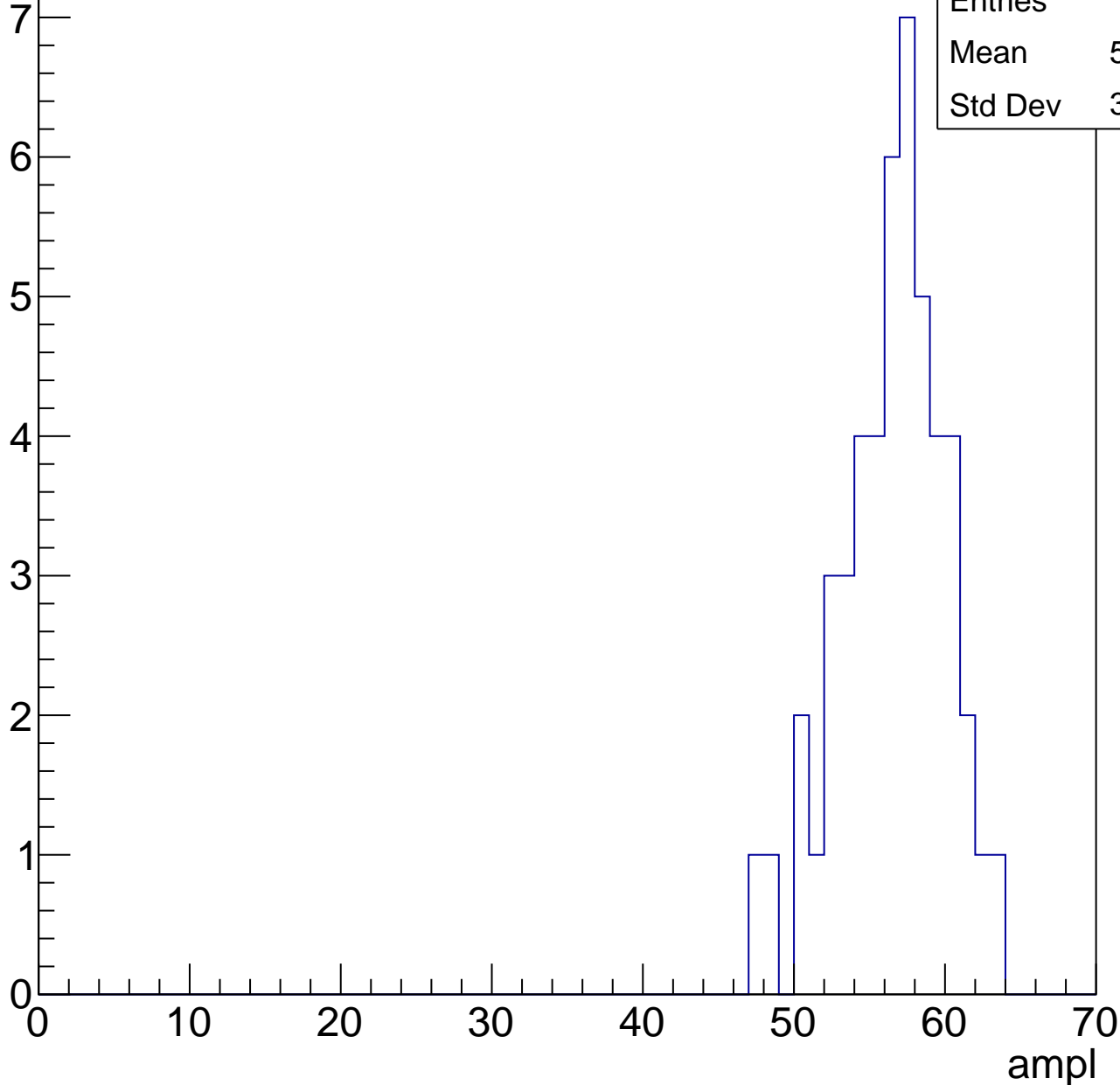
Entry



# B1L100S, U6-ch25, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

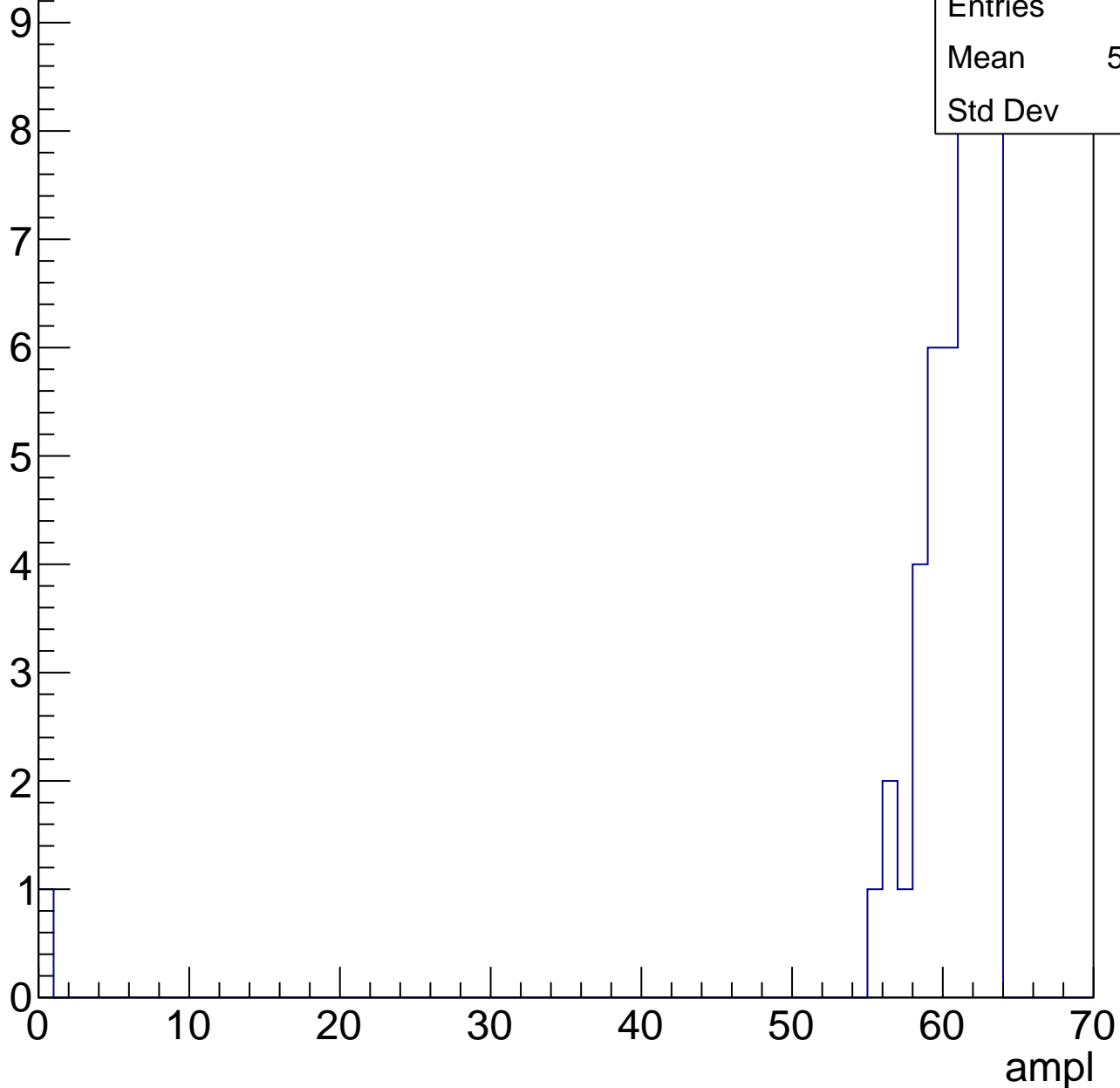


Entries	49
Mean	56.02
Std Dev	3.496

# B1L100S, U6-ch25, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

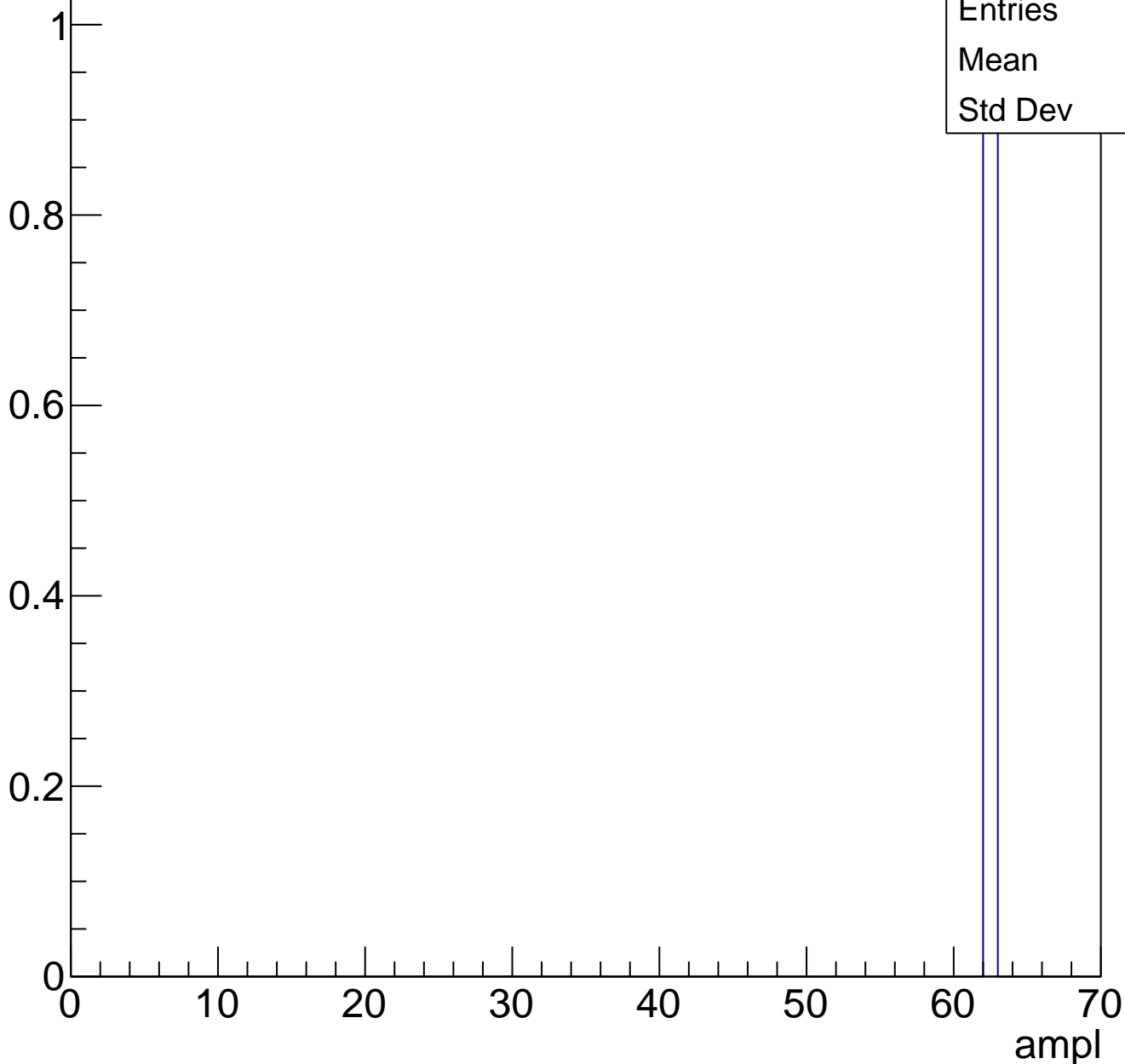
Entry



# B1L100S, U6-ch25, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry





# B1L100S, U6-ch25, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L100S, U6-ch26, adc0

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	66
Mean	28.27
Std Dev	5.002

**Gaus mean : 29.3369**

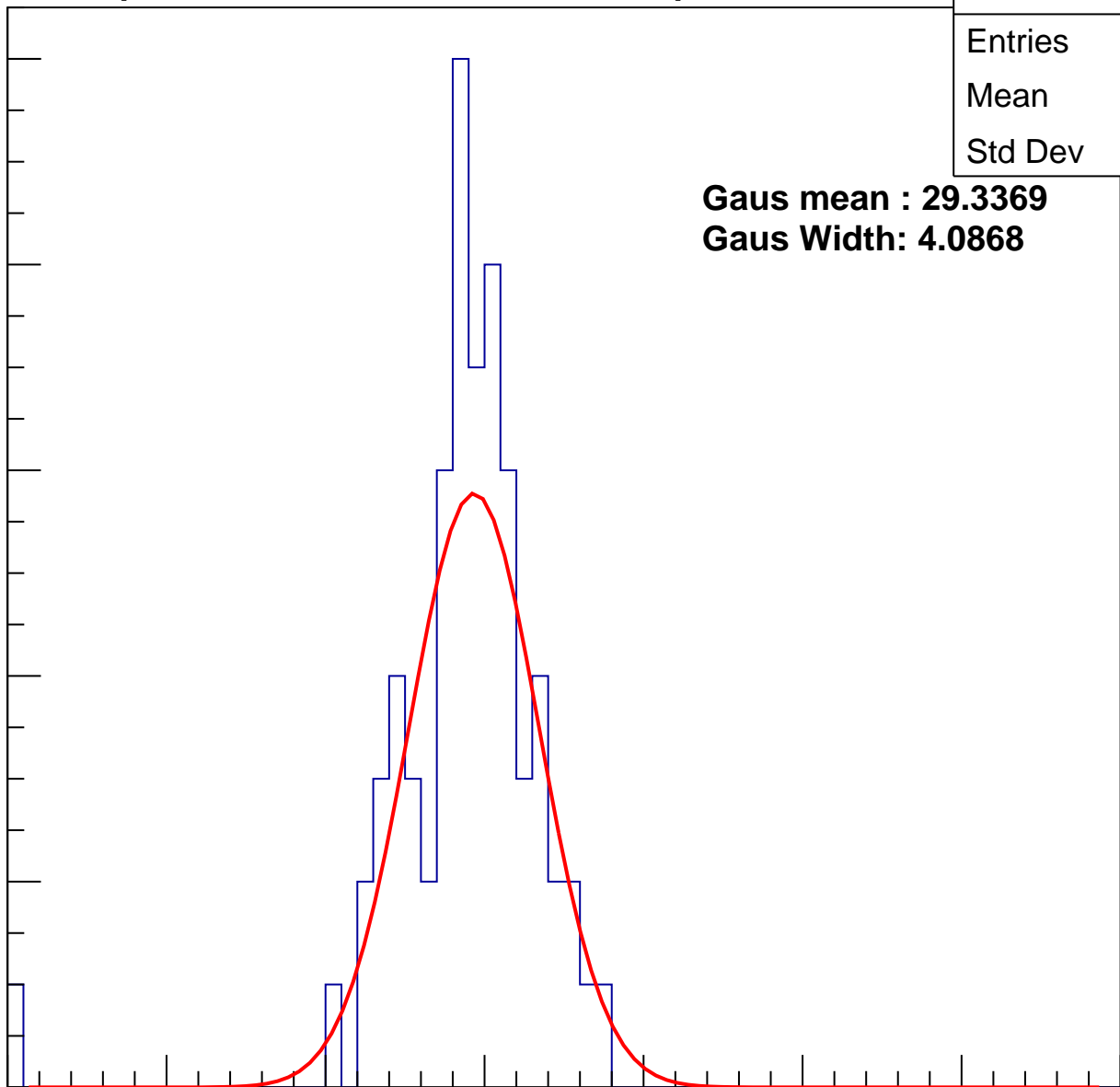
**Gaus Width: 4.0868**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L100S, U6-ch26, adc1

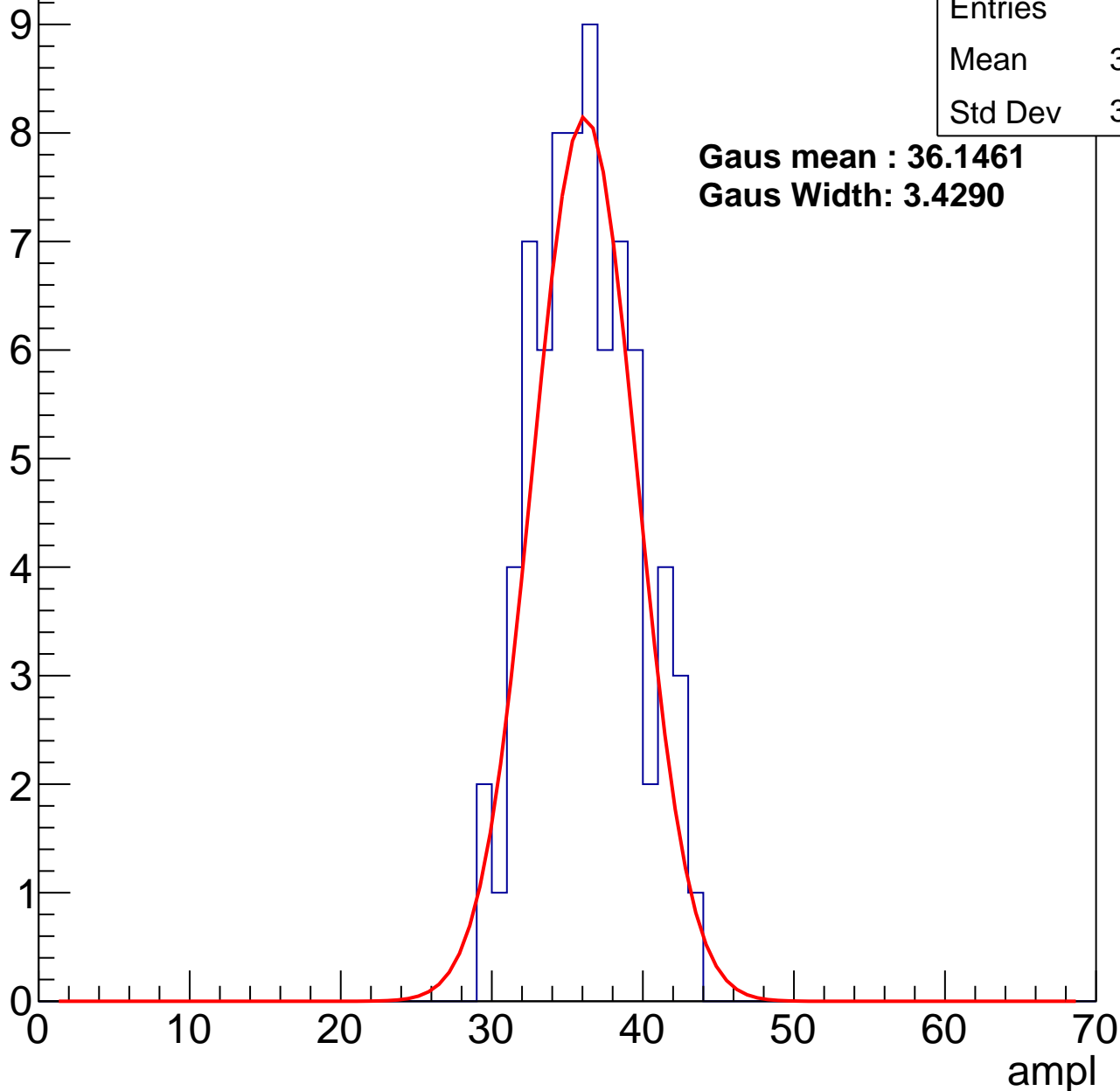
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	74
Mean	35.74
Std Dev	3.313

**Gaus mean : 36.1461**

**Gaus Width: 3.4290**



# B1L100S, U6-ch26, adc2

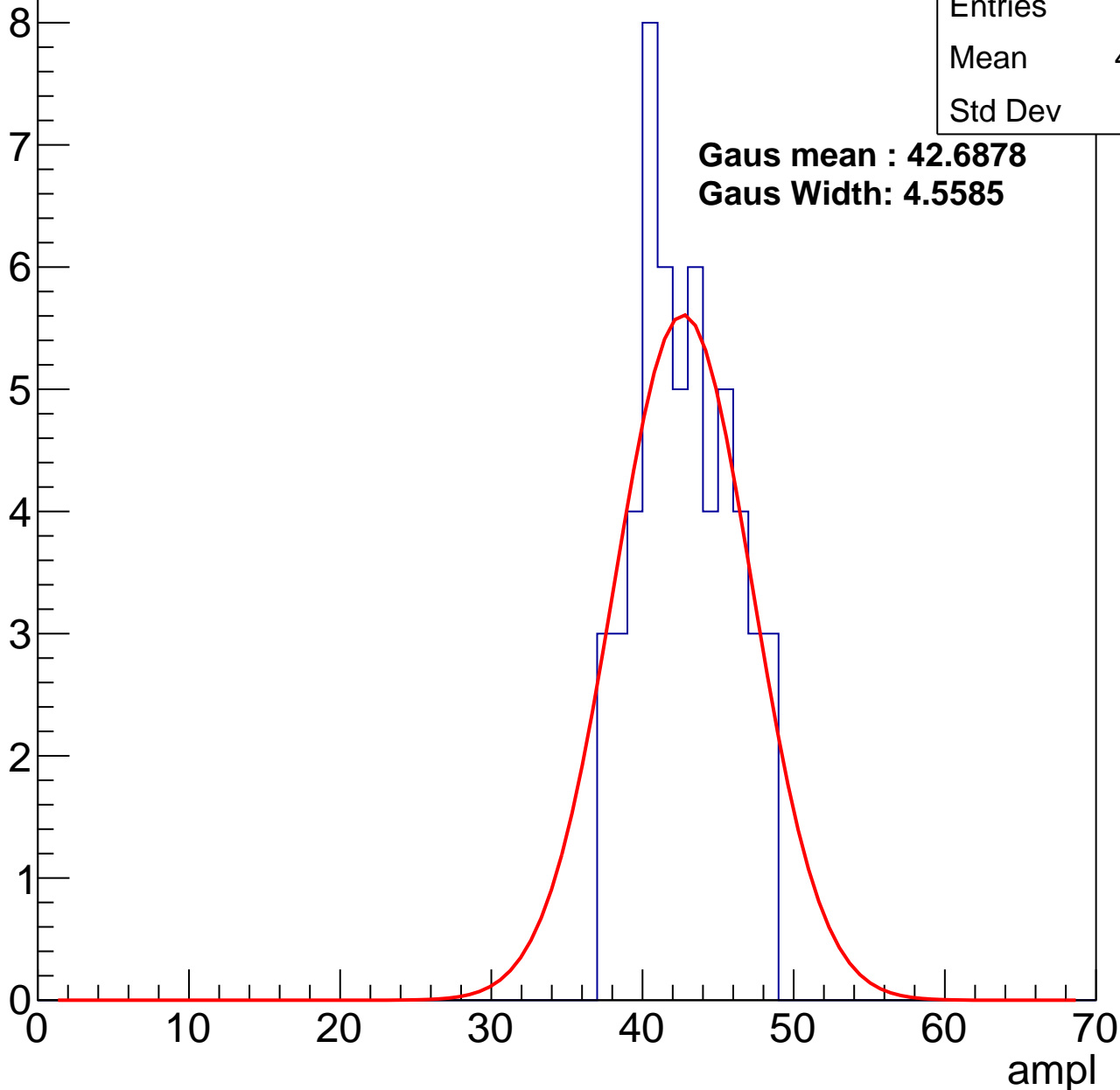
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	54
Mean	42.31
Std Dev	3.06

**Gaus mean : 42.6878**

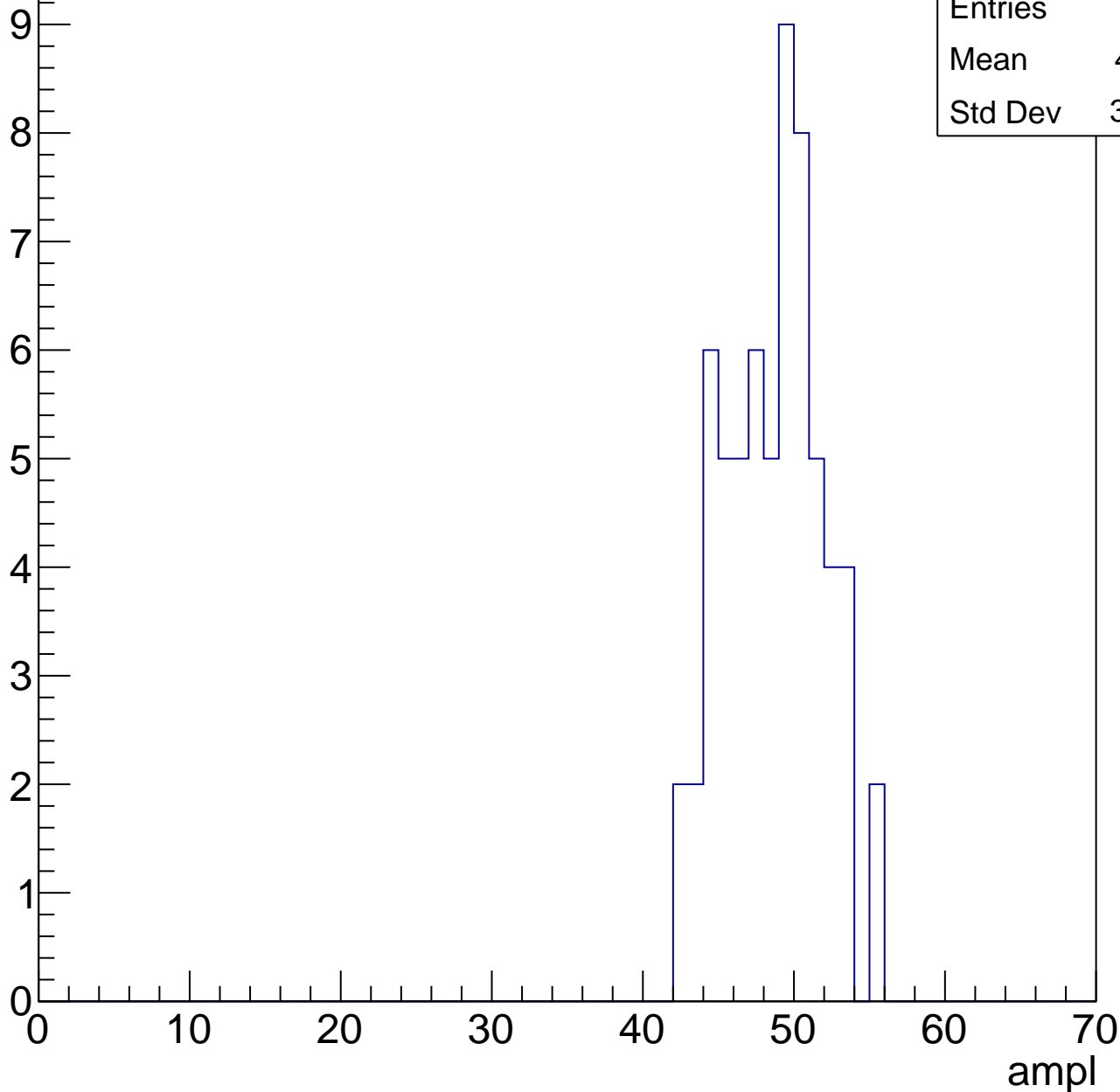
**Gaus Width: 4.5585**



# B1L100S, U6-ch26, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



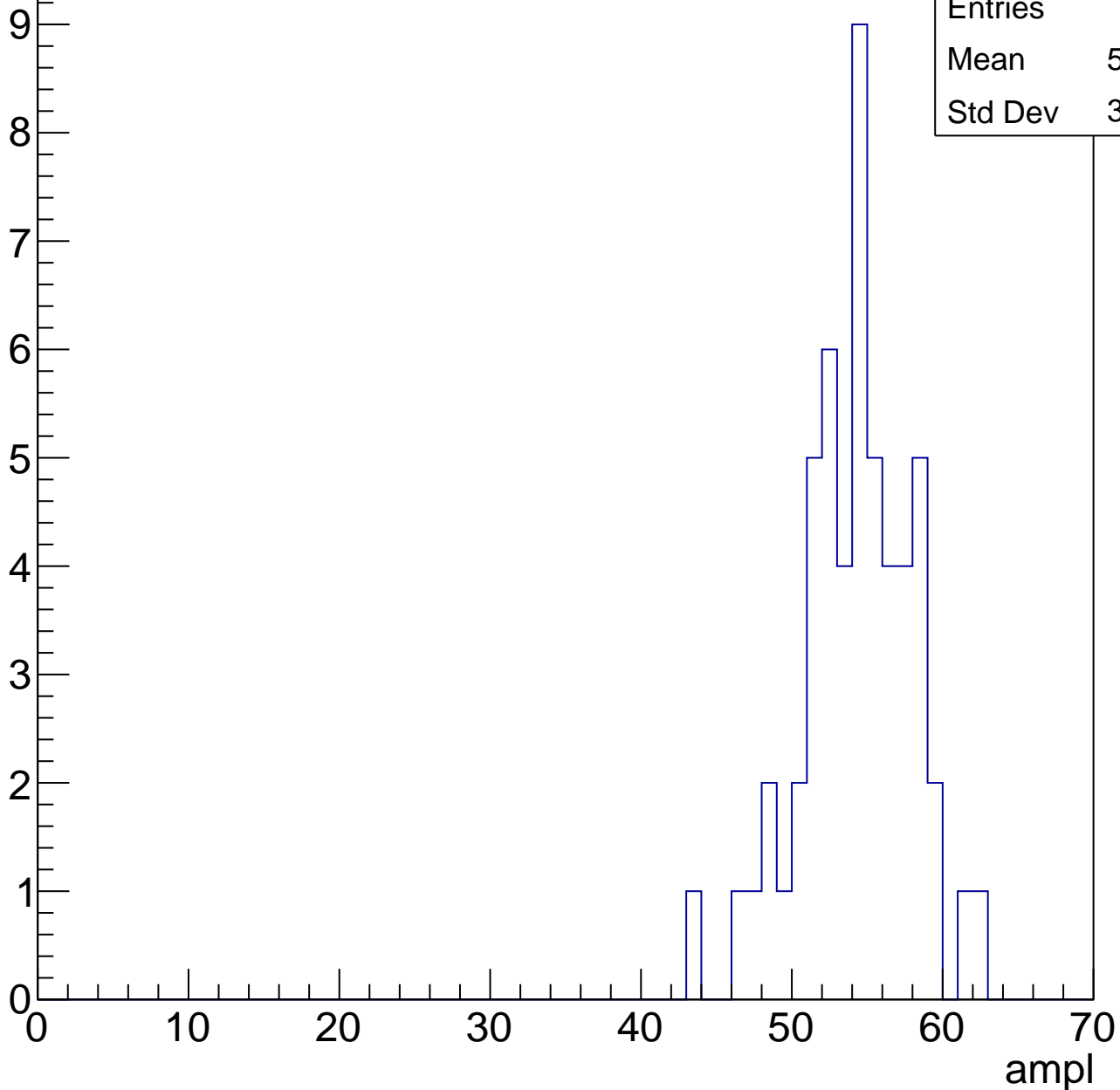
Entries	63
Mean	48.21
Std Dev	3.173

# B1L100S, U6-ch26, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	54
Mean	53.78
Std Dev	3.685

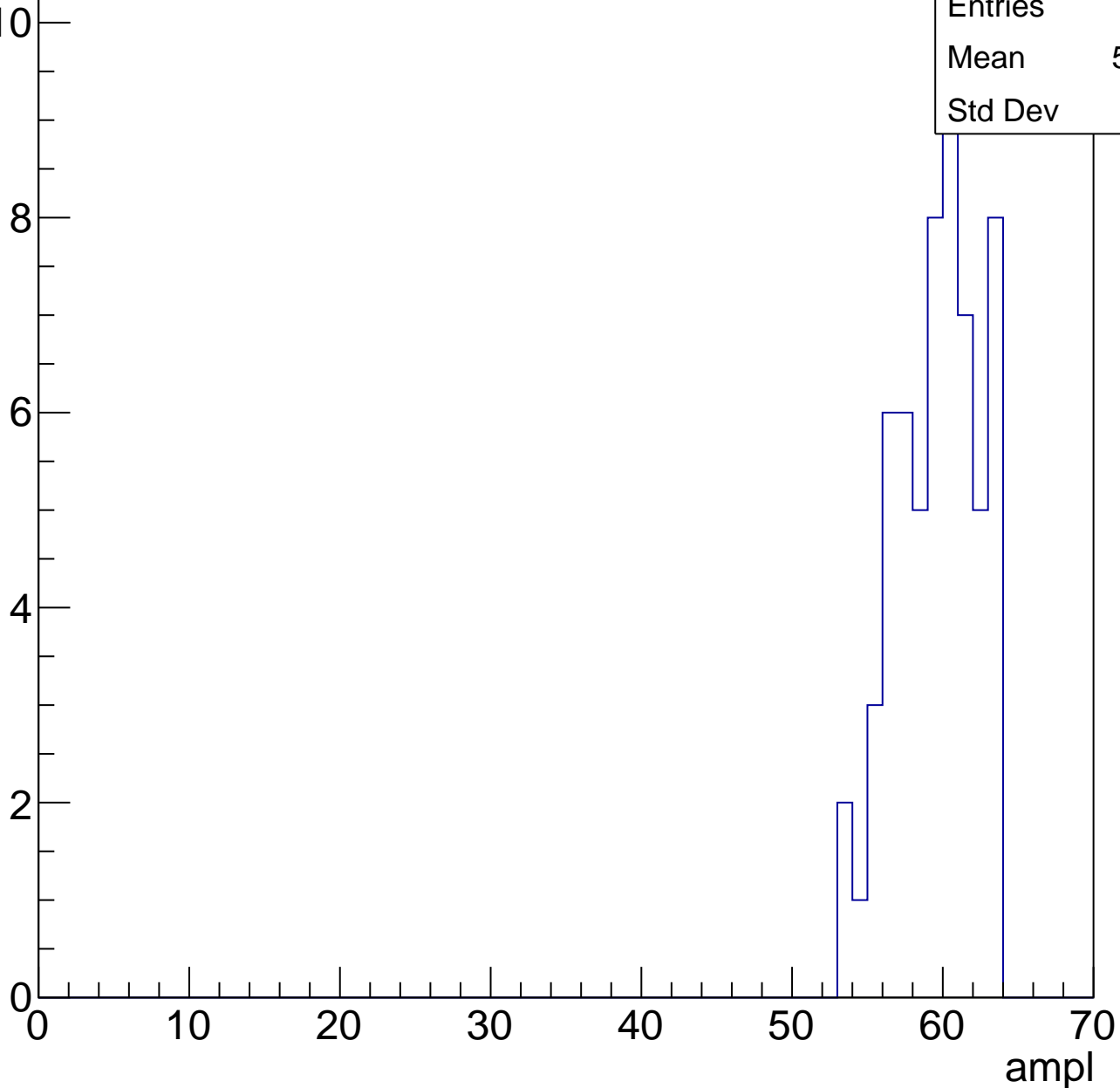


# B1L100S, U6-ch26, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

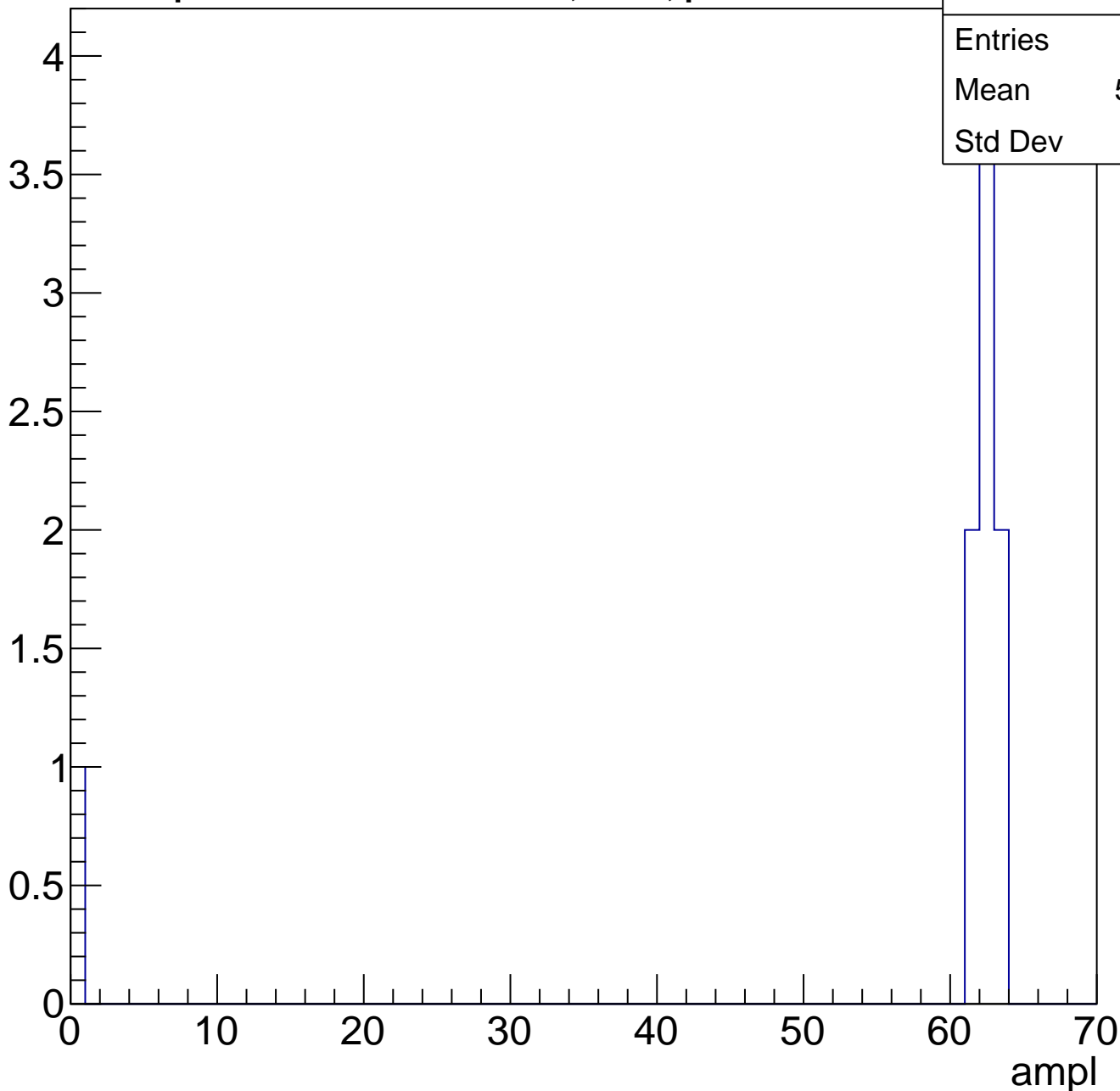
Entries	61
Mean	59.11
Std Dev	2.68



# B1L100S, U6-ch26, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry





# B1L100S, U6-ch26, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L100S, U6-ch27, adc0

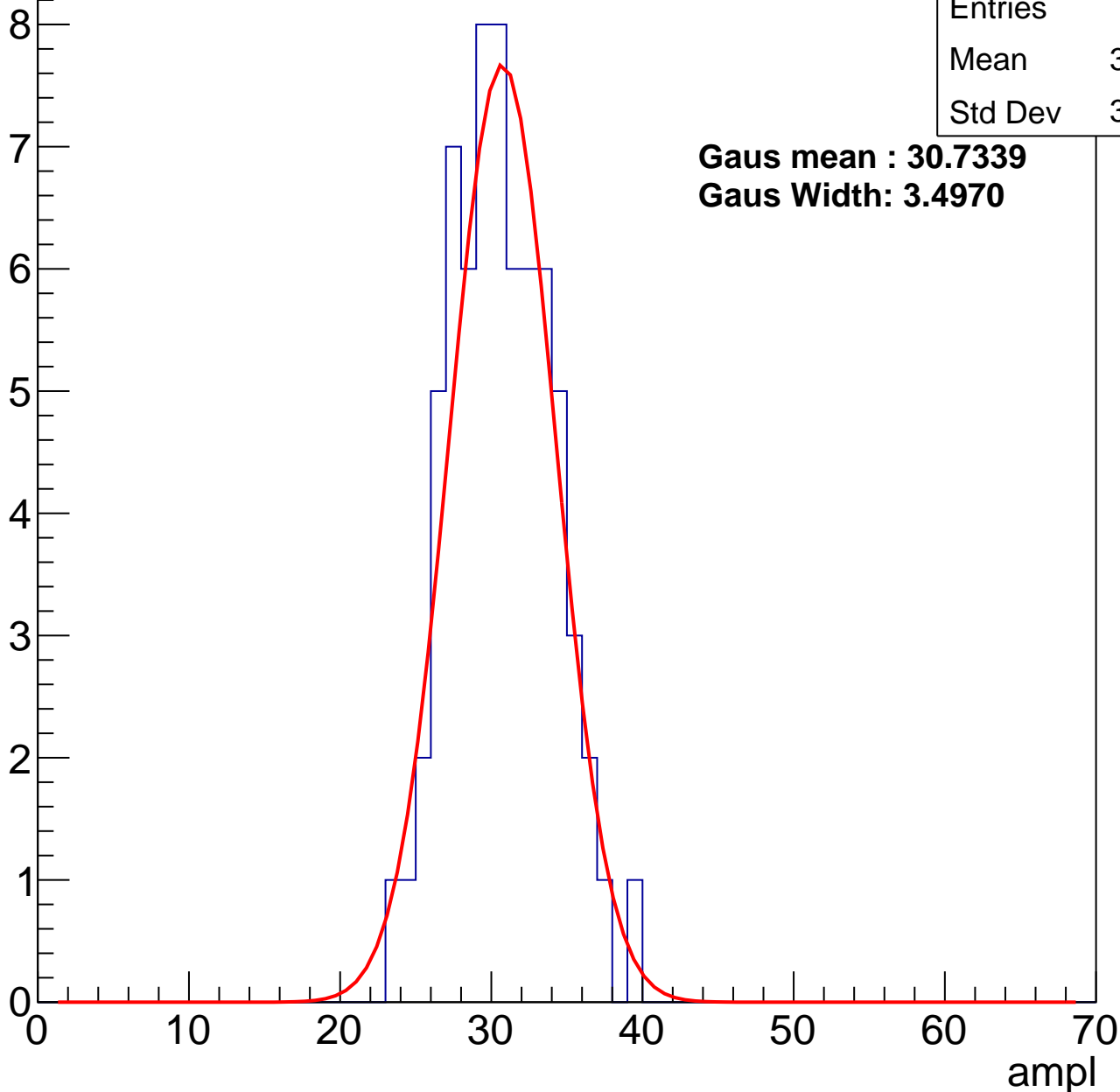
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	68
Mean	30.22
Std Dev	3.316

**Gaus mean : 30.7339**

**Gaus Width: 3.4970**



# B1L100S, U6-ch27, adc1

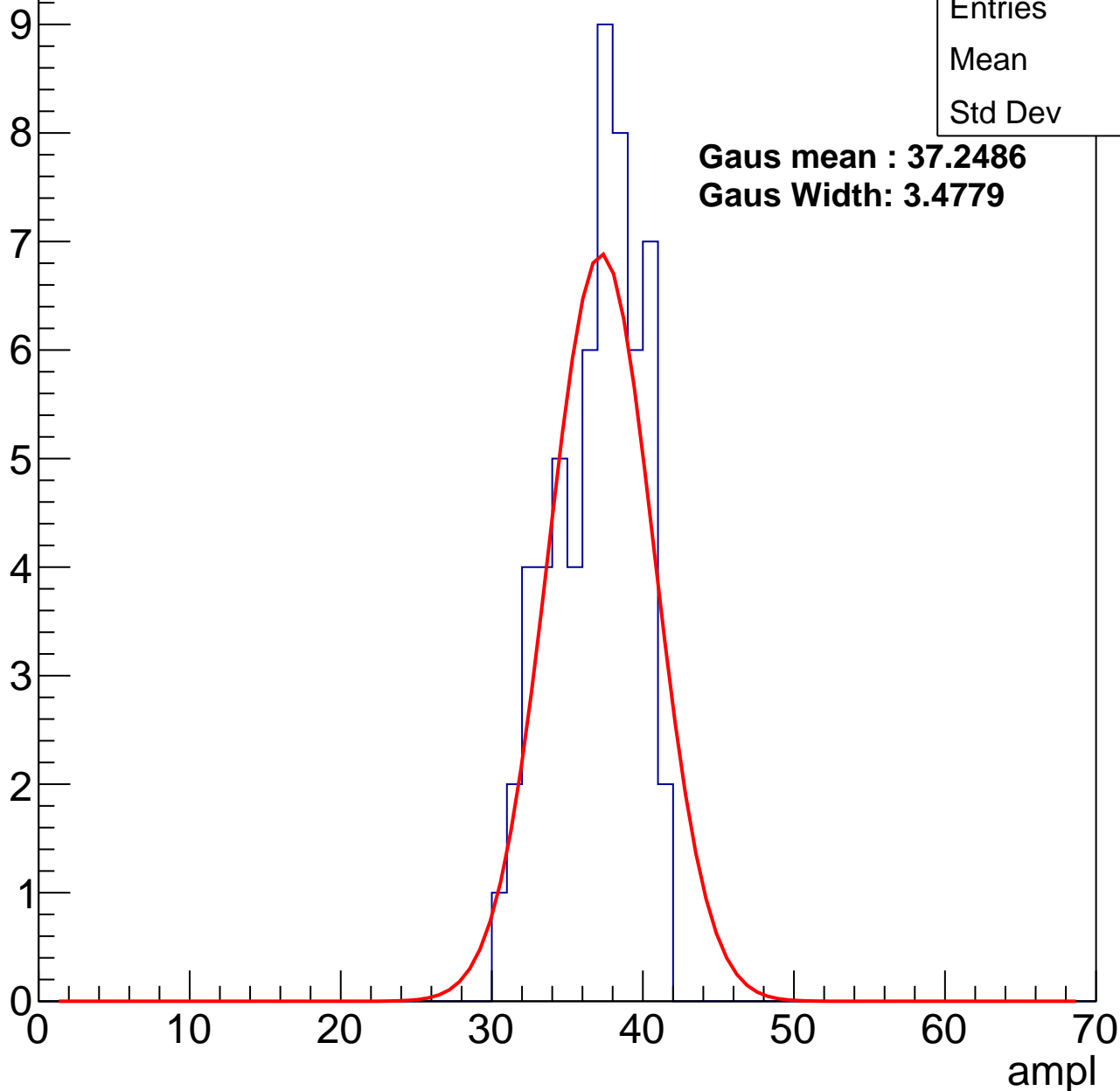
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	58
Mean	36.4
Std Dev	2.81

**Gaus mean : 37.2486**

**Gaus Width: 3.4779**



# B1L100S, U6-ch27, adc2

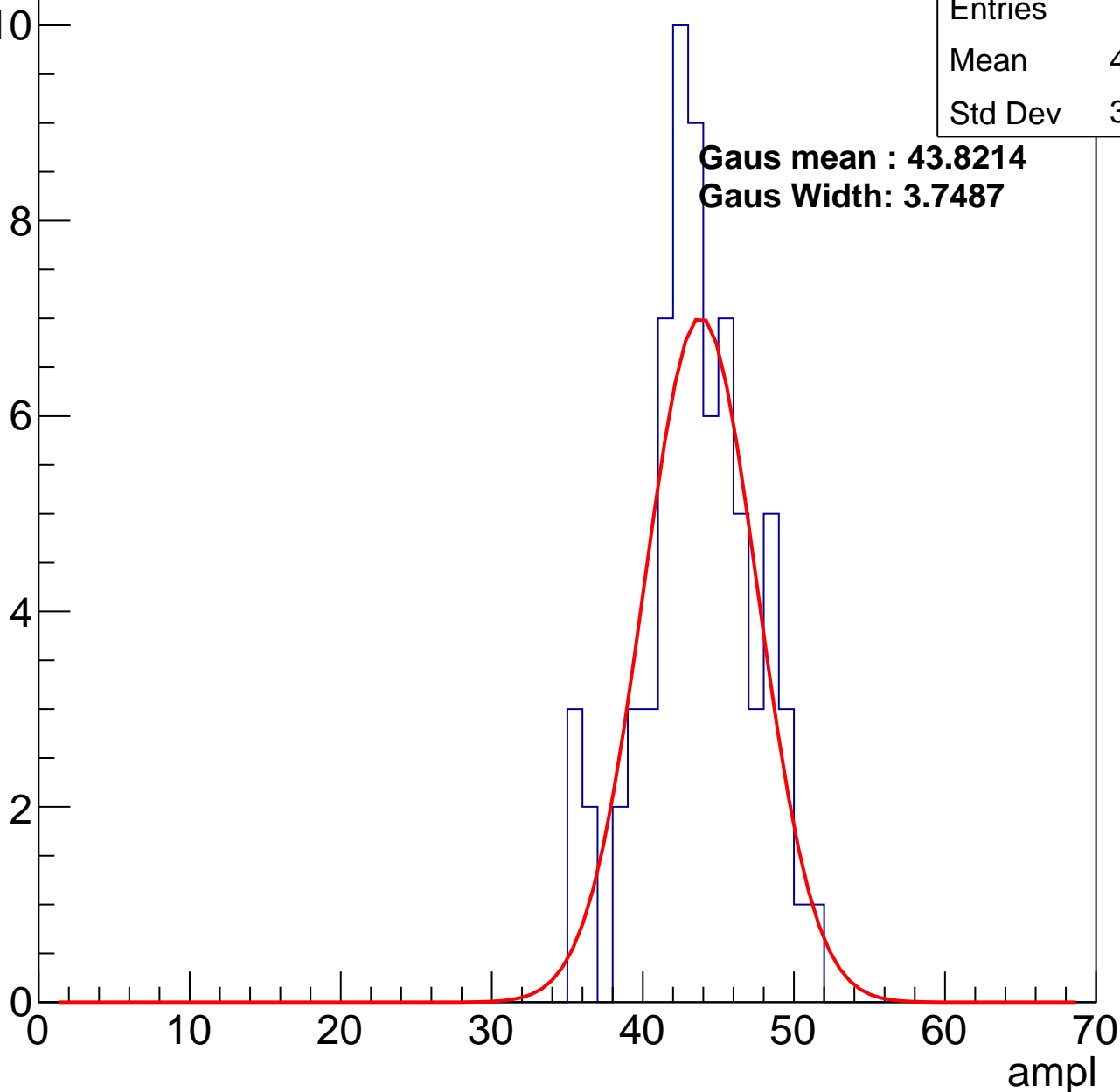
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	70
Mean	43.17
Std Dev	3.633

**Gaus mean : 43.8214**

**Gaus Width: 3.7487**

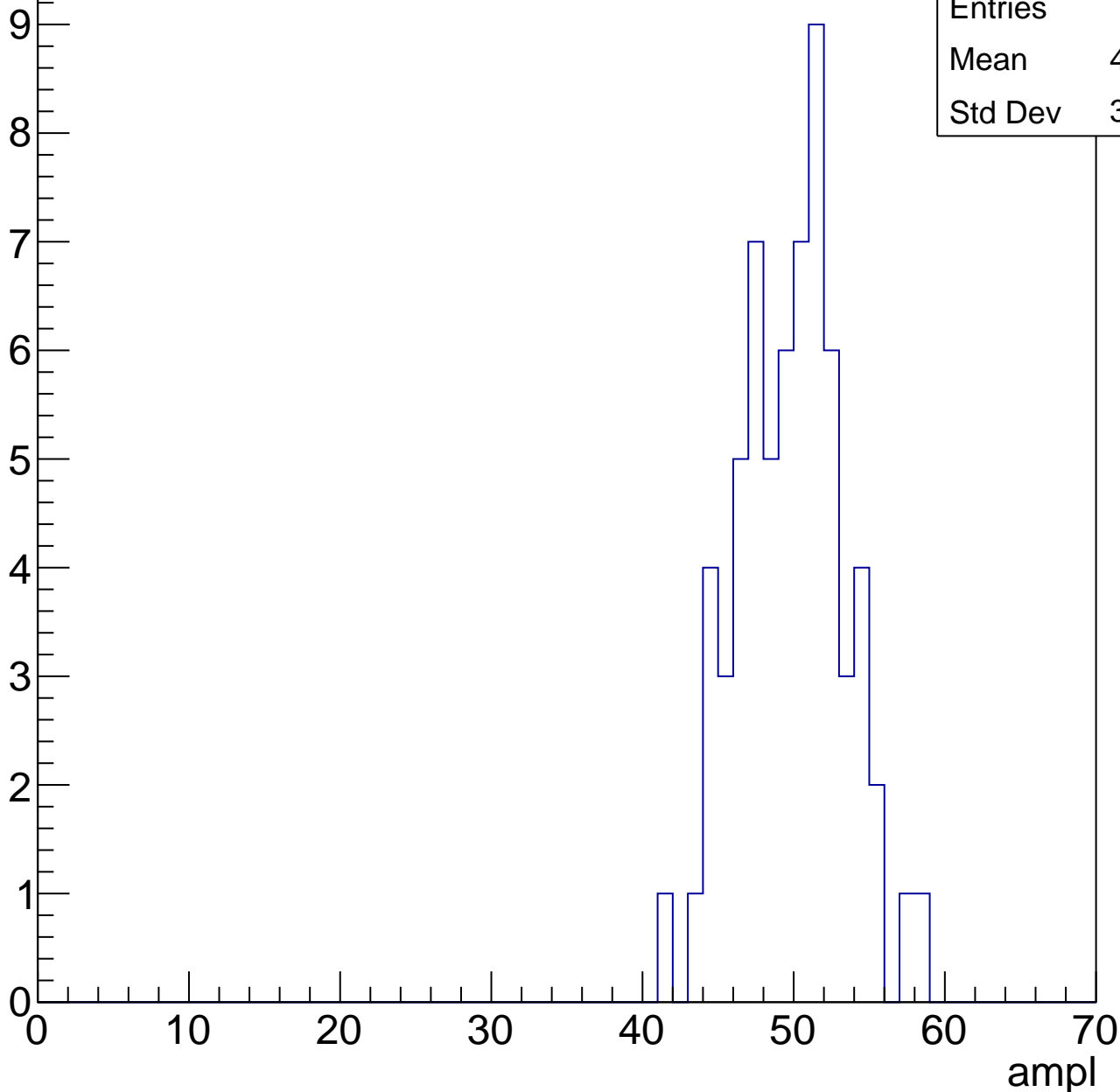


# B1L100S, U6-ch27, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	65
Mean	49.37
Std Dev	3.462

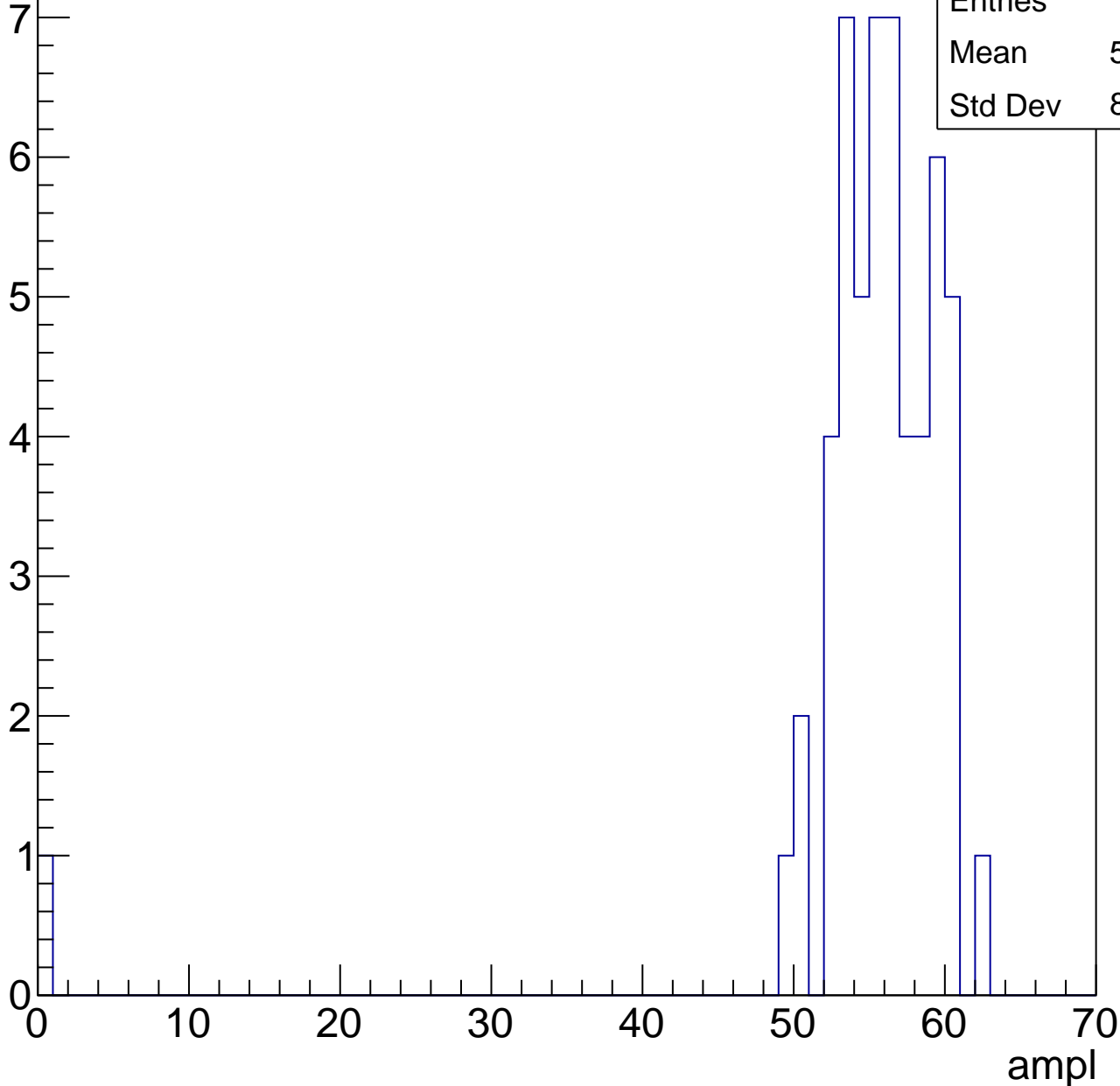


# B1L100S, U6-ch27, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	54
Mean	54.65
Std Dev	8.053



# B1L100S, U6-ch27, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

10

8

6

4

2

0

0

10

20

30

40

50

60

70

ampl

Entries	50
Mean	59.96
Std Dev	2.416

# B1L100S, U6-ch27, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry





# B1L100S, U6-ch27, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



# B1L100S, U6-ch28, adc0

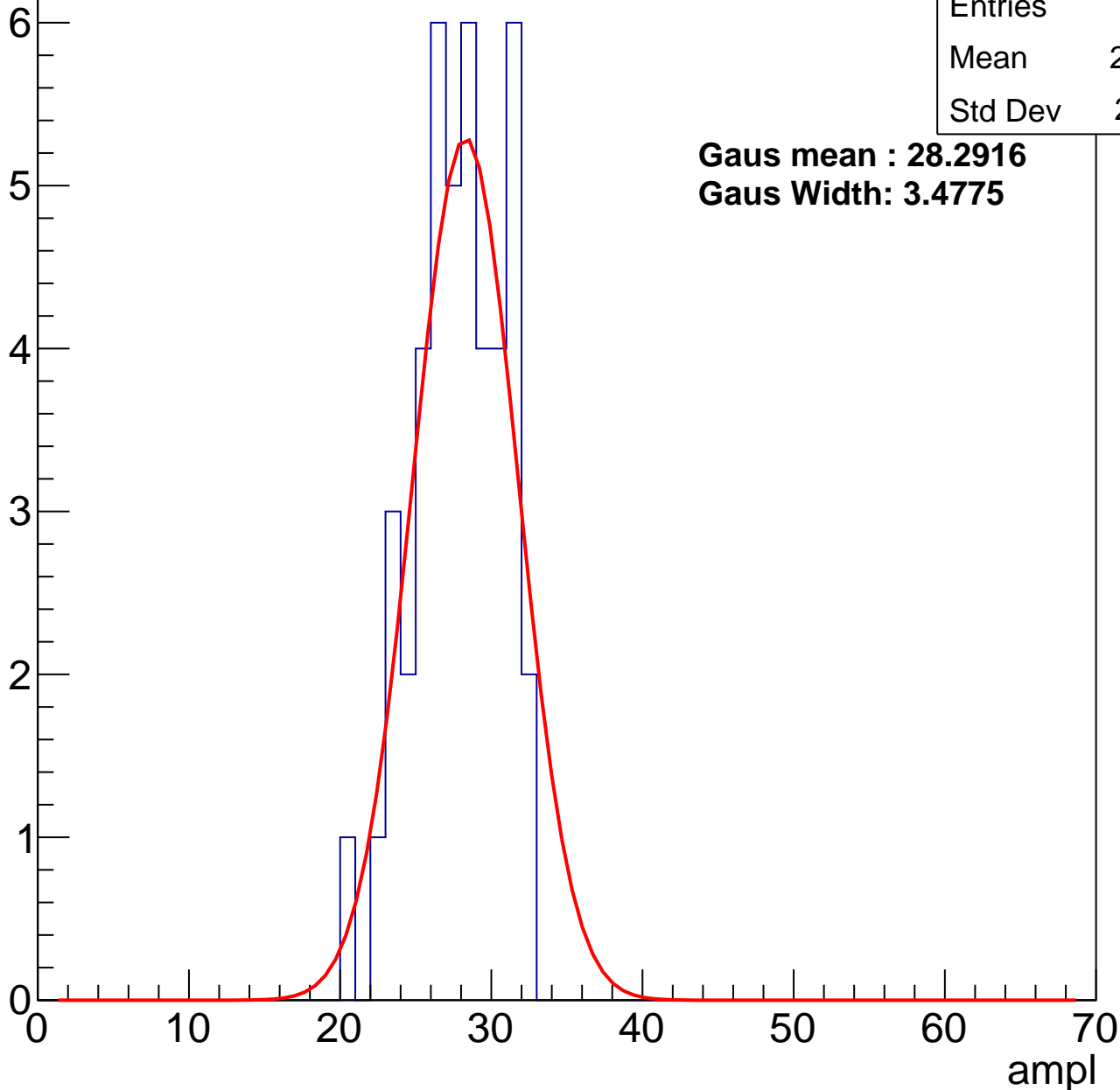
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	44
Mean	27.36
Std Dev	2.861

**Gaus mean : 28.2916**

**Gaus Width: 3.4775**



# B1L100S, U6-ch28, adc1

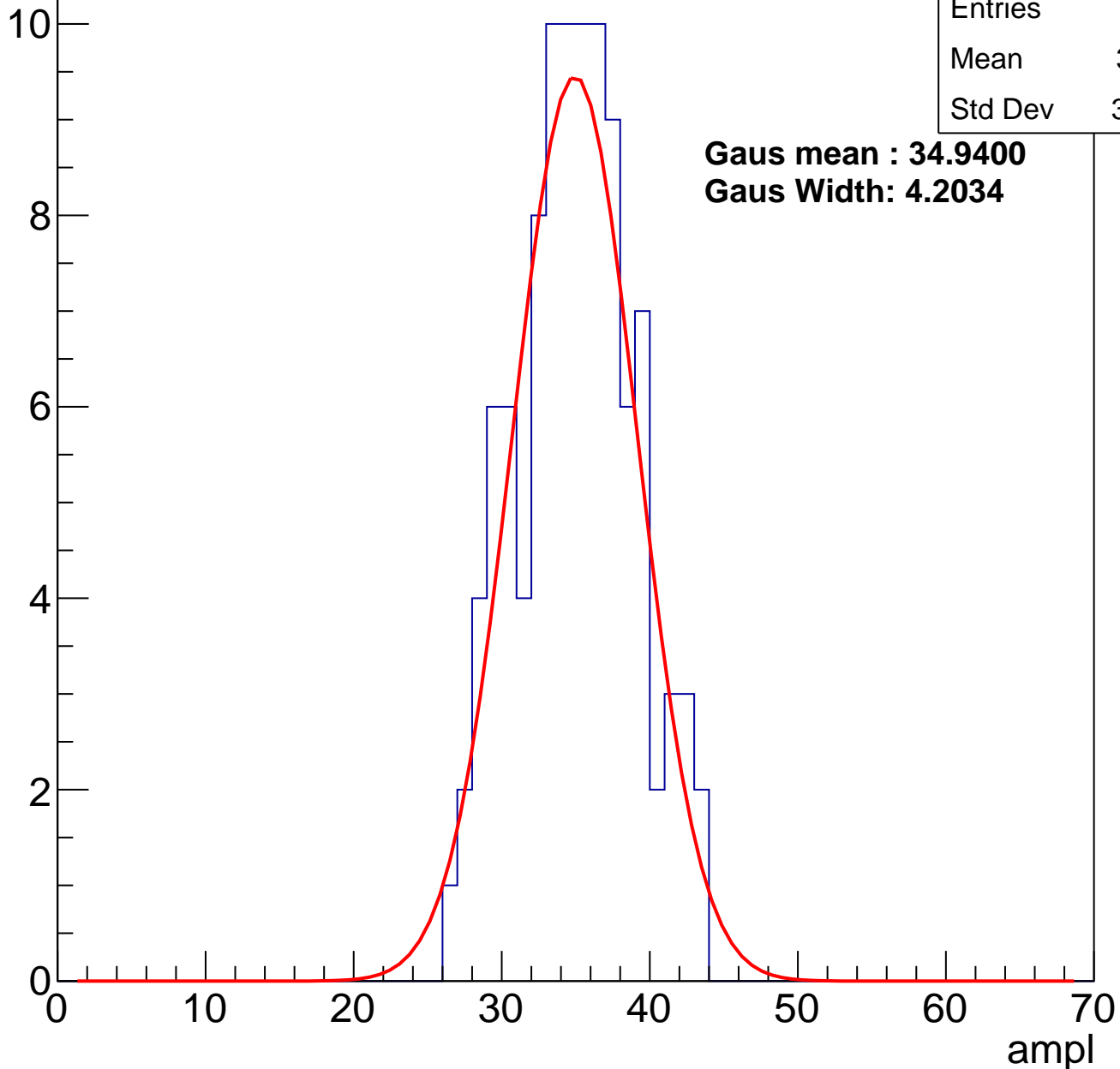
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	103
Mean	34.51
Std Dev	3.914

**Gaus mean : 34.9400**

**Gaus Width: 4.2034**

Entry



# B1L100S, U6-ch28, adc2

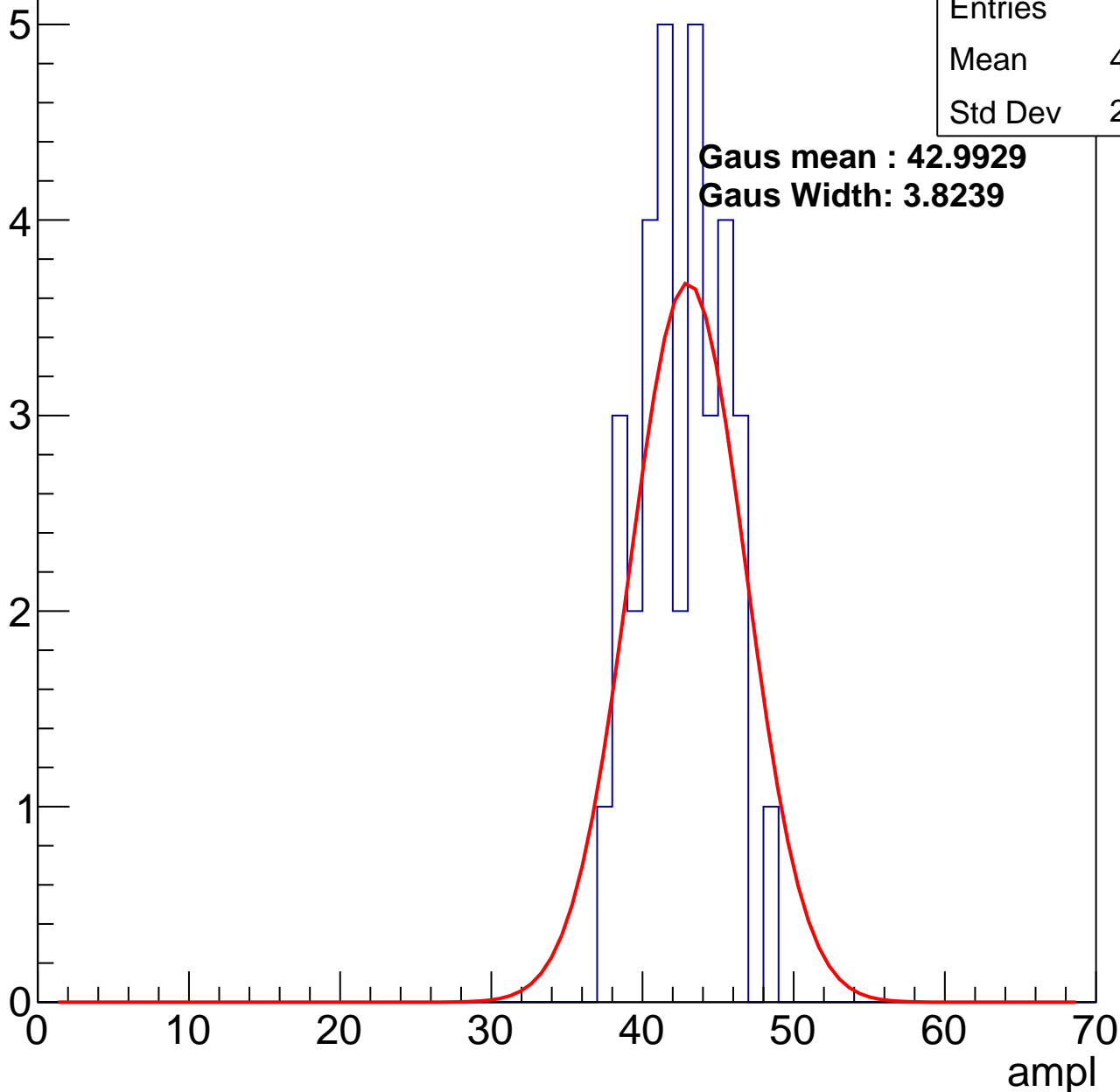
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	33
Mean	42.15
Std Dev	2.743

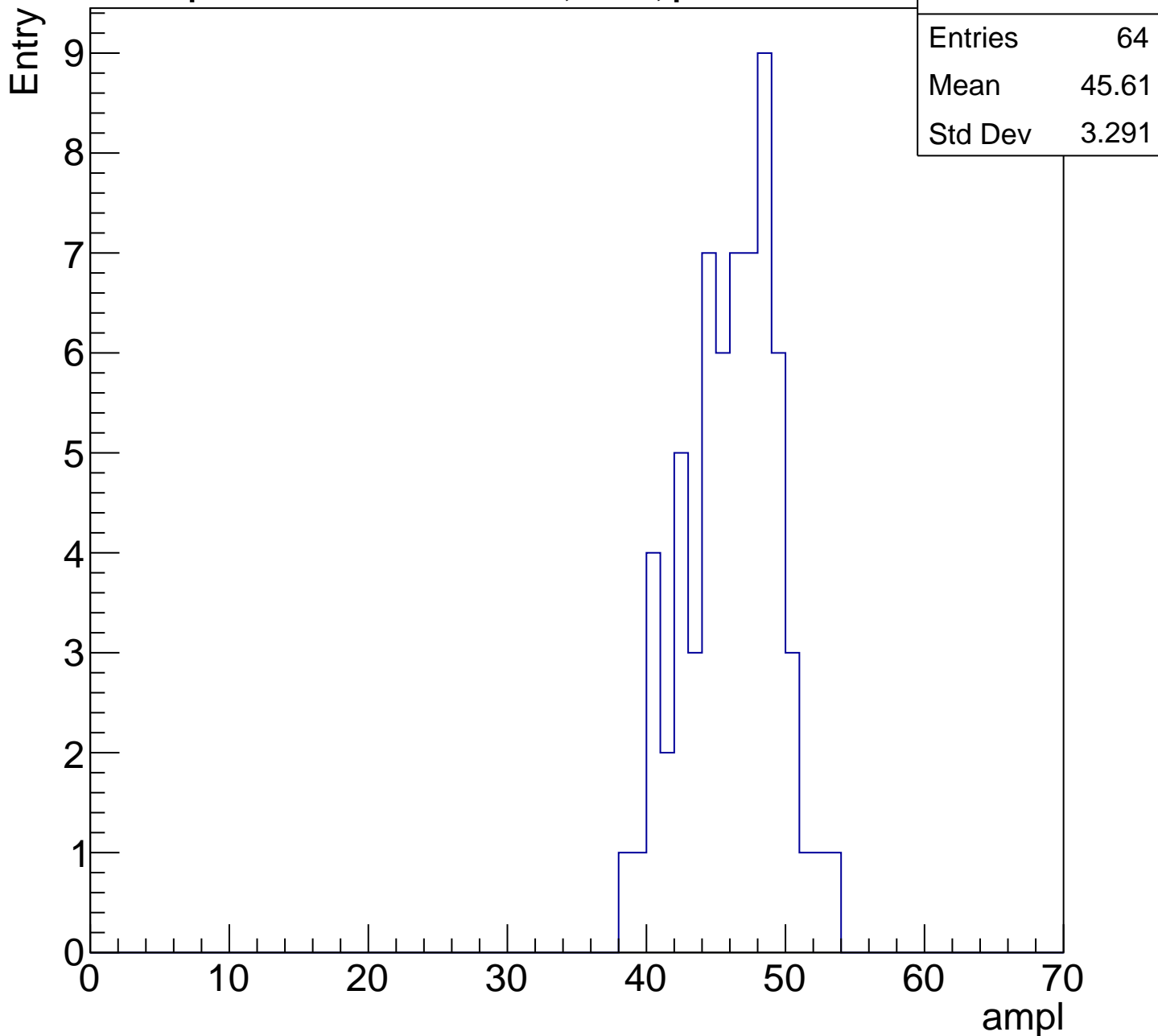
**Gaus mean : 42.9929**

**Gaus Width: 3.8239**



# B1L100S, U6-ch28, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2



# B1L100S, U6-ch28, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	69
Mean	53.1
Std Dev	3.06

Entry

10

8

6

4

2

0

0

10

20

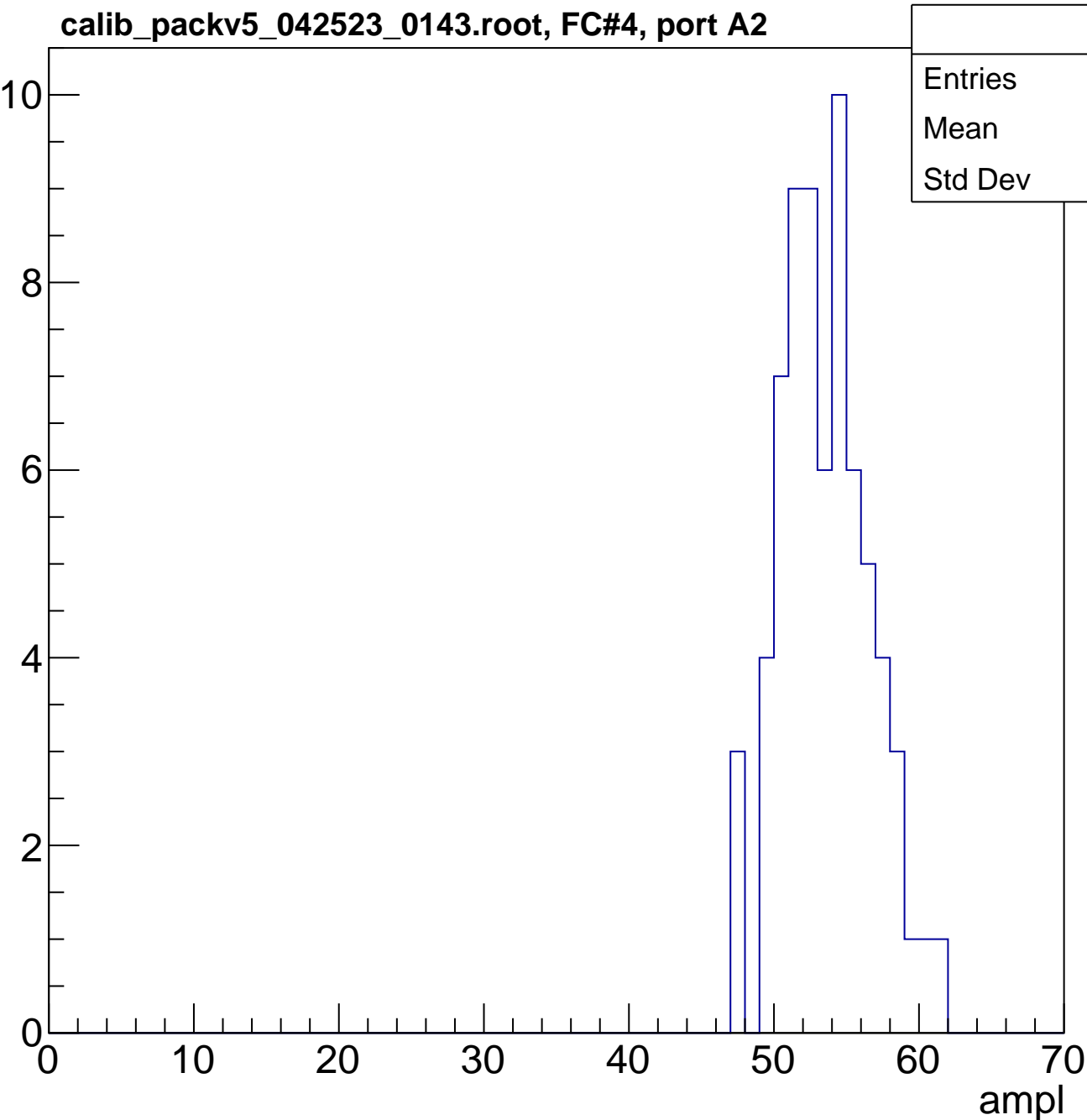
30

40

50

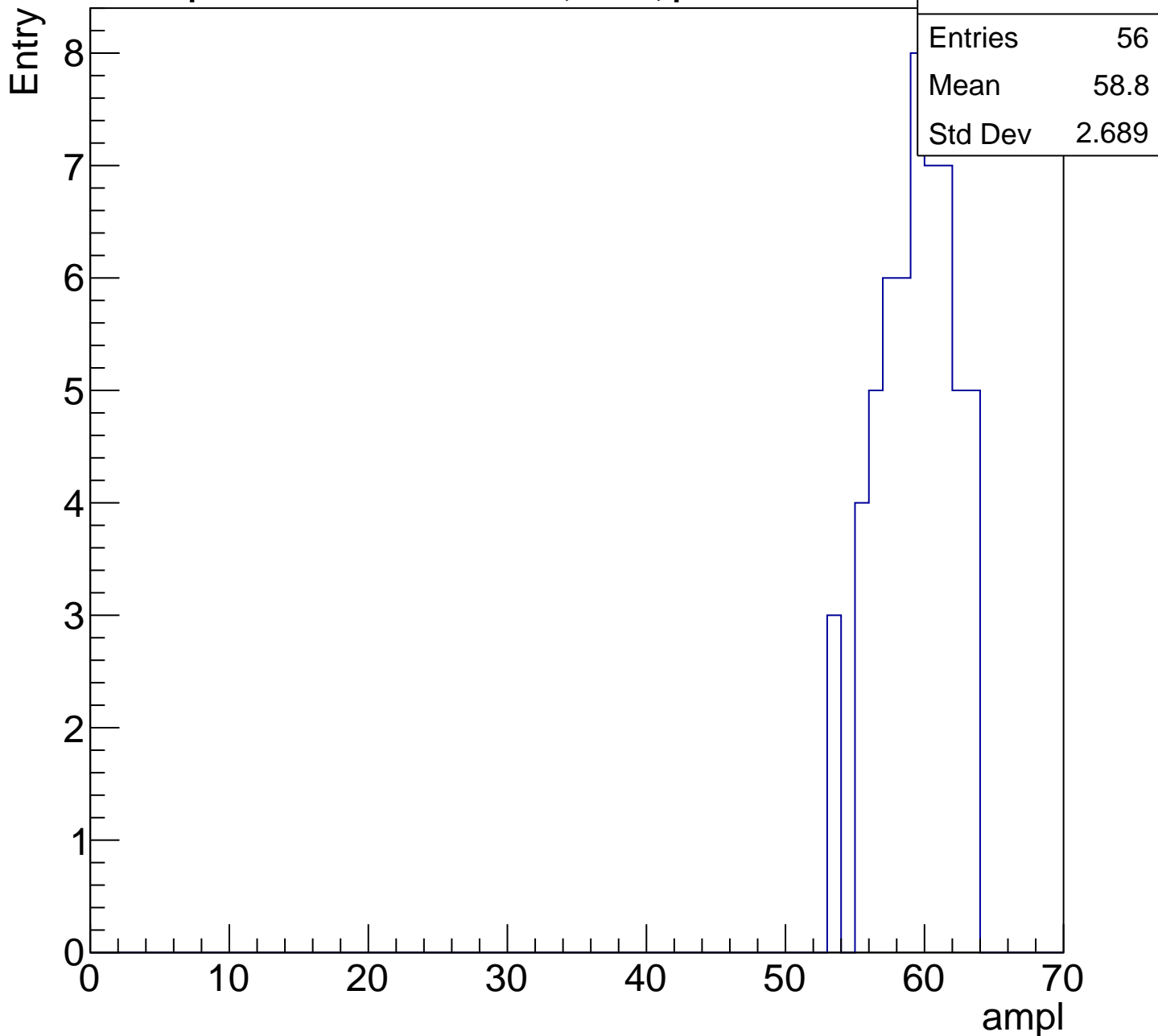
60

ampl



# B1L100S, U6-ch28, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

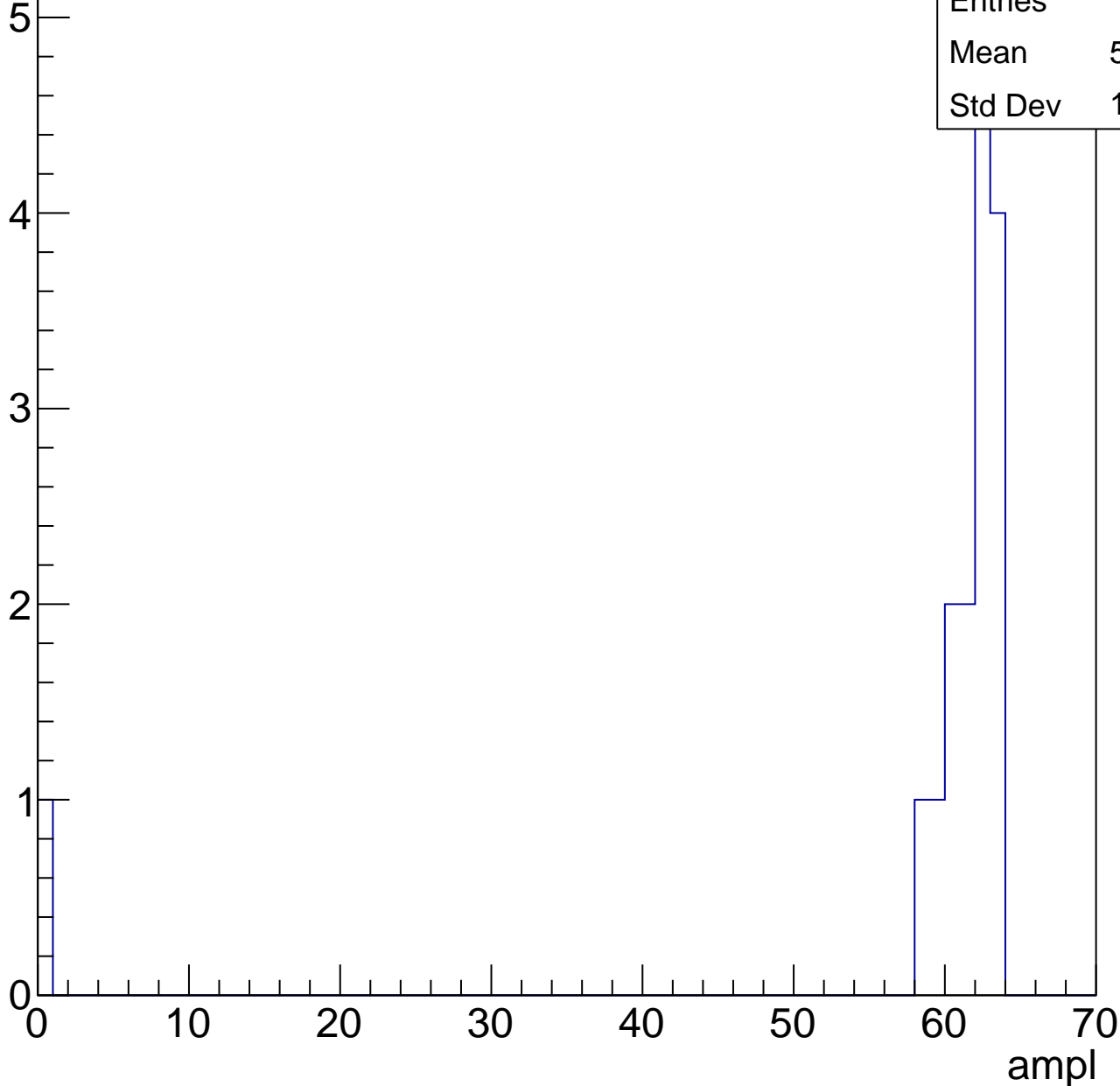


# B1L100S, U6-ch28, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	16
Mean	57.56
Std Dev	14.93

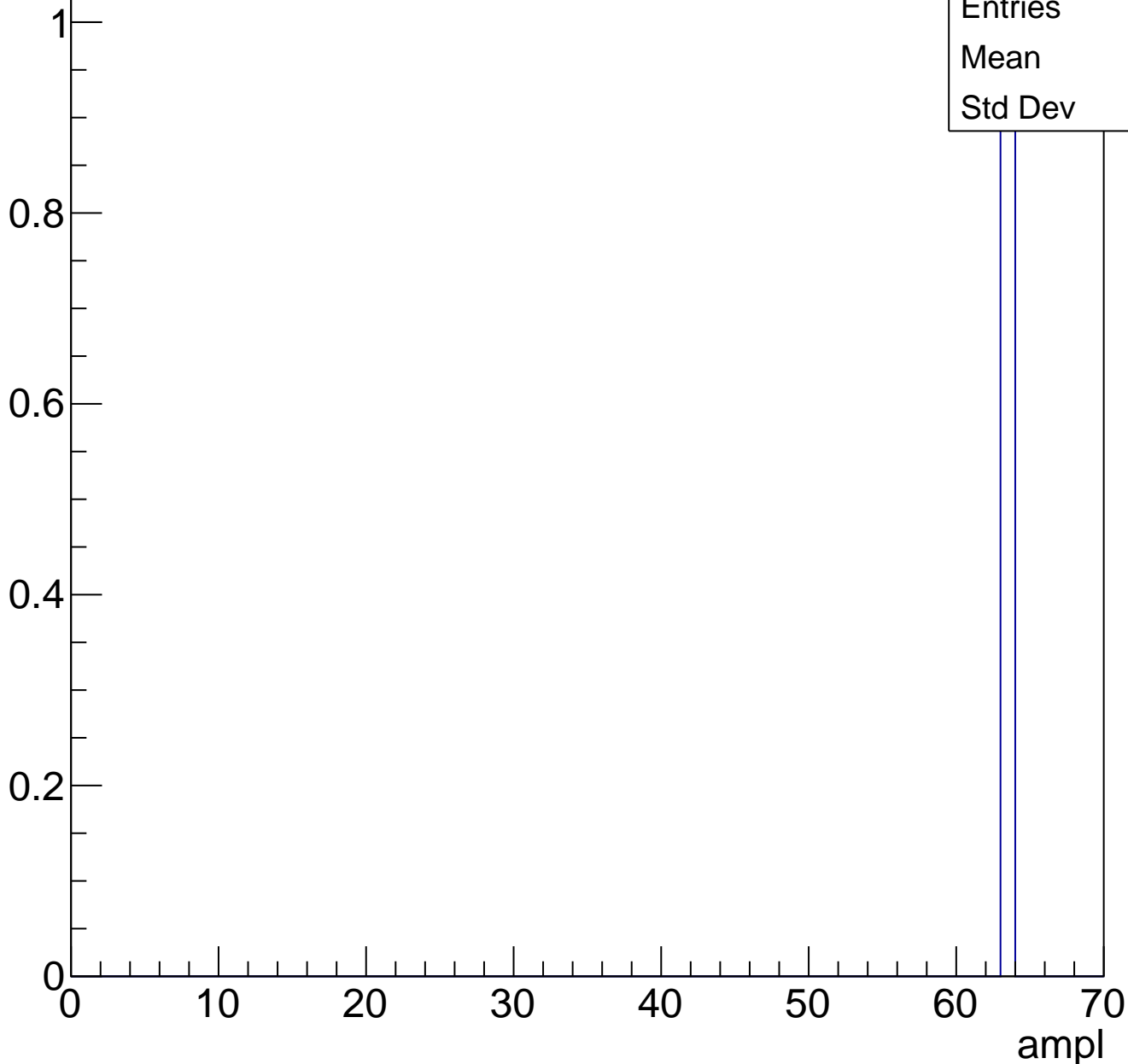




# B1L100S, U6-ch28, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



# B1L100S, U6-ch29, adc0

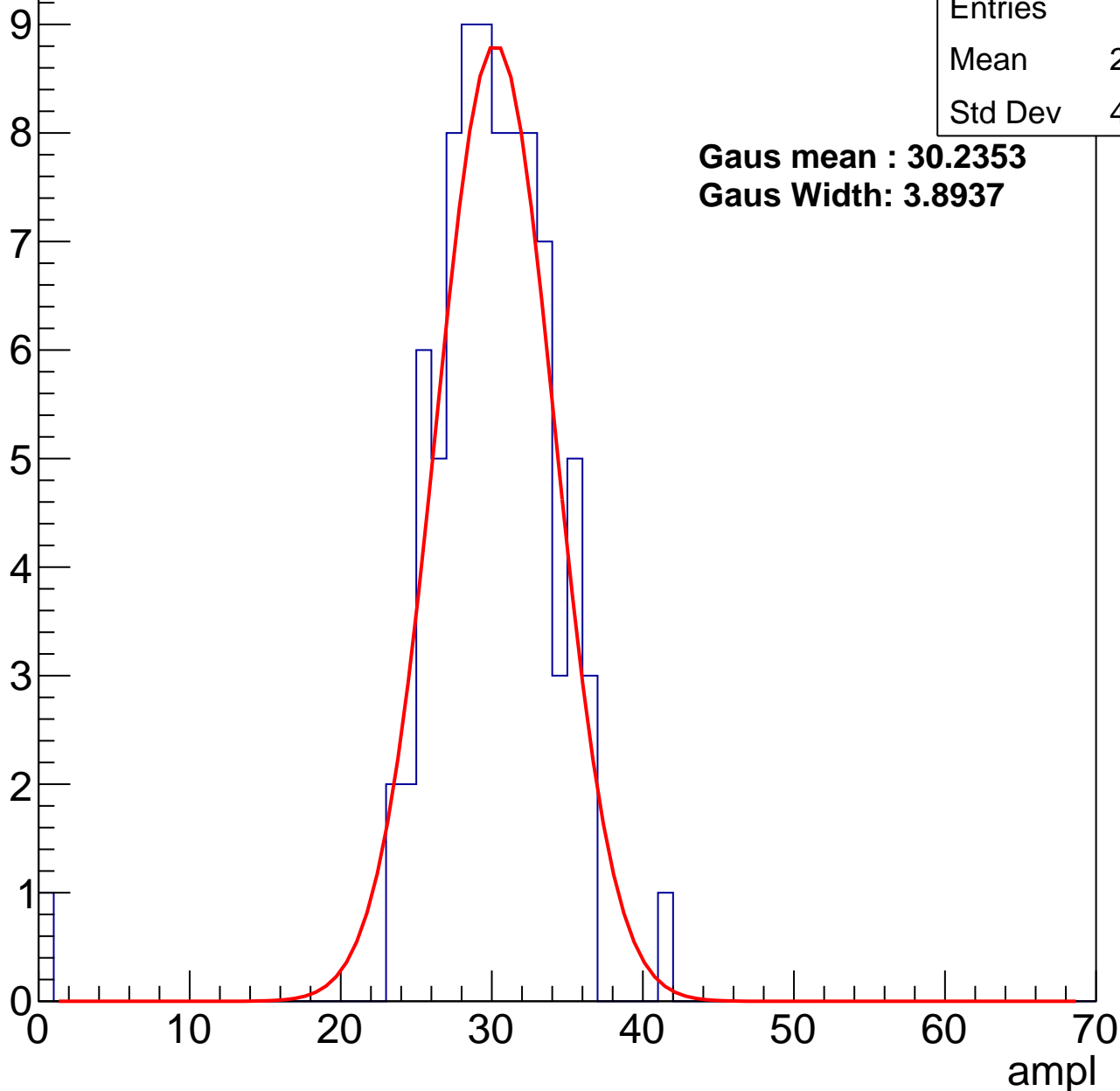
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	85
Mean	29.46
Std Dev	4.724

**Gaus mean : 30.2353**

**Gaus Width: 3.8937**



# B1L100S, U6-ch29, adc1

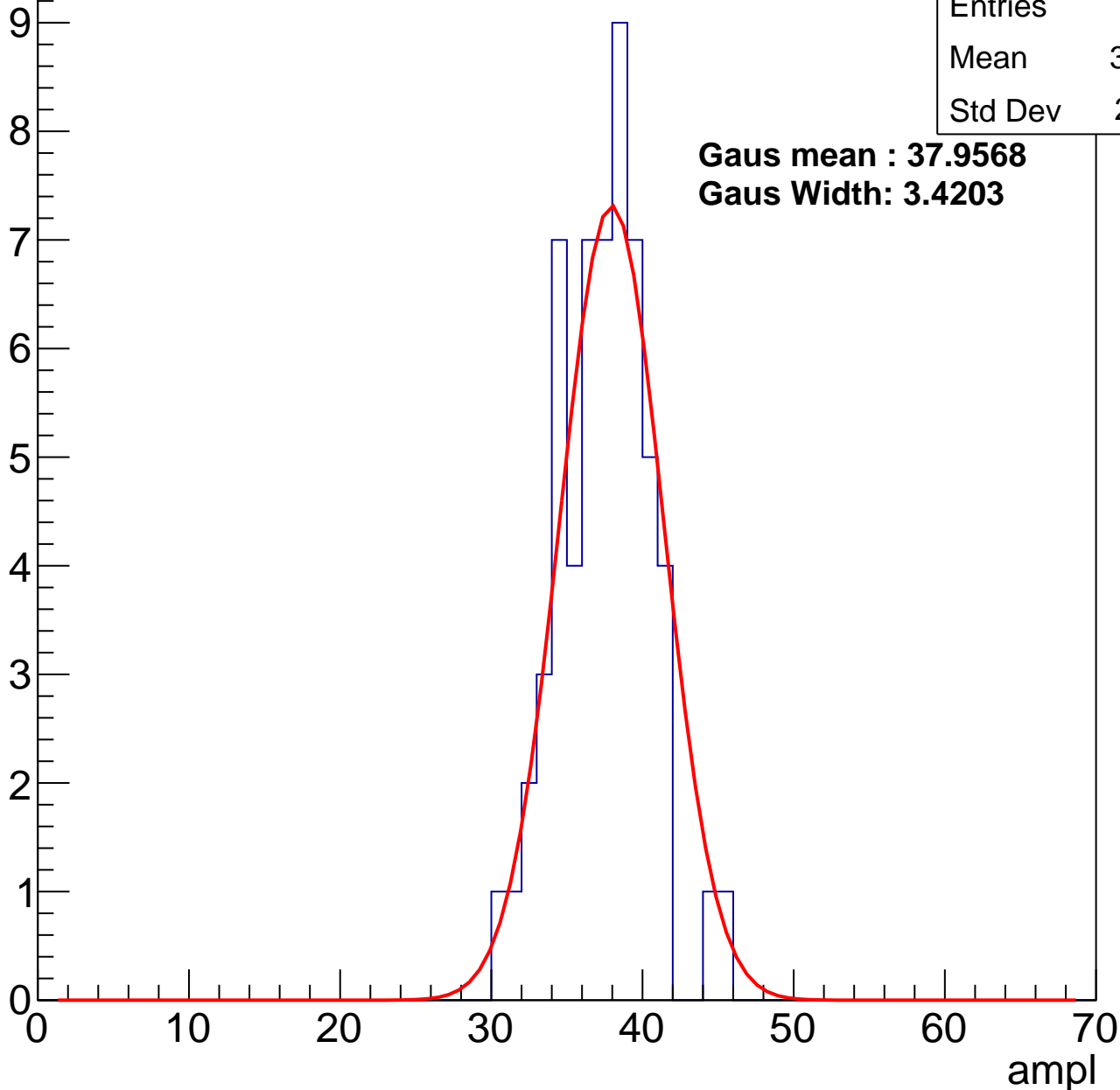
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	59
Mean	36.97
Std Dev	2.991

**Gaus mean : 37.9568**

**Gaus Width: 3.4203**



# B1L100S, U6-ch29, adc2

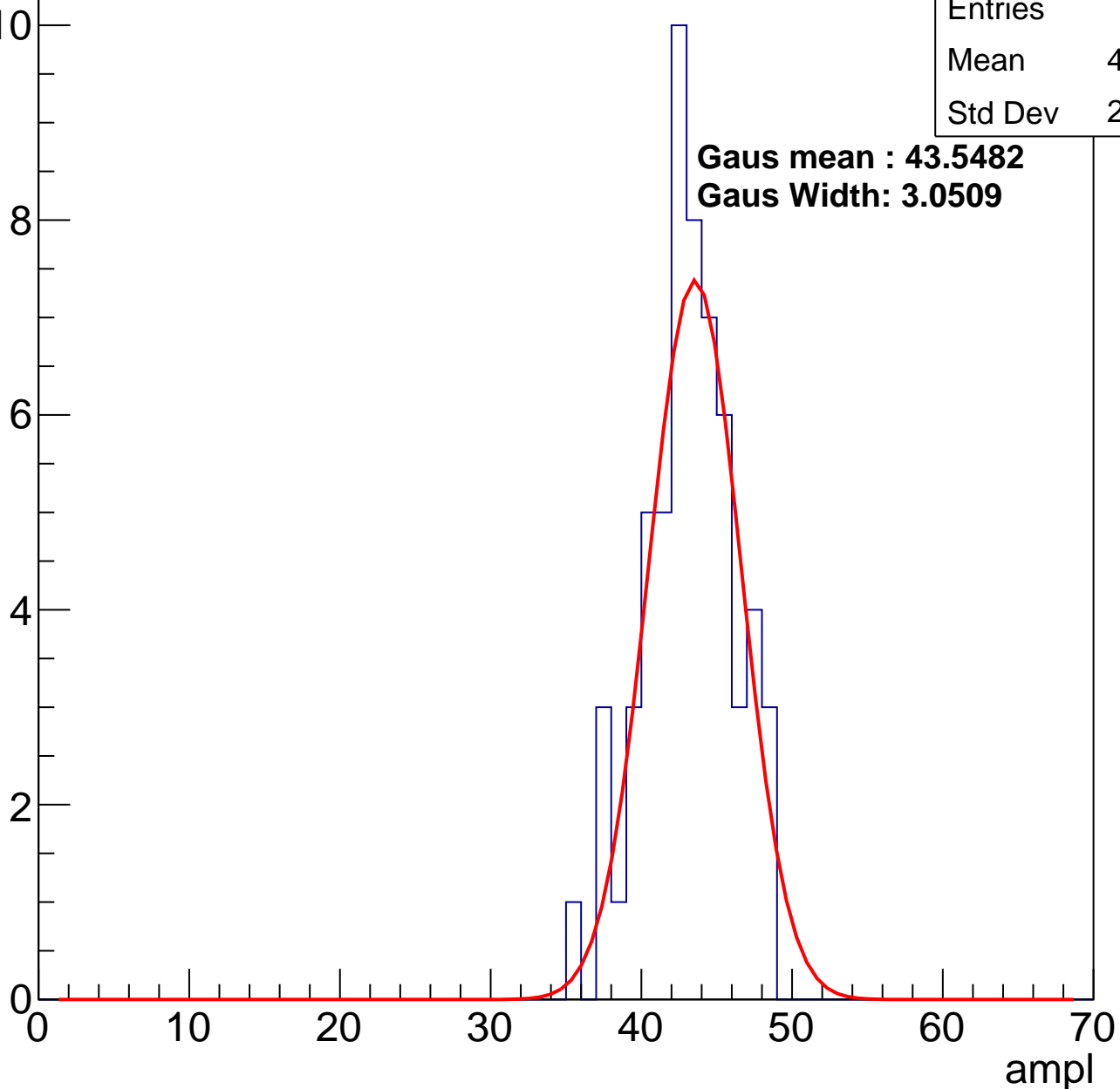
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	59
Mean	42.68
Std Dev	2.943

**Gaus mean : 43.5482**

**Gaus Width: 3.0509**

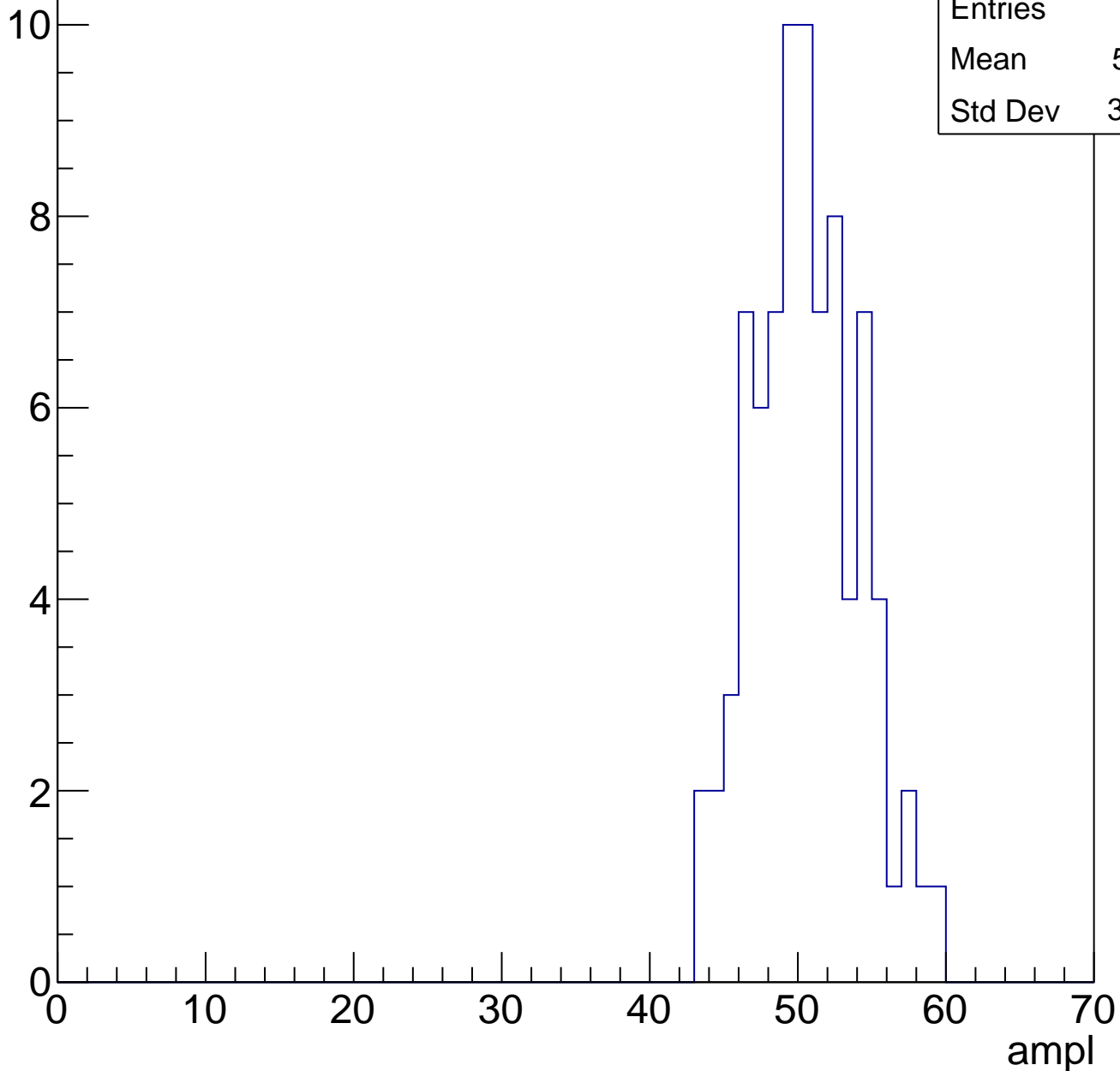


# B1L100S, U6-ch29, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

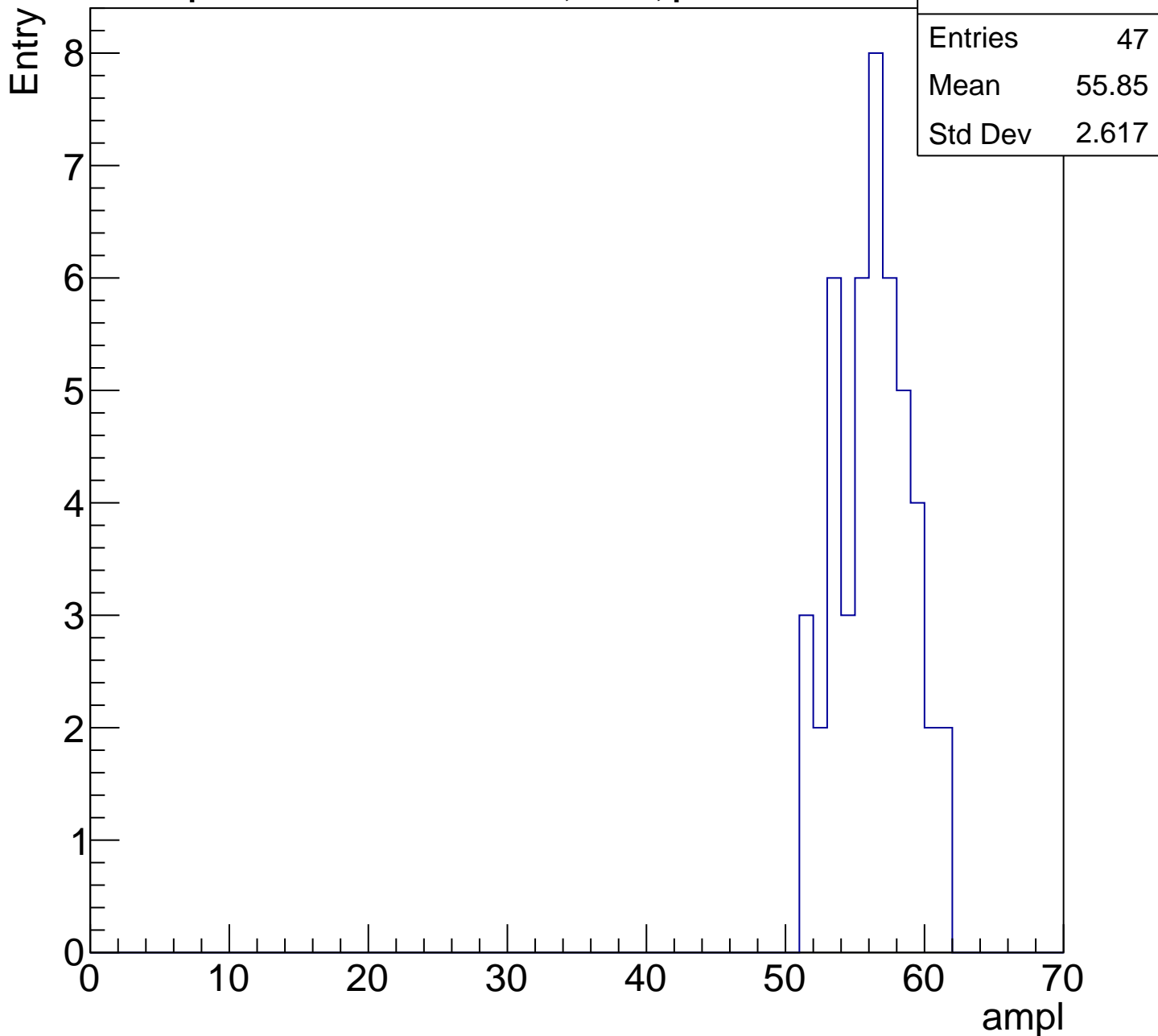
Entries	82
Mean	50.11
Std Dev	3.517

Entry



# B1L100S, U6-ch29, adc4

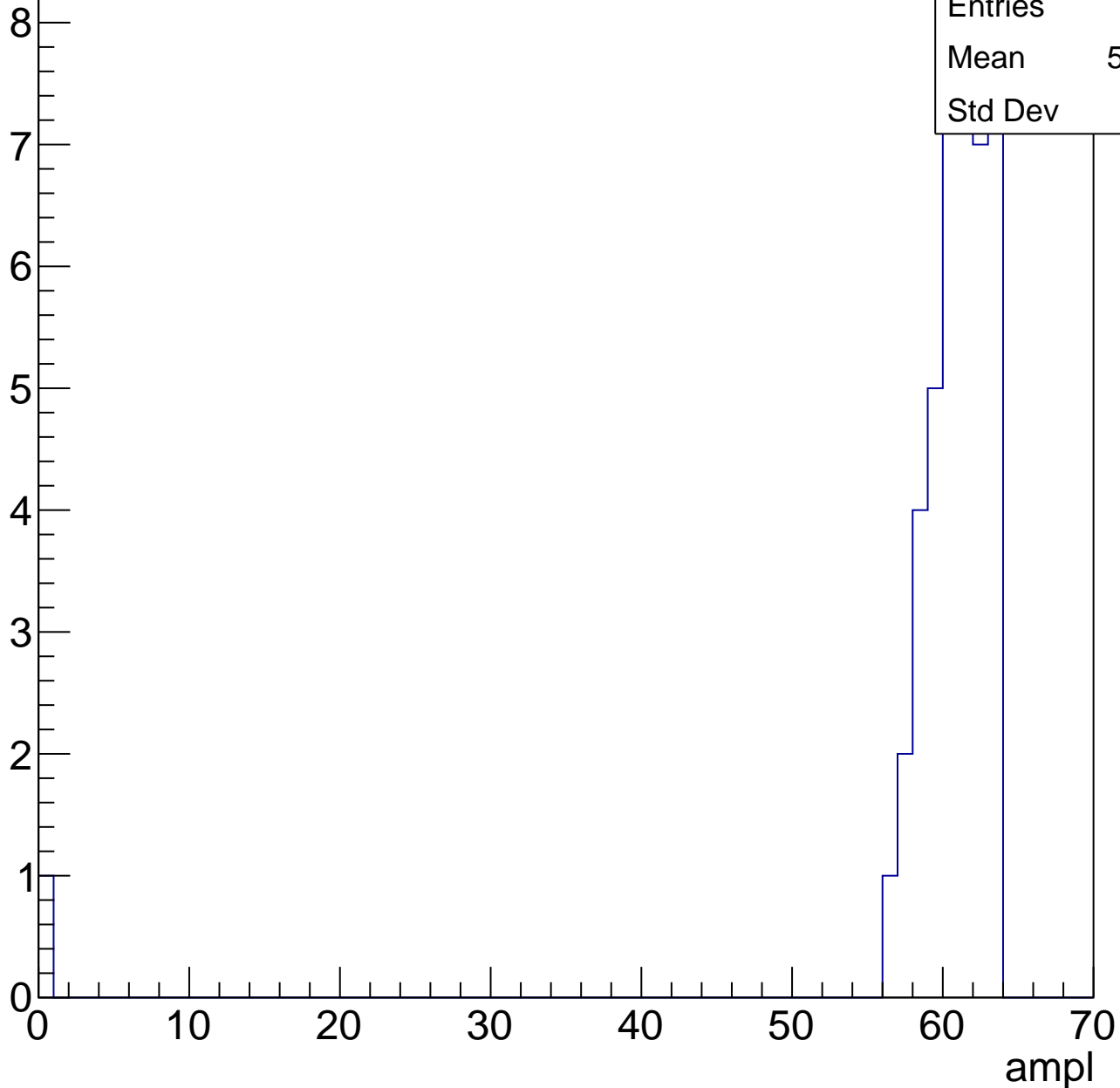
calib\_packv5\_042523\_0143.root, FC#4, port A2



# B1L100S, U6-ch29, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

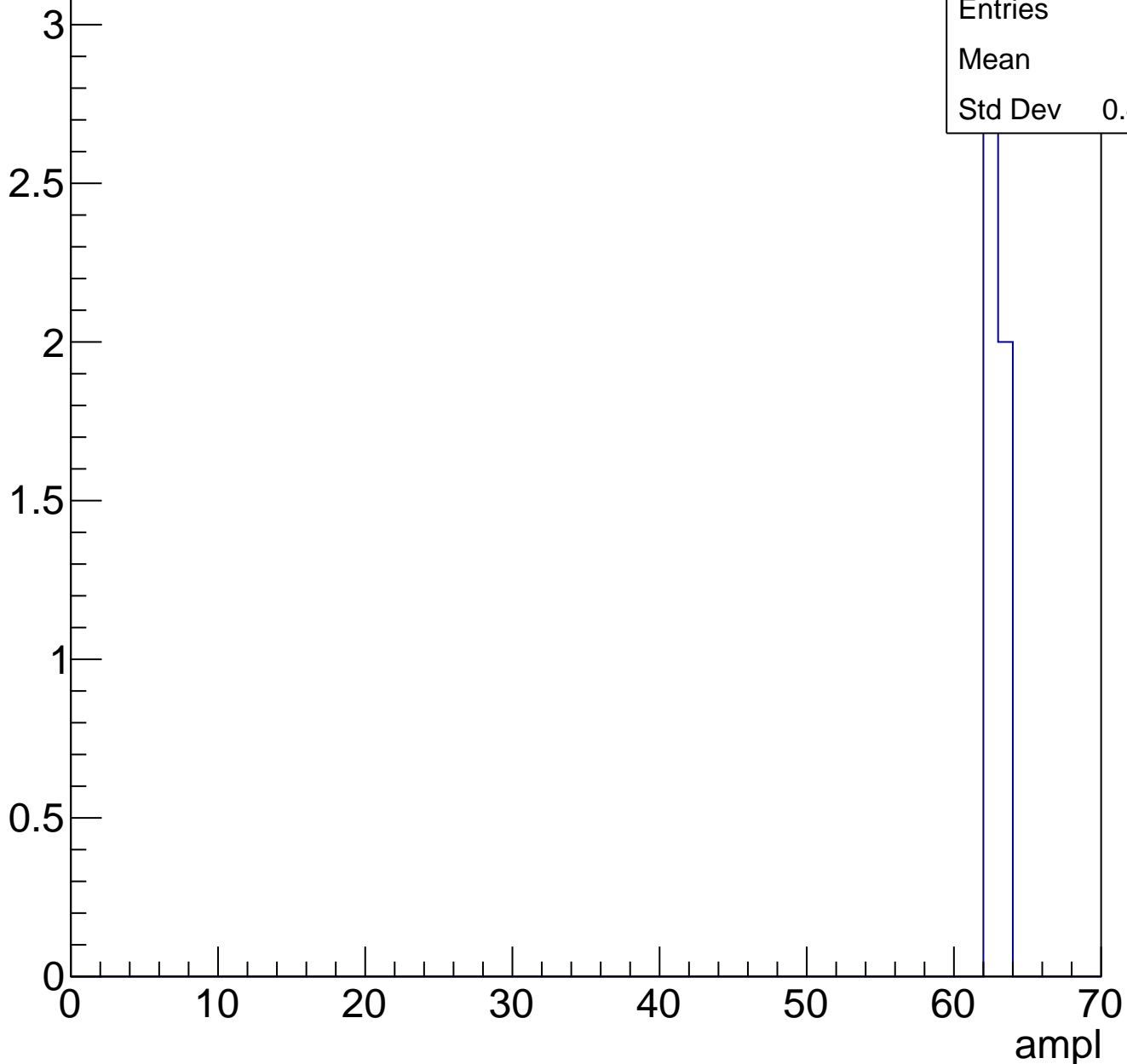


Entries	44
Mean	59.16
Std Dev	9.21

# B1L100S, U6-ch29, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry





# B1L100S, U6-ch29, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



# B1L100S, U6-ch30, adc0

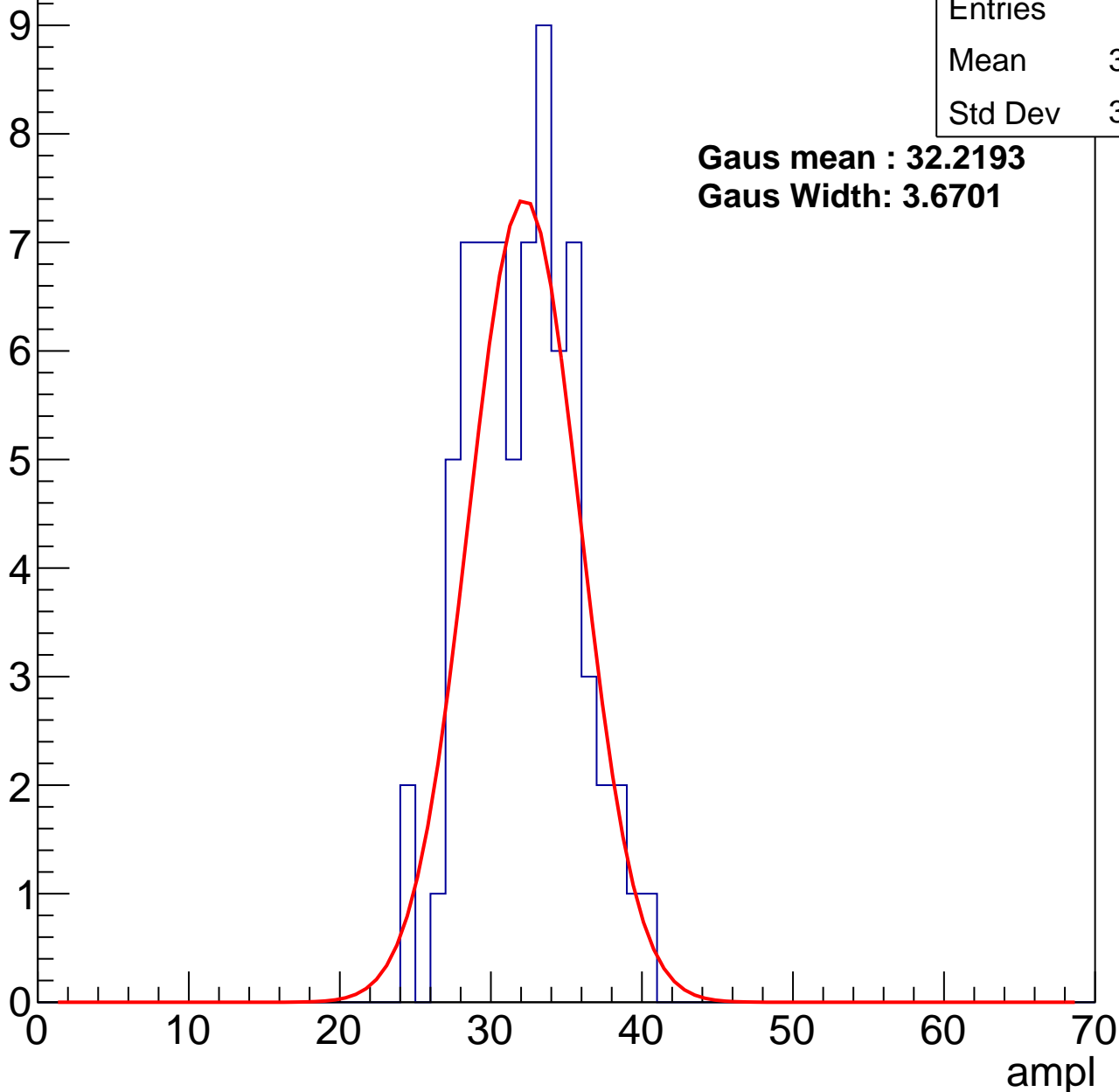
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	72
Mean	31.67
Std Dev	3.472

**Gaus mean : 32.2193**

**Gaus Width: 3.6701**



# B1L100S, U6-ch30, adc1

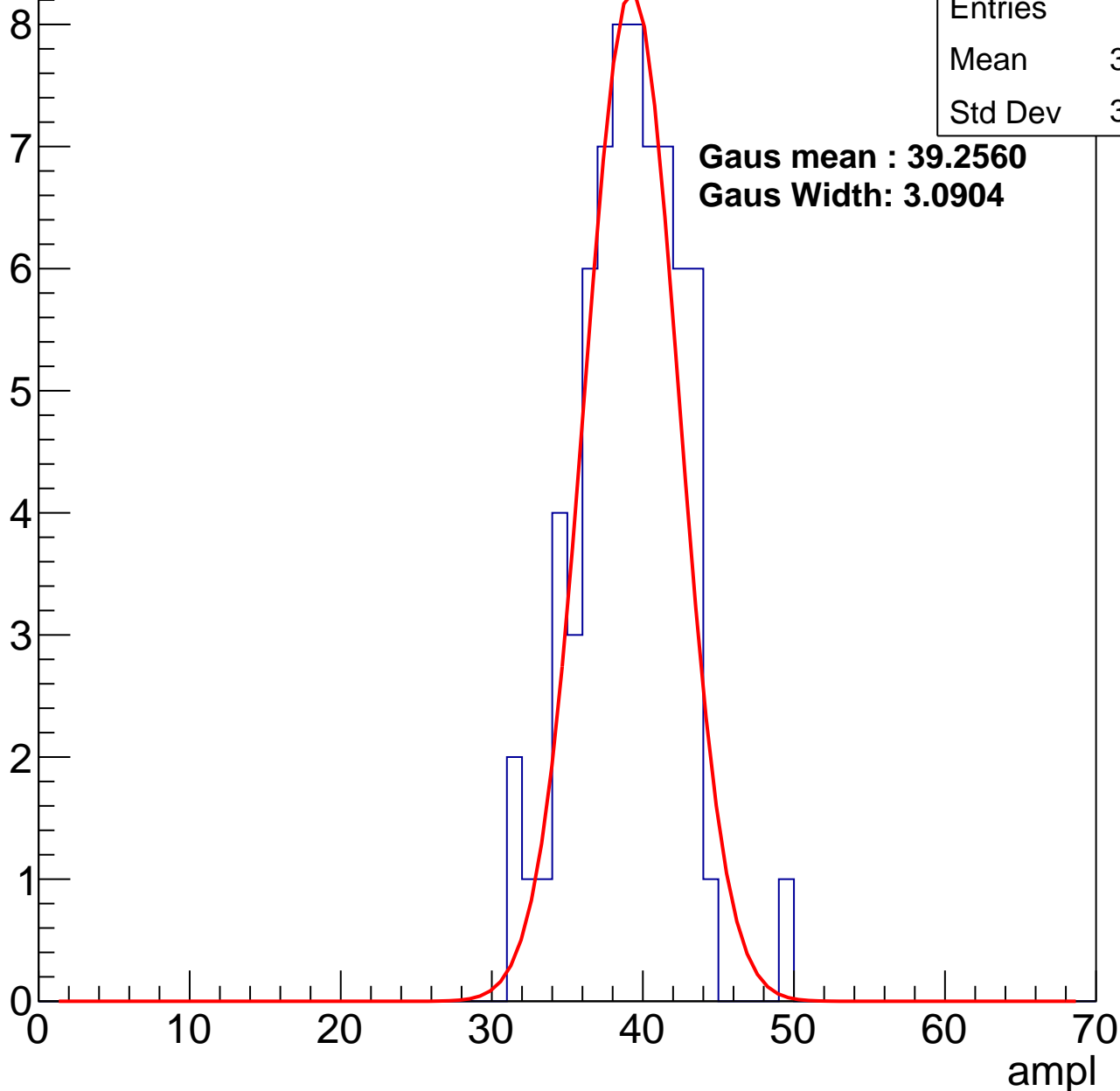
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	68
Mean	38.66
Std Dev	3.328

**Gaus mean : 39.2560**

**Gaus Width: 3.0904**



# B1L100S, U6-ch30, adc2

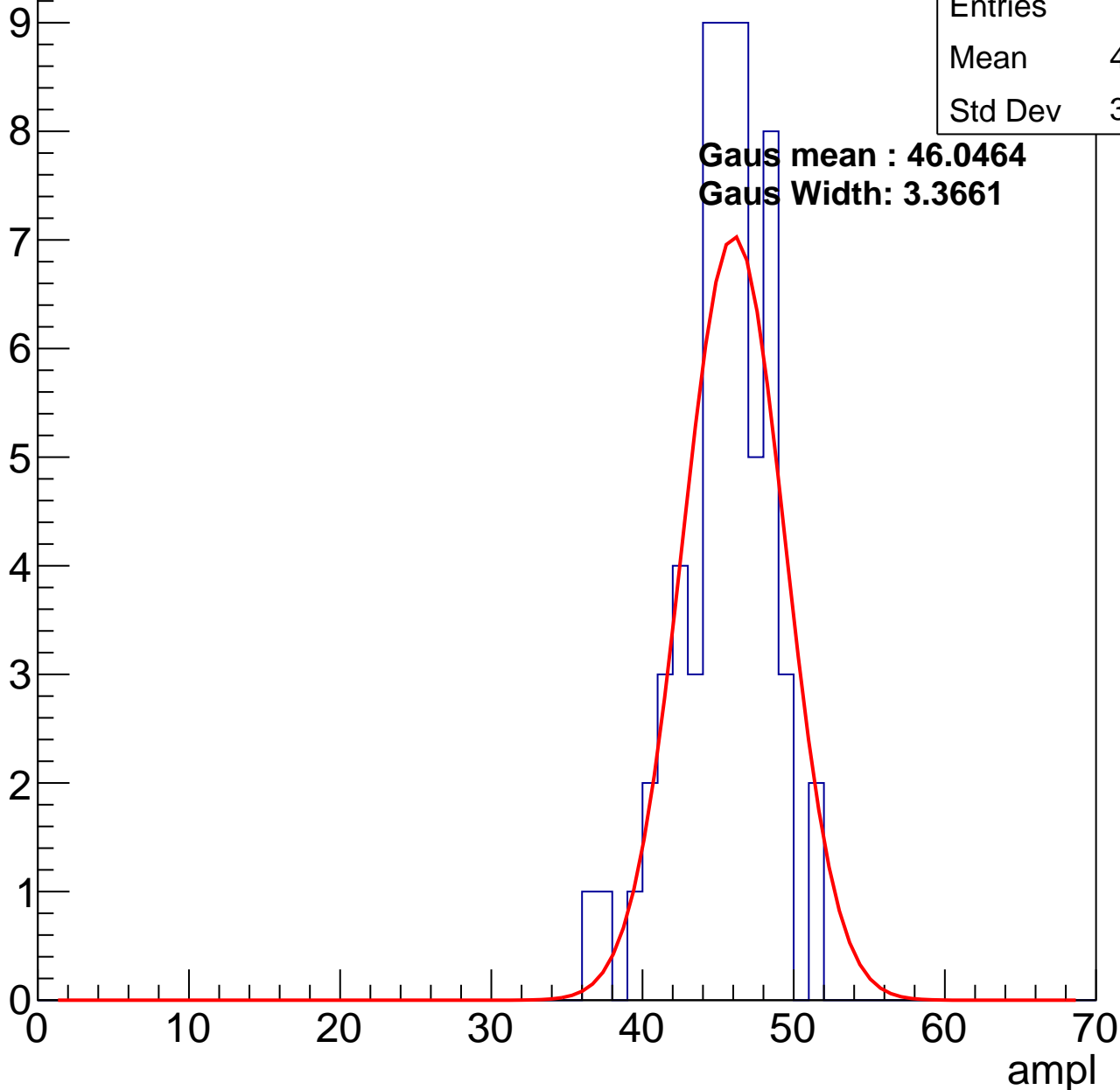
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	60
Mean	44.92
Std Dev	3.046

**Gaus mean : 46.0464**

**Gaus Width: 3.3661**

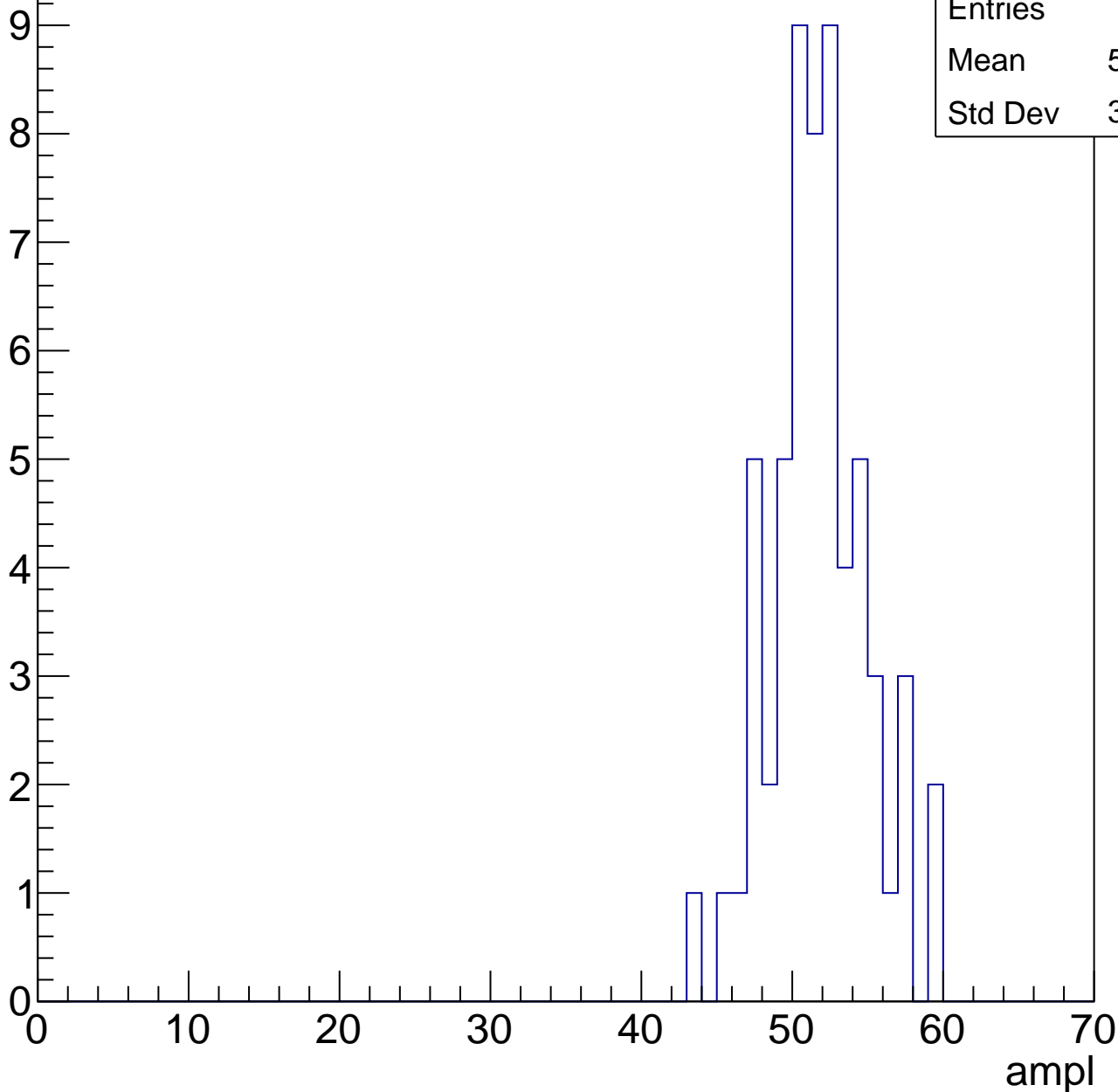


# B1L100S, U6-ch30, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	59
Mean	51.32
Std Dev	3.254

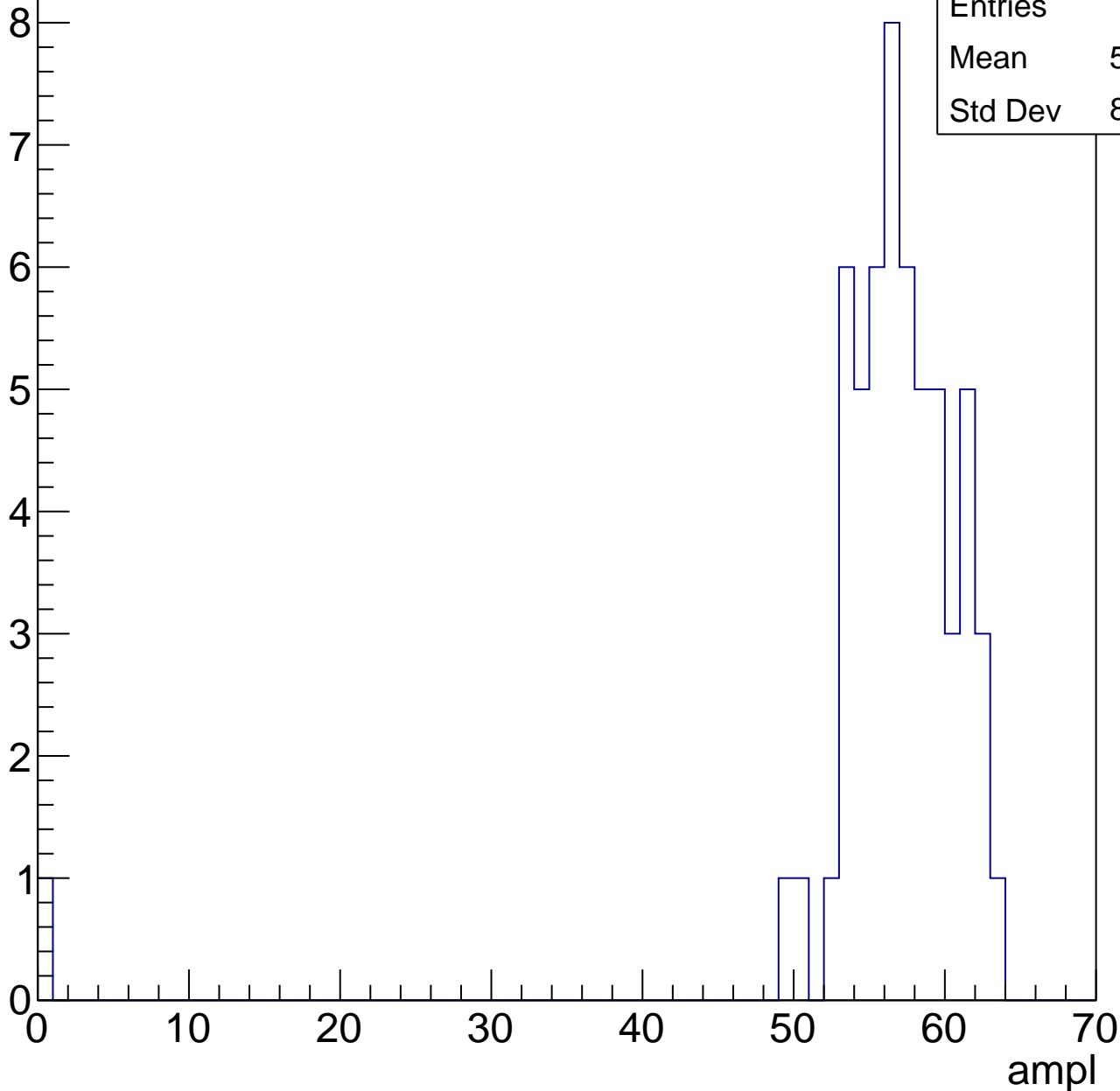


# B1L100S, U6-ch30, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

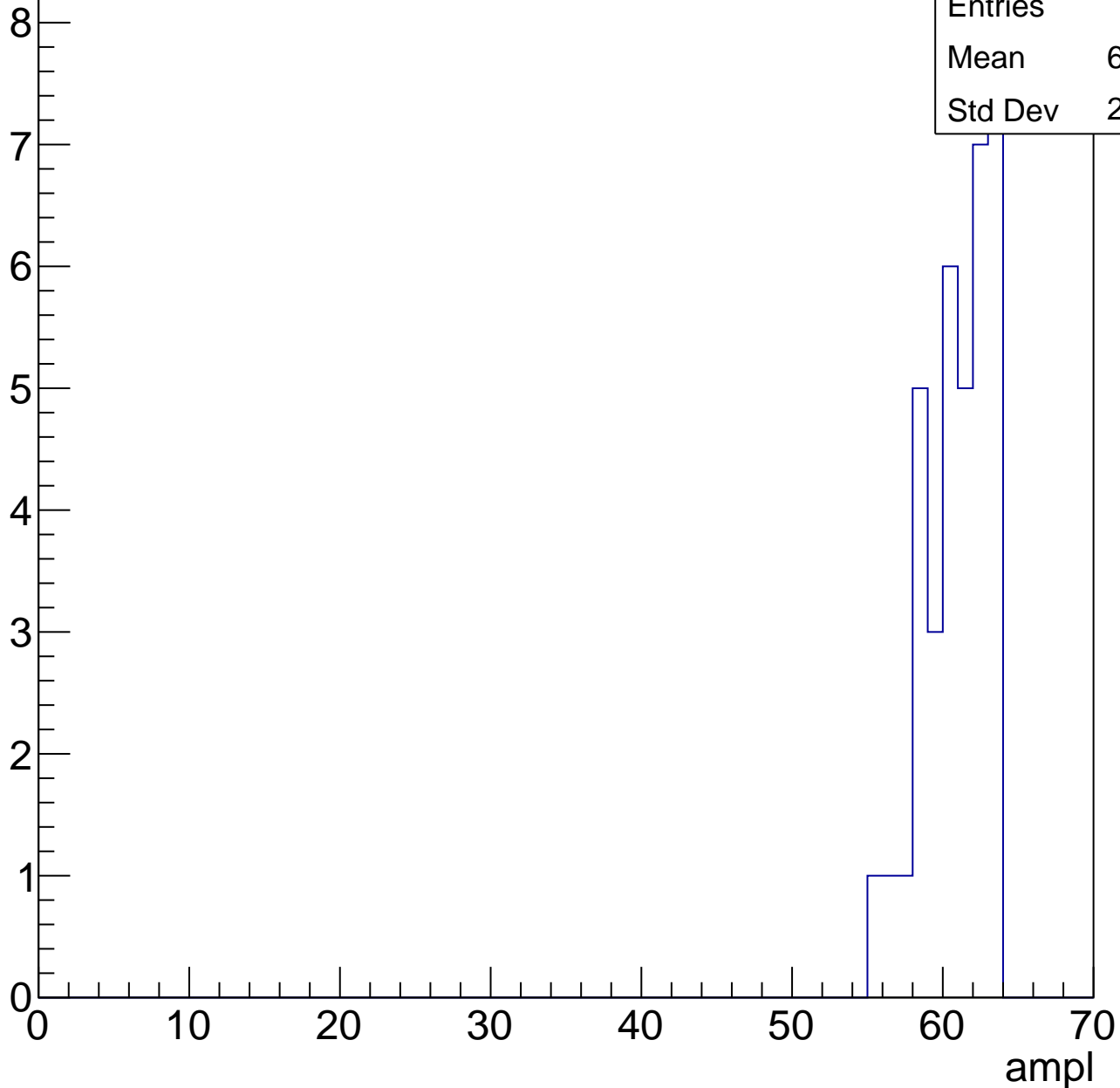
Entries	57
Mean	55.75
Std Dev	8.073



# B1L100S, U6-ch30, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



# B1L100S, U6-ch30, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry





# B1L100S, U6-ch30, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



# B1L100S, U6-ch31, adc0

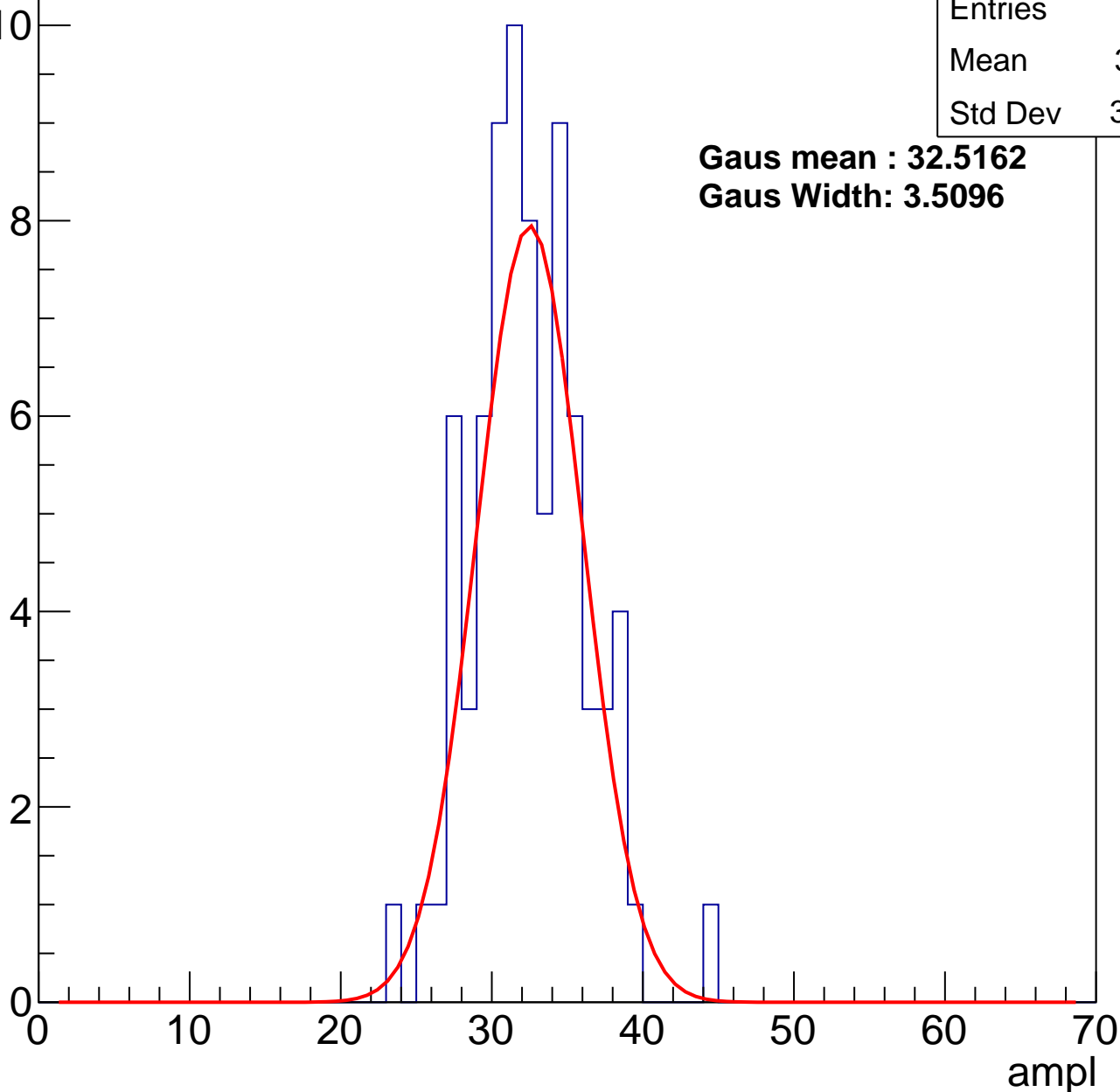
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	77
Mean	32.01
Std Dev	3.638

**Gaus mean : 32.5162**

**Gaus Width: 3.5096**



# B1L100S, U6-ch31, adc1

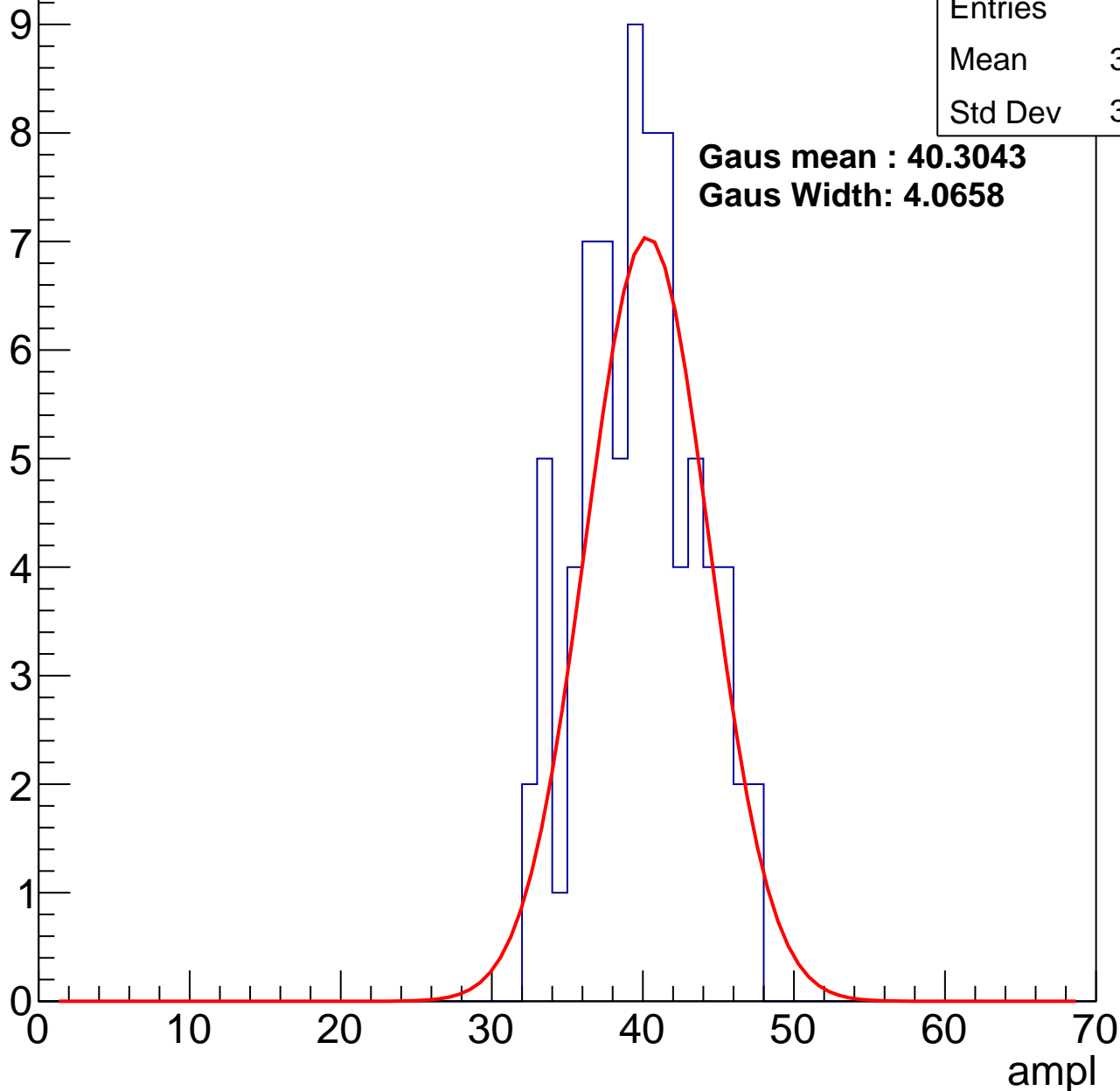
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	77
Mean	39.32
Std Dev	3.747

**Gaus mean : 40.3043**

**Gaus Width: 4.0658**



# B1L100S, U6-ch31, adc2

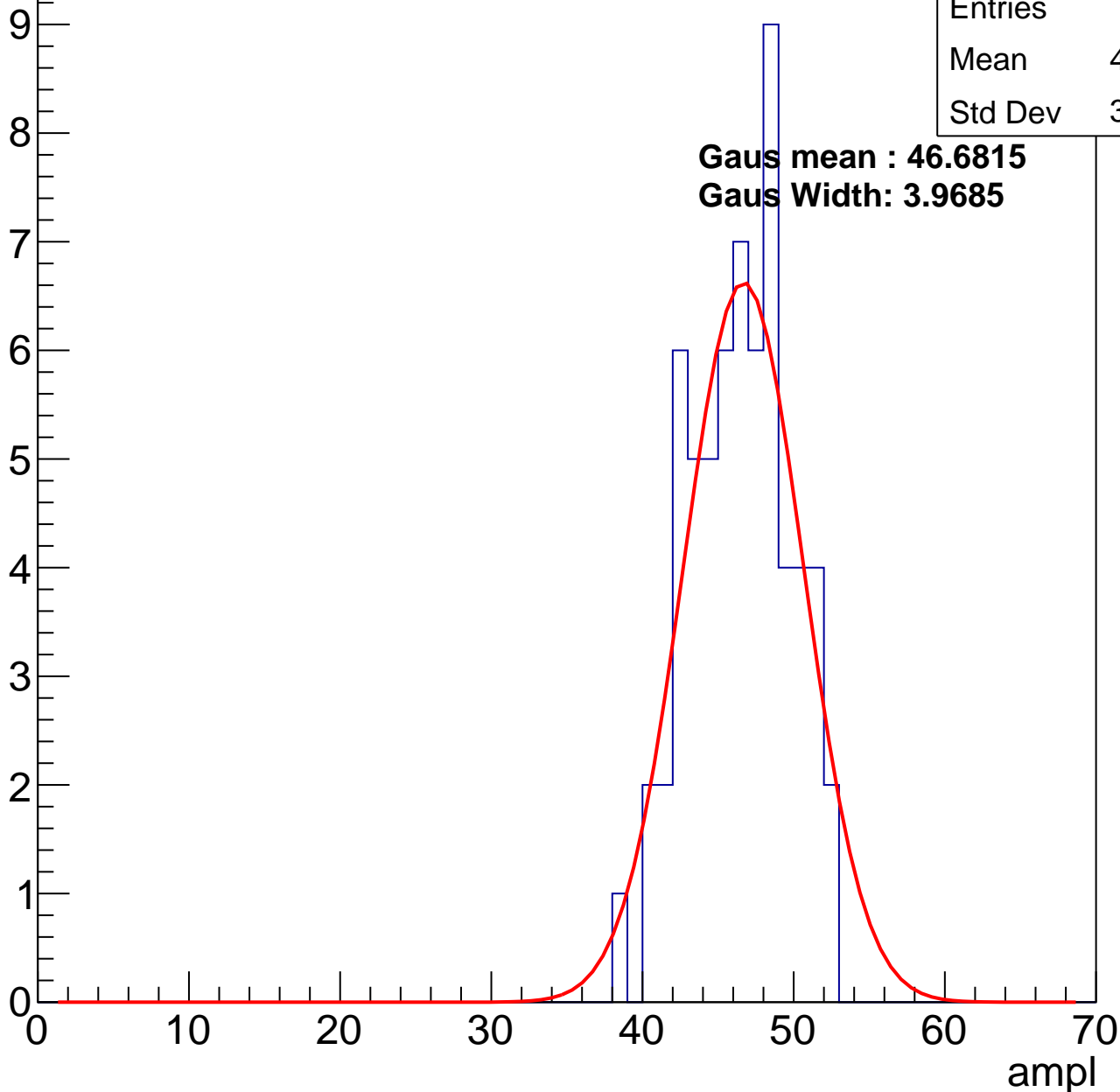
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	63
Mean	45.98
Std Dev	3.254

**Gaus mean : 46.6815**

**Gaus Width: 3.9685**

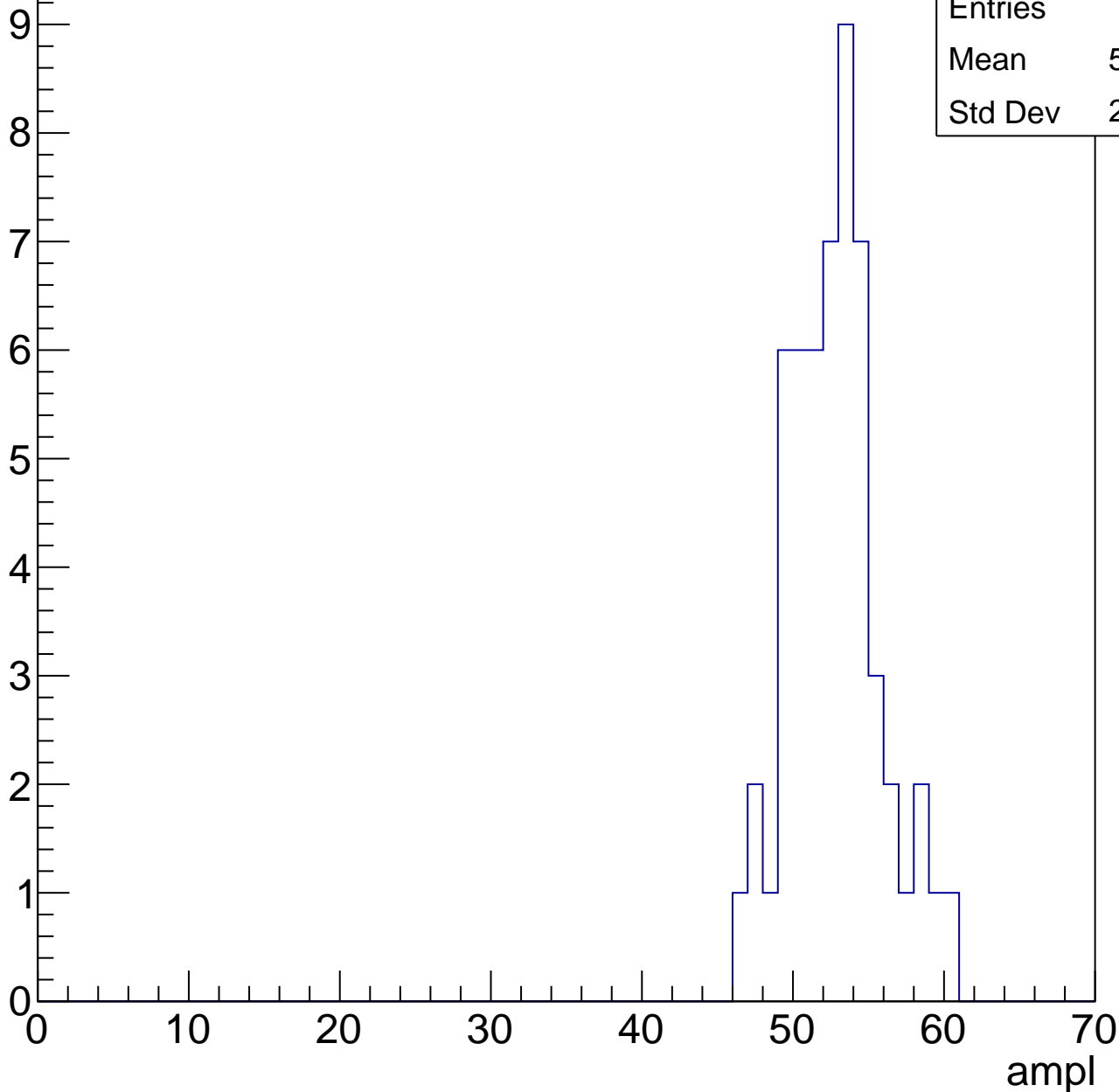


# B1L100S, U6-ch31, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

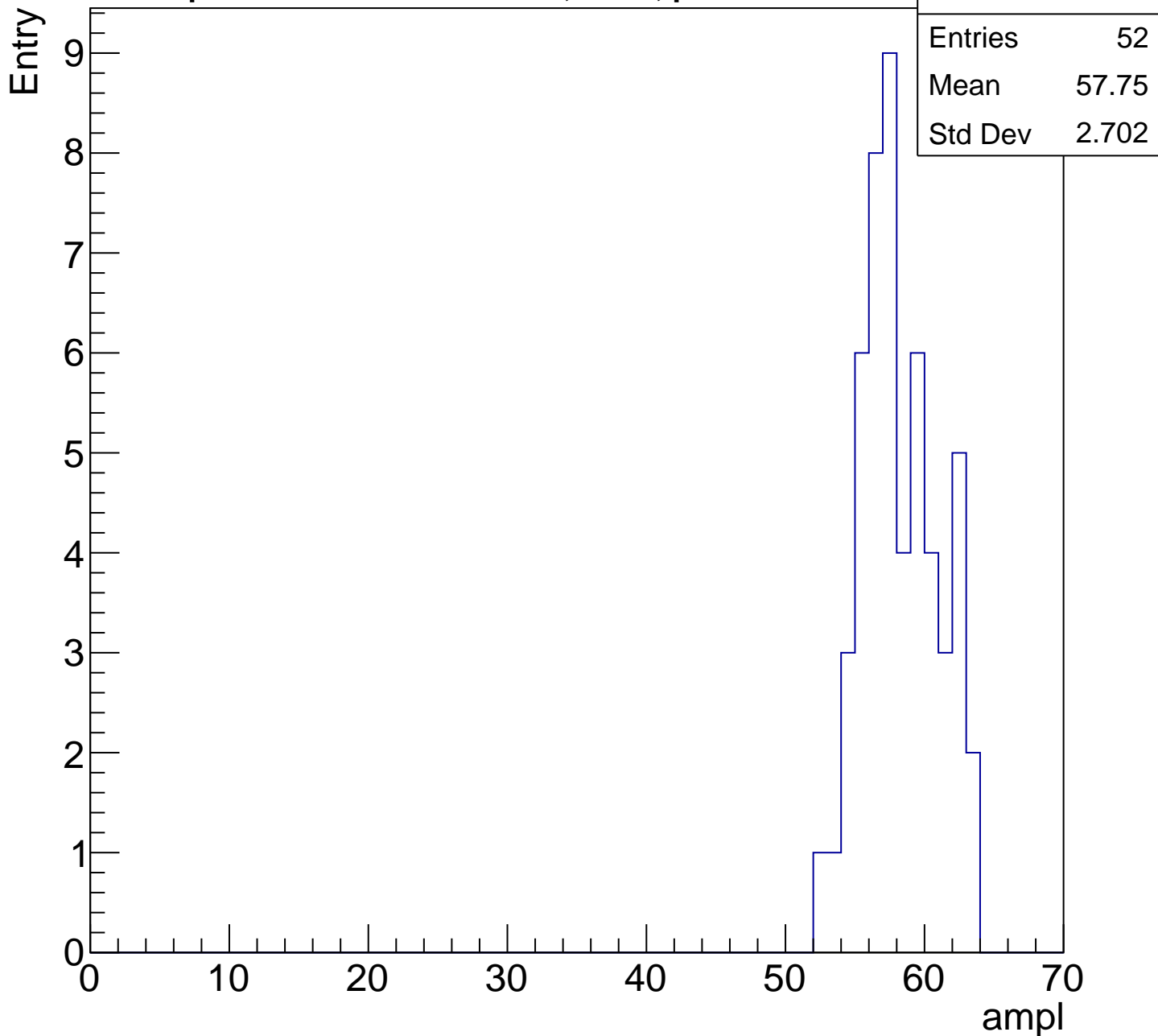
Entry

Entries	55
Mean	52.29
Std Dev	2.977



# B1L100S, U6-ch31, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

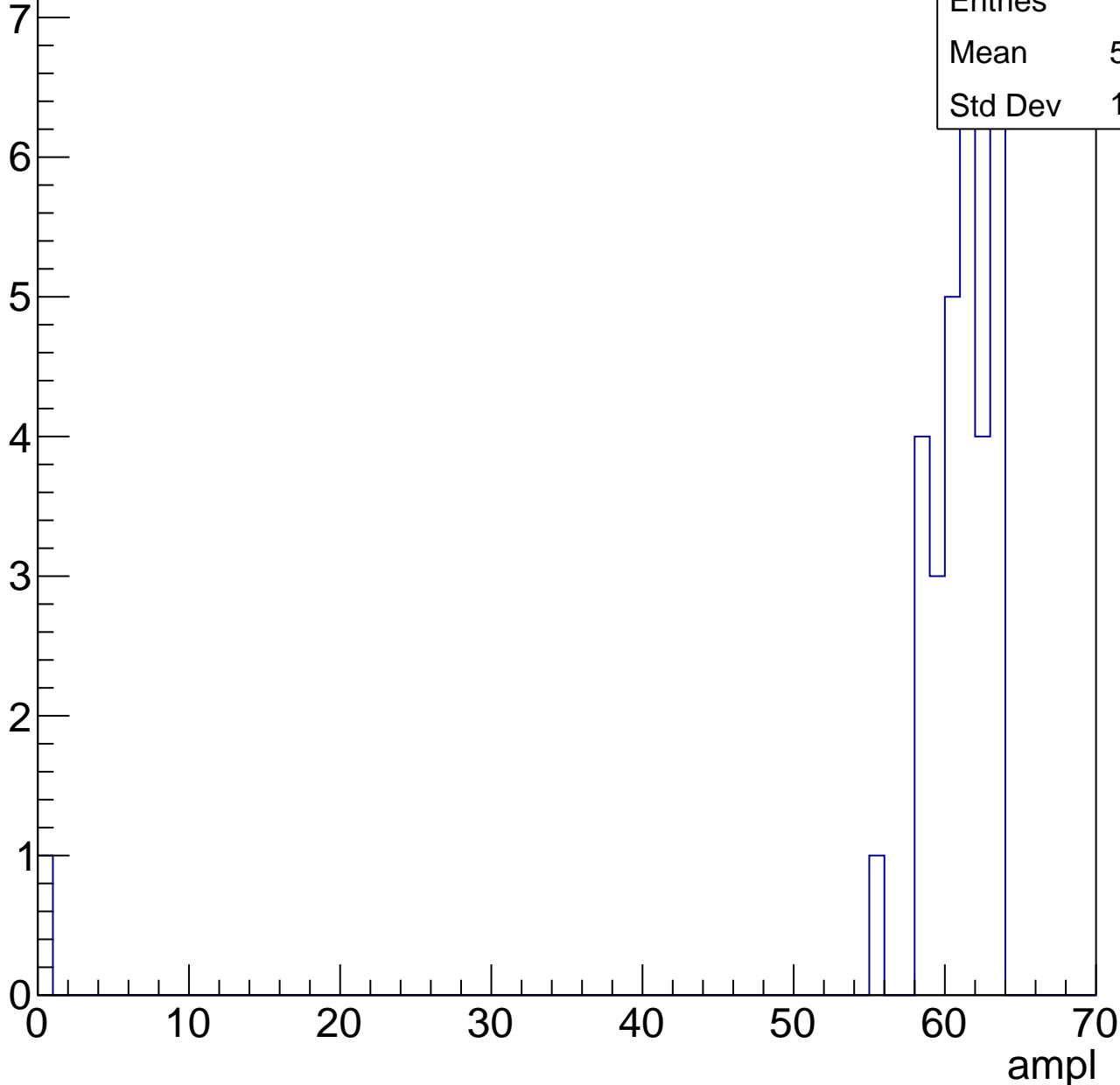


# B1L100S, U6-ch31, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	32
Mean	58.75
Std Dev	10.72



# B1L100S, U6-ch31, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry





# B1L100S, U6-ch31, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L100S, U6-ch32, adc0

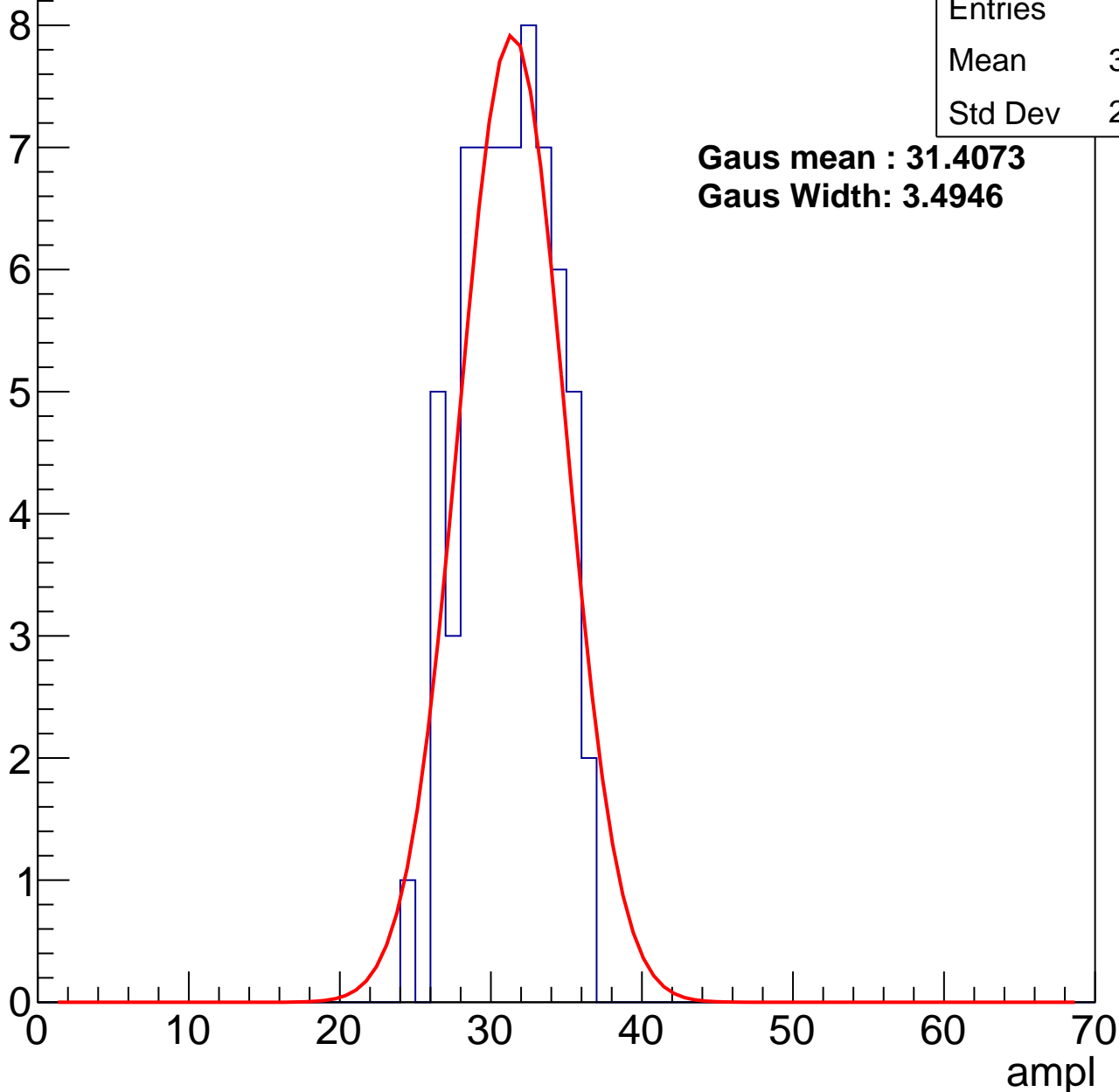
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	65
Mean	30.75
Std Dev	2.872

**Gaus mean : 31.4073**

**Gaus Width: 3.4946**



# B1L100S, U6-ch32, adc1

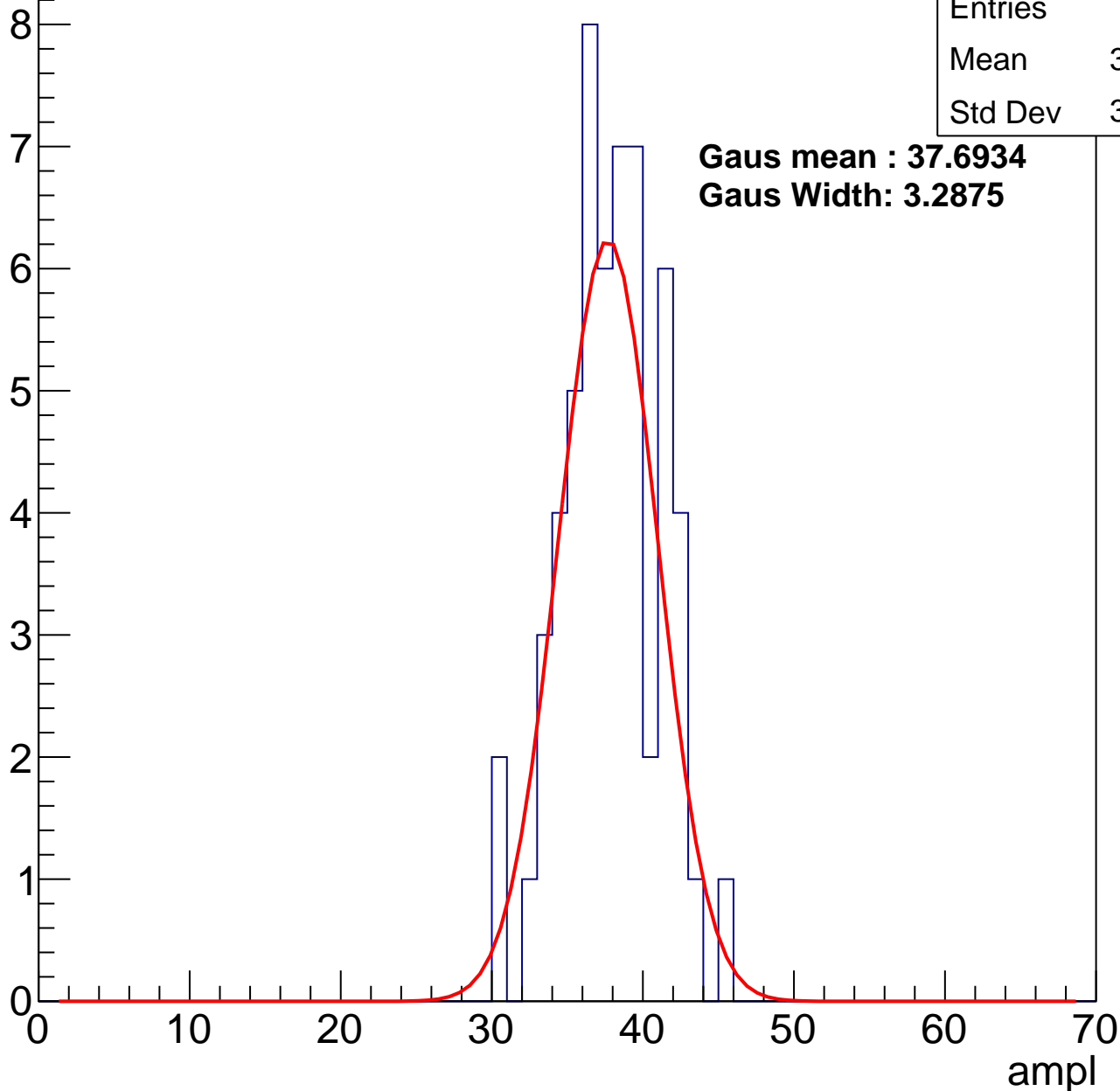
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	57
Mean	37.42
Std Dev	3.173

**Gaus mean : 37.6934**

**Gaus Width: 3.2875**



# B1L100S, U6-ch32, adc2

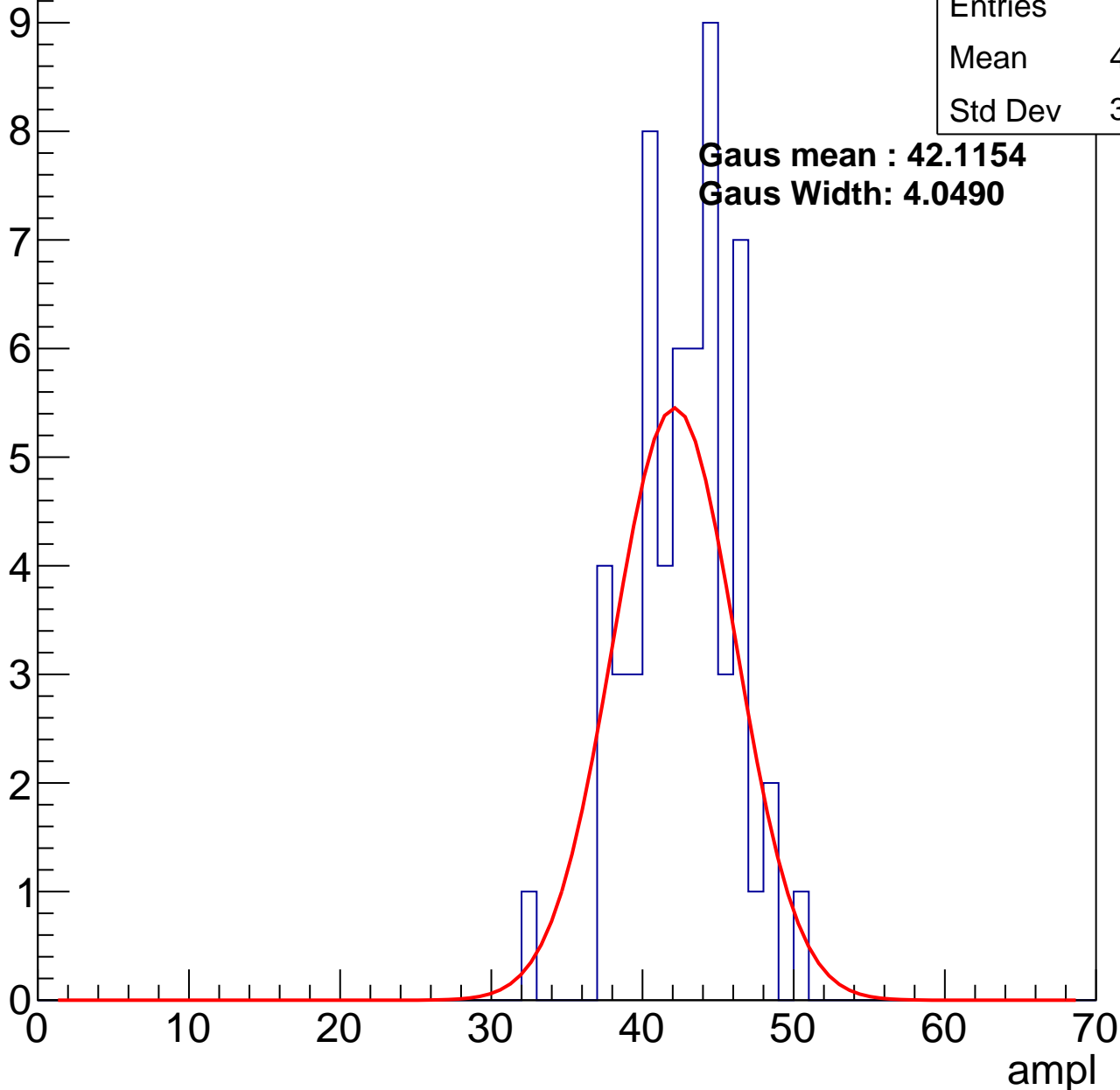
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	58
Mean	42.26
Std Dev	3.345

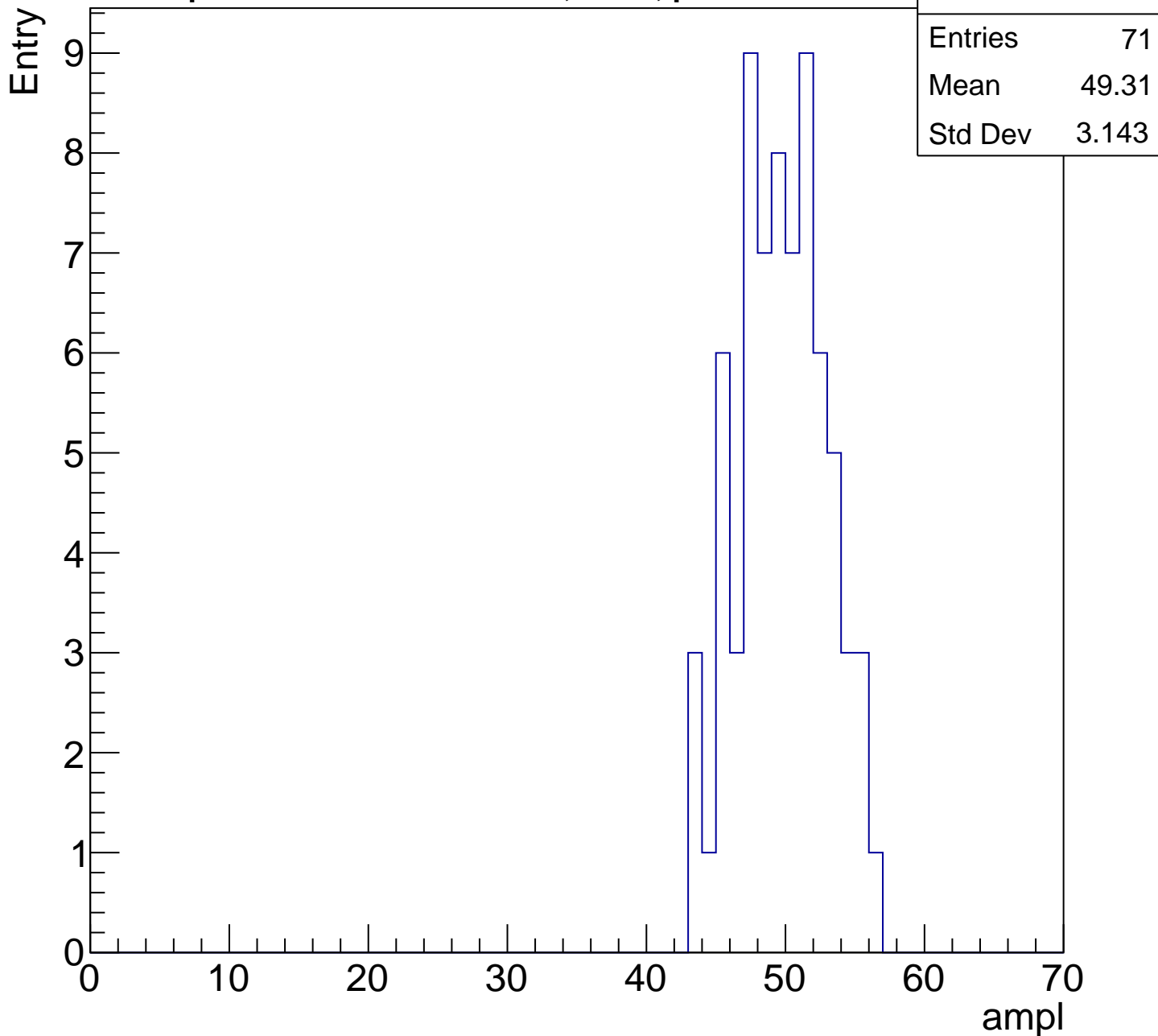
**Gaus mean : 42.1154**

**Gaus Width: 4.0490**



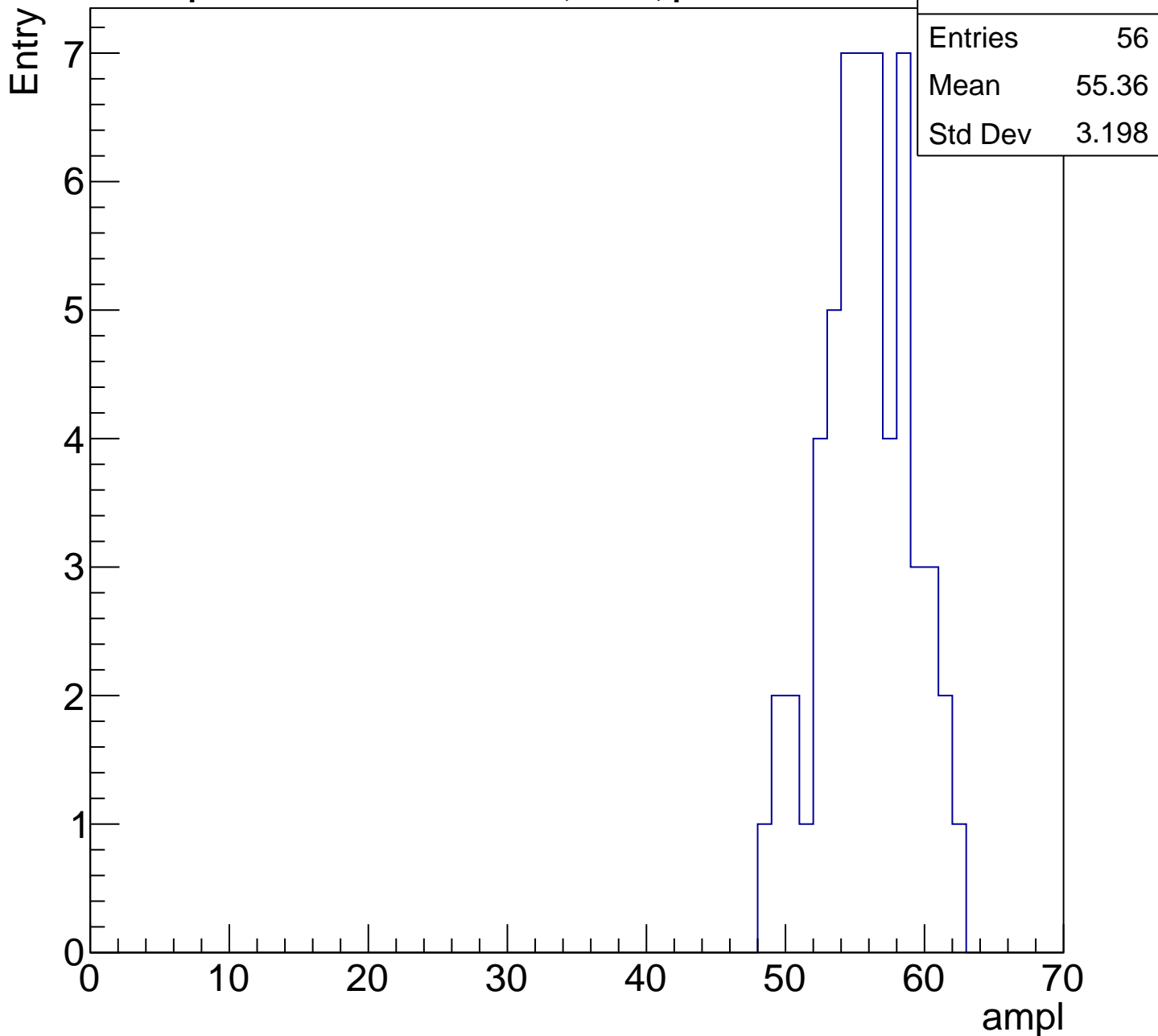
# B1L100S, U6-ch32, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2



# B1L100S, U6-ch32, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2



# B1L100S, U6-ch32, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	49
Mean	58.98
Std Dev	8.775

ampl

0

10

20

30

40

50

60

70

# B1L100S, U6-ch32, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	4
Mean	61.75
Std Dev	0.8292

ampl

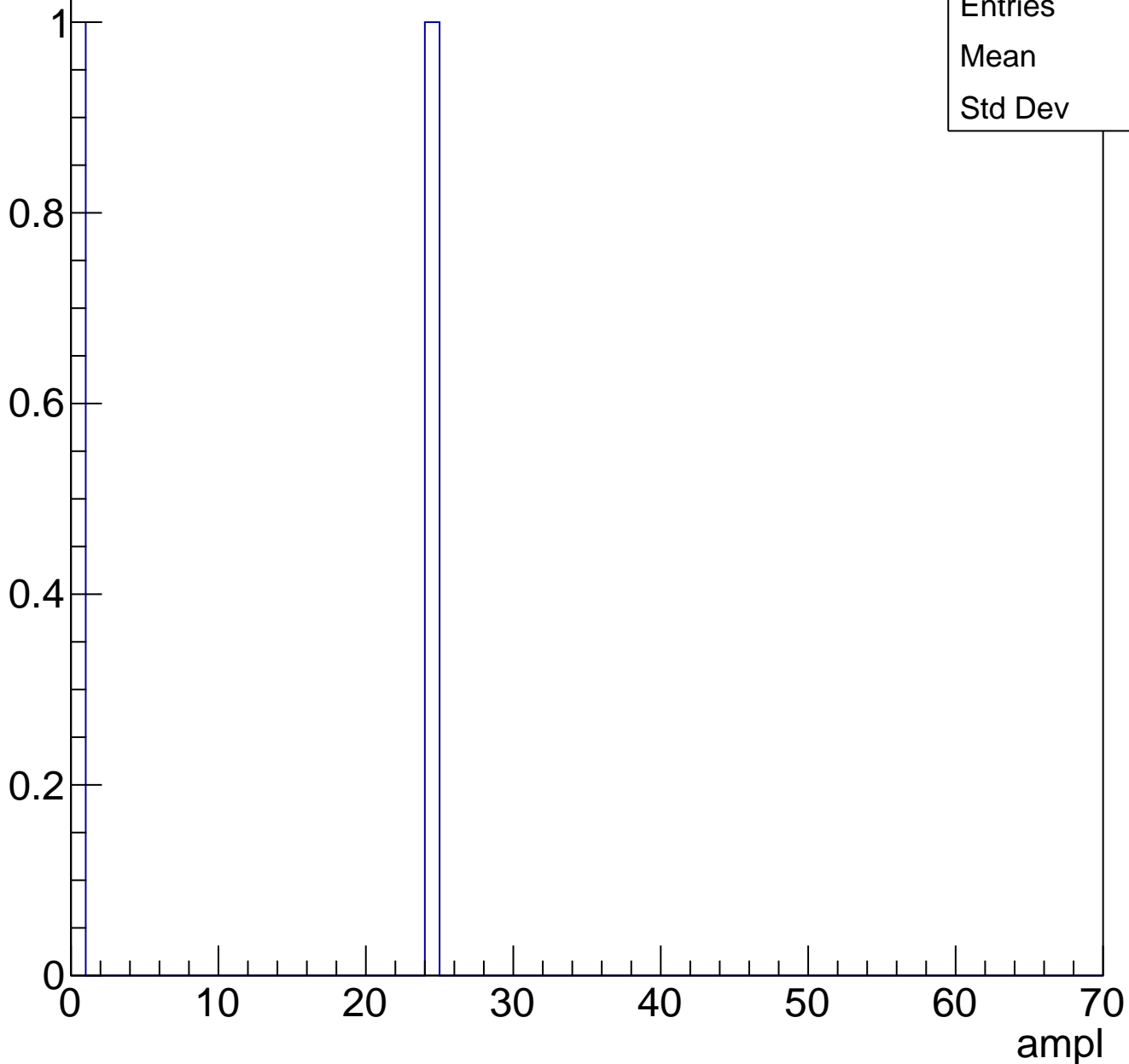
0 10 20 30 40 50 60 70



# B1L100S, U6-ch32, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



# B1L100S, U6-ch33, adc0

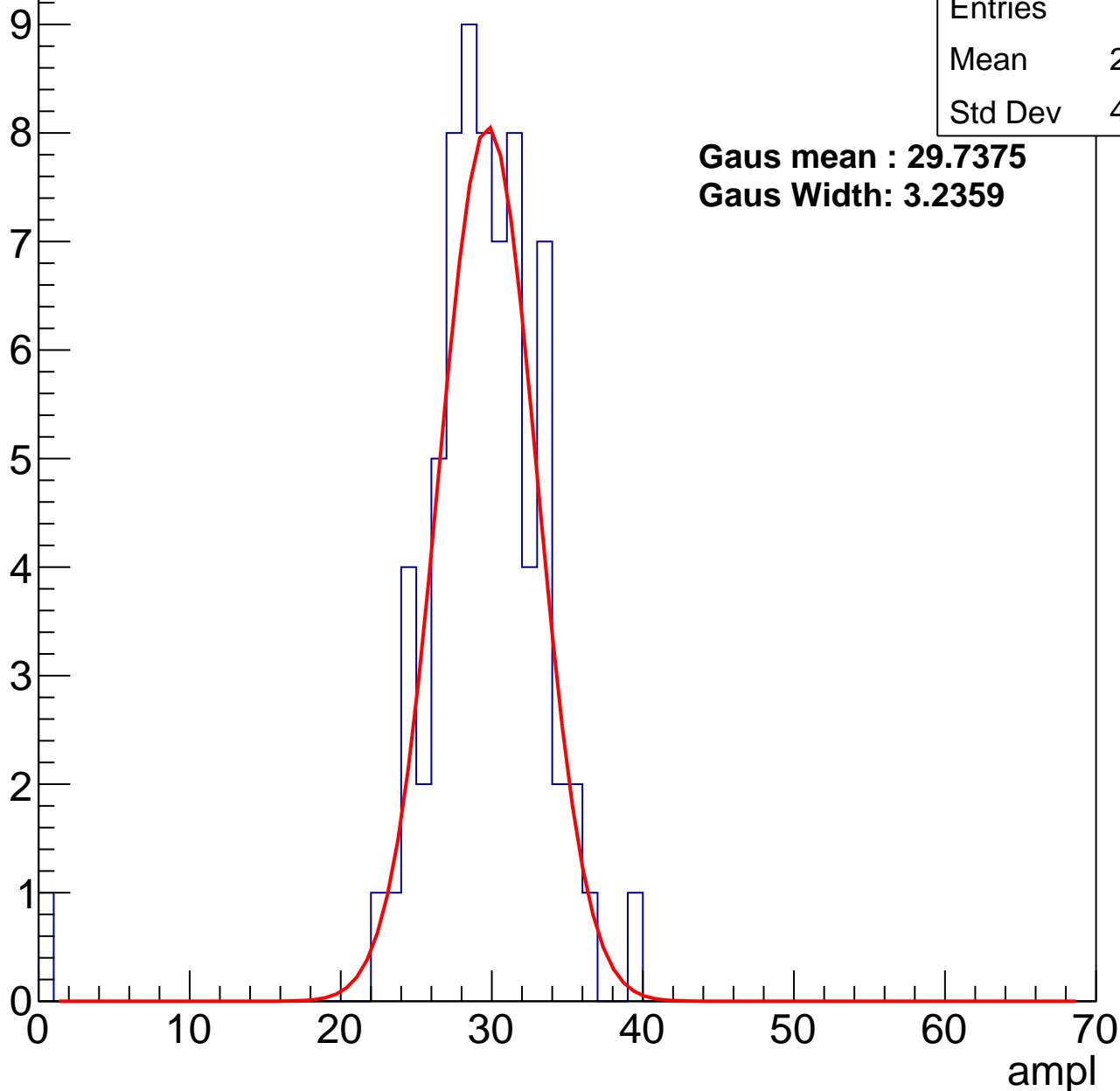
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	71
Mean	28.89
Std Dev	4.749

**Gaus mean : 29.7375**

**Gaus Width: 3.2359**



# B1L100S, U6-ch33, adc1

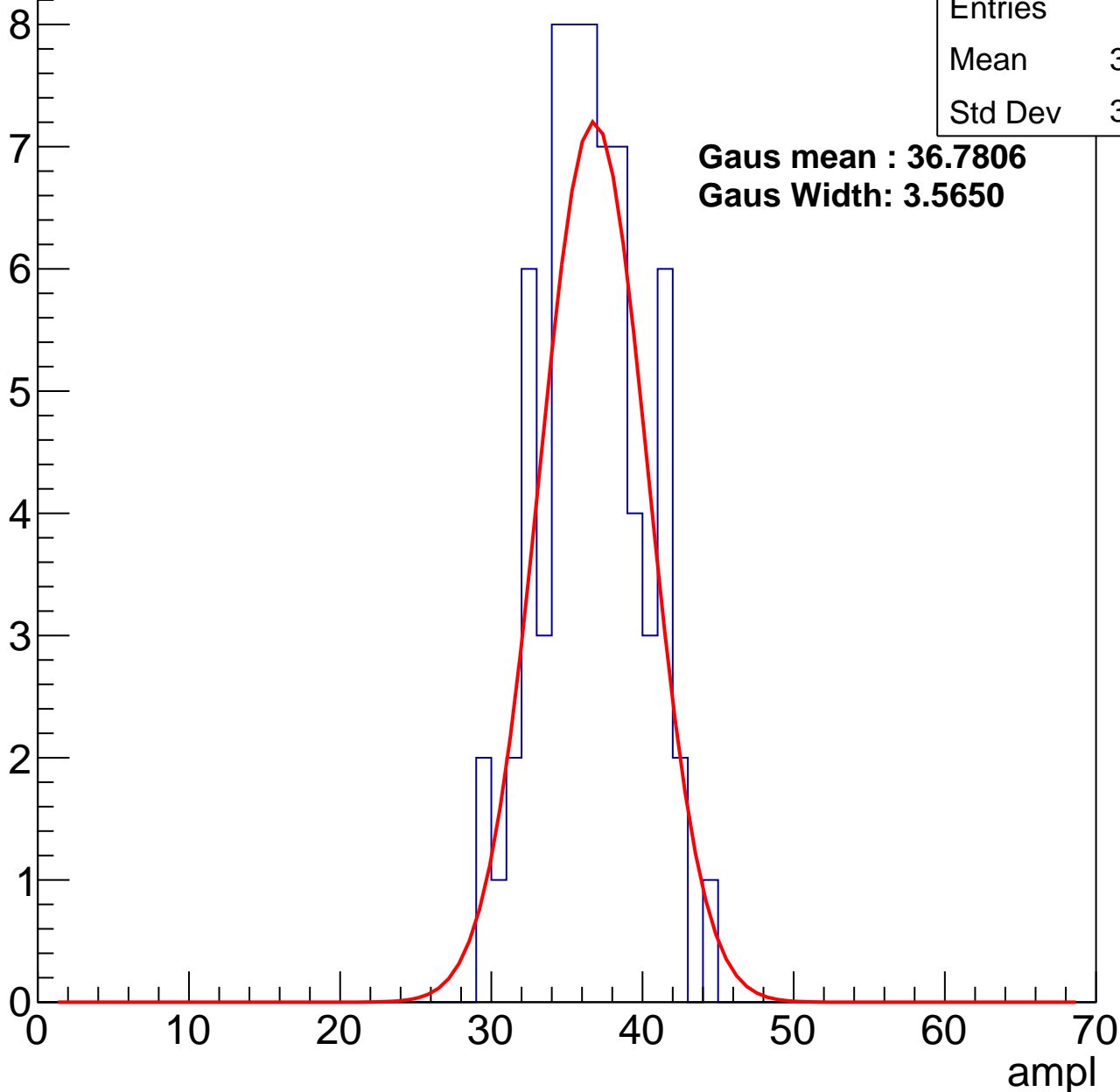
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	68
Mean	36.12
Std Dev	3.323

**Gaus mean : 36.7806**

**Gaus Width: 3.5650**



# B1L100S, U6-ch33, adc2

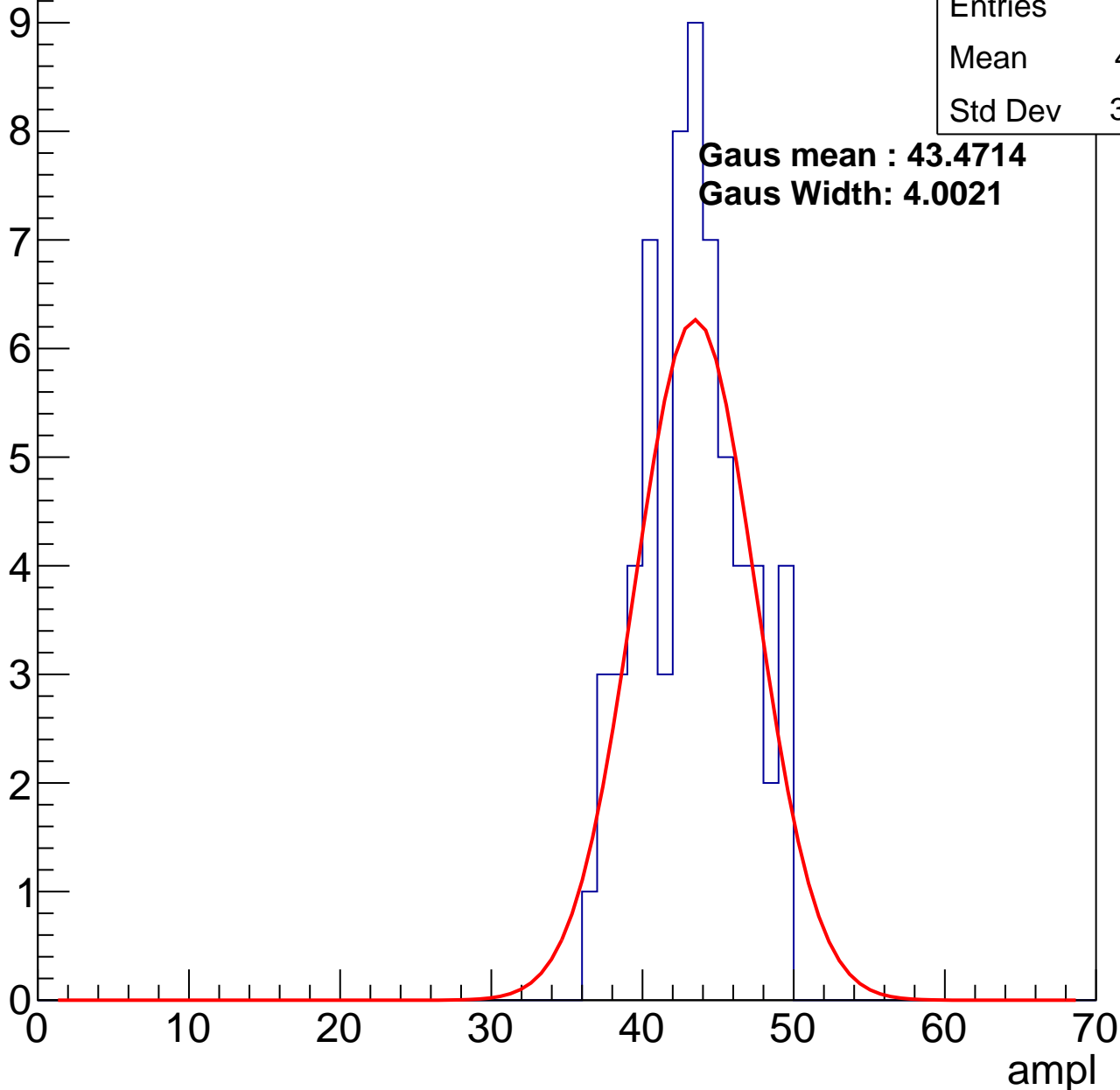
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	64
Mean	42.81
Std Dev	3.302

**Gaus mean : 43.4714**

**Gaus Width: 4.0021**

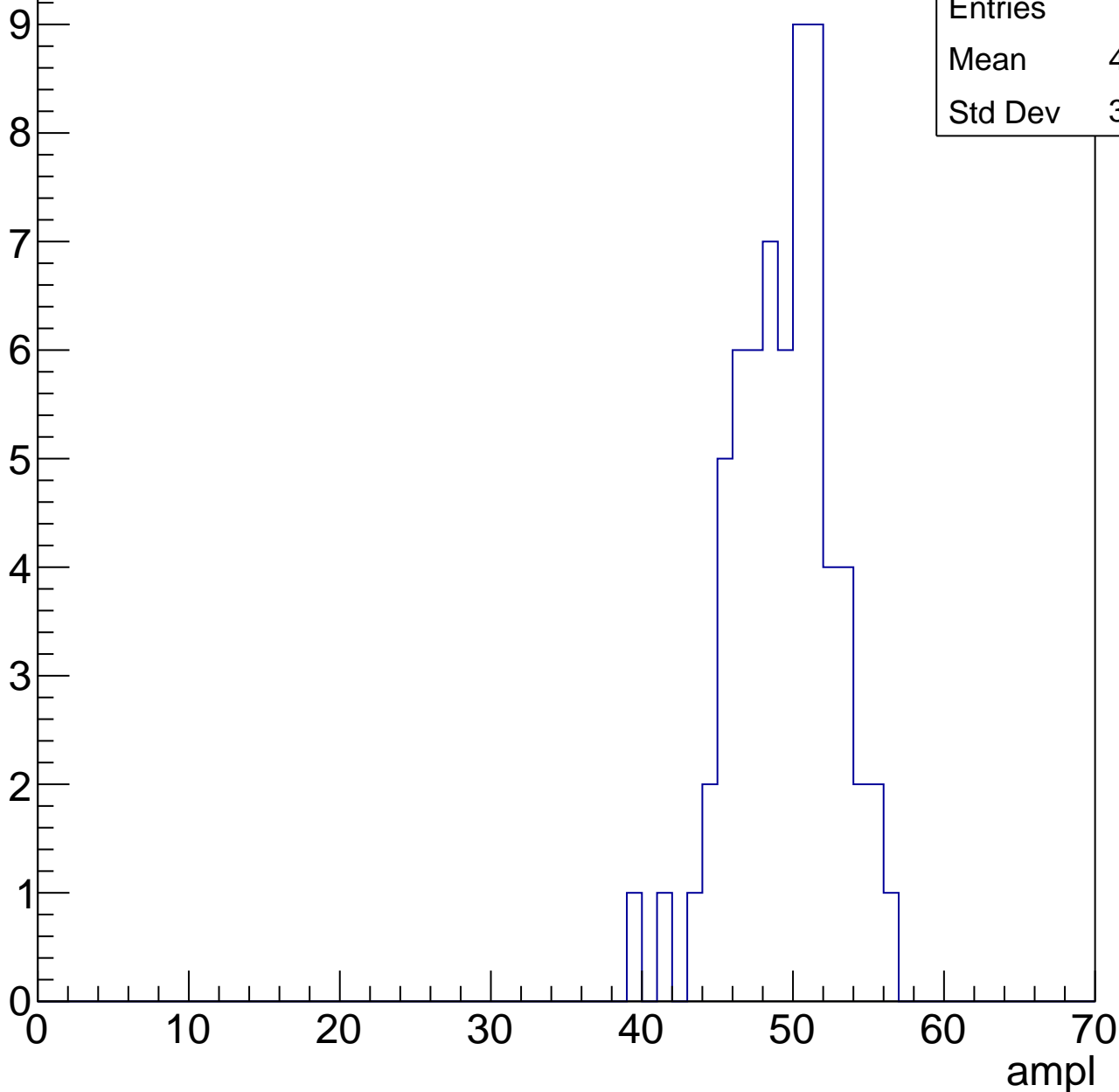


# B1L100S, U6-ch33, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

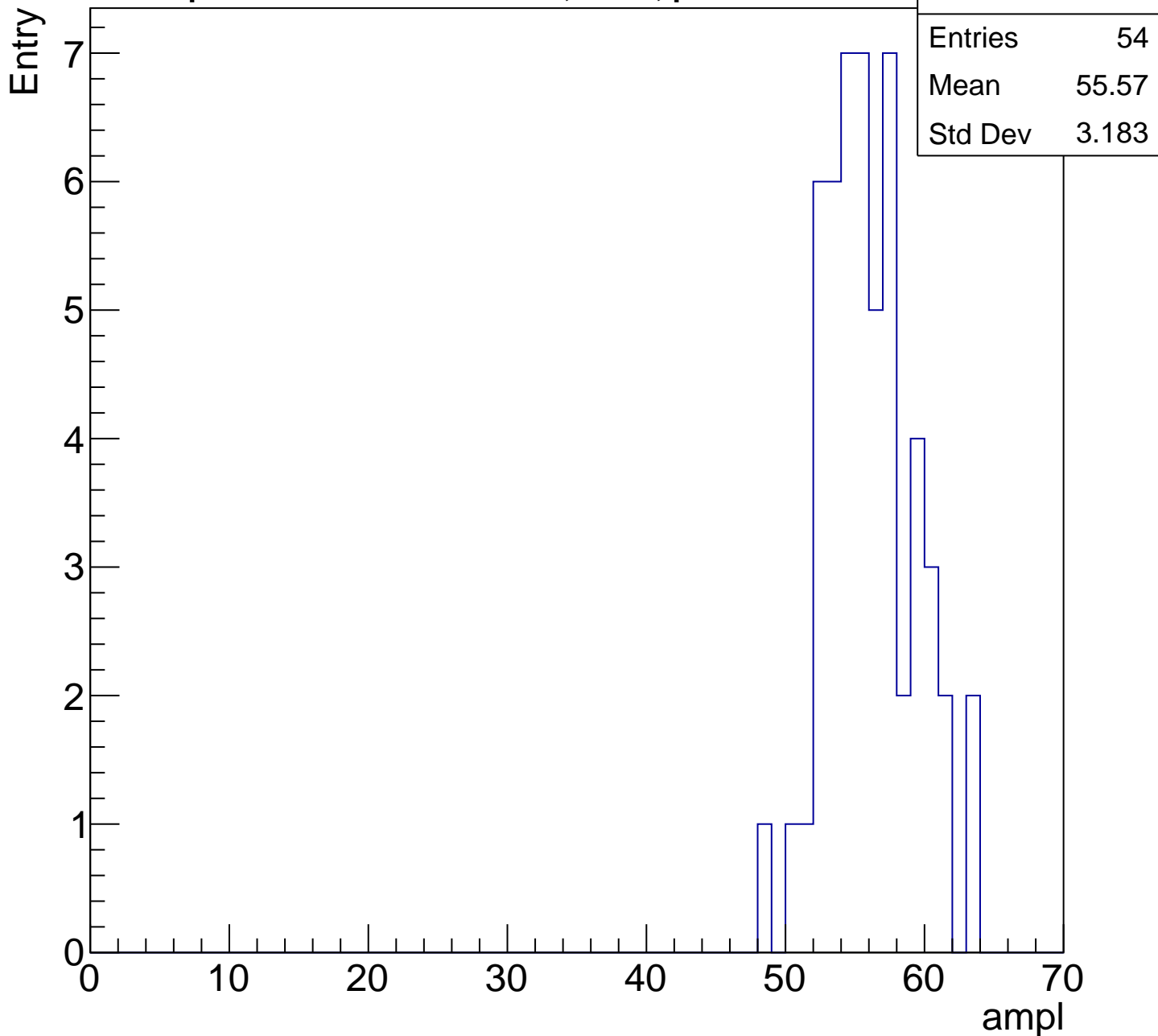
Entry

Entries	66
Mean	48.89
Std Dev	3.326



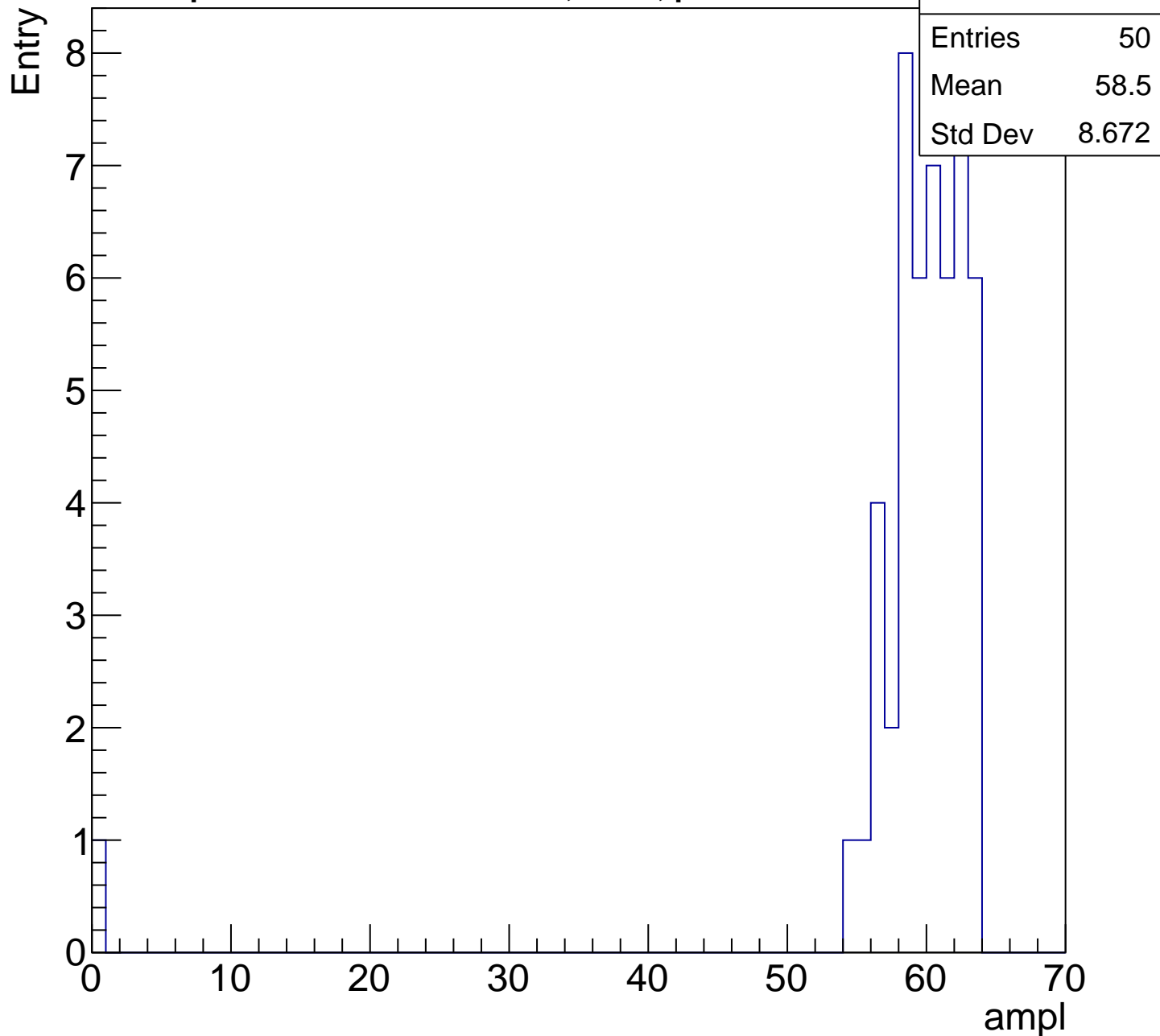
# B1L100S, U6-ch33, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2



# B1L100S, U6-ch33, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2



# B1L100S, U6-ch33, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	7
Mean	61.29
Std Dev	1.906

0 10 20 30 40 50 60 70

ampl

1



# B1L100S, U6-ch33, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L100S, U6-ch34, adc0

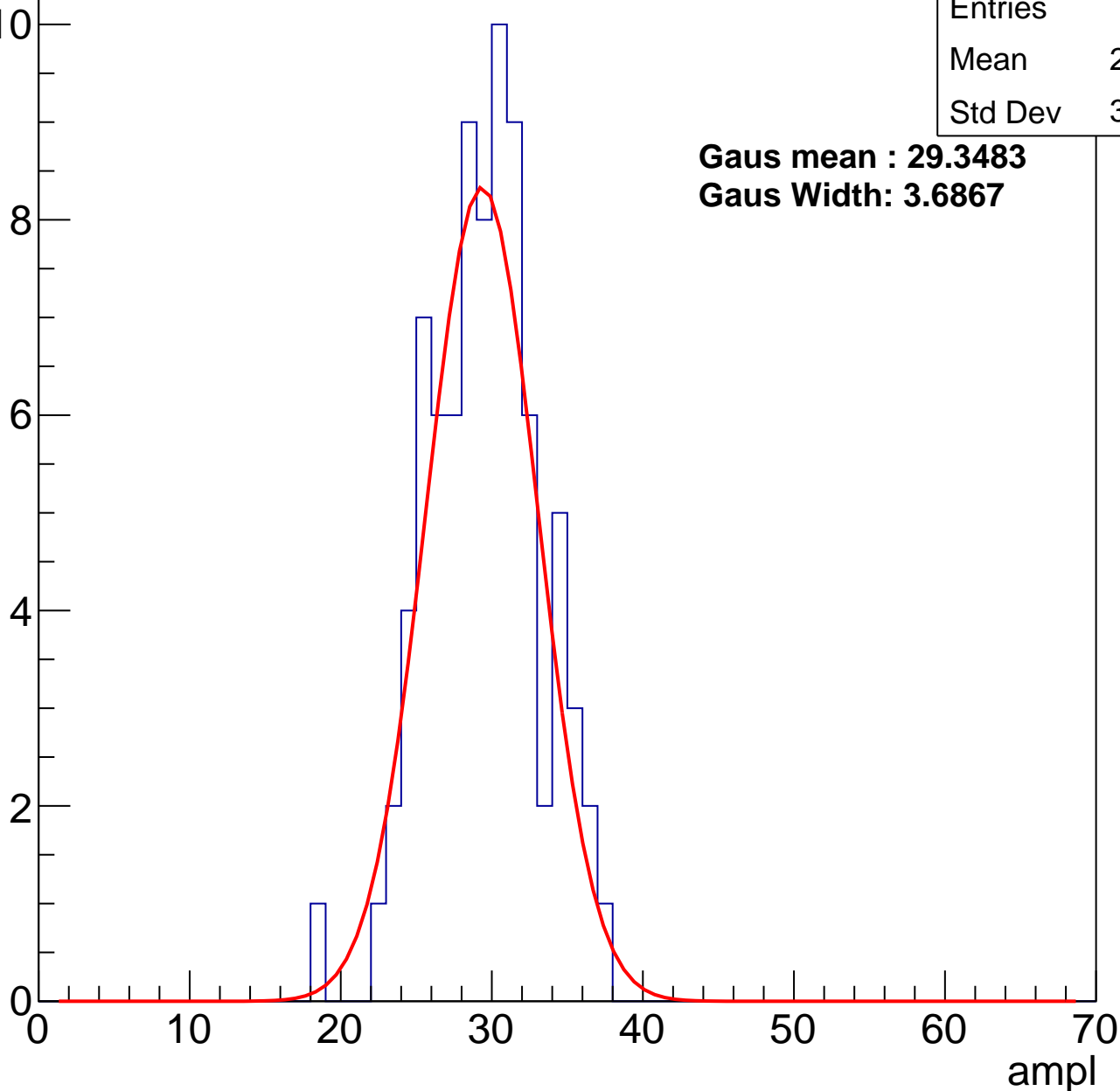
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	82
Mean	29.02
Std Dev	3.609

**Gaus mean : 29.3483**

**Gaus Width: 3.6867**



# B1L100S, U6-ch34, adc1

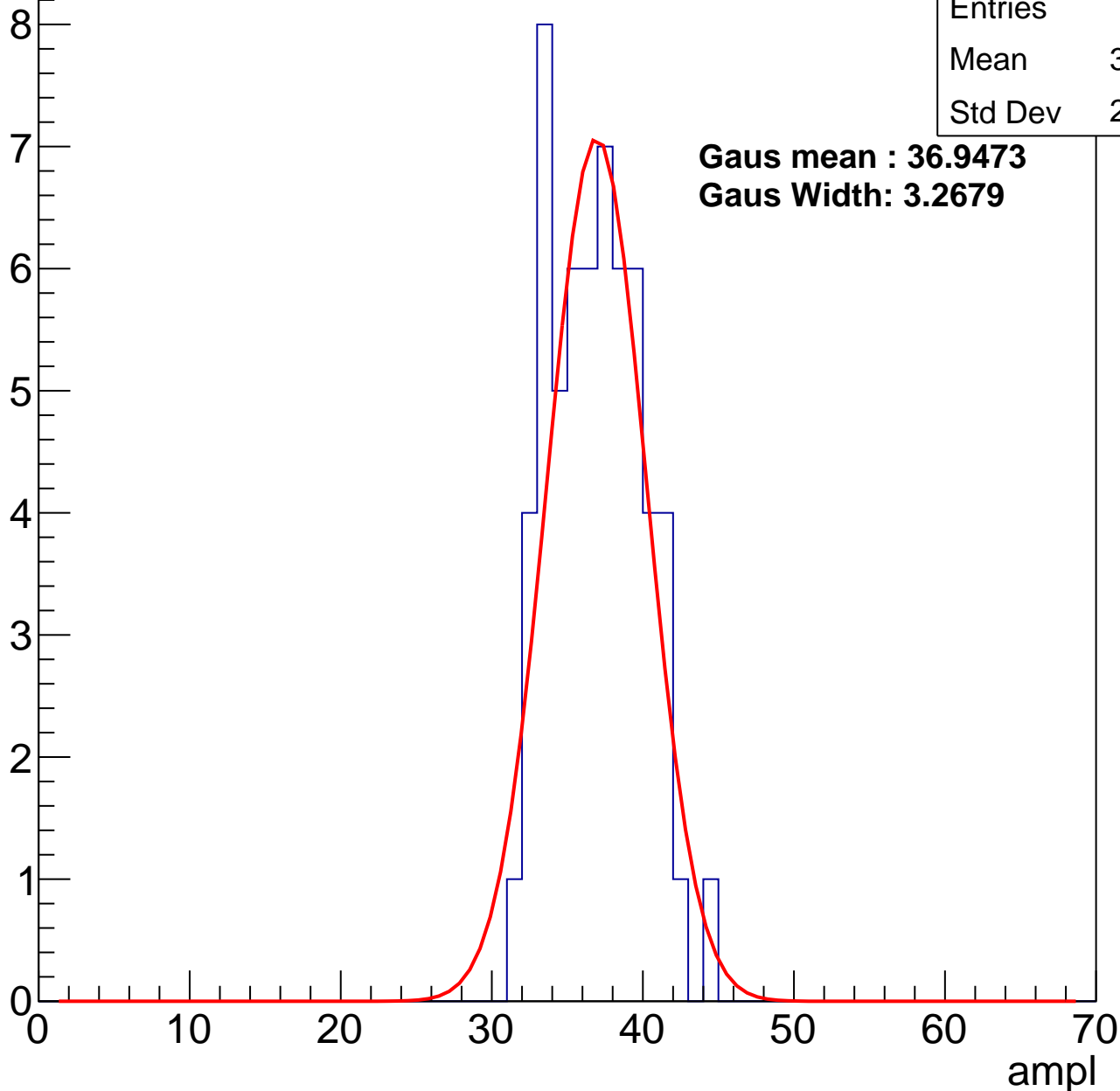
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	59
Mean	36.44
Std Dev	2.982

**Gaus mean : 36.9473**

**Gaus Width: 3.2679**



# B1L100S, U6-ch34, adc2

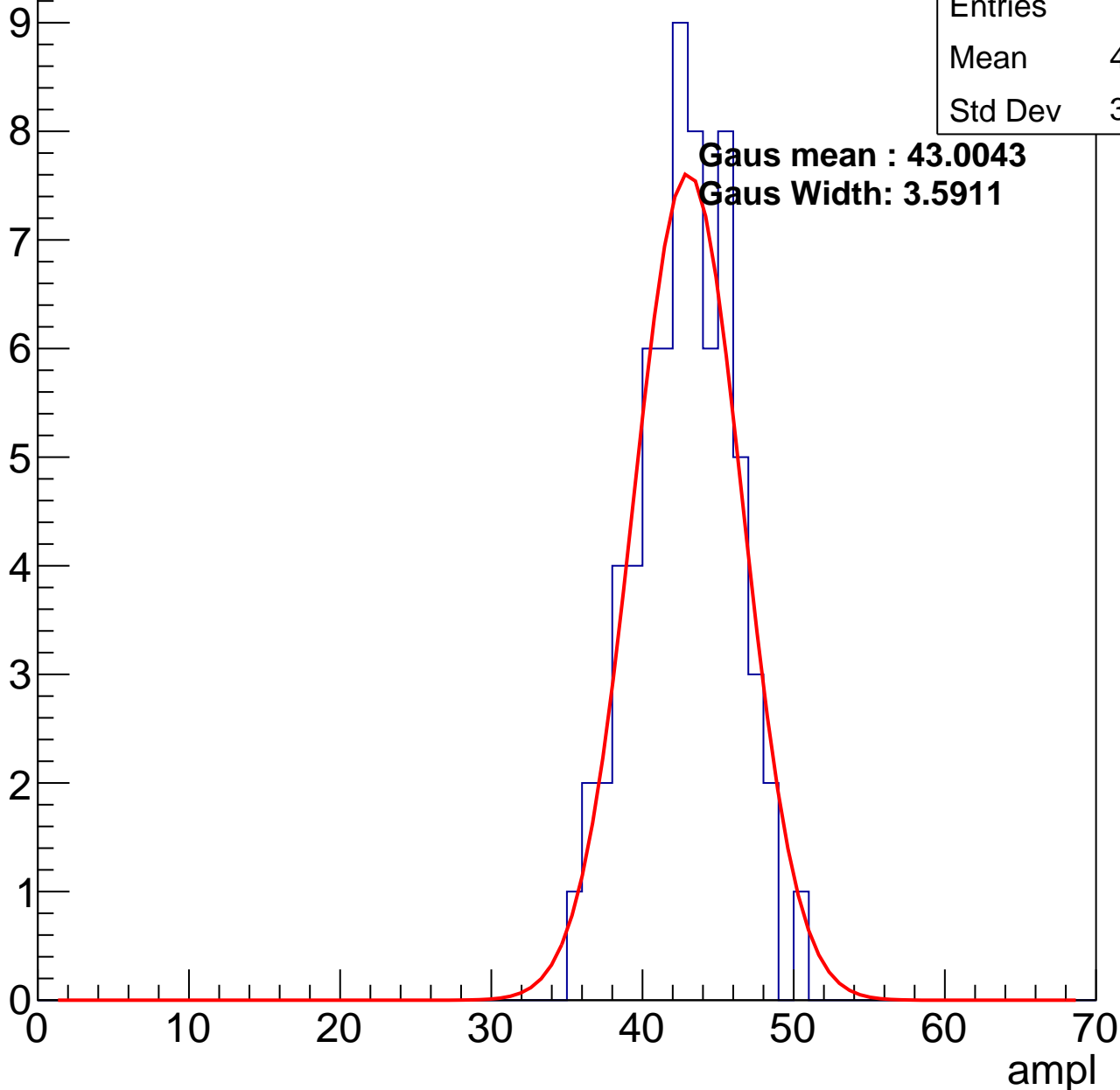
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	67
Mean	42.36
Std Dev	3.203

**Gaus mean : 43.0043**

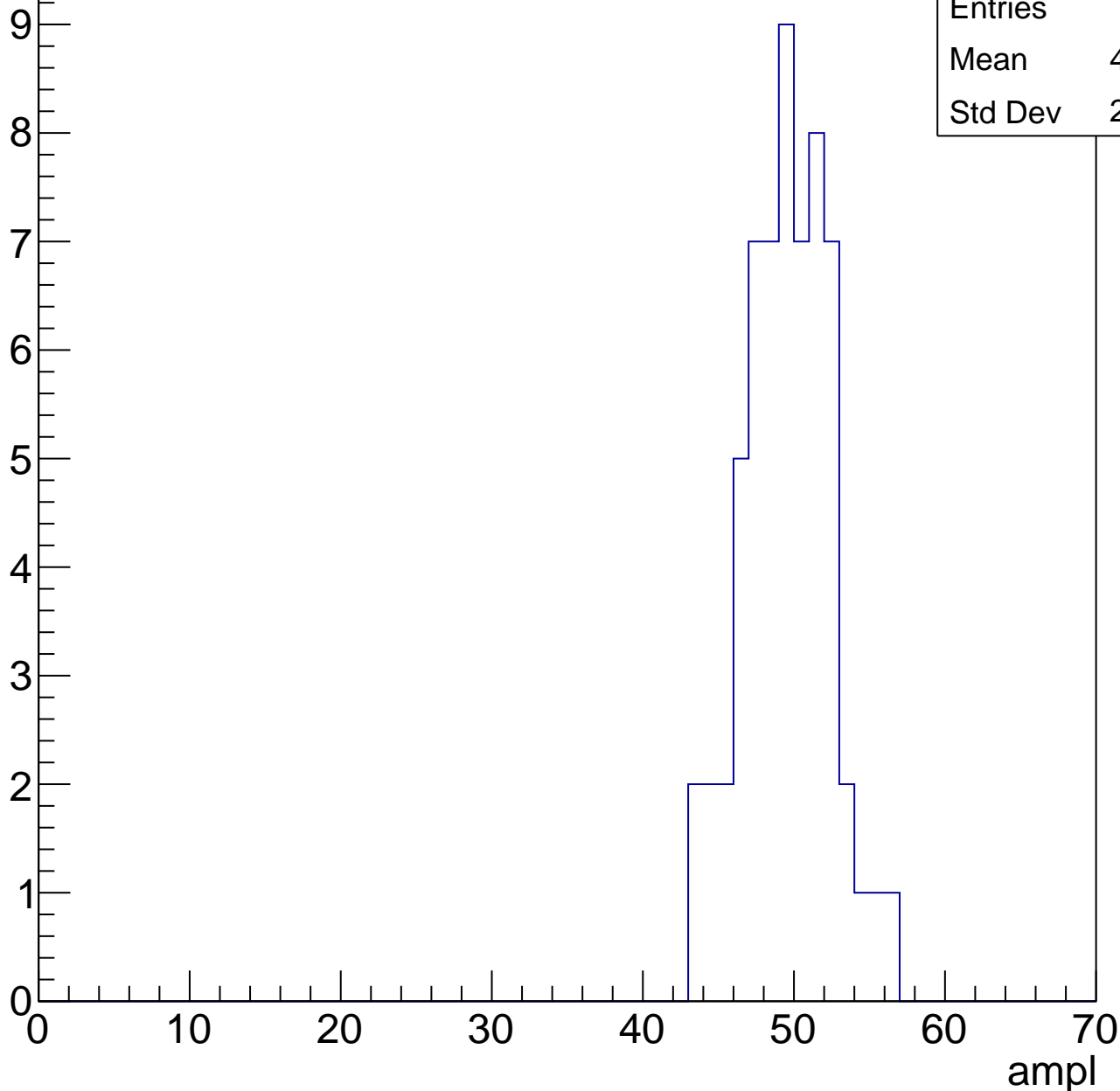
**Gaus Width: 3.5911**



# B1L100S, U6-ch34, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

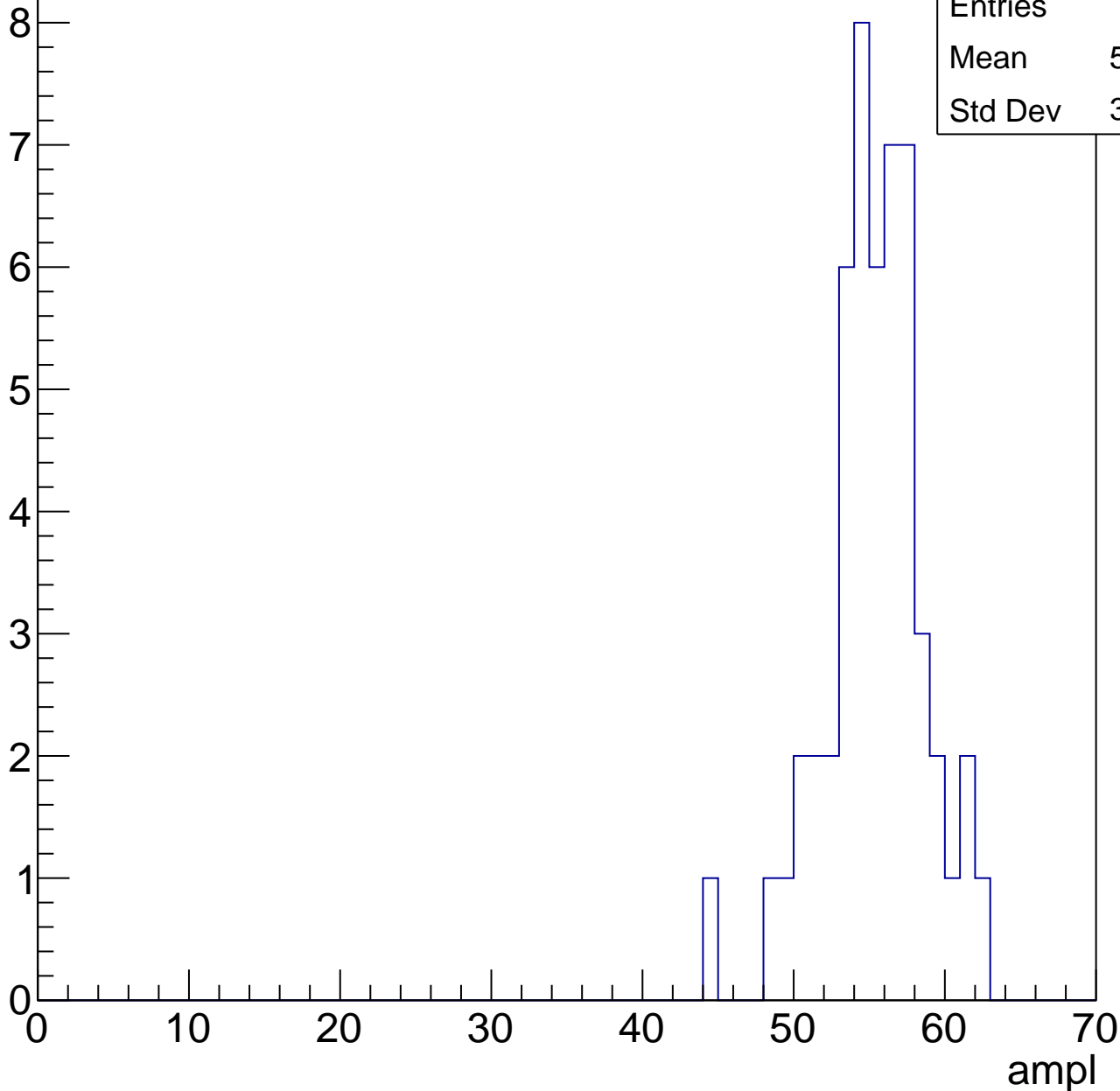


# B1L100S, U6-ch34, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

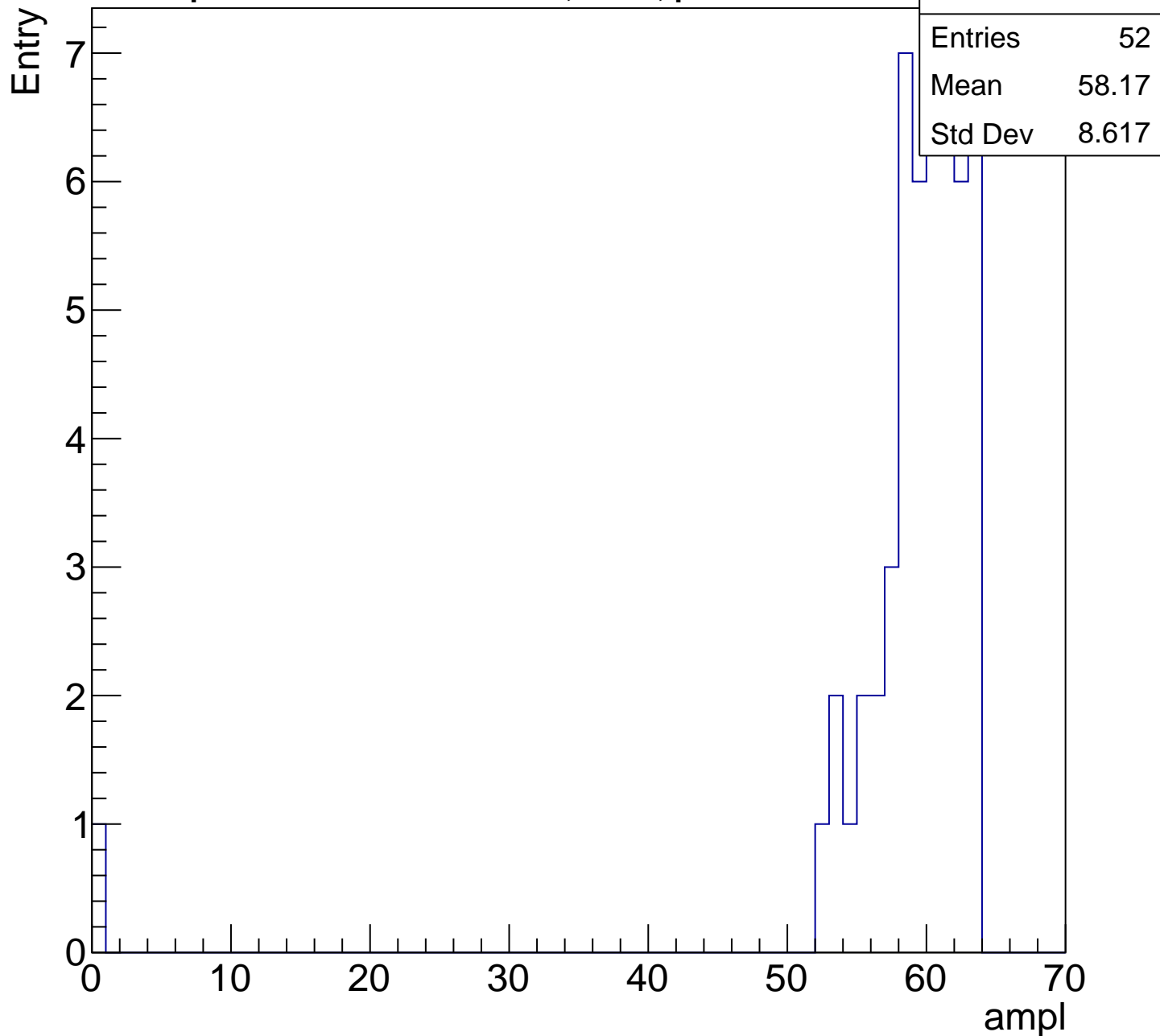
Entry

Entries	52
Mean	54.88
Std Dev	3.332



# B1L100S, U6-ch34, adc5

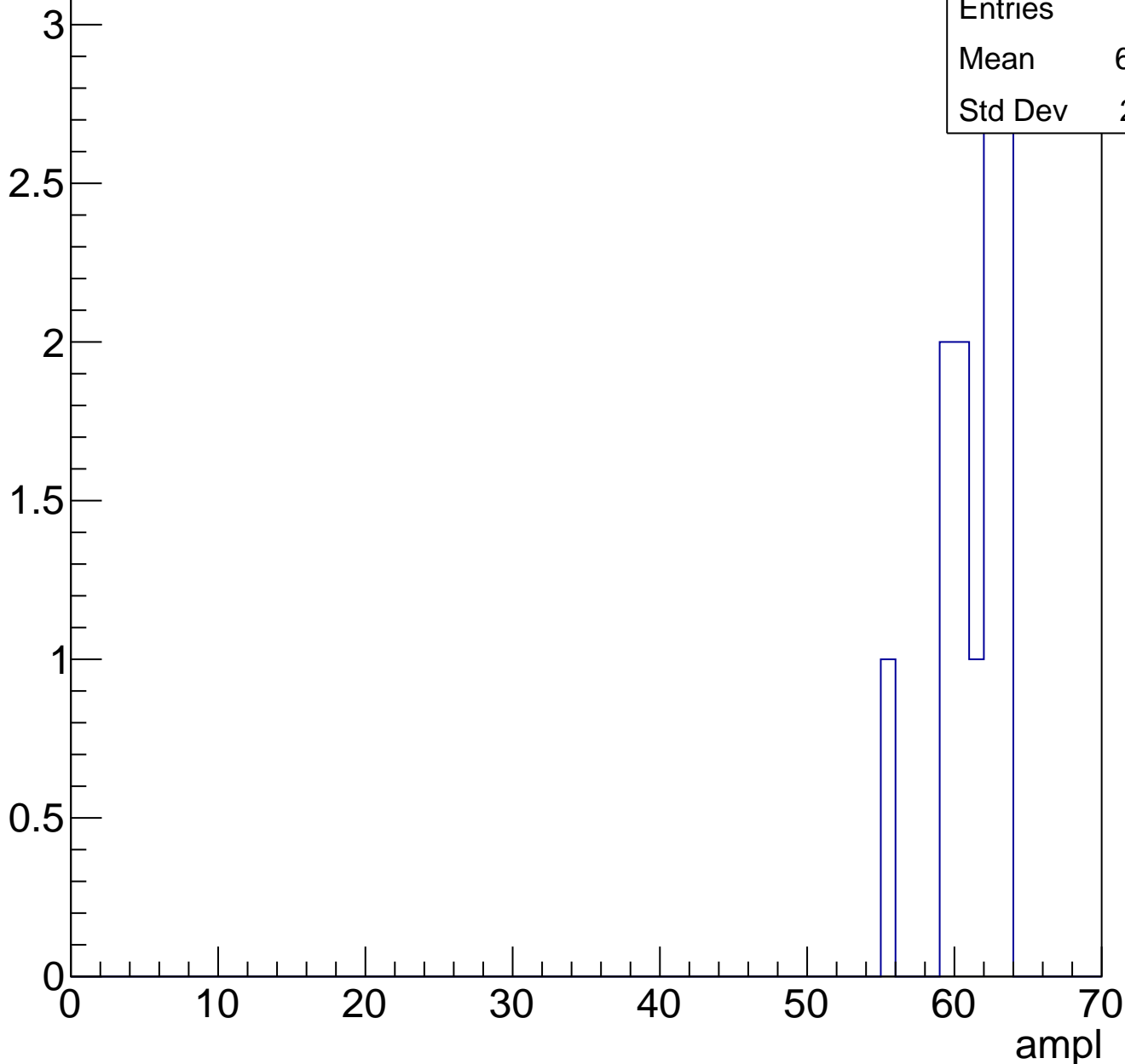
calib\_packv5\_042523\_0143.root, FC#4, port A2



# B1L100S, U6-ch34, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry





# B1L100S, U6-ch34, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



# B1L100S, U6-ch35, adc0

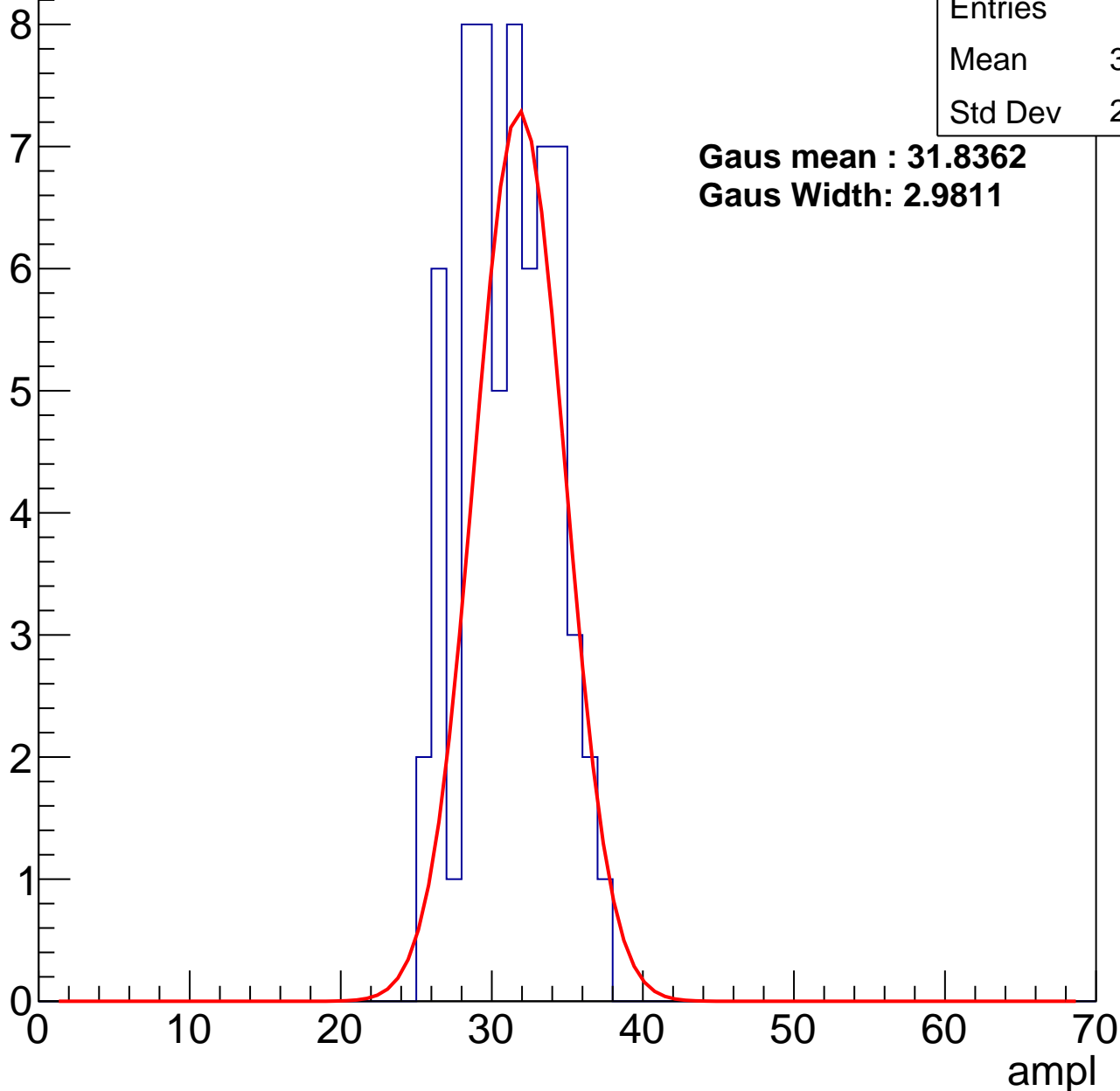
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	64
Mean	30.66
Std Dev	2.985

**Gaus mean : 31.8362**

**Gaus Width: 2.9811**



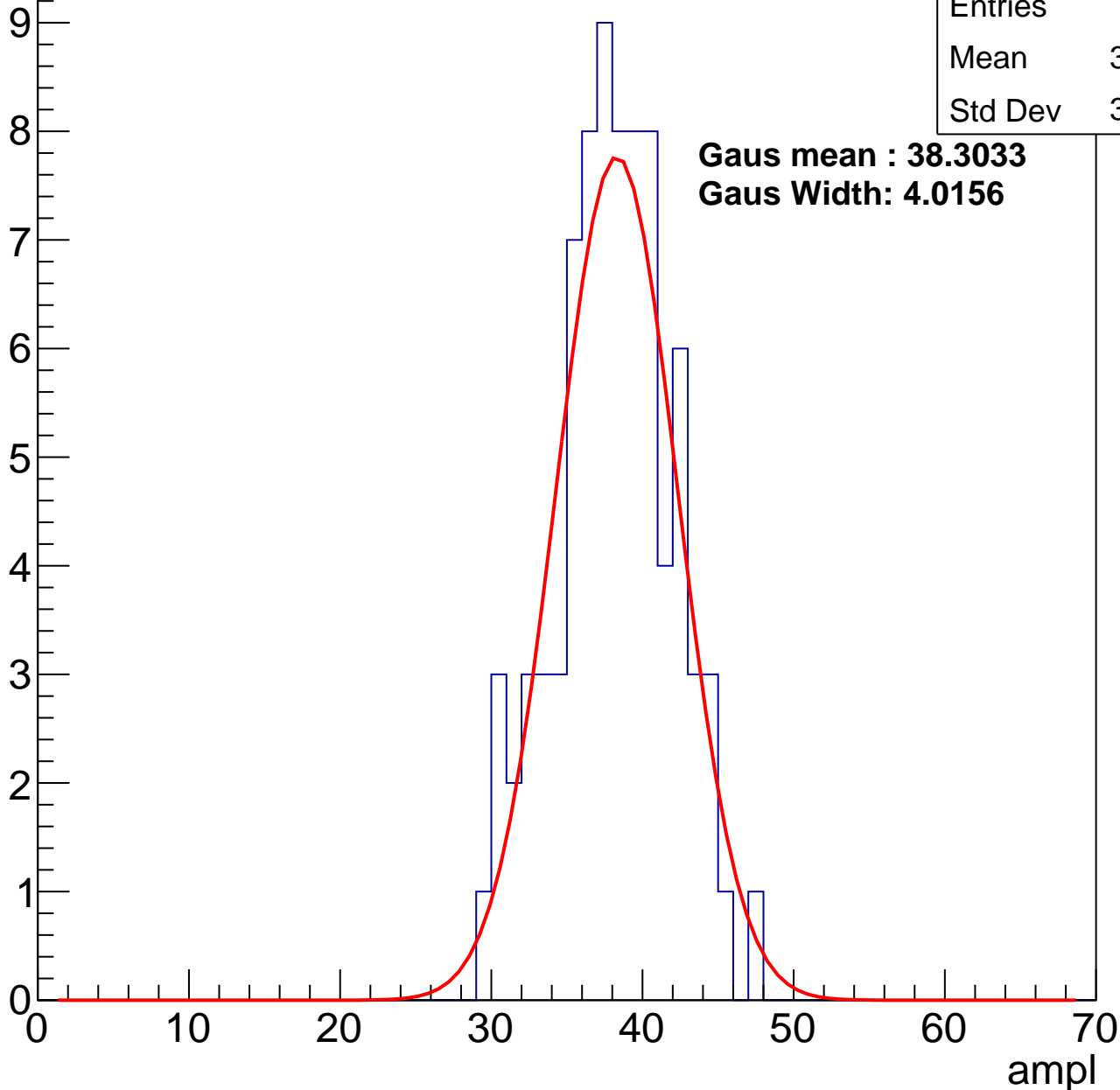
# B1L100S, U6-ch35, adc1

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	81
Mean	37.64
Std Dev	3.818

**Gaus mean : 38.3033**  
**Gaus Width: 4.0156**



# B1L100S, U6-ch35, adc2

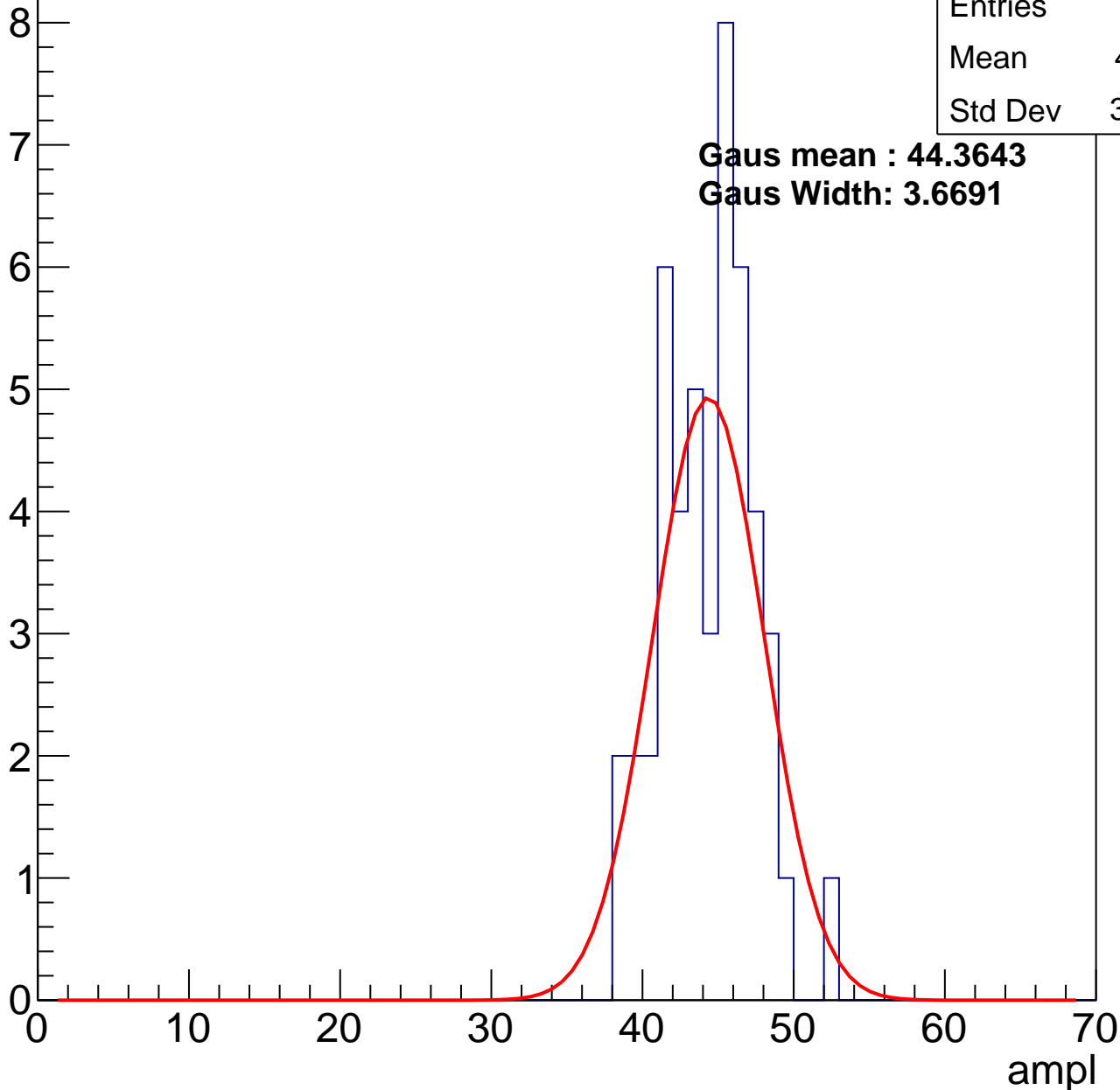
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	47
Mean	43.91
Std Dev	3.038

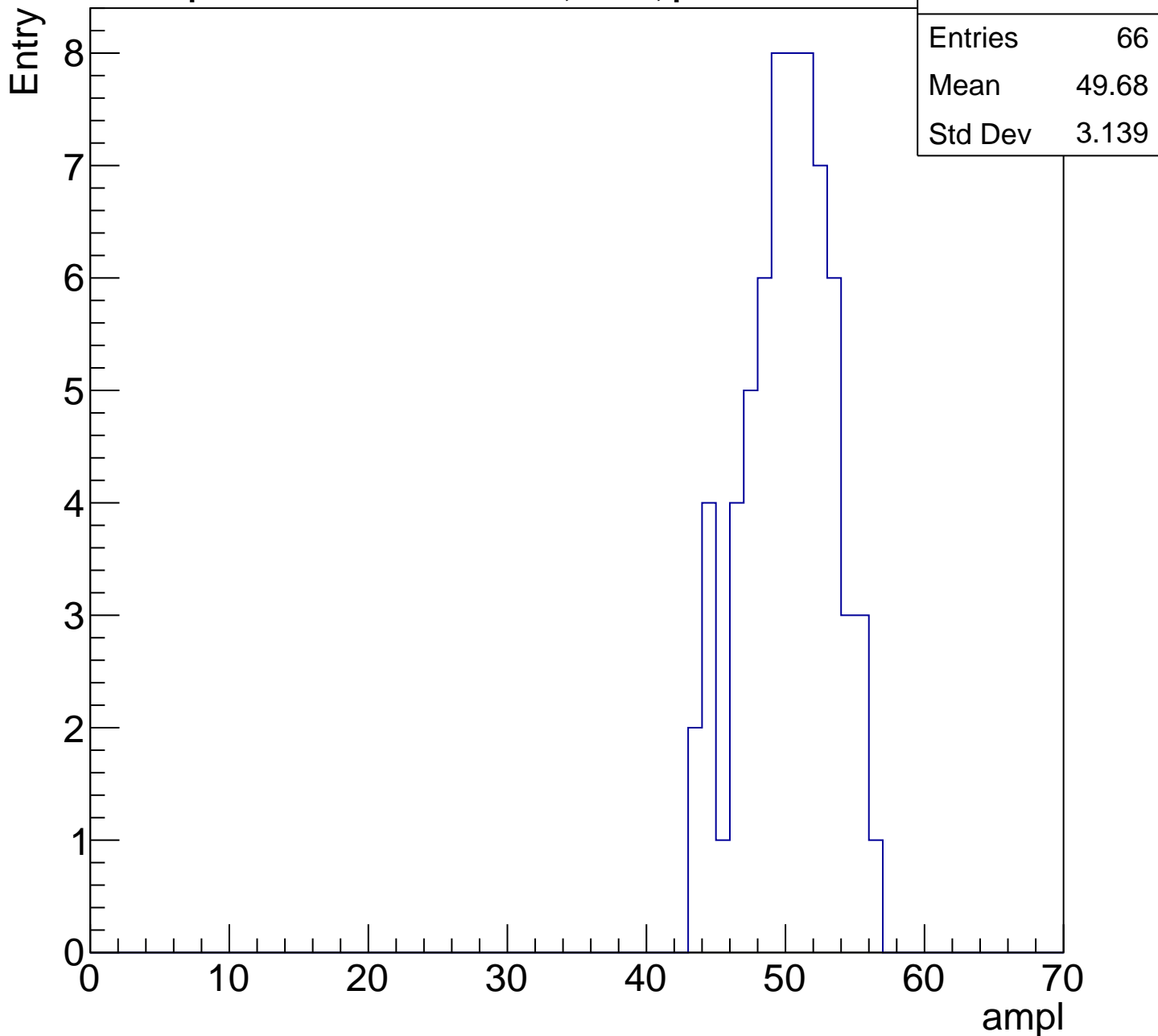
**Gaus mean : 44.3643**

**Gaus Width: 3.6691**



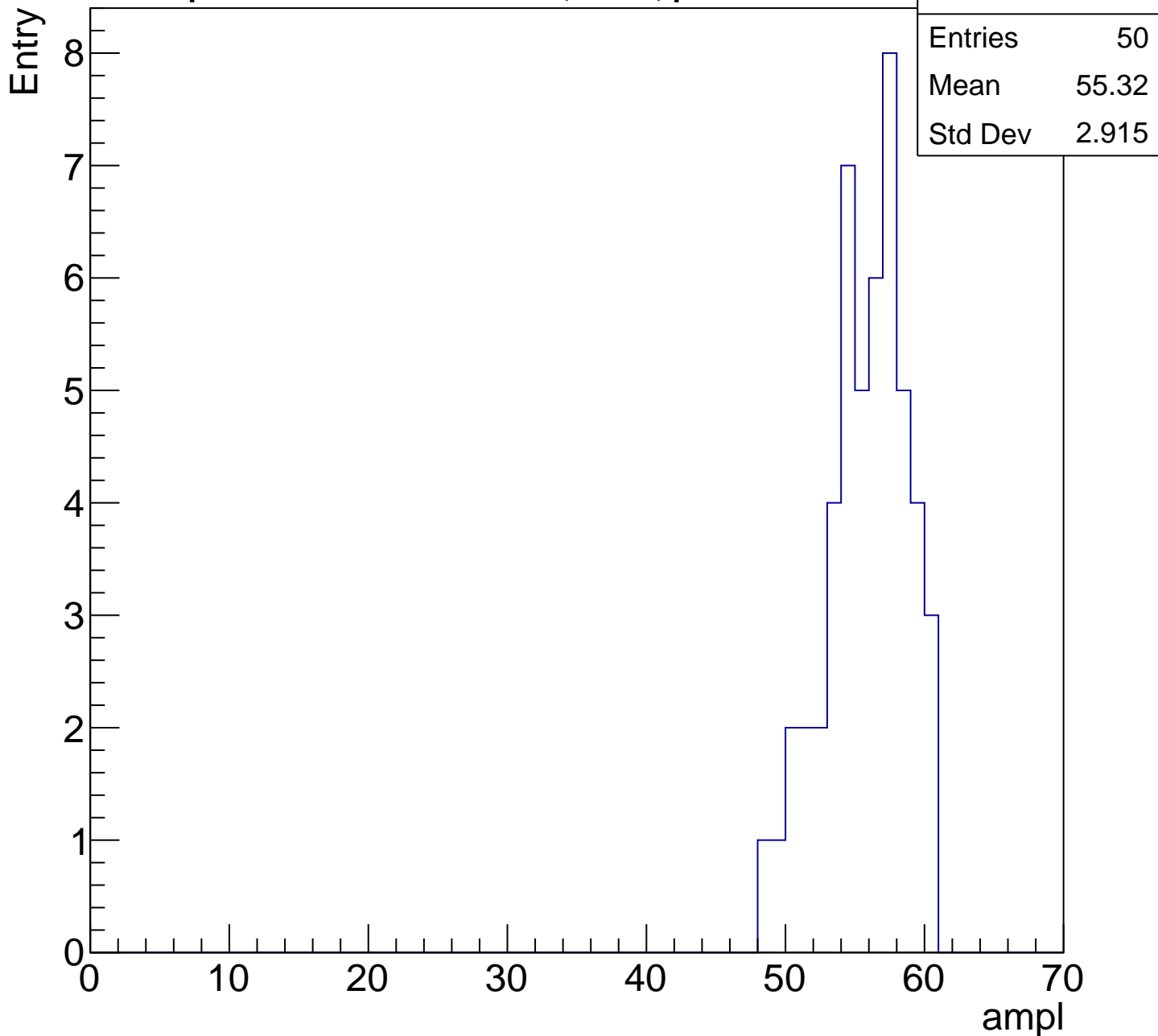
# B1L100S, U6-ch35, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2



# B1L100S, U6-ch35, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2



# B1L100S, U6-ch35, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	50
Mean	58.96
Std Dev	8.729

ampl

0

10

20

30

40

50

60

70

# B1L100S, U6-ch35, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

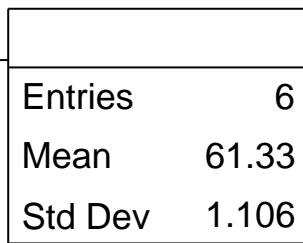
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	6
Mean	61.33
Std Dev	1.106

0 10 20 30 40 50 60 70

ampl





# B1L100S, U6-ch35, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



# B1L100S, U6-ch36, adc0

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	74
Mean	29.19
Std Dev	3.376

**Gaus mean : 29.4673**

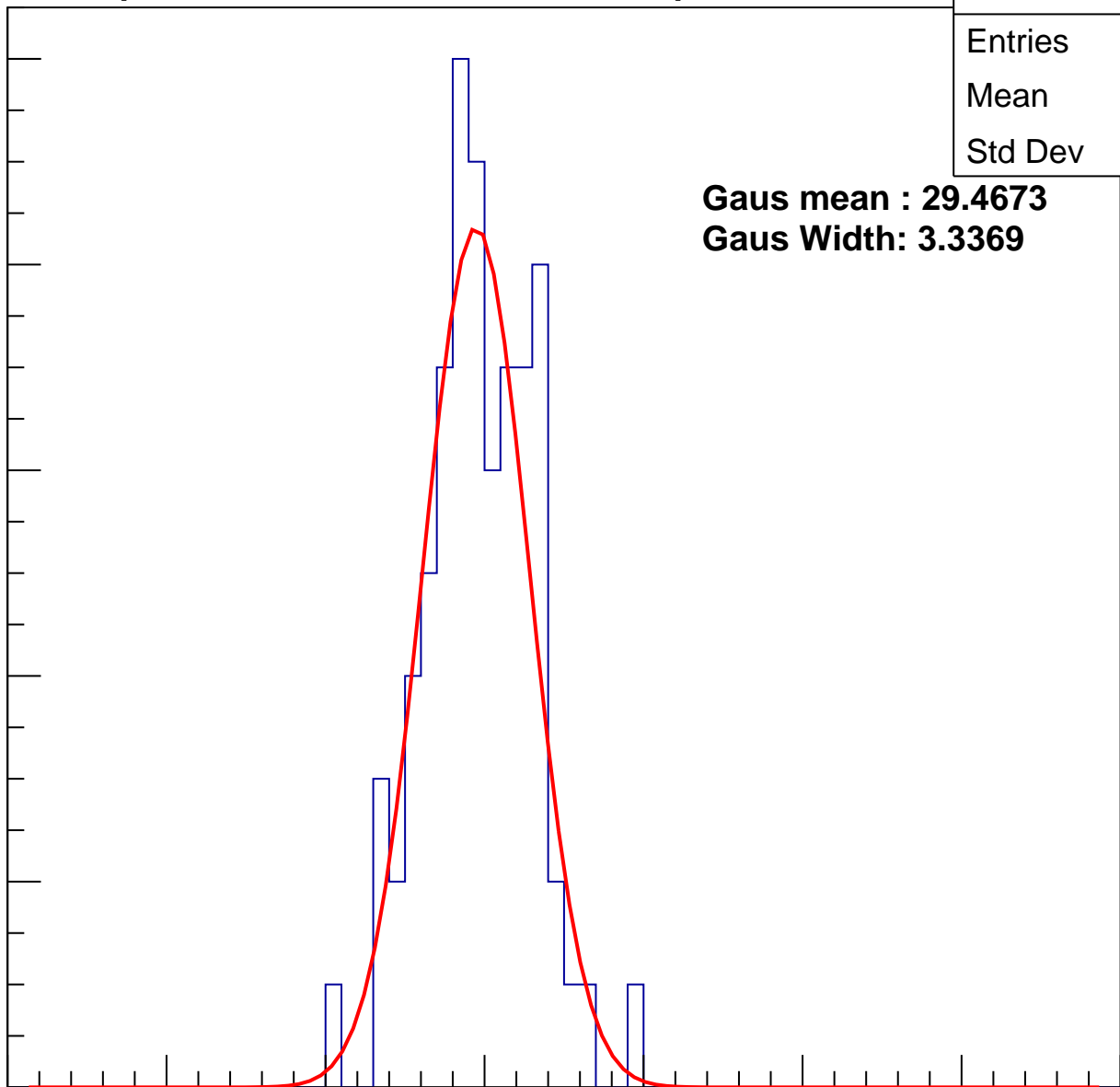
**Gaus Width: 3.3369**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L100S, U6-ch36, adc1

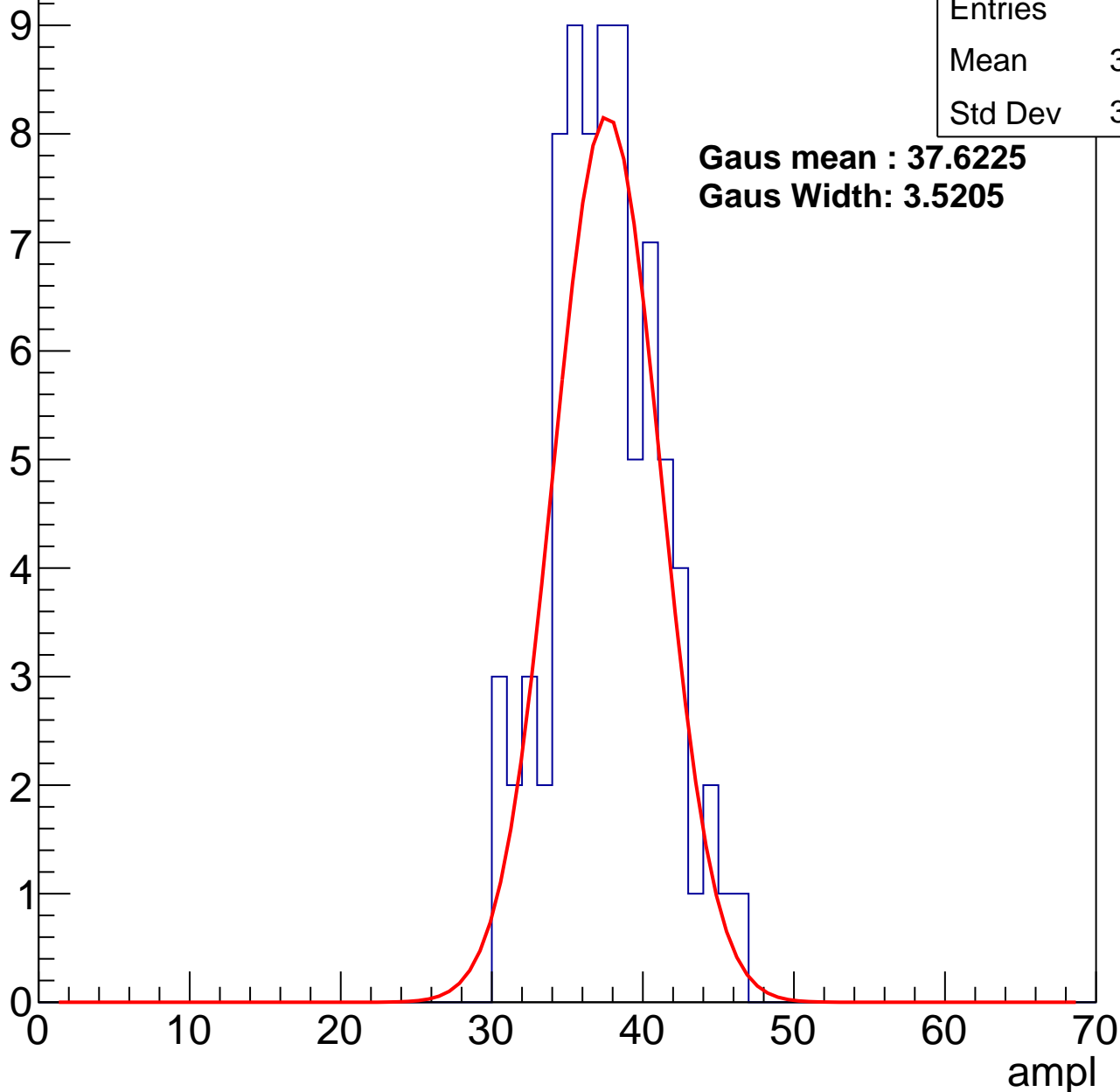
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	79
Mean	37.14
Std Dev	3.543

**Gaus mean : 37.6225**

**Gaus Width: 3.5205**



# B1L100S, U6-ch36, adc2

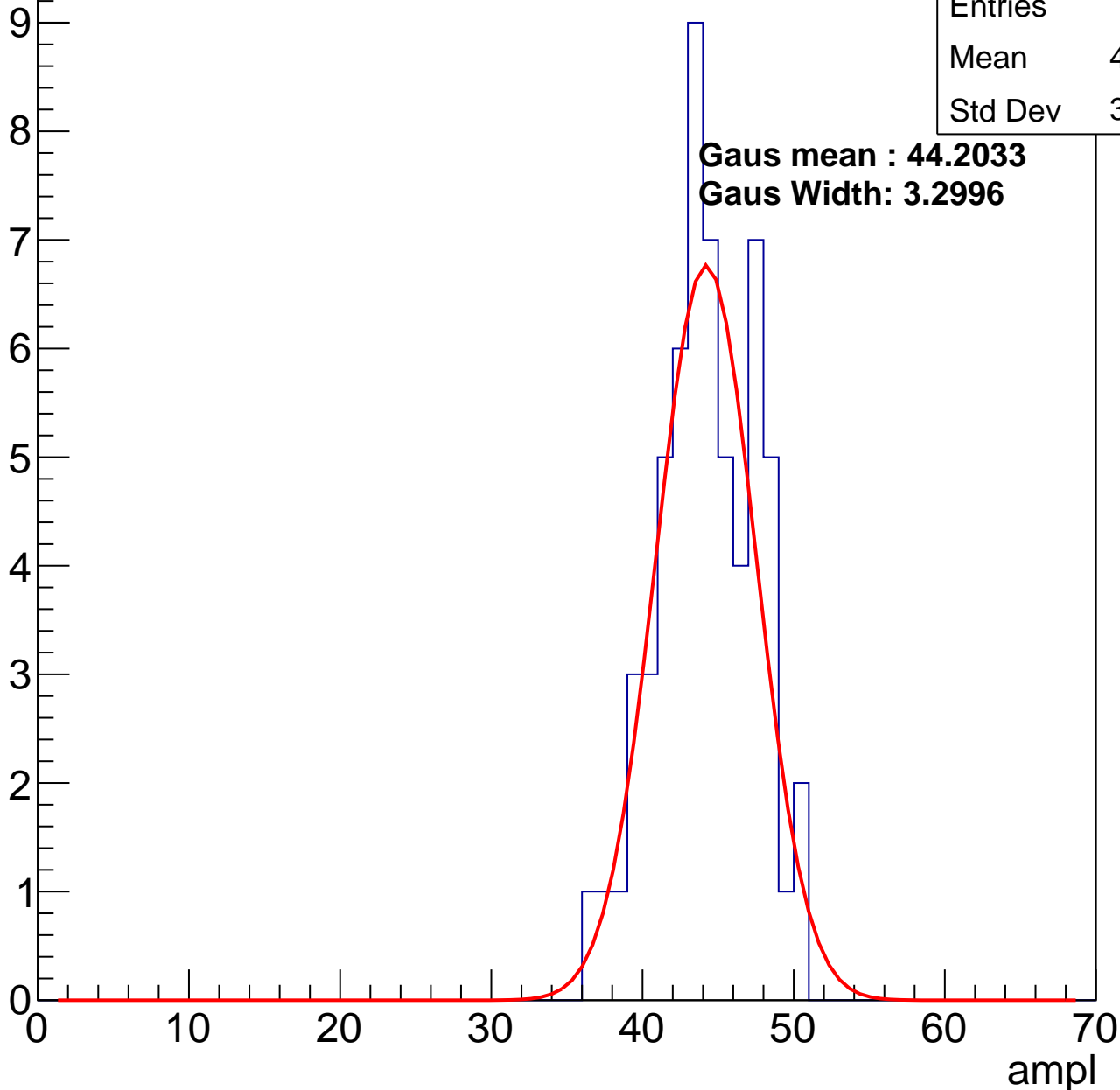
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	60
Mean	43.78
Std Dev	3.184

**Gaus mean : 44.2033**

**Gaus Width: 3.2996**

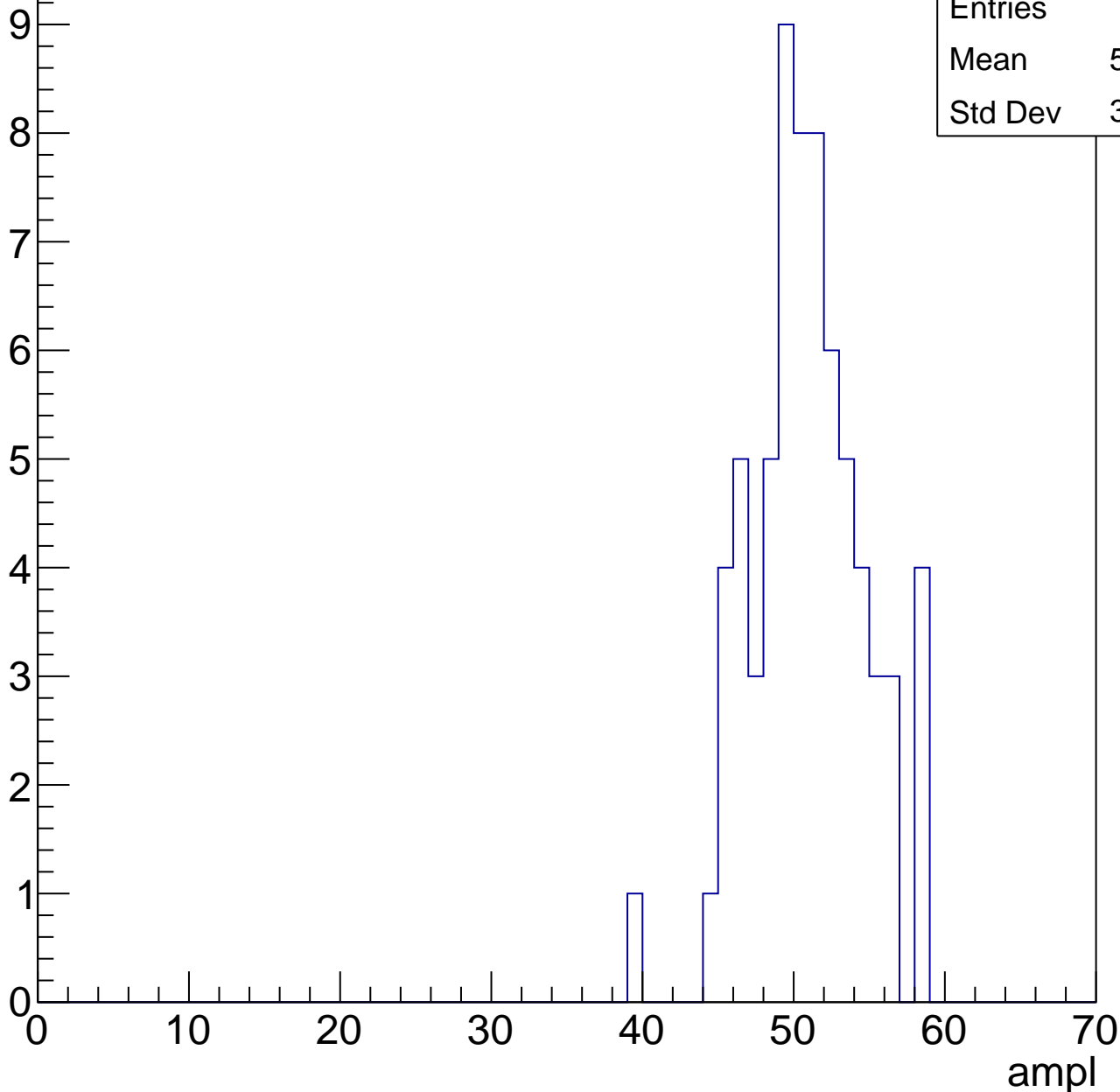


# B1L100S, U6-ch36, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	69
Mean	50.45
Std Dev	3.728



# B1L100S, U6-ch36, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

7

6

5

4

3

2

1

0

Entries 51

Mean 55.88

Std Dev 2.72

ampl

0

10

20

30

40

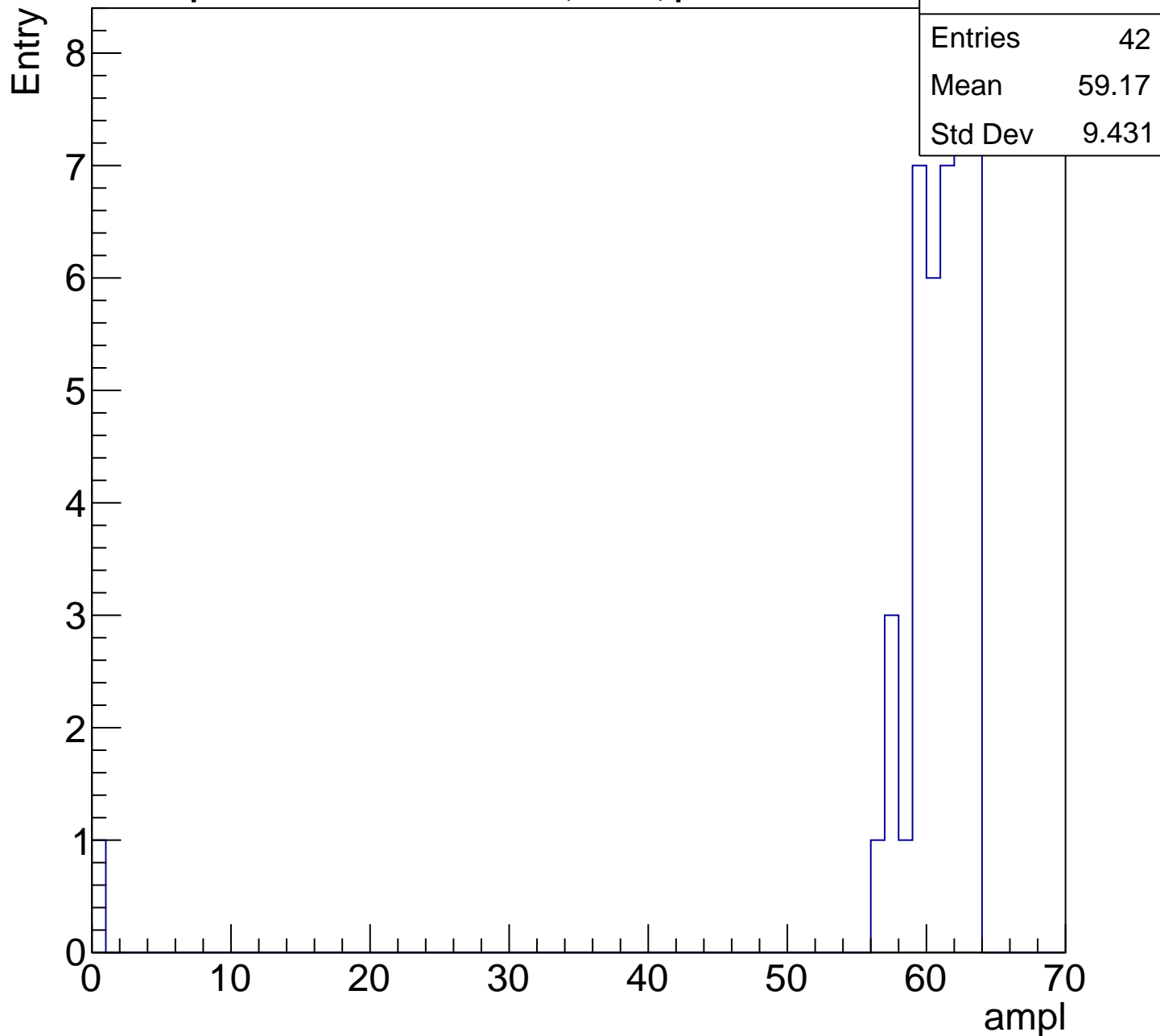
50

60

70

# B1L100S, U6-ch36, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2



# B1L100S, U6-ch36, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

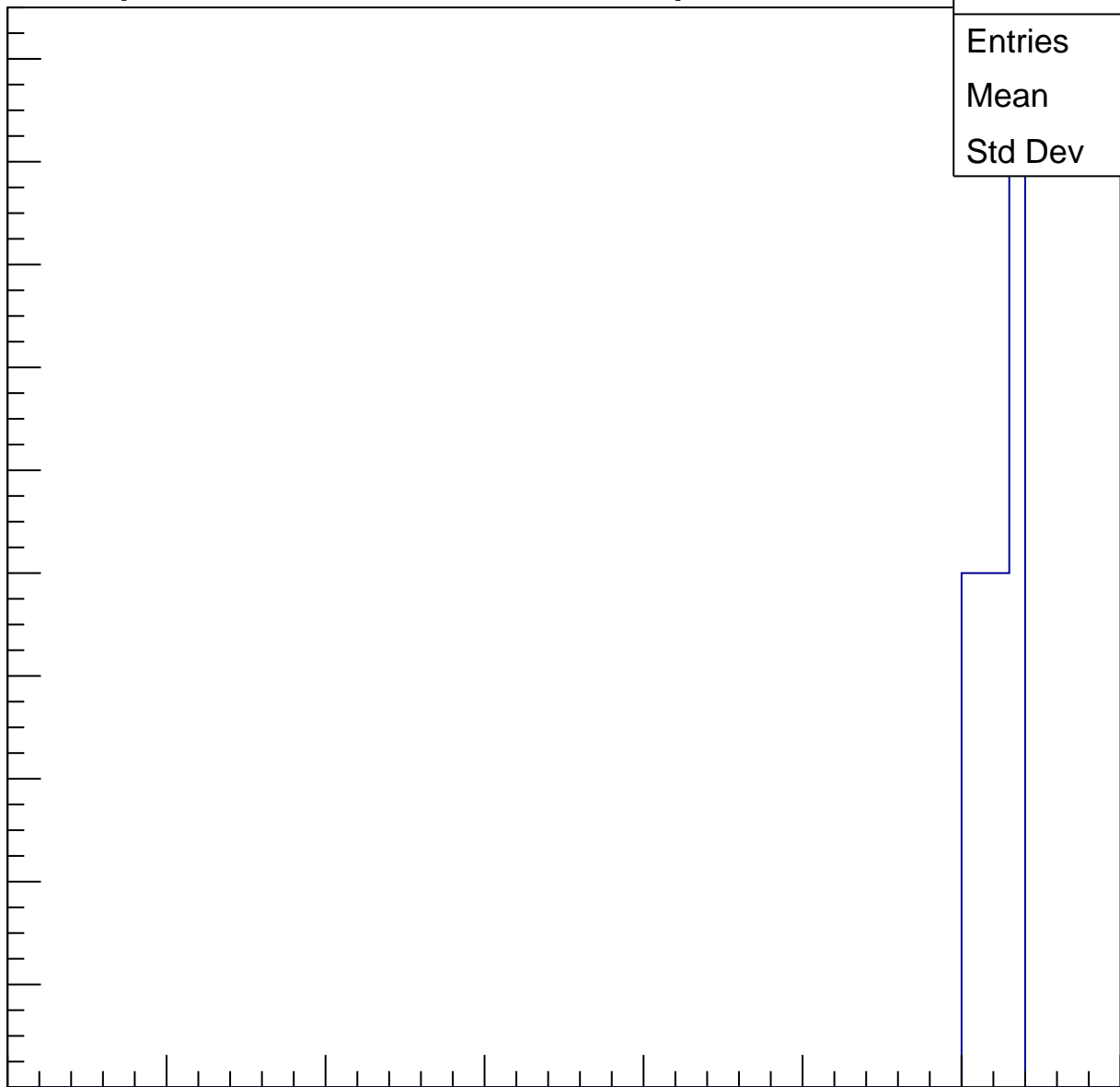
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	5
Mean	61.8
Std Dev	1.166

ampl

0 10 20 30 40 50 60 70





# B1L100S, U6-ch36, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



# B1L100S, U6-ch37, adc0

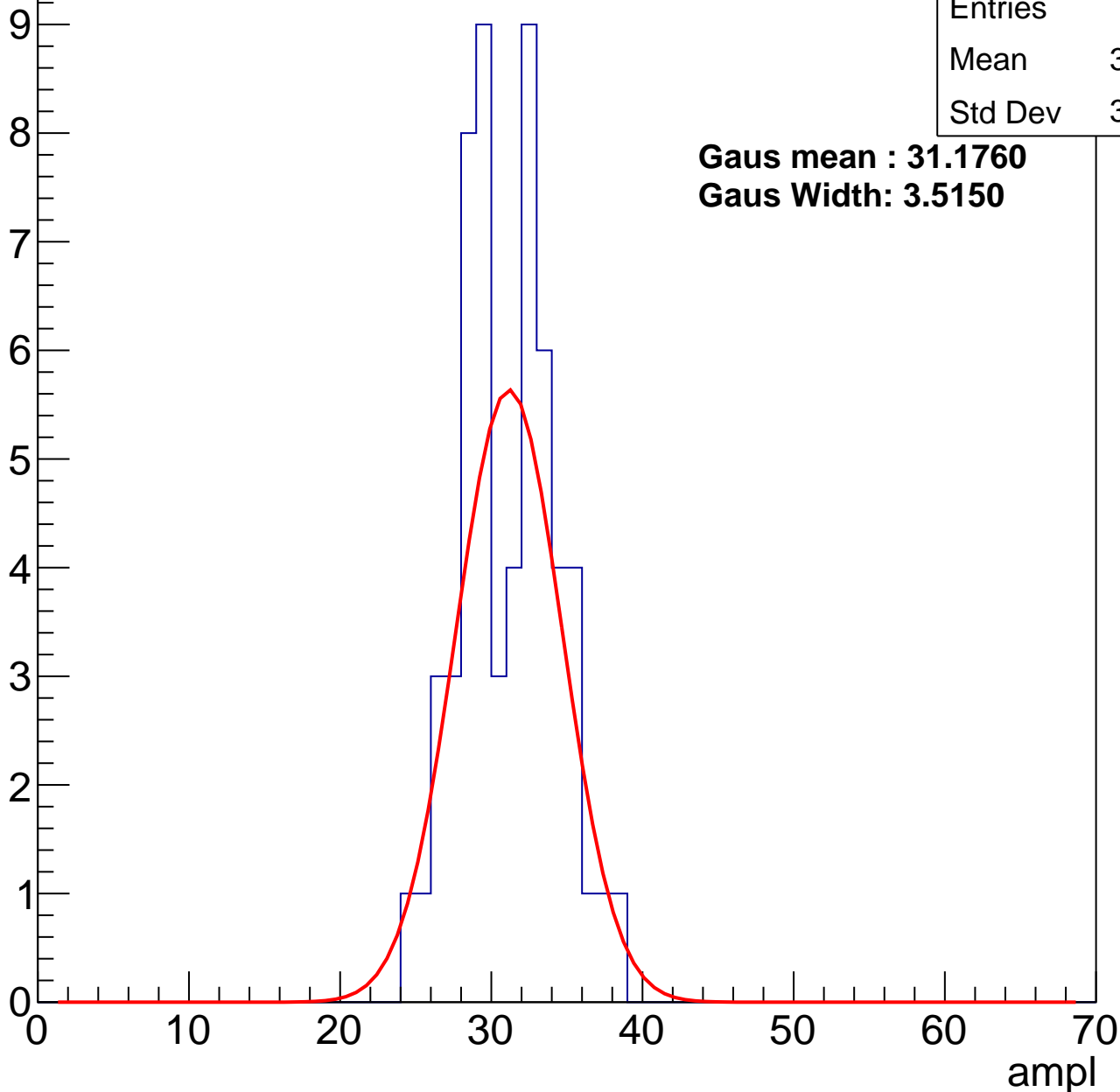
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	58
Mean	30.69
Std Dev	3.097

**Gaus mean : 31.1760**

**Gaus Width: 3.5150**



# B1L100S, U6-ch37, adc1

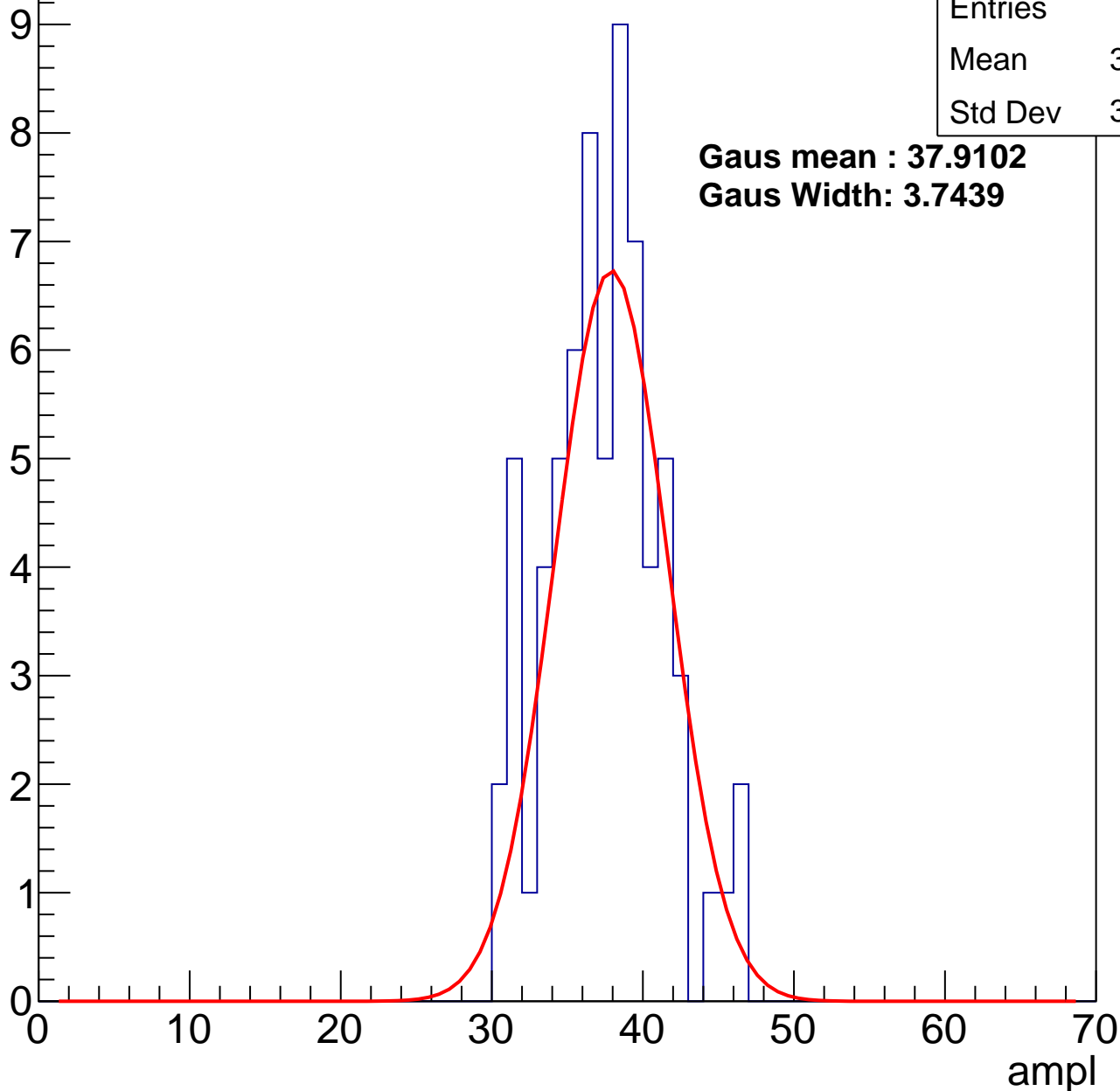
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	68
Mean	37.04
Std Dev	3.732

**Gaus mean : 37.9102**

**Gaus Width: 3.7439**



# B1L100S, U6-ch37, adc2

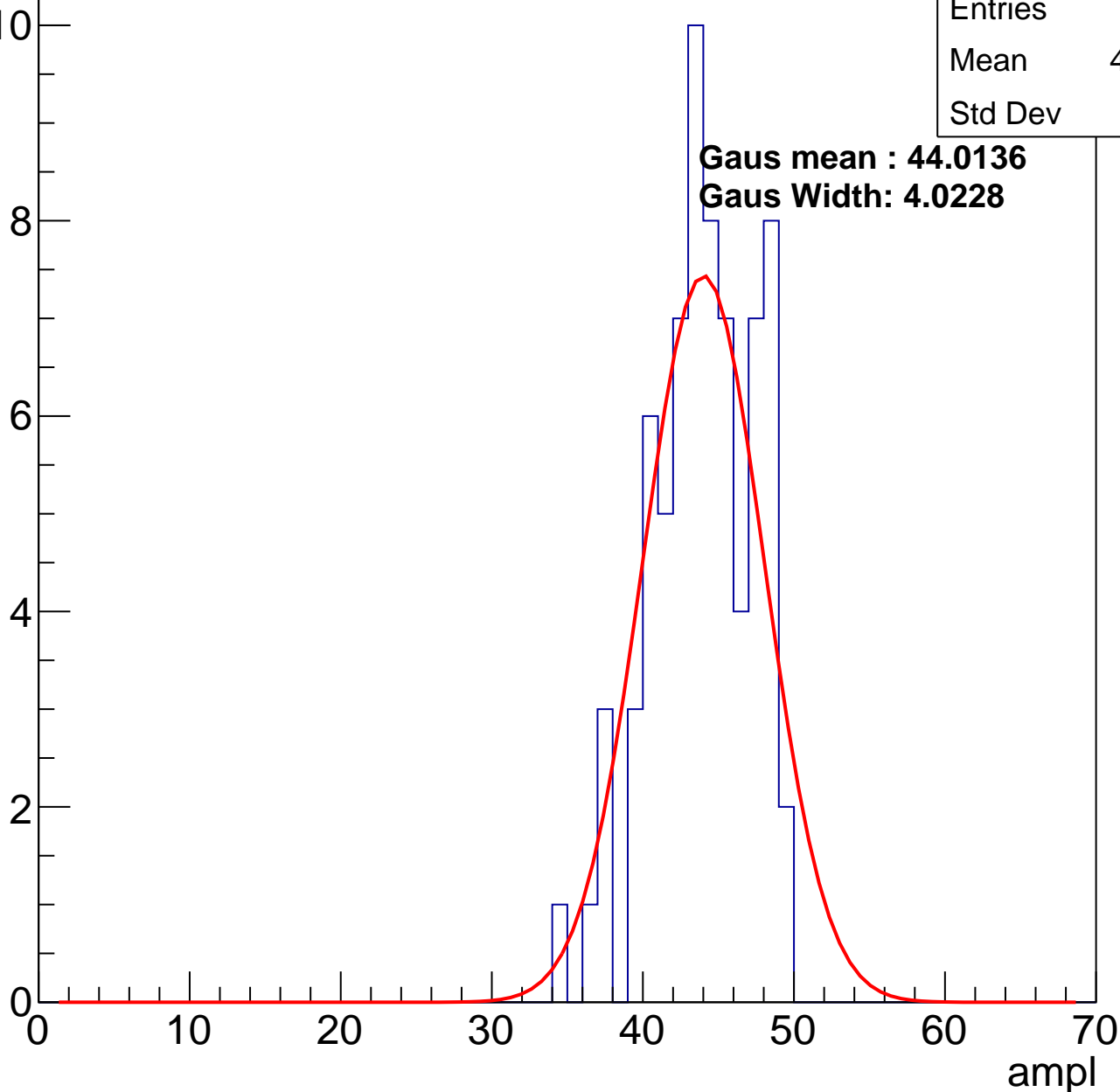
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	72
Mean	43.46
Std Dev	3.35

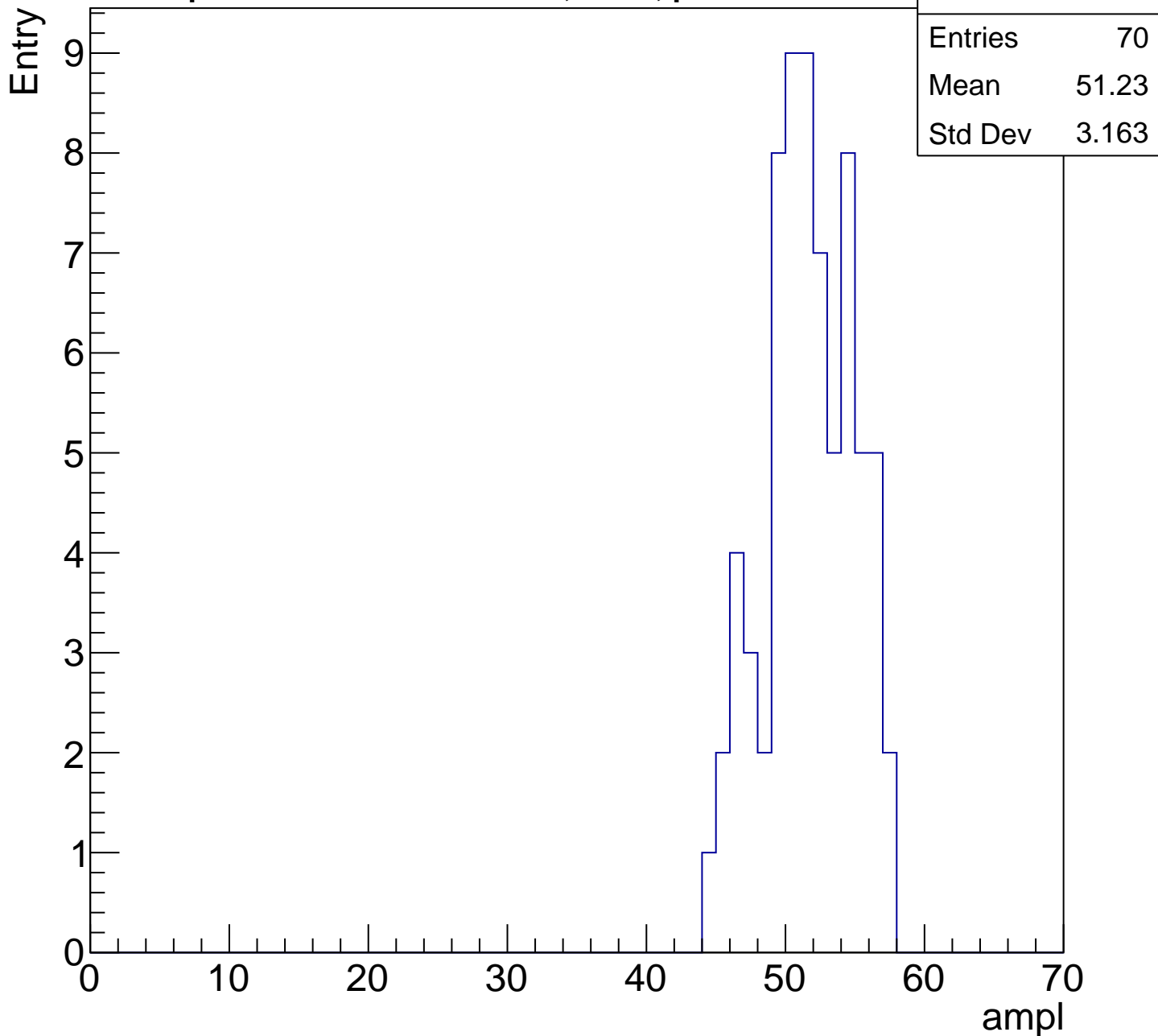
**Gaus mean : 44.0136**

**Gaus Width: 4.0228**



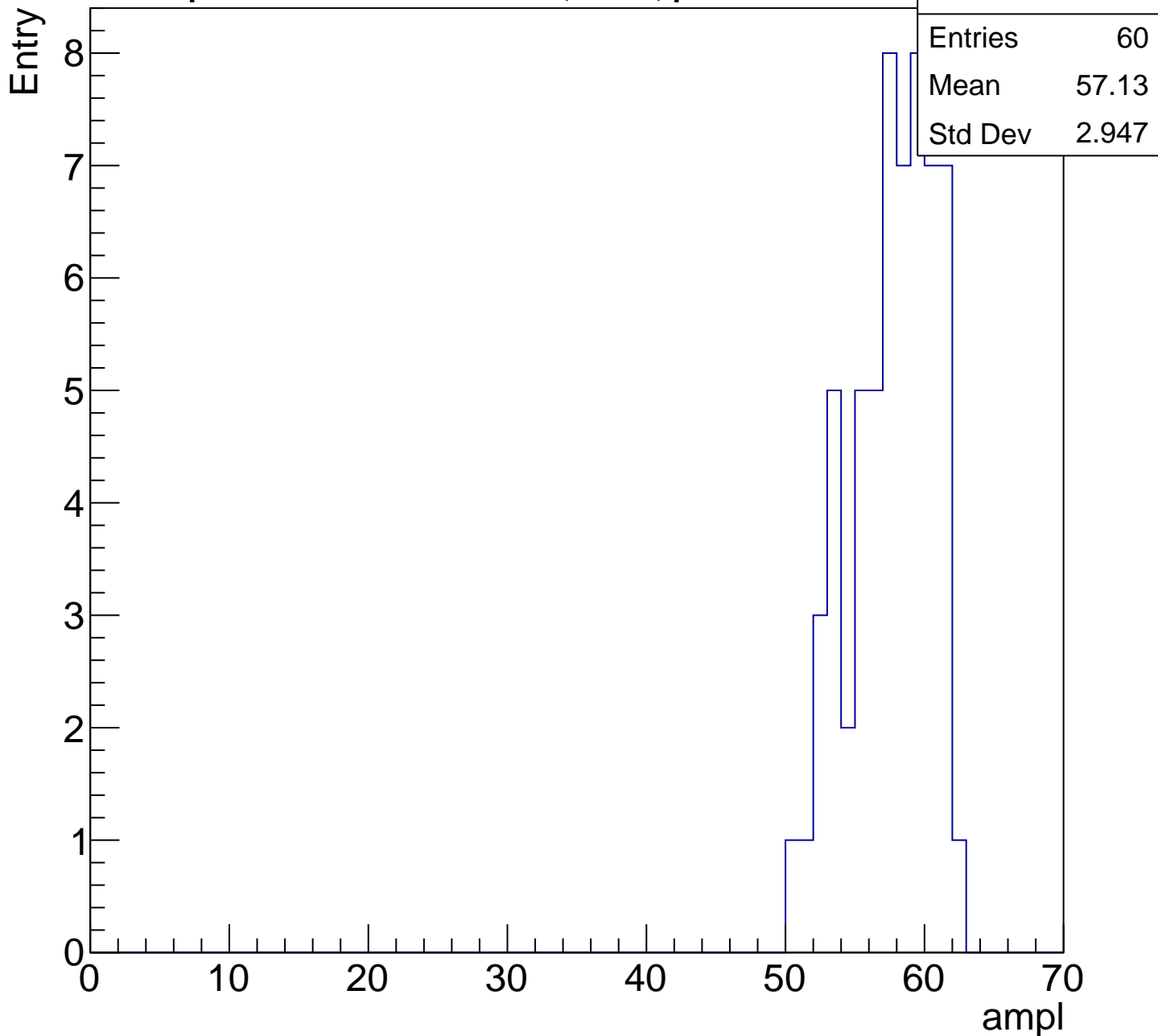
# B1L100S, U6-ch37, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2



# B1L100S, U6-ch37, adc4

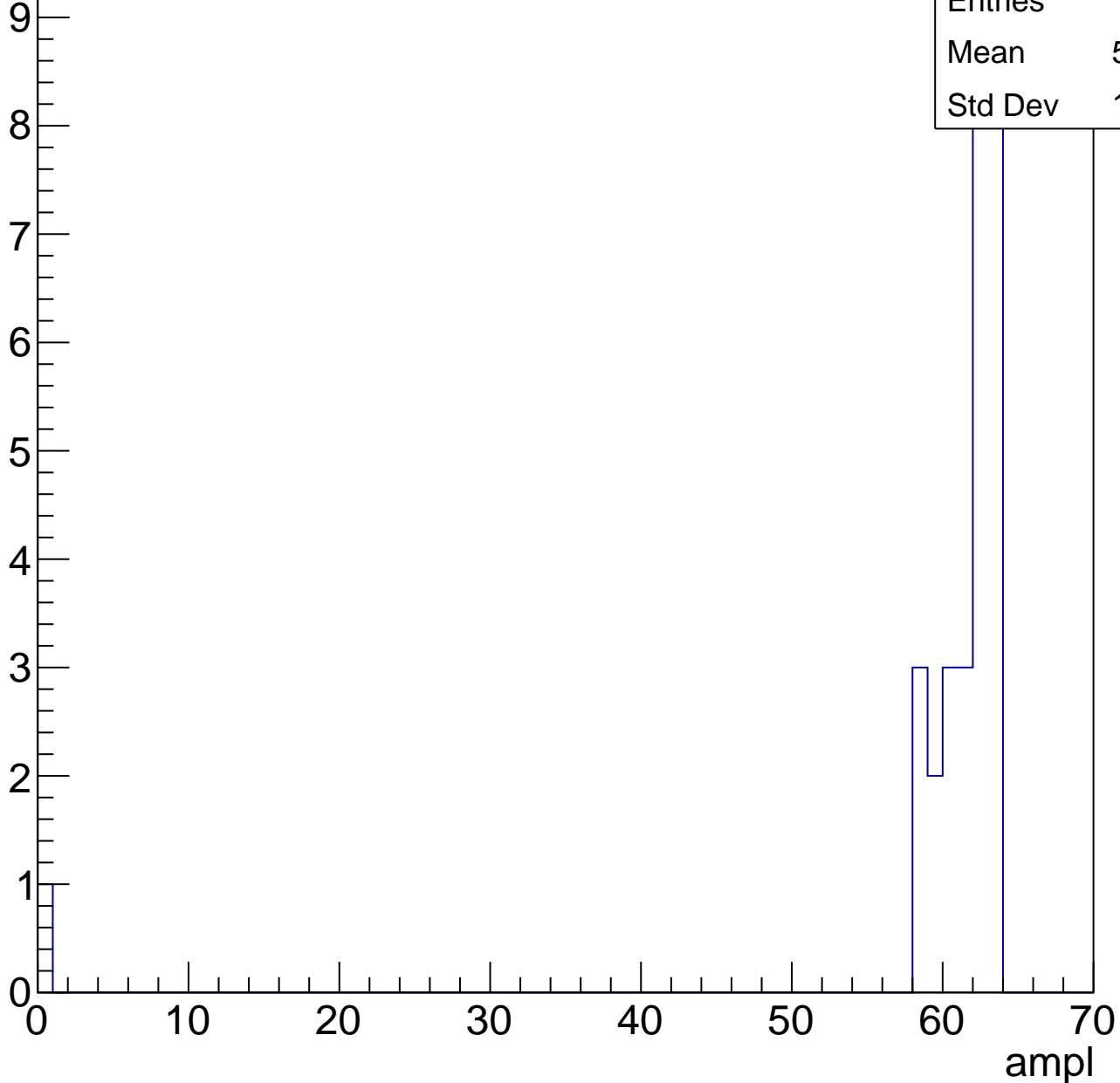
calib\_packv5\_042523\_0143.root, FC#4, port A2



# B1L100S, U6-ch37, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



# B1L100S, U6-ch37, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	2
Mean	63
Std Dev	0

0 10 20 30 40 50 60 70

ampl



# B1L100S, U6-ch37, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

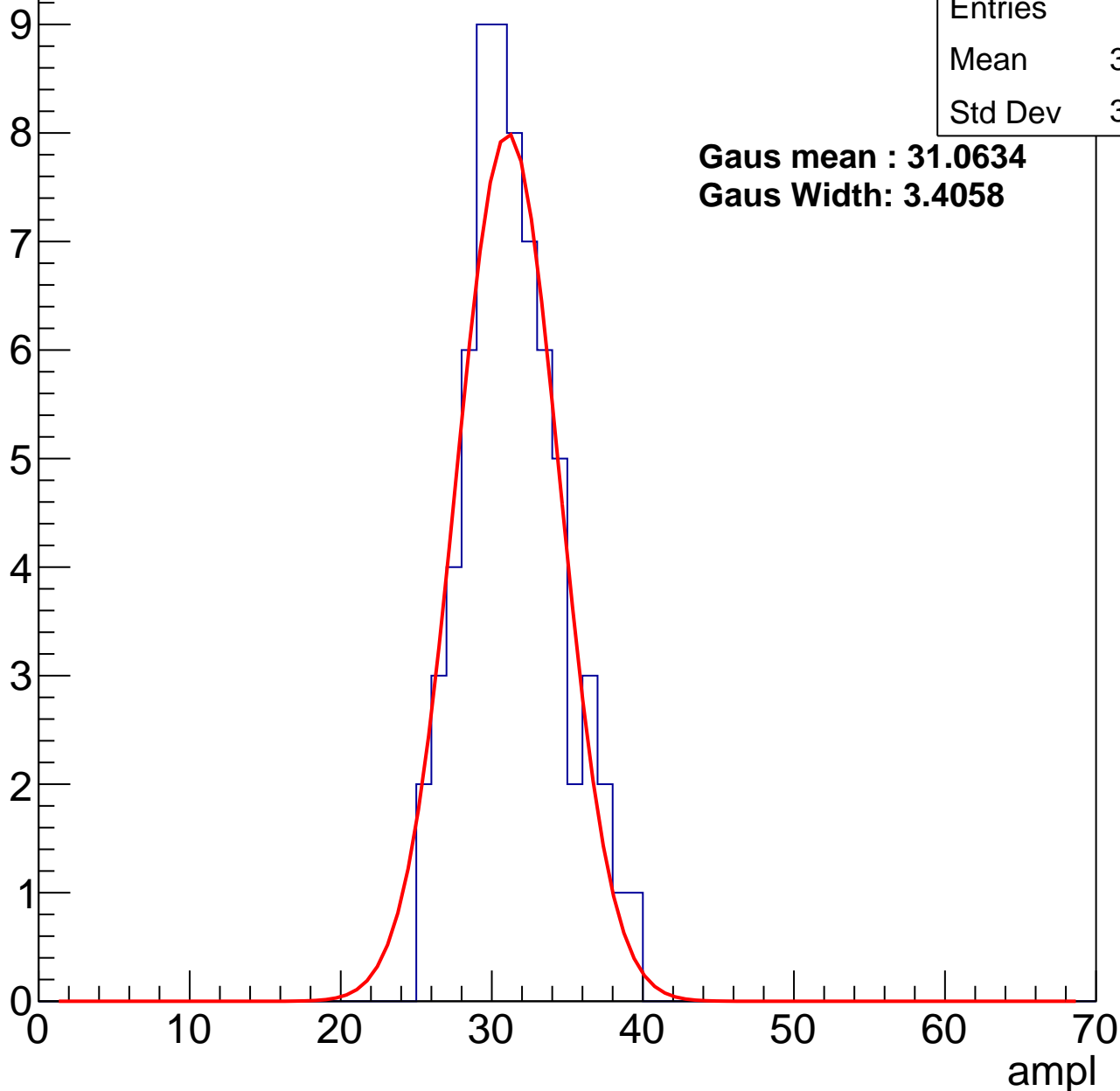


Entries	1
Mean	19
Std Dev	0

# B1L100S, U6-ch38, adc0

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



# B1L100S, U6-ch38, adc1

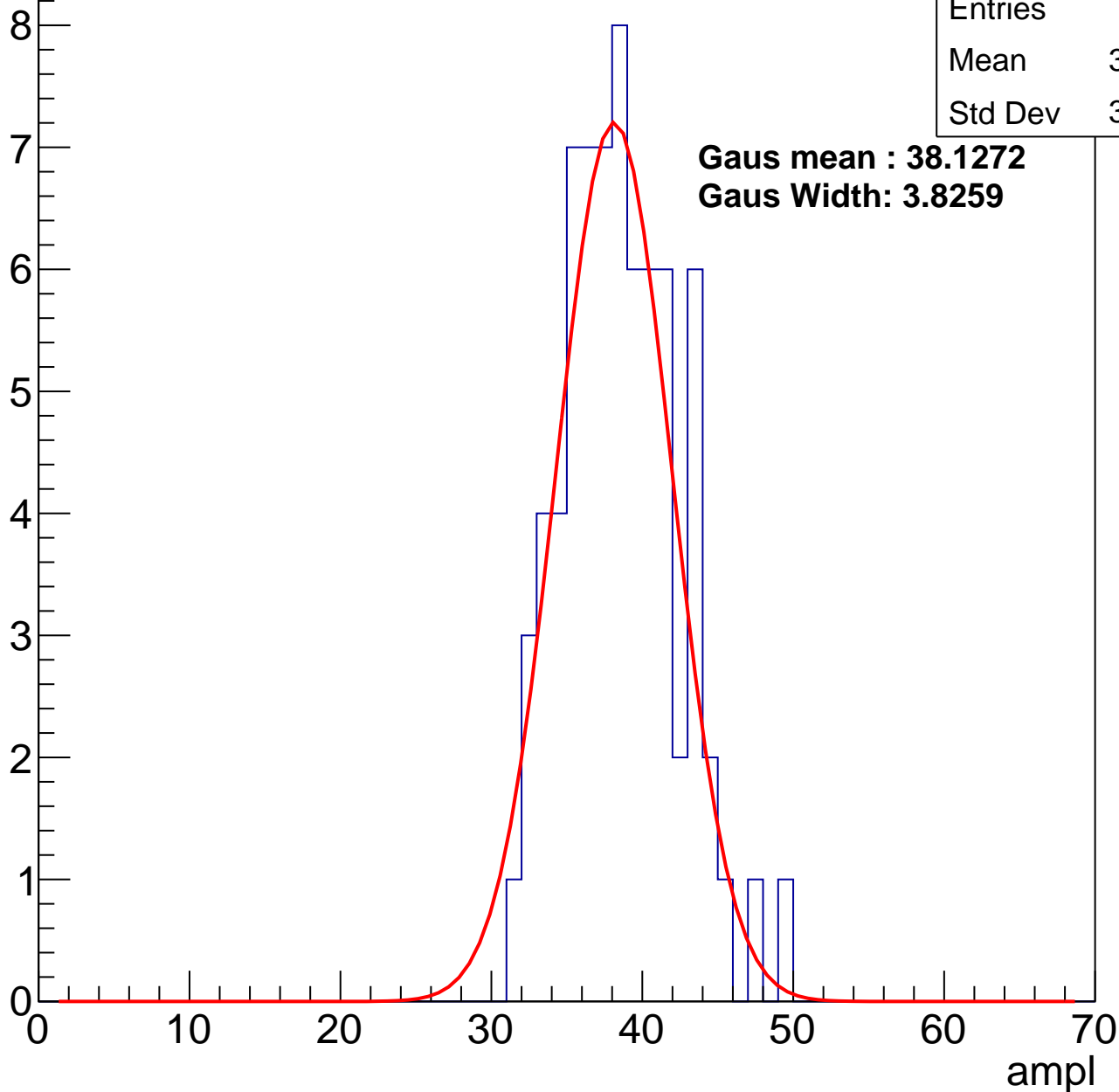
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	72
Mean	38.14
Std Dev	3.739

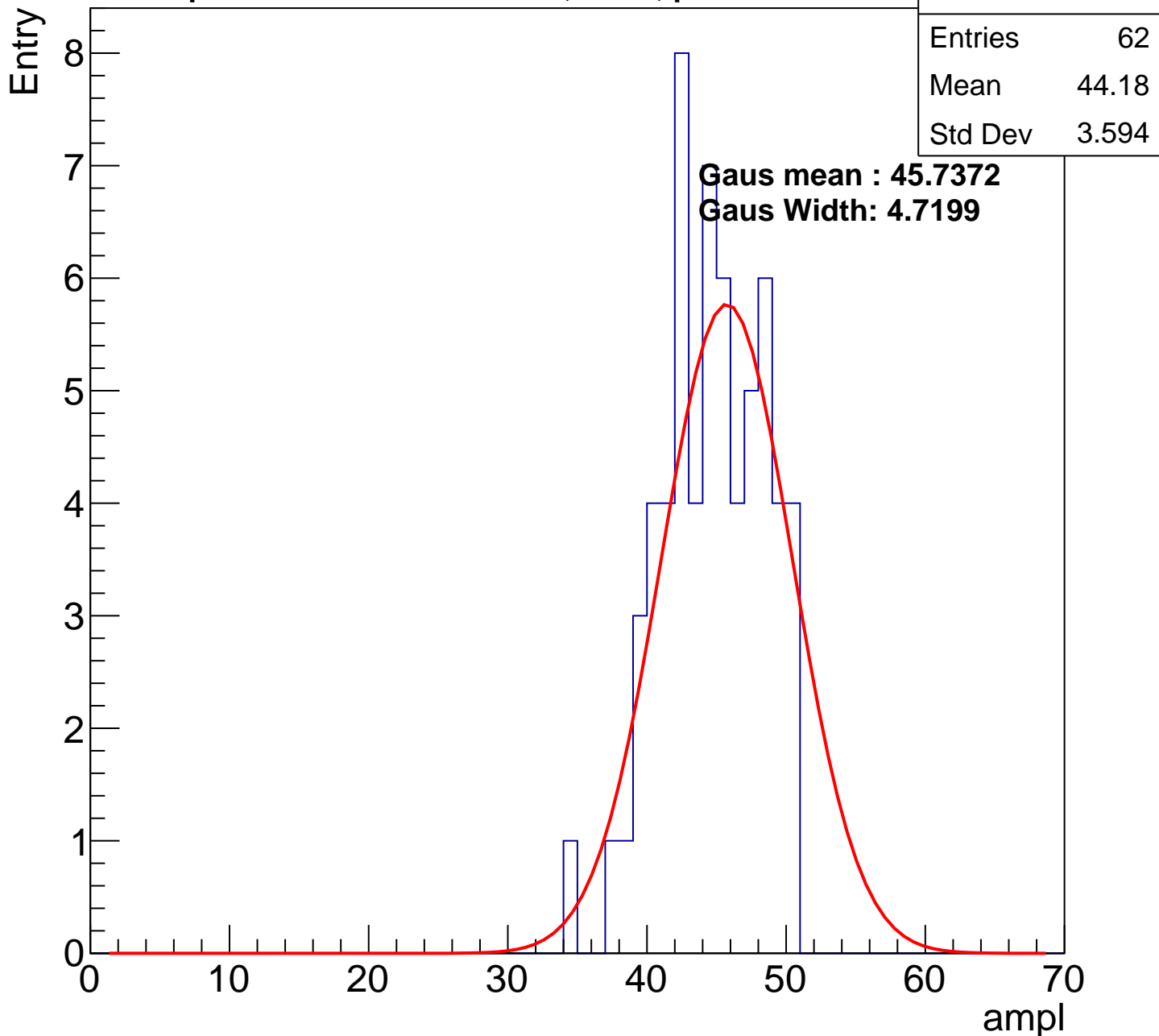
**Gaus mean : 38.1272**

**Gaus Width: 3.8259**



# B1L100S, U6-ch38, adc2

calib\_packv5\_042523\_0143.root, FC#4, port A2



# B1L100S, U6-ch38, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	63
Mean	50.49
Std Dev	3.265

Entry

10

8

6

4

2

0

0

10

20

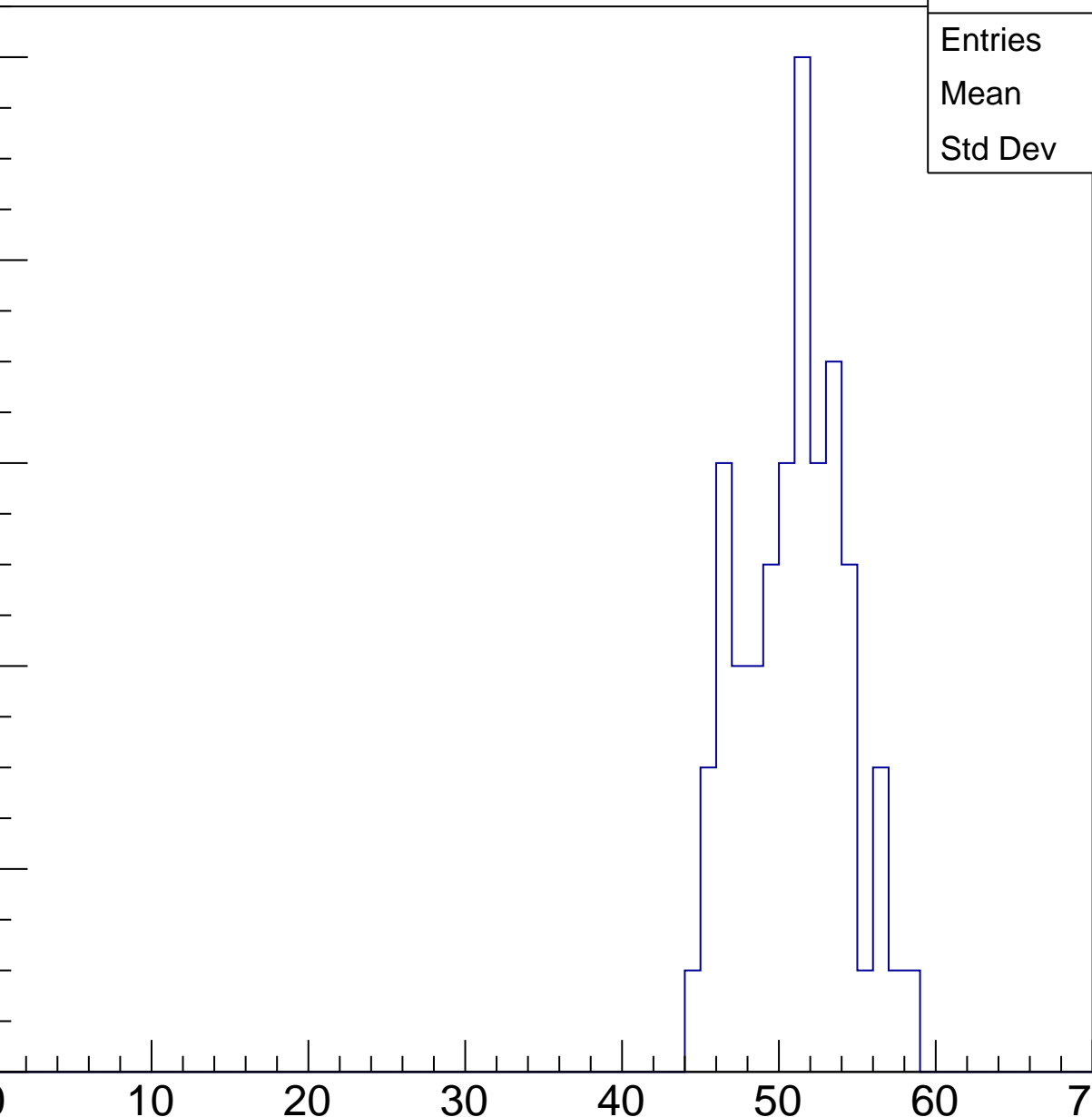
30

40

50

60

ampl

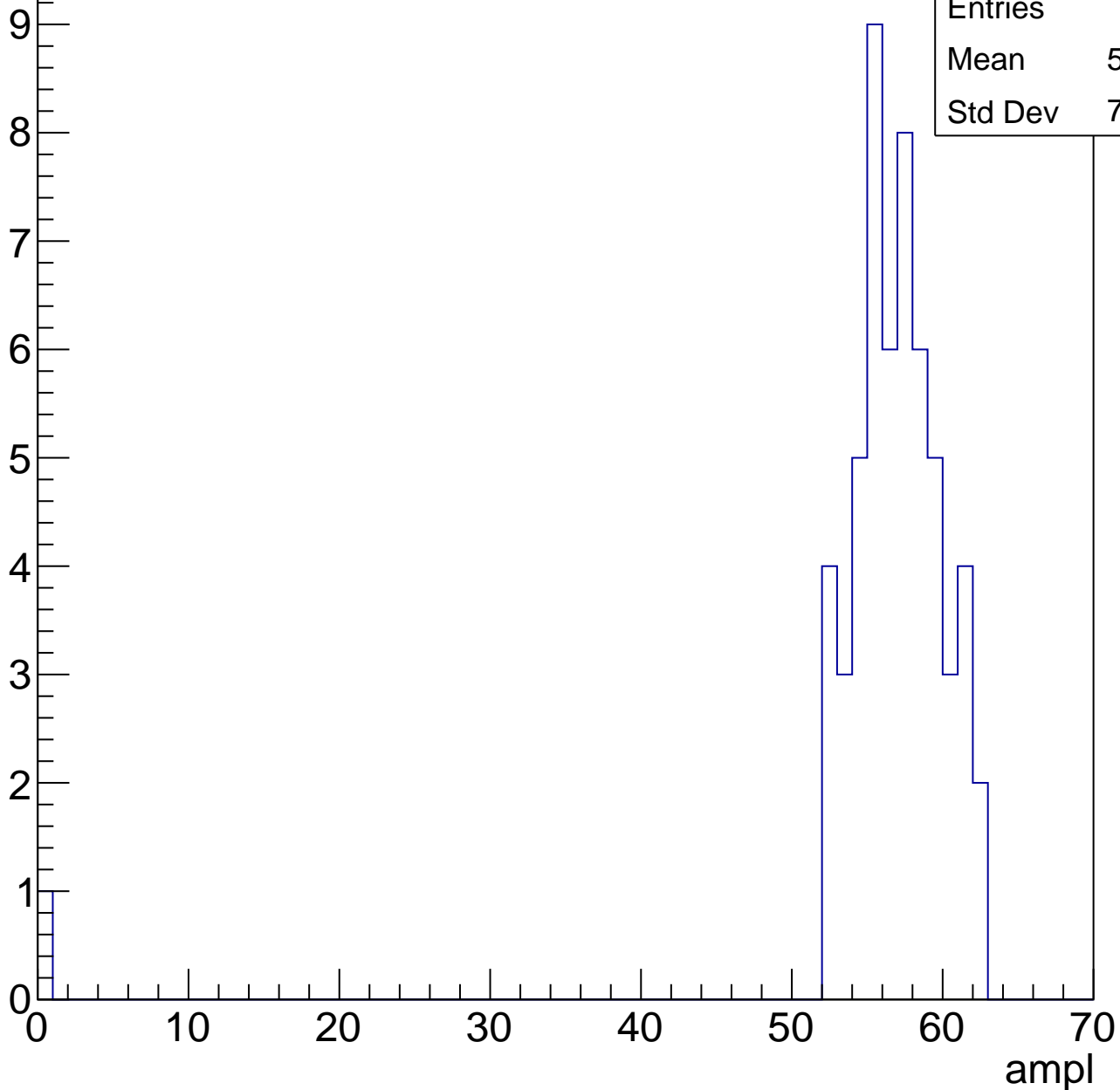


# B1L100S, U6-ch38, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	56
Mean	55.62
Std Dev	7.956



# B1L100S, U6-ch38, adc5

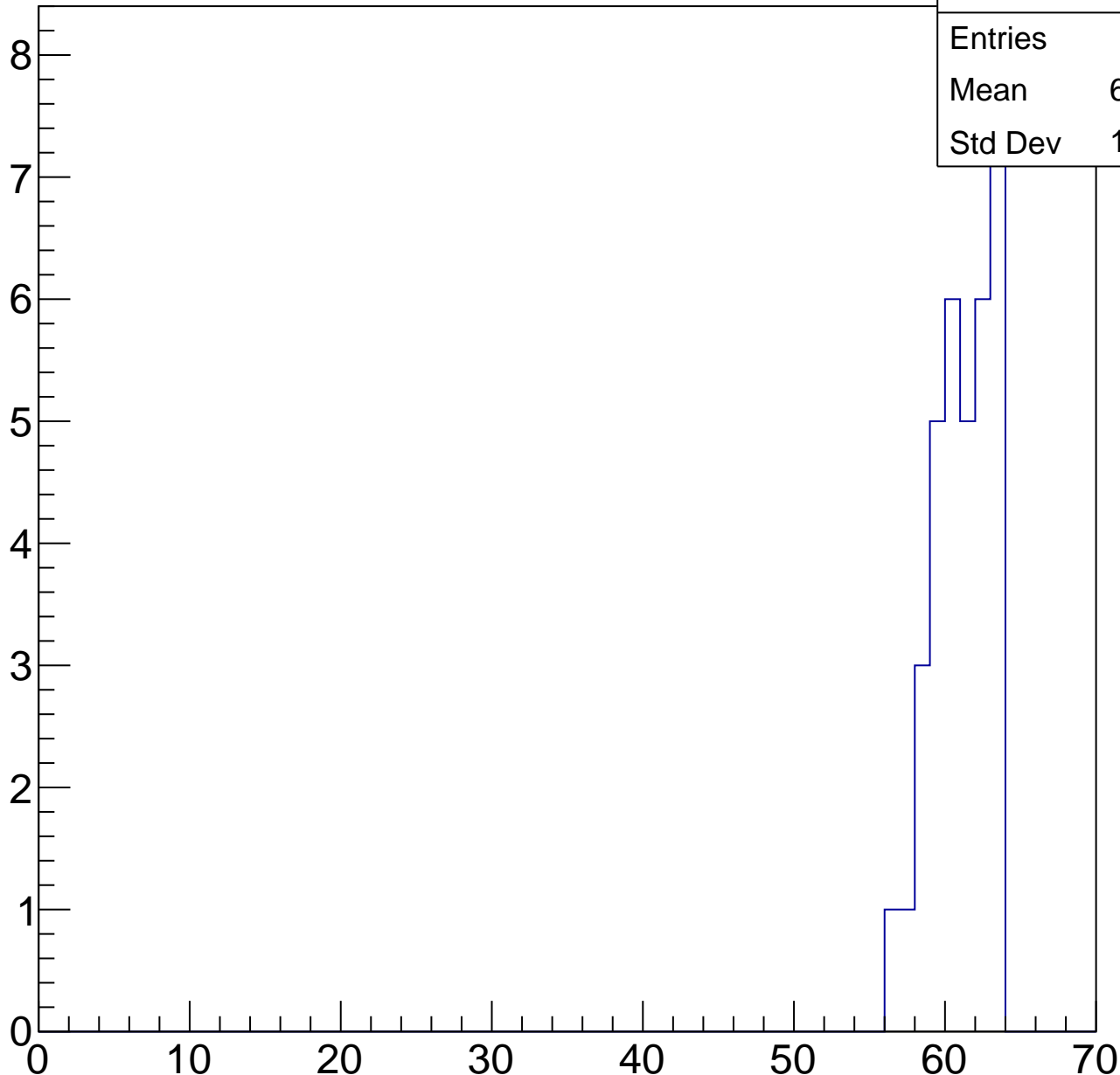
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	35
Mean	60.66
Std Dev	1.912

ampl



# B1L100S, U6-ch38, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	6
Mean	61.83
Std Dev	1.067

ampl

0 10 20 30 40 50 60 70



# B1L100S, U6-ch38, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

1  
0.8  
0.6  
0.4  
0.2  
0

Entries	1
Mean	25
Std Dev	0

ampl

# B1L100S, U6-ch39, adc0

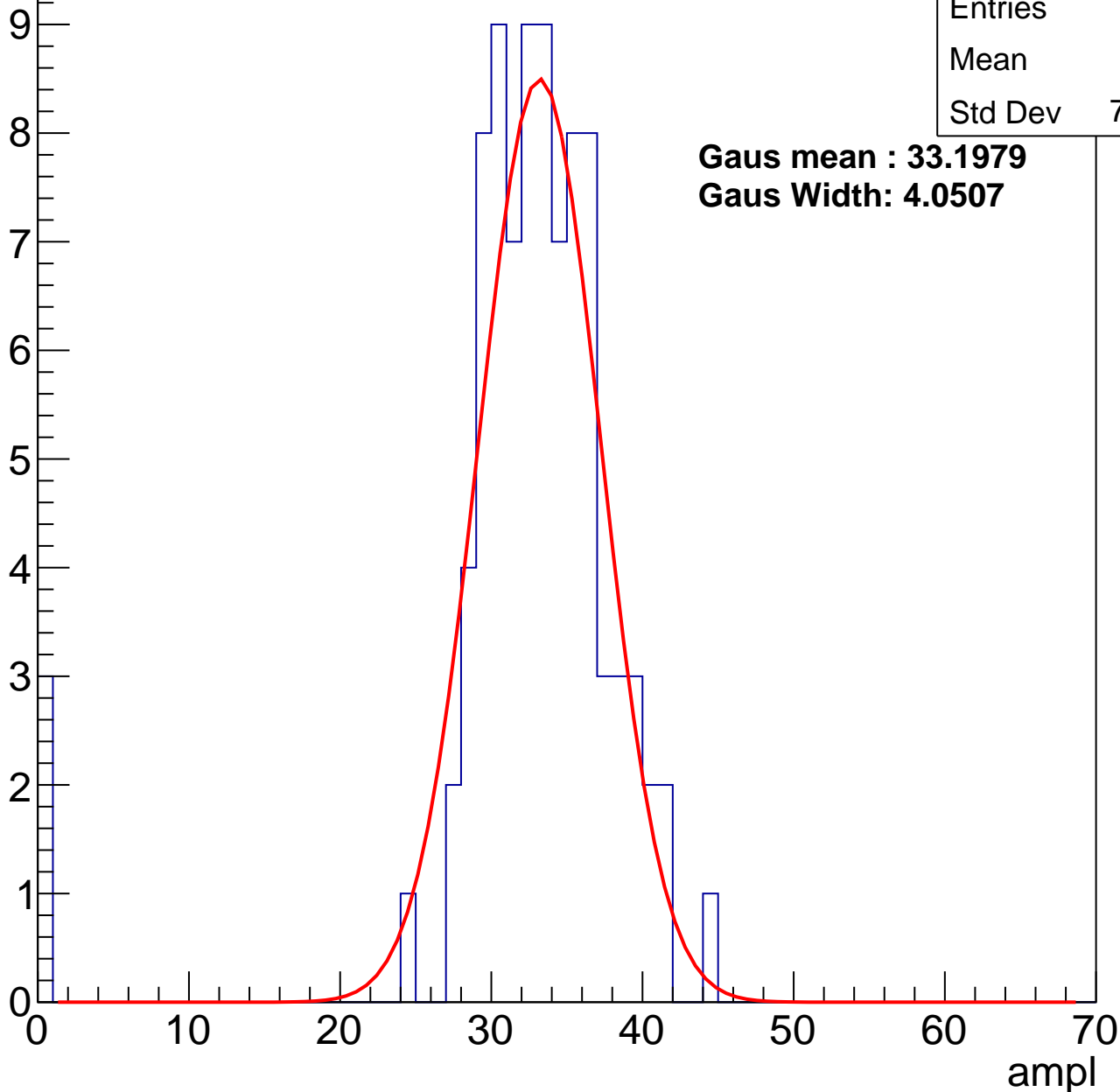
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	89
Mean	32
Std Dev	7.004

**Gaus mean : 33.1979**

**Gaus Width: 4.0507**



# B1L100S, U6-ch39, adc1

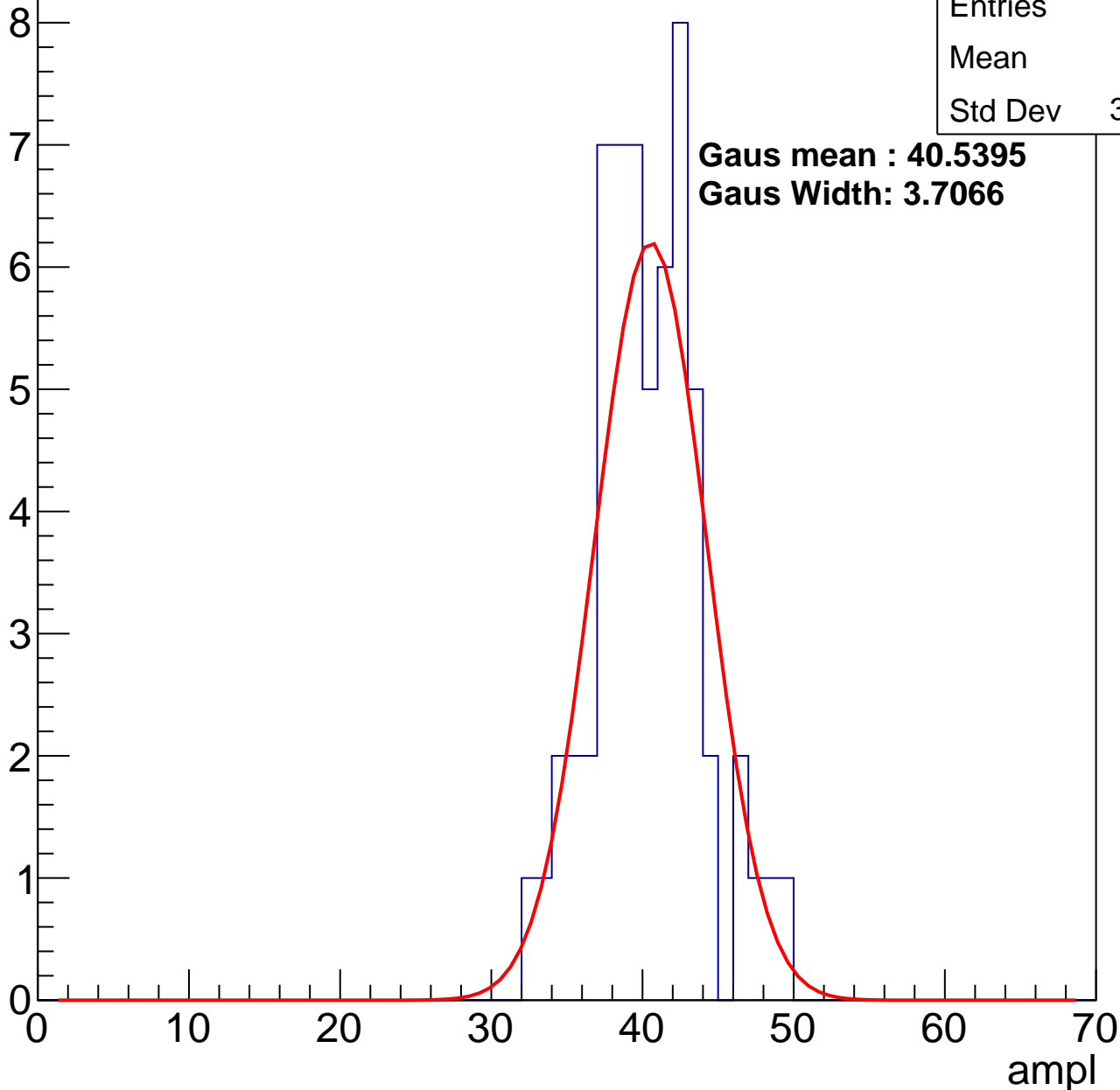
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	60
Mean	39.9
Std Dev	3.525

**Gaus mean : 40.5395**

**Gaus Width: 3.7066**



# B1L100S, U6-ch39, adc2

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	70
Mean	46.79
Std Dev	3.633

**Gaus mean : 46.9317**

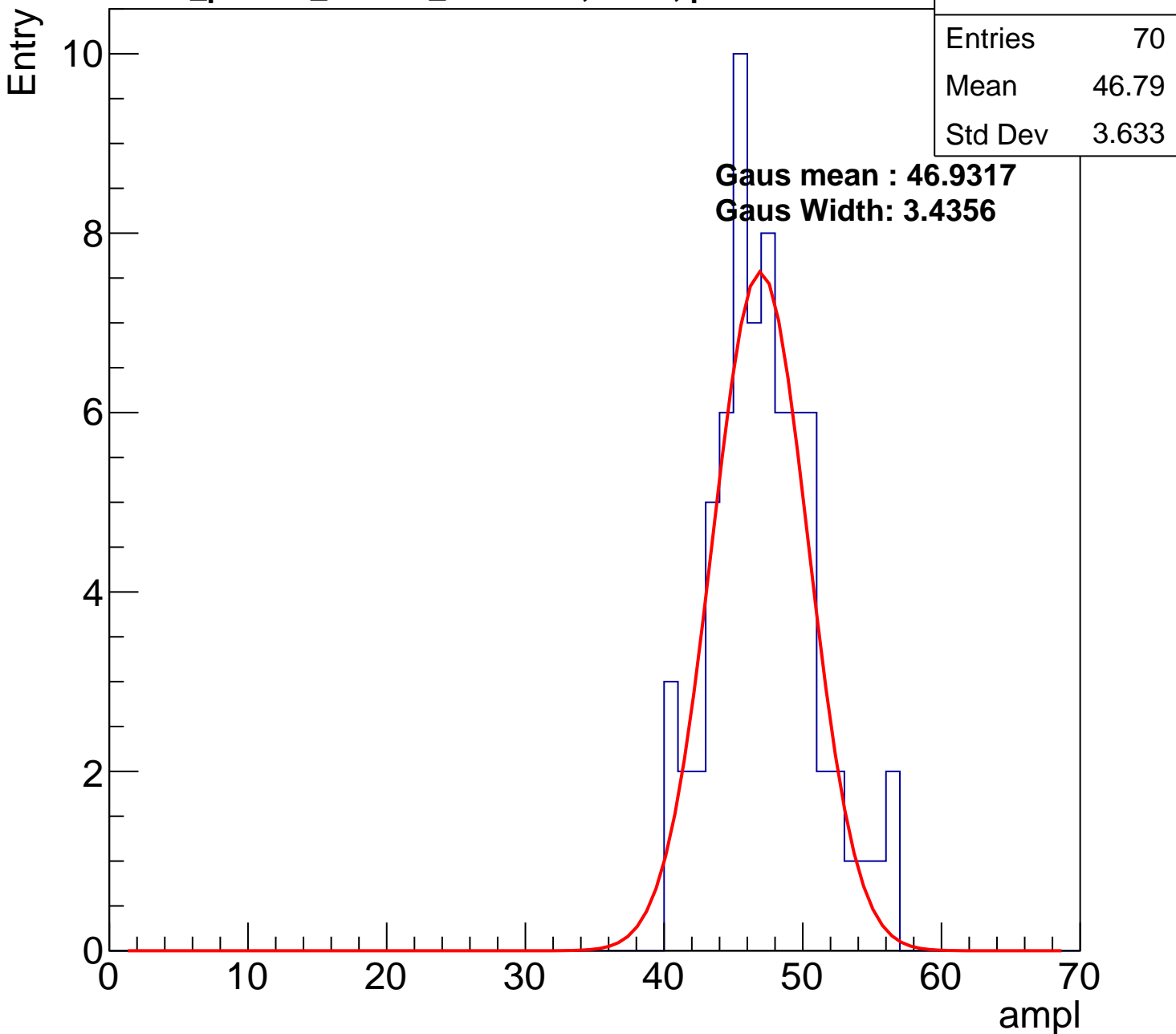
**Gaus Width: 3.4356**

Entry

10  
8  
6  
4  
2  
0

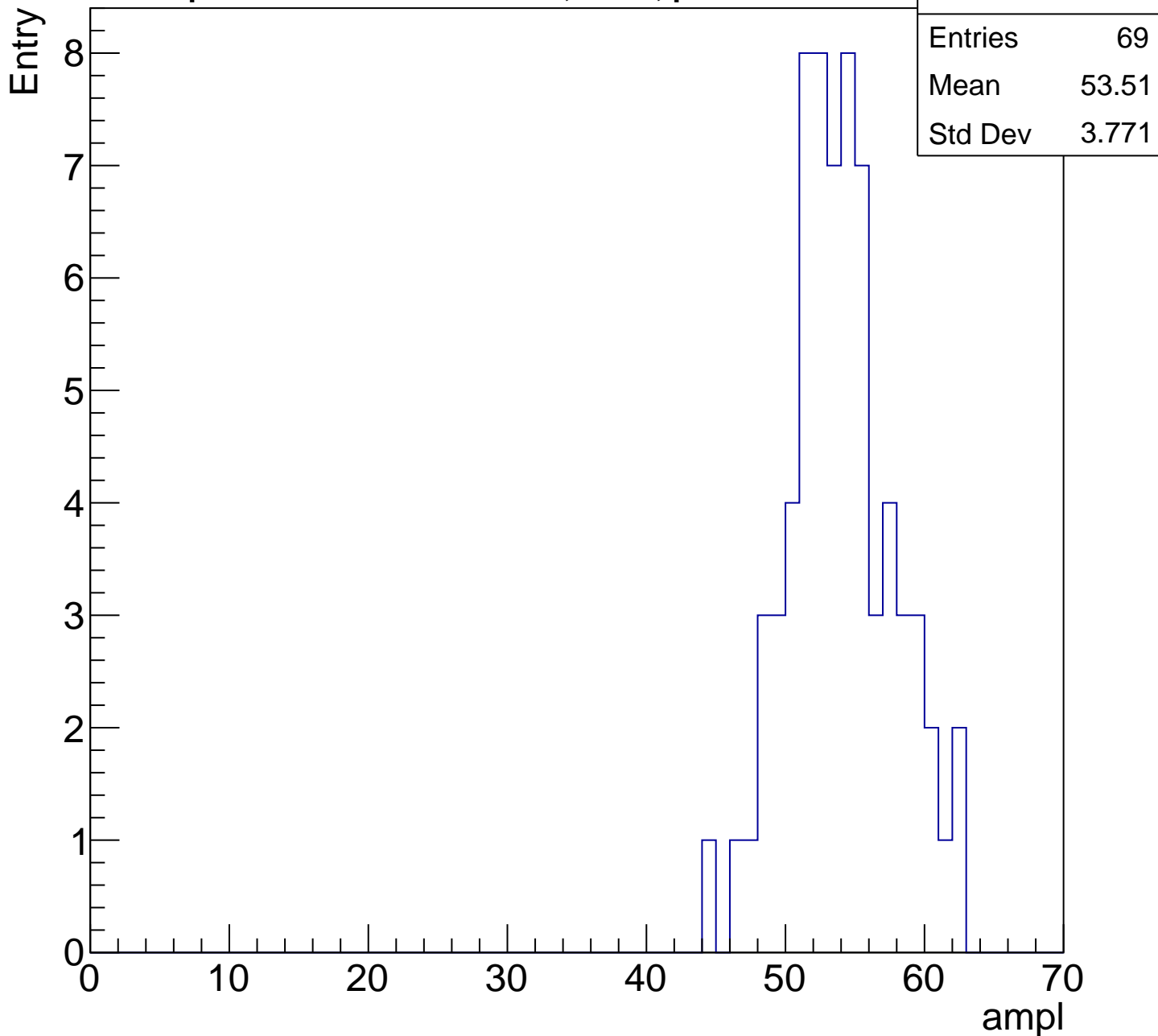
ampl

0 10 20 30 40 50 60 70



# B1L100S, U6-ch39, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2



# B1L100S, U6-ch39, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

7

6

5

4

3

2

1

0

Entries

54

Mean

57.8

Std Dev

8.336

ampl

0

10

20

30

40

50

60

70

# B1L100S, U6-ch39, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

7

6

5

4

3

2

1

0

Entries

12

Mean

62.08

Std Dev

1.187

ampl

0

10

20

30

40

50

60

70

# B1L100S, U6-ch39, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	0
Mean	0
Std Dev	0



# B1L100S, U6-ch39, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L100S, U6-ch40, adc0

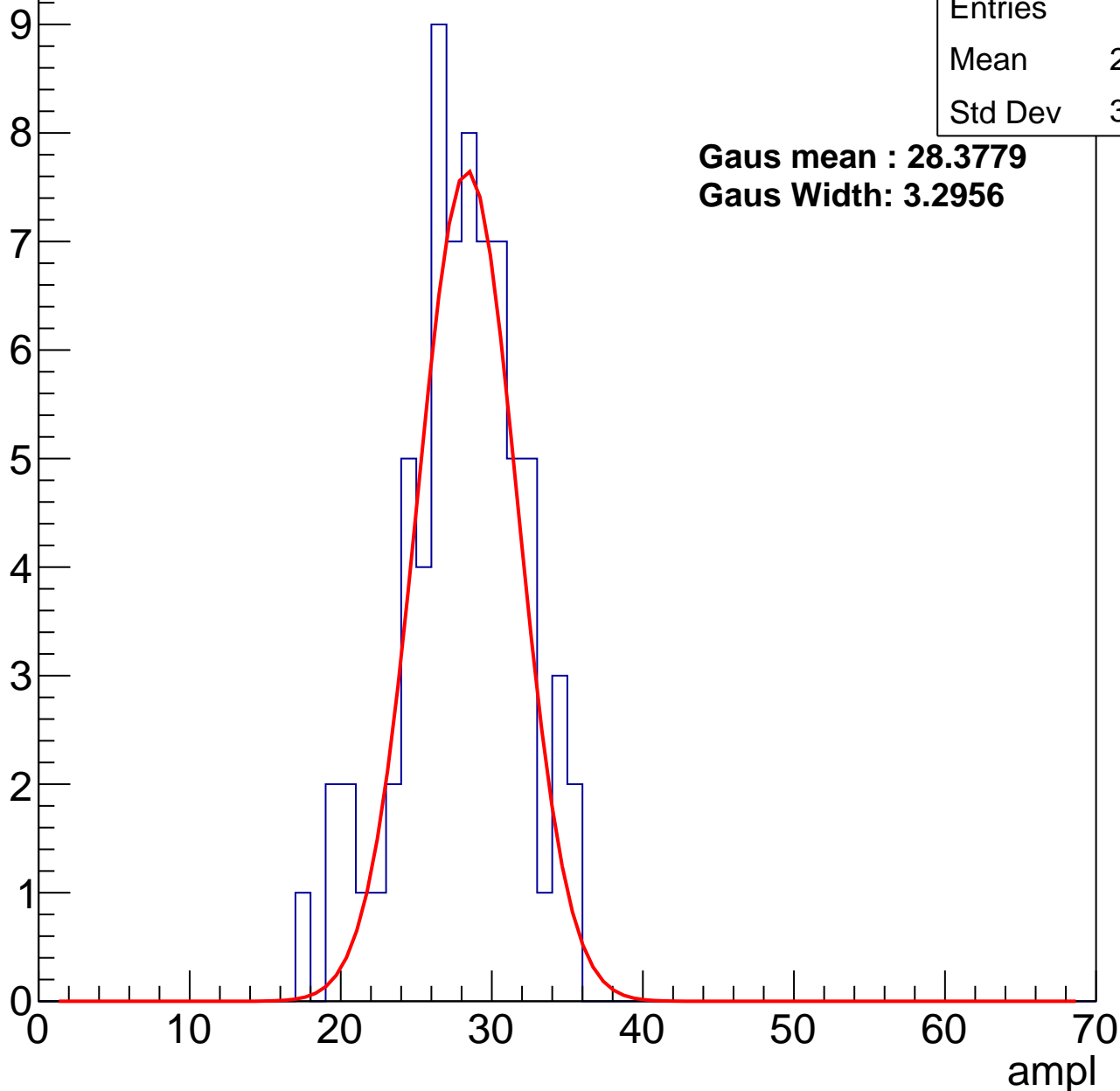
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	72
Mean	27.56
Std Dev	3.876

**Gaus mean : 28.3779**

**Gaus Width: 3.2956**



# B1L100S, U6-ch40, adc1

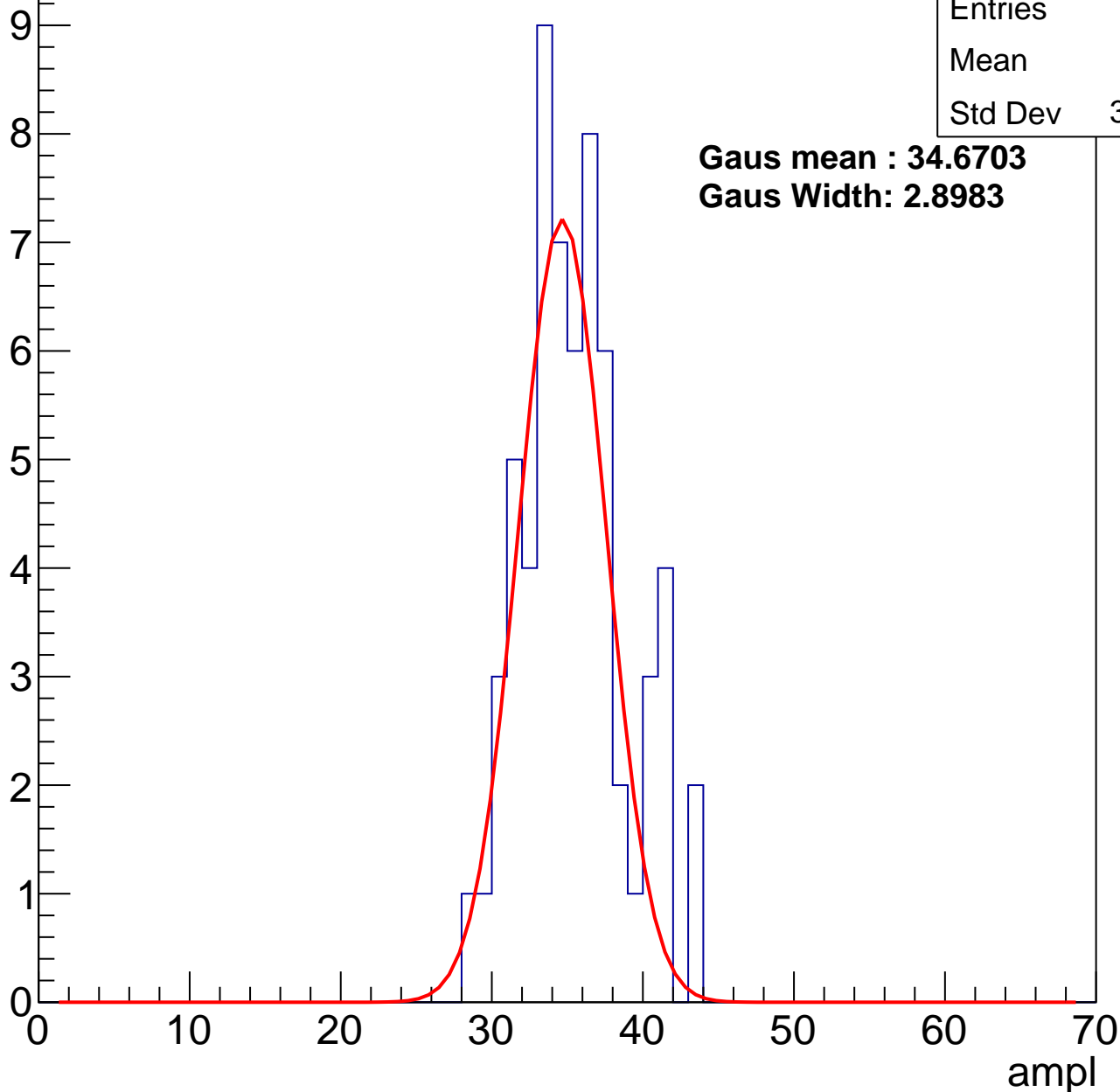
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	62
Mean	35
Std Dev	3.436

**Gaus mean : 34.6703**

**Gaus Width: 2.8983**



# B1L100S, U6-ch40, adc2

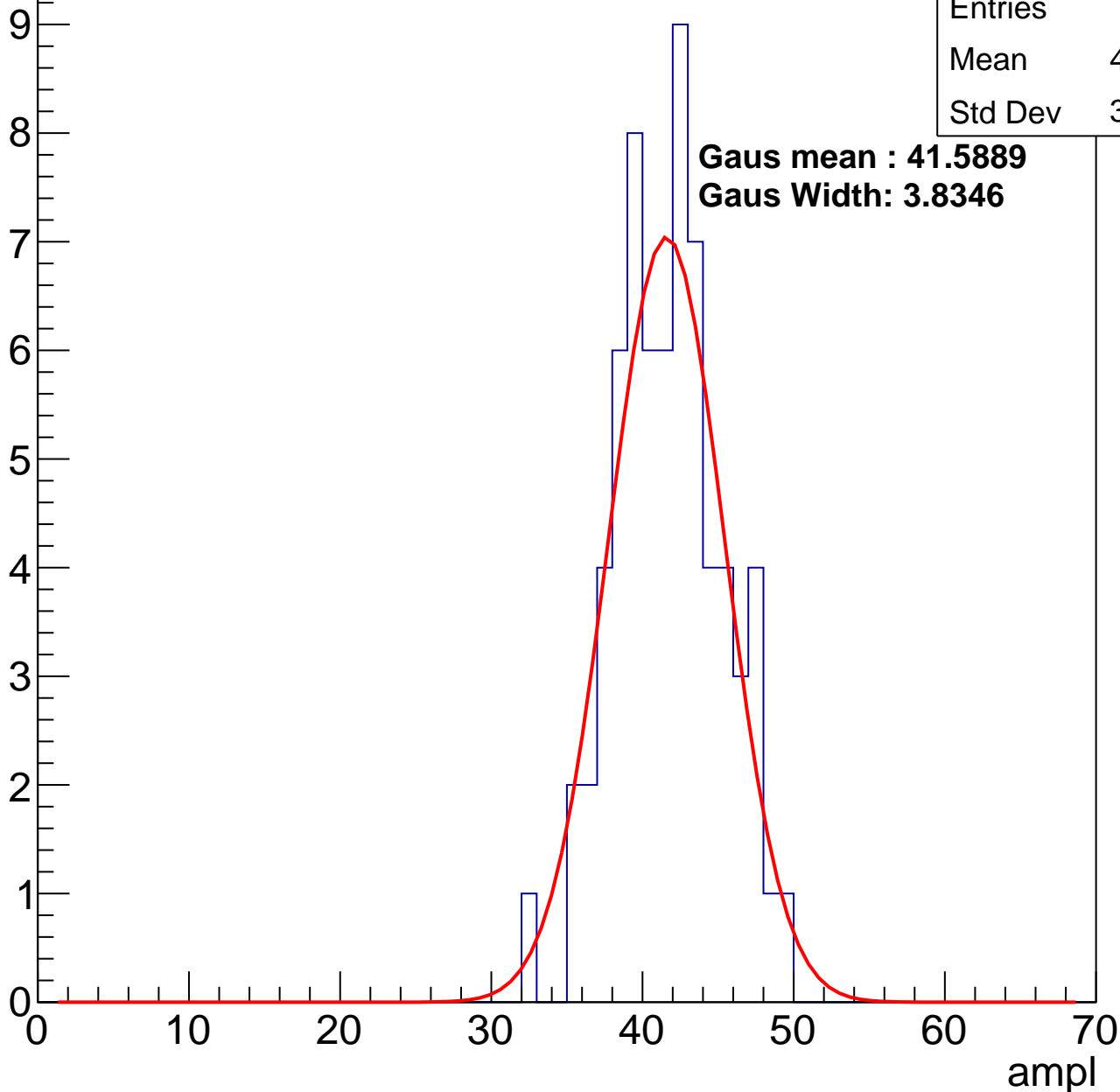
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	68
Mean	41.26
Std Dev	3.479

**Gaus mean : 41.5889**

**Gaus Width: 3.8346**

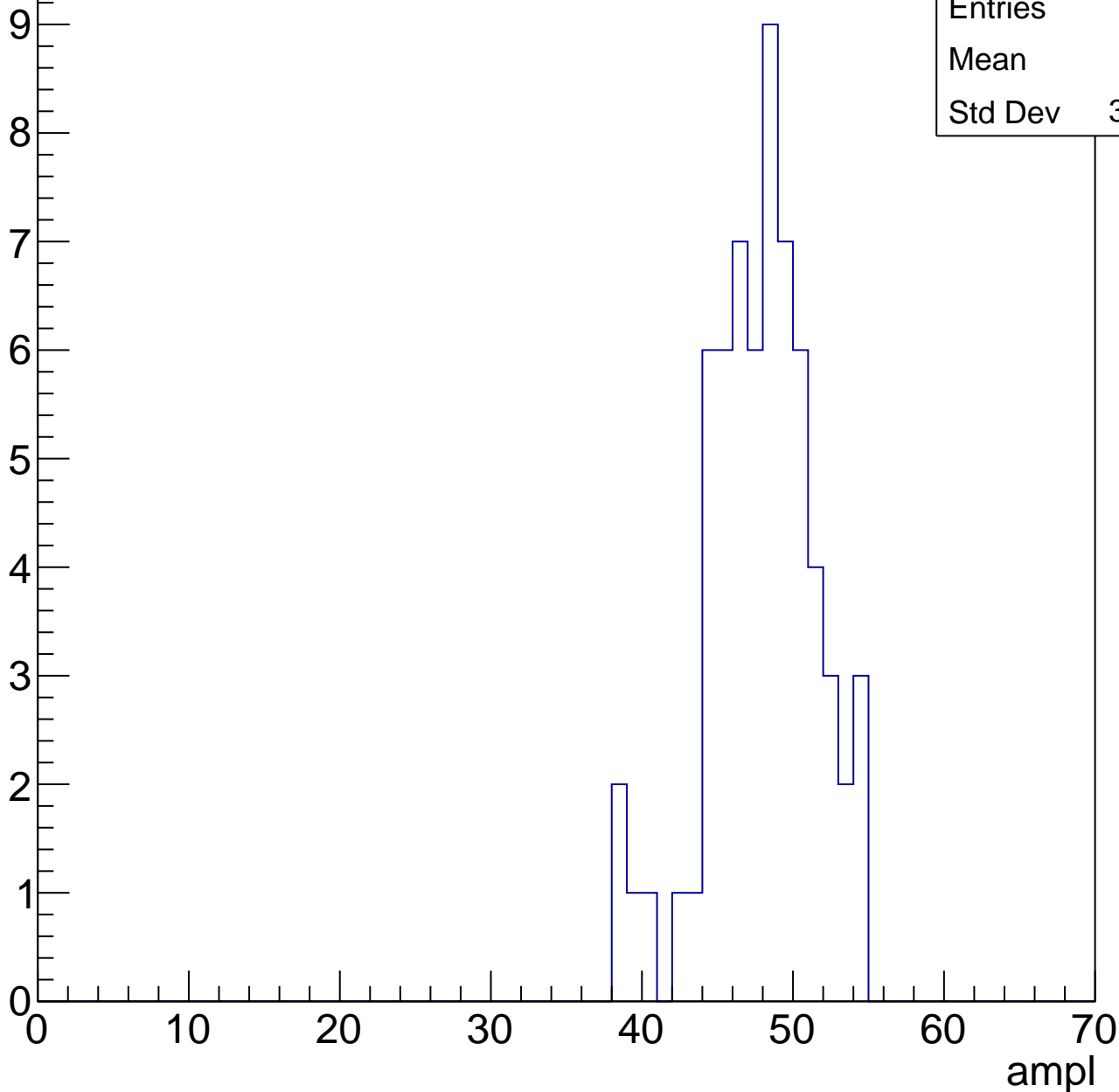


# B1L100S, U6-ch40, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	65
Mean	47.4
Std Dev	3.594



# B1L100S, U6-ch40, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

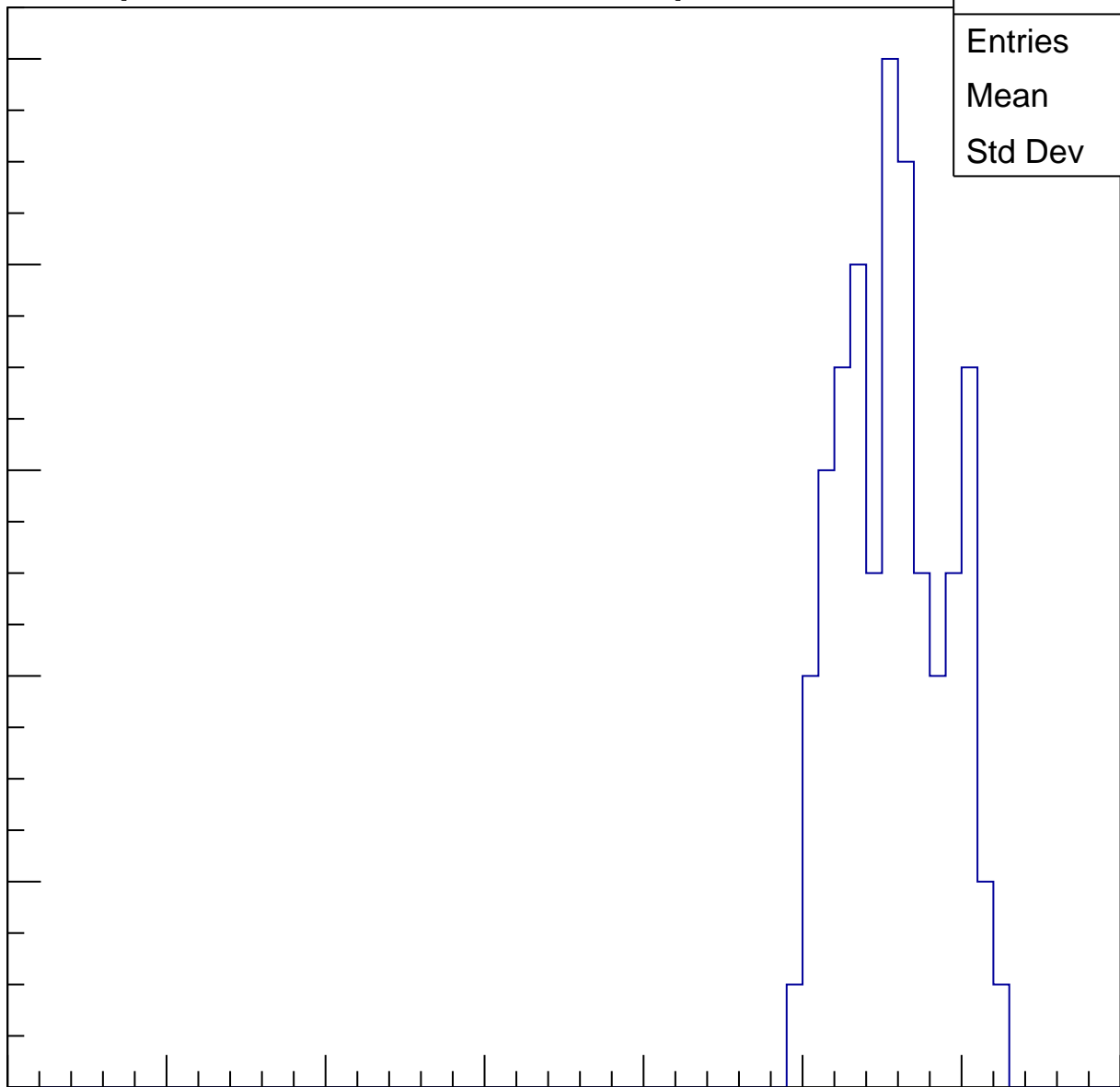
Entries	74
Mean	55.18
Std Dev	3.227

Entry

10  
8  
6  
4  
2  
0

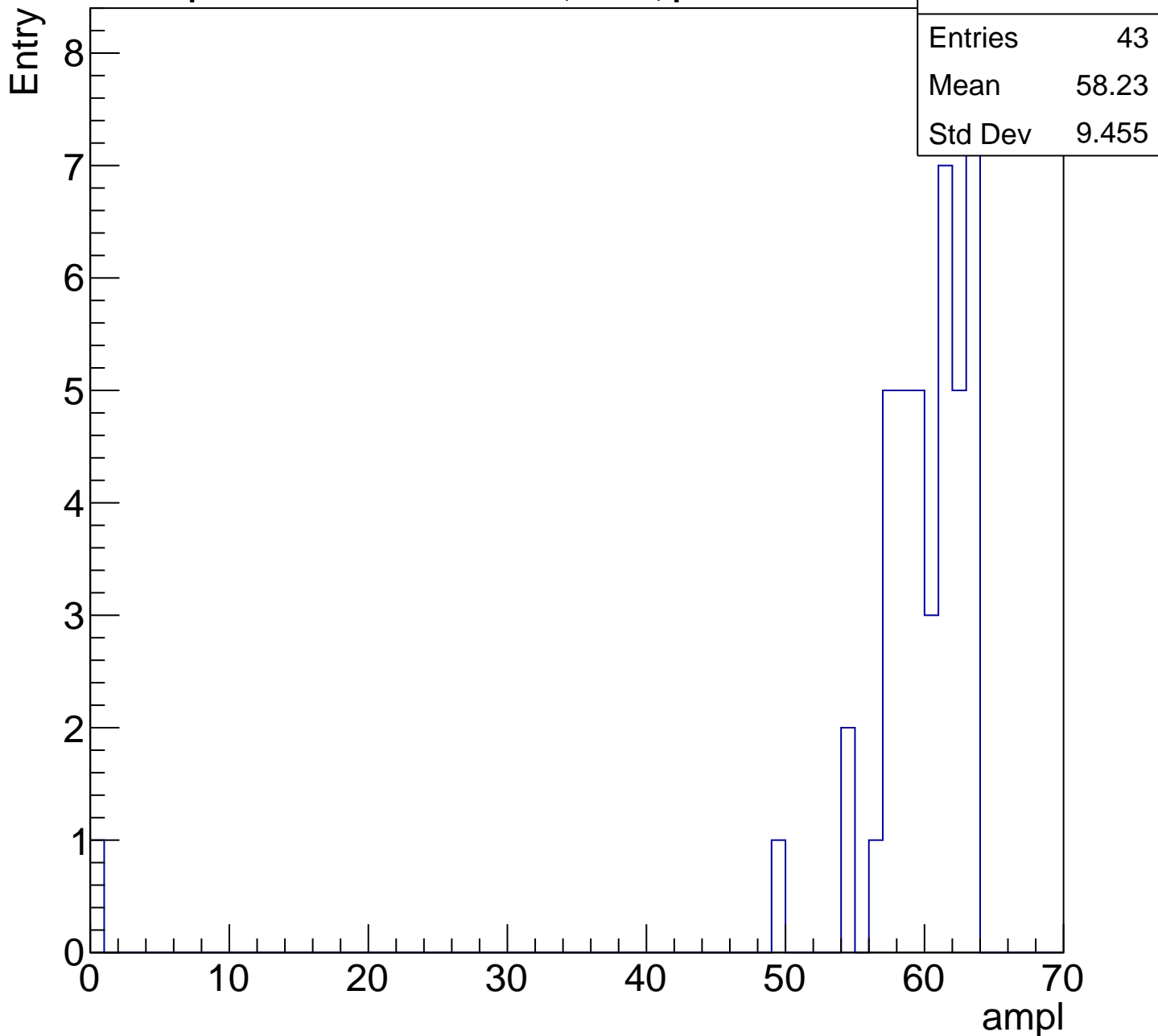
0 10 20 30 40 50 60 70

ampl



# B1L100S, U6-ch40, adc5

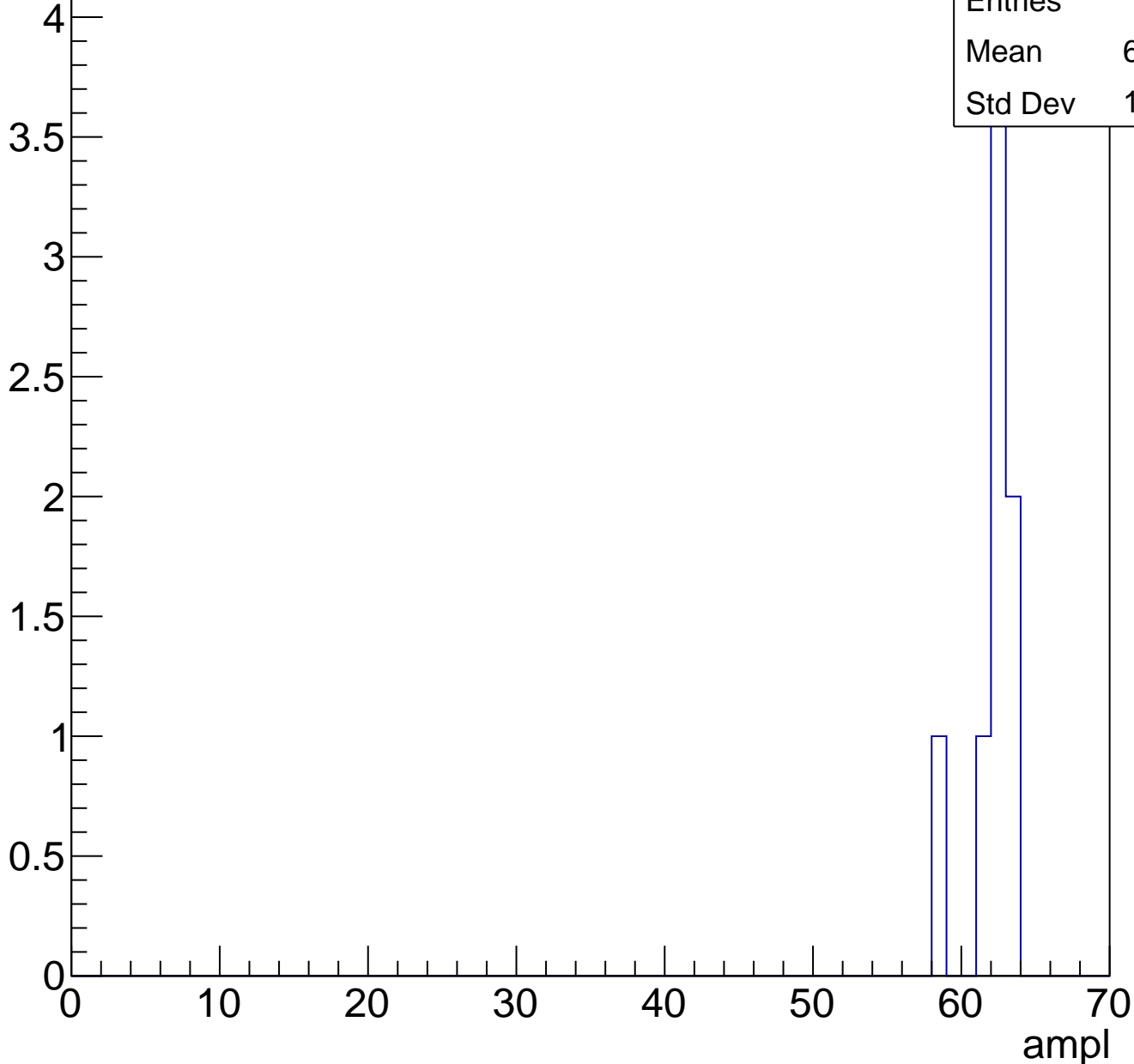
calib\_packv5\_042523\_0143.root, FC#4, port A2



# B1L100S, U6-ch40, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry





# B1L100S, U6-ch40, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L100S, U6-ch41, adc0

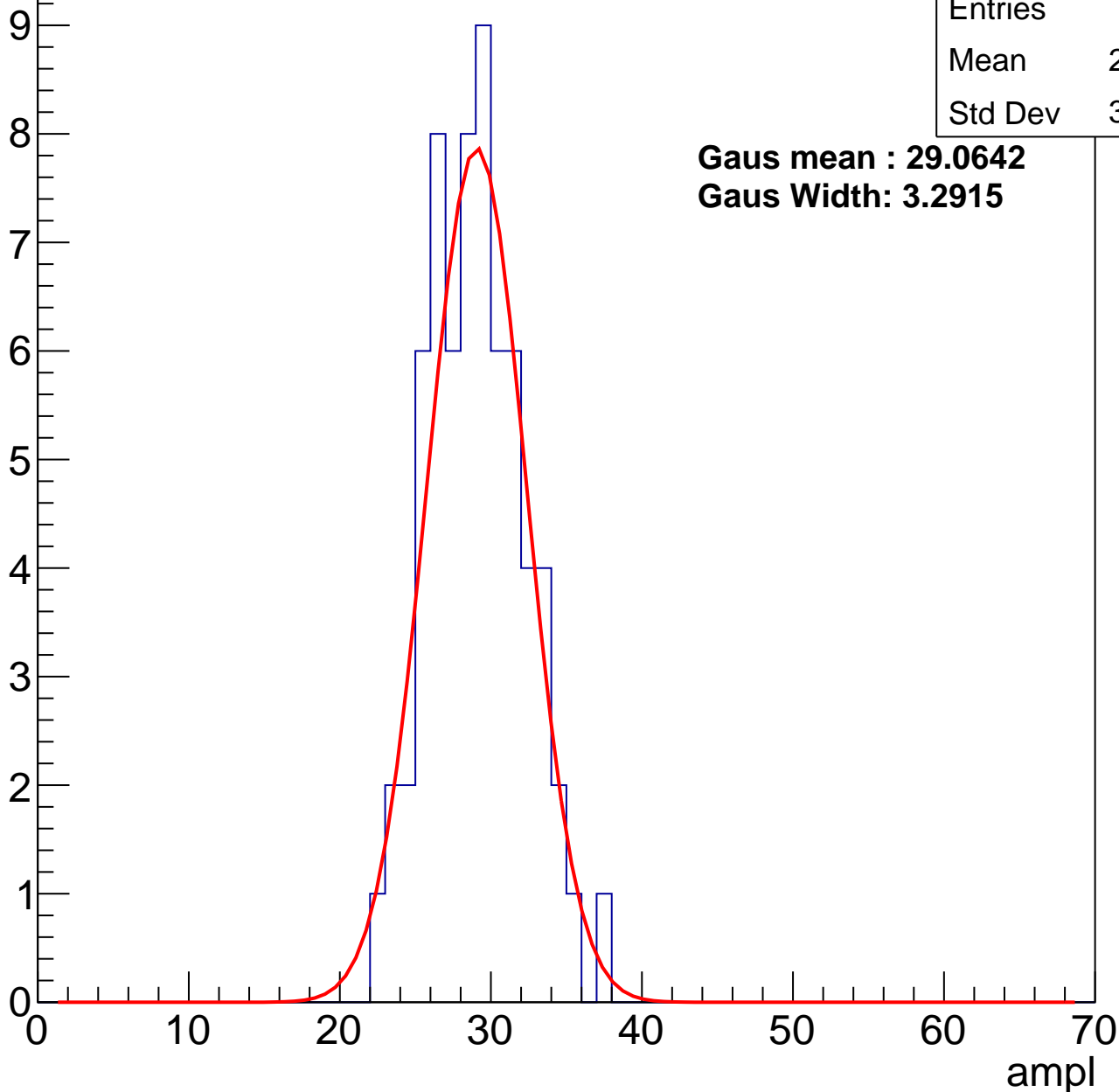
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	66
Mean	28.59
Std Dev	3.114

**Gaus mean : 29.0642**

**Gaus Width: 3.2915**



# B1L100S, U6-ch41, adc1

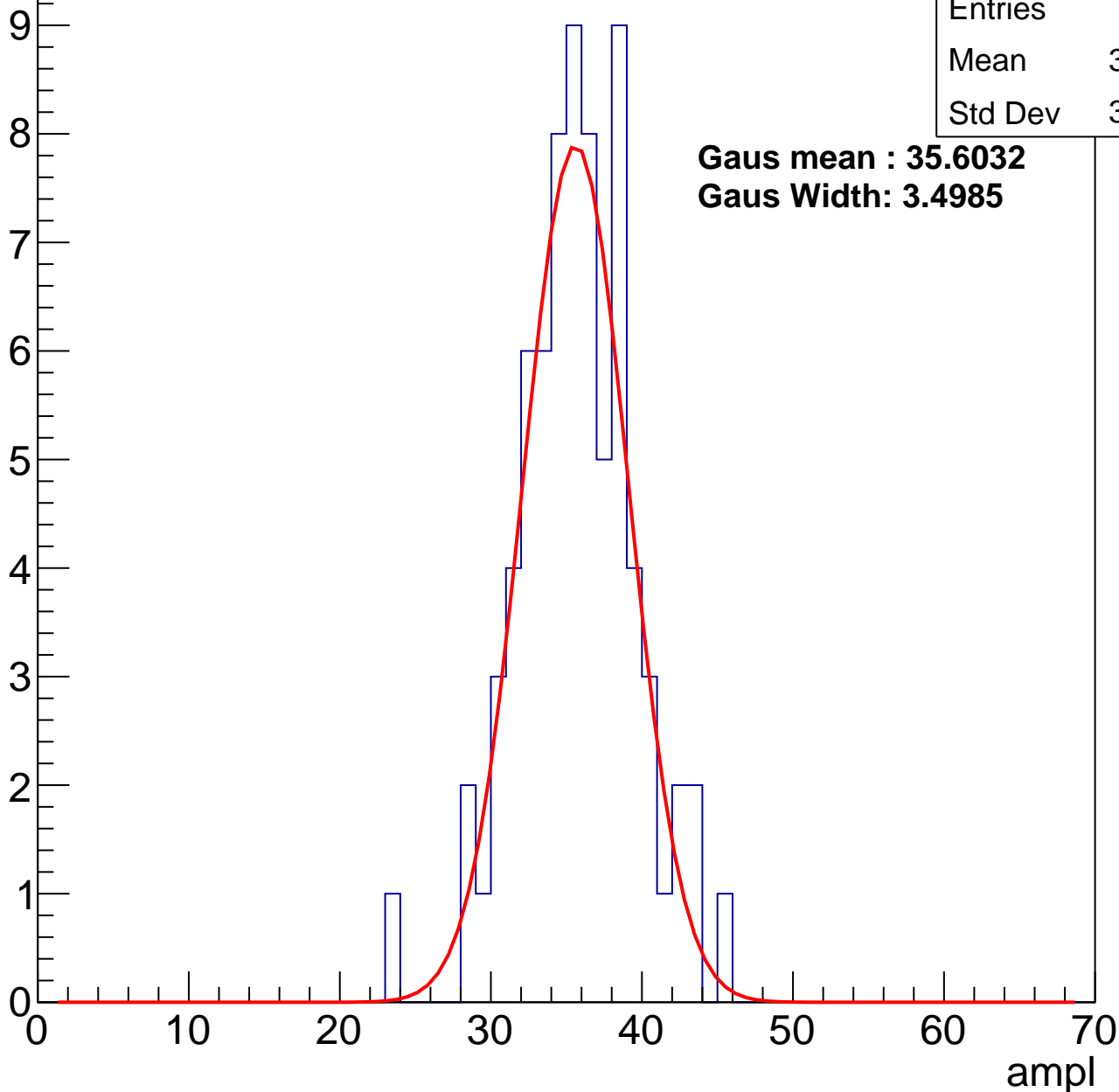
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	75
Mean	35.28
Std Dev	3.842

**Gaus mean : 35.6032**

**Gaus Width: 3.4985**



# B1L100S, U6-ch41, adc2

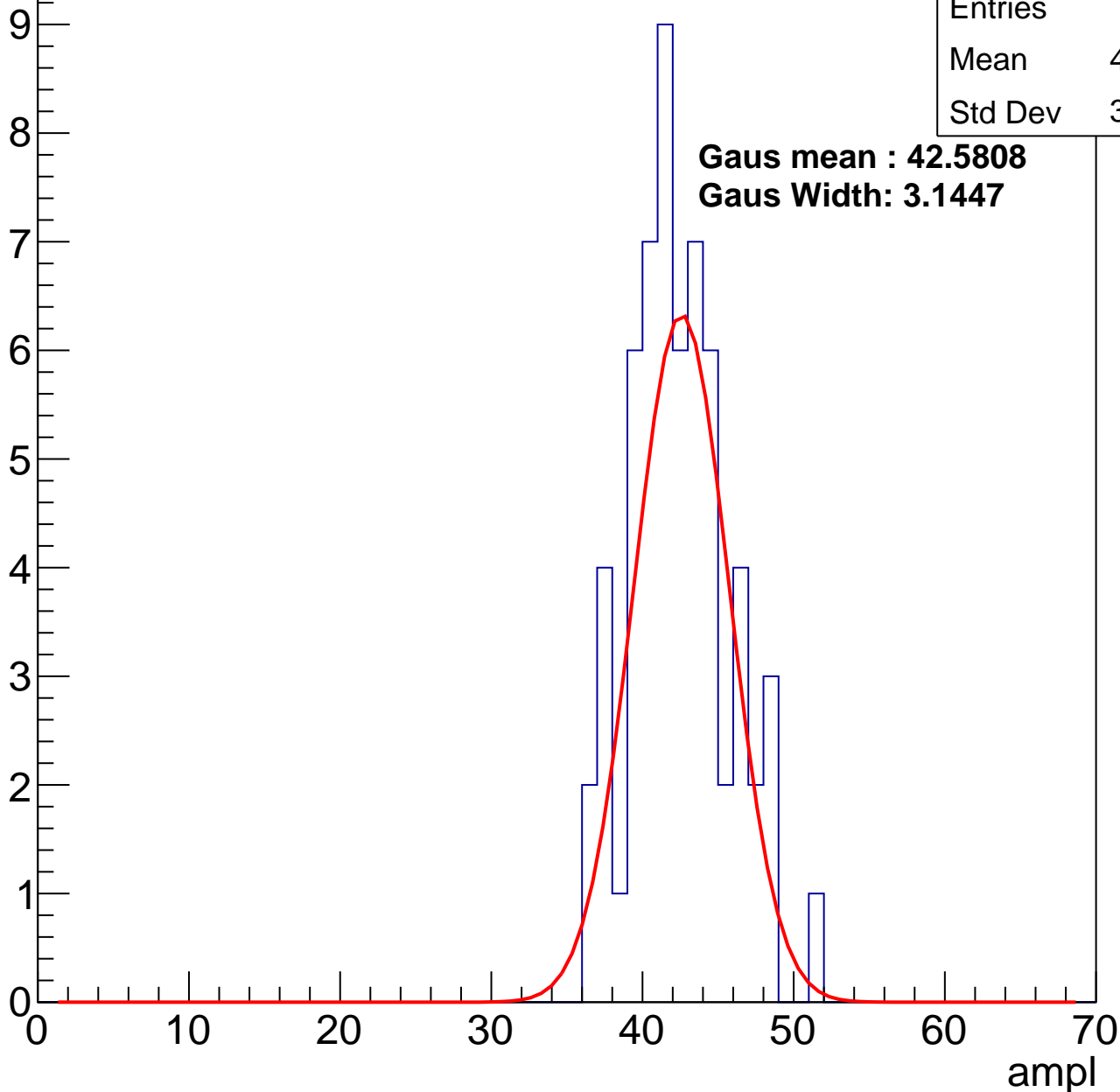
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	60
Mean	42.02
Std Dev	3.243

**Gaus mean : 42.5808**

**Gaus Width: 3.1447**



# B1L100S, U6-ch41, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

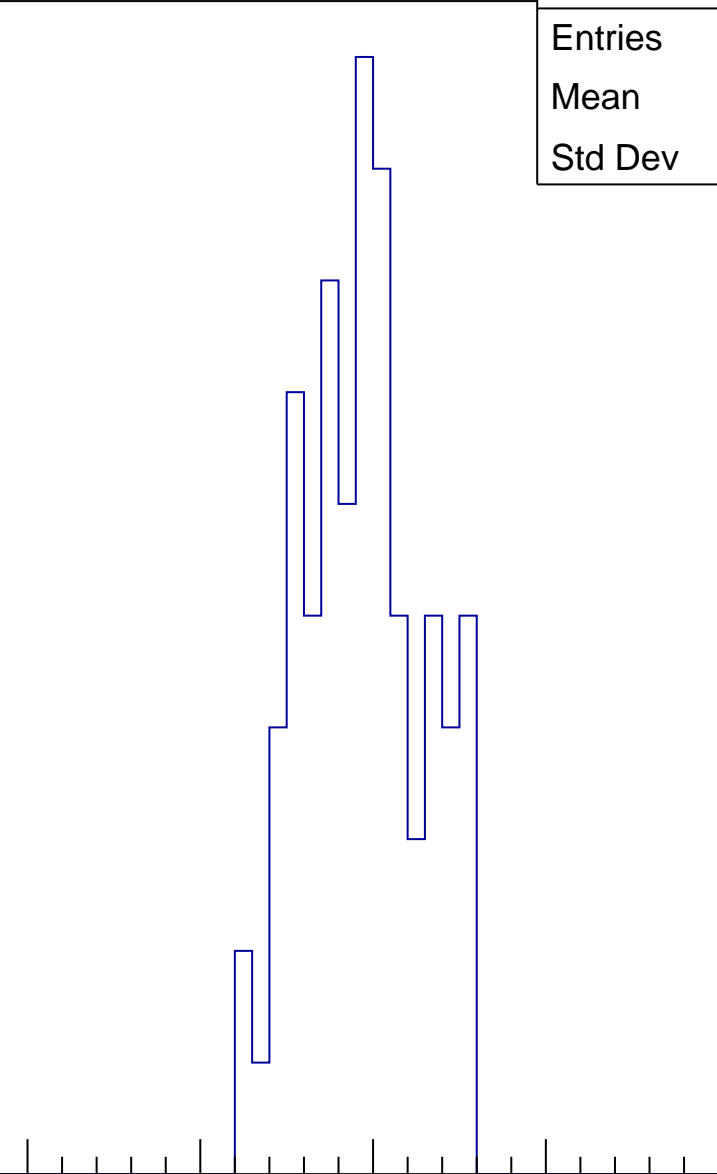
Entries	74
Mean	48.91
Std Dev	3.378

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

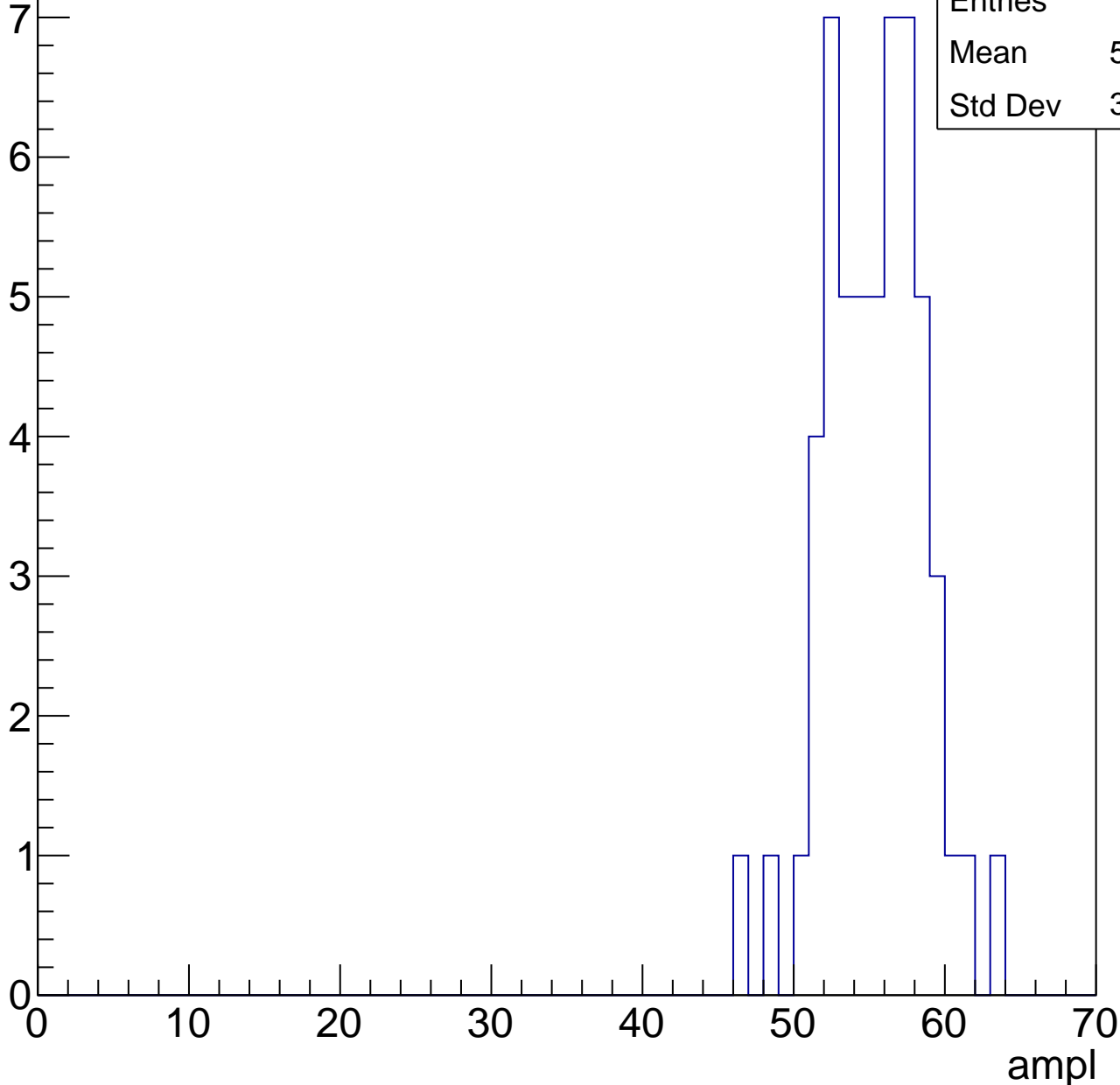


# B1L100S, U6-ch41, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	54
Mean	54.89
Std Dev	3.218



# B1L100S, U6-ch41, adc5

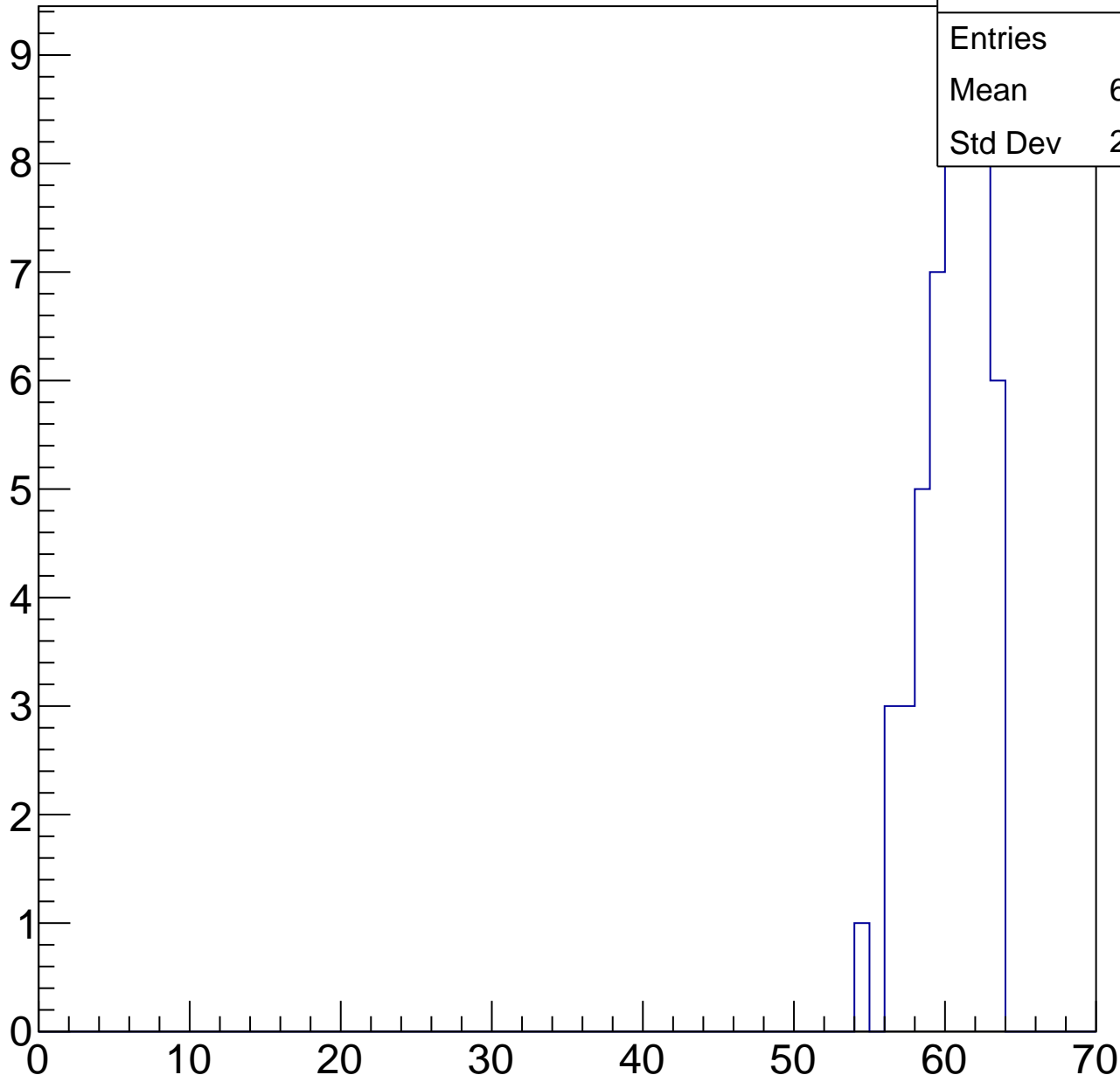
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	52
Mean	60.02
Std Dev	2.135

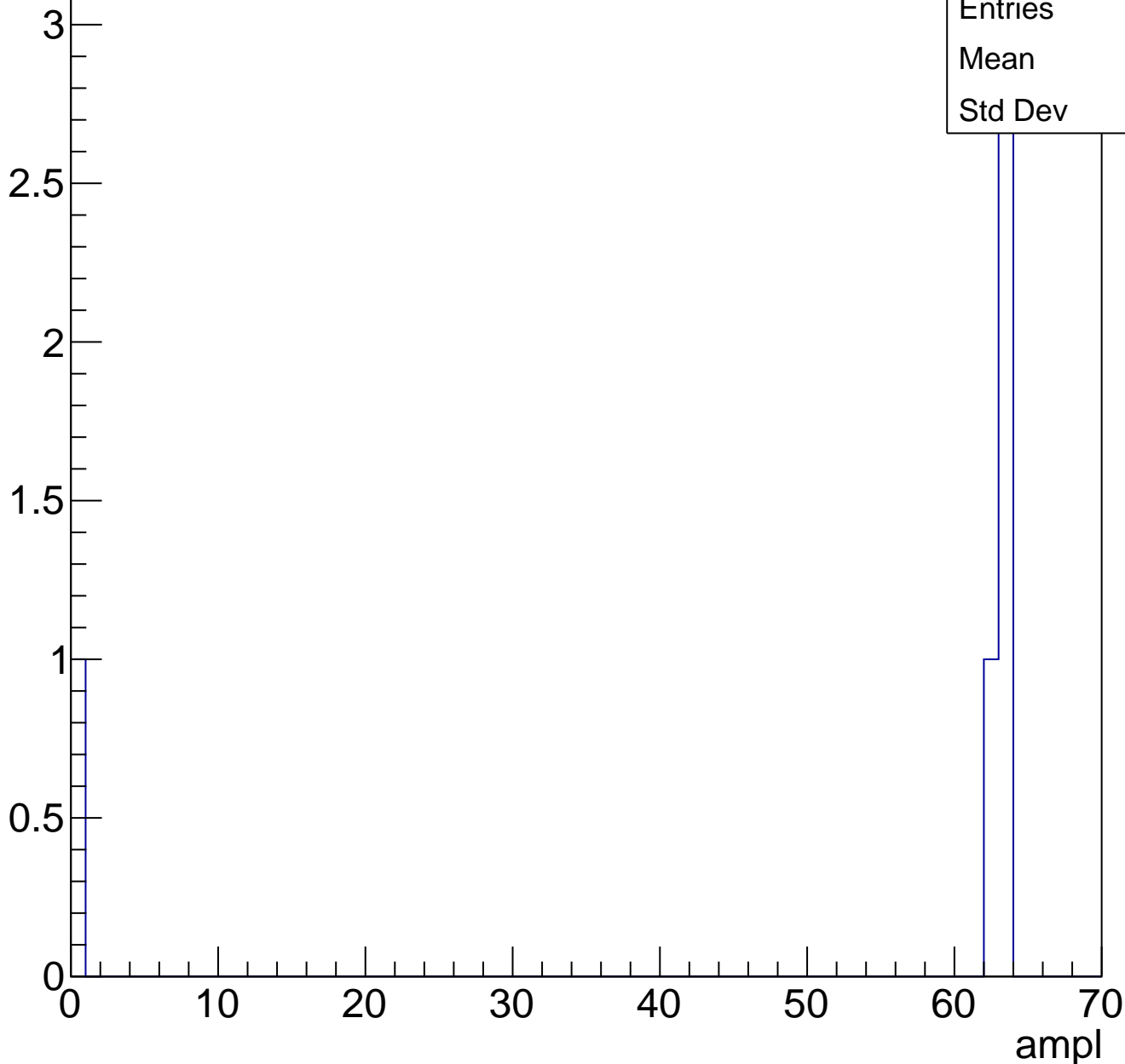
ampl



# B1L100S, U6-ch41, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry





# B1L100S, U6-ch41, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

1  
0.8  
0.6  
0.4  
0.2  
0

0

10

20

30

40

50

60

70

ampl

Entries	1
Mean	21
Std Dev	0

# B1L100S, U6-ch42, adc0

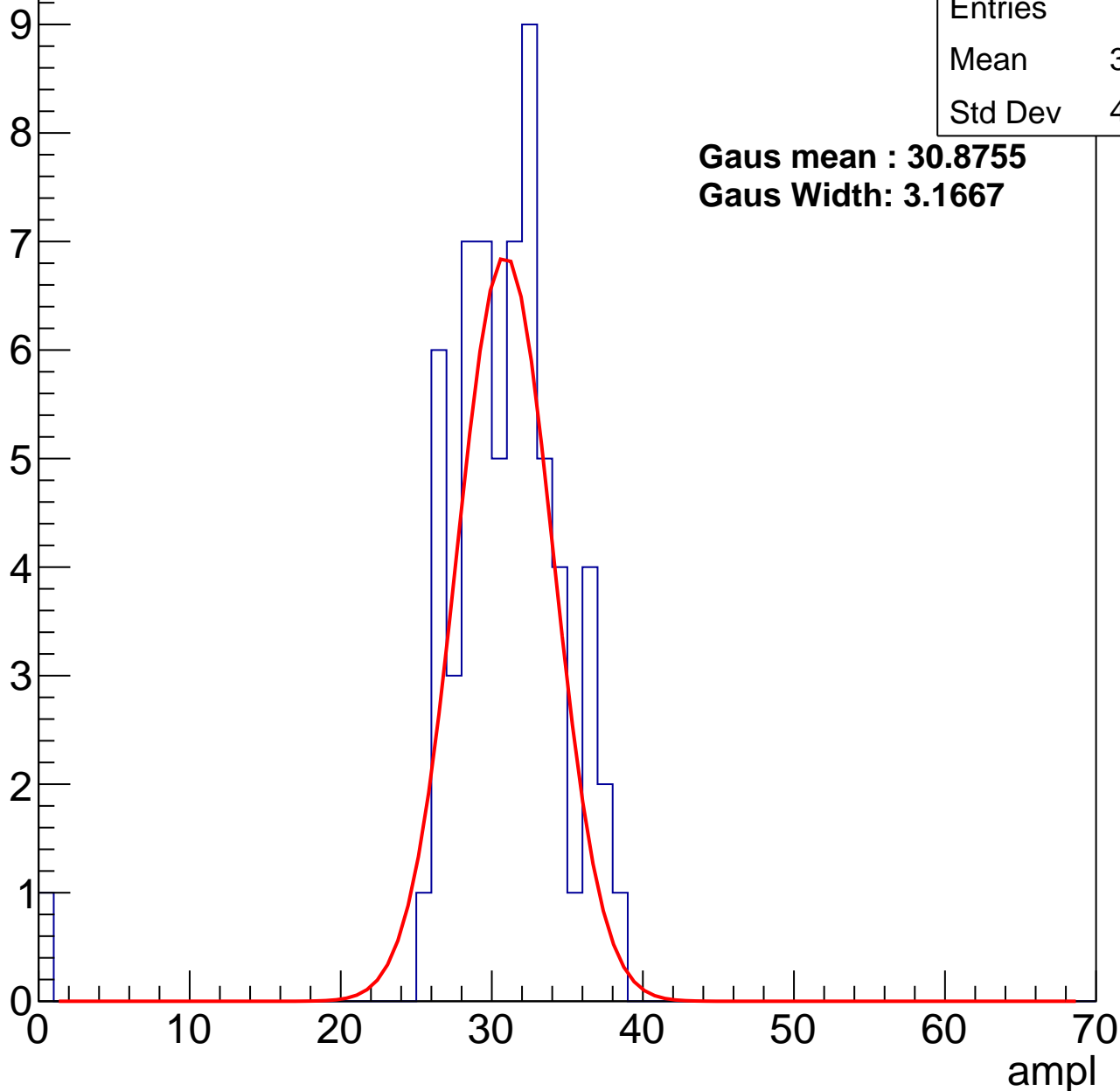
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	63
Mean	30.29
Std Dev	4.978

**Gaus mean : 30.8755**

**Gaus Width: 3.1667**



# B1L100S, U6-ch42, adc1

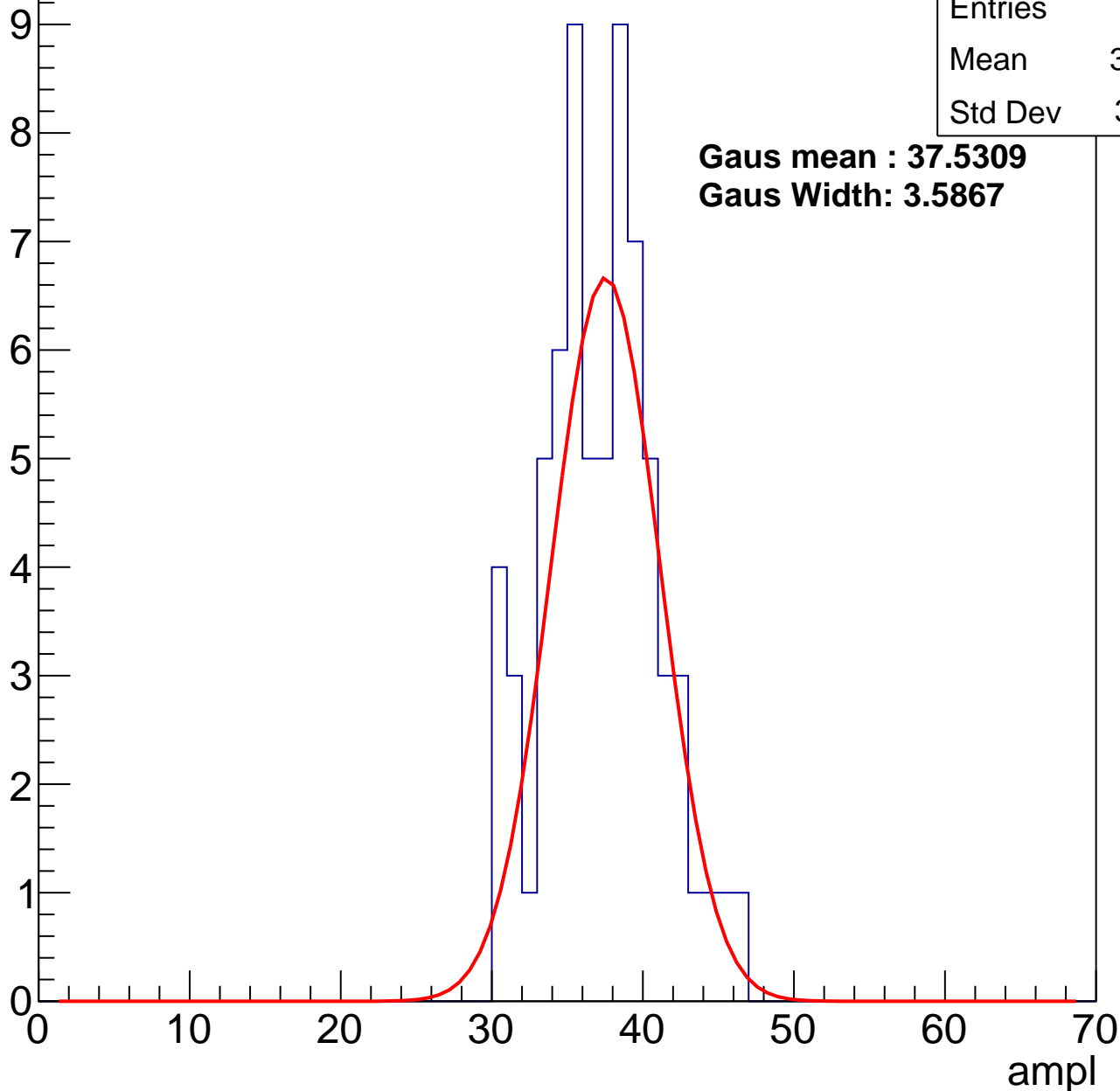
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	69
Mean	36.75
Std Dev	3.681

**Gaus mean : 37.5309**

**Gaus Width: 3.5867**



# B1L100S, U6-ch42, adc2

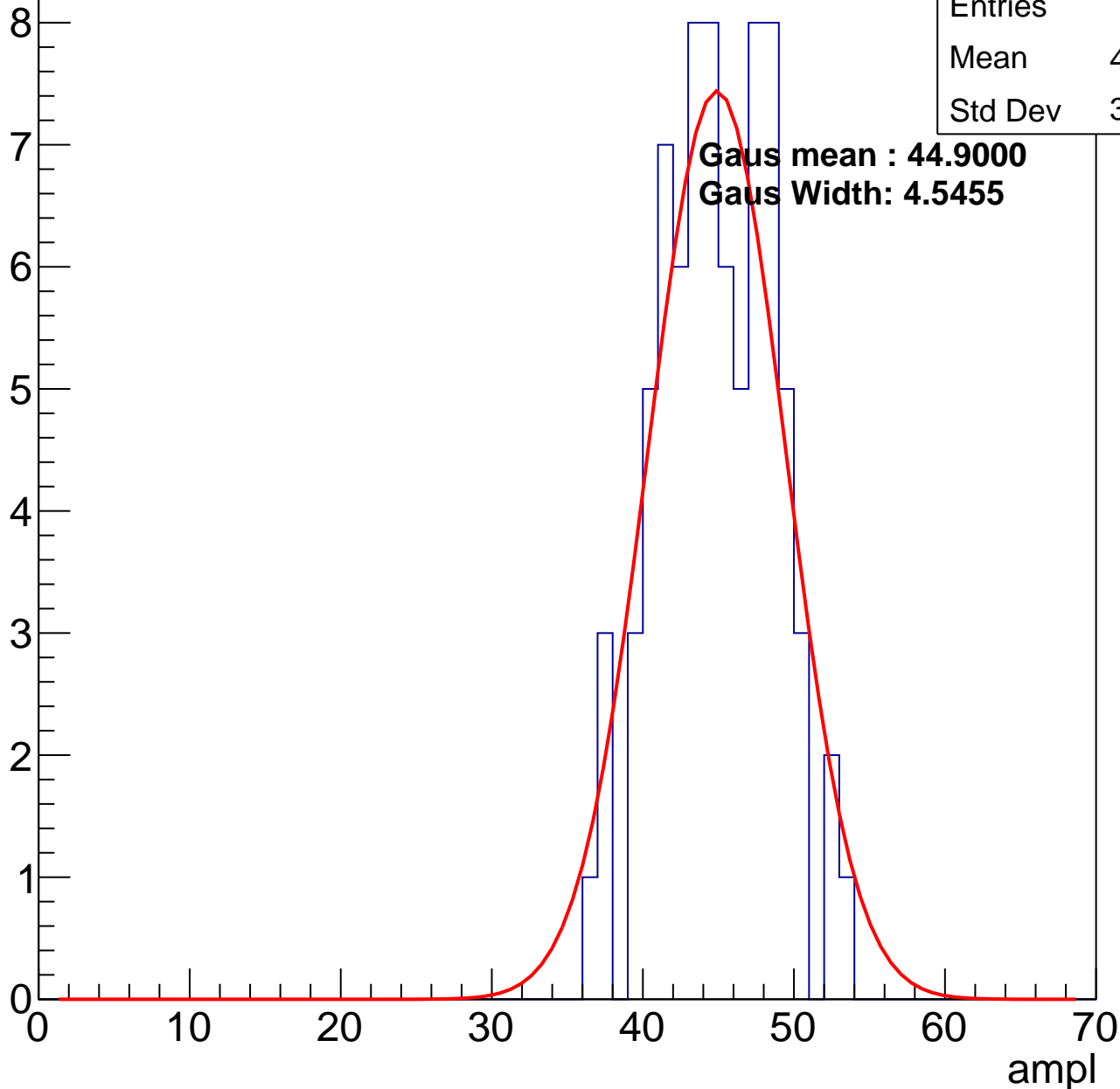
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	79
Mean	44.44
Std Dev	3.754

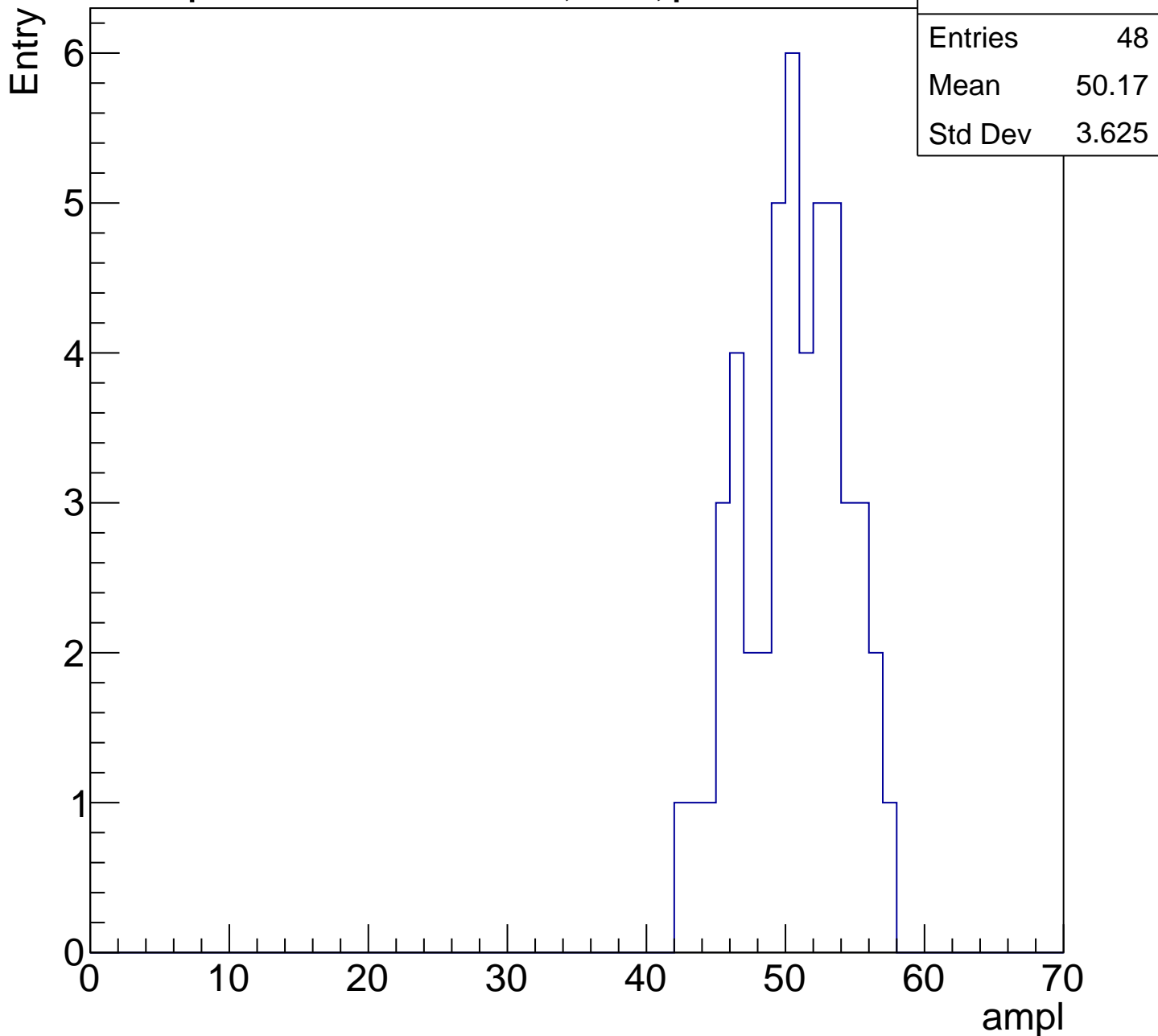
**Gaus mean : 44.9000**

**Gaus Width: 4.5455**



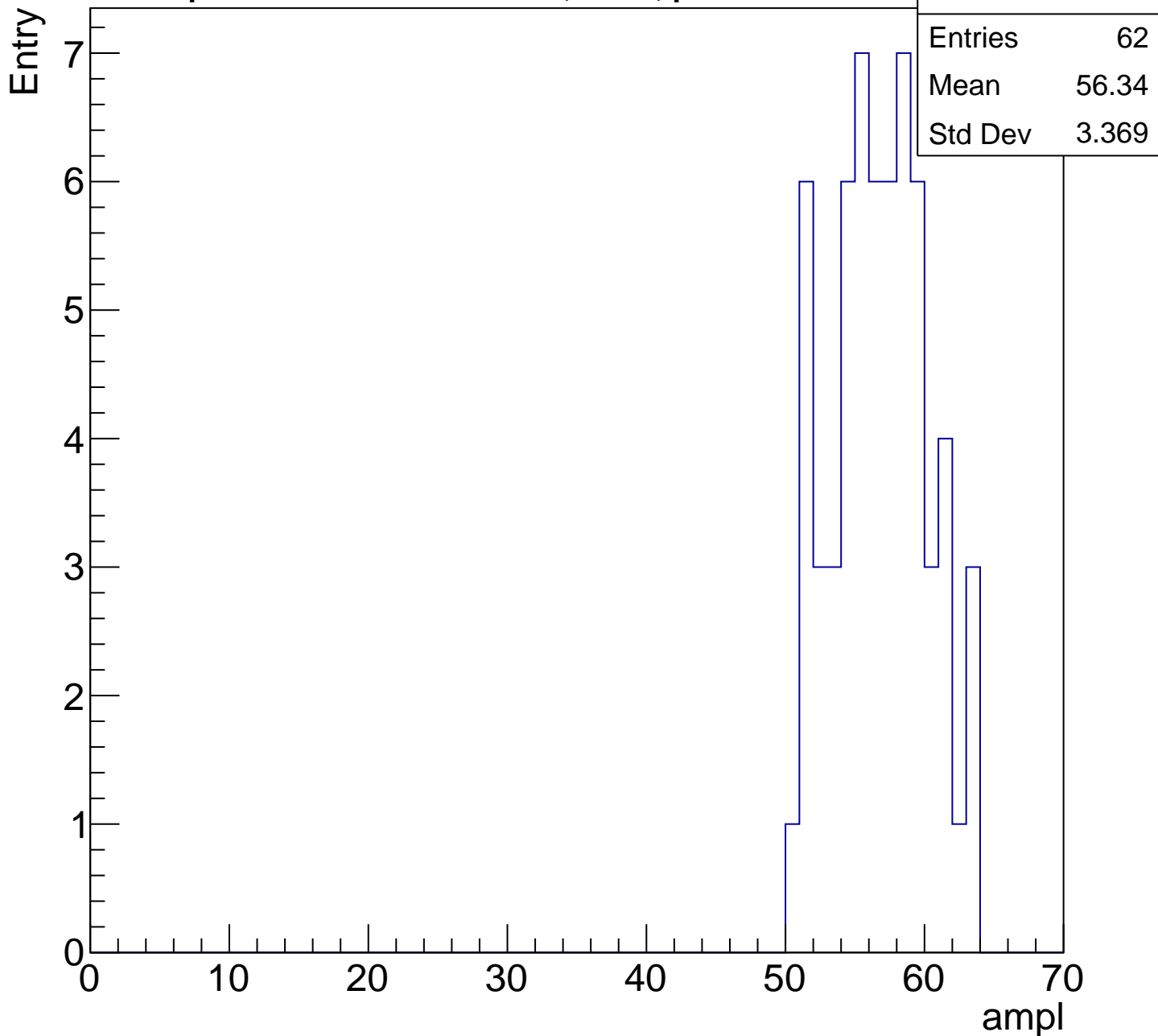
# B1L100S, U6-ch42, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2



# B1L100S, U6-ch42, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

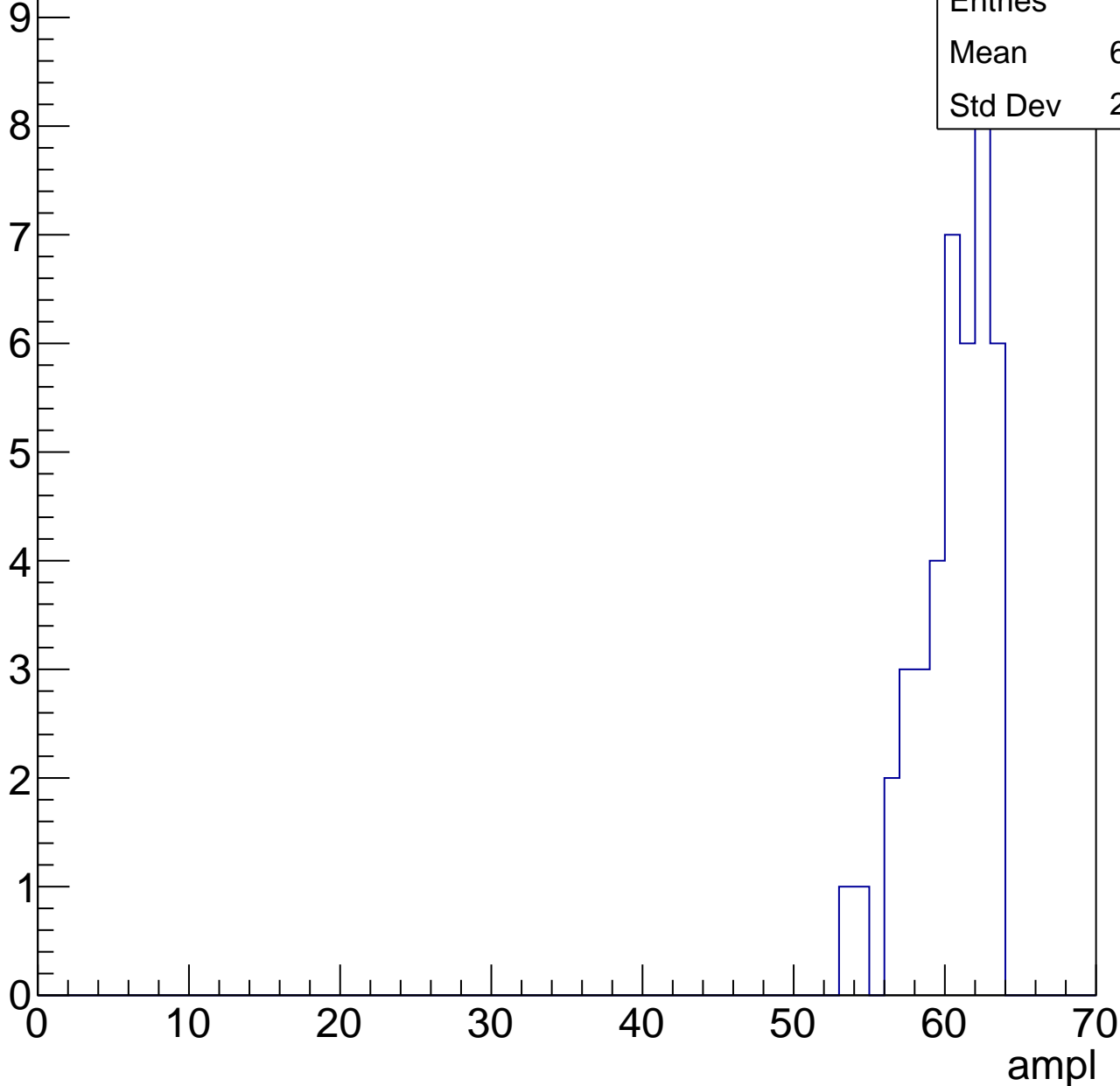


# B1L100S, U6-ch42, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

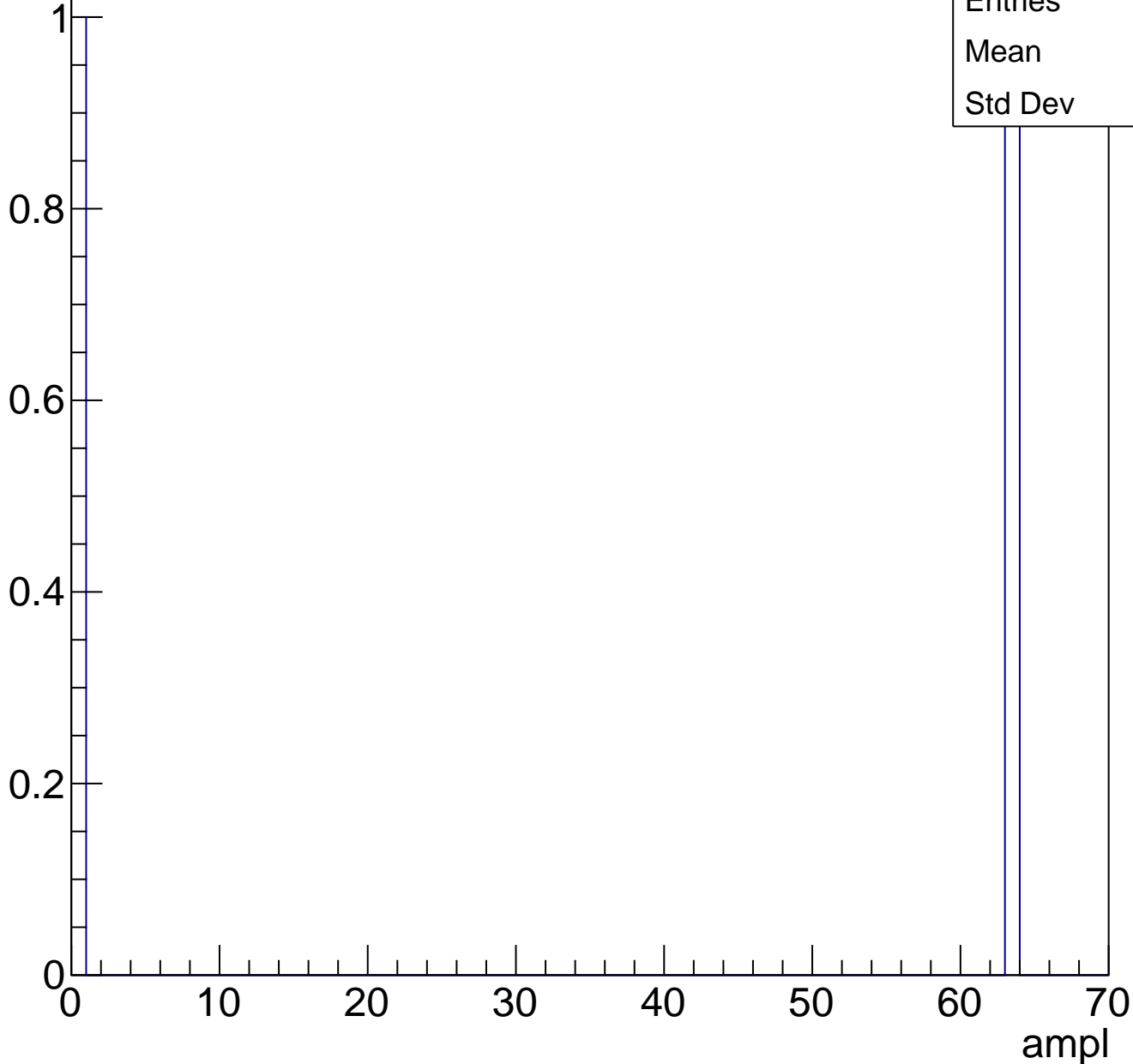
Entries	42
Mean	60.05
Std Dev	2.468



# B1L100S, U6-ch42, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry





# B1L100S, U6-ch42, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



# B1L100S, U6-ch43, adc0

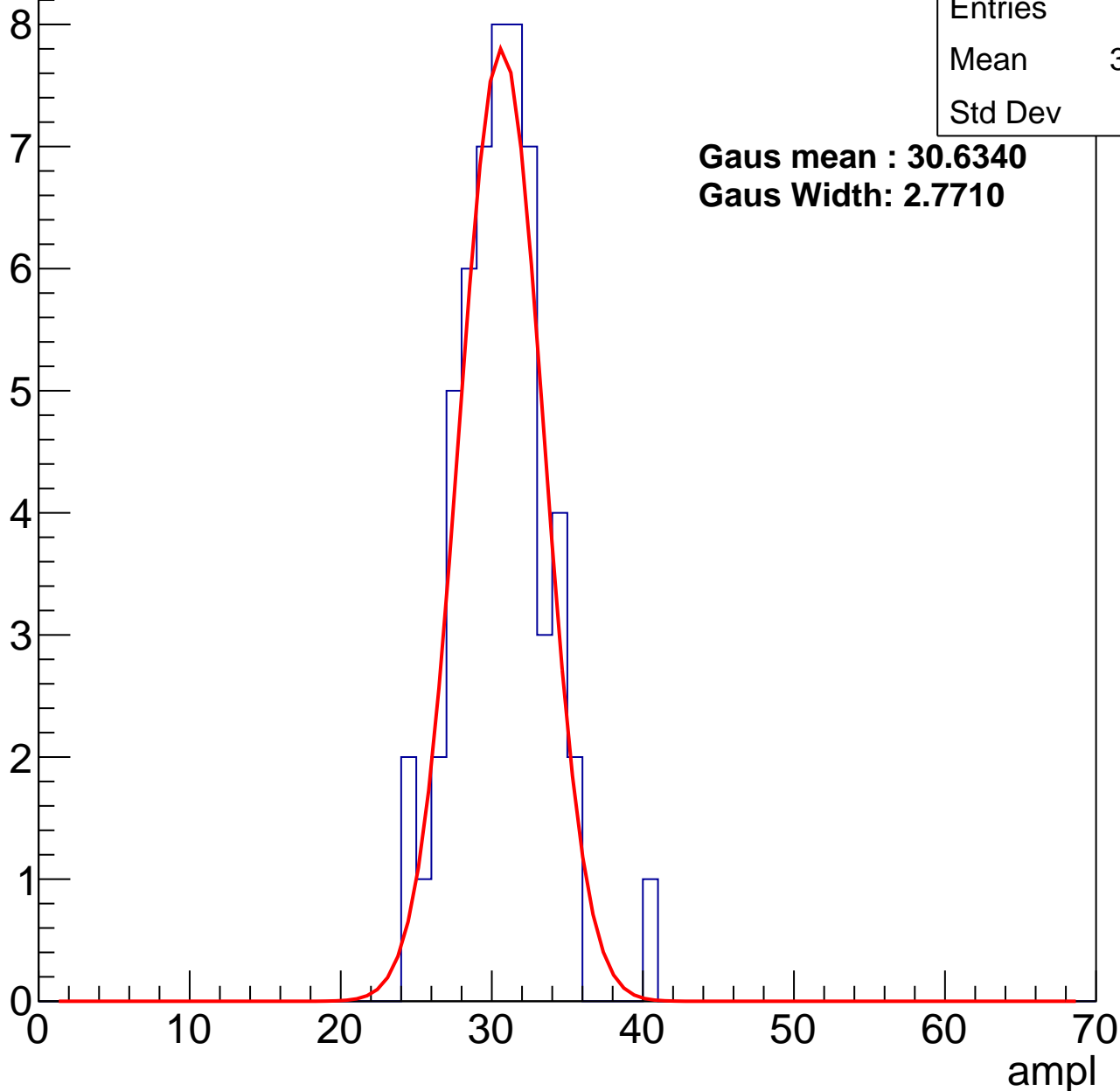
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	56
Mean	30.14
Std Dev	2.93

**Gaus mean : 30.6340**

**Gaus Width: 2.7710**



# B1L100S, U6-ch43, adc1

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	75
Mean	36.73
Std Dev	3.66

**Gaus mean : 36.8031**

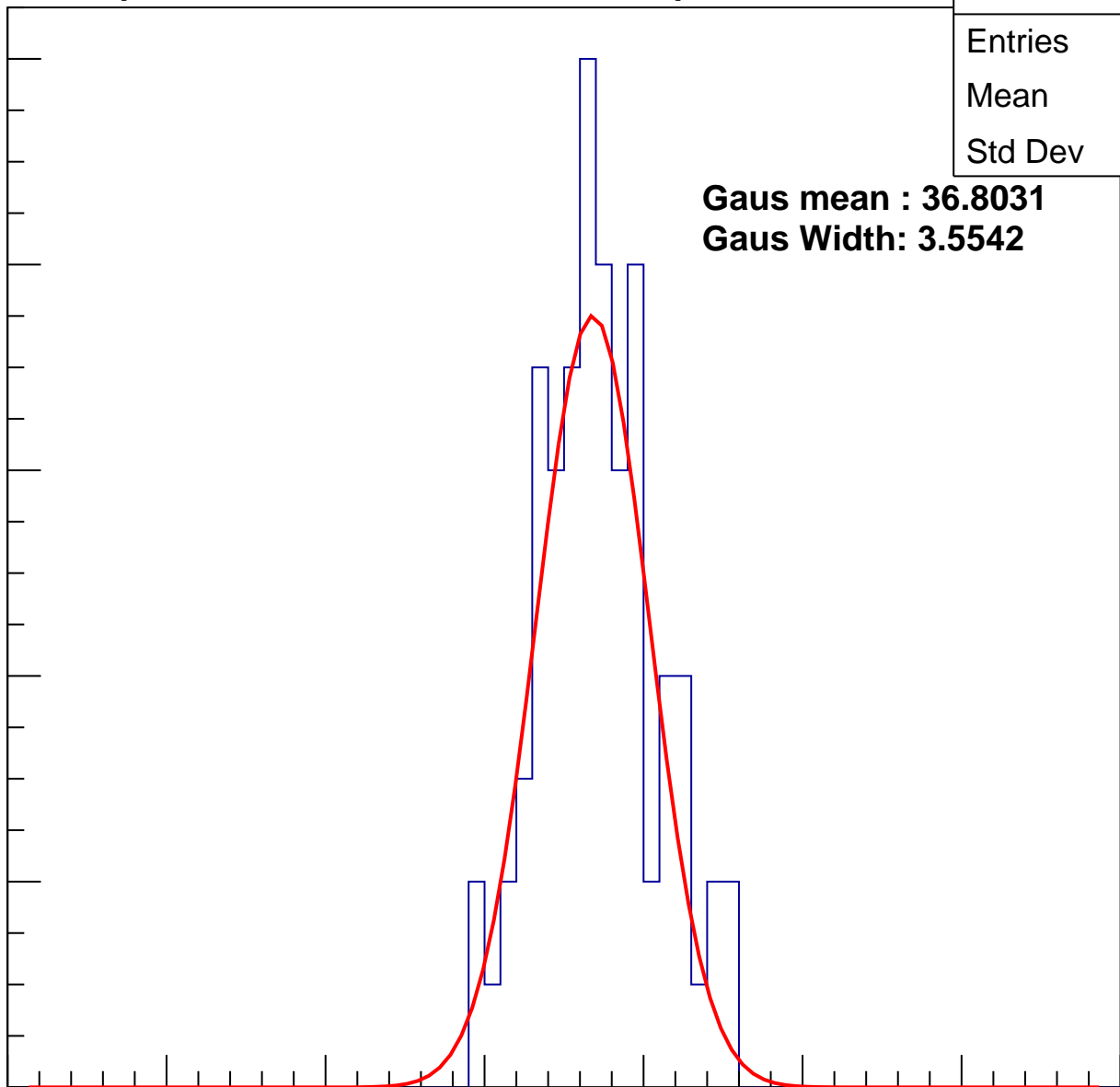
**Gaus Width: 3.5542**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B1L100S, U6-ch43, adc2

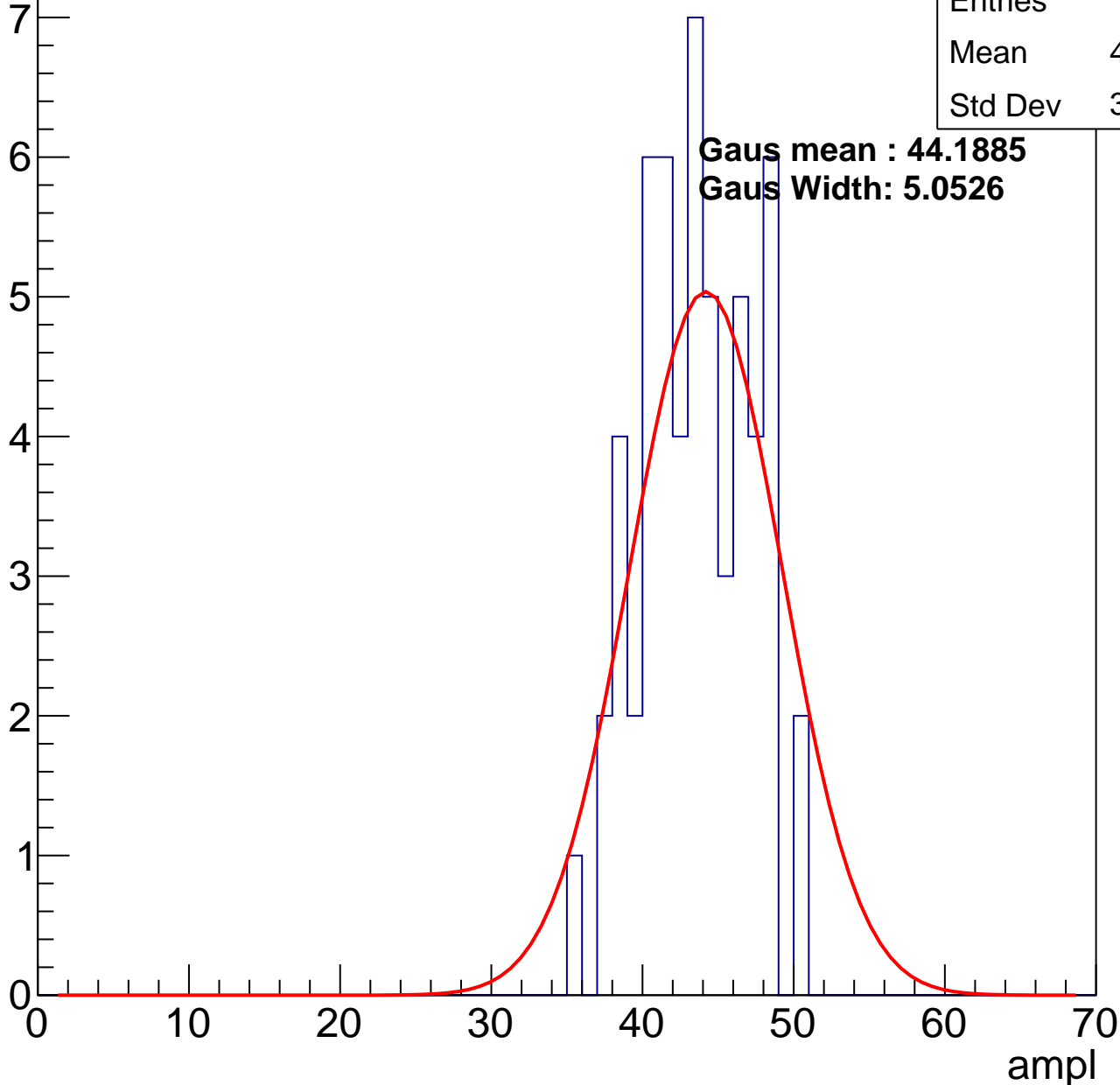
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	57
Mean	43.07
Std Dev	3.563

**Gaus mean : 44.1885**

**Gaus Width: 5.0526**

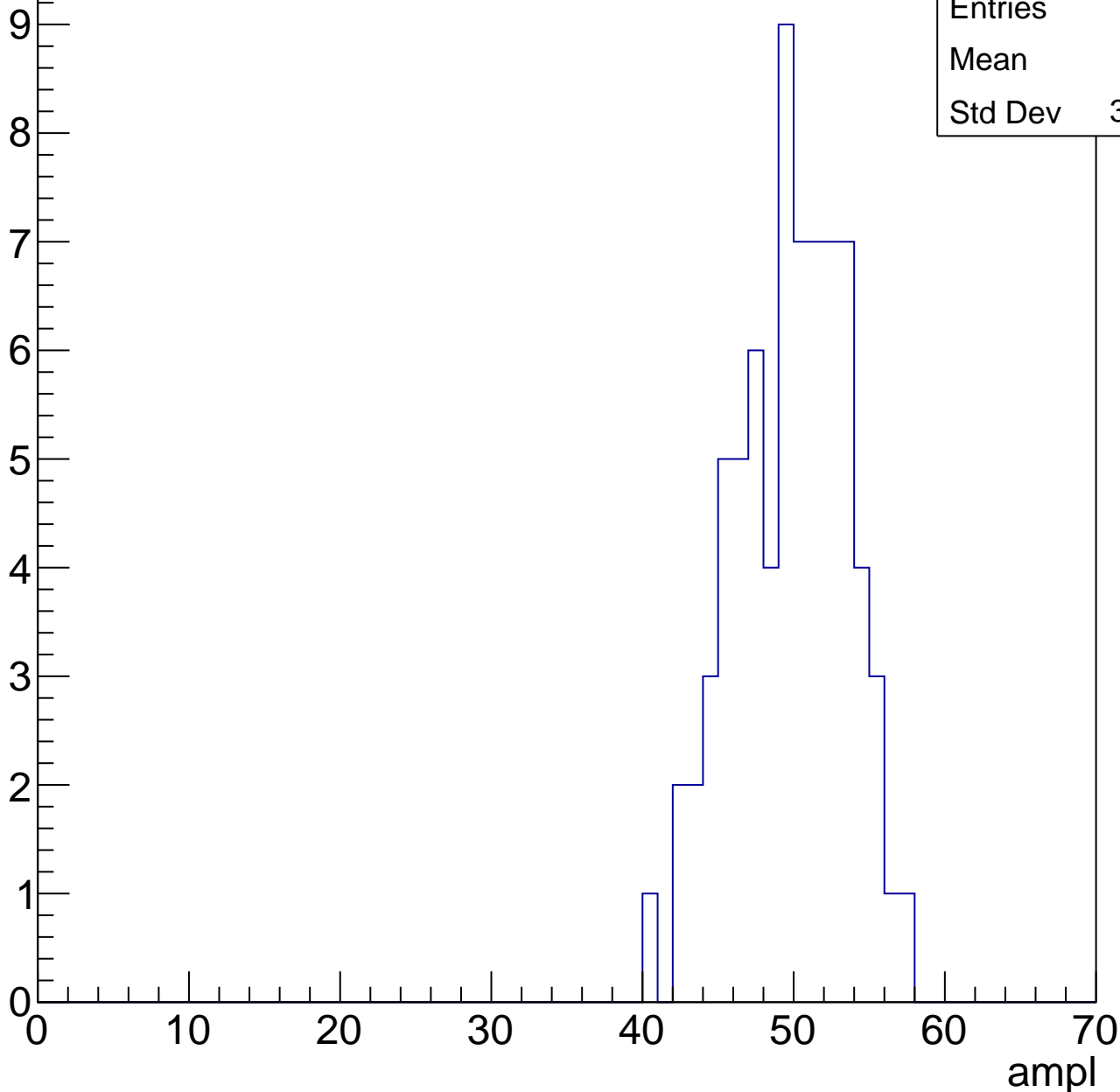


# B1L100S, U6-ch43, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

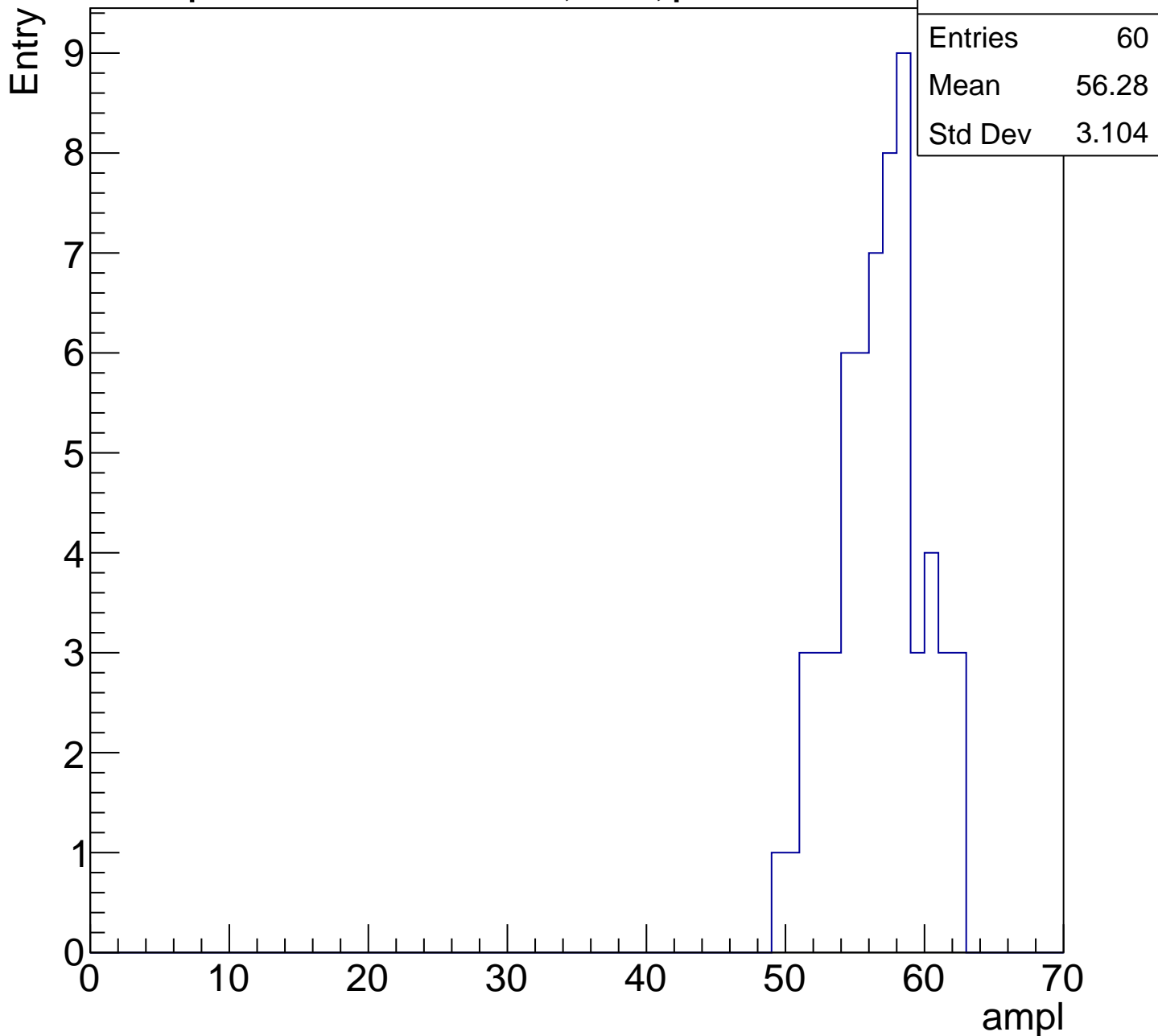
Entry

Entries	74
Mean	49.3
Std Dev	3.682



# B1L100S, U6-ch43, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2



# B1L100S, U6-ch43, adc5

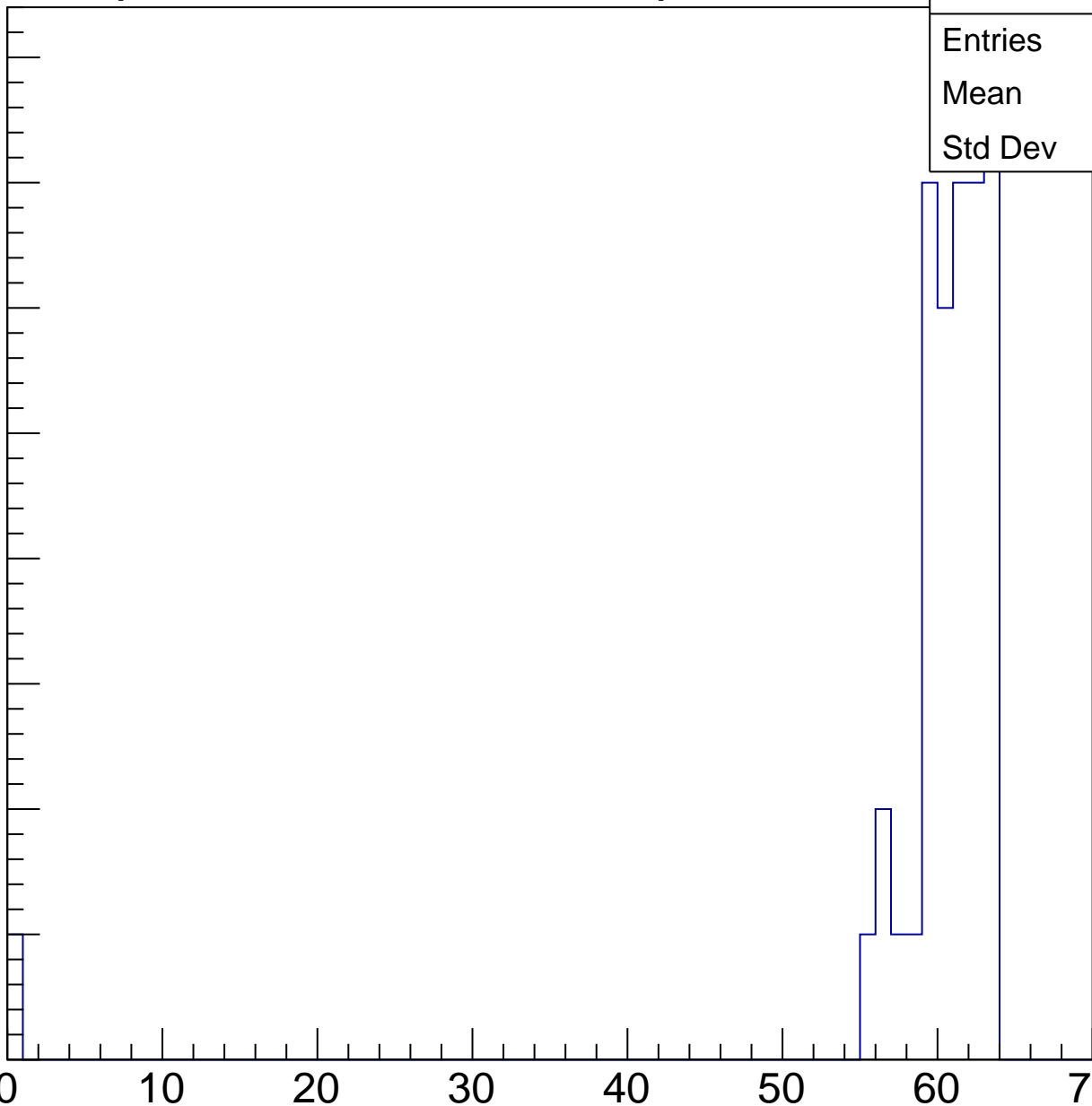
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	41
Mean	59.02
Std Dev	9.557

ampl



# B1L100S, U6-ch43, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	2
Mean	63
Std Dev	0

0 10 20 30 40 50 60 70

ampl



# B1L100S, U6-ch43, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



# B1L100S, U6-ch44, adc0

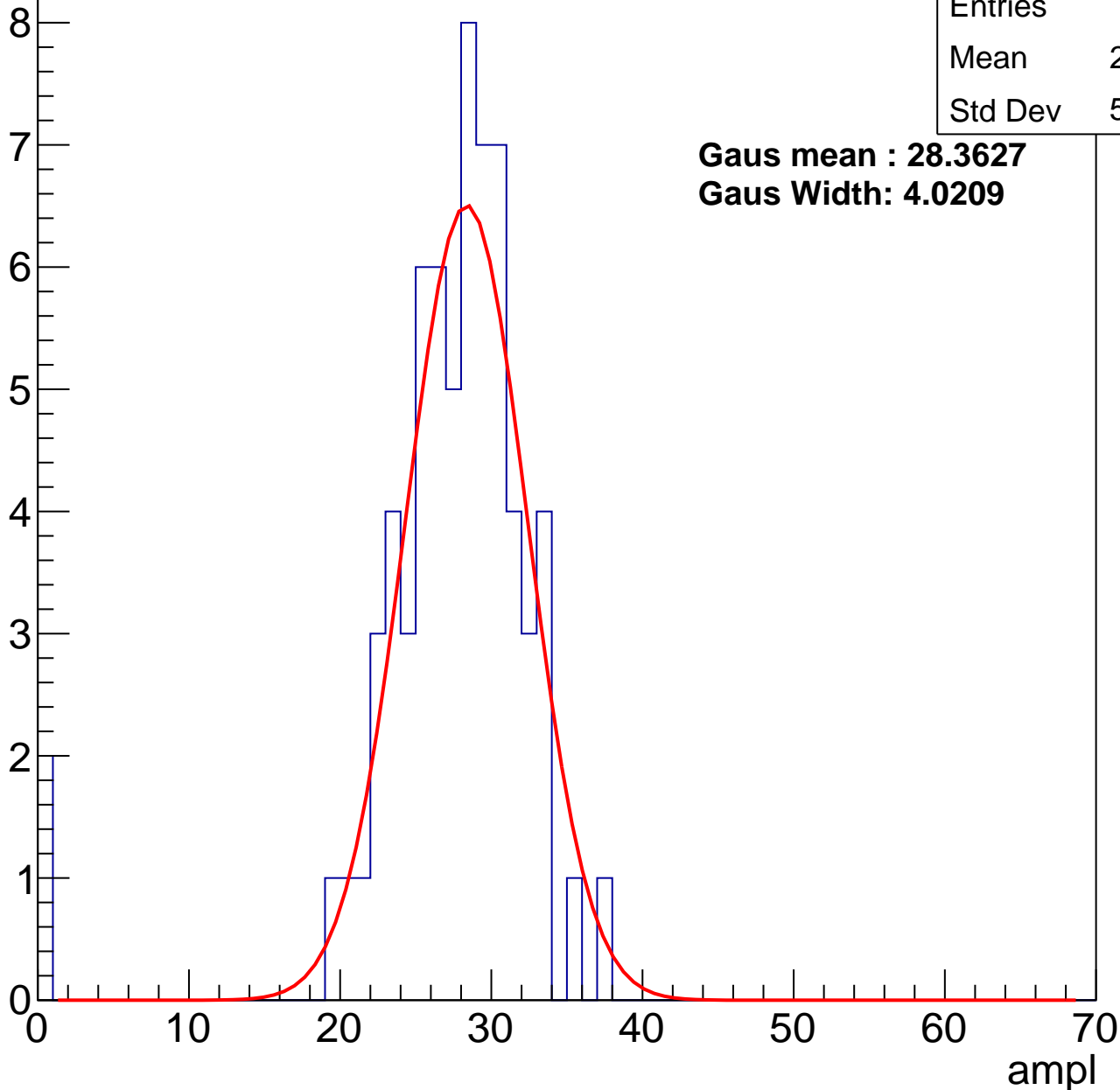
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	67
Mean	26.75
Std Dev	5.916

**Gaus mean : 28.3627**

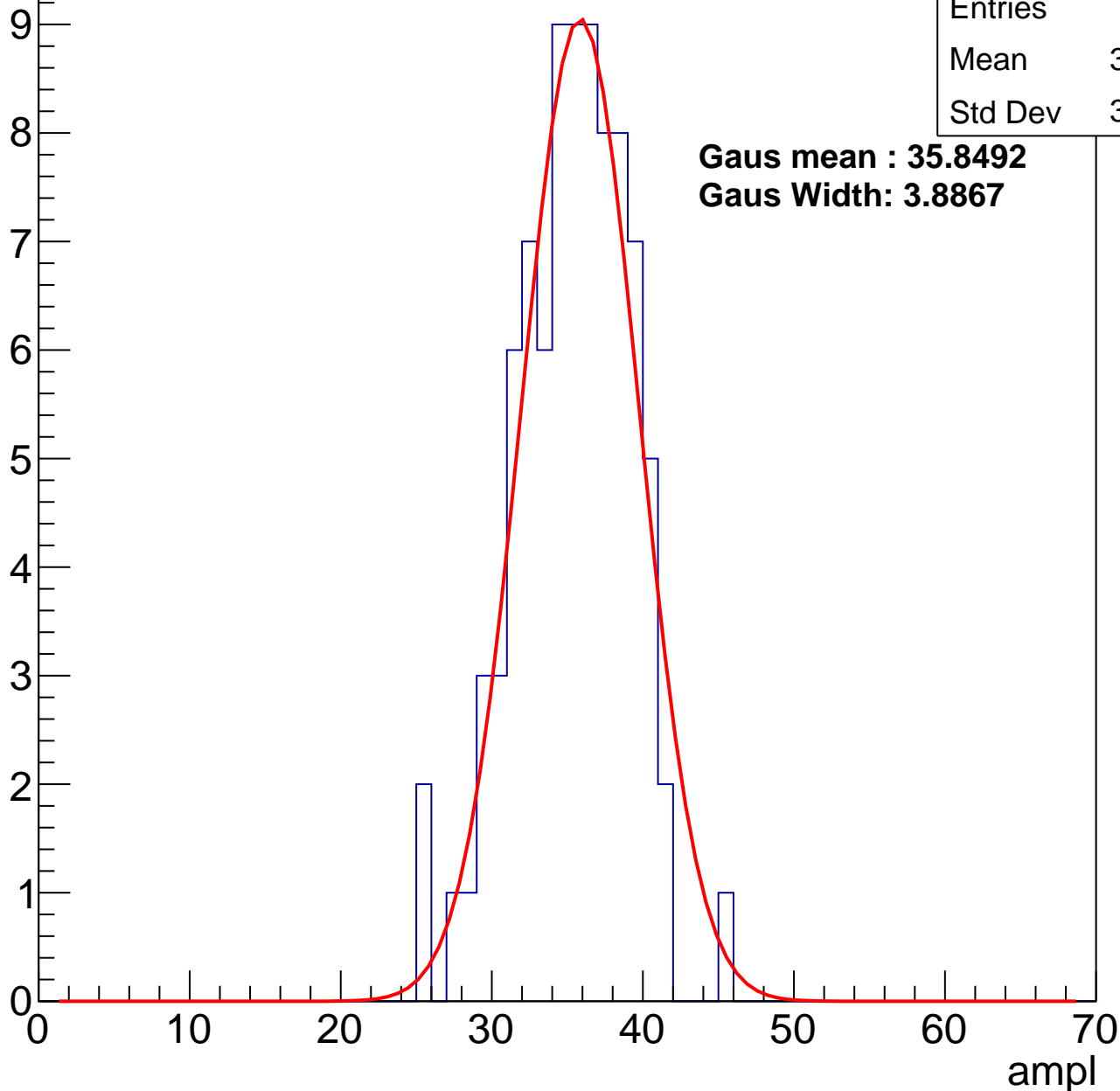
**Gaus Width: 4.0209**



# B1L100S, U6-ch44, adc1

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



# B1L100S, U6-ch44, adc2

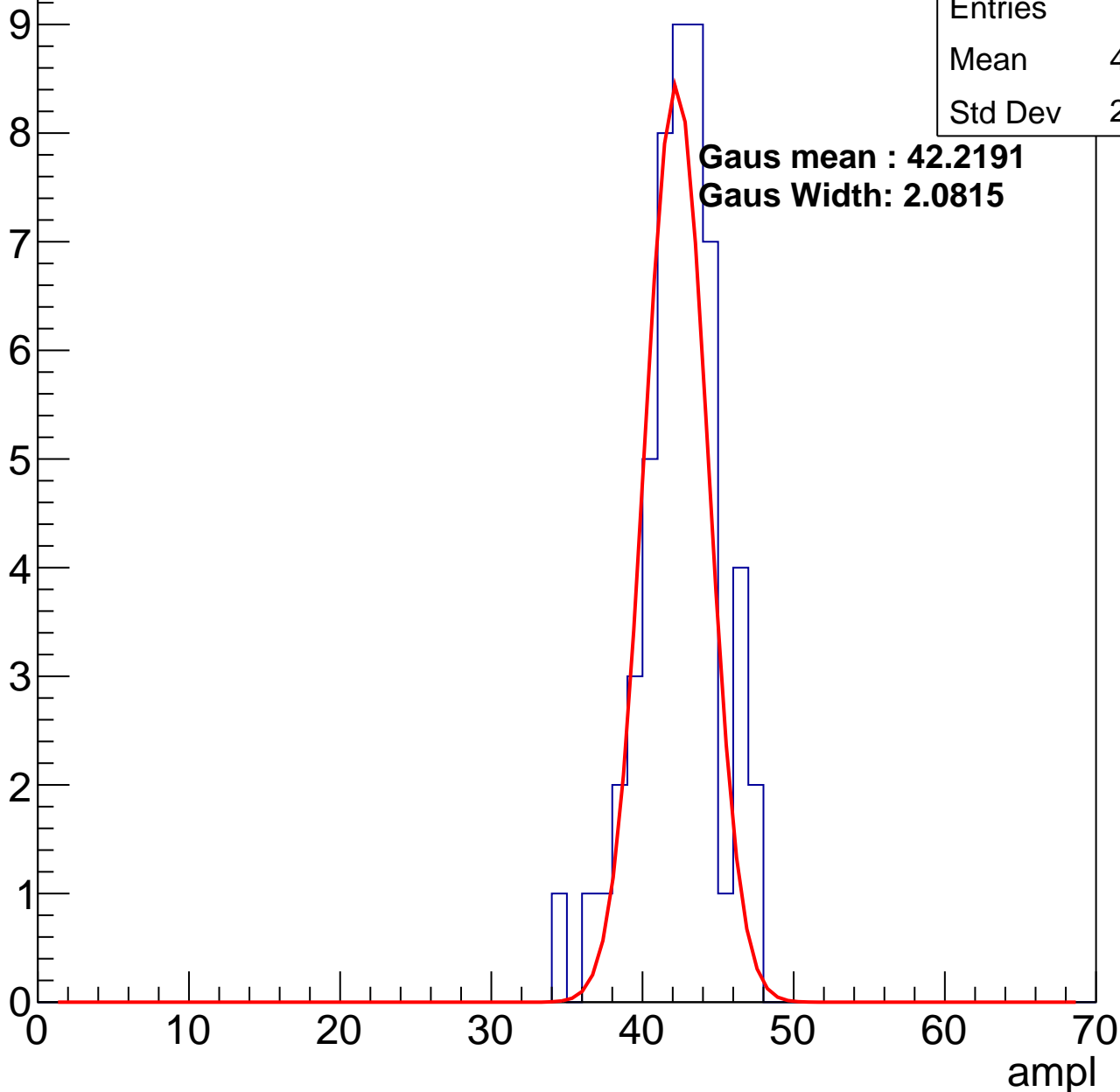
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	53
Mean	41.96
Std Dev	2.649

**Gaus mean : 42.2191**

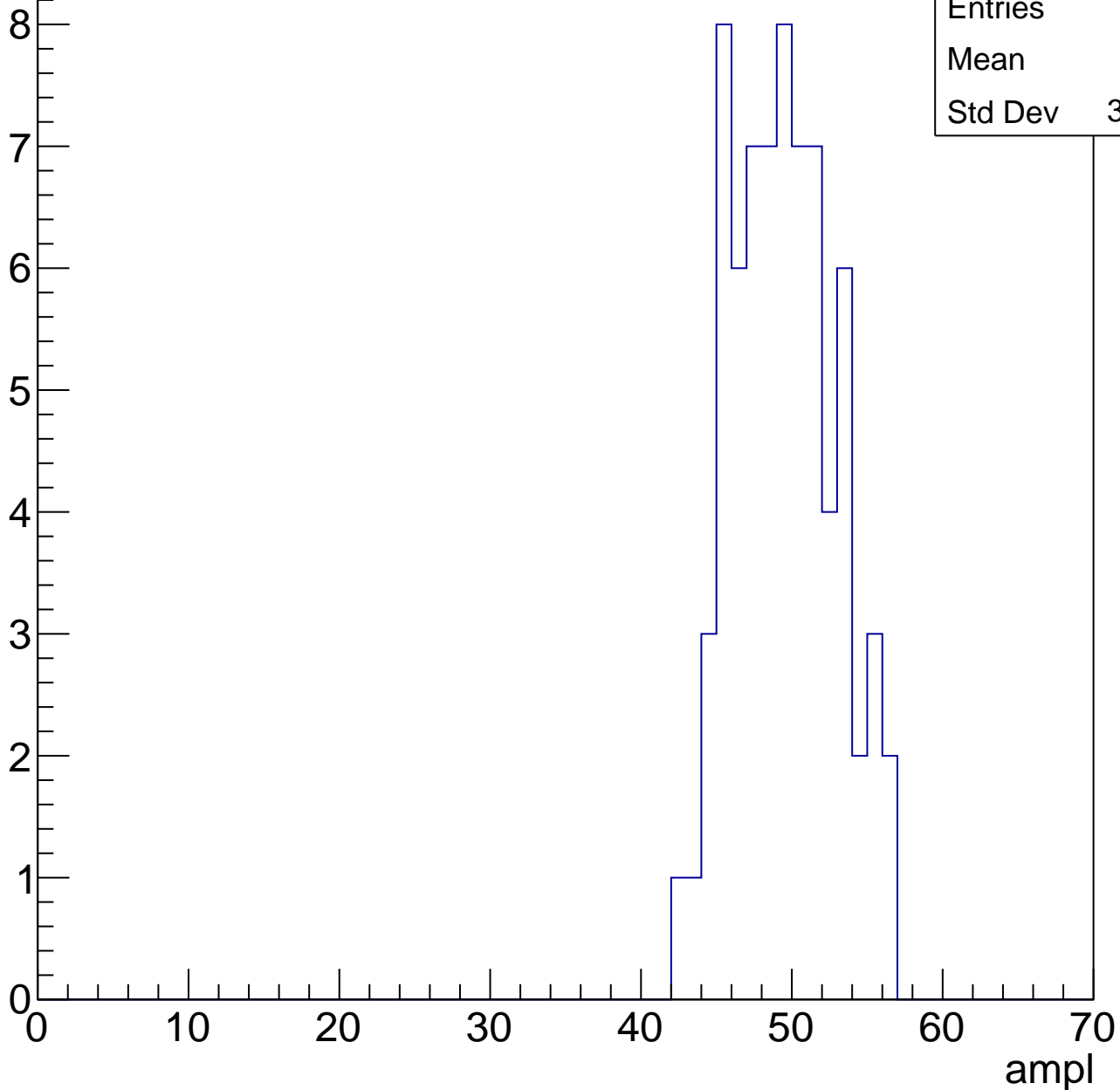
**Gaus Width: 2.0815**



# B1L100S, U6-ch44, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



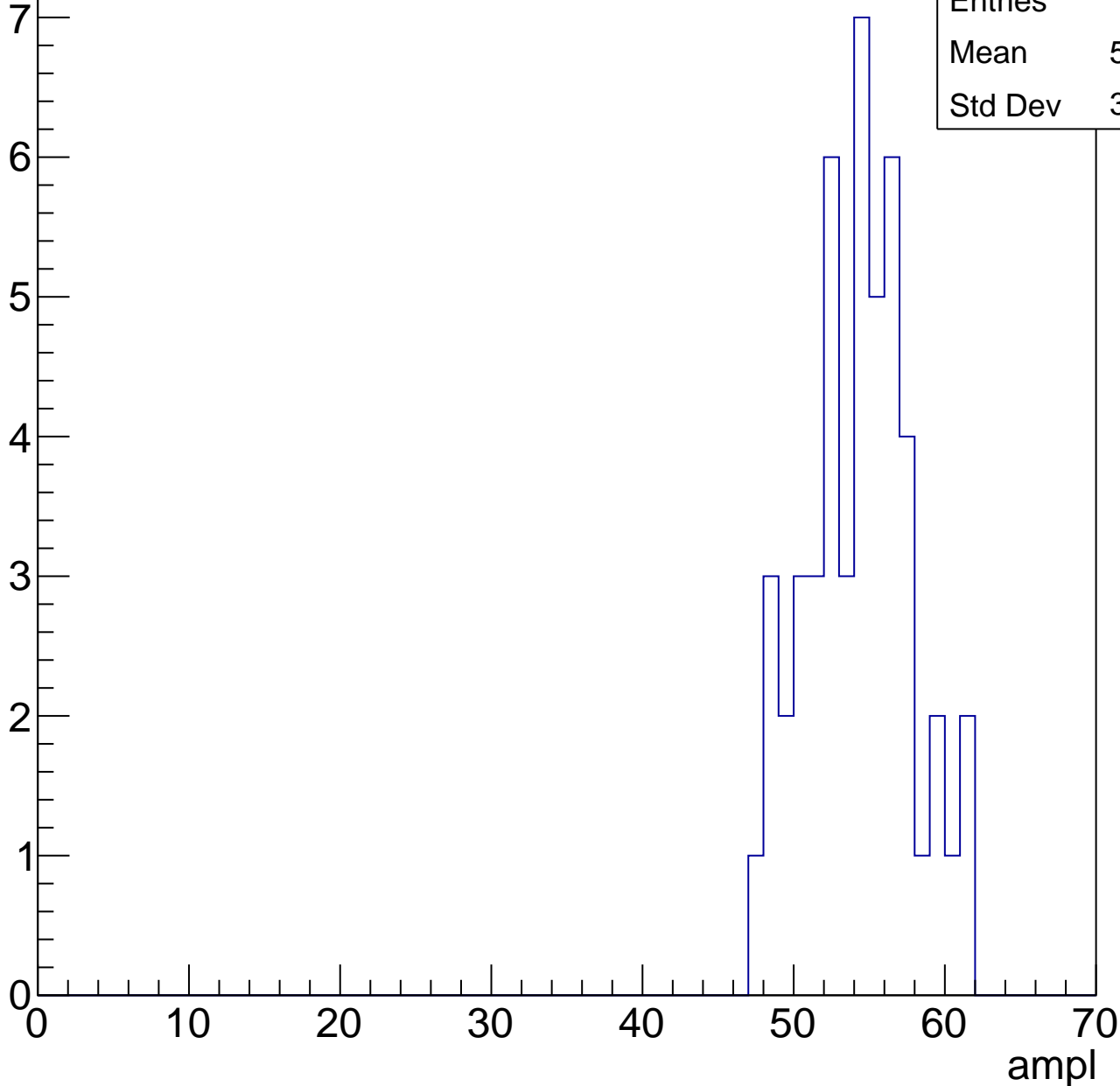
Entries	72
Mean	49
Std Dev	3.333

# B1L100S, U6-ch44, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

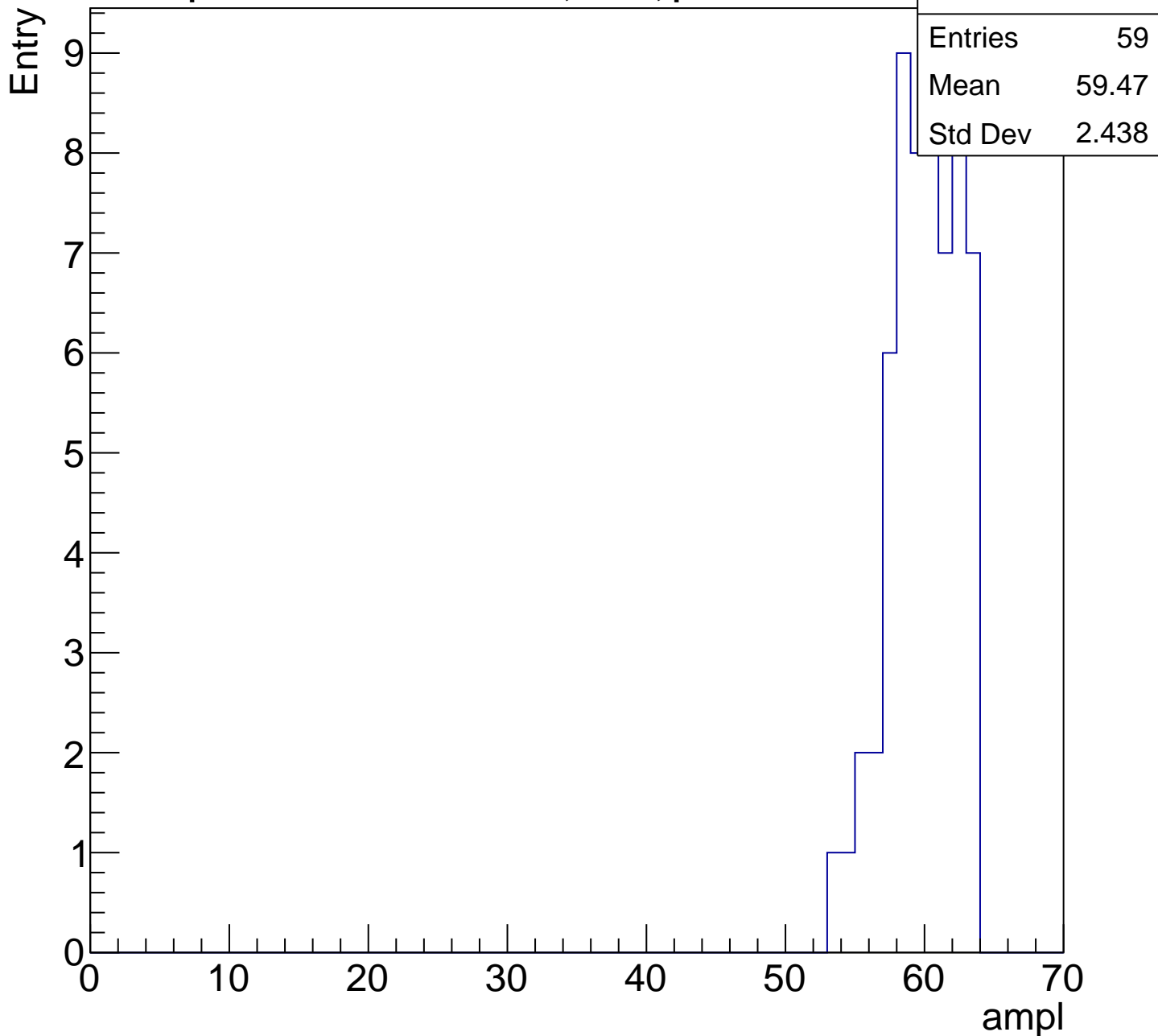
Entry

Entries	49
Mean	53.84
Std Dev	3.419



# B1L100S, U6-ch44, adc5

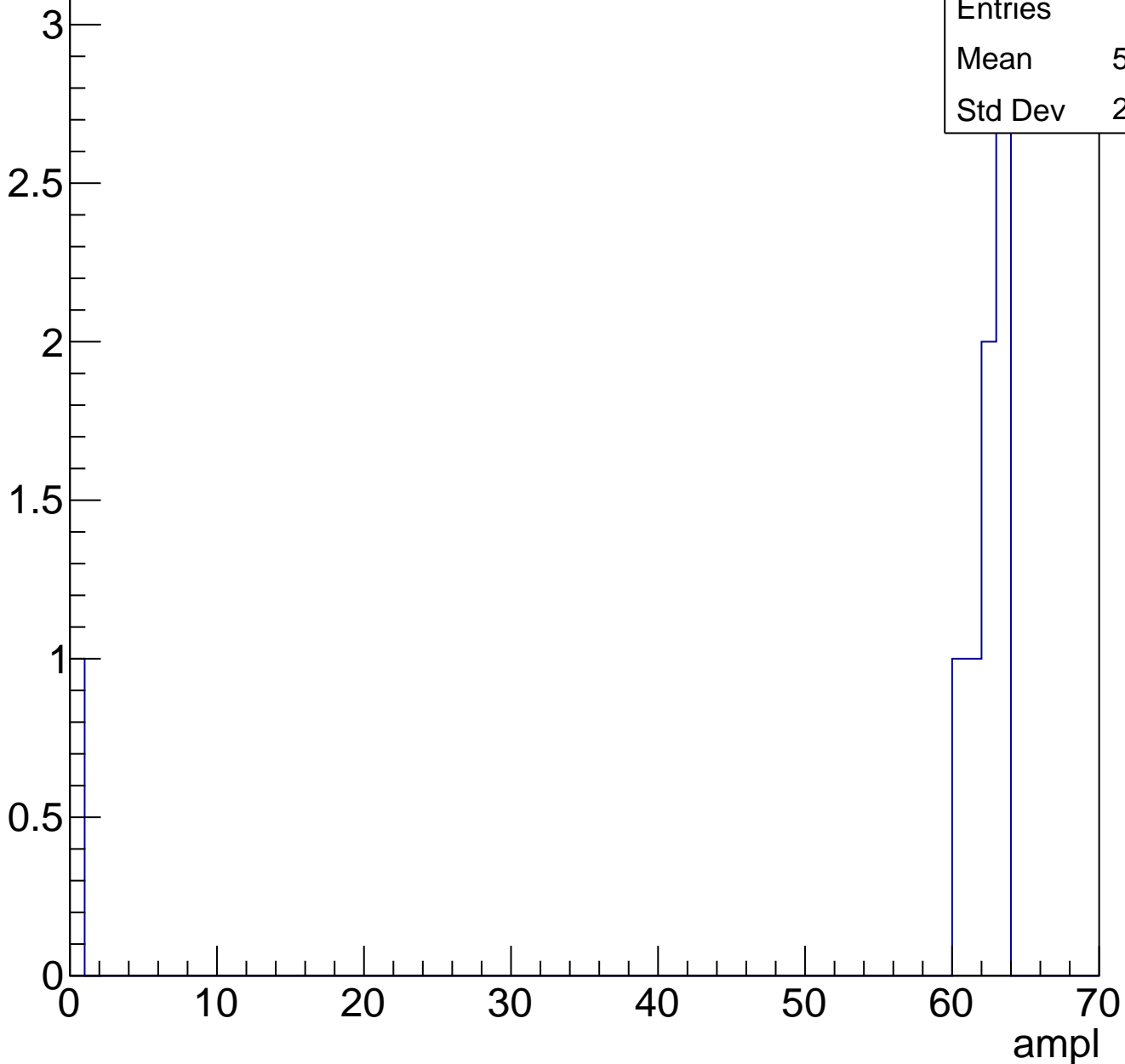
calib\_packv5\_042523\_0143.root, FC#4, port A2



# B1L100S, U6-ch44, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry





# B1L100S, U6-ch44, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L100S, U6-ch45, adc0

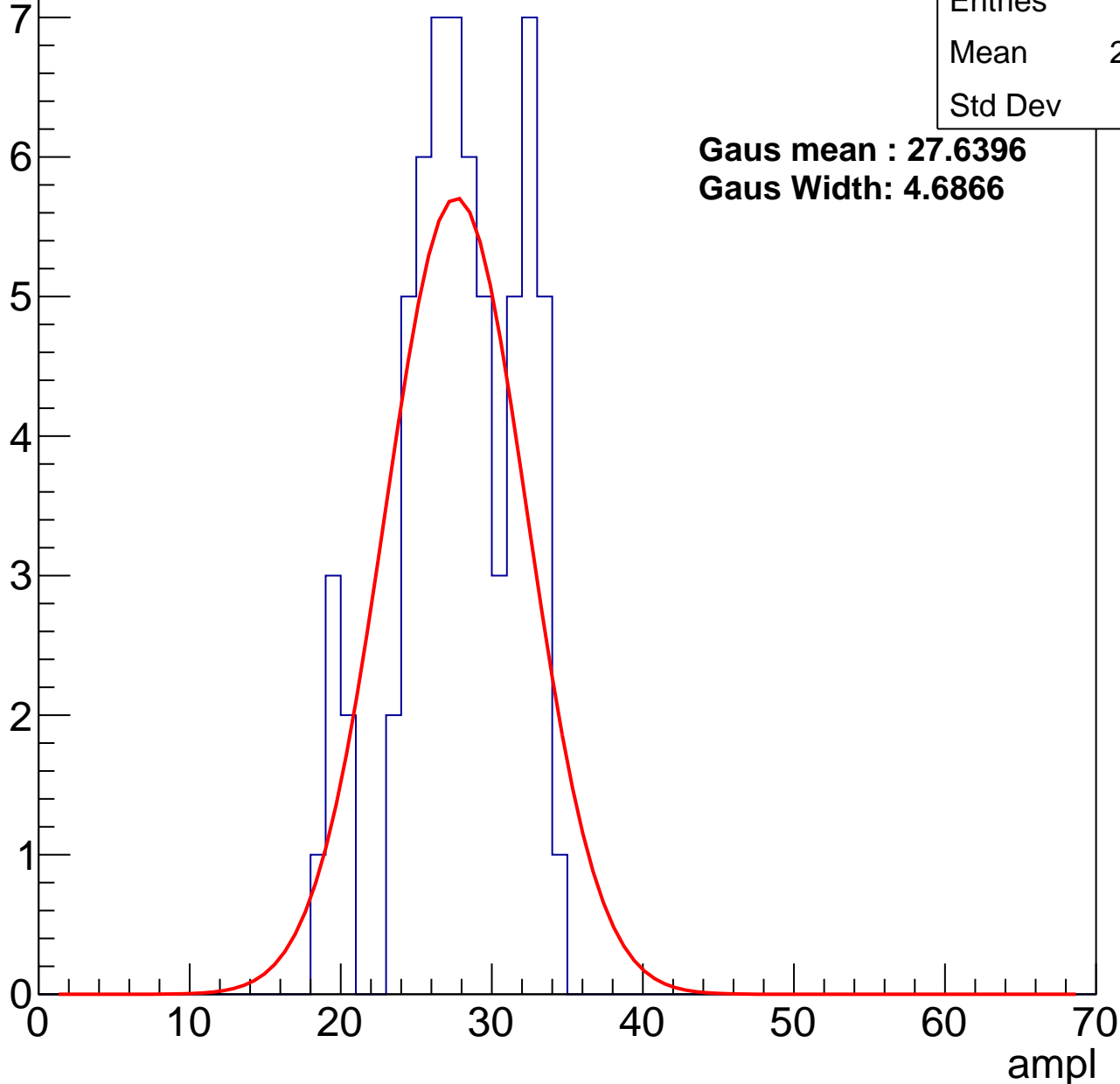
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	65
Mean	27.43
Std Dev	3.93

**Gaus mean : 27.6396**

**Gaus Width: 4.6866**



# B1L100S, U6-ch45, adc1

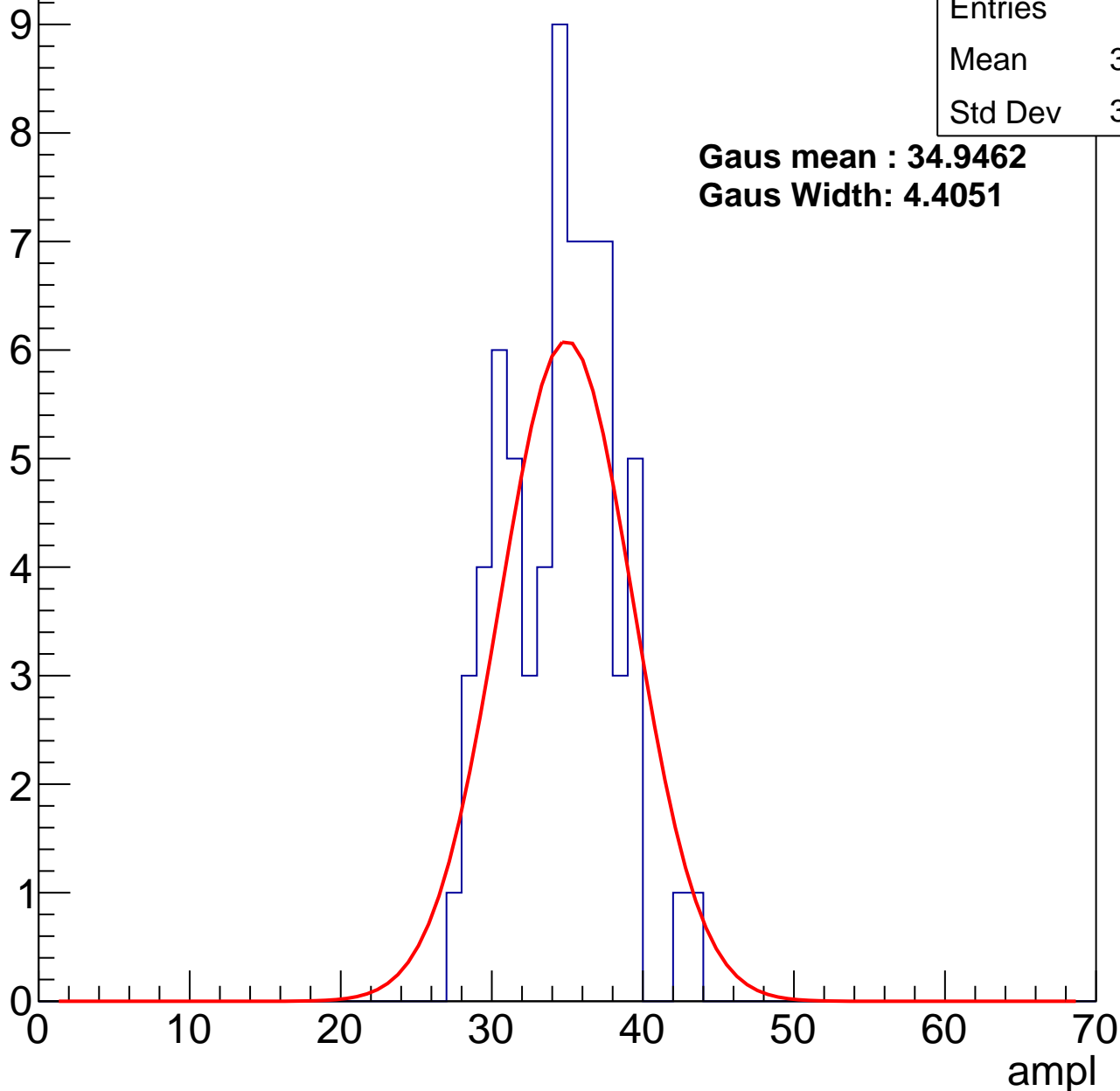
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	66
Mean	34.03
Std Dev	3.546

**Gaus mean : 34.9462**

**Gaus Width: 4.4051**



# B1L100S, U6-ch45, adc2

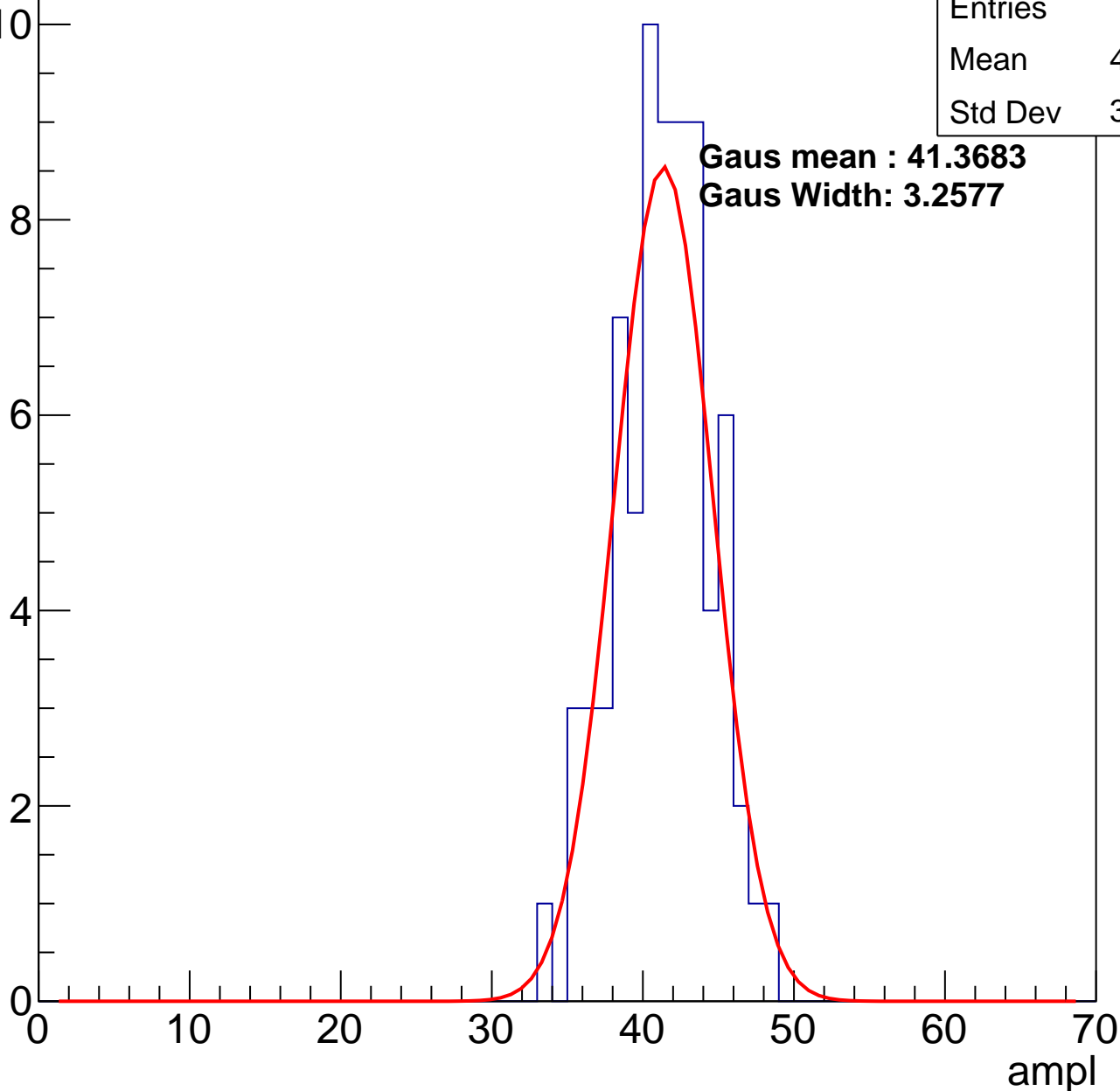
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	73
Mean	40.89
Std Dev	3.095

**Gaus mean : 41.3683**

**Gaus Width: 3.2577**

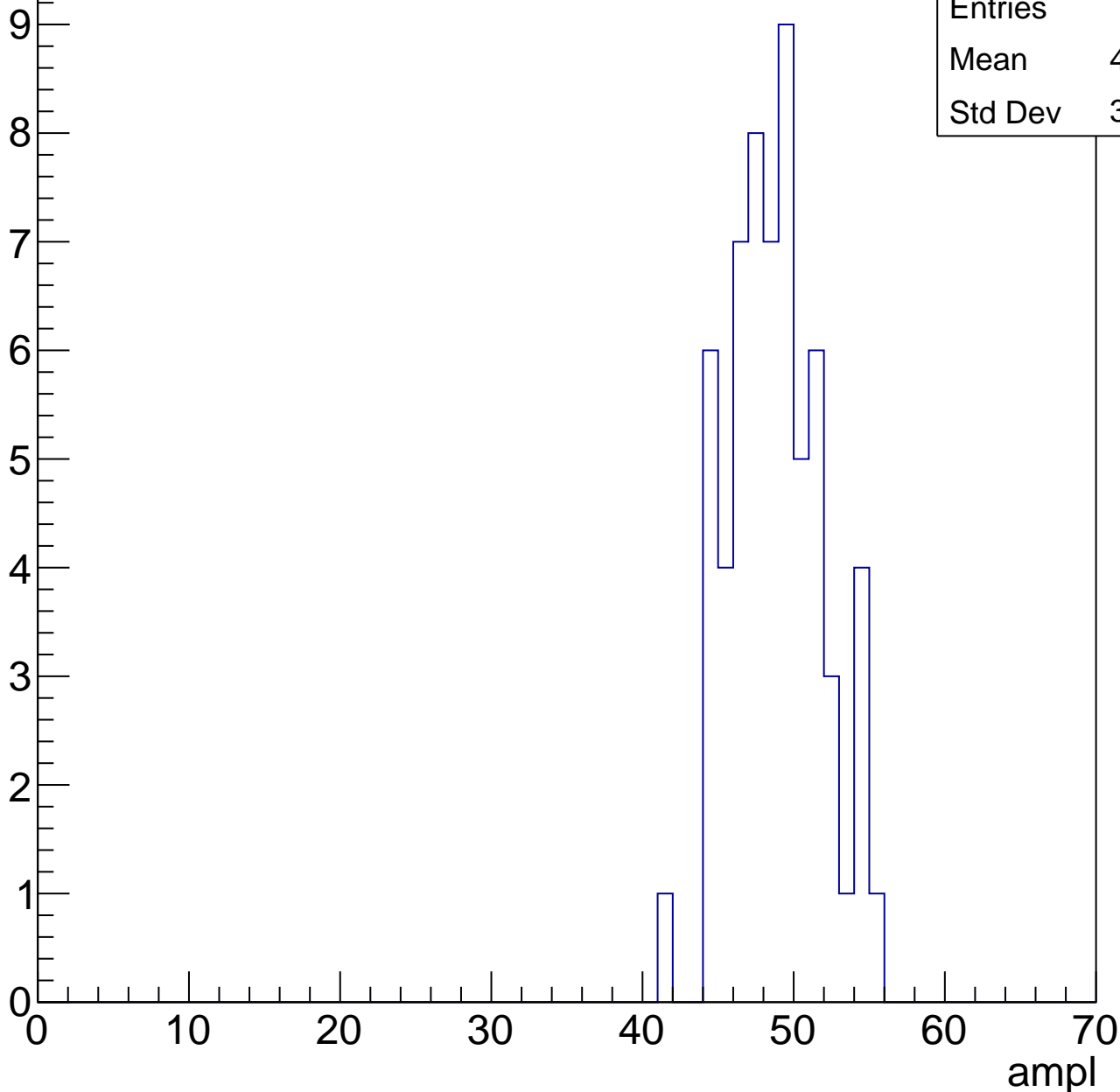


# B1L100S, U6-ch45, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

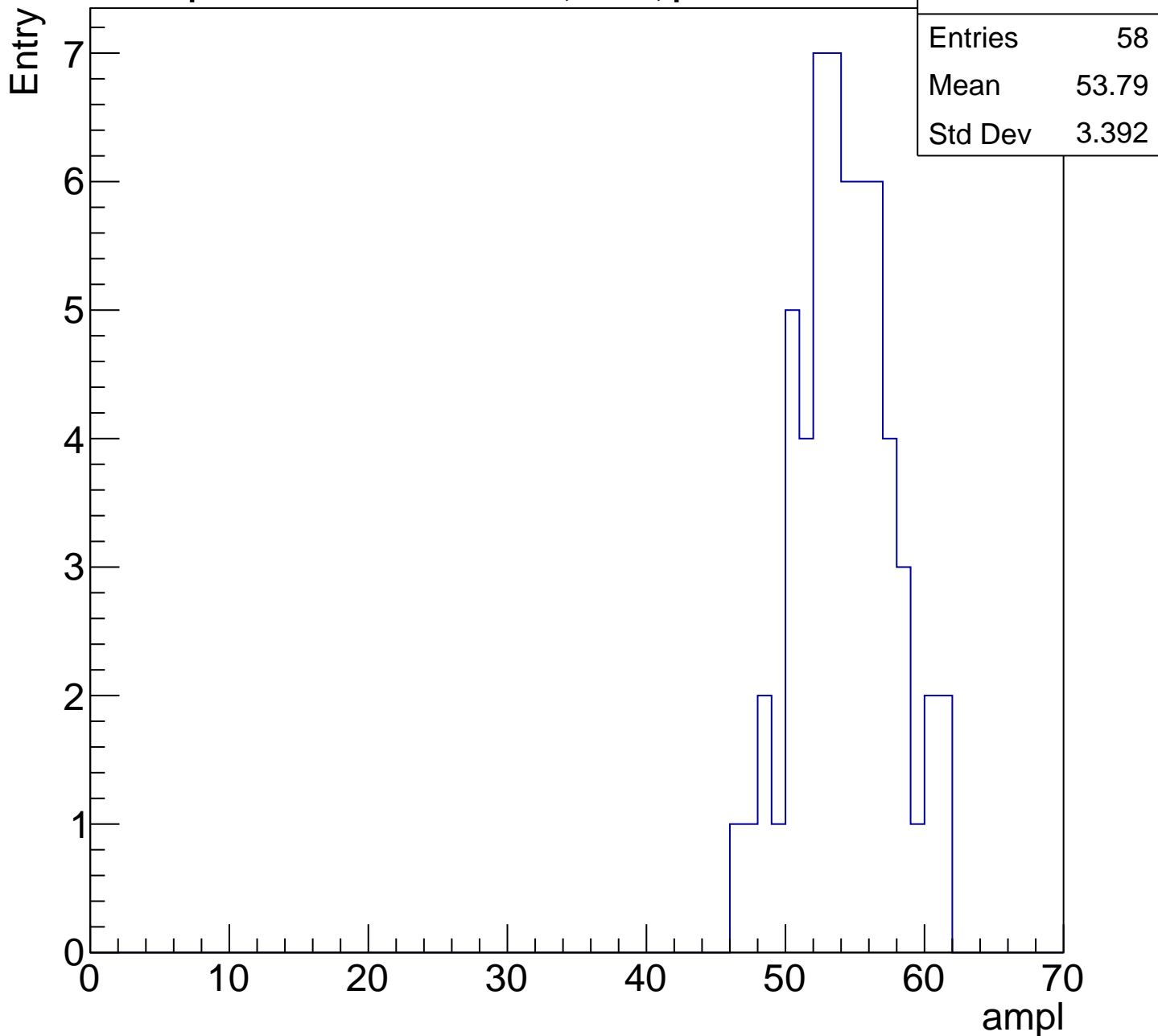
Entry

Entries	62
Mean	48.32
Std Dev	3.004



# B1L100S, U6-ch45, adc4

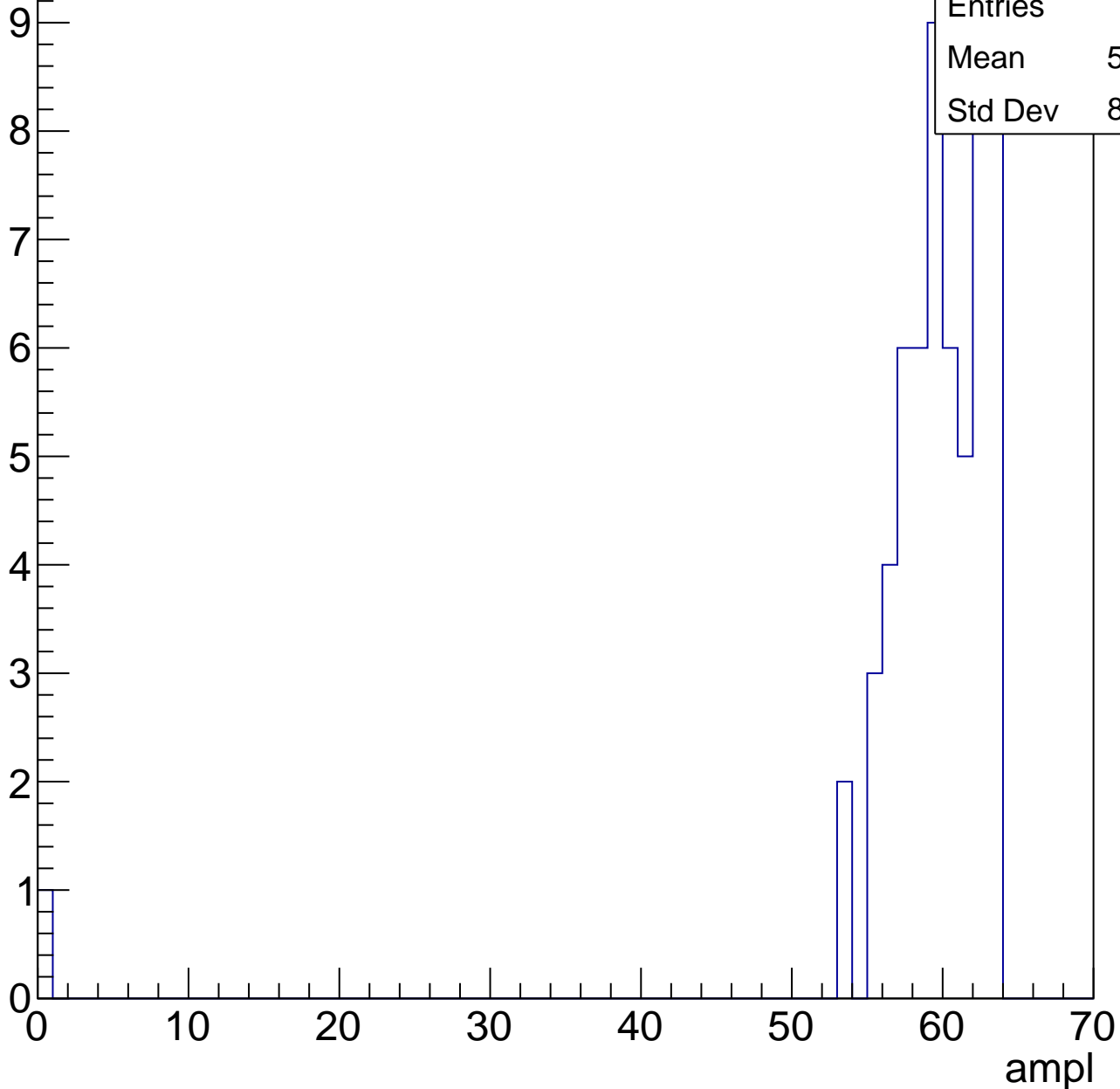
calib\_packv5\_042523\_0143.root, FC#4, port A2



# B1L100S, U6-ch45, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

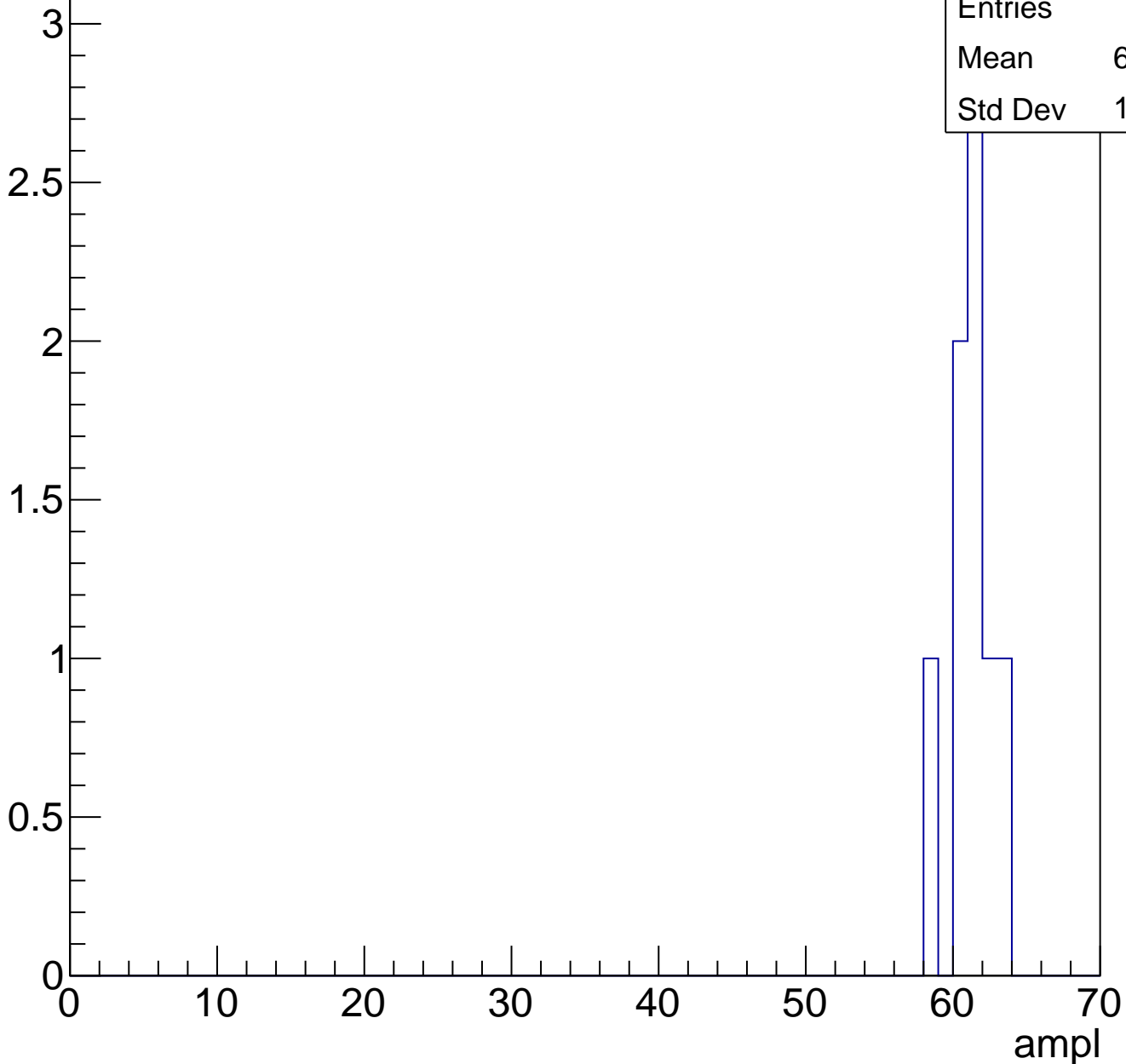
Entry



# B1L100S, U6-ch45, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry





# B1L100S, U6-ch45, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



# B1L100S, U6-ch46, adc0

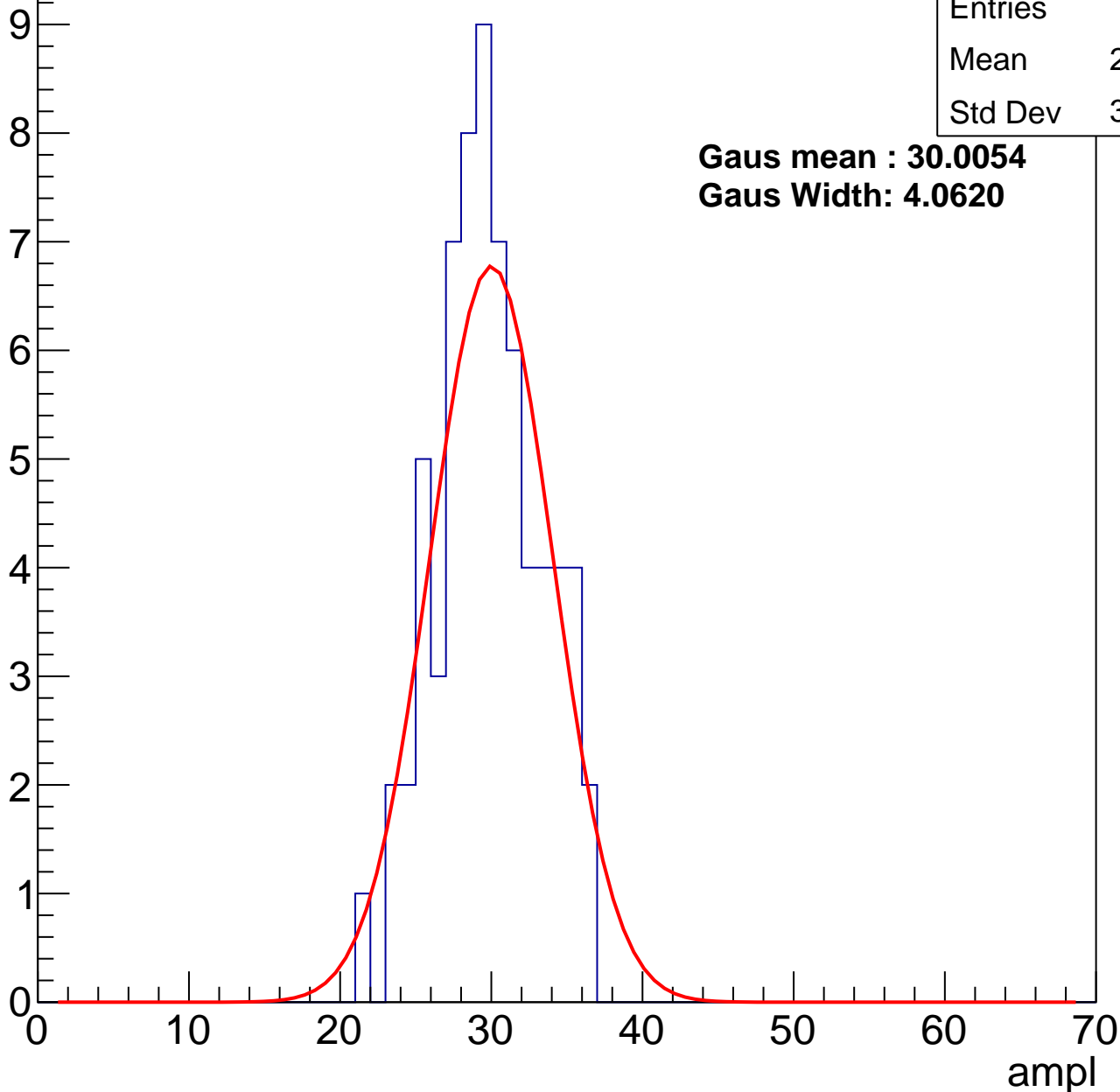
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	68
Mean	29.35
Std Dev	3.416

**Gaus mean : 30.0054**

**Gaus Width: 4.0620**



# B1L100S, U6-ch46, adc1

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	76
Mean	36.33
Std Dev	3.788

**Gaus mean : 36.9047**

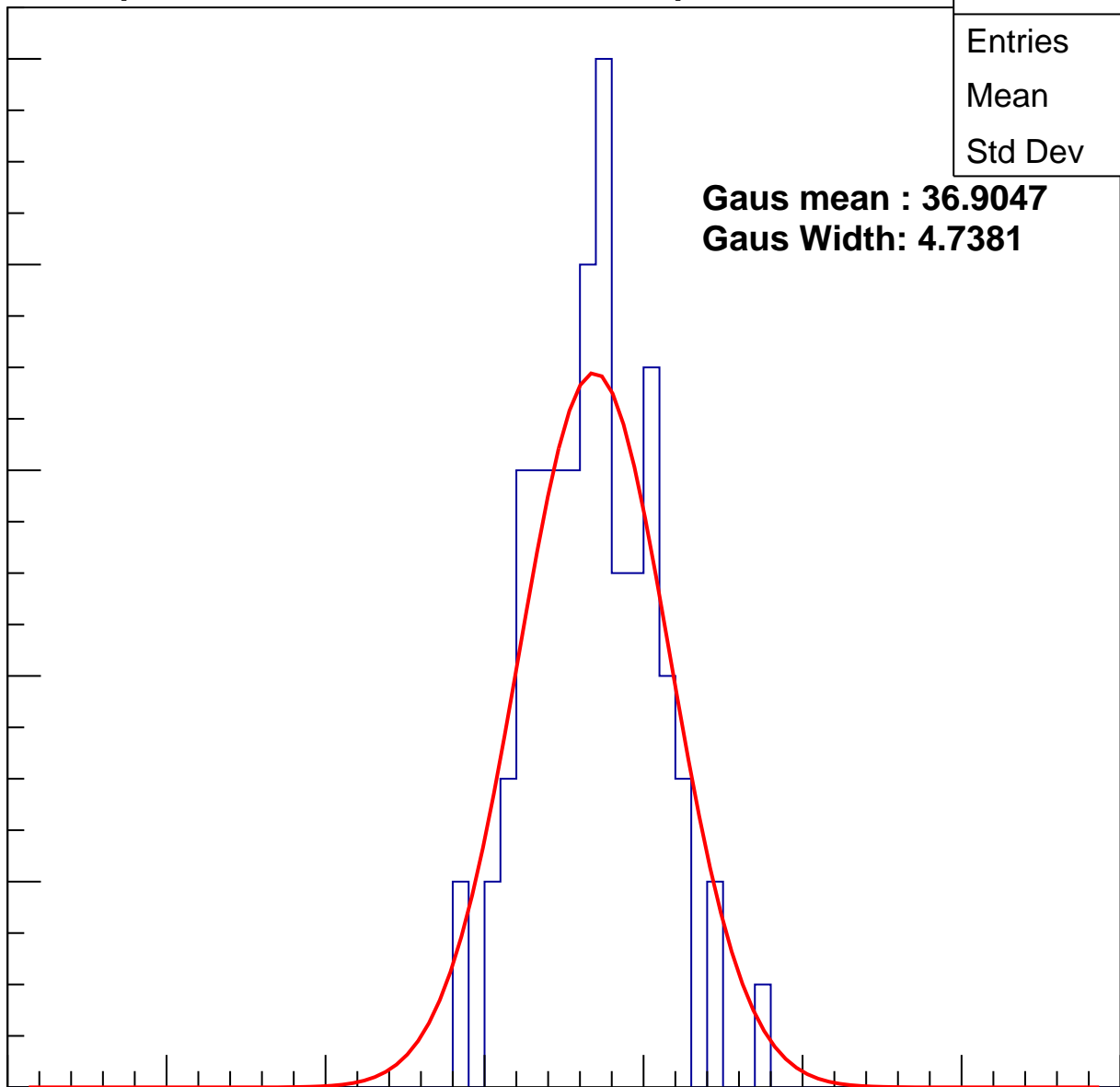
**Gaus Width: 4.7381**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L100S, U6-ch46, adc2

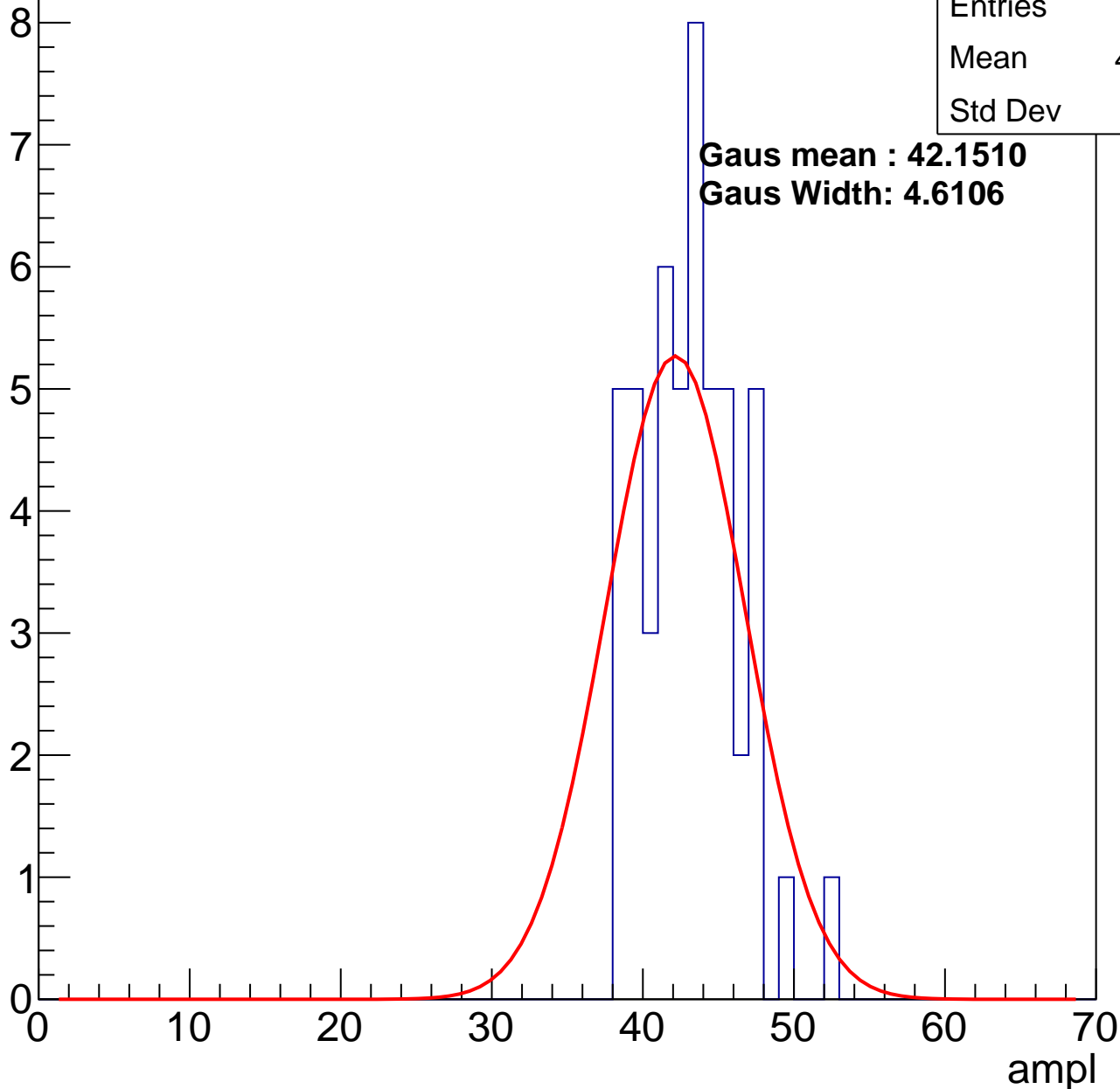
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	51
Mean	42.71
Std Dev	3.12

**Gaus mean : 42.1510**

**Gaus Width: 4.6106**

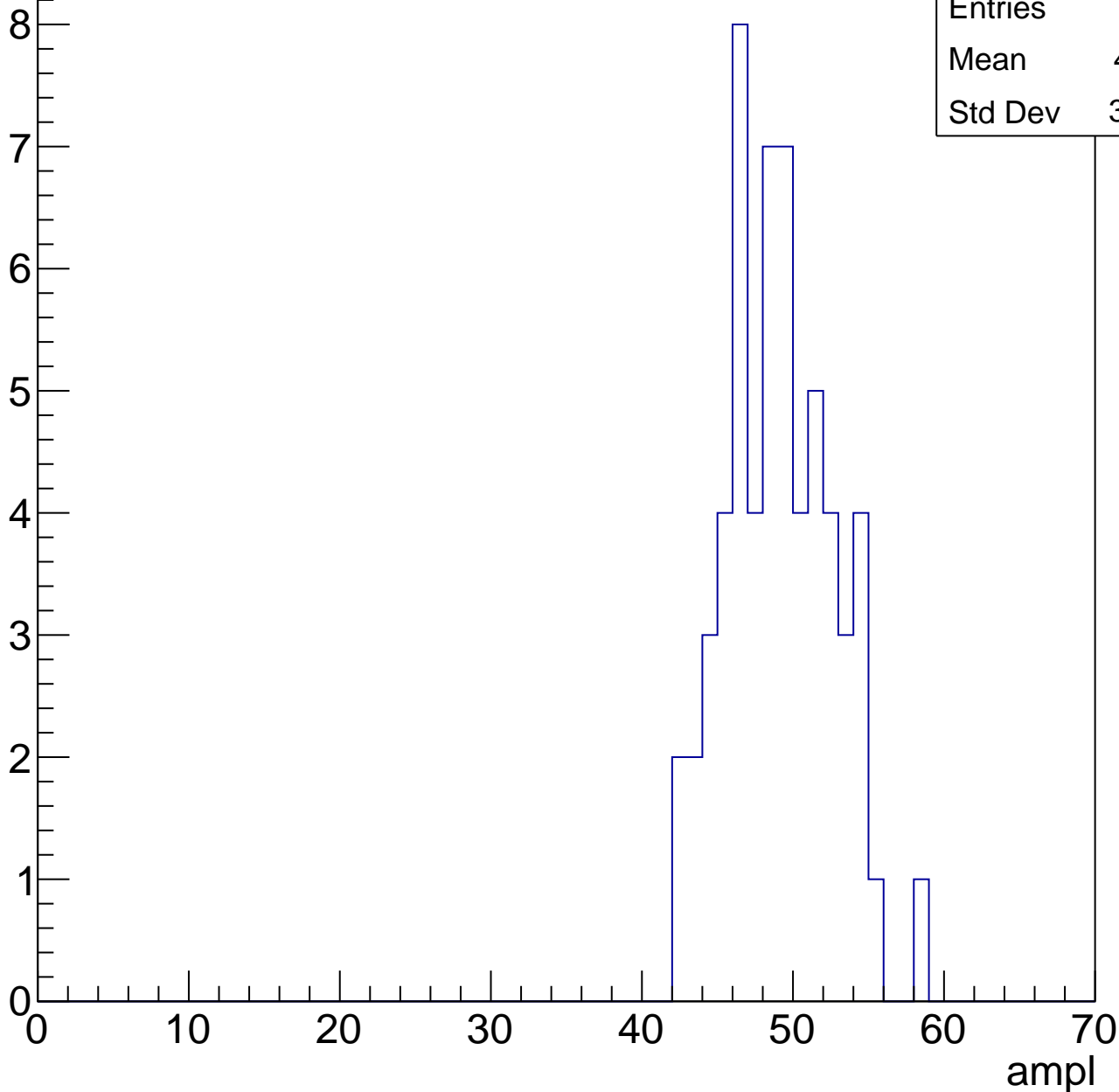


# B1L100S, U6-ch46, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

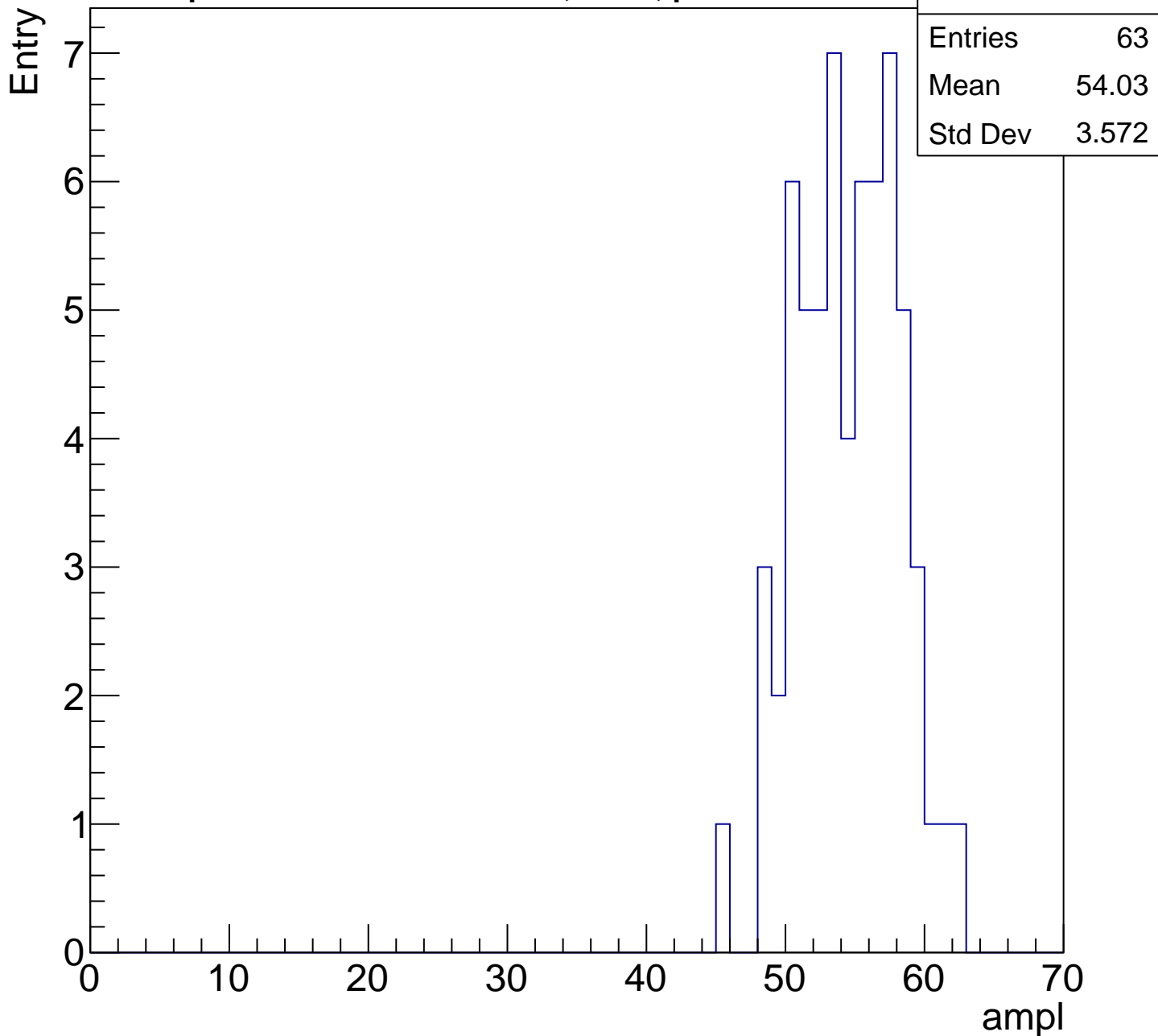
Entry

Entries	59
Mean	48.61
Std Dev	3.493



# B1L100S, U6-ch46, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2



# B1L100S, U6-ch46, adc5

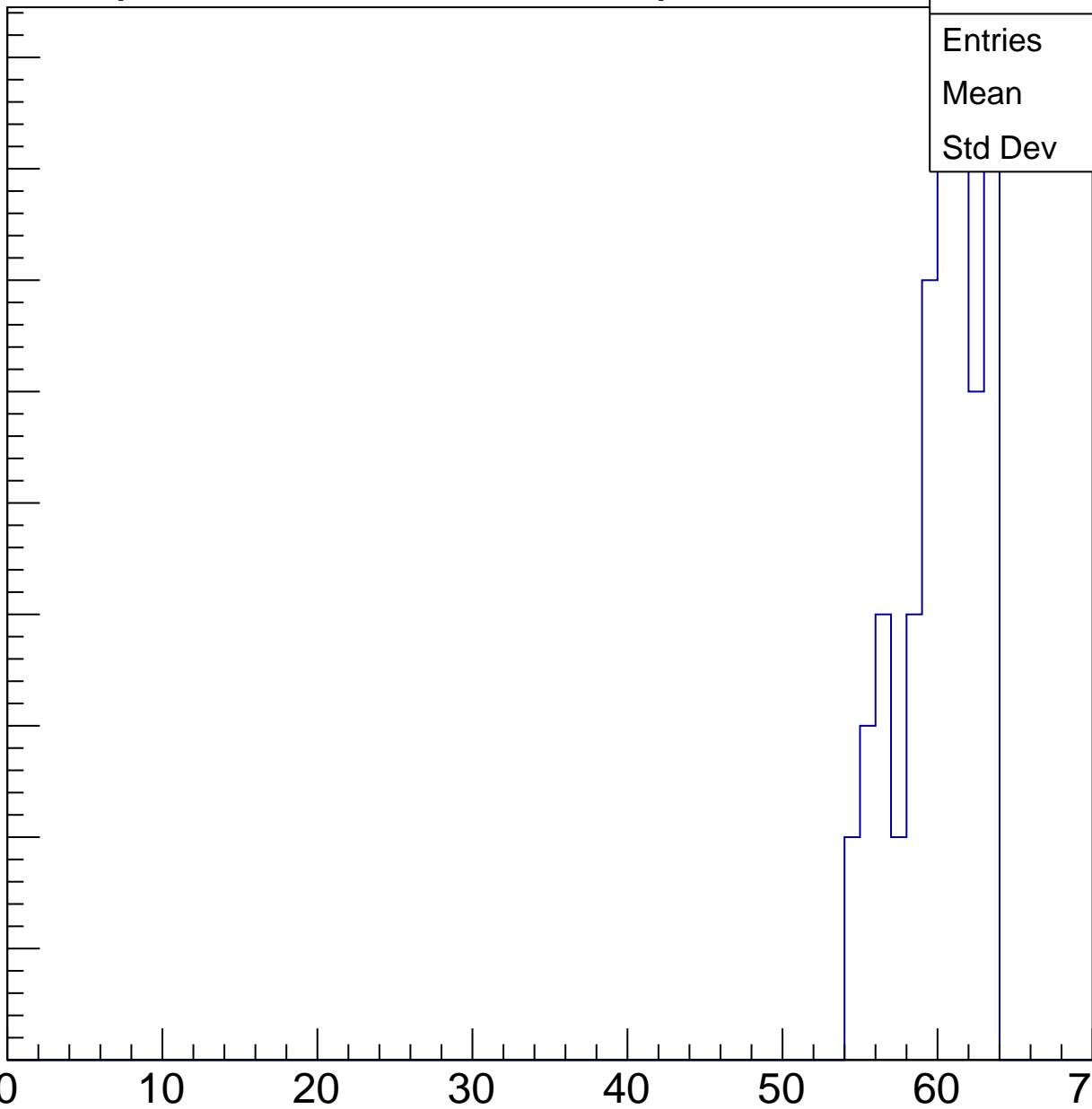
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	53
Mean	59.62
Std Dev	2.564

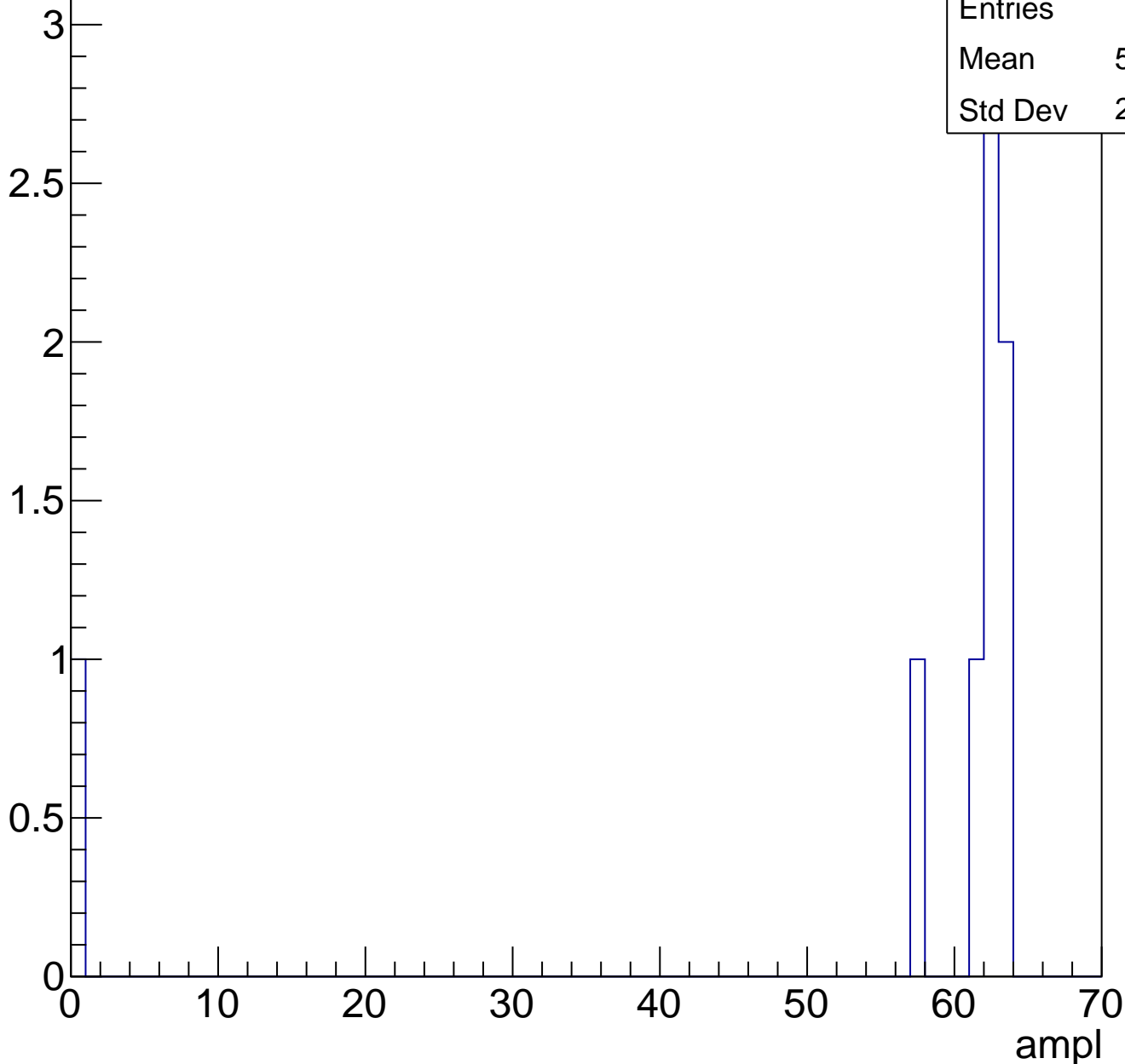
ampl



# B1L100S, U6-ch46, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry





# B1L100S, U6-ch46, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



# B1L100S, U6-ch47, adc0

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	78
Mean	29.41
Std Dev	3.353

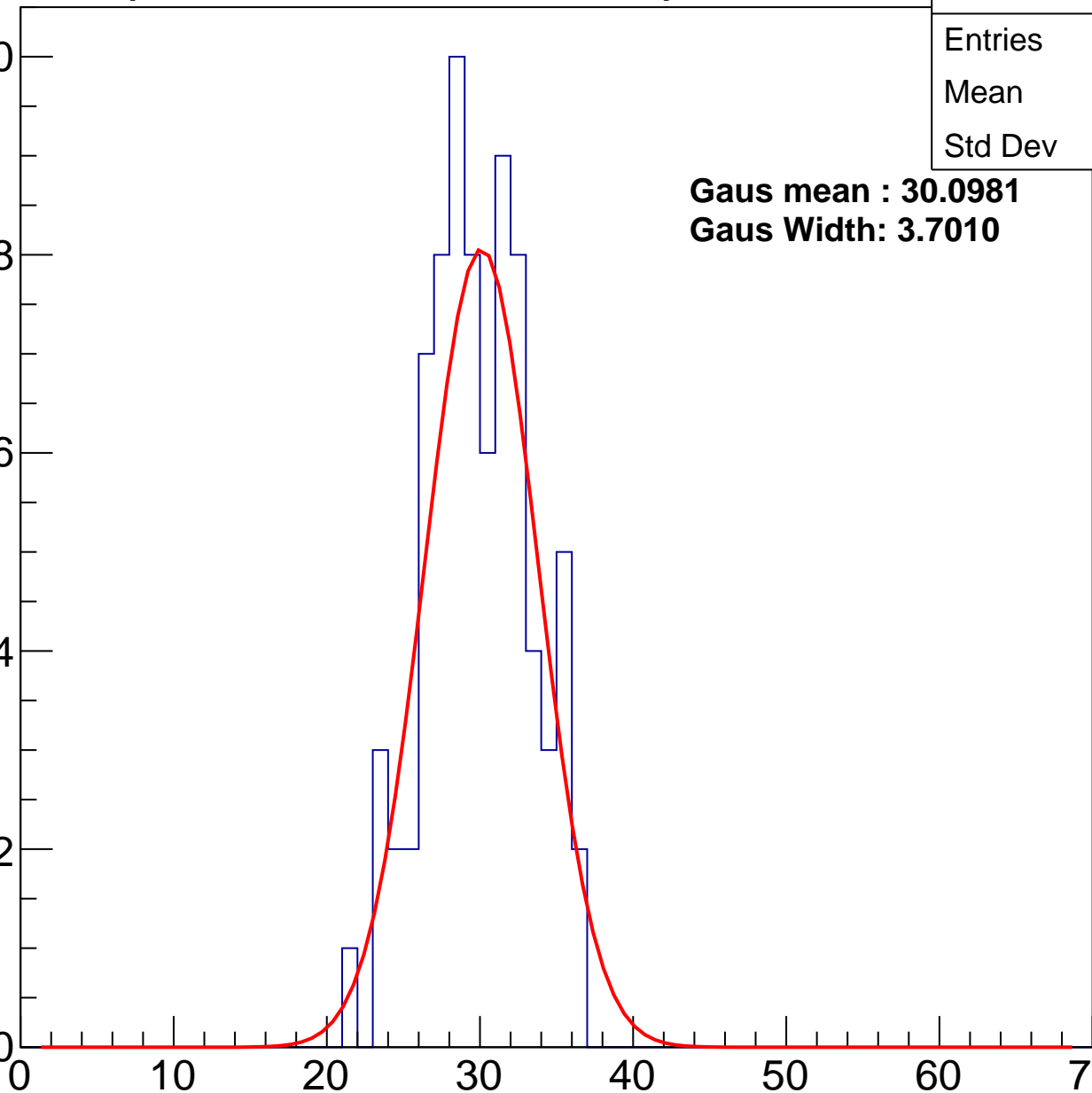
**Gaus mean : 30.0981**

**Gaus Width: 3.7010**

Entry

10  
8  
6  
4  
2  
0

ampl



# B1L100S, U6-ch47, adc1

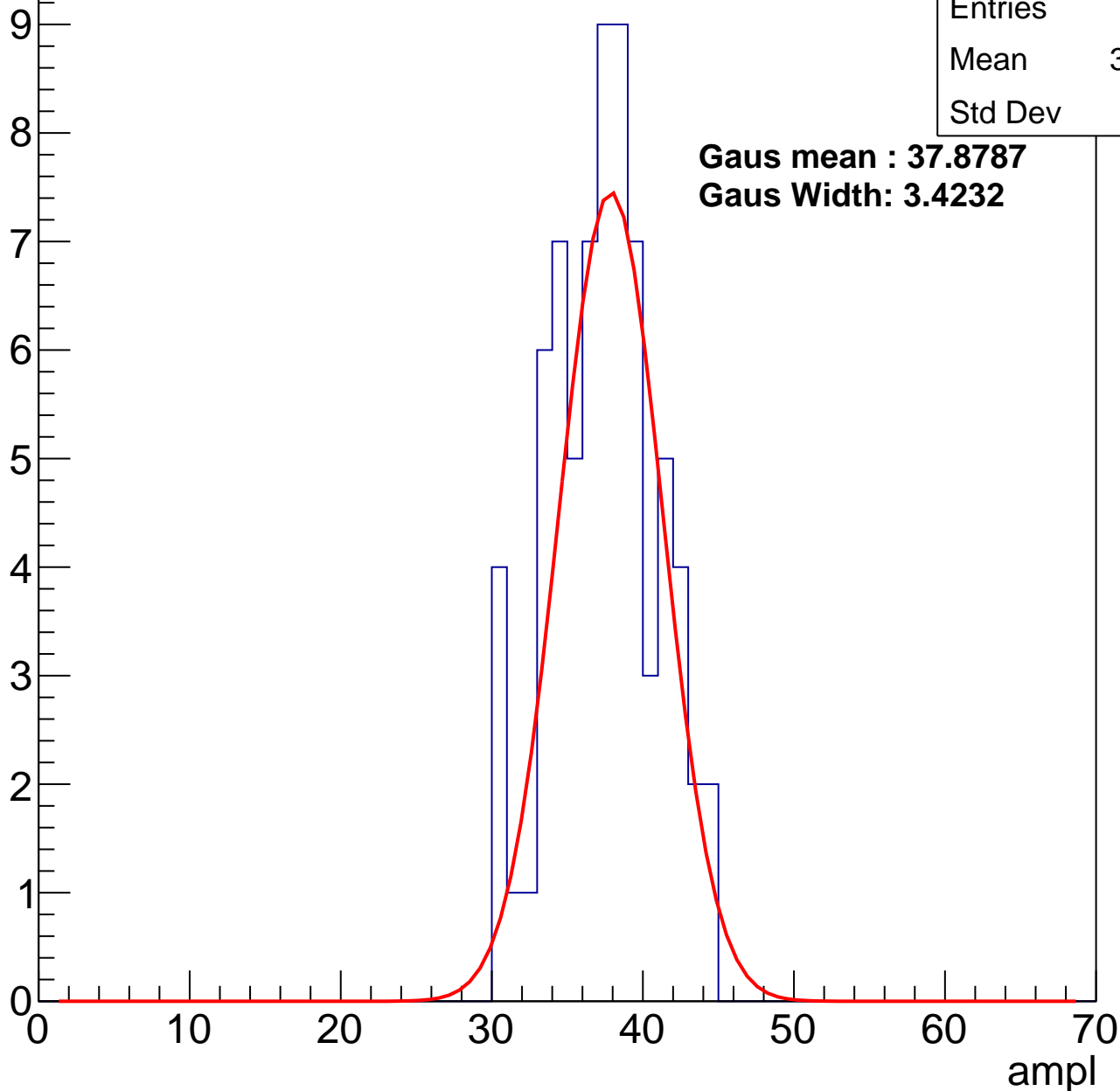
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	72
Mean	36.96
Std Dev	3.45

**Gaus mean : 37.8787**

**Gaus Width: 3.4232**



# B1L100S, U6-ch47, adc2

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	72
Mean	43.94
Std Dev	3.378

**Gaus mean : 44.6056**

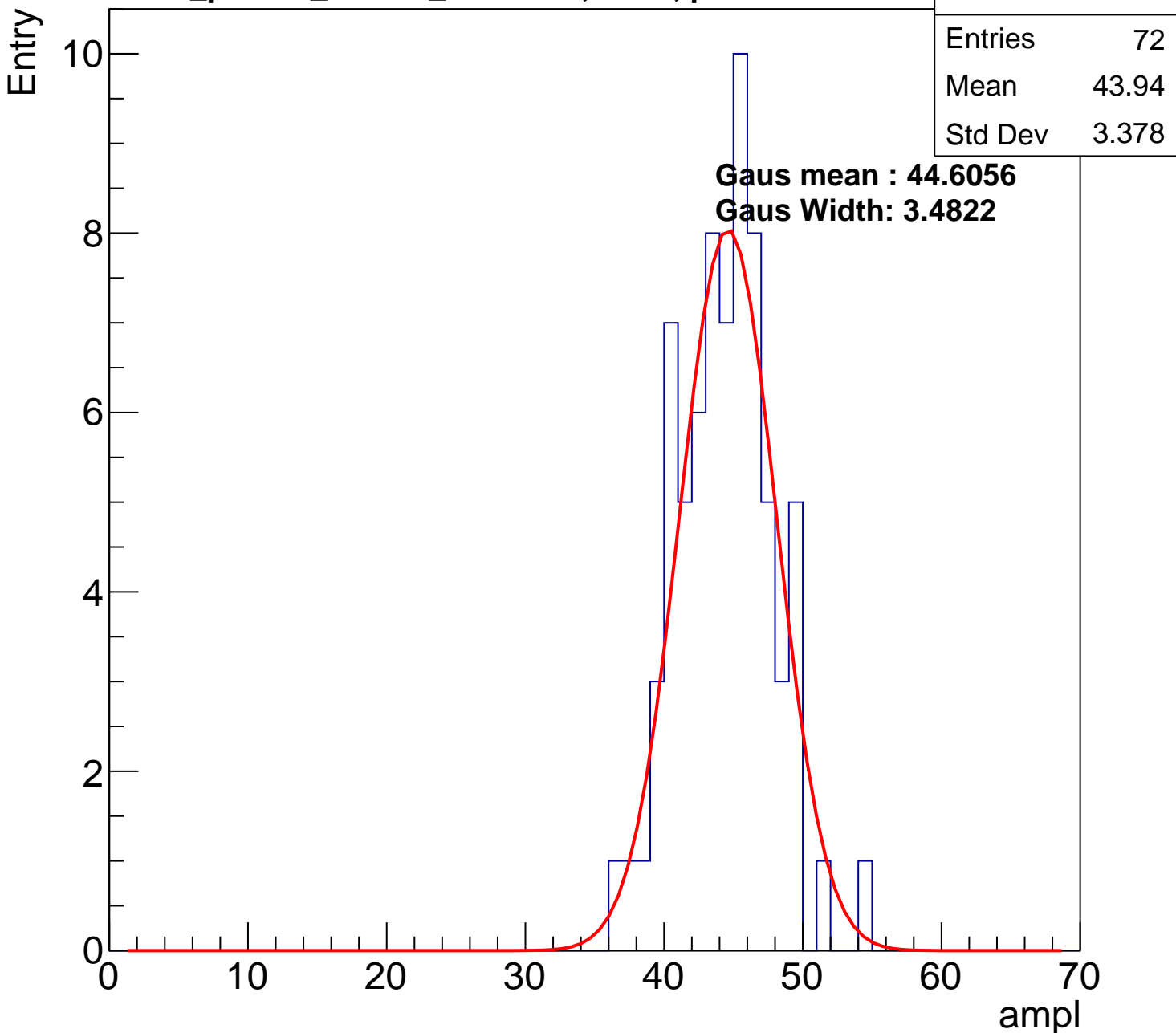
**Gaus Width: 3.4822**

Entry

10  
8  
6  
4  
2  
0

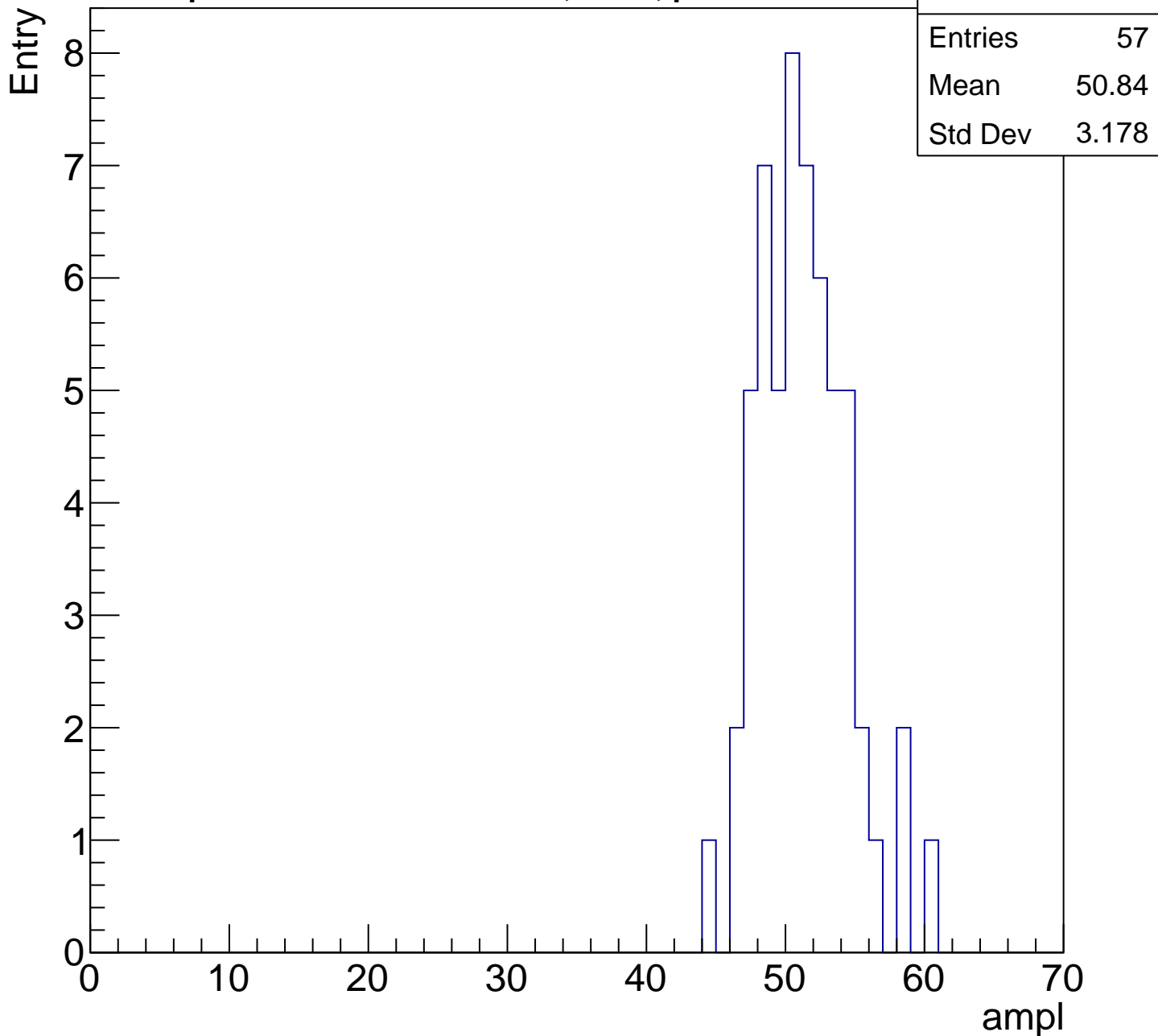
ampl

0 10 20 30 40 50 60 70



# B1L100S, U6-ch47, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2



# B1L100S, U6-ch47, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

10

8

6

4

2

0

0

10

20

30

40

50

60

ampl

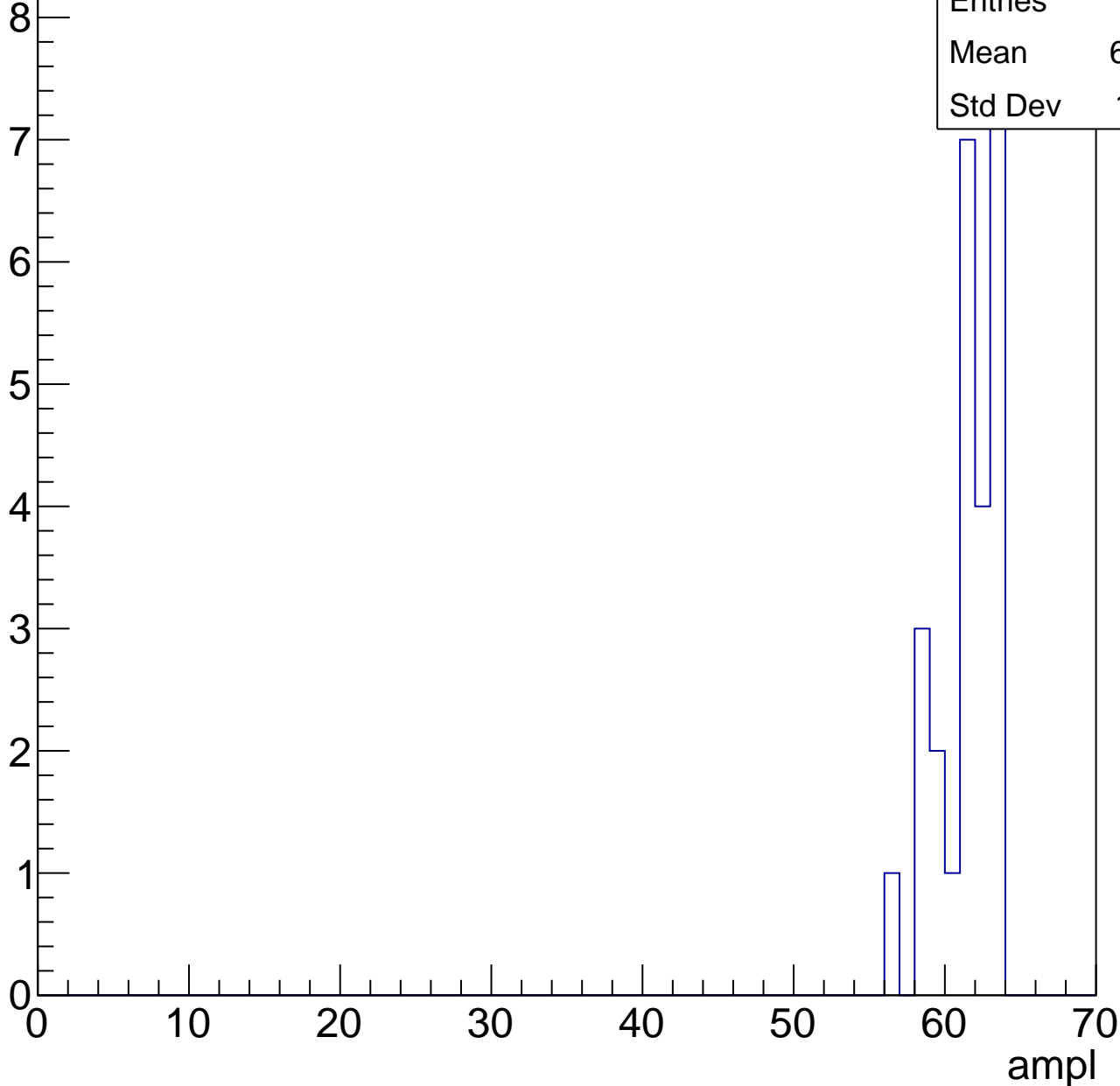
Entries	72
Mean	56.78
Std Dev	3.211

# B1L100S, U6-ch47, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	26
Mean	61.04
Std Dev	1.931



# B1L100S, U6-ch47, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

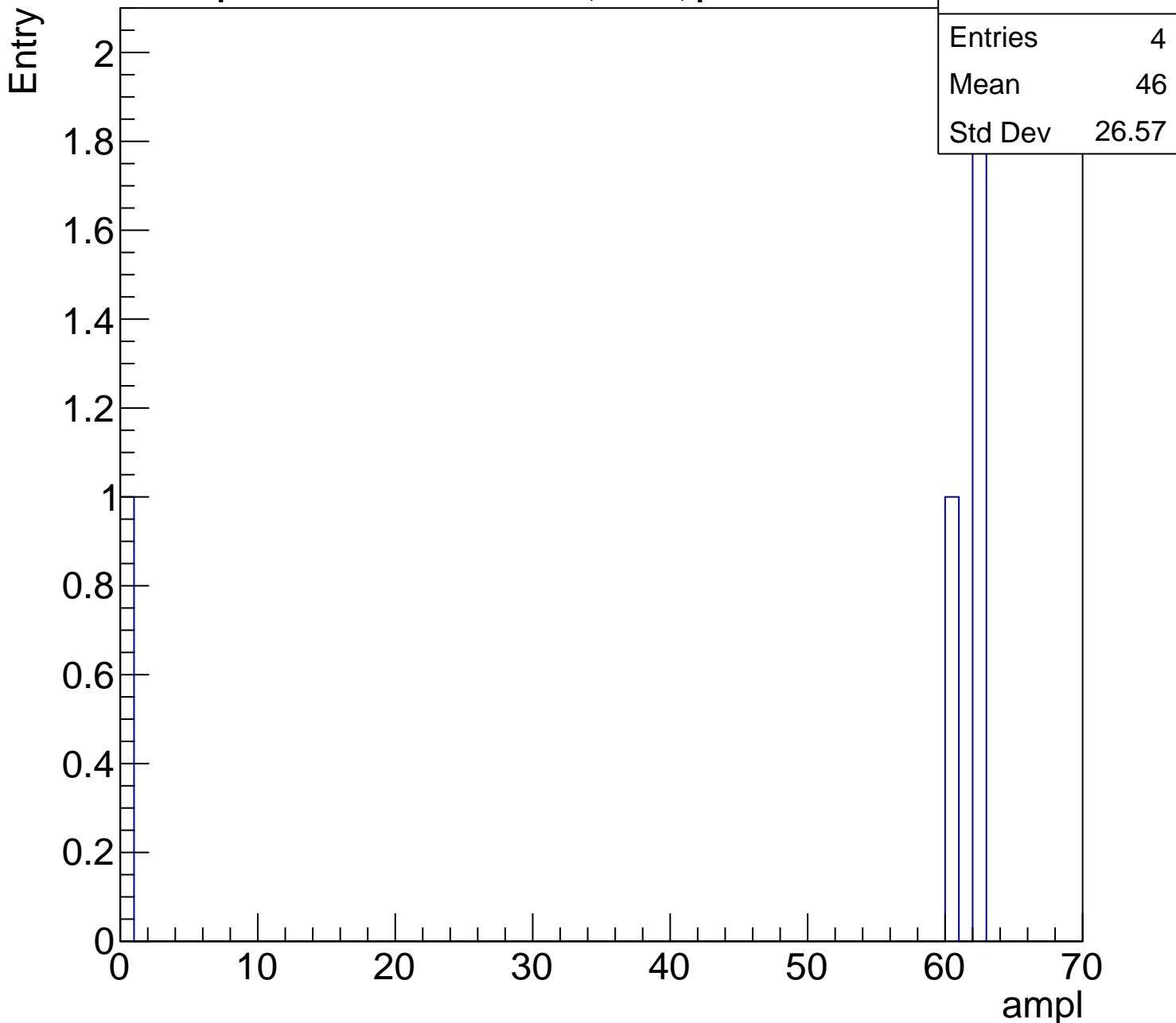
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	4
Mean	46
Std Dev	26.57

0 10 20 30 40 50 60 70

ampl

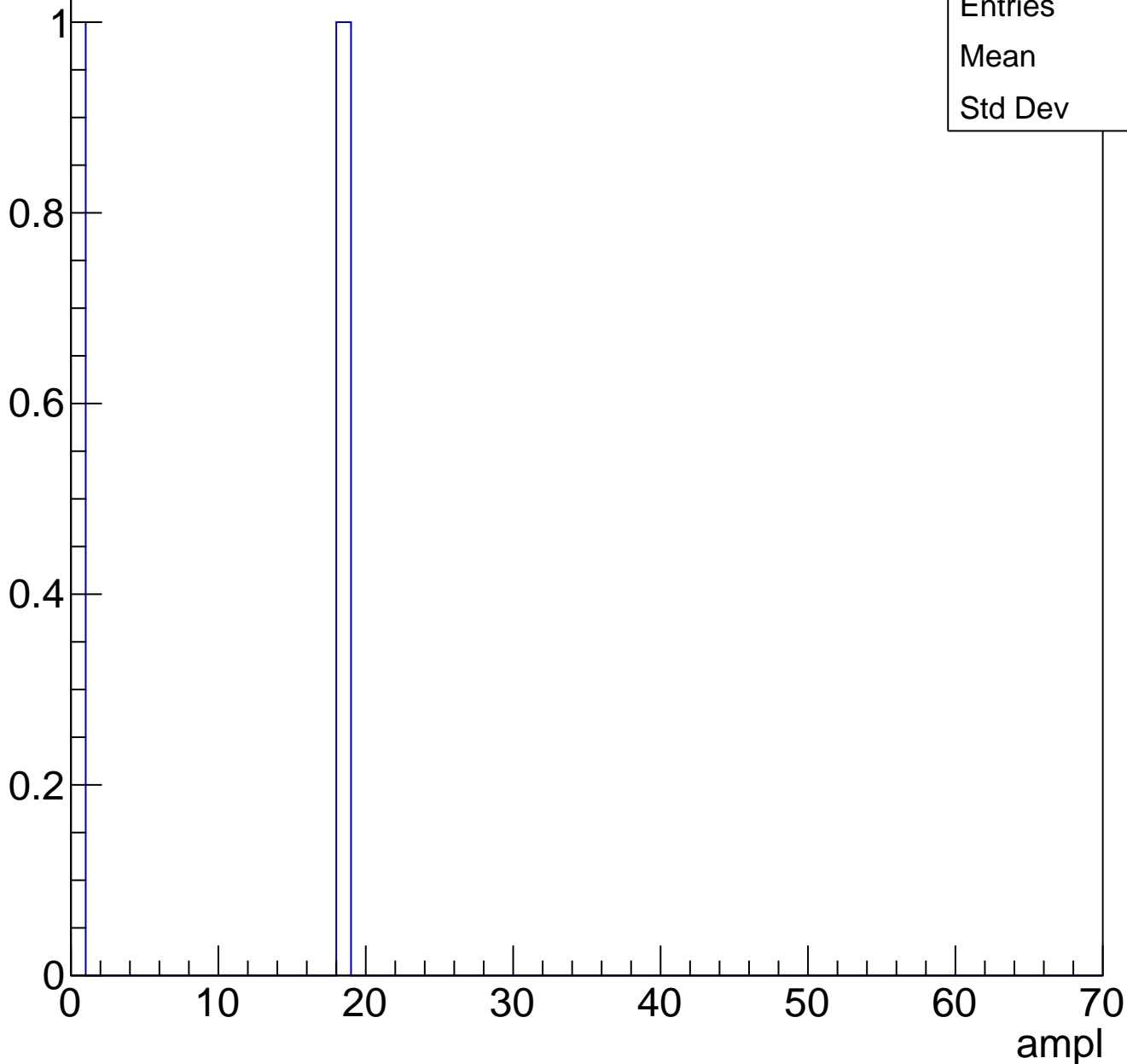




# B1L100S, U6-ch47, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



# B1L100S, U6-ch48, adc0

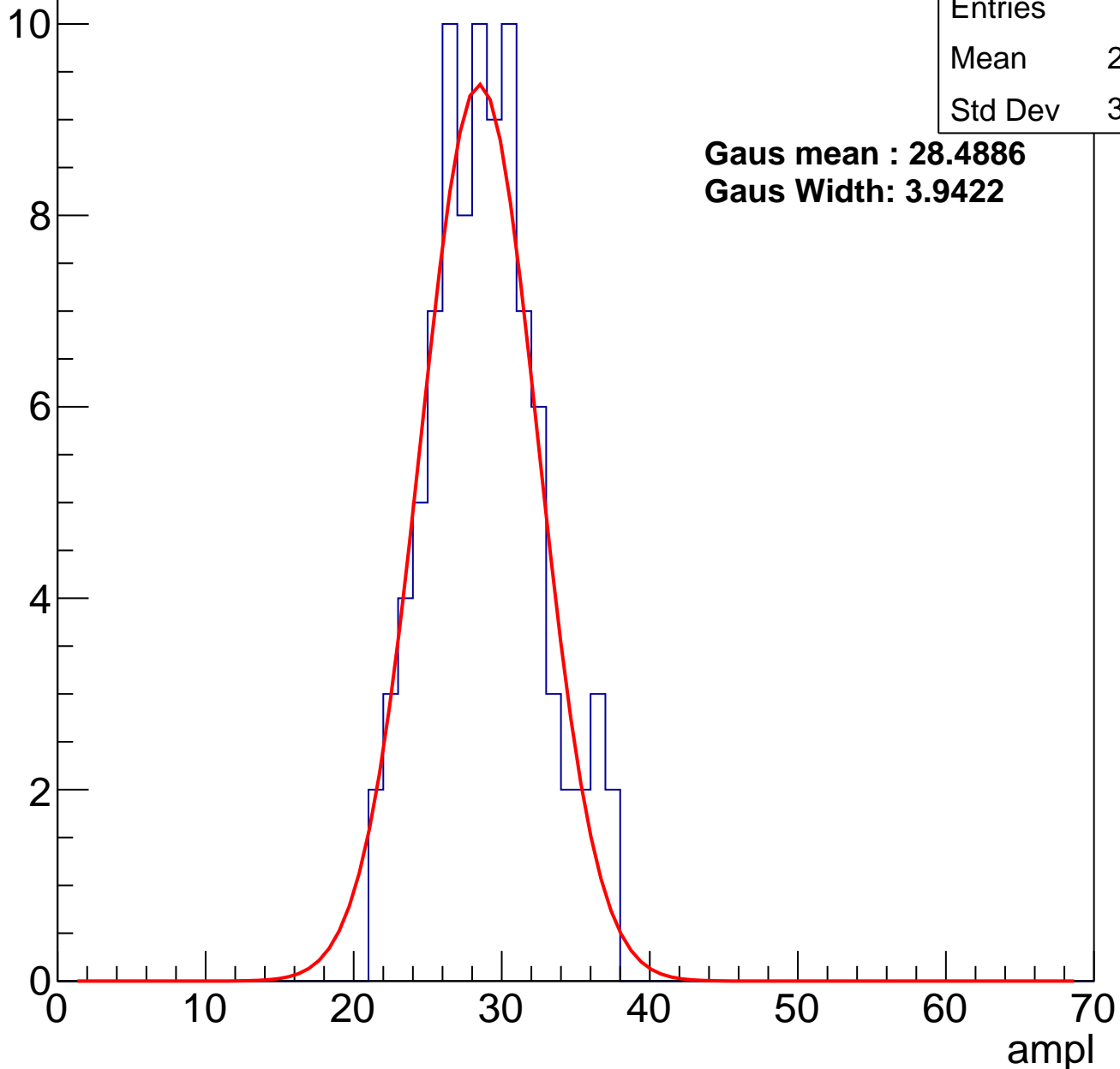
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	93
Mean	28.39
Std Dev	3.724

**Gaus mean : 28.4886**

**Gaus Width: 3.9422**

Entry



# B1L100S, U6-ch48, adc1

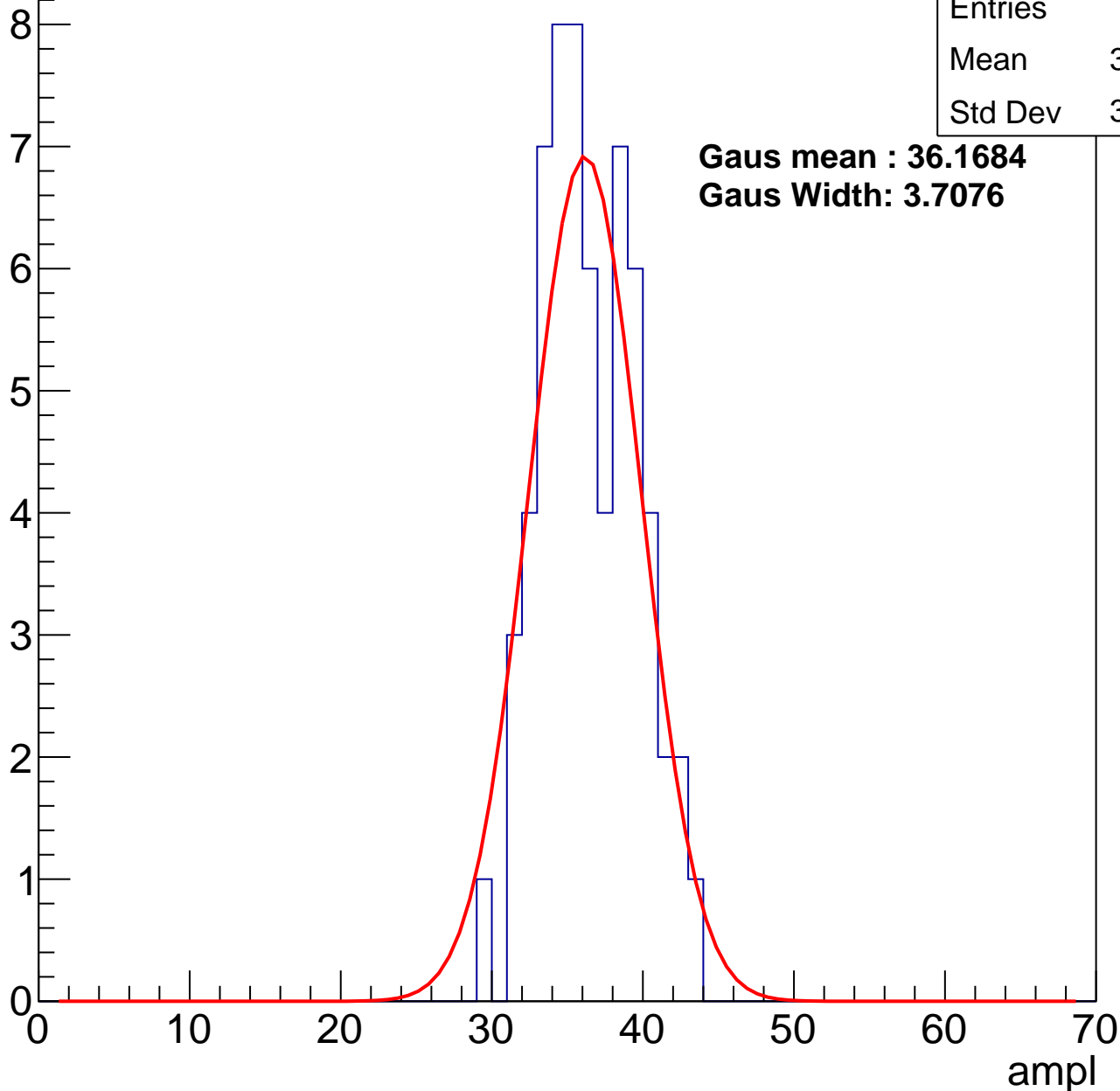
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	63
Mean	35.97
Std Dev	3.117

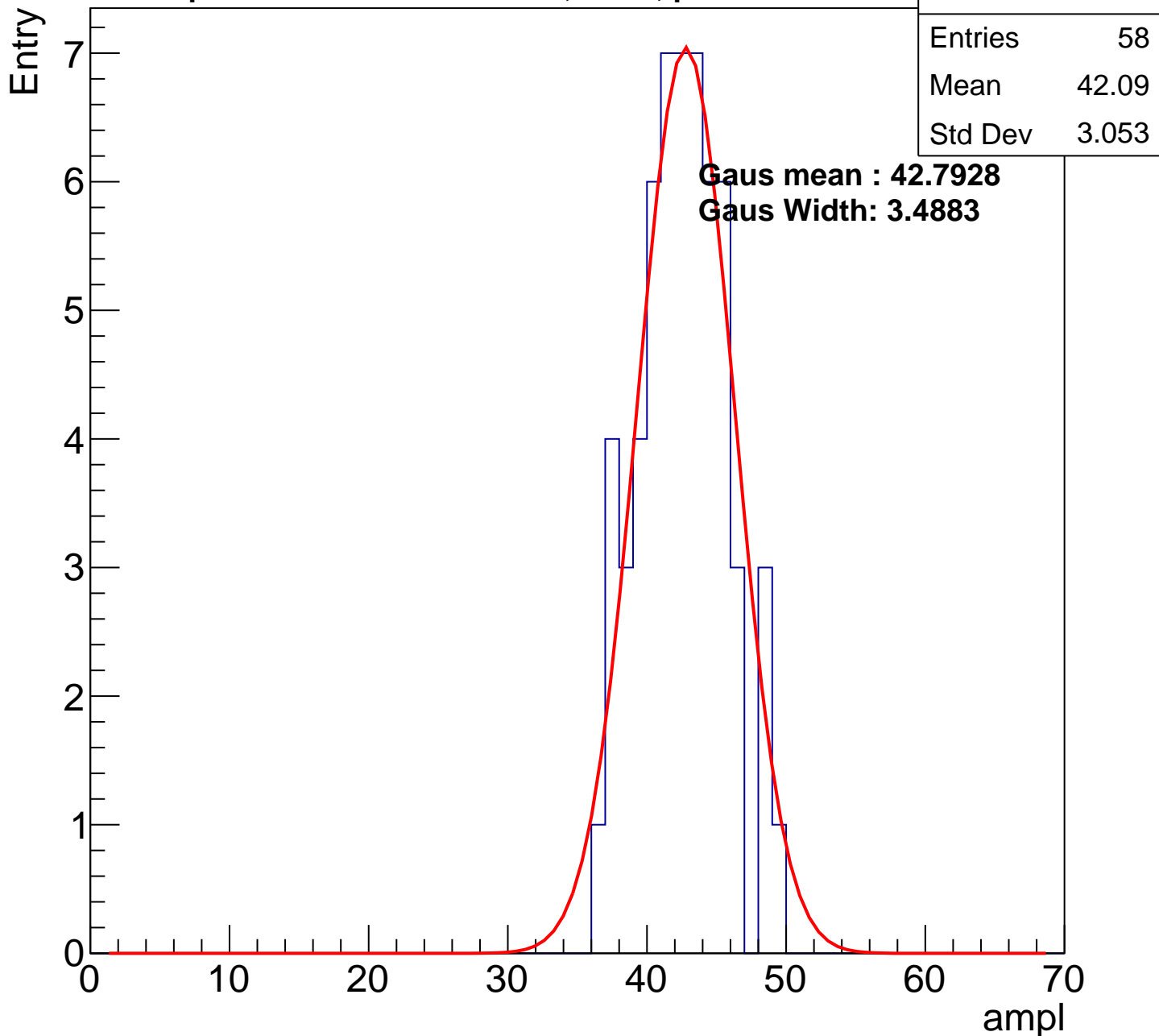
**Gaus mean : 36.1684**

**Gaus Width: 3.7076**



# B1L100S, U6-ch48, adc2

calib\_packv5\_042523\_0143.root, FC#4, port A2



# B1L100S, U6-ch48, adc3

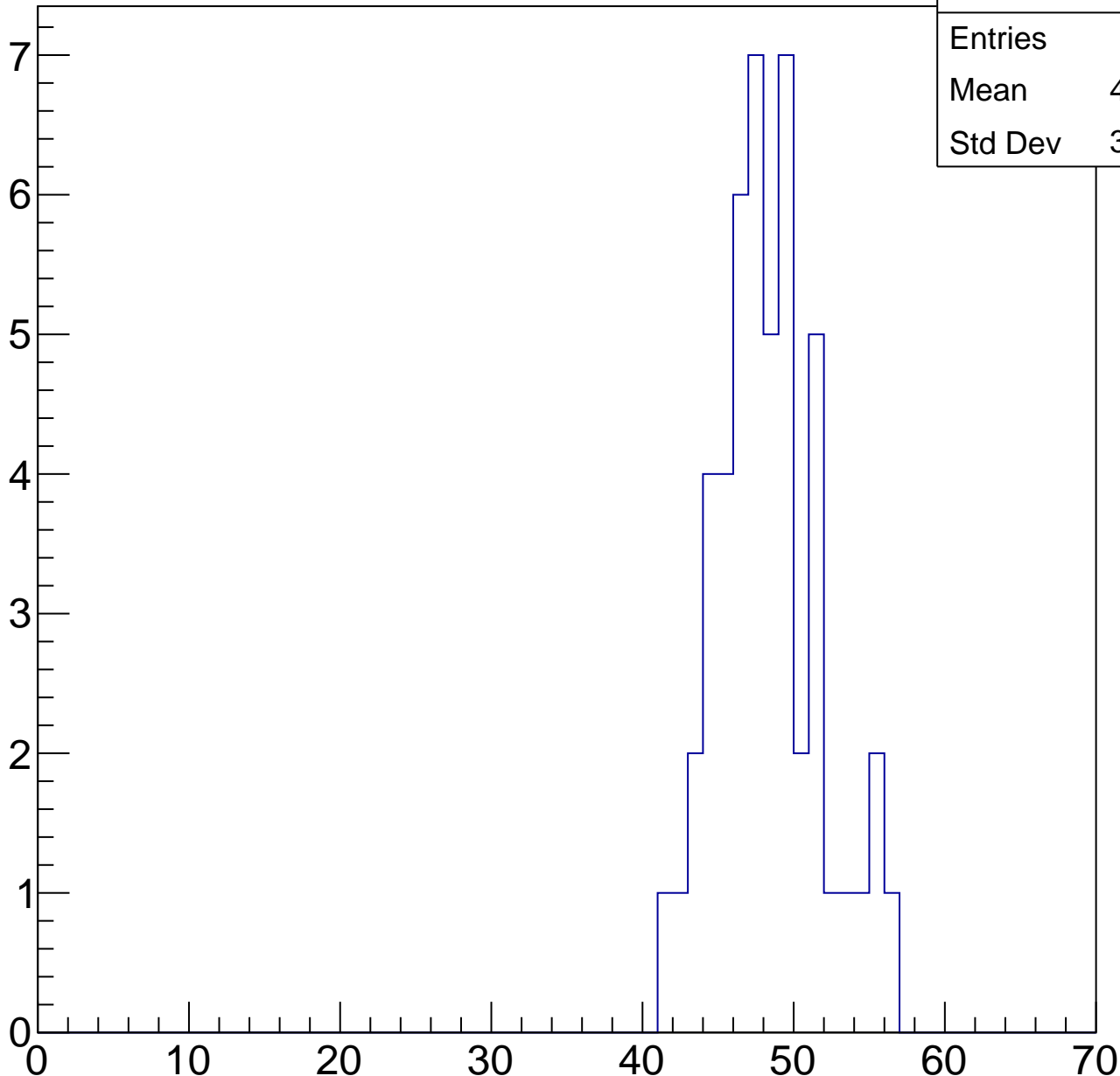
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

7  
6  
5  
4  
3  
2  
1  
0

Entries	50
Mean	47.86
Std Dev	3.359

ampl

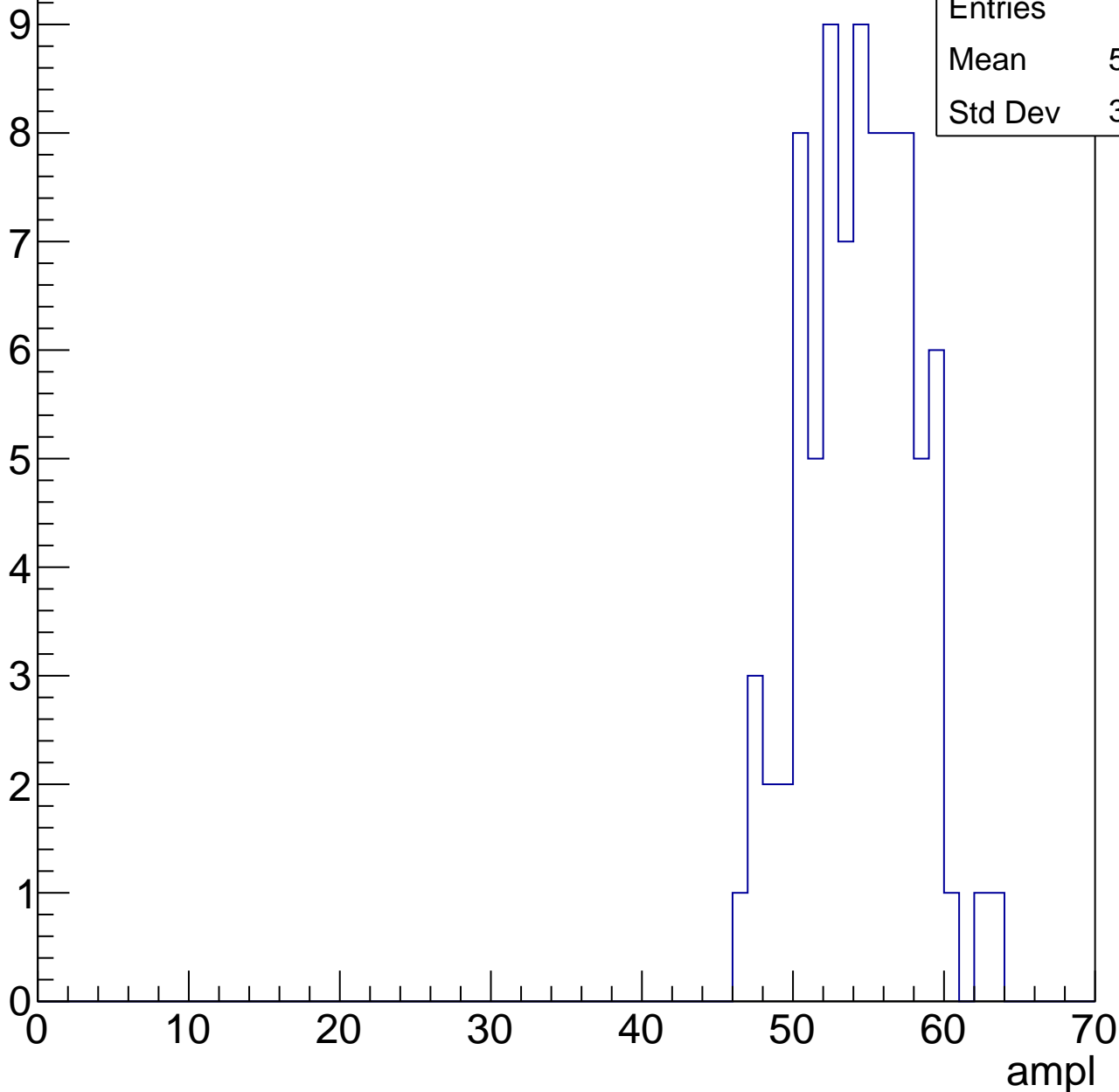


# B1L100S, U6-ch48, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

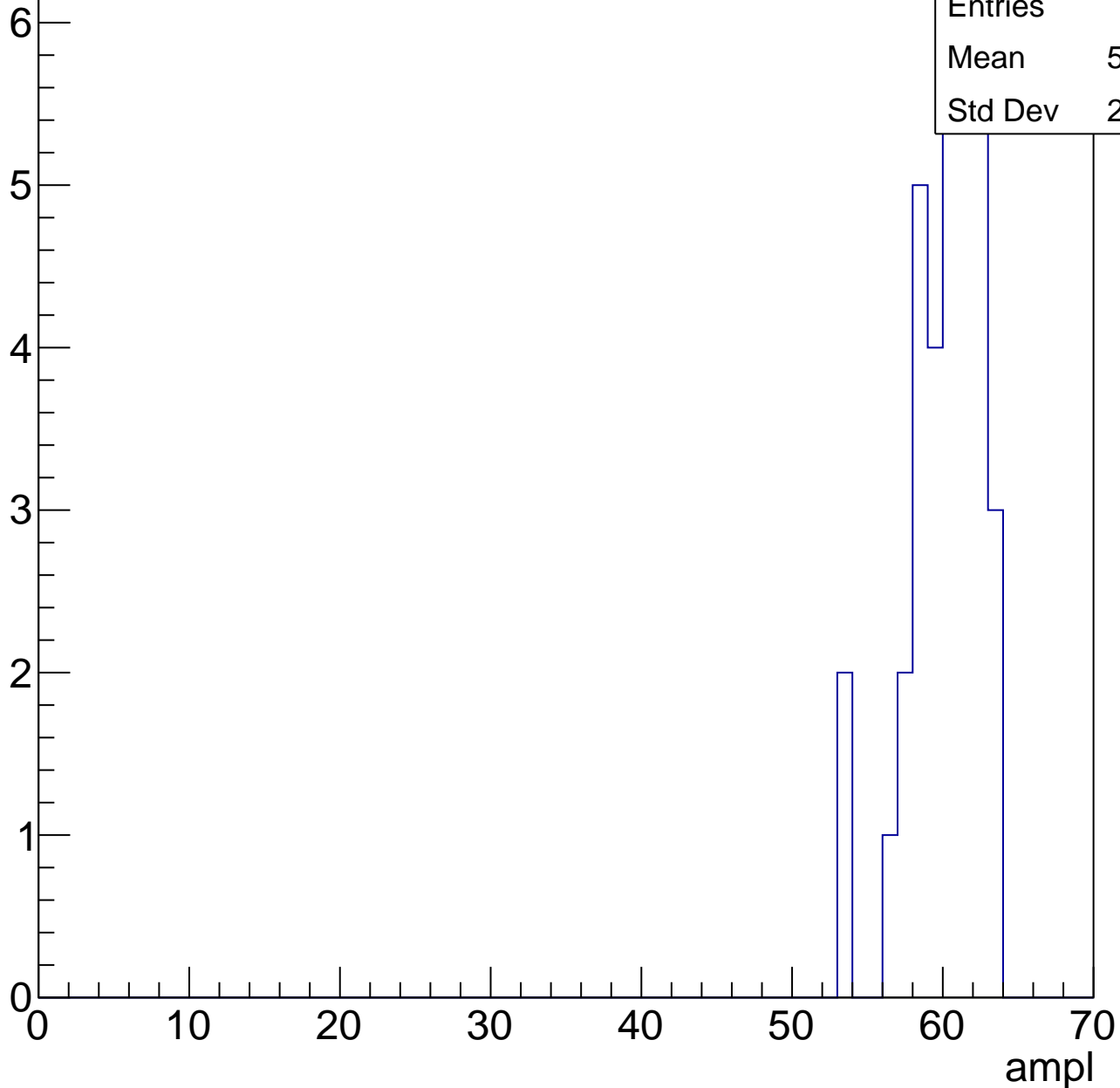
Entries	84
Mean	53.98
Std Dev	3.572



# B1L100S, U6-ch48, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

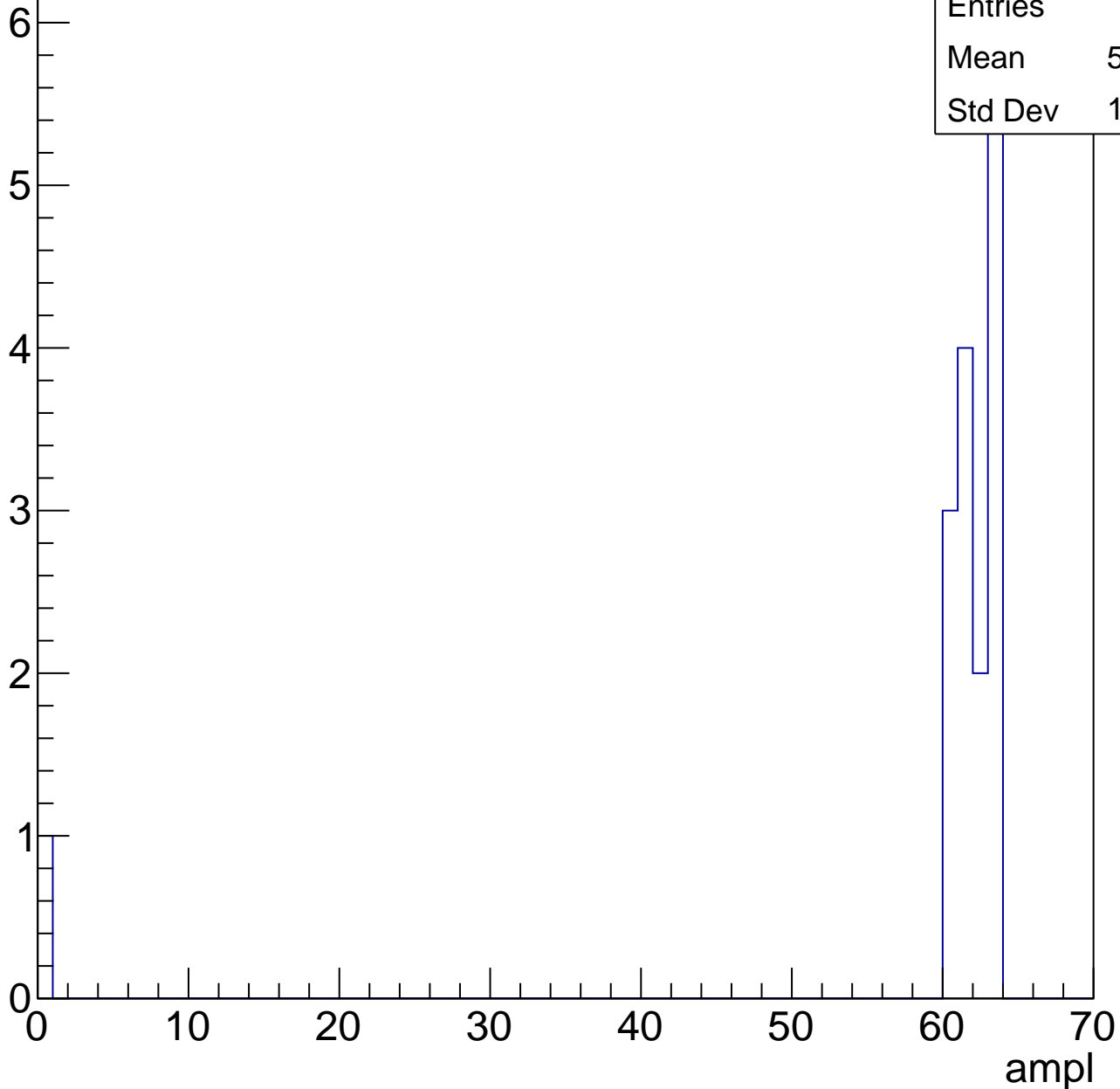


# B1L100S, U6-ch48, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	16
Mean	57.88
Std Dev	14.99

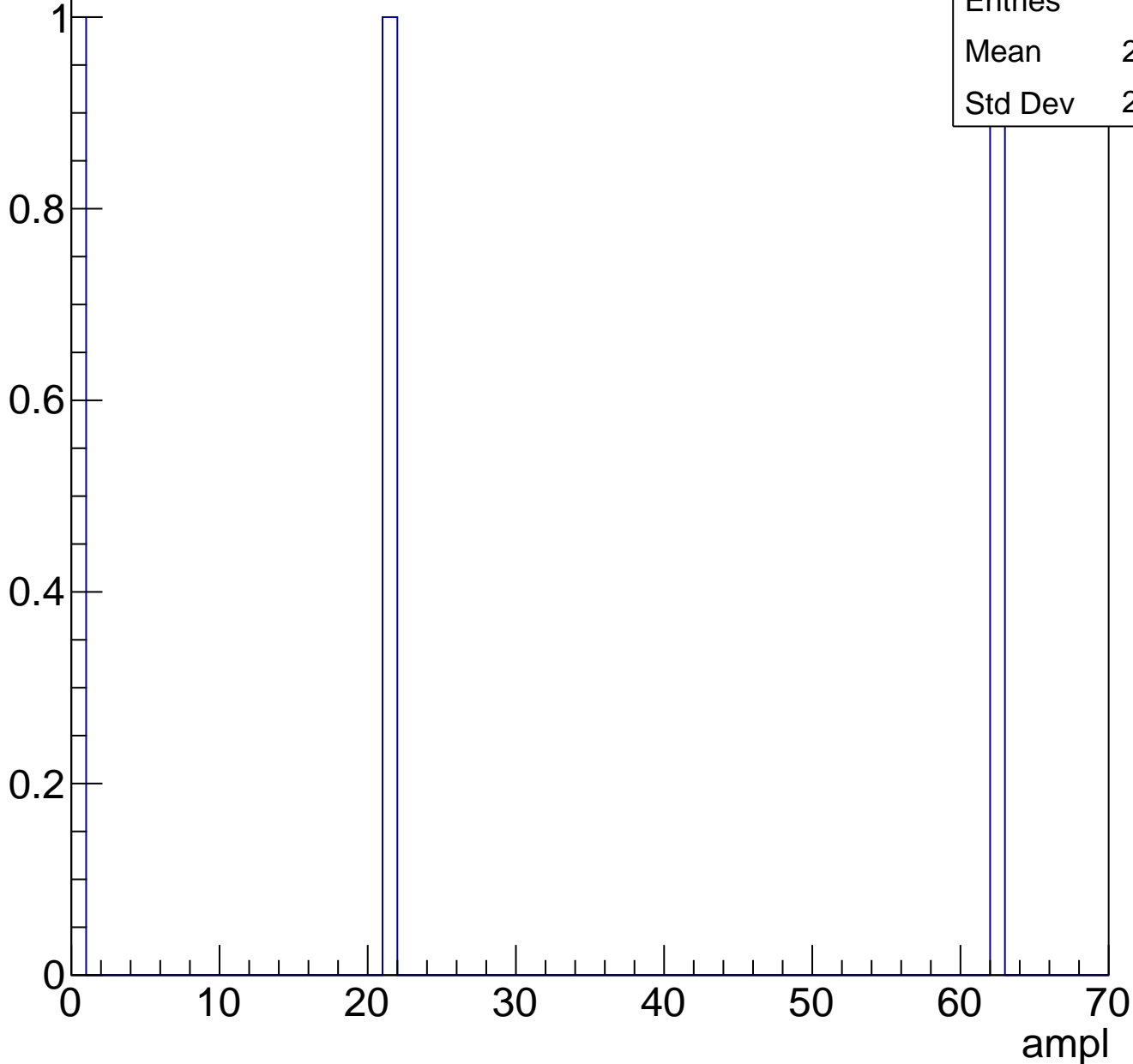




# B1L100S, U6-ch48, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	3
Mean	27.67
Std Dev	25.75

# B1L100S, U6-ch49, adc0

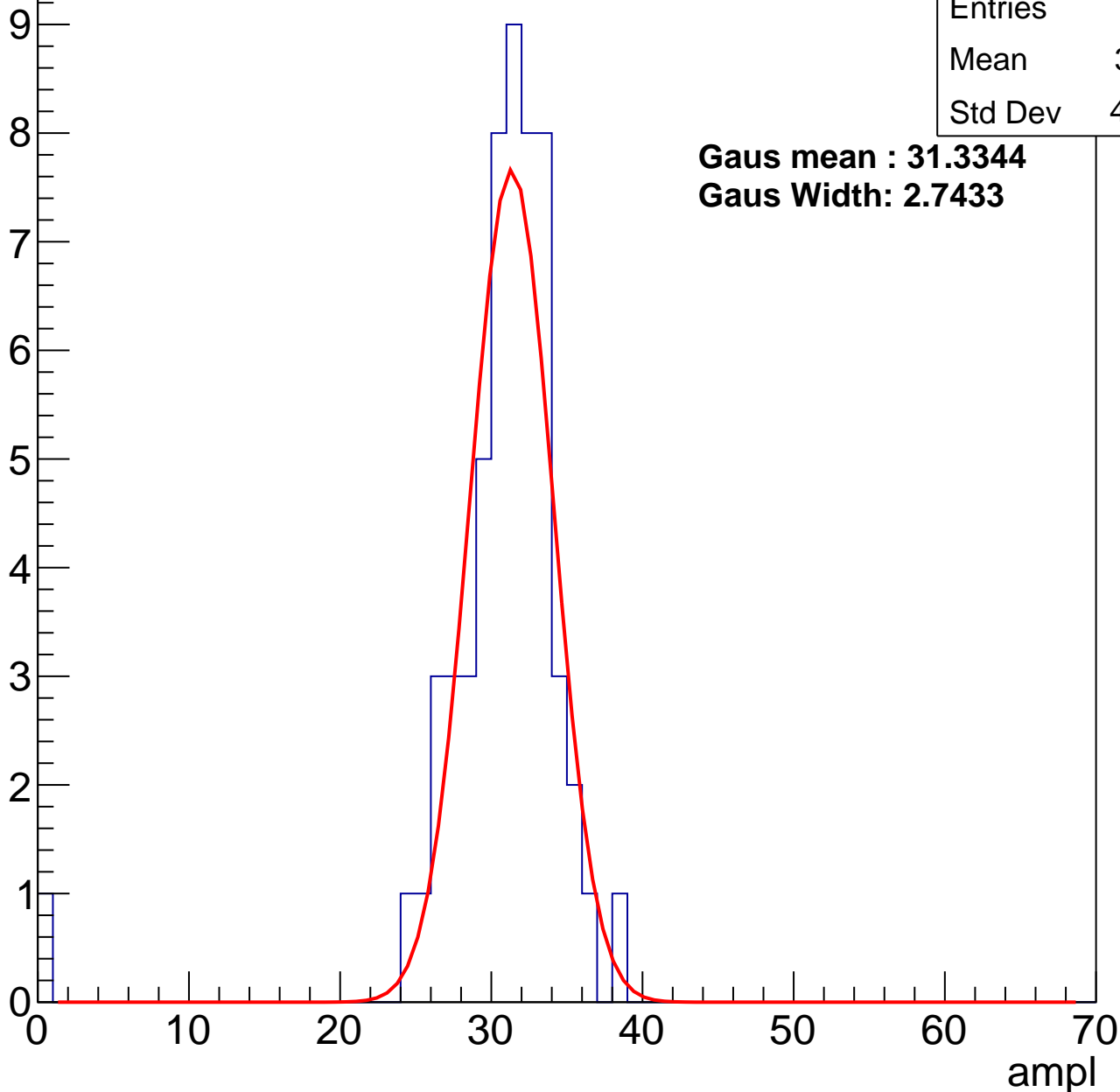
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	57
Mean	30.21
Std Dev	4.887

**Gaus mean : 31.3344**

**Gaus Width: 2.7433**



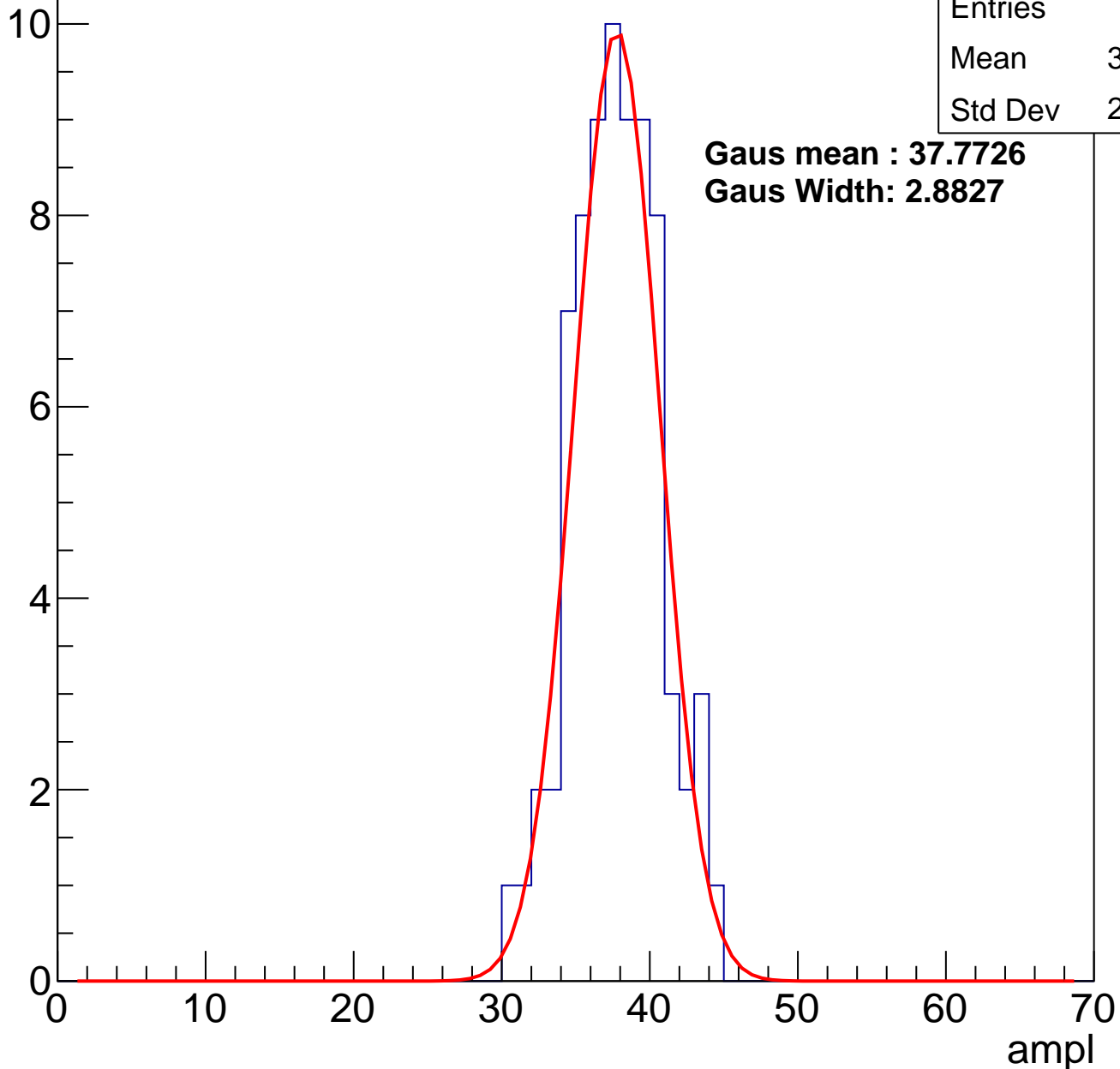
# B1L100S, U6-ch49, adc1

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	75
Mean	37.28
Std Dev	2.915

**Gaus mean : 37.7726**  
**Gaus Width: 2.8827**

Entry



# B1L100S, U6-ch49, adc2

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	67
Mean	44.81
Std Dev	3.173

**Gaus mean : 45.0242**

**Gaus Width: 3.0238**

Entry

10

8

6

4

2

0

0

10

20

30

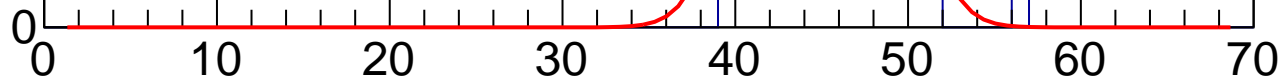
40

50

60

70

ampl

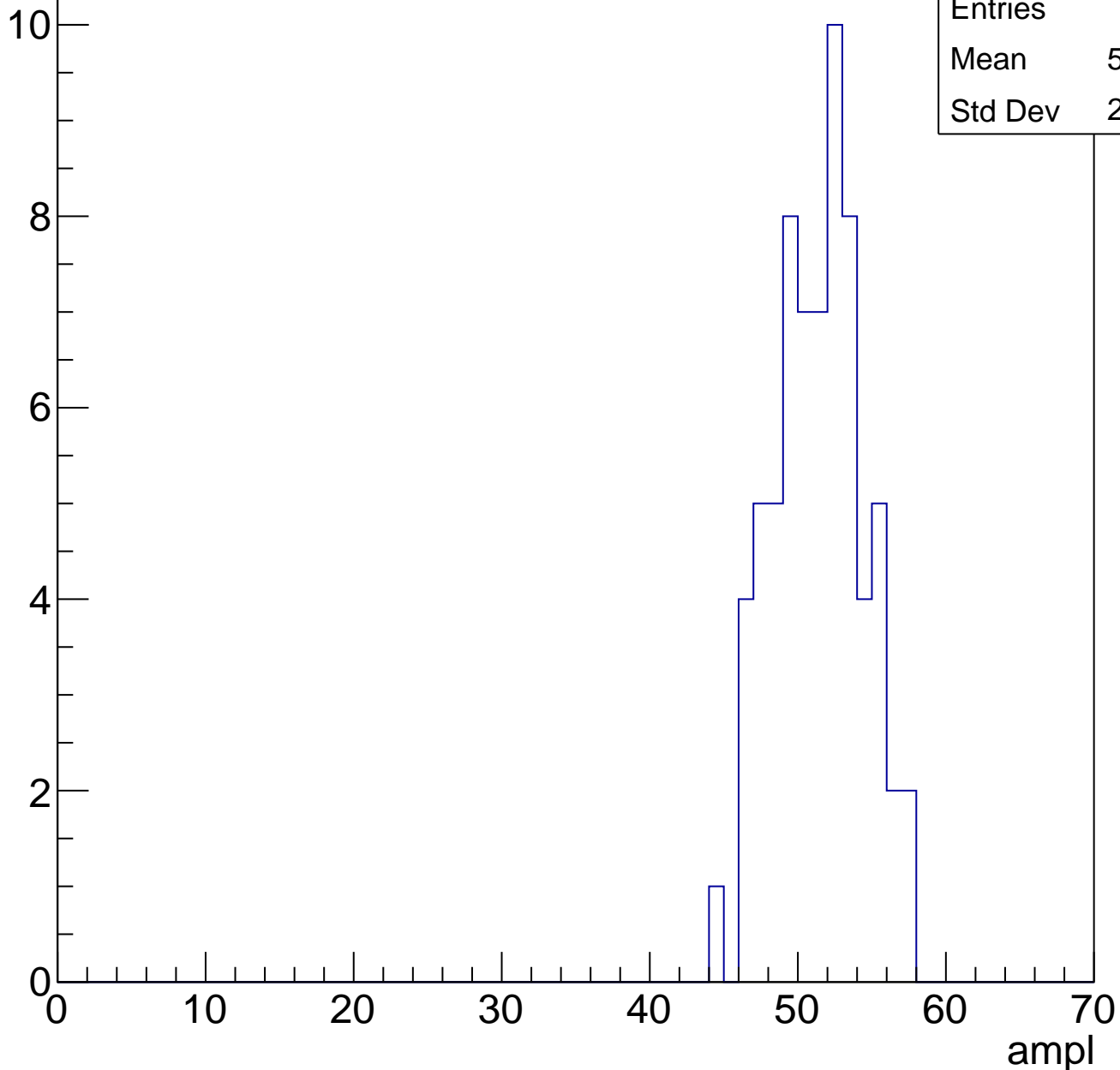


# B1L100S, U6-ch49, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	68
Mean	50.93
Std Dev	2.952

Entry

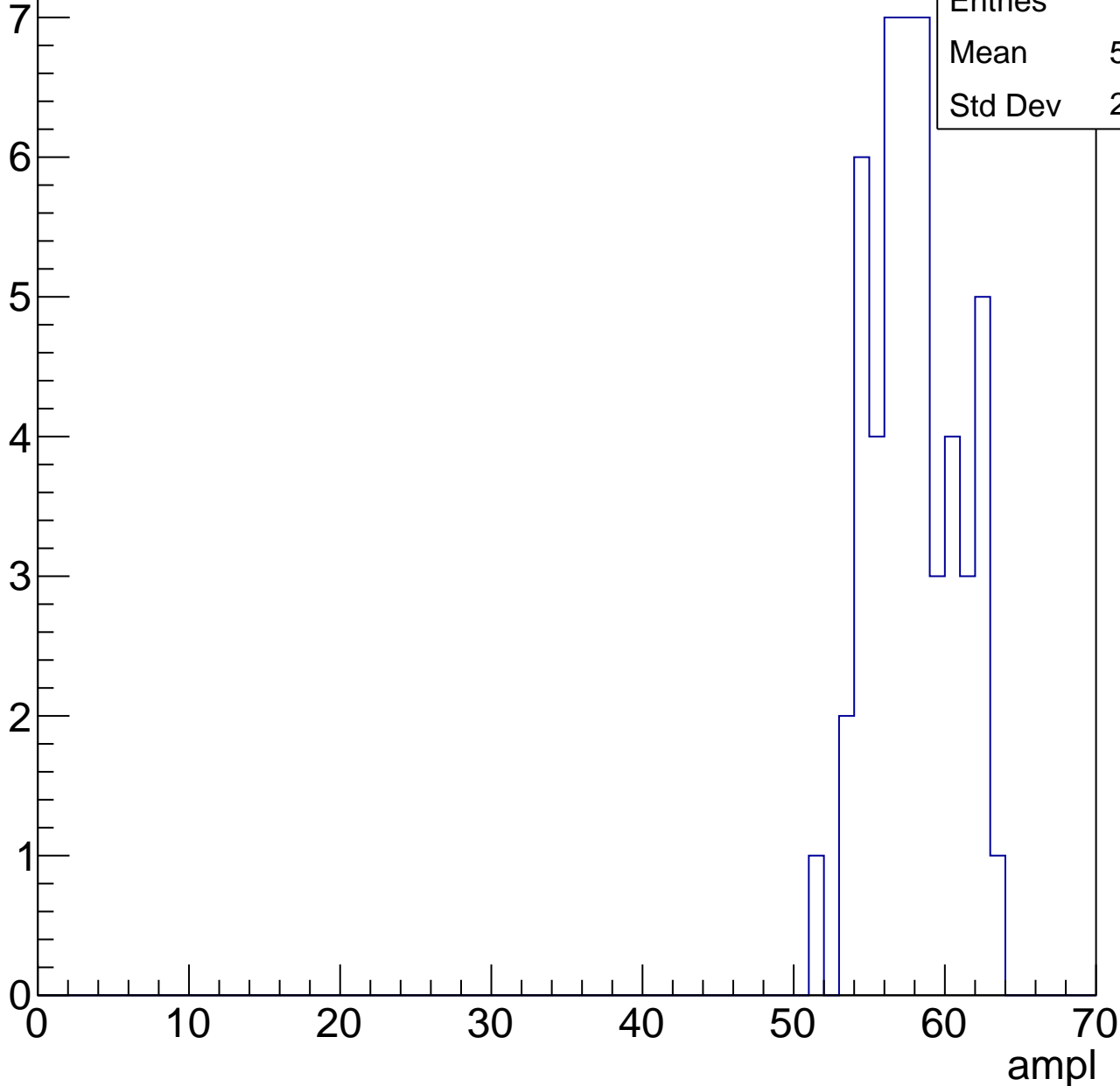


# B1L100S, U6-ch49, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

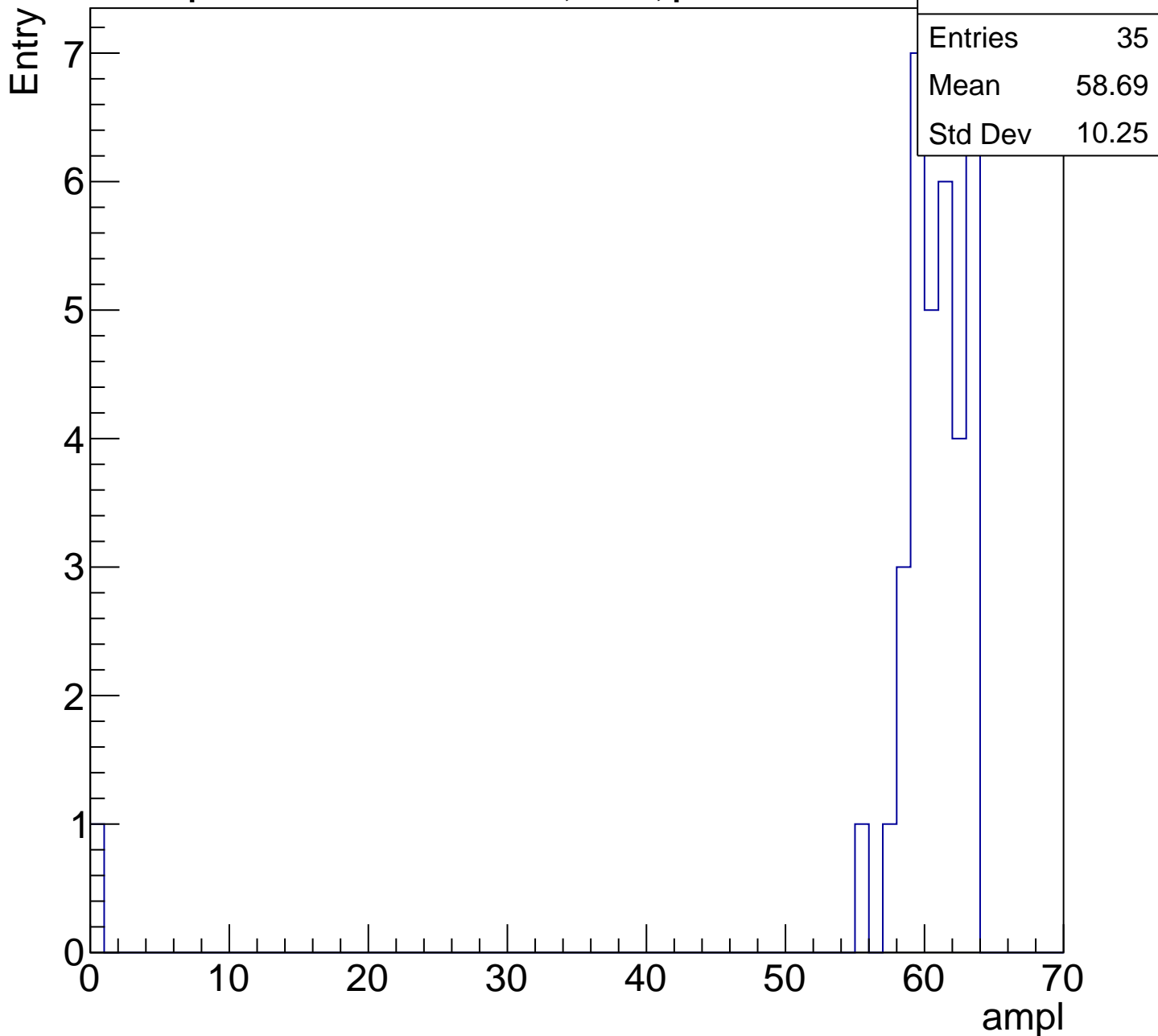
Entry

Entries	50
Mean	57.42
Std Dev	2.829



# B1L100S, U6-ch49, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2



# B1L100S, U6-ch49, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

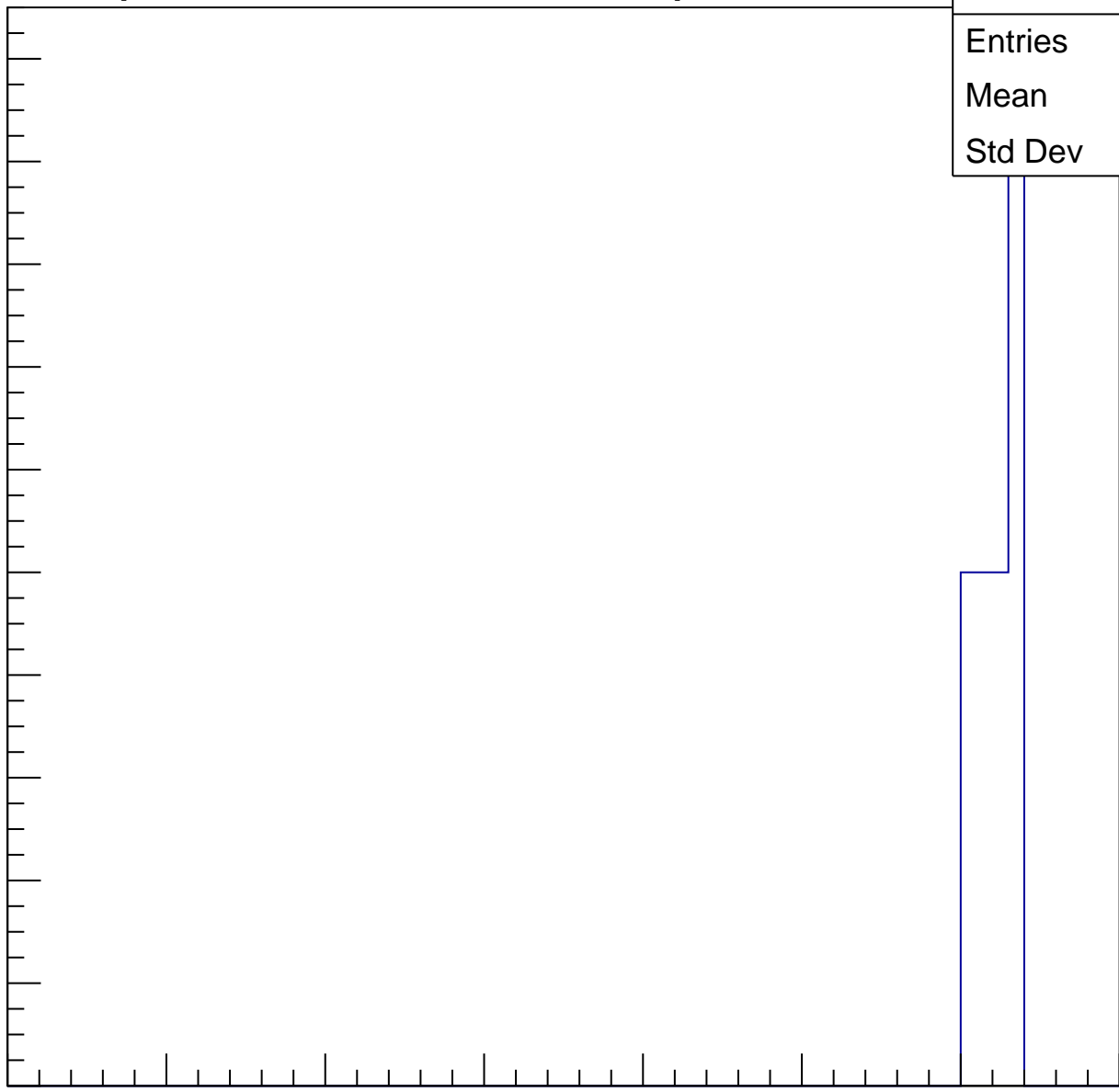
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	5
Mean	61.8
Std Dev	1.166

ampl

0 10 20 30 40 50 60 70





# B1L100S, U6-ch49, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L100S, U6-ch50, adc0

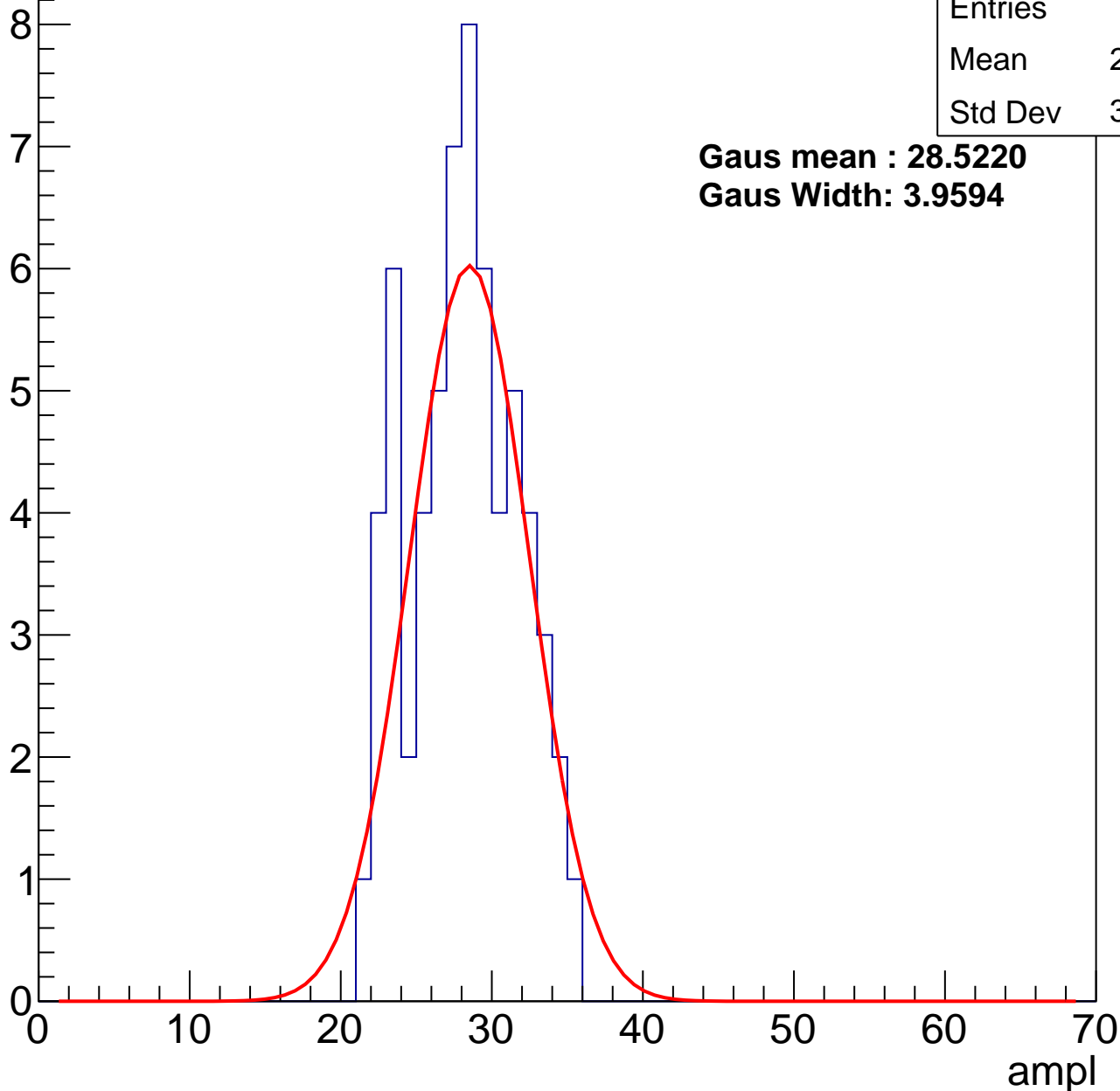
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	62
Mean	27.69
Std Dev	3.499

**Gaus mean : 28.5220**

**Gaus Width: 3.9594**



# B1L100S, U6-ch50, adc1

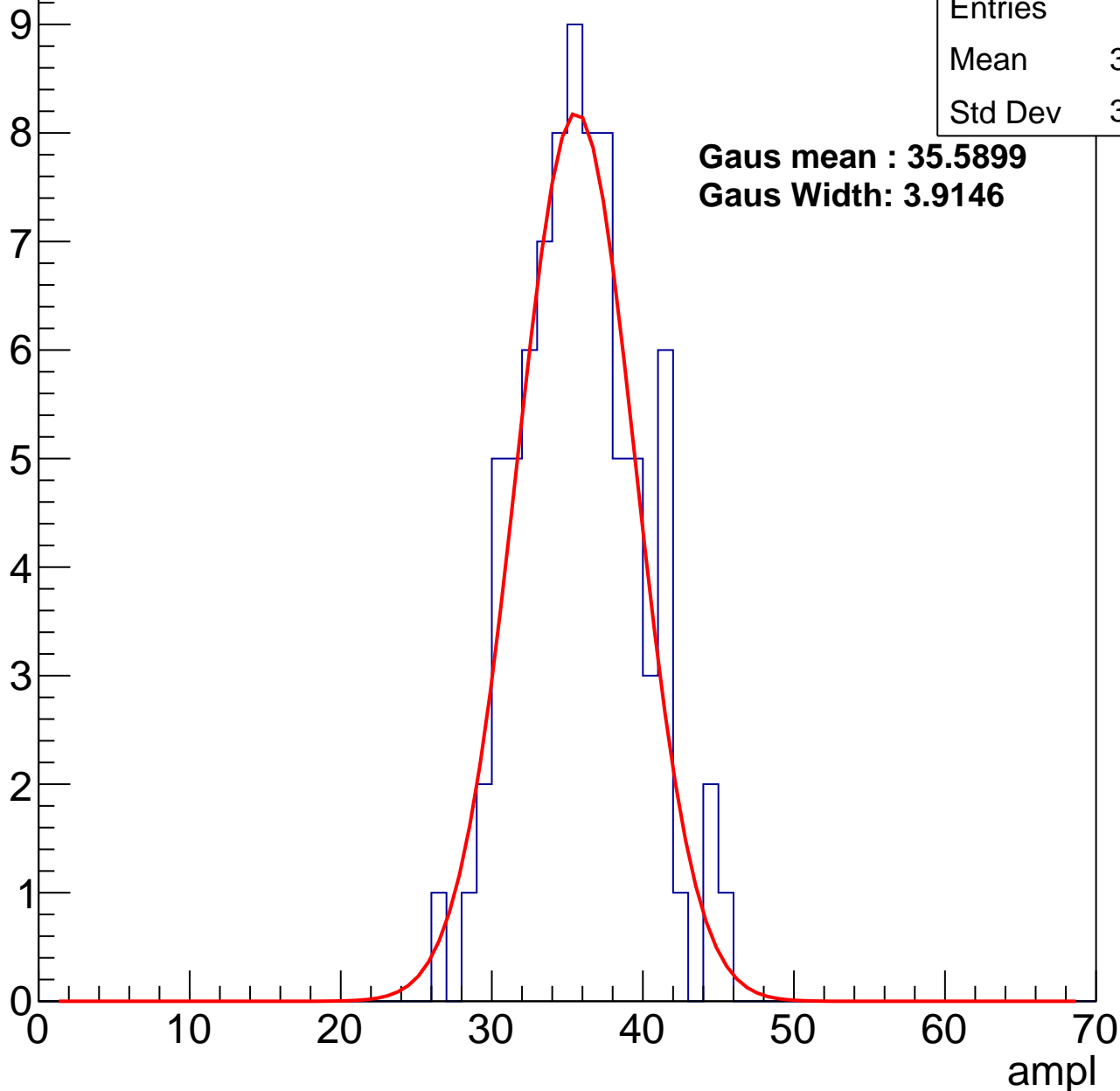
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	83
Mean	35.39
Std Dev	3.883

**Gaus mean : 35.5899**

**Gaus Width: 3.9146**



# B1L100S, U6-ch50, adc2

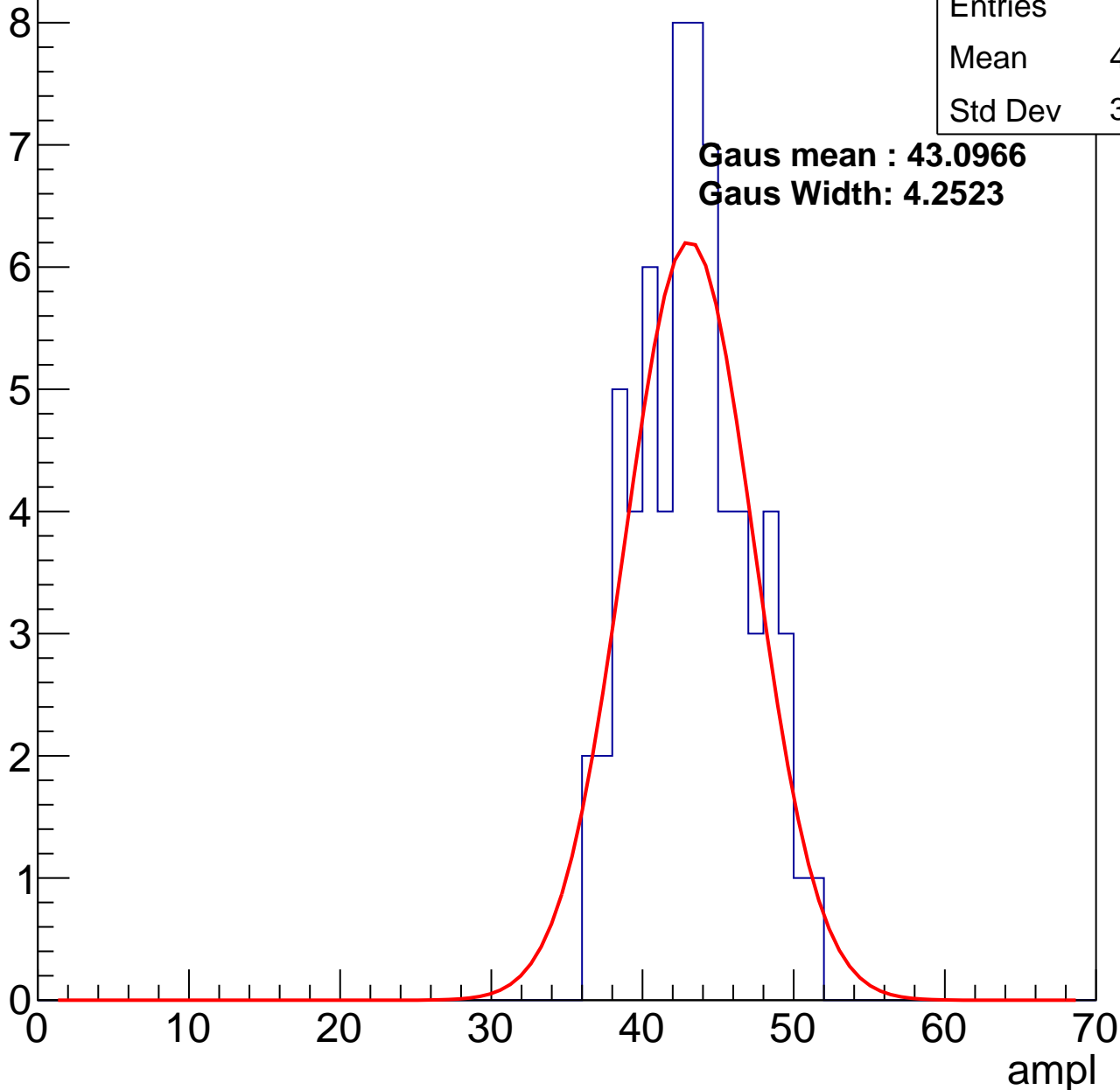
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	66
Mean	42.86
Std Dev	3.618

**Gaus mean : 43.0966**

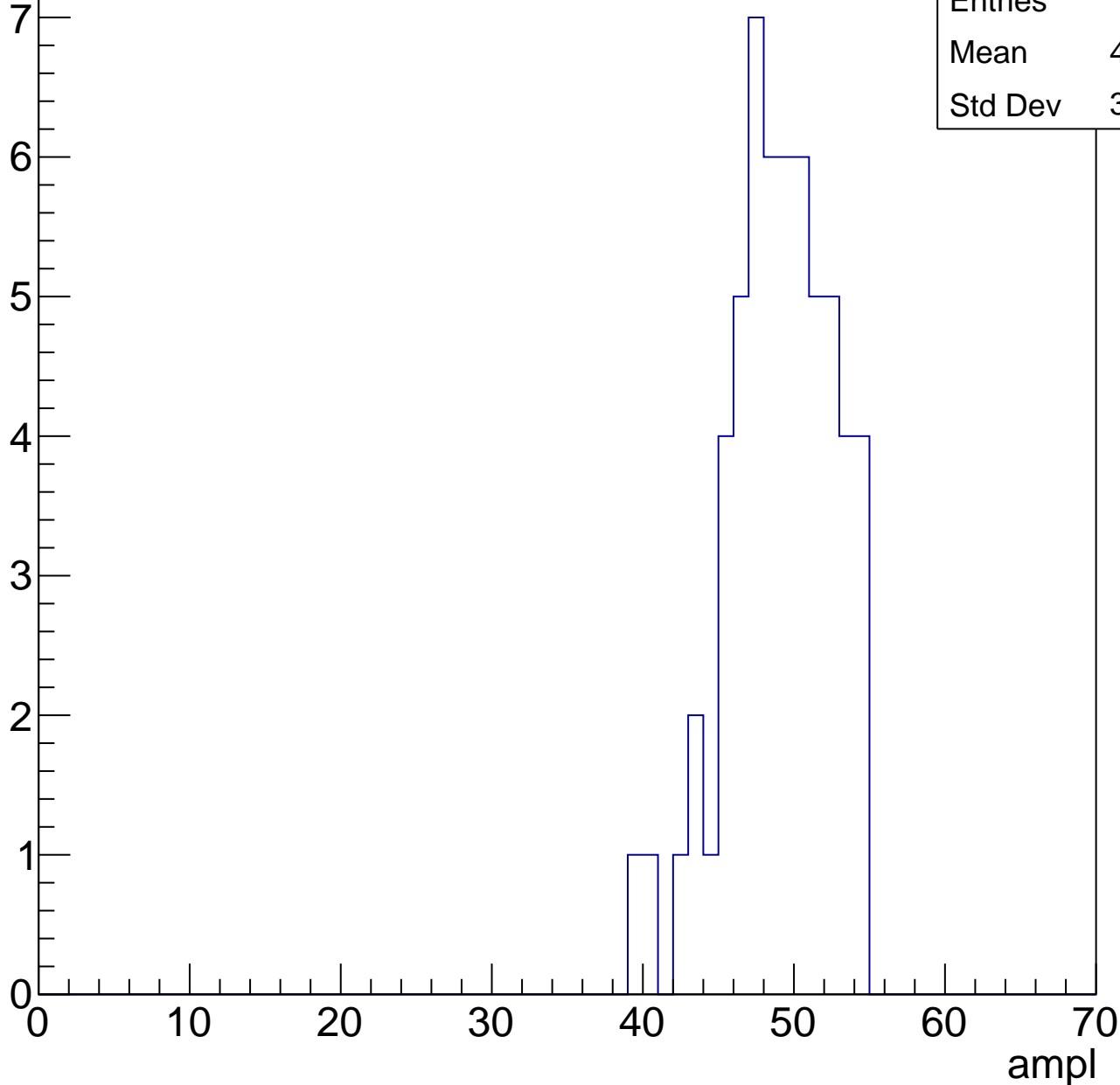
**Gaus Width: 4.2523**



# B1L100S, U6-ch50, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

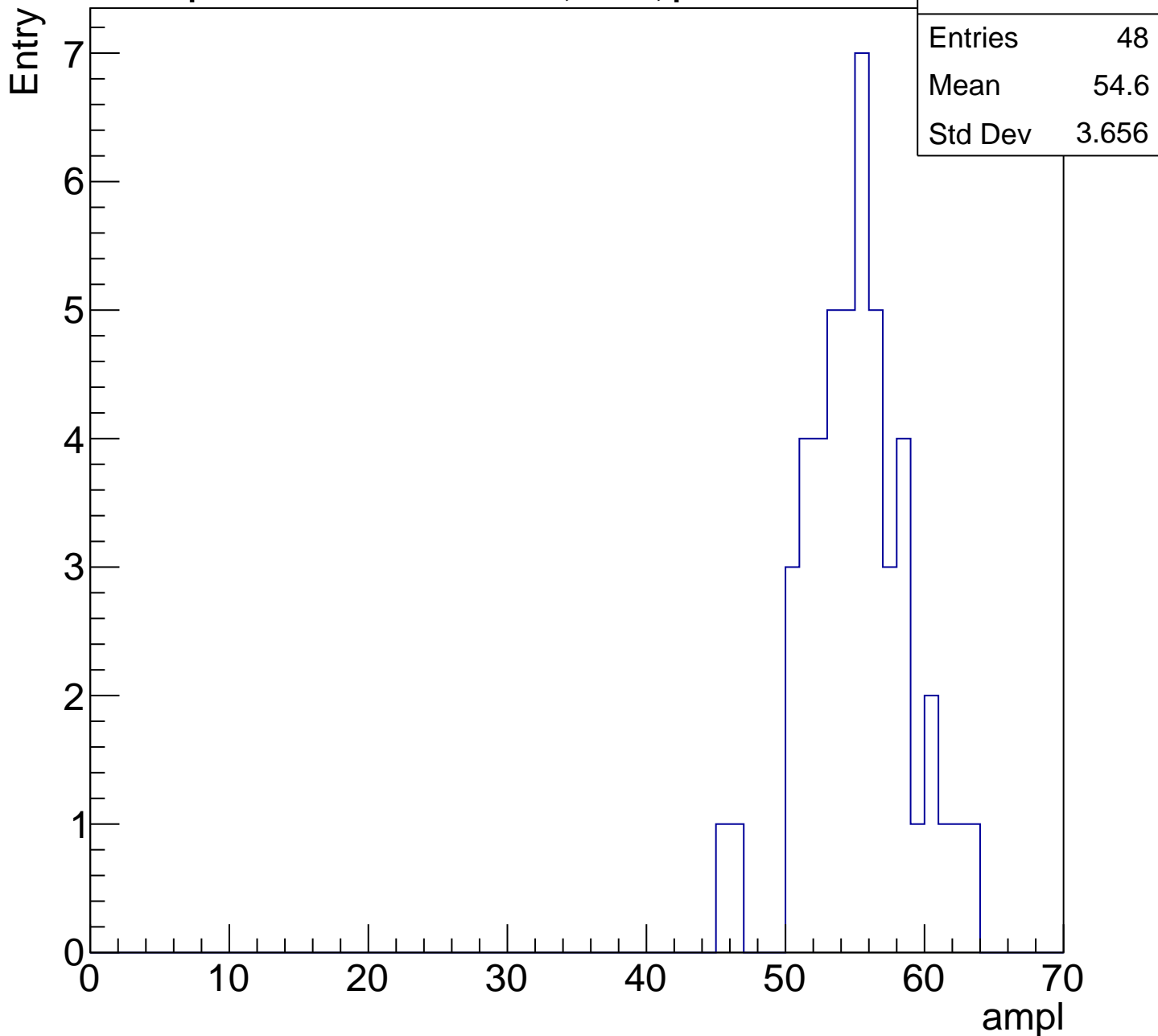
Entry



Entries	58
Mean	48.53
Std Dev	3.455

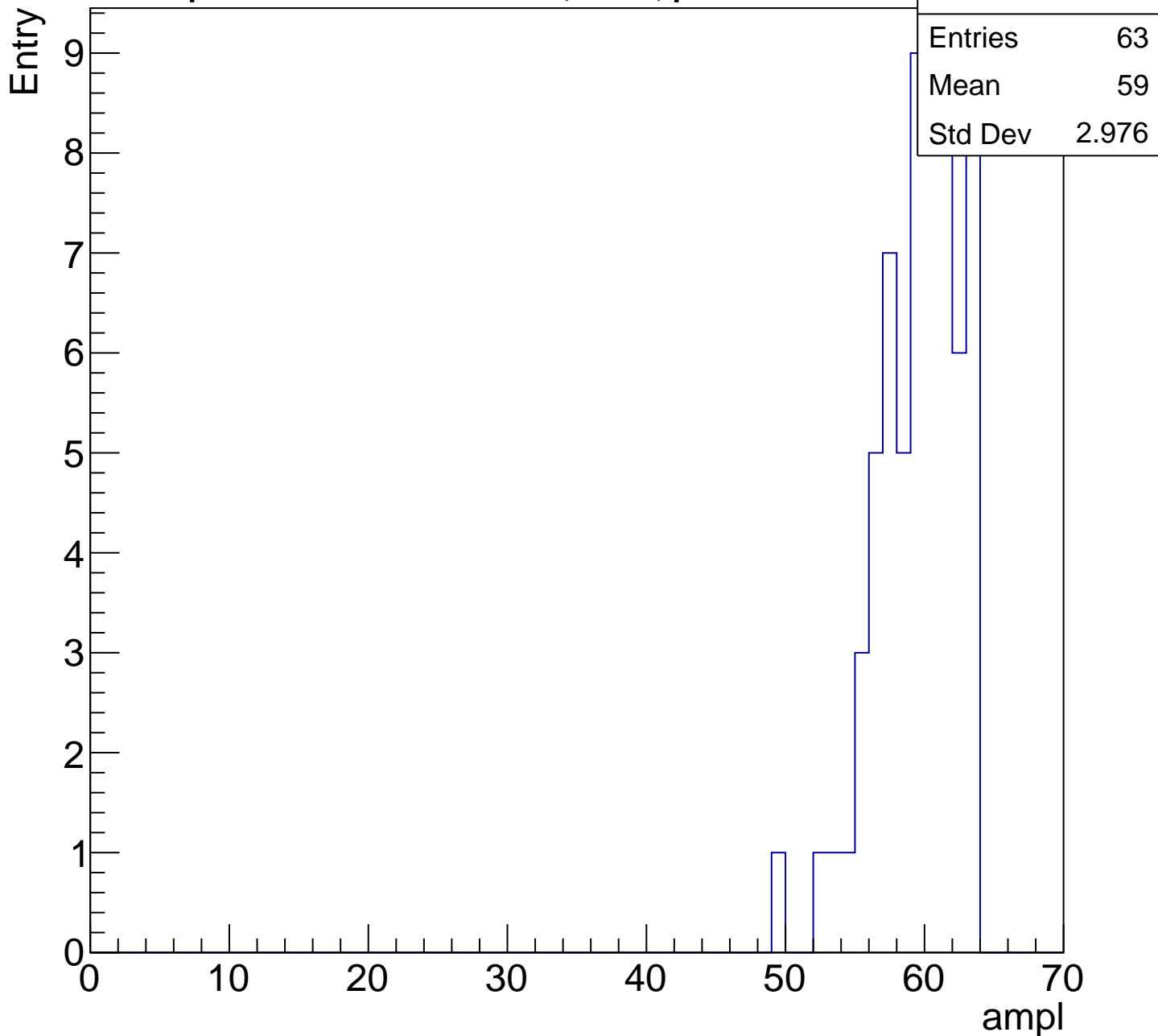
# B1L100S, U6-ch50, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2



# B1L100S, U6-ch50, adc5

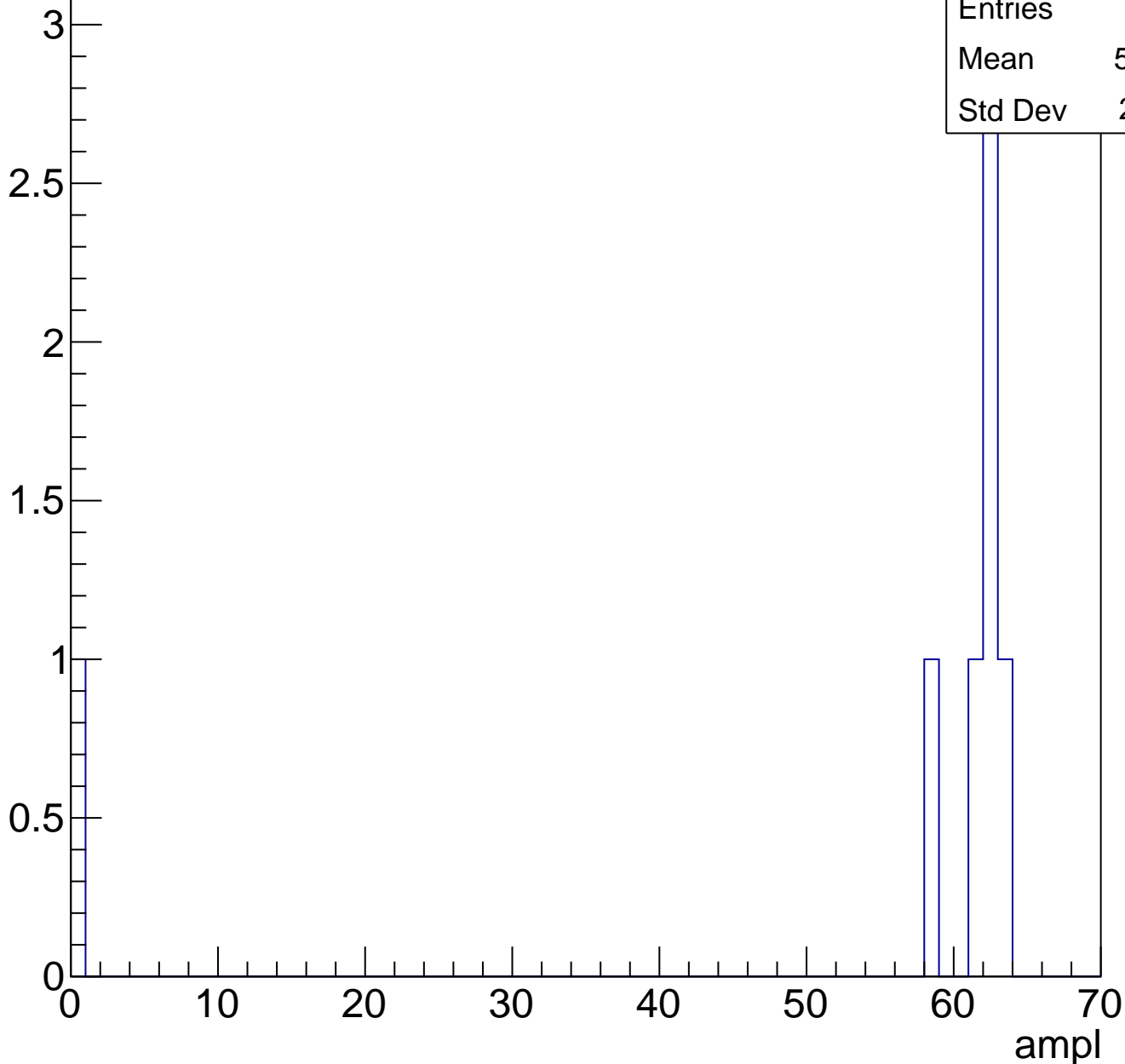
calib\_packv5\_042523\_0143.root, FC#4, port A2



# B1L100S, U6-ch50, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry





# B1L100S, U6-ch50, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L100S, U6-ch51, adc0

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	84
Mean	29.76
Std Dev	3.085

**Gaus mean : 30.3190**

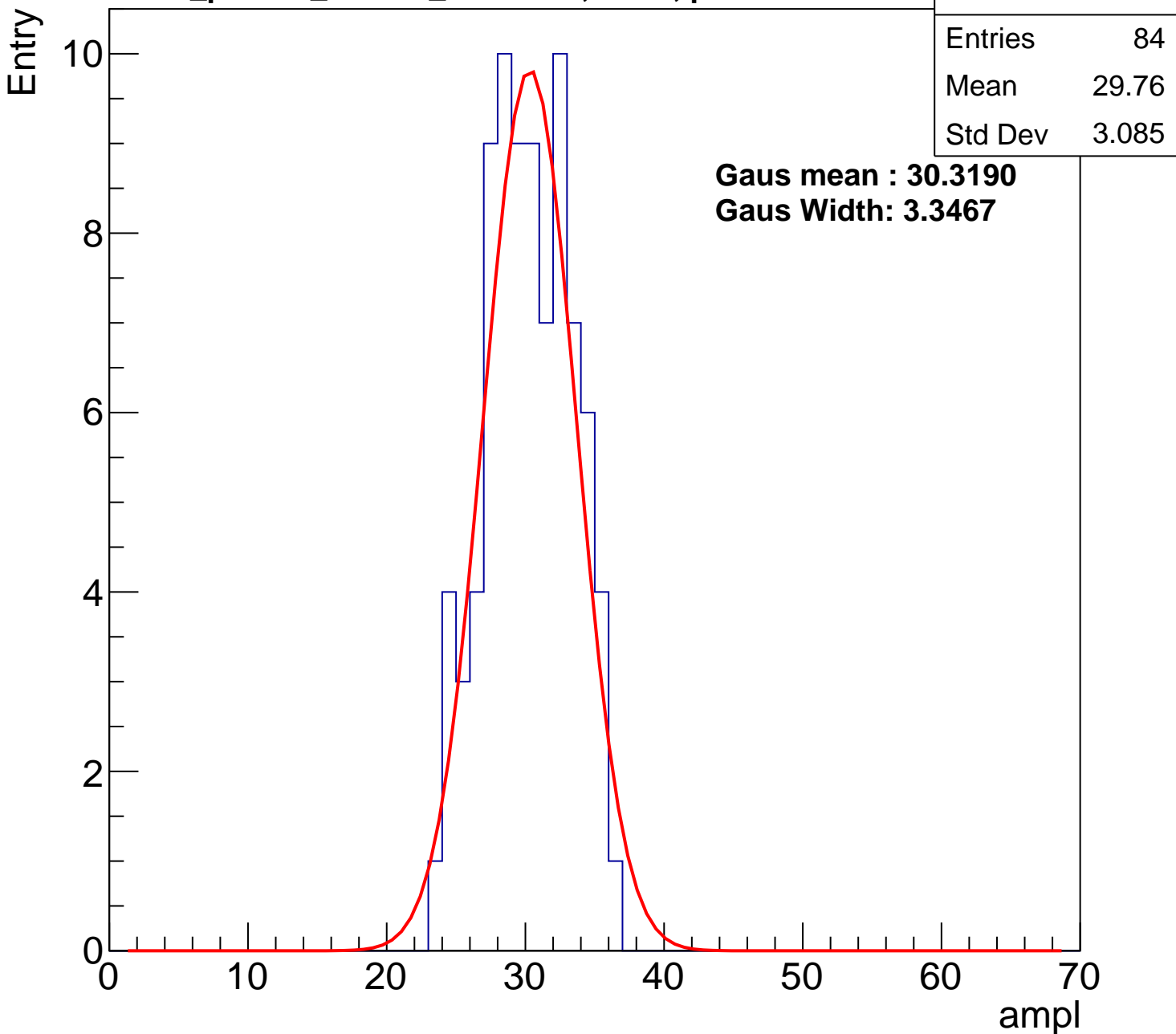
**Gaus Width: 3.3467**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L100S, U6-ch51, adc1

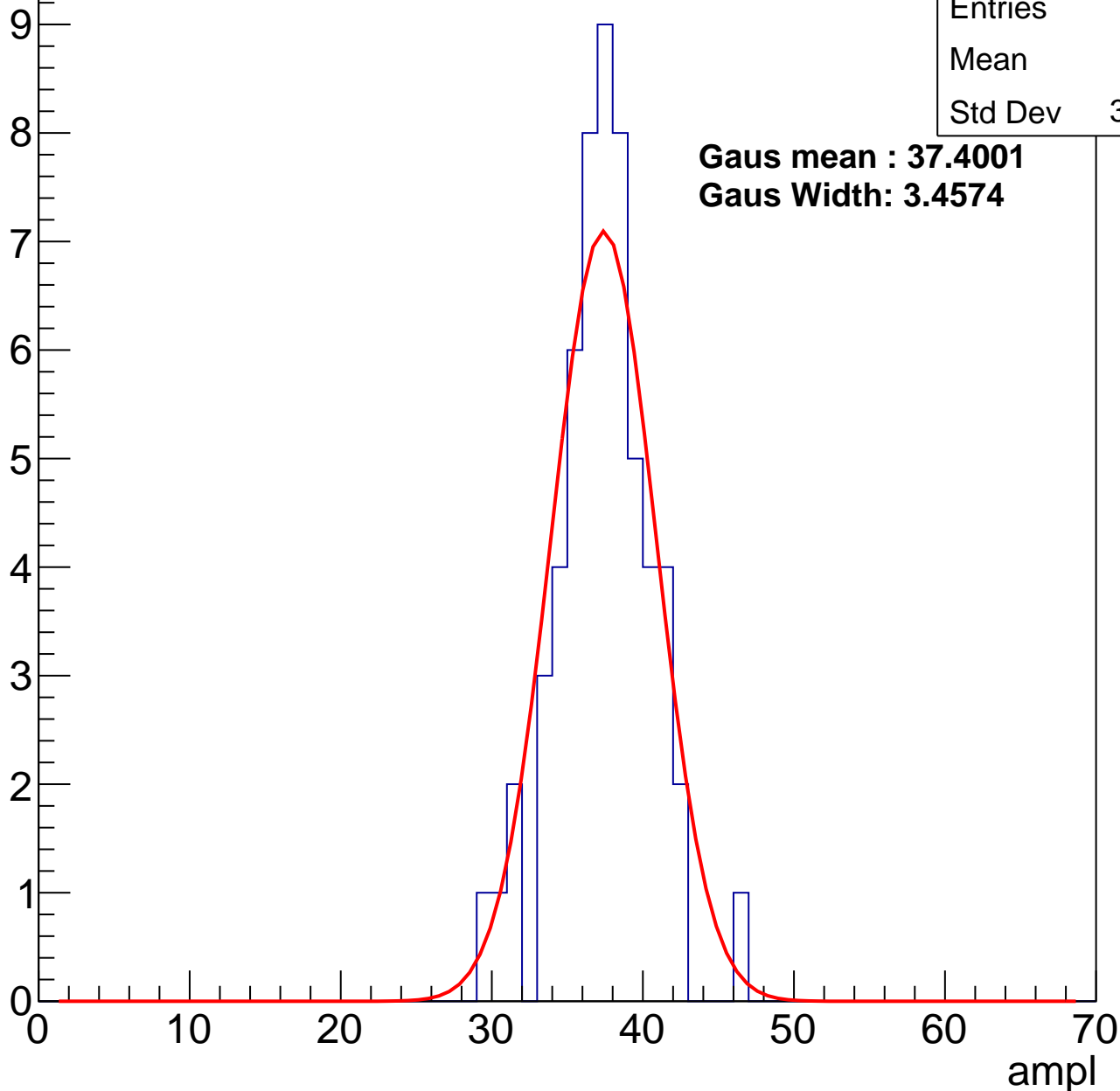
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	58
Mean	36.9
Std Dev	3.106

**Gaus mean : 37.4001**

**Gaus Width: 3.4574**



# B1L100S, U6-ch51, adc2

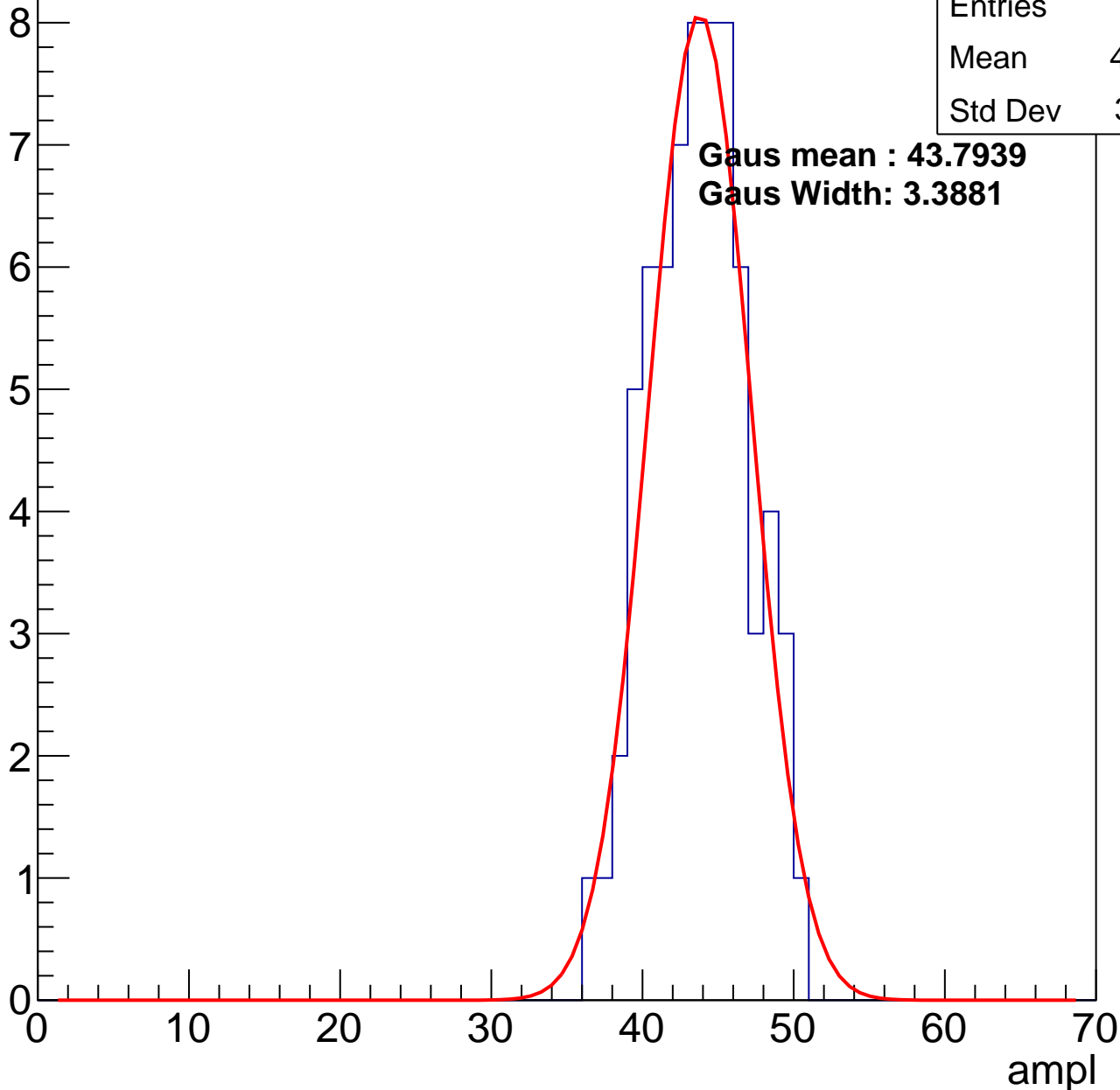
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	69
Mean	43.28
Std Dev	3.171

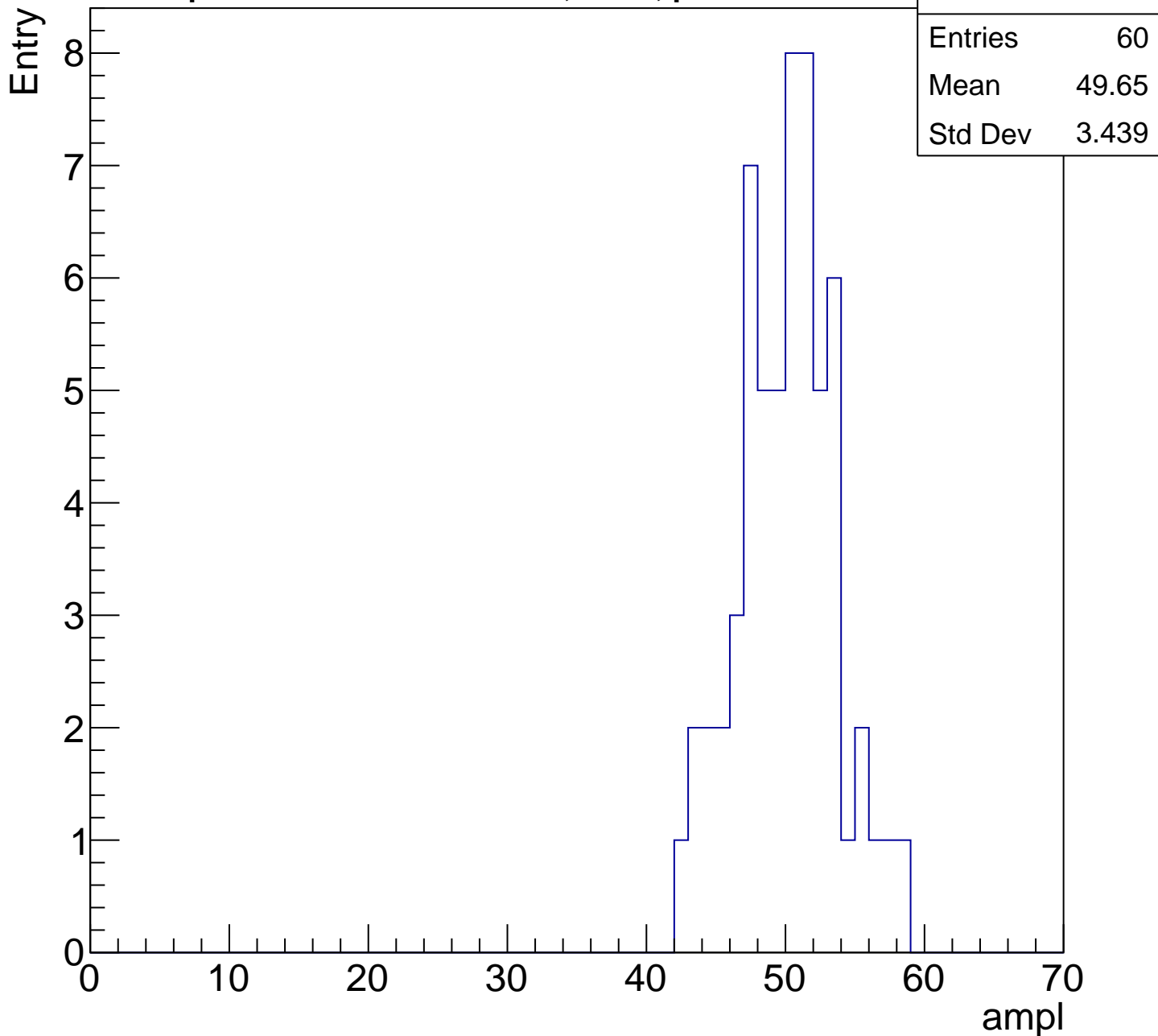
**Gaus mean : 43.7939**

**Gaus Width: 3.3881**



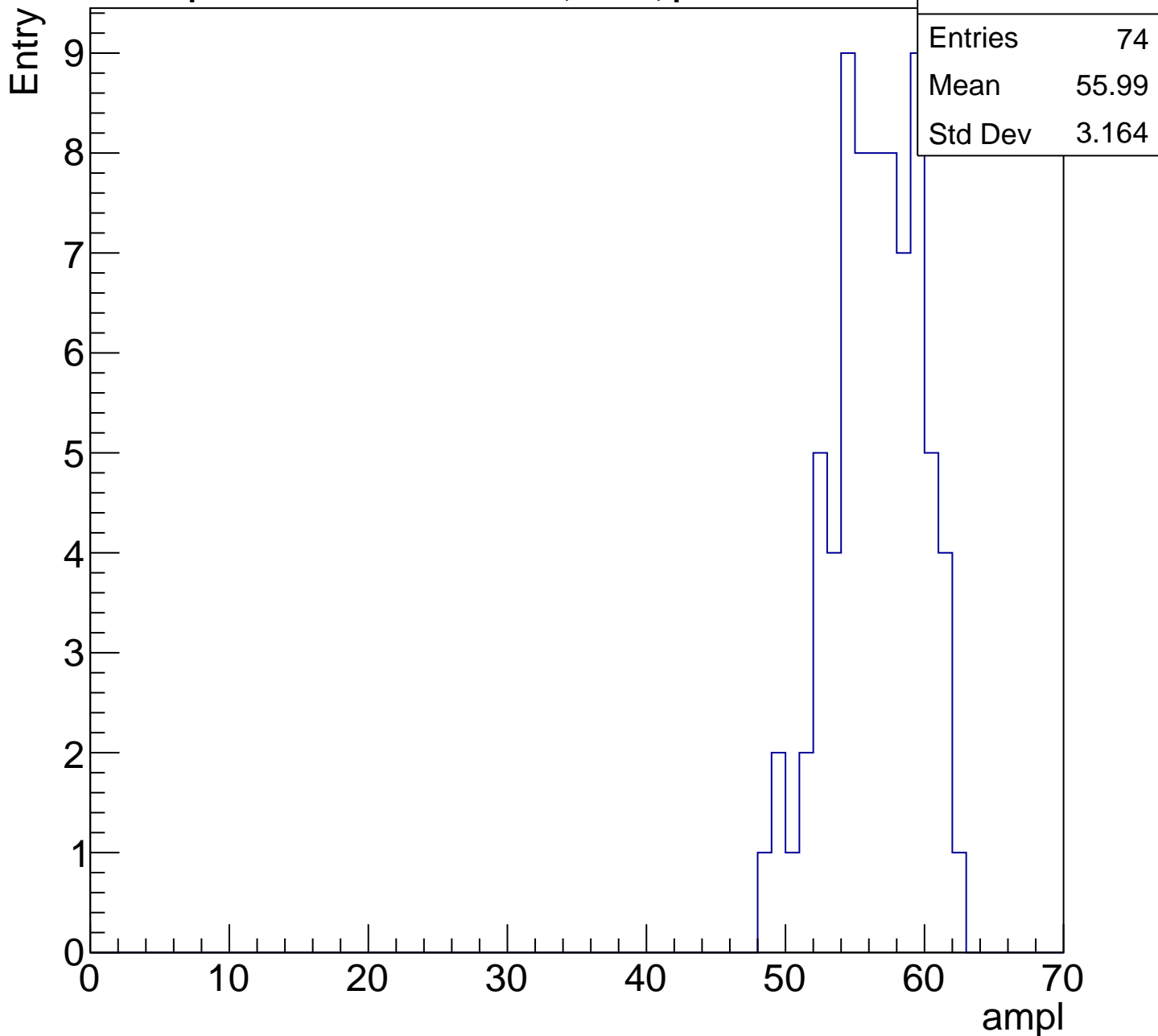
# B1L100S, U6-ch51, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2



# B1L100S, U6-ch51, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

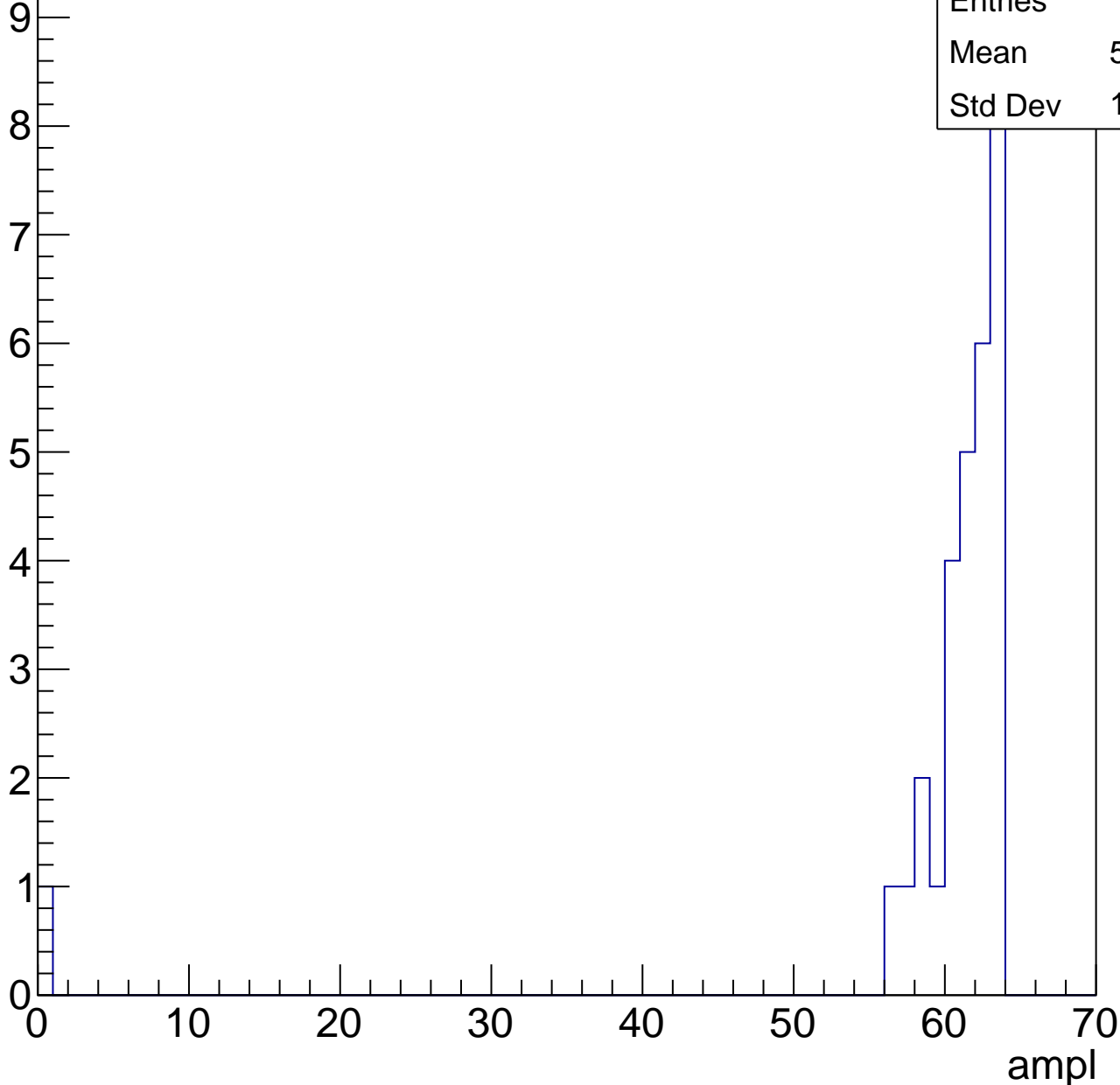


# B1L100S, U6-ch51, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

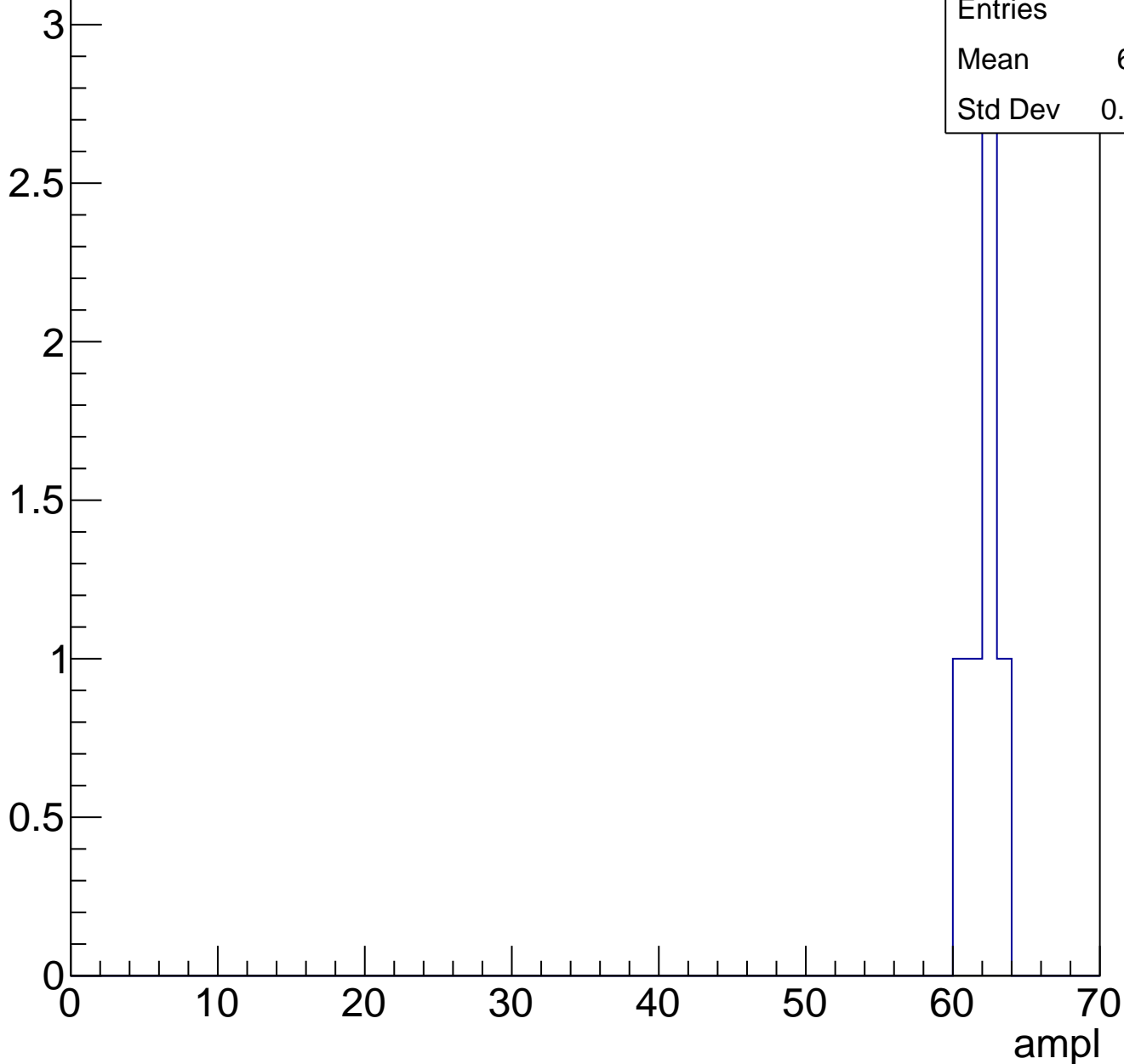
Entries	30
Mean	59.07
Std Dev	11.13



# B1L100S, U6-ch51, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry





# B1L100S, U6-ch51, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	3
Mean	6.333
Std Dev	8.957

# B1L100S, U6-ch52, adc0

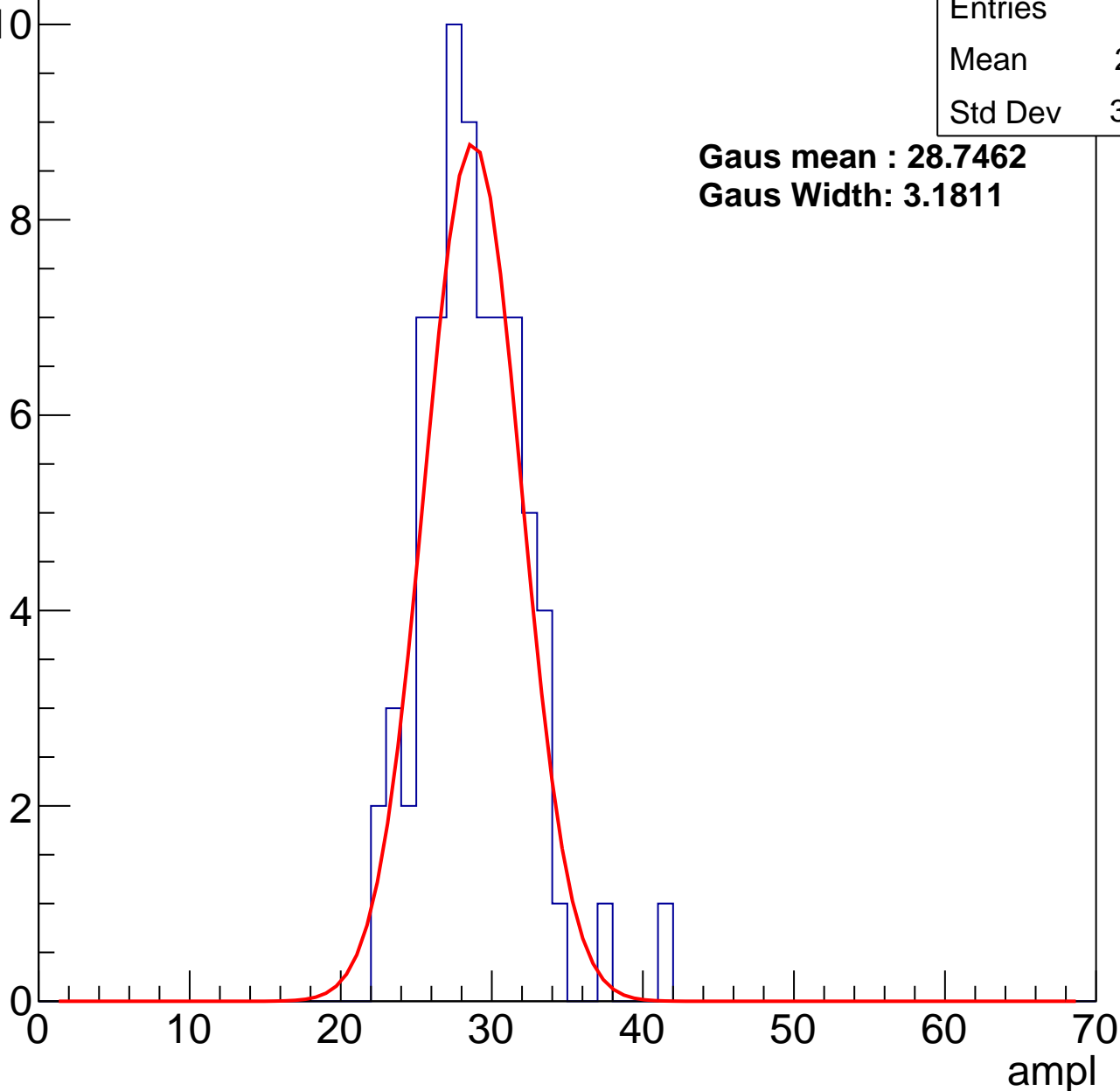
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	73
Mean	28.41
Std Dev	3.375

**Gaus mean : 28.7462**

**Gaus Width: 3.1811**



# B1L100S, U6-ch52, adc1

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	89
Mean	35.48
Std Dev	5.469

**Gaus mean : 36.5699**

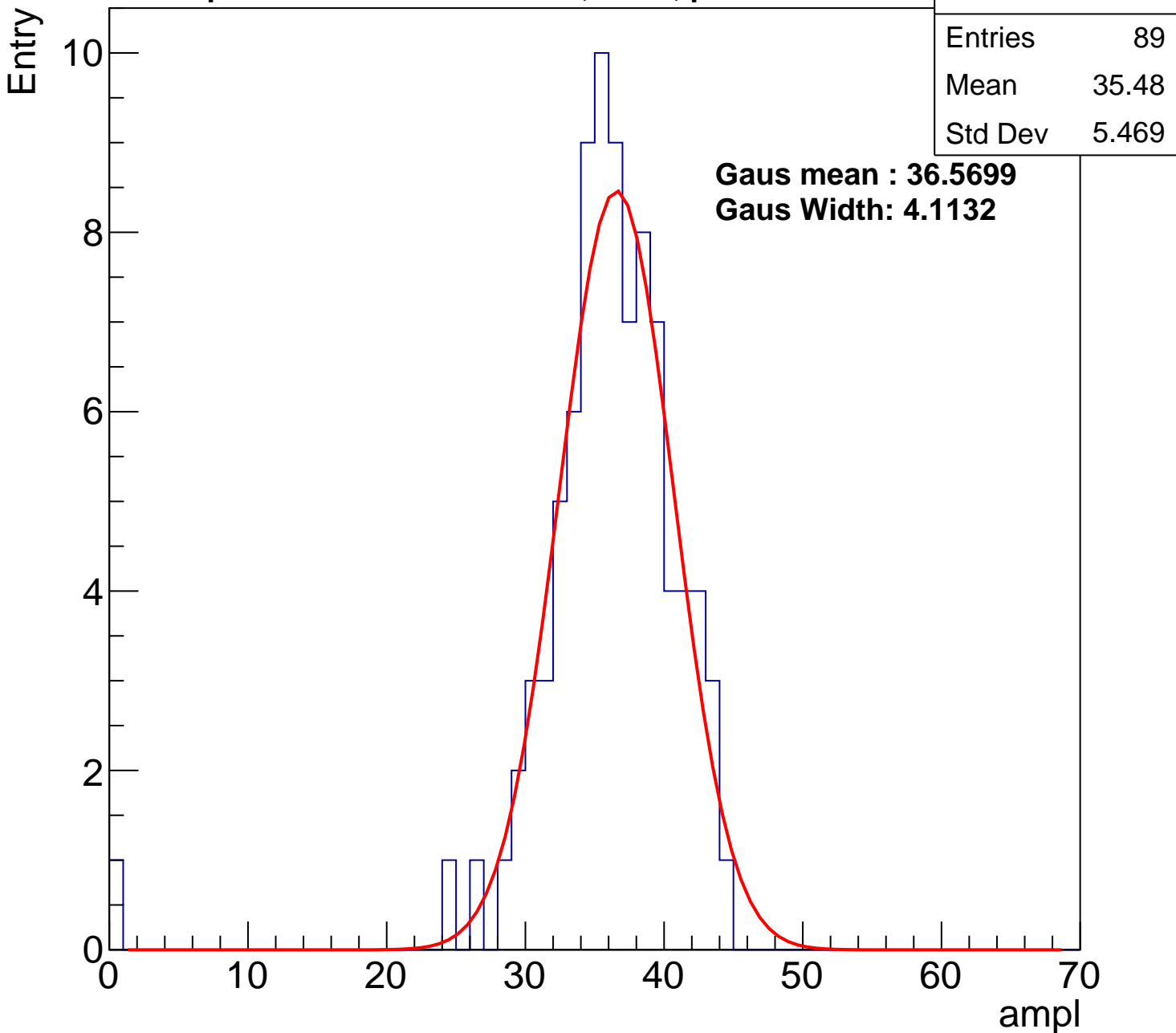
**Gaus Width: 4.1132**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L100S, U6-ch52, adc2

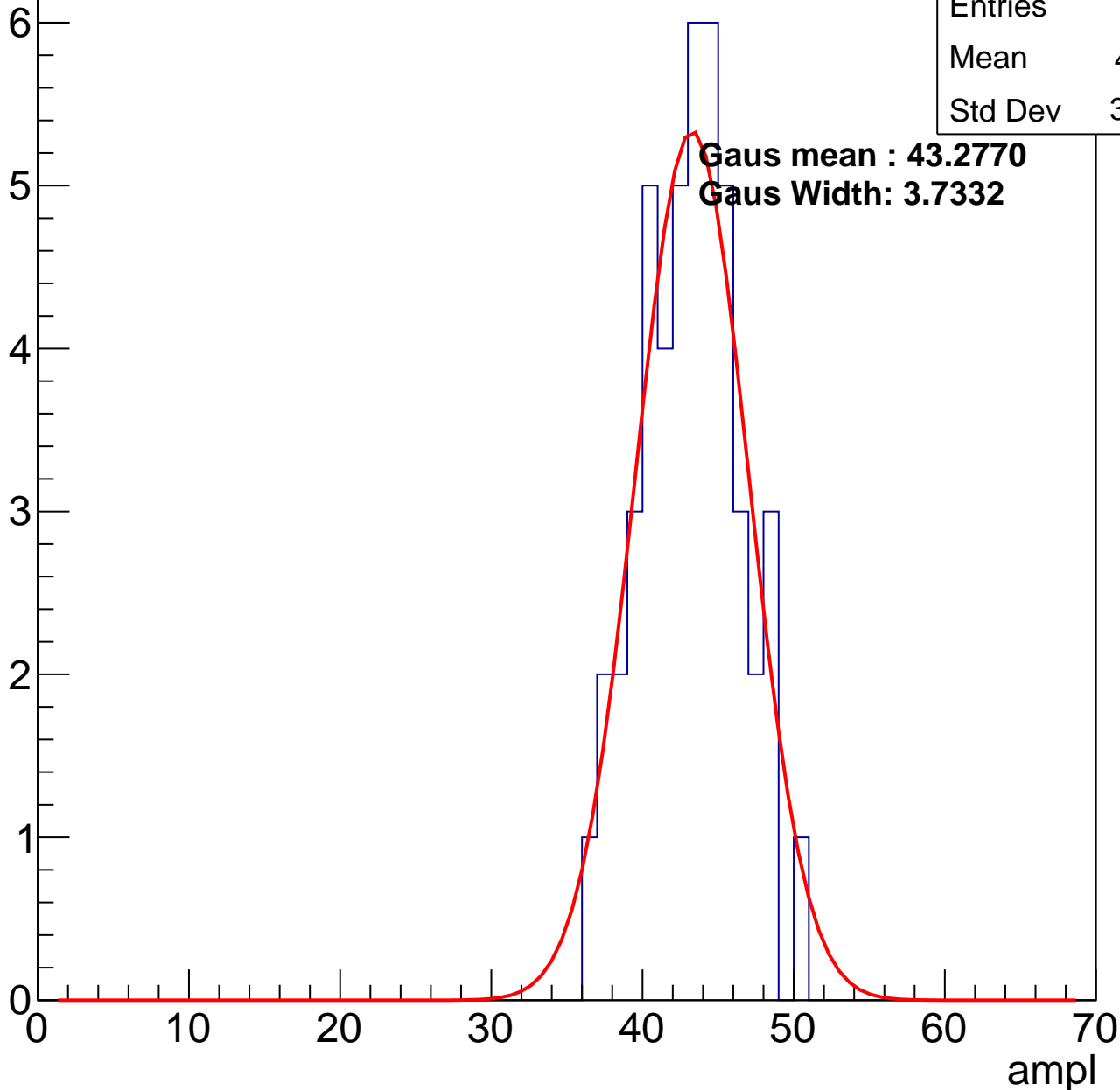
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	48
Mean	42.71
Std Dev	3.195

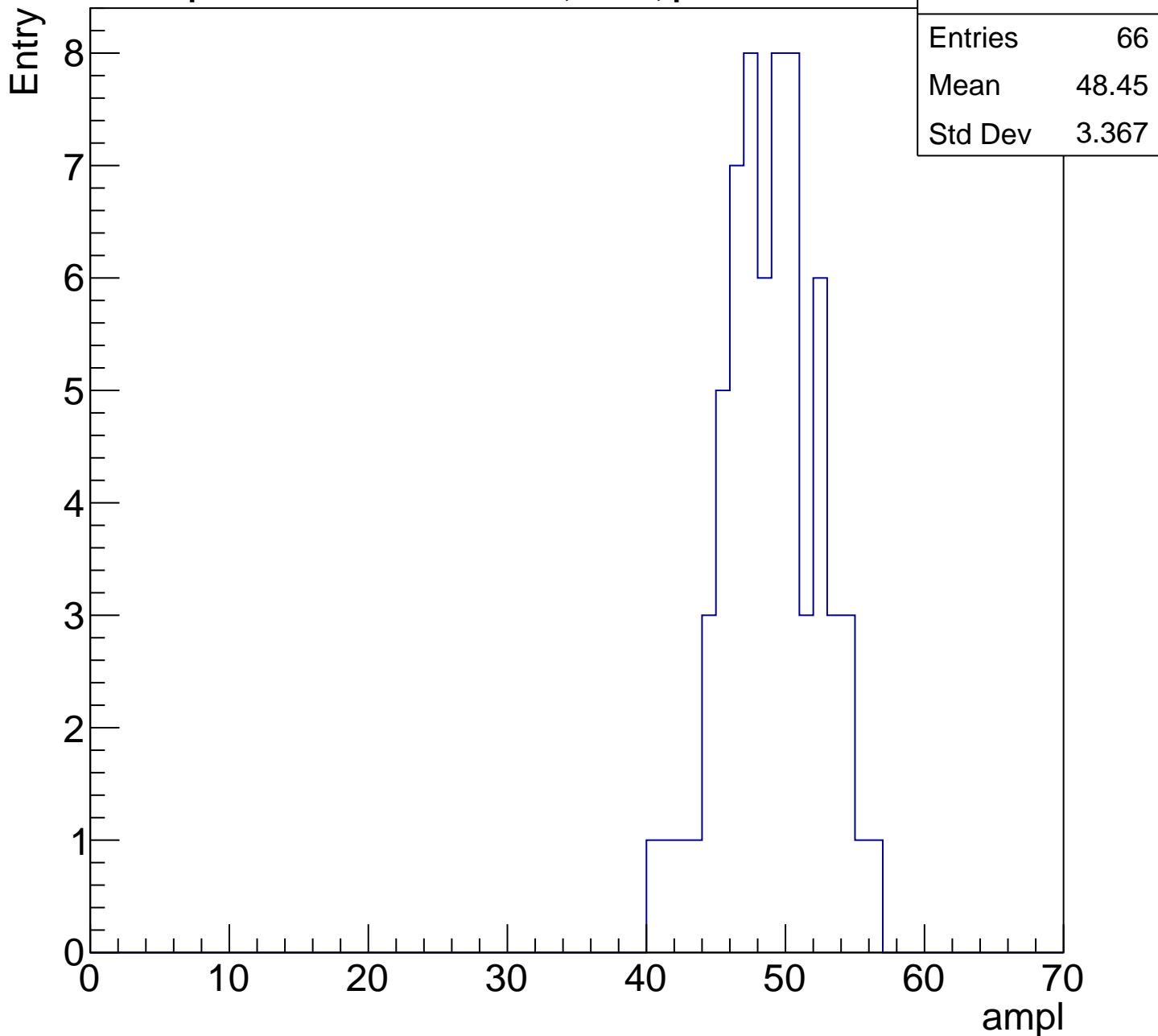
**Gaus mean : 43.2770**

**Gaus Width: 3.7332**



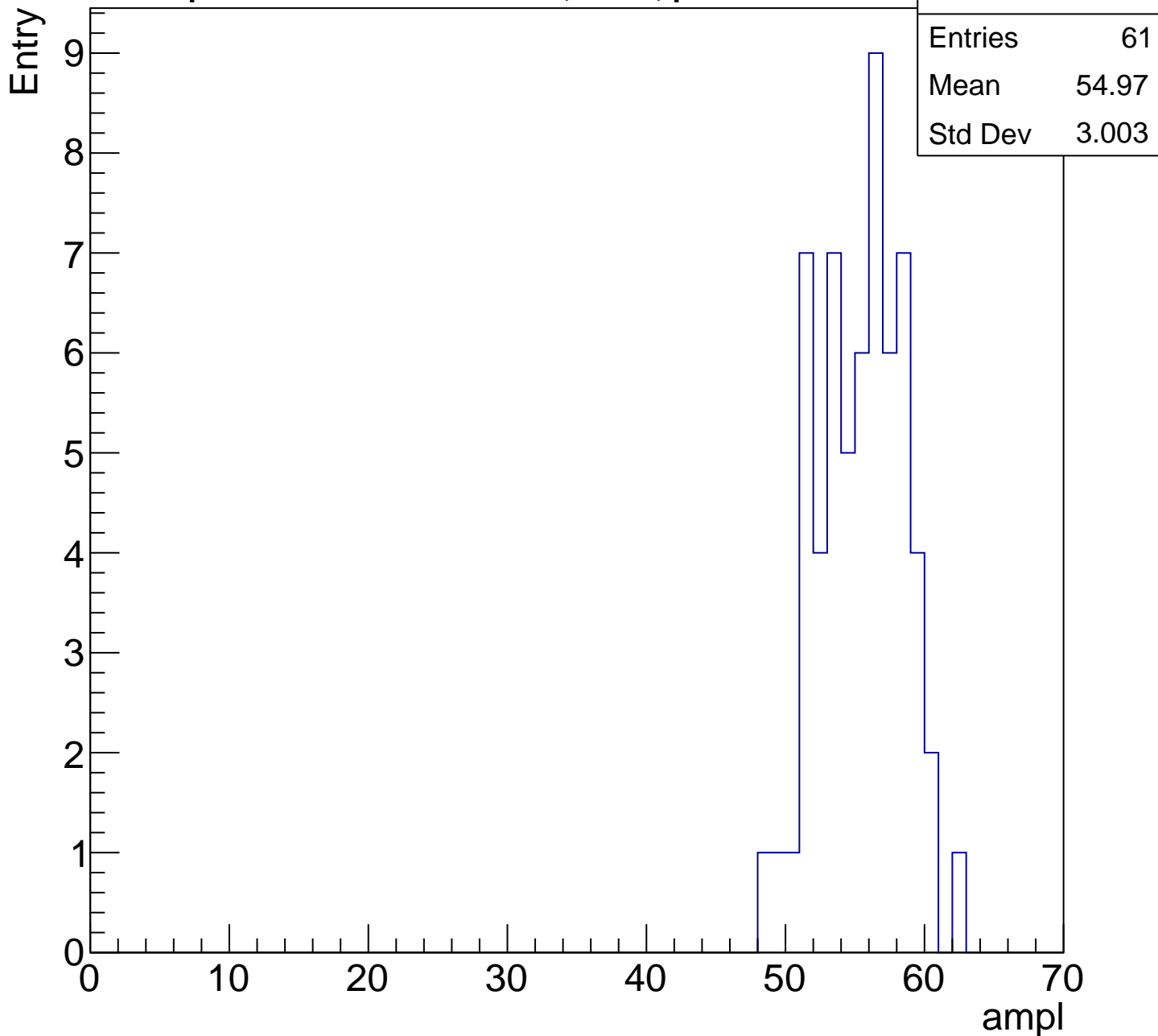
# B1L100S, U6-ch52, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2



# B1L100S, U6-ch52, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

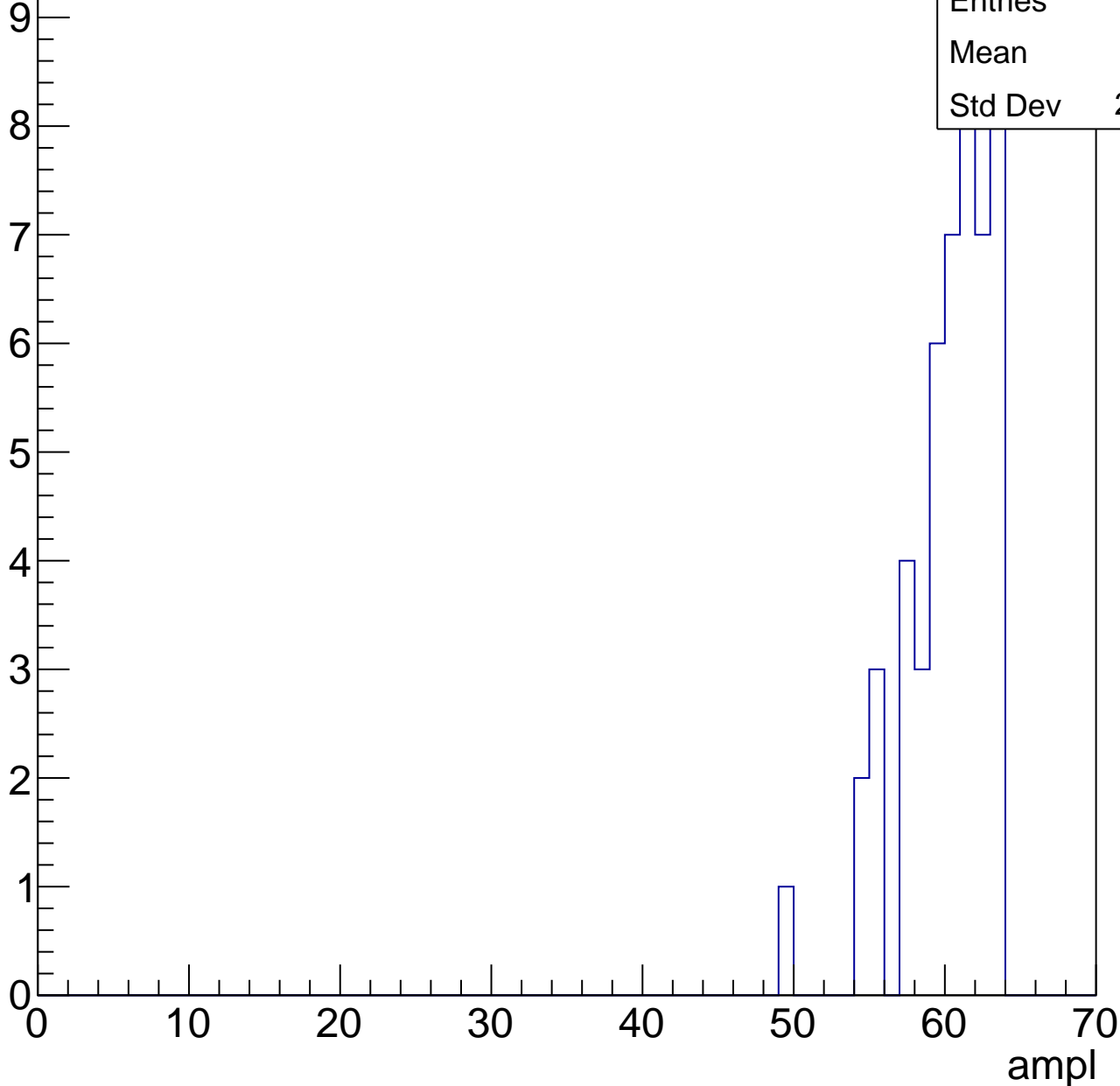


# B1L100S, U6-ch52, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	50
Mean	59.7
Std Dev	2.921



# B1L100S, U6-ch52, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

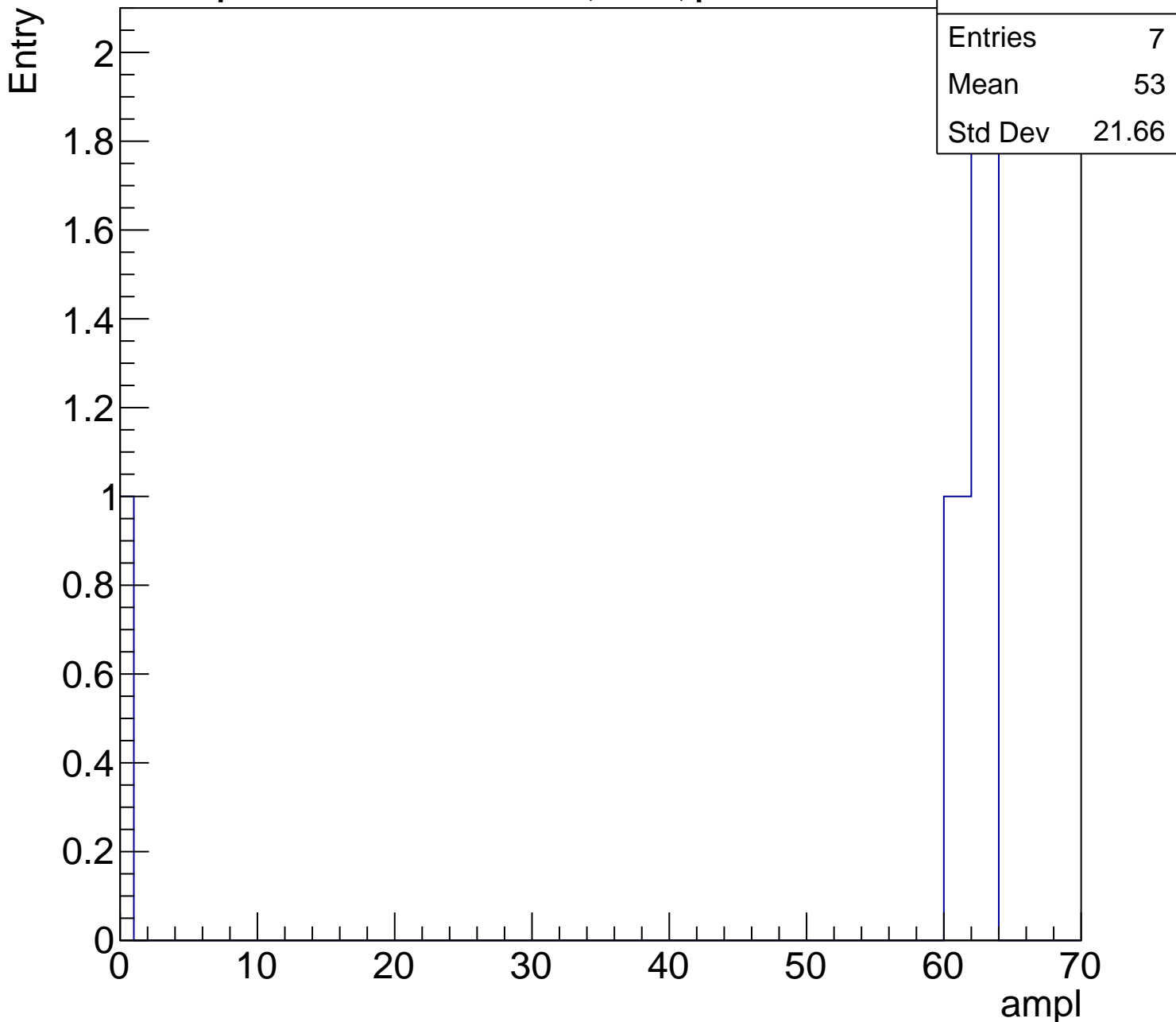
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	7
Mean	53
Std Dev	21.66

ampl

0 10 20 30 40 50 60 70





# B1L100S, U6-ch52, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



# B1L100S, U6-ch53, adc0

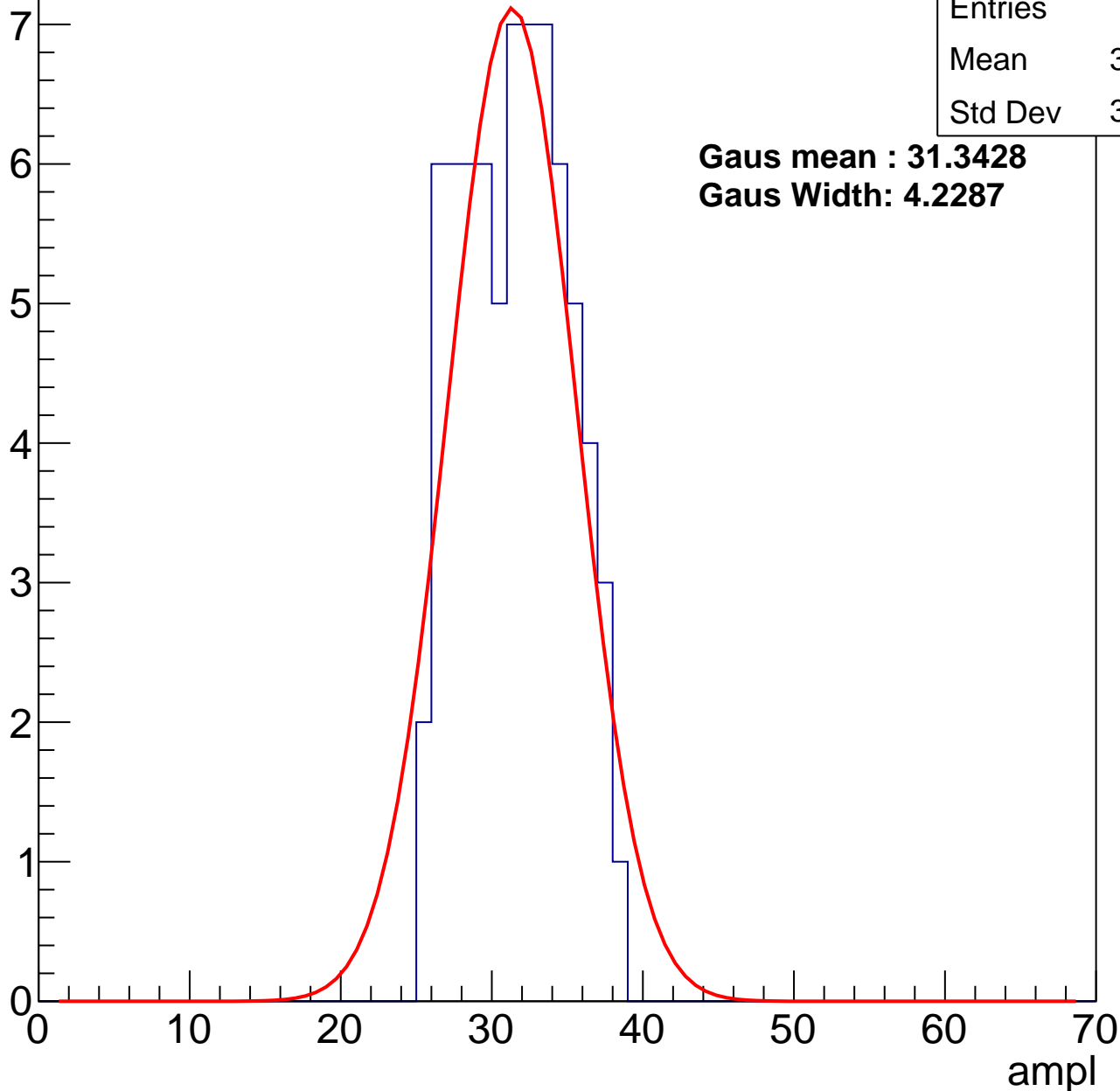
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	71
Mean	31.04
Std Dev	3.413

**Gaus mean : 31.3428**

**Gaus Width: 4.2287**



# B1L100S, U6-ch53, adc1

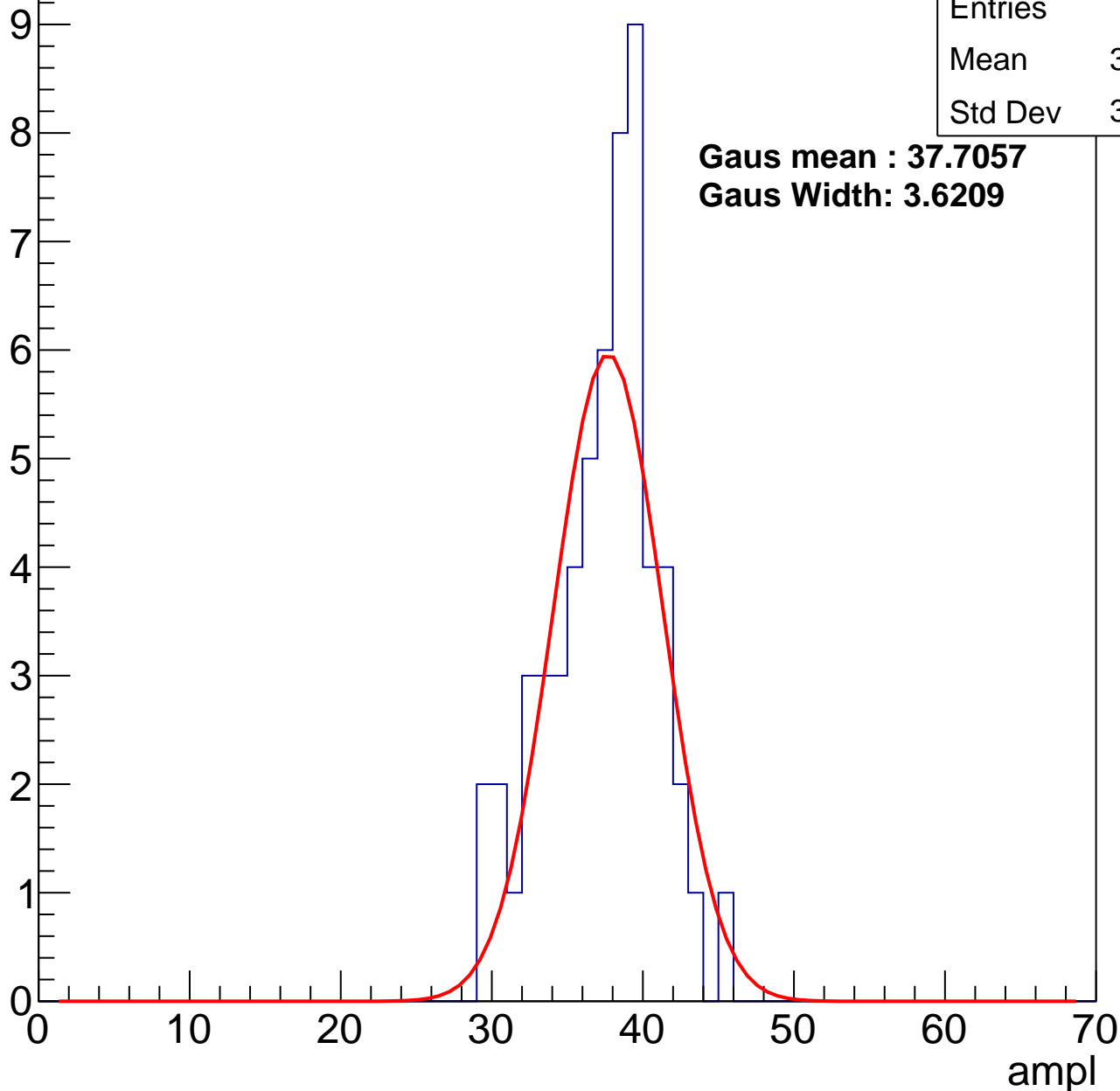
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	58
Mean	36.88
Std Dev	3.538

**Gaus mean : 37.7057**

**Gaus Width: 3.6209**



# B1L100S, U6-ch53, adc2

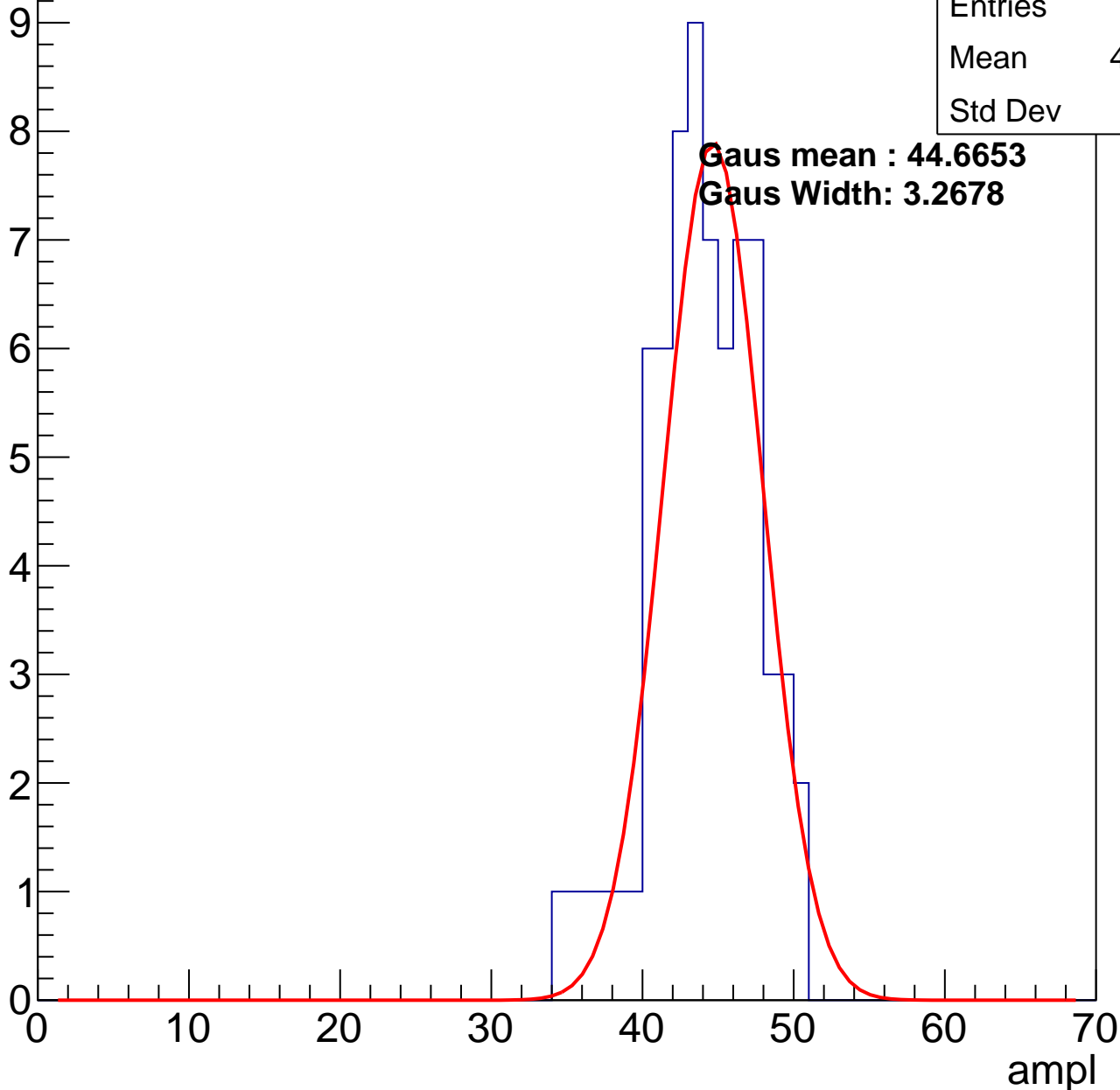
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	70
Mean	43.54
Std Dev	3.43

**Gaus mean : 44.6653**

**Gaus Width: 3.2678**

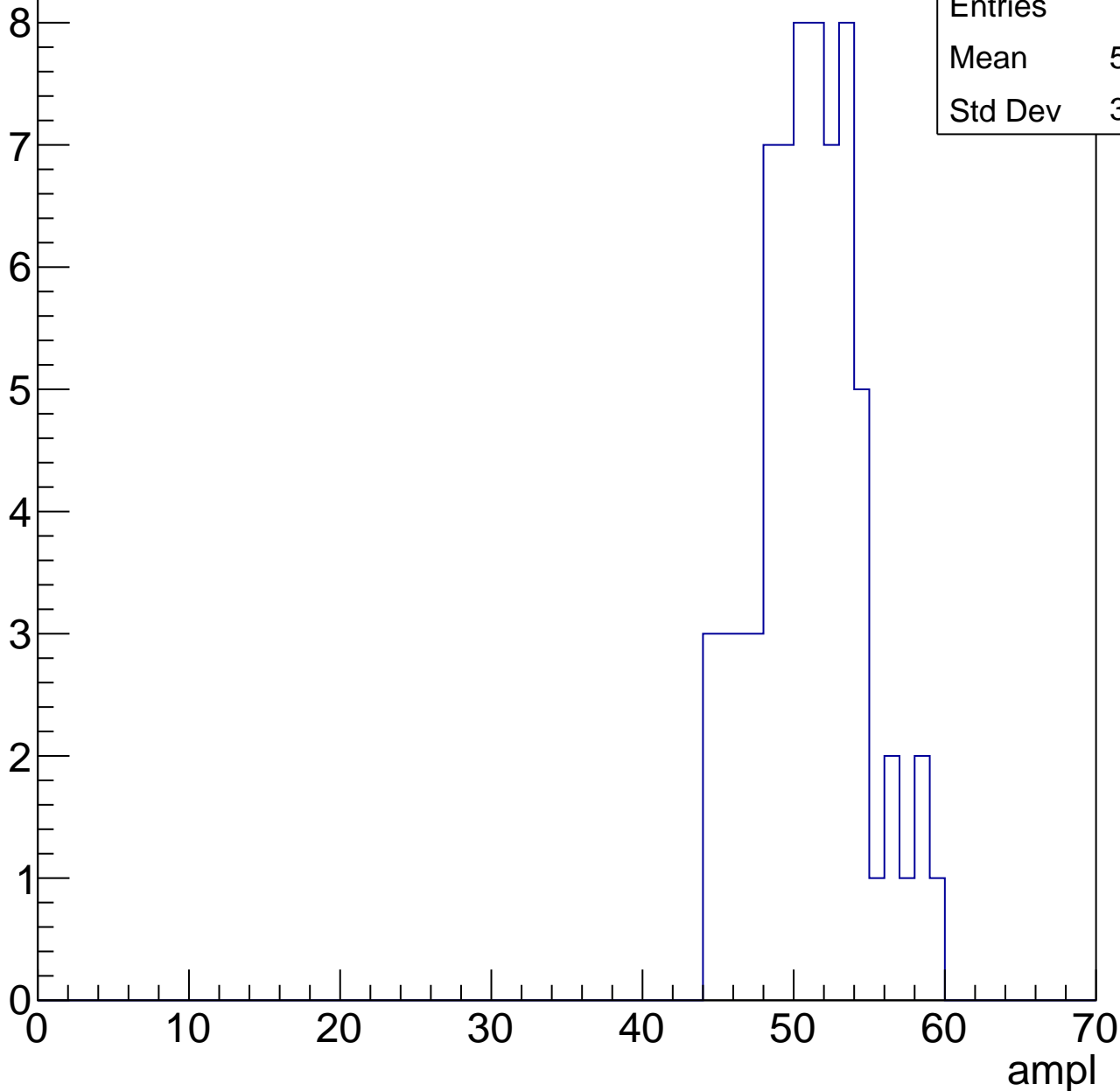


# B1L100S, U6-ch53, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

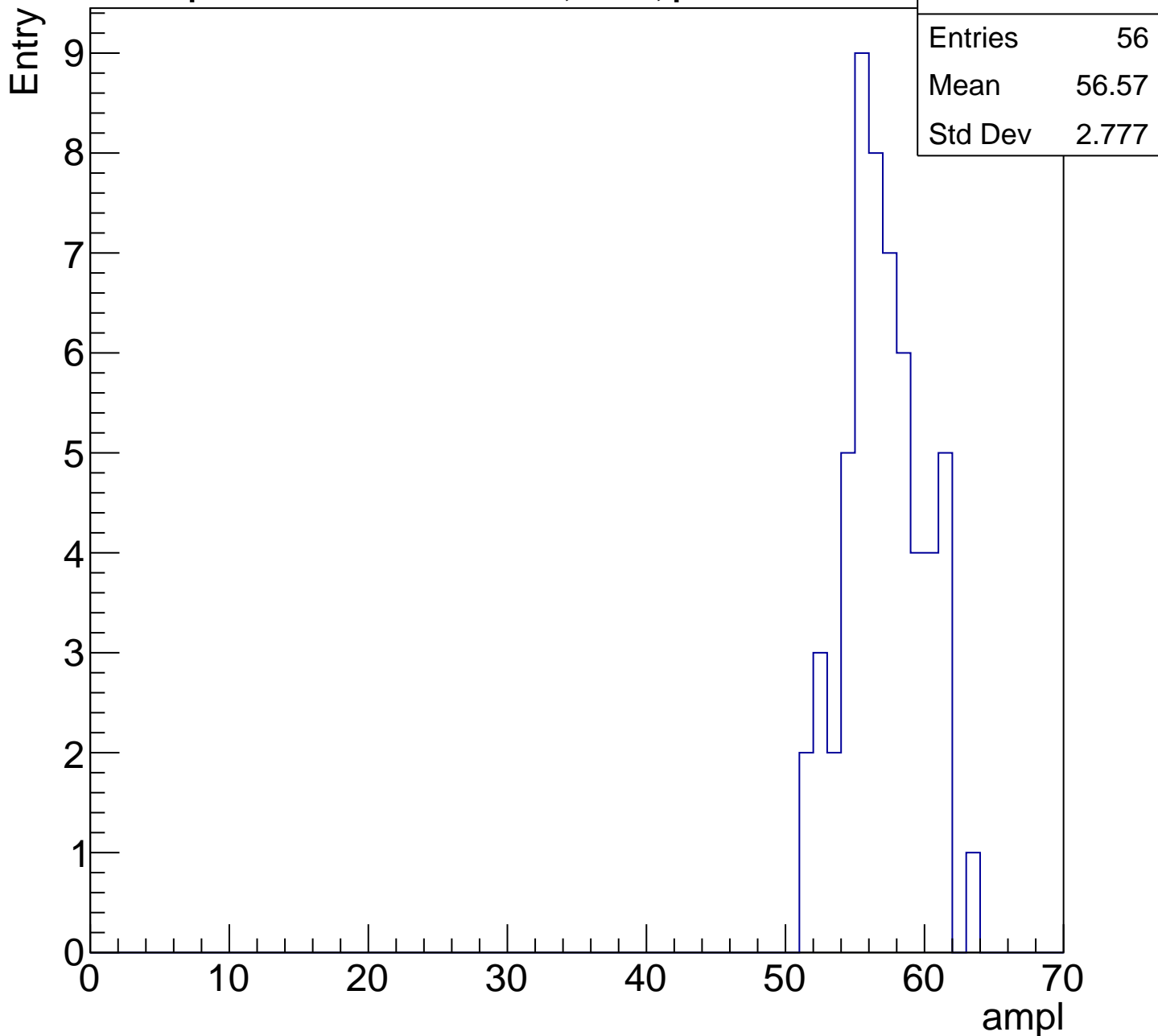
Entry

Entries	69
Mean	50.58
Std Dev	3.432



# B1L100S, U6-ch53, adc4

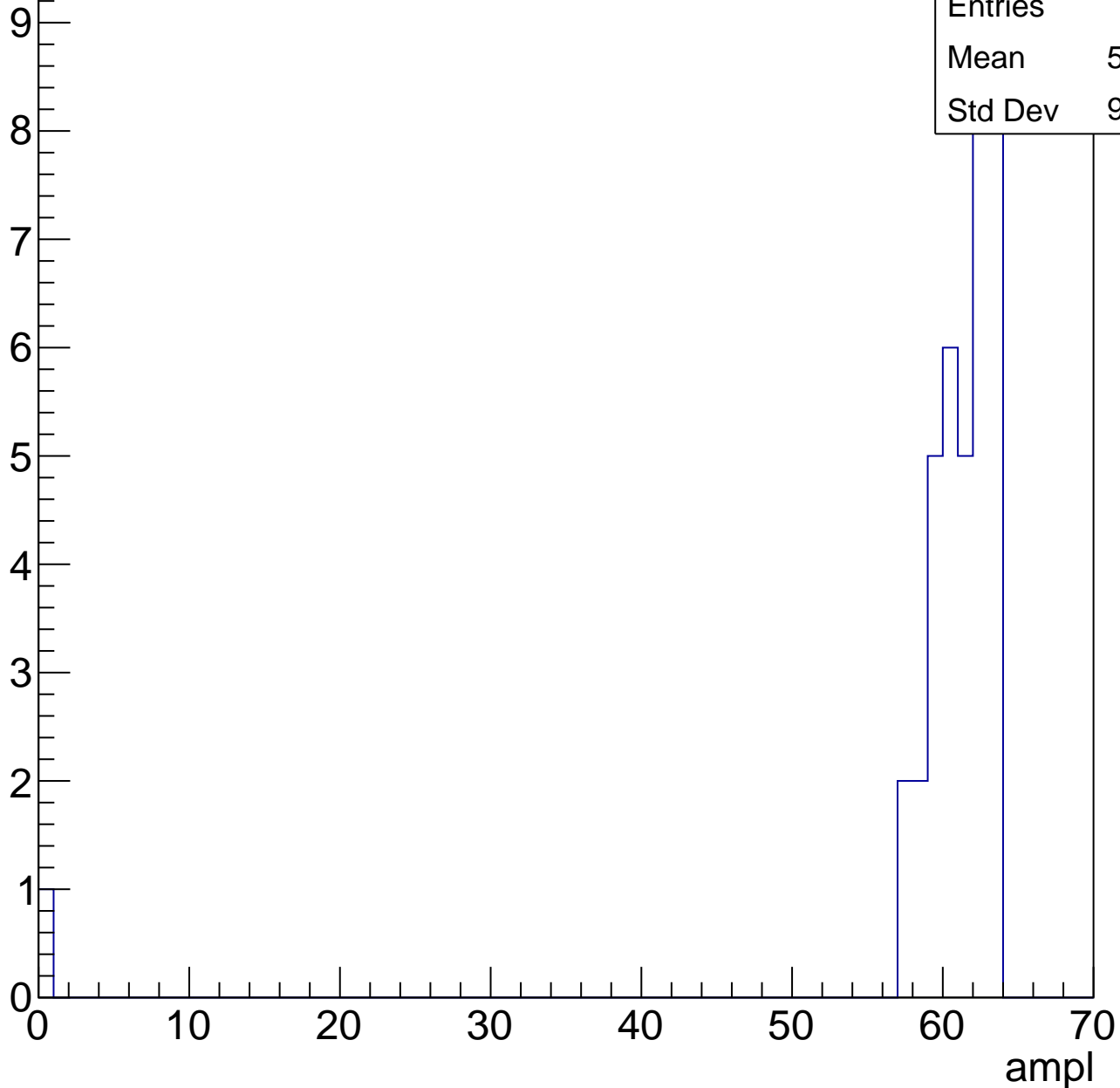
calib\_packv5\_042523\_0143.root, FC#4, port A2



# B1L100S, U6-ch53, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



# B1L100S, U6-ch53, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry





# B1L100S, U6-ch53, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L100S, U6-ch54, adc0

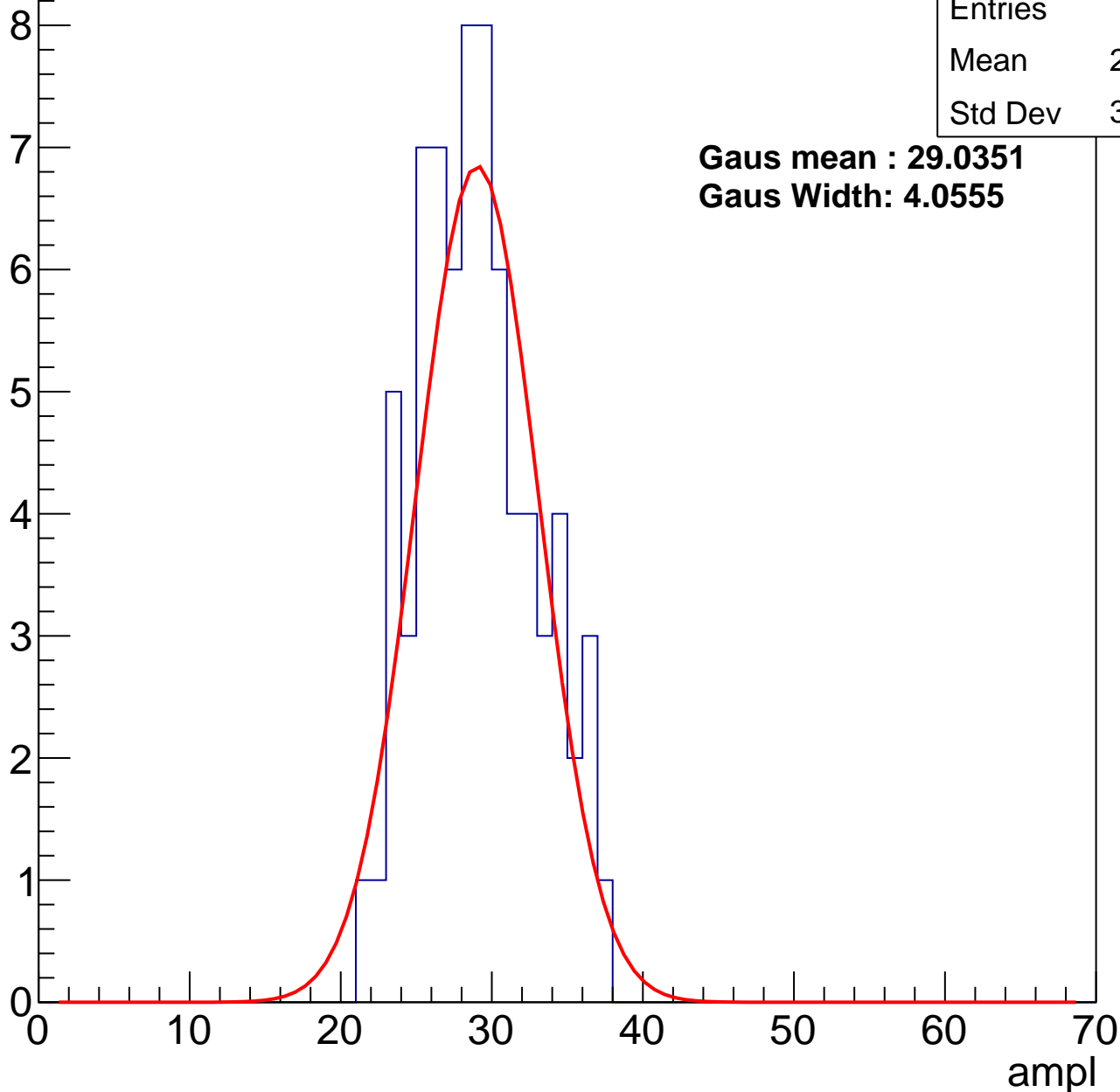
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	73
Mean	28.59
Std Dev	3.796

**Gaus mean : 29.0351**

**Gaus Width: 4.0555**



# B1L100S, U6-ch54, adc1

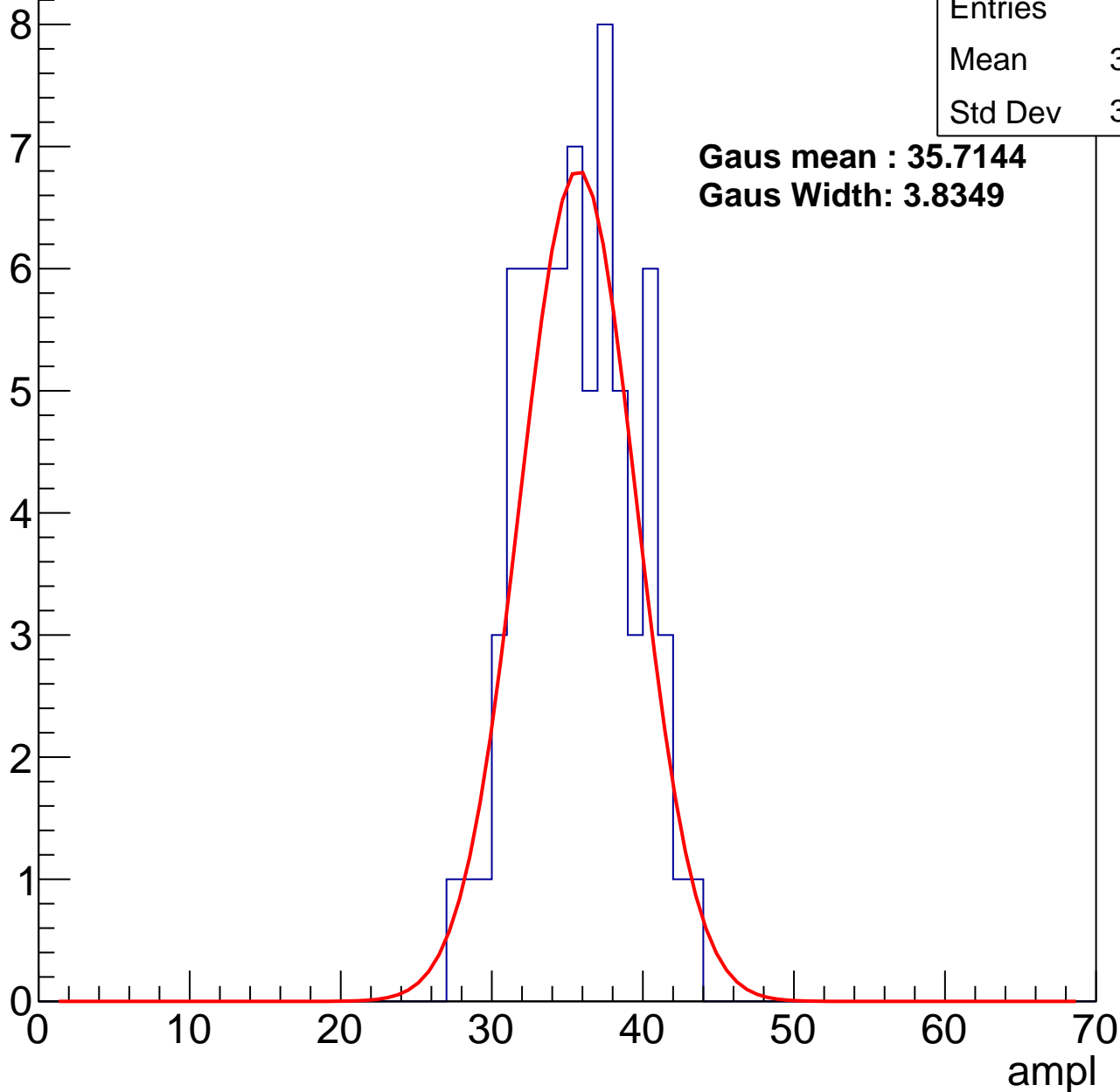
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	69
Mean	35.22
Std Dev	3.615

**Gaus mean : 35.7144**

**Gaus Width: 3.8349**



# B1L100S, U6-ch54, adc2

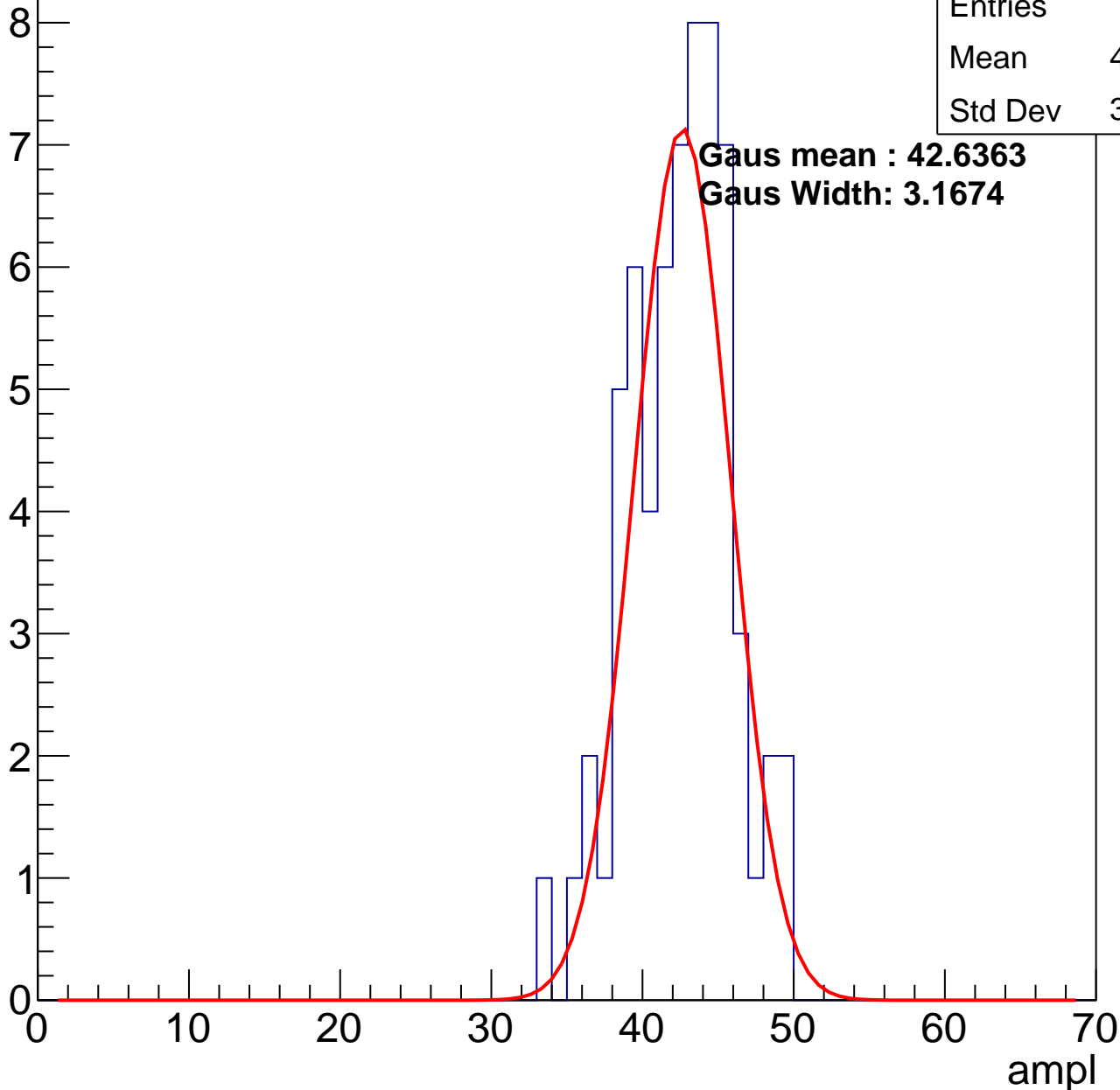
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	64
Mean	42.05
Std Dev	3.375

**Gaus mean : 42.6363**

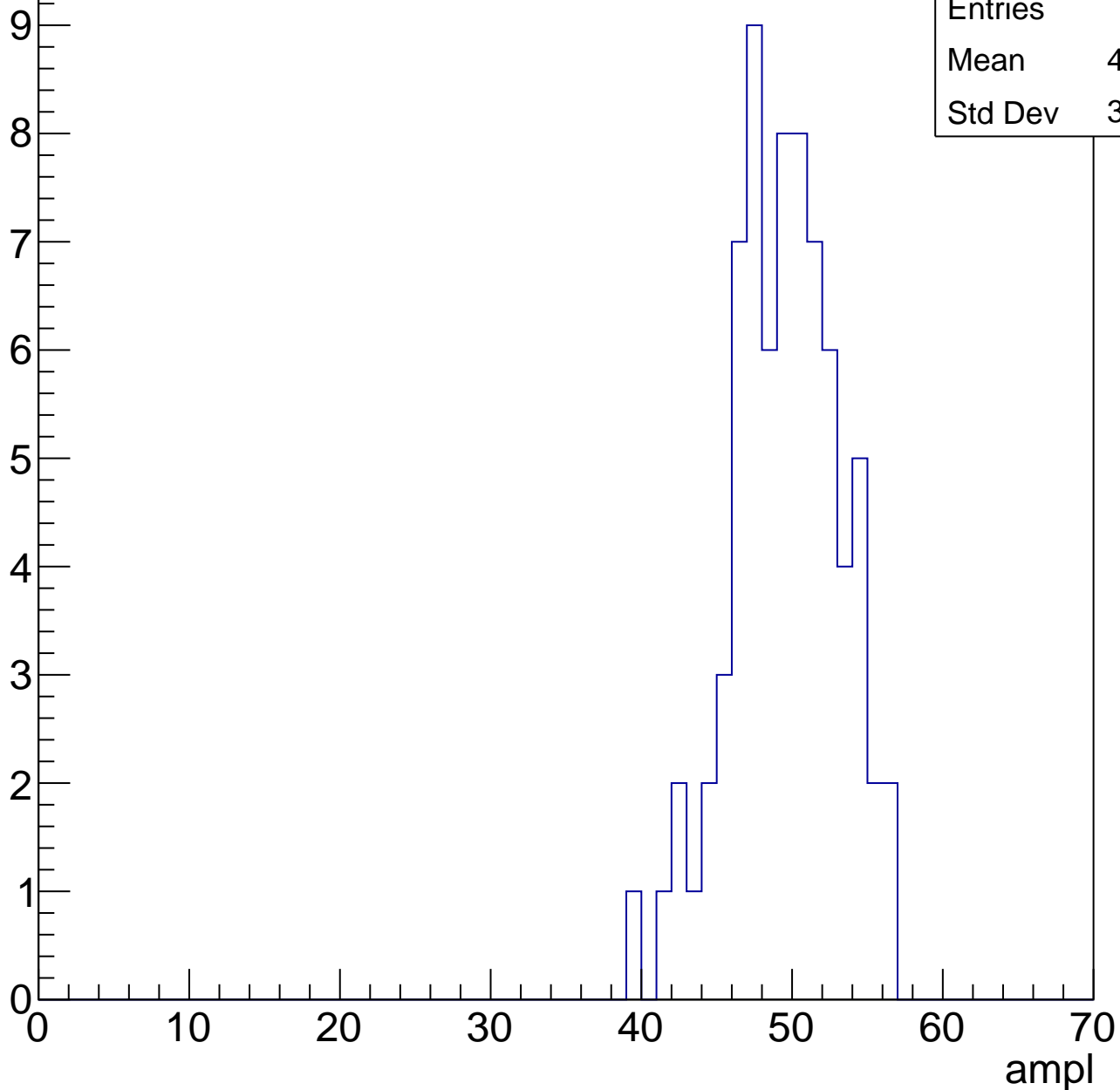
**Gaus Width: 3.1674**



# B1L100S, U6-ch54, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



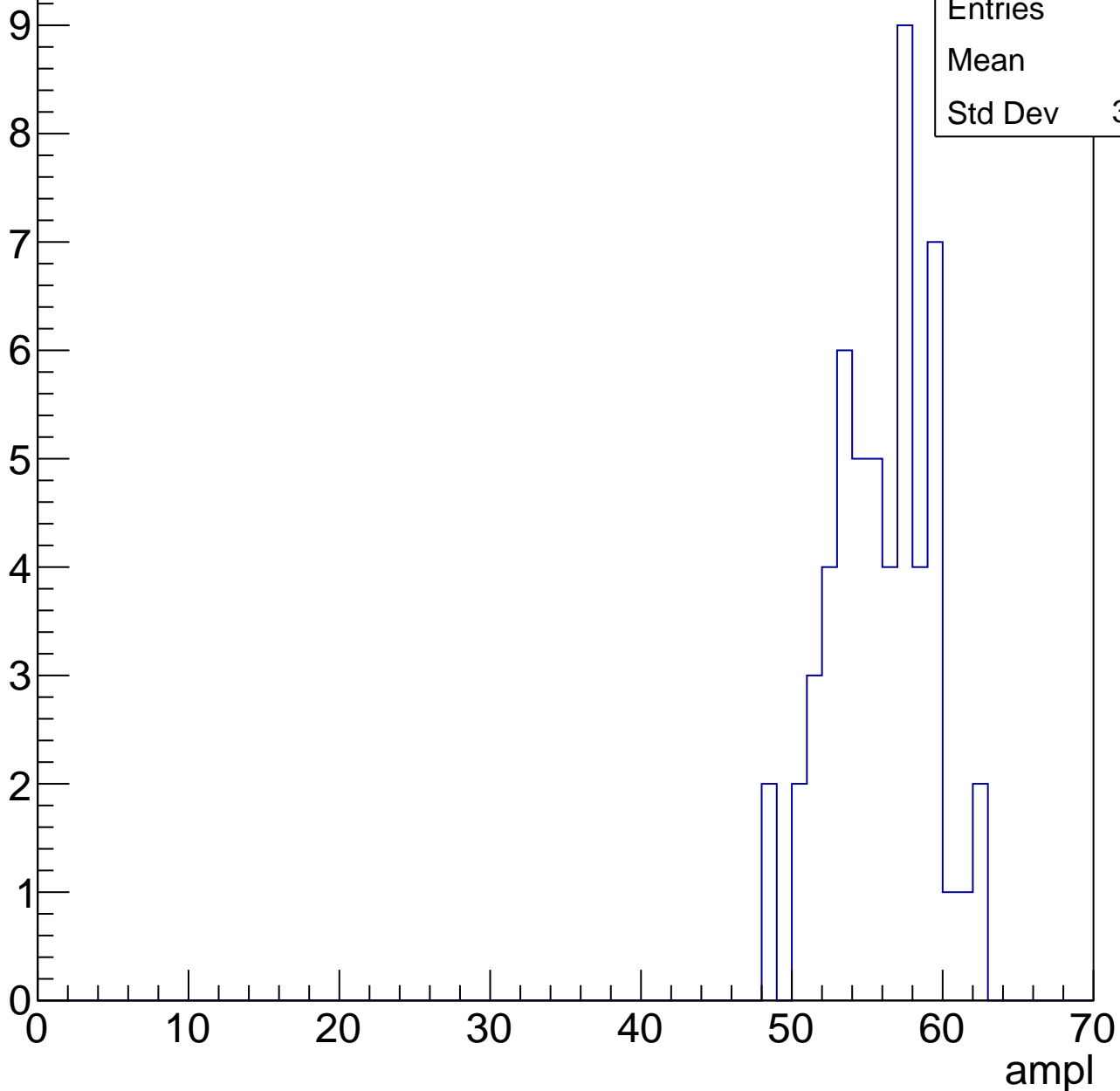
Entries	74
Mean	49.03
Std Dev	3.583

# B1L100S, U6-ch54, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	55
Mean	55.4
Std Dev	3.301



# B1L100S, U6-ch54, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	50
Mean	58.78
Std Dev	8.735

ampl

0

10

20

30

40

50

60

70

# B1L100S, U6-ch54, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	4
Mean	61.75
Std Dev	1.09

ampl

0 10 20 30 40 50 60 70



# B1L100S, U6-ch54, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L100S, U6-ch55, adc0

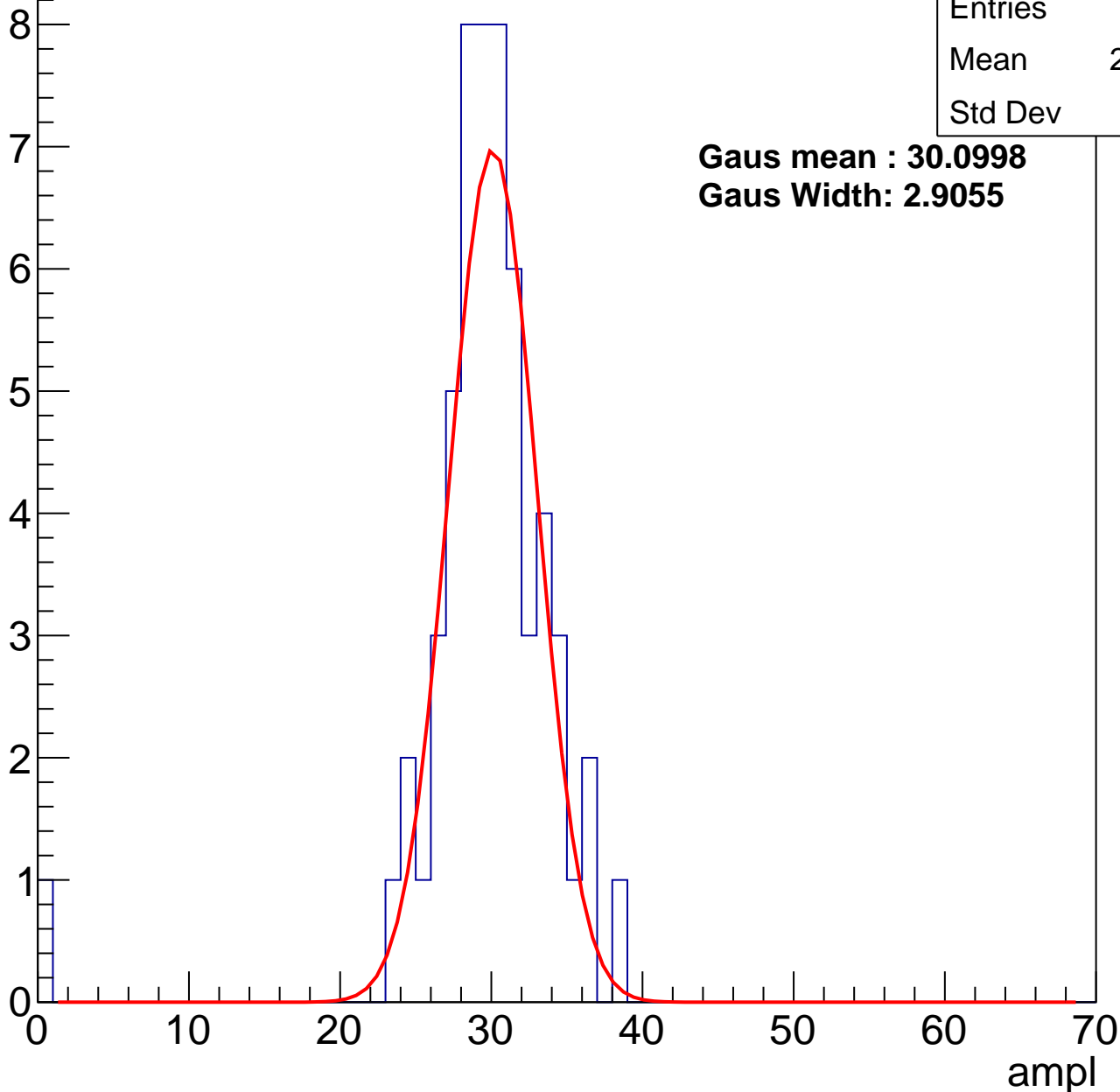
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	57
Mean	29.23
Std Dev	4.97

**Gaus mean : 30.0998**

**Gaus Width: 2.9055**



# B1L100S, U6-ch55, adc1

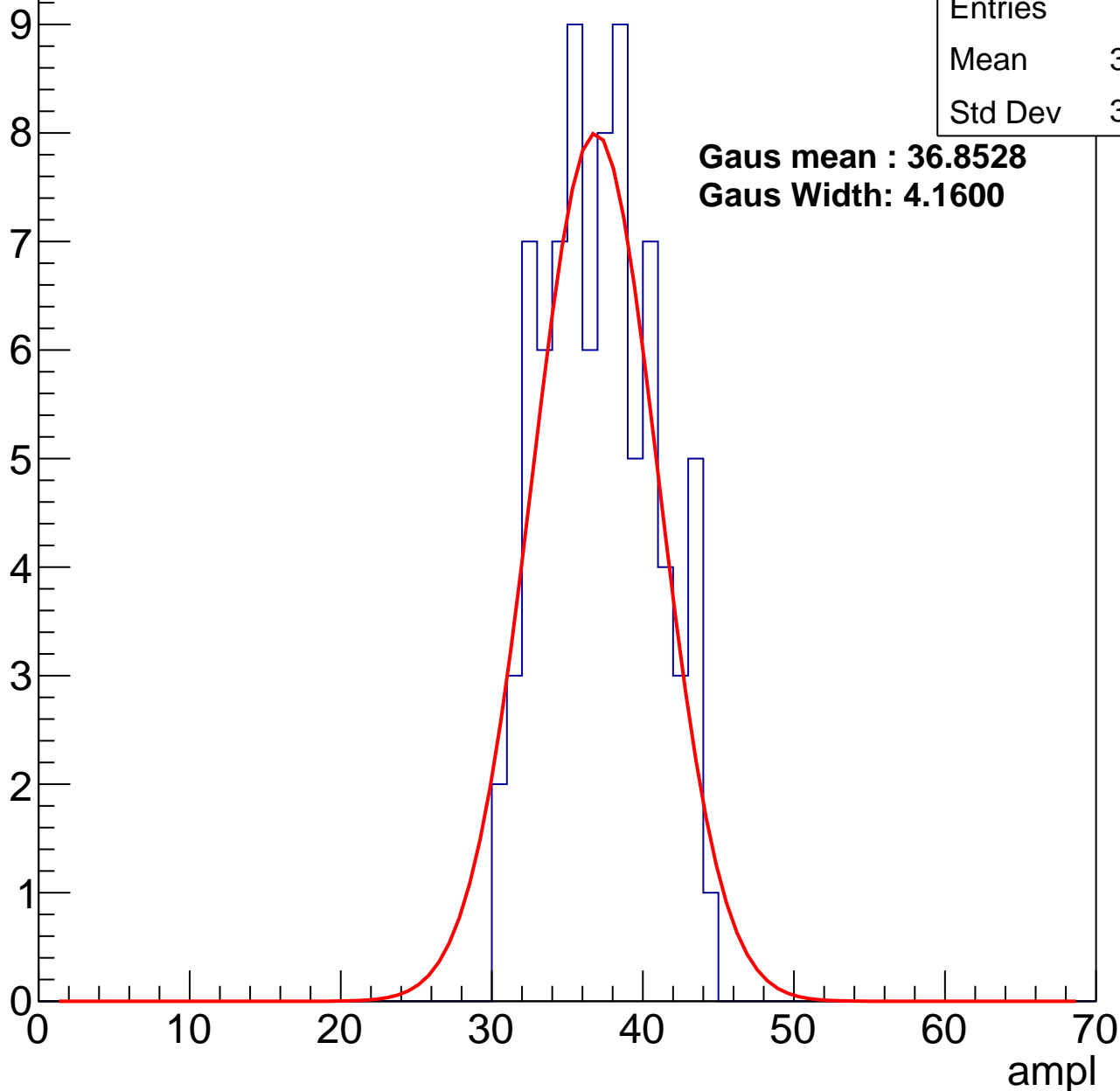
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	82
Mean	36.66
Std Dev	3.548

**Gaus mean : 36.8528**

**Gaus Width: 4.1600**



# B1L100S, U6-ch55, adc2

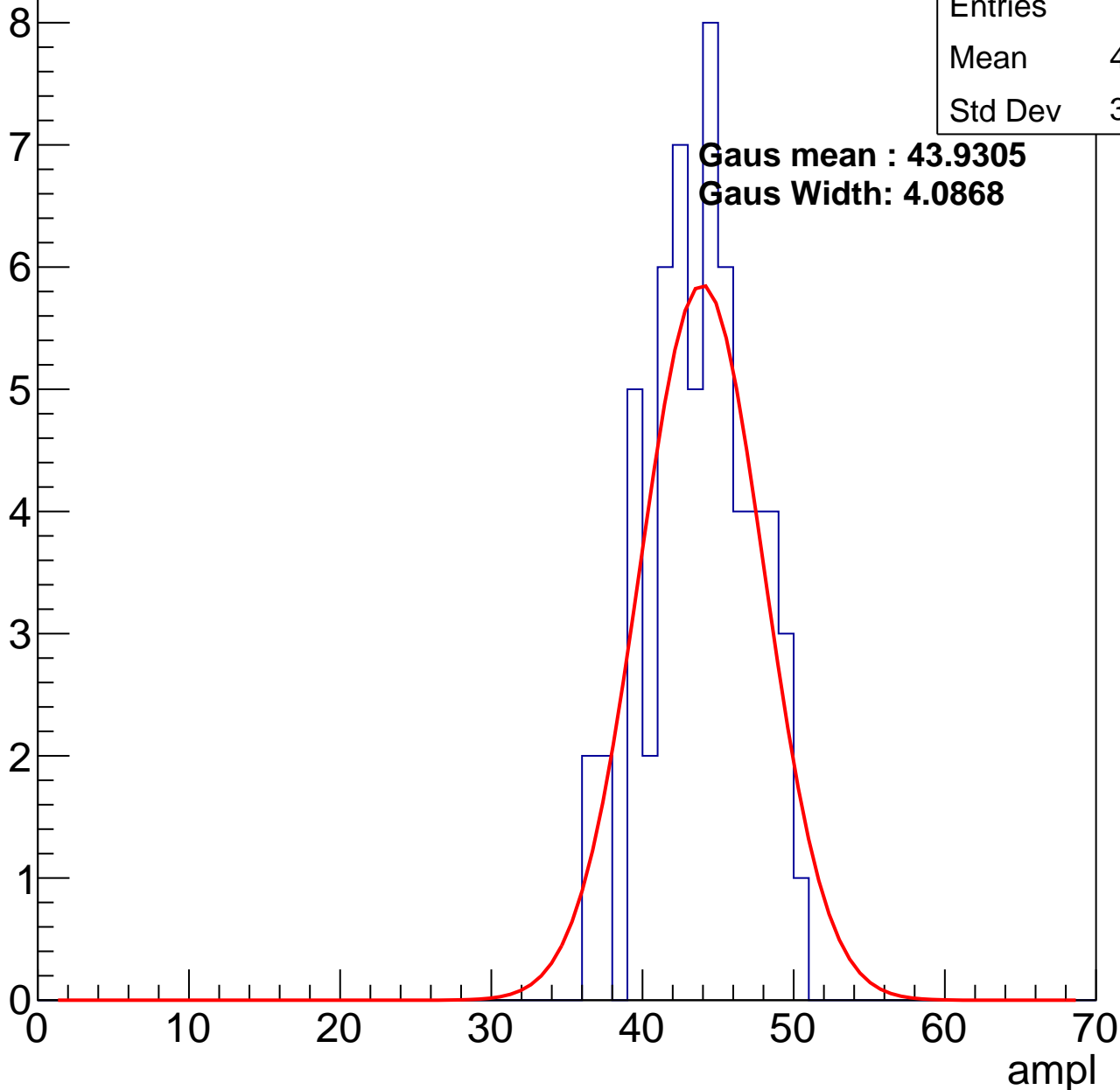
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	59
Mean	43.37
Std Dev	3.394

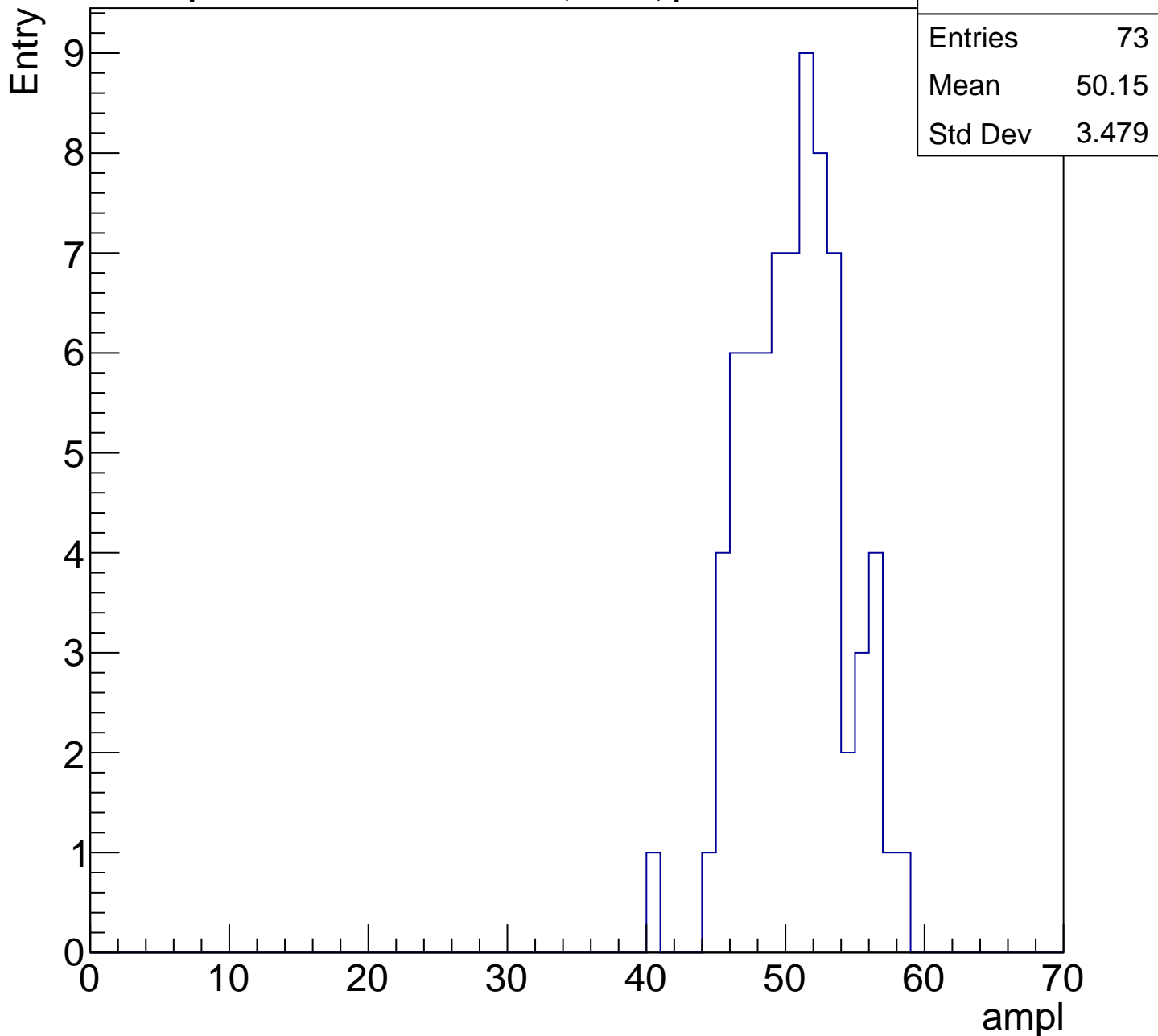
**Gaus mean : 43.9305**

**Gaus Width: 4.0868**



# B1L100S, U6-ch55, adc3

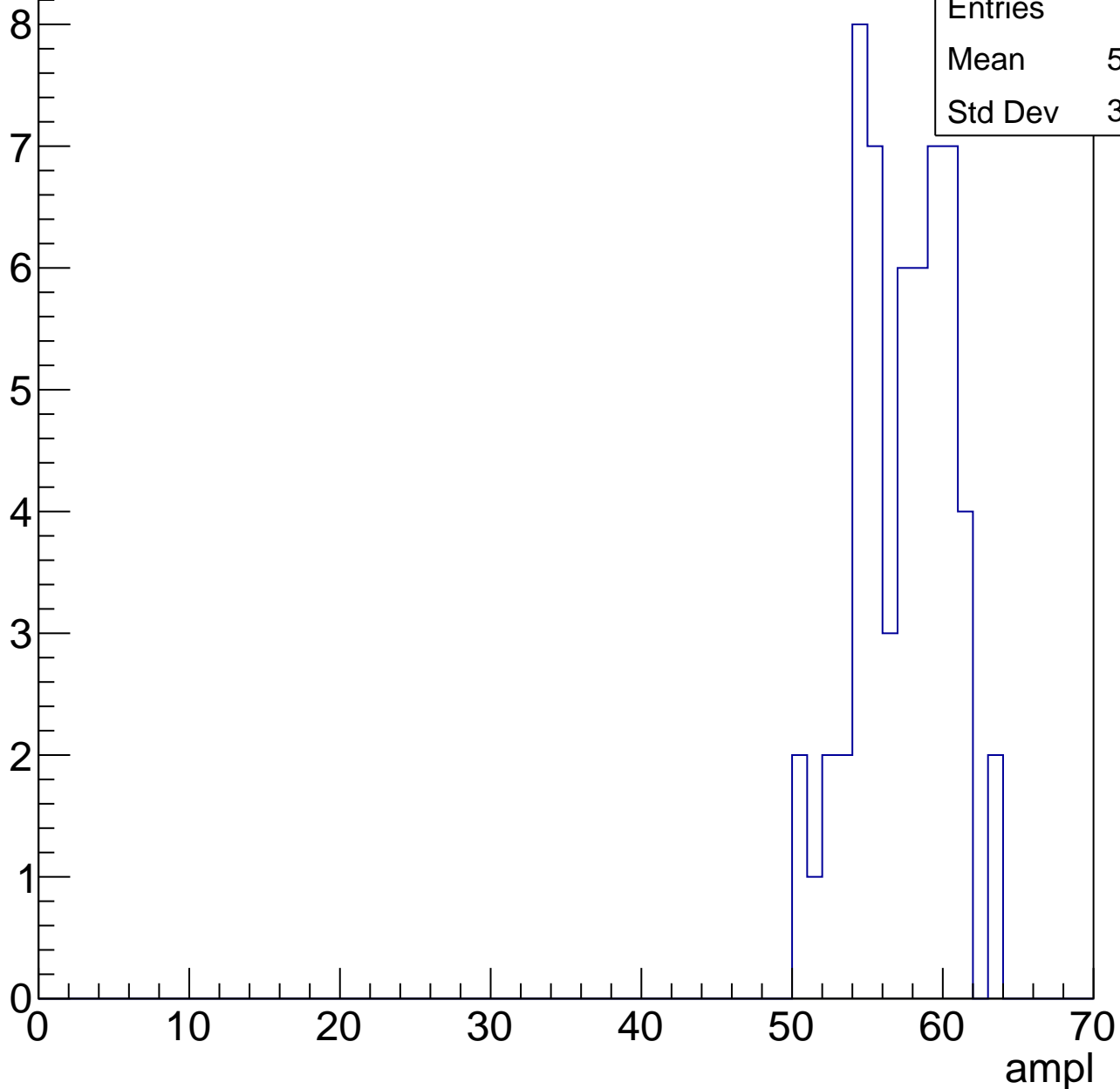
calib\_packv5\_042523\_0143.root, FC#4, port A2



# B1L100S, U6-ch55, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	57
Mean	56.82
Std Dev	3.107

# B1L100S, U6-ch55, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	39
Mean	58.69
Std Dev	9.845

Entry

10

8

6

4

2

0

0

10

20

30

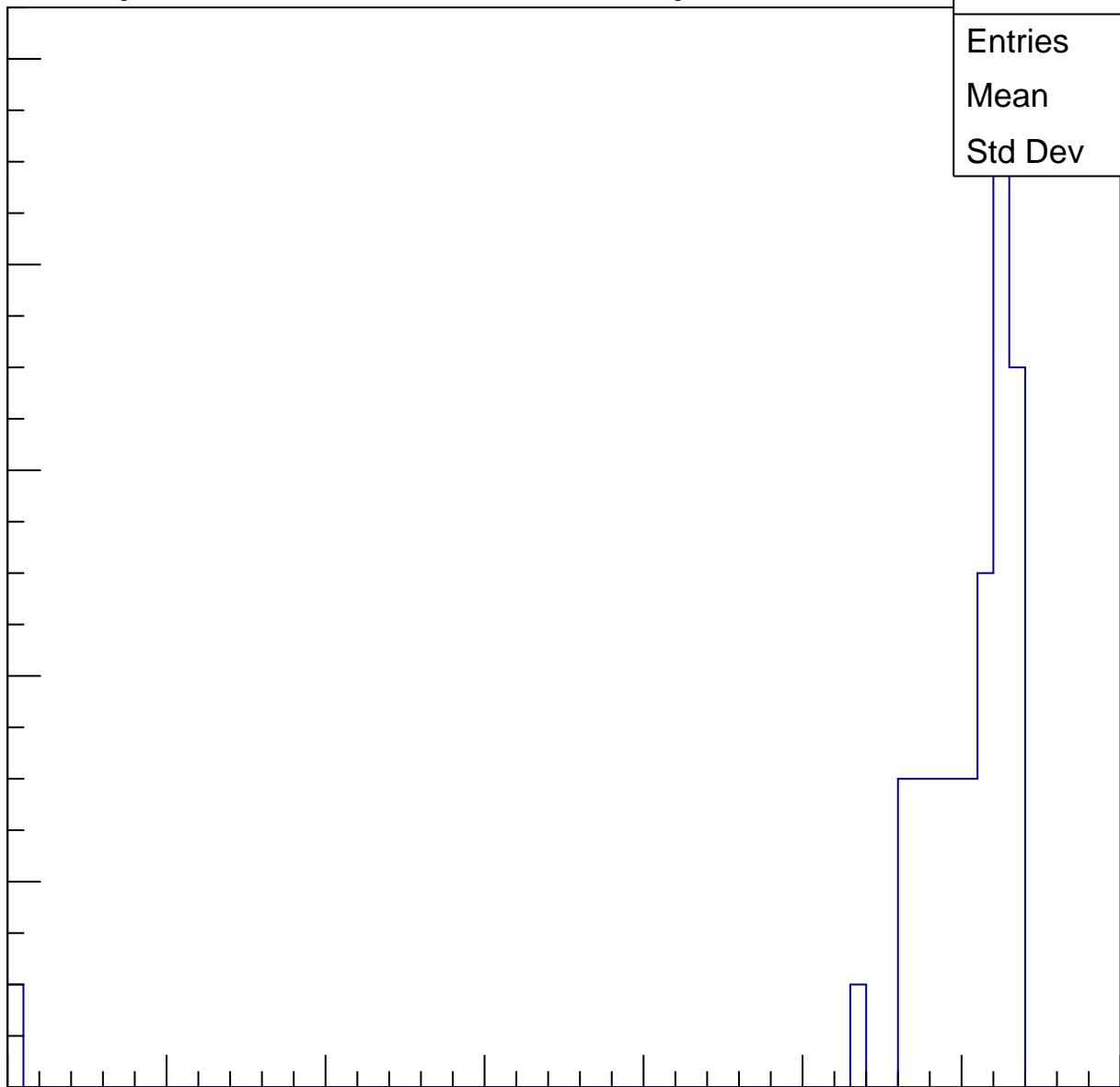
40

50

60

70

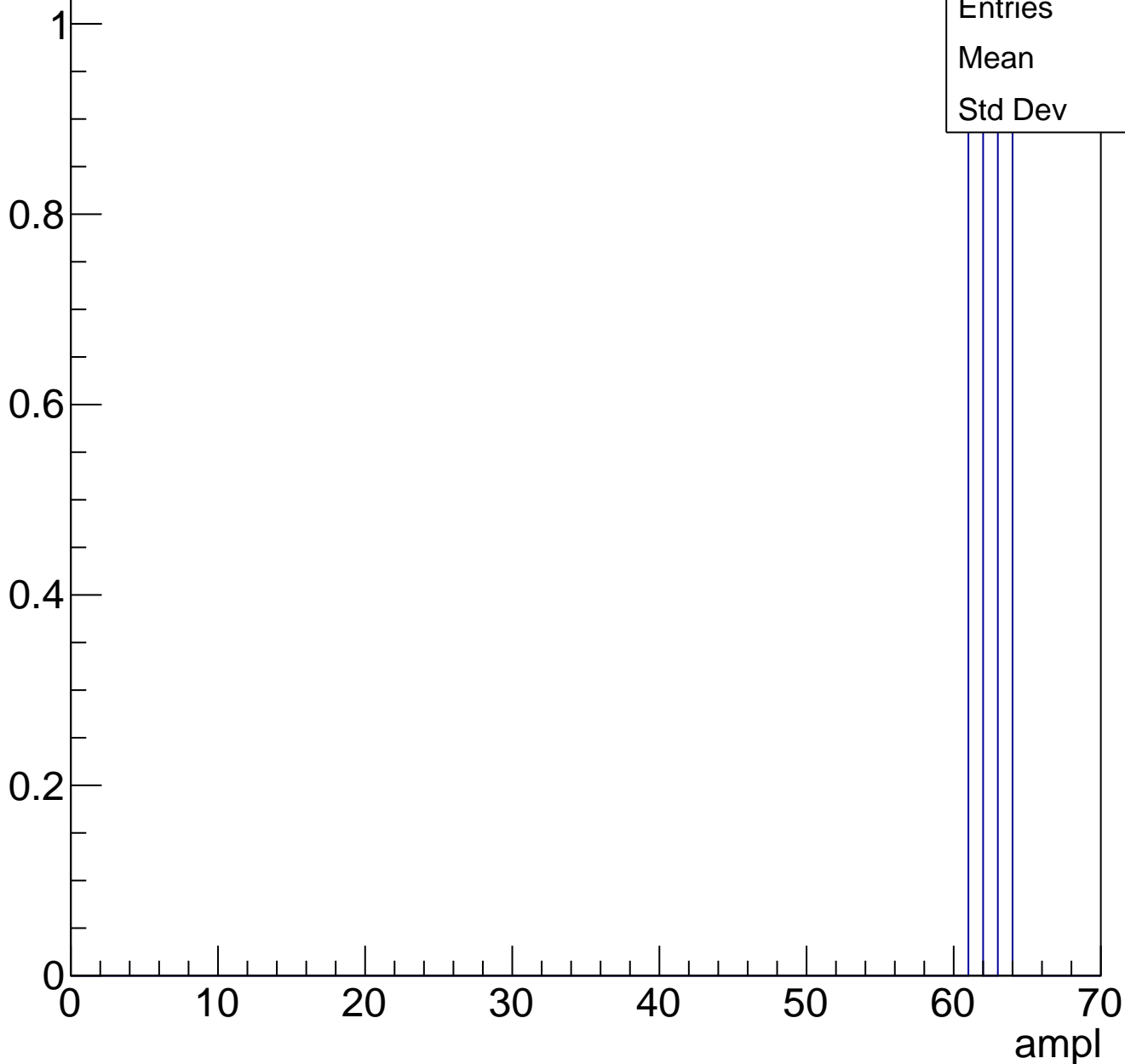
ampl



# B1L100S, U6-ch55, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry





# B1L100S, U6-ch55, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	0
Mean	0
Std Dev	0

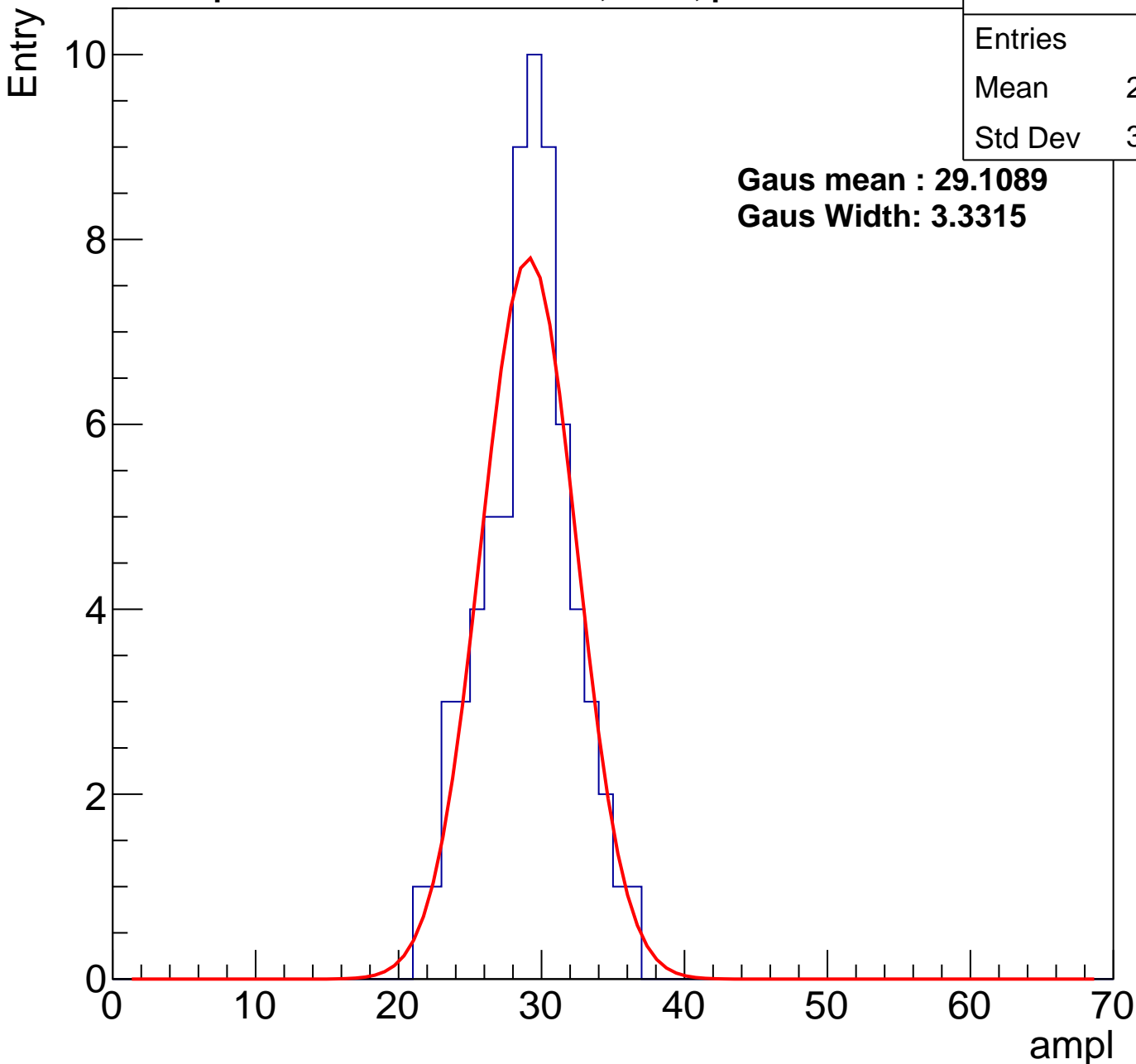
# B1L100S, U6-ch56, adc0

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	67
Mean	28.55
Std Dev	3.168

**Gaus mean : 29.1089**

**Gaus Width: 3.3315**



# B1L100S, U6-ch56, adc1

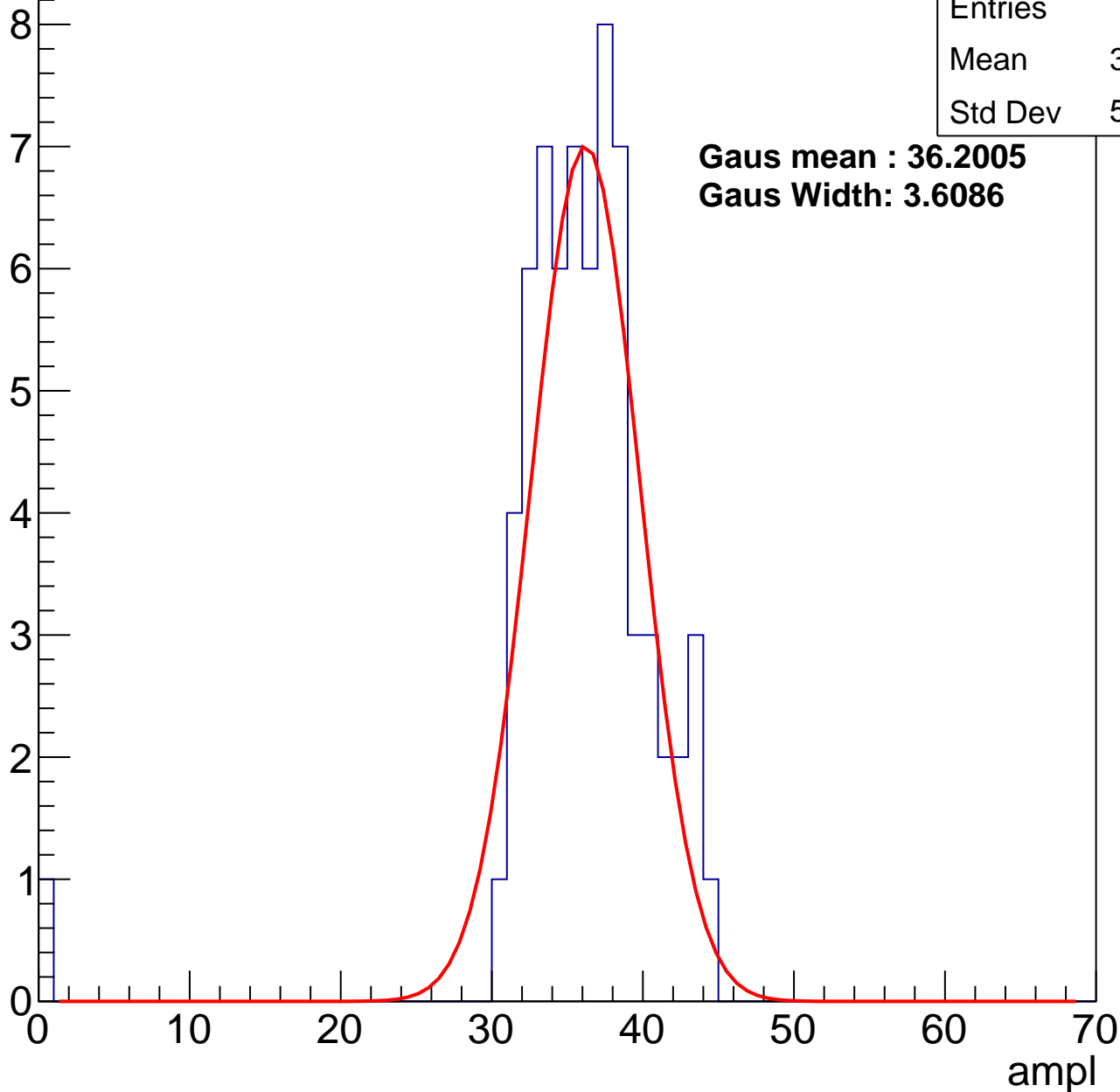
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	67
Mean	35.52
Std Dev	5.532

**Gaus mean : 36.2005**

**Gaus Width: 3.6086**



# B1L100S, U6-ch56, adc2

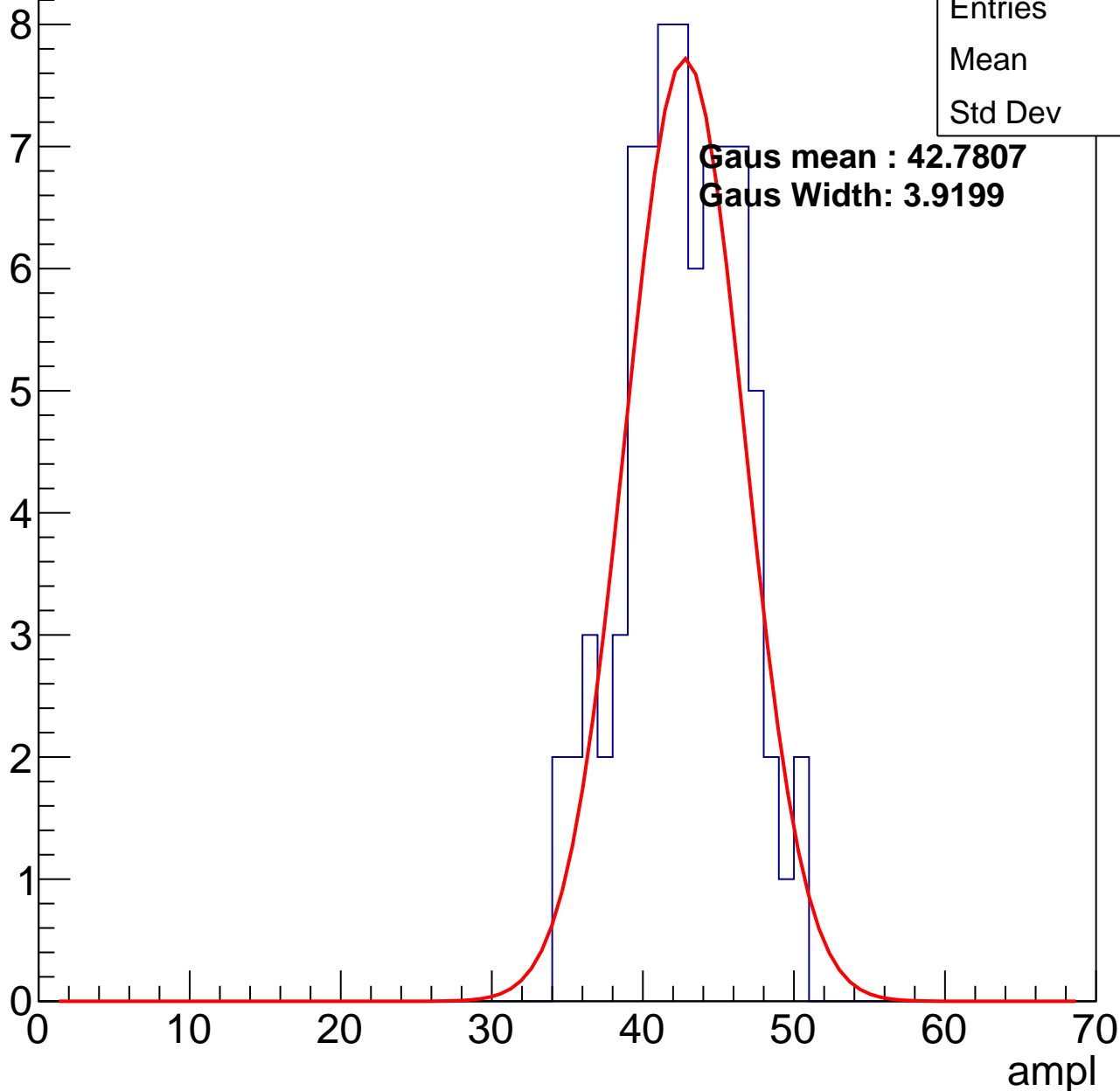
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	79
Mean	42.2
Std Dev	3.75

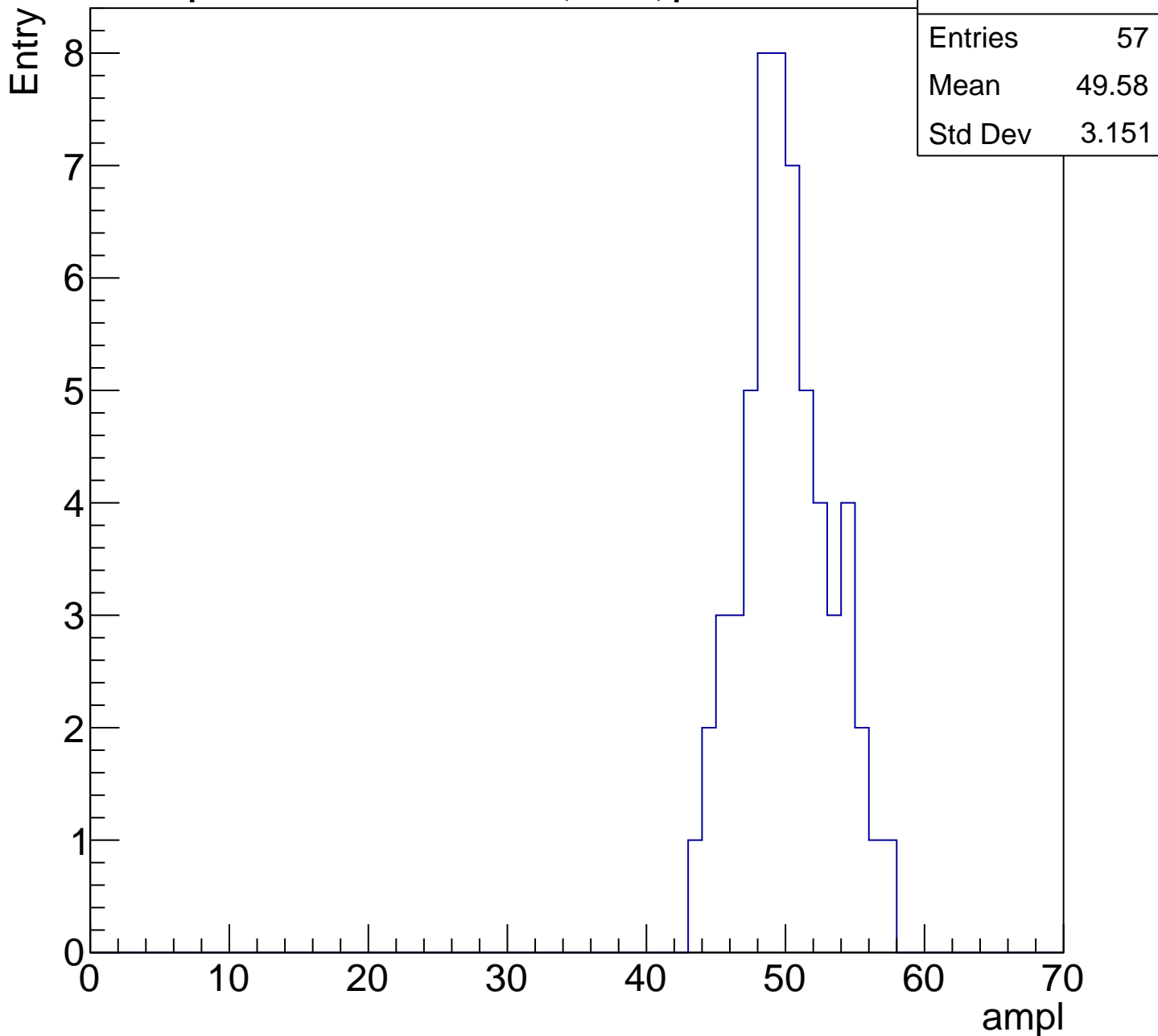
**Gaus mean : 42.7807**

**Gaus Width: 3.9199**



# B1L100S, U6-ch56, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

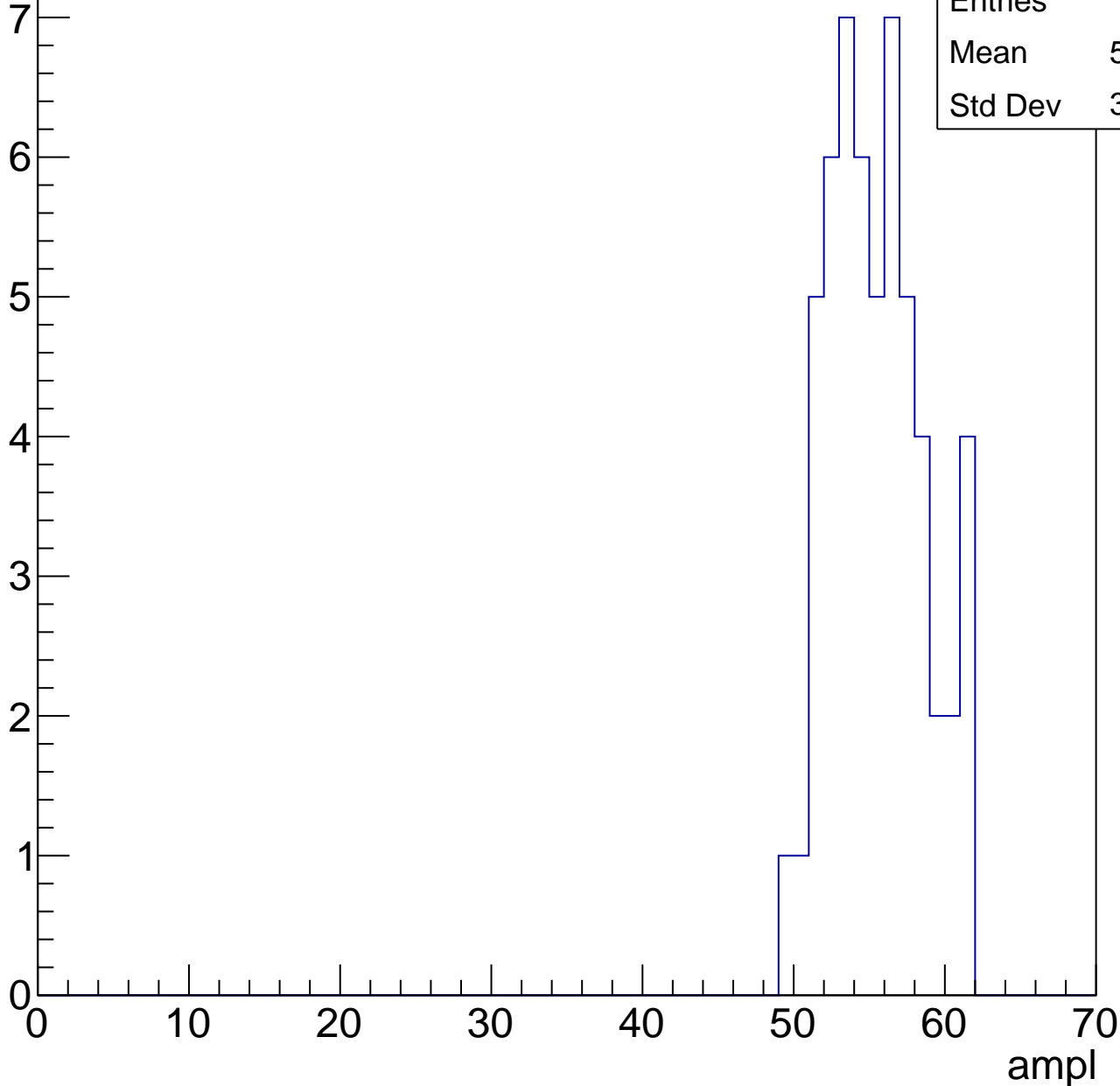


# B1L100S, U6-ch56, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	55
Mean	55.04
Std Dev	3.069



# B1L100S, U6-ch56, adc5

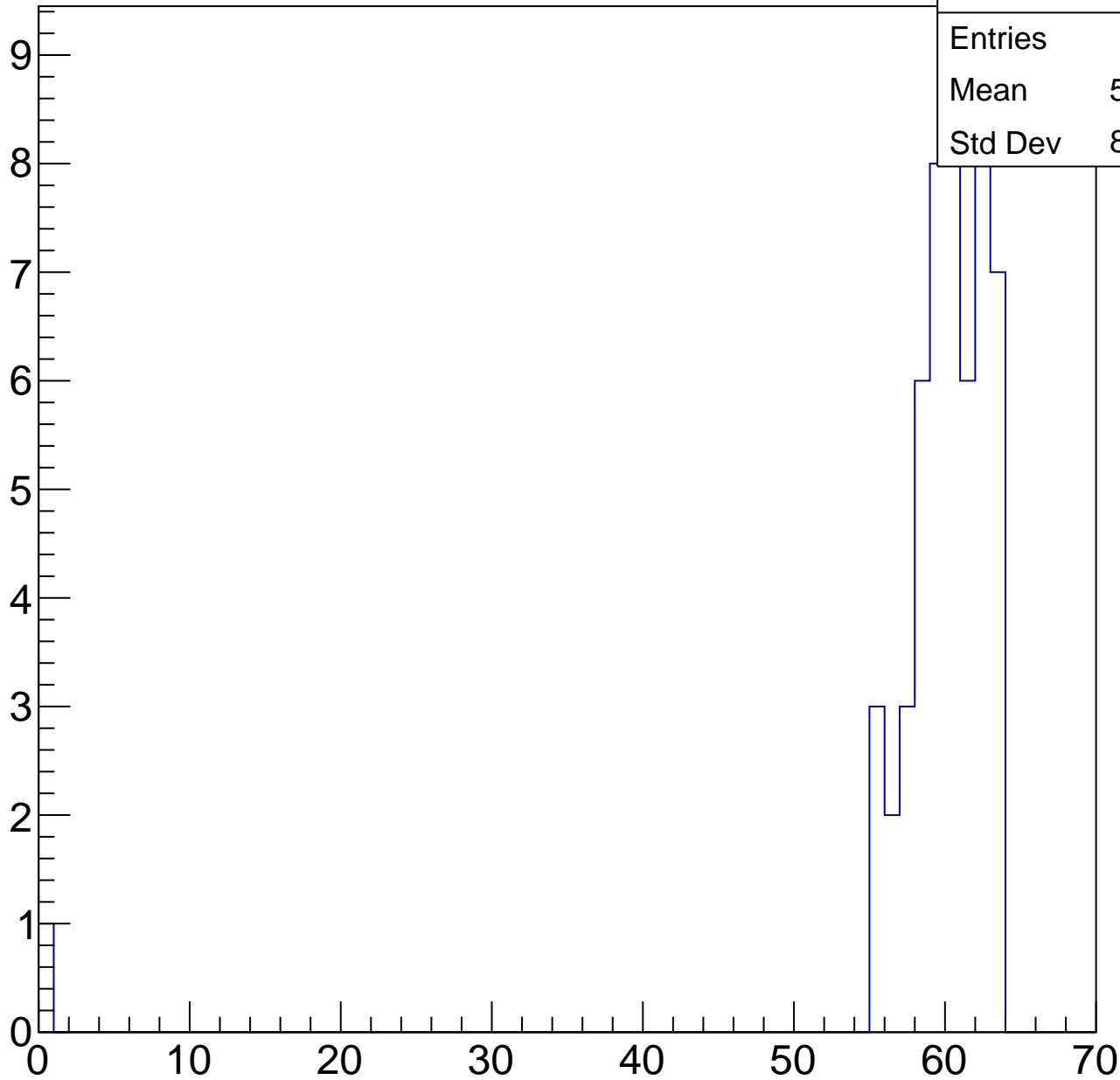
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	53
Mean	58.74
Std Dev	8.452

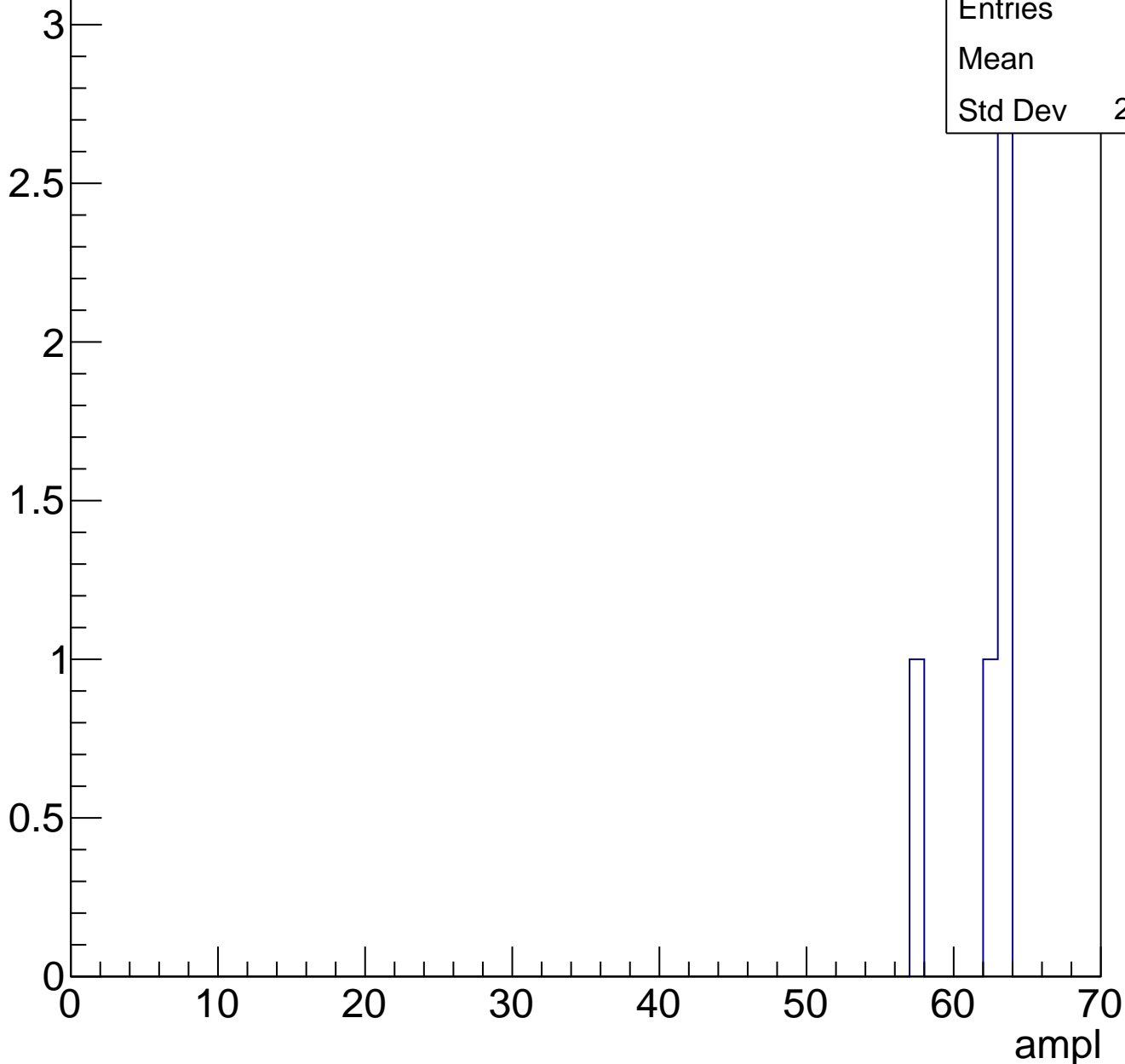
ampl



# B1L100S, U6-ch56, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry





# B1L100S, U6-ch56, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L100S, U6-ch57, adc0

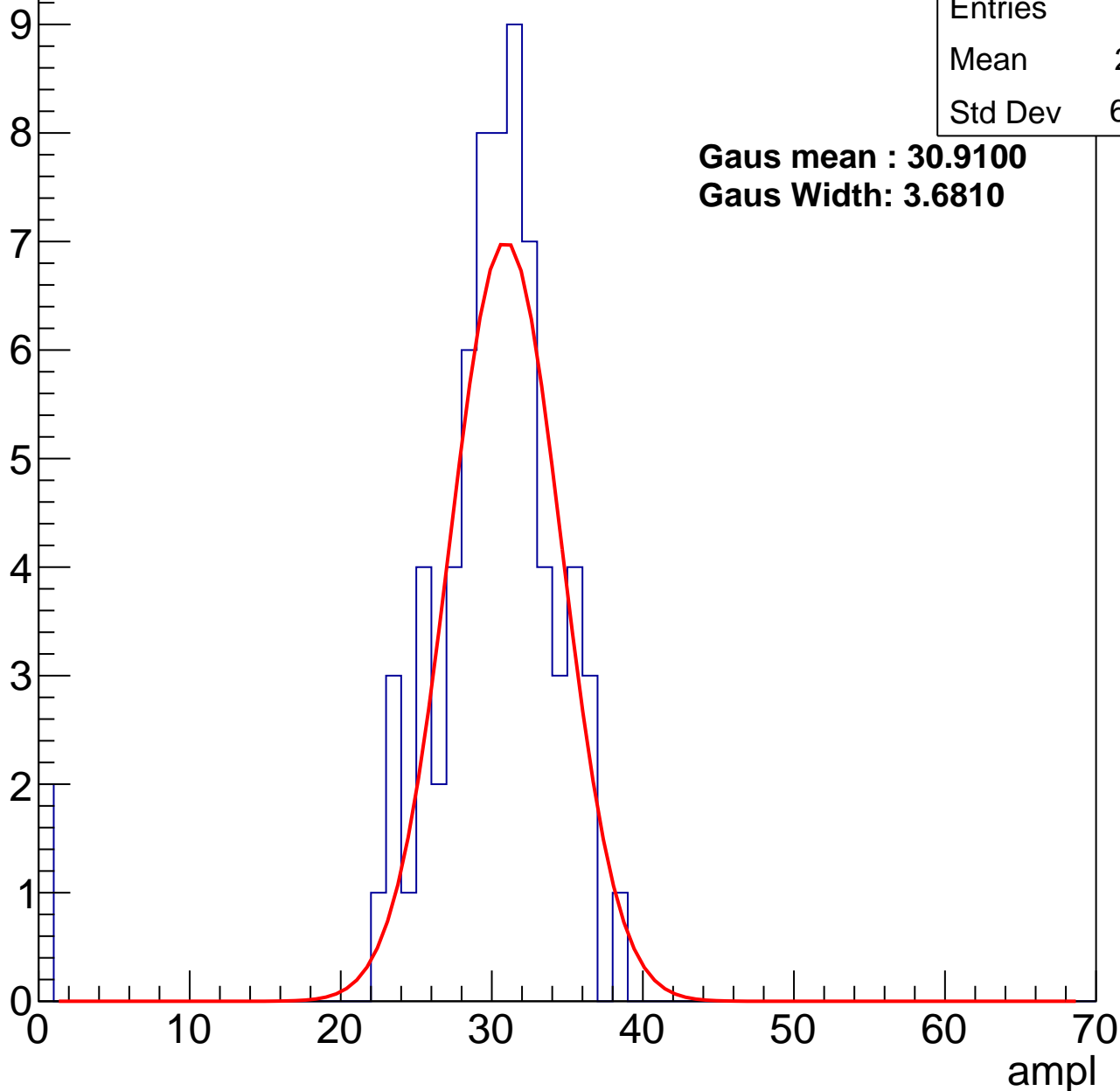
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	70
Mean	29.11
Std Dev	6.077

**Gaus mean : 30.9100**

**Gaus Width: 3.6810**



# B1L100S, U6-ch57, adc1

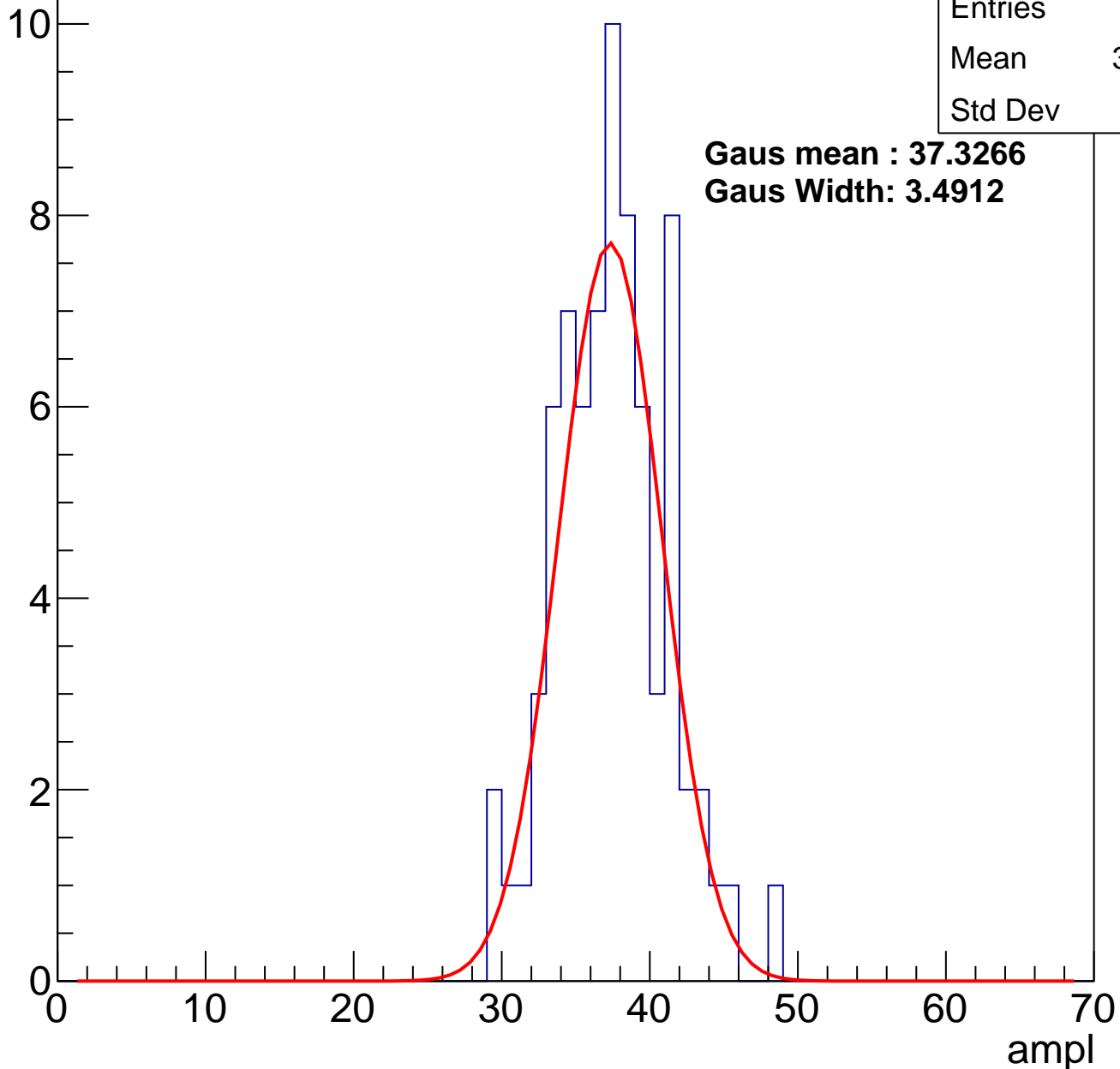
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	75
Mean	37.01
Std Dev	3.69

**Gaus mean : 37.3266**

**Gaus Width: 3.4912**

Entry



# B1L100S, U6-ch57, adc2

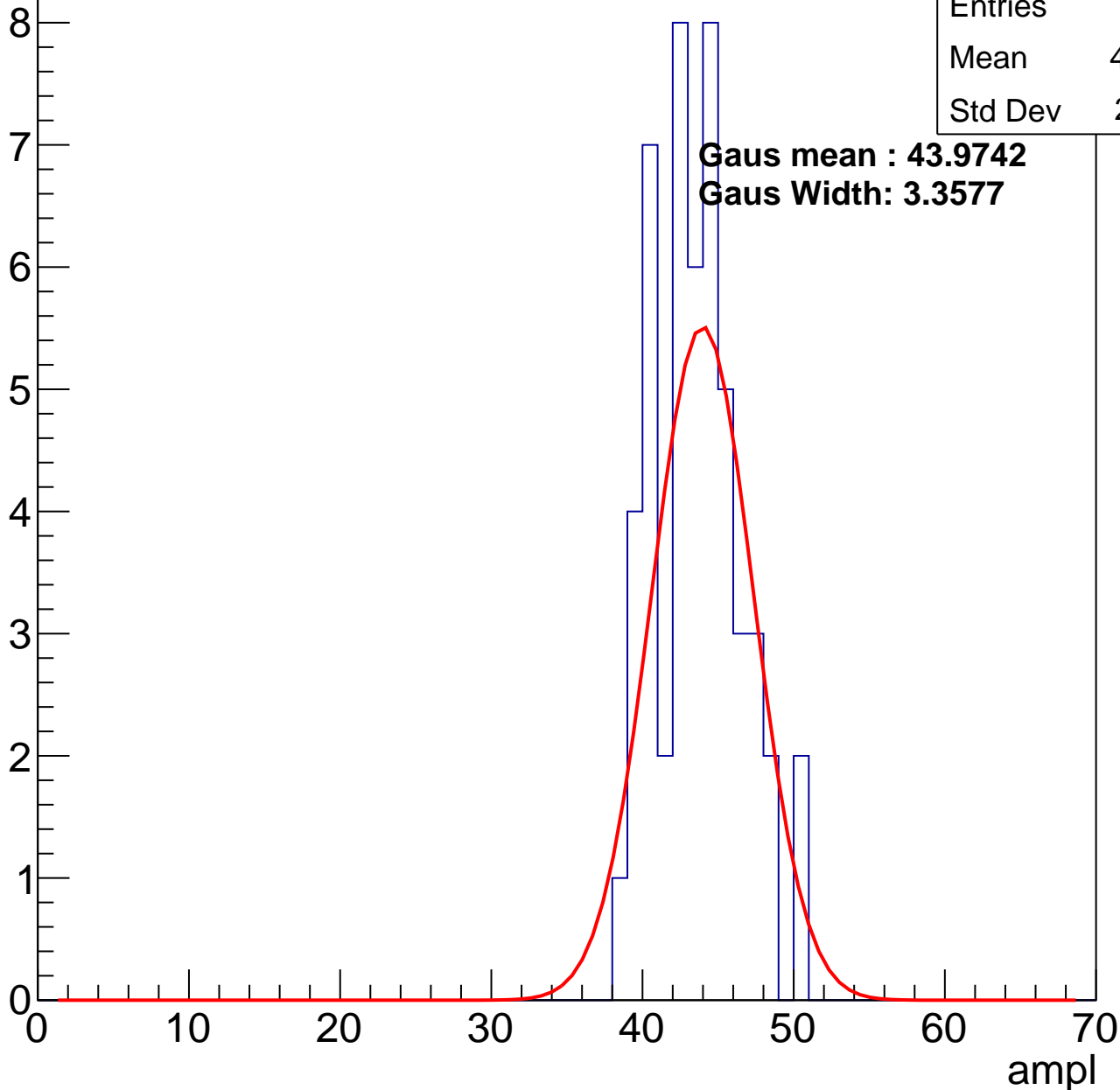
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	51
Mean	43.18
Std Dev	2.861

**Gaus mean : 43.9742**

**Gaus Width: 3.3577**

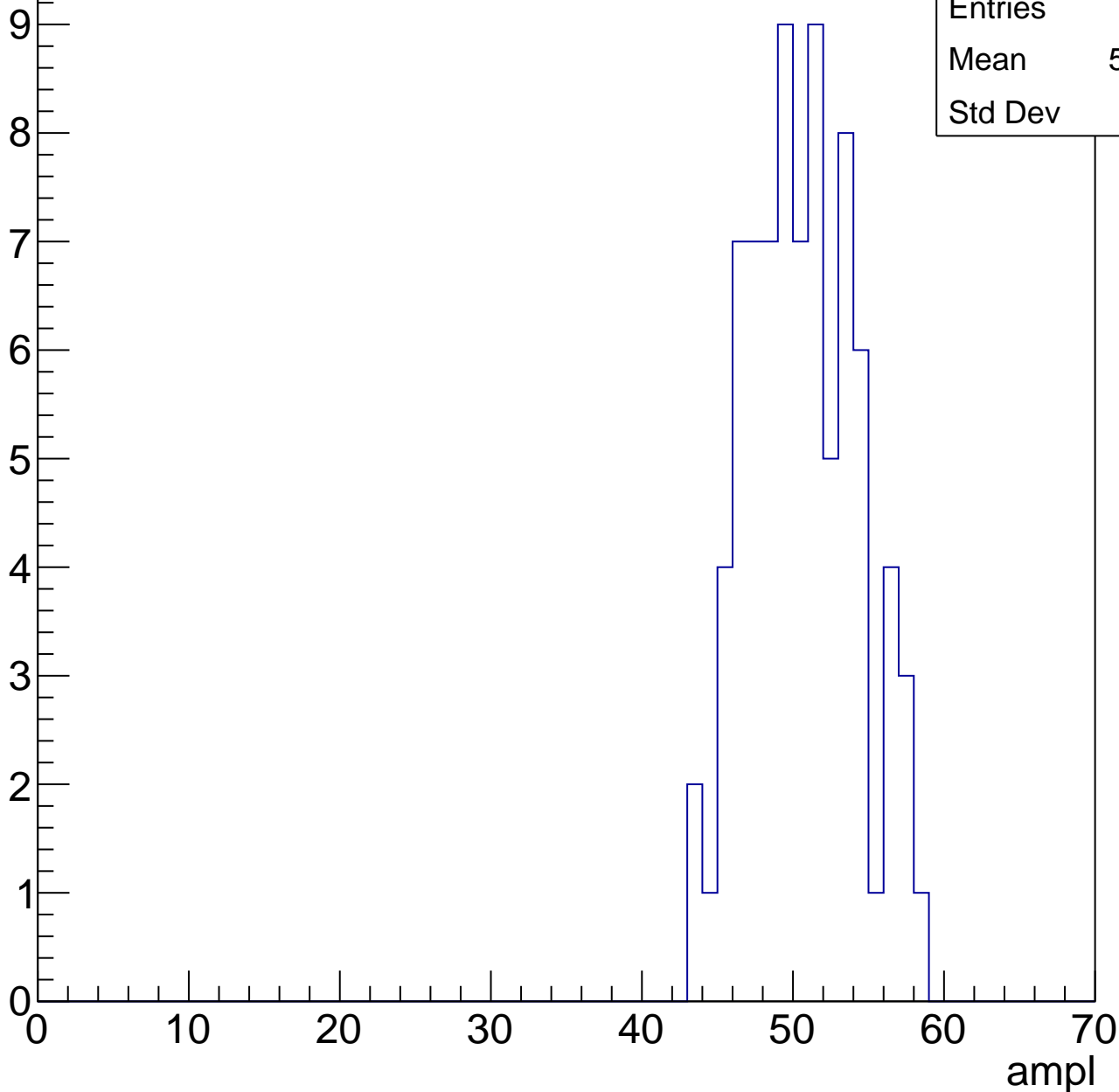


# B1L100S, U6-ch57, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

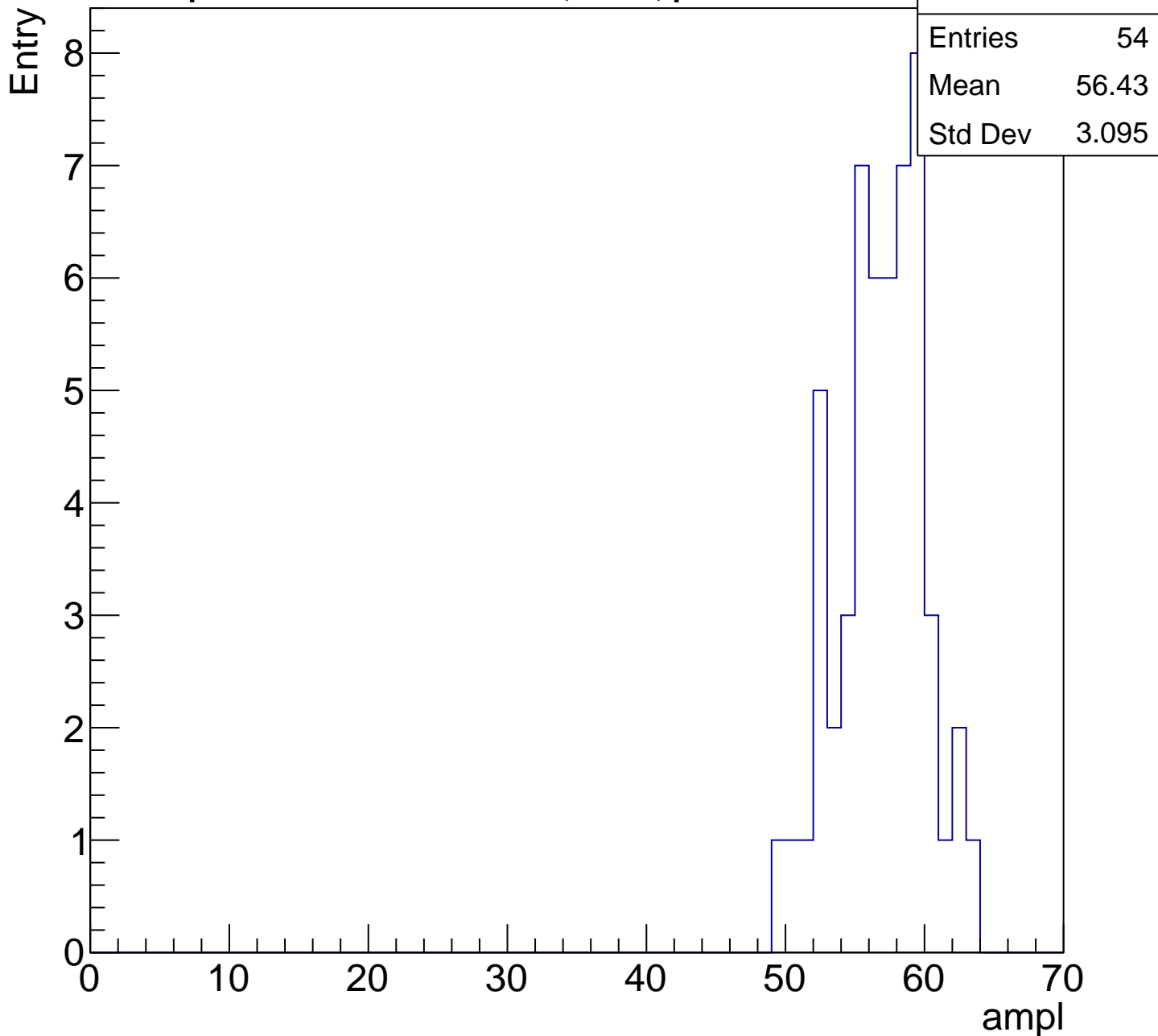
Entry

Entries	81
Mean	50.16
Std Dev	3.55



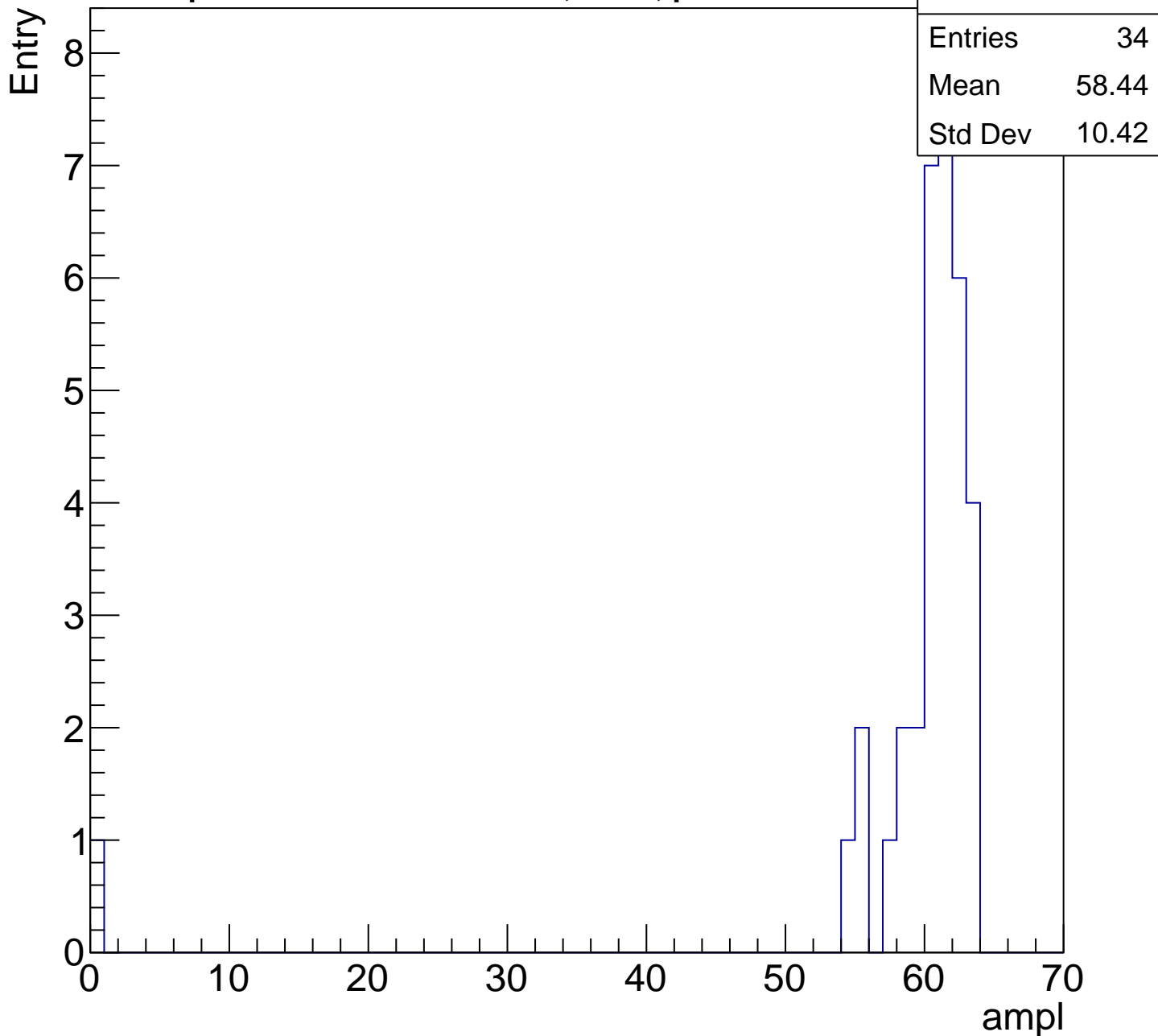
# B1L100S, U6-ch57, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2



# B1L100S, U6-ch57, adc5

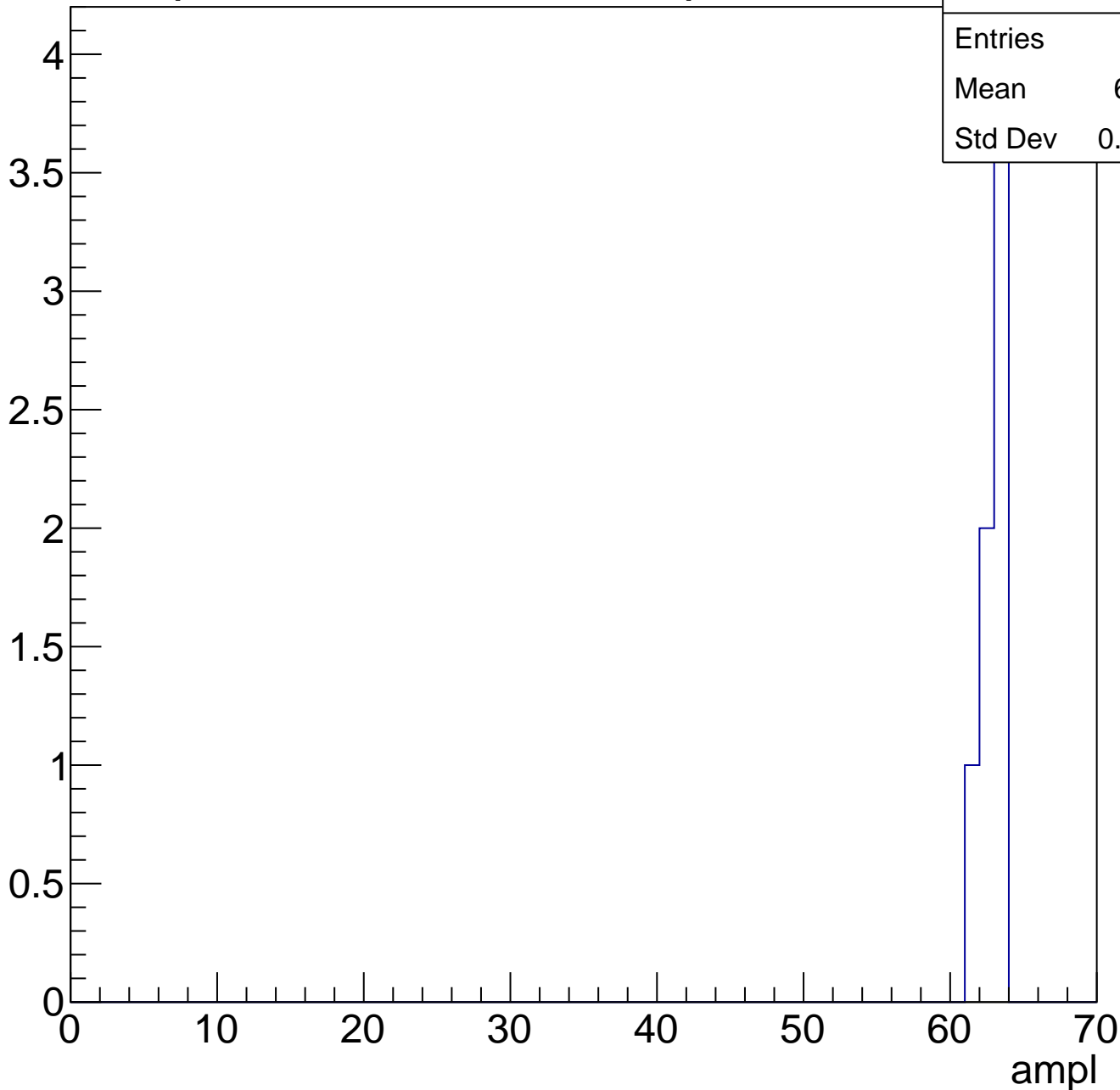
calib\_packv5\_042523\_0143.root, FC#4, port A2



# B1L100S, U6-ch57, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry





# B1L100S, U6-ch57, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



# B1L100S, U6-ch58, adc0

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	87
Mean	27.85
Std Dev	4.74

**Gaus mean : 28.0772**

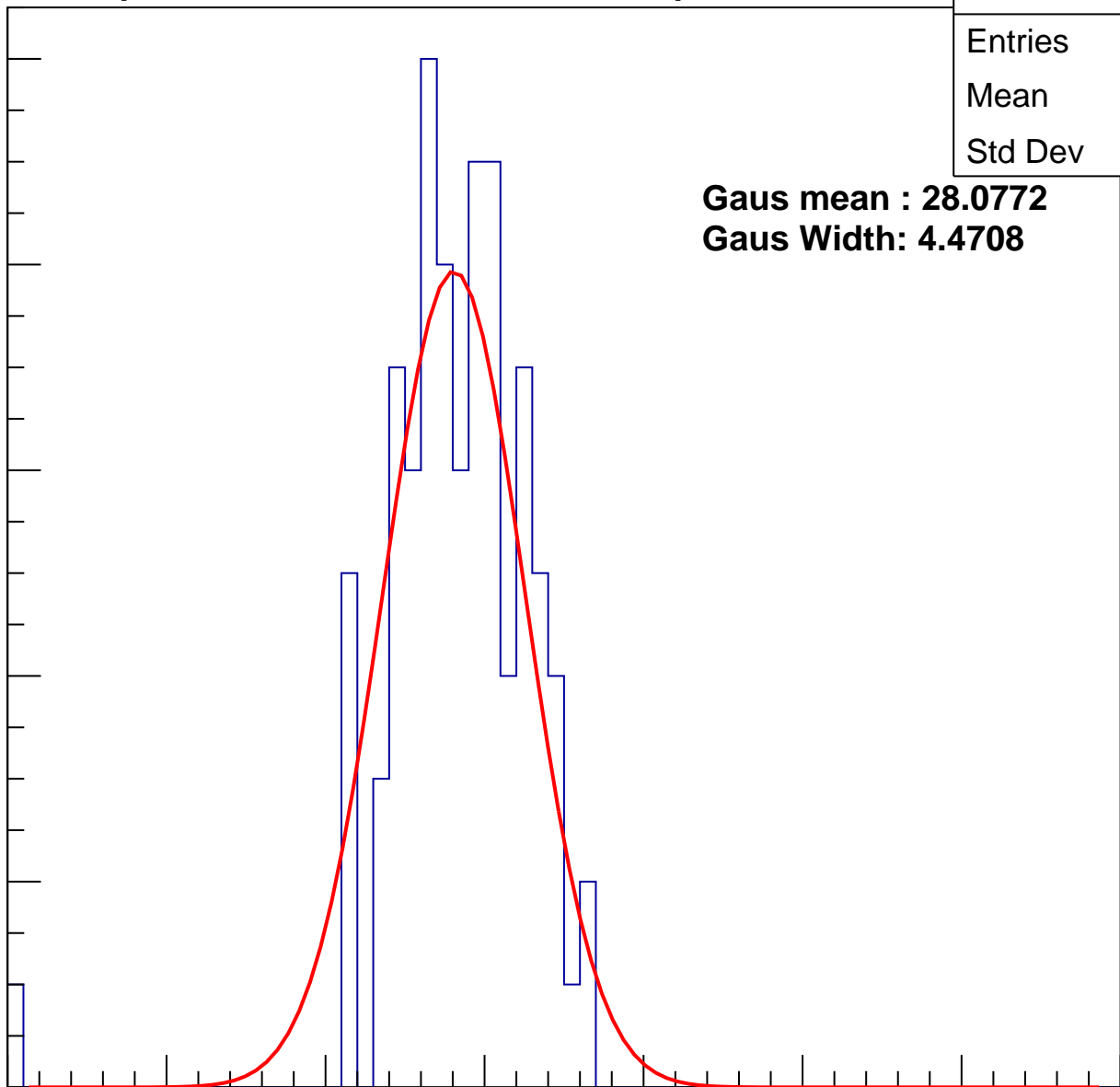
**Gaus Width: 4.4708**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L100S, U6-ch58, adc1

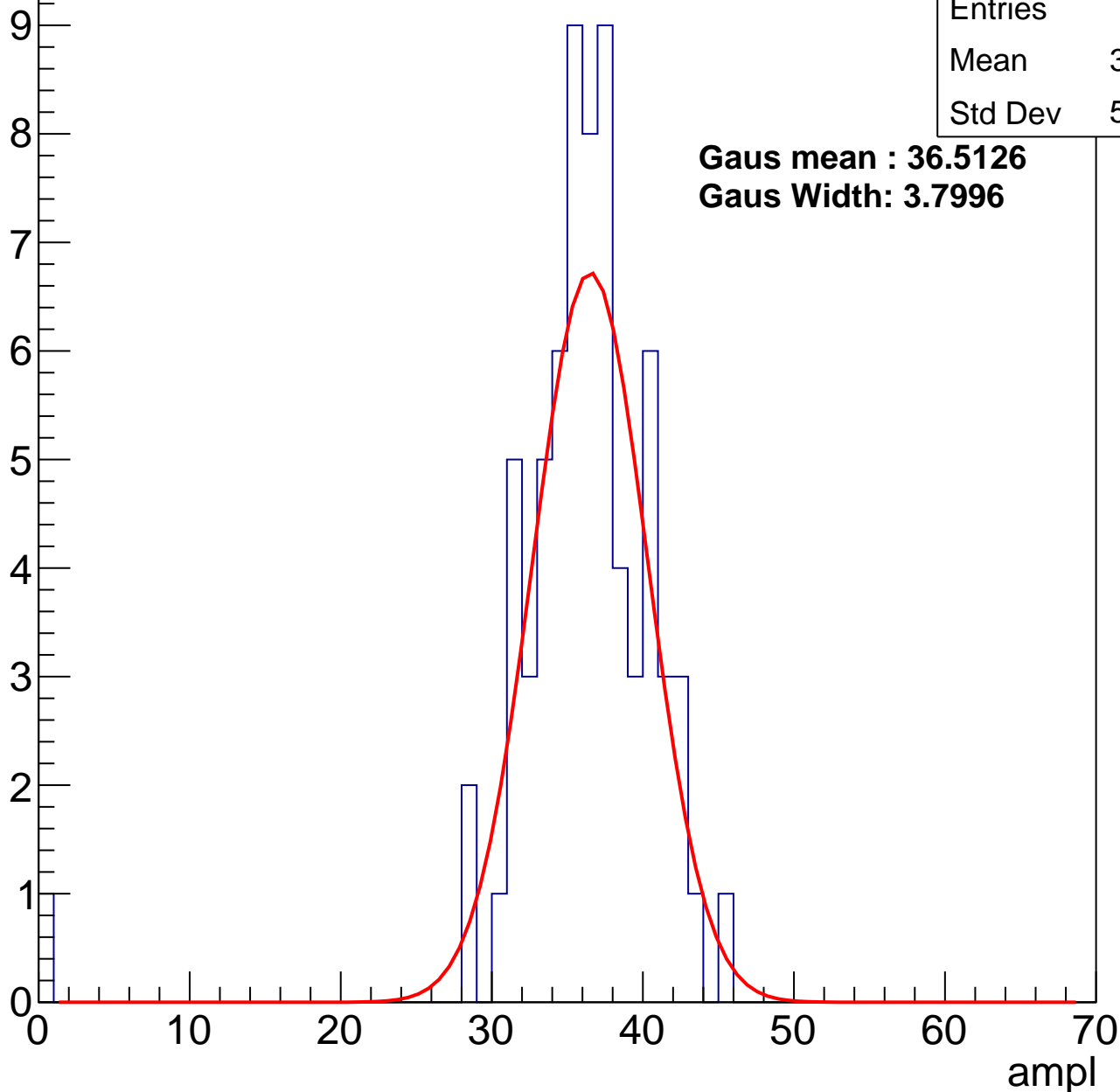
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	70
Mean	35.54
Std Dev	5.552

**Gaus mean : 36.5126**

**Gaus Width: 3.7996**



# B1L100S, U6-ch58, adc2

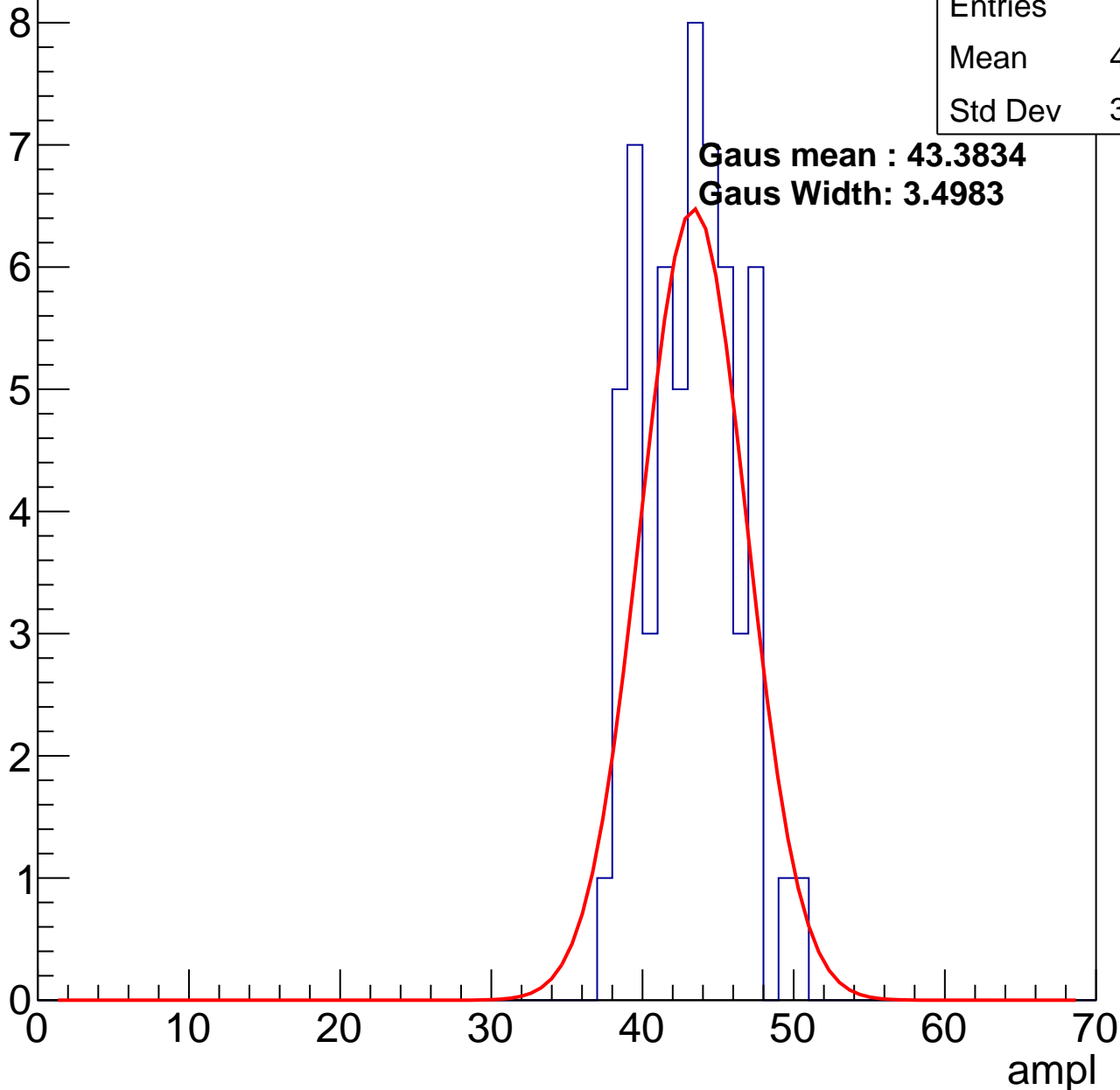
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	59
Mean	42.66
Std Dev	3.084

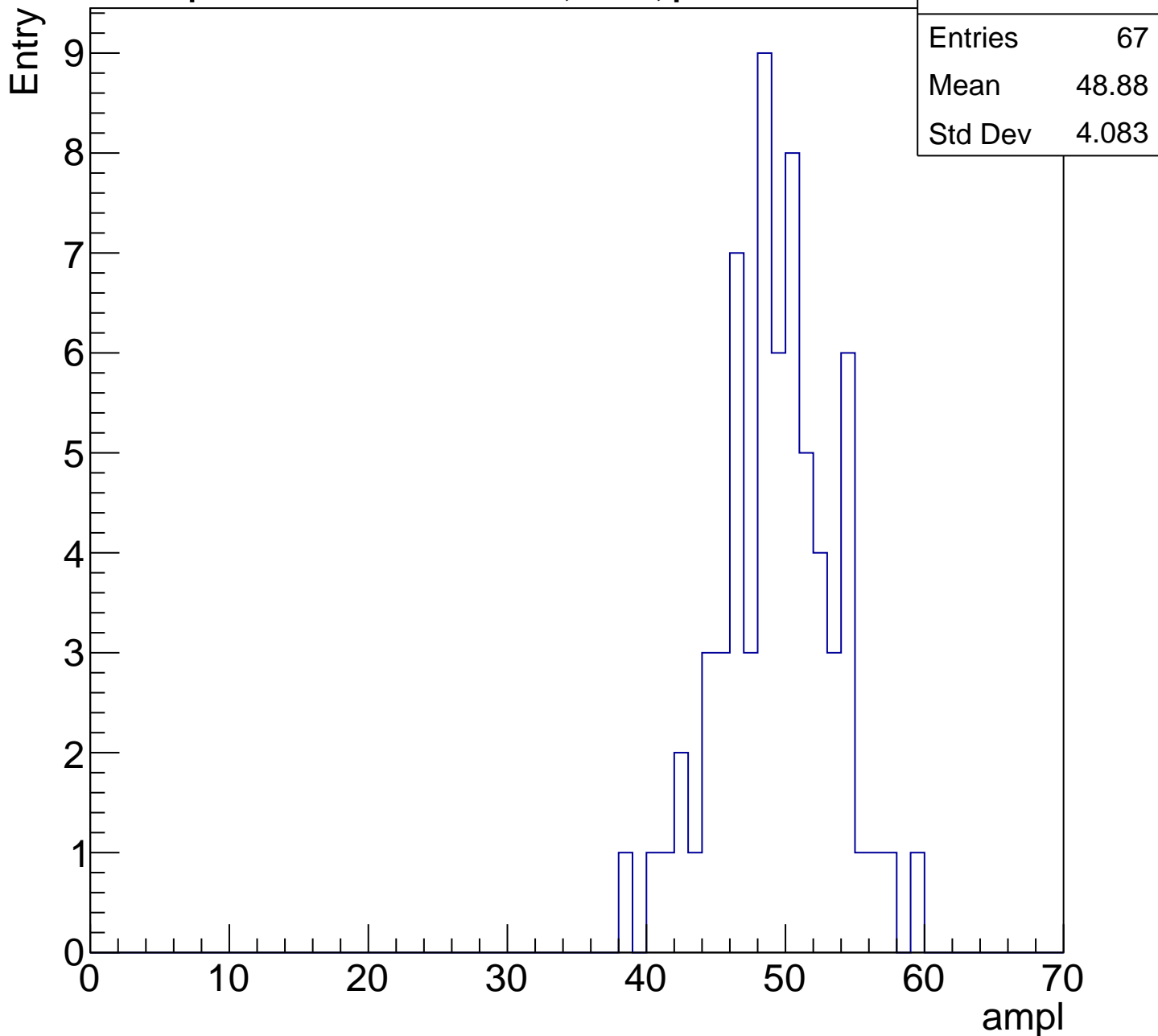
**Gaus mean : 43.3834**

**Gaus Width: 3.4983**



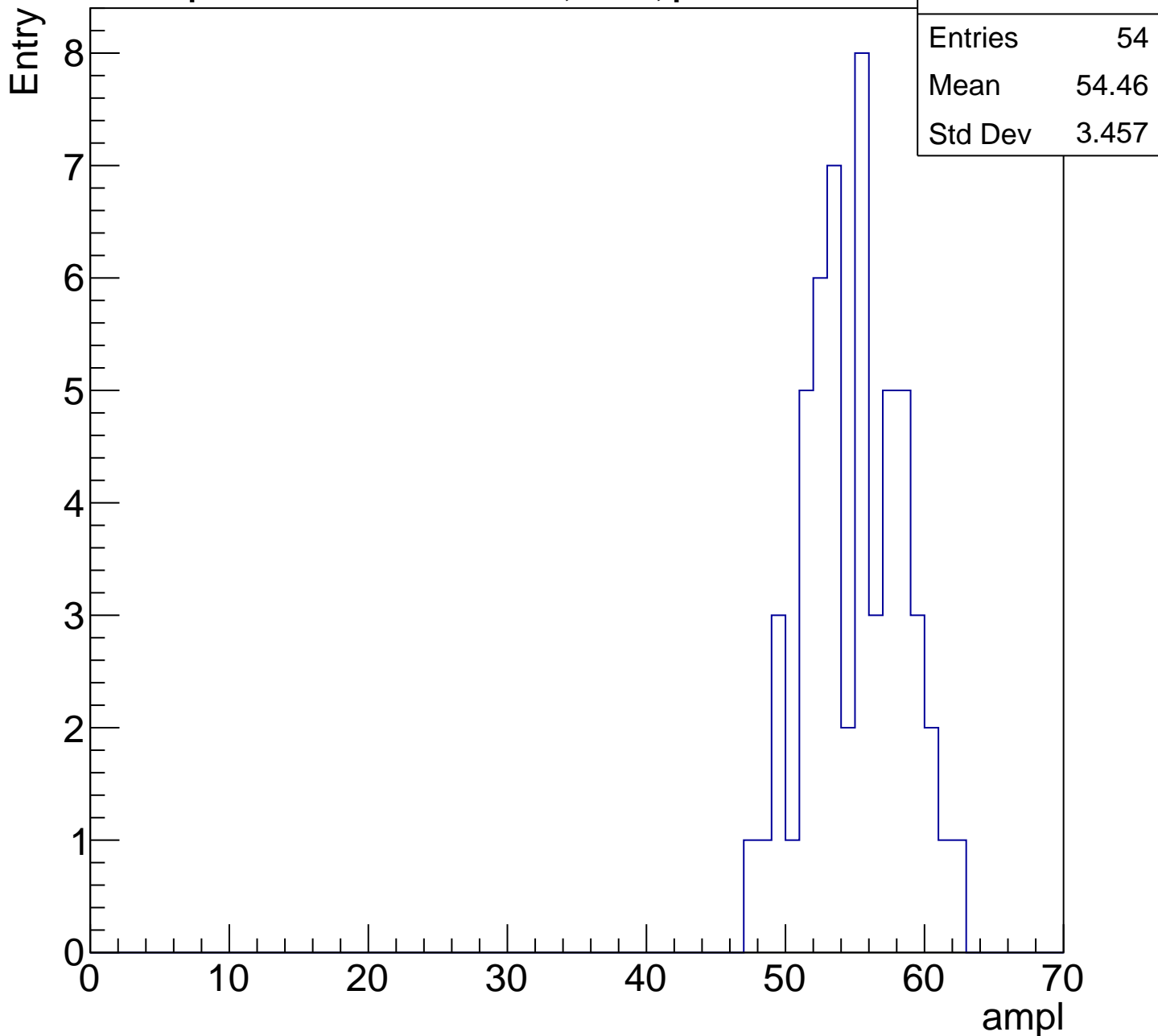
# B1L100S, U6-ch58, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2



# B1L100S, U6-ch58, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2



# B1L100S, U6-ch58, adc5

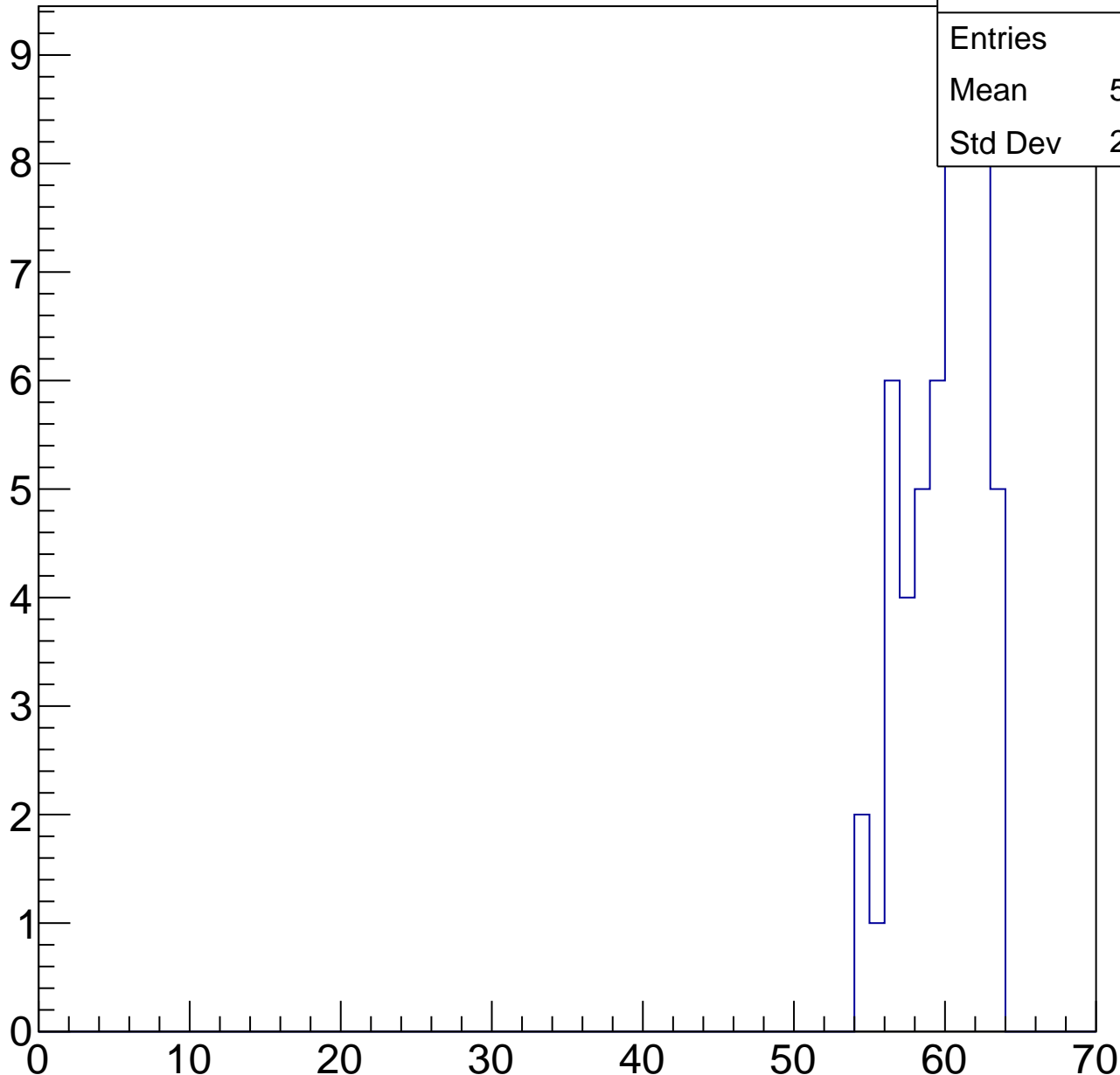
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	54
Mean	59.46
Std Dev	2.455

ampl

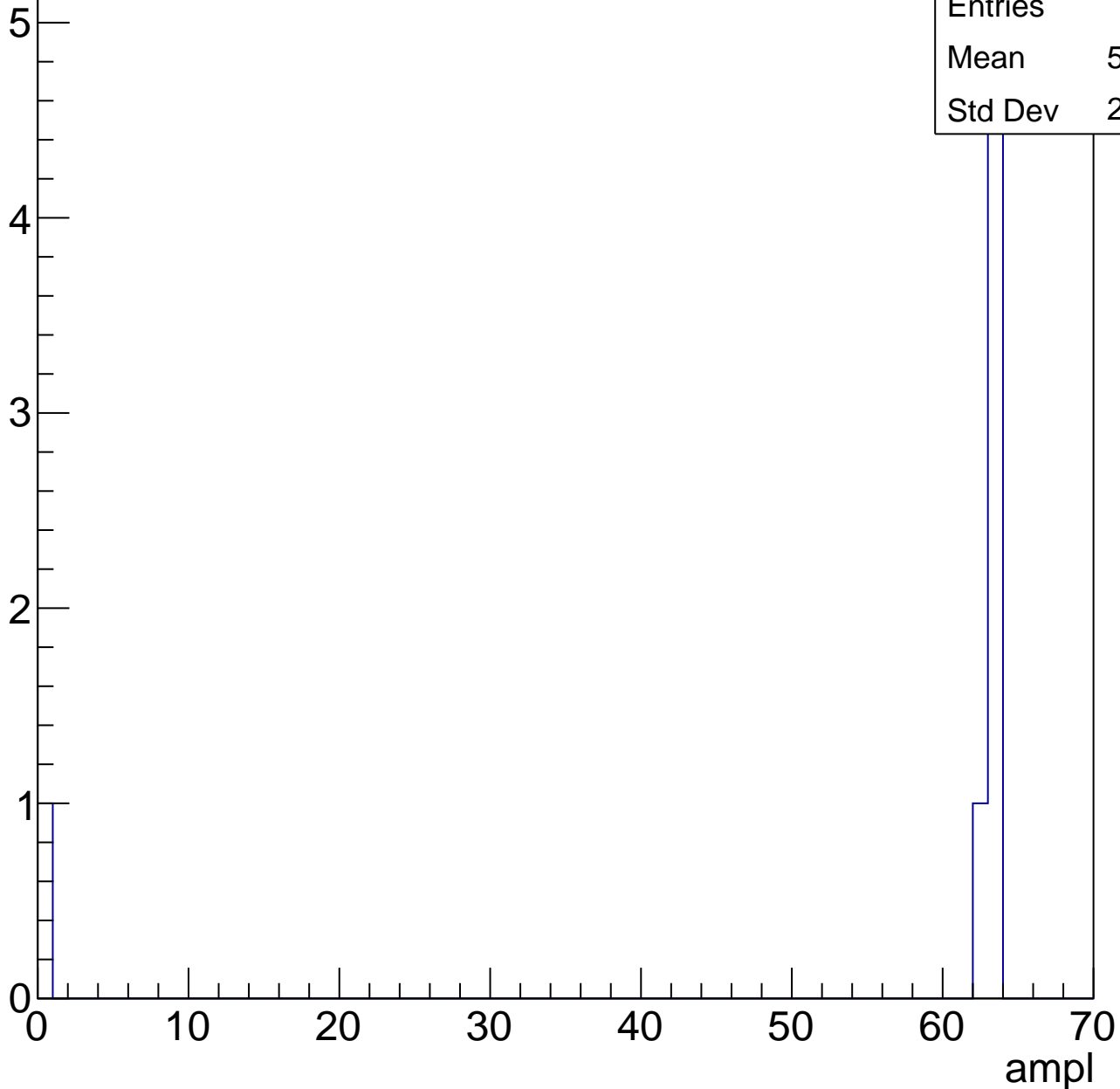


# B1L100S, U6-ch58, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	7
Mean	53.86
Std Dev	21.99





# B1L100S, U6-ch58, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L100S, U6-ch59, adc0

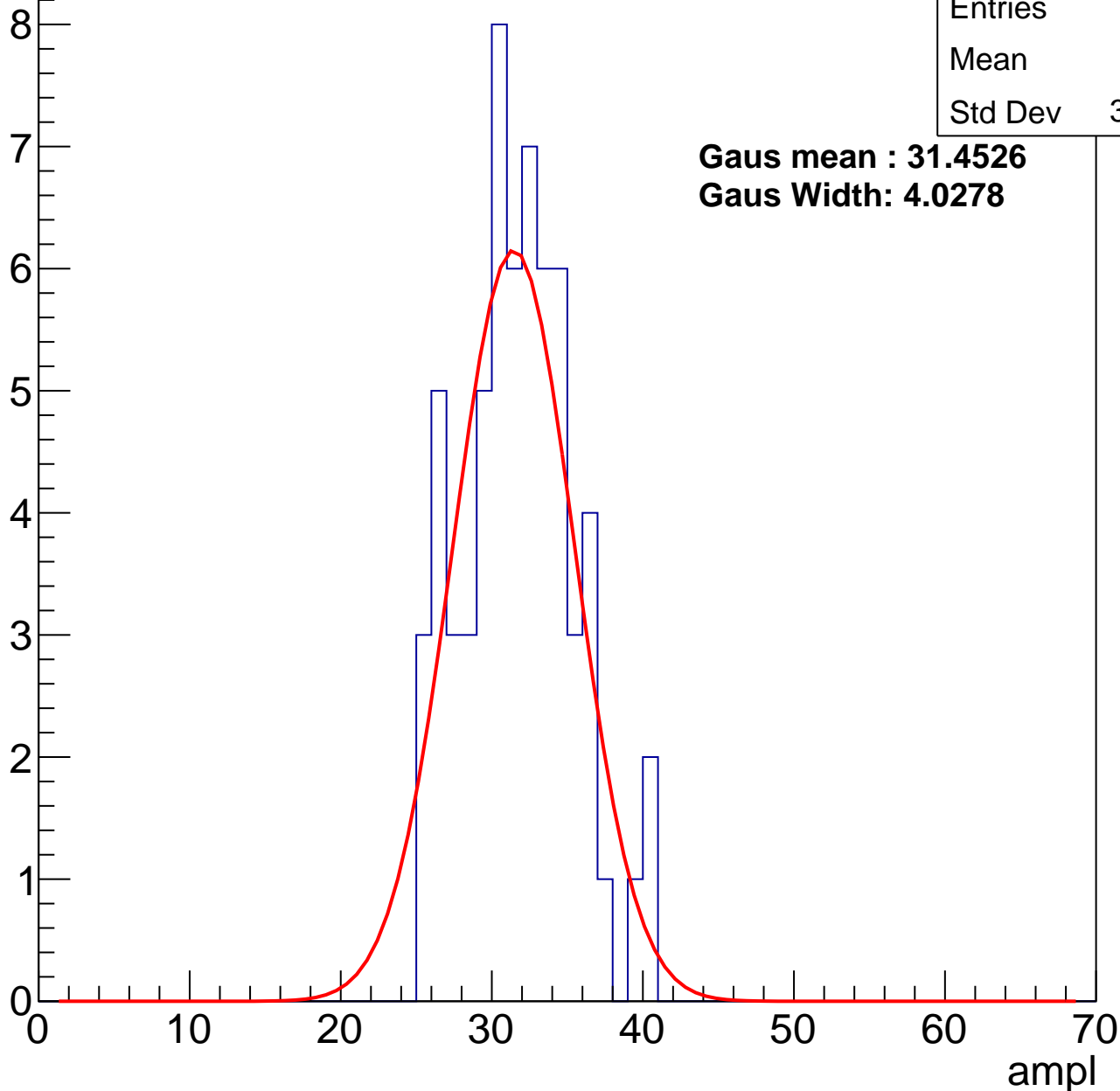
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	63
Mean	31.3
Std Dev	3.619

**Gaus mean : 31.4526**

**Gaus Width: 4.0278**



# B1L100S, U6-ch59, adc1

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	79
Mean	38.27
Std Dev	3.791

**Gaus mean : 38.8027**

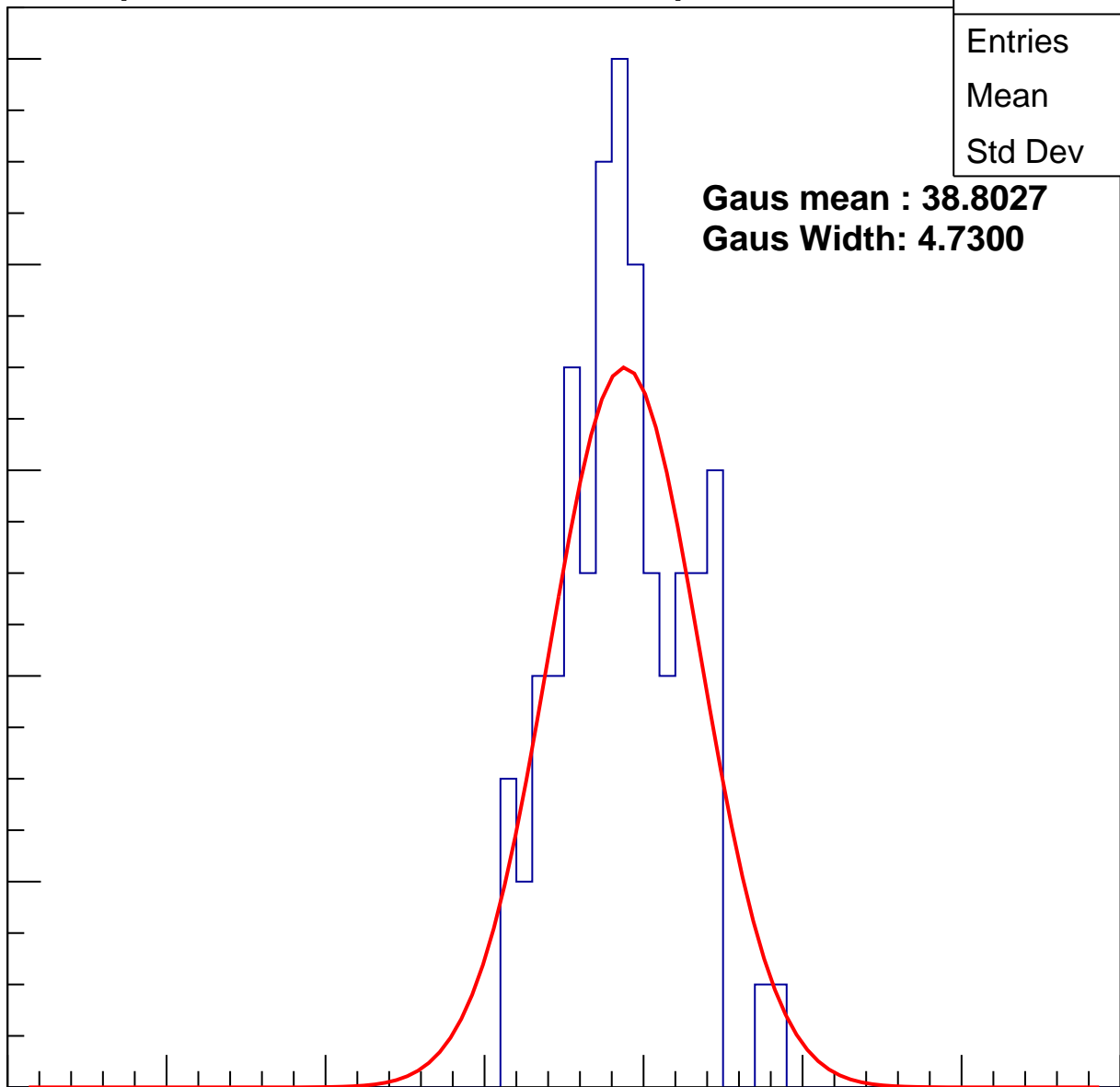
**Gaus Width: 4.7300**

Entry

10  
8  
6  
4  
2  
0

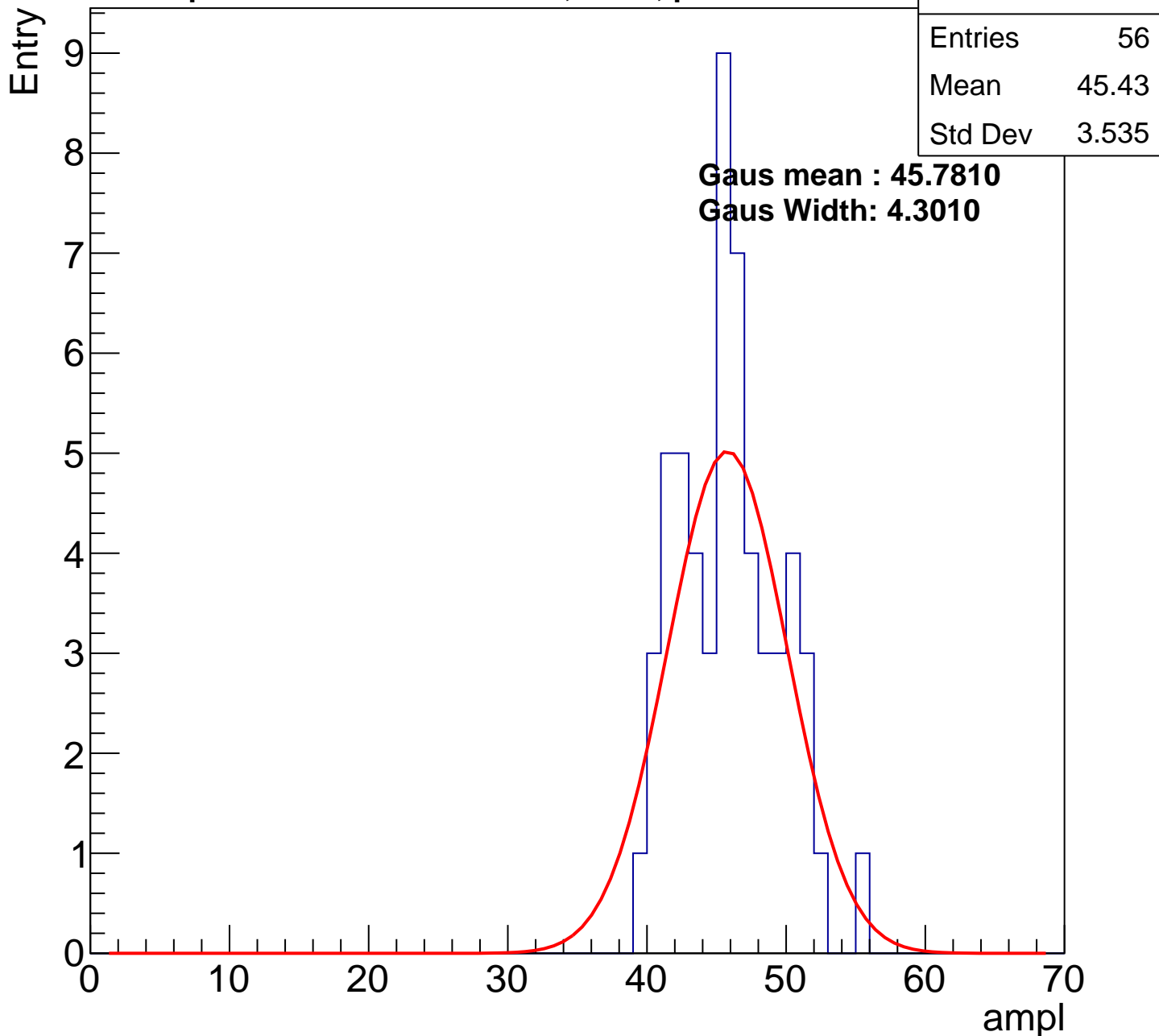
ampl

0 10 20 30 40 50 60 70



# B1L100S, U6-ch59, adc2

calib\_packv5\_042523\_0143.root, FC#4, port A2

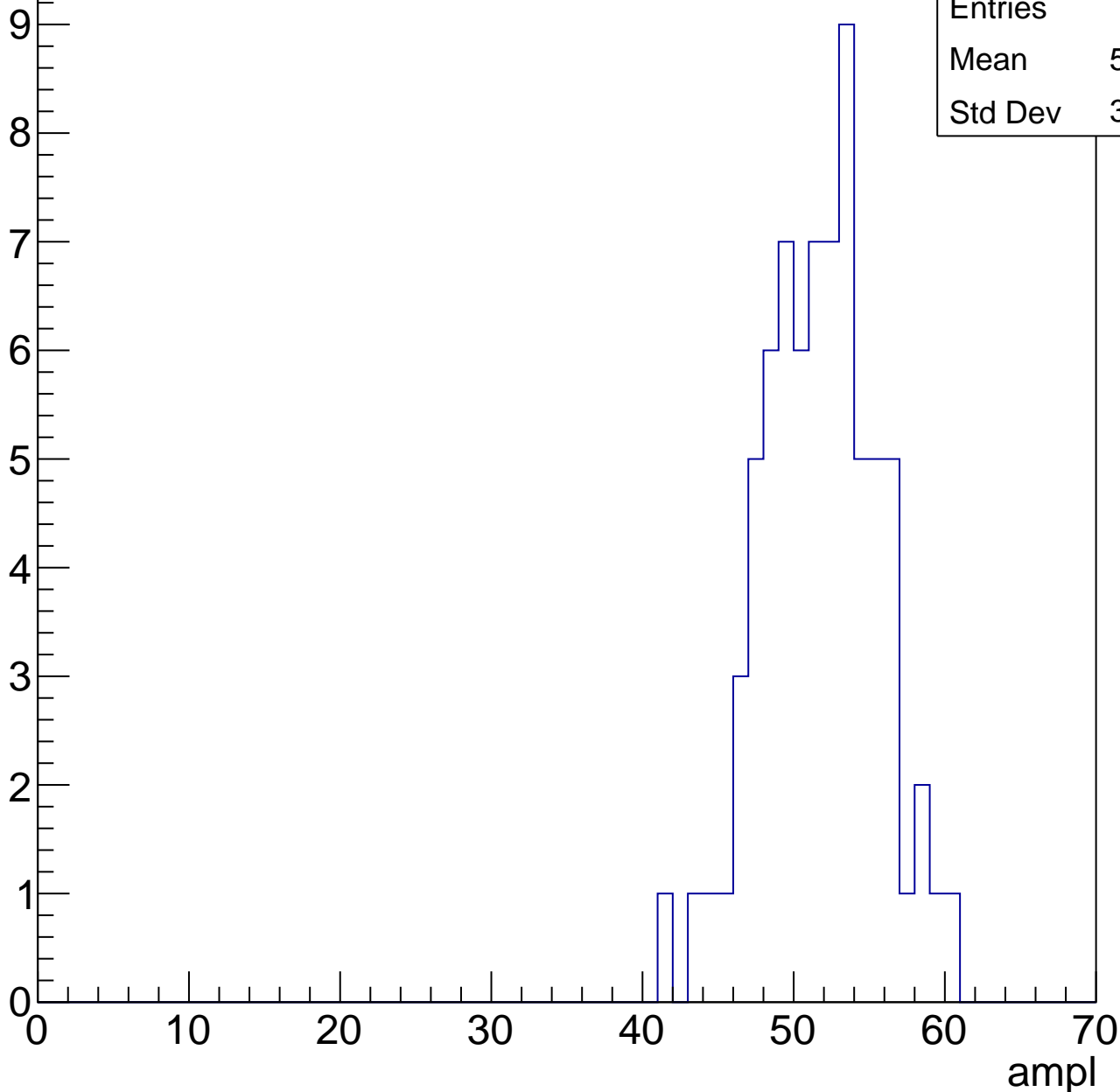


# B1L100S, U6-ch59, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	74
Mean	51.24
Std Dev	3.784

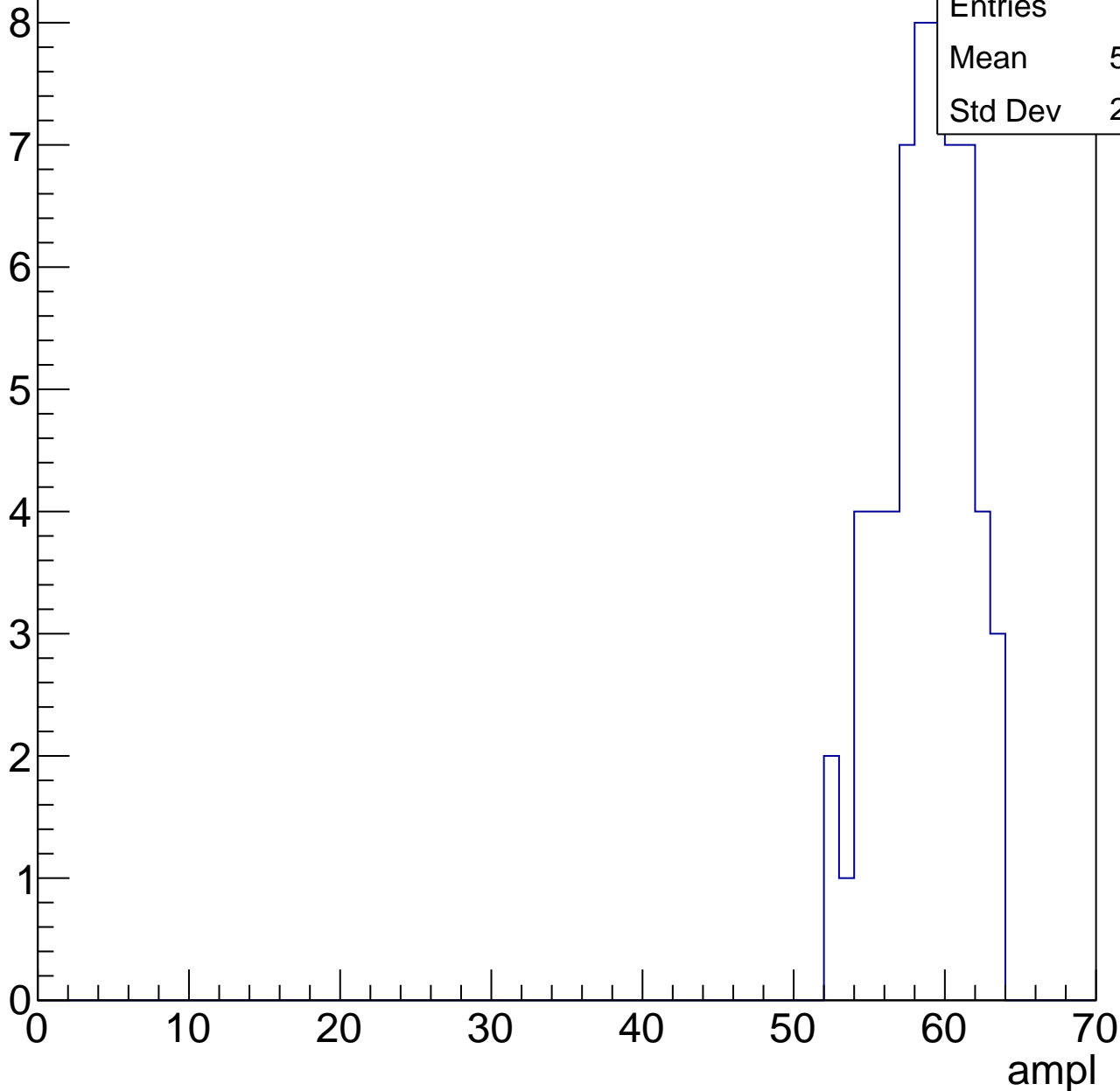


# B1L100S, U6-ch59, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	59
Mean	58.24
Std Dev	2.776

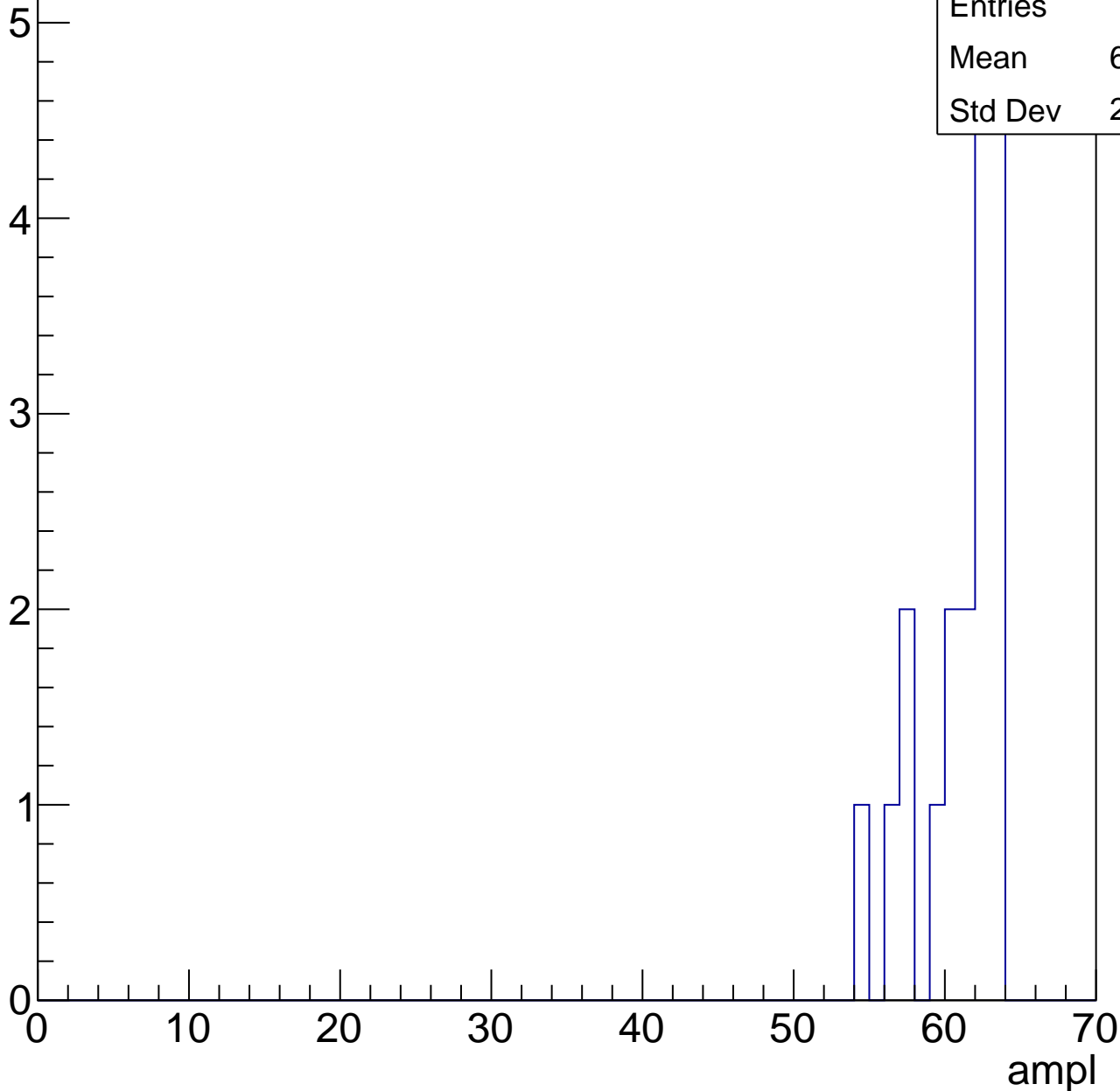


# B1L100S, U6-ch59, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

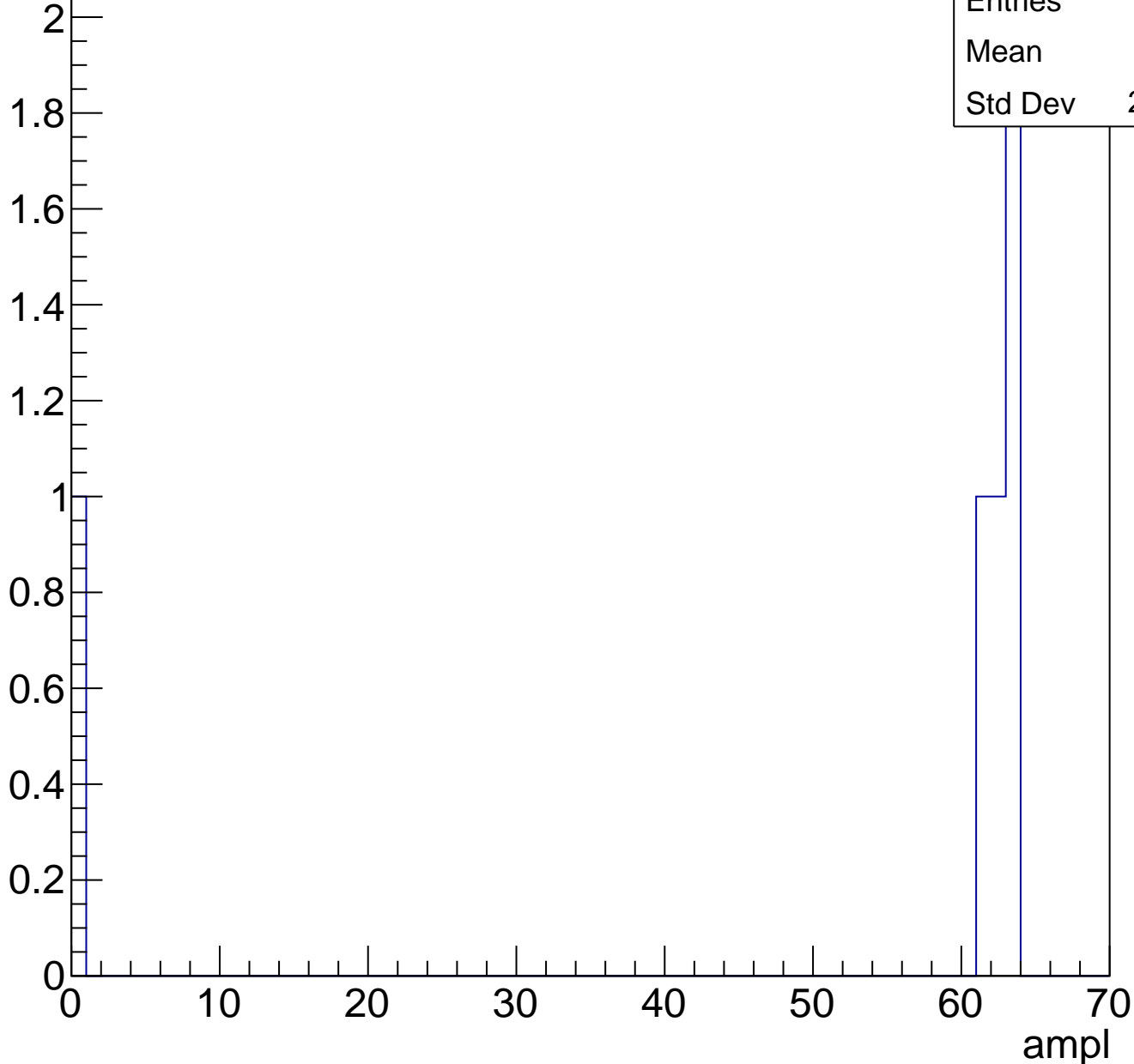
Entries	19
Mean	60.53
Std Dev	2.643



# B1L100S, U6-ch59, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry





# B1L100S, U6-ch59, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	2
Mean	0
Std Dev	0

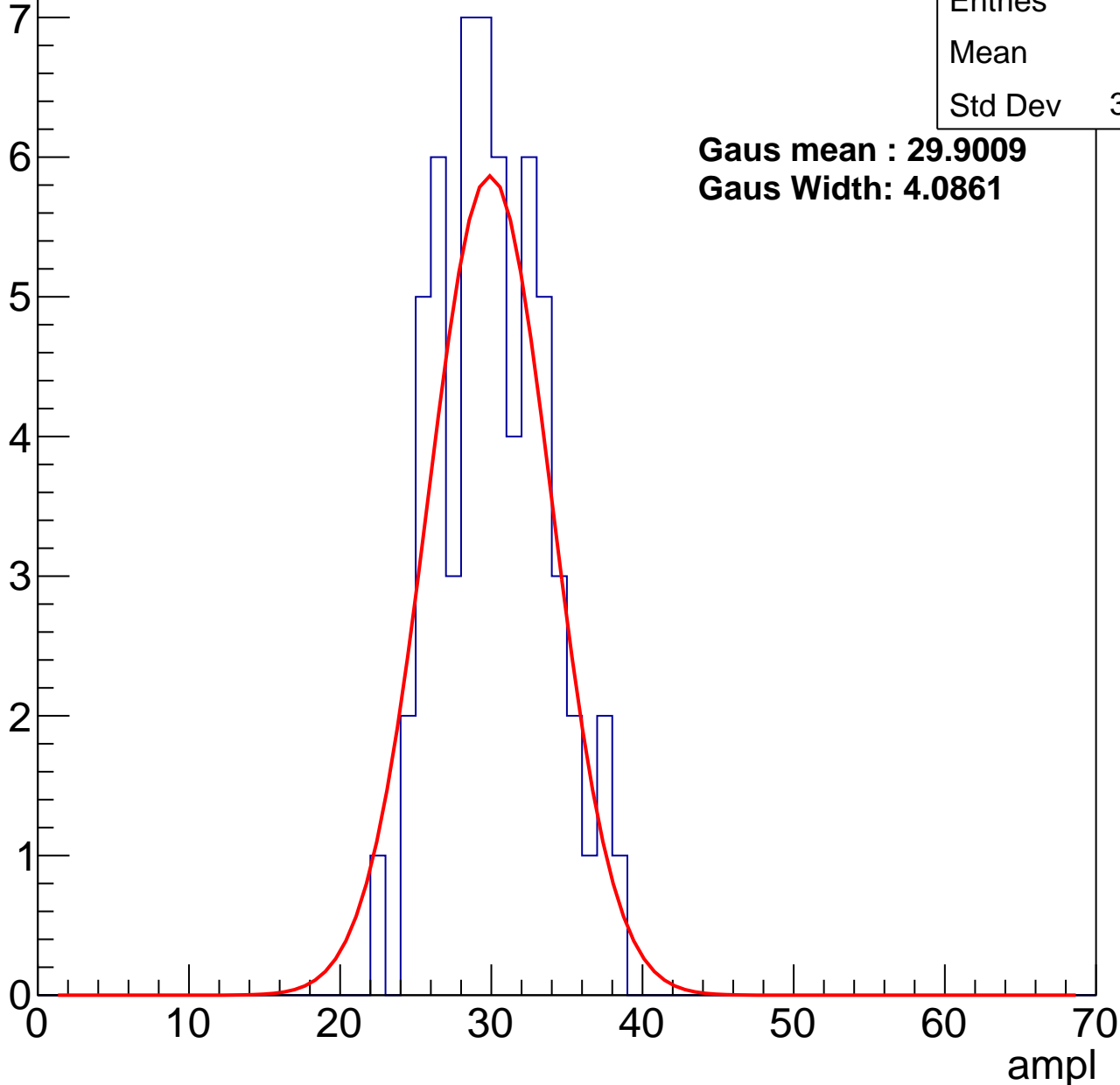
# B1L100S, U6-ch60, adc0

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	61
Mean	29.7
Std Dev	3.582

**Gaus mean : 29.9009**  
**Gaus Width: 4.0861**



# B1L100S, U6-ch60, adc1

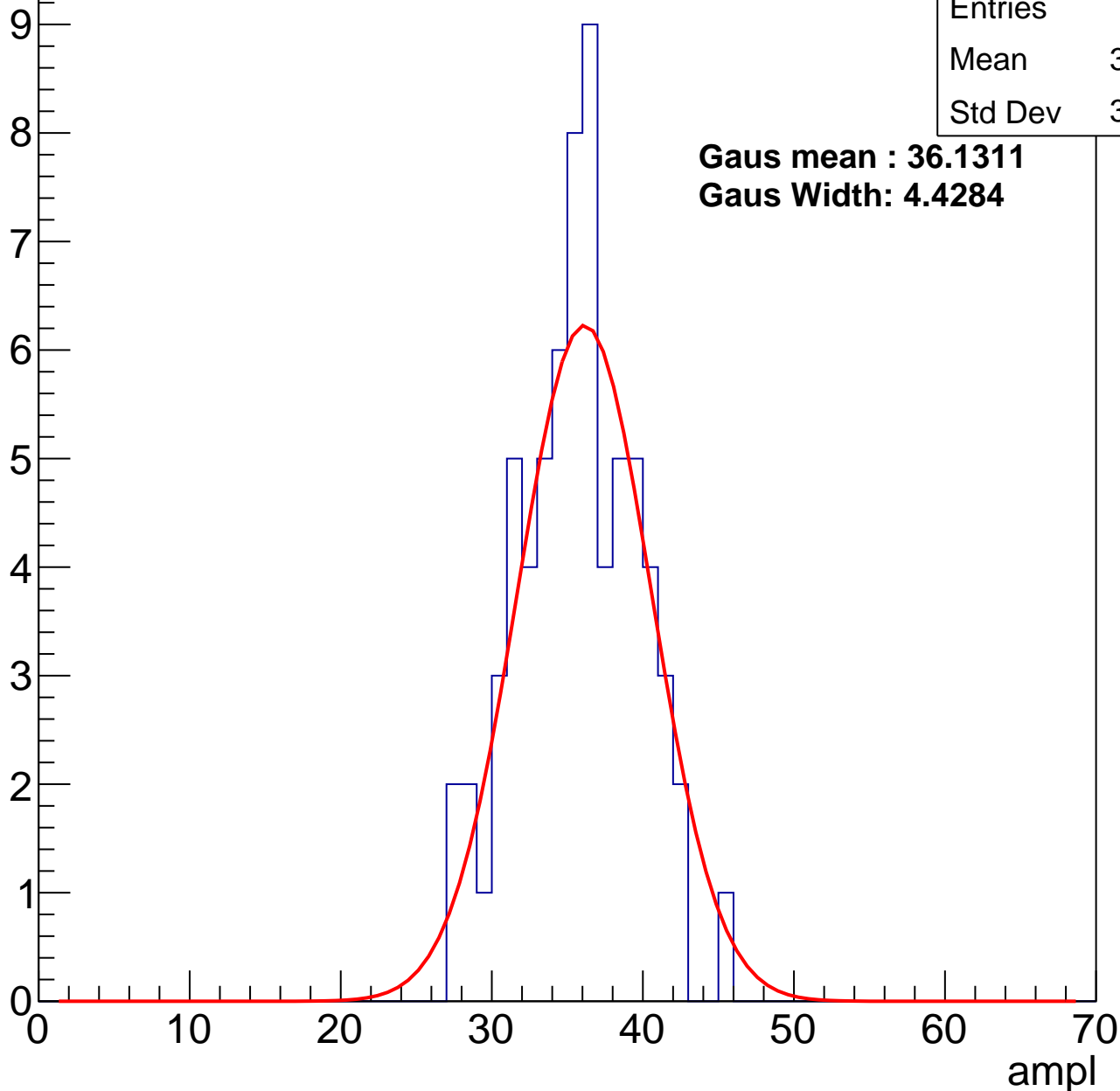
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	69
Mean	35.22
Std Dev	3.867

**Gaus mean : 36.1311**

**Gaus Width: 4.4284**



# B1L100S, U6-ch60, adc2

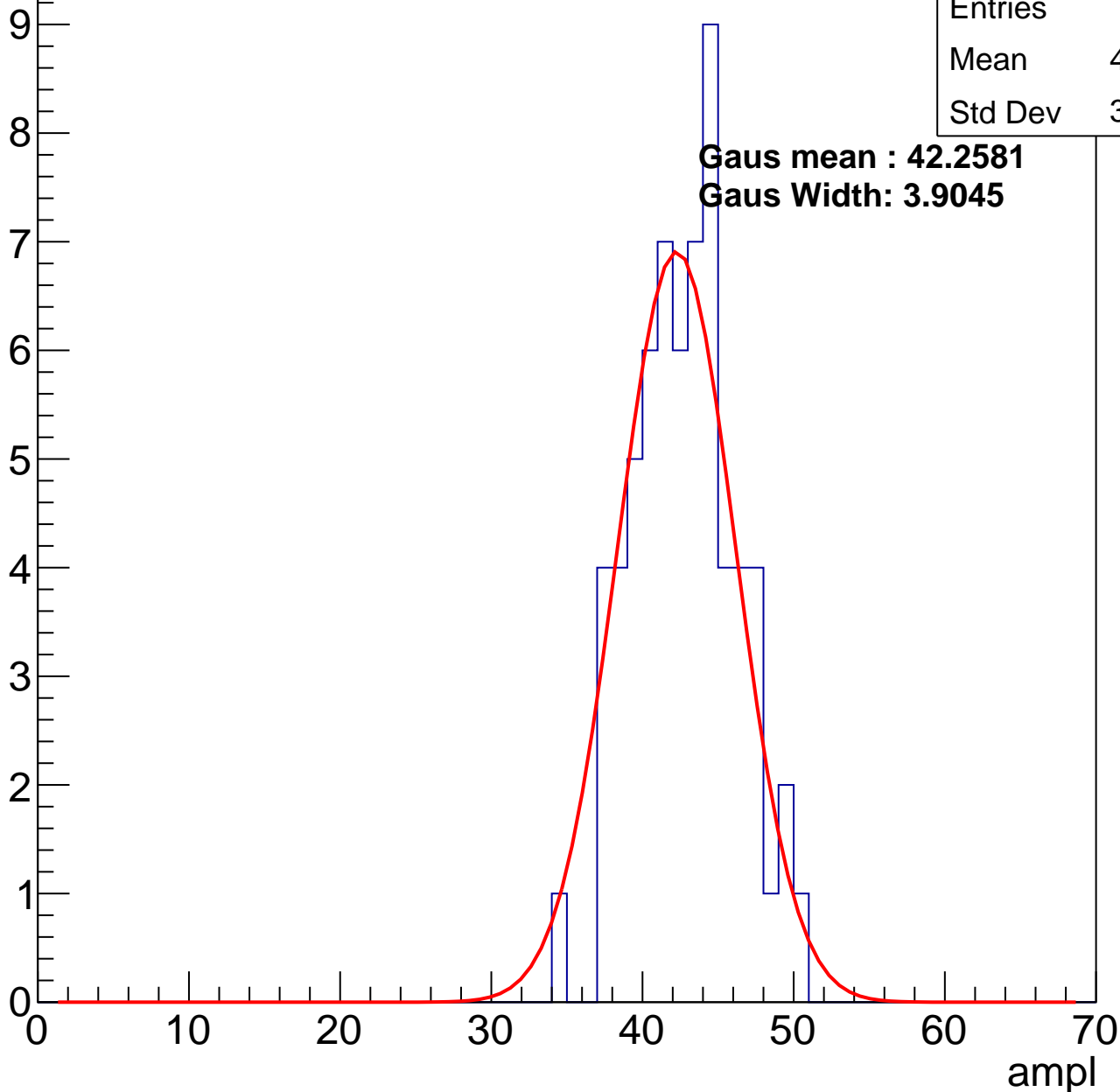
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	65
Mean	42.35
Std Dev	3.367

**Gaus mean : 42.2581**

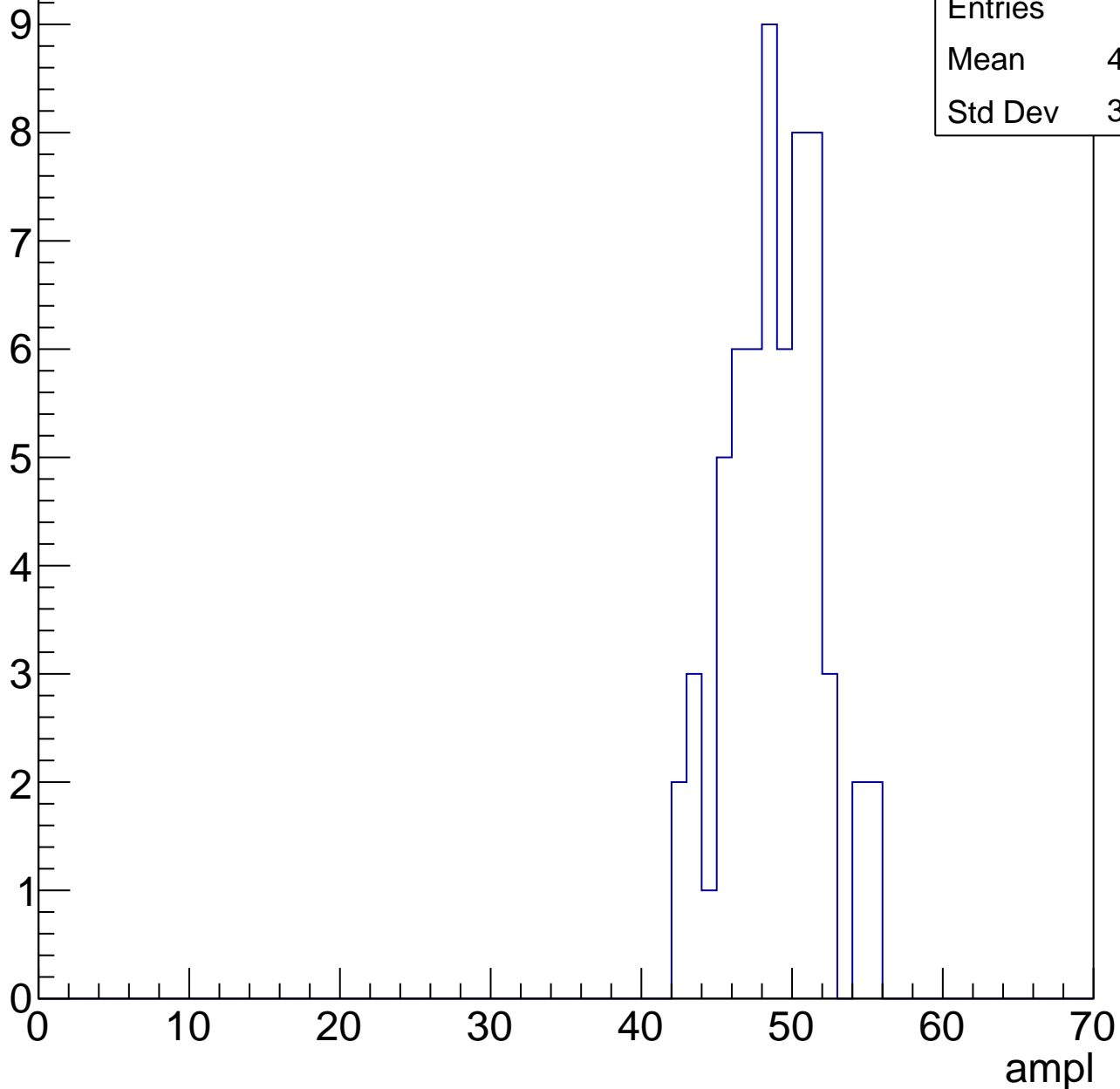
**Gaus Width: 3.9045**



# B1L100S, U6-ch60, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

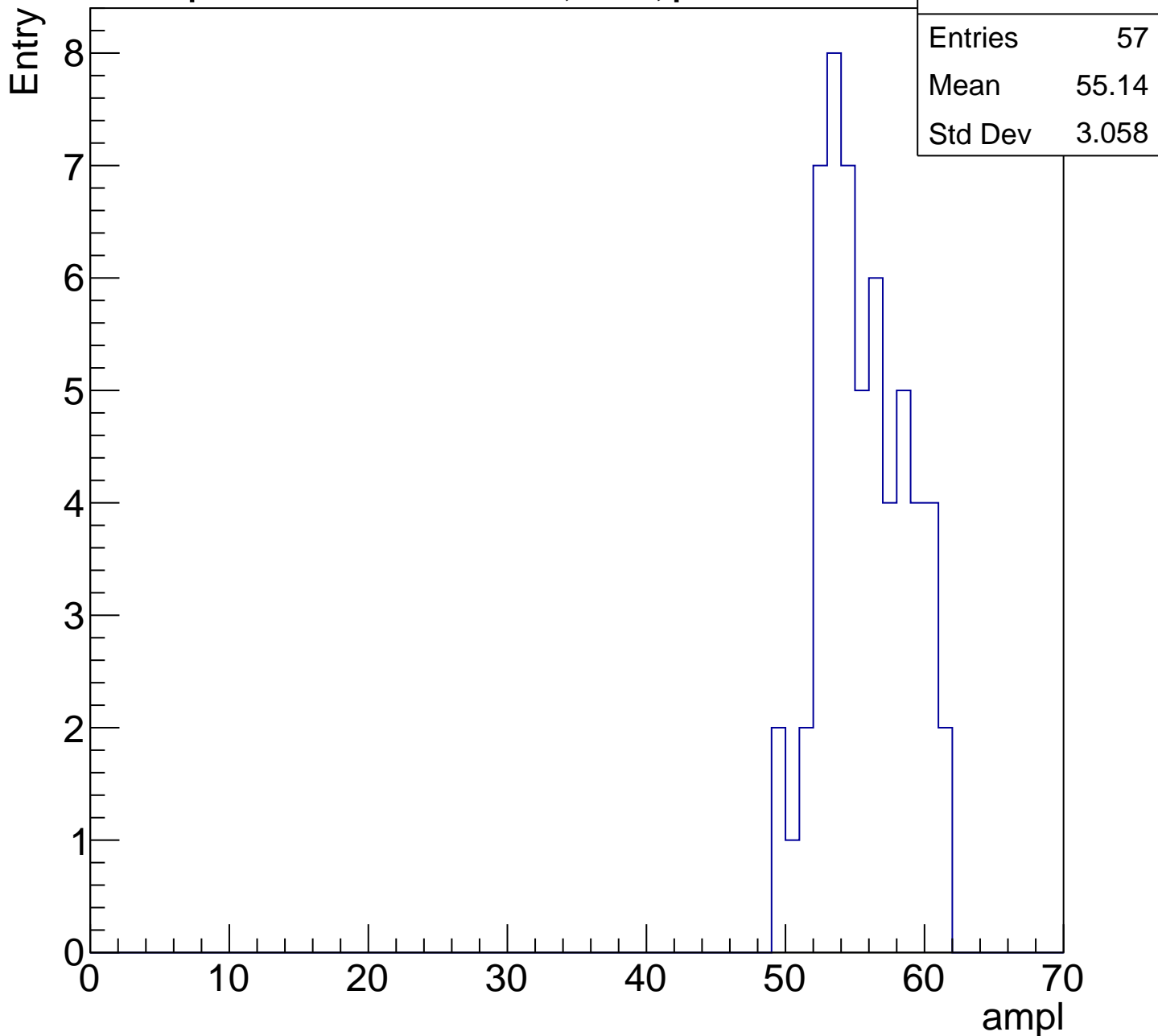
Entry



Entries	61
Mean	48.33
Std Dev	3.028

# B1L100S, U6-ch60, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

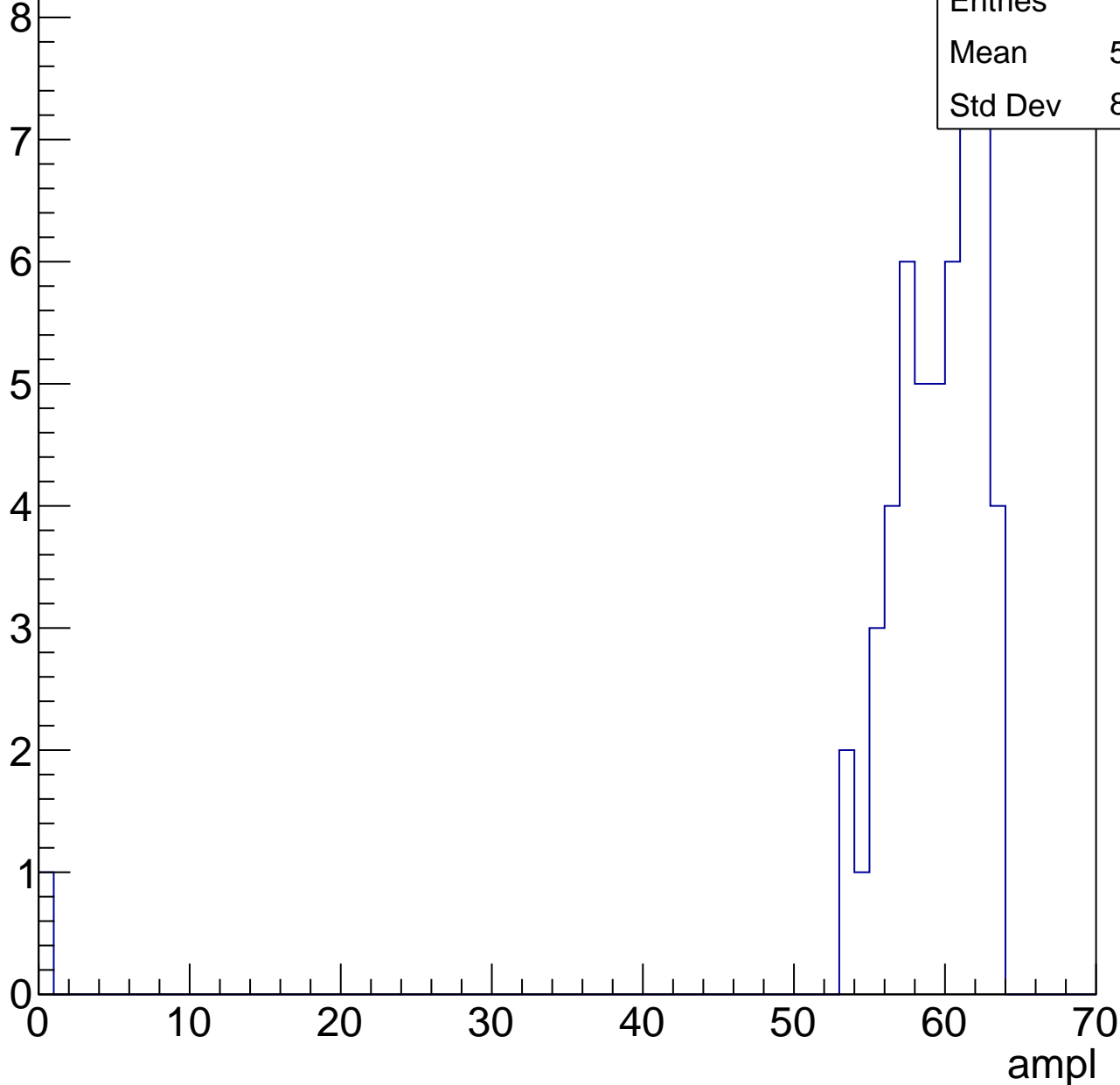


# B1L100S, U6-ch60, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	53
Mean	57.96
Std Dev	8.476

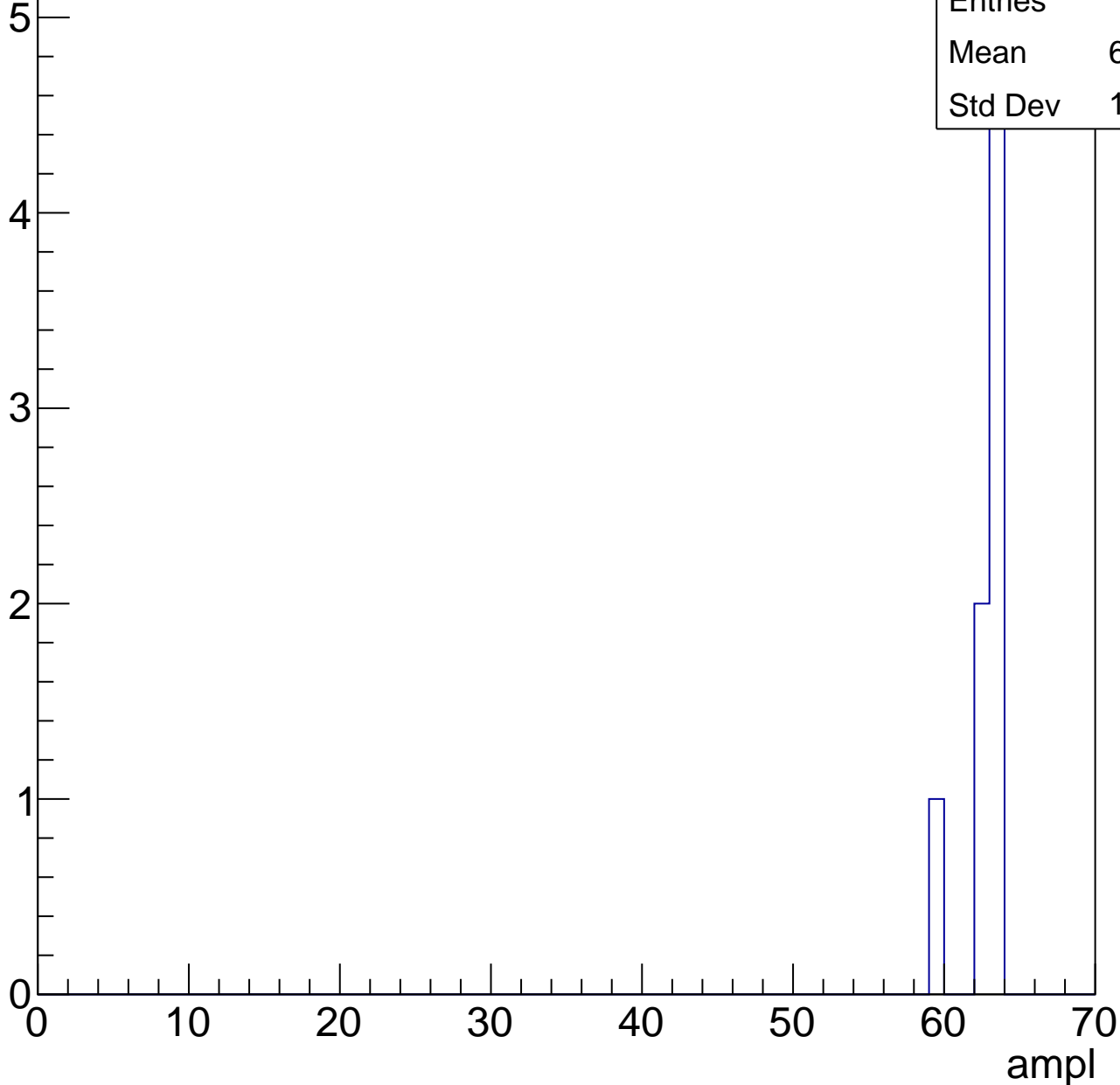


# B1L100S, U6-ch60, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	8
Mean	62.25
Std Dev	1.299

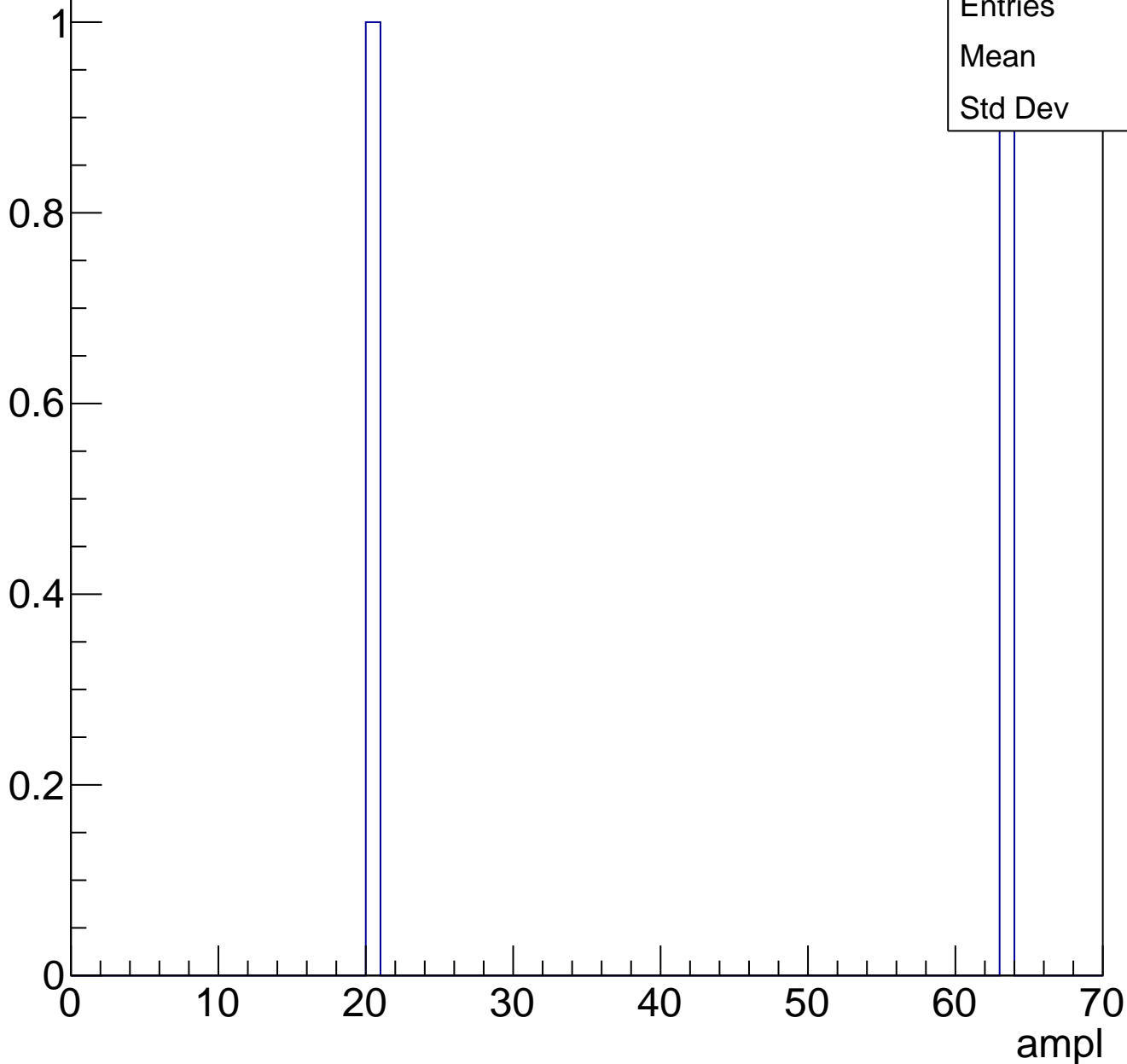




# B1L100S, U6-ch60, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



# B1L100S, U6-ch61, adc0

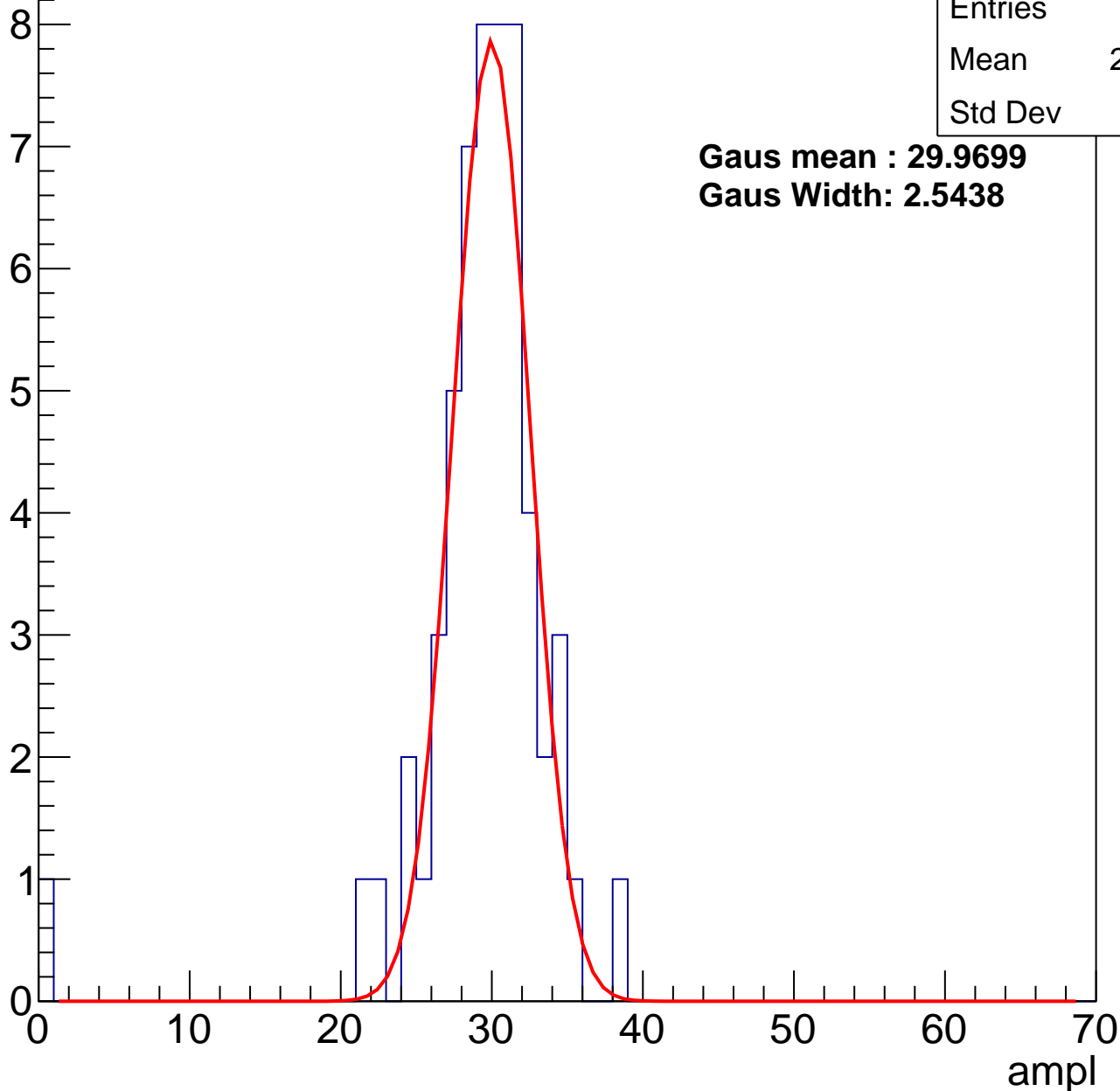
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	56
Mean	28.82
Std Dev	4.95

**Gaus mean : 29.9699**

**Gaus Width: 2.5438**



# B1L100S, U6-ch61, adc1

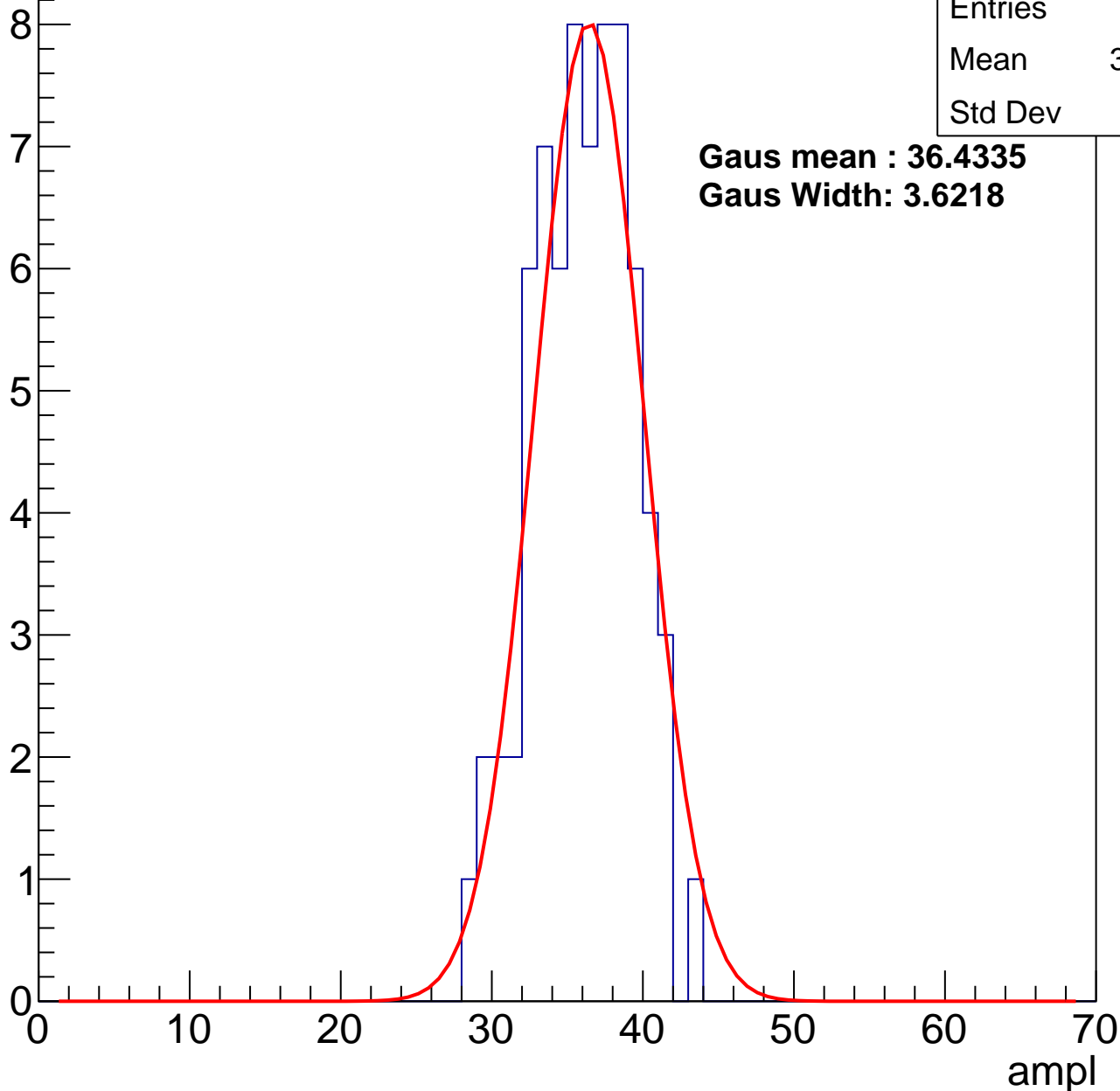
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	71
Mean	35.59
Std Dev	3.24

**Gaus mean : 36.4335**

**Gaus Width: 3.6218**



# B1L100S, U6-ch61, adc2

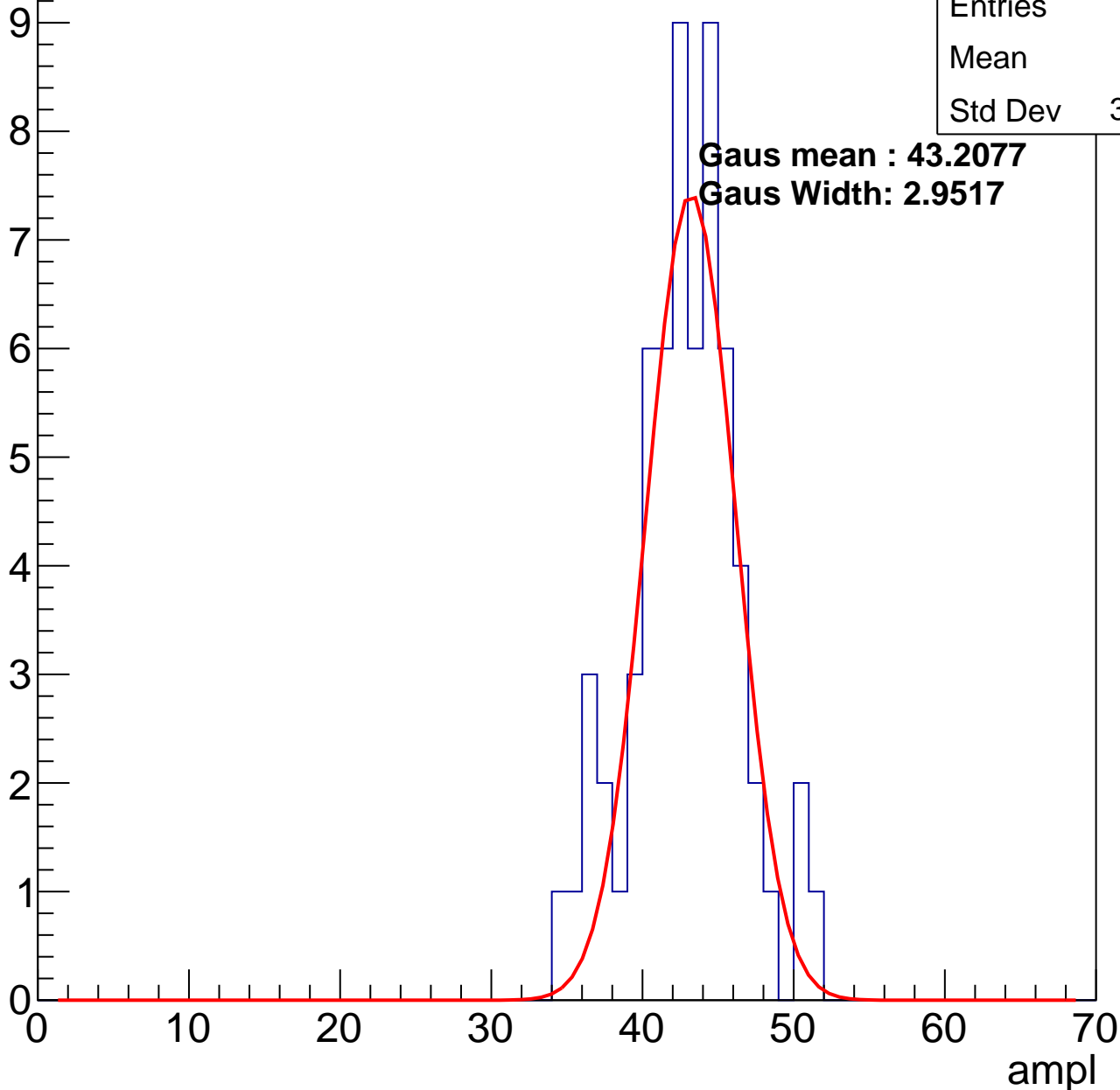
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	63
Mean	42.4
Std Dev	3.539

**Gaus mean : 43.2077**

**Gaus Width: 2.9517**



# B1L100S, U6-ch61, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	80
Mean	49.1
Std Dev	3.463

Entry

10

8

6

4

2

0

0

10

20

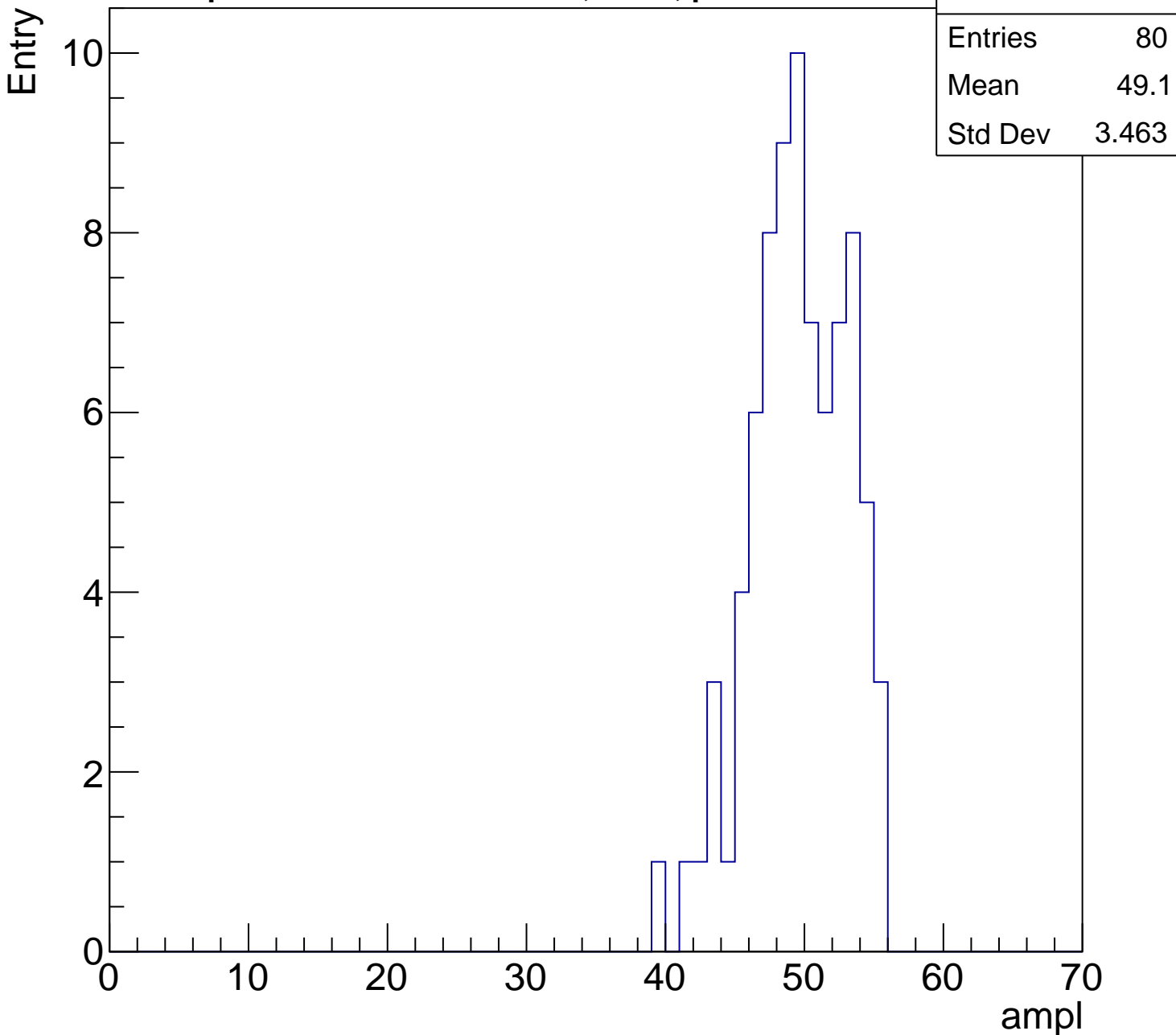
30

40

50

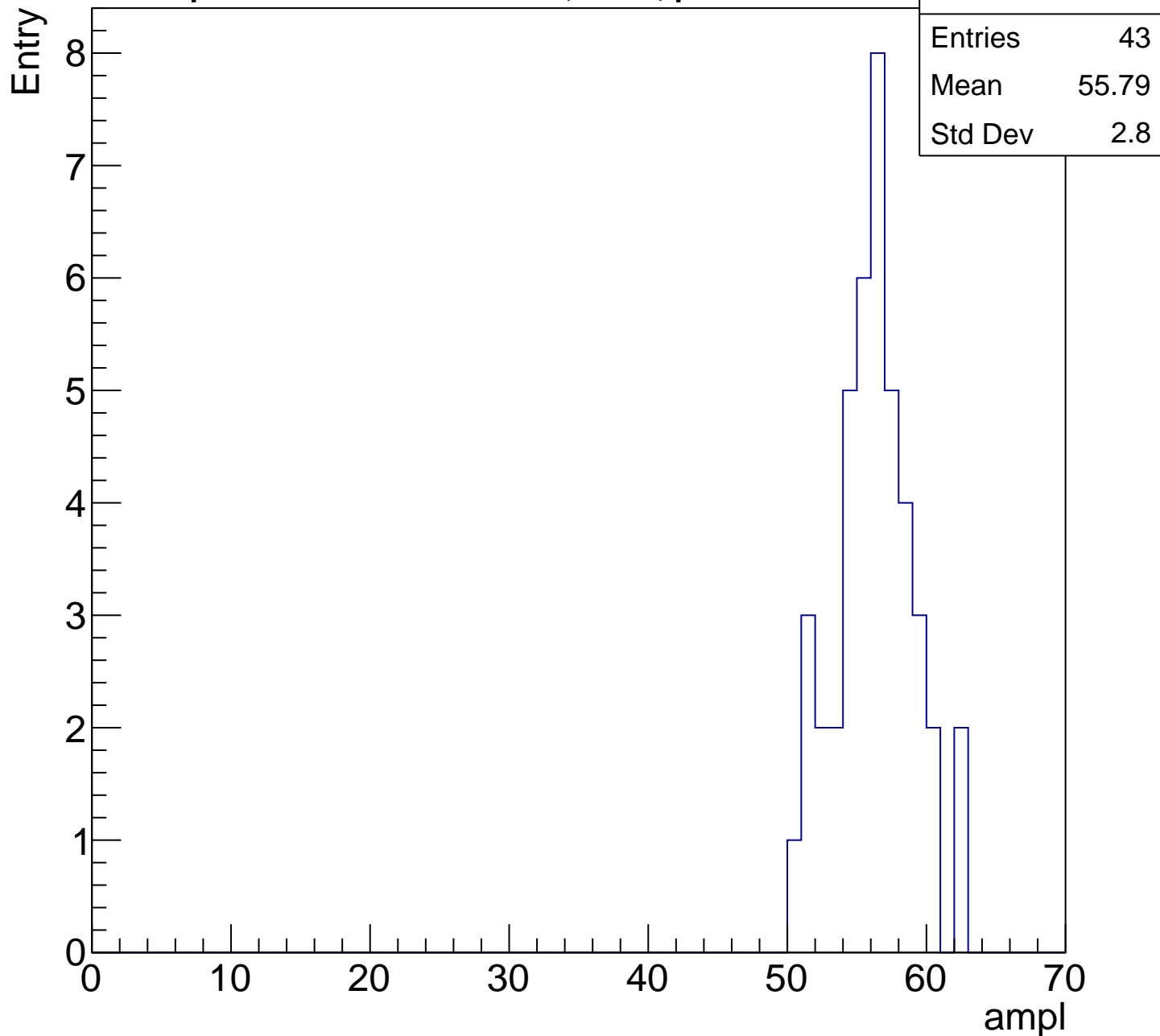
60

ampl



# B1L100S, U6-ch61, adc4

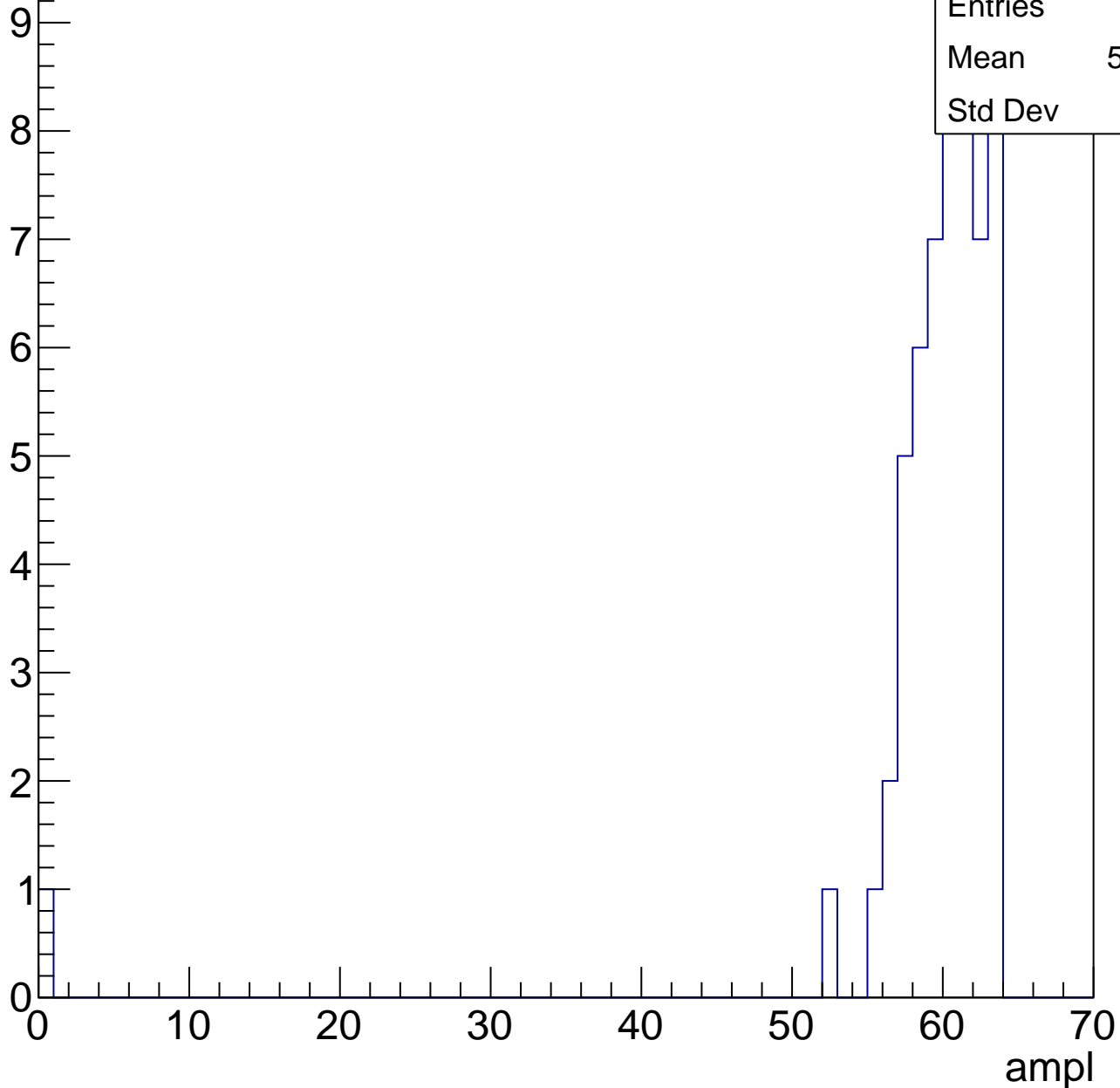
calib\_packv5\_042523\_0143.root, FC#4, port A2



# B1L100S, U6-ch61, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



# B1L100S, U6-ch61, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry





# B1L100S, U6-ch61, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L100S, U6-ch62, adc0

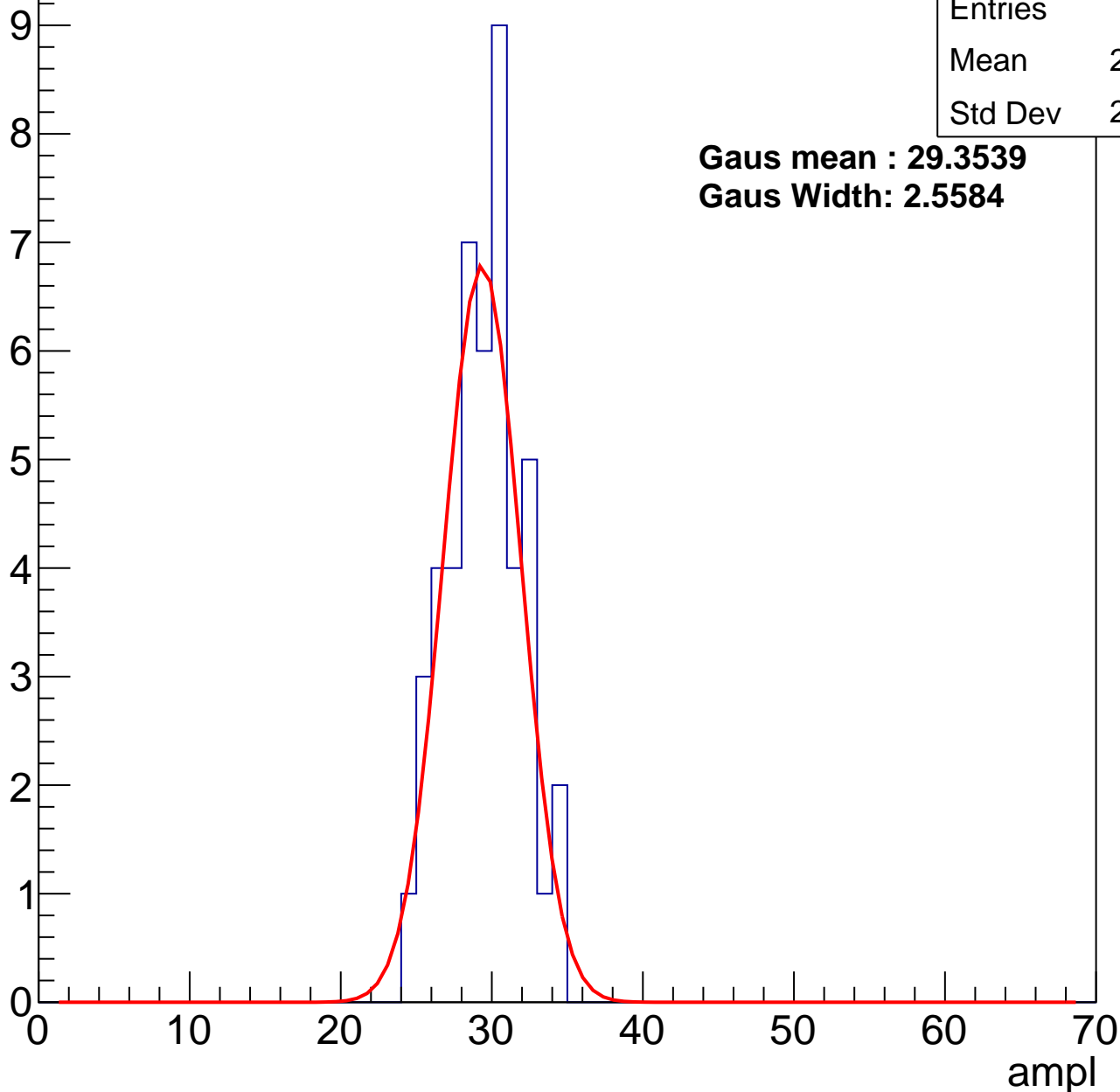
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	46
Mean	29.04
Std Dev	2.413

**Gaus mean : 29.3539**

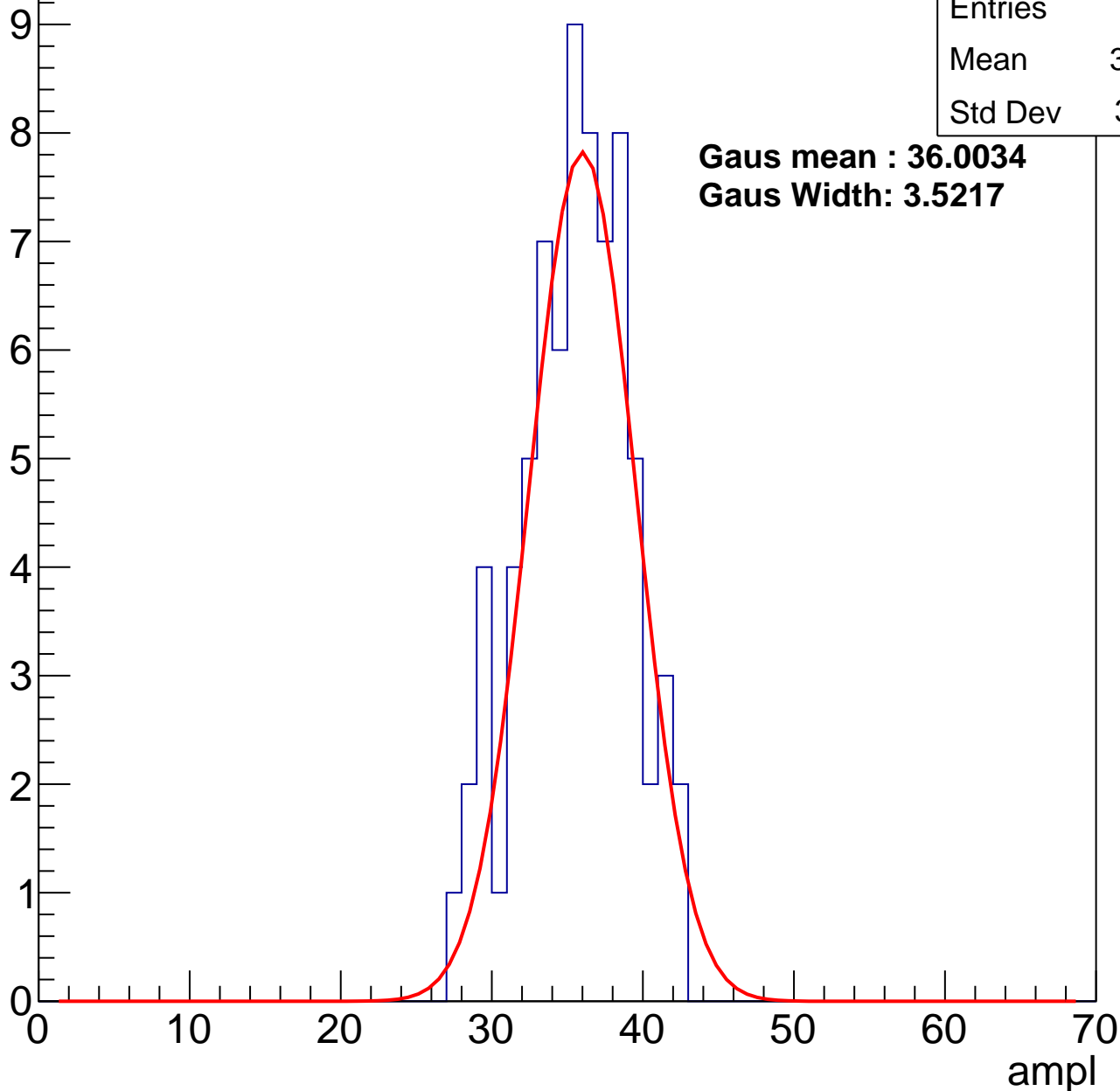
**Gaus Width: 2.5584**



# B1L100S, U6-ch62, adc1

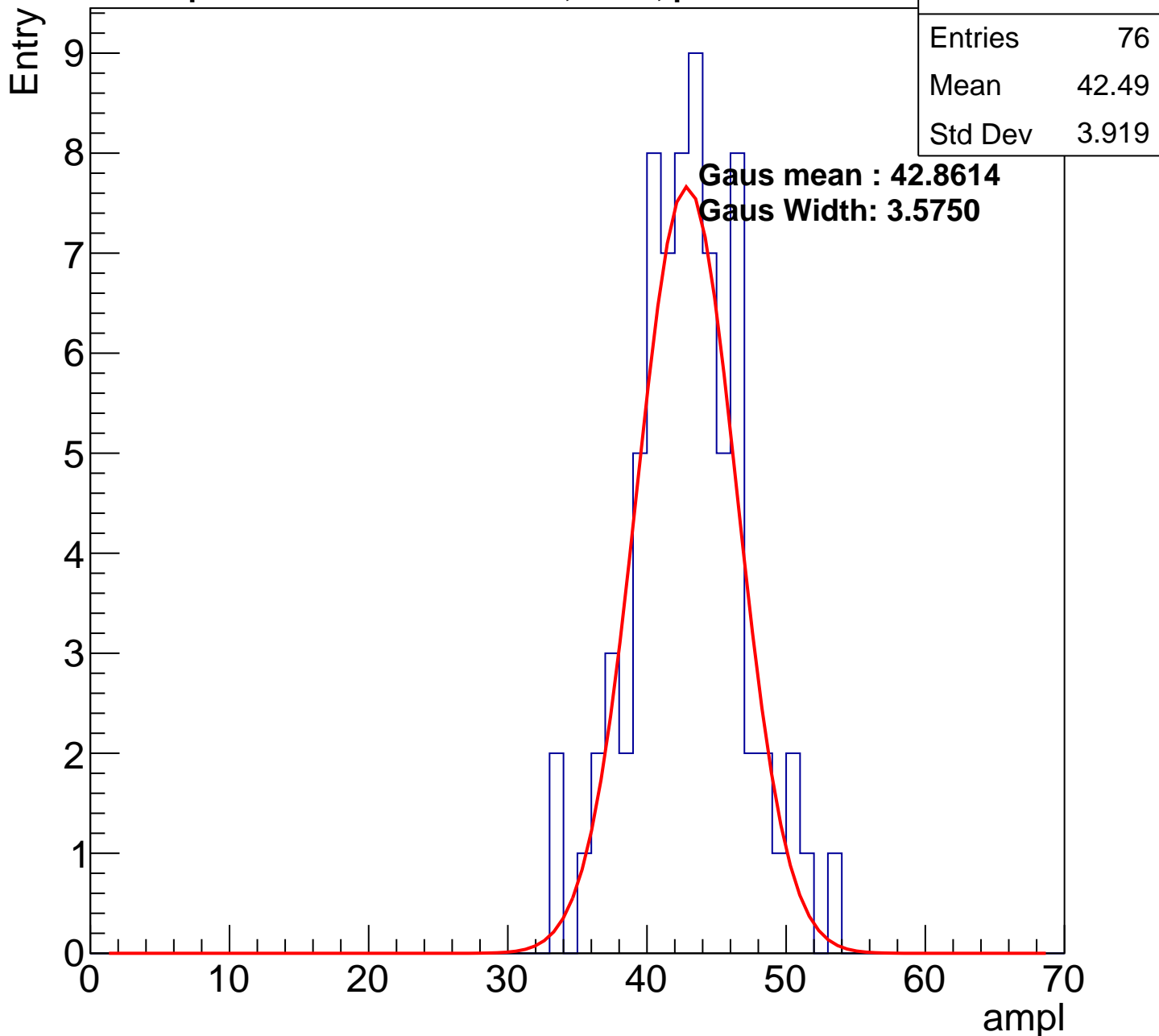
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



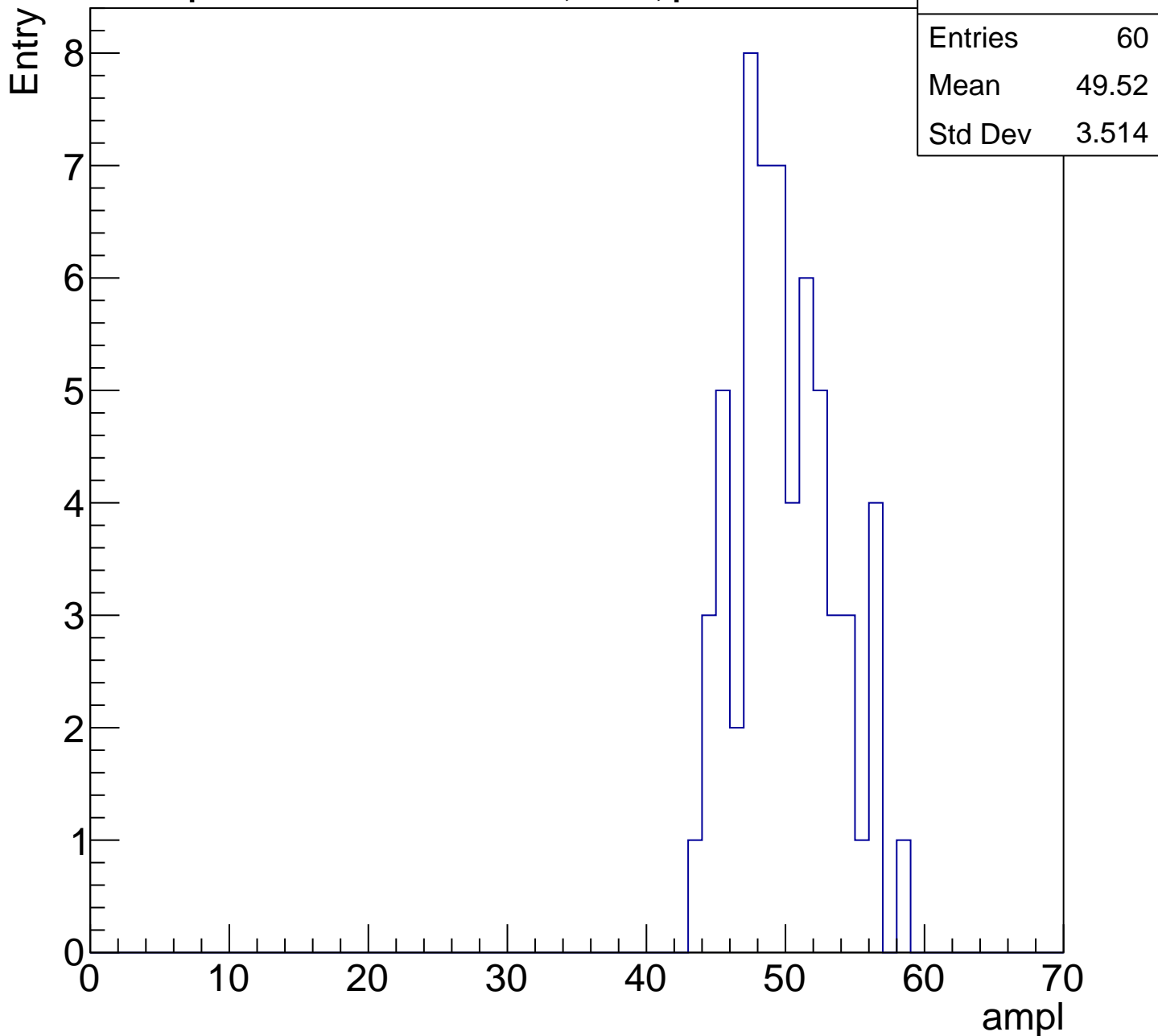
# B1L100S, U6-ch62, adc2

calib\_packv5\_042523\_0143.root, FC#4, port A2



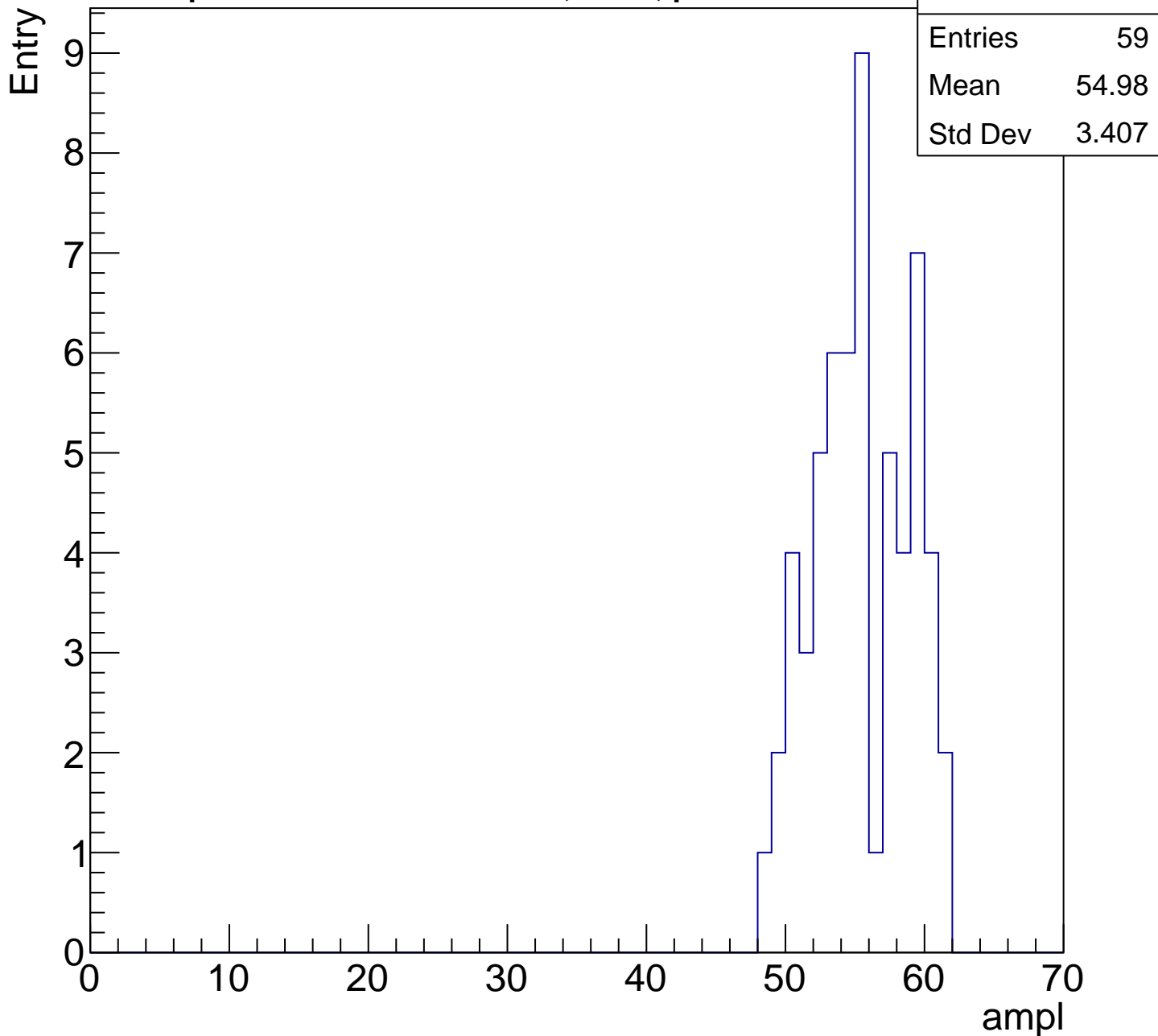
# B1L100S, U6-ch62, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2



# B1L100S, U6-ch62, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2



# B1L100S, U6-ch62, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	48
Mean	58.75
Std Dev	8.922

ampl

0 10 20 30 40 50 60 70

0

1

2

3

4

5

6

7

8

9

# B1L100S, U6-ch62, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

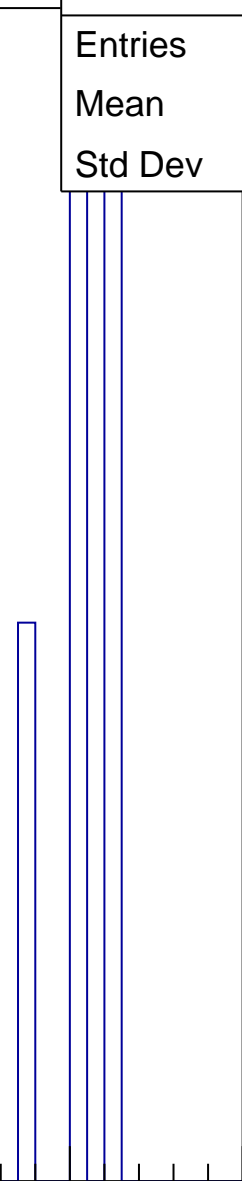
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	5
Mean	60.2
Std Dev	1.833

0 10 20 30 40 50 60 70

ampl





# B1L100S, U6-ch62, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	3
Mean	21
Std Dev	29.7

# B1L100S, U6-ch63, adc0

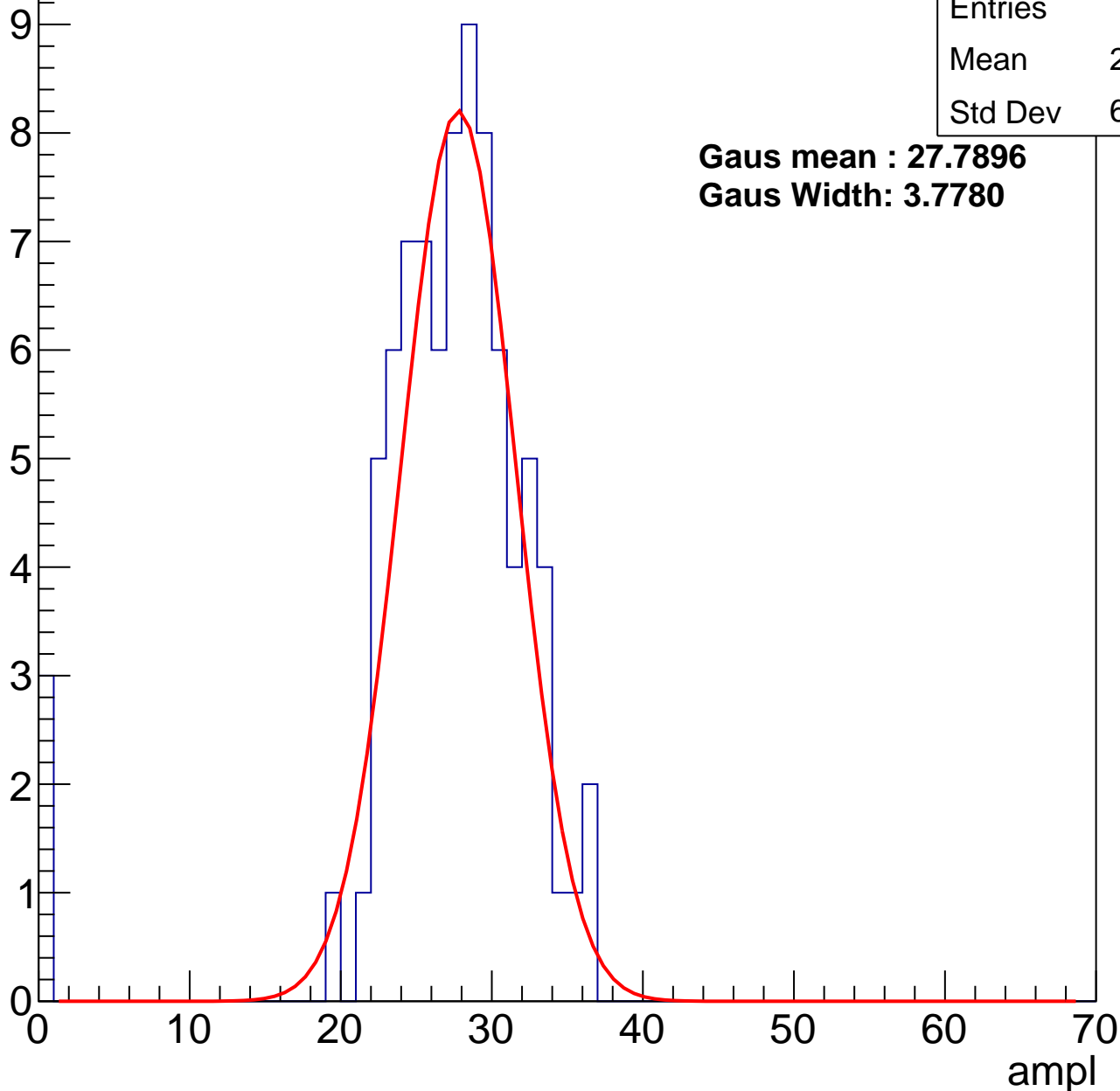
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	84
Mean	26.48
Std Dev	6.254

**Gaus mean : 27.7896**

**Gaus Width: 3.7780**



# B1L100S, U6-ch63, adc1

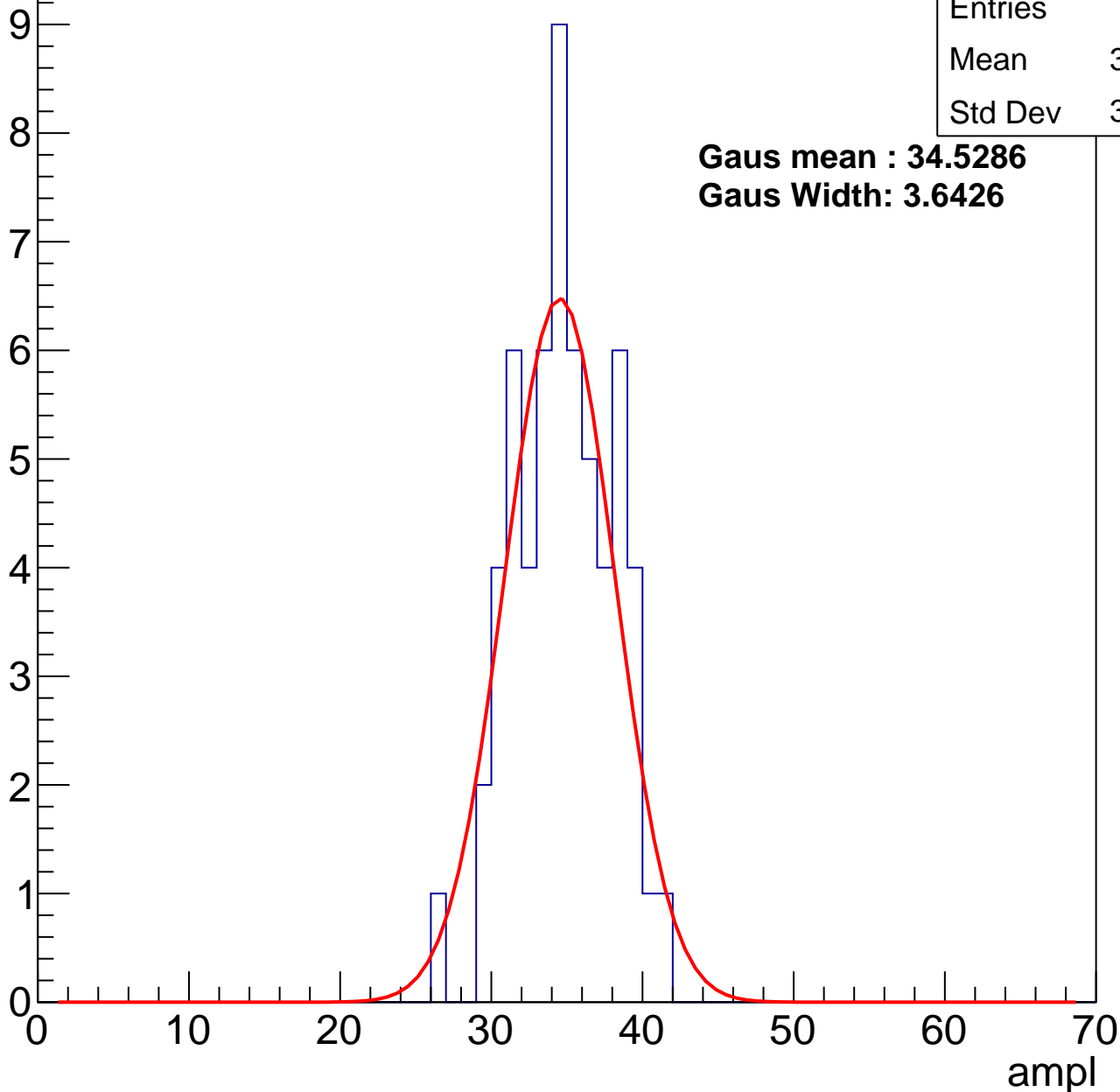
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	59
Mean	34.32
Std Dev	3.165

**Gaus mean : 34.5286**

**Gaus Width: 3.6426**



# B1L100S, U6-ch63, adc2

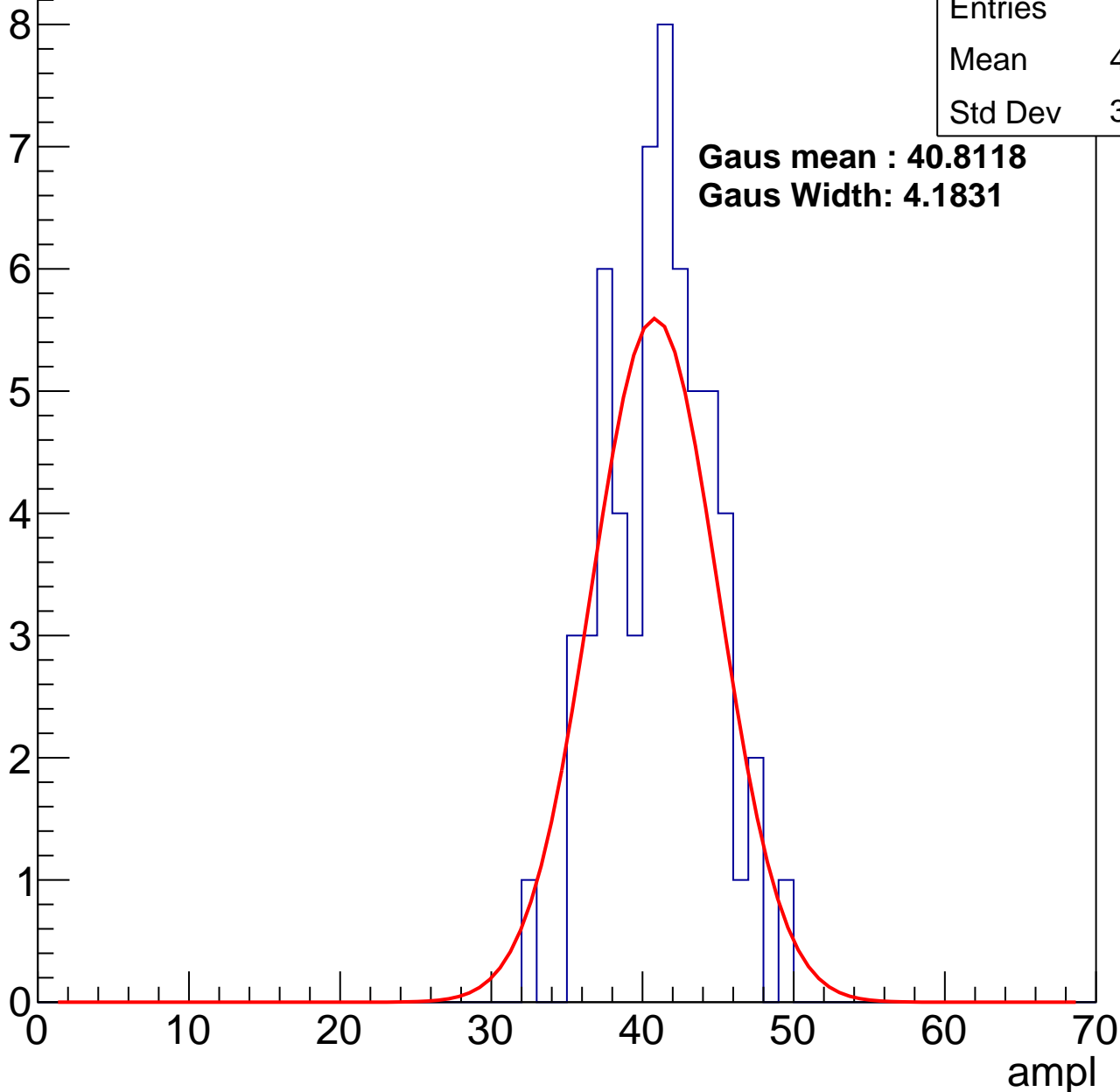
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	59
Mean	40.68
Std Dev	3.456

**Gaus mean : 40.8118**

**Gaus Width: 4.1831**

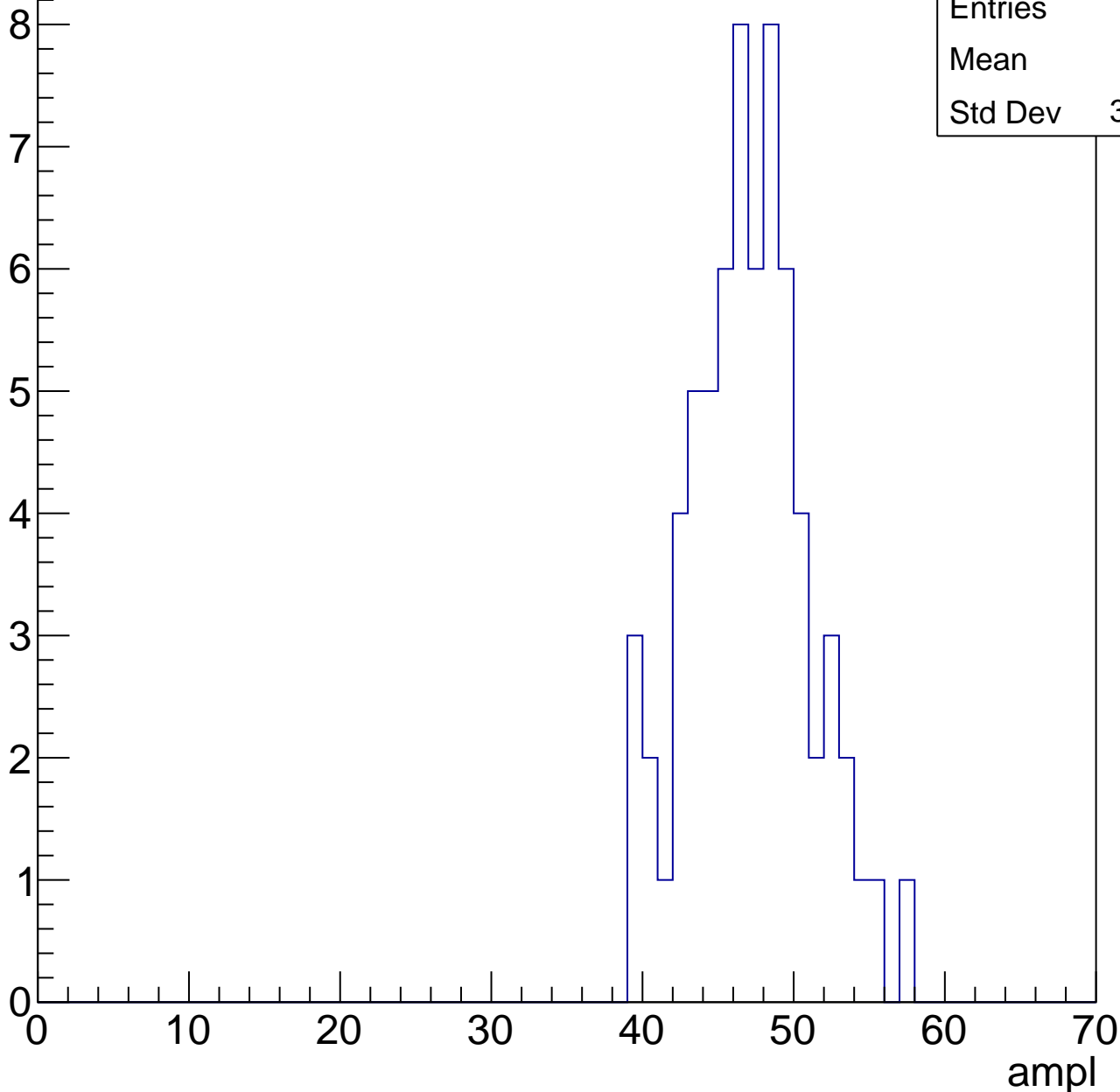


# B1L100S, U6-ch63, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

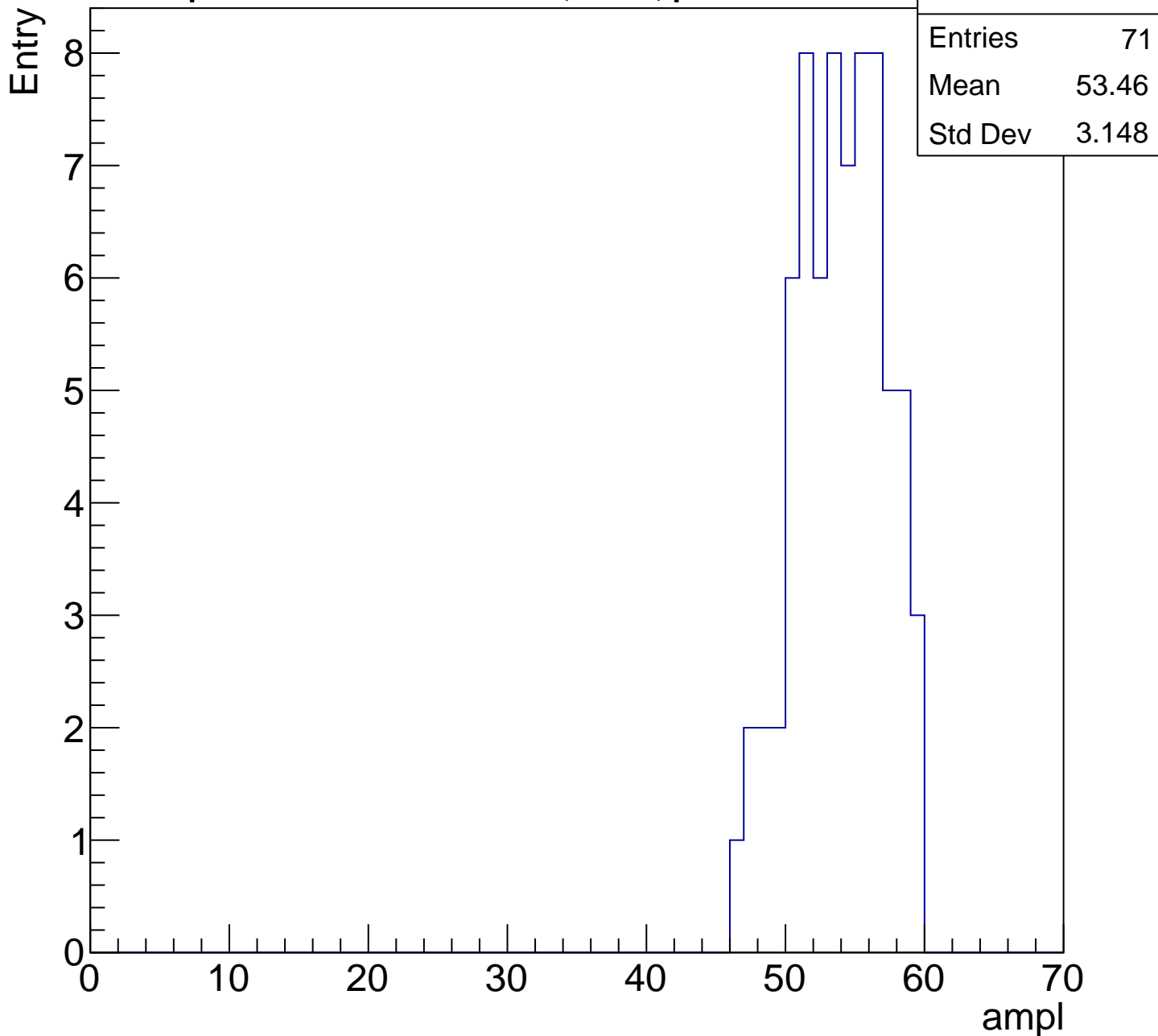
Entry

Entries	68
Mean	46.6
Std Dev	3.896



# B1L100S, U6-ch63, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

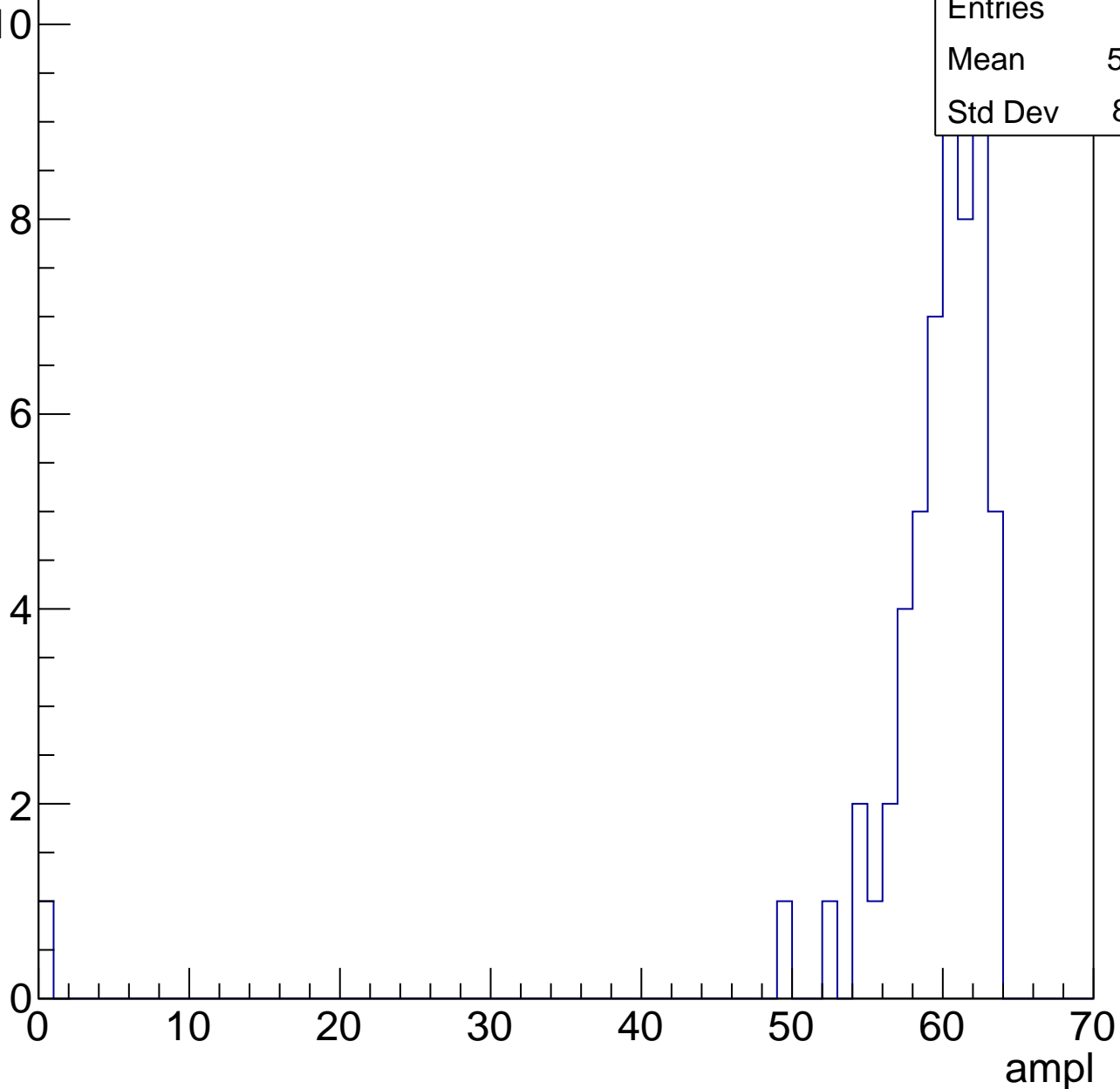


# B1L100S, U6-ch63, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	57
Mean	58.42
Std Dev	8.301

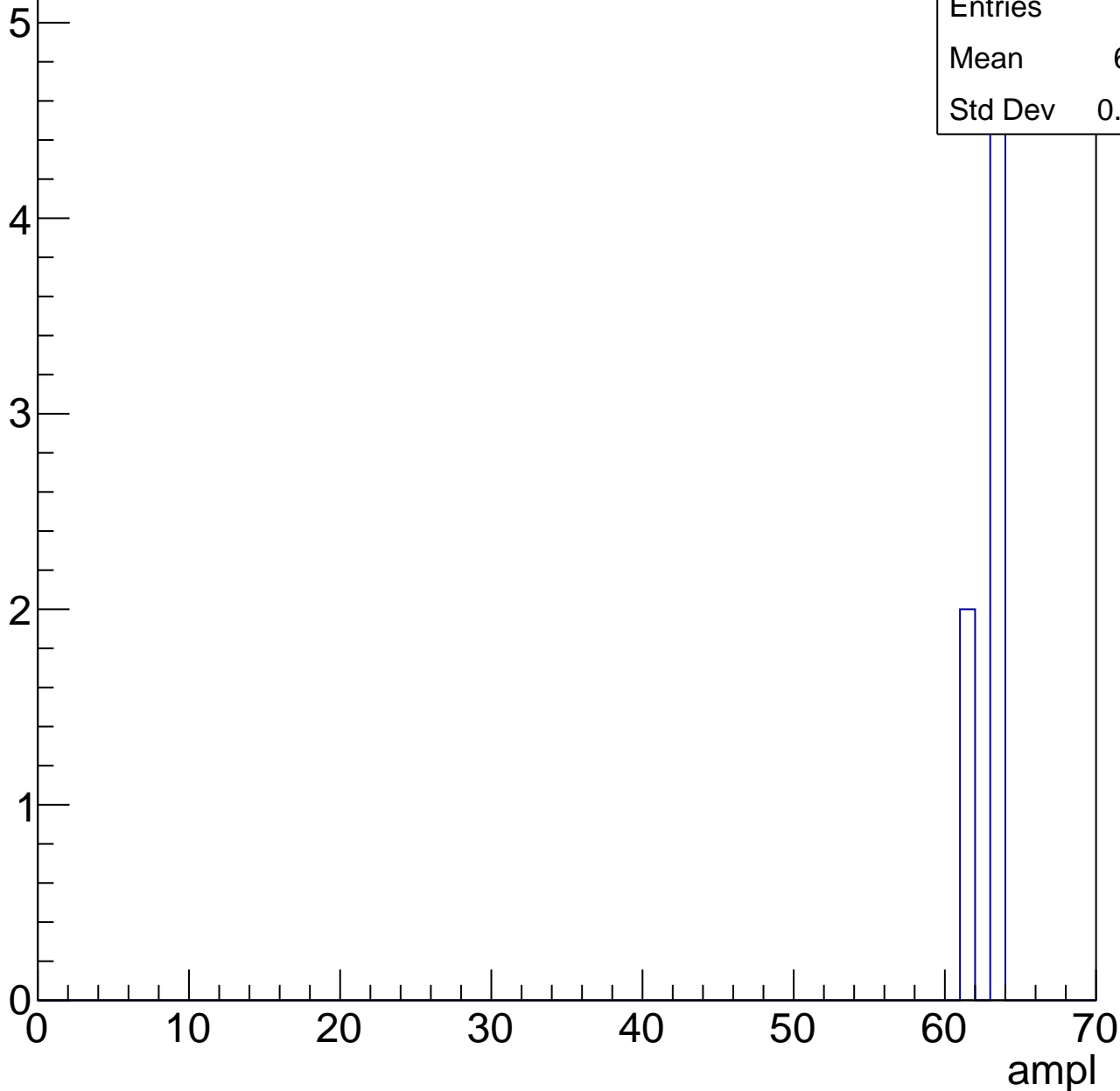


# B1L100S, U6-ch63, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	7
Mean	62.43
Std Dev	0.9035





# B1L100S, U6-ch63, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L100S, U6-ch64, adc0

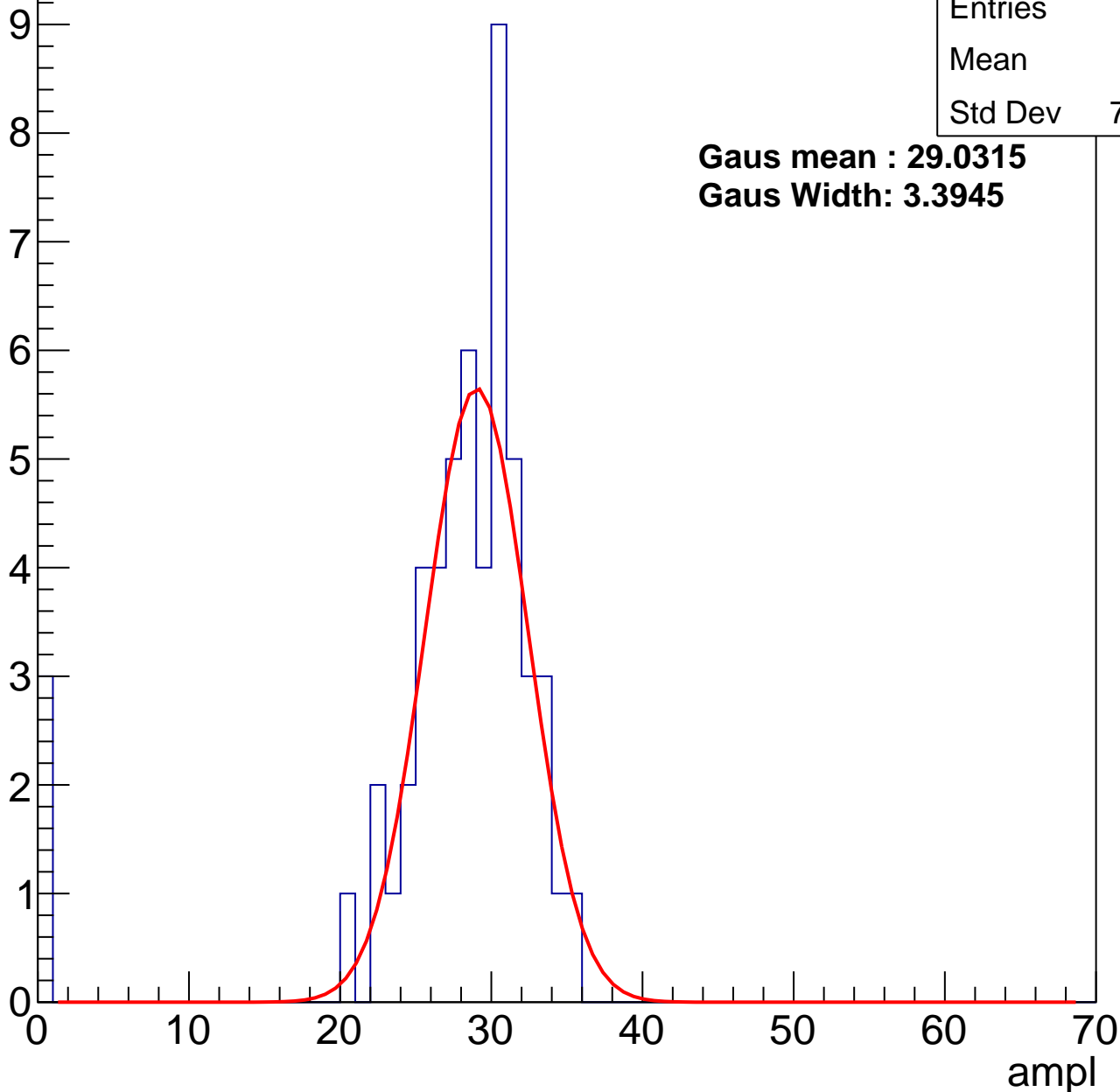
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	54
Mean	26.8
Std Dev	7.222

**Gaus mean : 29.0315**

**Gaus Width: 3.3945**



# B1L100S, U6-ch64, adc1

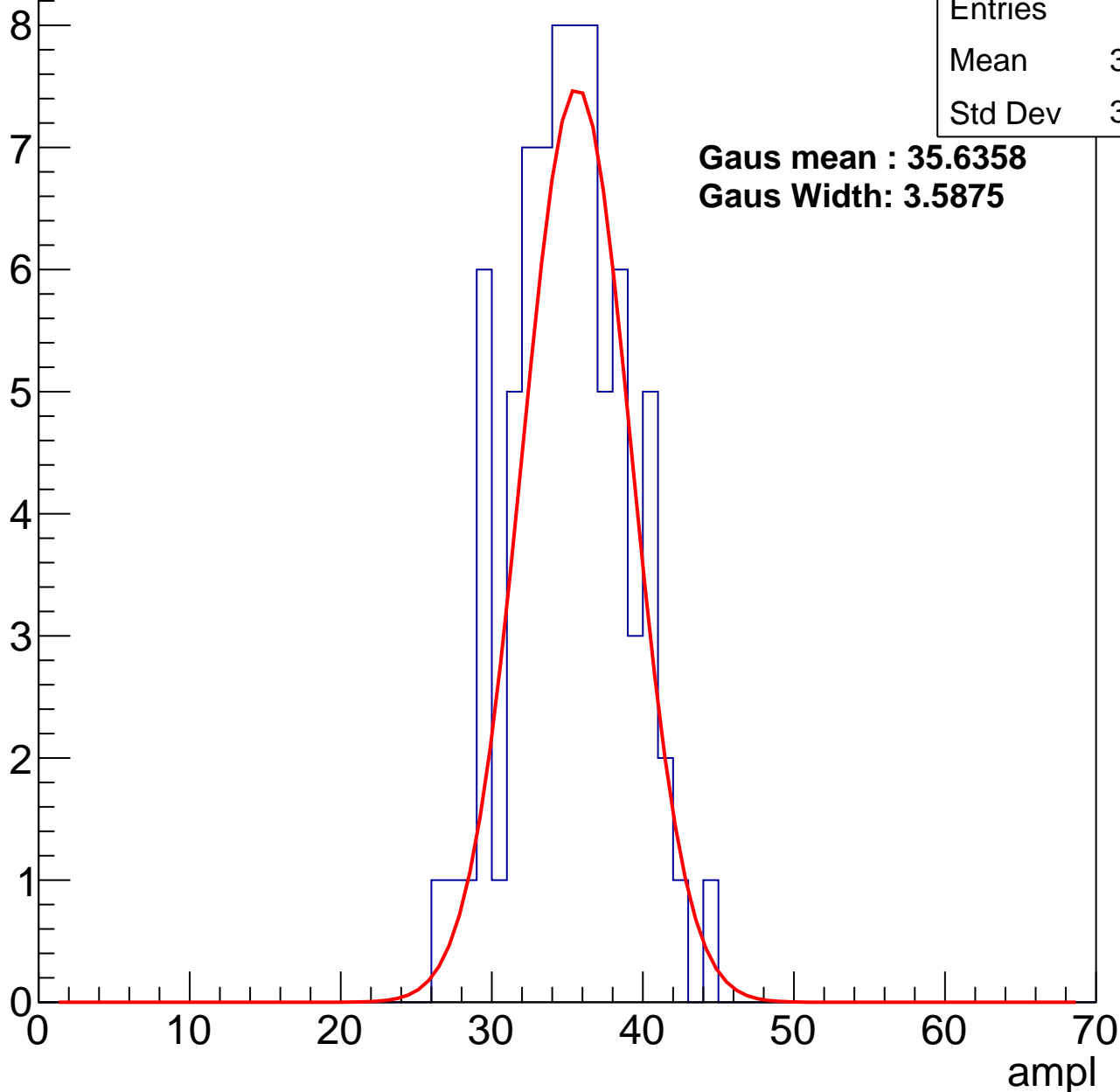
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	76
Mean	34.64
Std Dev	3.737

**Gaus mean : 35.6358**

**Gaus Width: 3.5875**

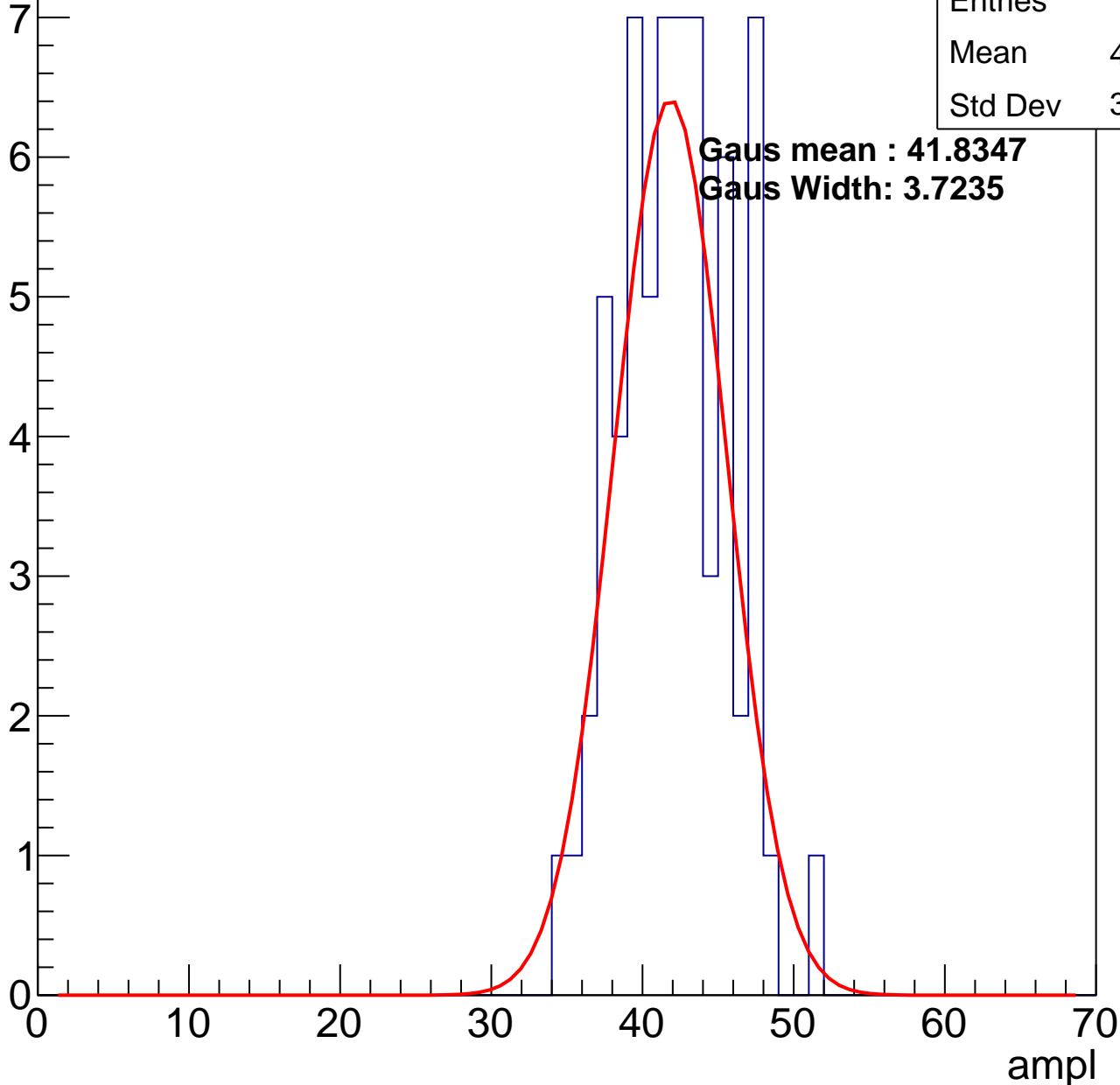


# B1L100S, U6-ch64, adc2

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

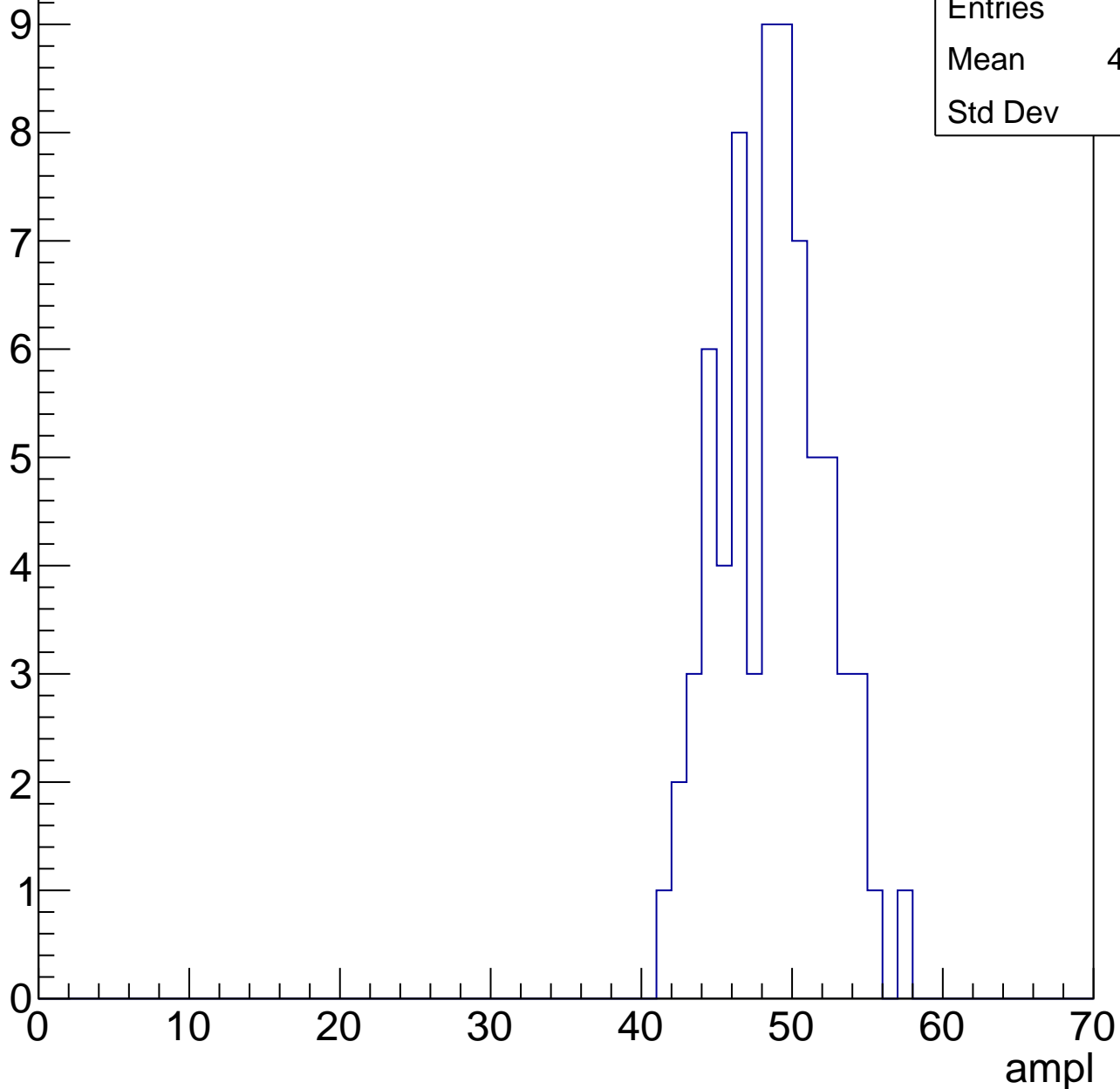
Entries	66
Mean	41.74
Std Dev	3.603



# B1L100S, U6-ch64, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

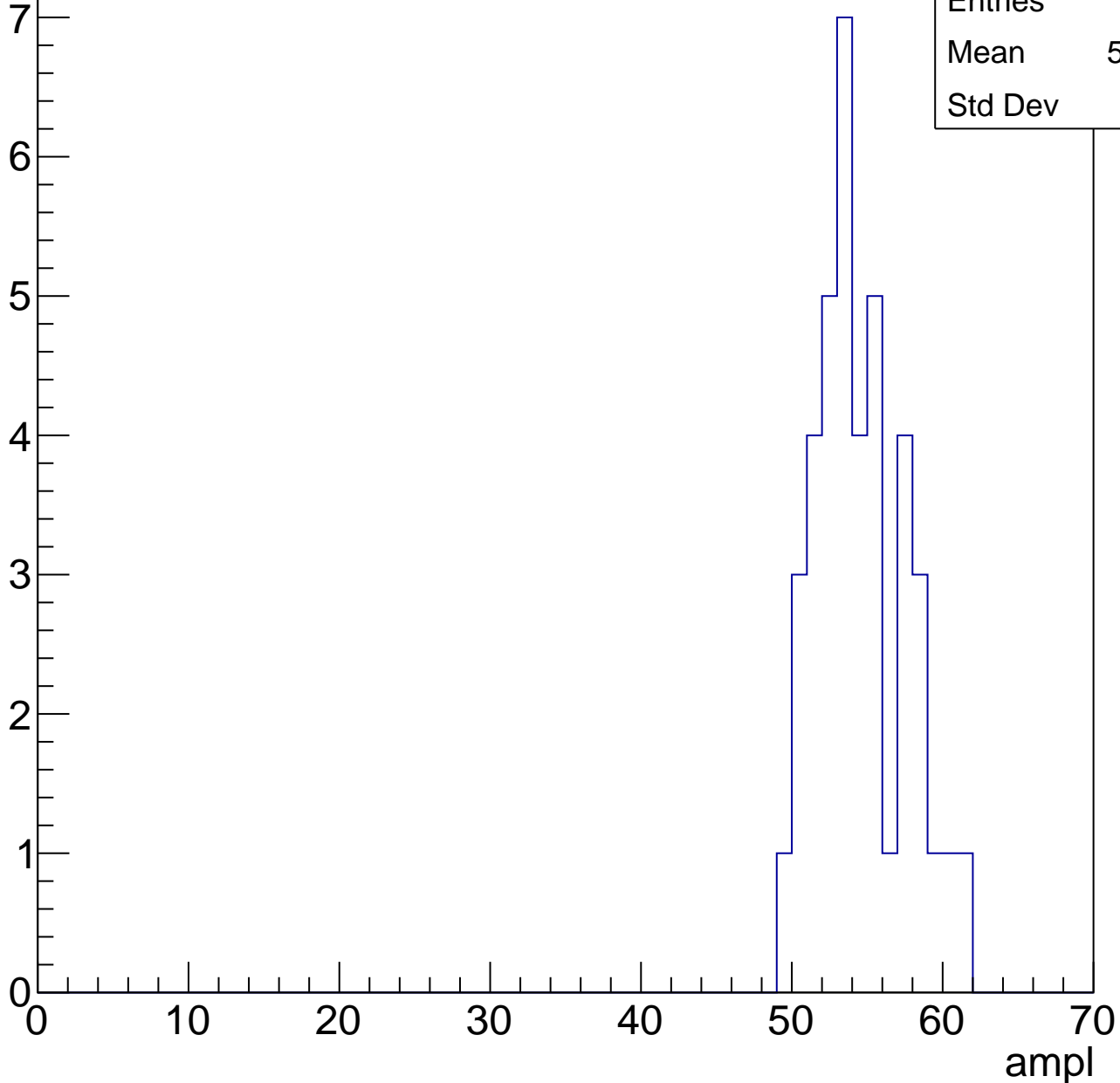


# B1L100S, U6-ch64, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

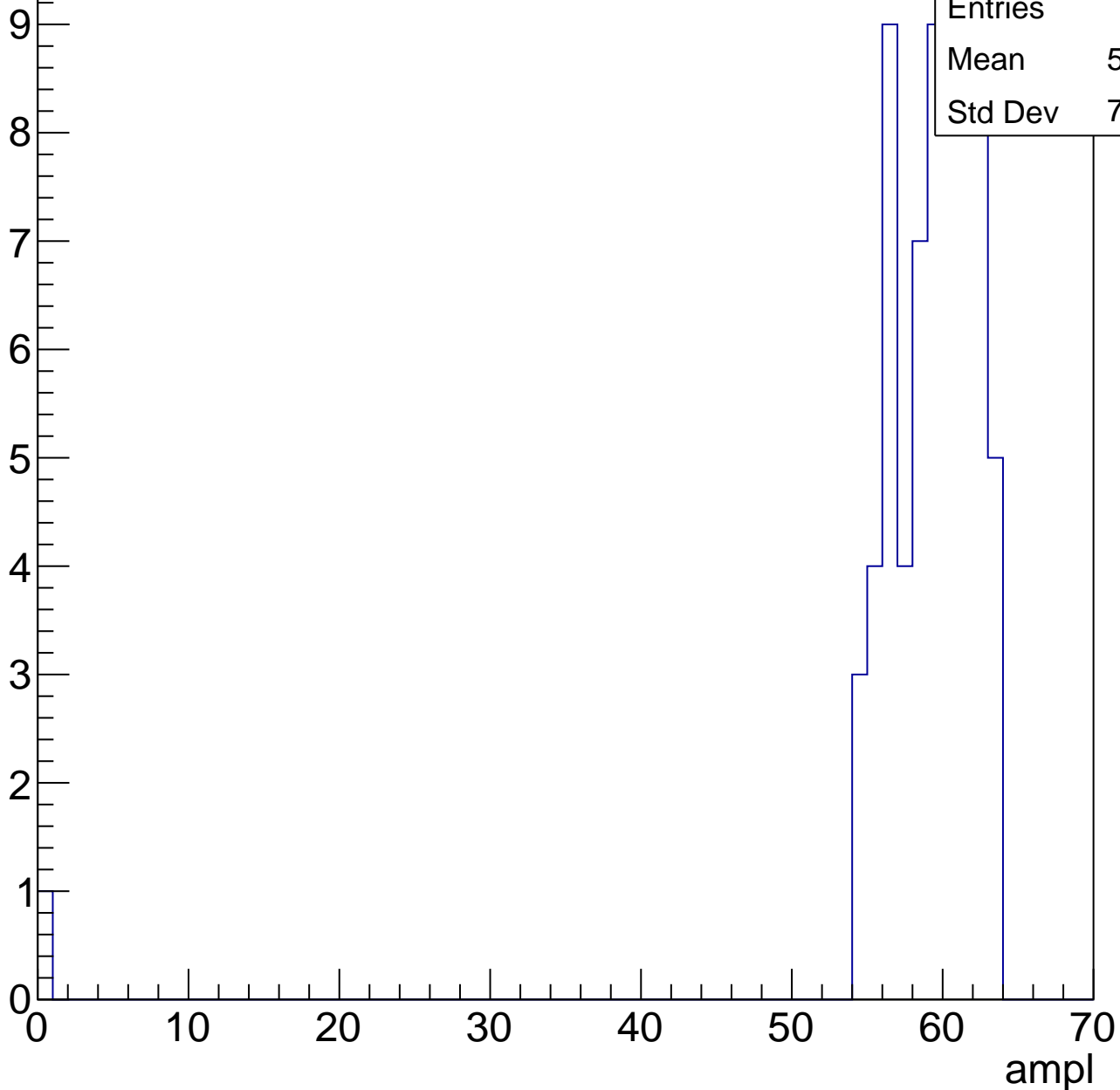
Entries	40
Mean	54.08
Std Dev	2.91



# B1L100S, U6-ch64, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

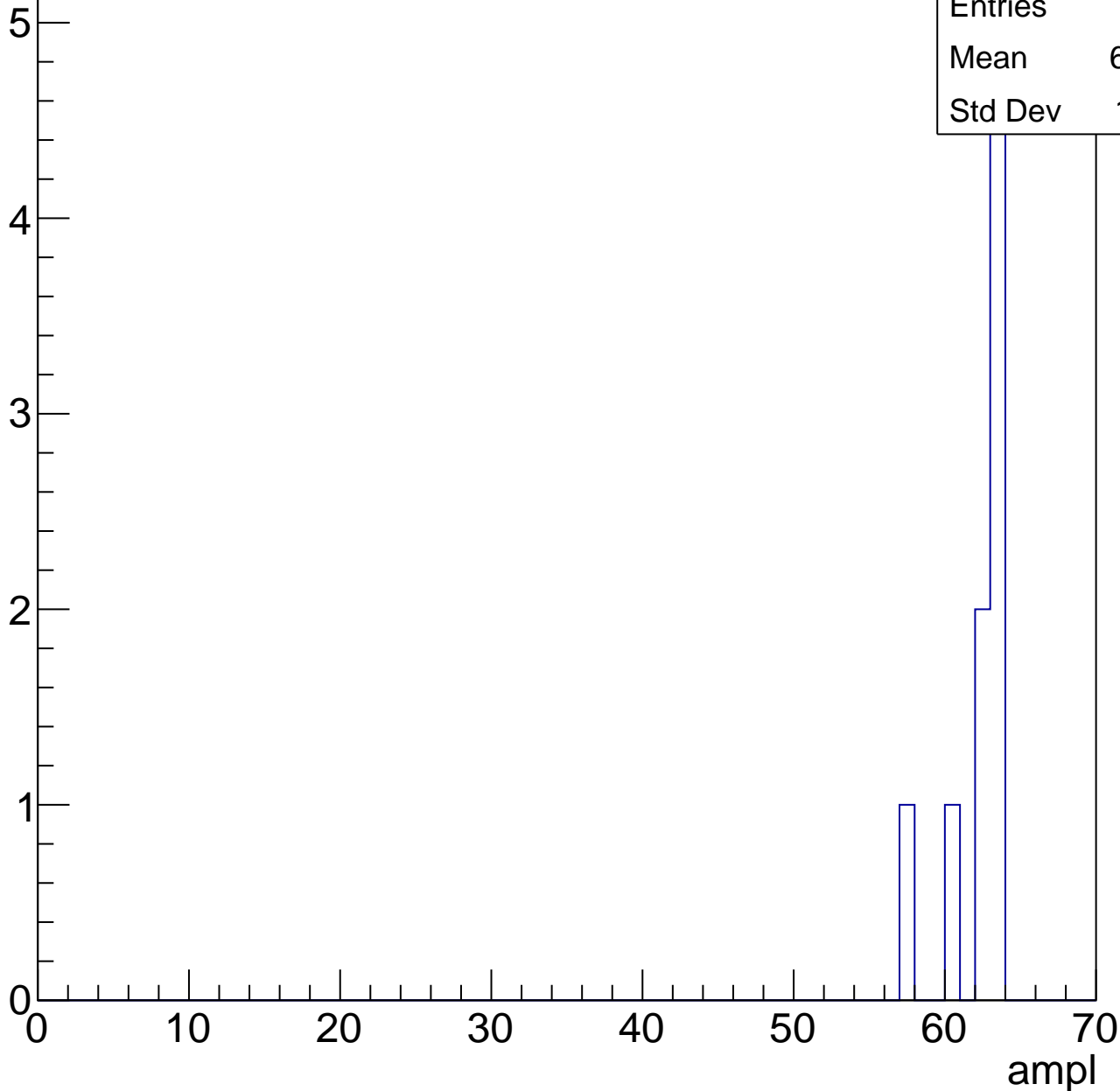


# B1L100S, U6-ch64, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	9
Mean	61.78
Std Dev	1.931





# B1L100S, U6-ch64, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L100S, U6-ch65, adc0

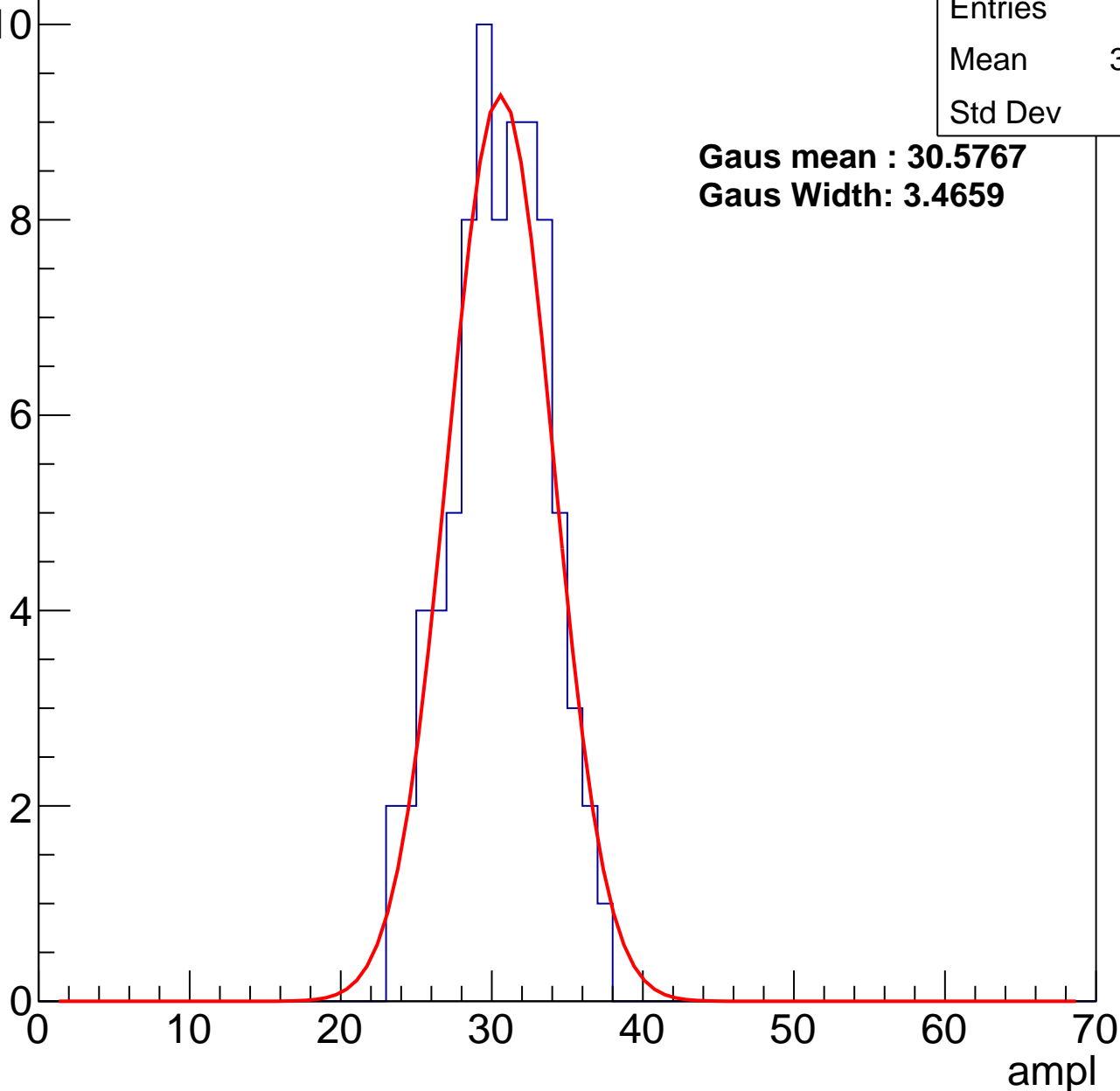
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	80
Mean	30.02
Std Dev	3.19

**Gaus mean : 30.5767**

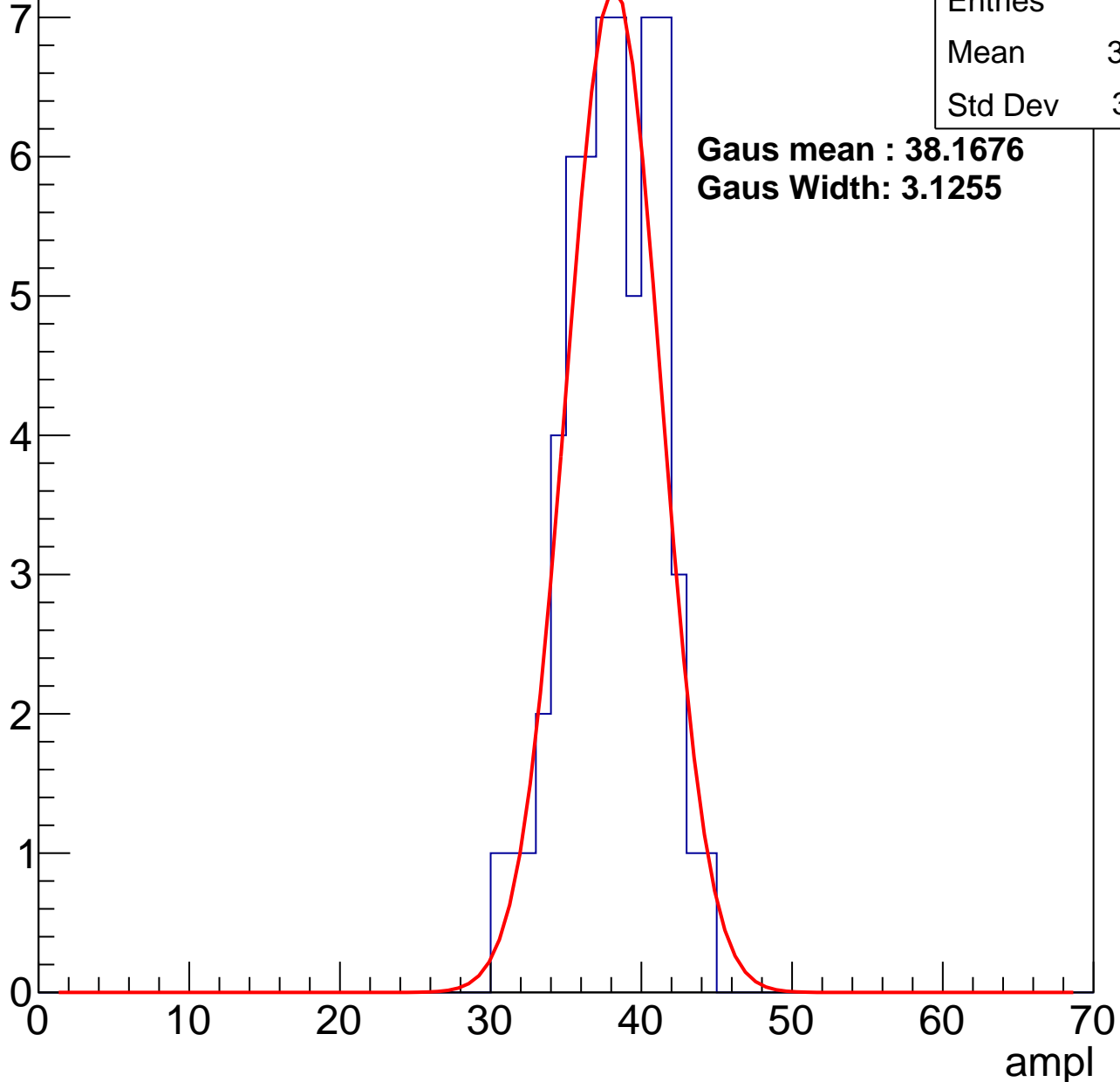
**Gaus Width: 3.4659**



# B1L100S, U6-ch65, adc1

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



# B1L100S, U6-ch65, adc2

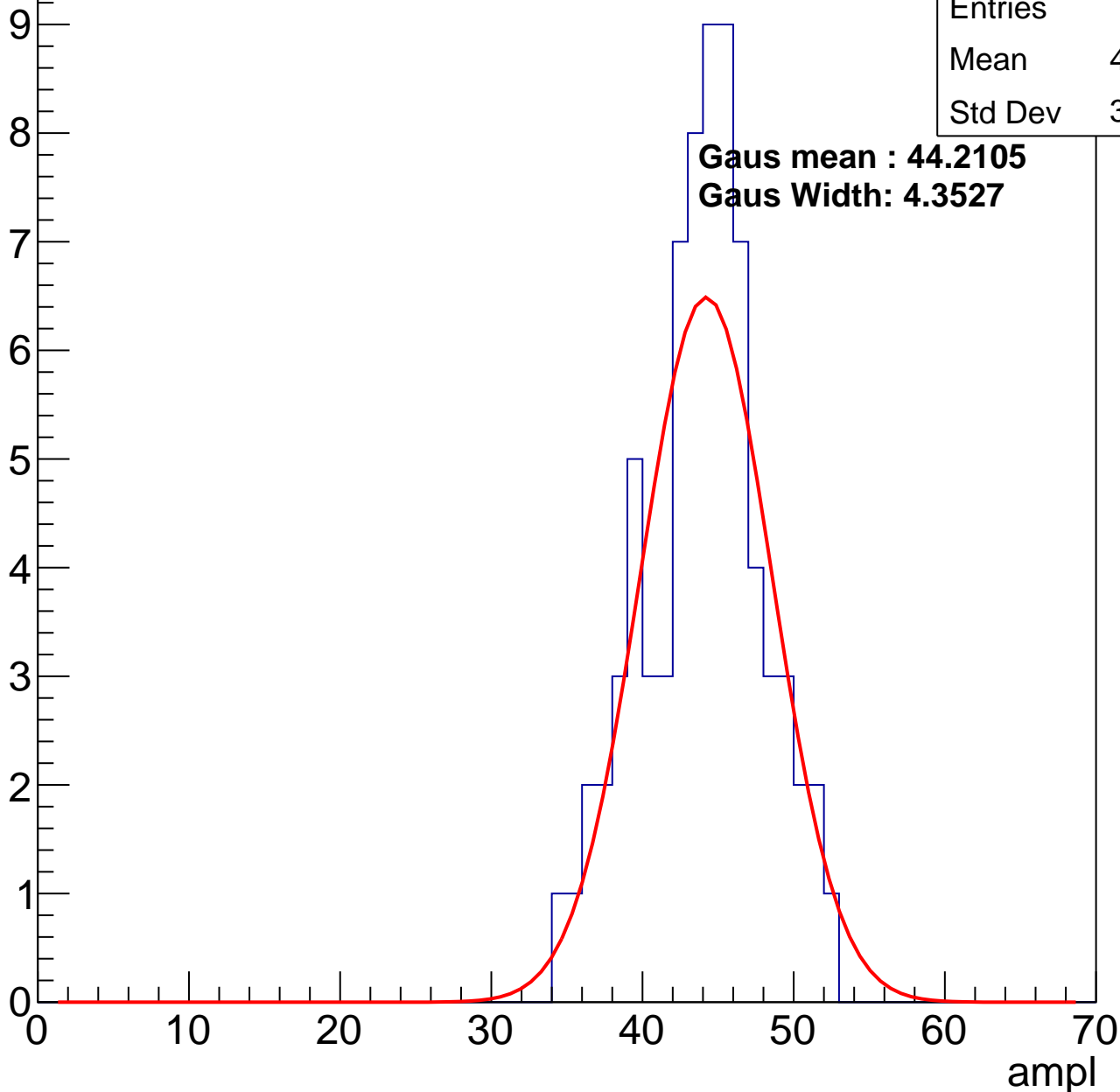
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	75
Mean	43.48
Std Dev	3.934

**Gaus mean : 44.2105**

**Gaus Width: 4.3527**

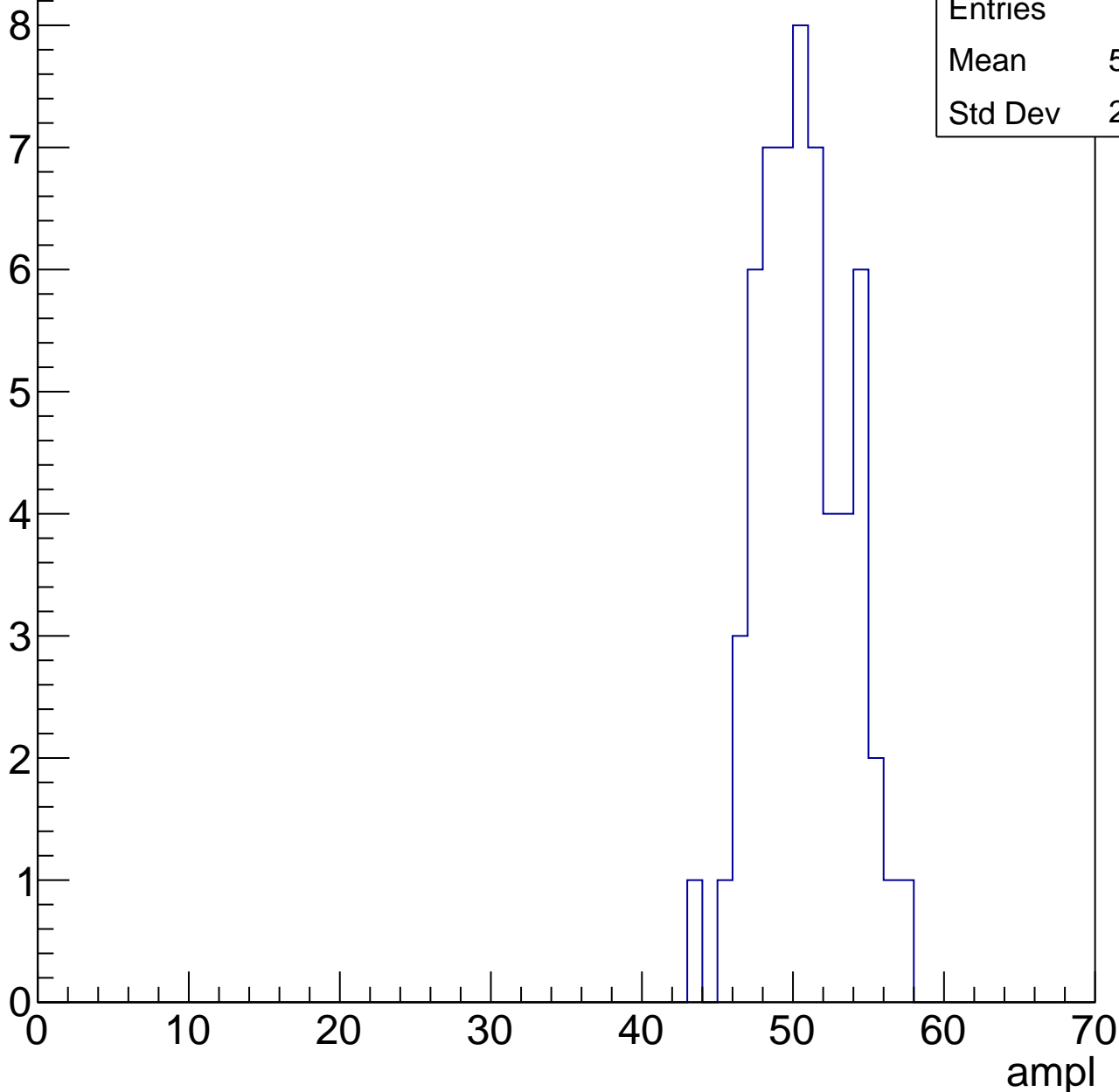


# B1L100S, U6-ch65, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

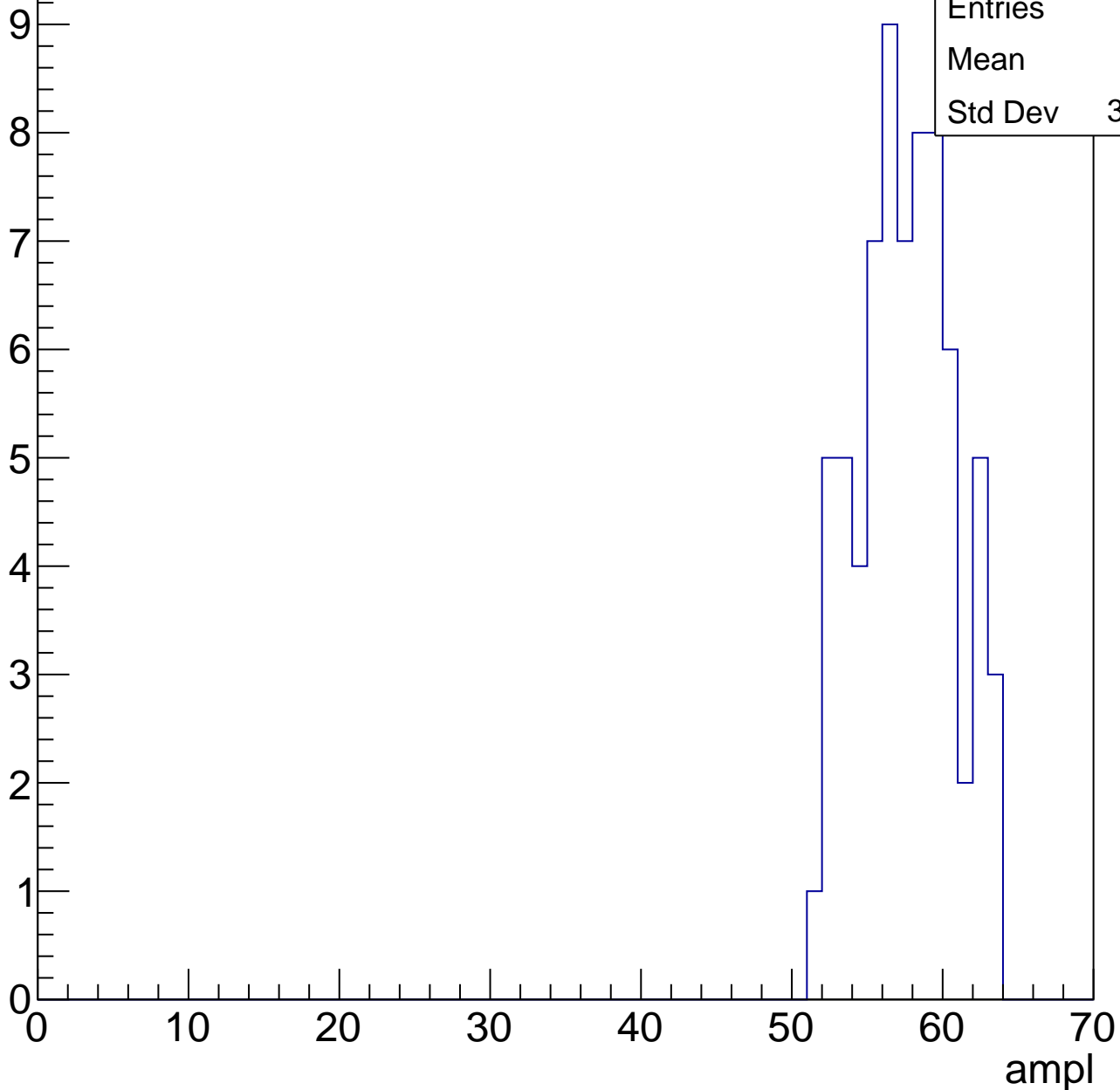
Entries	58
Mean	50.19
Std Dev	2.933



# B1L100S, U6-ch65, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	70
Mean	57.1
Std Dev	3.099

# B1L100S, U6-ch65, adc5

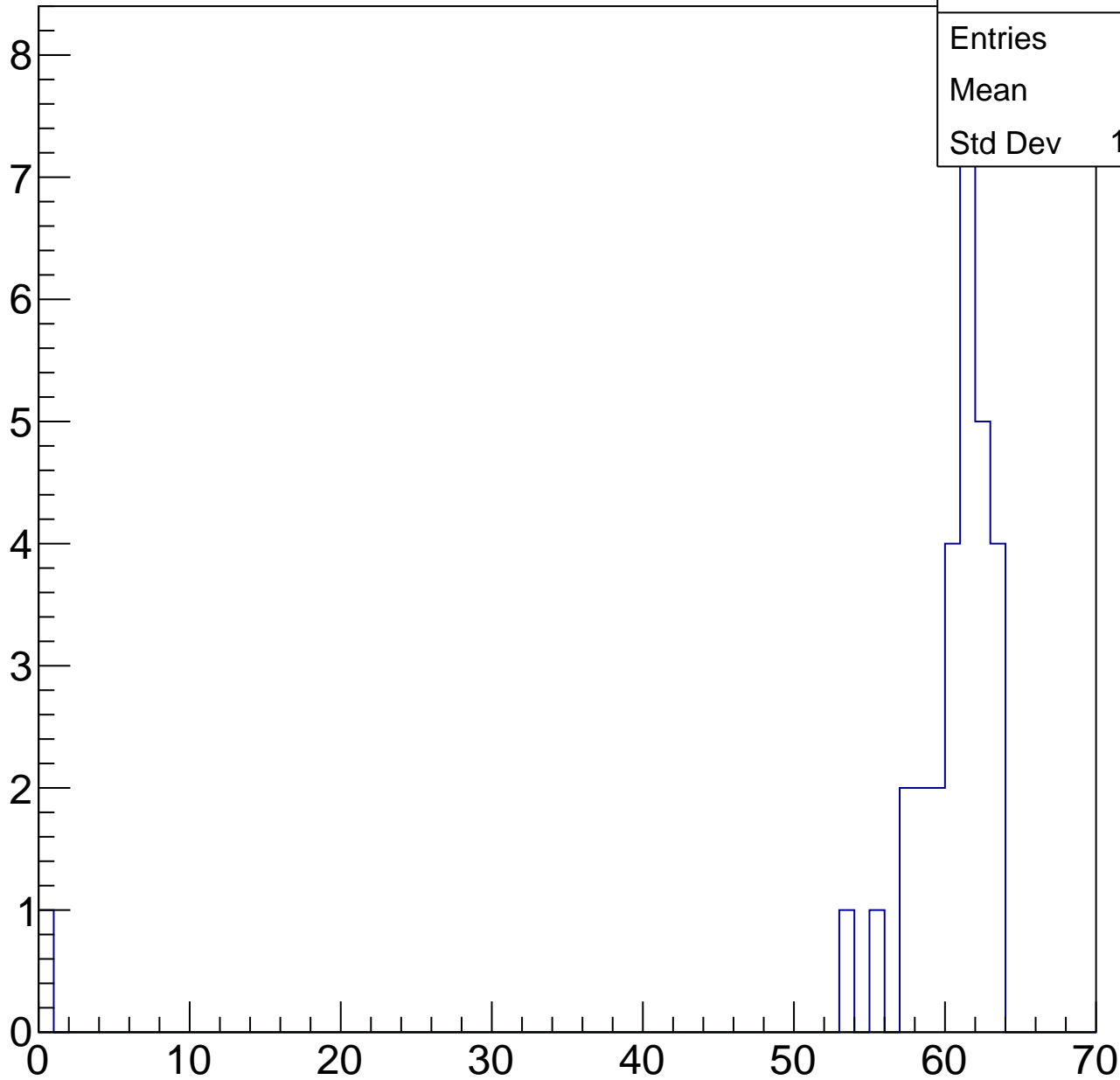
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	30
Mean	58.2
Std Dev	11.06

ampl



# B1L100S, U6-ch65, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	2
Mean	63
Std Dev	0

0 10 20 30 40 50 60 70

ampl



# B1L100S, U6-ch65, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	1
Mean	63
Std Dev	0

# B1L100S, U6-ch66, adc0

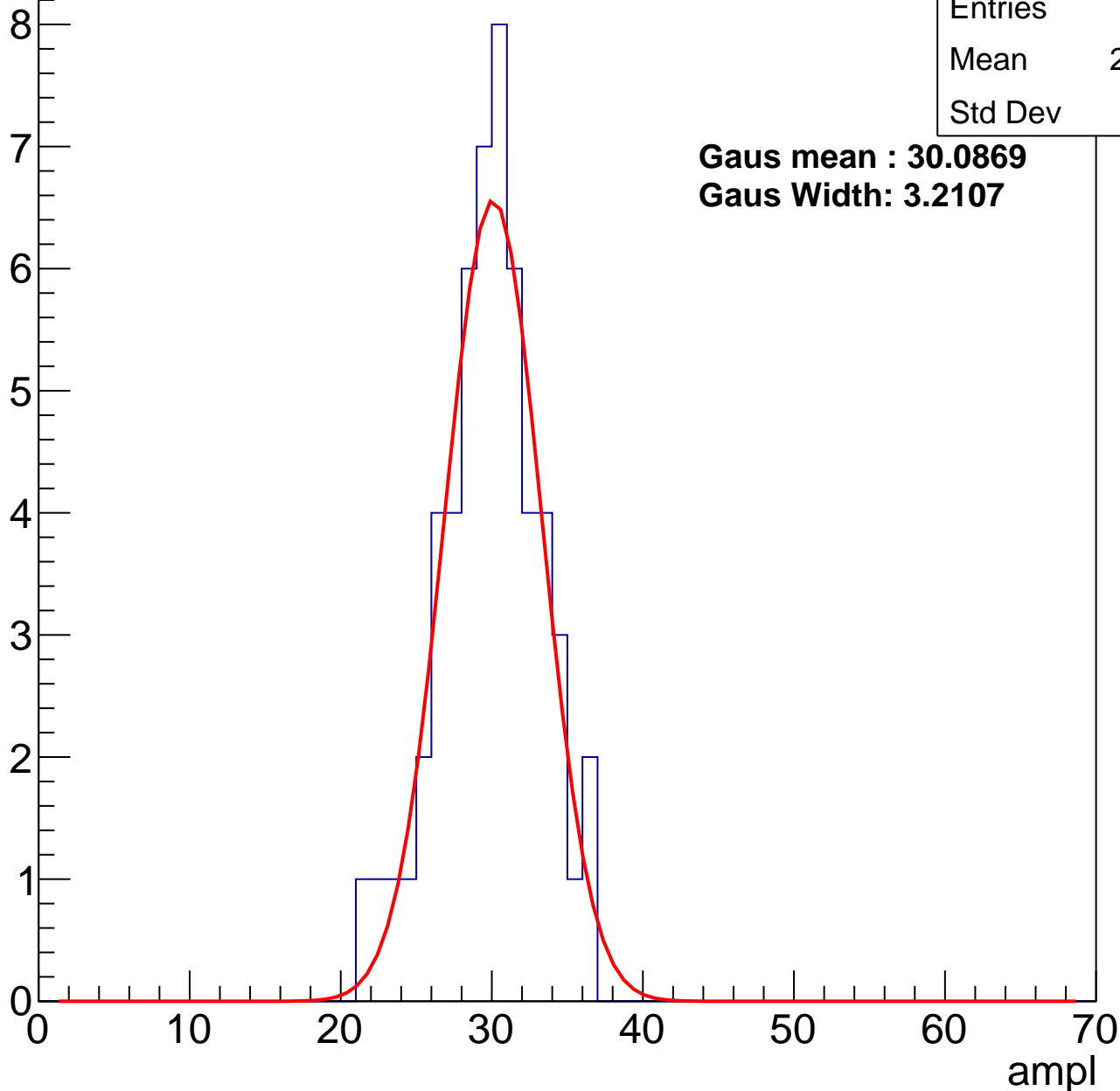
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	55
Mean	29.42
Std Dev	3.29

**Gaus mean : 30.0869**

**Gaus Width: 3.2107**



# B1L100S, U6-ch66, adc1

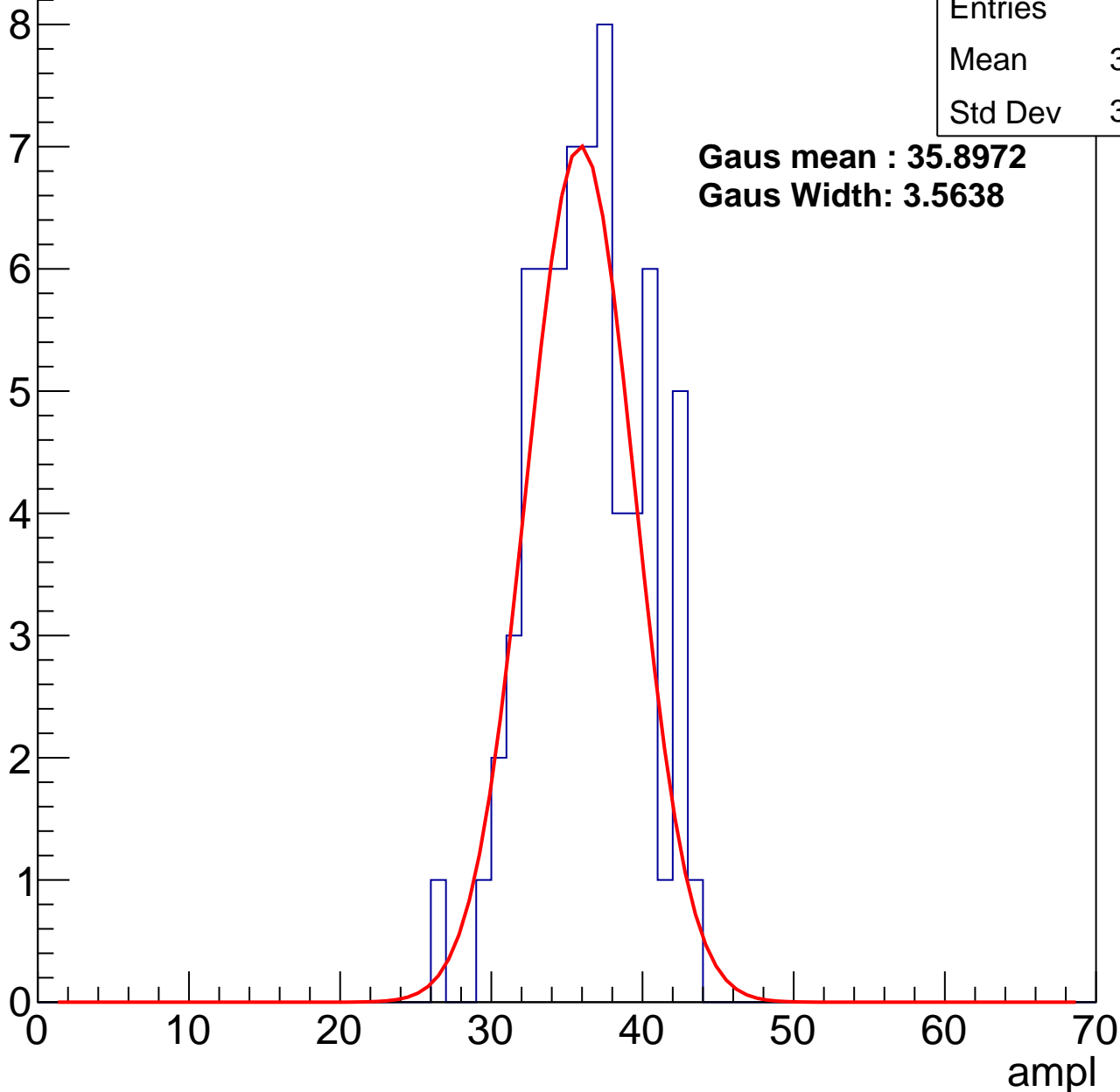
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	68
Mean	35.84
Std Dev	3.608

**Gaus mean : 35.8972**

**Gaus Width: 3.5638**



# B1L100S, U6-ch66, adc2

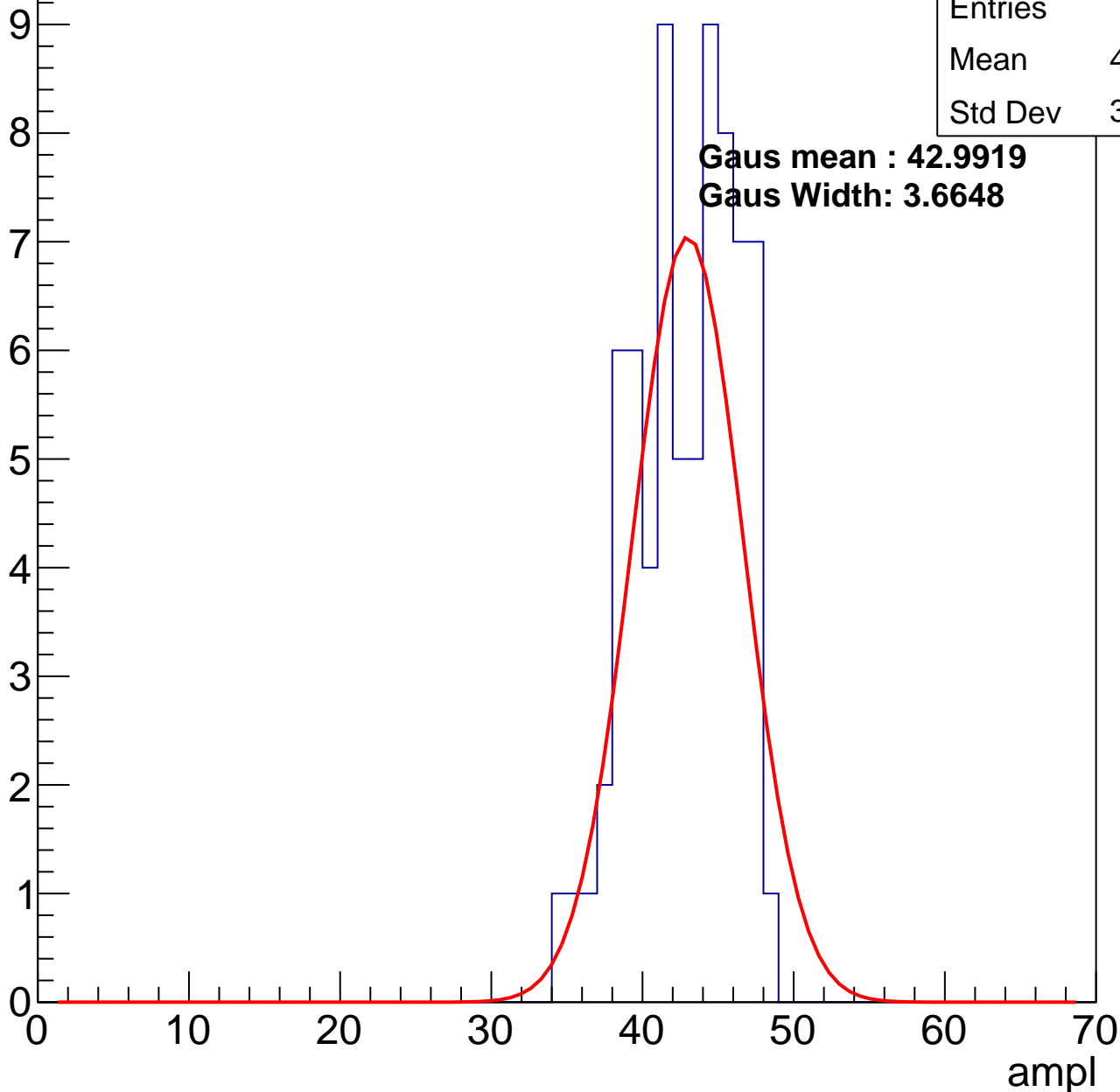
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	72
Mean	42.36
Std Dev	3.335

**Gaus mean : 42.9919**

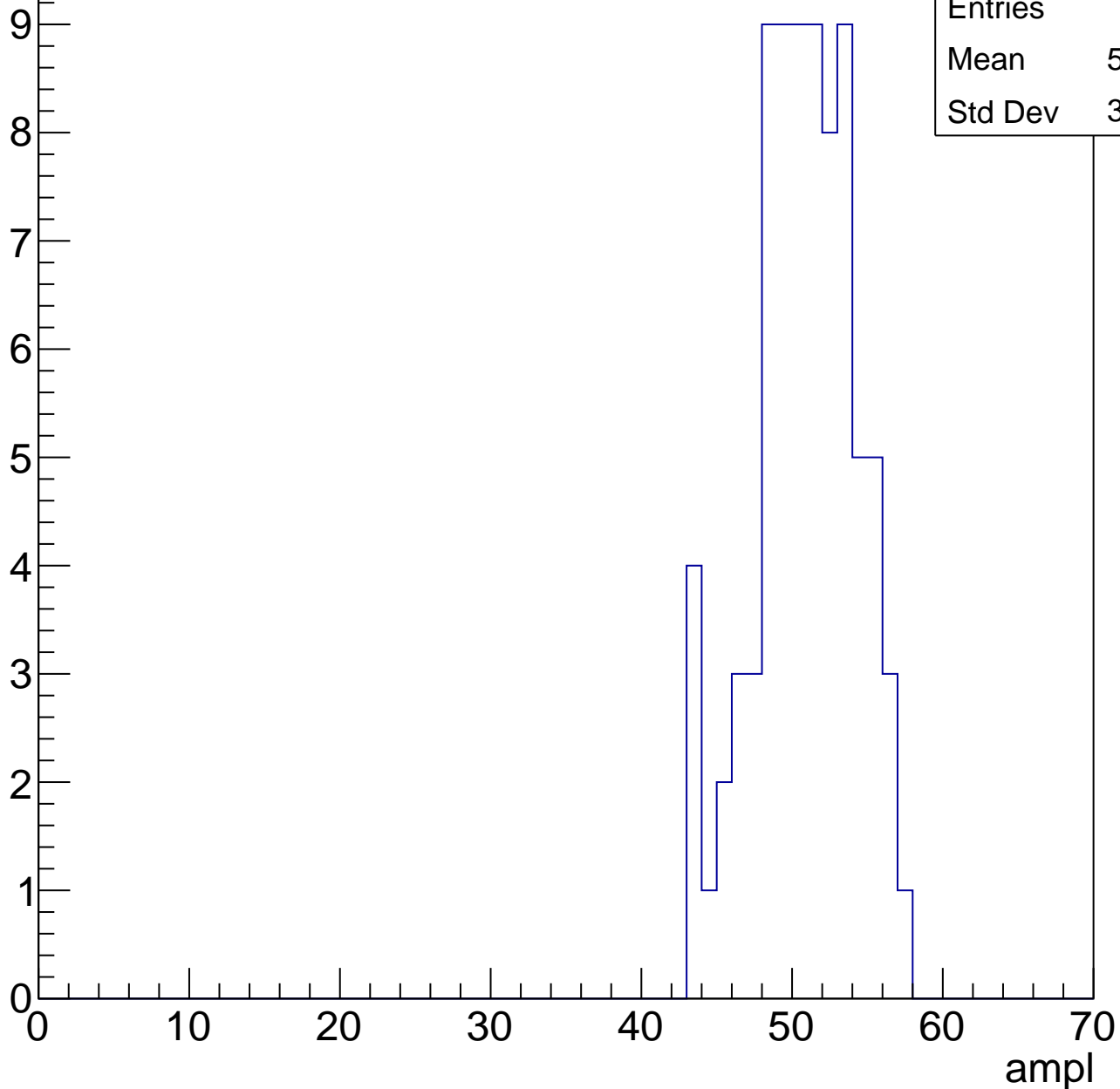
**Gaus Width: 3.6648**



# B1L100S, U6-ch66, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



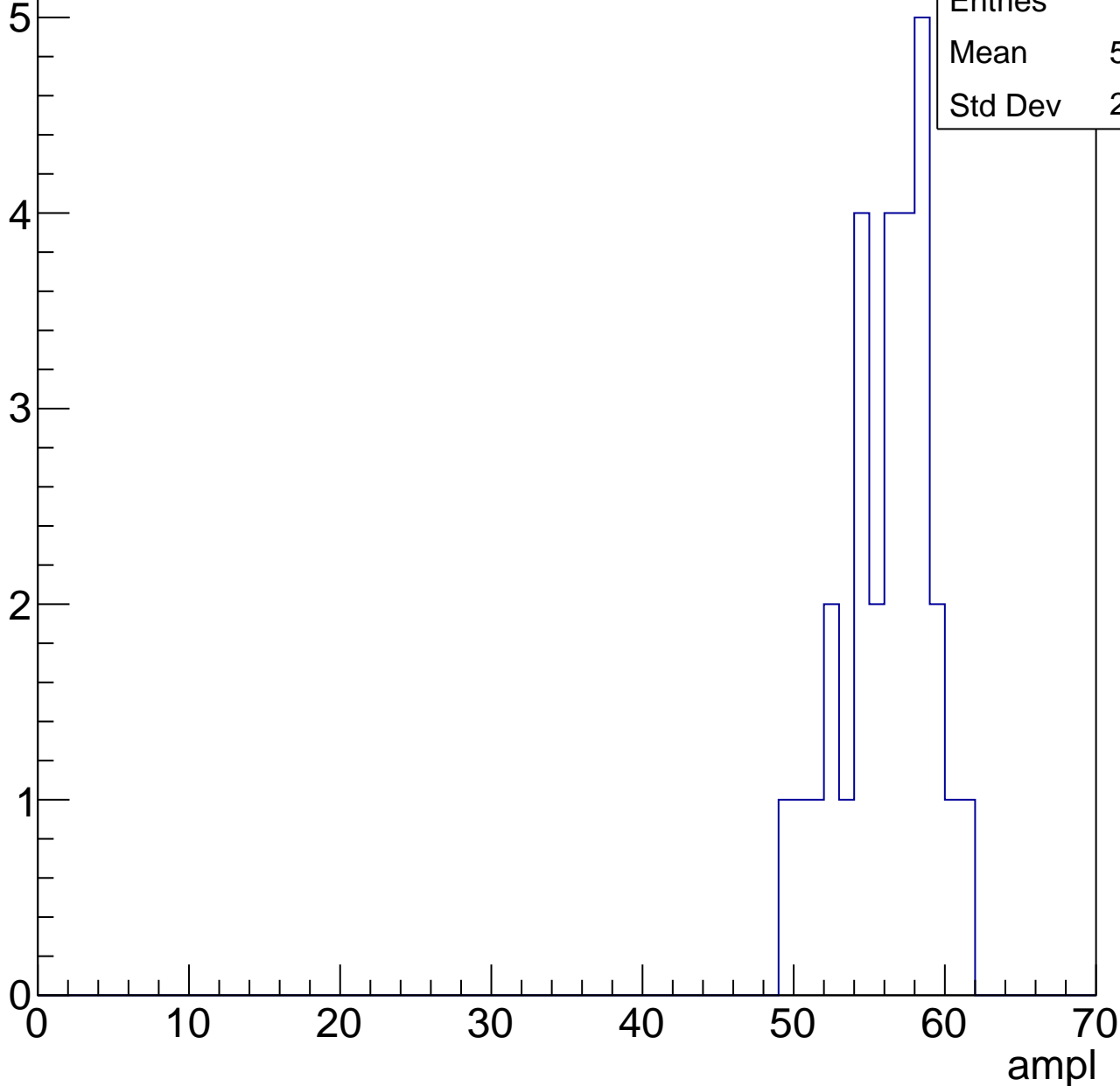
Entries	80
Mean	50.38
Std Dev	3.307

# B1L100S, U6-ch66, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	29
Mean	55.66
Std Dev	2.928



# B1L100S, U6-ch66, adc5

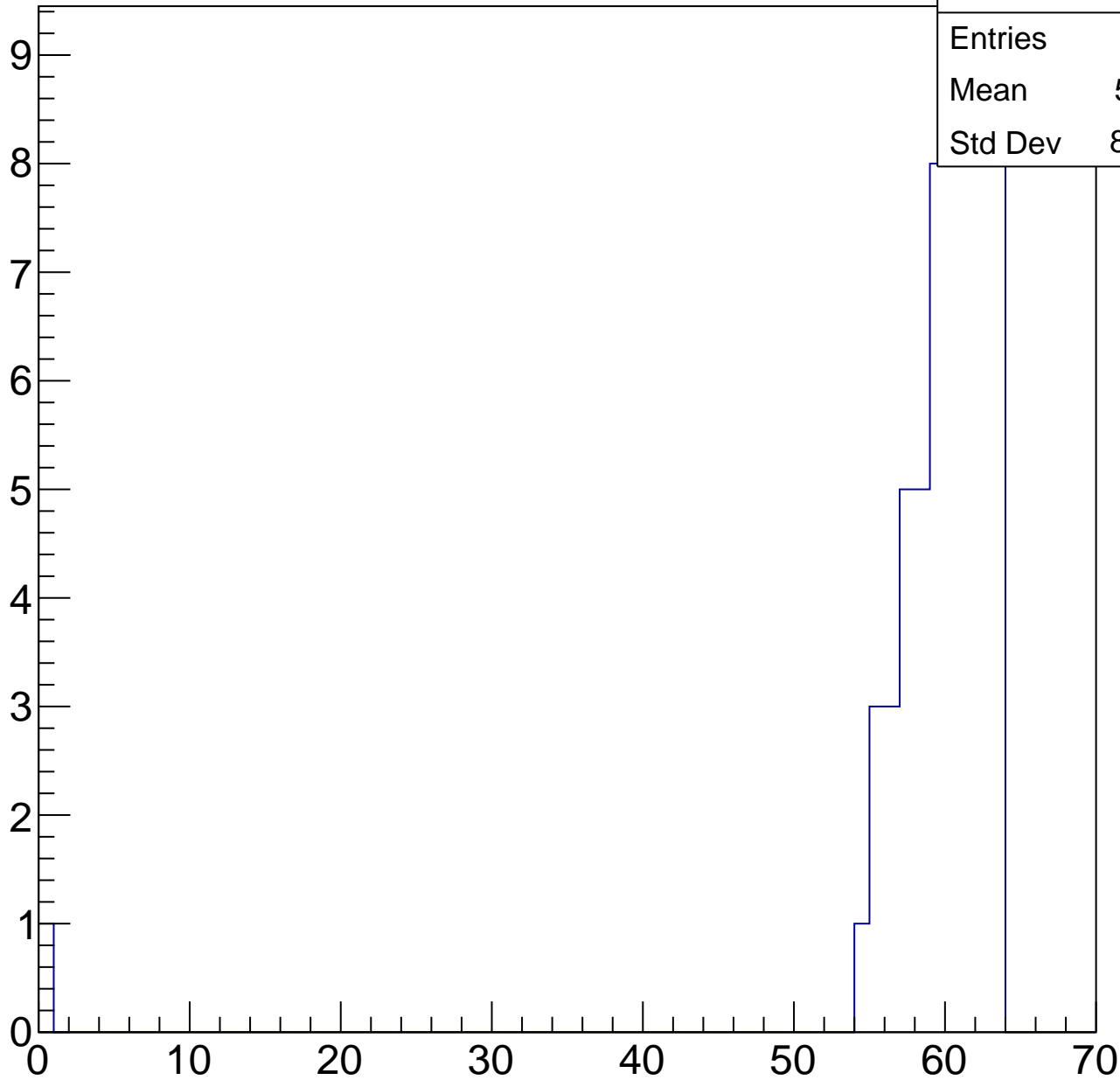
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	59
Mean	58.71
Std Dev	8.078

ampl



# B1L100S, U6-ch66, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

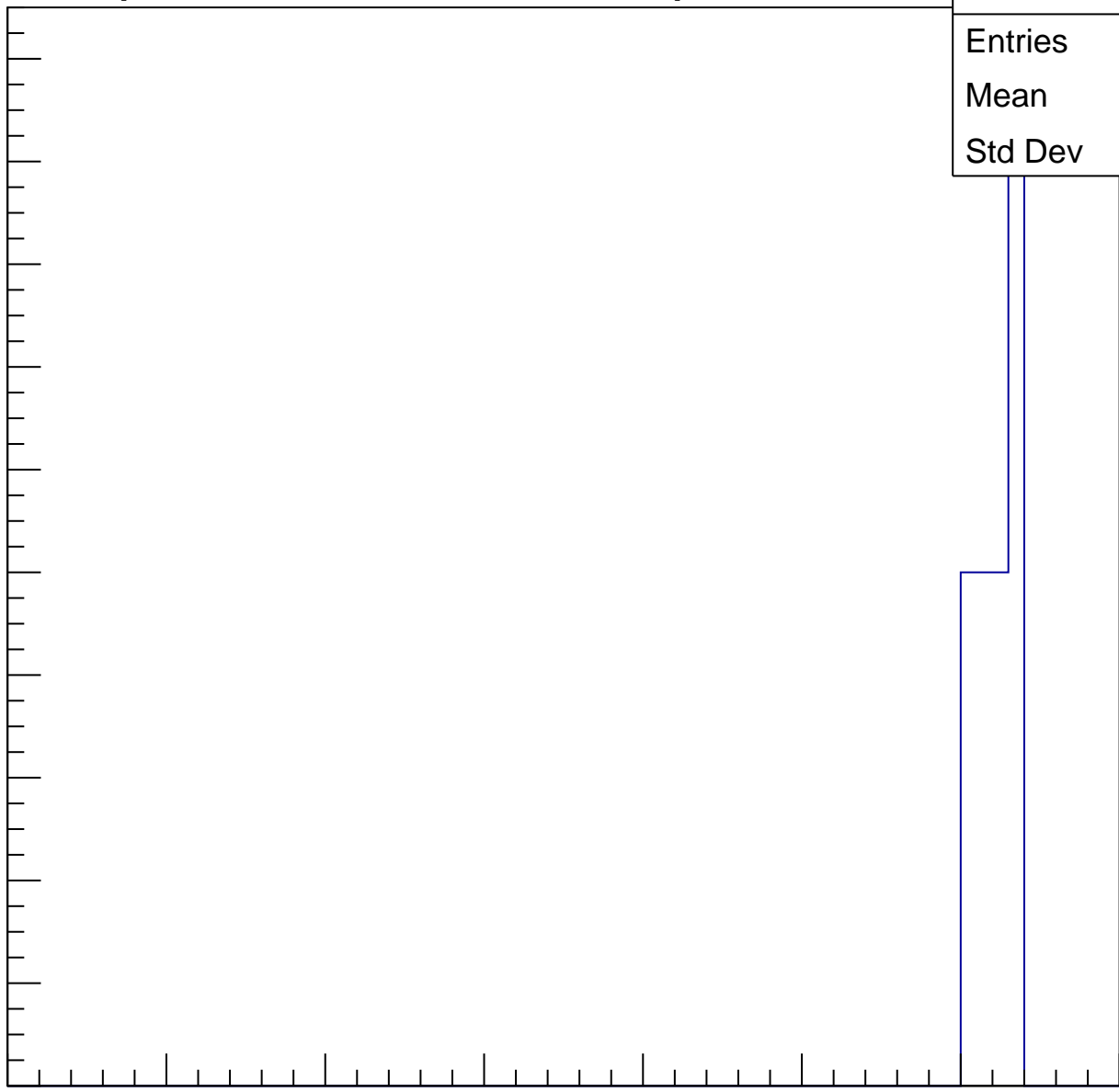
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	5
Mean	61.8
Std Dev	1.166

ampl

0 10 20 30 40 50 60 70





# B1L100S, U6-ch66, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L100S, U6-ch67, adc0

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	81
Mean	29.91
Std Dev	4.816

**Gaus mean : 30.7790**

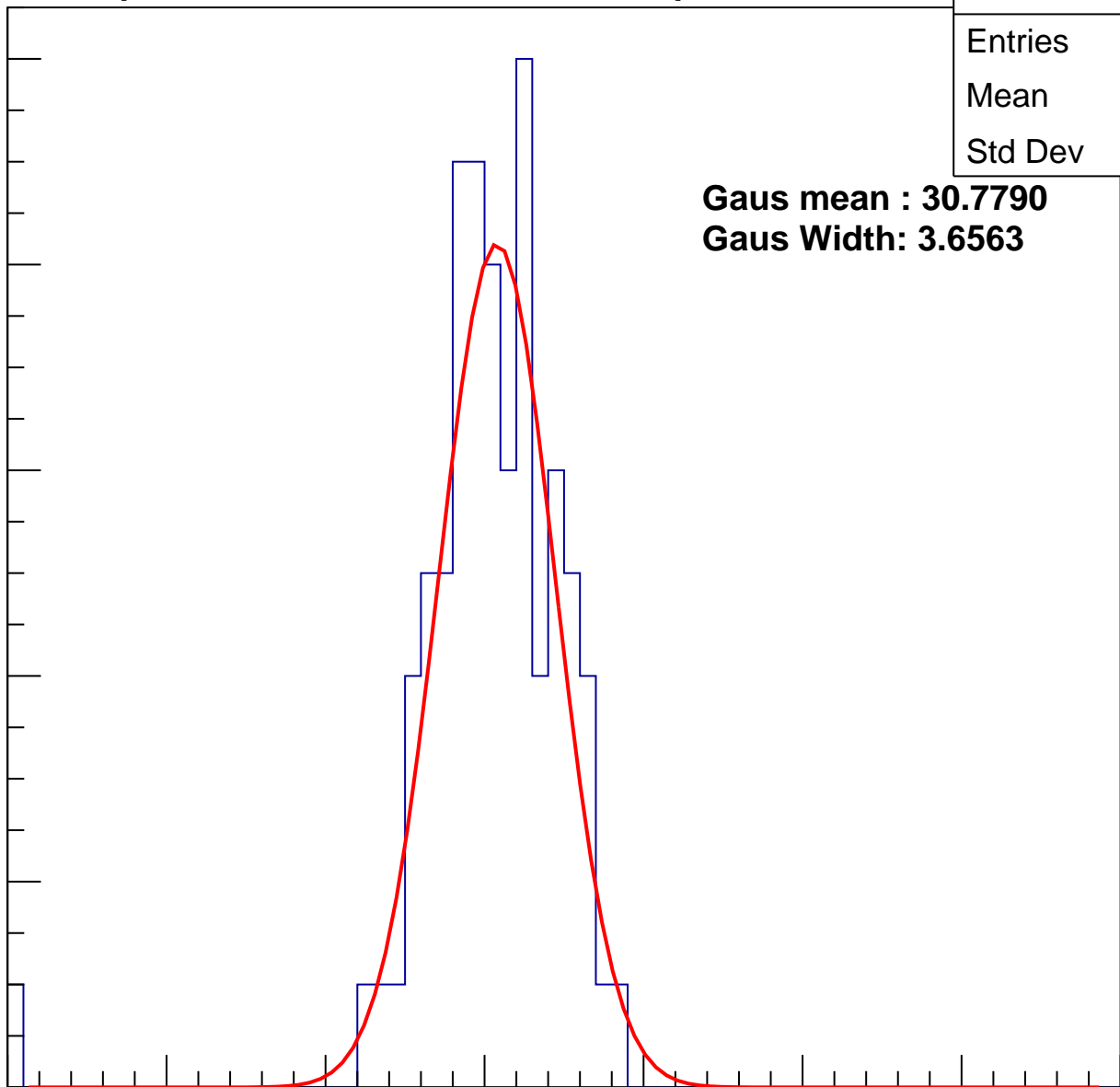
**Gaus Width: 3.6563**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L100S, U6-ch67, adc1

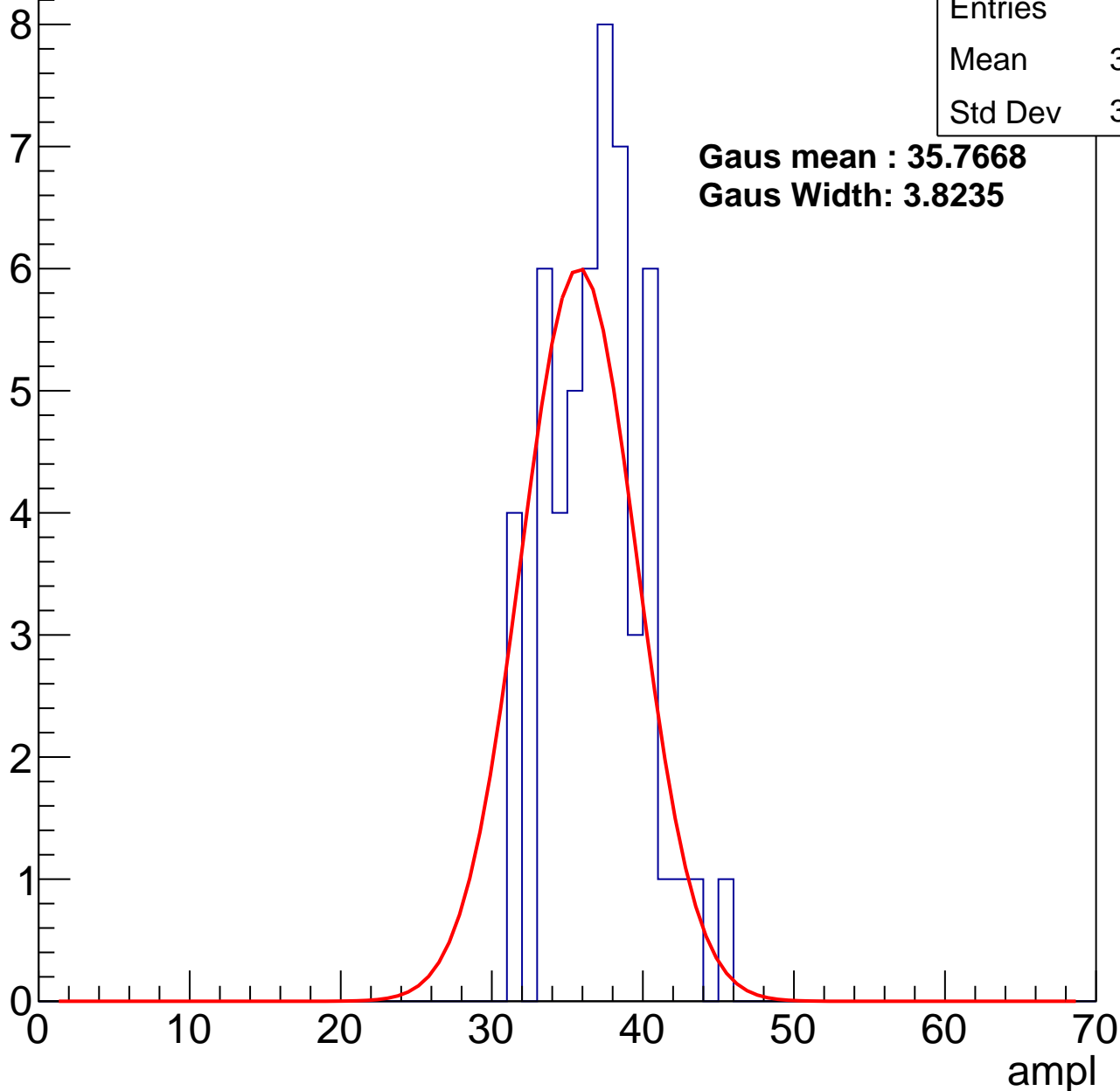
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	53
Mean	36.58
Std Dev	3.092

**Gaus mean : 35.7668**

**Gaus Width: 3.8235**



# B1L100S, U6-ch67, adc2

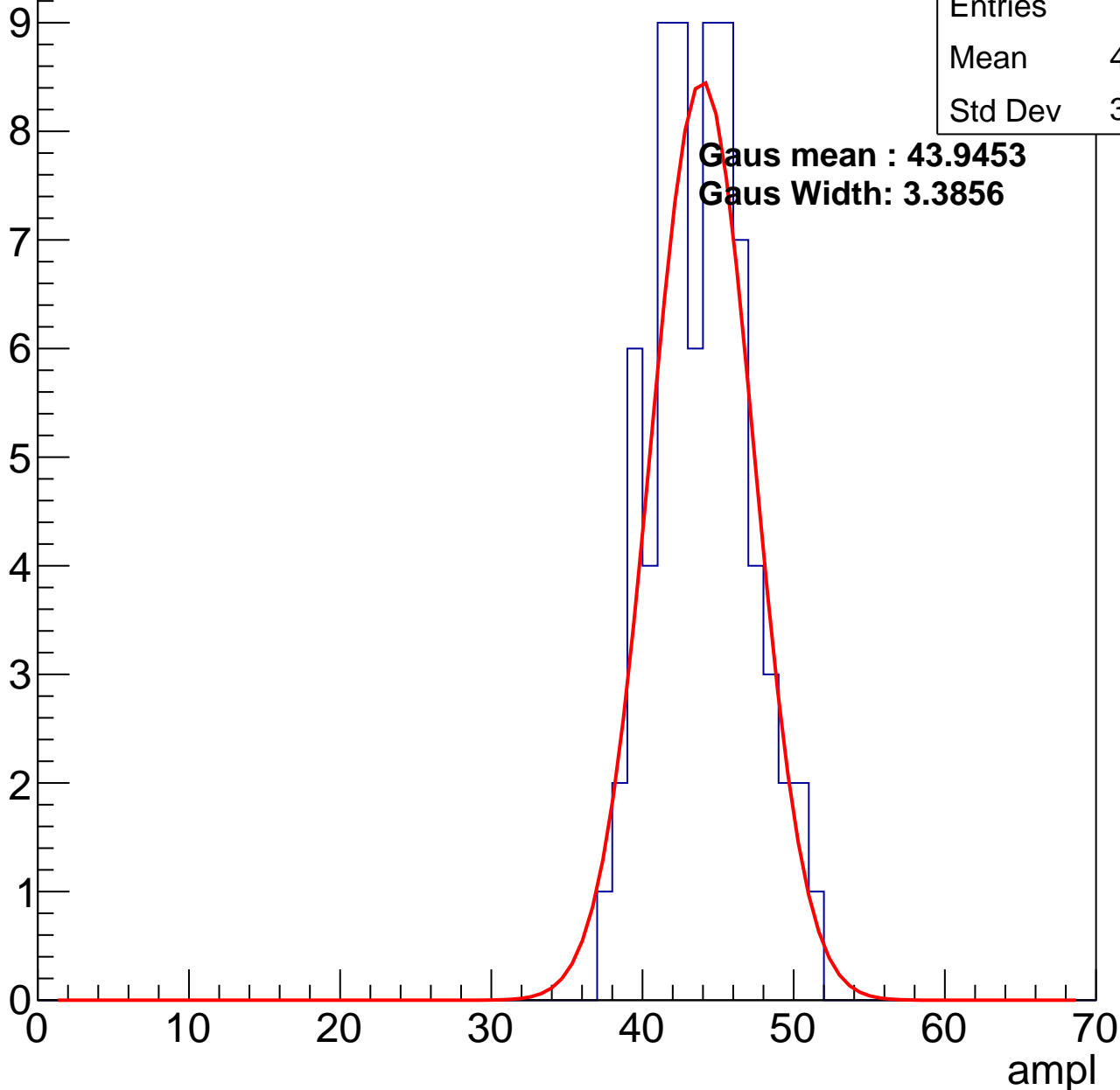
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	74
Mean	43.46
Std Dev	3.137

**Gaus mean : 43.9453**

**Gaus Width: 3.3856**

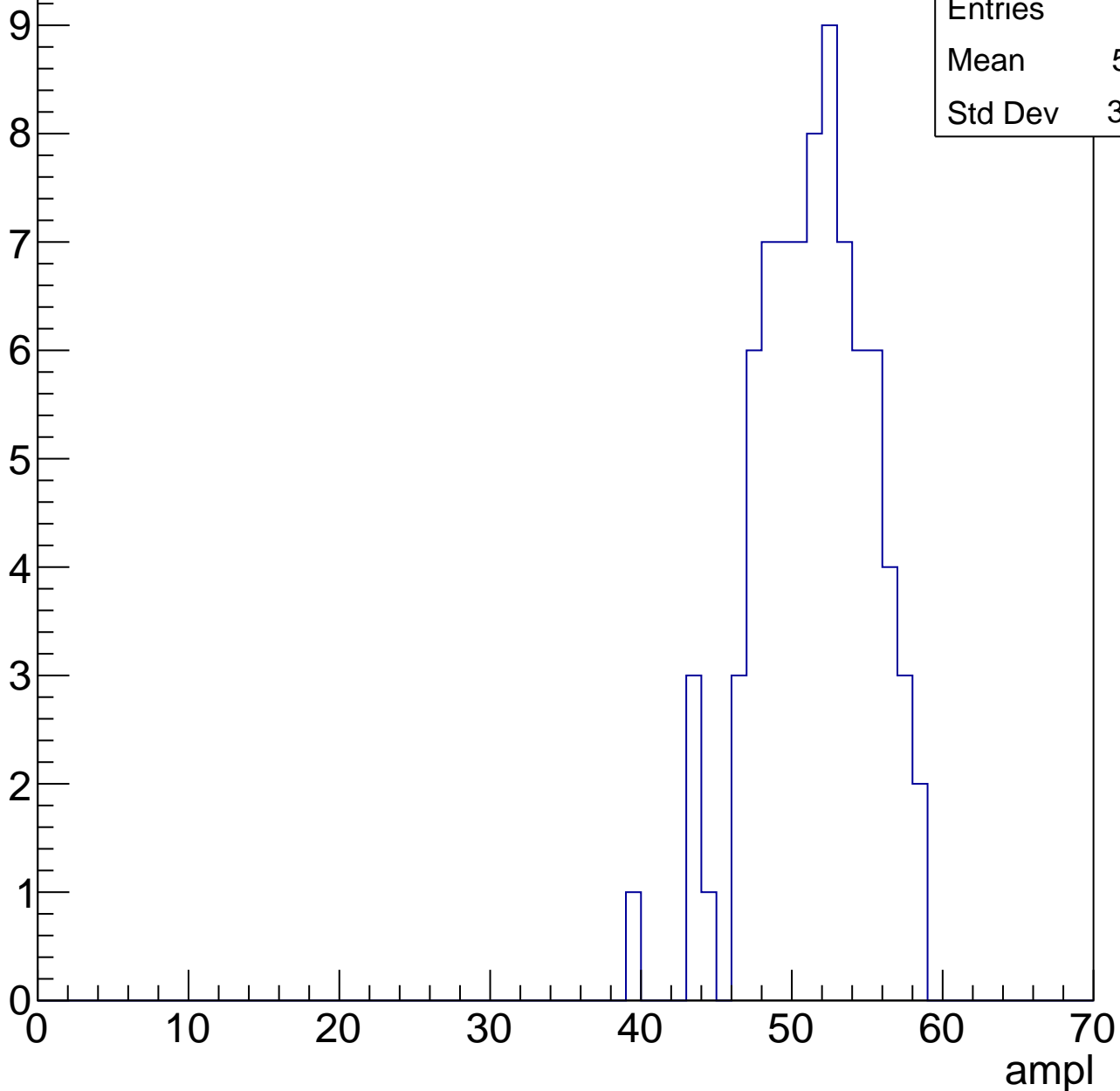


# B1L100S, U6-ch67, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

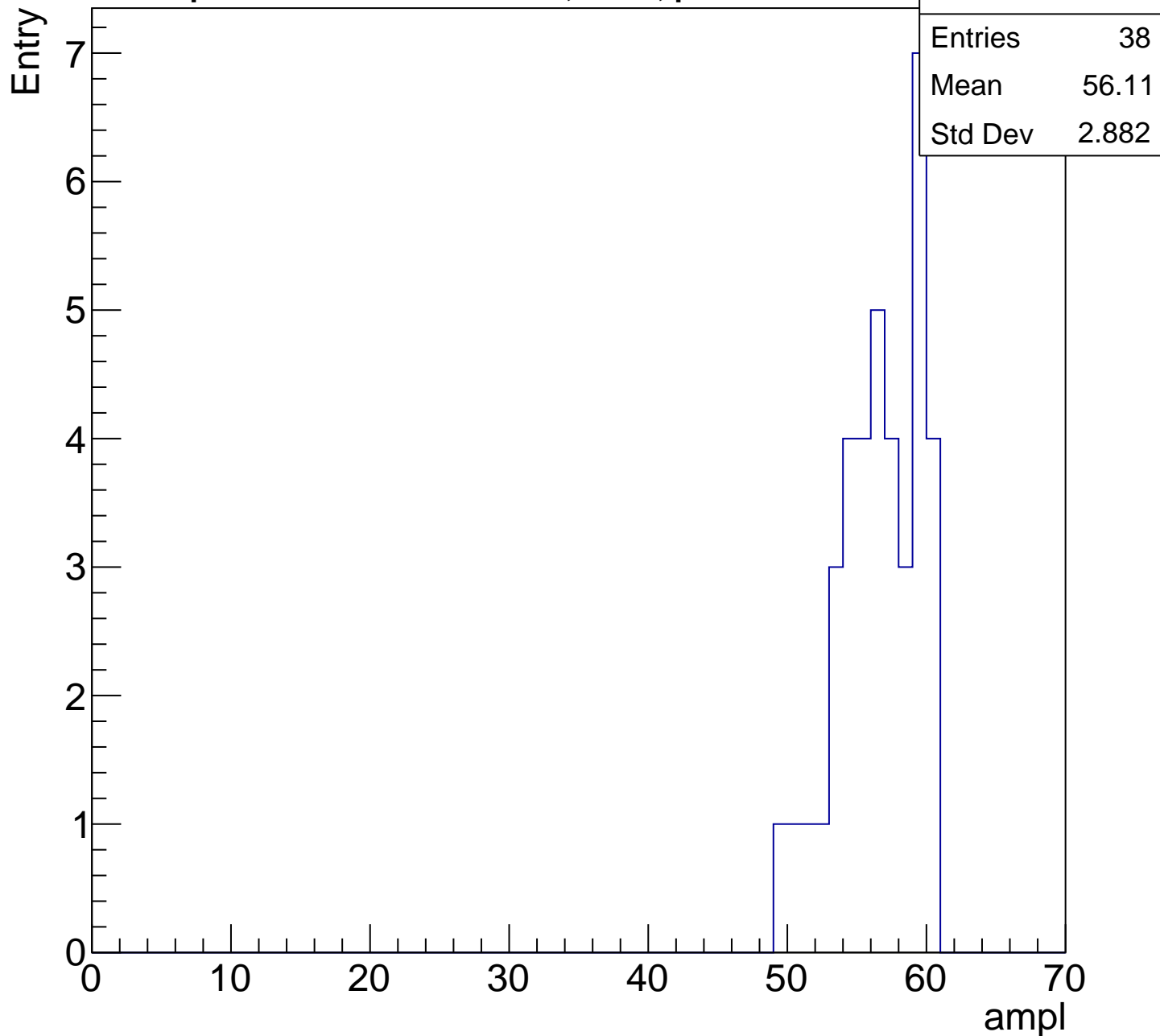
Entry

Entries	80
Mean	50.91
Std Dev	3.785



# B1L100S, U6-ch67, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2



# B1L100S, U6-ch67, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

10

Entries 47

Mean 59.34

Std Dev 8.959

8

6

4

2

0

0

10

20

30

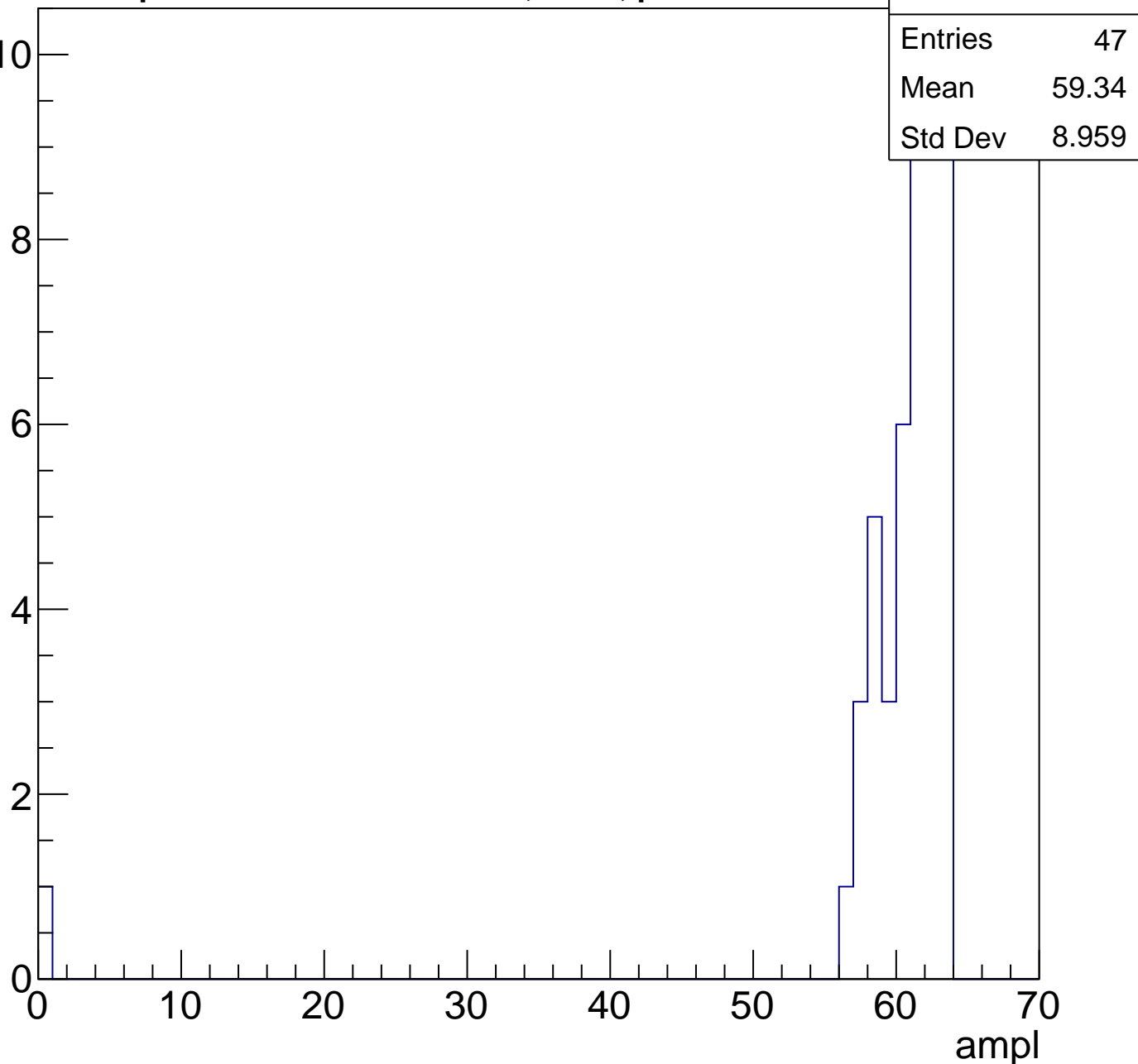
40

50

60

70

ampl



# B1L100S, U6-ch67, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry





# B1L100S, U6-ch67, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L100S, U6-ch68, adc0

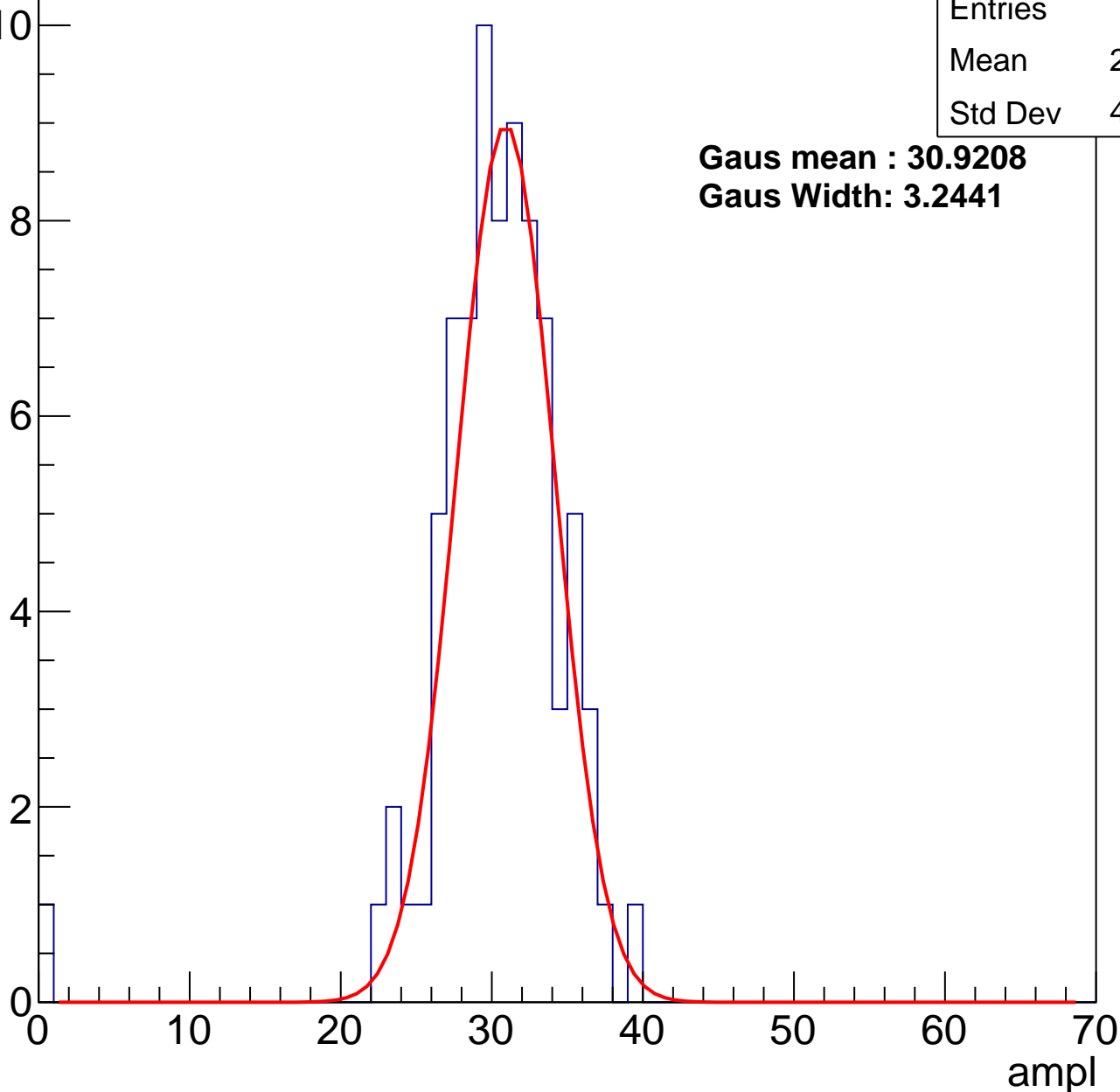
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	80
Mean	29.86
Std Dev	4.766

**Gaus mean : 30.9208**

**Gaus Width: 3.2441**



# B1L100S, U6-ch68, adc1

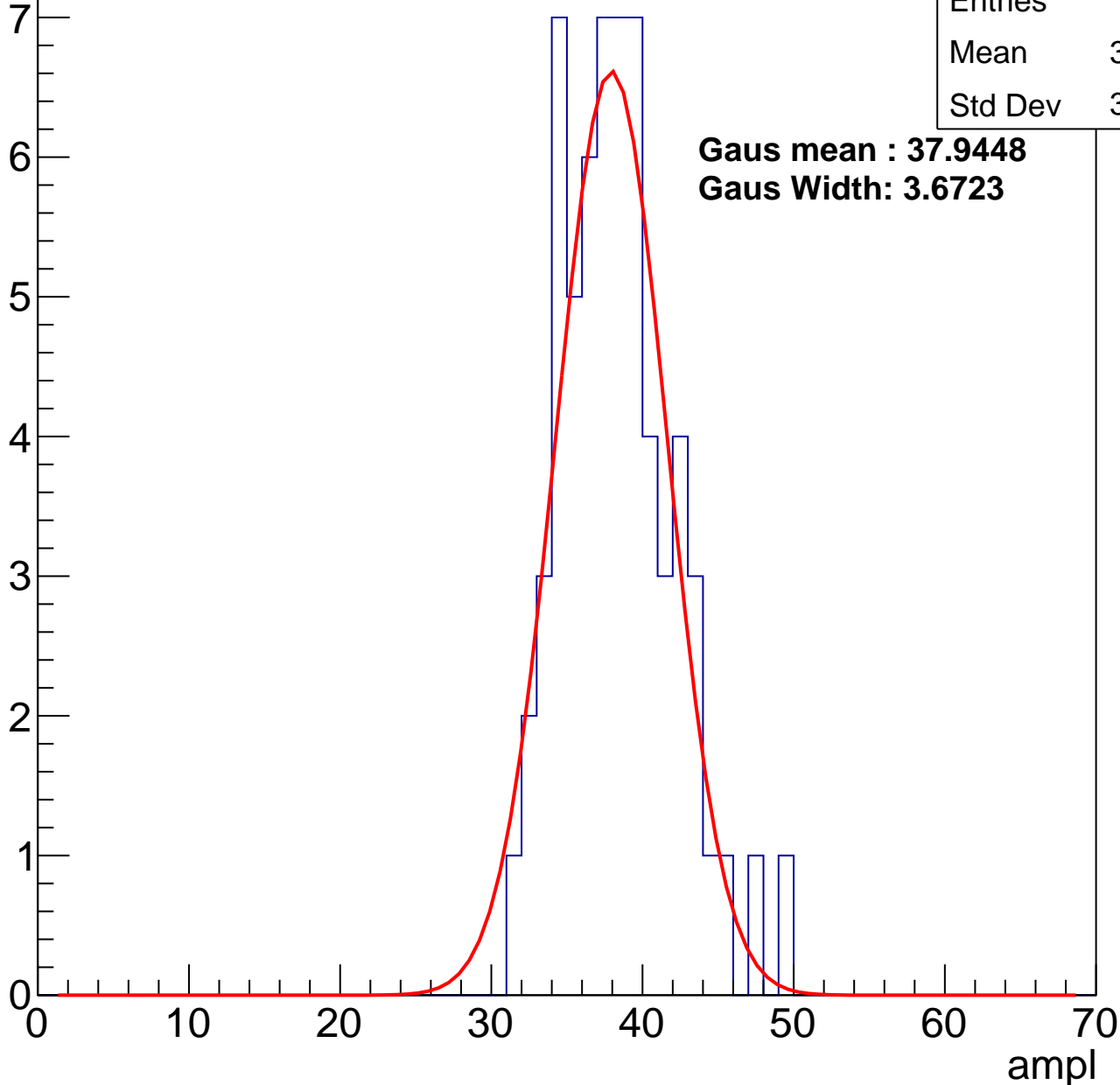
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	63
Mean	37.87
Std Dev	3.693

**Gaus mean : 37.9448**

**Gaus Width: 3.6723**



# B1L100S, U6-ch68, adc2

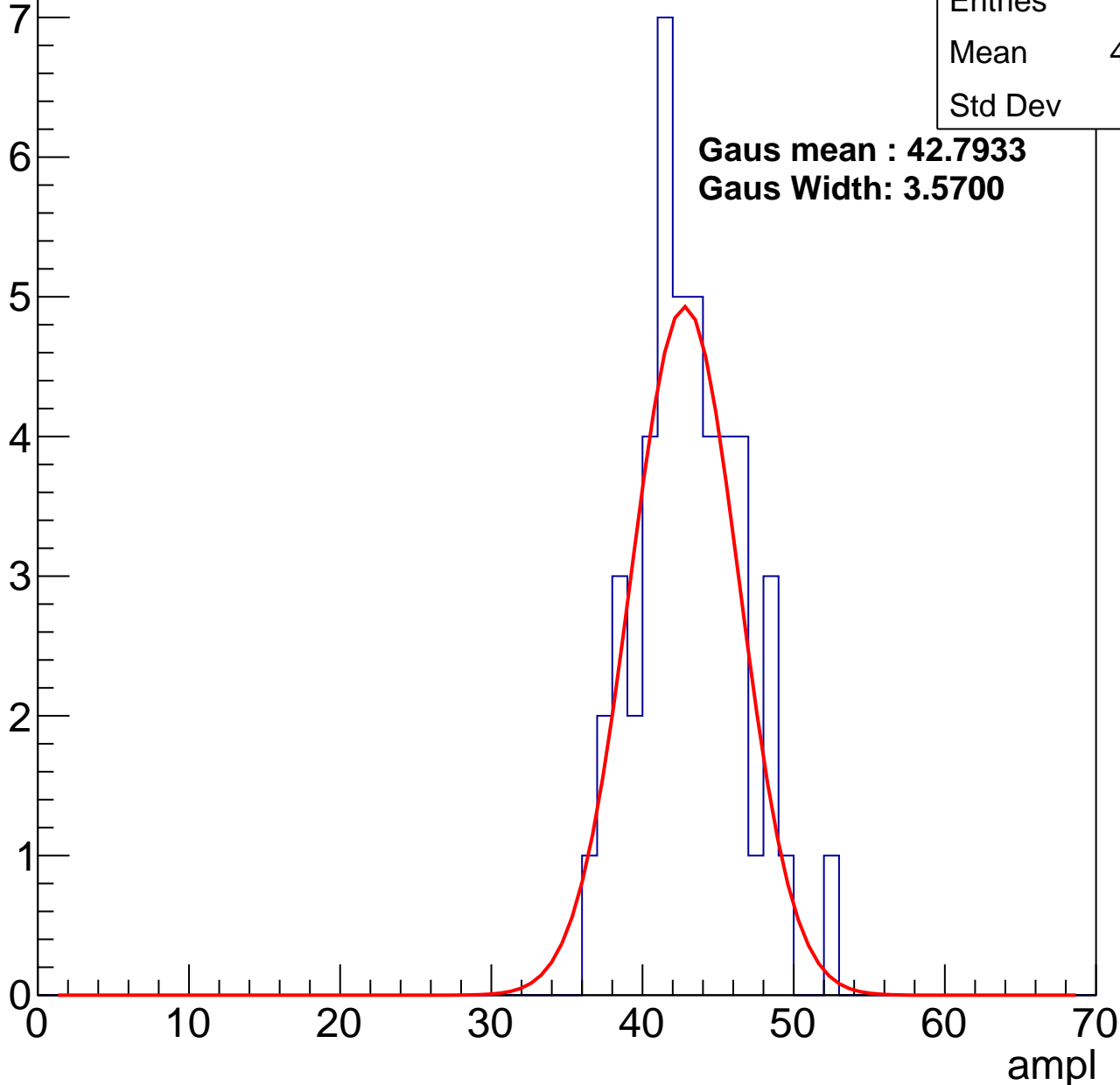
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	47
Mean	42.68
Std Dev	3.44

**Gaus mean : 42.7933**

**Gaus Width: 3.5700**

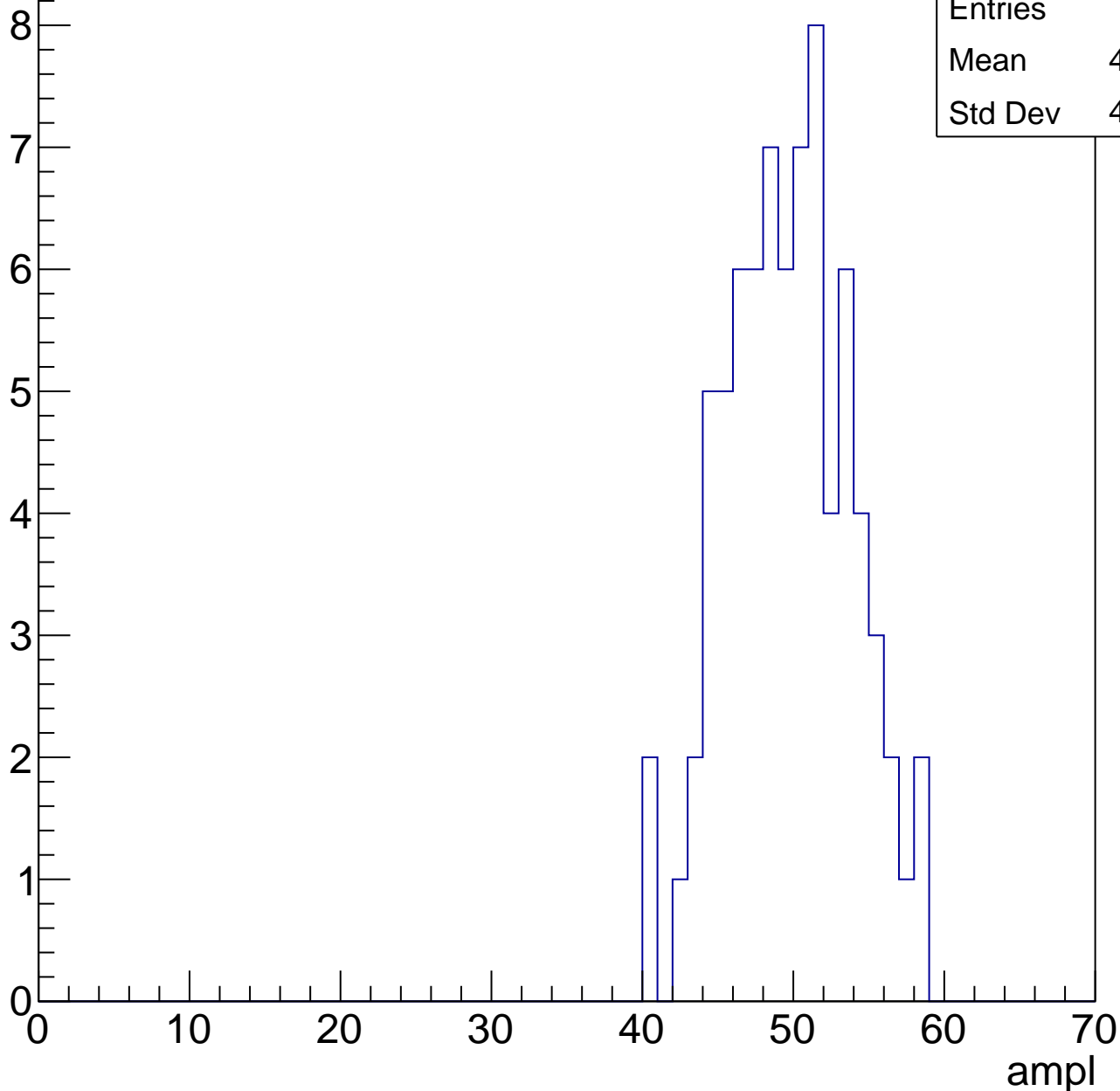


# B1L100S, U6-ch68, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	77
Mean	49.23
Std Dev	4.064

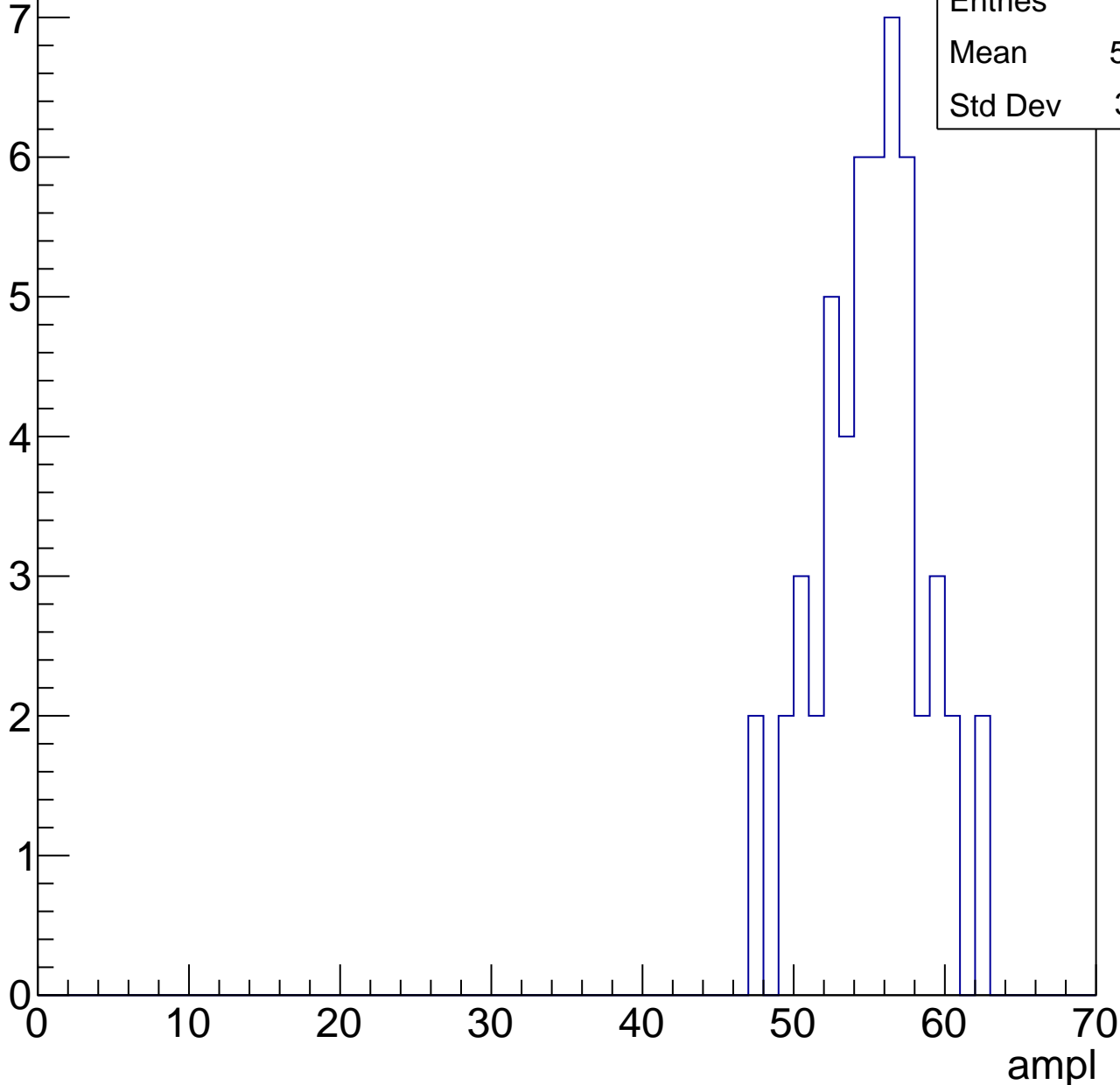


# B1L100S, U6-ch68, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	52
Mean	54.63
Std Dev	3.431



# B1L100S, U6-ch68, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	51
Mean	59.04
Std Dev	8.593

ampl

0

10

20

30

40

50

60

70

# B1L100S, U6-ch68, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	4
Mean	62
Std Dev	0.7071

ampl

0 10 20 30 40 50 60 70



# B1L100S, U6-ch68, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



# B1L100S, U6-ch69, adc0

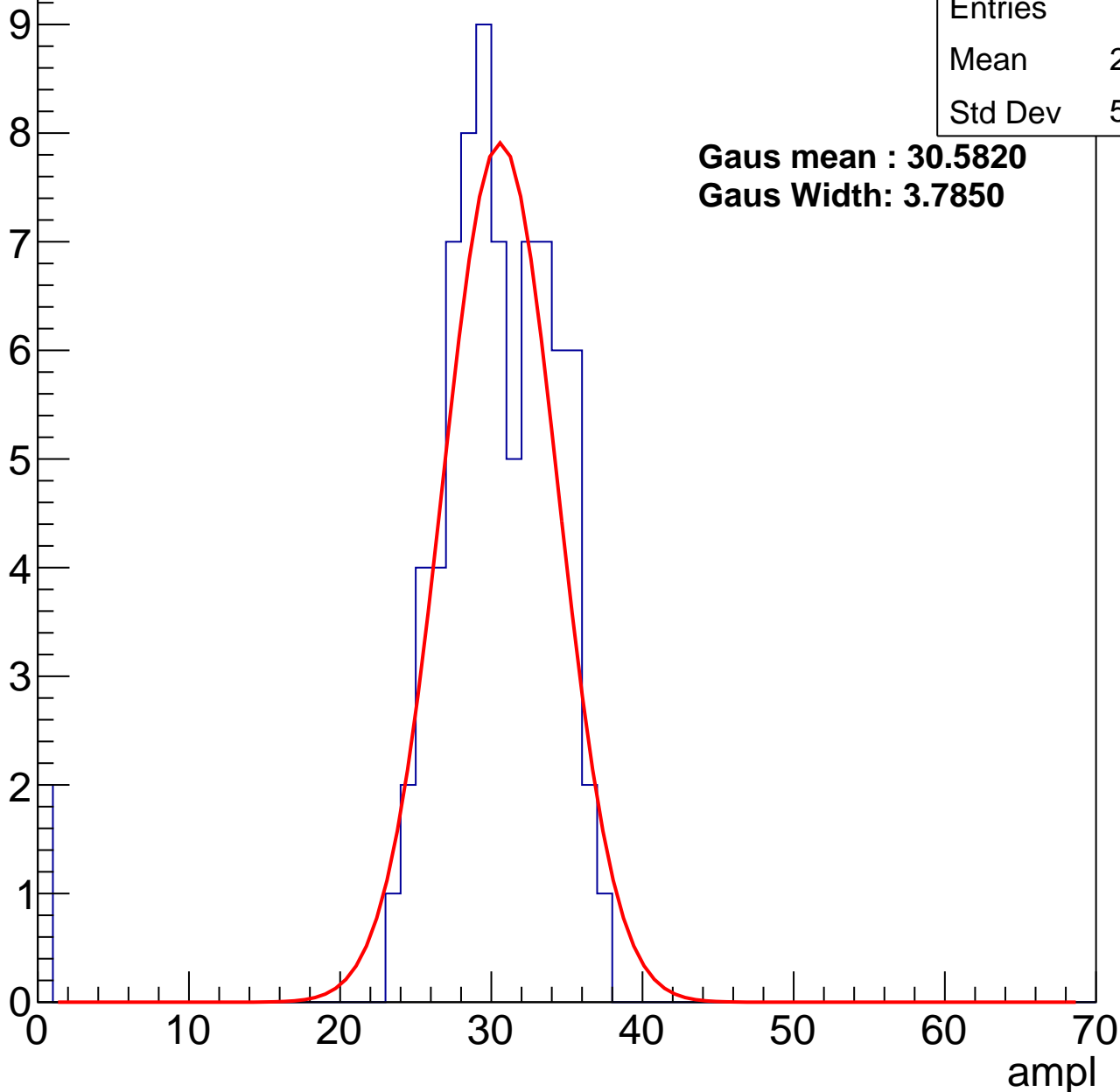
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	78
Mean	29.38
Std Dev	5.798

**Gaus mean : 30.5820**

**Gaus Width: 3.7850**



# B1L100S, U6-ch69, adc1

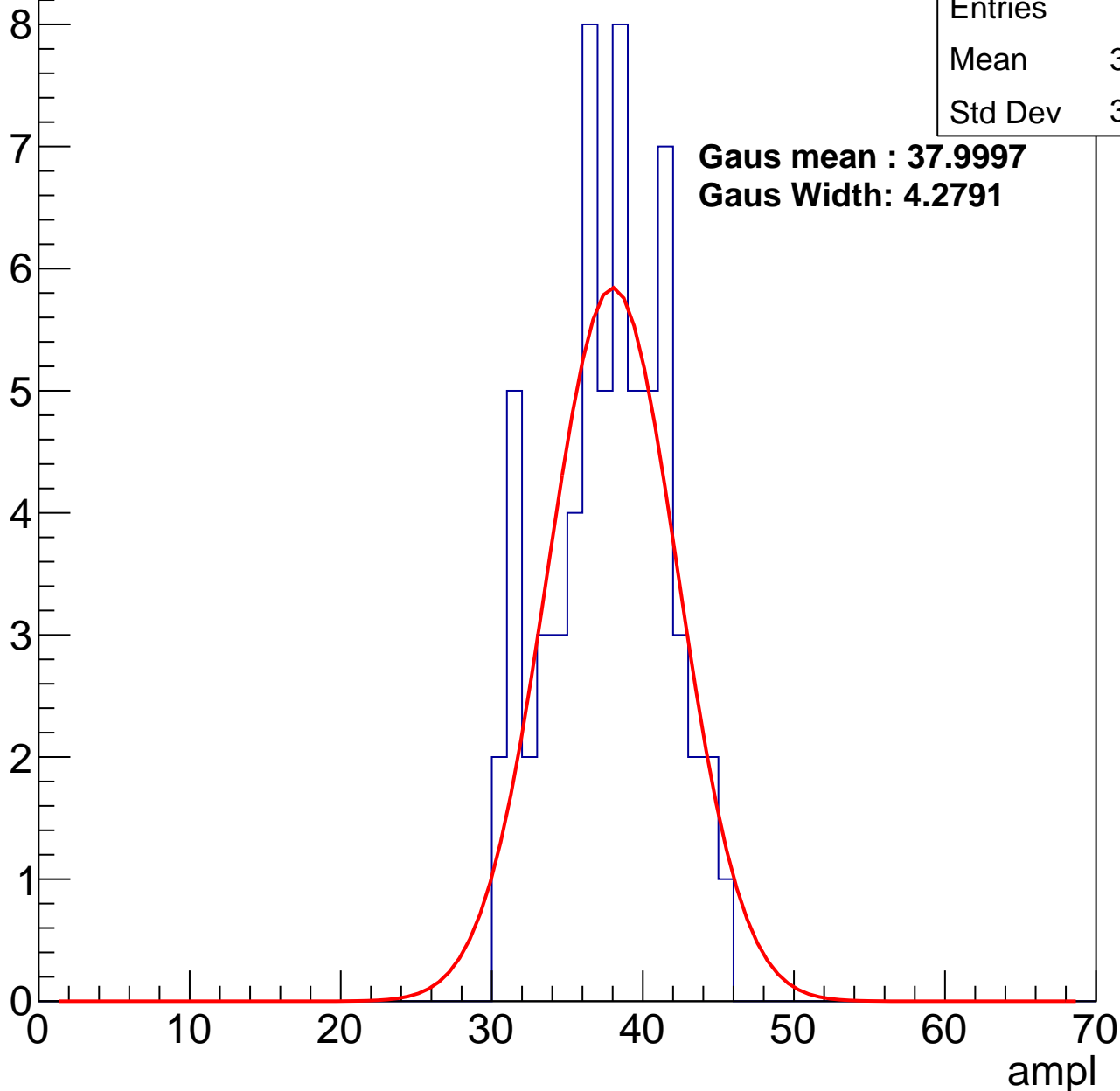
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	65
Mean	37.29
Std Dev	3.753

**Gaus mean : 37.9997**

**Gaus Width: 4.2791**



# B1L100S, U6-ch69, adc2

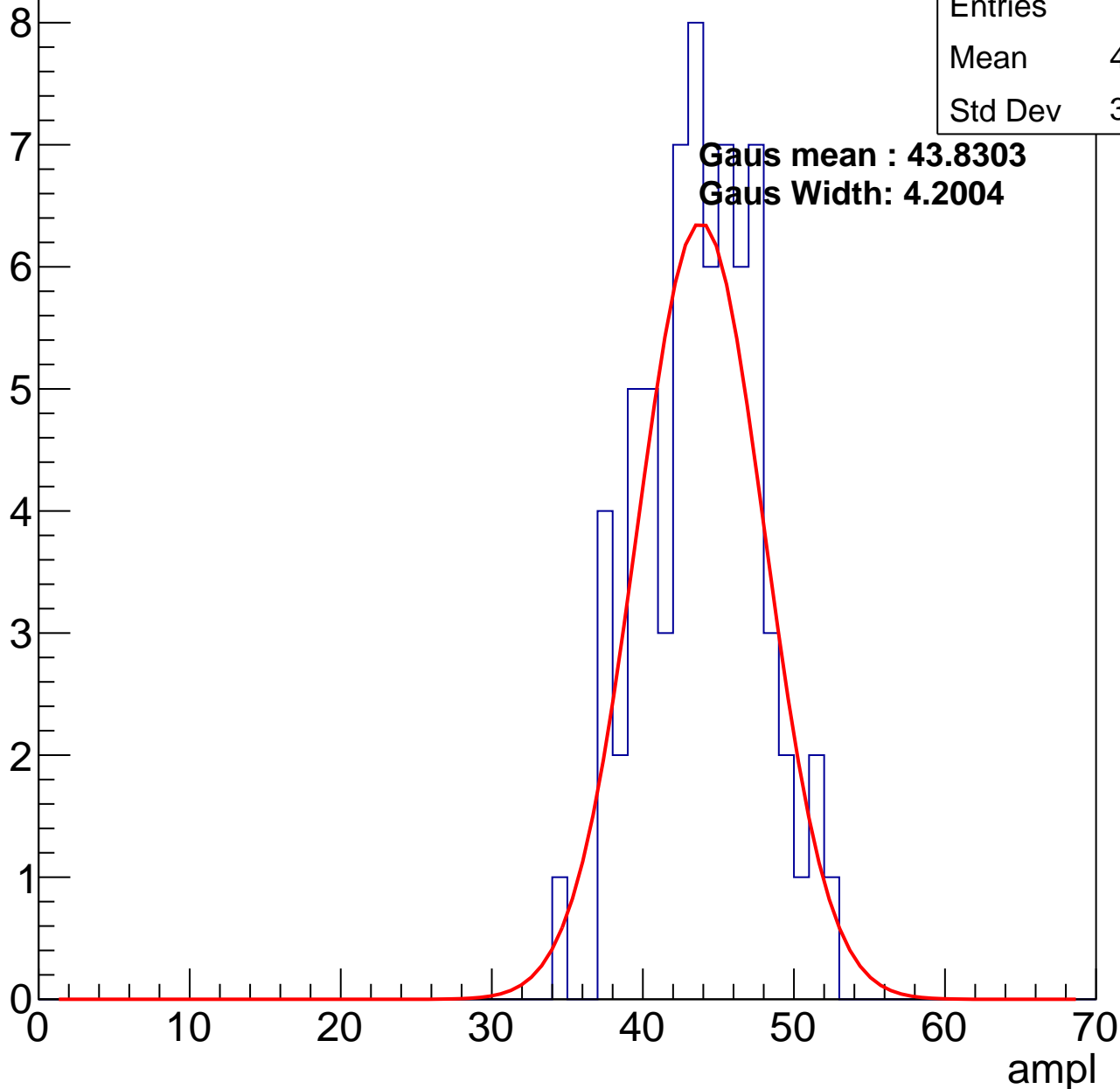
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	70
Mean	43.49
Std Dev	3.794

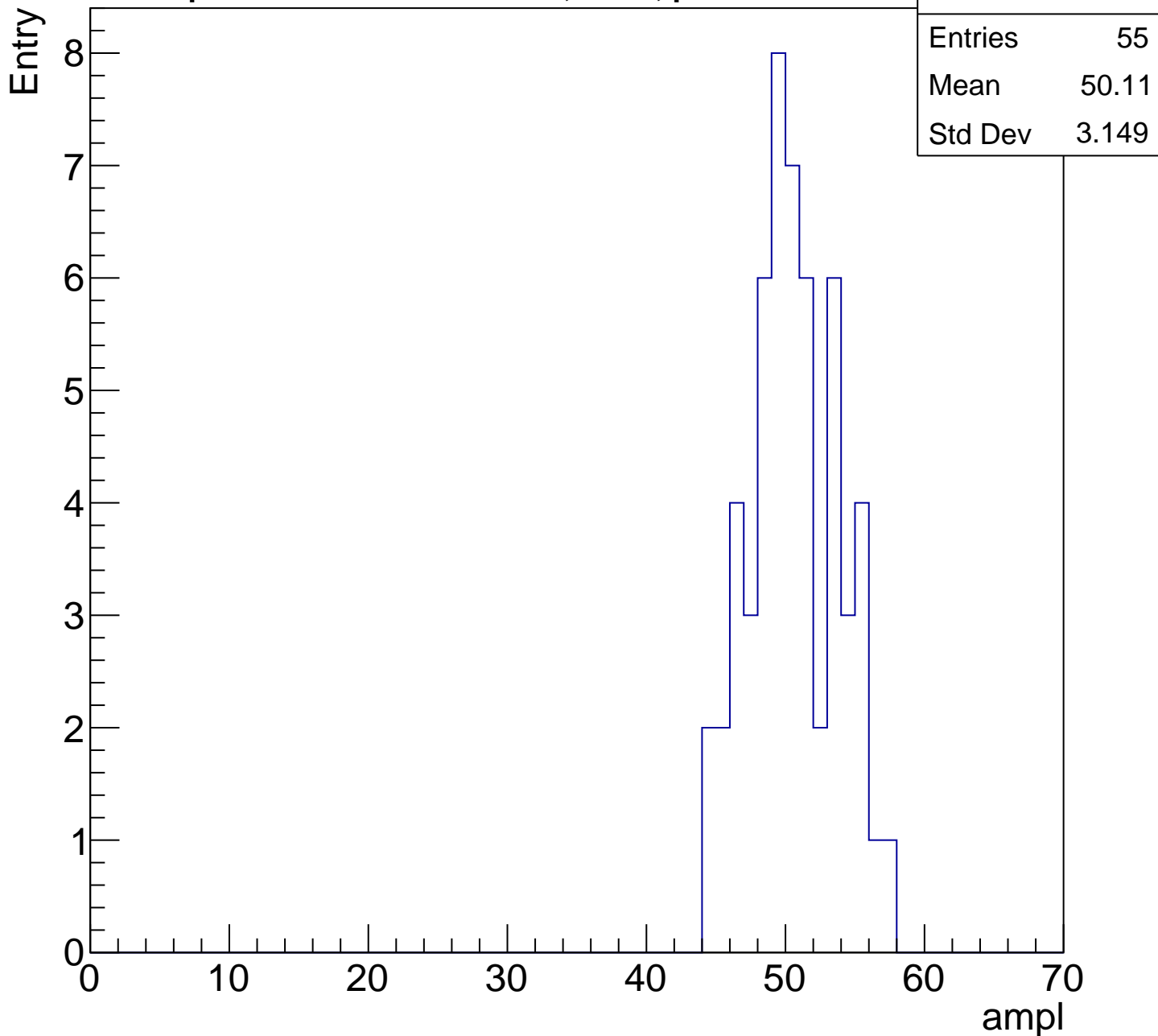
**Gaus mean : 43.8303**

**Gaus Width: 4.2004**



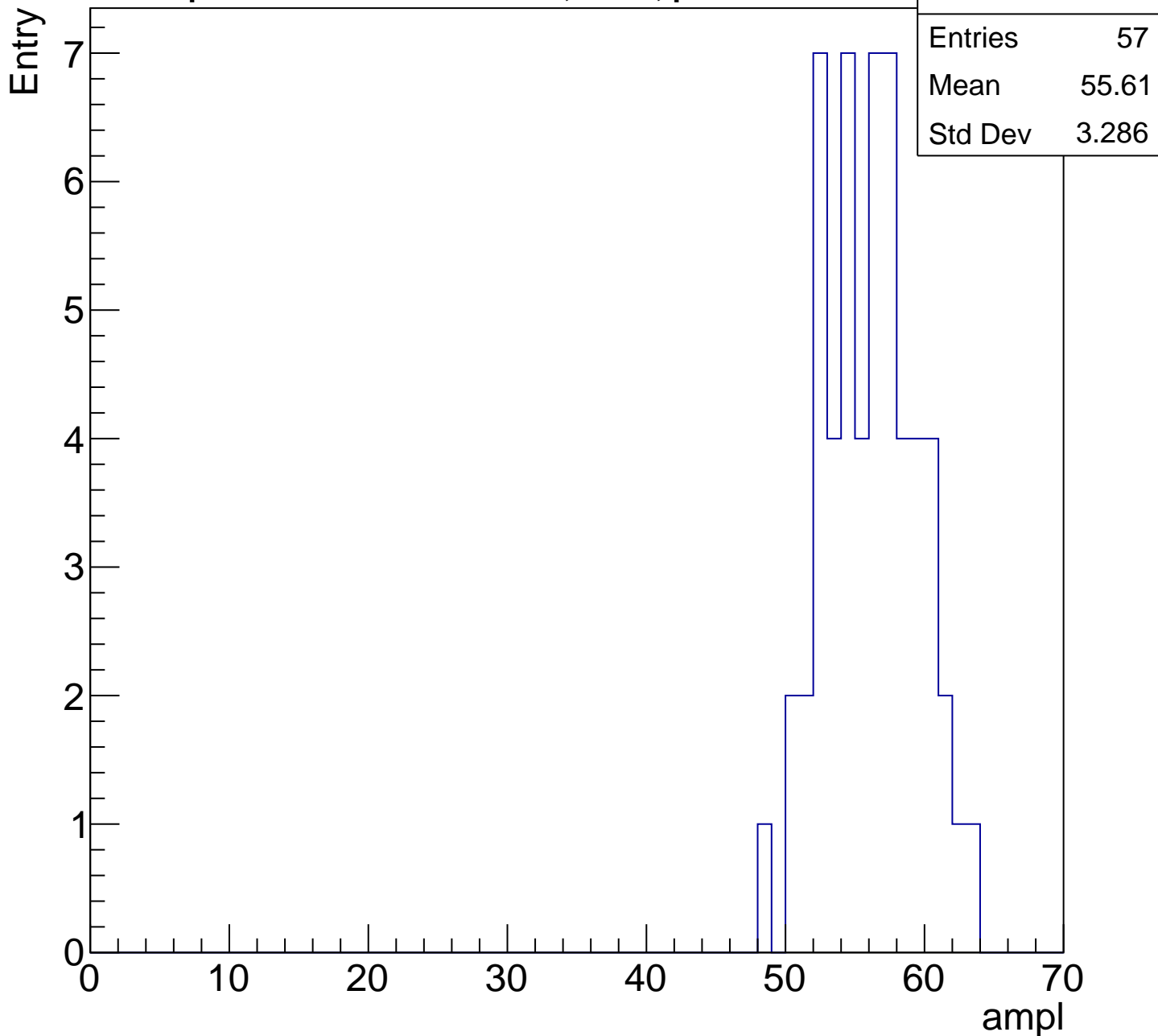
# B1L100S, U6-ch69, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2



# B1L100S, U6-ch69, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2



# B1L100S, U6-ch69, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

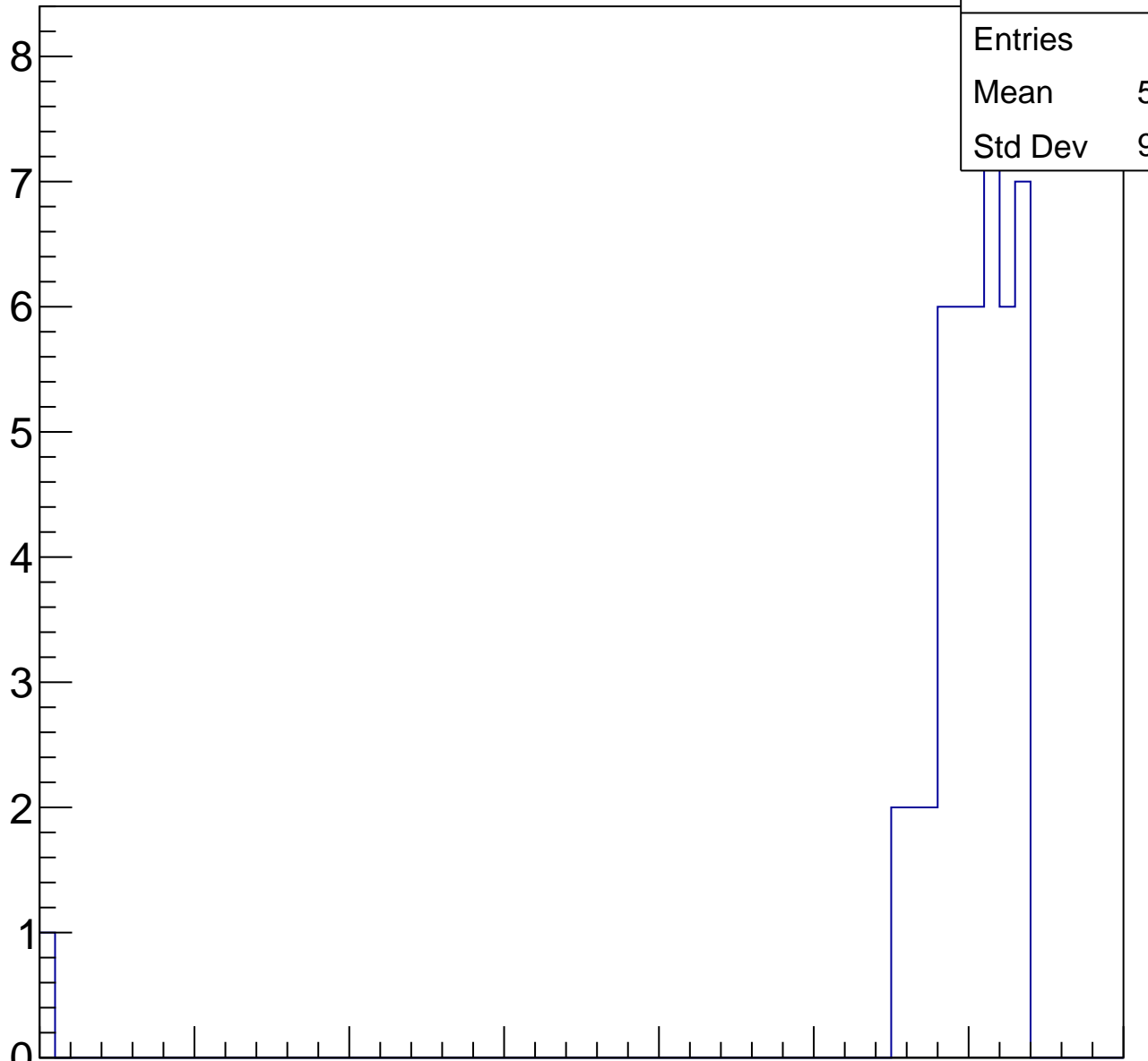
Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	46
Mean	58.67
Std Dev	9.022

ampl

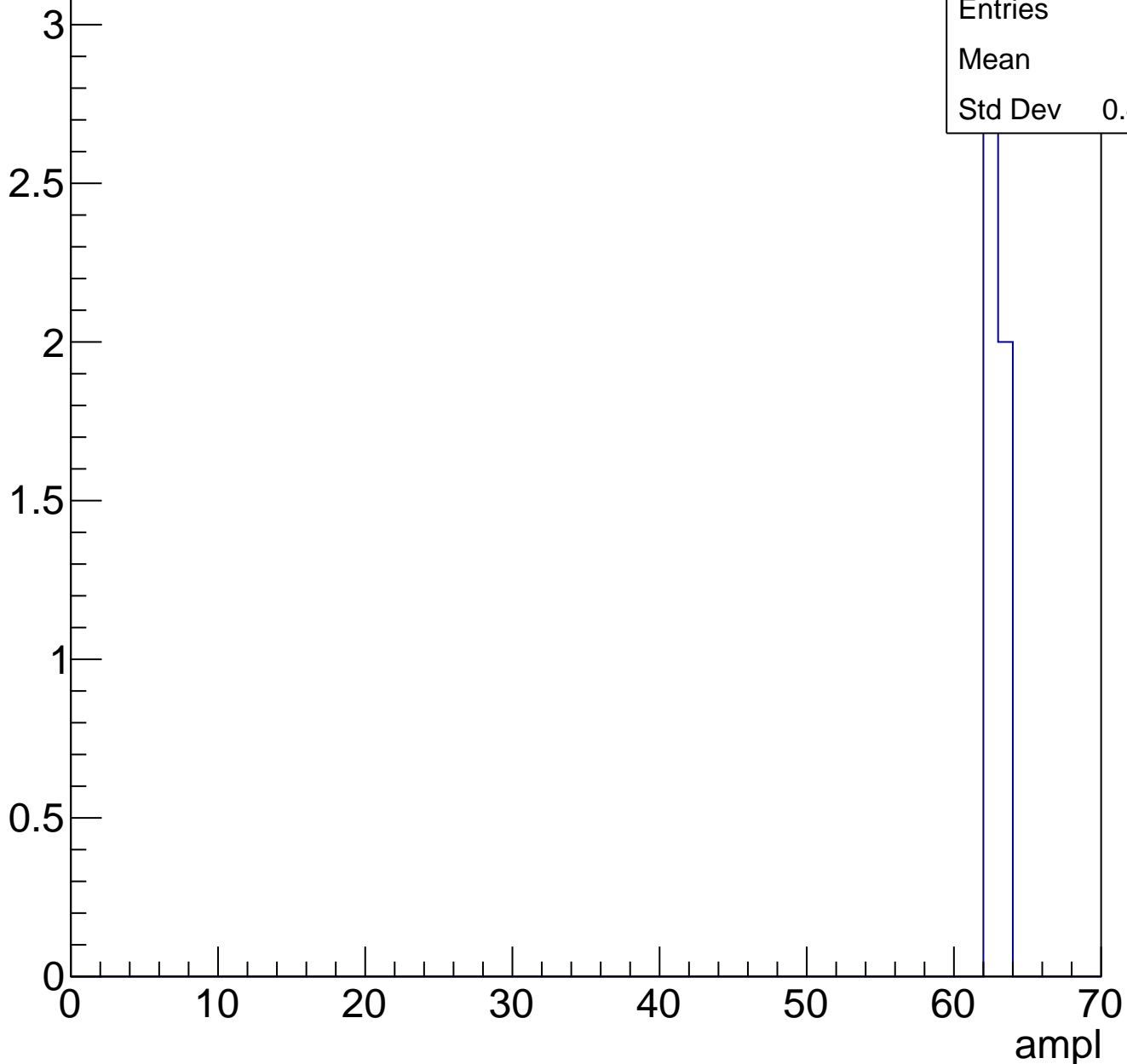
0 10 20 30 40 50 60 70



# B1L100S, U6-ch69, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry





# B1L100S, U6-ch69, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L100S, U6-ch70, adc0

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	64
Mean	31.06
Std Dev	3.517

**Gaus mean : 31.3593**

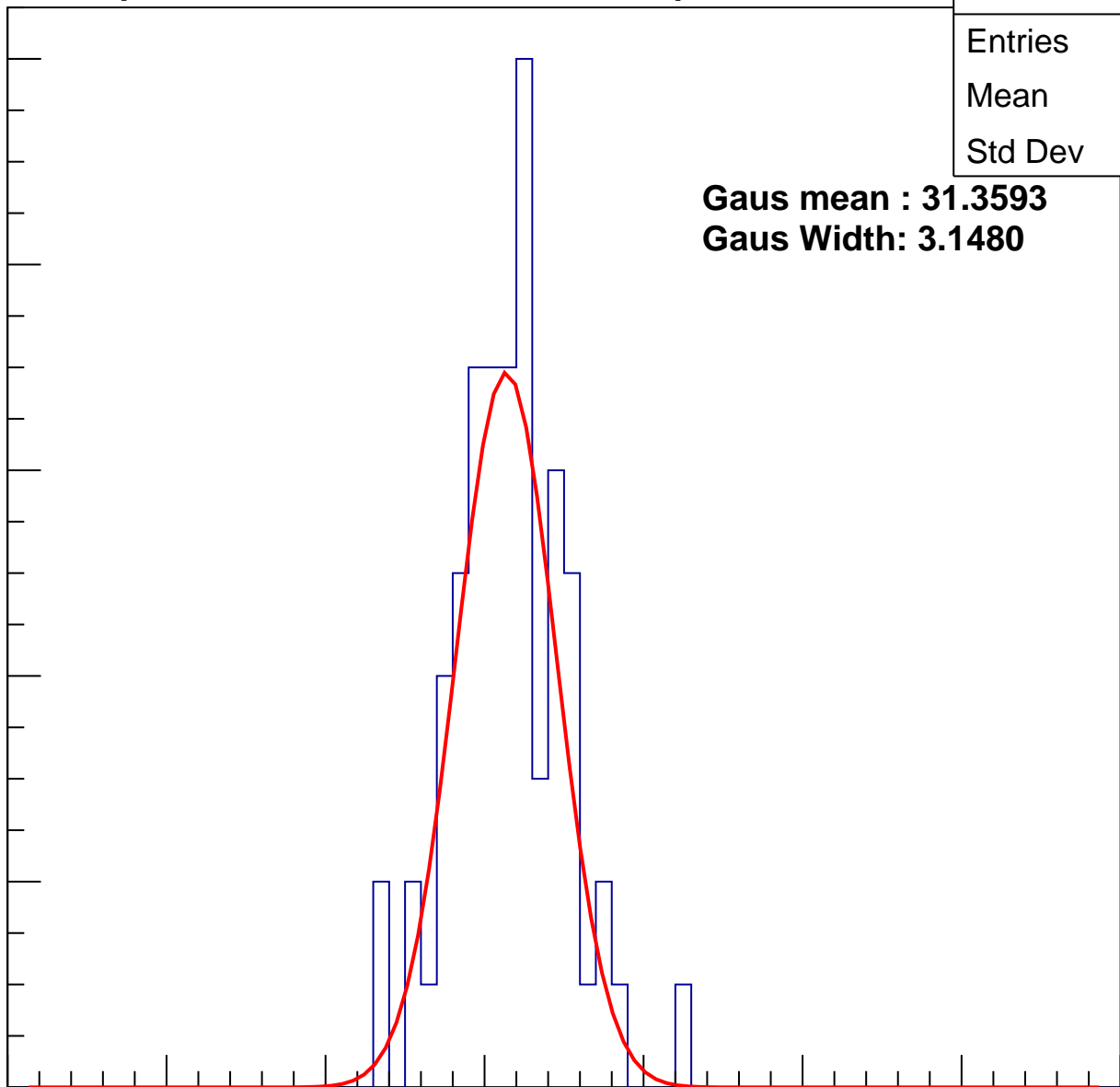
**Gaus Width: 3.1480**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L100S, U6-ch70, adc1

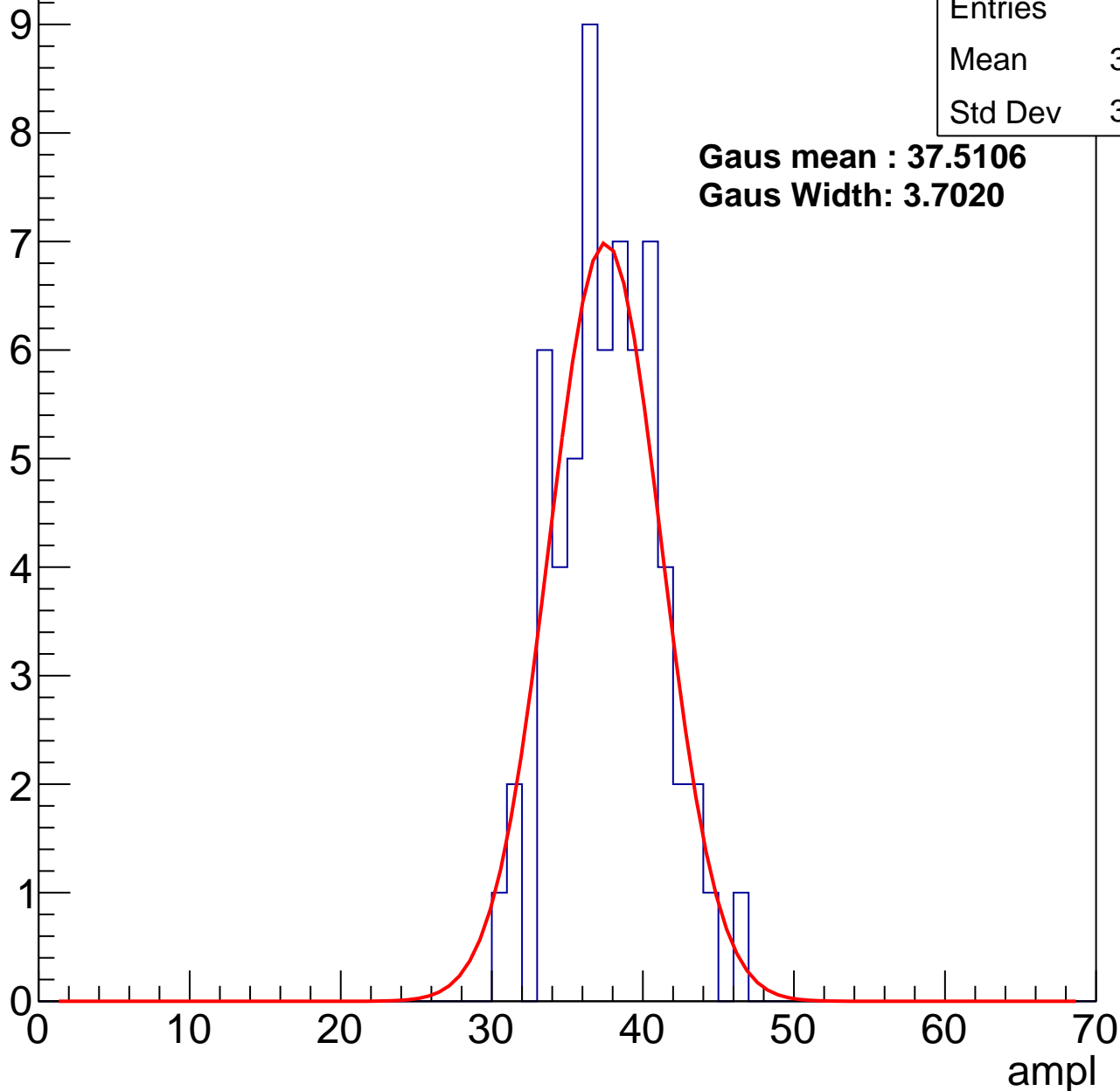
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	63
Mean	37.32
Std Dev	3.299

**Gaus mean : 37.5106**

**Gaus Width: 3.7020**



# B1L100S, U6-ch70, adc2

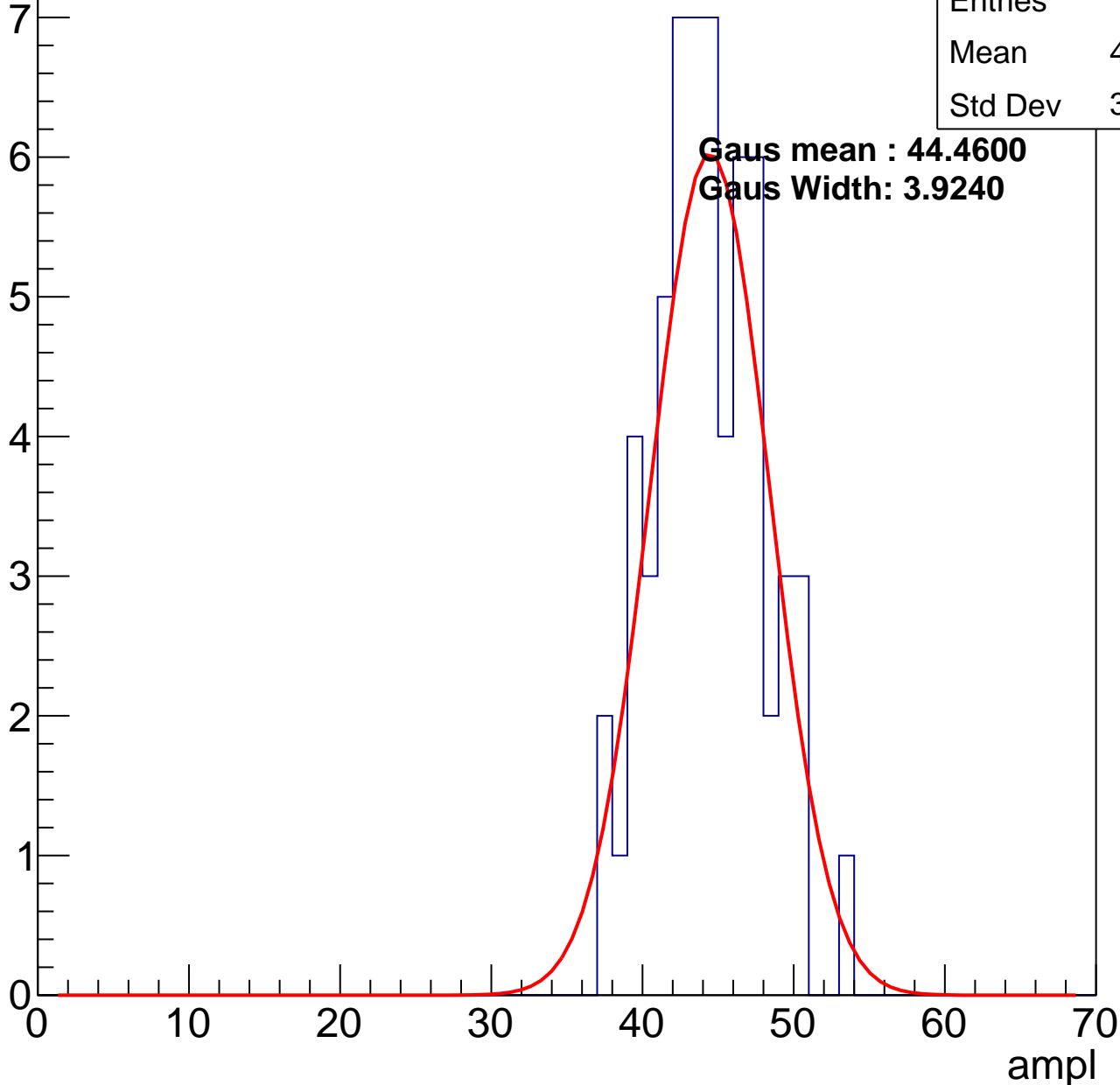
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	61
Mean	43.93
Std Dev	3.482

**Gaus mean : 44.4600**

**Gaus Width: 3.9240**

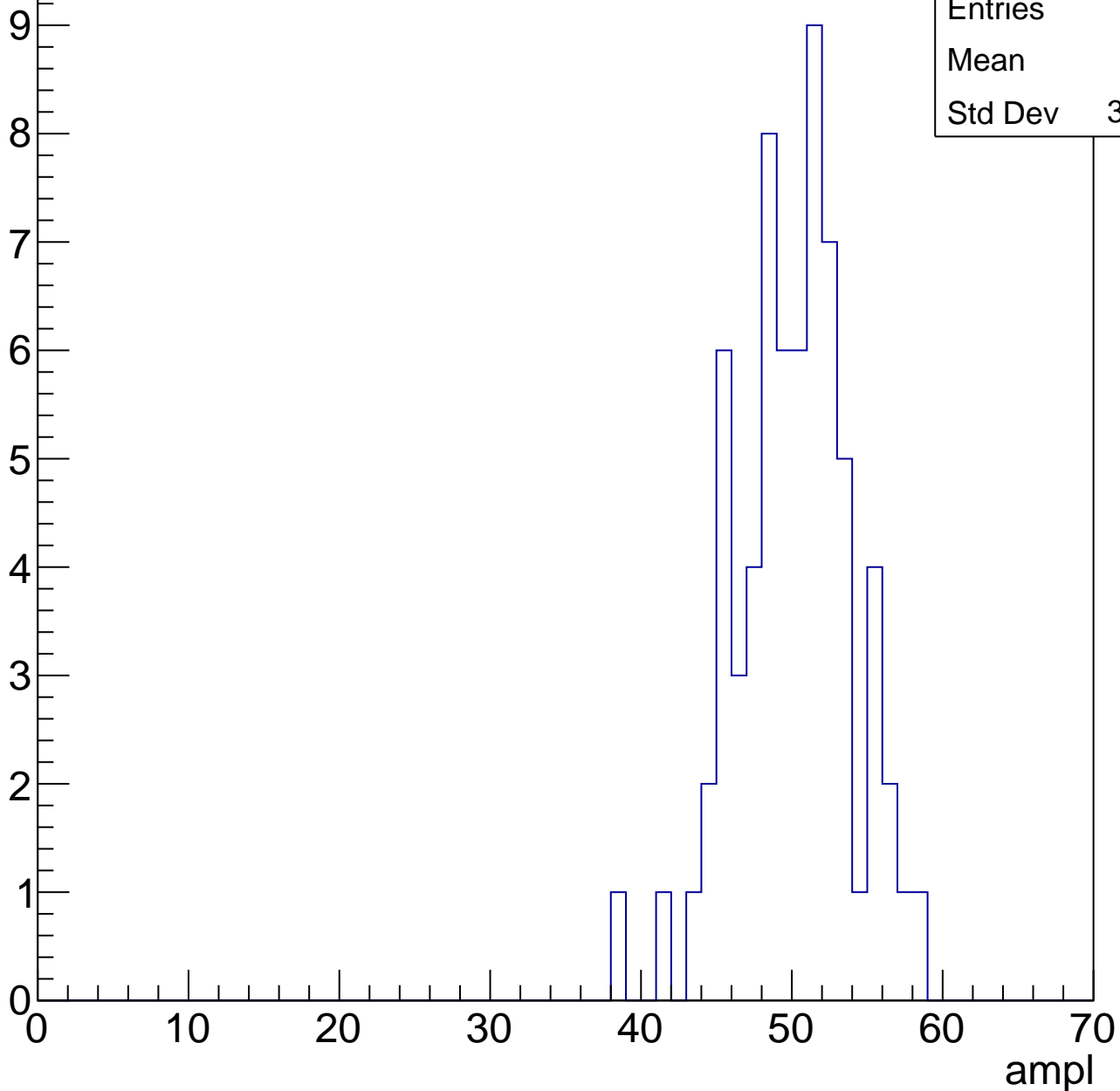


# B1L100S, U6-ch70, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	68
Mean	49.6
Std Dev	3.816

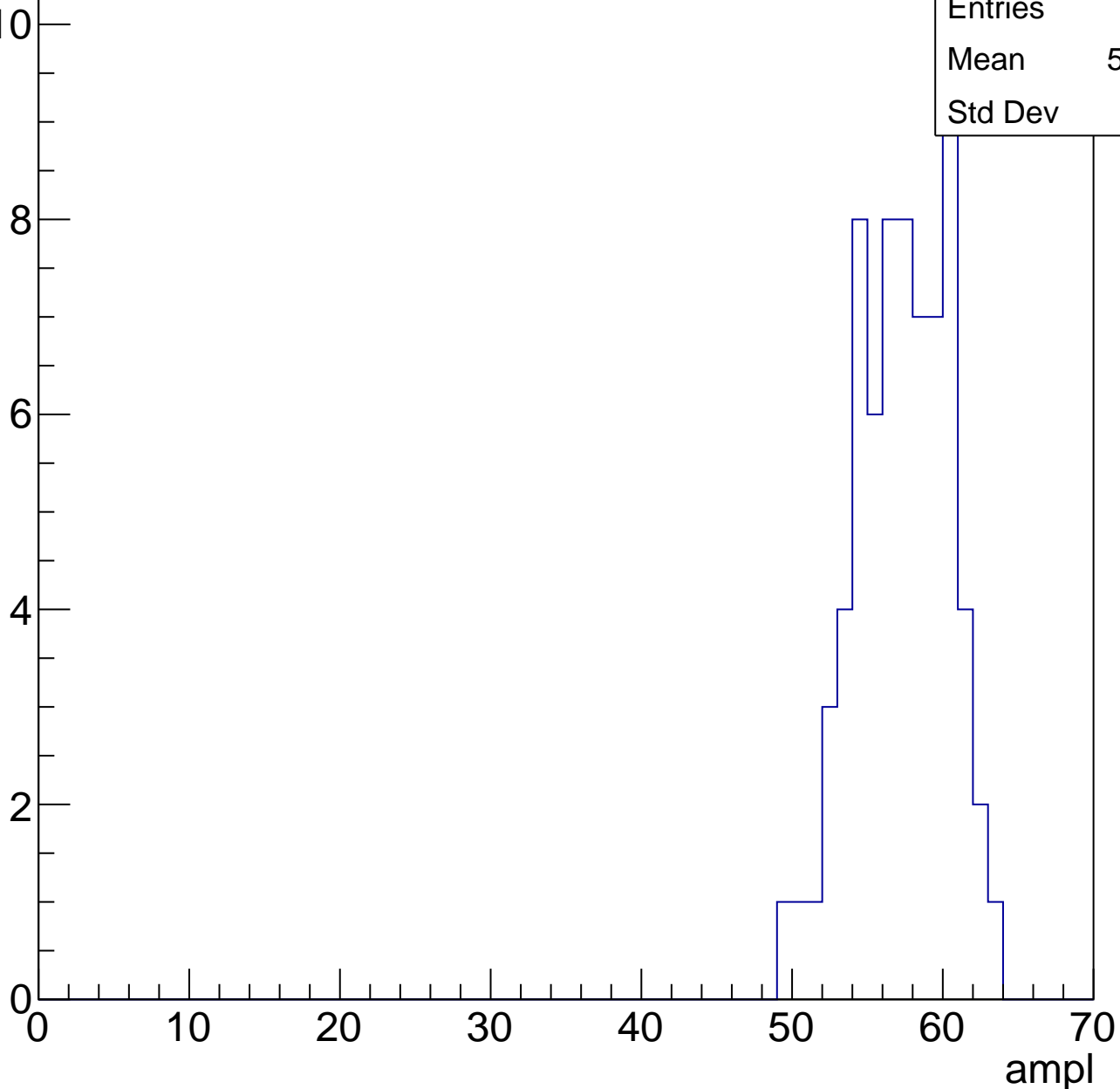


# B1L100S, U6-ch70, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	71
Mean	56.82
Std Dev	3.06

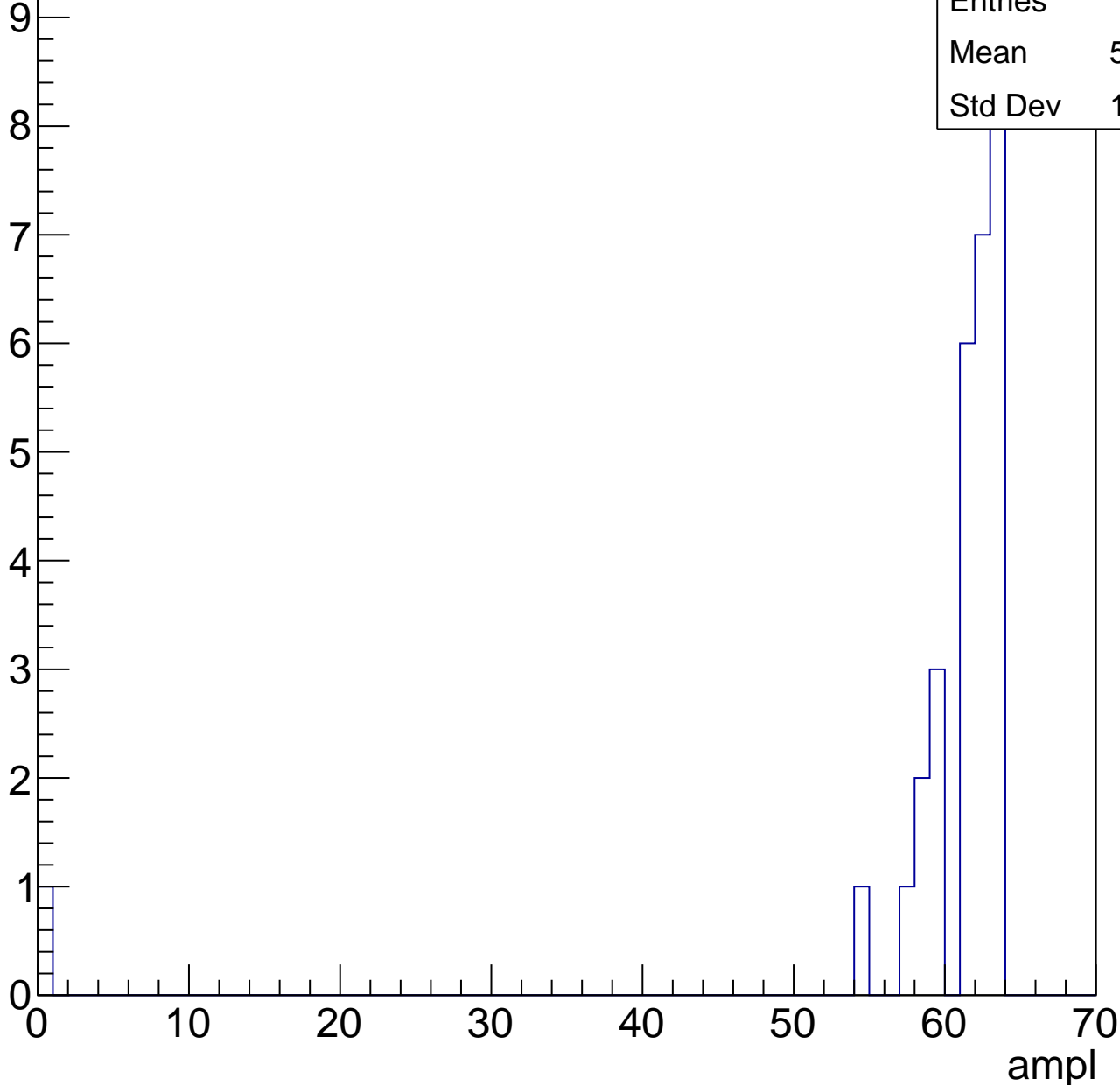


# B1L100S, U6-ch70, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	30
Mean	59.03
Std Dev	11.17



# B1L100S, U6-ch70, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry





# B1L100S, U6-ch70, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L100S, U6-ch71, adc0

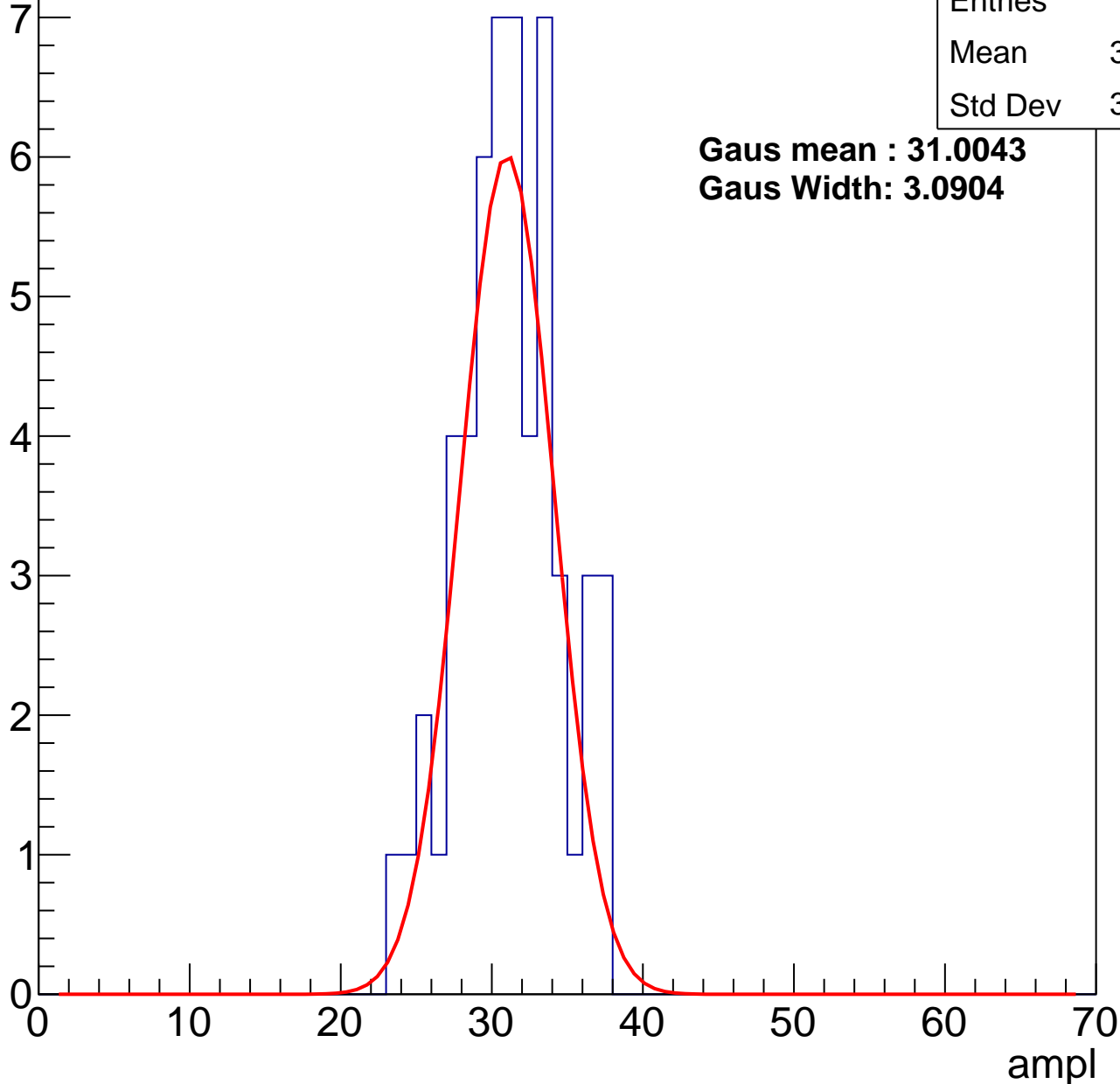
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	54
Mean	30.72
Std Dev	3.319

**Gaus mean : 31.0043**

**Gaus Width: 3.0904**



# B1L100S, U6-ch71, adc1

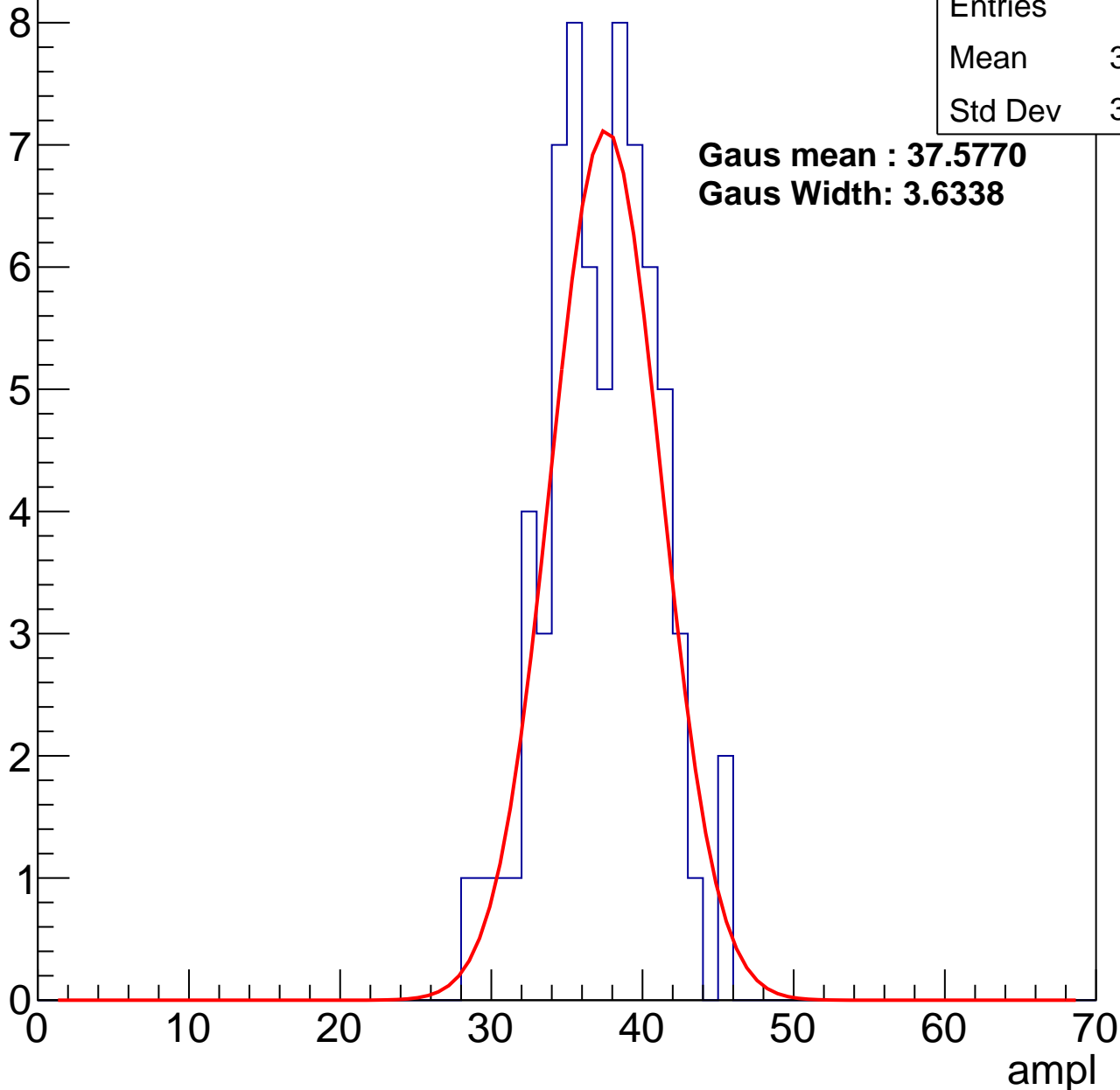
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	69
Mean	36.88
Std Dev	3.586

**Gaus mean : 37.5770**

**Gaus Width: 3.6338**



# B1L100S, U6-ch71, adc2

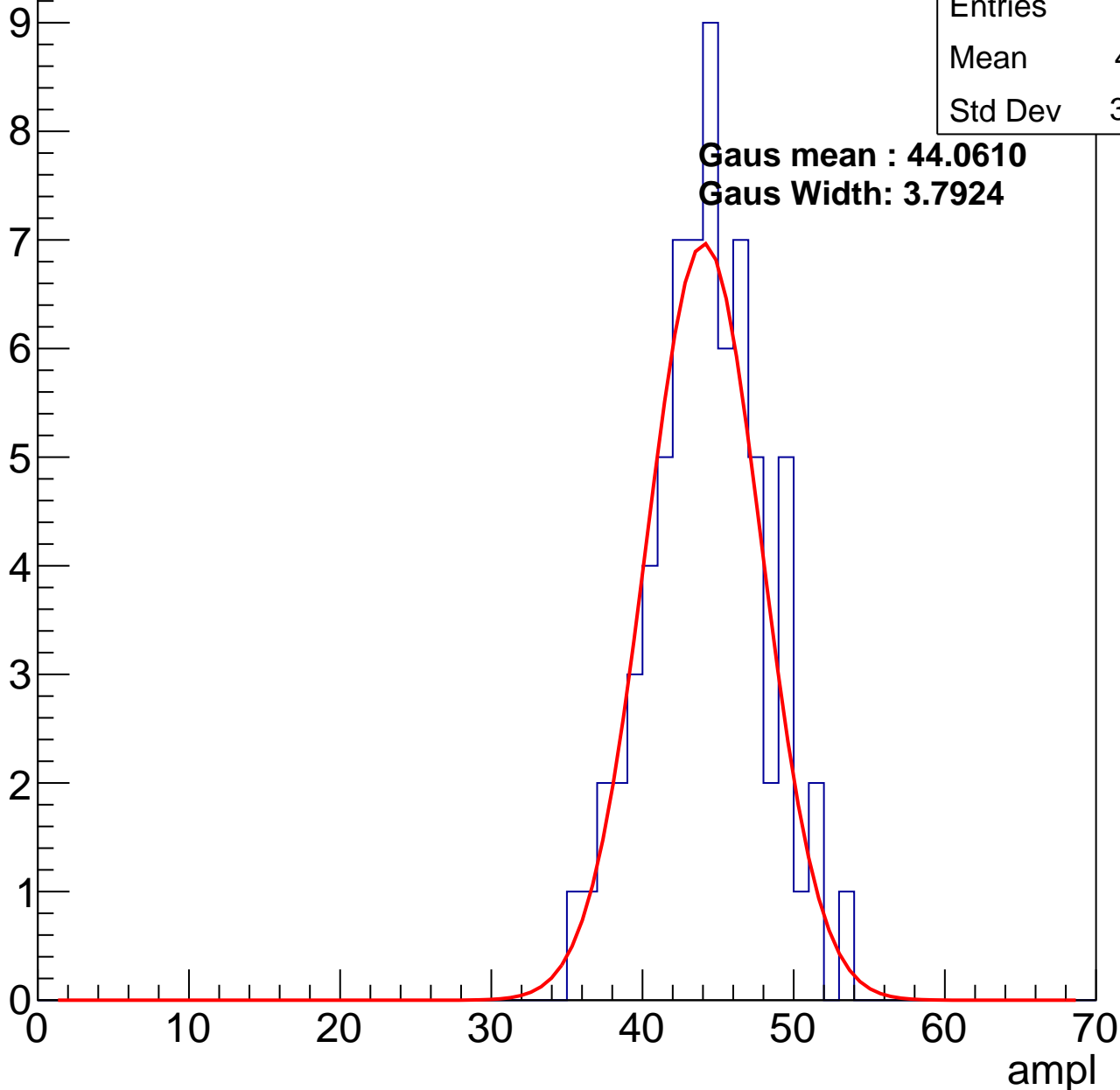
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	70
Mean	43.81
Std Dev	3.747

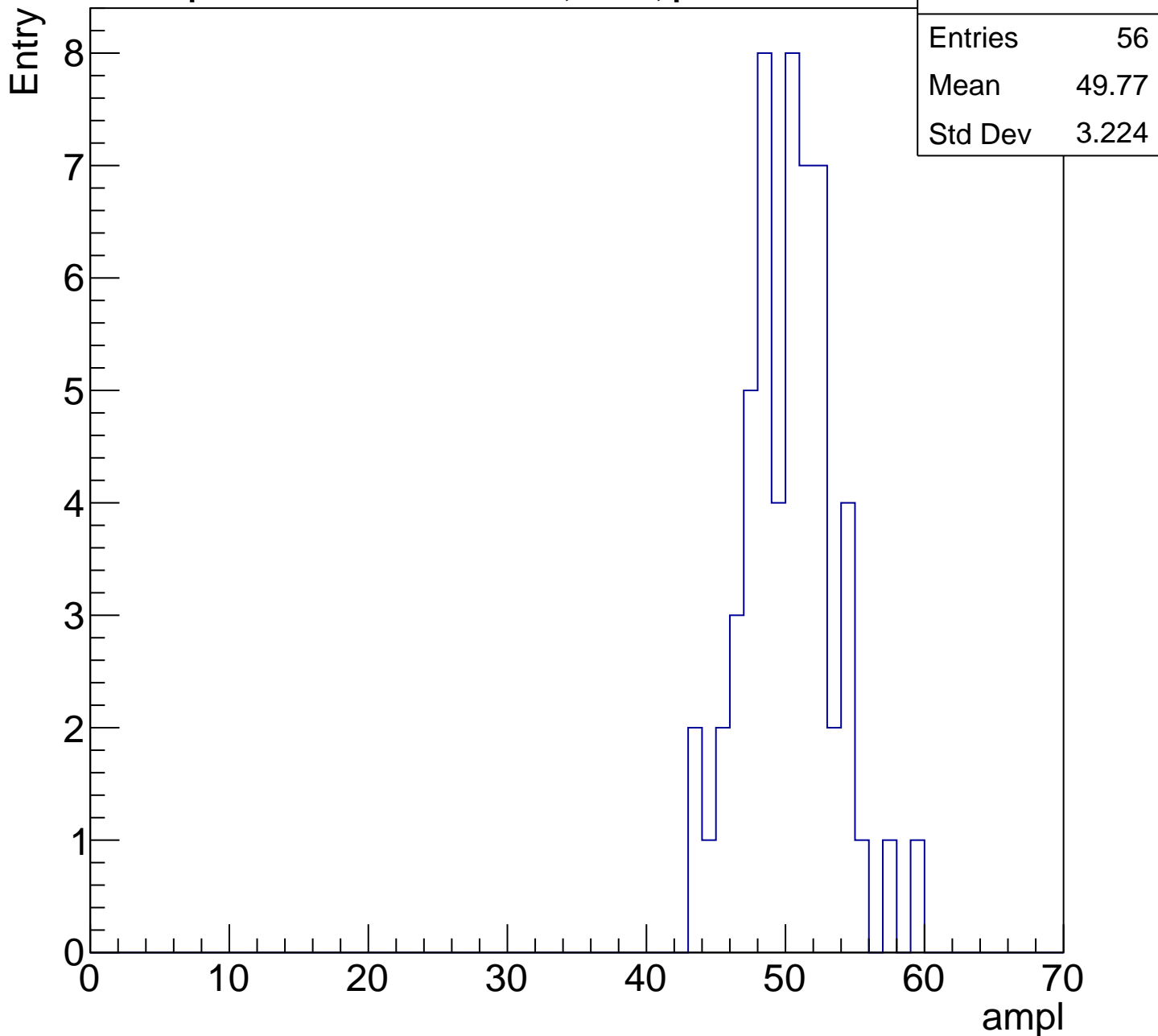
**Gaus mean : 44.0610**

**Gaus Width: 3.7924**



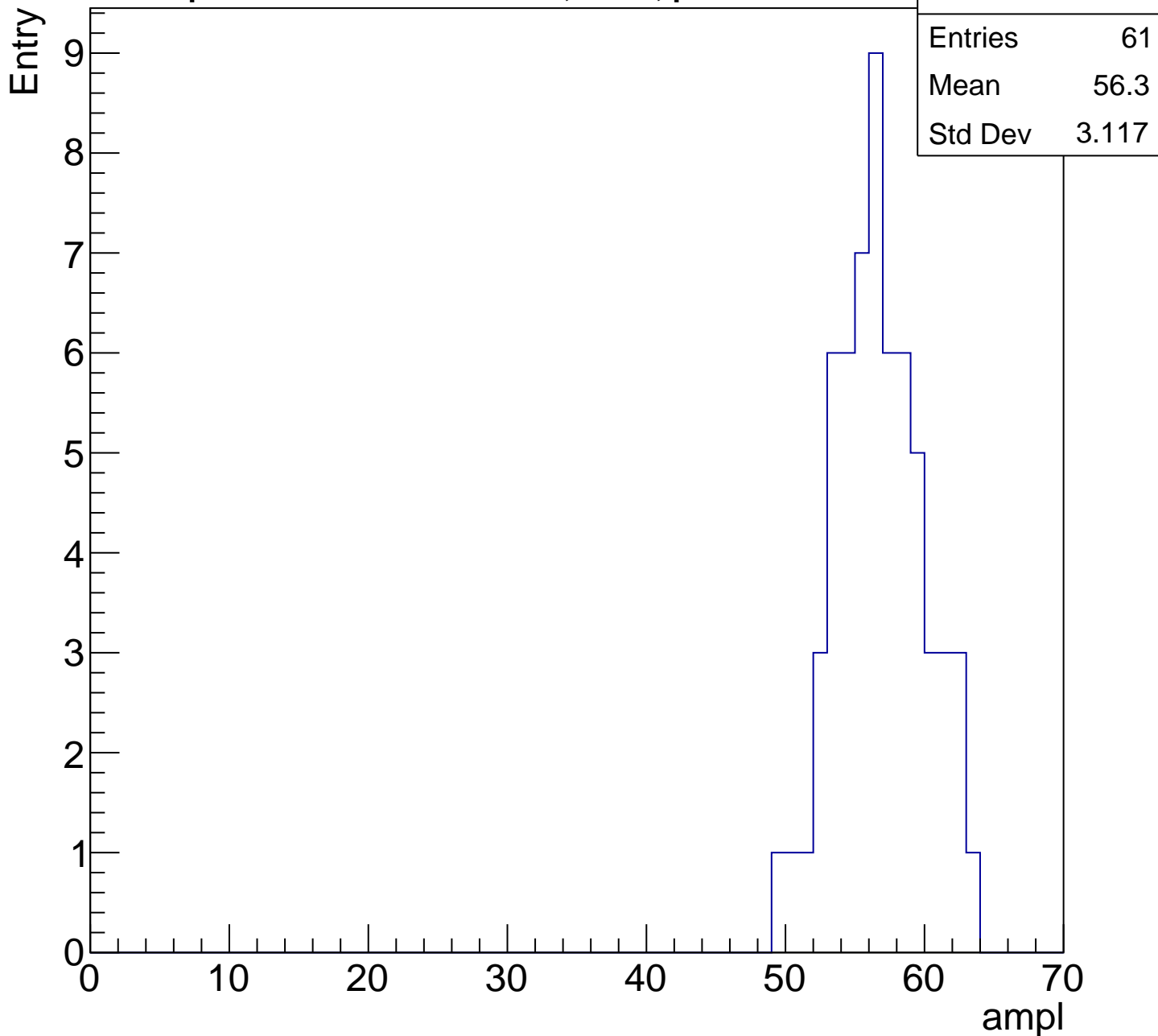
# B1L100S, U6-ch71, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2



# B1L100S, U6-ch71, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

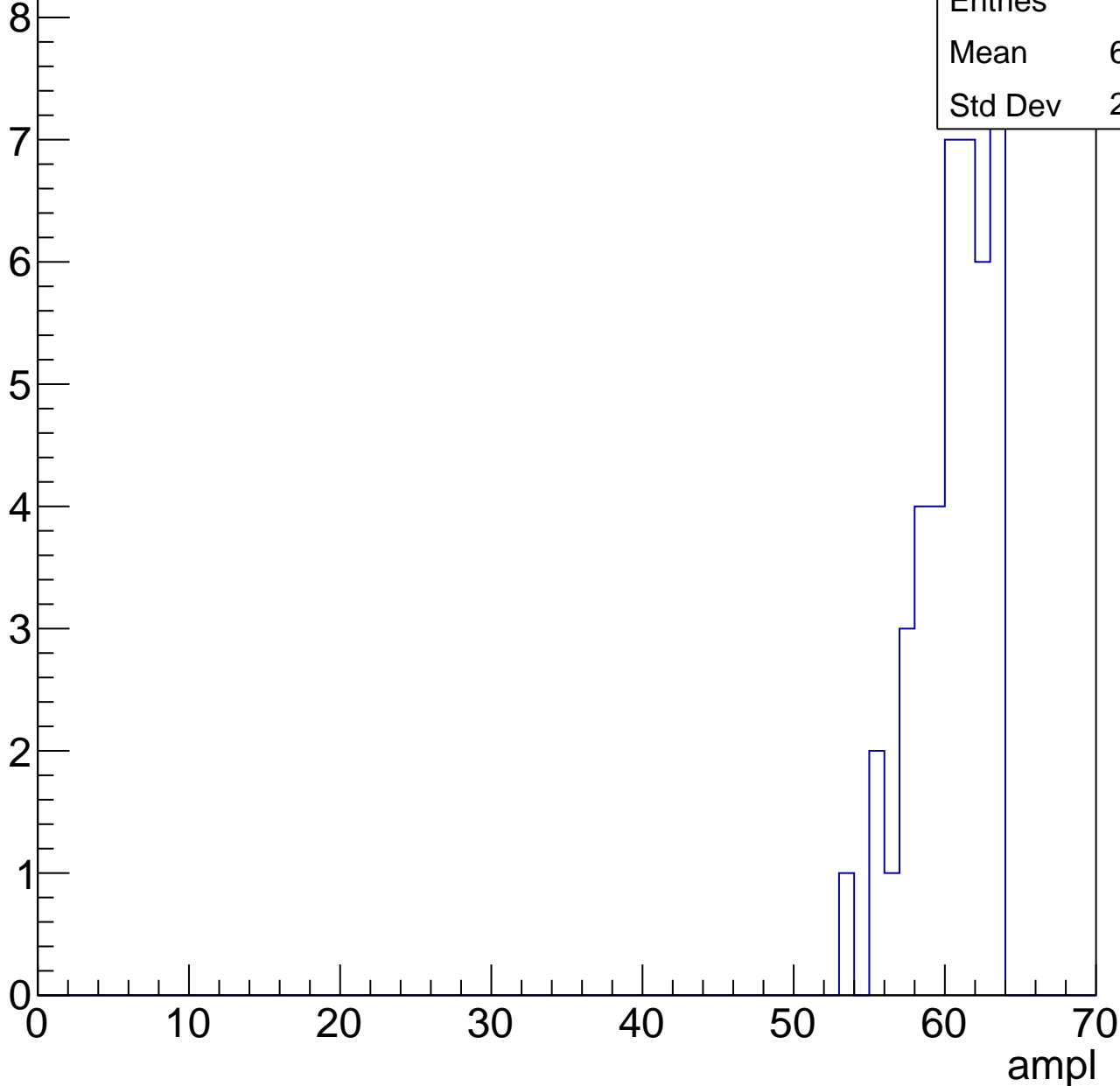


# B1L100S, U6-ch71, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

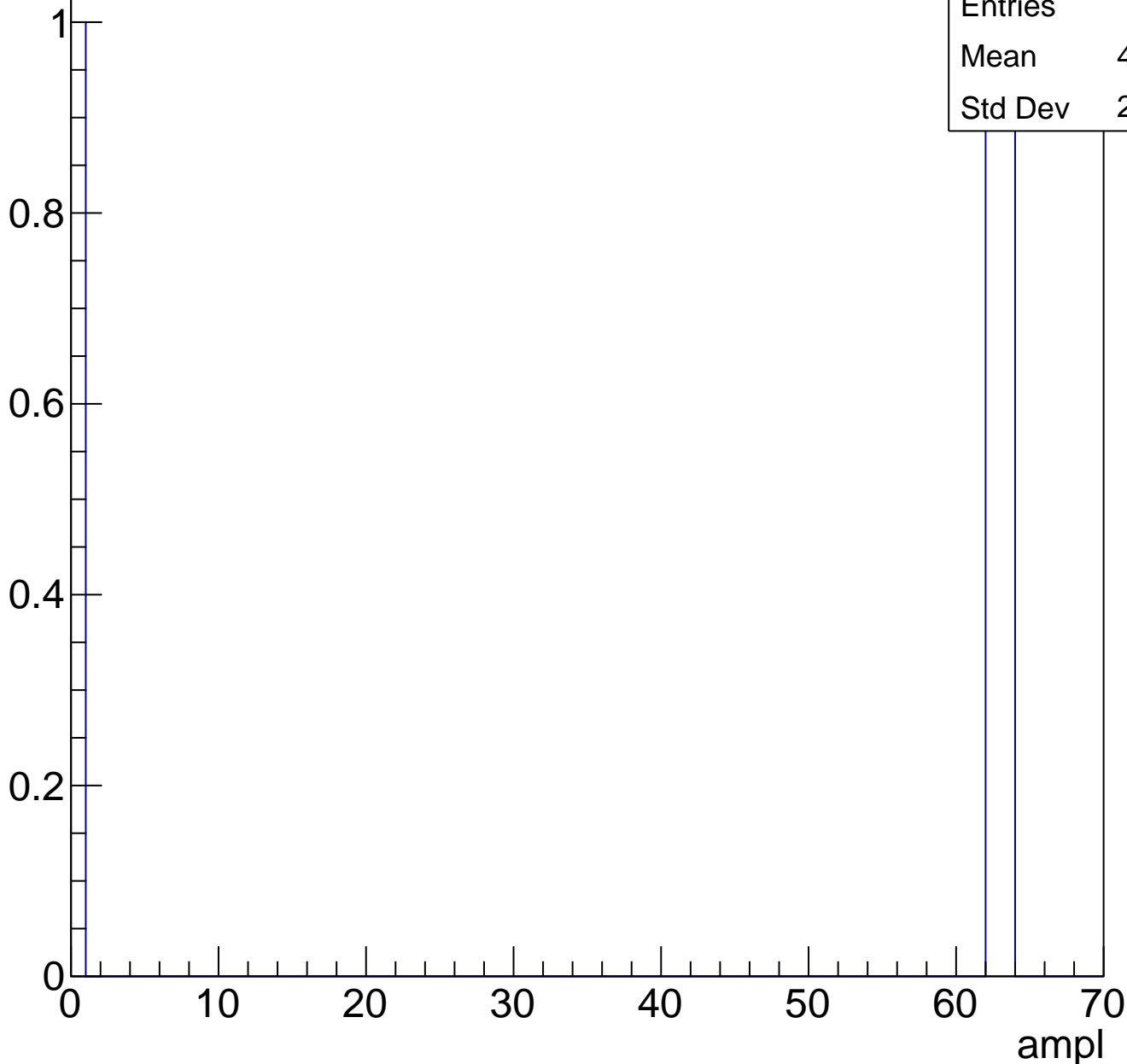
Entries	43
Mean	60.02
Std Dev	2.482



# B1L100S, U6-ch71, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry





# B1L100S, U6-ch71, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L100S, U6-ch72, adc0

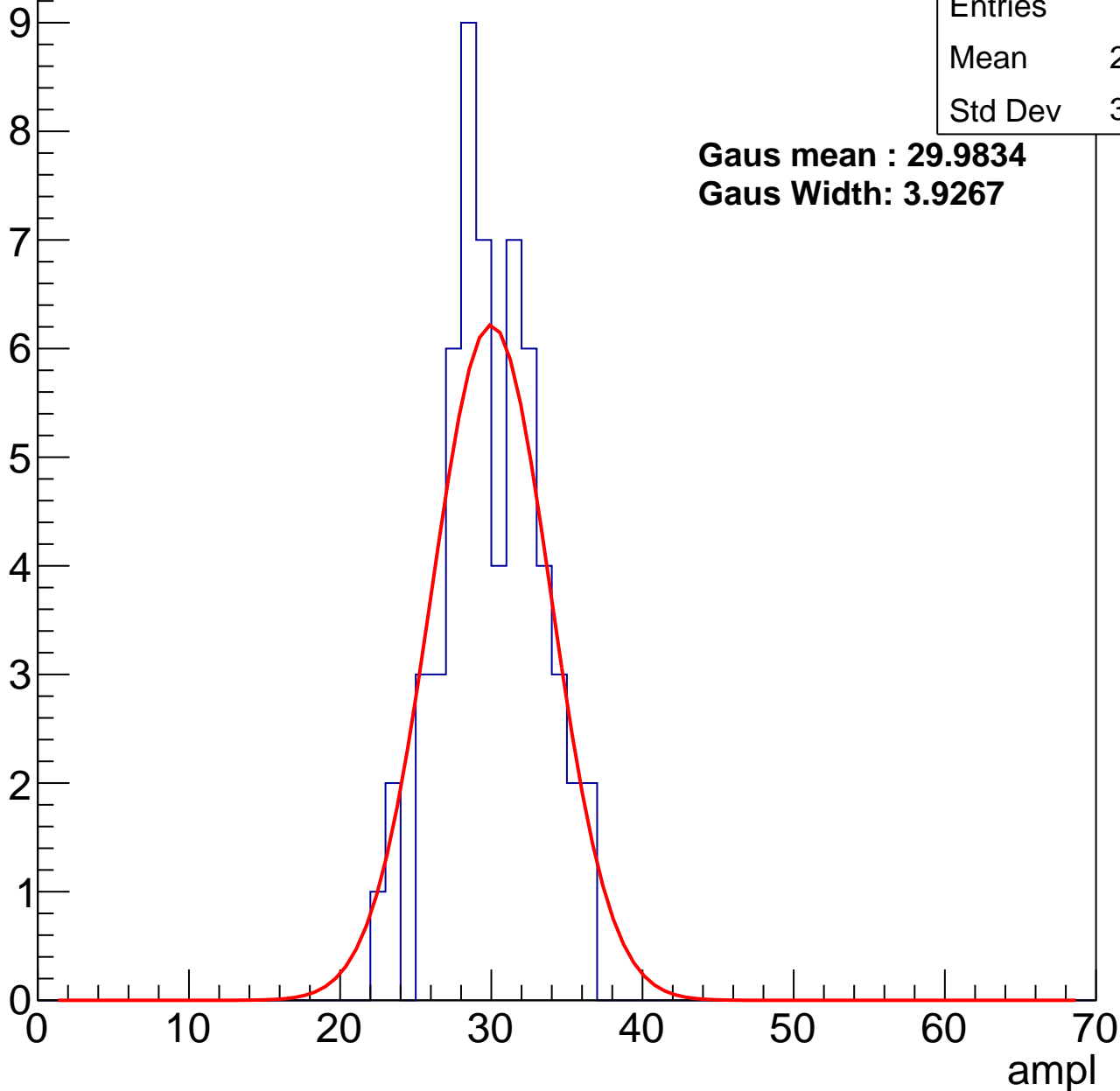
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	59
Mean	29.54
Std Dev	3.207

**Gaus mean : 29.9834**

**Gaus Width: 3.9267**



# B1L100S, U6-ch72, adc1

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	74
Mean	35.65
Std Dev	5.591

**Gaus mean : 36.4229**

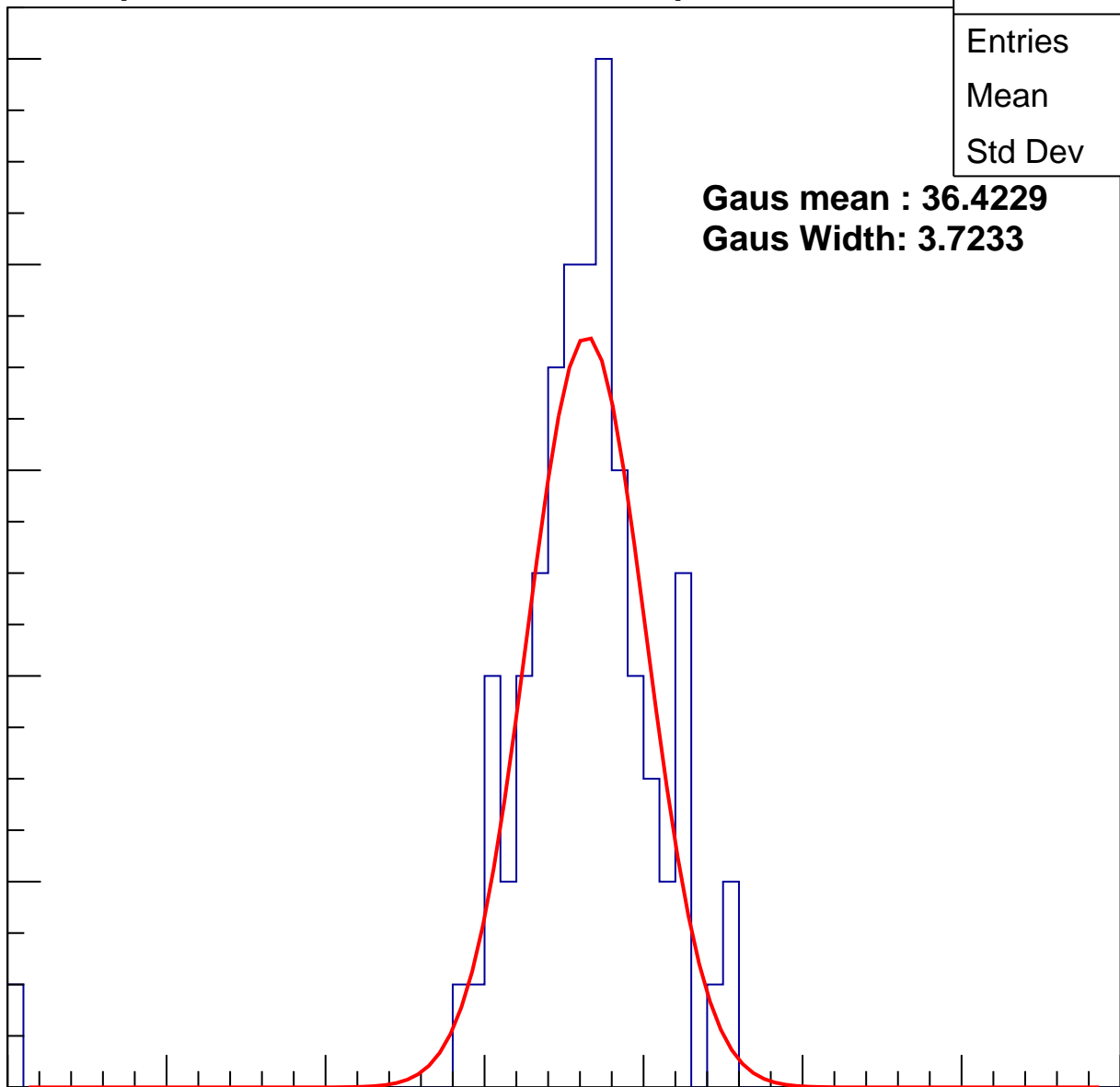
**Gaus Width: 3.7233**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L100S, U6-ch72, adc2

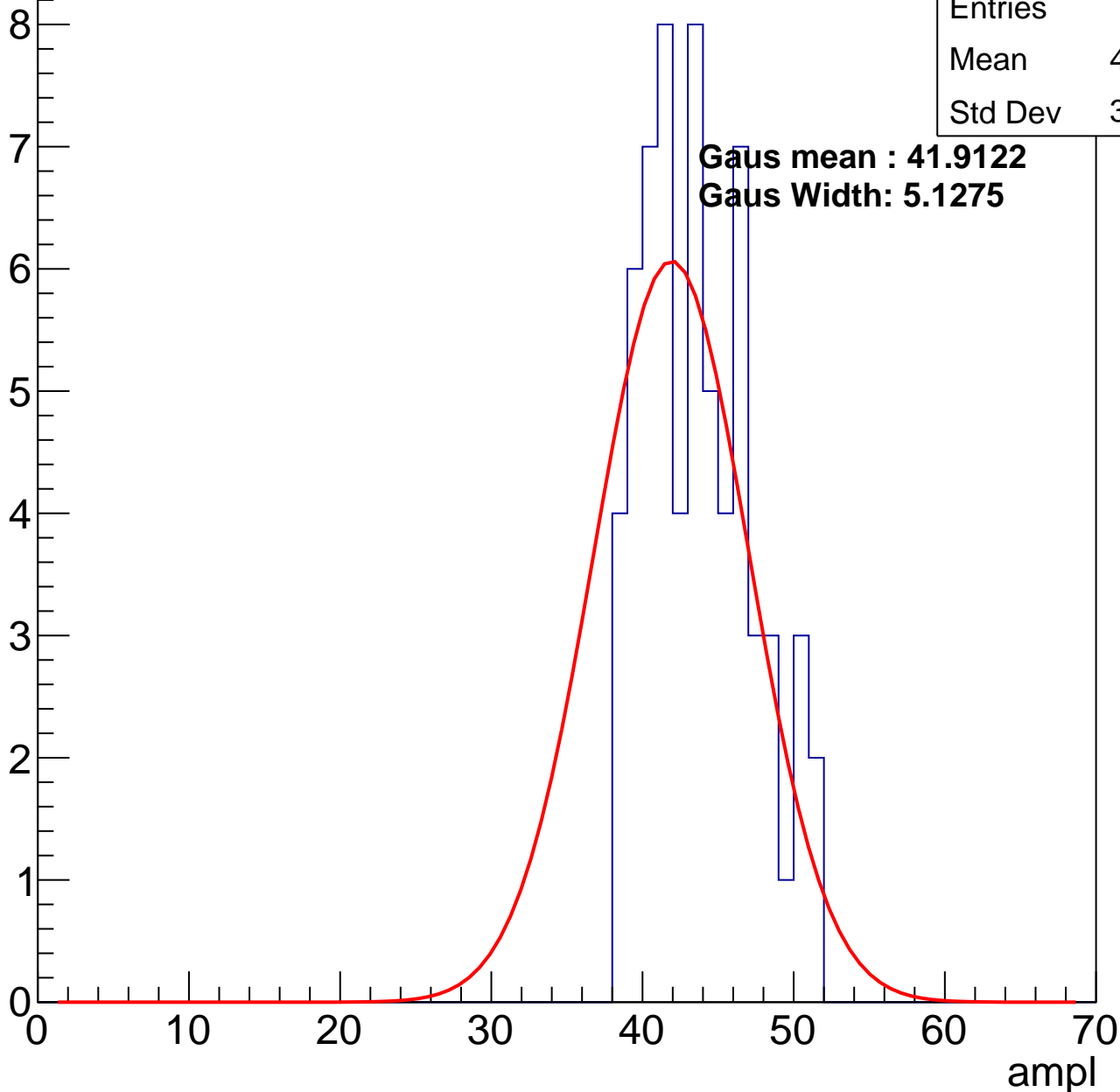
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	65
Mean	43.29
Std Dev	3.525

**Gaus mean : 41.9122**

**Gaus Width: 5.1275**

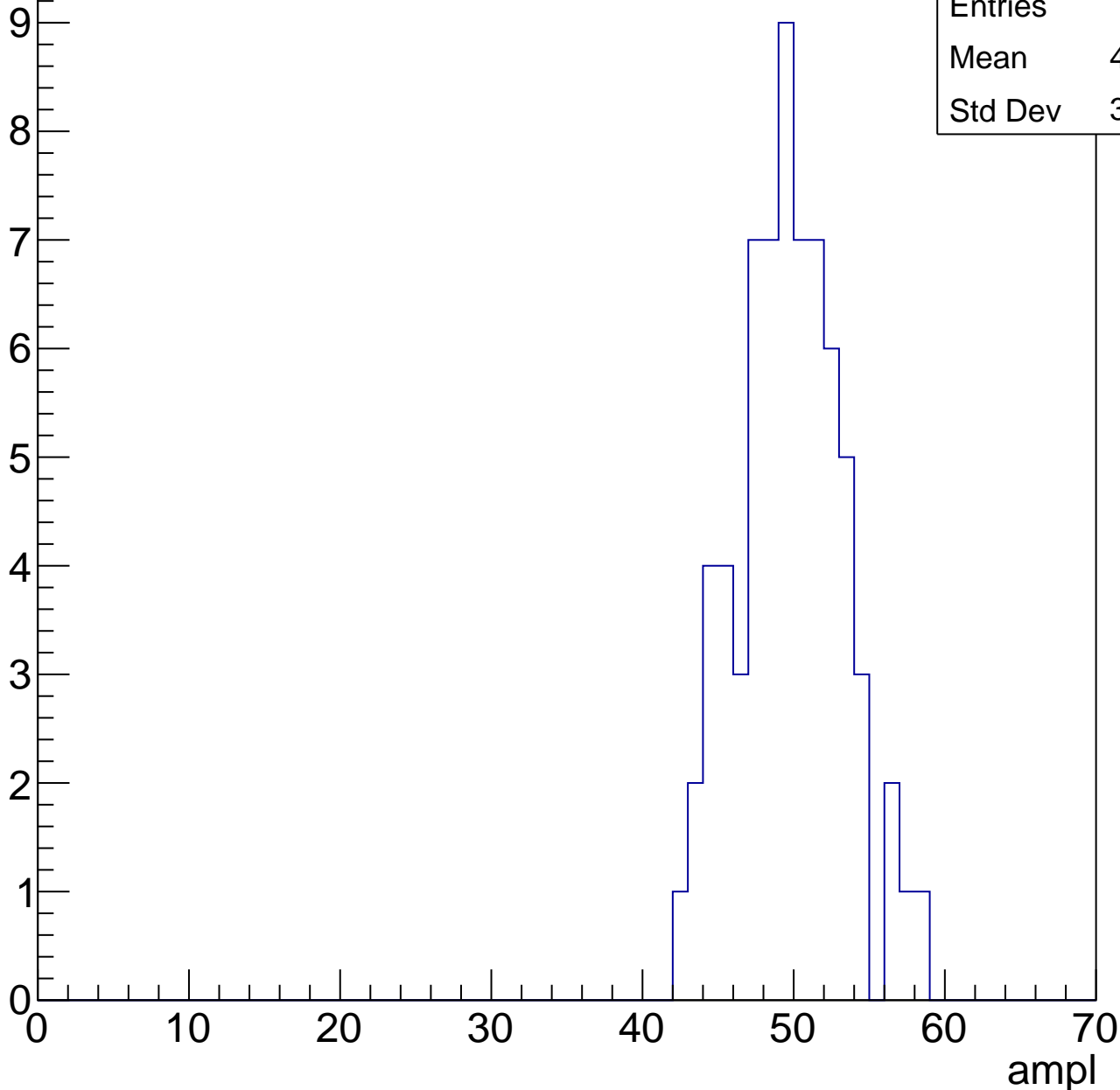


# B1L100S, U6-ch72, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	69
Mean	49.29
Std Dev	3.465



# B1L100S, U6-ch72, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

10

8

6

4

2

0

0

10

20

30

40

50

60

ampl

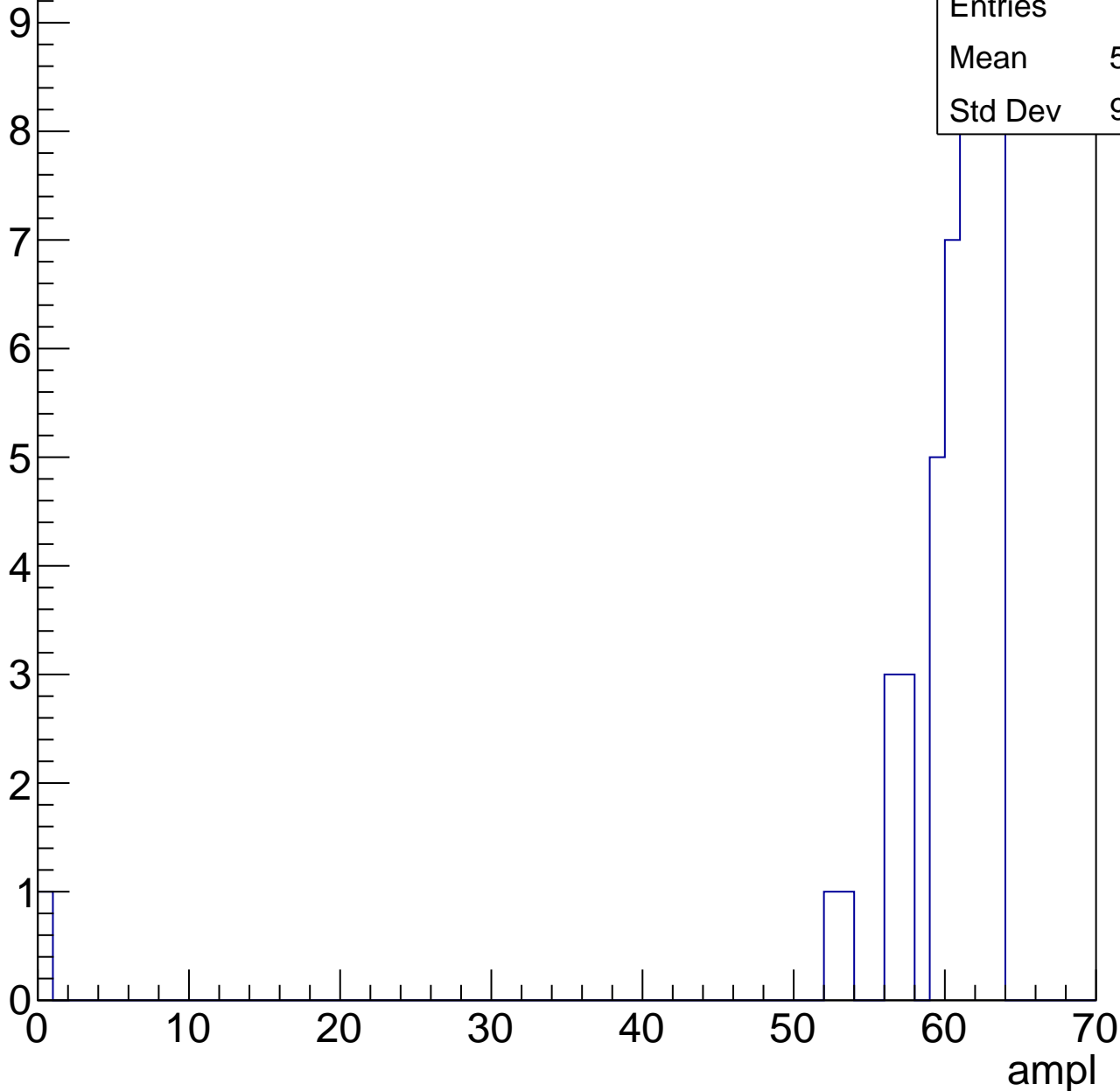
Entries	55
Mean	56.16
Std Dev	2.492

# B1L100S, U6-ch72, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	46
Mean	58.87
Std Dev	9.145



# B1L100S, U6-ch72, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry





# B1L100S, U6-ch72, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L100S, U6-ch73, adc0

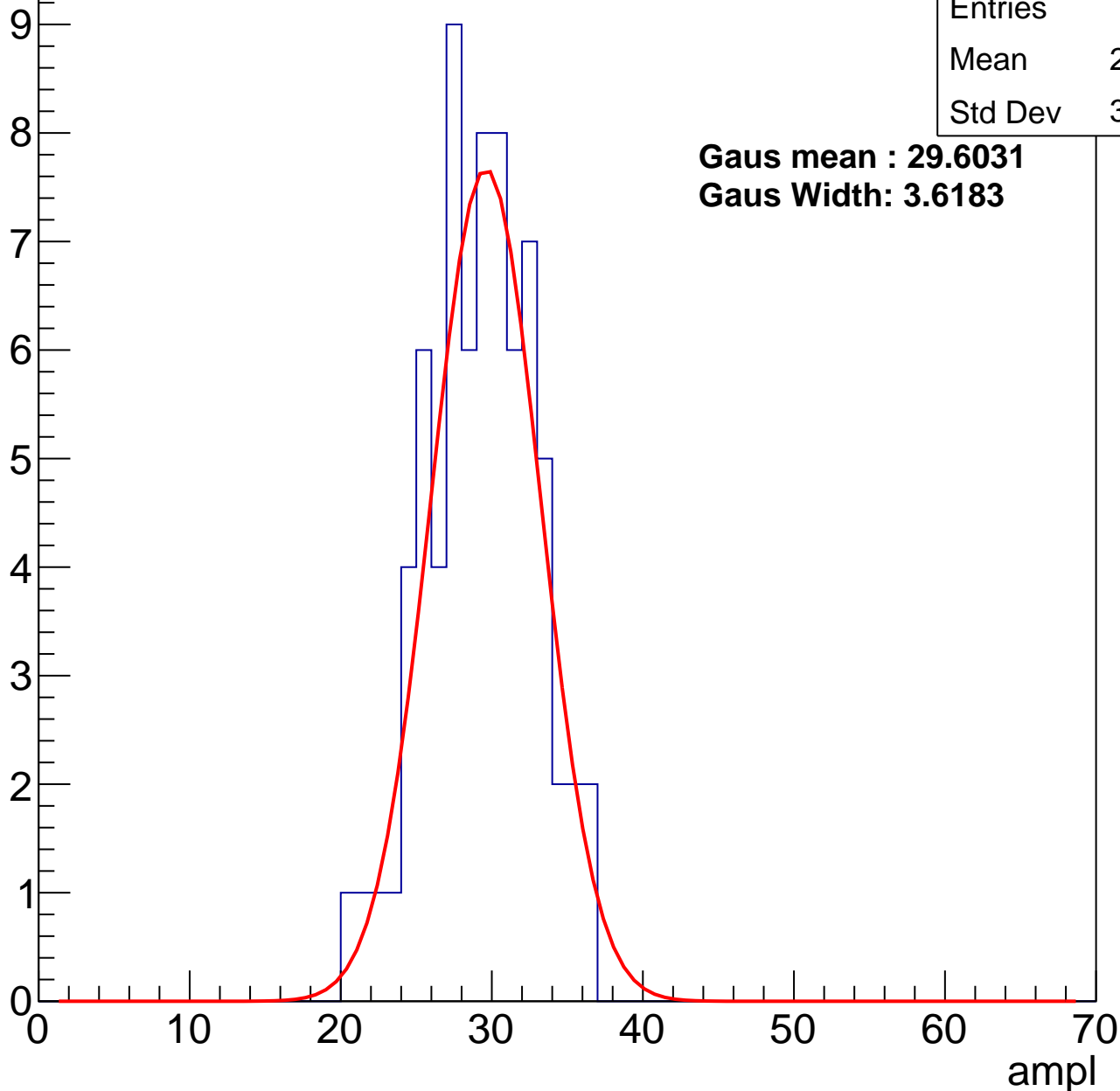
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	73
Mean	28.82
Std Dev	3.505

**Gaus mean : 29.6031**

**Gaus Width: 3.6183**



# B1L100S, U6-ch73, adc1

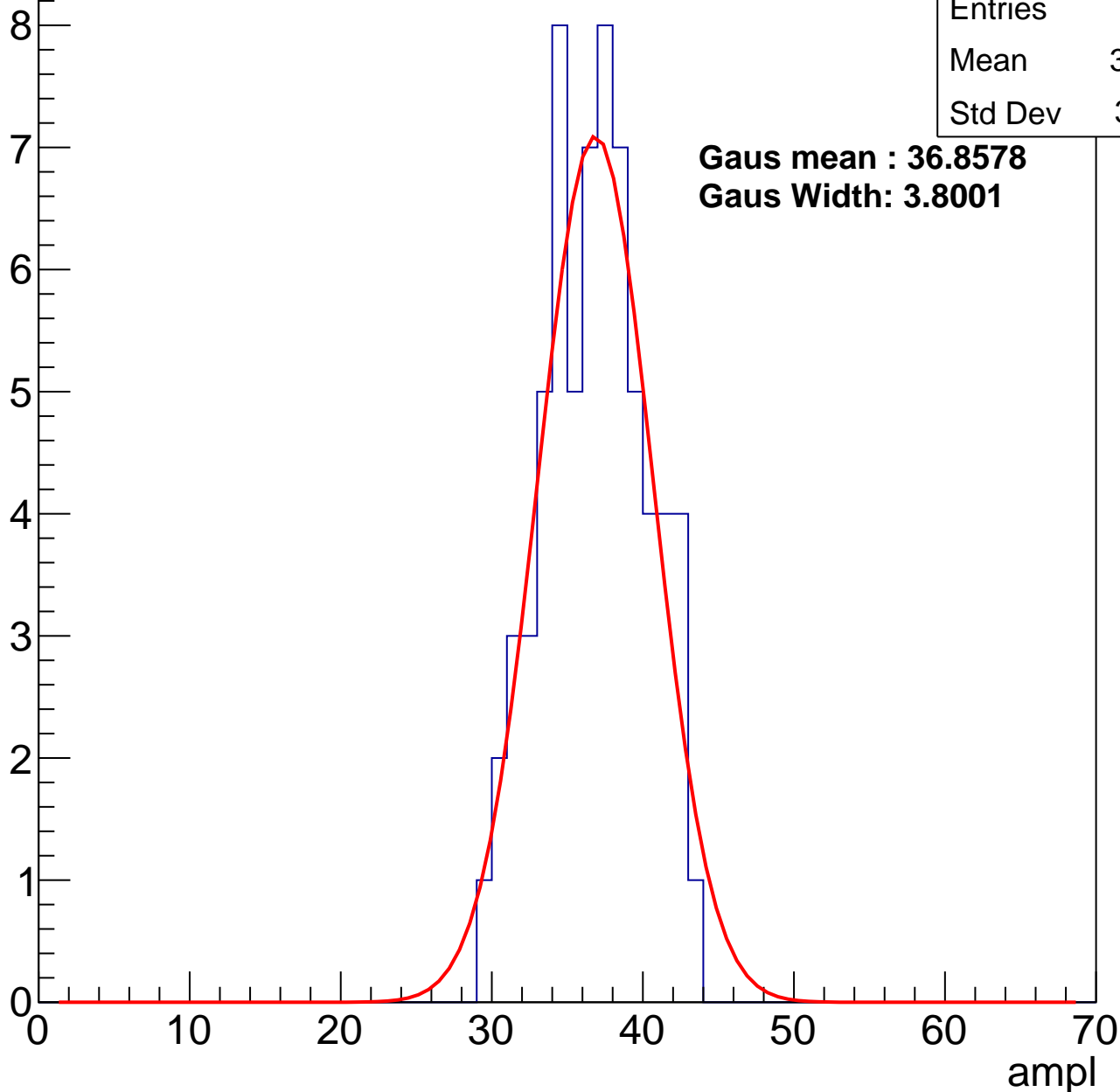
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	67
Mean	36.33
Std Dev	3.361

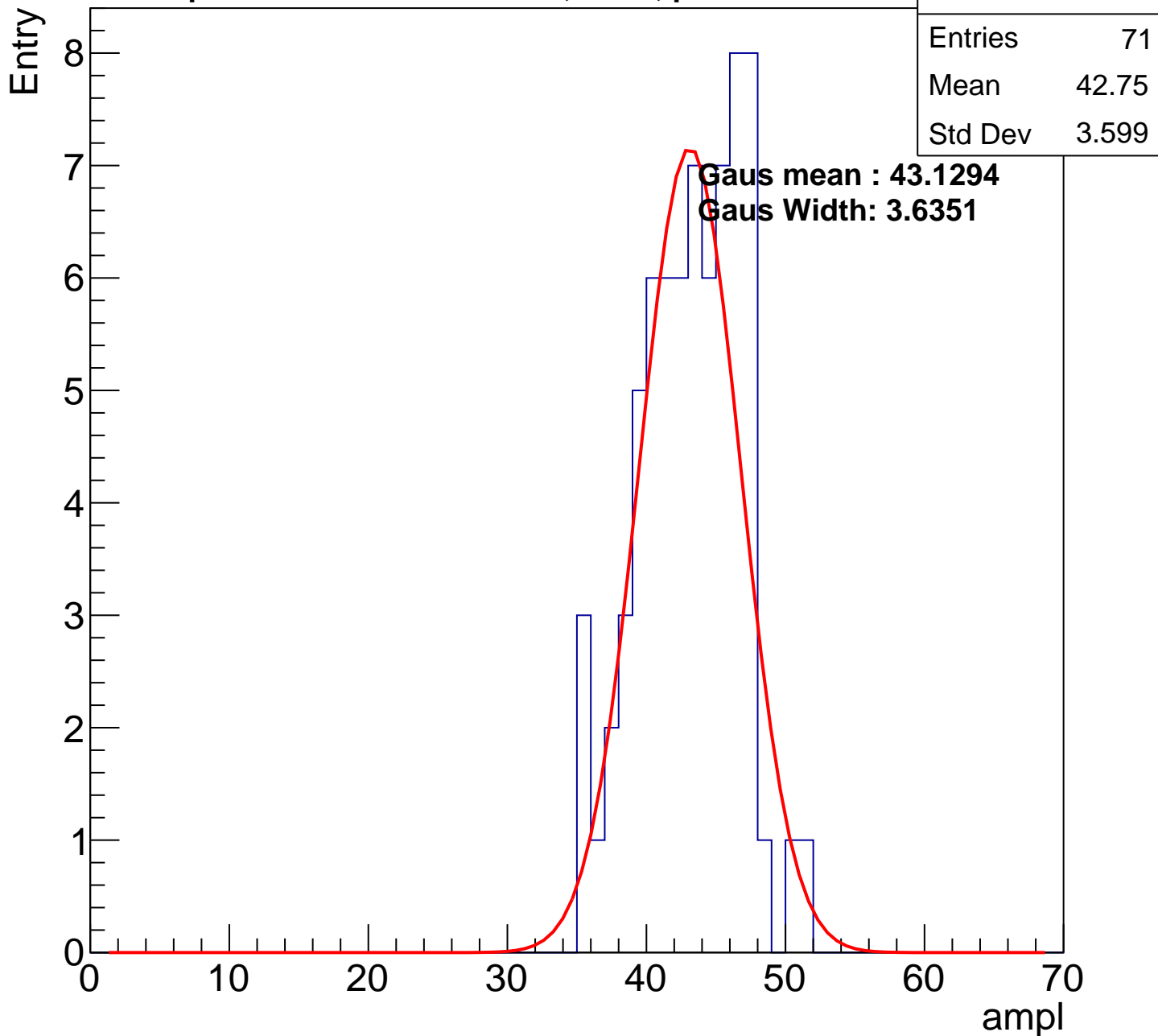
**Gaus mean : 36.8578**

**Gaus Width: 3.8001**



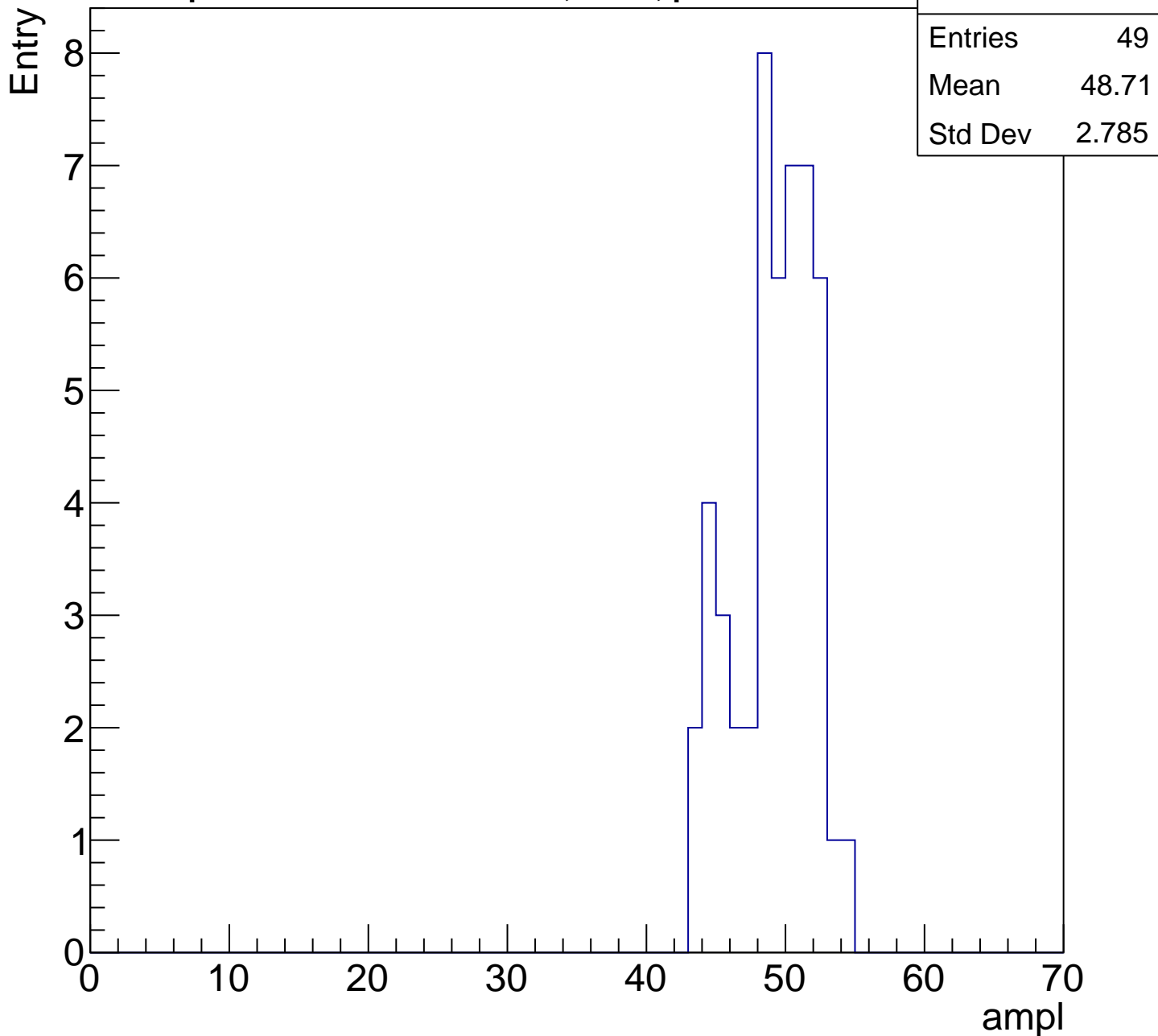
# B1L100S, U6-ch73, adc2

calib\_packv5\_042523\_0143.root, FC#4, port A2



# B1L100S, U6-ch73, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

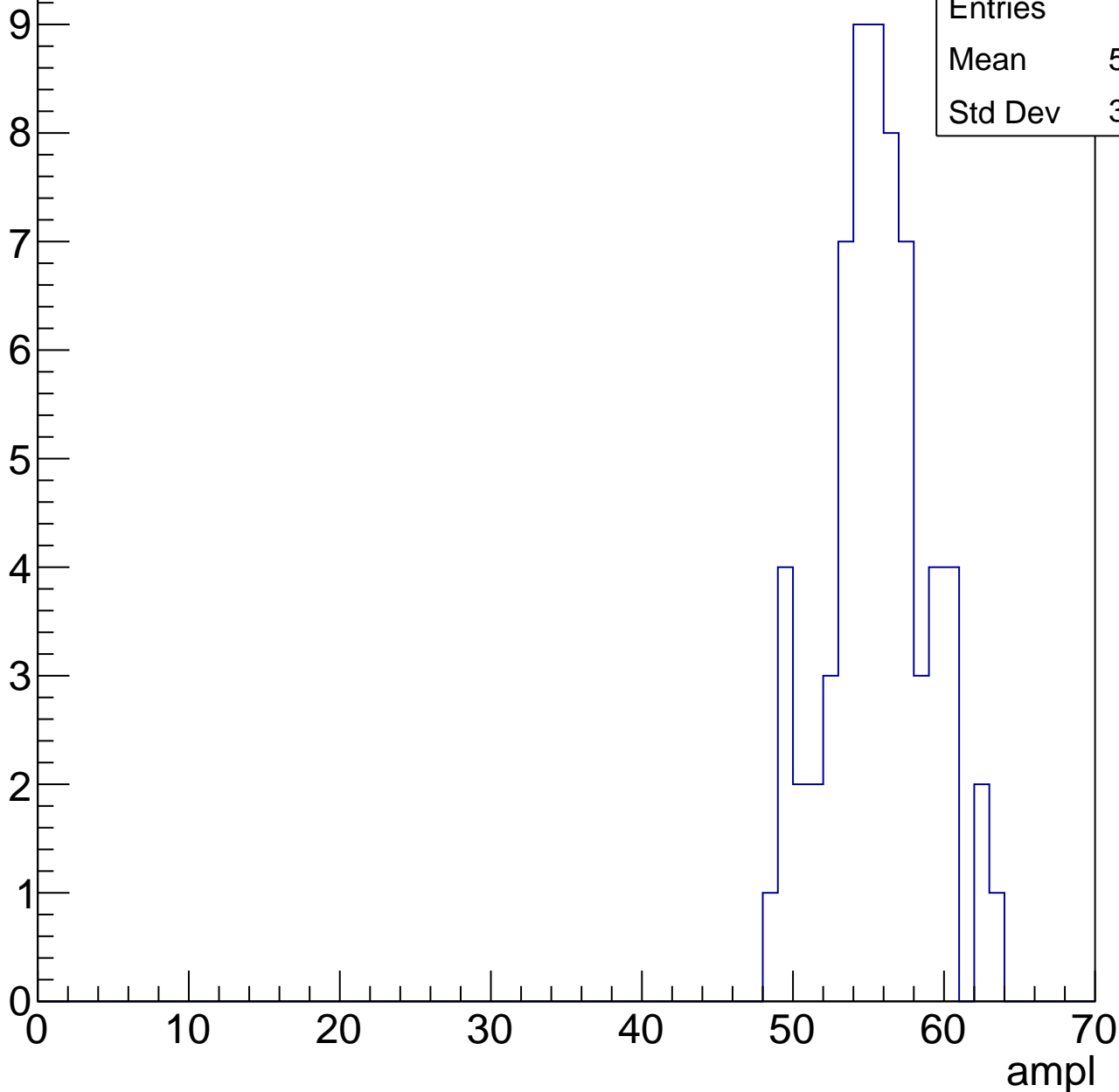


# B1L100S, U6-ch73, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	66
Mean	55.12
Std Dev	3.319

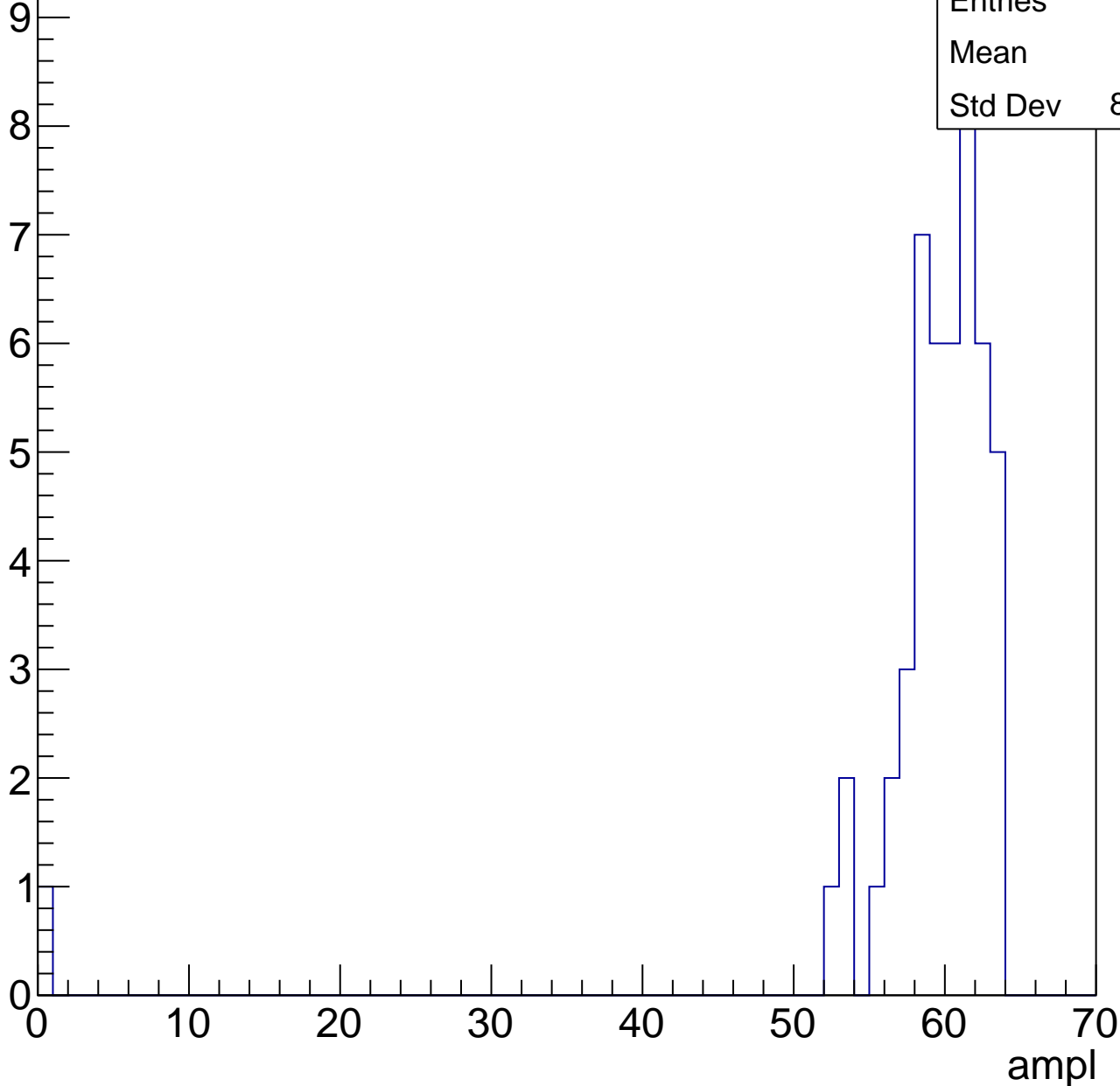


# B1L100S, U6-ch73, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

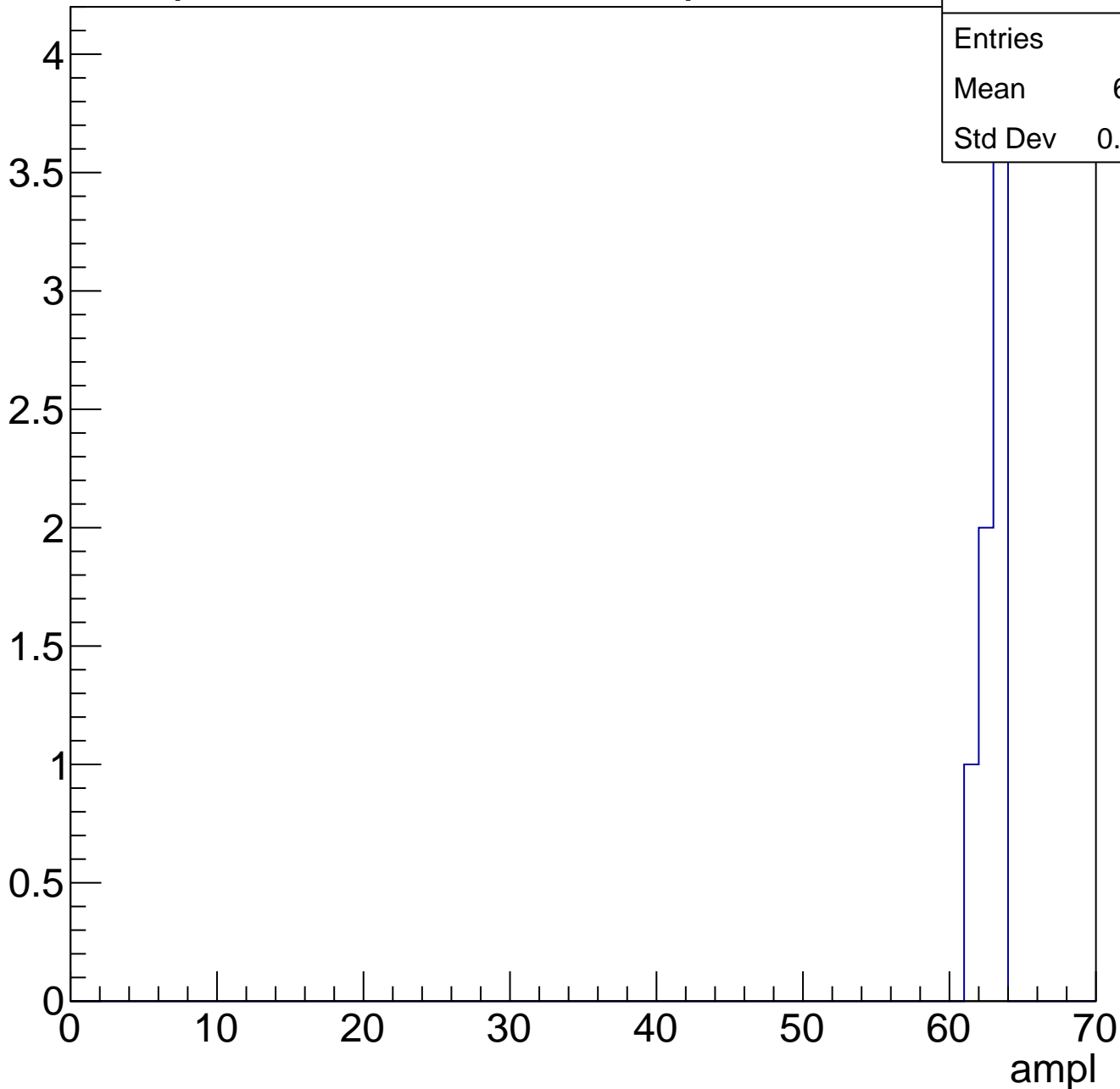
Entries	49
Mean	58.2
Std Dev	8.806



# B1L100S, U6-ch73, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry





# B1L100S, U6-ch73, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



# B1L100S, U6-ch74, adc0

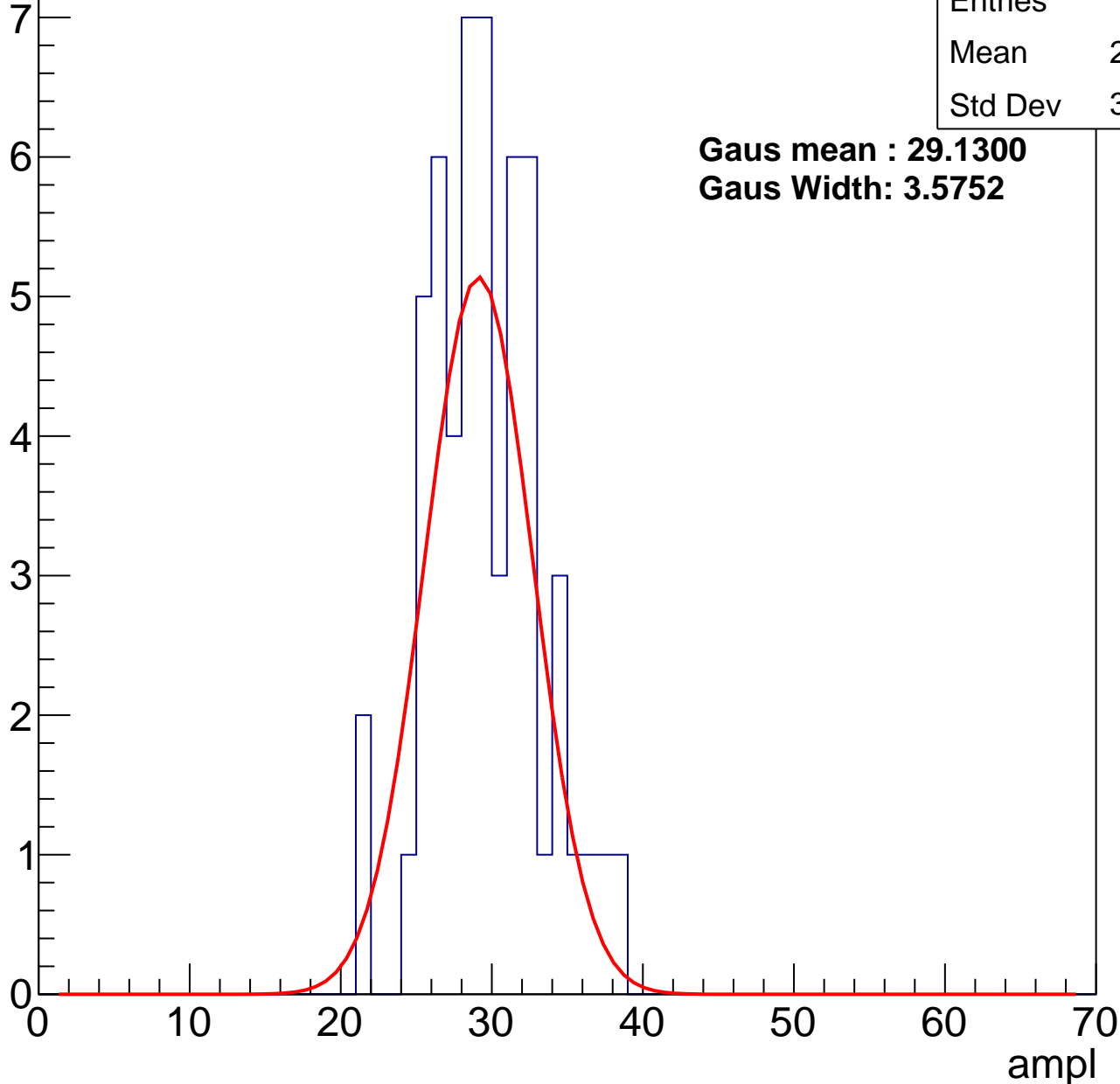
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	55
Mean	29.15
Std Dev	3.595

**Gaus mean : 29.1300**

**Gaus Width: 3.5752**



# B1L100S, U6-ch74, adc1

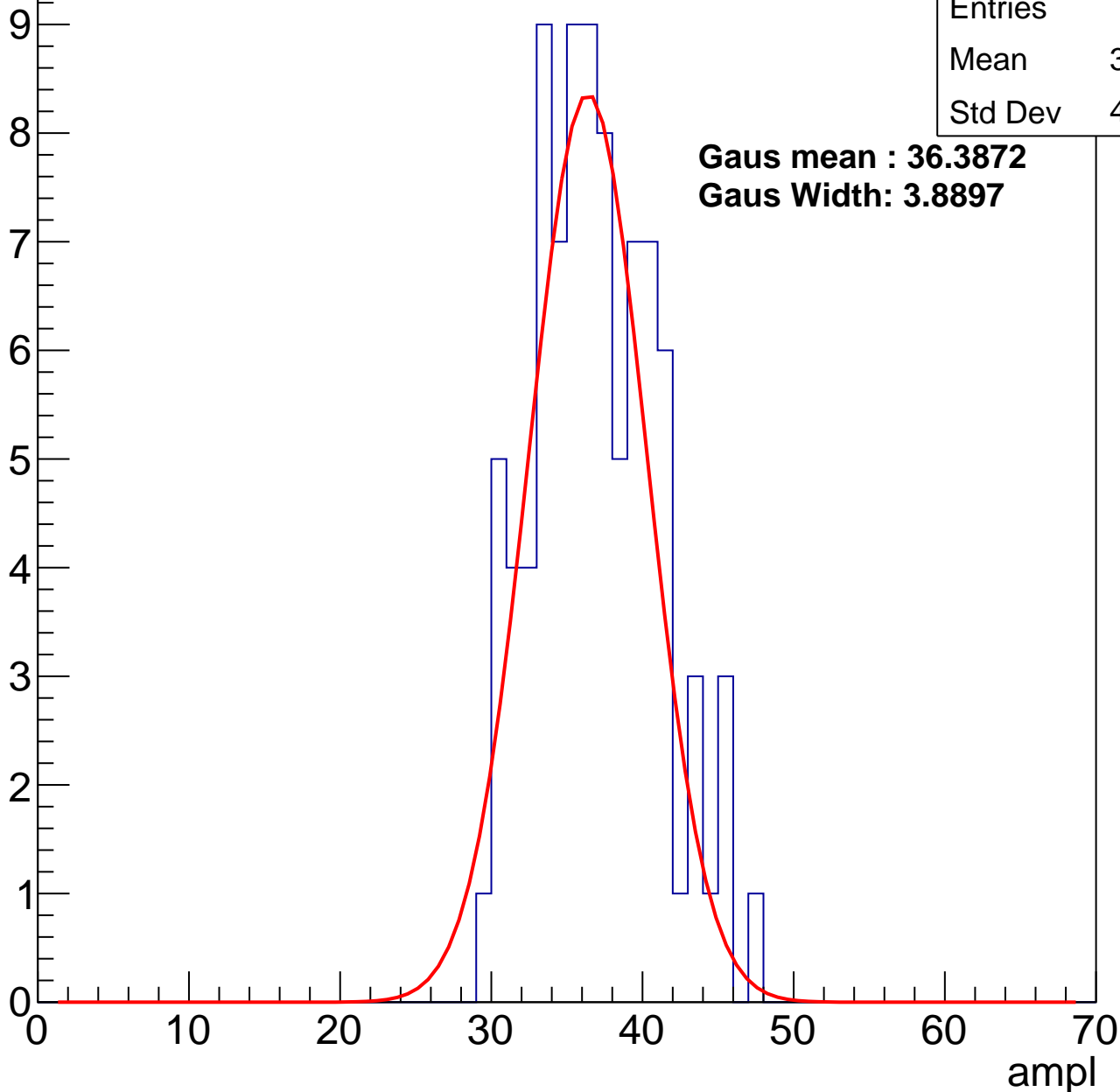
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	90
Mean	36.52
Std Dev	4.014

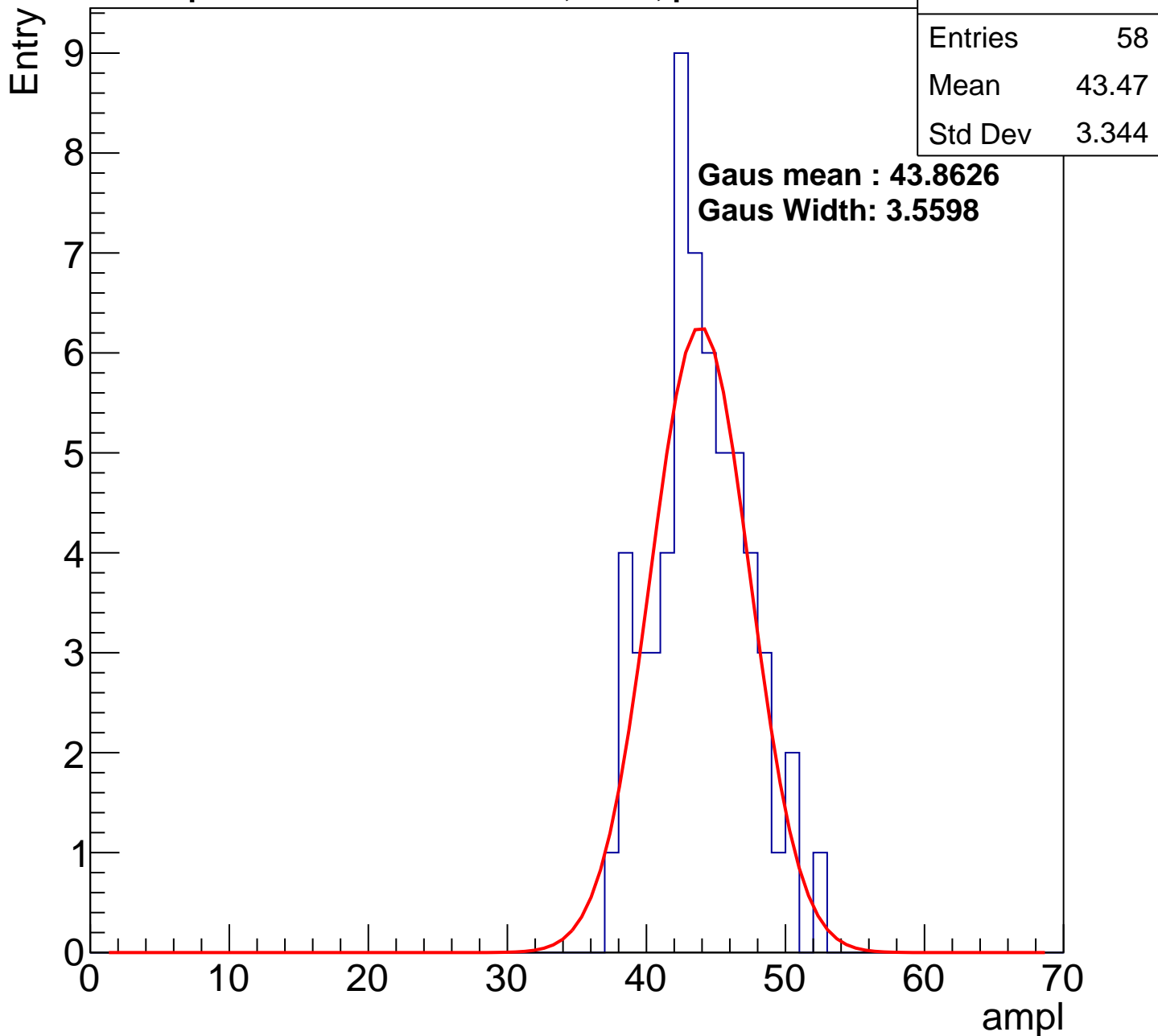
**Gaus mean : 36.3872**

**Gaus Width: 3.8897**



# B1L100S, U6-ch74, adc2

calib\_packv5\_042523\_0143.root, FC#4, port A2

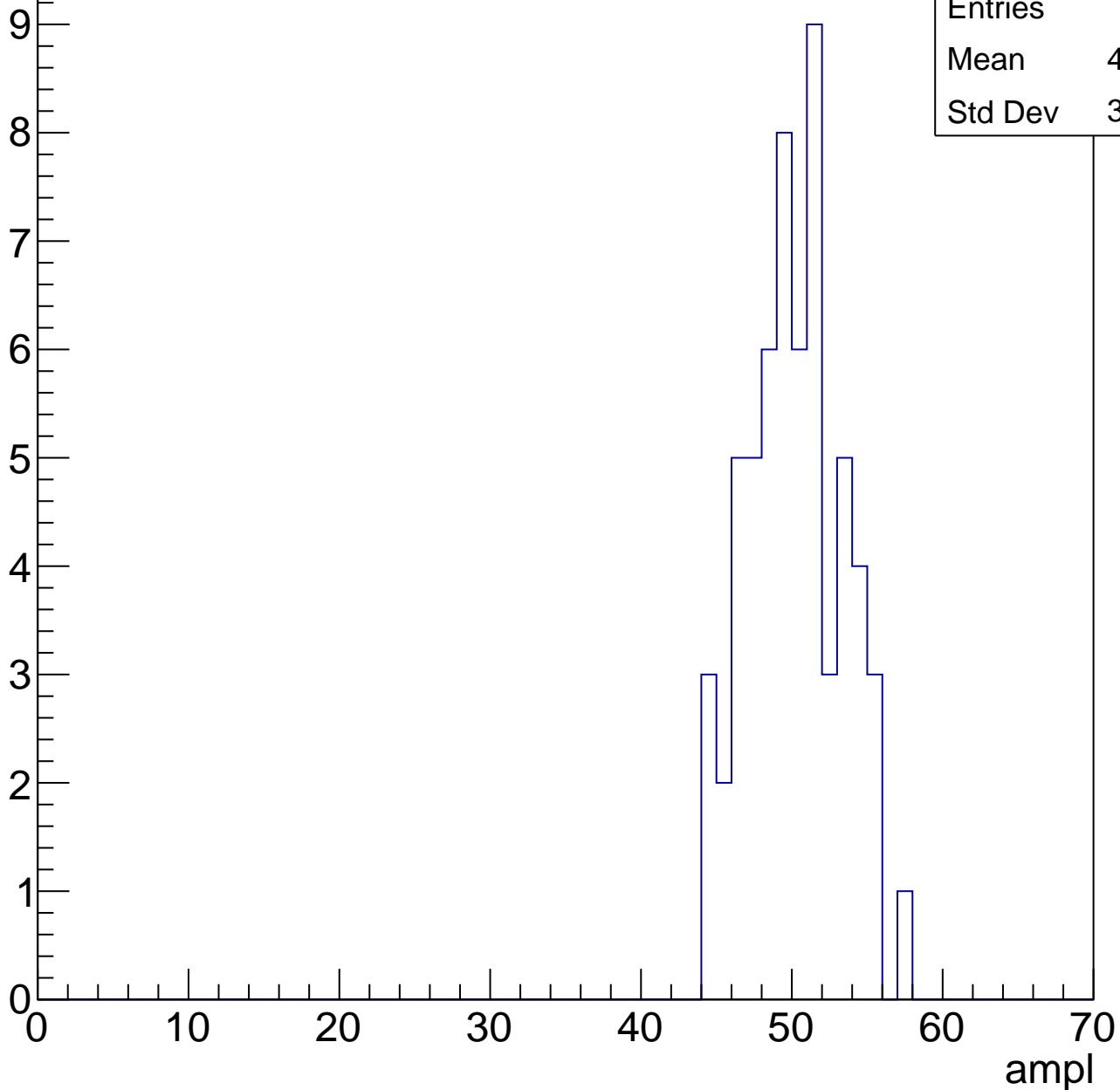


# B1L100S, U6-ch74, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

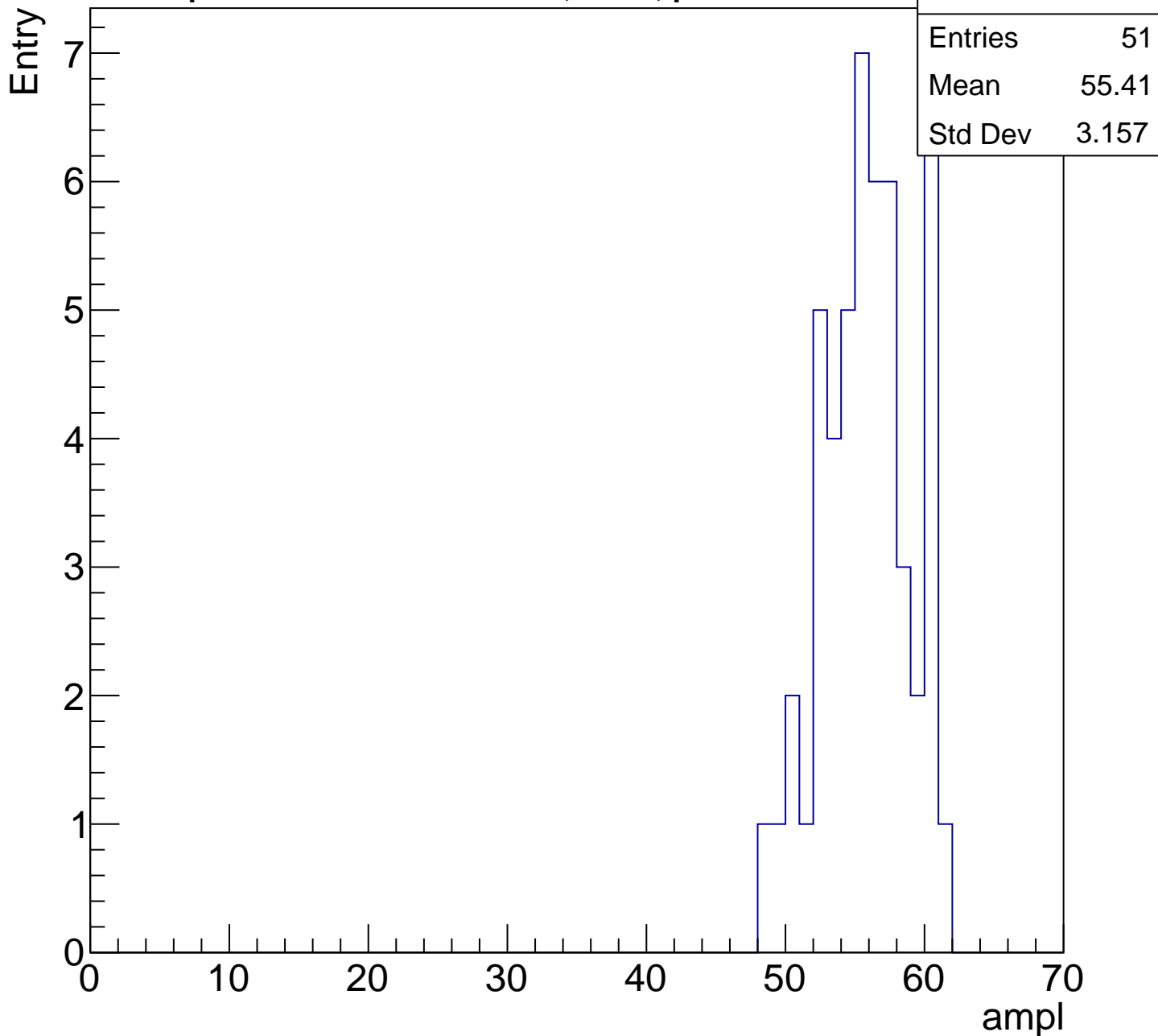
Entry

Entries	60
Mean	49.75
Std Dev	3.069



# B1L100S, U6-ch74, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2



# B1L100S, U6-ch74, adc5

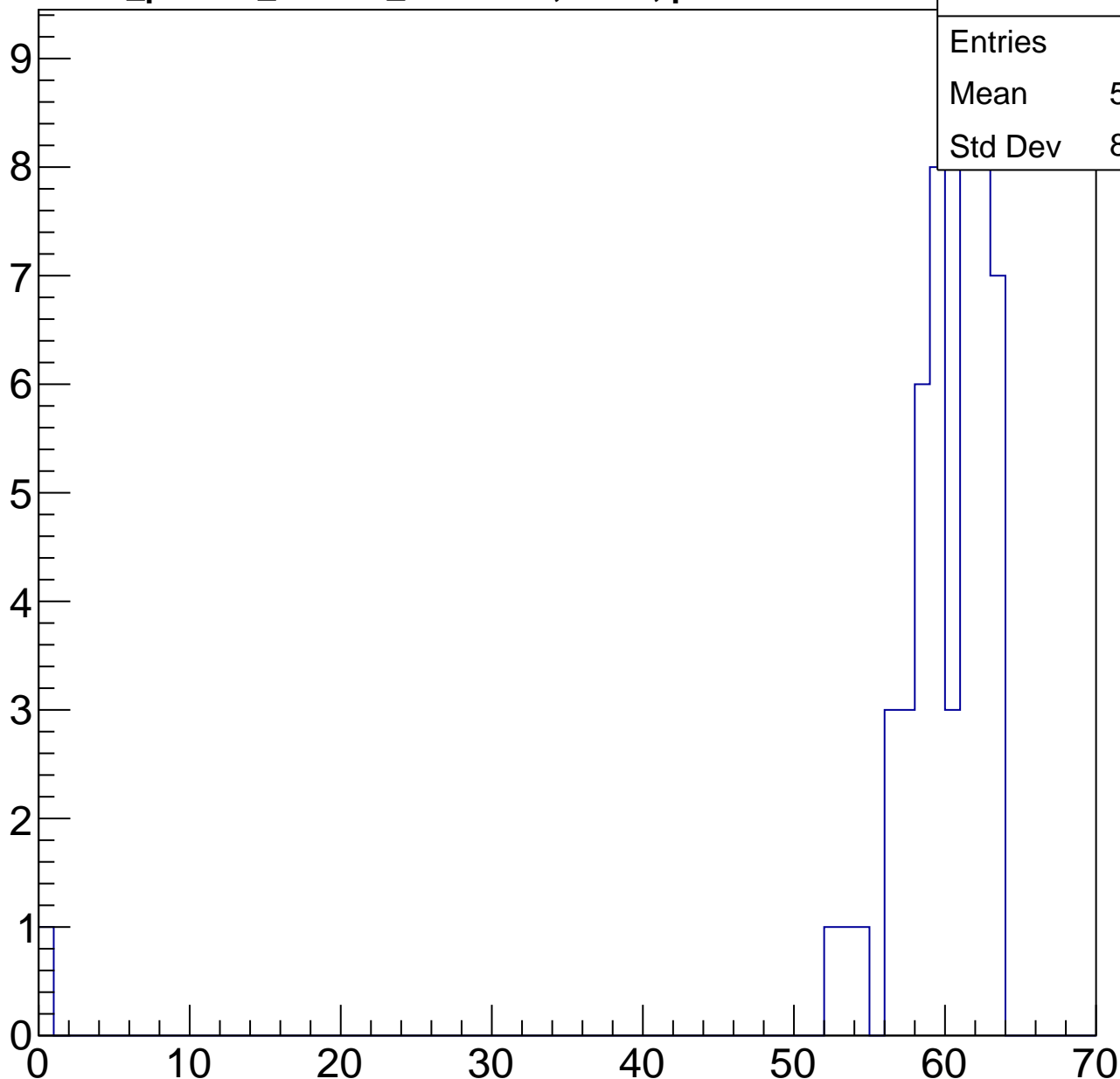
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	51
Mean	58.53
Std Dev	8.692

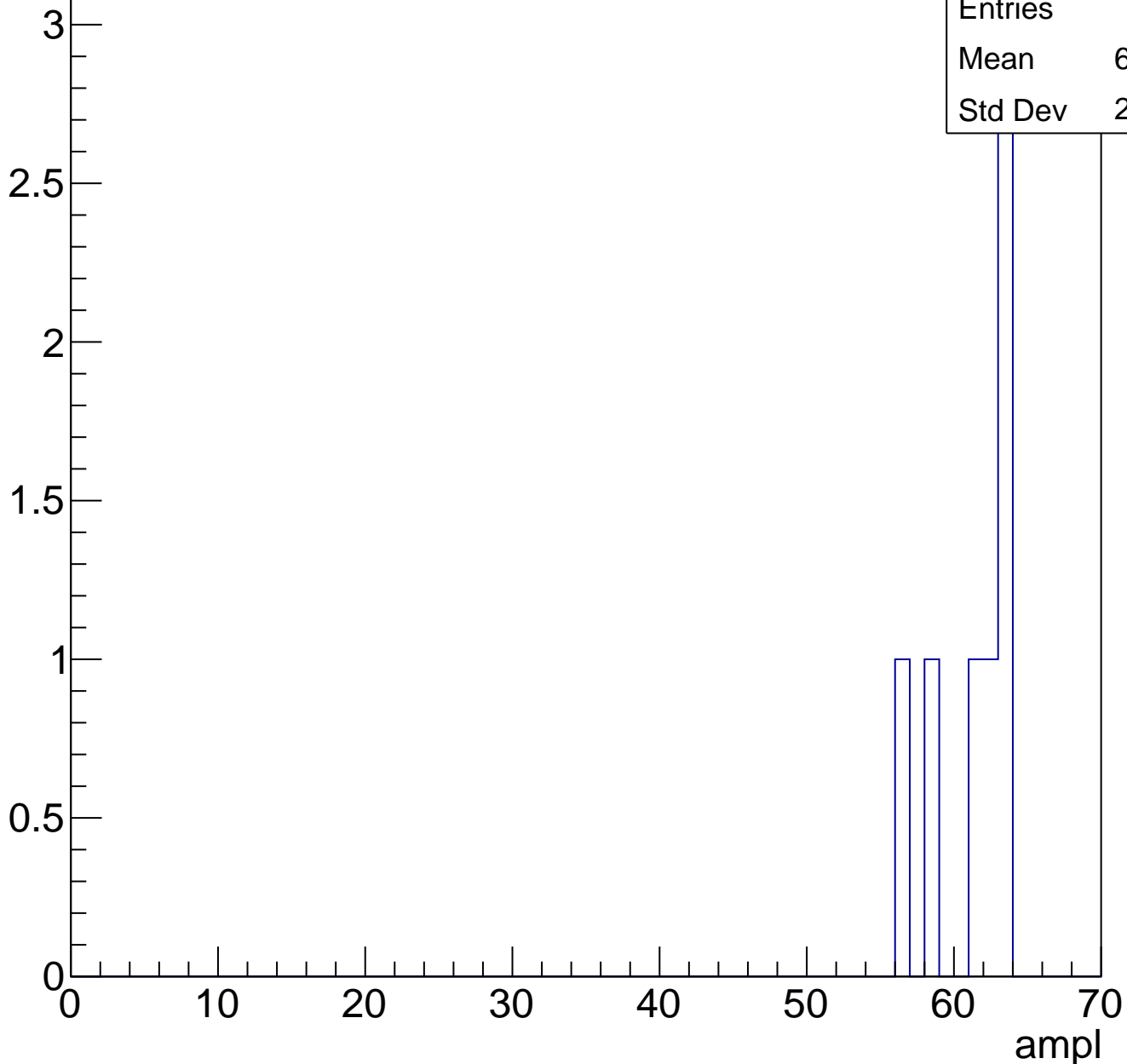
ampl



# B1L100S, U6-ch74, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	7
Mean	60.86
Std Dev	2.587



# B1L100S, U6-ch74, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L100S, U6-ch75, adc0

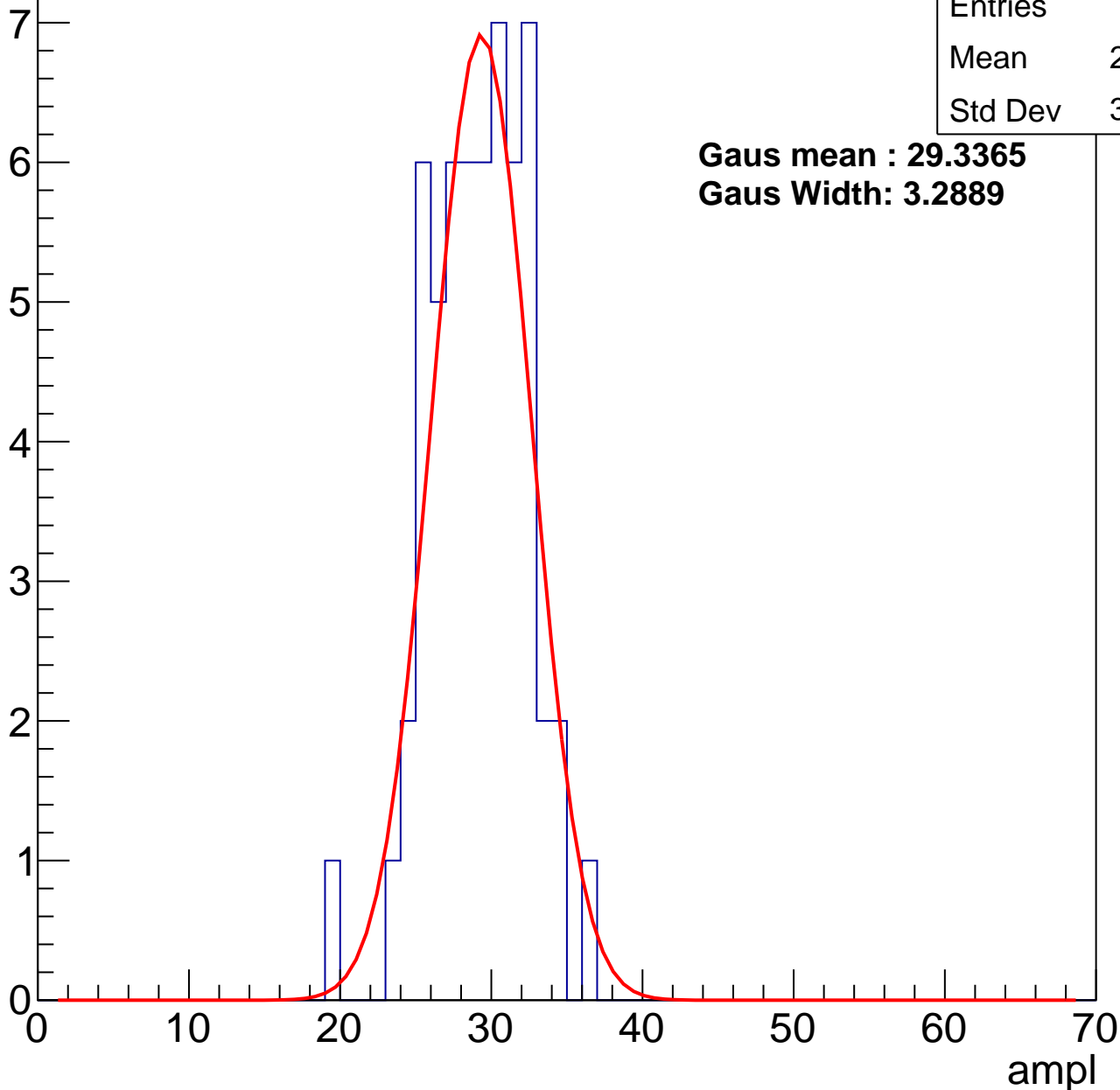
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	58
Mean	28.69
Std Dev	3.152

**Gaus mean : 29.3365**

**Gaus Width: 3.2889**



# B1L100S, U6-ch75, adc1

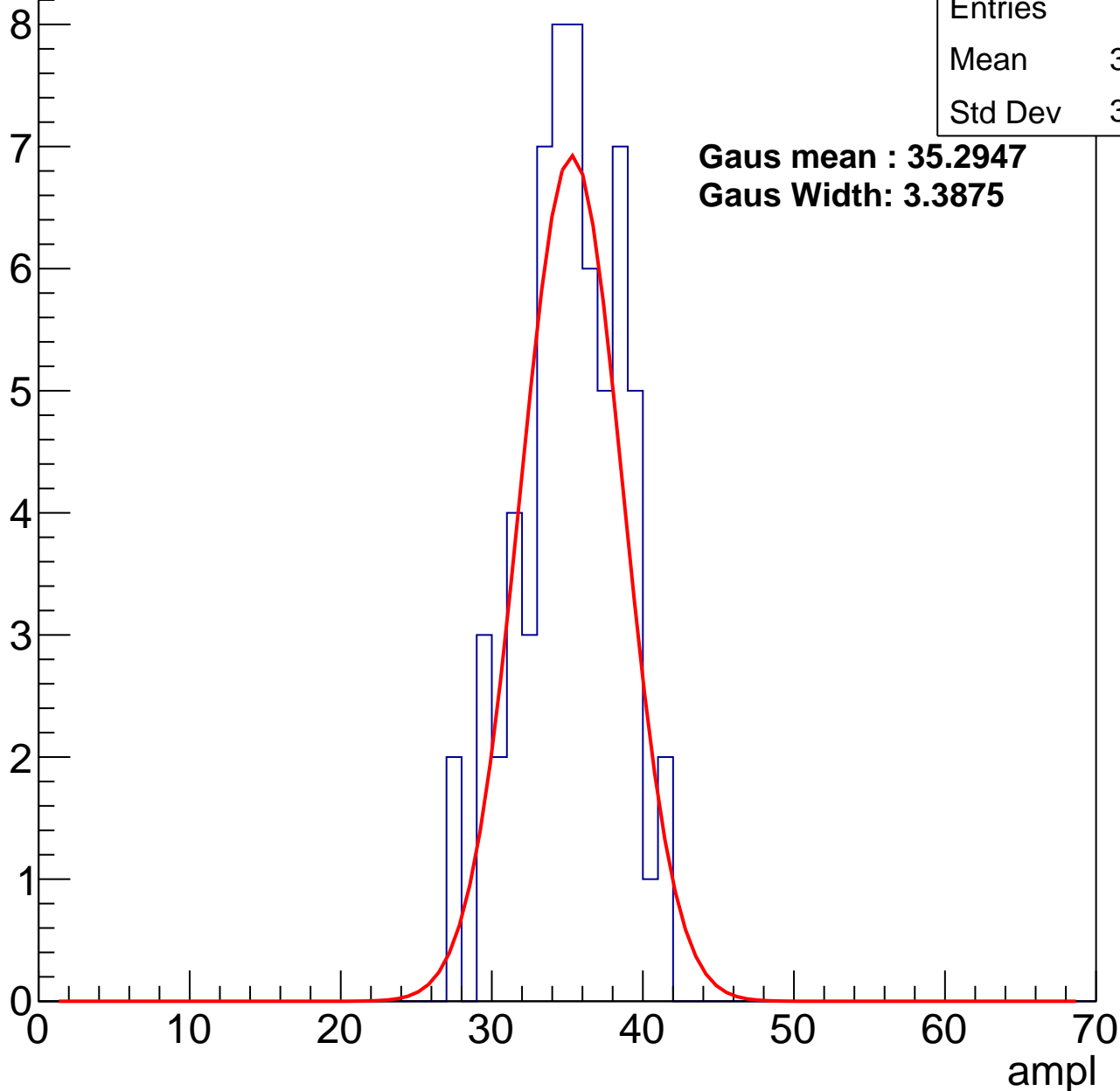
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	63
Mean	34.73
Std Dev	3.272

**Gaus mean : 35.2947**

**Gaus Width: 3.3875**



# B1L100S, U6-ch75, adc2

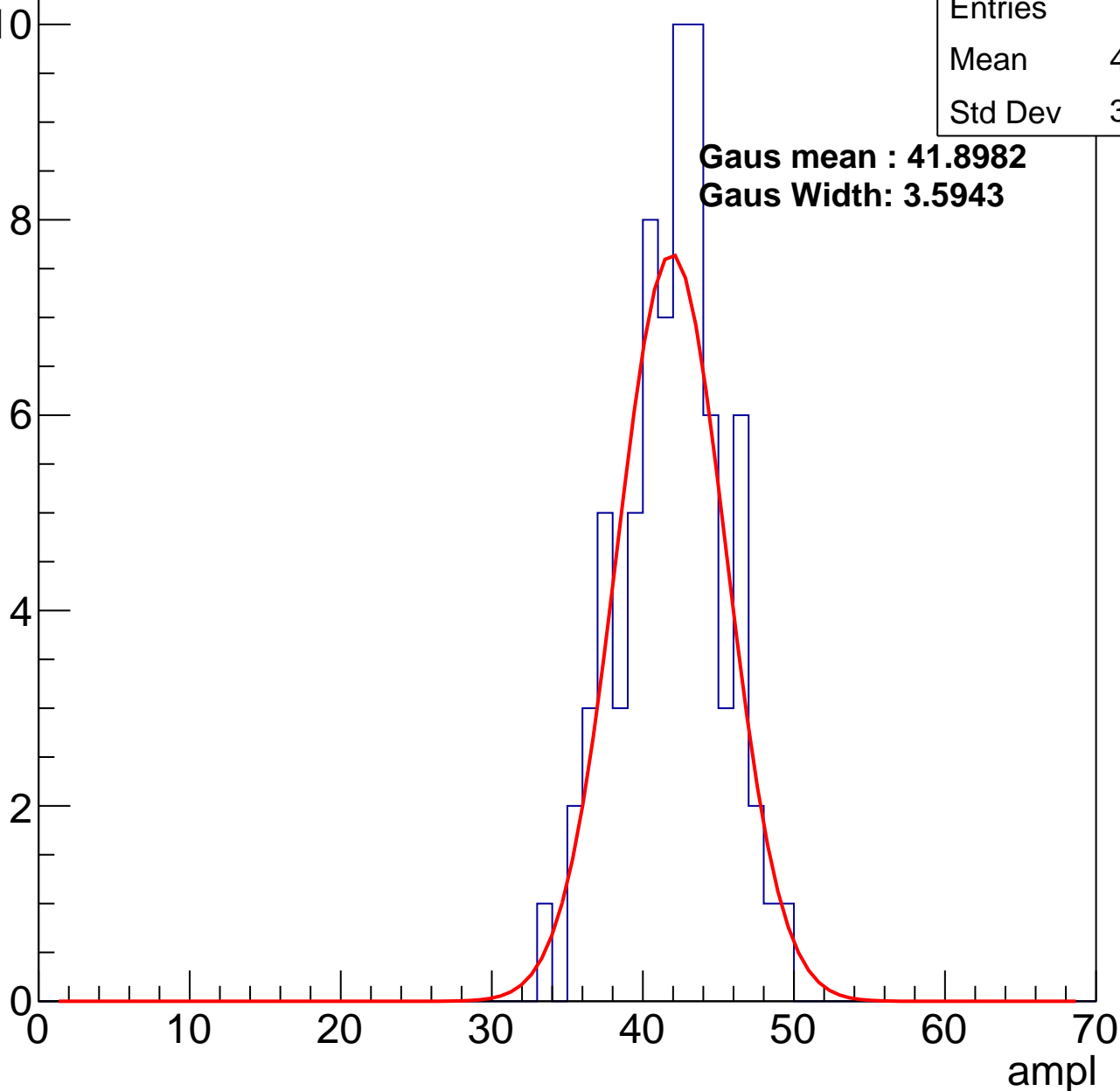
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	73
Mean	41.48
Std Dev	3.344

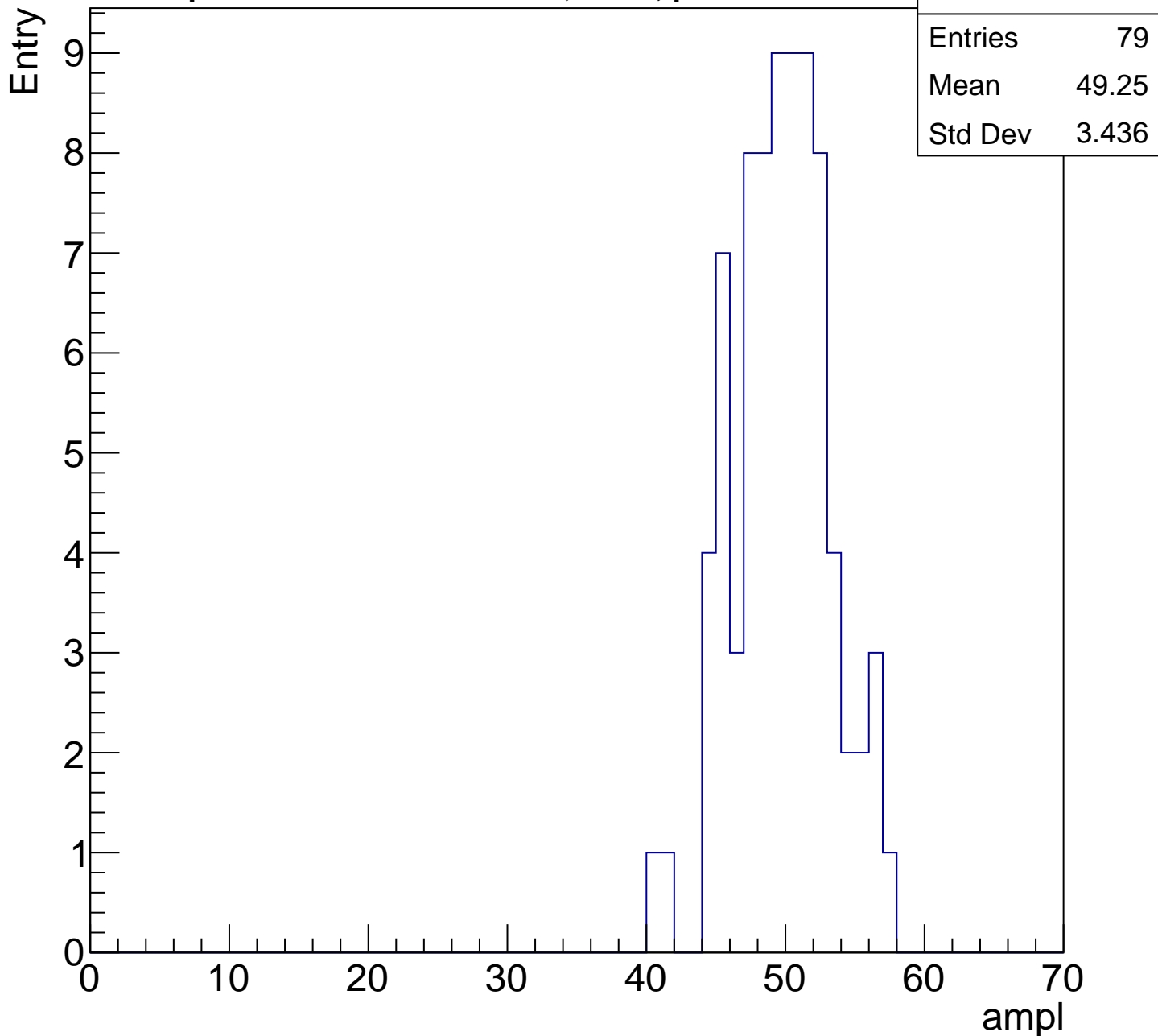
**Gaus mean : 41.8982**

**Gaus Width: 3.5943**



# B1L100S, U6-ch75, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

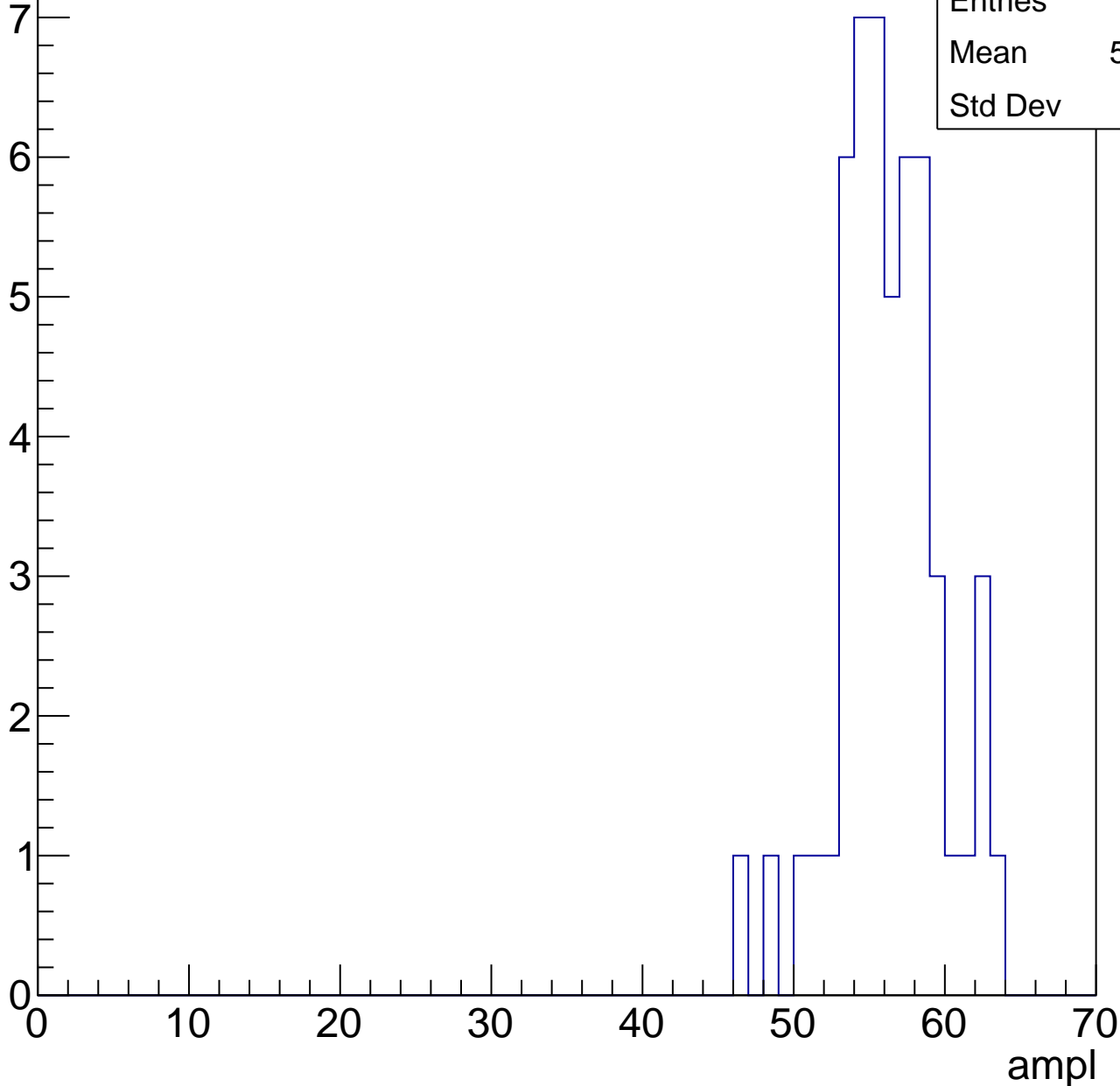


# B1L100S, U6-ch75, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

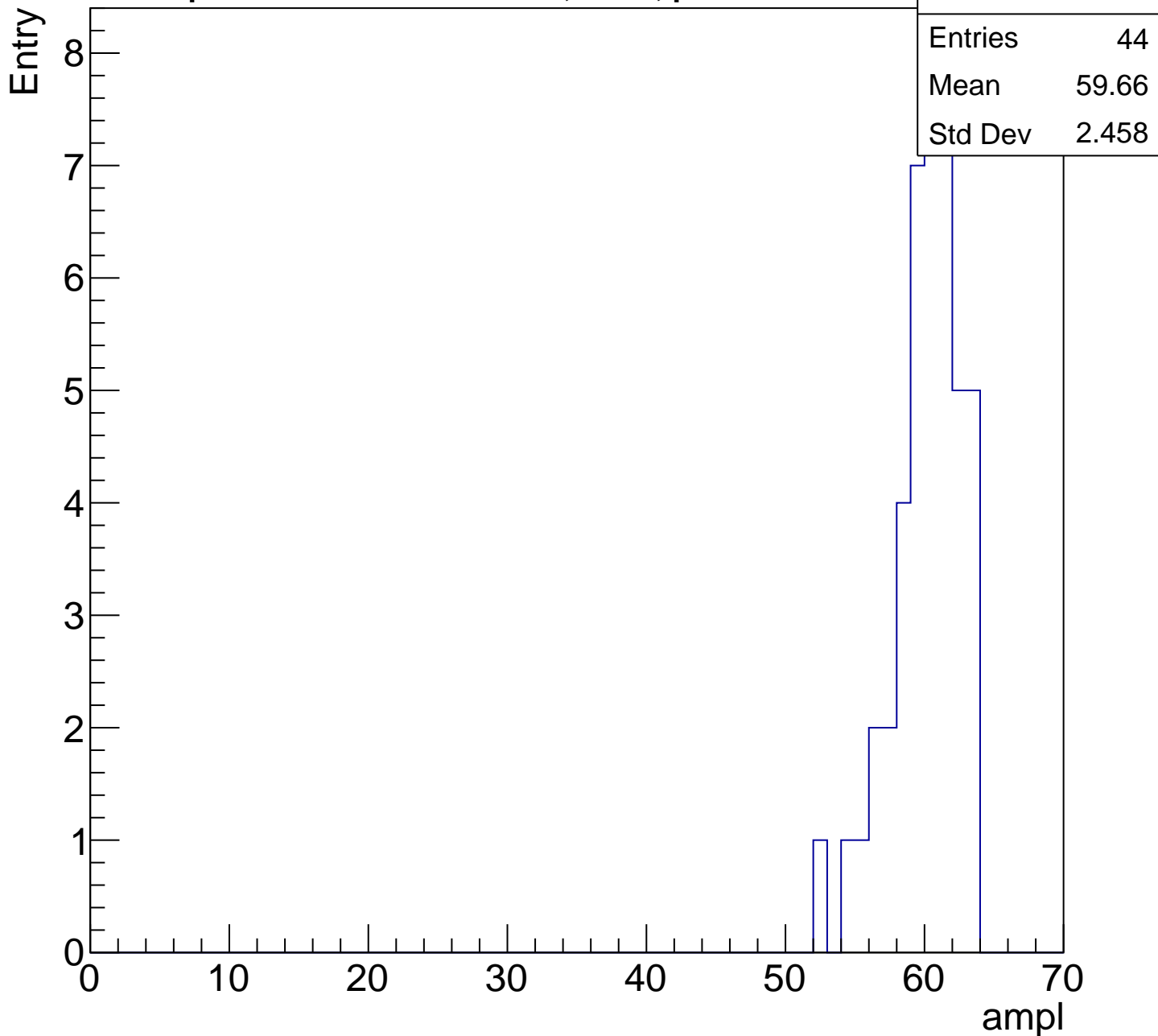
Entry

Entries	51
Mean	55.78
Std Dev	3.38



# B1L100S, U6-ch75, adc5

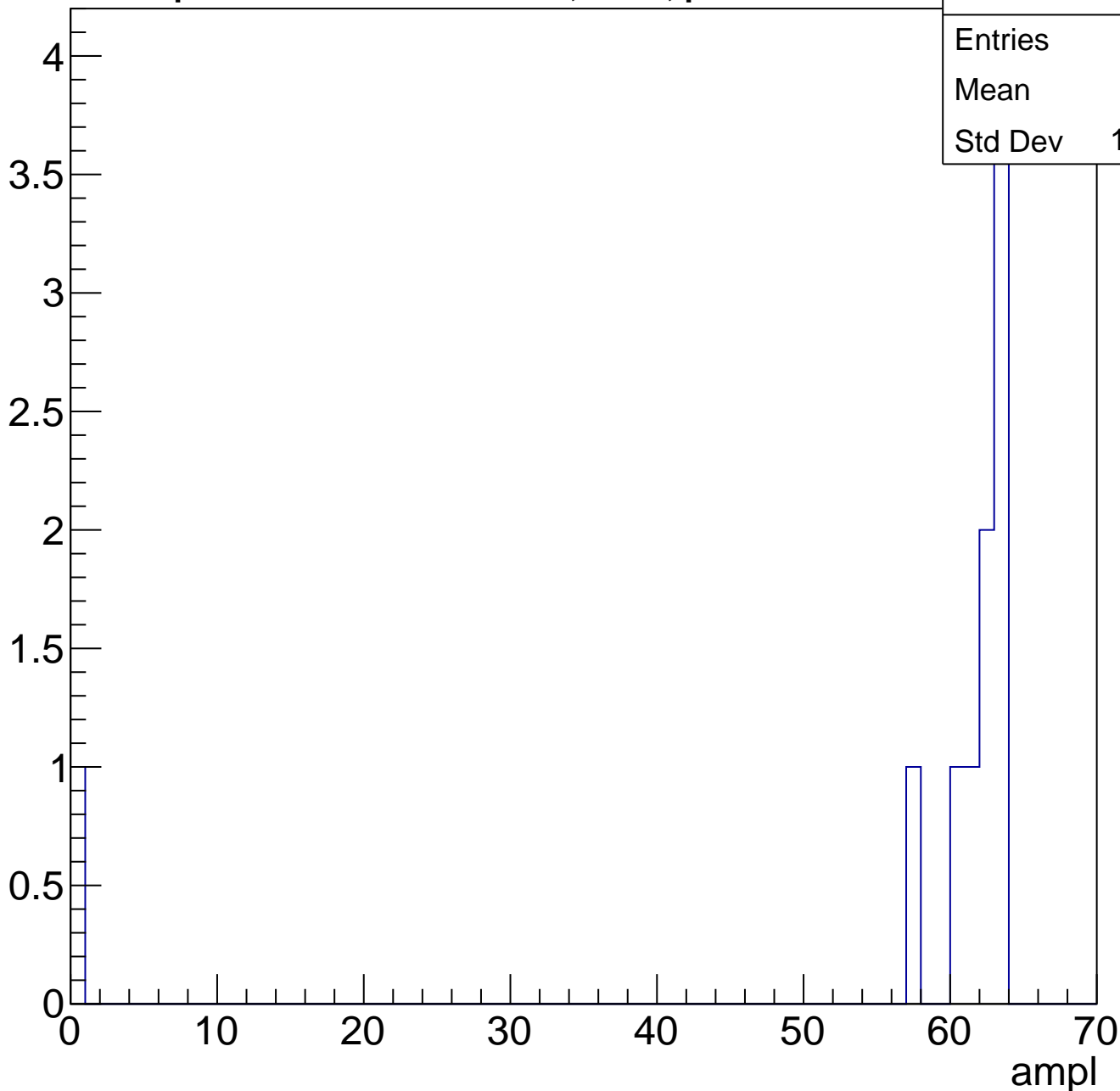
calib\_packv5\_042523\_0143.root, FC#4, port A2



# B1L100S, U6-ch75, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	10
Mean	55.4
Std Dev	18.55



# B1L100S, U6-ch75, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L100S, U6-ch76, adc0

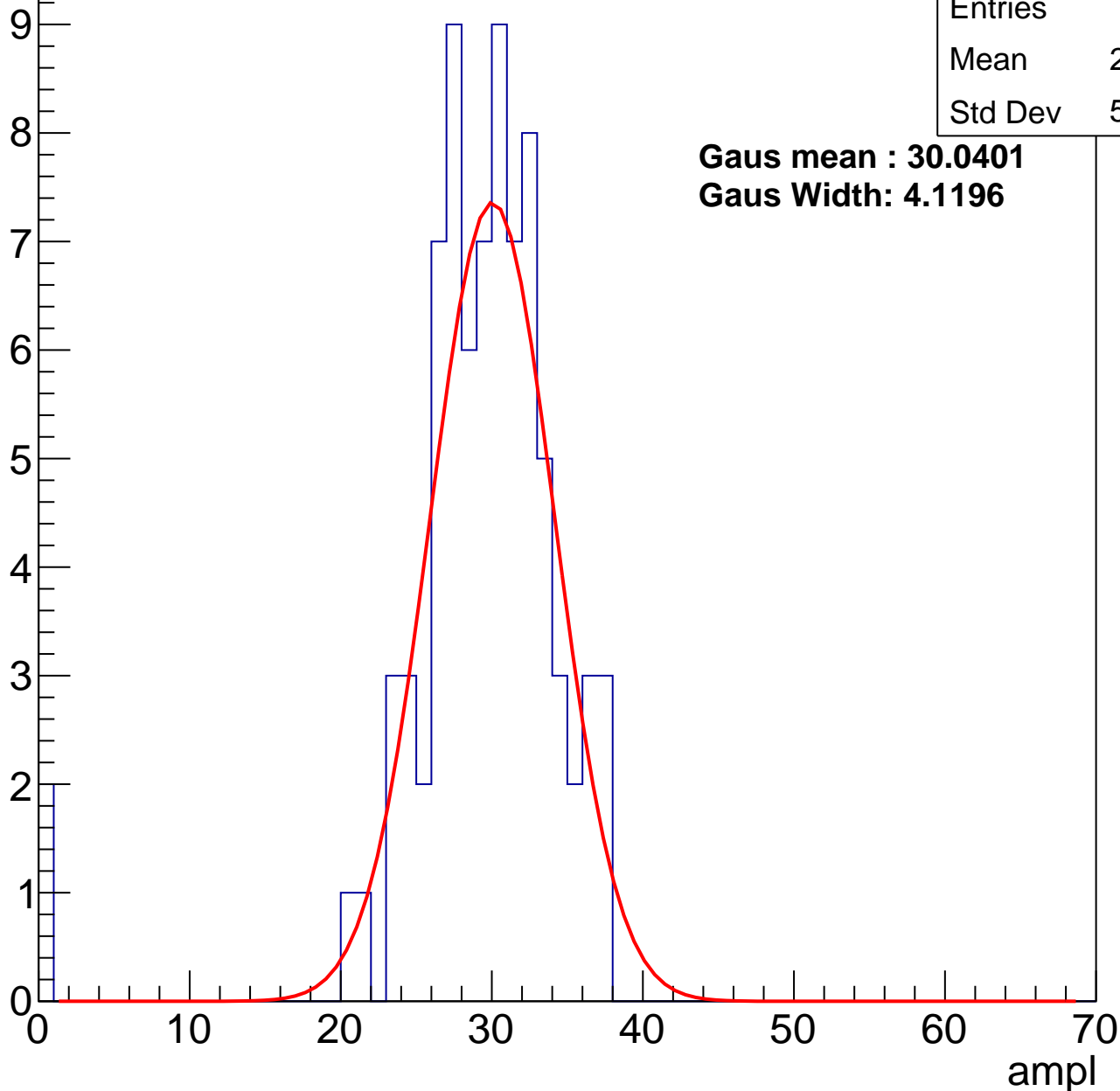
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	81
Mean	28.73
Std Dev	5.896

**Gaus mean : 30.0401**

**Gaus Width: 4.1196**



# B1L100S, U6-ch76, adc1

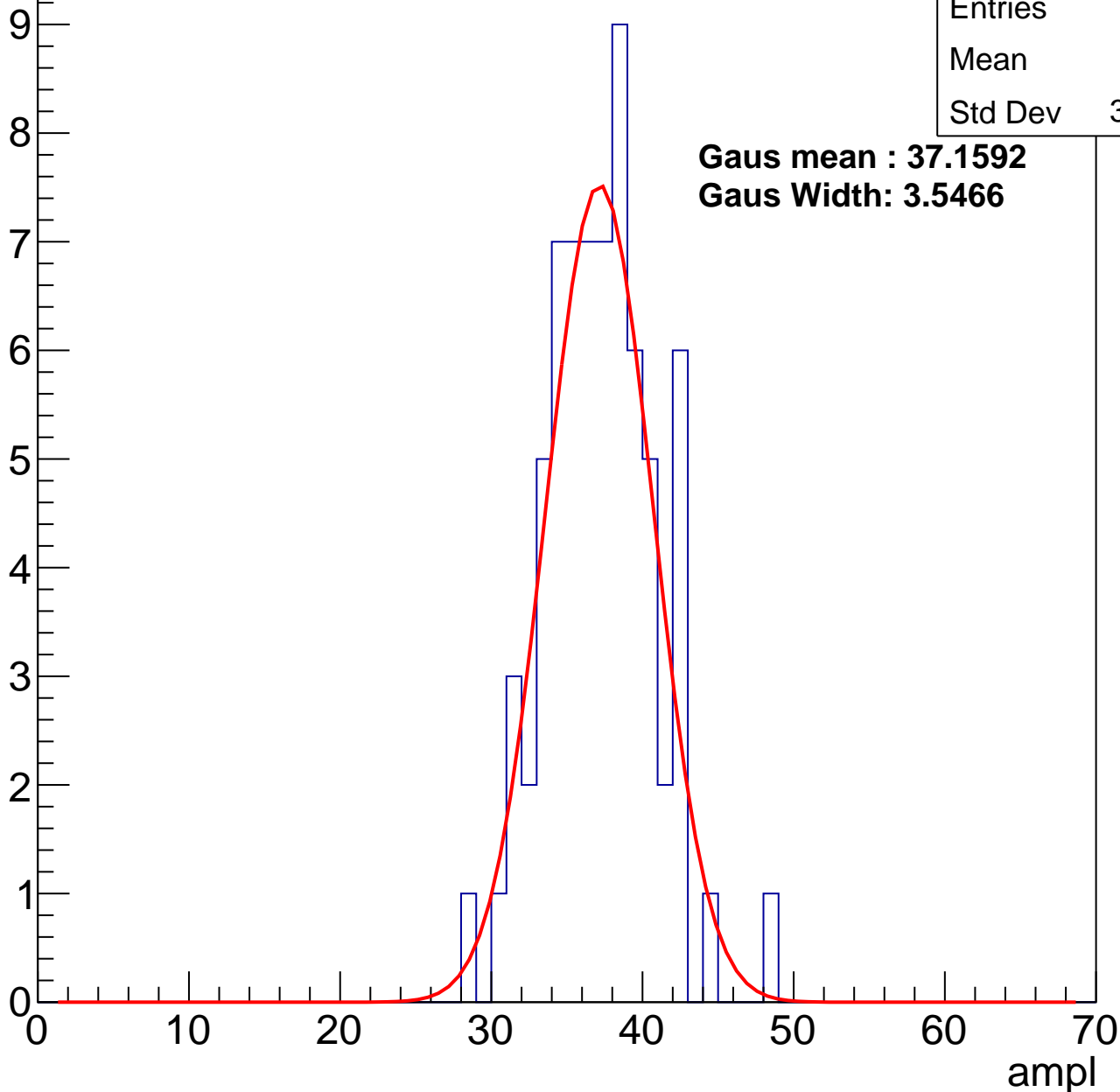
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	70
Mean	36.8
Std Dev	3.572

**Gaus mean : 37.1592**

**Gaus Width: 3.5466**



# B1L100S, U6-ch76, adc2

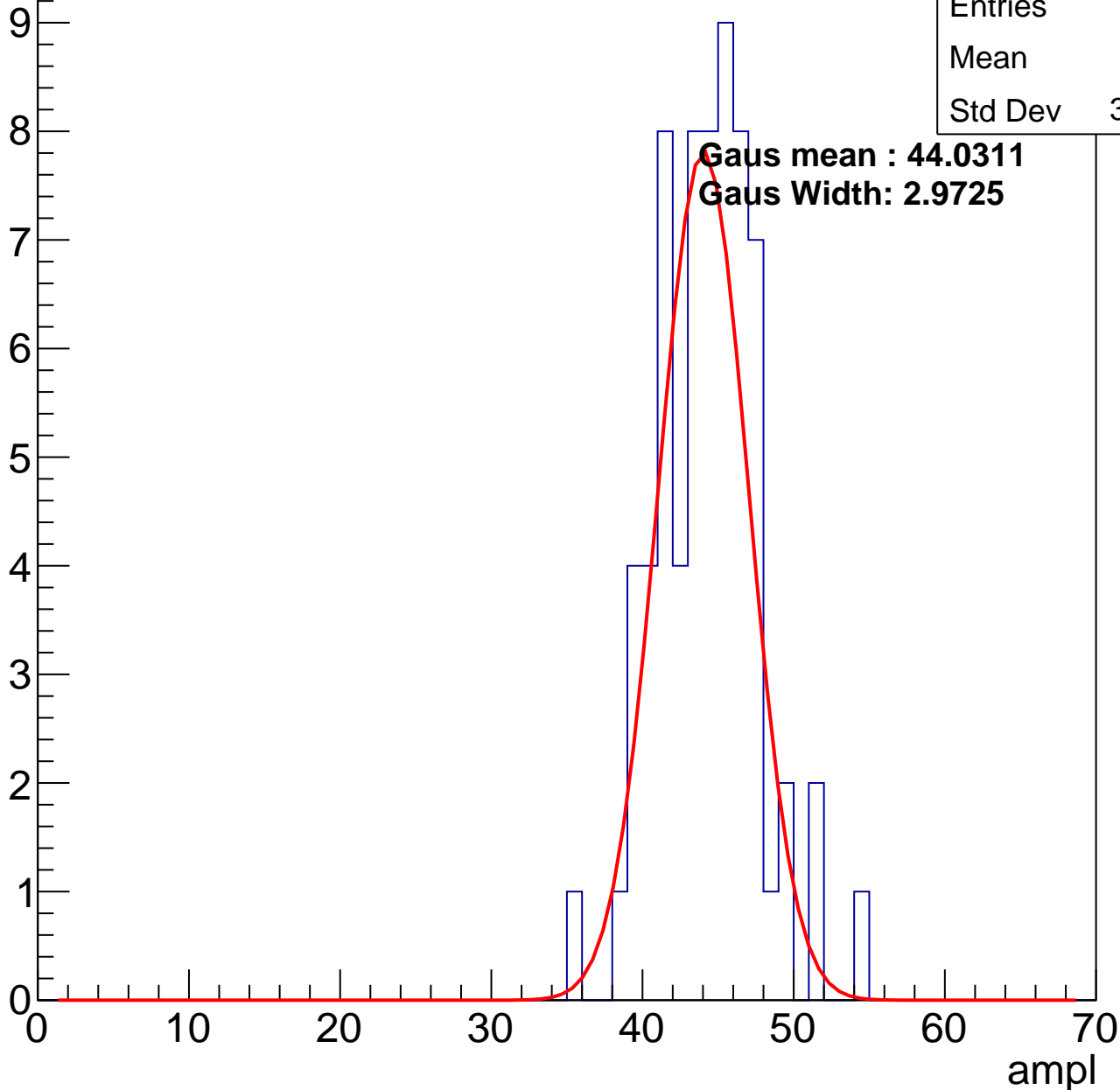
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	68
Mean	43.9
Std Dev	3.308

**Gaus mean : 44.0311**

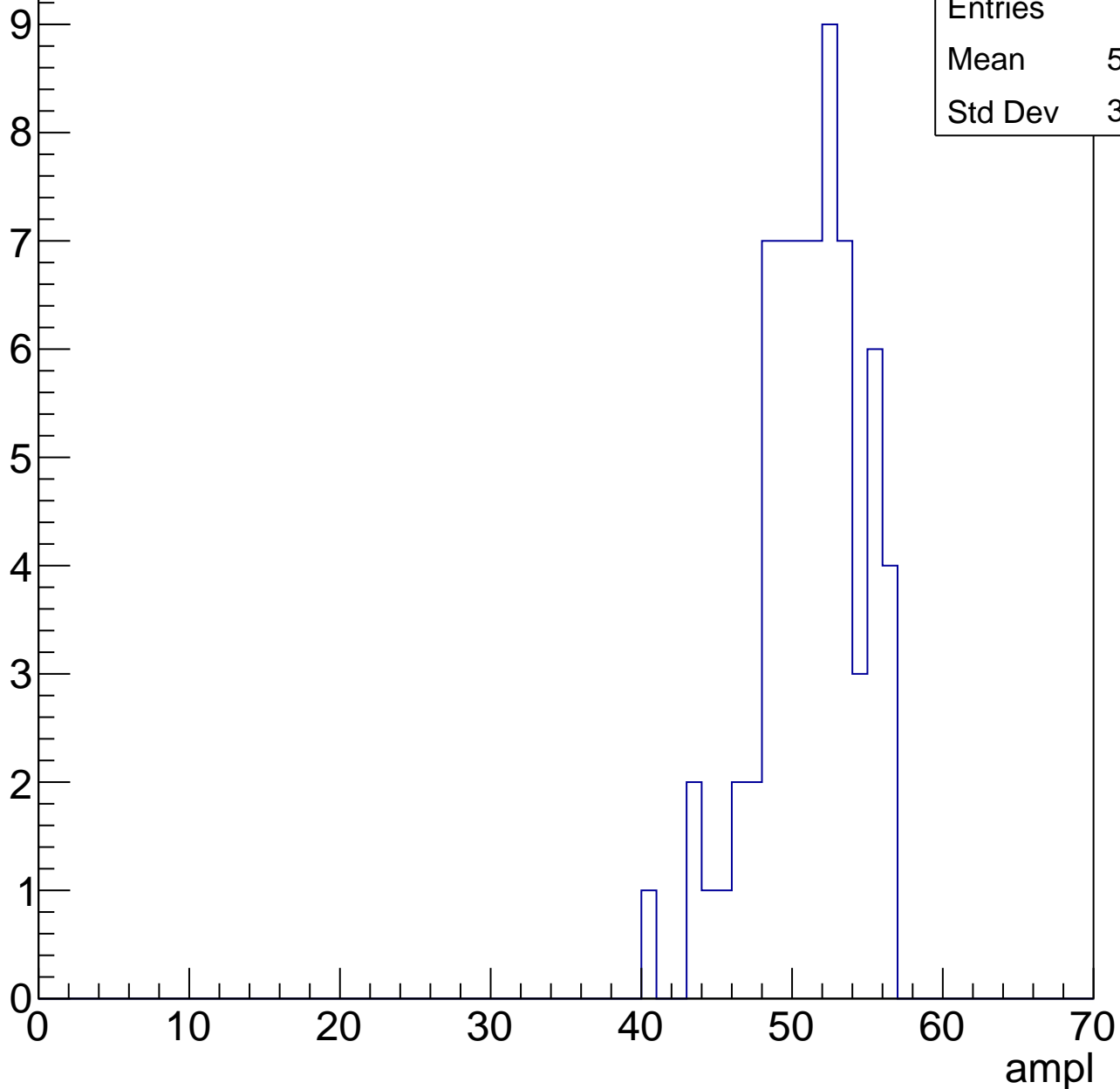
**Gaus Width: 2.9725**



# B1L100S, U6-ch76, adc3

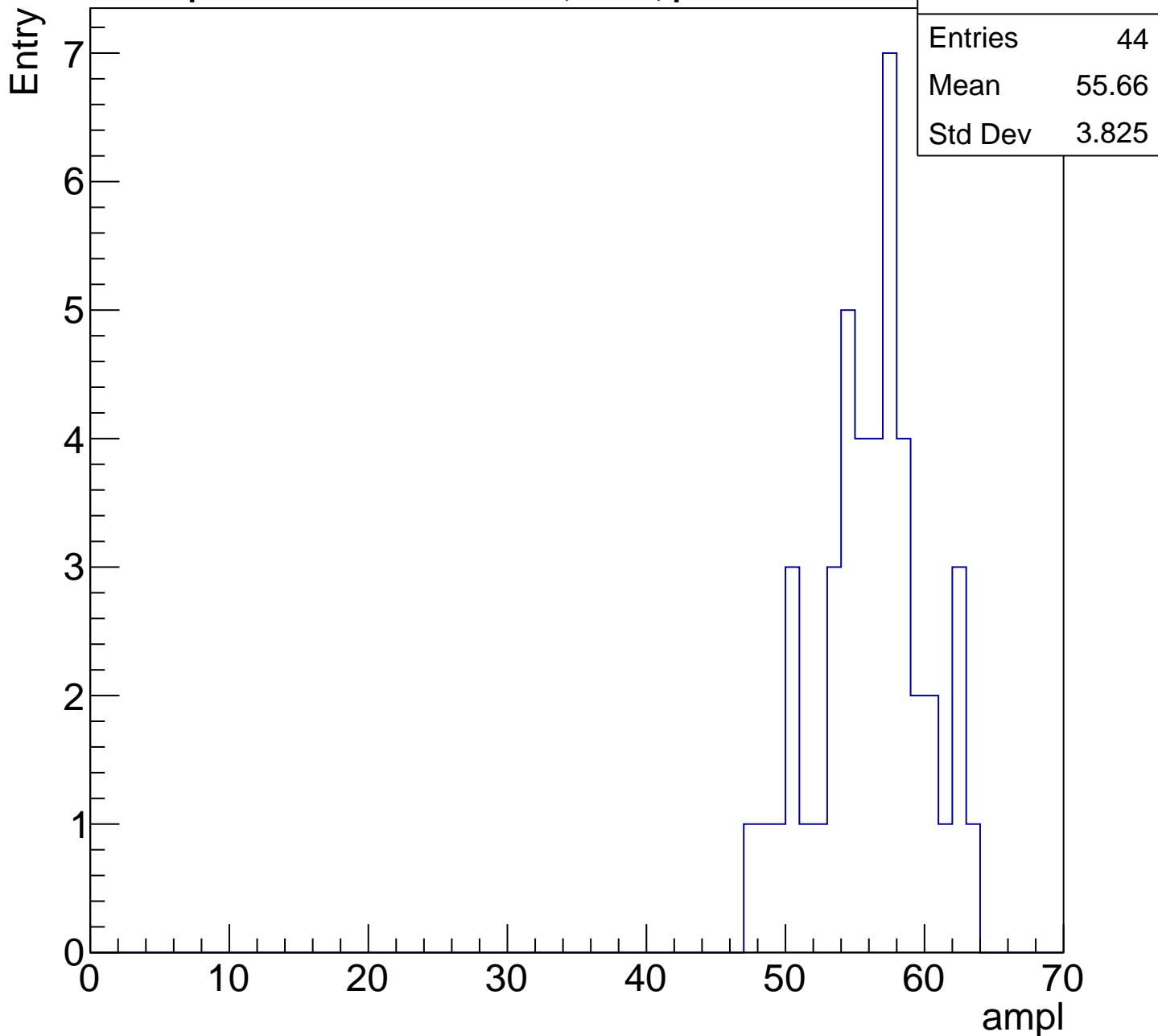
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



# B1L100S, U6-ch76, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2



# B1L100S, U6-ch76, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	51
Mean	58.92
Std Dev	8.591

ampl

0 10 20 30 40 50 60 70

0

1

2

3

4

5

6

7

8

9

# B1L100S, U6-ch76, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

1  
0.8  
0.6  
0.4  
0.2  
0

Entries	3
Mean	60.67
Std Dev	2.625

0 10 20 30 40 50 60 70

ampl



# B1L100S, U6-ch76, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L100S, U6-ch77, adc0

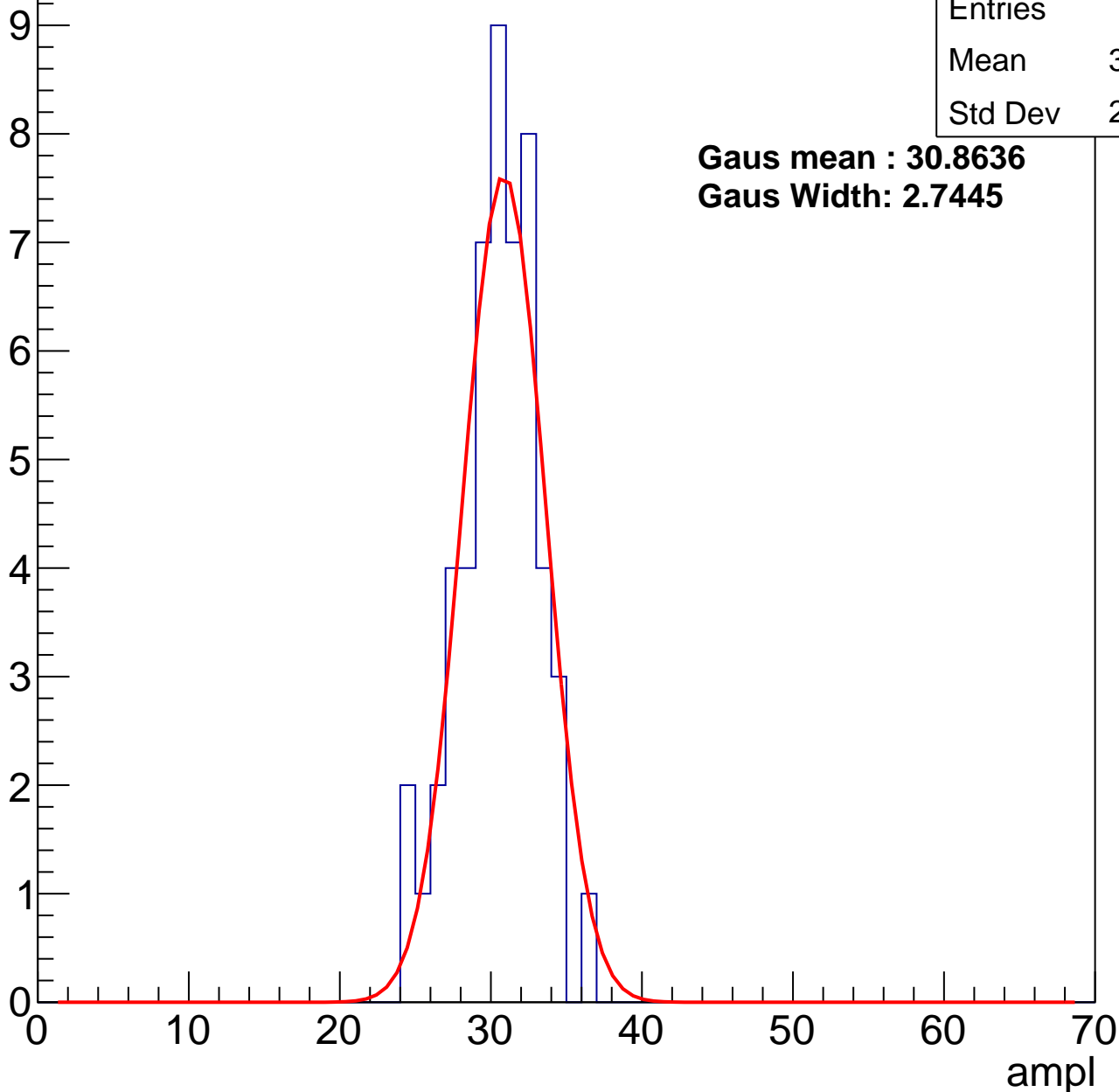
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	52
Mean	30.02
Std Dev	2.583

**Gaus mean : 30.8636**

**Gaus Width: 2.7445**



# B1L100S, U6-ch77, adc1

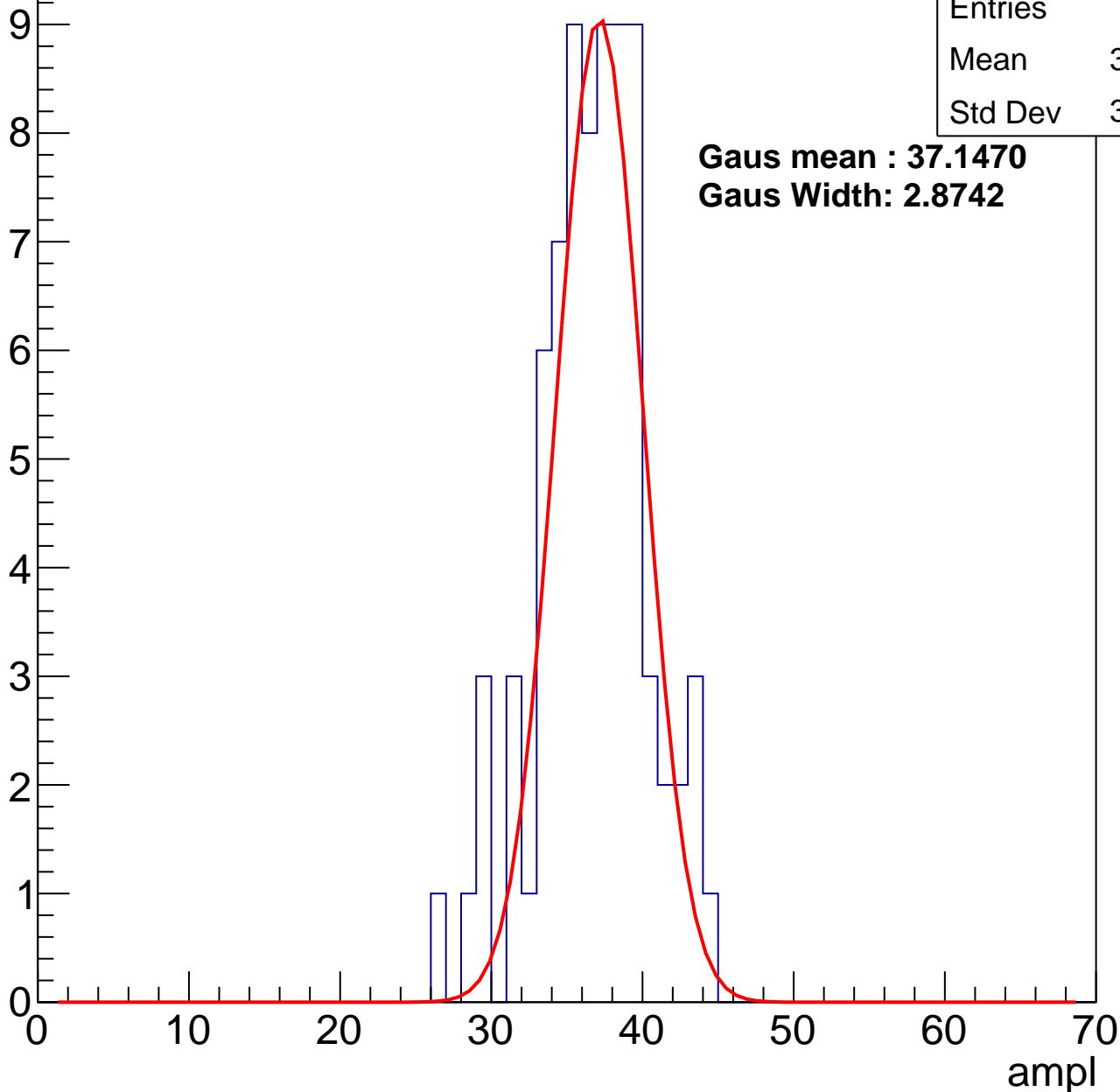
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	77
Mean	36.23
Std Dev	3.596

**Gaus mean : 37.1470**

**Gaus Width: 2.8742**



# B1L100S, U6-ch77, adc2

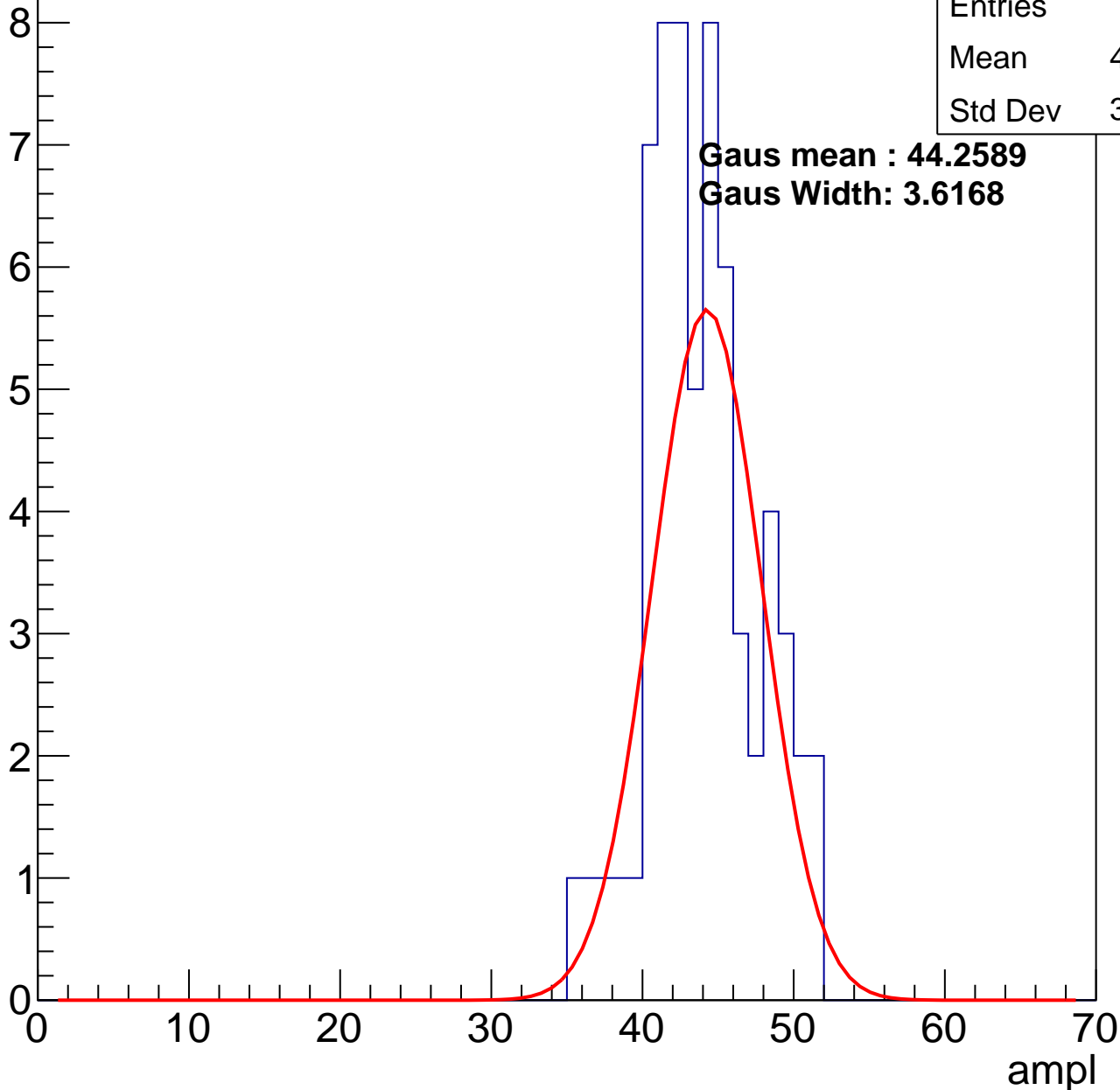
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	63
Mean	43.48
Std Dev	3.572

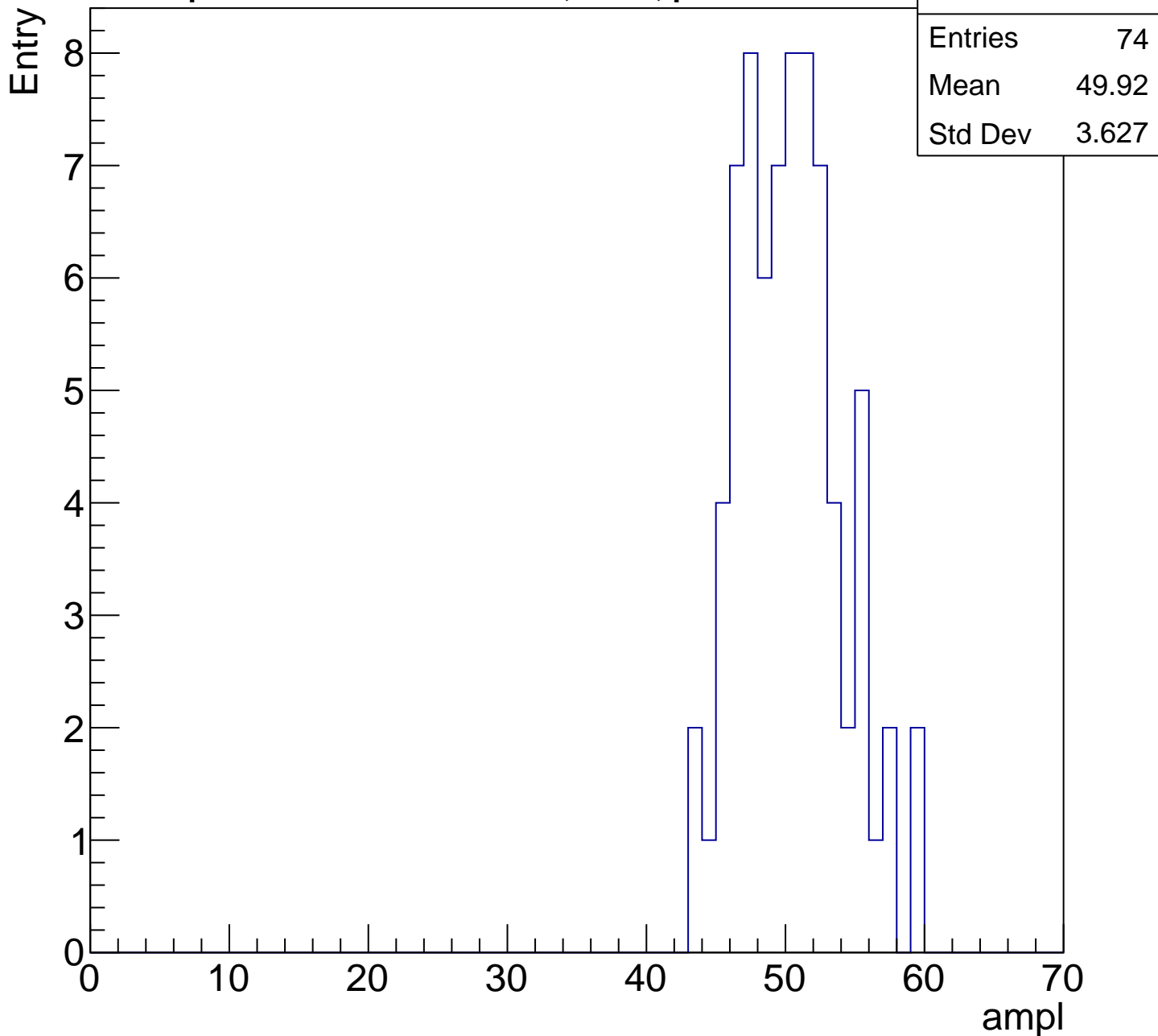
**Gaus mean : 44.2589**

**Gaus Width: 3.6168**



# B1L100S, U6-ch77, adc3

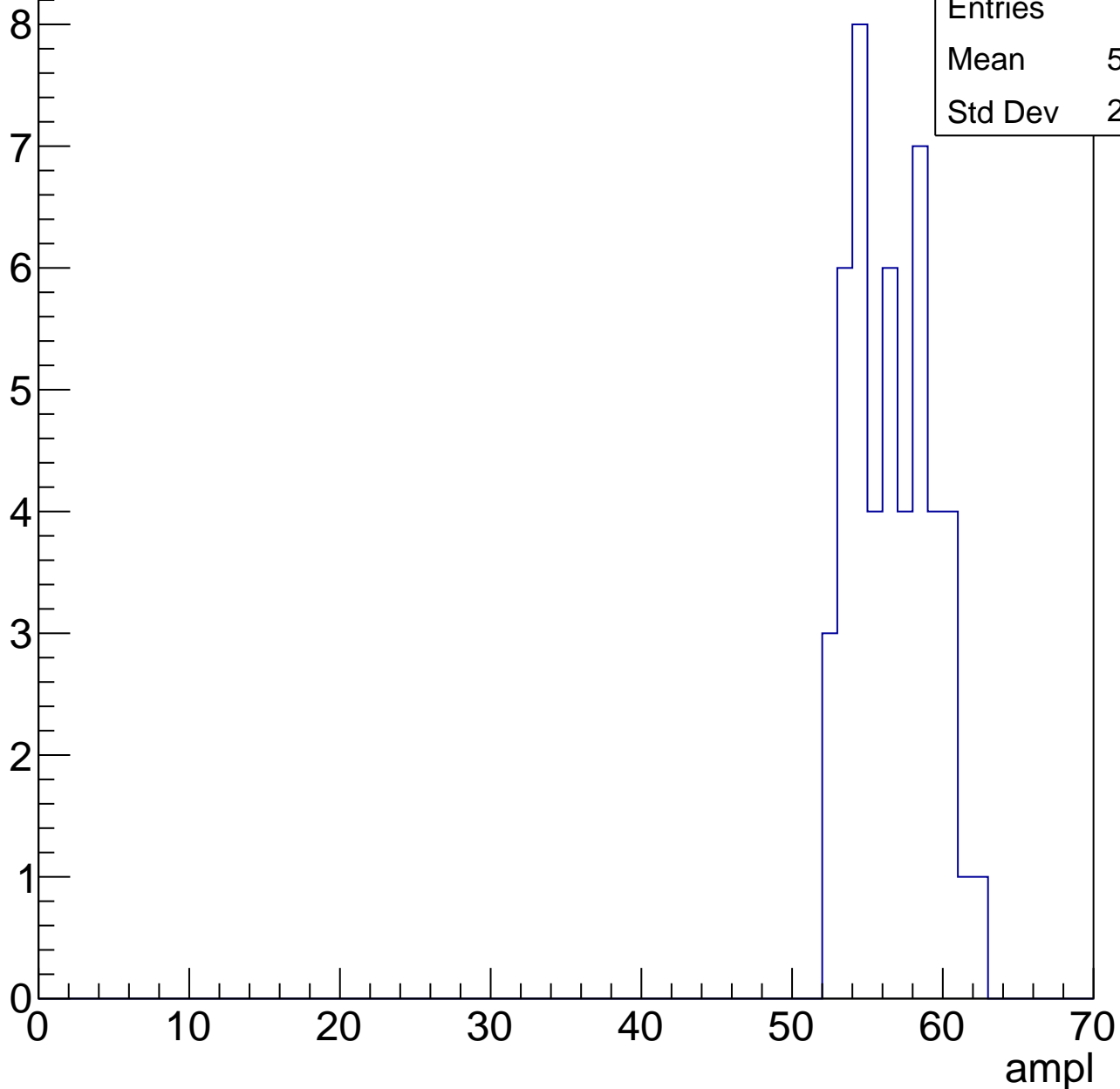
calib\_packv5\_042523\_0143.root, FC#4, port A2



# B1L100S, U6-ch77, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



# B1L100S, U6-ch77, adc5

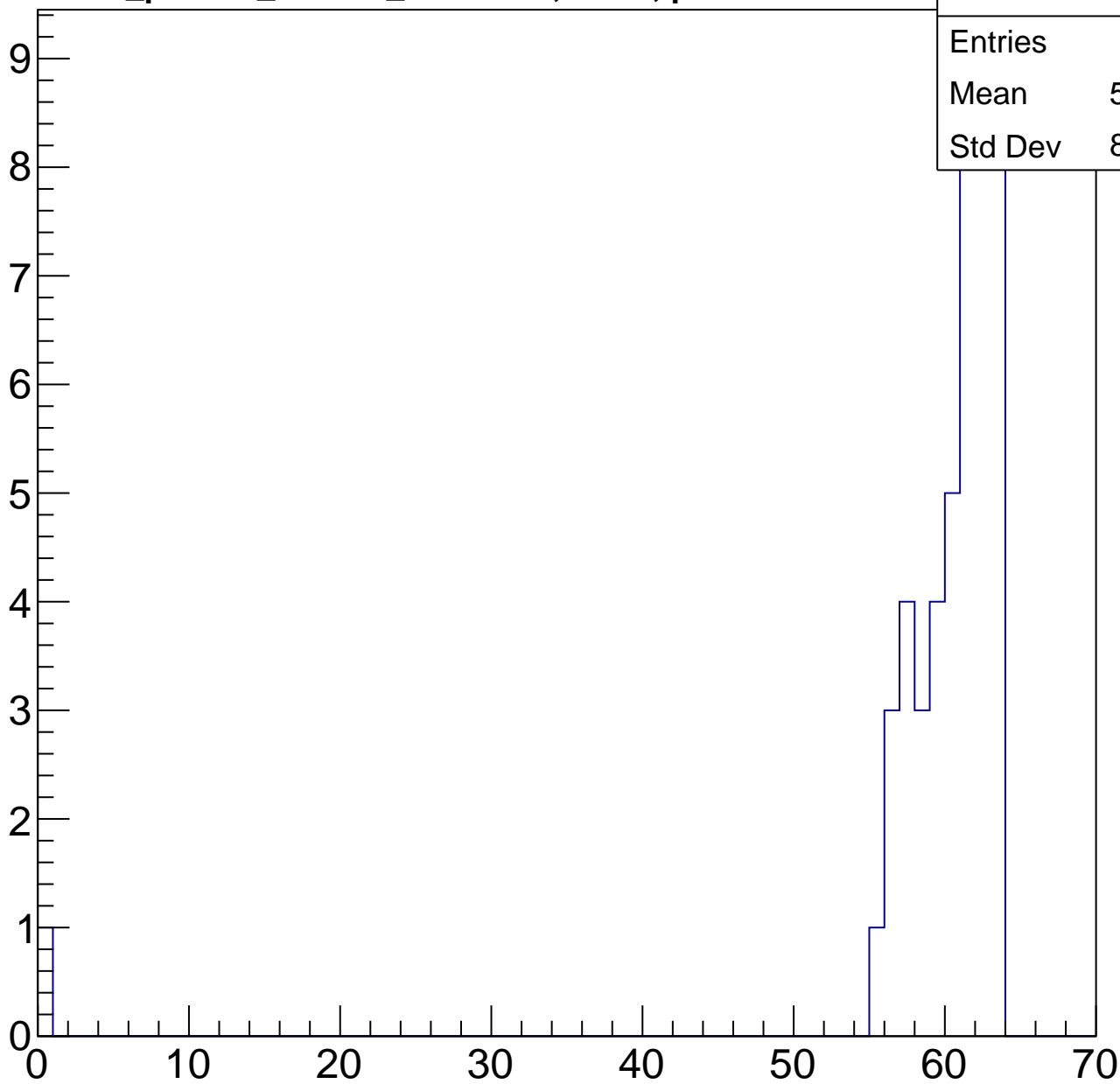
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	47
Mean	58.98
Std Dev	8.983

ampl



# B1L100S, U6-ch77, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

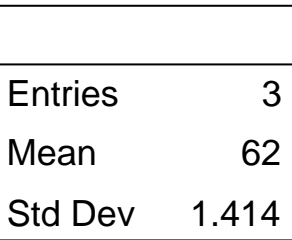
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	3
Mean	62
Std Dev	1.414

0 10 20 30 40 50 60 70

ampl





# B1L100S, U6-ch77, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L100S, U6-ch78, adc0

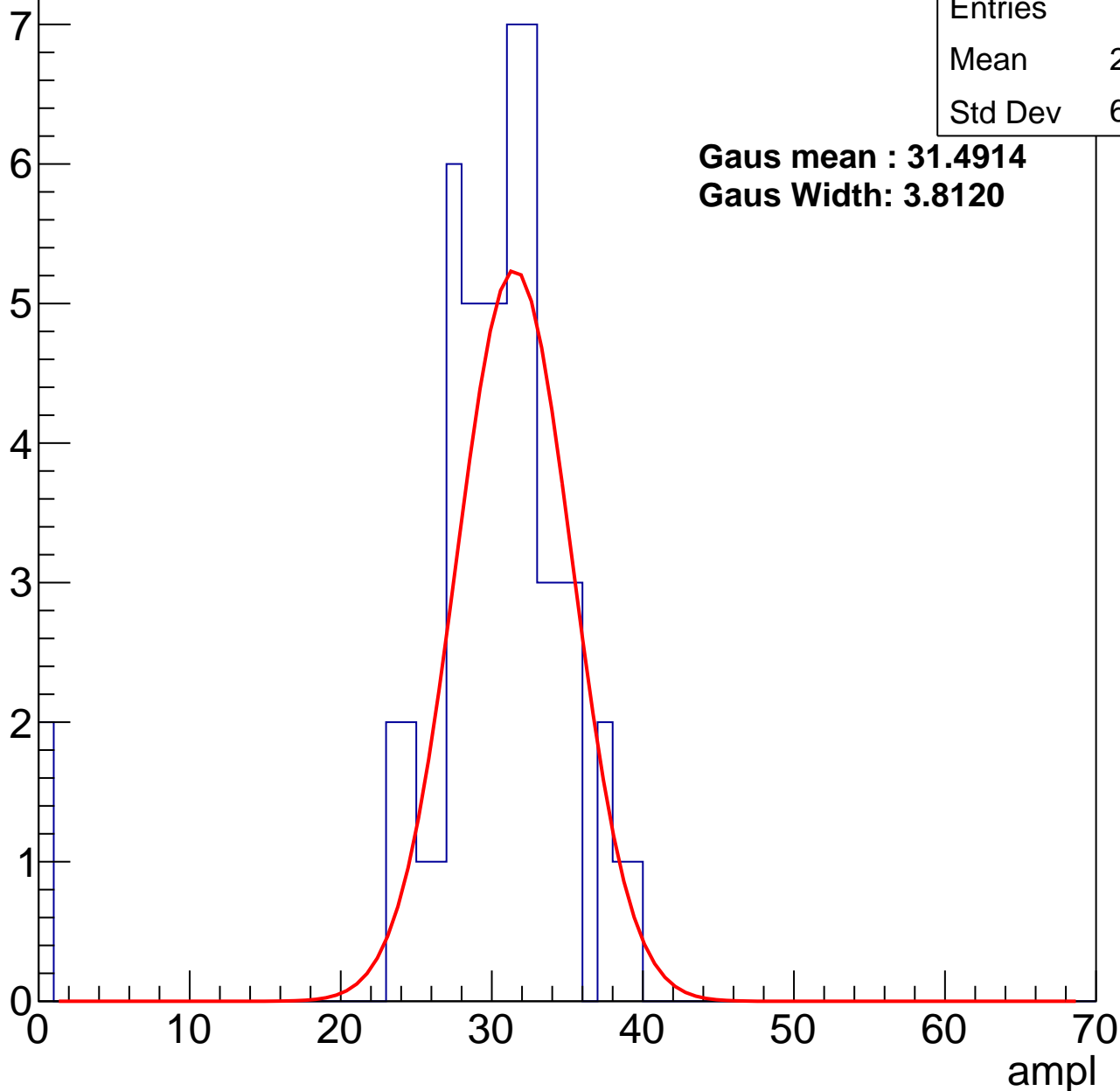
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	56
Mean	29.29
Std Dev	6.667

**Gaus mean : 31.4914**

**Gaus Width: 3.8120**



# B1L100S, U6-ch78, adc1

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	57
Mean	35.61
Std Dev	3.144

**Gaus mean : 35.8549**

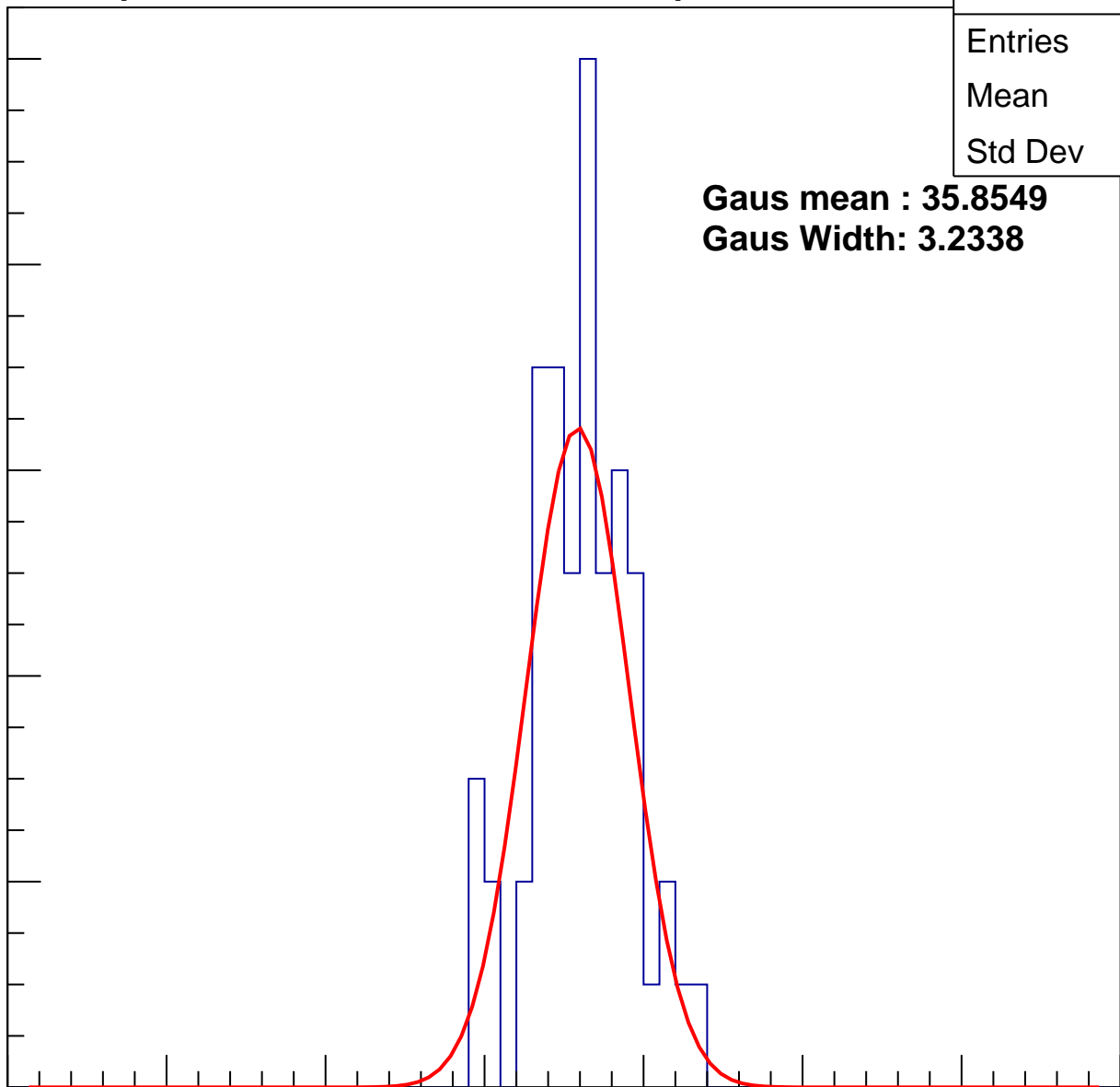
**Gaus Width: 3.2338**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B1L100S, U6-ch78, adc2

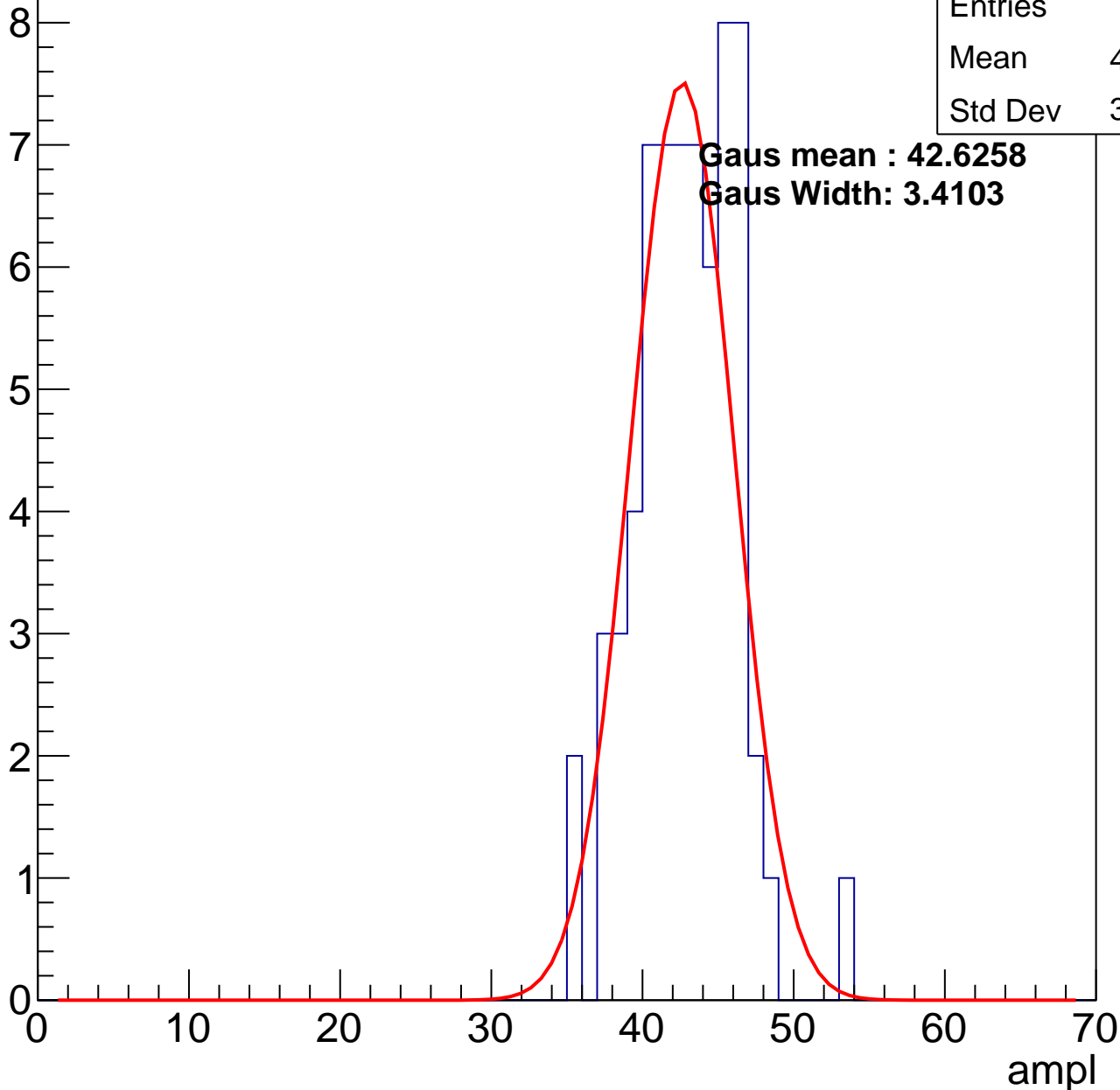
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	66
Mean	42.42
Std Dev	3.299

**Gaus mean : 42.6258**

**Gaus Width: 3.4103**

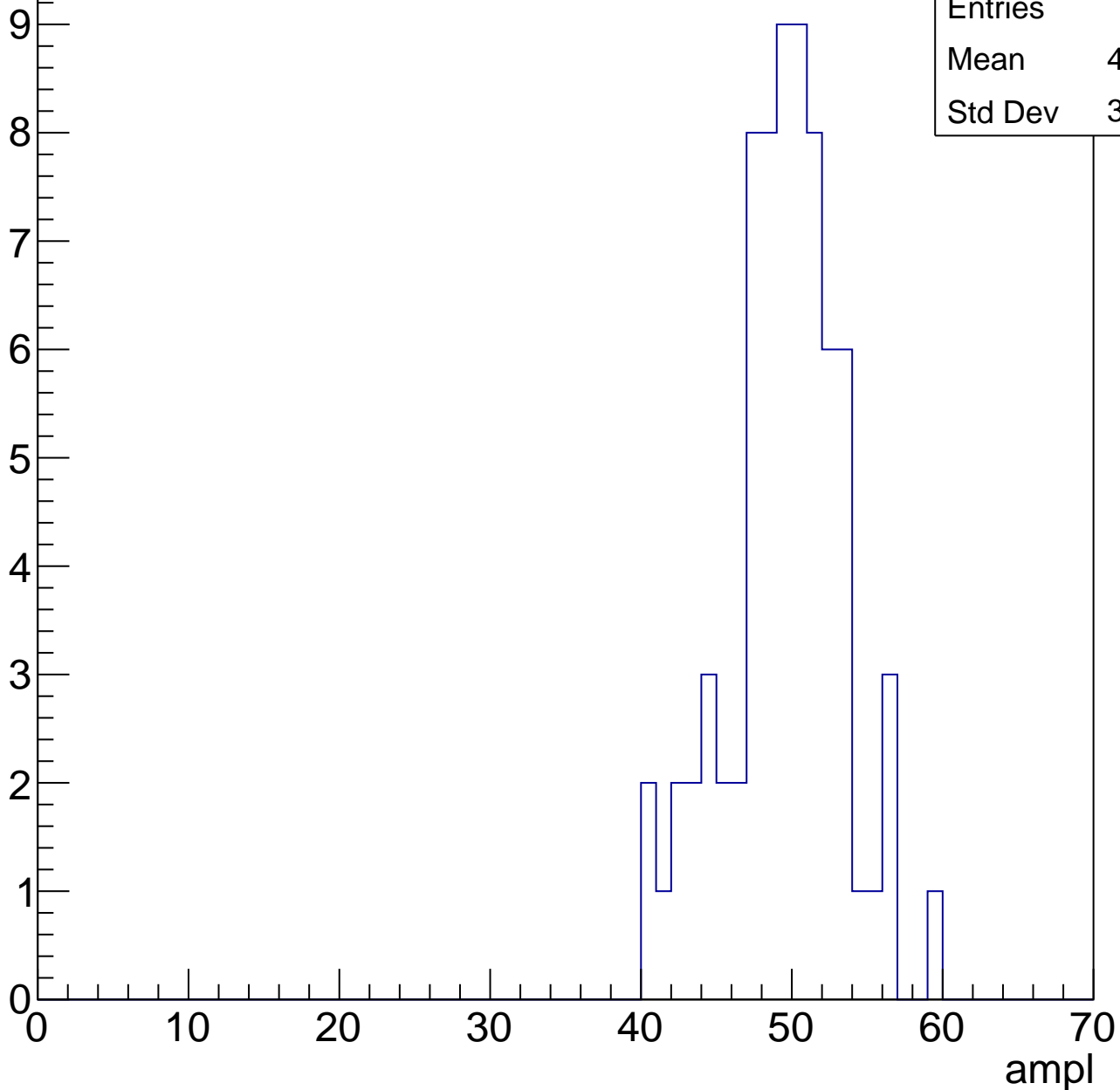


# B1L100S, U6-ch78, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	74
Mean	49.05
Std Dev	3.784

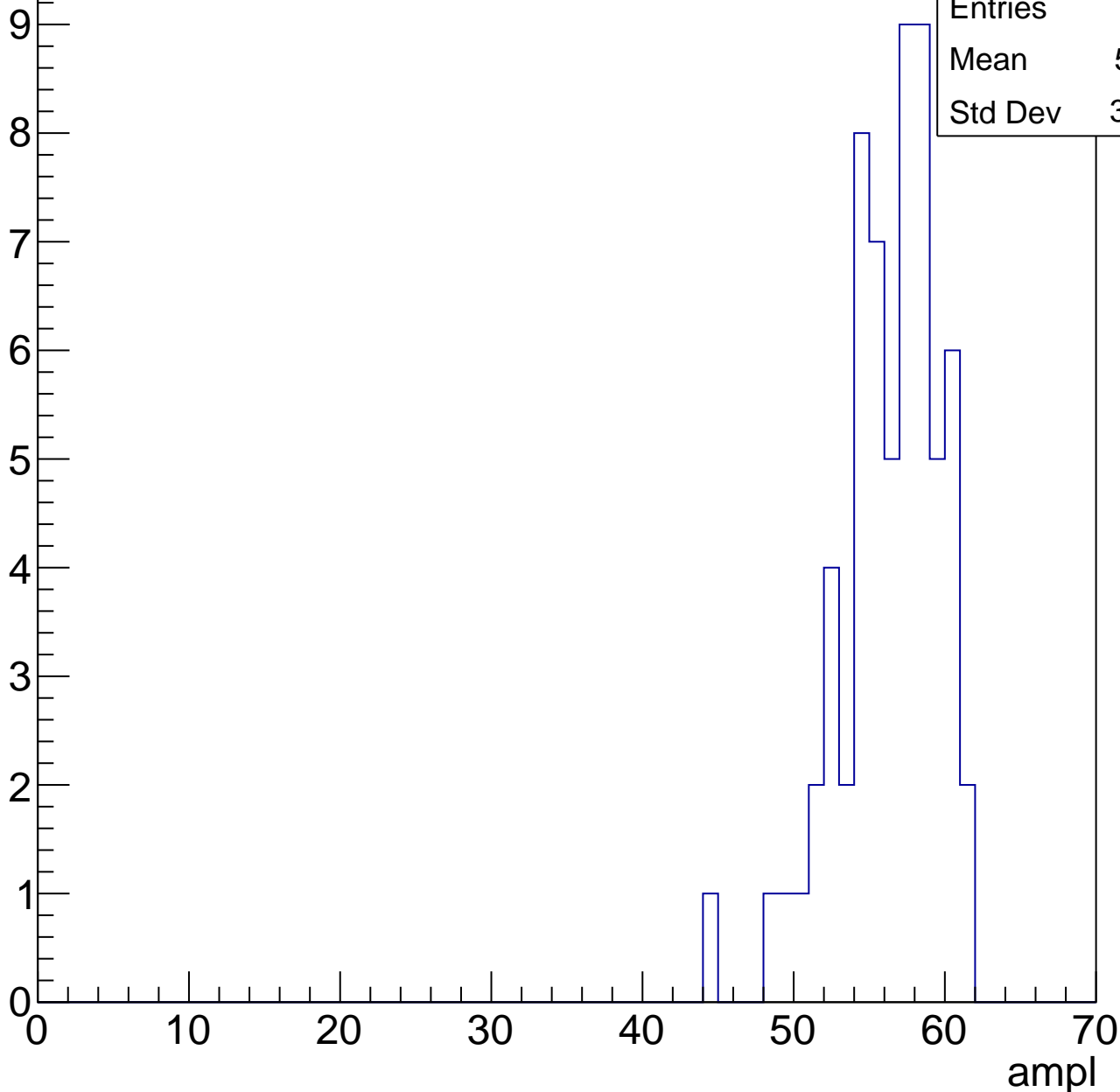


# B1L100S, U6-ch78, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	63
Mean	55.81
Std Dev	3.328

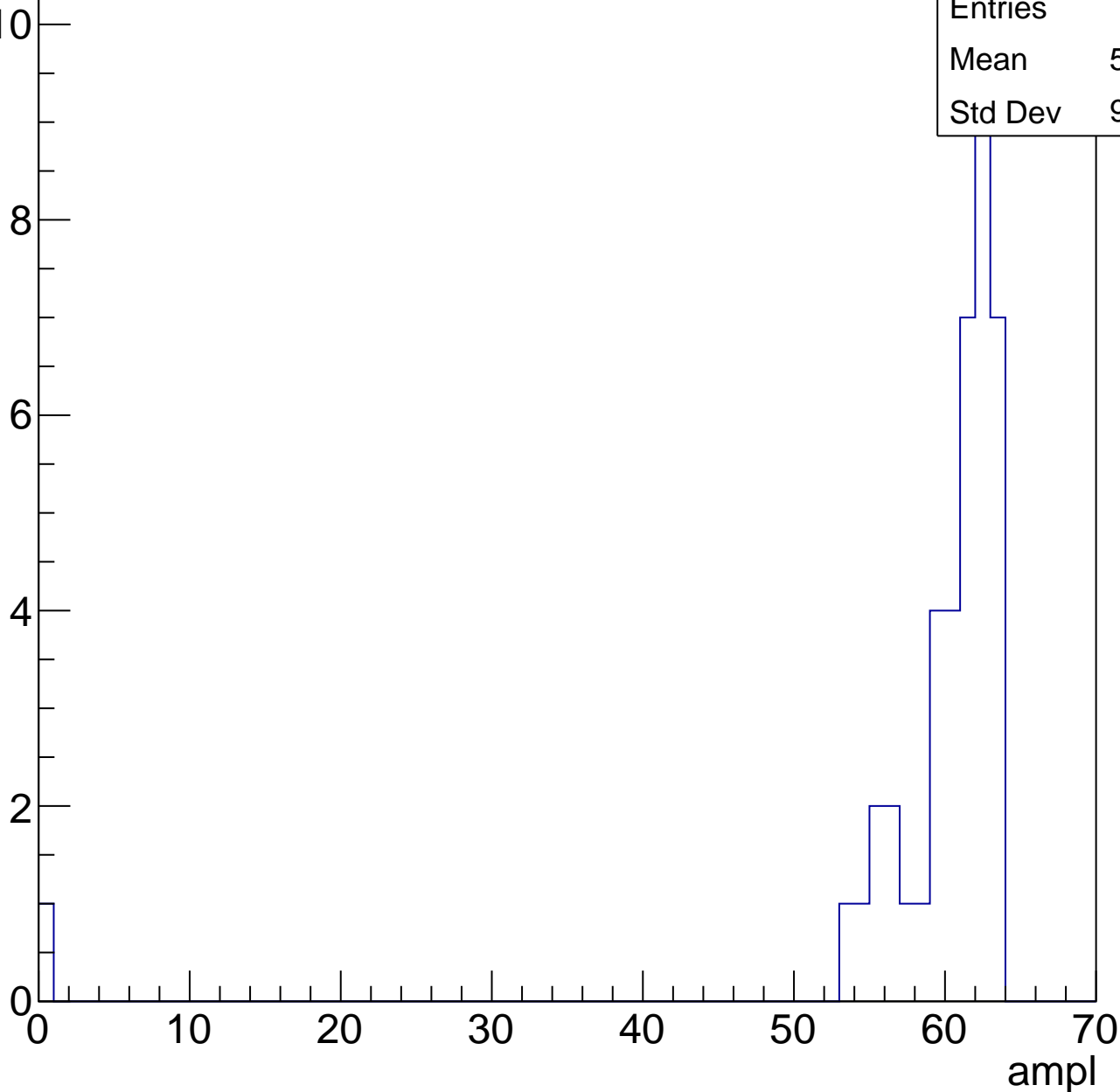


# B1L100S, U6-ch78, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	41
Mean	58.73
Std Dev	9.663



# B1L100S, U6-ch78, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry





# B1L100S, U6-ch78, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	3
Mean	0
Std Dev	0

# B1L100S, U6-ch79, adc0

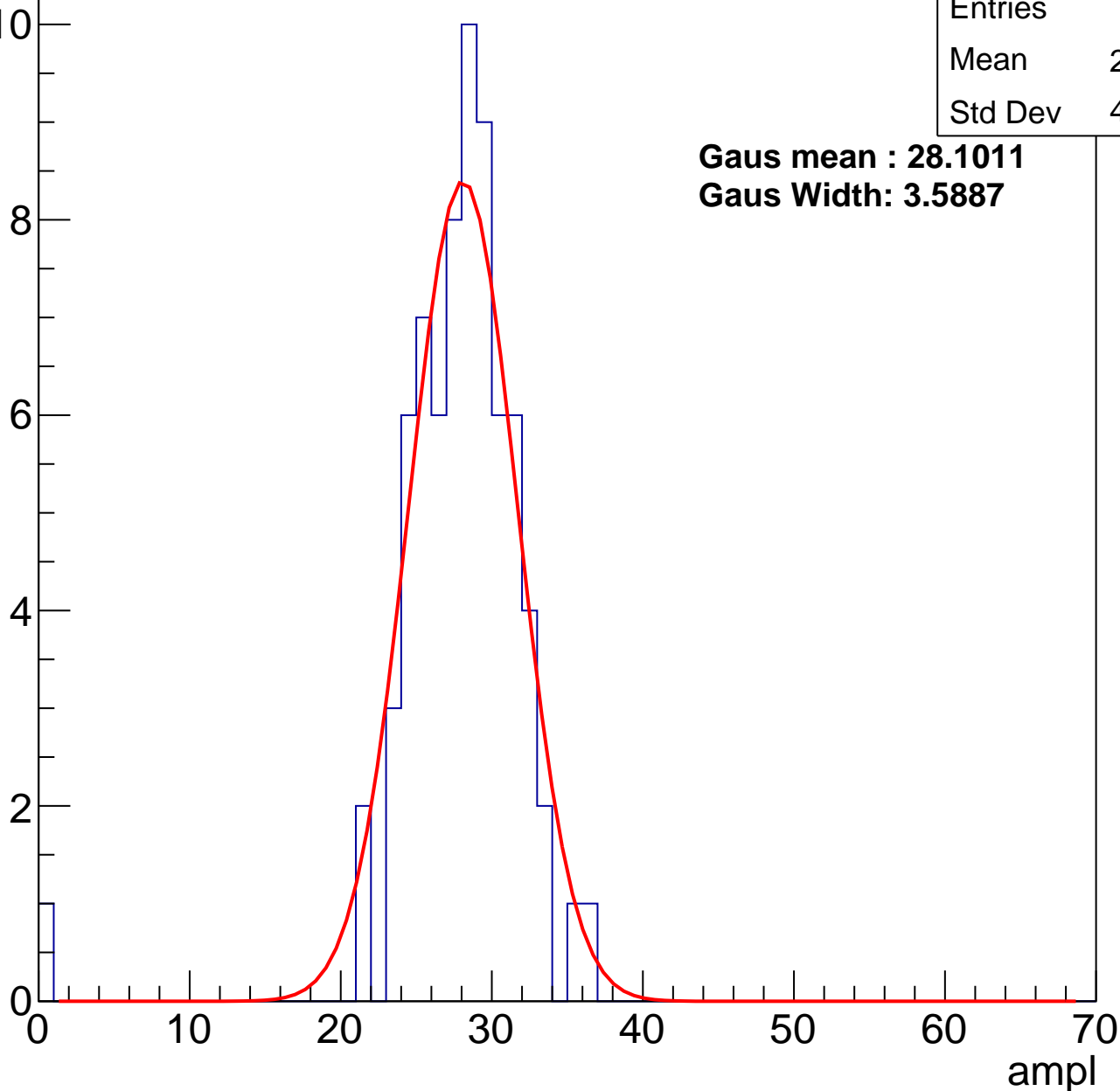
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	72
Mean	27.42
Std Dev	4.468

**Gaus mean : 28.1011**

**Gaus Width: 3.5887**



# B1L100S, U6-ch79, adc1

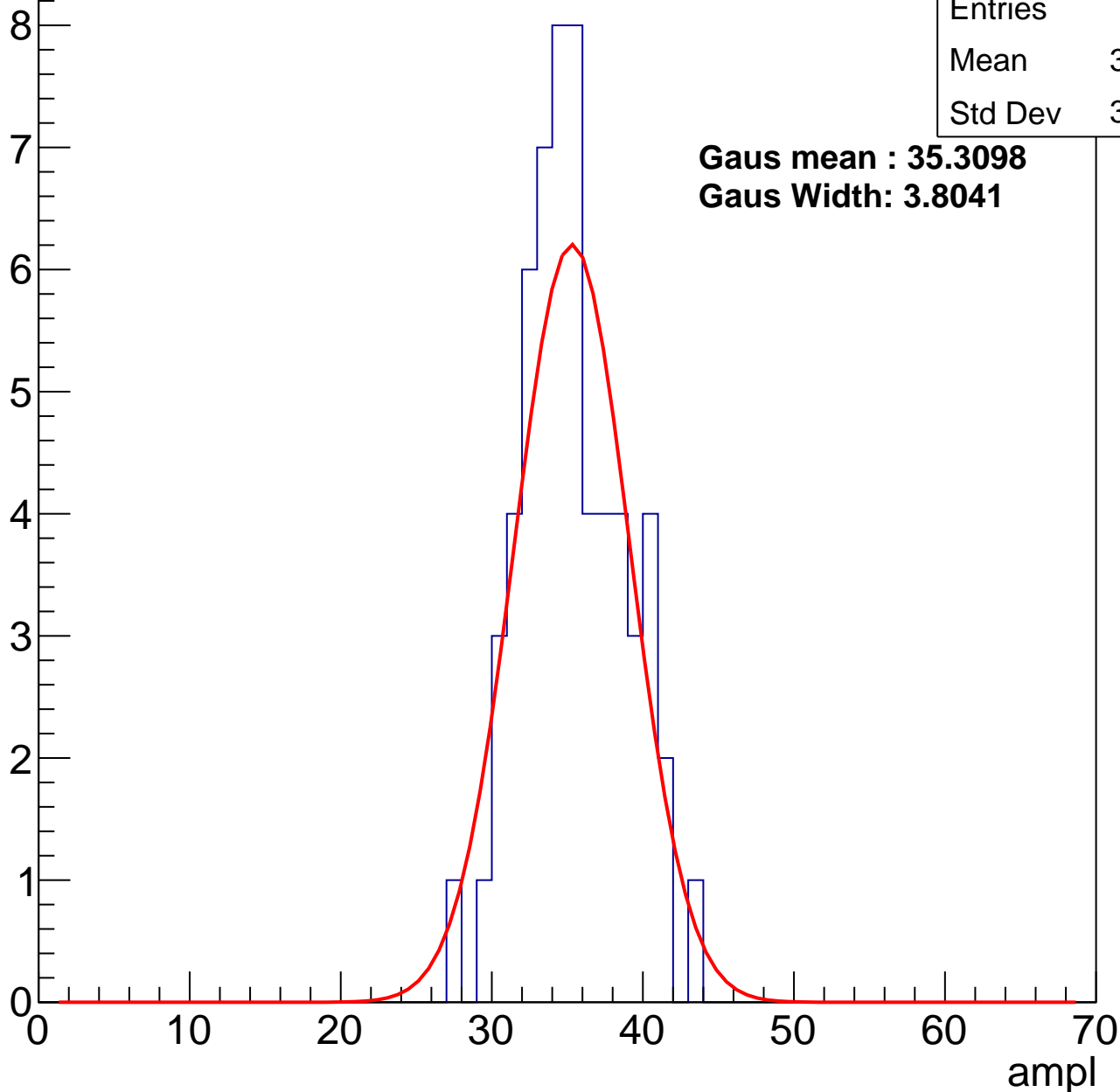
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	60
Mean	34.85
Std Dev	3.336

**Gaus mean : 35.3098**

**Gaus Width: 3.8041**



# B1L100S, U6-ch79, adc2

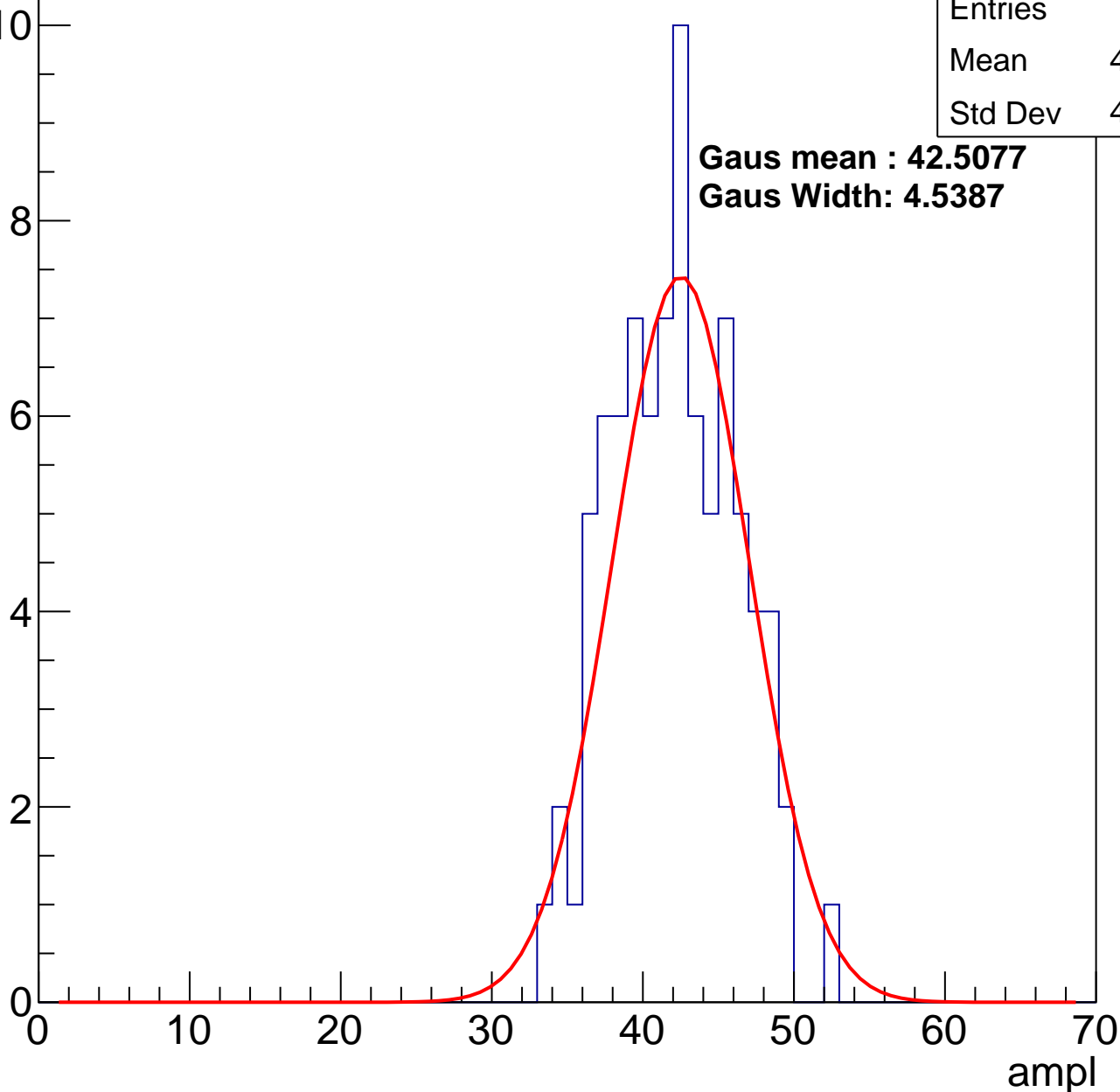
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	85
Mean	41.64
Std Dev	4.026

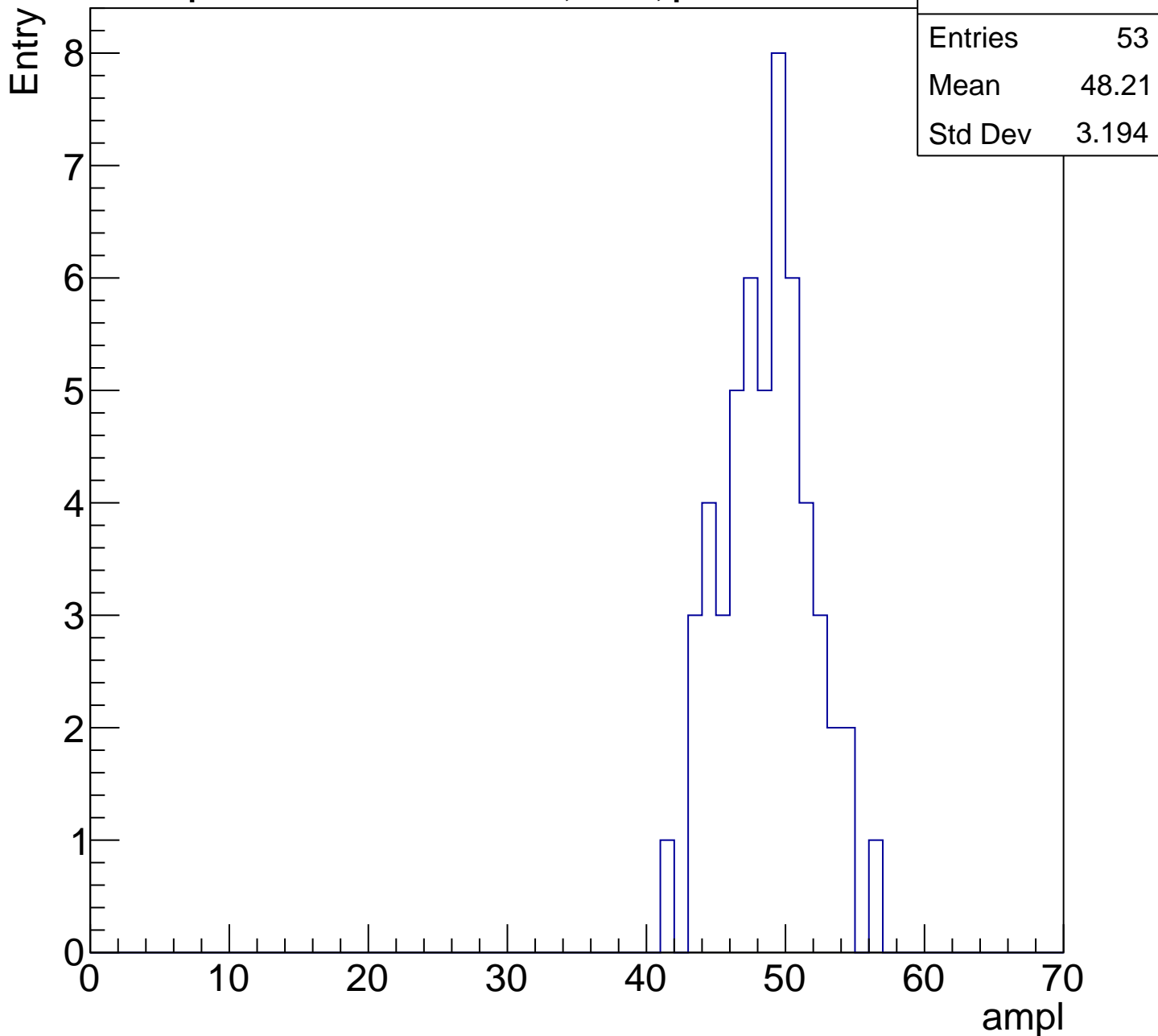
**Gaus mean : 42.5077**

**Gaus Width: 4.5387**



# B1L100S, U6-ch79, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

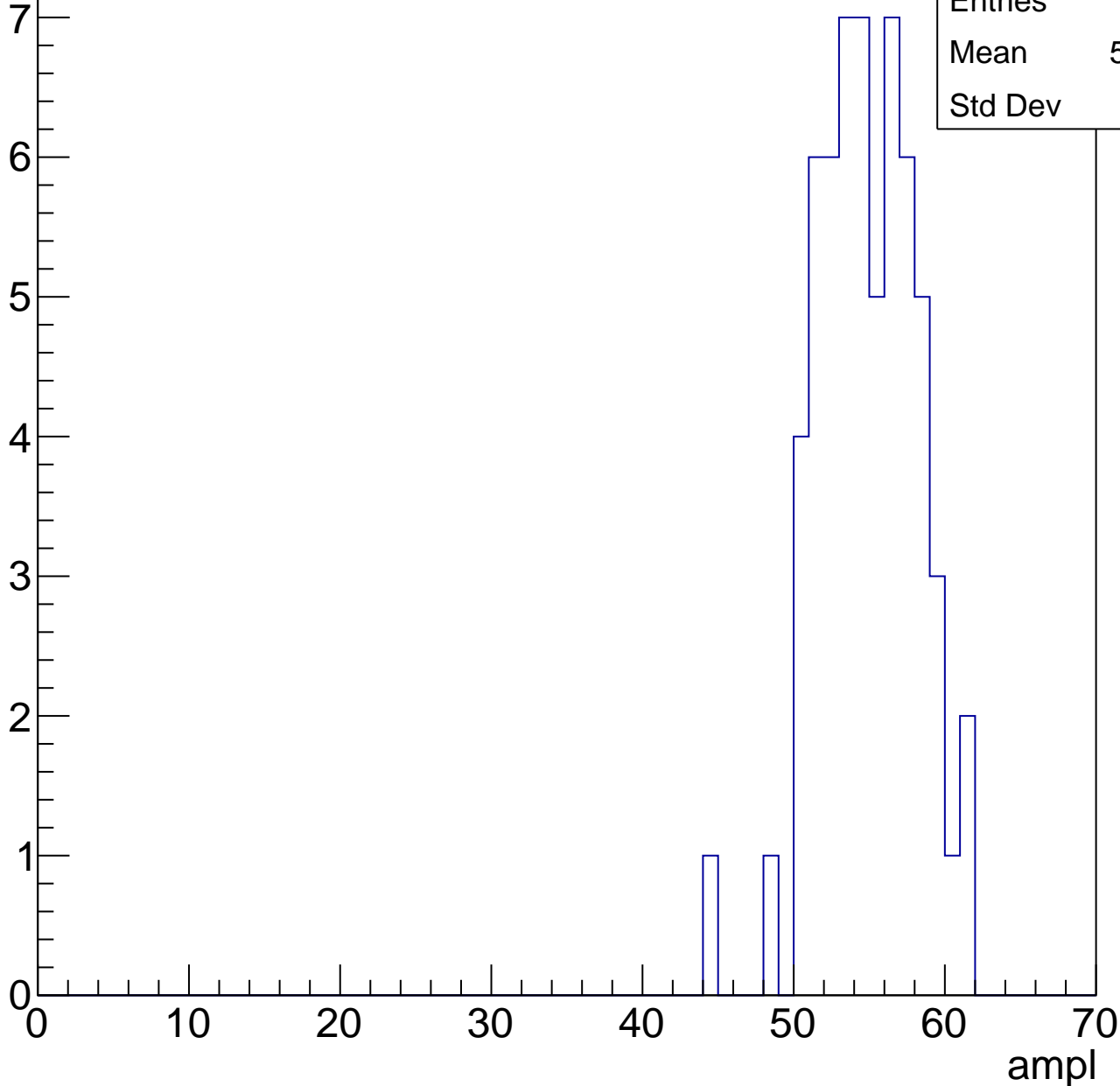


# B1L100S, U6-ch79, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	61
Mean	54.38
Std Dev	3.27



# B1L100S, U6-ch79, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	60
Mean	58.58
Std Dev	8.063

ampl

0 10 20 30 40 50 60 70

0

1

2

3

4

5

6

7

8

9

# B1L100S, U6-ch79, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	3
Mean	62.67
Std Dev	0.4714

ampl

0 10 20 30 40 50 60 70



# B1L100S, U6-ch79, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



# B1L100S, U6-ch80, adc0

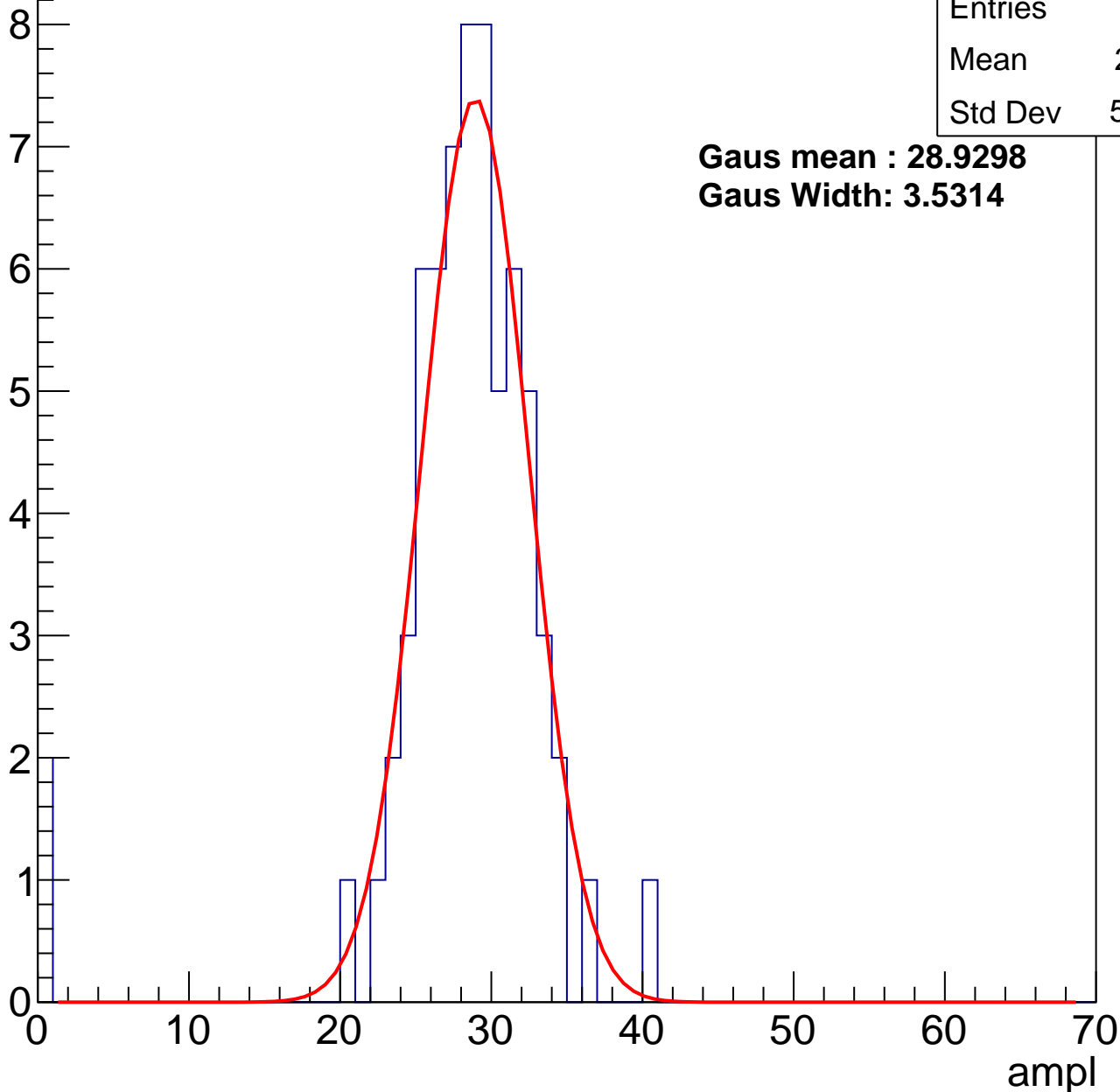
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	67
Mean	27.61
Std Dev	5.932

**Gaus mean : 28.9298**

**Gaus Width: 3.5314**



# B1L100S, U6-ch80, adc1

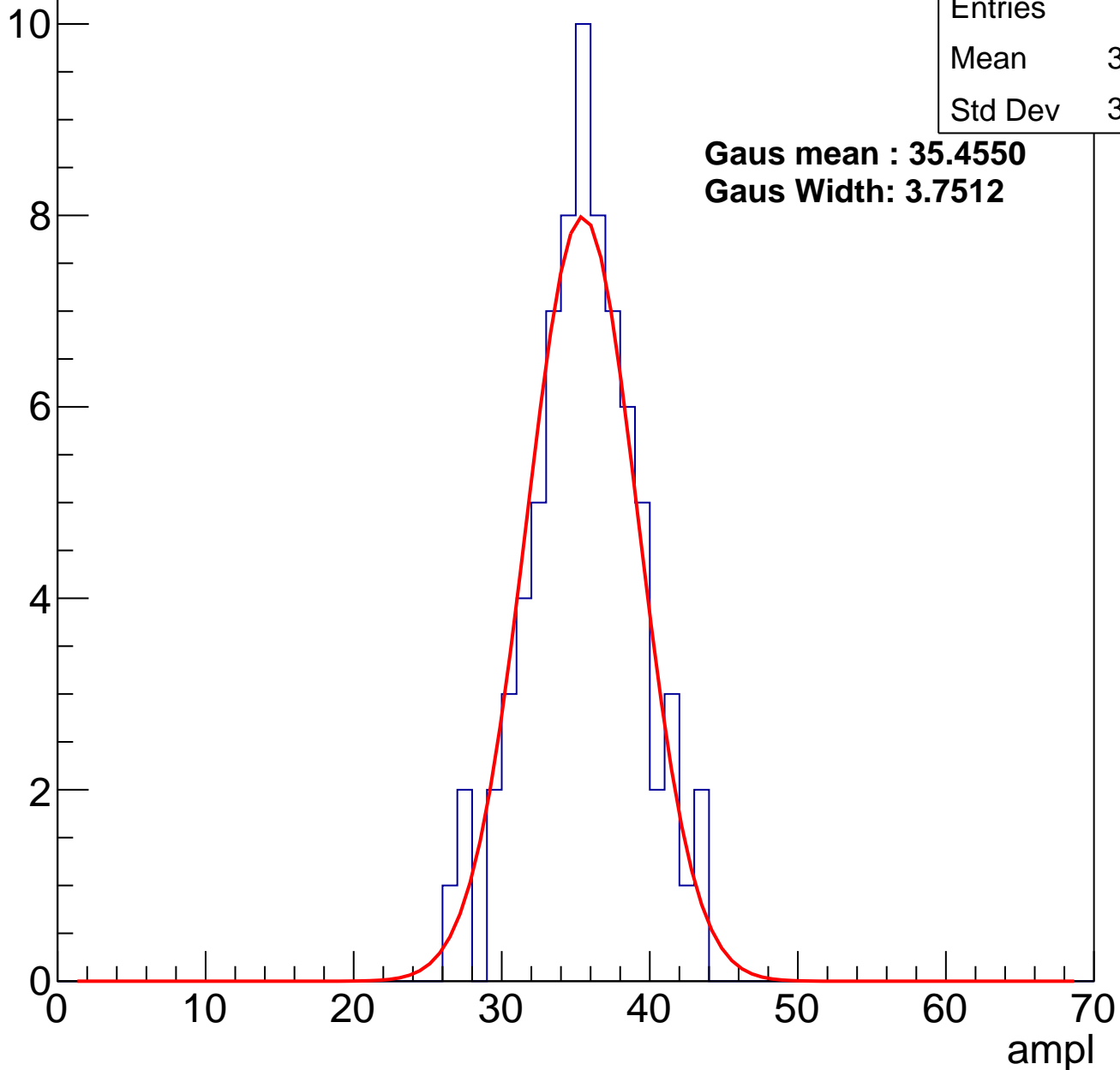
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	76
Mean	35.08
Std Dev	3.637

**Gaus mean : 35.4550**

**Gaus Width: 3.7512**

Entry



# B1L100S, U6-ch80, adc2

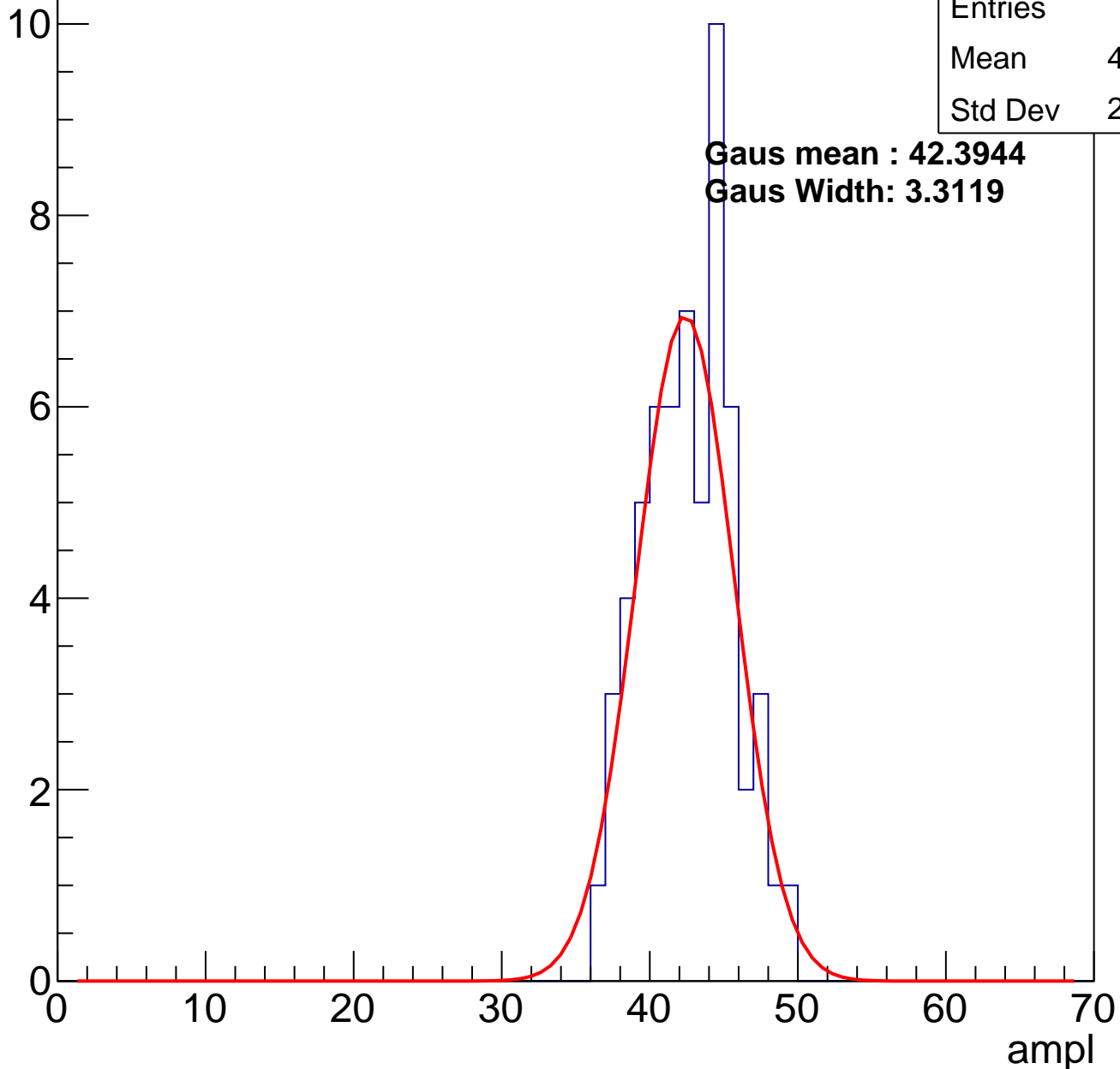
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	60
Mean	42.15
Std Dev	2.999

**Gaus mean : 42.3944**

**Gaus Width: 3.3119**

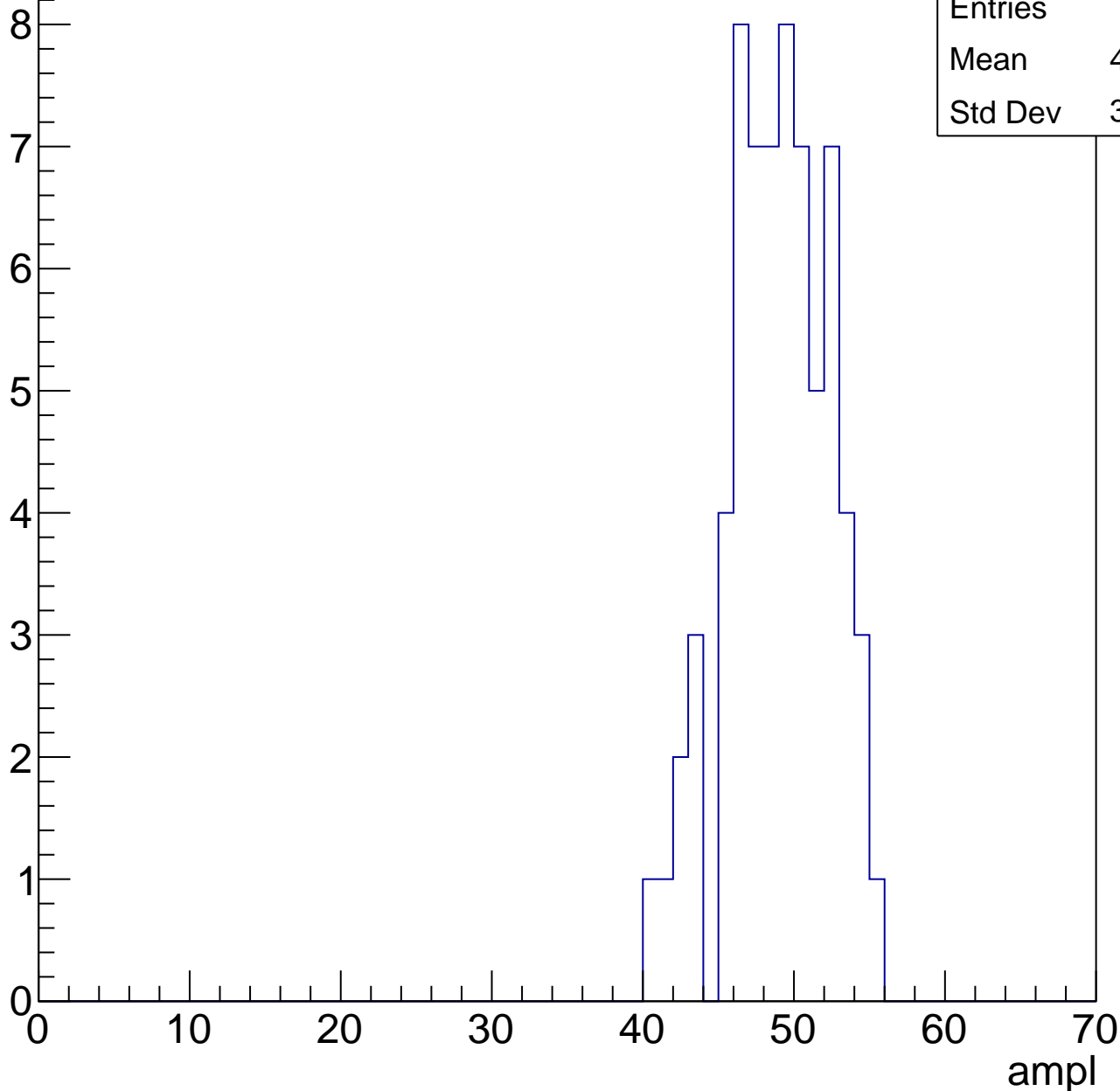
Entry



# B1L100S, U6-ch80, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

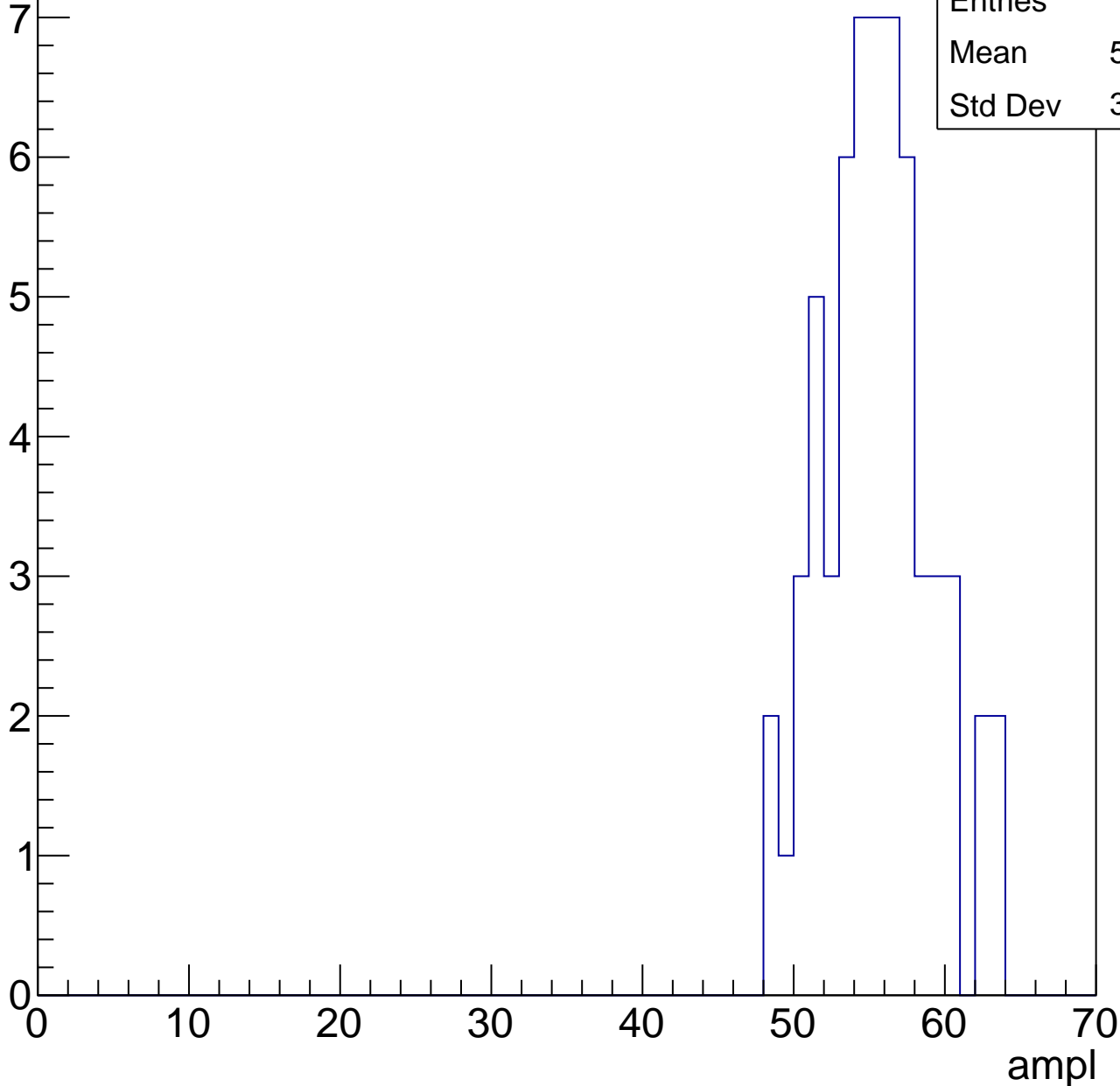


# B1L100S, U6-ch80, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	60
Mean	55.03
Std Dev	3.545

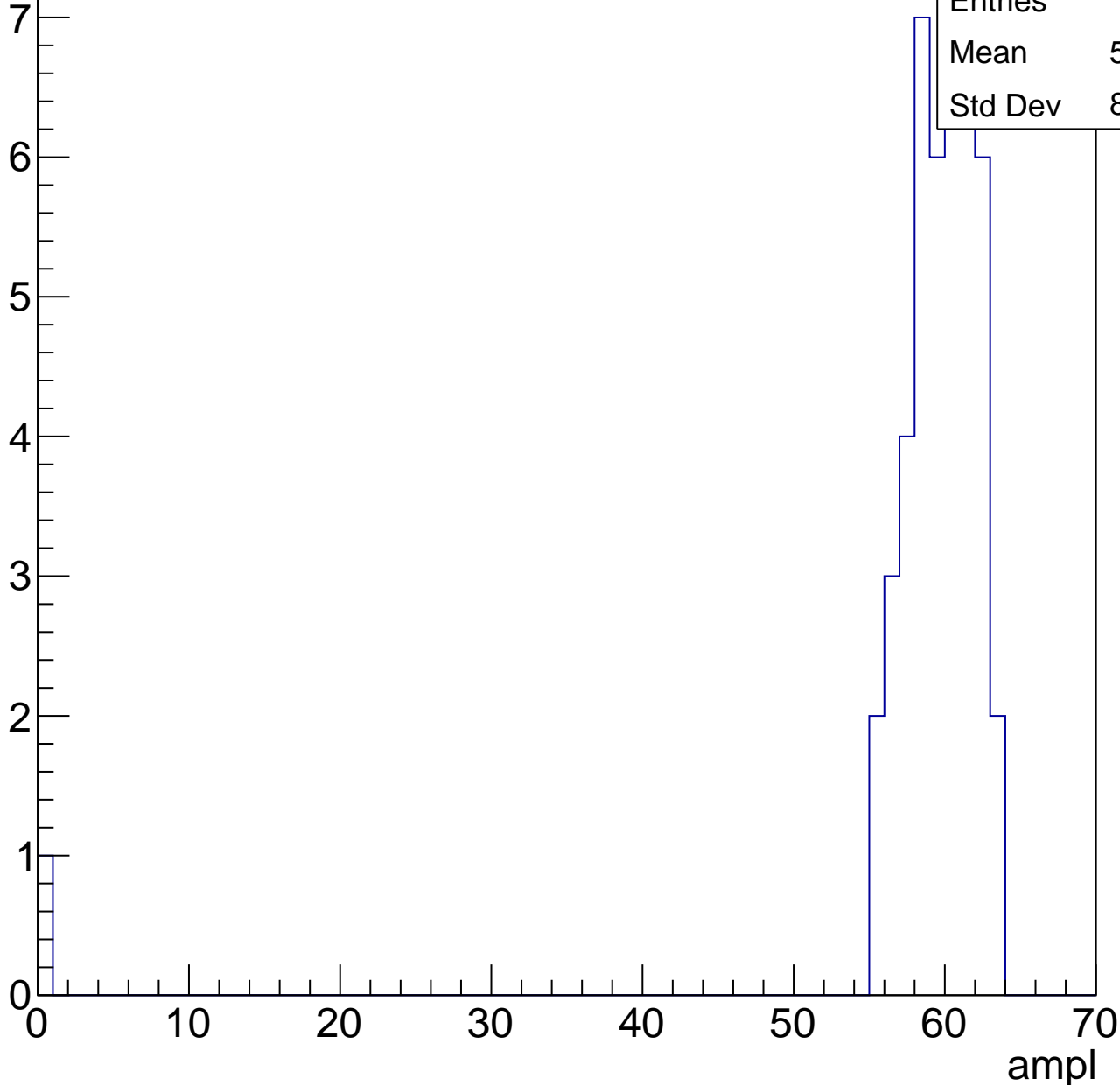


# B1L100S, U6-ch80, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	45
Mean	58.02
Std Dev	8.995

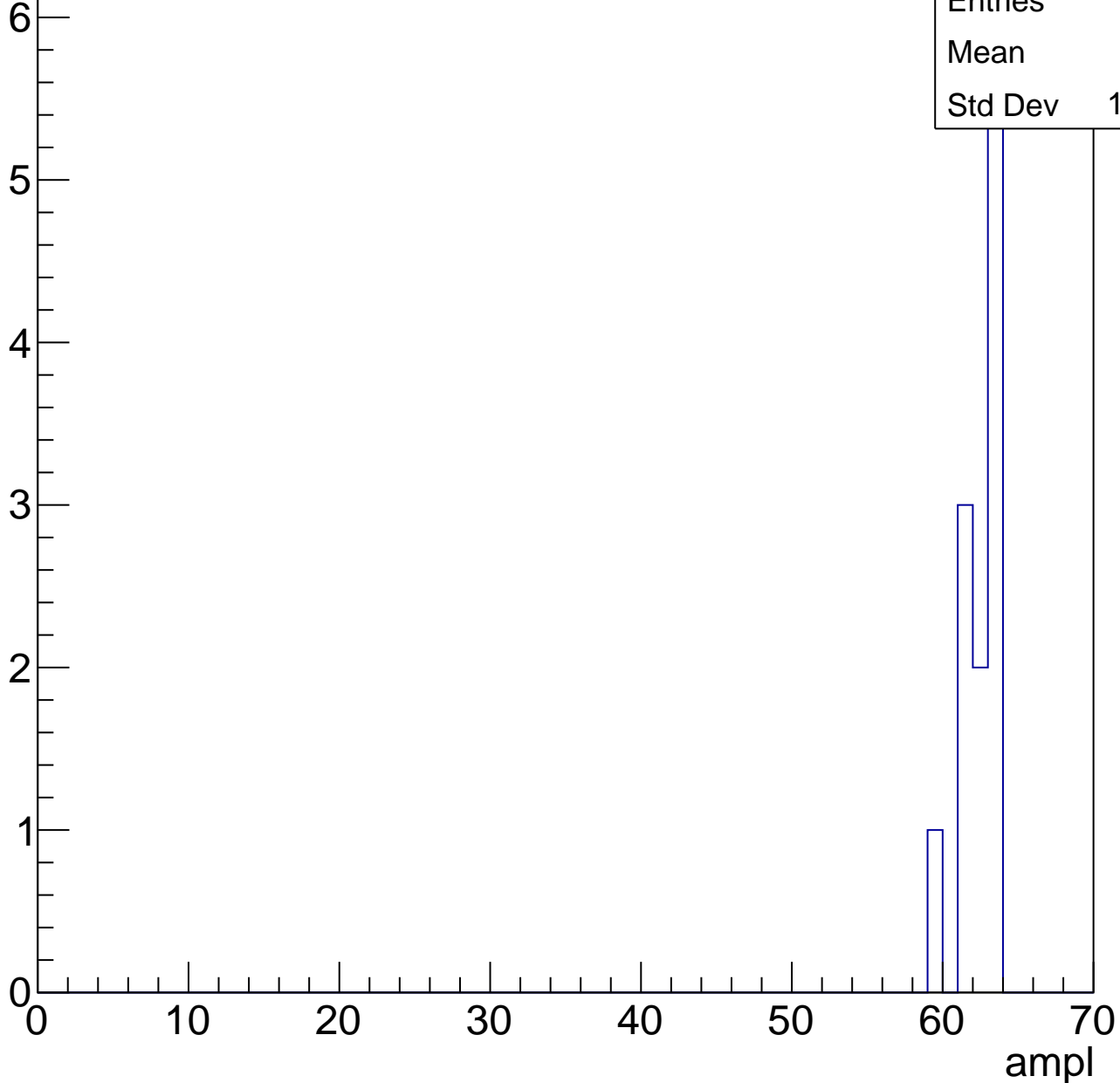


# B1L100S, U6-ch80, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	12
Mean	62
Std Dev	1.225





# B1L100S, U6-ch80, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



# B1L100S, U6-ch81, adc0

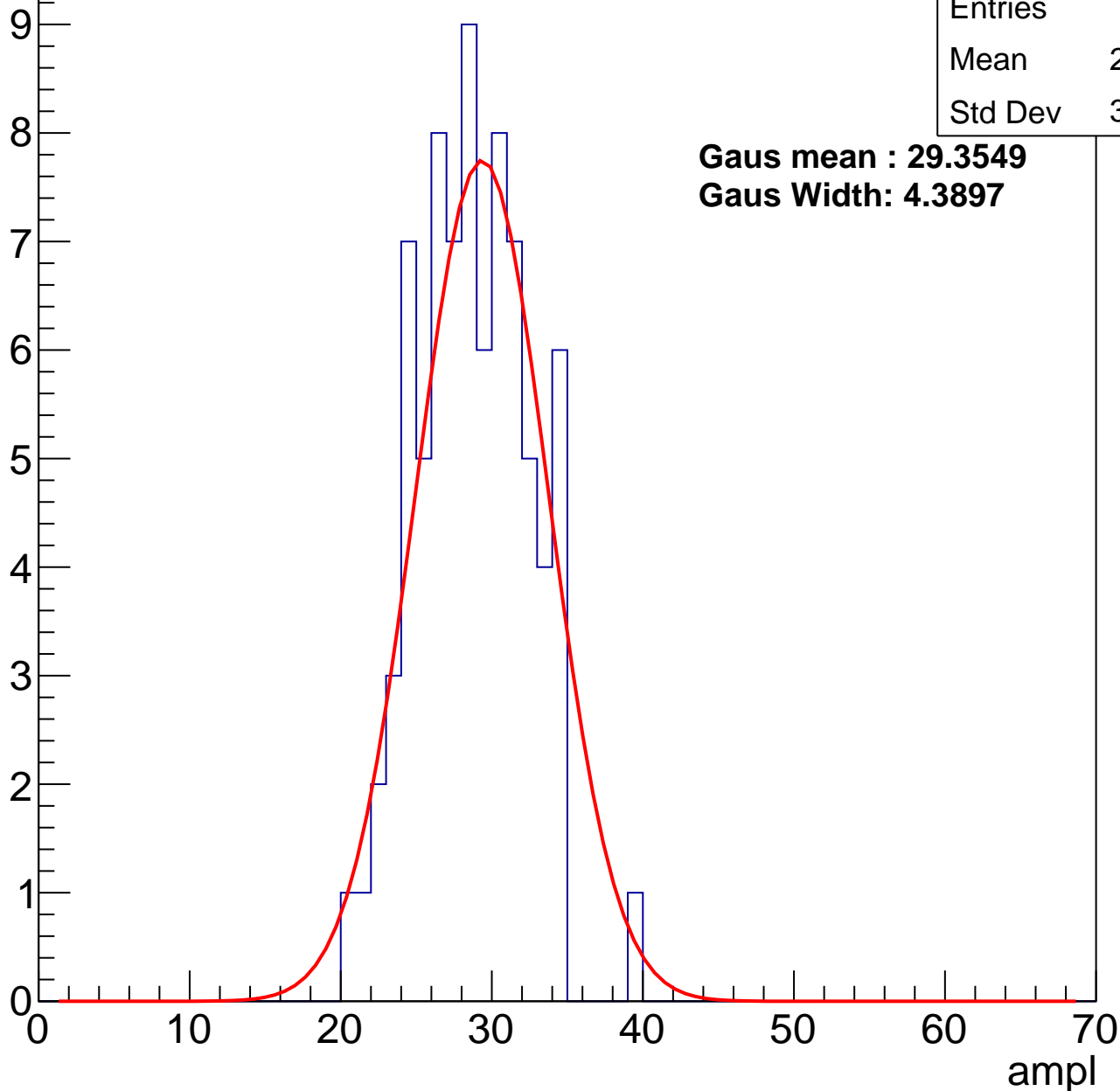
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	80
Mean	28.27
Std Dev	3.654

**Gaus mean : 29.3549**

**Gaus Width: 4.3897**



# B1L100S, U6-ch81, adc1

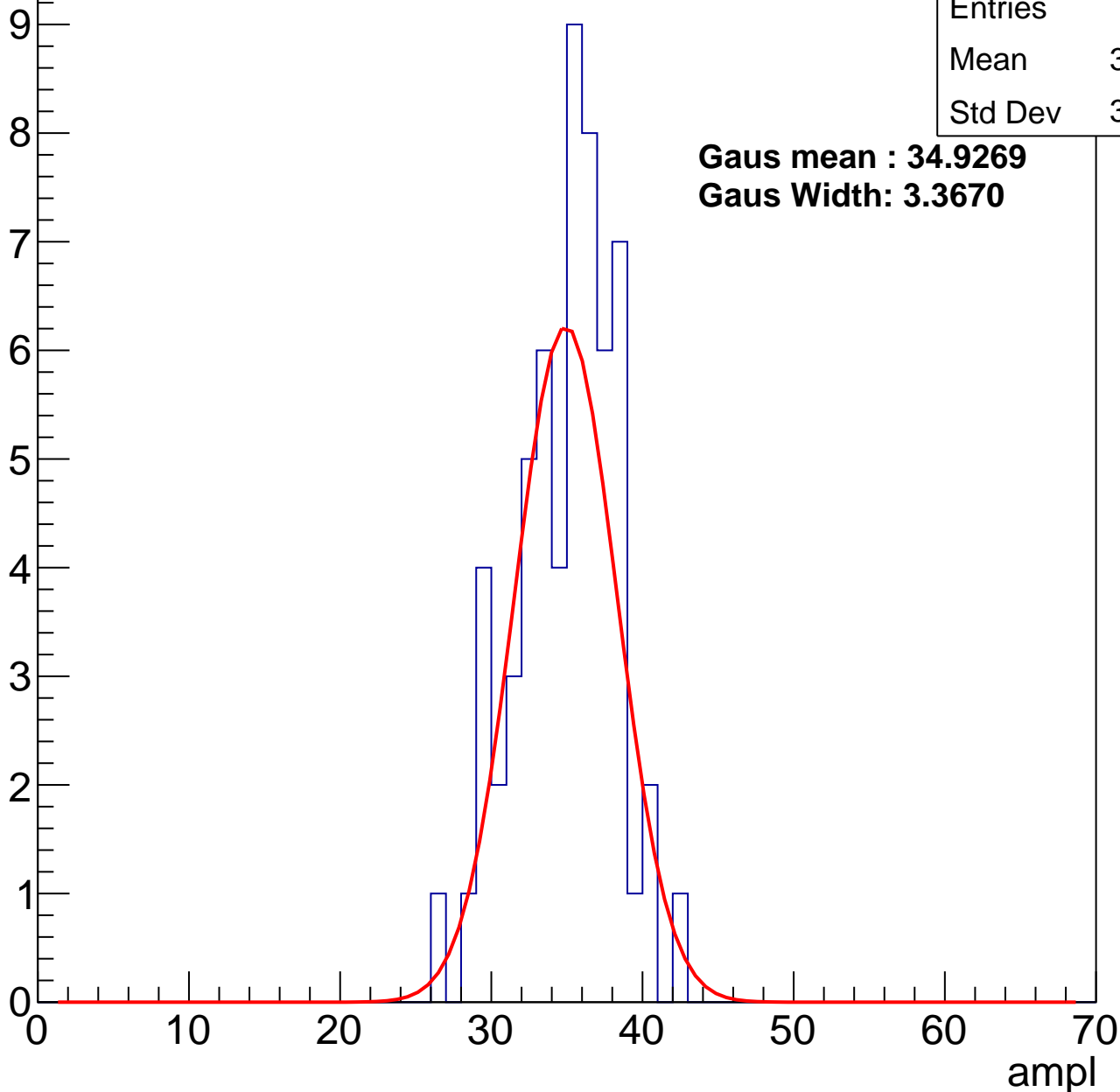
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	60
Mean	34.48
Std Dev	3.263

**Gaus mean : 34.9269**

**Gaus Width: 3.3670**



# B1L100S, U6-ch81, adc2

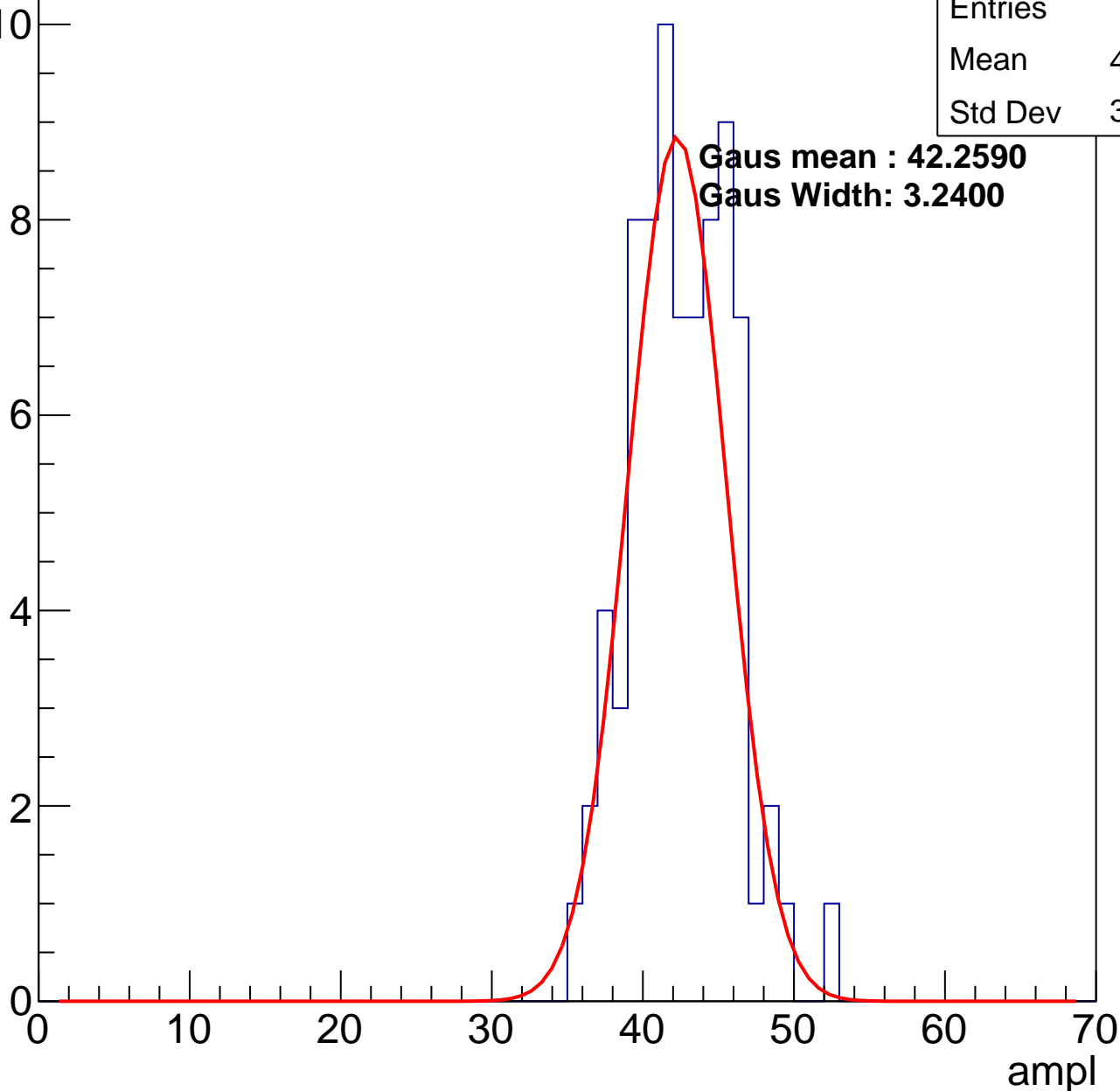
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	79
Mean	42.14
Std Dev	3.298

**Gaus mean : 42.2590**

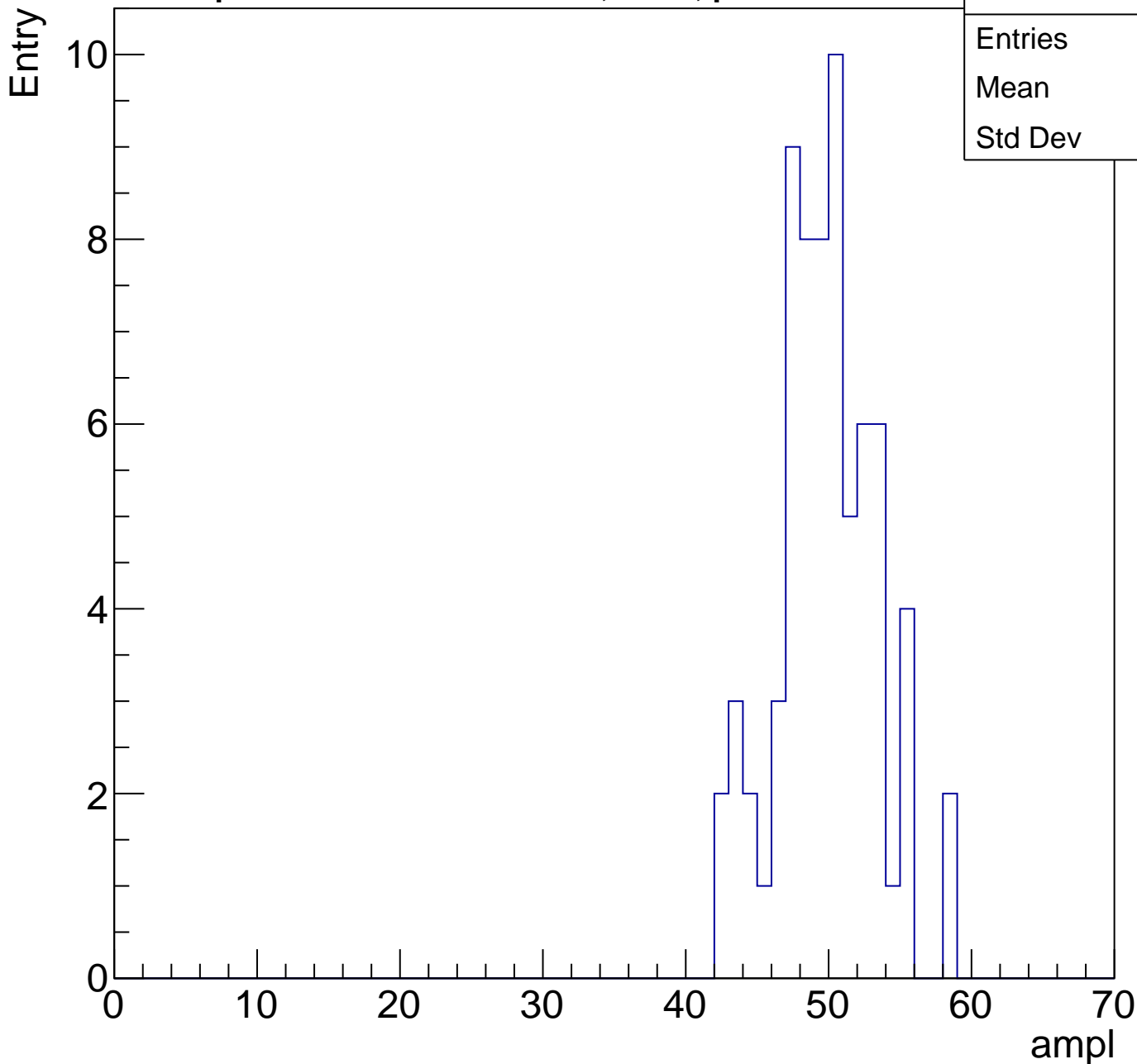
**Gaus Width: 3.2400**



# B1L100S, U6-ch81, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	70
Mean	49.4
Std Dev	3.47

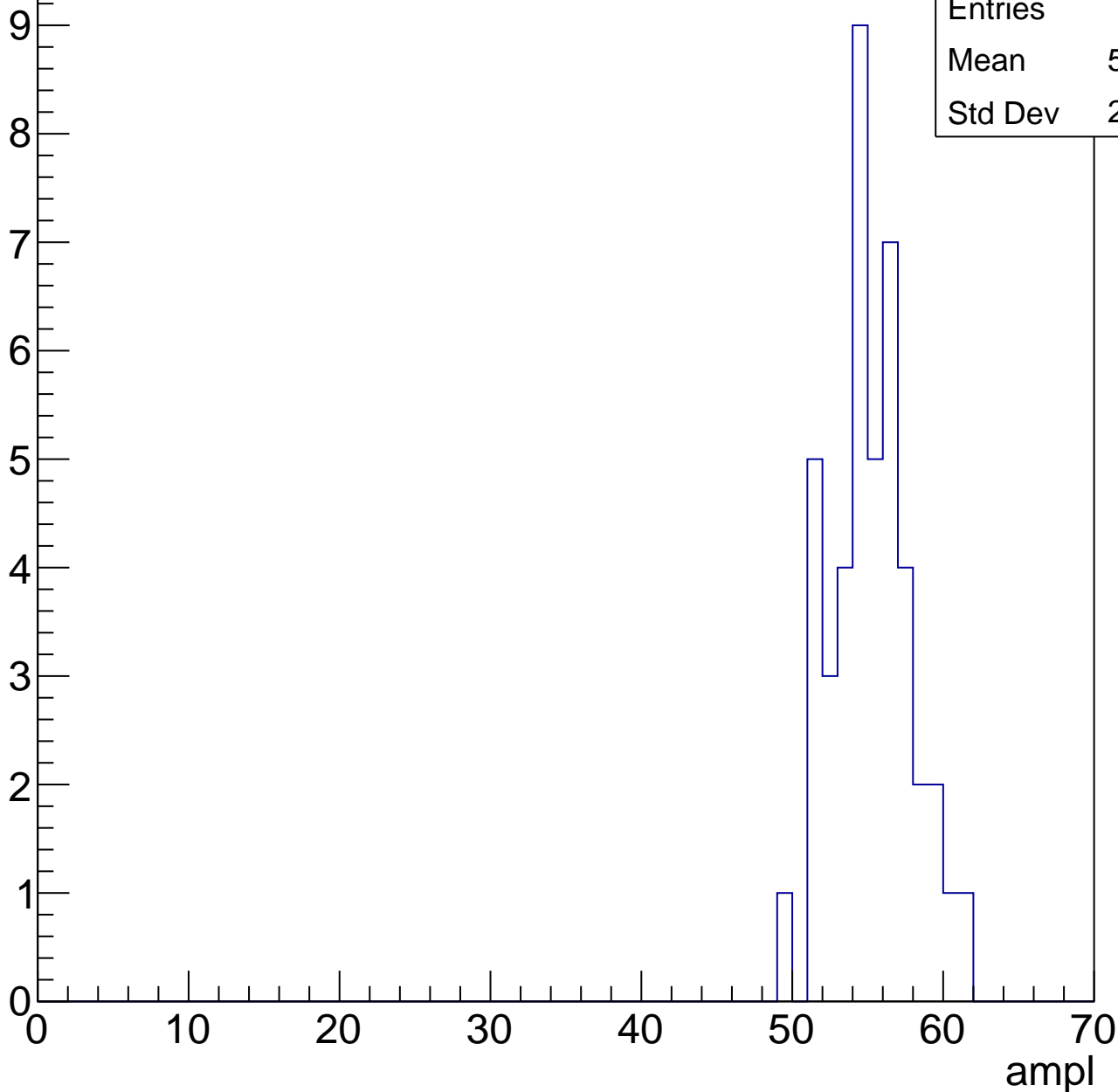


# B1L100S, U6-ch81, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

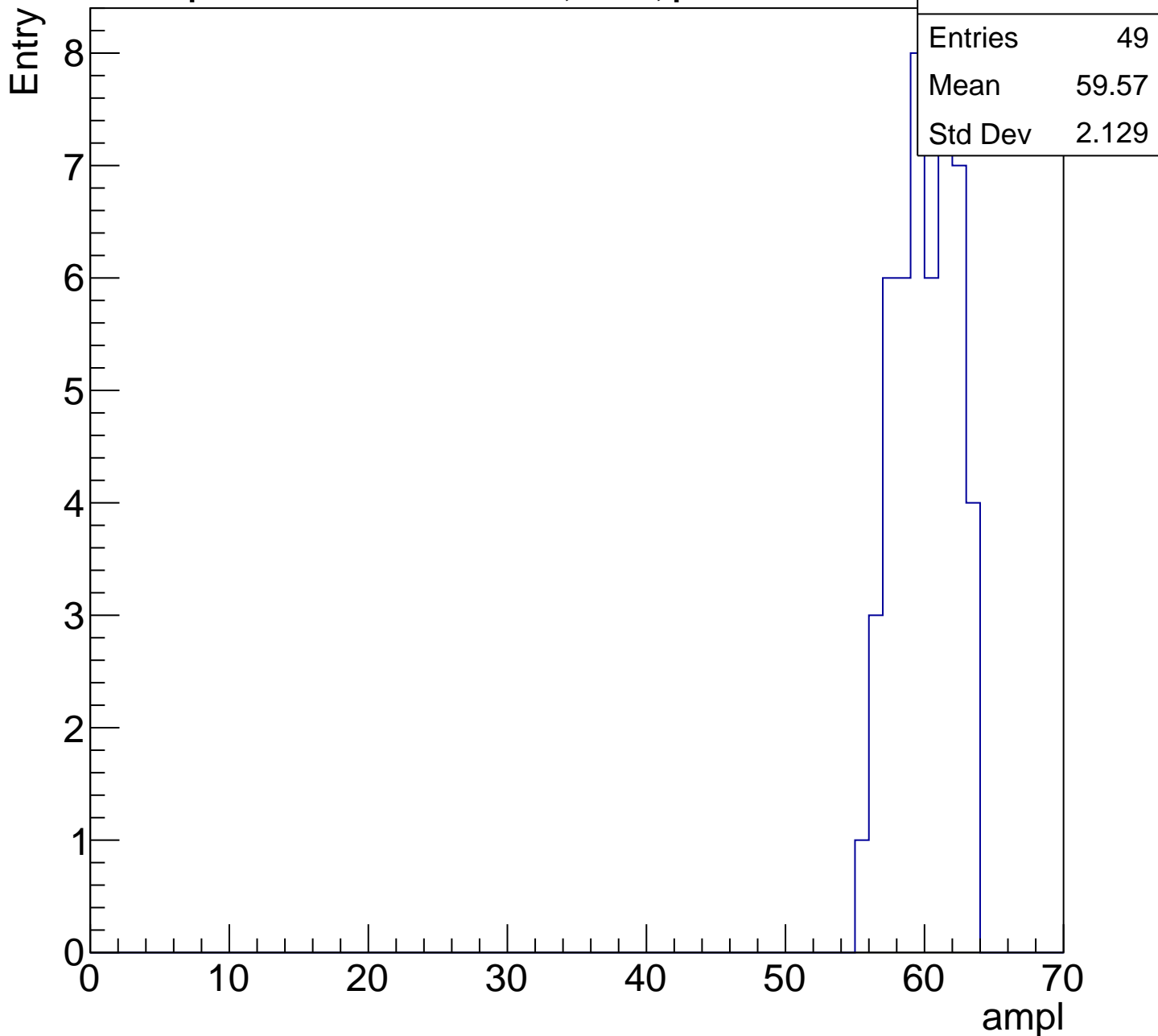
Entry

Entries	44
Mean	54.73
Std Dev	2.606



# B1L100S, U6-ch81, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

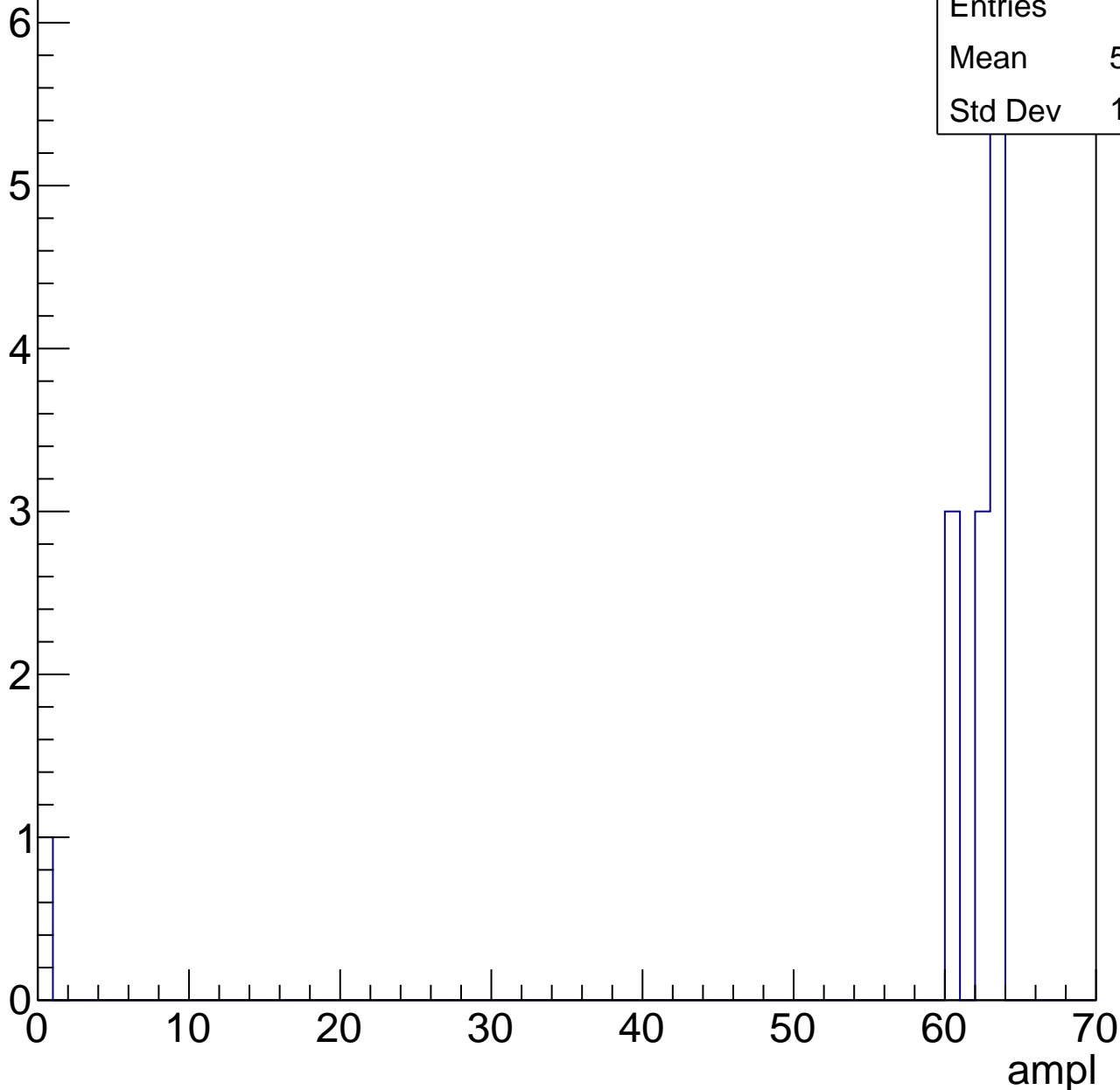


# B1L100S, U6-ch81, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	13
Mean	57.23
Std Dev	16.56





# B1L100S, U6-ch81, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



# B1L100S, U6-ch82, adc0

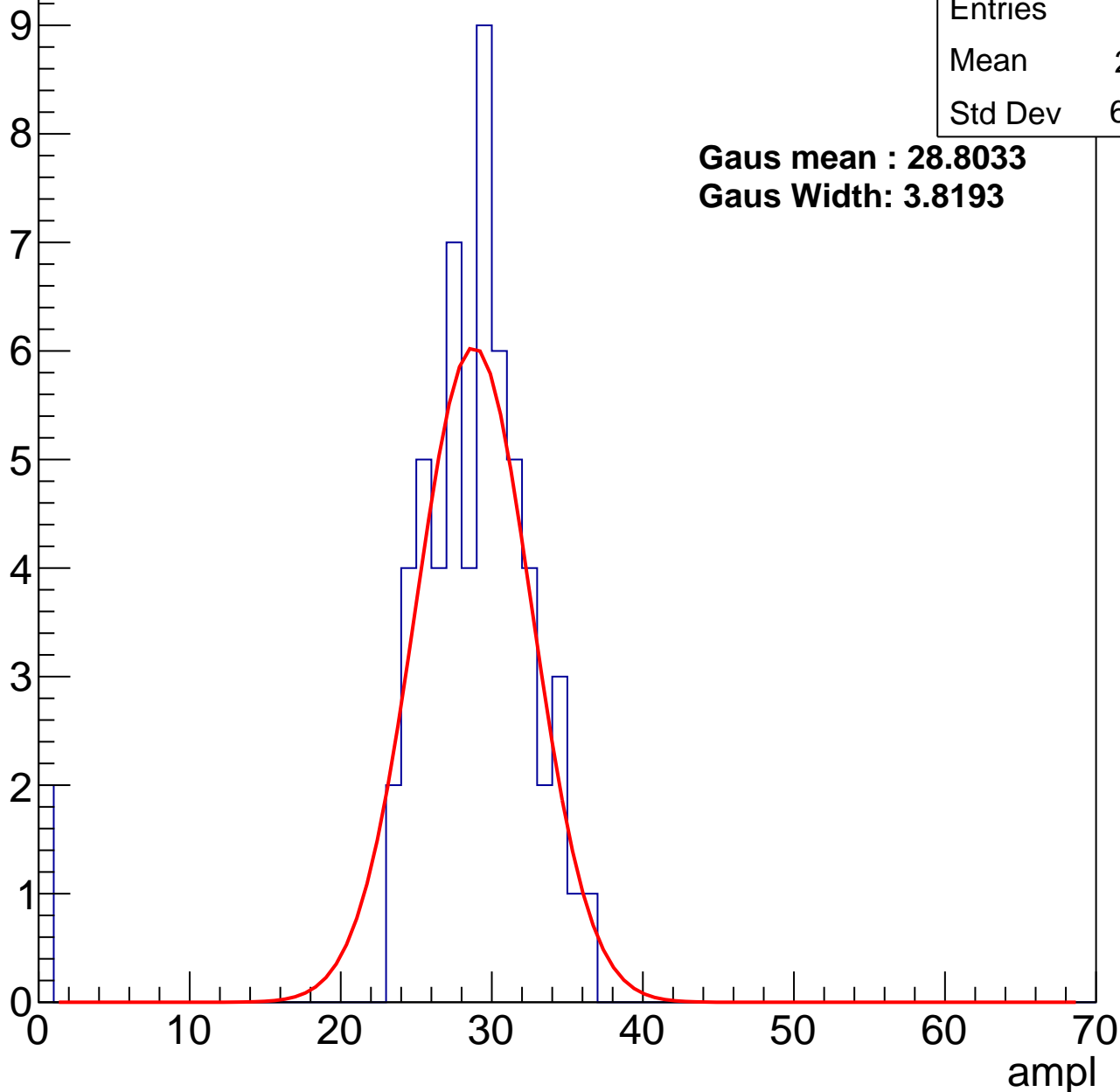
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	59
Mean	27.71
Std Dev	6.048

**Gaus mean : 28.8033**

**Gaus Width: 3.8193**



# B1L100S, U6-ch82, adc1

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	70
Mean	34.34
Std Dev	3.641

**Gaus mean : 34.9866**

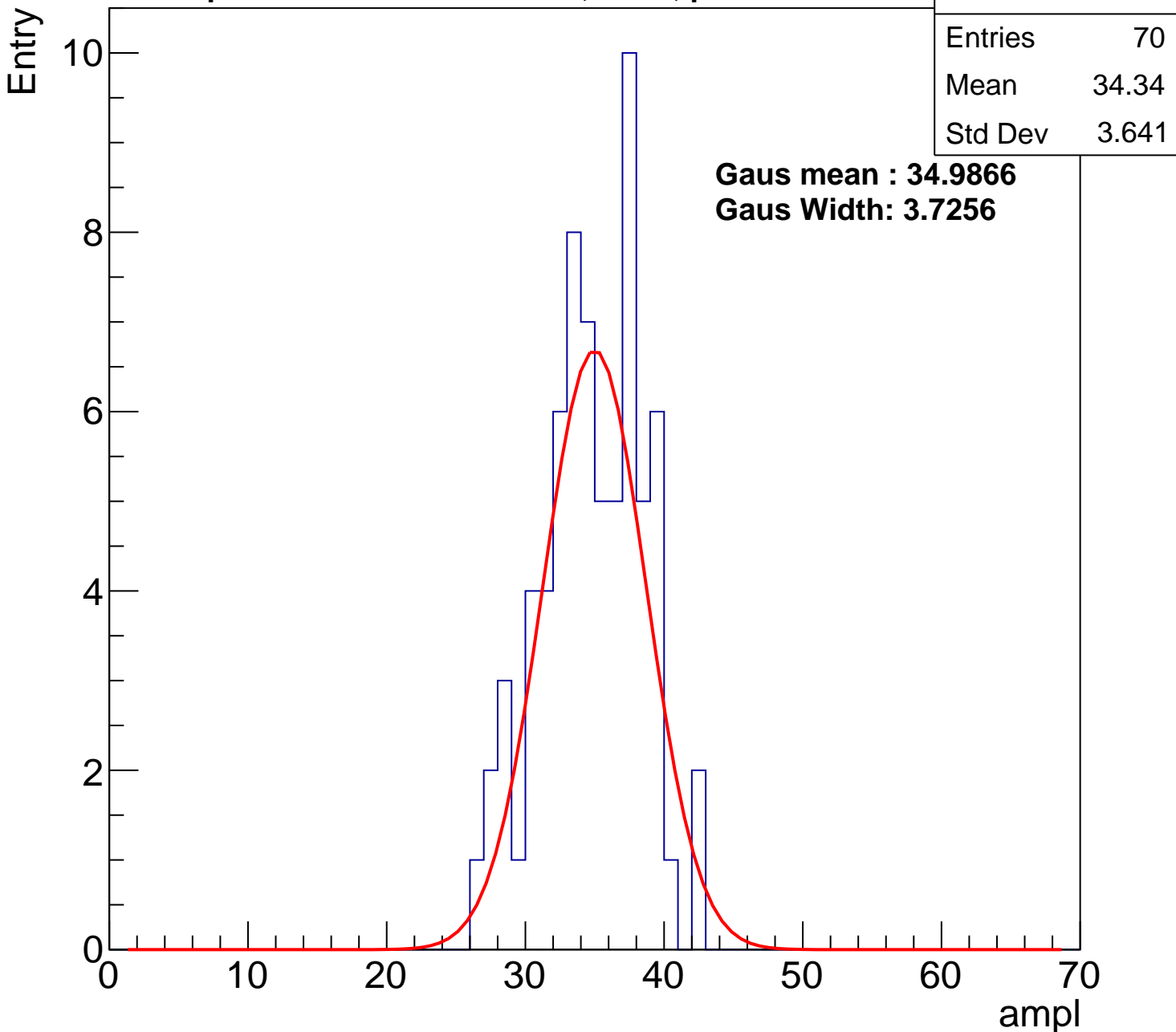
**Gaus Width: 3.7256**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B1L100S, U6-ch82, adc2

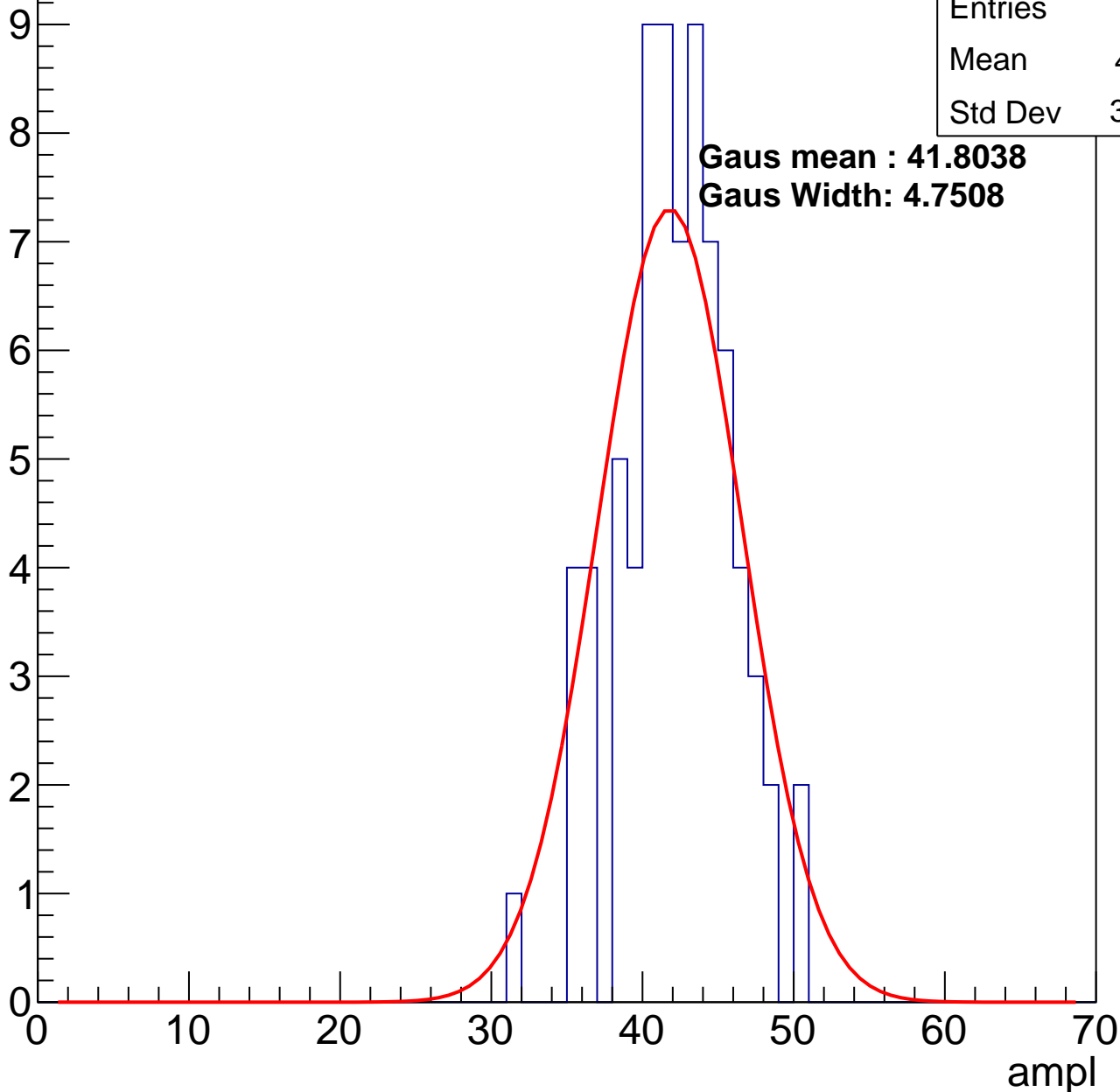
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	76
Mean	41.71
Std Dev	3.709

**Gaus mean : 41.8038**

**Gaus Width: 4.7508**

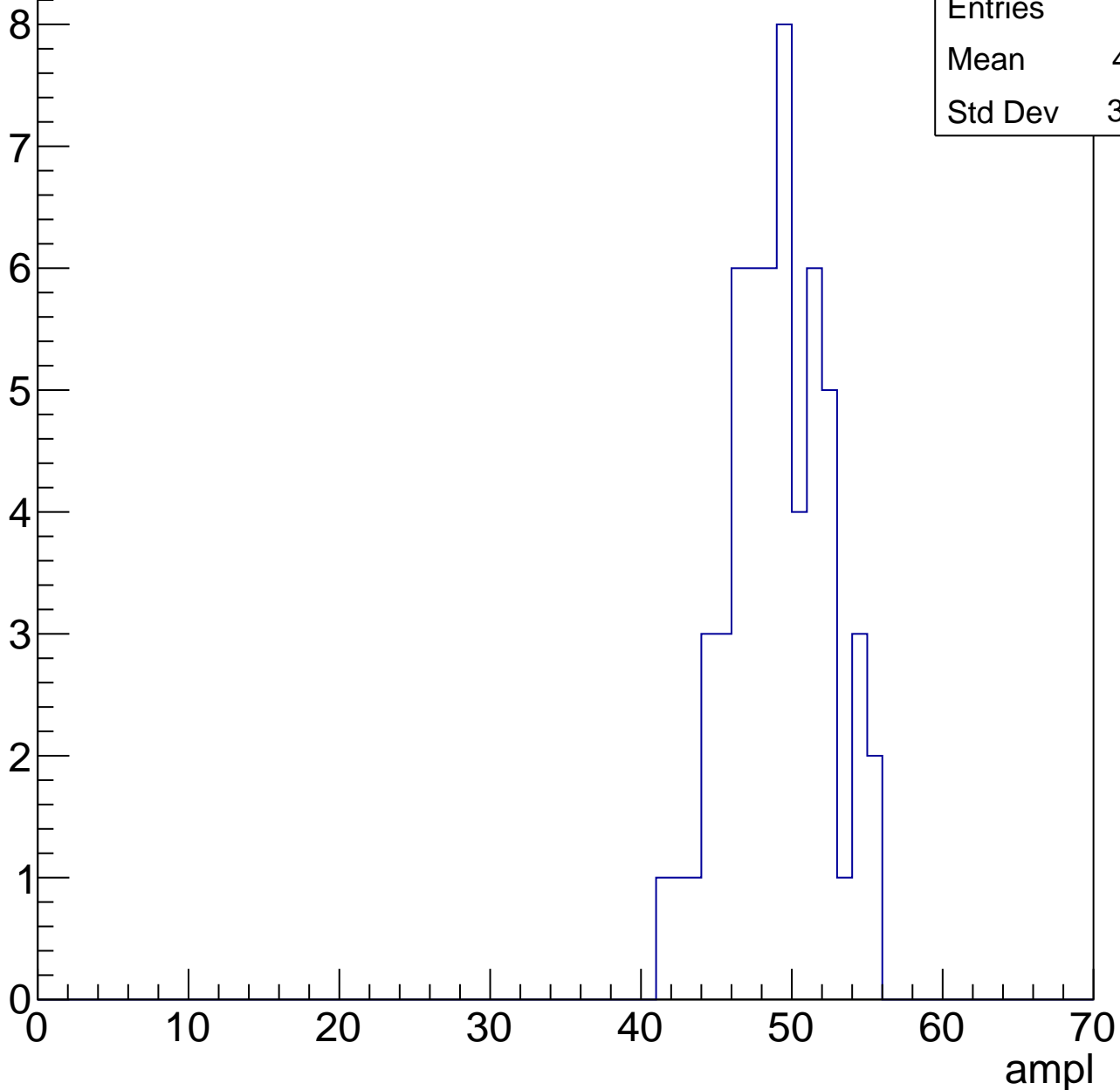


# B1L100S, U6-ch82, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	56
Mean	48.61
Std Dev	3.228

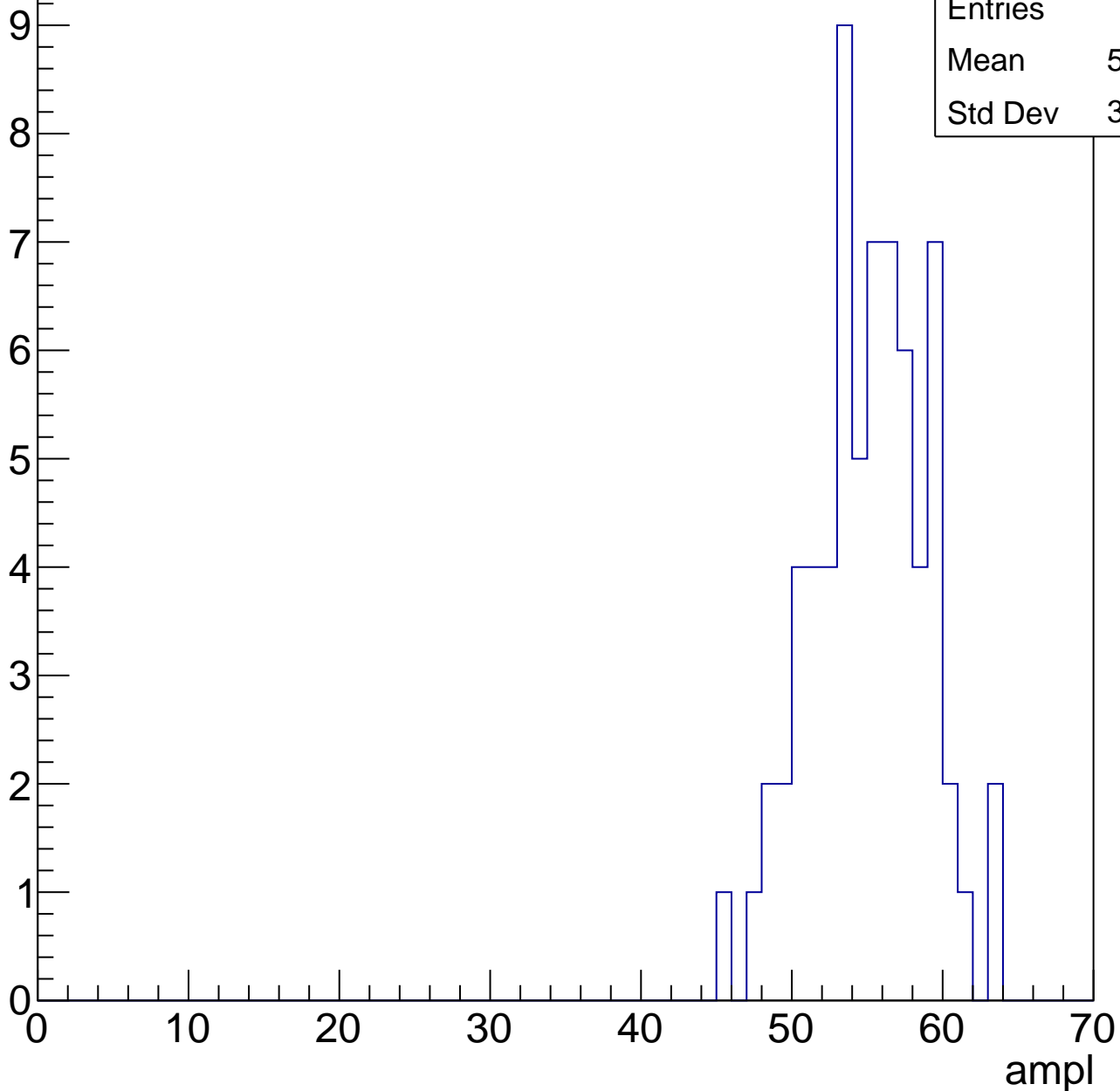


# B1L100S, U6-ch82, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	68
Mean	54.65
Std Dev	3.756

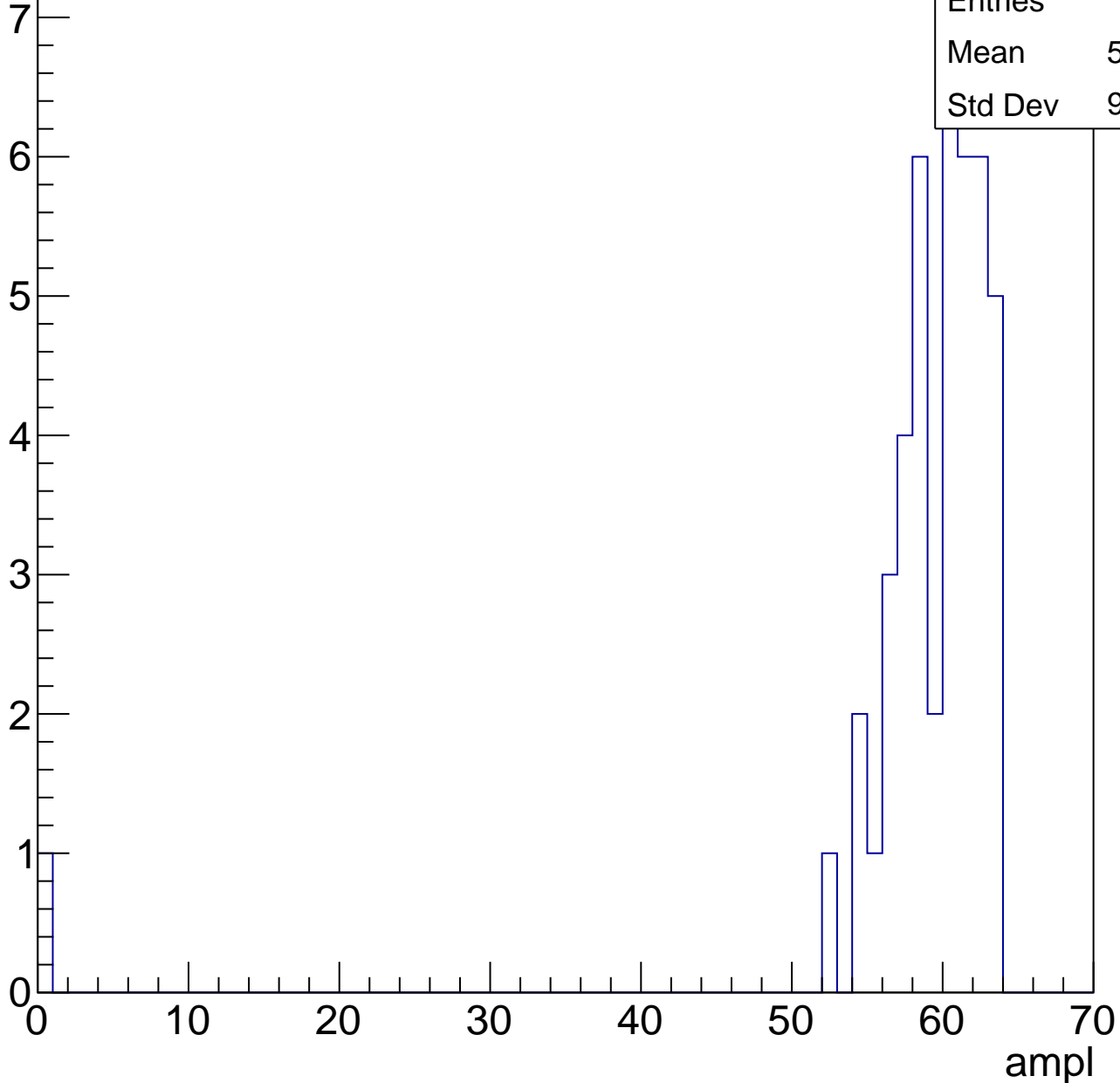


# B1L100S, U6-ch82, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

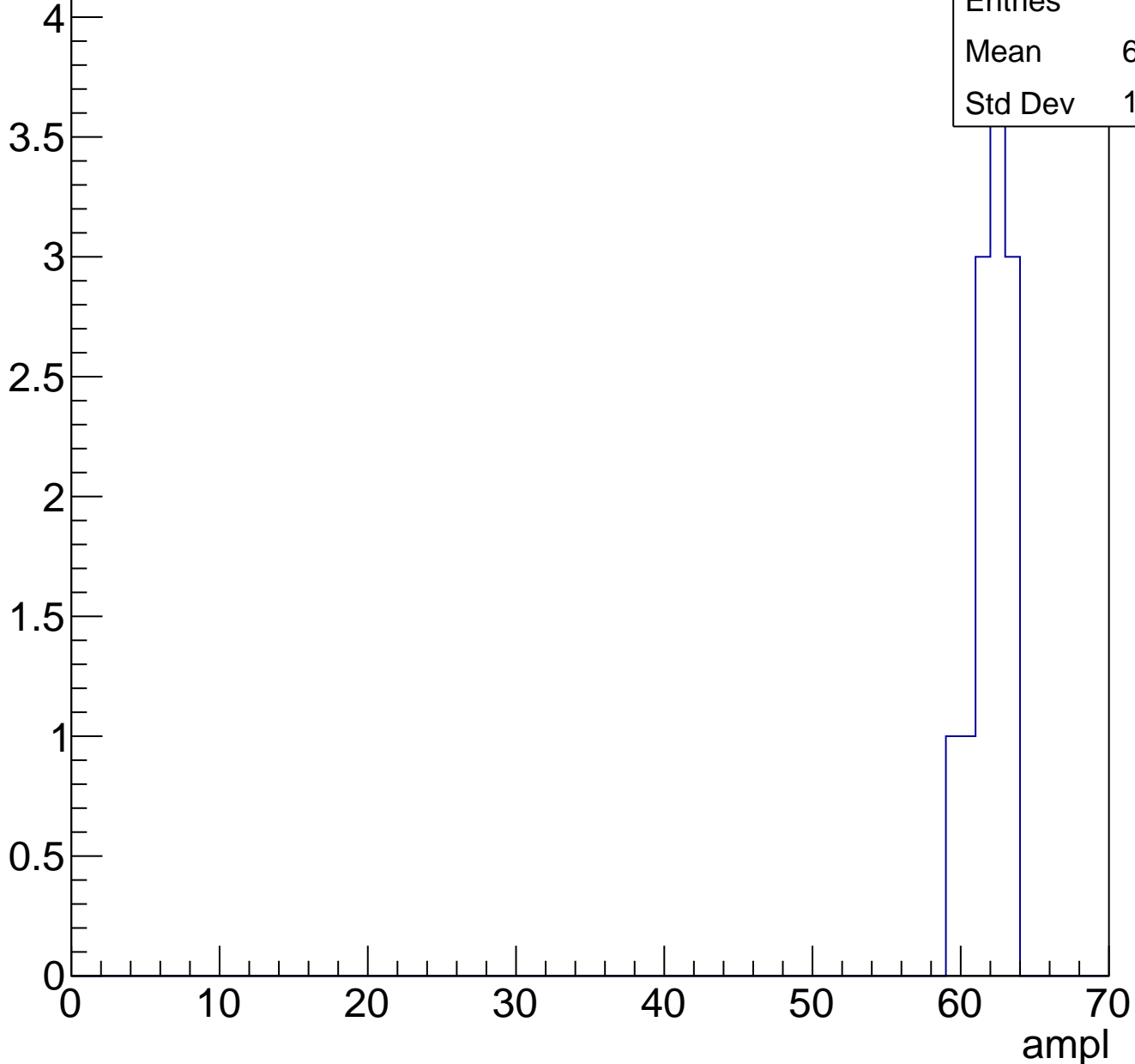
Entries	44
Mean	57.95
Std Dev	9.247



# B1L100S, U6-ch82, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry





# B1L100S, U6-ch82, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	1
Mean	23
Std Dev	0

# B1L100S, U6-ch83, adc0

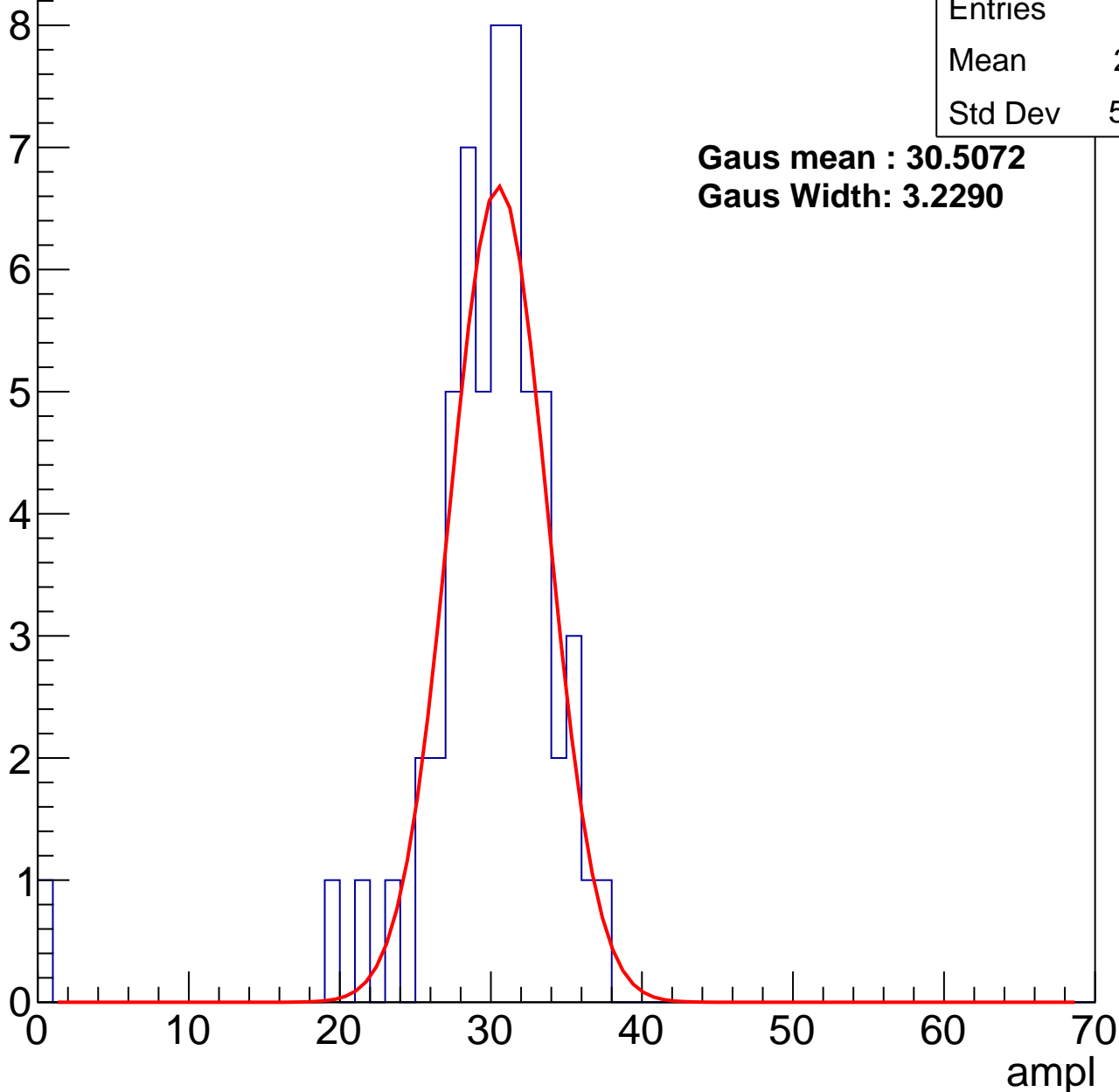
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	58
Mean	29.31
Std Dev	5.167

**Gaus mean : 30.5072**

**Gaus Width: 3.2290**



# B1L100S, U6-ch83, adc1

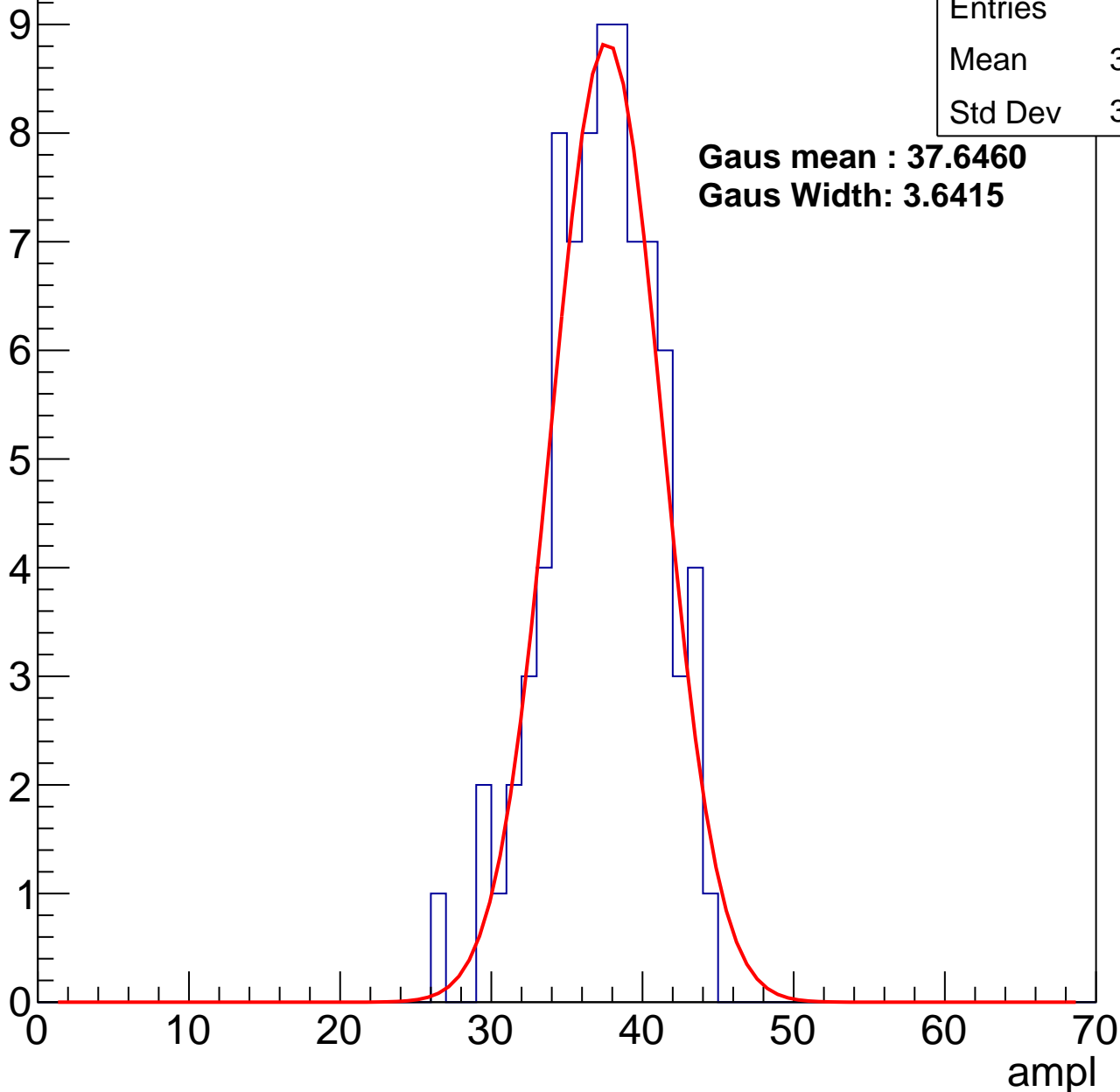
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	82
Mean	36.89
Std Dev	3.629

**Gaus mean : 37.6460**

**Gaus Width: 3.6415**

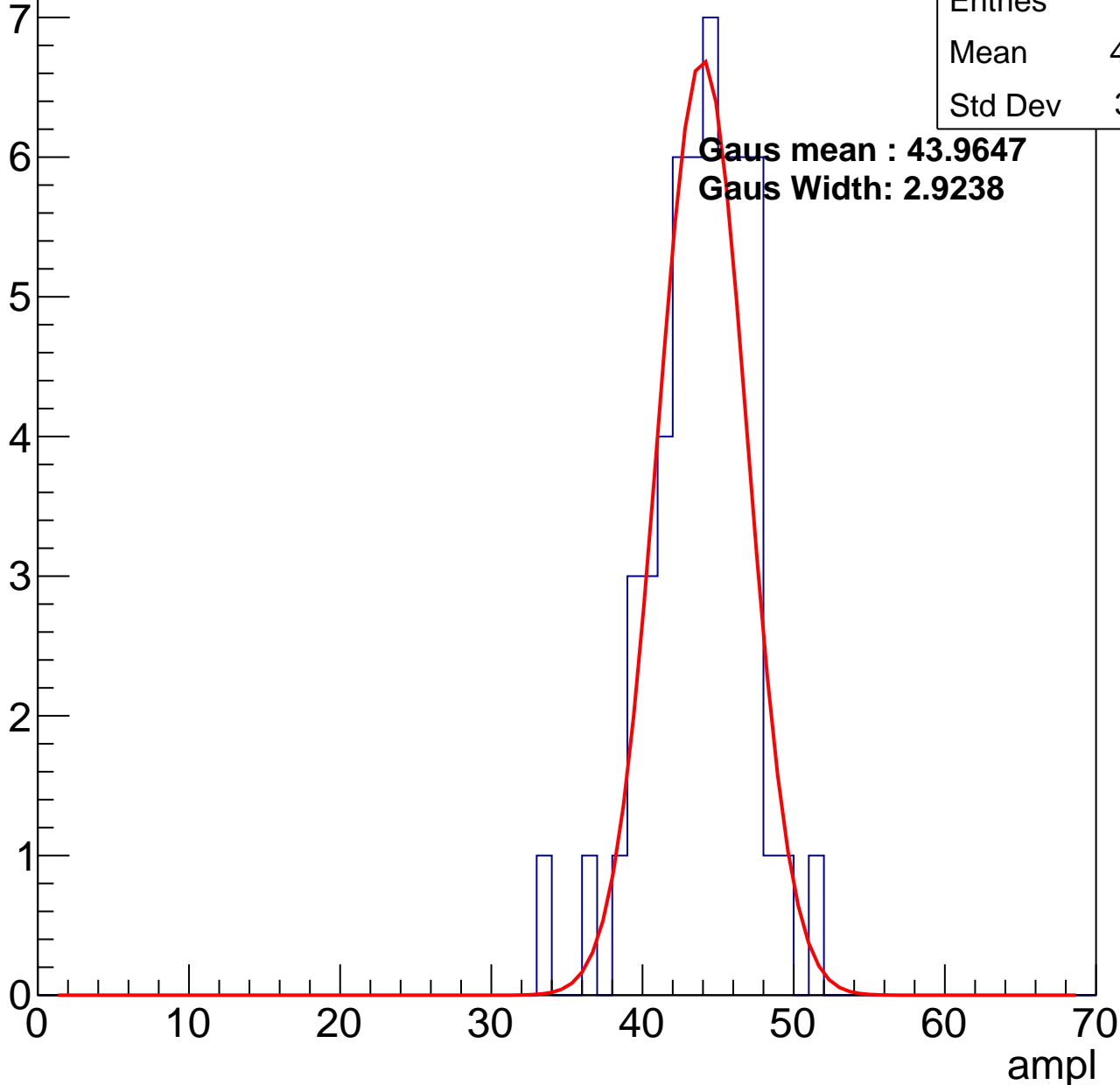


# B1L100S, U6-ch83, adc2

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	53
Mean	43.43
Std Dev	3.271

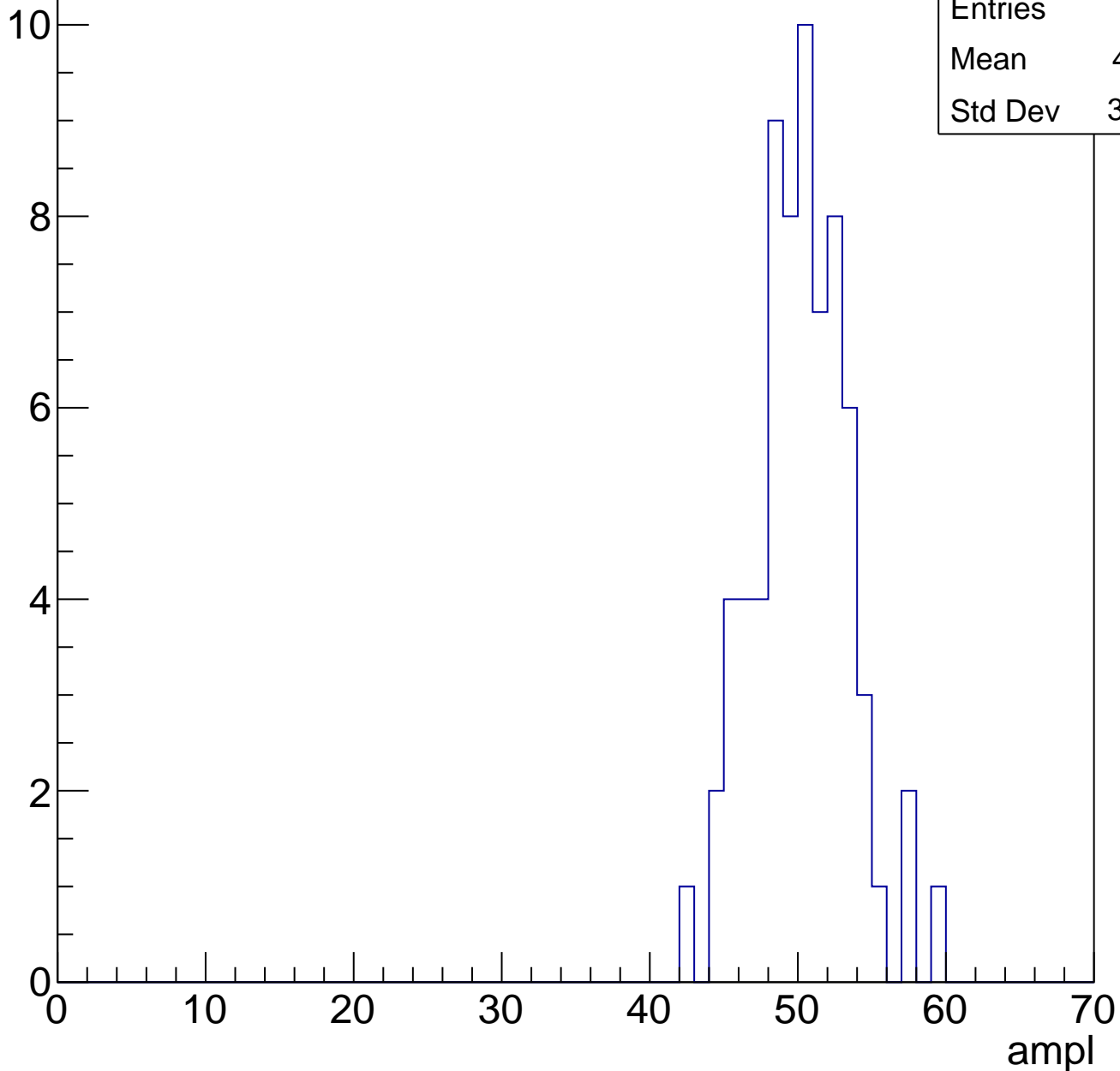


# B1L100S, U6-ch83, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

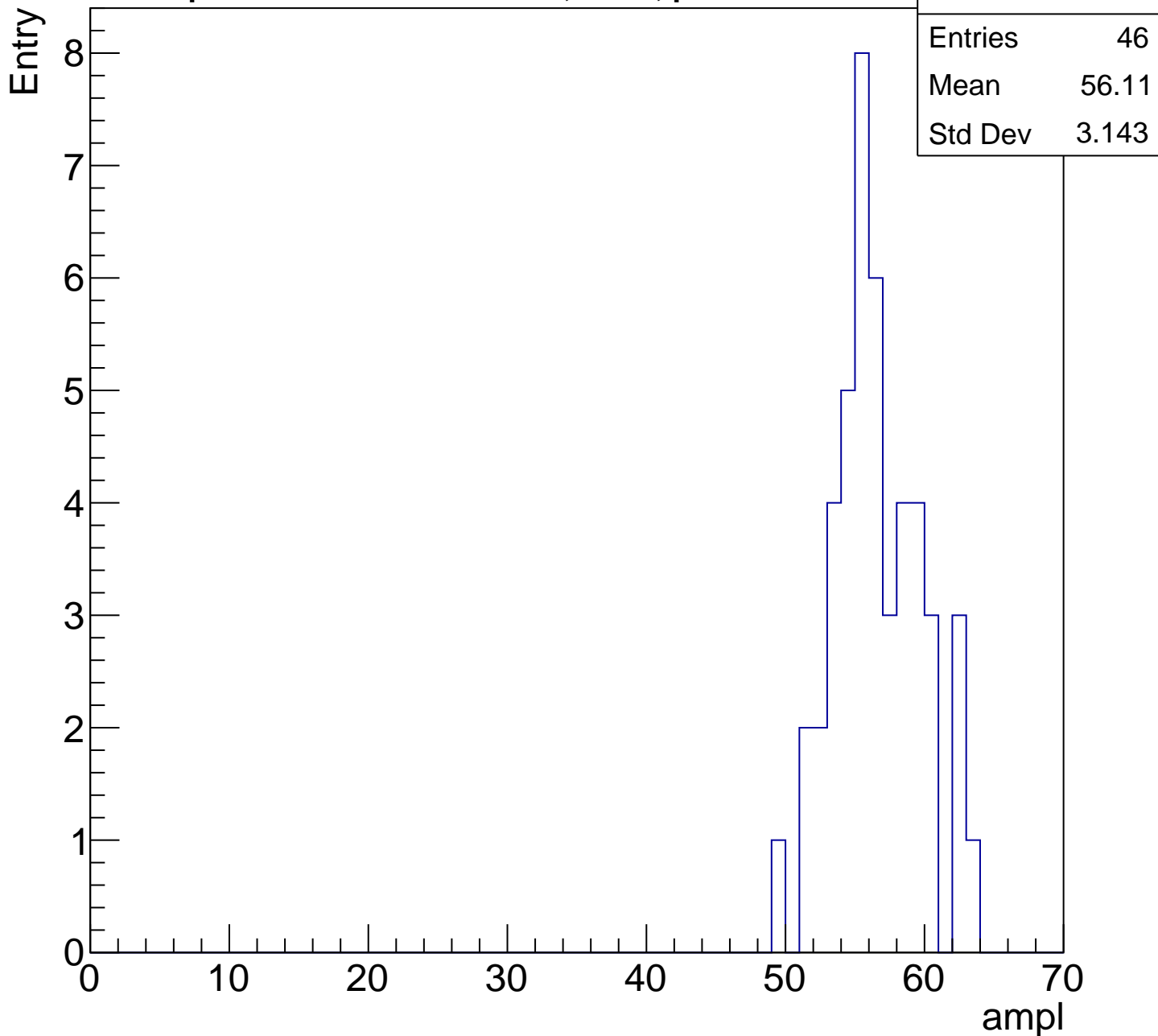
Entries	70
Mean	49.81
Std Dev	3.213

Entry



# B1L100S, U6-ch83, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

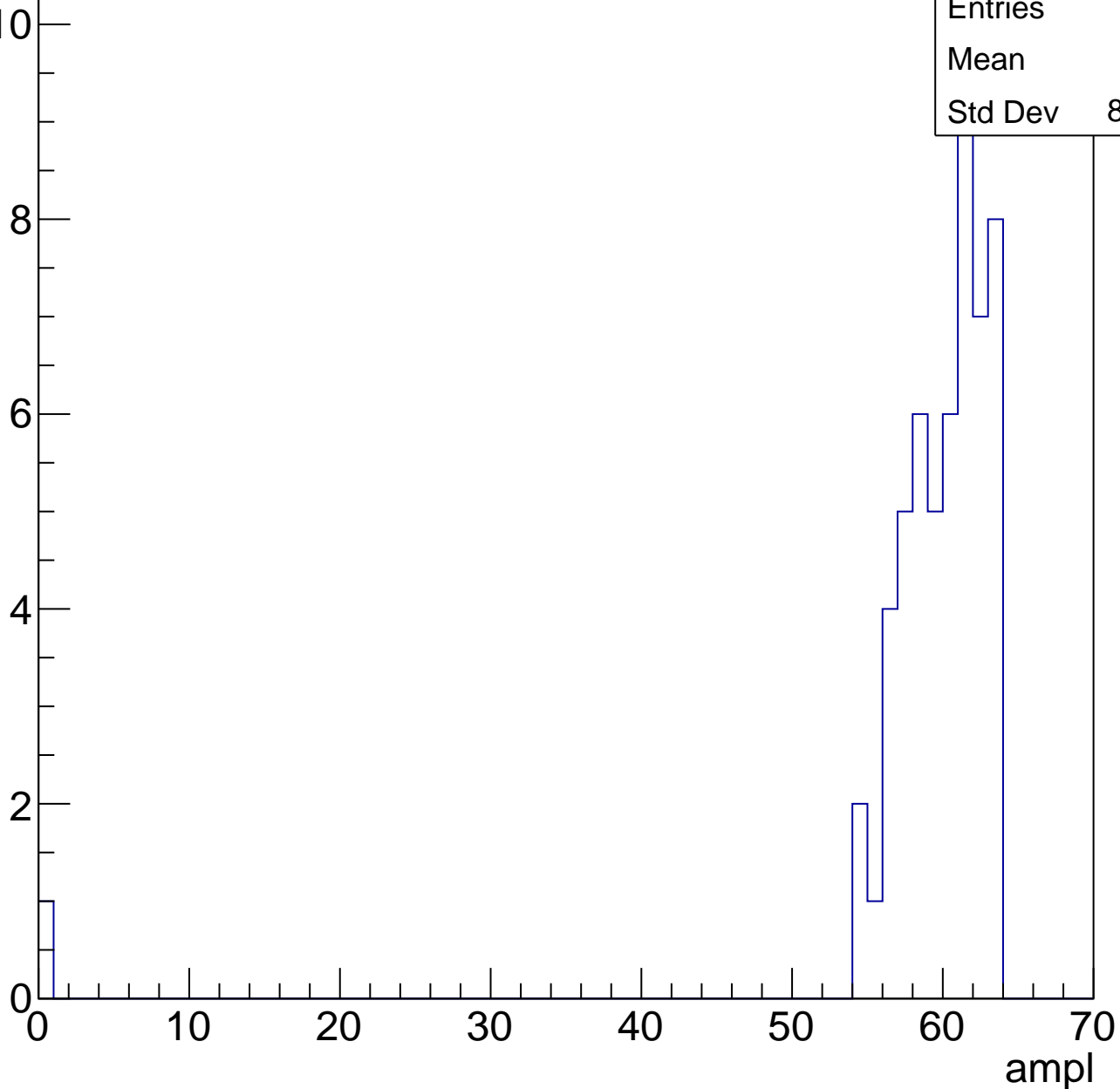


# B1L100S, U6-ch83, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

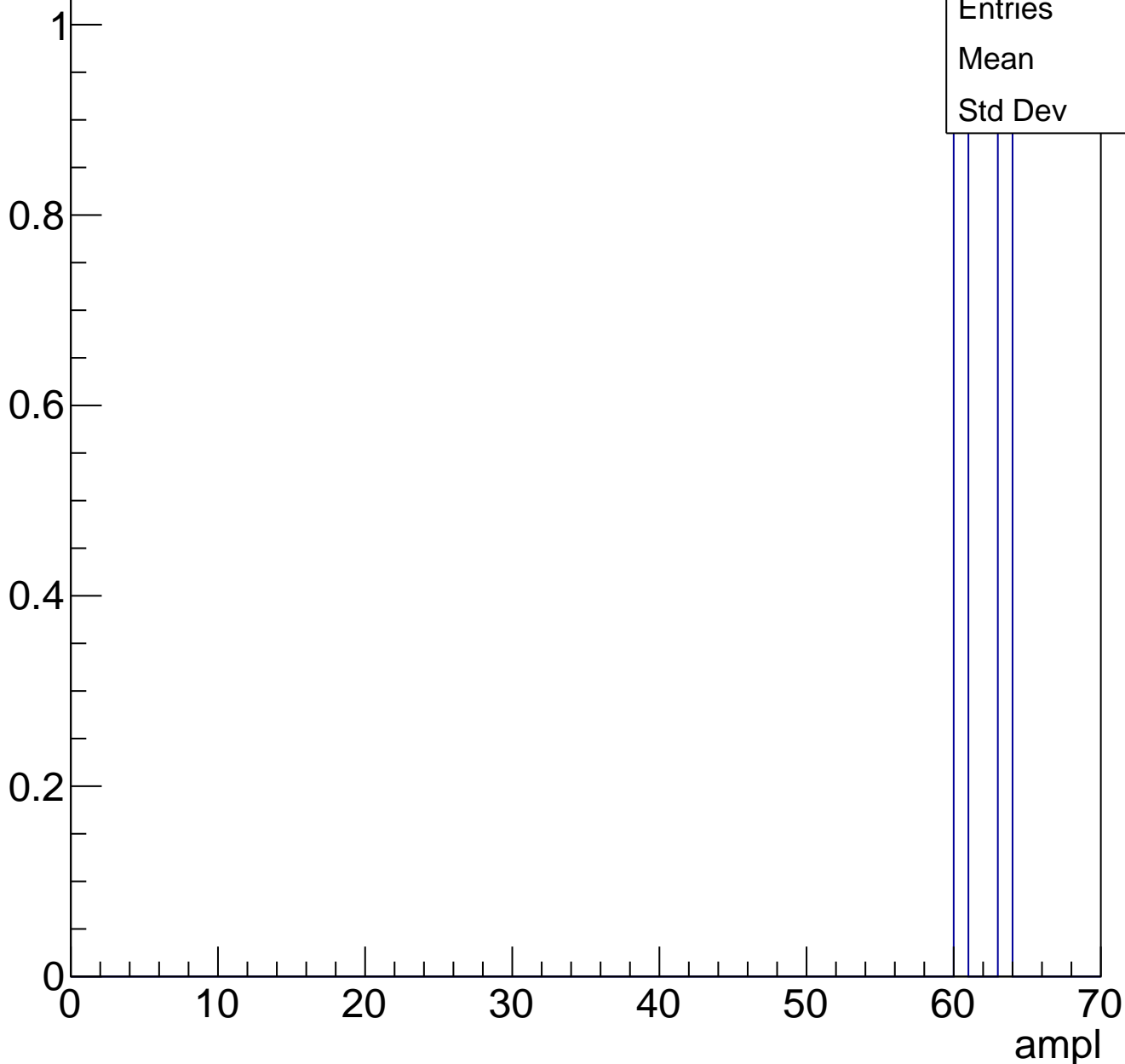
Entries	55
Mean	58.6
Std Dev	8.353



# B1L100S, U6-ch83, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry





# B1L100S, U6-ch83, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L100S, U6-ch84, adc0

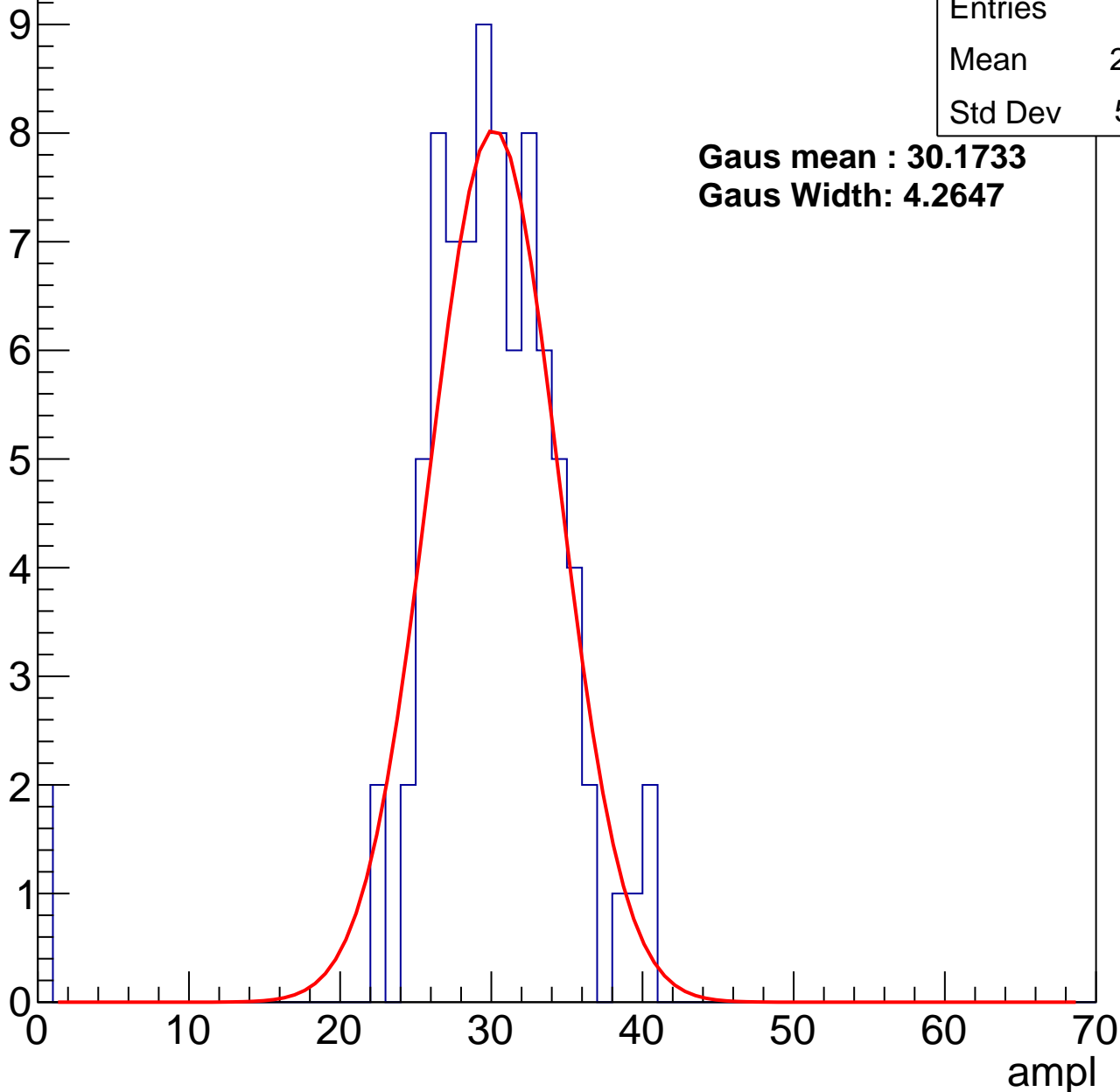
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	85
Mean	29.29
Std Dev	5.941

**Gaus mean : 30.1733**

**Gaus Width: 4.2647**



# B1L100S, U6-ch84, adc1

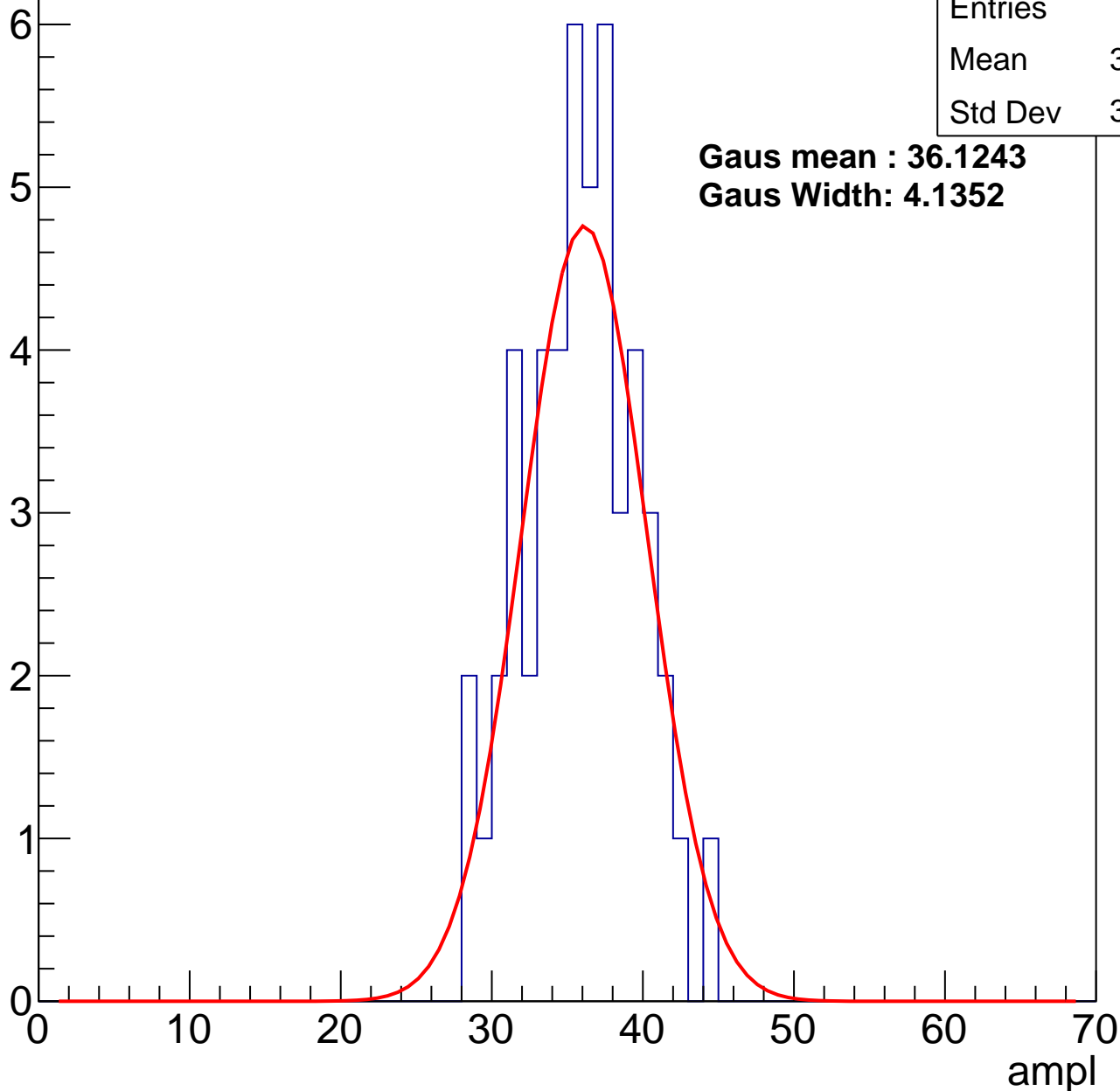
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	50
Mean	35.42
Std Dev	3.672

**Gaus mean : 36.1243**

**Gaus Width: 4.1352**



# B1L100S, U6-ch84, adc2

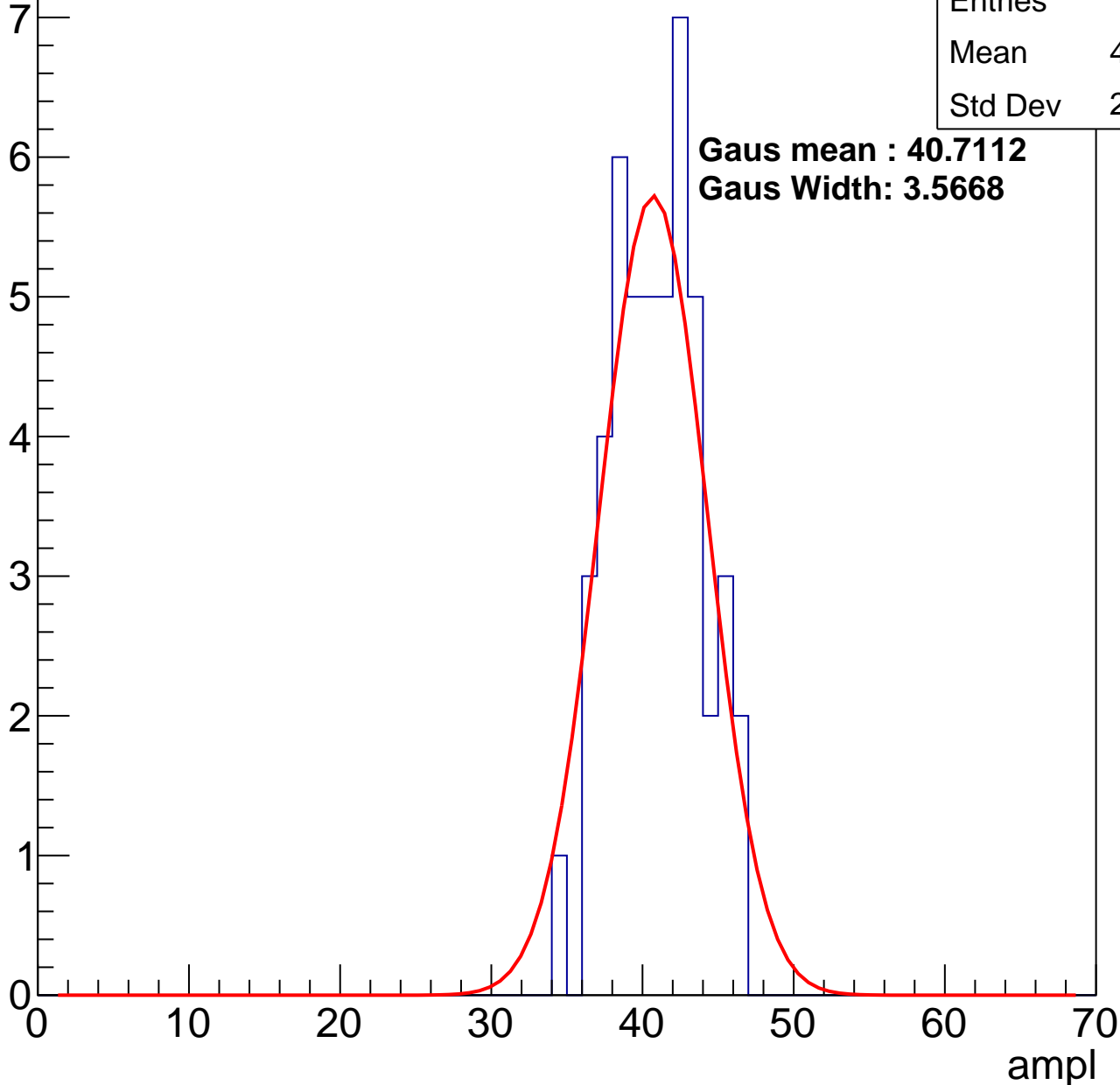
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	48
Mean	40.46
Std Dev	2.872

**Gaus mean : 40.7112**

**Gaus Width: 3.5668**

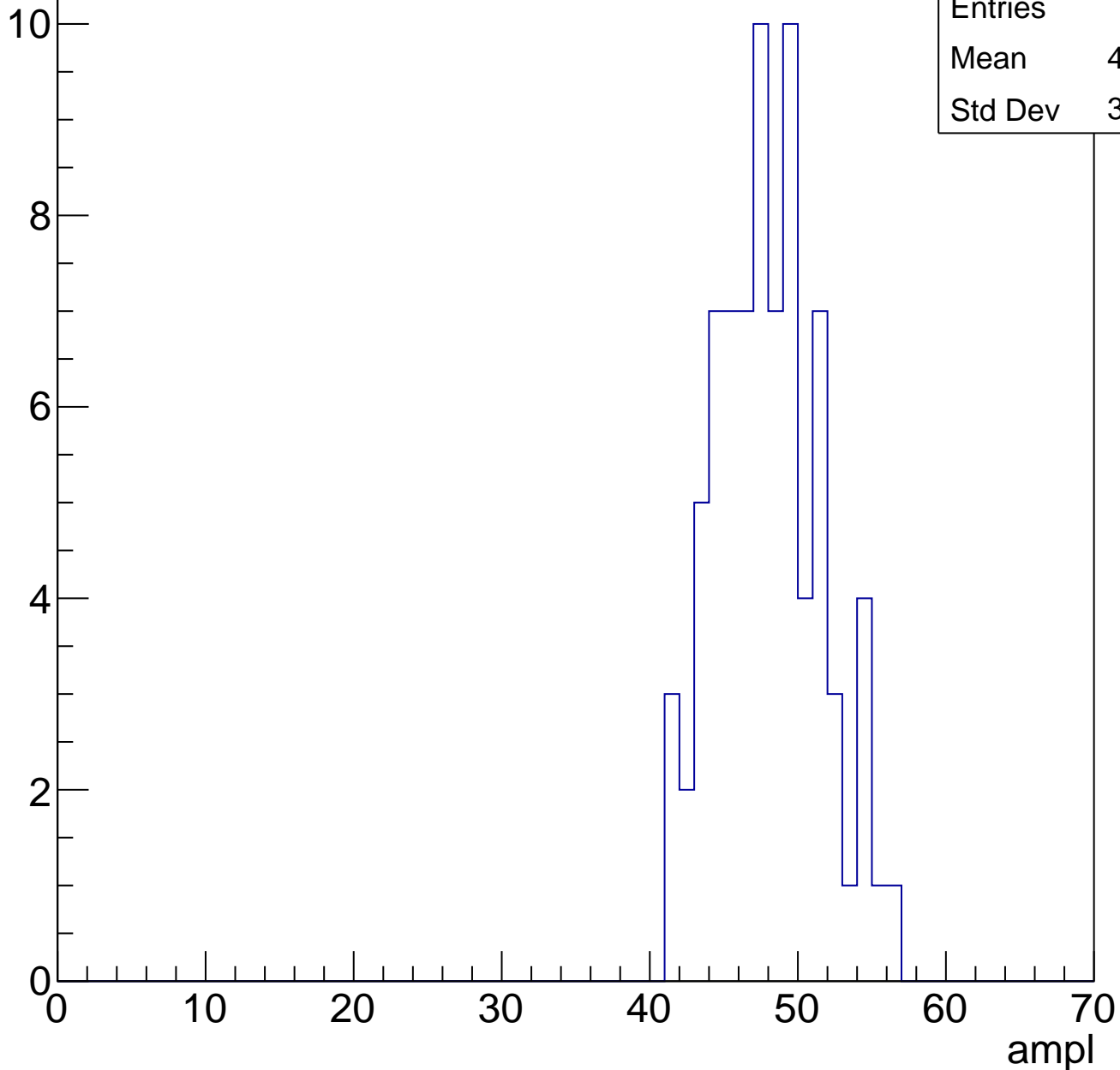


# B1L100S, U6-ch84, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

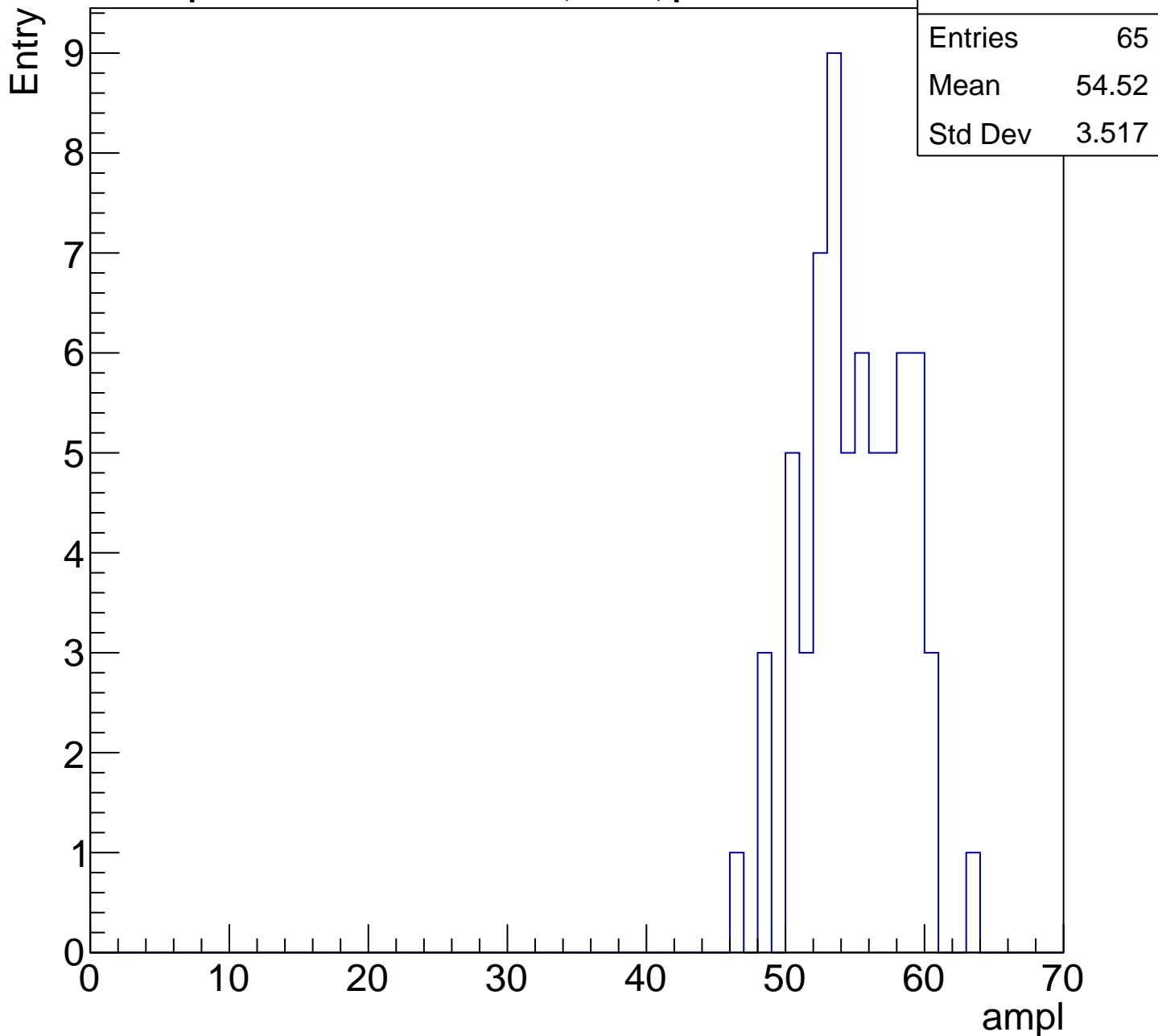
Entries	79
Mean	47.54
Std Dev	3.485

Entry



# B1L100S, U6-ch84, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

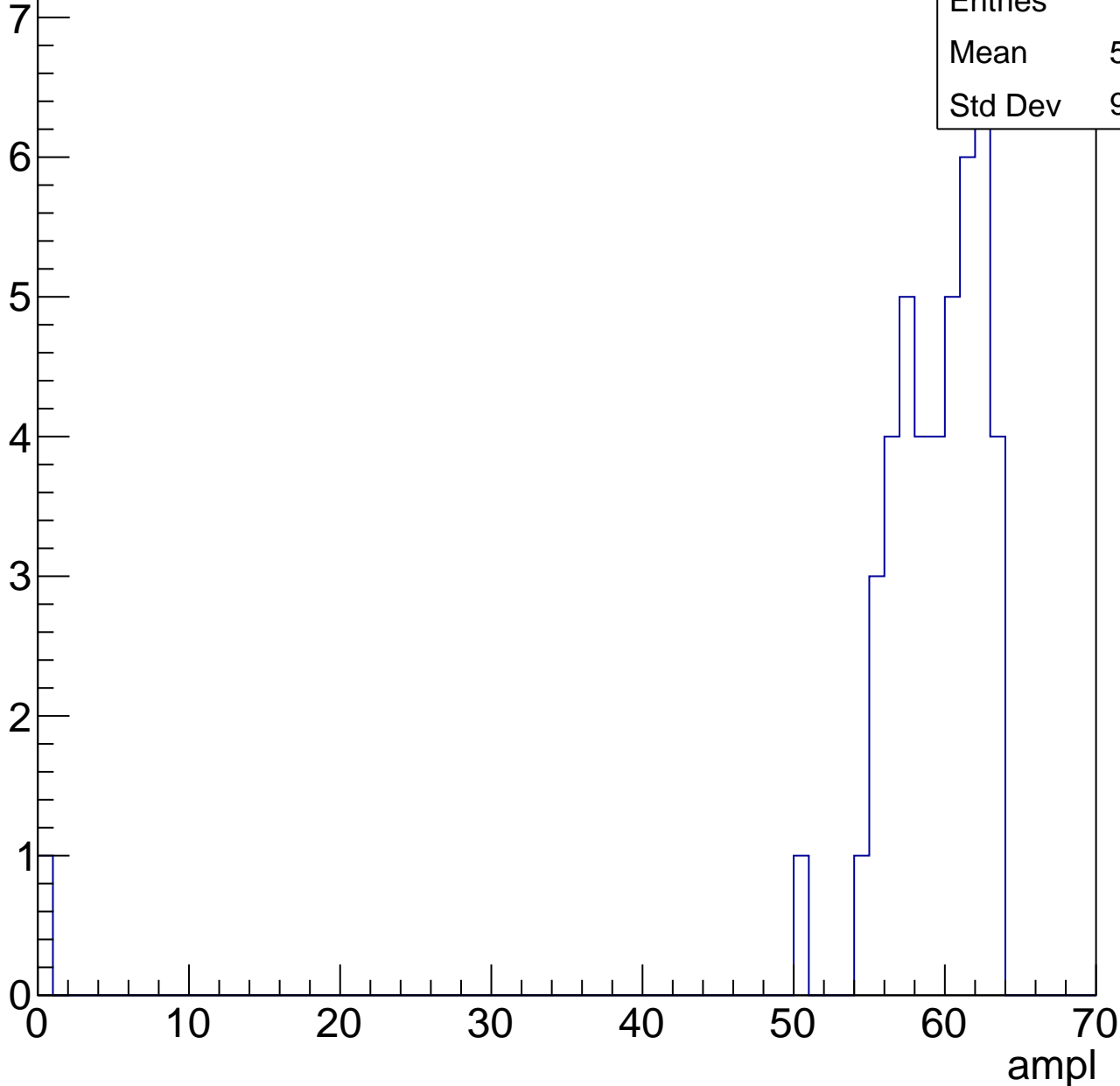


# B1L100S, U6-ch84, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	45
Mean	57.73
Std Dev	9.164

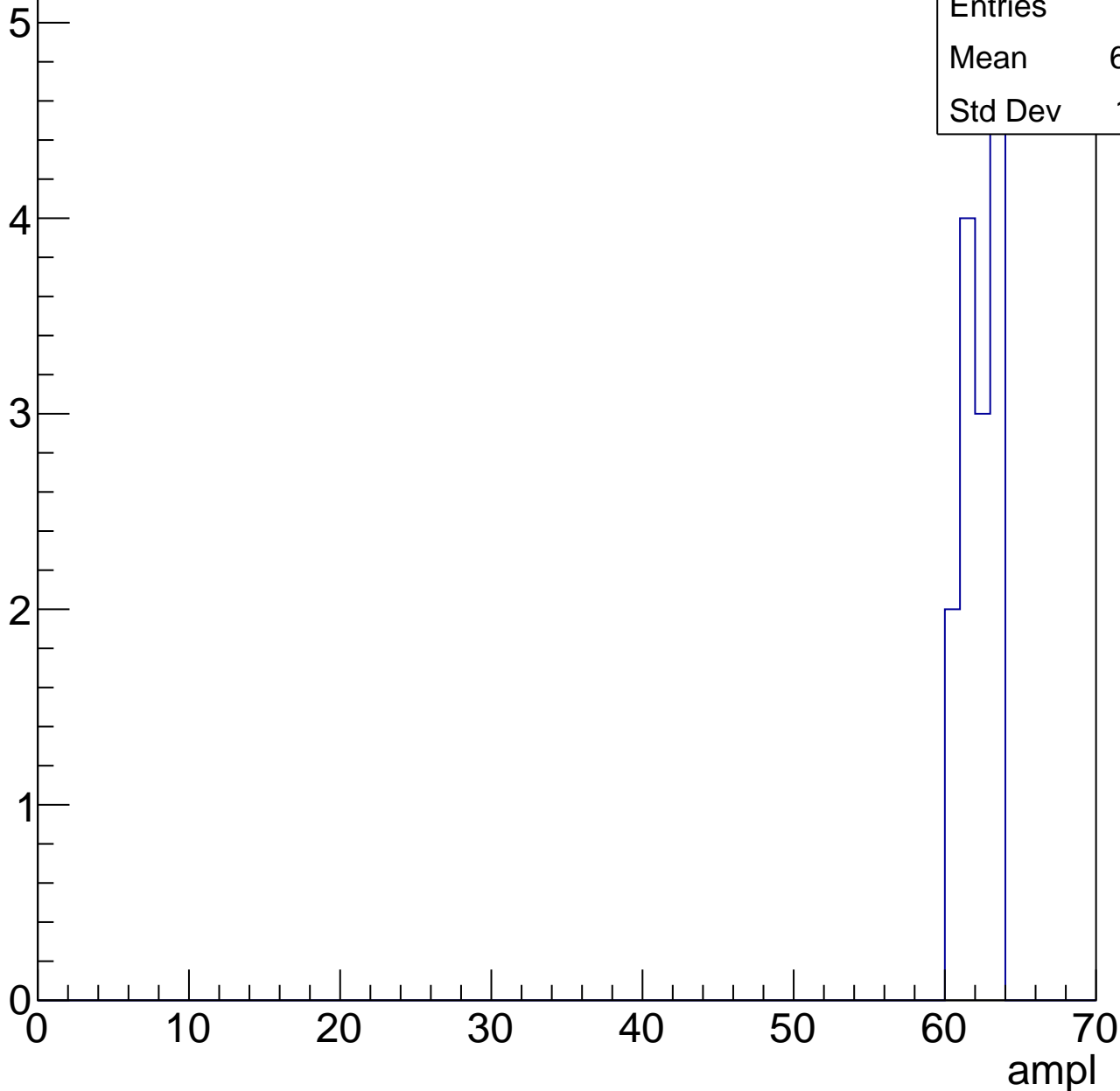


# B1L100S, U6-ch84, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	14
Mean	61.79
Std Dev	1.081





# B1L100S, U6-ch84, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	2
Mean	10
Std Dev	10

# B1L100S, U6-ch85, adc0

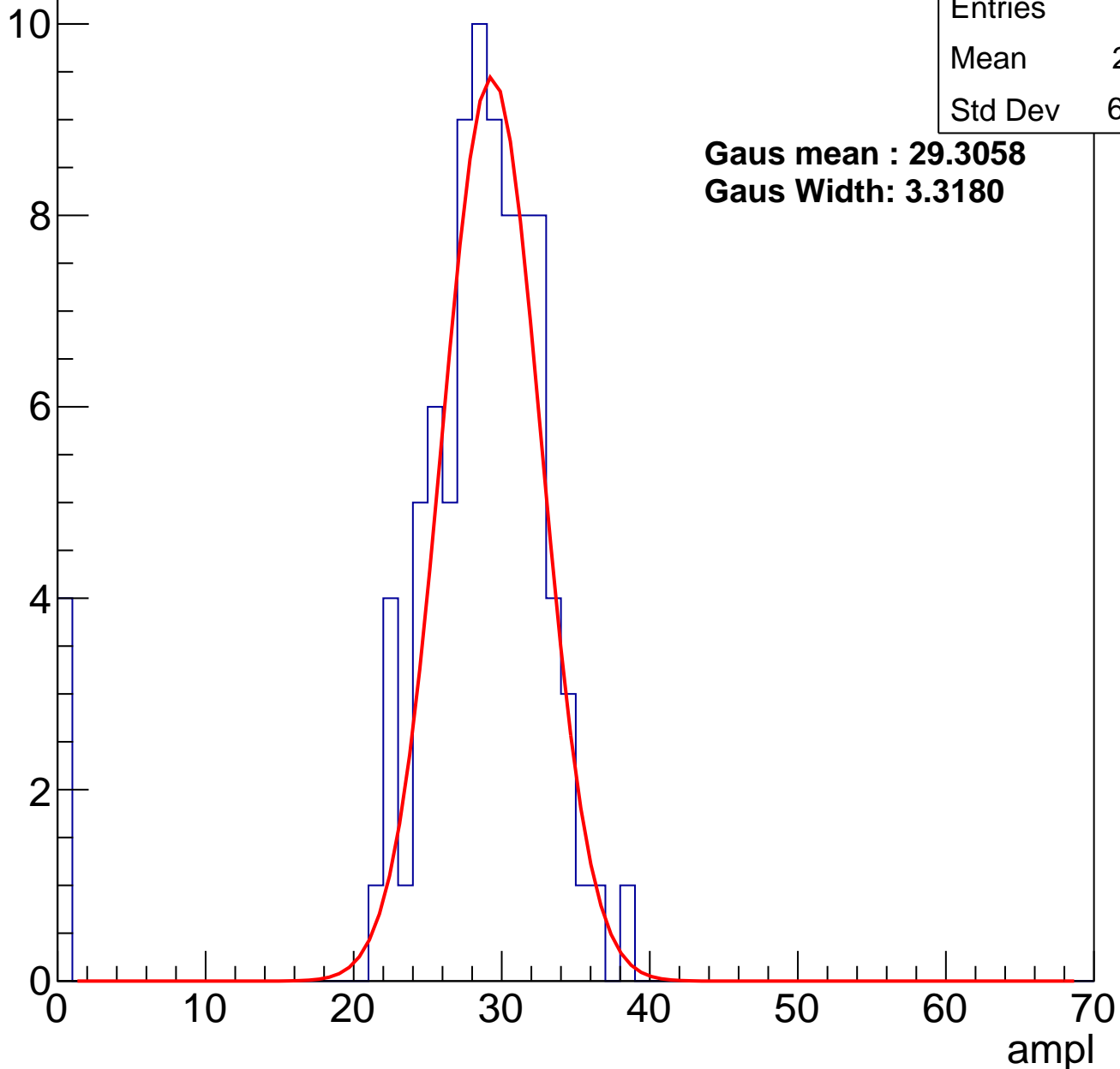
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	88
Mean	27.31
Std Dev	6.856

**Gaus mean : 29.3058**

**Gaus Width: 3.3180**

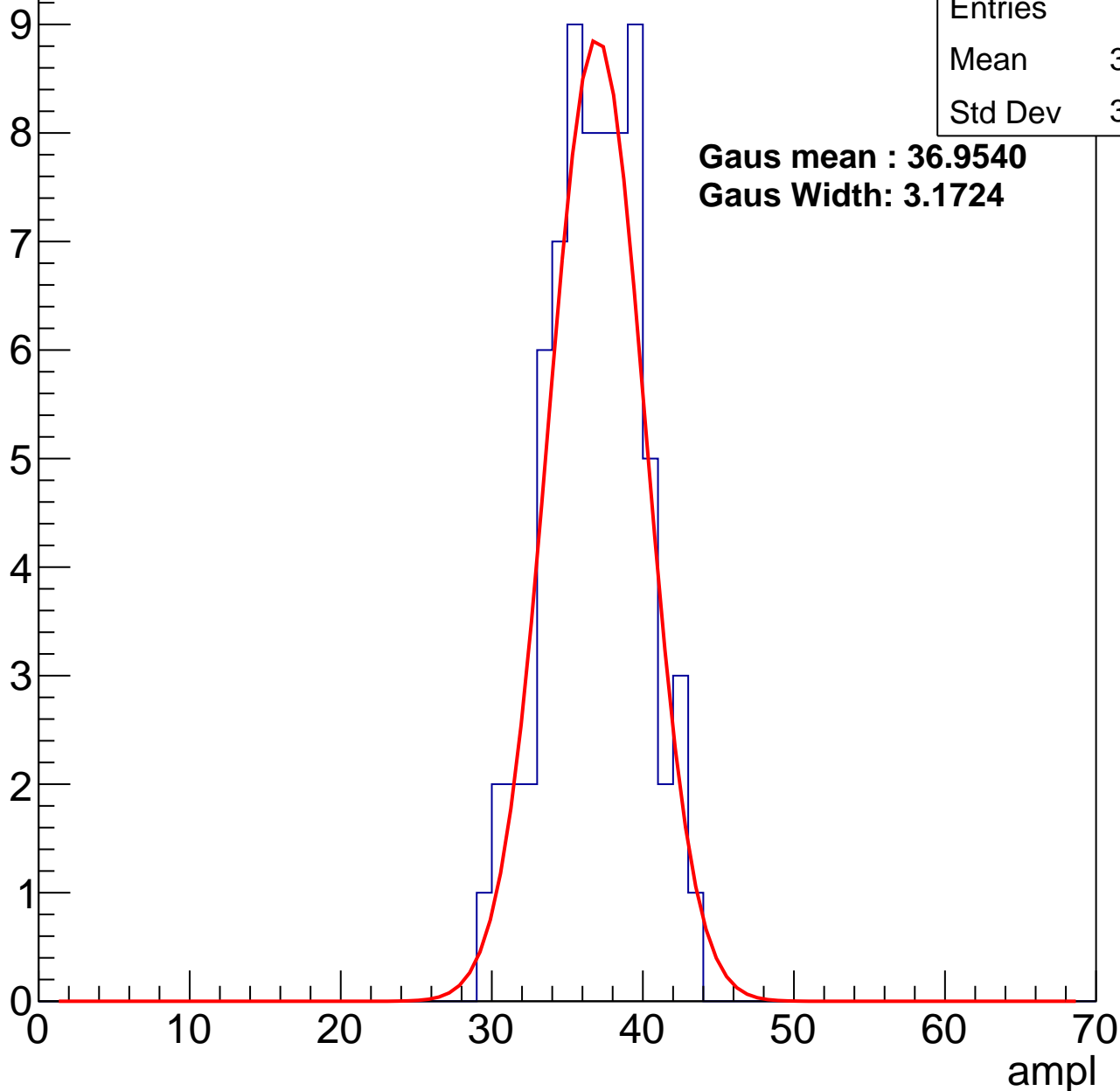
Entry



# B1L100S, U6-ch85, adc1

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



# B1L100S, U6-ch85, adc2

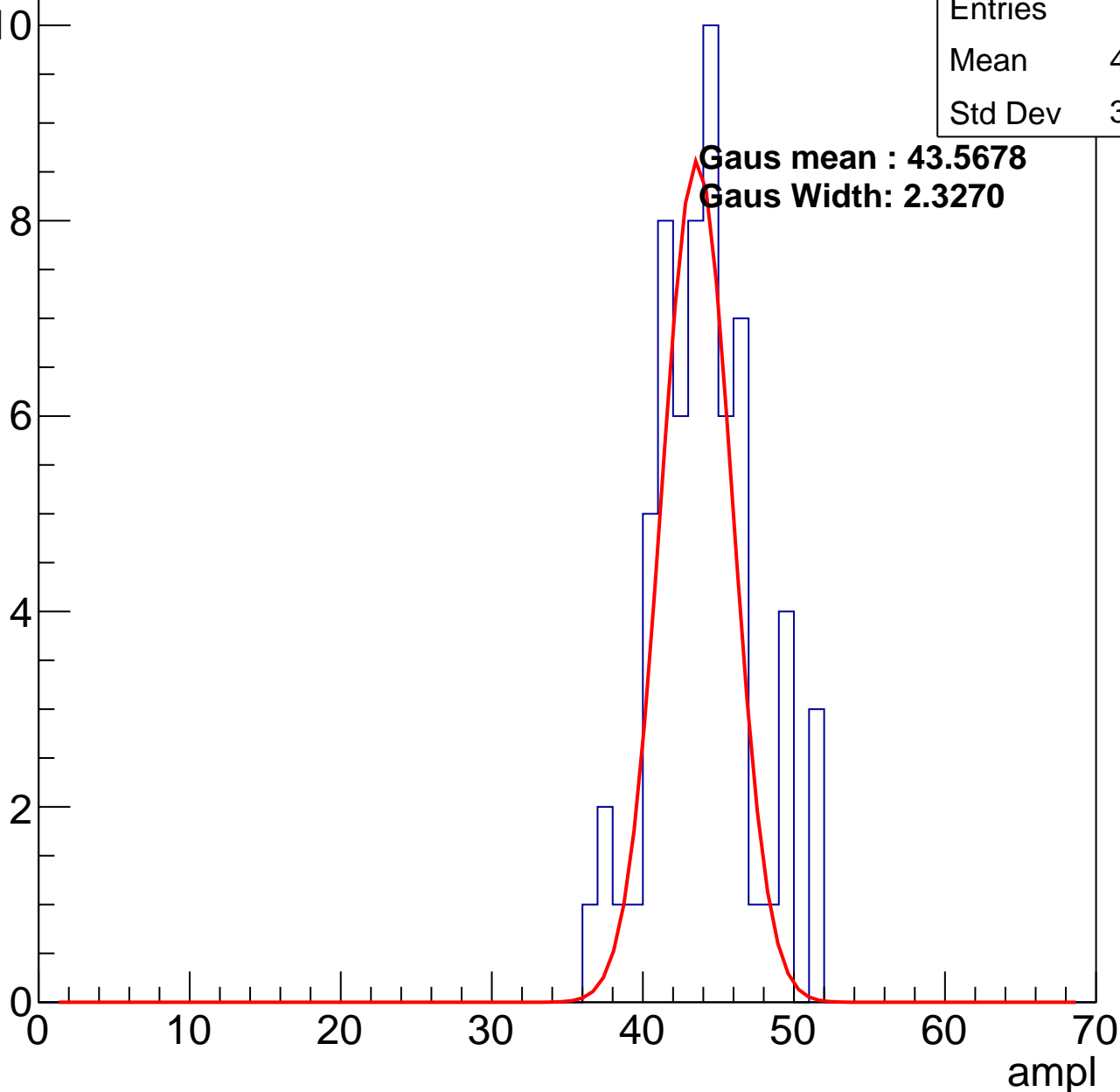
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	64
Mean	43.55
Std Dev	3.307

**Gaus mean : 43.5678**

**Gaus Width: 2.3270**

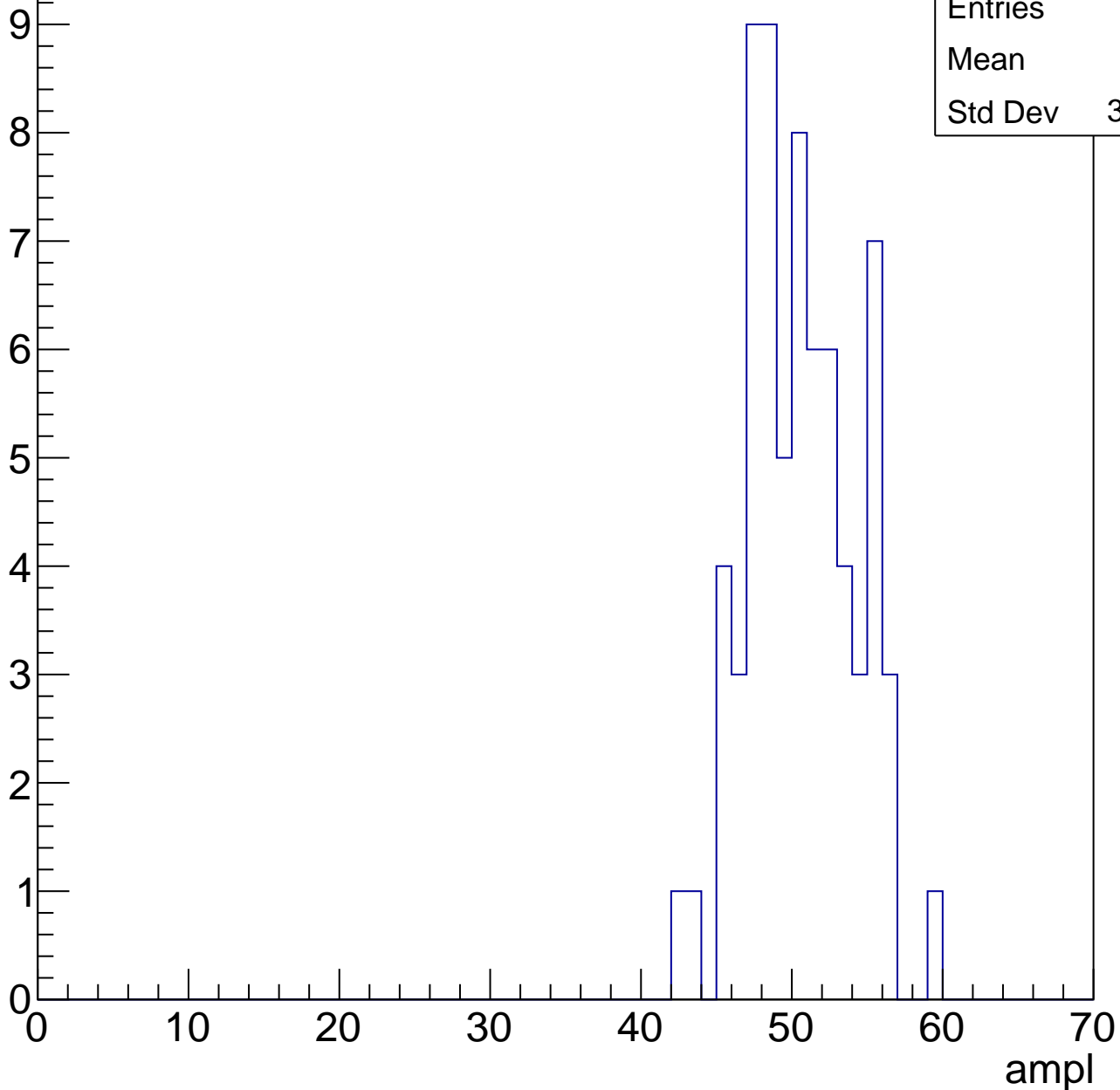


# B1L100S, U6-ch85, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

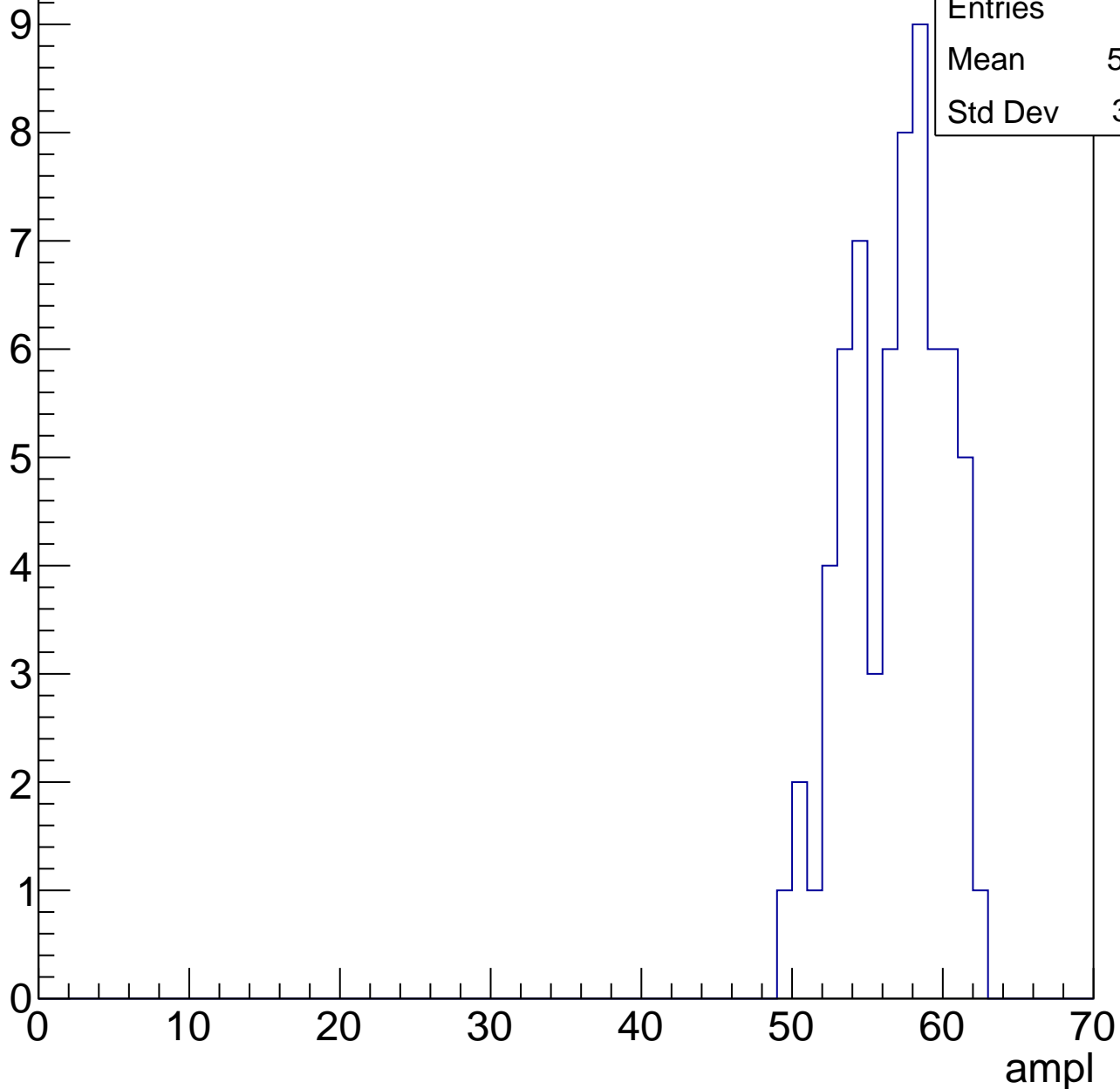
Entries	70
Mean	50.1
Std Dev	3.506



# B1L100S, U6-ch85, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

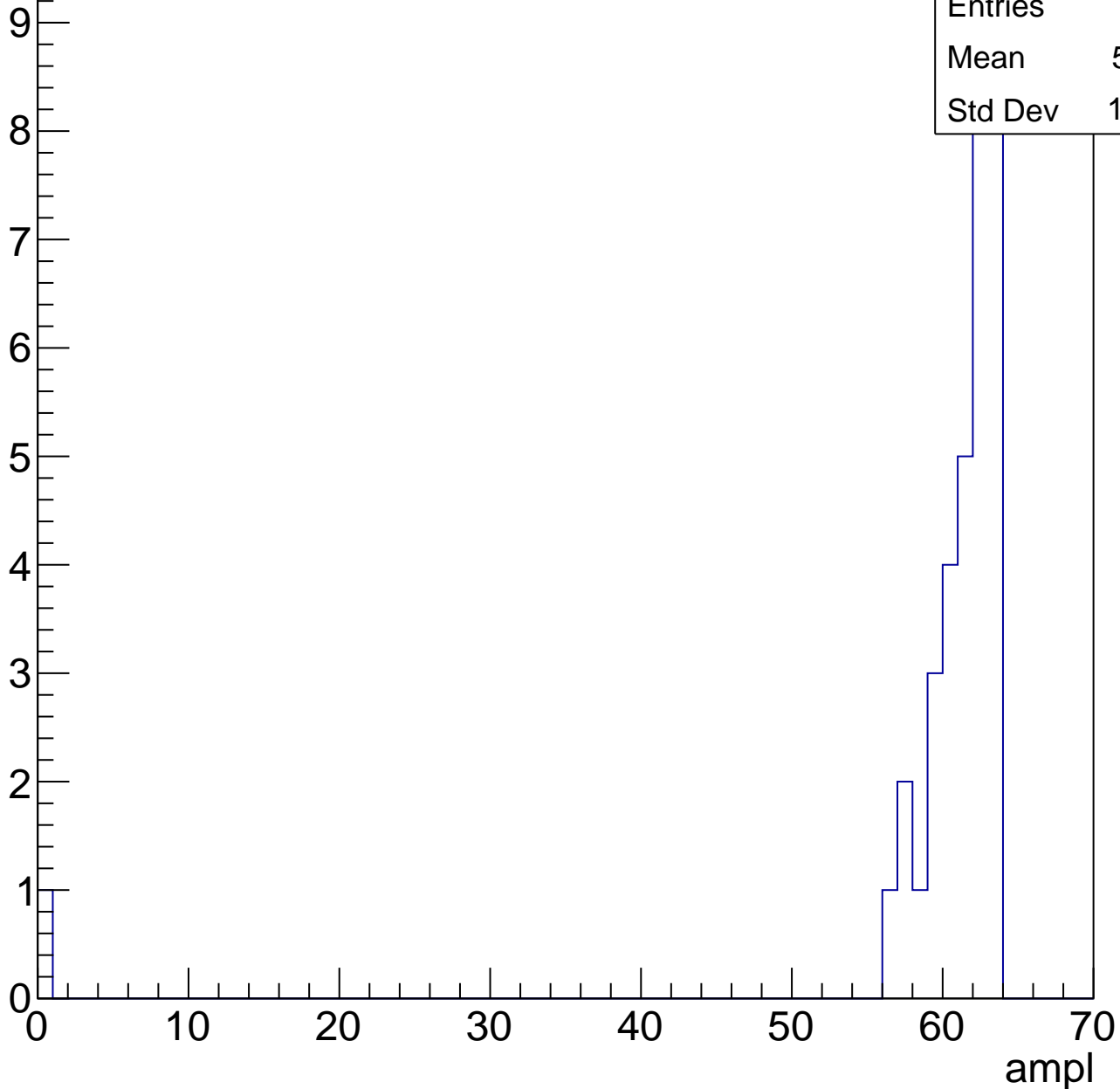


# B1L100S, U6-ch85, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	34
Mean	59.21
Std Dev	10.48



# B1L100S, U6-ch85, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry





# B1L100S, U6-ch85, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L100S, U6-ch86, adc0

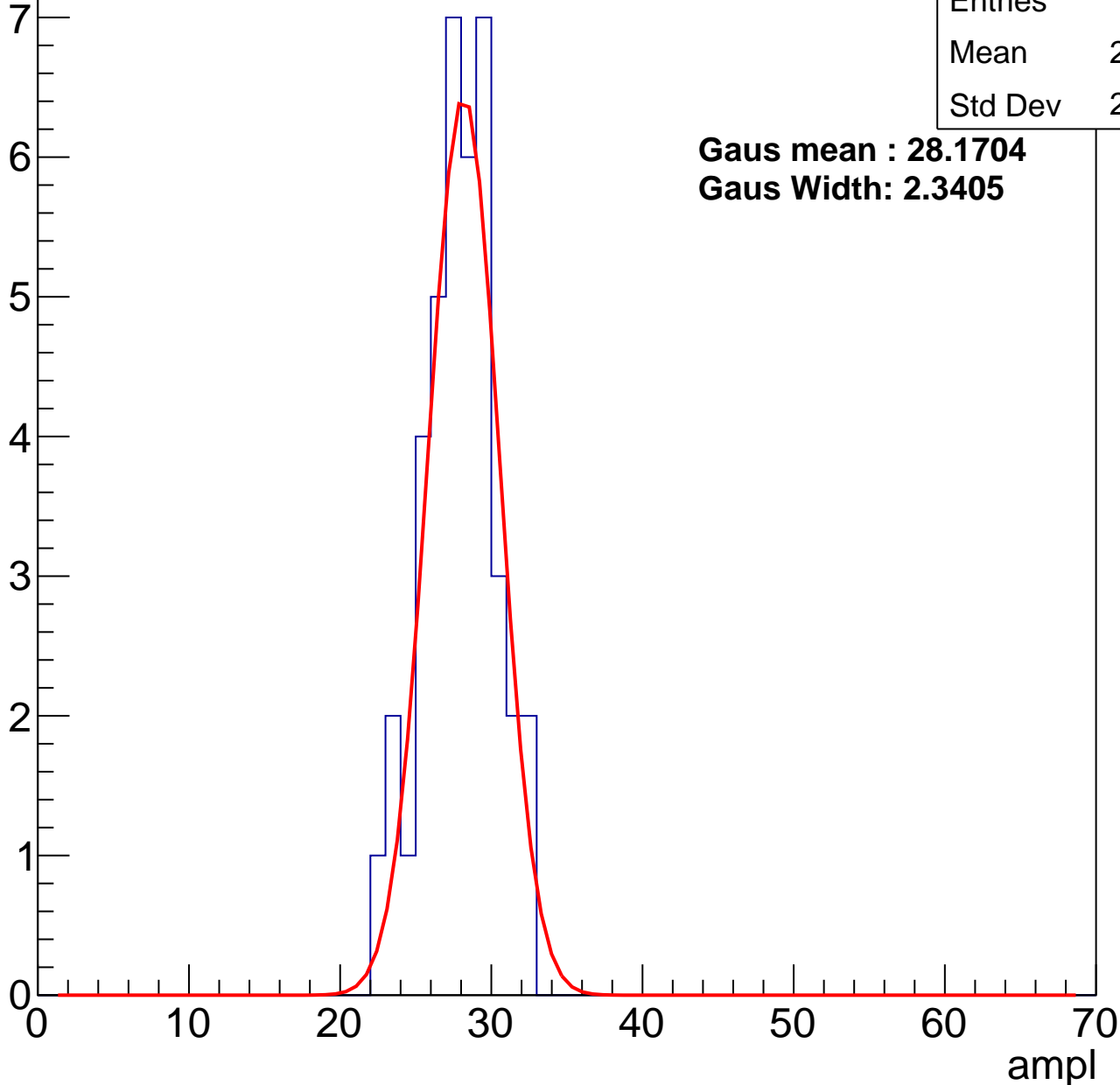
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	40
Mean	27.45
Std Dev	2.355

**Gaus mean : 28.1704**

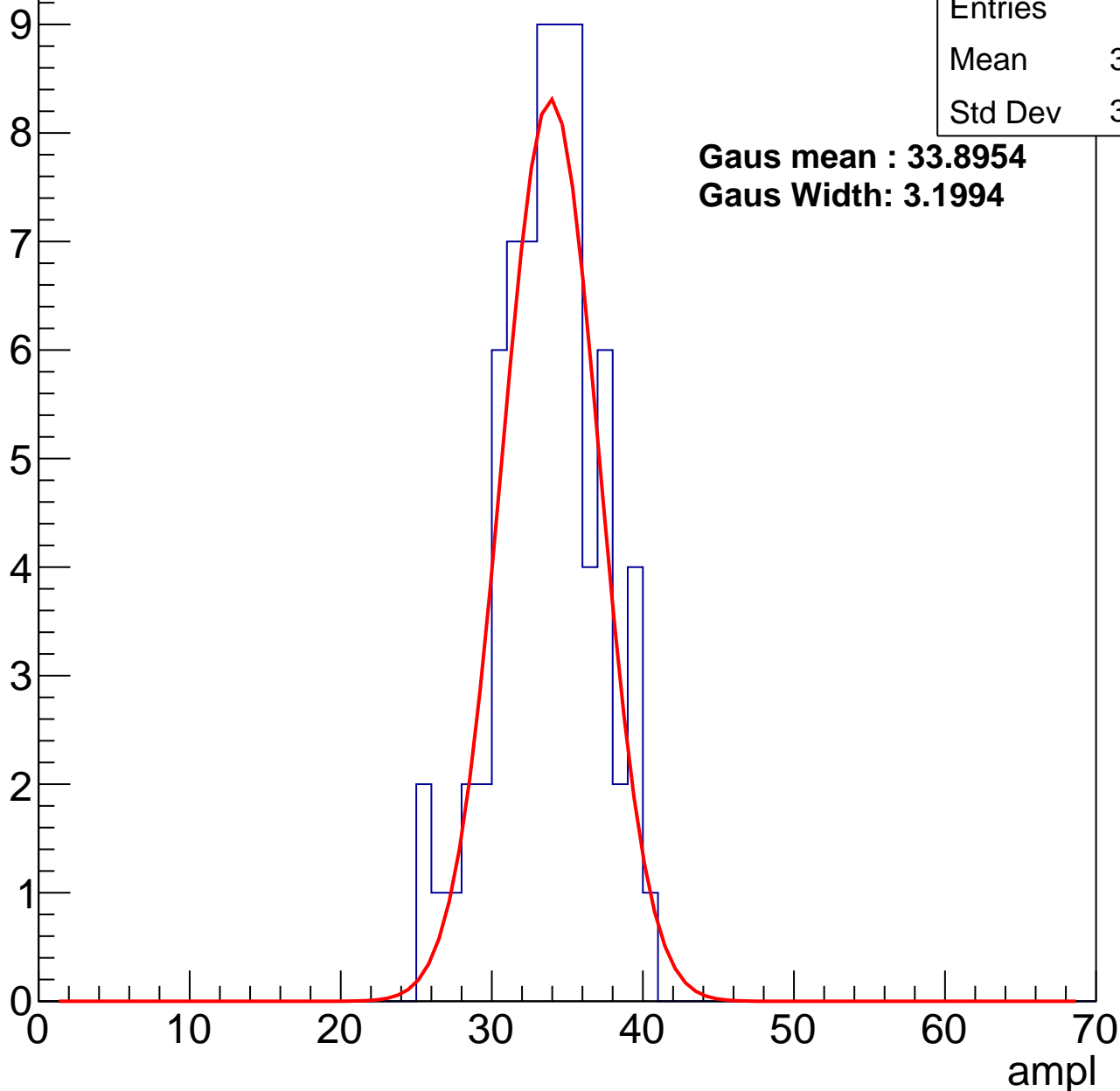
**Gaus Width: 2.3405**



# B1L100S, U6-ch86, adc1

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



# B1L100S, U6-ch86, adc2

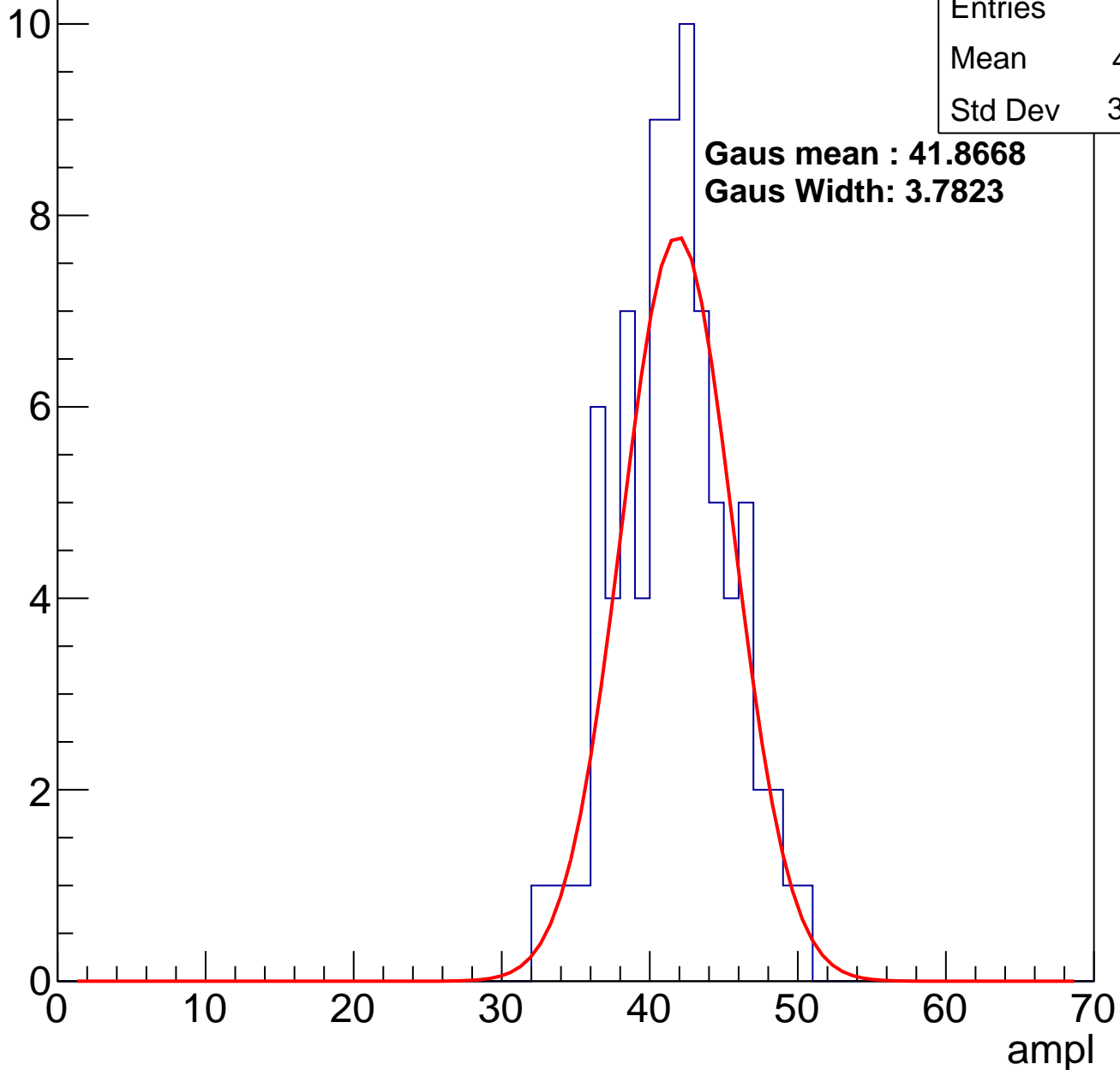
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	80
Mean	41.11
Std Dev	3.738

**Gaus mean : 41.8668**

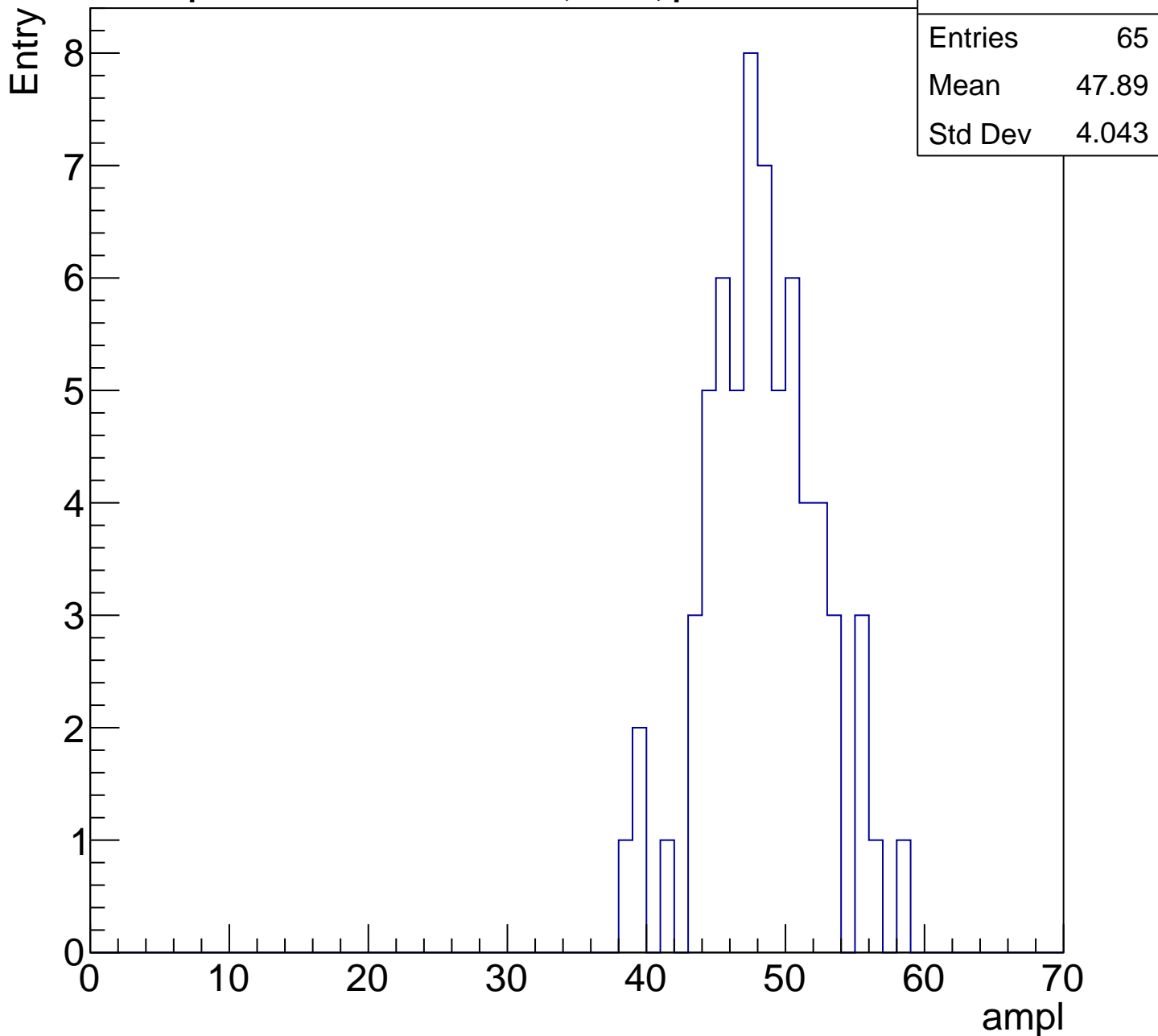
**Gaus Width: 3.7823**

Entry



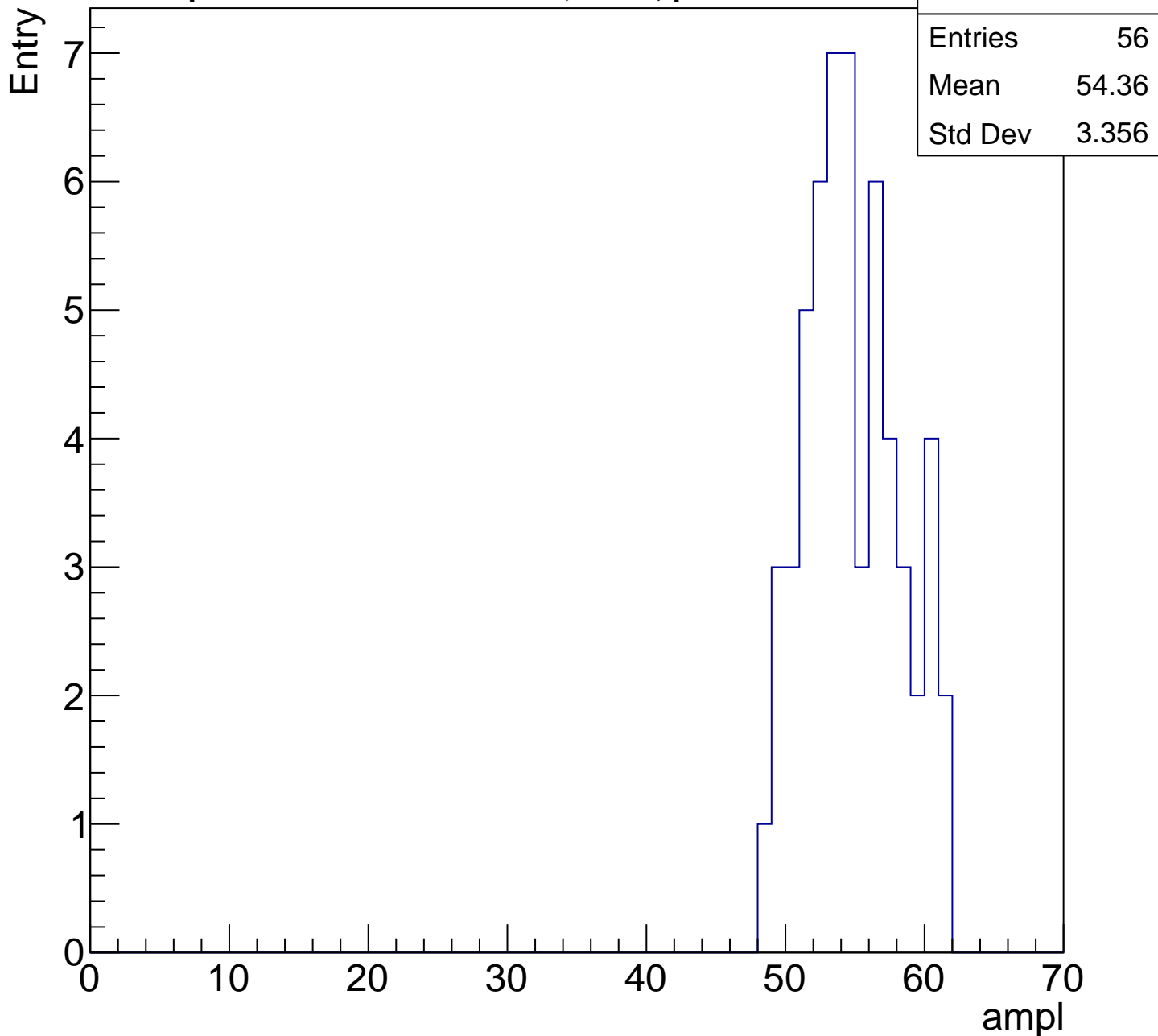
# B1L100S, U6-ch86, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2



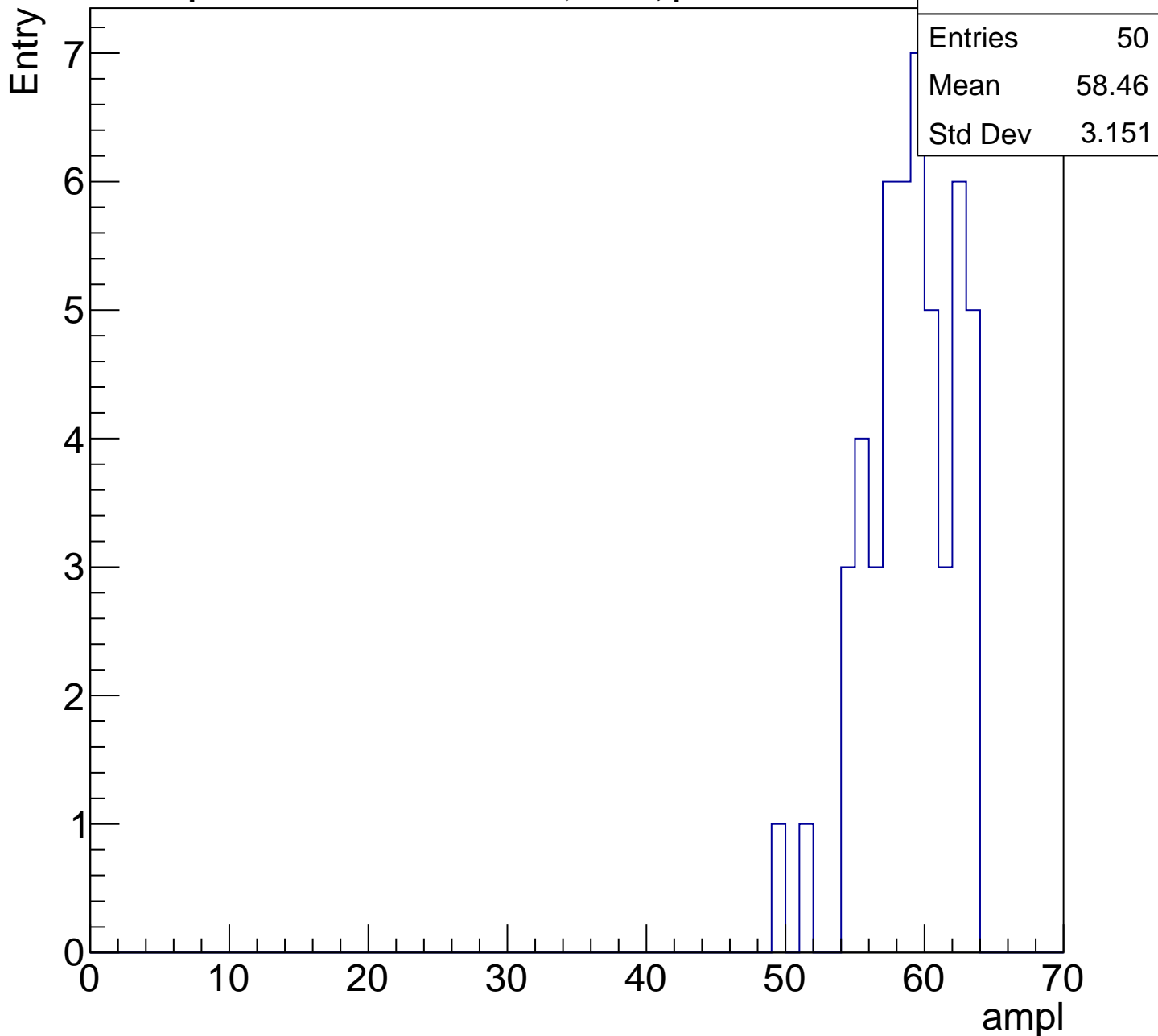
# B1L100S, U6-ch86, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2



# B1L100S, U6-ch86, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

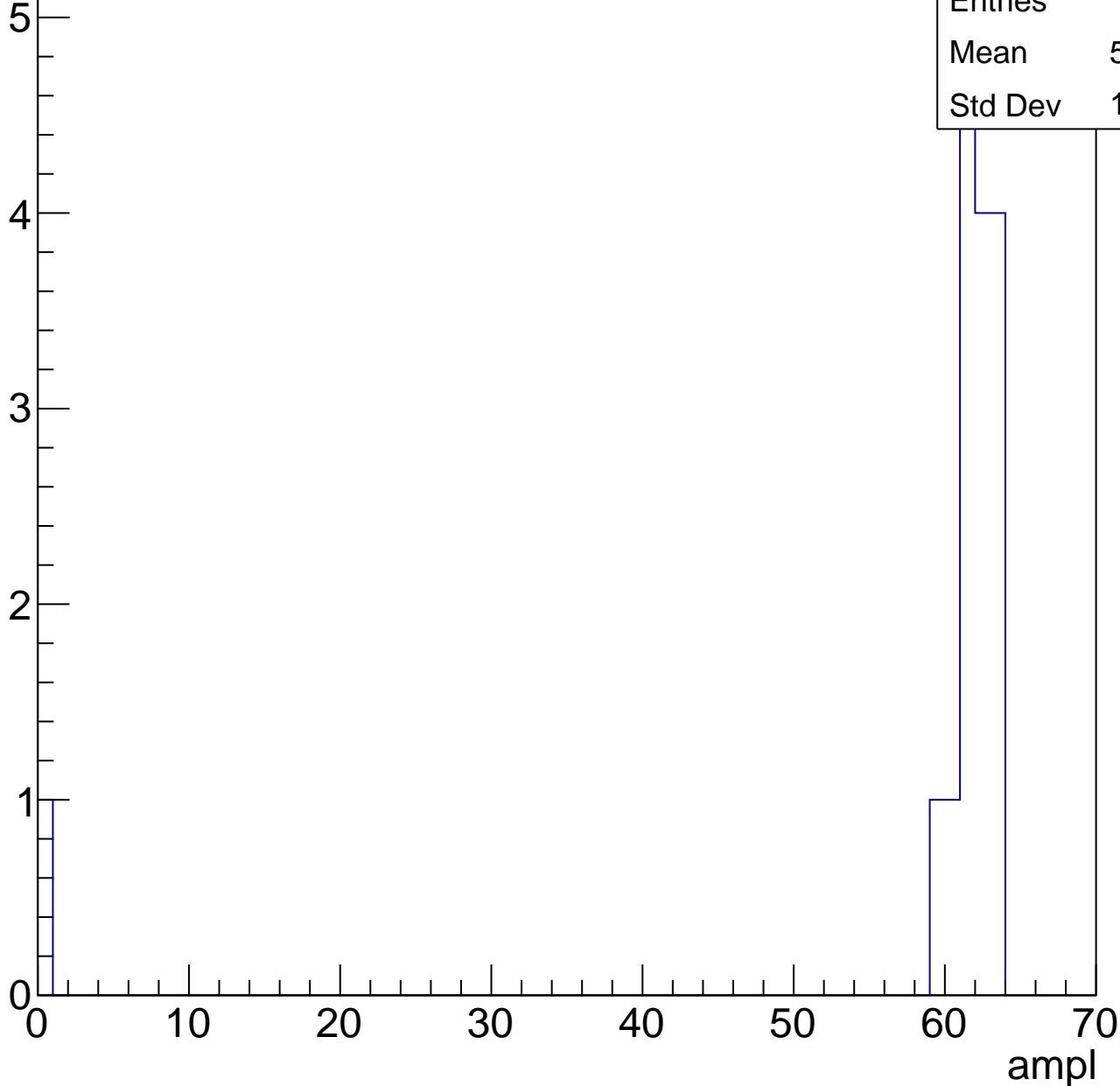


# B1L100S, U6-ch86, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	16
Mean	57.75
Std Dev	14.95





# B1L100S, U6-ch86, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



# B1L100S, U6-ch87, adc0

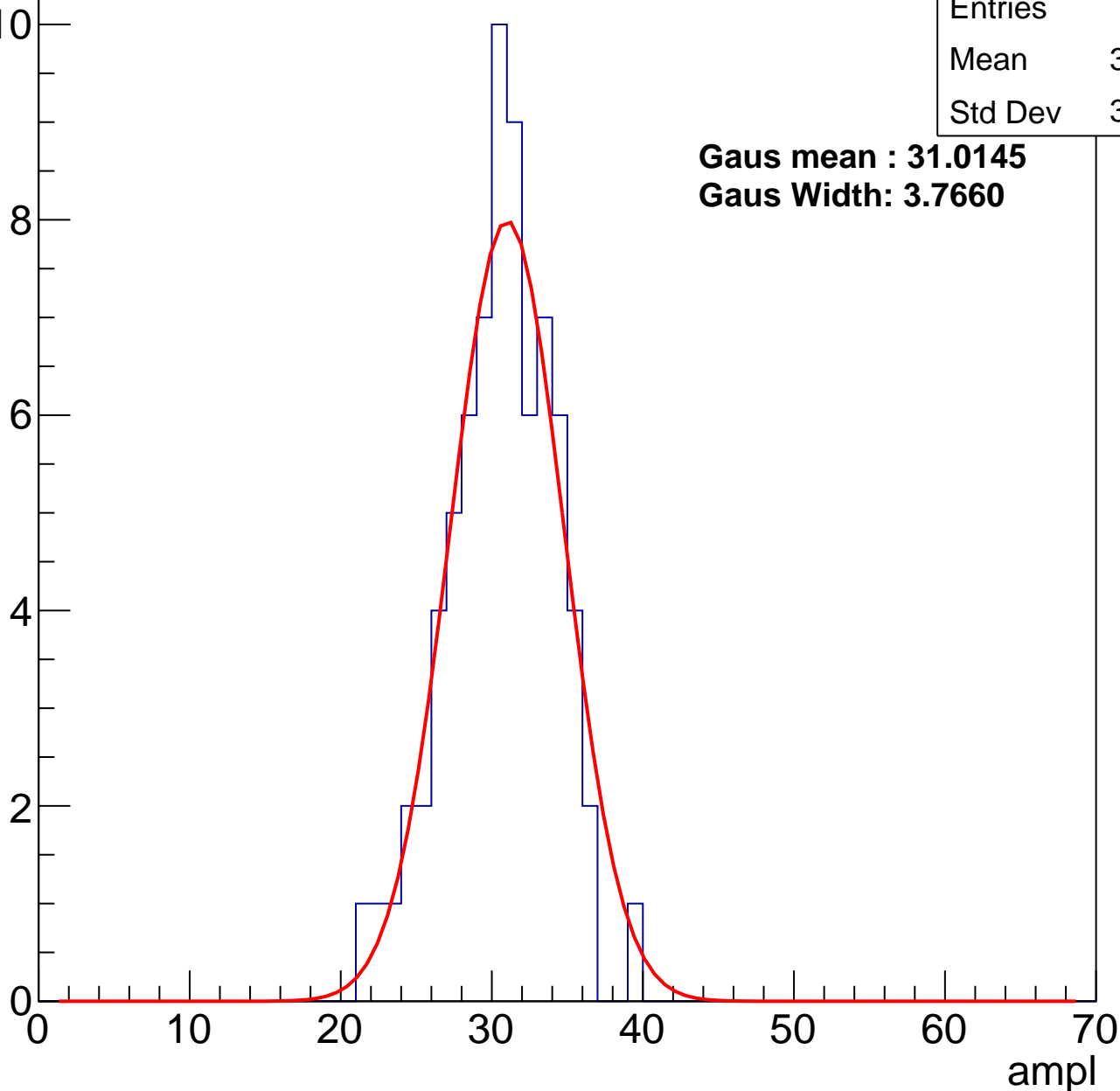
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	74
Mean	30.15
Std Dev	3.486

**Gaus mean : 31.0145**

**Gaus Width: 3.7660**



# B1L100S, U6-ch87, adc1

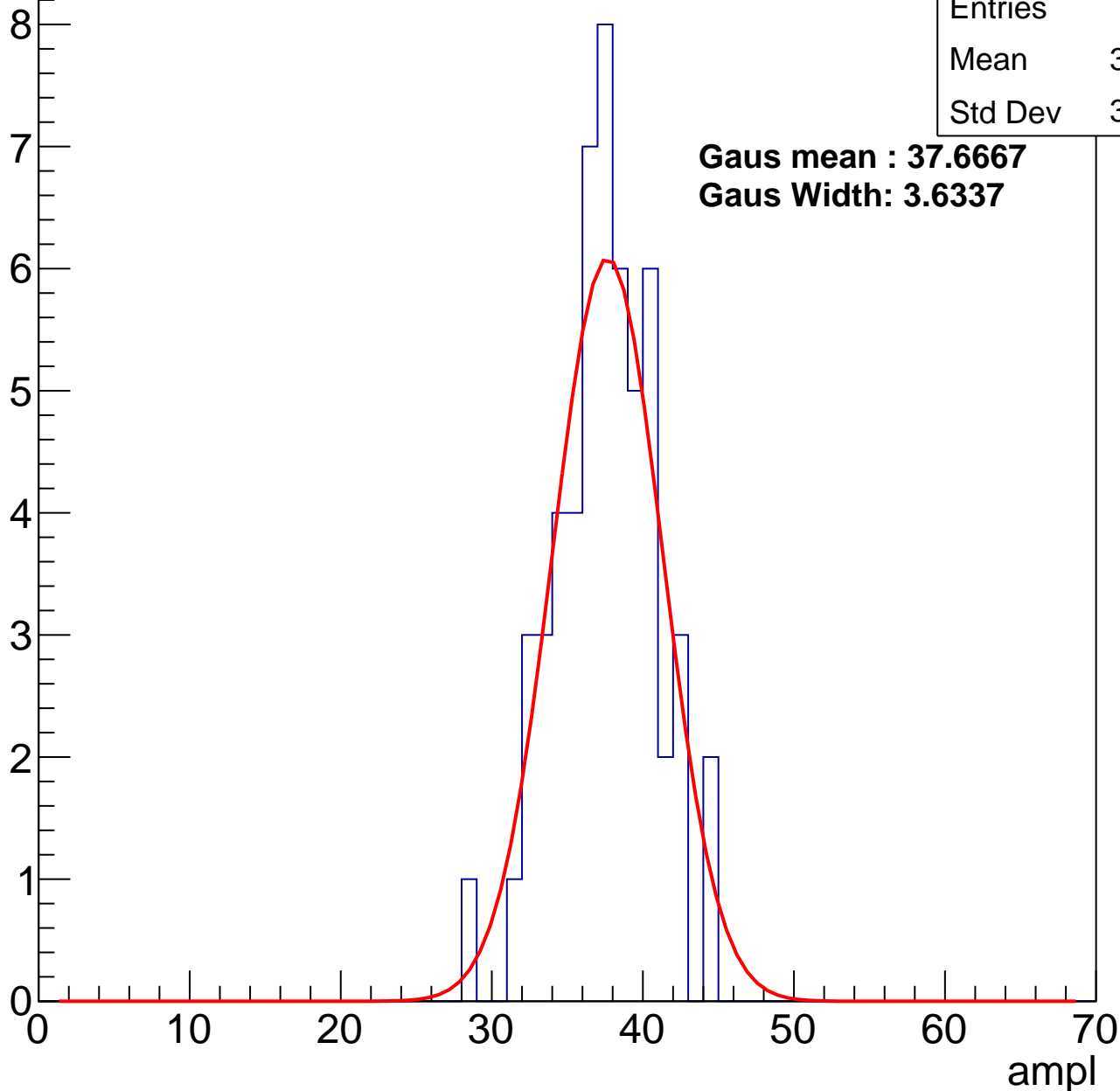
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	55
Mean	37.04
Std Dev	3.258

**Gaus mean : 37.6667**

**Gaus Width: 3.6337**



# B1L100S, U6-ch87, adc2

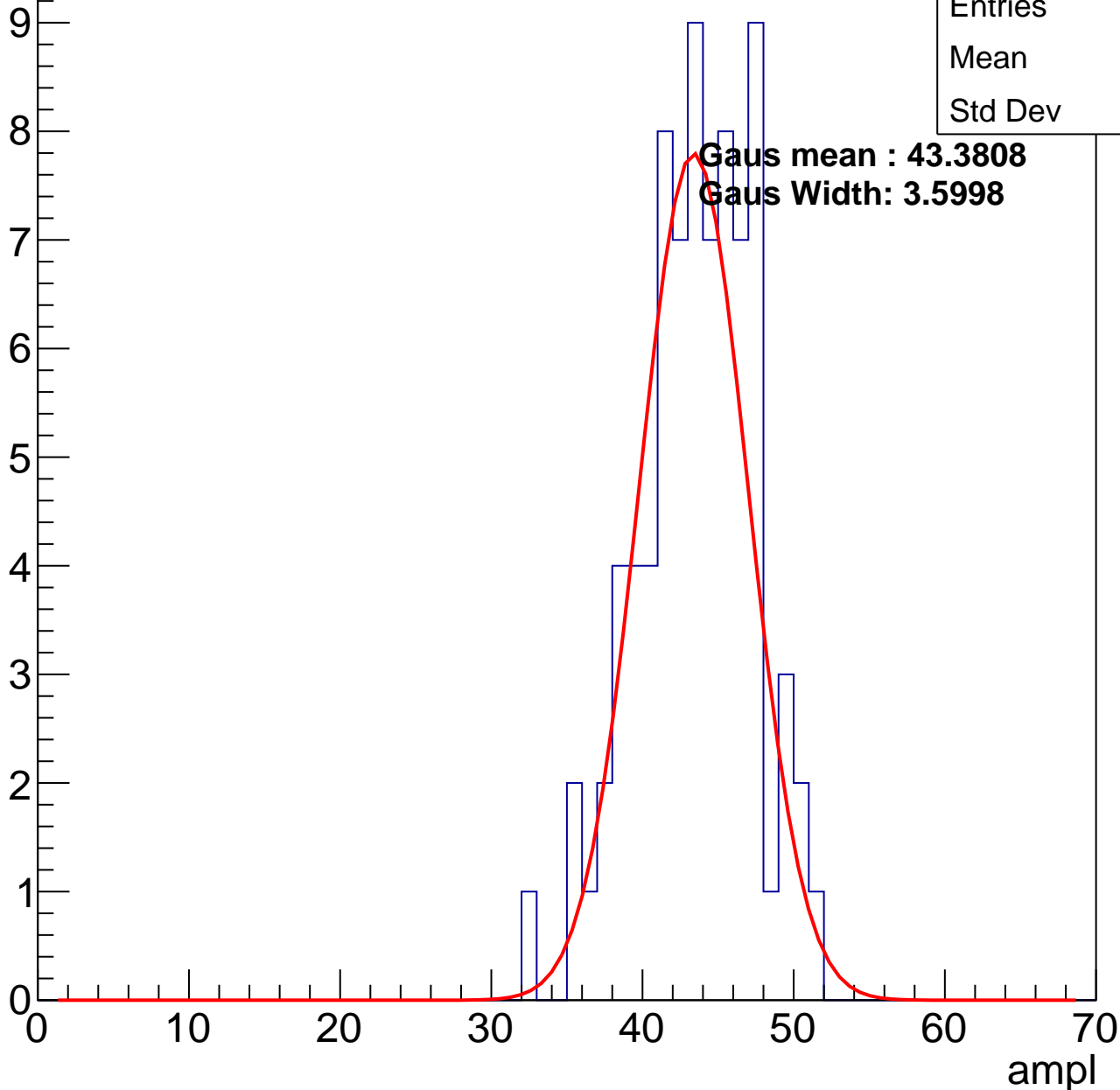
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	80
Mean	43.1
Std Dev	3.79

**Gaus mean : 43.3808**

**Gaus Width: 3.5998**

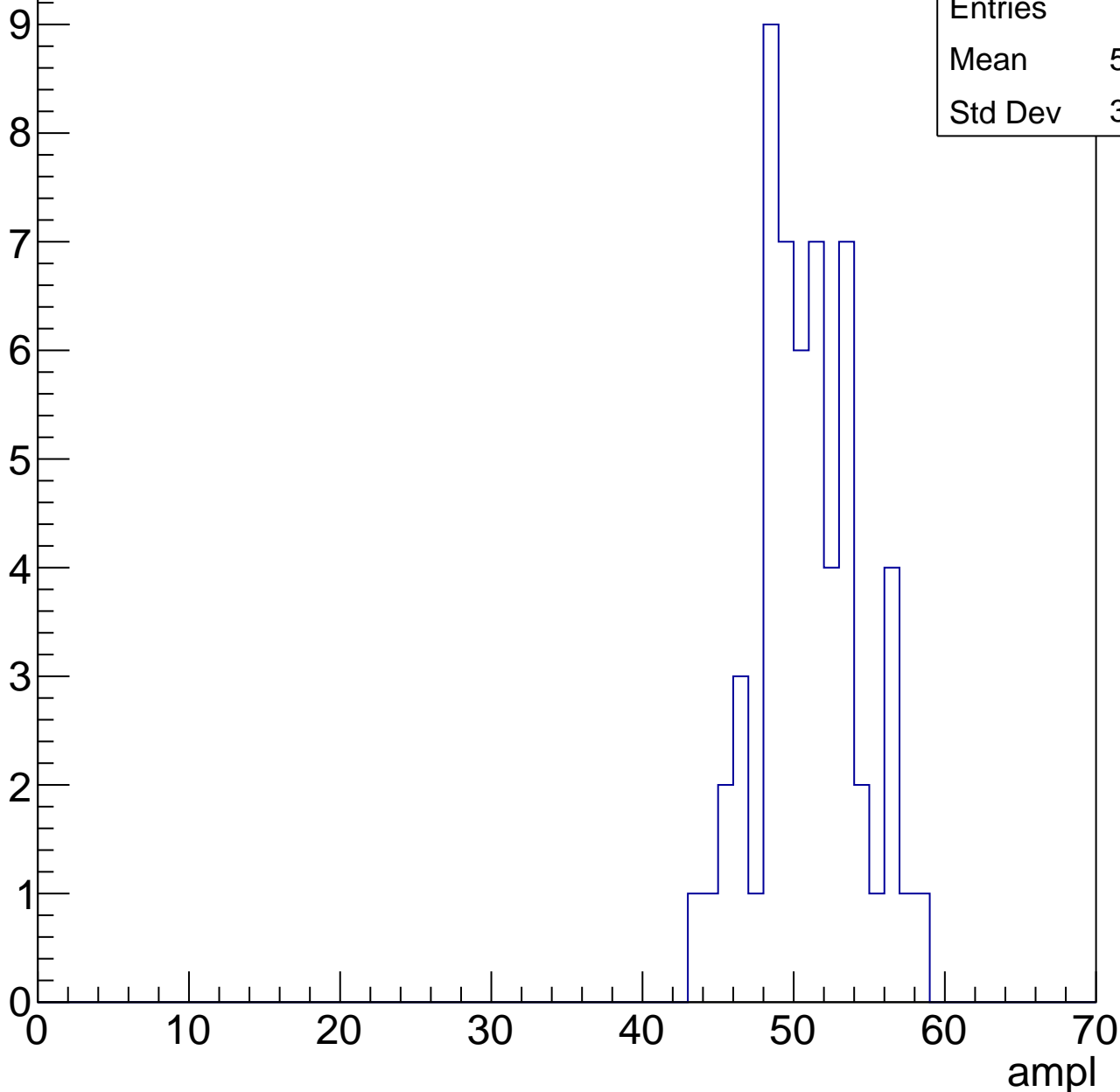


# B1L100S, U6-ch87, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

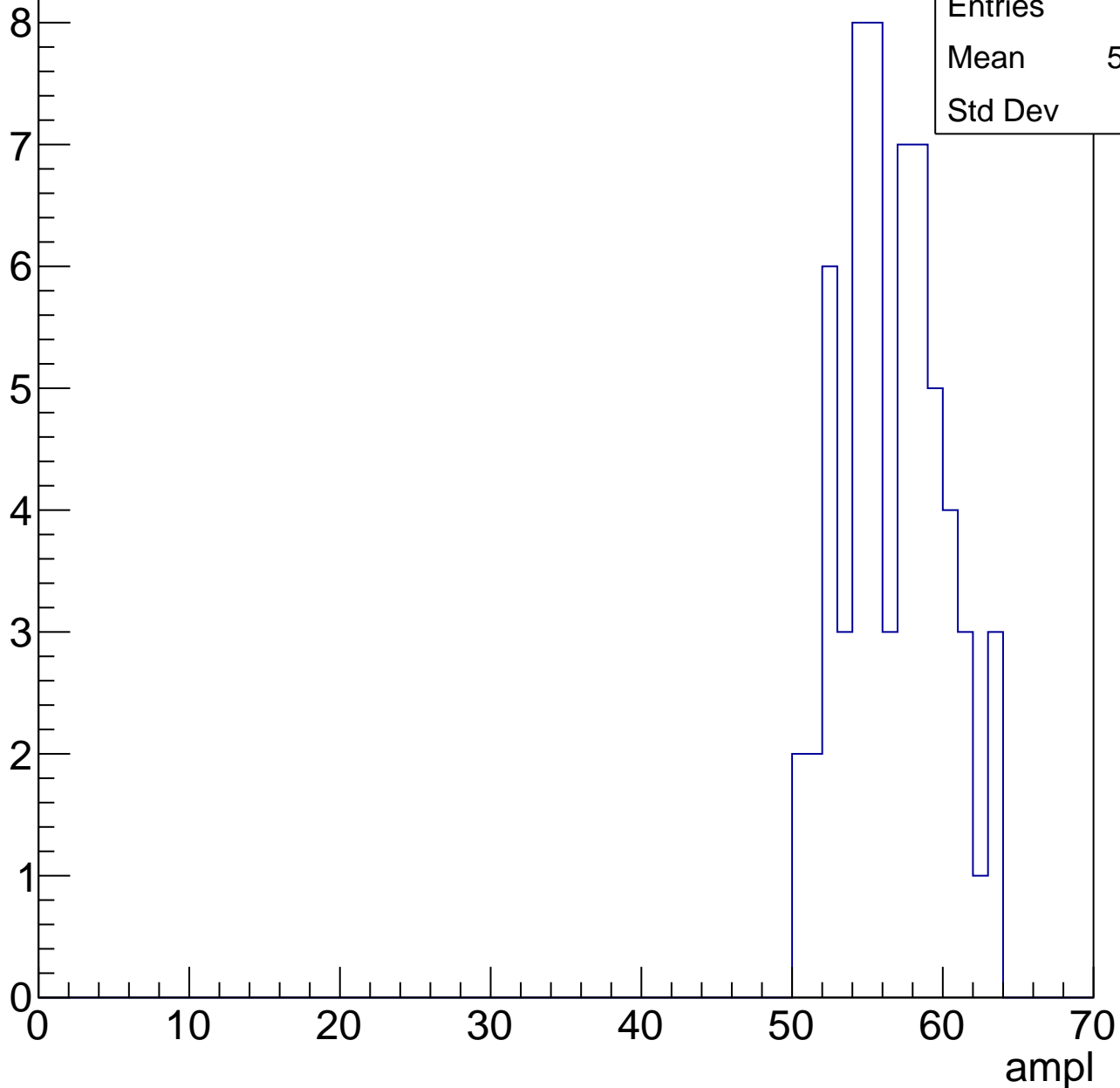
Entries	57
Mean	50.44
Std Dev	3.309



# B1L100S, U6-ch87, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

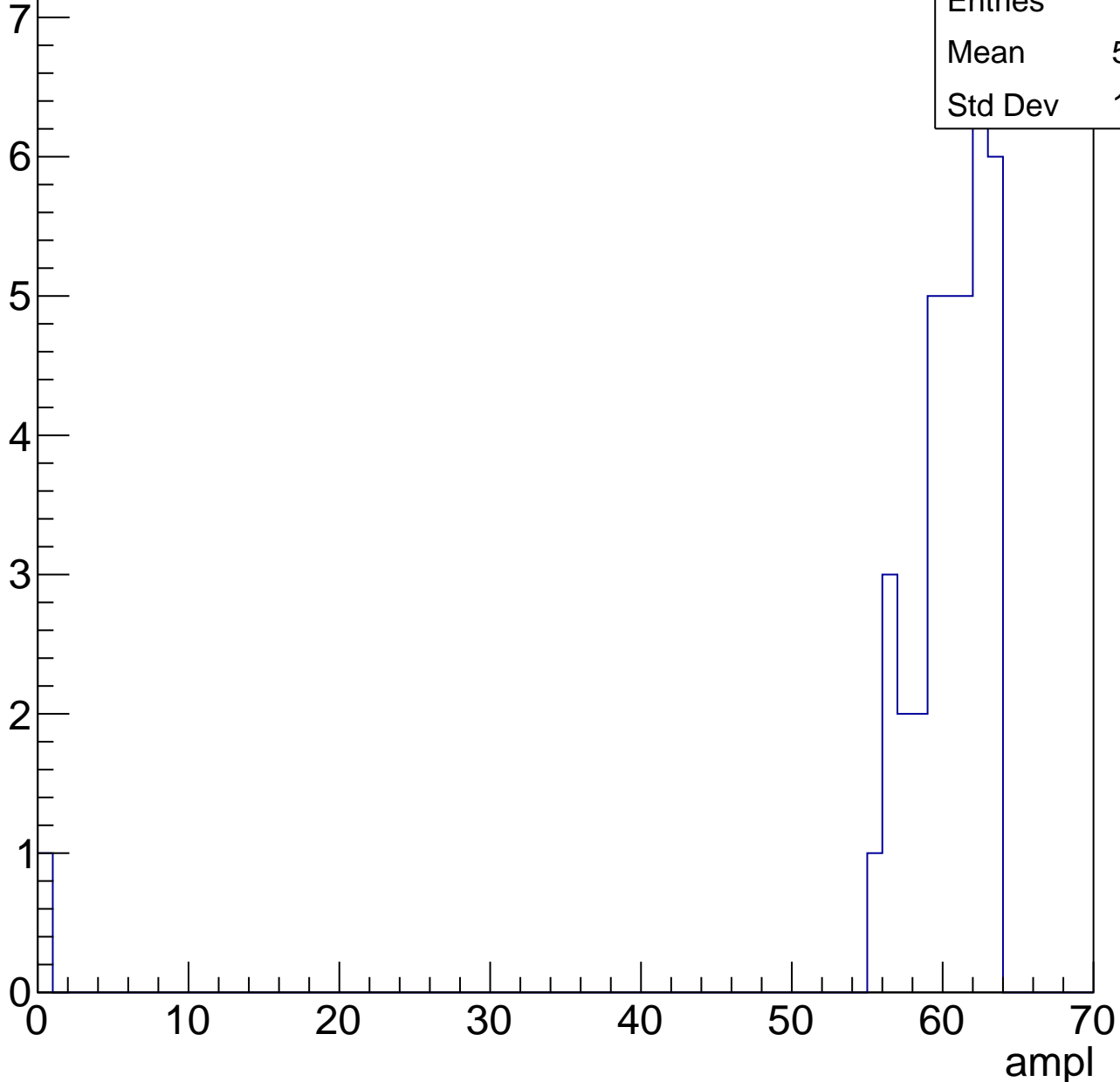


# B1L100S, U6-ch87, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	37
Mean	58.51
Std Dev	10.01



# B1L100S, U6-ch87, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	6
Mean	61.5
Std Dev	0.9574

ampl

0 10 20 30 40 50 60 70



# B1L100S, U6-ch87, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



# B1L100S, U6-ch88, adc0

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	66
Mean	26.94
Std Dev	4.635

**Gaus mean : 27.9808**

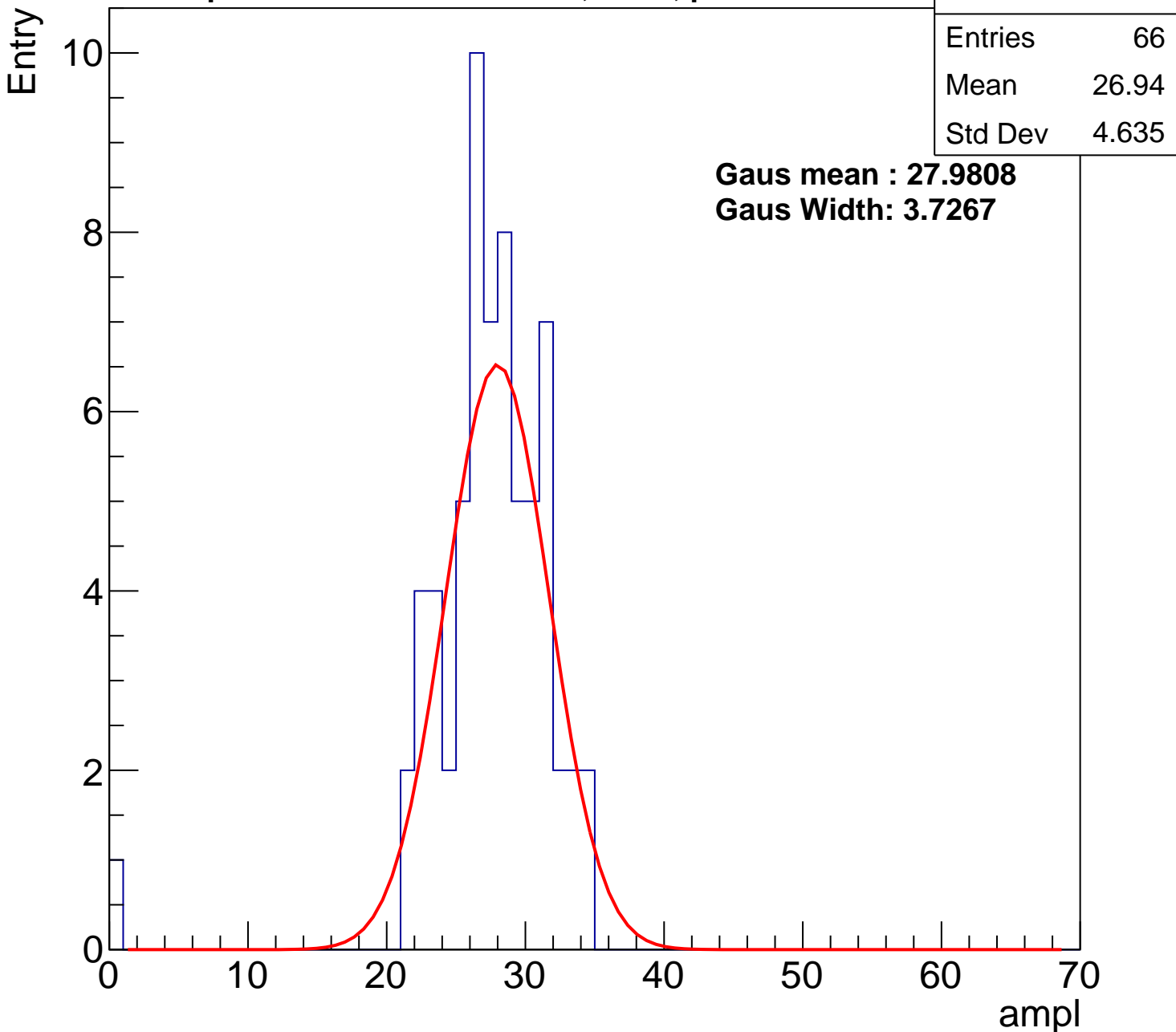
**Gaus Width: 3.7267**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L100S, U6-ch88, adc1

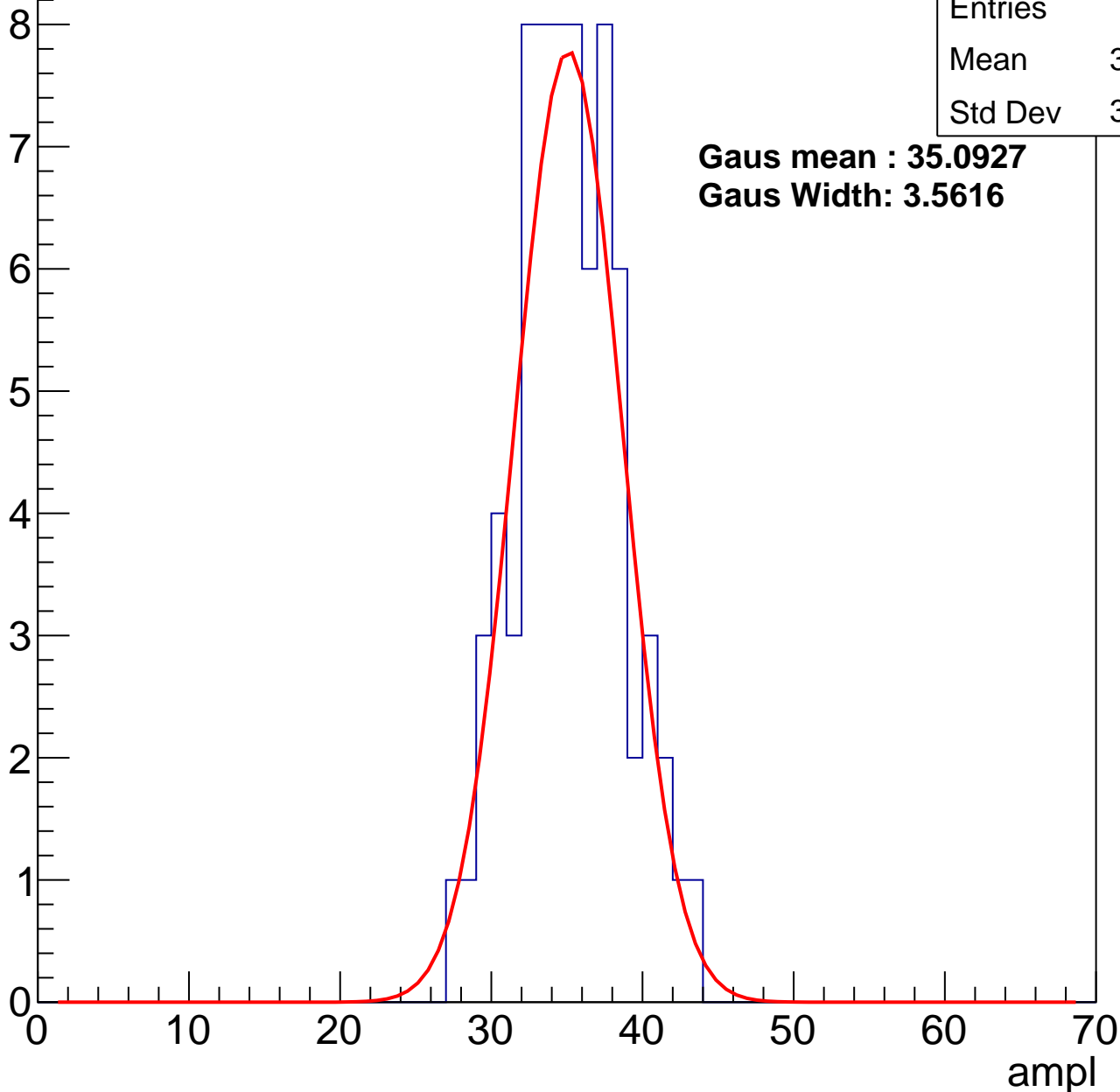
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	73
Mean	34.68
Std Dev	3.428

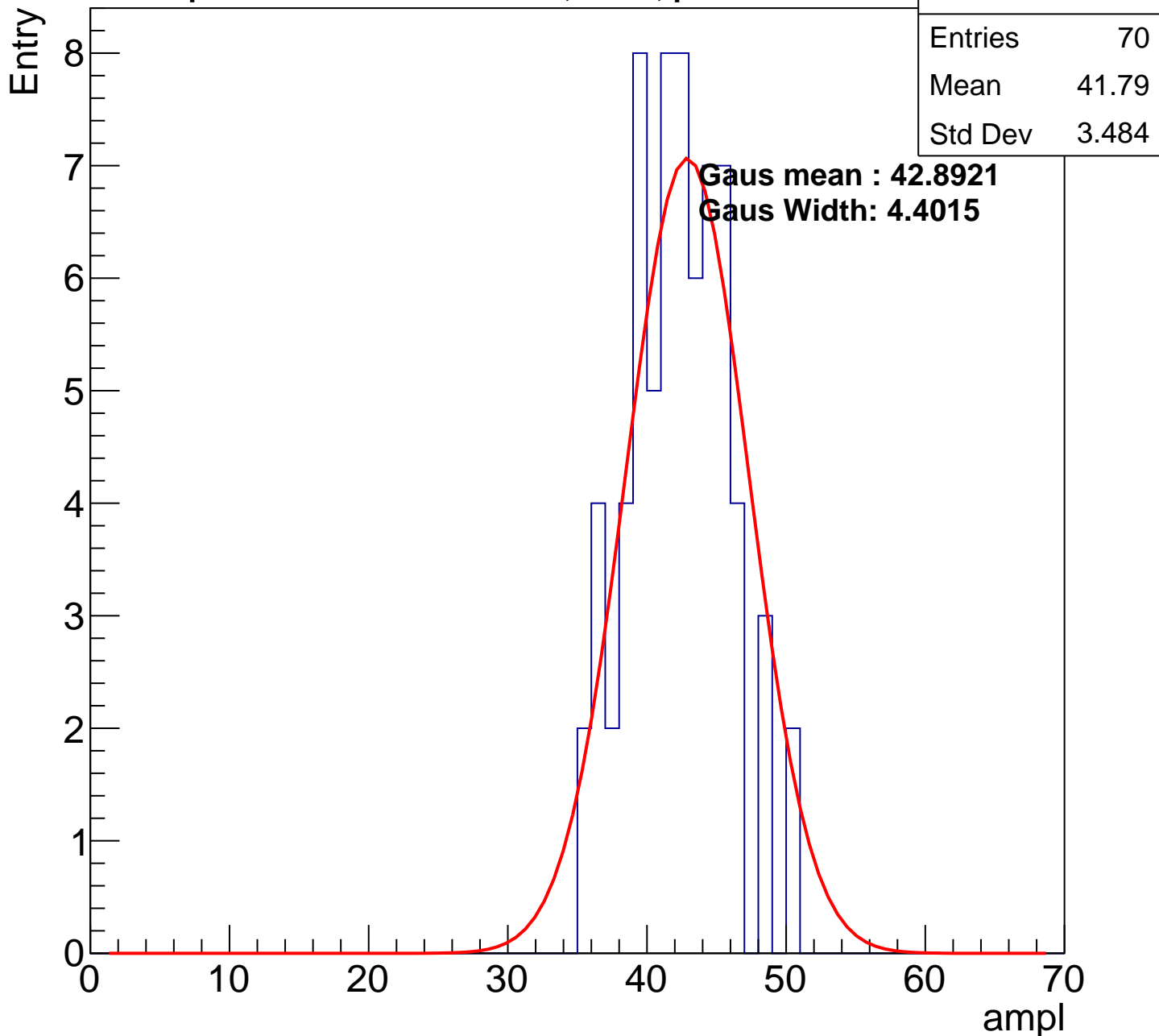
**Gaus mean : 35.0927**

**Gaus Width: 3.5616**



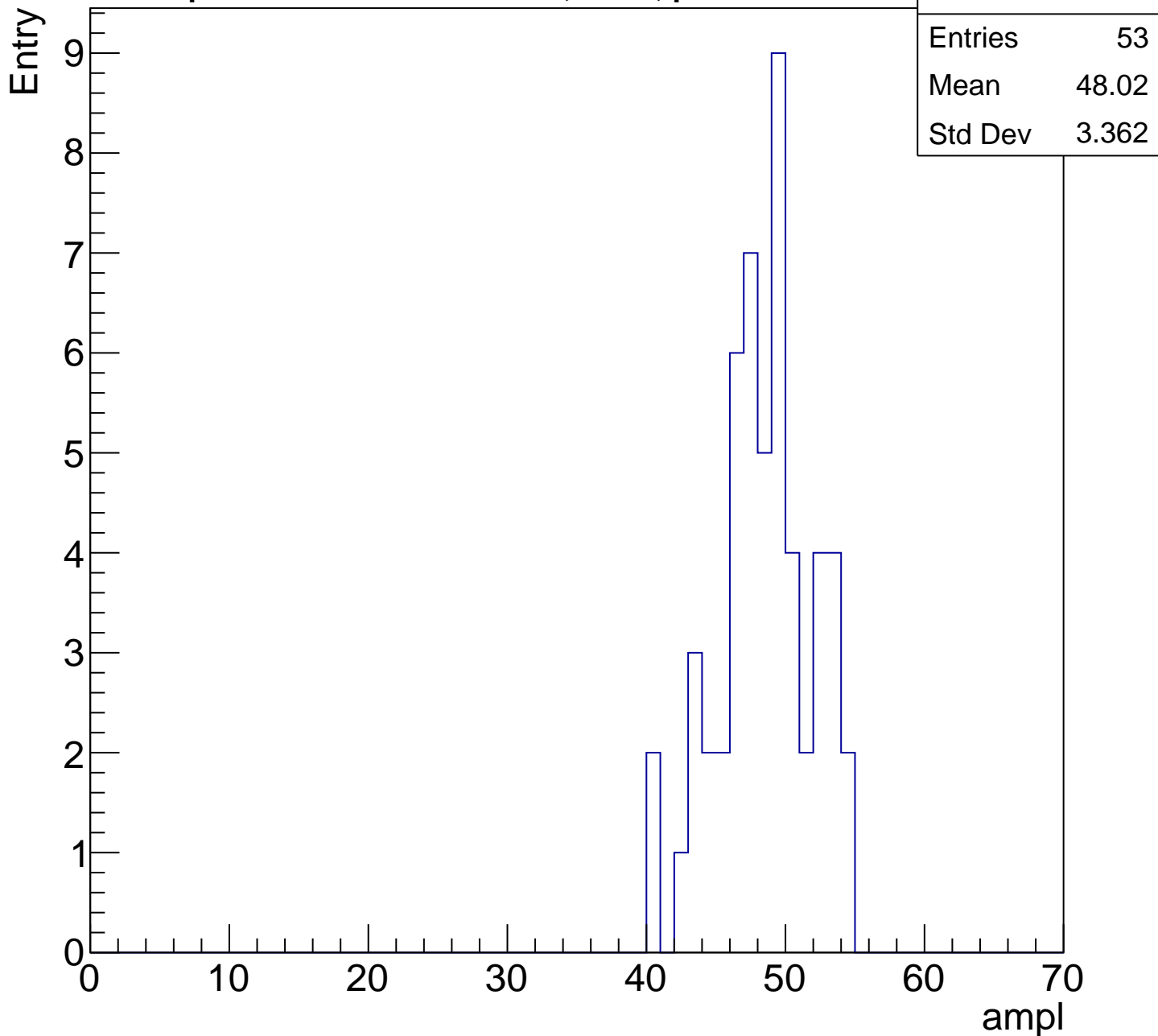
# B1L100S, U6-ch88, adc2

calib\_packv5\_042523\_0143.root, FC#4, port A2



# B1L100S, U6-ch88, adc3

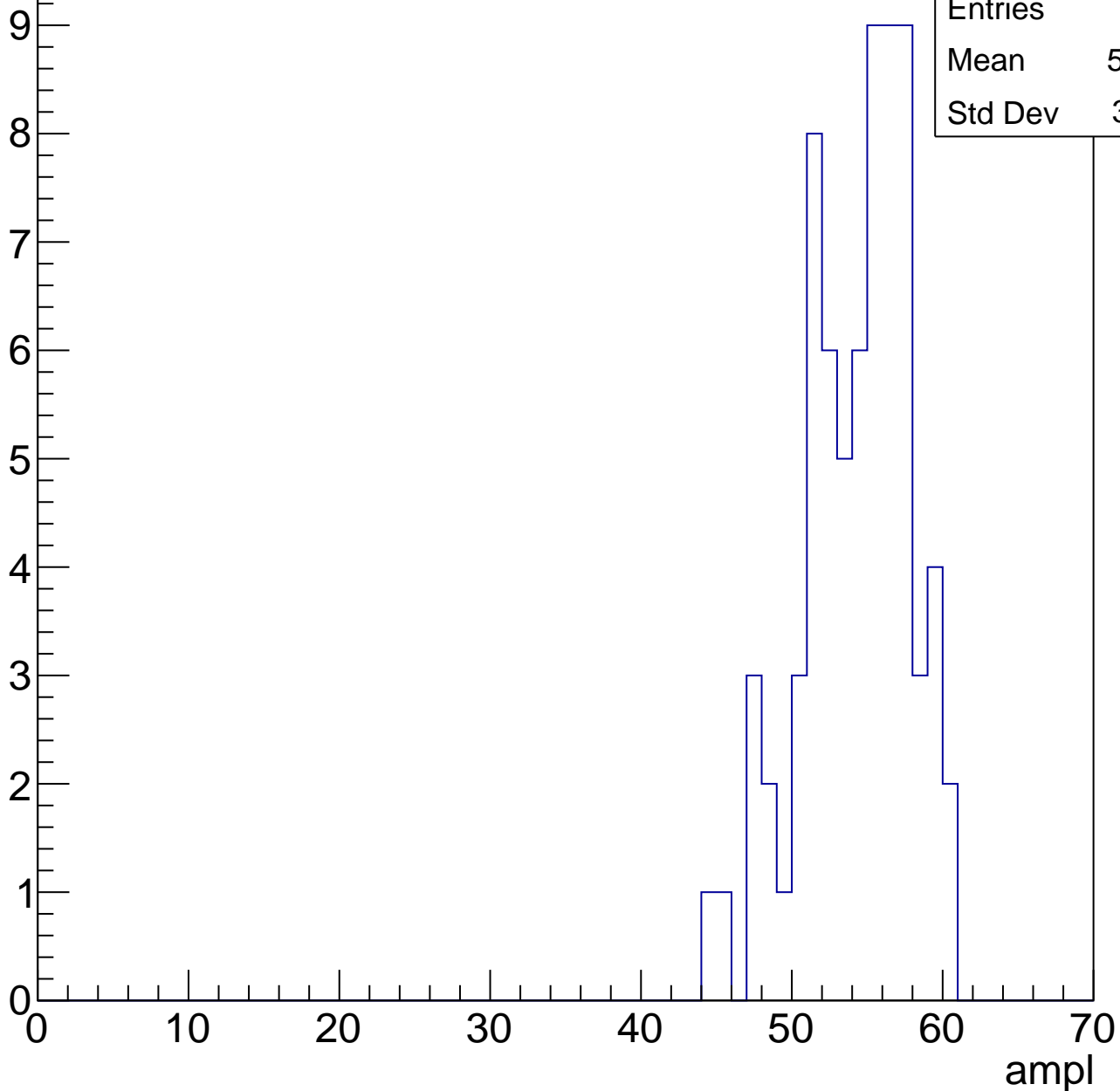
calib\_packv5\_042523\_0143.root, FC#4, port A2



# B1L100S, U6-ch88, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

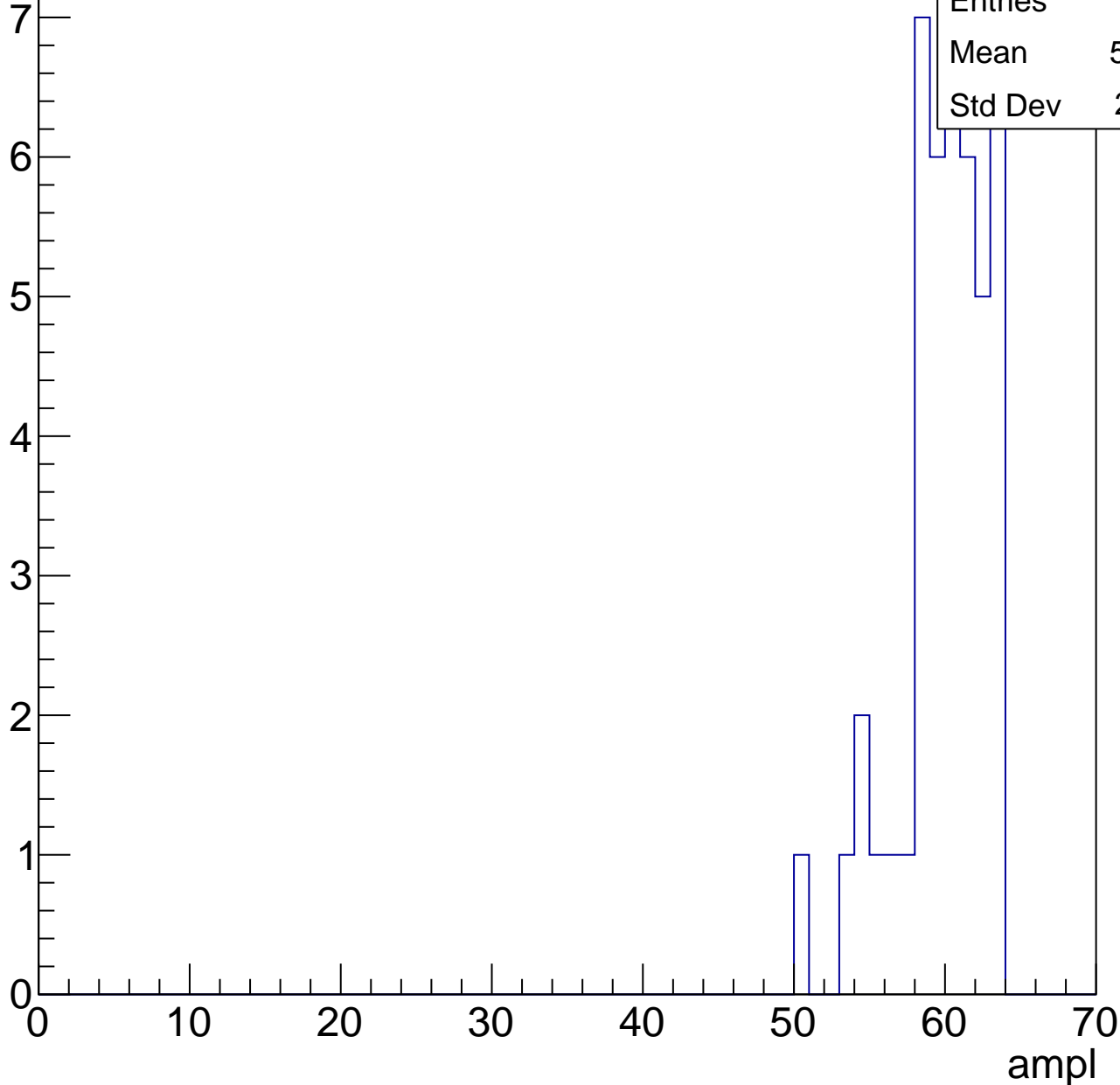
Entry



# B1L100S, U6-ch88, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

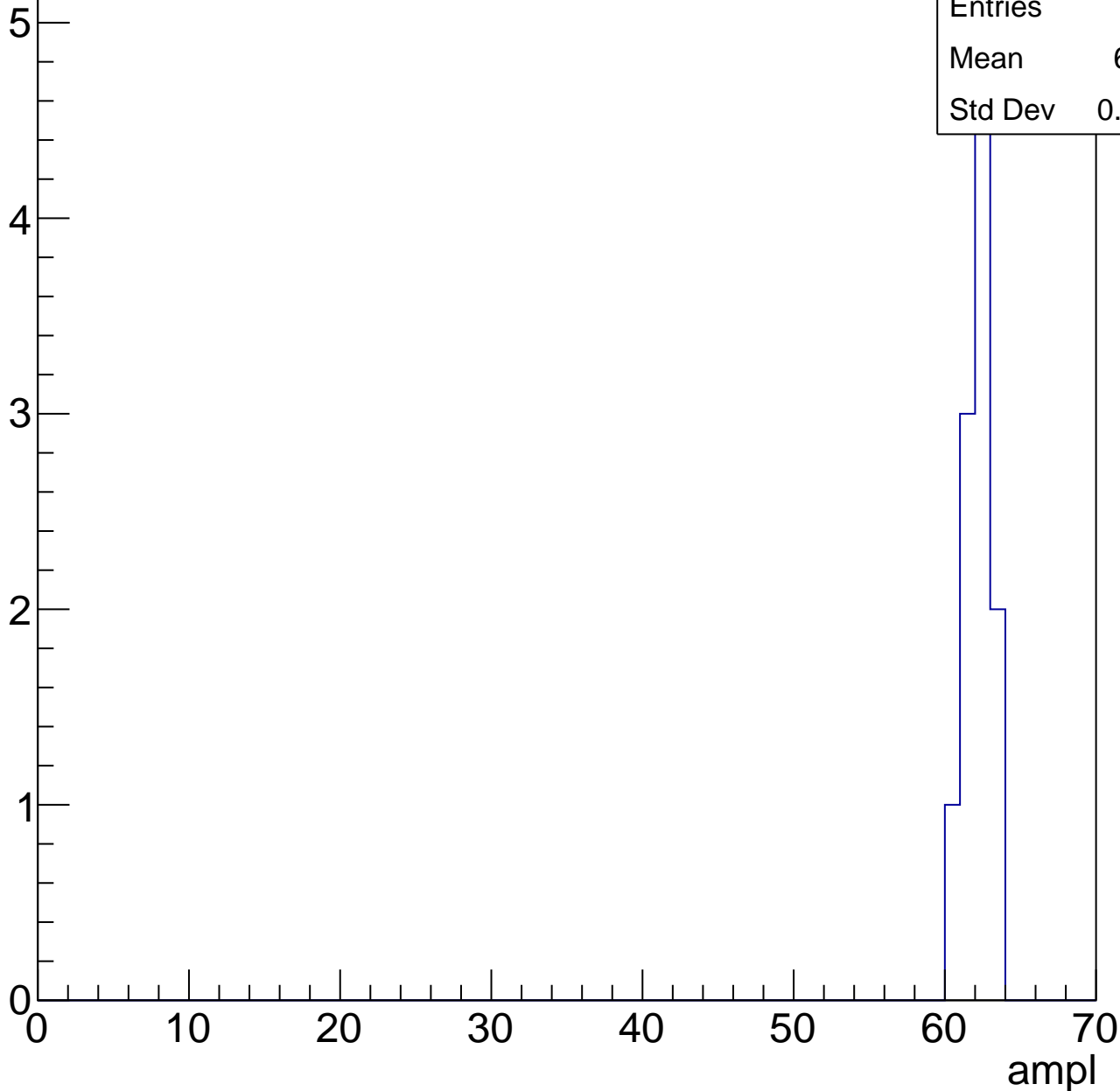


# B1L100S, U6-ch88, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	11
Mean	61.73
Std Dev	0.8624

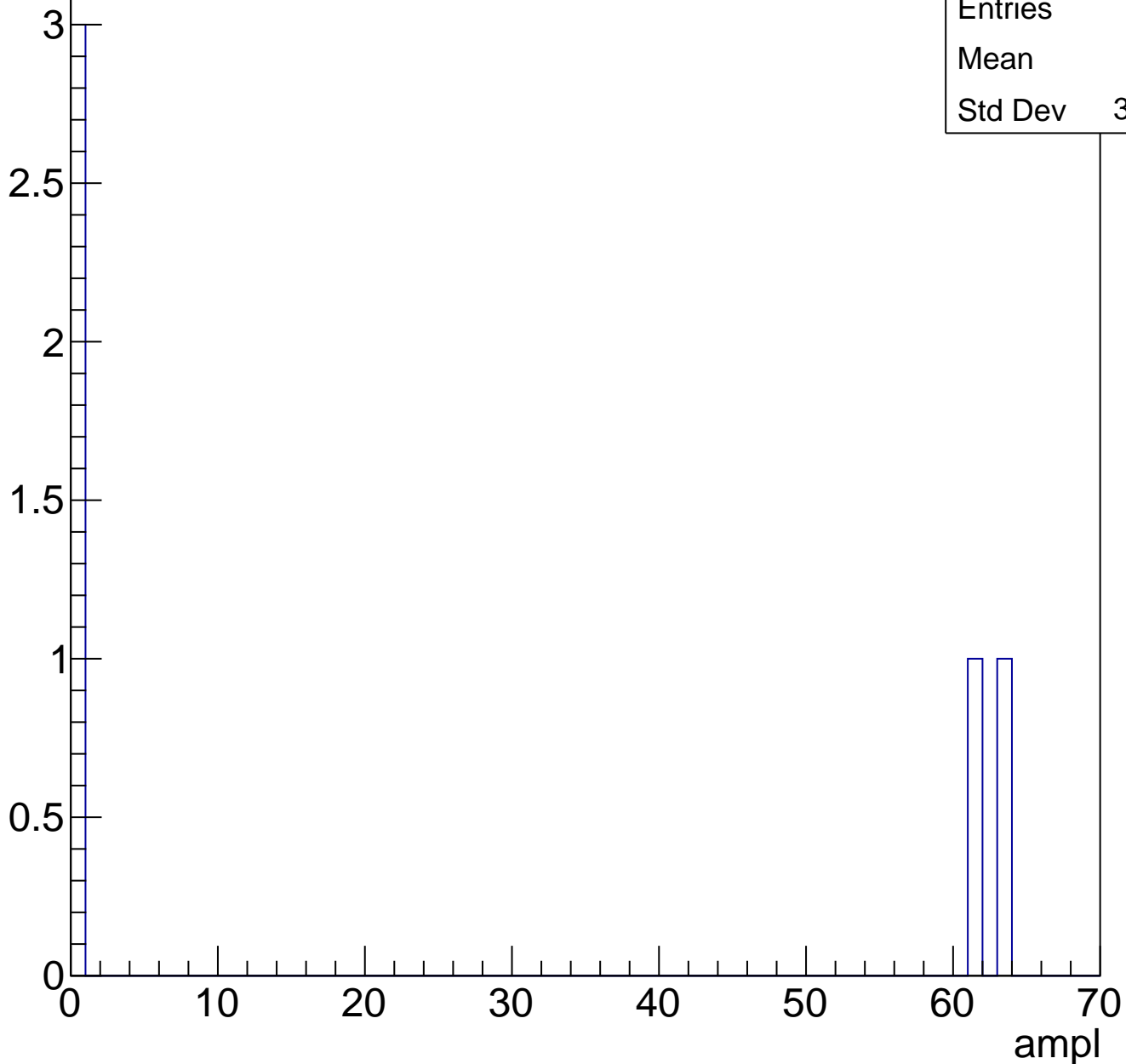




# B1L100S, U6-ch88, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



# B1L100S, U6-ch89, adc0

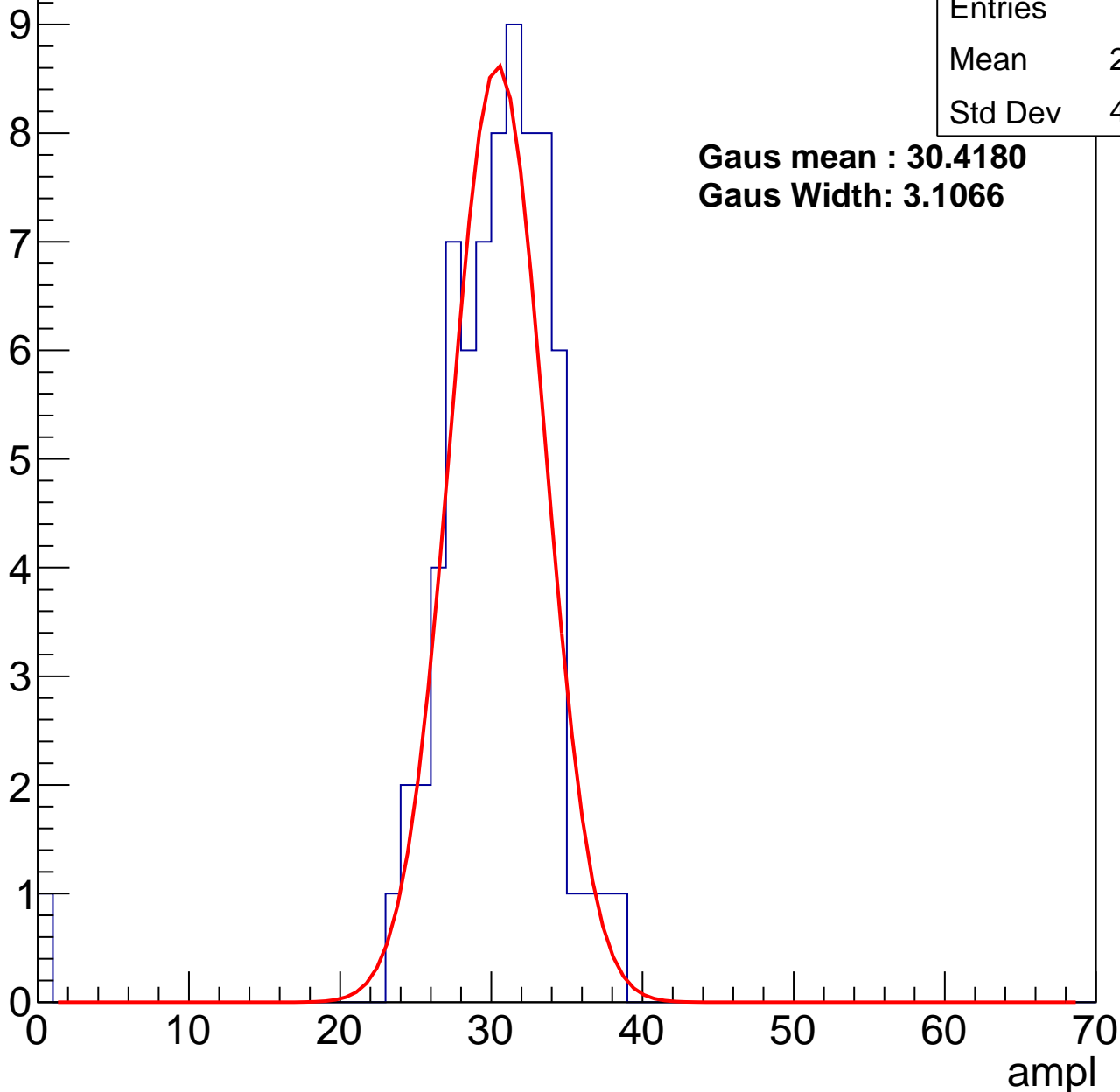
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	73
Mean	29.78
Std Dev	4.694

**Gaus mean : 30.4180**

**Gaus Width: 3.1066**



# B1L100S, U6-ch89, adc1

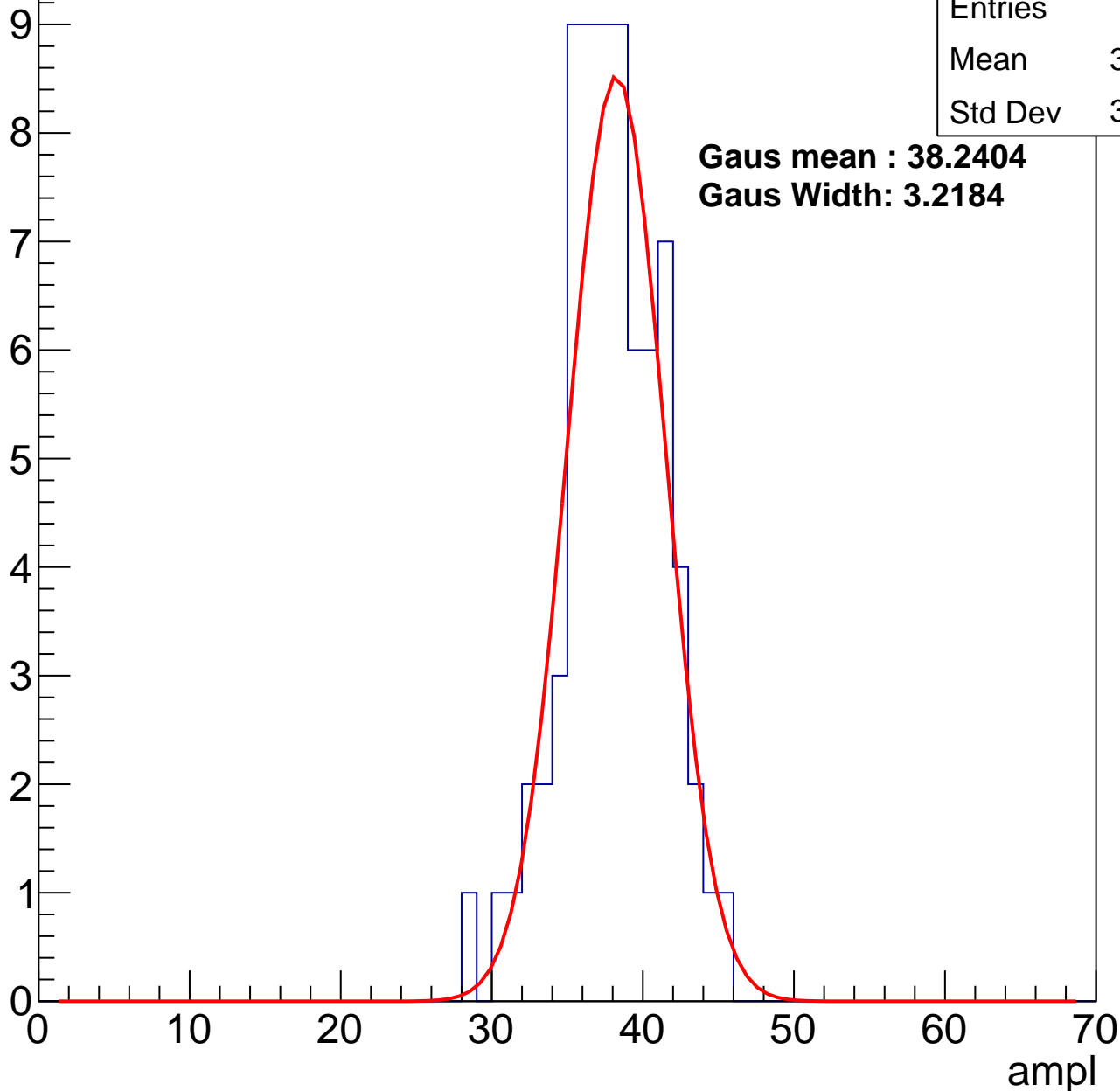
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	73
Mean	37.52
Std Dev	3.278

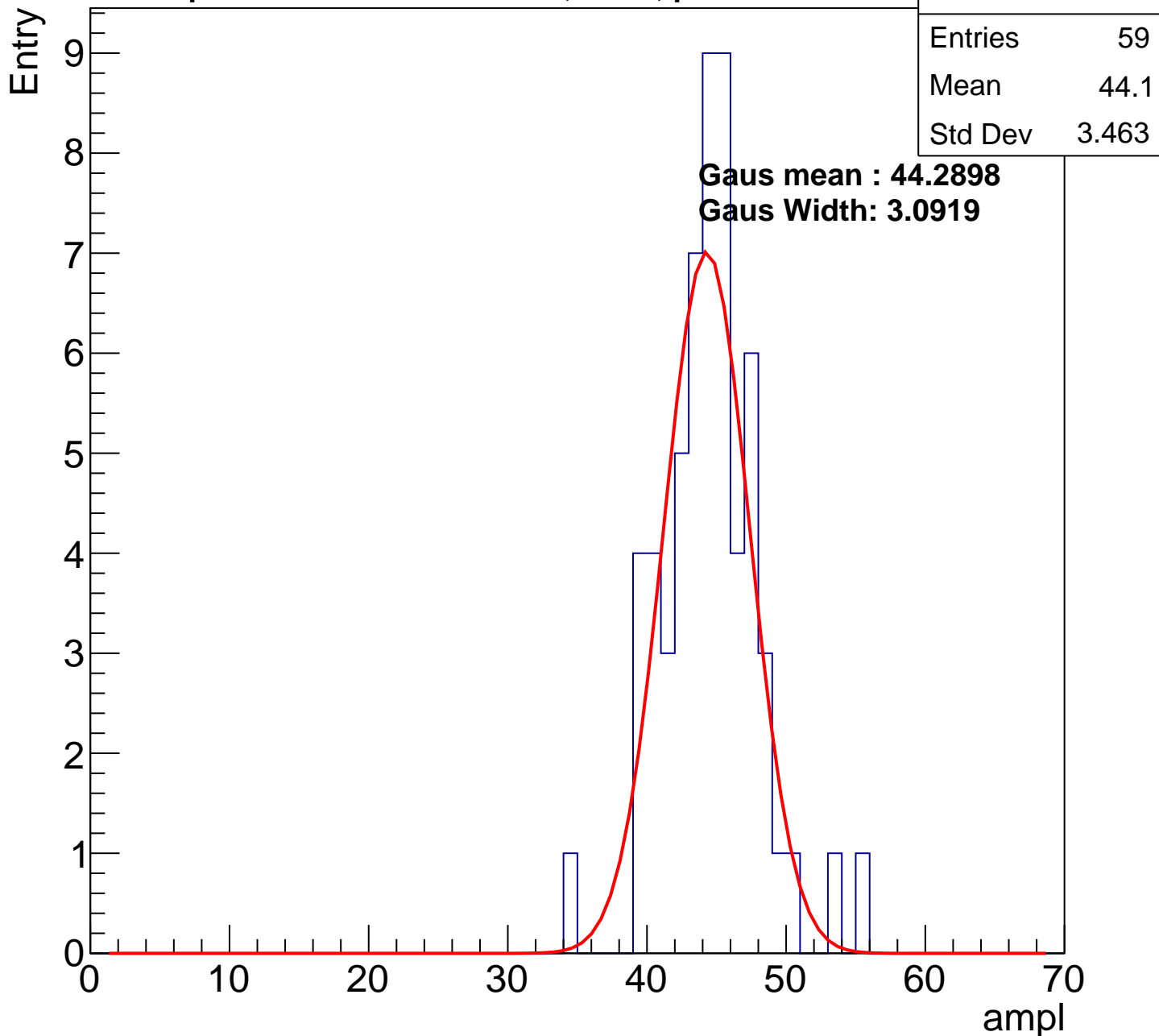
**Gaus mean : 38.2404**

**Gaus Width: 3.2184**



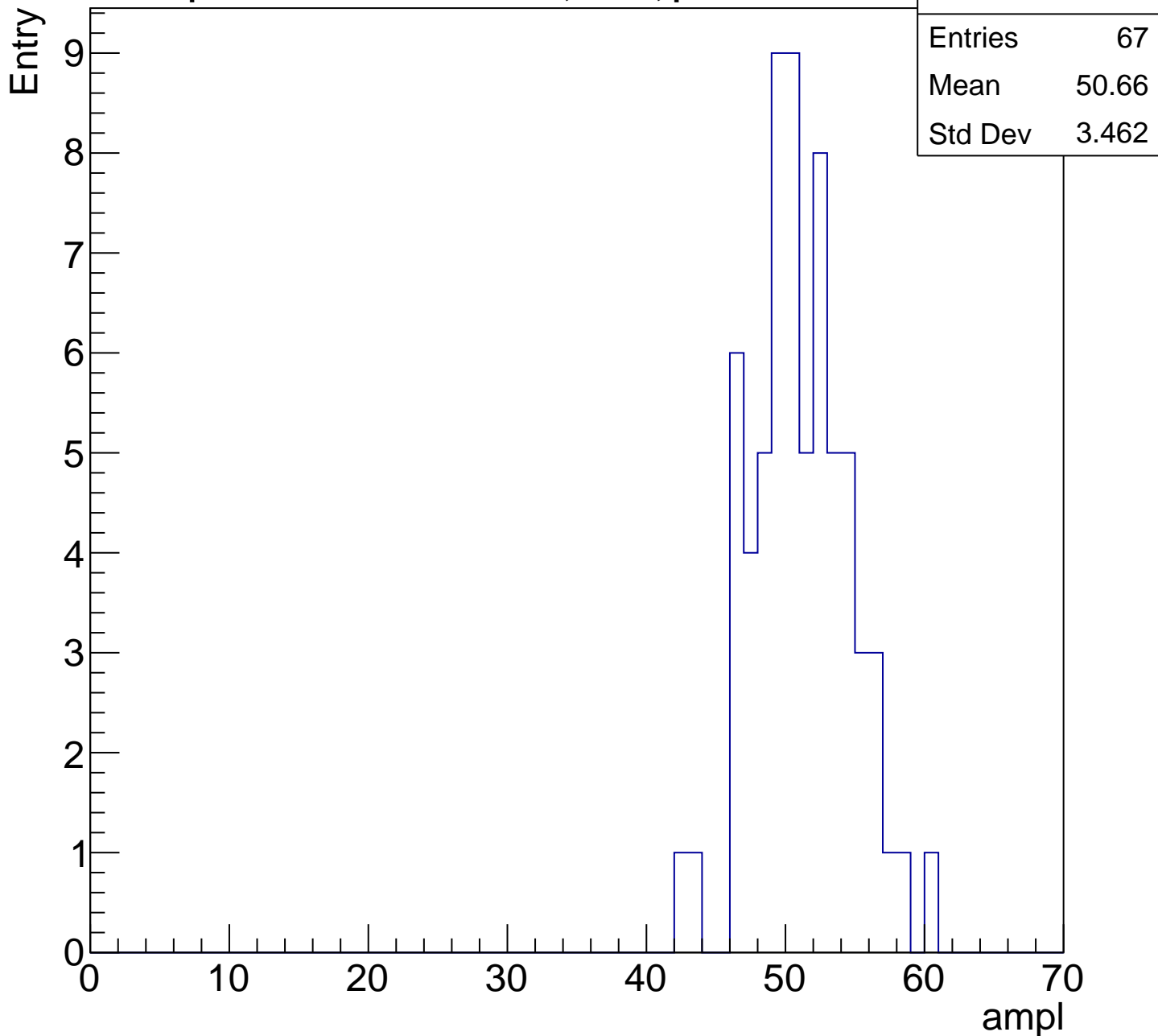
# B1L100S, U6-ch89, adc2

calib\_packv5\_042523\_0143.root, FC#4, port A2



# B1L100S, U6-ch89, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2



# B1L100S, U6-ch89, adc4

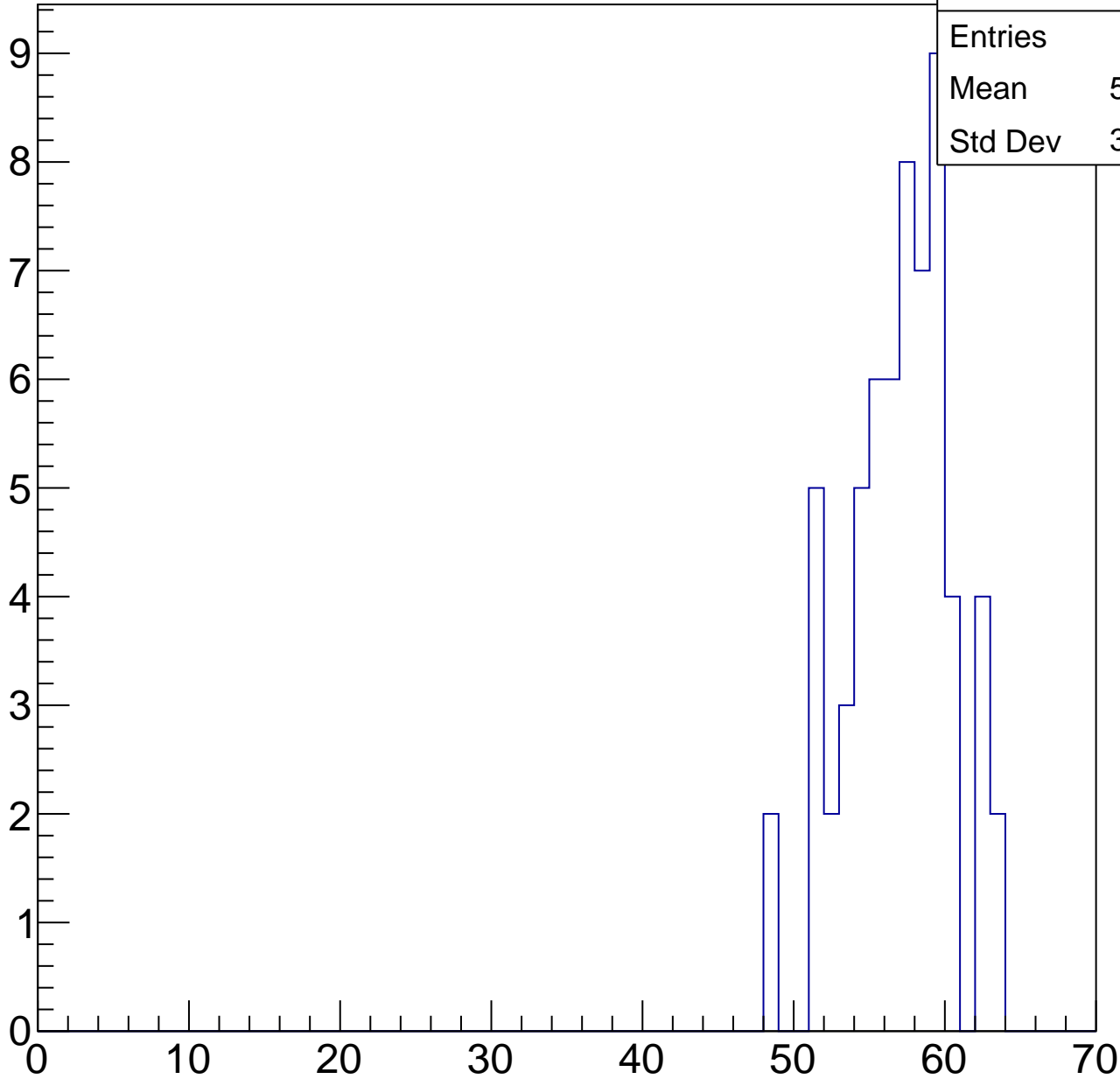
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	63
Mean	56.46
Std Dev	3.445

ampl

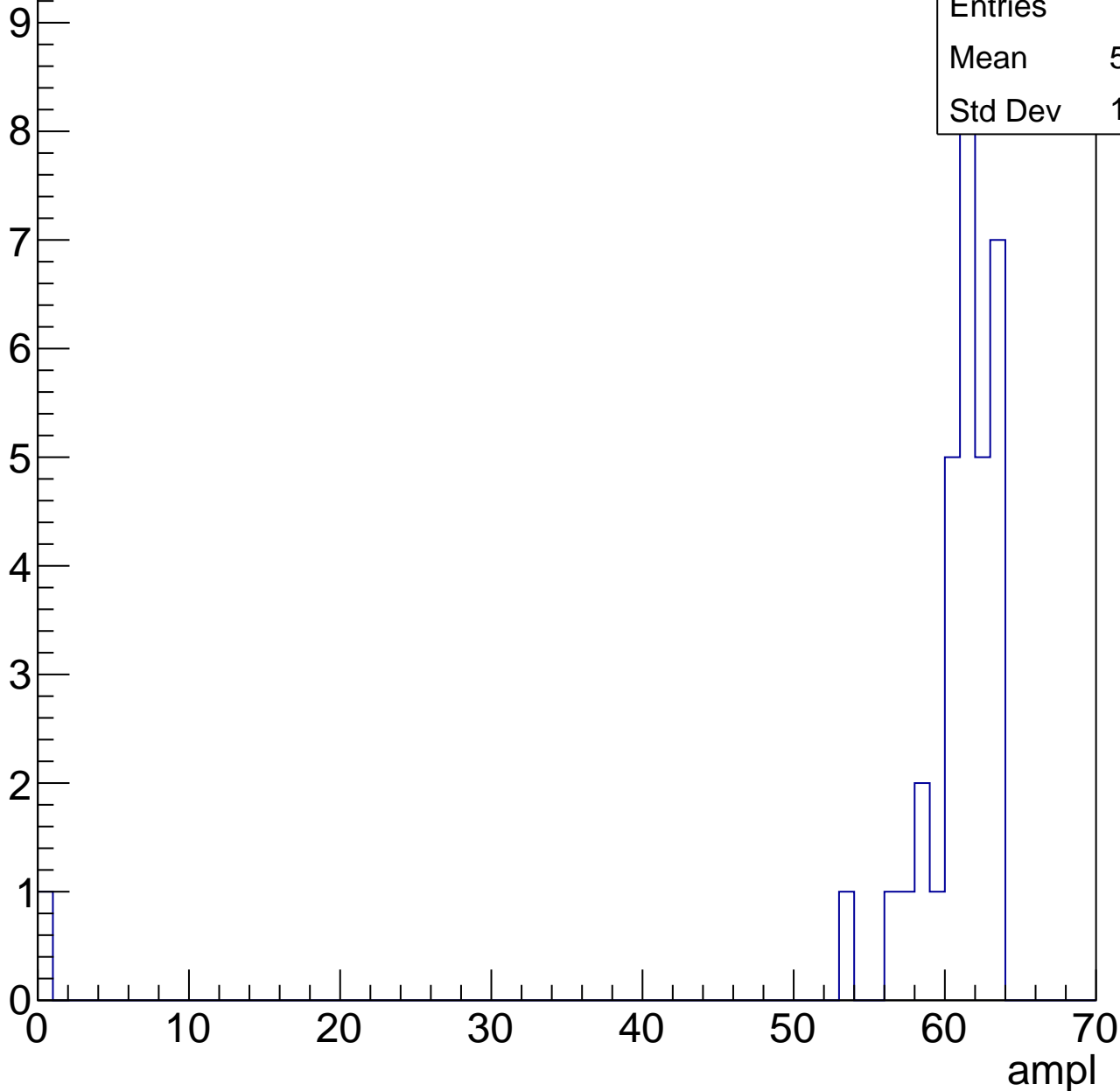


# B1L100S, U6-ch89, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	33
Mean	58.82
Std Dev	10.63



# B1L100S, U6-ch89, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry





# B1L100S, U6-ch89, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L100S, U6-ch90, adc0

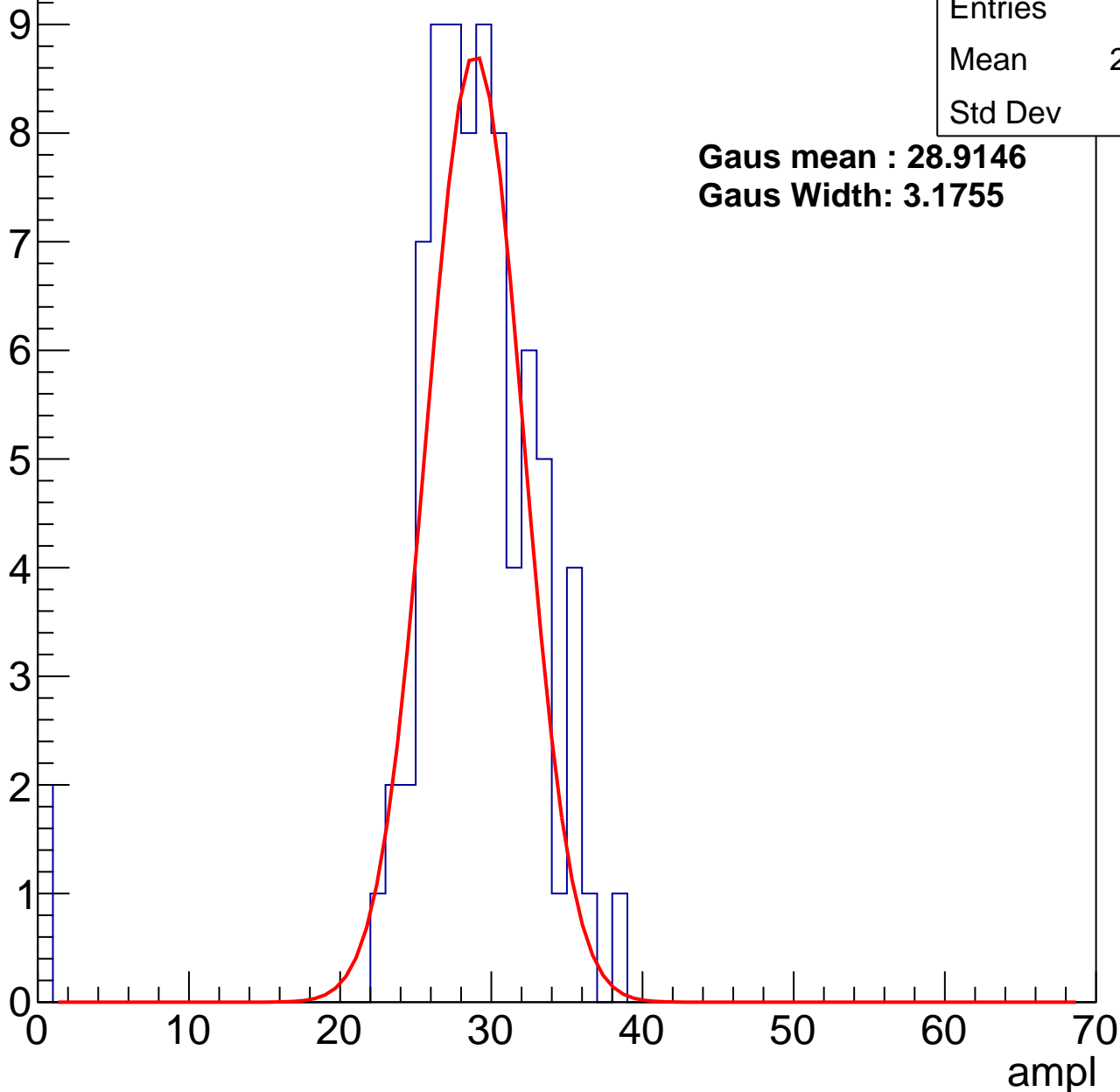
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	79
Mean	28.13
Std Dev	5.61

**Gaus mean : 28.9146**

**Gaus Width: 3.1755**



# B1L100S, U6-ch90, adc1

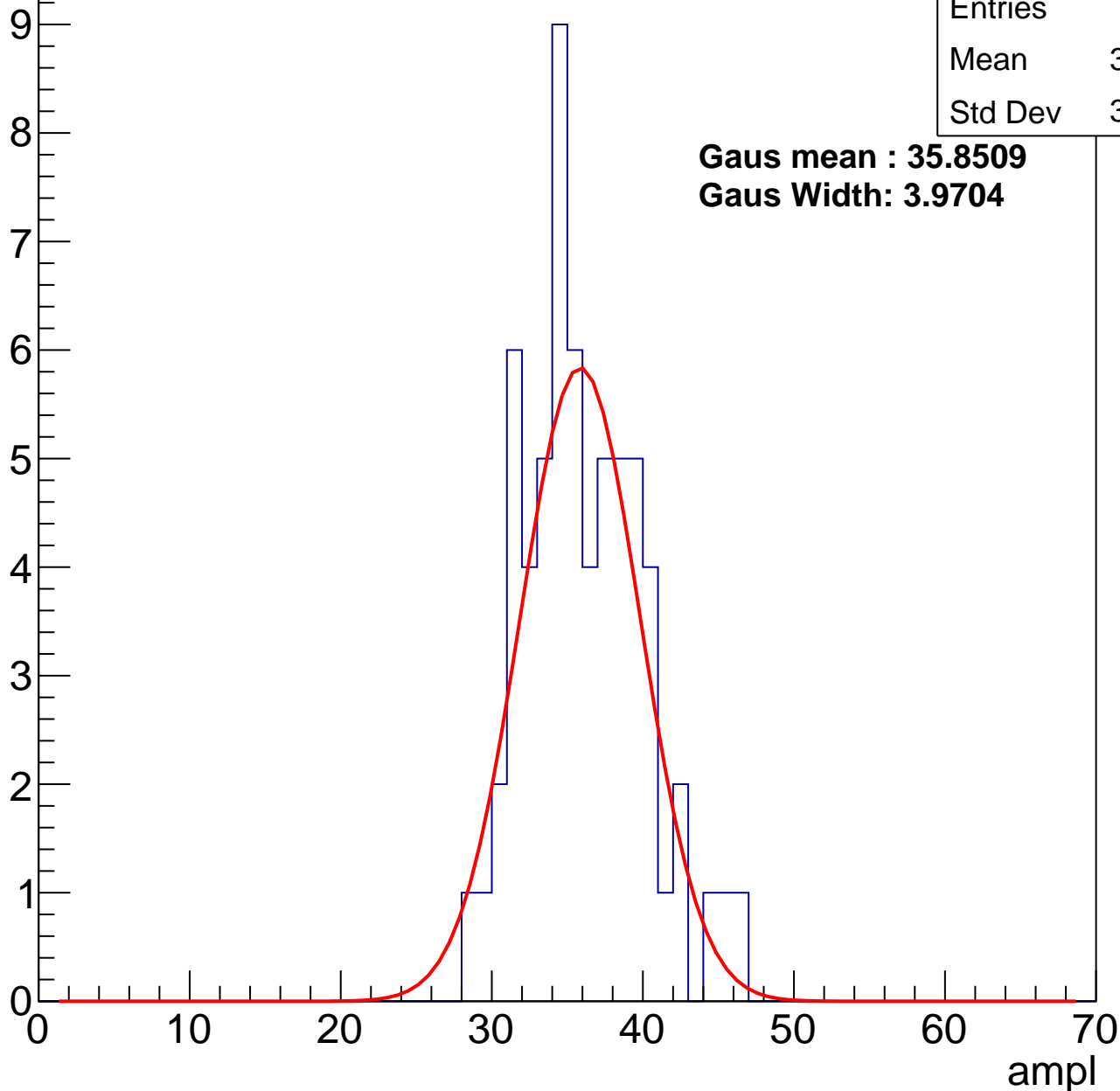
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	63
Mean	35.65
Std Dev	3.892

**Gaus mean : 35.8509**

**Gaus Width: 3.9704**

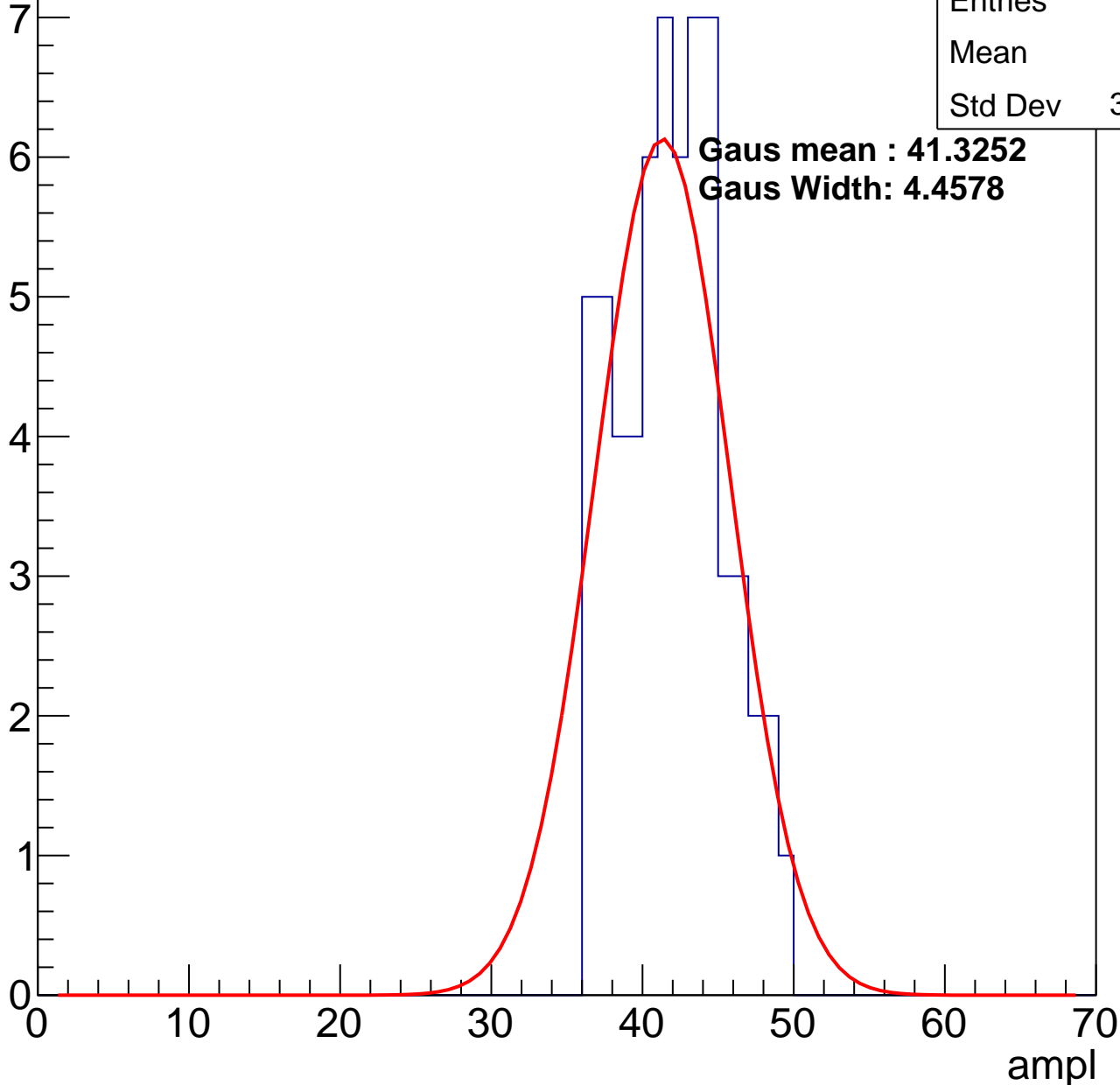


# B1L100S, U6-ch90, adc2

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	62
Mean	41.5
Std Dev	3.364

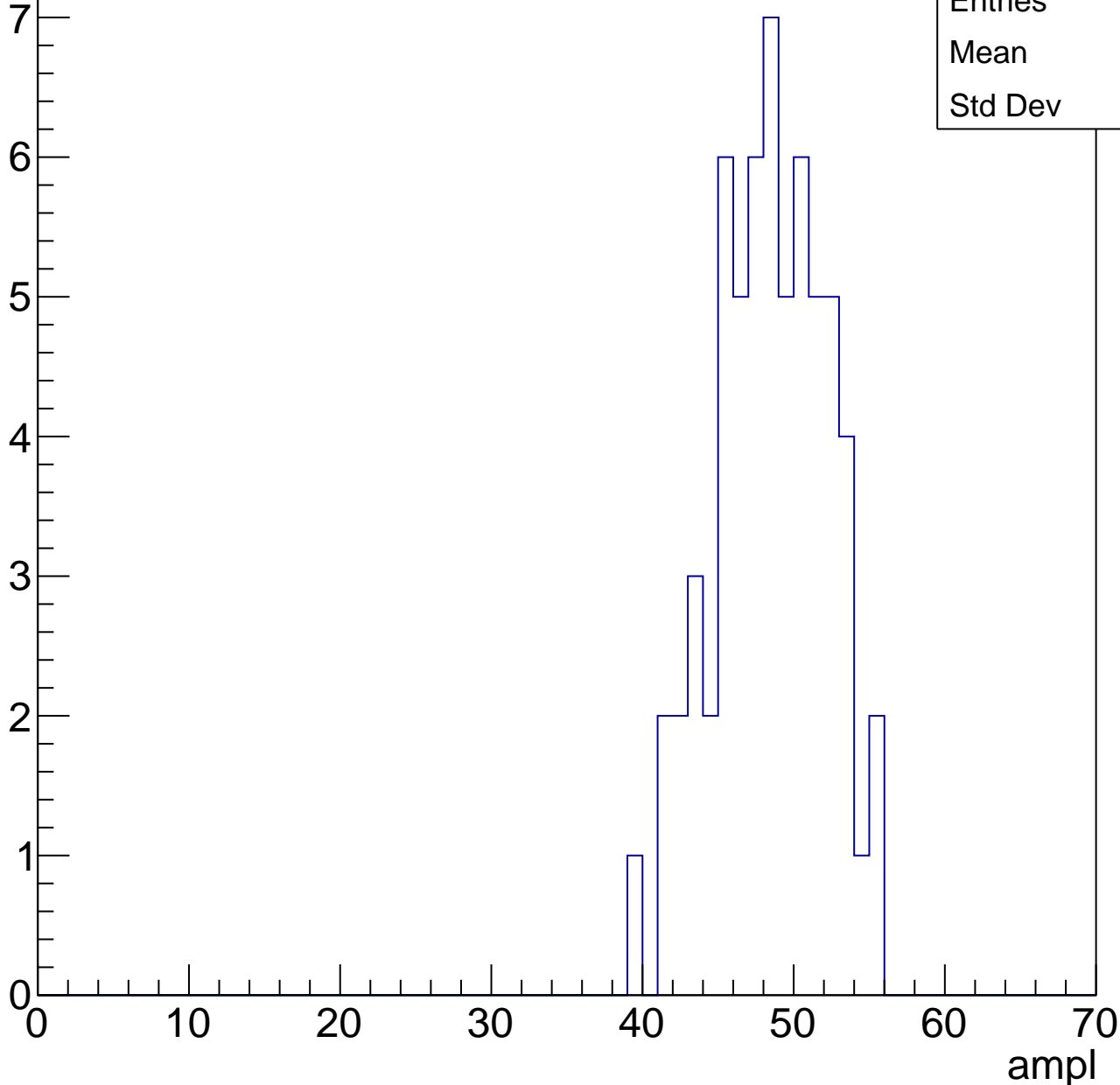


# B1L100S, U6-ch90, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	62
Mean	48
Std Dev	3.65

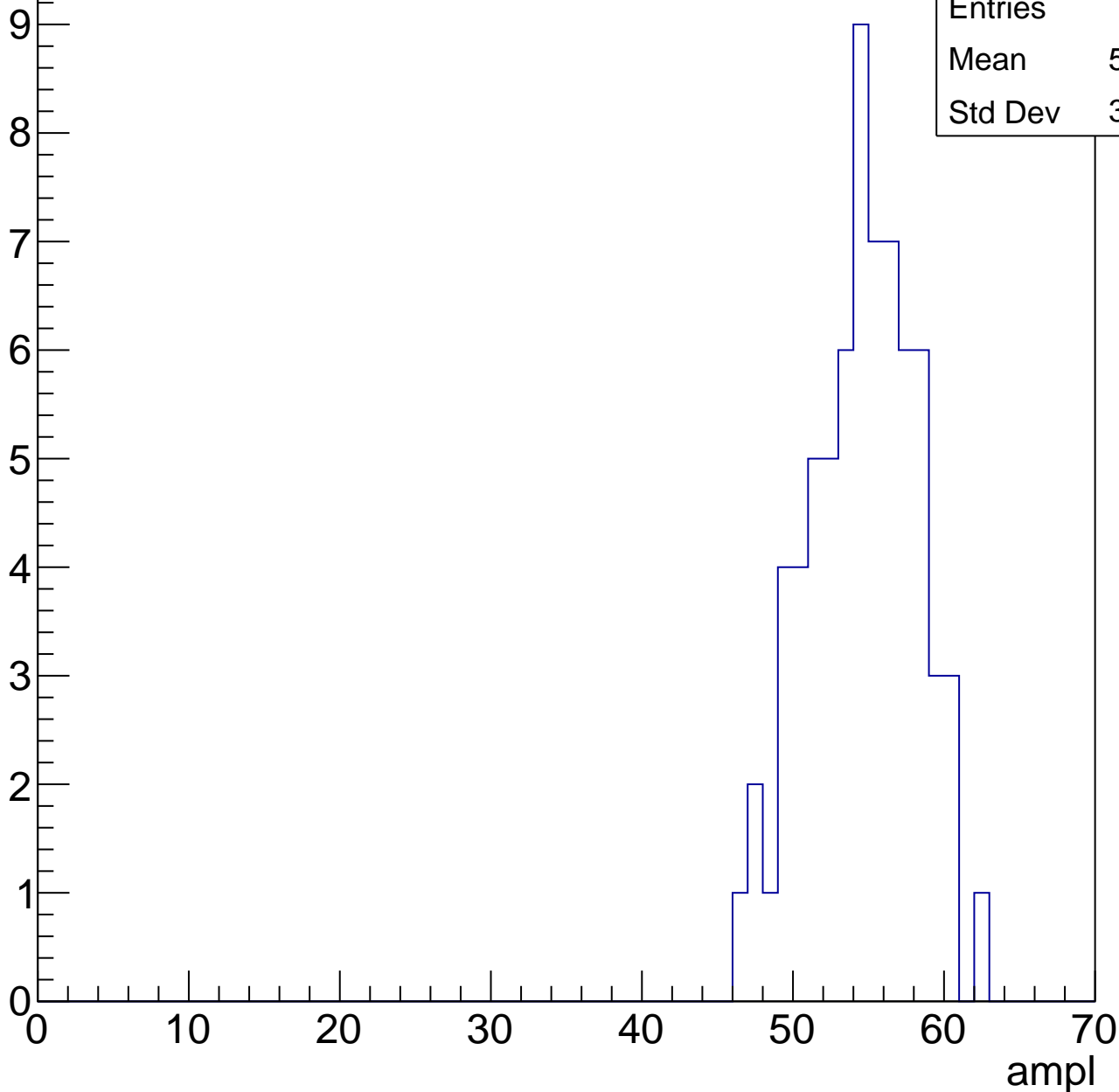


# B1L100S, U6-ch90, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	70
Mean	54.13
Std Dev	3.513



# B1L100S, U6-ch90, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

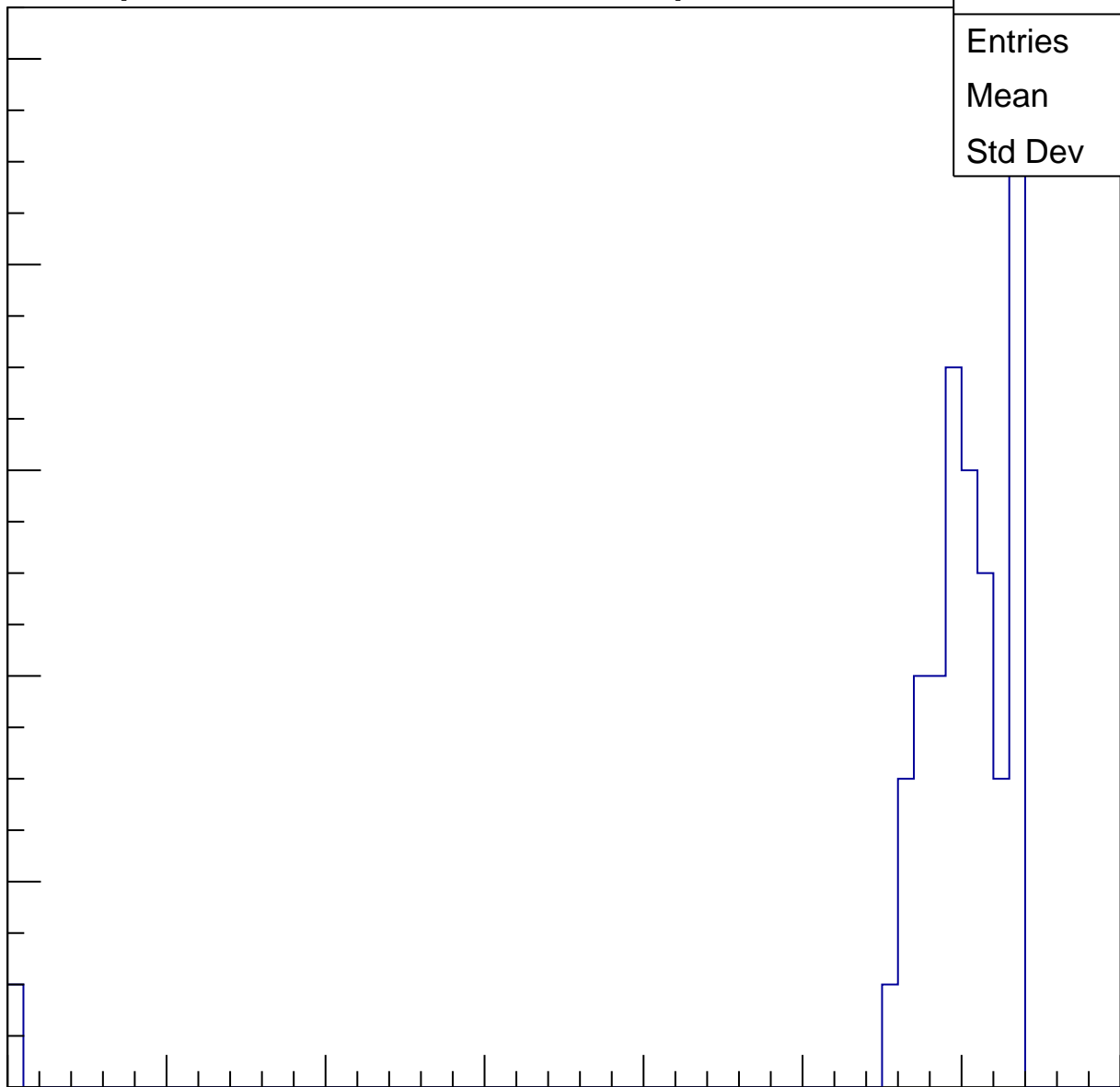
Entries	44
Mean	58.57
Std Dev	9.23

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B1L100S, U6-ch90, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

6

5

4

3

2

1

0

Entries

12

Mean

61.42

Std Dev

0.6401

ampl

0

10

20

30

40

50

60

70



# B1L100S, U6-ch90, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L100S, U6-ch91, adc0

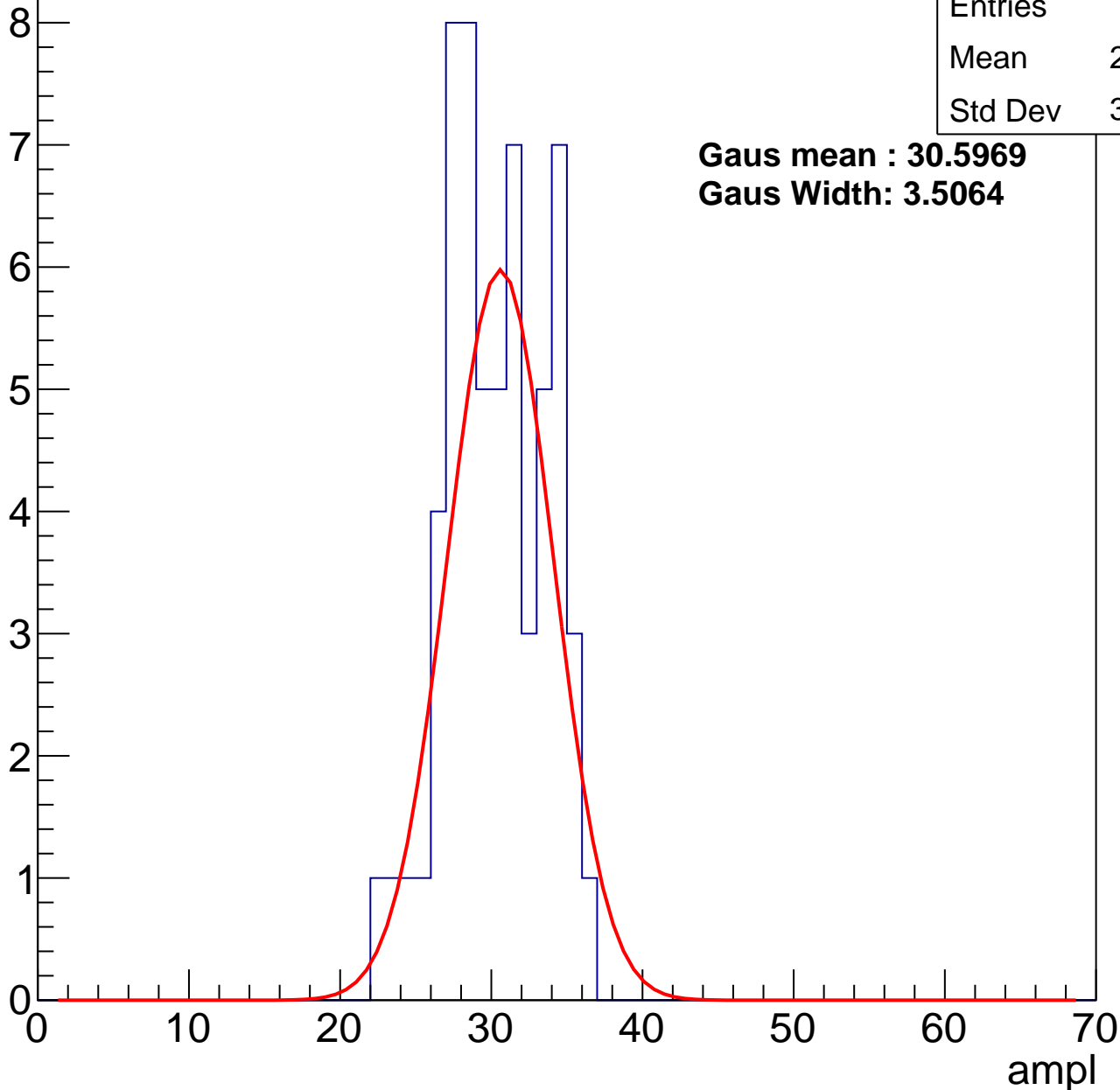
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	60
Mean	29.83
Std Dev	3.246

**Gaus mean : 30.5969**

**Gaus Width: 3.5064**



# B1L100S, U6-ch91, adc1

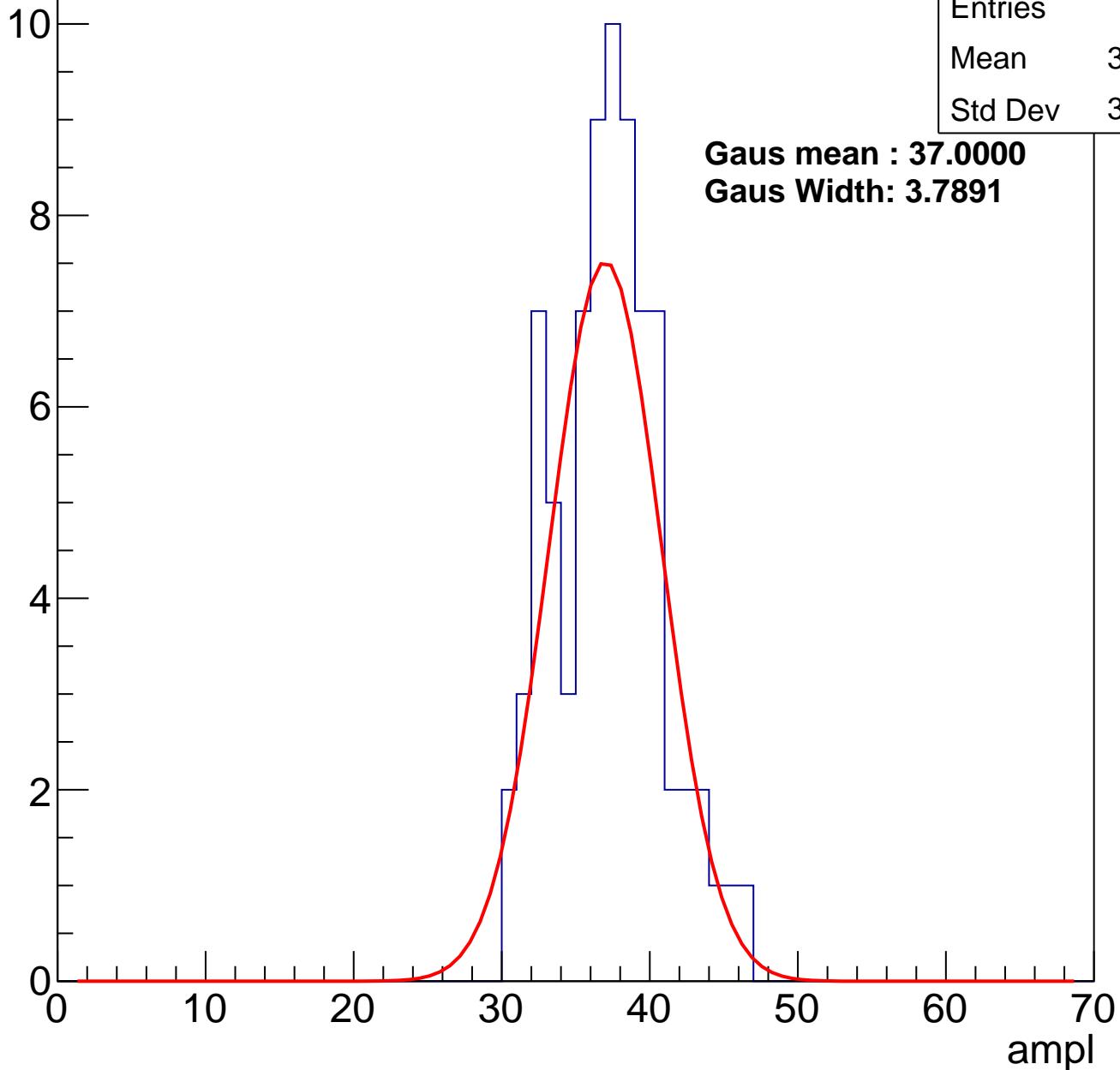
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	78
Mean	36.73
Std Dev	3.522

**Gaus mean : 37.0000**

**Gaus Width: 3.7891**

Entry



# B1L100S, U6-ch91, adc2

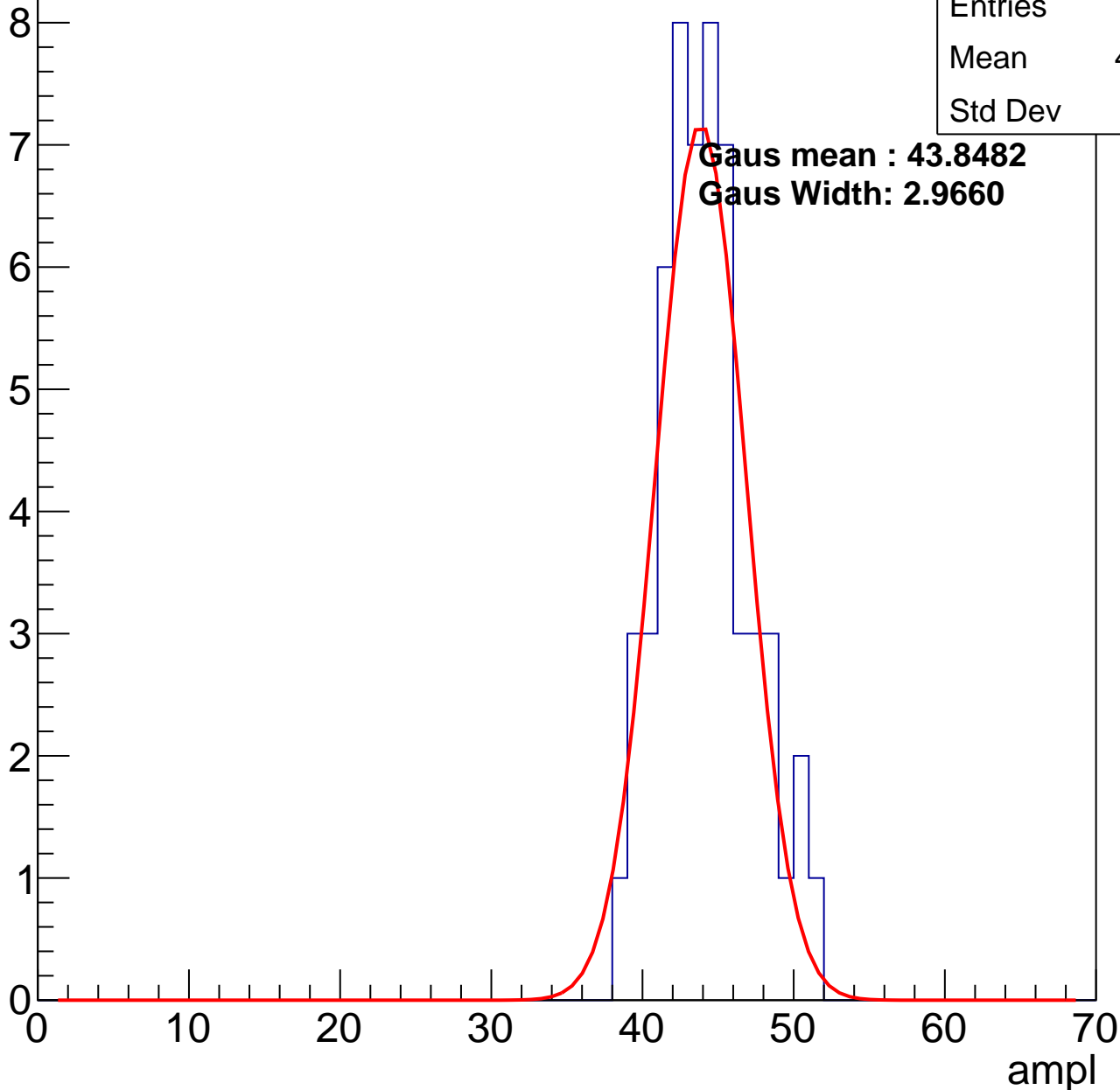
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	56
Mean	43.71
Std Dev	2.95

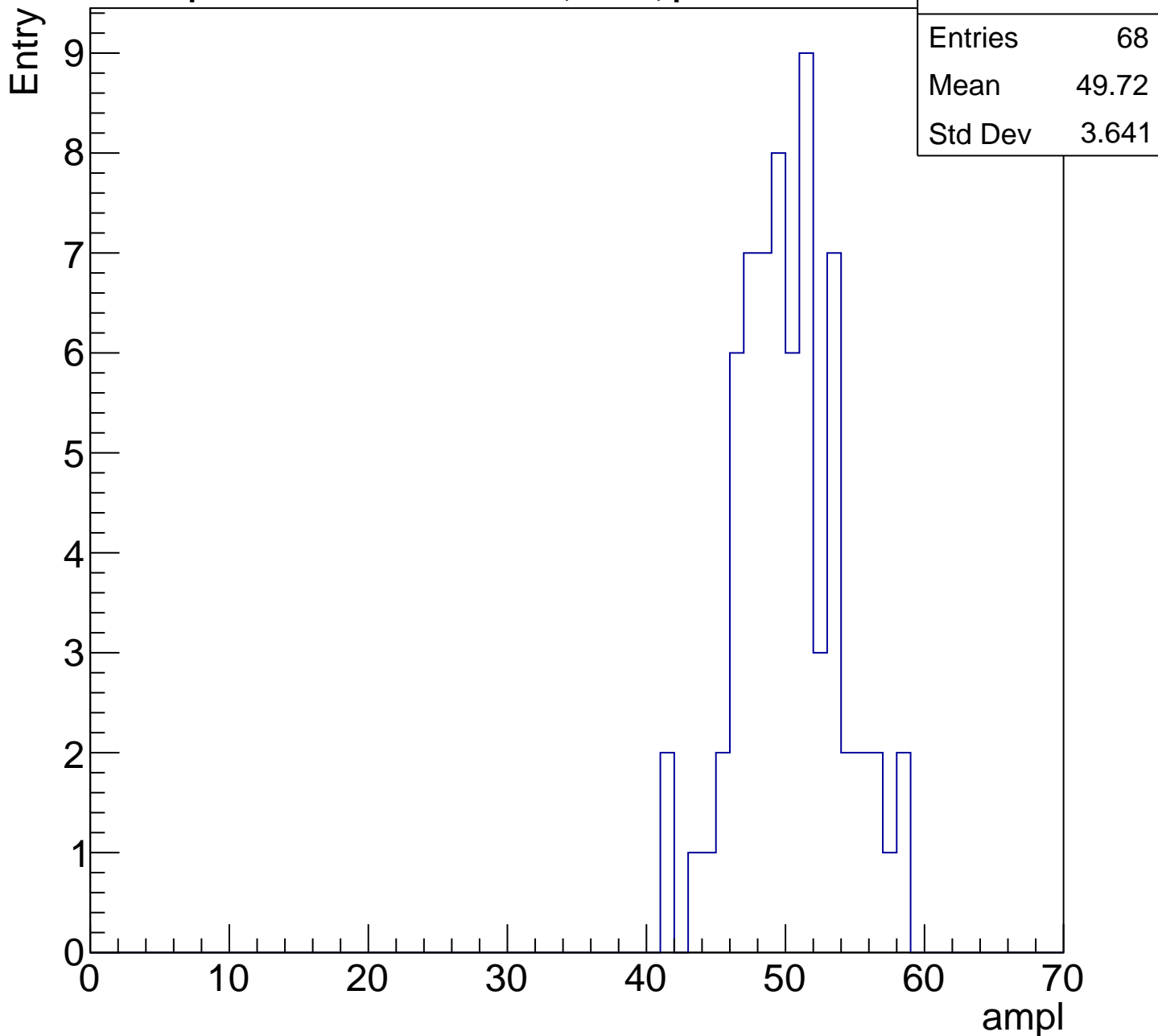
**Gaus mean : 43.8482**

**Gaus Width: 2.9660**



# B1L100S, U6-ch91, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

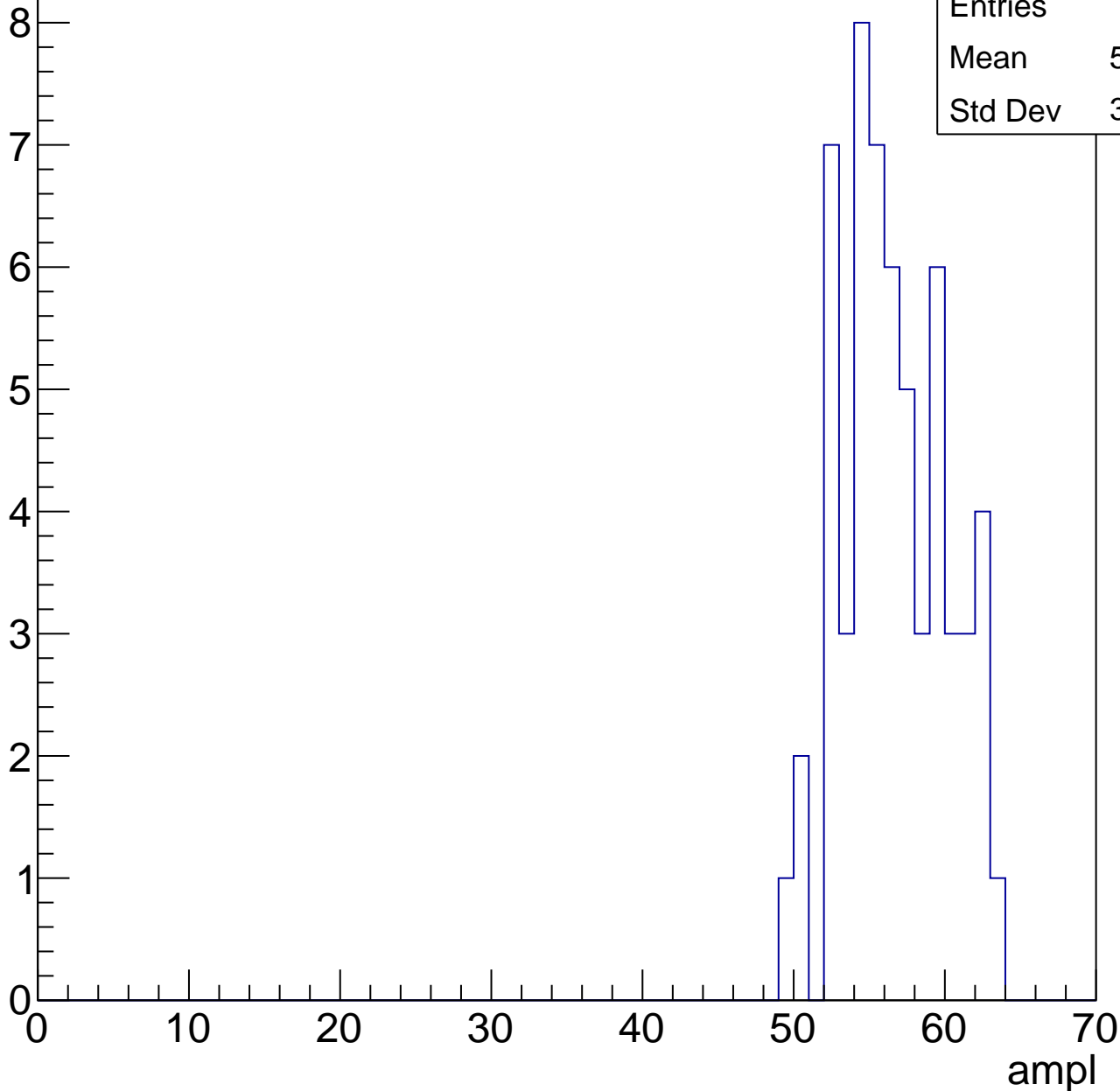


# B1L100S, U6-ch91, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	59
Mean	56.14
Std Dev	3.407

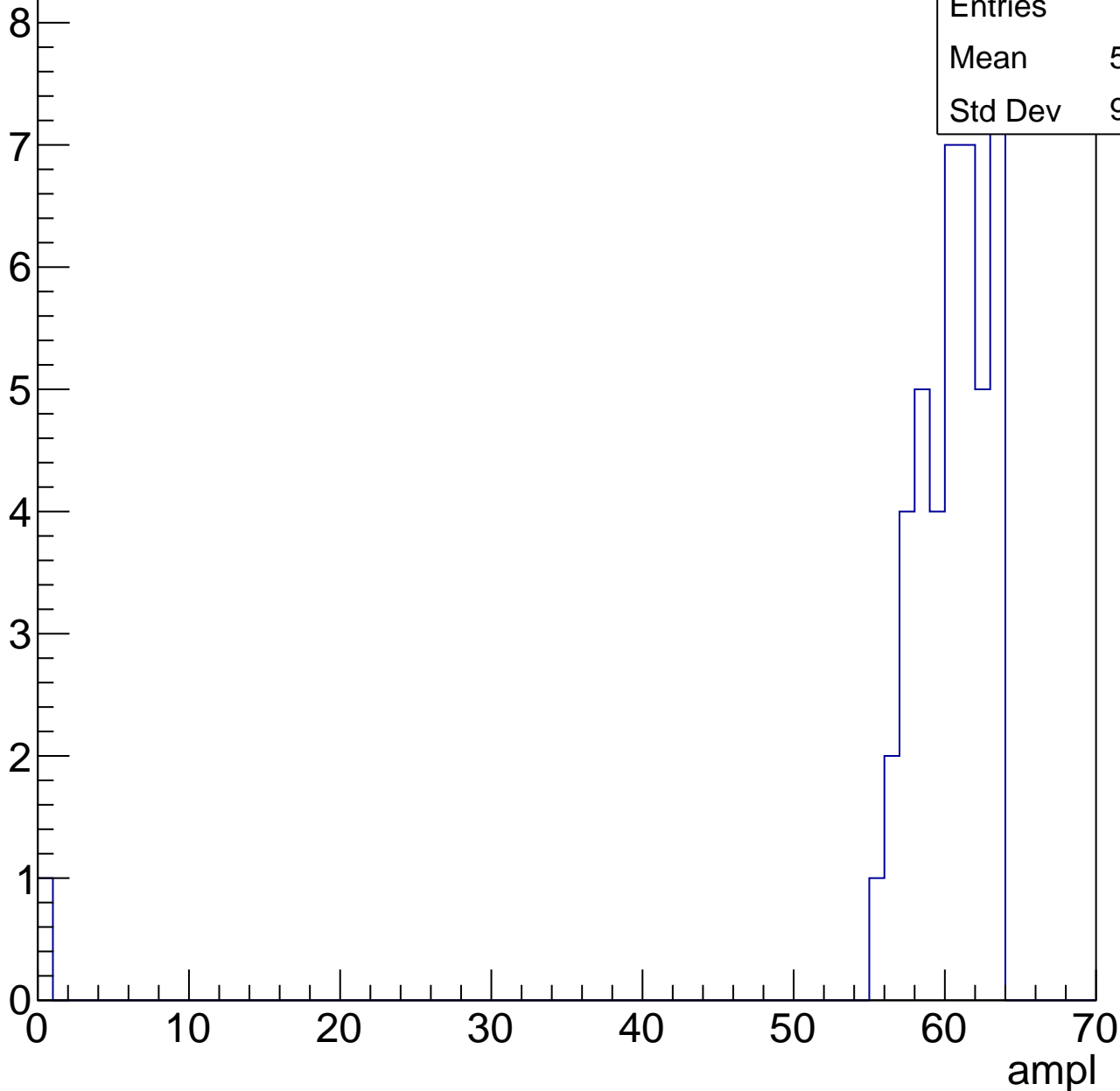


# B1L100S, U6-ch91, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	44
Mean	58.68
Std Dev	9.219



# B1L100S, U6-ch91, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry





# B1L100S, U6-ch91, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



# B1L100S, U6-ch92, adc0

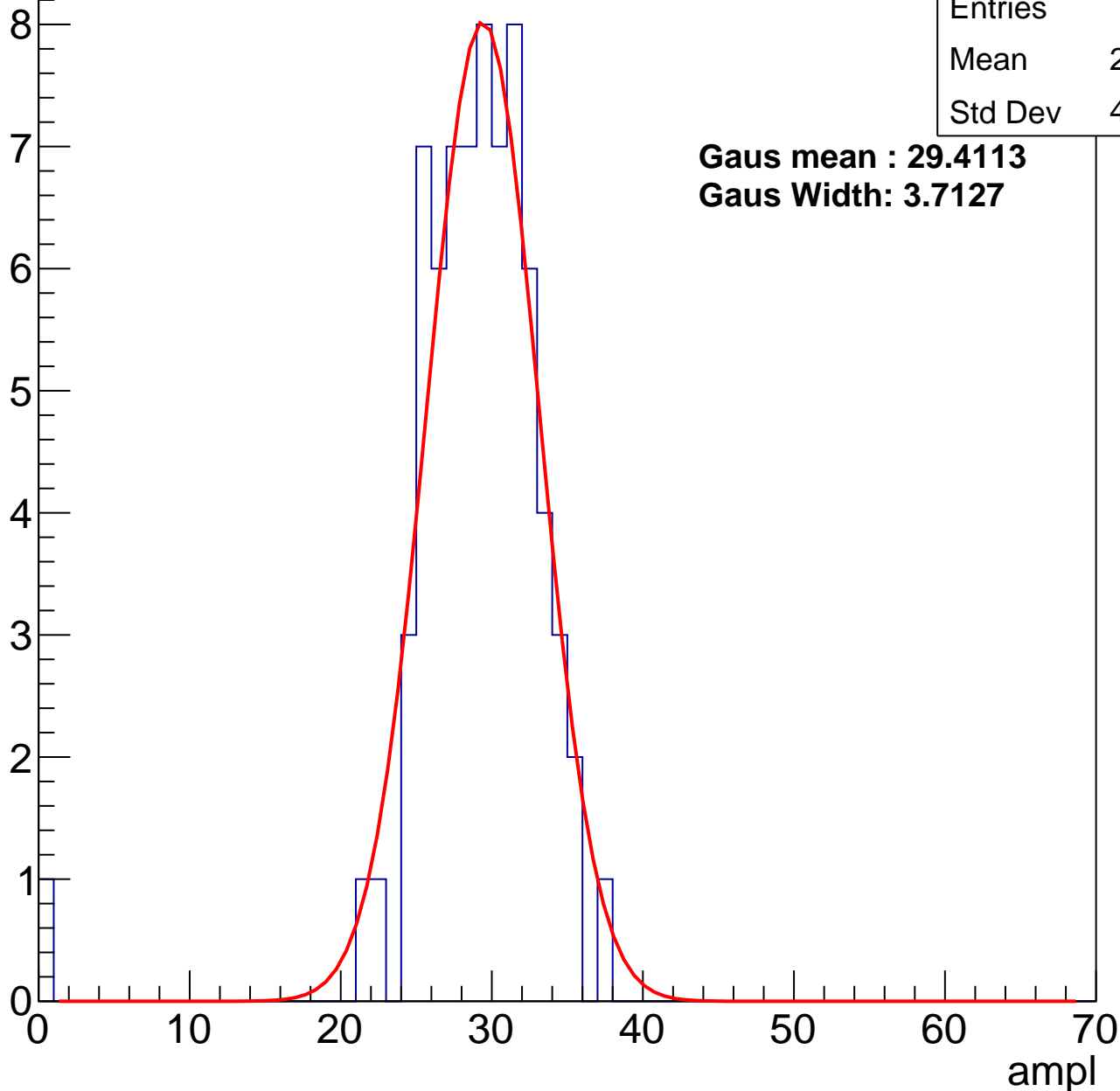
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	72
Mean	28.53
Std Dev	4.687

**Gaus mean : 29.4113**

**Gaus Width: 3.7127**



# B1L100S, U6-ch92, adc1

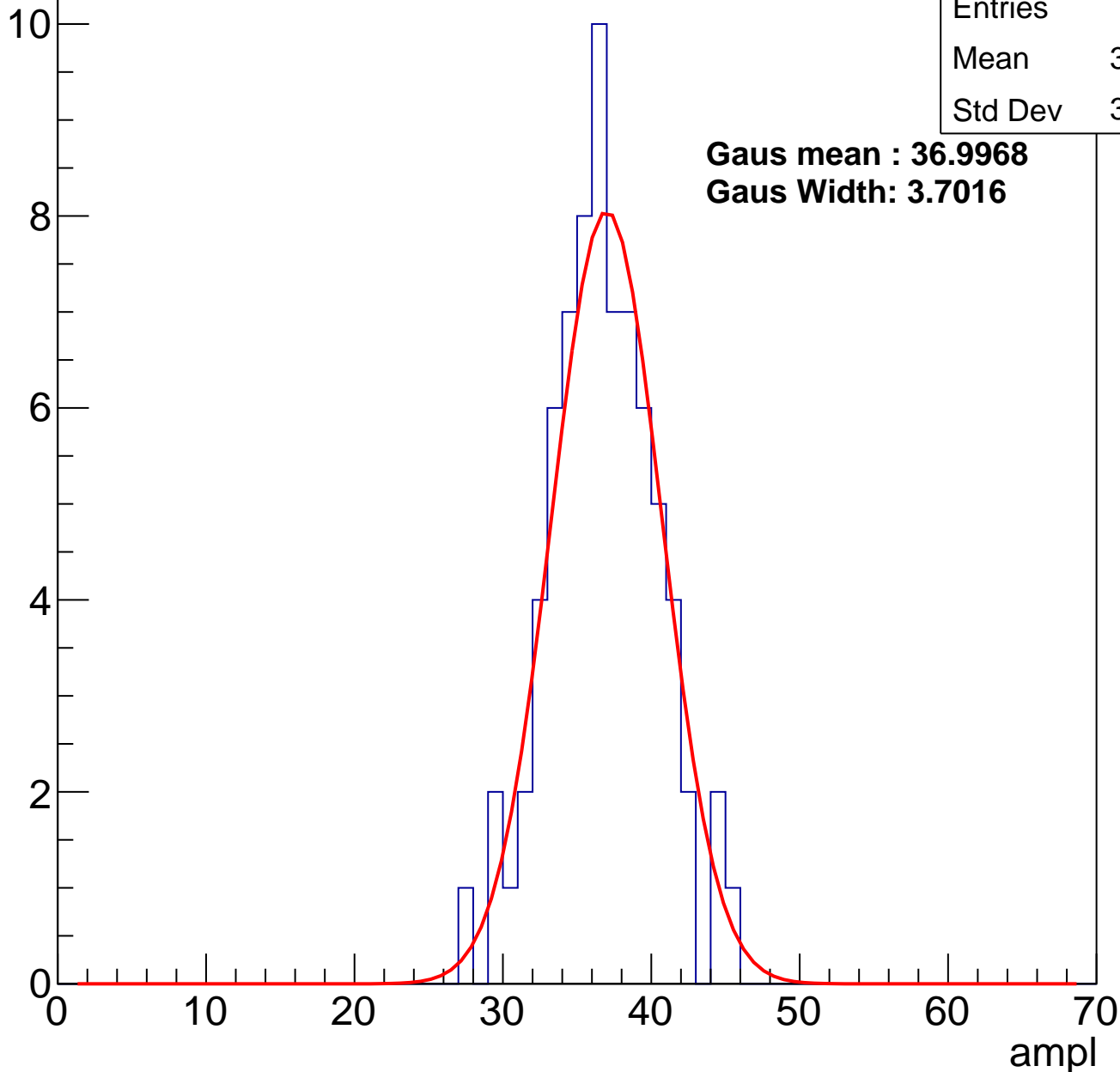
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	75
Mean	36.28
Std Dev	3.584

**Gaus mean : 36.9968**

**Gaus Width: 3.7016**

Entry



# B1L100S, U6-ch92, adc2

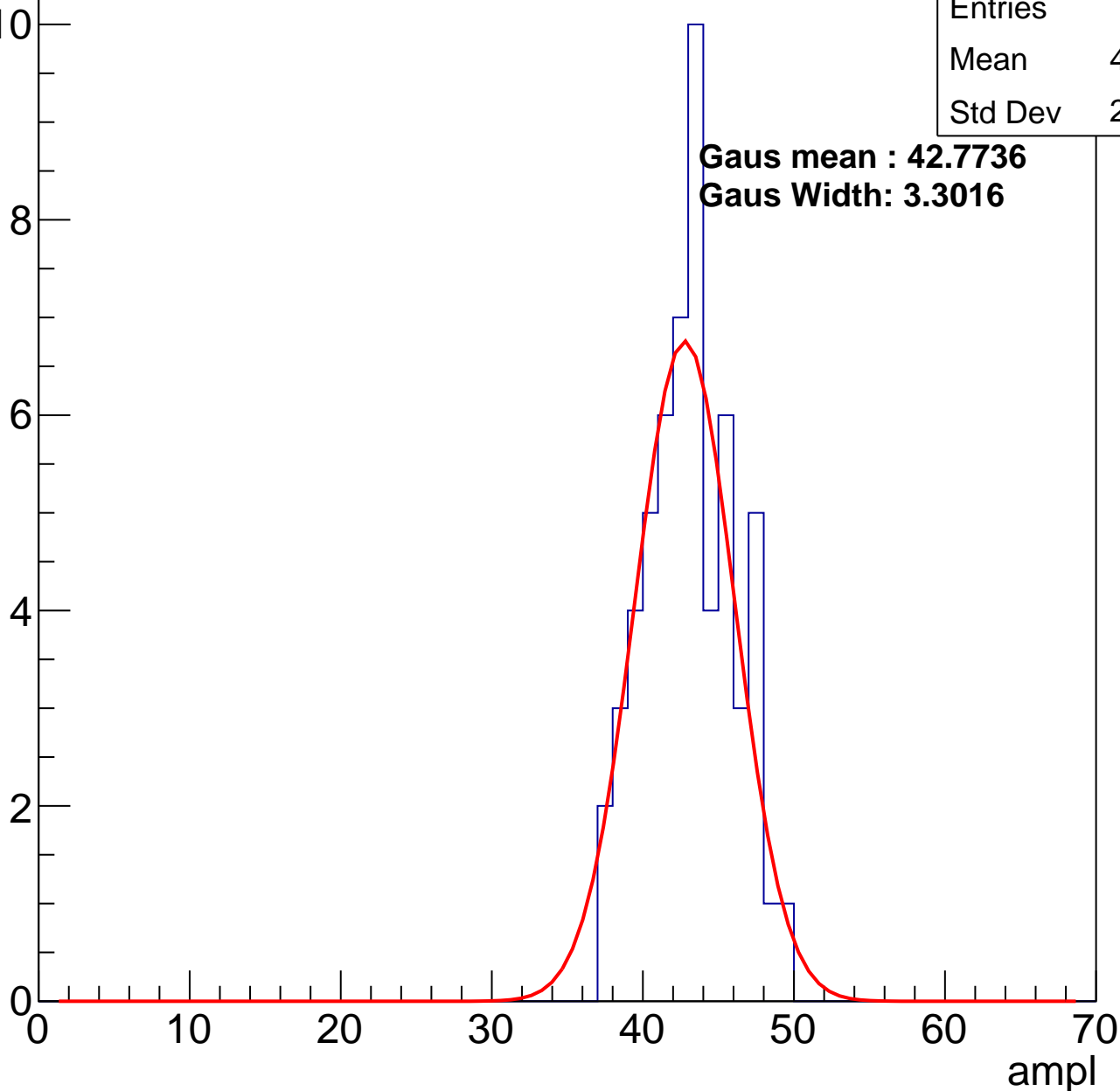
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	57
Mean	42.63
Std Dev	2.888

**Gaus mean : 42.7736**

**Gaus Width: 3.3016**



# B1L100S, U6-ch92, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

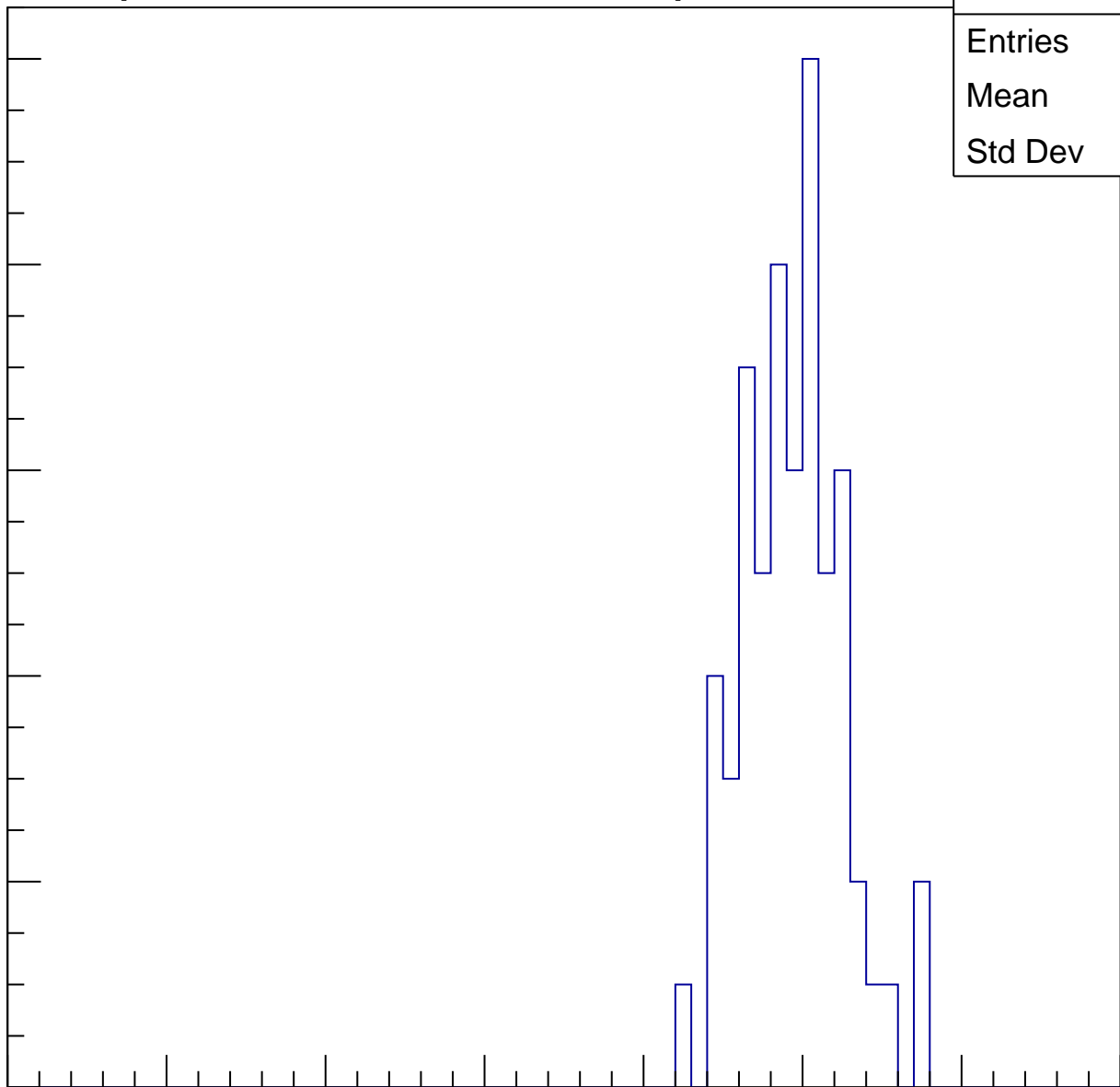
Entries	61
Mean	48.92
Std Dev	3.117

Entry

10  
8  
6  
4  
2  
0

ampl

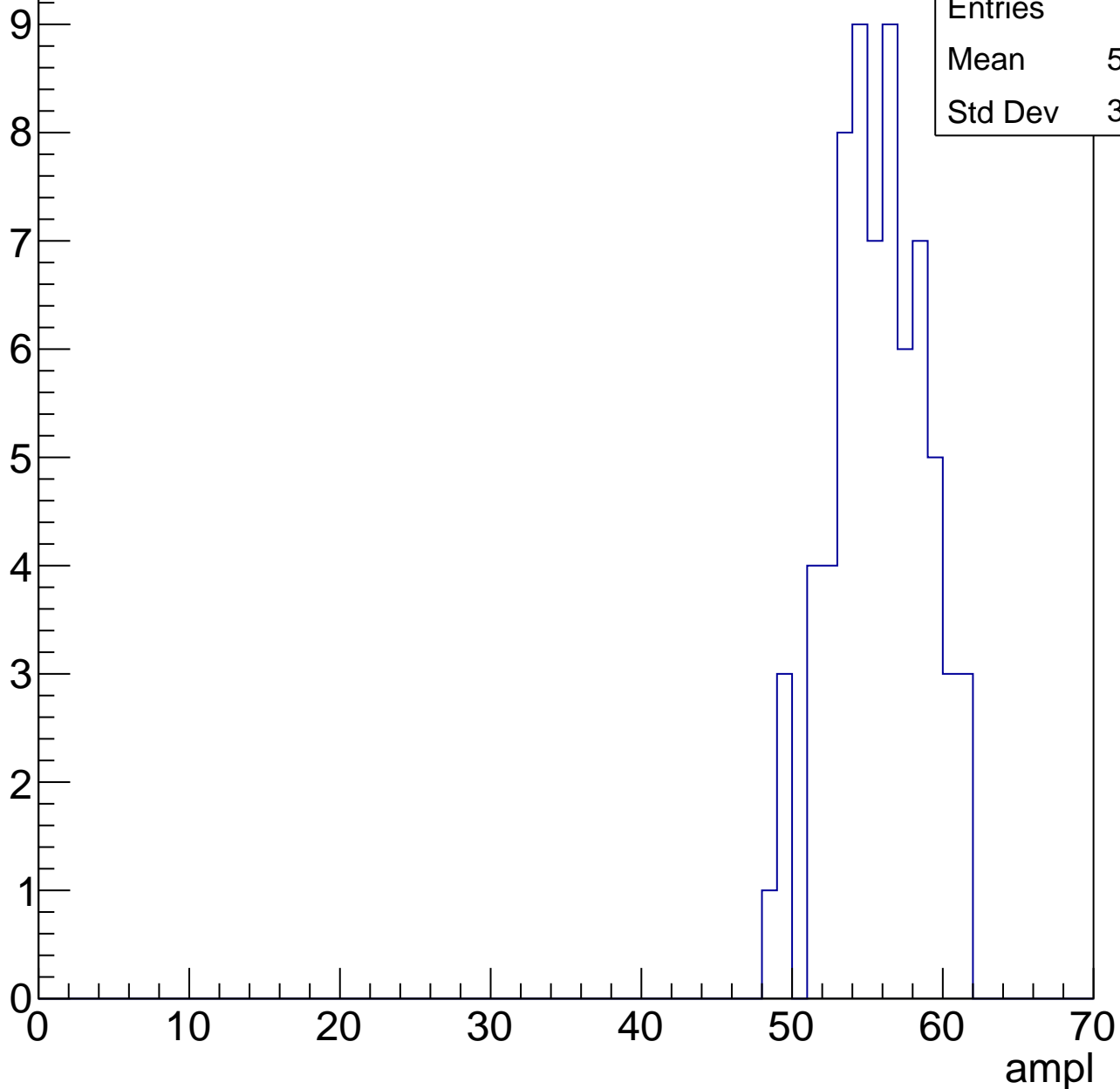
0 10 20 30 40 50 60 70



# B1L100S, U6-ch92, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

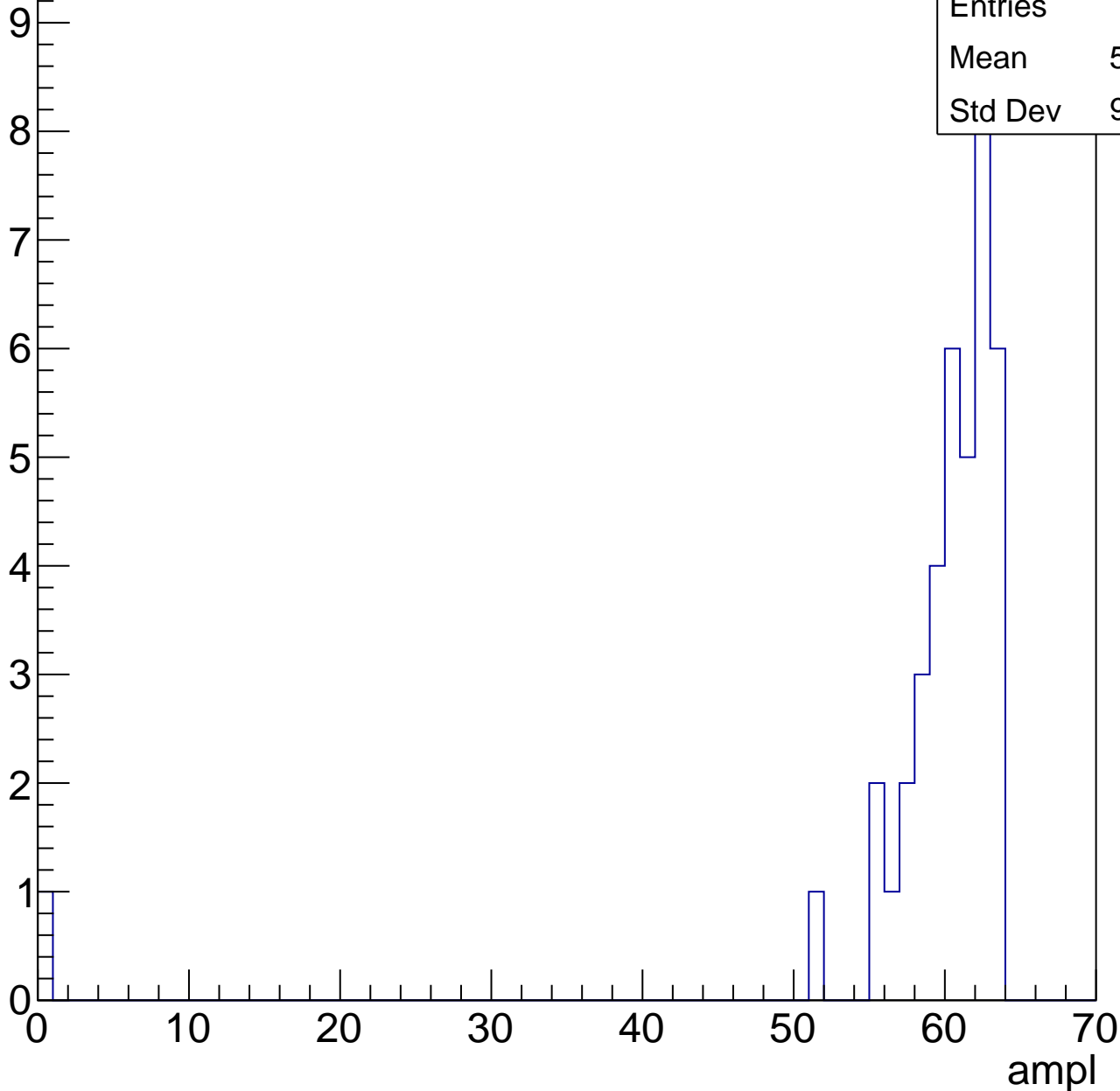


# B1L100S, U6-ch92, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

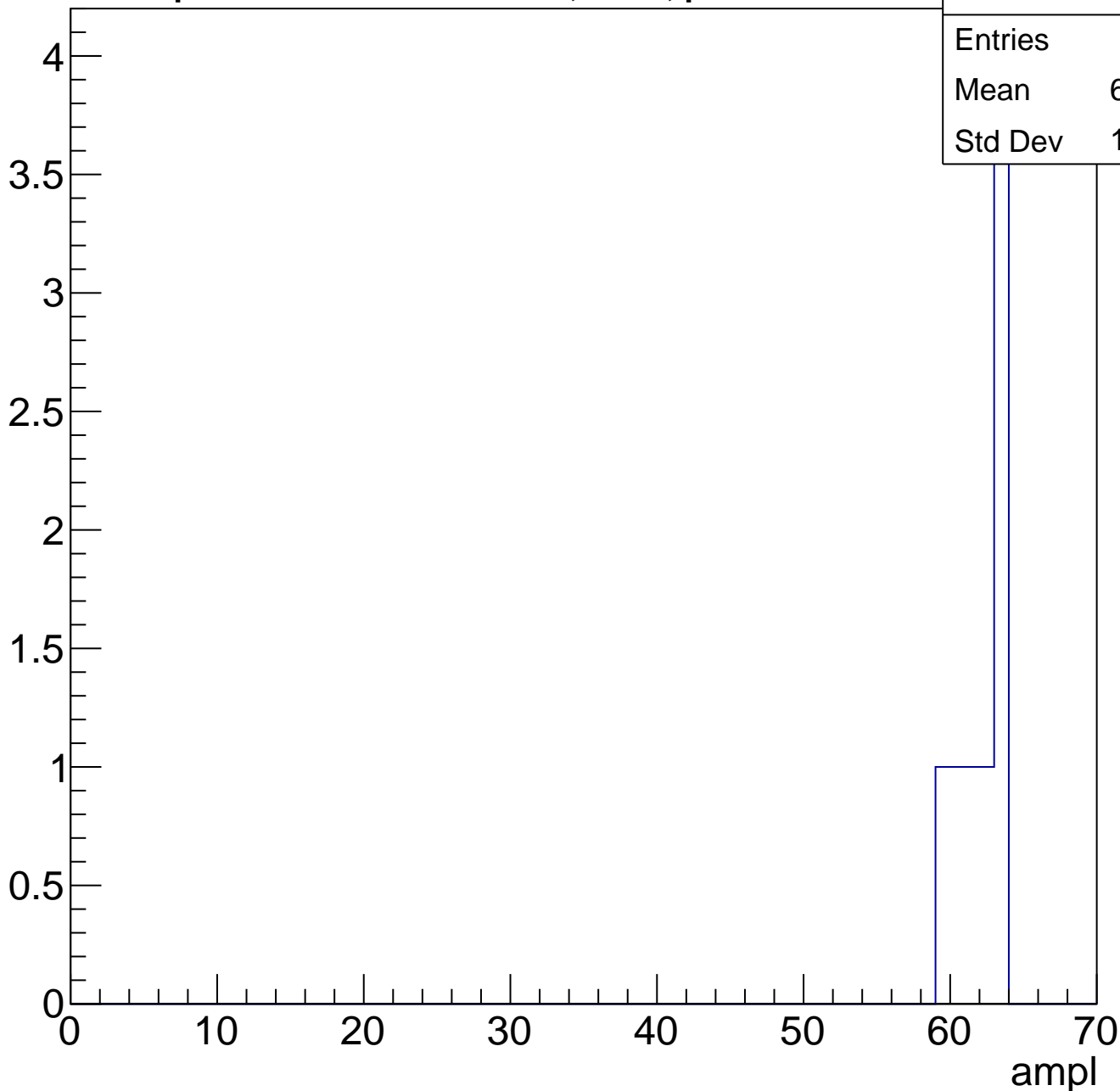
Entries	40
Mean	58.55
Std Dev	9.736



# B1L100S, U6-ch92, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

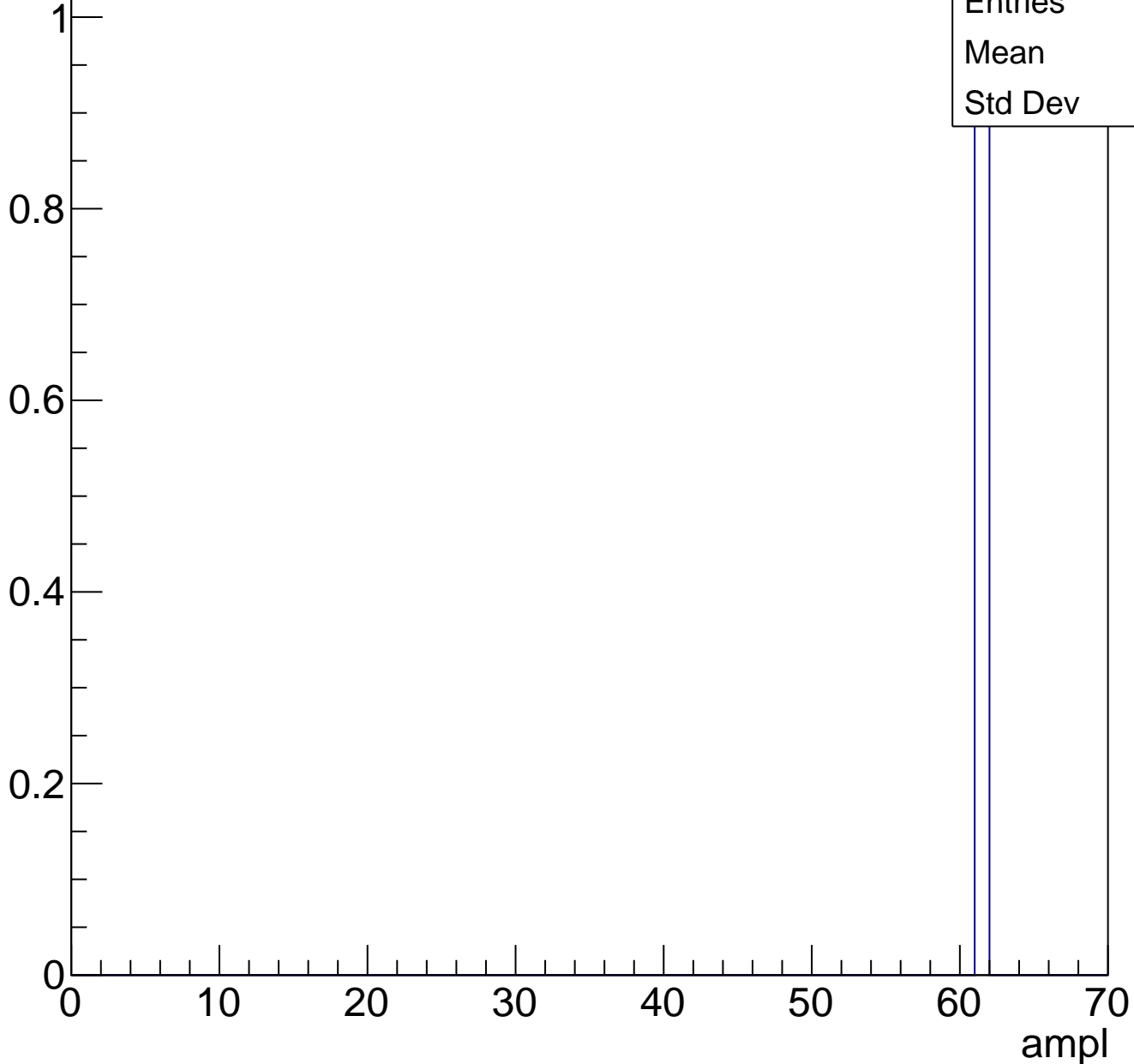




# B1L100S, U6-ch92, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



# B1L100S, U6-ch93, adc0

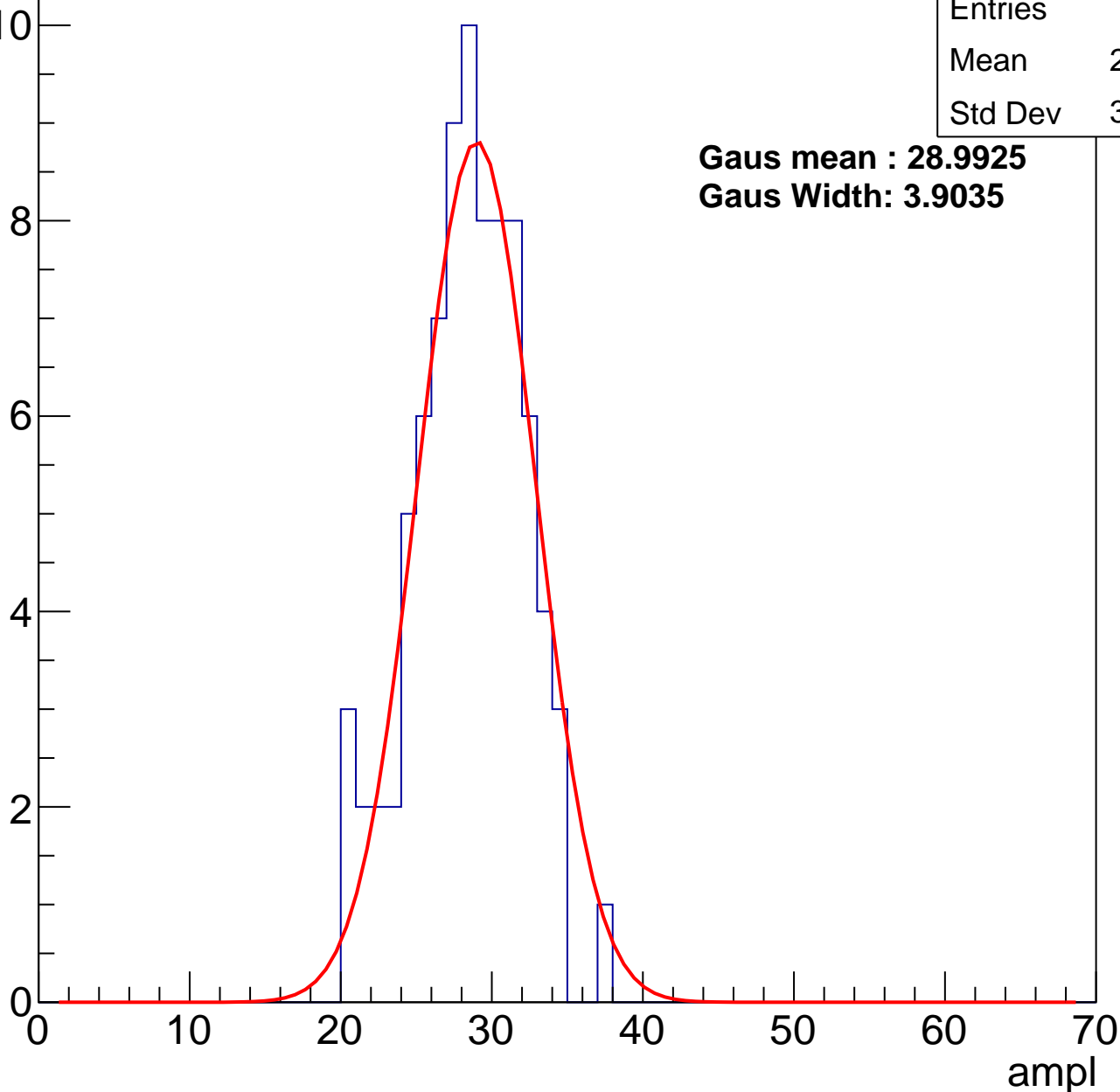
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	84
Mean	27.98
Std Dev	3.586

**Gaus mean : 28.9925**

**Gaus Width: 3.9035**



# B1L100S, U6-ch93, adc1

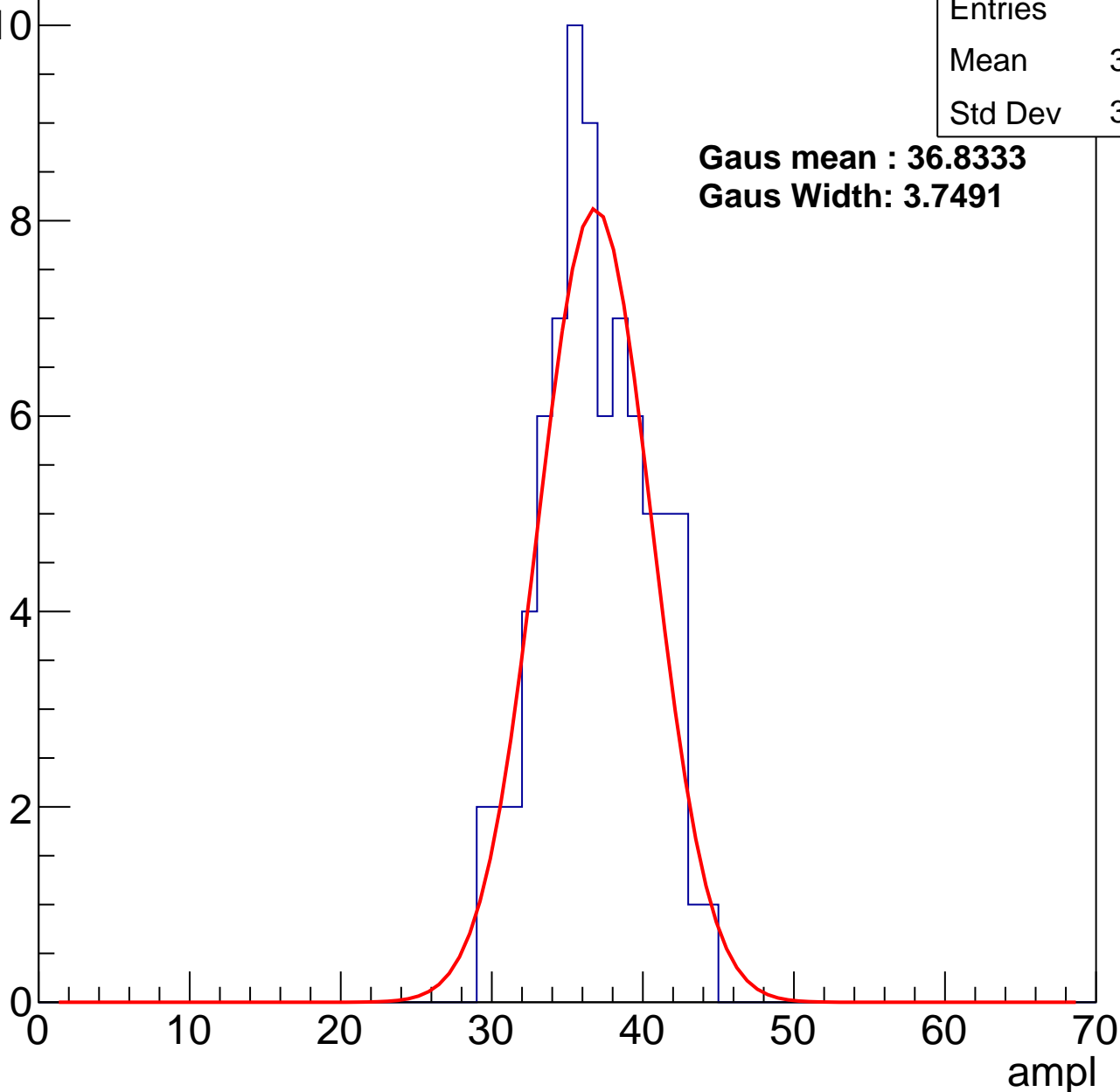
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	78
Mean	36.44
Std Dev	3.485

**Gaus mean : 36.8333**

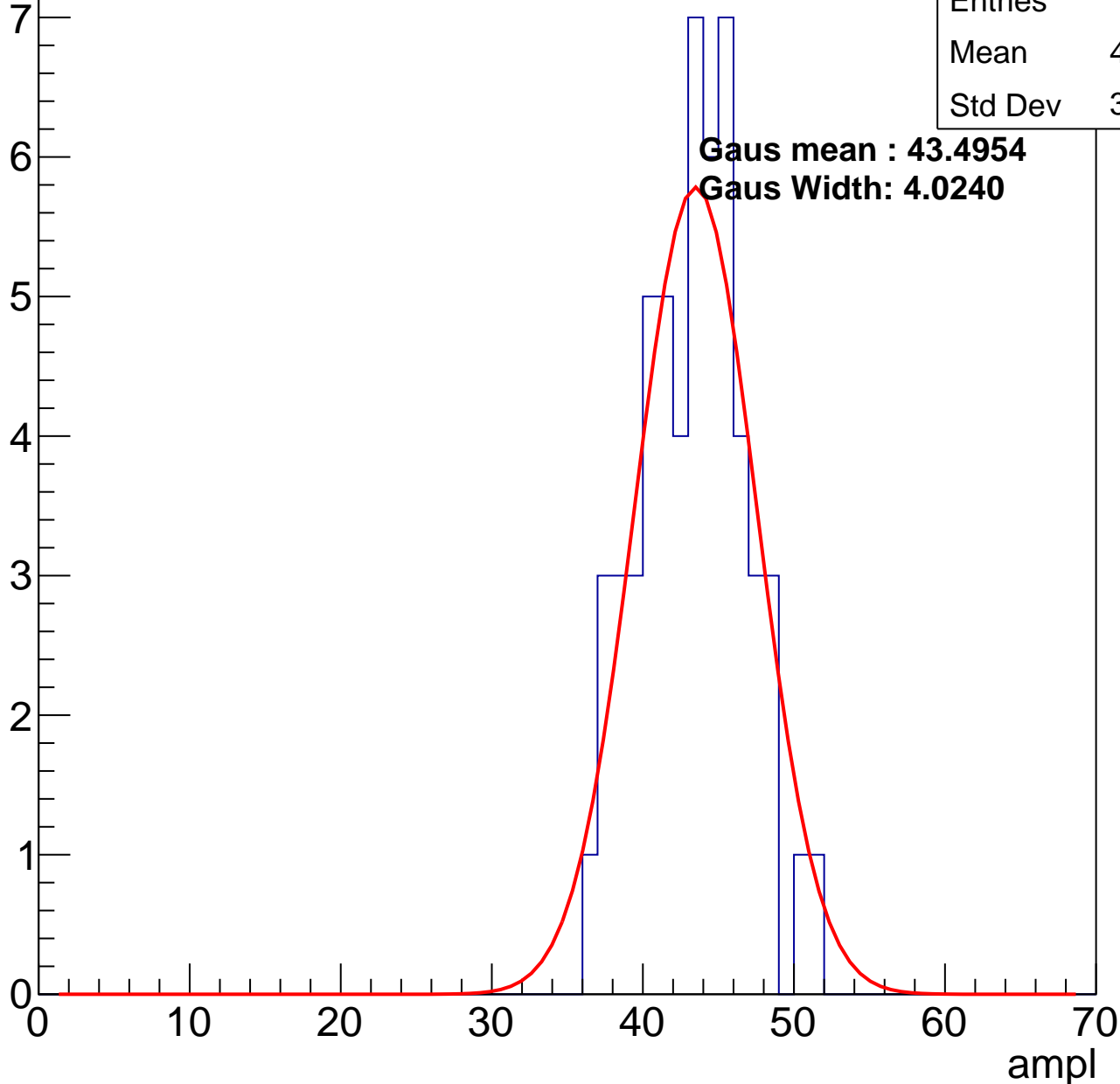
**Gaus Width: 3.7491**



# B1L100S, U6-ch93, adc2

calib\_packv5\_042523\_0143.root, FC#4, port A2

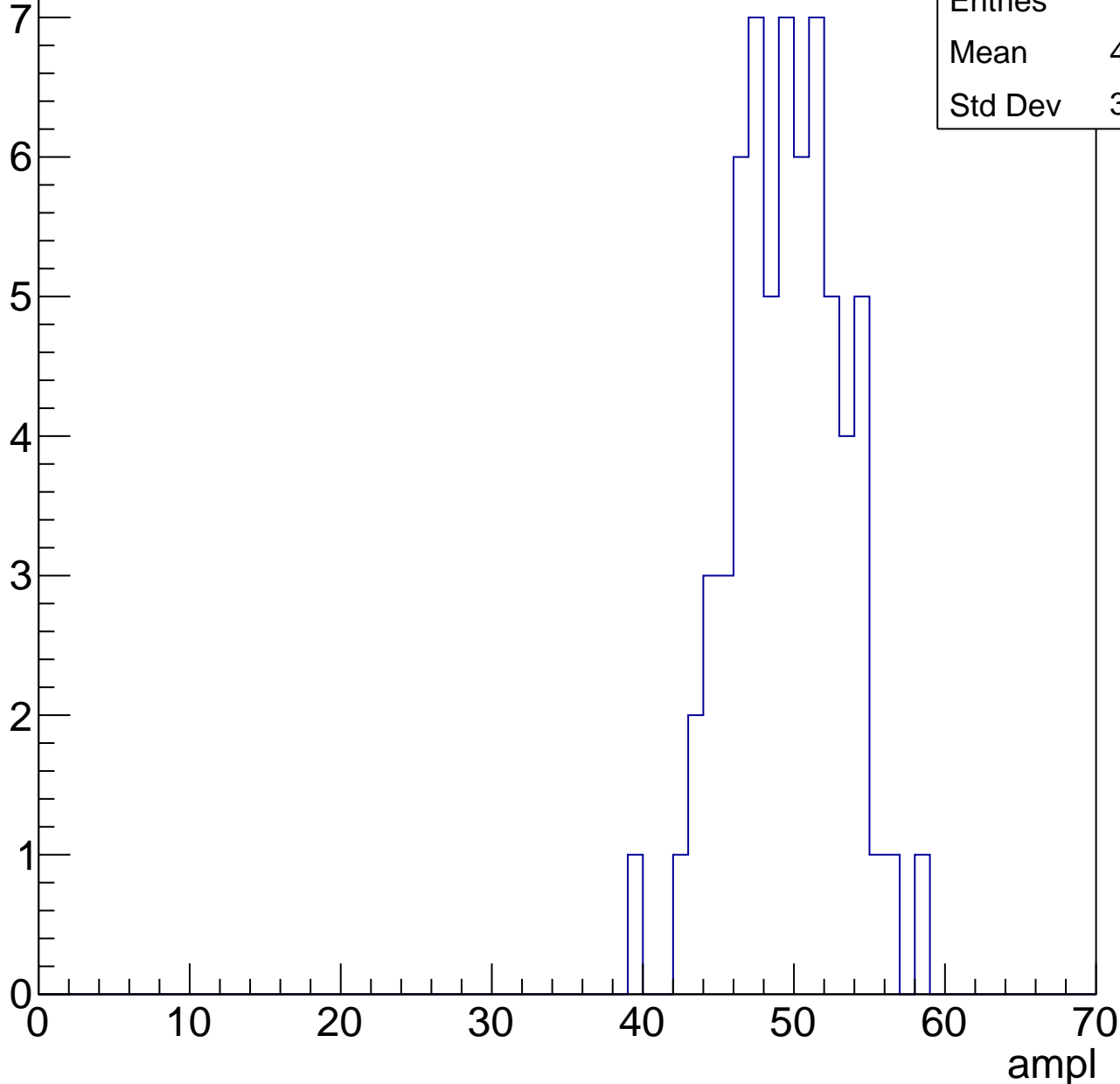
Entry



# B1L100S, U6-ch93, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

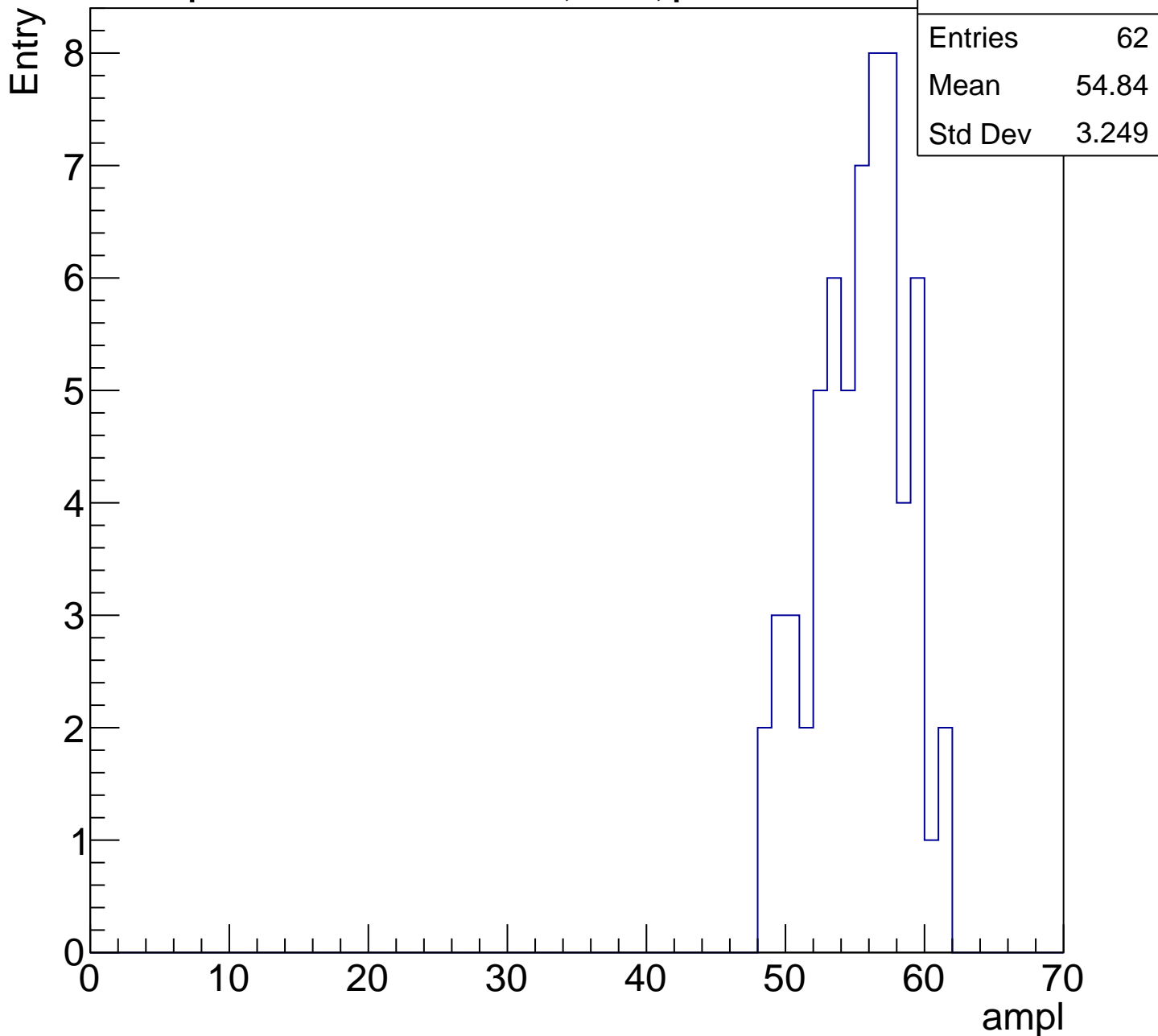
Entry



Entries	65
Mean	49.08
Std Dev	3.647

# B1L100S, U6-ch93, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2



# B1L100S, U6-ch93, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

10

8

6

4

2

0

0

10

20

30

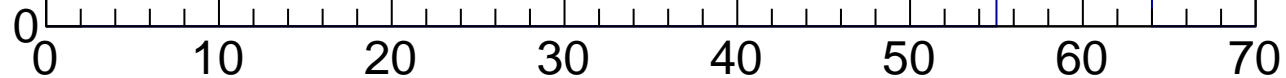
40

50

60

ampl

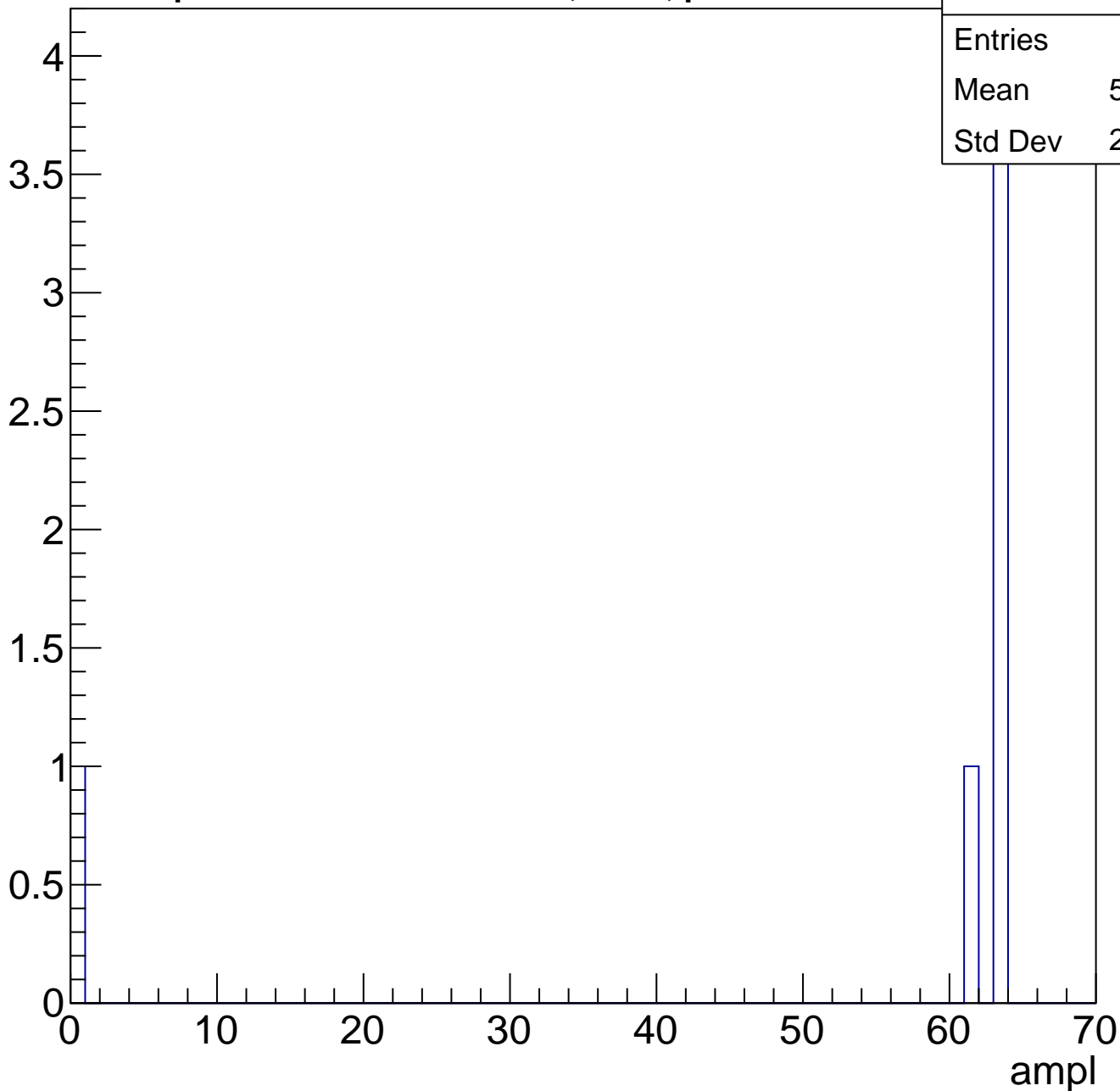
Entries	46
Mean	60.24
Std Dev	2.118



# B1L100S, U6-ch93, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry





# B1L100S, U6-ch93, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L100S, U6-ch94, adc0

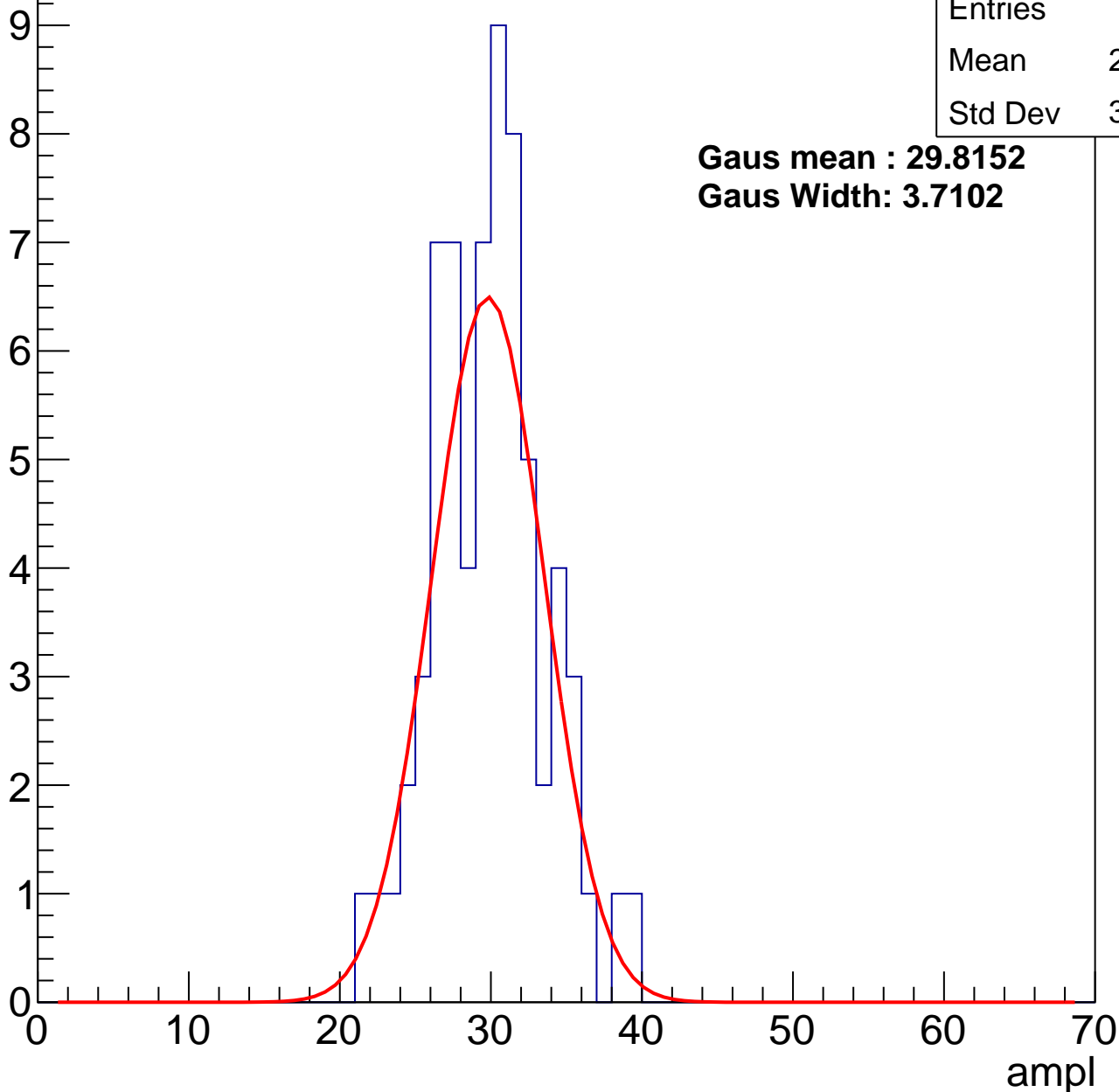
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	67
Mean	29.45
Std Dev	3.634

**Gaus mean : 29.8152**

**Gaus Width: 3.7102**



# B1L100S, U6-ch94, adc1

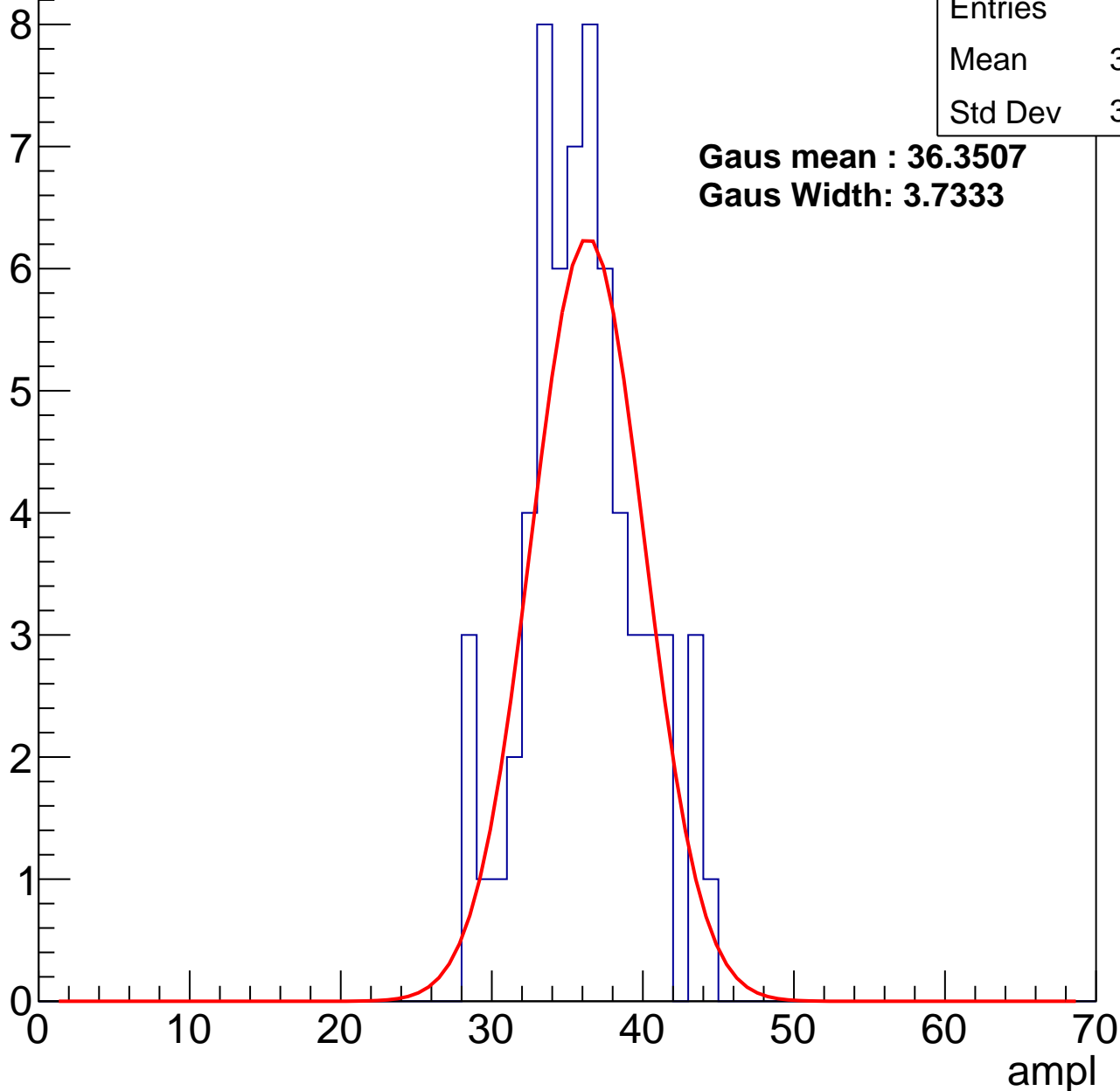
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	63
Mean	35.57
Std Dev	3.706

**Gaus mean : 36.3507**

**Gaus Width: 3.7333**



# B1L100S, U6-ch94, adc2

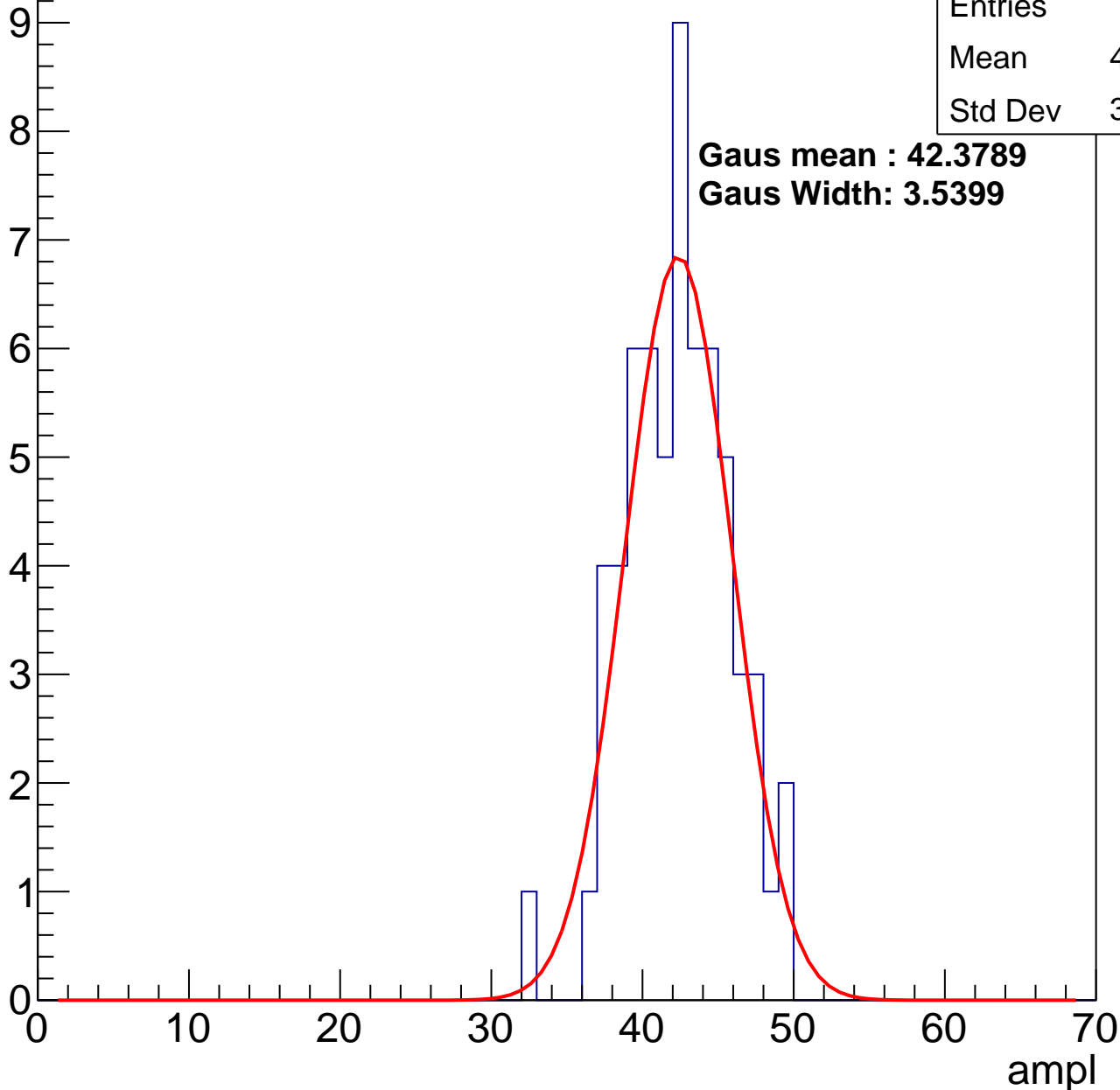
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	62
Mean	41.89
Std Dev	3.394

**Gaus mean : 42.3789**

**Gaus Width: 3.5399**

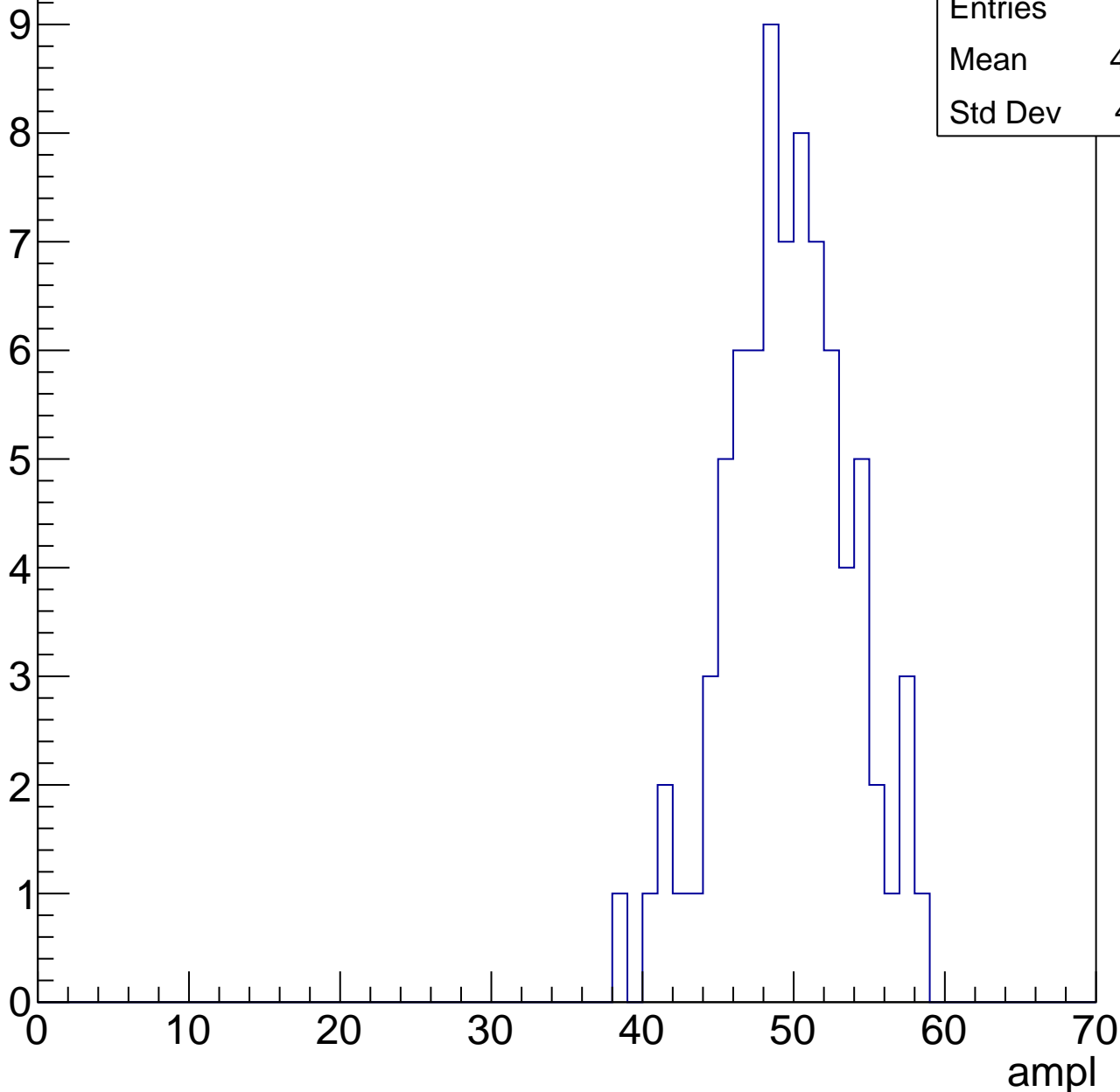


# B1L100S, U6-ch94, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

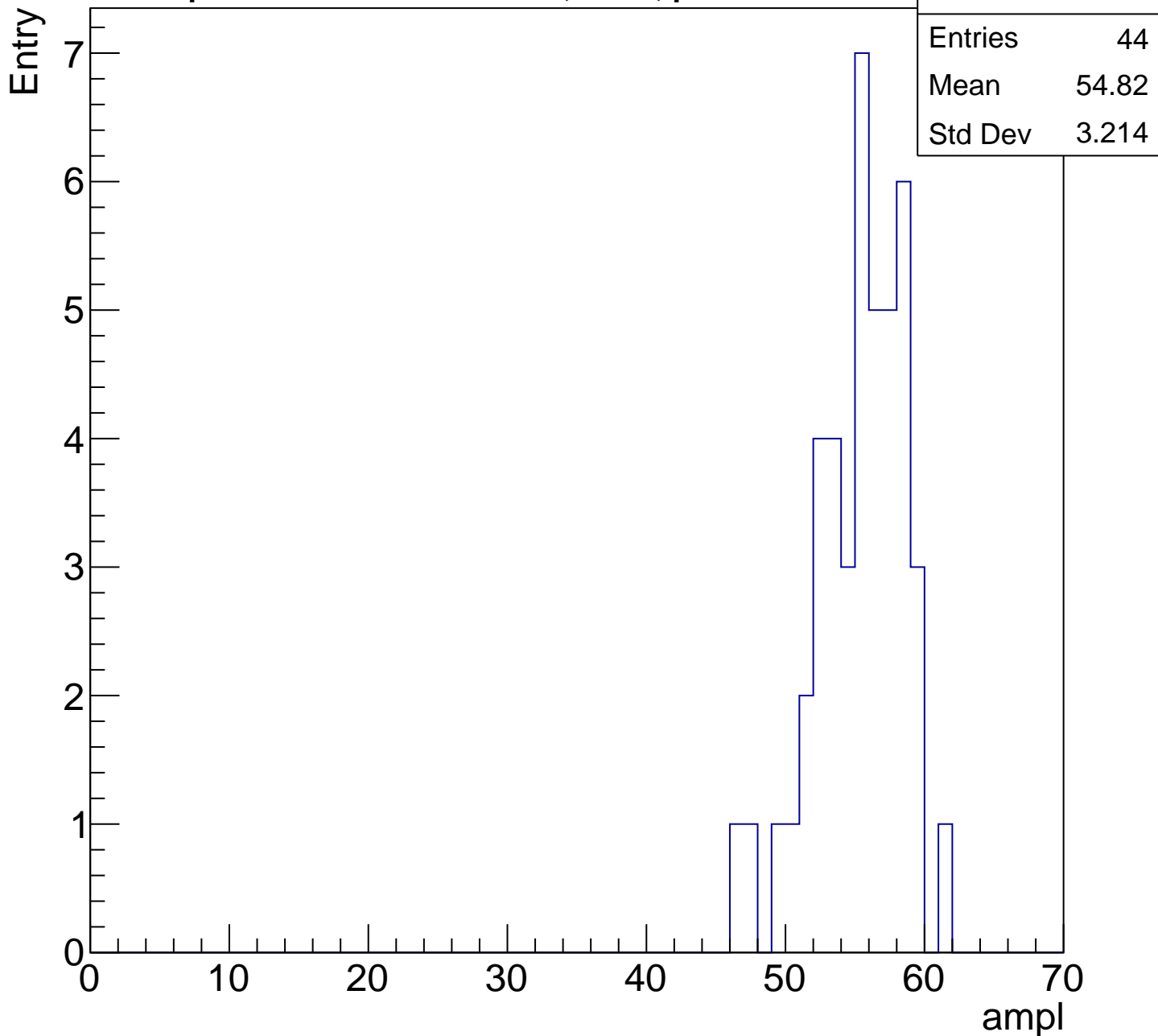
Entry

Entries	79
Mean	49.13
Std Dev	4.101



# B1L100S, U6-ch94, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

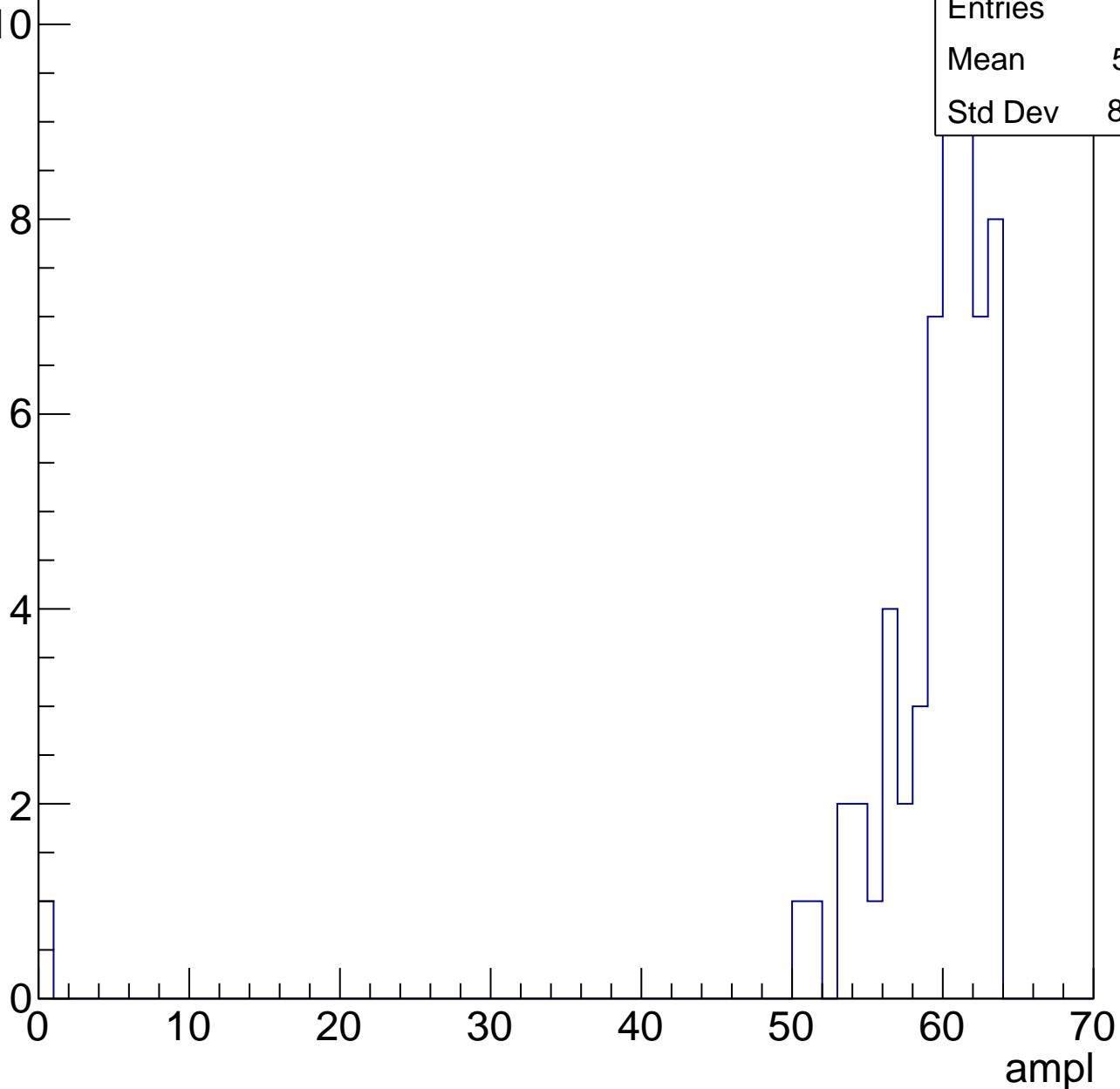


# B1L100S, U6-ch94, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

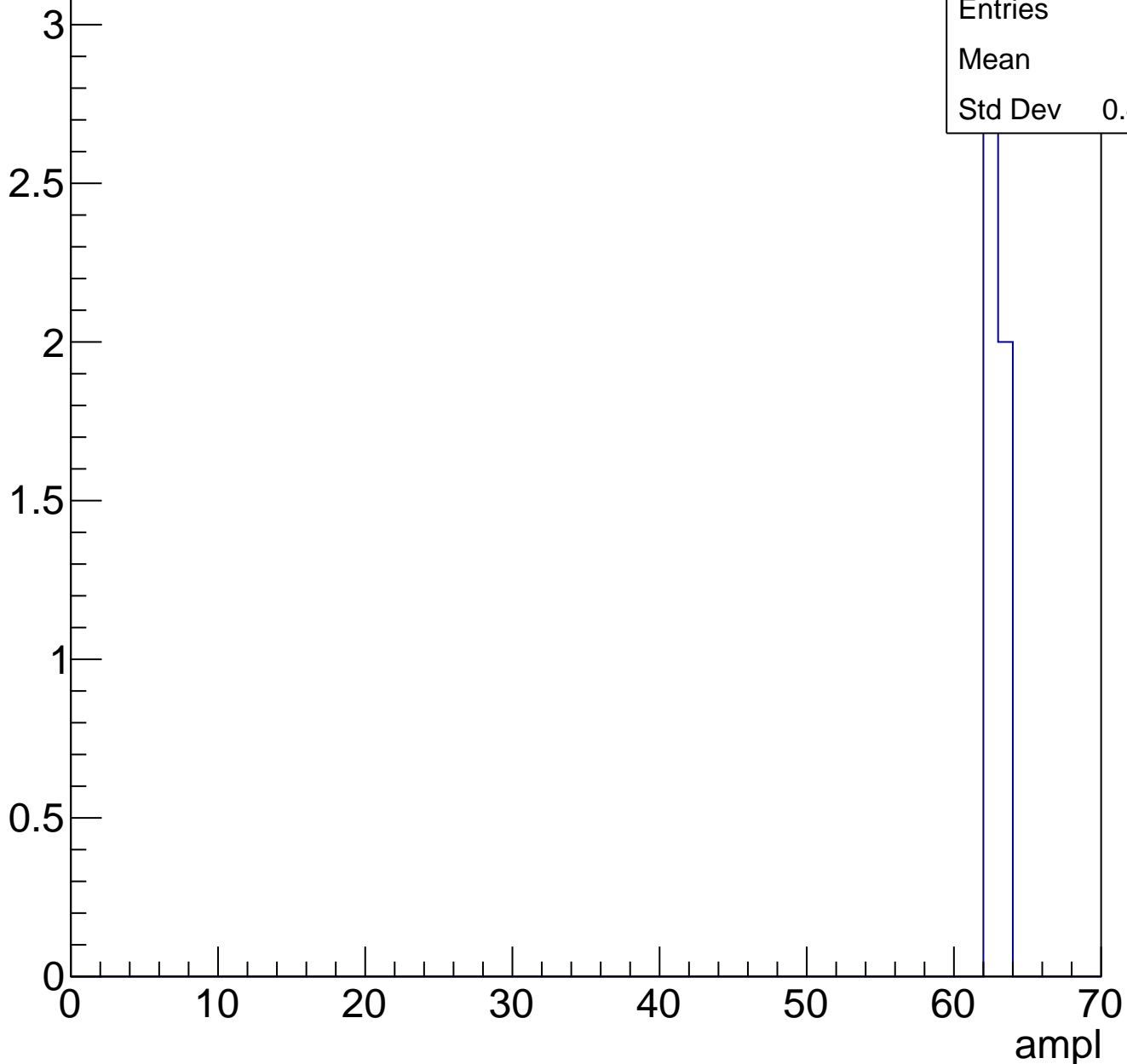
Entries	58
Mean	58.31
Std Dev	8.326



# B1L100S, U6-ch94, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry





# B1L100S, U6-ch94, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L100S, U6-ch95, adc0

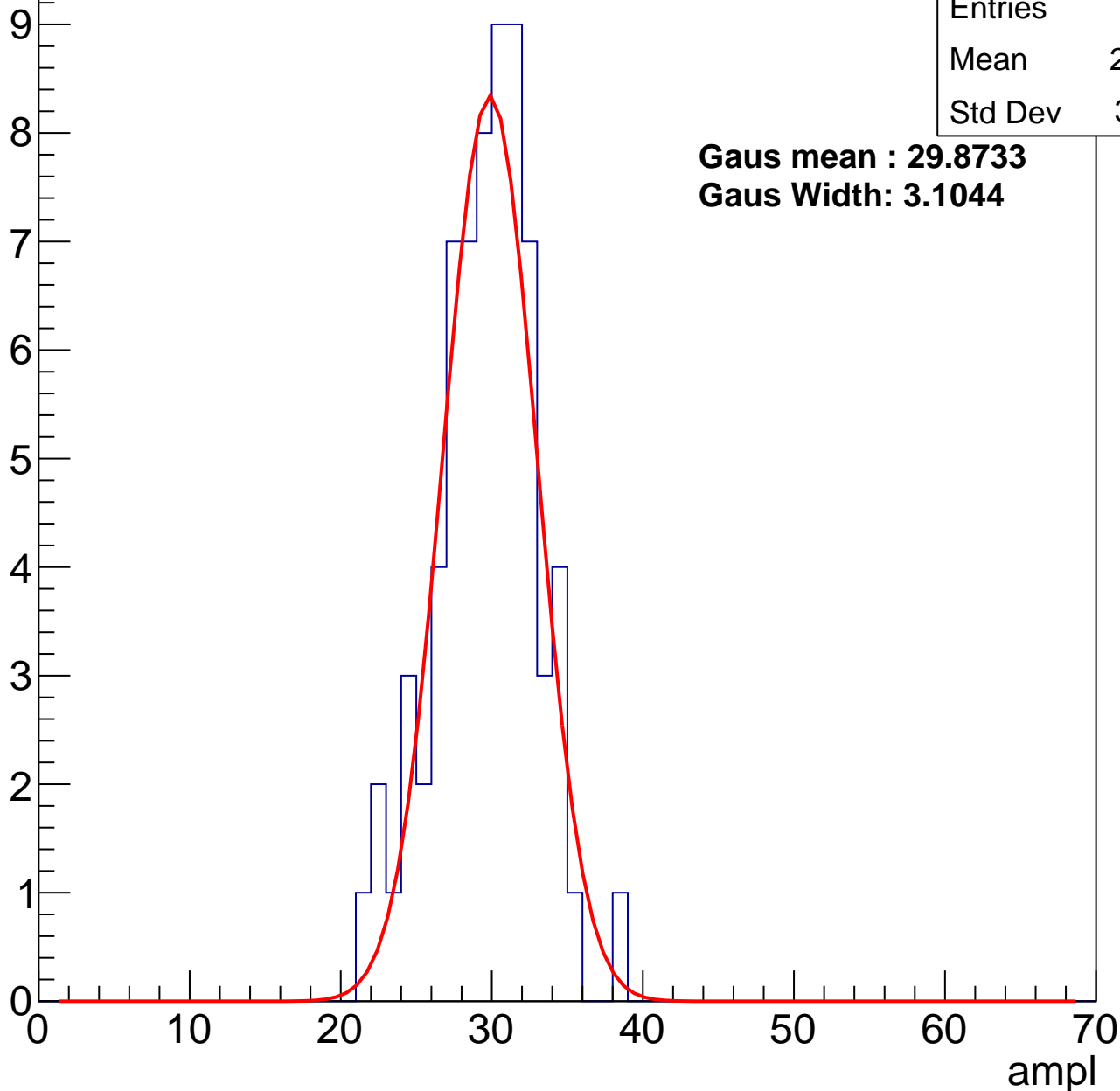
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	69
Mean	29.16
Std Dev	3.291

**Gaus mean : 29.8733**

**Gaus Width: 3.1044**



# B1L100S, U6-ch95, adc1

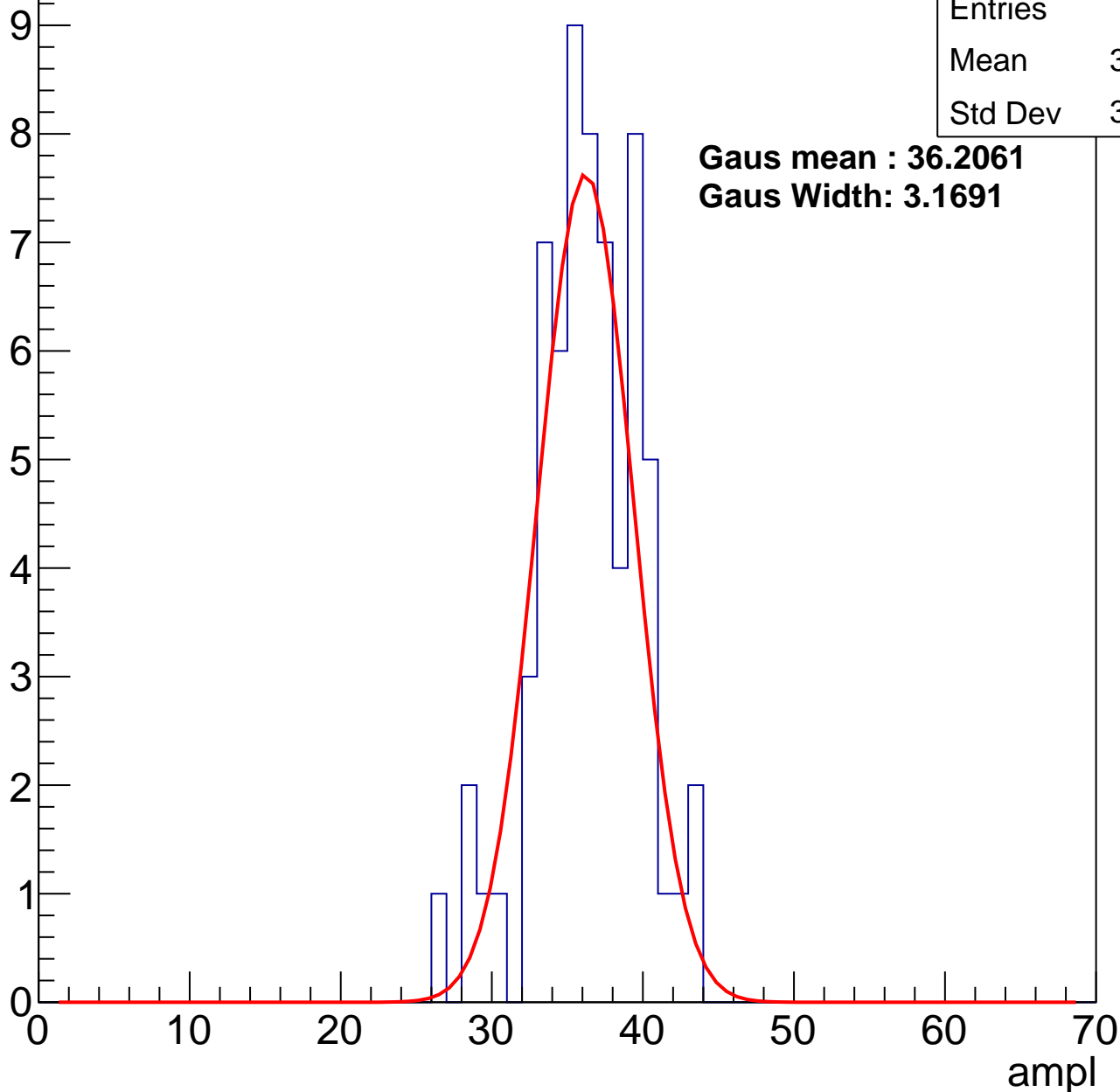
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	66
Mean	35.86
Std Dev	3.459

**Gaus mean : 36.2061**

**Gaus Width: 3.1691**



# B1L100S, U6-ch95, adc2

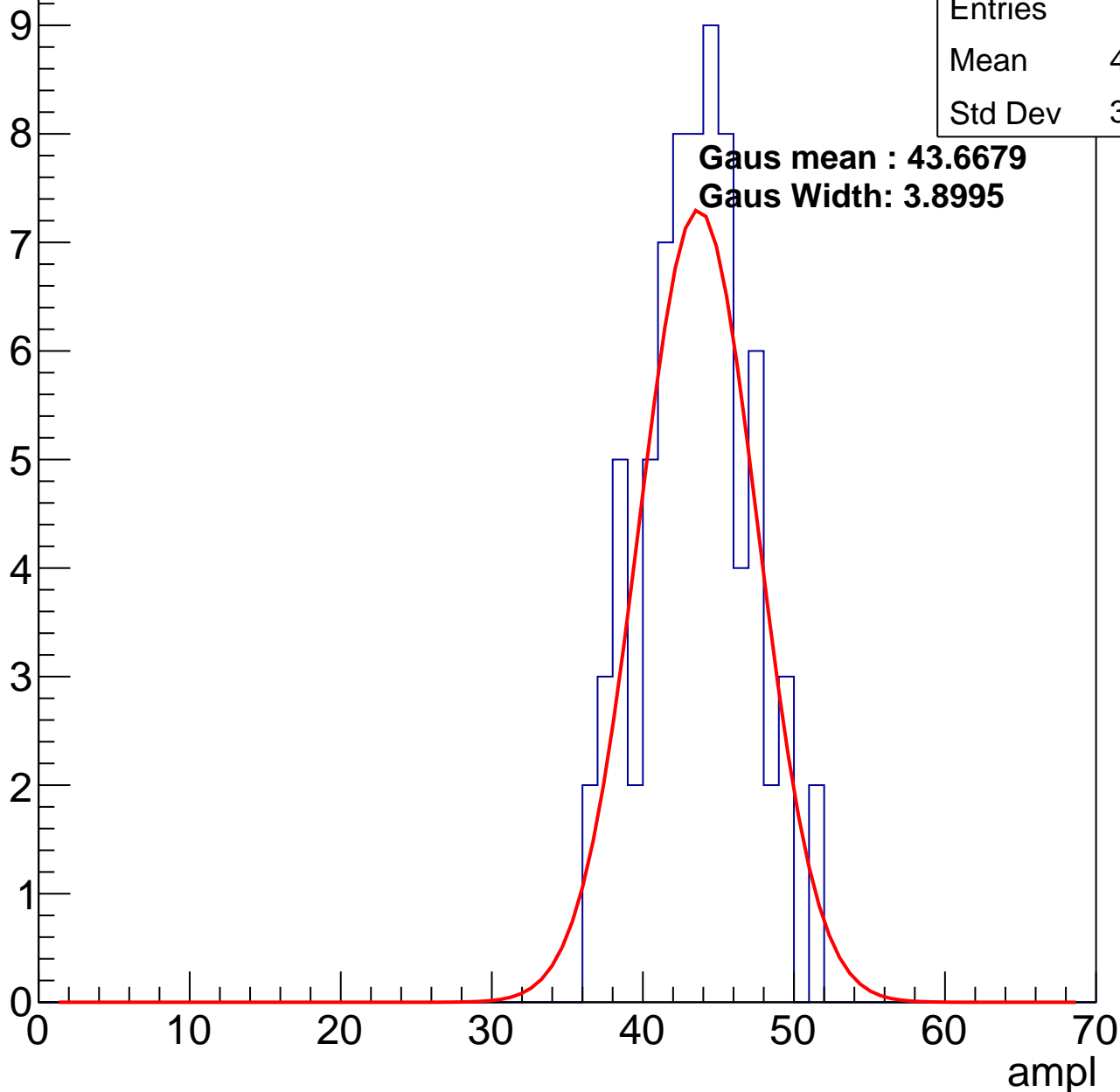
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	74
Mean	43.04
Std Dev	3.493

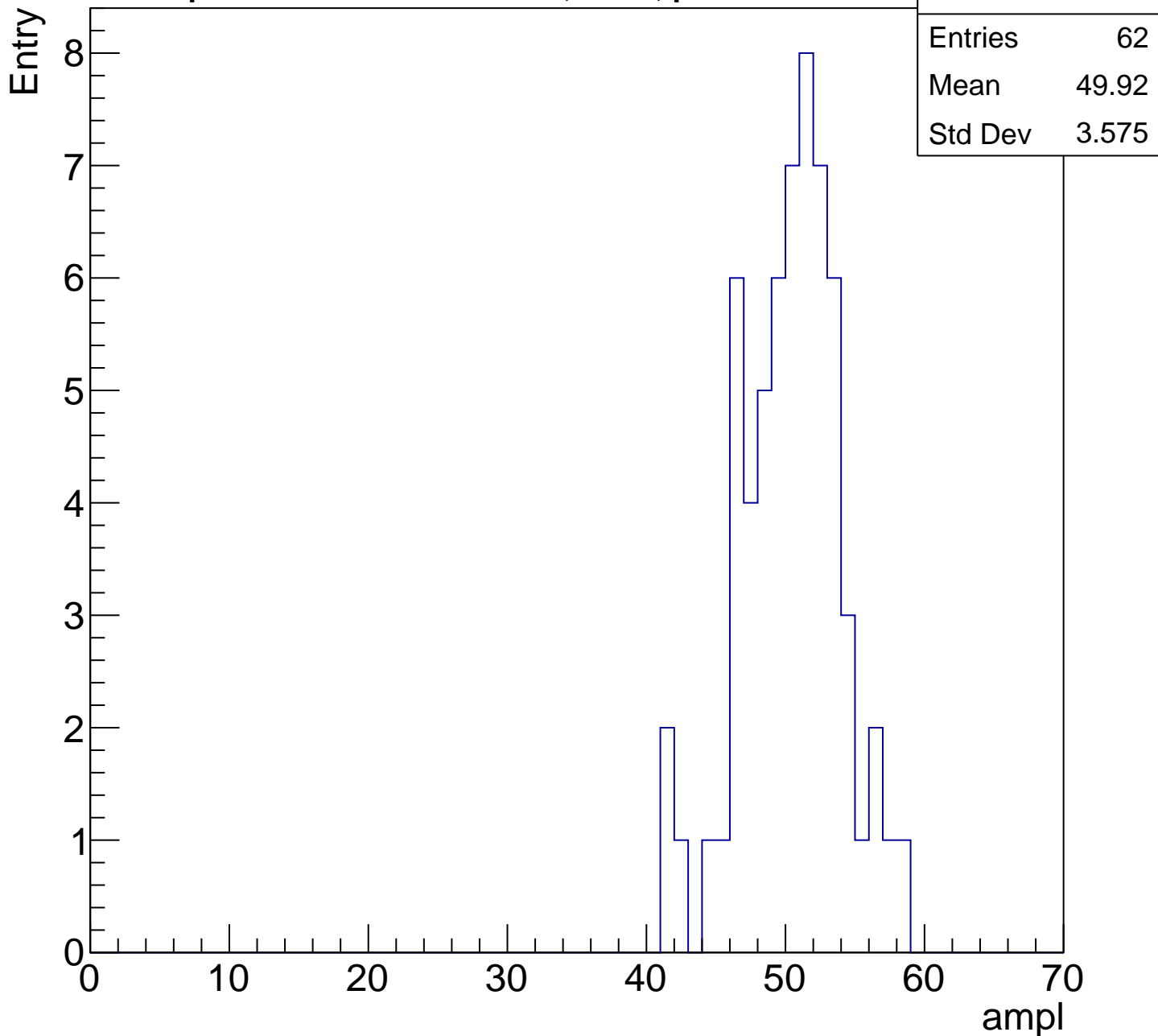
**Gaus mean : 43.6679**

**Gaus Width: 3.8995**



# B1L100S, U6-ch95, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2



# B1L100S, U6-ch95, adc4

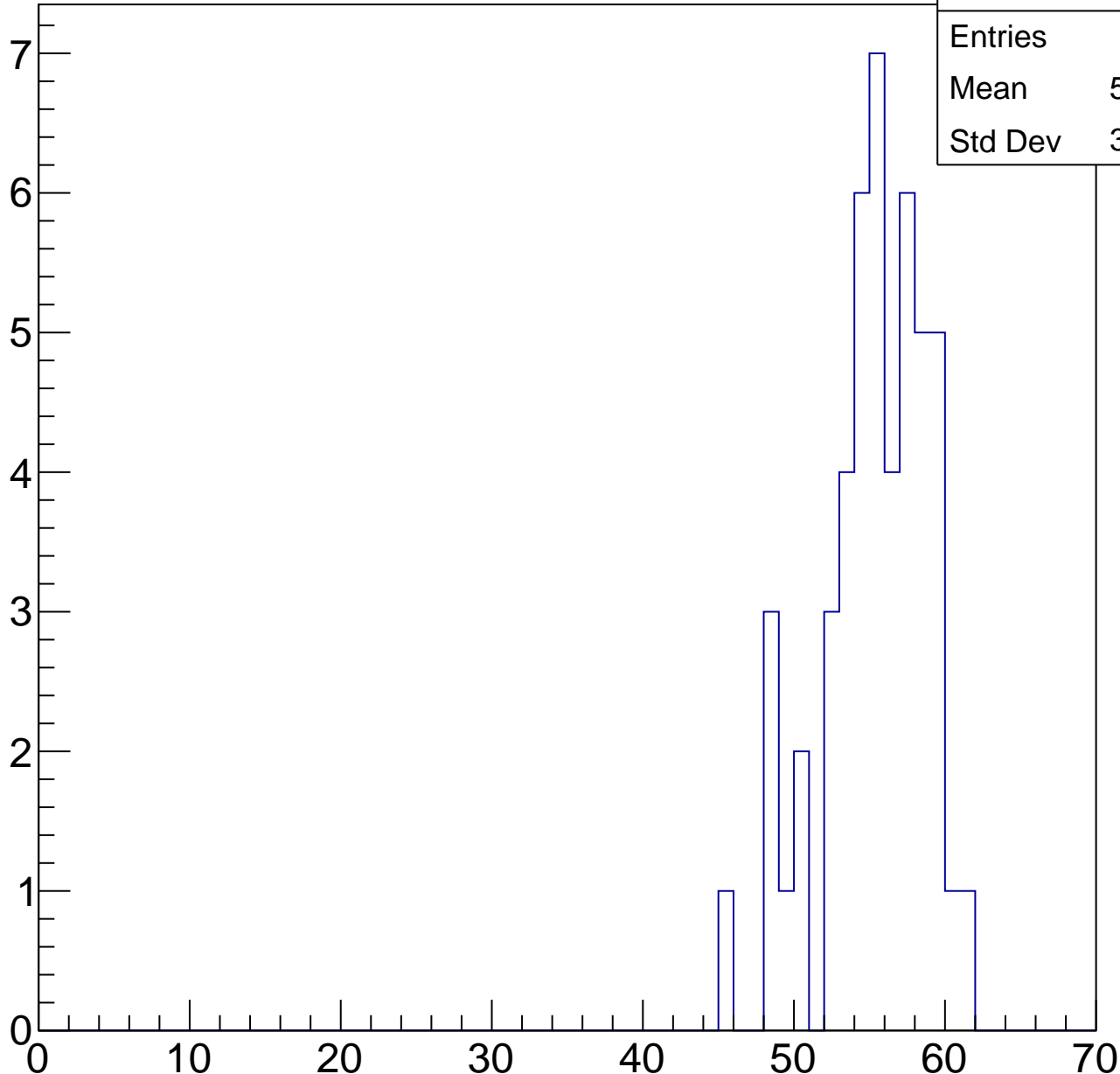
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

7  
6  
5  
4  
3  
2  
1  
0

Entries	49
Mean	54.84
Std Dev	3.484

ampl



# B1L100S, U6-ch95, adc5

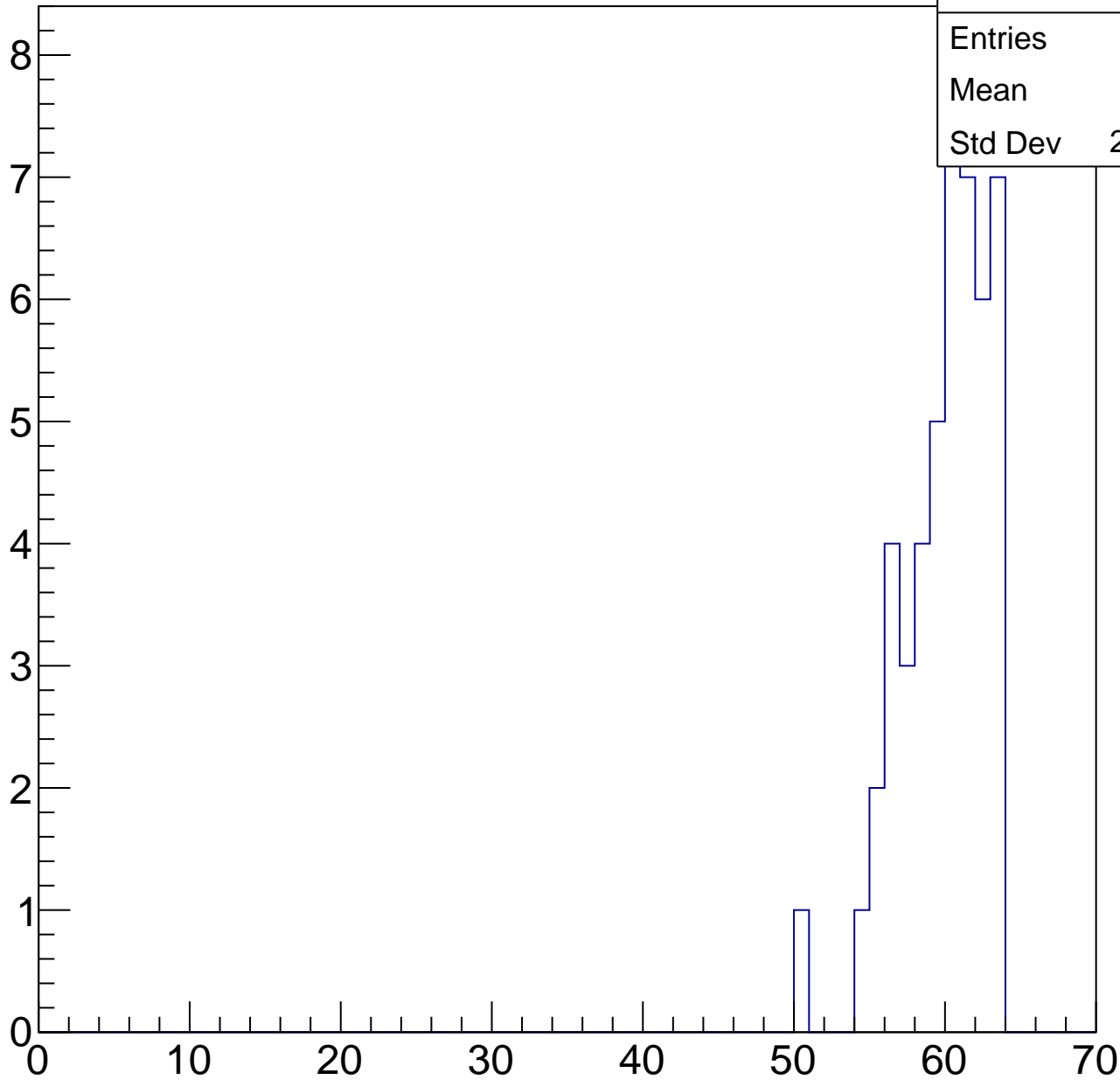
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	48
Mean	59.5
Std Dev	2.814

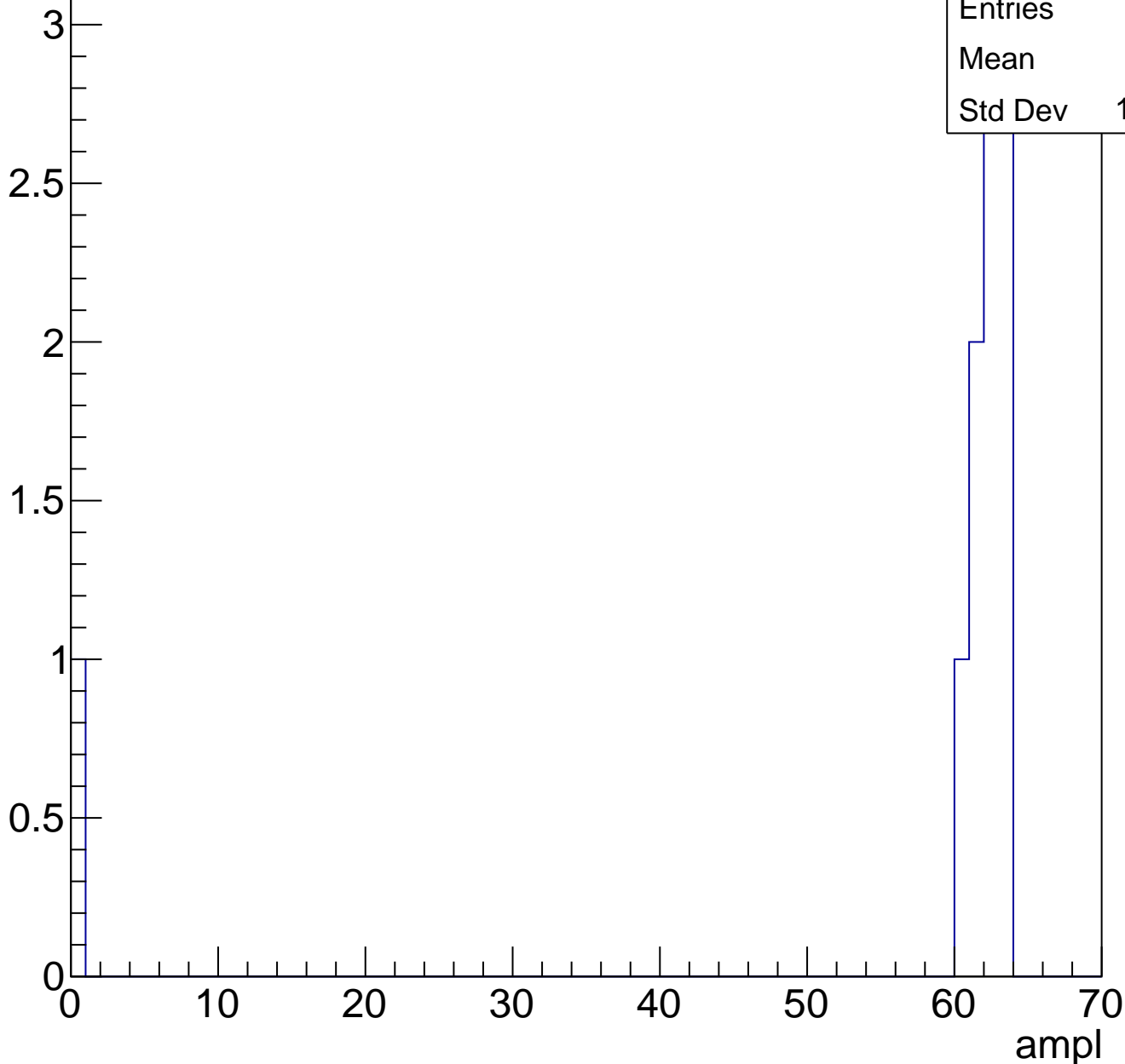
ampl



# B1L100S, U6-ch95, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry





# B1L100S, U6-ch95, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



# B1L100S, U6-ch96, adc0

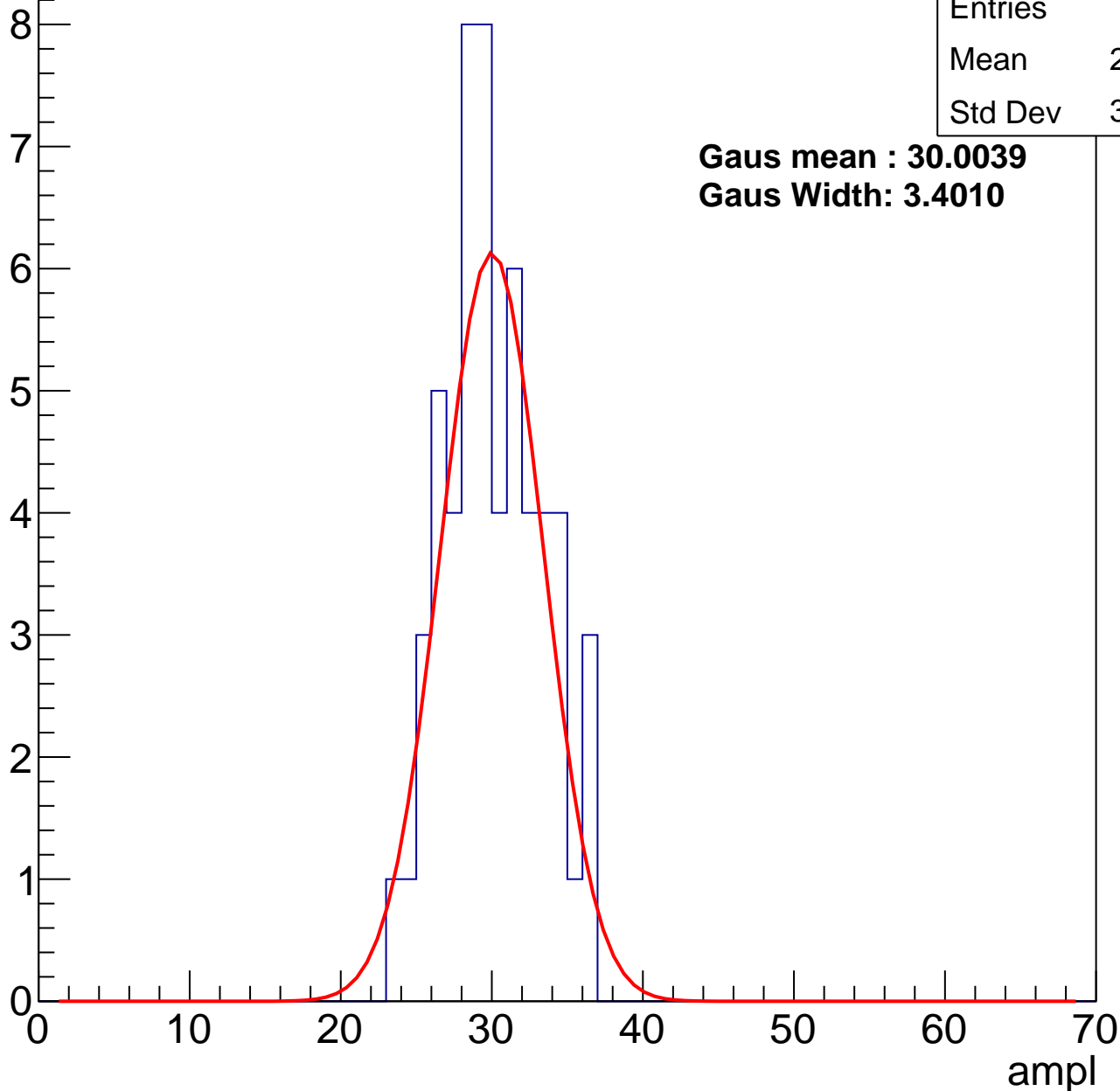
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	56
Mean	29.66
Std Dev	3.175

**Gaus mean : 30.0039**

**Gaus Width: 3.4010**



# B1L100S, U6-ch96, adc1

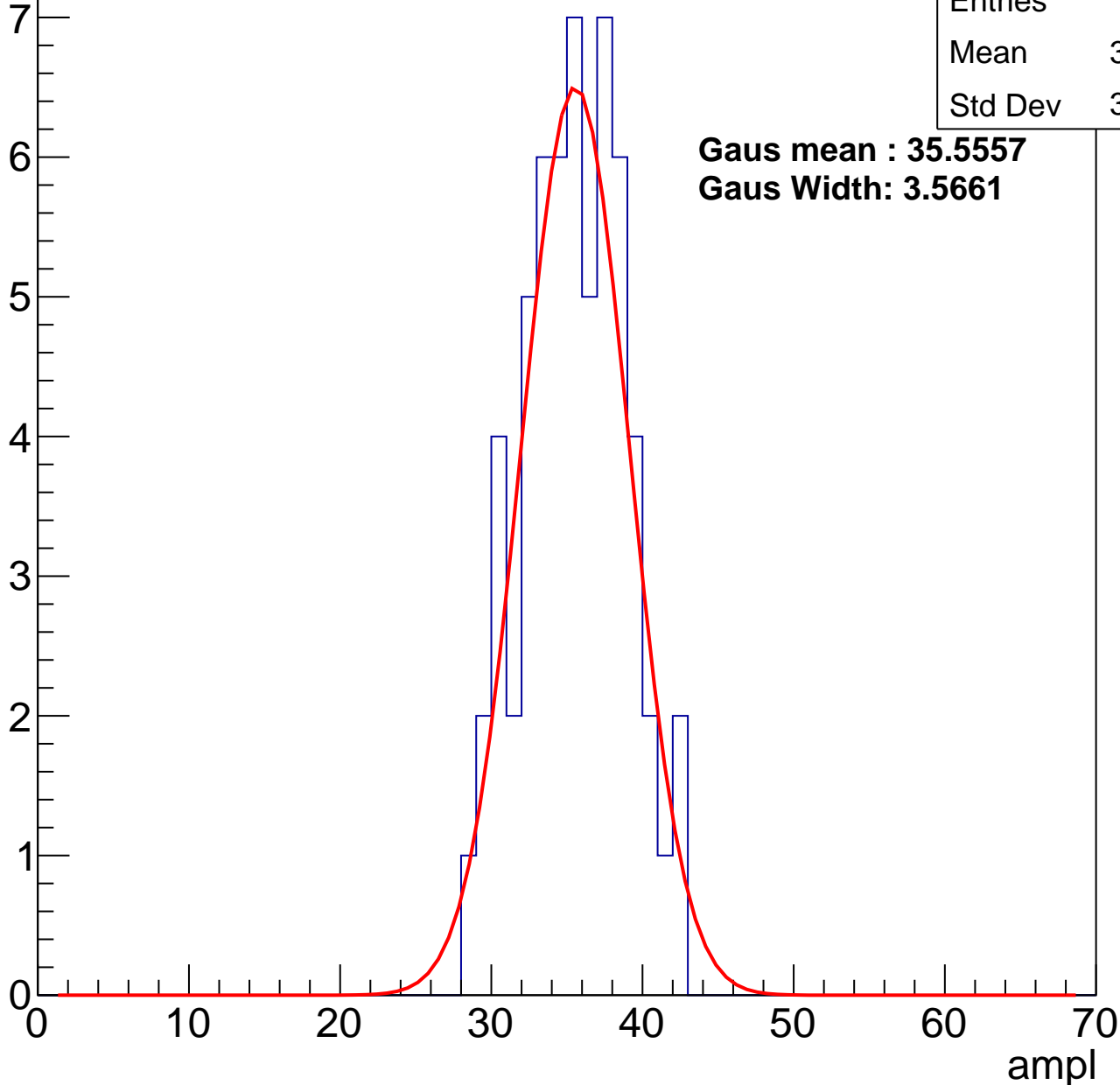
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	60
Mean	35.05
Std Dev	3.324

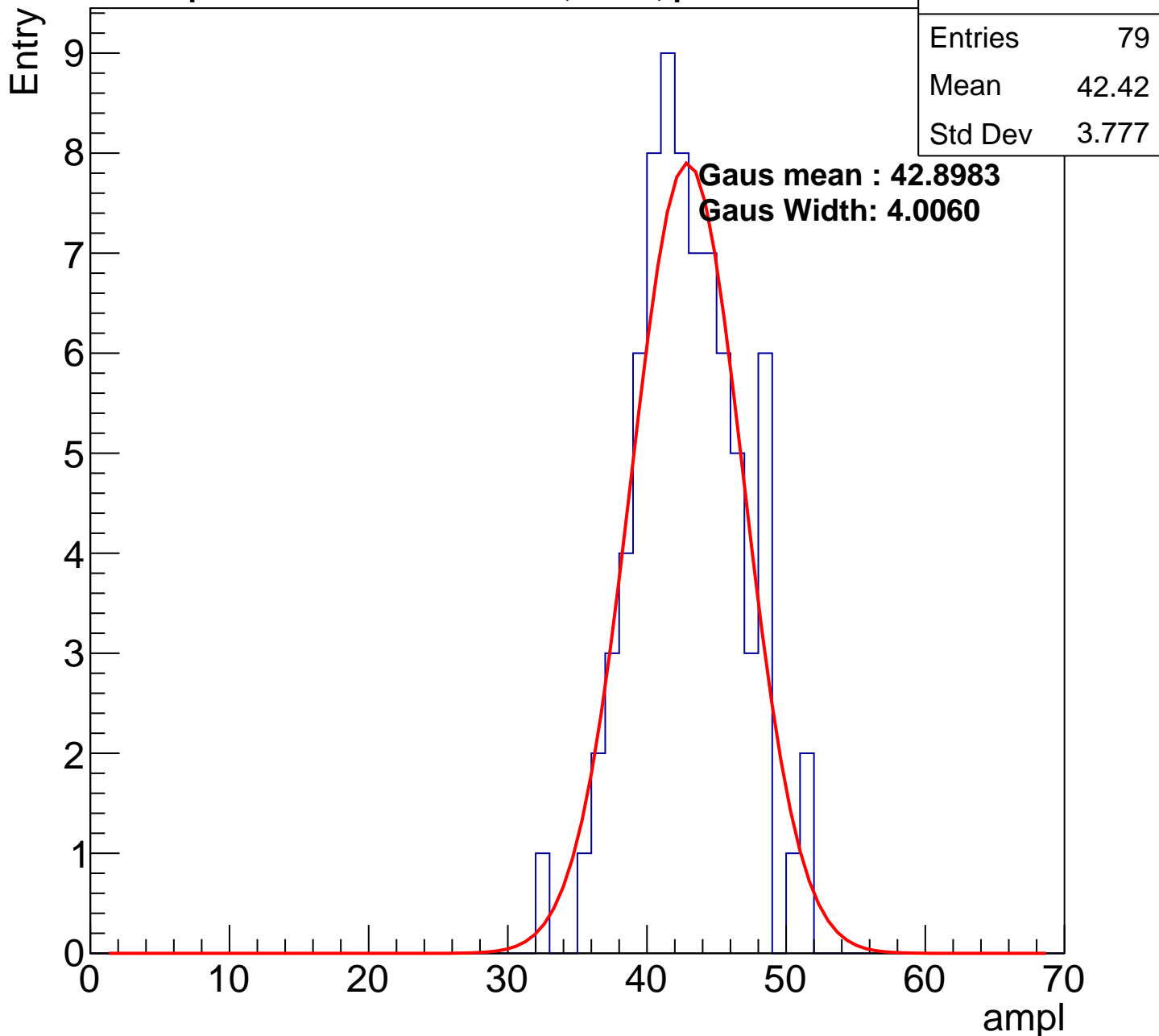
**Gaus mean : 35.5557**

**Gaus Width: 3.5661**



# B1L100S, U6-ch96, adc2

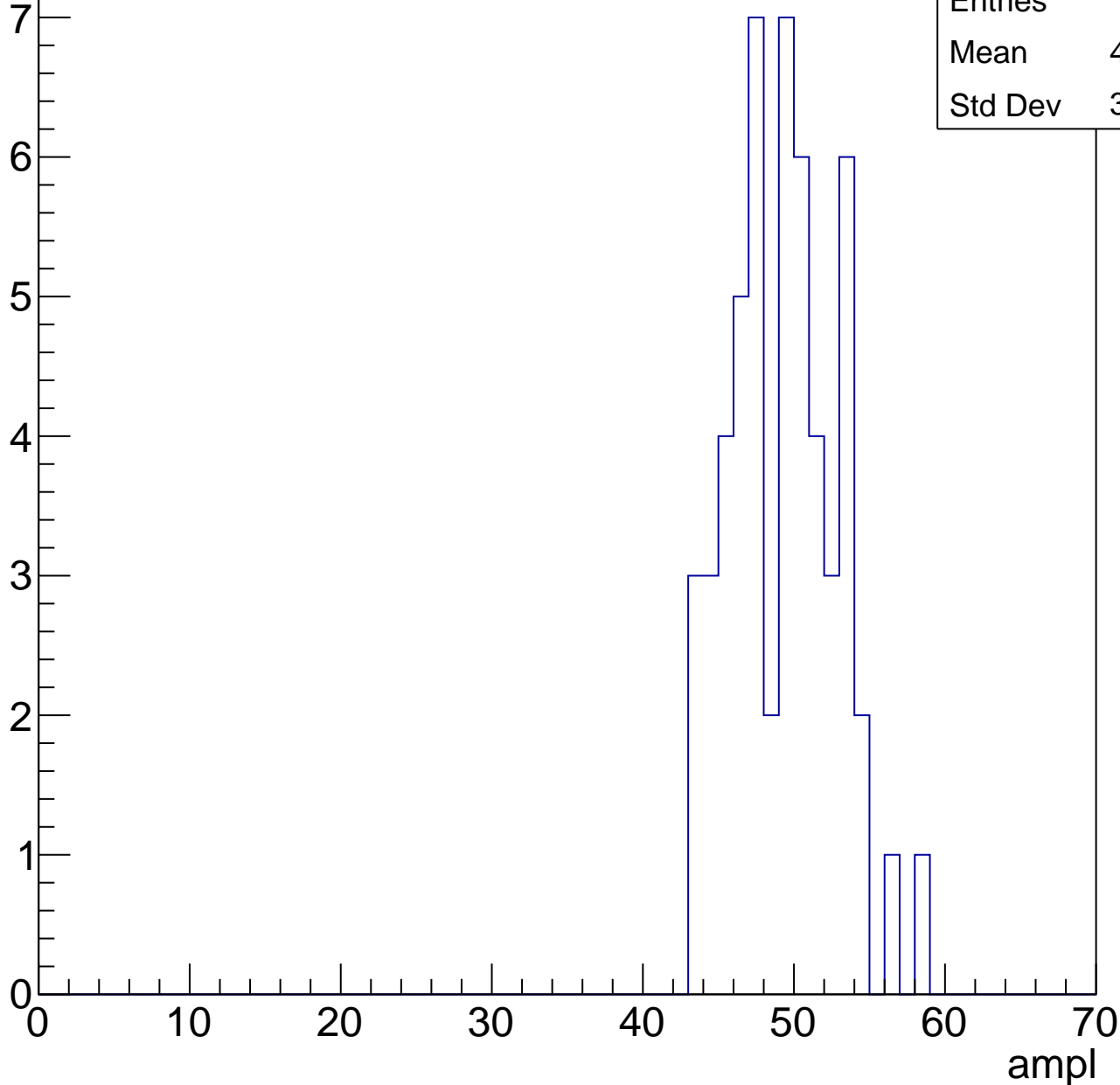
calib\_packv5\_042523\_0143.root, FC#4, port A2



# B1L100S, U6-ch96, adc3

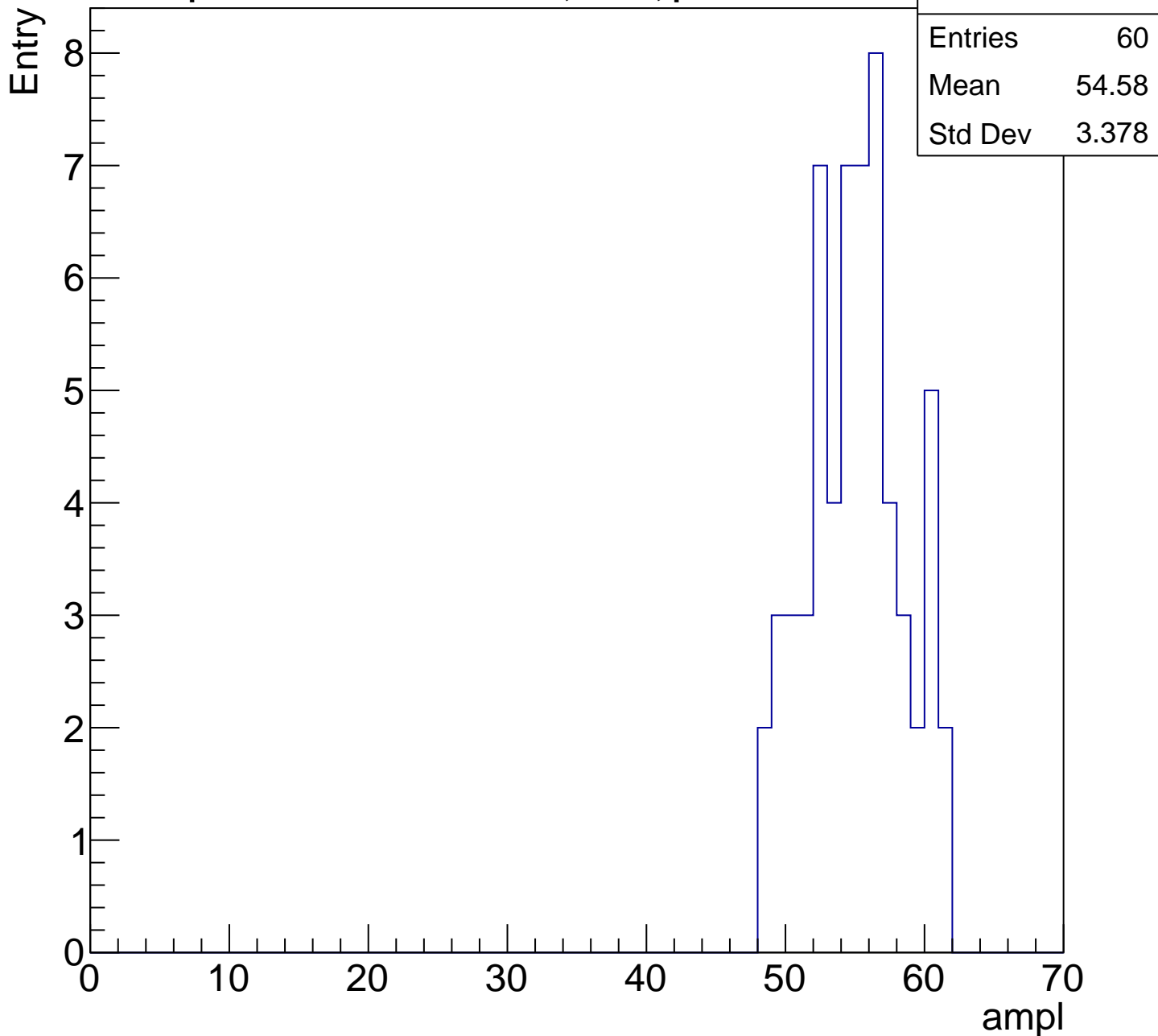
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



# B1L100S, U6-ch96, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2



# B1L100S, U6-ch96, adc5

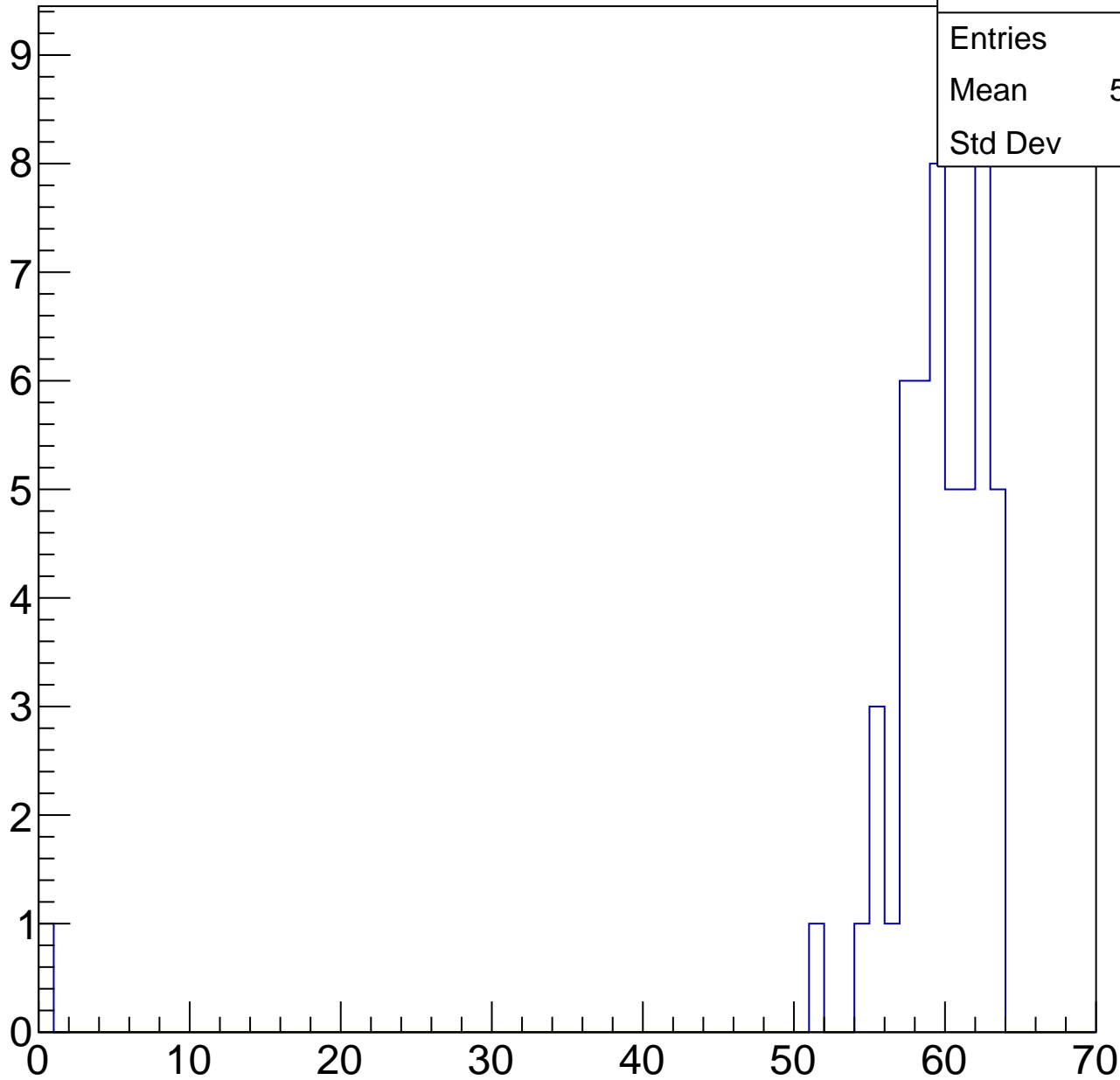
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	51
Mean	58.16
Std Dev	8.64

ampl

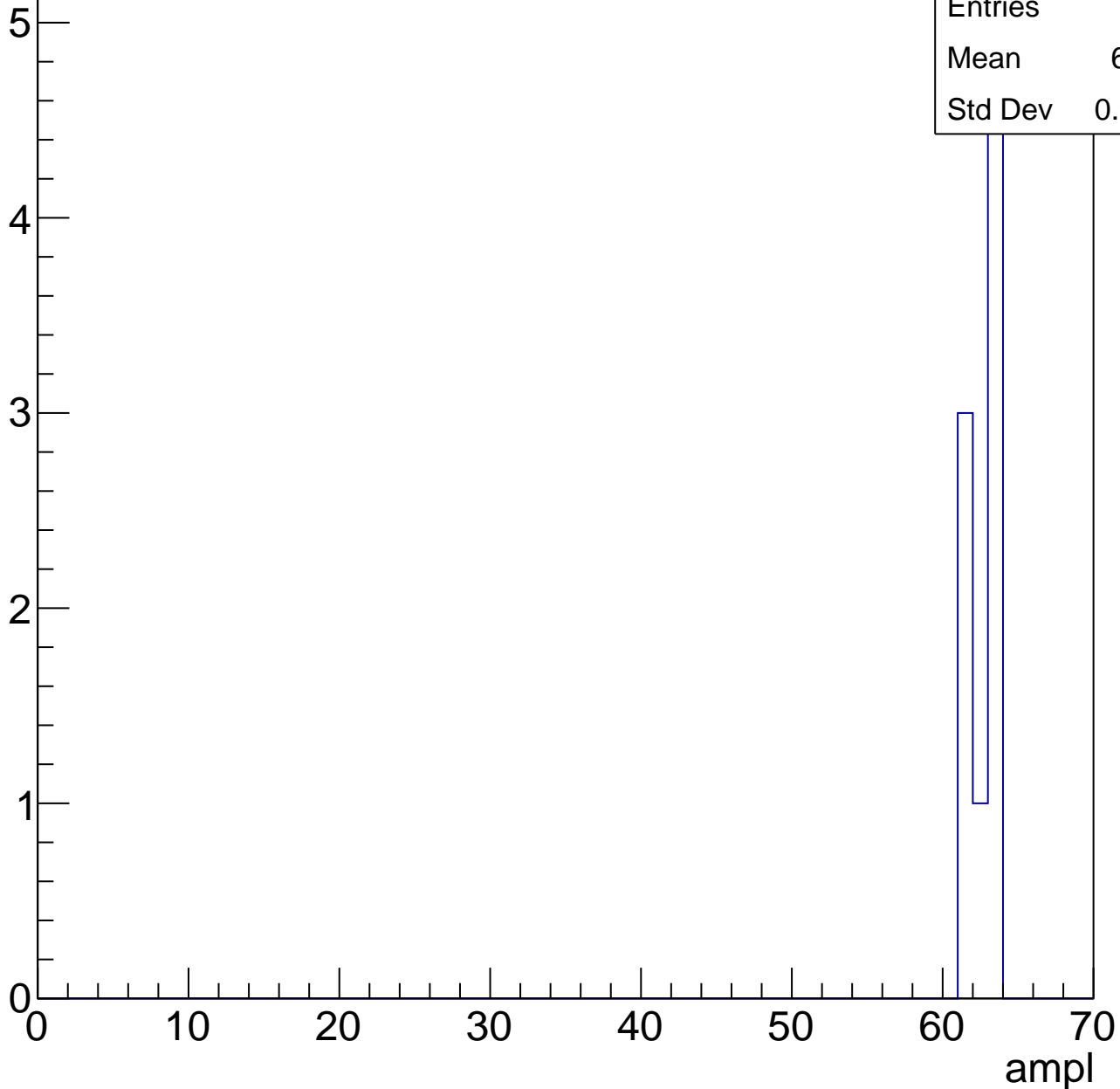


# B1L100S, U6-ch96, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	9
Mean	62.22
Std Dev	0.9162





# B1L100S, U6-ch96, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



# B1L100S, U6-ch97, adc0

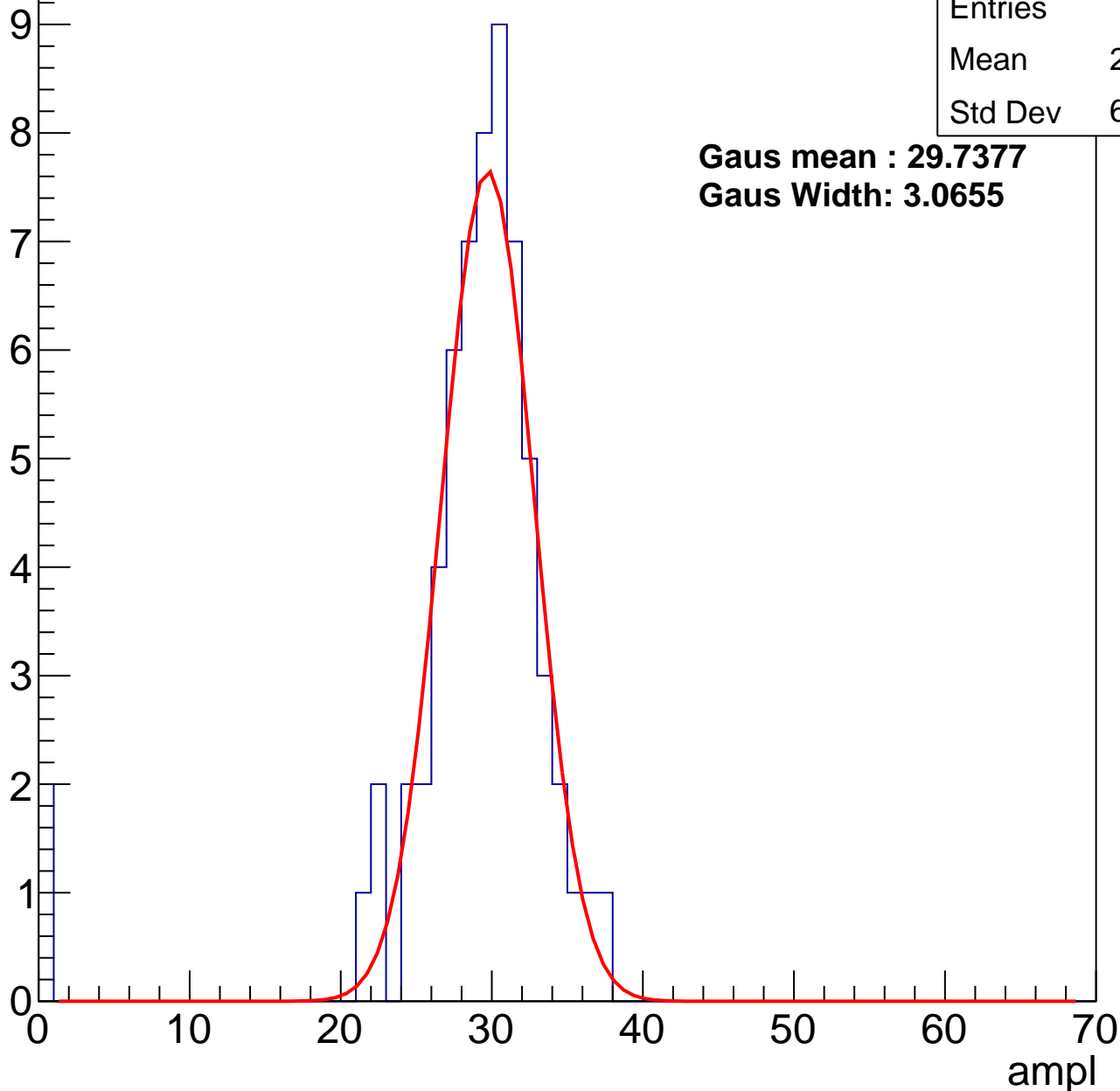
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	63
Mean	28.24
Std Dev	6.023

**Gaus mean : 29.7377**

**Gaus Width: 3.0655**



# B1L100S, U6-ch97, adc1

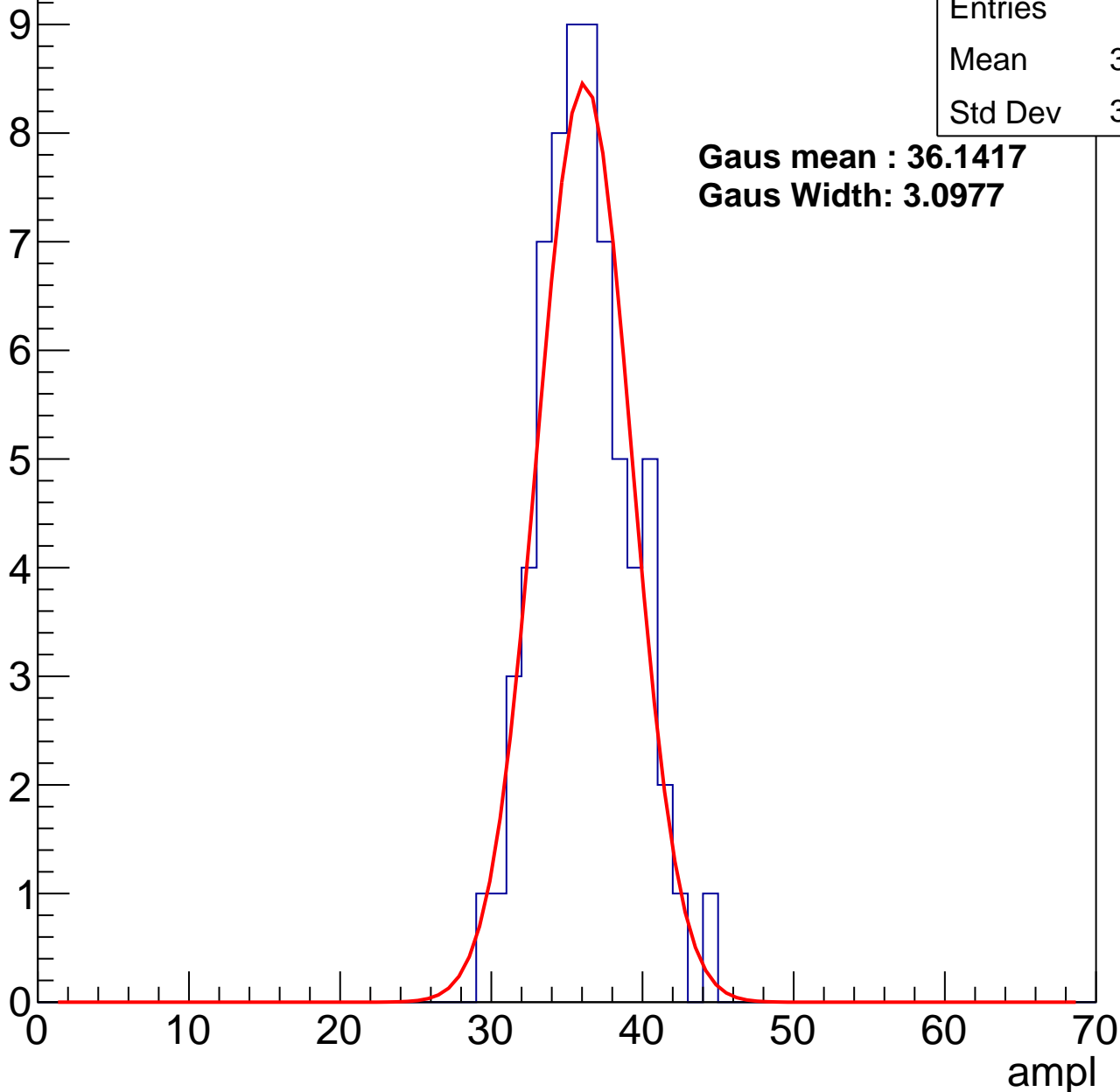
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	67
Mean	35.75
Std Dev	3.034

**Gaus mean : 36.1417**

**Gaus Width: 3.0977**



# B1L100S, U6-ch97, adc2

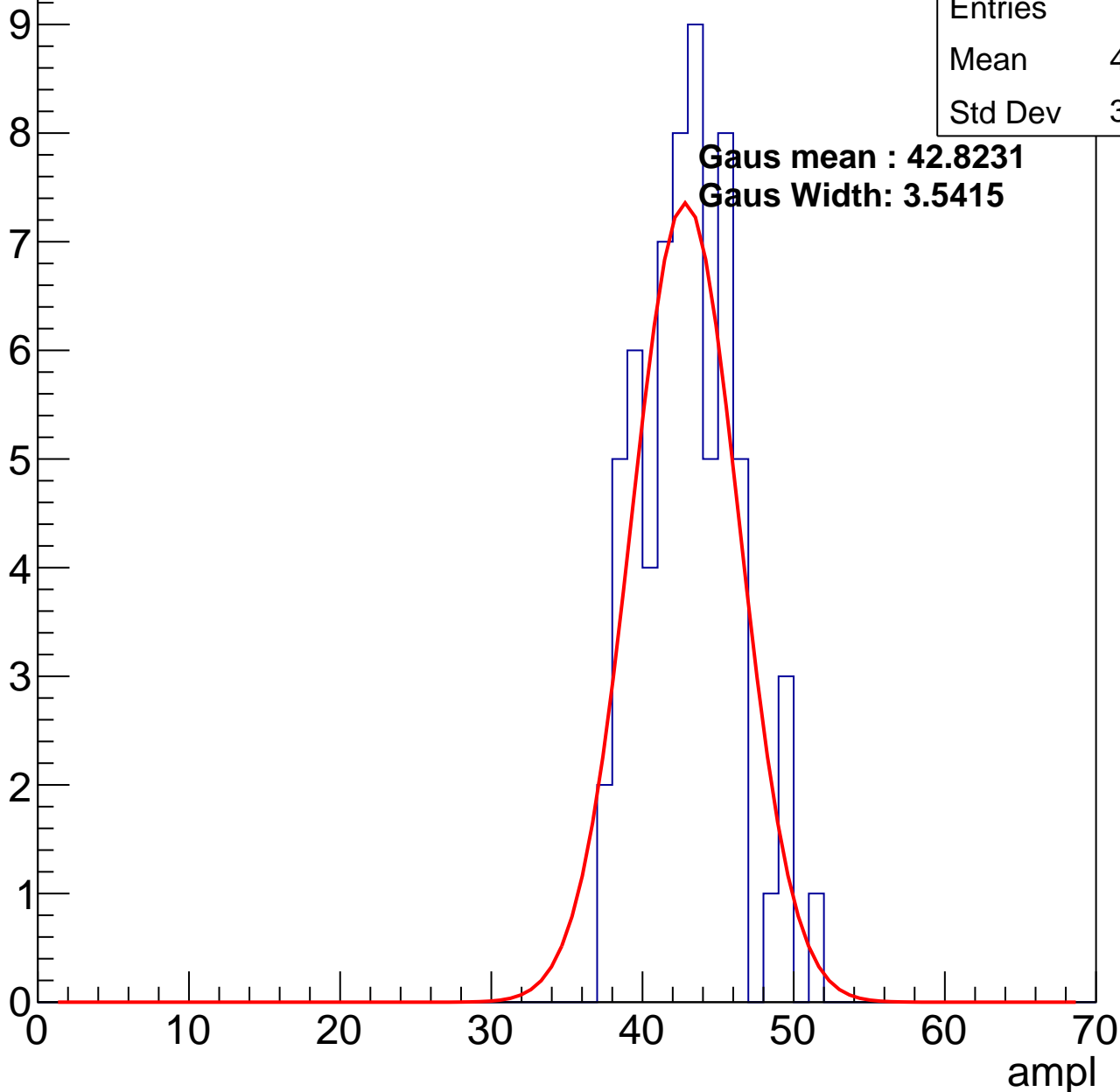
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	64
Mean	42.56
Std Dev	3.142

**Gaus mean : 42.8231**

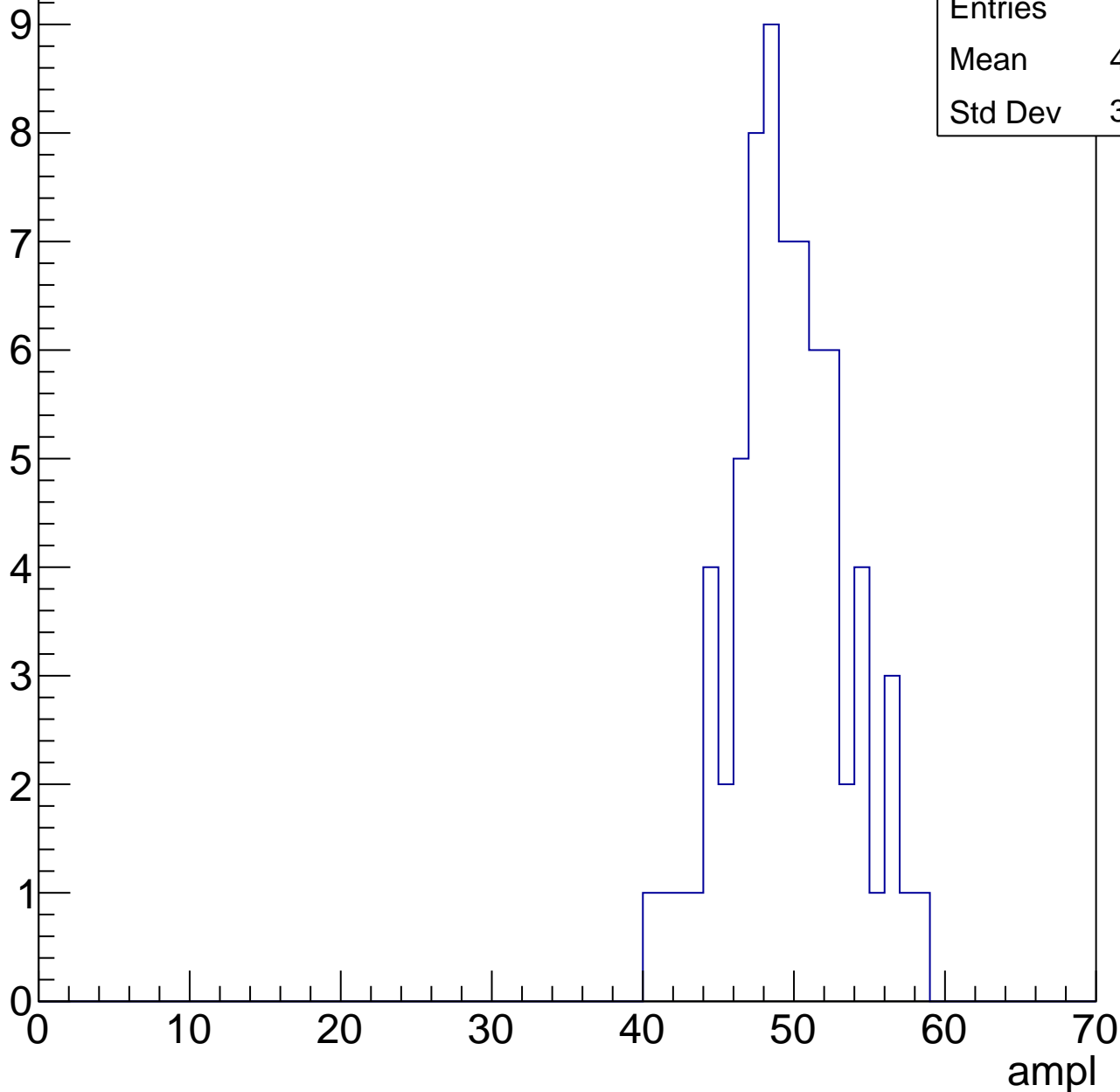
**Gaus Width: 3.5415**



# B1L100S, U6-ch97, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	70
Mean	49.16
Std Dev	3.763

# B1L100S, U6-ch97, adc4

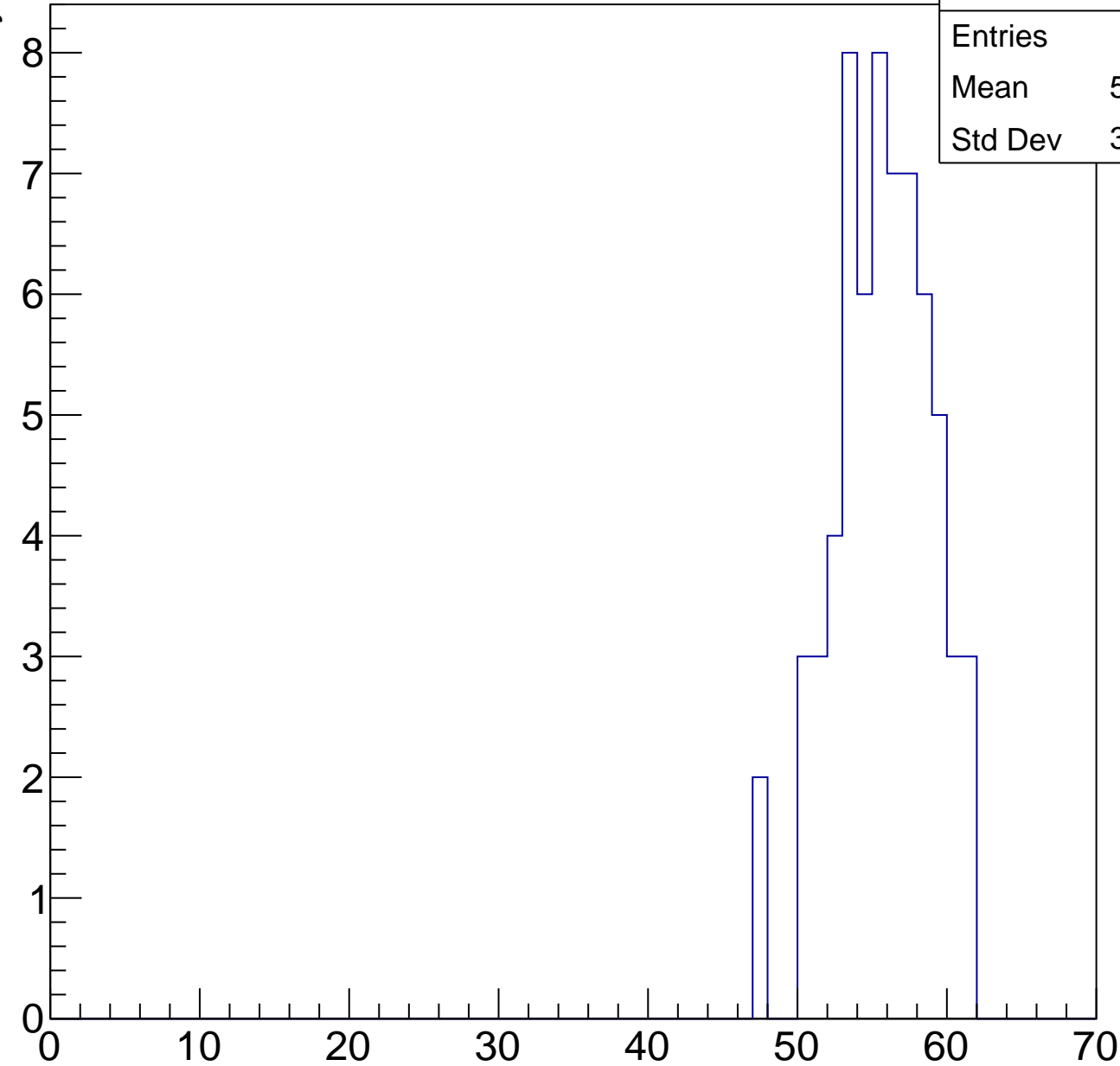
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	65
Mean	55.23
Std Dev	3.219

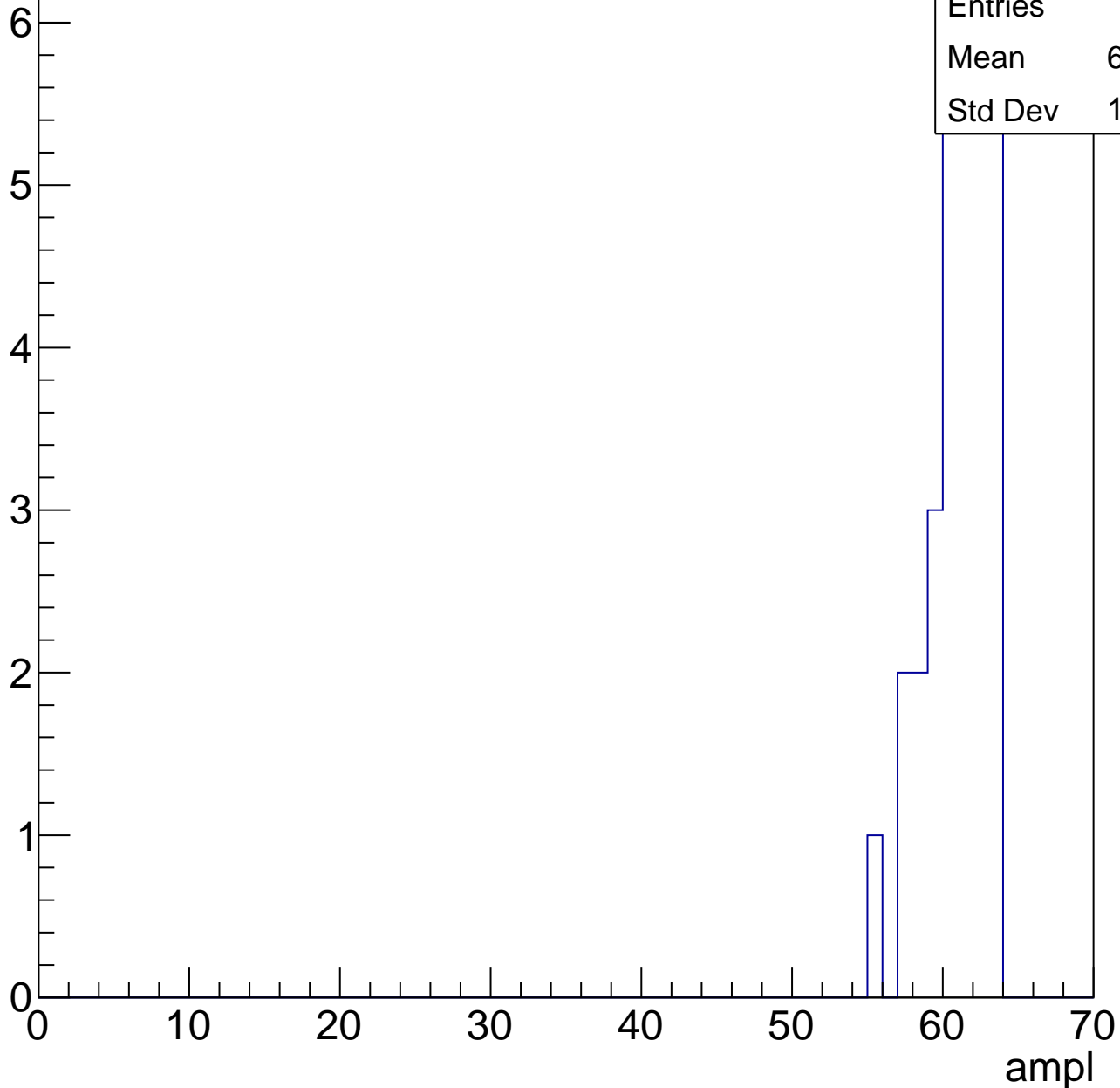
ampl



# B1L100S, U6-ch97, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

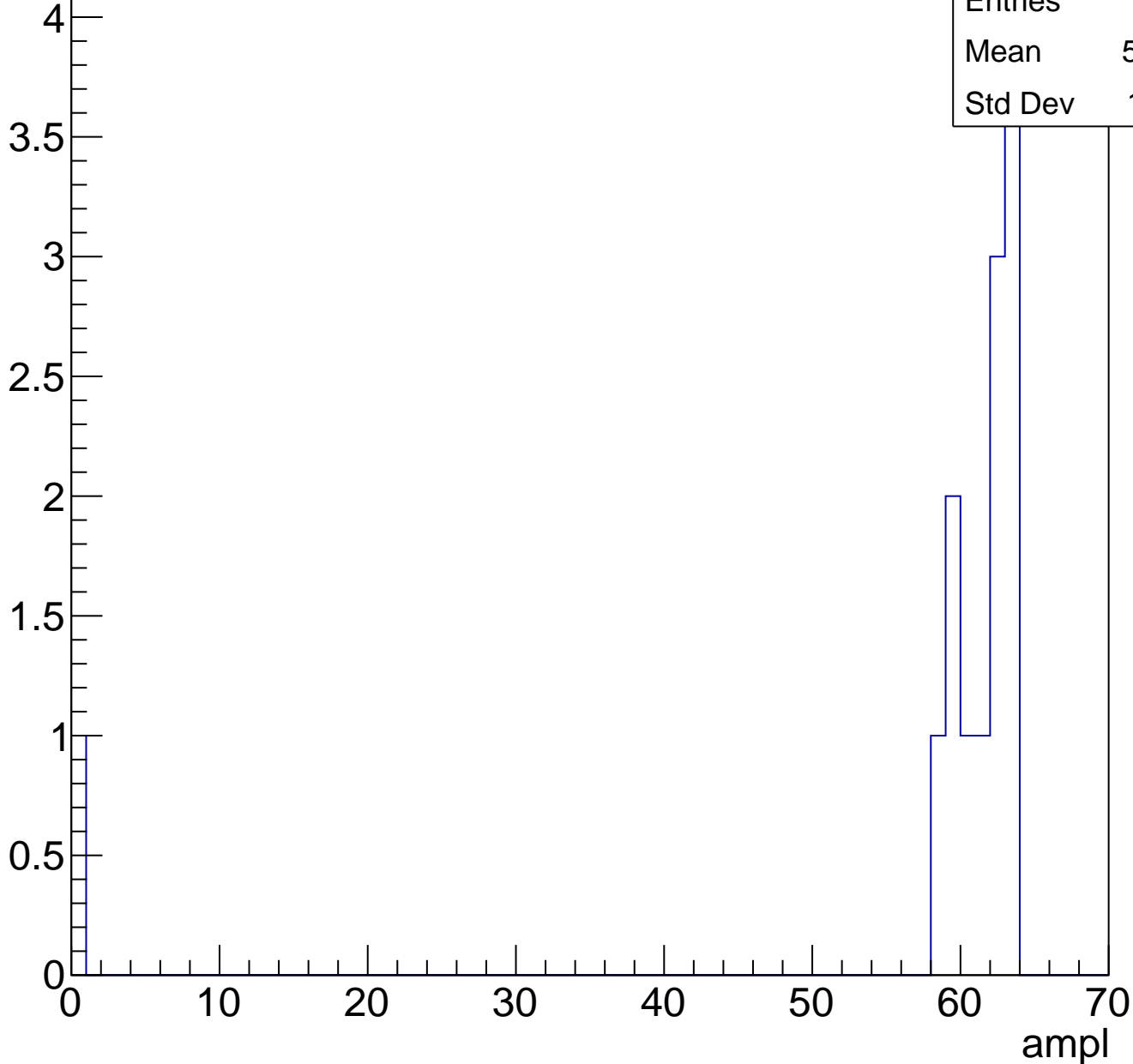
Entry



# B1L100S, U6-ch97, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

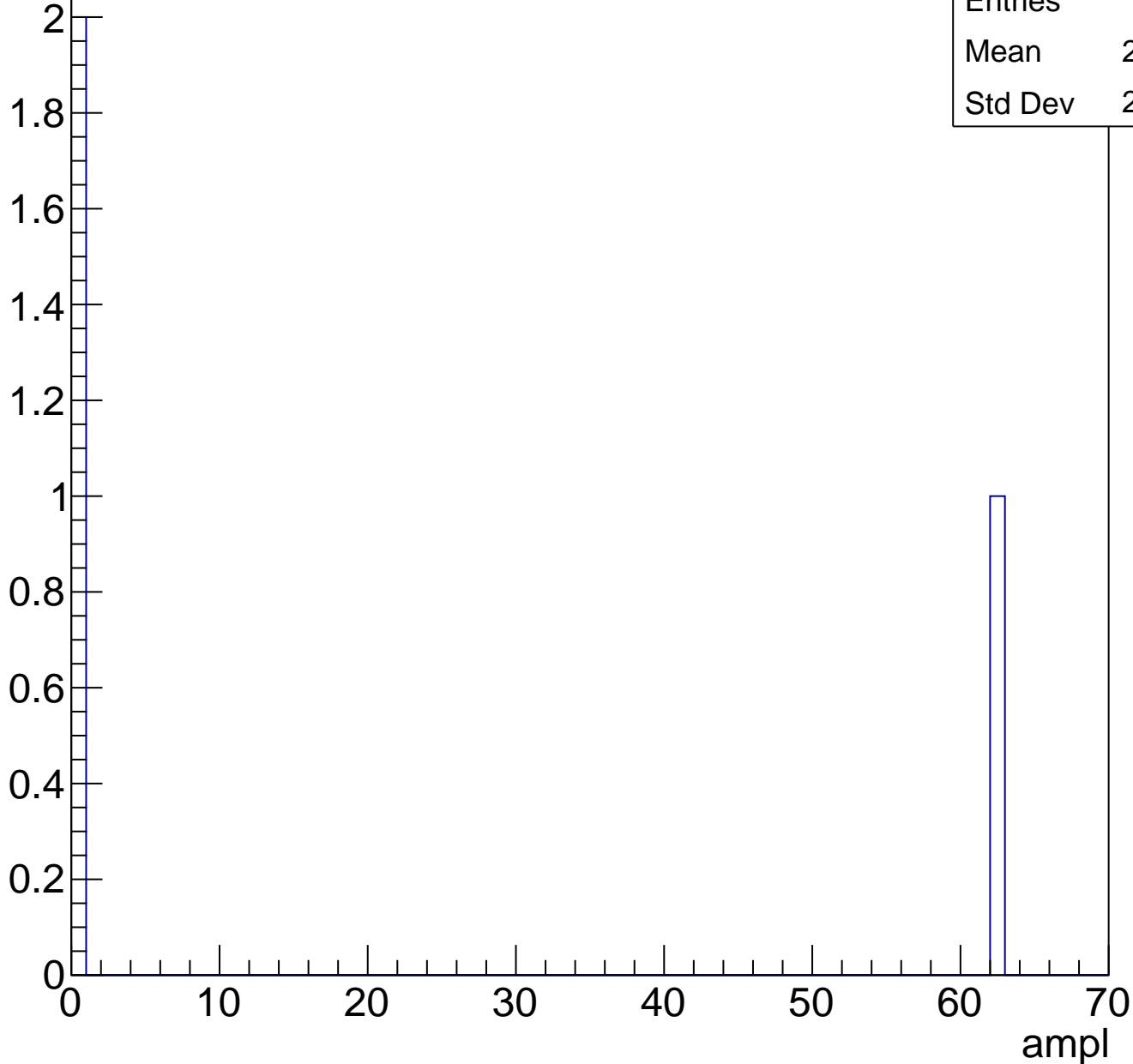




# B1L100S, U6-ch97, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



# B1L100S, U6-ch98, adc0

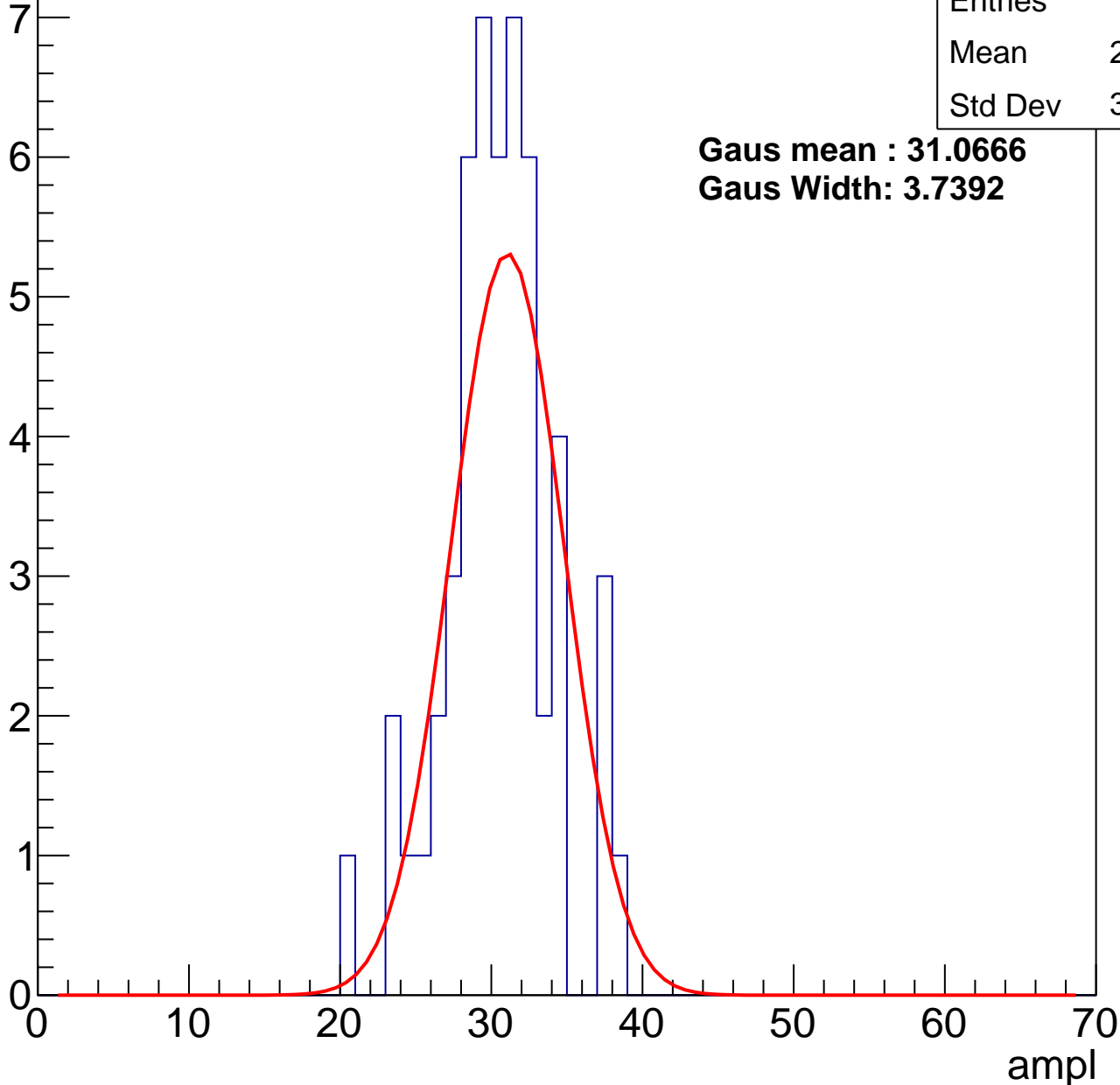
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	52
Mean	29.98
Std Dev	3.597

**Gaus mean : 31.0666**

**Gaus Width: 3.7392**



# B1L100S, U6-ch98, adc1

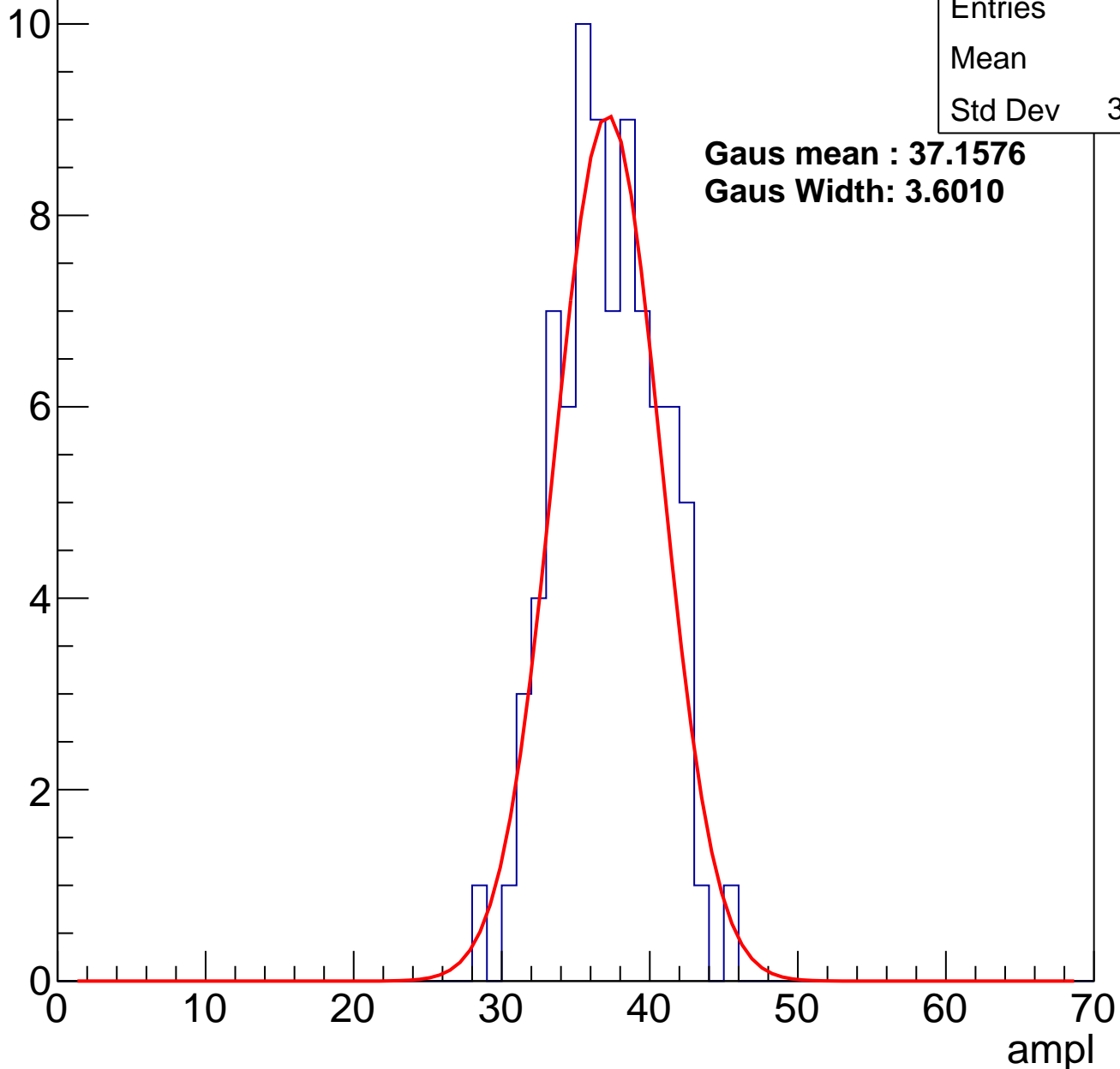
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	83
Mean	36.7
Std Dev	3.396

**Gaus mean : 37.1576**

**Gaus Width: 3.6010**

Entry



# B1L100S, U6-ch98, adc2

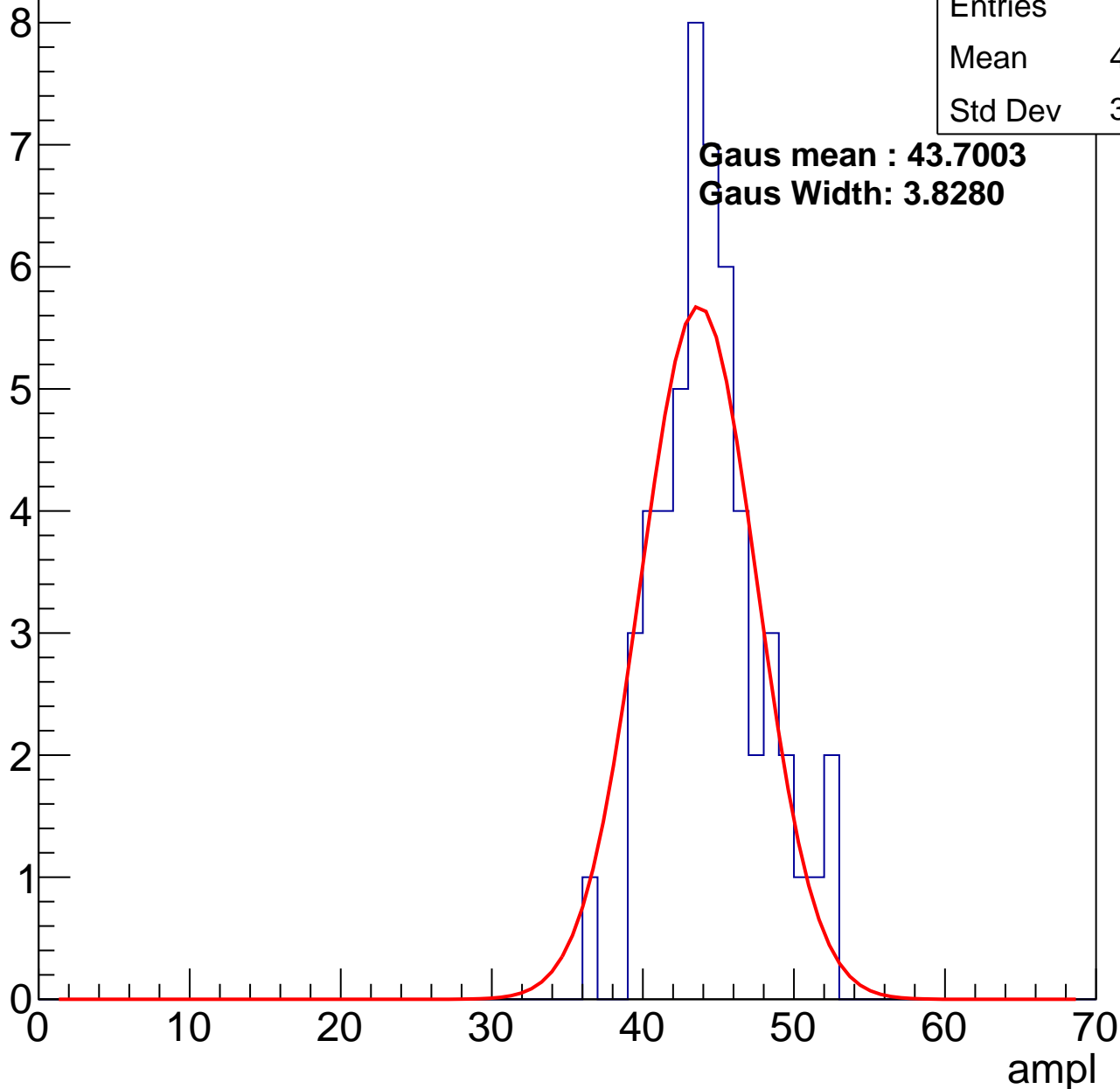
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	53
Mean	44.04
Std Dev	3.415

**Gaus mean : 43.7003**

**Gaus Width: 3.8280**

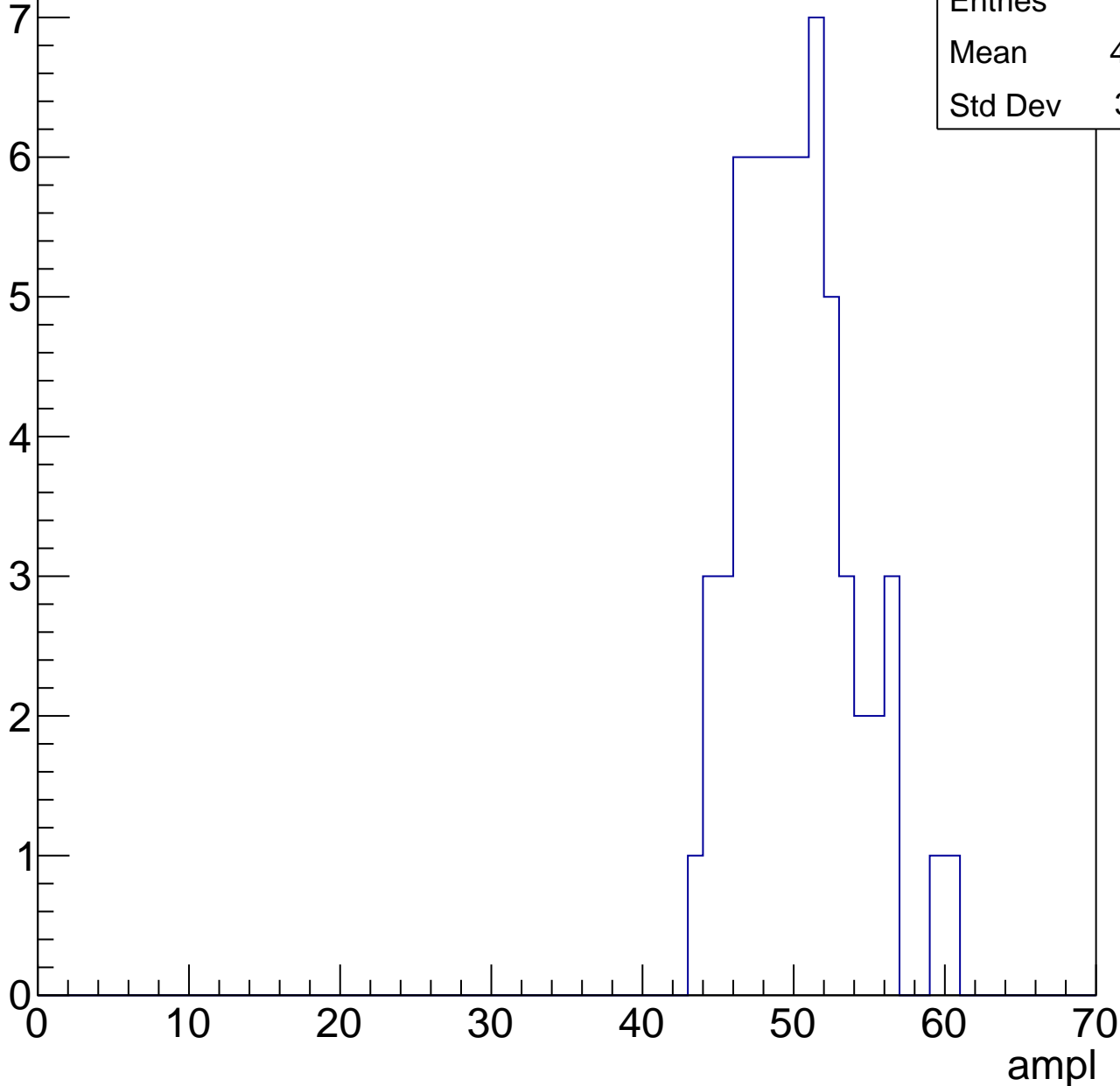


# B1L100S, U6-ch98, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	61
Mean	49.69
Std Dev	3.691

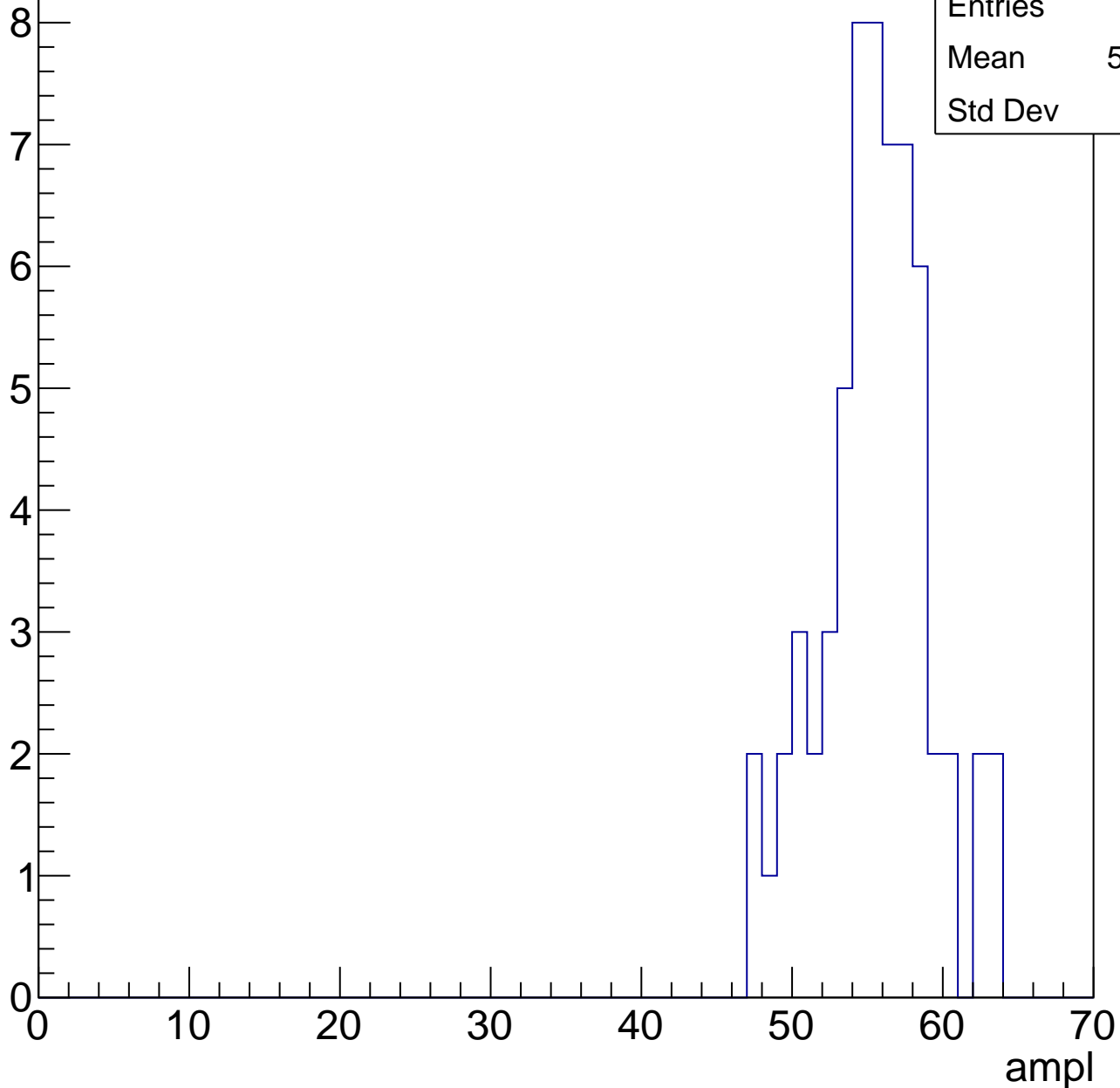


# B1L100S, U6-ch98, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	62
Mean	55.03
Std Dev	3.61

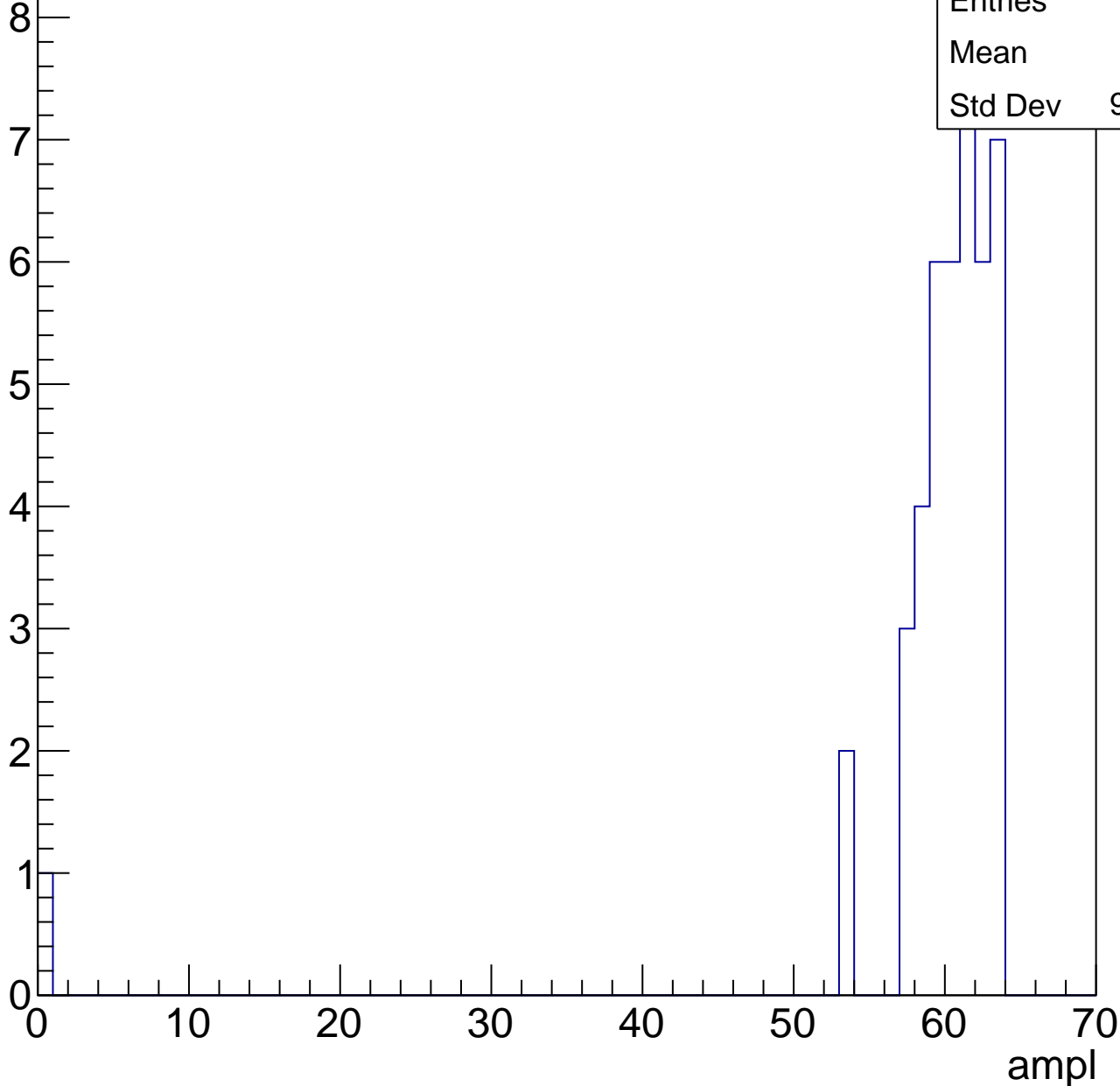


# B1L100S, U6-ch98, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	43
Mean	58.7
Std Dev	9.362



# B1L100S, U6-ch98, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

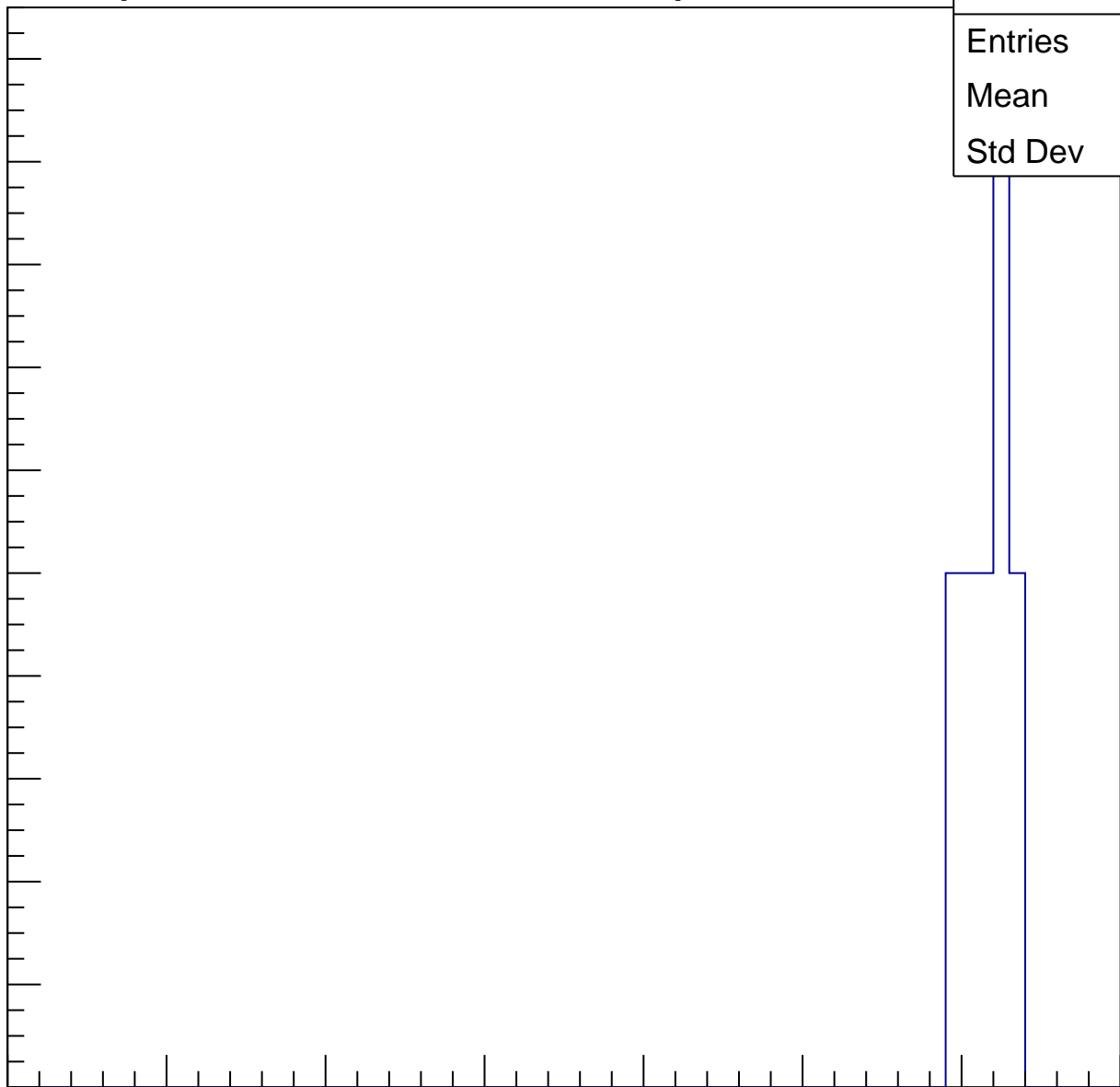
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	6
Mean	61.17
Std Dev	1.344

0 10 20 30 40 50 60 70

ampl





# B1L100S, U6-ch98, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



# B1L100S, U6-ch99, adc0

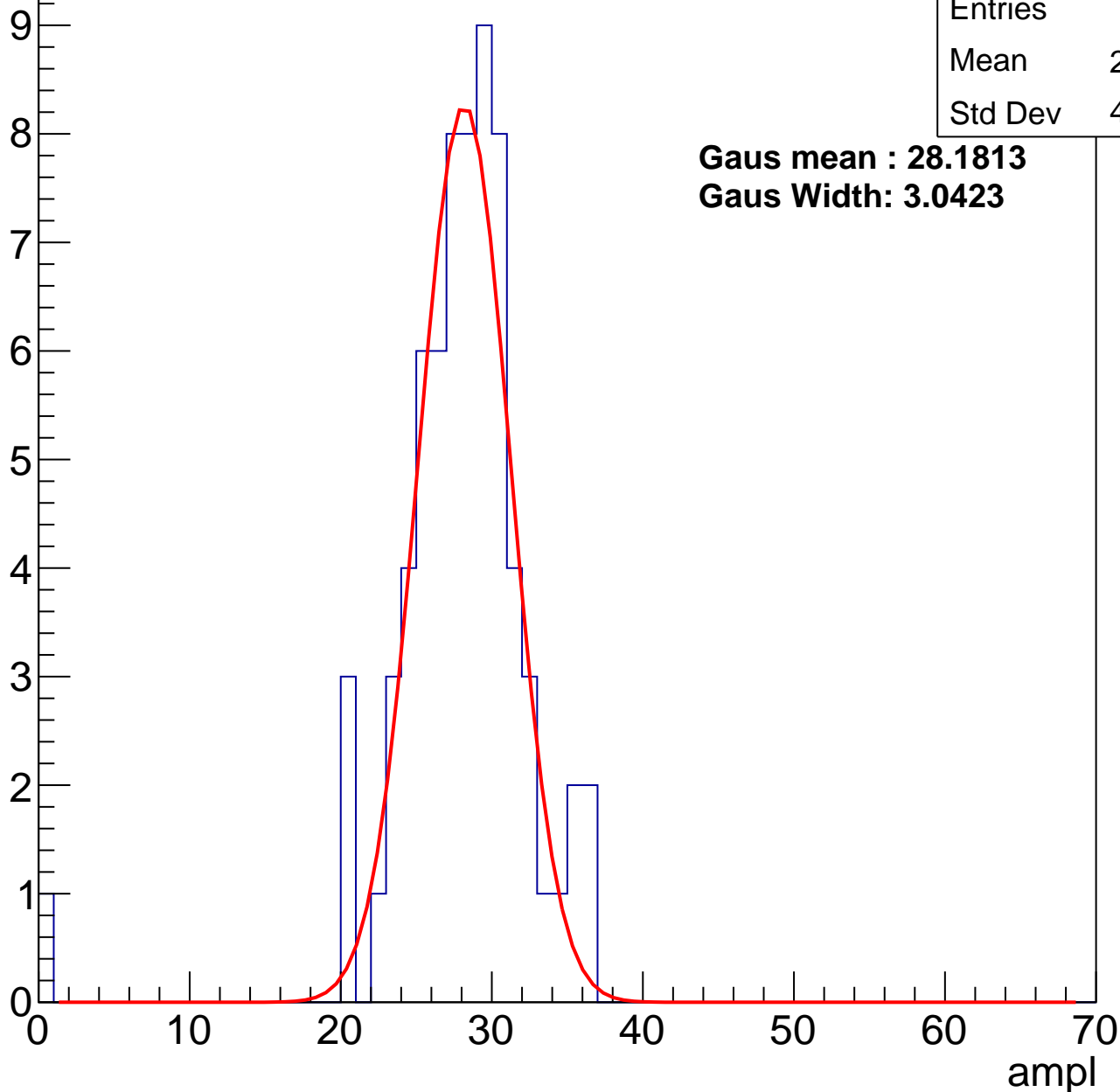
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	70
Mean	27.47
Std Dev	4.825

**Gaus mean : 28.1813**

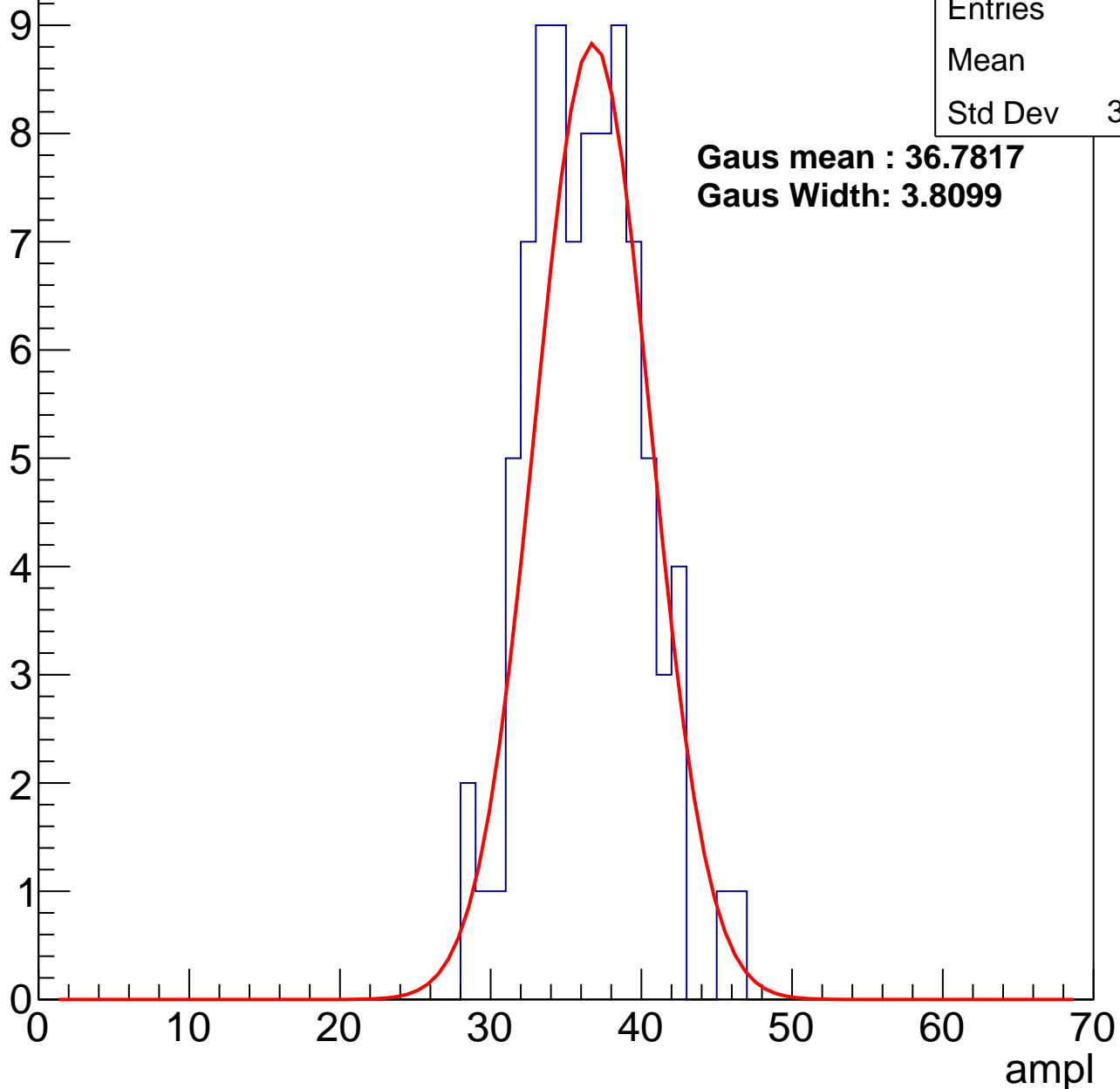
**Gaus Width: 3.0423**



# B1L100S, U6-ch99, adc1

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



# B1L100S, U6-ch99, adc2

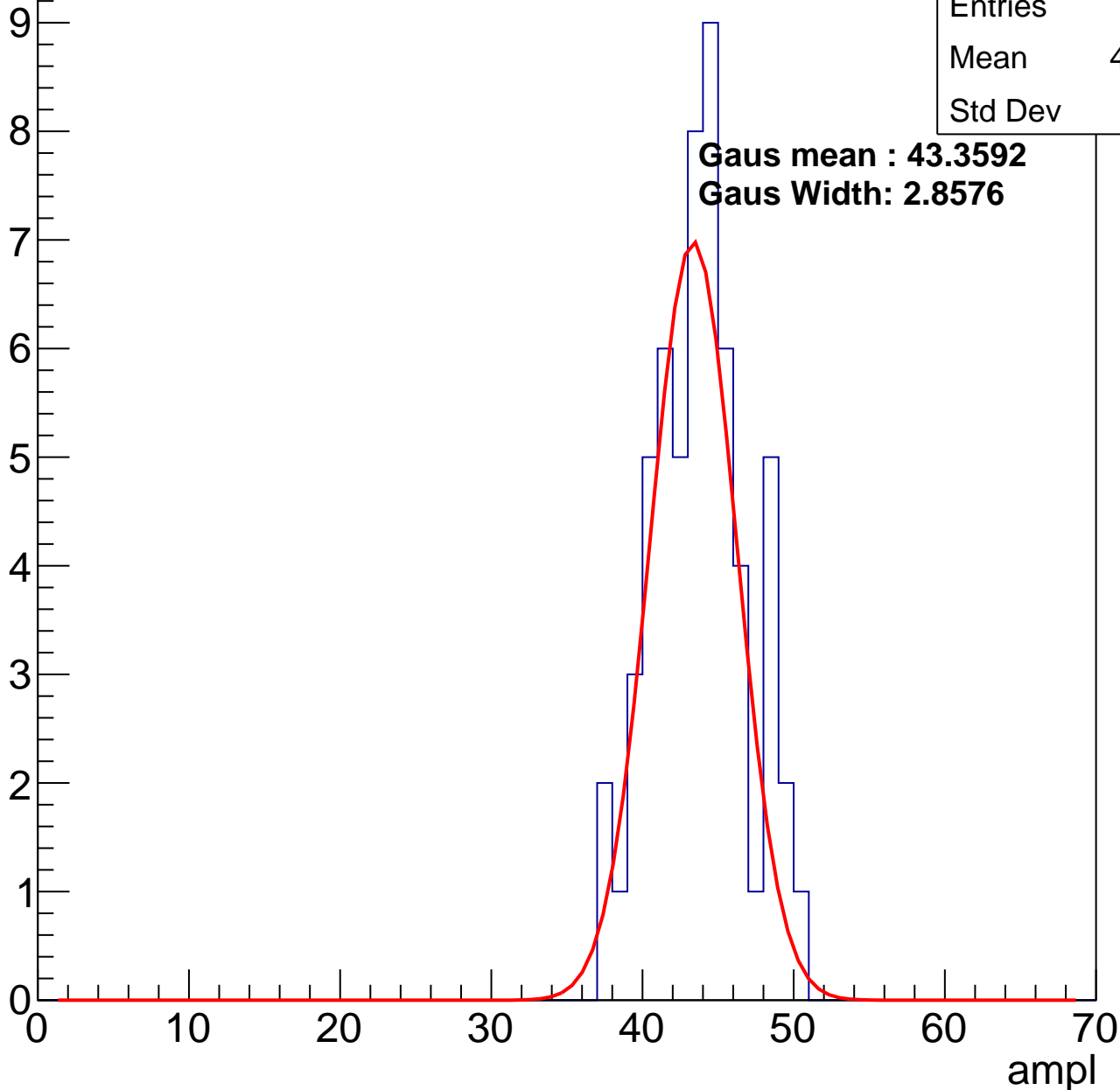
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	58
Mean	43.34
Std Dev	3.06

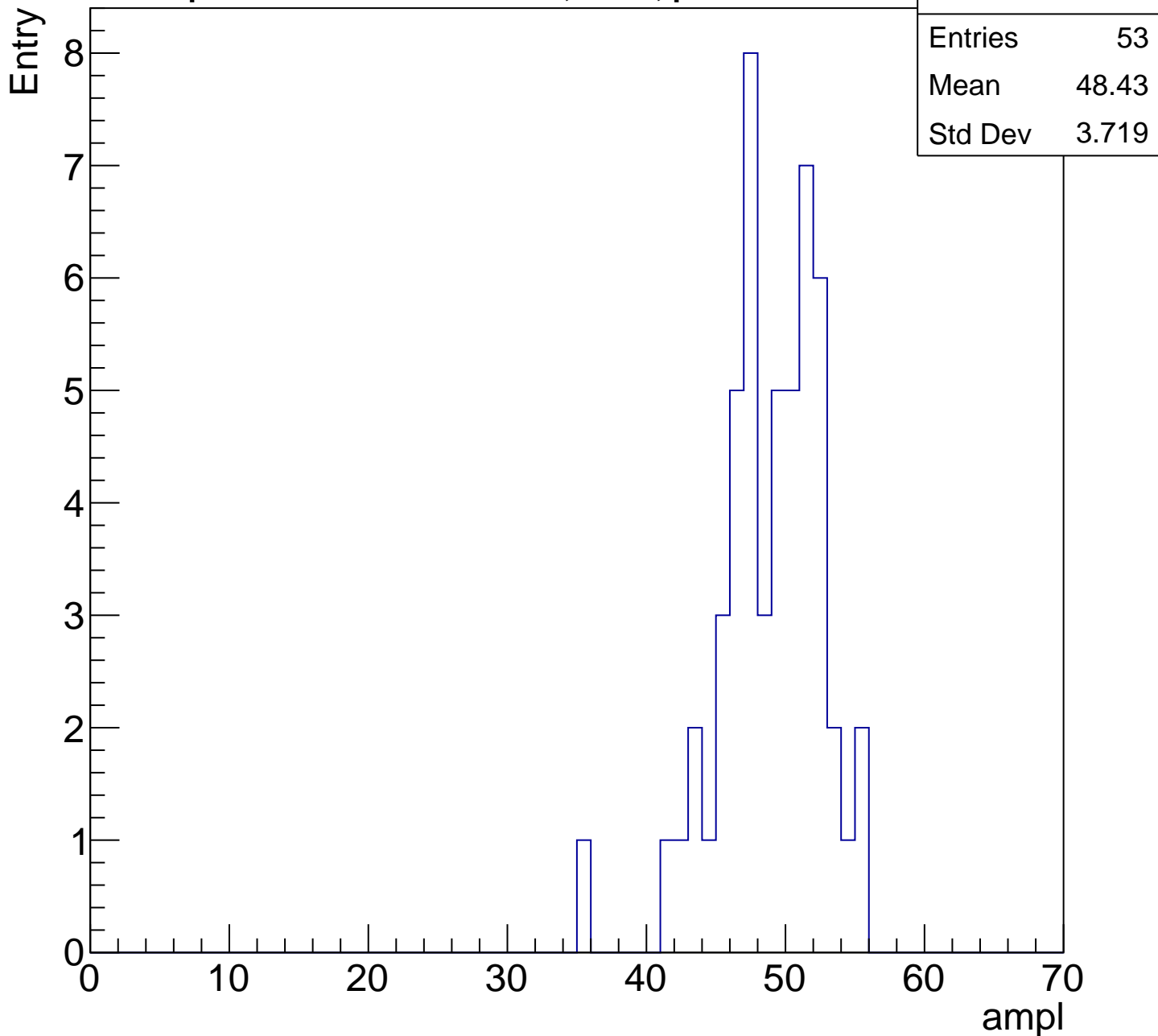
**Gaus mean : 43.3592**

**Gaus Width: 2.8576**



# B1L100S, U6-ch99, adc3

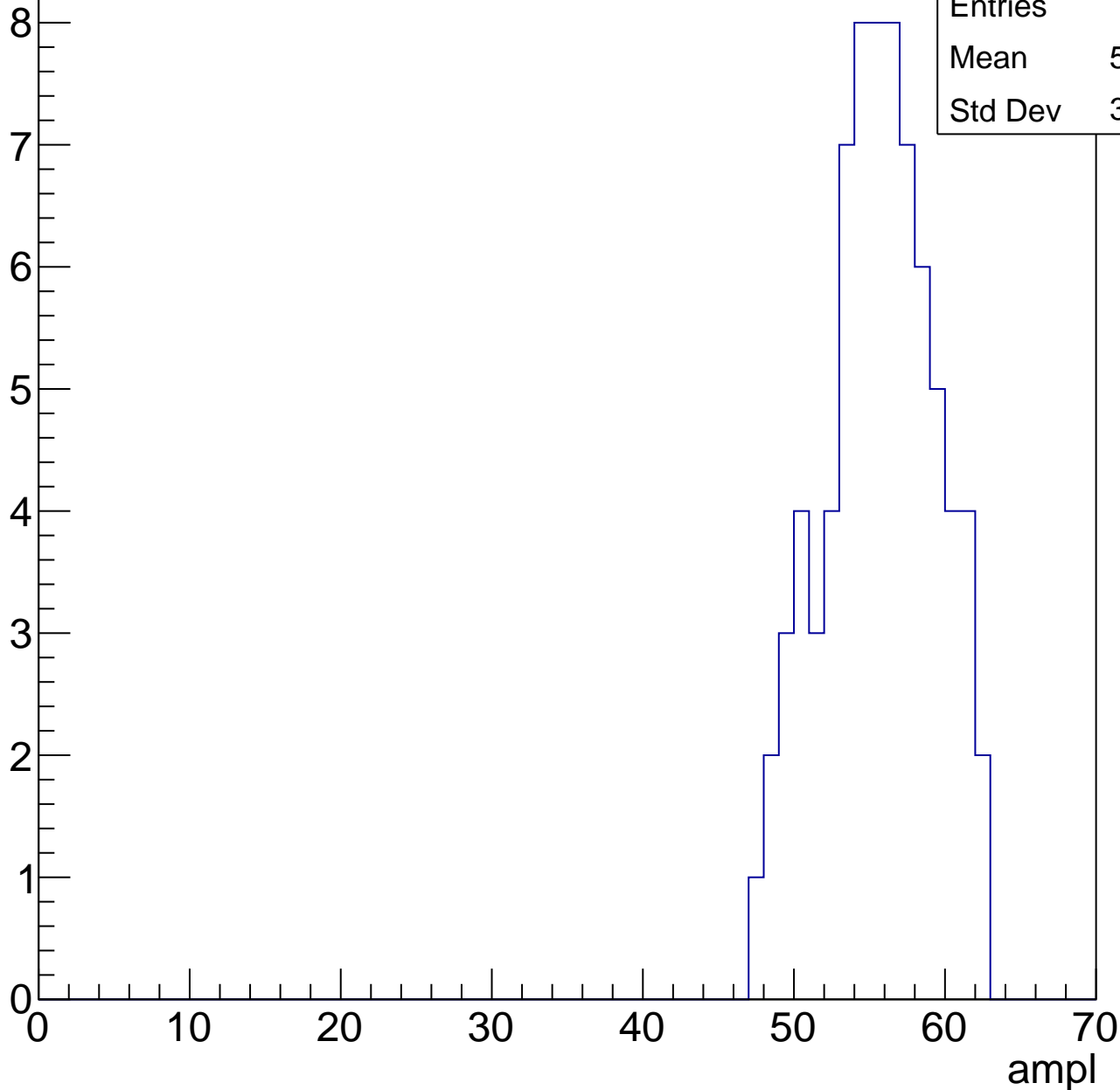
calib\_packv5\_042523\_0143.root, FC#4, port A2



# B1L100S, U6-ch99, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

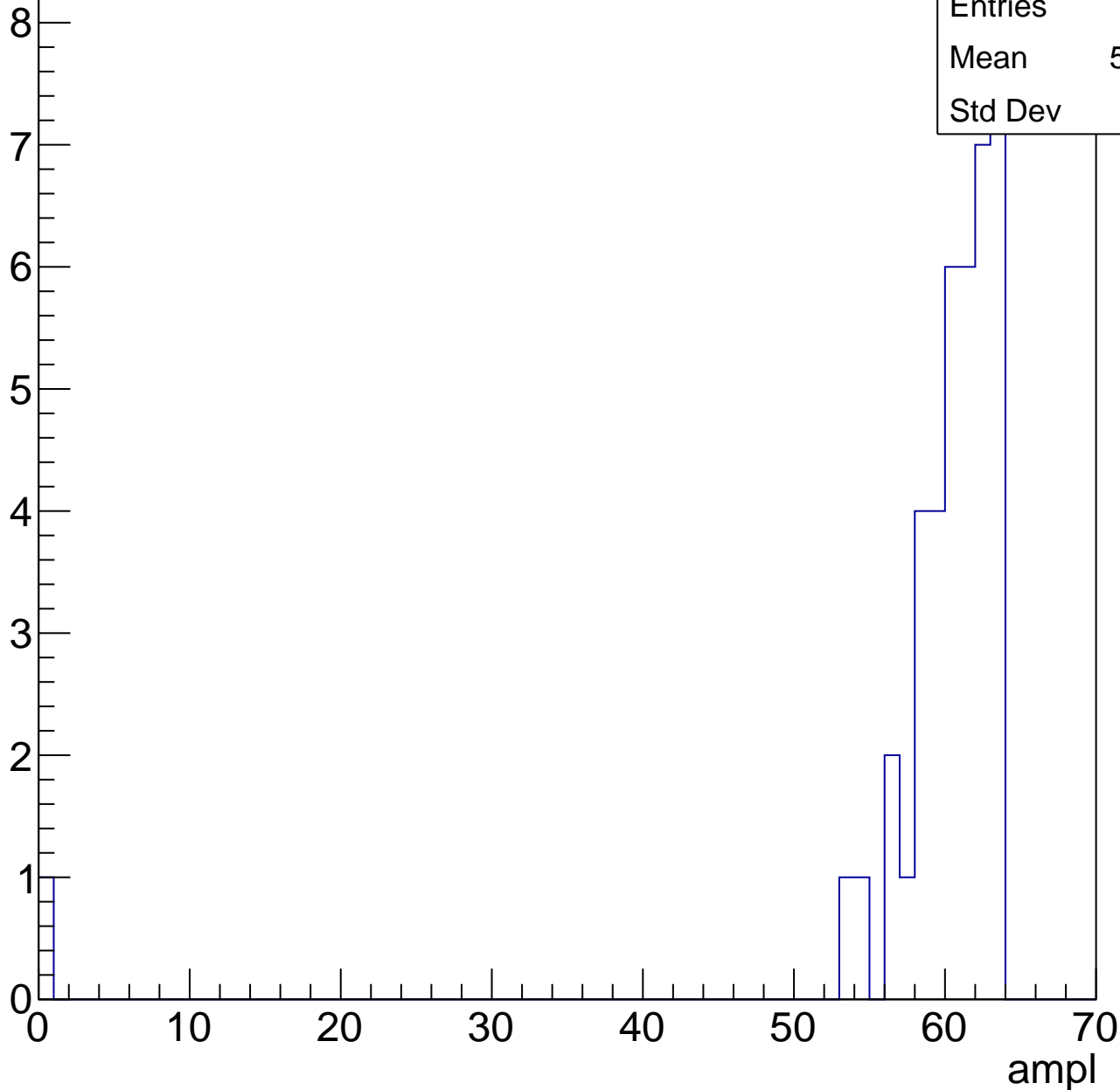


# B1L100S, U6-ch99, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	41
Mean	58.73
Std Dev	9.61



# B1L100S, U6-ch99, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	6
Mean	60.17
Std Dev	2.609

ampl

0 10 20 30 40 50 60 70



# B1L100S, U6-ch99, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L100S, U6-ch100, adc0

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	73
Mean	30.6
Std Dev	3.122

**Gaus mean : 30.7190**

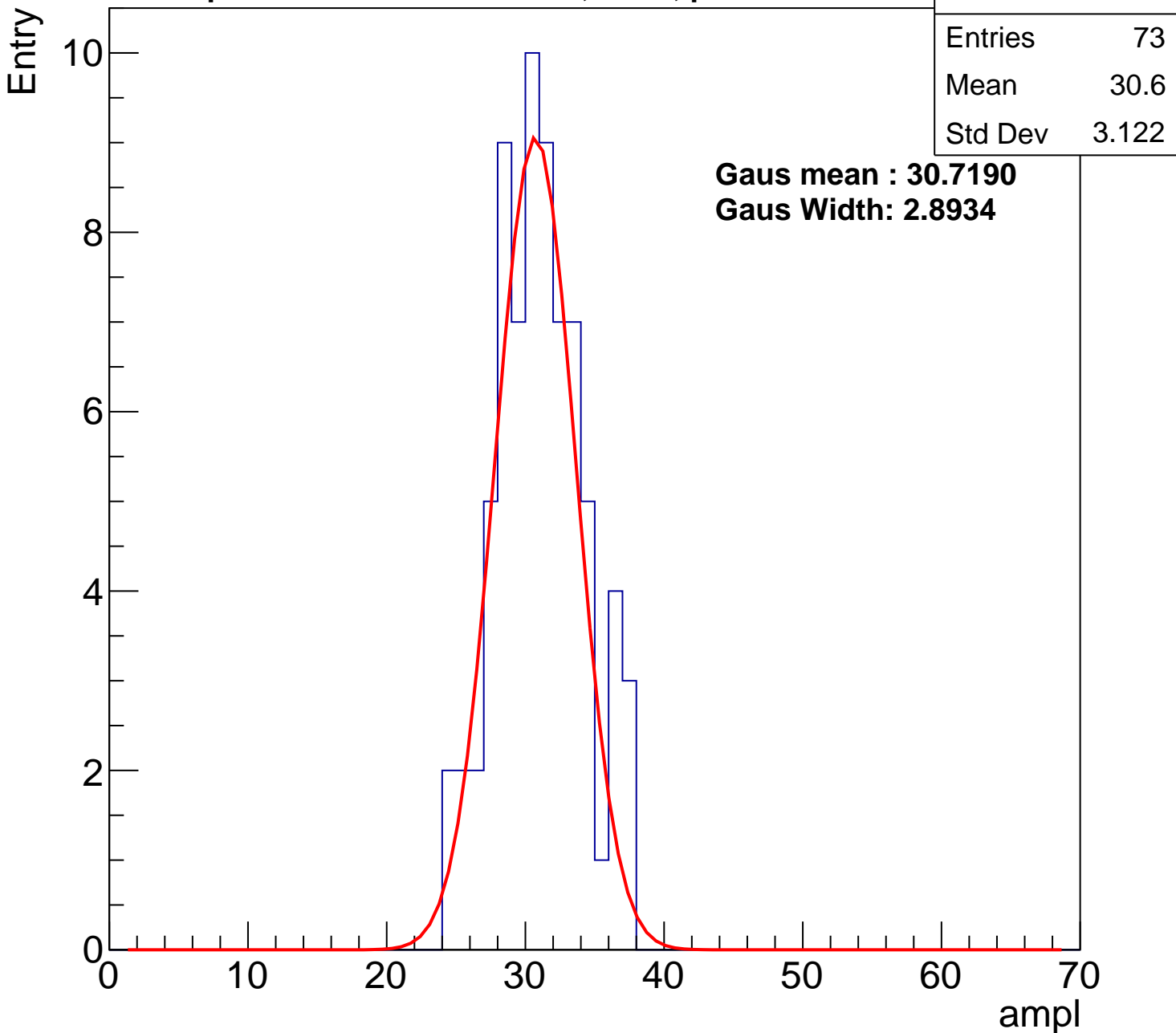
**Gaus Width: 2.8934**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L100S, U6-ch100, adc1

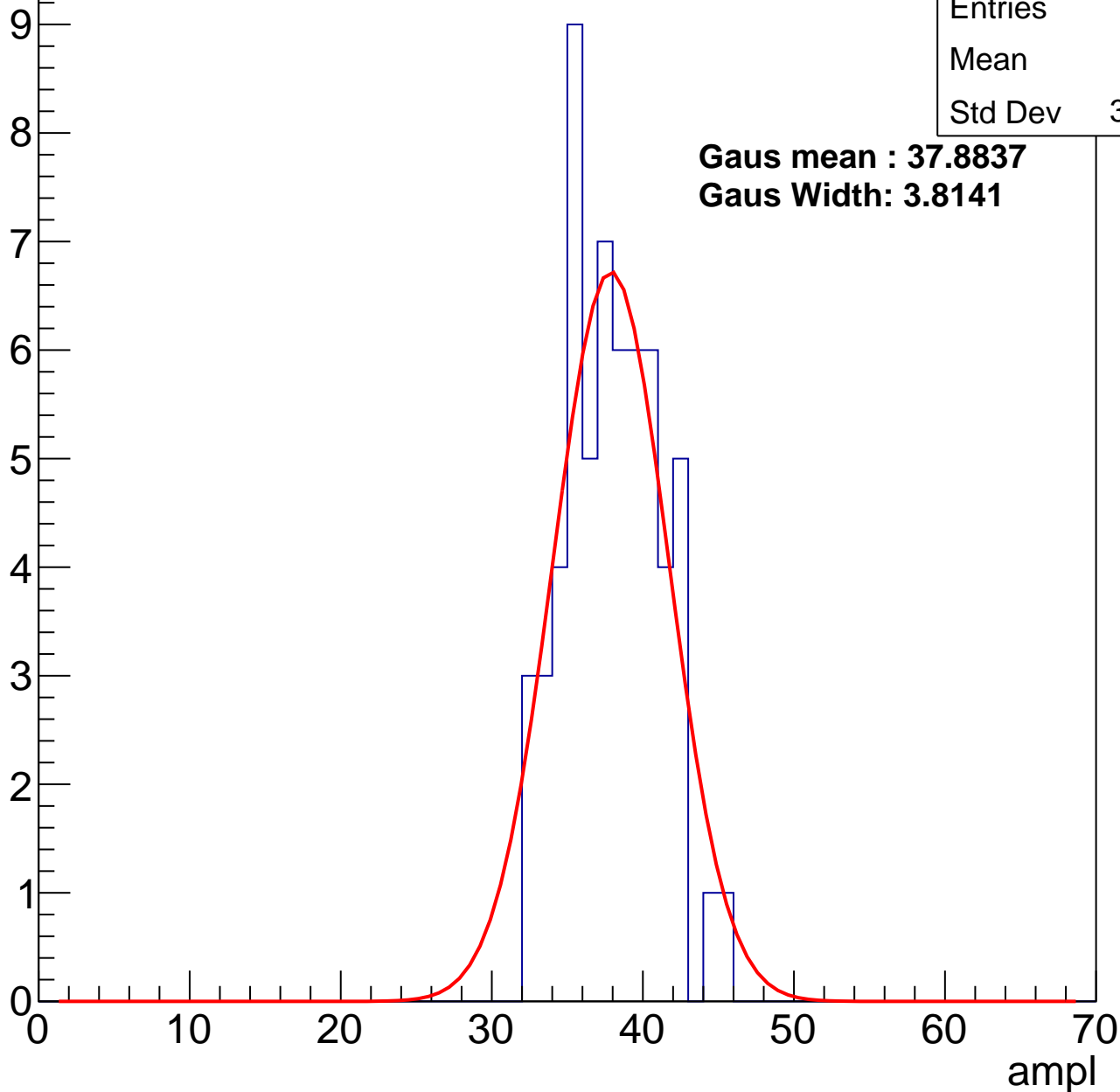
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	60
Mean	37.5
Std Dev	3.085

**Gaus mean : 37.8837**

**Gaus Width: 3.8141**



# B1L100S, U6-ch100, adc2

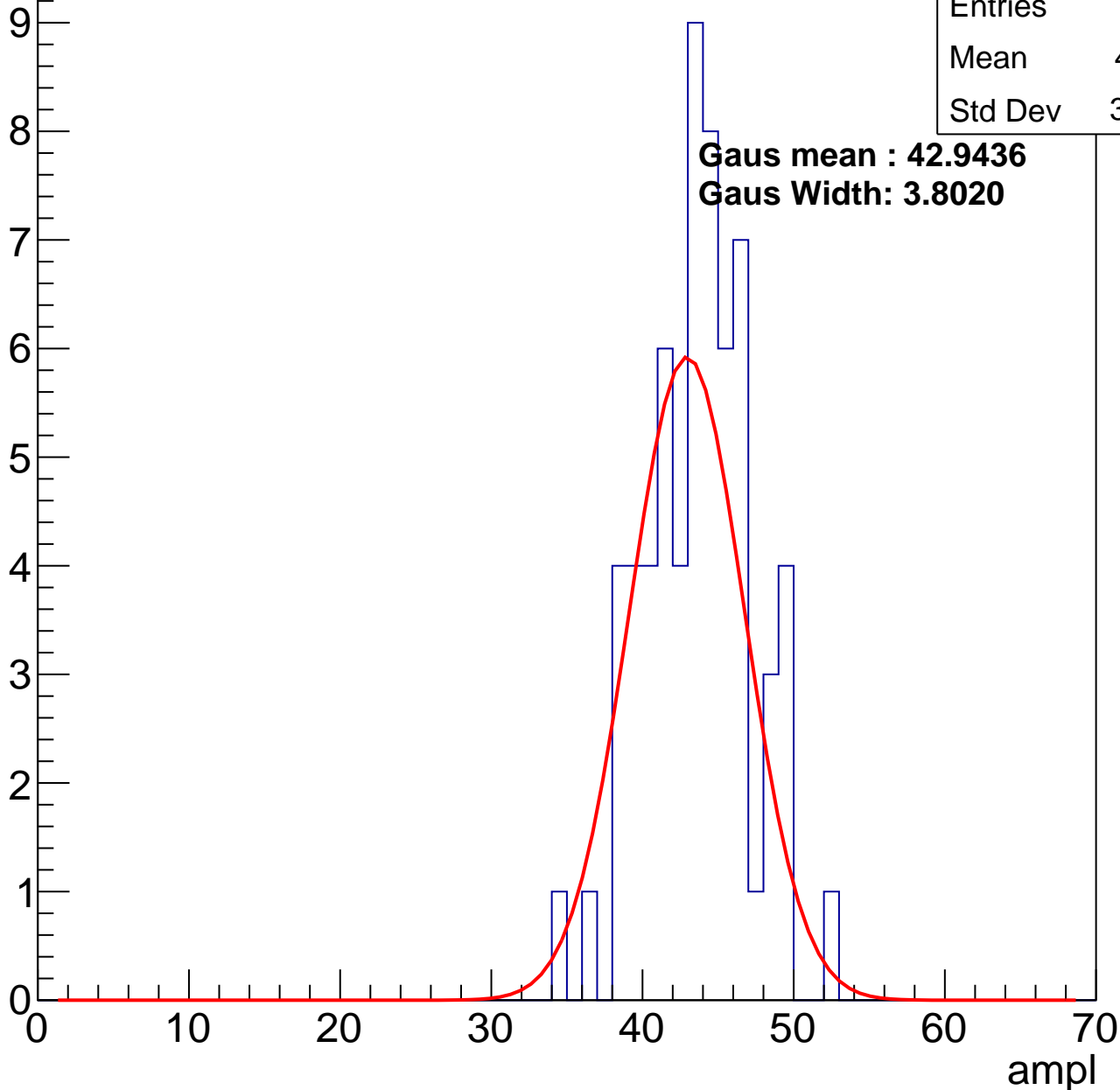
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	63
Mean	43.21
Std Dev	3.488

**Gaus mean : 42.9436**

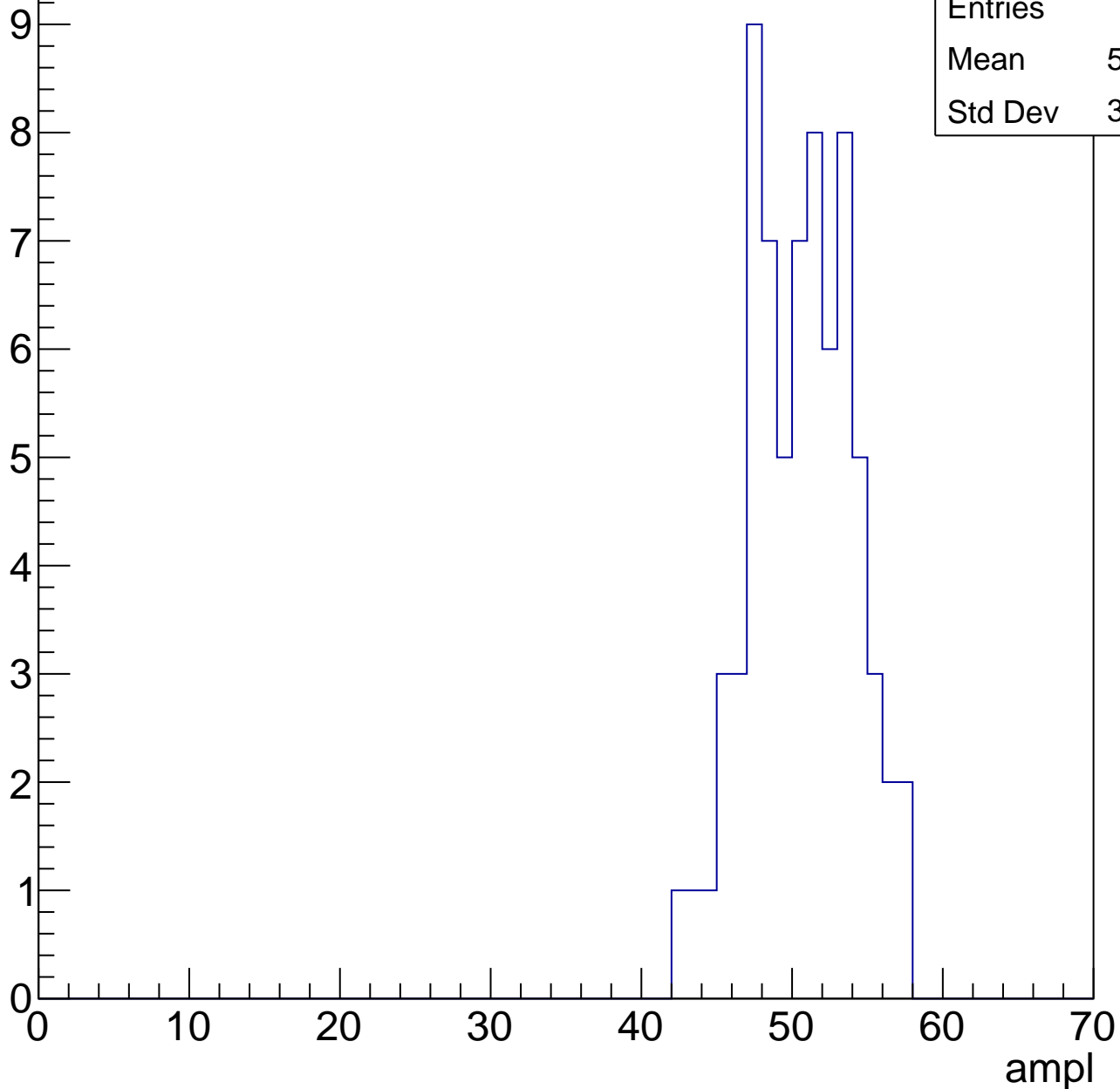
**Gaus Width: 3.8020**



# B1L100S, U6-ch100, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

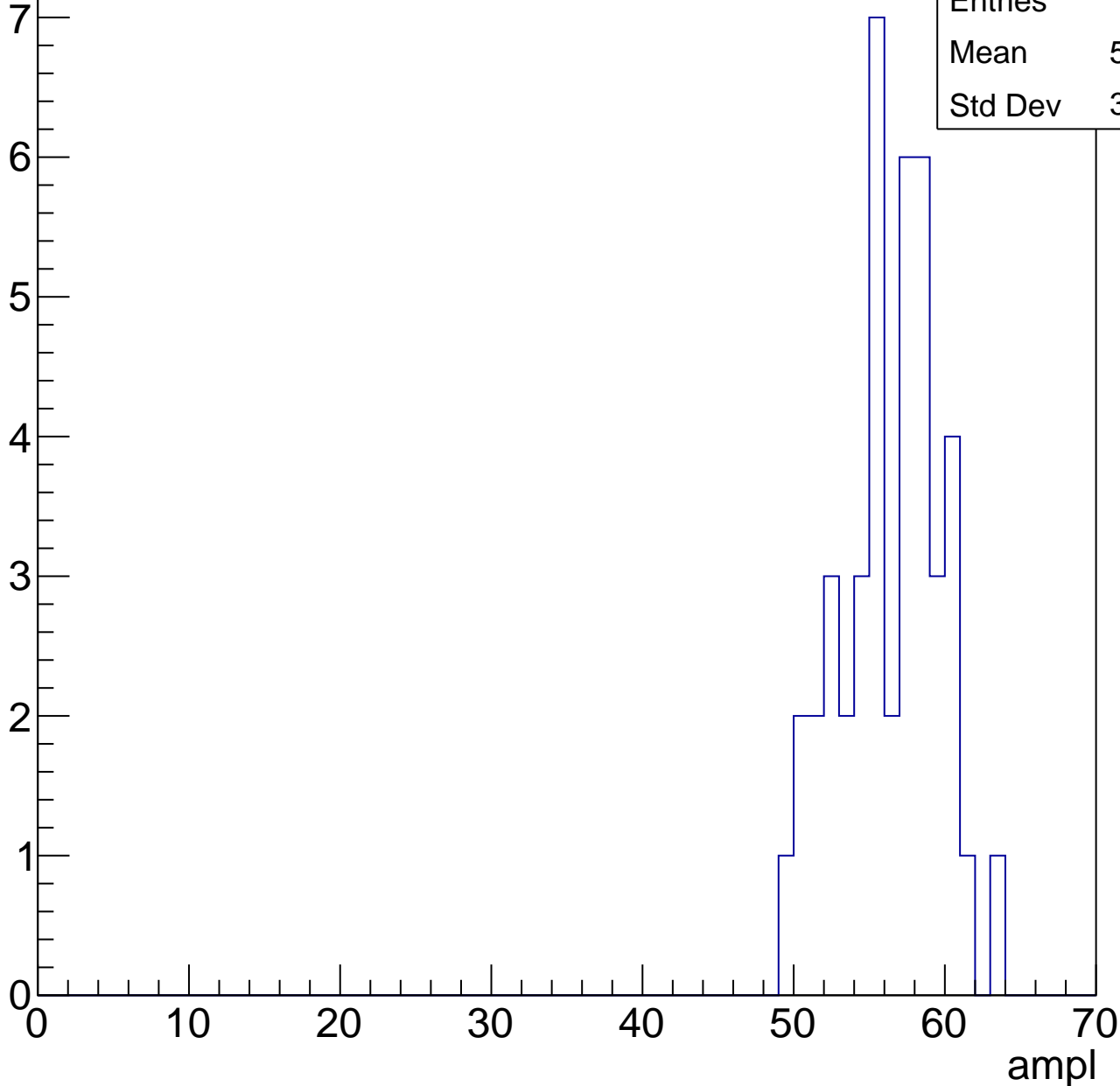


# B1L100S, U6-ch100, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	43
Mean	55.88
Std Dev	3.236

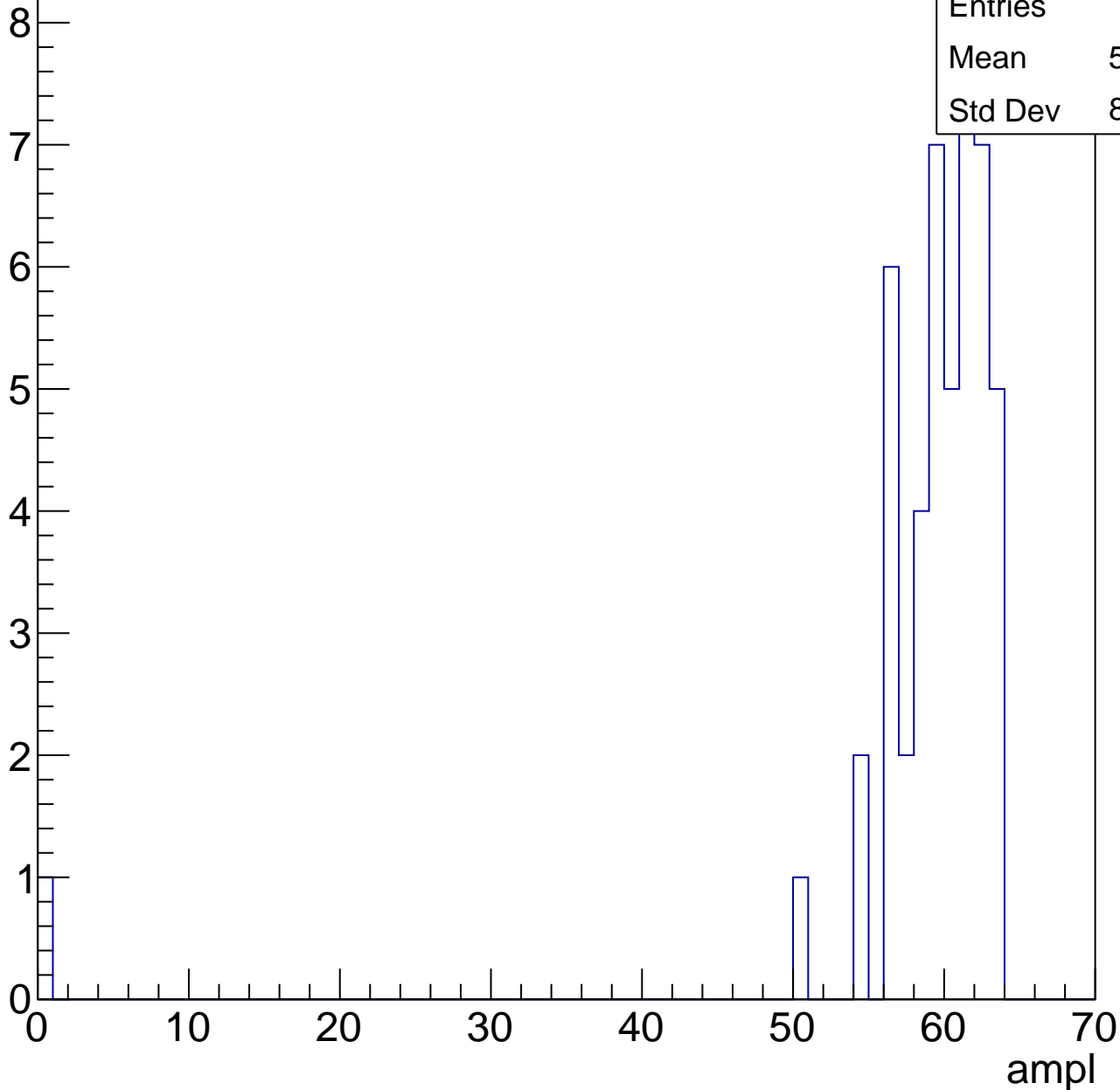


# B1L100S, U6-ch100, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	48
Mean	58.12
Std Dev	8.922



# B1L100S, U6-ch100, adc6

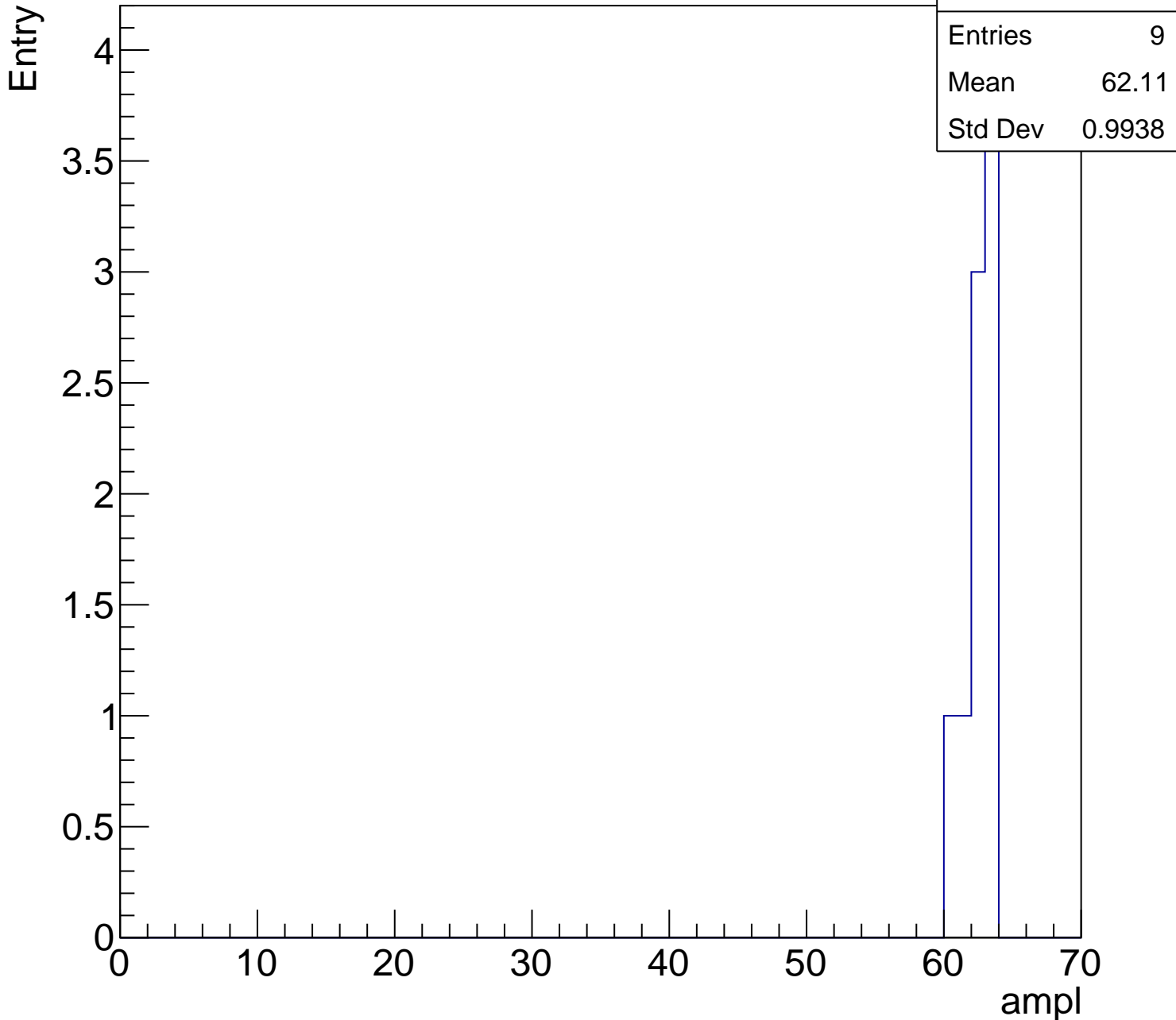
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

4  
3.5  
3  
2.5  
2  
1.5  
1  
0.5  
0

Entries	9
Mean	62.11
Std Dev	0.9938

ampl





# B1L100S, U6-ch100, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



# B1L100S, U6-ch101, adc0

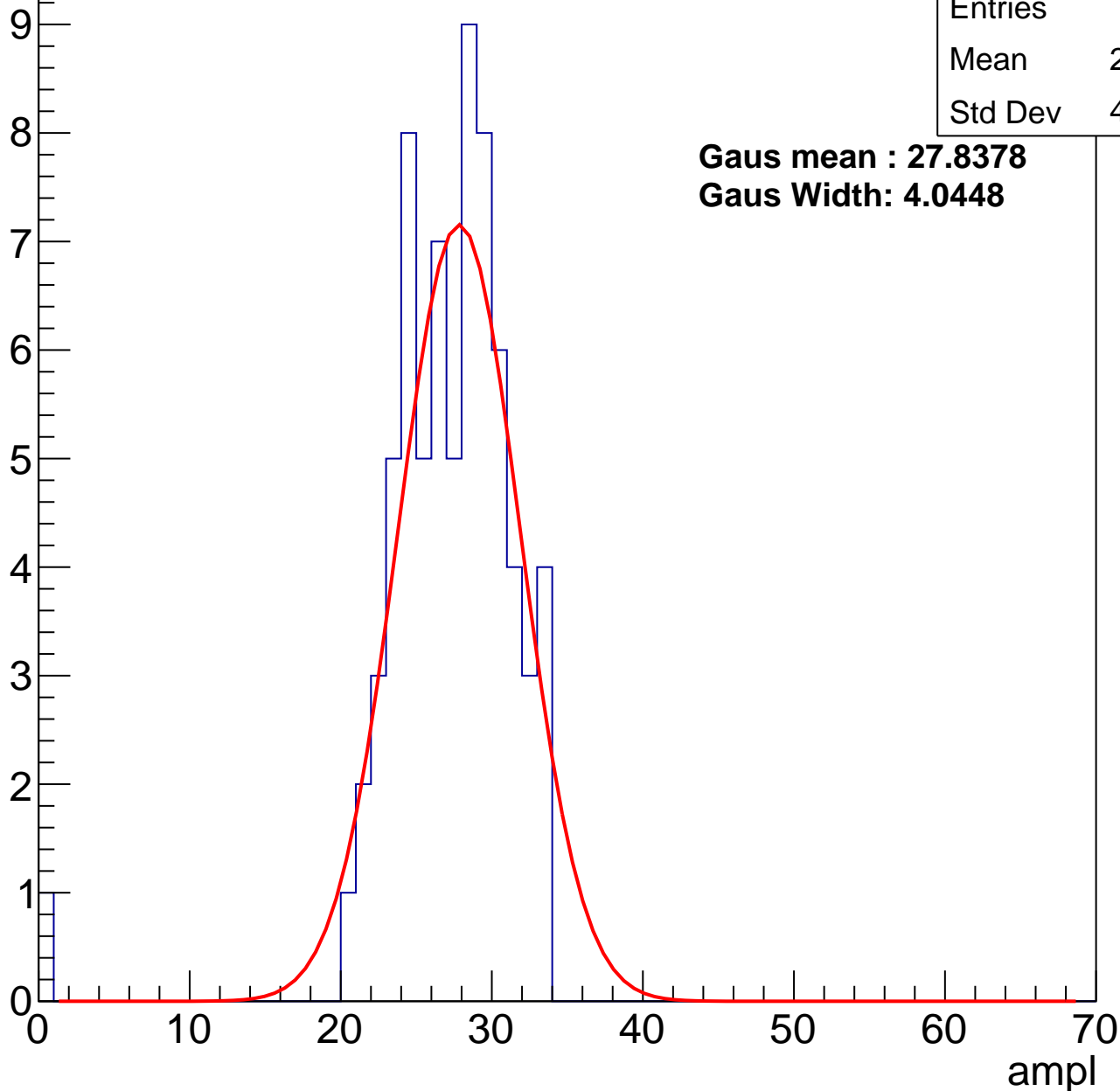
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	71
Mean	26.66
Std Dev	4.556

**Gaus mean : 27.8378**

**Gaus Width: 4.0448**



# B1L100S, U6-ch101, adc1

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	75
Mean	34.2
Std Dev	3.567

**Gaus mean : 34.9510**

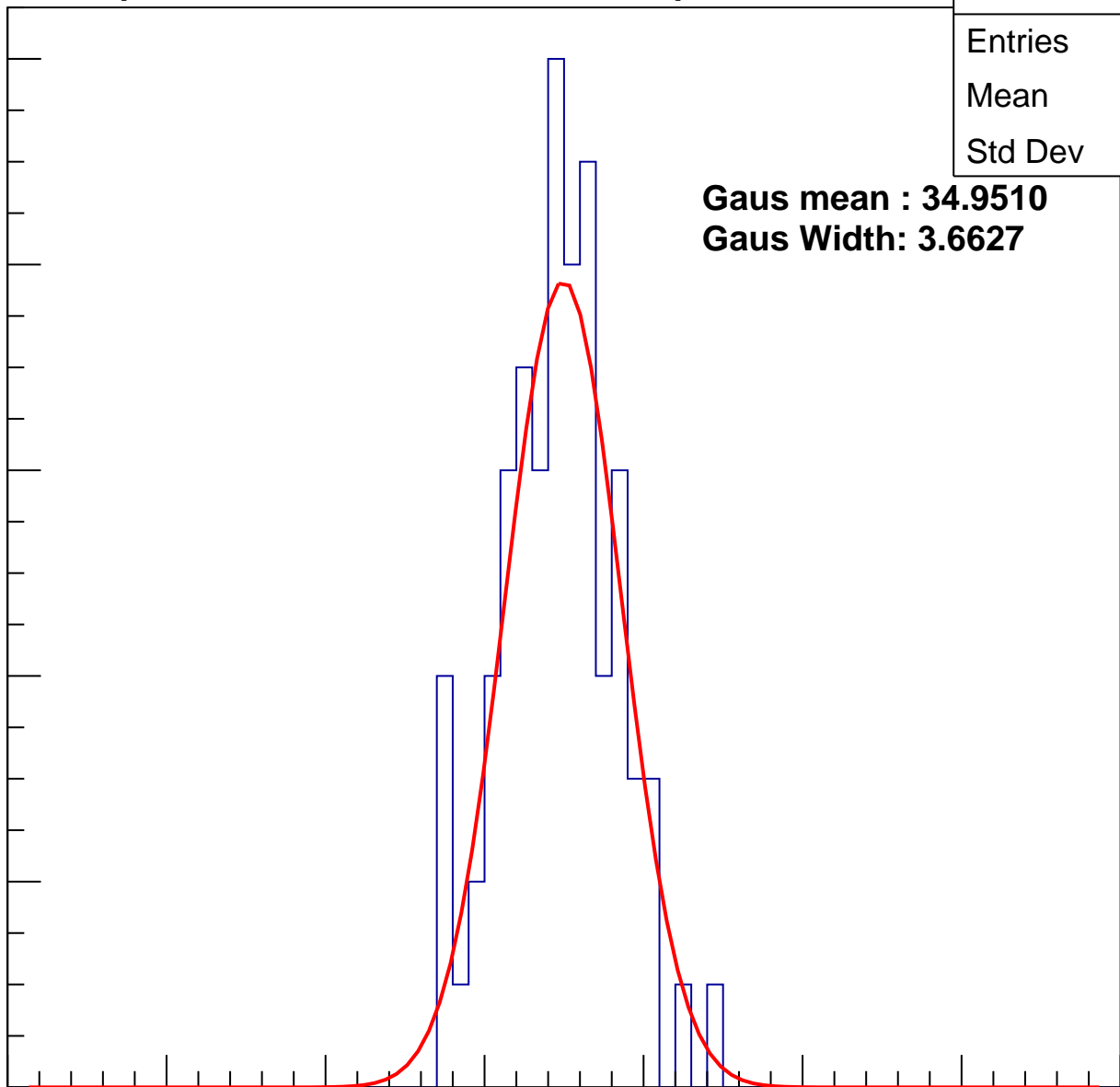
**Gaus Width: 3.6627**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L100S, U6-ch101, adc2

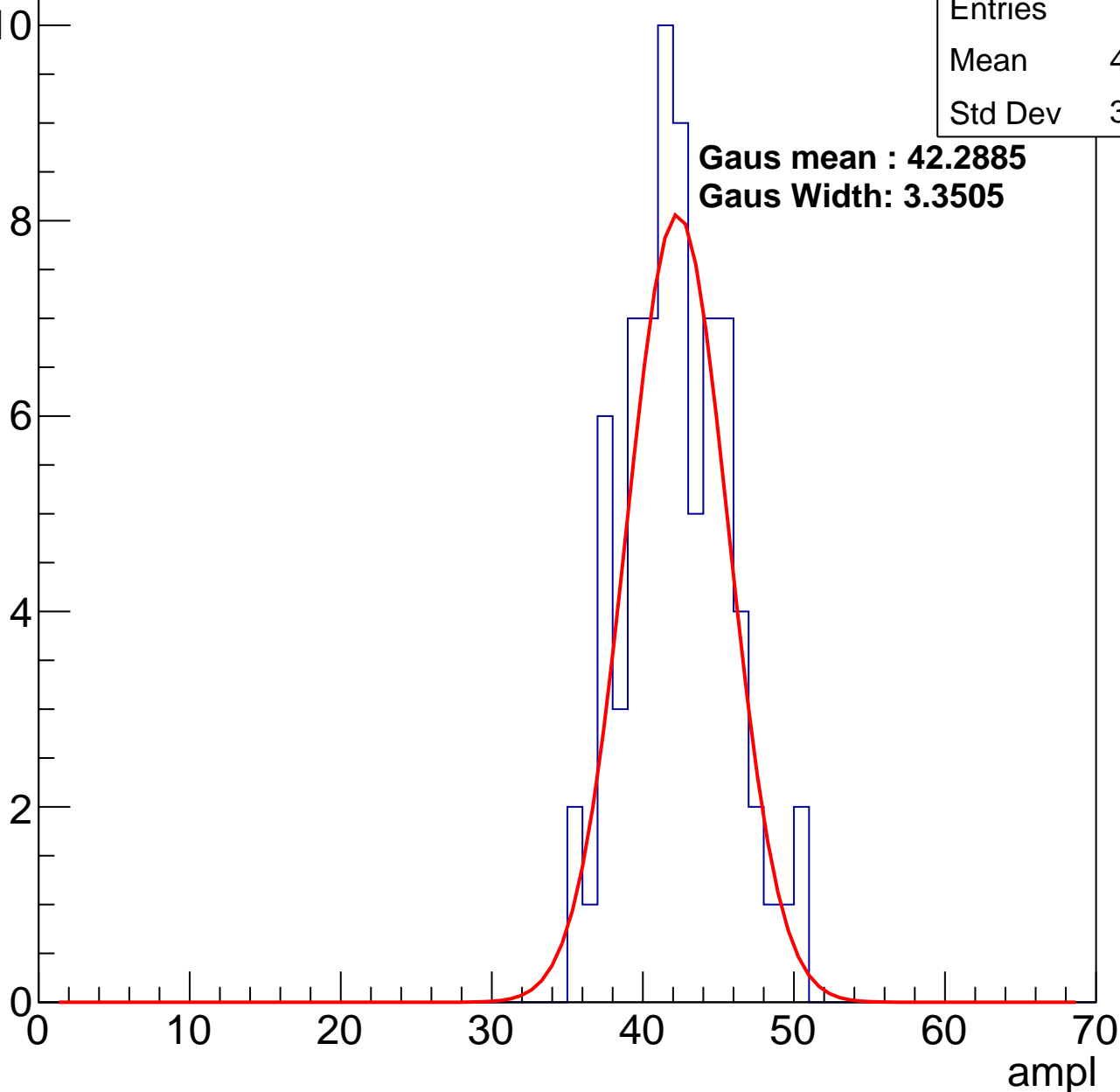
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	74
Mean	41.84
Std Dev	3.397

**Gaus mean : 42.2885**

**Gaus Width: 3.3505**

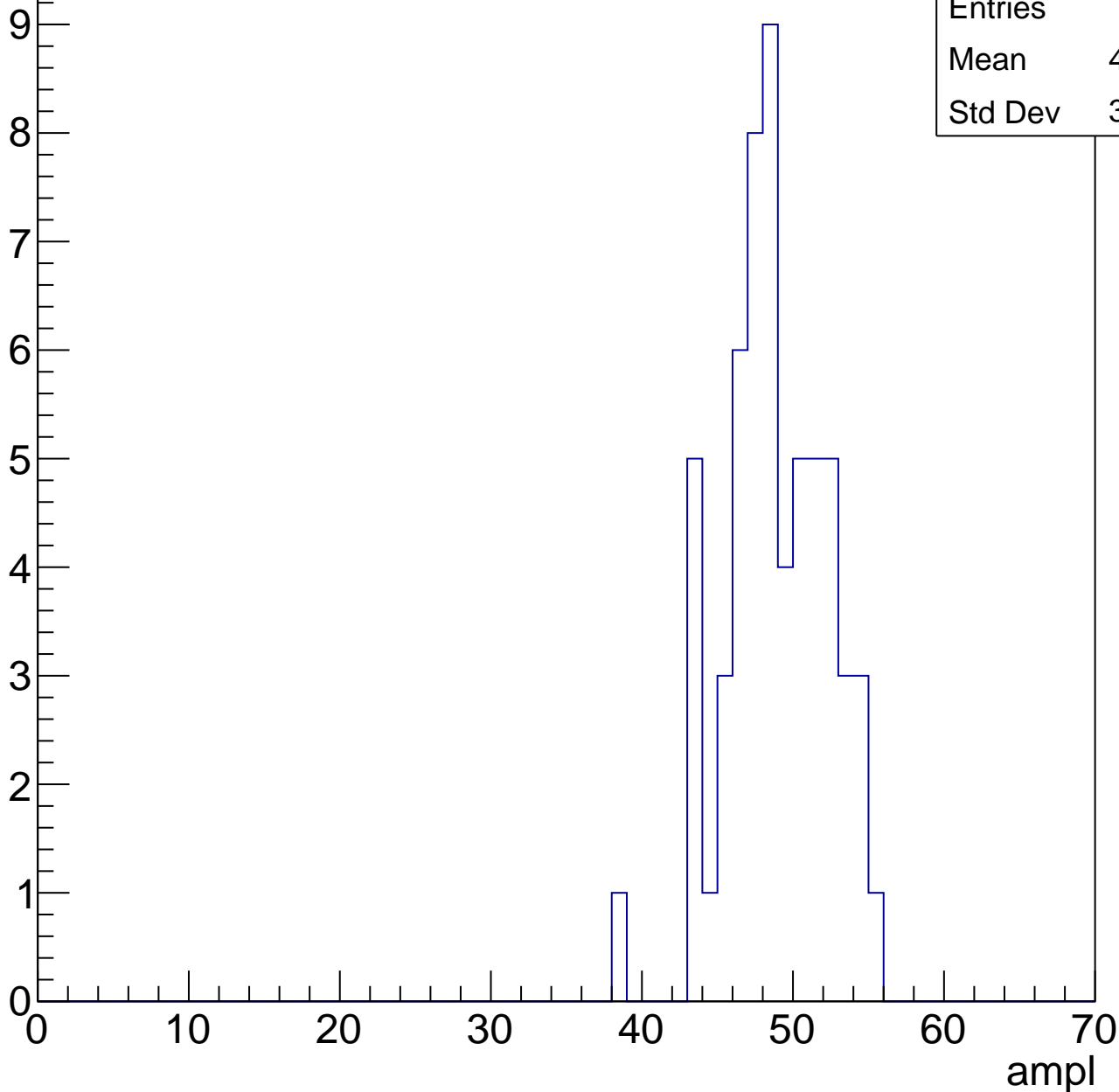


# B1L100S, U6-ch101, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

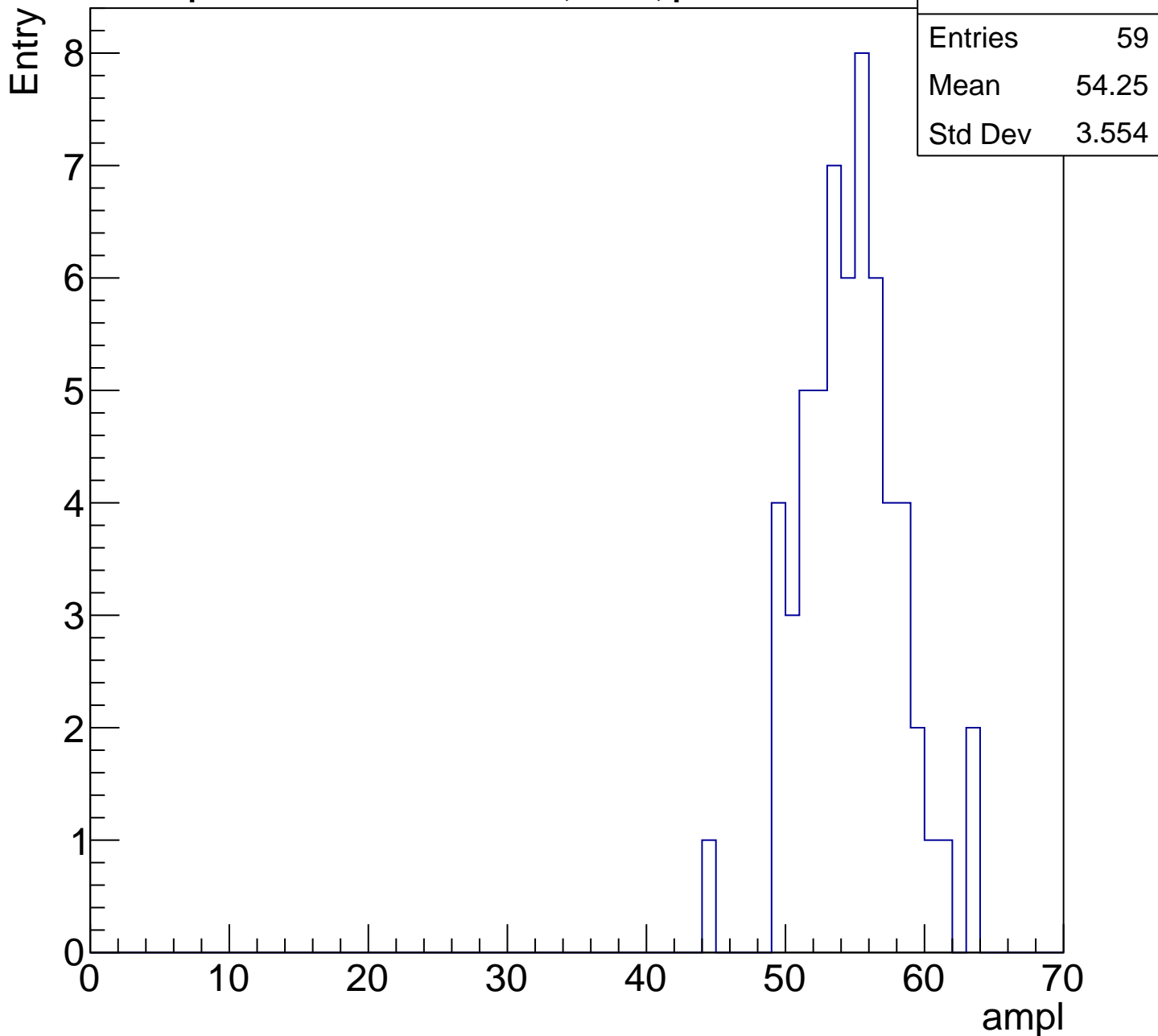
Entry

Entries	59
Mean	48.36
Std Dev	3.379



# B1L100S, U6-ch101, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

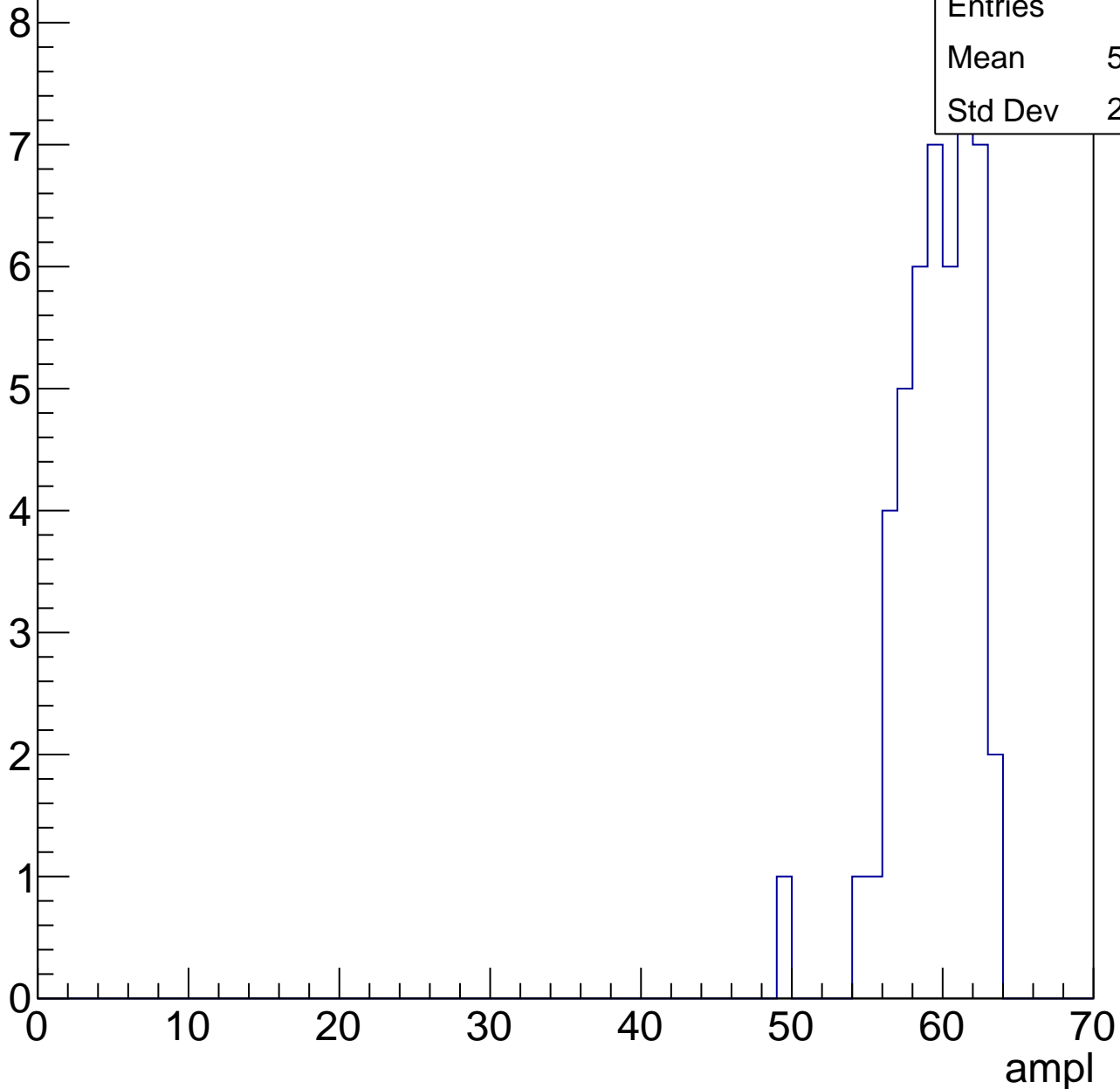


# B1L100S, U6-ch101, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	48
Mean	59.08
Std Dev	2.644

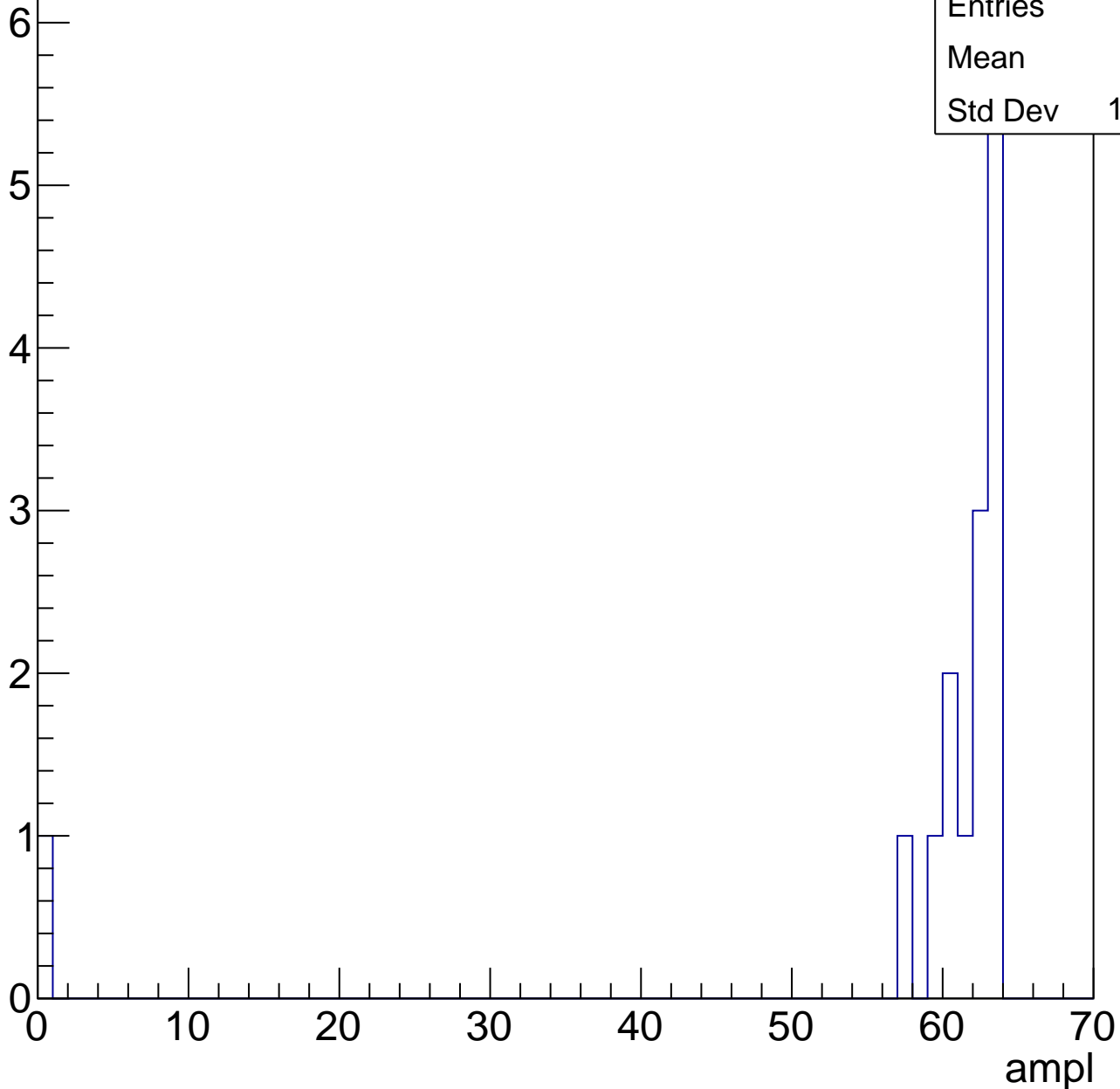


# B1L100S, U6-ch101, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	15
Mean	57.4
Std Dev	15.44

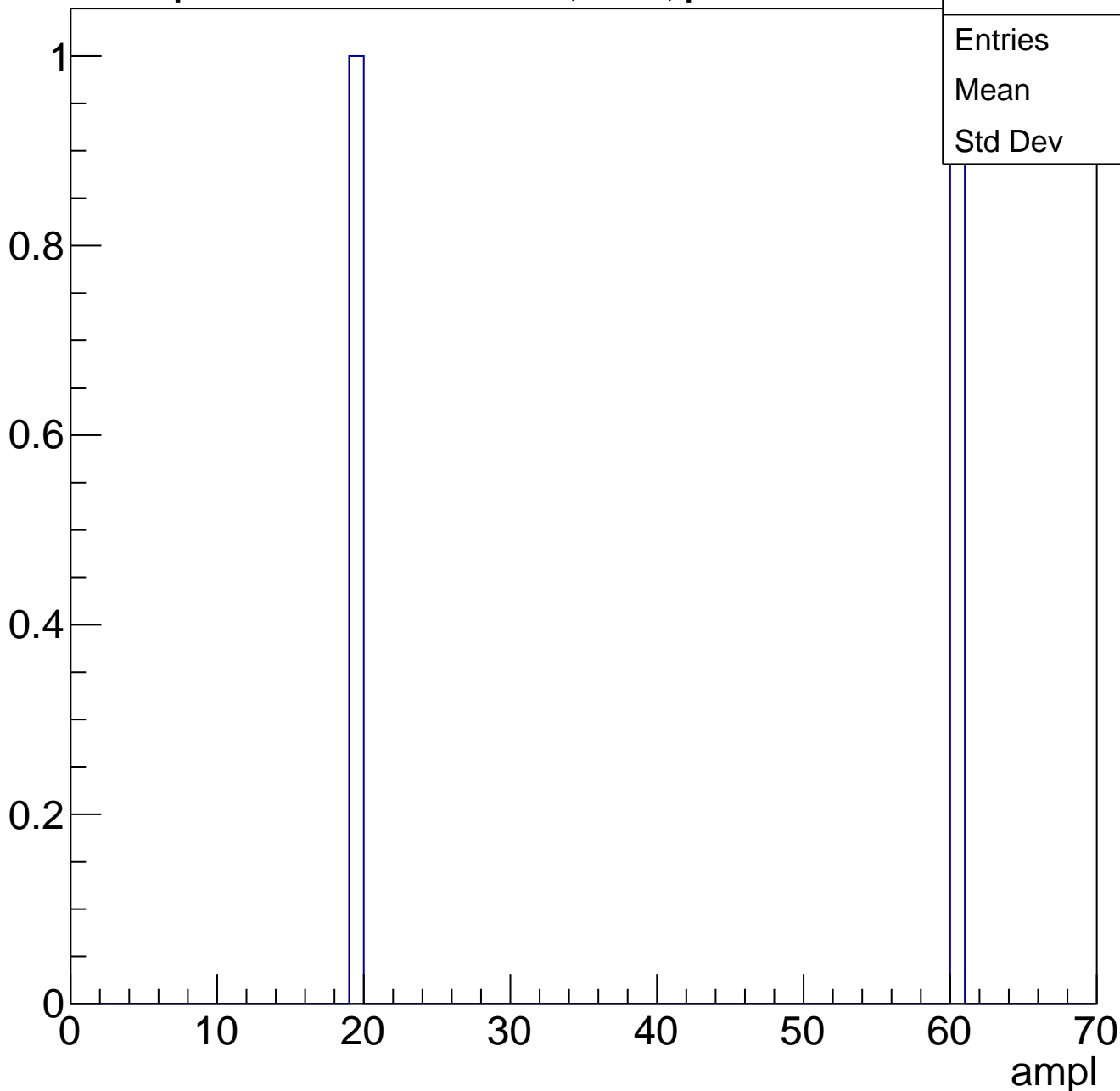




# B1L100S, U6-ch101, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	2
Mean	39.5
Std Dev	20.5

# B1L100S, U6-ch102, adc0

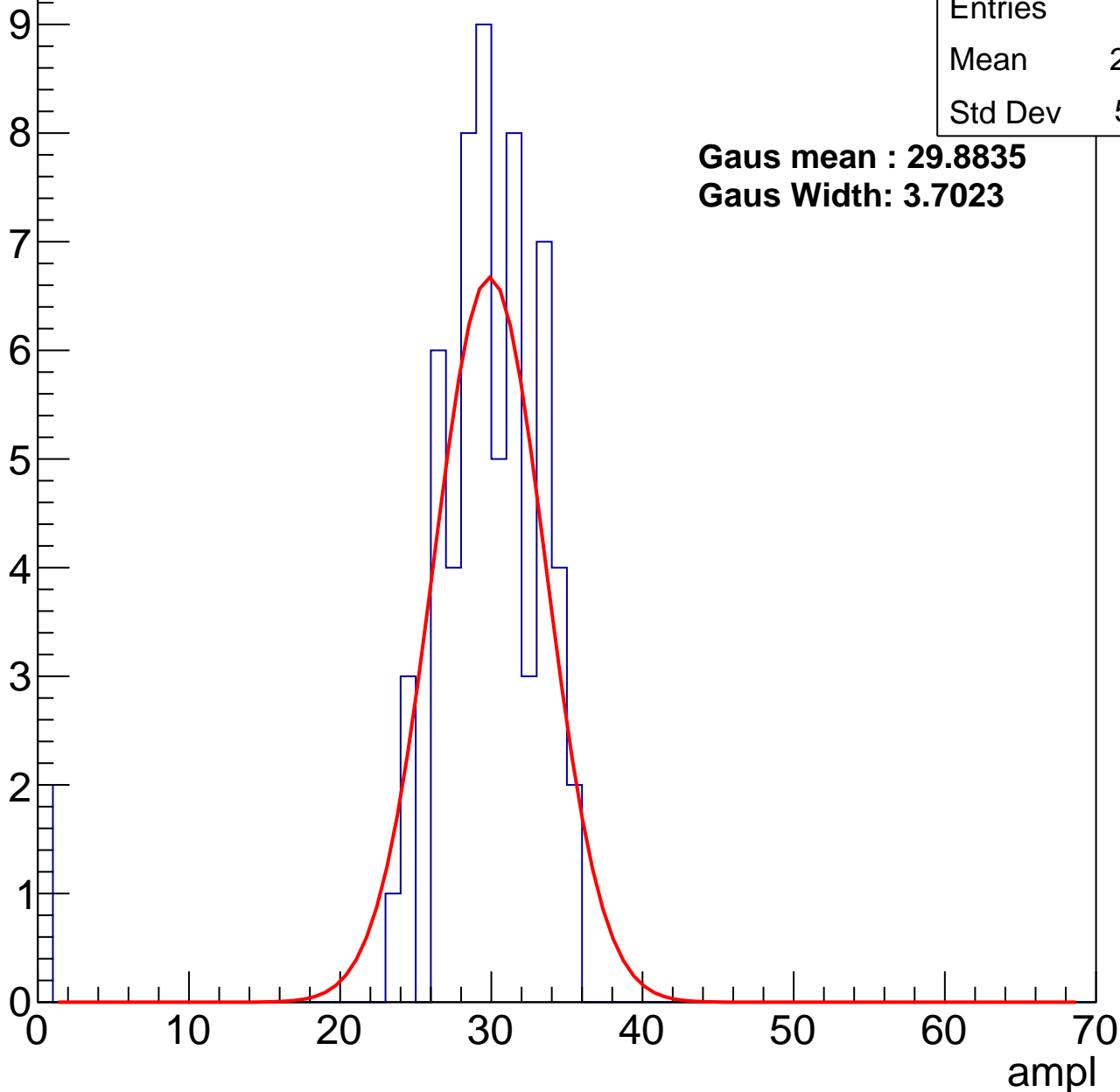
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	62
Mean	28.63
Std Dev	5.971

**Gaus mean : 29.8835**

**Gaus Width: 3.7023**



# B1L100S, U6-ch102, adc1

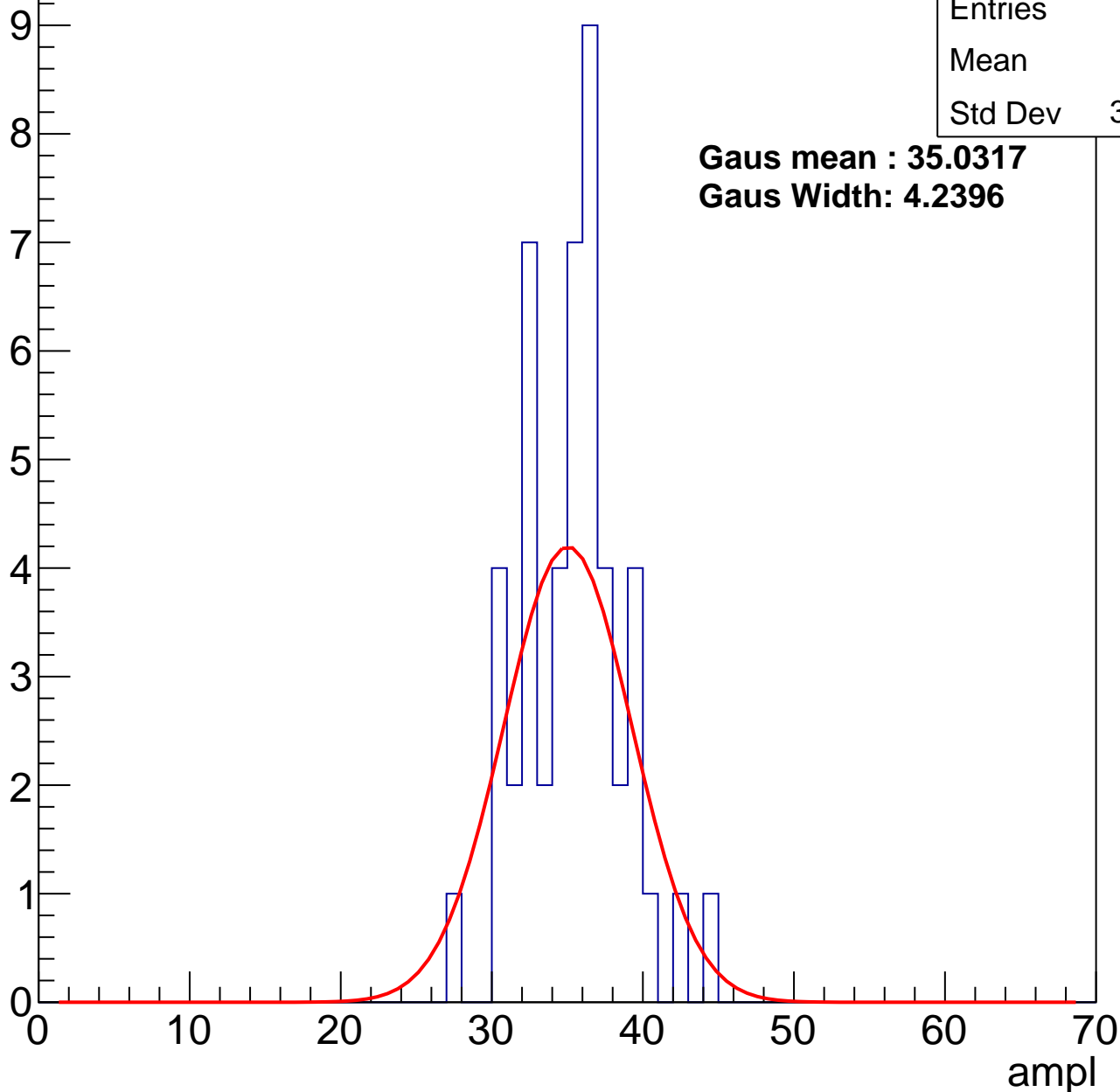
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	49
Mean	34.9
Std Dev	3.297

**Gaus mean : 35.0317**

**Gaus Width: 4.2396**



# B1L100S, U6-ch102, adc2

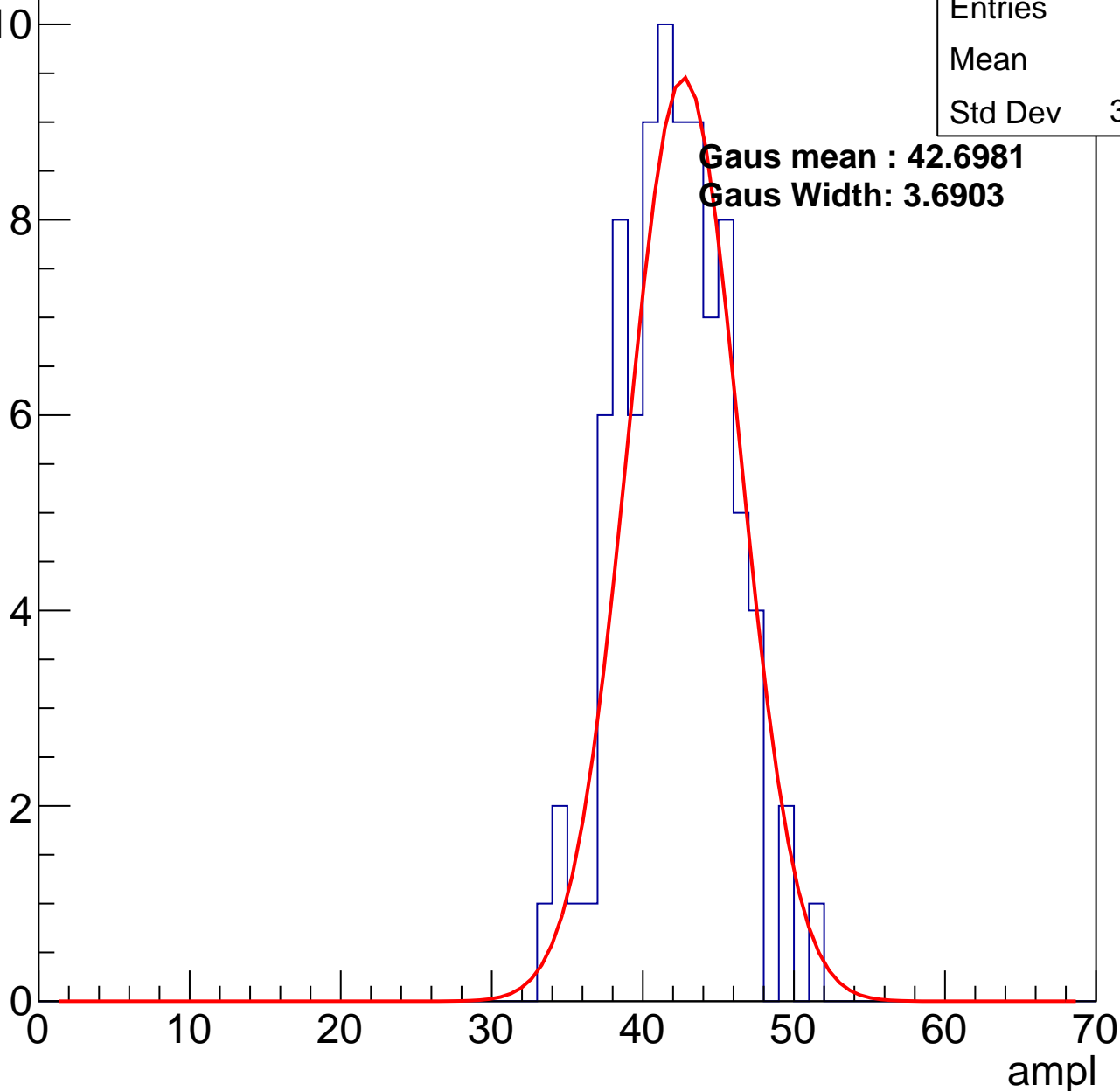
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	89
Mean	41.6
Std Dev	3.556

**Gaus mean : 42.6981**

**Gaus Width: 3.6903**

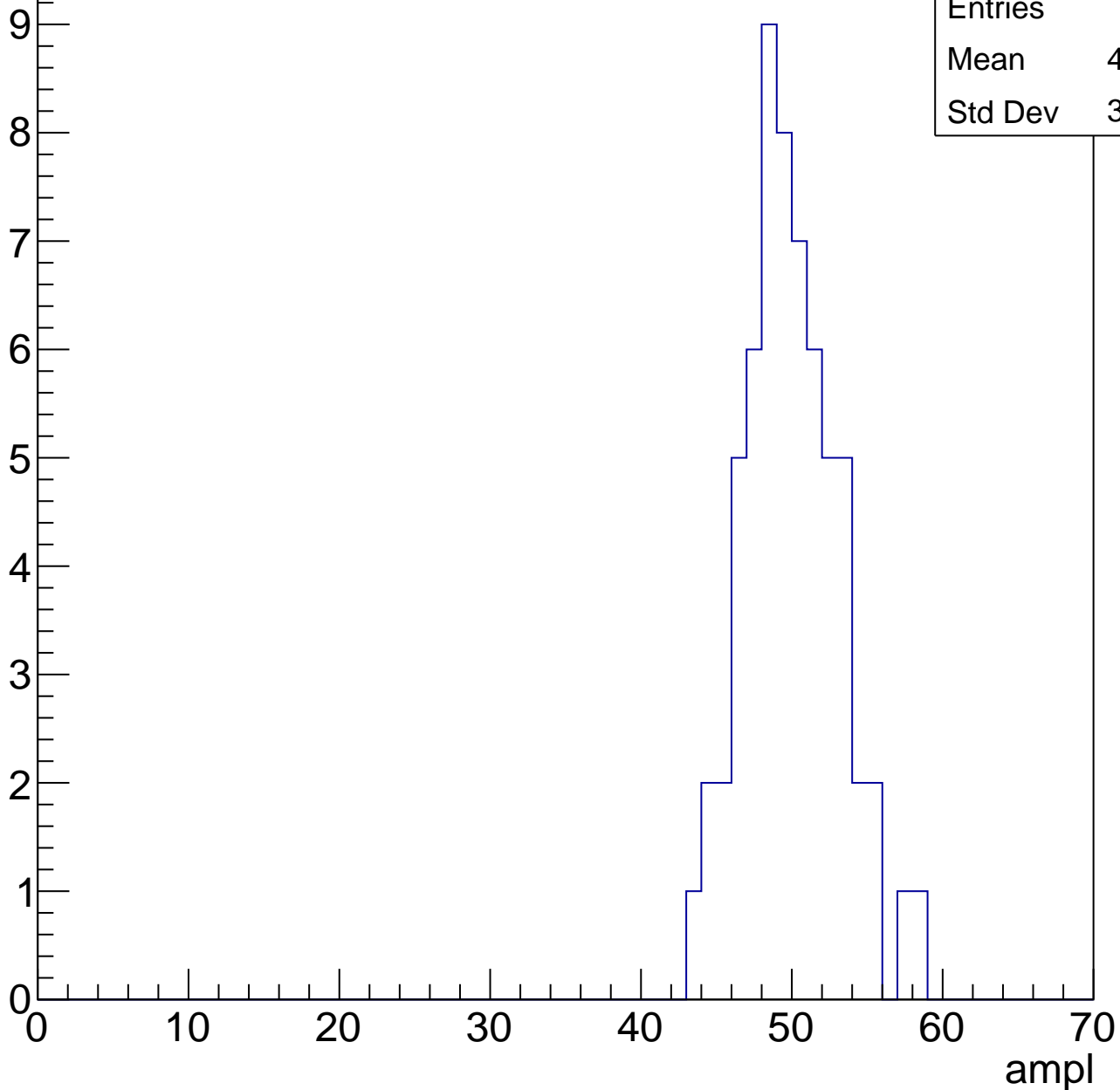


# B1L100S, U6-ch102, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	62
Mean	49.53
Std Dev	3.115

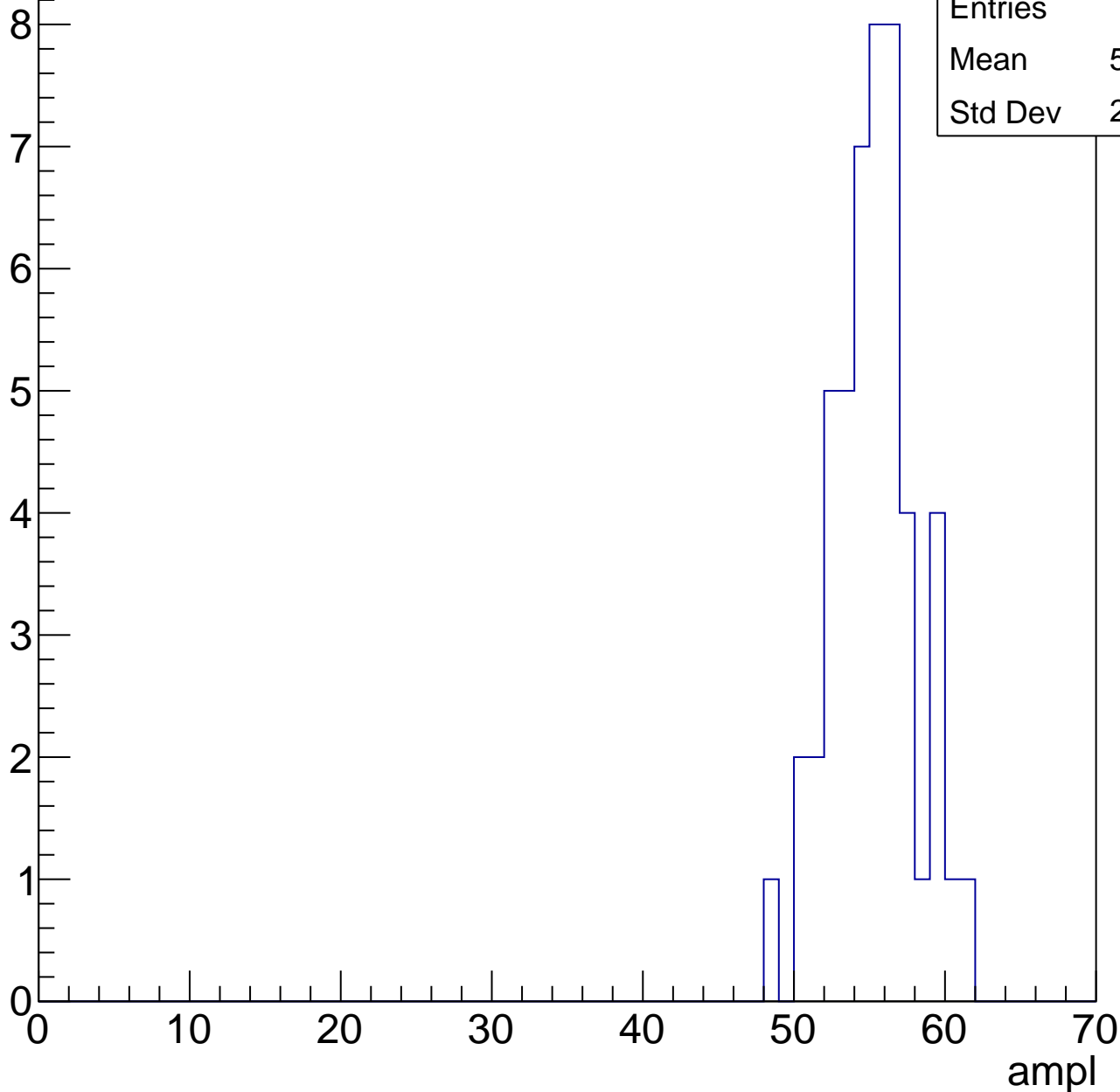


# B1L100S, U6-ch102, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

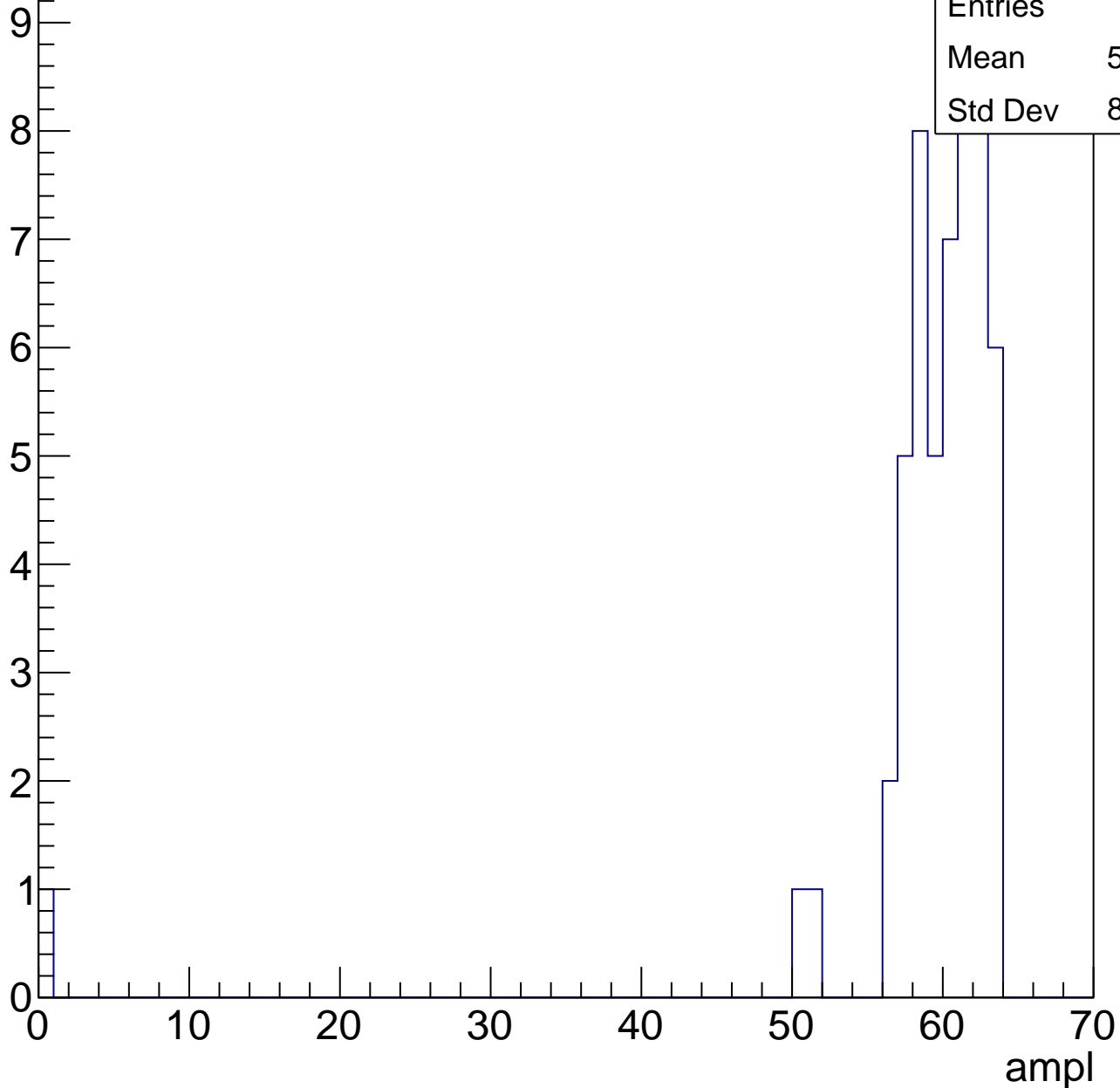
Entries	49
Mean	54.78
Std Dev	2.705



# B1L100S, U6-ch102, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

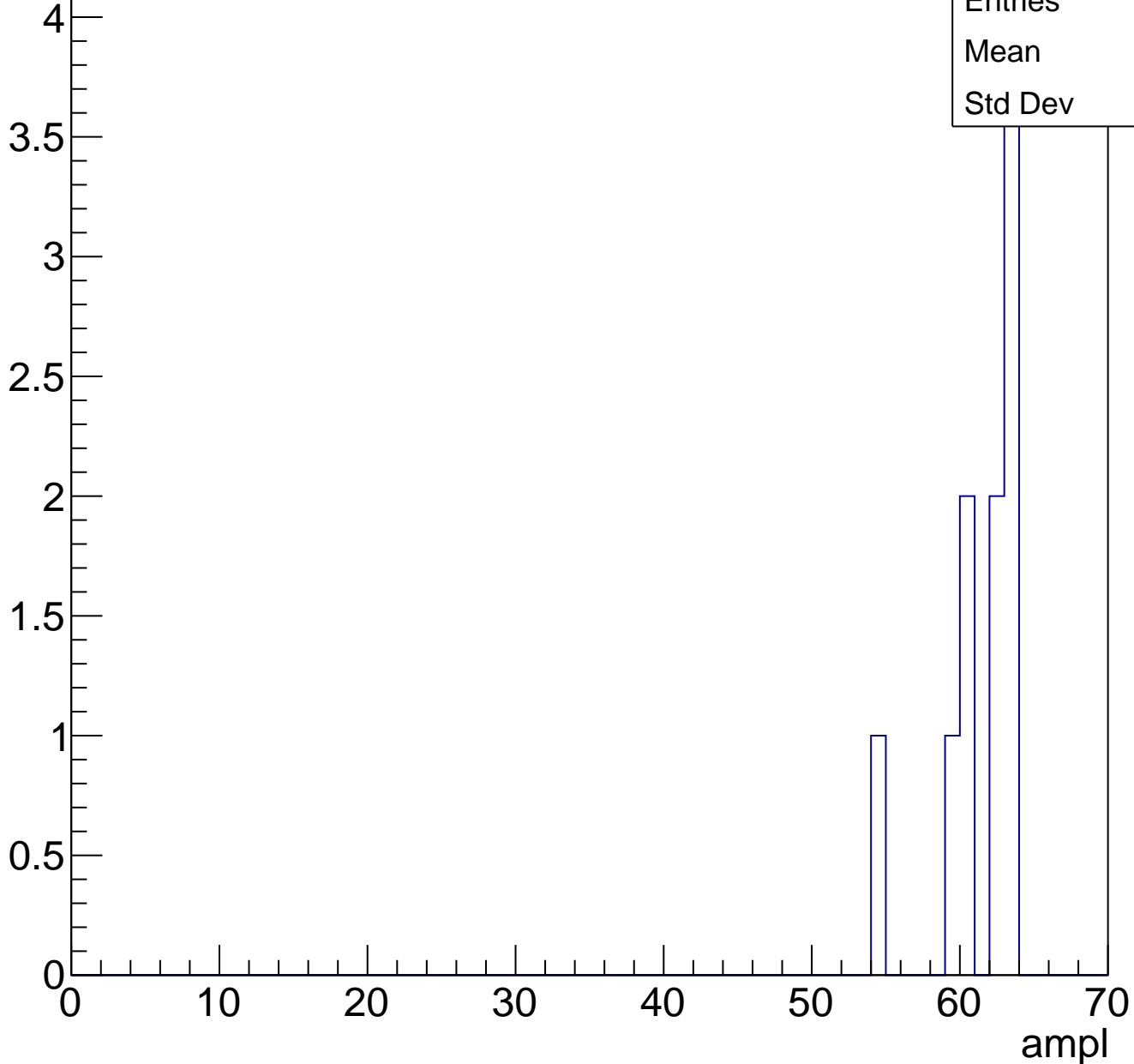
Entry



# B1L100S, U6-ch102, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	10
Mean	60.9
Std Dev	2.7



# B1L100S, U6-ch102, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



# B1L100S, U6-ch103, adc0

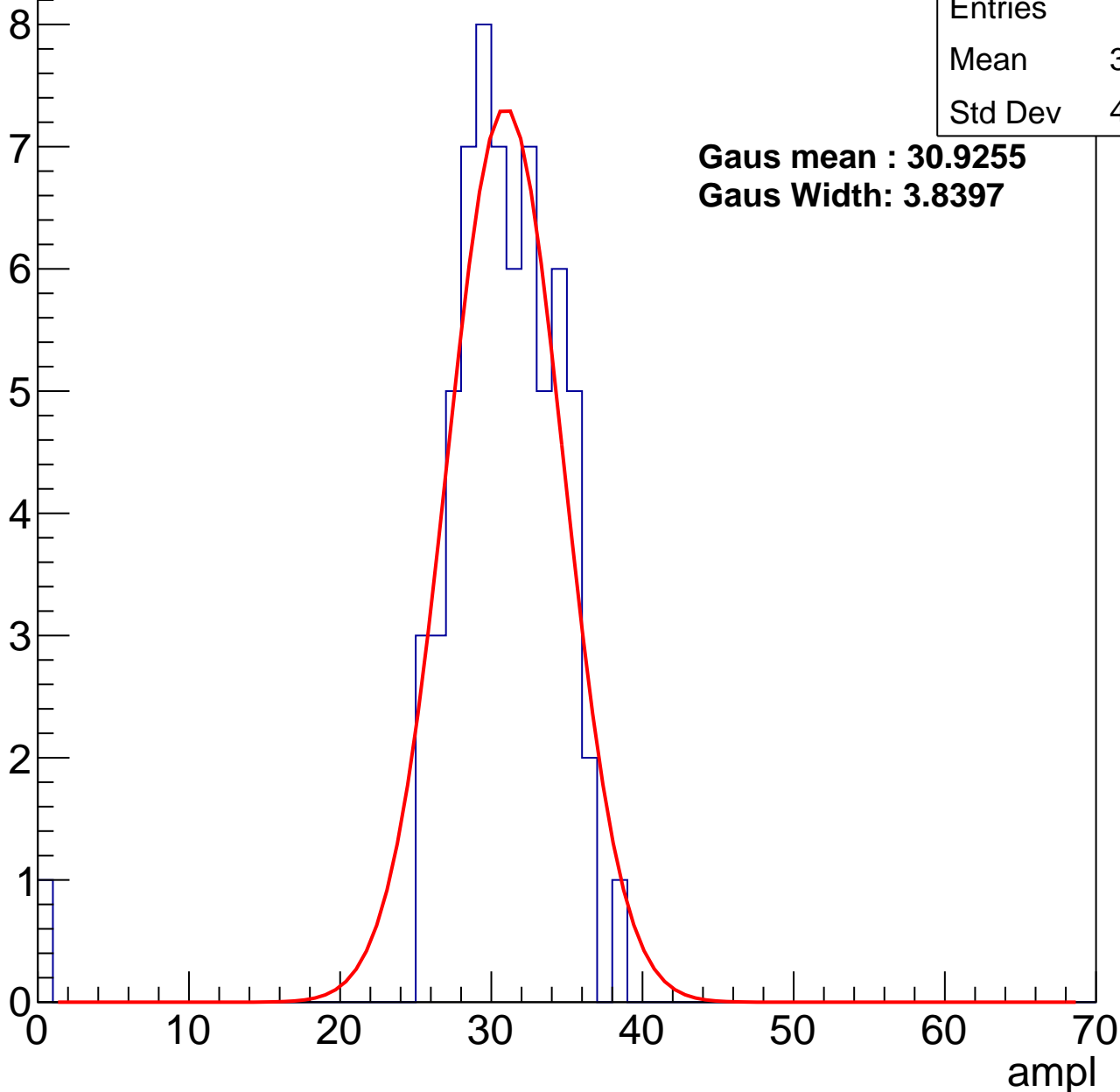
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	66
Mean	30.15
Std Dev	4.828

**Gaus mean : 30.9255**

**Gaus Width: 3.8397**



# B1L100S, U6-ch103, adc1

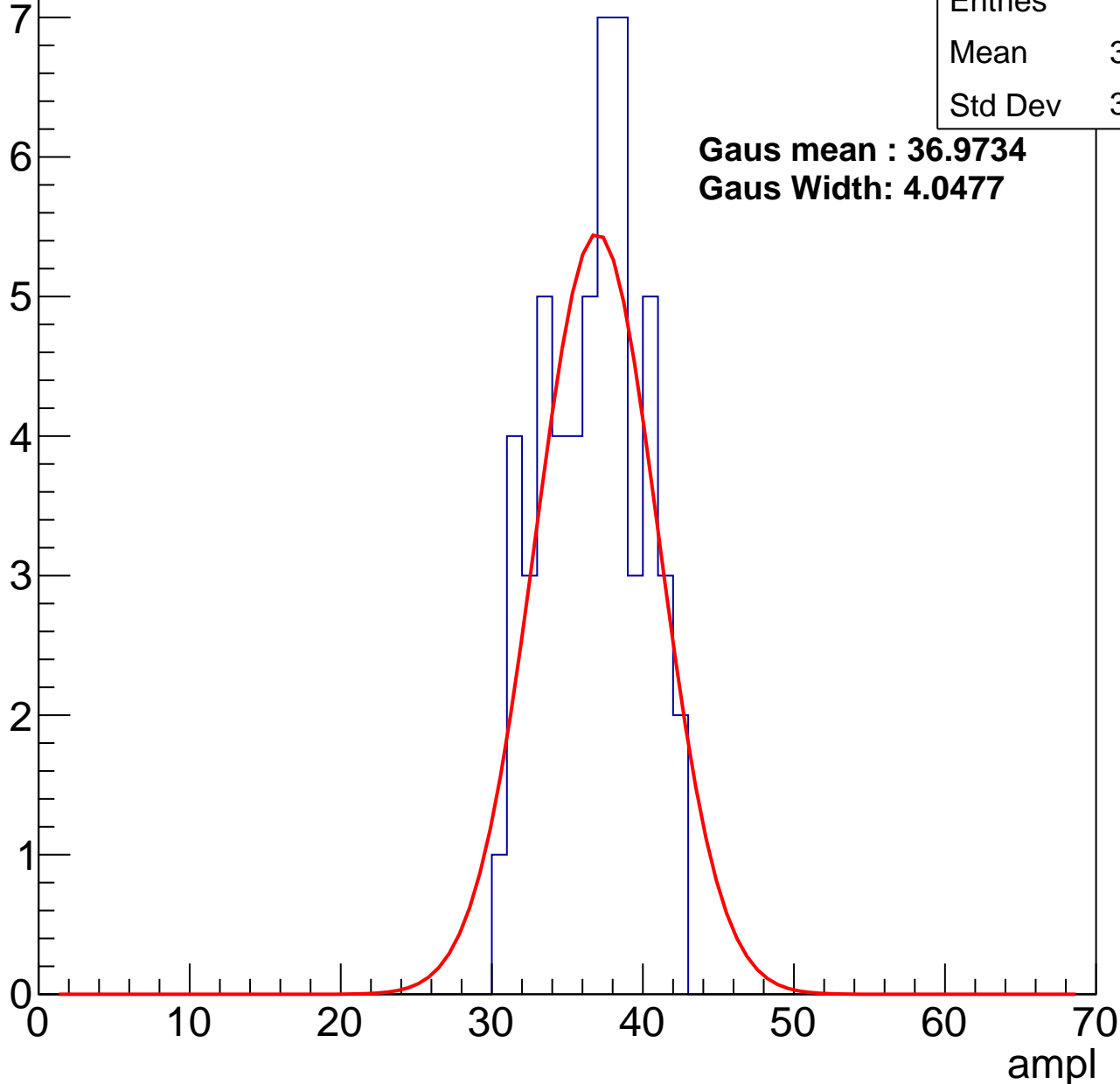
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	53
Mean	36.23
Std Dev	3.178

**Gaus mean : 36.9734**

**Gaus Width: 4.0477**



# B1L100S, U6-ch103, adc2

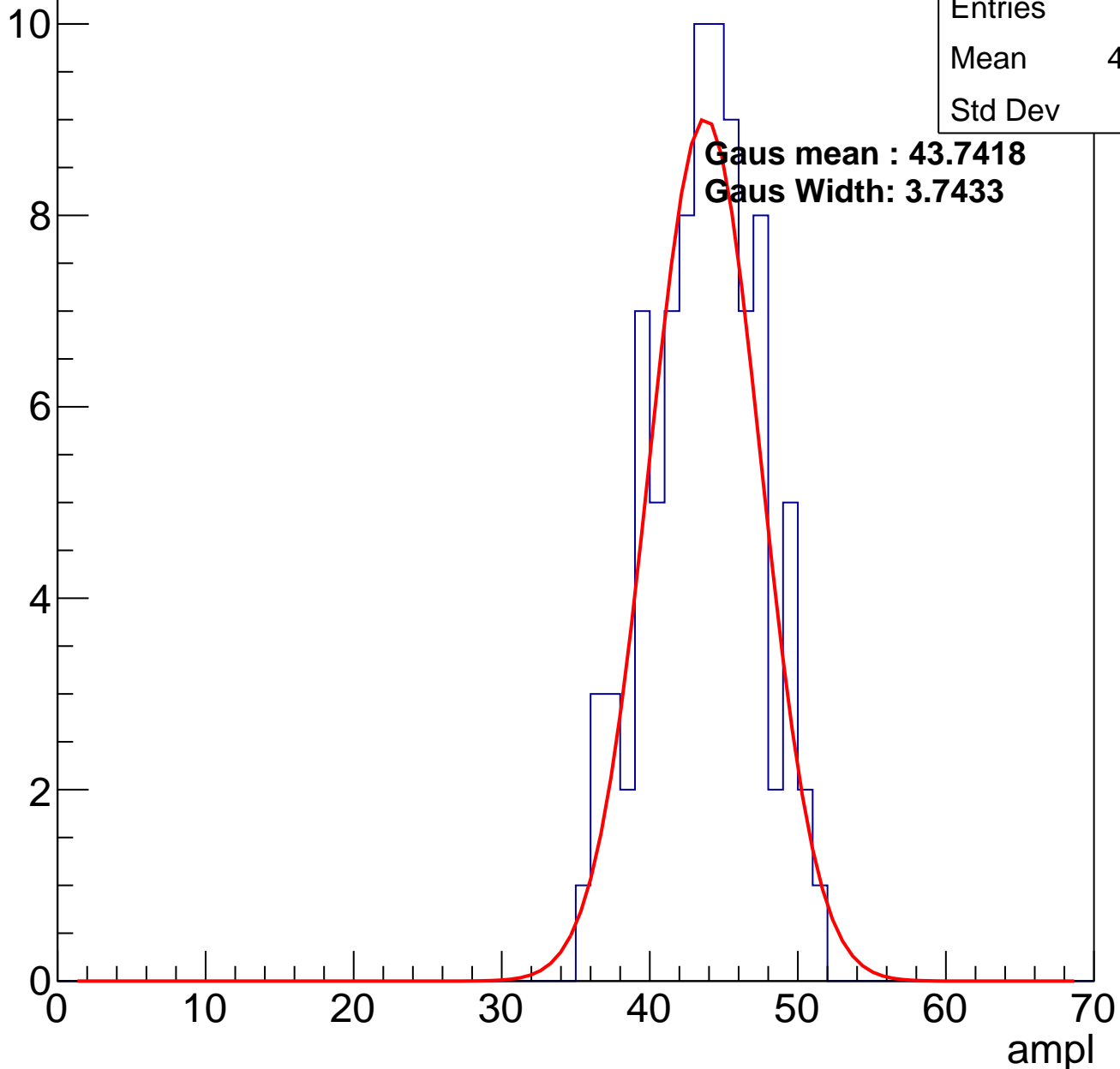
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	90
Mean	43.23
Std Dev	3.63

**Gaus mean : 43.7418**

**Gaus Width: 3.7433**

Entry

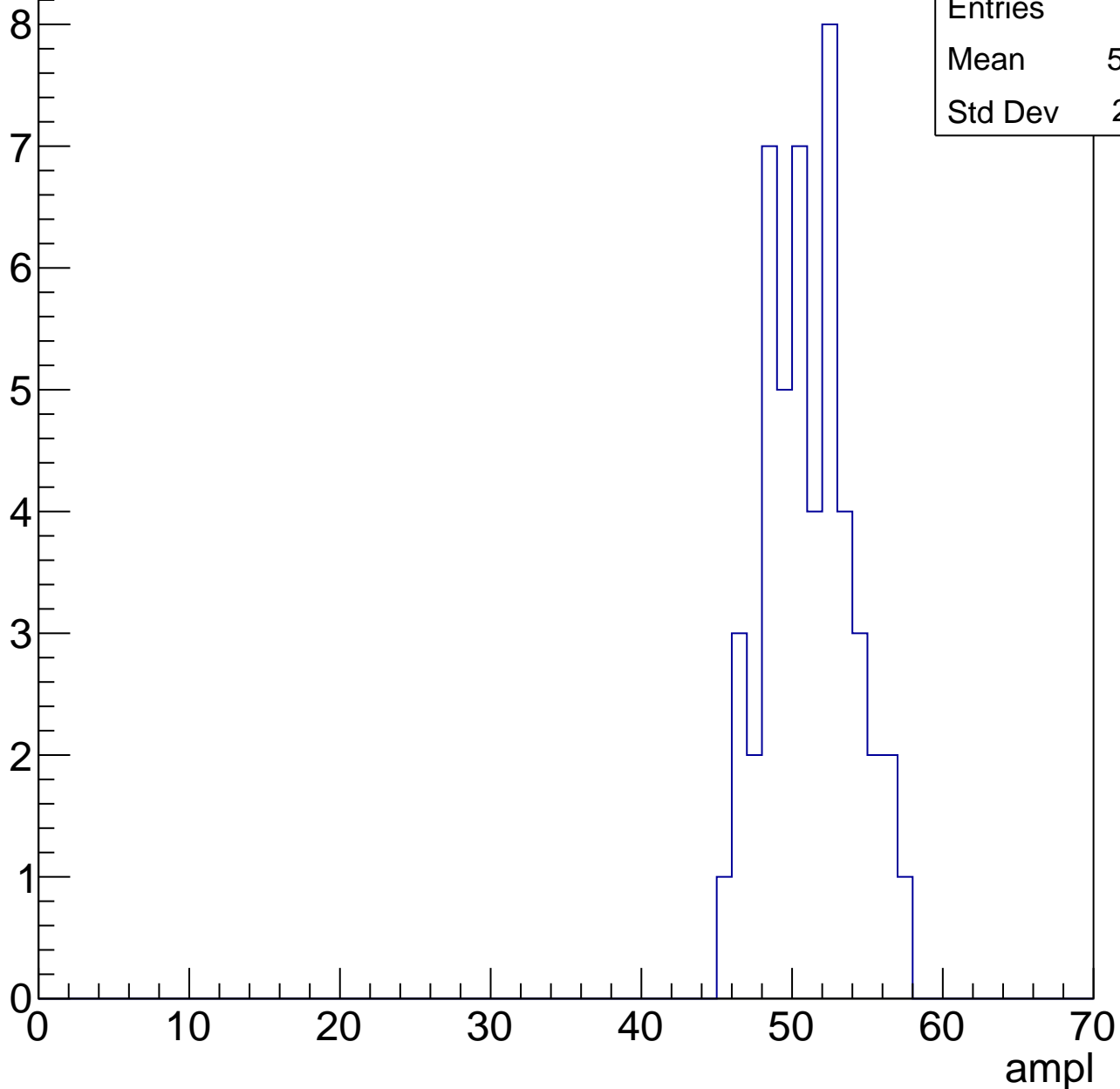


# B1L100S, U6-ch103, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	49
Mean	50.63
Std Dev	2.841

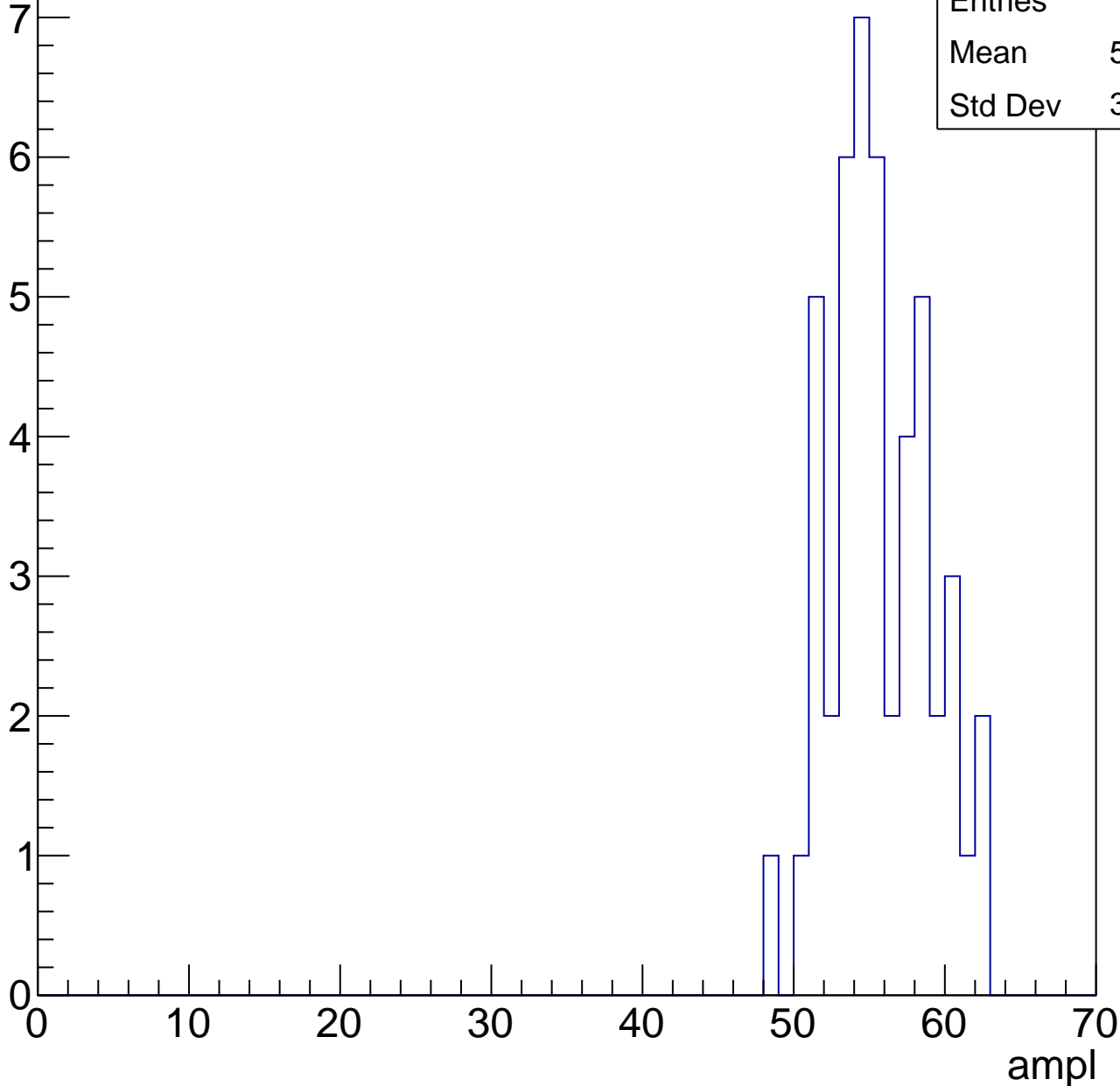


# B1L100S, U6-ch103, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

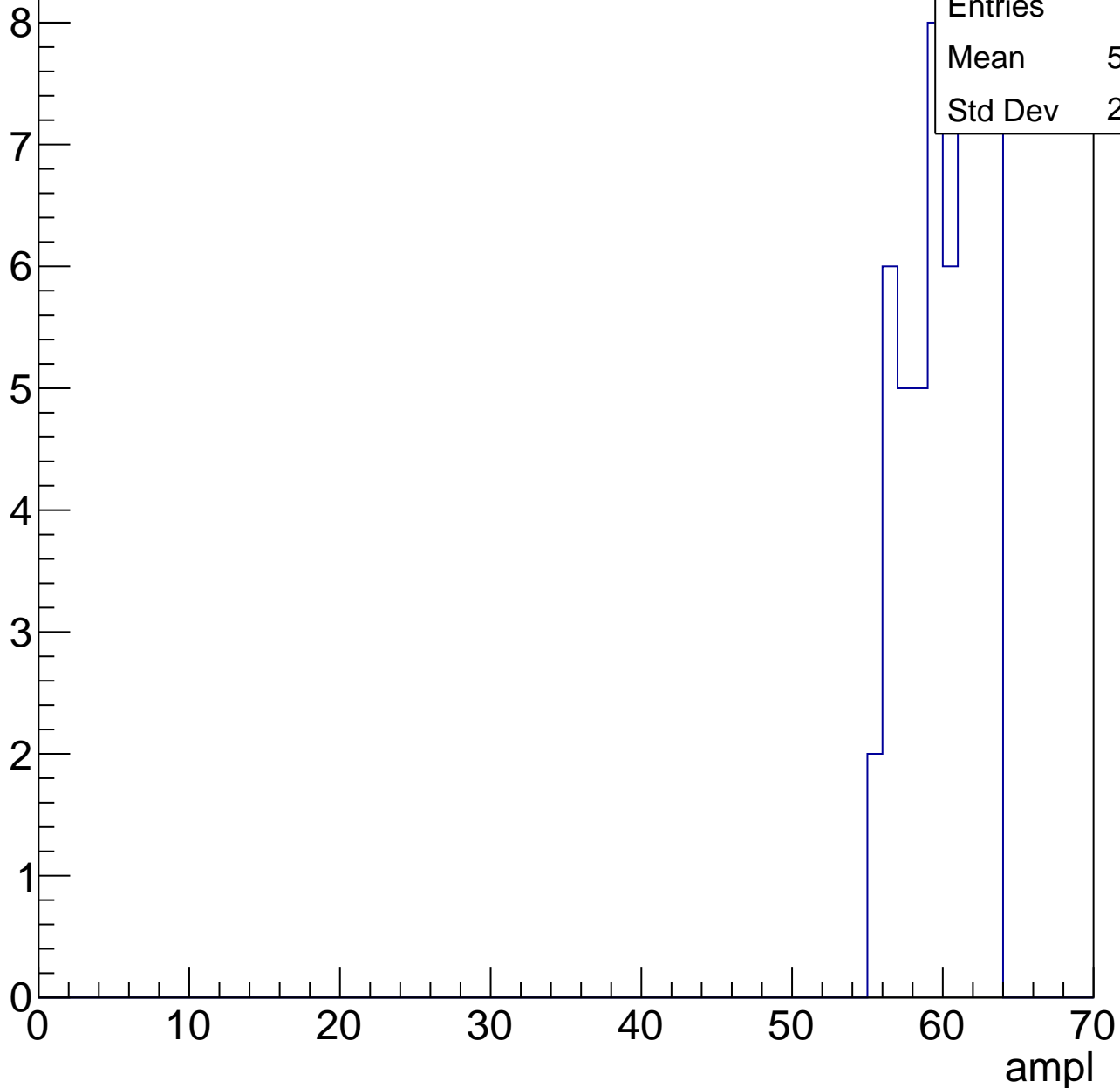
Entries	47
Mean	55.23
Std Dev	3.276



# B1L100S, U6-ch103, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

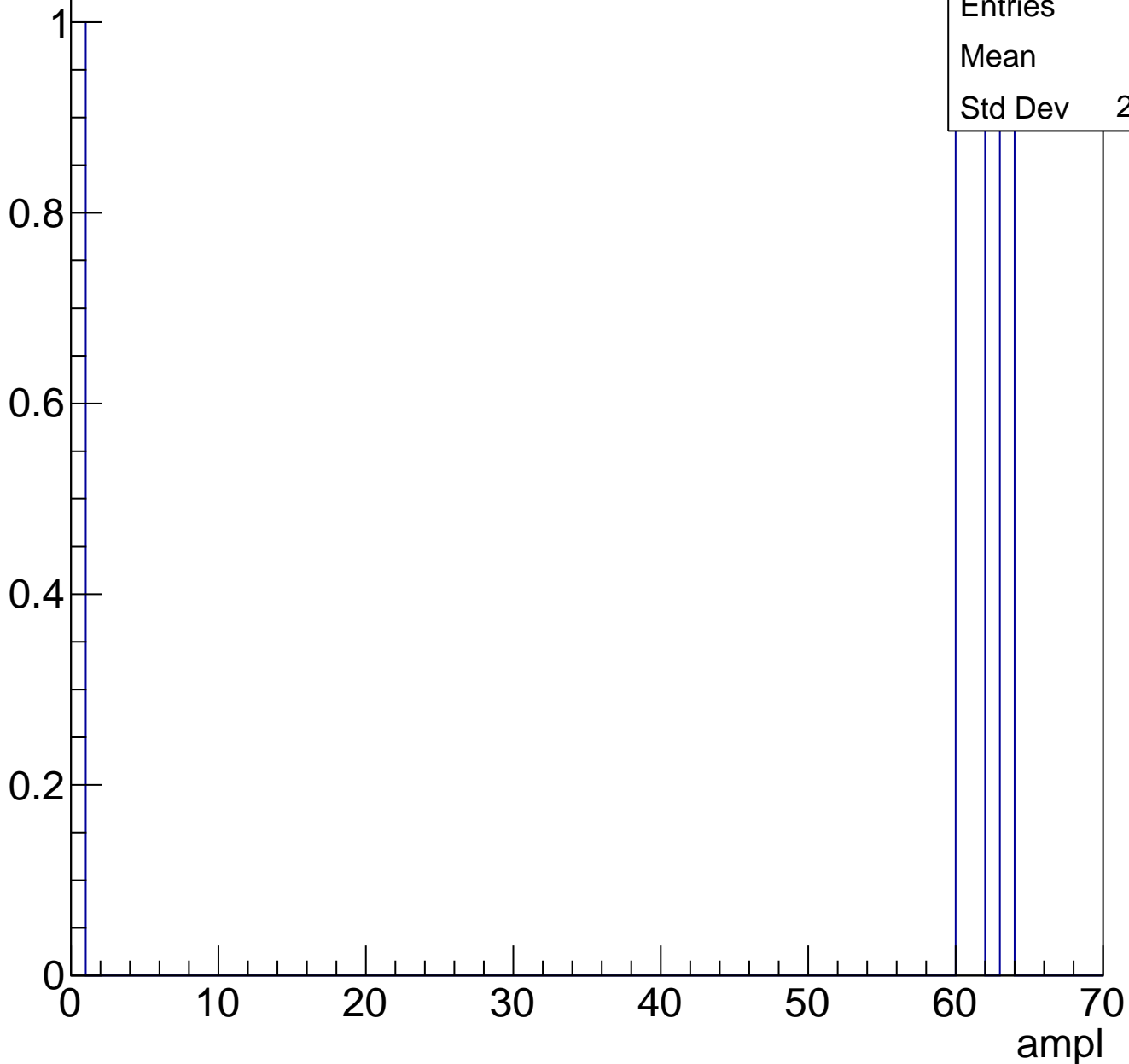


Entries	56
Mean	59.66
Std Dev	2.407

# B1L100S, U6-ch103, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

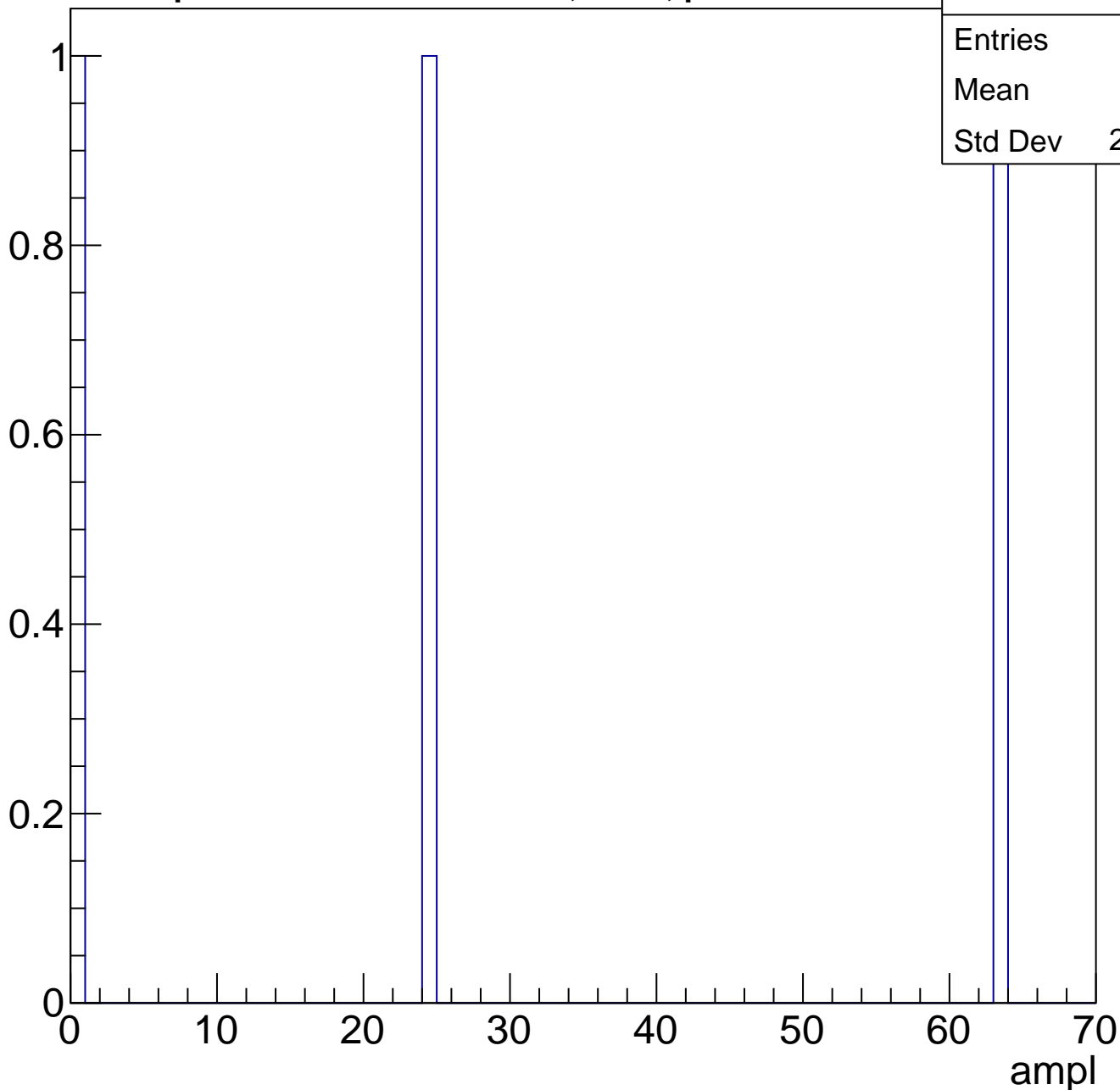




# B1L100S, U6-ch103, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



# B1L100S, U6-ch104, adc0

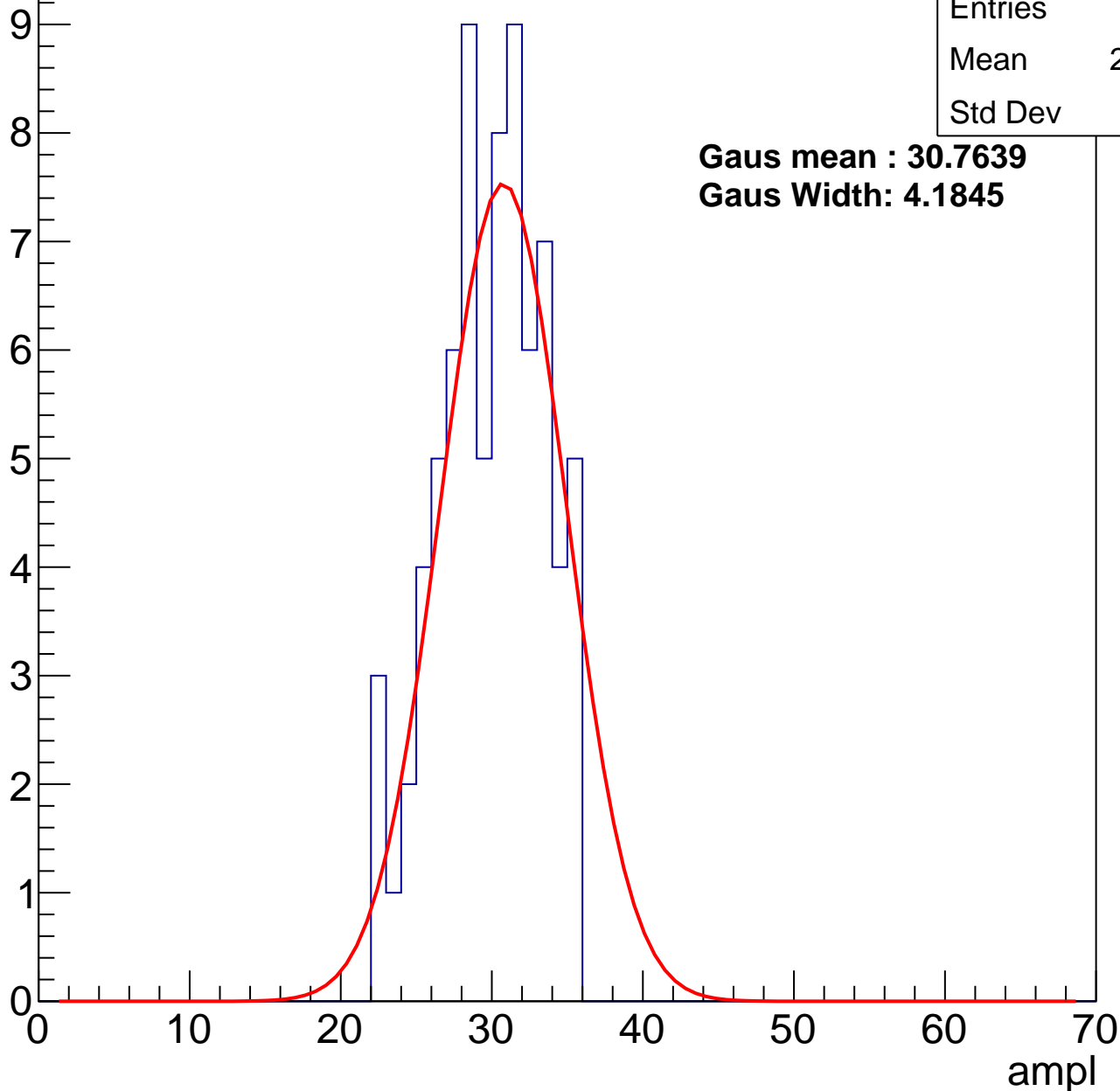
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	74
Mean	29.45
Std Dev	3.39

**Gaus mean : 30.7639**

**Gaus Width: 4.1845**



# B1L100S, U6-ch104, adc1

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	61
Mean	36.82
Std Dev	3.247

**Gaus mean : 37.1892**

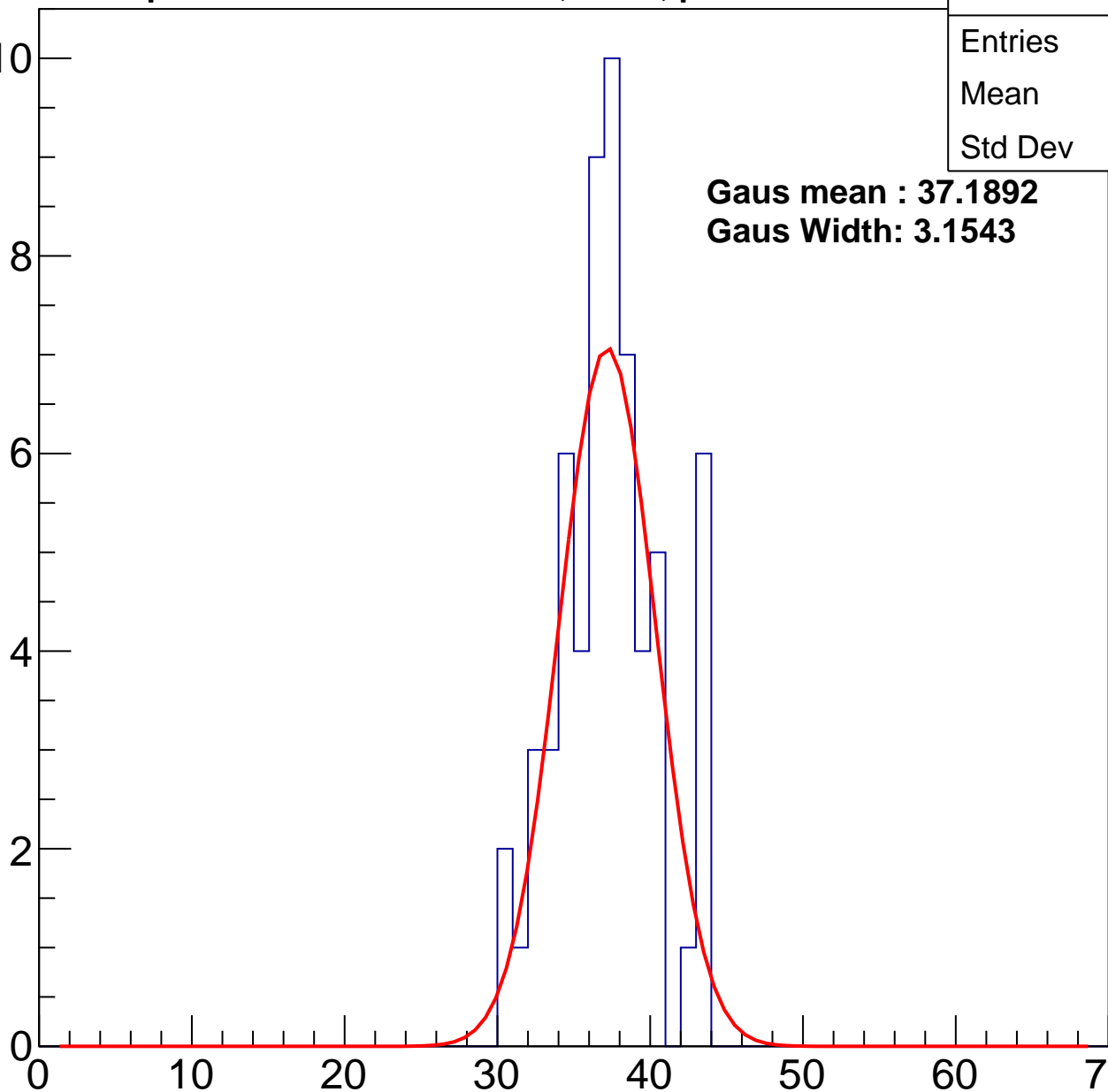
**Gaus Width: 3.1543**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B1L100S, U6-ch104, adc2

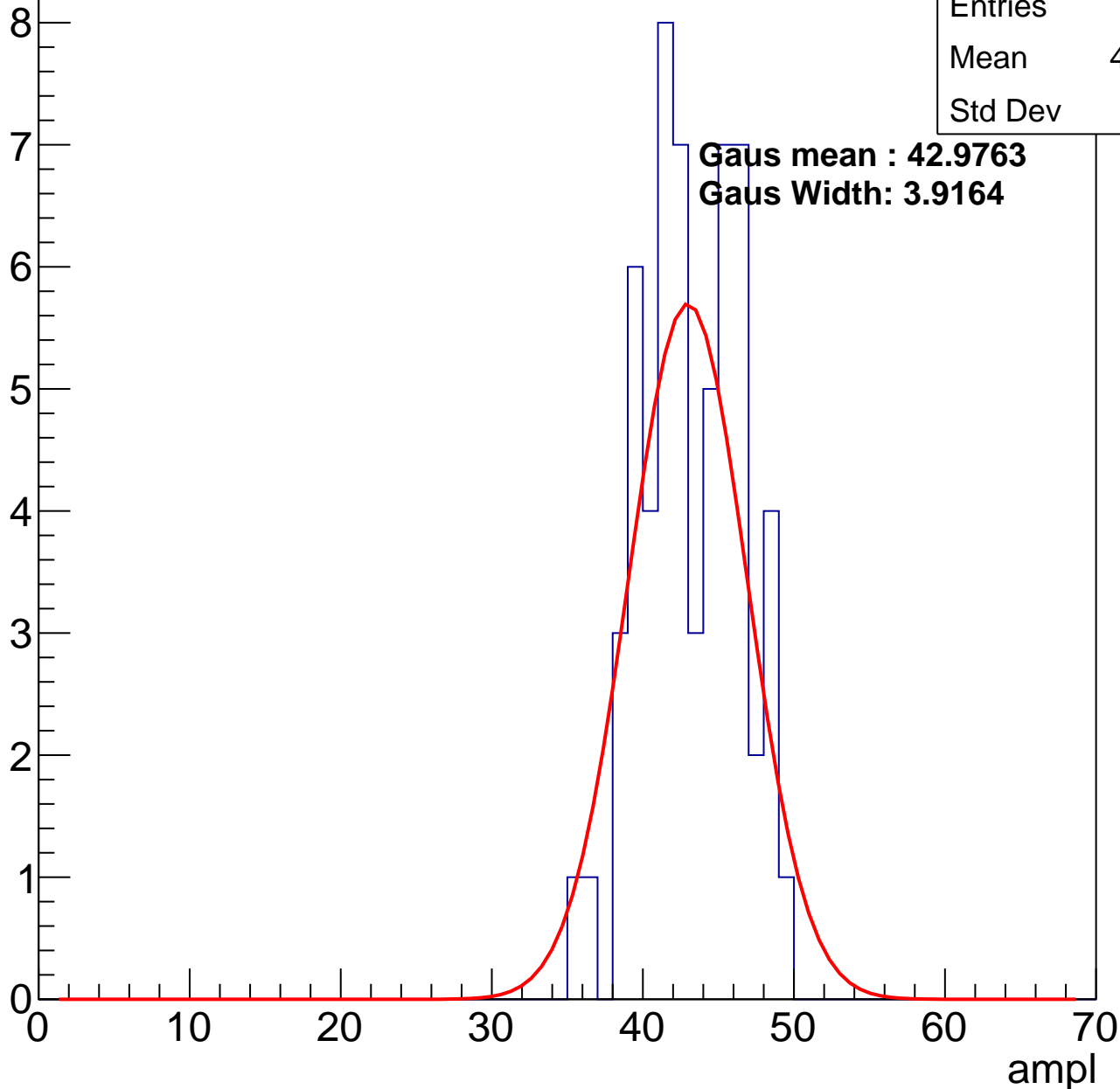
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	59
Mean	42.75
Std Dev	3.24

**Gaus mean : 42.9763**

**Gaus Width: 3.9164**

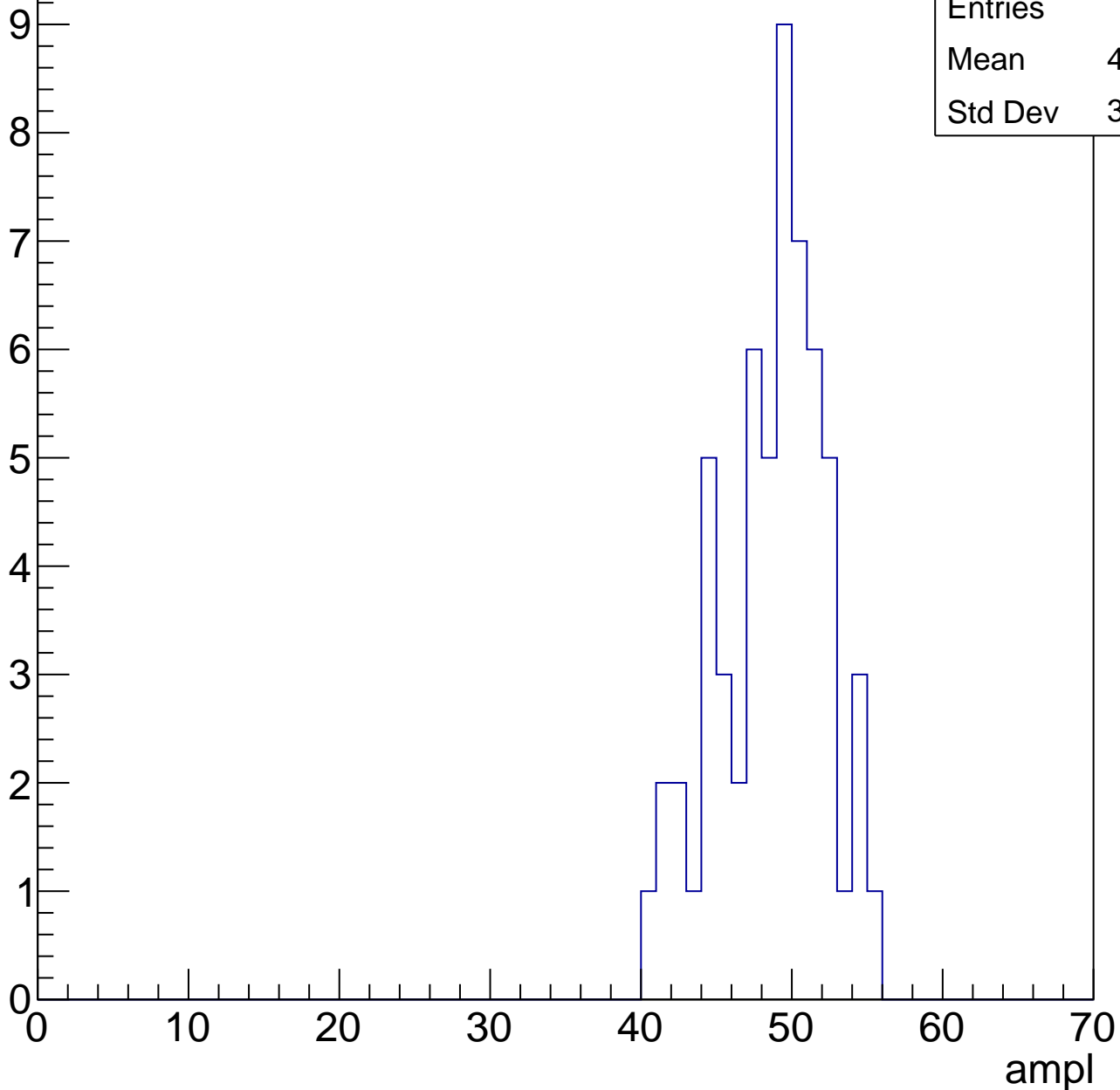


# B1L100S, U6-ch104, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

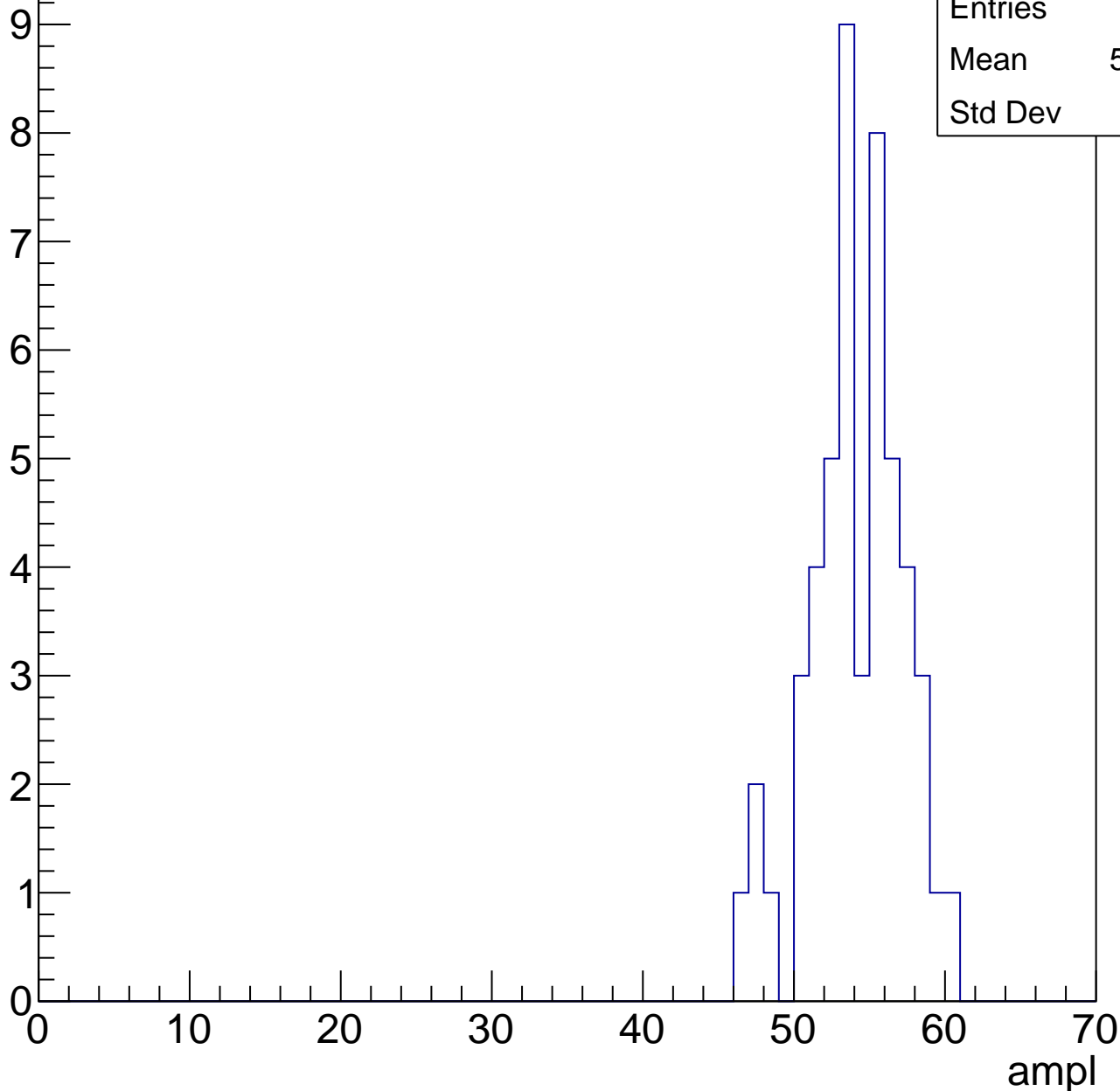
Entries	59
Mean	48.22
Std Dev	3.518



# B1L100S, U6-ch104, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



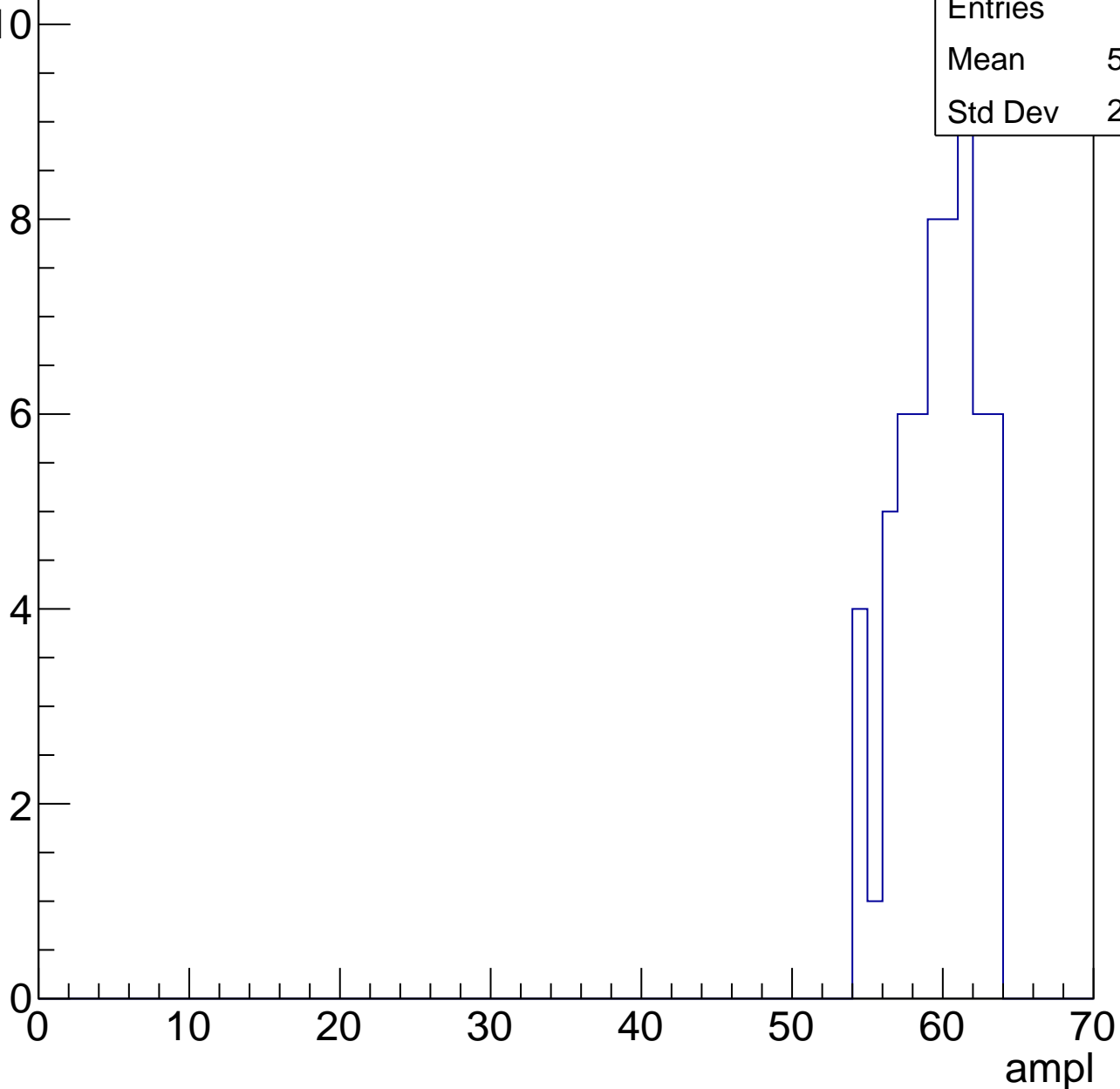
Entries	50
Mean	53.64
Std Dev	3.09

# B1L100S, U6-ch104, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

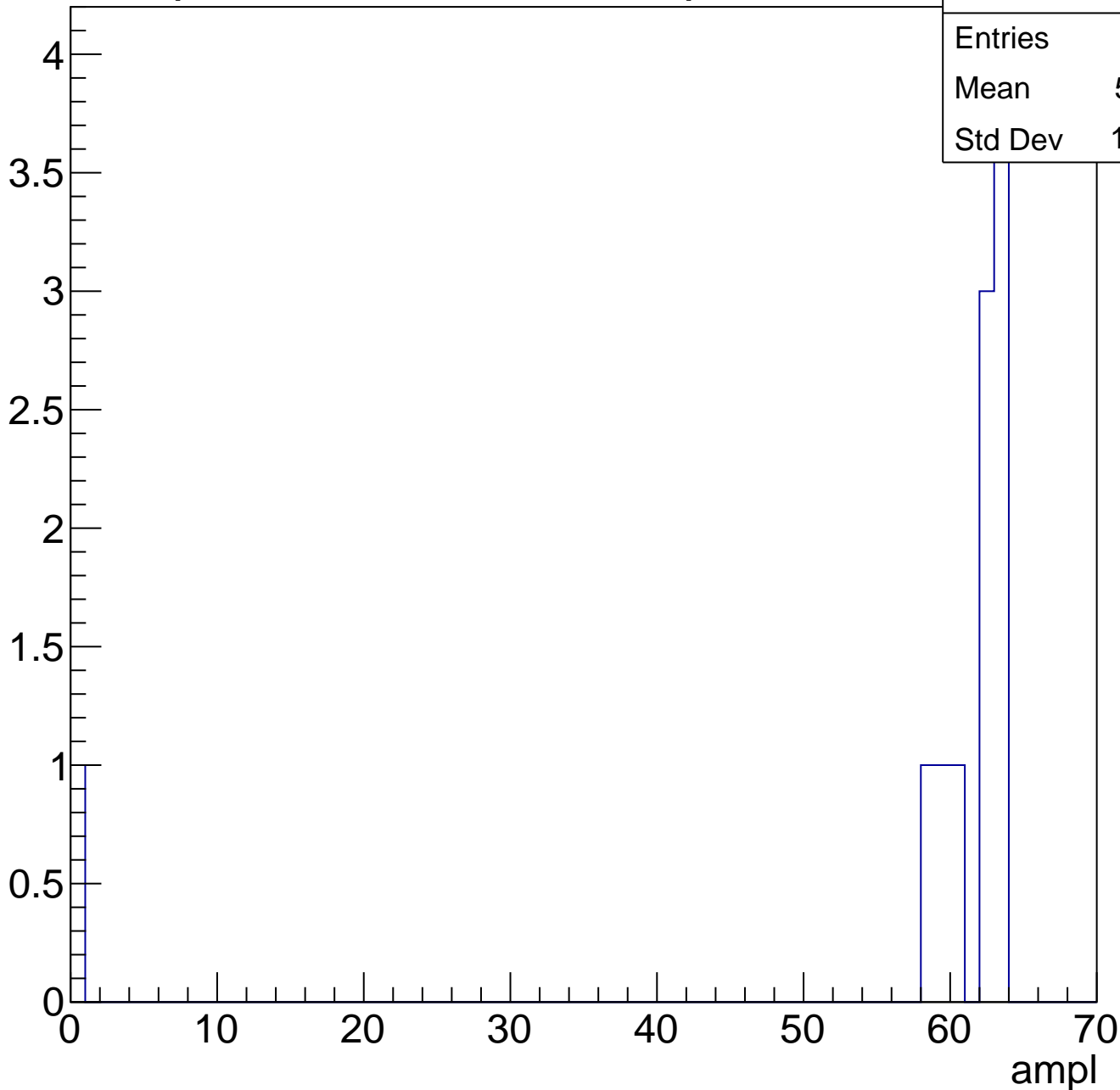
Entries	60
Mean	59.22
Std Dev	2.537



# B1L100S, U6-ch104, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

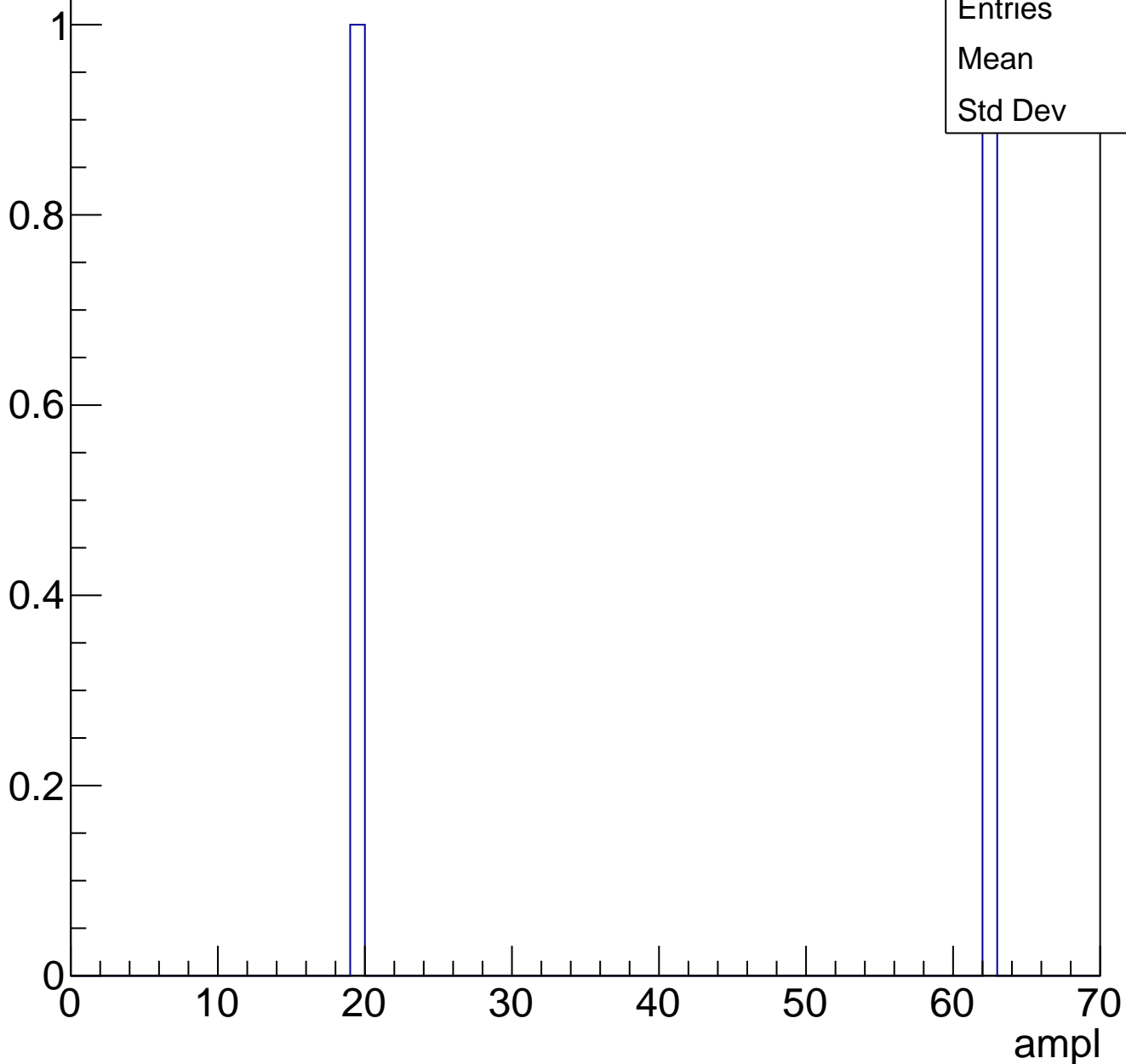




# B1L100S, U6-ch104, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



# B1L100S, U6-ch105, adc0

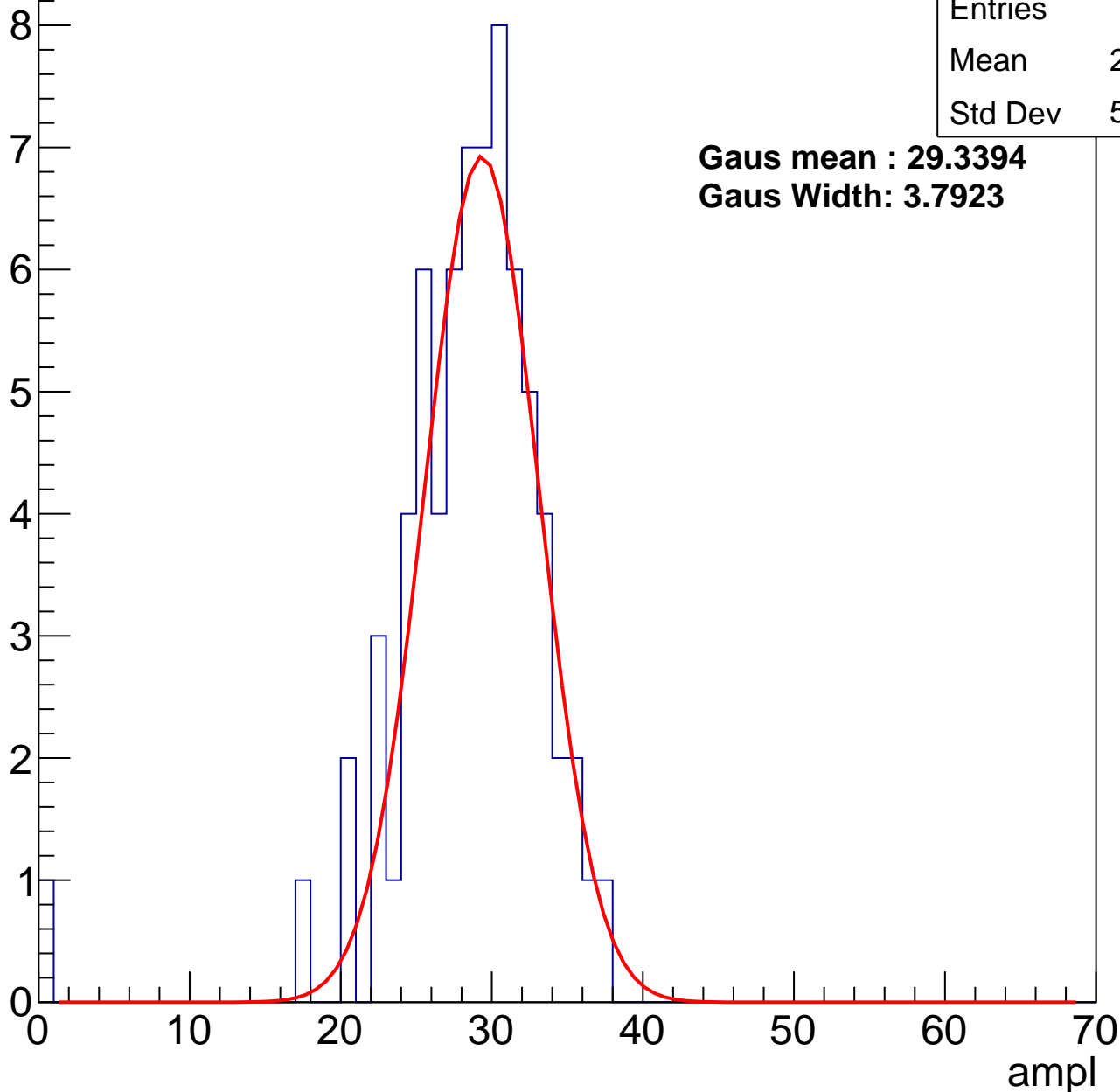
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	71
Mean	27.97
Std Dev	5.165

**Gaus mean : 29.3394**

**Gaus Width: 3.7923**



# B1L100S, U6-ch105, adc1

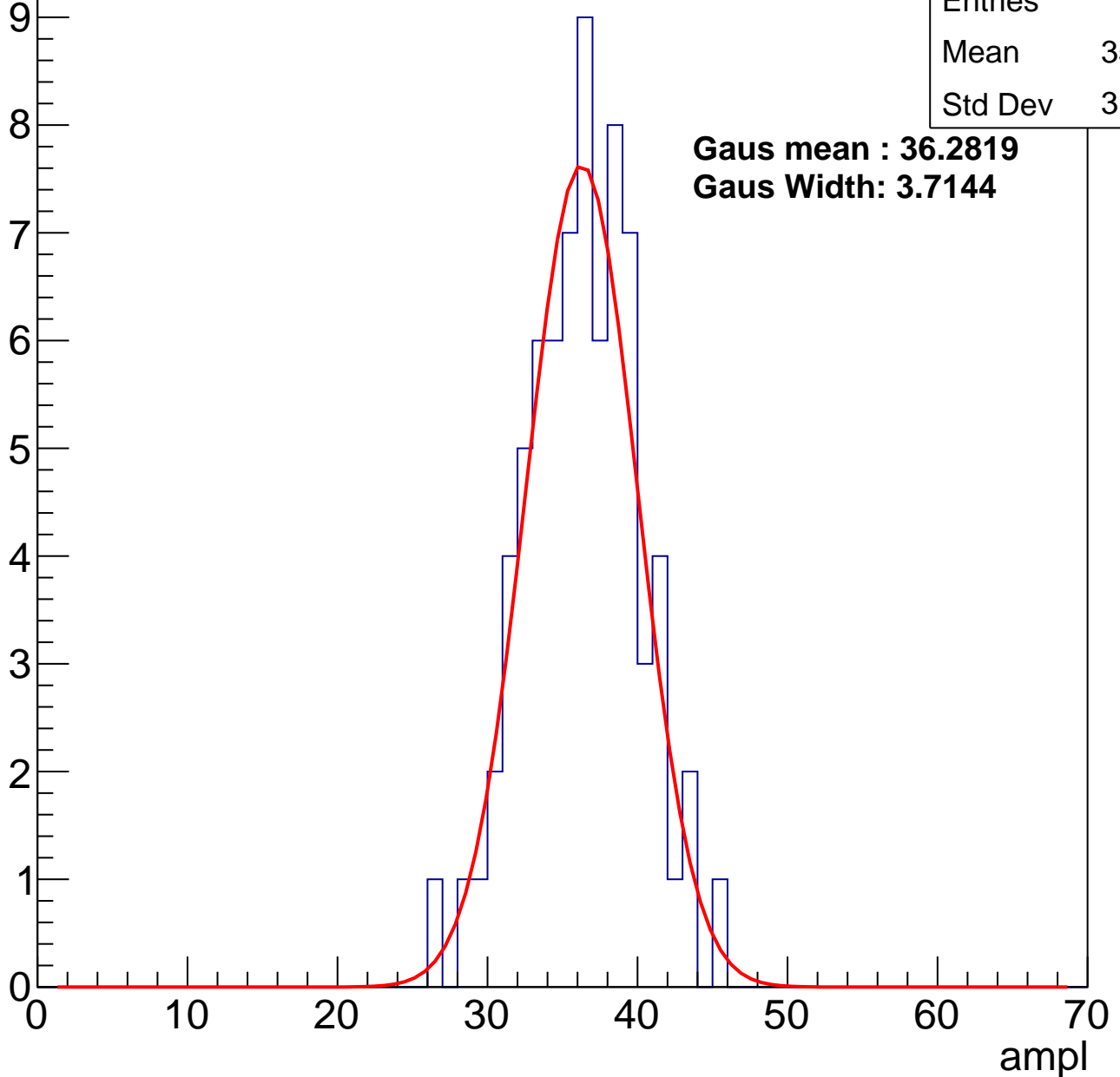
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	74
Mean	35.86
Std Dev	3.699

**Gaus mean : 36.2819**

**Gaus Width: 3.7144**



# B1L100S, U6-ch105, adc2

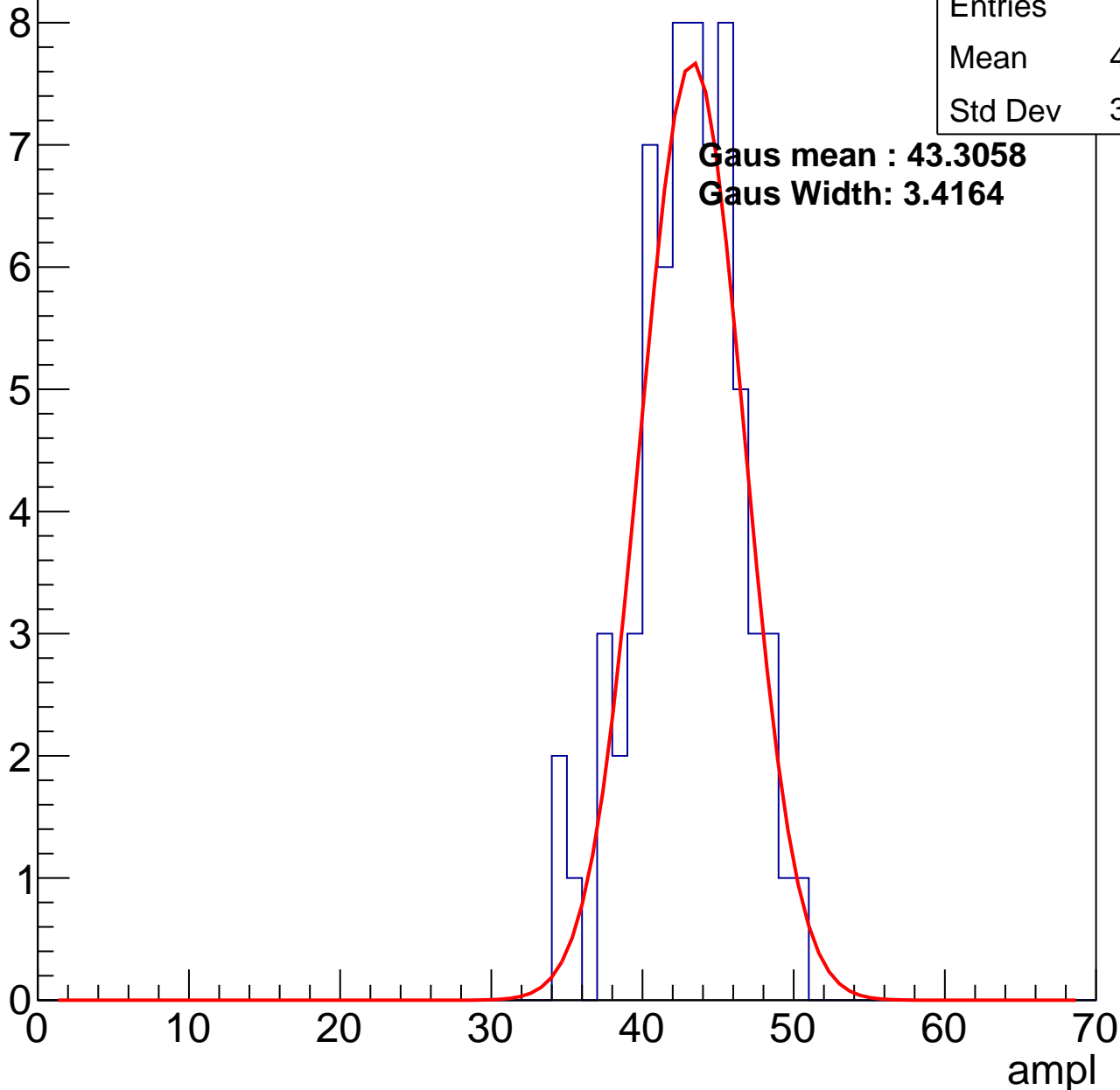
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	68
Mean	42.57
Std Dev	3.444

**Gaus mean : 43.3058**

**Gaus Width: 3.4164**

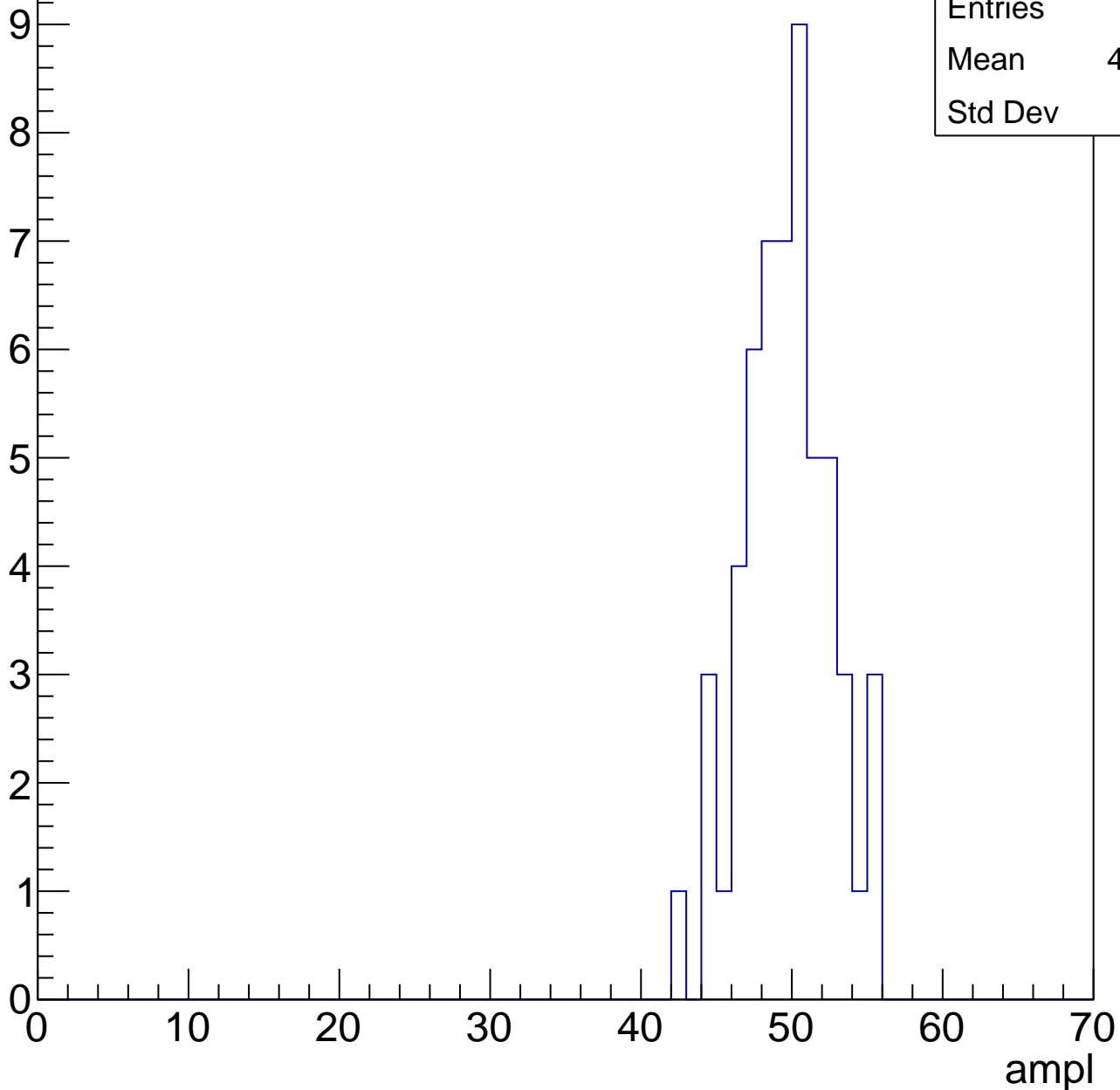


# B1L100S, U6-ch105, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

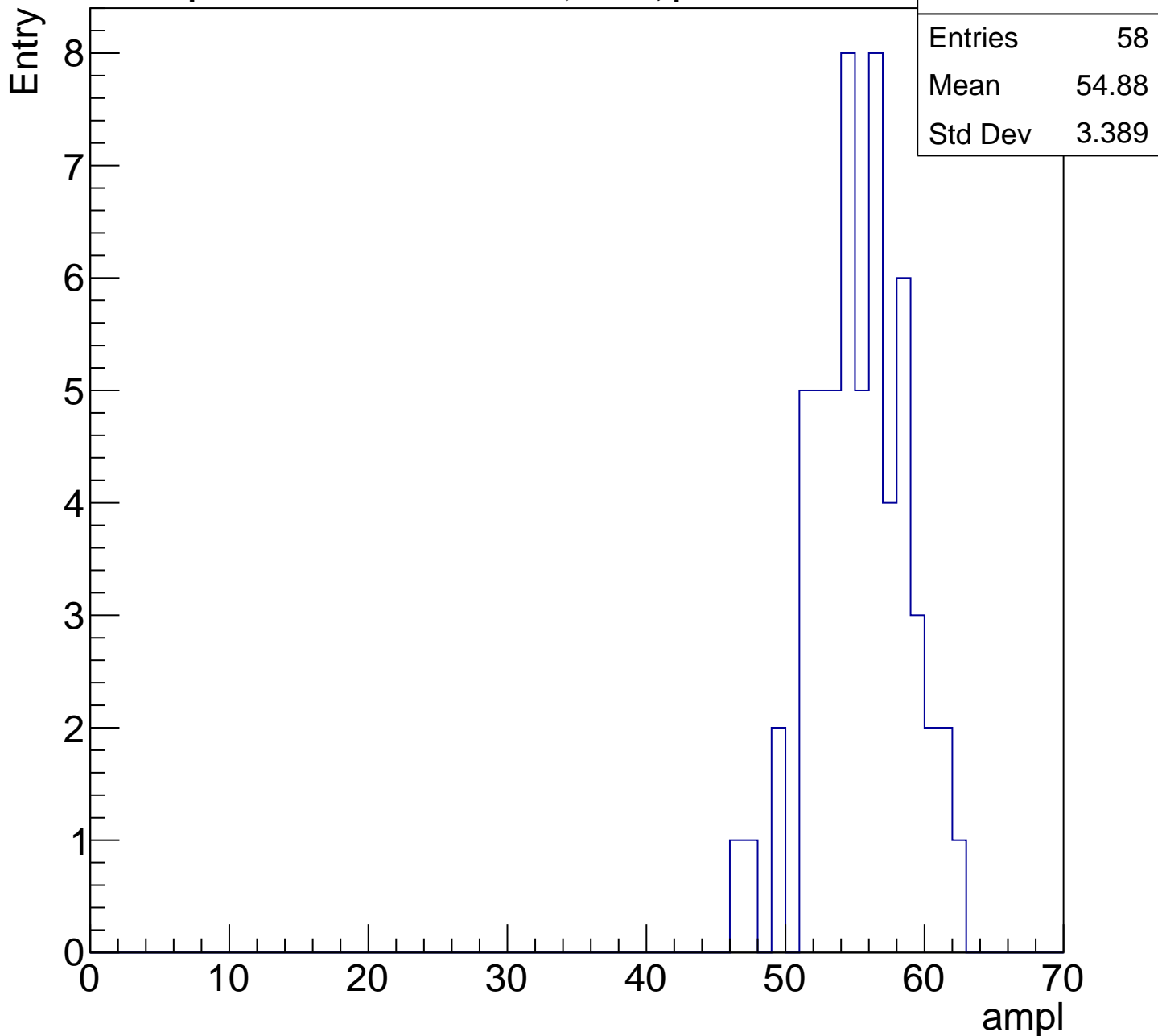
Entry

Entries	55
Mean	49.22
Std Dev	2.89



# B1L100S, U6-ch105, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2



# B1L100S, U6-ch105, adc5

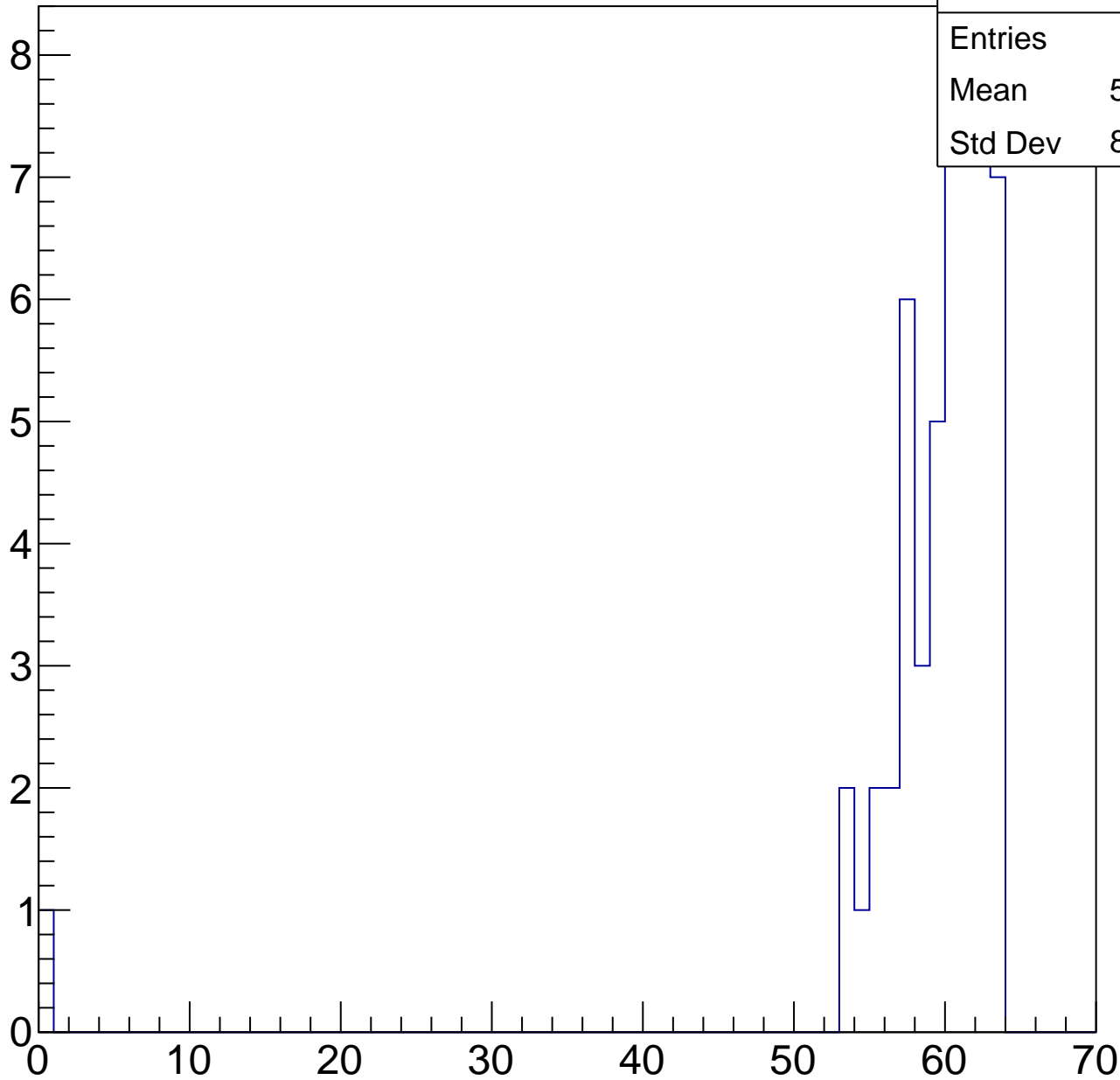
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	53
Mean	58.45
Std Dev	8.538

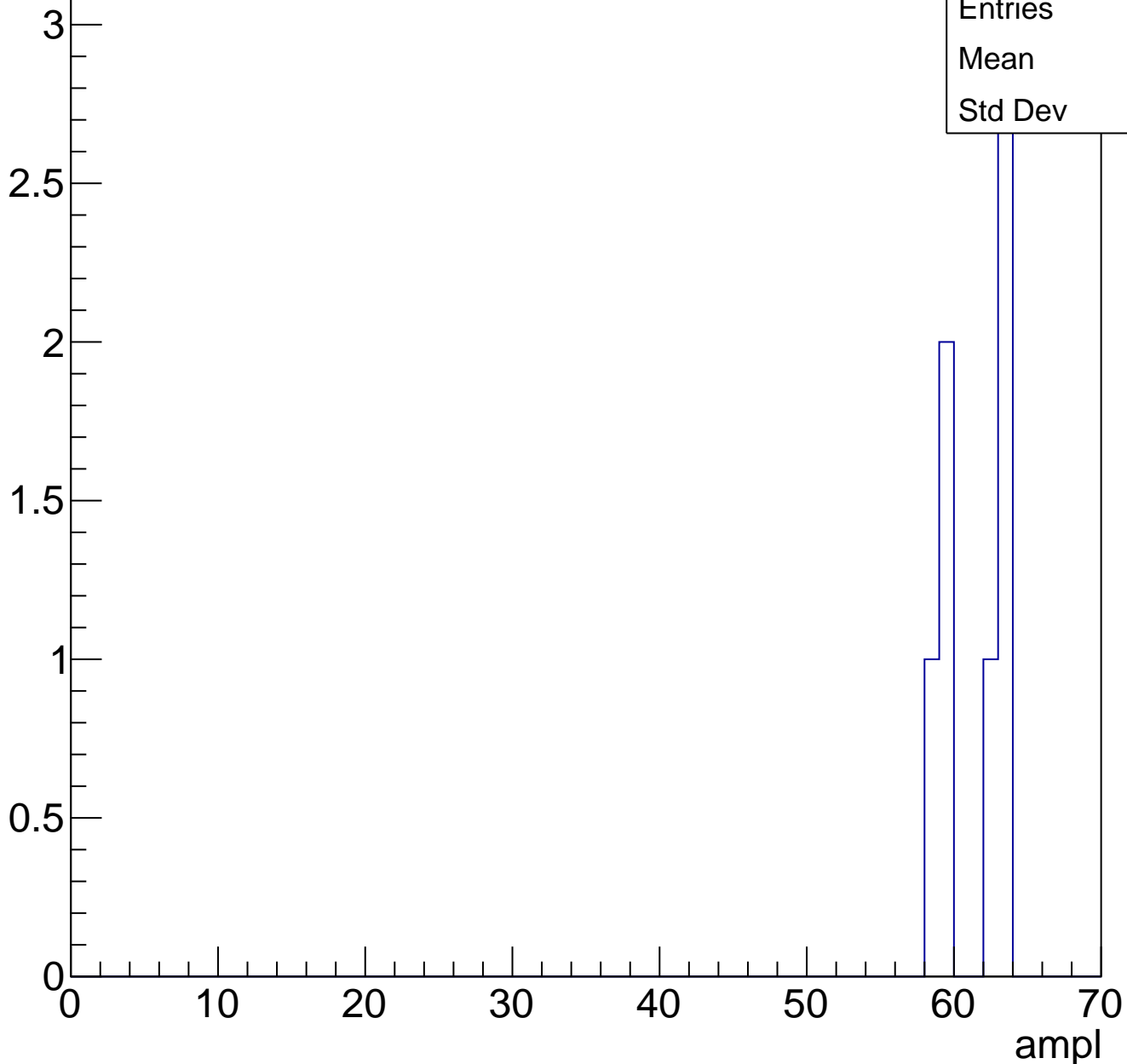
ampl



# B1L100S, U6-ch105, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry





# B1L100S, U6-ch105, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L100S, U6-ch106, adc0

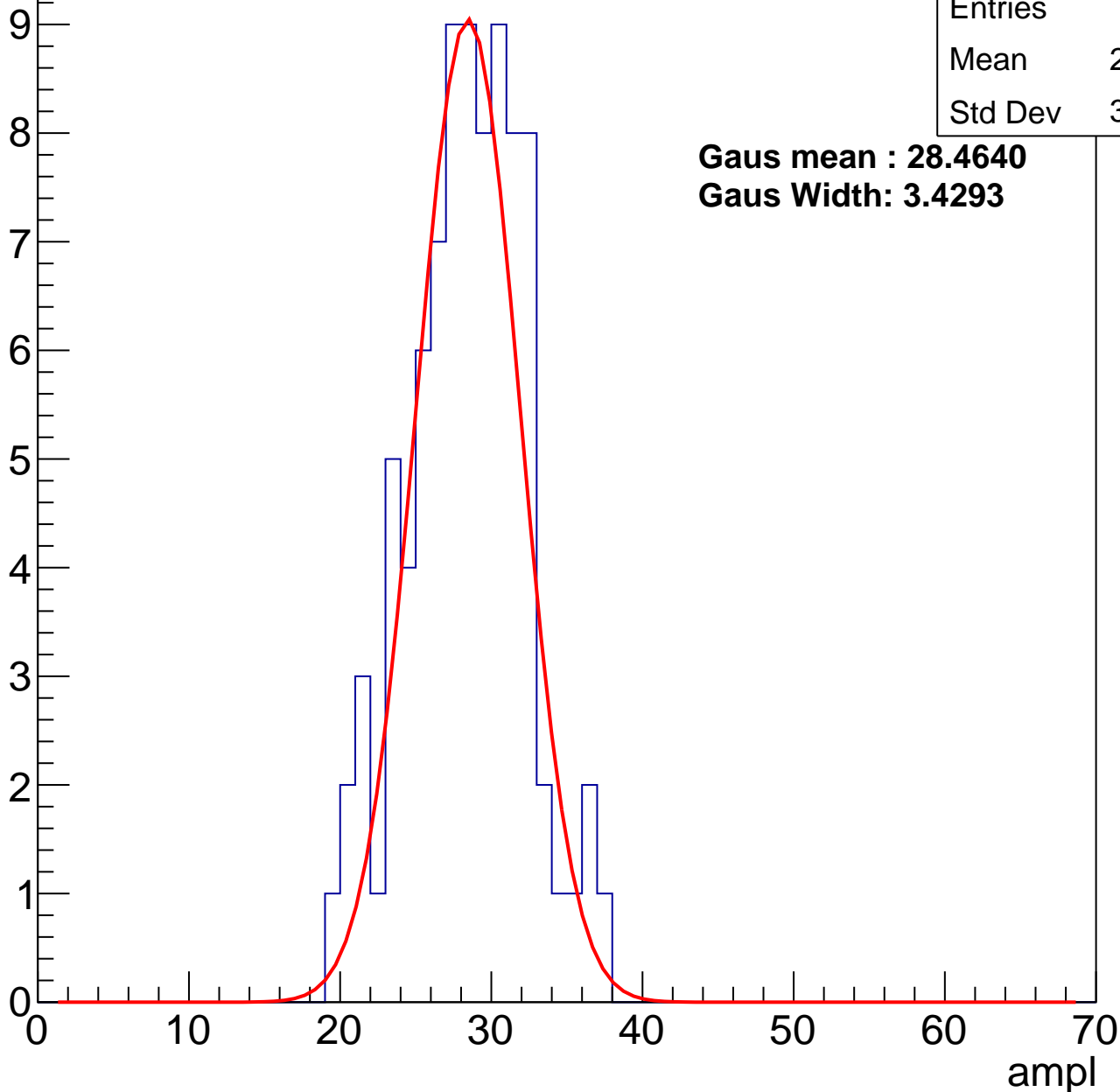
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	87
Mean	27.95
Std Dev	3.805

**Gaus mean : 28.4640**

**Gaus Width: 3.4293**



# B1L100S, U6-ch106, adc1

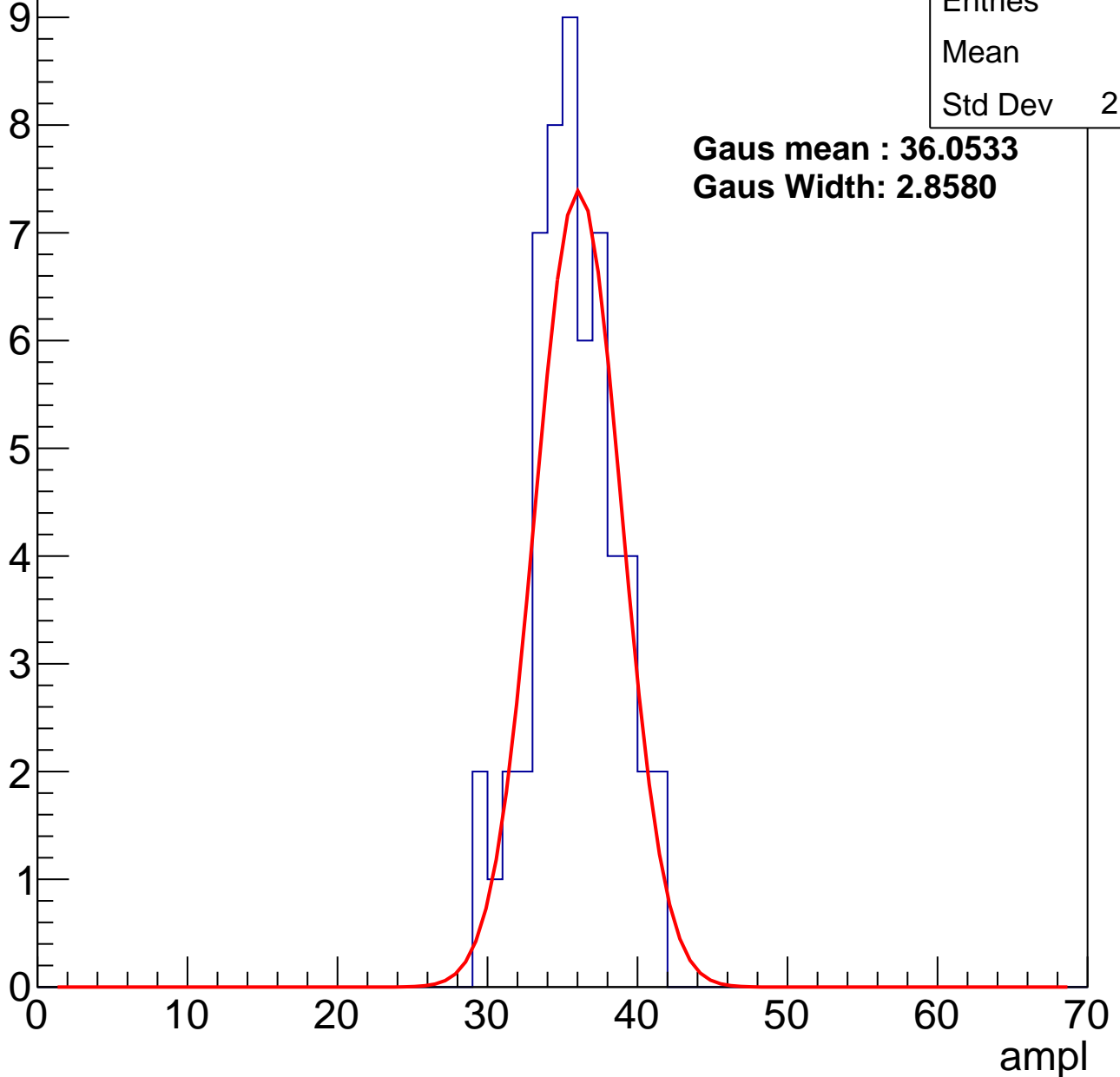
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	56
Mean	35.3
Std Dev	2.783

**Gaus mean : 36.0533**

**Gaus Width: 2.8580**



# B1L100S, U6-ch106, adc2

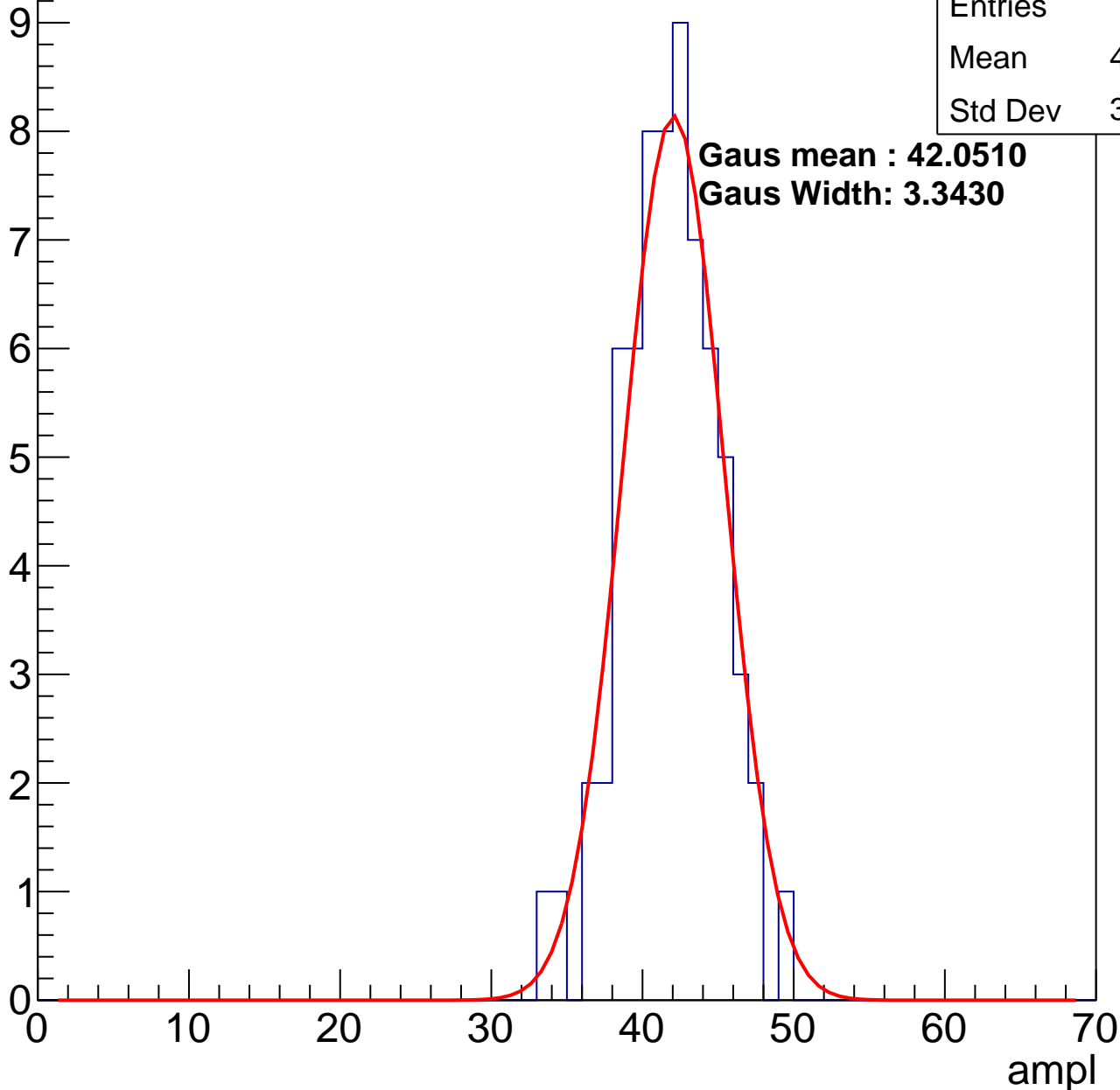
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	67
Mean	41.37
Std Dev	3.124

**Gaus mean : 42.0510**

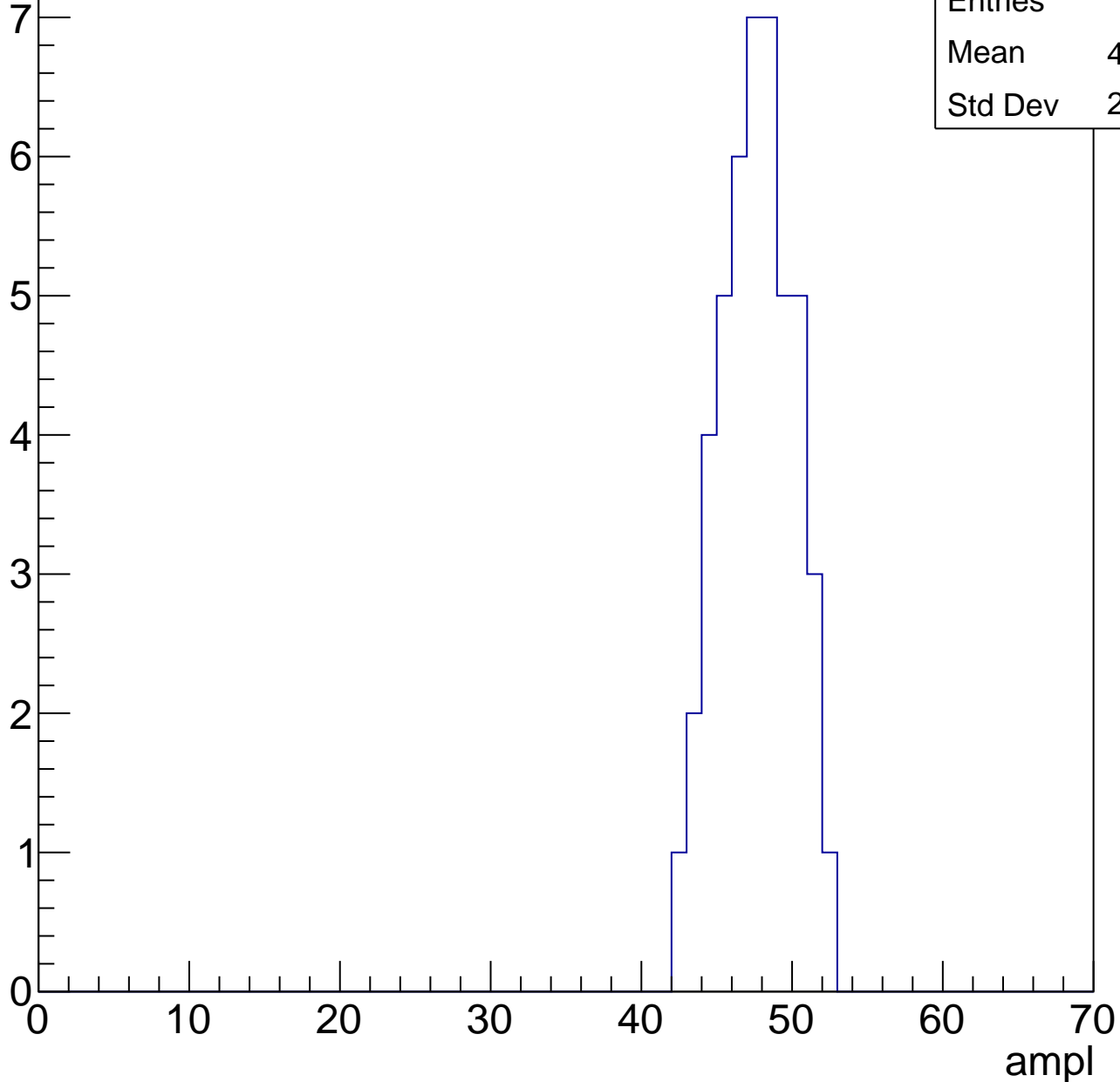
**Gaus Width: 3.3430**



# B1L100S, U6-ch106, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



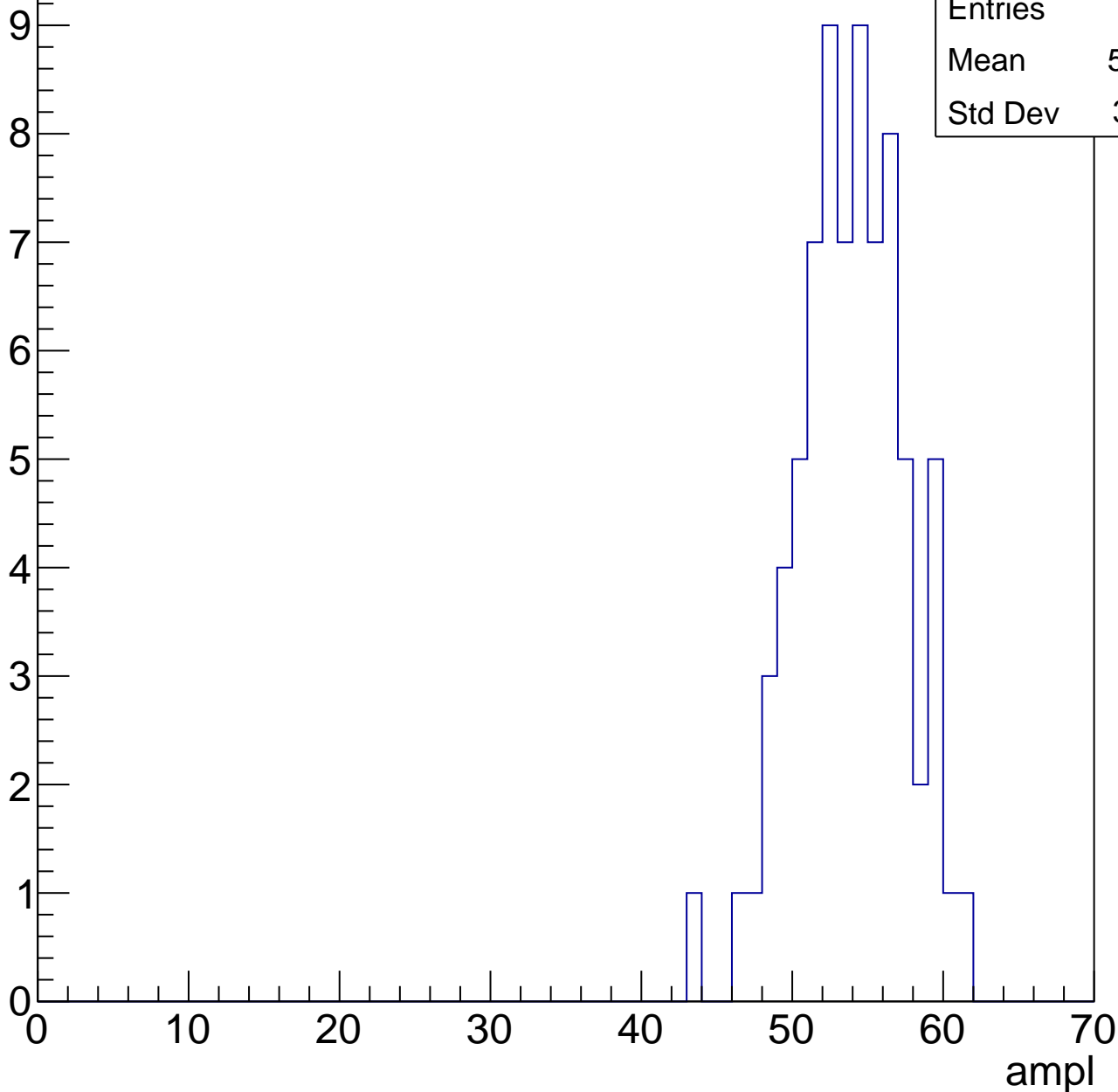
Entries	46
Mean	47.17
Std Dev	2.389

# B1L100S, U6-ch106, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

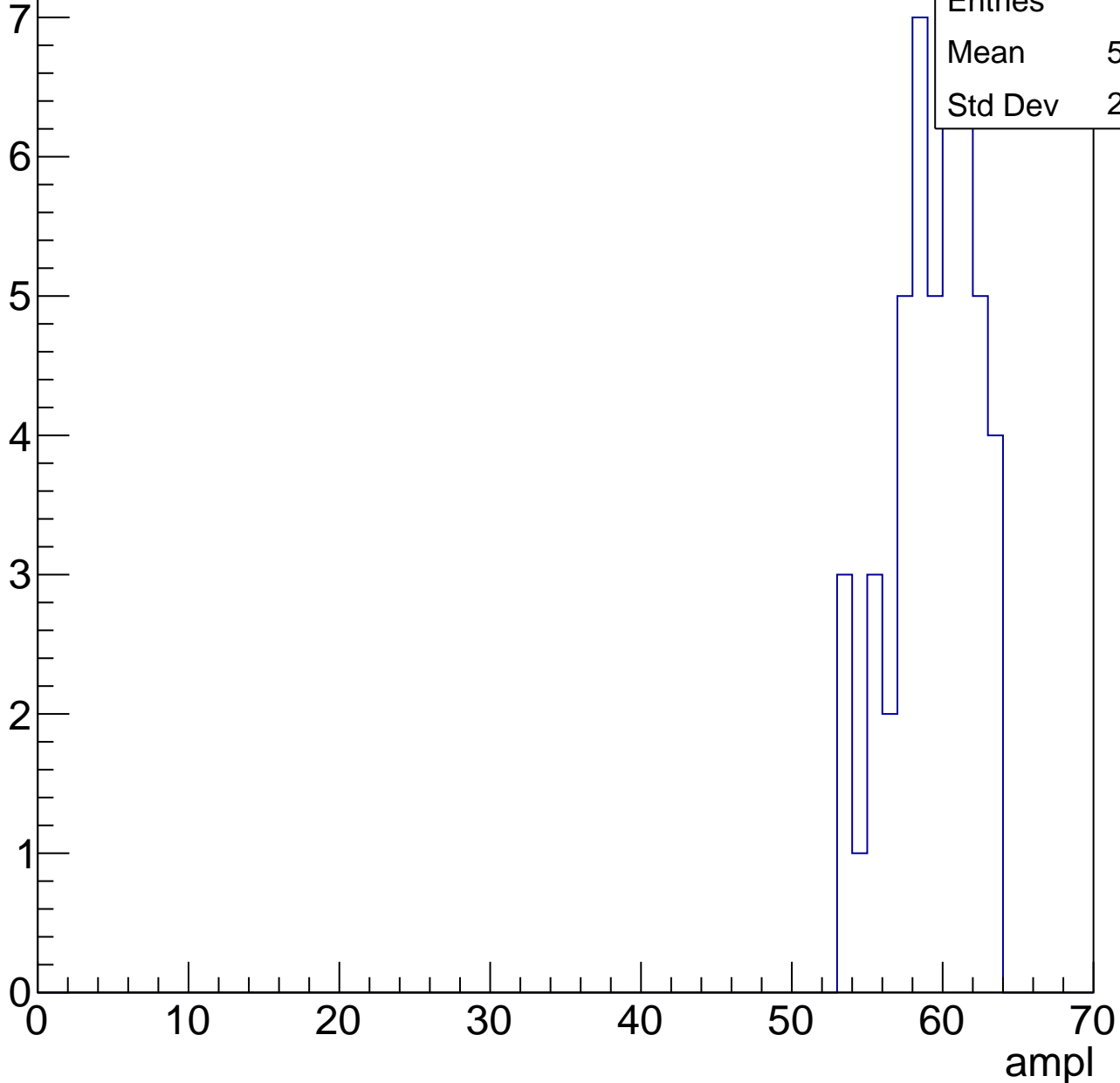
Entries	76
Mean	53.39
Std Dev	3.491



# B1L100S, U6-ch106, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

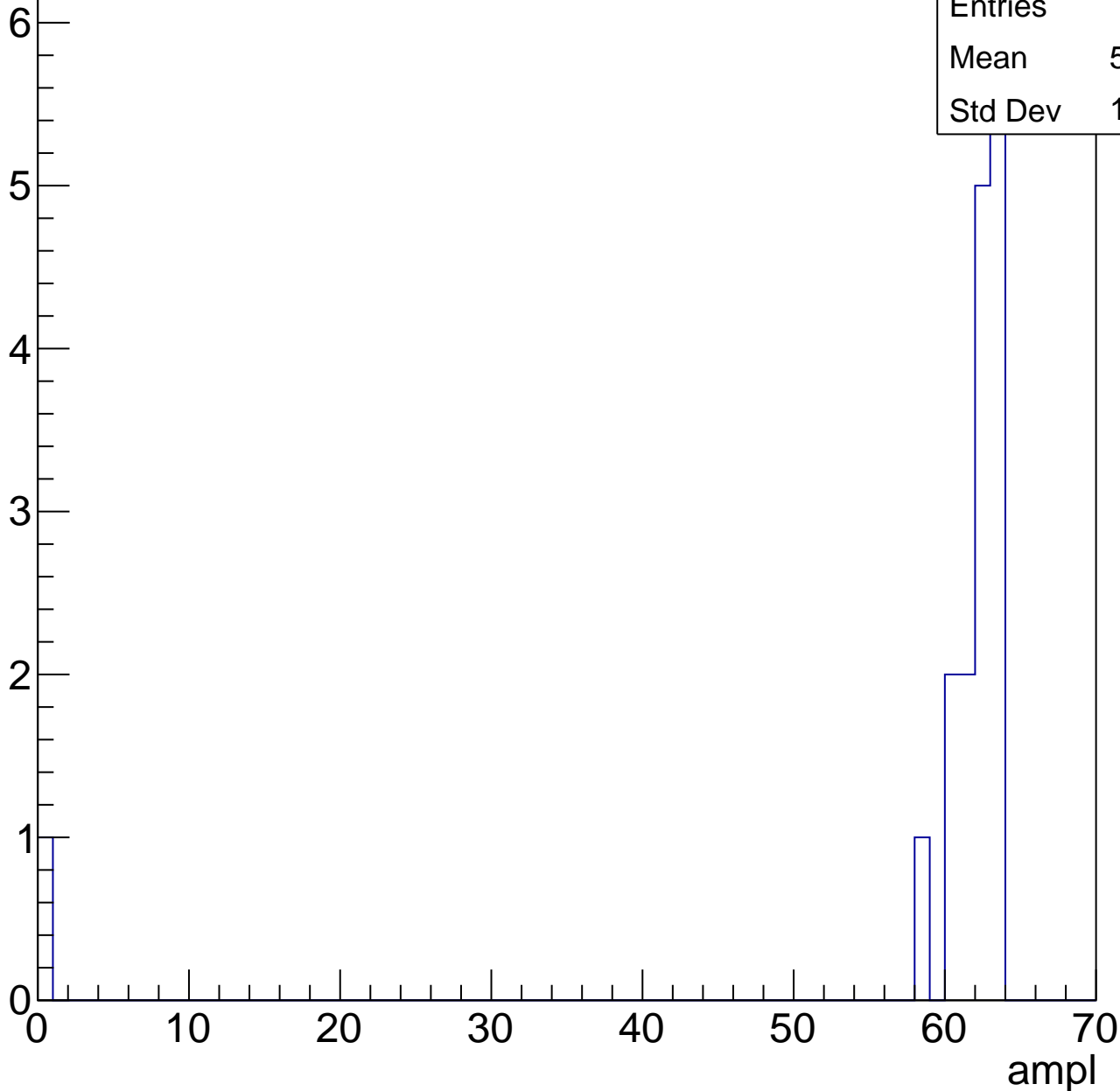


# B1L100S, U6-ch106, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	17
Mean	58.12
Std Dev	14.59





# B1L100S, U6-ch106, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L100S, U6-ch107, adc0

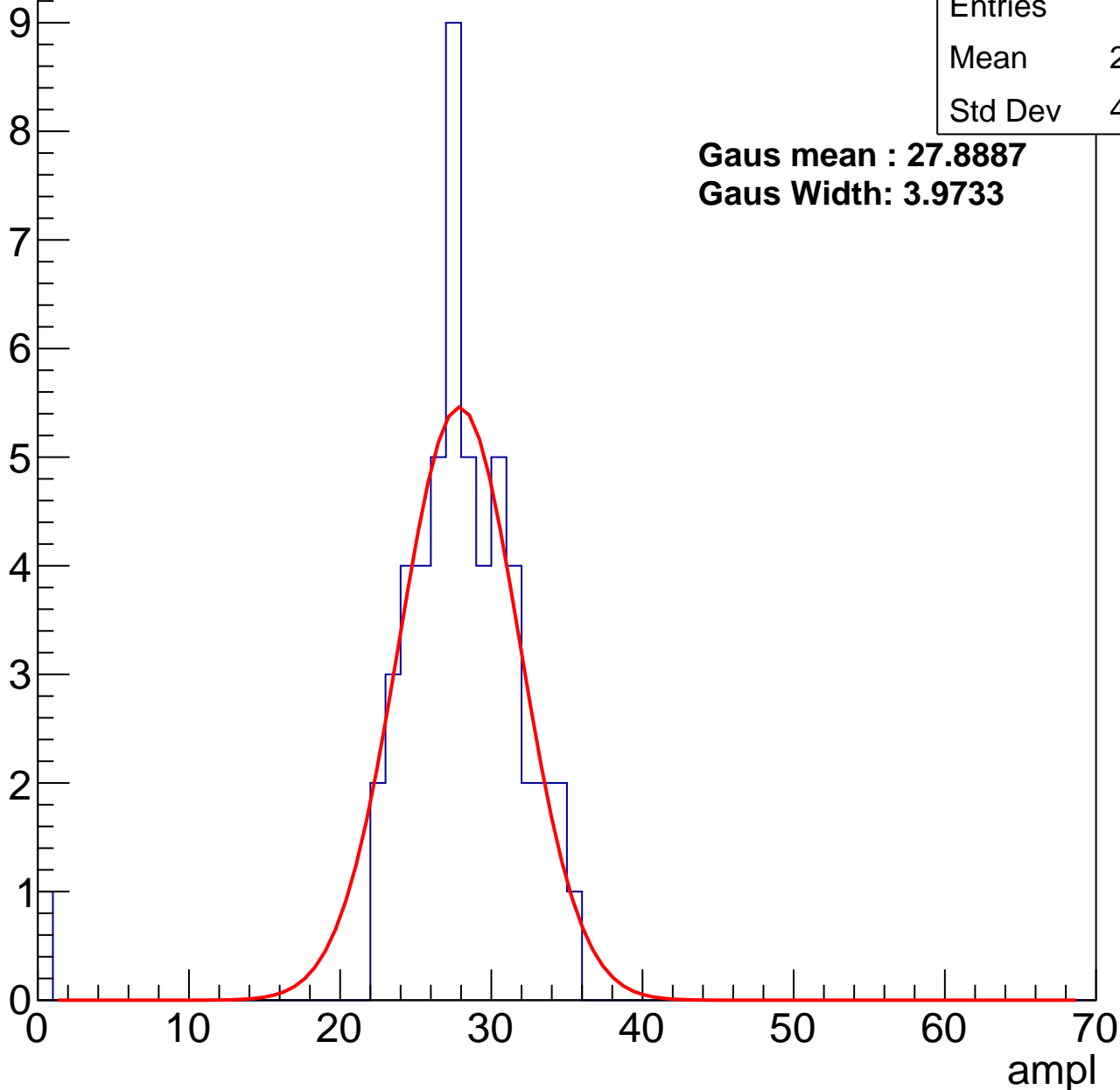
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	53
Mean	27.26
Std Dev	4.942

**Gaus mean : 27.8887**

**Gaus Width: 3.9733**



# B1L100S, U6-ch107, adc1

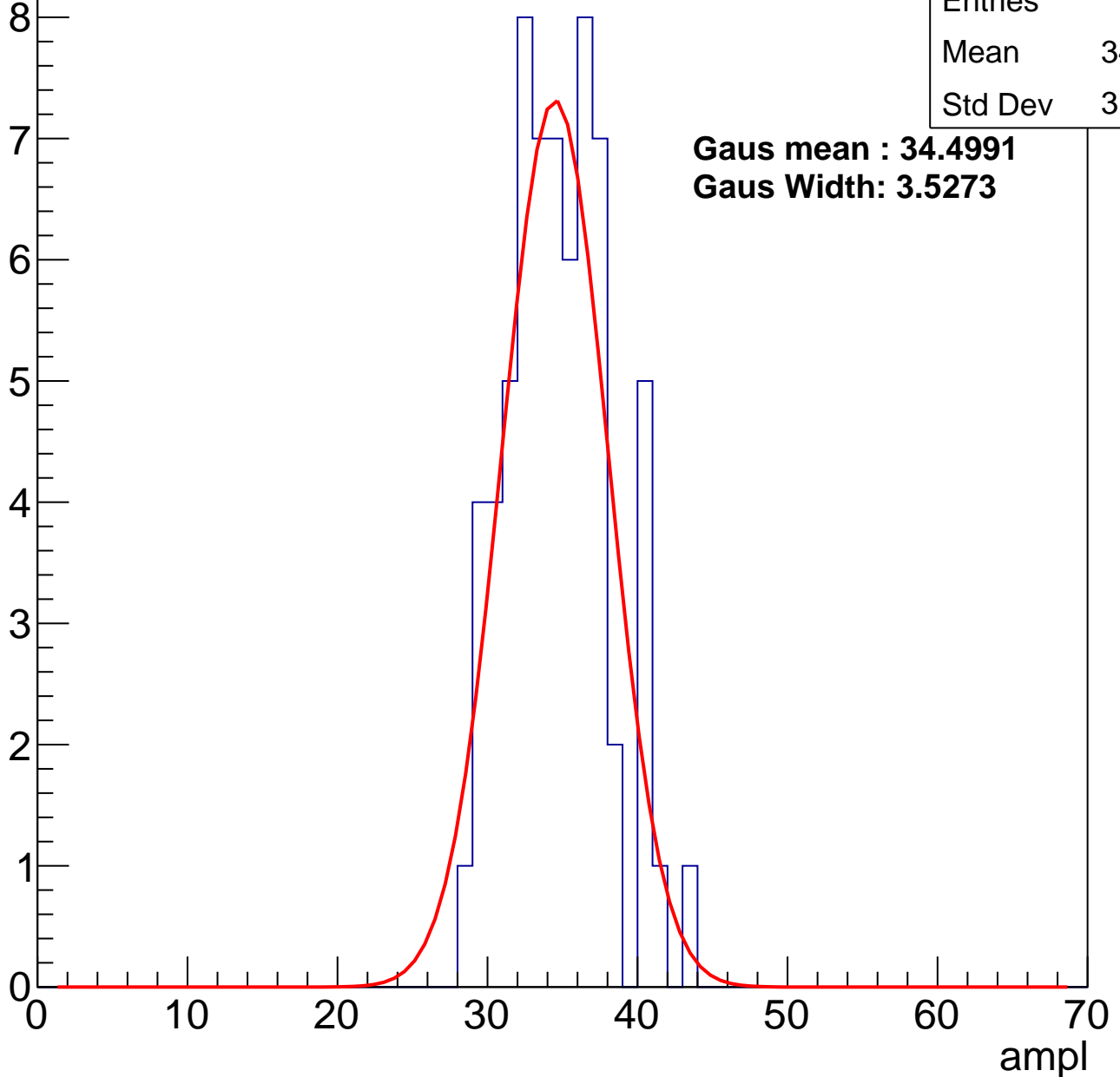
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	66
Mean	34.26
Std Dev	3.309

**Gaus mean : 34.4991**

**Gaus Width: 3.5273**



# B1L100S, U6-ch107, adc2

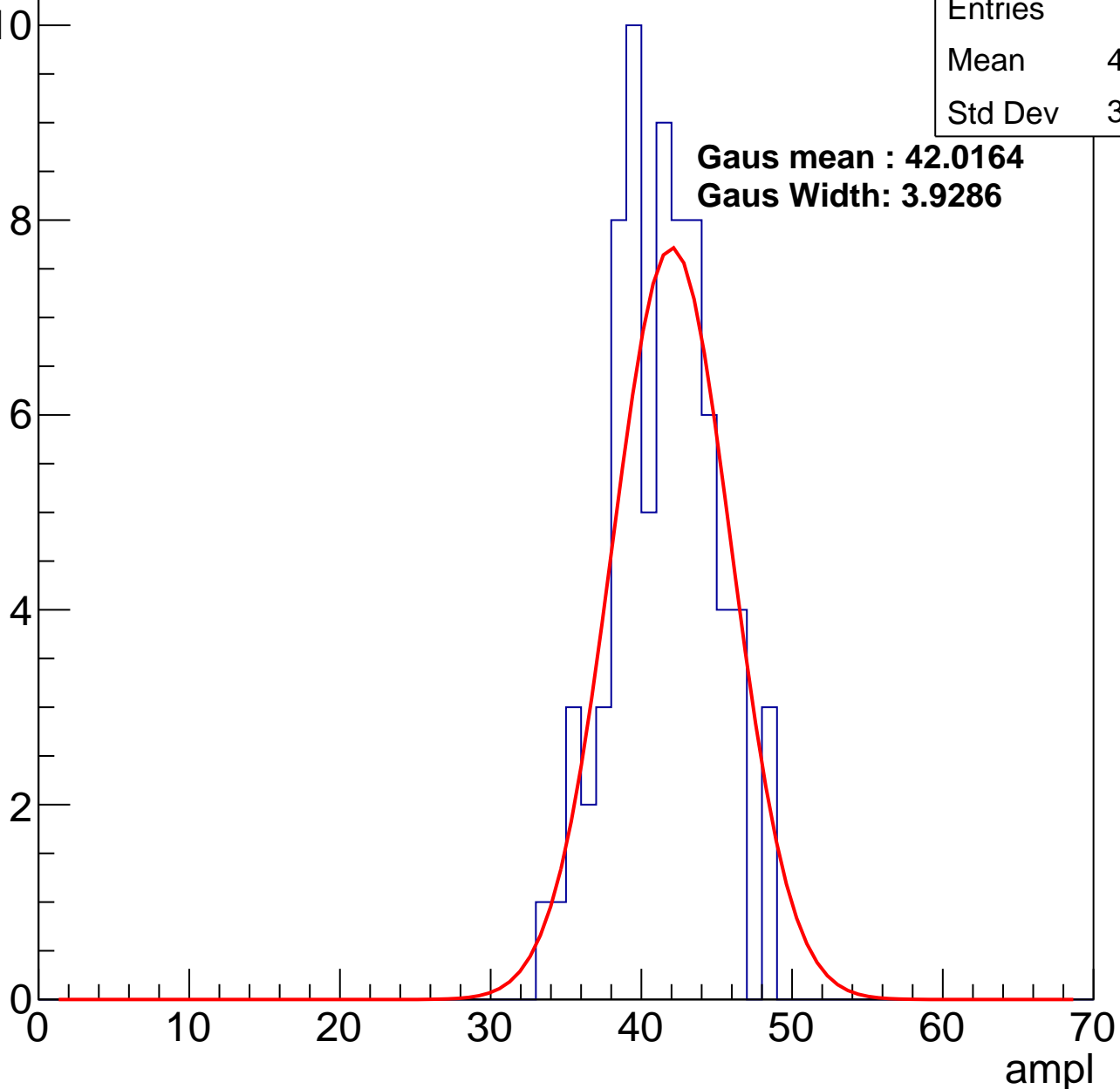
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	75
Mean	40.93
Std Dev	3.348

**Gaus mean : 42.0164**

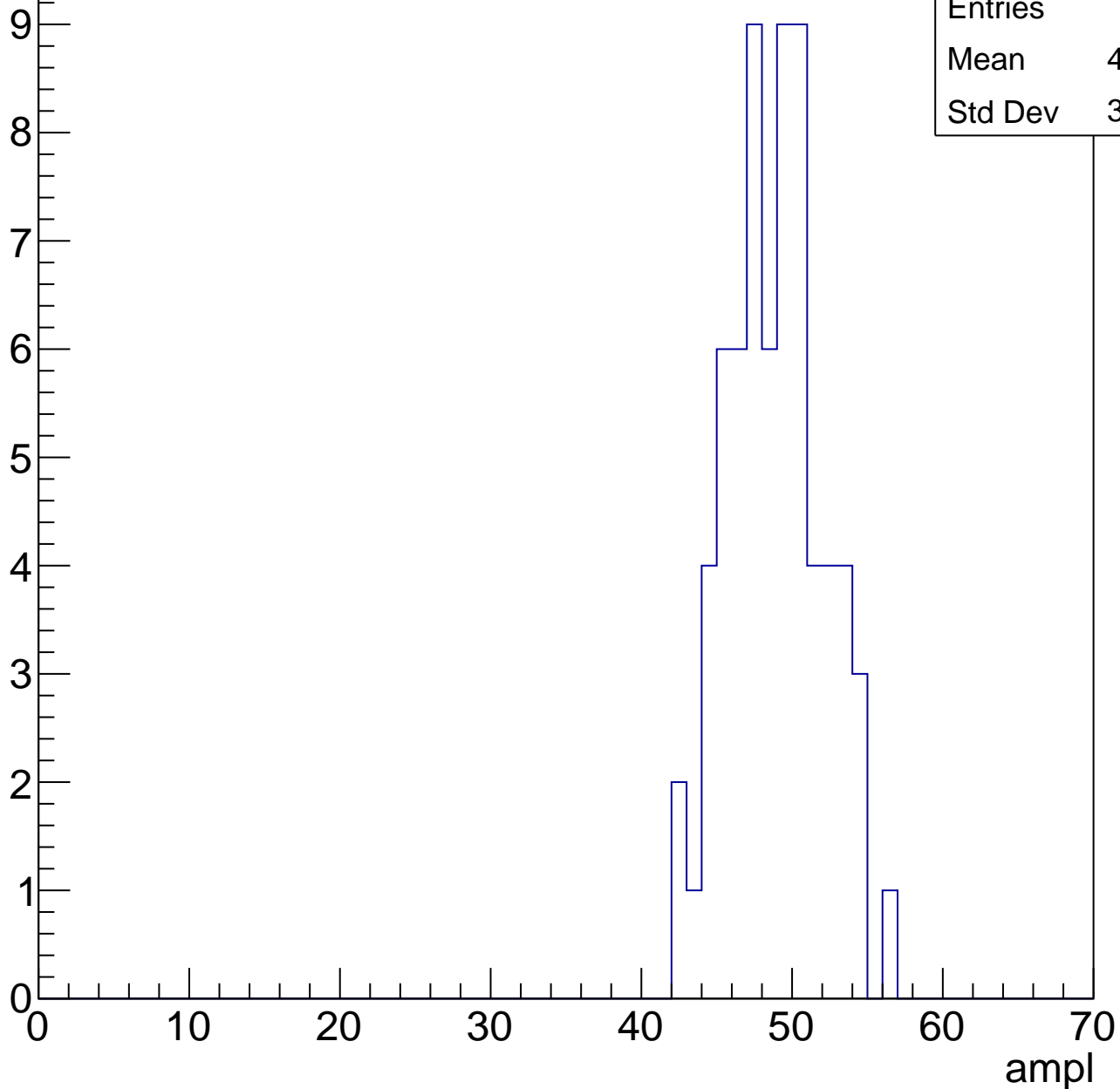
**Gaus Width: 3.9286**



# B1L100S, U6-ch107, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



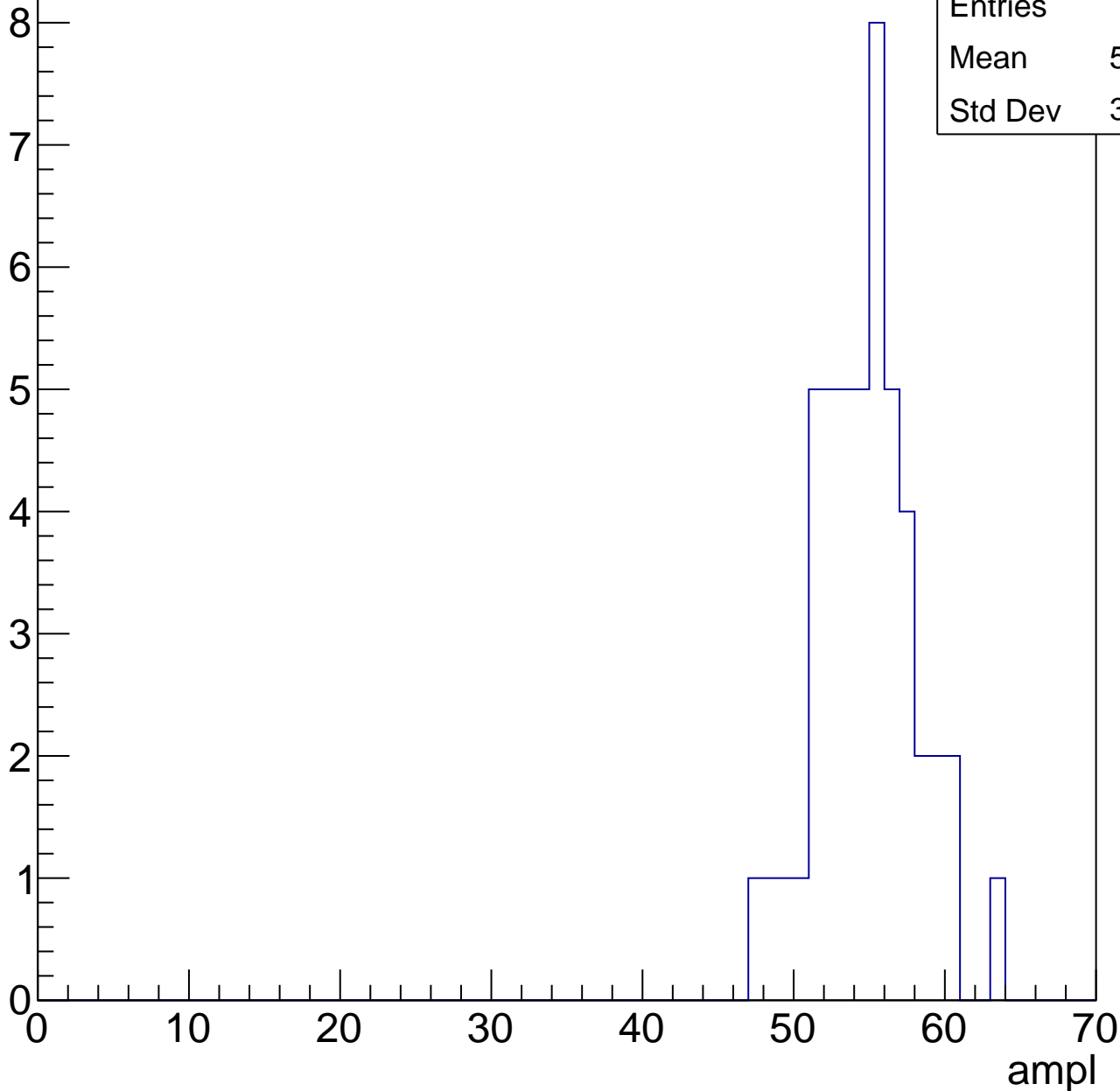
Entries	68
Mean	48.43
Std Dev	3.098

# B1L100S, U6-ch107, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

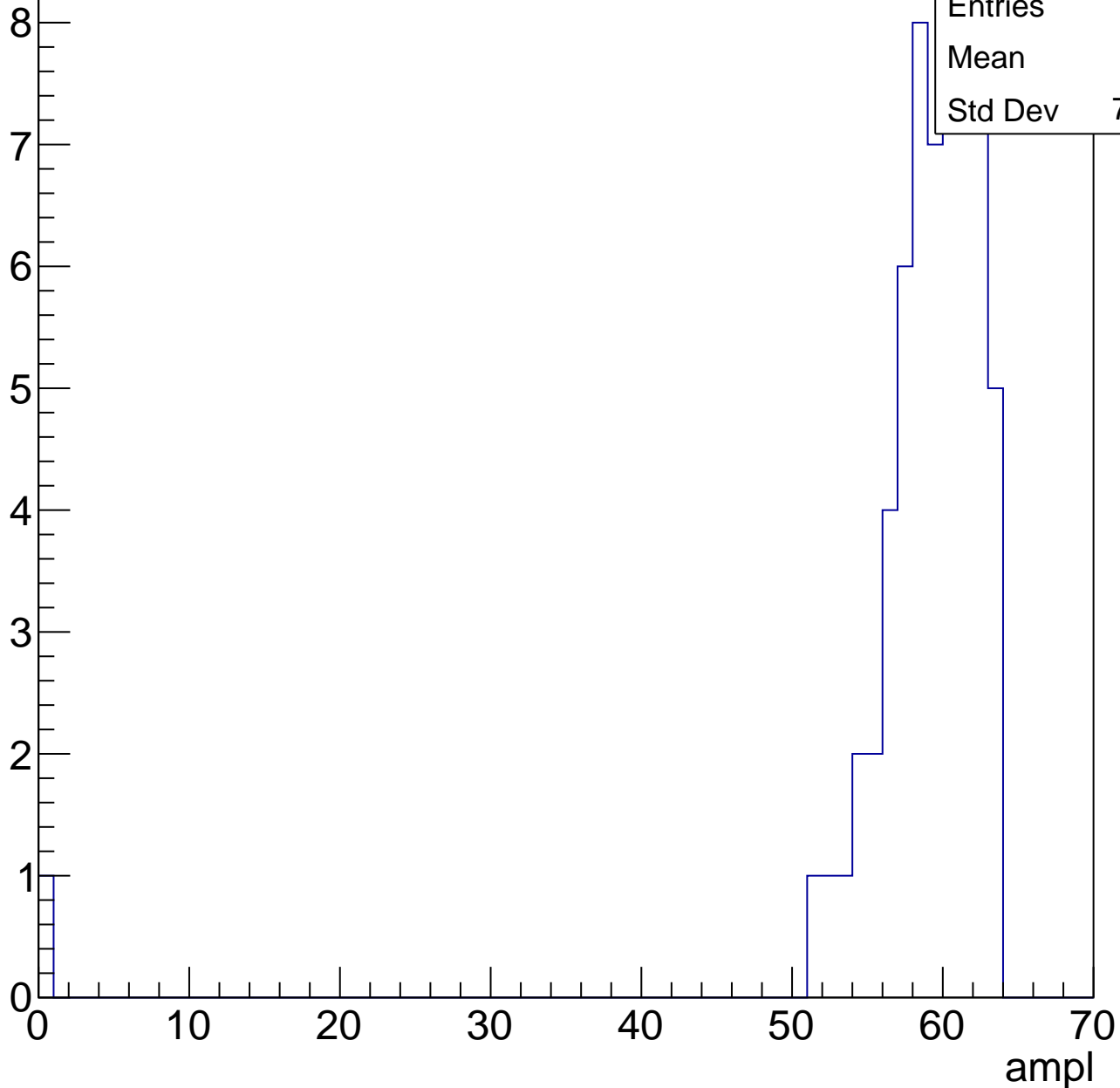
Entries	48
Mean	54.35
Std Dev	3.192



# B1L100S, U6-ch107, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

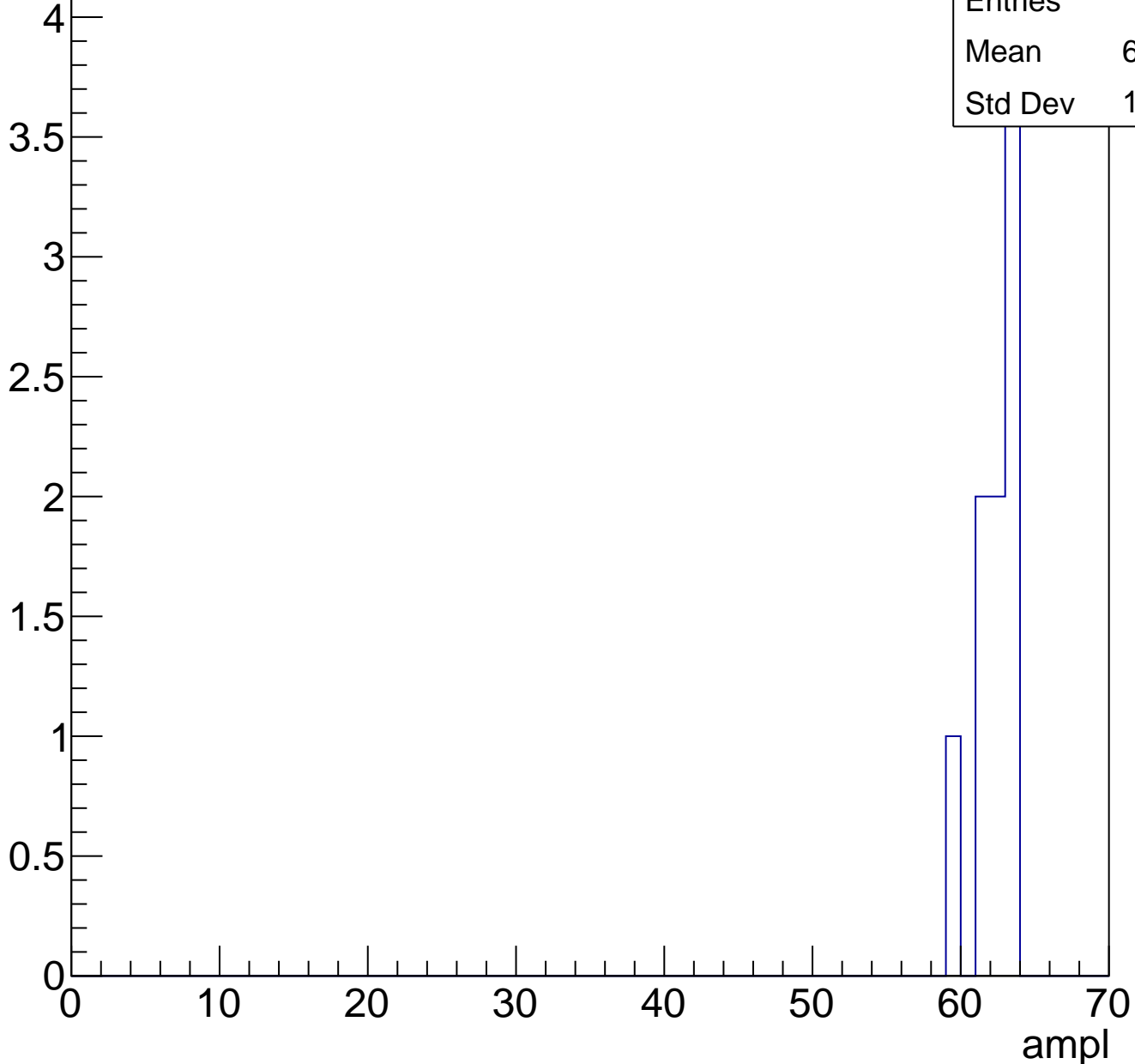
Entry



# B1L100S, U6-ch107, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry





# B1L100S, U6-ch107, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L100S, U6-ch108, adc0

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	89
Mean	29.53
Std Dev	4.929

**Gaus mean : 30.8558**

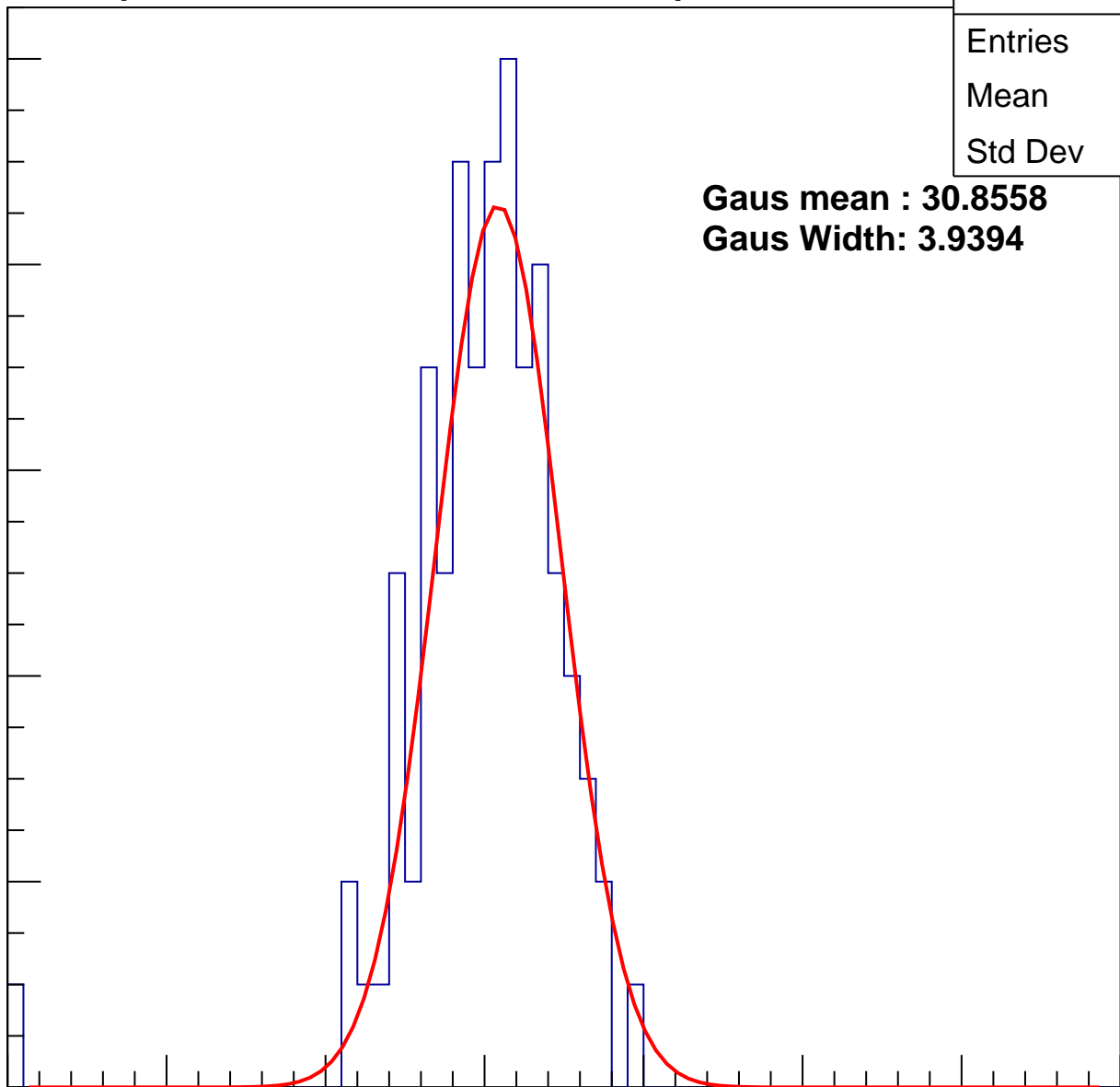
**Gaus Width: 3.9394**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L100S, U6-ch108, adc1

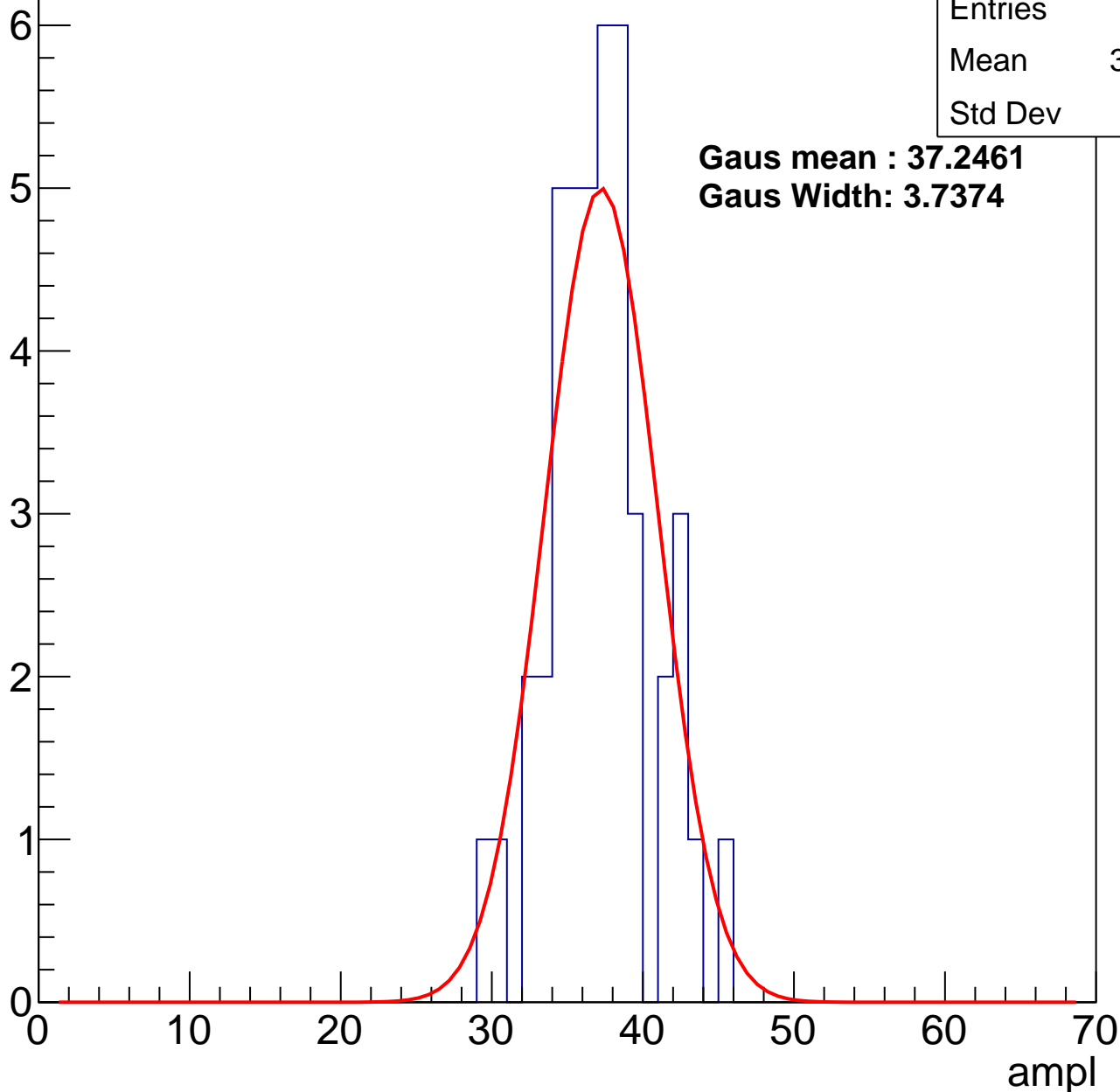
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	43
Mean	36.67
Std Dev	3.36

**Gaus mean : 37.2461**

**Gaus Width: 3.7374**



# B1L100S, U6-ch108, adc2

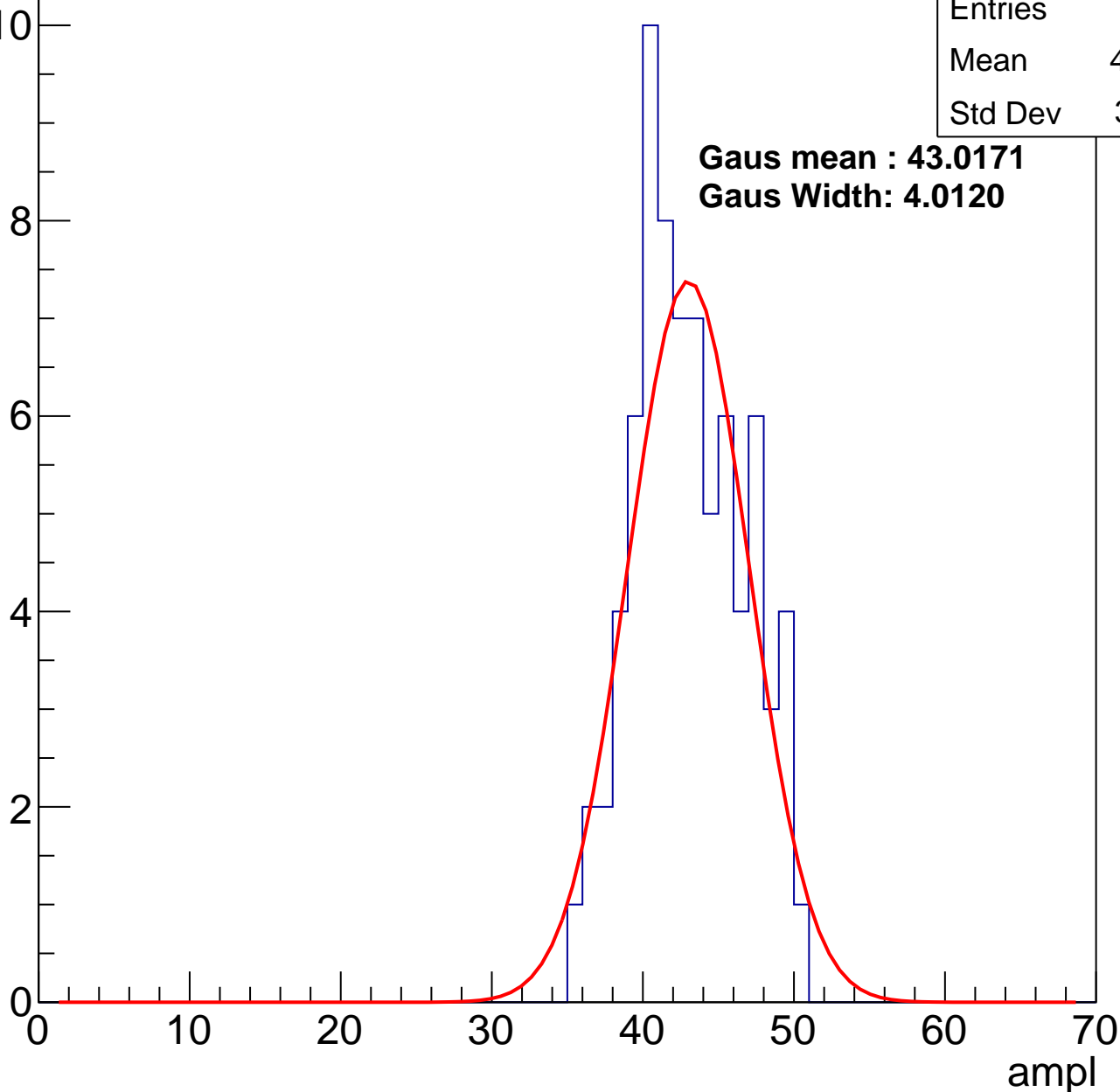
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	76
Mean	42.58
Std Dev	3.581

**Gaus mean : 43.0171**

**Gaus Width: 4.0120**

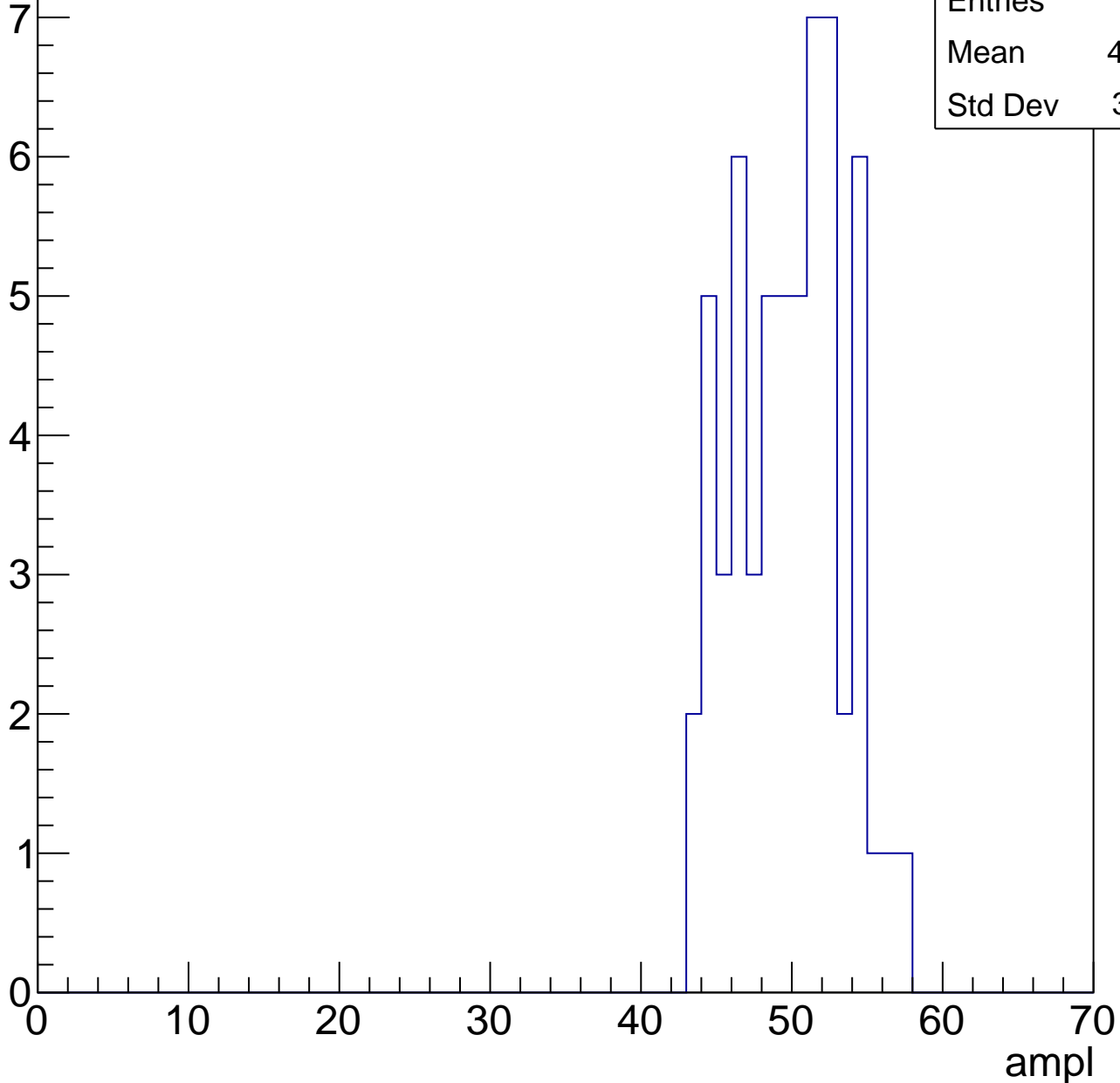


# B1L100S, U6-ch108, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	59
Mean	49.36
Std Dev	3.531

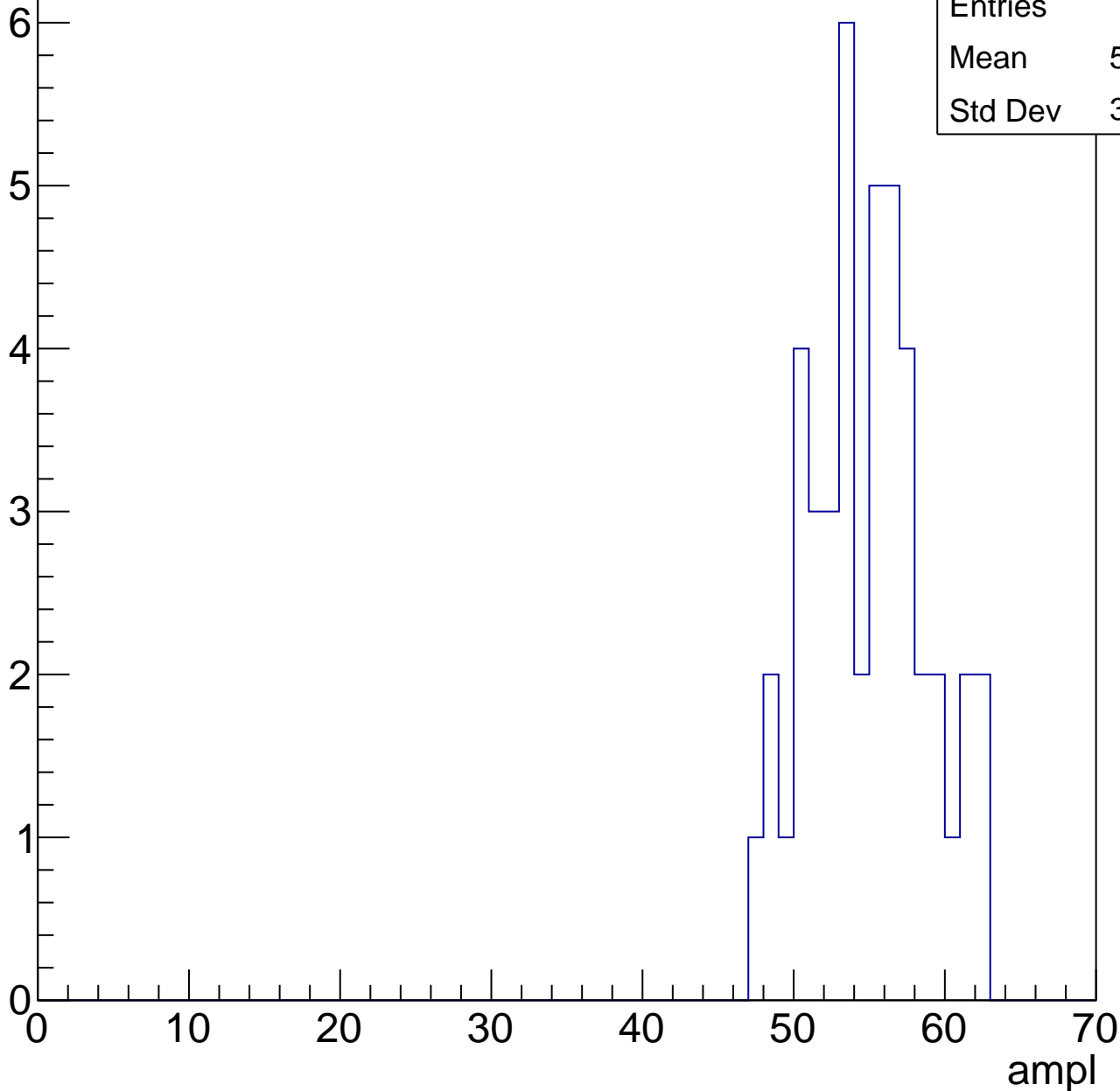


# B1L100S, U6-ch108, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	45
Mean	54.44
Std Dev	3.804



# B1L100S, U6-ch108, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	62
Mean	58.05
Std Dev	7.904

ampl

0

10

20

30

40

50

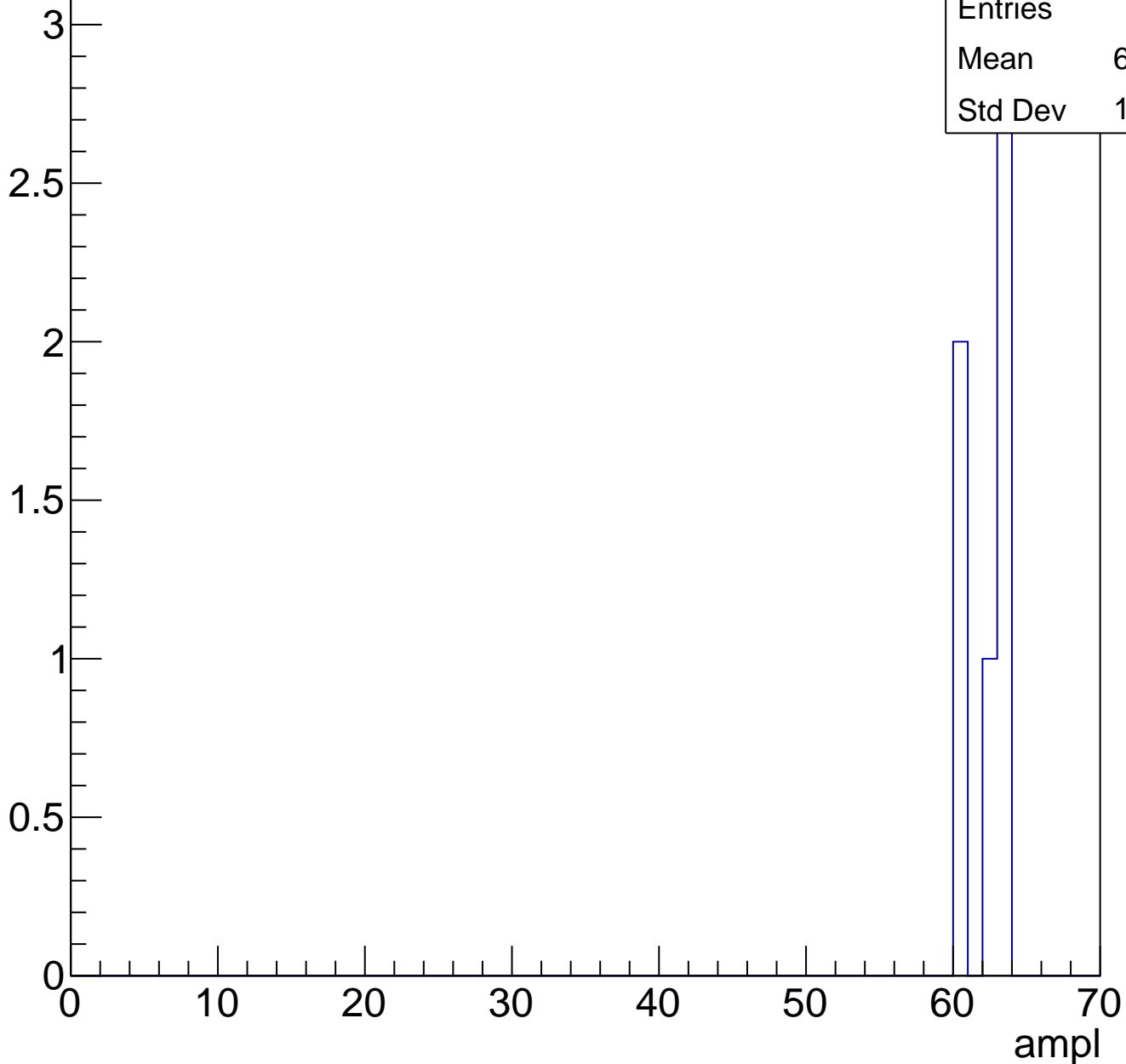
60

70

# B1L100S, U6-ch108, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry





# B1L100S, U6-ch108, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	1
Mean	63
Std Dev	0

# B1L100S, U6-ch109, adc0

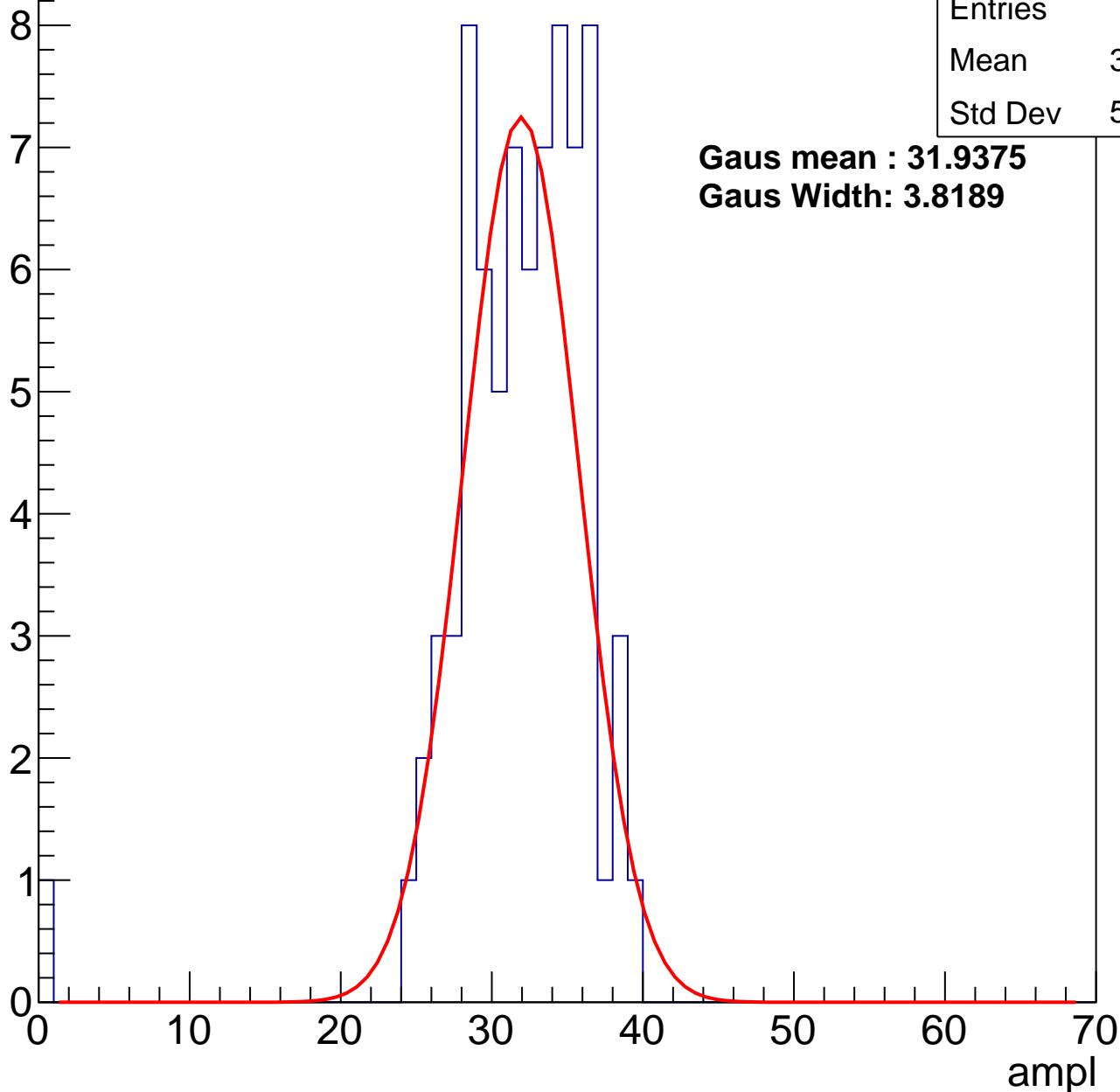
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	77
Mean	31.38
Std Dev	5.045

**Gaus mean : 31.9375**

**Gaus Width: 3.8189**



# B1L100S, U6-ch109, adc1

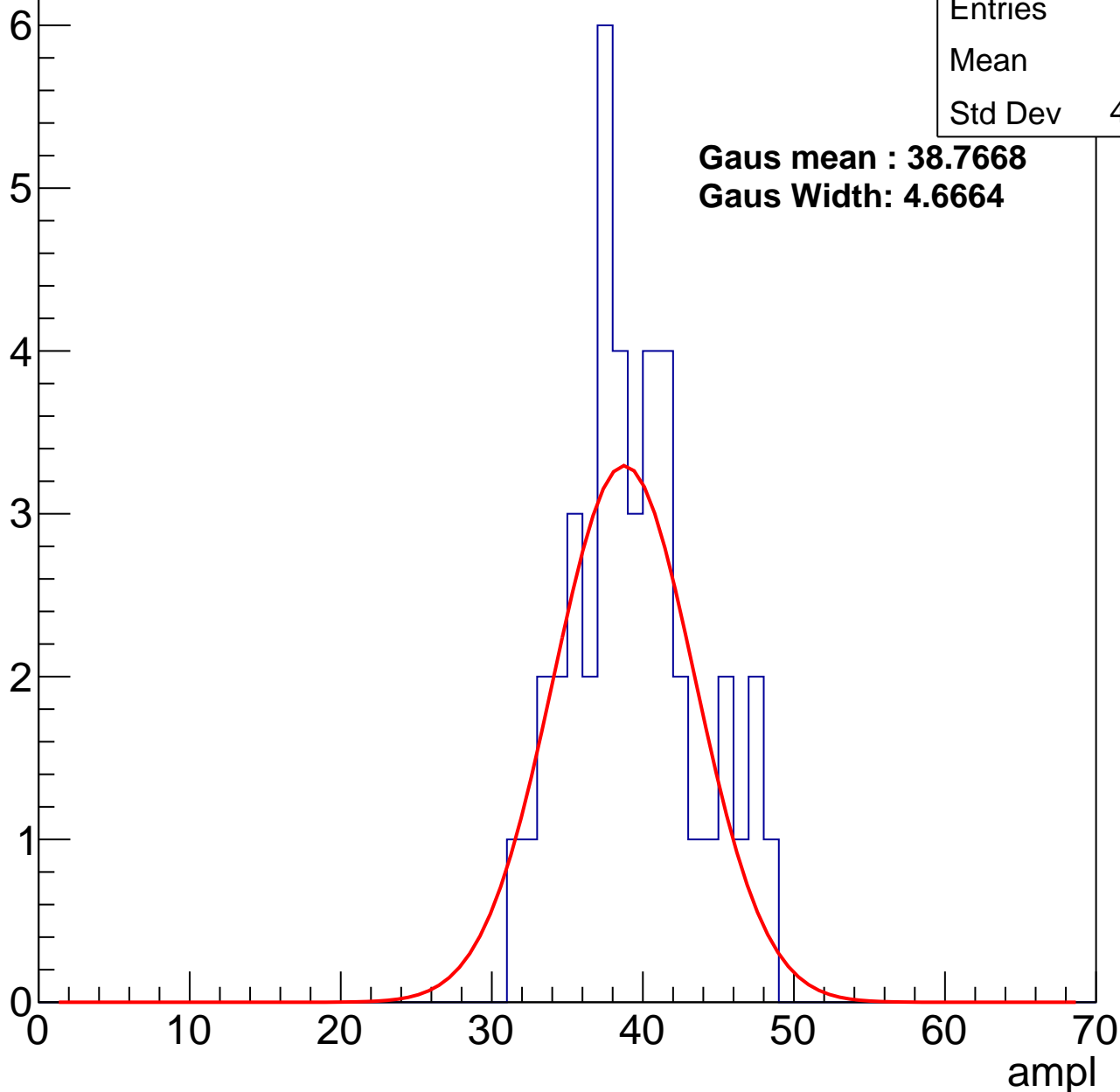
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	42
Mean	39
Std Dev	4.192

**Gaus mean : 38.7668**

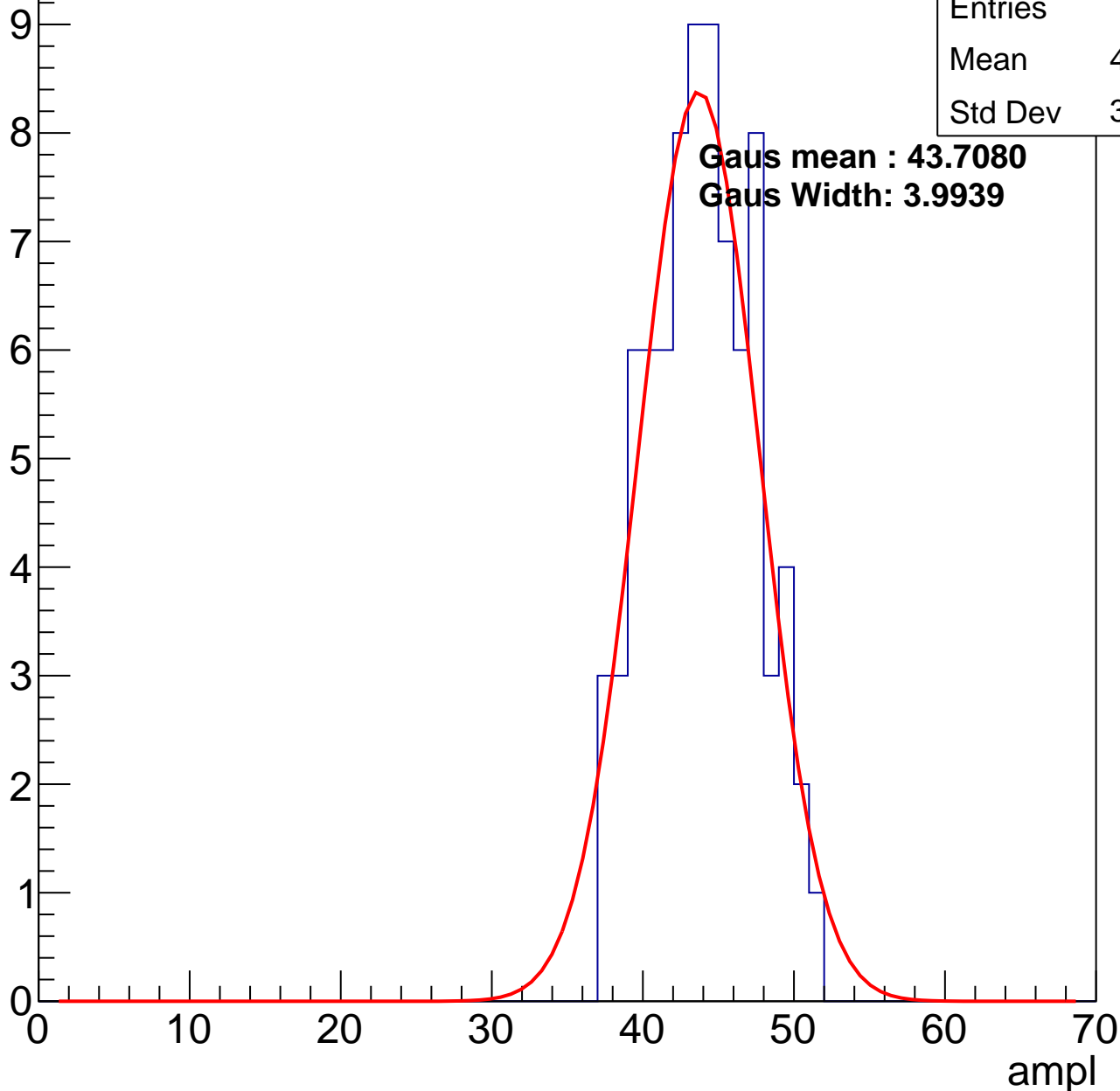
**Gaus Width: 4.6664**



# B1L100S, U6-ch109, adc2

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



# B1L100S, U6-ch109, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

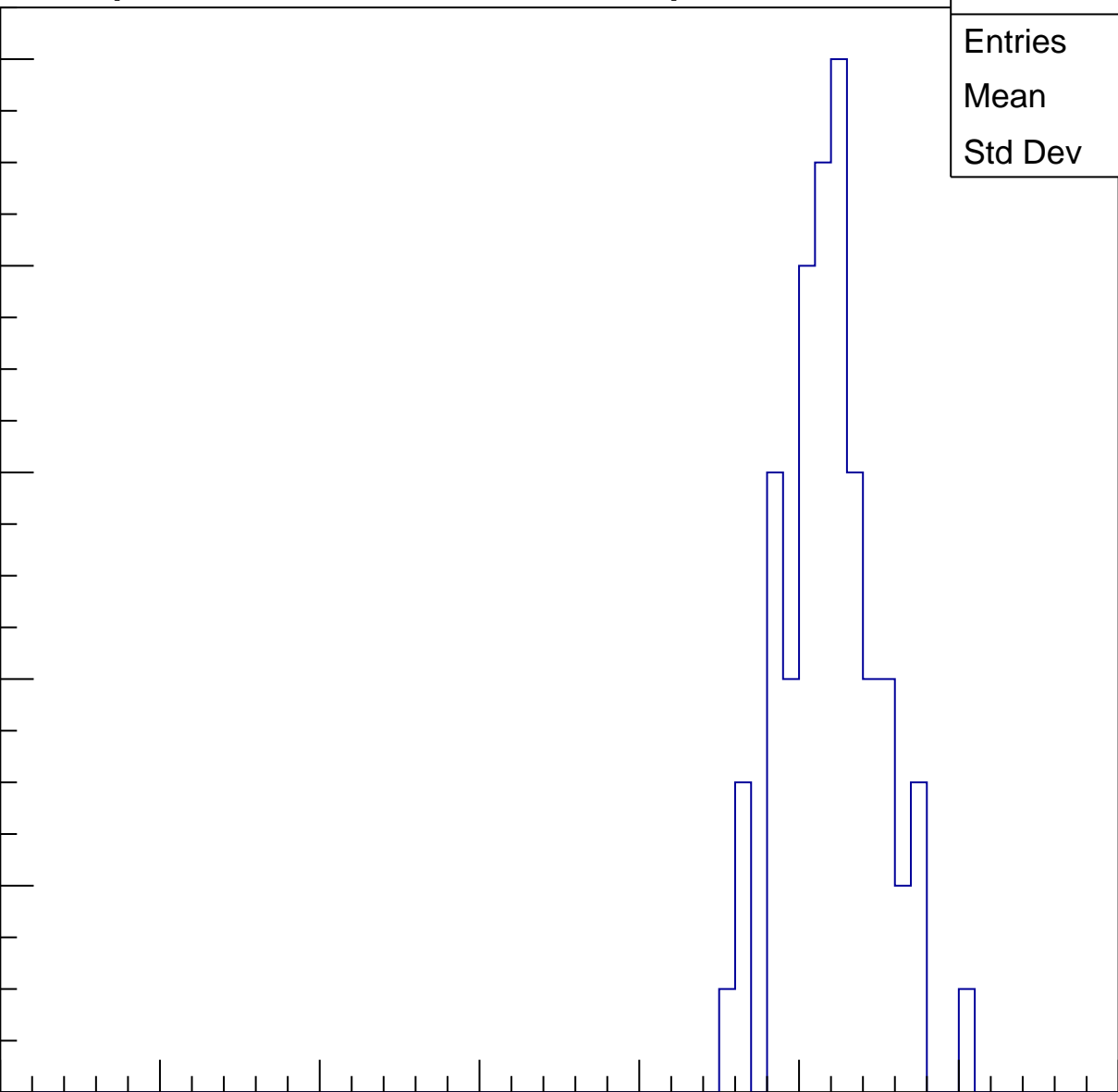
Entries	61
Mean	51.52
Std Dev	2.99

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

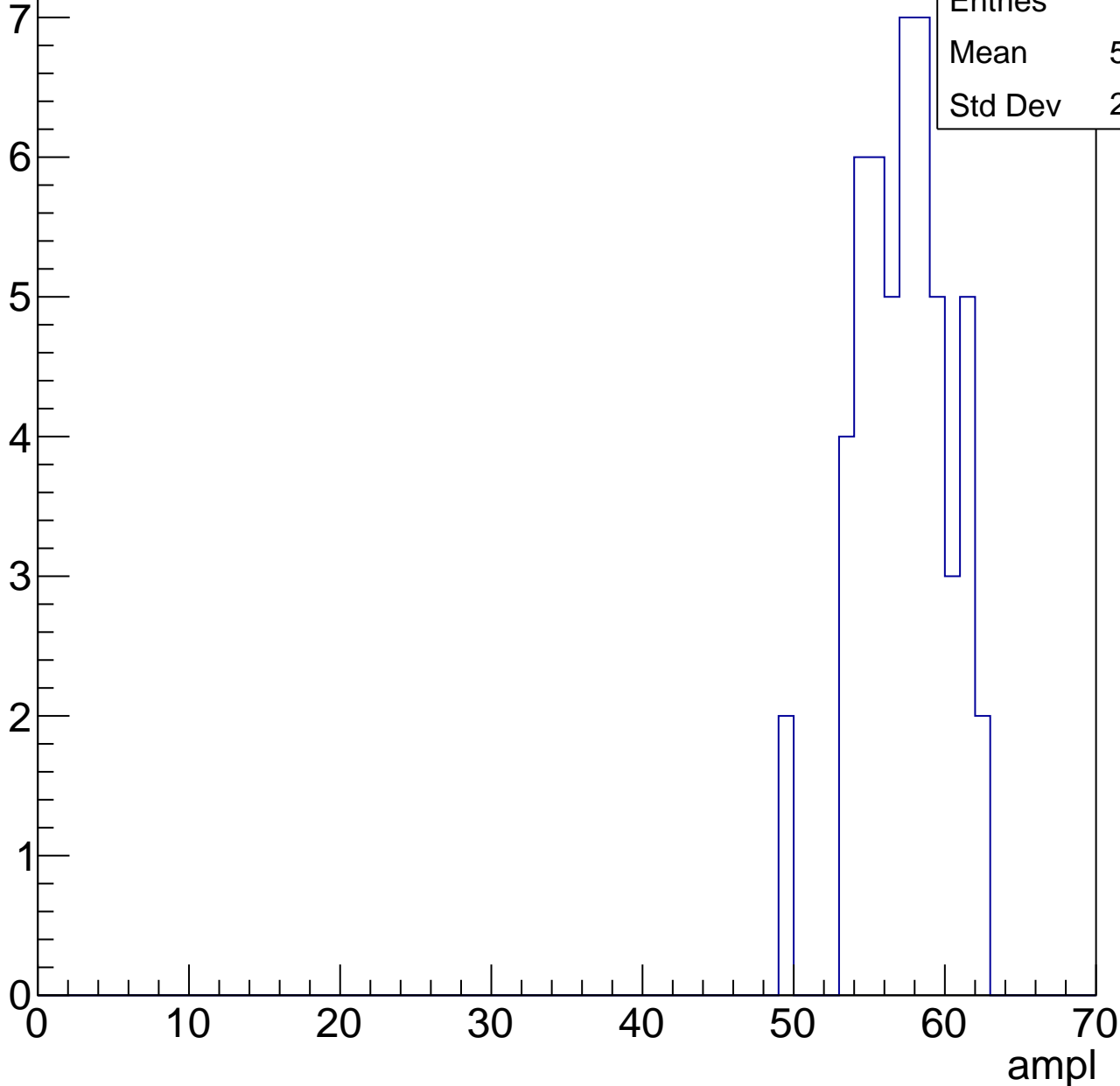


# B1L100S, U6-ch109, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	52
Mean	56.79
Std Dev	2.963

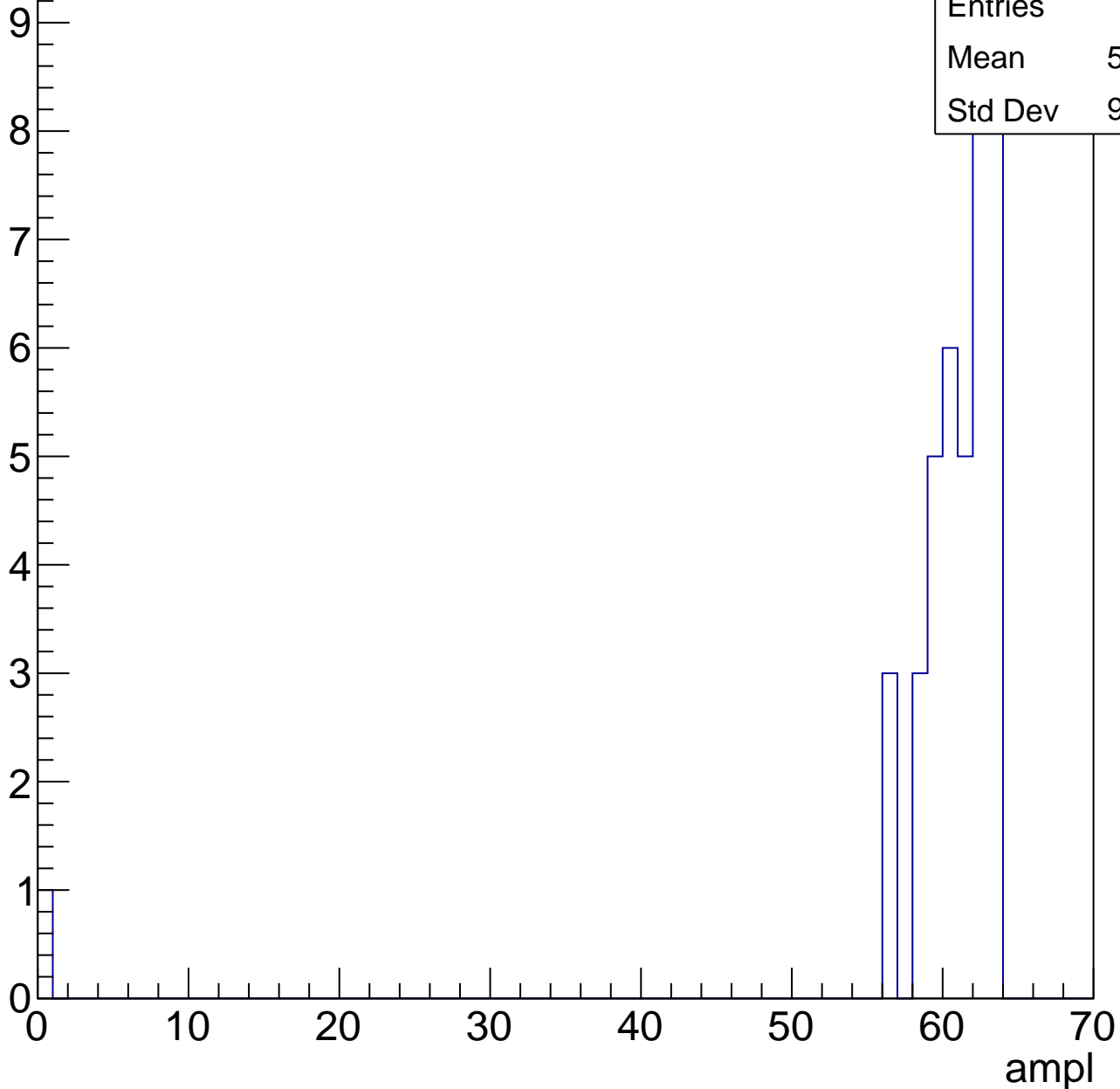


# B1L100S, U6-ch109, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	40
Mean	59.12
Std Dev	9.686



# B1L100S, U6-ch109, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



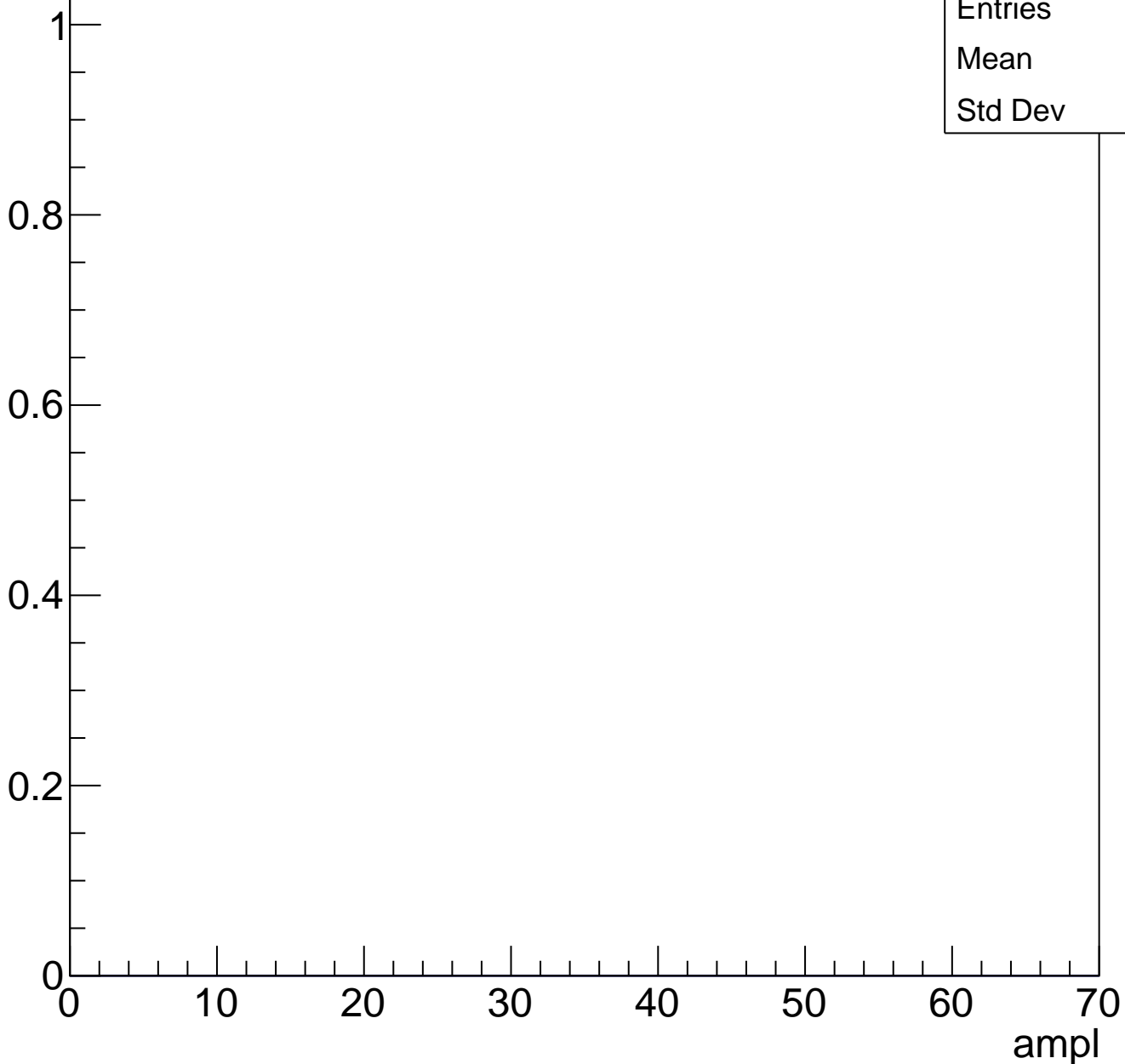
Entries	1
Mean	63
Std Dev	0



# B1L100S, U6-ch109, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L100S, U6-ch110, adc0

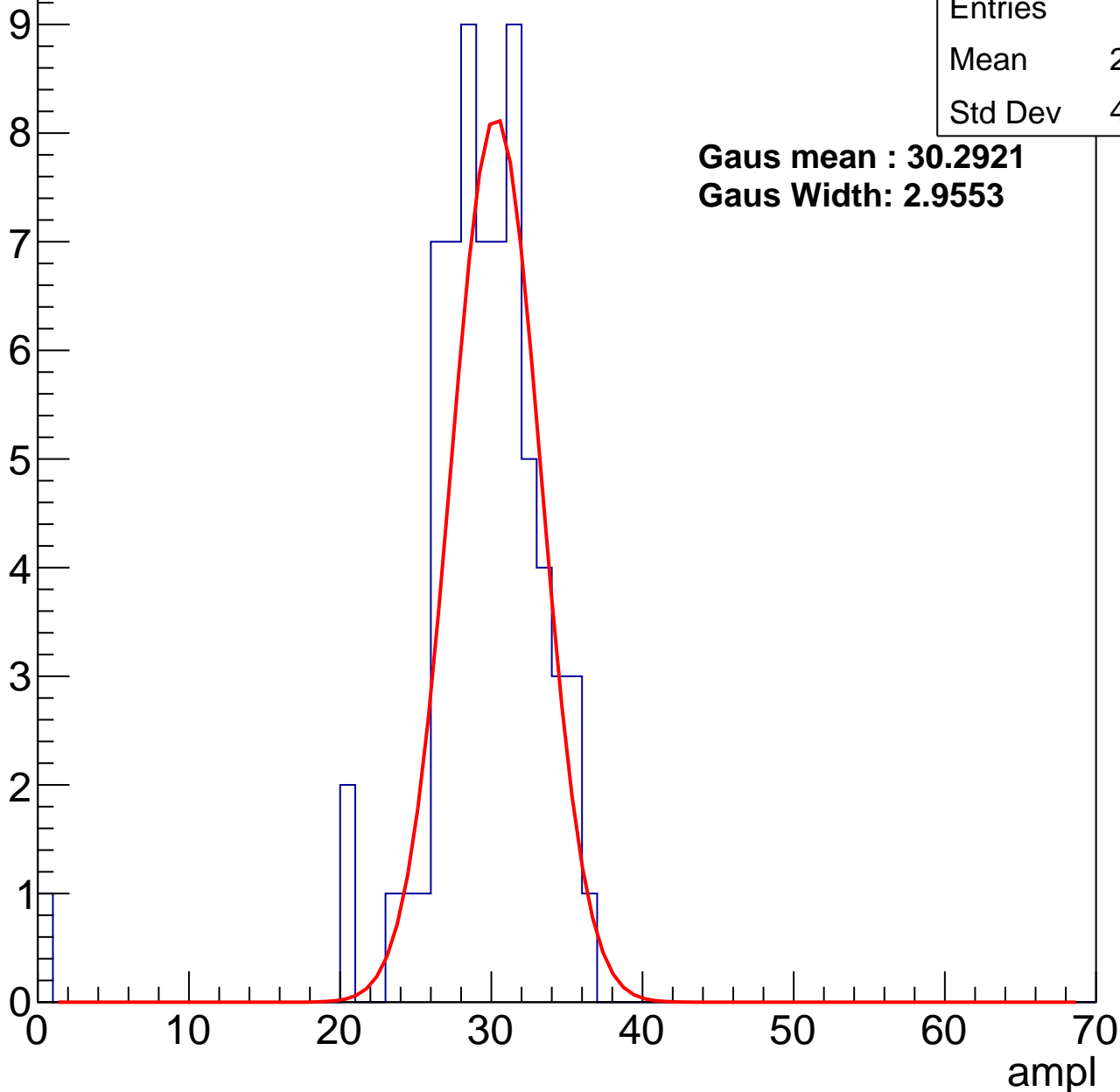
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	68
Mean	28.85
Std Dev	4.794

**Gaus mean : 30.2921**

**Gaus Width: 2.9553**



# B1L100S, U6-ch110, adc1

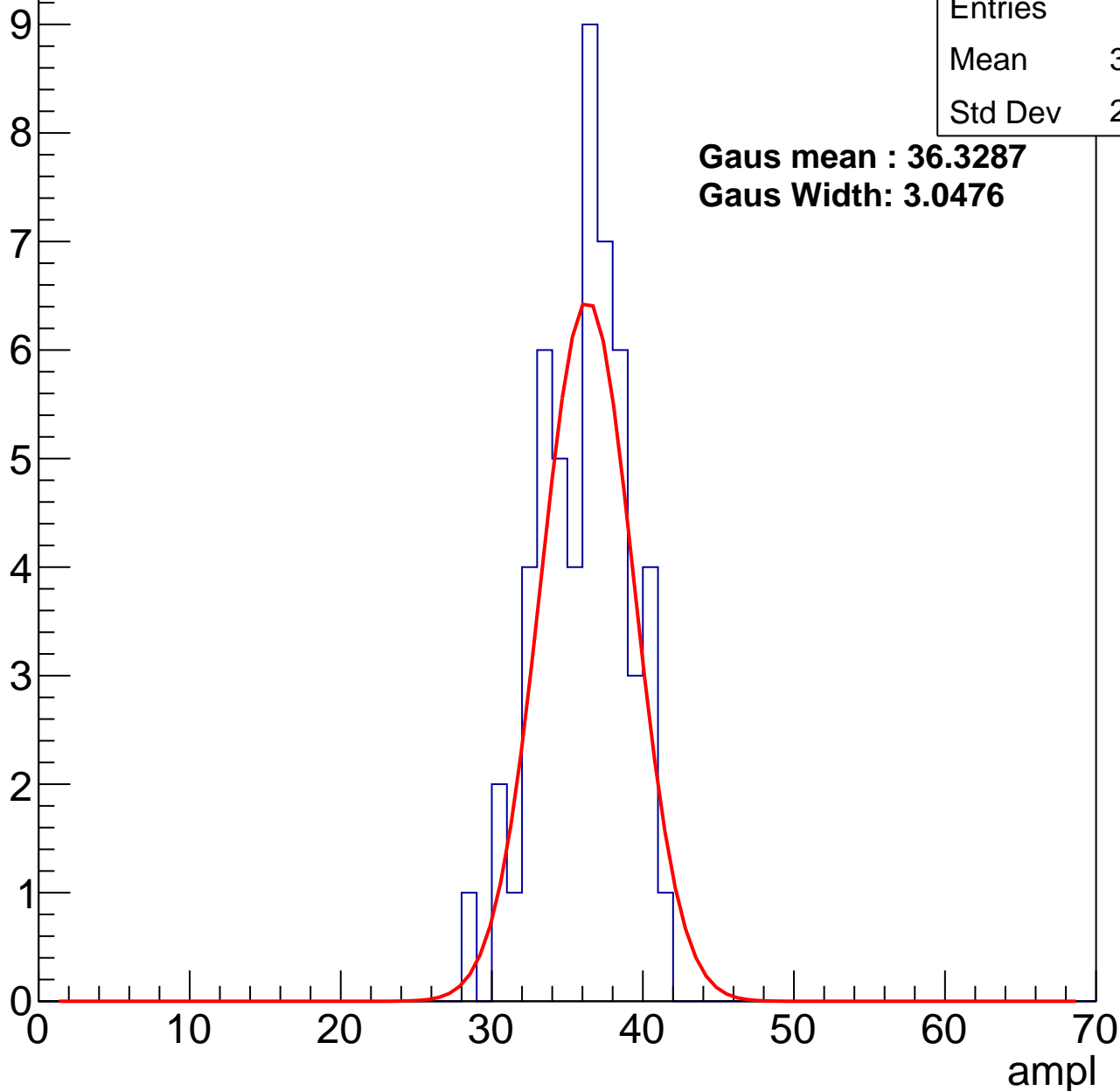
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	53
Mean	35.55
Std Dev	2.878

**Gaus mean : 36.3287**

**Gaus Width: 3.0476**



# B1L100S, U6-ch110, adc2

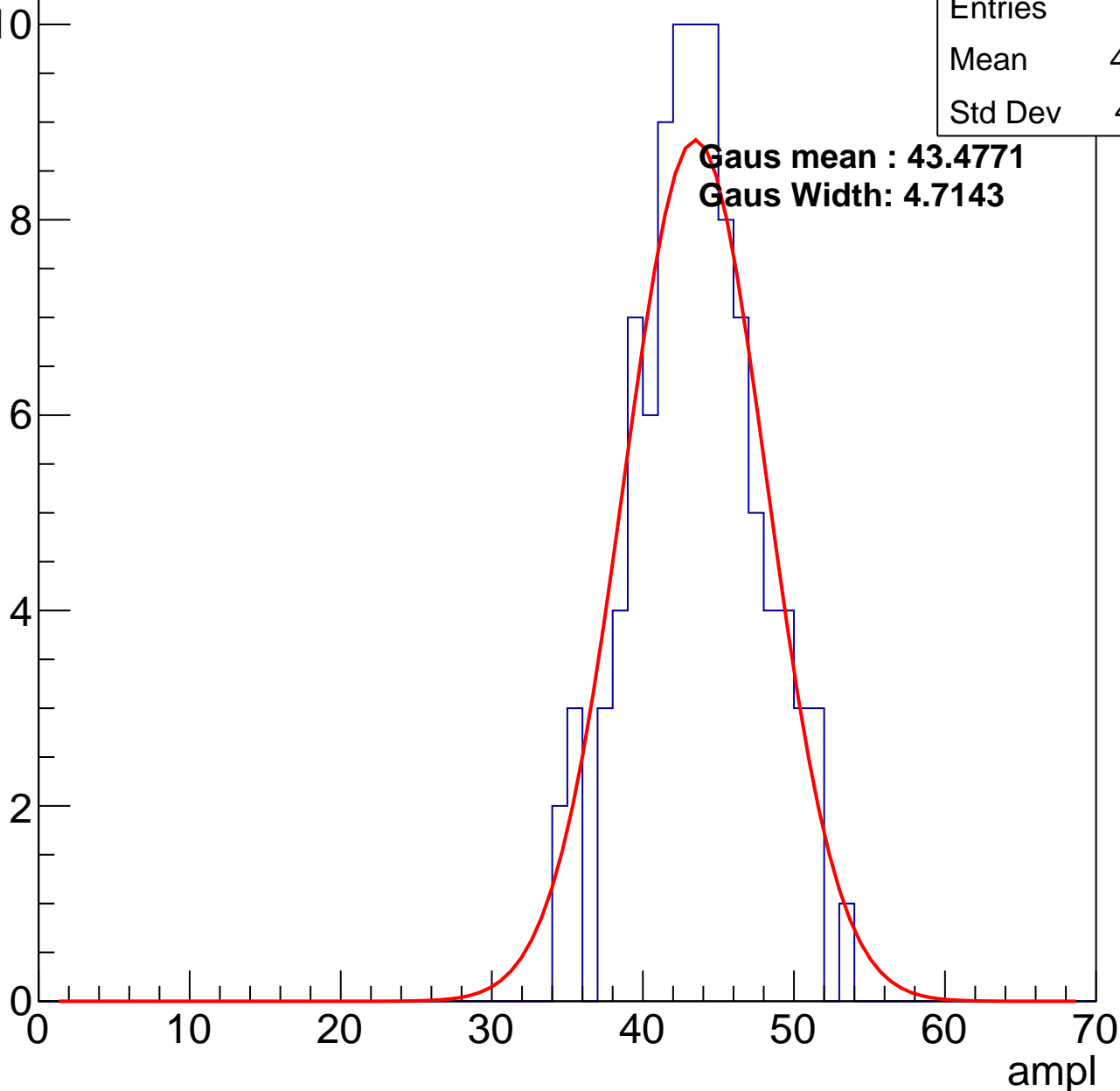
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	99
Mean	43.12
Std Dev	4.071

**Gaus mean : 43.4771**

**Gaus Width: 4.7143**

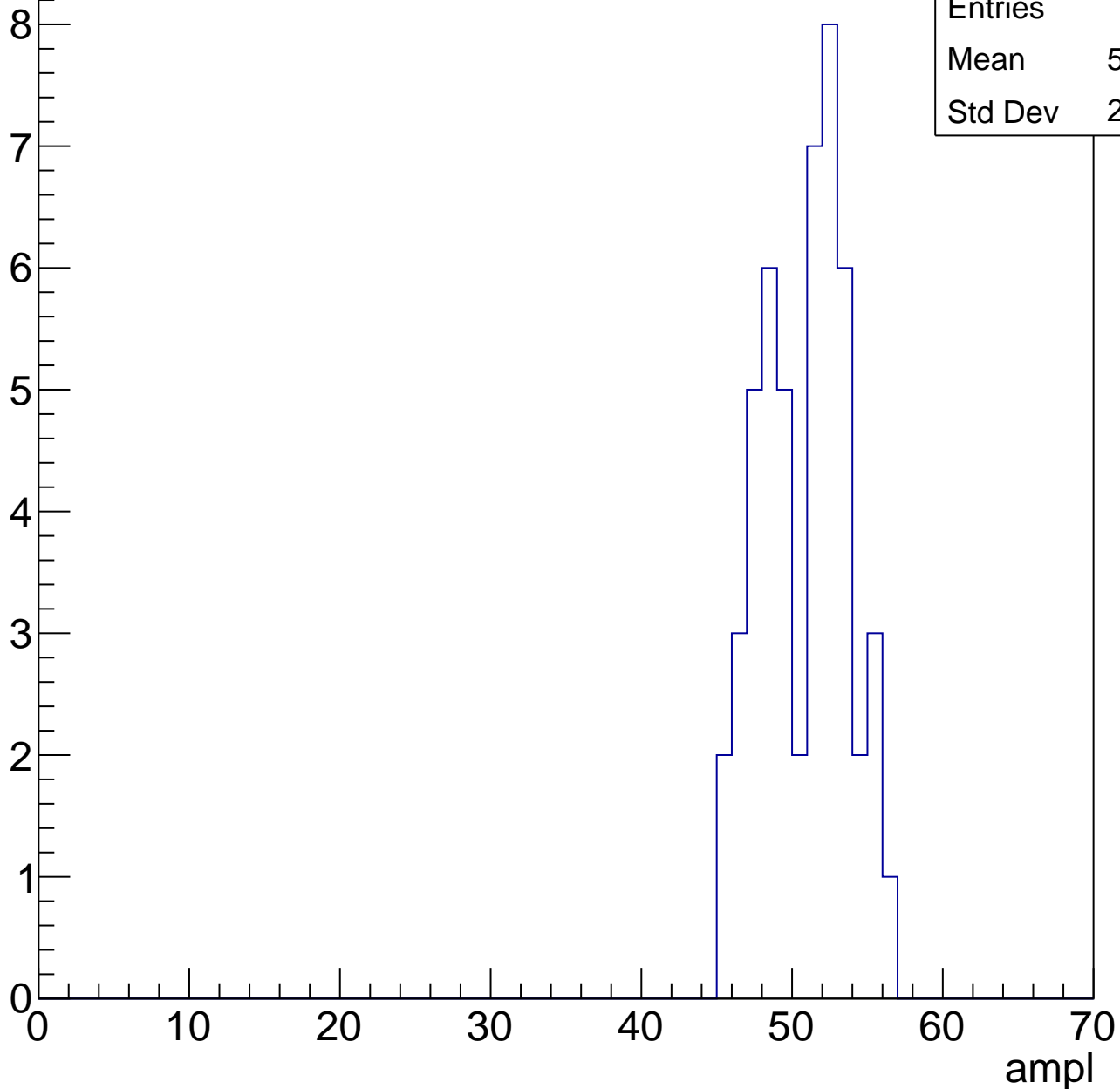


# B1L100S, U6-ch110, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	50
Mean	50.32
Std Dev	2.839

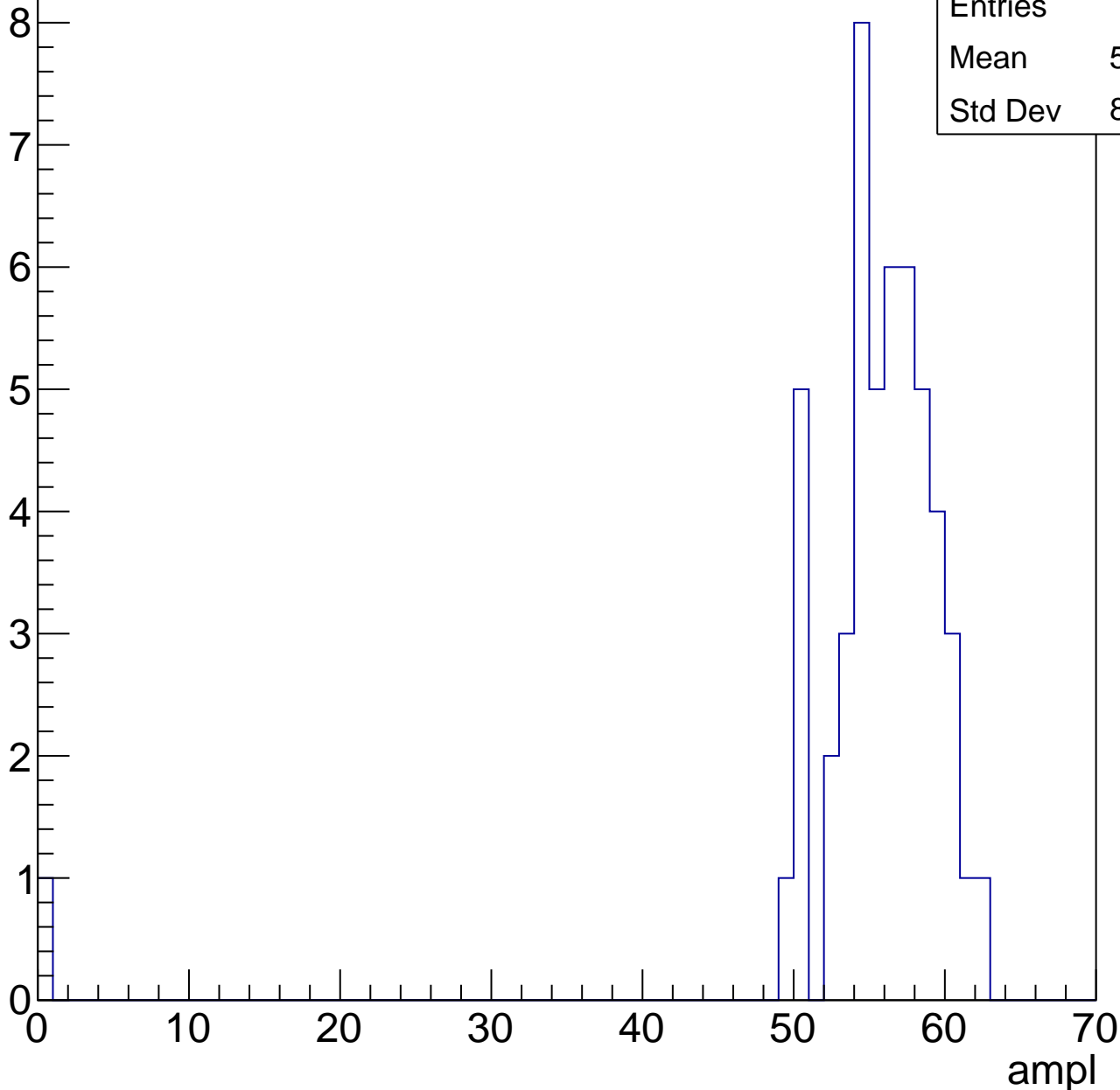


# B1L100S, U6-ch110, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

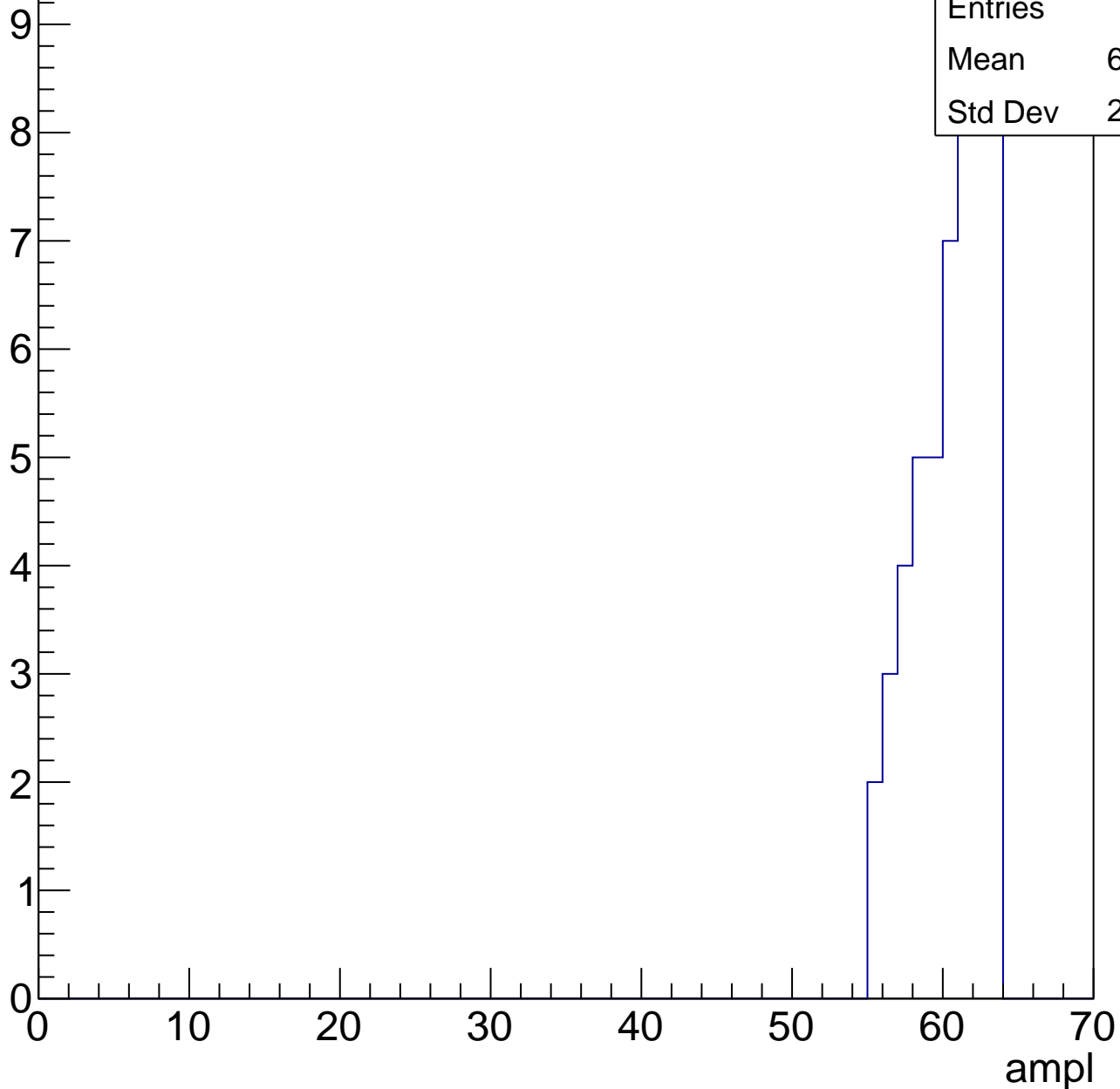
Entries	51
Mean	54.43
Std Dev	8.292



# B1L100S, U6-ch110, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

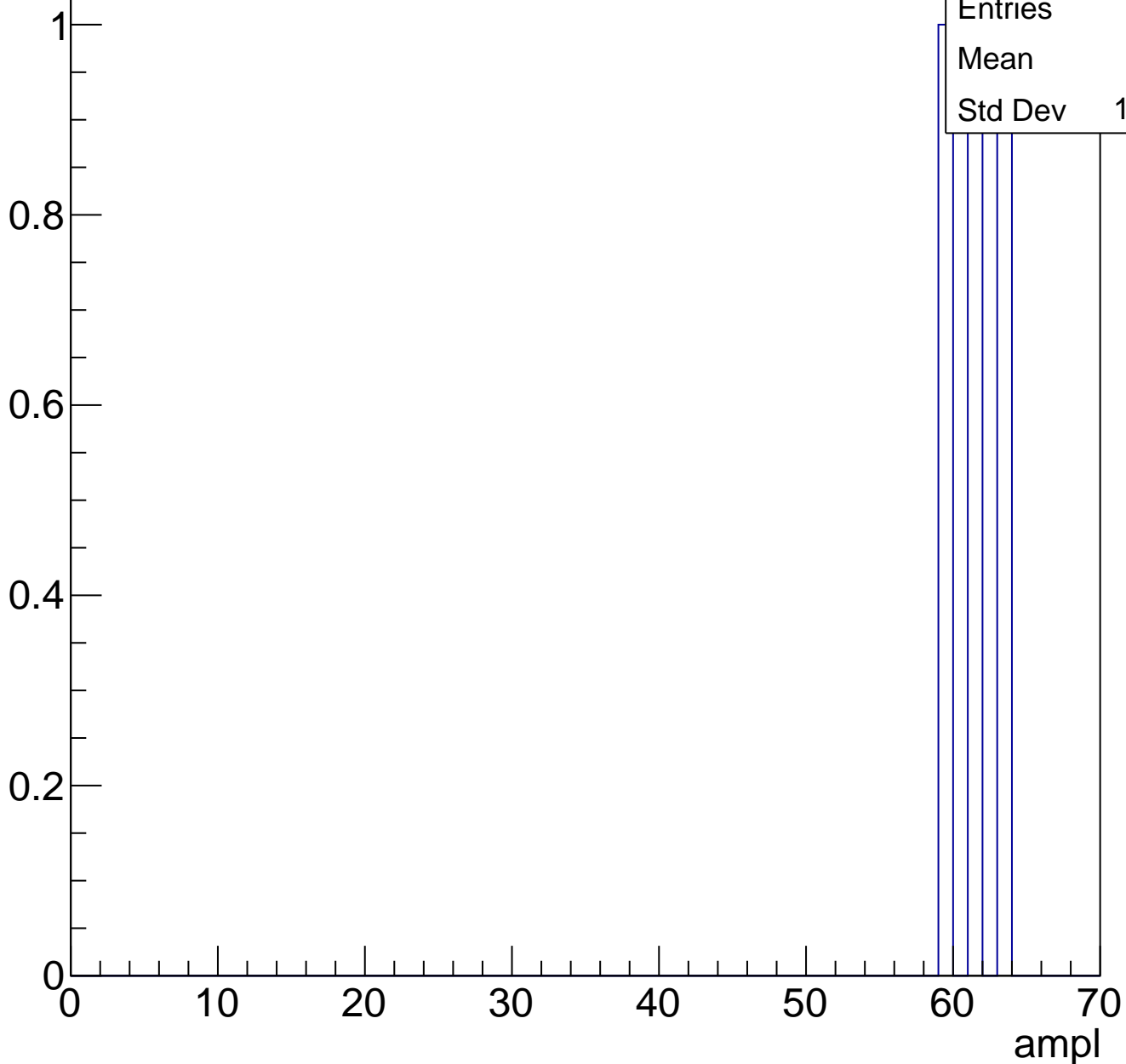


Entries	52
Mean	60.08
Std Dev	2.336

# B1L100S, U6-ch110, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry





# B1L100S, U6-ch110, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



# B1L100S, U6-ch111, adc0

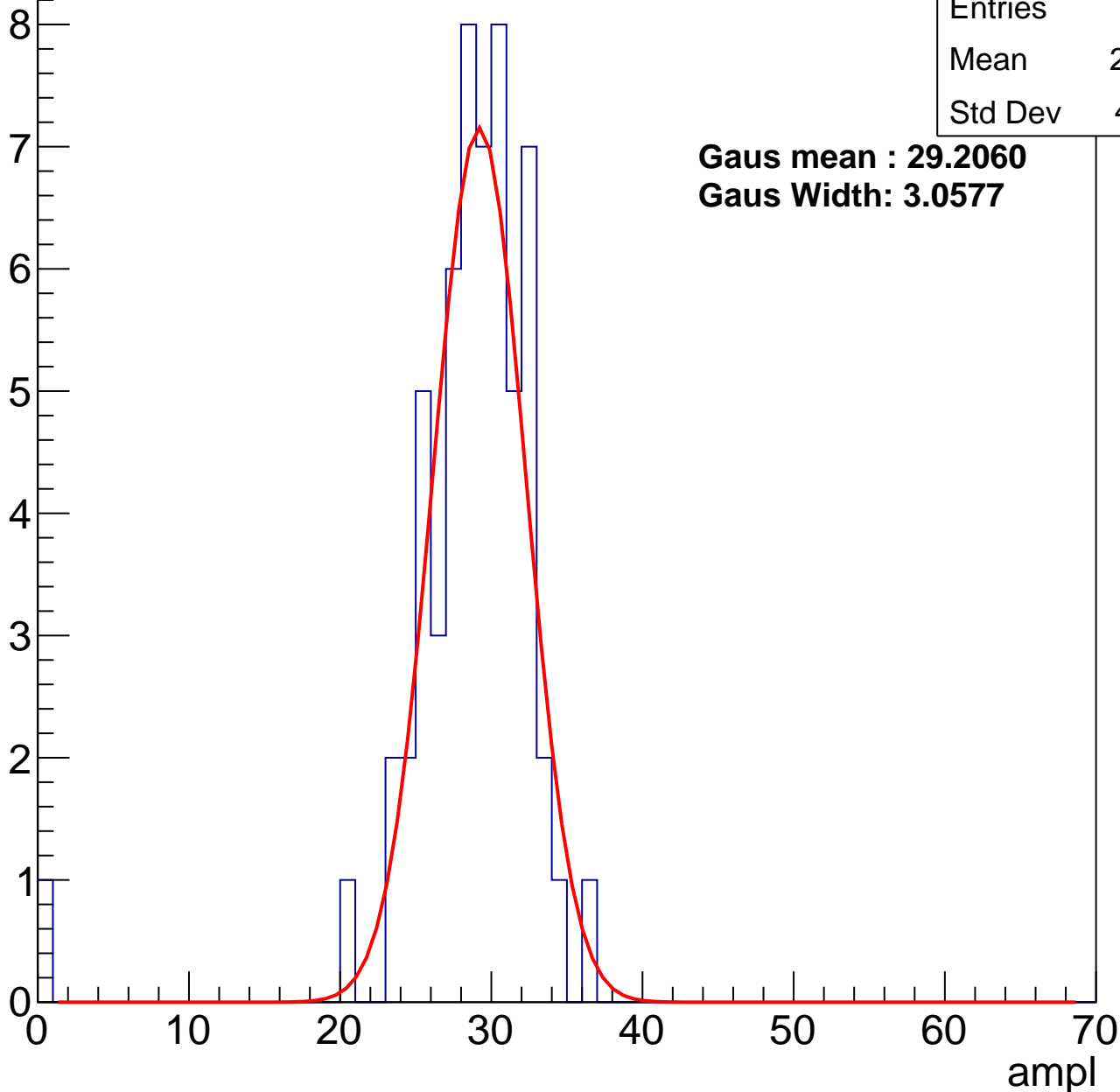
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	59
Mean	28.15
Std Dev	4.761

**Gaus mean : 29.2060**

**Gaus Width: 3.0577**



# B1L100S, U6-ch111, adc1

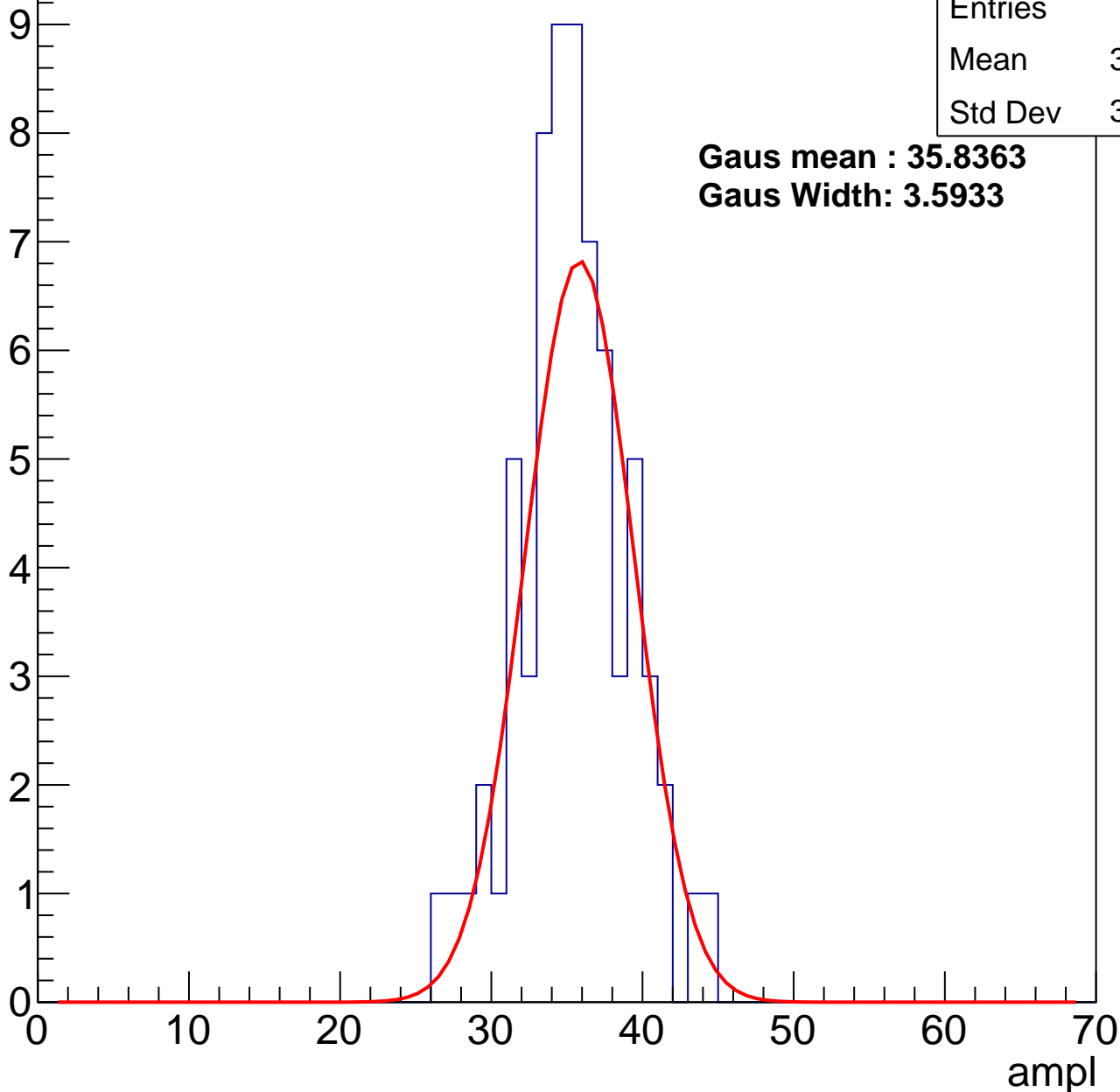
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	68
Mean	34.96
Std Dev	3.575

**Gaus mean : 35.8363**

**Gaus Width: 3.5933**



# B1L100S, U6-ch111, adc2

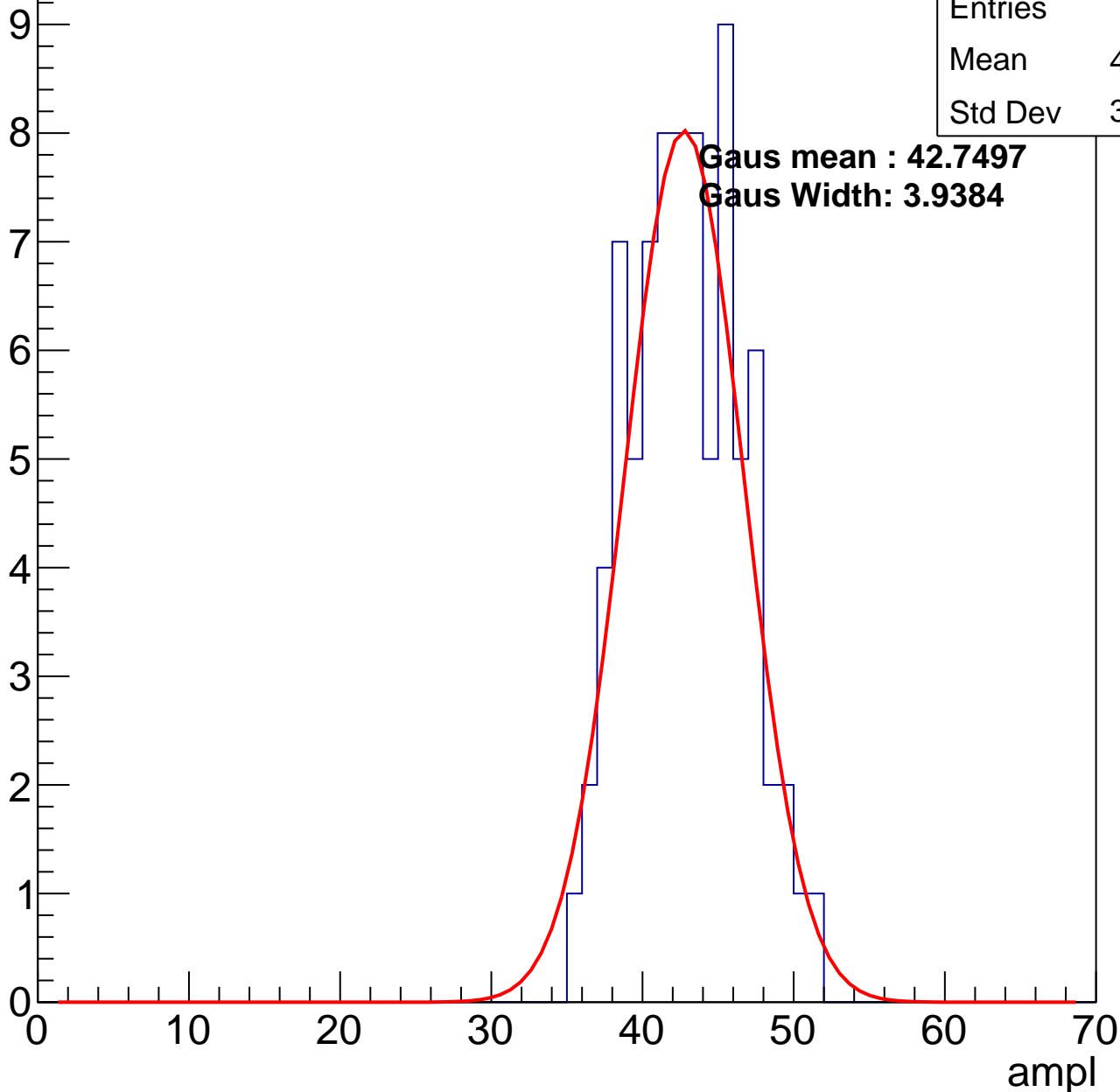
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	81
Mean	42.42
Std Dev	3.607

**Gaus mean : 42.7497**

**Gaus Width: 3.9384**

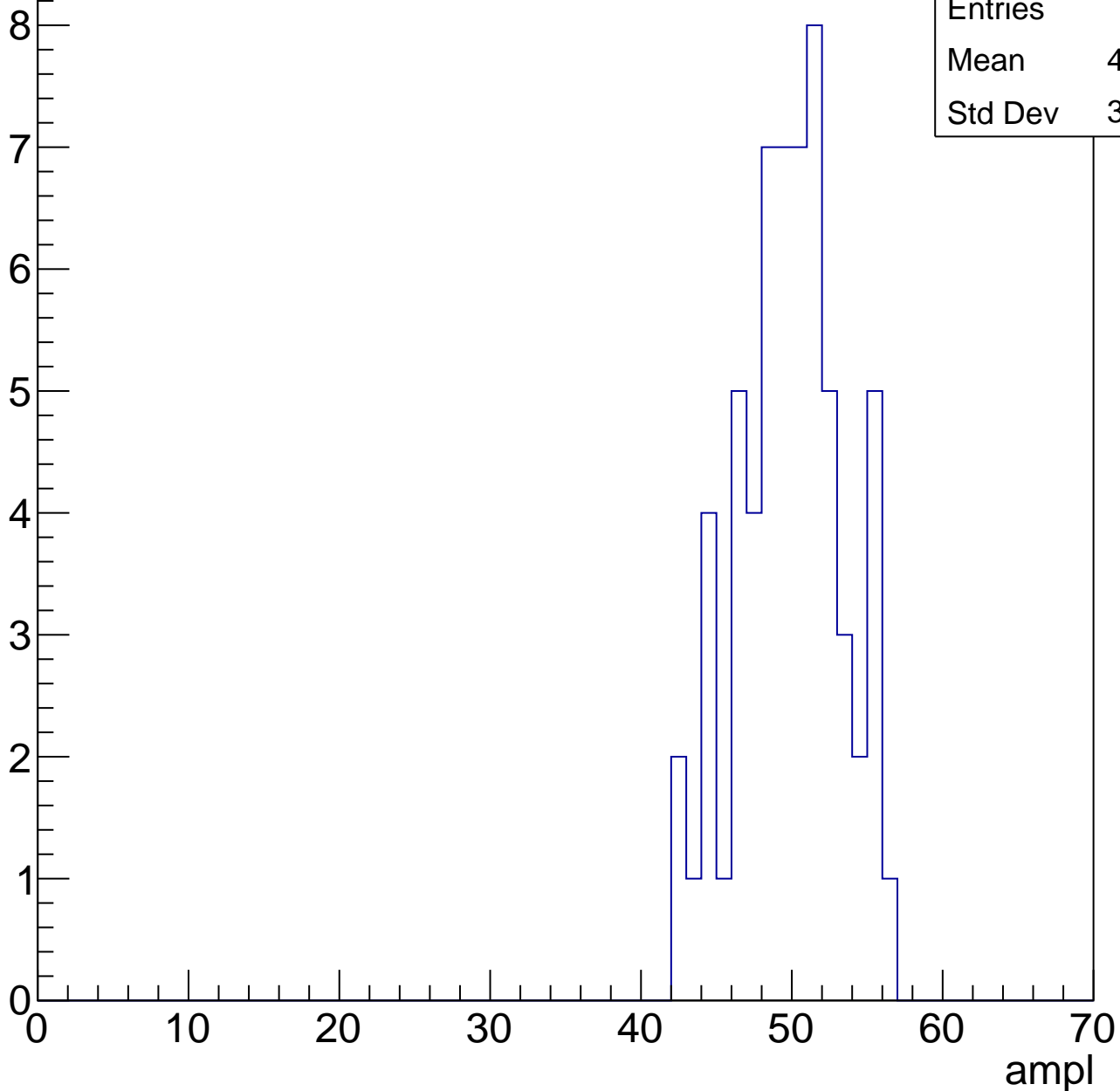


# B1L100S, U6-ch111, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	62
Mean	49.37
Std Dev	3.409

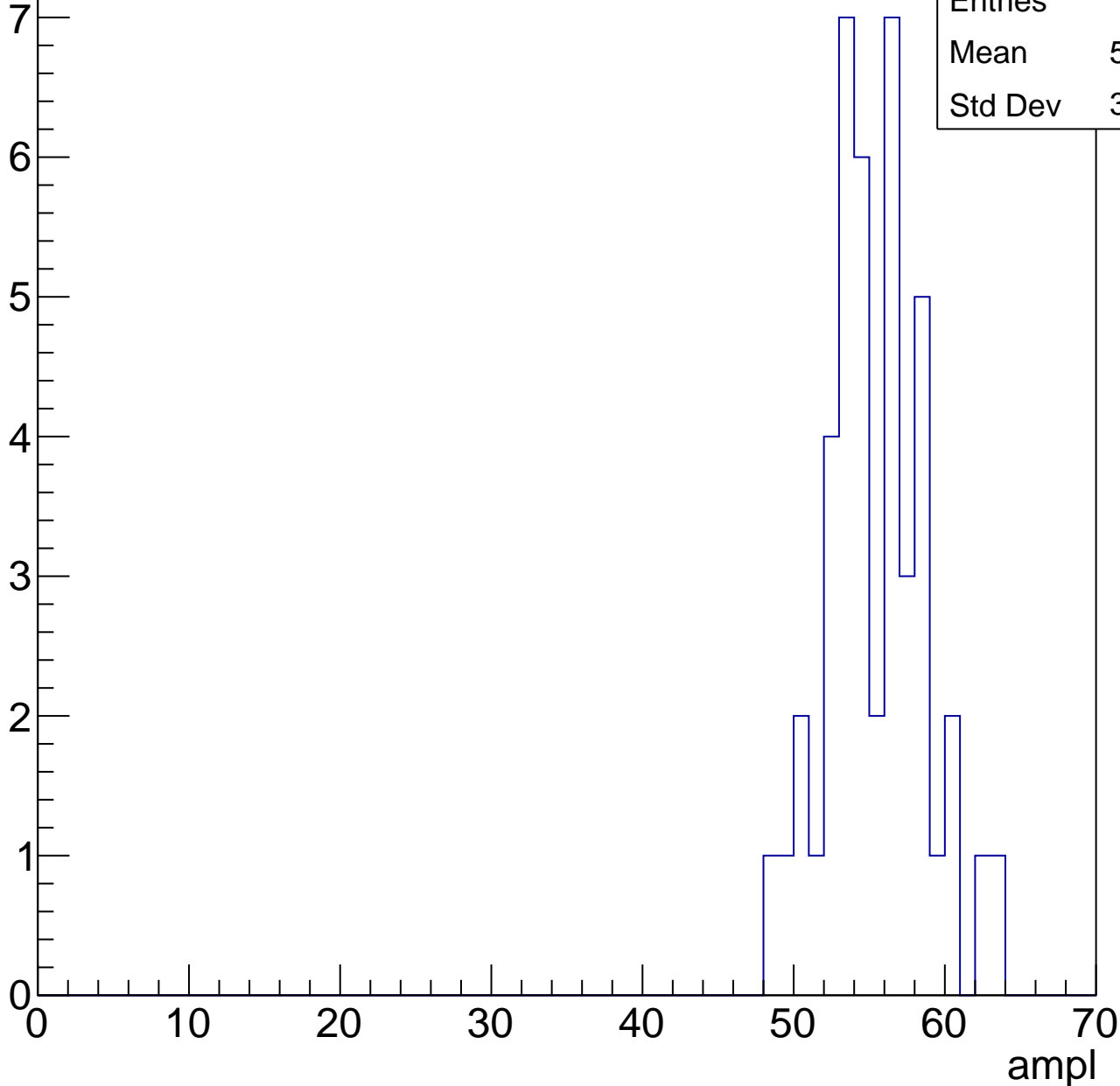


# B1L100S, U6-ch111, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	44
Mean	54.95
Std Dev	3.247



# B1L100S, U6-ch111, adc5

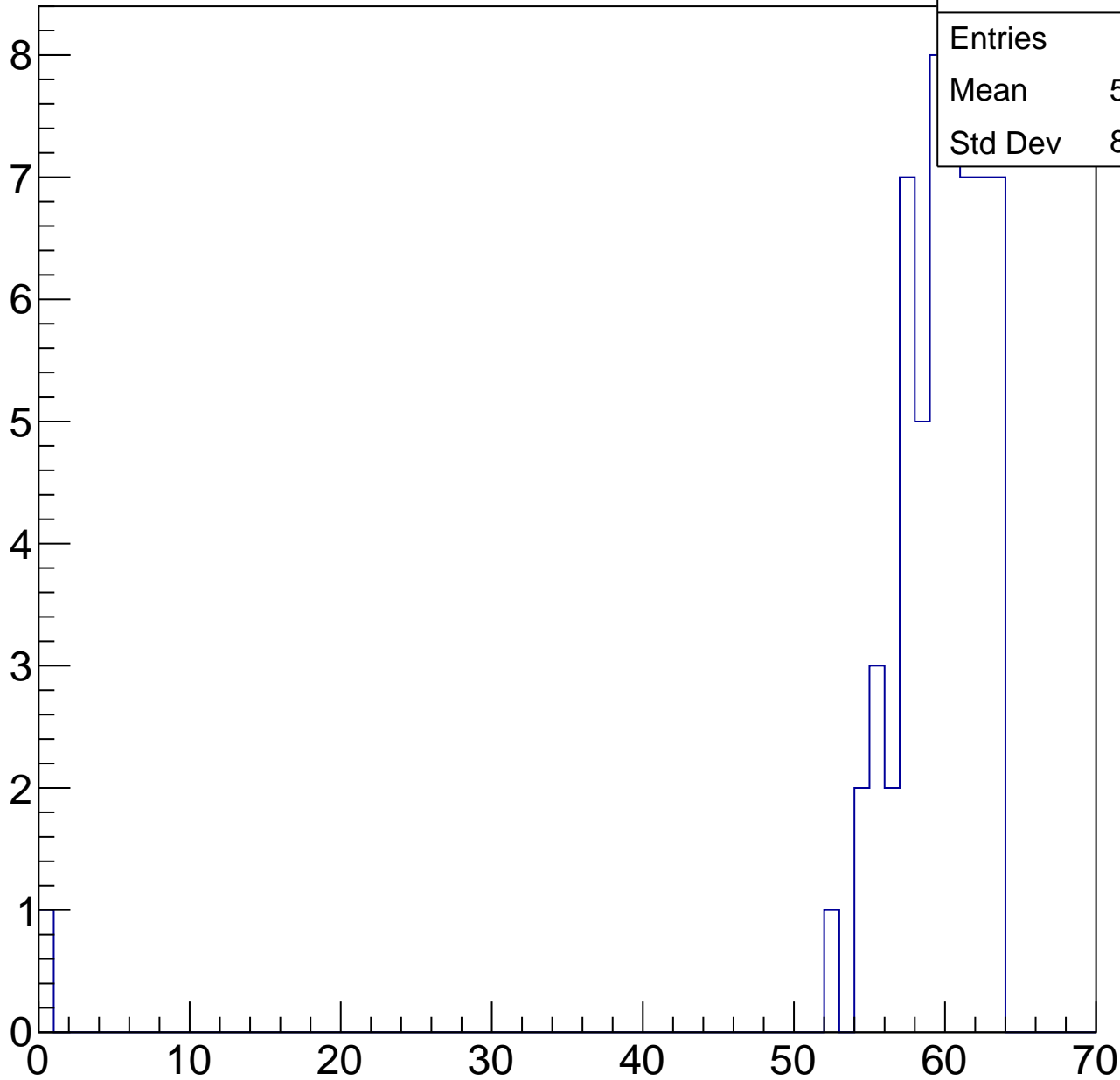
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	58
Mean	58.28
Std Dev	8.157

ampl



# B1L100S, U6-ch111, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

3

2.5

2

1.5

1

0.5

0

Entries

8

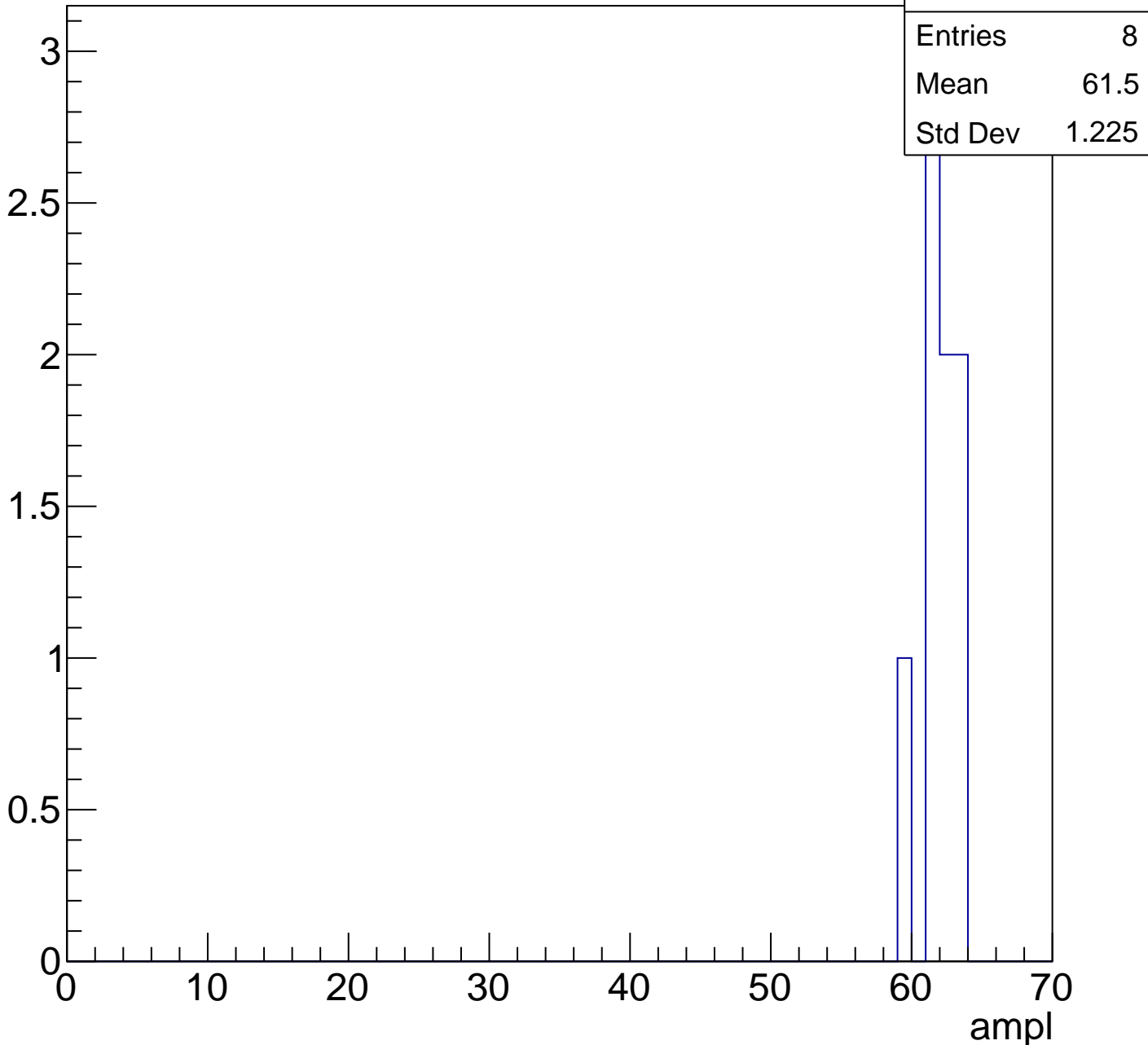
Mean

61.5

Std Dev

1.225

ampl





# B1L100S, U6-ch111, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L100S, U6-ch112, adc0

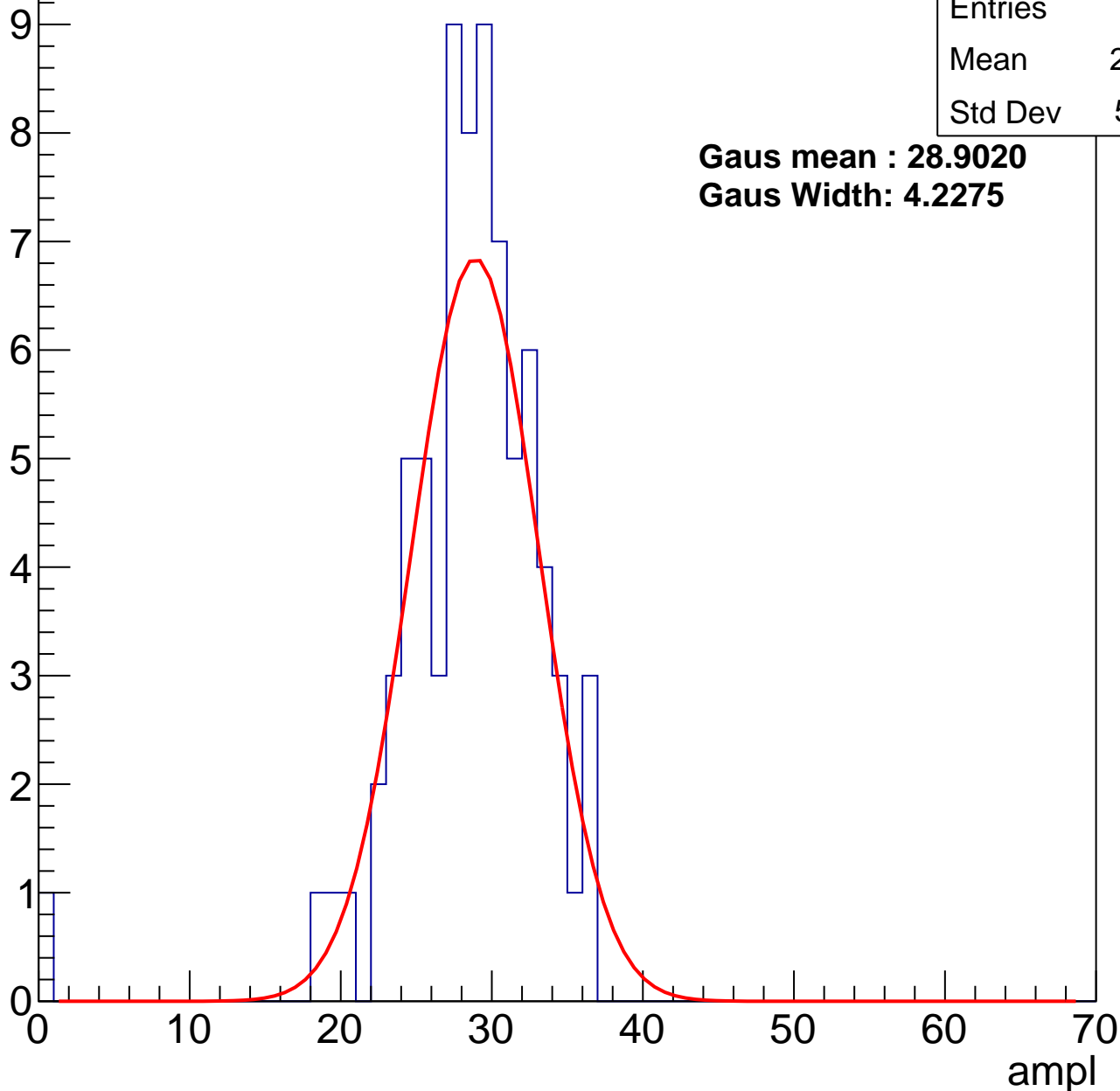
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	77
Mean	27.99
Std Dev	5.031

**Gaus mean : 28.9020**

**Gaus Width: 4.2275**



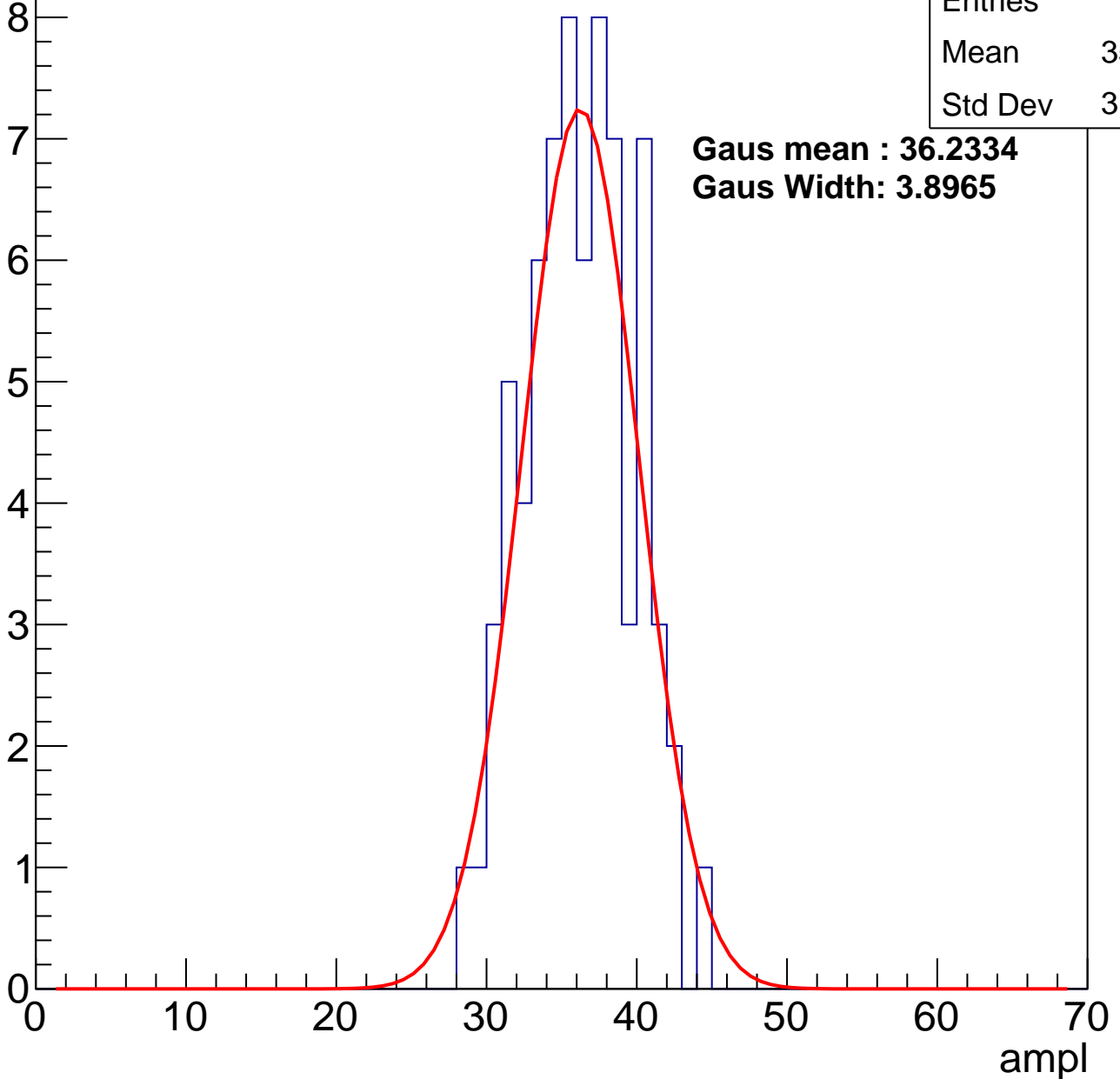
# B1L100S, U6-ch112, adc1

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	72
Mean	35.72
Std Dev	3.497

**Gaus mean : 36.2334**  
**Gaus Width: 3.8965**



# B1L100S, U6-ch112, adc2

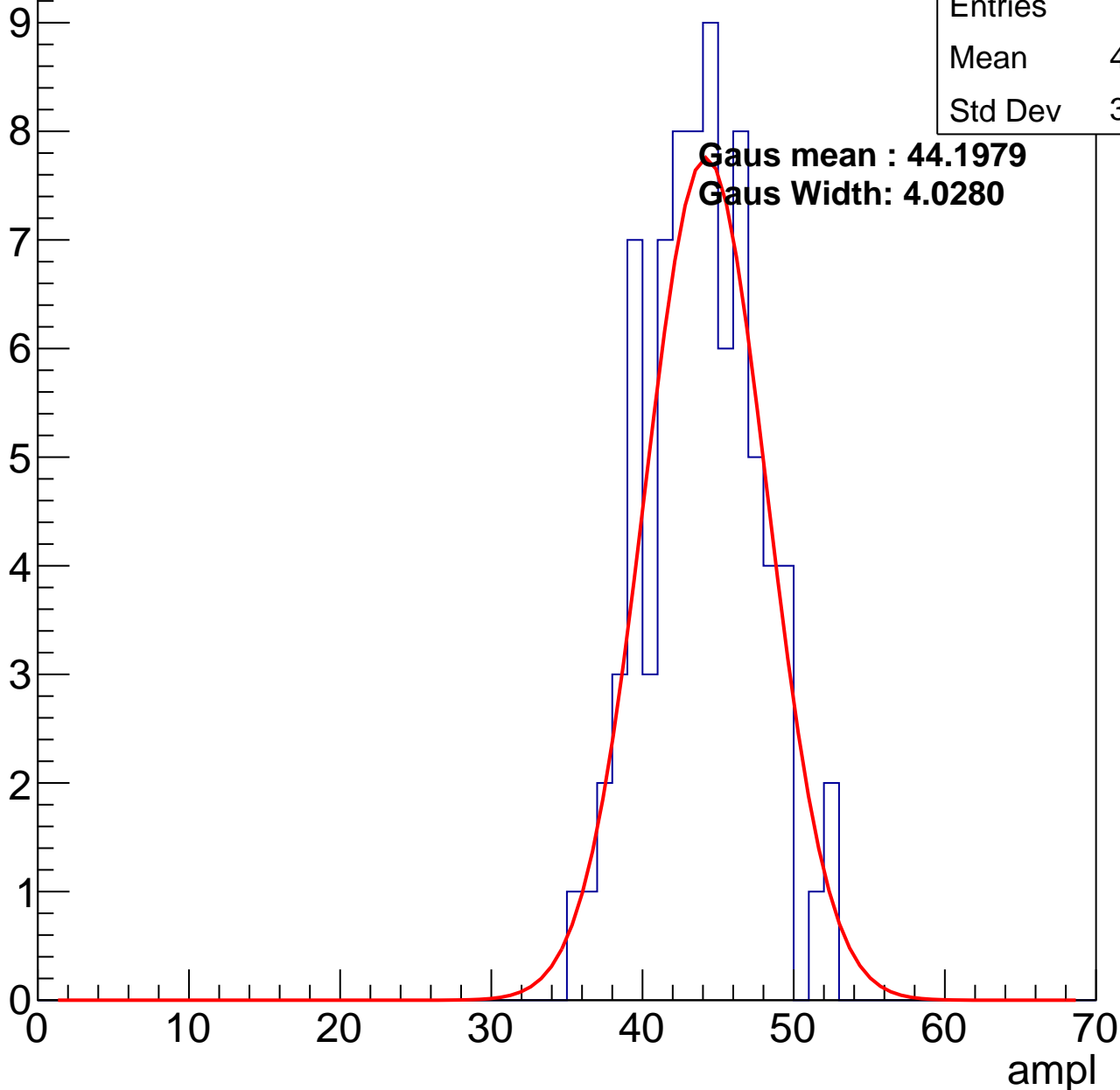
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	79
Mean	43.43
Std Dev	3.689

**Gaus mean : 44.1979**

**Gaus Width: 4.0280**

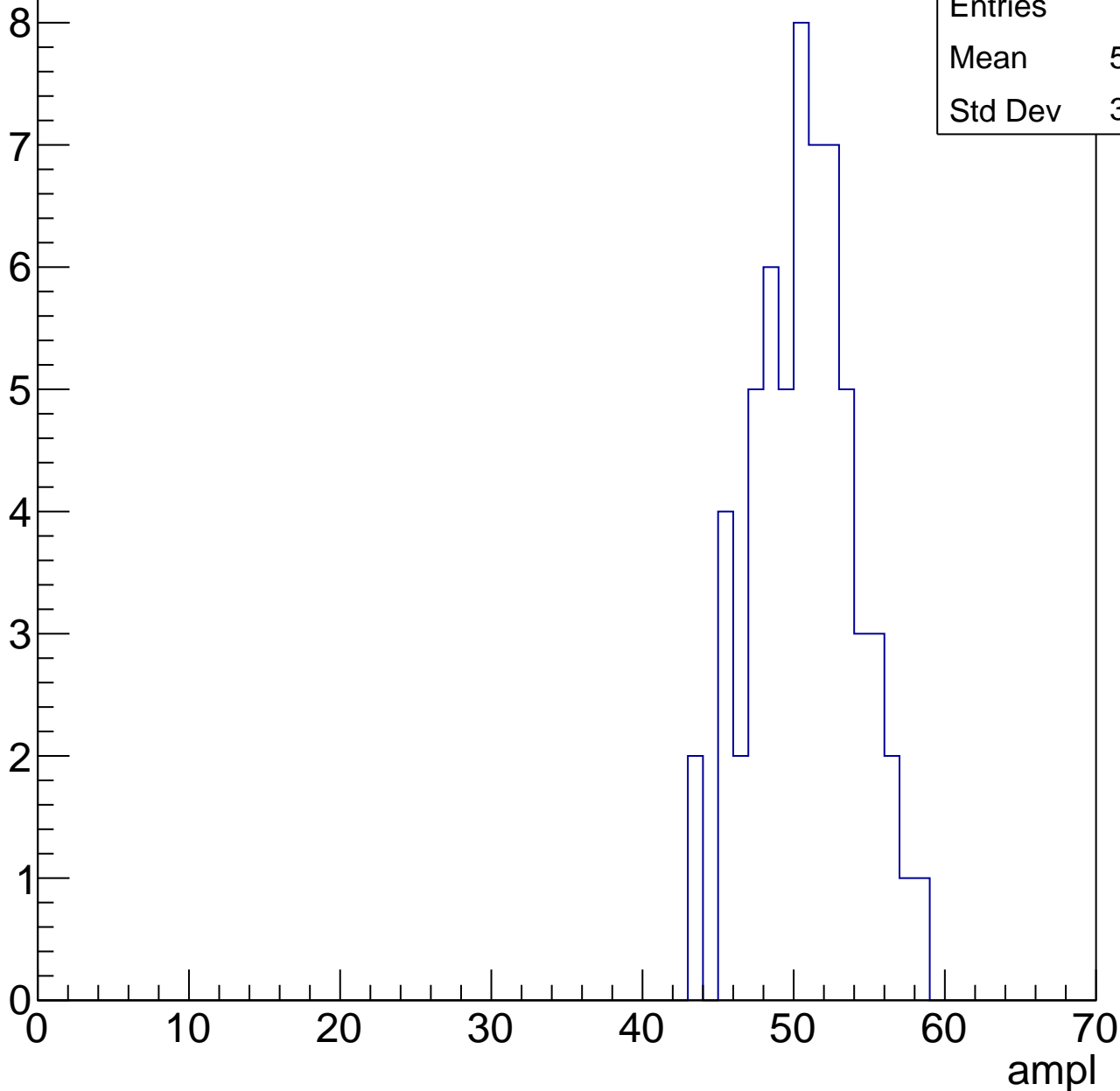


# B1L100S, U6-ch112, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

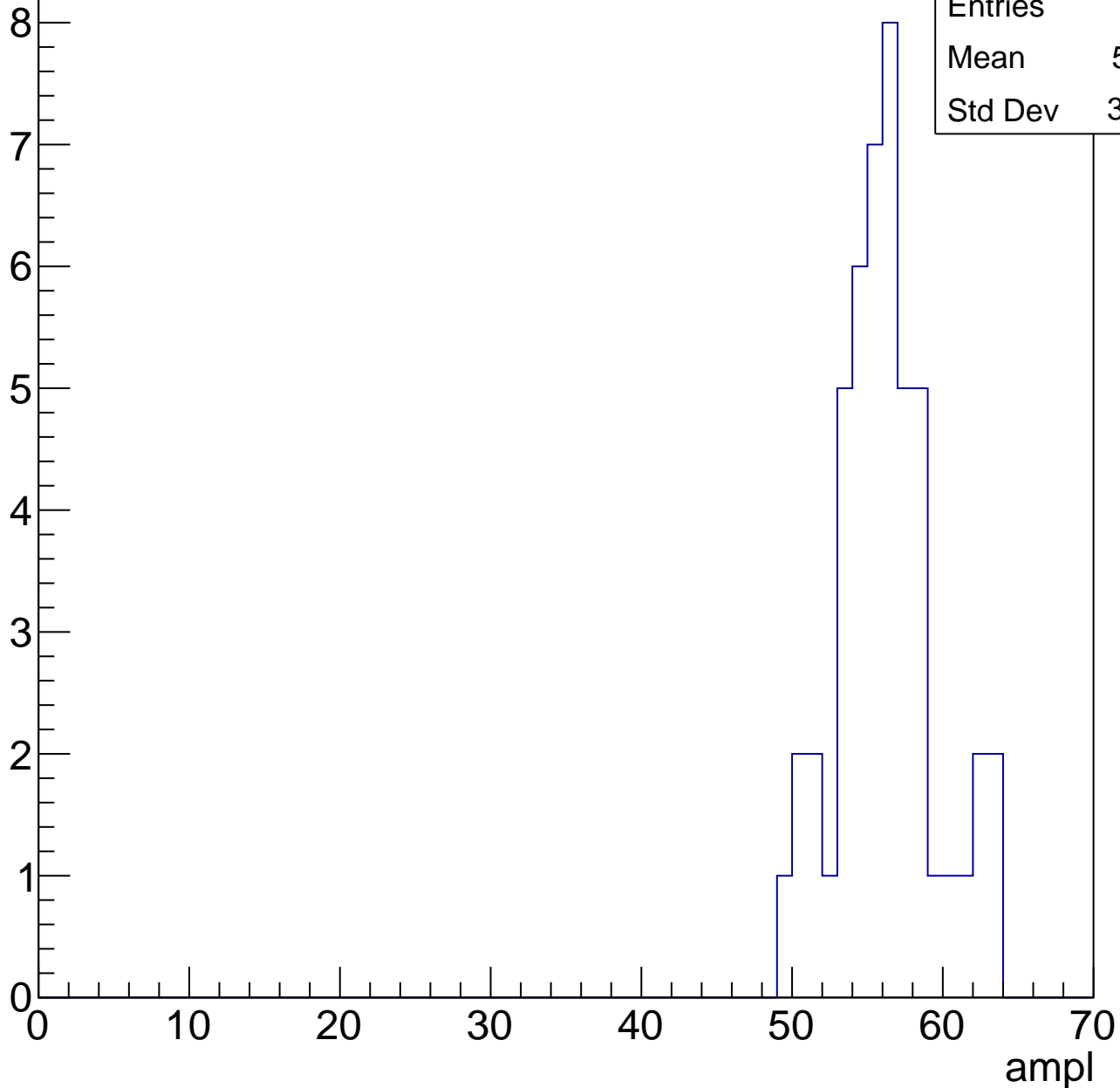
Entries	61
Mean	50.26
Std Dev	3.358



# B1L100S, U6-ch112, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

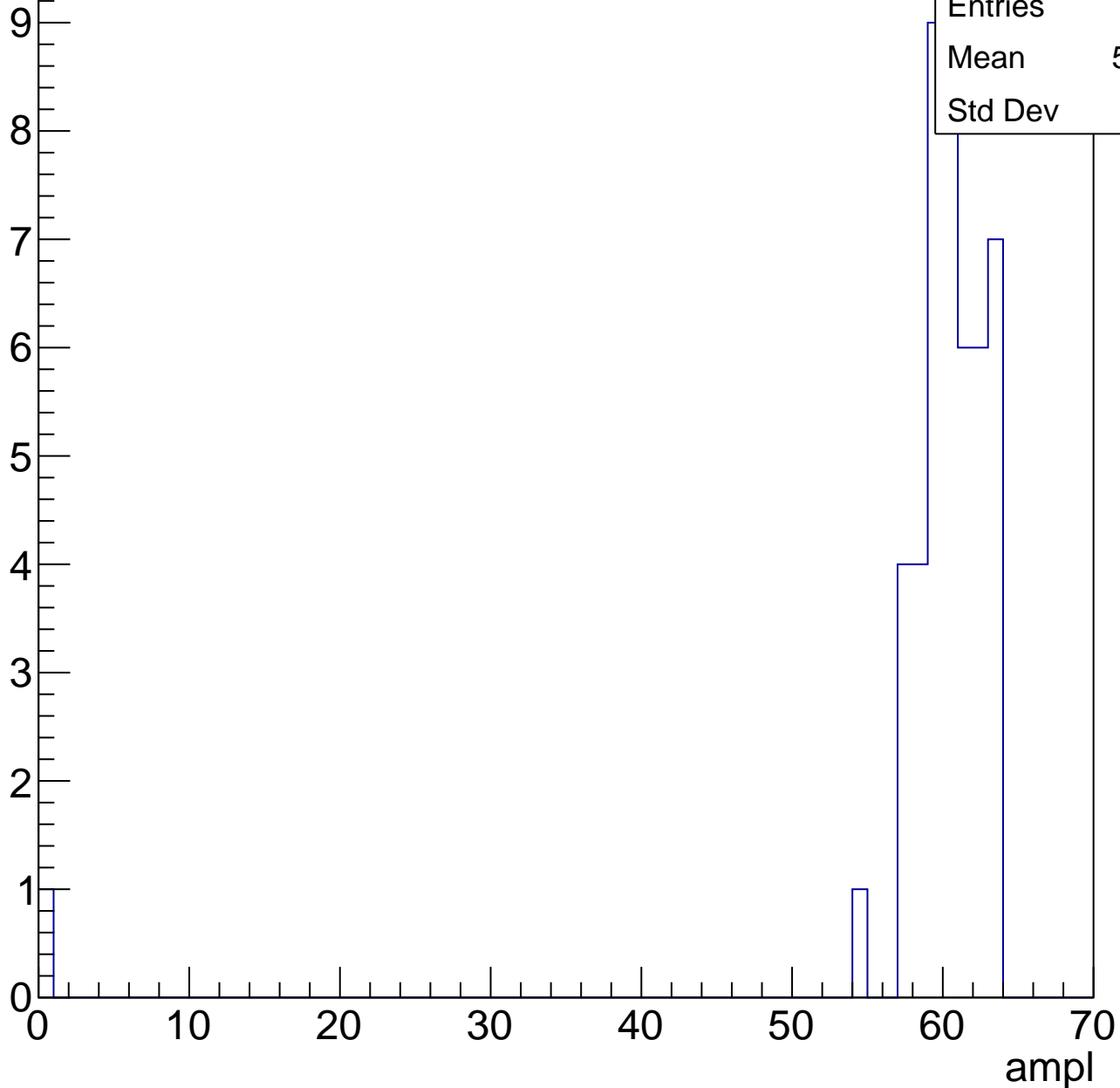


Entries	49
Mean	55.71
Std Dev	3.207

# B1L100S, U6-ch112, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

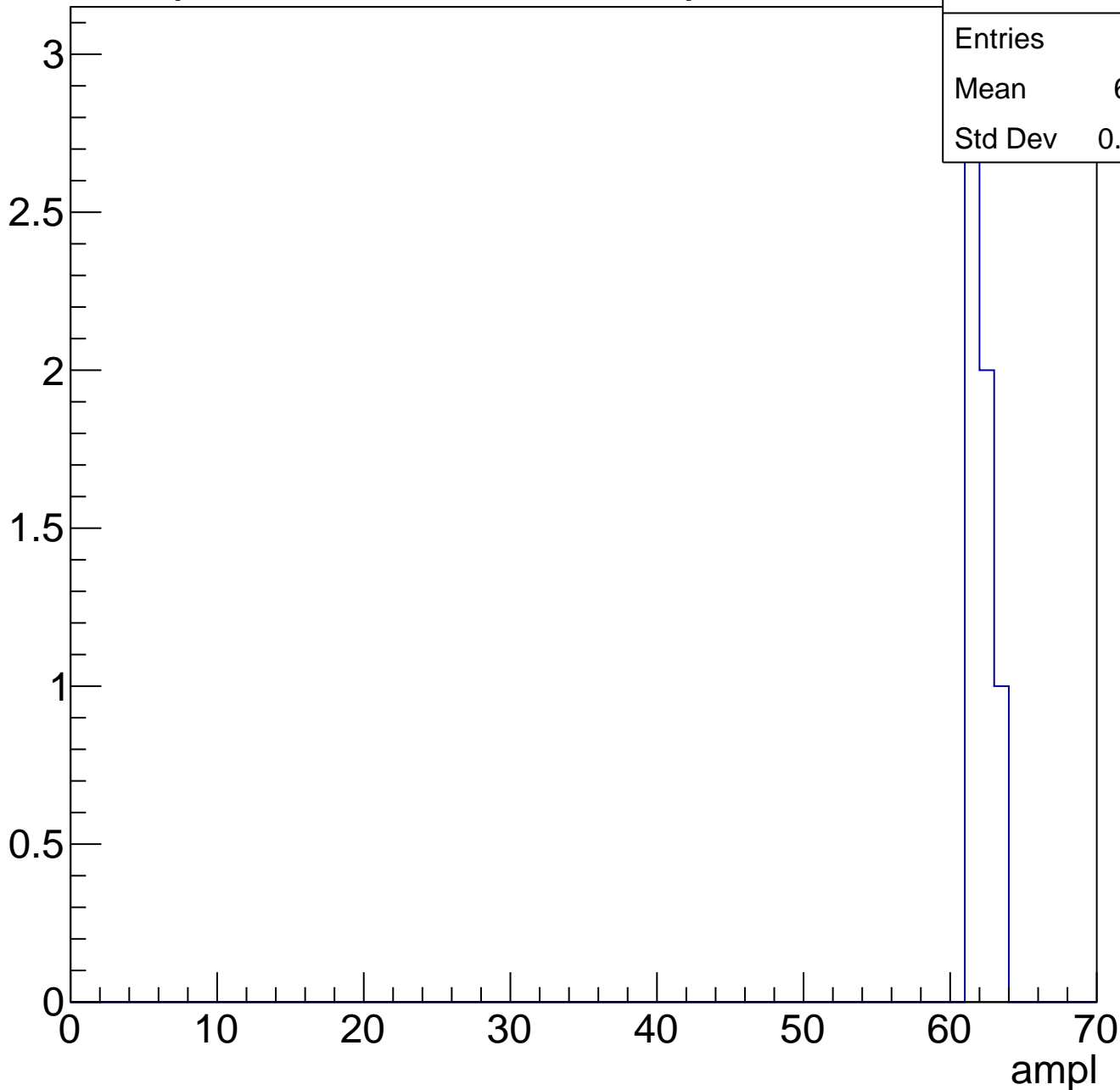


Entries	47
Mean	58.81
Std Dev	8.9

# B1L100S, U6-ch112, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry





# B1L100S, U6-ch112, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L100S, U6-ch113, adc0

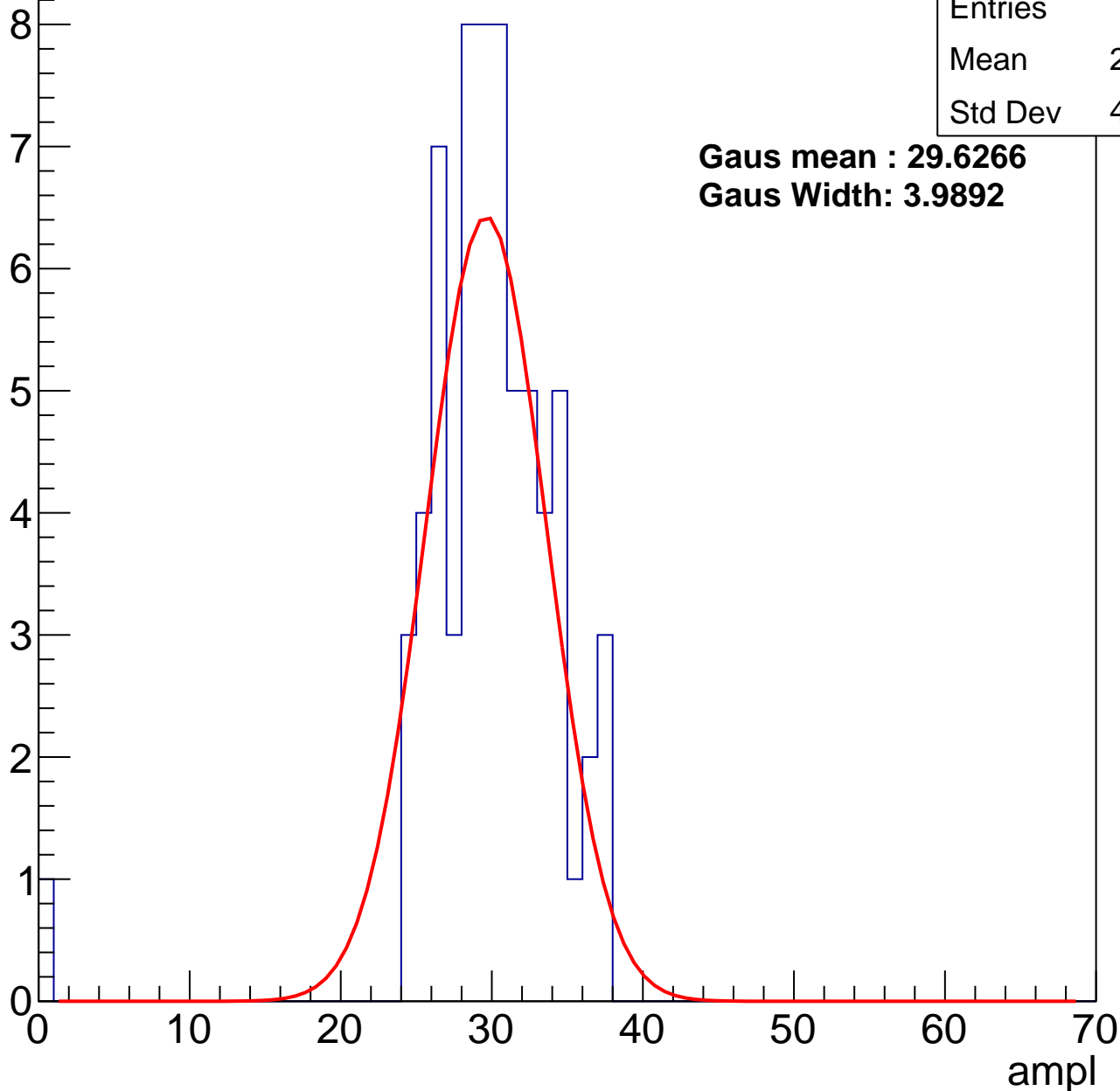
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	67
Mean	29.34
Std Dev	4.952

**Gaus mean : 29.6266**

**Gaus Width: 3.9892**



# B1L100S, U6-ch113, adc1

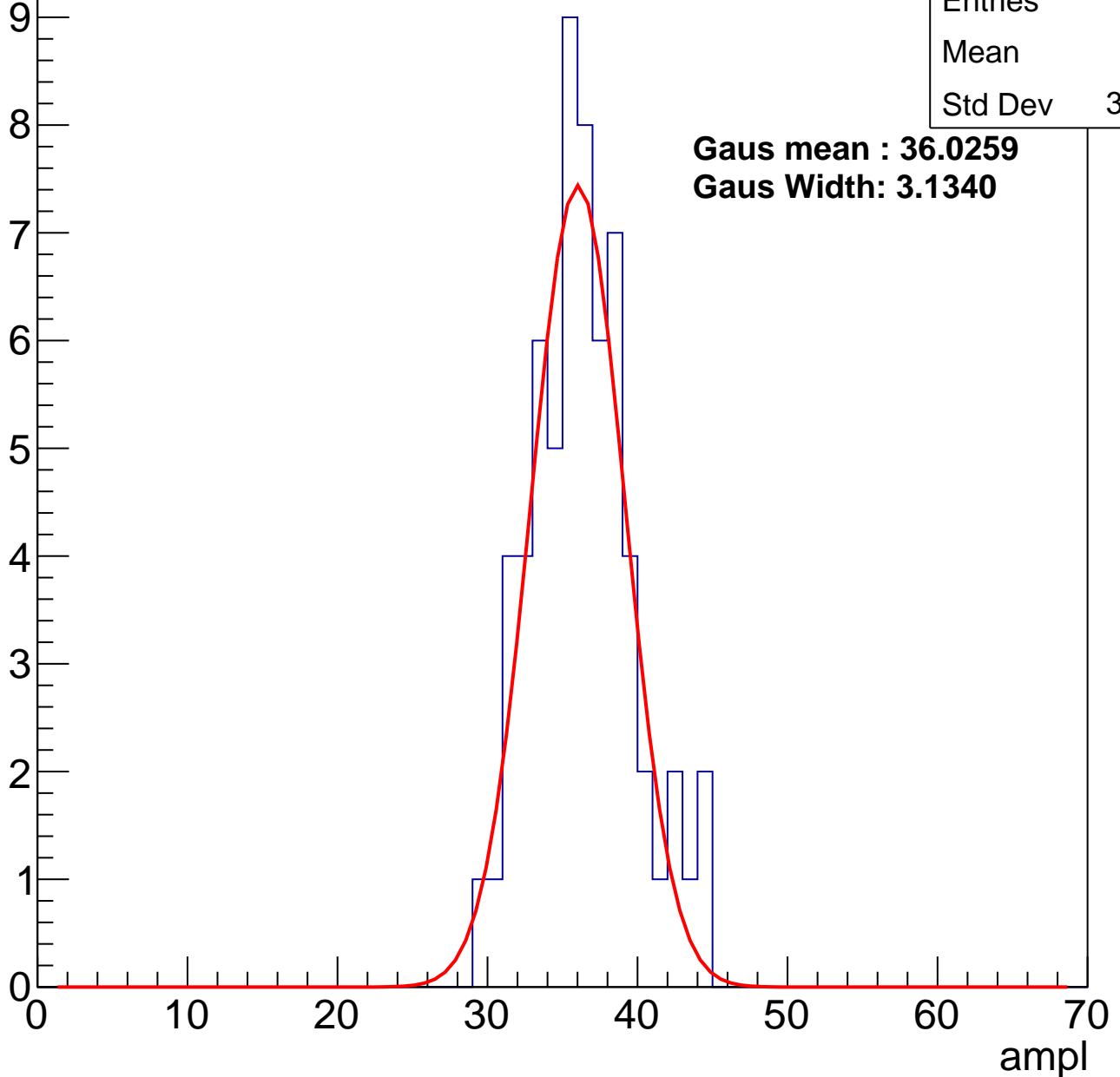
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	63
Mean	35.9
Std Dev	3.351

**Gaus mean : 36.0259**

**Gaus Width: 3.1340**



# B1L100S, U6-ch113, adc2

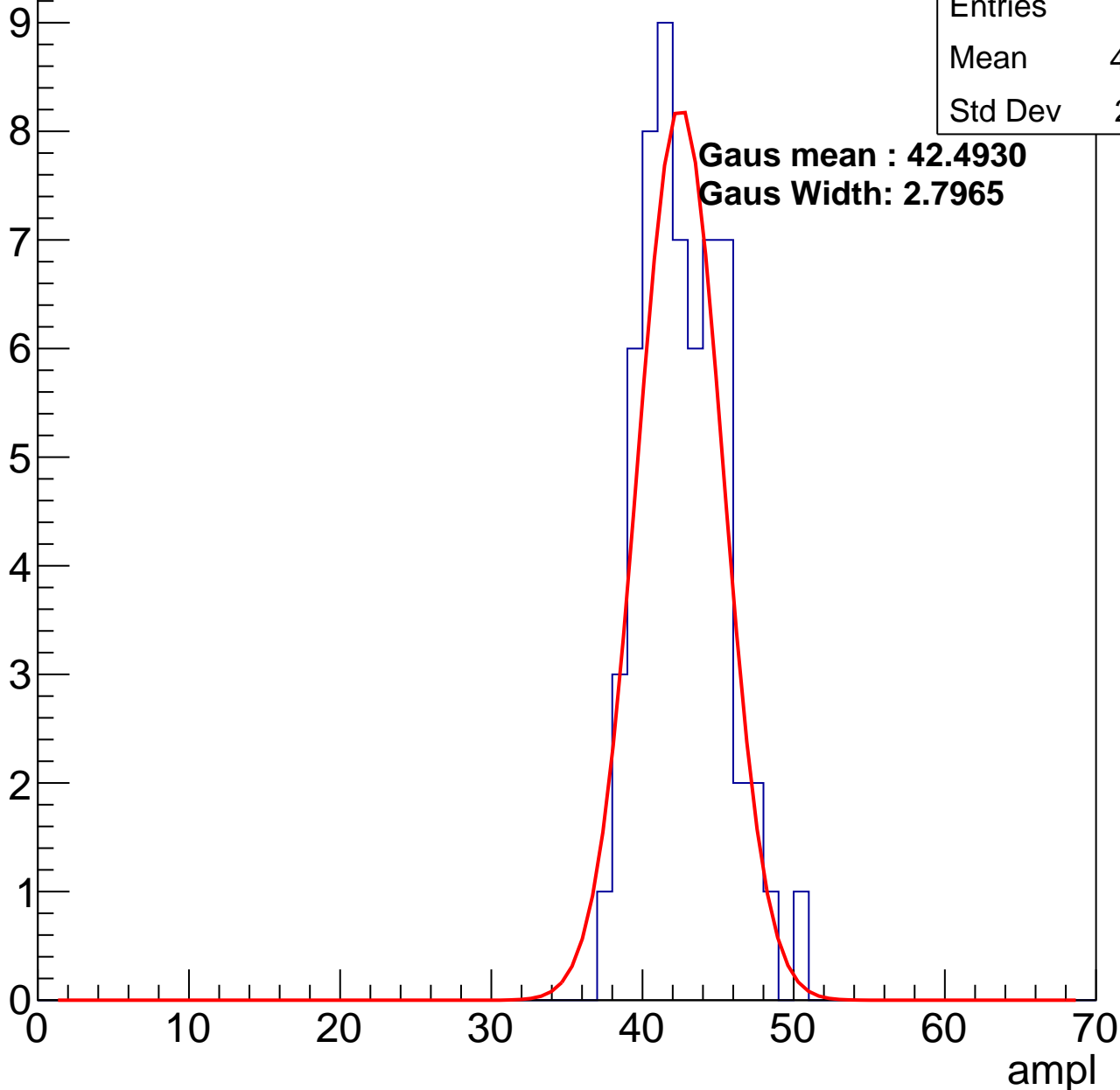
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	60
Mean	42.22
Std Dev	2.721

**Gaus mean : 42.4930**

**Gaus Width: 2.7965**



# B1L100S, U6-ch113, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

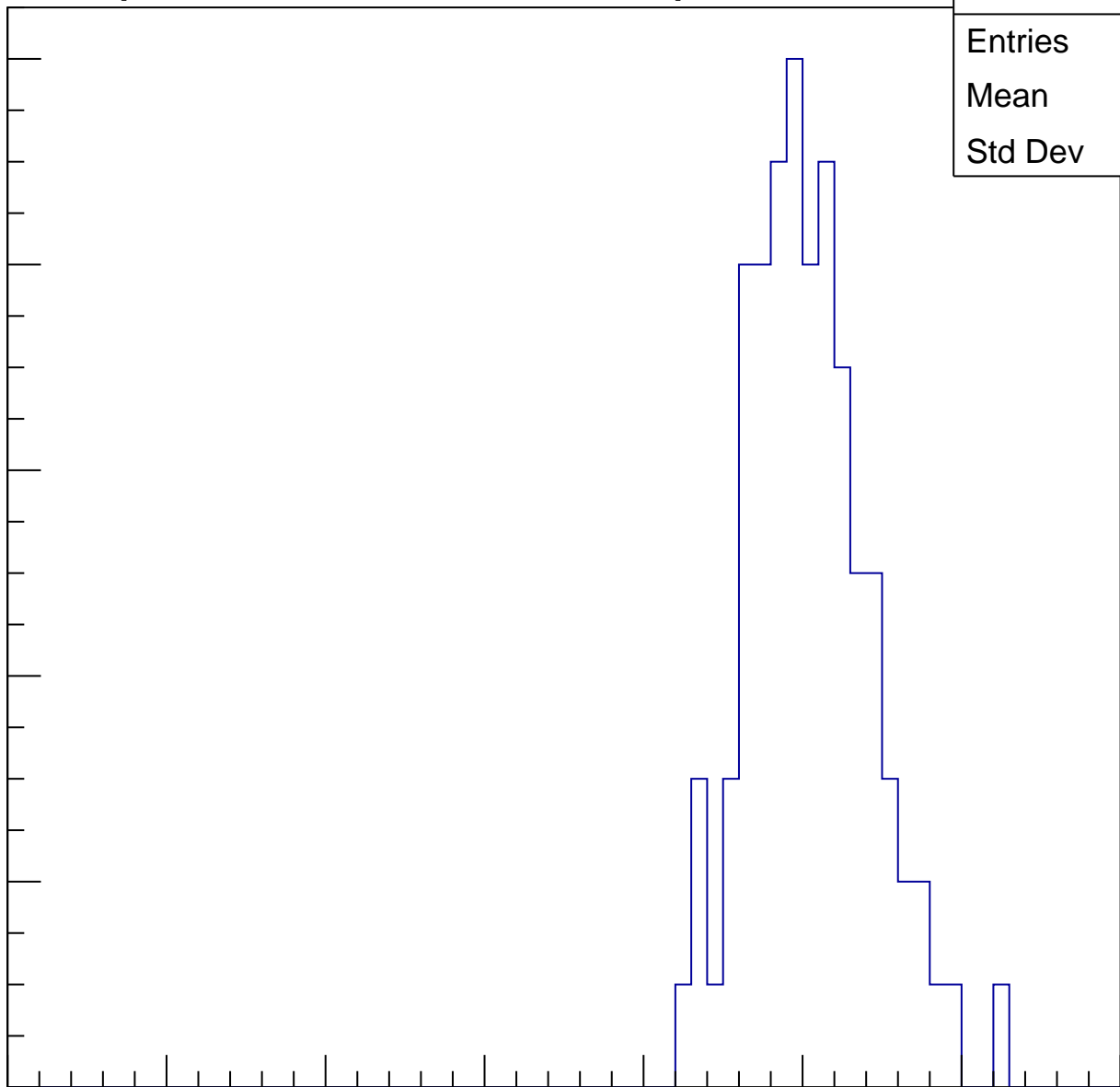
Entries	87
Mean	49.93
Std Dev	3.811

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B1L100S, U6-ch113, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

7

6

5

4

3

2

1

0

Entries 55

Mean 56.42

Std Dev 2.865

ampl

0

10

20

30

40

50

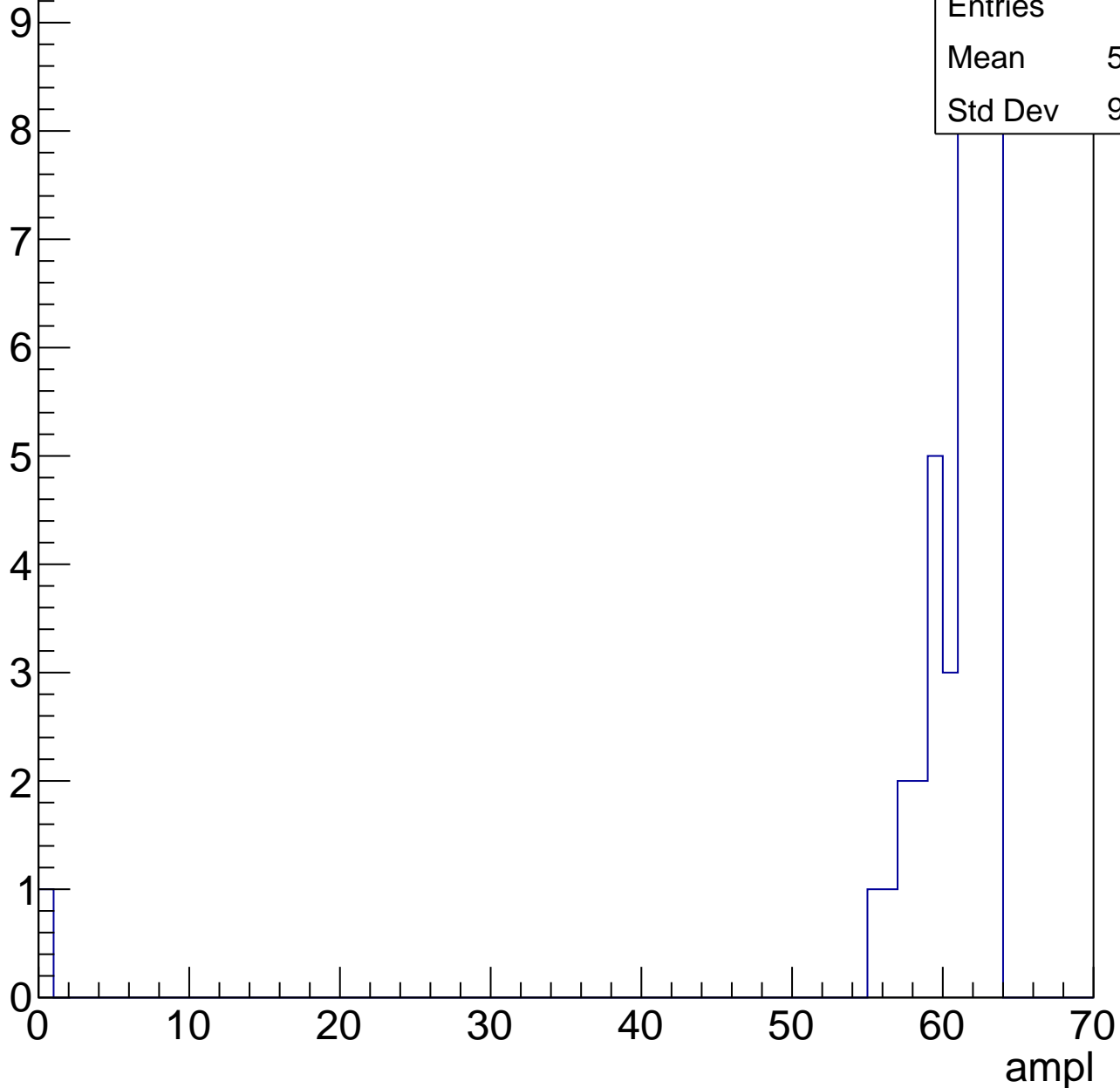
60

70

# B1L100S, U6-ch113, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



# B1L100S, U6-ch113, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	0
Mean	0
Std Dev	0



# B1L100S, U6-ch113, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



# B1L100S, U6-ch114, adc0

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	66
Mean	28.74
Std Dev	4.949

**Gaus mean : 29.7768**

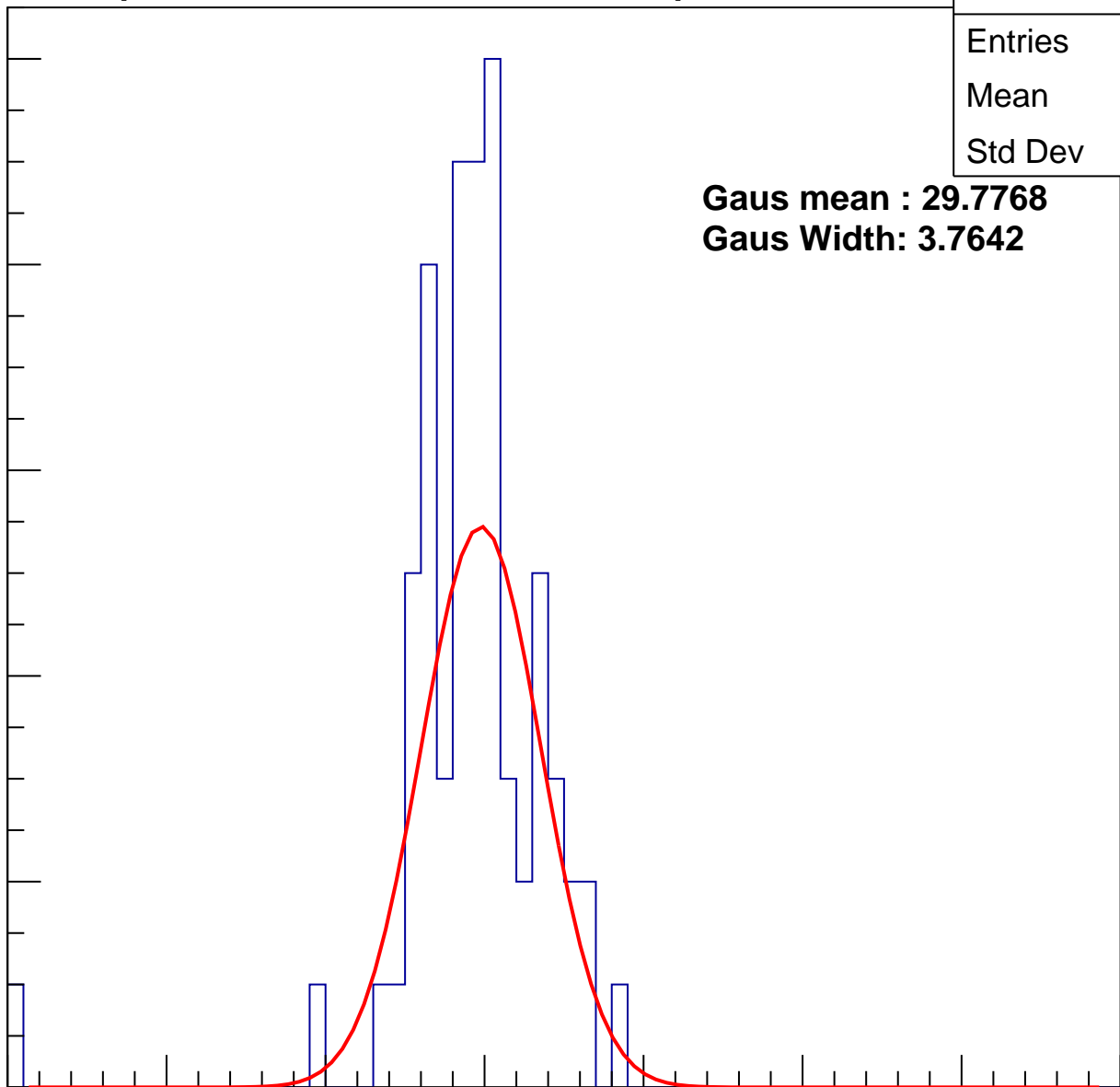
**Gaus Width: 3.7642**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L100S, U6-ch114, adc1

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	66
Mean	35.24
Std Dev	3.22

**Gaus mean : 35.8027**

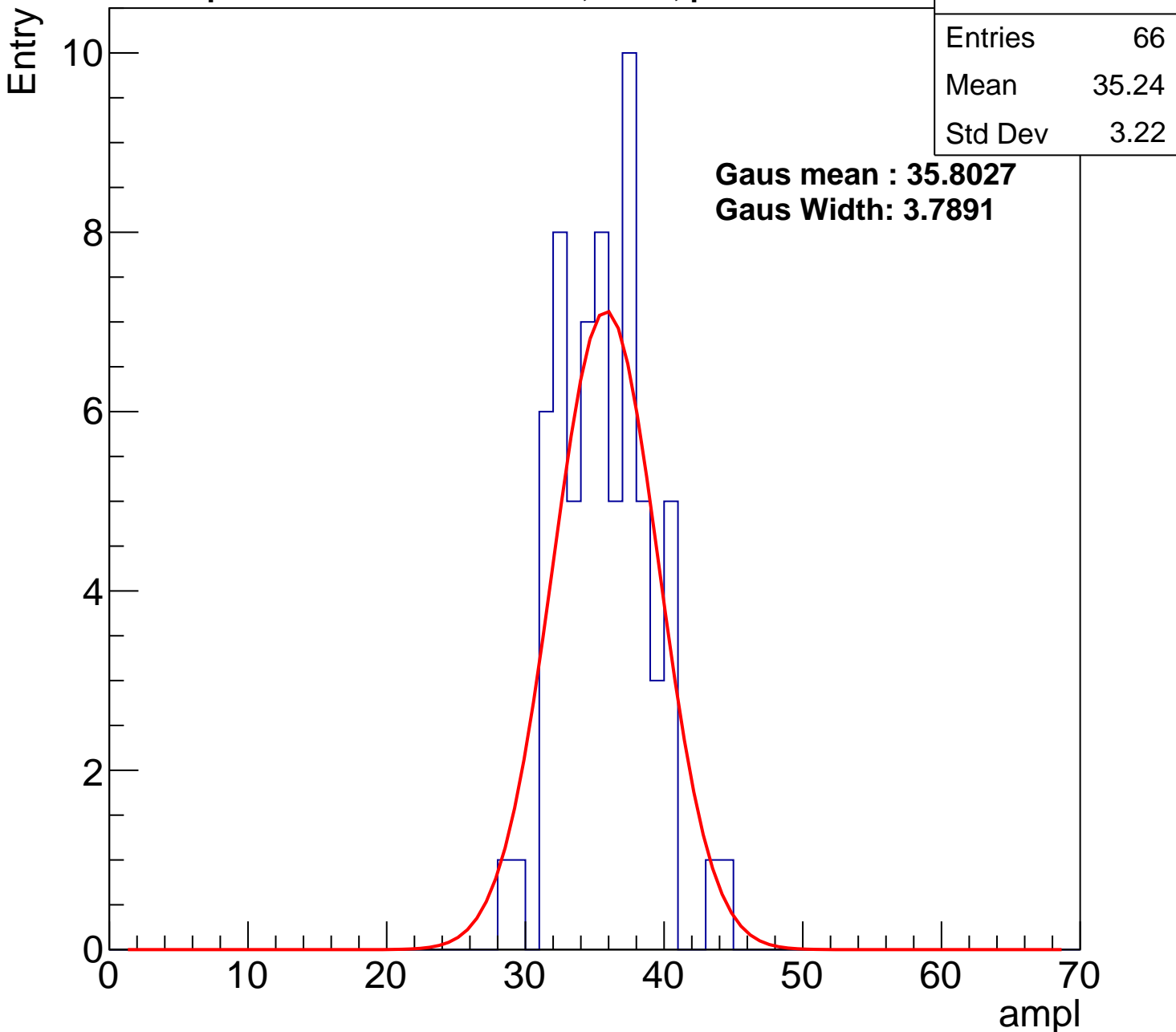
**Gaus Width: 3.7891**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B1L100S, U6-ch114, adc2

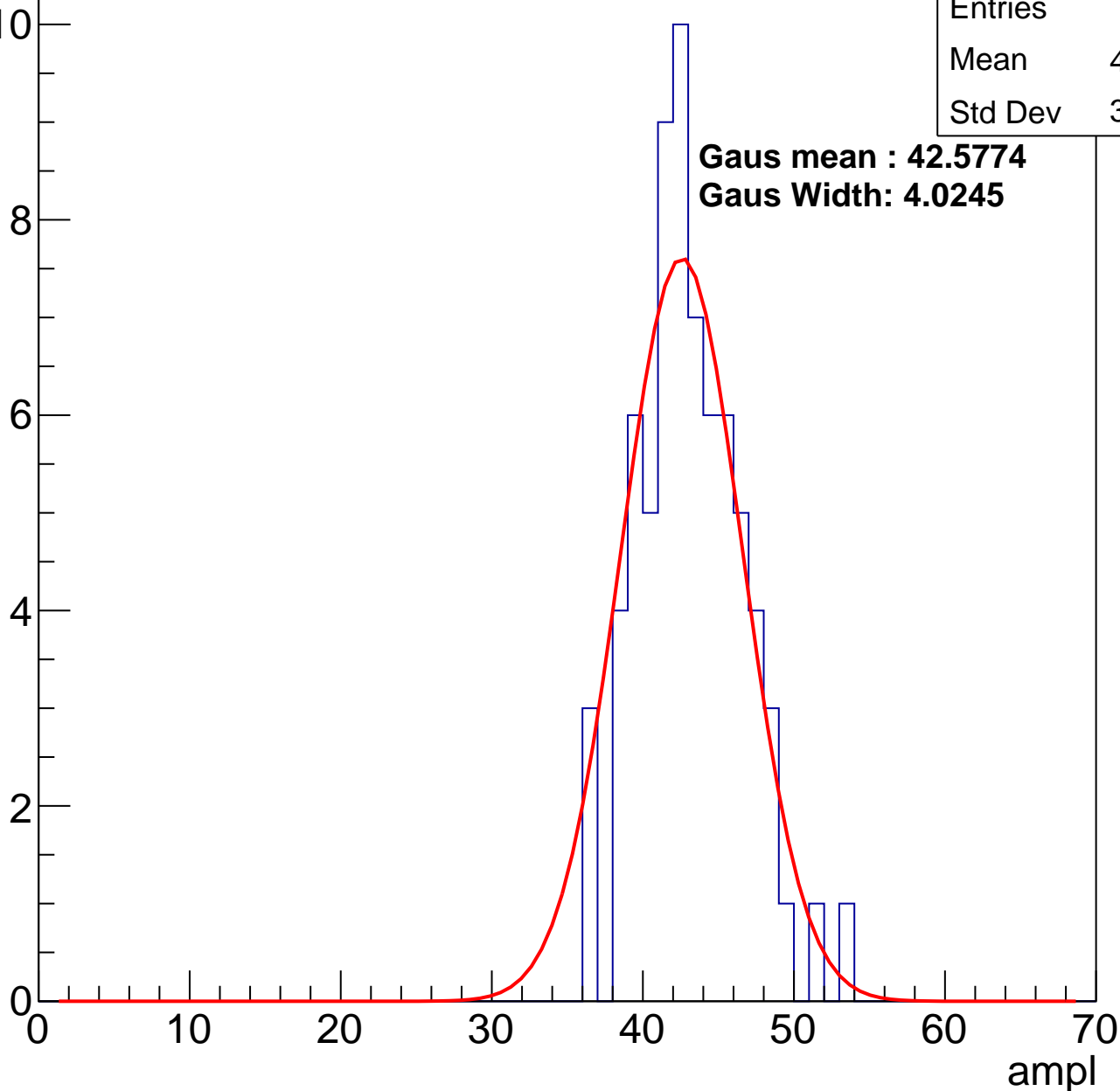
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	71
Mean	42.72
Std Dev	3.444

**Gaus mean : 42.5774**

**Gaus Width: 4.0245**

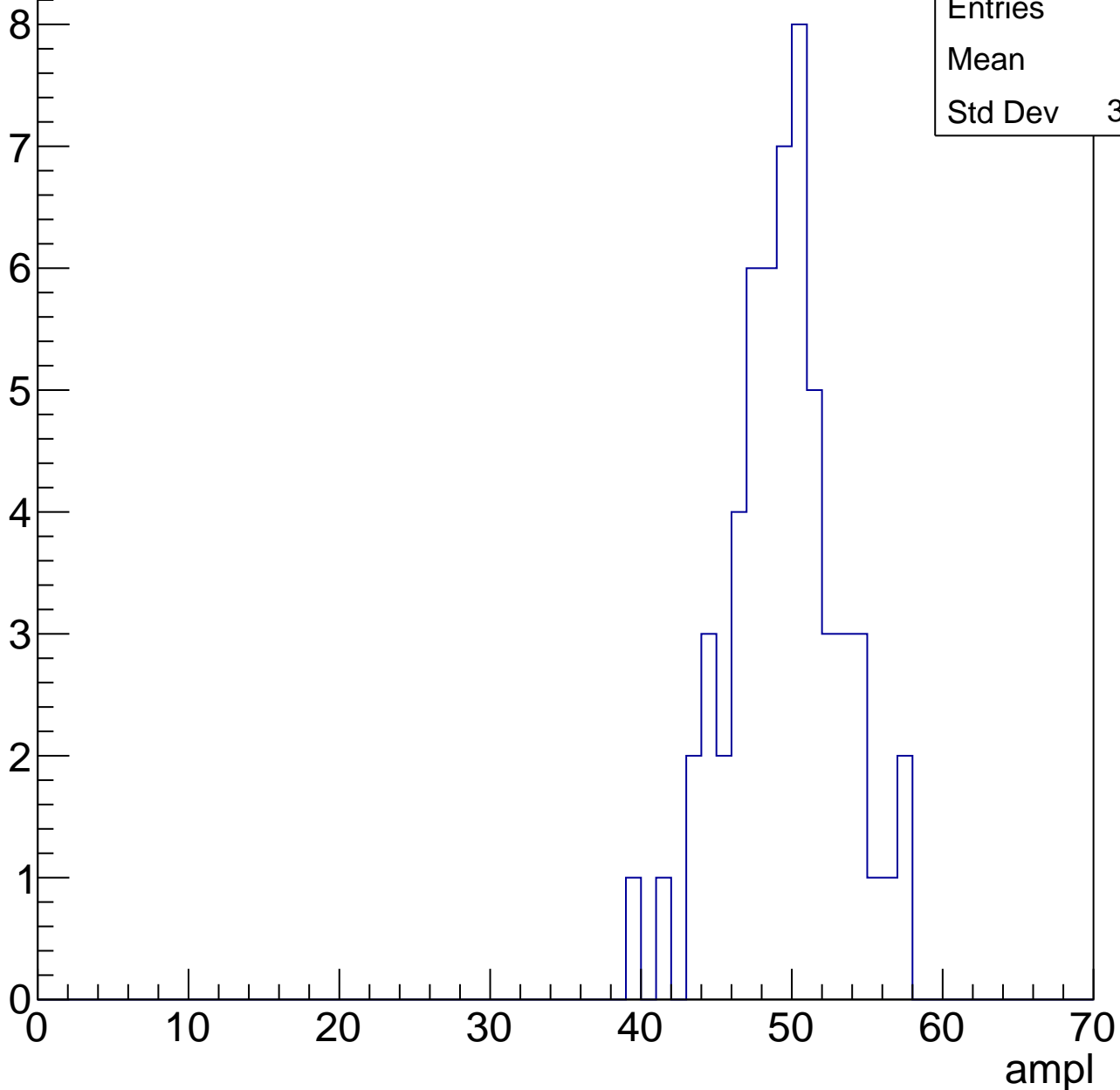


# B1L100S, U6-ch114, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	58
Mean	49
Std Dev	3.714

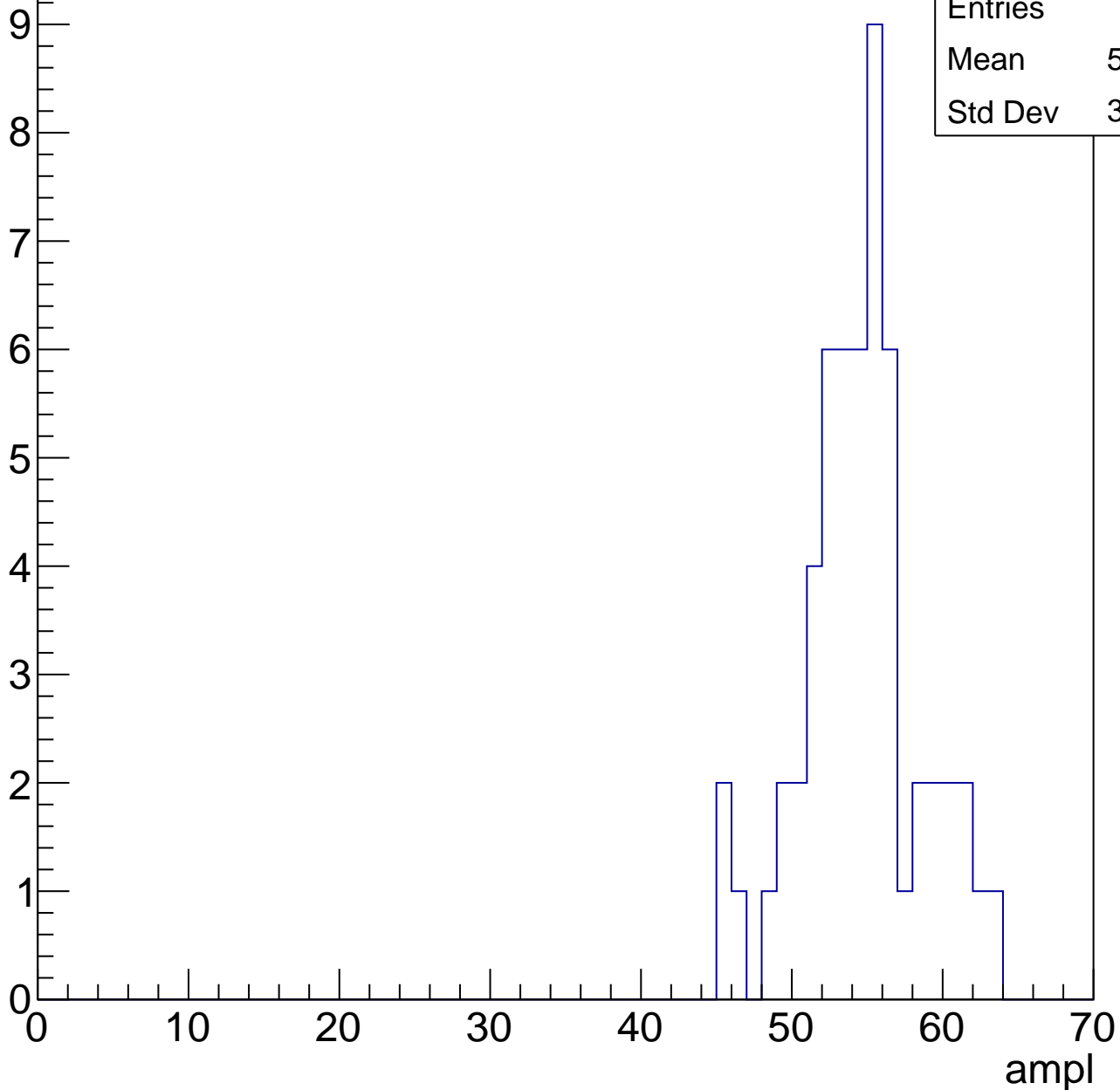


# B1L100S, U6-ch114, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	56
Mean	54.09
Std Dev	3.893

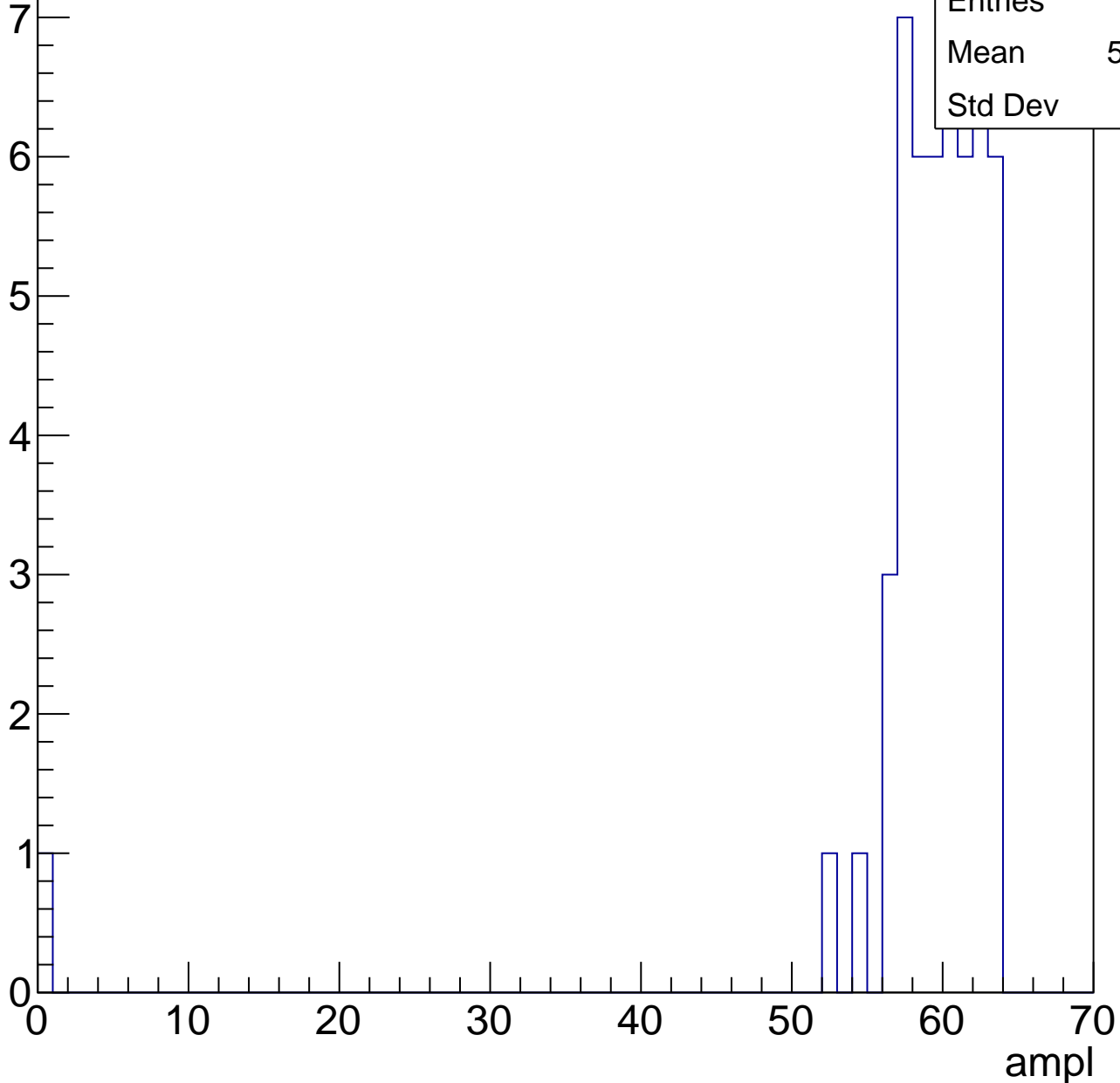


# B1L100S, U6-ch114, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

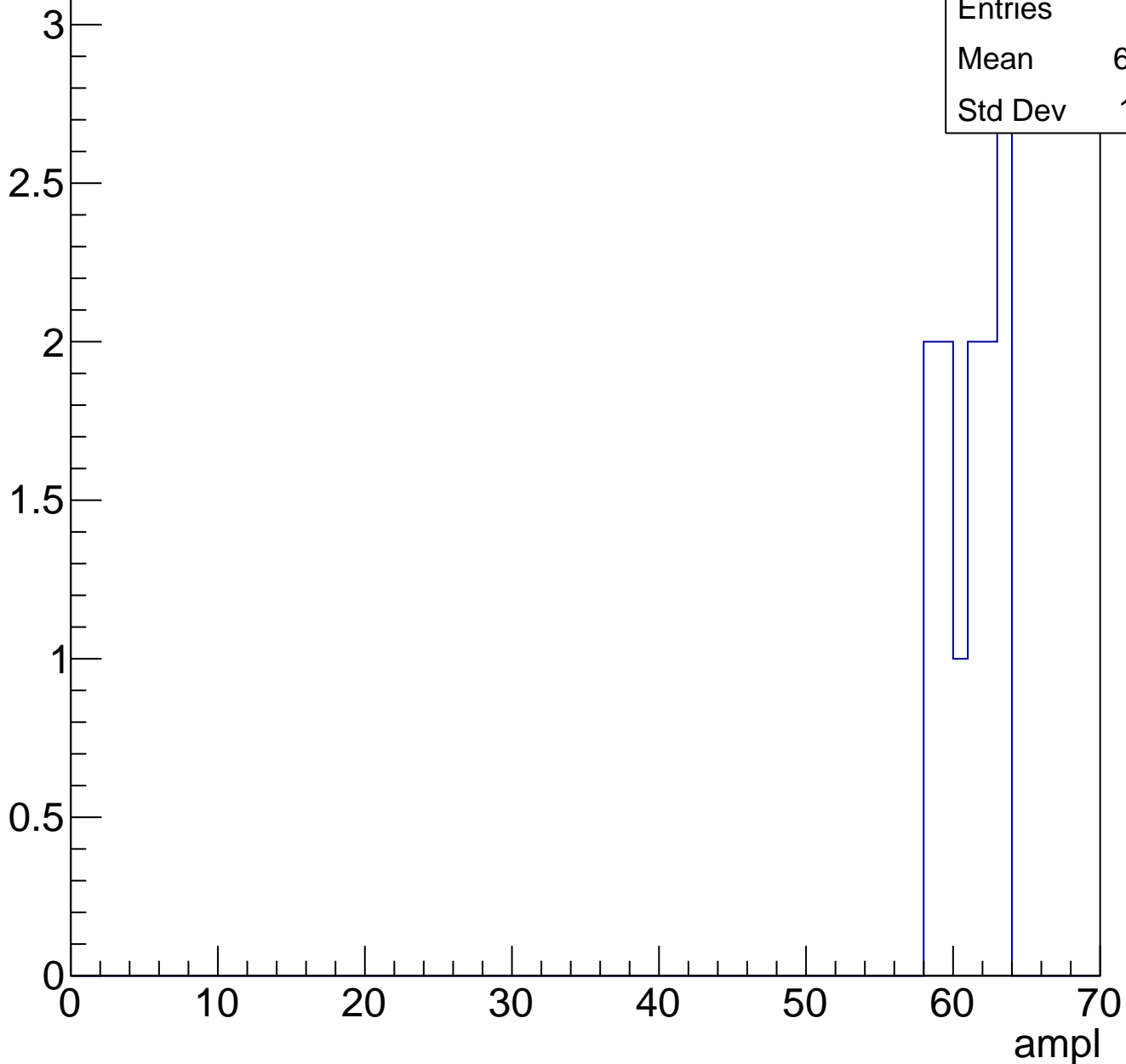
Entries	51
Mean	58.29
Std Dev	8.61



# B1L100S, U6-ch114, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry





# B1L100S, U6-ch114, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L100S, U6-ch115, adc0

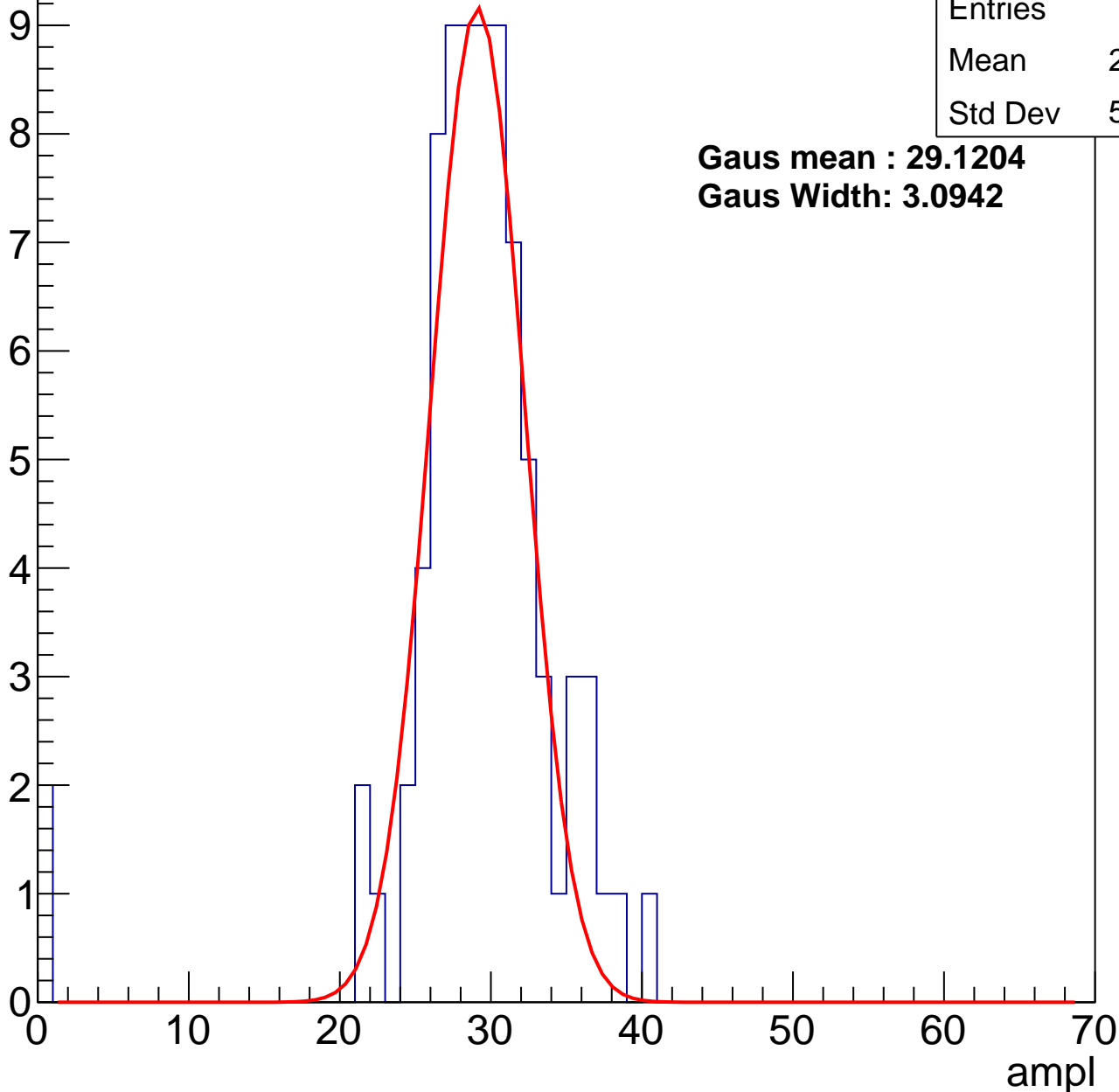
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	80
Mean	28.55
Std Dev	5.863

**Gaus mean : 29.1204**

**Gaus Width: 3.0942**



# B1L100S, U6-ch115, adc1

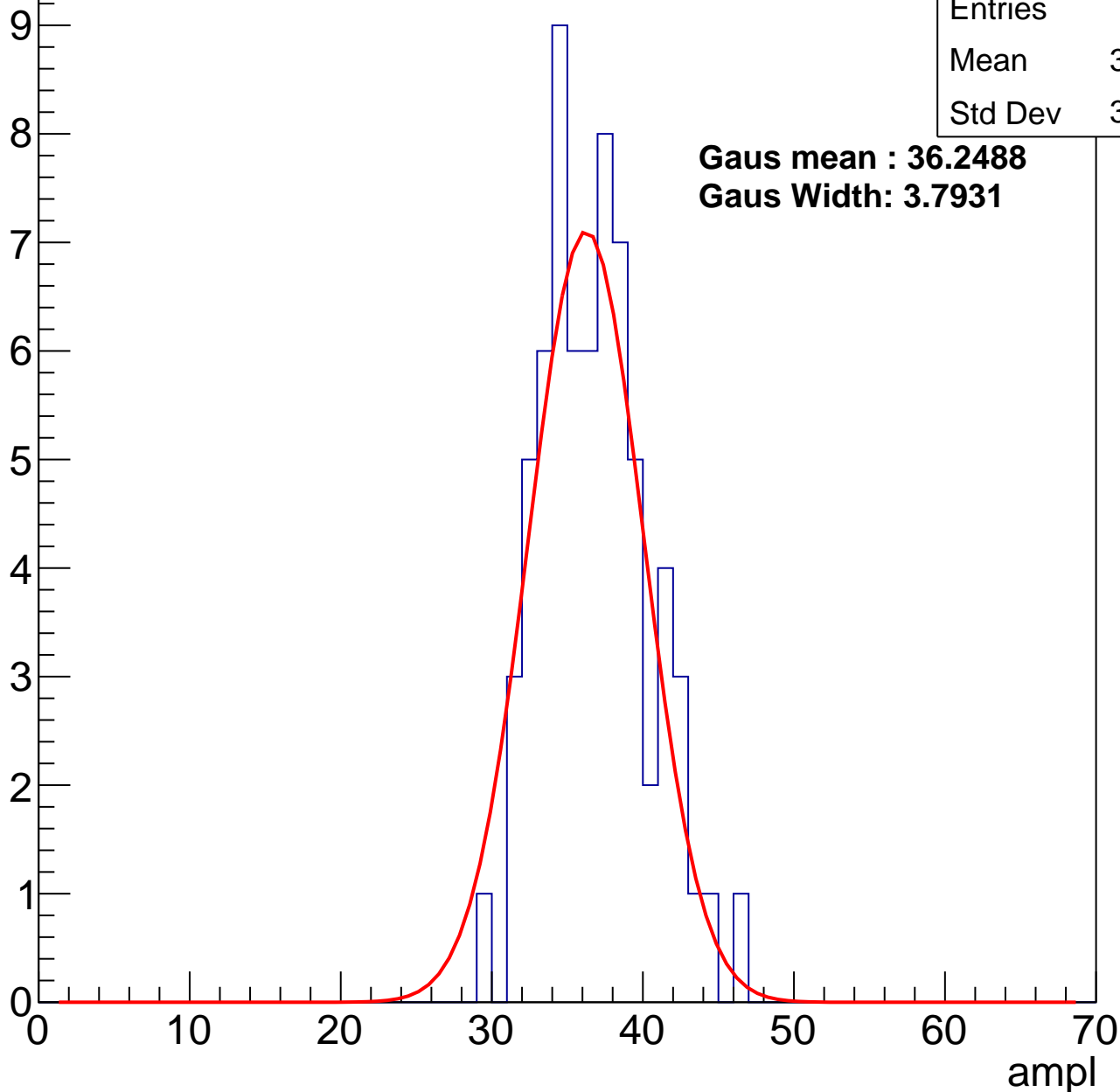
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	68
Mean	36.35
Std Dev	3.484

**Gaus mean : 36.2488**

**Gaus Width: 3.7931**



# B1L100S, U6-ch115, adc2

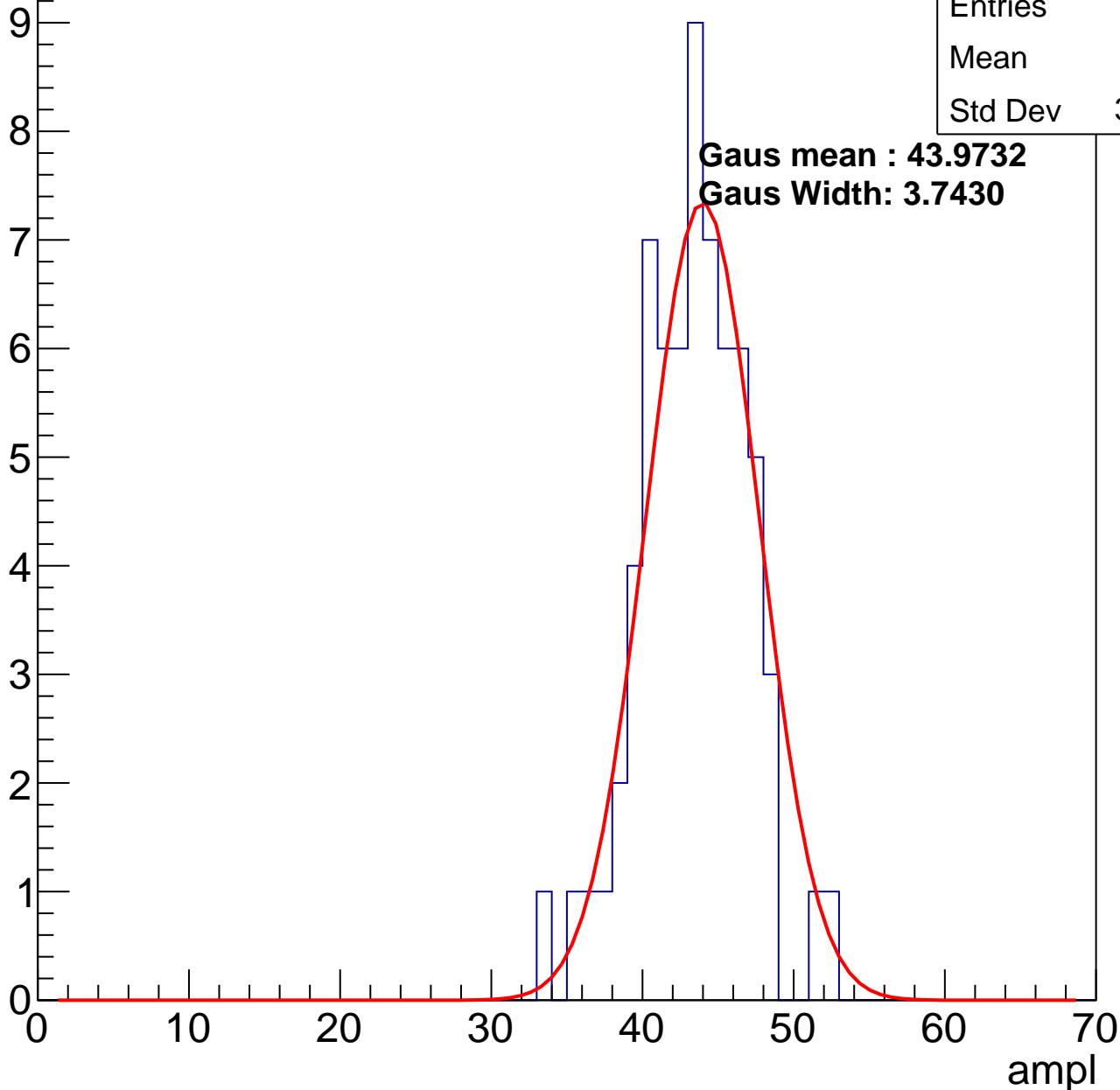
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	67
Mean	42.9
Std Dev	3.541

**Gaus mean : 43.9732**

**Gaus Width: 3.7430**

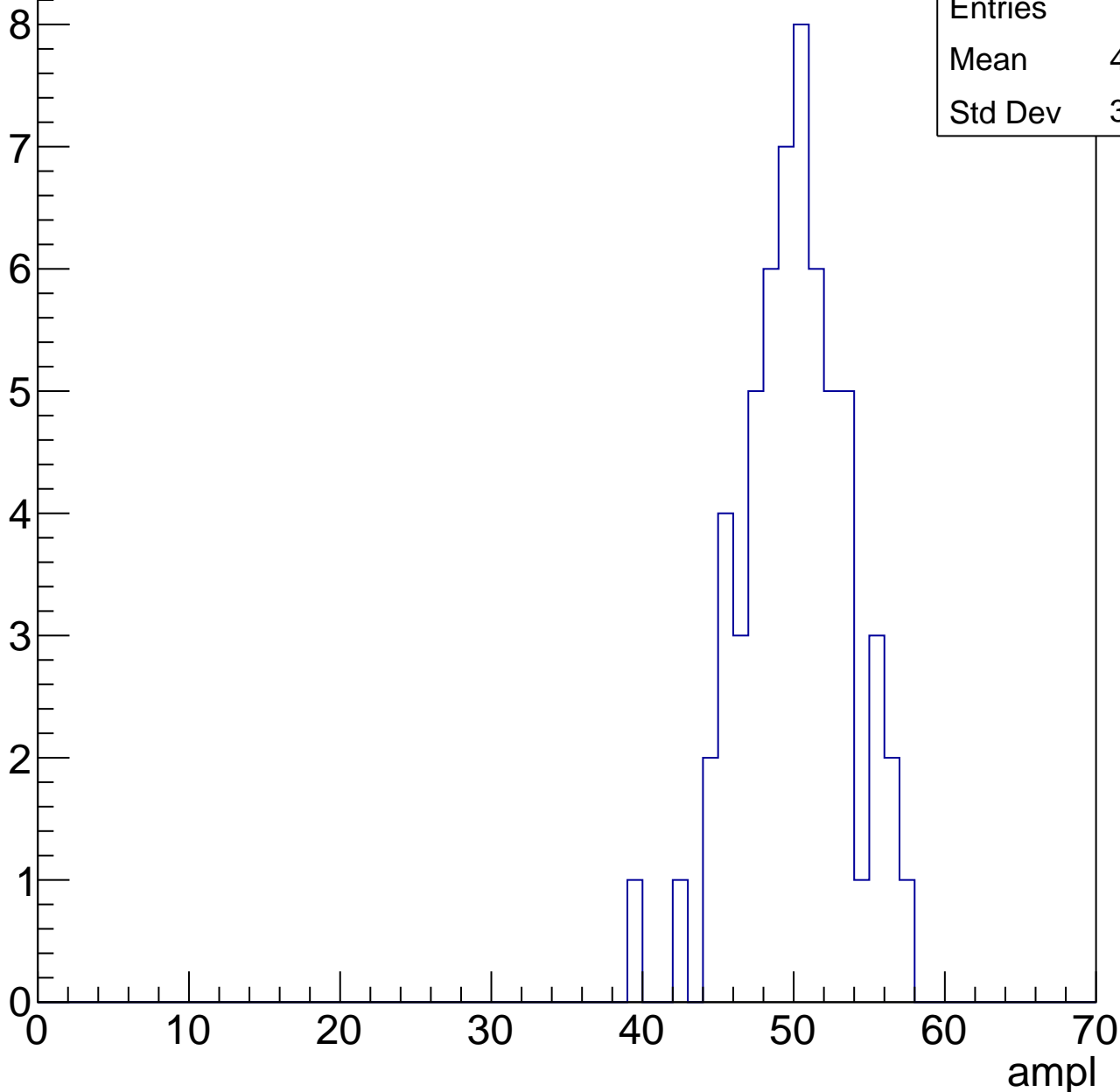


# B1L100S, U6-ch115, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	60
Mean	49.53
Std Dev	3.538

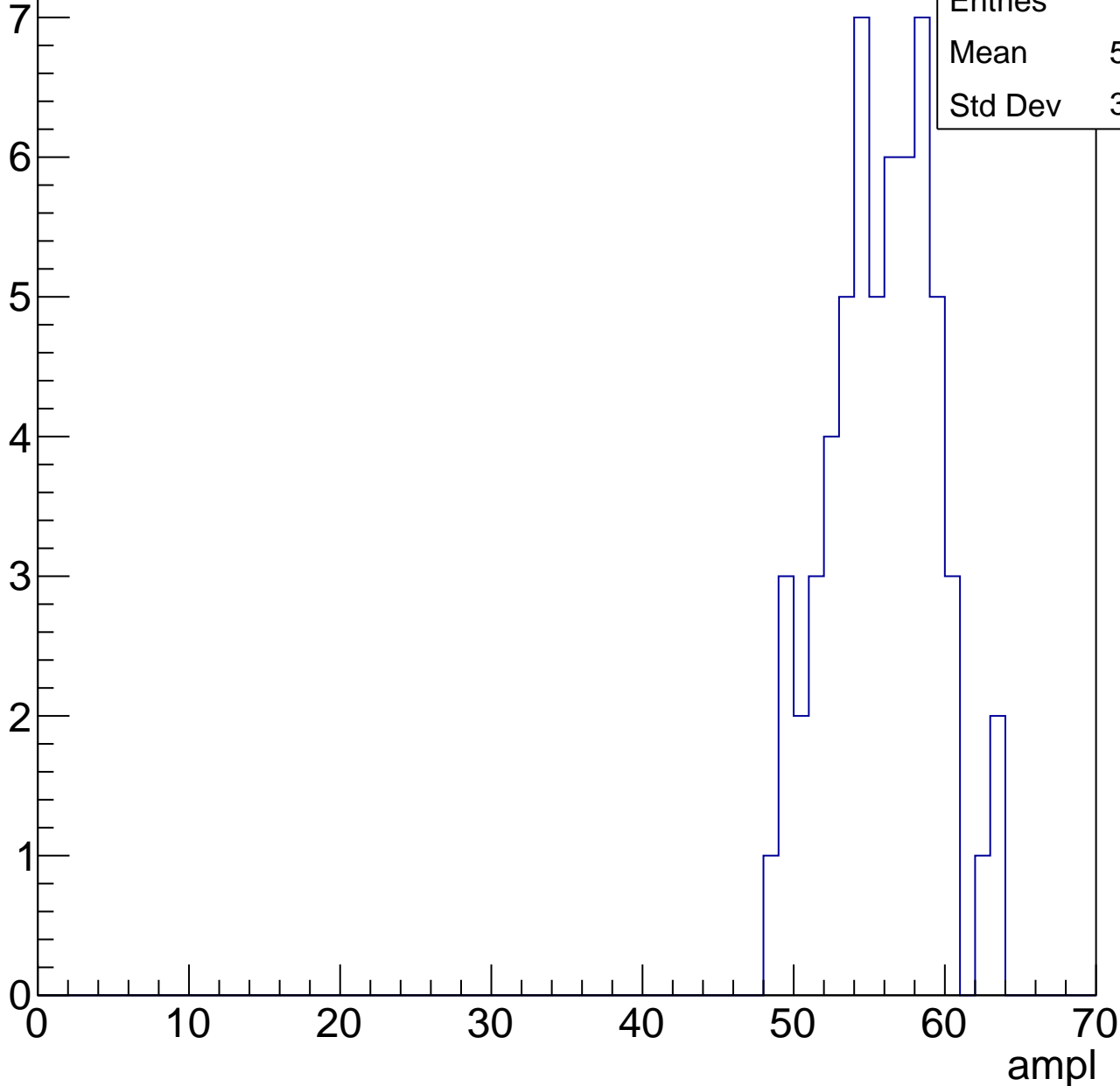


# B1L100S, U6-ch115, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	60
Mean	55.35
Std Dev	3.502

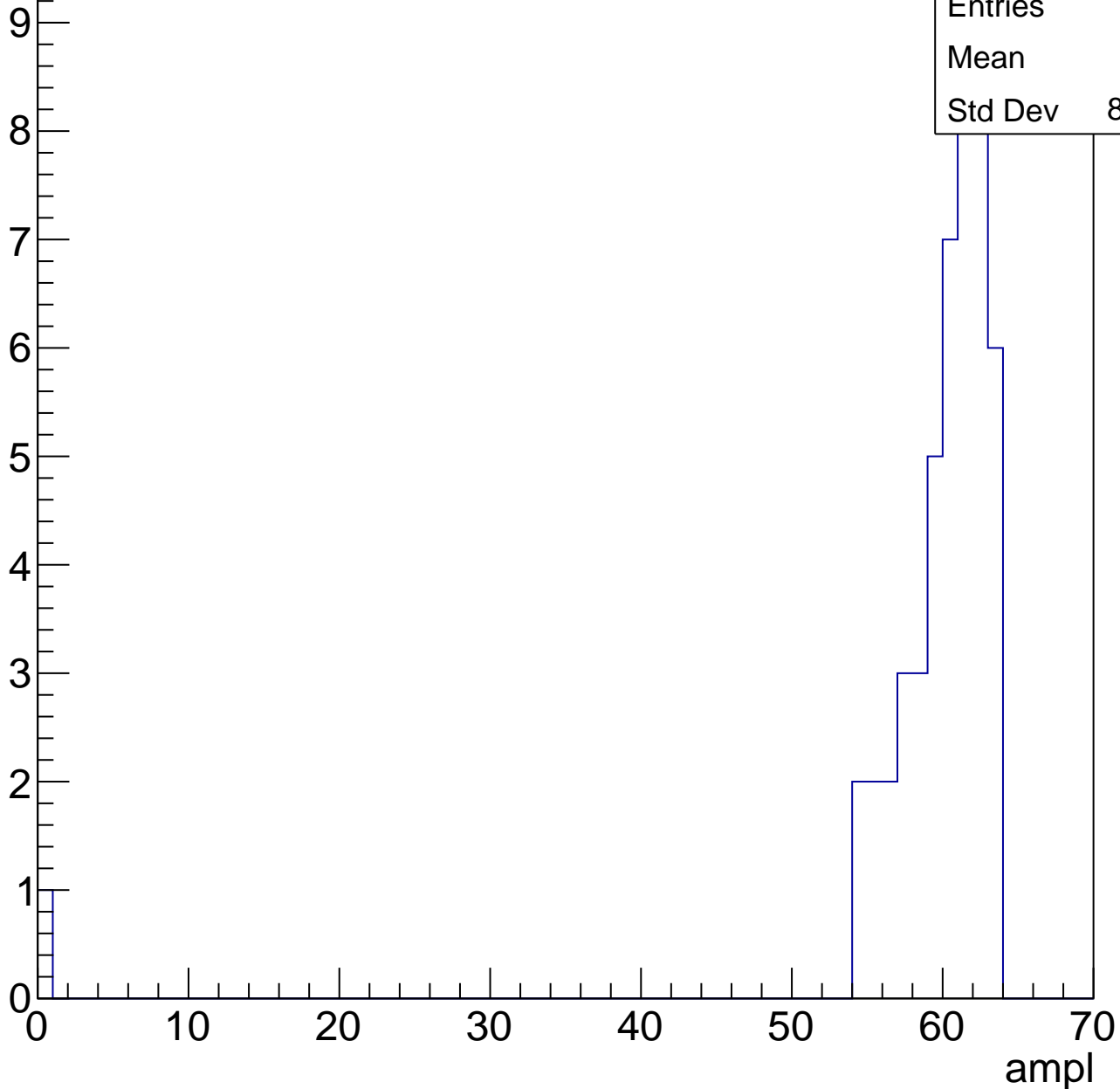


# B1L100S, U6-ch115, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	48
Mean	58.6
Std Dev	8.897



# B1L100S, U6-ch115, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	4
Mean	62.25
Std Dev	0.8292

ampl

0 10 20 30 40 50 60 70



# B1L100S, U6-ch115, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	2
Mean	9.5
Std Dev	9.5

# B1L100S, U6-ch116, adc0

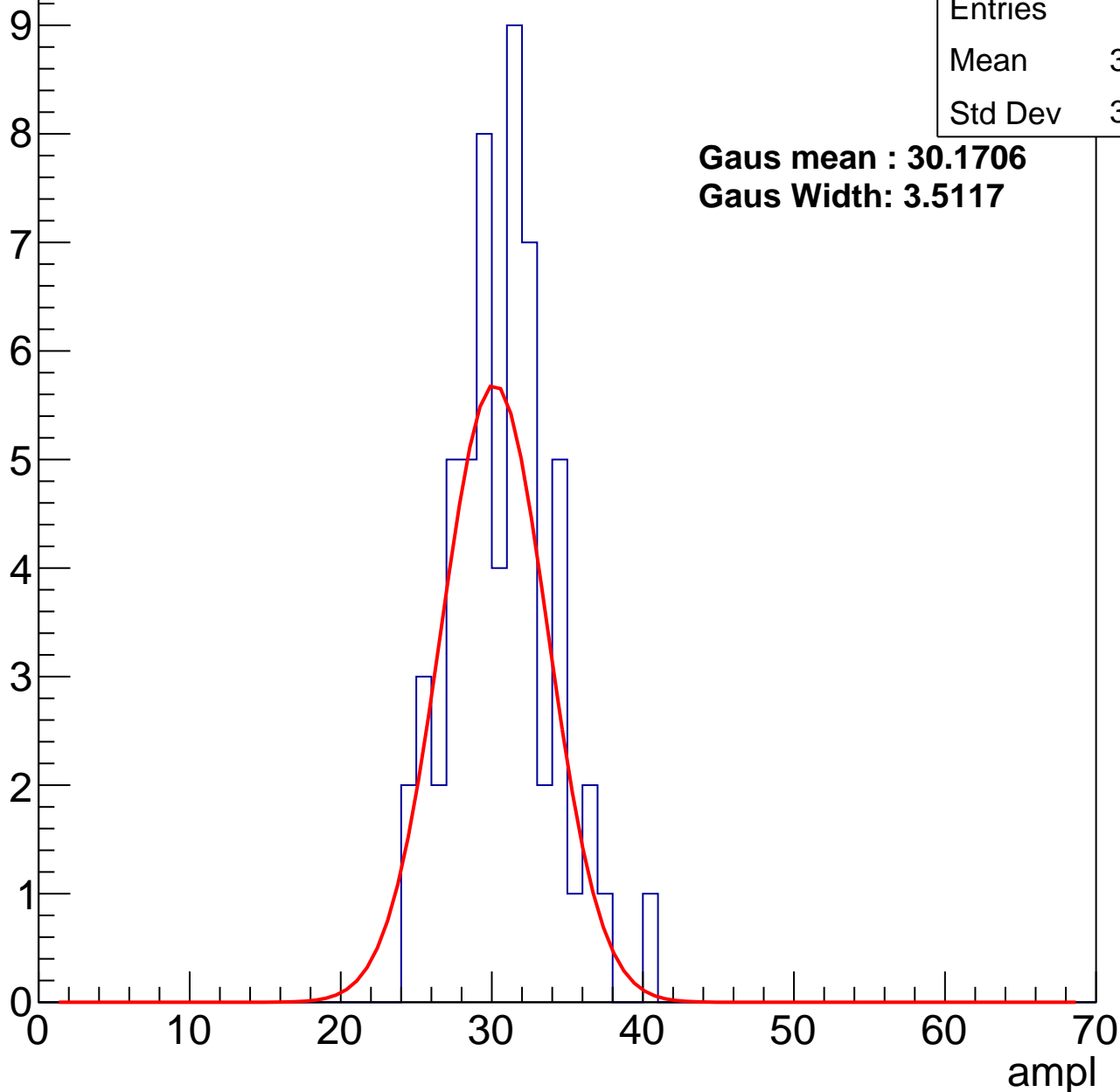
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	57
Mean	30.26
Std Dev	3.322

**Gaus mean : 30.1706**

**Gaus Width: 3.5117**



# B1L100S, U6-ch116, adc1

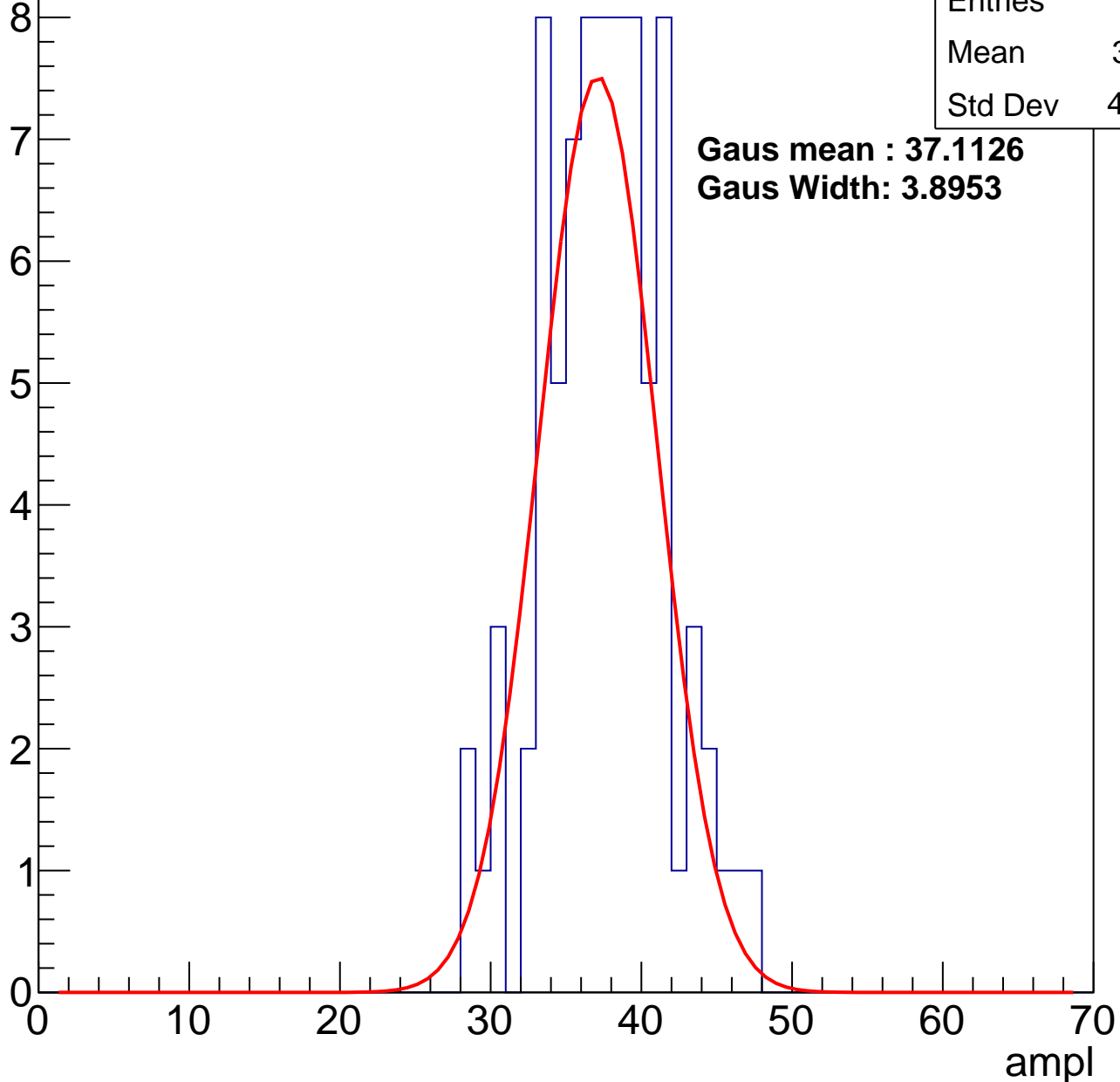
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	82
Mean	37.11
Std Dev	4.012

**Gaus mean : 37.1126**

**Gaus Width: 3.8953**



# B1L100S, U6-ch116, adc2

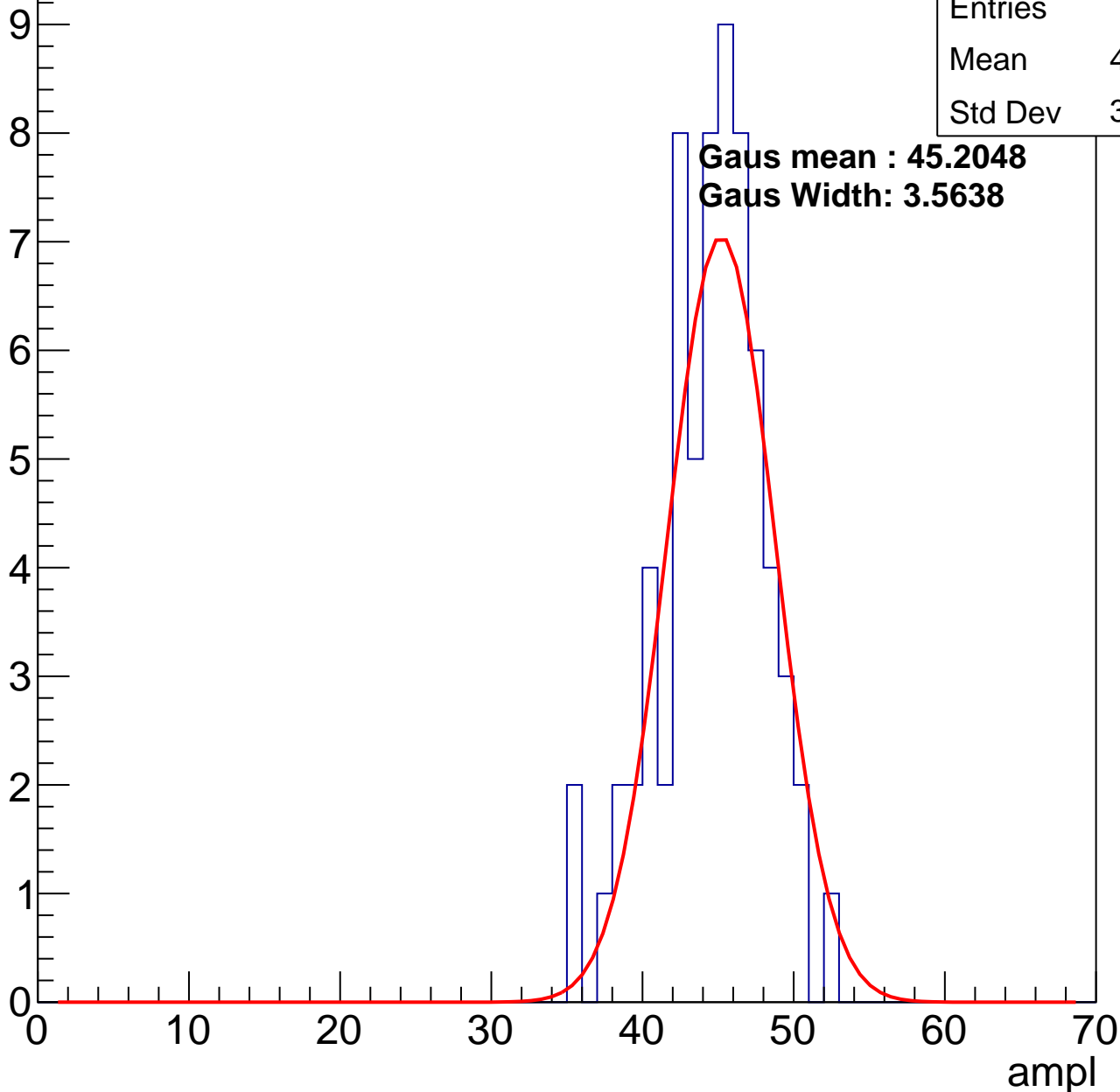
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	67
Mean	44.06
Std Dev	3.502

**Gaus mean : 45.2048**

**Gaus Width: 3.5638**

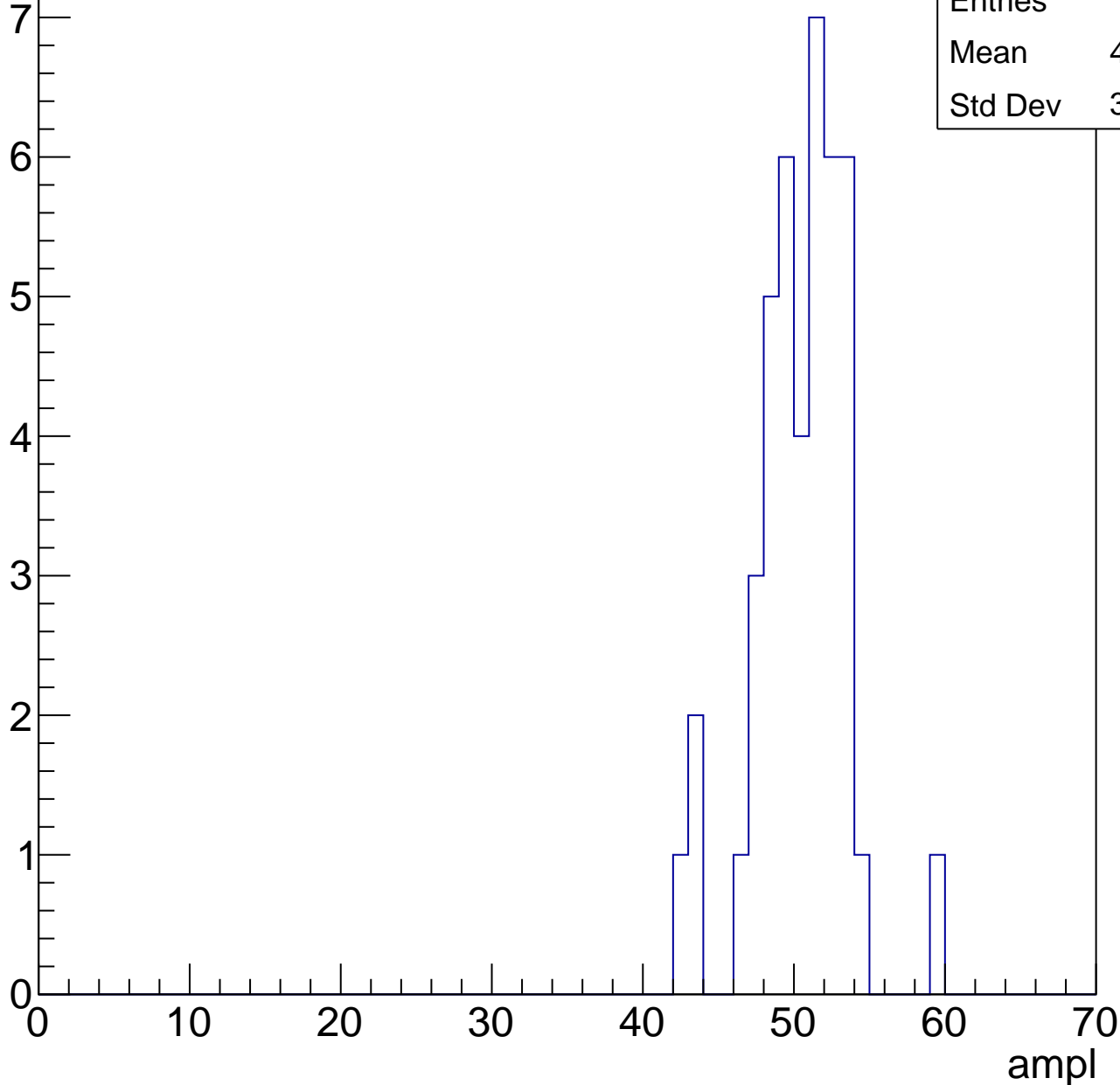


# B1L100S, U6-ch116, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	43
Mean	49.98
Std Dev	3.099

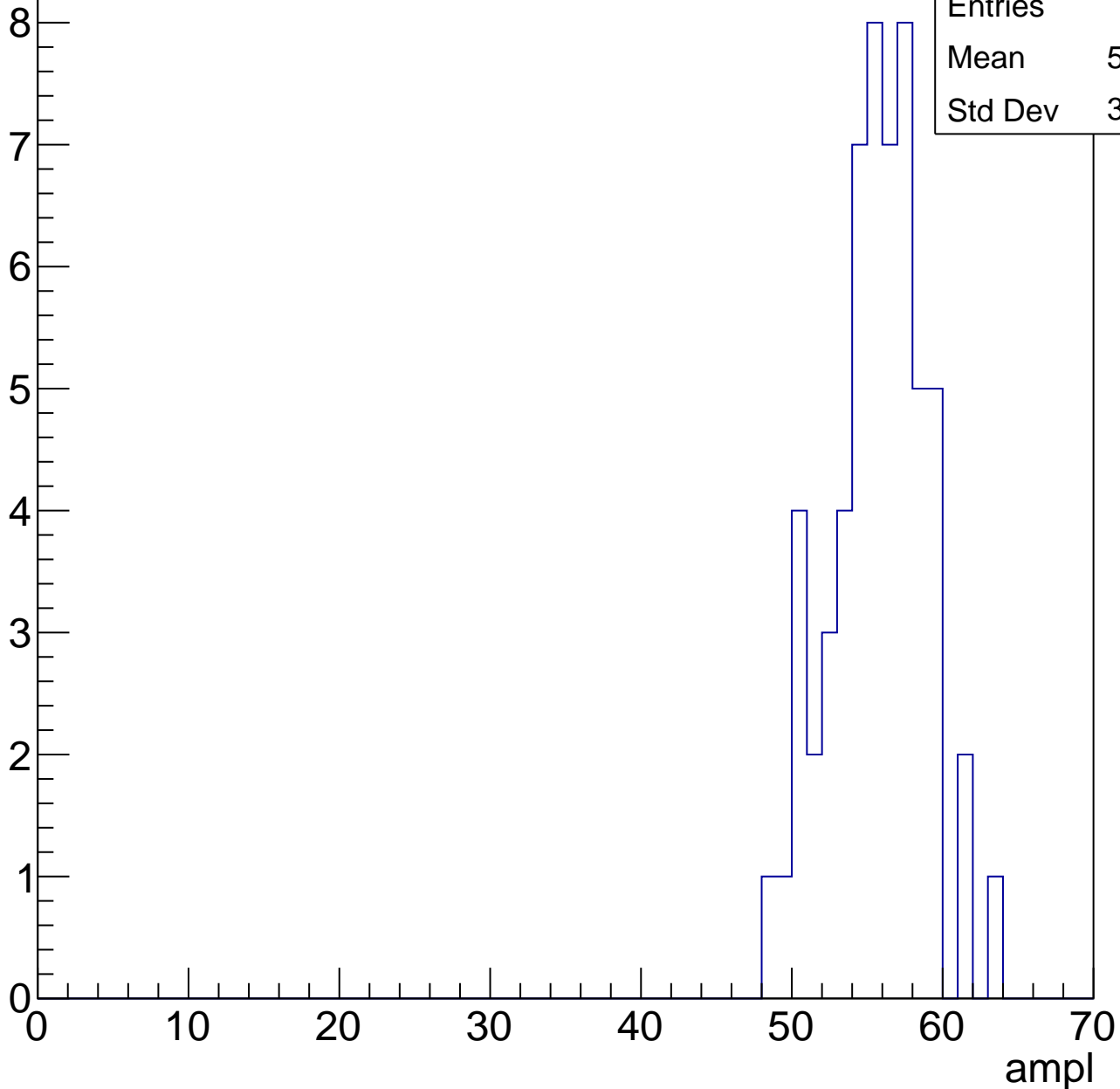


# B1L100S, U6-ch116, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	58
Mean	55.22
Std Dev	3.119

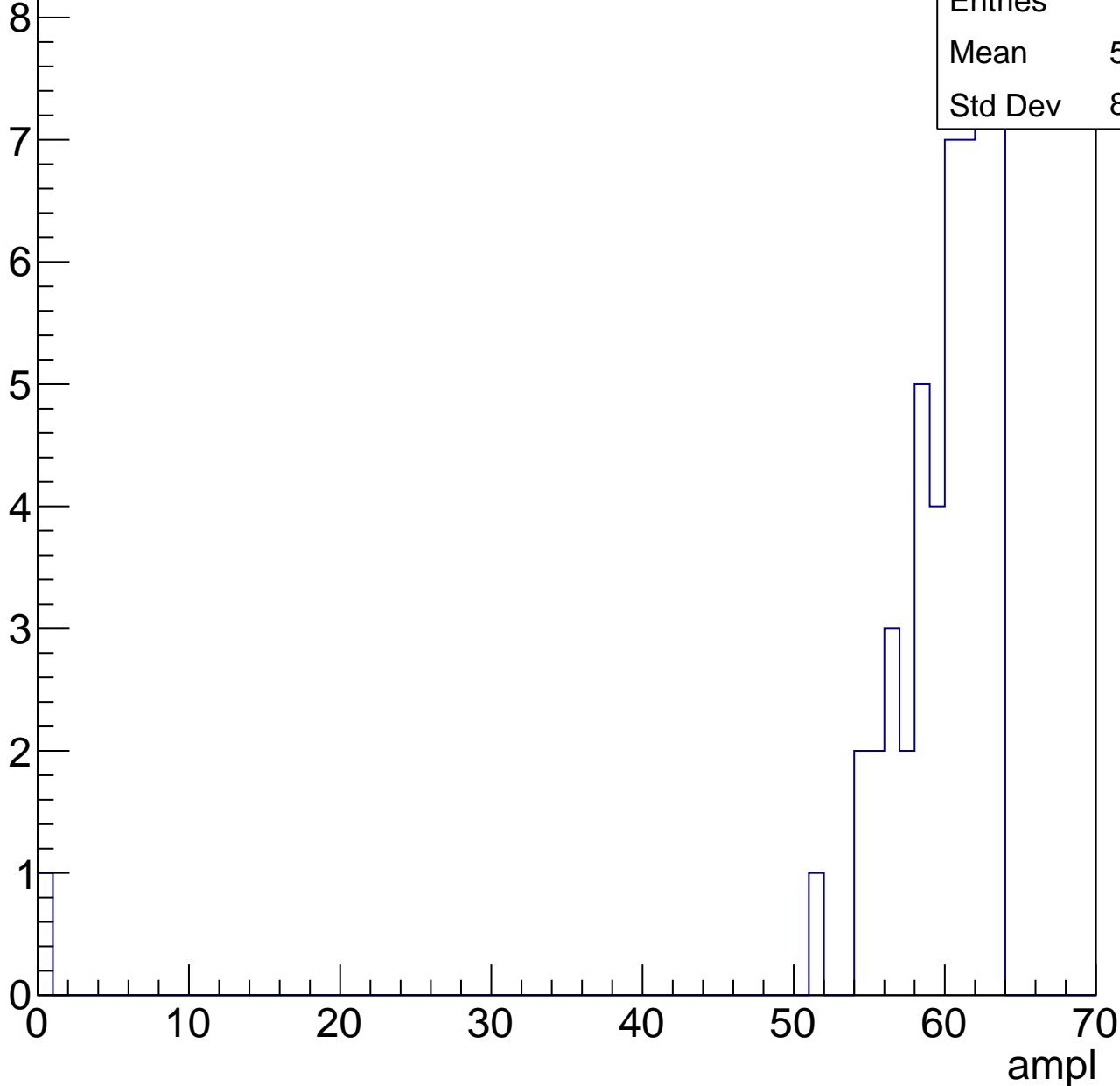


# B1L100S, U6-ch116, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

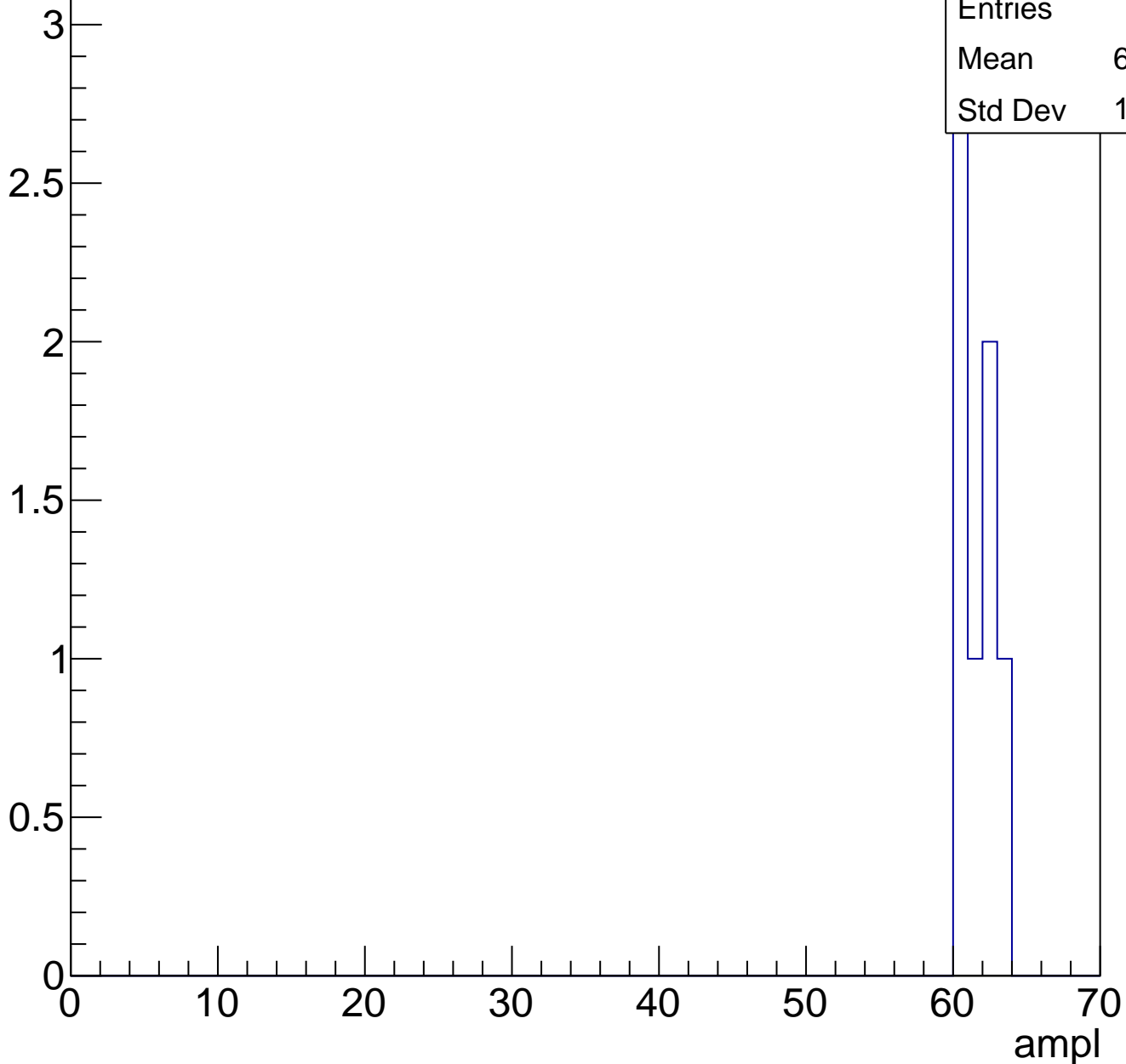
Entries	50
Mean	58.48
Std Dev	8.819



# B1L100S, U6-ch116, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	7
Mean	61.14
Std Dev	1.125



# B1L100S, U6-ch116, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L100S, U6-ch117, adc0

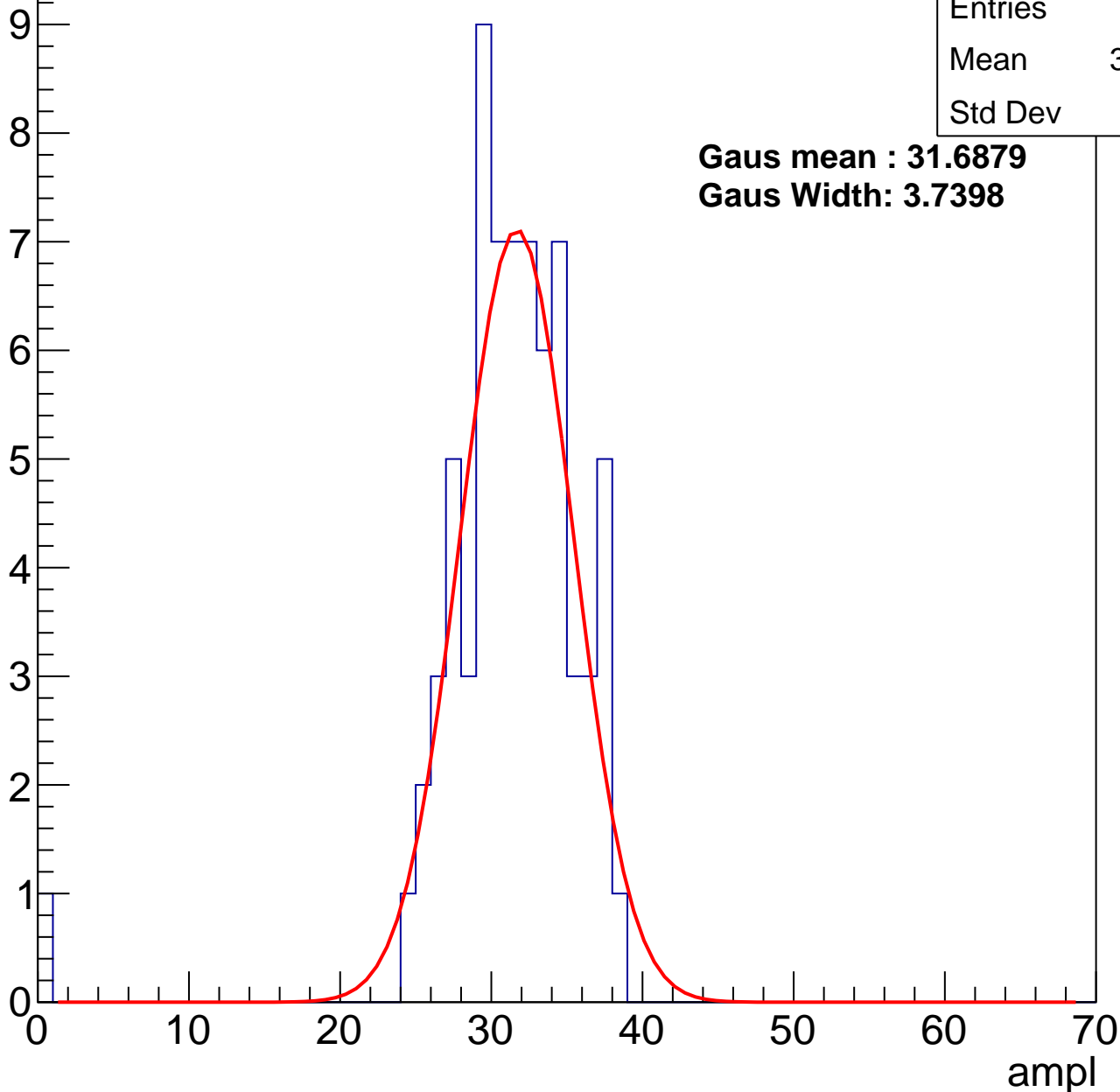
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	70
Mean	30.79
Std Dev	5

**Gaus mean : 31.6879**

**Gaus Width: 3.7398**



# B1L100S, U6-ch117, adc1

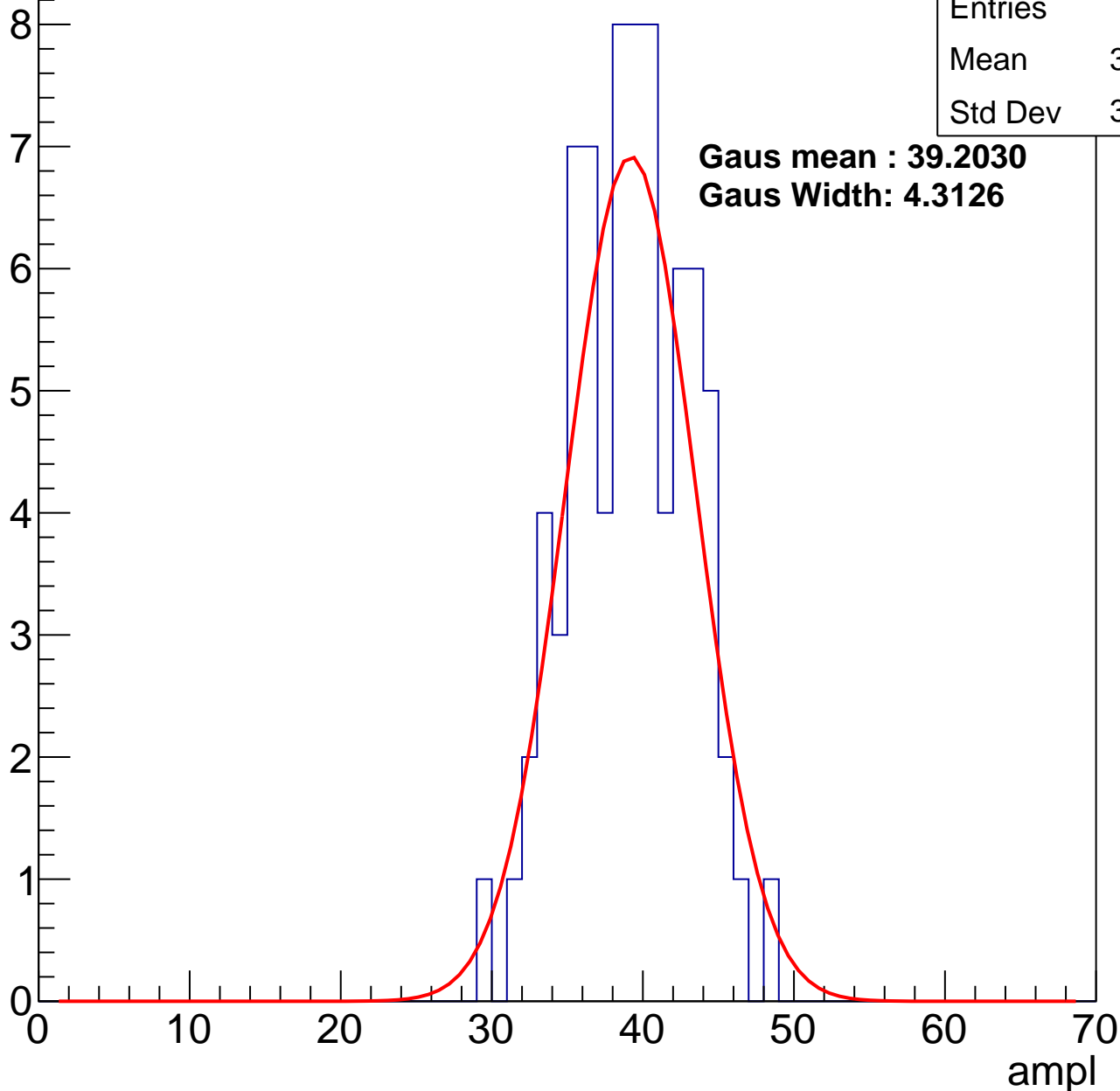
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	78
Mean	38.68
Std Dev	3.878

**Gaus mean : 39.2030**

**Gaus Width: 4.3126**

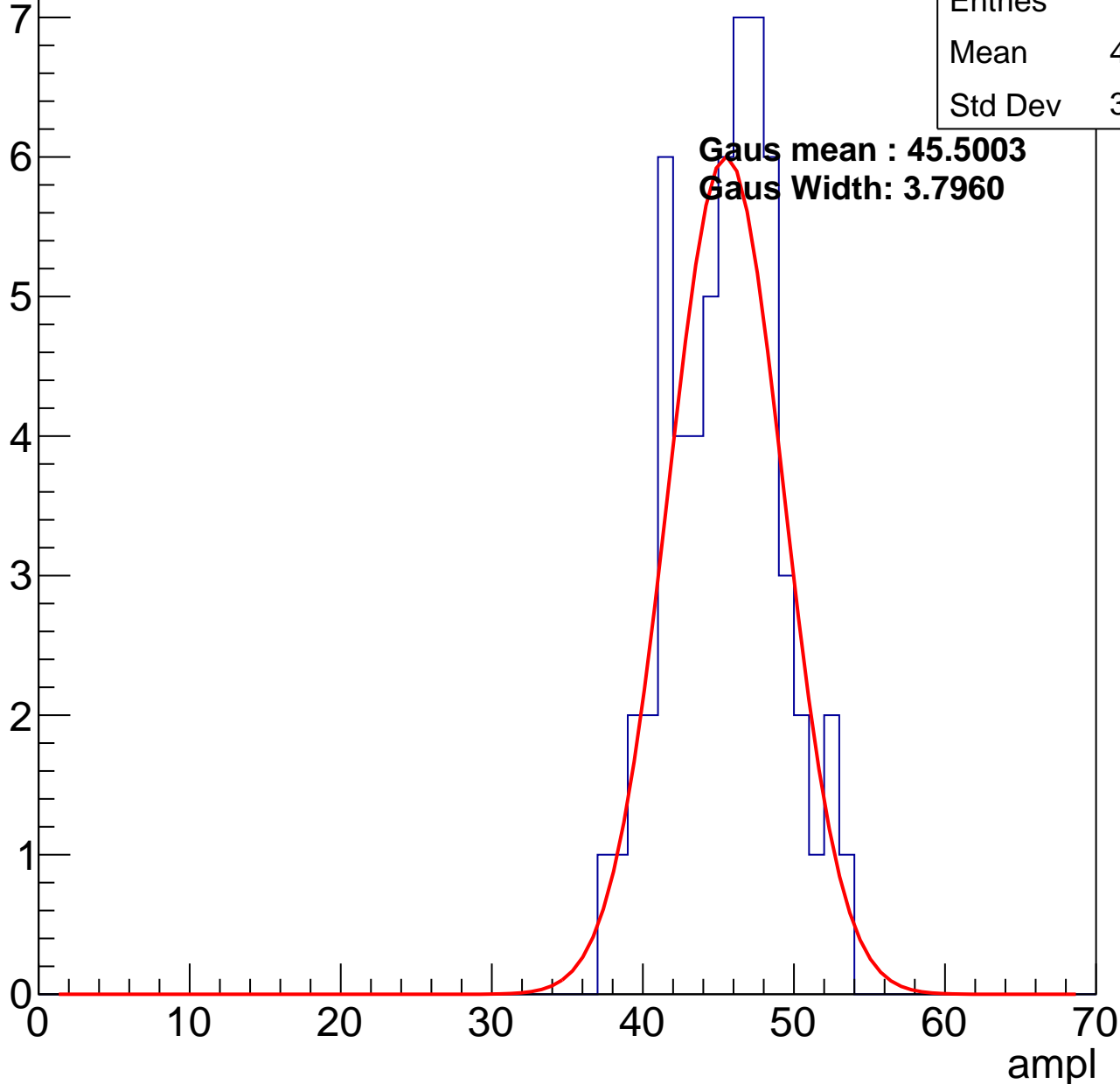


# B1L100S, U6-ch117, adc2

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	60
Mean	45.05
Std Dev	3.589

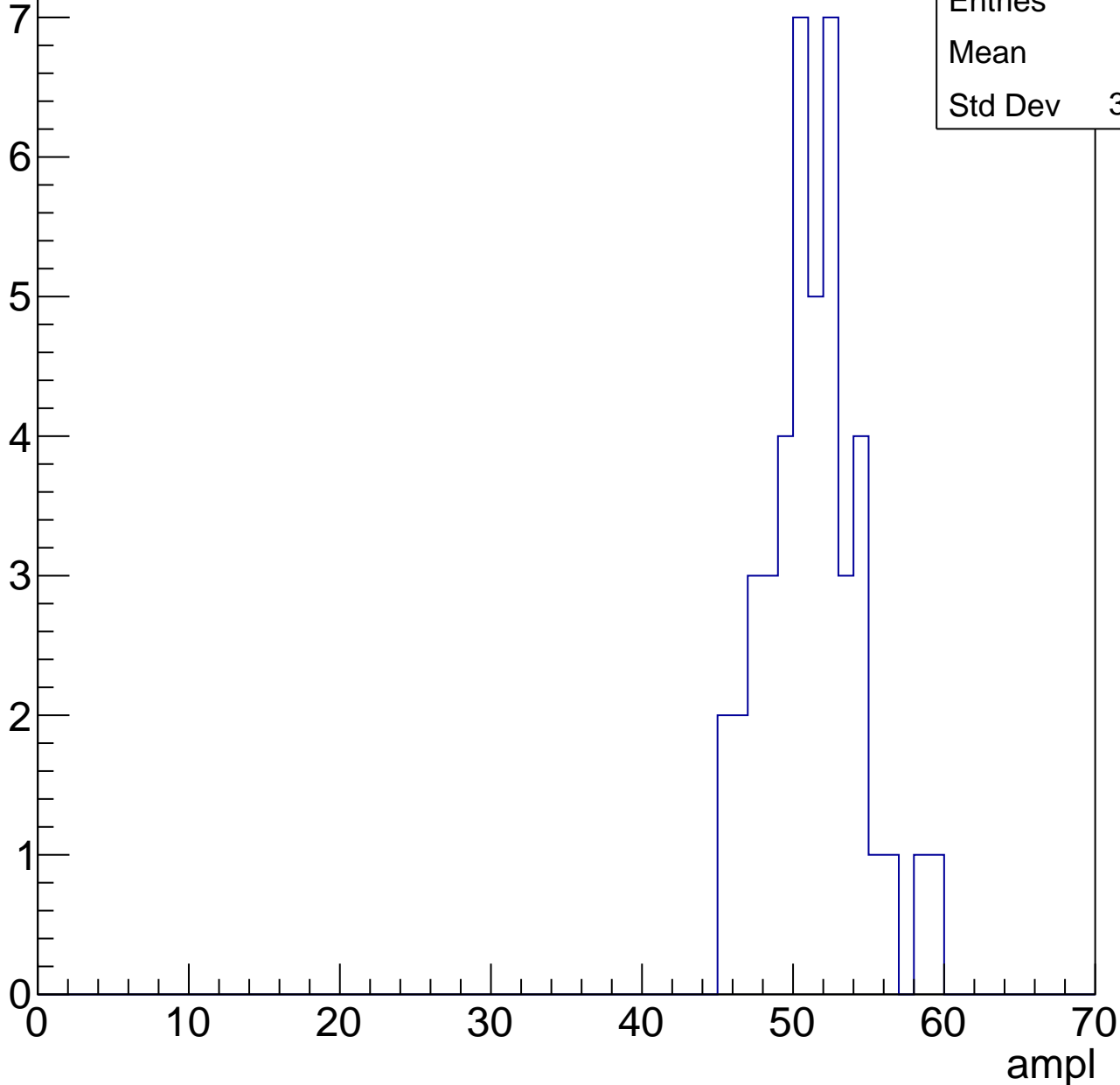


# B1L100S, U6-ch117, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	44
Mean	50.8
Std Dev	3.116

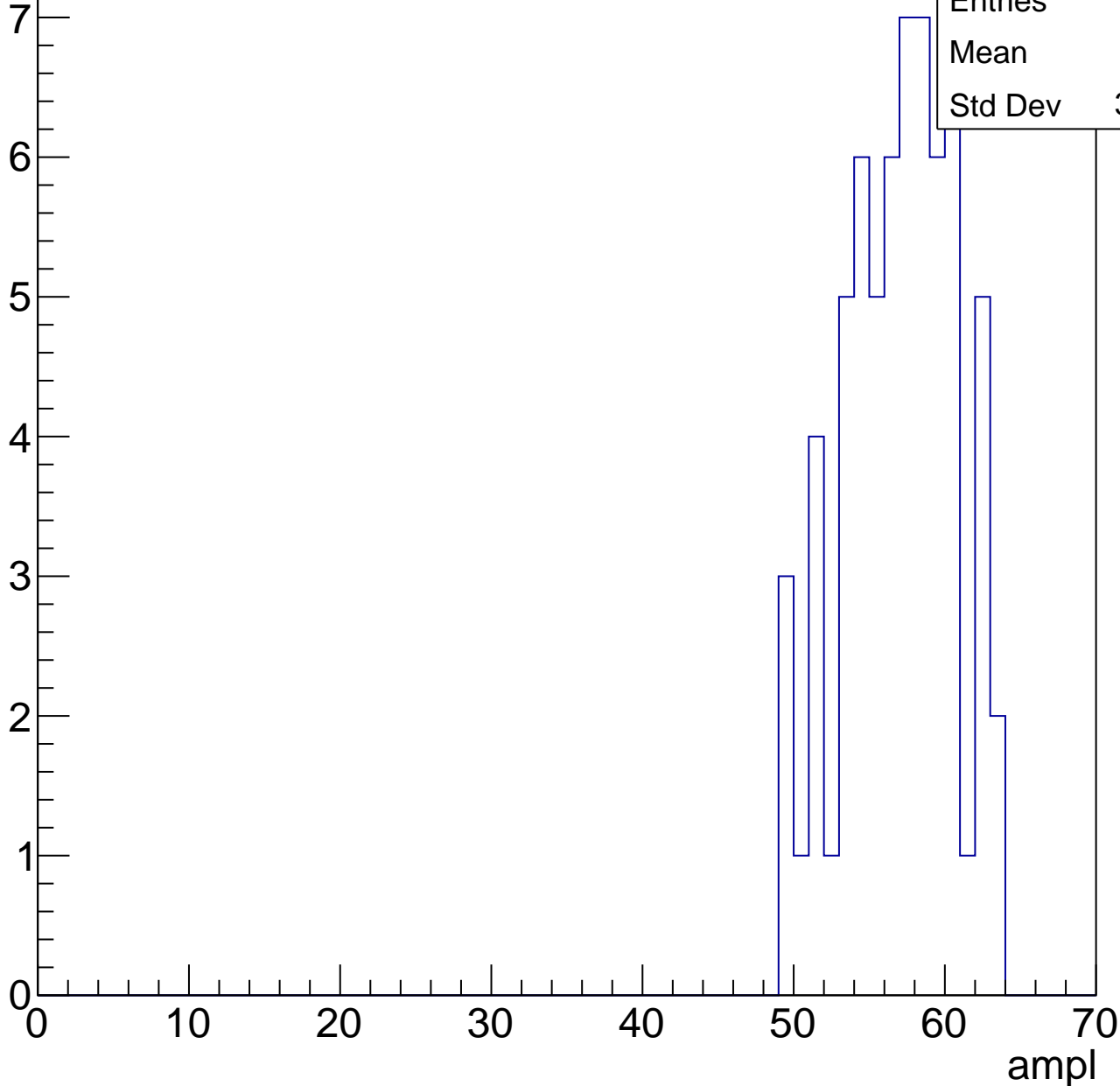


# B1L100S, U6-ch117, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	66
Mean	56.5
Std Dev	3.611

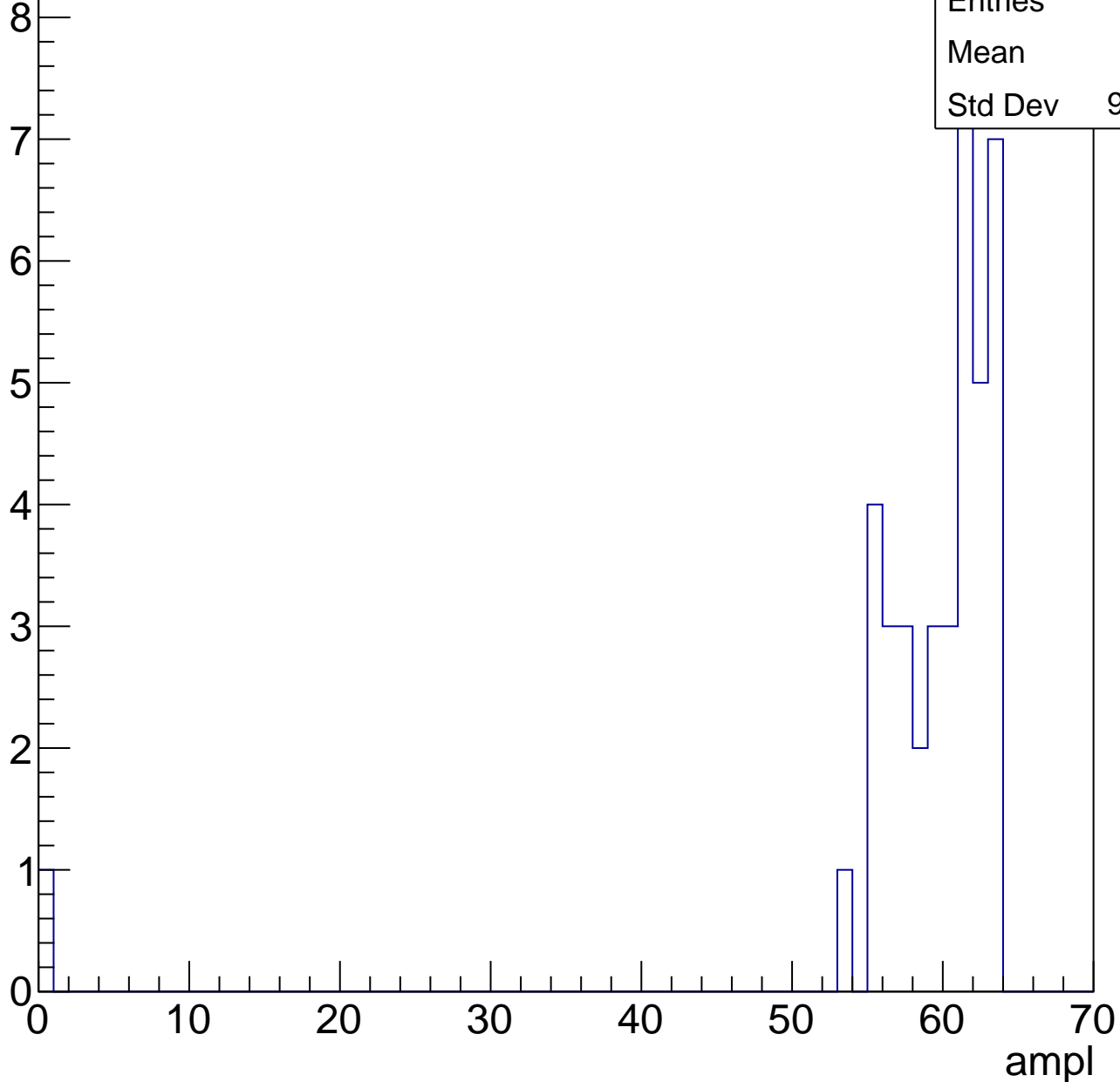


# B1L100S, U6-ch117, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	40
Mean	58.1
Std Dev	9.723



# B1L100S, U6-ch117, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry





# B1L100S, U6-ch117, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



# B1L100S, U6-ch118, adc0

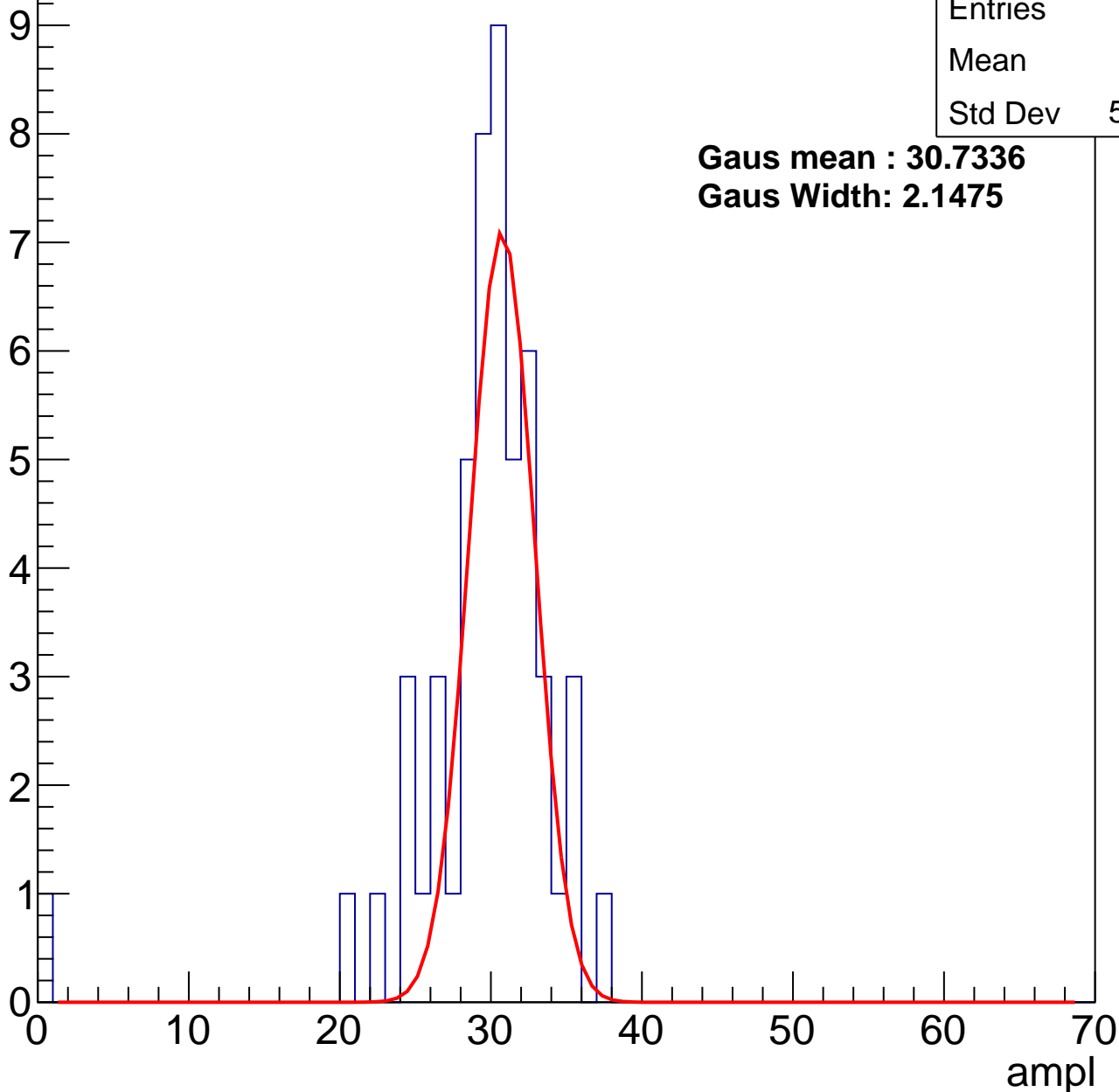
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	52
Mean	29
Std Dev	5.237

**Gaus mean : 30.7336**

**Gaus Width: 2.1475**



# B1L100S, U6-ch118, adc1

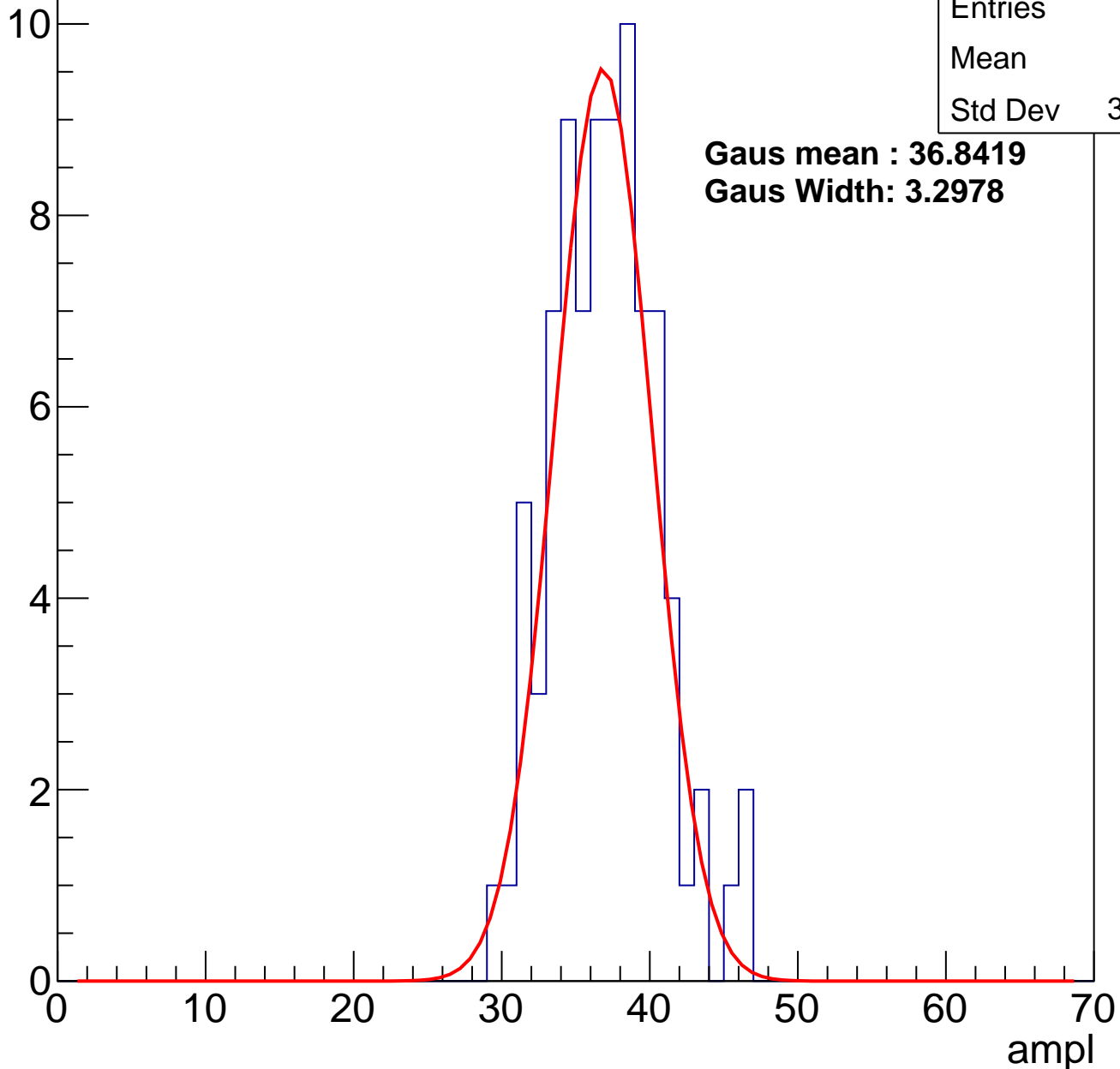
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	85
Mean	36.6
Std Dev	3.552

**Gaus mean : 36.8419**

**Gaus Width: 3.2978**

Entry



# B1L100S, U6-ch118, adc2

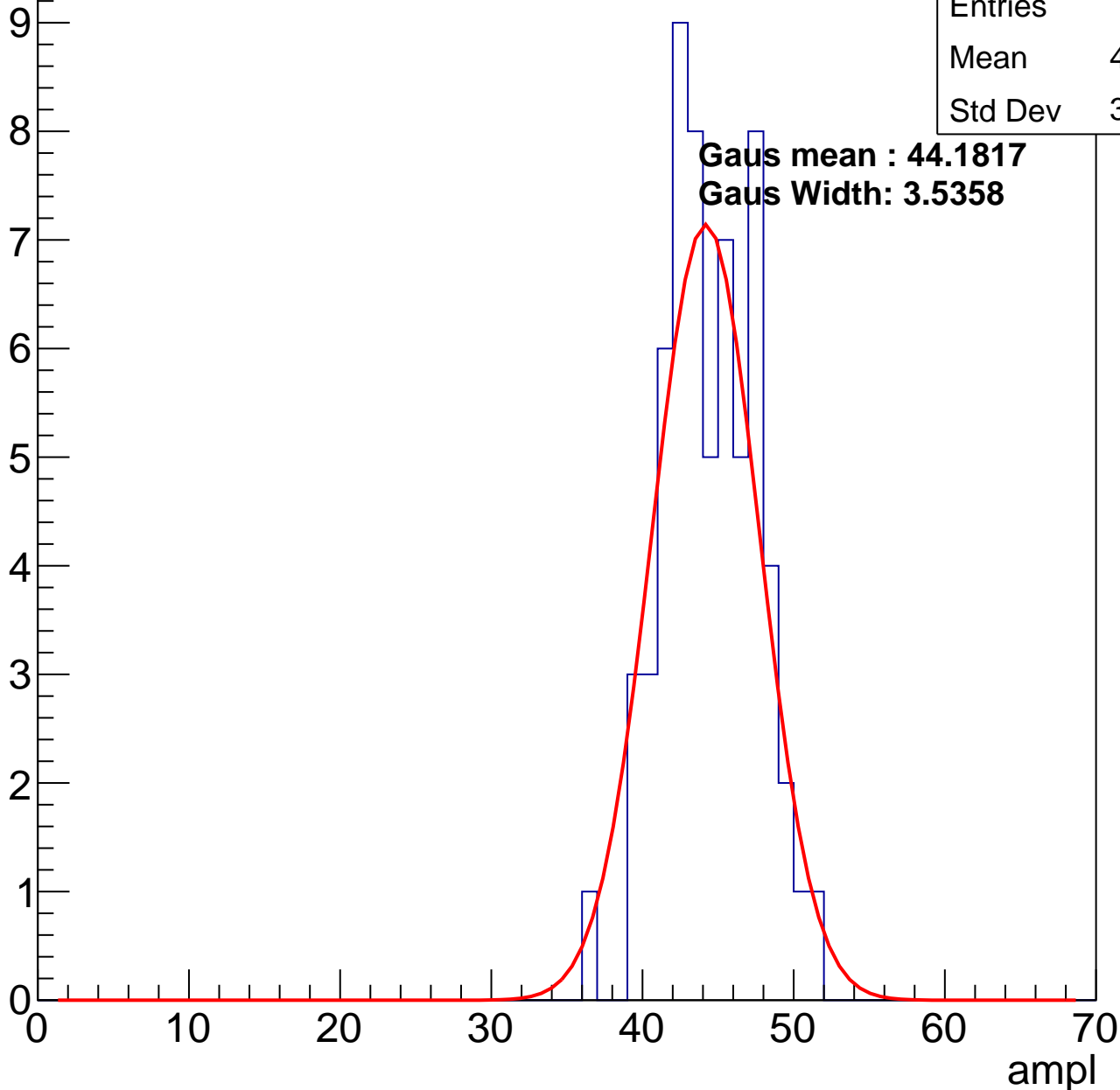
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	63
Mean	44.02
Std Dev	3.042

**Gaus mean : 44.1817**

**Gaus Width: 3.5358**

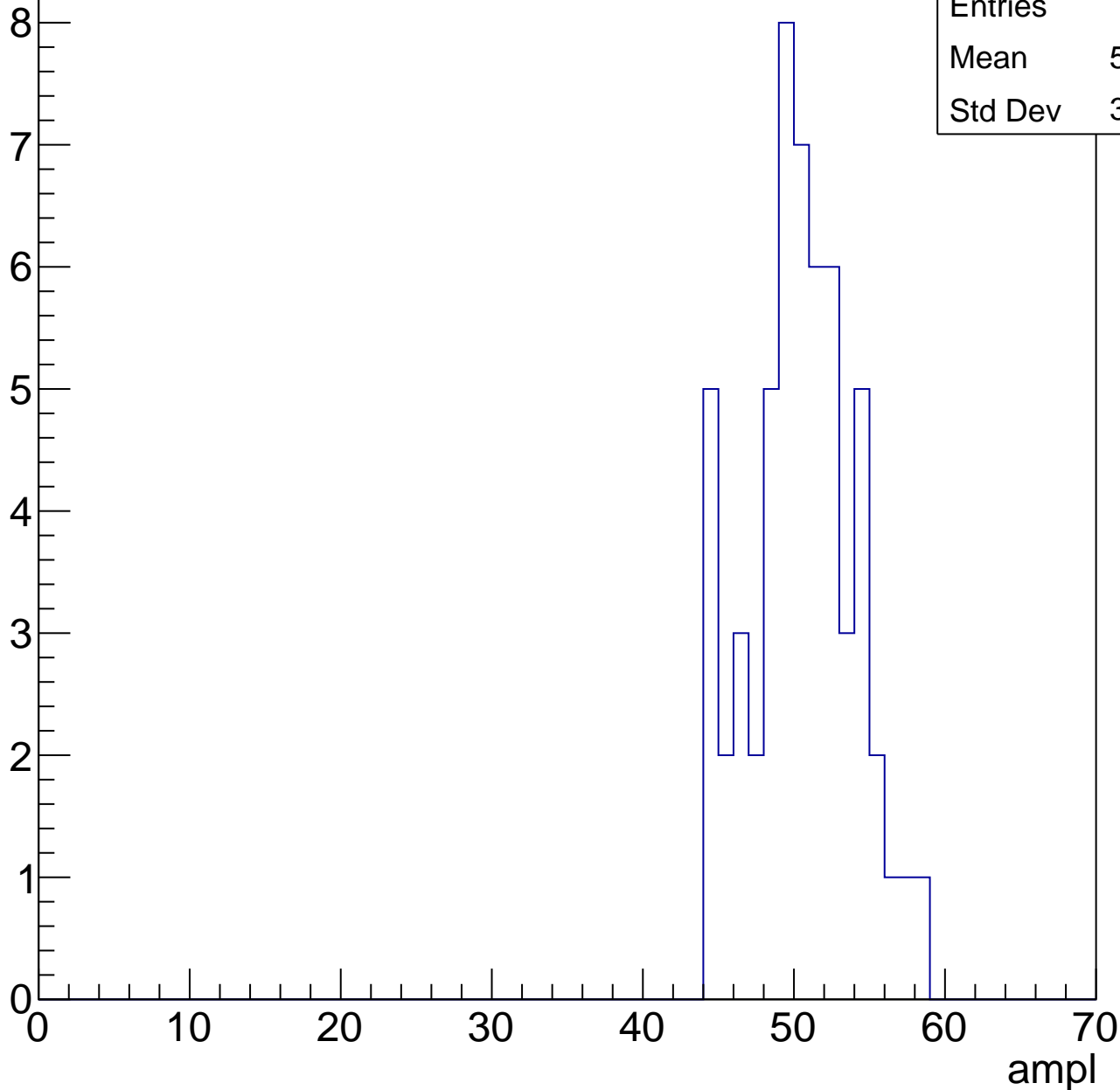


# B1L100S, U6-ch118, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	57
Mean	50.04
Std Dev	3.403

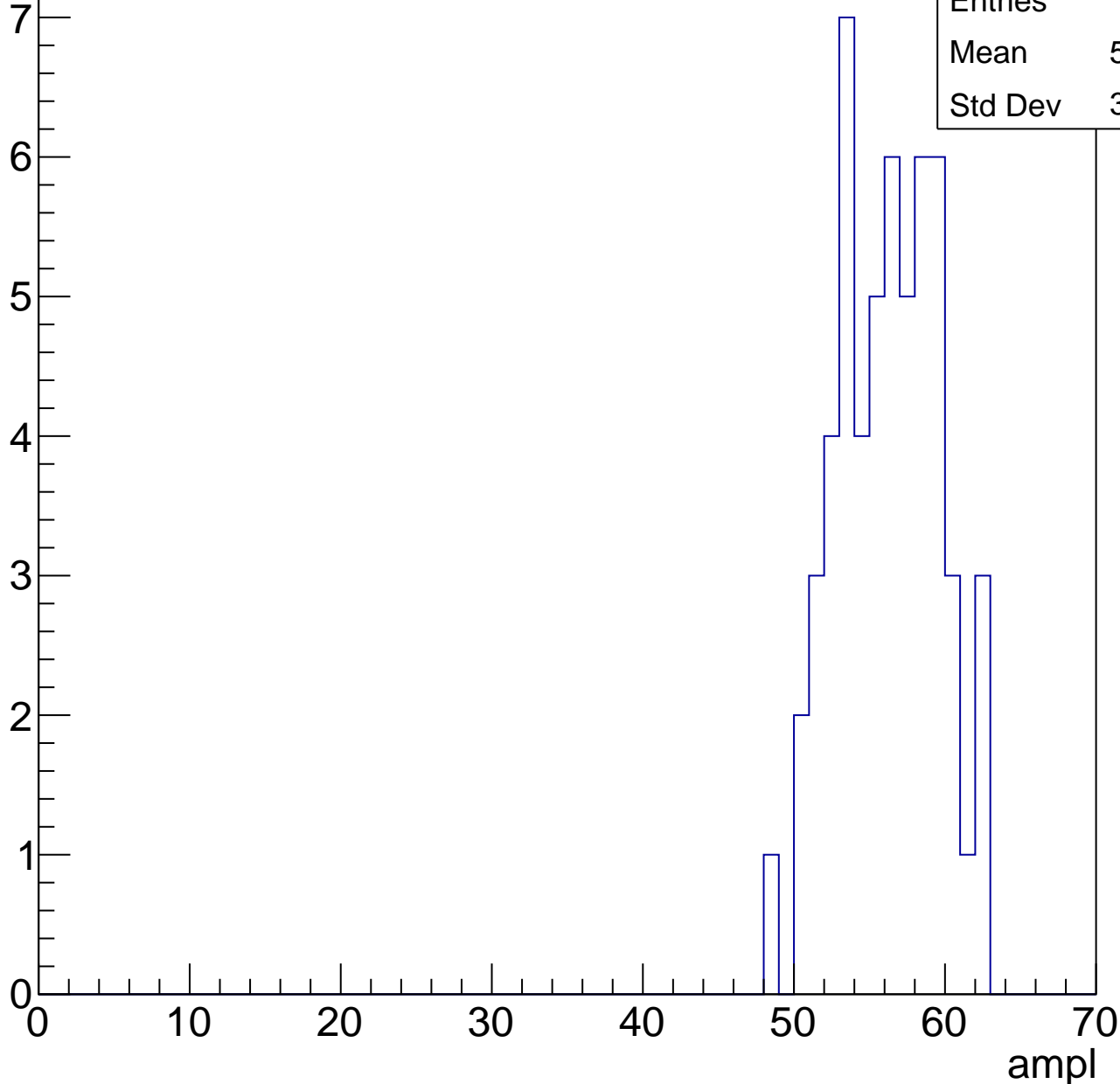


# B1L100S, U6-ch118, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	56
Mean	55.73
Std Dev	3.325



# B1L100S, U6-ch118, adc5

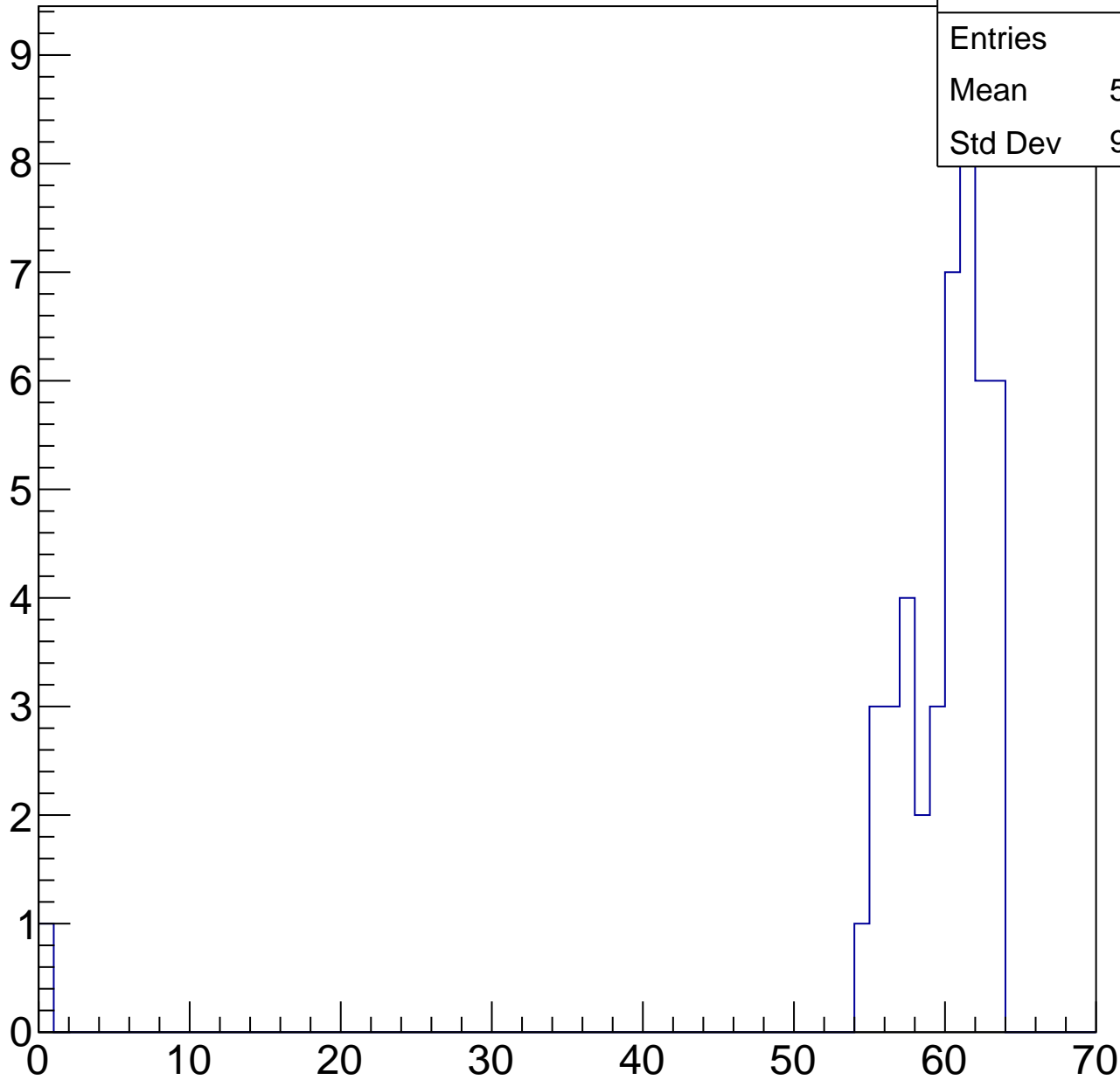
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	45
Mean	58.38
Std Dev	9.159

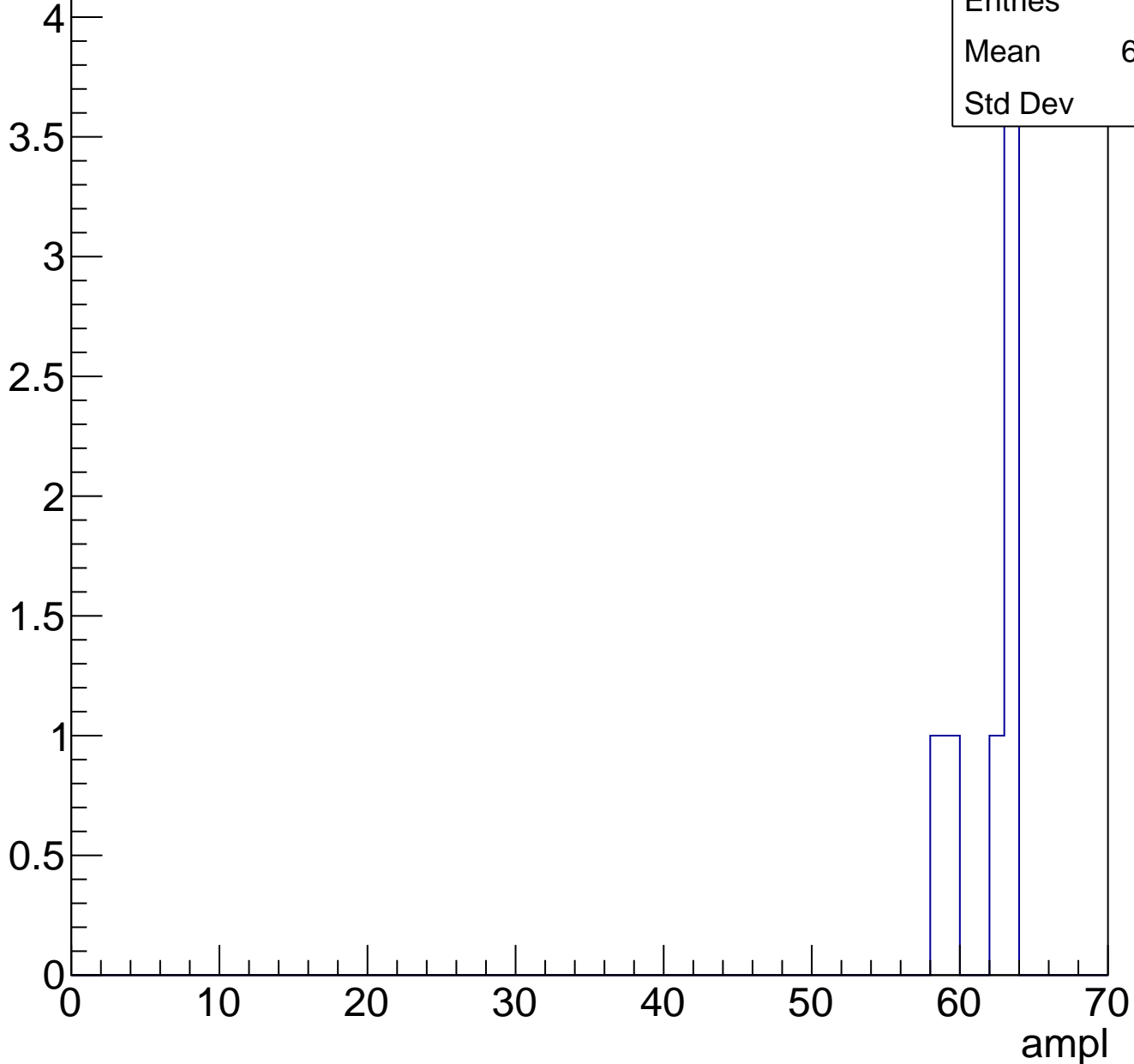
ampl



# B1L100S, U6-ch118, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry





# B1L100S, U6-ch118, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



# B1L100S, U6-ch119, adc0

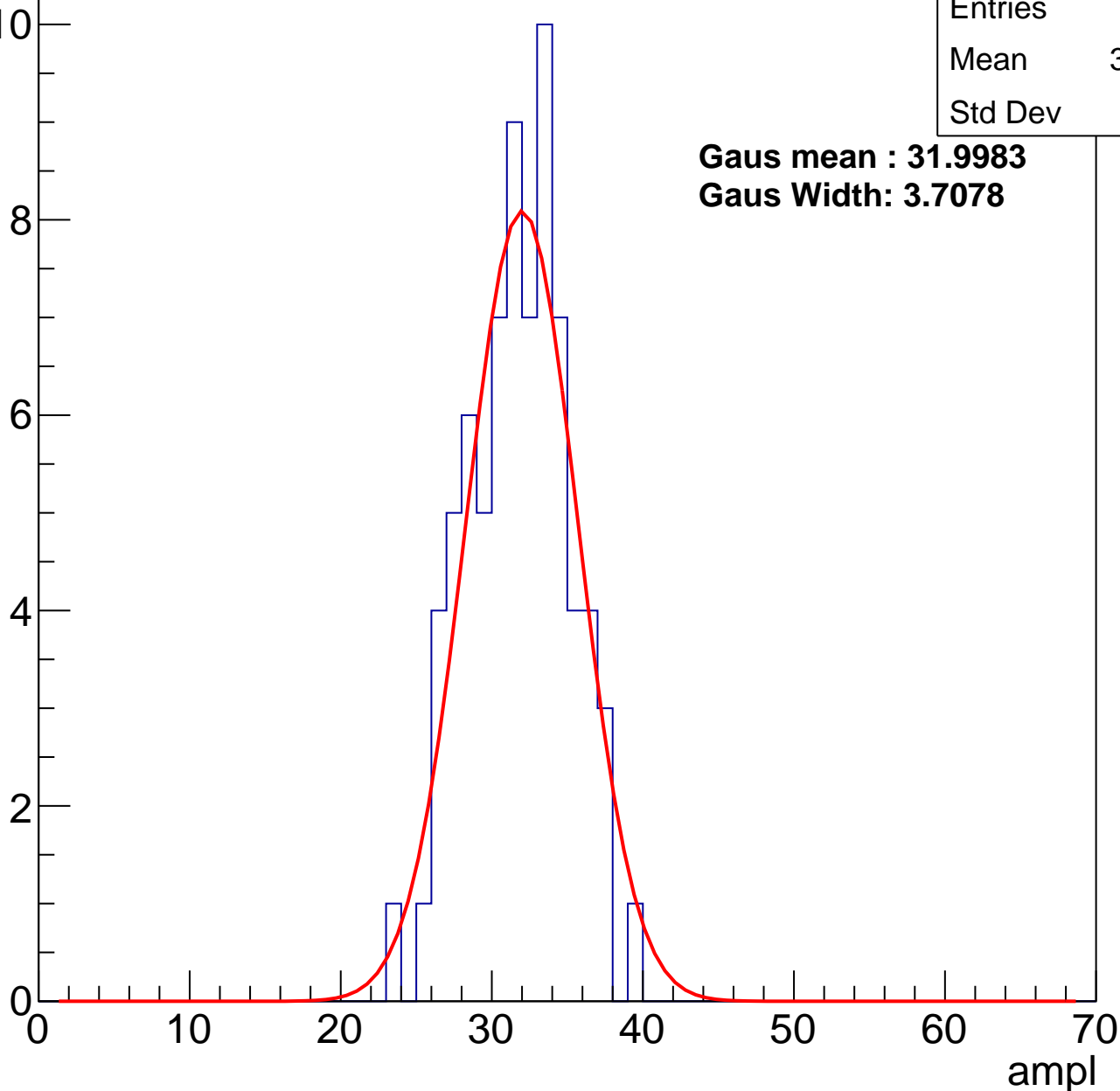
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	74
Mean	31.28
Std Dev	3.29

**Gaus mean : 31.9983**

**Gaus Width: 3.7078**



# B1L100S, U6-ch119, adc1

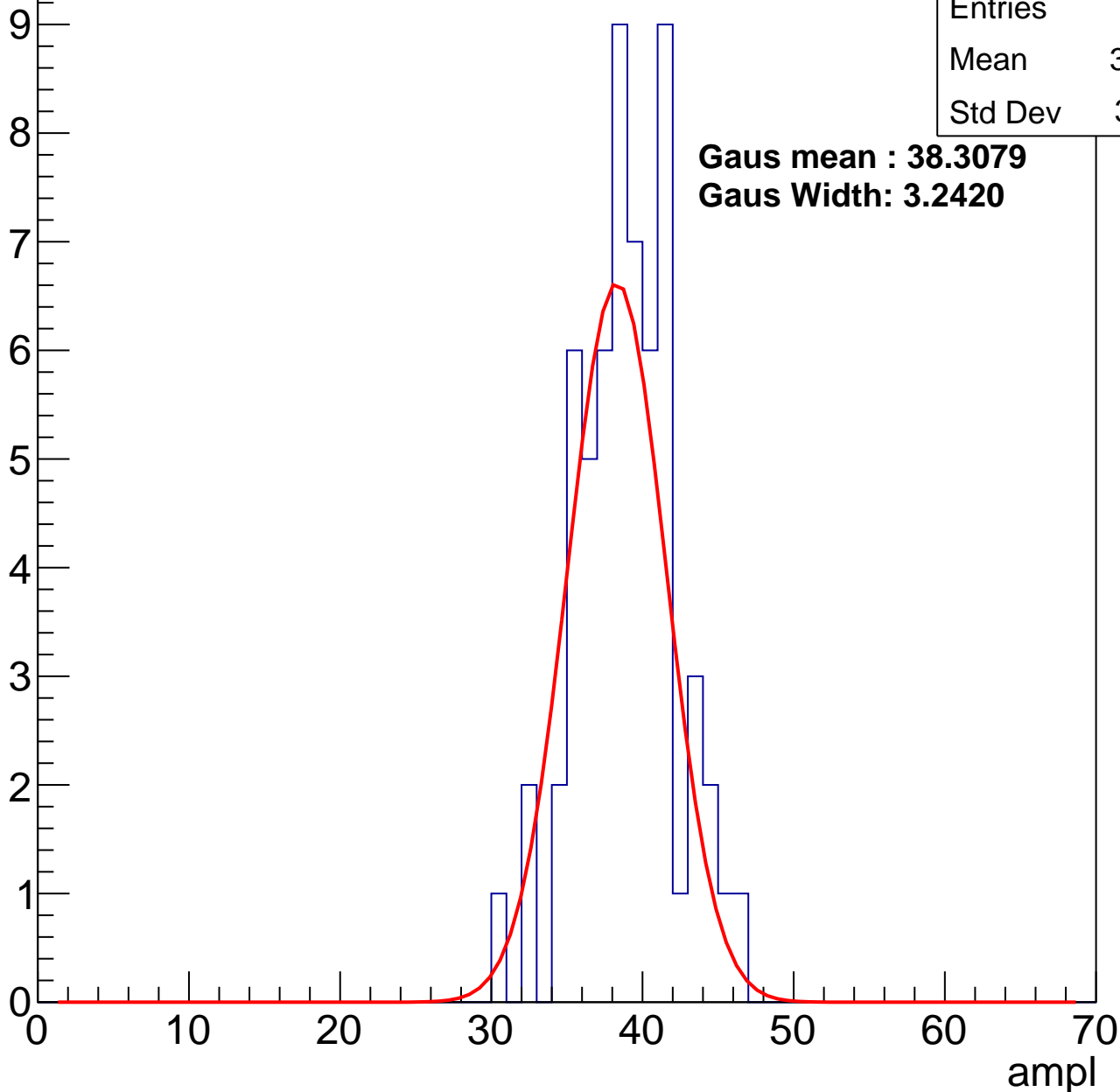
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	61
Mean	38.49
Std Dev	3.191

**Gaus mean : 38.3079**

**Gaus Width: 3.2420**



# B1L100S, U6-ch119, adc2

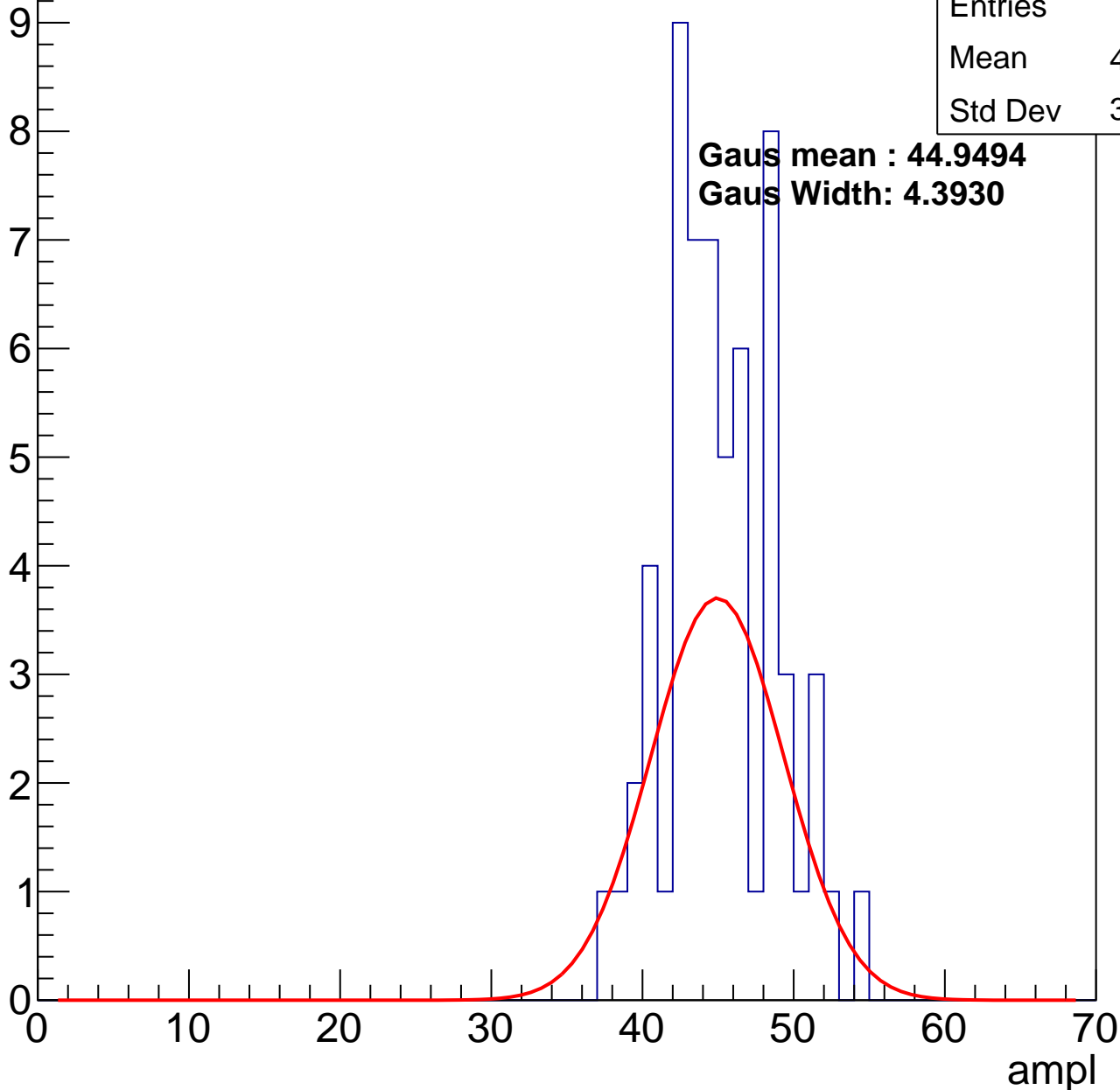
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	61
Mean	44.74
Std Dev	3.635

**Gaus mean : 44.9494**

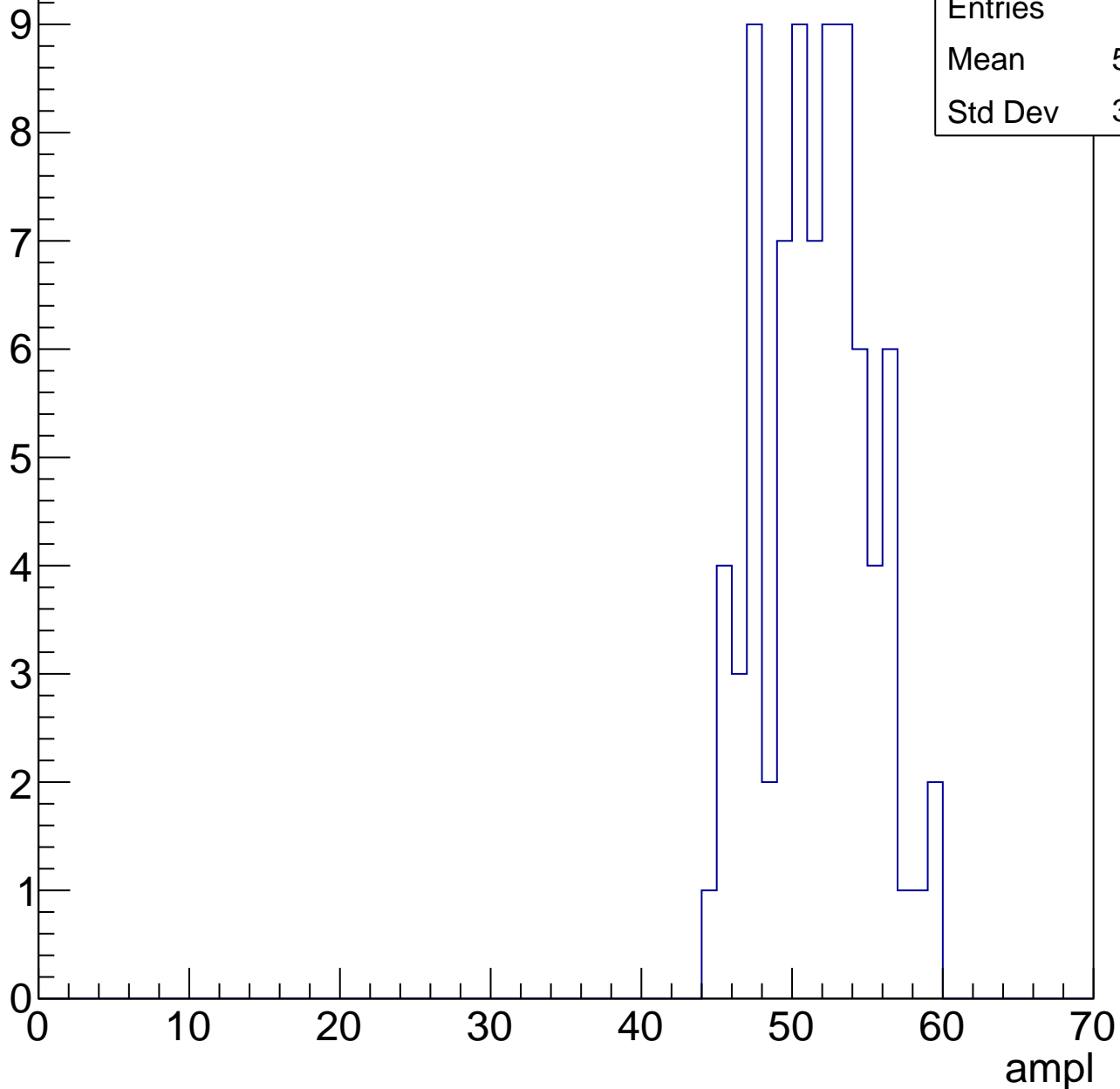
**Gaus Width: 4.3930**



# B1L100S, U6-ch119, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

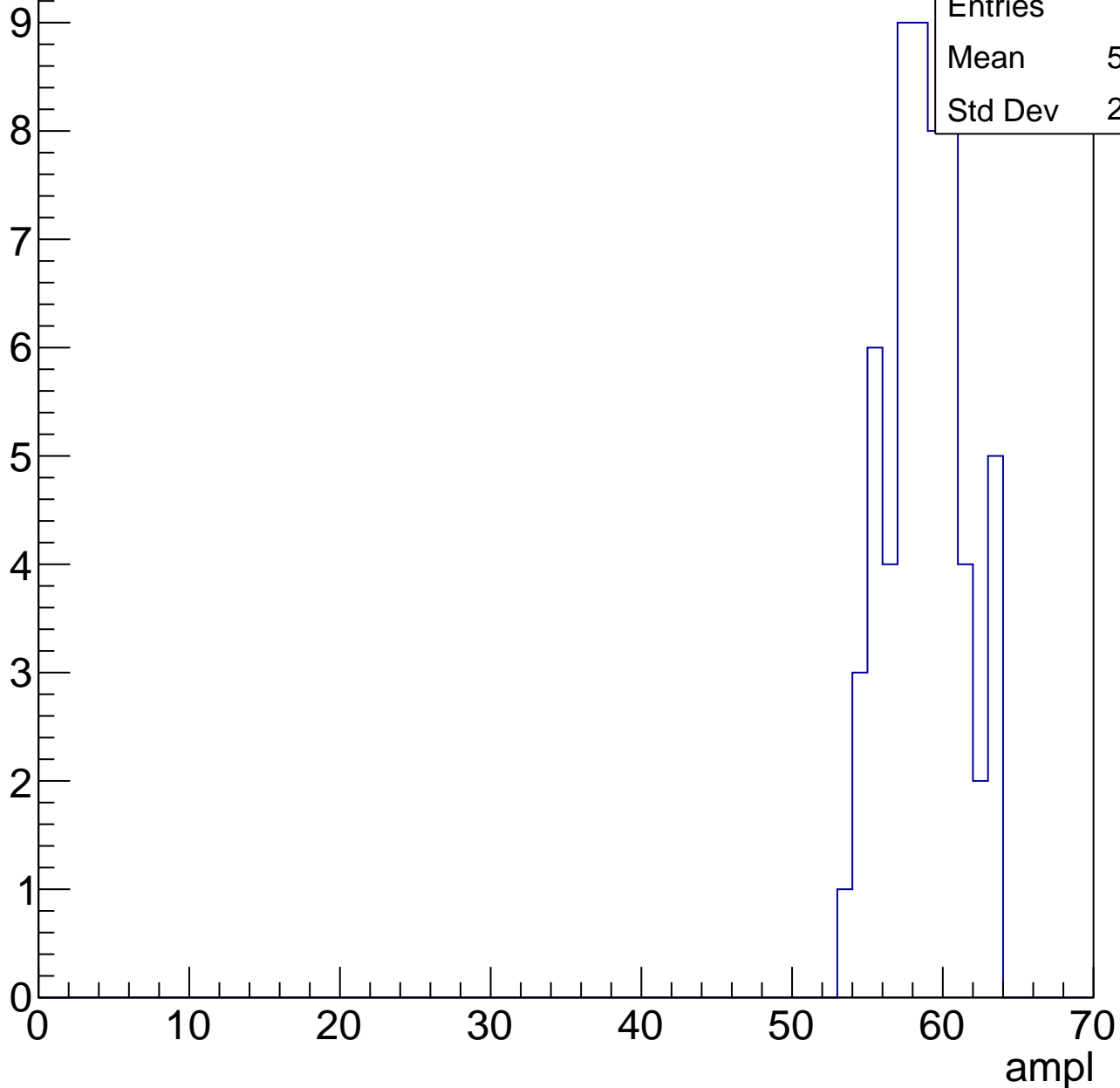
Entry



# B1L100S, U6-ch119, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

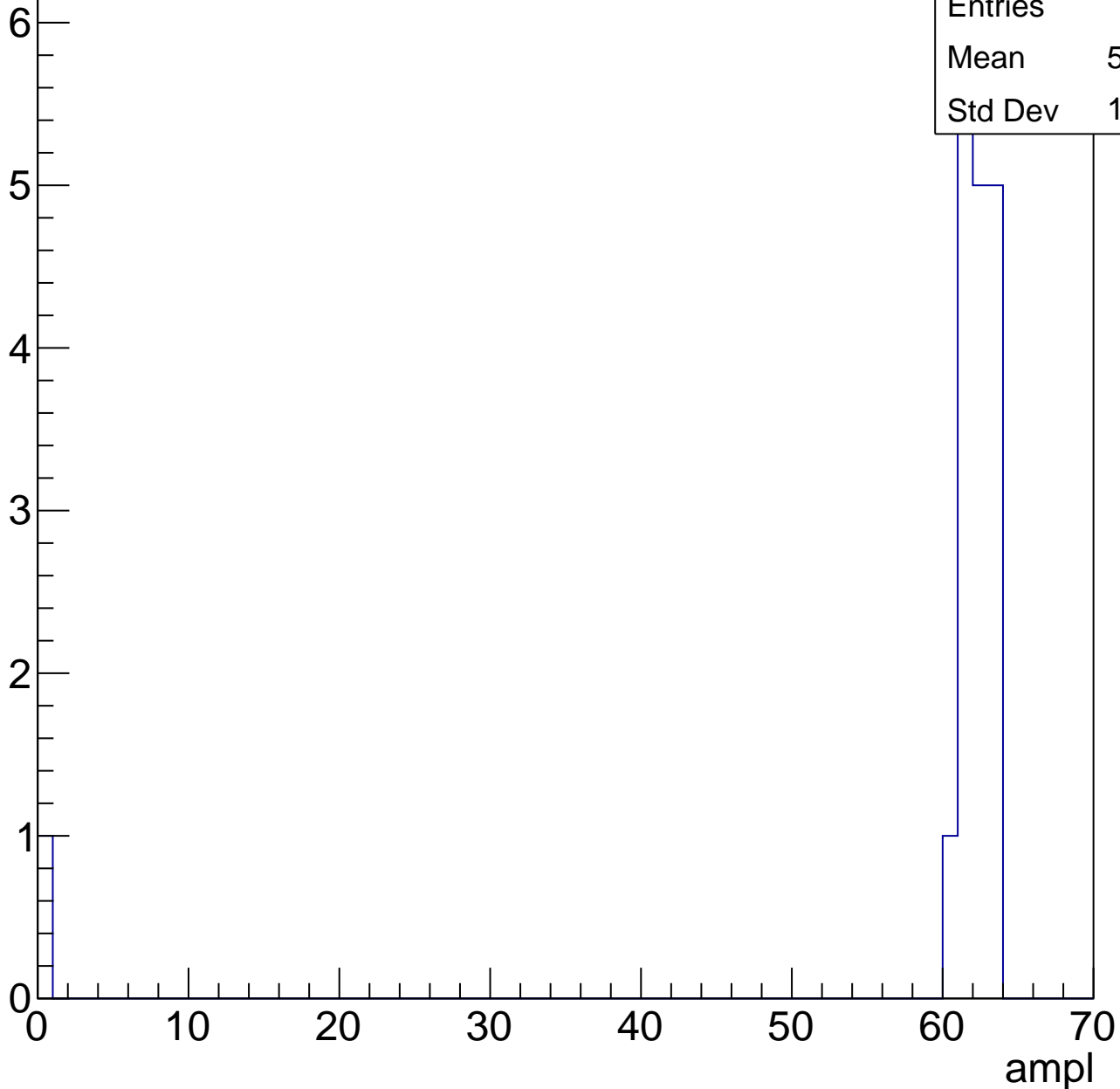


# B1L100S, U6-ch119, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	18
Mean	58.39
Std Dev	14.19



# B1L100S, U6-ch119, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry





# B1L100S, U6-ch119, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



# B1L100S, U6-ch120, adc0

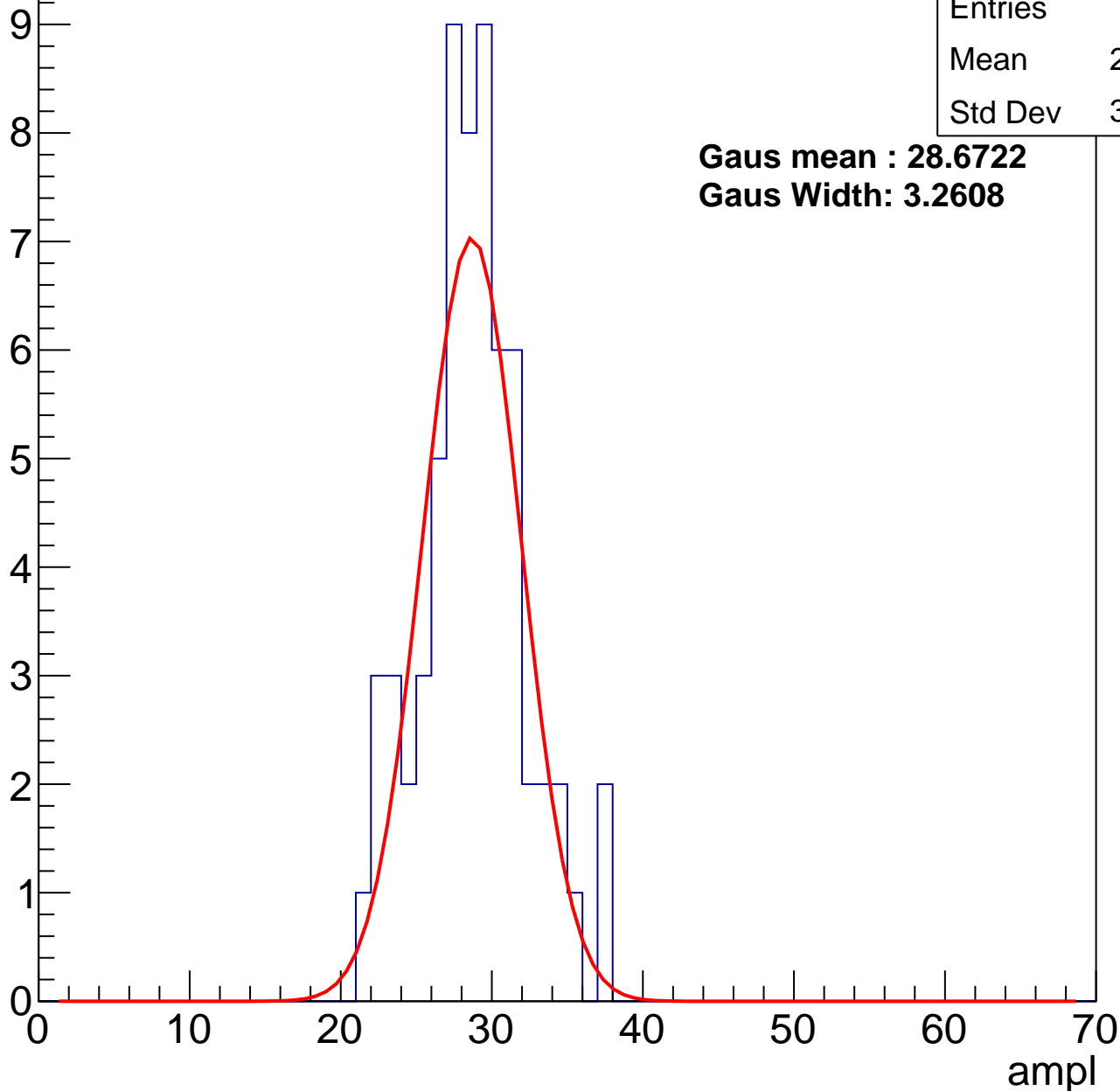
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	64
Mean	28.28
Std Dev	3.462

**Gaus mean : 28.6722**

**Gaus Width: 3.2608**



# B1L100S, U6-ch120, adc1

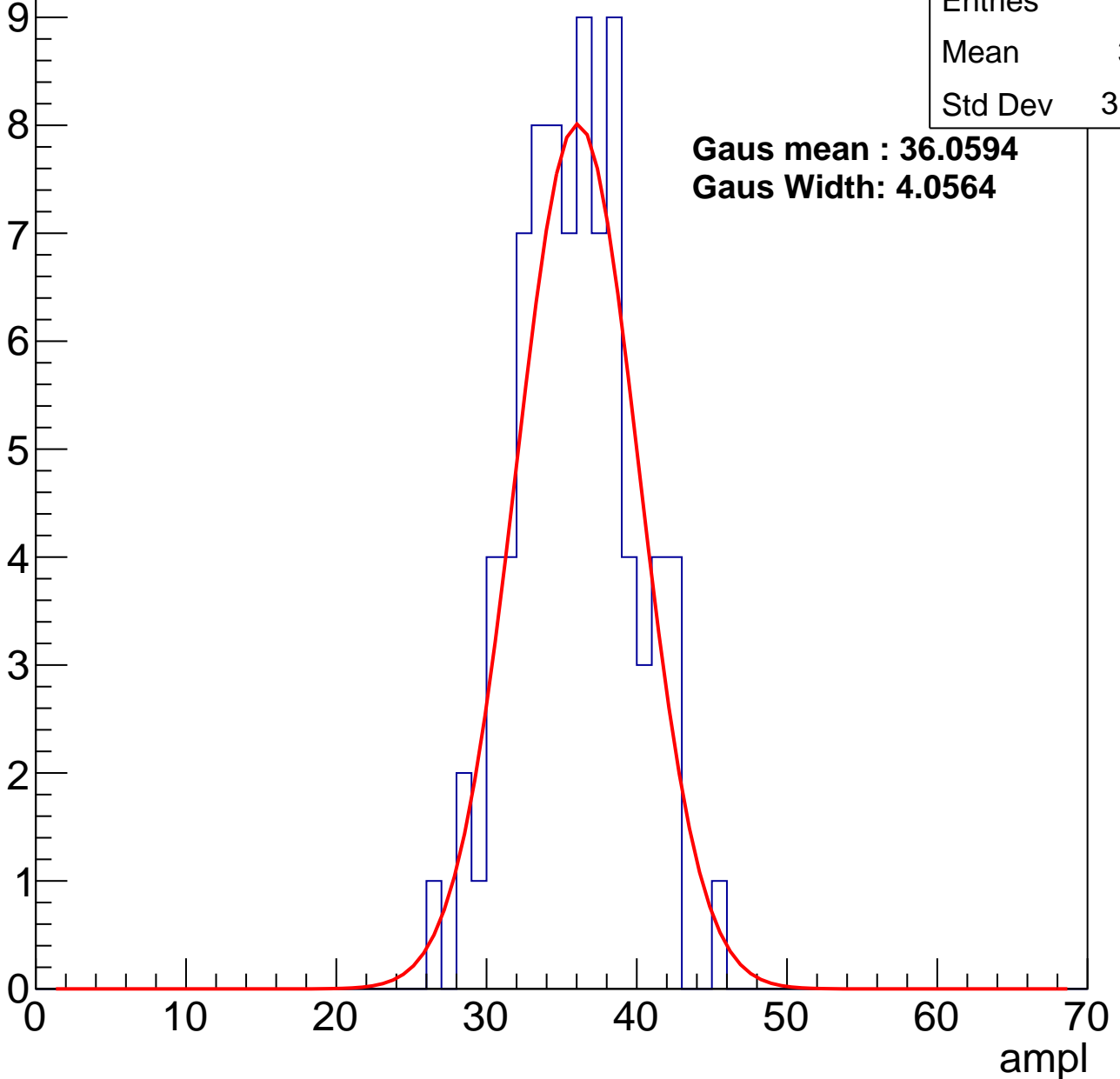
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	83
Mean	35.4
Std Dev	3.748

**Gaus mean : 36.0594**

**Gaus Width: 4.0564**



# B1L100S, U6-ch120, adc2

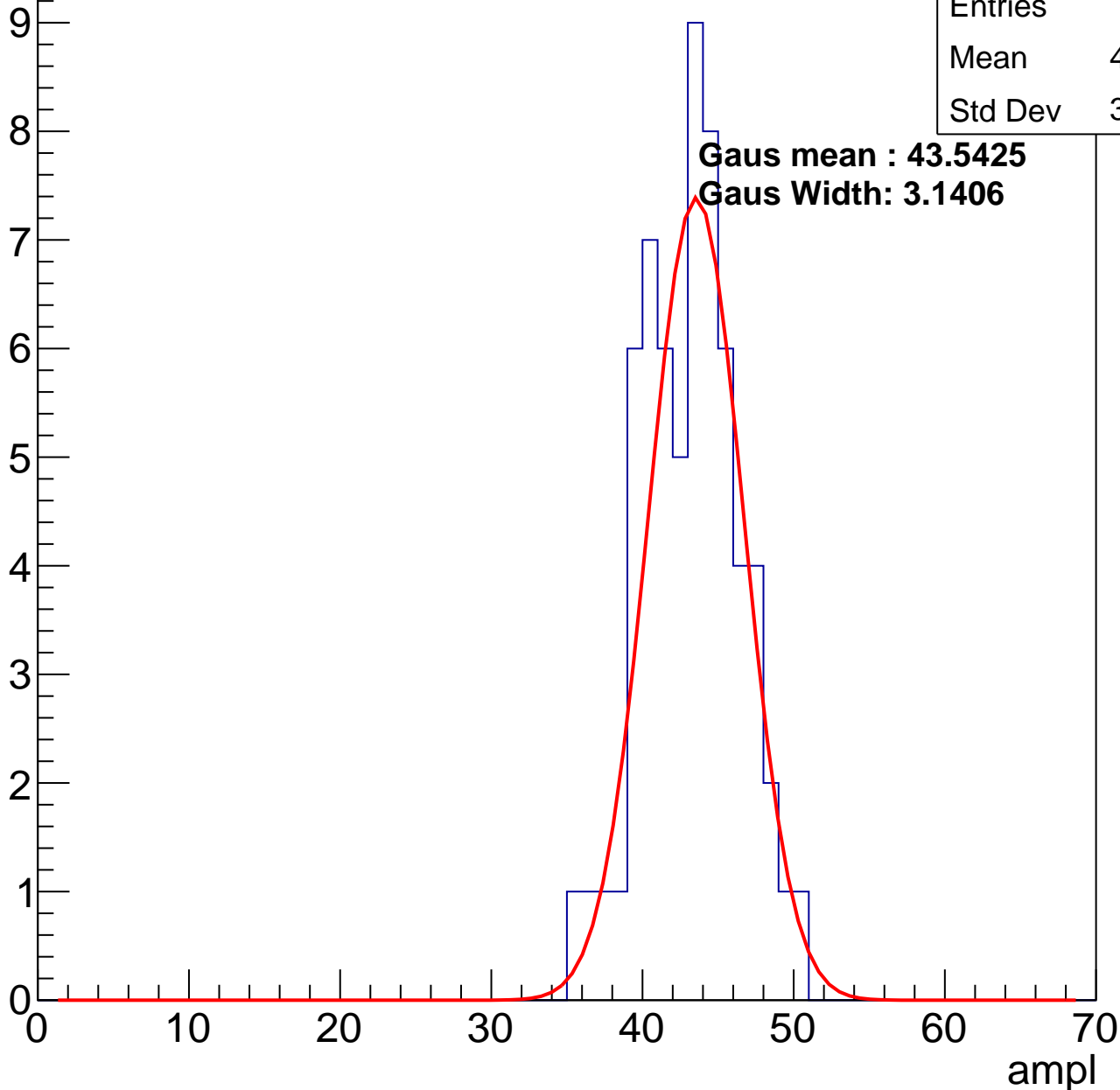
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	63
Mean	42.73
Std Dev	3.148

**Gaus mean : 43.5425**

**Gaus Width: 3.1406**

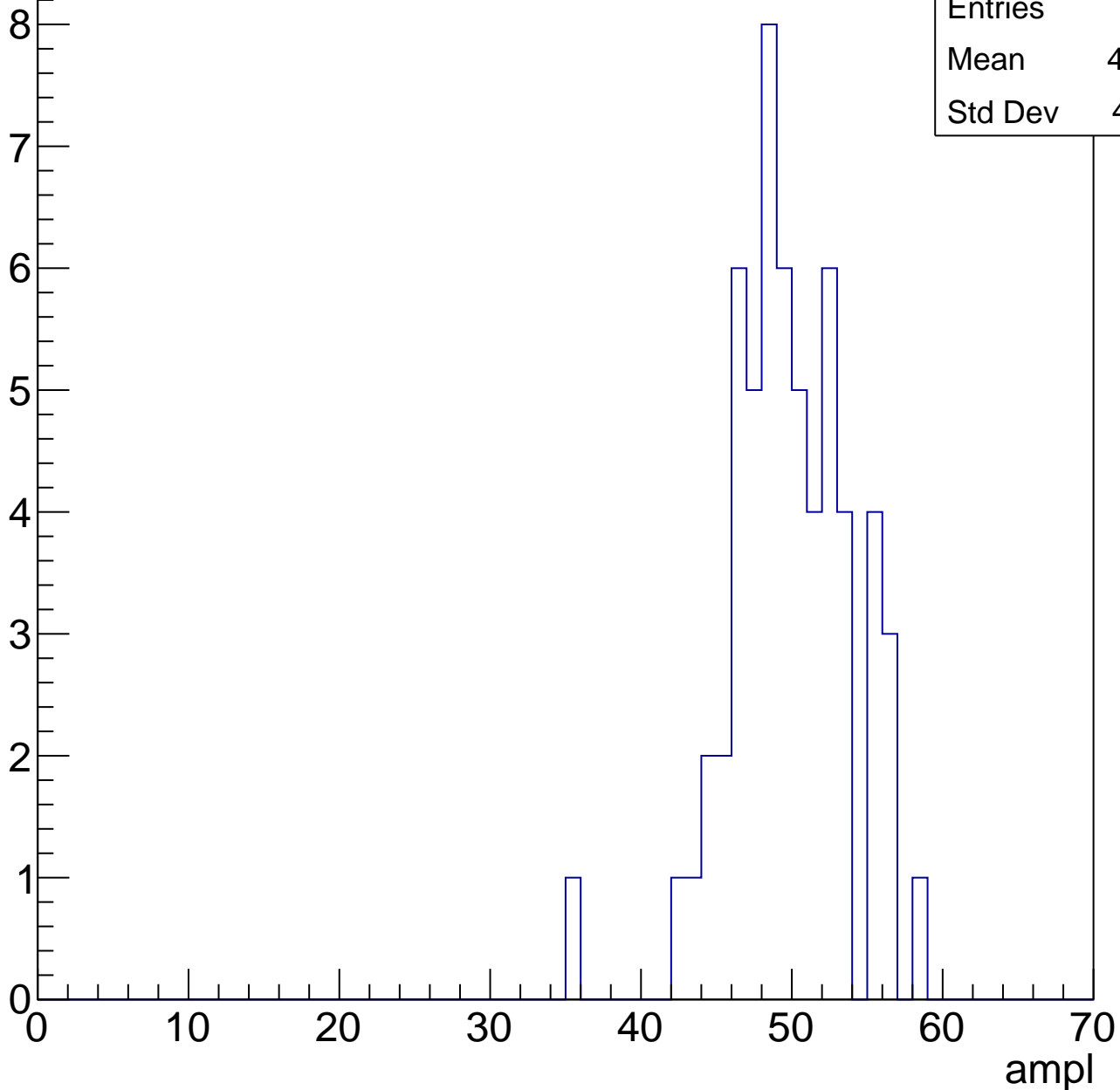


# B1L100S, U6-ch120, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	59
Mean	49.34
Std Dev	4.011

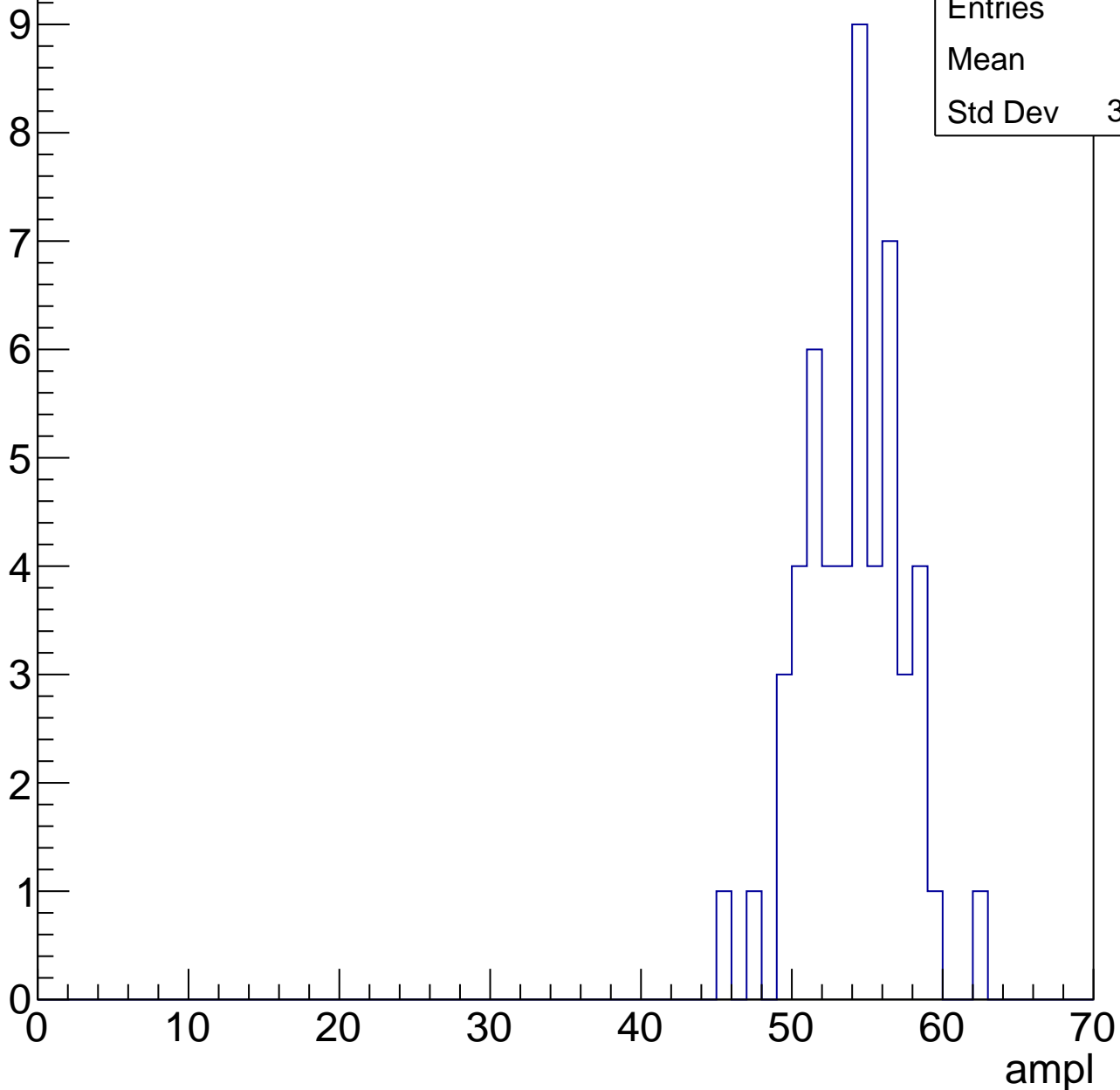


# B1L100S, U6-ch120, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	52
Mean	53.6
Std Dev	3.242

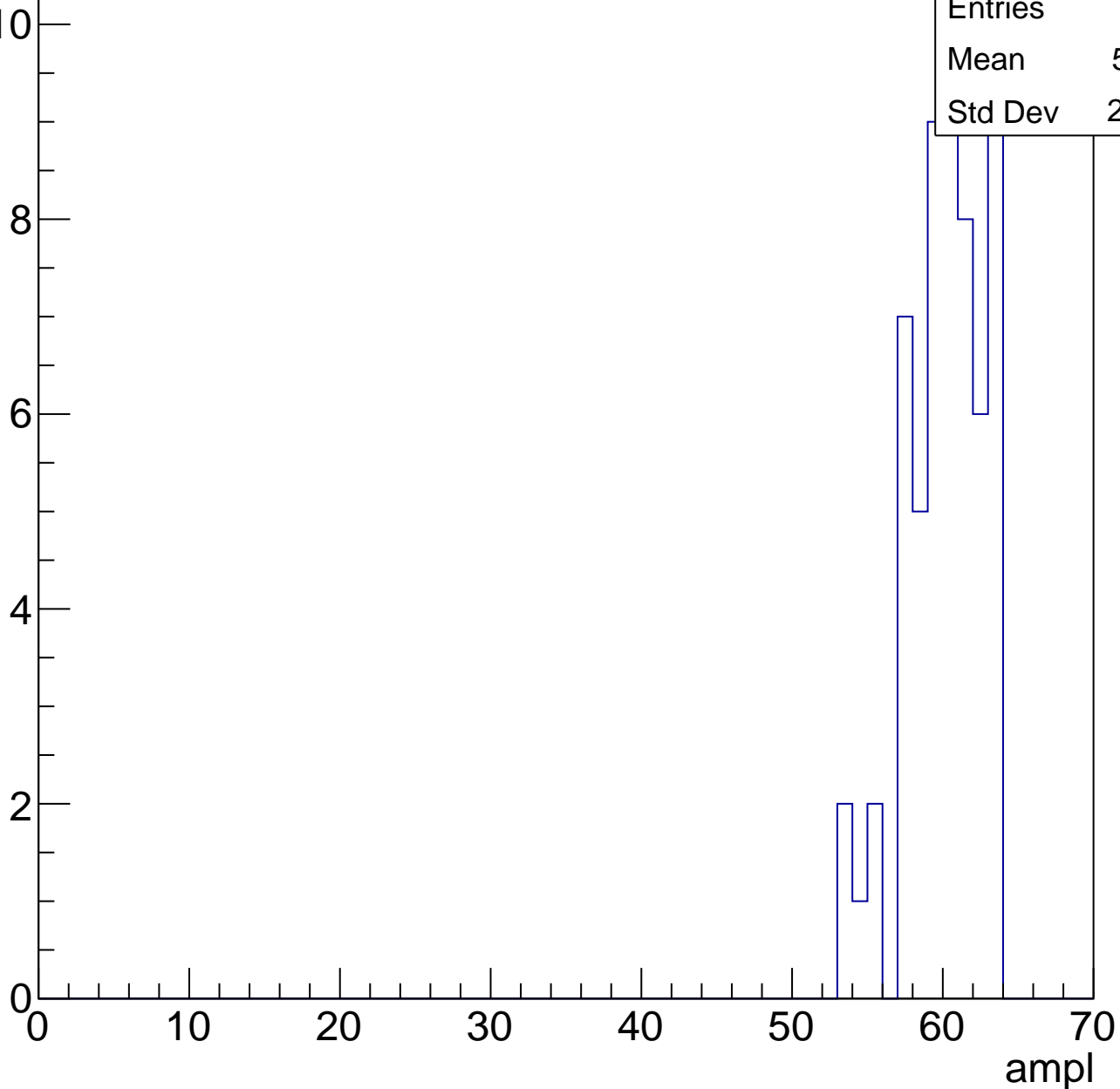


# B1L100S, U6-ch120, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	59
Mean	59.61
Std Dev	2.538



# B1L100S, U6-ch120, adc6

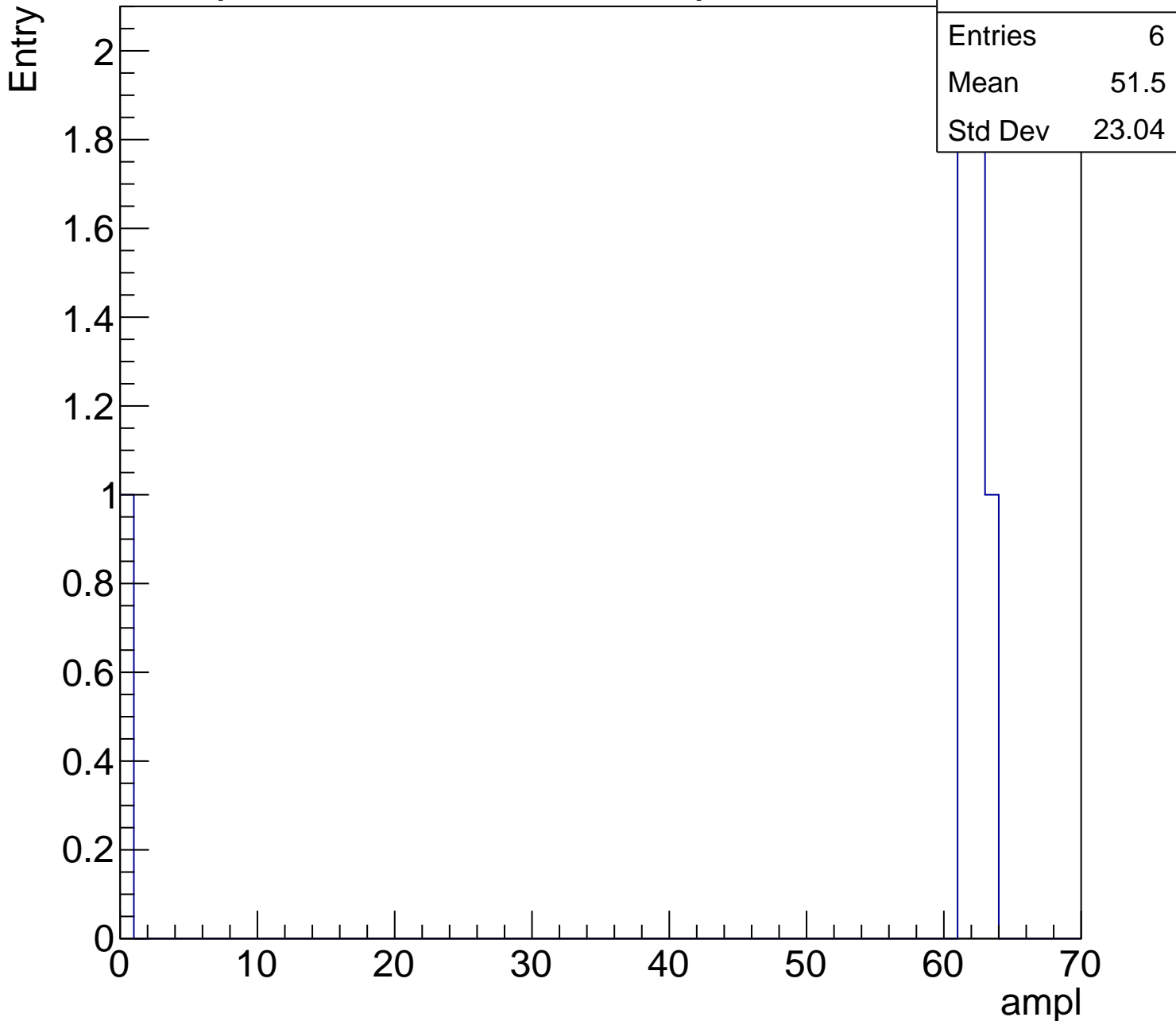
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	6
Mean	51.5
Std Dev	23.04

ampl





# B1L100S, U6-ch120, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	2
Mean	31
Std Dev	31

# B1L100S, U6-ch121, adc0

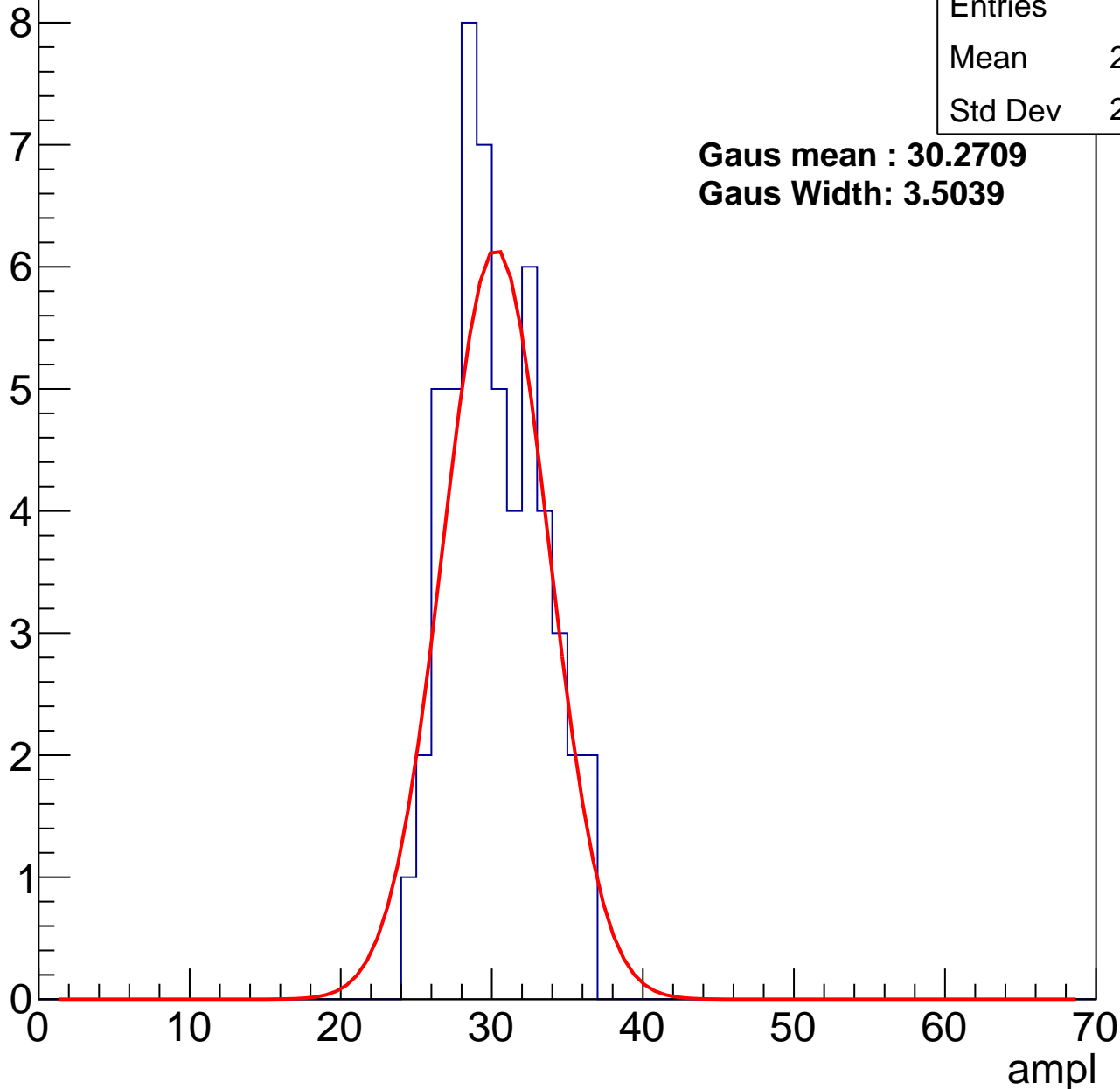
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	54
Mean	29.78
Std Dev	2.986

**Gaus mean : 30.2709**

**Gaus Width: 3.5039**



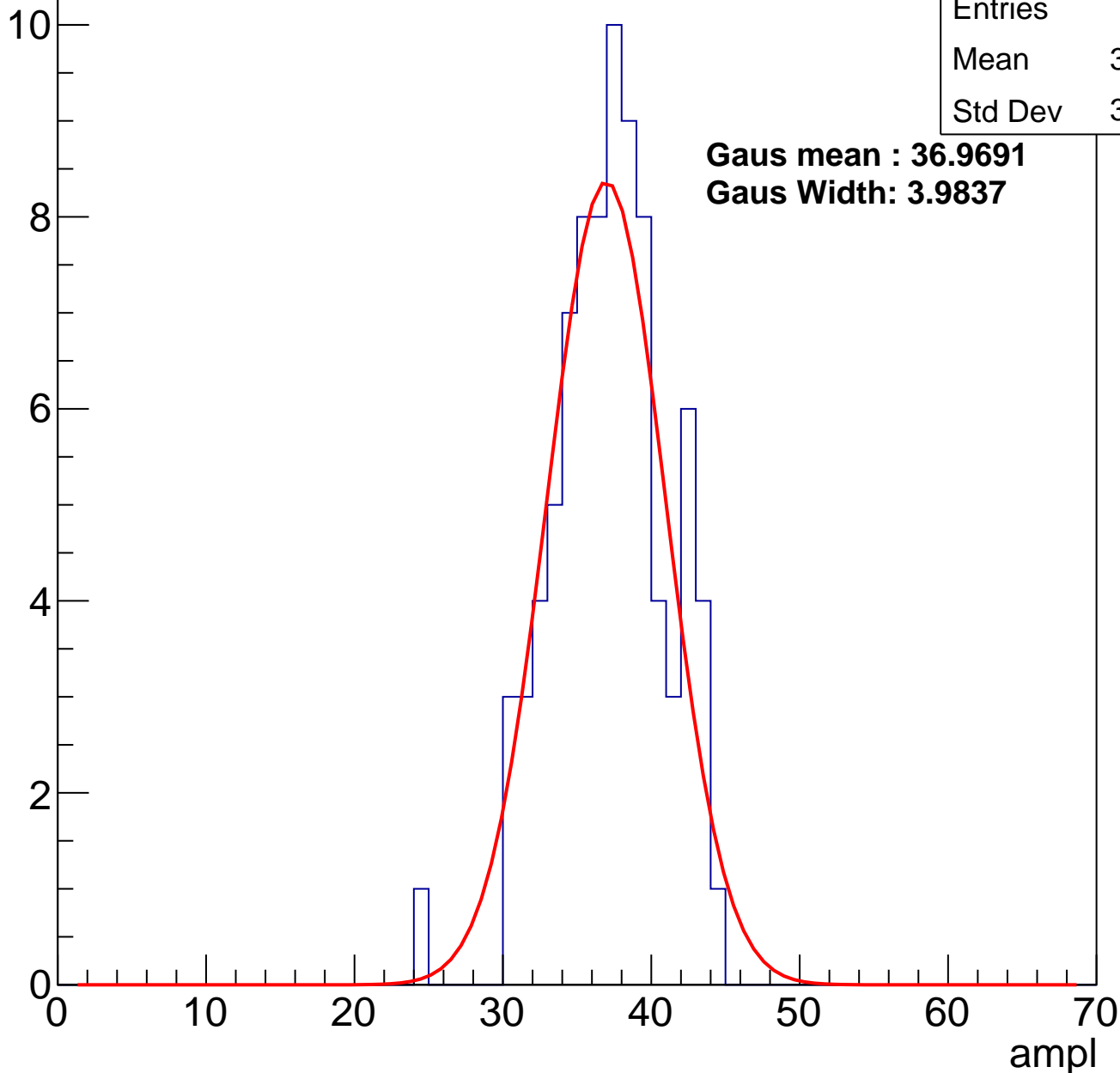
# B1L100S, U6-ch121, adc1

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	84
Mean	36.68
Std Dev	3.726

**Gaus mean : 36.9691**  
**Gaus Width: 3.9837**

Entry



# B1L100S, U6-ch121, adc2

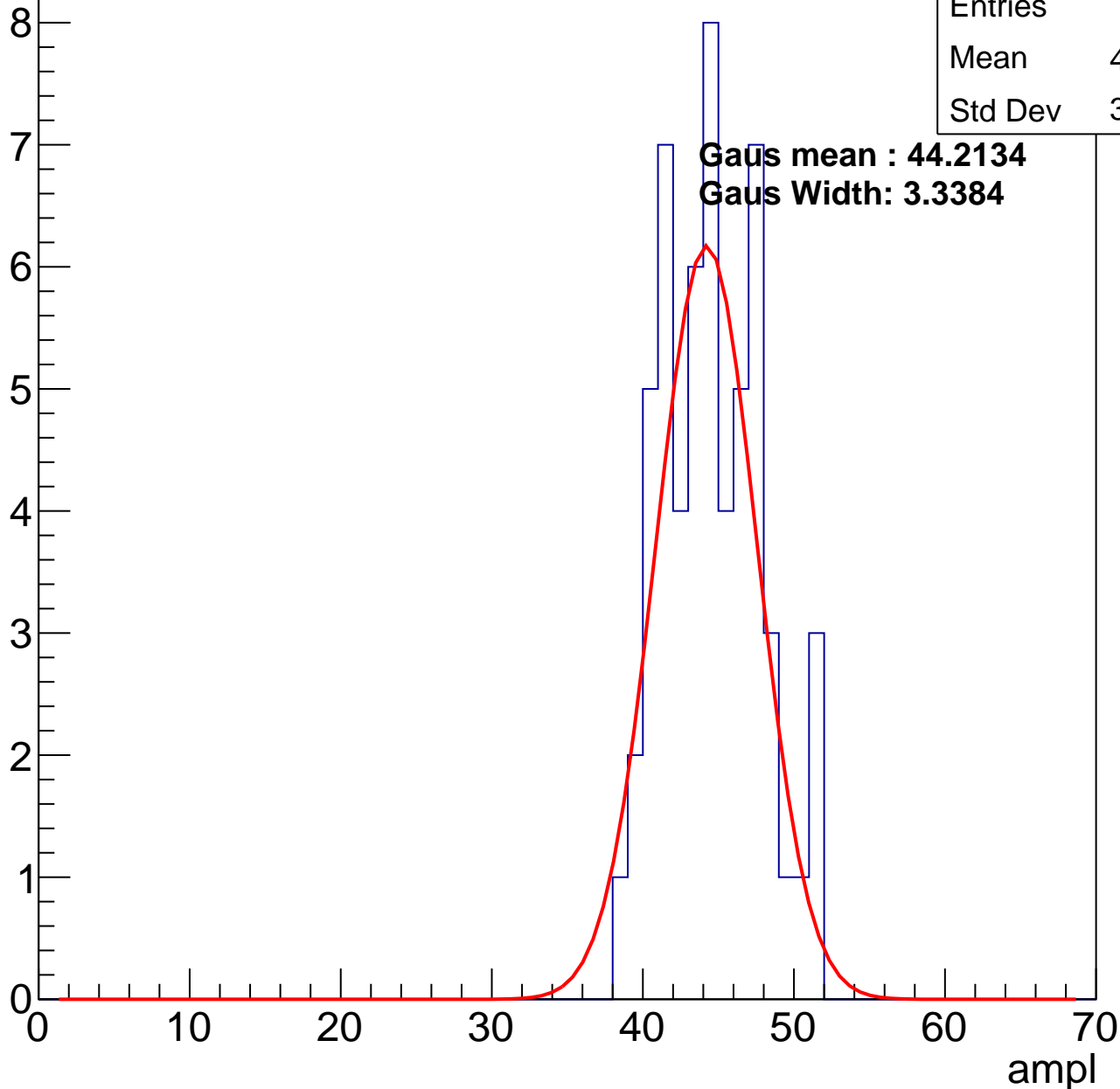
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	57
Mean	44.14
Std Dev	3.225

**Gaus mean : 44.2134**

**Gaus Width: 3.3384**

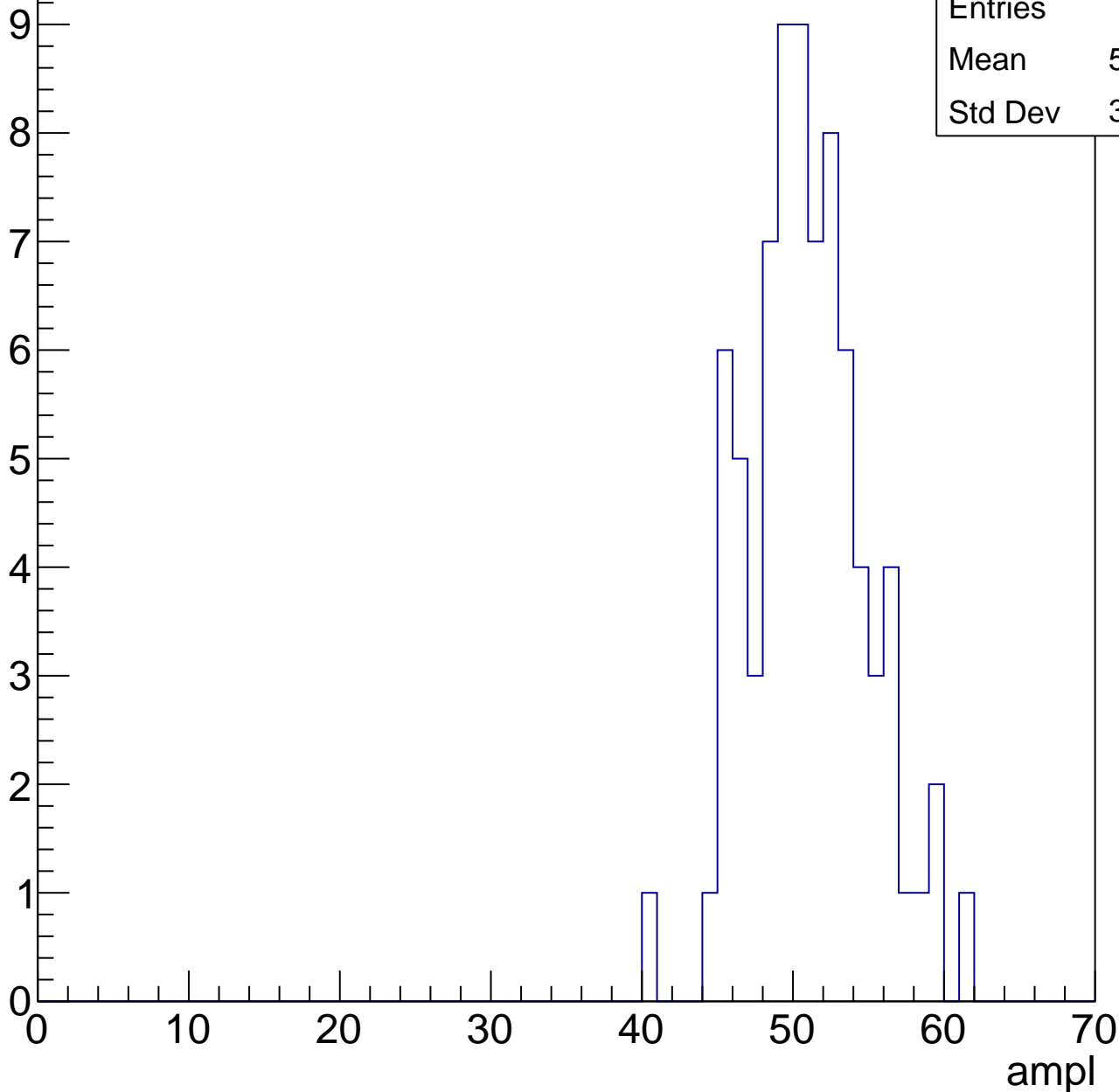


# B1L100S, U6-ch121, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	78
Mean	50.54
Std Dev	3.888

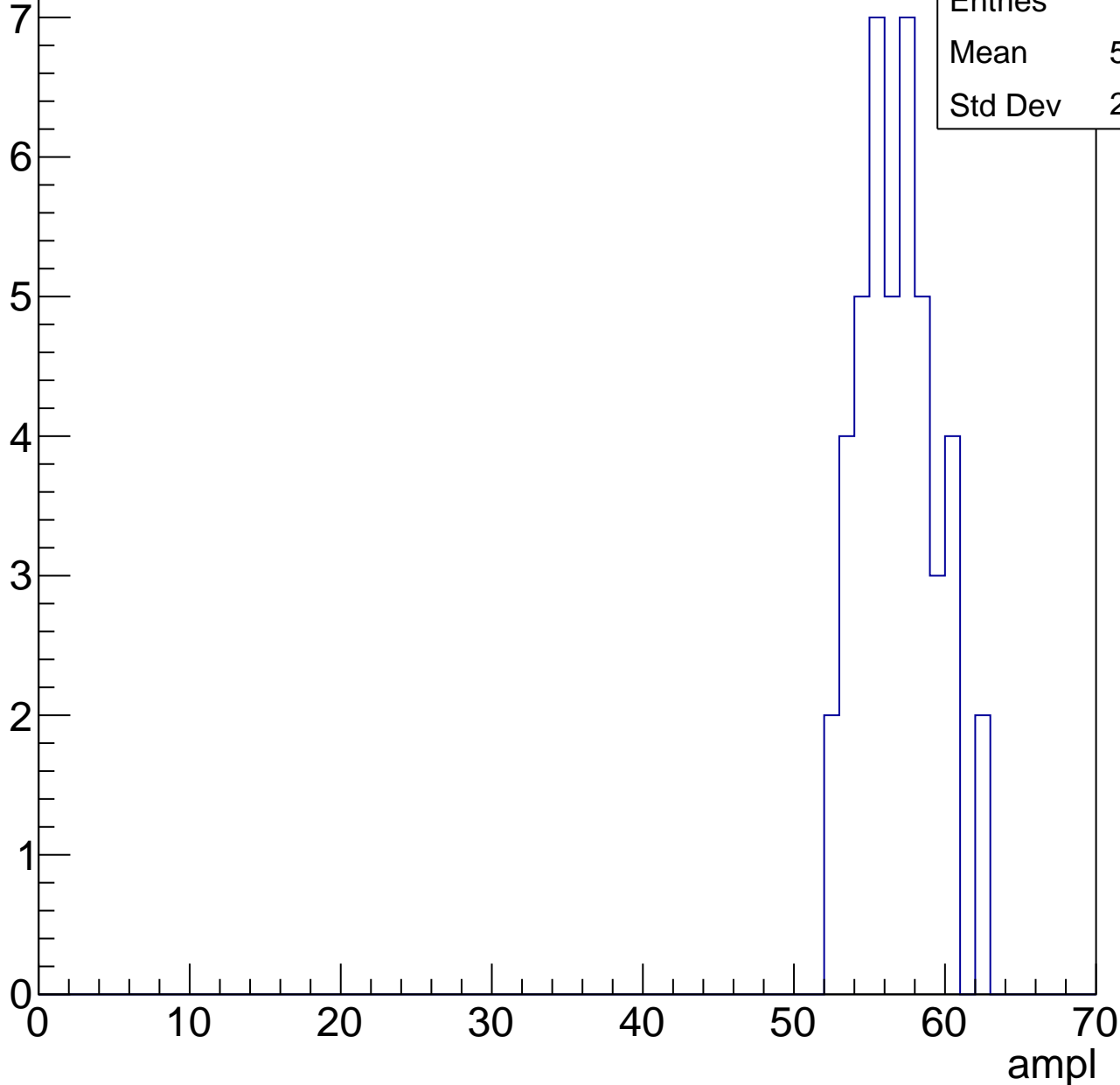


# B1L100S, U6-ch121, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	44
Mean	56.39
Std Dev	2.516

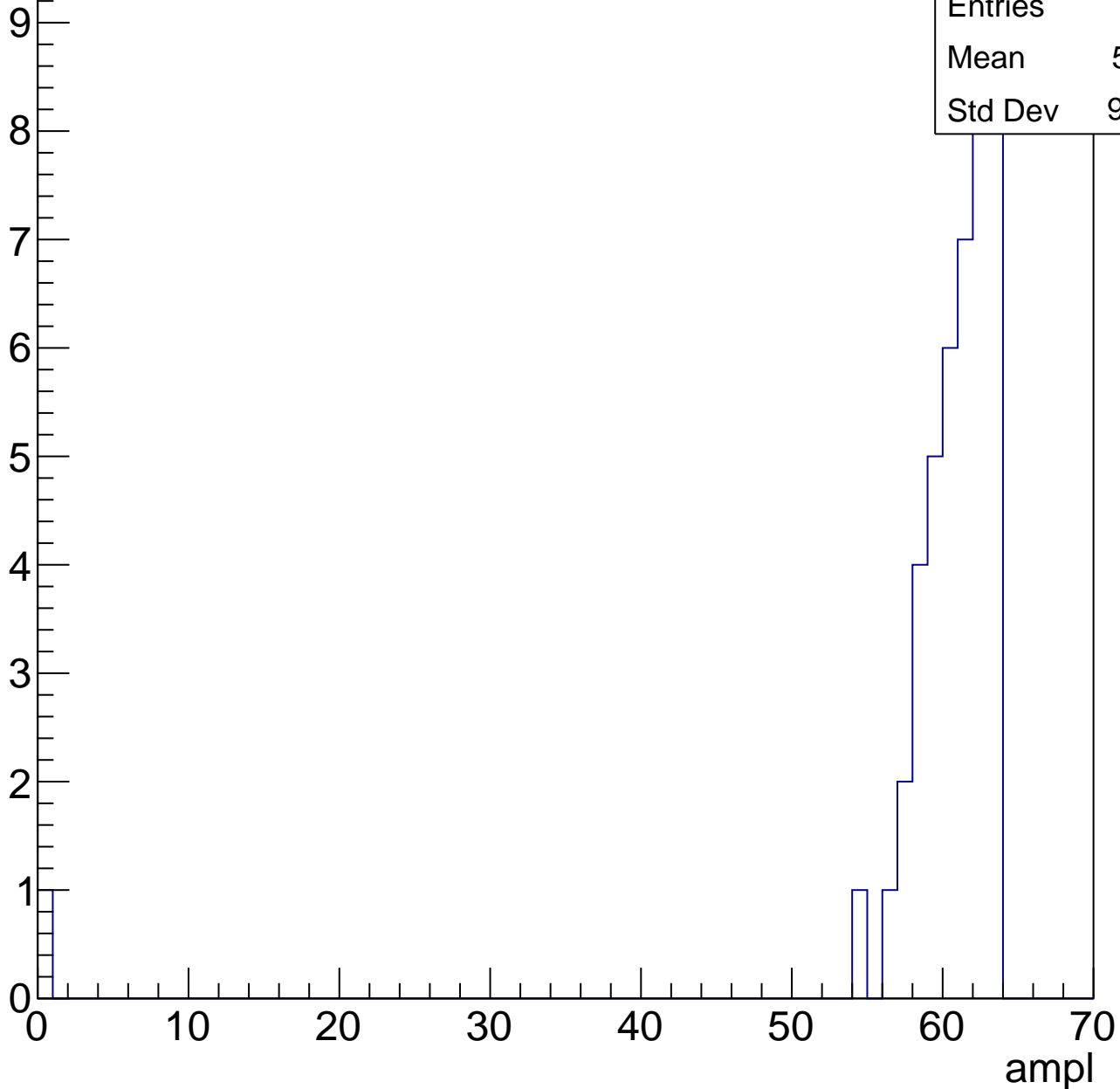


# B1L100S, U6-ch121, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	44
Mean	59.11
Std Dev	9.264



# B1L100S, U6-ch121, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

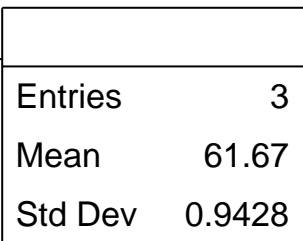
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	3
Mean	61.67
Std Dev	0.9428

0 10 20 30 40 50 60 70

ampl





# B1L100S, U6-ch121, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L100S, U6-ch122, adc0

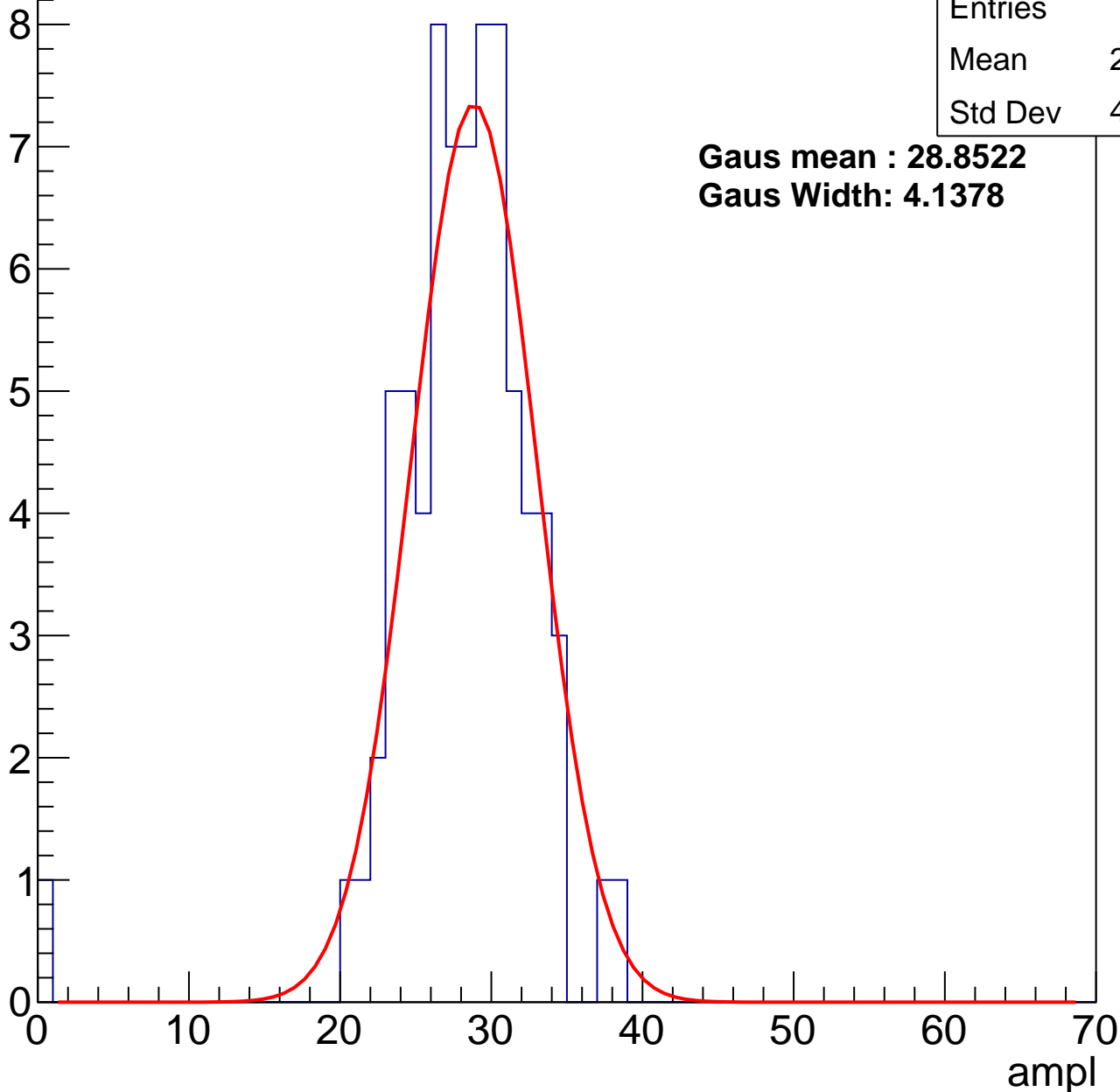
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	75
Mean	27.69
Std Dev	4.872

**Gaus mean : 28.8522**

**Gaus Width: 4.1378**



# B1L100S, U6-ch122, adc1

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	66
Mean	35
Std Dev	3.294

**Gaus mean : 35.5566**

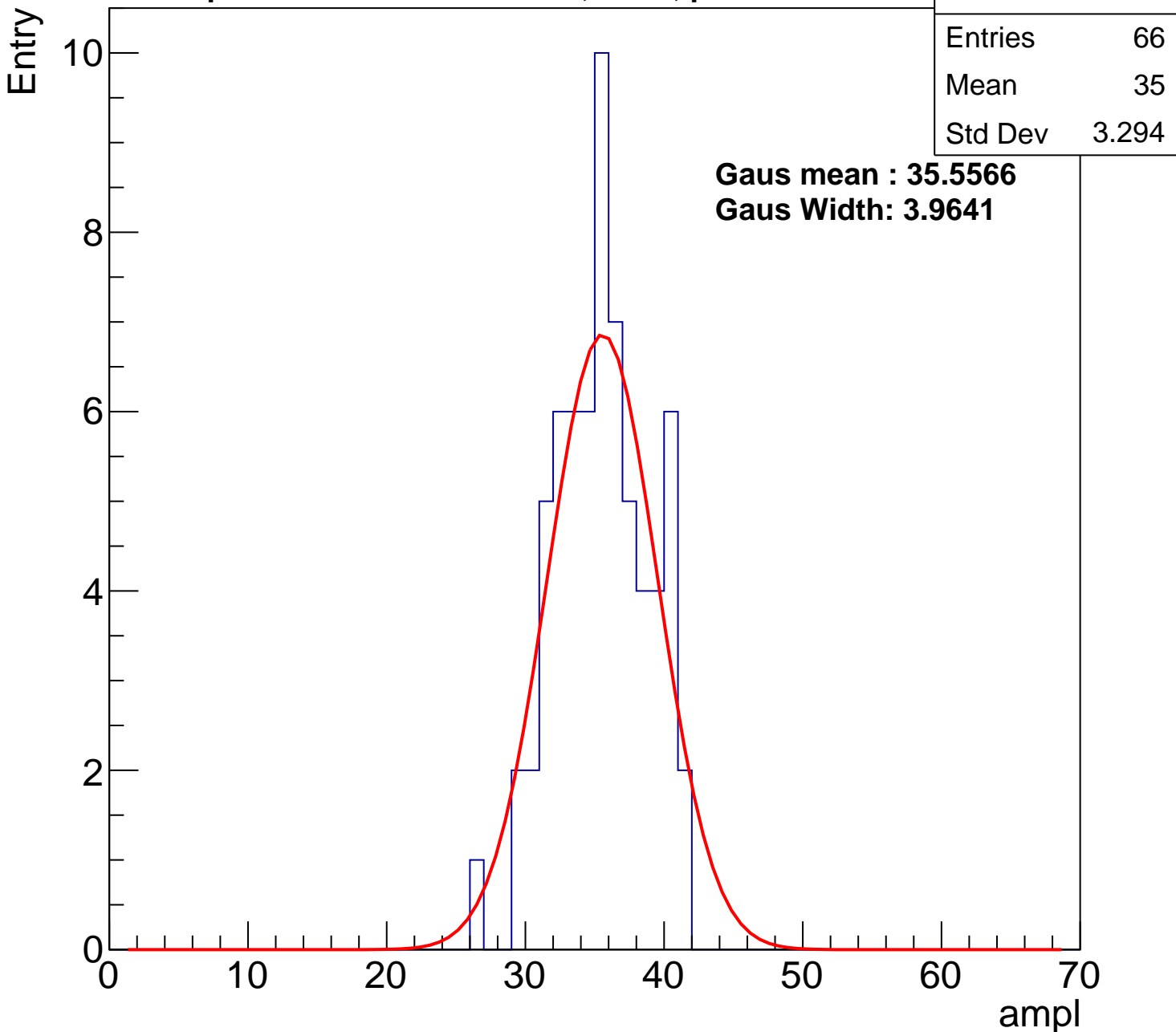
**Gaus Width: 3.9641**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L100S, U6-ch122, adc2

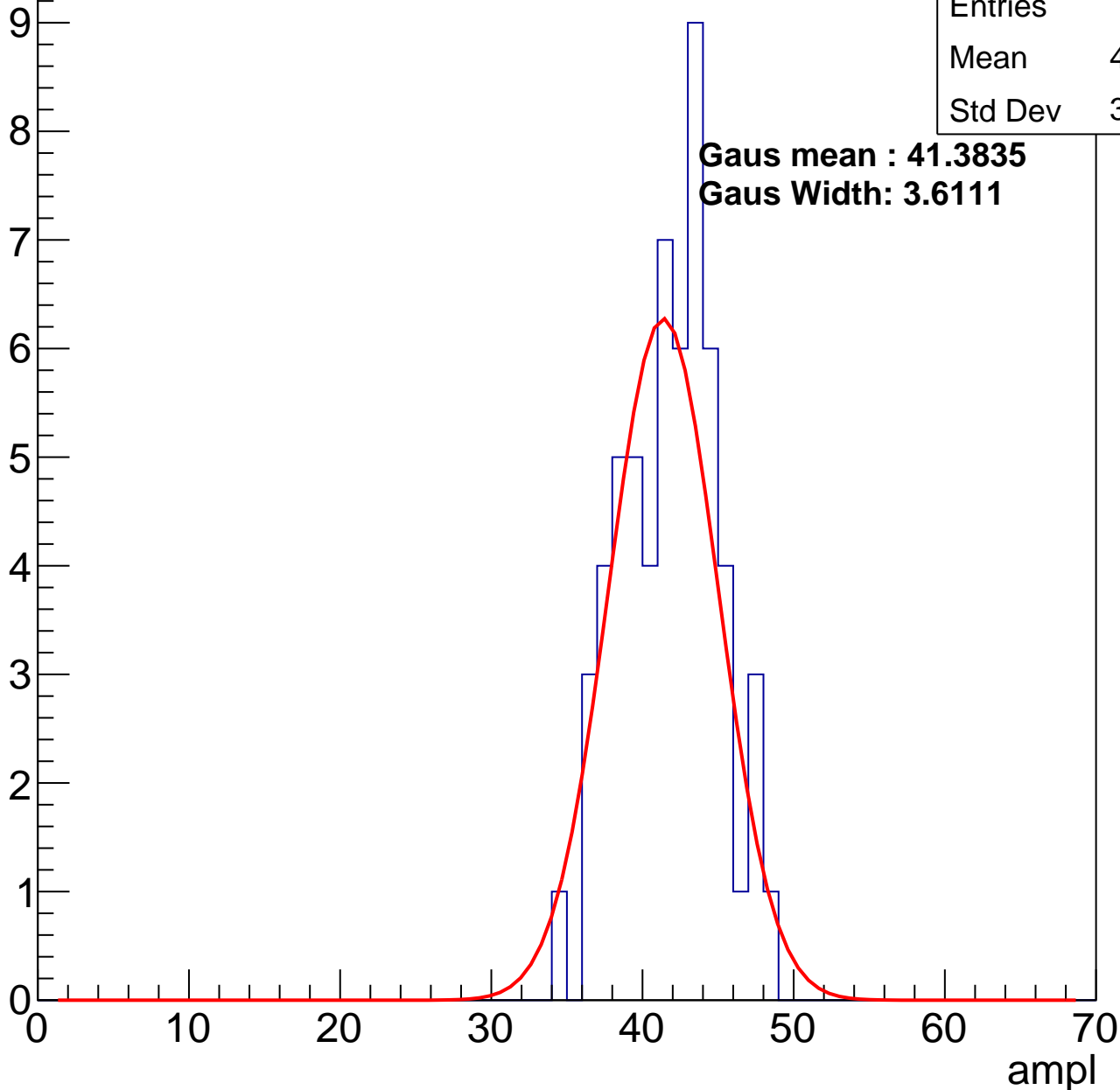
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	59
Mean	41.36
Std Dev	3.166

**Gaus mean : 41.3835**

**Gaus Width: 3.6111**

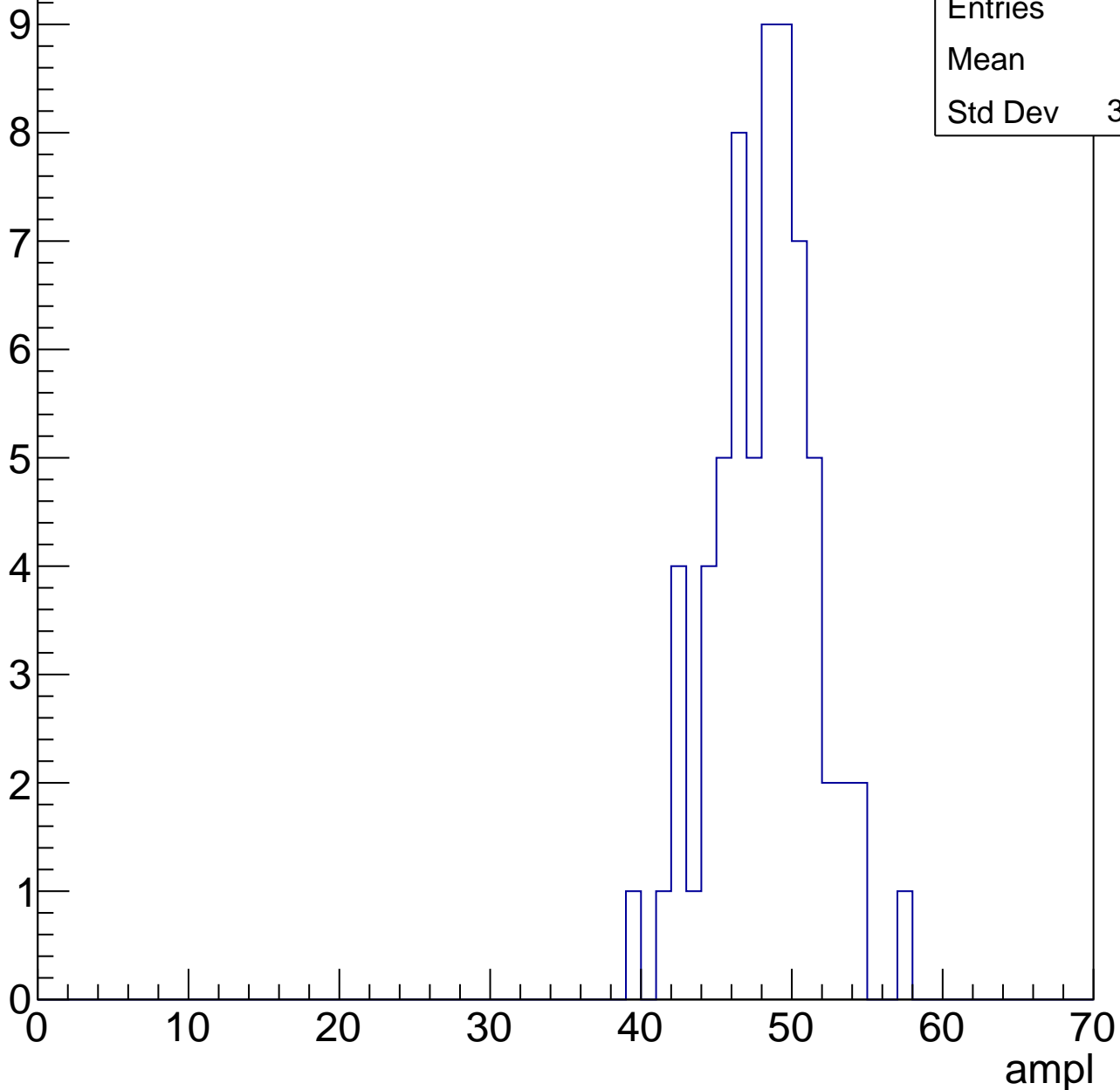


# B1L100S, U6-ch122, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	66
Mean	47.7
Std Dev	3.384

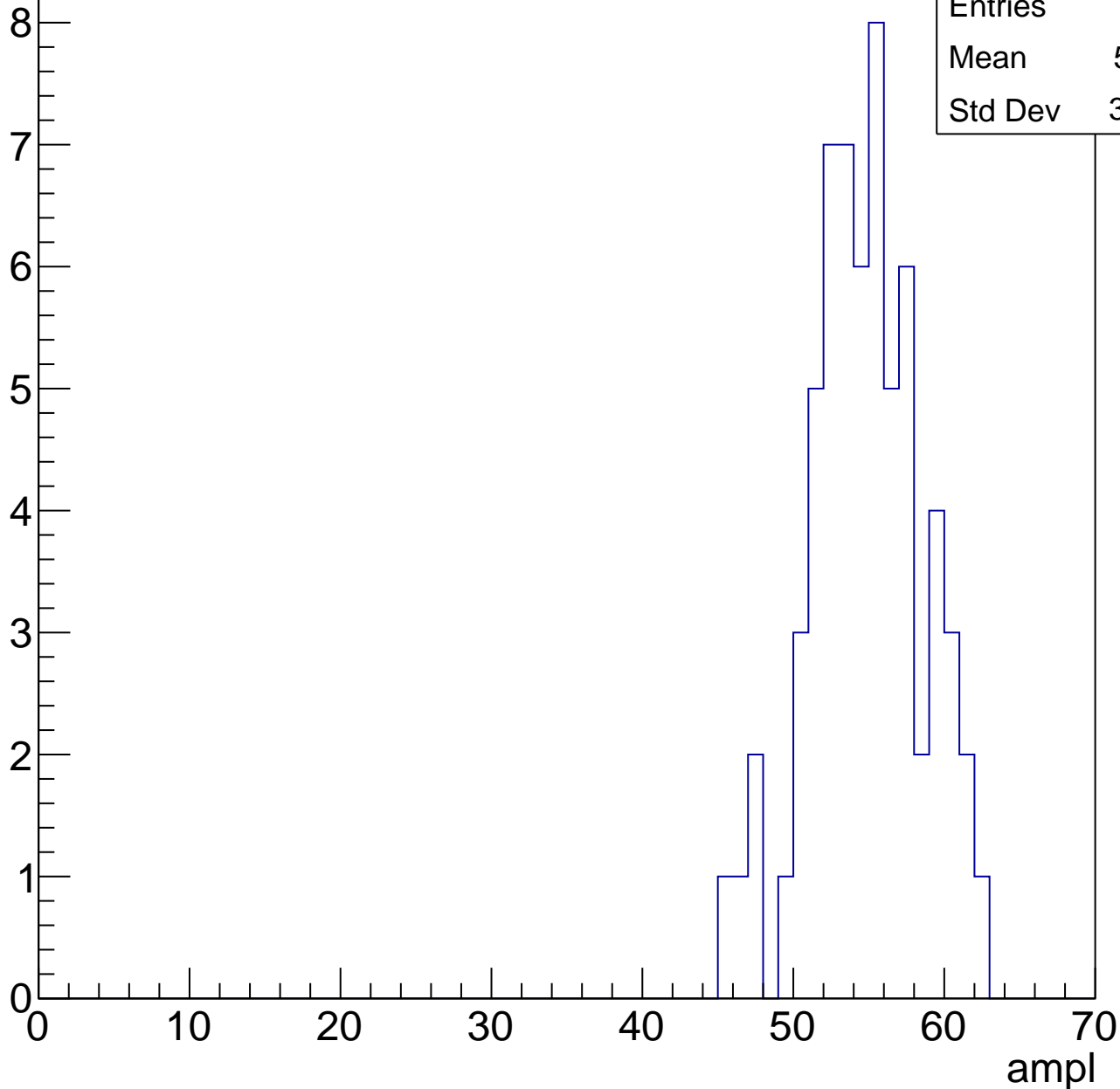


# B1L100S, U6-ch122, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	64
Mean	54.31
Std Dev	3.695

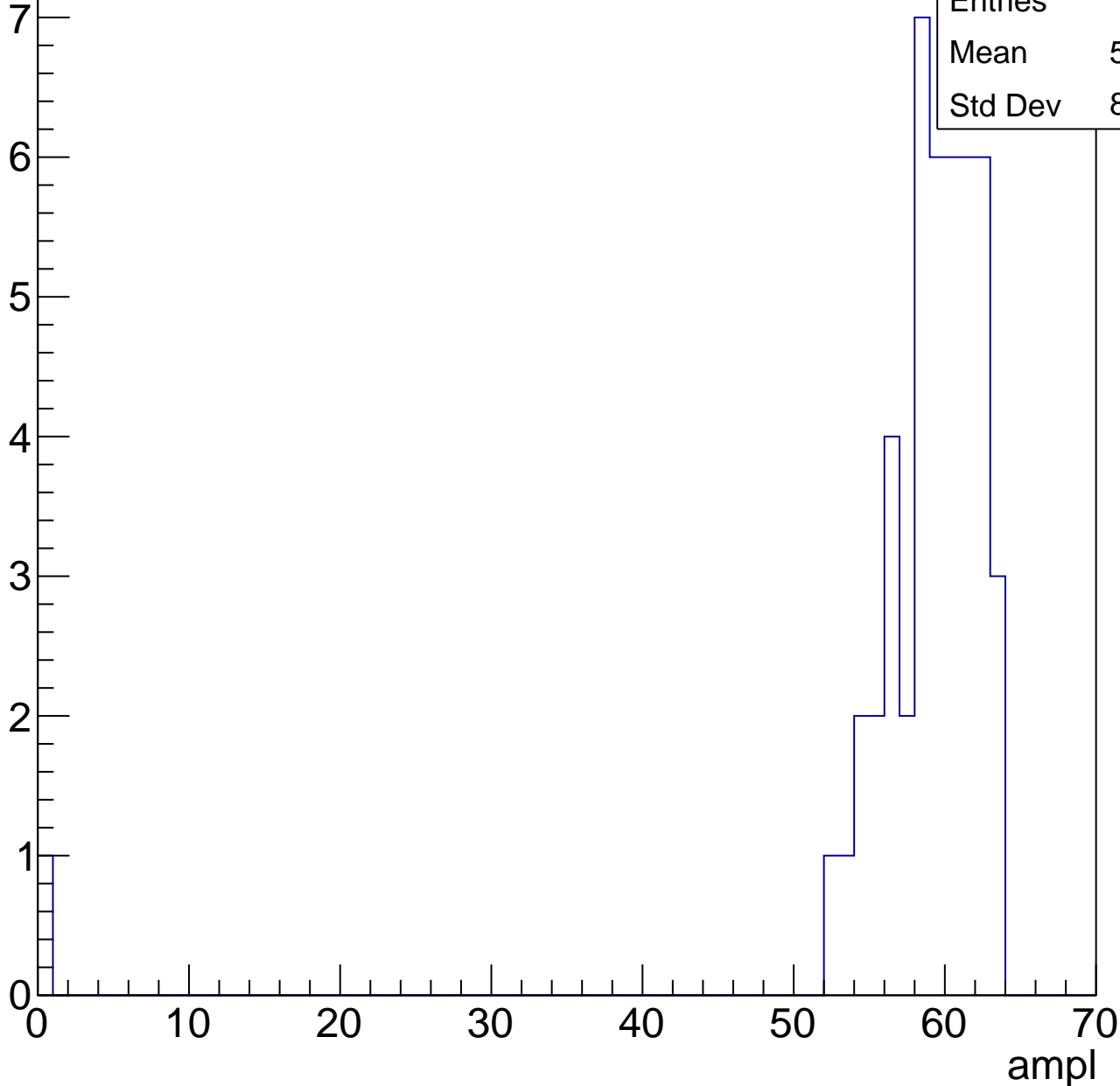


# B1L100S, U6-ch122, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	47
Mean	57.62
Std Dev	8.922

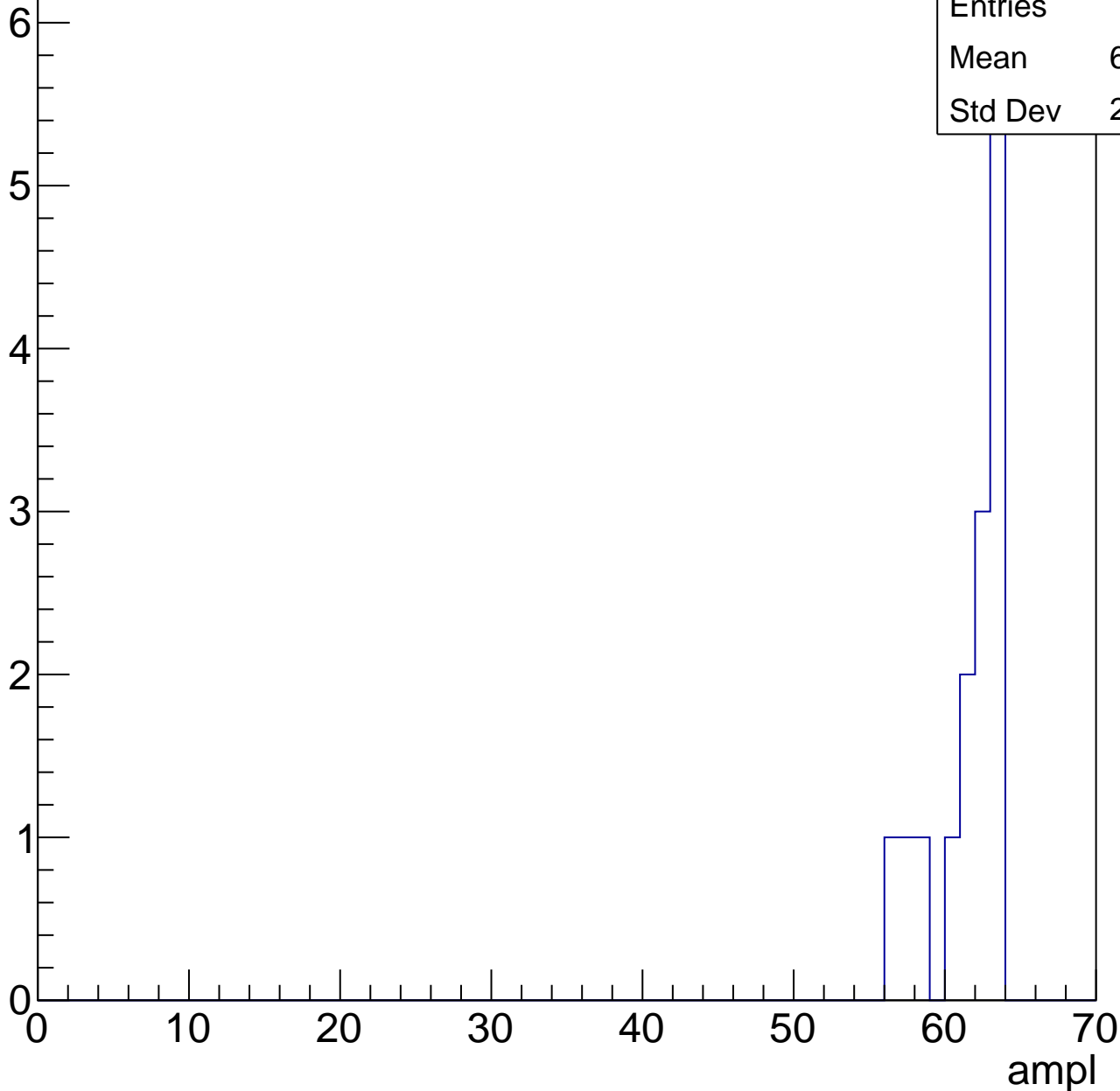


# B1L100S, U6-ch122, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	15
Mean	61.13
Std Dev	2.276





# B1L100S, U6-ch122, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



# B1L100S, U6-ch123, adc0

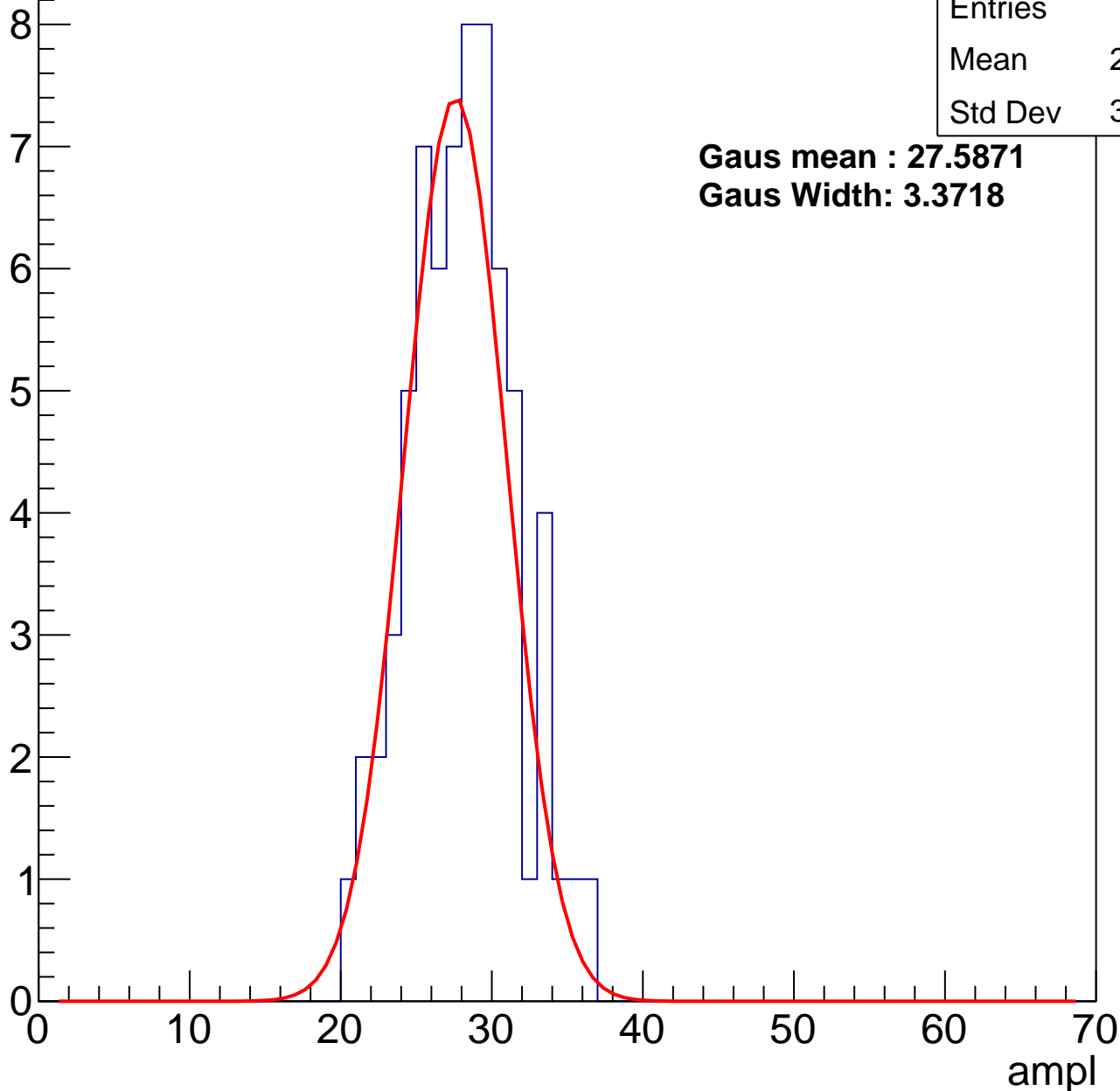
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	68
Mean	27.57
Std Dev	3.457

**Gaus mean : 27.5871**

**Gaus Width: 3.3718**



# B1L100S, U6-ch123, adc1

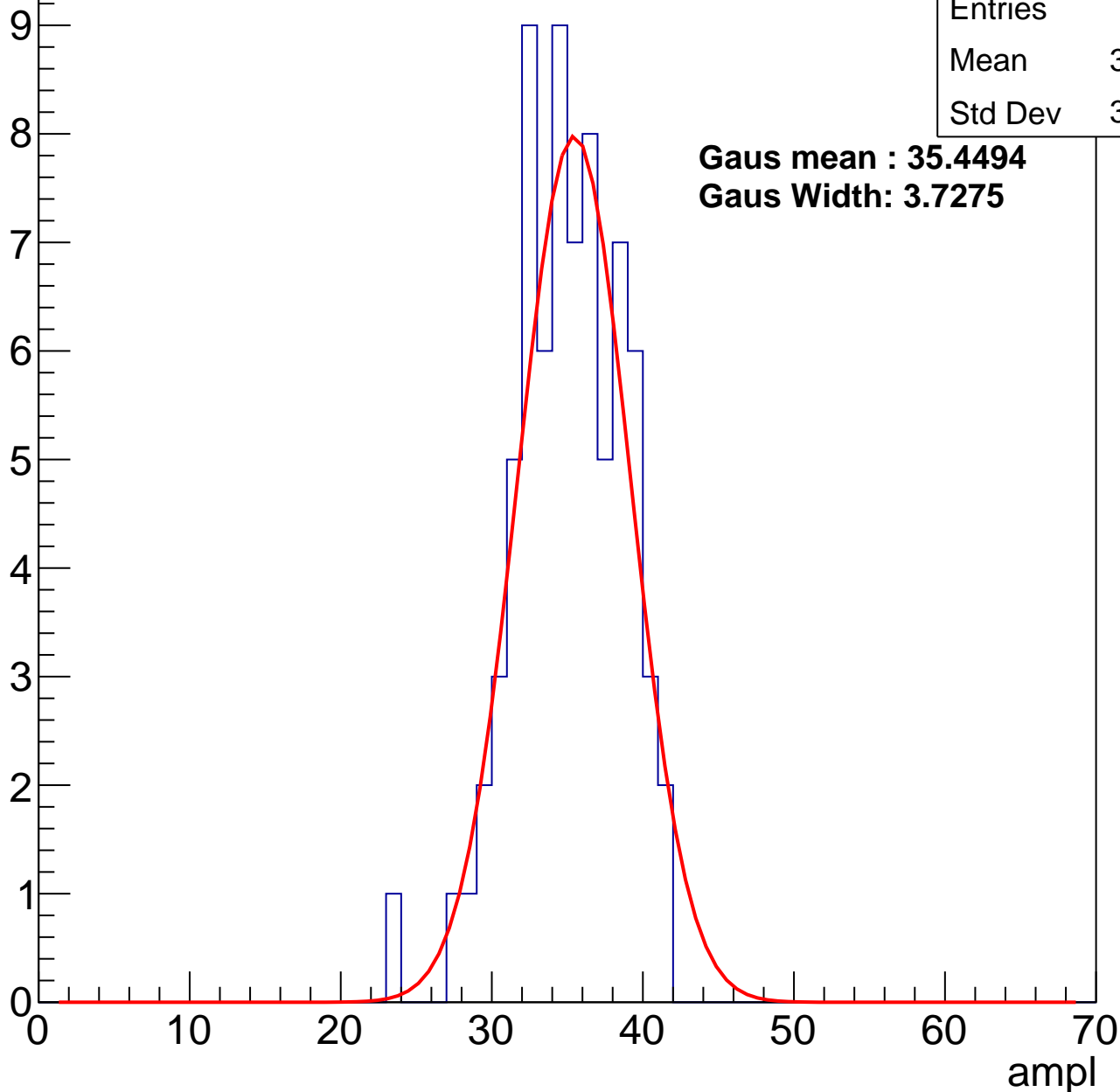
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	75
Mean	34.57
Std Dev	3.499

**Gaus mean : 35.4494**

**Gaus Width: 3.7275**



# B1L100S, U6-ch123, adc2

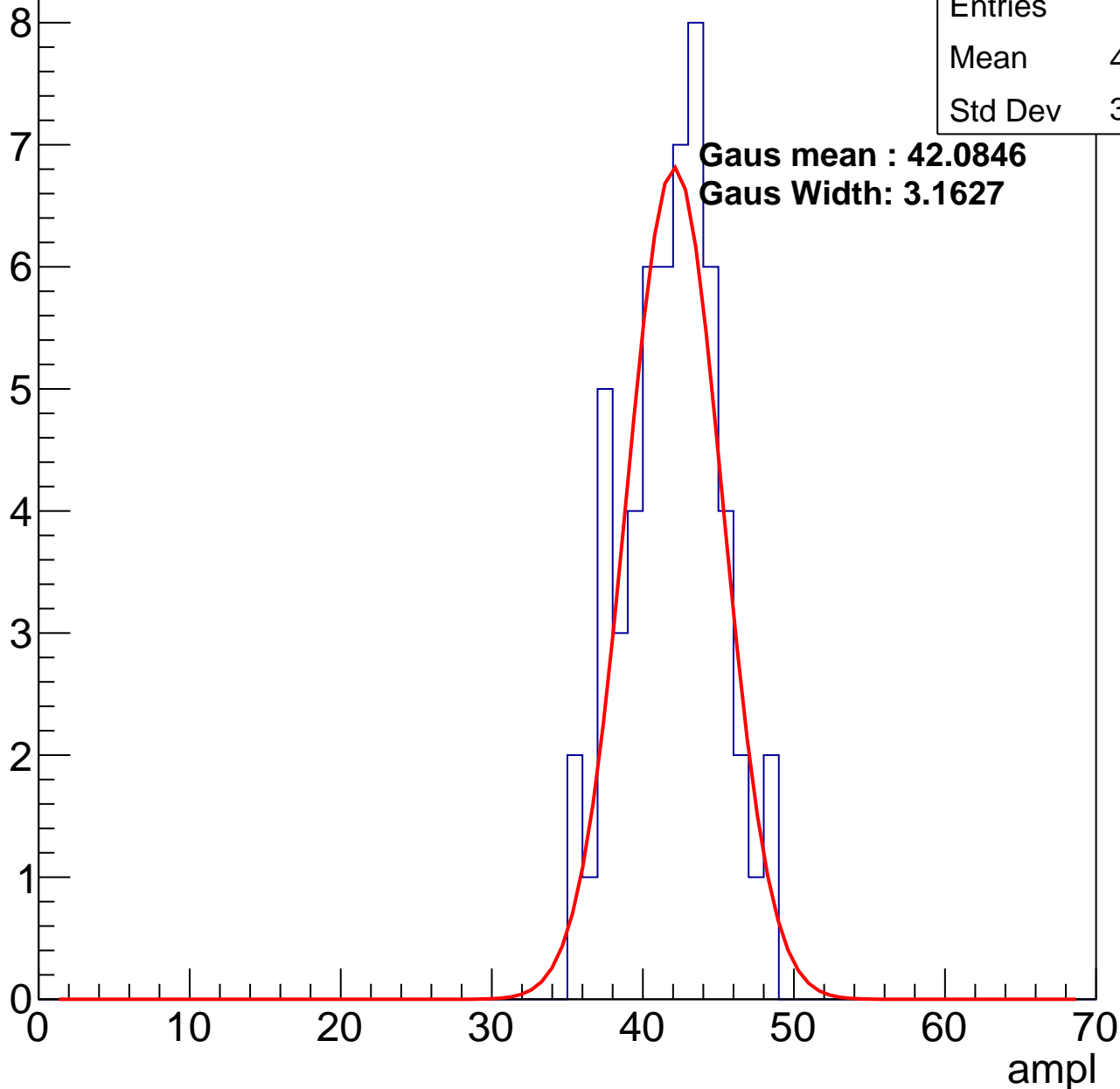
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	57
Mean	41.47
Std Dev	3.118

**Gaus mean : 42.0846**

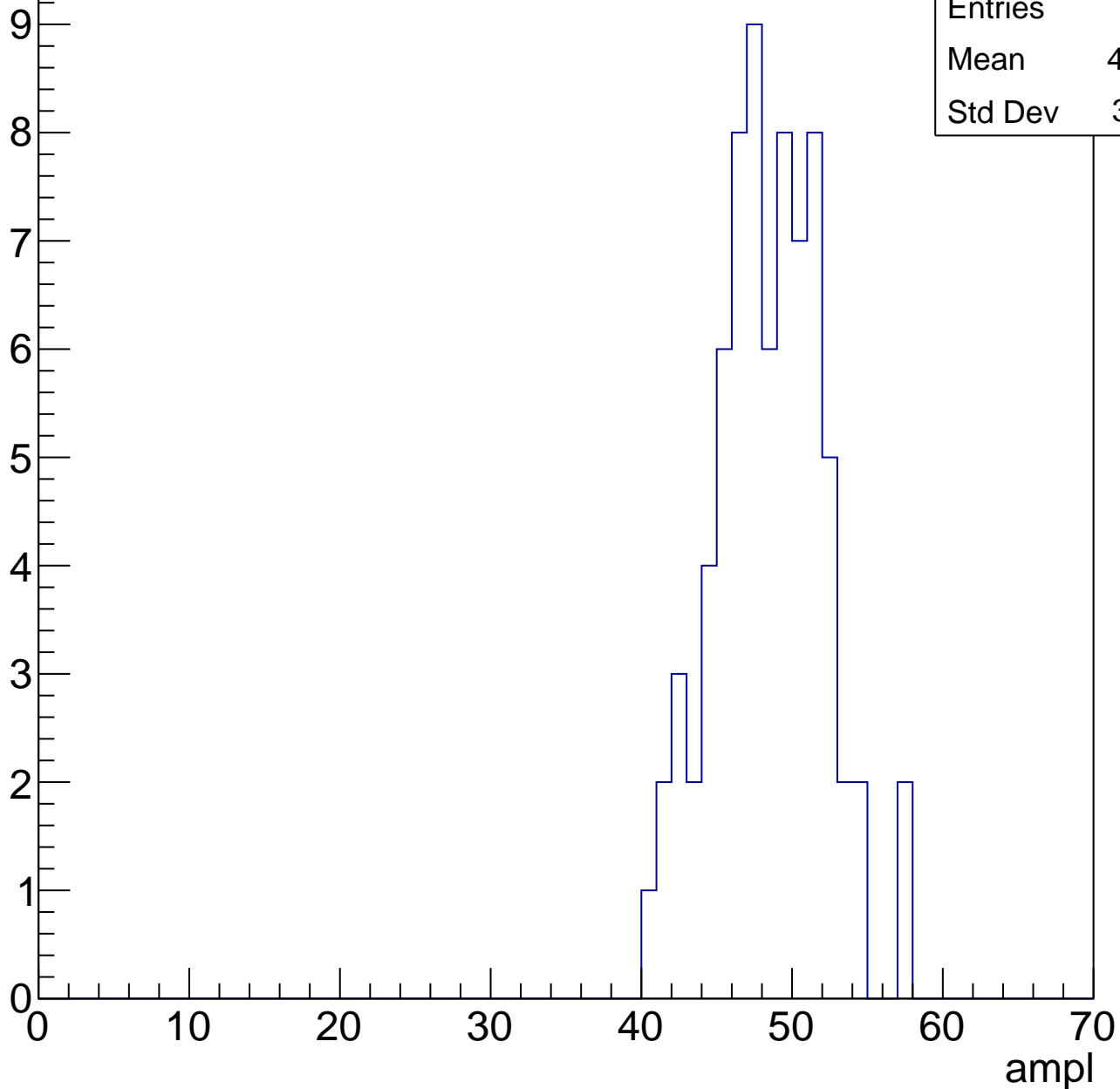
**Gaus Width: 3.1627**



# B1L100S, U6-ch123, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



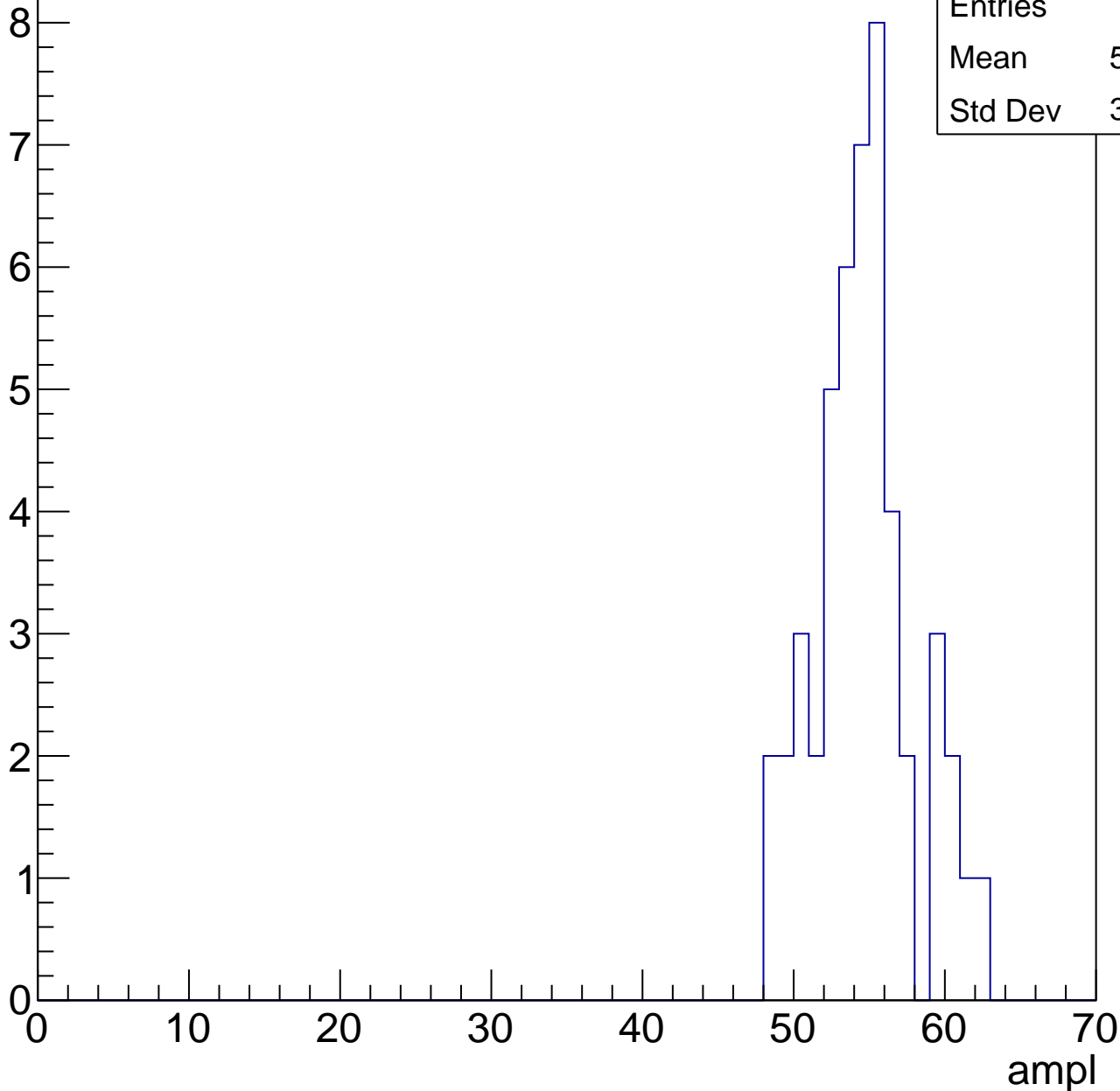
Entries	75
Mean	47.96
Std Dev	3.561

# B1L100S, U6-ch123, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

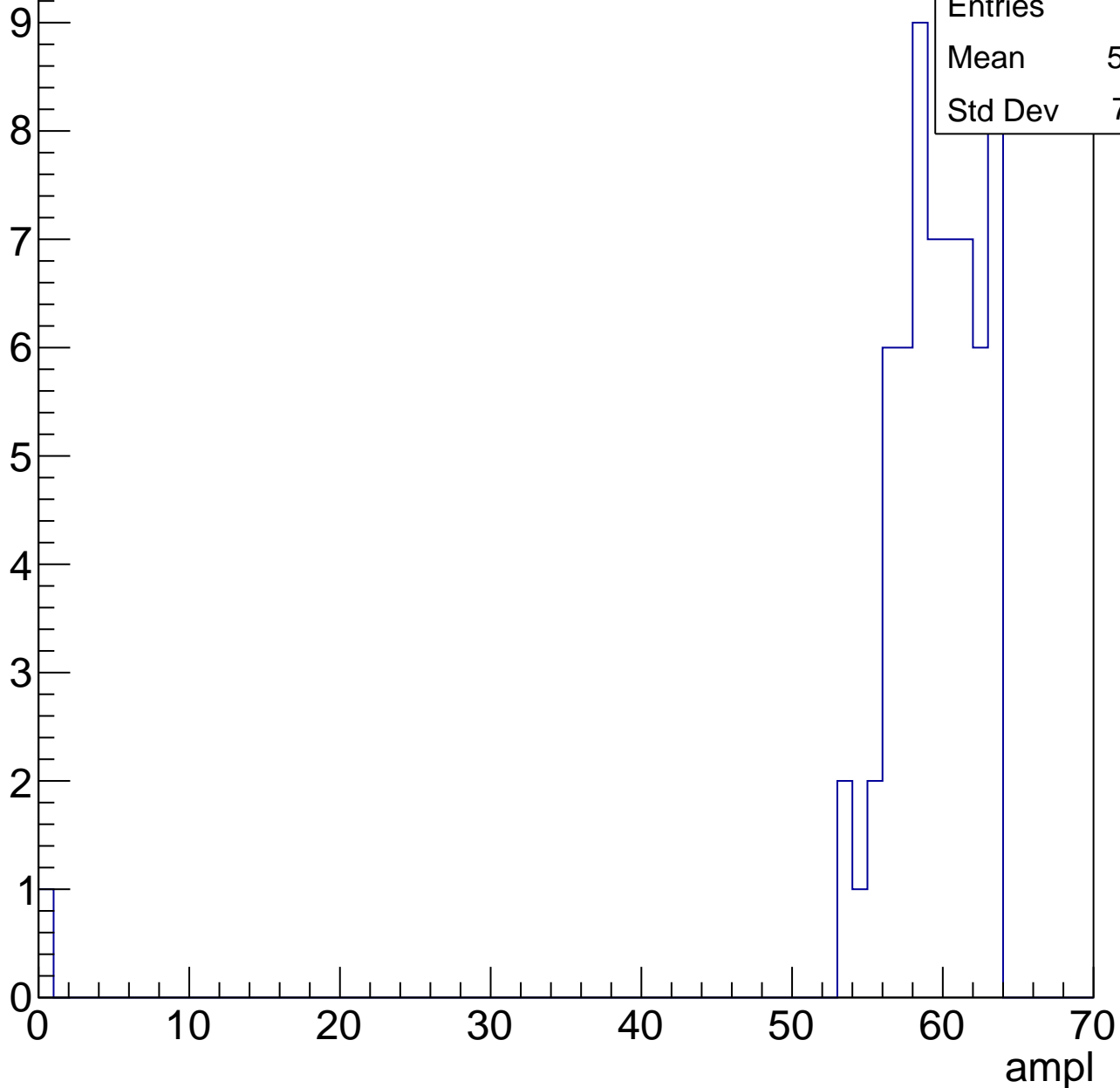
Entries	48
Mean	54.17
Std Dev	3.274



# B1L100S, U6-ch123, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

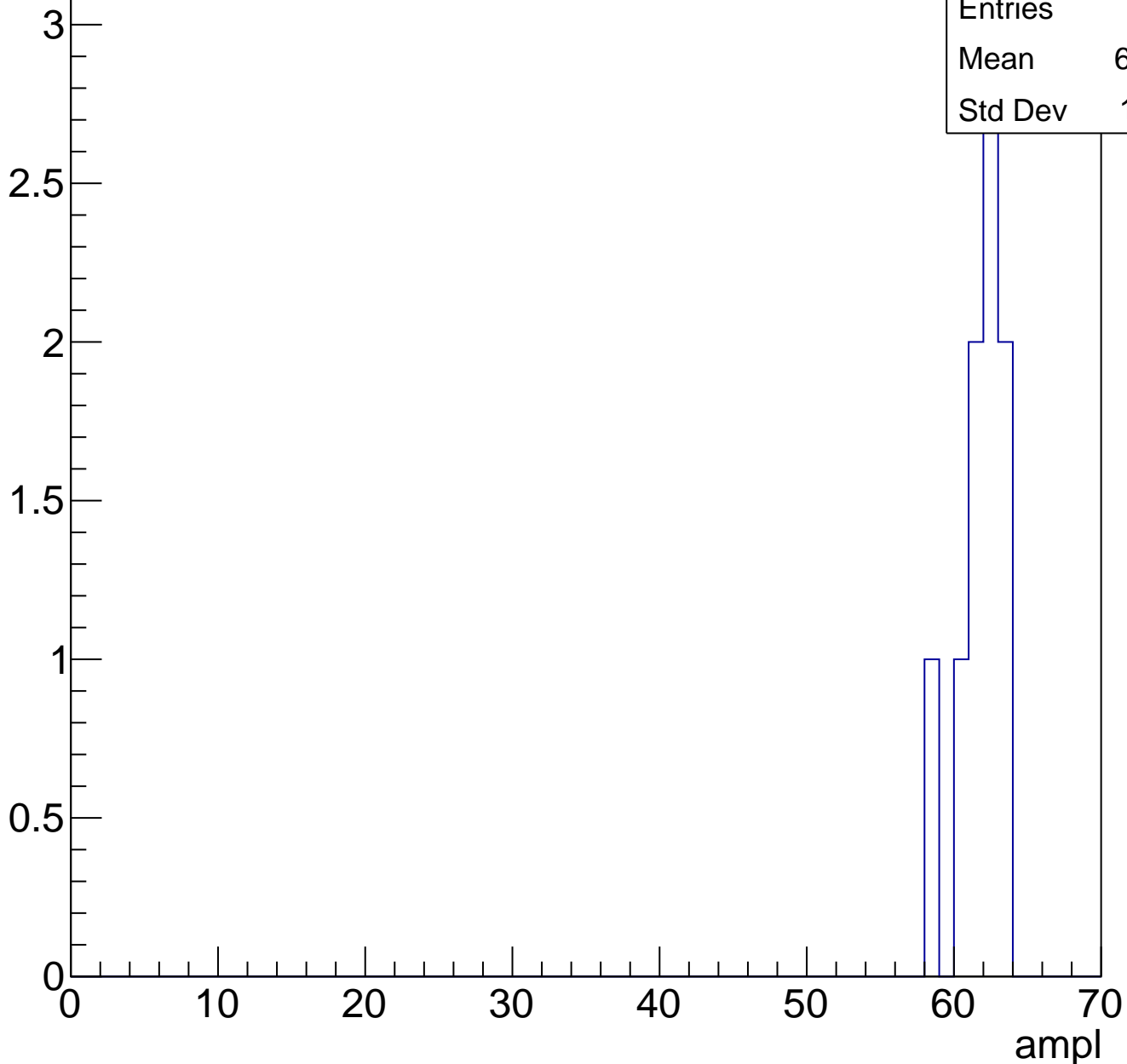
Entry



# B1L100S, U6-ch123, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry





# B1L100S, U6-ch123, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L100S, U6-ch124, adc0

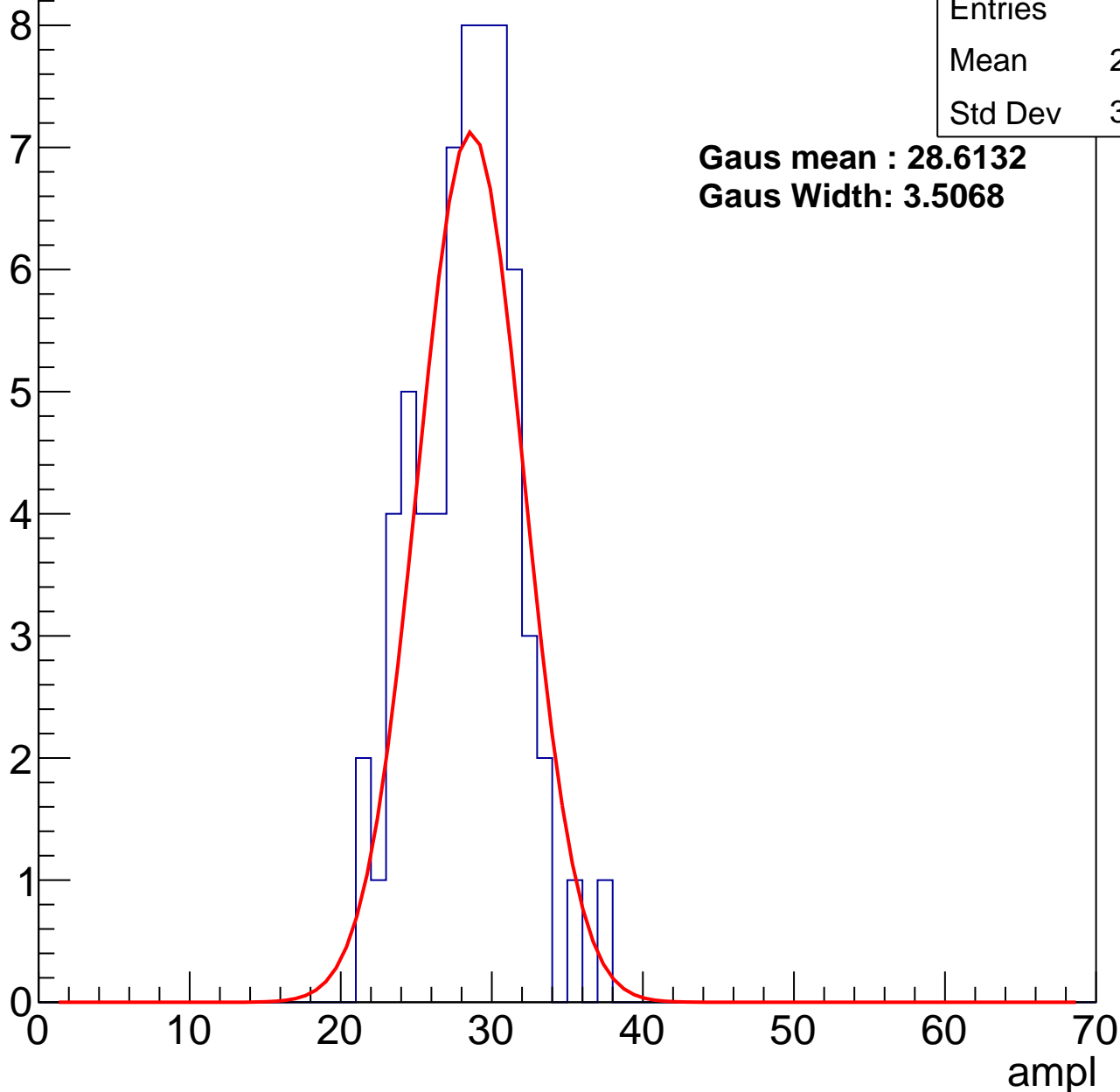
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	64
Mean	27.89
Std Dev	3.294

**Gaus mean : 28.6132**

**Gaus Width: 3.5068**



# B1L100S, U6-ch124, adc1

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	86
Mean	35.45
Std Dev	4.002

**Gaus mean : 36.1590**

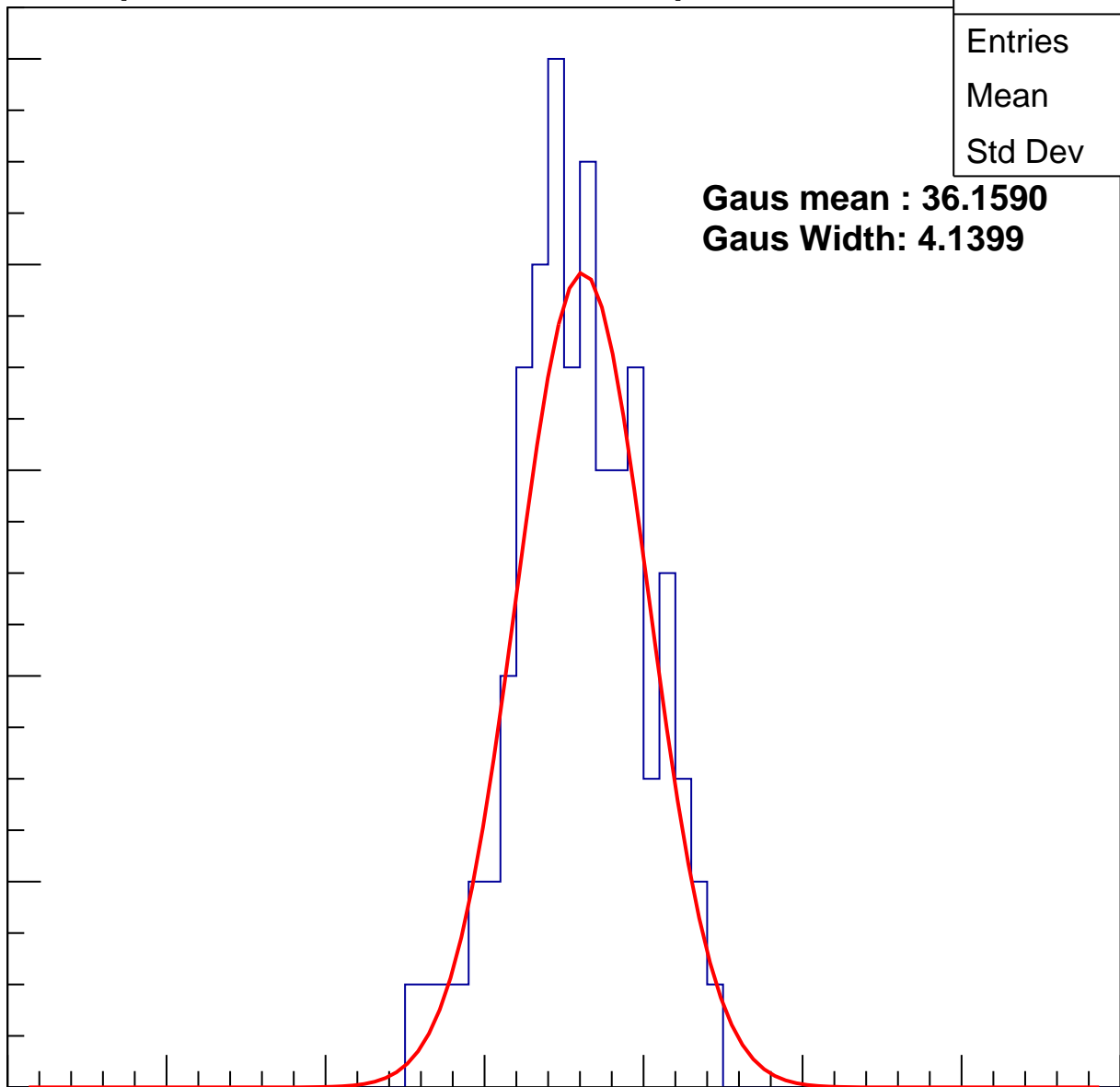
**Gaus Width: 4.1399**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L100S, U6-ch124, adc2

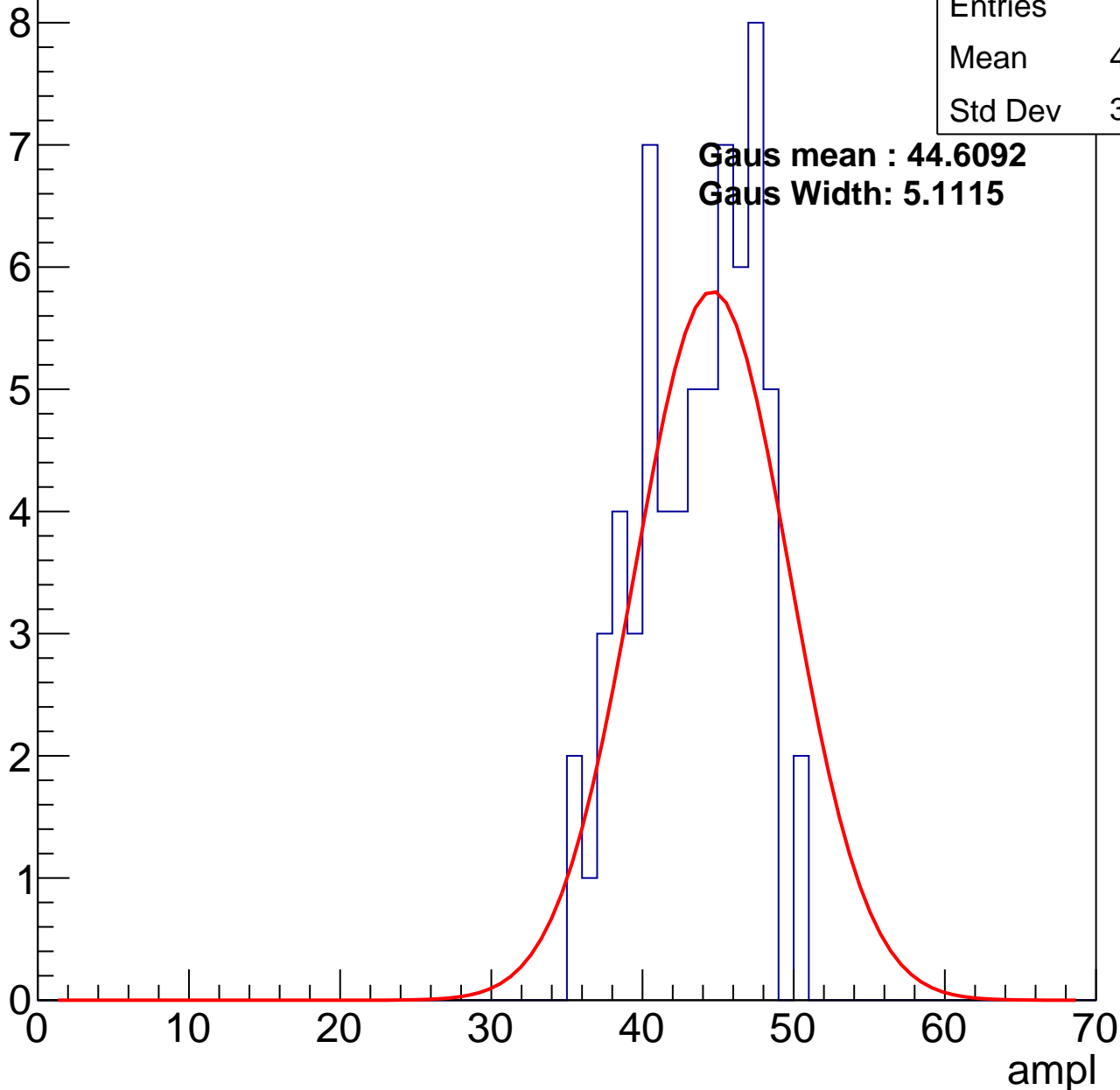
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	66
Mean	43.03
Std Dev	3.802

**Gaus mean : 44.6092**

**Gaus Width: 5.1115**

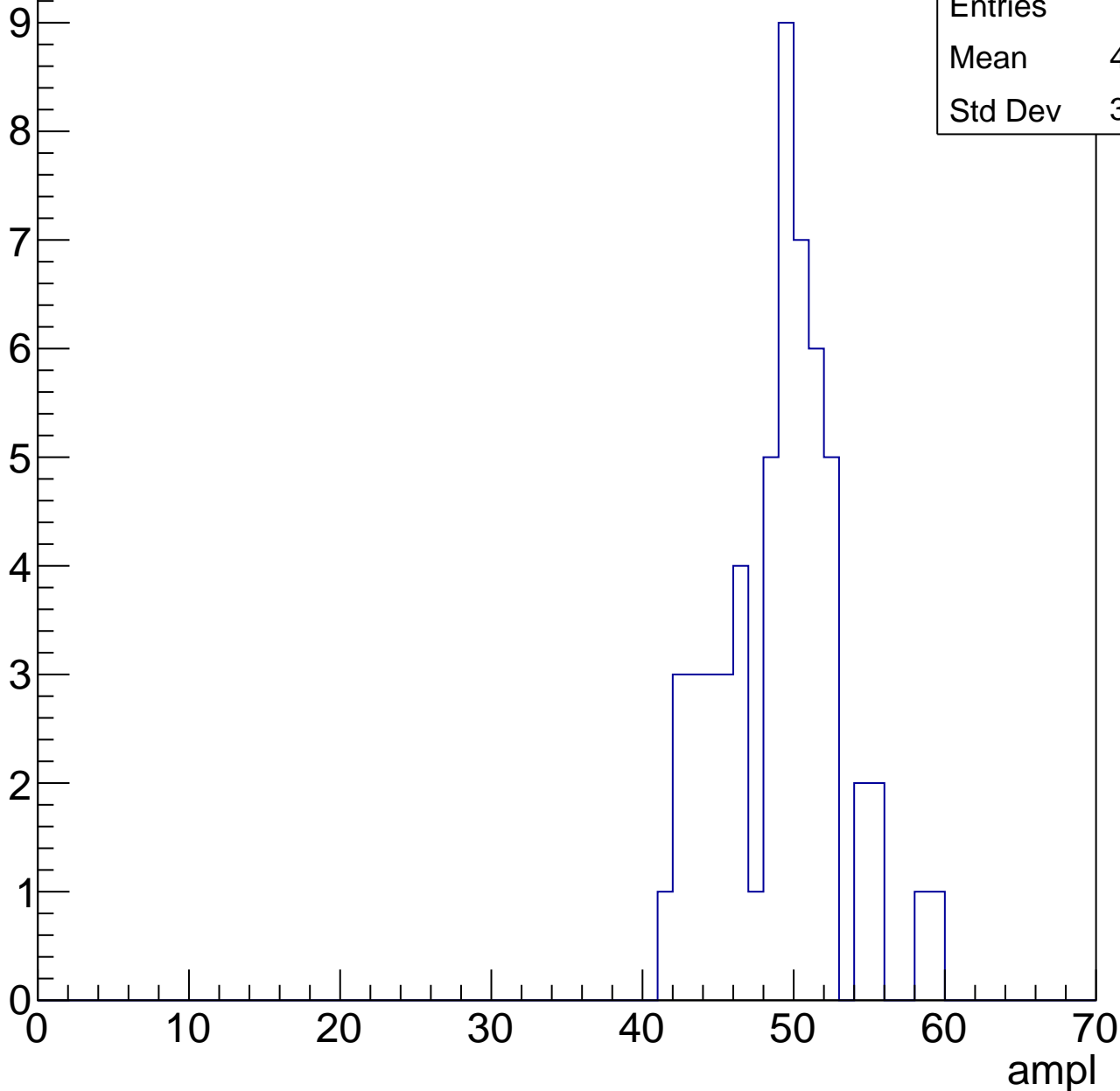


# B1L100S, U6-ch124, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	56
Mean	48.68
Std Dev	3.919

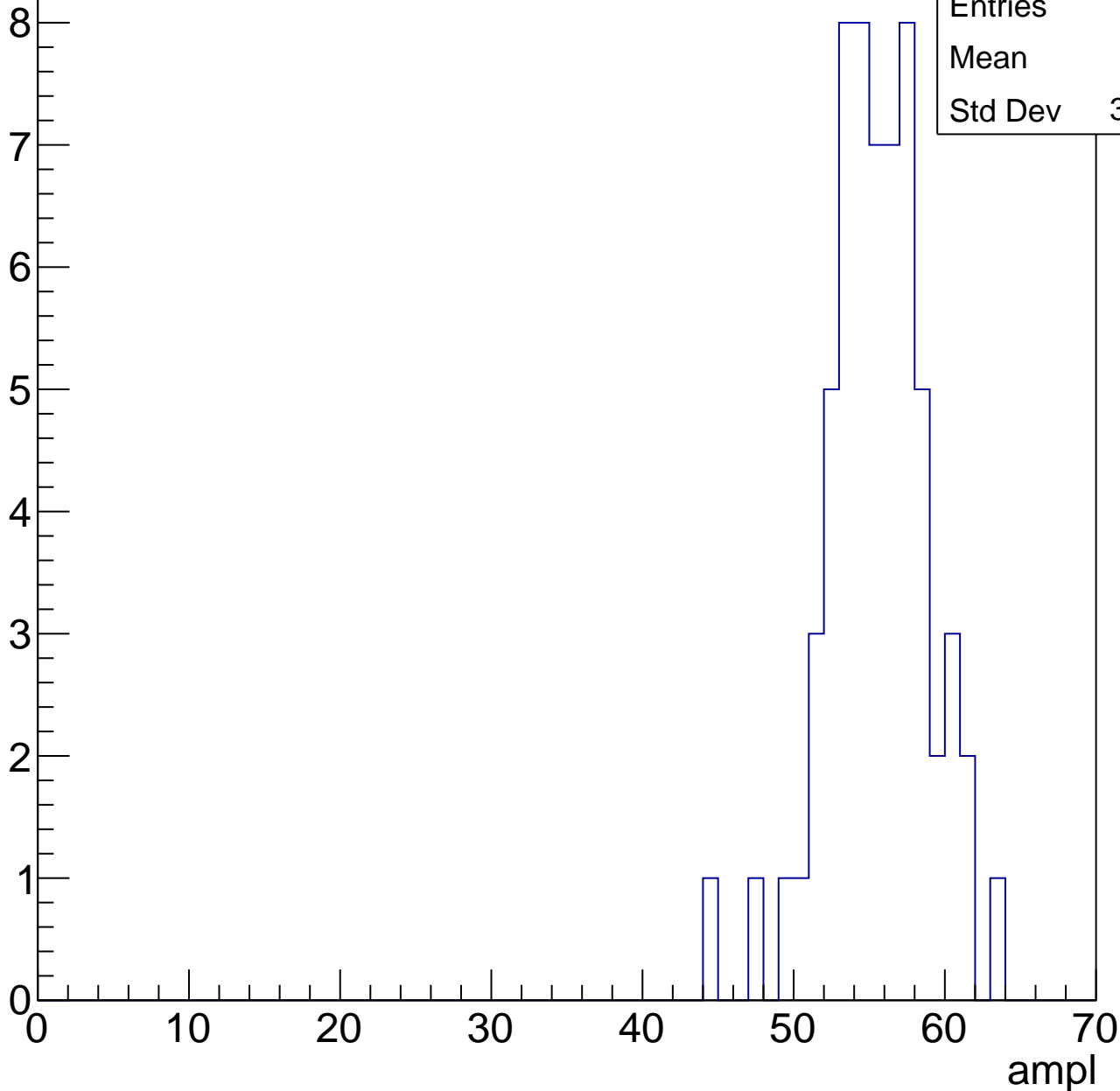


# B1L100S, U6-ch124, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	63
Mean	55
Std Dev	3.348

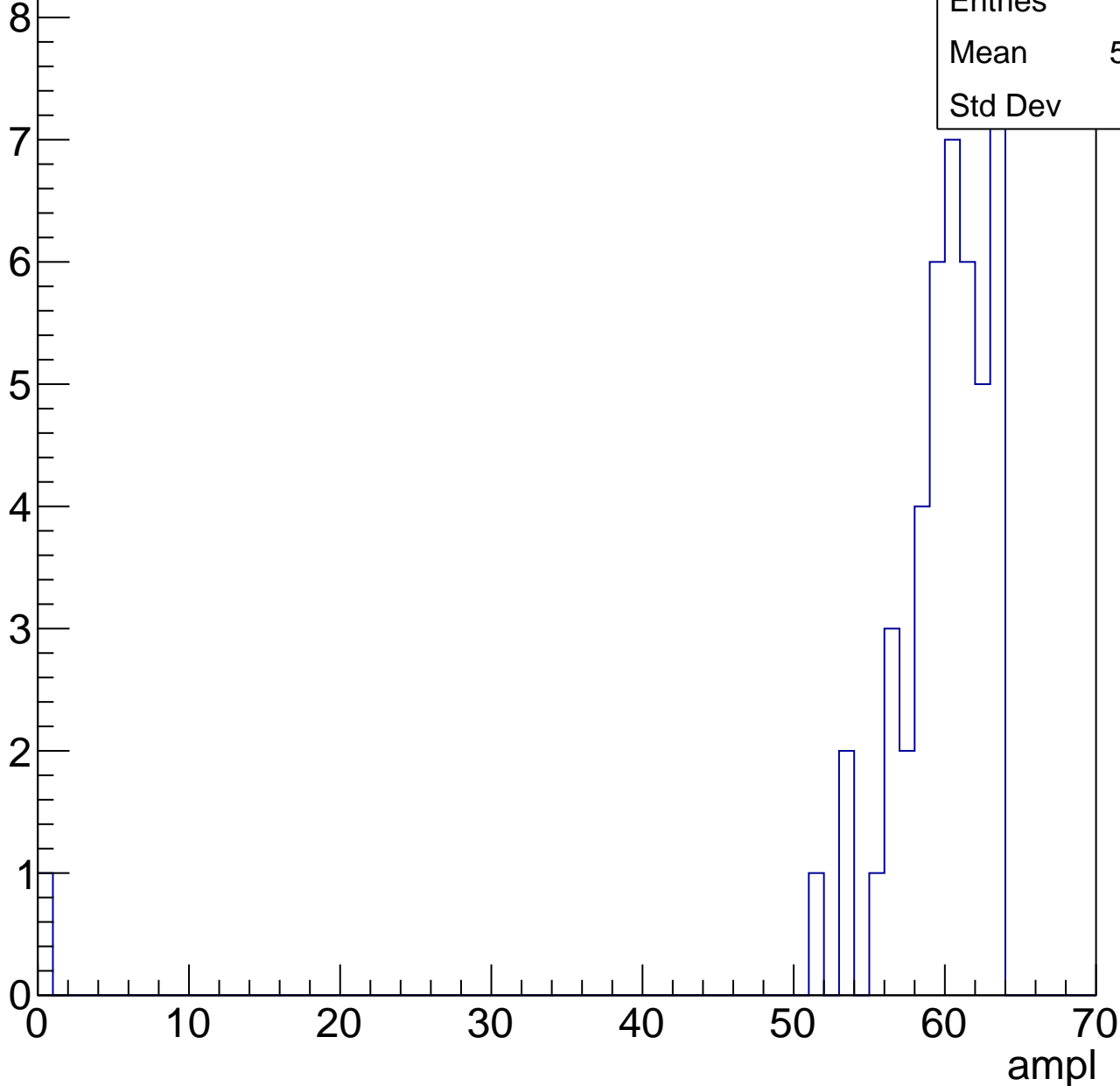


# B1L100S, U6-ch124, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

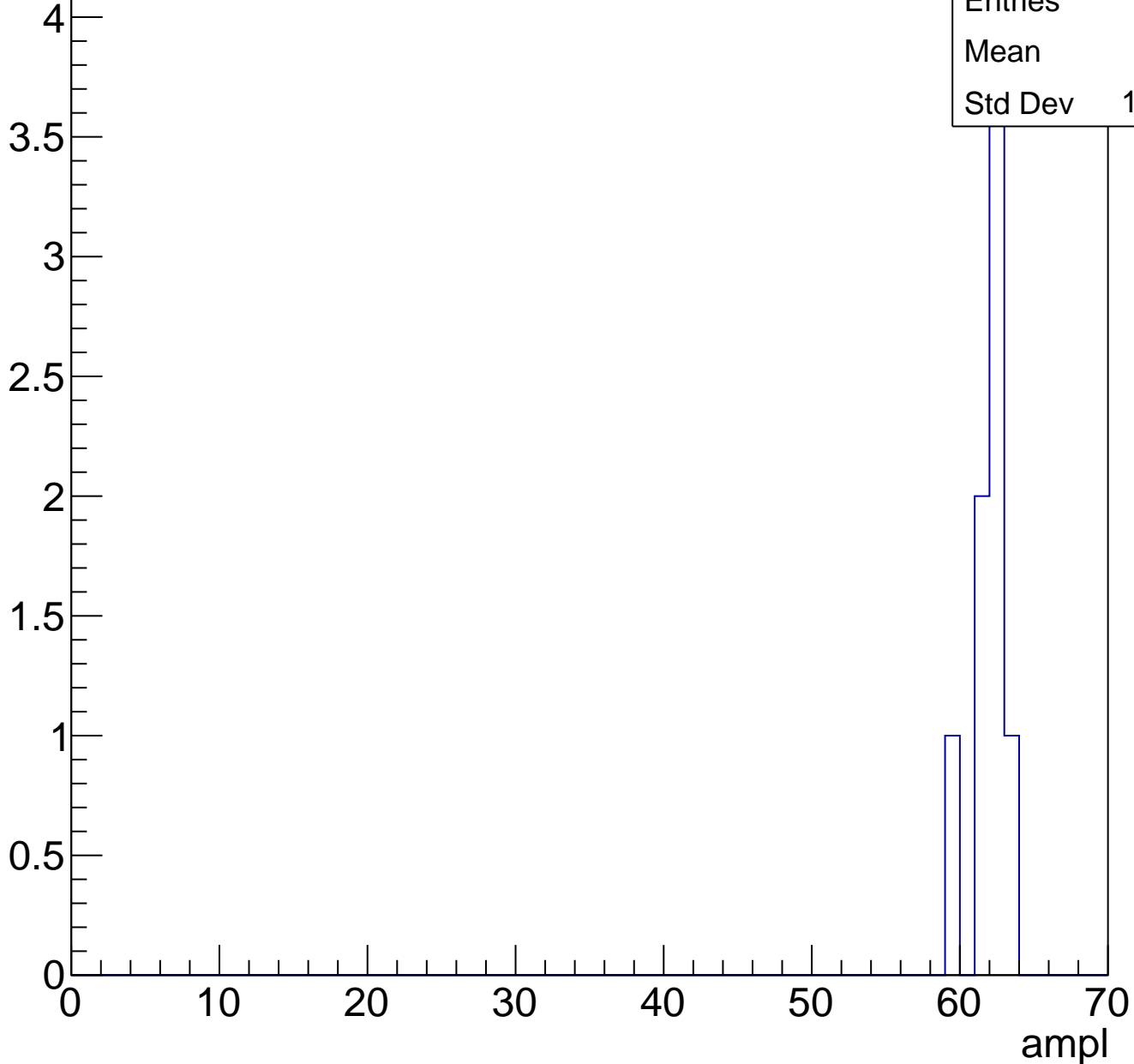
Entries	46
Mean	58.26
Std Dev	9.15



# B1L100S, U6-ch124, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

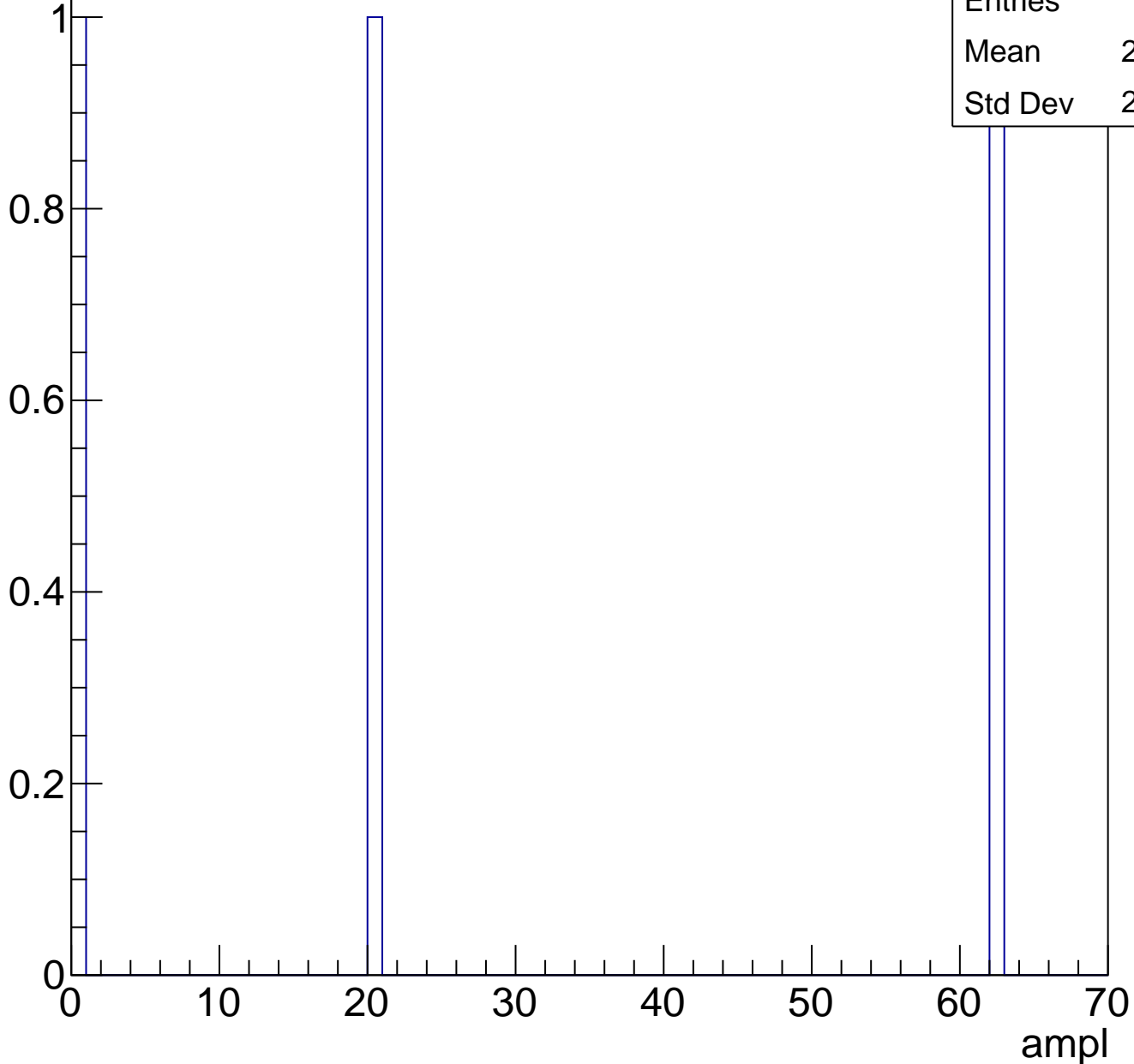




# B1L100S, U6-ch124, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	3
Mean	27.33
Std Dev	25.84

# B1L100S, U6-ch125, adc0

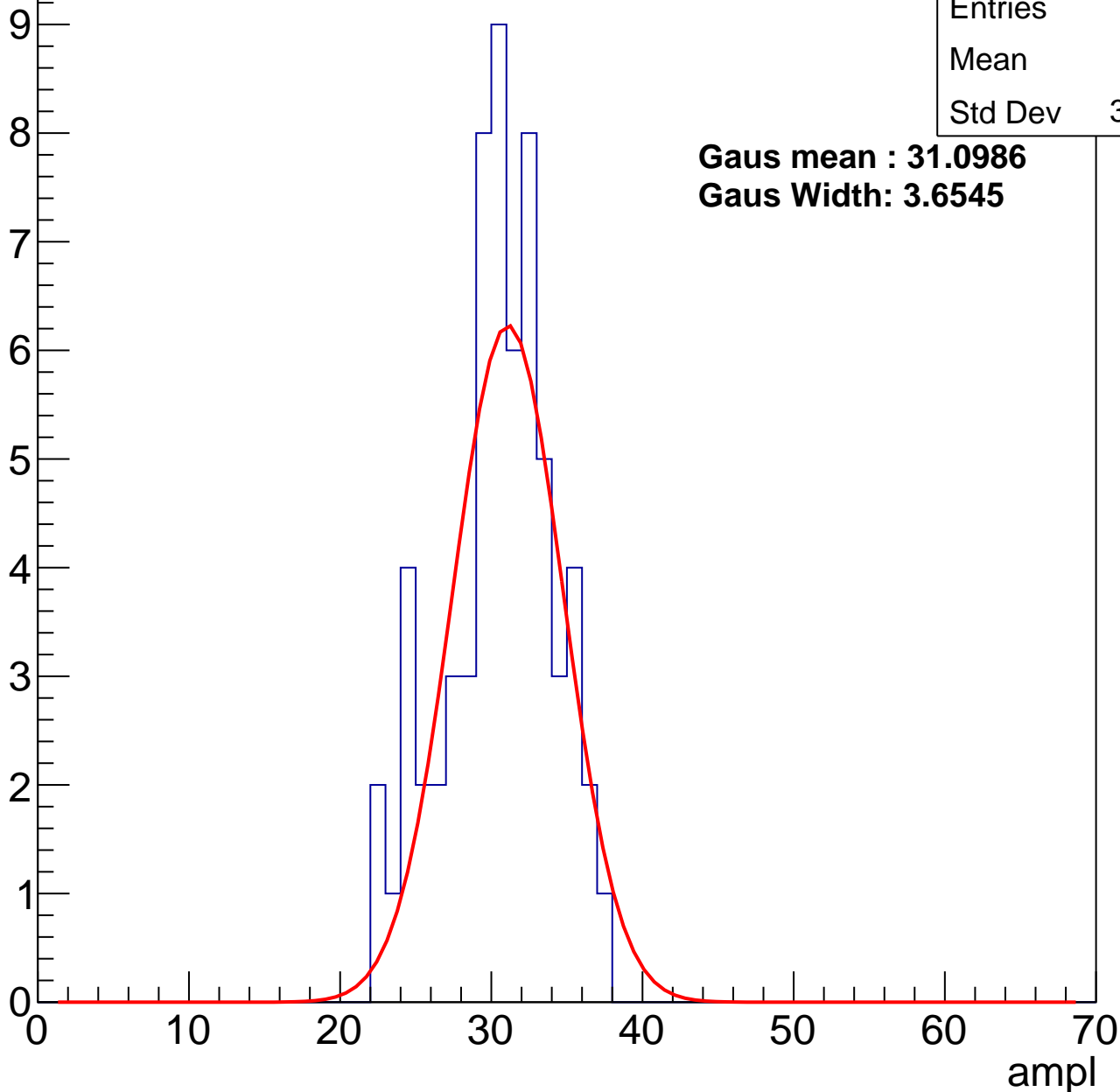
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	63
Mean	30
Std Dev	3.568

**Gaus mean : 31.0986**

**Gaus Width: 3.6545**



# B1L100S, U6-ch125, adc1

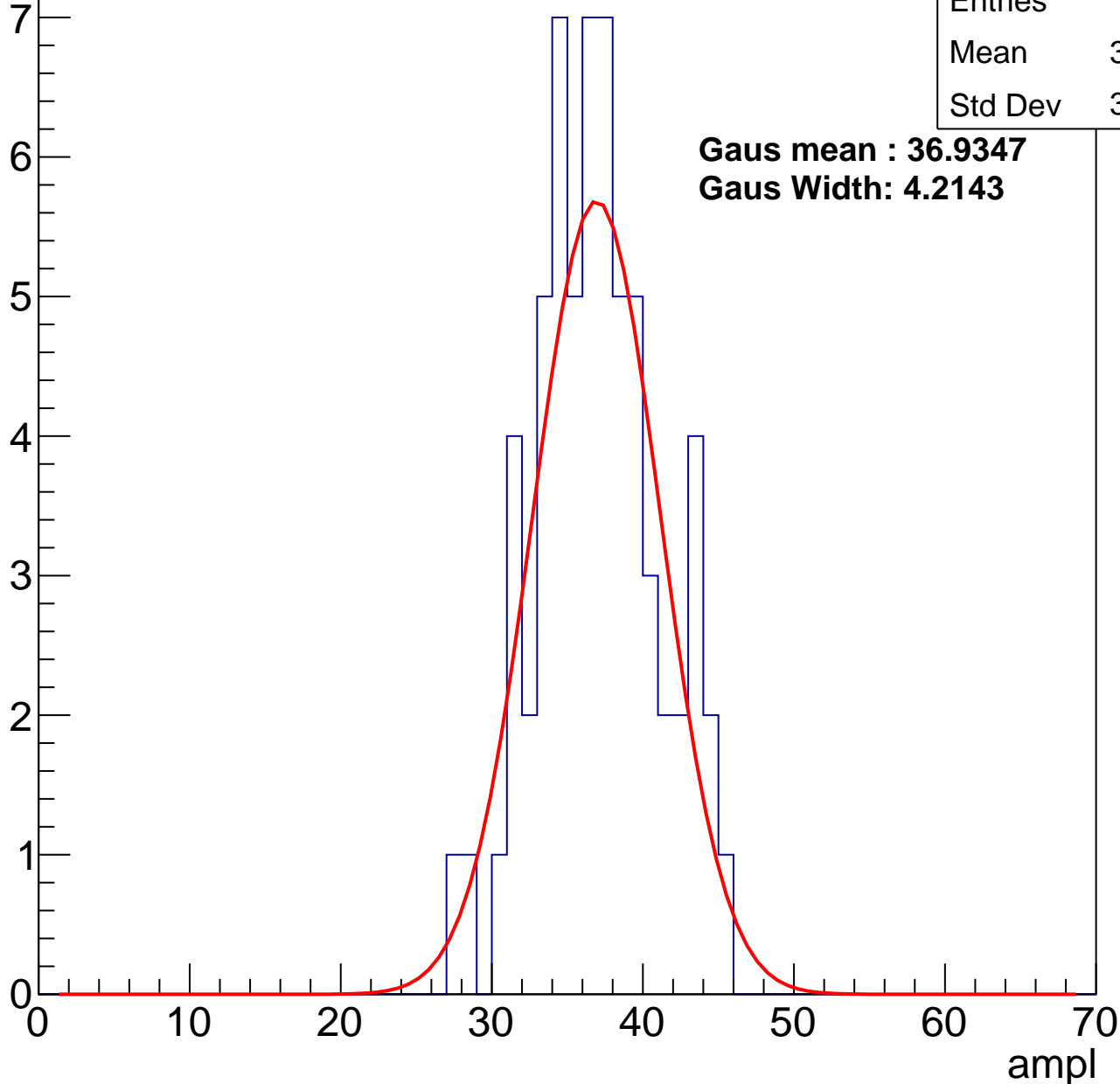
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	64
Mean	36.53
Std Dev	3.992

**Gaus mean : 36.9347**

**Gaus Width: 4.2143**



# B1L100S, U6-ch125, adc2

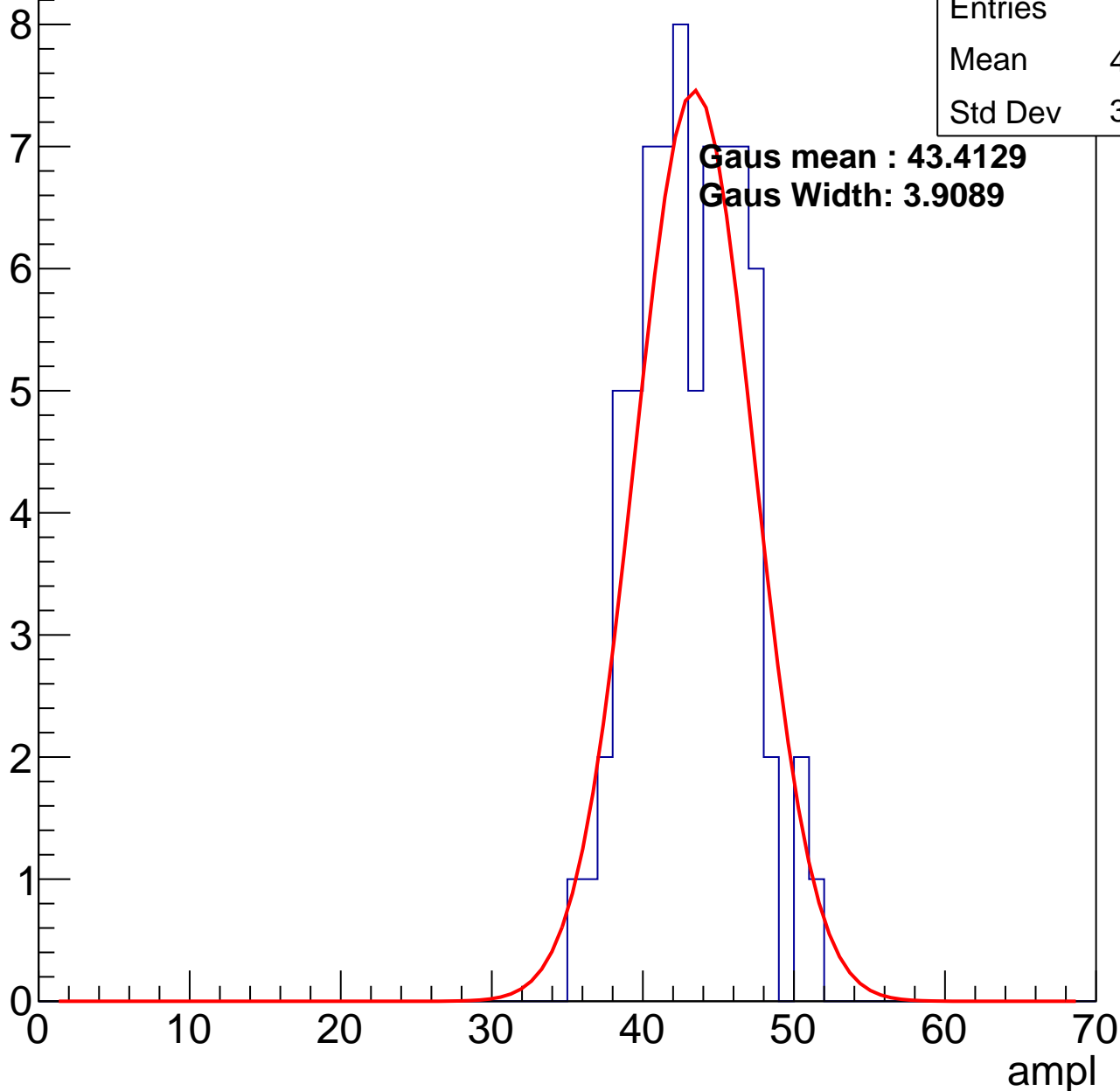
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	73
Mean	42.77
Std Dev	3.494

**Gaus mean : 43.4129**

**Gaus Width: 3.9089**

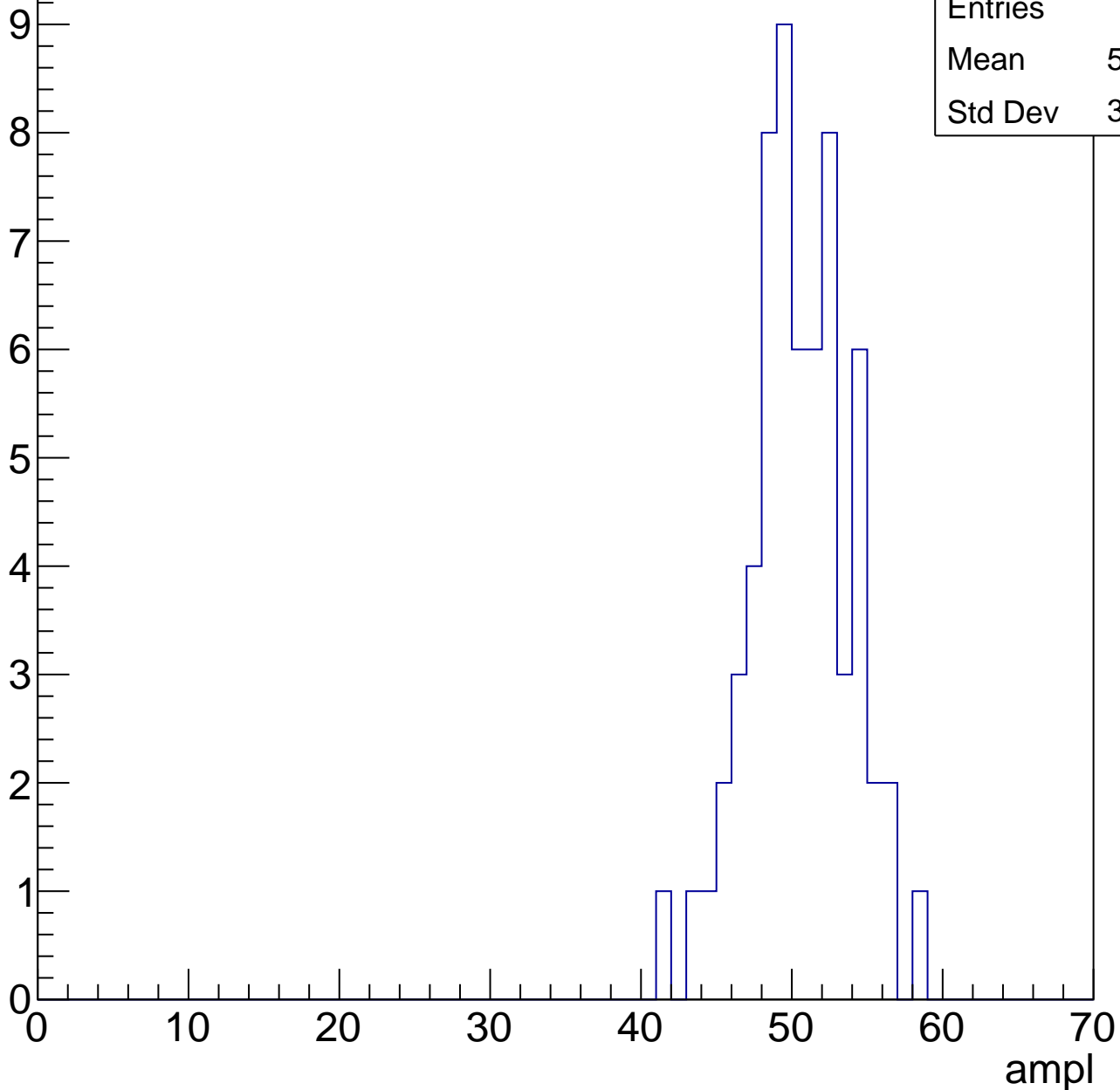


# B1L100S, U6-ch125, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

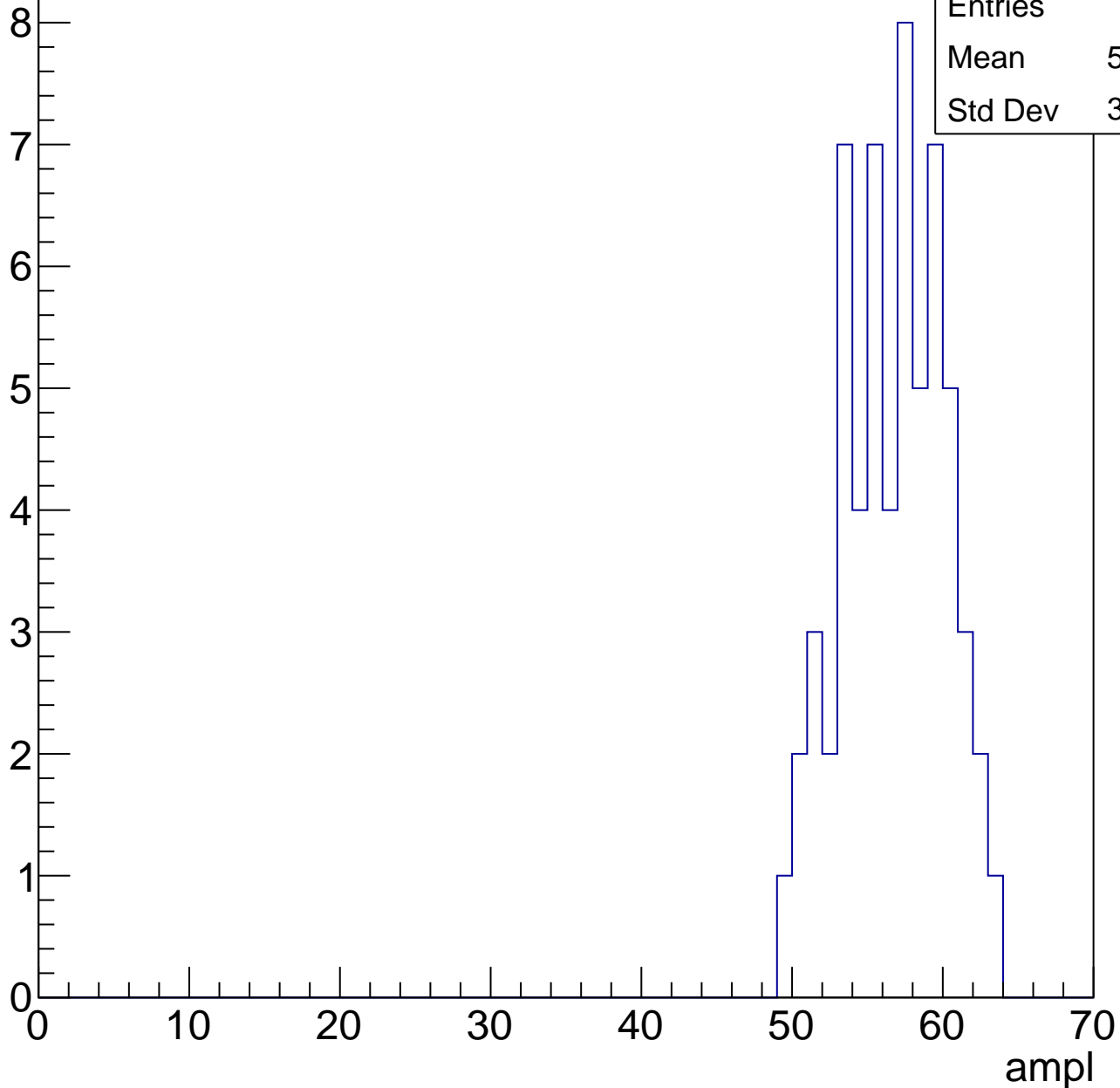
Entries	63
Mean	50.06
Std Dev	3.304



# B1L100S, U6-ch125, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



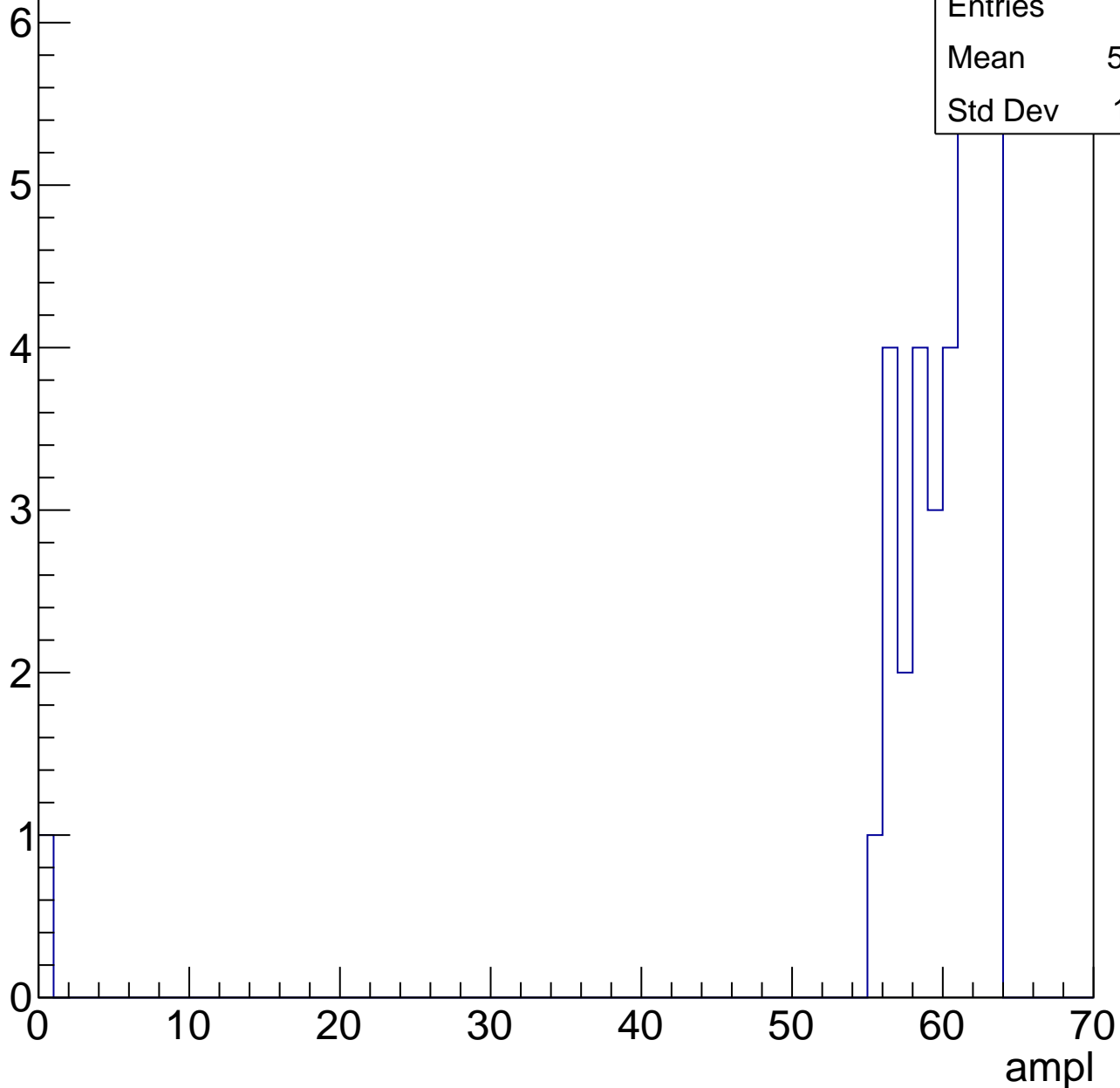
Entries	61
Mean	56.25
Std Dev	3.332

# B1L100S, U6-ch125, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	37
Mean	58.32
Std Dev	10.01



# B1L100S, U6-ch125, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry





# B1L100S, U6-ch125, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



# B1L100S, U6-ch126, adc0

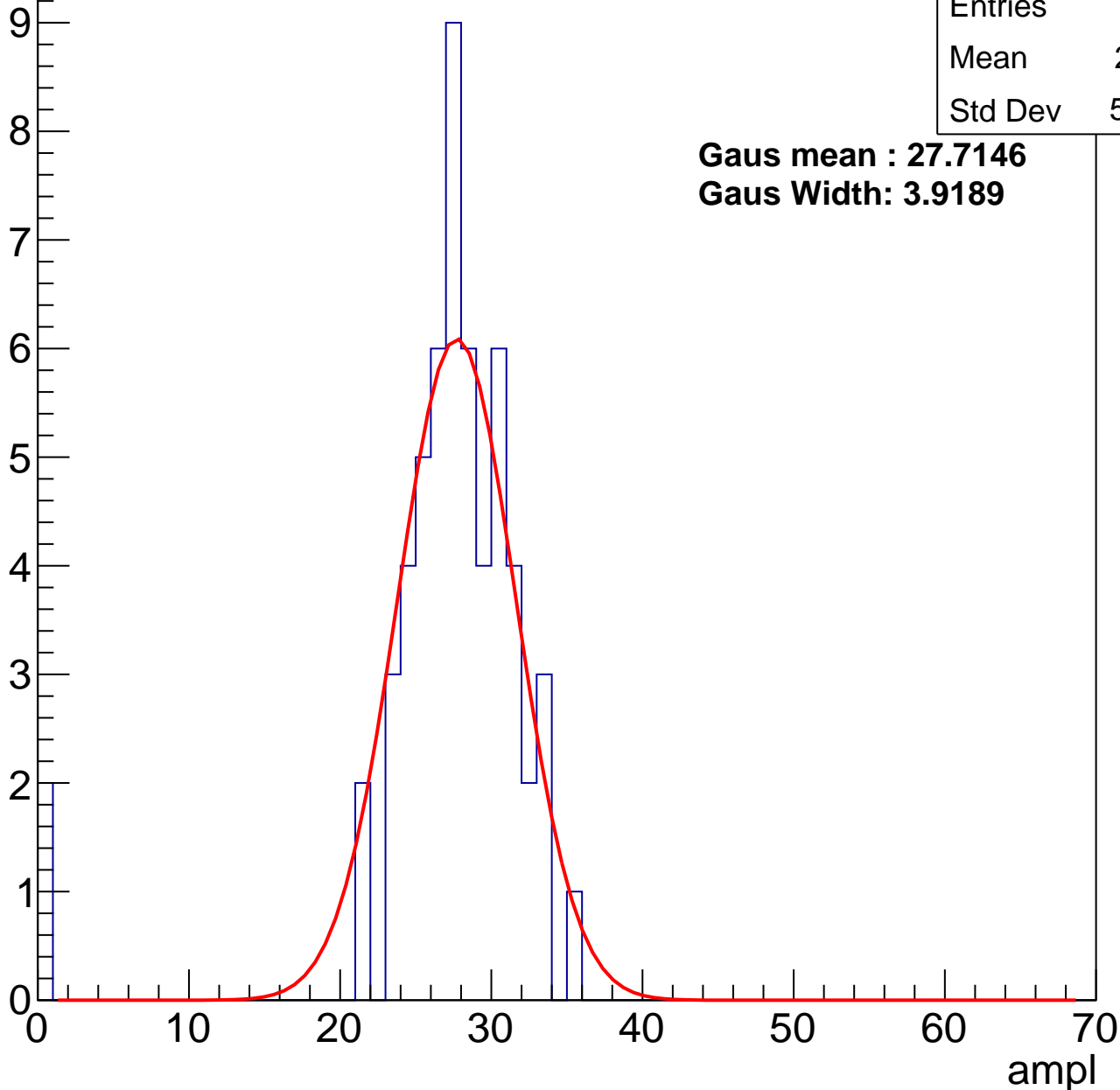
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	57
Mean	26.61
Std Dev	5.914

**Gaus mean : 27.7146**

**Gaus Width: 3.9189**



# B1L100S, U6-ch126, adc1

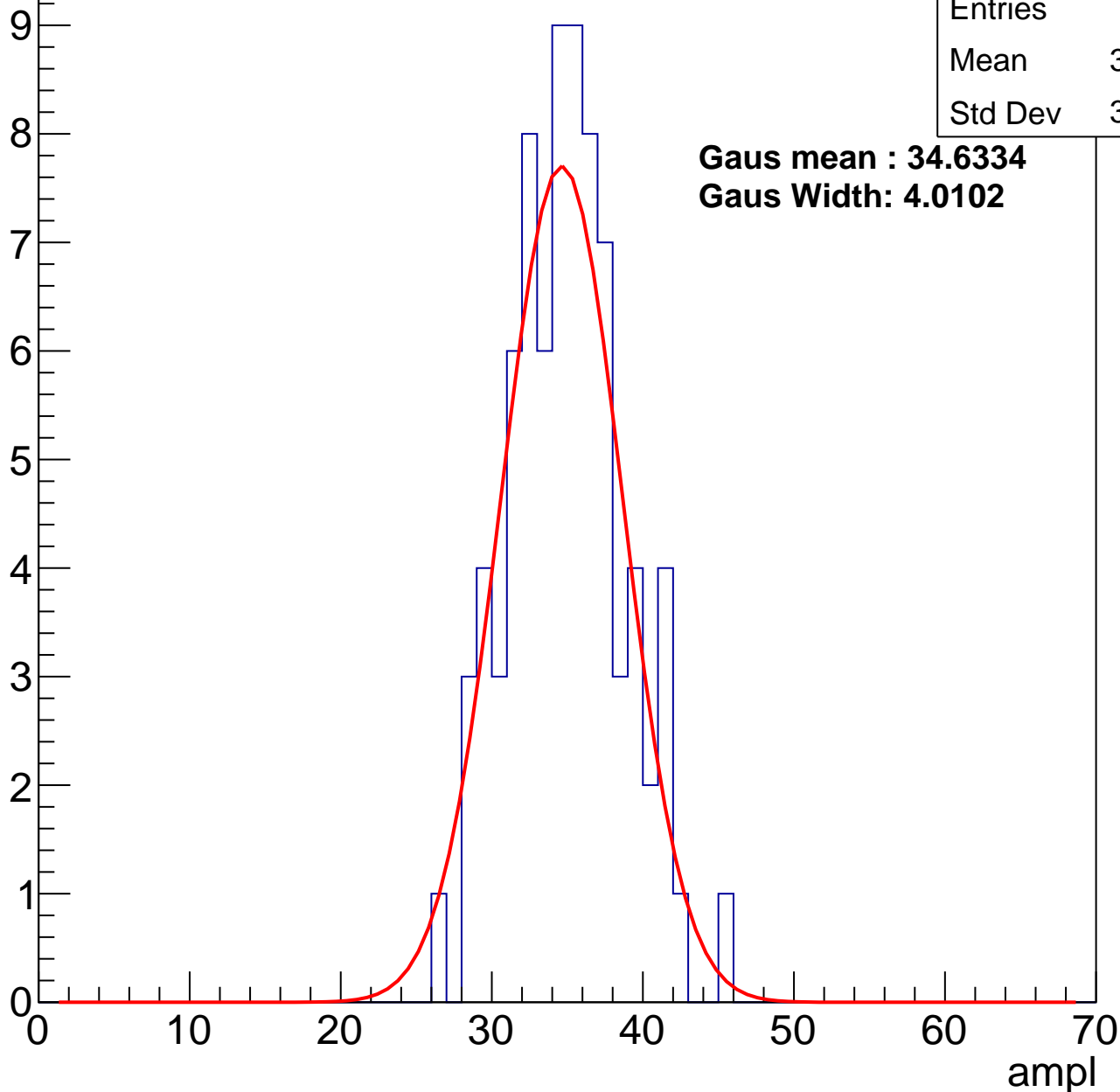
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	79
Mean	34.49
Std Dev	3.728

**Gaus mean : 34.6334**

**Gaus Width: 4.0102**



# B1L100S, U6-ch126, adc2

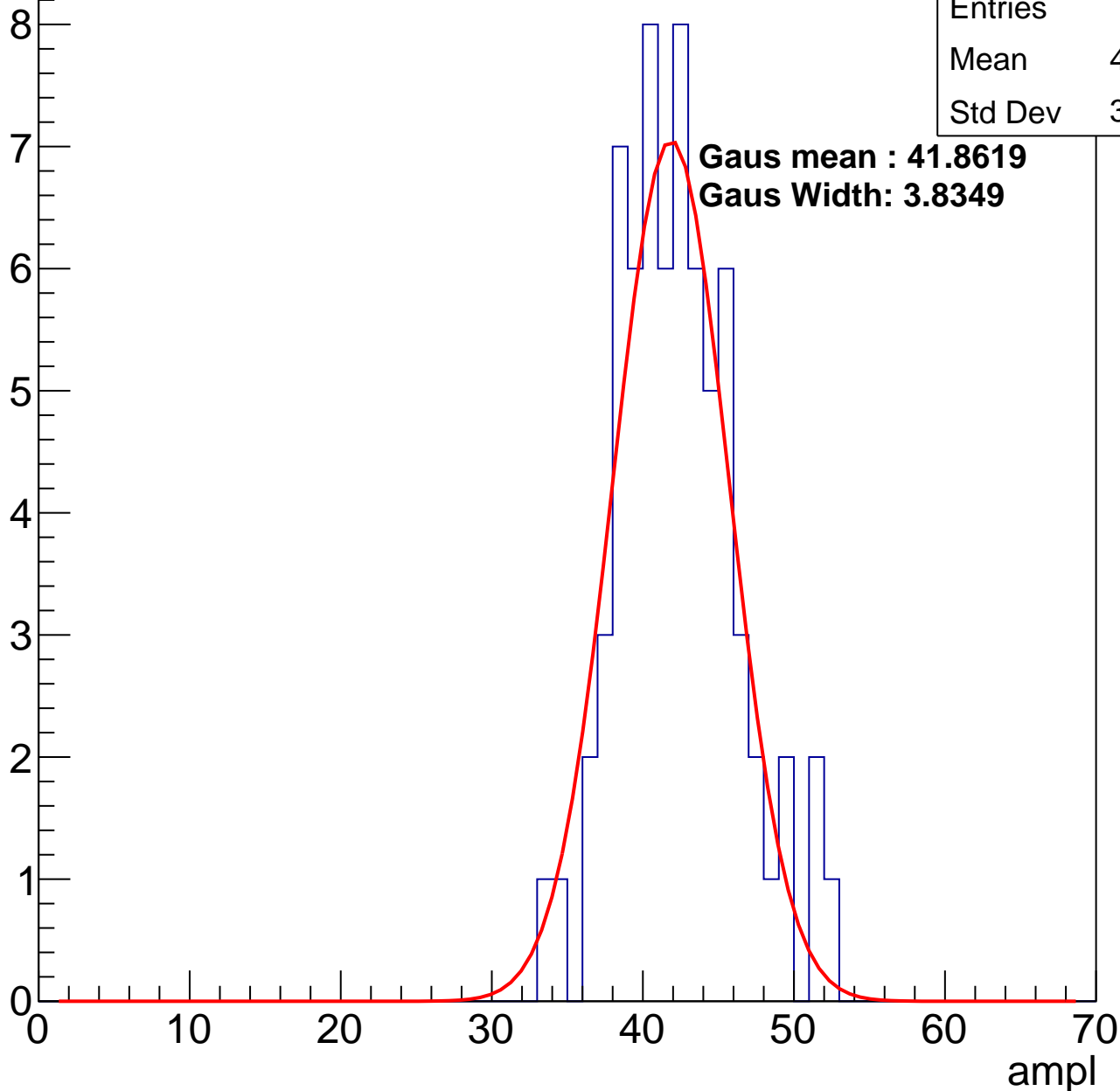
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	70
Mean	41.89
Std Dev	3.908

**Gaus mean : 41.8619**

**Gaus Width: 3.8349**

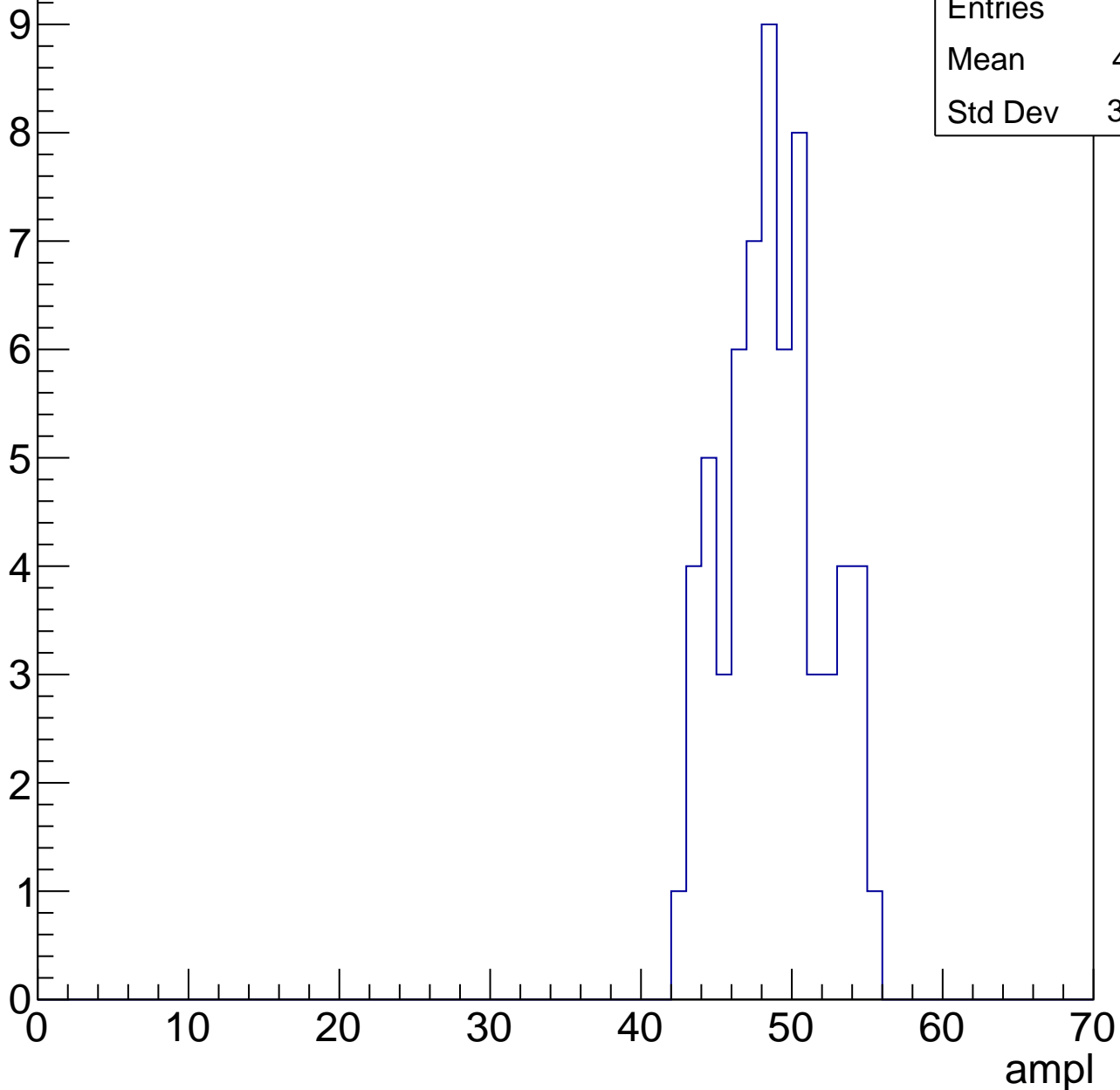


# B1L100S, U6-ch126, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	64
Mean	48.31
Std Dev	3.245



# B1L100S, U6-ch126, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	61
Mean	54.56
Std Dev	3.262

ampl

0 10 20 30 40 50 60 70

1

2

3

4

5

6

7

8

# B1L100S, U6-ch126, adc5

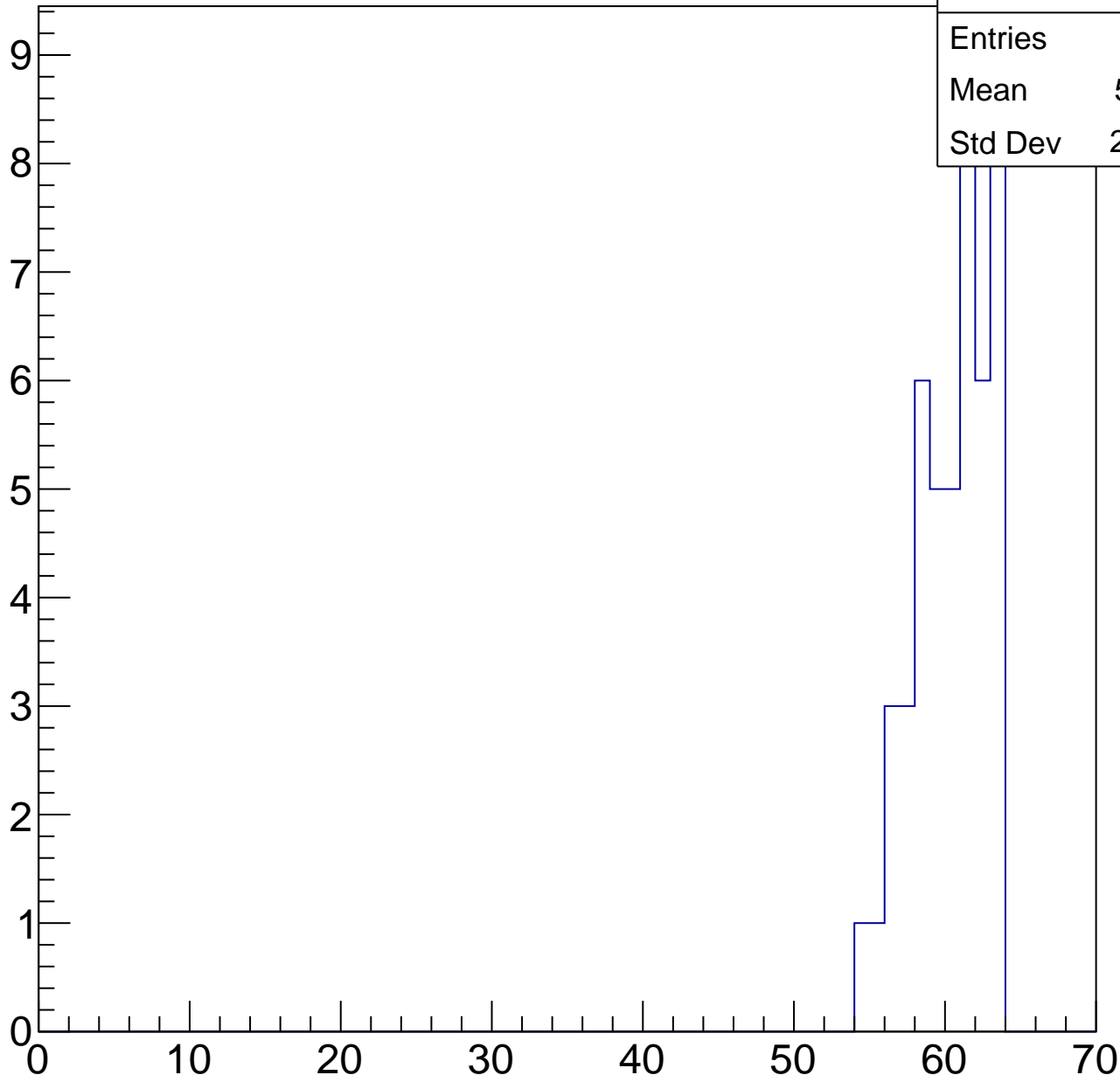
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	47
Mean	59.91
Std Dev	2.395

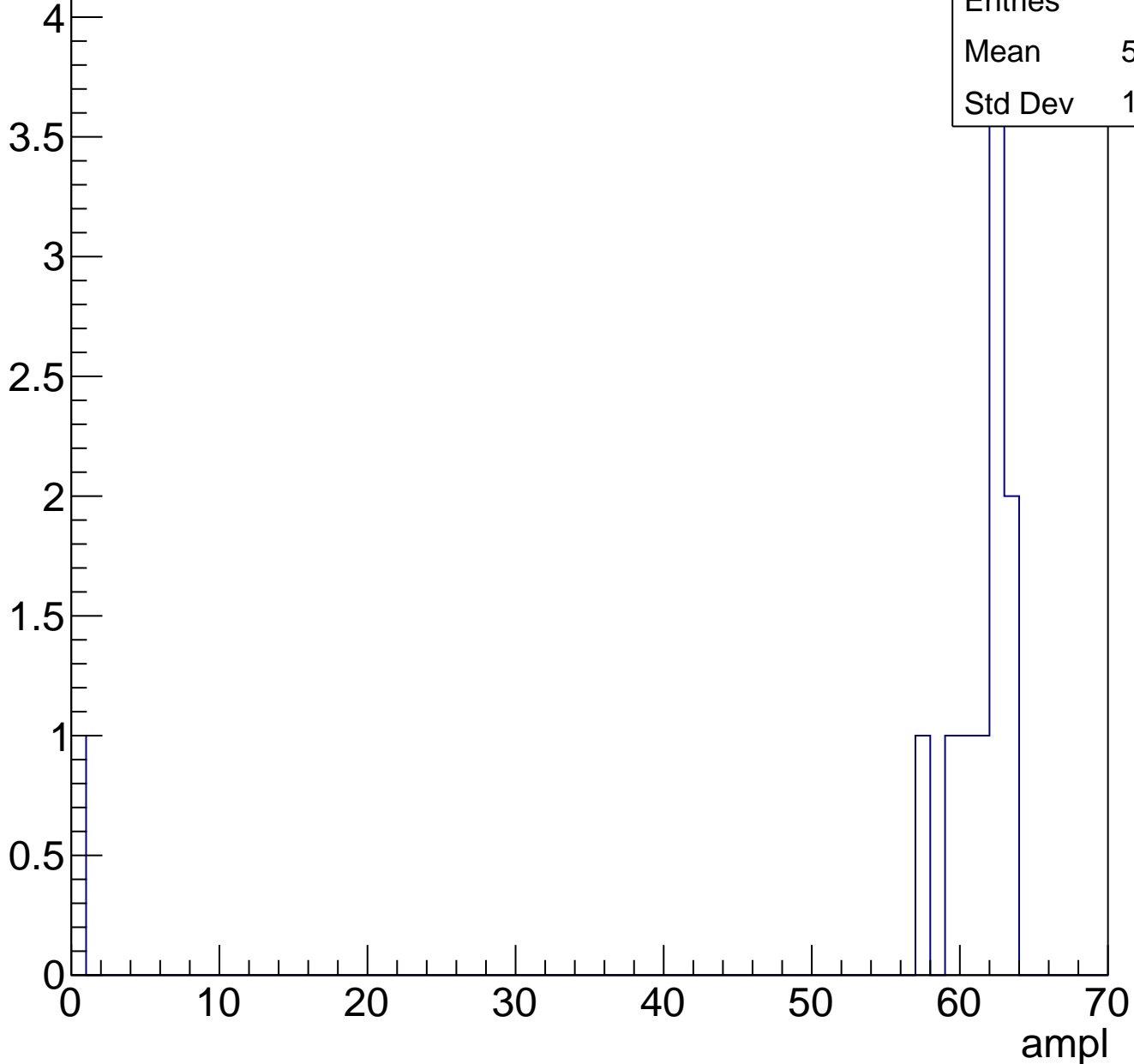
ampl



# B1L100S, U6-ch126, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	11
Mean	55.55
Std Dev	17.65



# B1L100S, U6-ch126, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L100S, U6-ch127, adc0

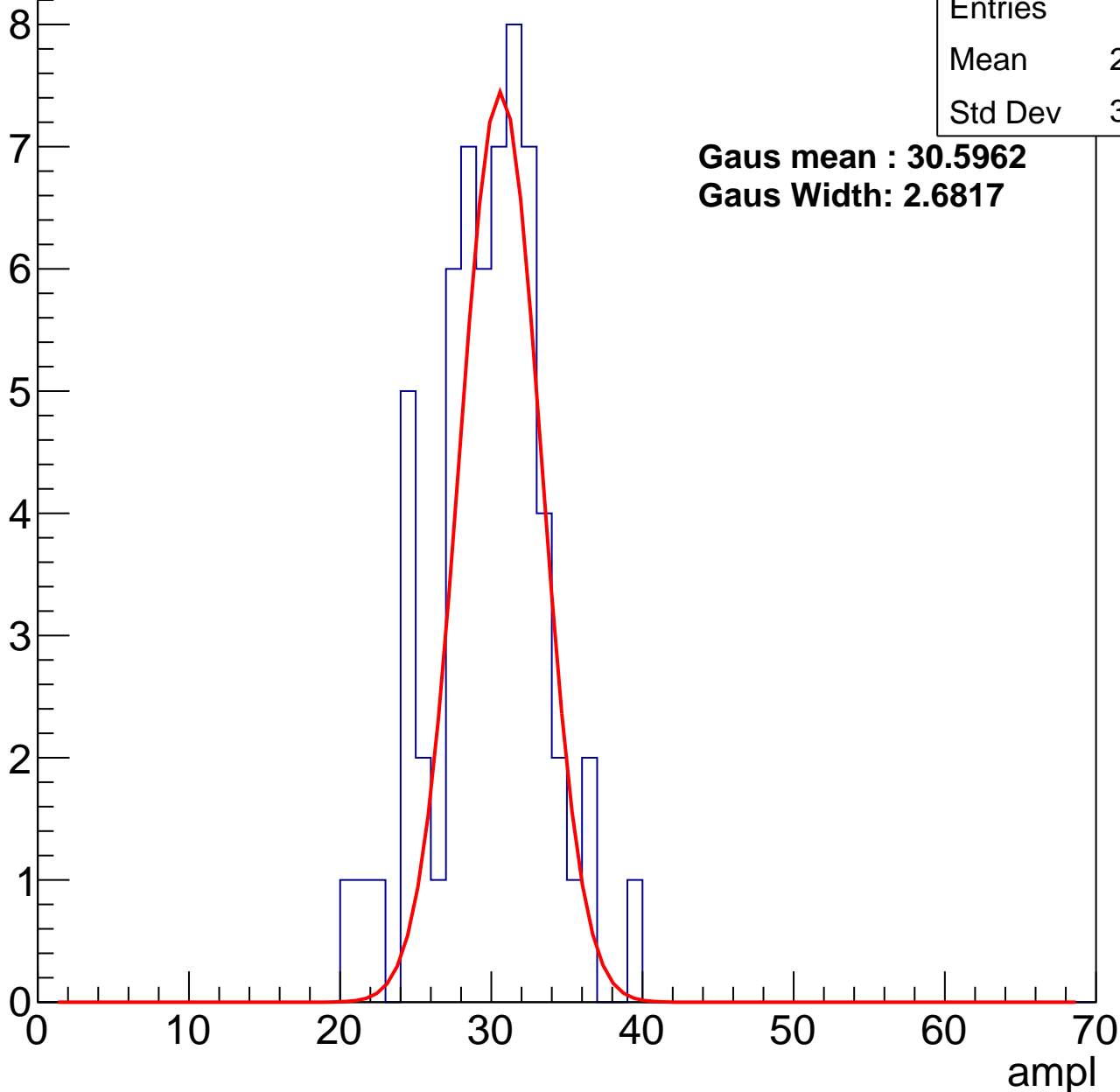
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	62
Mean	29.34
Std Dev	3.667

**Gaus mean : 30.5962**

**Gaus Width: 2.6817**



# B1L100S, U6-ch127, adc1

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	84
Mean	36.89
Std Dev	4.14

**Gaus mean : 37.0589**

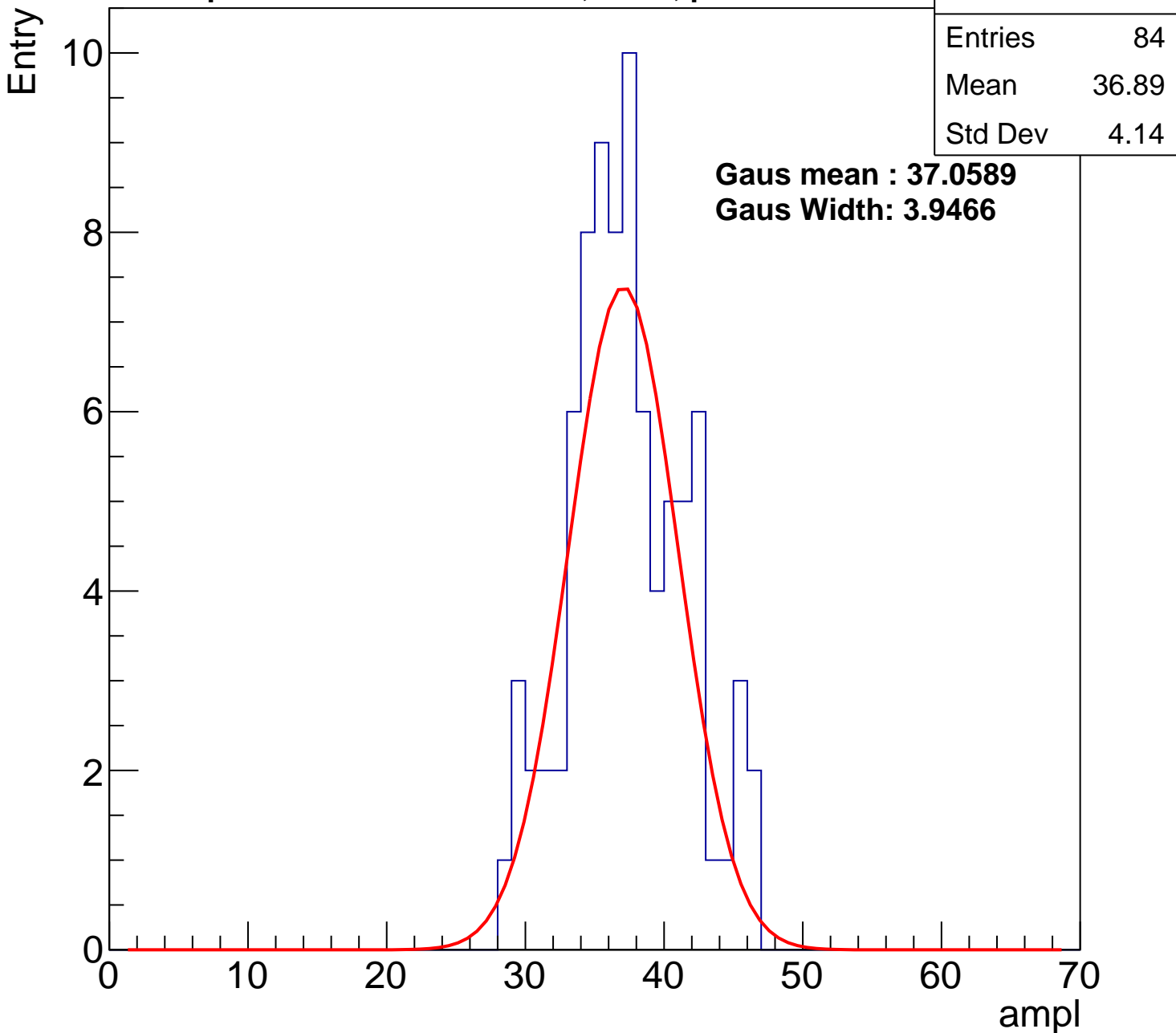
**Gaus Width: 3.9466**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L100S, U6-ch127, adc2

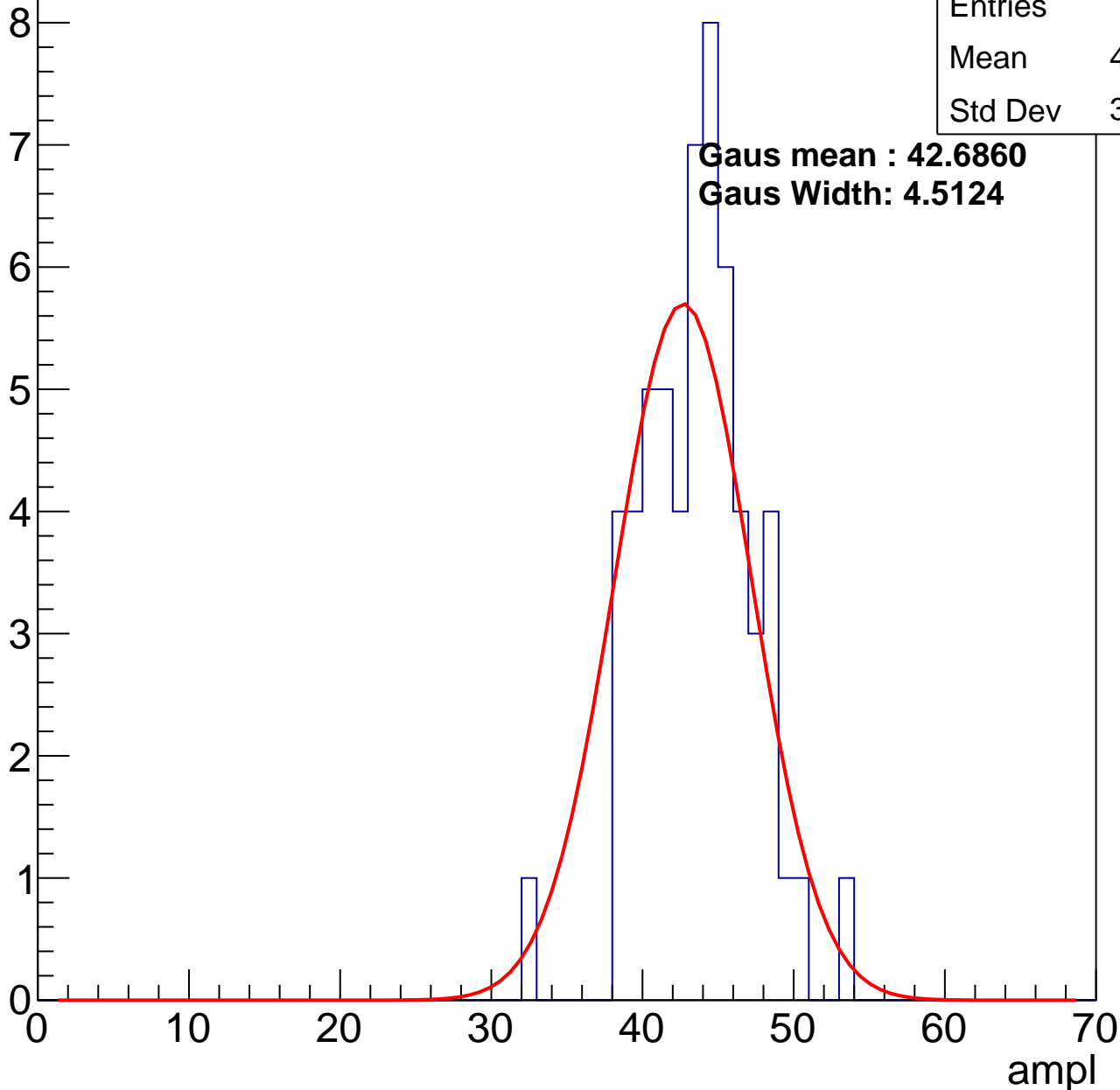
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	58
Mean	43.19
Std Dev	3.603

**Gaus mean : 42.6860**

**Gaus Width: 4.5124**

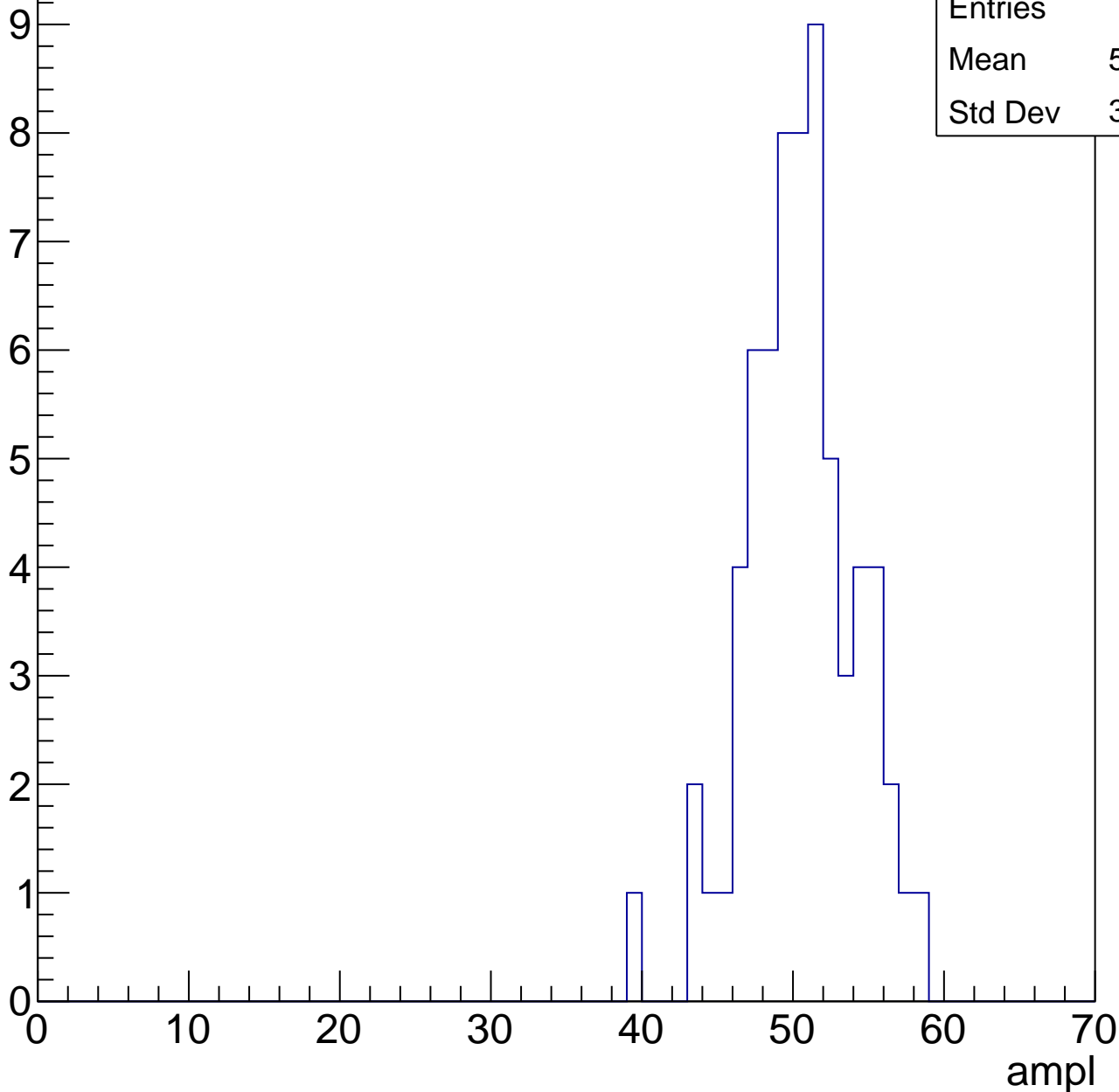


# B1L100S, U6-ch127, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	66
Mean	50.02
Std Dev	3.557

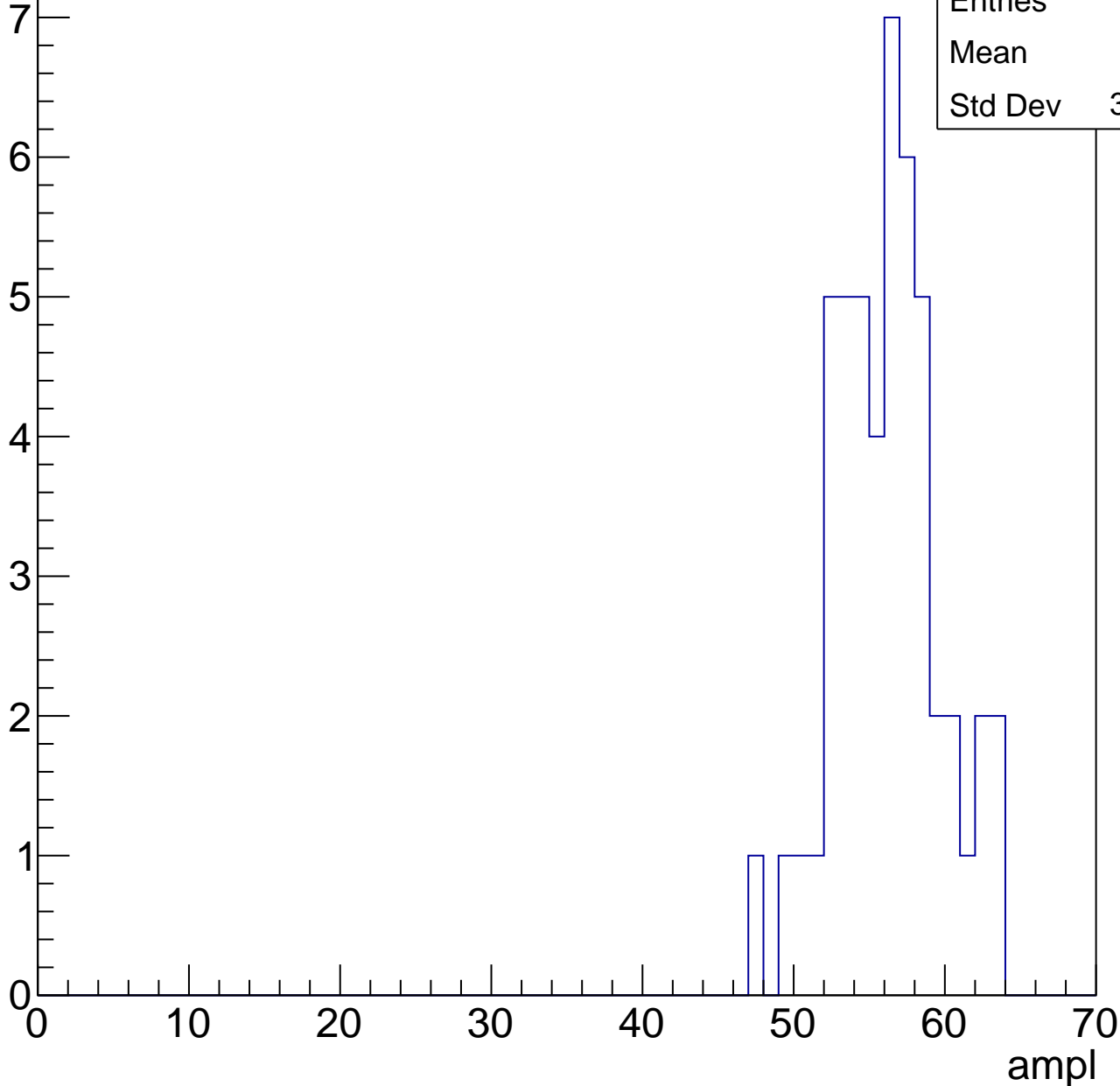


# B1L100S, U6-ch127, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

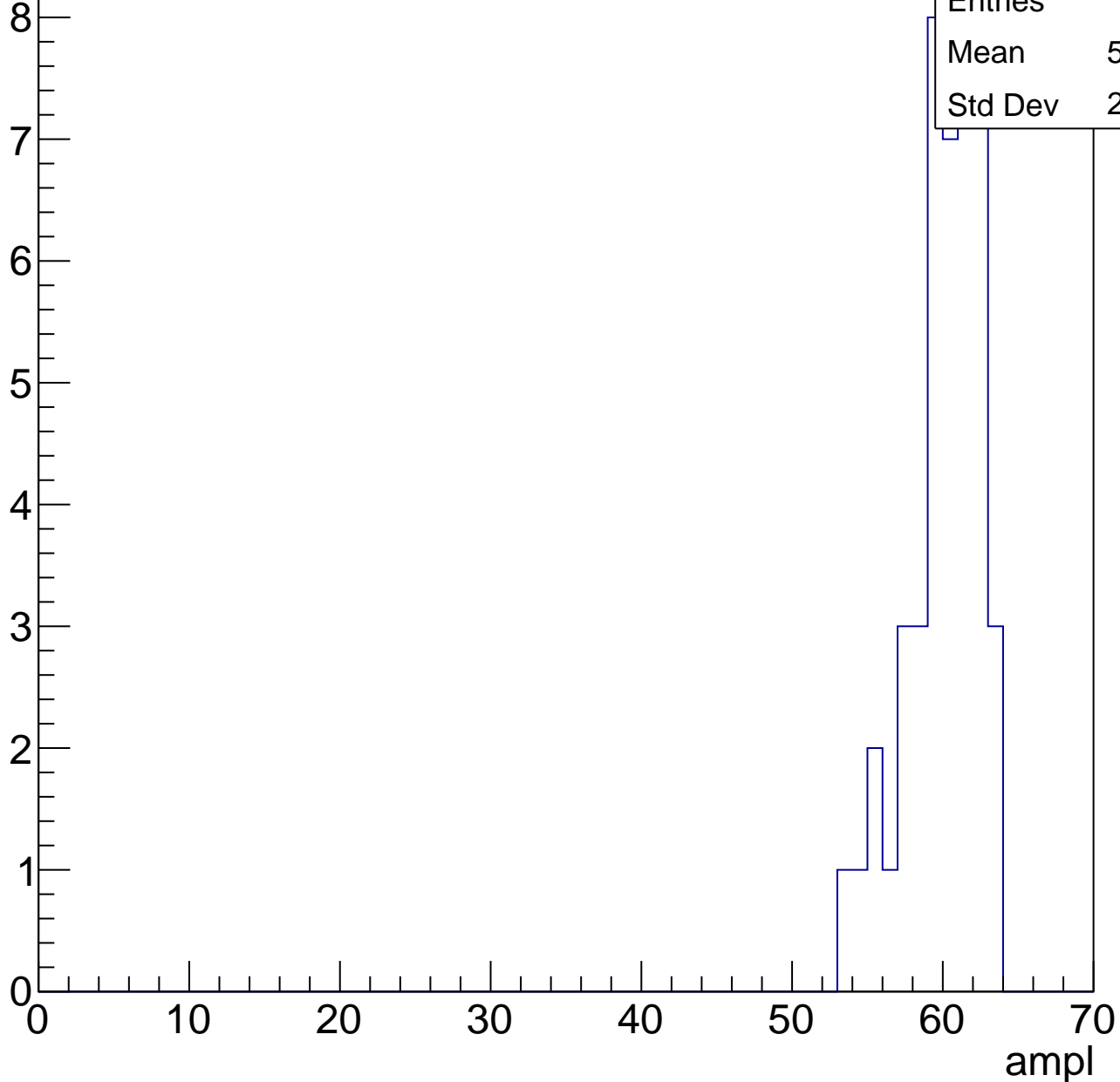
Entries	50
Mean	55.7
Std Dev	3.483



# B1L100S, U6-ch127, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

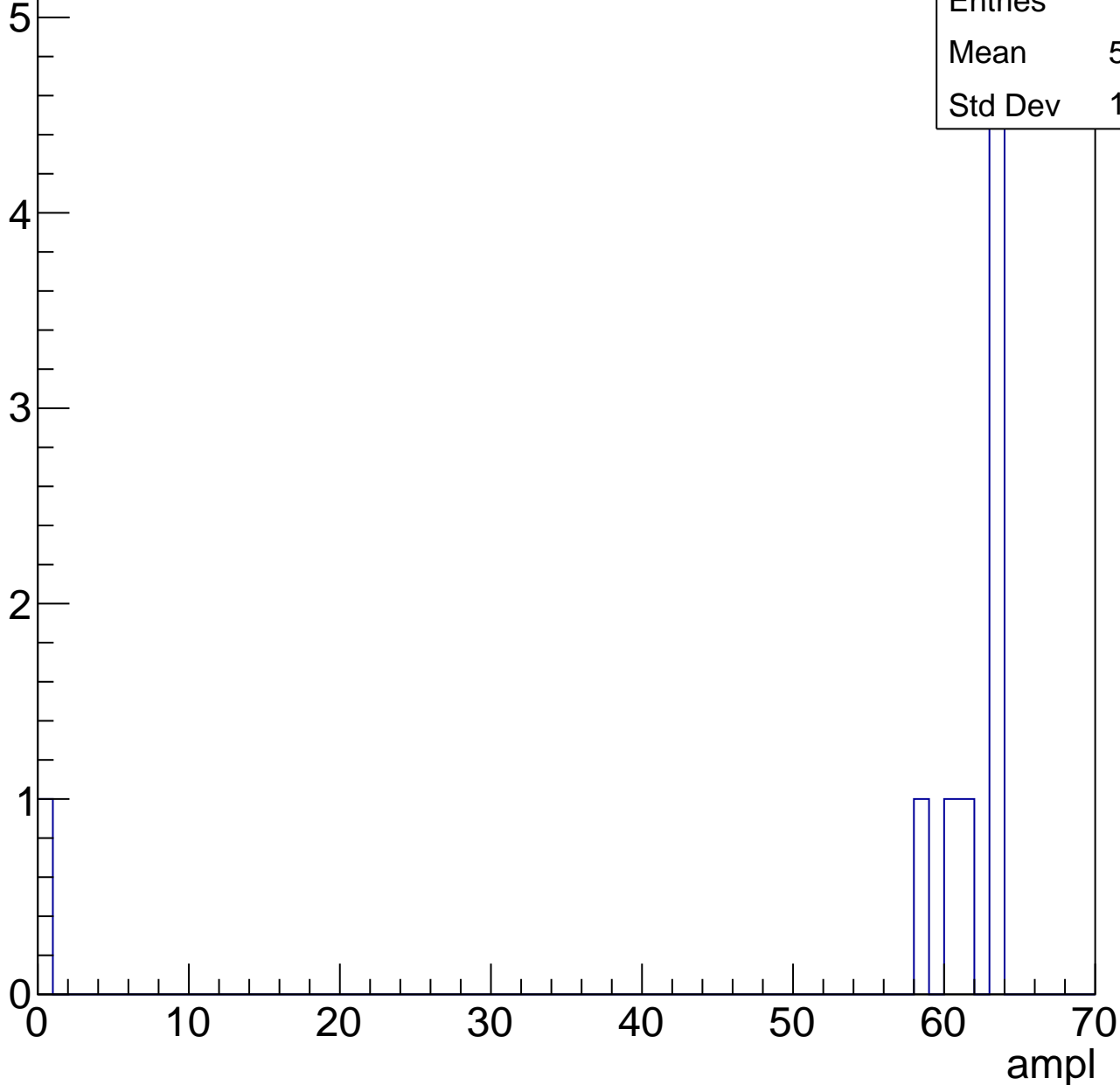


# B1L100S, U6-ch127, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	9
Mean	54.89
Std Dev	19.48





# B1L100S, U6-ch127, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L100S, U6-ch127, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	0
Mean	0
Std Dev	0