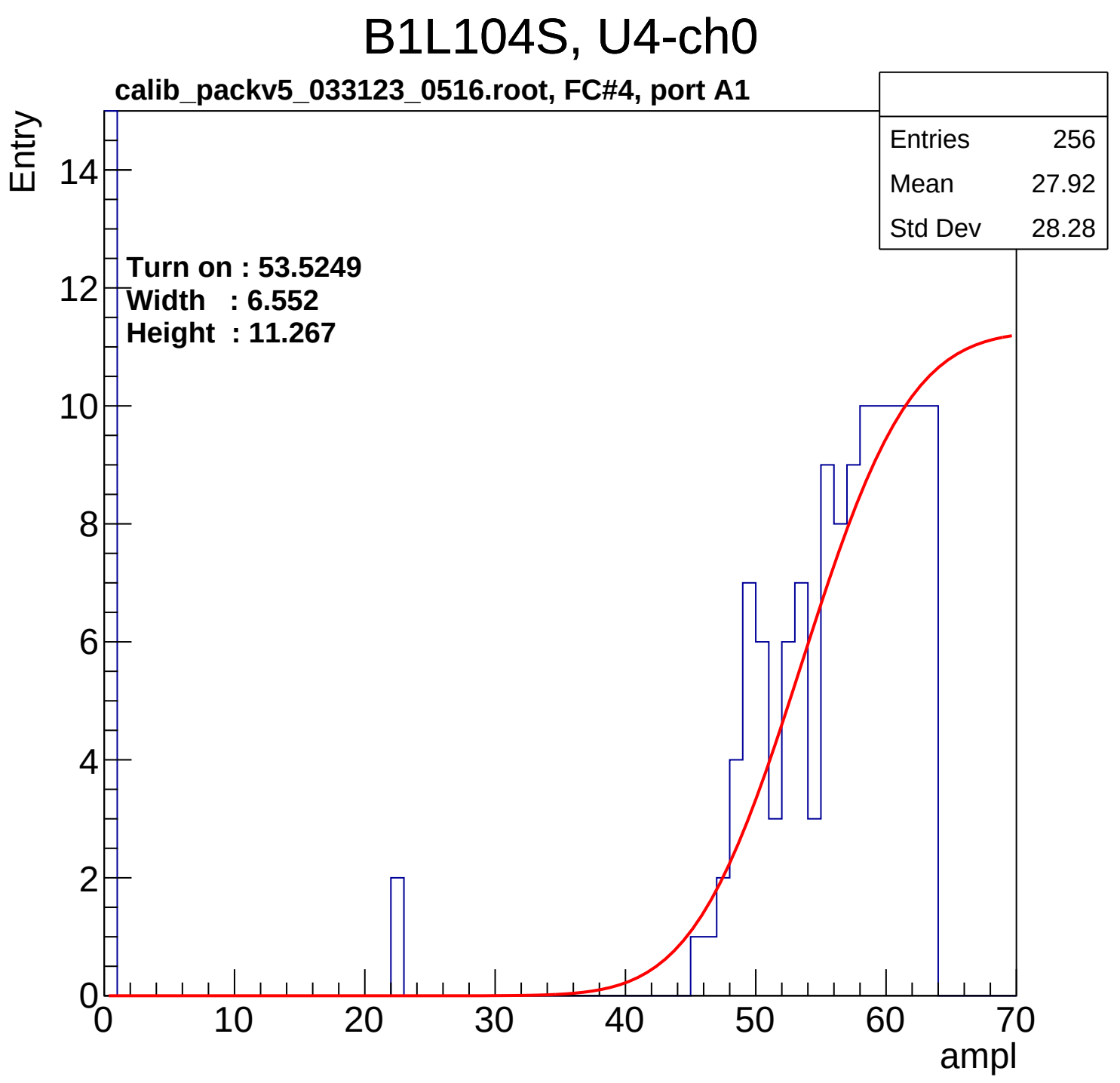
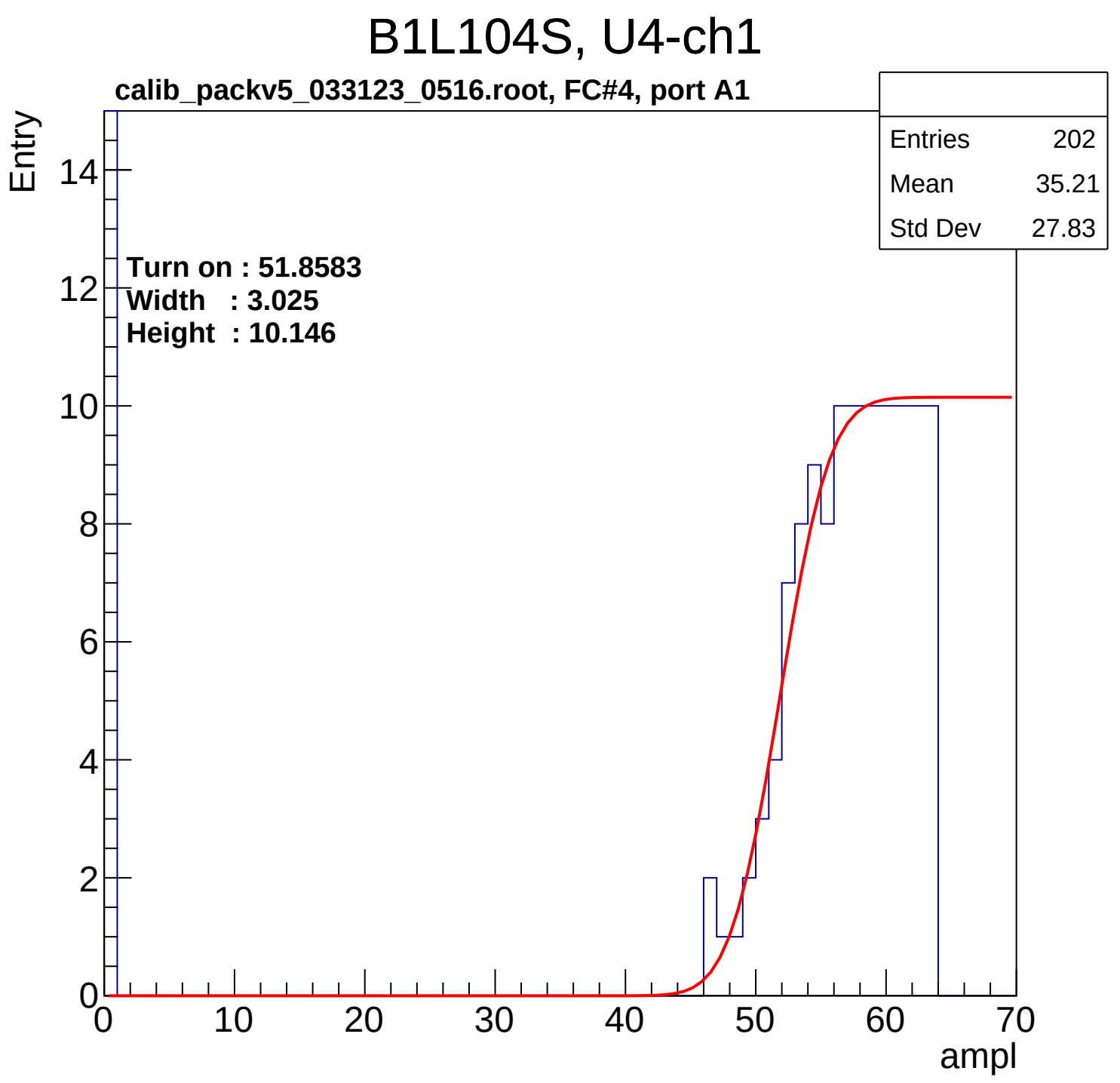
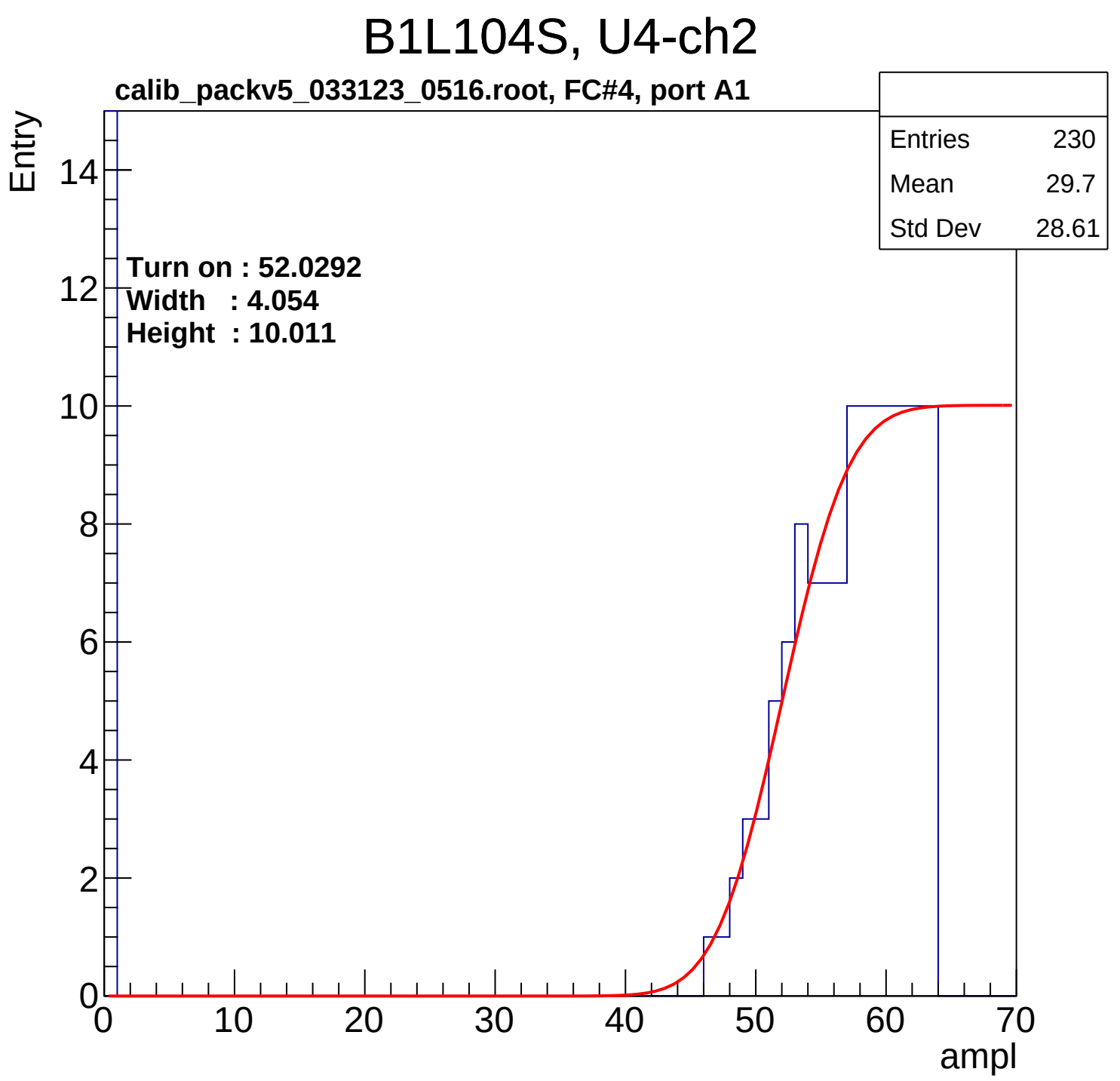
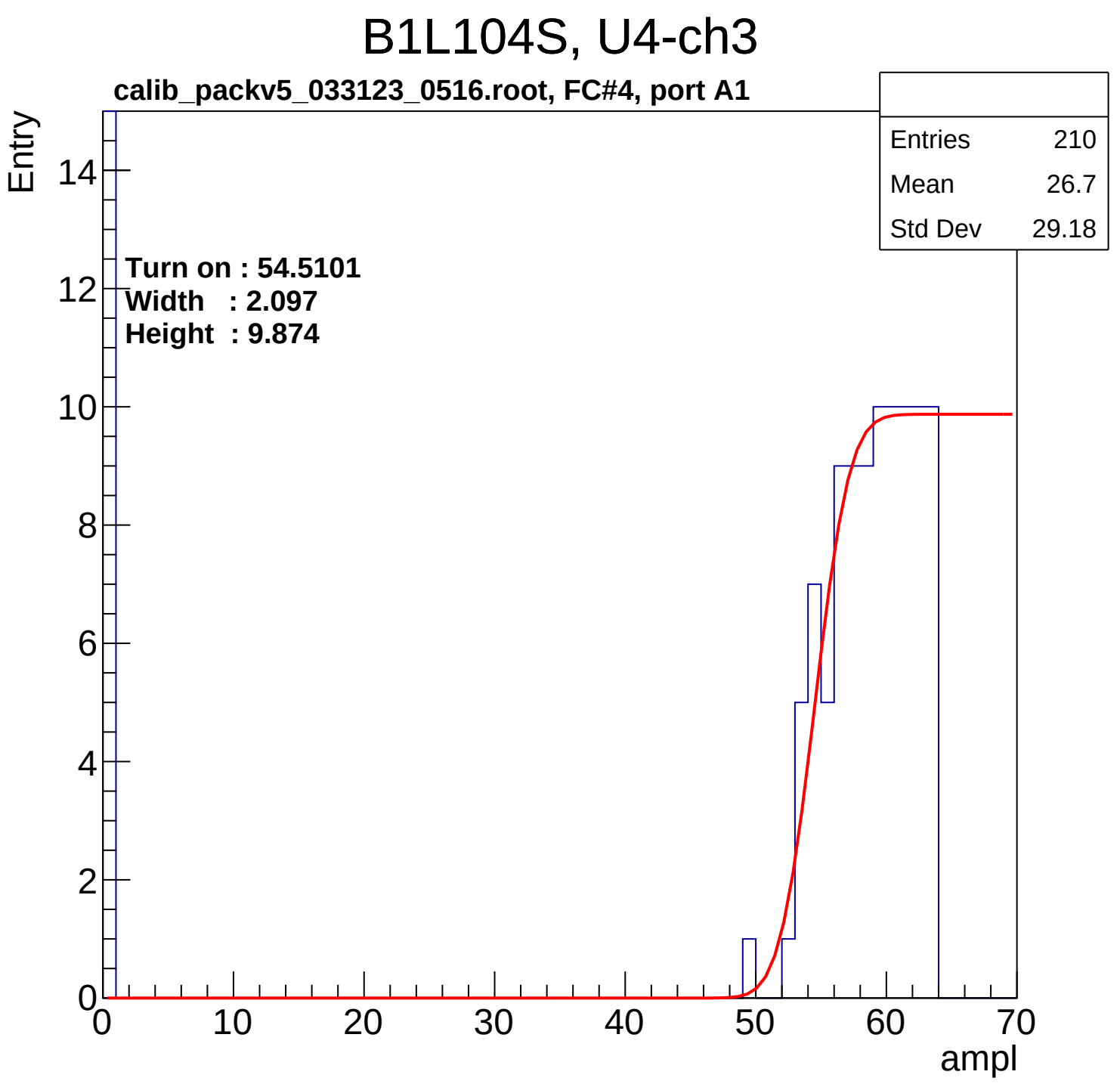
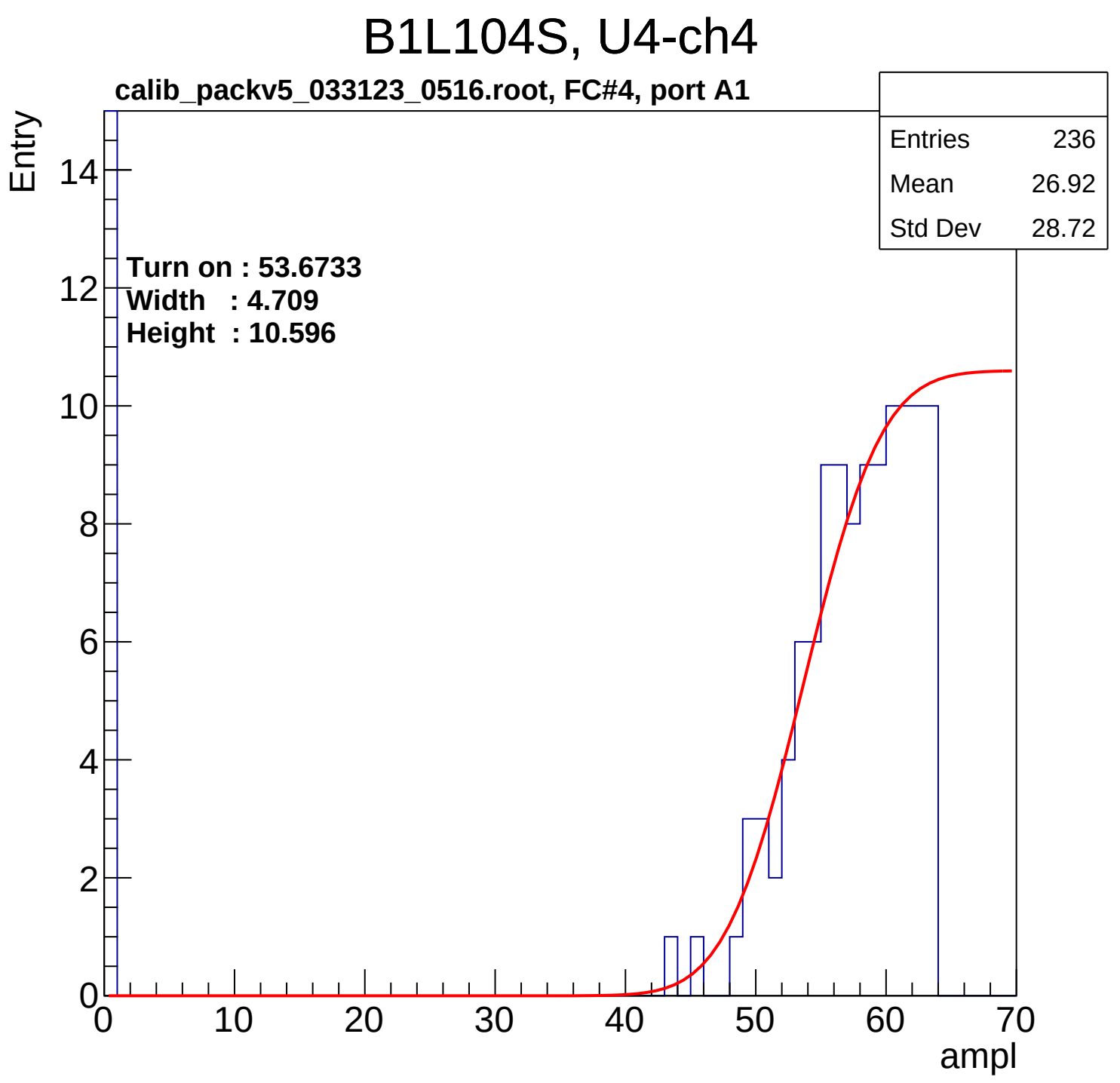
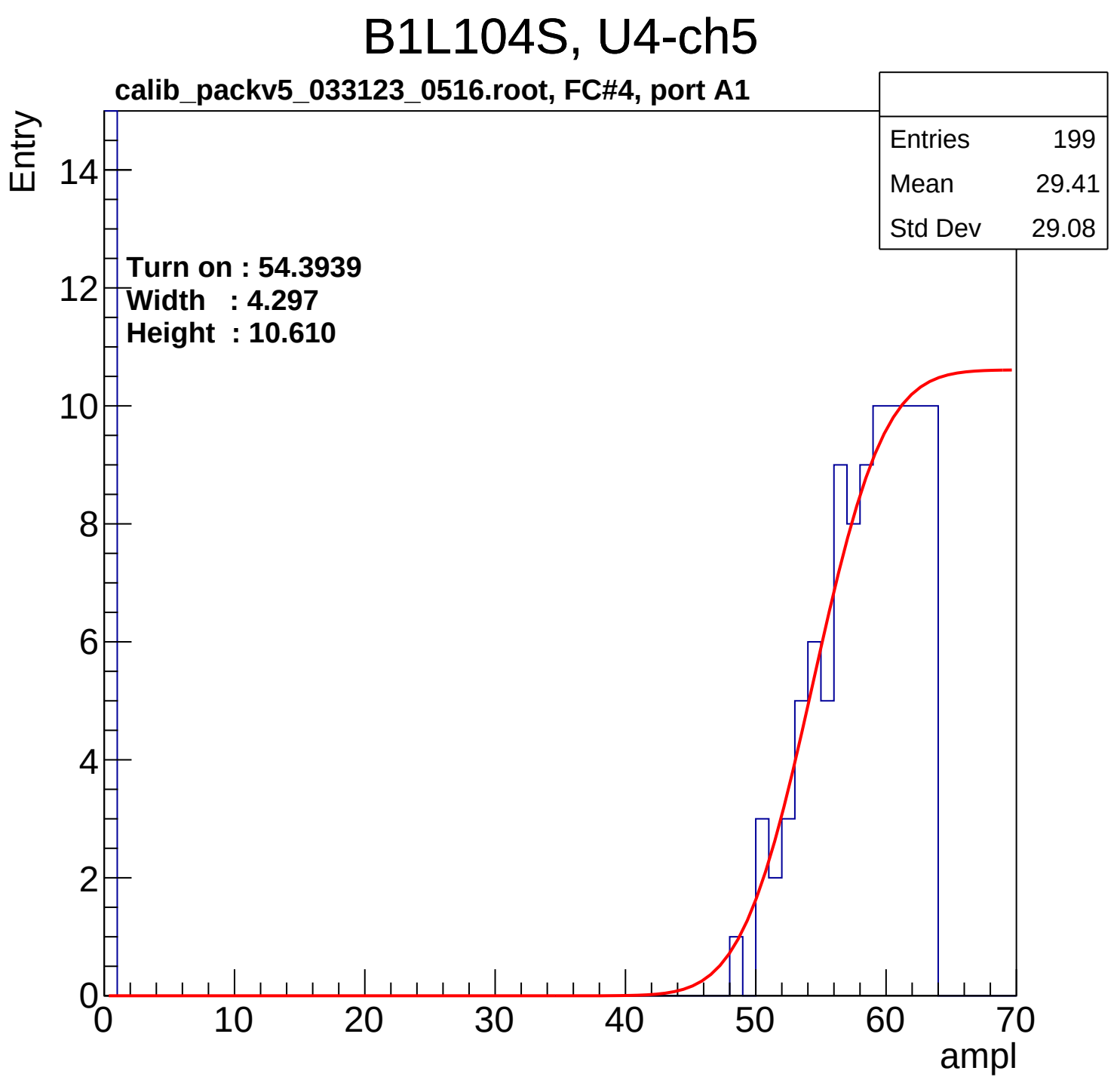

B1L104S, U4-ch0
calib_packv5_033123_0516.root, FC#4, port A1
Entries 256
Mean 27.92
Std Dev 28.28
Turn on : 53.5249
Width : 6.552
Height : 11.267
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

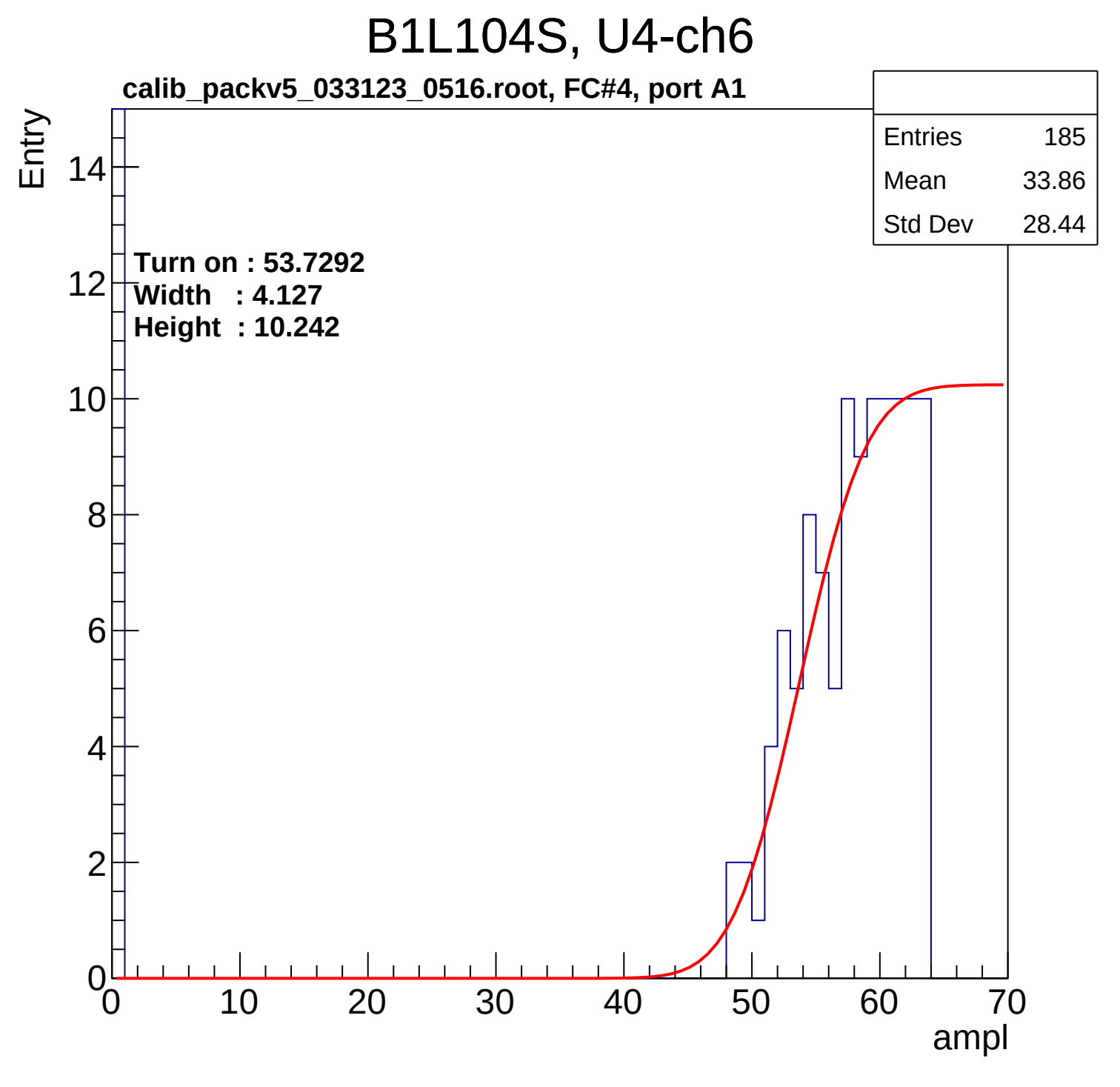

B1L104S, U4-ch1
calib_packv5_033123_0516.root, FC#4, port A1
Entries 202
Mean 35.21
Std Dev 27.83
Turn on : 51.8583
Width : 3.025
Height : 10.146
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

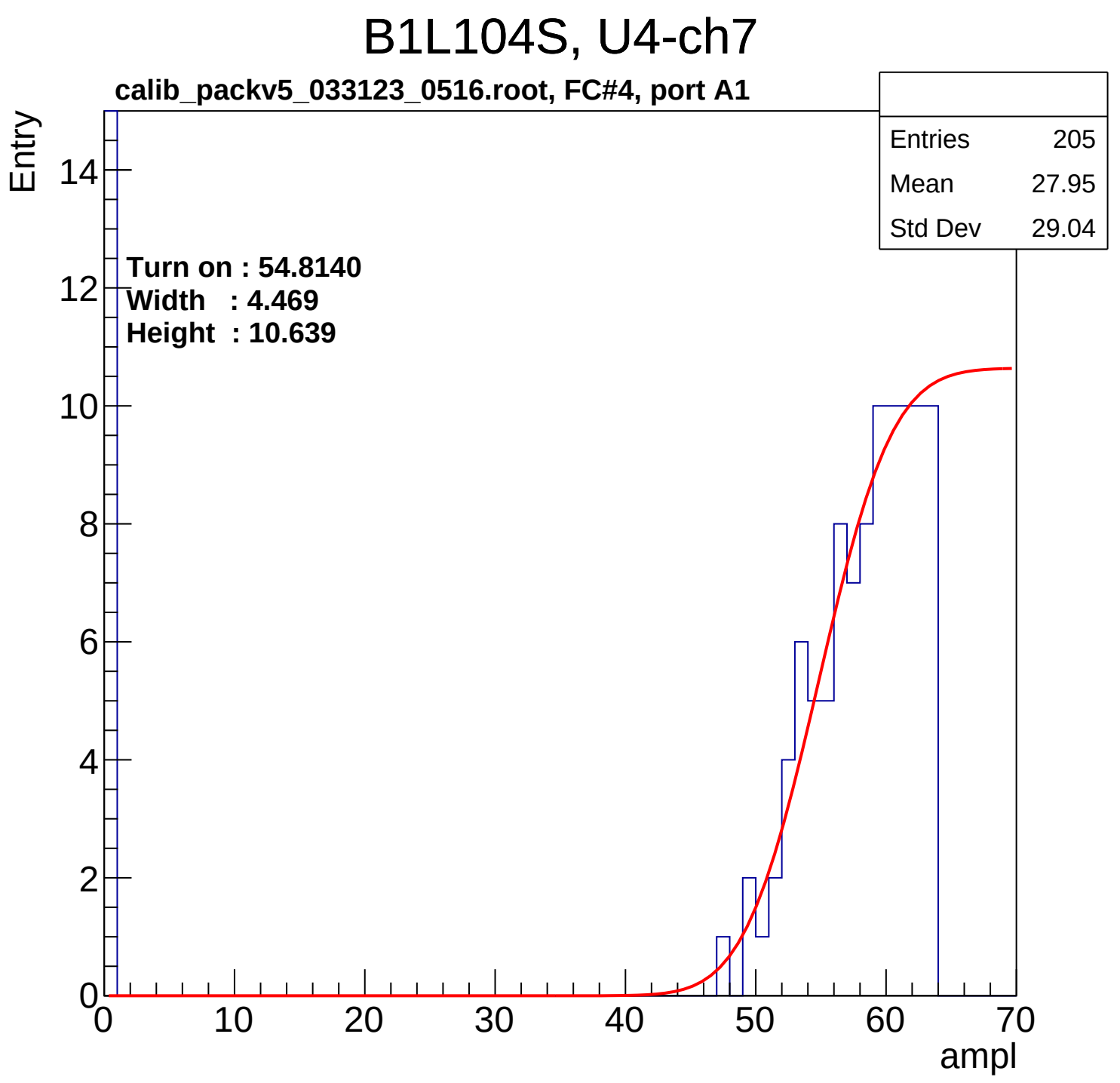

B1L104S, U4-ch2
calib_packv5_033123_0516.root, FC#4, port A1
Entries 230
Mean 29.7
Std Dev 28.61
Turn on : 52.0292
Width : 4.054
Height : 10.011
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

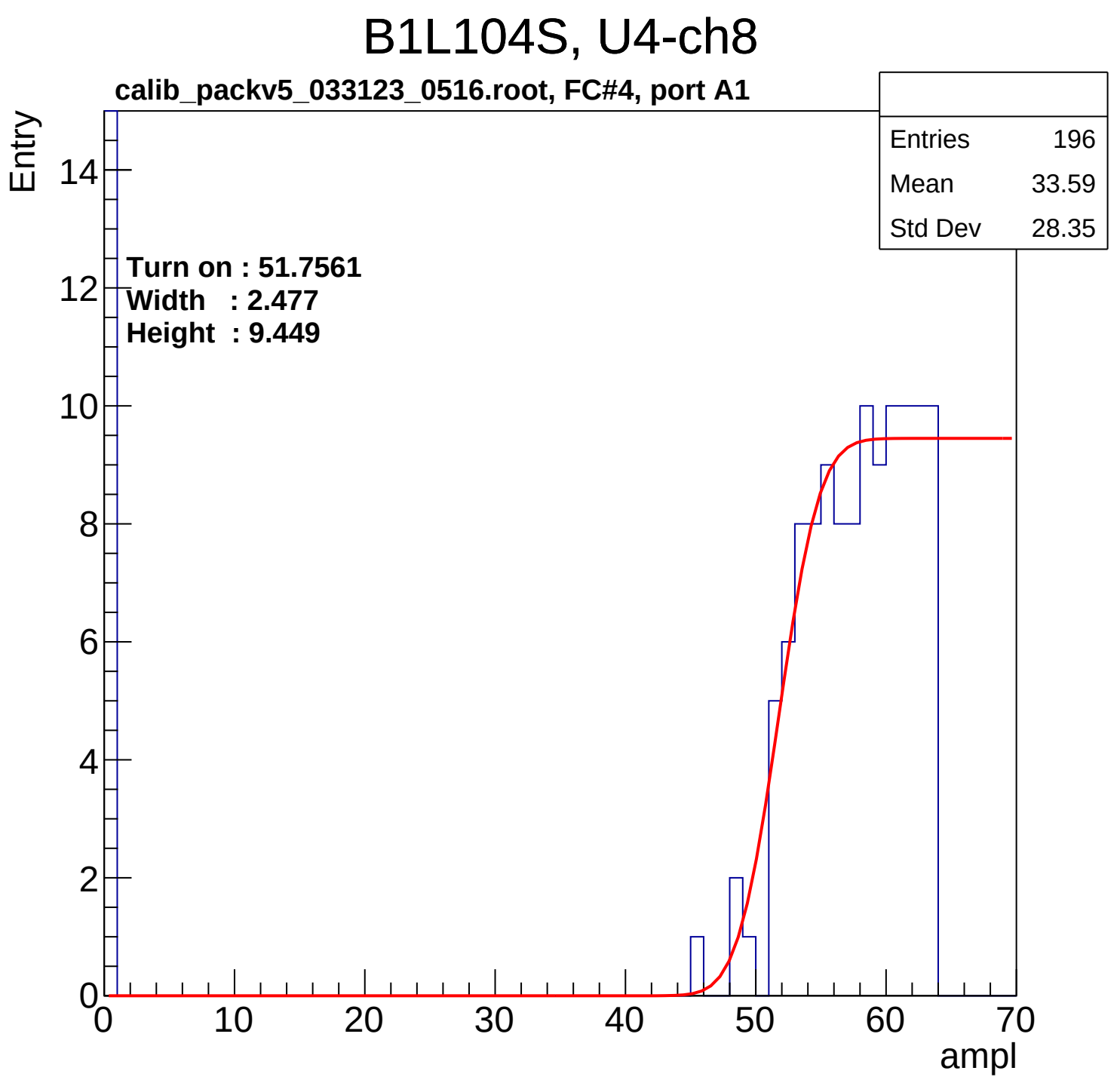

B1L104S, U4-ch3
calib_packv5_033123_0516.root, FC#4, port A1
Entries 210
Mean 26.7
Std Dev 29.18
Turn on : 54.5101
Width : 2.097
Height : 9.874
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

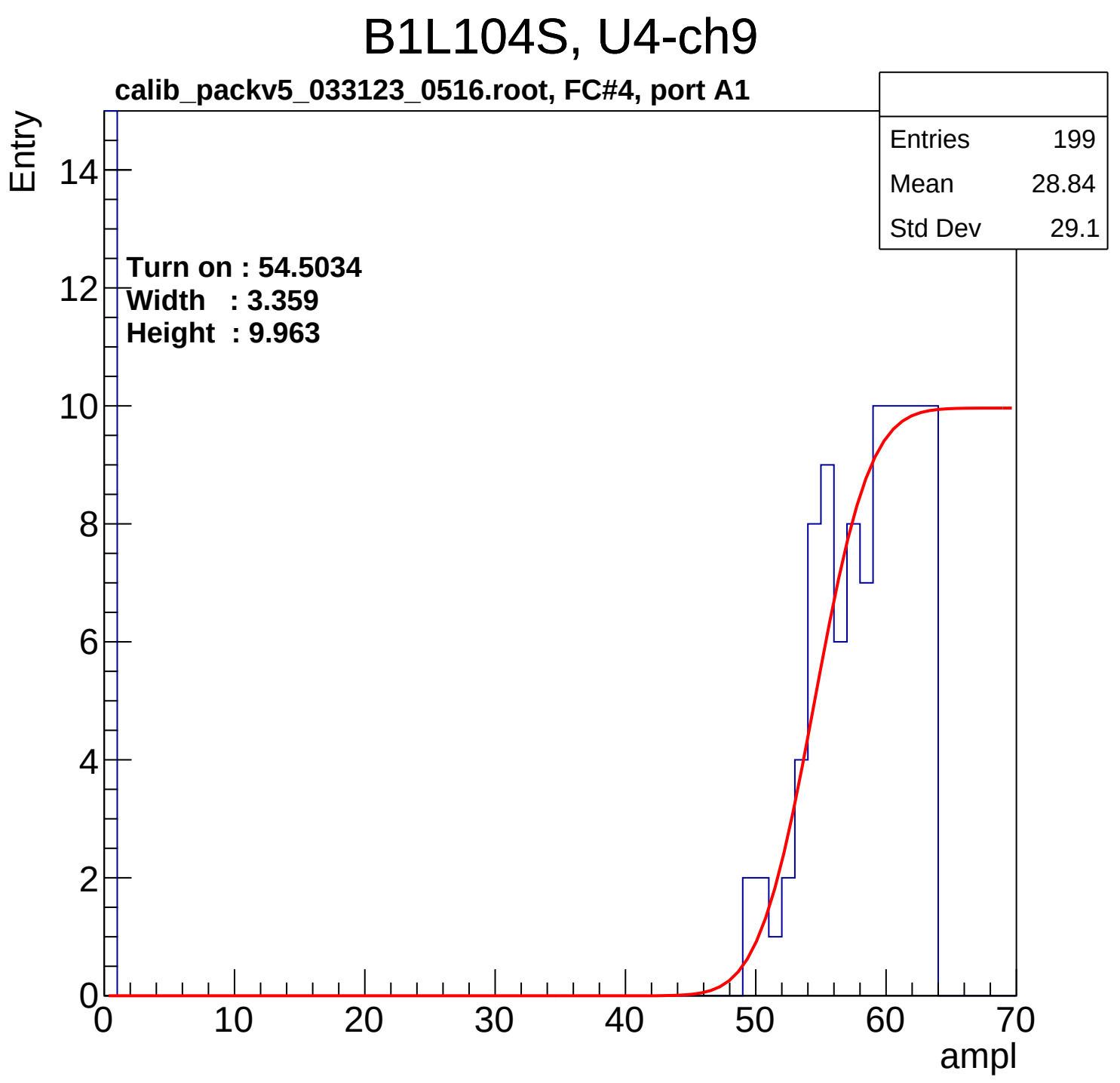

B1L104S, U4-ch4
calib_packv5_033123_0516.root, FC#4, port A1
Entries 236
Mean 26.92
Std Dev 28.72
Turn on : 53.6733
Width : 4.709
Height : 10.596
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

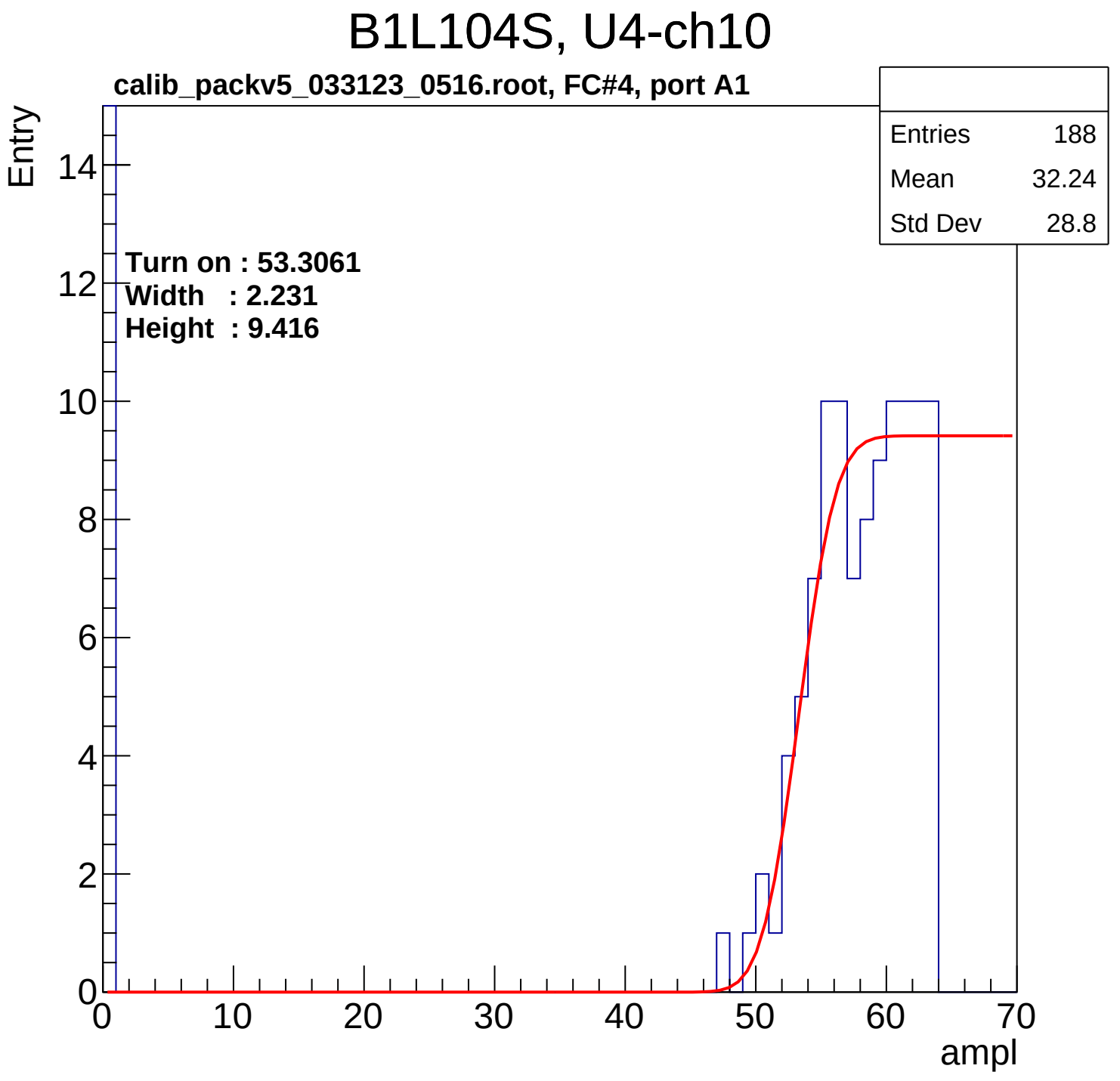

B1L104S, U4-ch5
calib_packv5_033123_0516.root, FC#4, port A1
Entries 199
Mean 29.41
Std Dev 29.08
Turn on : 54.3939
Width : 4.297
Height : 10.610
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

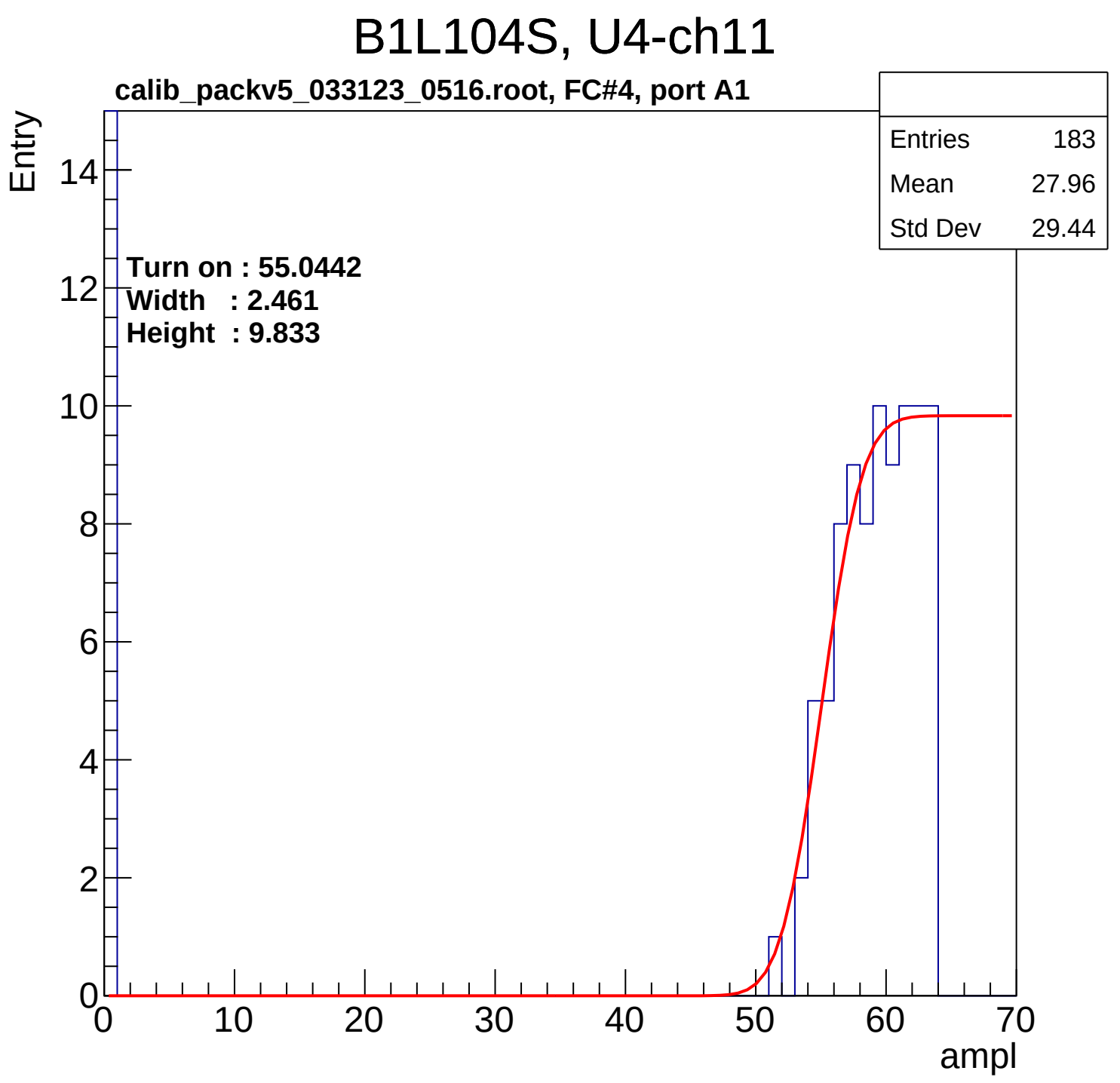

B1L104S, U4-ch6
calib_packv5_033123_0516.root, FC#4, port A1
Entries 185
Mean 33.86
Std Dev 28.44
Turn on : 53.7292
Width : 4.127
Height : 10.242
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

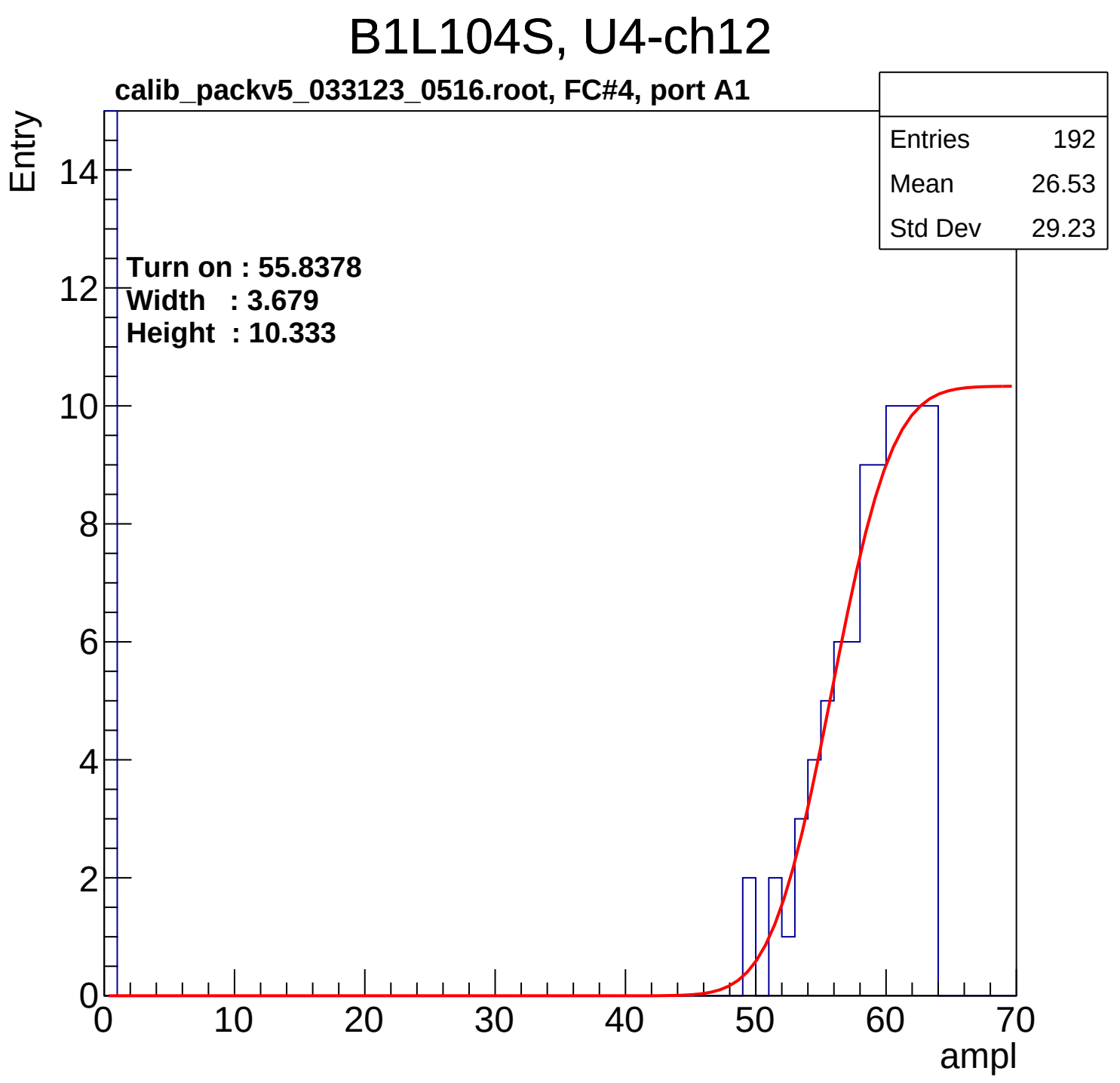

B1L104S, U4-ch7
calib_packv5_033123_0516.root, FC#4, port A1
Entries 205
Mean 27.95
Std Dev 29.04
Turn on : 54.8140
Width : 4.469
Height : 10.639
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

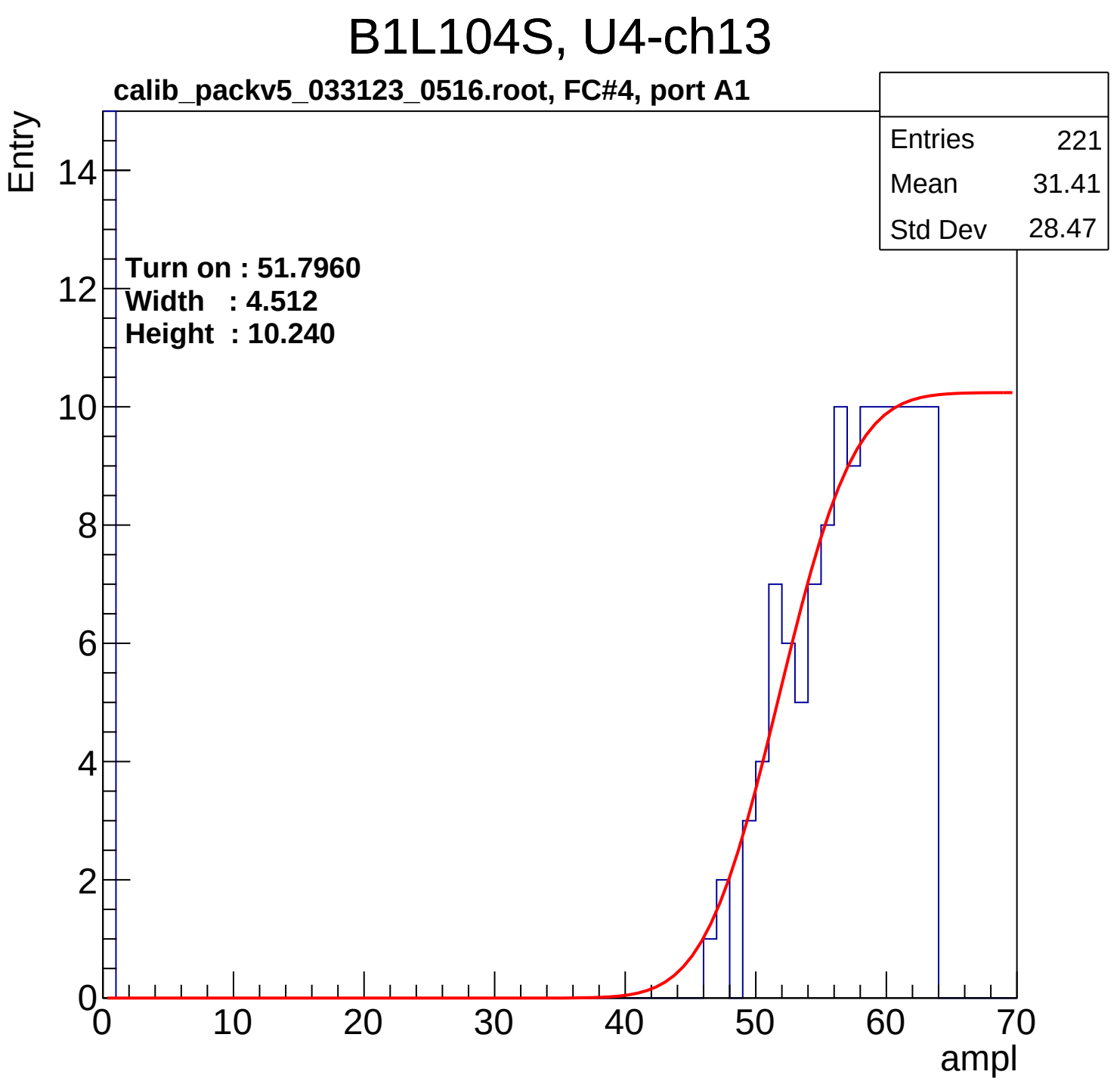

B1L104S, U4-ch8
calib_packv5_033123_0516.root, FC#4, port A1
Entries 196
Mean 33.59
Std Dev 28.35
Turn on : 51.7561
Width : 2.477
Height : 9.449
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

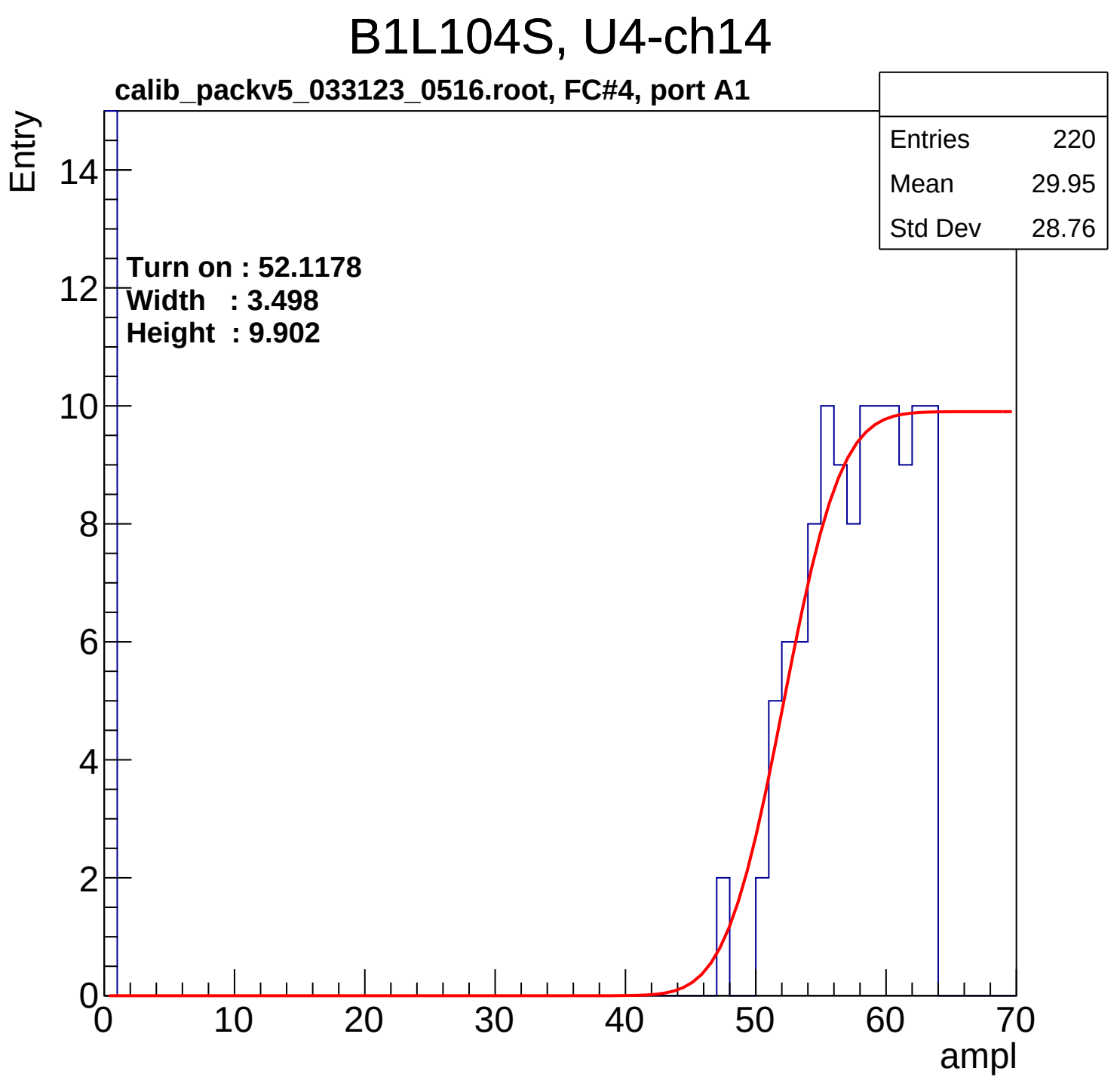

B1L104S, U4-ch9
calib_packv5_033123_0516.root, FC#4, port A1
Entries 199
Mean 28.84
Std Dev 29.1
Turn on : 54.5034
Width : 3.359
Height : 9.963
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

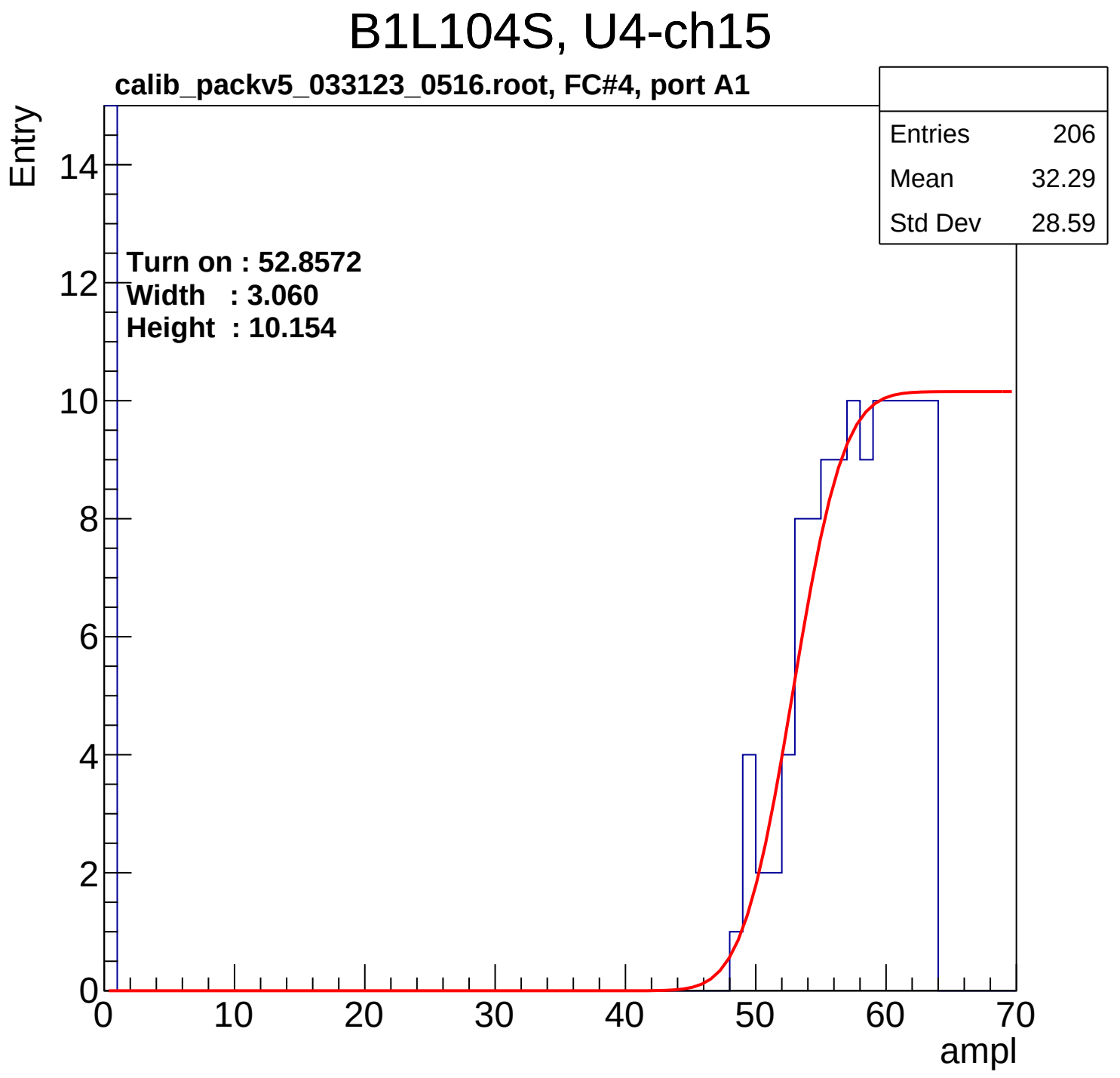

B1L104S, U4-ch10
calib_packv5_033123_0516.root, FC#4, port A1
Entries 188
Mean 32.24
Std Dev 28.8
Turn on : 53.3061
Width : 2.231
Height : 9.416
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

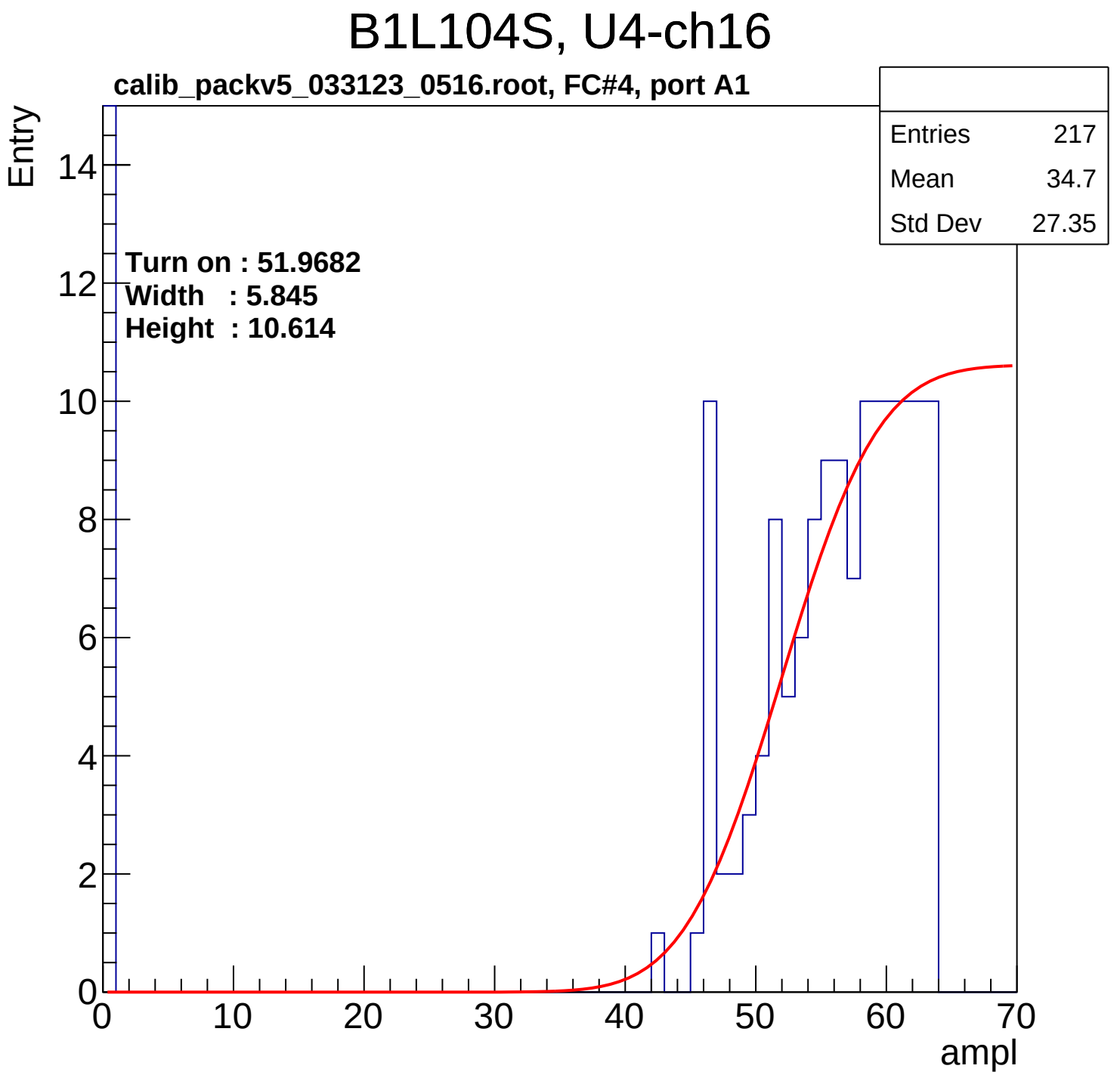

B1L104S, U4-ch11
calib_packv5_033123_0516.root, FC#4, port A1
Entries 183
Mean 27.96
Std Dev 29.44
Turn on : 55.0442
Width : 2.461
Height : 9.833
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

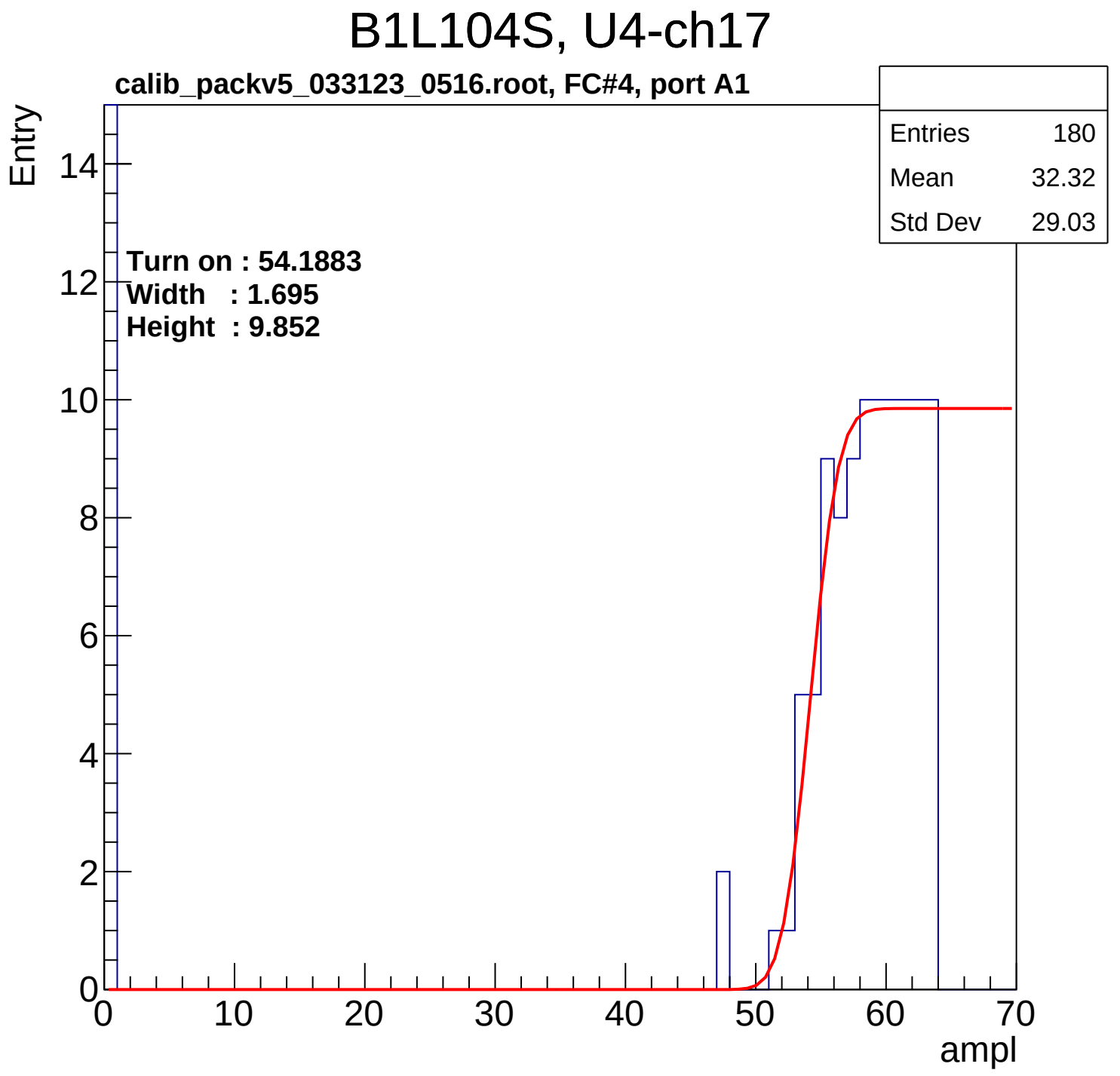

B1L104S, U4-ch12
calib_packv5_033123_0516.root, FC#4, port A1
Entries 192
Mean 26.53
Std Dev 29.23
Turn on : 55.8378
Width : 3.679
Height : 10.333
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

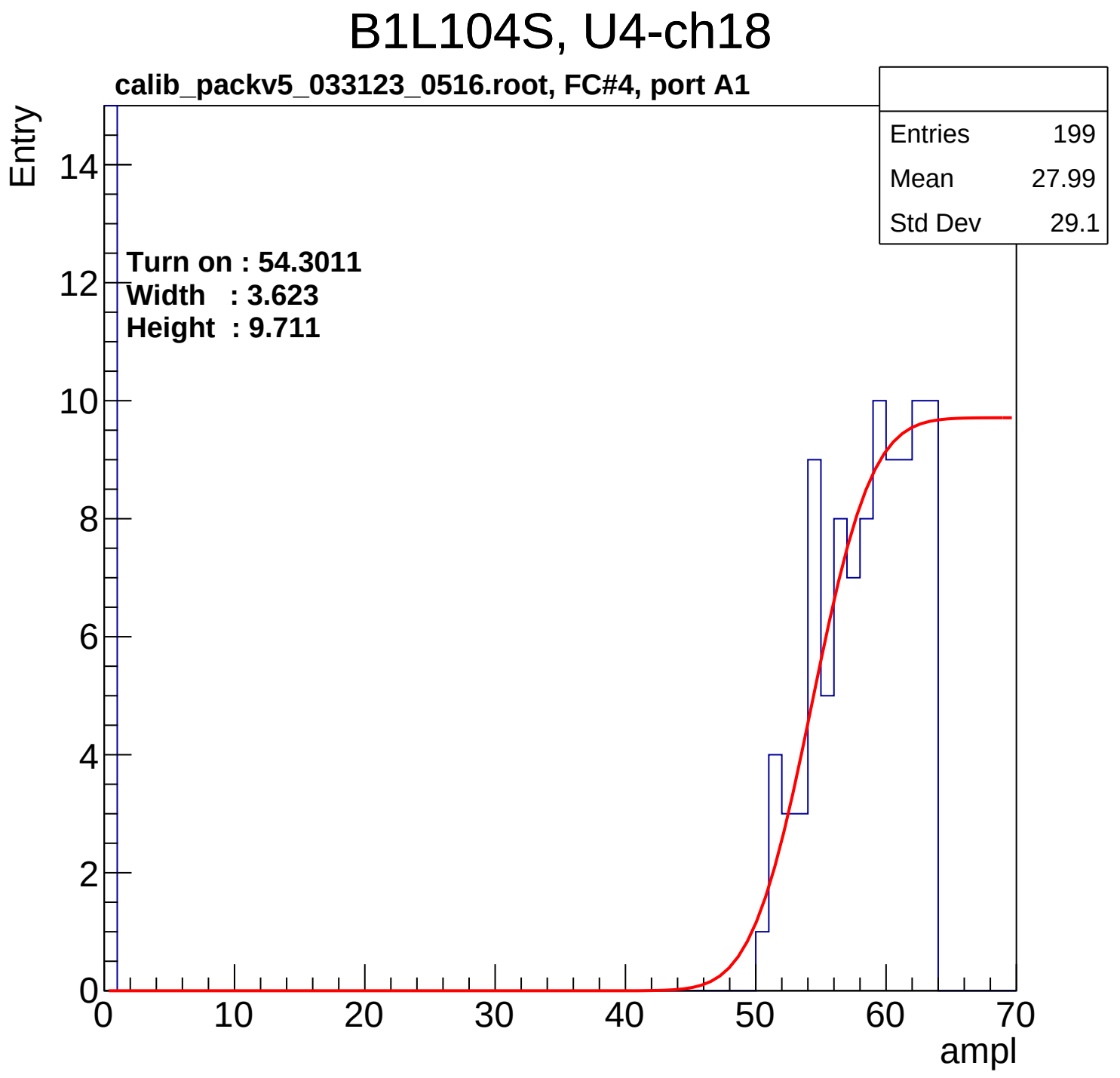

B1L104S, U4-ch13
calib_packv5_033123_0516.root, FC#4, port A1
Entries 221
Mean 31.41
Std Dev 28.47
Turn on : 51.7960
Width : 4.512
Height : 10.240
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

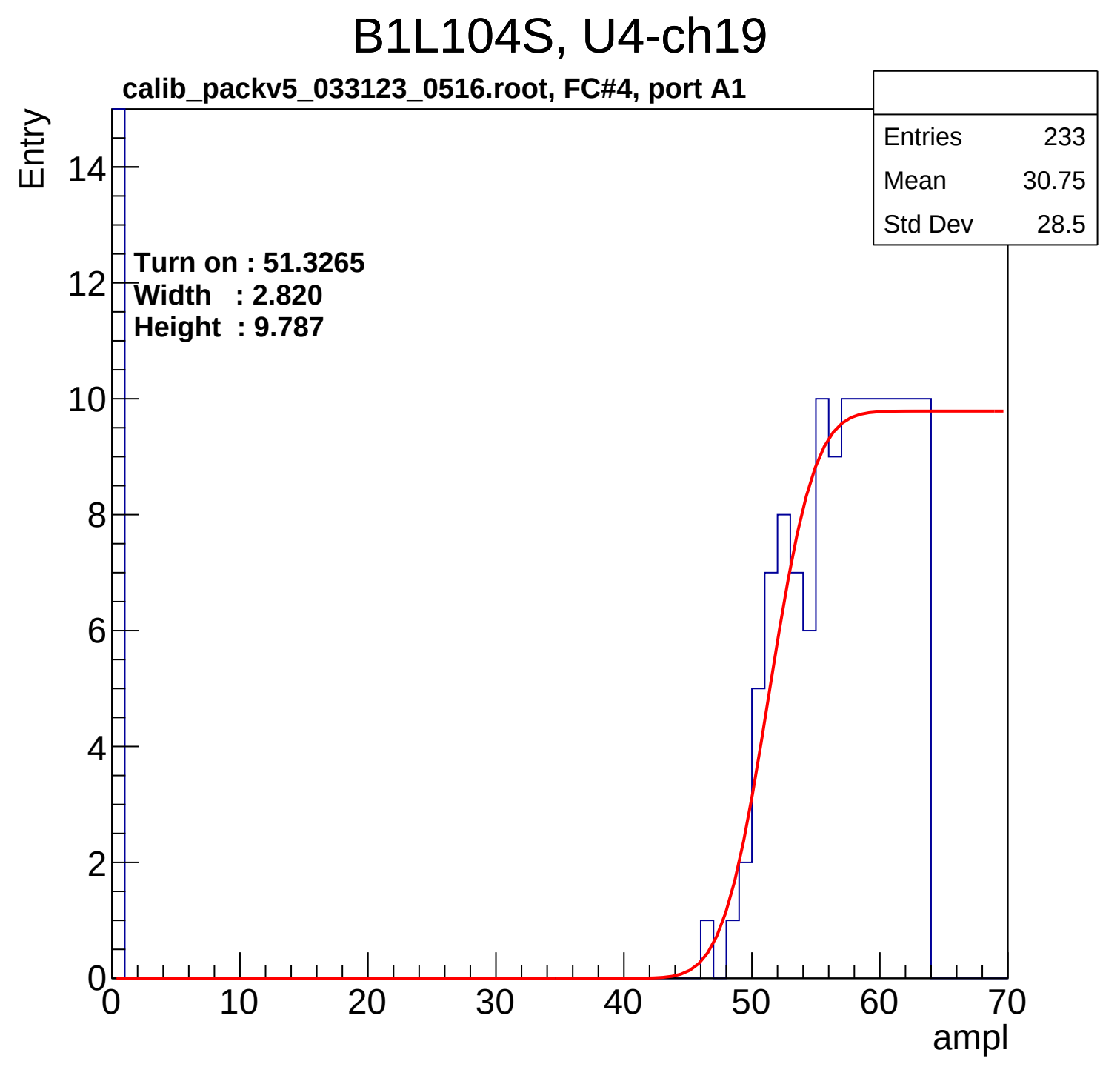

B1L104S, U4-ch14
calib_packv5_033123_0516.root, FC#4, port A1
Entries 220
Mean 29.95
Std Dev 28.76
Turn on : 52.1178
Width : 3.498
Height : 9.902
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

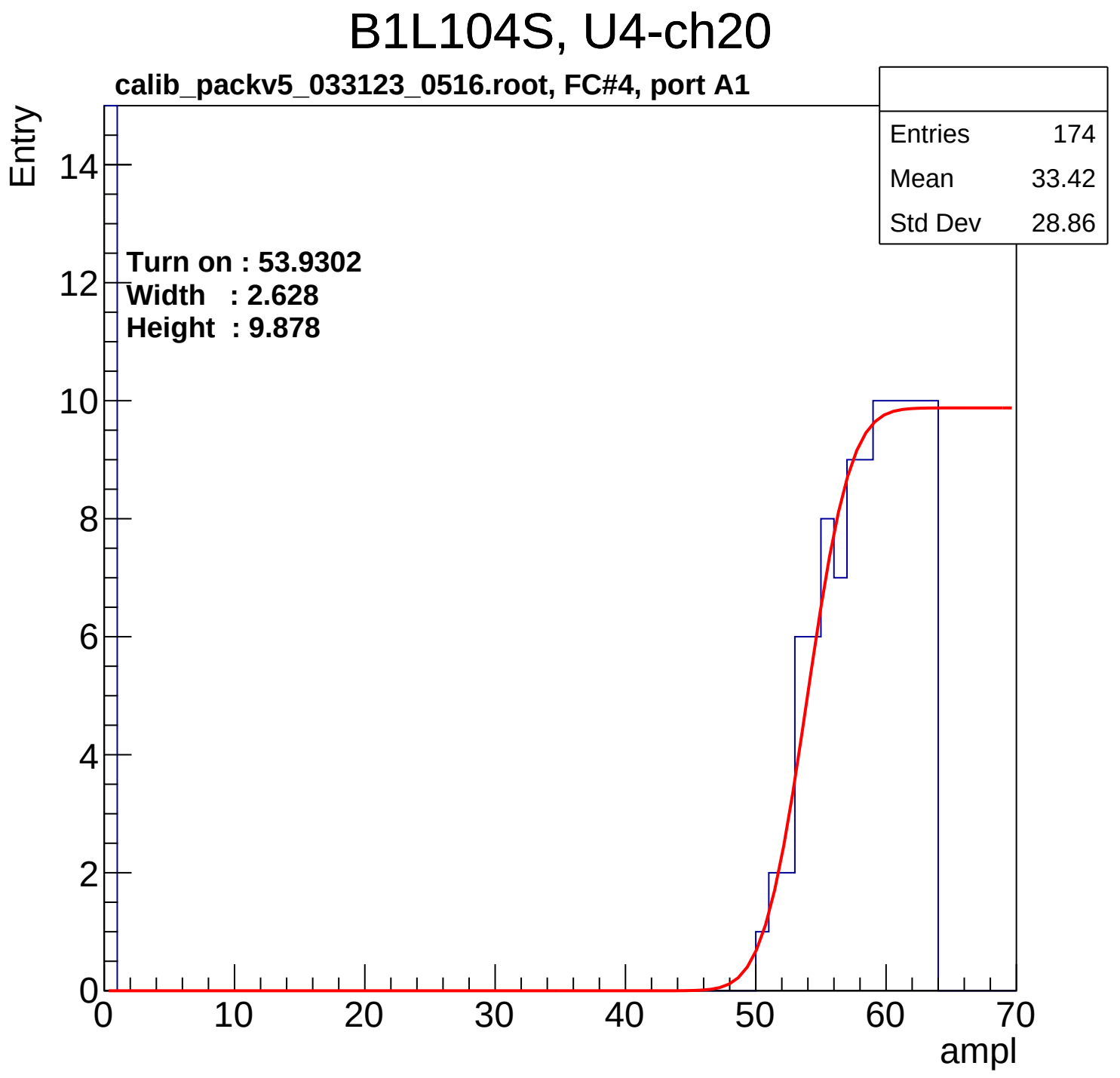

B1L104S, U4-ch15
calib_packv5_033123_0516.root, FC#4, port A1
Entries 206
Mean 32.29
Std Dev 28.59
Turn on : 52.8572
Width : 3.060
Height : 10.154
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

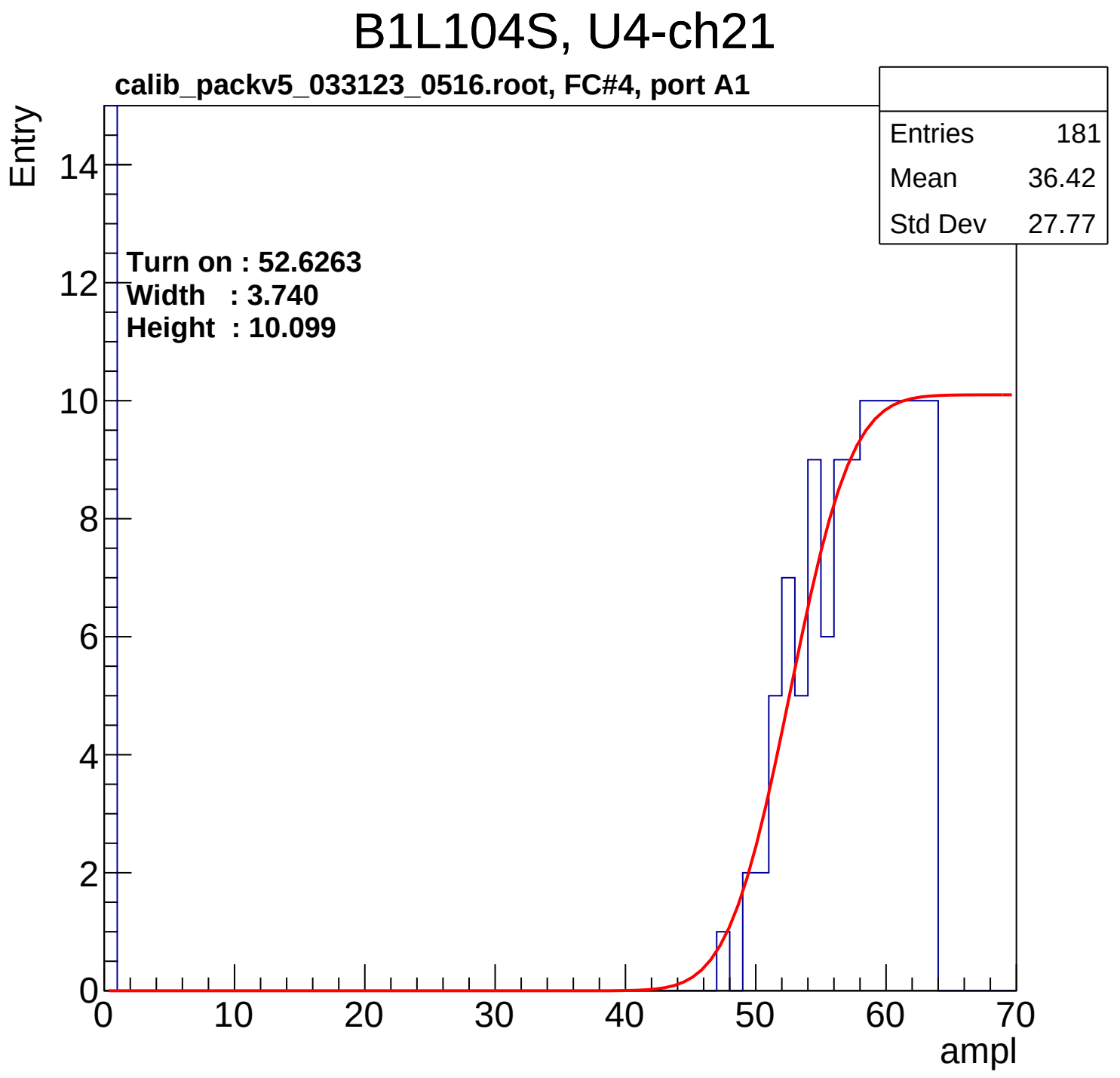

B1L104S, U4-ch16
calib_packv5_033123_0516.root, FC#4, port A1
Entries 217
Mean 34.7
Std Dev 27.35
Turn on : 51.9682
Width : 5.845
Height : 10.614
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

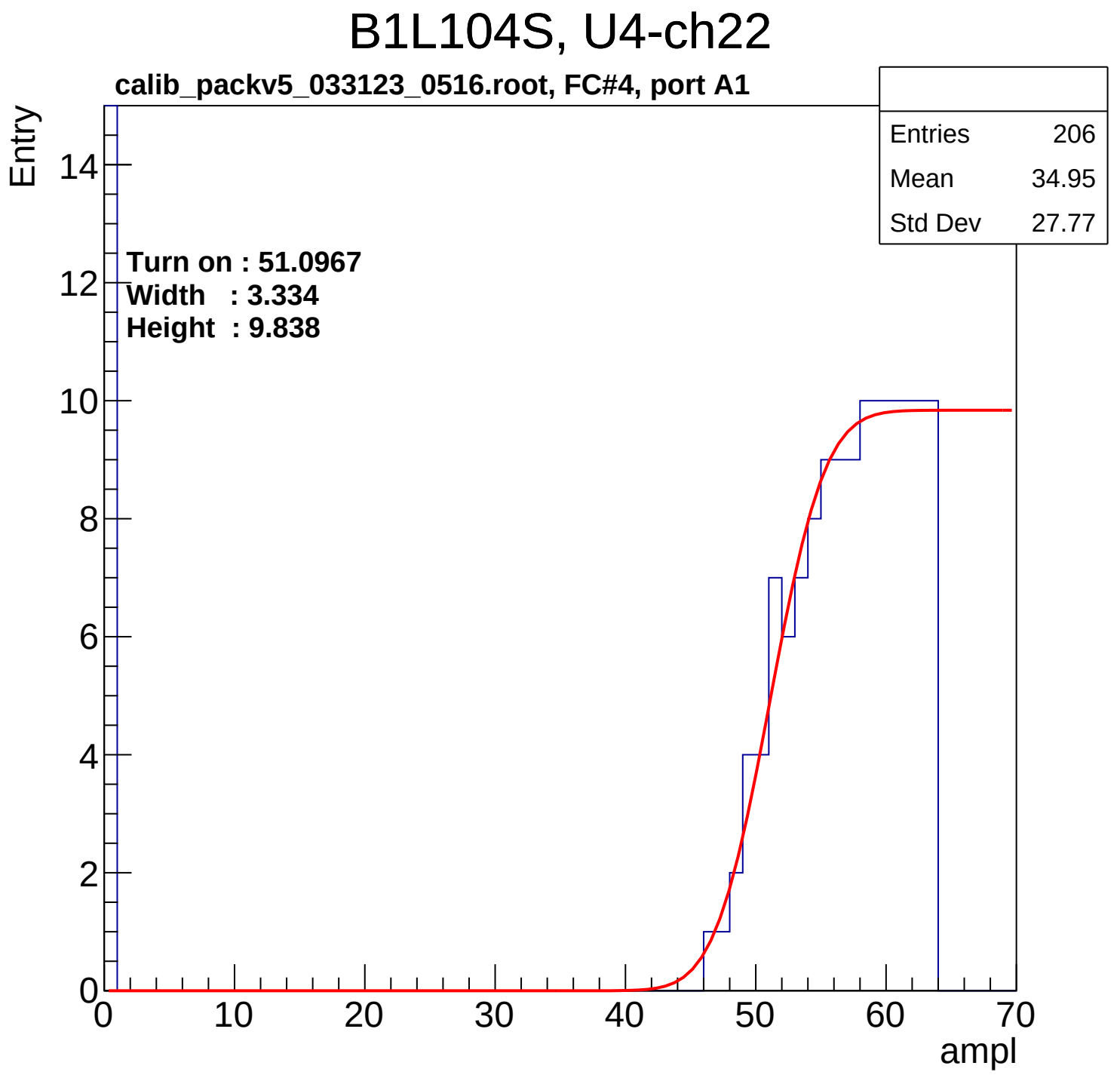

B1L104S, U4-ch17
calib_packv5_033123_0516.root, FC#4, port A1
Entries 180
Mean 32.32
Std Dev 29.03
Turn on : 54.1883
Width : 1.695
Height : 9.852
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

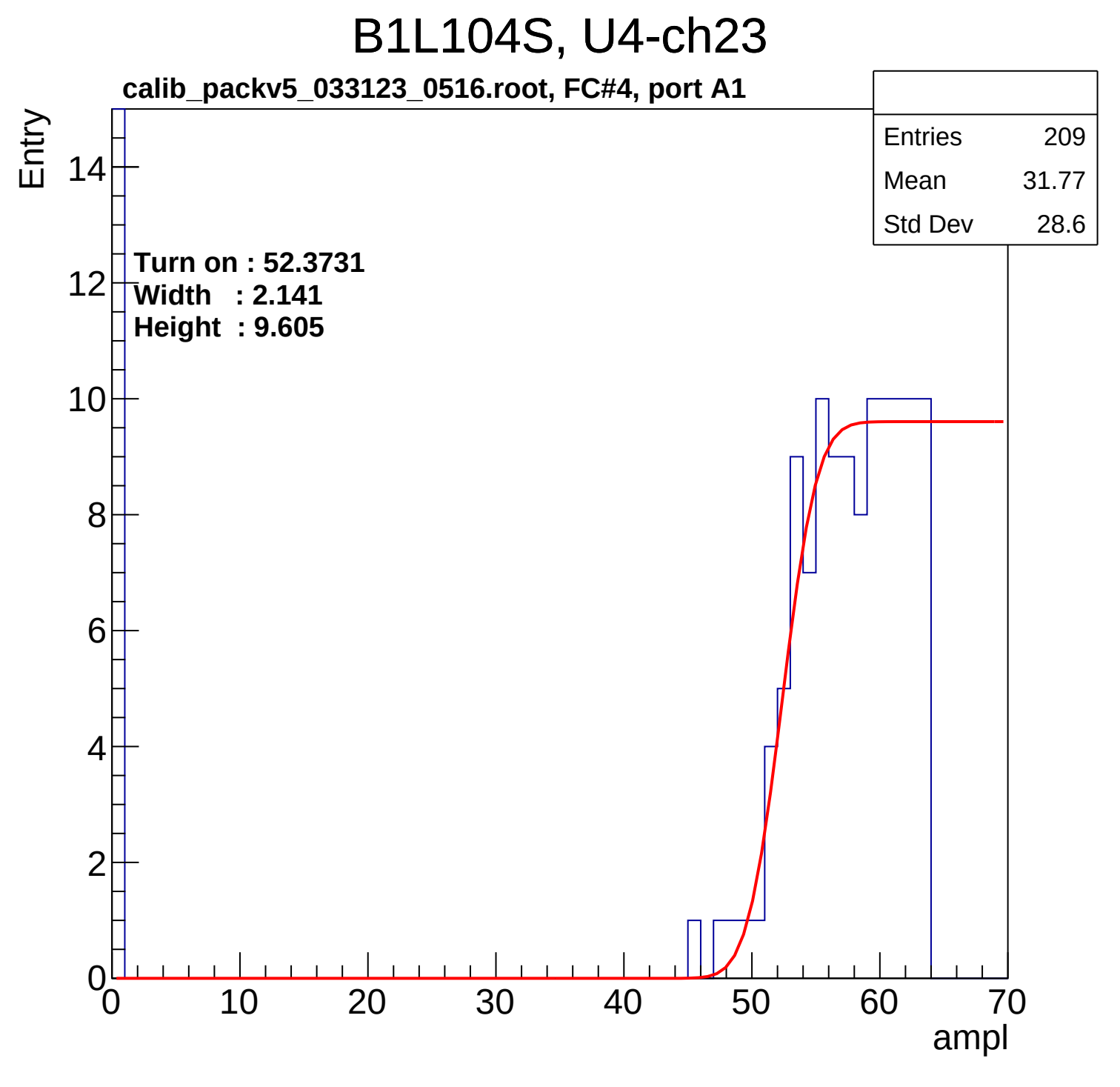

B1L104S, U4-ch18
calib_packv5_033123_0516.root, FC#4, port A1
Entries 199
Mean 27.99
Std Dev 29.1
Turn on : 54.3011
Width : 3.623
Height : 9.711
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

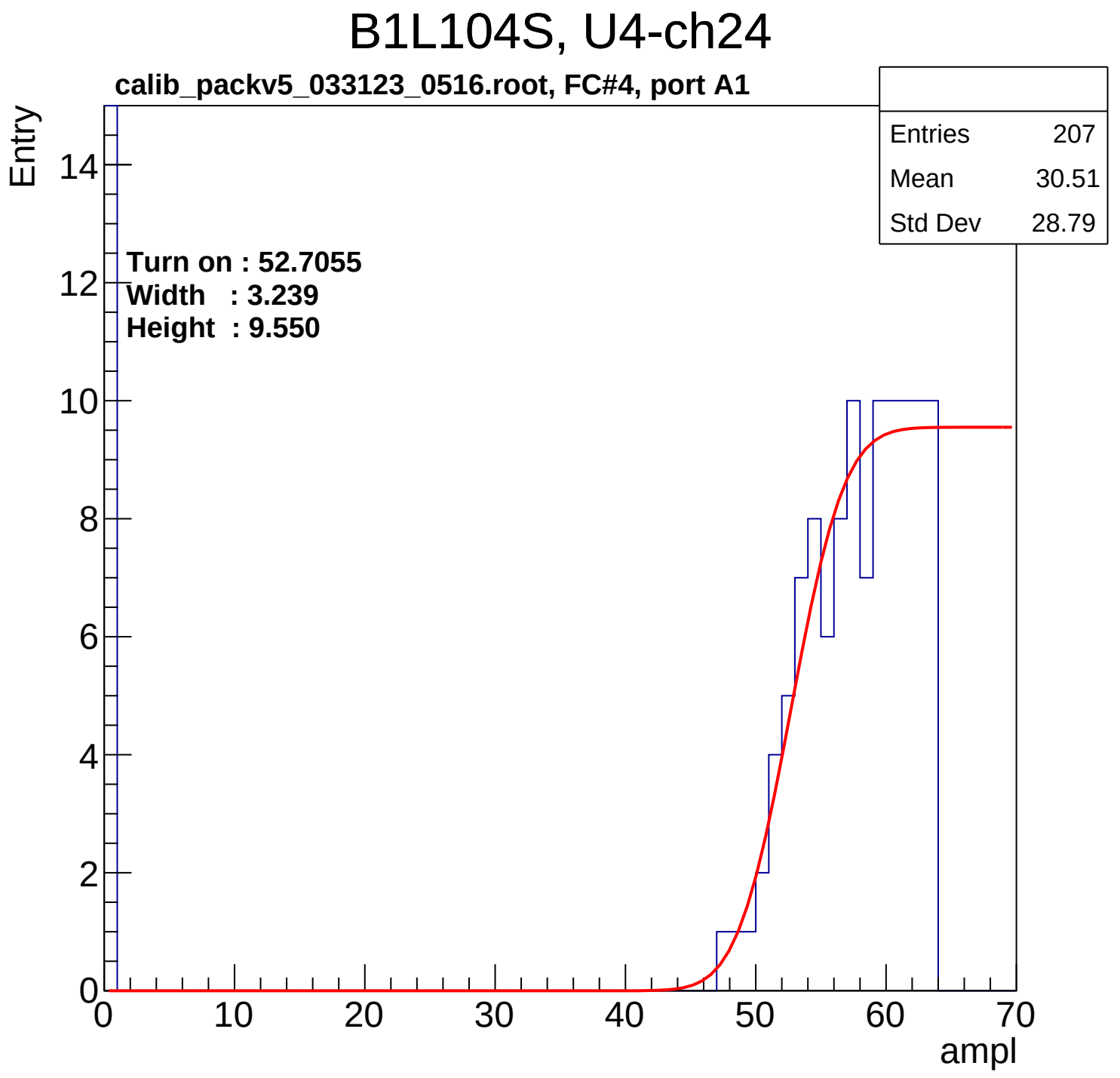

B1L104S, U4-ch19
calib_packv5_033123_0516.root, FC#4, port A1
Entries 233
Mean 30.75
Std Dev 28.5
Turn on : 51.3265
Width : 2.820
Height : 9.787
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

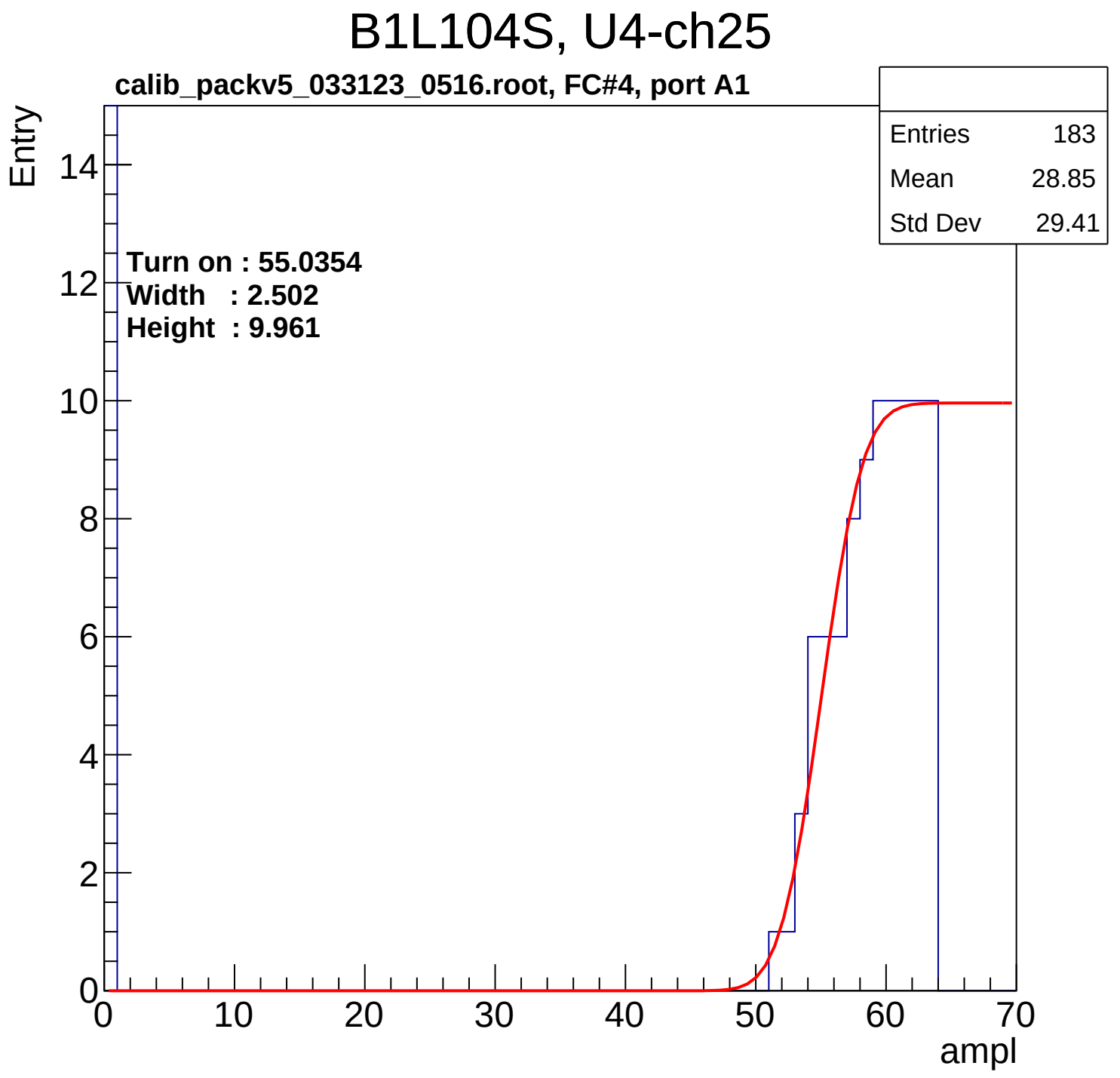

B1L104S, U4-ch20
calib_packv5_033123_0516.root, FC#4, port A1
Entries 174
Mean 33.42
Std Dev 28.86
Turn on : 53.9302
Width : 2.628
Height : 9.878
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

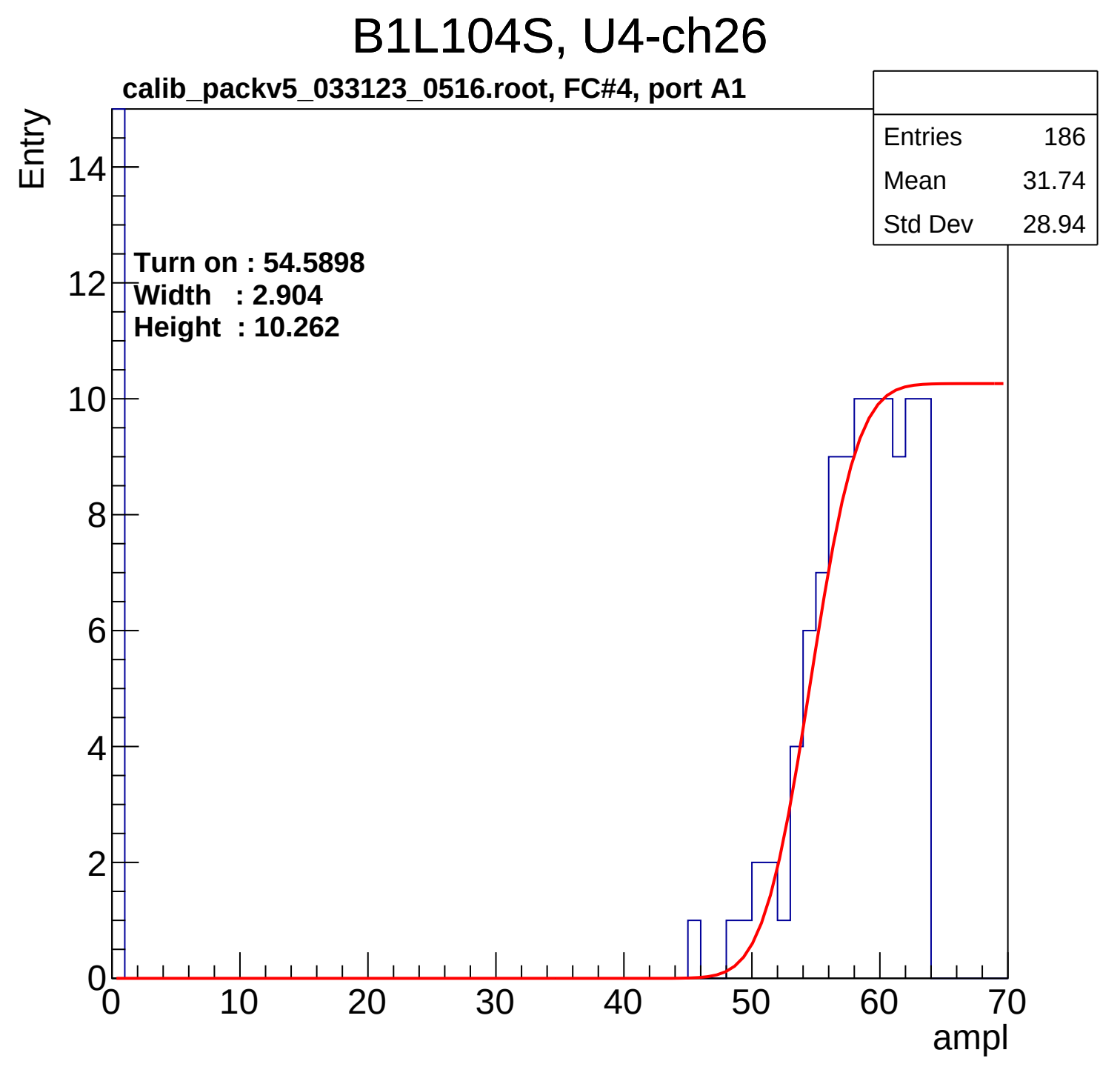

B1L104S, U4-ch21
calib_packv5_033123_0516.root, FC#4, port A1
Entries 181
Mean 36.42
Std Dev 27.77
Turn on : 52.6263
Width : 3.740
Height : 10.099
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

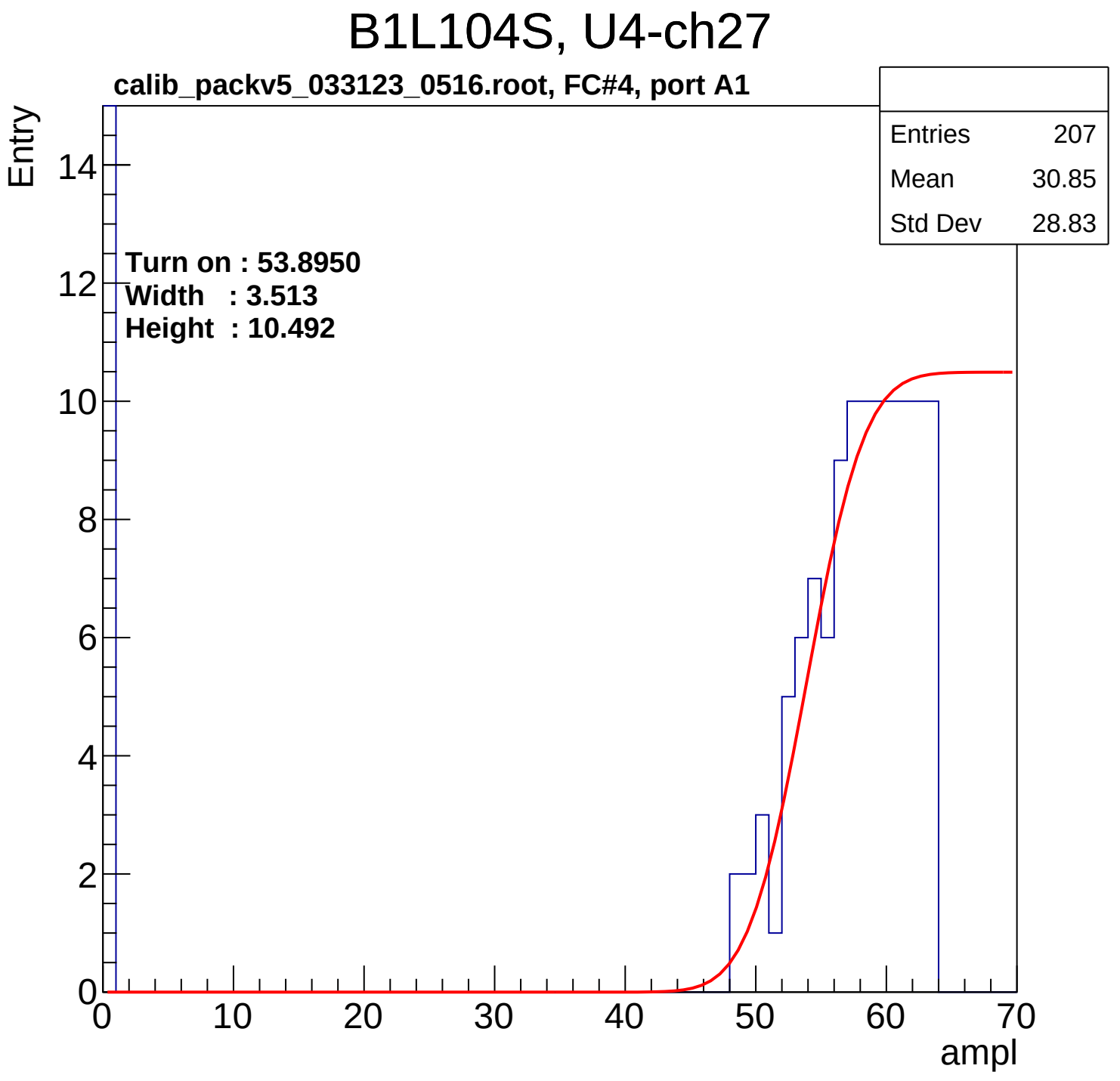

B1L104S, U4-ch22
calib_packv5_033123_0516.root, FC#4, port A1
Entries 206
Mean 34.95
Std Dev 27.77
Turn on : 51.0967
Width : 3.334
Height : 9.838
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

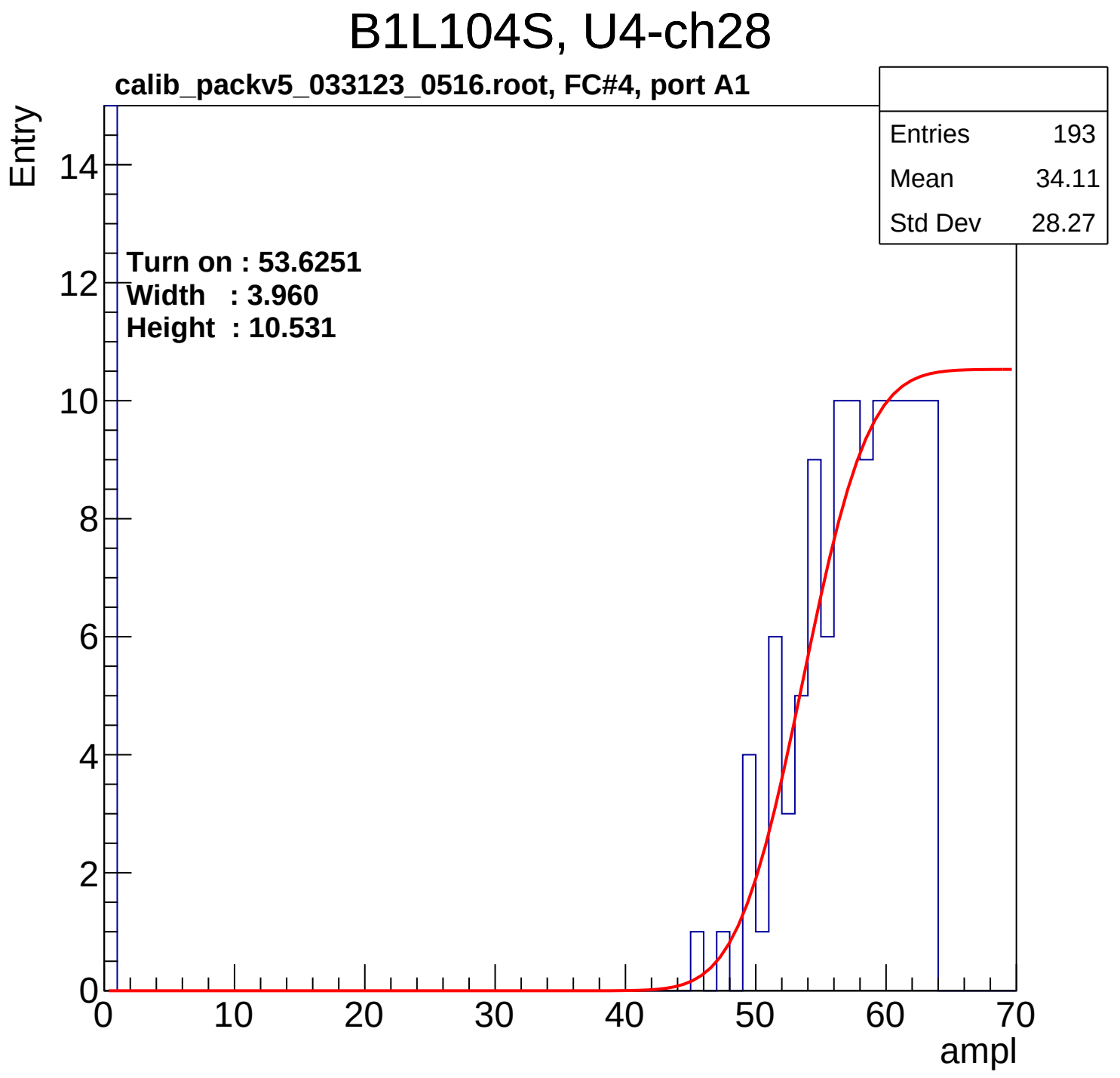

B1L104S, U4-ch23
calib_packv5_033123_0516.root, FC#4, port A1
Entries 209
Mean 31.77
Std Dev 28.6
Turn on : 52.3731
Width : 2.141
Height : 9.605
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

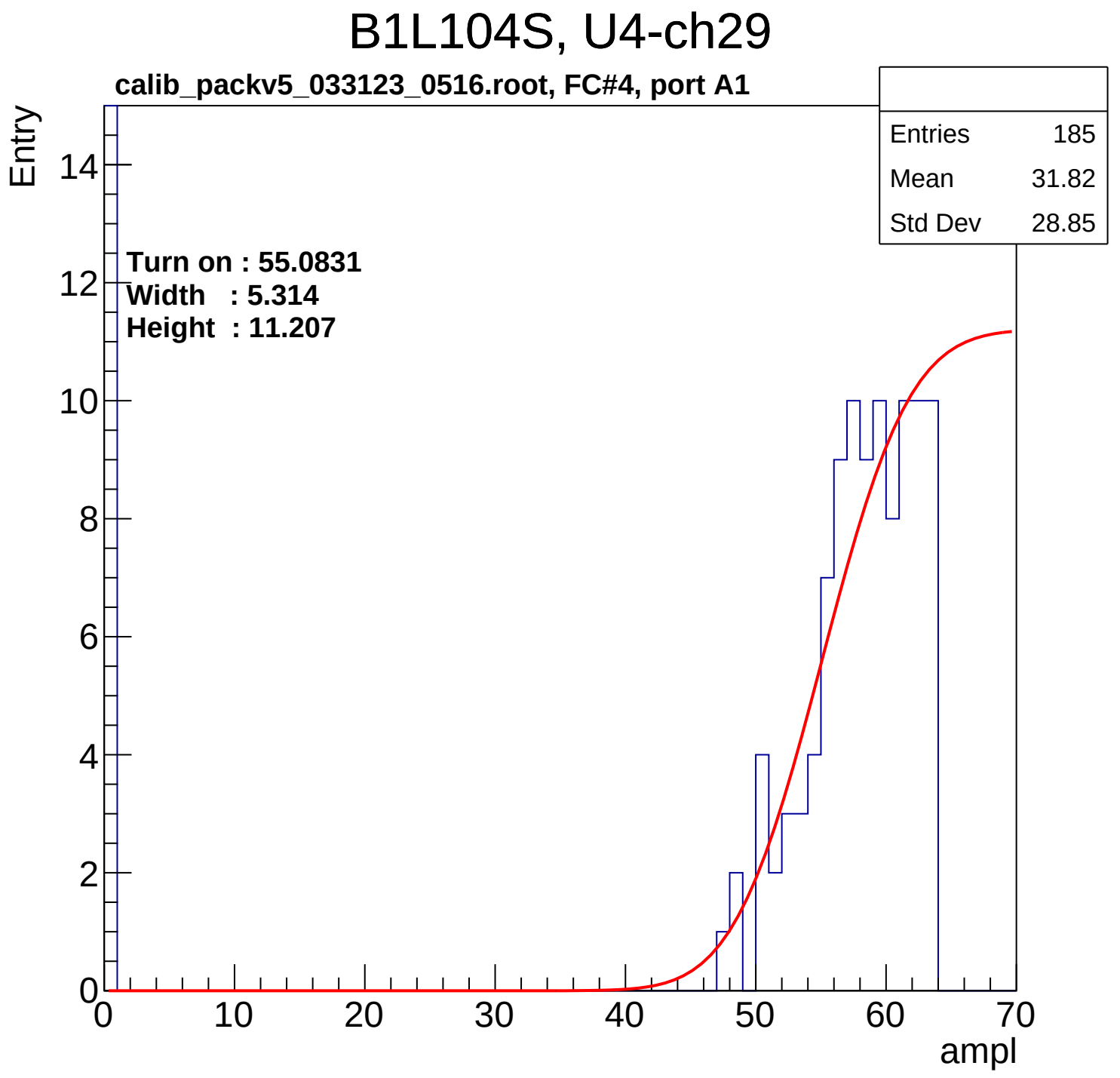

B1L104S, U4-ch24
calib_packv5_033123_0516.root, FC#4, port A1
Entries 207
Mean 30.51
Std Dev 28.79
Turn on : 52.7055
Width : 3.239
Height : 9.550
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

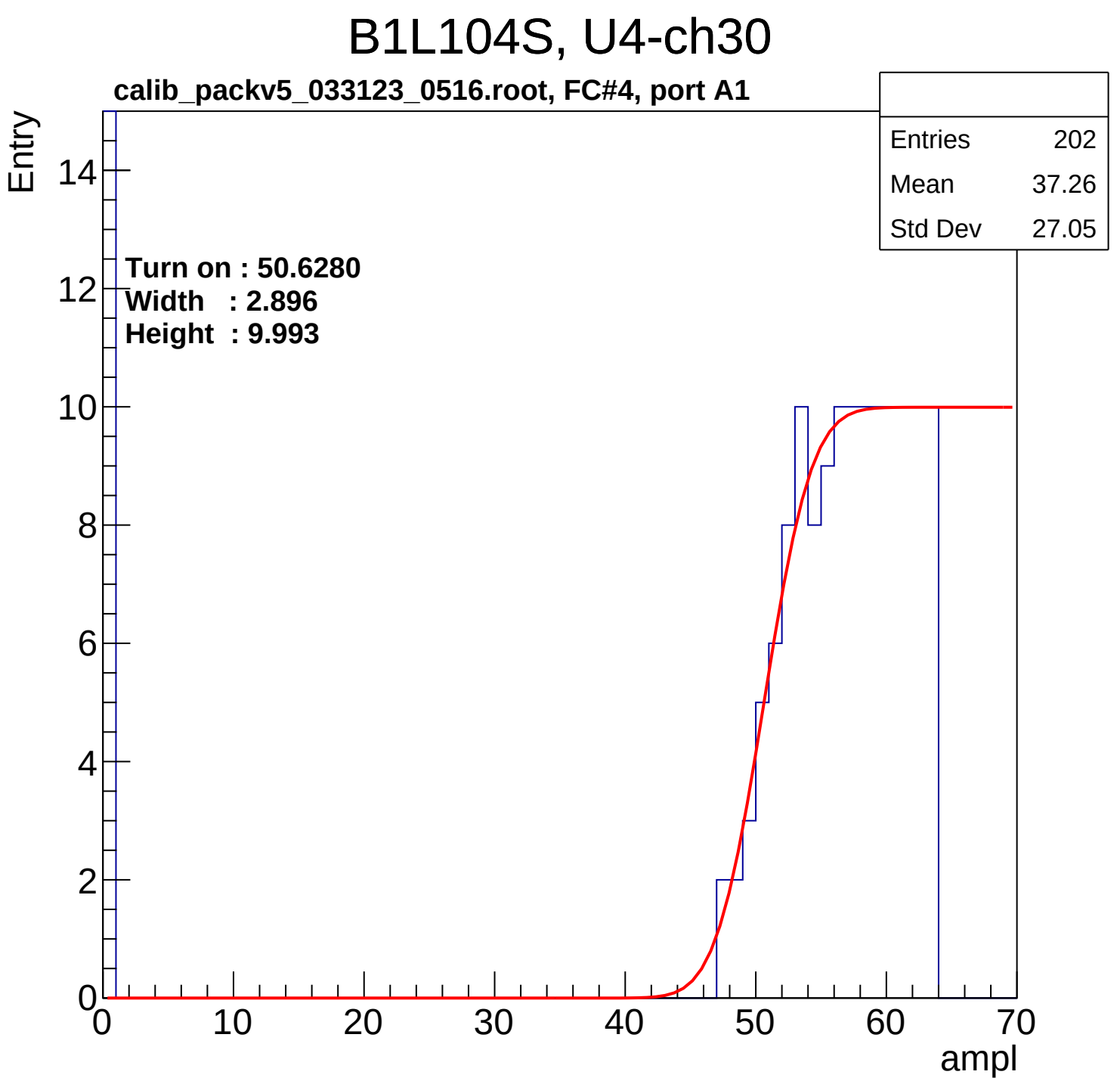

B1L104S, U4-ch25
calib_packv5_033123_0516.root, FC#4, port A1
Entries 183
Mean 28.85
Std Dev 29.41
Turn on : 55.0354
Width : 2.502
Height : 9.961
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

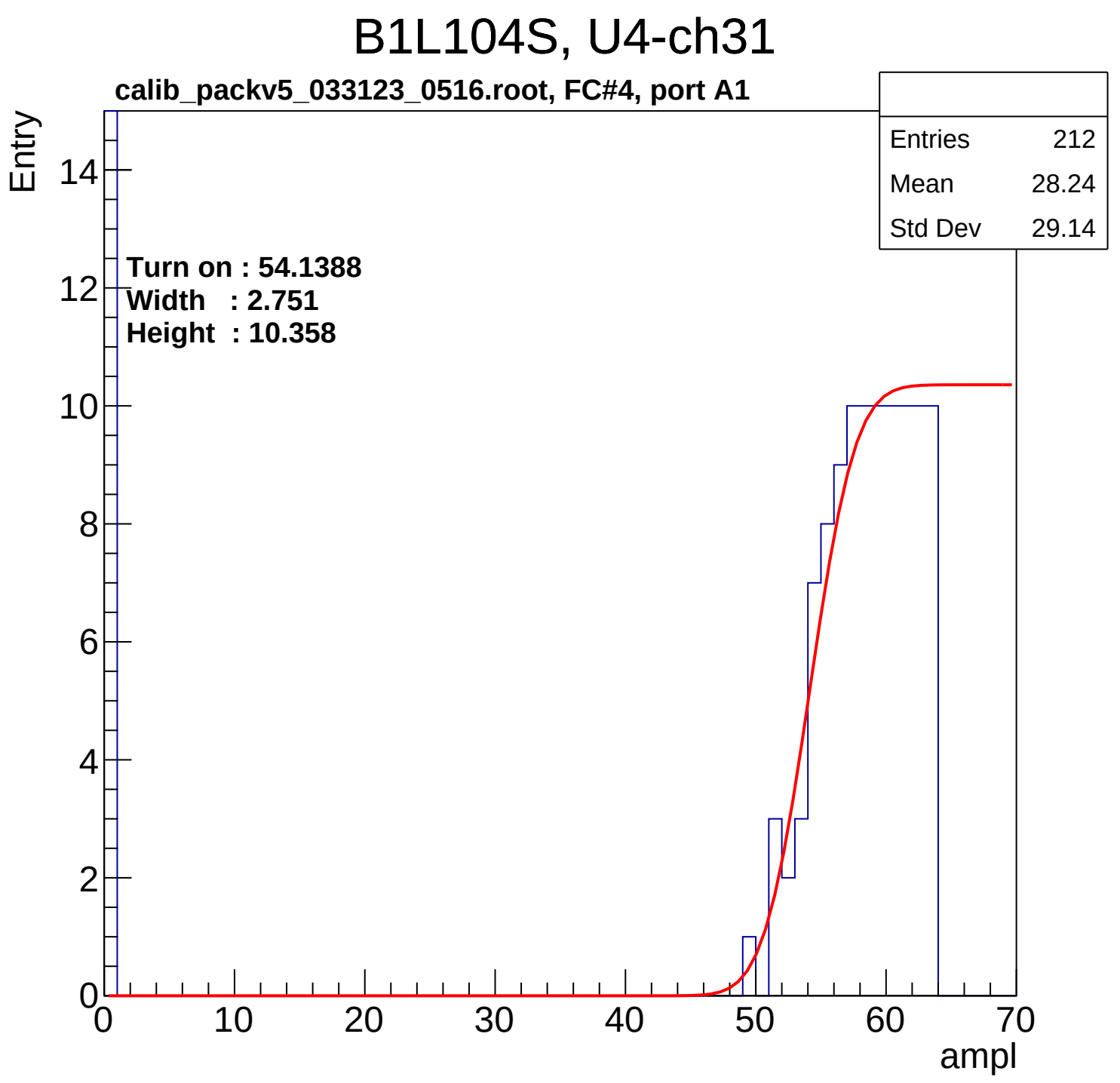

B1L104S, U4-ch26
calib_packv5_033123_0516.root, FC#4, port A1
Entries 186
Mean 31.74
Std Dev 28.94
Turn on : 54.5898
Width : 2.904
Height : 10.262
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

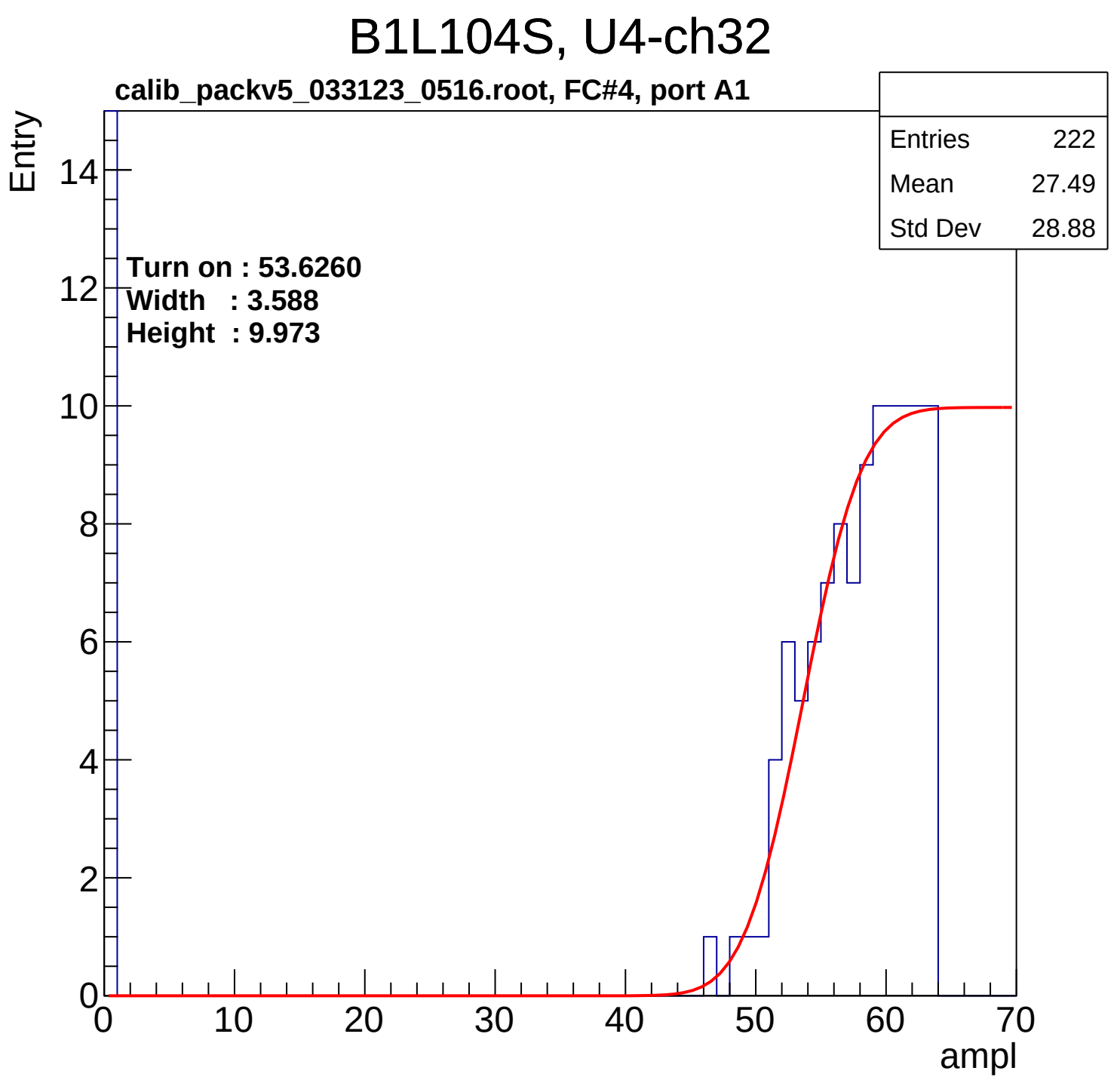

B1L104S, U4-ch27
calib_packv5_033123_0516.root, FC#4, port A1
Entries 207
Mean 30.85
Std Dev 28.83
Turn on : 53.8950
Width : 3.513
Height : 10.492
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

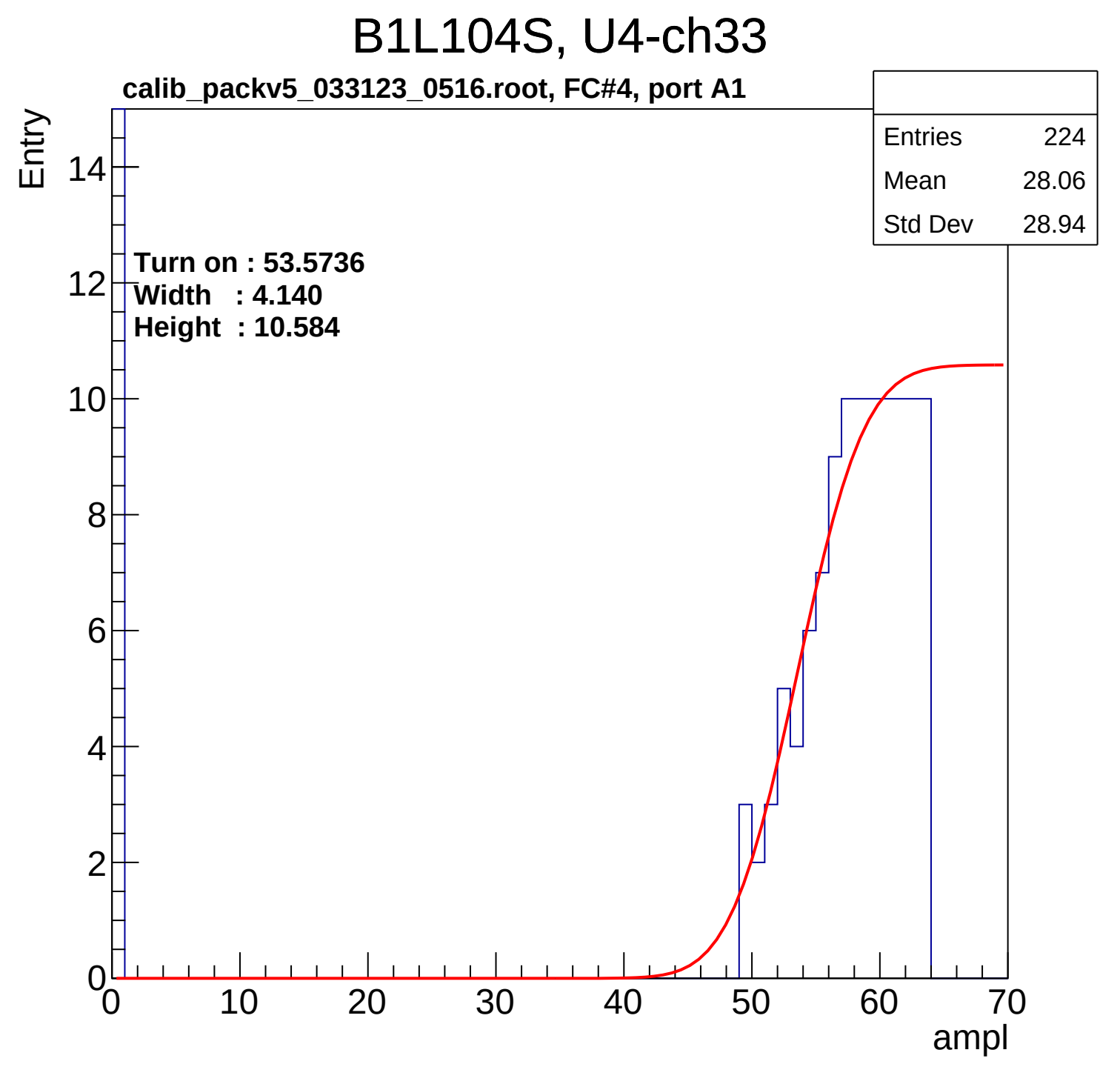

B1L104S, U4-ch28
calib_packv5_033123_0516.root, FC#4, port A1
Entries 193
Mean 34.11
Std Dev 28.27
Turn on : 53.6251
Width : 3.960
Height : 10.531
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

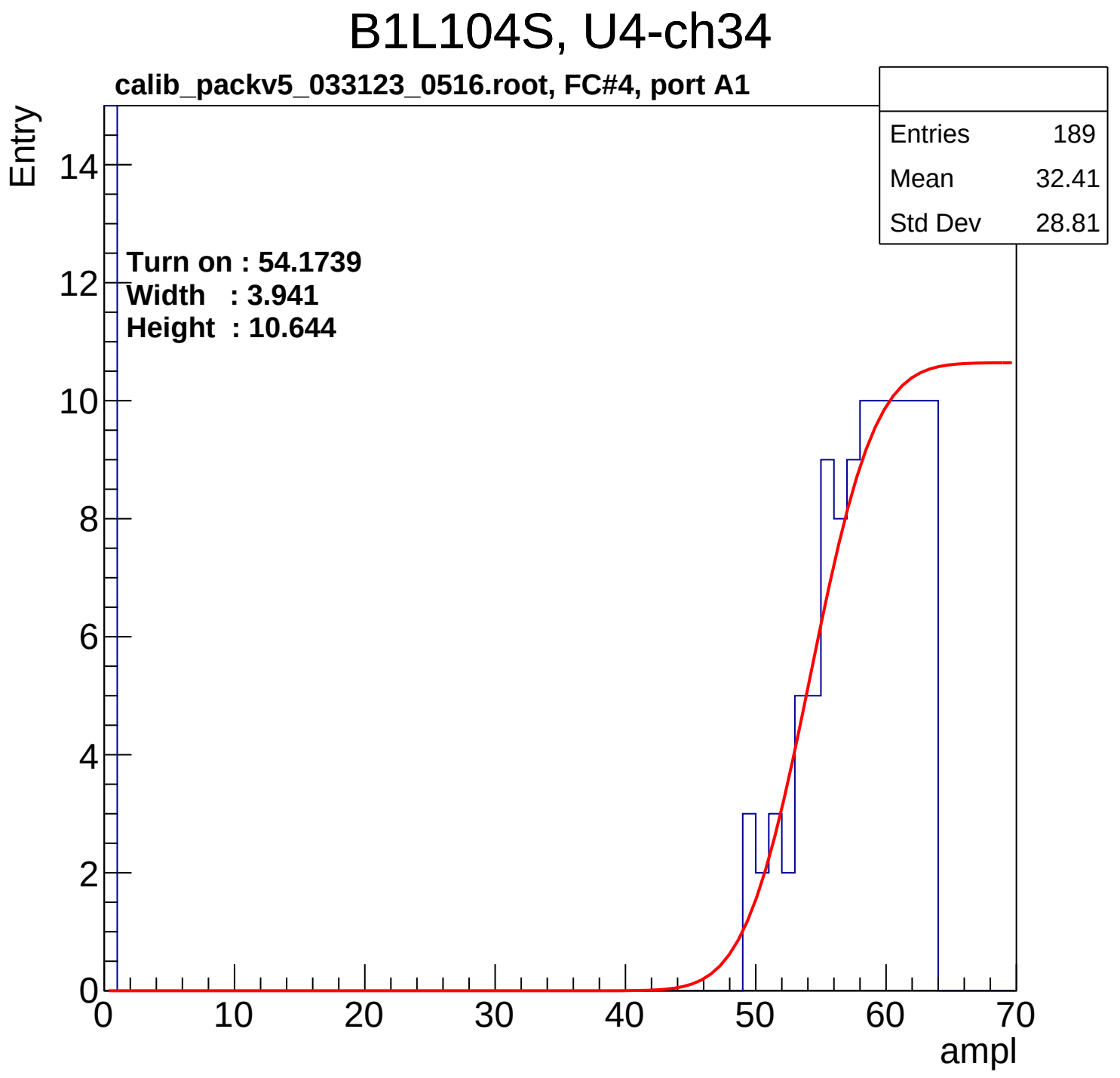

B1L104S, U4-ch29
calib_packv5_033123_0516.root, FC#4, port A1
Entries 185
Mean 31.82
Std Dev 28.85
Turn on : 55.0831
Width : 5.314
Height : 11.207
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

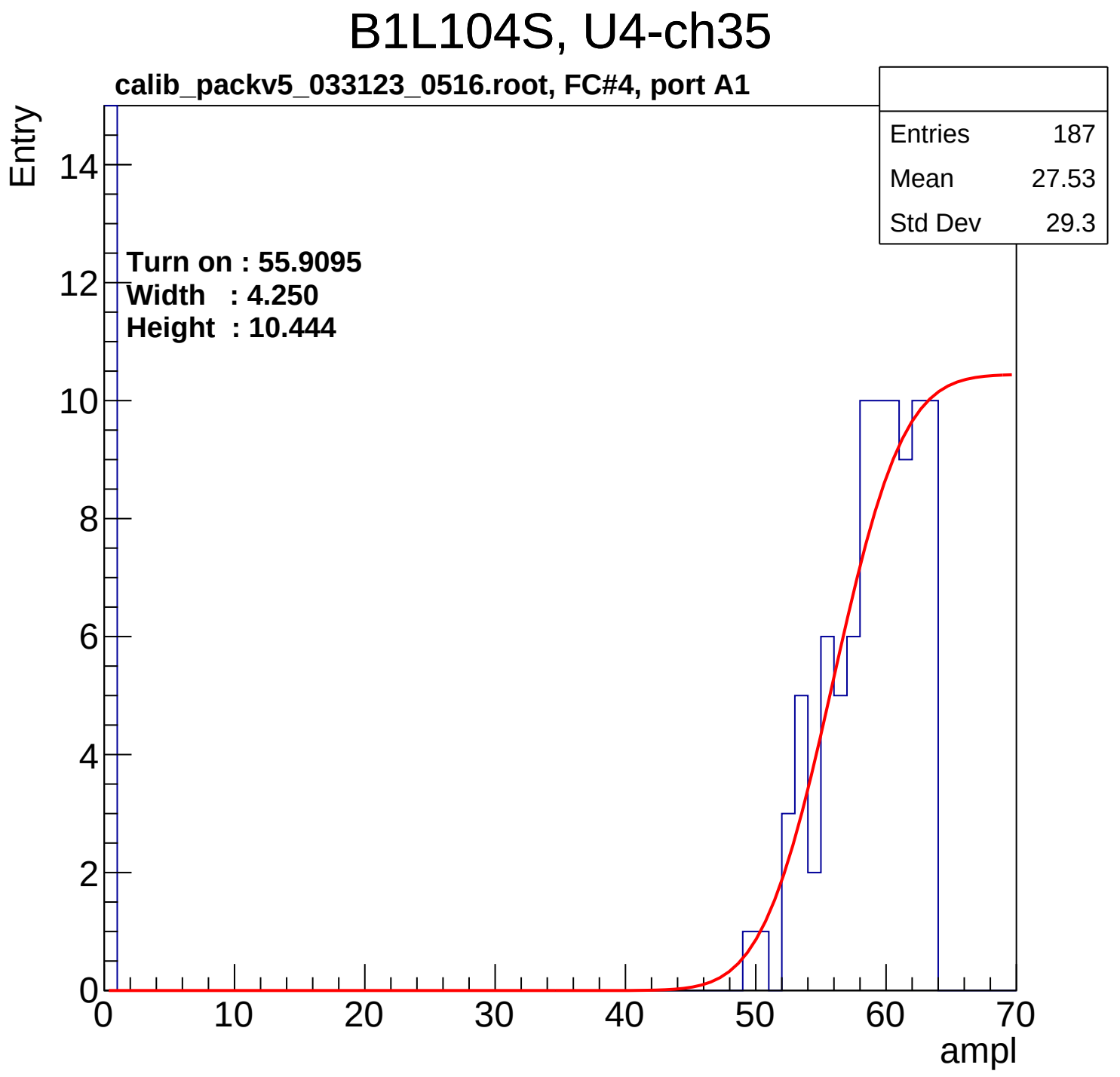

B1L104S, U4-ch30
calib_packv5_033123_0516.root, FC#4, port A1
Entries 202
Mean 37.26
Std Dev 27.05
Turn on : 50.6280
Width : 2.896
Height : 9.993
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

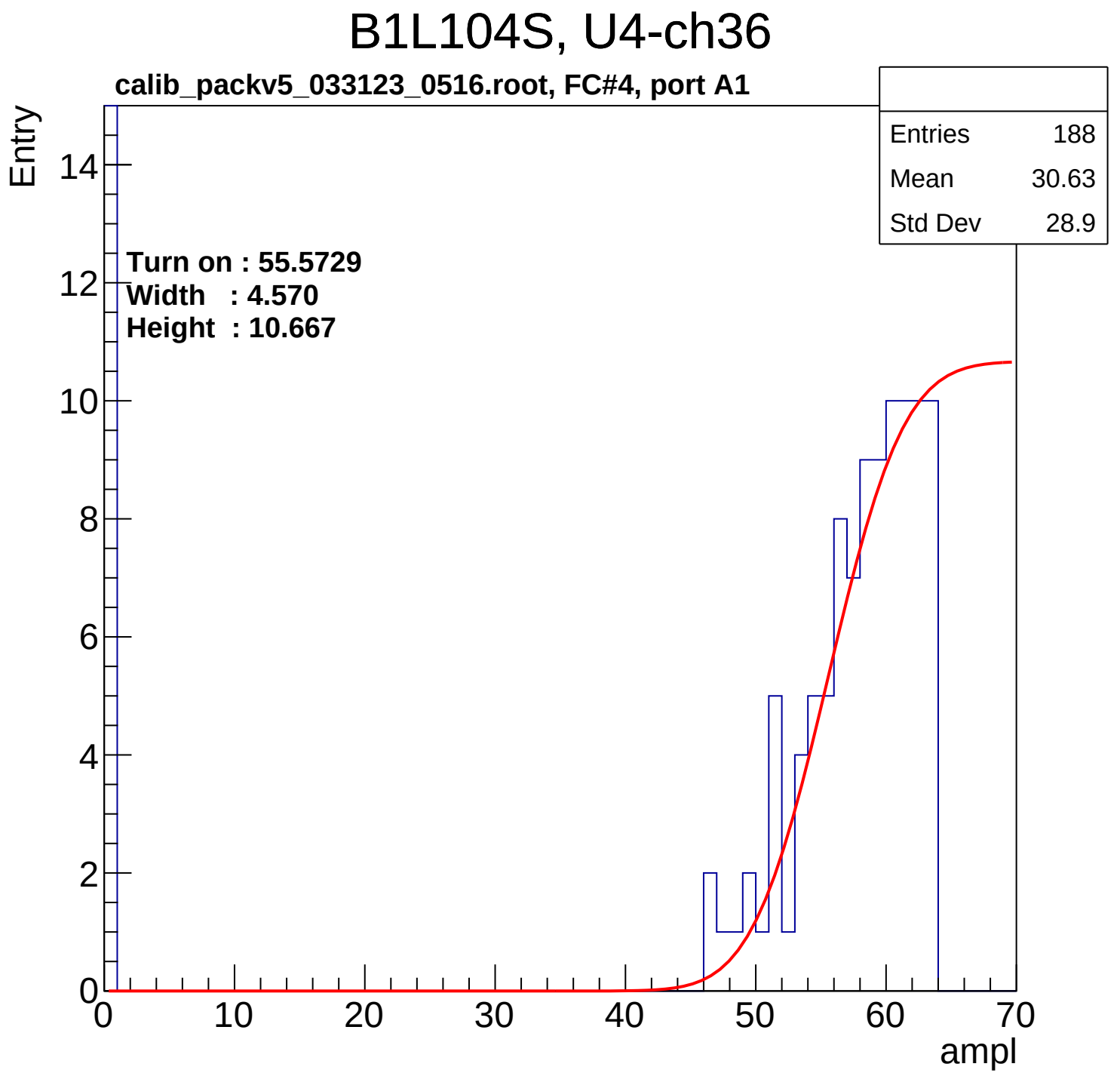

B1L104S, U4-ch31
calib_packv5_033123_0516.root, FC#4, port A1
Entries 212
Mean 28.24
Std Dev 29.14
Turn on : 54.1388
Width : 2.751
Height : 10.358
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

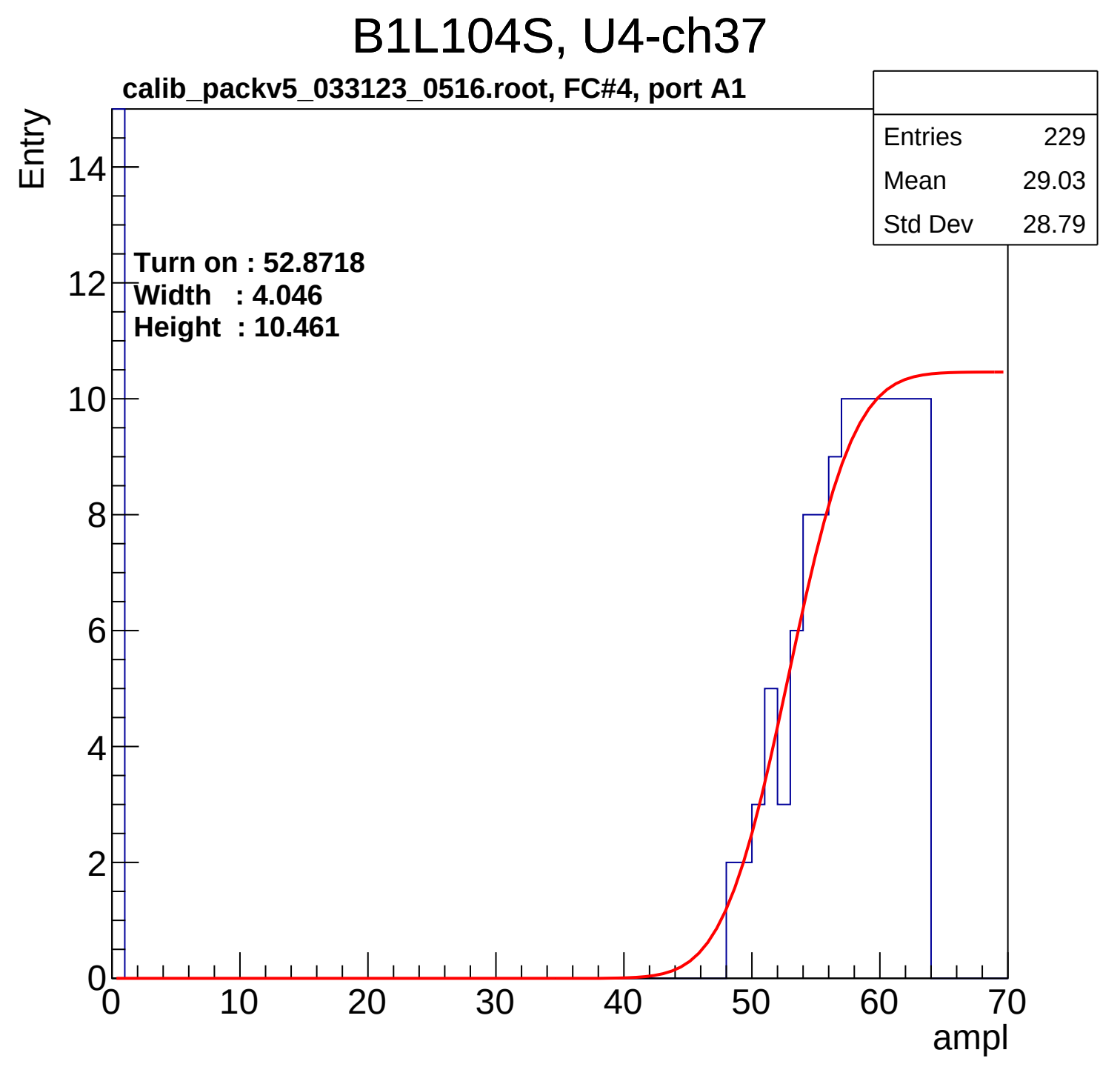

B1L104S, U4-ch32
calib_packv5_033123_0516.root, FC#4, port A1
Entries 222
Mean 27.49
Std Dev 28.88
Turn on : 53.6260
Width : 3.588
Height : 9.973
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

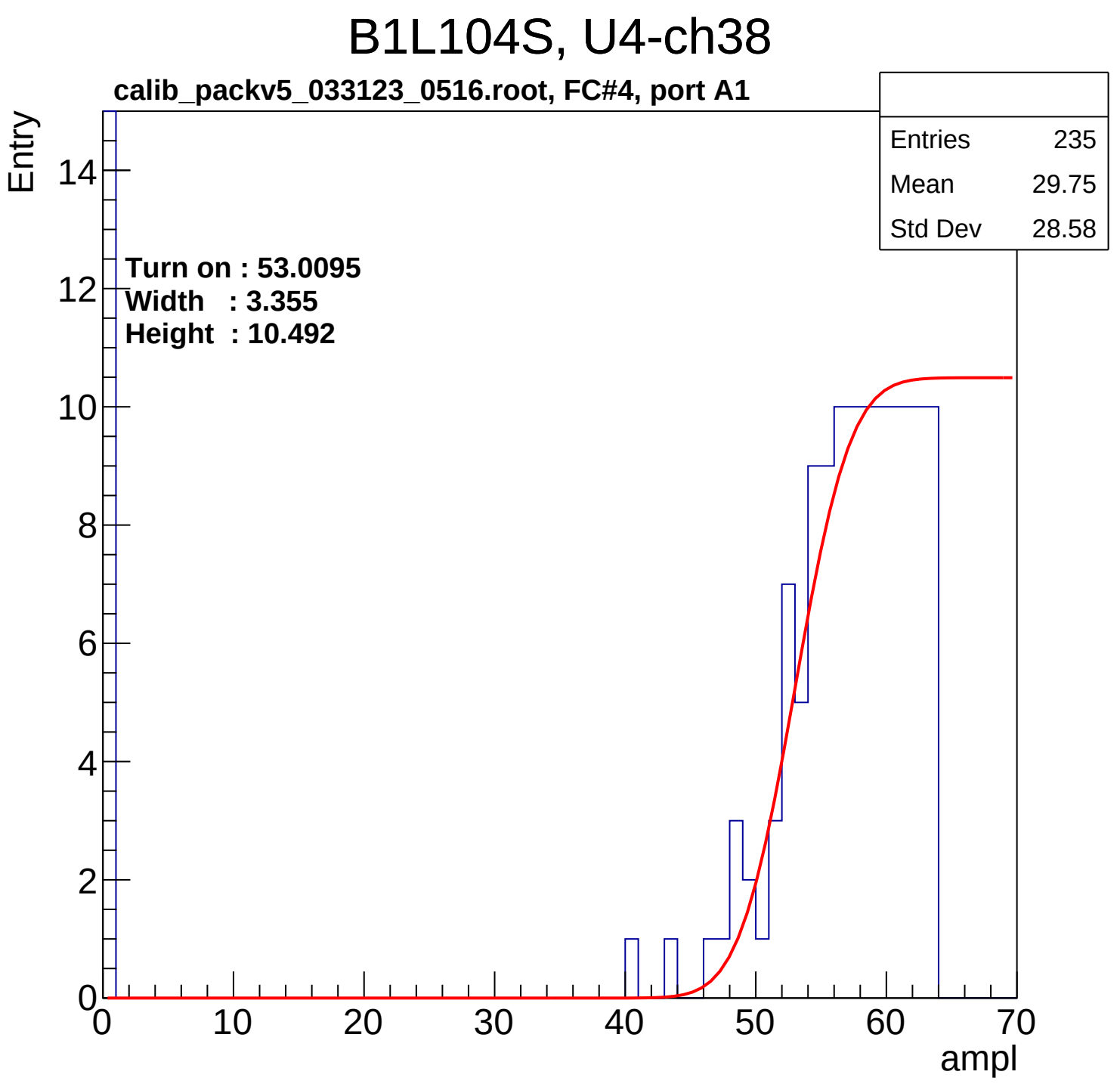

B1L104S, U4-ch33
calib_packv5_033123_0516.root, FC#4, port A1
Entries 224
Mean 28.06
Std Dev 28.94
Turn on : 53.5736
Width : 4.140
Height : 10.584
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

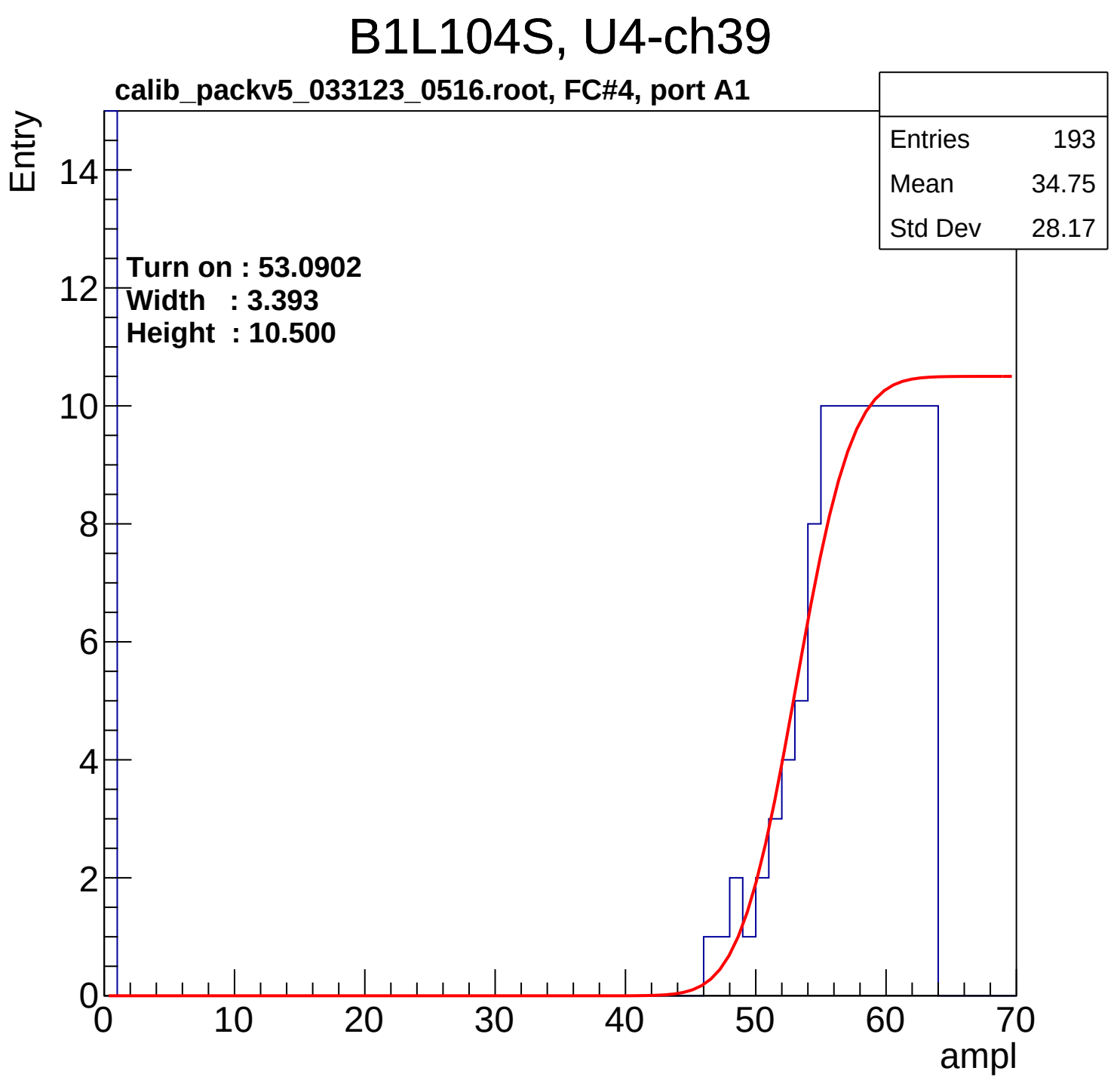

B1L104S, U4-ch34
calib_packv5_033123_0516.root, FC#4, port A1
Entries 189
Mean 32.41
Std Dev 28.81
Turn on : 54.1739
Width : 3.941
Height : 10.644
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

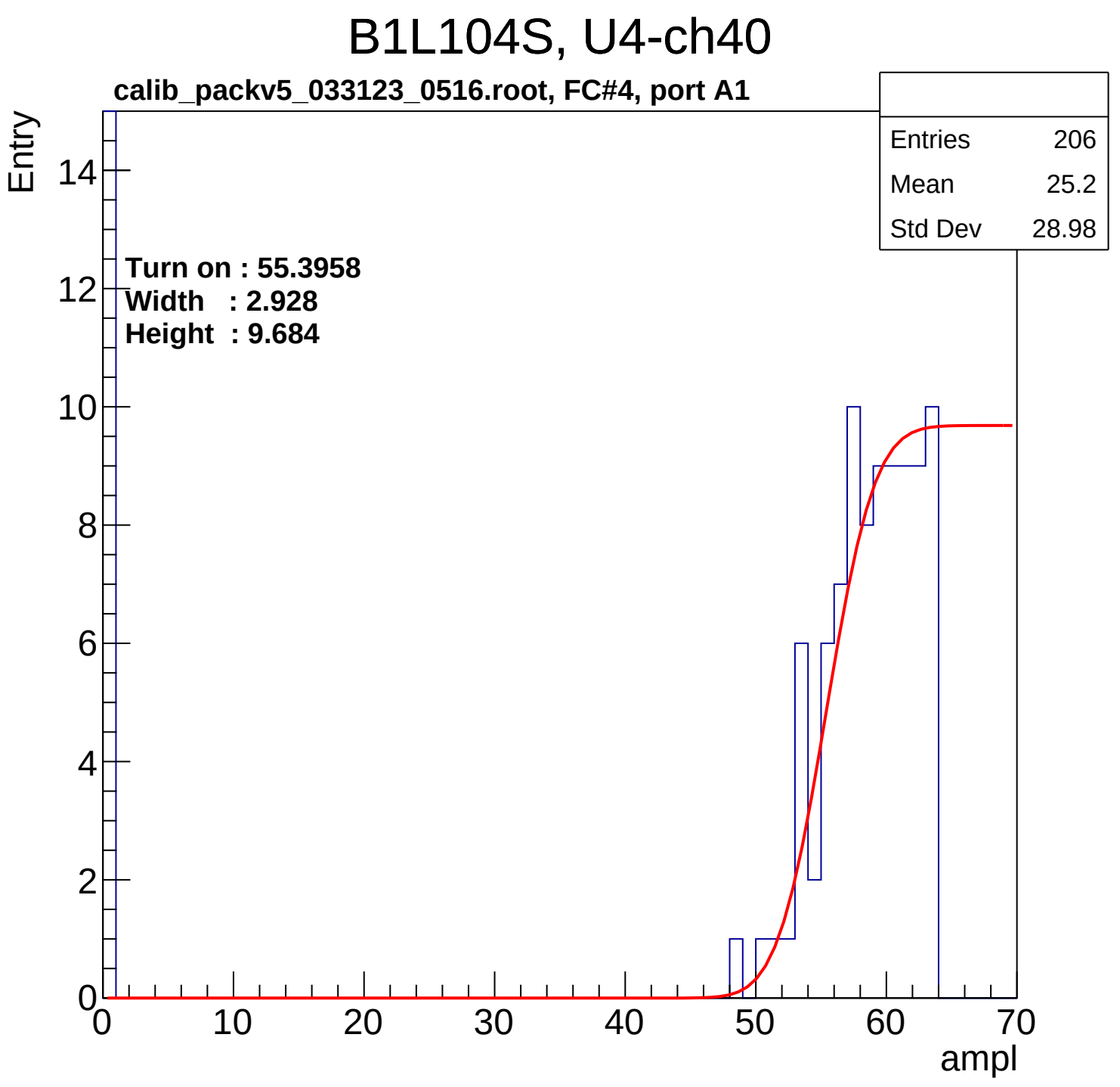

B1L104S, U4-ch35
calib_packv5_033123_0516.root, FC#4, port A1
Entries 187
Mean 27.53
Std Dev 29.3
Turn on : 55.9095
Width : 4.250
Height : 10.444
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

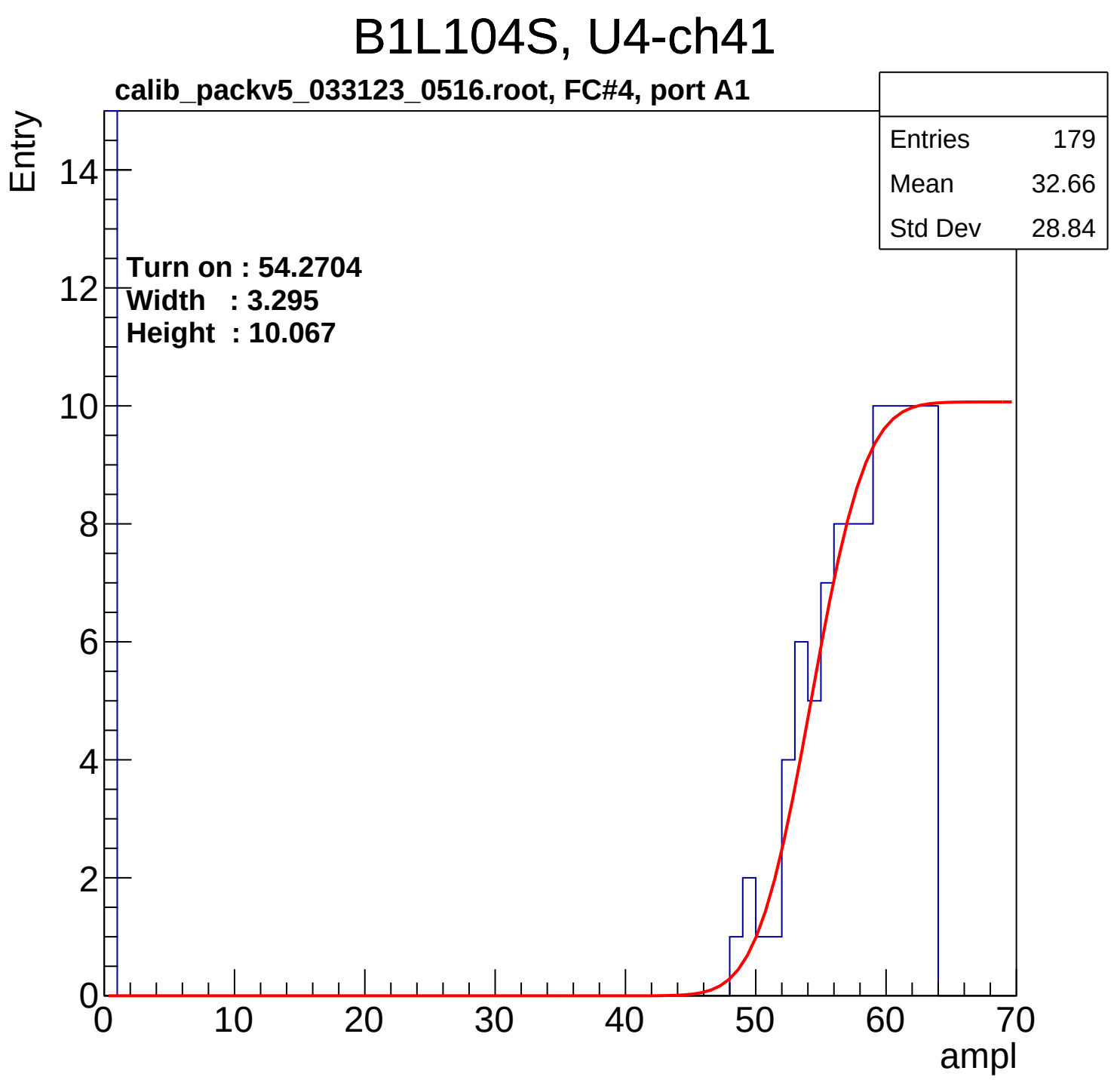

B1L104S, U4-ch36
calib_packv5_033123_0516.root, FC#4, port A1
Entries 188
Mean 30.63
Std Dev 28.9
Turn on : 55.5729
Width : 4.570
Height : 10.667
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

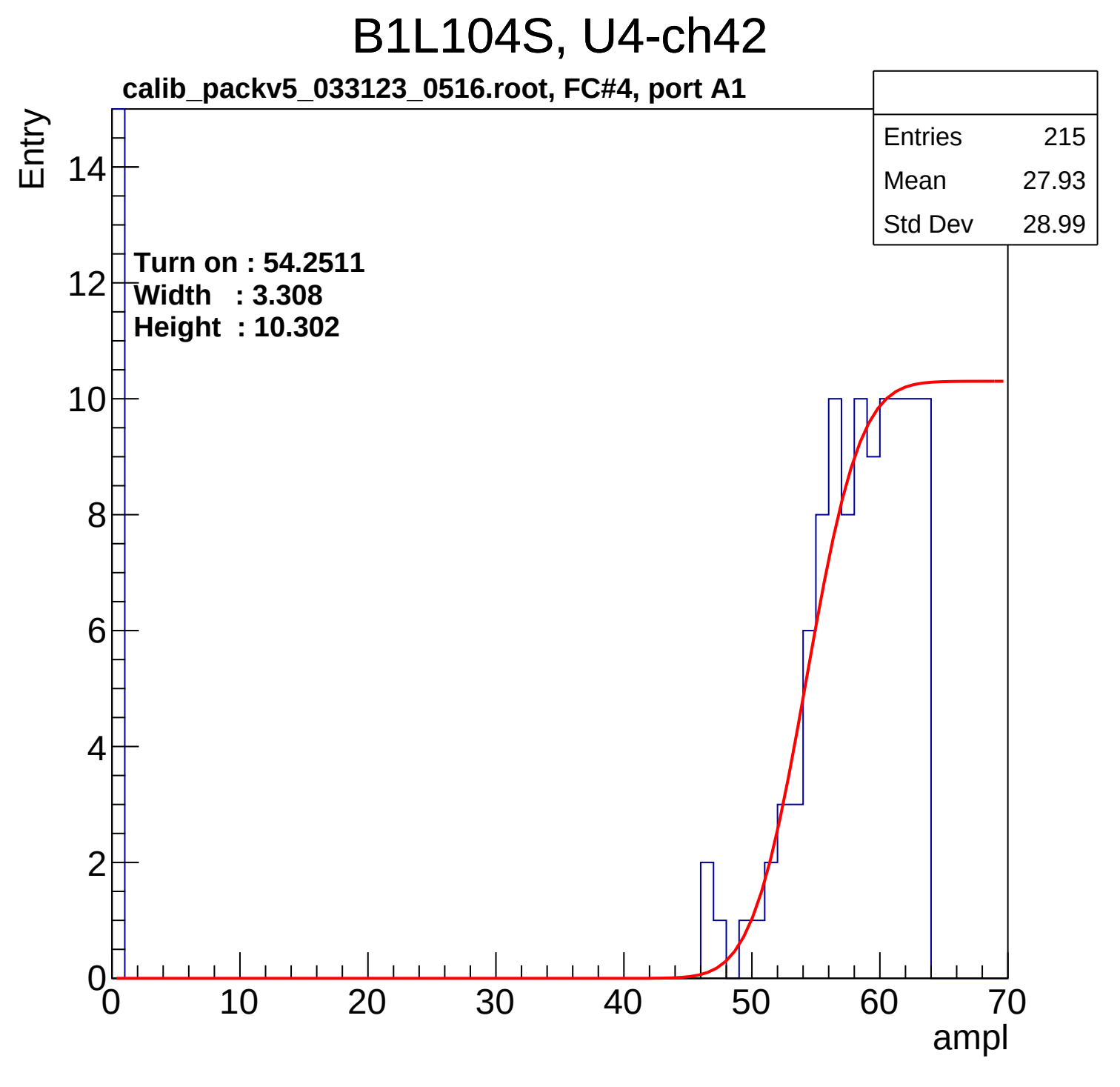

B1L104S, U4-ch37
calib_packv5_033123_0516.root, FC#4, port A1
Entries 229
Mean 29.03
Std Dev 28.79
Turn on : 52.8718
Width : 4.046
Height : 10.461
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

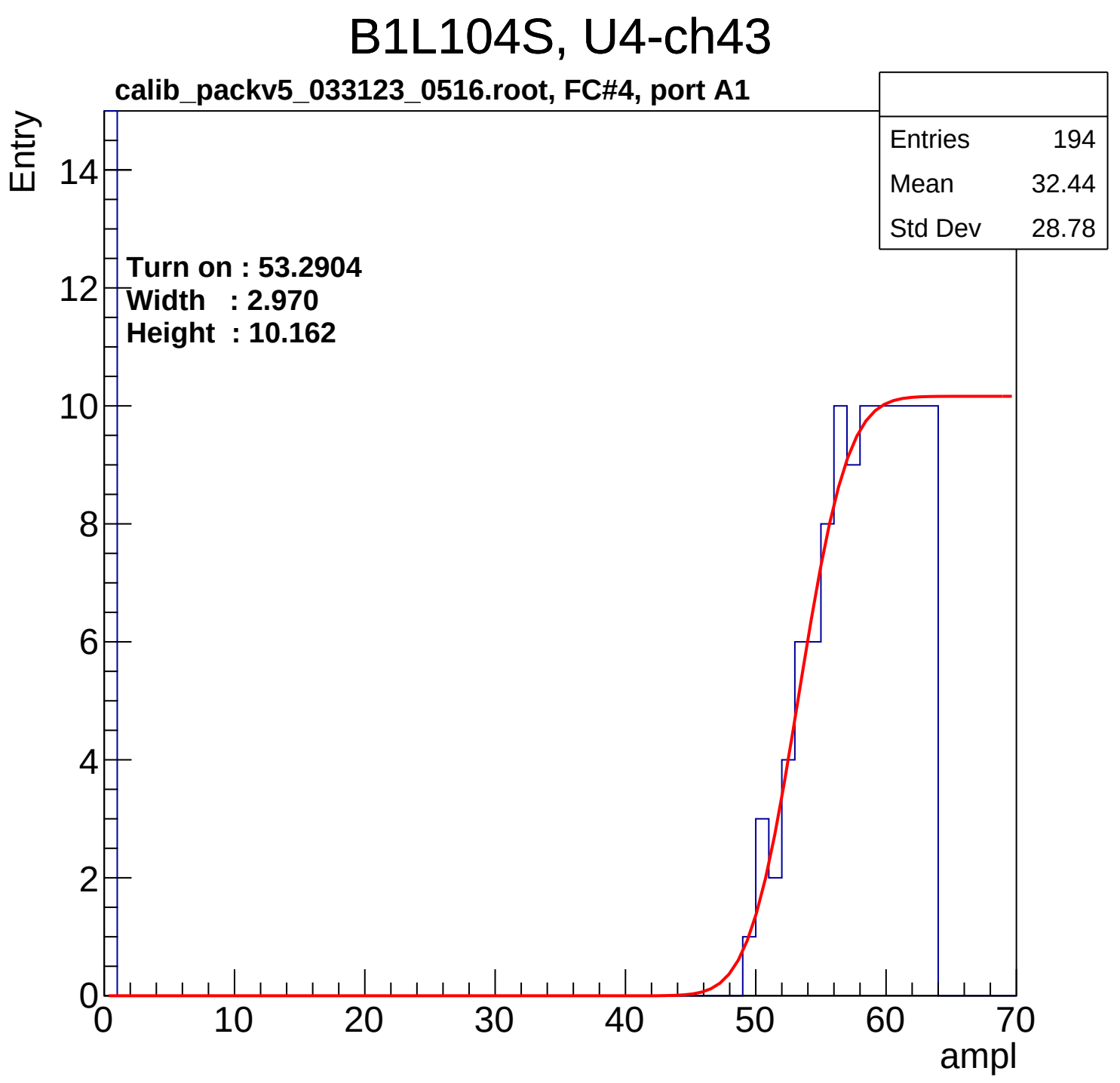

B1L104S, U4-ch38
calib_packv5_033123_0516.root, FC#4, port A1
Entries 235
Mean 29.75
Std Dev 28.58
Turn on : 53.0095
Width : 3.355
Height : 10.492
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

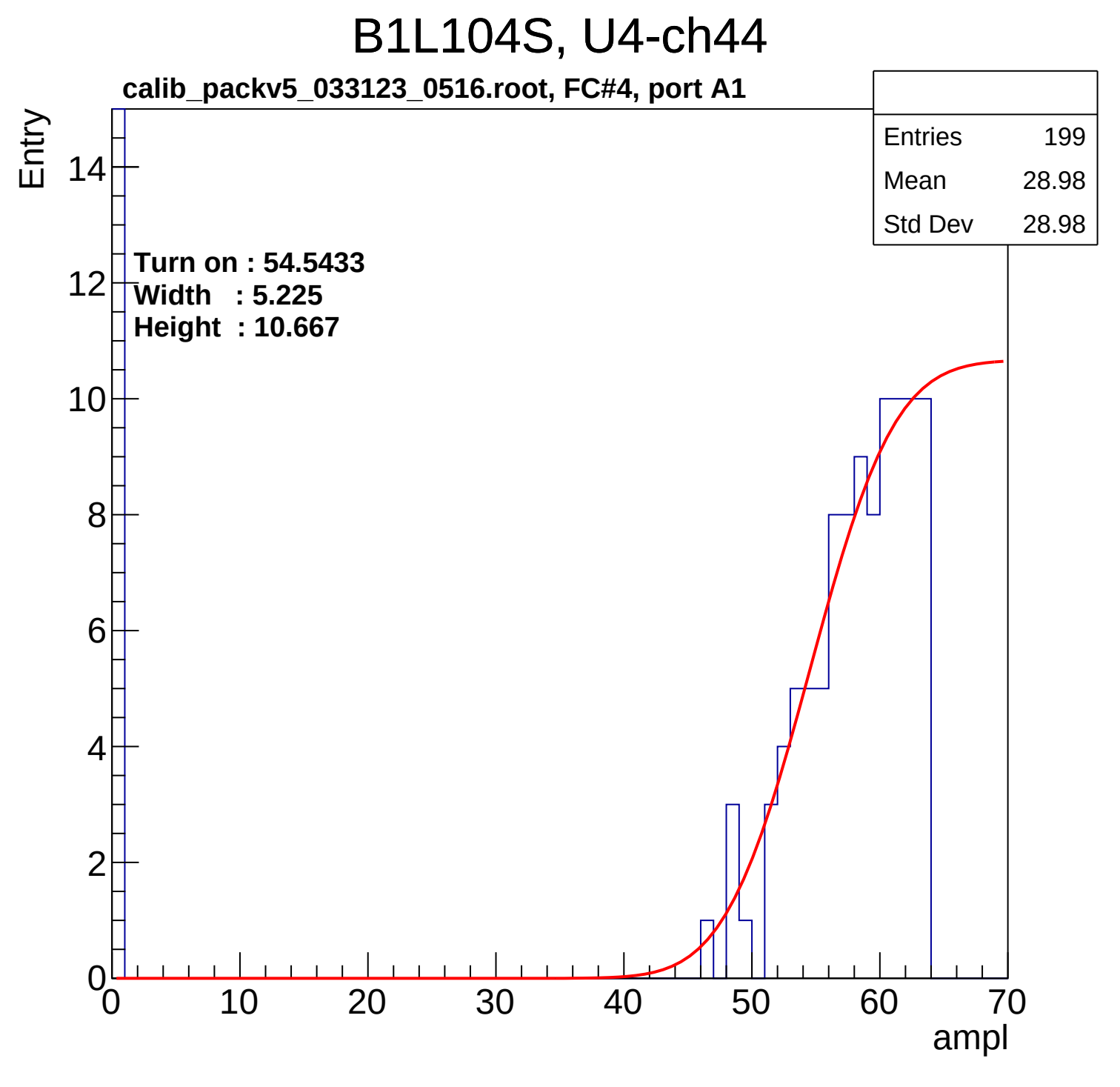

B1L104S, U4-ch39
calib_packv5_033123_0516.root, FC#4, port A1
Entries 193
Mean 34.75
Std Dev 28.17
Turn on : 53.0902
Width : 3.393
Height : 10.500
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

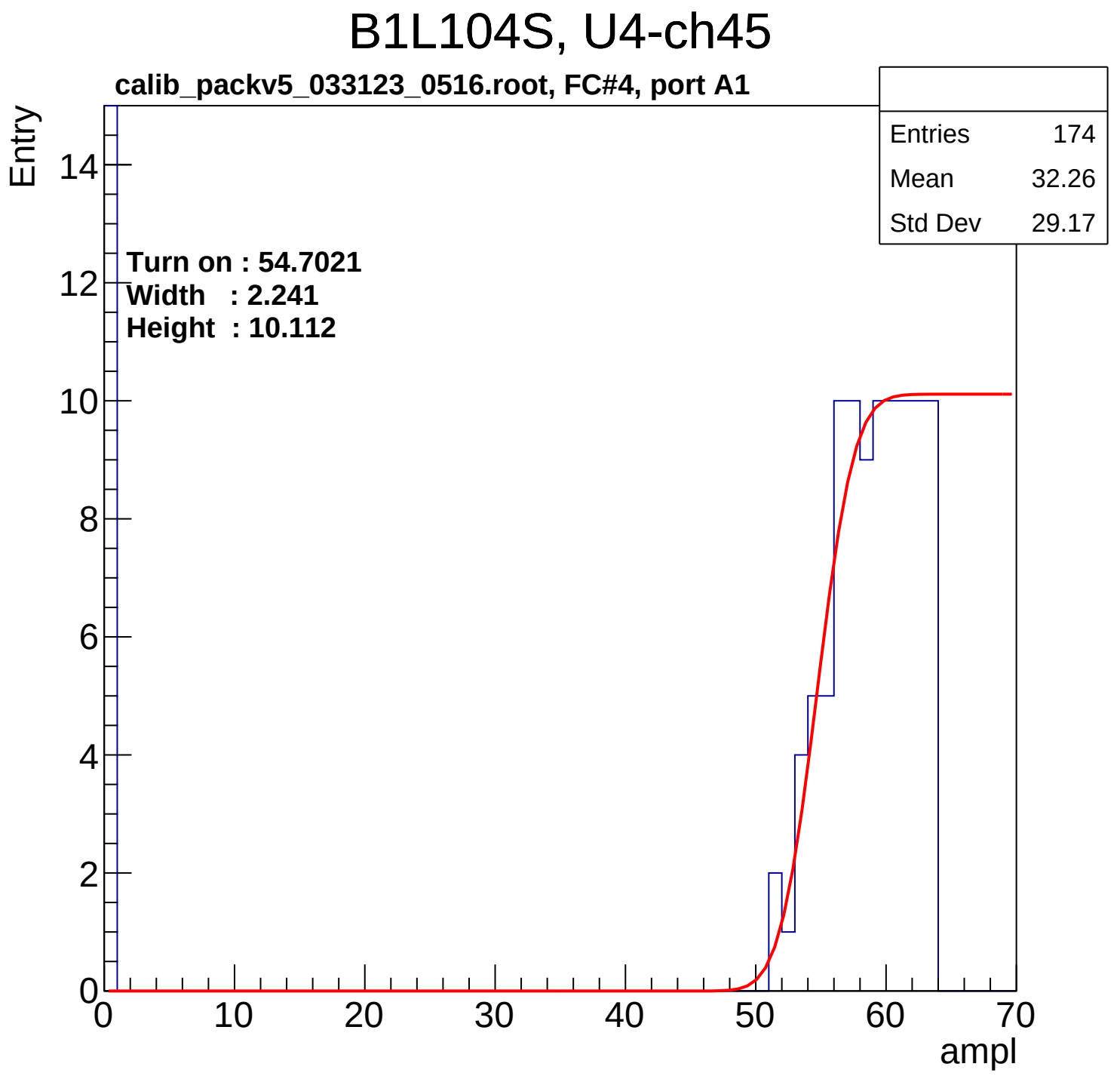

B1L104S, U4-ch40
calib_packv5_033123_0516.root, FC#4, port A1
Entries 206
Mean 25.2
Std Dev 28.98
Turn on : 55.3958
Width : 2.928
Height : 9.684
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

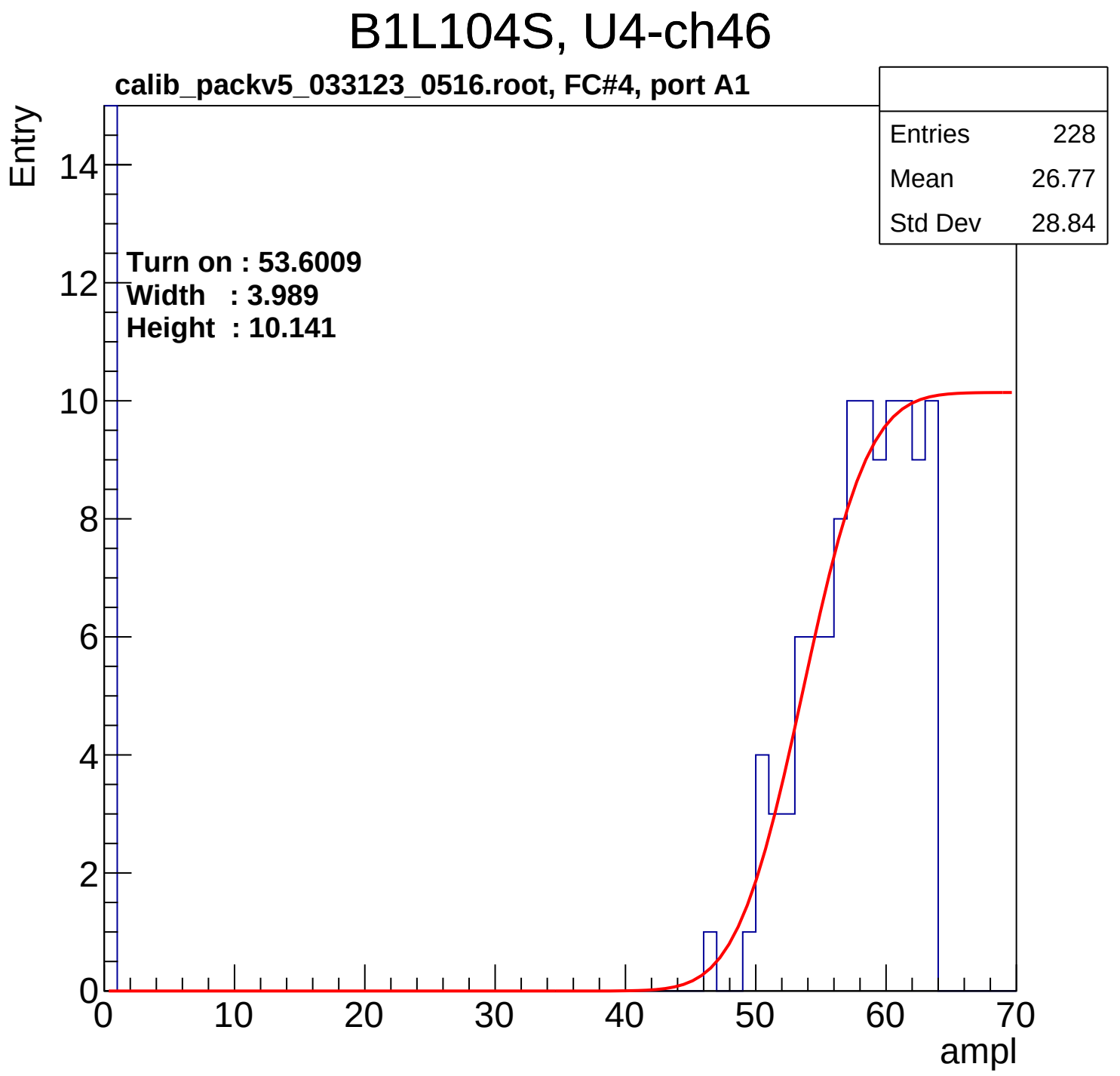

B1L104S, U4-ch41
calib_packv5_033123_0516.root, FC#4, port A1
Entries 179
Mean 32.66
Std Dev 28.84
Turn on : 54.2704
Width : 3.295
Height : 10.067
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

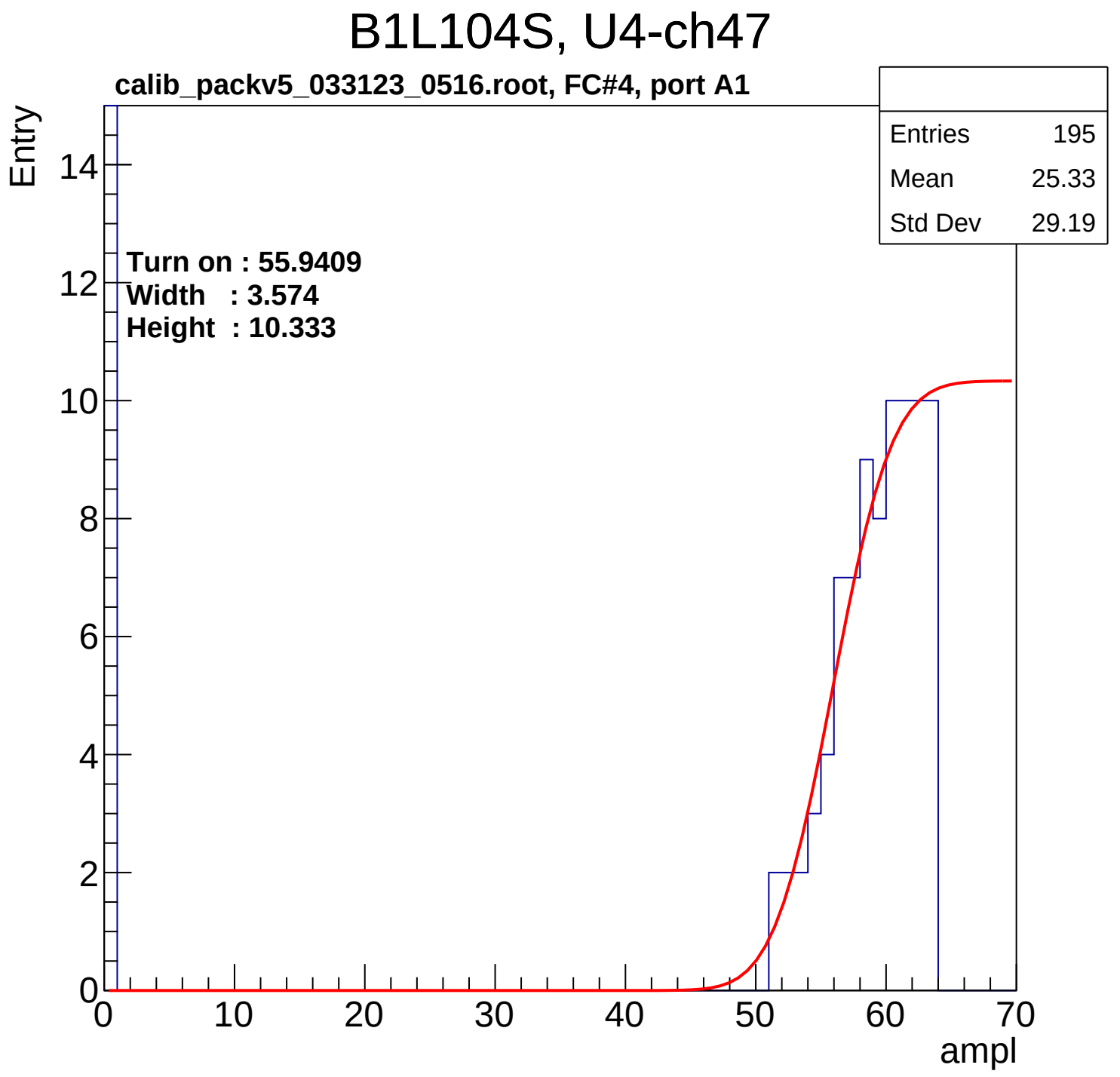

B1L104S, U4-ch42
calib_packv5_033123_0516.root, FC#4, port A1
Entries 215
Mean 27.93
Std Dev 28.99
Turn on : 54.2511
Width : 3.308
Height : 10.302
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

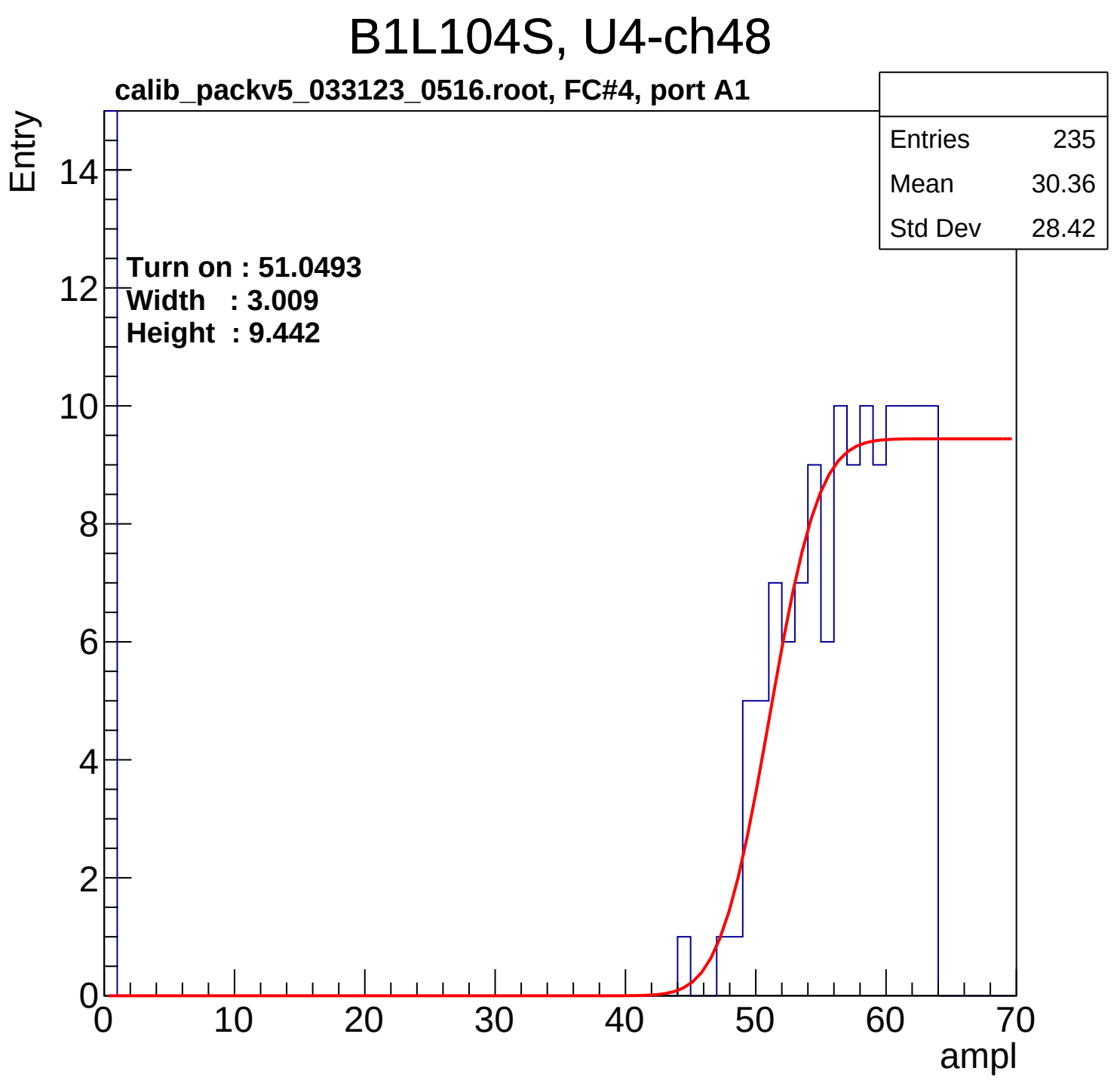

B1L104S, U4-ch43
calib_packv5_033123_0516.root, FC#4, port A1
Entries 194
Mean 32.44
Std Dev 28.78
Turn on : 53.2904
Width : 2.970
Height : 10.162
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

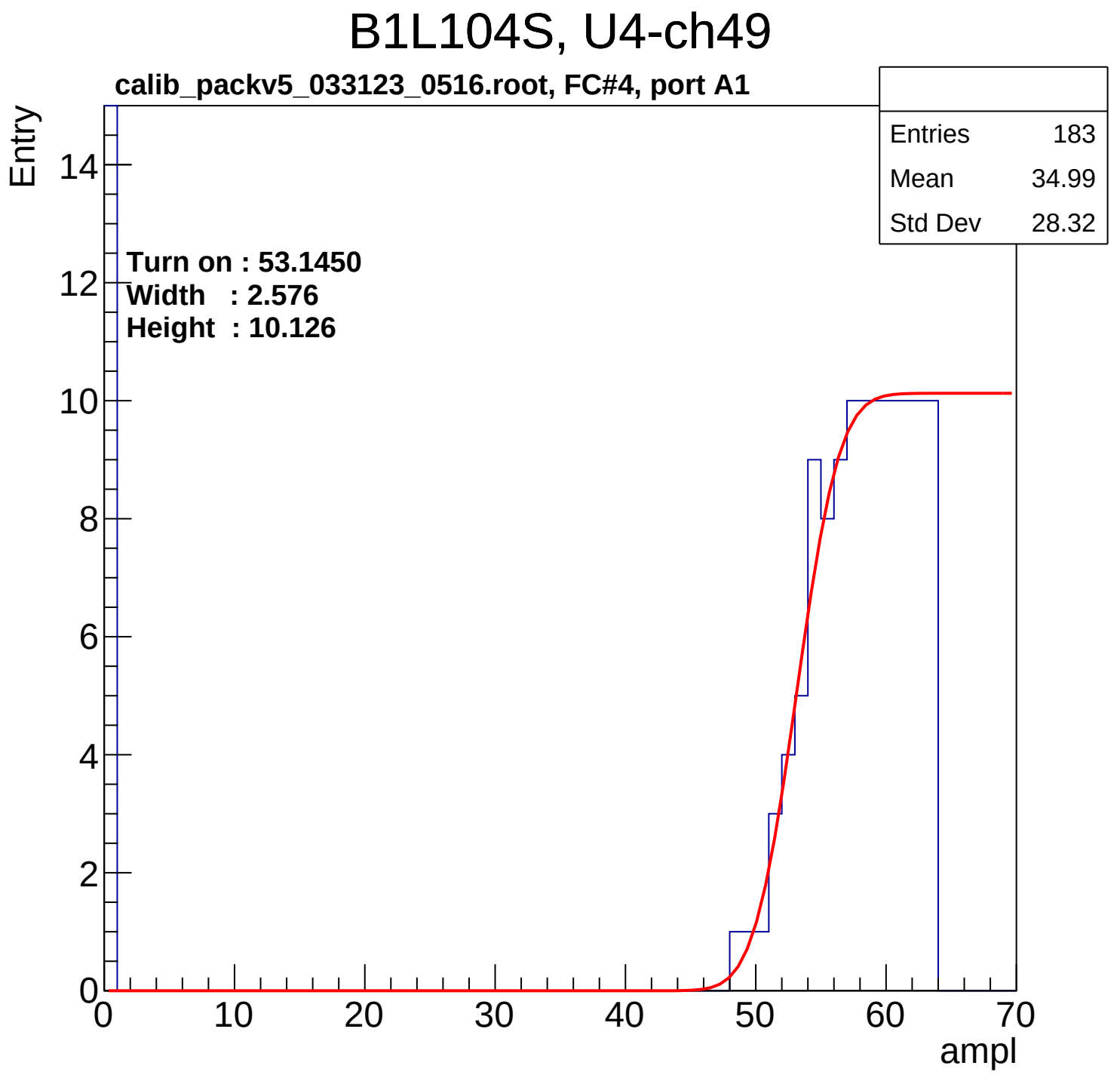

B1L104S, U4-ch44
calib_packv5_033123_0516.root, FC#4, port A1
Entries 199
Mean 28.98
Std Dev 28.98
Turn on : 54.5433
Width : 5.225
Height : 10.667
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

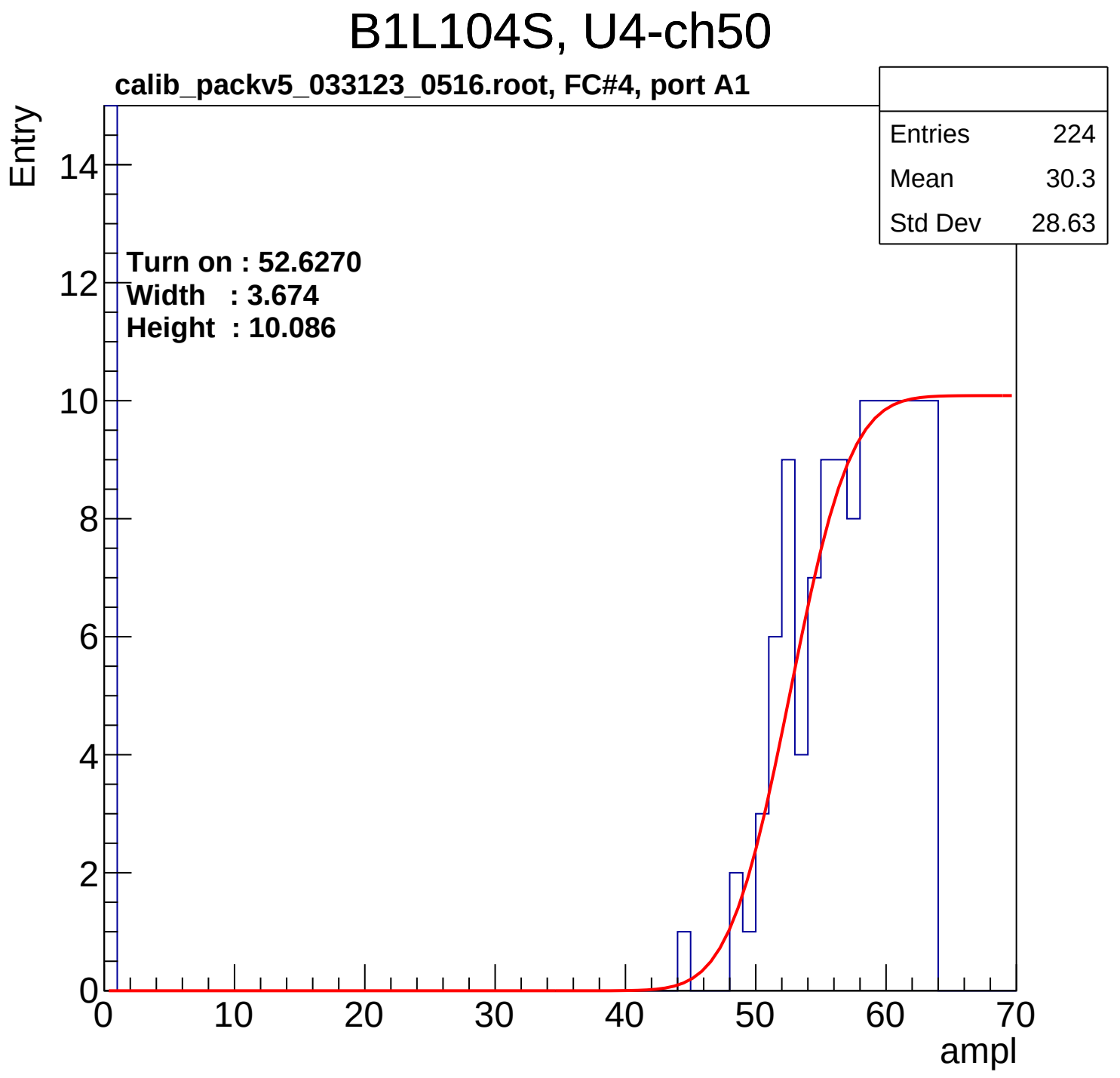

B1L104S, U4-ch45
calib_packv5_033123_0516.root, FC#4, port A1
Entries 174
Mean 32.26
Std Dev 29.17
Turn on : 54.7021
Width : 2.241
Height : 10.112
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

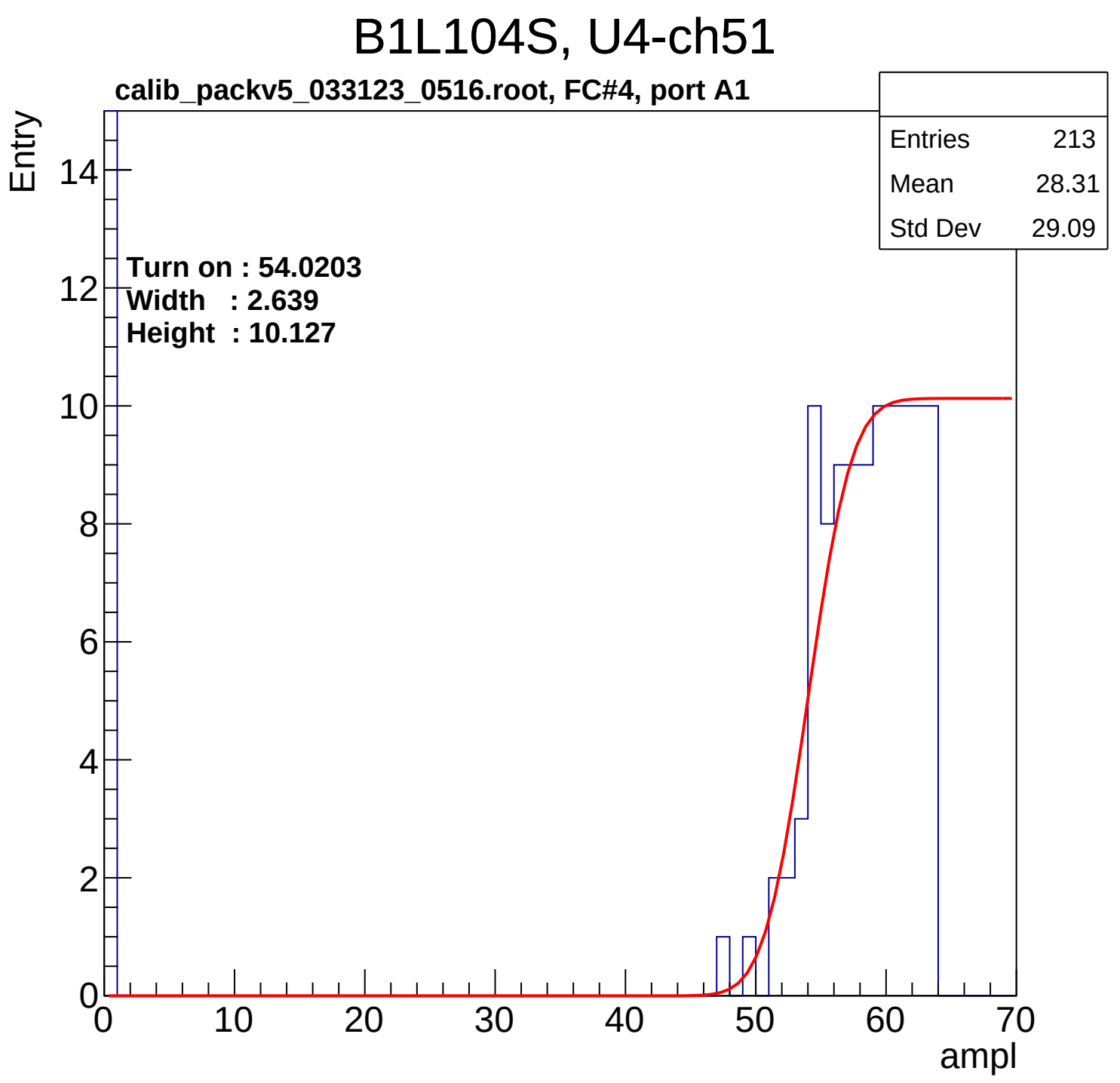

B1L104S, U4-ch46
calib_packv5_033123_0516.root, FC#4, port A1
Entries 228
Mean 26.77
Std Dev 28.84
Turn on : 53.6009
Width : 3.989
Height : 10.141
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

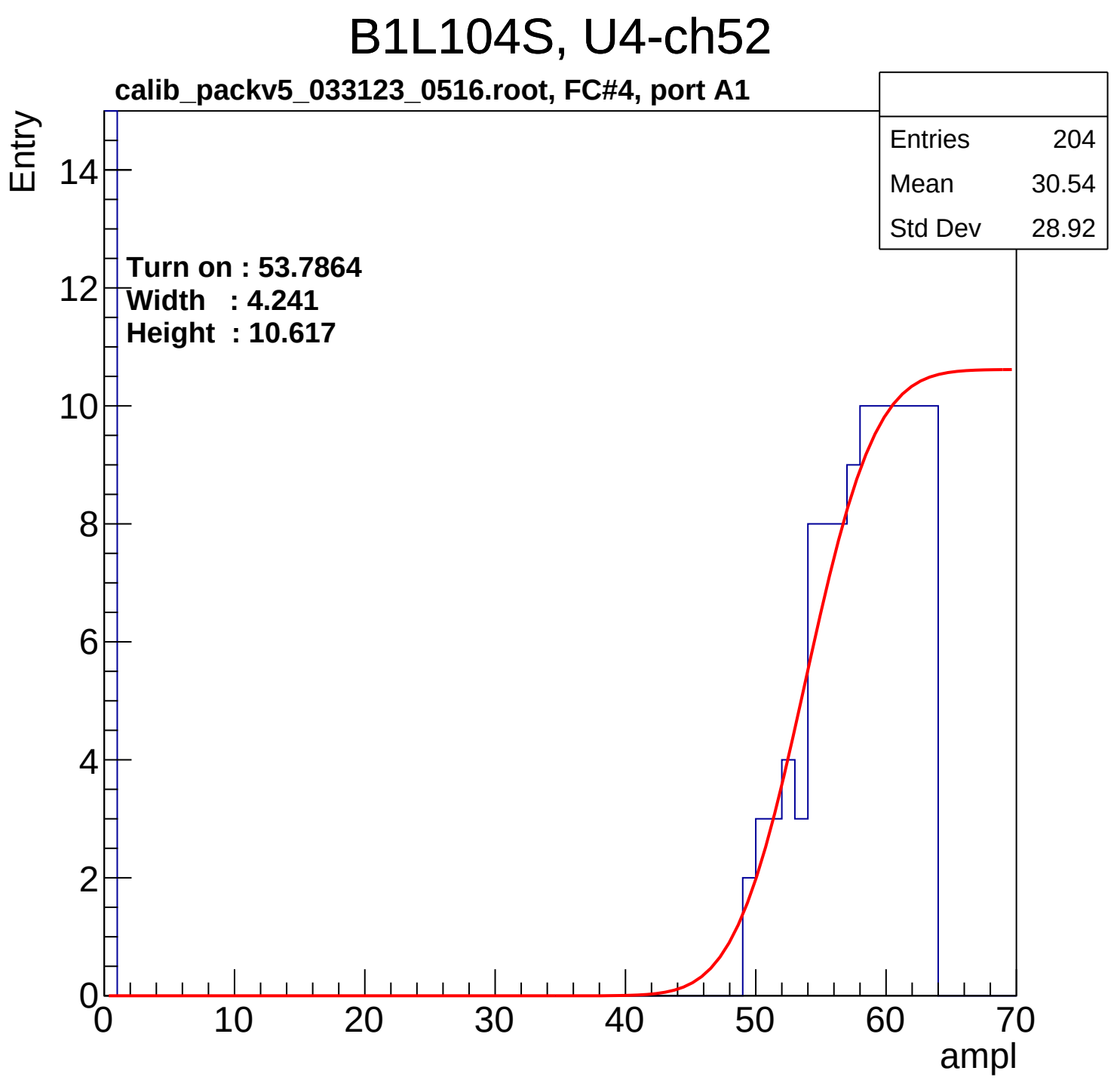

B1L104S, U4-ch47
calib_packv5_033123_0516.root, FC#4, port A1
Entries 195
Mean 25.33
Std Dev 29.19
Turn on : 55.9409
Width : 3.574
Height : 10.333
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

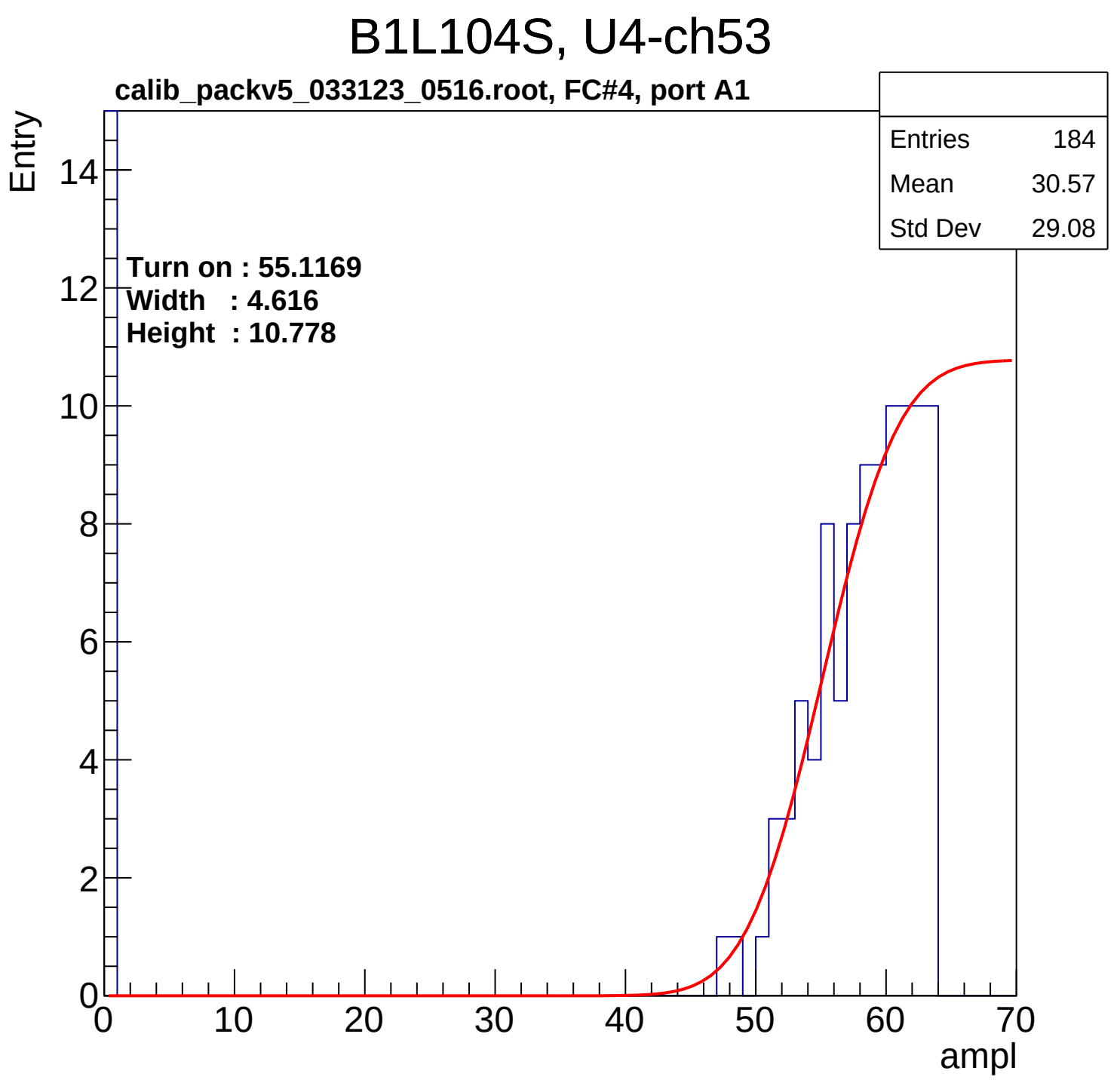

B1L104S, U4-ch48
calib_packv5_033123_0516.root, FC#4, port A1
Entries 235
Mean 30.36
Std Dev 28.42
Turn on : 51.0493
Width : 3.009
Height : 9.442
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

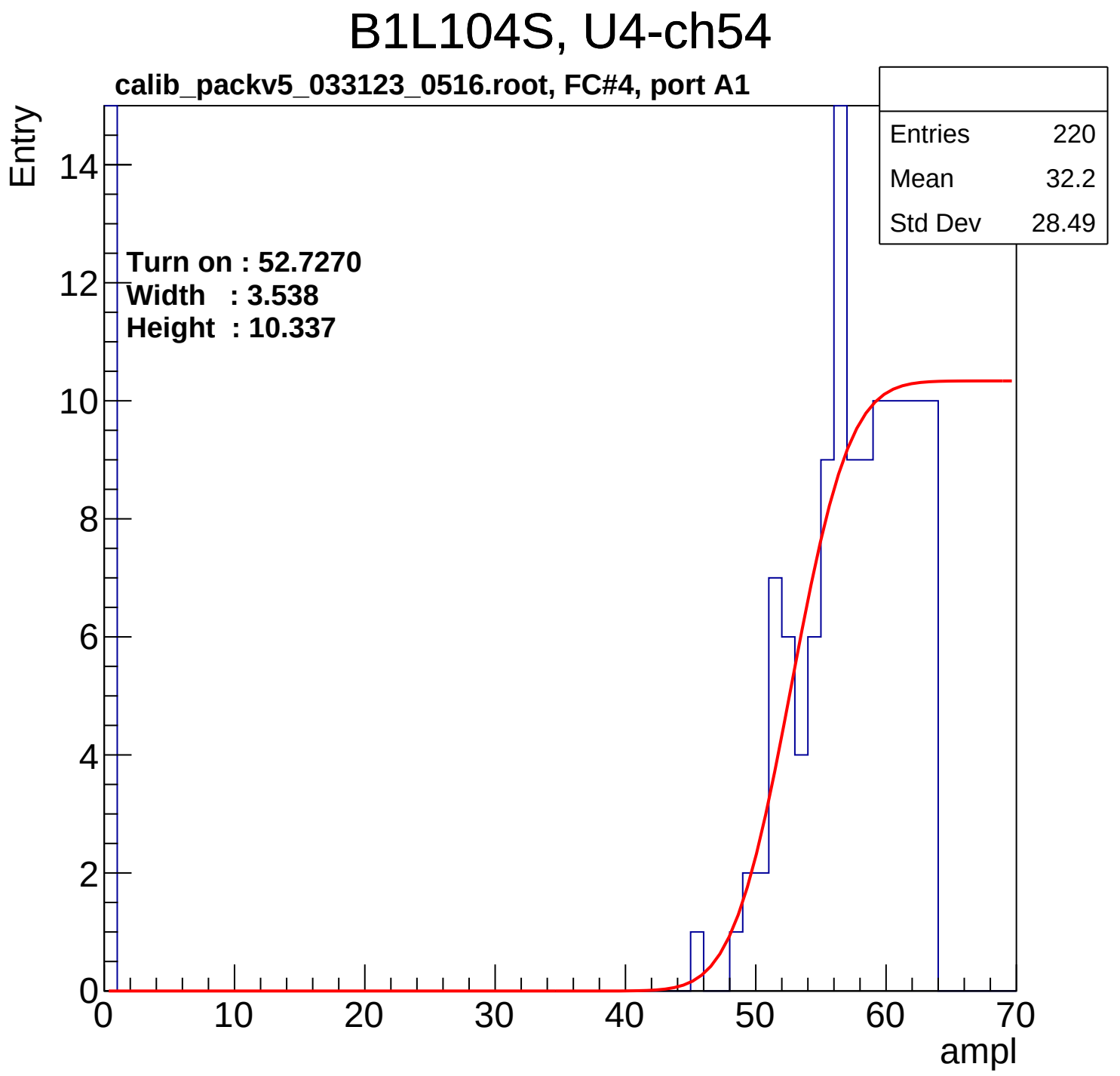

B1L104S, U4-ch49
calib_packv5_033123_0516.root, FC#4, port A1
Entries 183
Mean 34.99
Std Dev 28.32
Turn on : 53.1450
Width : 2.576
Height : 10.126
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

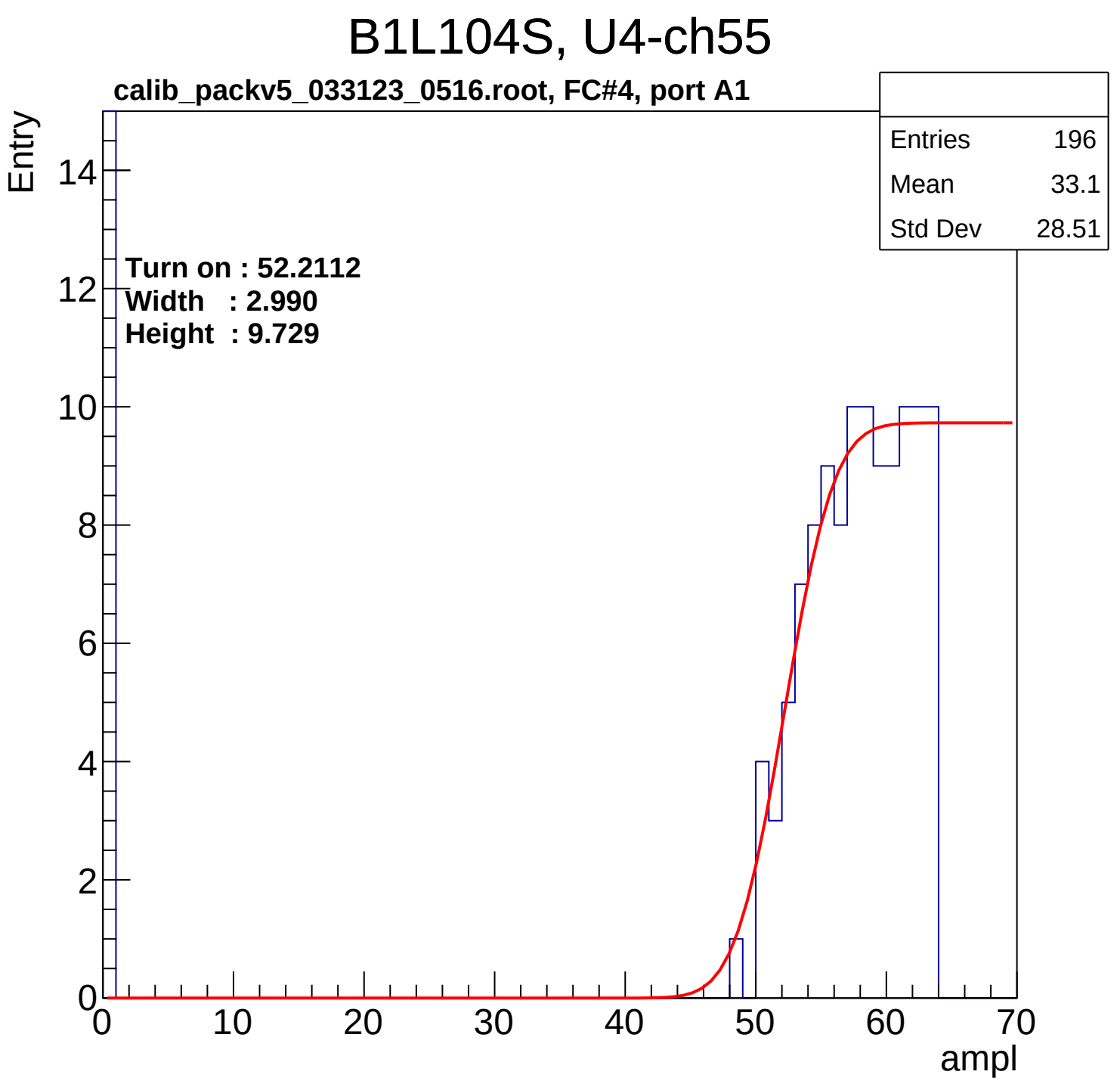

B1L104S, U4-ch50
calib_packv5_033123_0516.root, FC#4, port A1
Entries 224
Mean 30.3
Std Dev 28.63
Turn on : 52.6270
Width : 3.674
Height : 10.086
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

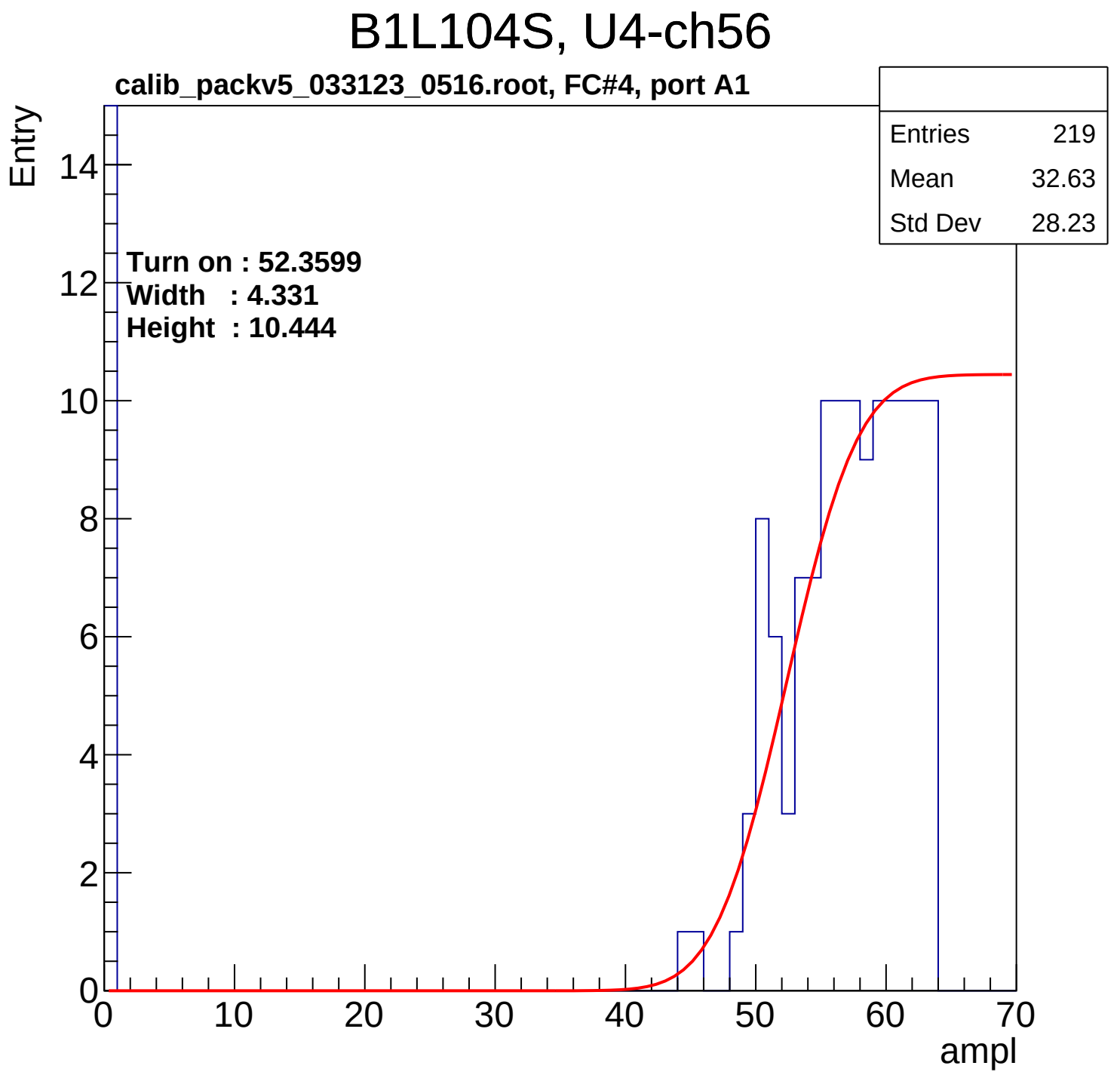

B1L104S, U4-ch51
calib_packv5_033123_0516.root, FC#4, port A1
Entries 213
Mean 28.31
Std Dev 29.09
Turn on : 54.0203
Width : 2.639
Height : 10.127
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

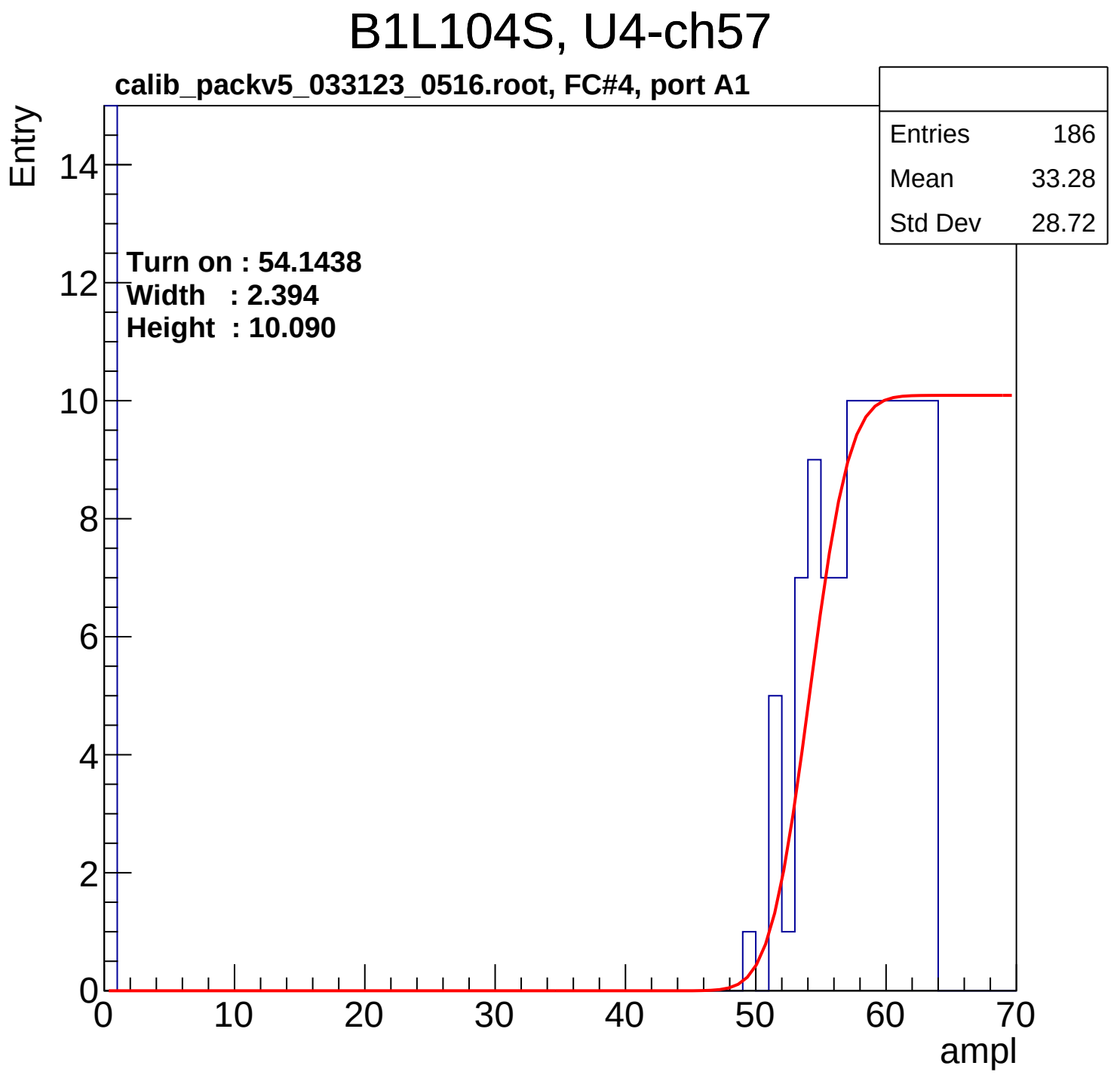

B1L104S, U4-ch52
calib_packv5_033123_0516.root, FC#4, port A1
Entries 204
Mean 30.54
Std Dev 28.92
Turn on : 53.7864
Width : 4.241
Height : 10.617
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

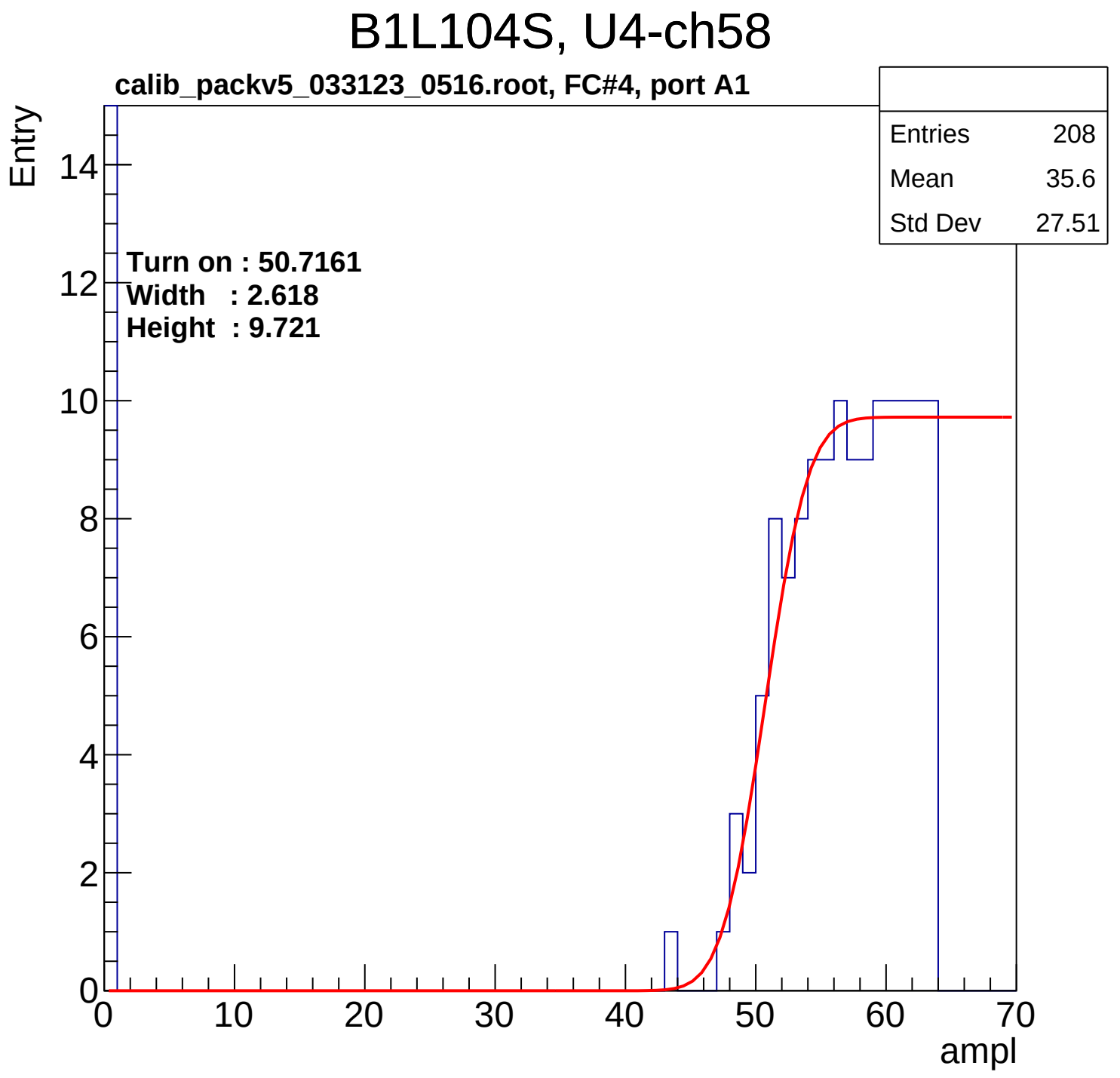

B1L104S, U4-ch53
calib_packv5_033123_0516.root, FC#4, port A1
Entries 184
Mean 30.57
Std Dev 29.08
Turn on : 55.1169
Width : 4.616
Height : 10.778
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

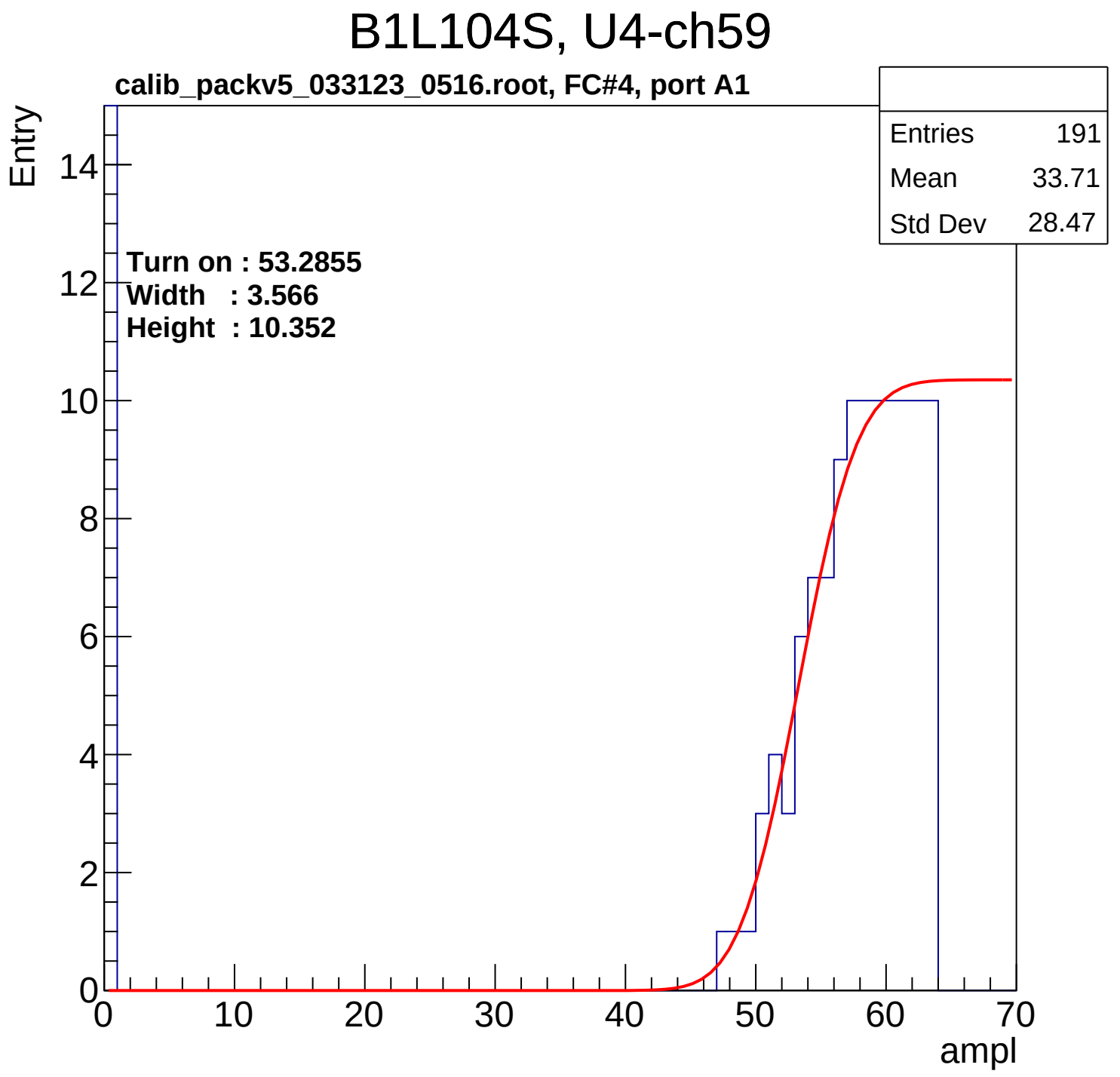

B1L104S, U4-ch54
calib_packv5_033123_0516.root, FC#4, port A1
Entries 220
Mean 32.2
Std Dev 28.49
Turn on : 52.7270
Width : 3.538
Height : 10.337
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

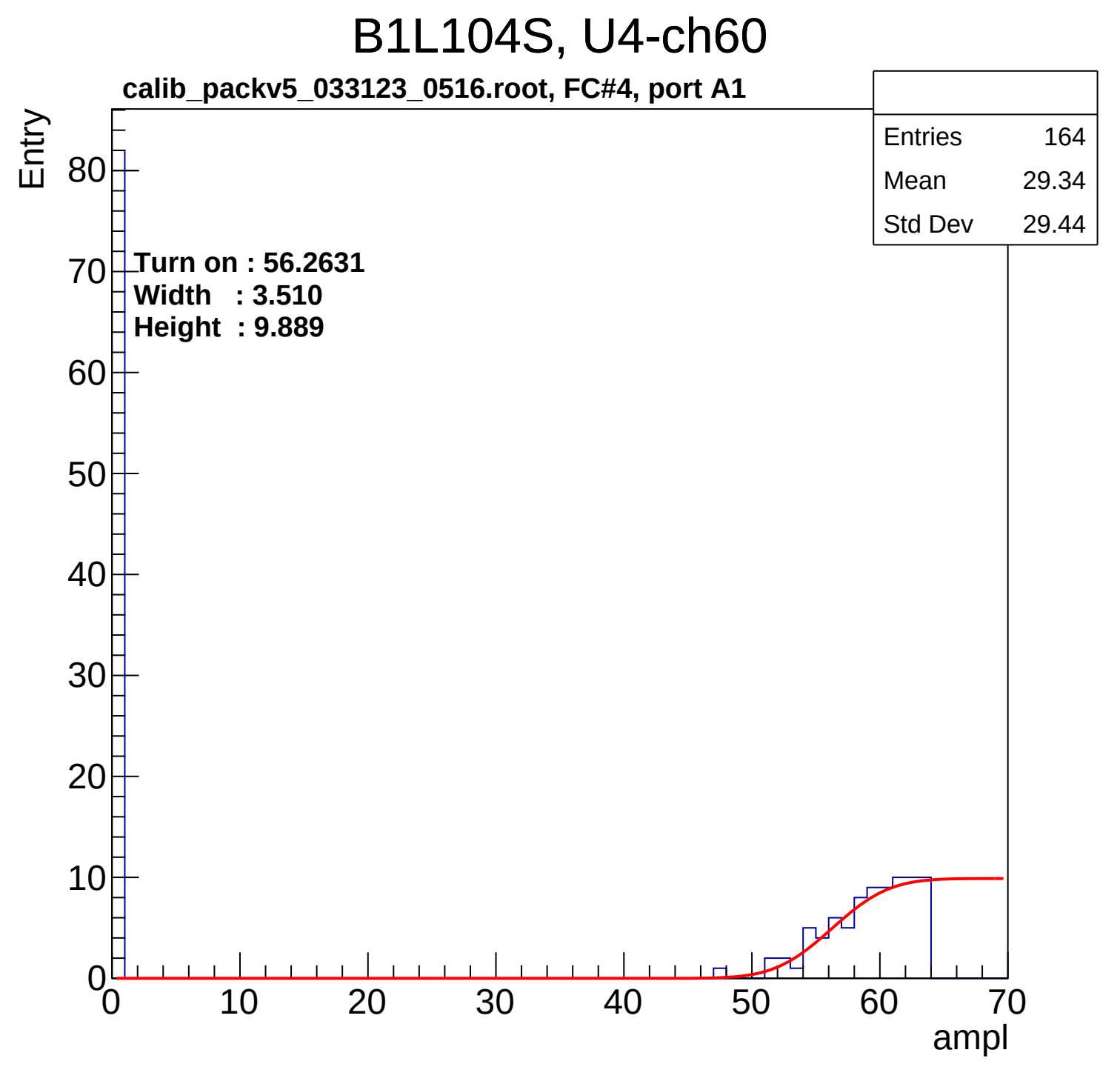

B1L104S, U4-ch55
calib_packv5_033123_0516.root, FC#4, port A1
Entries 196
Mean 33.1
Std Dev 28.51
Turn on : 52.2112
Width : 2.990
Height : 9.729
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

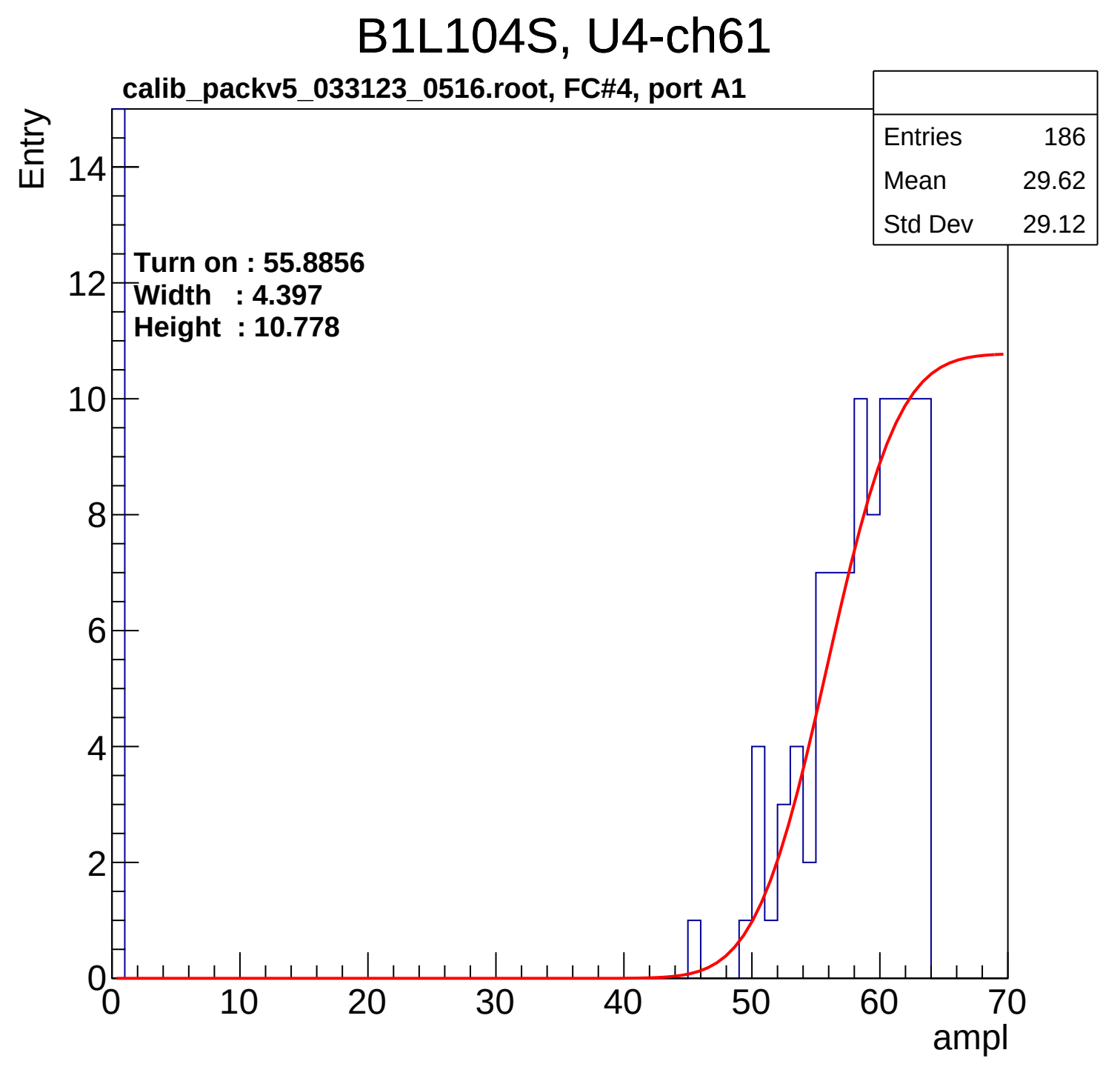

B1L104S, U4-ch56
calib_packv5_033123_0516.root, FC#4, port A1
Entries 219
Mean 32.63
Std Dev 28.23
Turn on : 52.3599
Width : 4.331
Height : 10.444
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

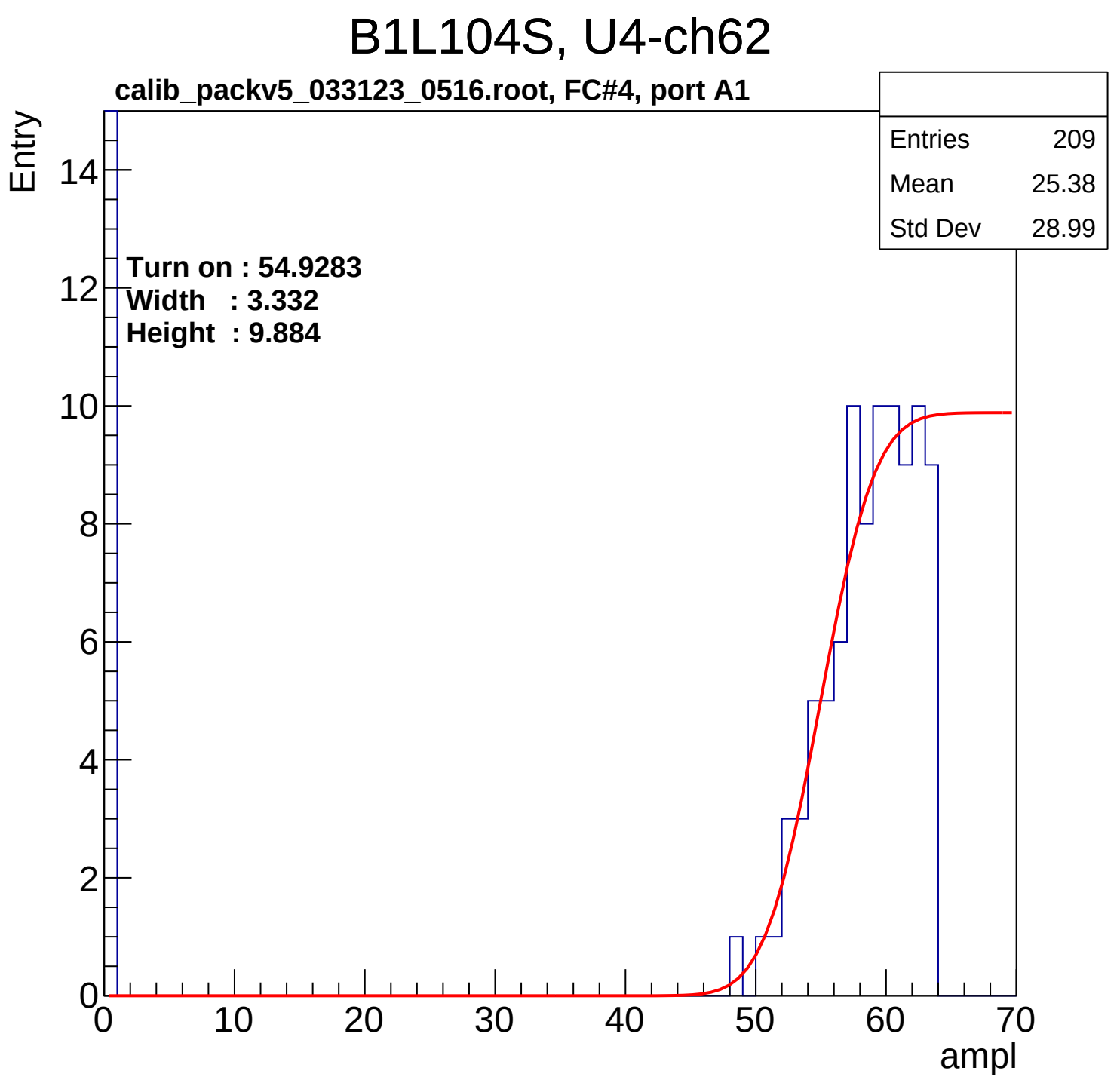

B1L104S, U4-ch57
calib_packv5_033123_0516.root, FC#4, port A1
Entries 186
Mean 33.28
Std Dev 28.72
Turn on : 54.1438
Width : 2.394
Height : 10.090
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

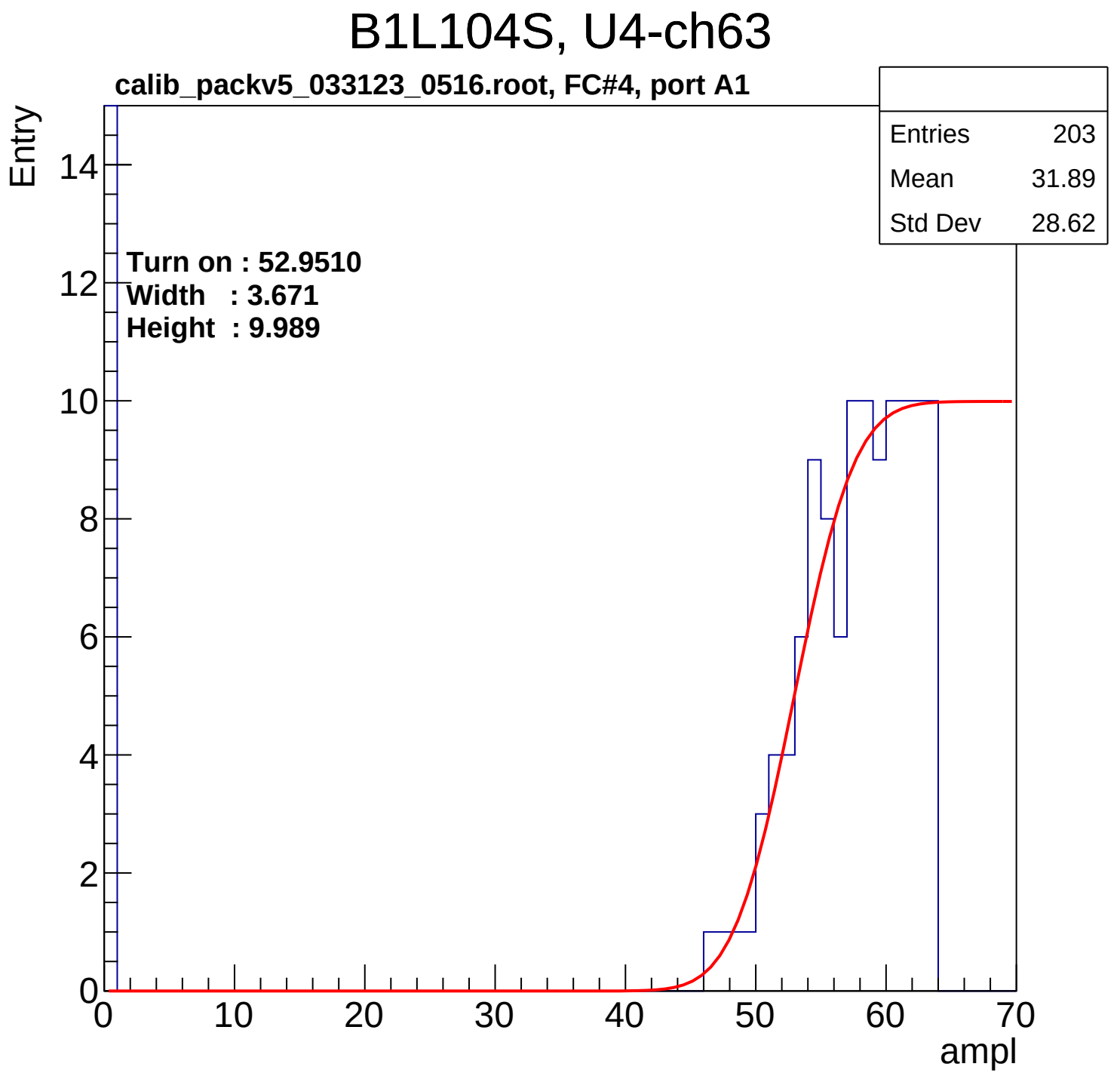

B1L104S, U4-ch58
calib_packv5_033123_0516.root, FC#4, port A1
Entries 208
Mean 35.6
Std Dev 27.51
Turn on : 50.7161
Width : 2.618
Height : 9.721
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

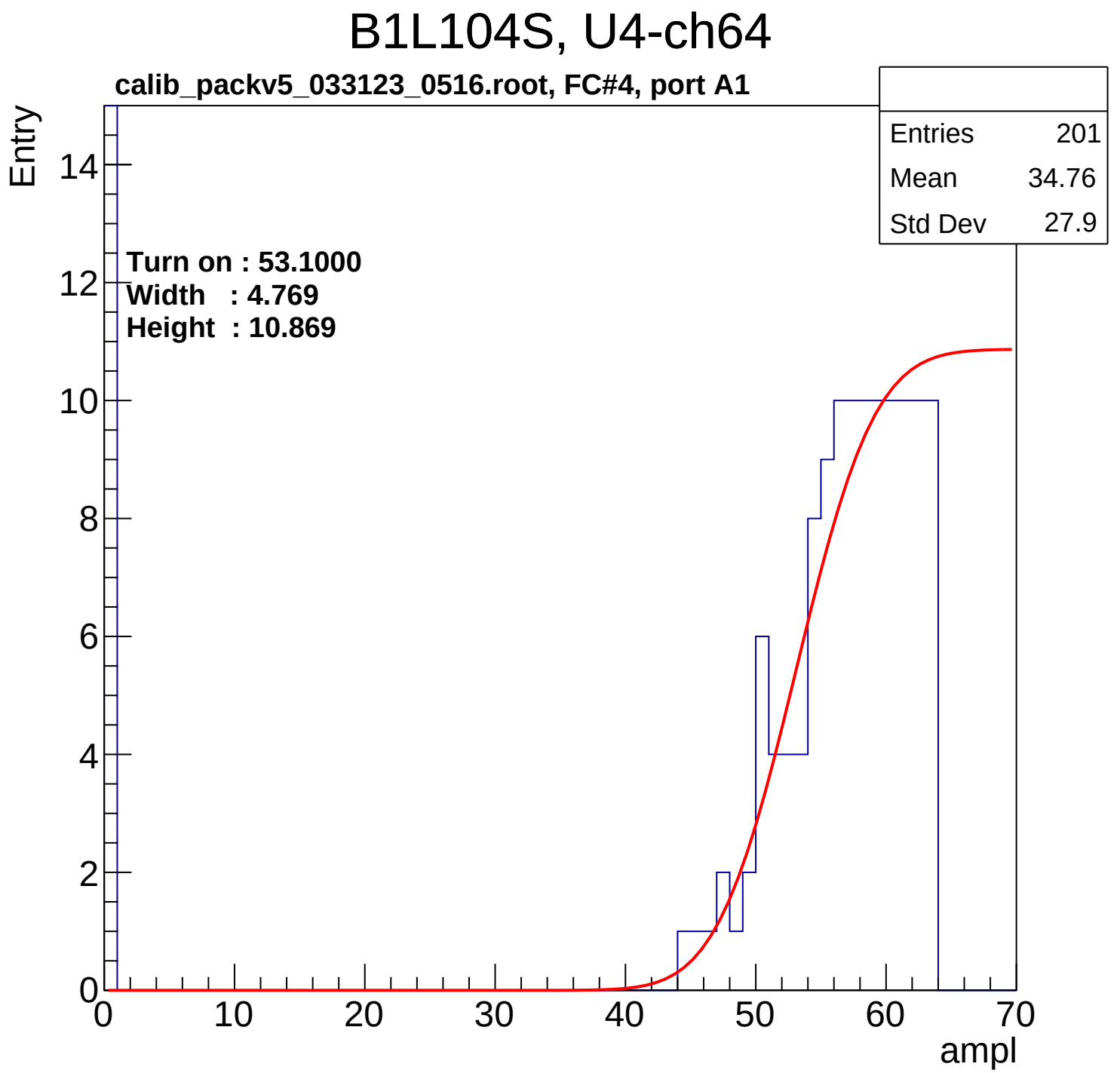

B1L104S, U4-ch59
calib_packv5_033123_0516.root, FC#4, port A1
Entries 191
Mean 33.71
Std Dev 28.47
Turn on : 53.2855
Width : 3.566
Height : 10.352
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

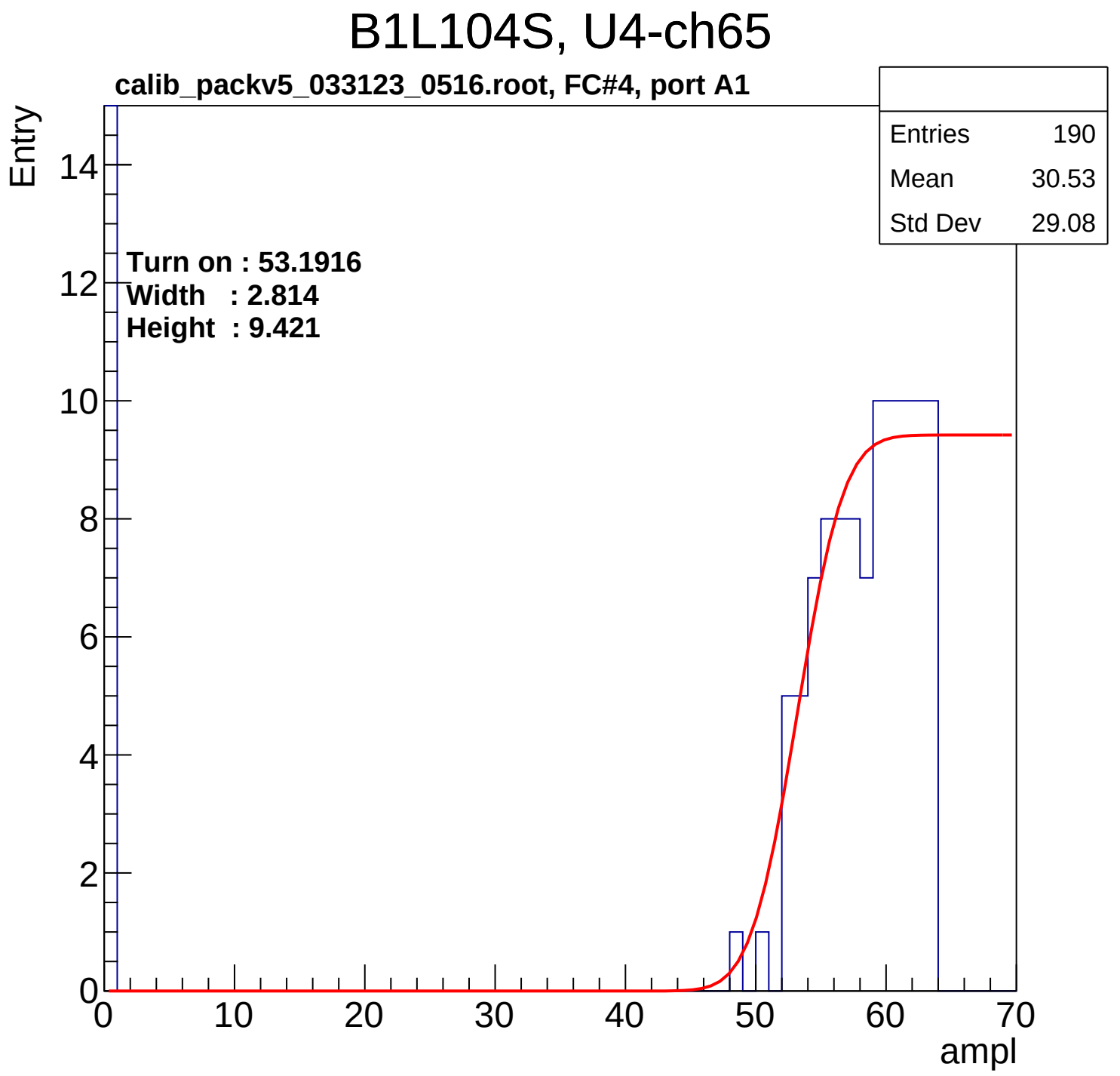

B1L104S, U4-ch60
calib_packv5_033123_0516.root, FC#4, port A1
Entries 164
Mean 29.34
Std Dev 29.44
Turn on : 56.2631
Width : 3.510
Height : 9.889
Entry
ampl
0
10
20
30
40
50
60
70
80

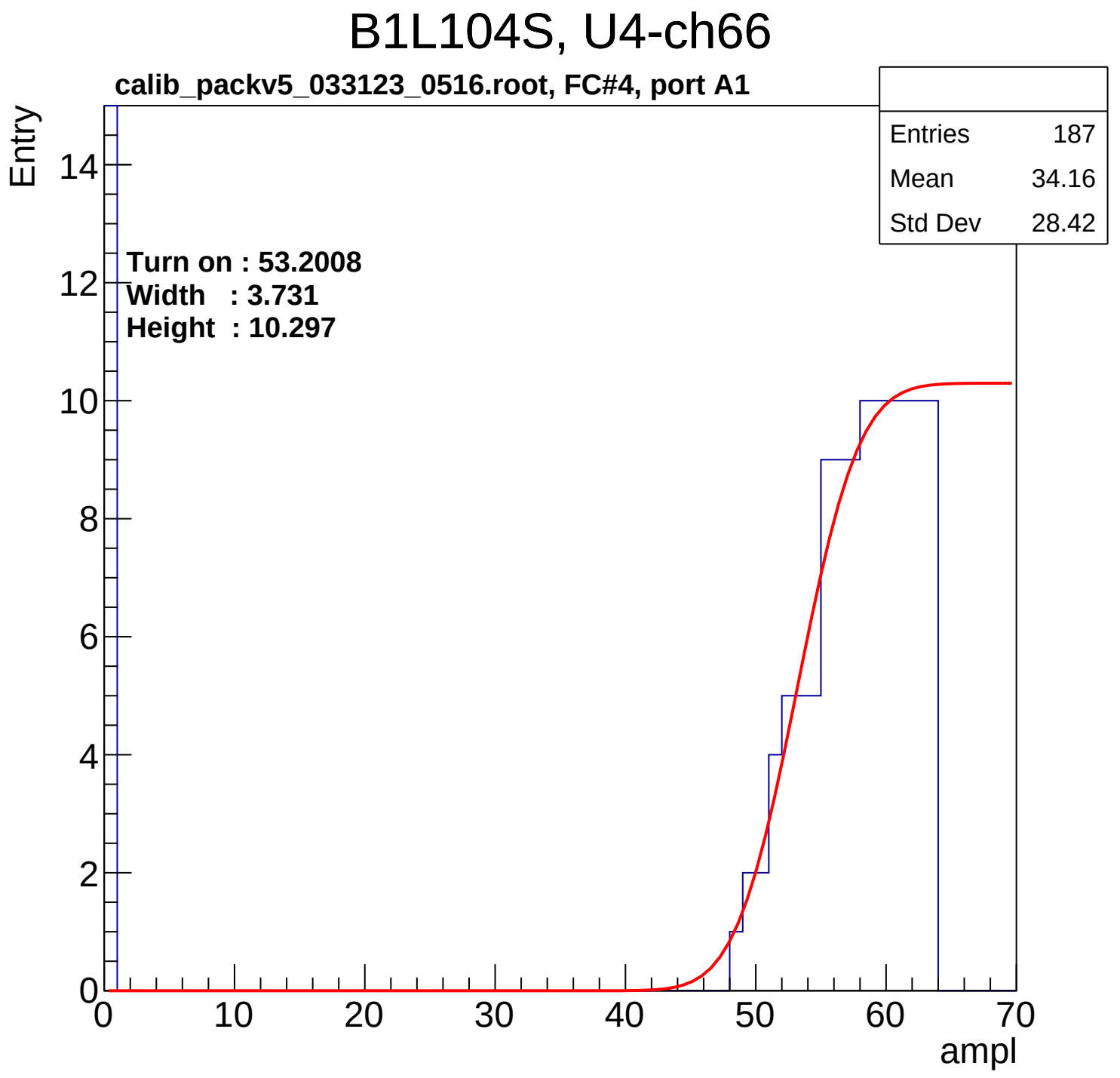

B1L104S, U4-ch61
calib_packv5_033123_0516.root, FC#4, port A1
Entries 186
Mean 29.62
Std Dev 29.12
Turn on : 55.8856
Width : 4.397
Height : 10.778
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

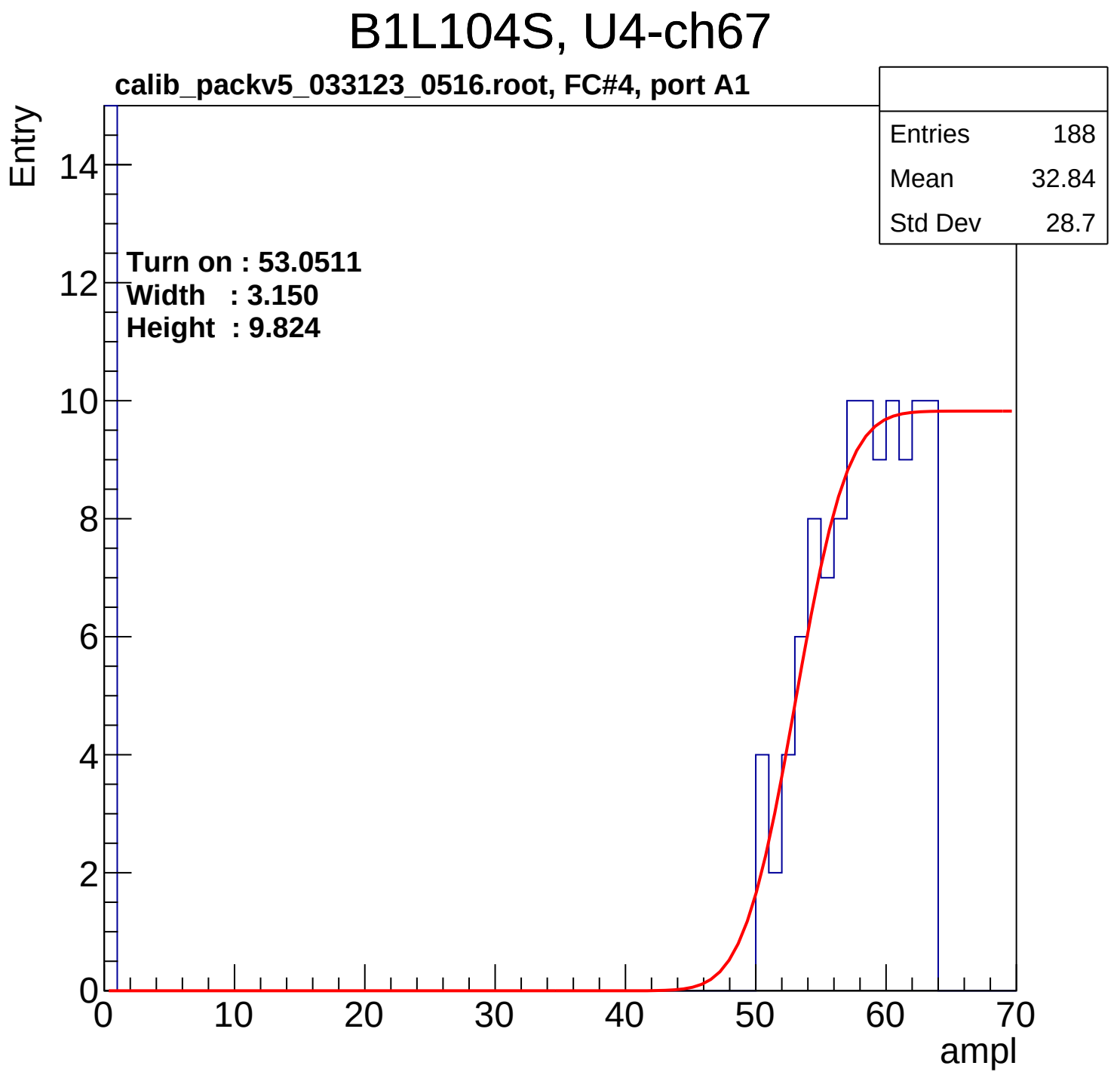

B1L104S, U4-ch62
calib_packv5_033123_0516.root, FC#4, port A1
Entries 209
Mean 25.38
Std Dev 28.99
Turn on : 54.9283
Width : 3.332
Height : 9.884
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

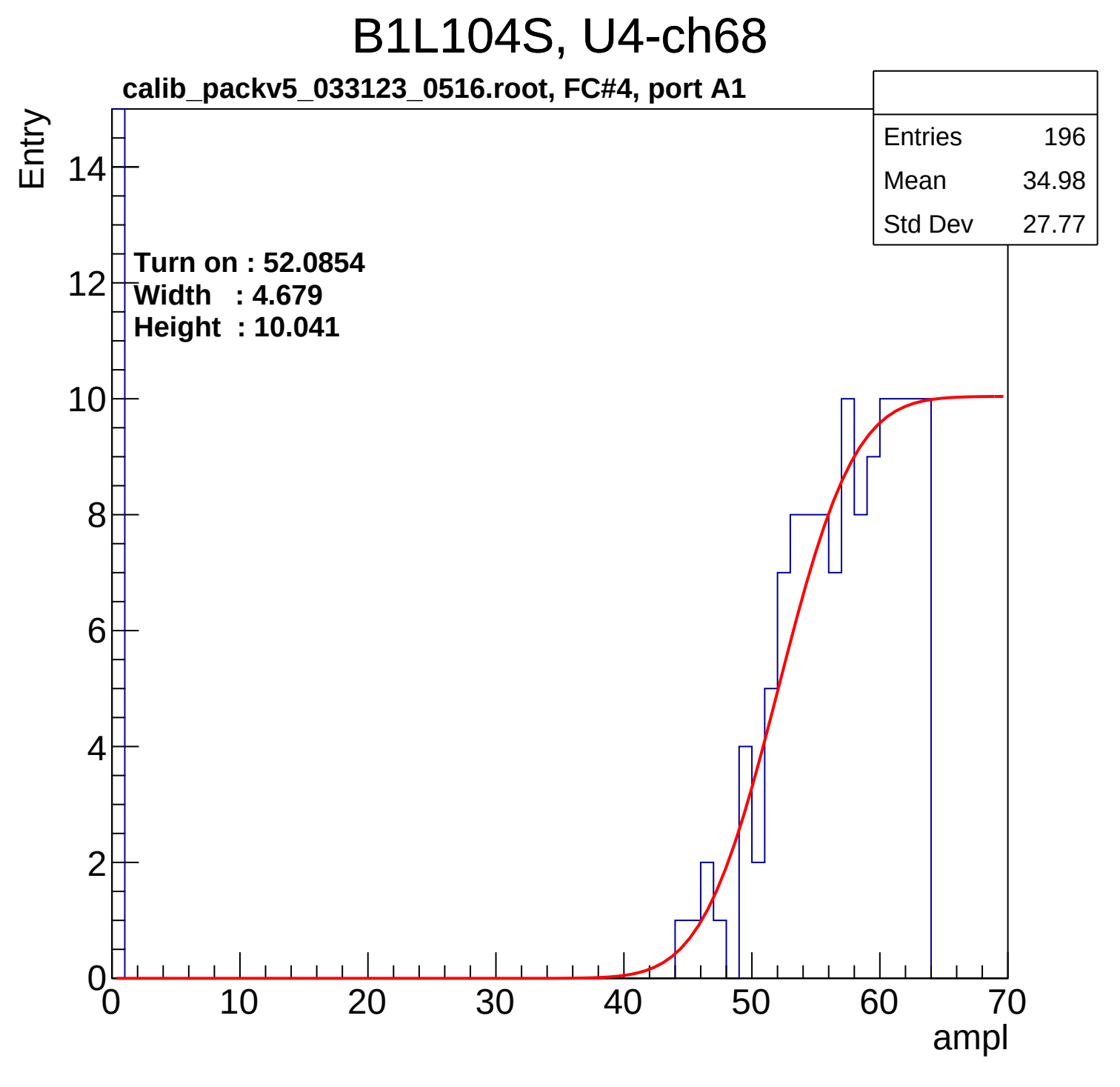

B1L104S, U4-ch63
calib_packv5_033123_0516.root, FC#4, port A1
Entries 203
Mean 31.89
Std Dev 28.62
Turn on : 52.9510
Width : 3.671
Height : 9.989
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

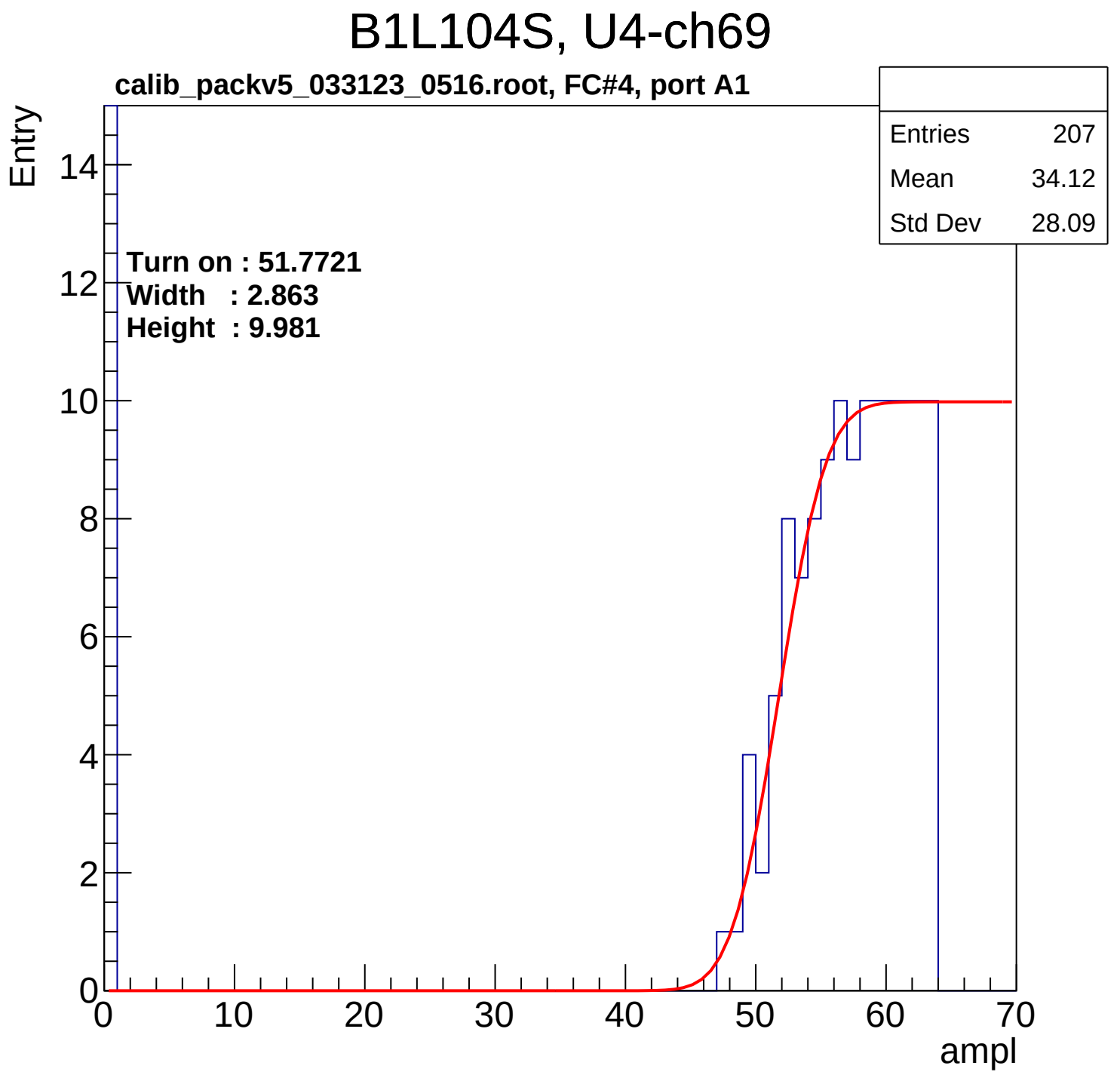

B1L104S, U4-ch64
calib_packv5_033123_0516.root, FC#4, port A1
Entries 201
Mean 34.76
Std Dev 27.9
Turn on : 53.1000
Width : 4.769
Height : 10.869
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

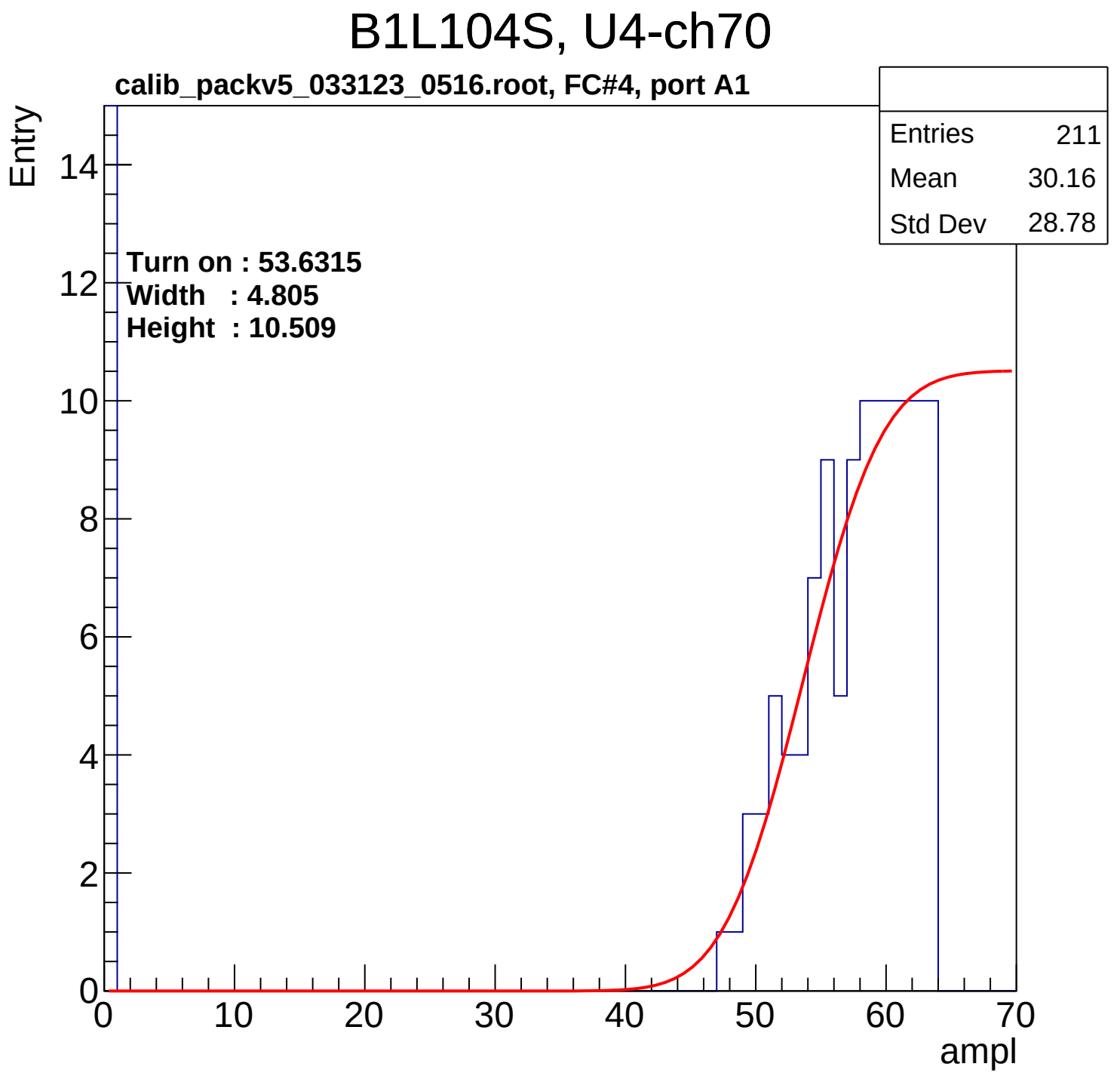

B1L104S, U4-ch65
calib_packv5_033123_0516.root, FC#4, port A1
Entries 190
Mean 30.53
Std Dev 29.08
Turn on : 53.1916
Width : 2.814
Height : 9.421
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

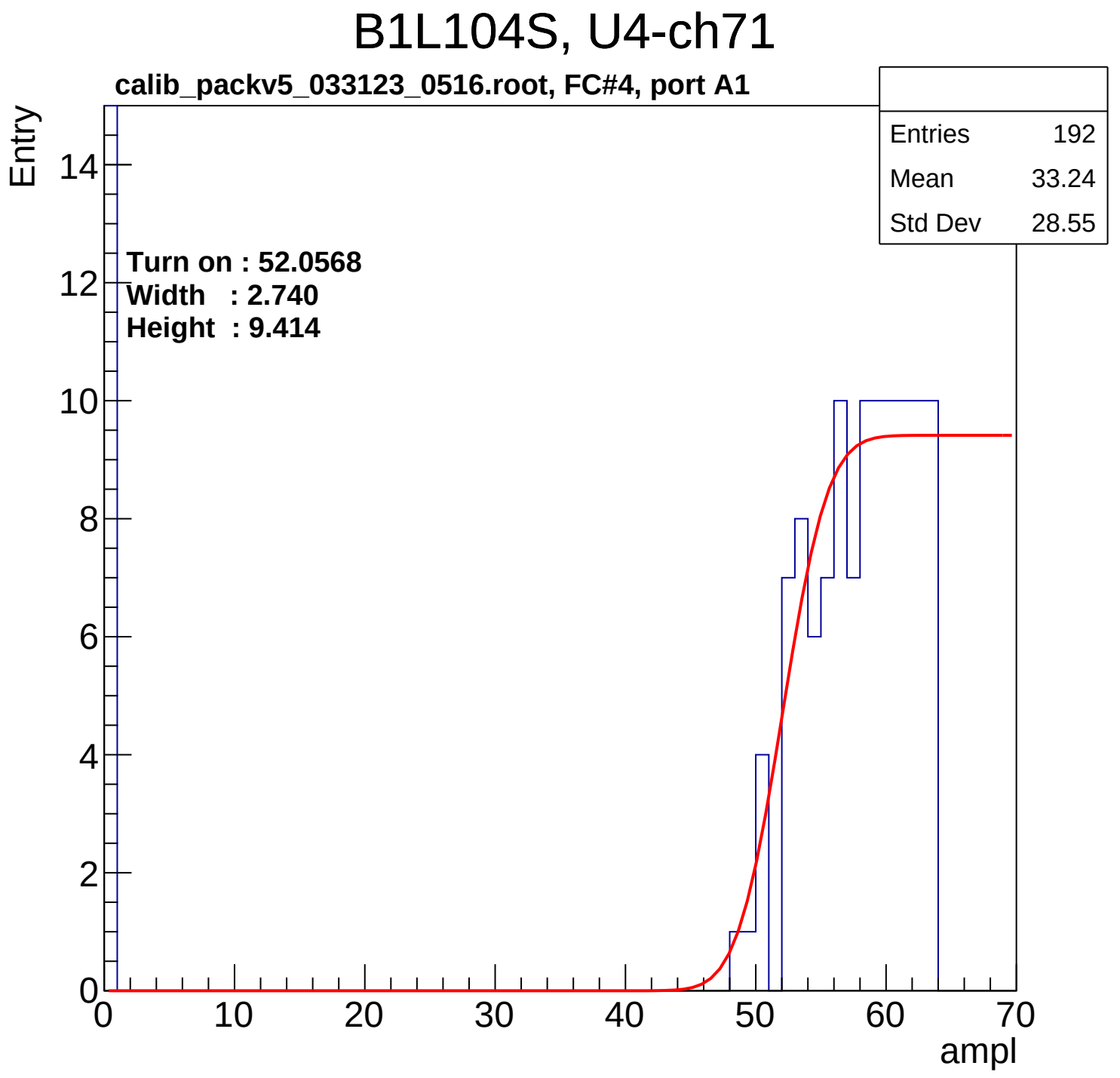

B1L104S, U4-ch66
calib_packv5_033123_0516.root, FC#4, port A1
Entries 187
Mean 34.16
Std Dev 28.42
Turn on : 53.2008
Width : 3.731
Height : 10.297
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

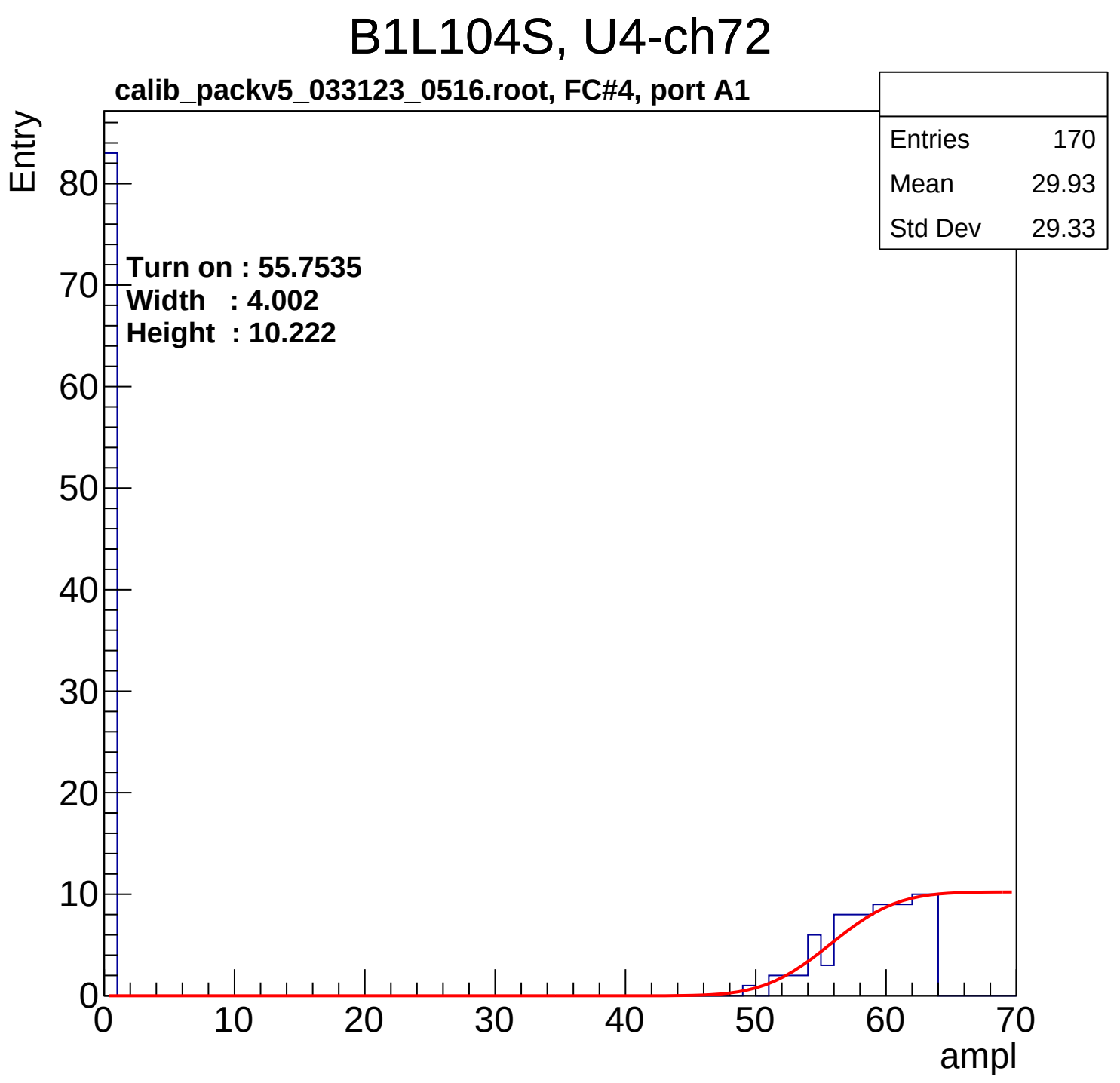

B1L104S, U4-ch67
calib_packv5_033123_0516.root, FC#4, port A1
Entries 188
Mean 32.84
Std Dev 28.7
Turn on : 53.0511
Width : 3.150
Height : 9.824
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

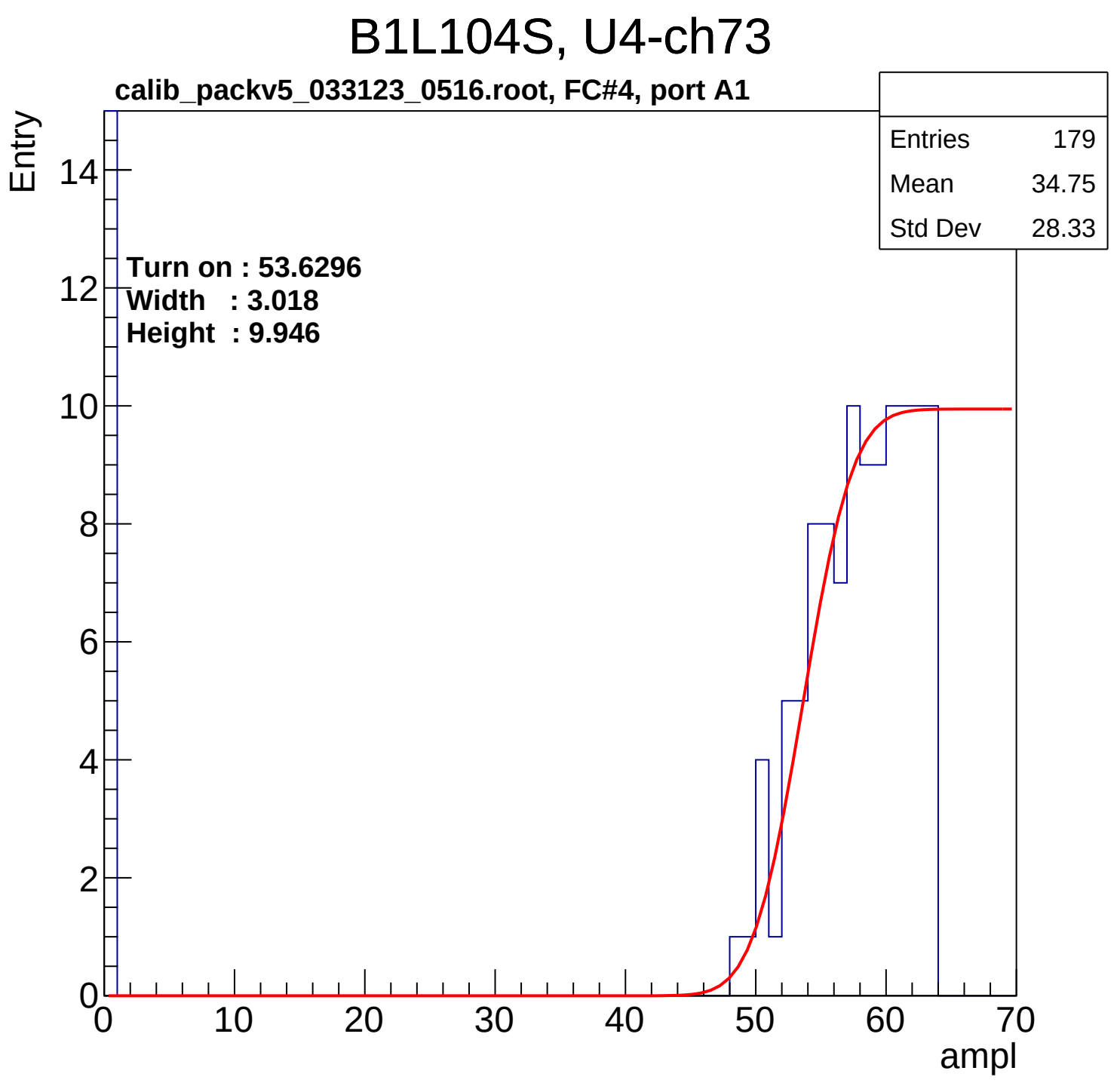

B1L104S, U4-ch68
calib_packv5_033123_0516.root, FC#4, port A1
Entries 196
Mean 34.98
Std Dev 27.77
Turn on : 52.0854
Width : 4.679
Height : 10.041
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

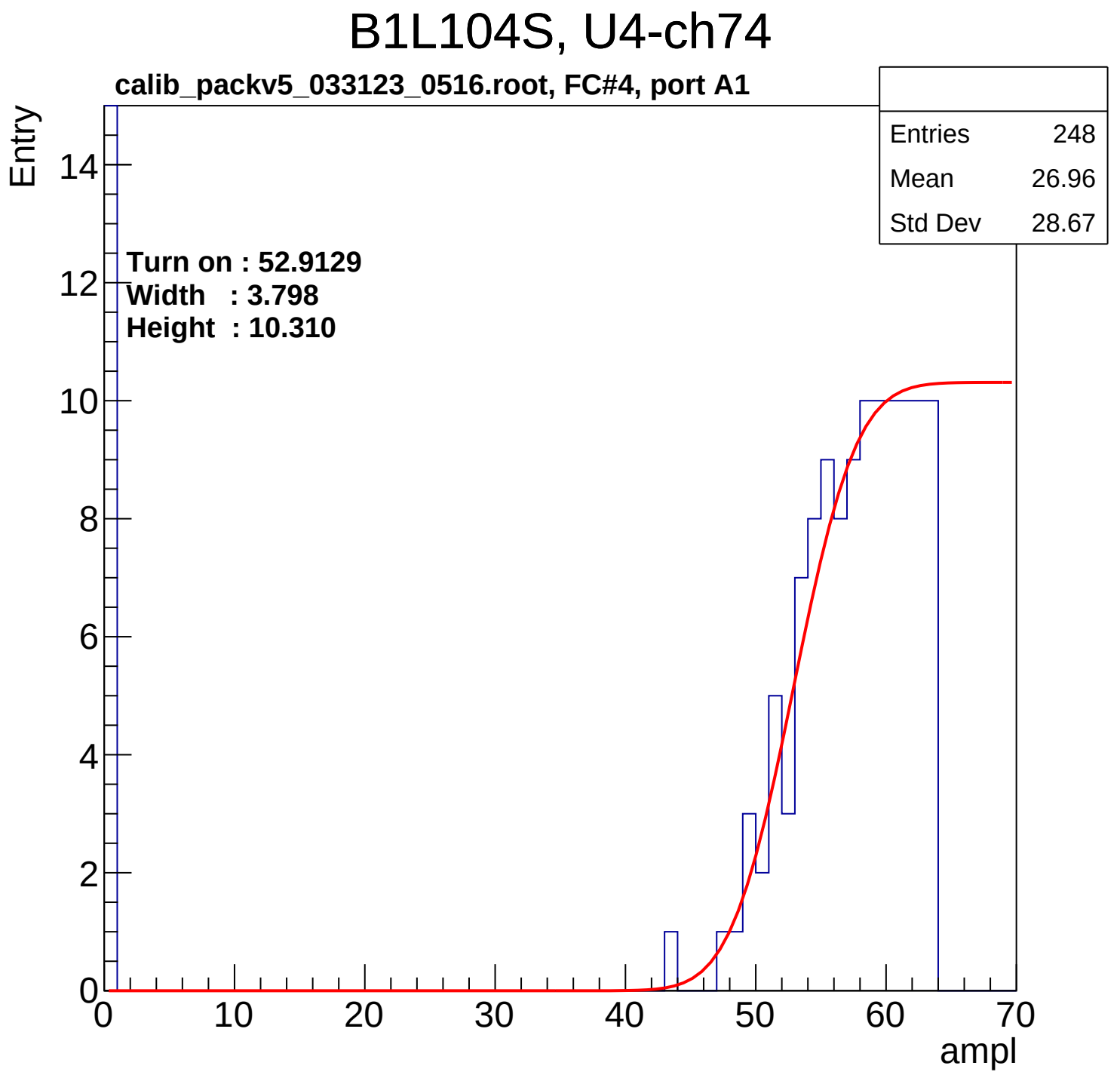

B1L104S, U4-ch69
calib_packv5_033123_0516.root, FC#4, port A1
Entries 207
Mean 34.12
Std Dev 28.09
Turn on : 51.7721
Width : 2.863
Height : 9.981
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

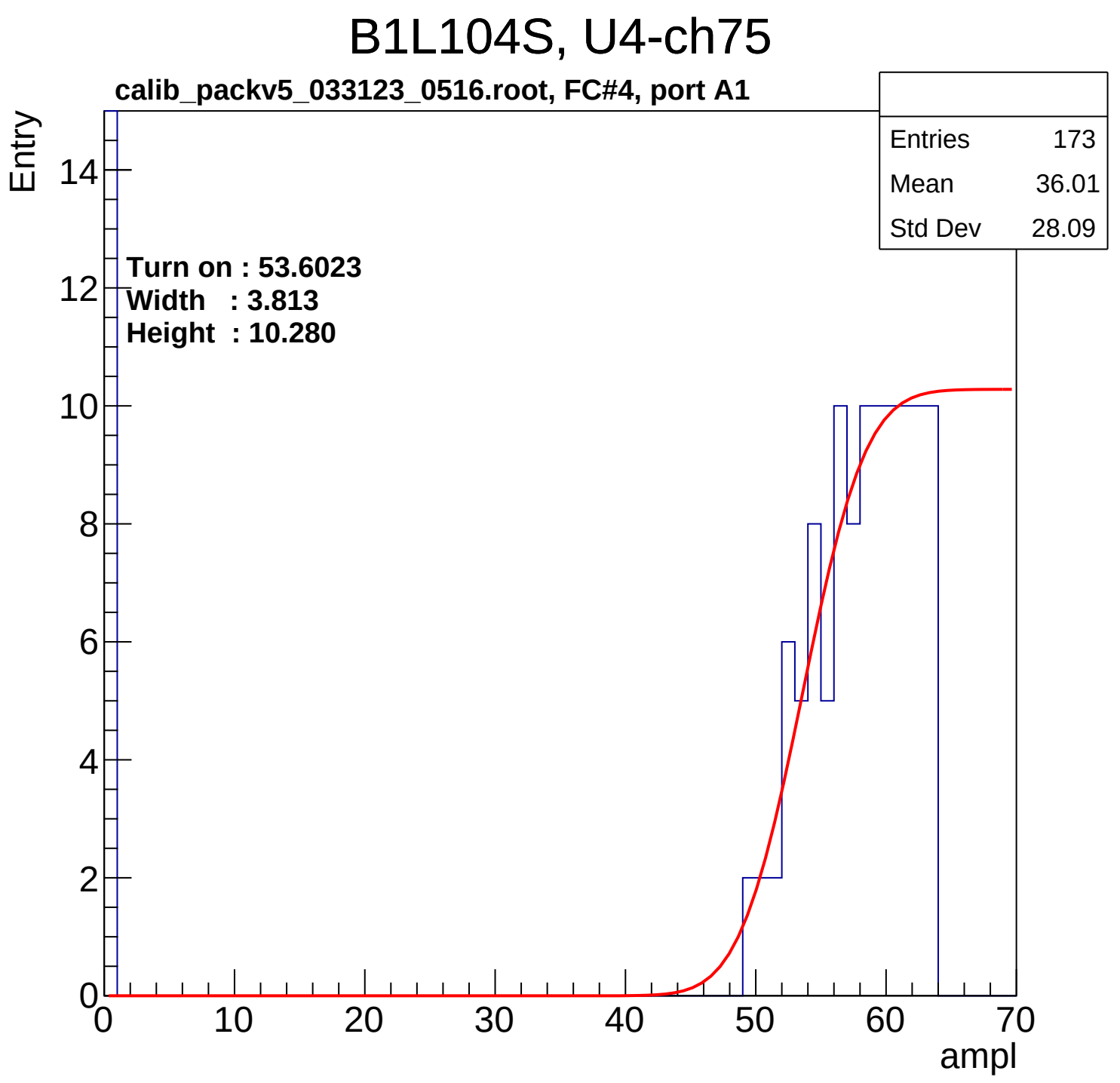

B1L104S, U4-ch70
calib_packv5_033123_0516.root, FC#4, port A1
Entries 211
Mean 30.16
Std Dev 28.78
Turn on : 53.6315
Width : 4.805
Height : 10.509
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

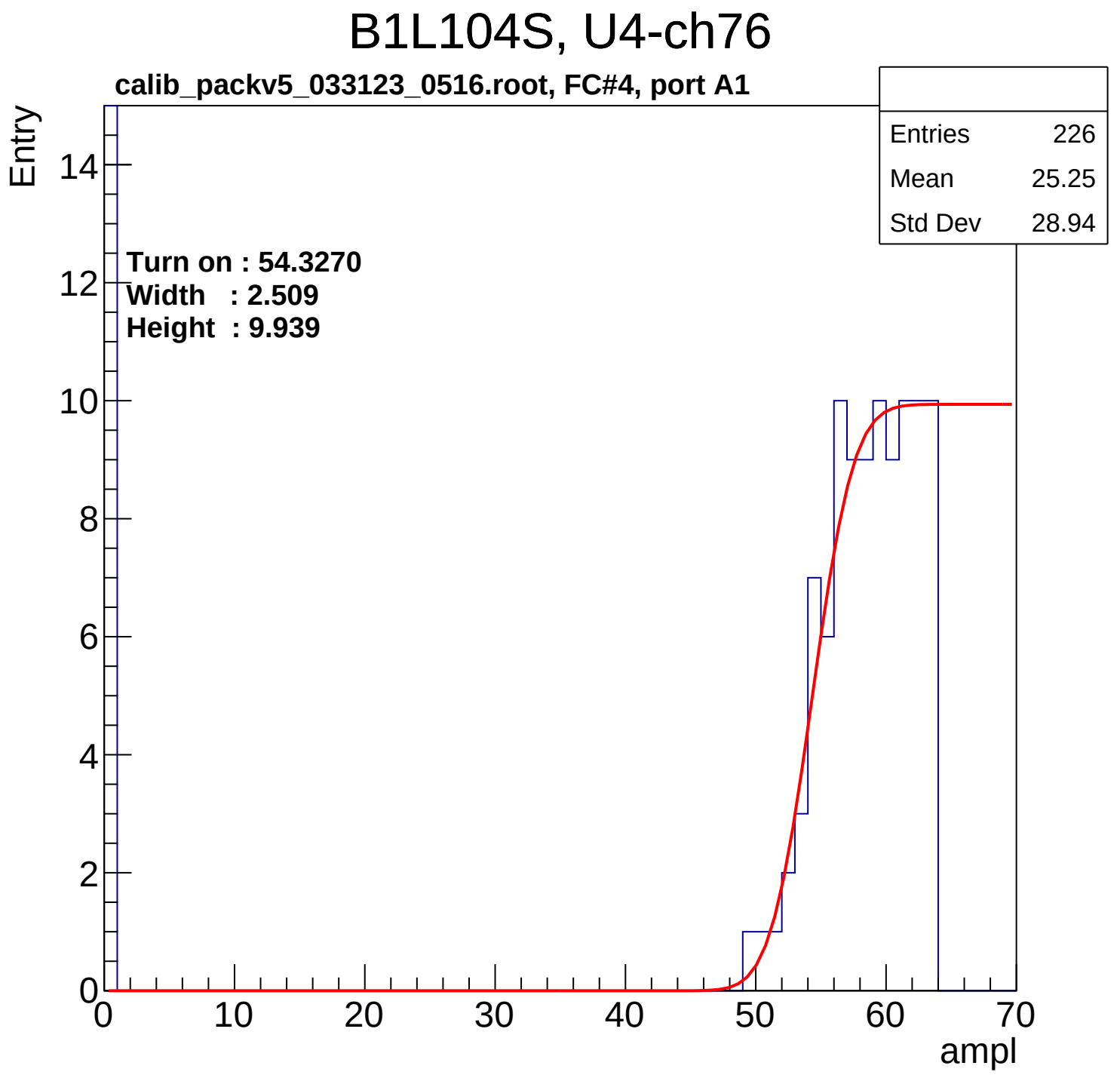

B1L104S, U4-ch71
calib_packv5_033123_0516.root, FC#4, port A1
Entries 192
Mean 33.24
Std Dev 28.55
Turn on : 52.0568
Width : 2.740
Height : 9.414
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

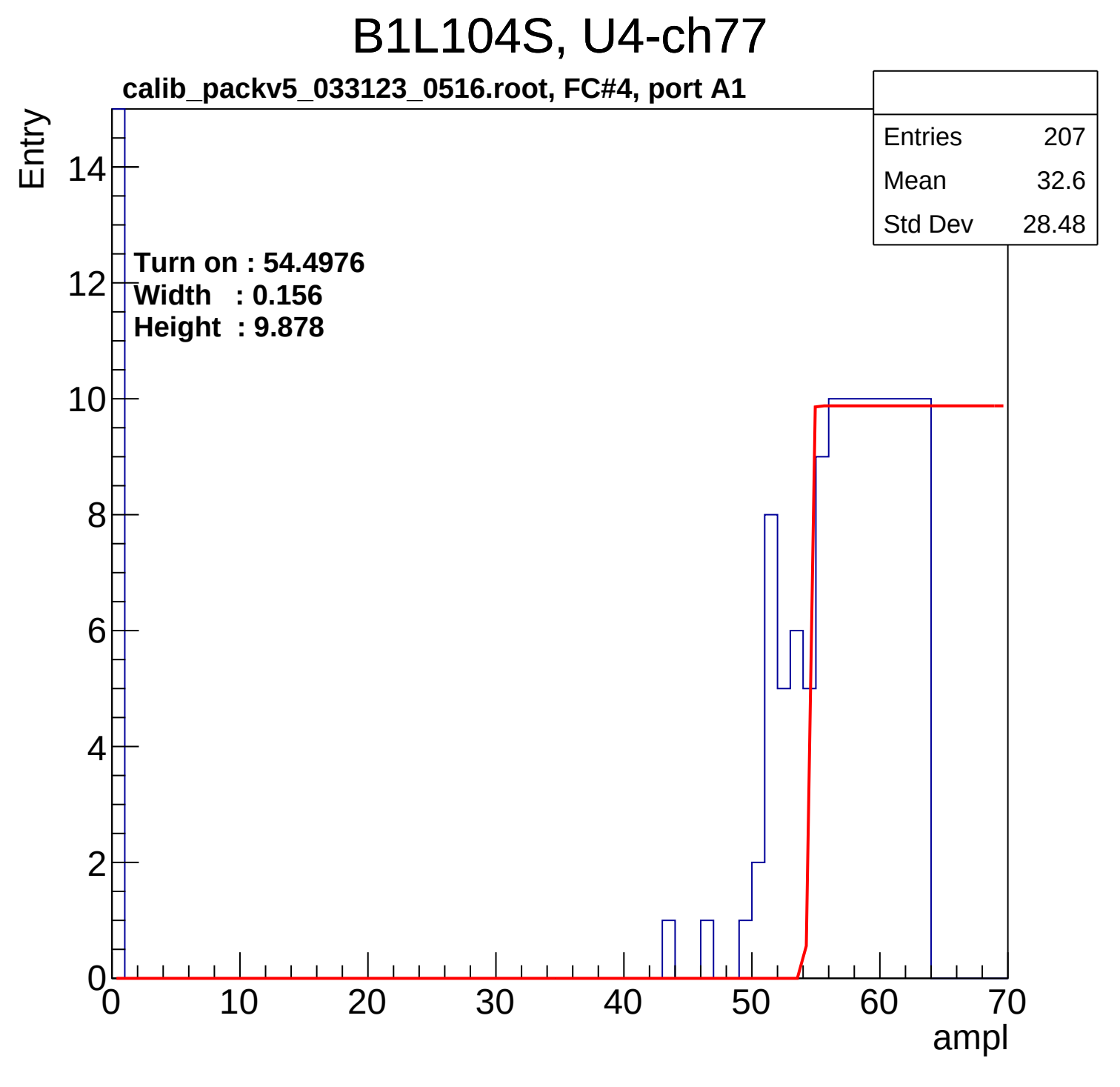

B1L104S, U4-ch72
calib_packv5_033123_0516.root, FC#4, port A1
Entries 170
Mean 29.93
Std Dev 29.33
Turn on : 55.7535
Width : 4.002
Height : 10.222
Entry
0
10
20
30
40
50
60
70
80
ampl

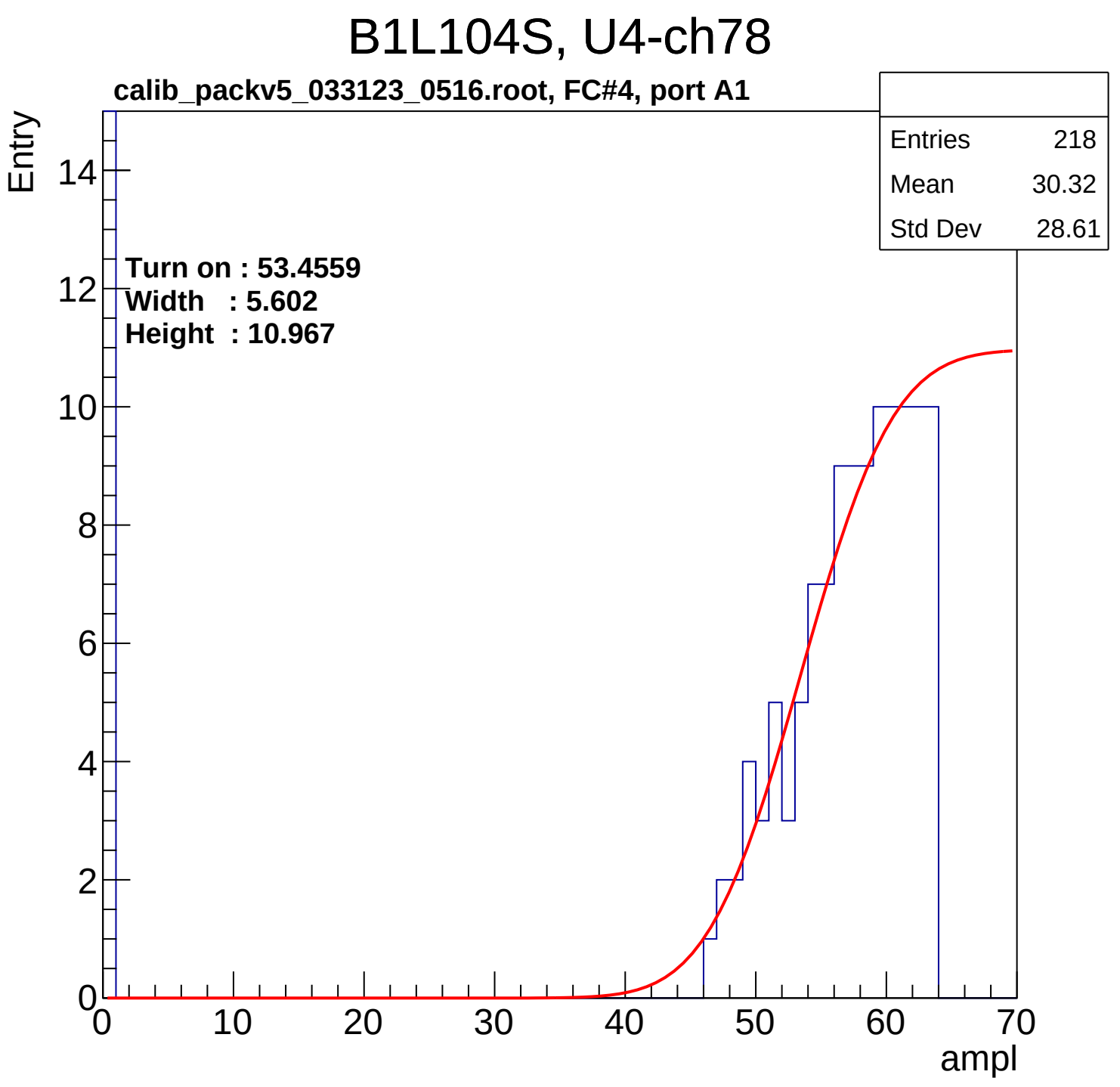

B1L104S, U4-ch73
calib_packv5_033123_0516.root, FC#4, port A1
Entries 179
Mean 34.75
Std Dev 28.33
Turn on : 53.6296
Width : 3.018
Height : 9.946
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

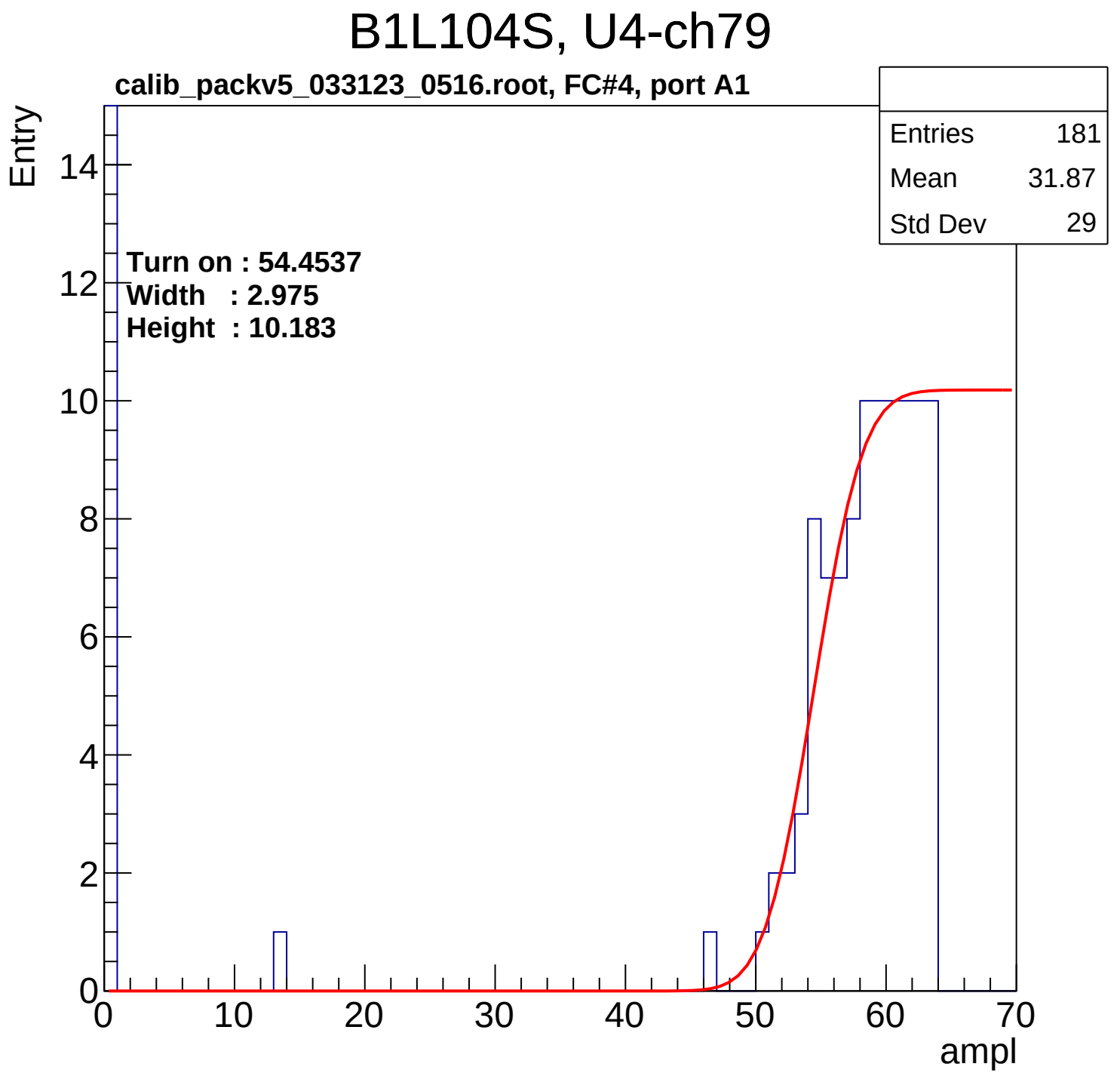

B1L104S, U4-ch74
calib_packv5_033123_0516.root, FC#4, port A1
Entries 248
Mean 26.96
Std Dev 28.67
Turn on : 52.9129
Width : 3.798
Height : 10.310
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

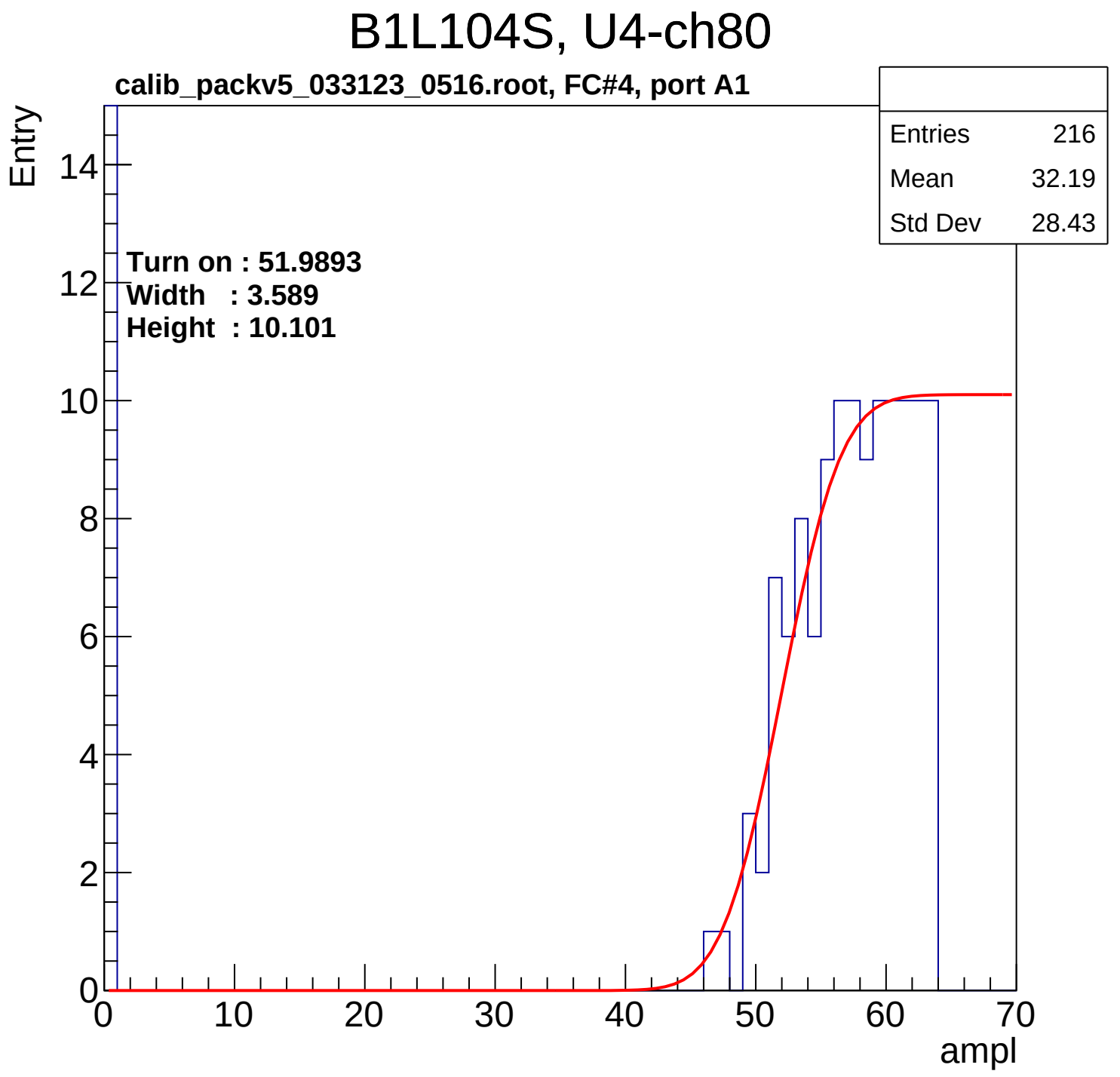

B1L104S, U4-ch75
calib_packv5_033123_0516.root, FC#4, port A1
Entries 173
Mean 36.01
Std Dev 28.09
Turn on : 53.6023
Width : 3.813
Height : 10.280
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

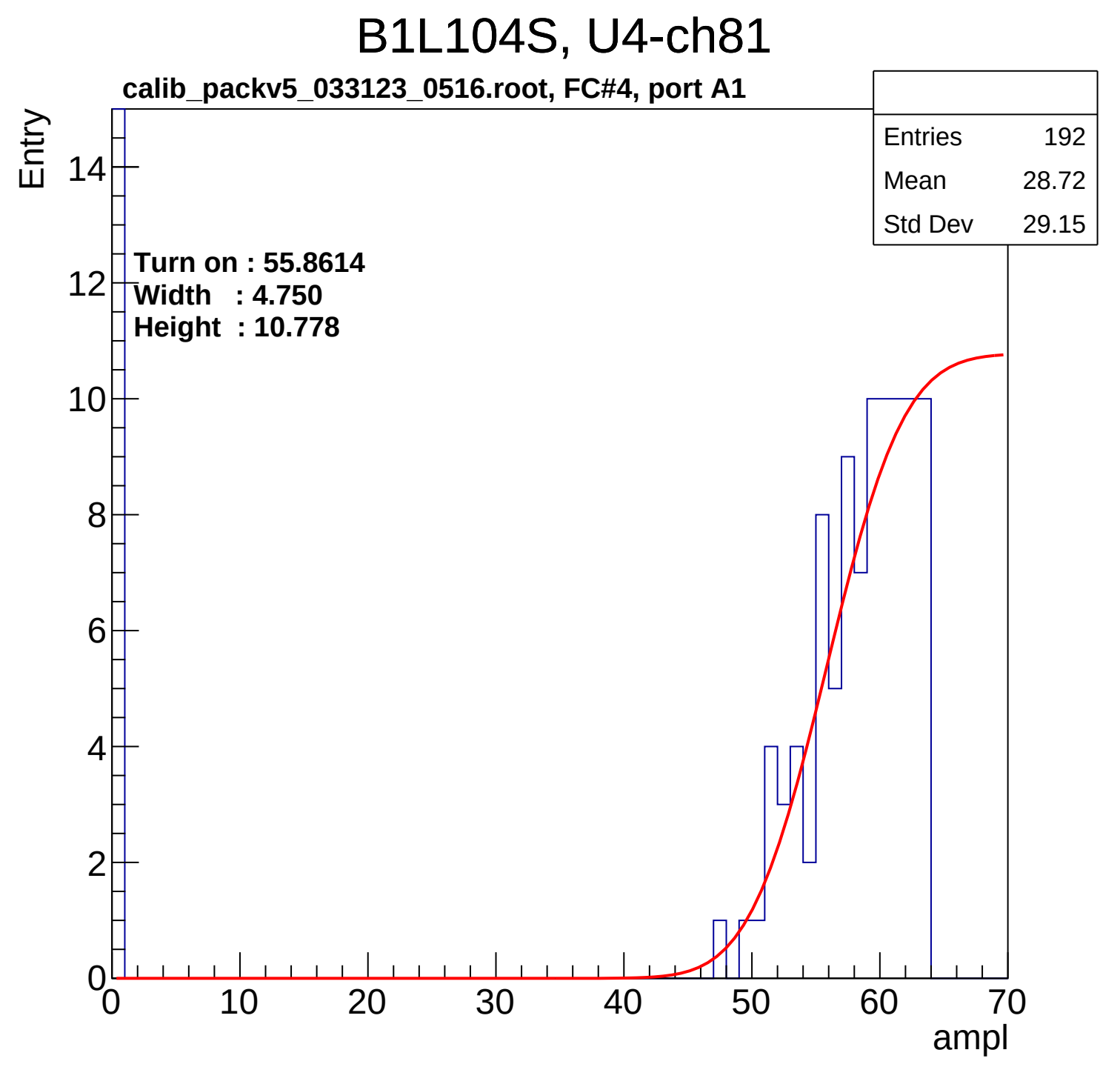

B1L104S, U4-ch76
calib_packv5_033123_0516.root, FC#4, port A1
Entries 226
Mean 25.25
Std Dev 28.94
Turn on : 54.3270
Width : 2.509
Height : 9.939
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

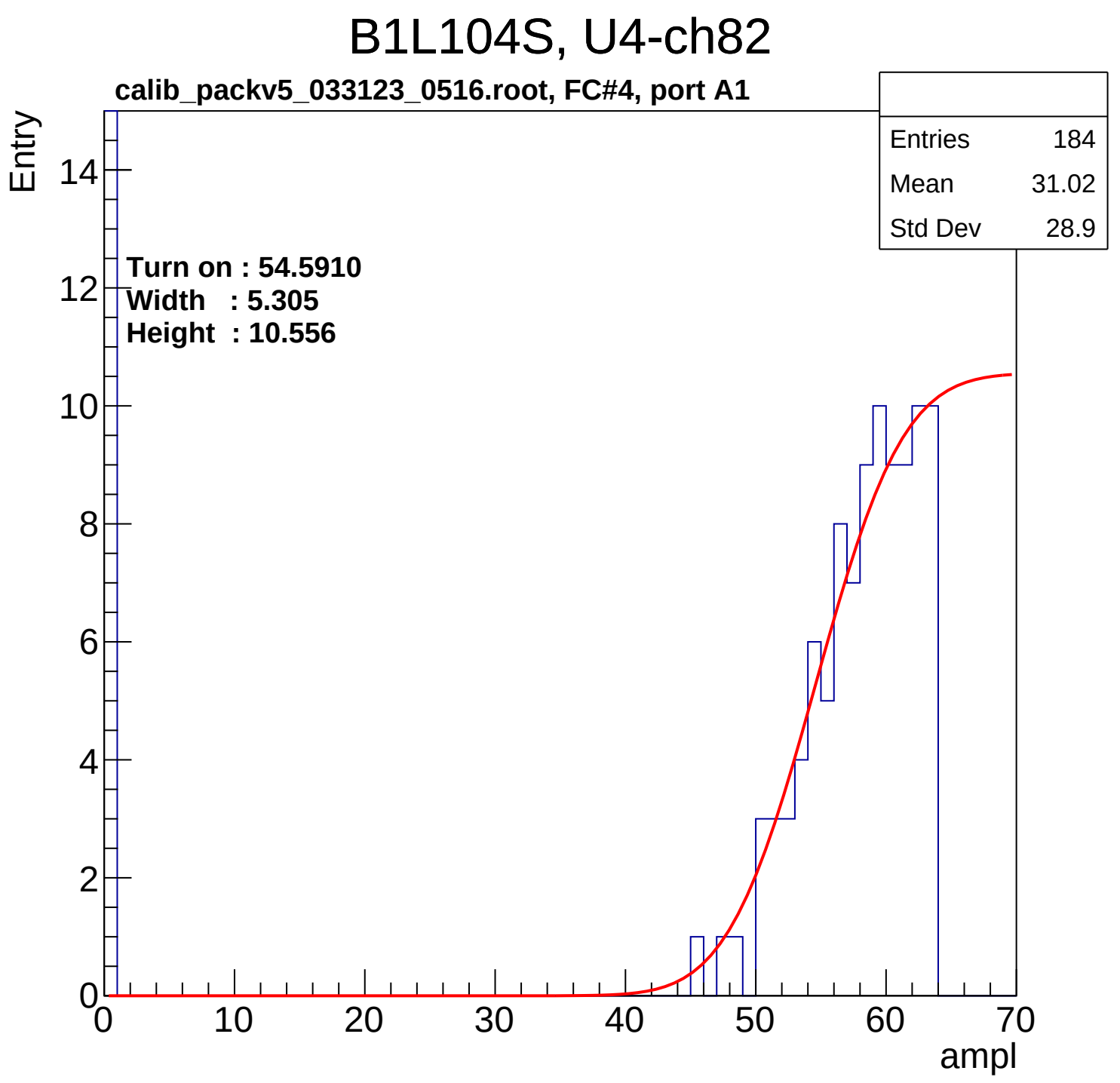

B1L104S, U4-ch77
calib_packv5_033123_0516.root, FC#4, port A1
Entries 207
Mean 32.6
Std Dev 28.48
Turn on : 54.4976
Width : 0.156
Height : 9.878
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

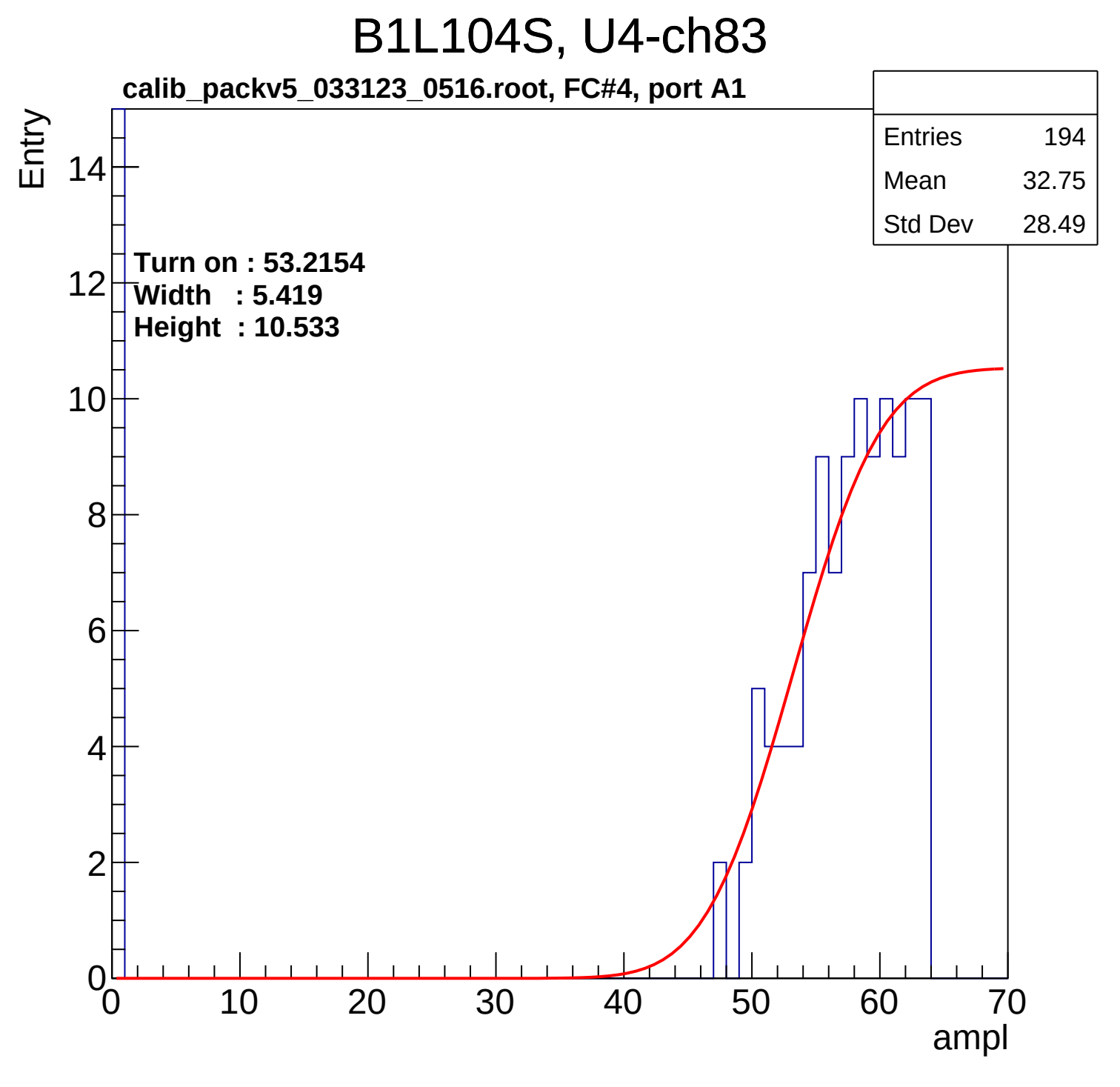

B1L104S, U4-ch78
calib_packv5_033123_0516.root, FC#4, port A1
Entries 218
Mean 30.32
Std Dev 28.61
Turn on : 53.4559
Width : 5.602
Height : 10.967
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

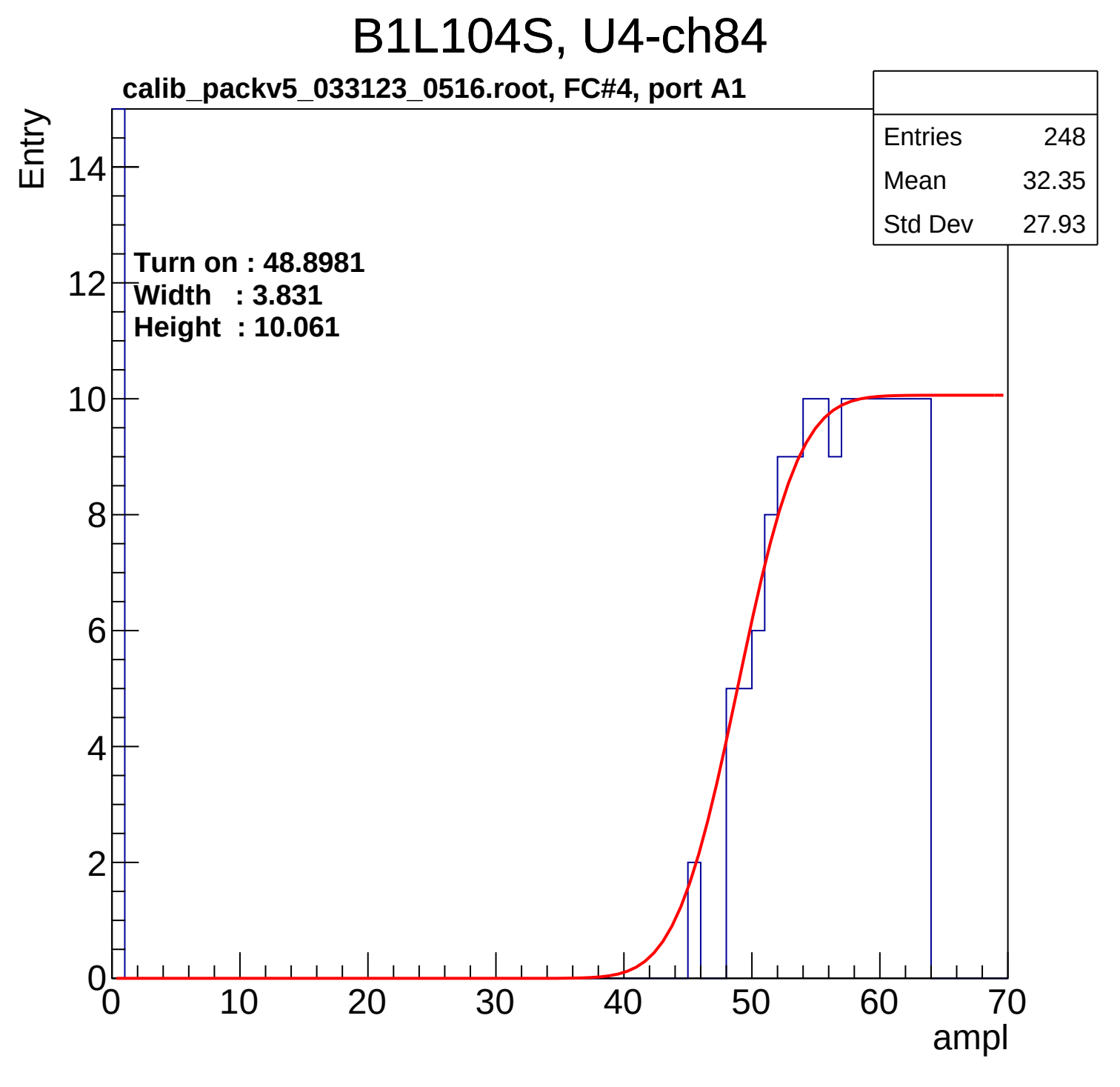

B1L104S, U4-ch79
calib_packv5_033123_0516.root, FC#4, port A1
Entries 181
Mean 31.87
Std Dev 29
Turn on : 54.4537
Width : 2.975
Height : 10.183
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

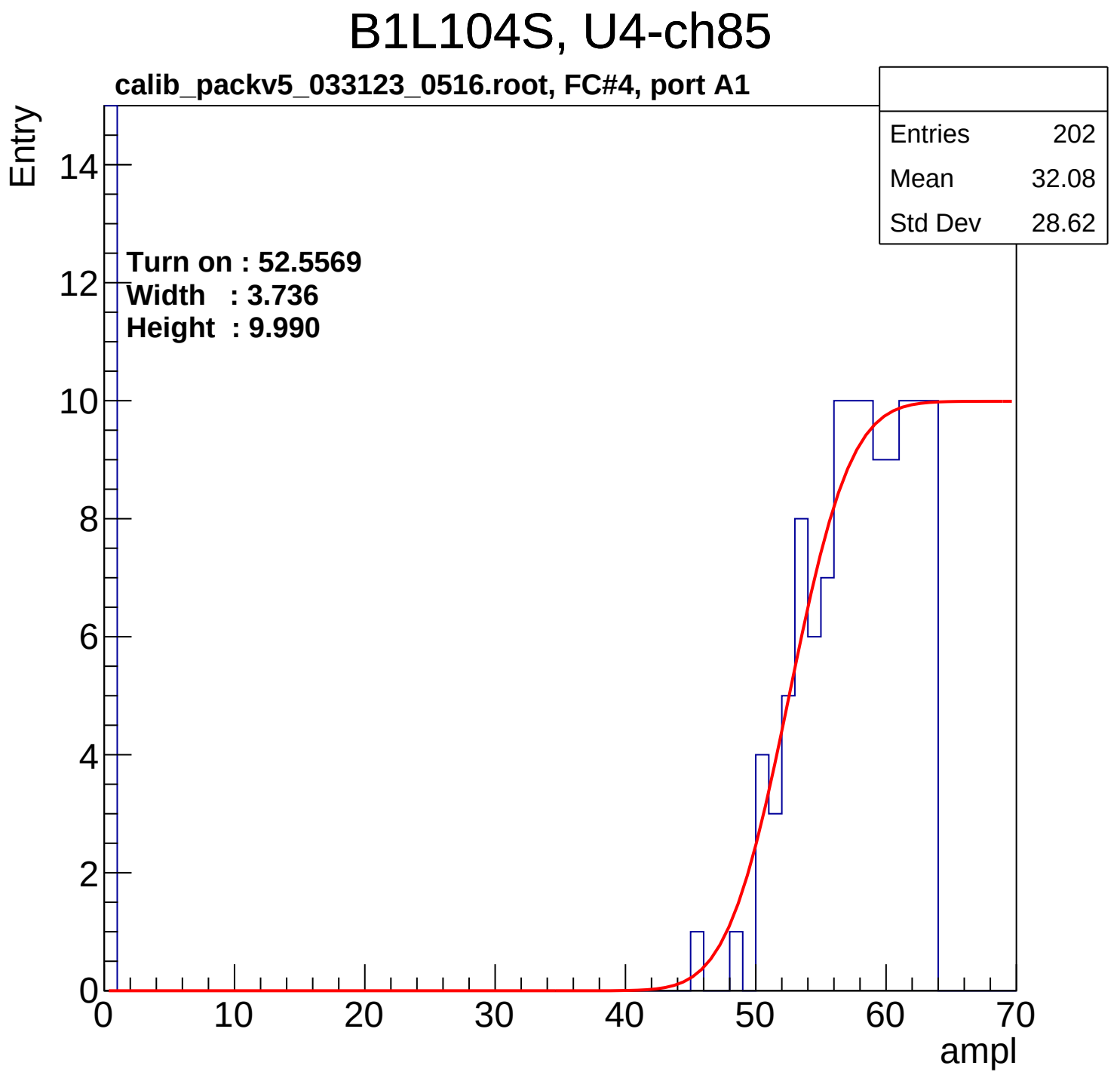

B1L104S, U4-ch80
calib_packv5_033123_0516.root, FC#4, port A1
Entries 216
Mean 32.19
Std Dev 28.43
Turn on : 51.9893
Width : 3.589
Height : 10.101
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

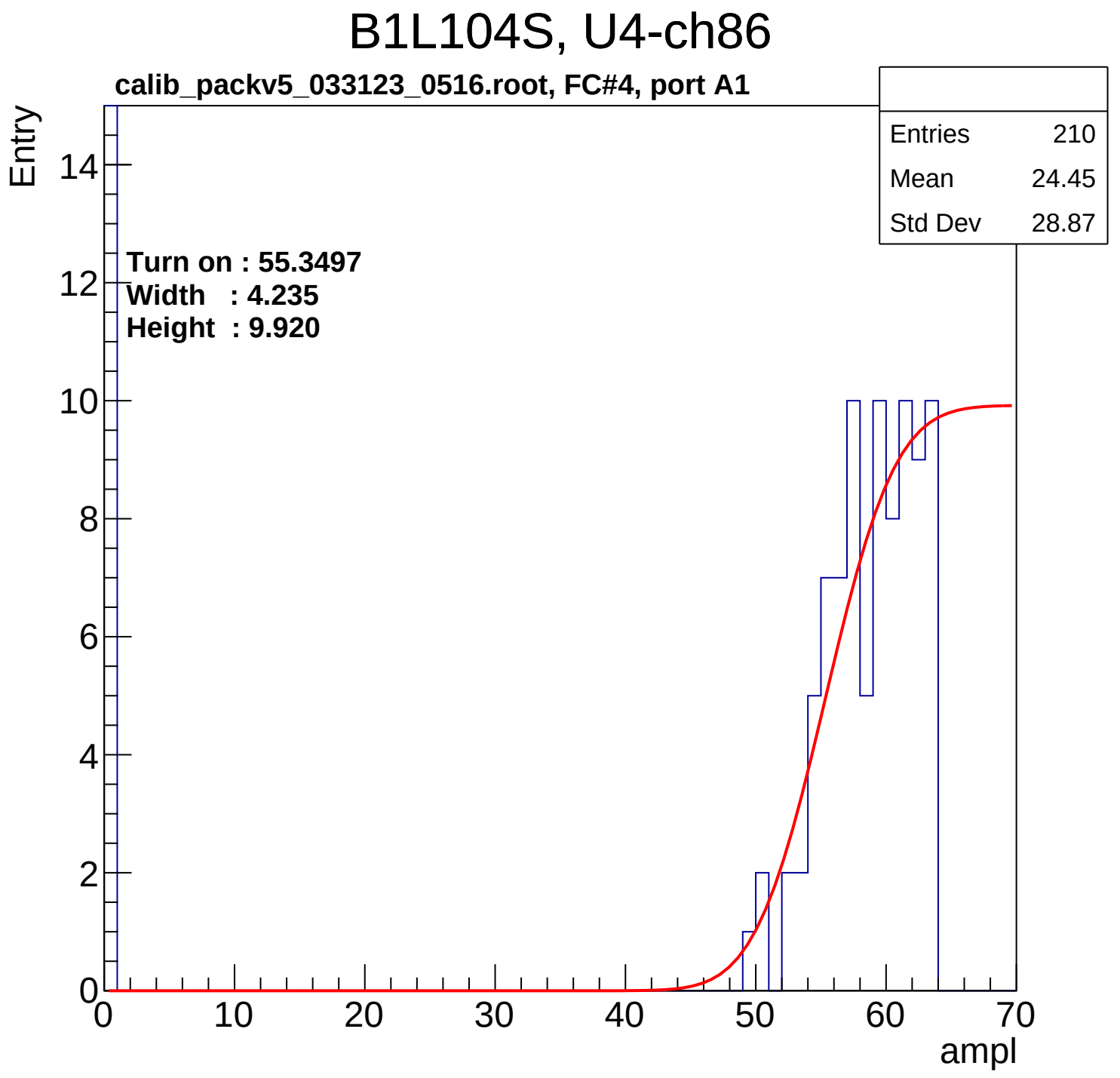

B1L104S, U4-ch81
calib_packv5_033123_0516.root, FC#4, port A1
Entries 192
Mean 28.72
Std Dev 29.15
Turn on : 55.8614
Width : 4.750
Height : 10.778
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

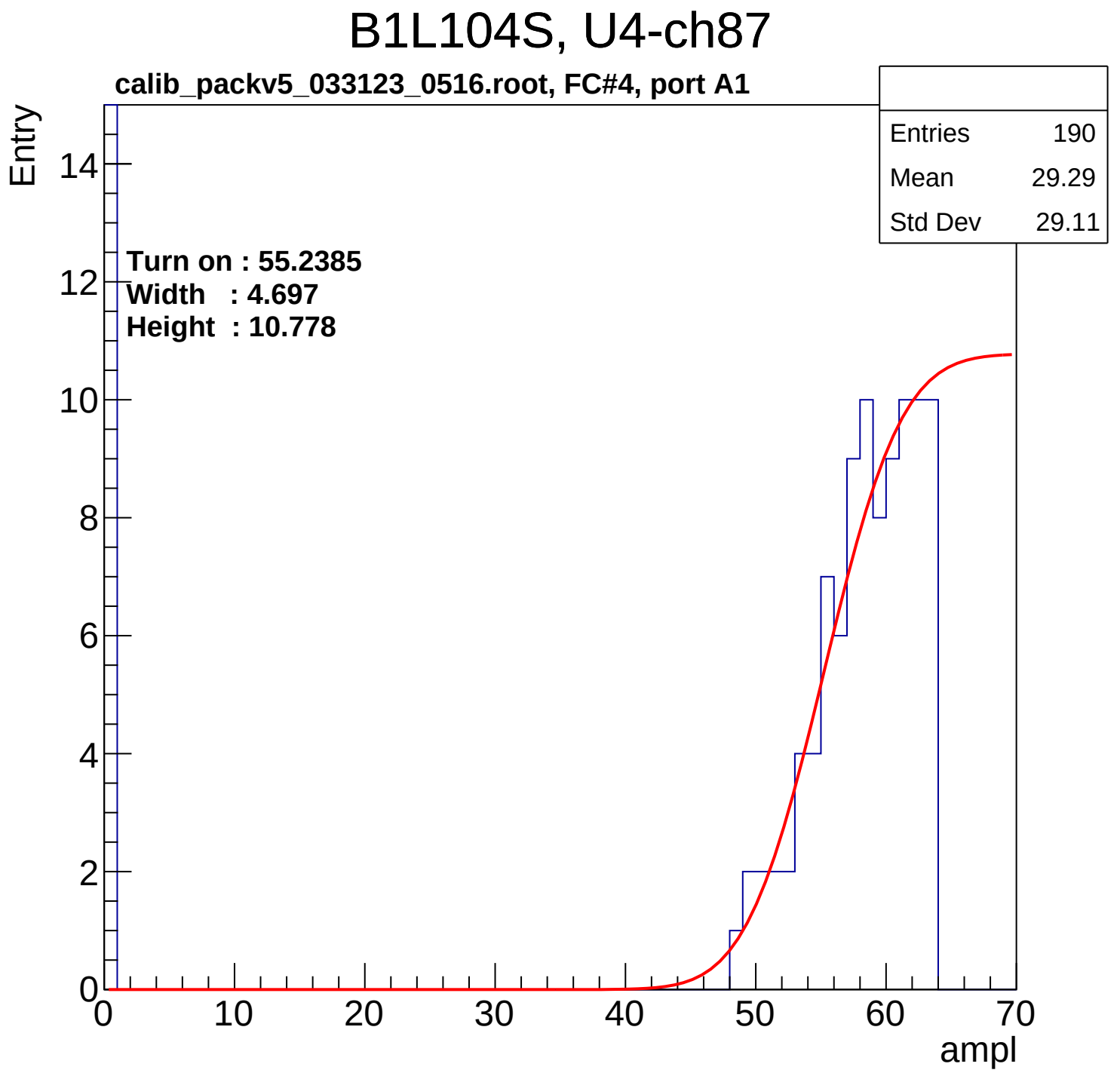

B1L104S, U4-ch82
calib_packv5_033123_0516.root, FC#4, port A1
Entries 184
Mean 31.02
Std Dev 28.9
Turn on : 54.5910
Width : 5.305
Height : 10.556
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

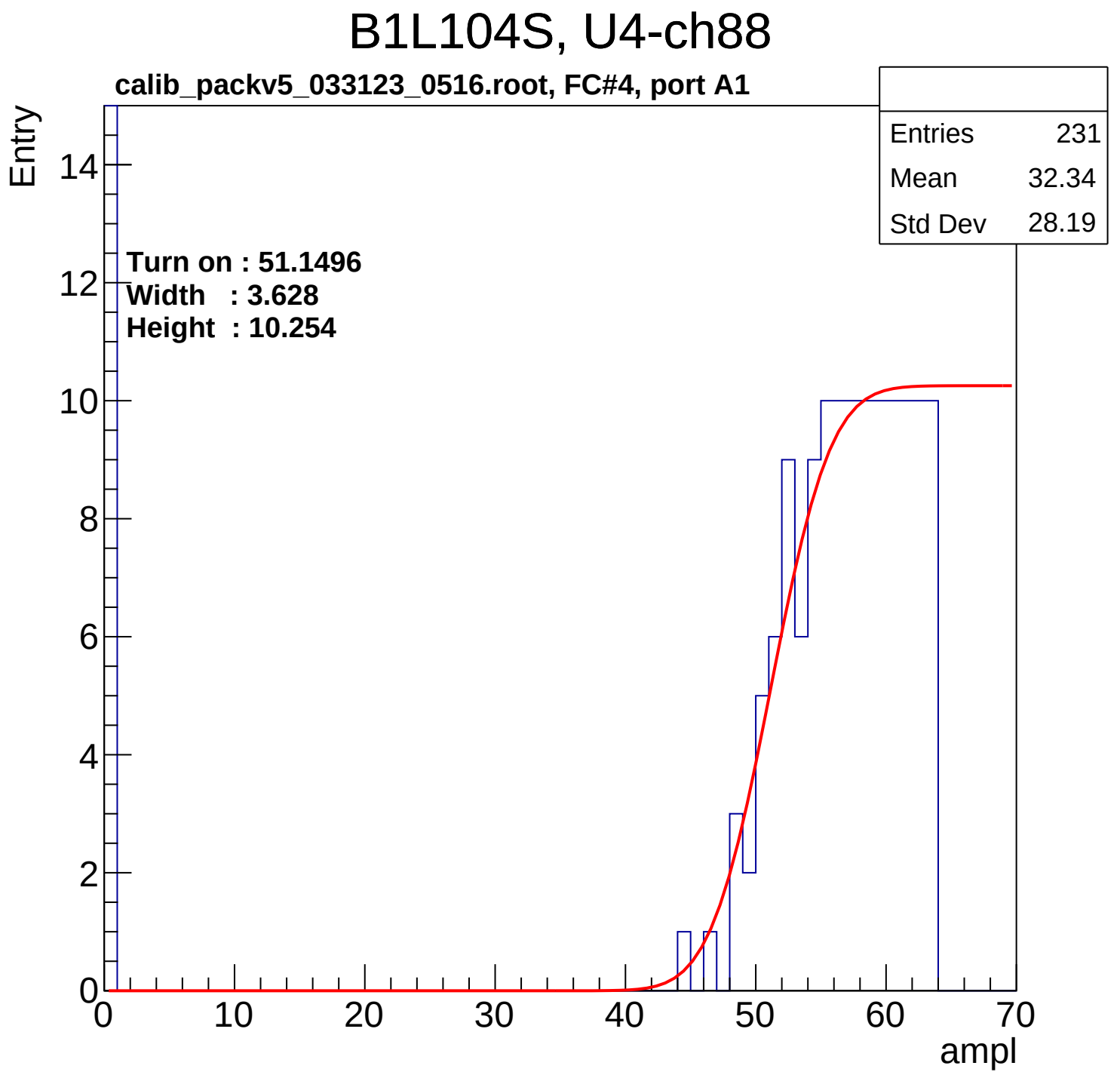

B1L104S, U4-ch83
calib_packv5_033123_0516.root, FC#4, port A1
Entries 194
Mean 32.75
Std Dev 28.49
Turn on : 53.2154
Width : 5.419
Height : 10.533
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

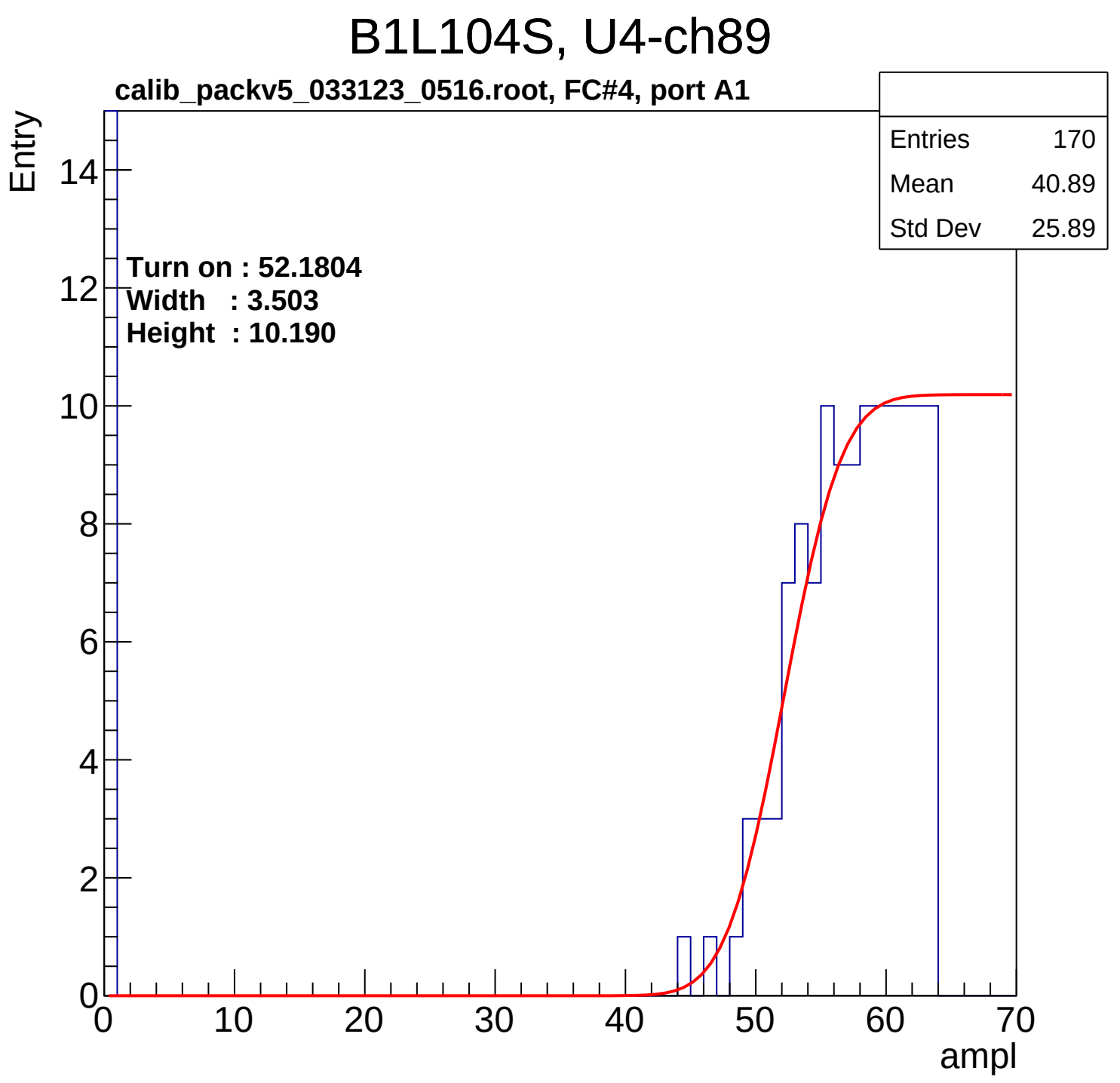

B1L104S, U4-ch84
calib_packv5_033123_0516.root, FC#4, port A1
Entries 248
Mean 32.35
Std Dev 27.93
Turn on : 48.8981
Width : 3.831
Height : 10.061
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

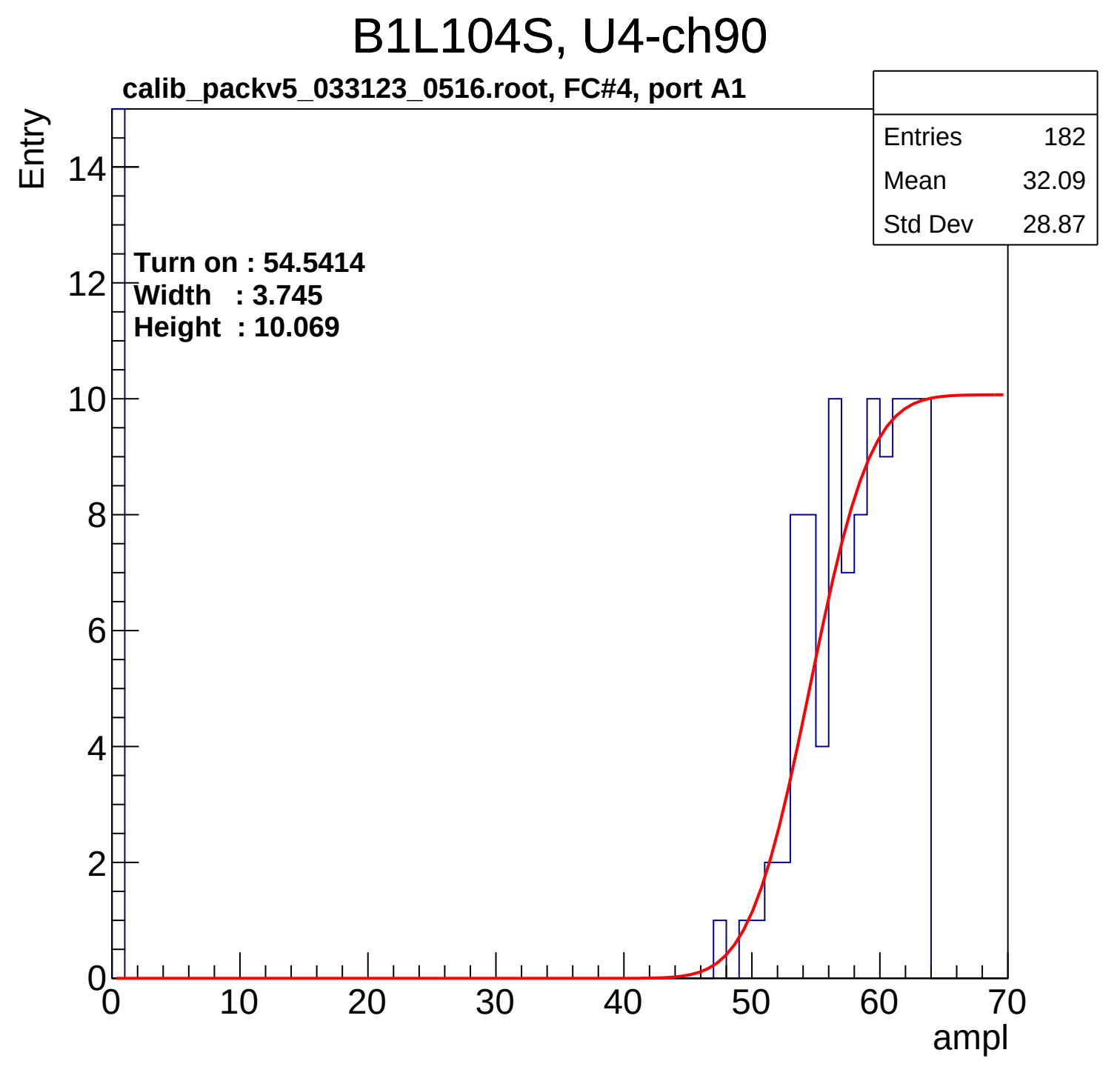

B1L104S, U4-ch85
calib_packv5_033123_0516.root, FC#4, port A1
Entries 202
Mean 32.08
Std Dev 28.62
Turn on : 52.5569
Width : 3.736
Height : 9.990
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

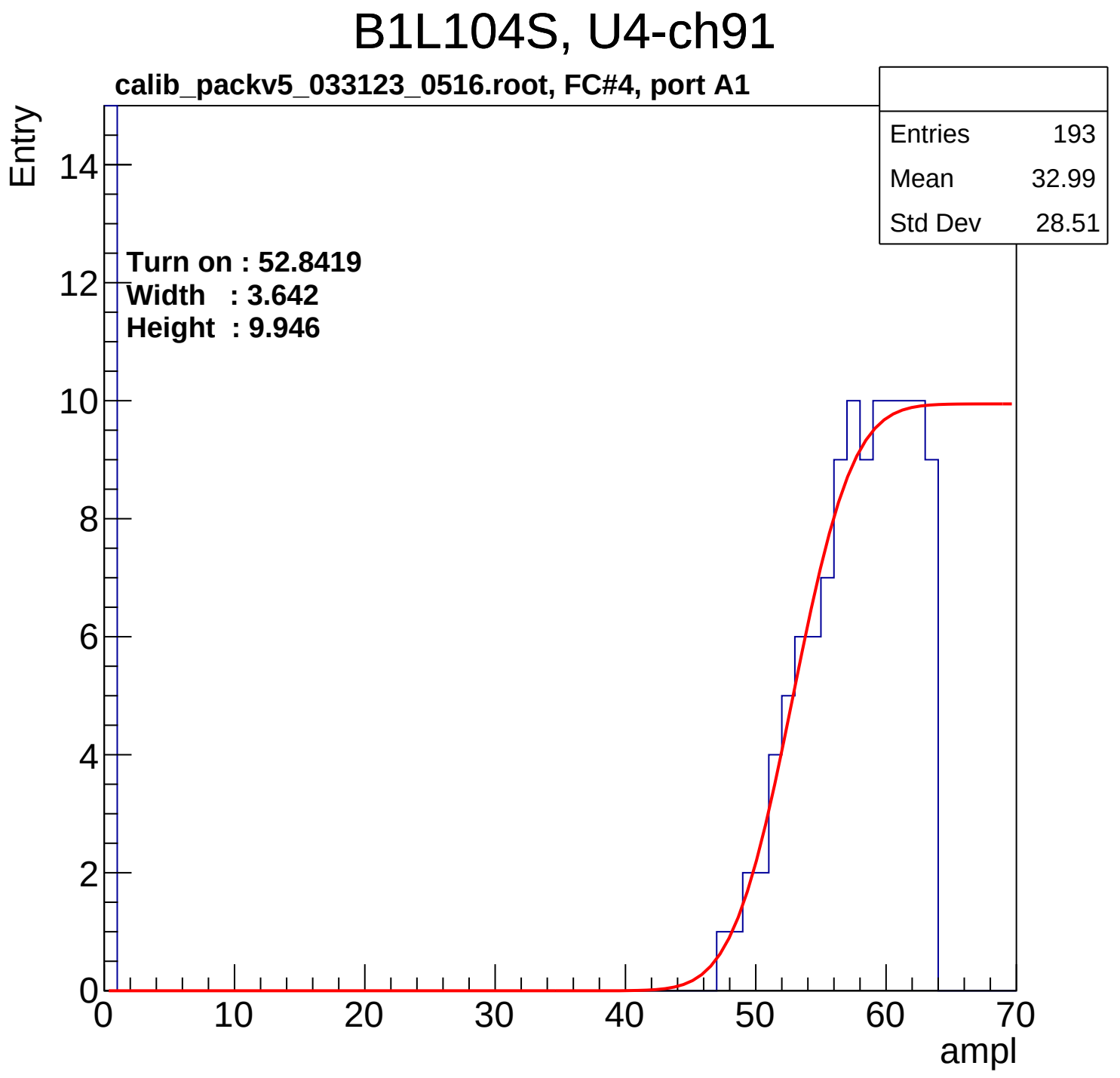

B1L104S, U4-ch86
calib_packv5_033123_0516.root, FC#4, port A1
Entries 210
Mean 24.45
Std Dev 28.87
Turn on : 55.3497
Width : 4.235
Height : 9.920
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

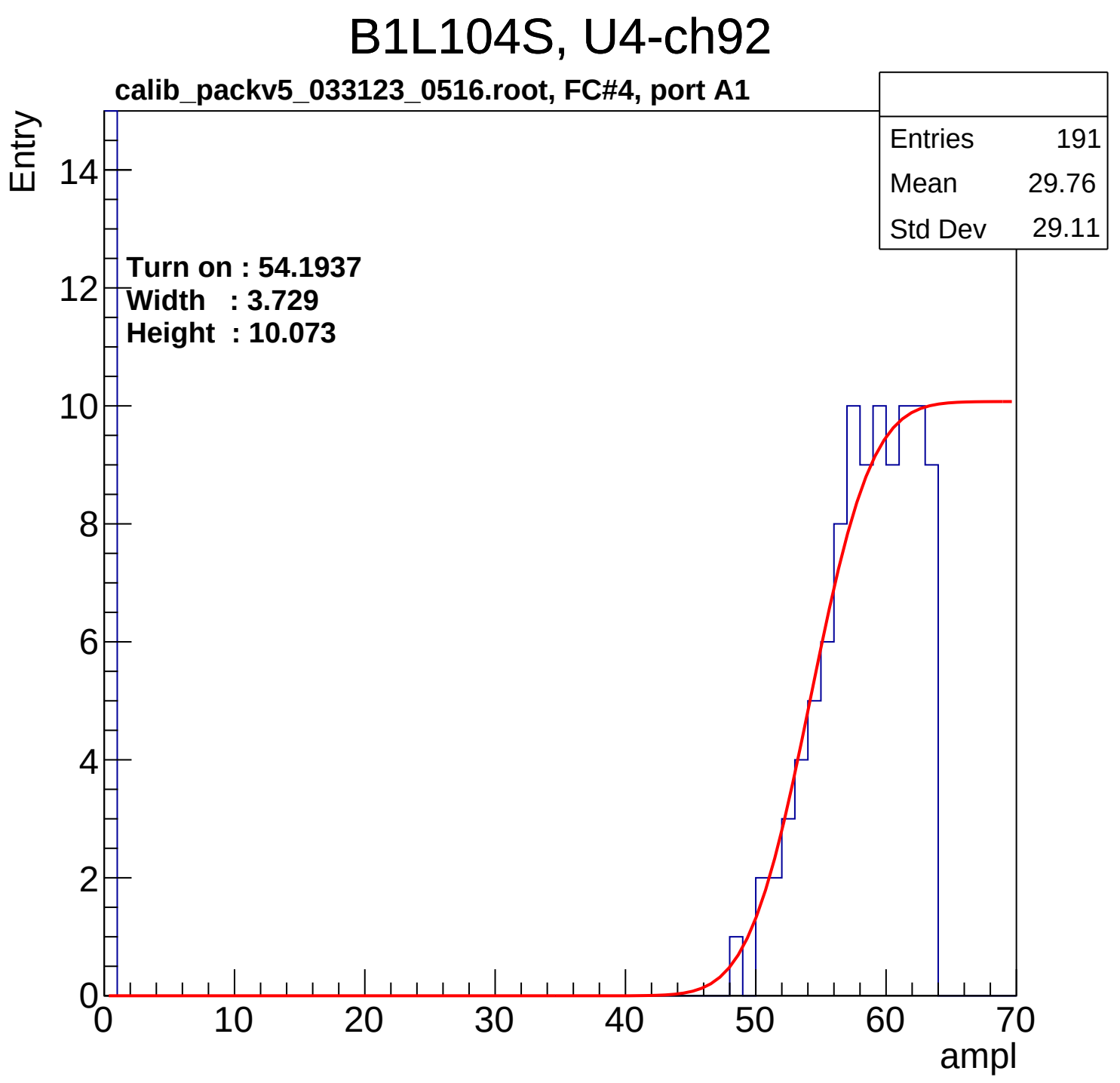

B1L104S, U4-ch87
calib_packv5_033123_0516.root, FC#4, port A1
Entries 190
Mean 29.29
Std Dev 29.11
Turn on : 55.2385
Width : 4.697
Height : 10.778
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

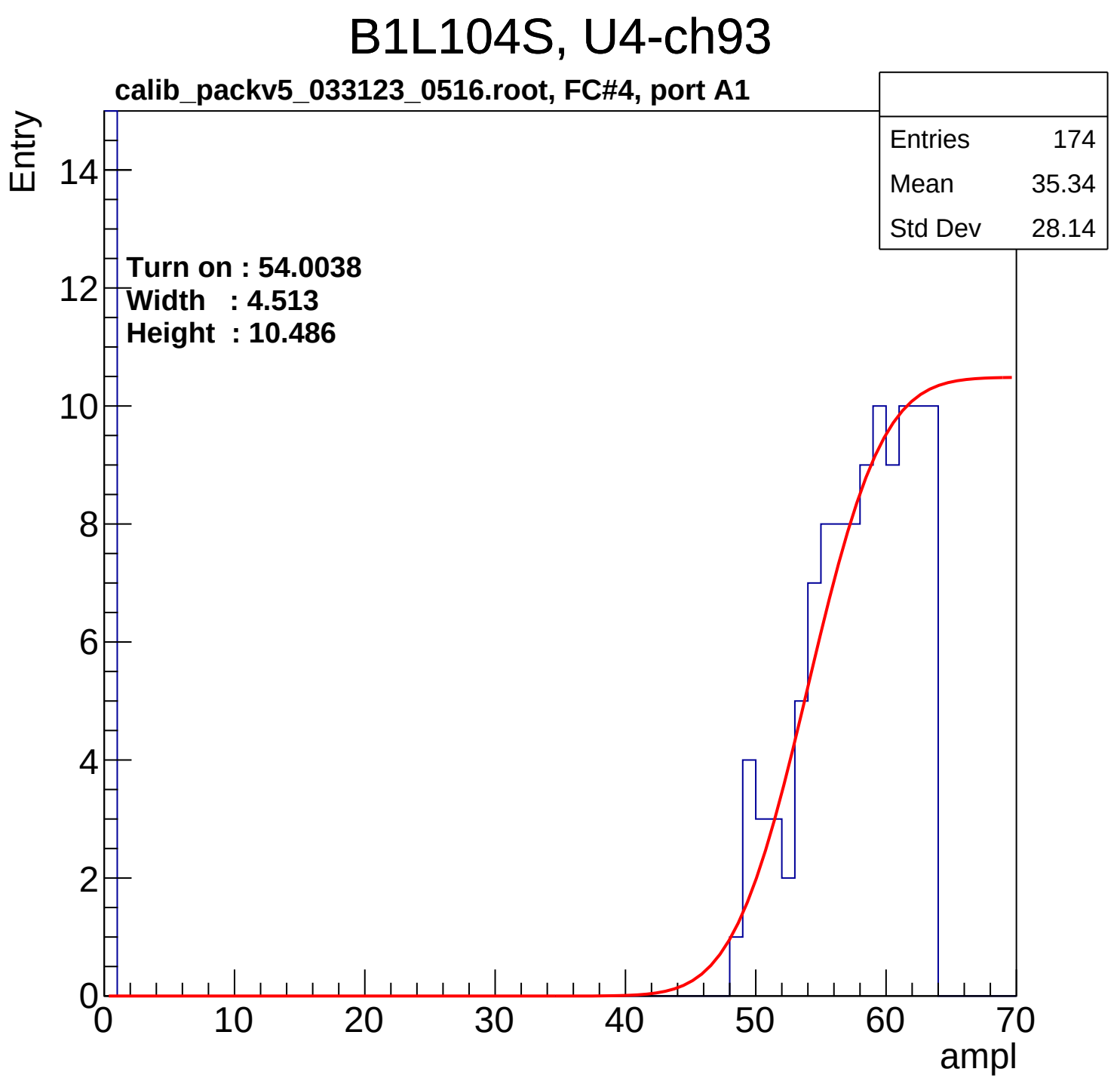

B1L104S, U4-ch88
calib_packv5_033123_0516.root, FC#4, port A1
Entries 231
Mean 32.34
Std Dev 28.19
Turn on : 51.1496
Width : 3.628
Height : 10.254
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

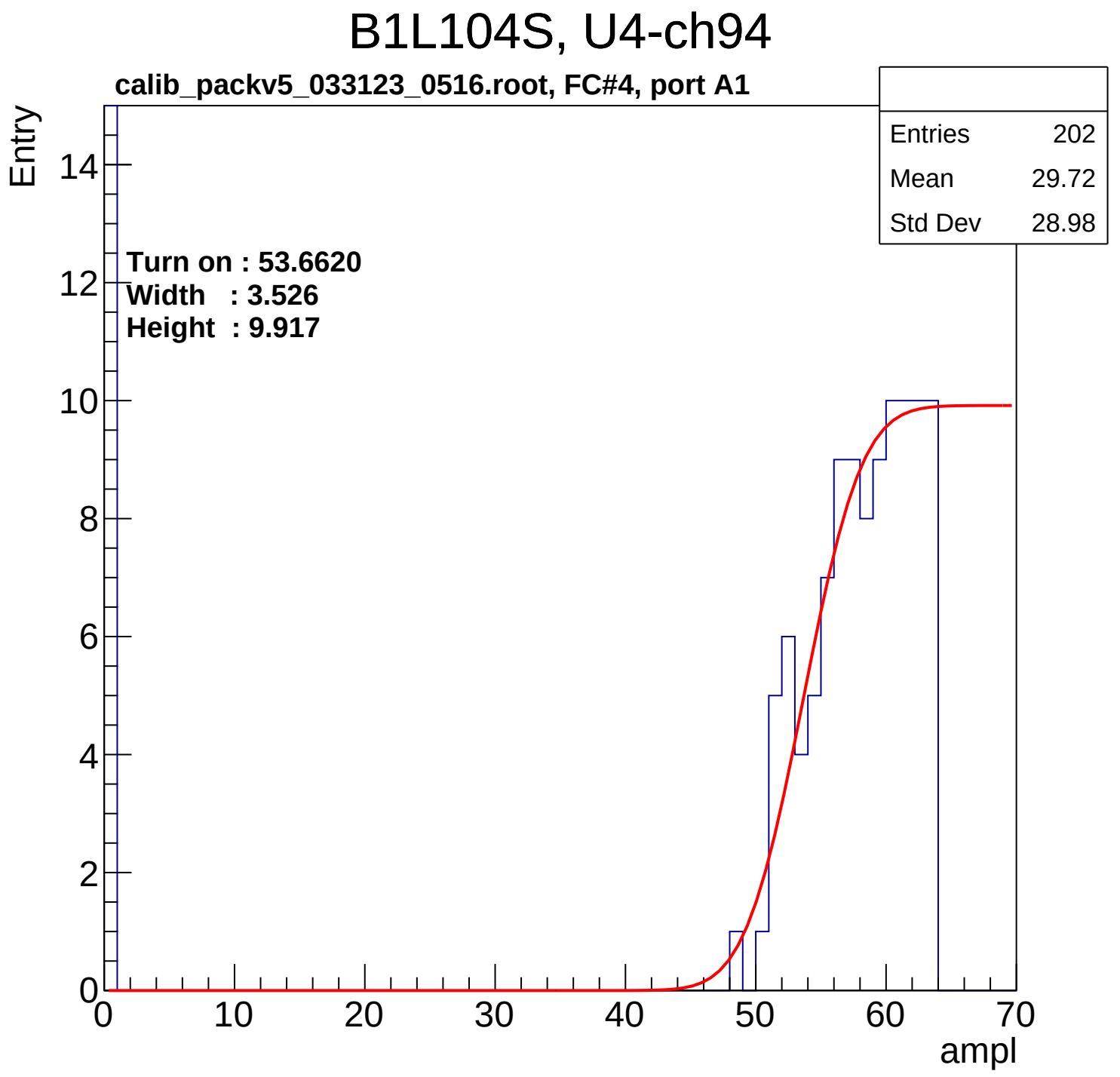

B1L104S, U4-ch89
calib_packv5_033123_0516.root, FC#4, port A1
Entries 170
Mean 40.89
Std Dev 25.89
Turn on : 52.1804
Width : 3.503
Height : 10.190
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

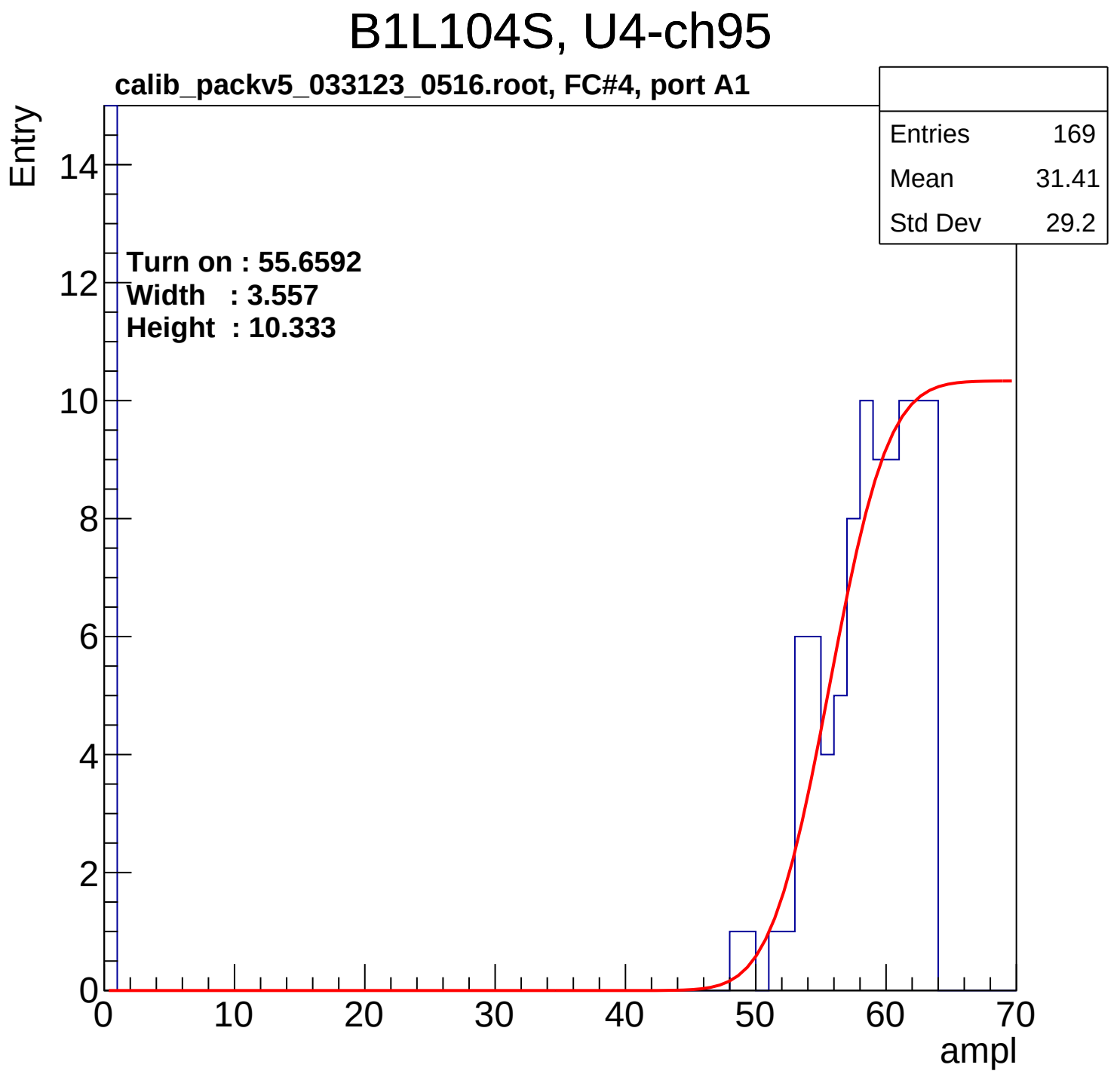

B1L104S, U4-ch90
calib_packv5_033123_0516.root, FC#4, port A1
Entries 182
Mean 32.09
Std Dev 28.87
Turn on : 54.5414
Width : 3.745
Height : 10.069
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

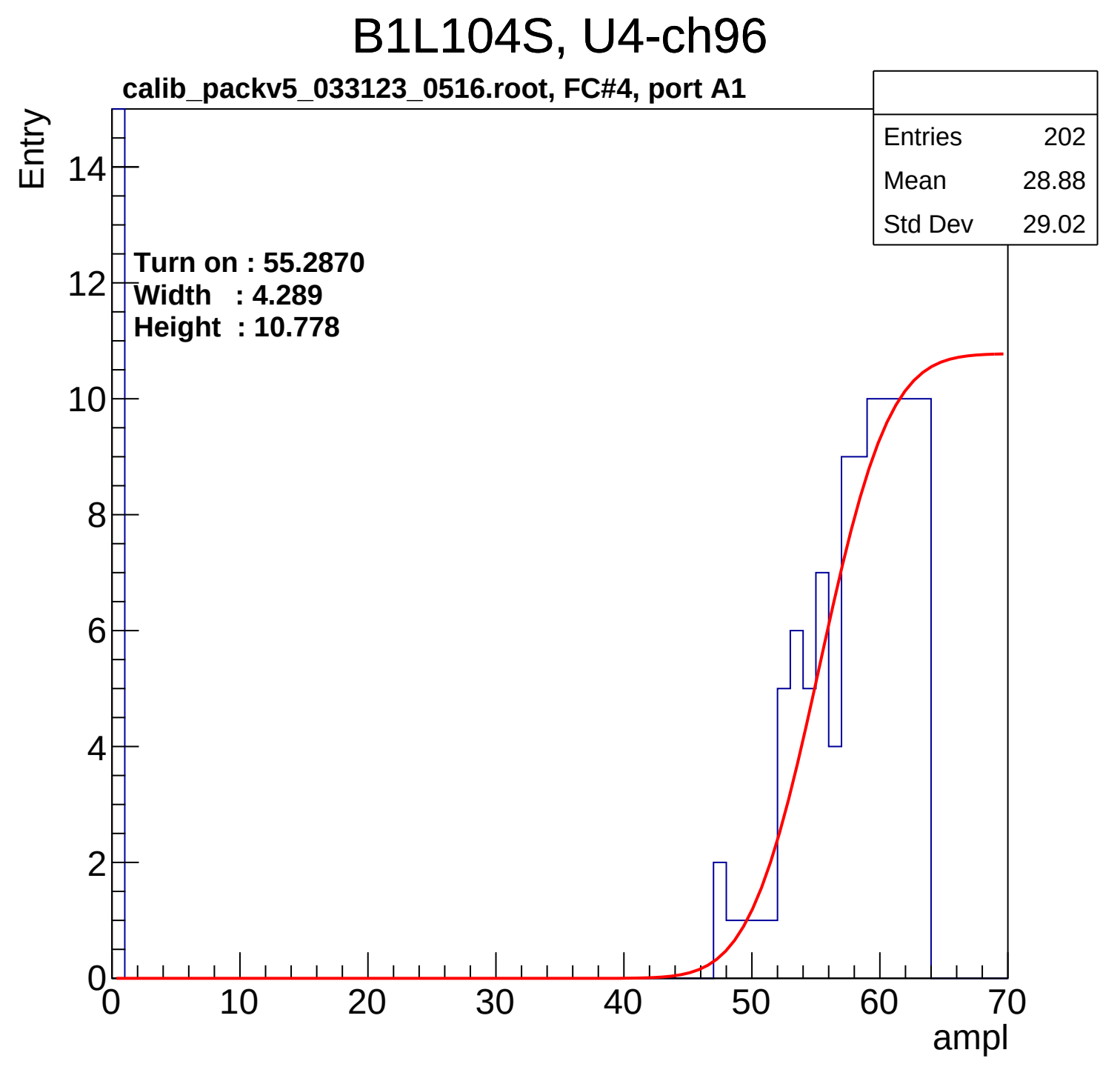

B1L104S, U4-ch91
calib_packv5_033123_0516.root, FC#4, port A1
Entries 193
Mean 32.99
Std Dev 28.51
Turn on : 52.8419
Width : 3.642
Height : 9.946
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

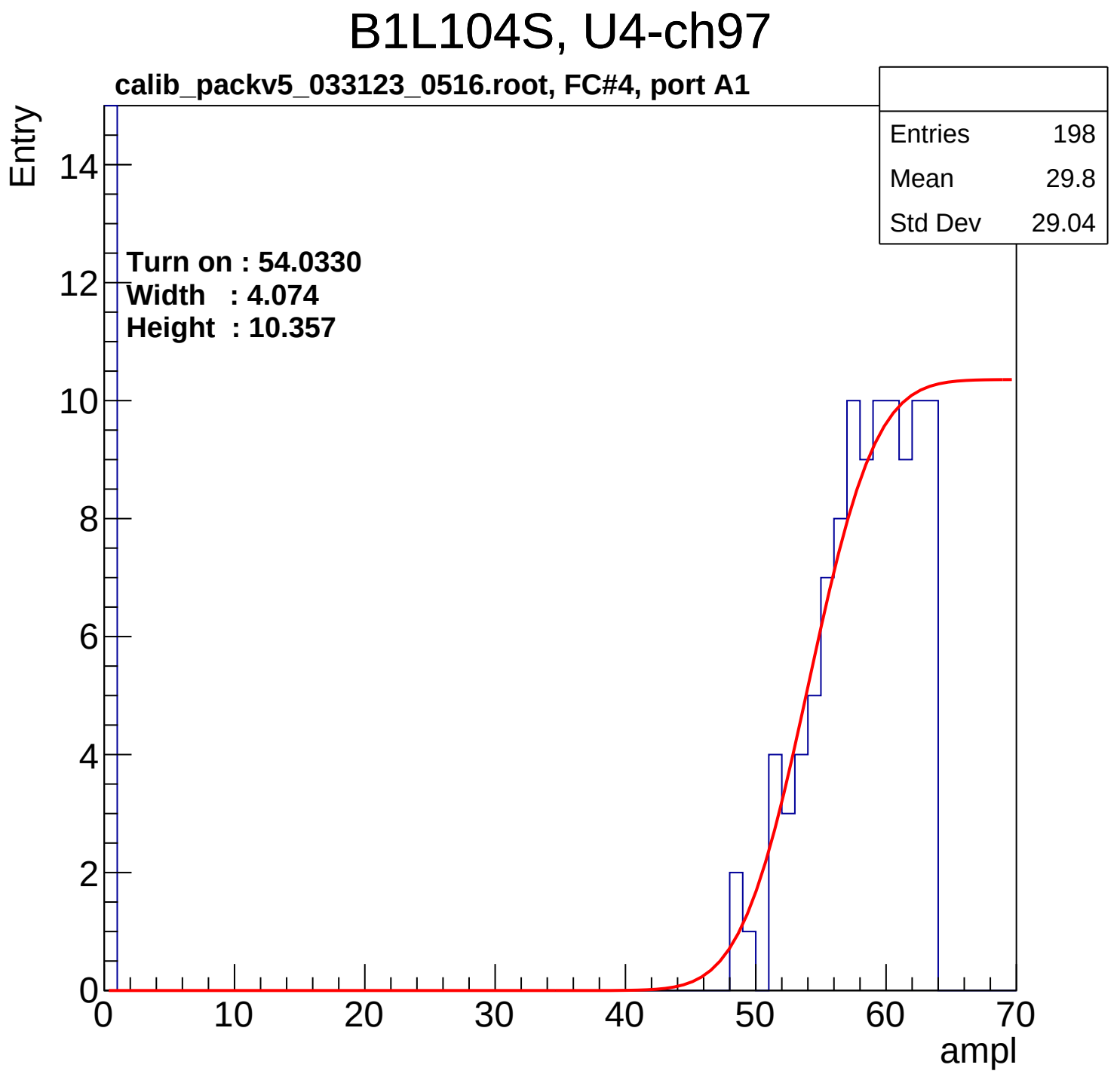

B1L104S, U4-ch92
calib_packv5_033123_0516.root, FC#4, port A1
Entries 191
Mean 29.76
Std Dev 29.11
Turn on : 54.1937
Width : 3.729
Height : 10.073
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

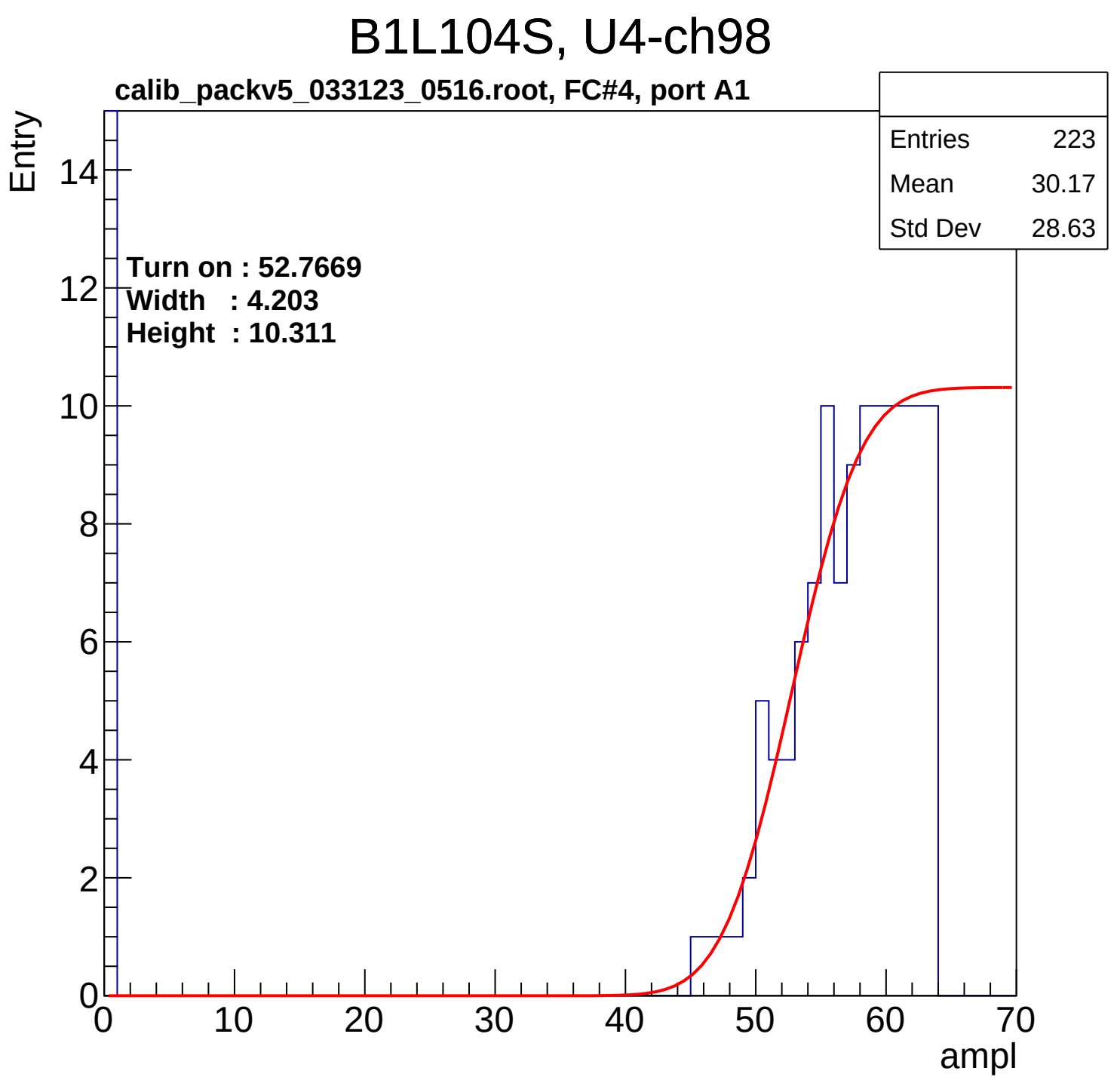

B1L104S, U4-ch93
calib_packv5_033123_0516.root, FC#4, port A1
Entries 174
Mean 35.34
Std Dev 28.14
Turn on : 54.0038
Width : 4.513
Height : 10.486
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

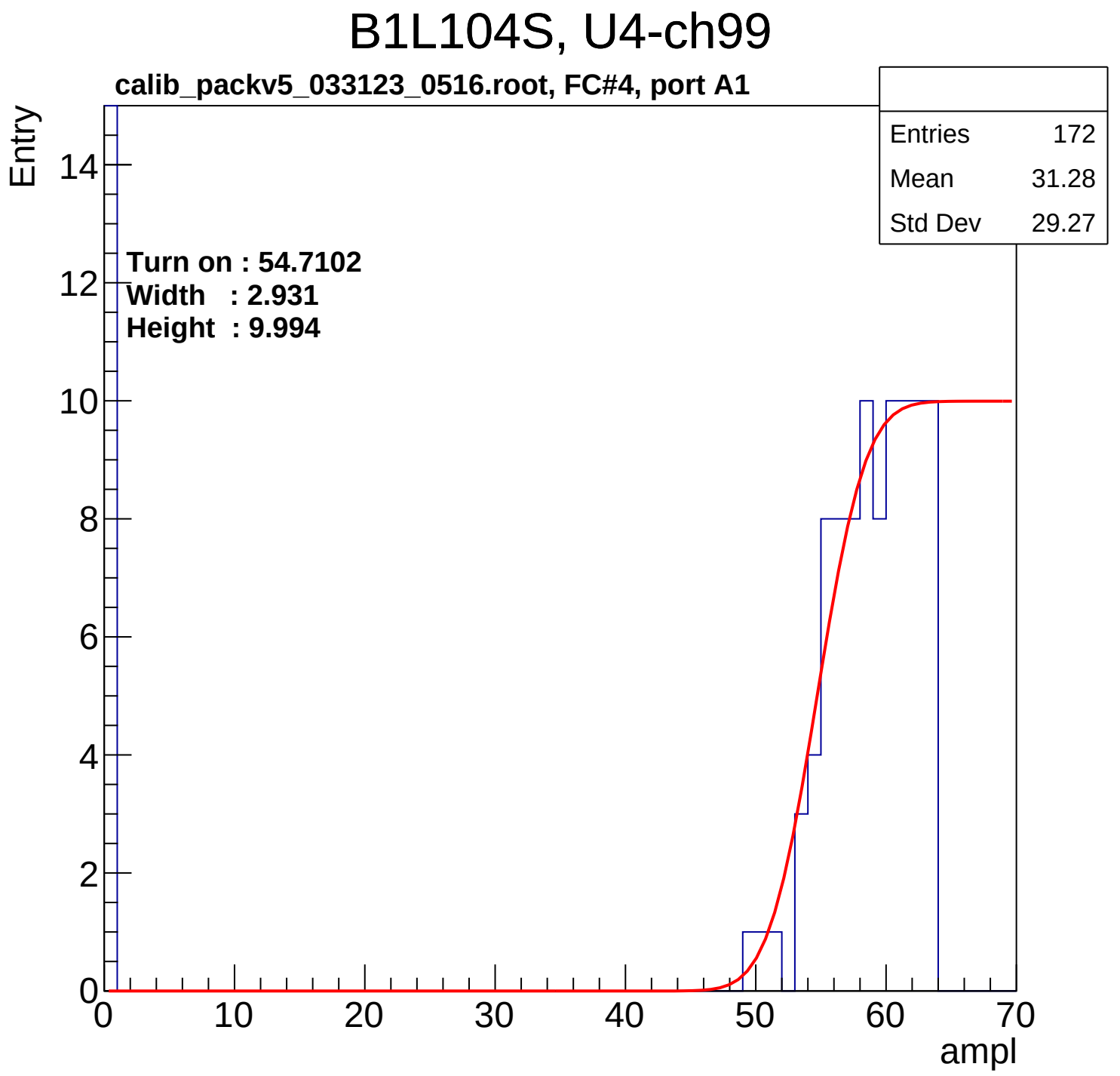

B1L104S, U4-ch94
calib_packv5_033123_0516.root, FC#4, port A1
Entries 202
Mean 29.72
Std Dev 28.98
Turn on : 53.6620
Width : 3.526
Height : 9.917
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

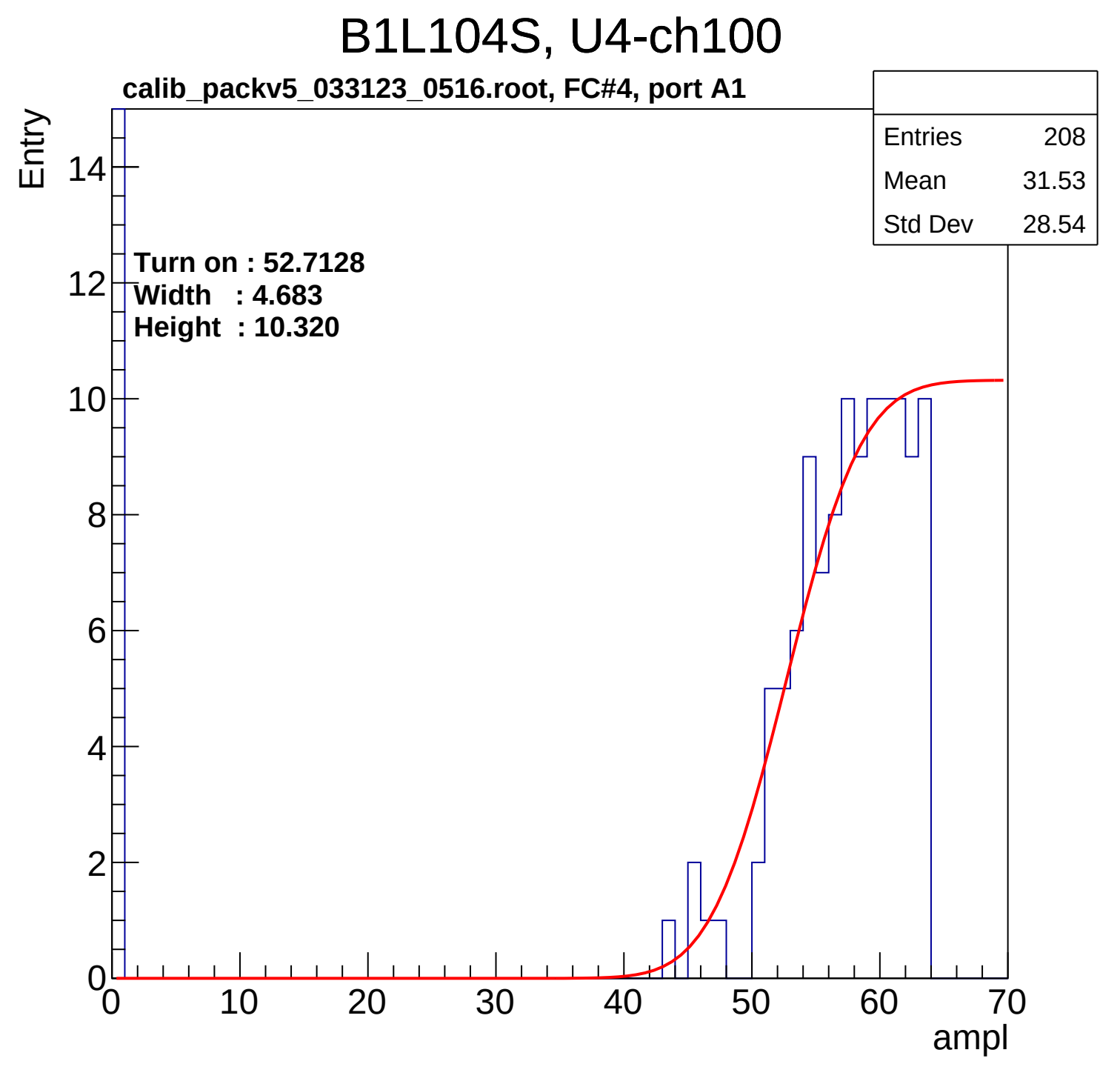

B1L104S, U4-ch95
calib_packv5_033123_0516.root, FC#4, port A1
Entries 169
Mean 31.41
Std Dev 29.2
Turn on : 55.6592
Width : 3.557
Height : 10.333
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

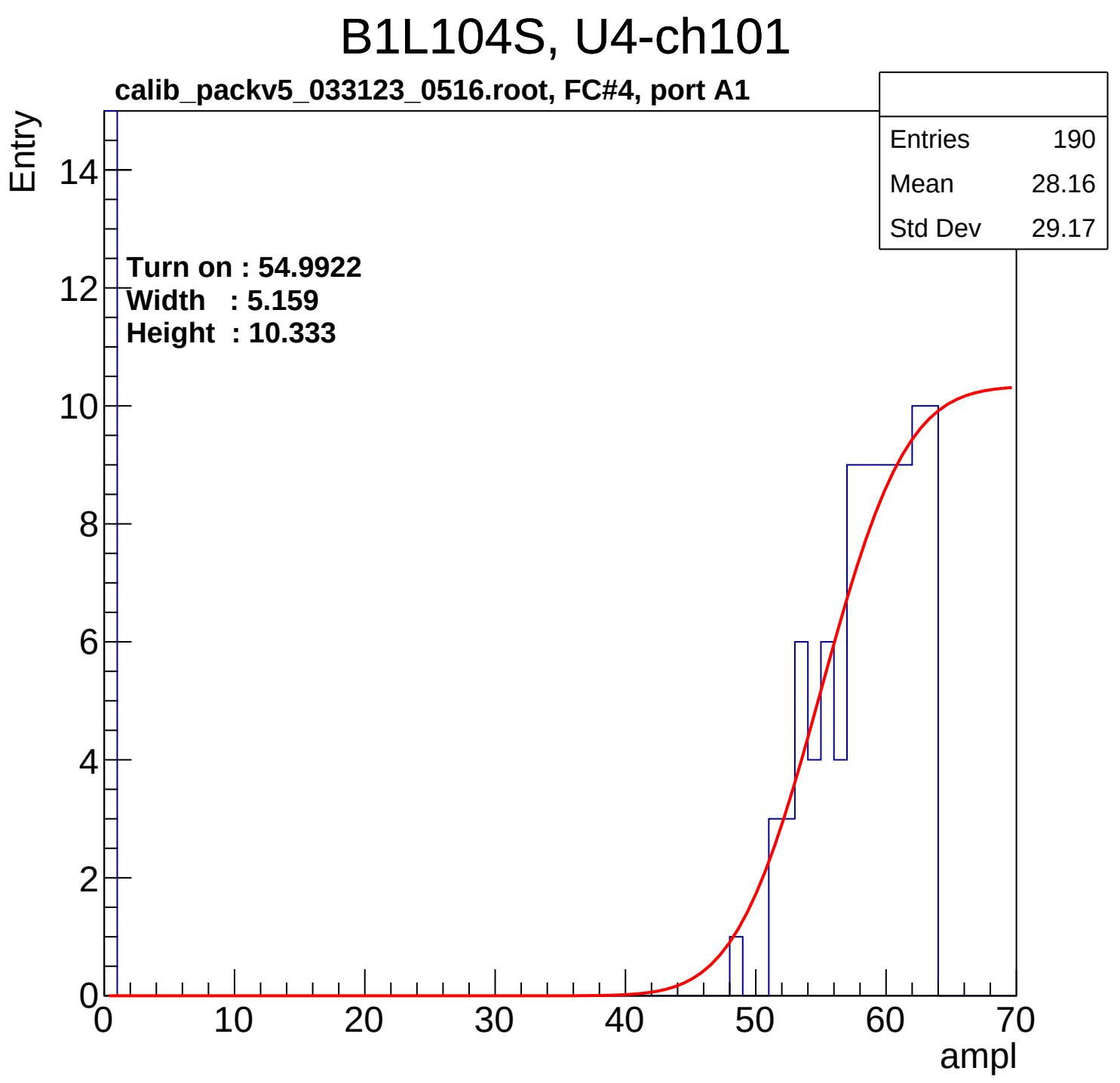

B1L104S, U4-ch96
calib_packv5_033123_0516.root, FC#4, port A1
Entries 202
Mean 28.88
Std Dev 29.02
Turn on : 55.2870
Width : 4.289
Height : 10.778
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

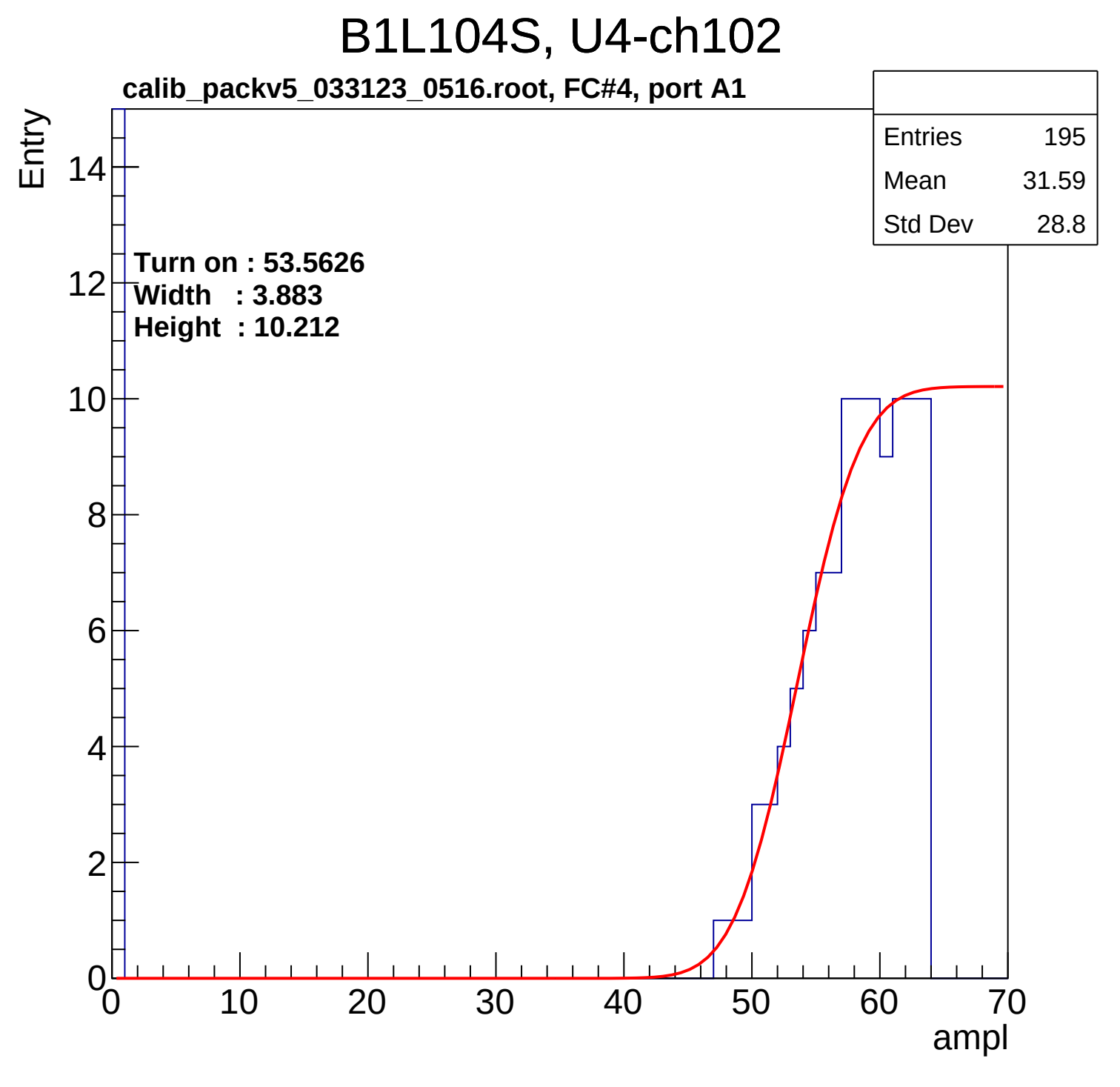

B1L104S, U4-ch97
calib_packv5_033123_0516.root, FC#4, port A1
Entries 198
Mean 29.8
Std Dev 29.04
Turn on : 54.0330
Width : 4.074
Height : 10.357
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

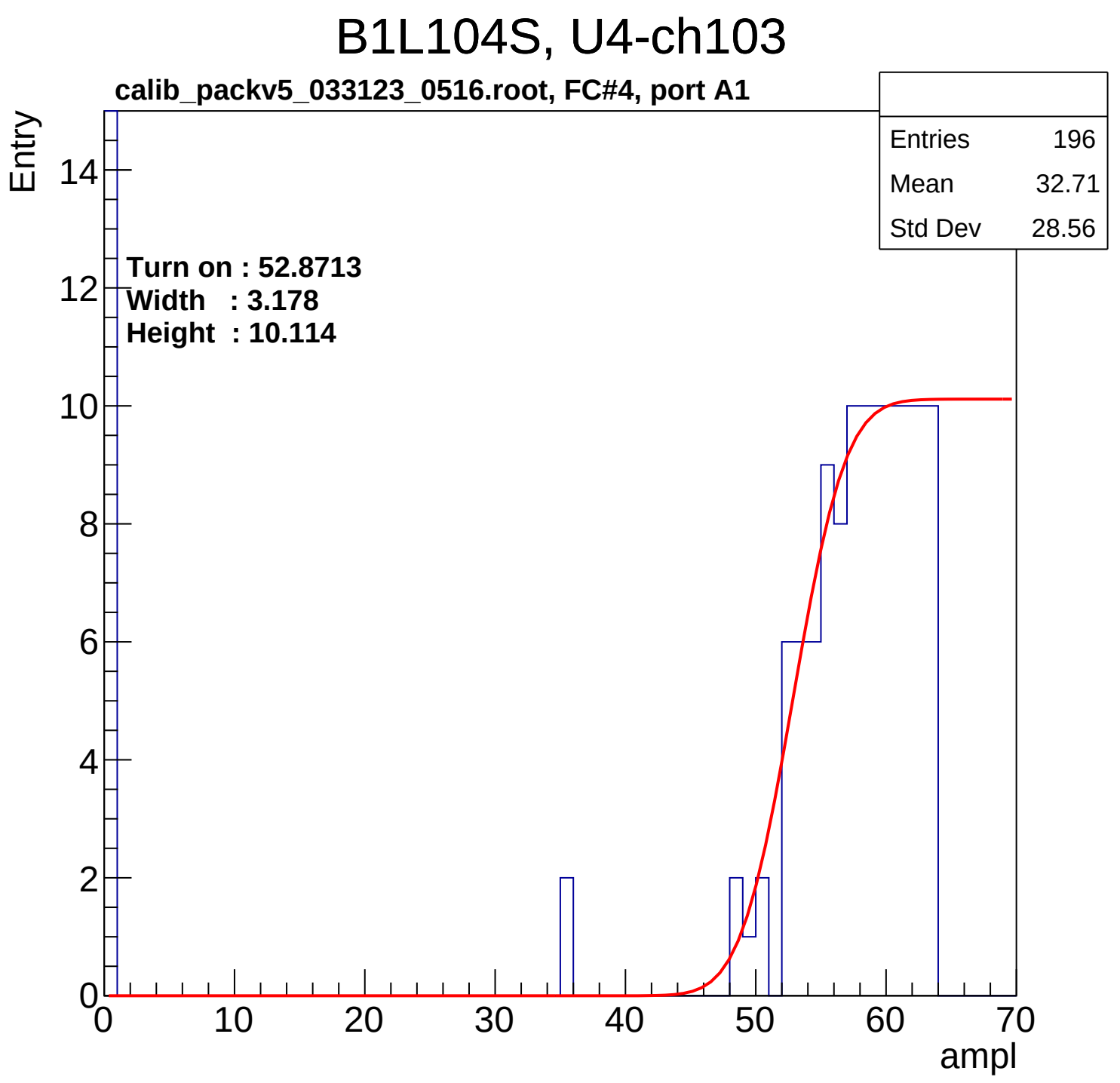

B1L104S, U4-ch98
calib_packv5_033123_0516.root, FC#4, port A1
Entries 223
Mean 30.17
Std Dev 28.63
Turn on : 52.7669
Width : 4.203
Height : 10.311
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

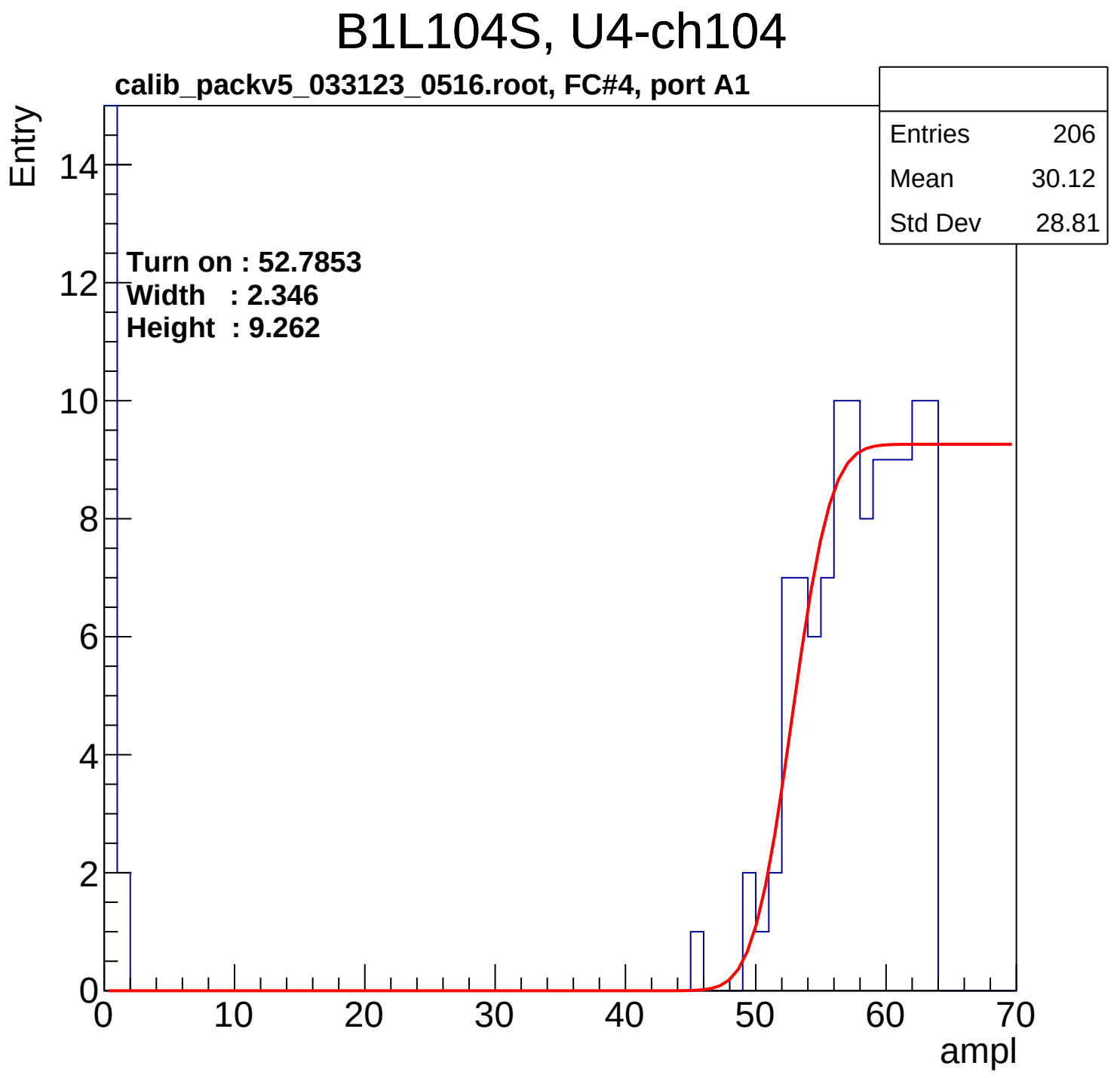

B1L104S, U4-ch99
calib_packv5_033123_0516.root, FC#4, port A1
Entries 172
Mean 31.28
Std Dev 29.27
Turn on : 54.7102
Width : 2.931
Height : 9.994
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

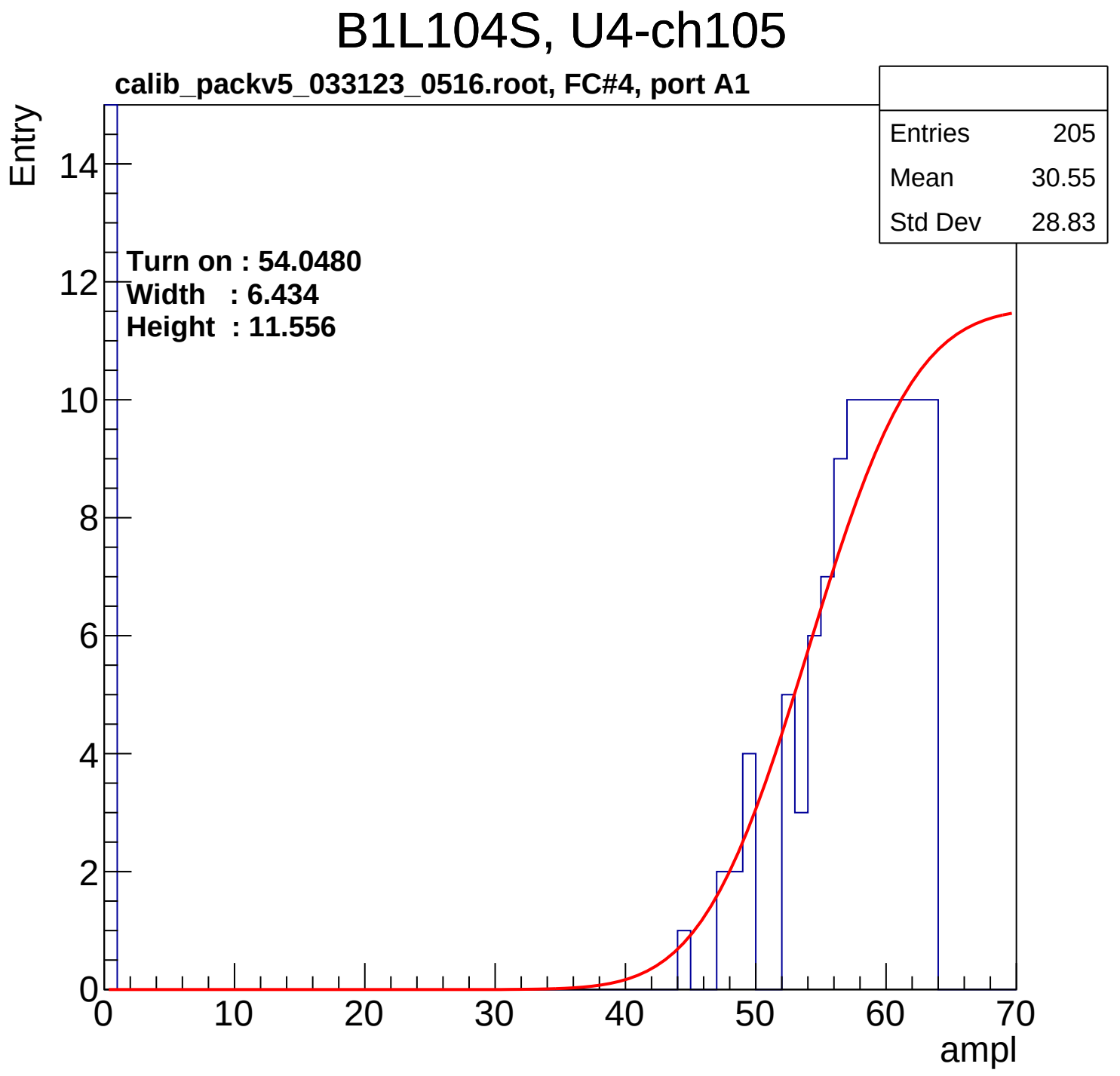

B1L104S, U4-ch100
calib_packv5_033123_0516.root, FC#4, port A1
Entries 208
Mean 31.53
Std Dev 28.54
Turn on : 52.7128
Width : 4.683
Height : 10.320
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

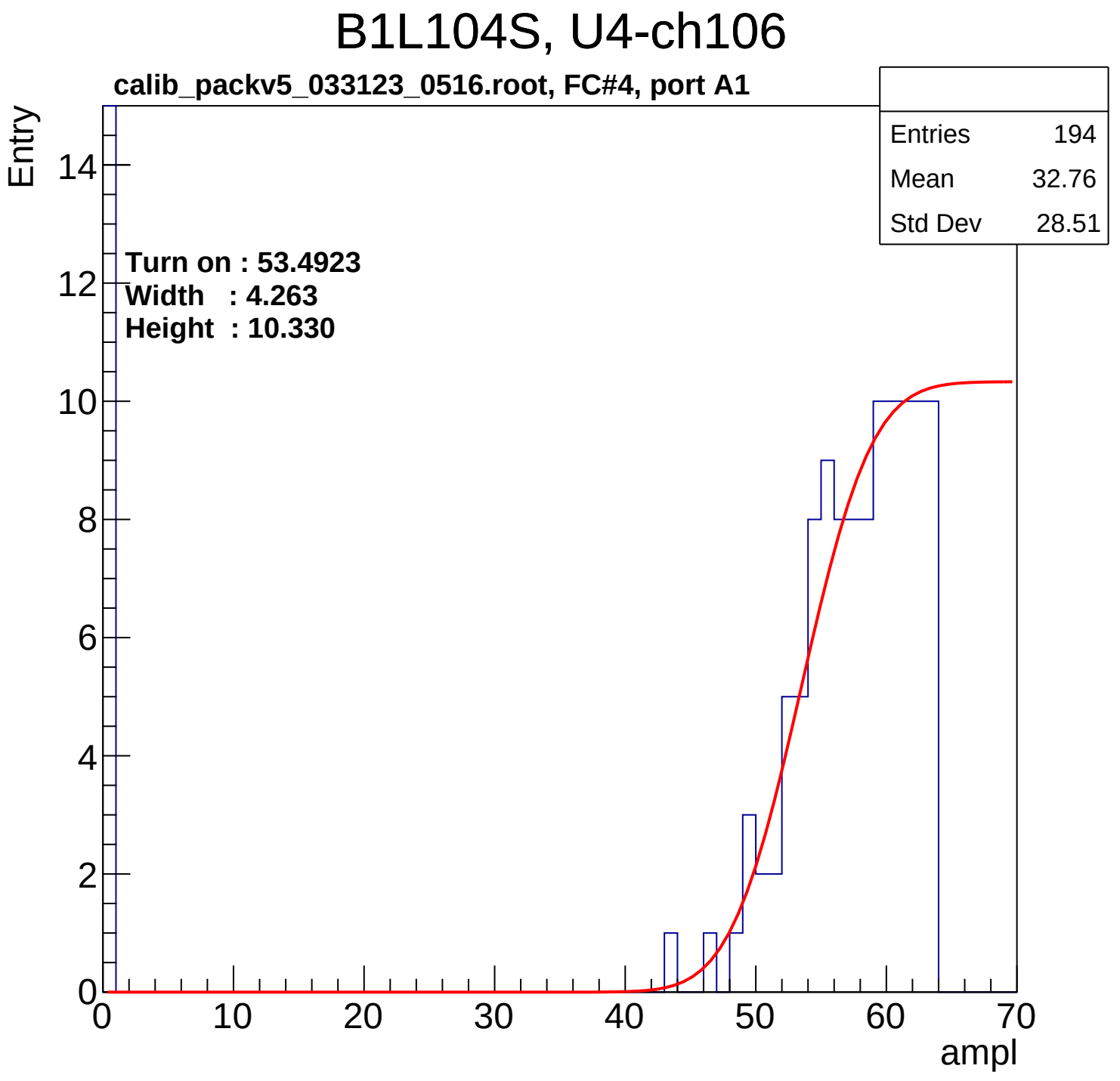

B1L104S, U4-ch101
calib_packv5_033123_0516.root, FC#4, port A1
Entries 190
Mean 28.16
Std Dev 29.17
Turn on : 54.9922
Width : 5.159
Height : 10.333
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

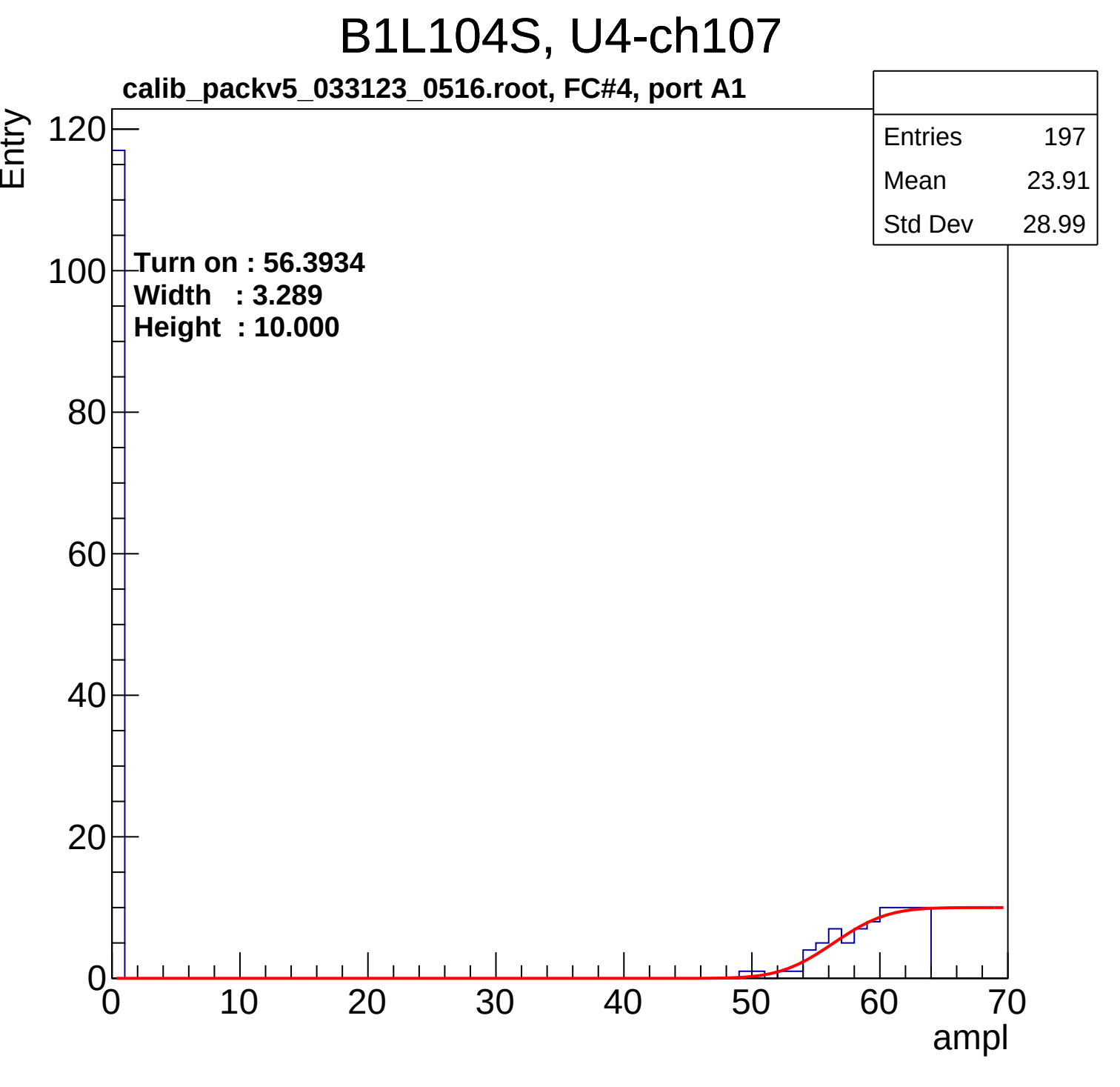

B1L104S, U4-ch102
calib_packv5_033123_0516.root, FC#4, port A1
Entries 195
Mean 31.59
Std Dev 28.8
Turn on : 53.5626
Width : 3.883
Height : 10.212
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

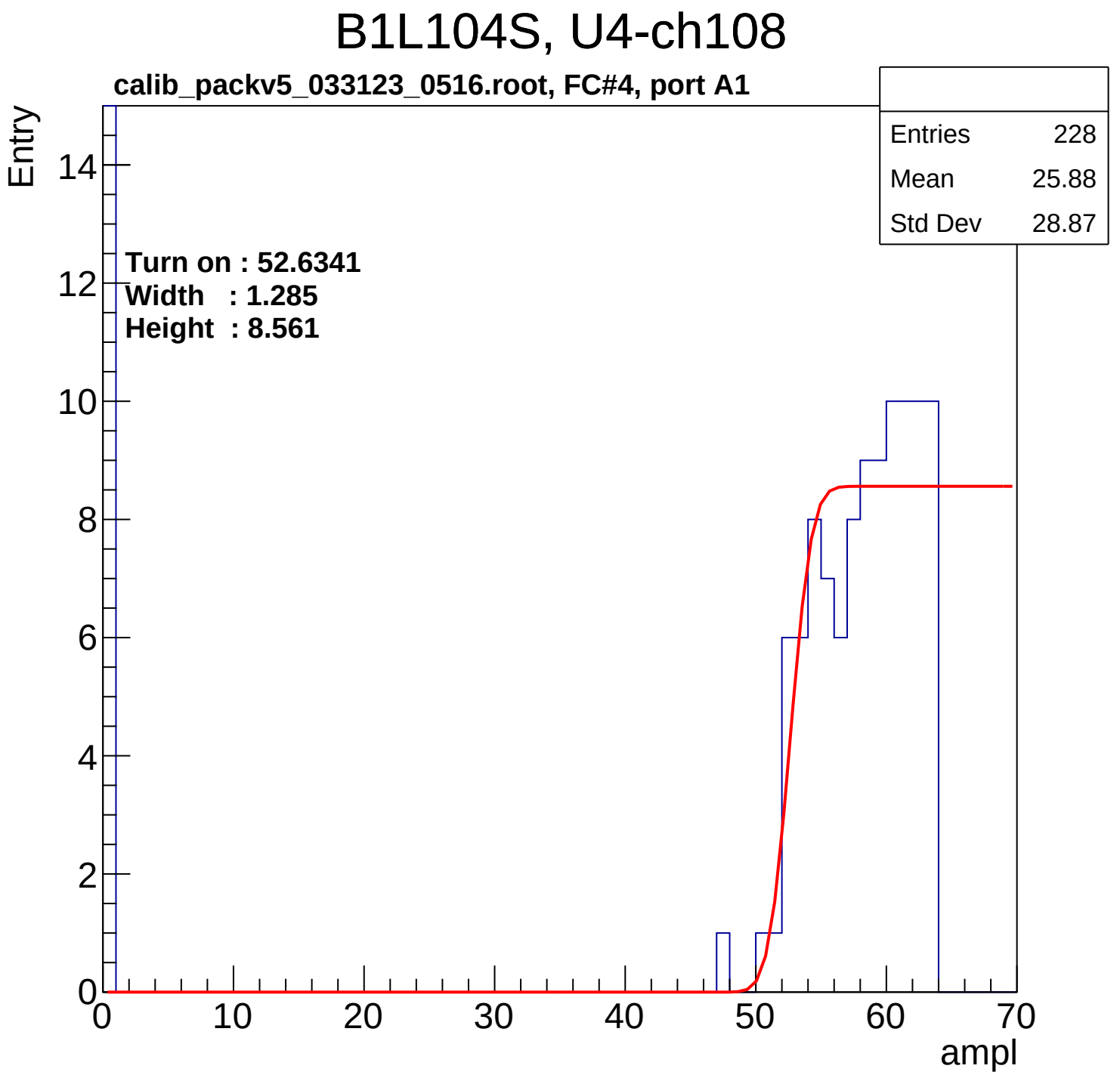

B1L104S, U4-ch103
calib_packv5_033123_0516.root, FC#4, port A1
Entries 196
Mean 32.71
Std Dev 28.56
Turn on : 52.8713
Width : 3.178
Height : 10.114
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

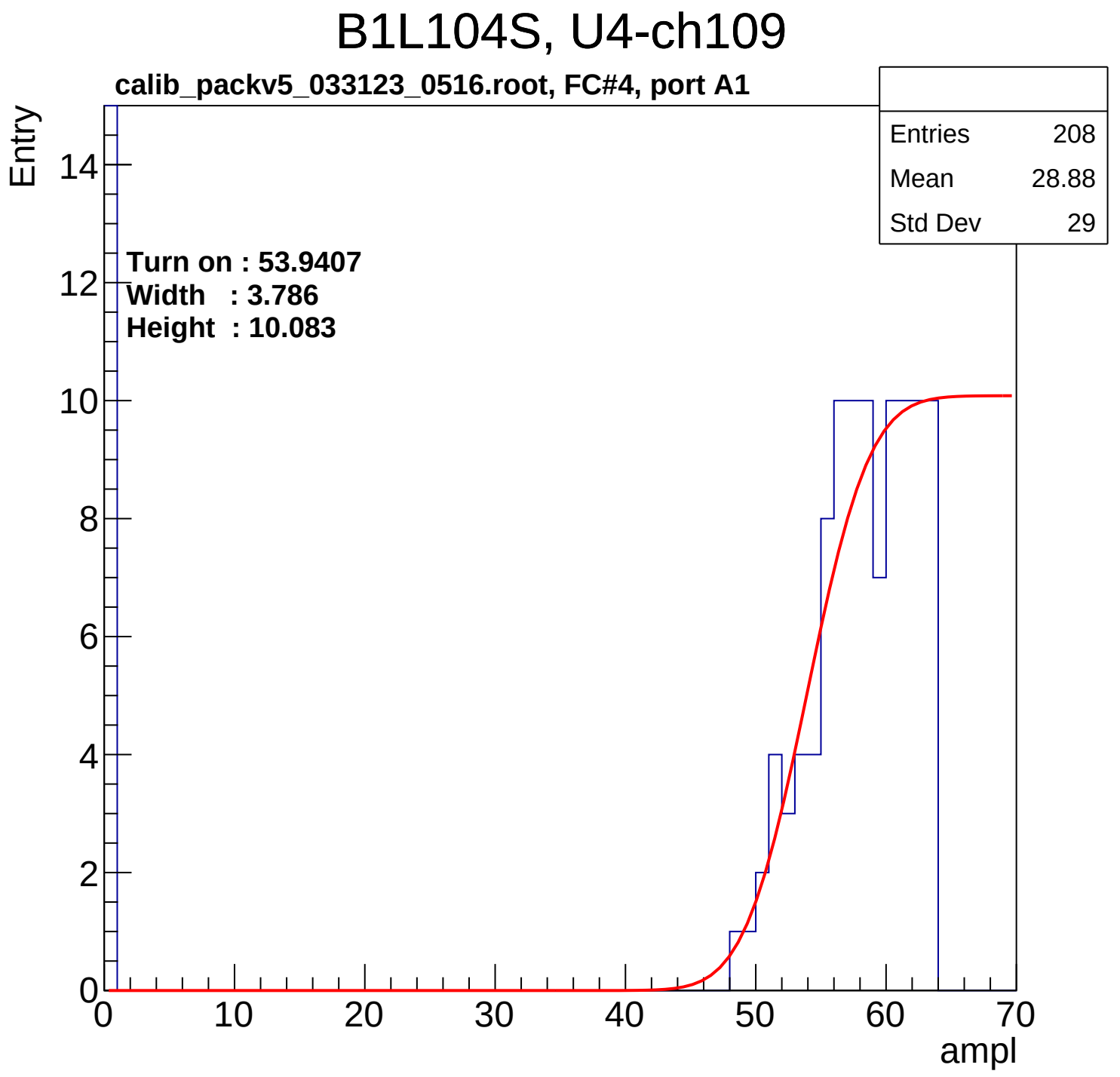

B1L104S, U4-ch104
calib_packv5_033123_0516.root, FC#4, port A1
Entries 206
Mean 30.12
Std Dev 28.81
Turn on : 52.7853
Width : 2.346
Height : 9.262
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

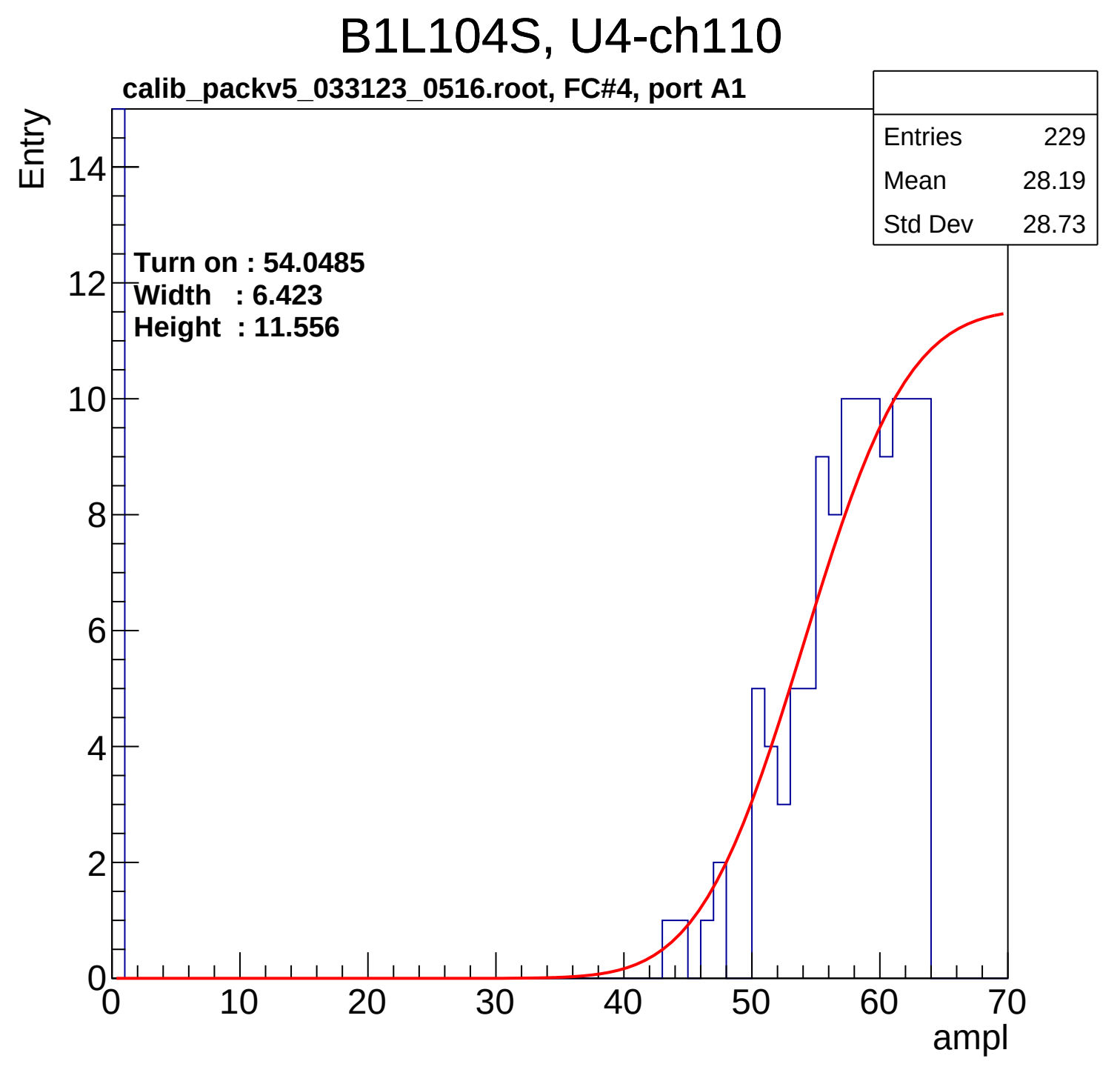

B1L104S, U4-ch105
calib_packv5_033123_0516.root, FC#4, port A1
Entries 205
Mean 30.55
Std Dev 28.83
Turn on : 54.0480
Width : 6.434
Height : 11.556
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

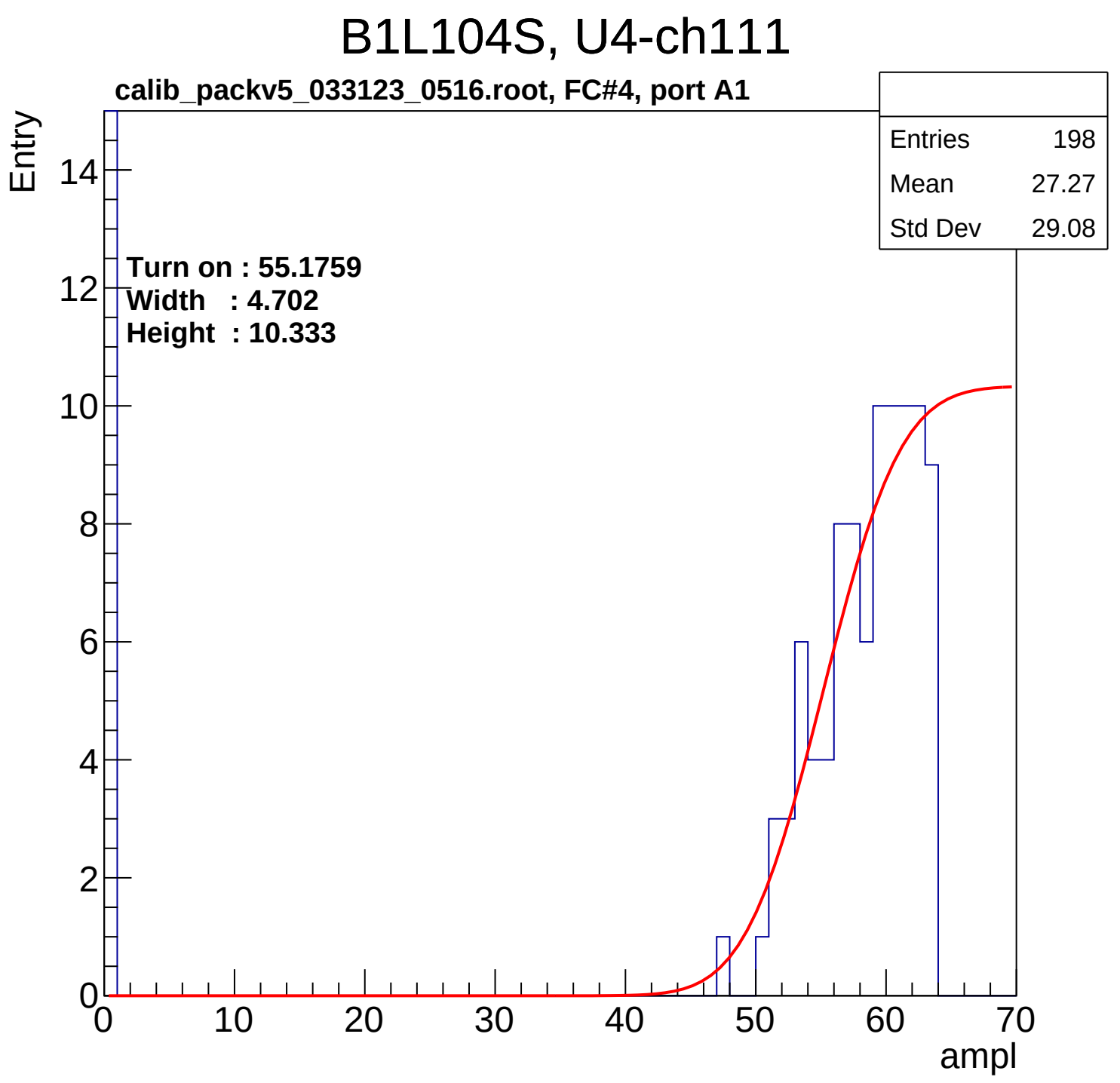

B1L104S, U4-ch106
calib_packv5_033123_0516.root, FC#4, port A1
Entries 194
Mean 32.76
Std Dev 28.51
Turn on : 53.4923
Width : 4.263
Height : 10.330
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

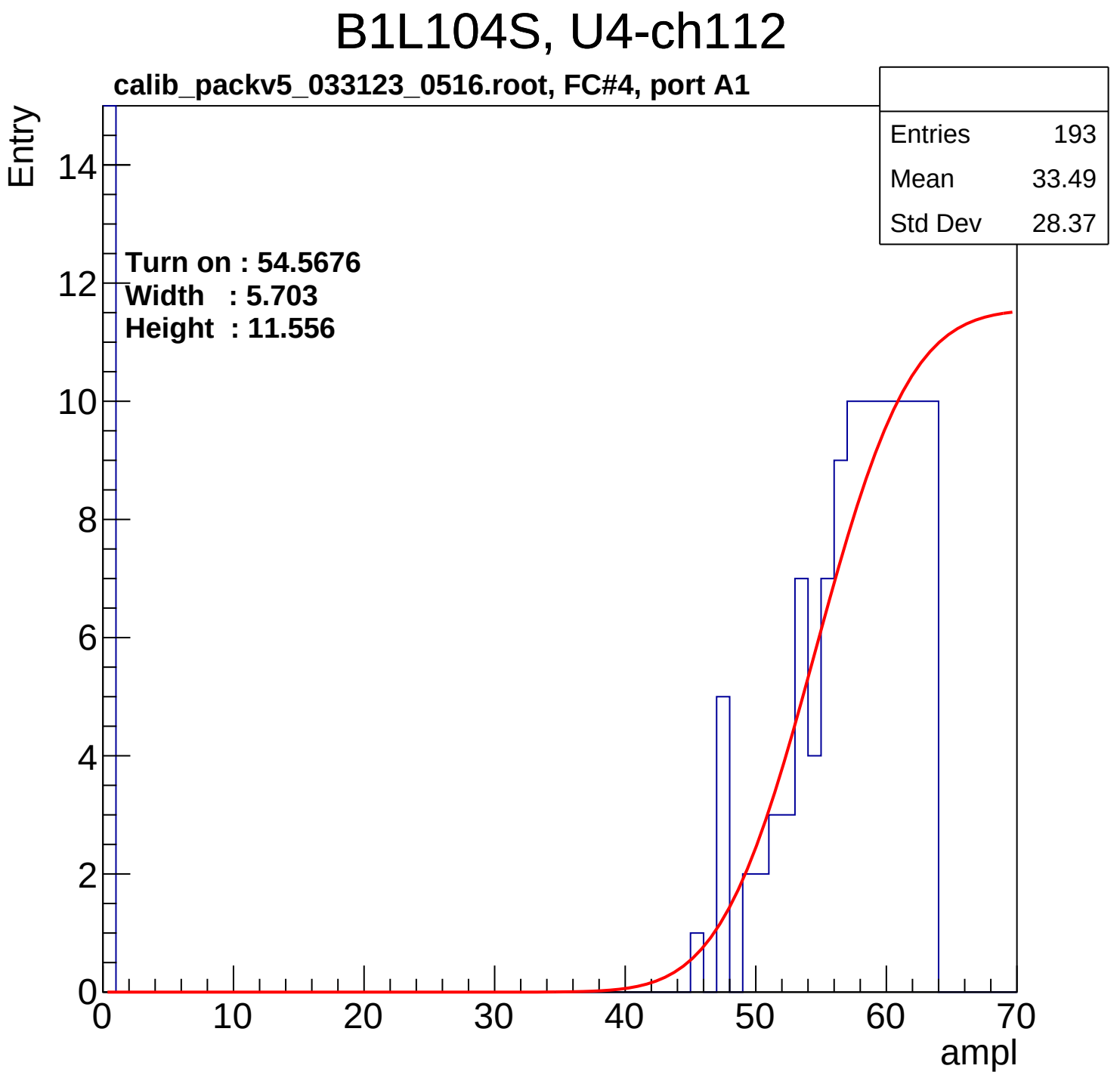

B1L104S, U4-ch107
calib_packv5_033123_0516.root, FC#4, port A1
Entries 197
Mean 23.91
Std Dev 28.99
Turn on : 56.3934
Width : 3.289
Height : 10.000
Entry
ampl
0
20
40
60
80
100
120
0
10
20
30
40
50
60
70

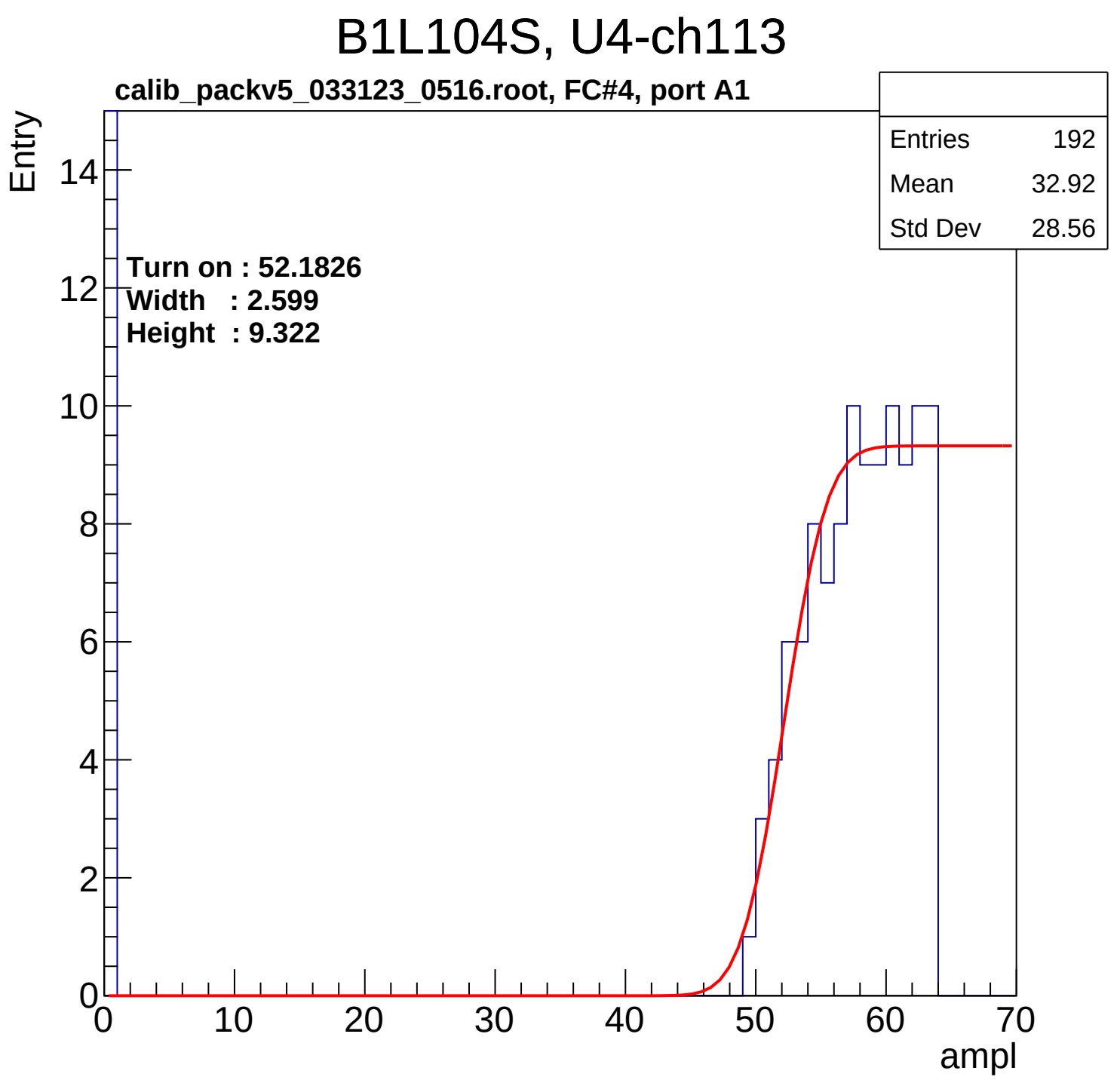

B1L104S, U4-ch108
calib_packv5_033123_0516.root, FC#4, port A1
Entries 228
Mean 25.88
Std Dev 28.87
Turn on : 52.6341
Width : 1.285
Height : 8.561
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

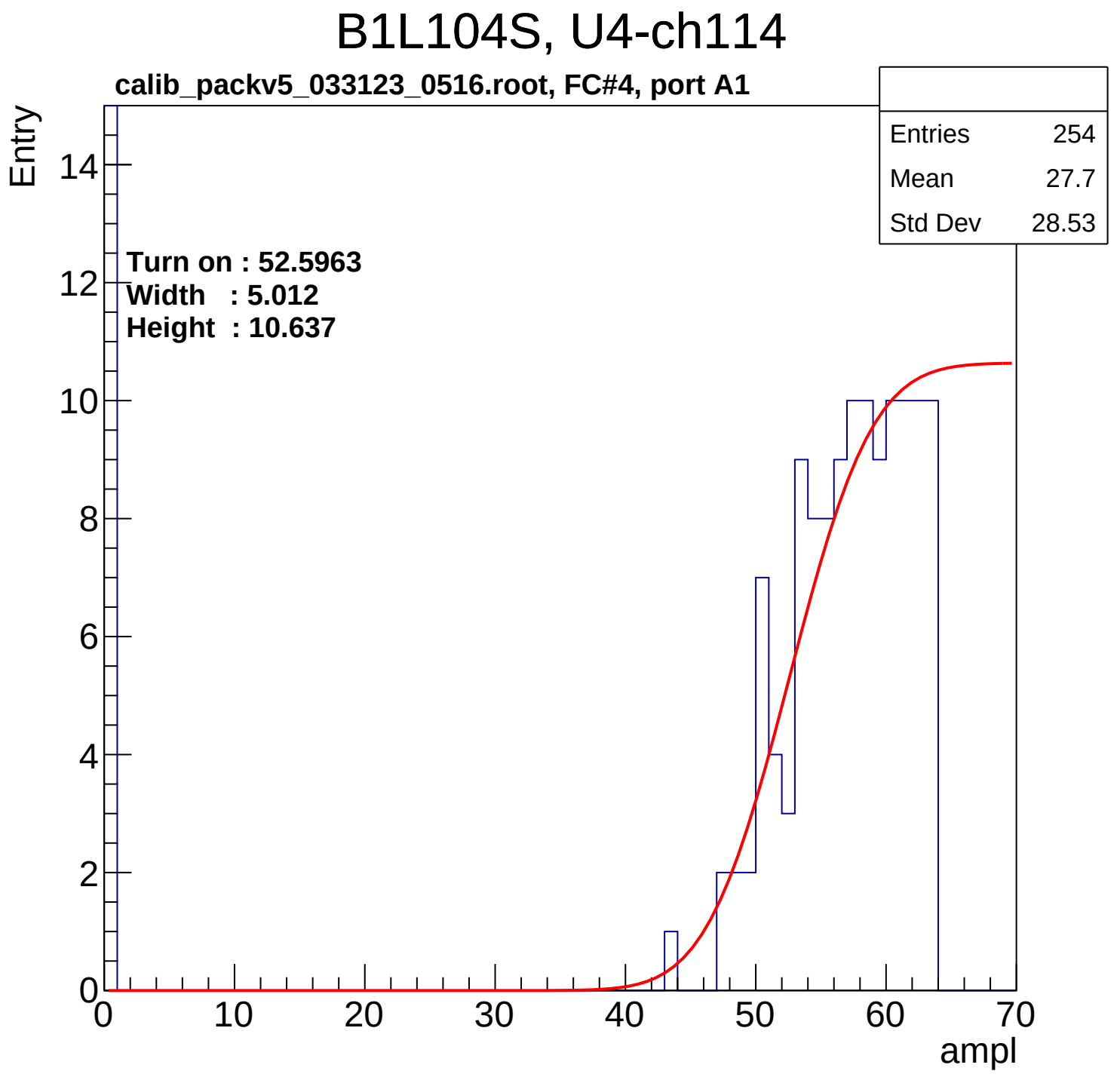

B1L104S, U4-ch109
calib_packv5_033123_0516.root, FC#4, port A1
Entries 208
Mean 28.88
Std Dev 29
Turn on : 53.9407
Width : 3.786
Height : 10.083
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

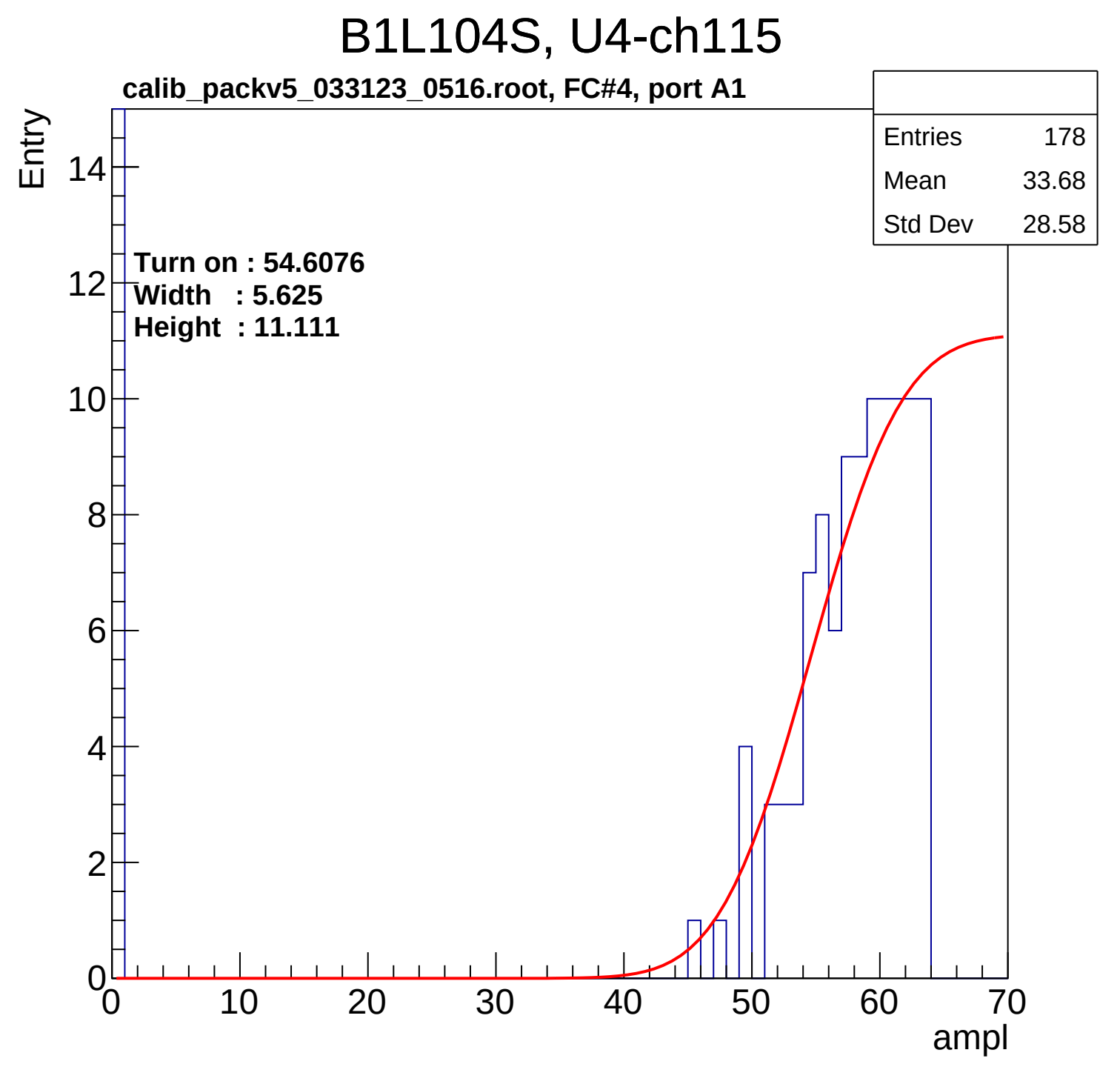

B1L104S, U4-ch110
calib_packv5_033123_0516.root, FC#4, port A1
Entries 229
Mean 28.19
Std Dev 28.73
Turn on : 54.0485
Width : 6.423
Height : 11.556
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

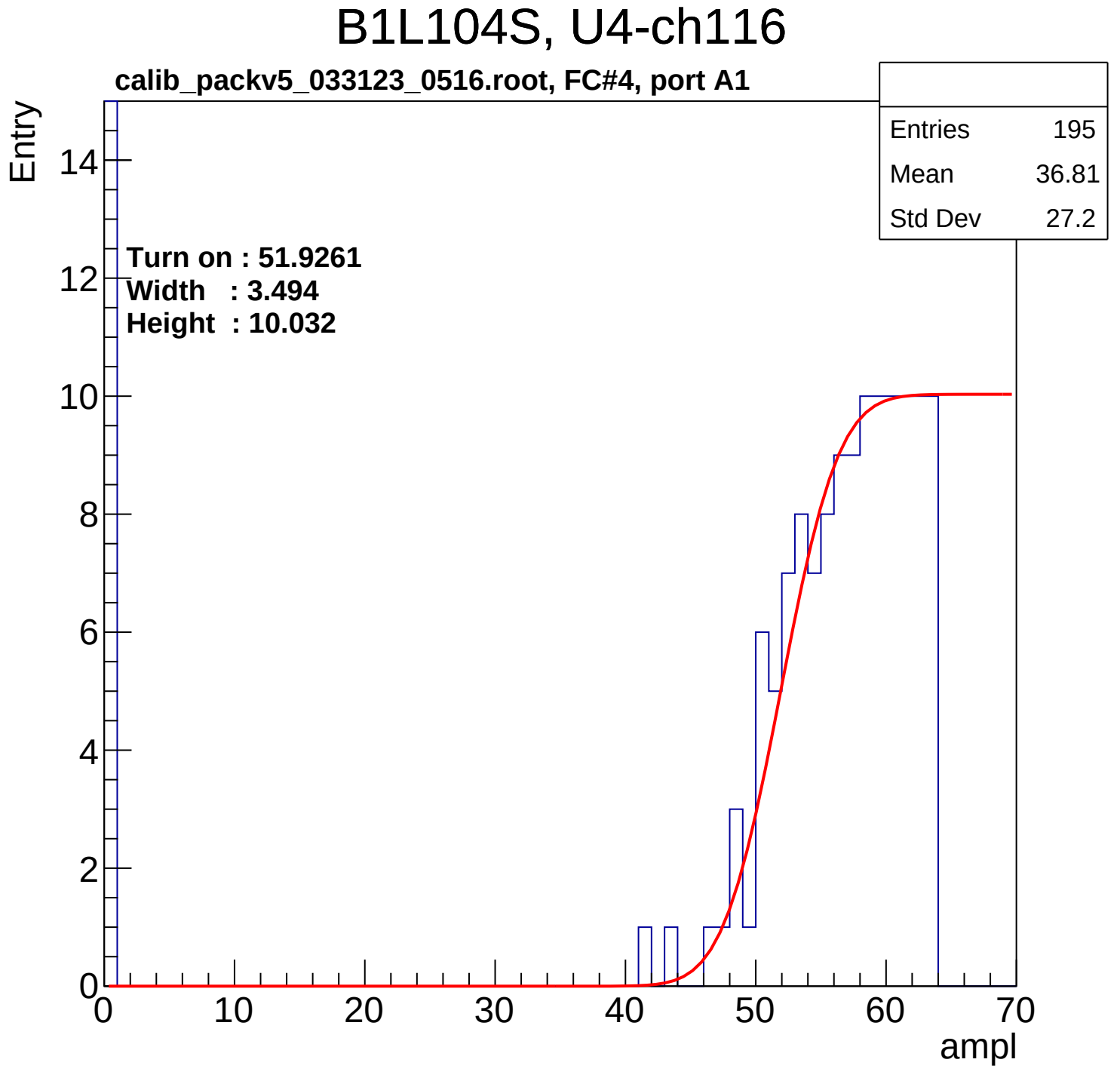

B1L104S, U4-ch111
calib_packv5_033123_0516.root, FC#4, port A1
Entries 198
Mean 27.27
Std Dev 29.08
Turn on : 55.1759
Width : 4.702
Height : 10.333
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

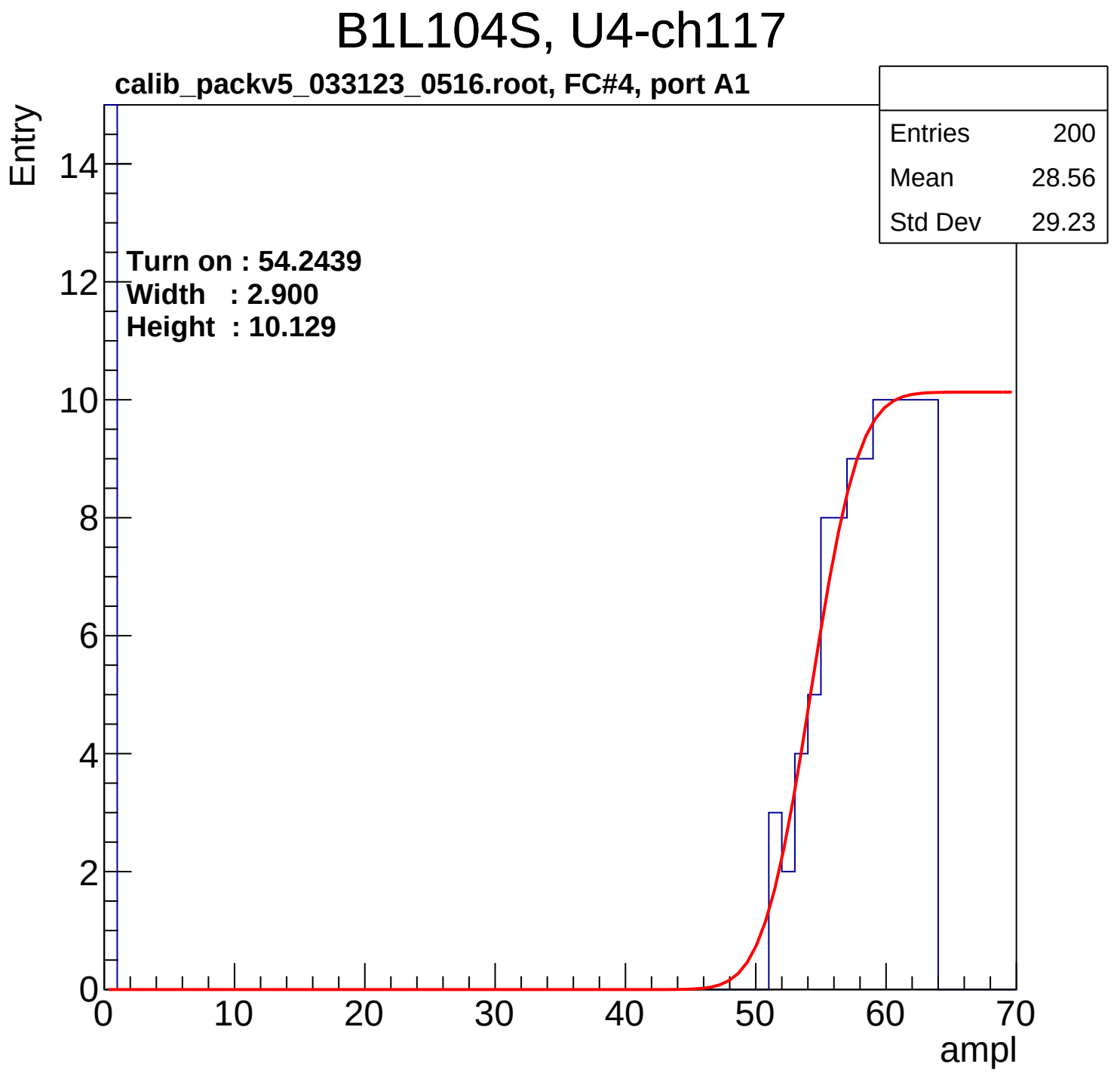

B1L104S, U4-ch112
calib_packv5_033123_0516.root, FC#4, port A1
Entries 193
Mean 33.49
Std Dev 28.37
Turn on : 54.5676
Width : 5.703
Height : 11.556
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

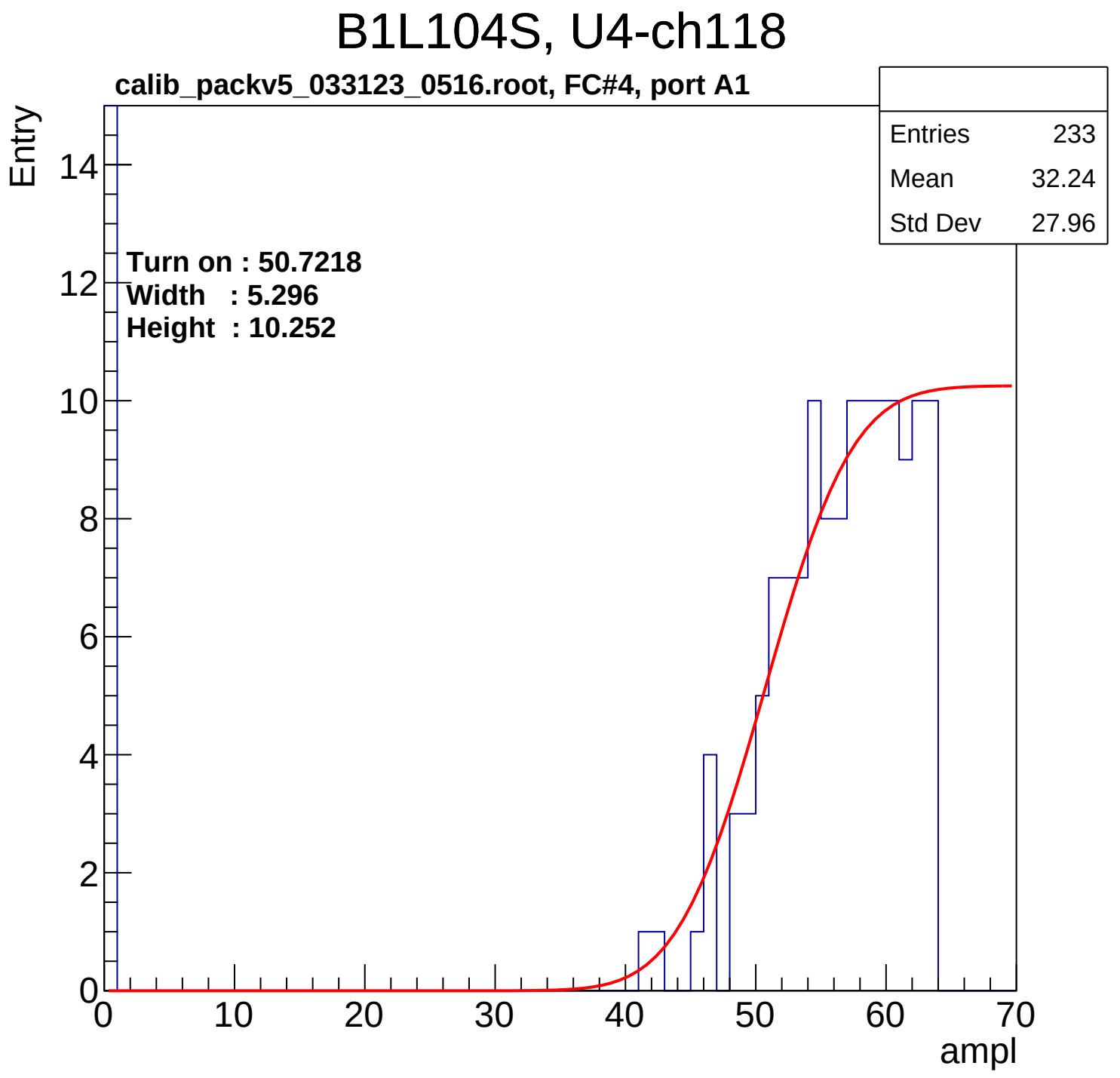

B1L104S, U4-ch113
calib_packv5_033123_0516.root, FC#4, port A1
Entries 192
Mean 32.92
Std Dev 28.56
Turn on : 52.1826
Width : 2.599
Height : 9.322
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

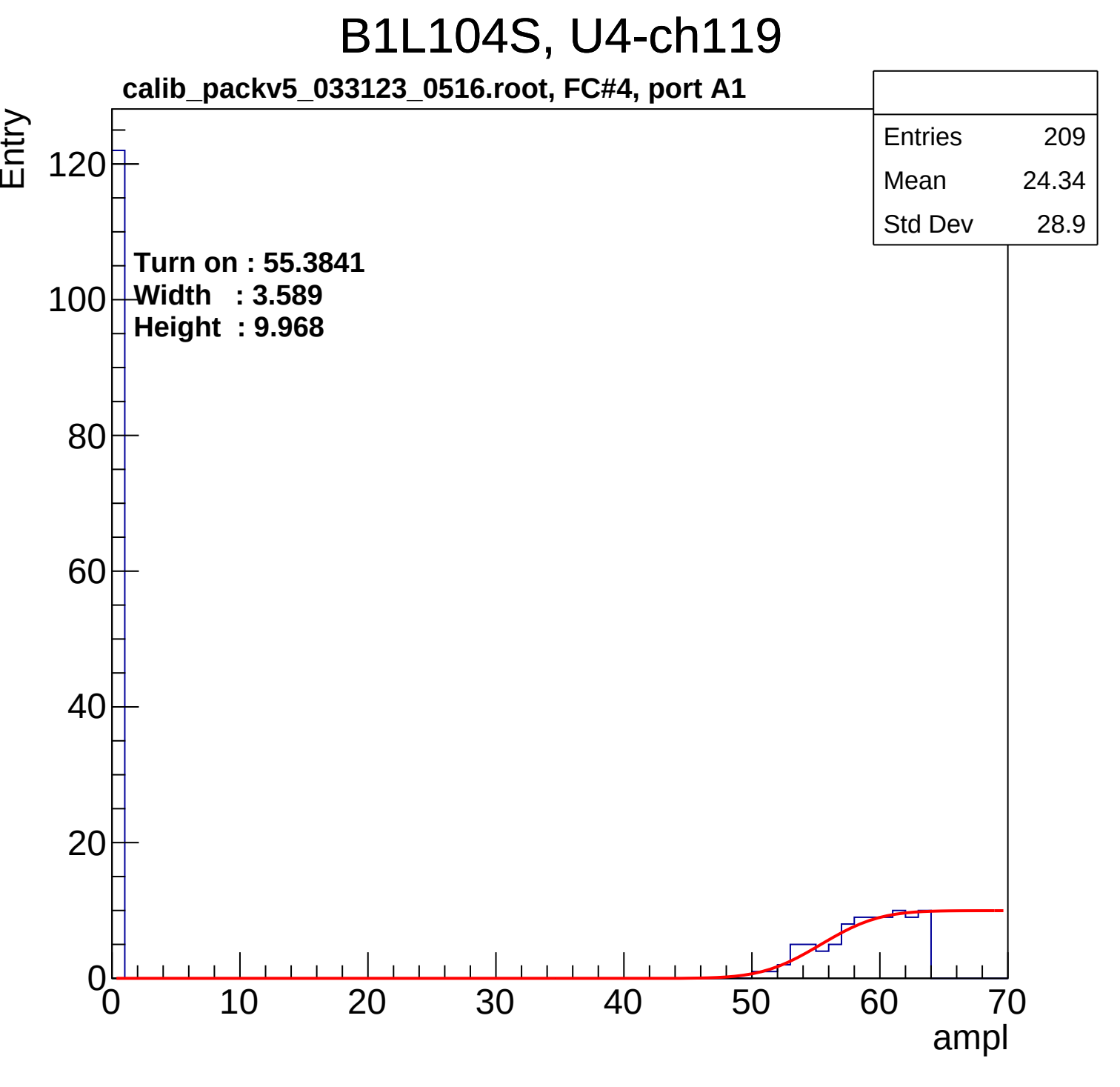

B1L104S, U4-ch114
calib_packv5_033123_0516.root, FC#4, port A1
Entries 254
Mean 27.7
Std Dev 28.53
Turn on : 52.5963
Width : 5.012
Height : 10.637
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

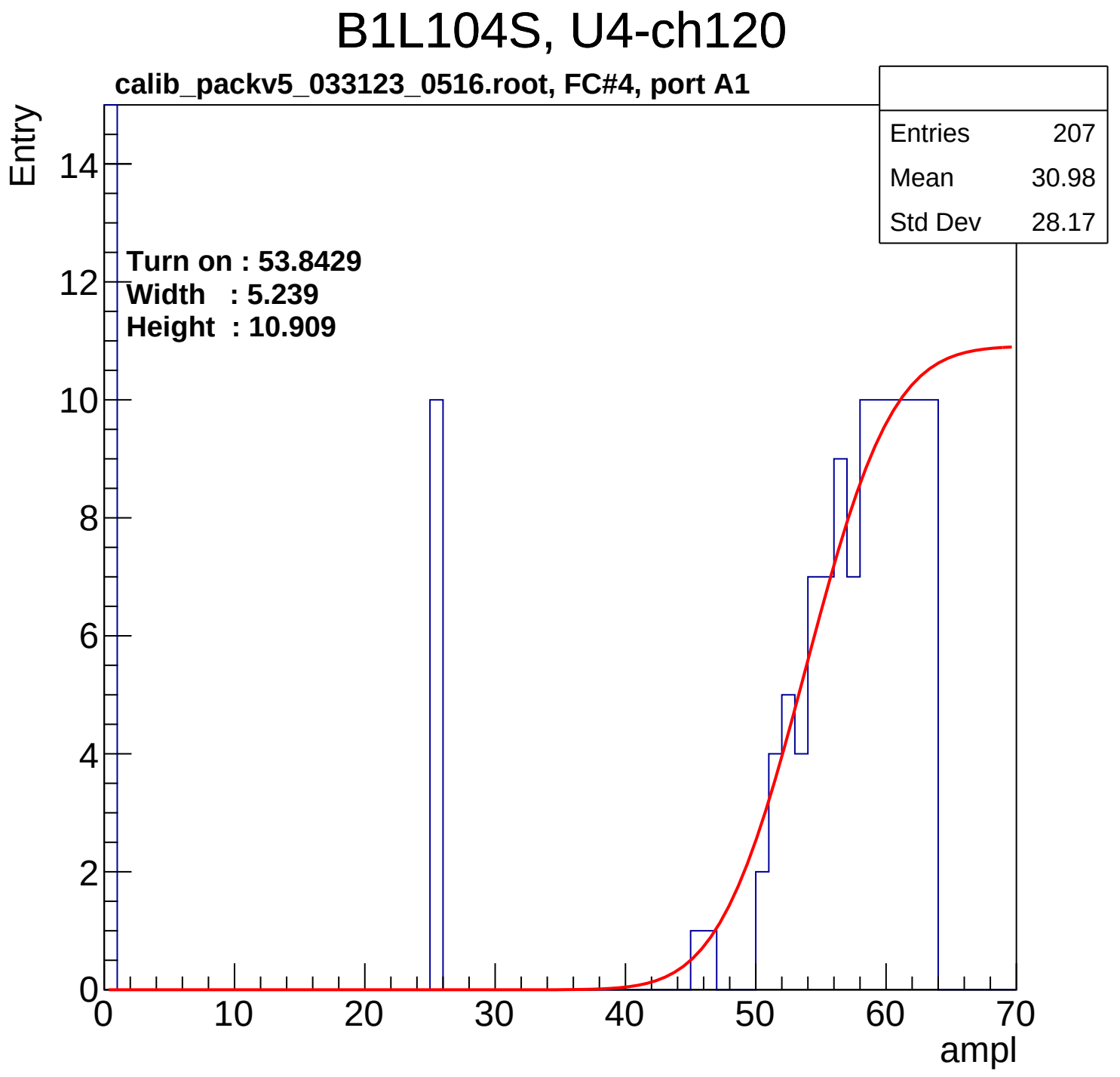

B1L104S, U4-ch115
calib_packv5_033123_0516.root, FC#4, port A1
Entries 178
Mean 33.68
Std Dev 28.58
Turn on : 54.6076
Width : 5.625
Height : 11.111
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

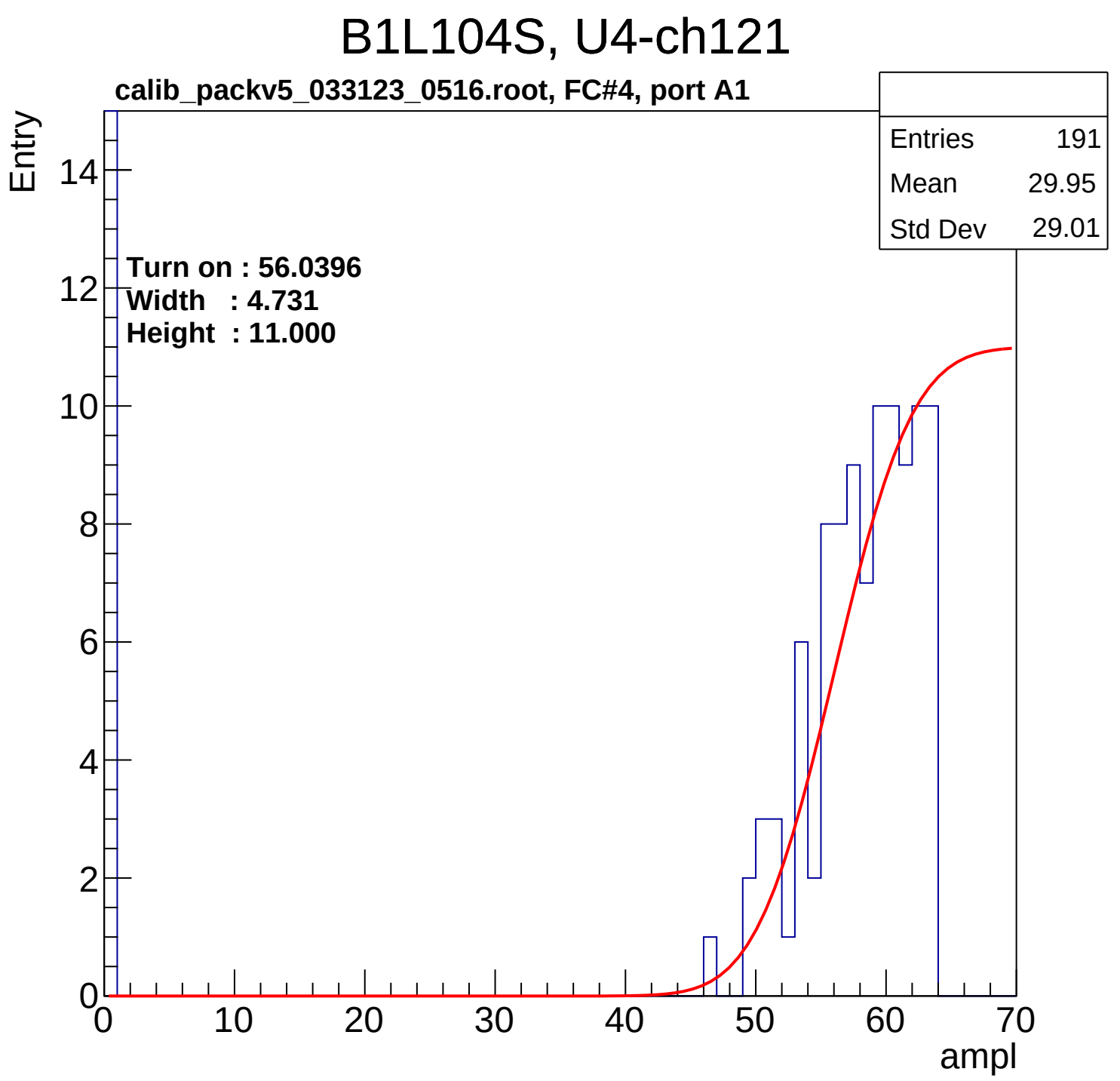

B1L104S, U4-ch116
calib_packv5_033123_0516.root, FC#4, port A1
Entries 195
Mean 36.81
Std Dev 27.2
Turn on : 51.9261
Width : 3.494
Height : 10.032
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

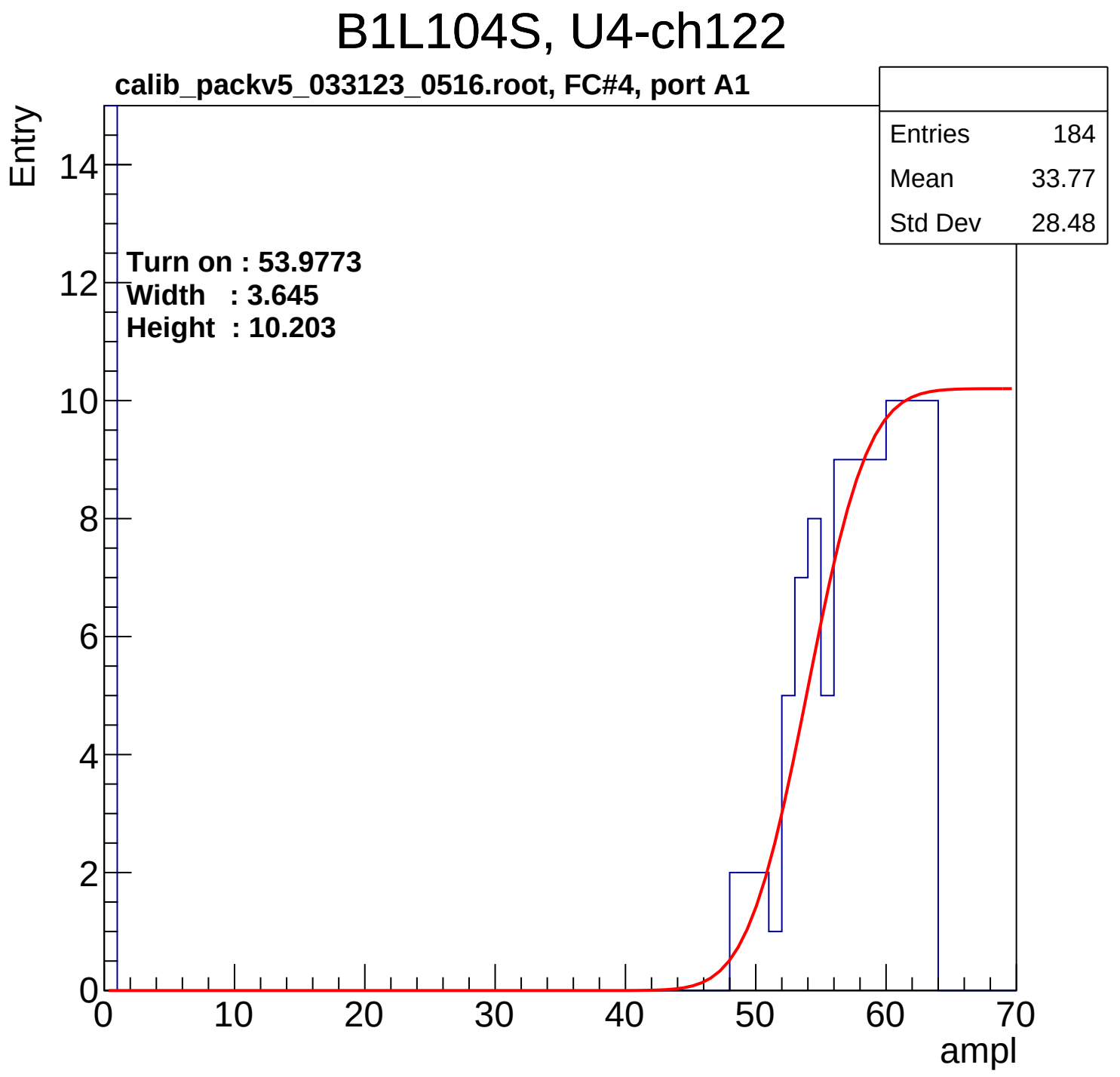

B1L104S, U4-ch117
calib_packv5_033123_0516.root, FC#4, port A1
Entries 200
Mean 28.56
Std Dev 29.23
Turn on : 54.2439
Width : 2.900
Height : 10.129
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

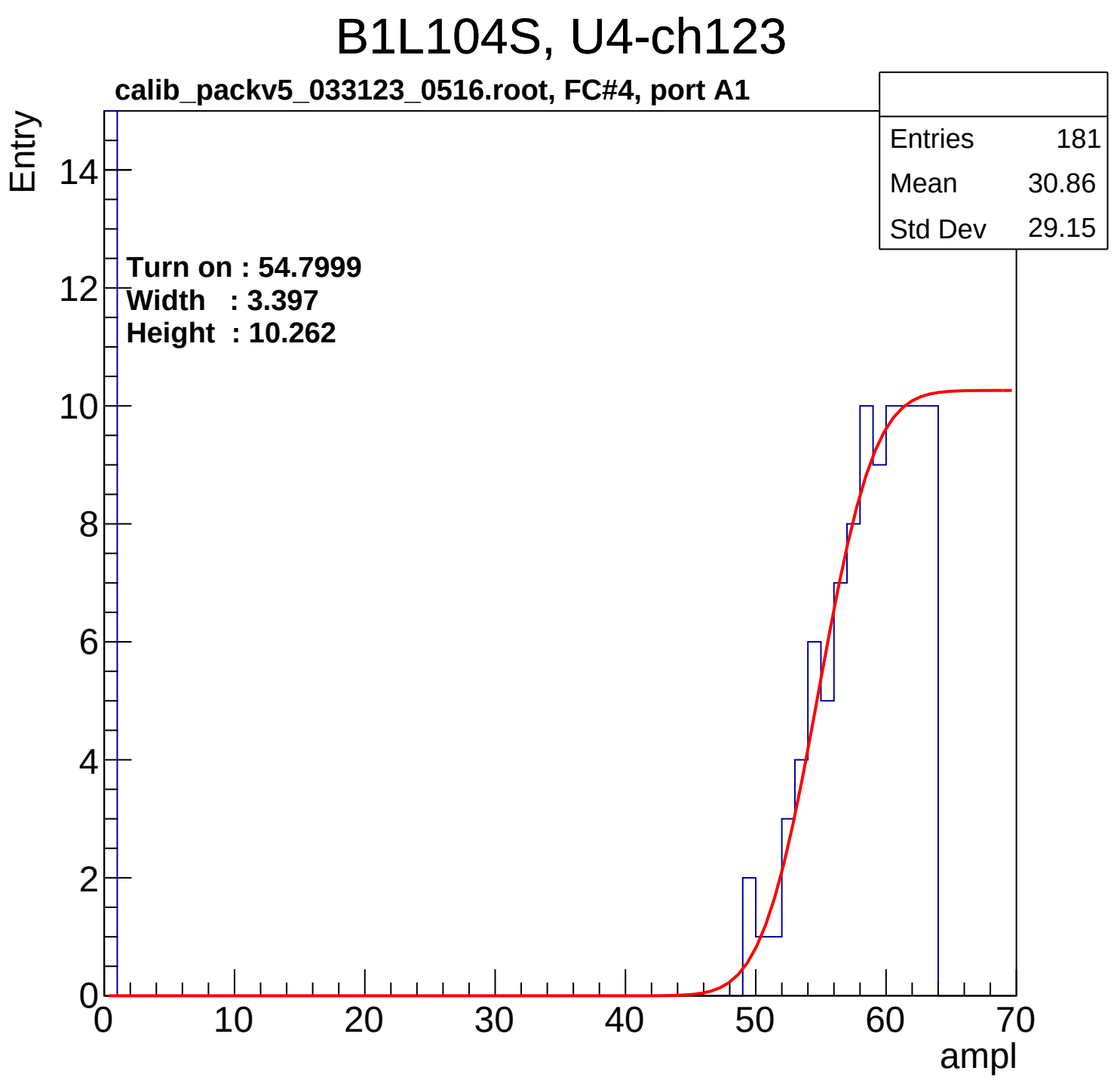

B1L104S, U4-ch118
calib_packv5_033123_0516.root, FC#4, port A1
Entries 233
Mean 32.24
Std Dev 27.96
Turn on : 50.7218
Width : 5.296
Height : 10.252
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

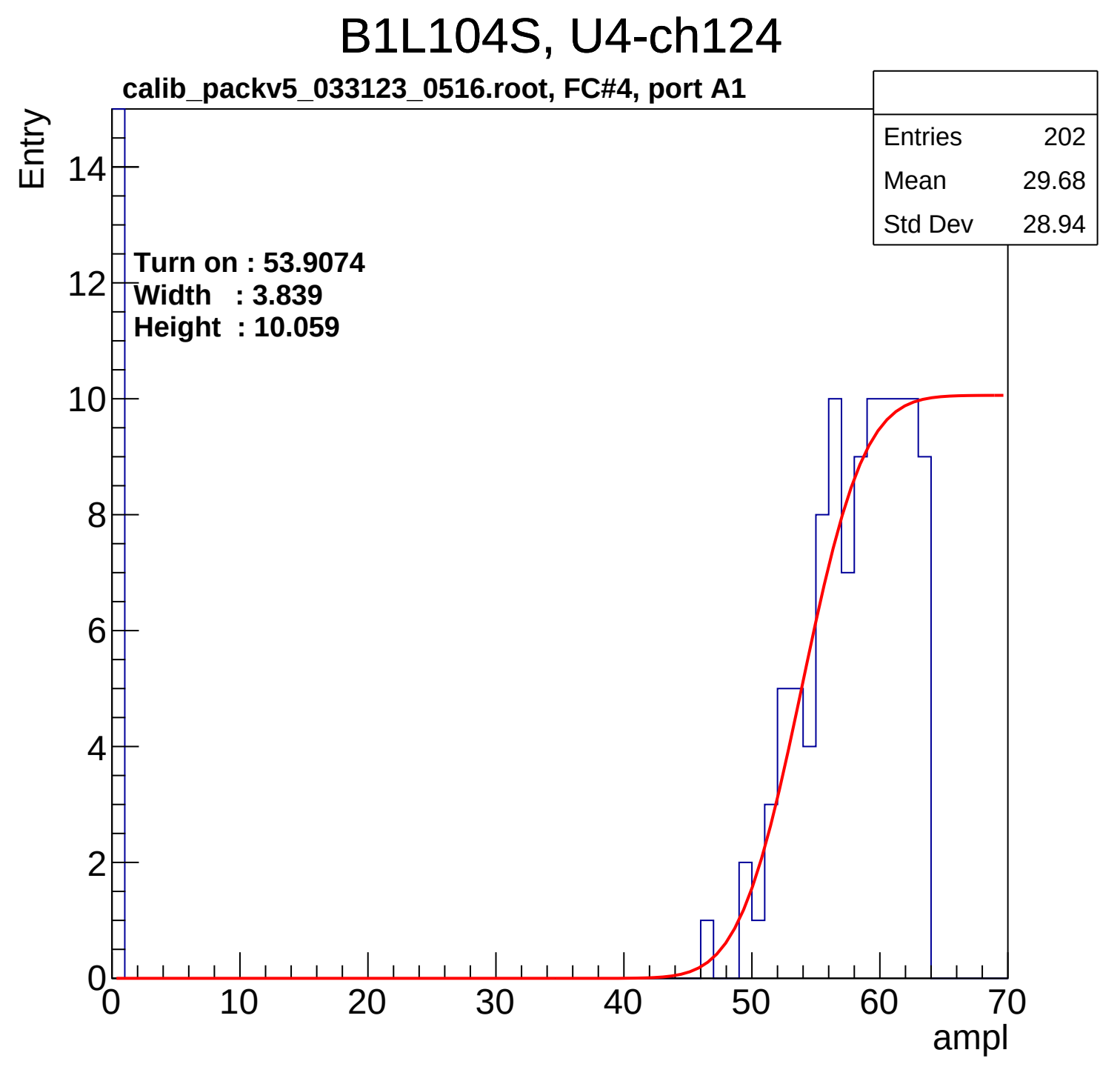

B1L104S, U4-ch119
calib_packv5_033123_0516.root, FC#4, port A1
Entries 209
Mean 24.34
Std Dev 28.9
Turn on : 55.3841
Width : 3.589
Height : 9.968
Entry
ampl
0
20
40
60
80
100
120
0
10
20
30
40
50
60
70

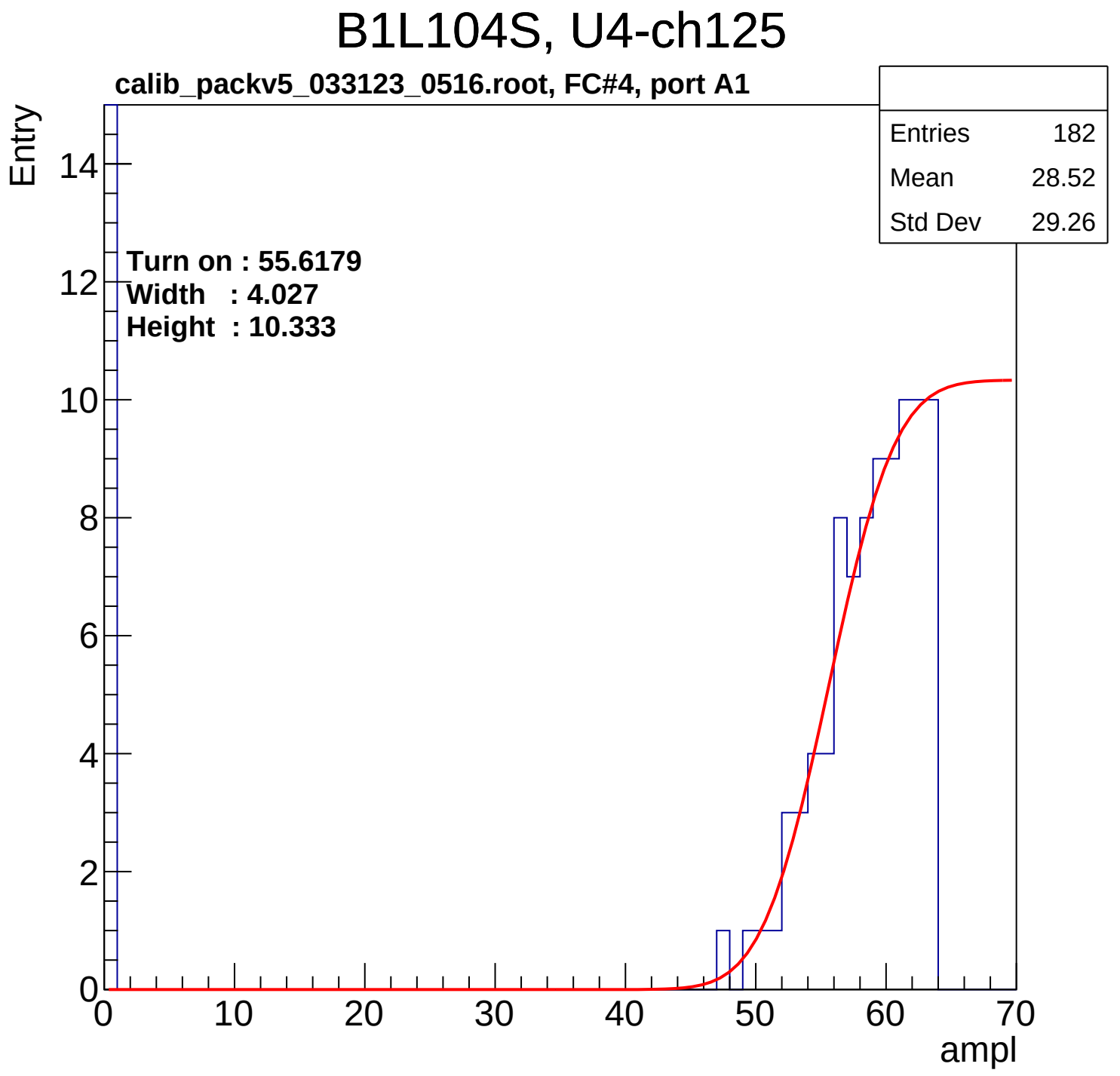

B1L104S, U4-ch120
calib_packv5_033123_0516.root, FC#4, port A1
Entries 207
Mean 30.98
Std Dev 28.17
Turn on : 53.8429
Width : 5.239
Height : 10.909
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

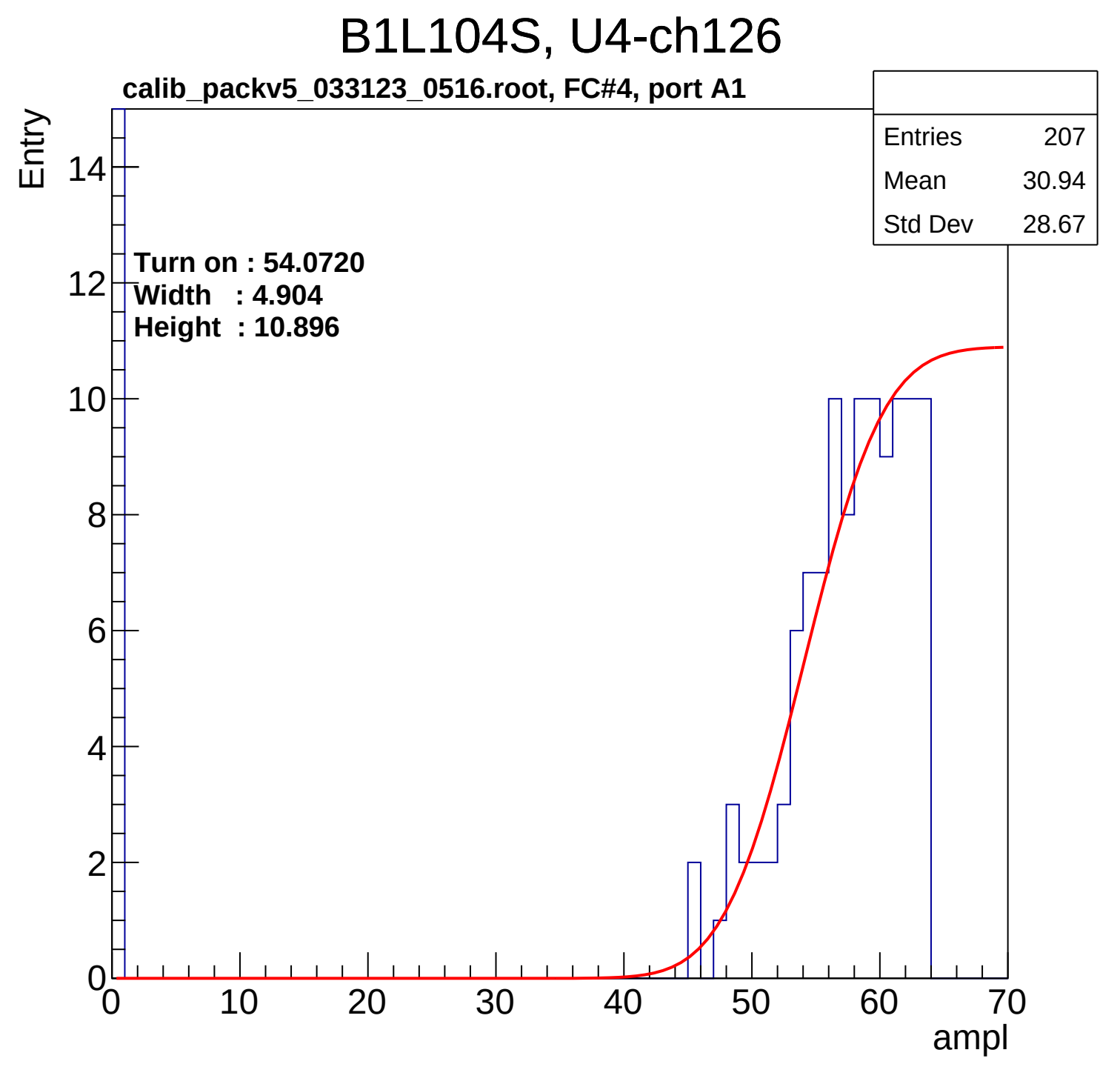

B1L104S, U4-ch121
calib_packv5_033123_0516.root, FC#4, port A1
Entries 191
Mean 29.95
Std Dev 29.01
Turn on : 56.0396
Width : 4.731
Height : 11.000
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

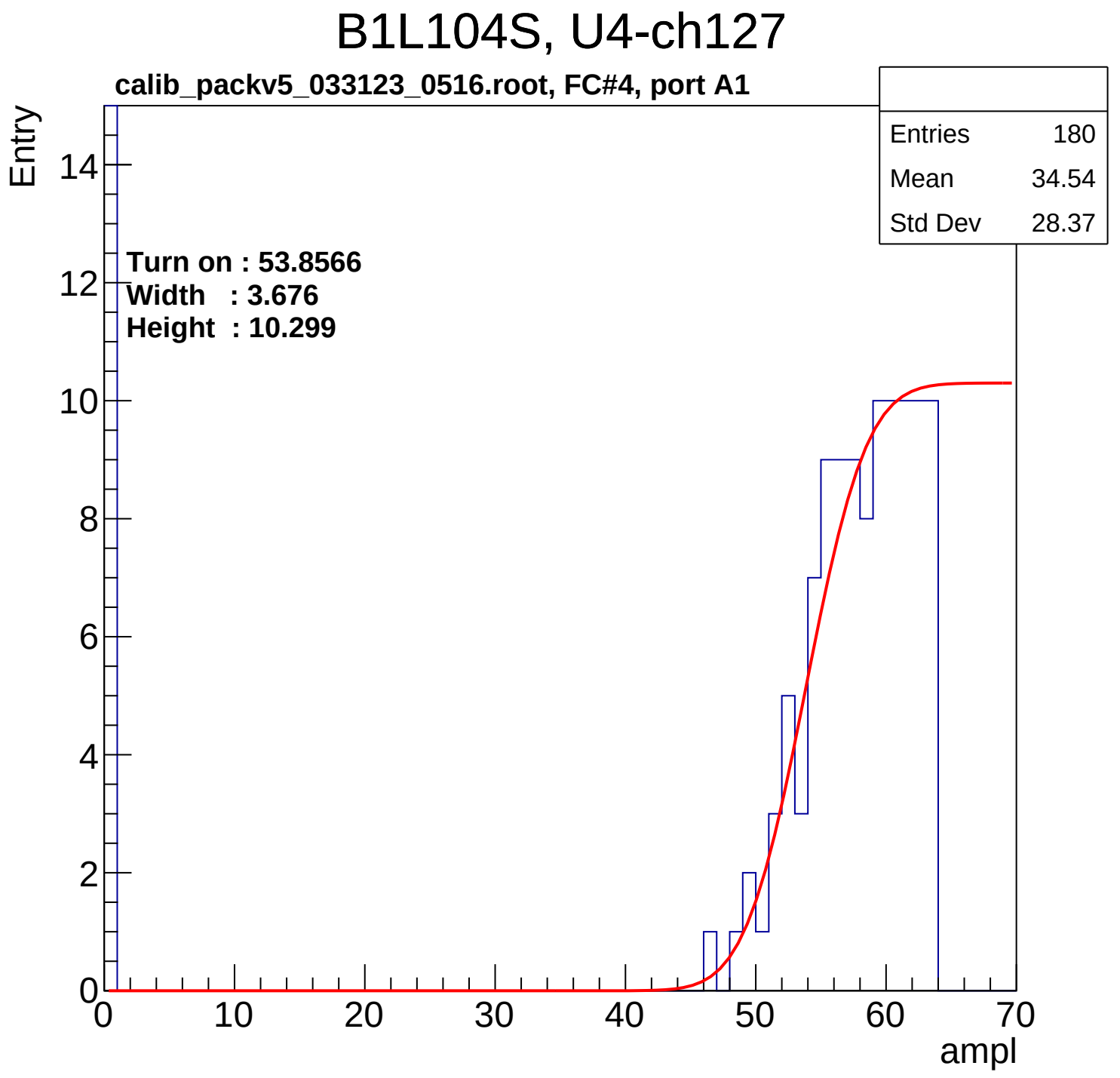

B1L104S, U4-ch122
calib_packv5_033123_0516.root, FC#4, port A1
Entries 184
Mean 33.77
Std Dev 28.48
Turn on : 53.9773
Width : 3.645
Height : 10.203
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

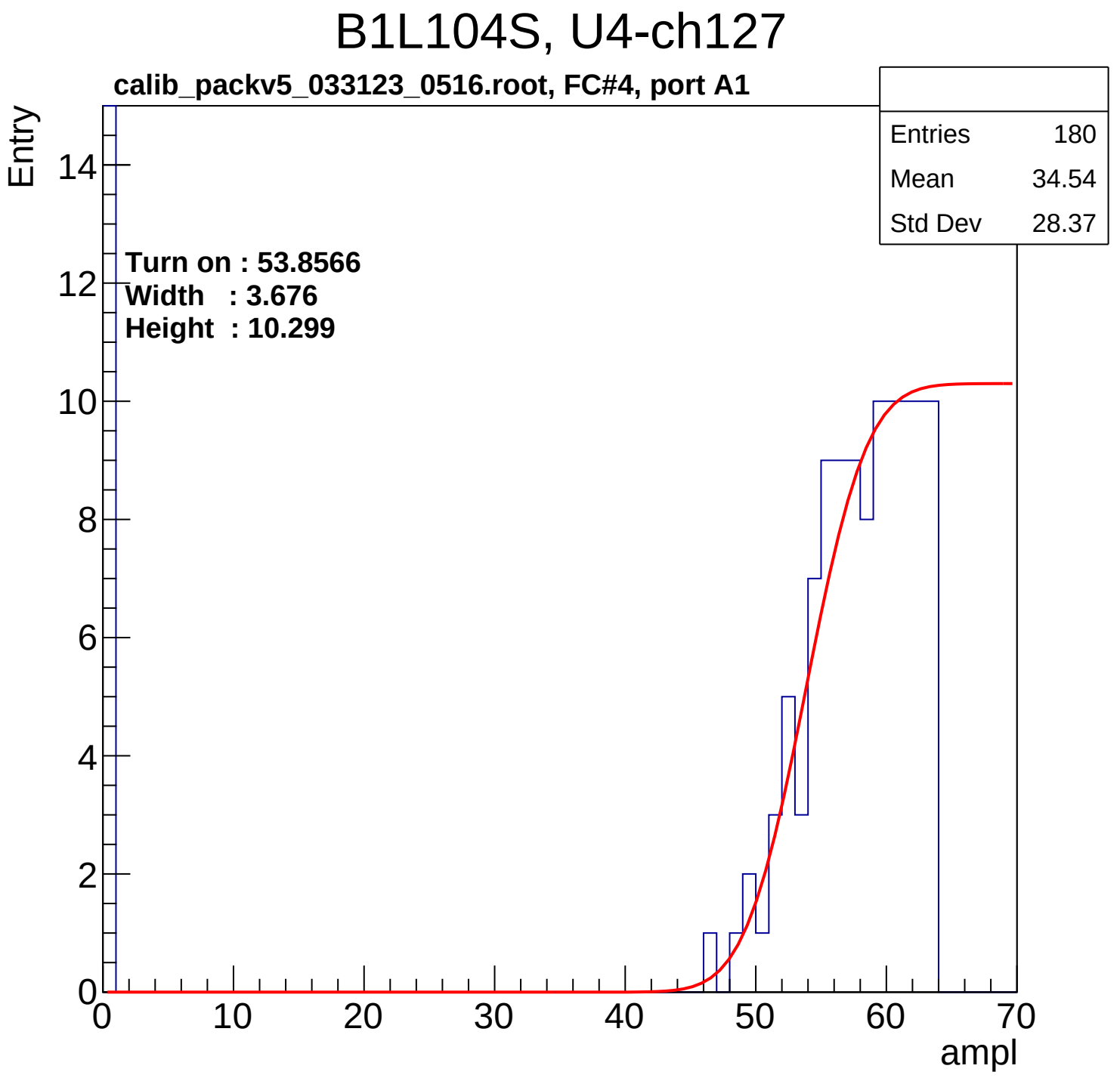

B1L104S, U4-ch123
calib_packv5_033123_0516.root, FC#4, port A1
Entries 181
Mean 30.86
Std Dev 29.15
Turn on : 54.7999
Width : 3.397
Height : 10.262
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L104S, U4-ch124
calib_packv5_033123_0516.root, FC#4, port A1
Entries 202
Mean 29.68
Std Dev 28.94
Turn on : 53.9074
Width : 3.839
Height : 10.059
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L104S, U4-ch125
calib_packv5_033123_0516.root, FC#4, port A1
Entries 182
Mean 28.52
Std Dev 29.26
Turn on : 55.6179
Width : 4.027
Height : 10.333
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L104S, U4-ch126
calib_packv5_033123_0516.root, FC#4, port A1
Entries 207
Mean 30.94
Std Dev 28.67
Turn on : 54.0720
Width : 4.904
Height : 10.896
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L104S, U4-ch127
calib_packv5_033123_0516.root, FC#4, port A1
Entries 180
Mean 34.54
Std Dev 28.37
Turn on : 53.8566
Width : 3.676
Height : 10.299
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L104S, U4-ch127
calib_packv5_033123_0516.root, FC#4, port A1
Entries 180
Mean 34.54
Std Dev 28.37
Turn on : 53.8566
Width : 3.676
Height : 10.299
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70