

B0L001S, U3-ch3, adc6 calib_packv5_042523_0143.root, FC#9, port A1 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2

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40

50

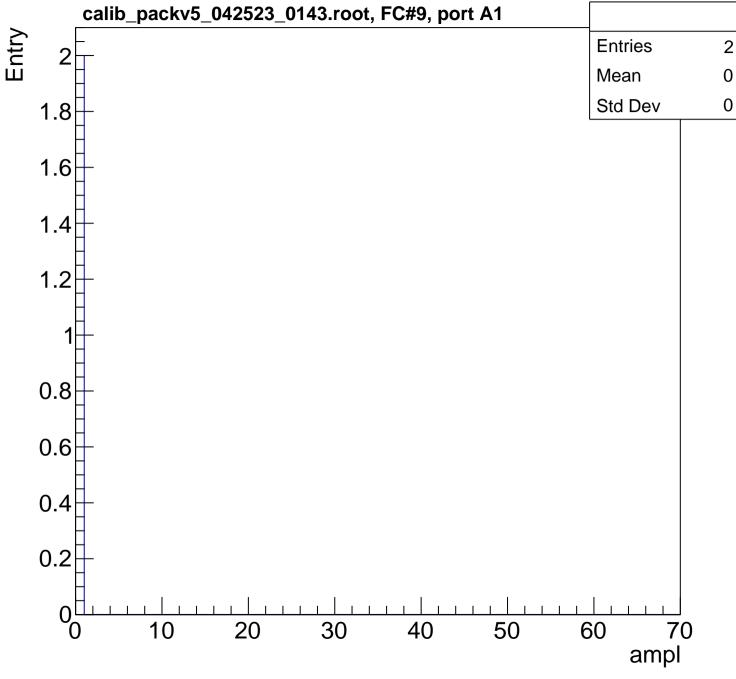
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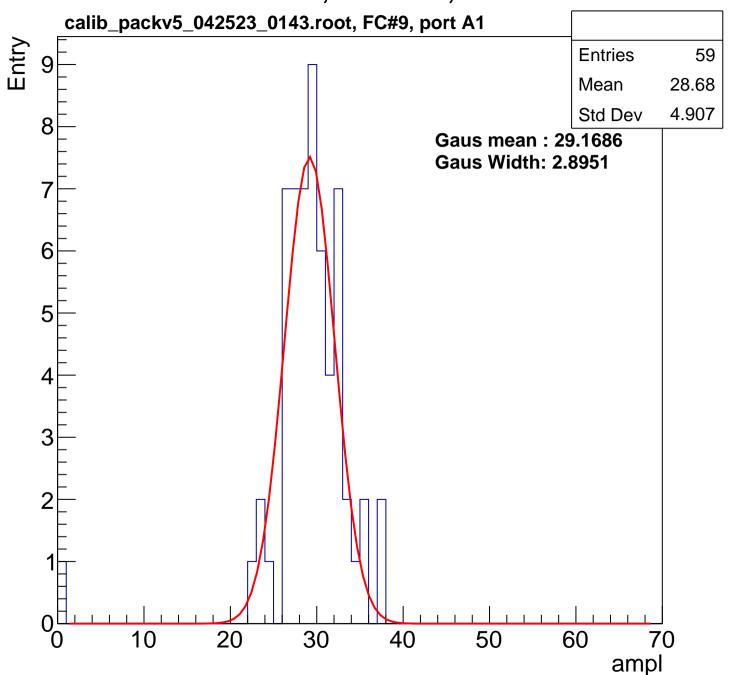
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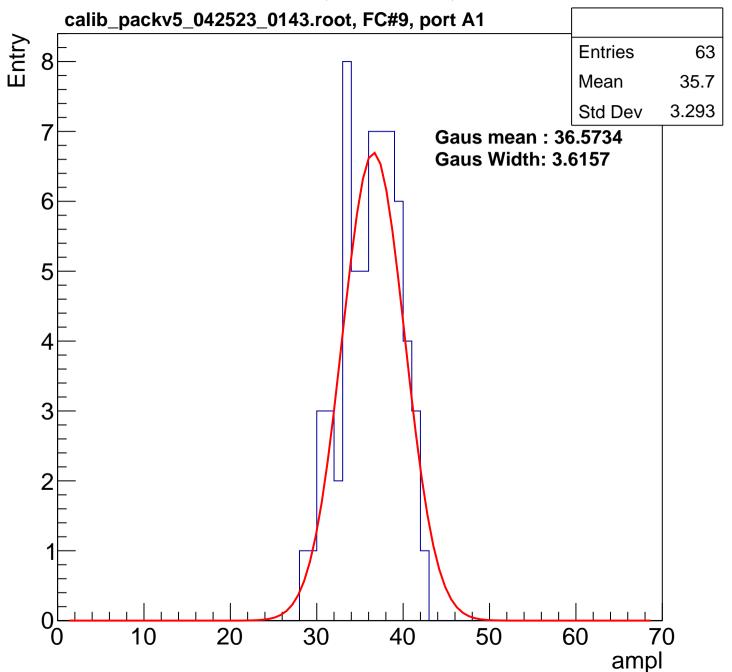
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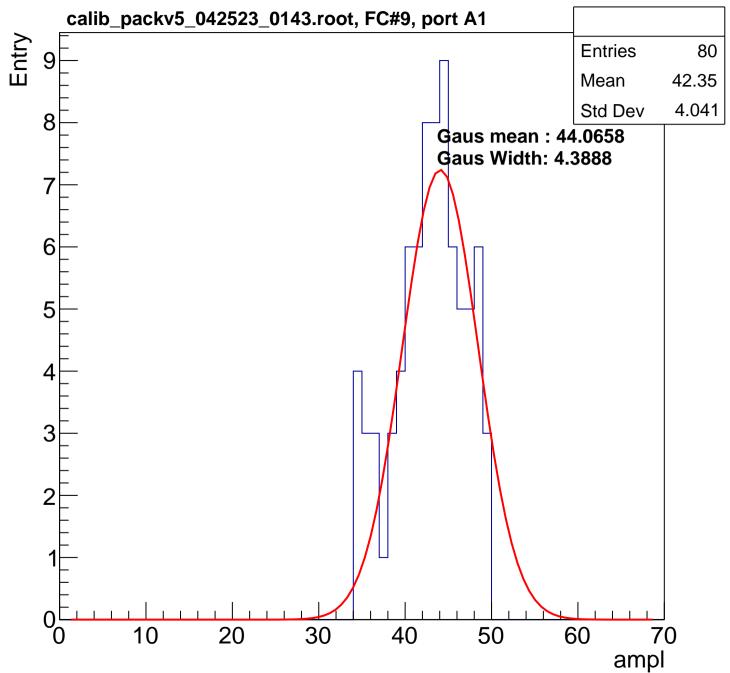
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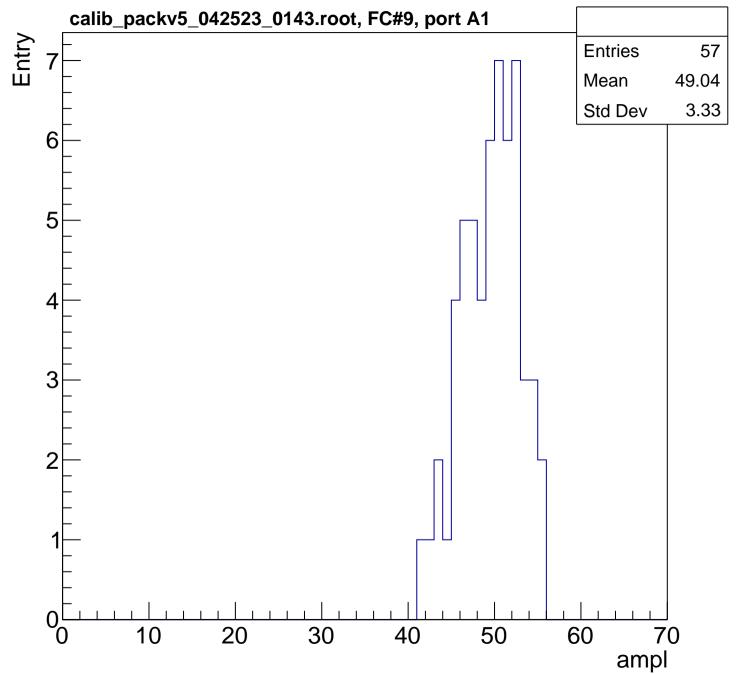
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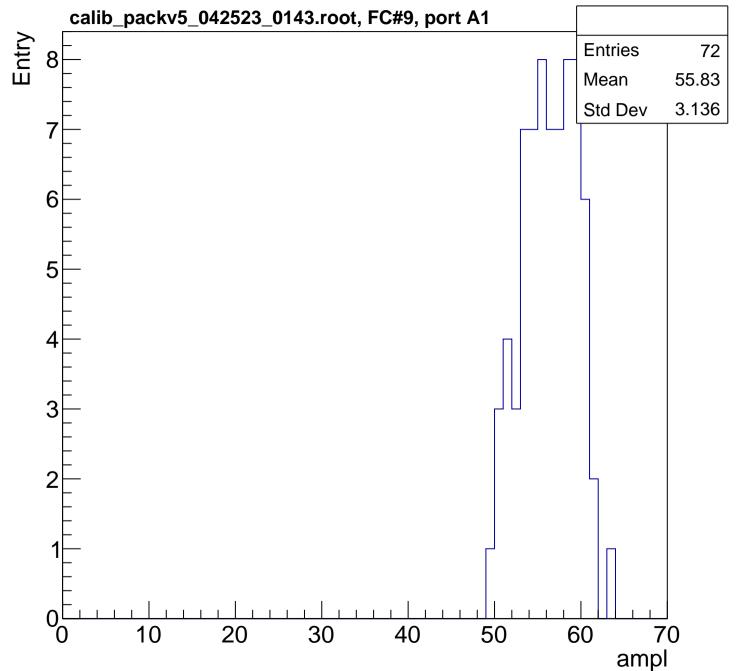


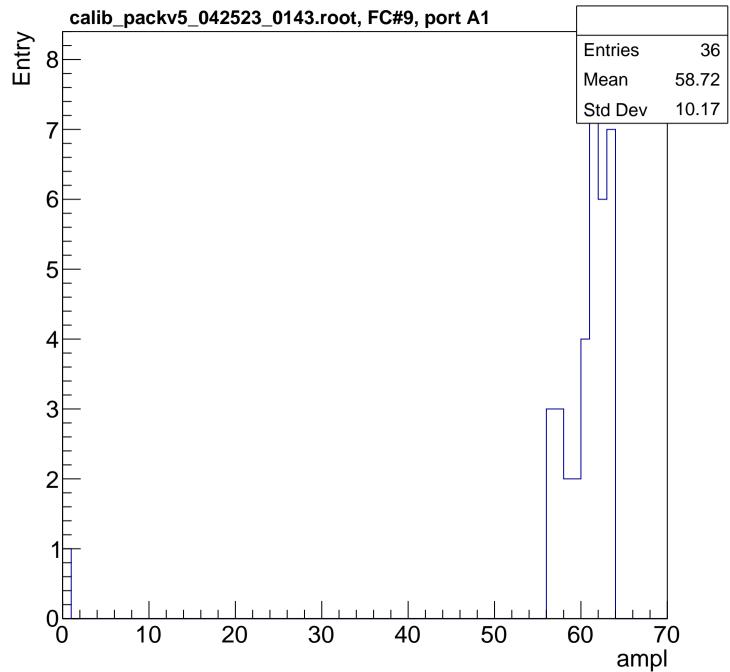


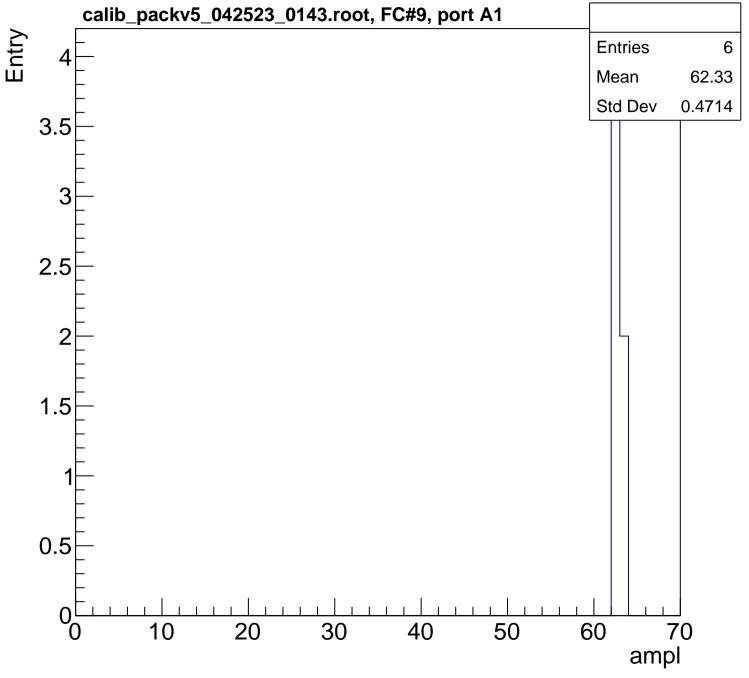




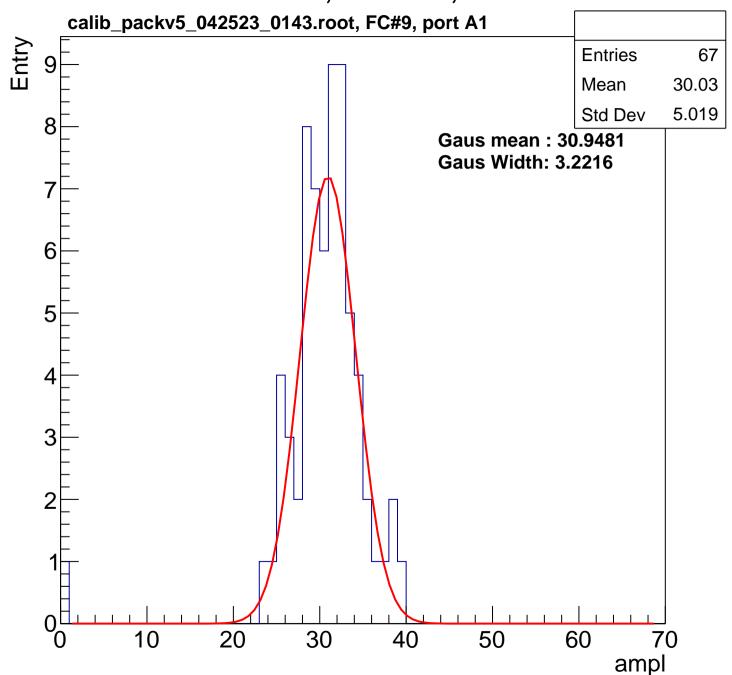


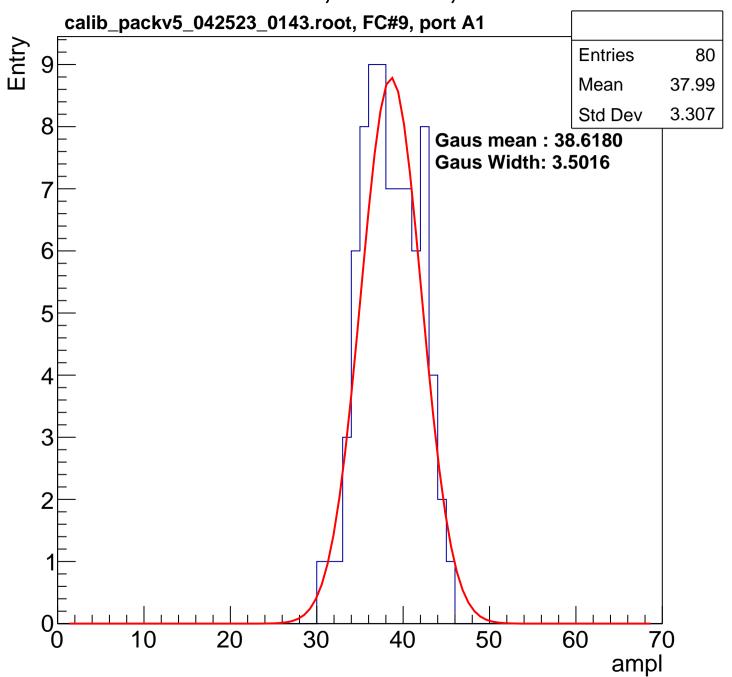


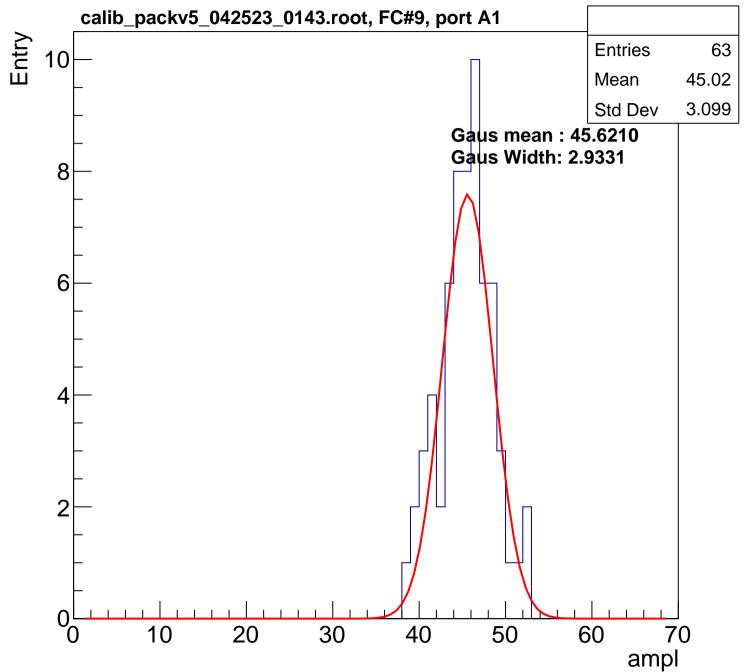


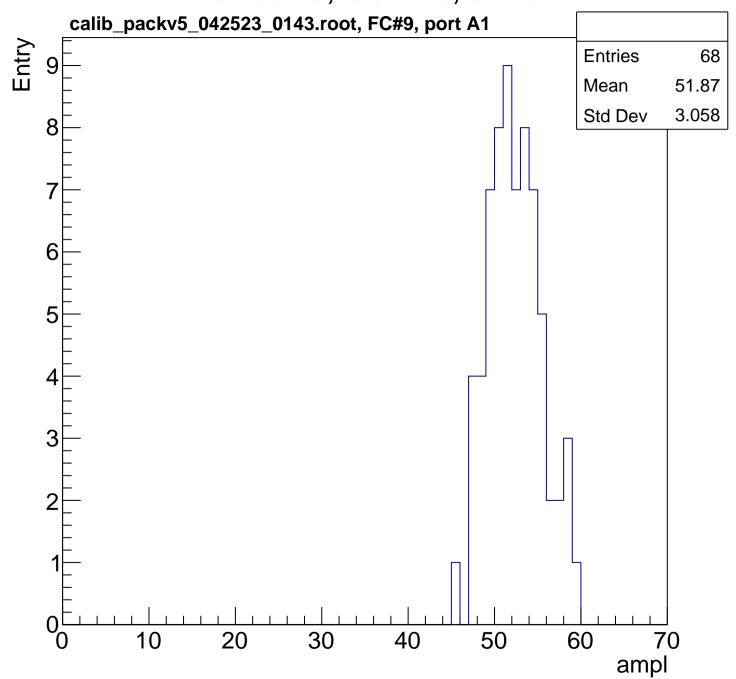


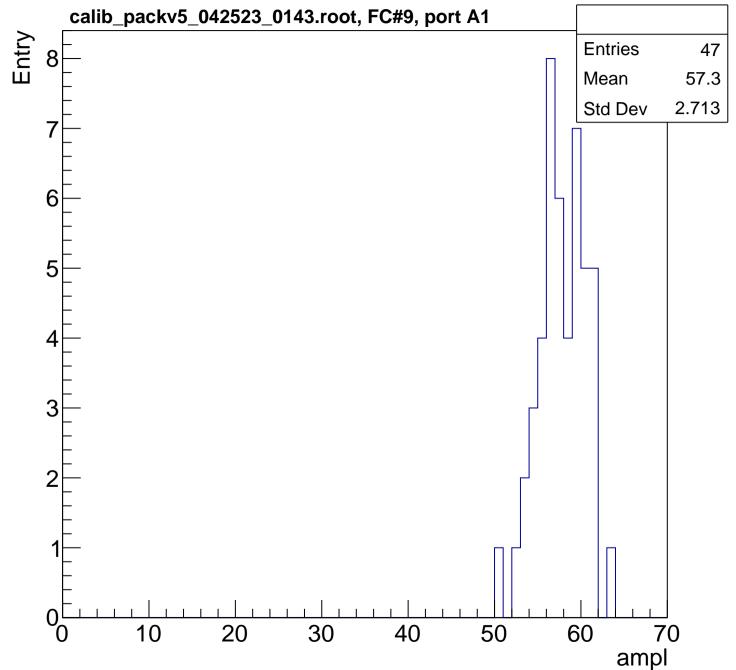
B0L001S, U3-ch4, adc7 calib_packv5_042523_0143.root, FC#9, port A1 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

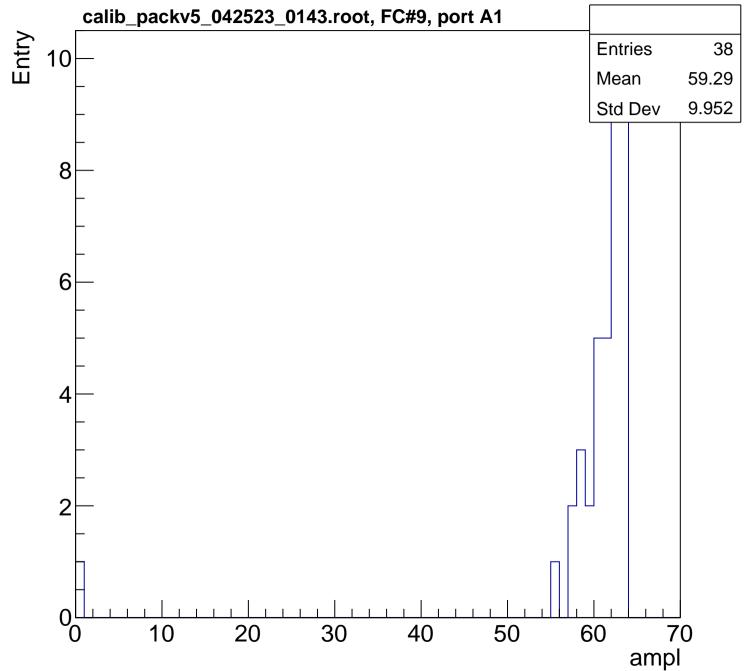


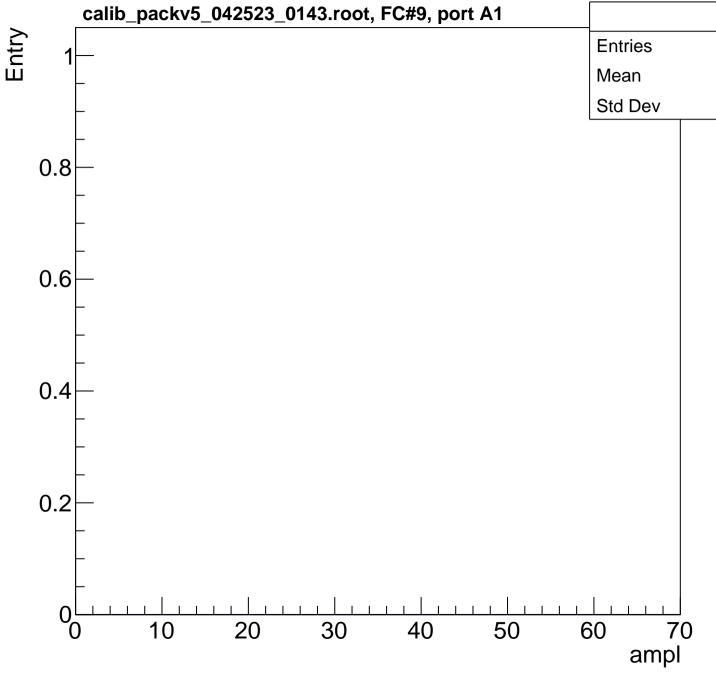


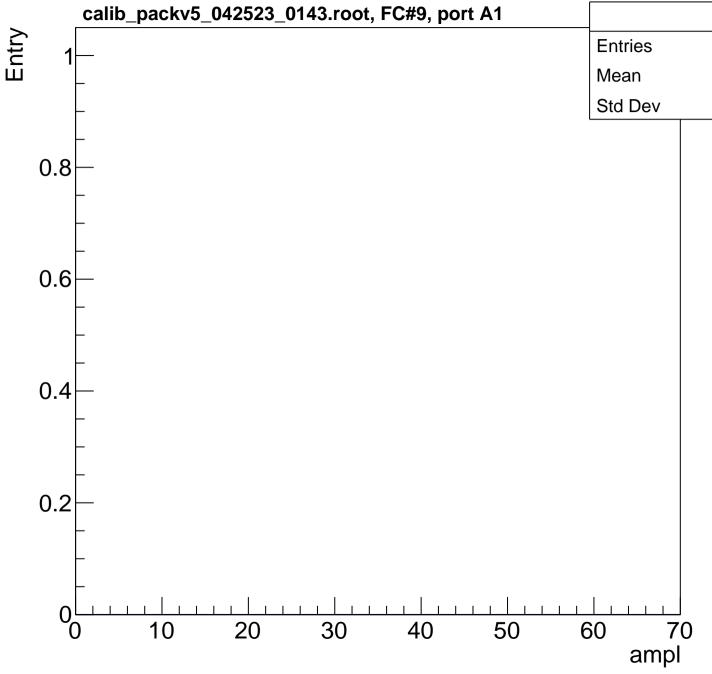


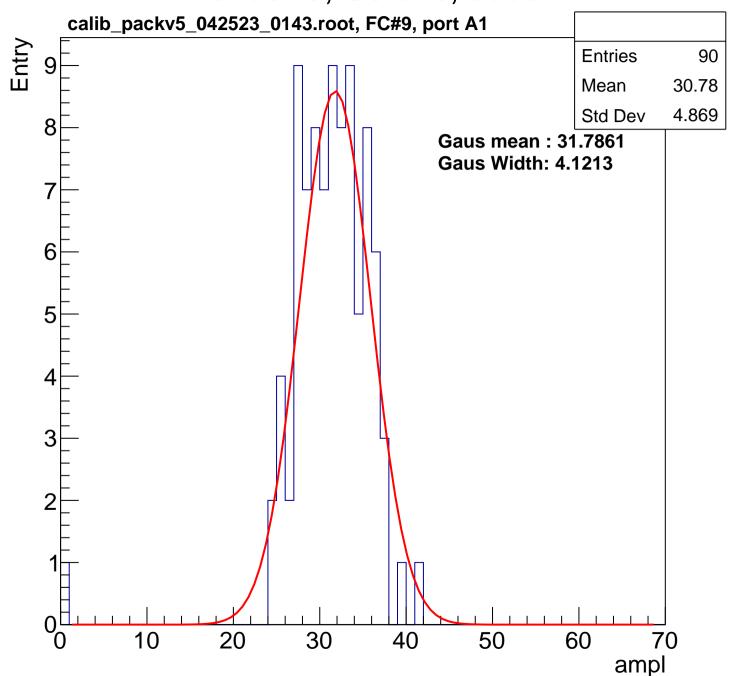


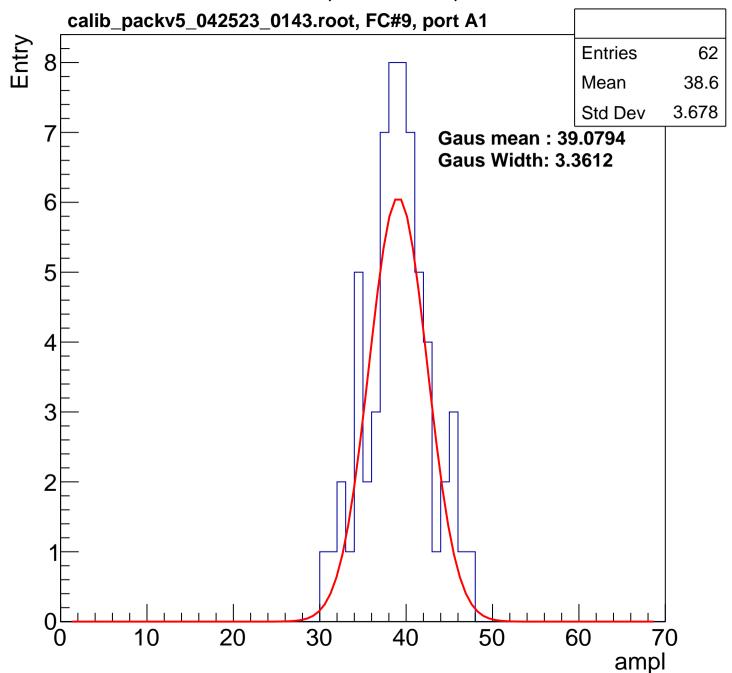


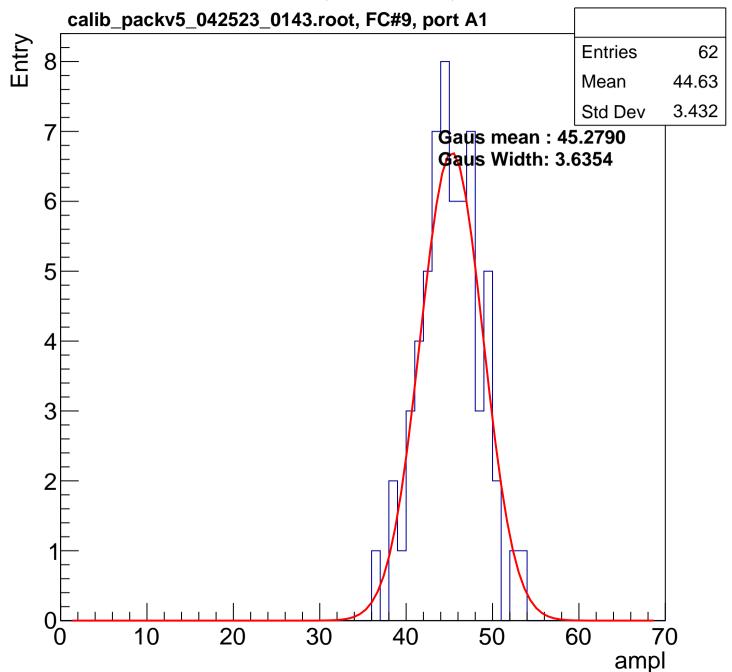


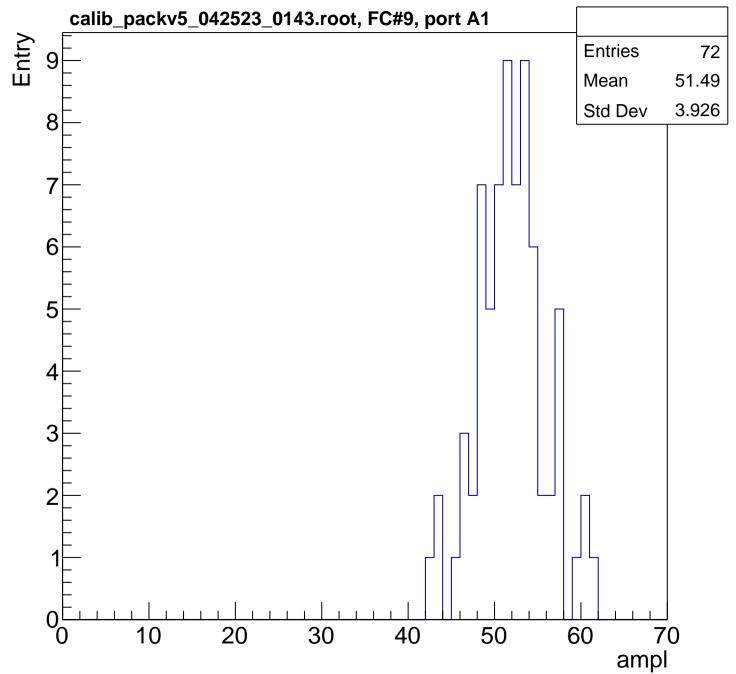


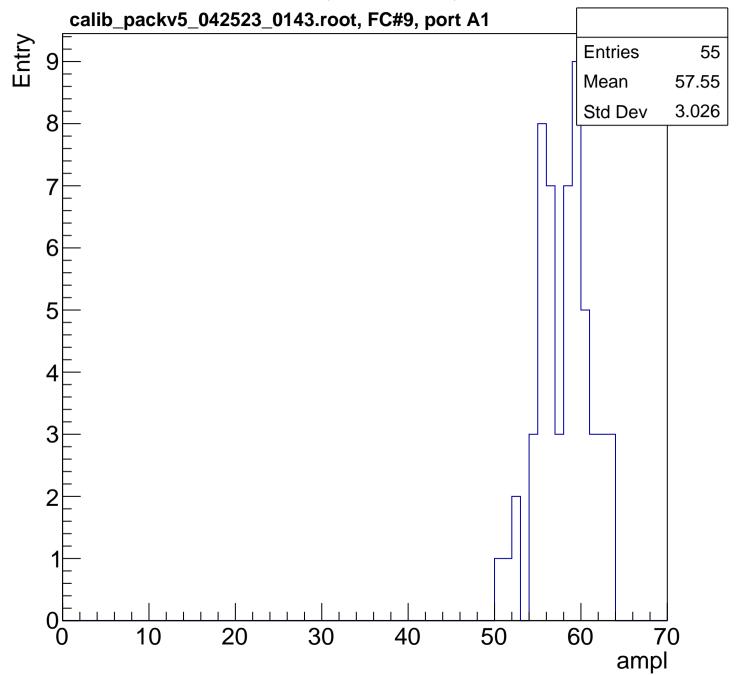


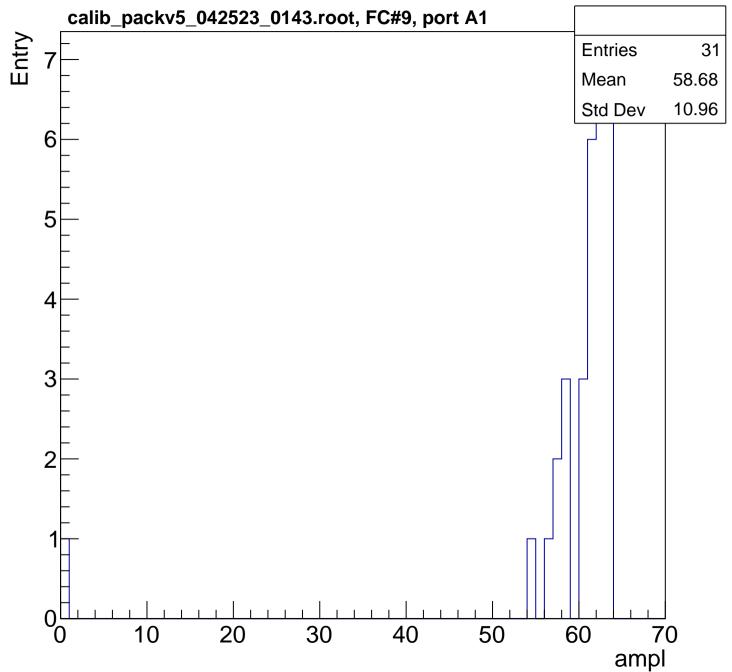


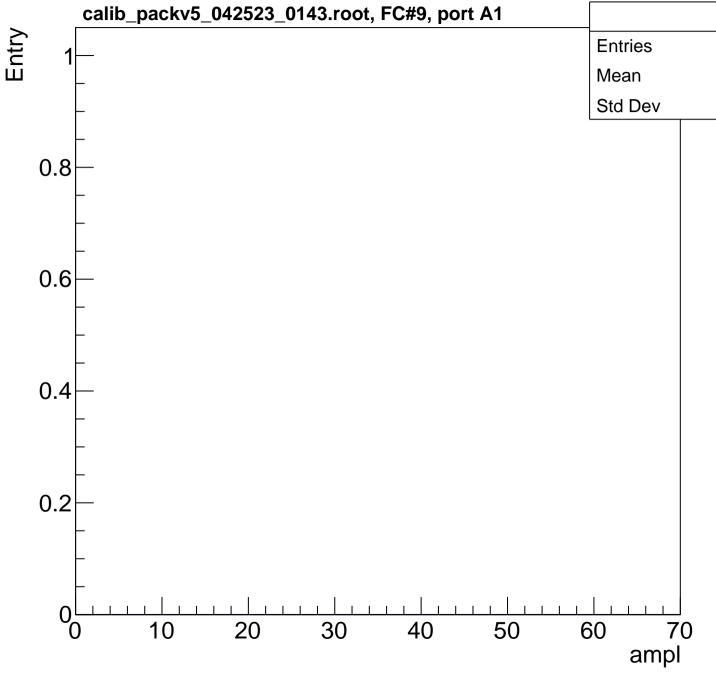


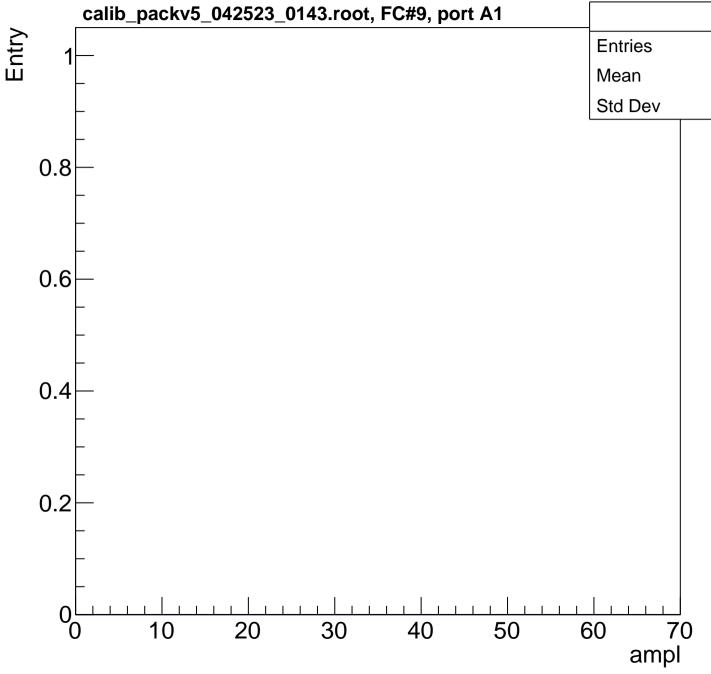


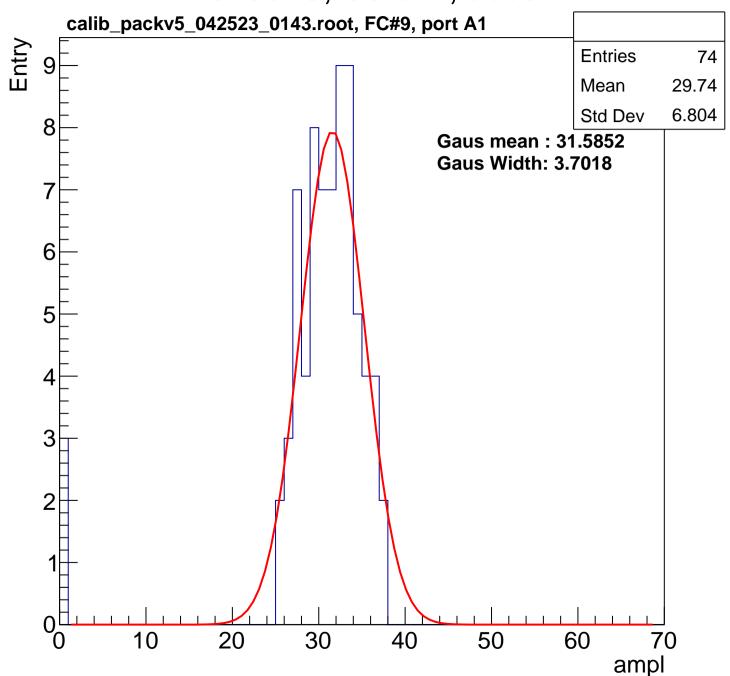


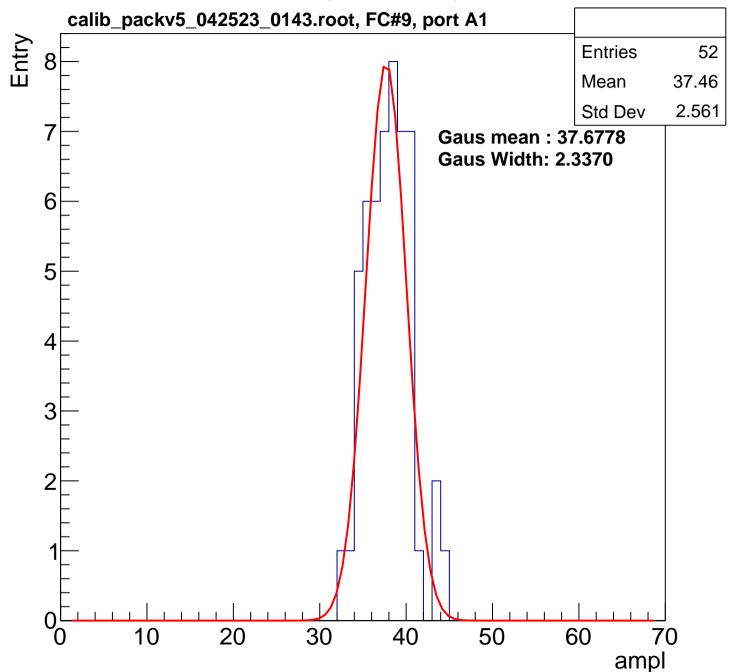


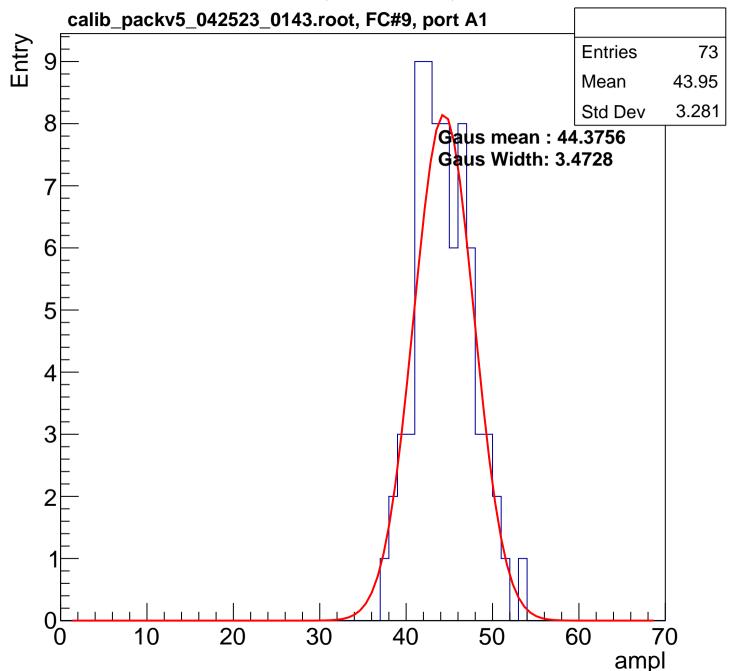


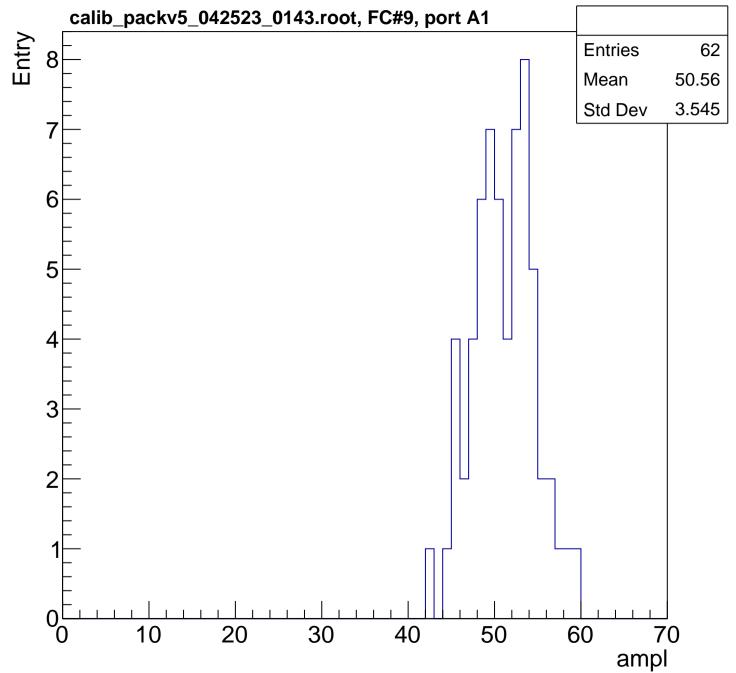


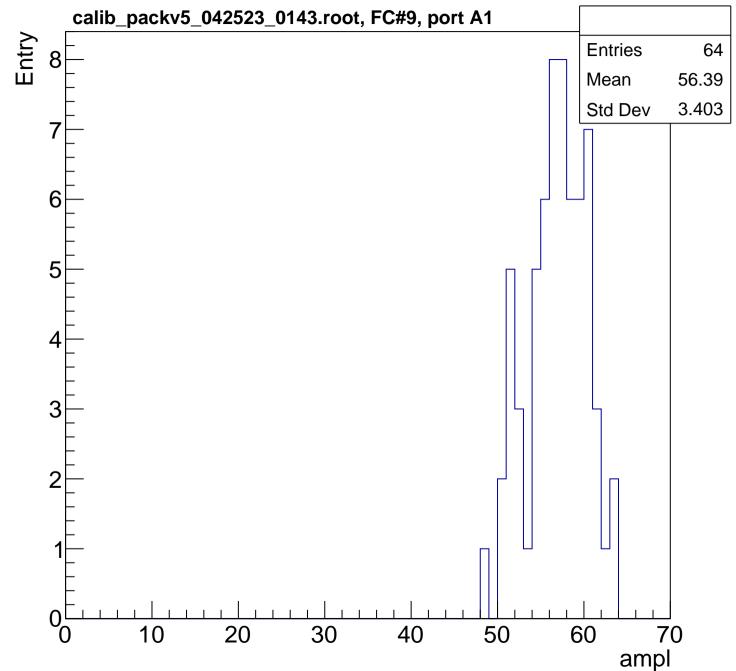


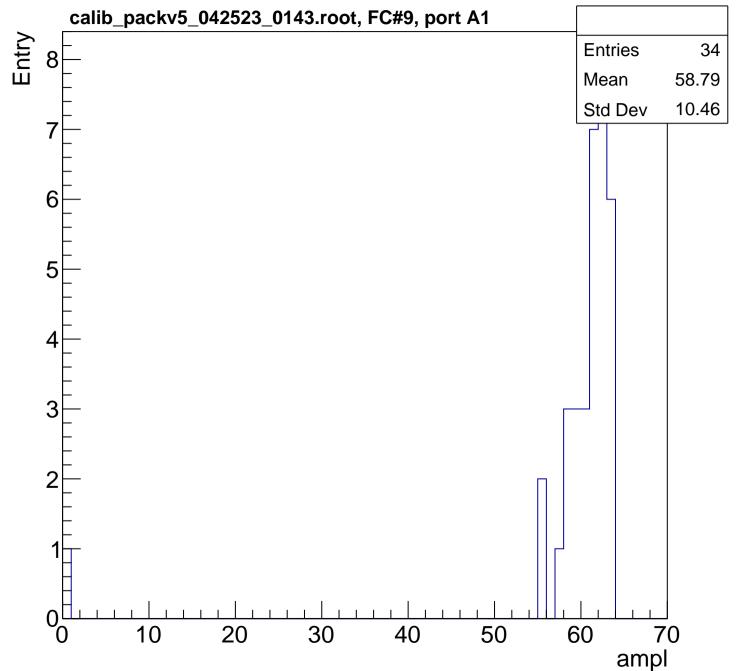


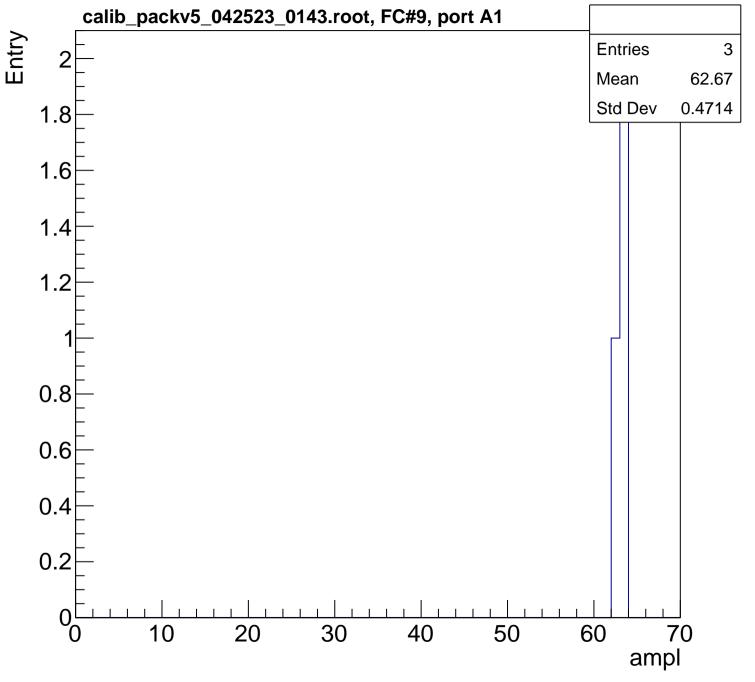




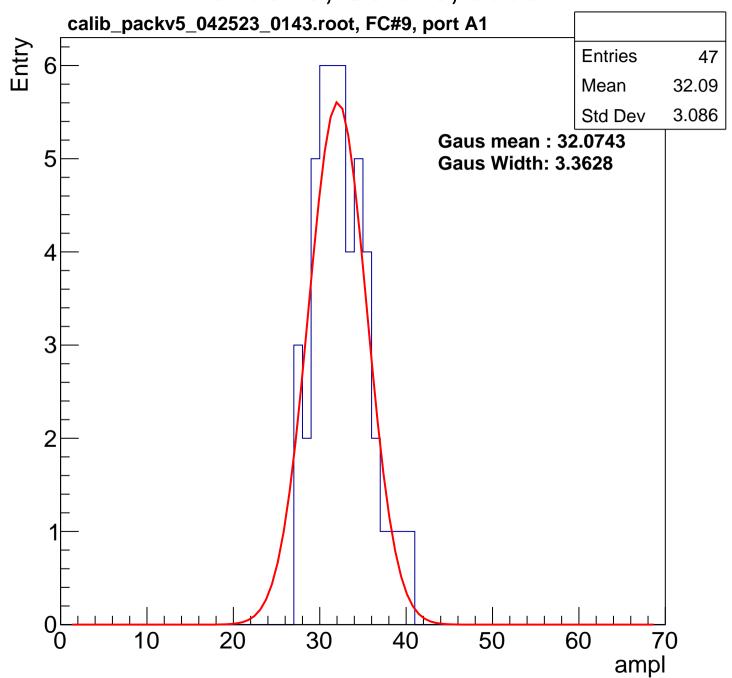


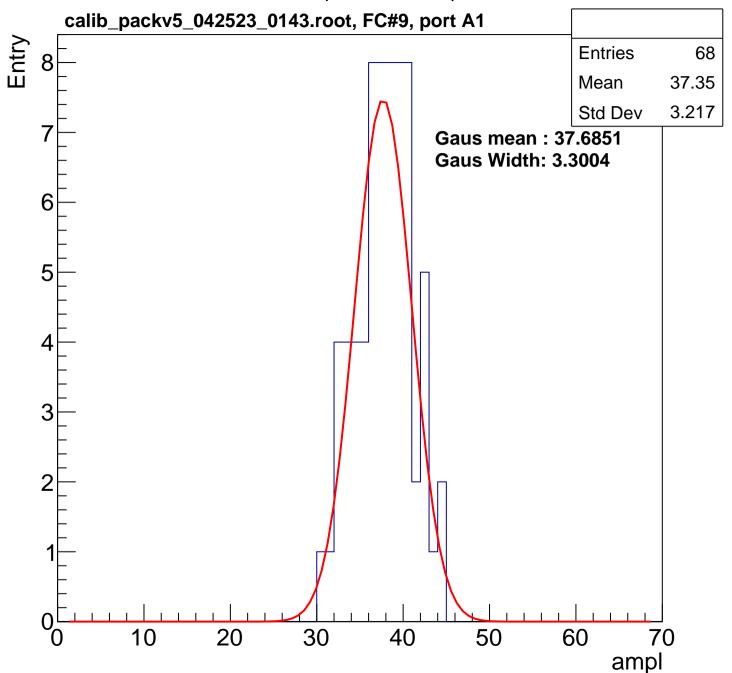


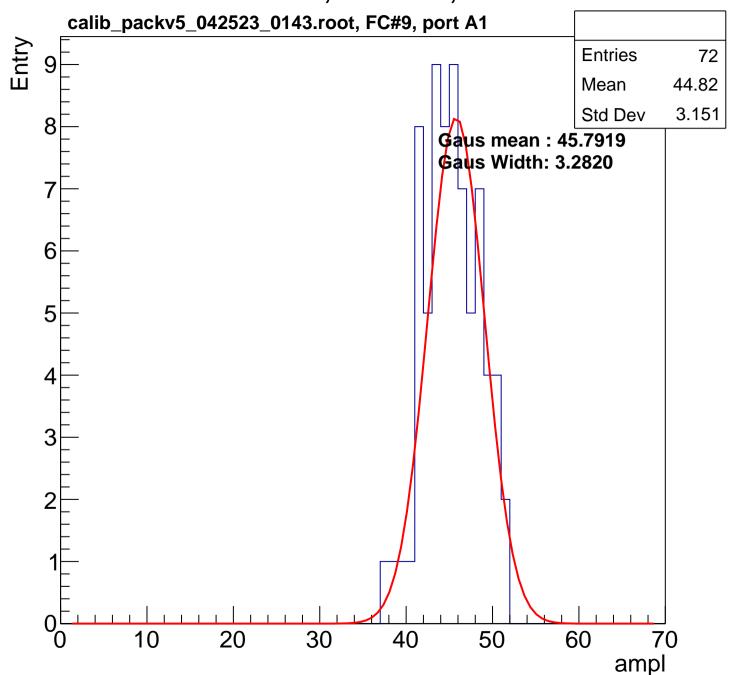


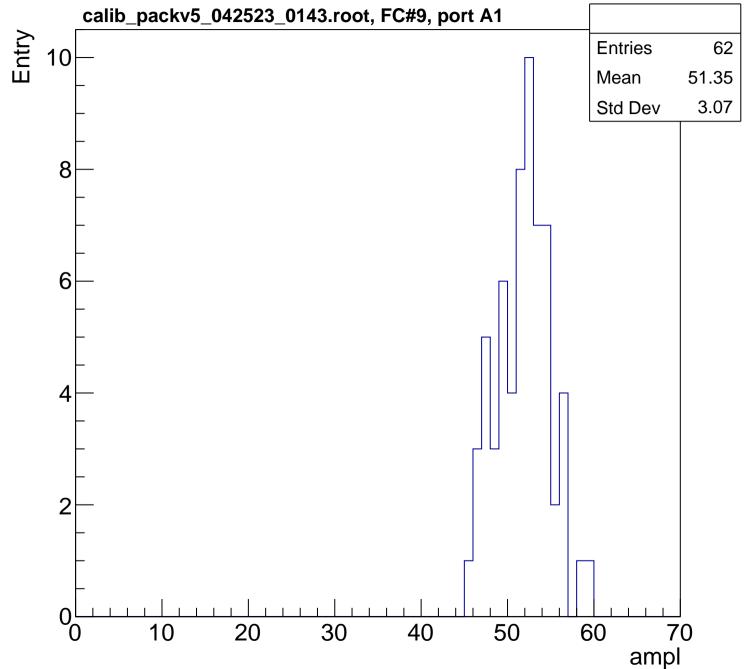


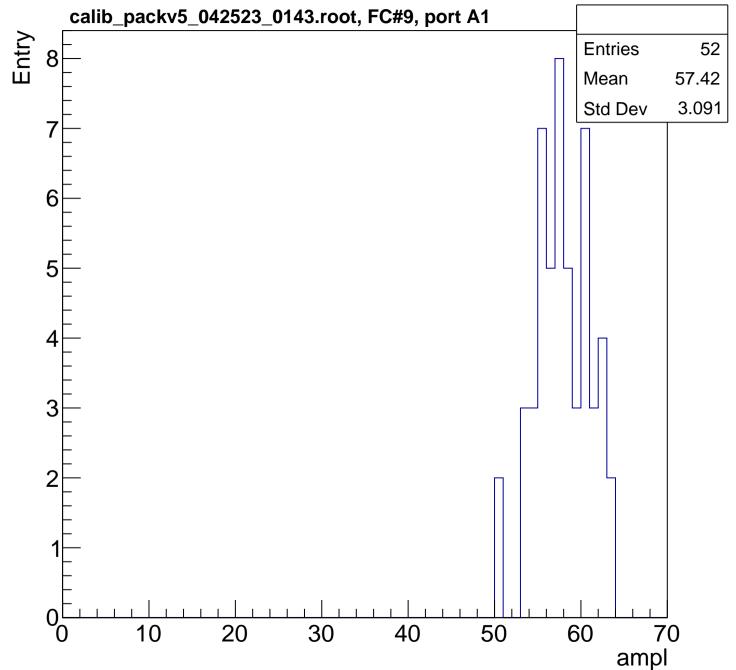


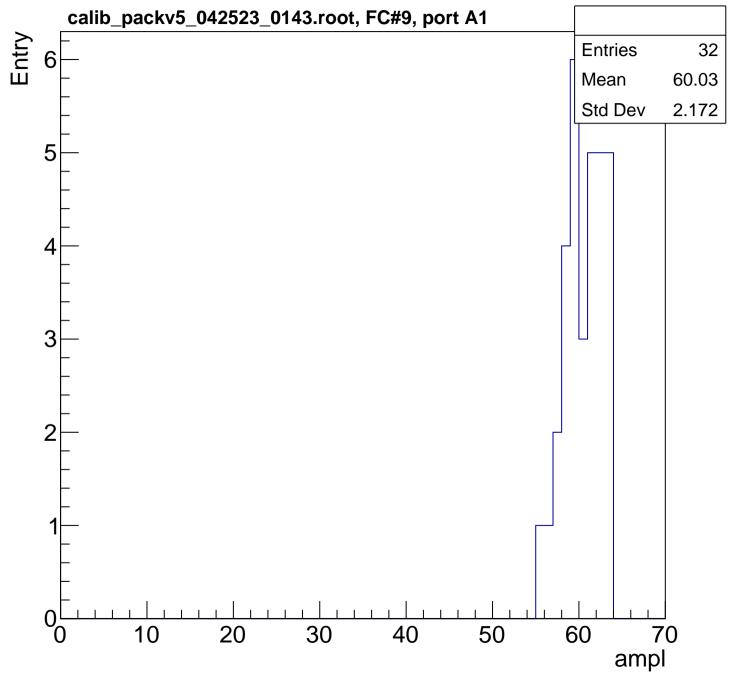


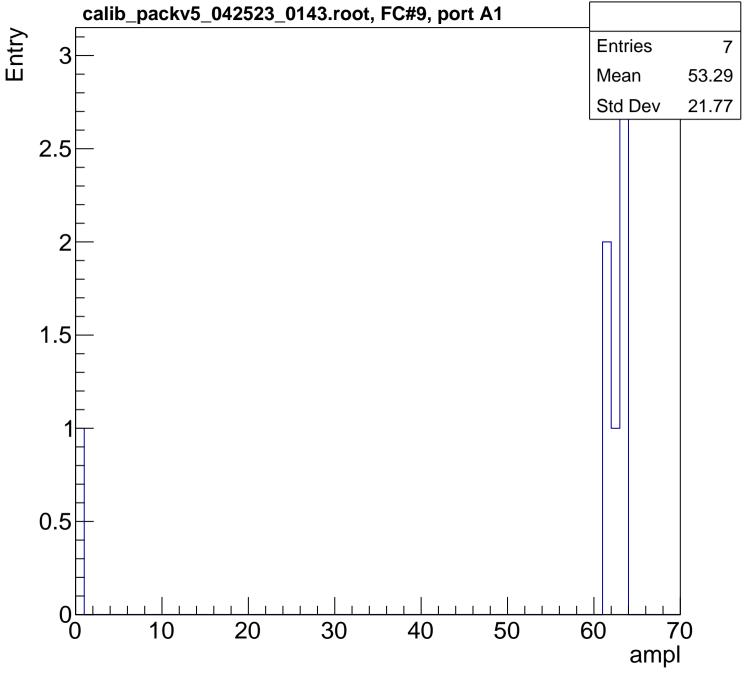




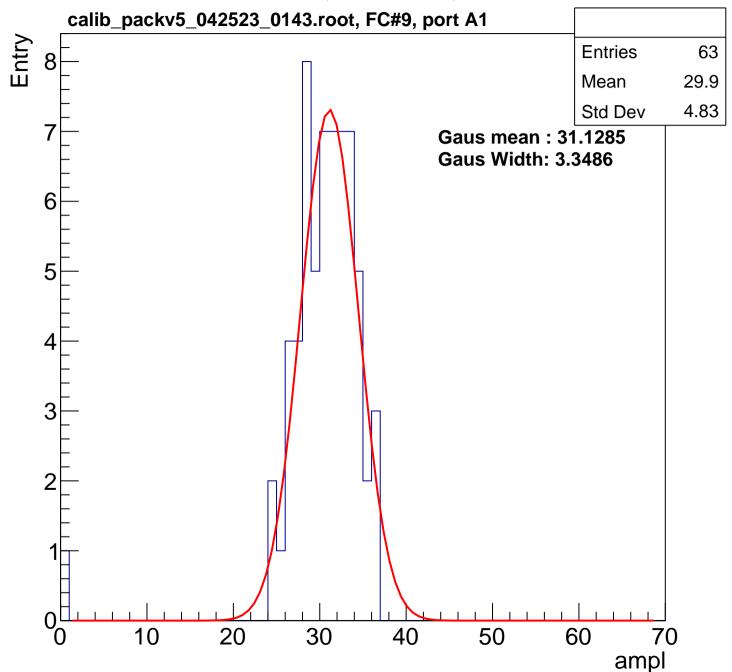


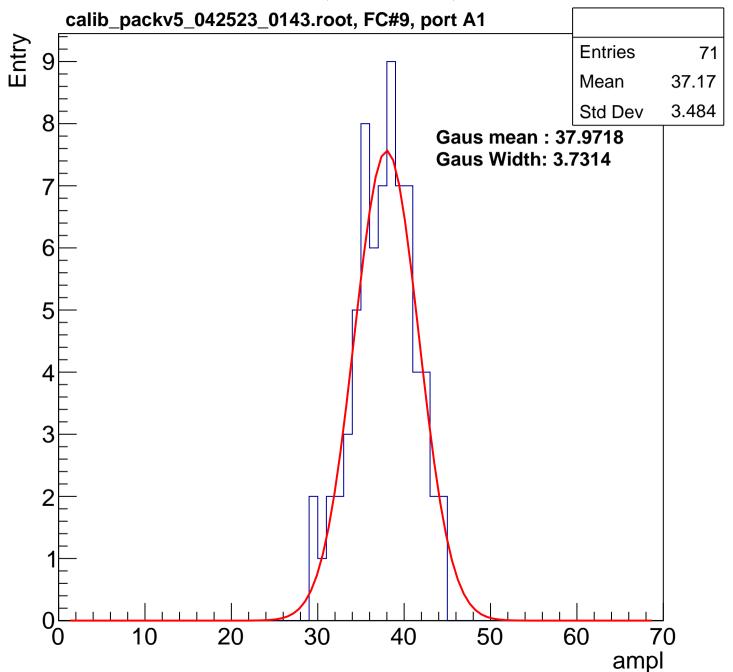


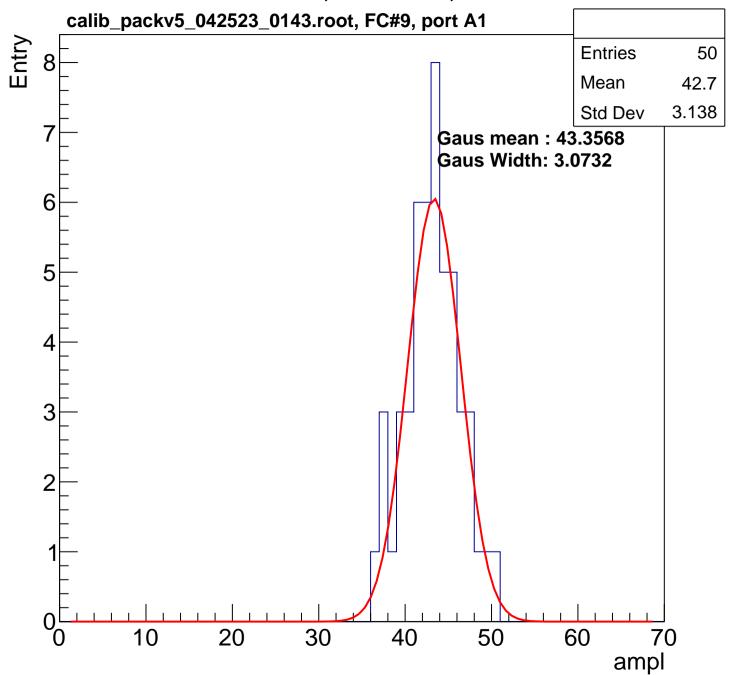


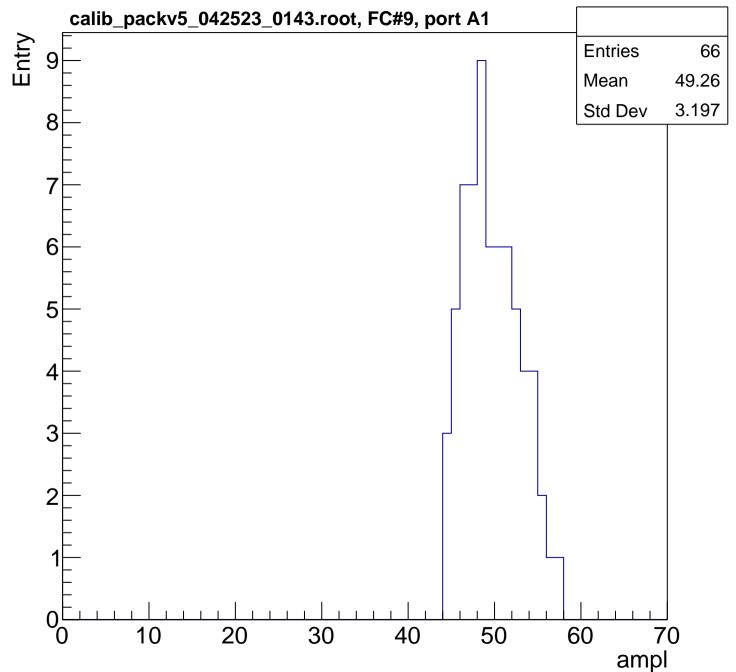


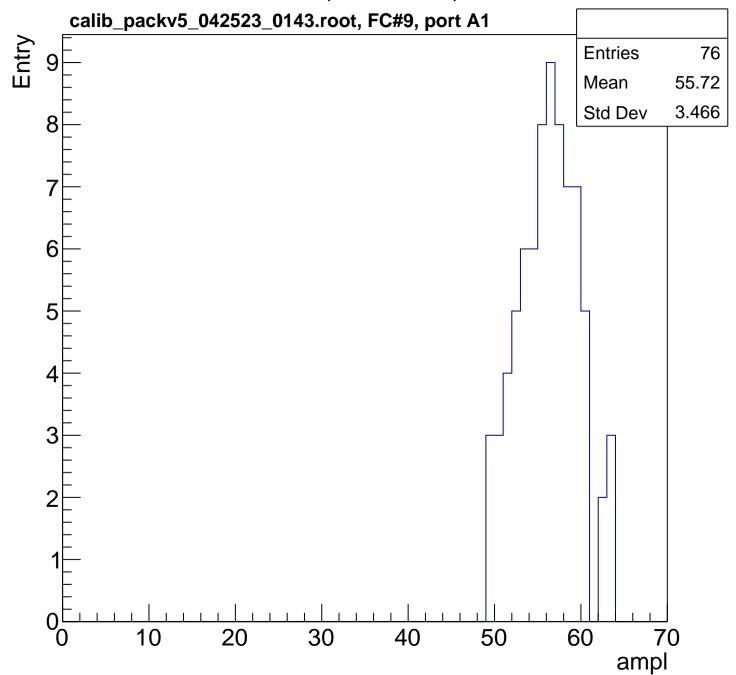
B0L001S, U3-ch8, adc7 calib_packv5_042523_0143.root, FC#9, port A1 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

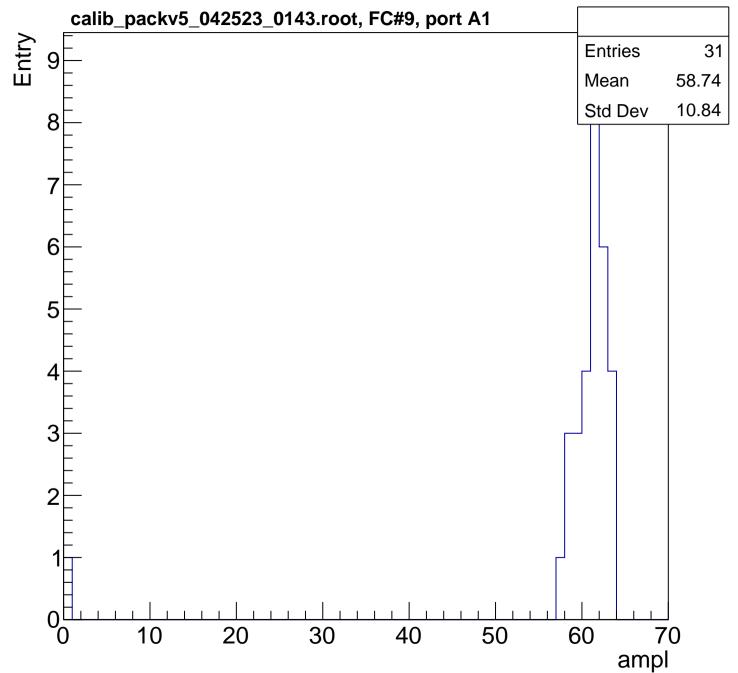


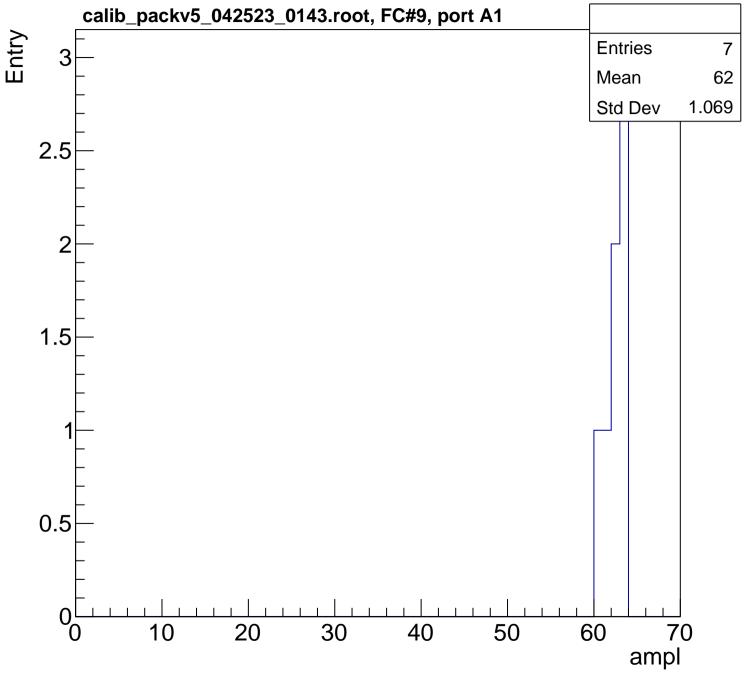


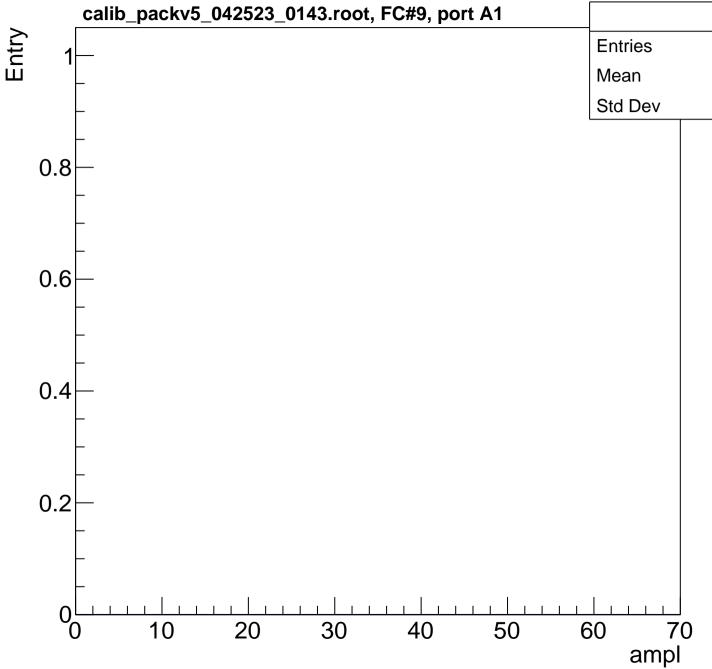


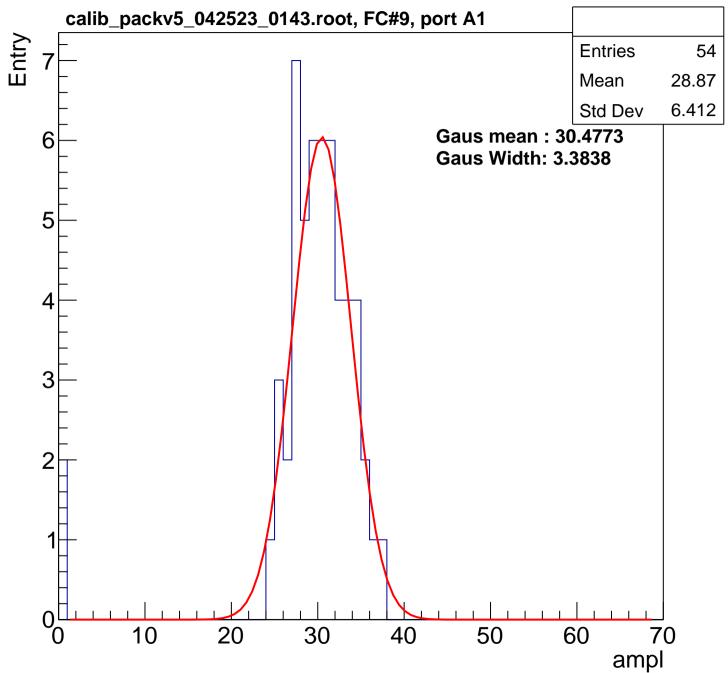


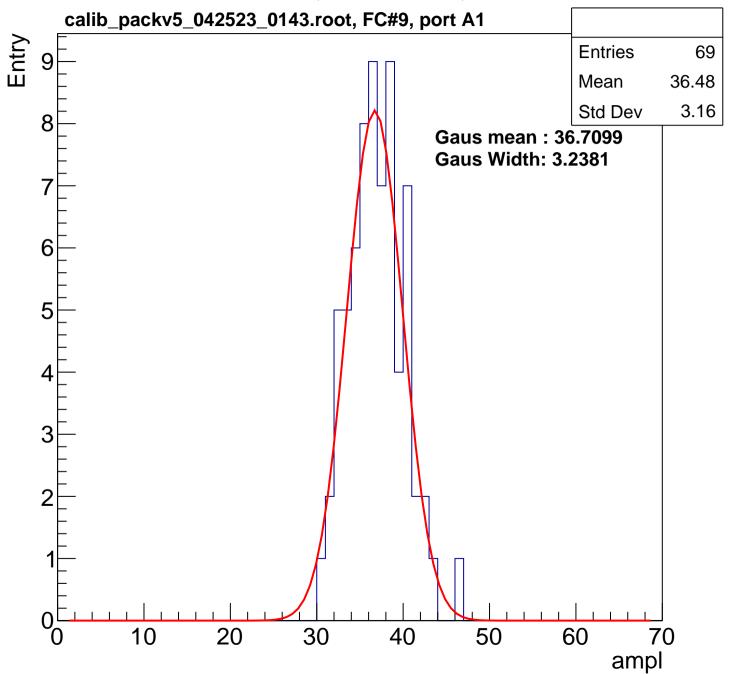


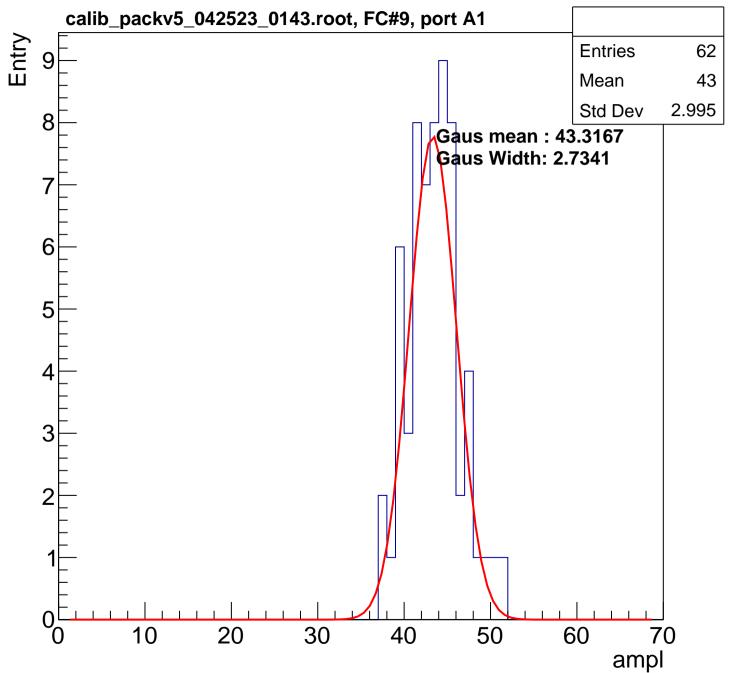


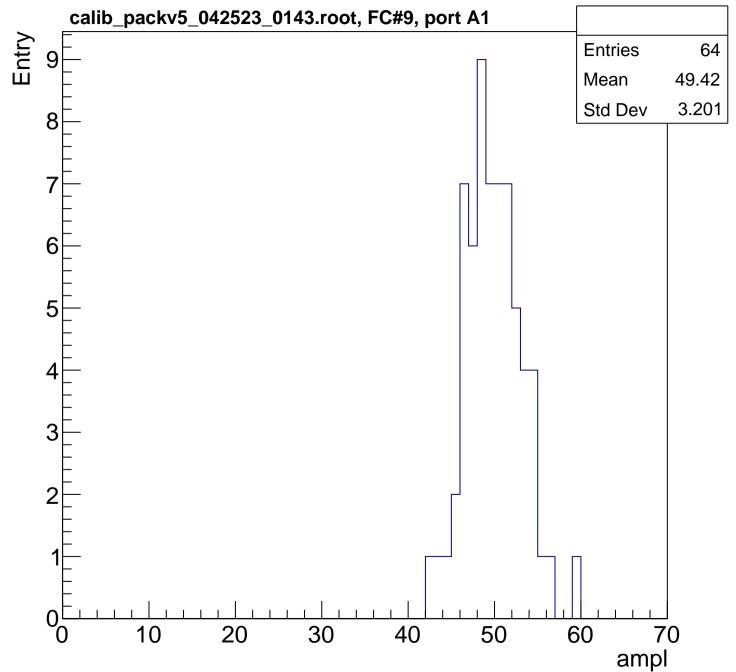


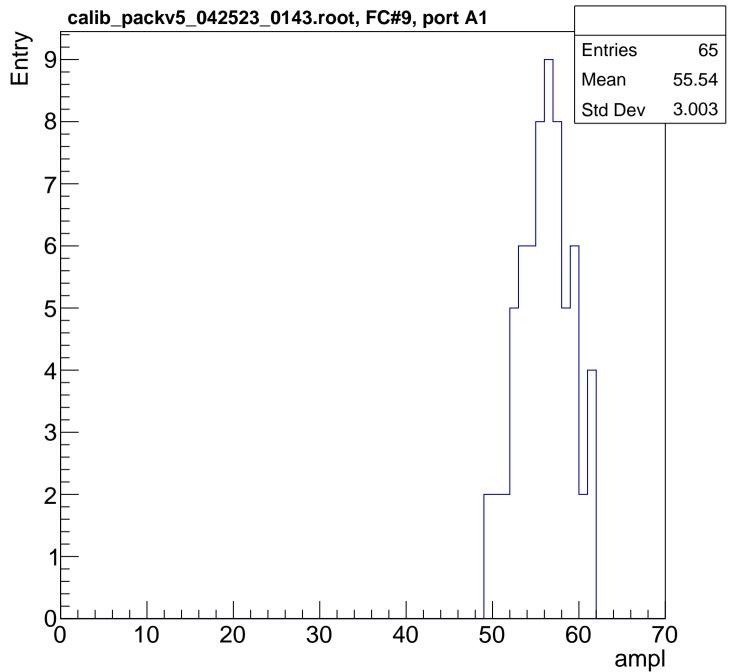


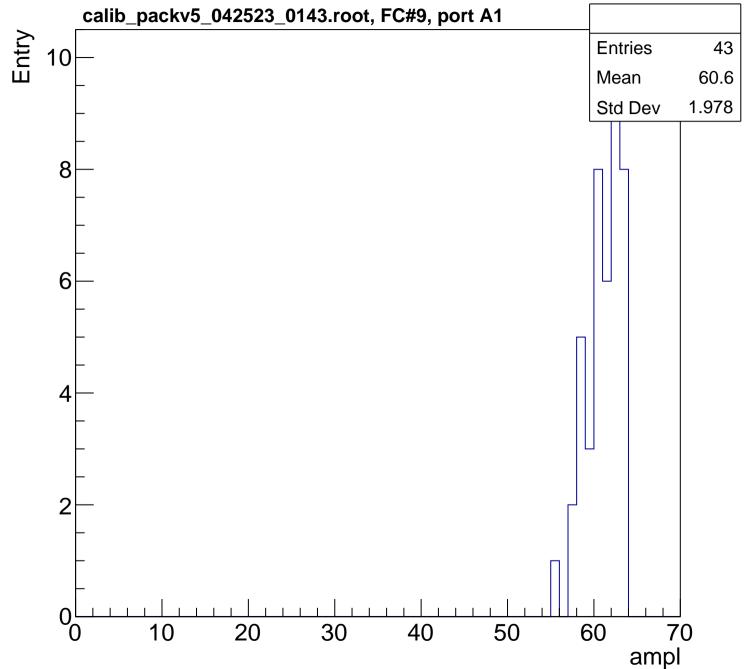


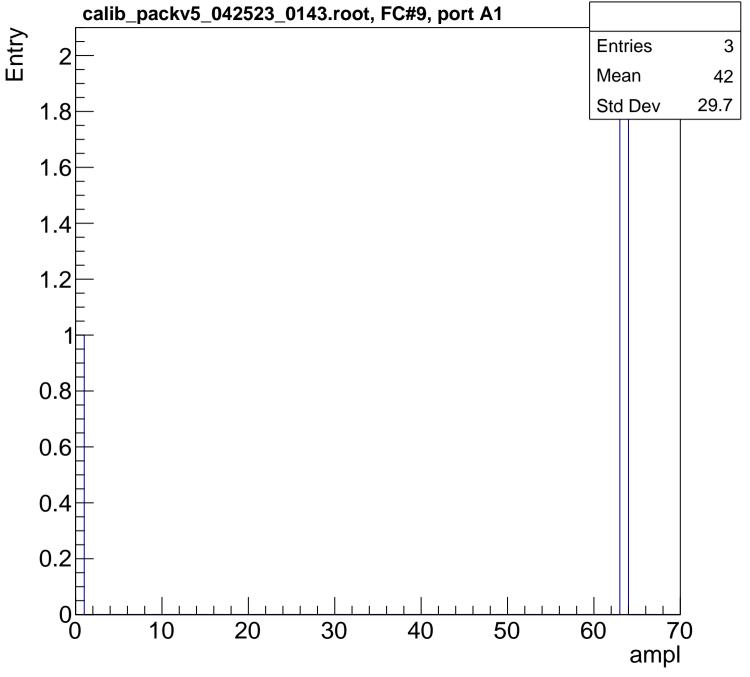








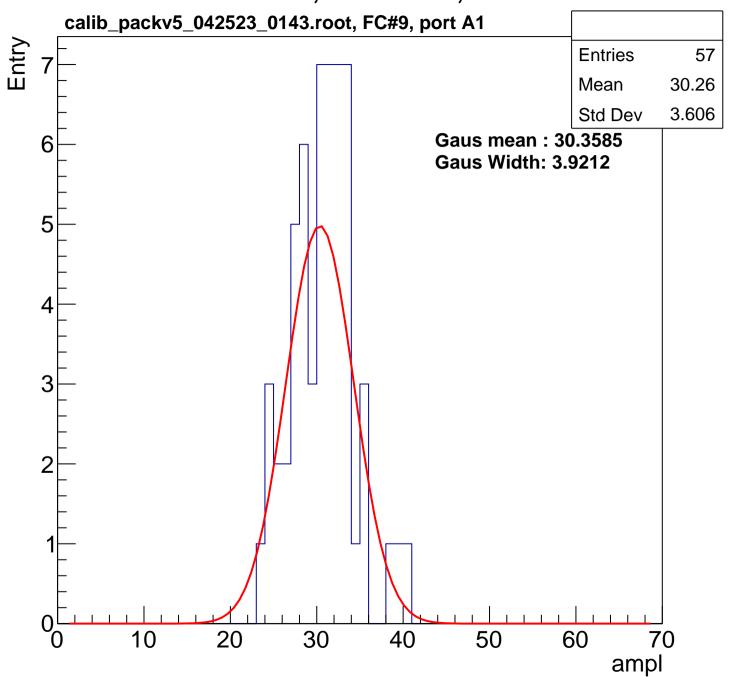


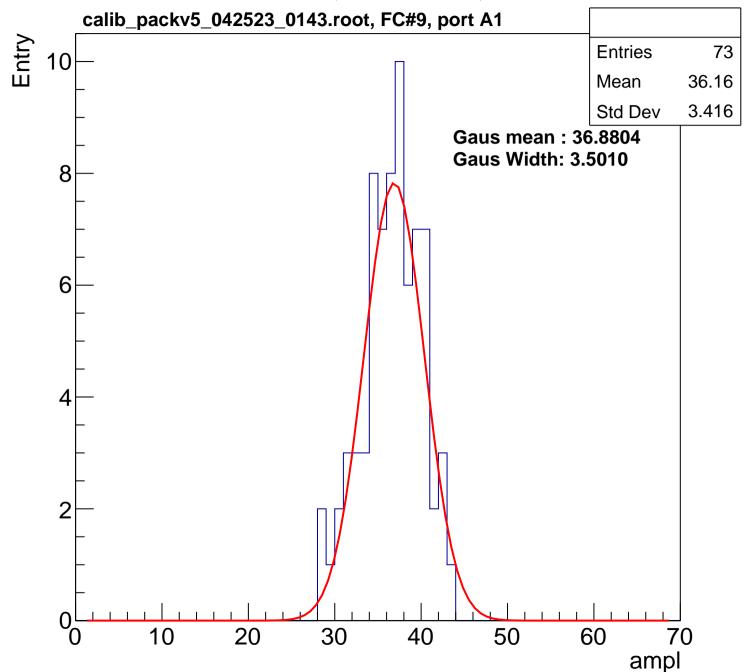


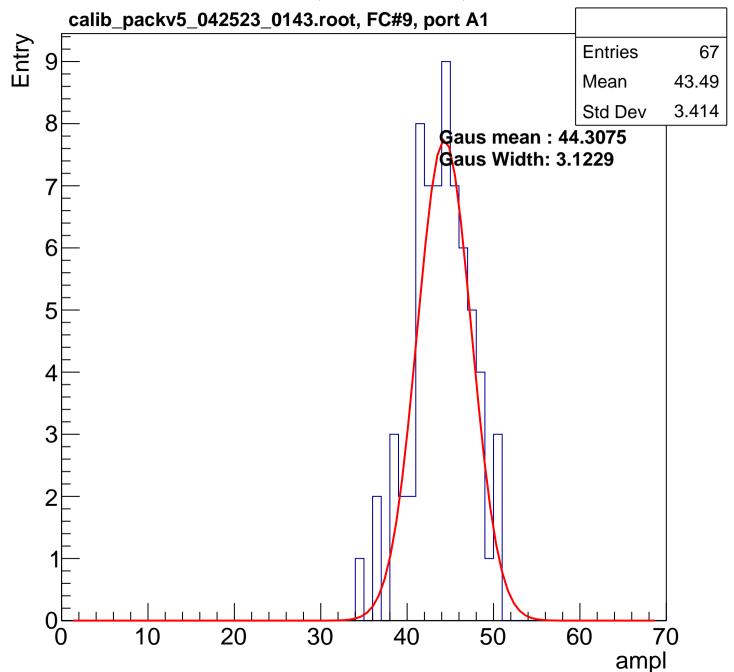
B0L001S, U3-ch10, adc7 calib_packv5_042523_0143.root, FC#9, port A1 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60

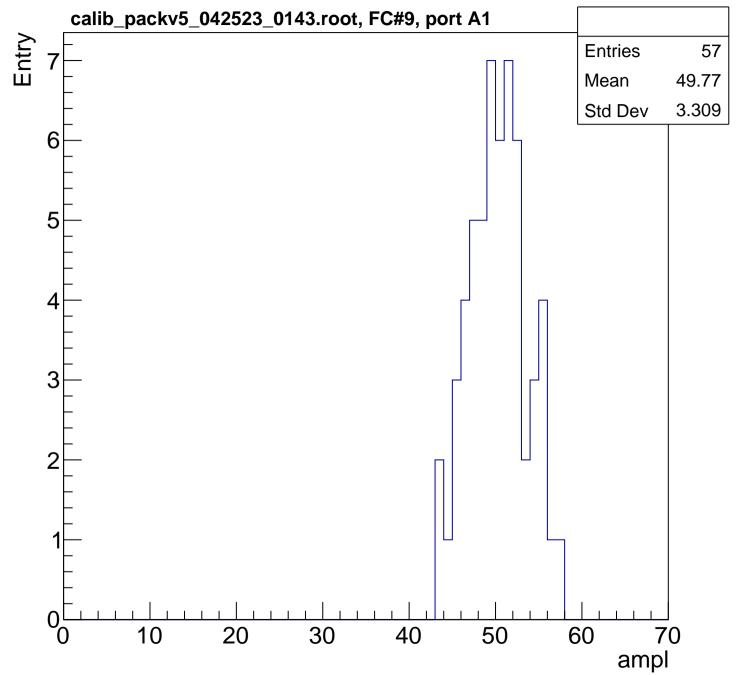
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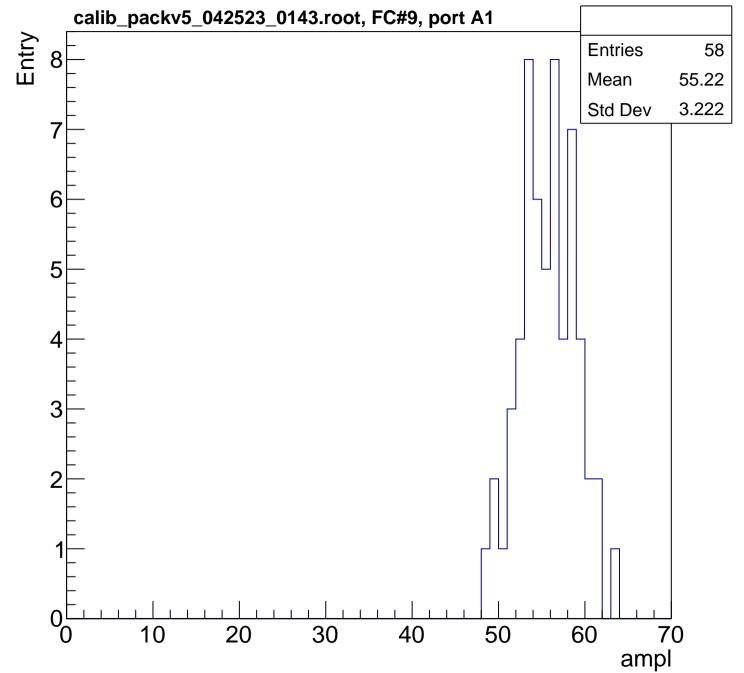
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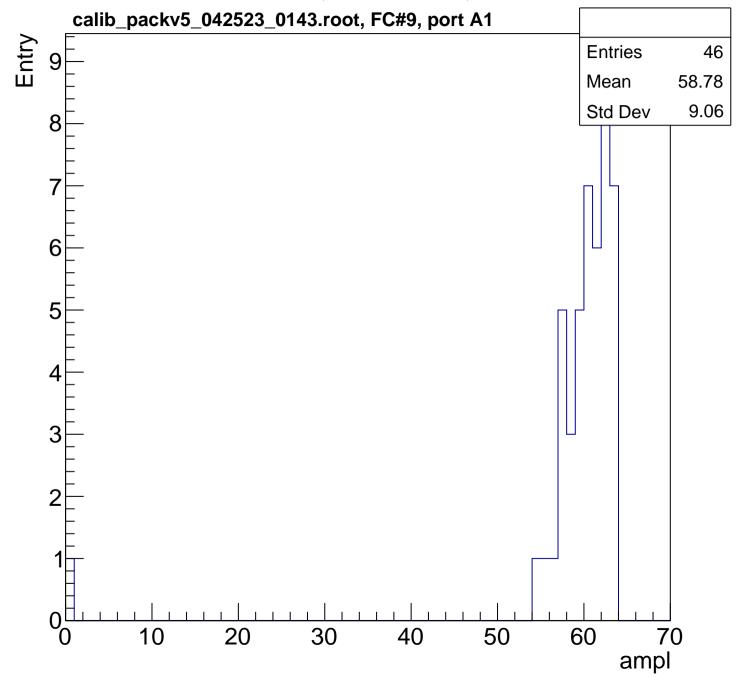


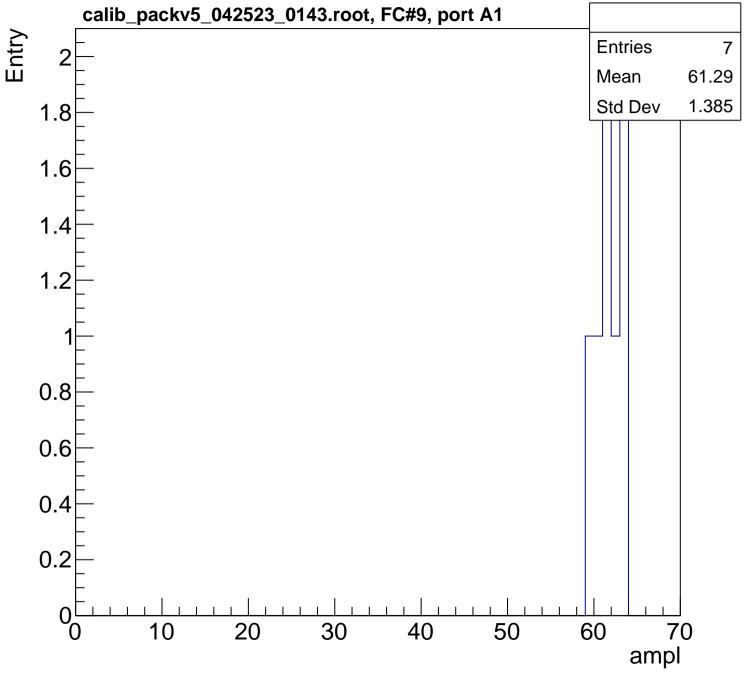


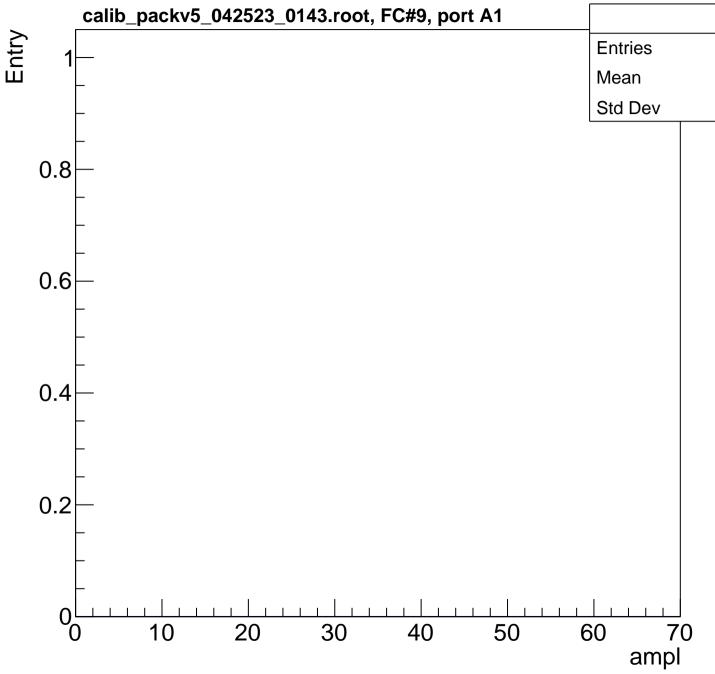


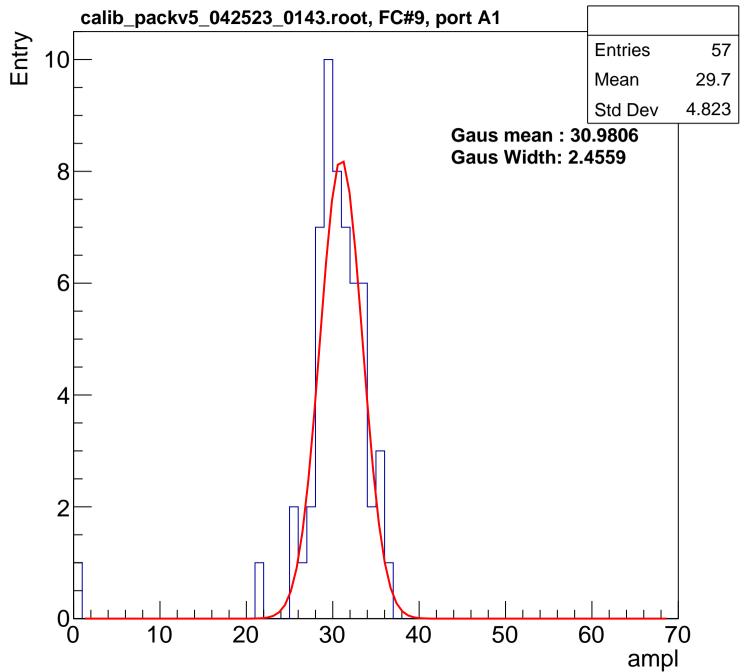


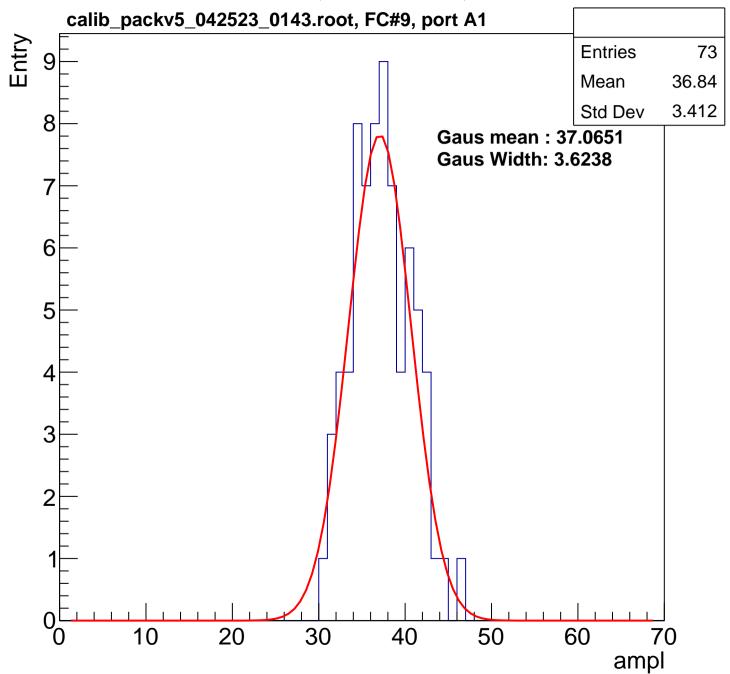


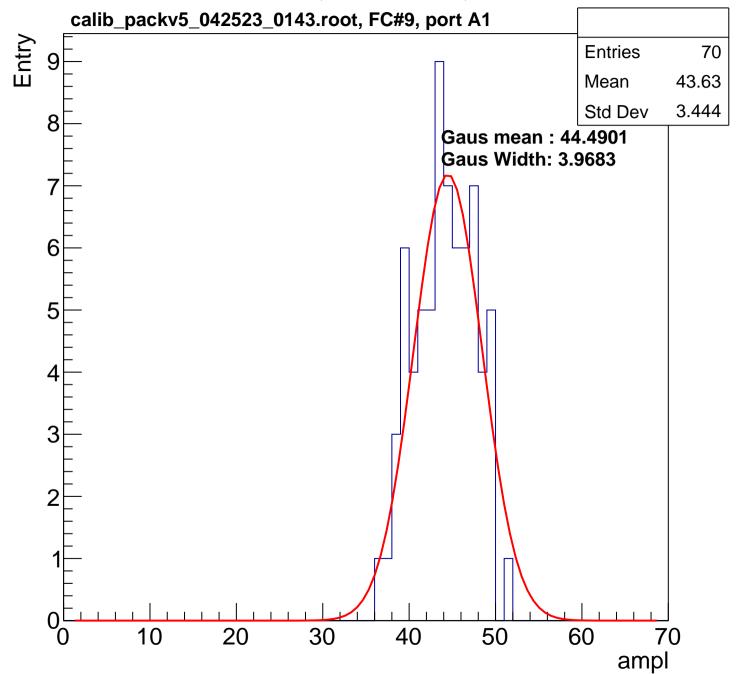


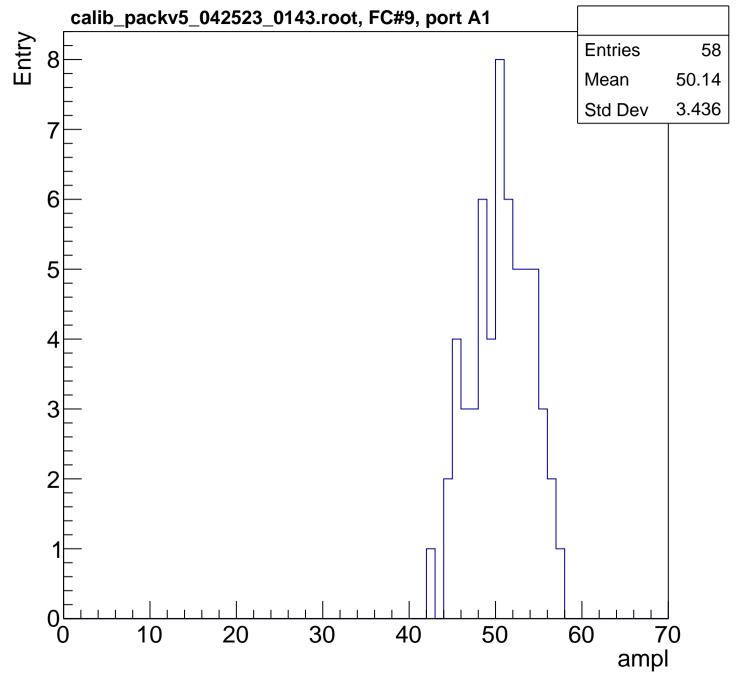


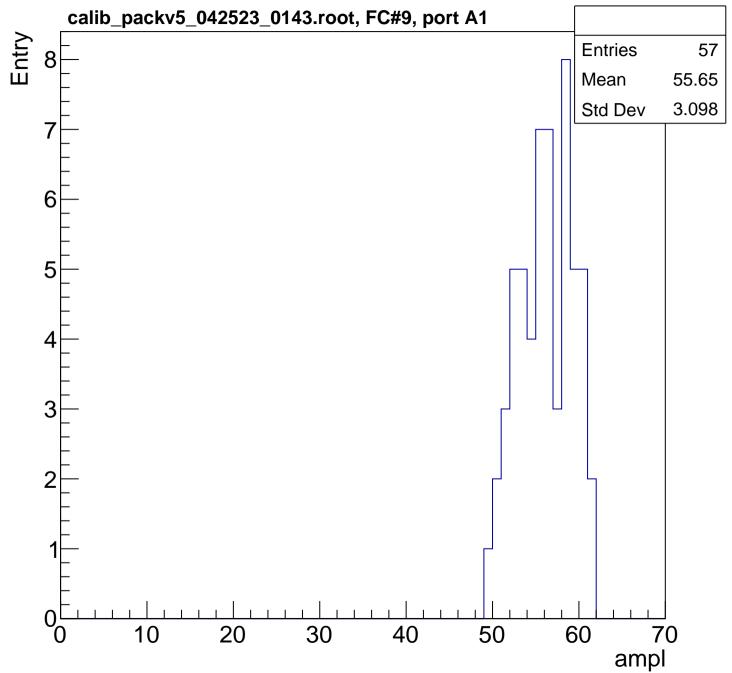


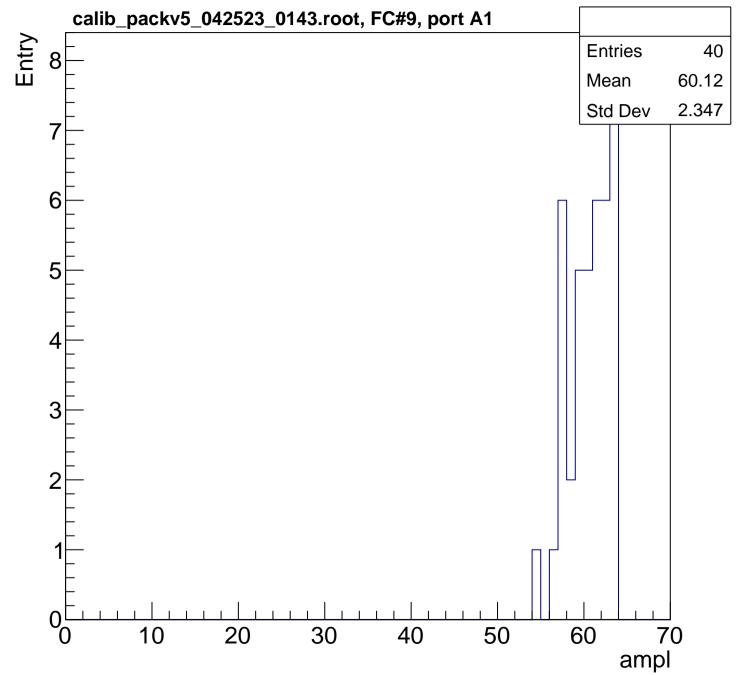


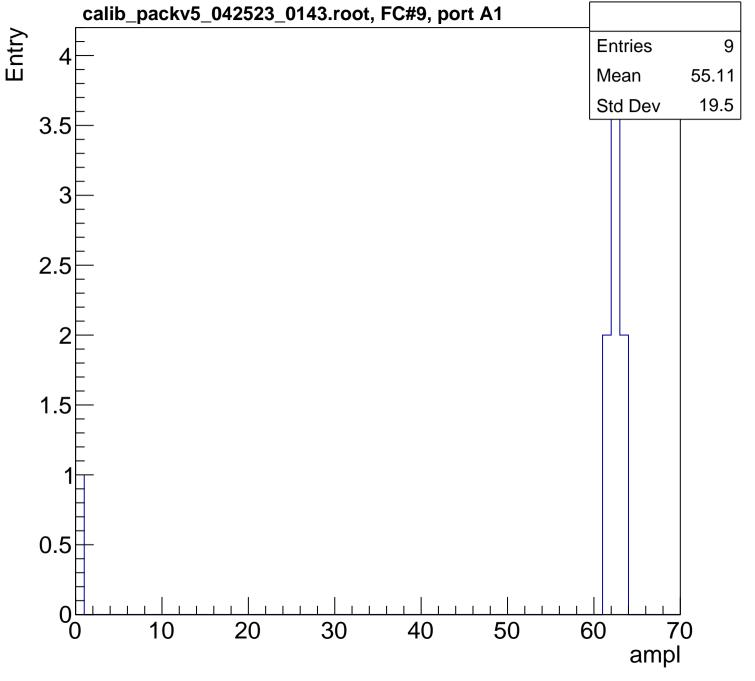




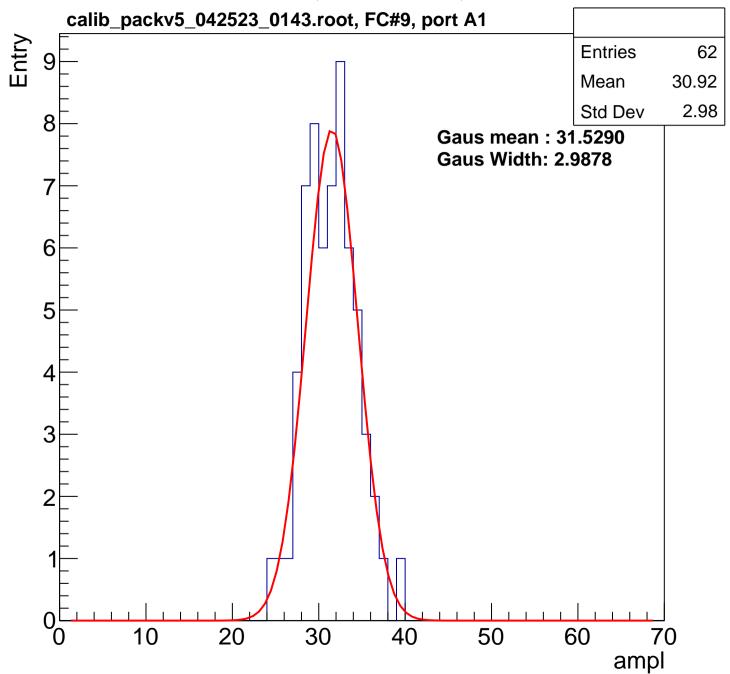


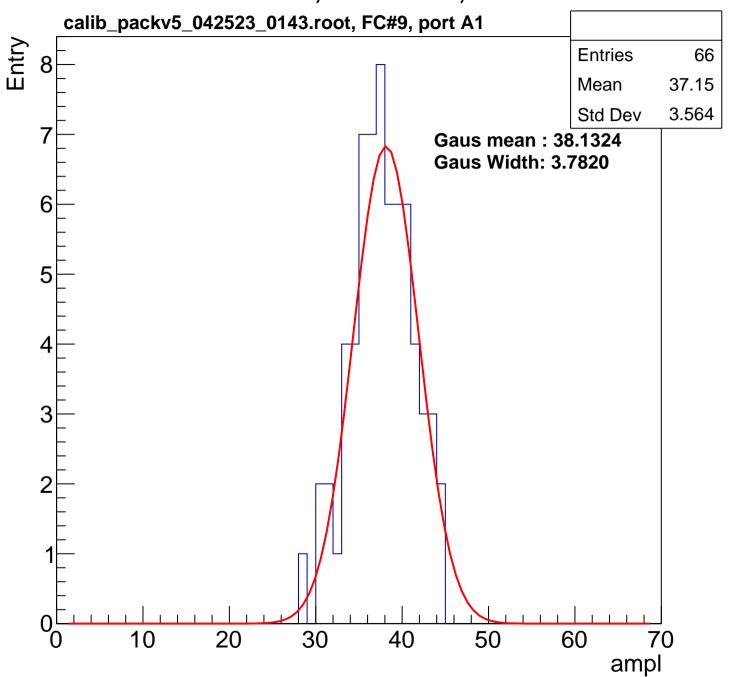


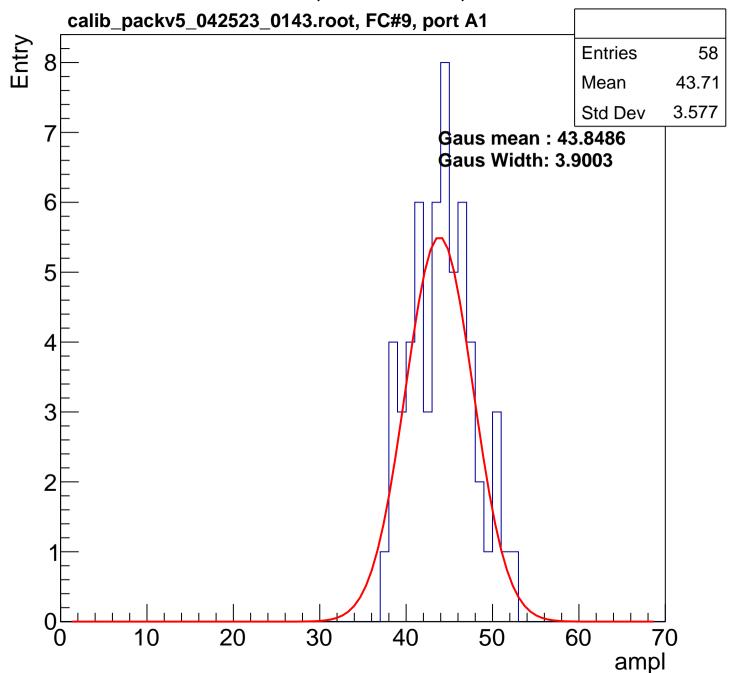


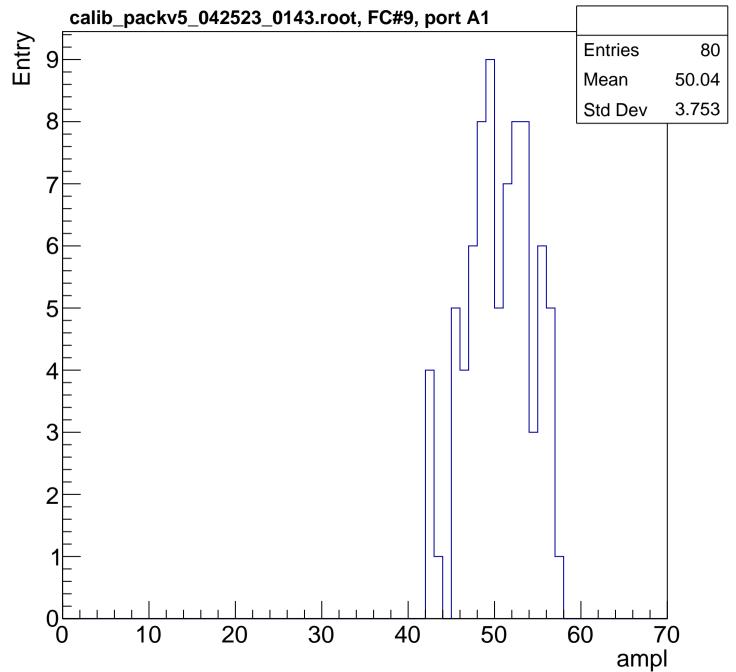


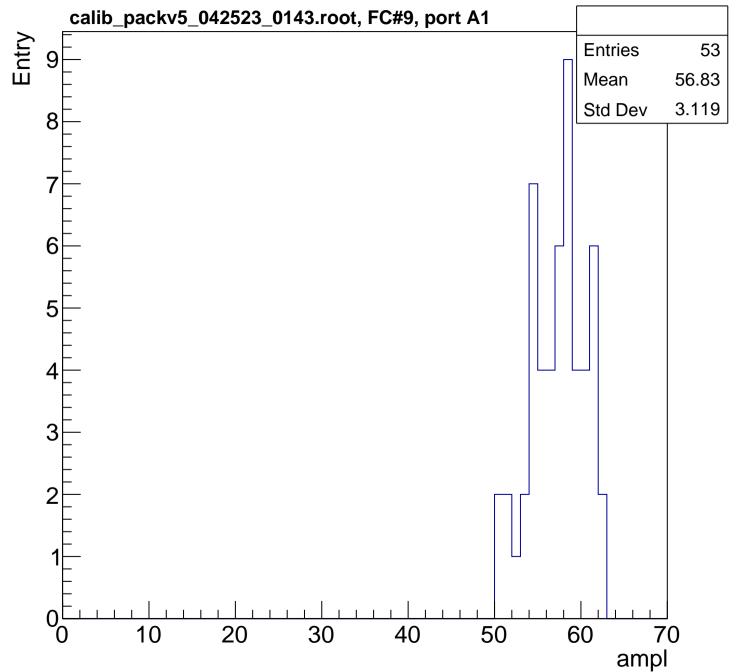


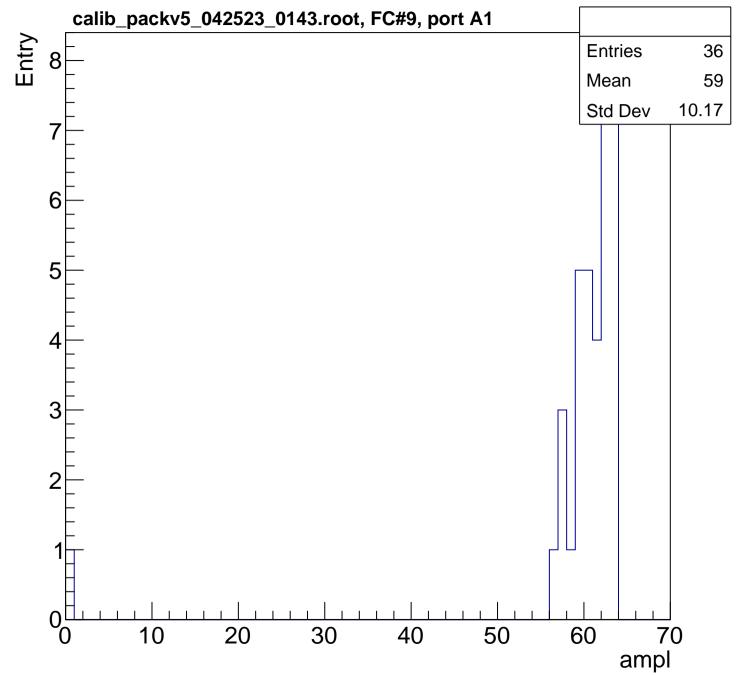


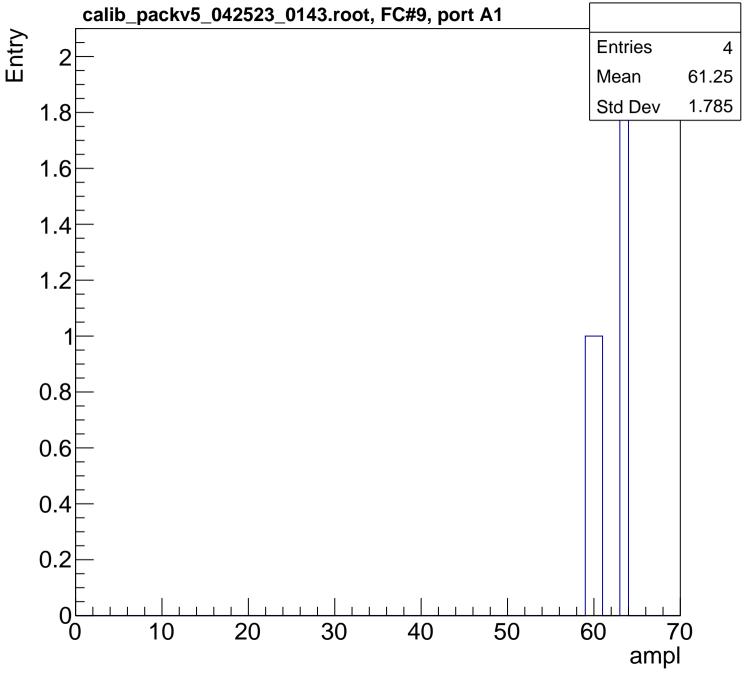


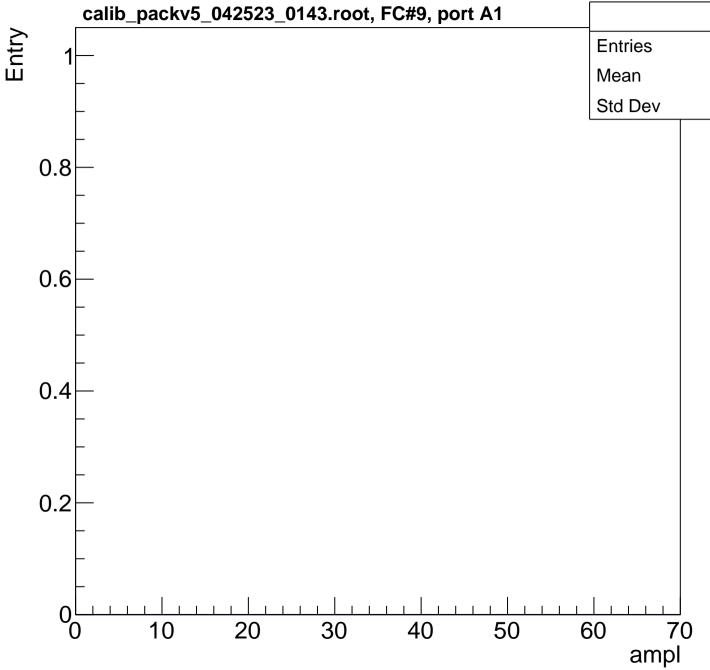


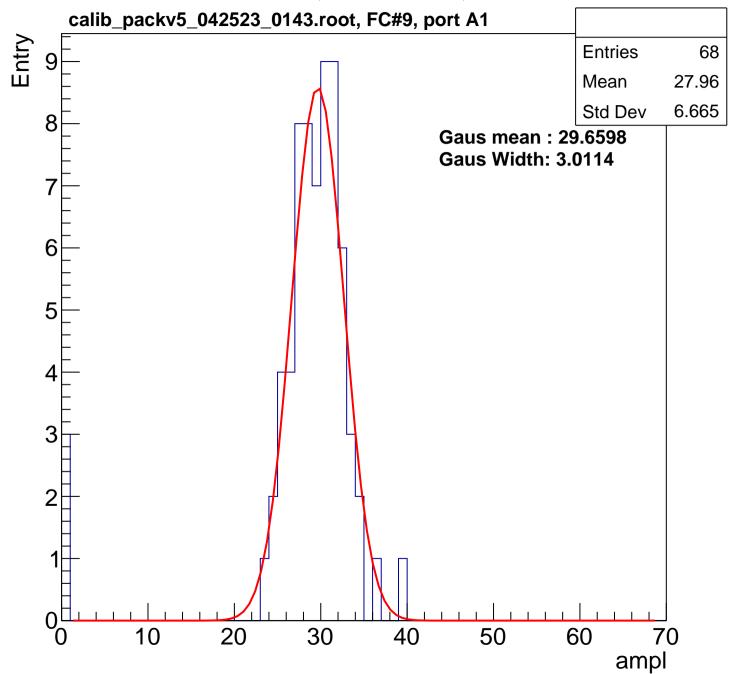


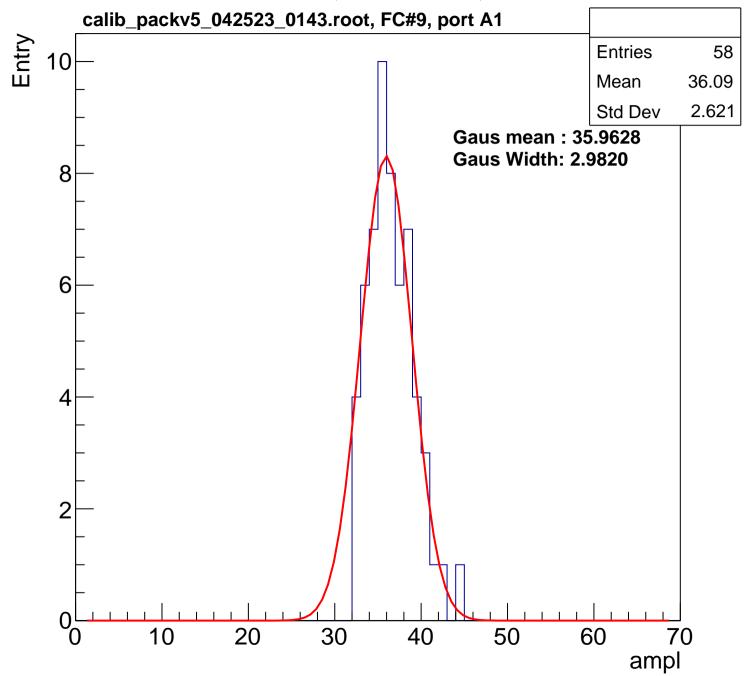


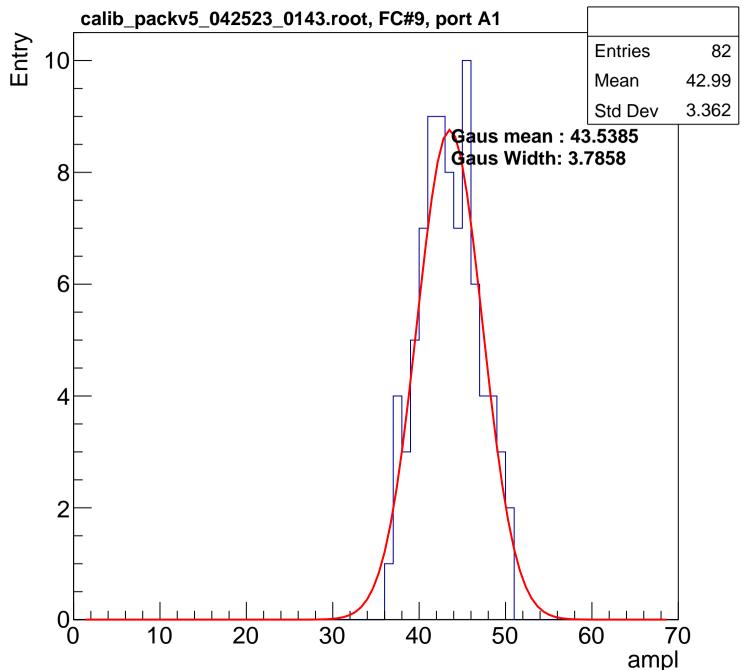


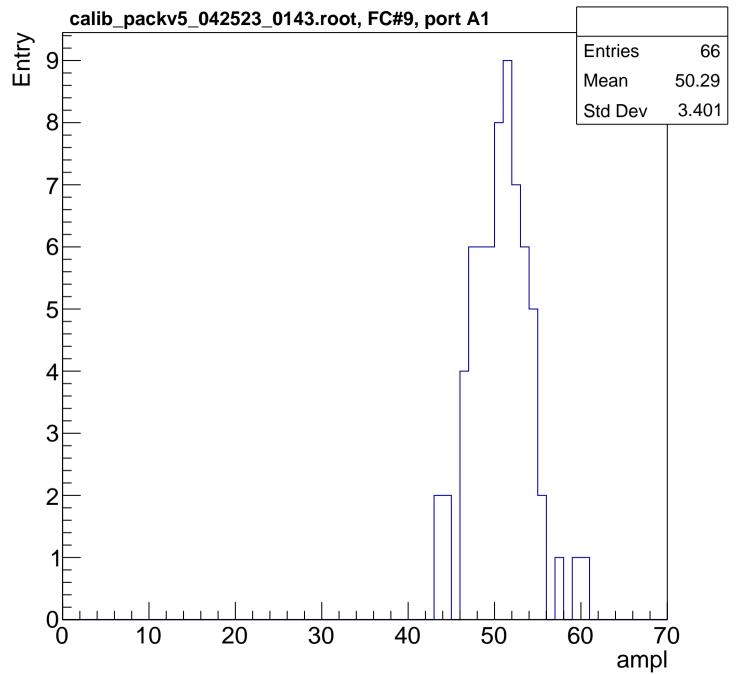


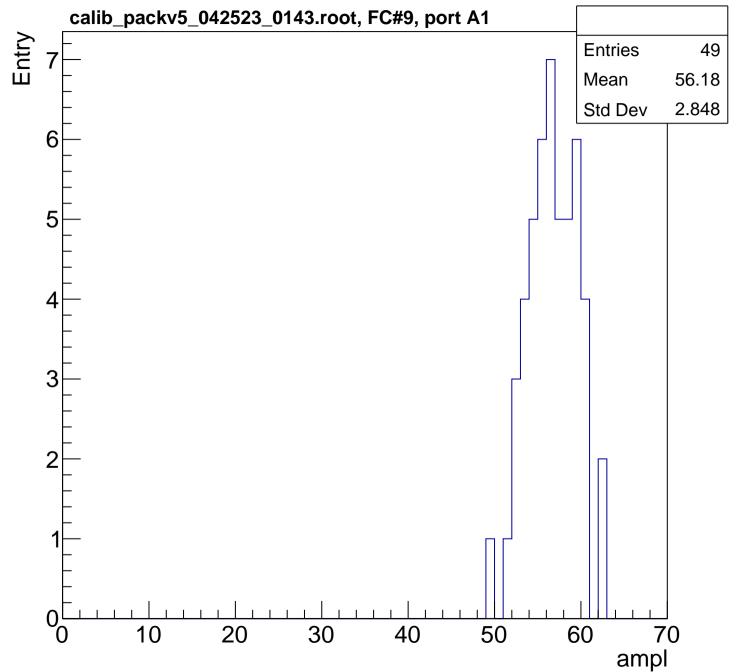


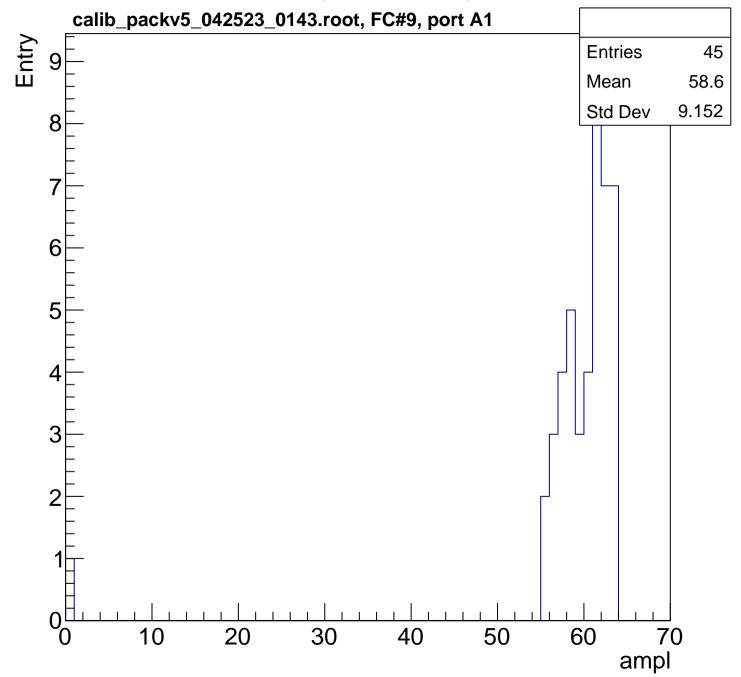


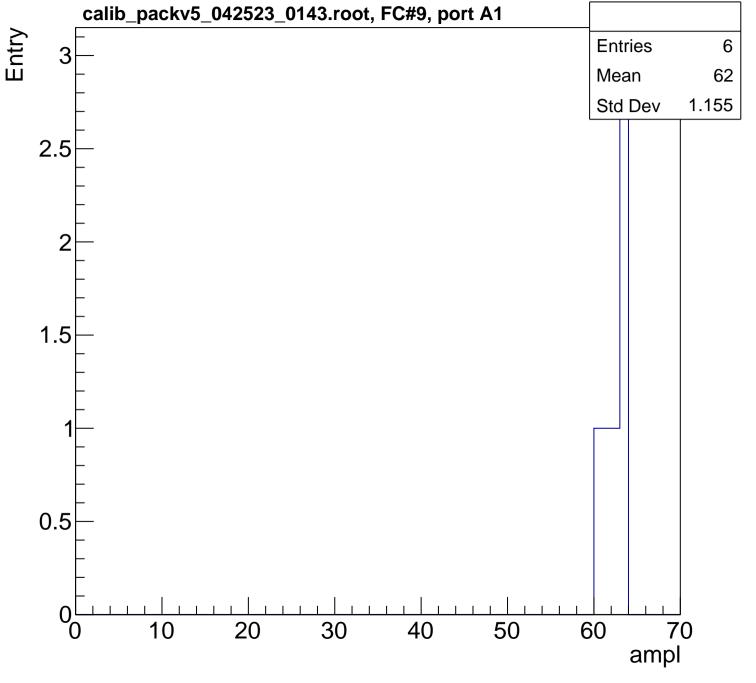




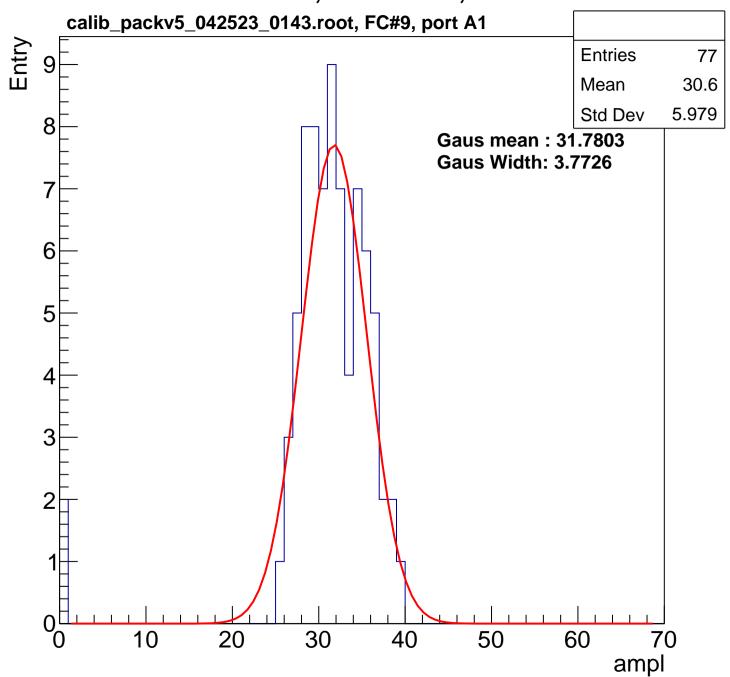


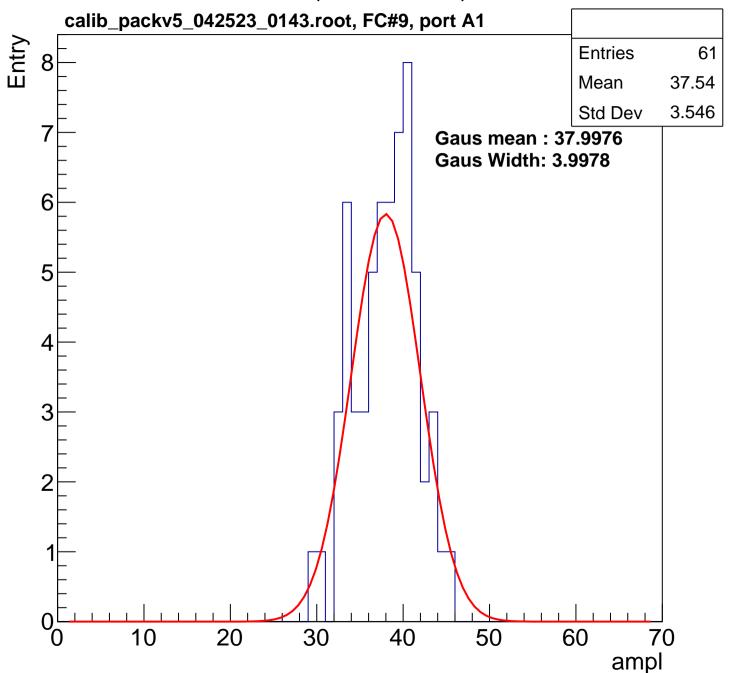


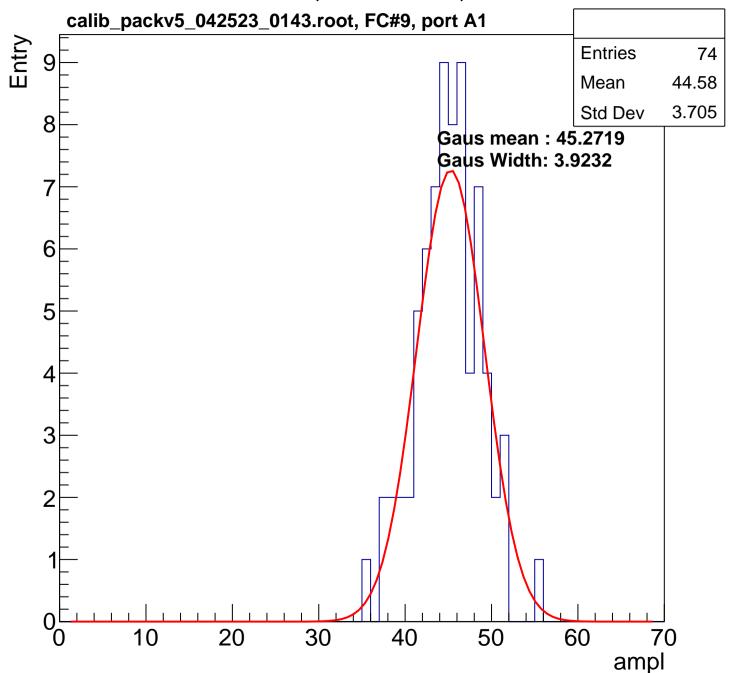


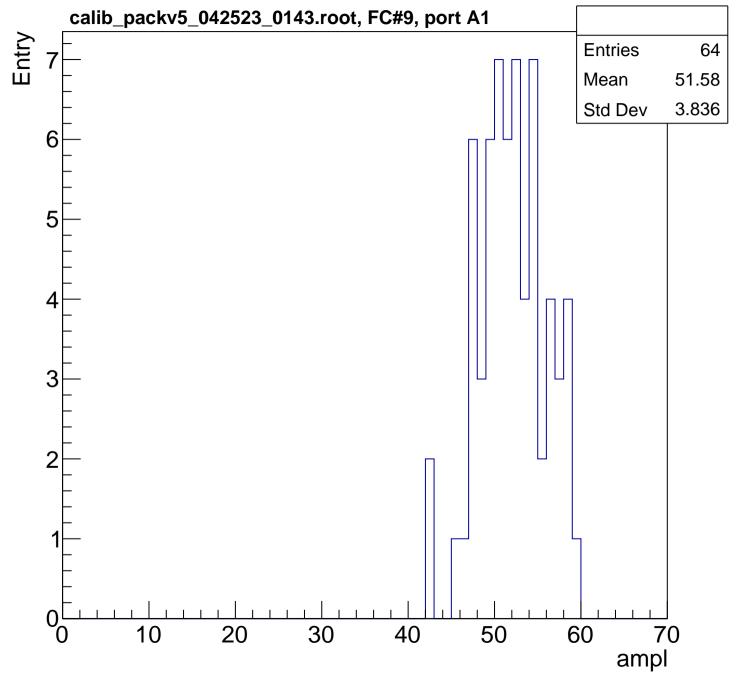


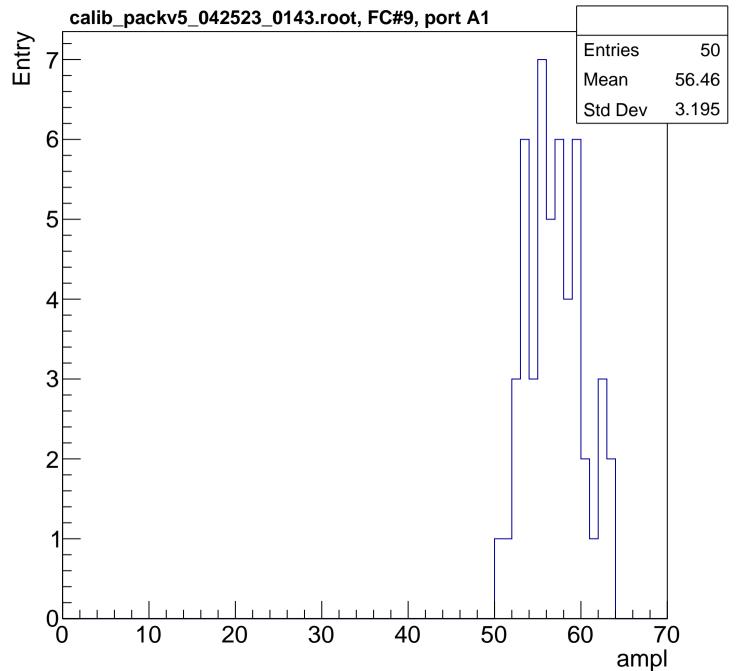


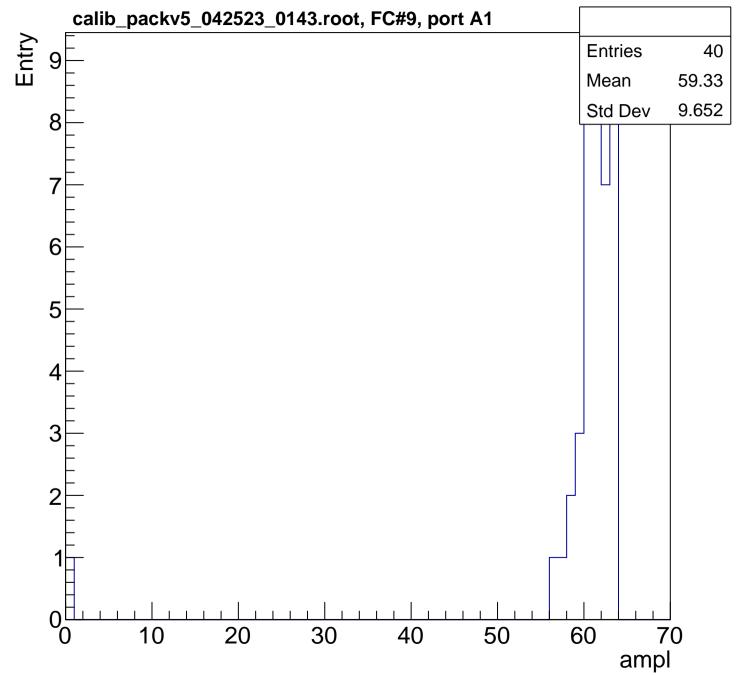


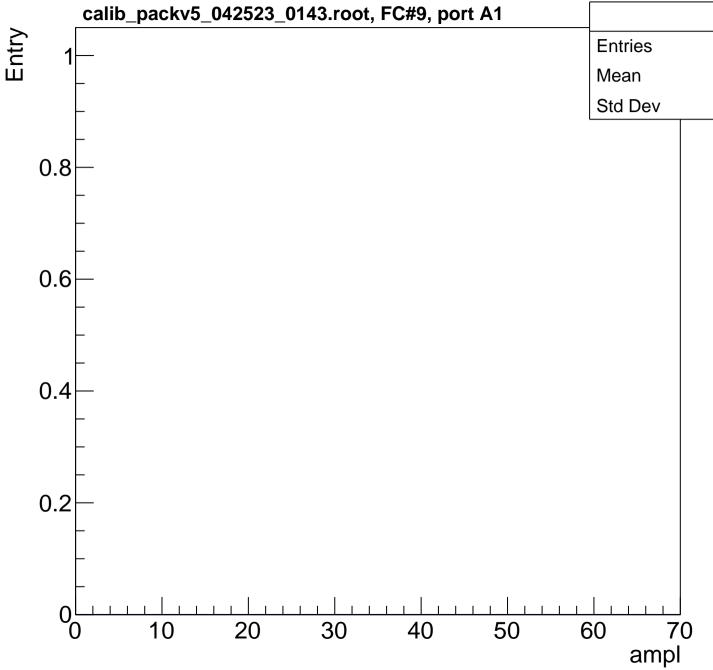






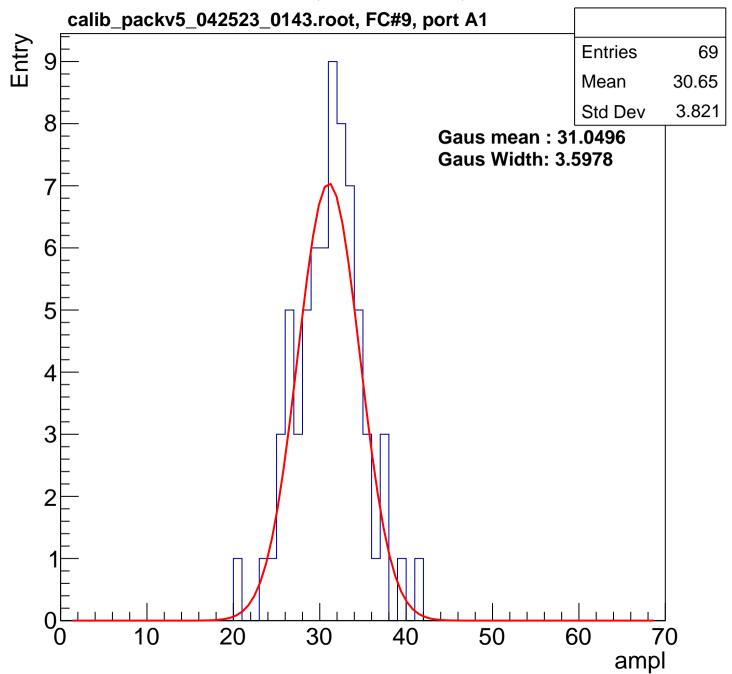


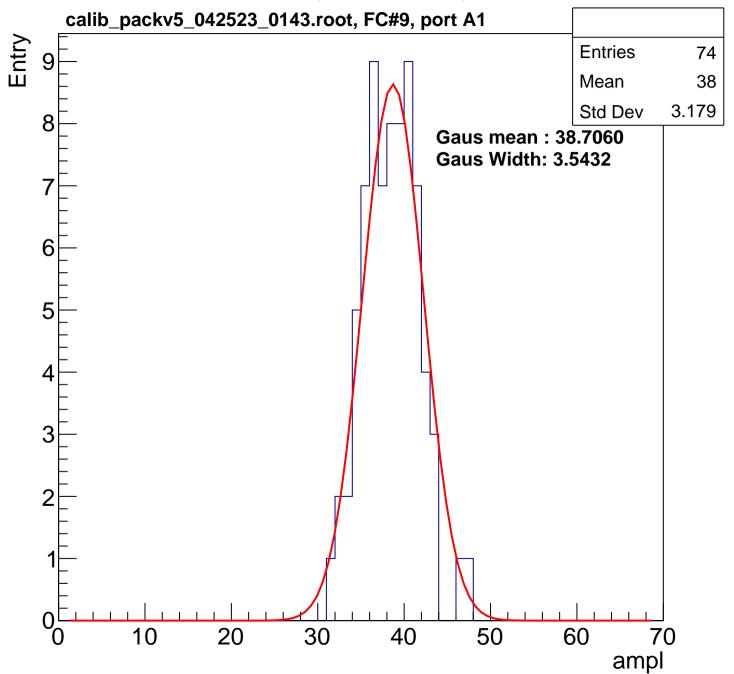


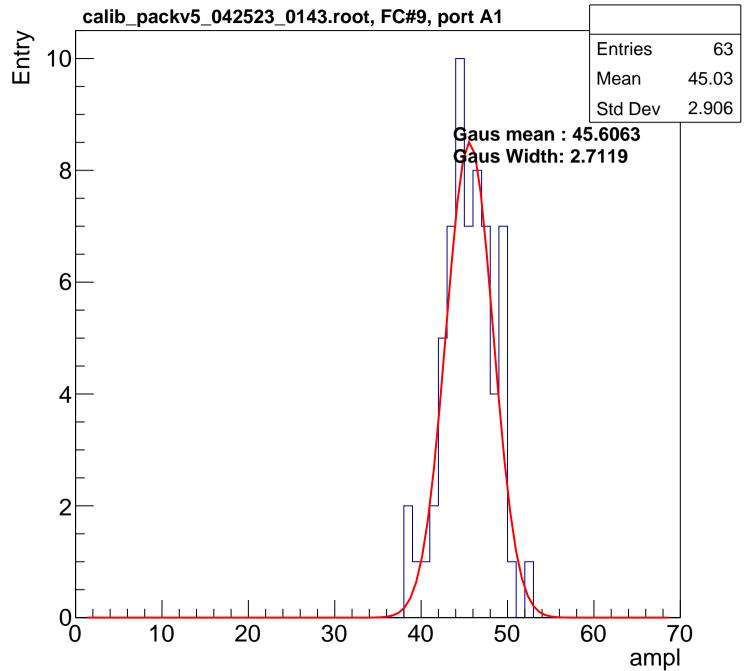


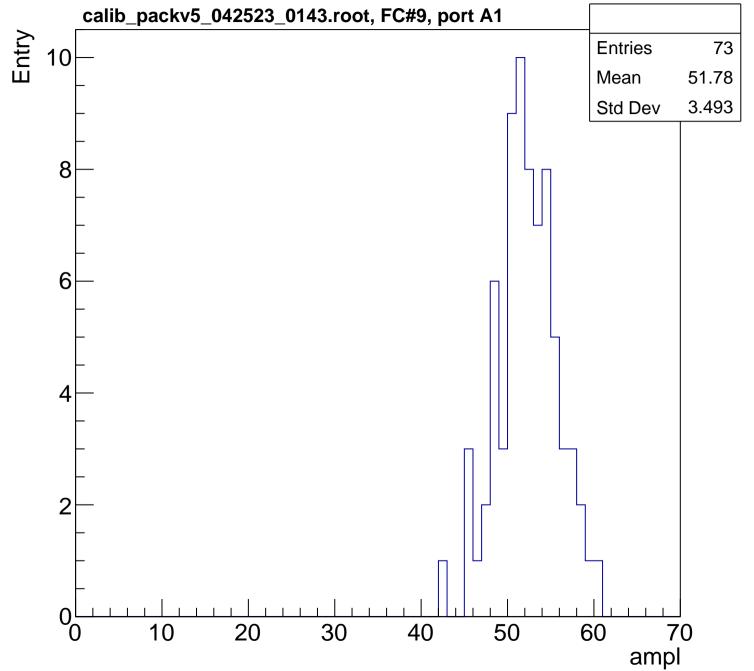
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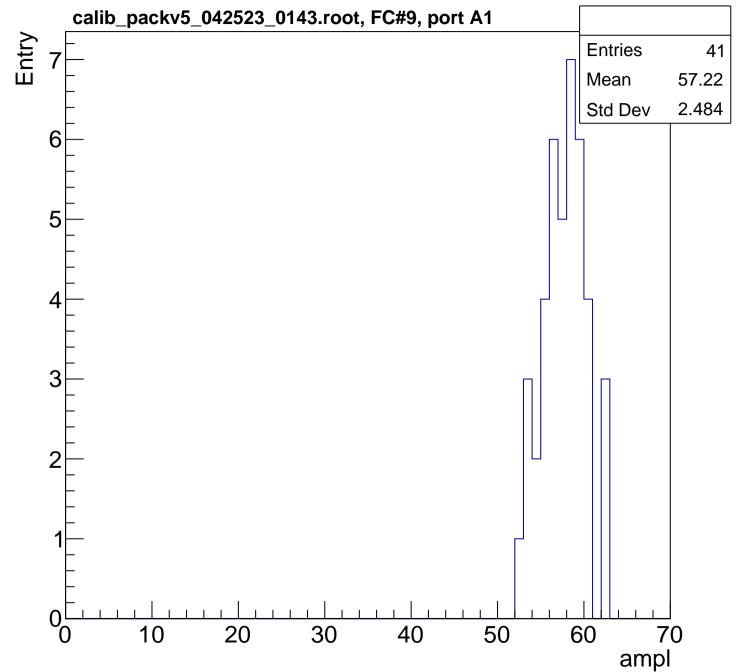


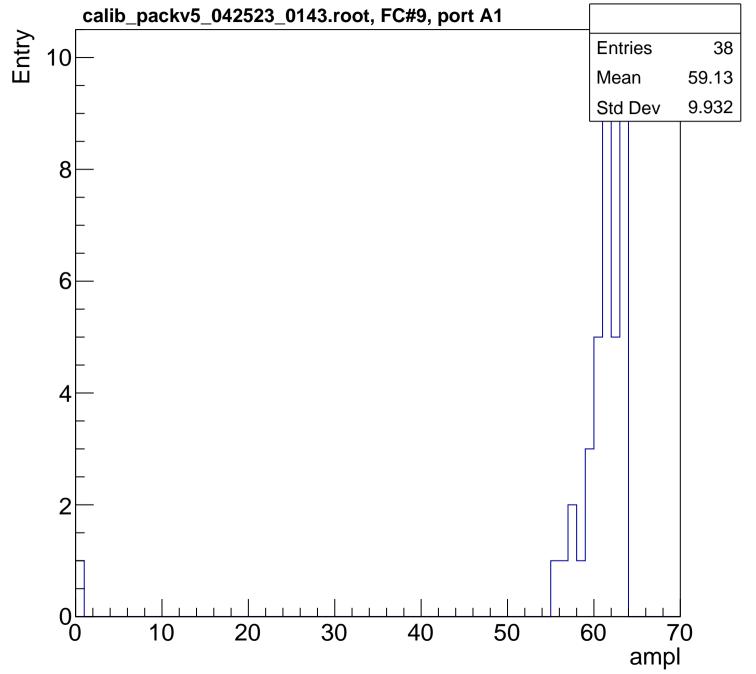


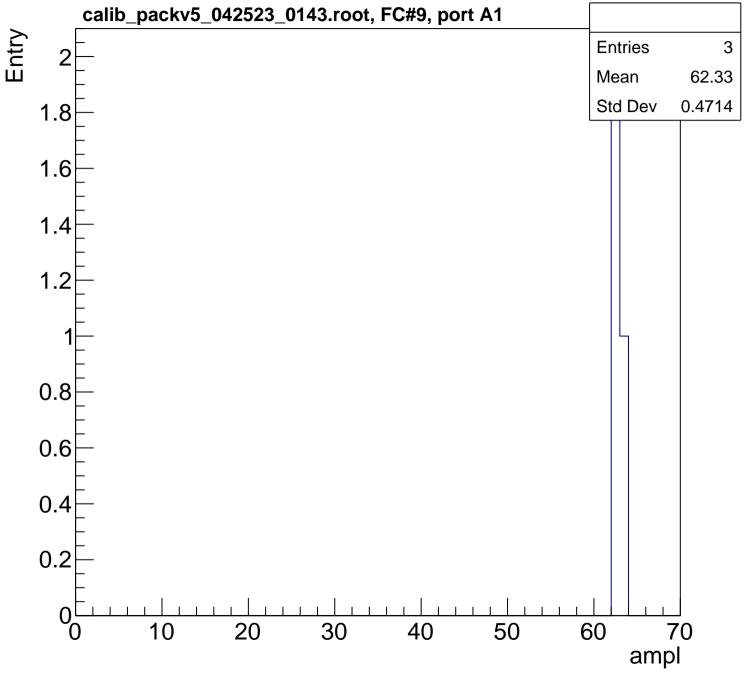










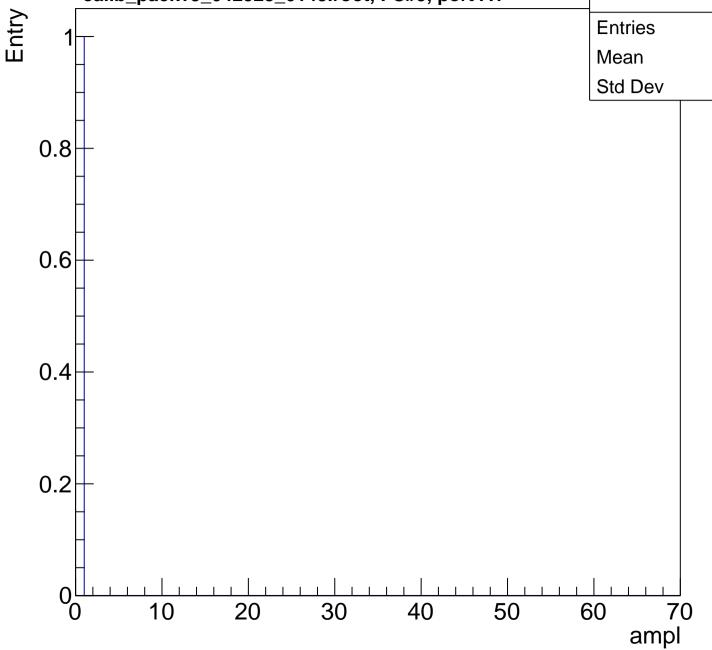


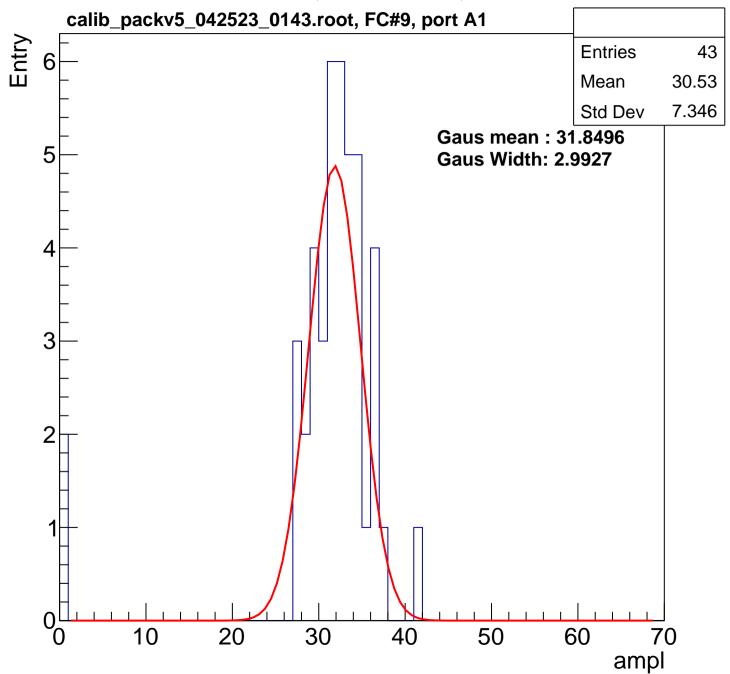
B0L001S, U3-ch16, adc7 calib_packv5_042523_0143.root, FC#9, port A1

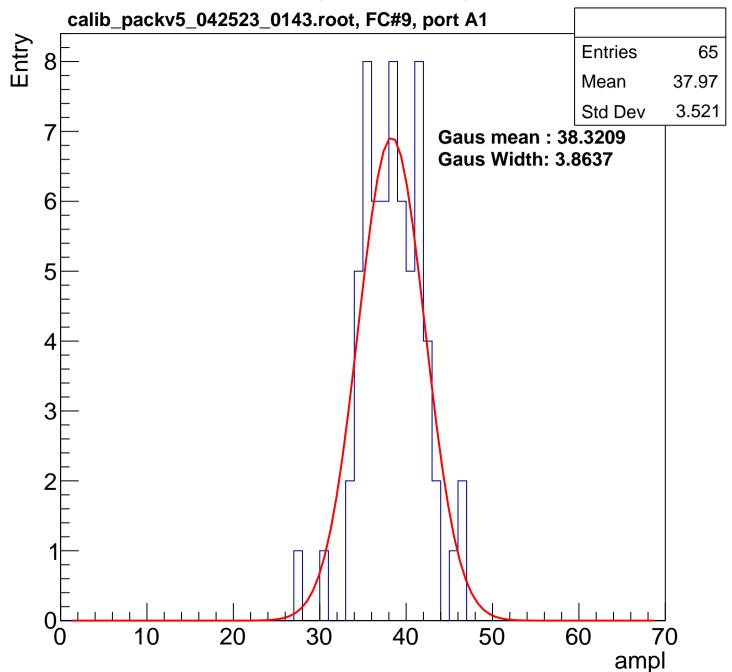
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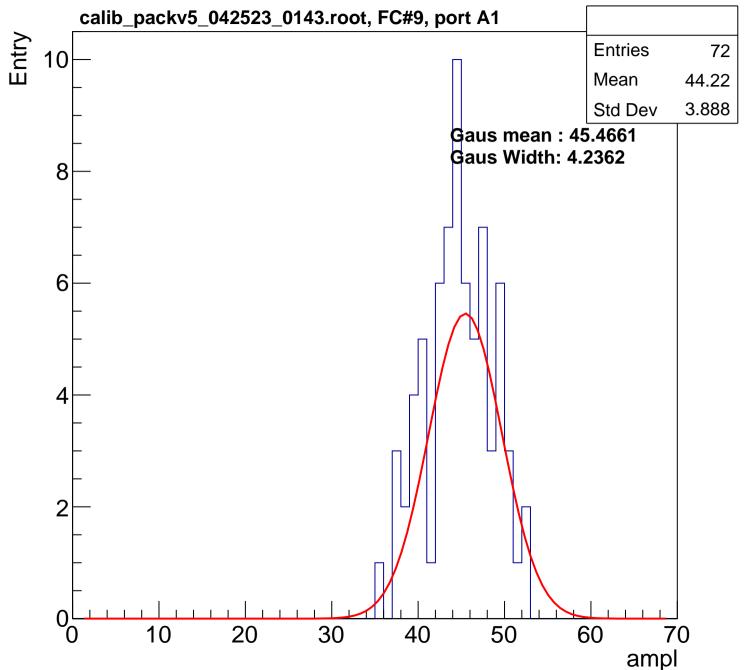
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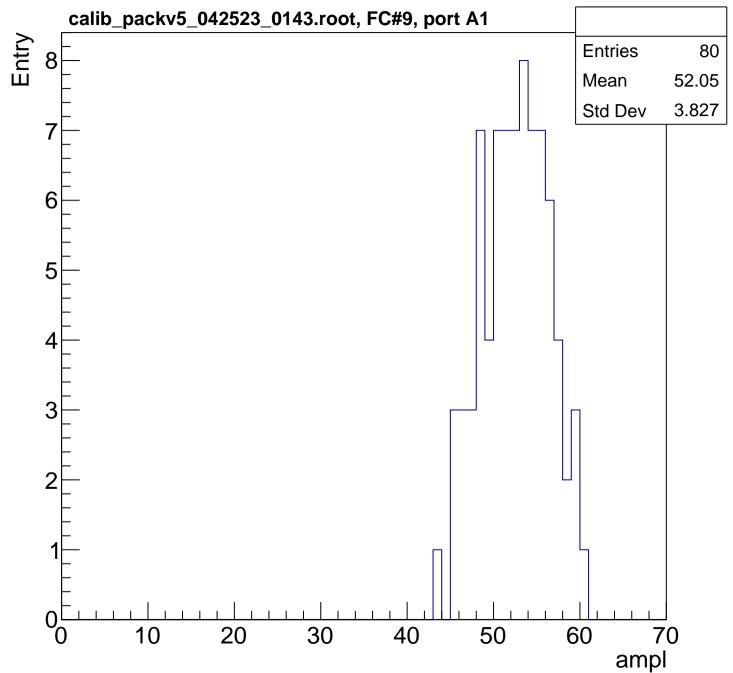
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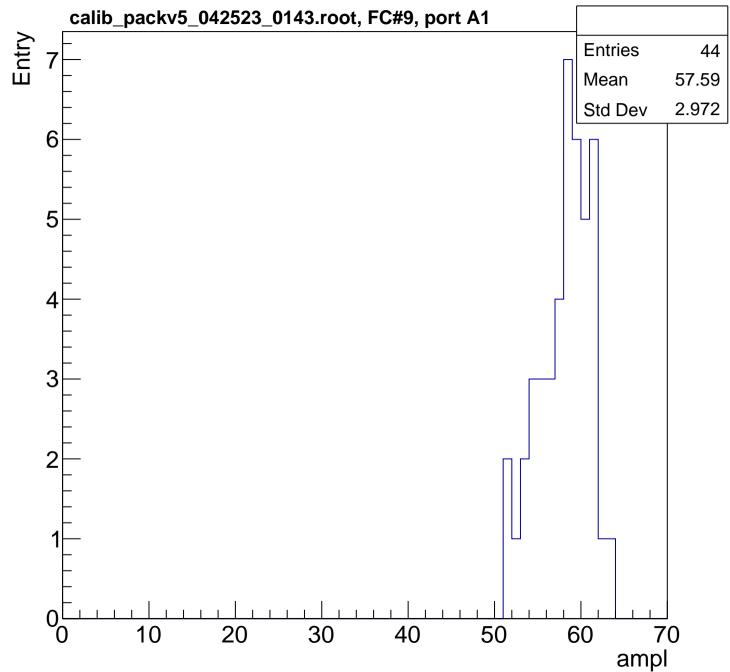


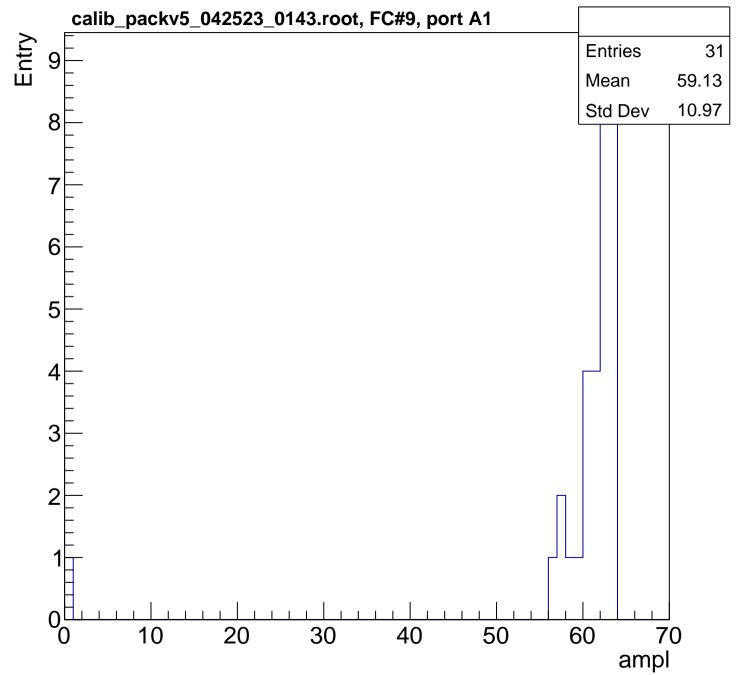


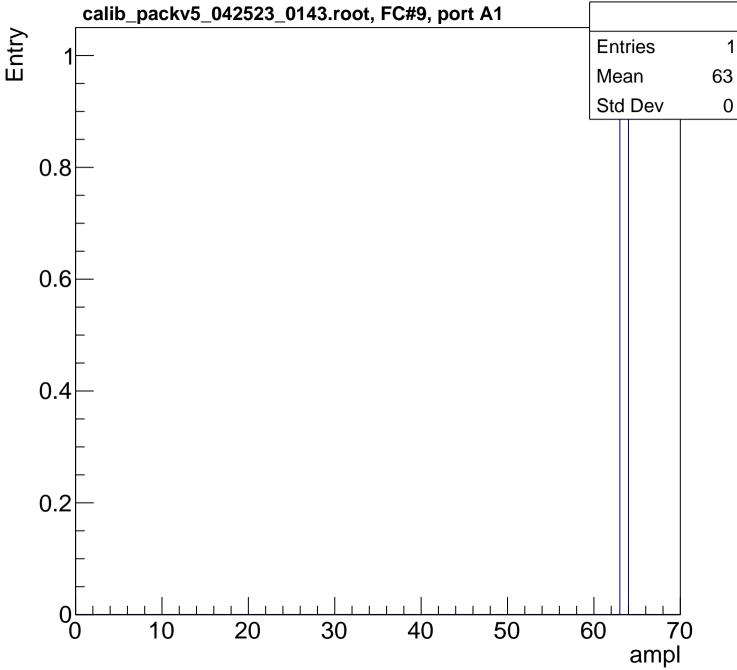


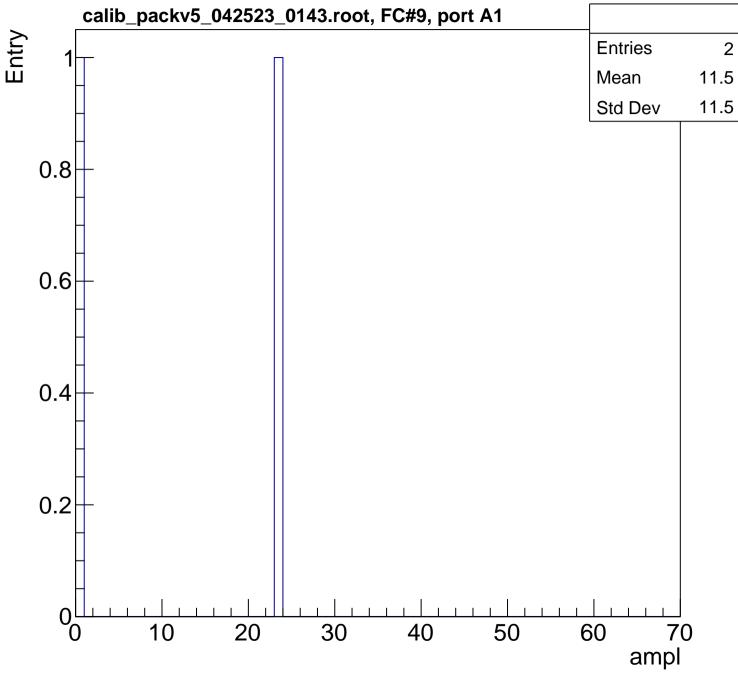


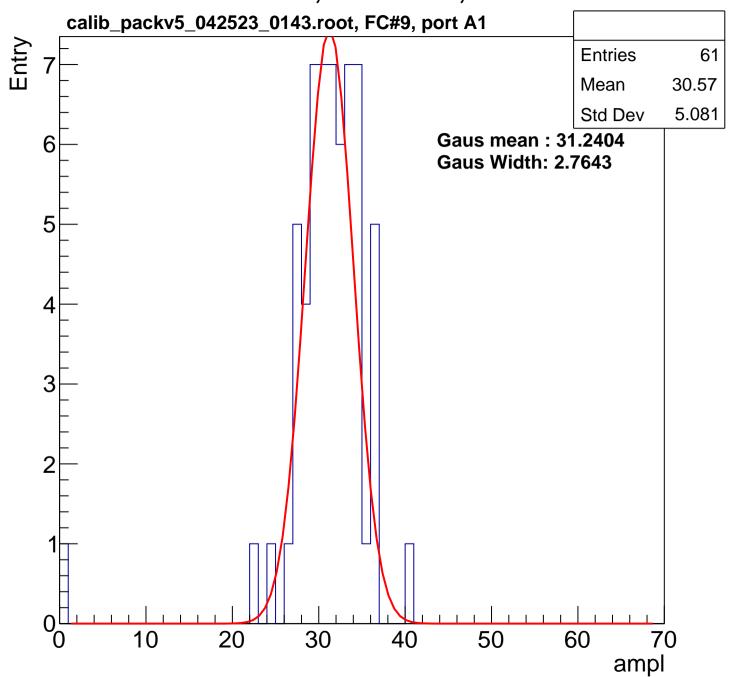


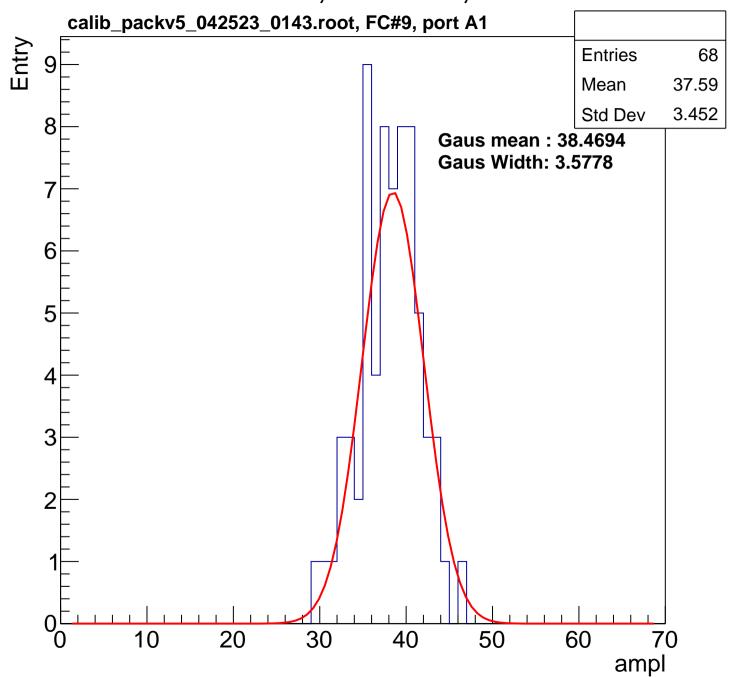


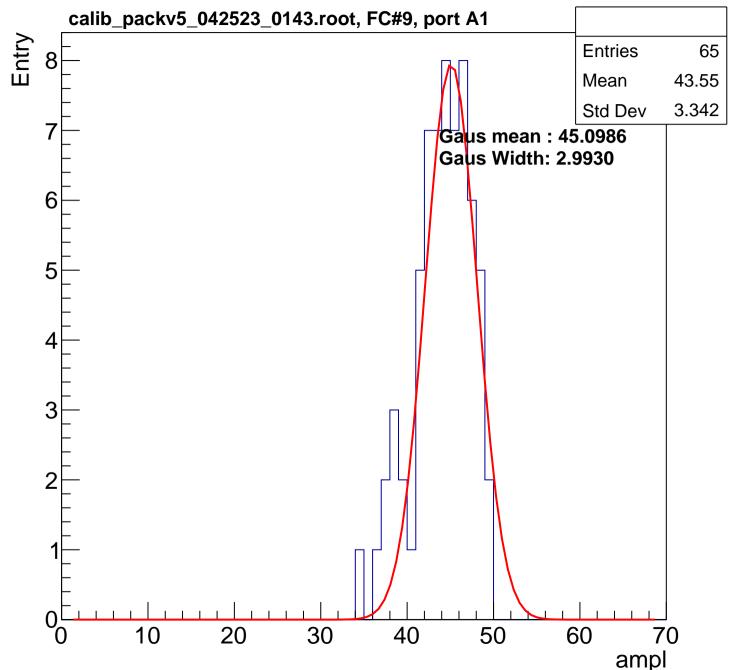


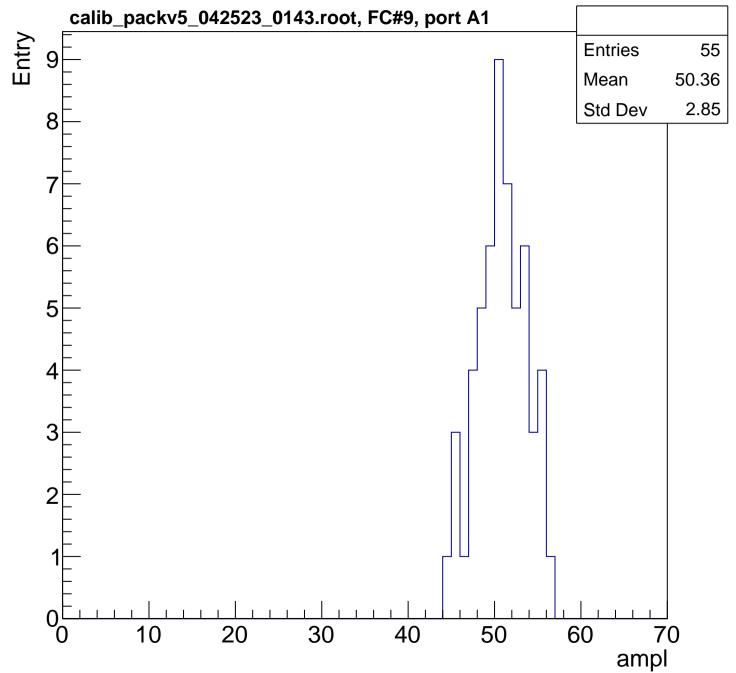


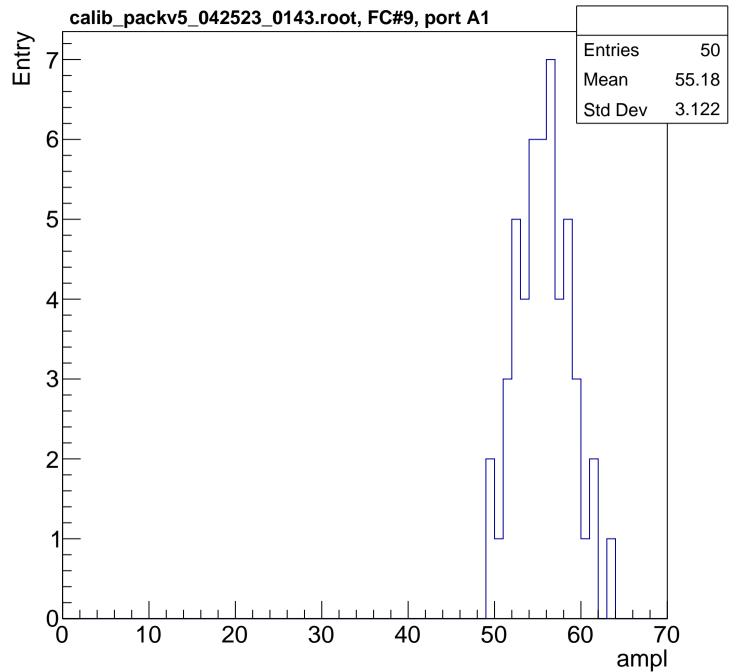


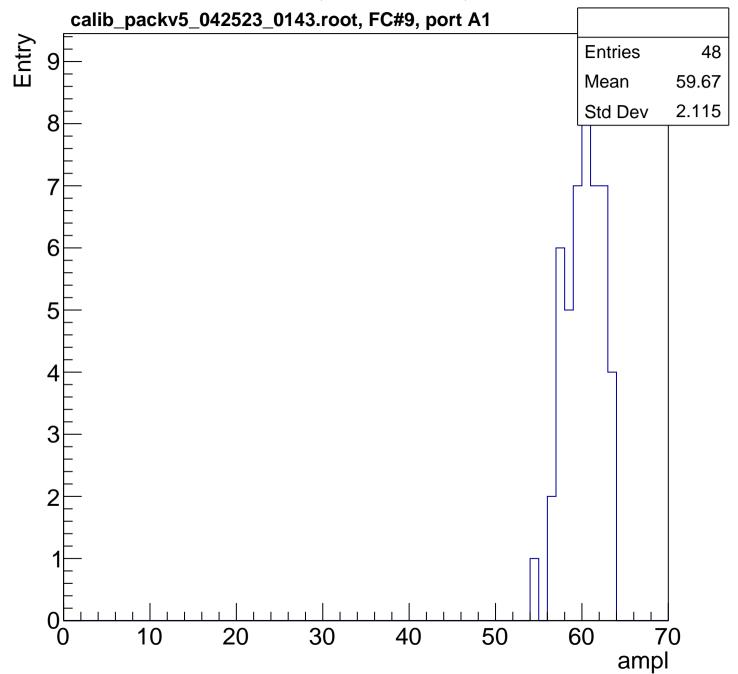


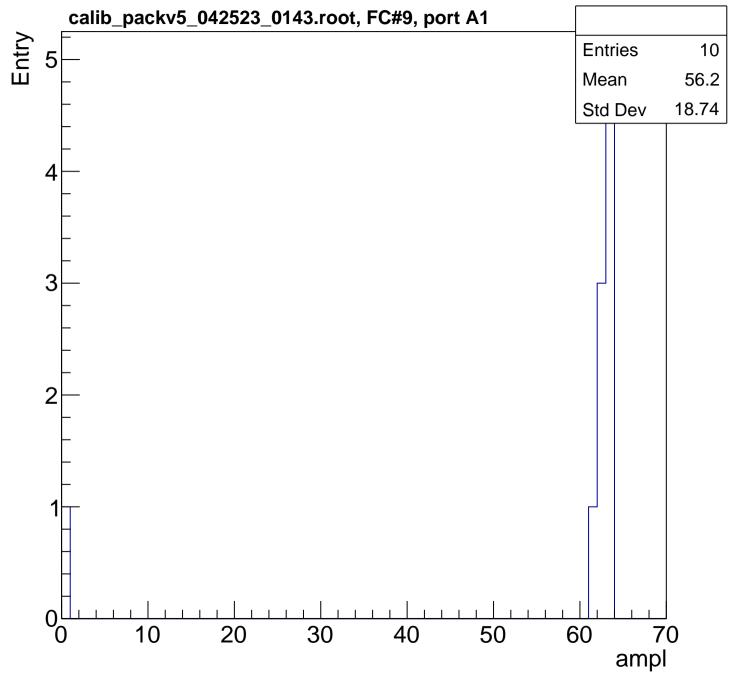












B0L001S, U3-ch18, adc7 calib_packv5_042523_0143.root, FC#9, port A1 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2

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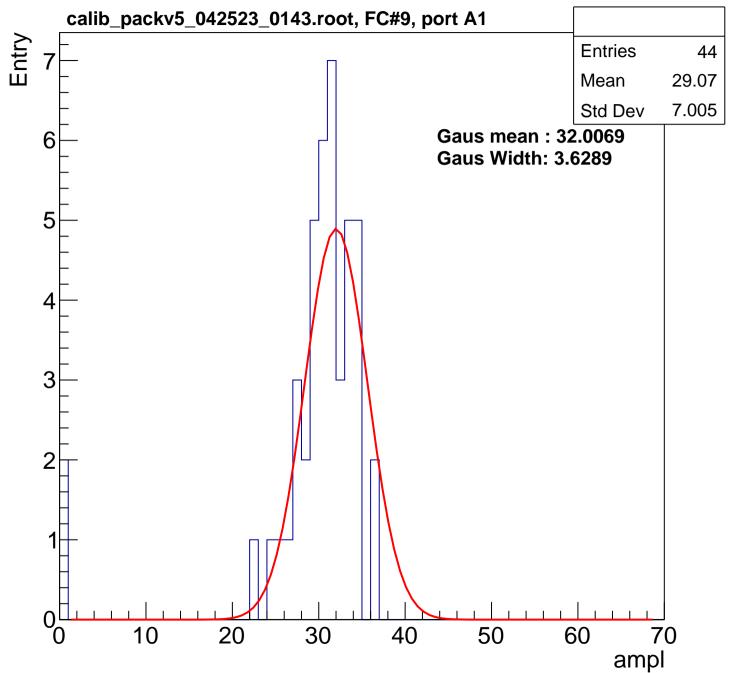
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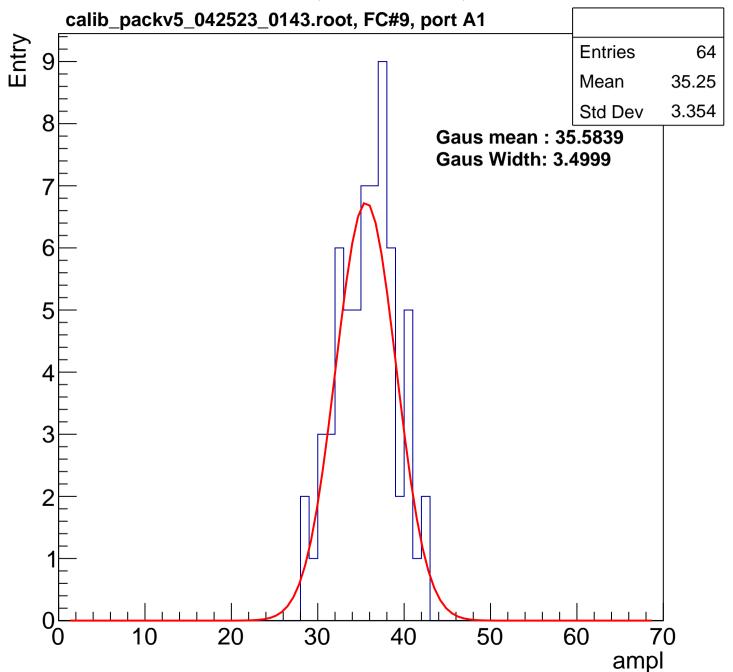
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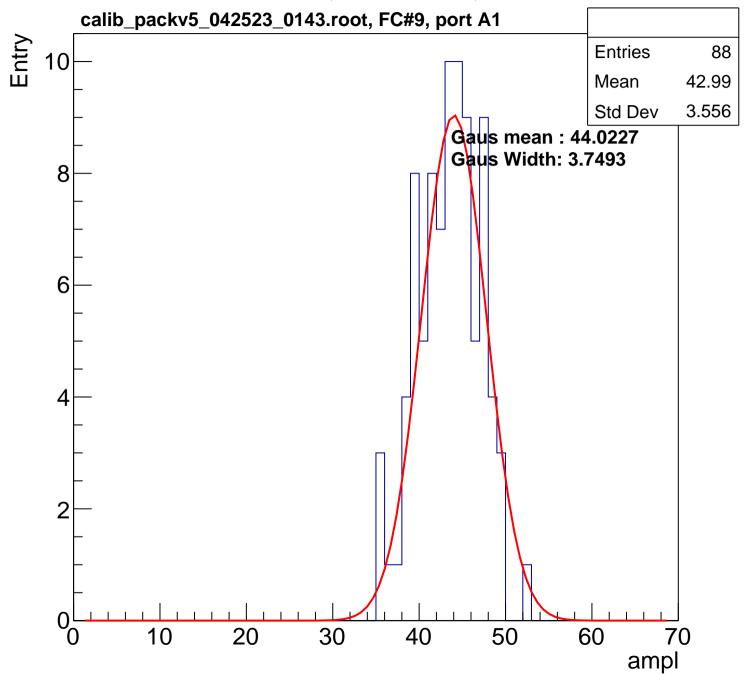
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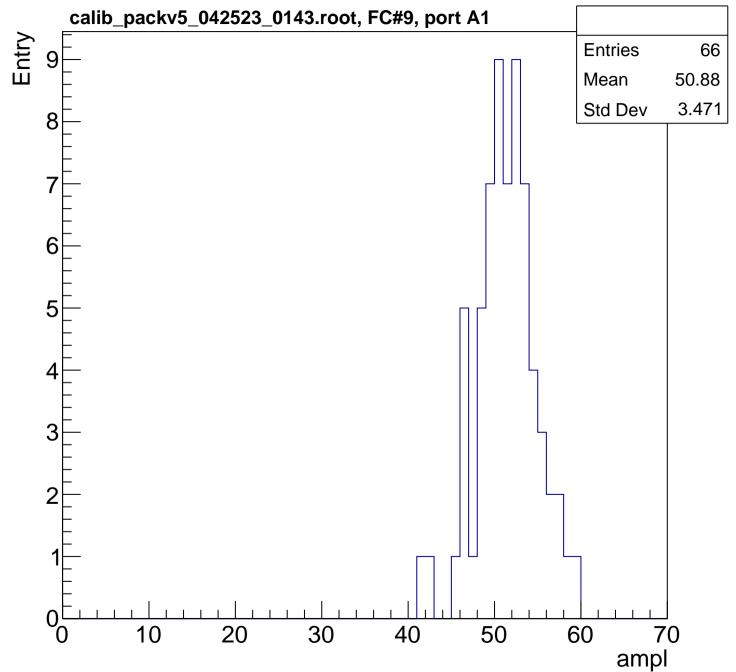
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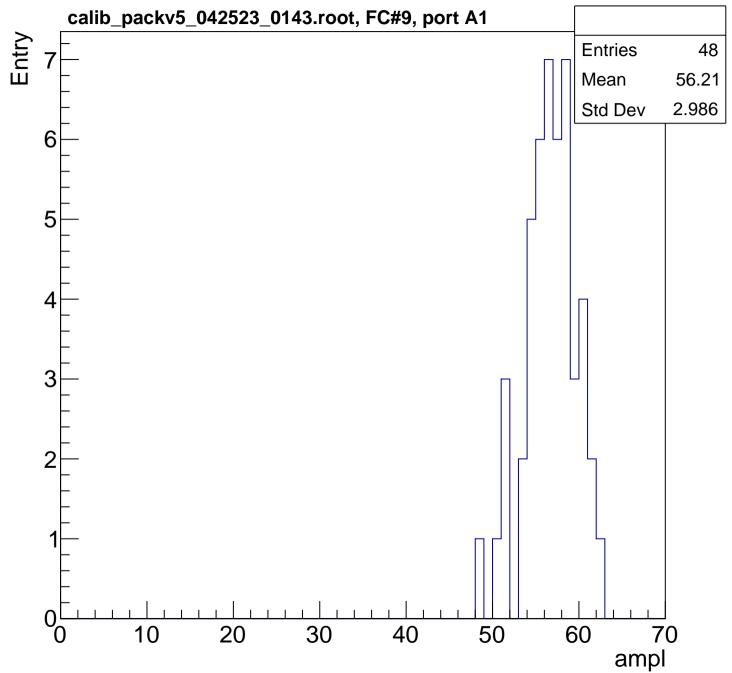
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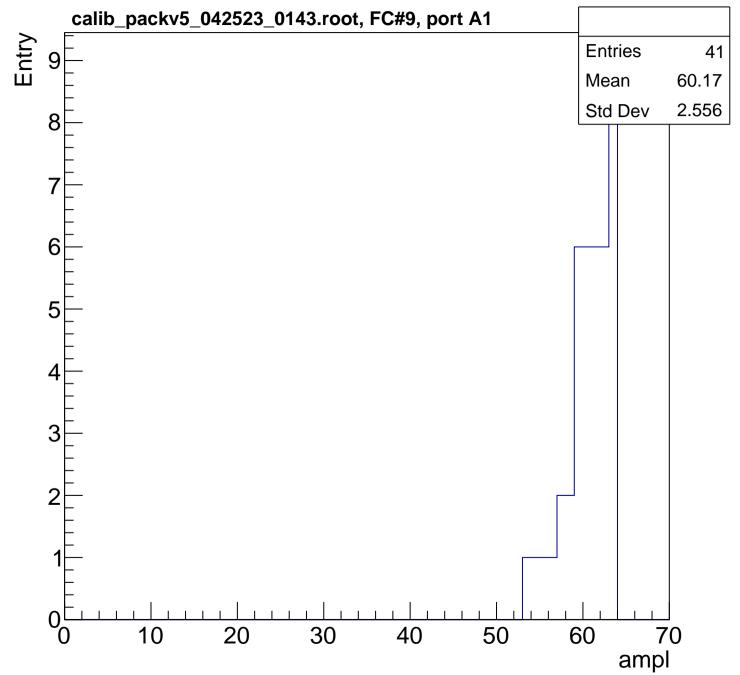


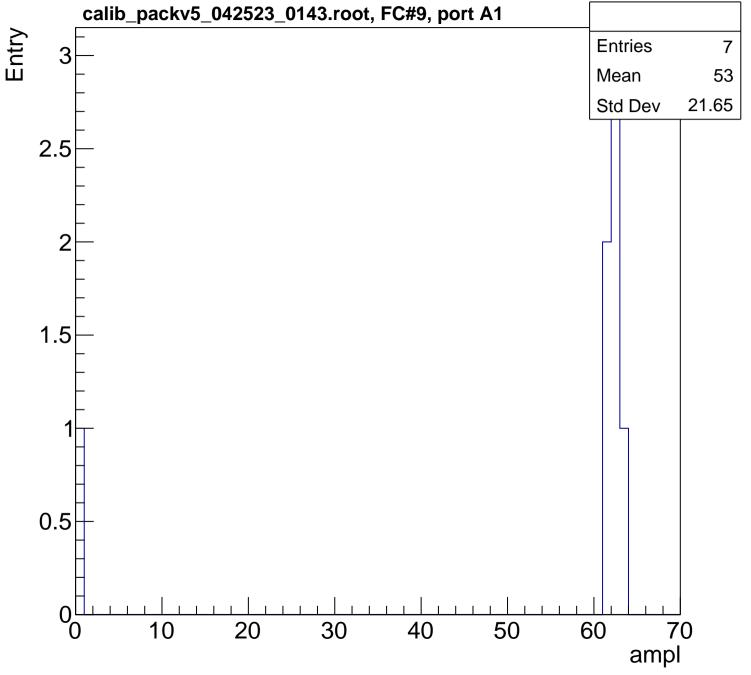




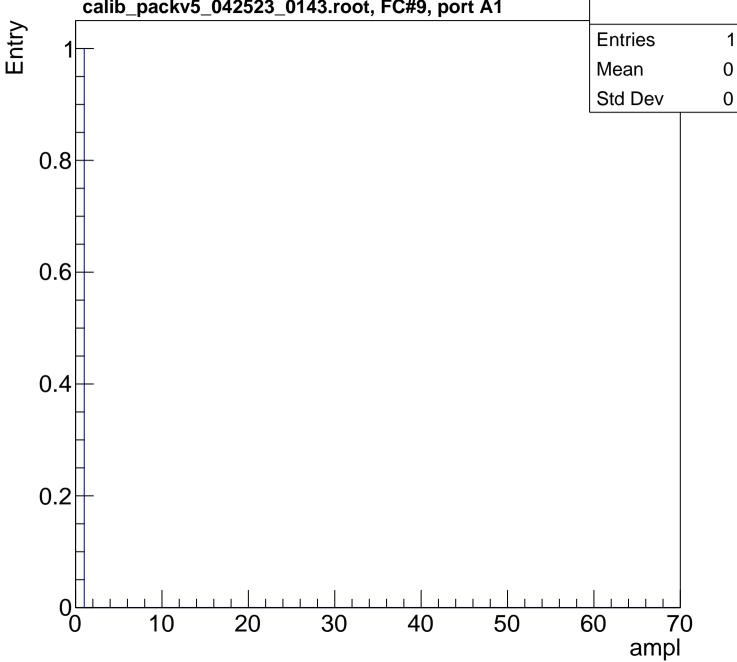


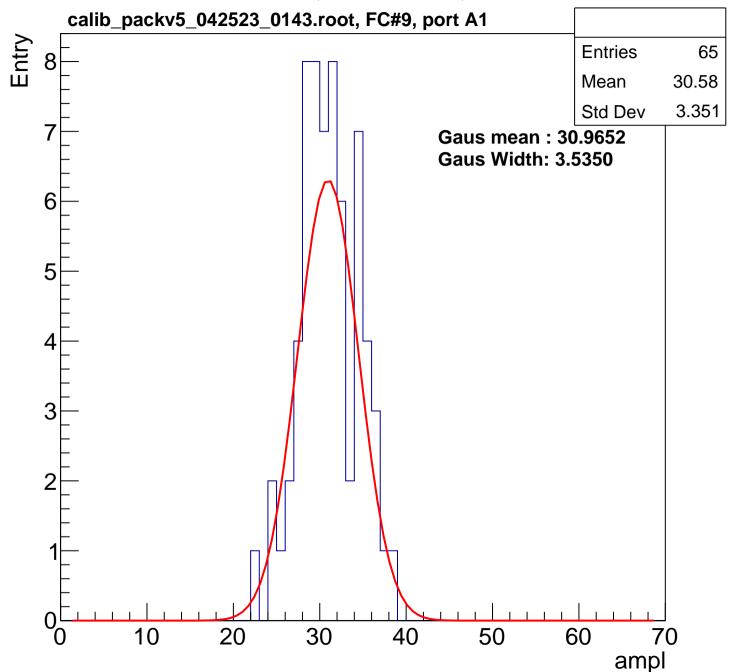


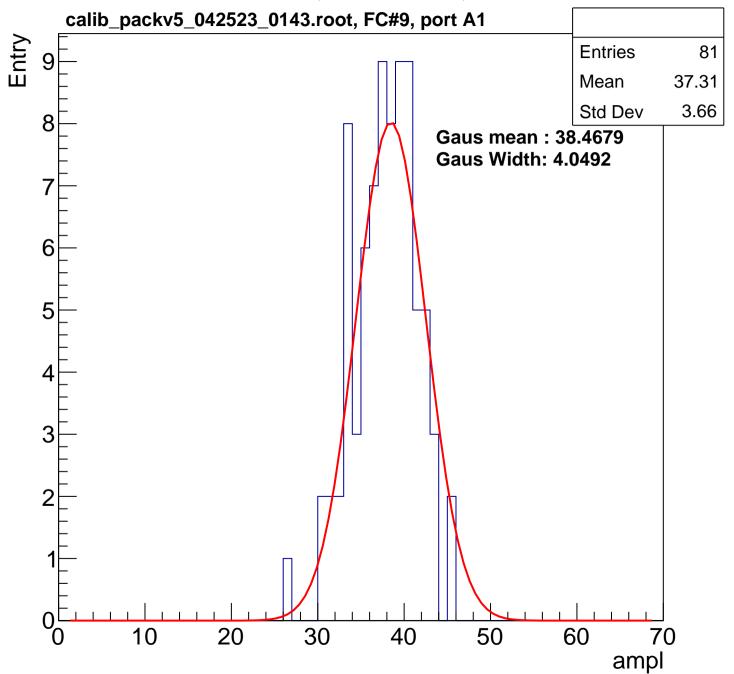


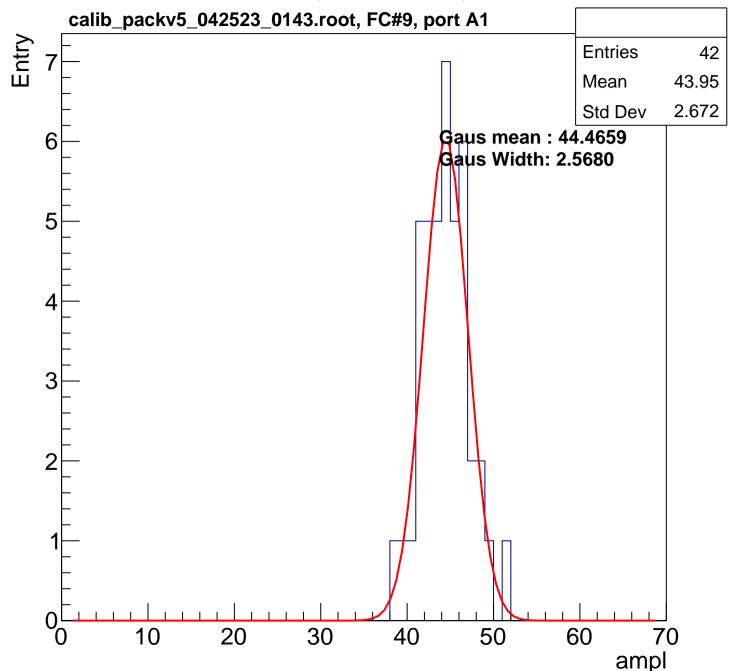


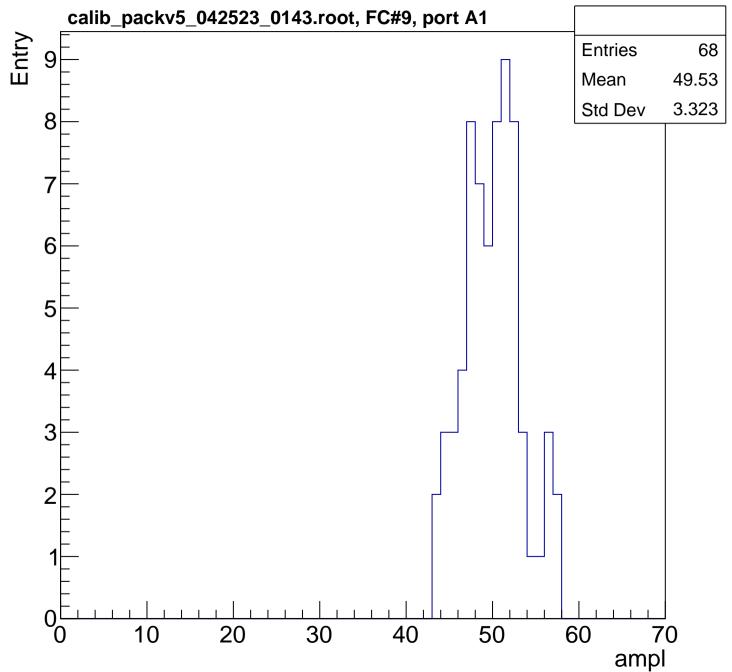
B0L001S, U3-ch19, adc7 calib_packv5_042523_0143.root, FC#9, port A1

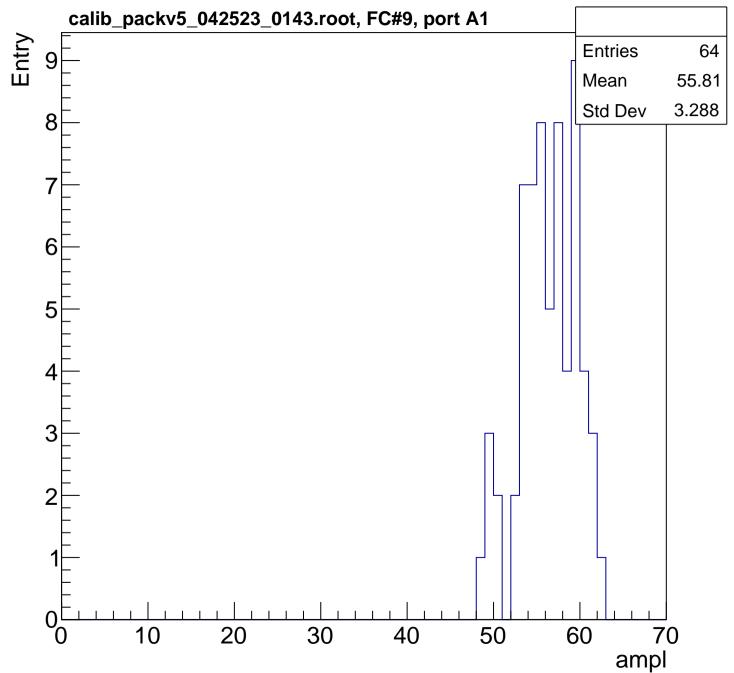


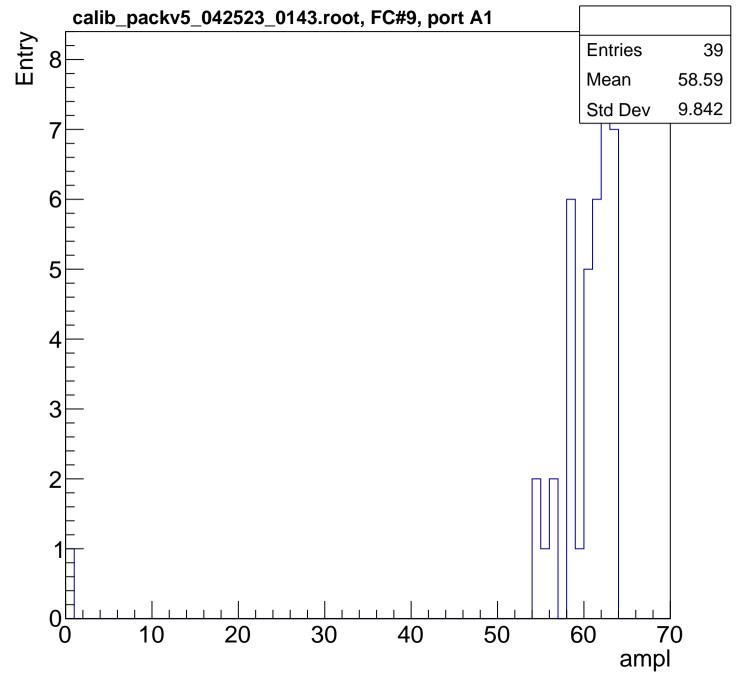


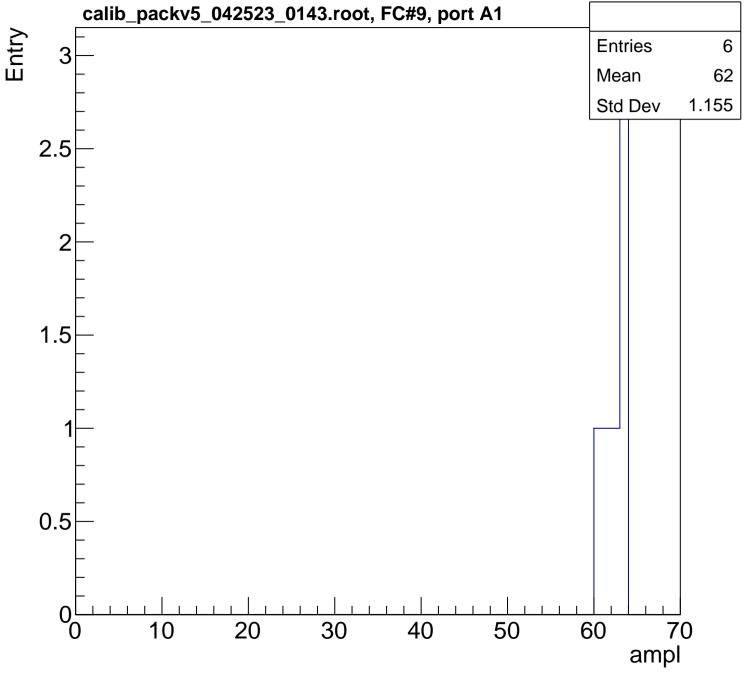




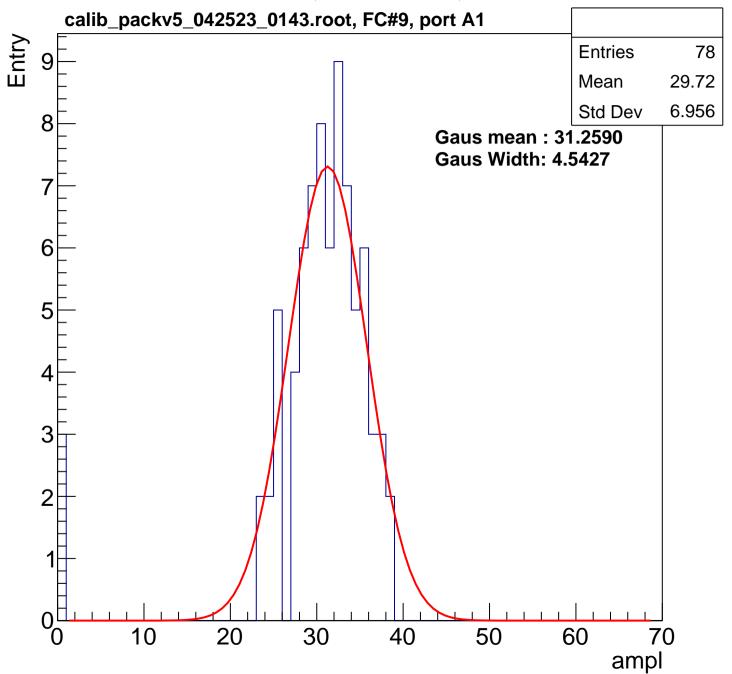


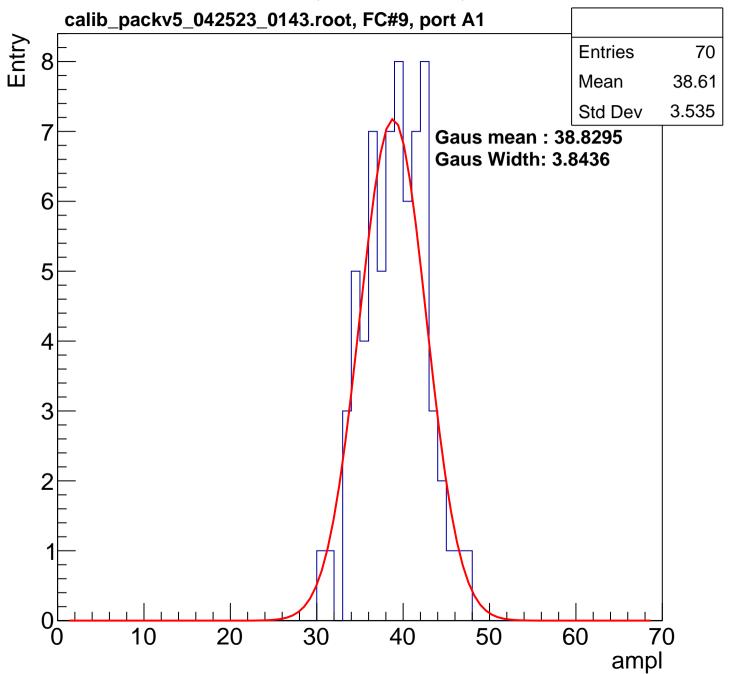


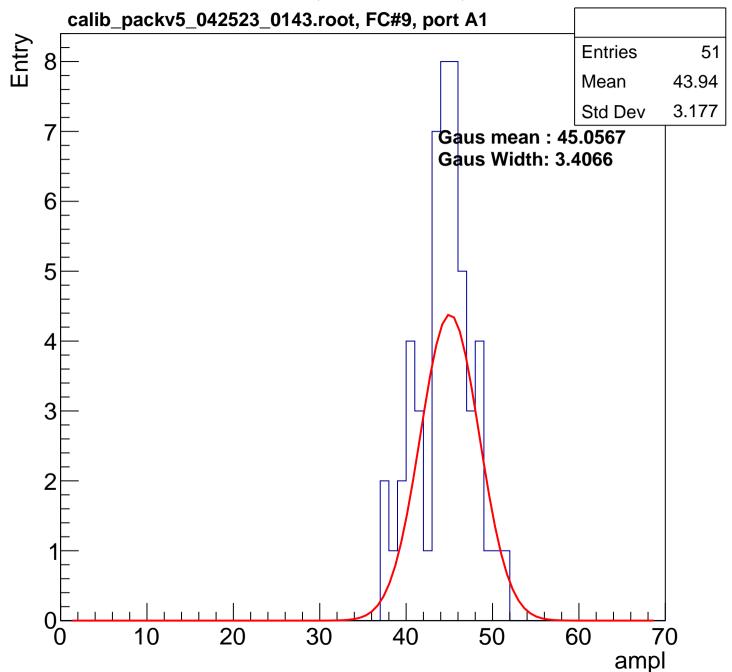


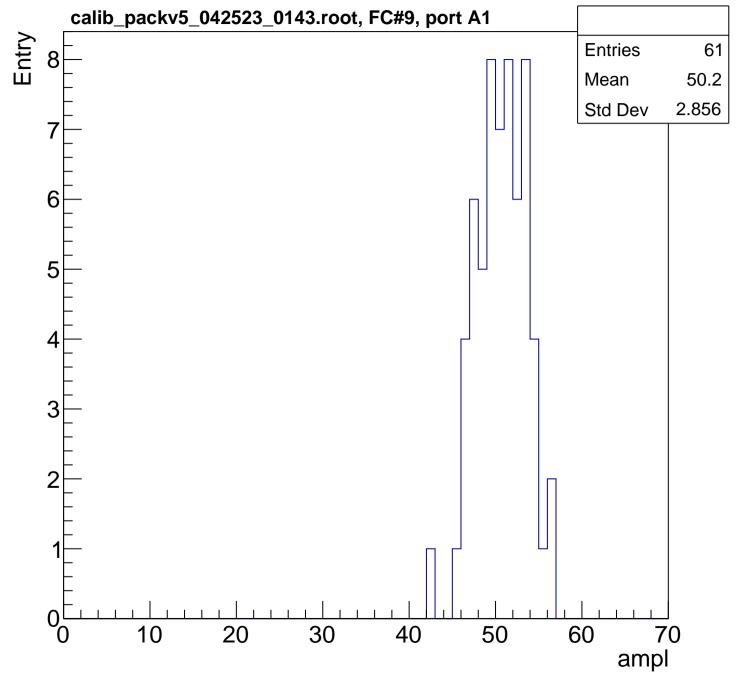


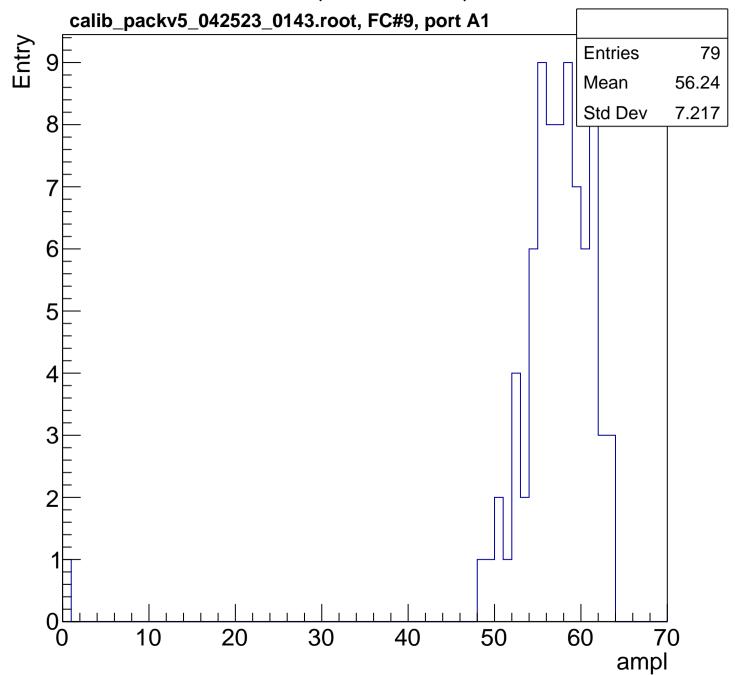


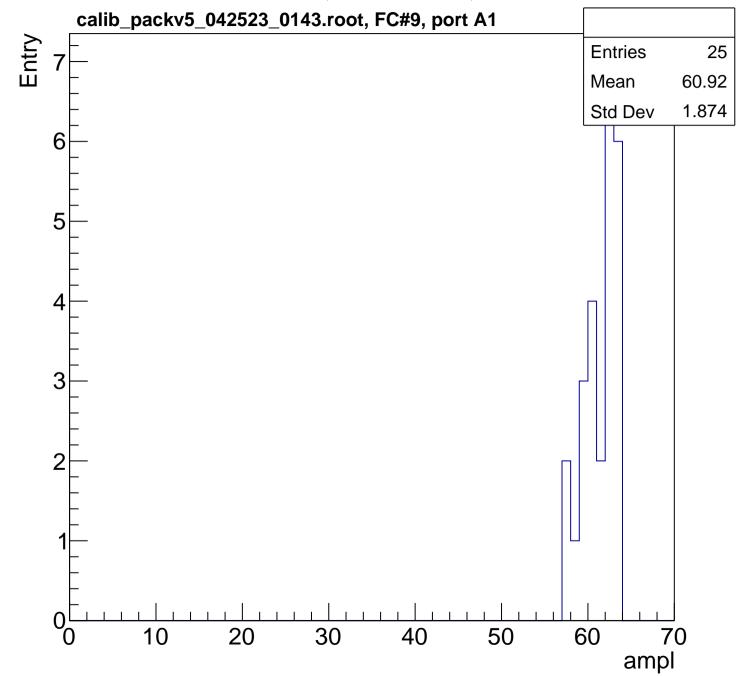






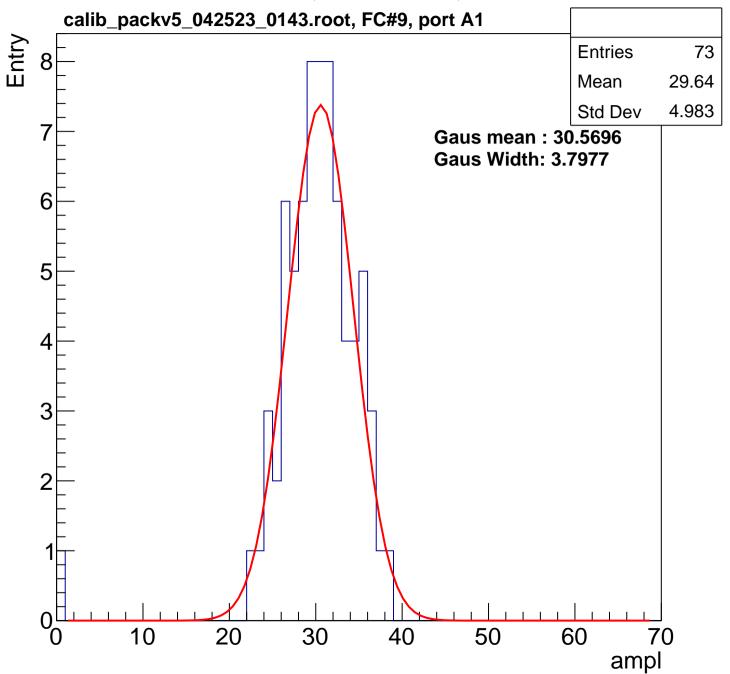


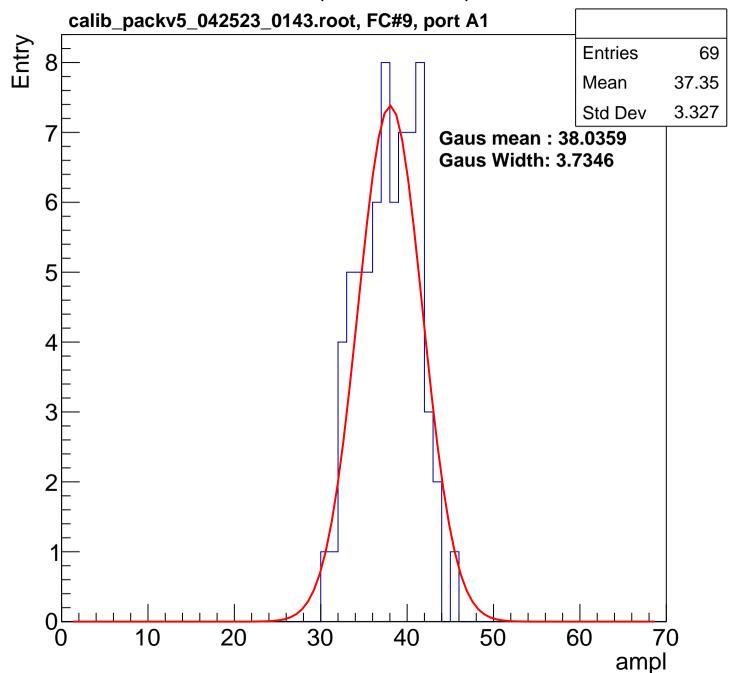


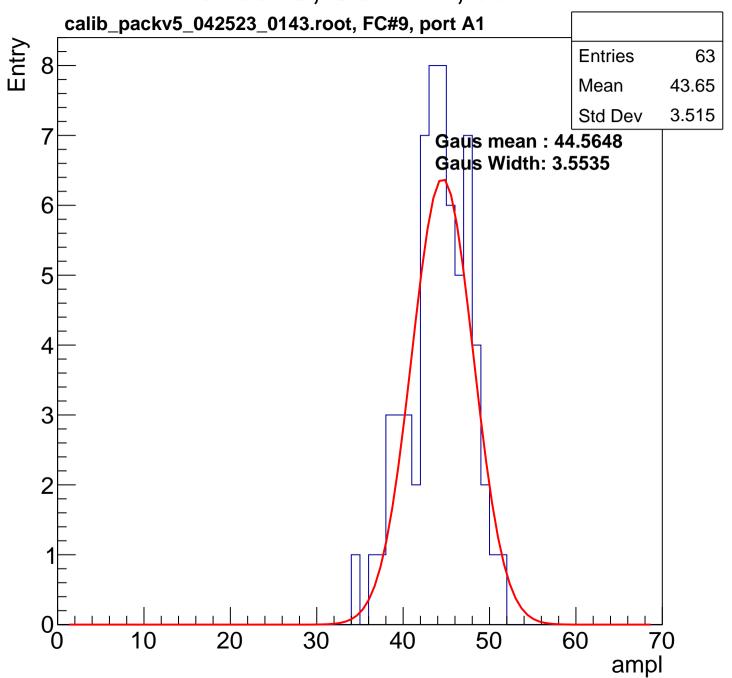


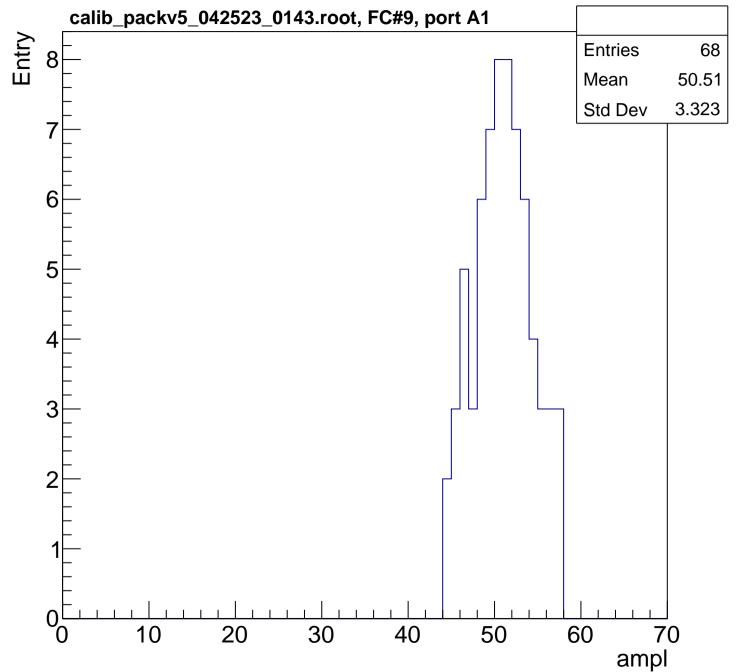


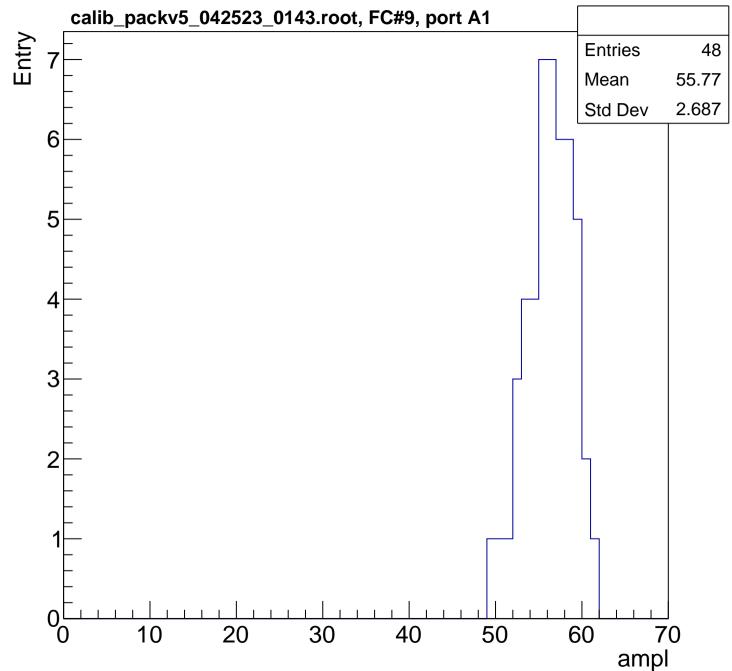


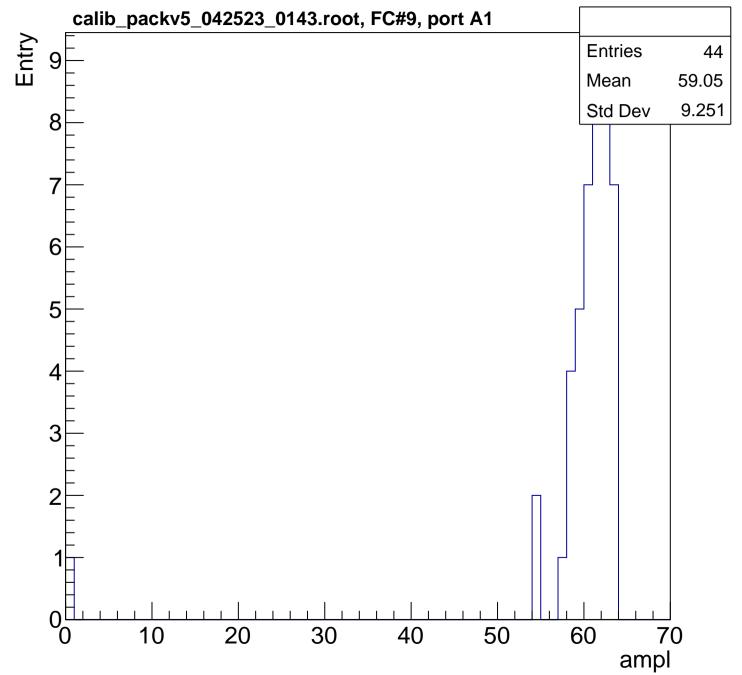


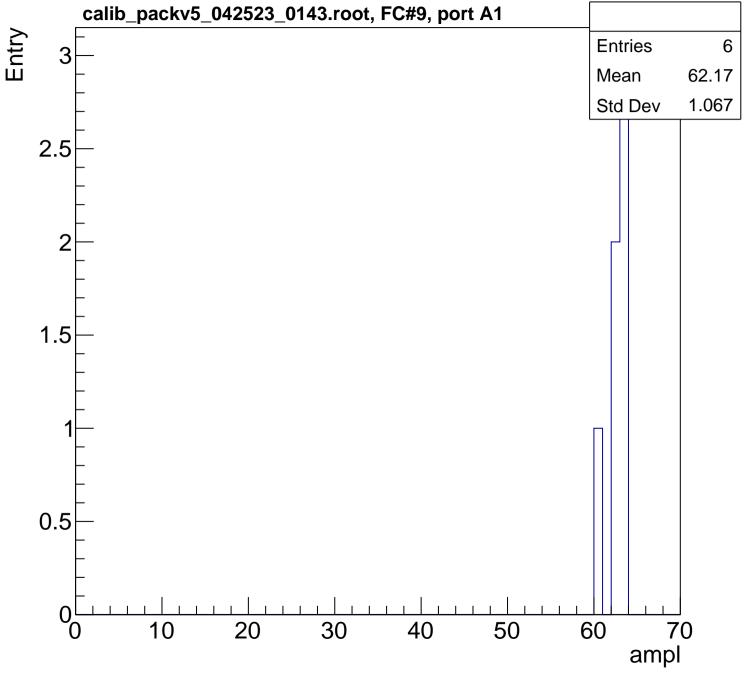






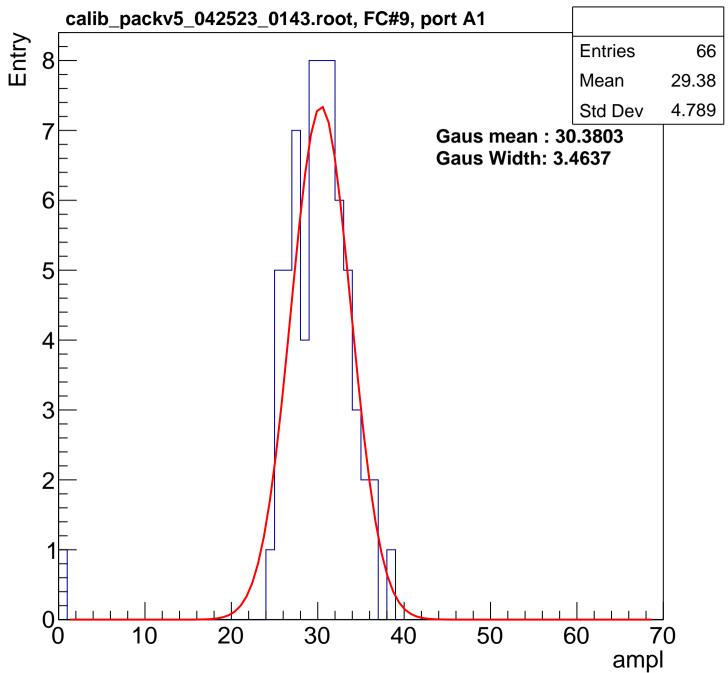


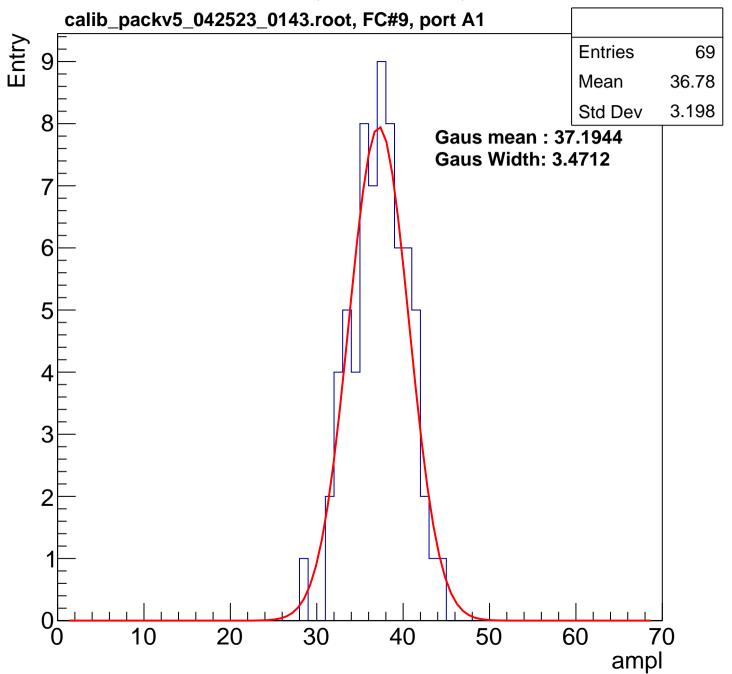


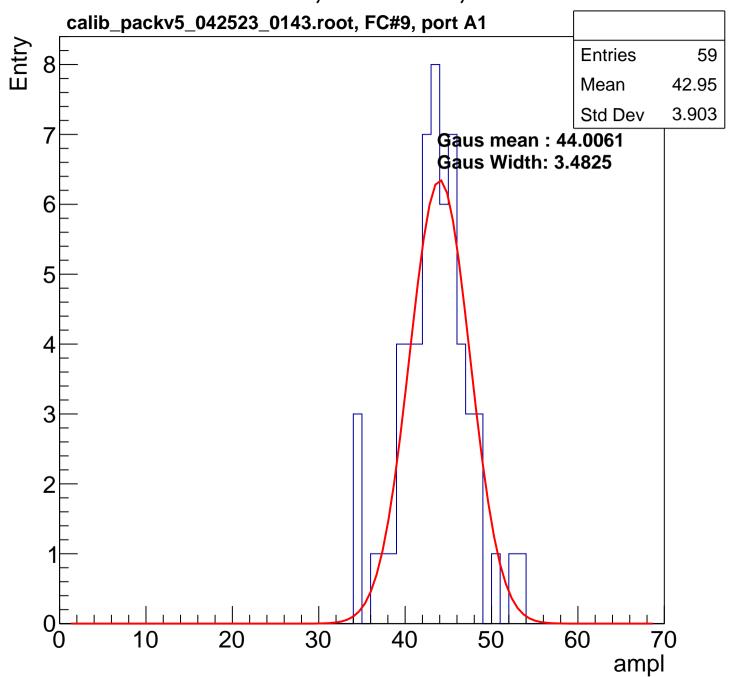


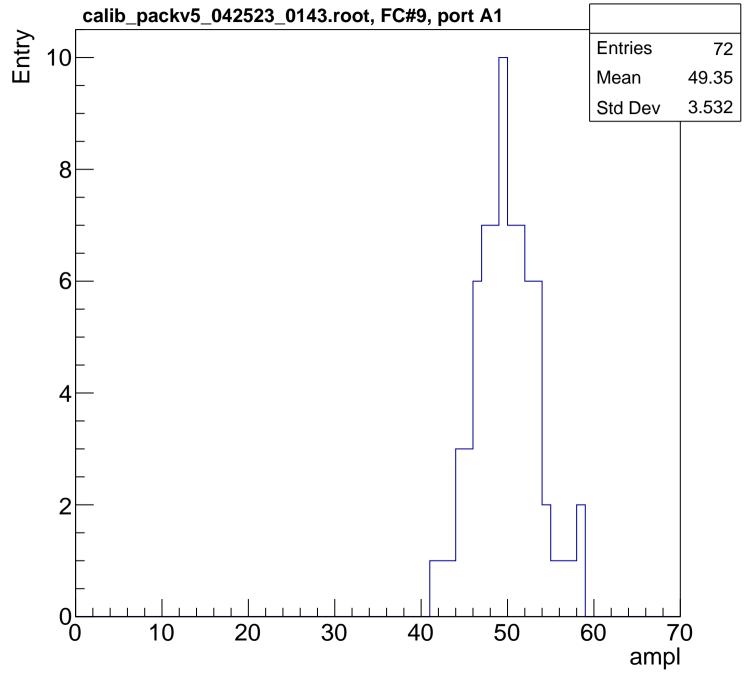
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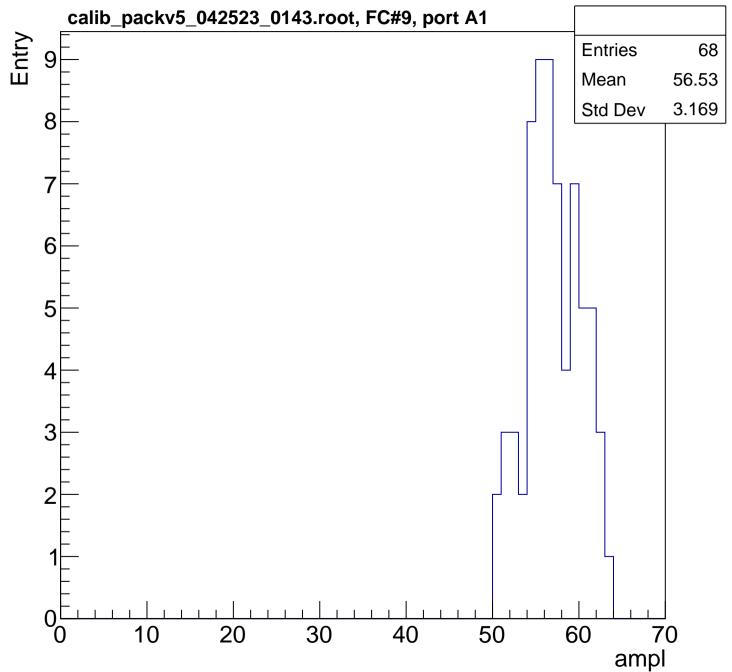


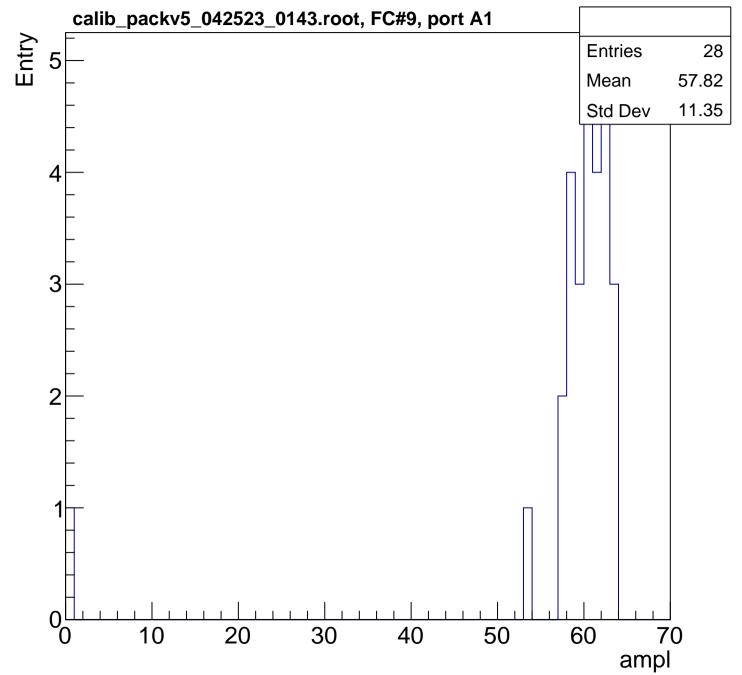


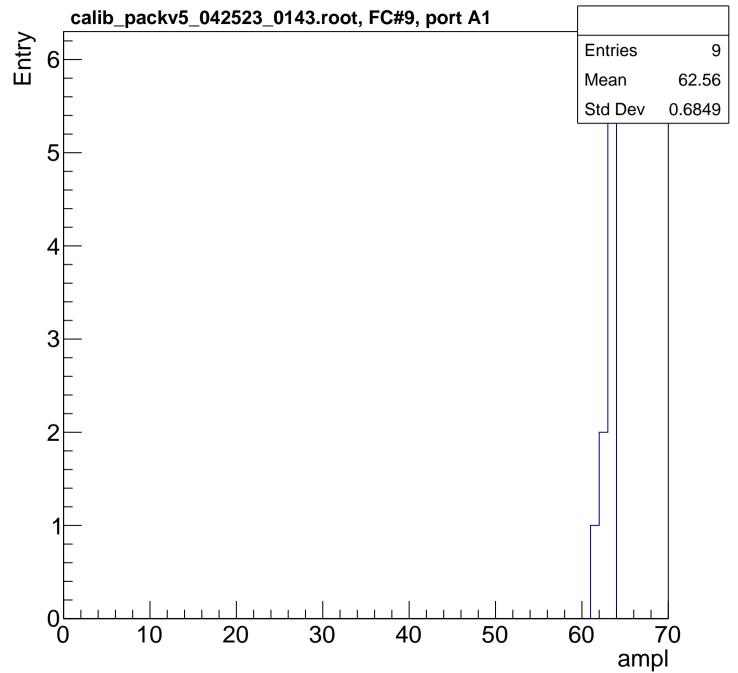


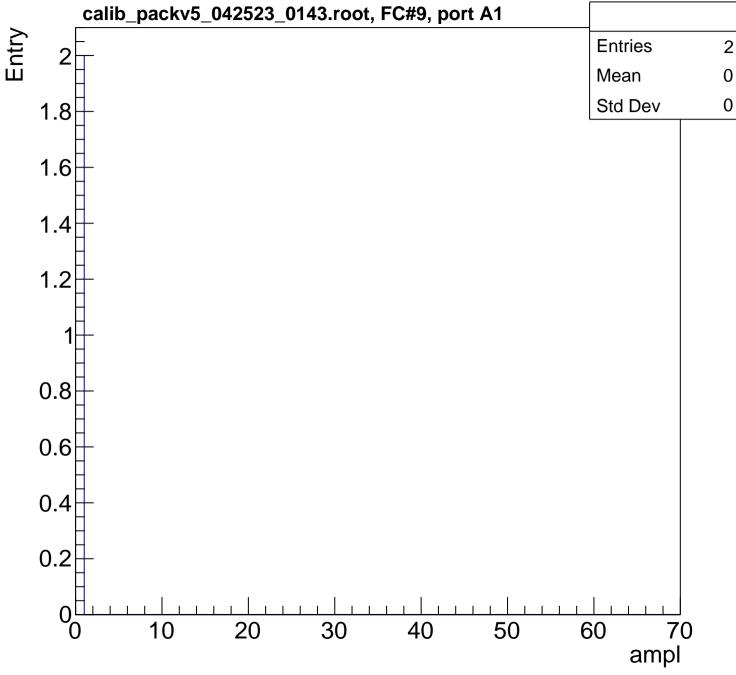


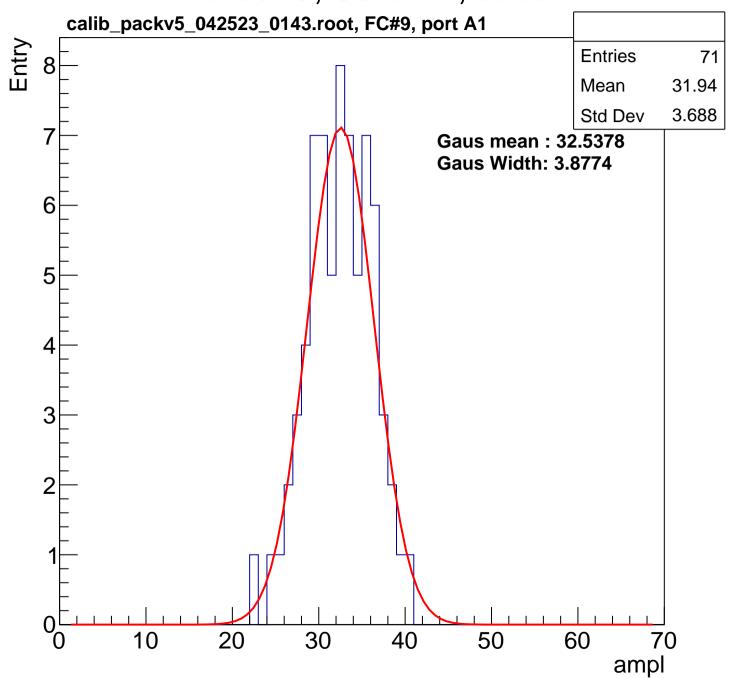


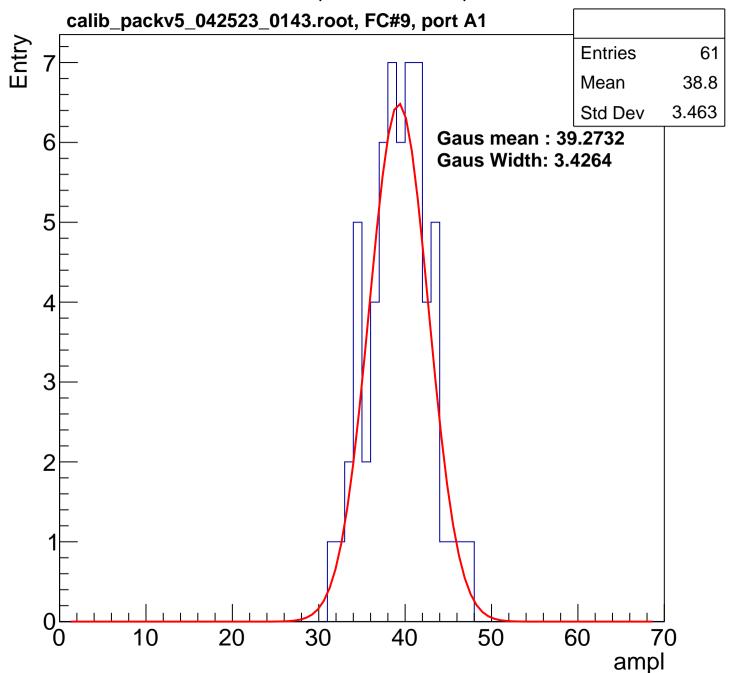


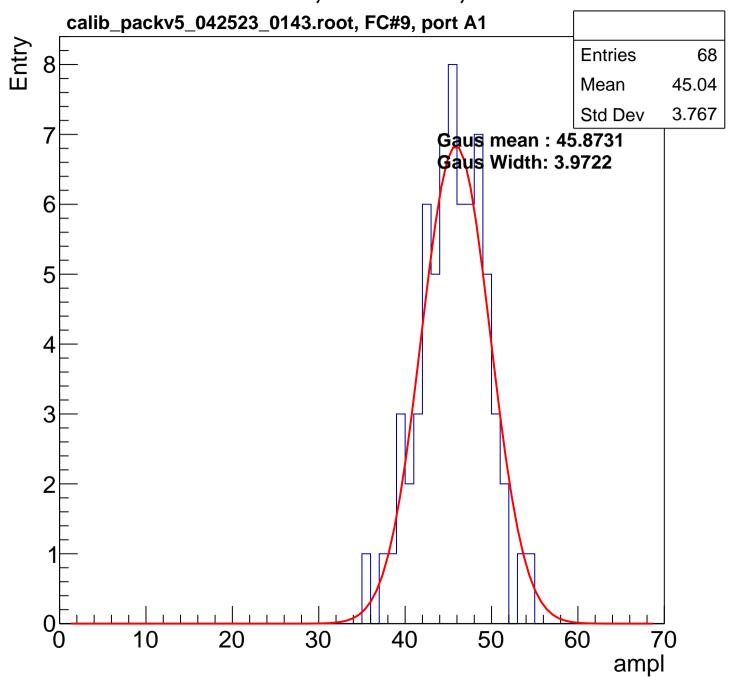


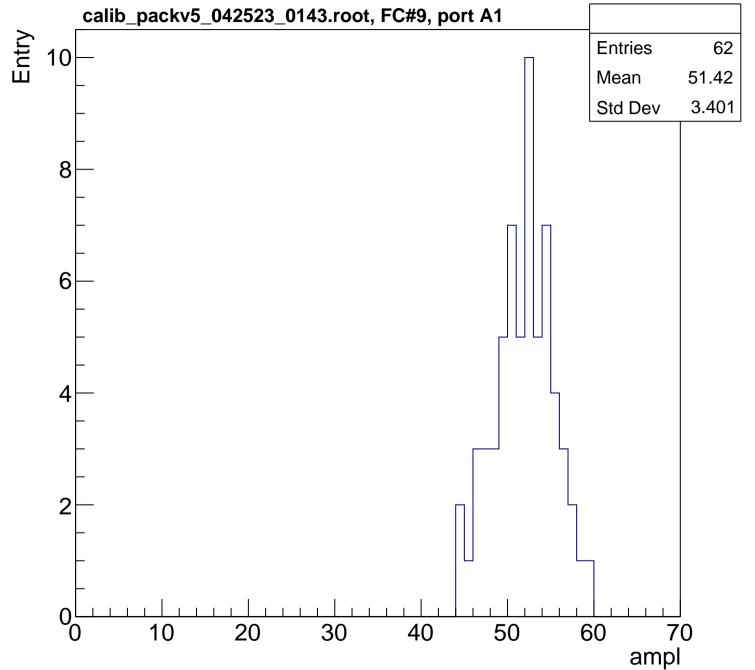


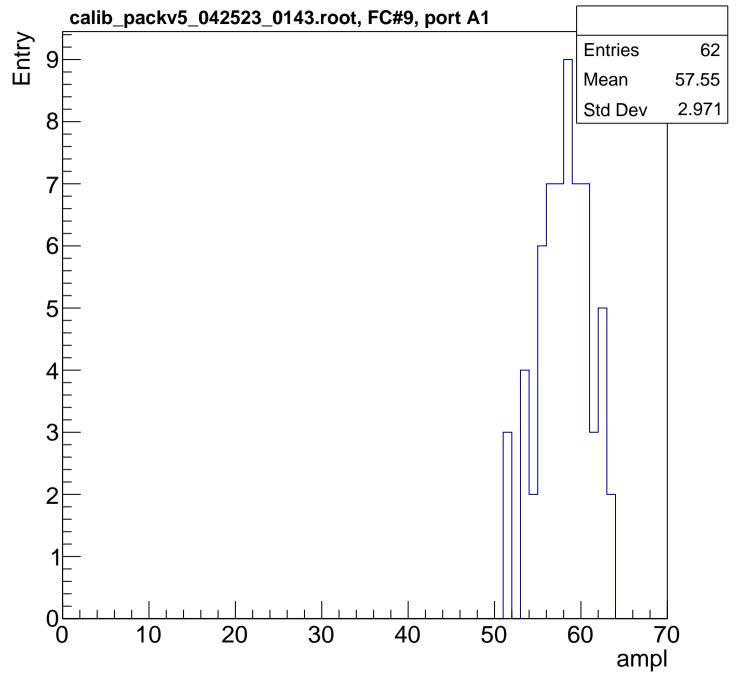


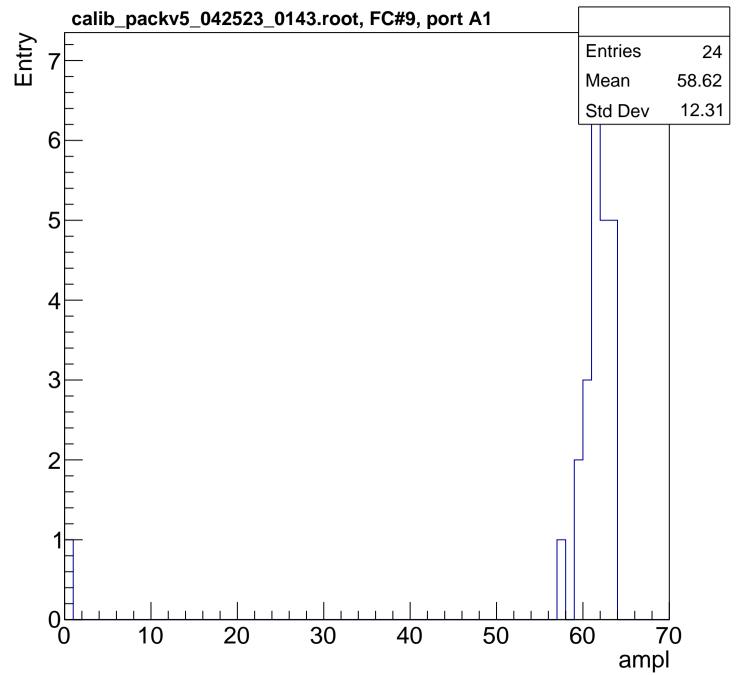


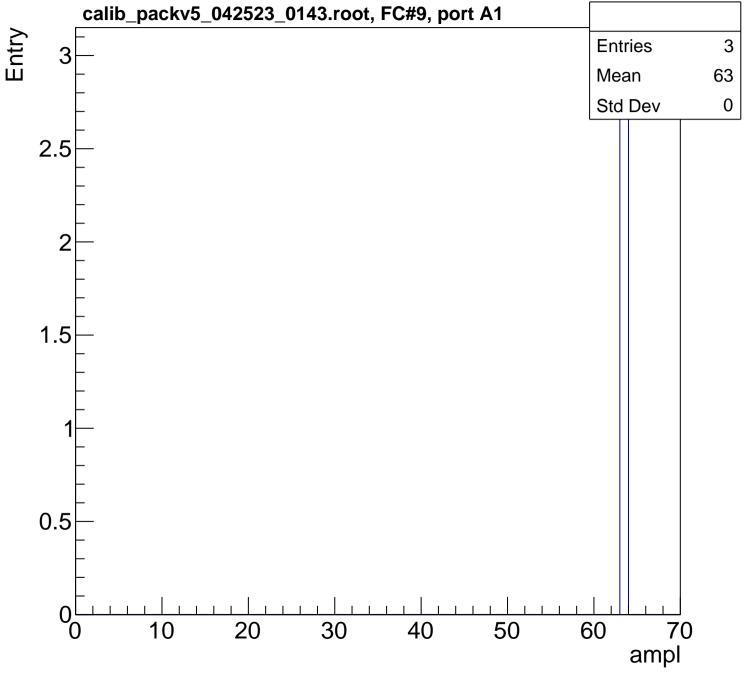


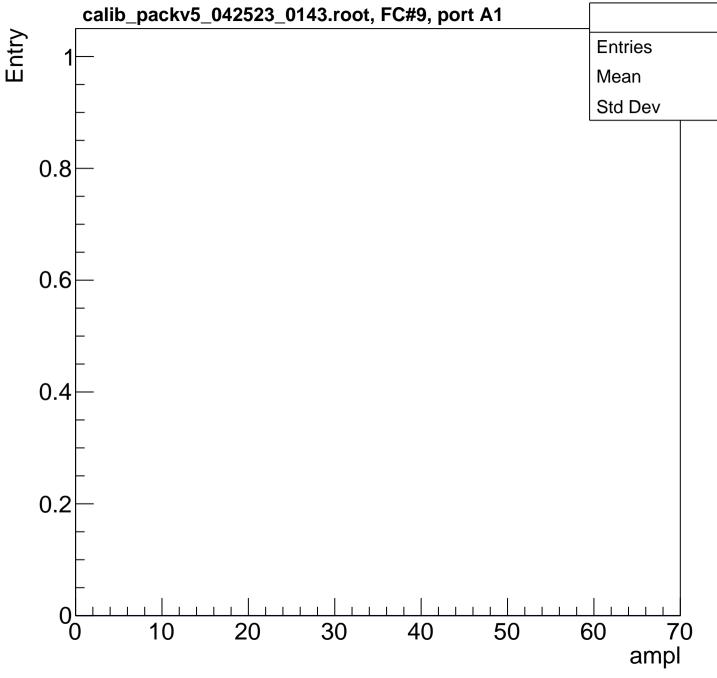


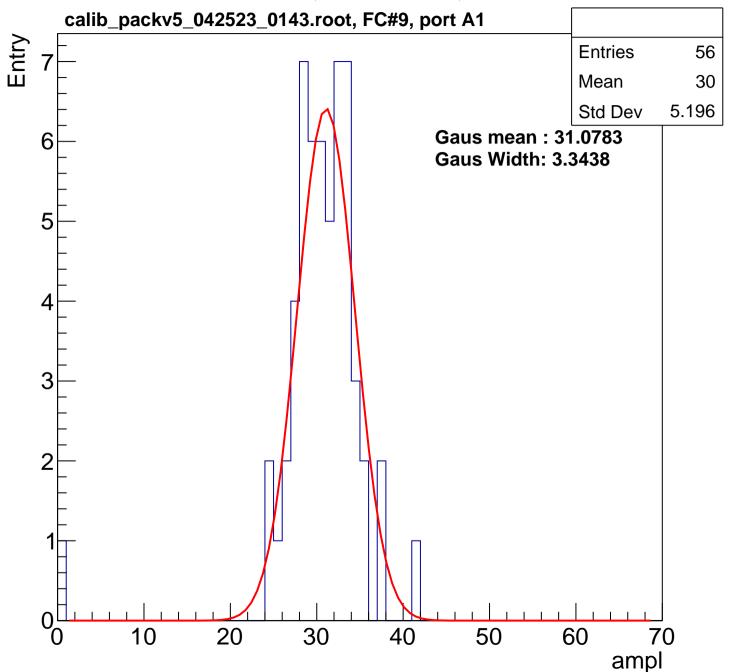


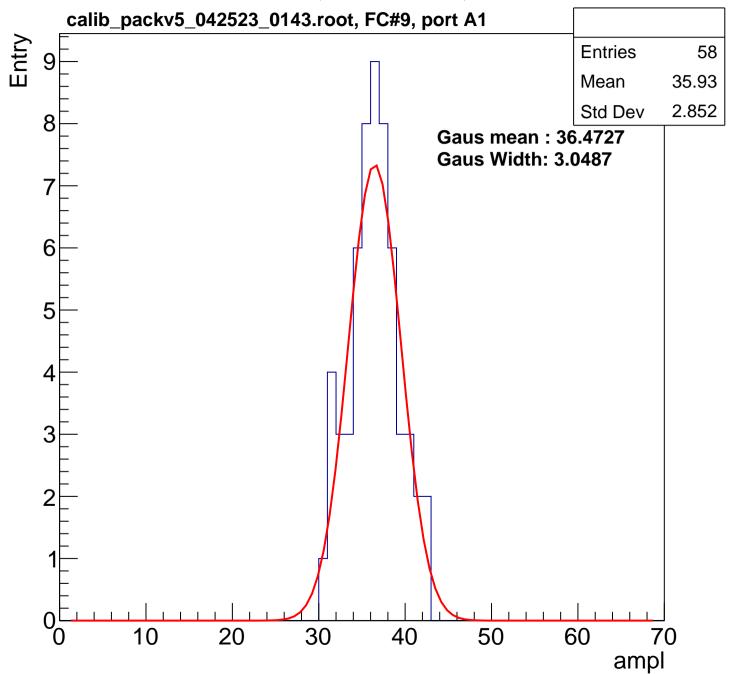


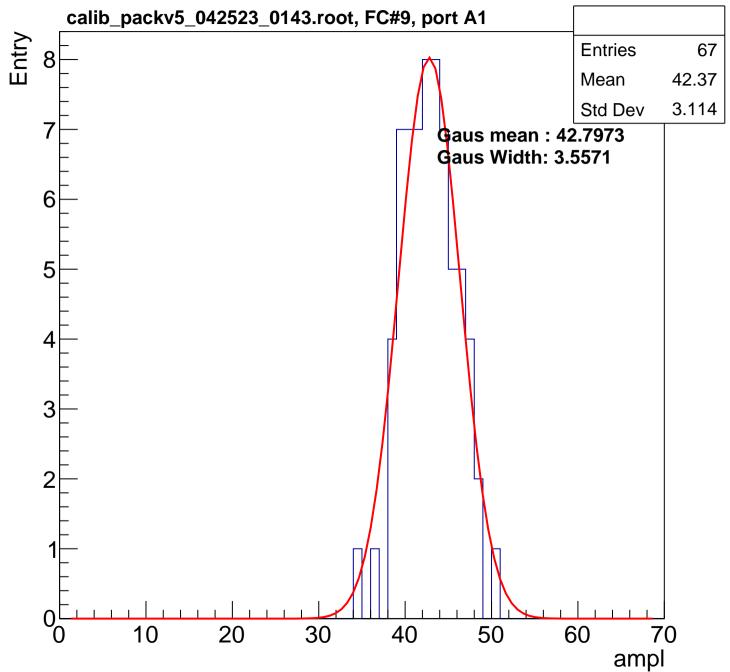


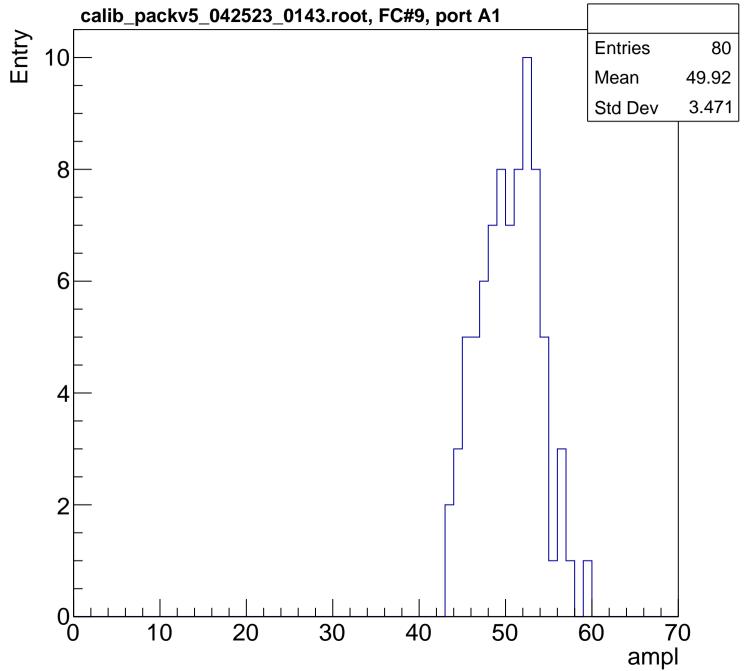


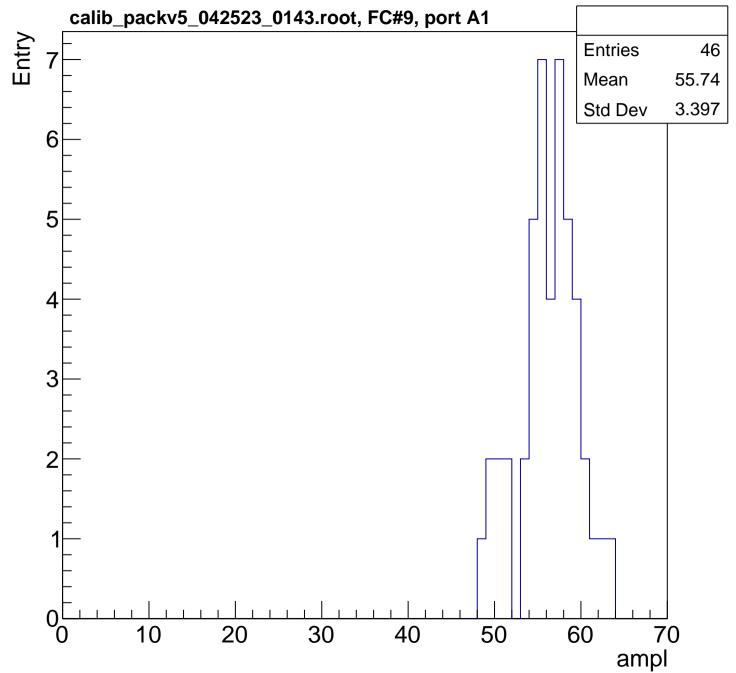


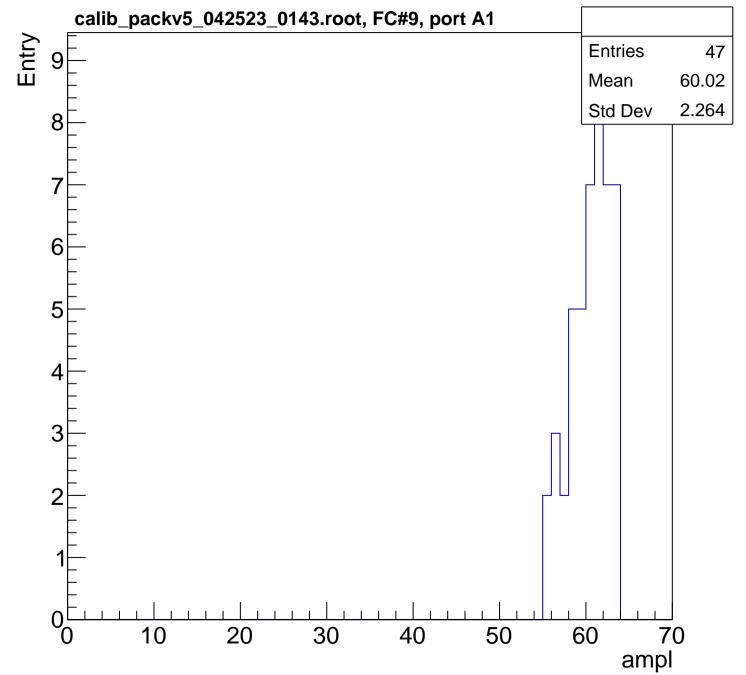


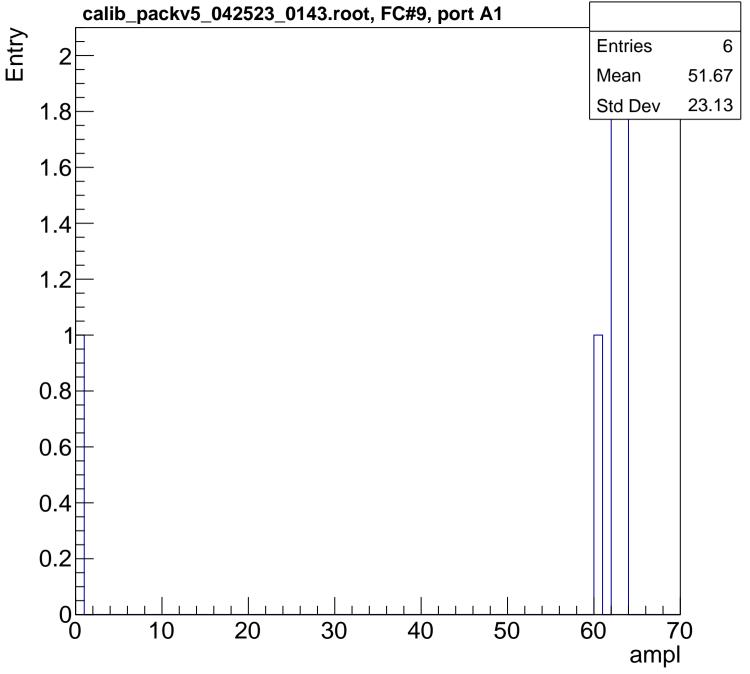


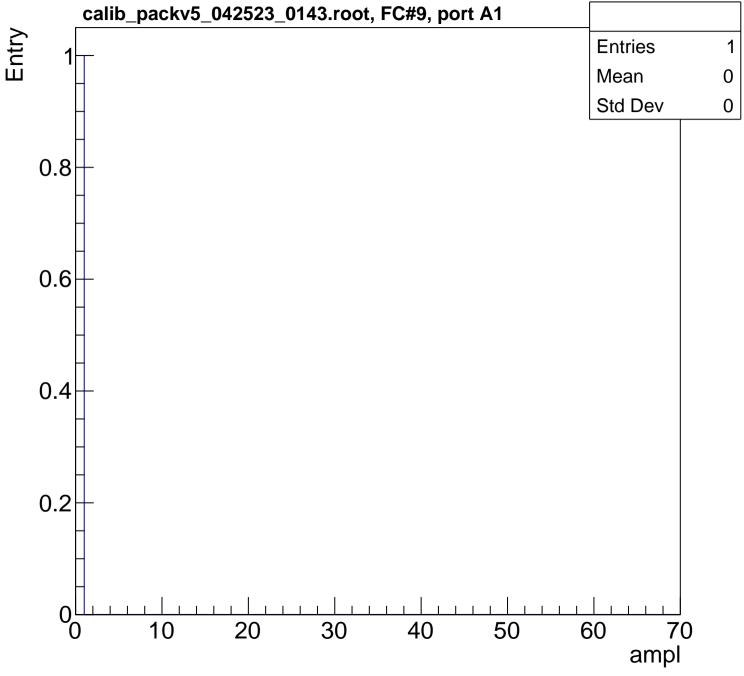


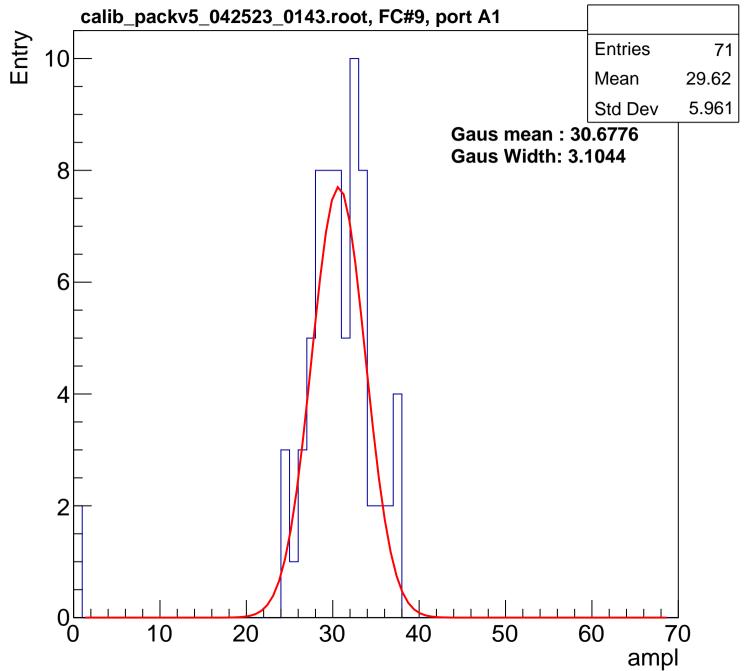


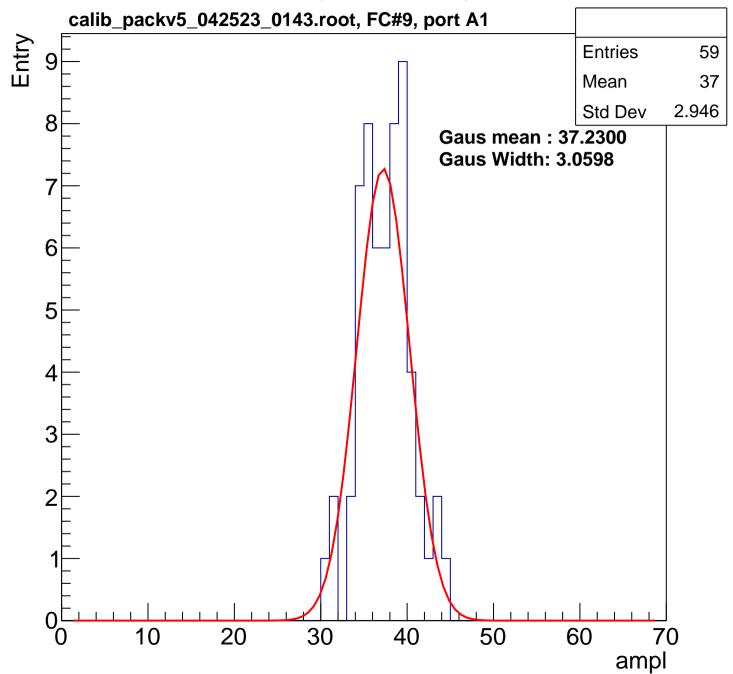


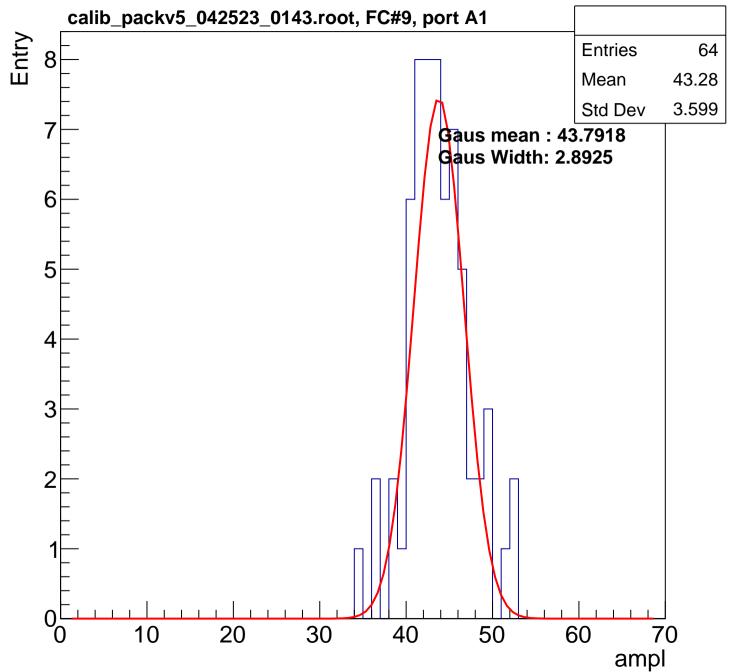


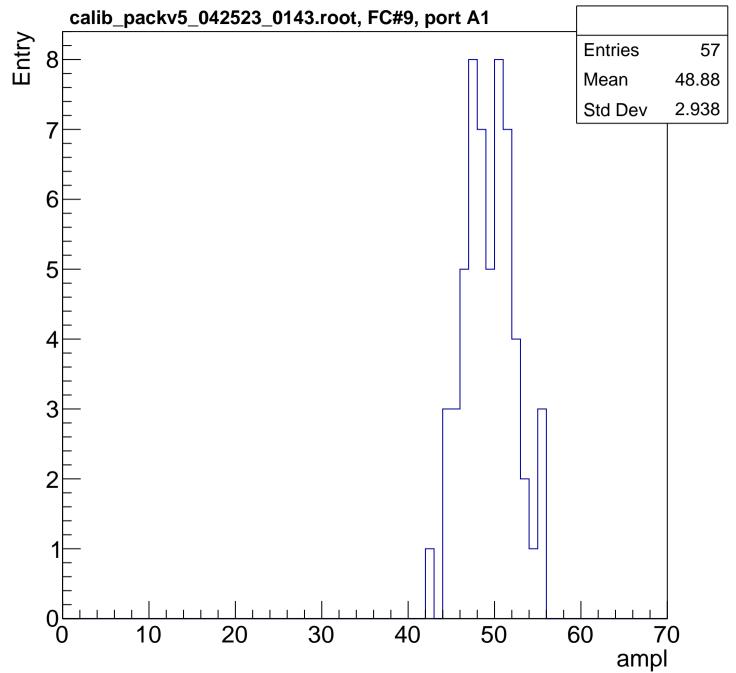


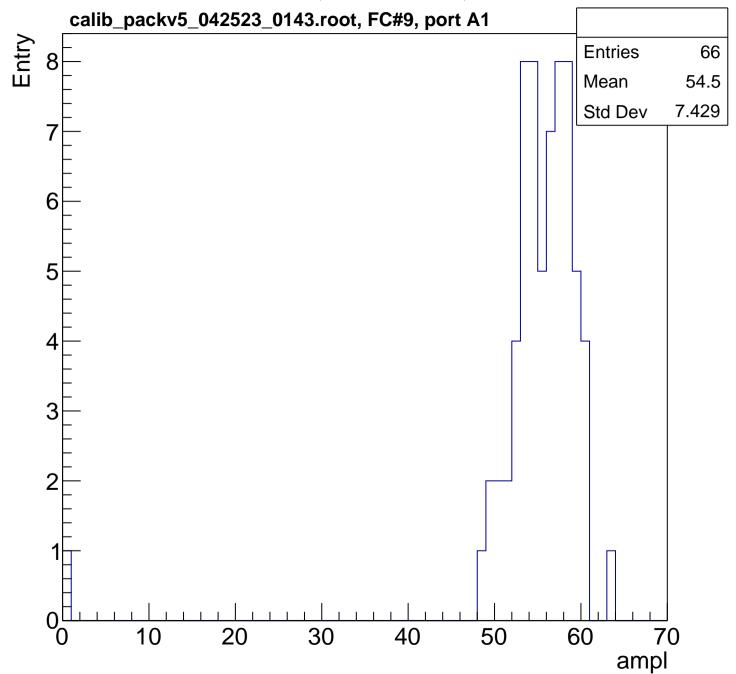


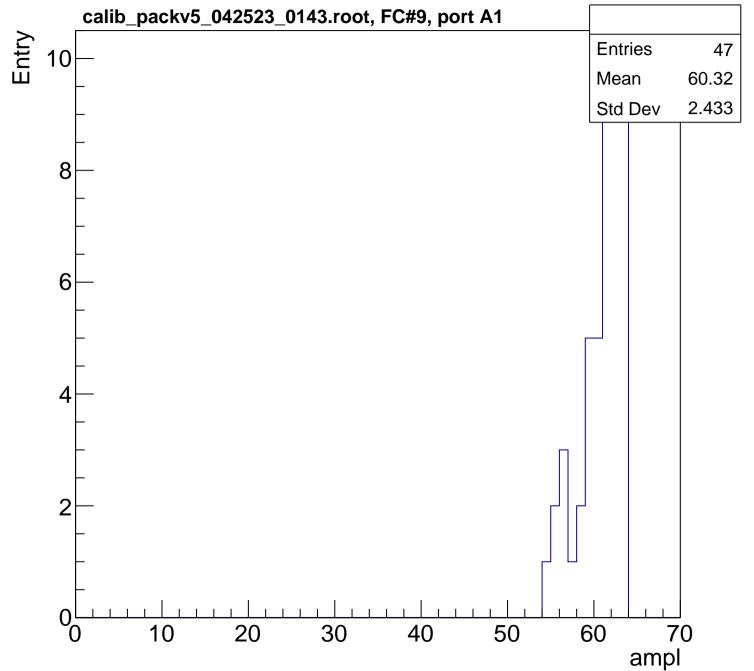


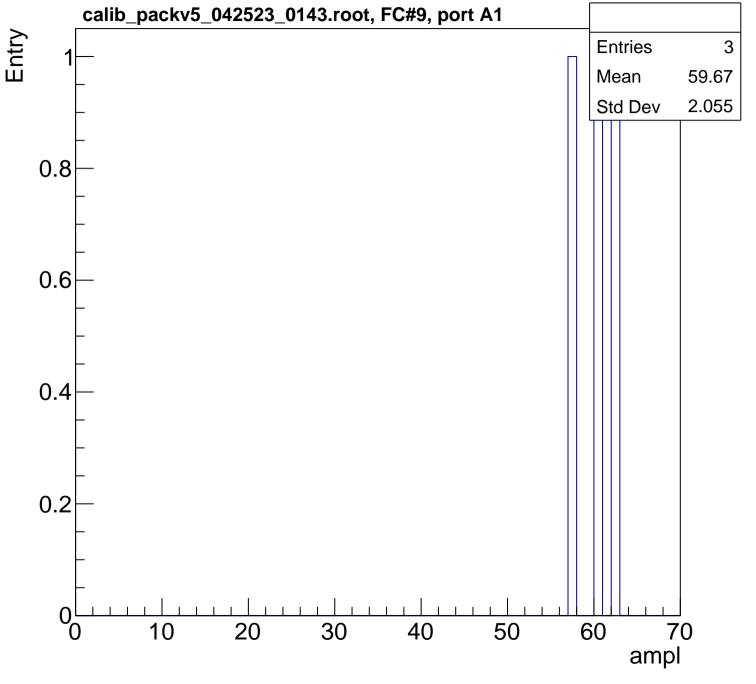




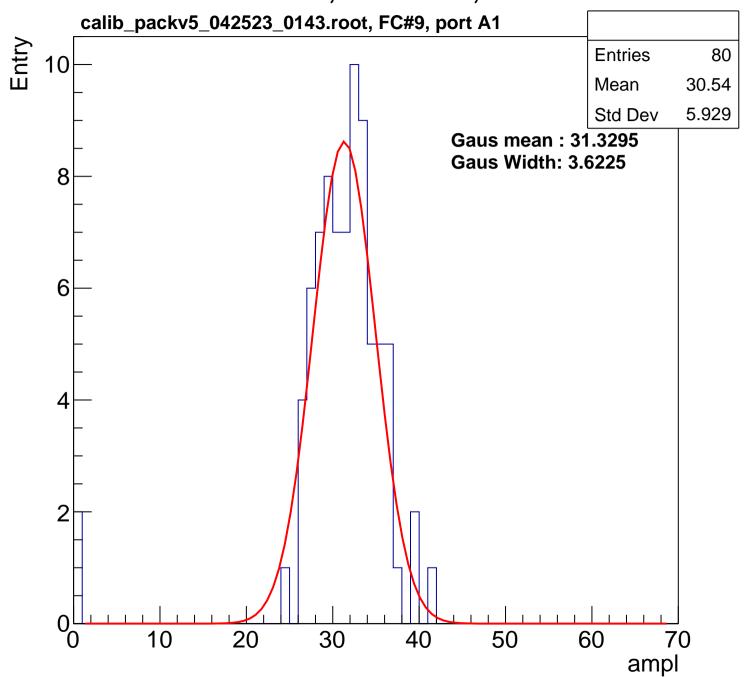


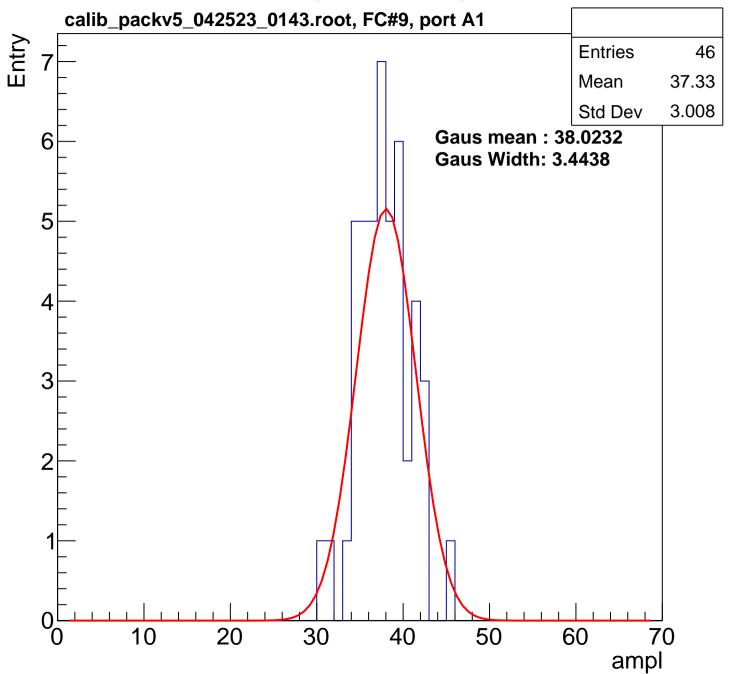


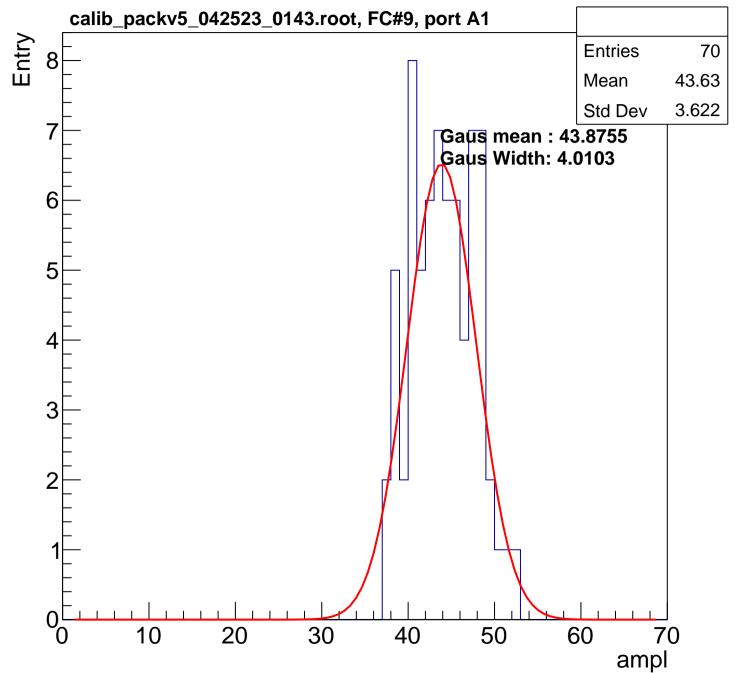


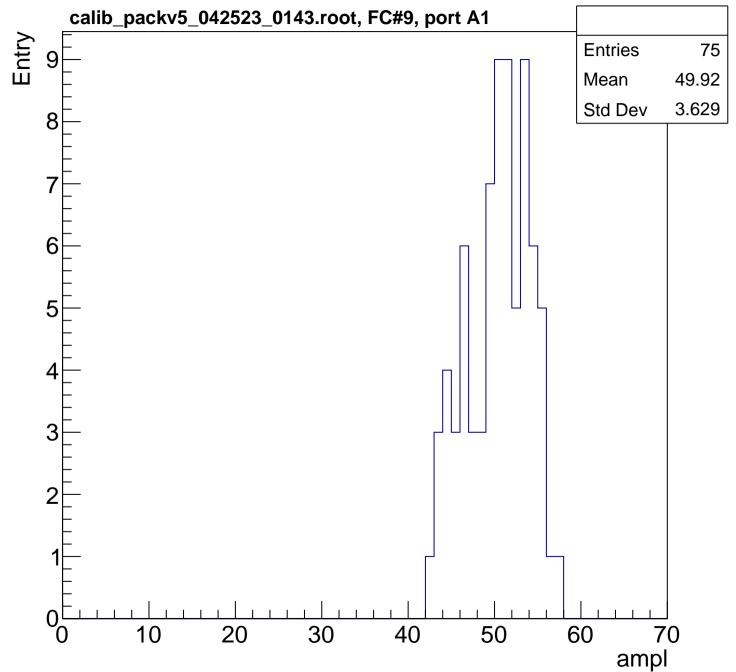


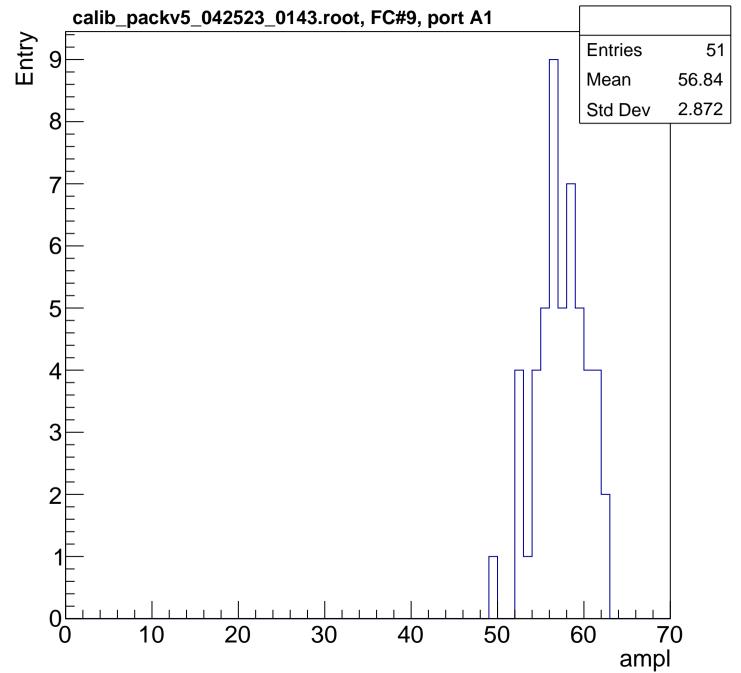


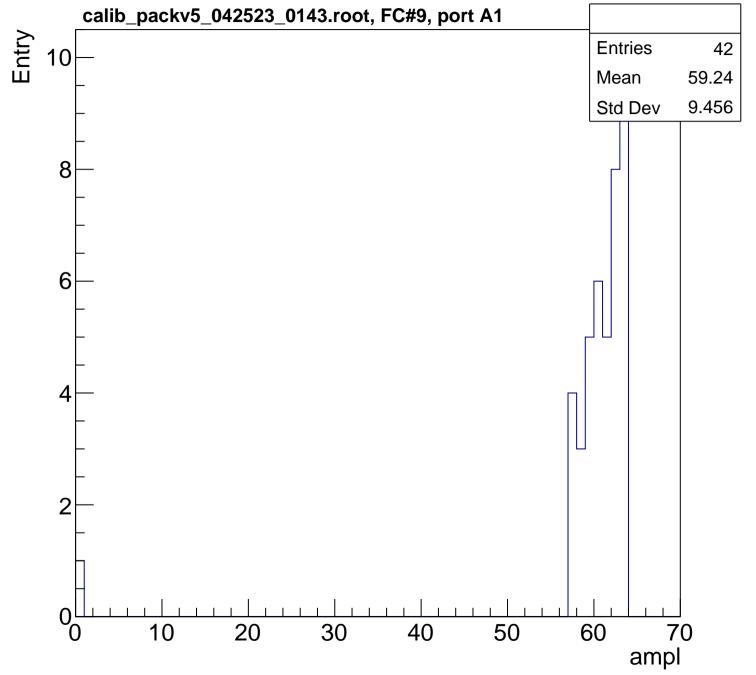


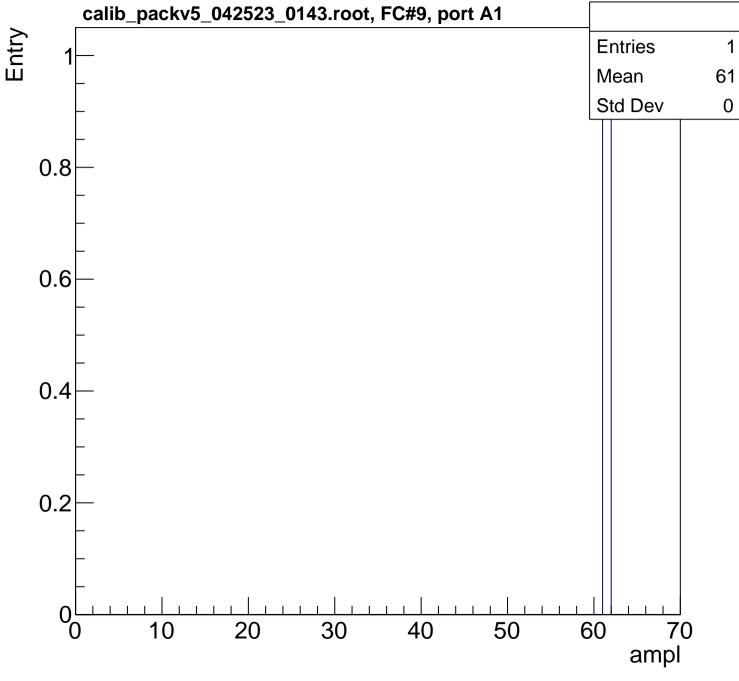


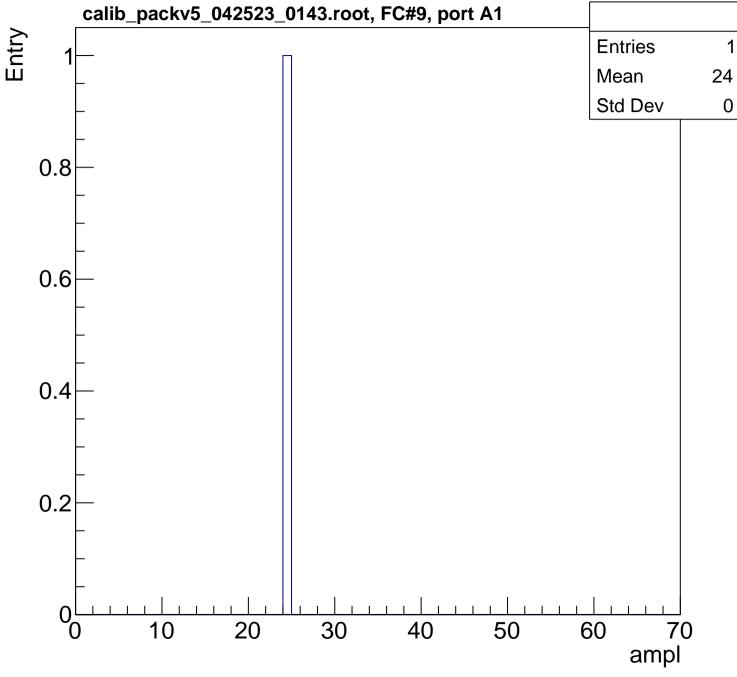


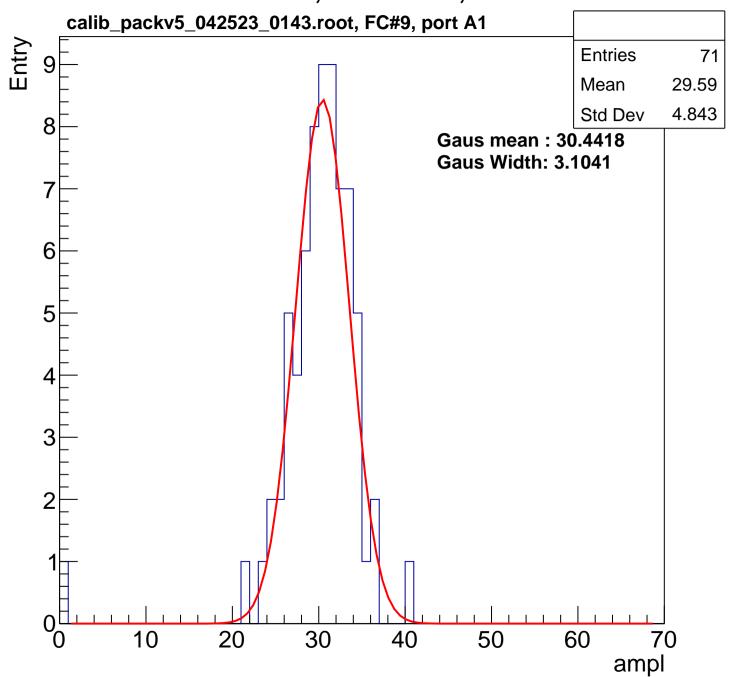


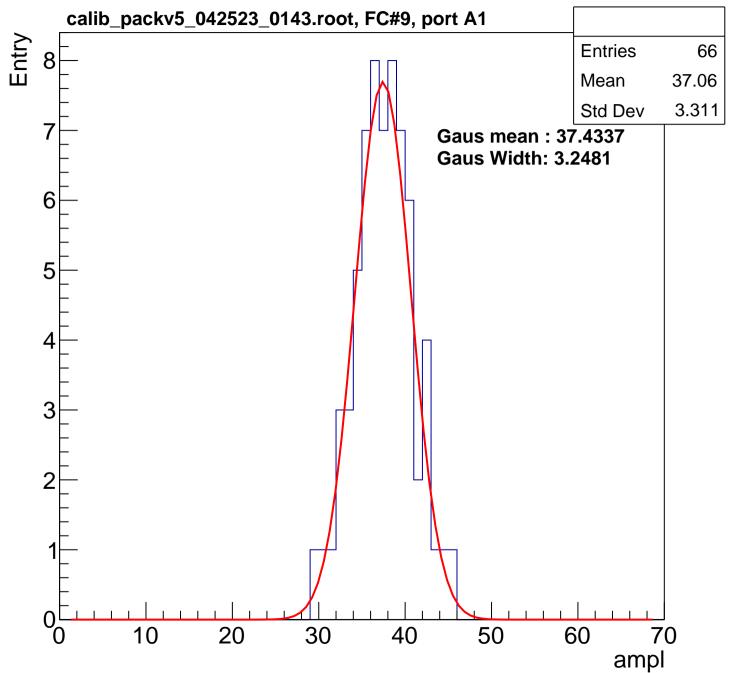


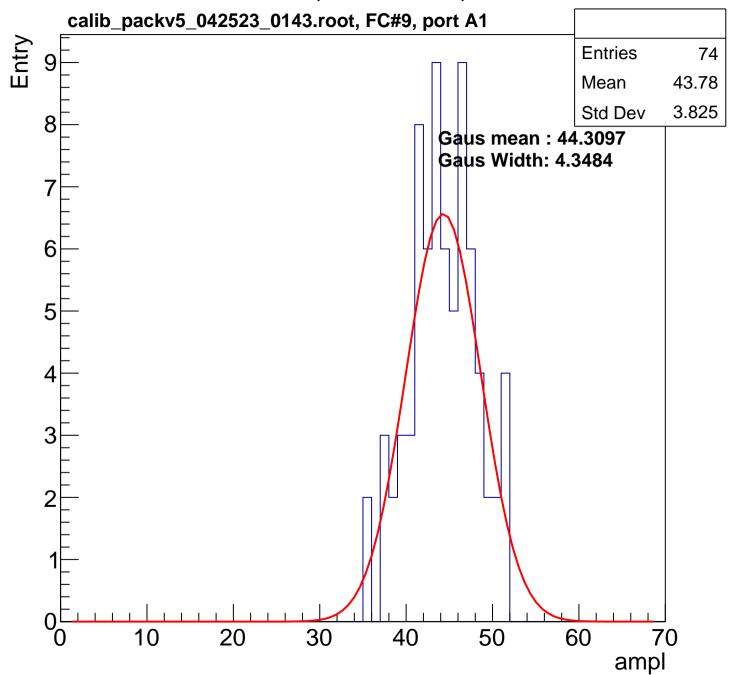


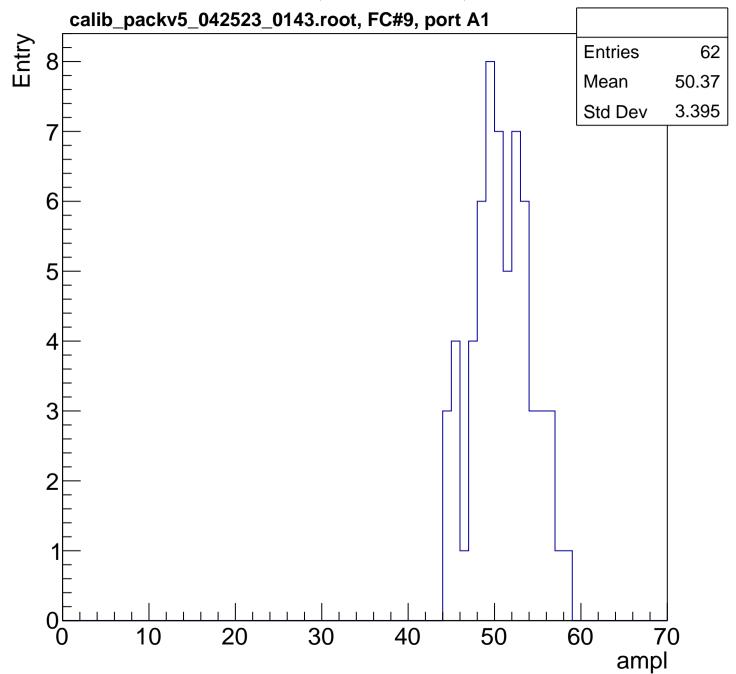


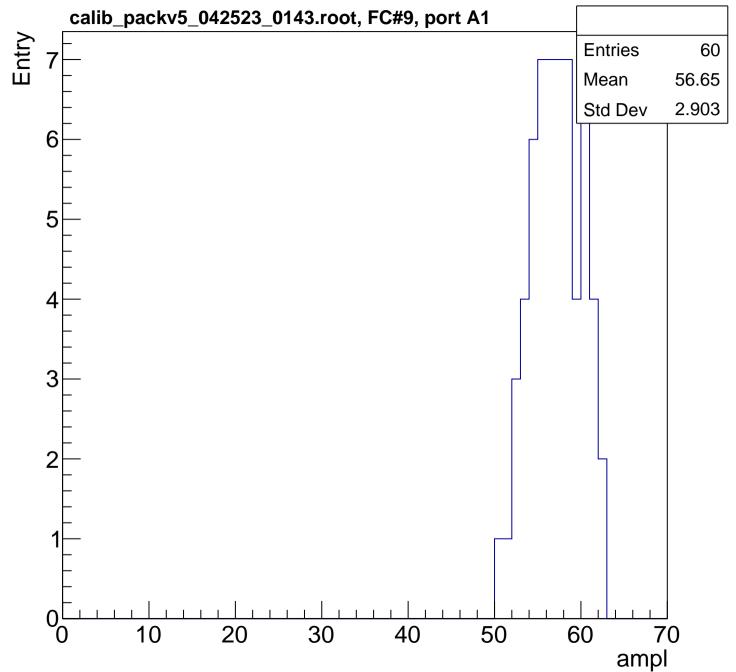


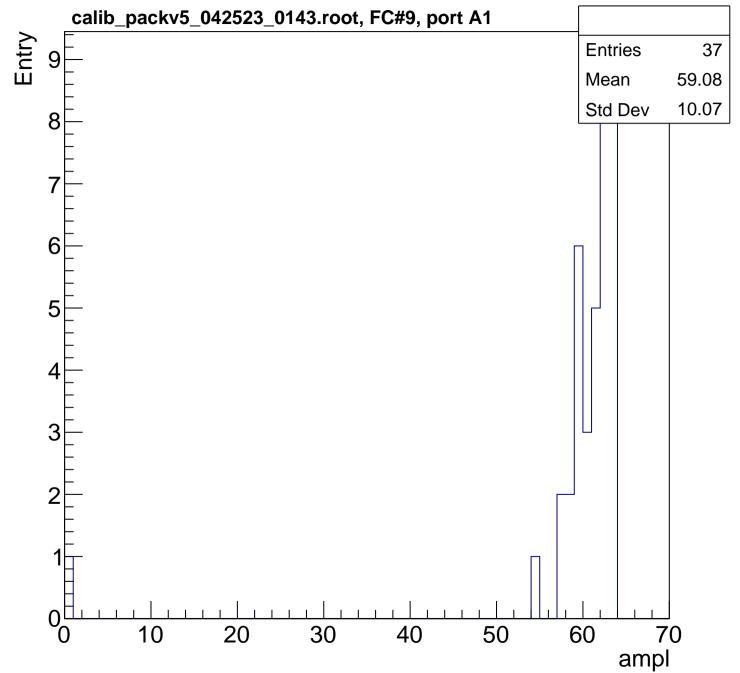


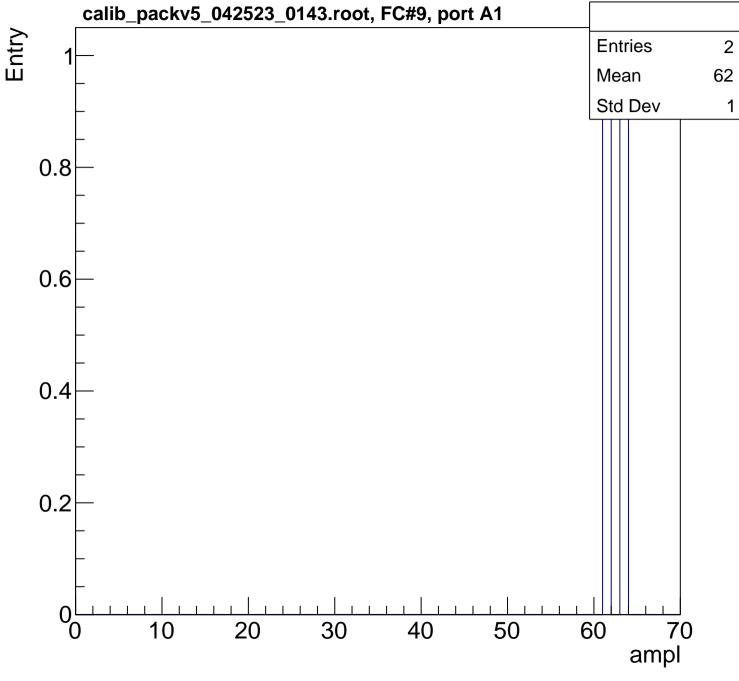




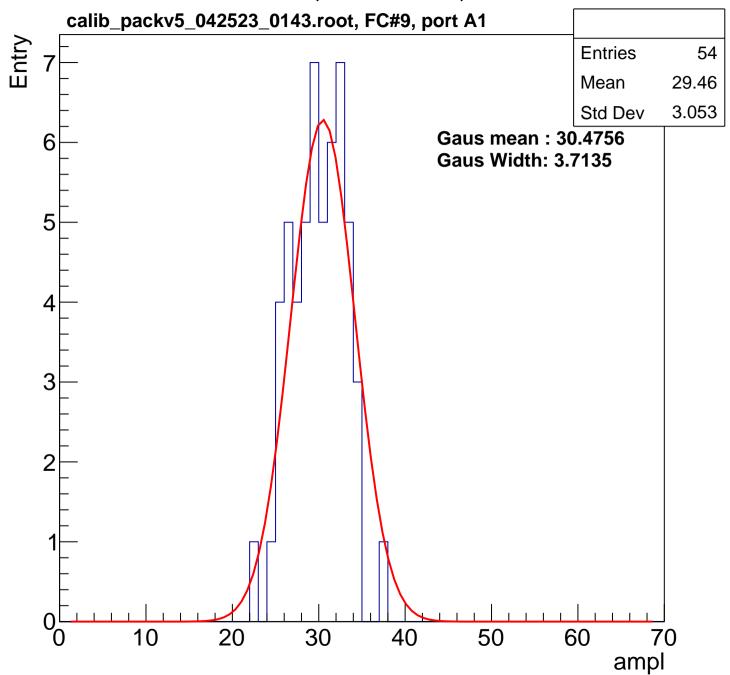


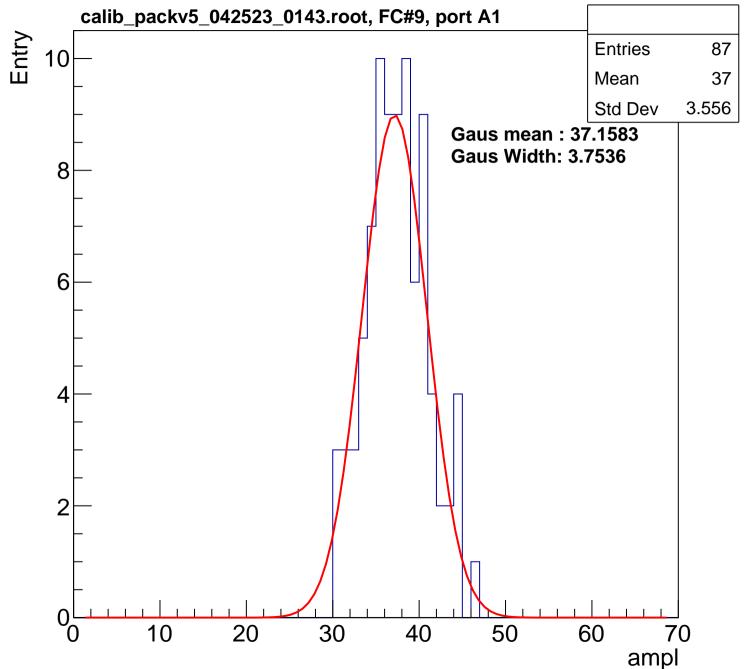


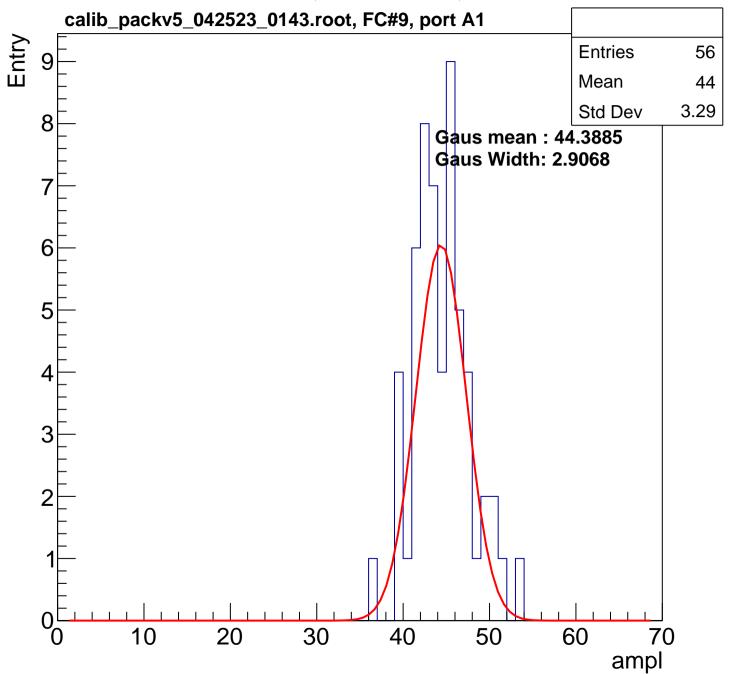


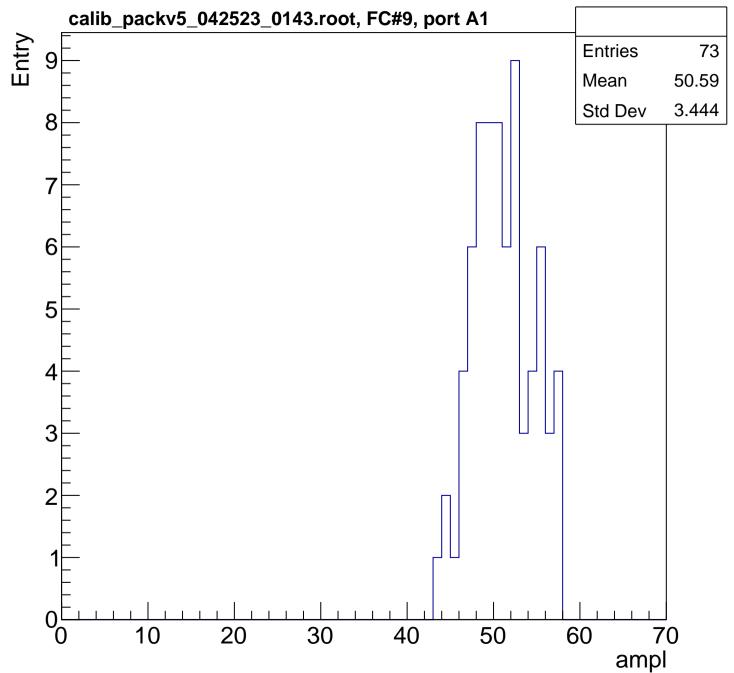


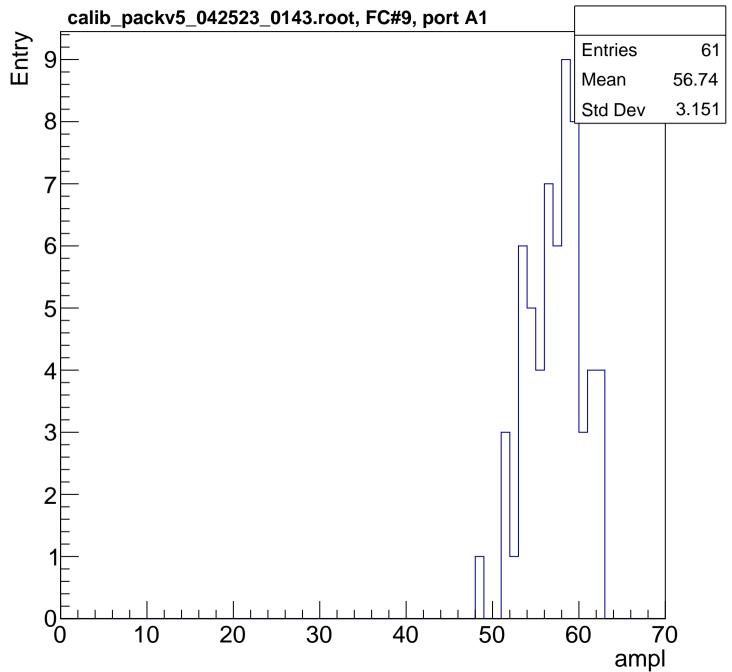


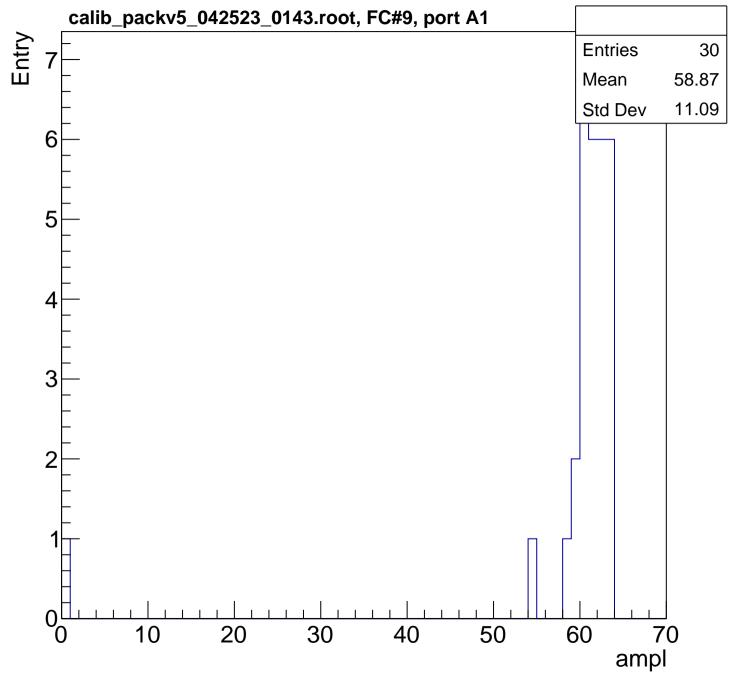


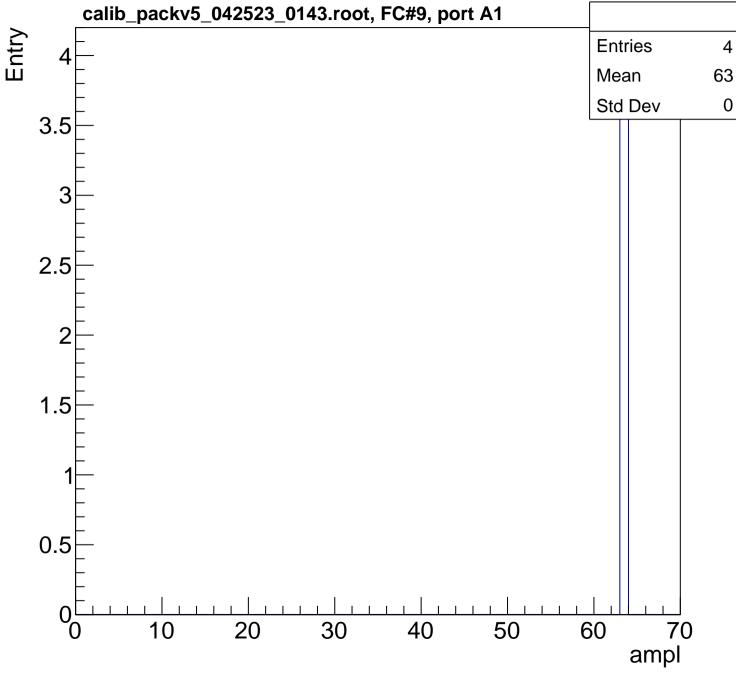






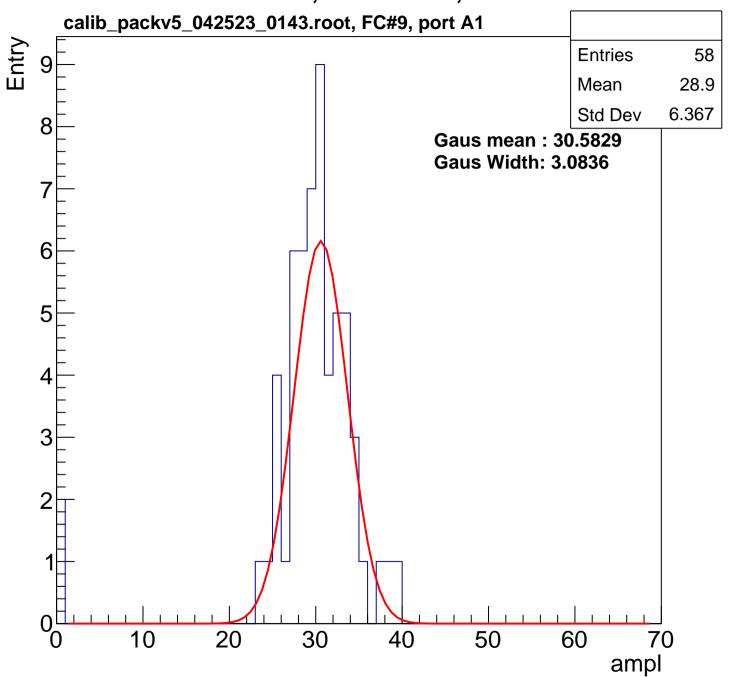


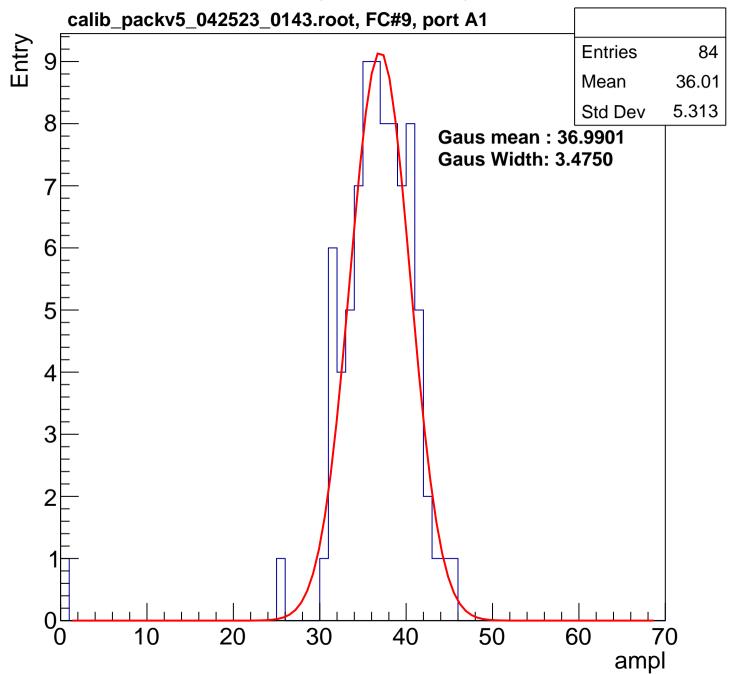


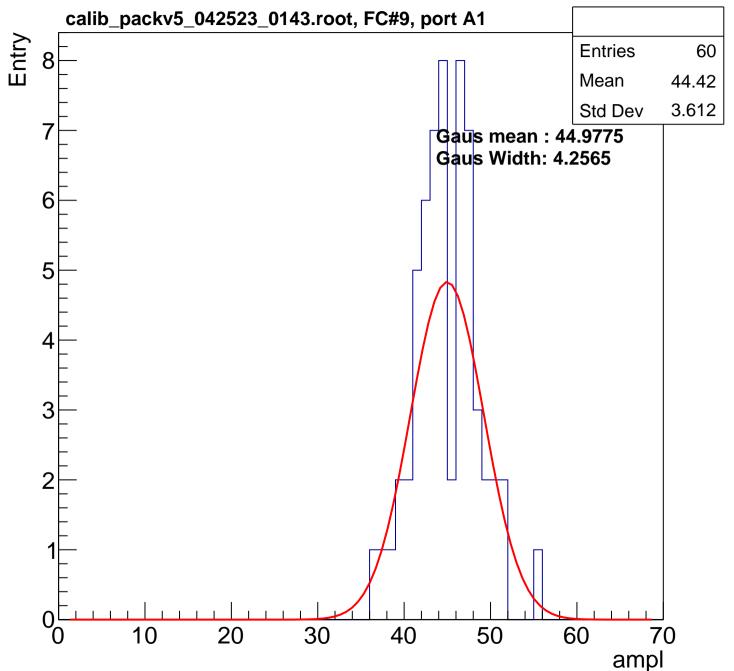


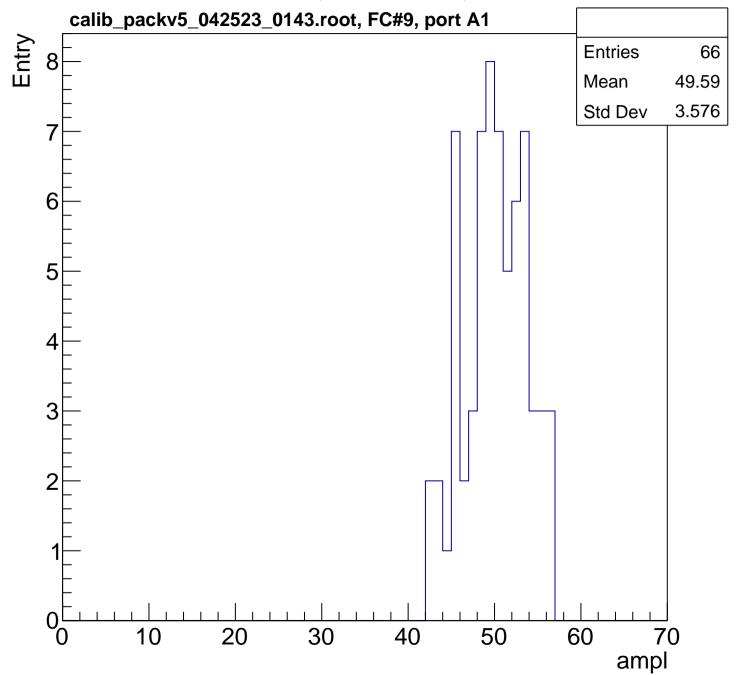
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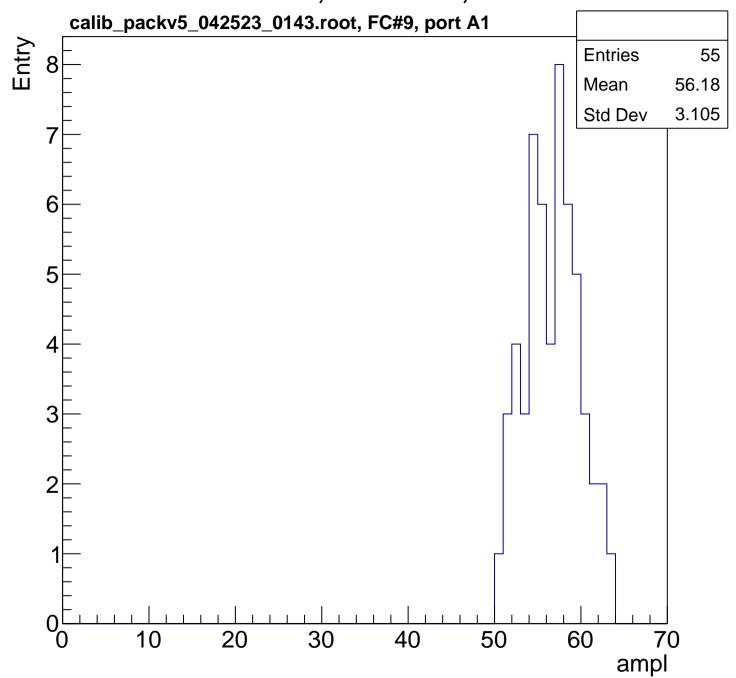


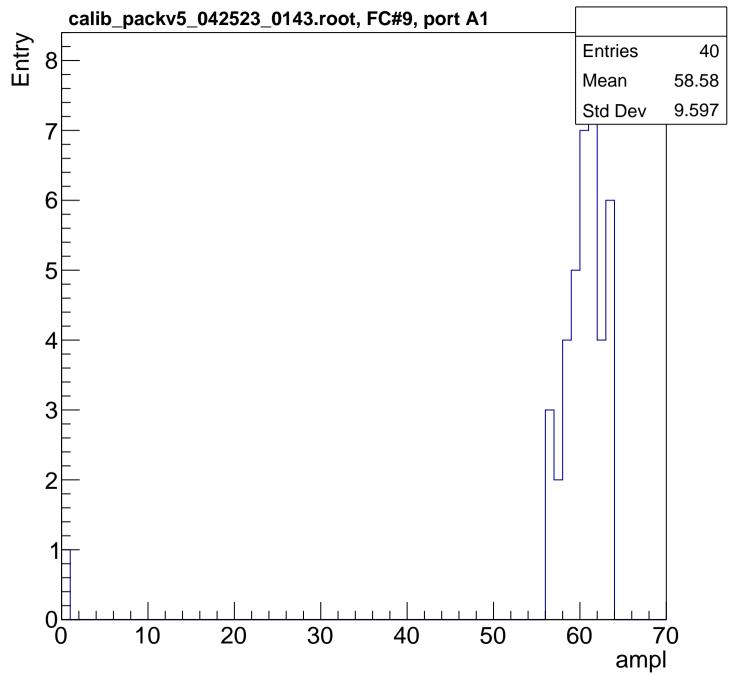


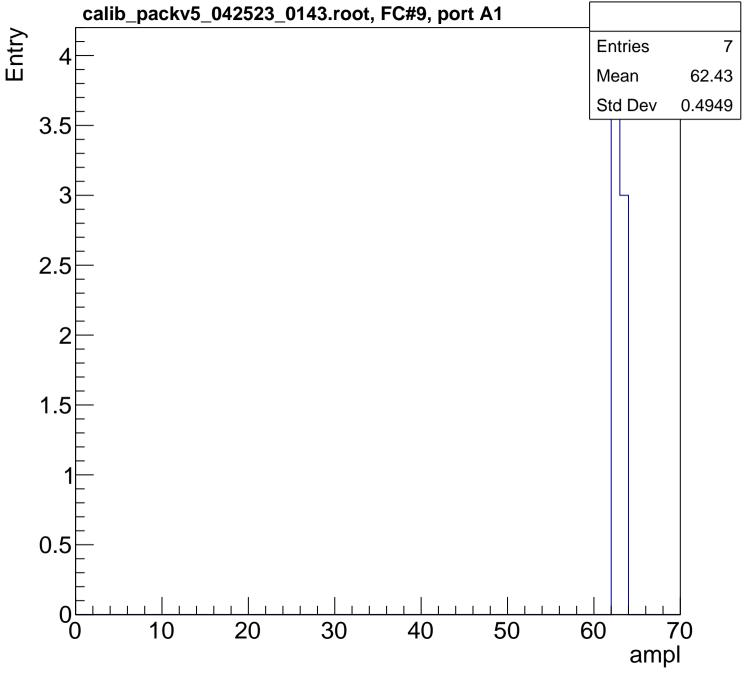


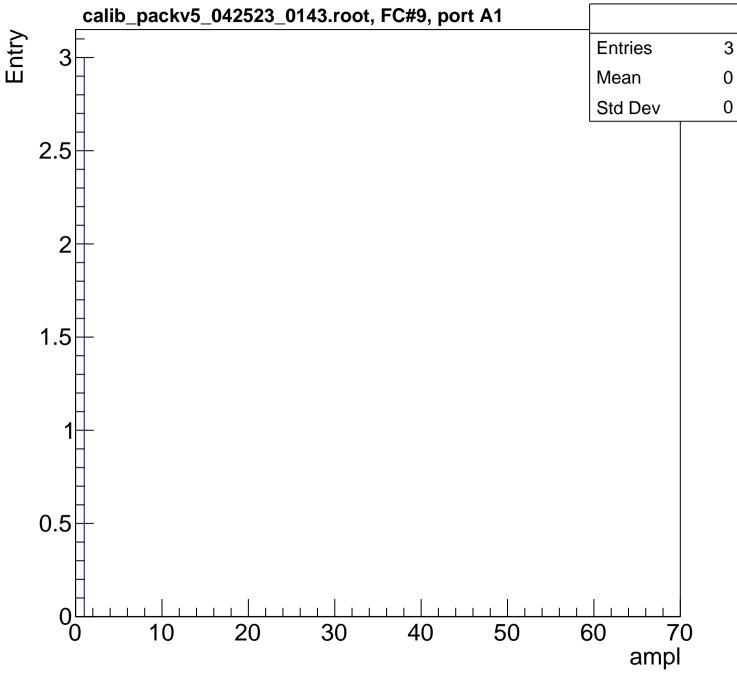


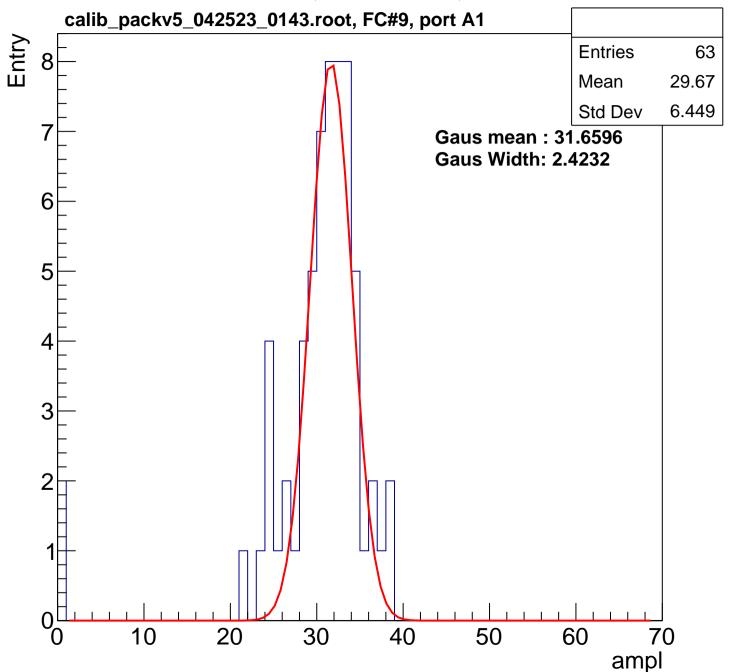


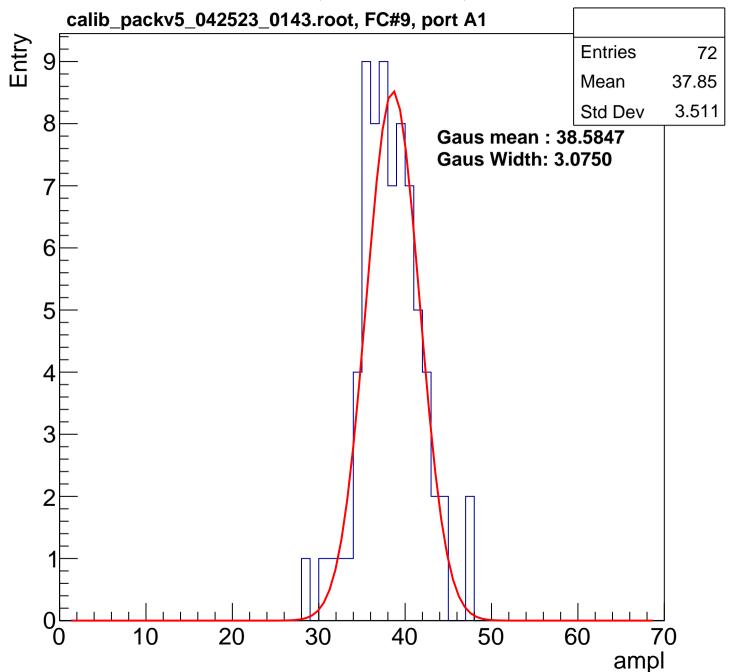


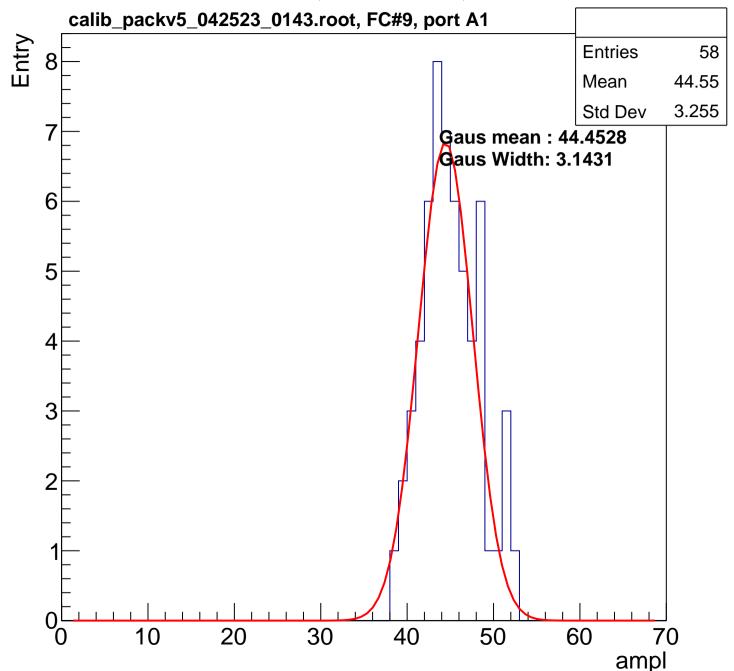


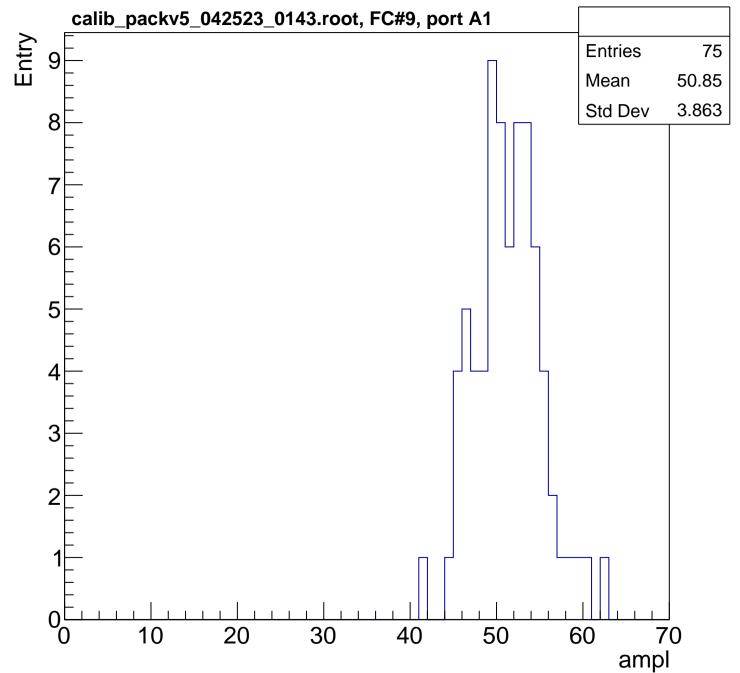


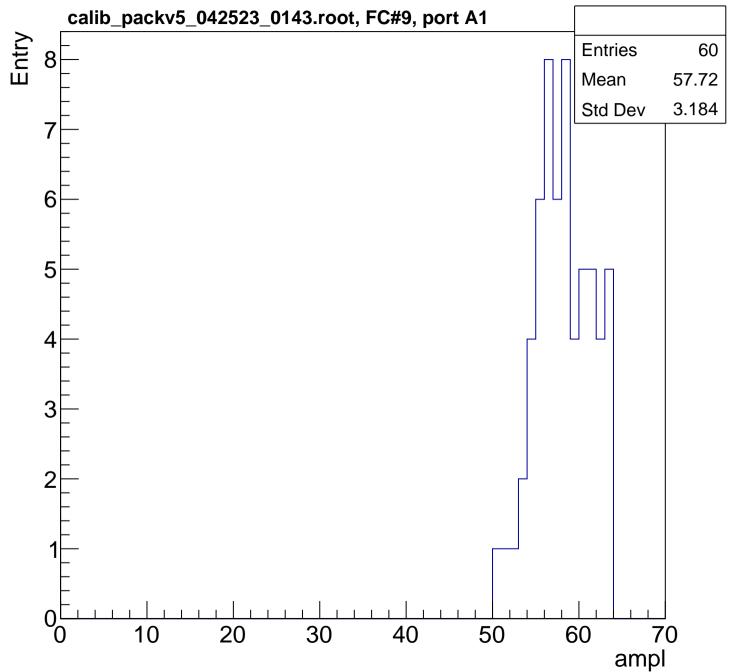


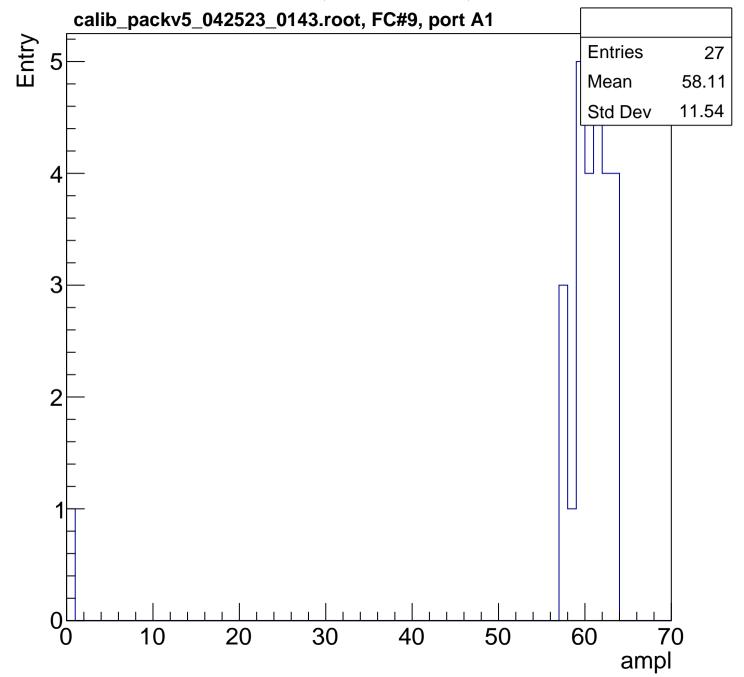


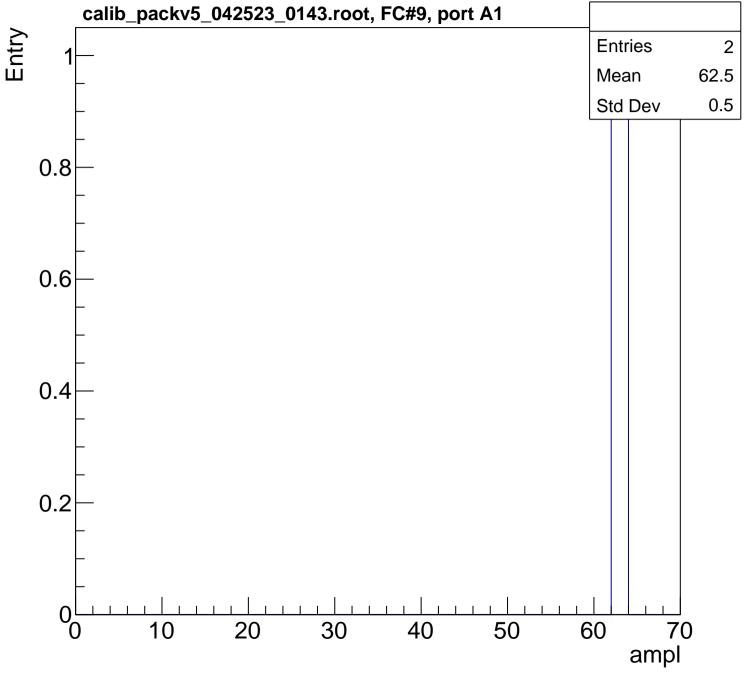


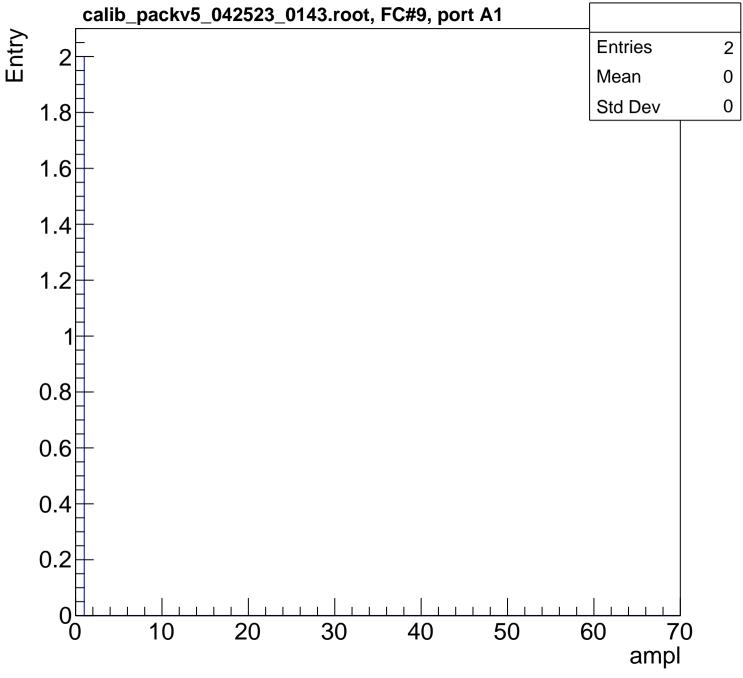


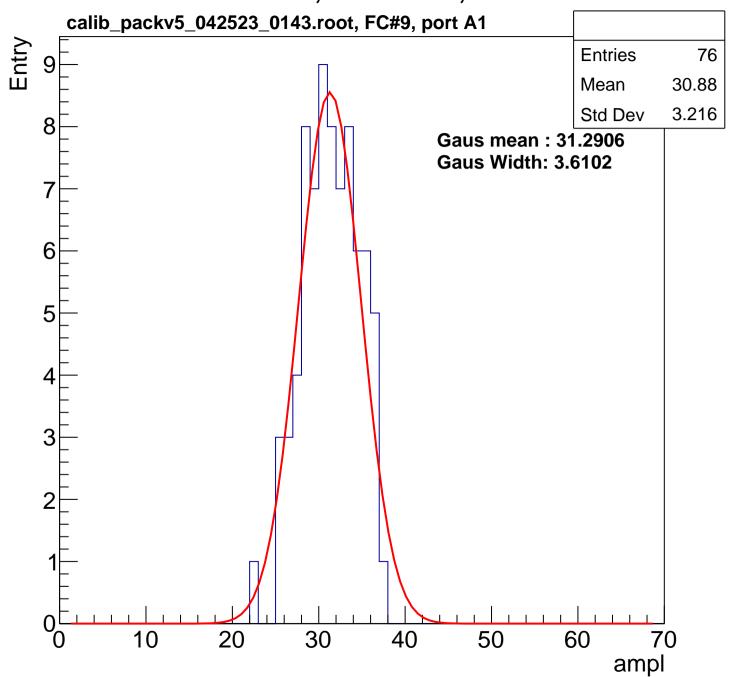


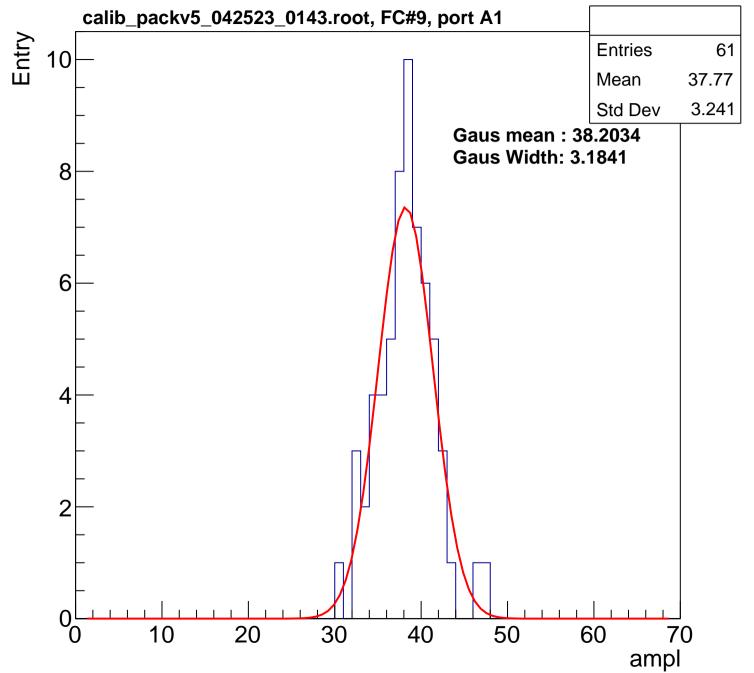


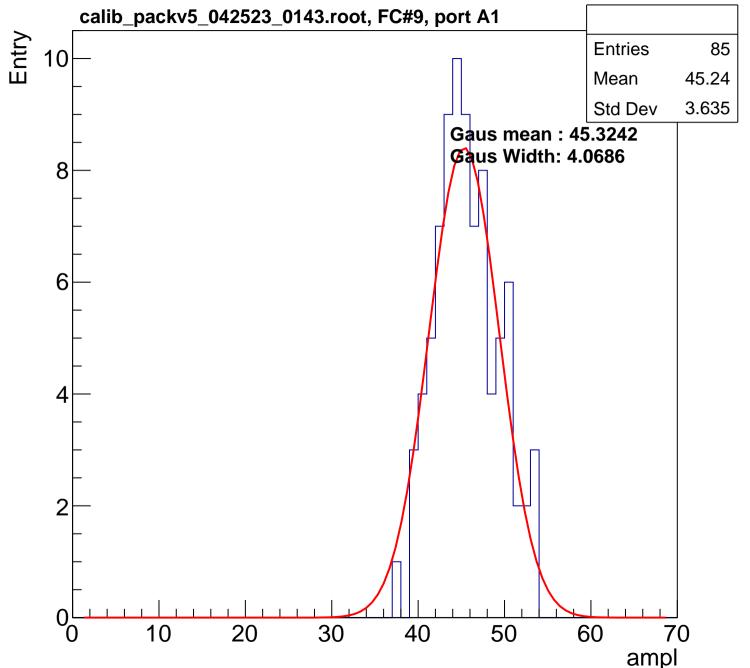


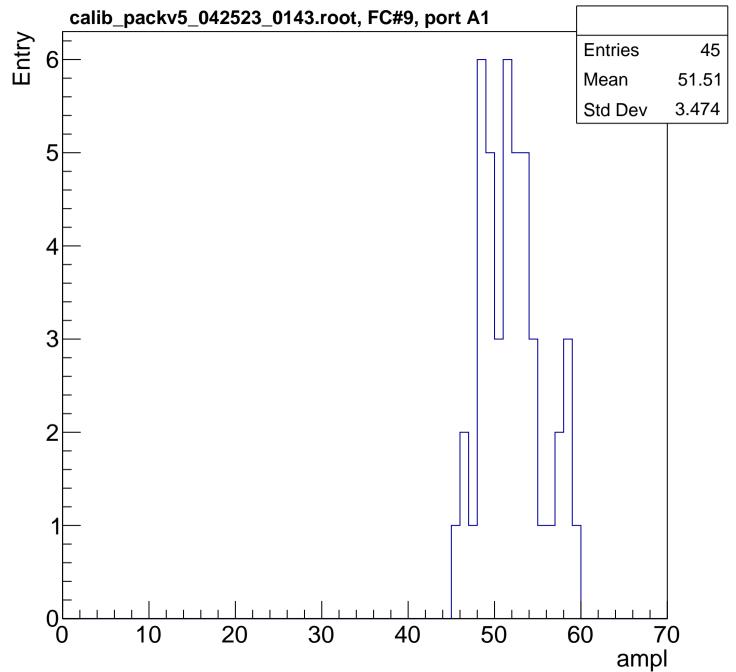


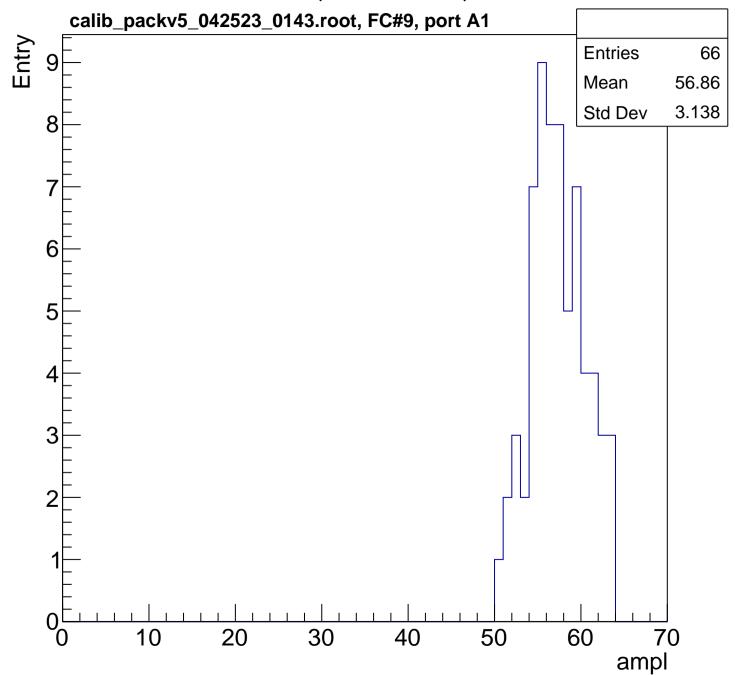


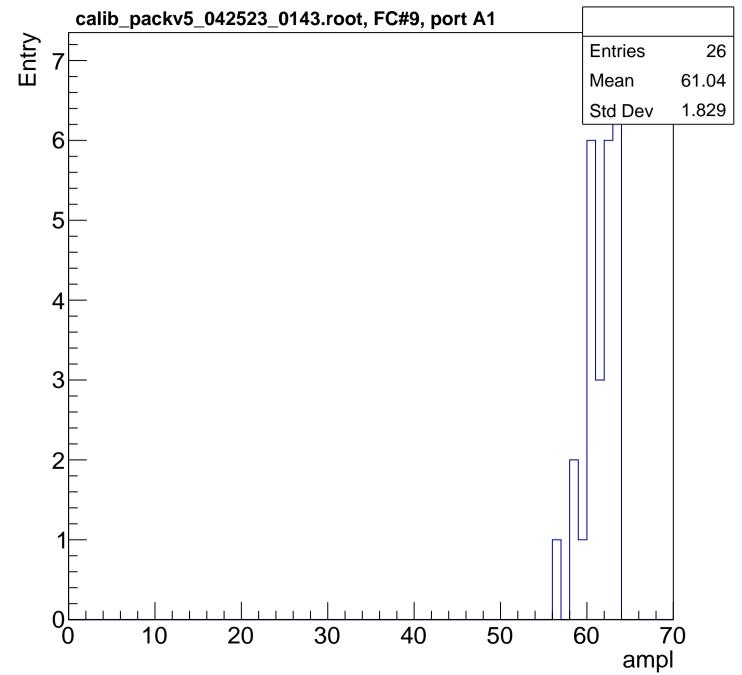


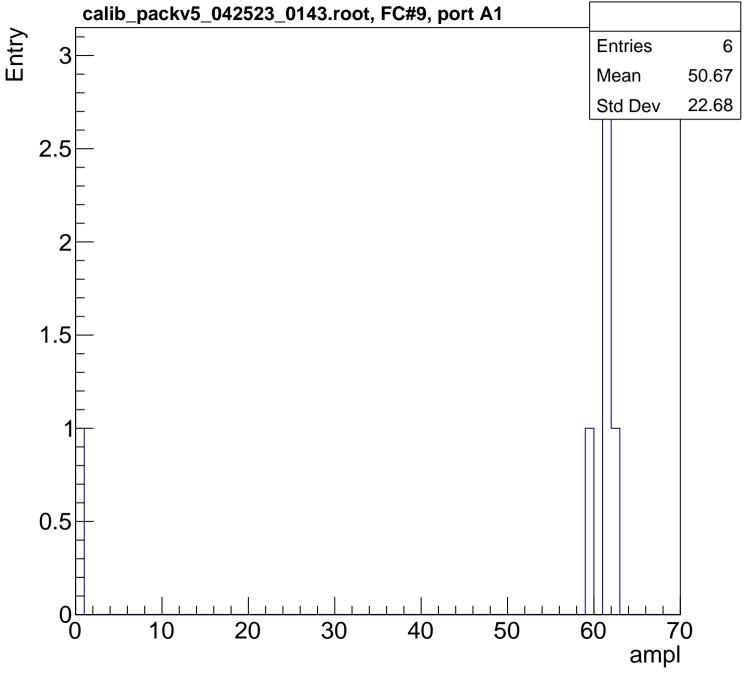


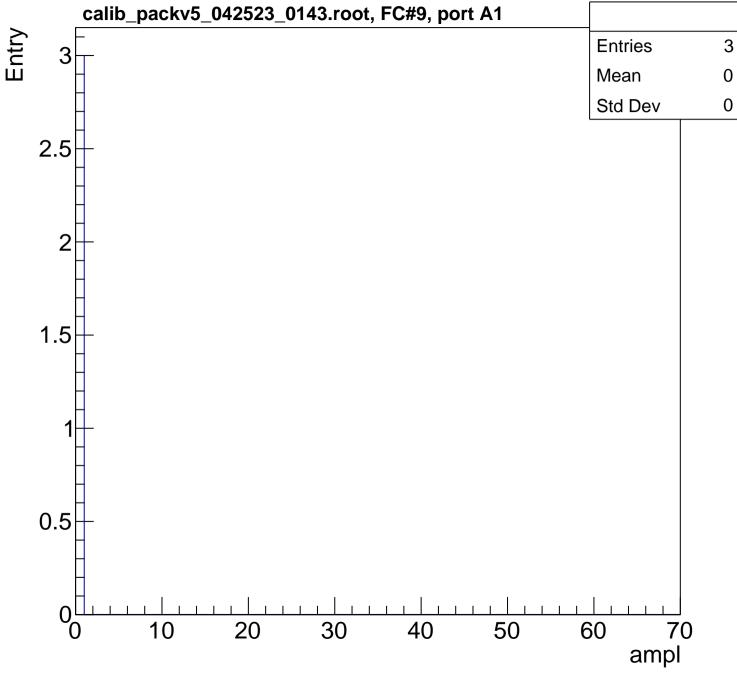


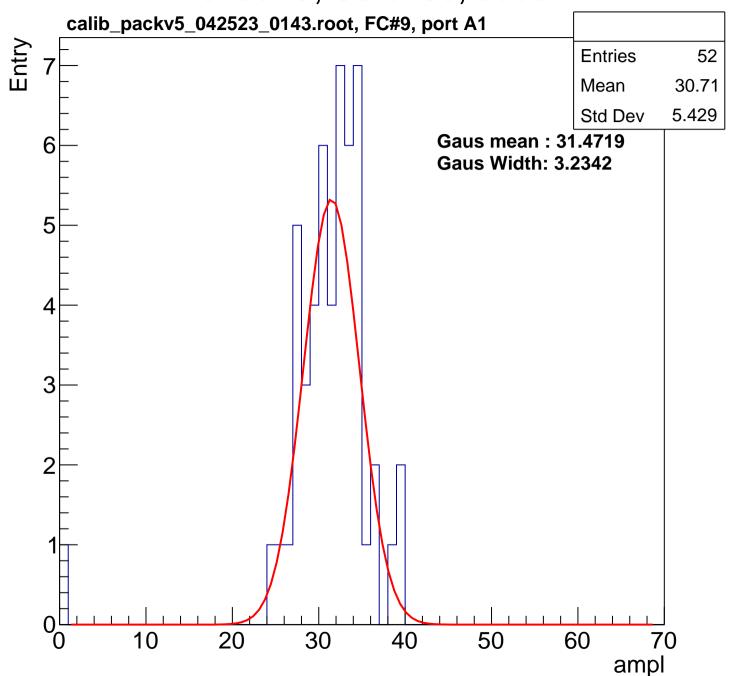


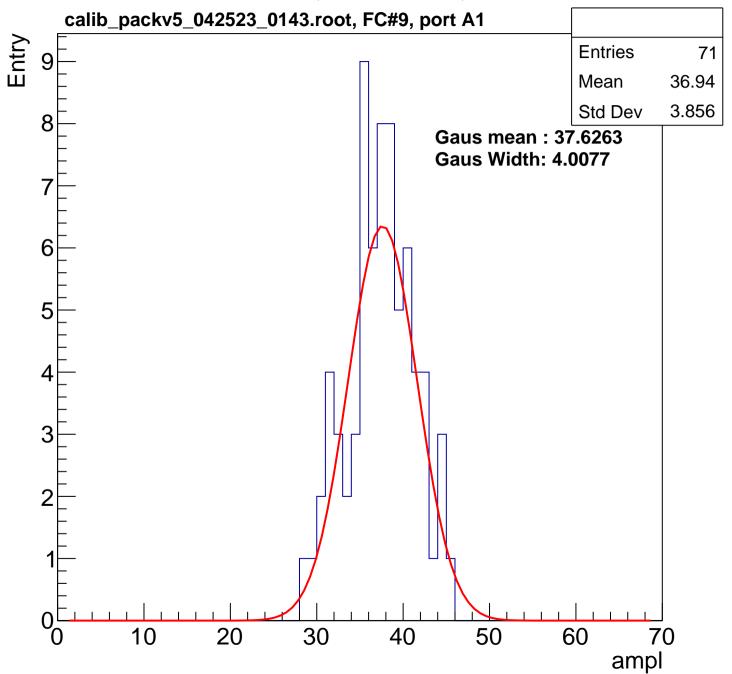


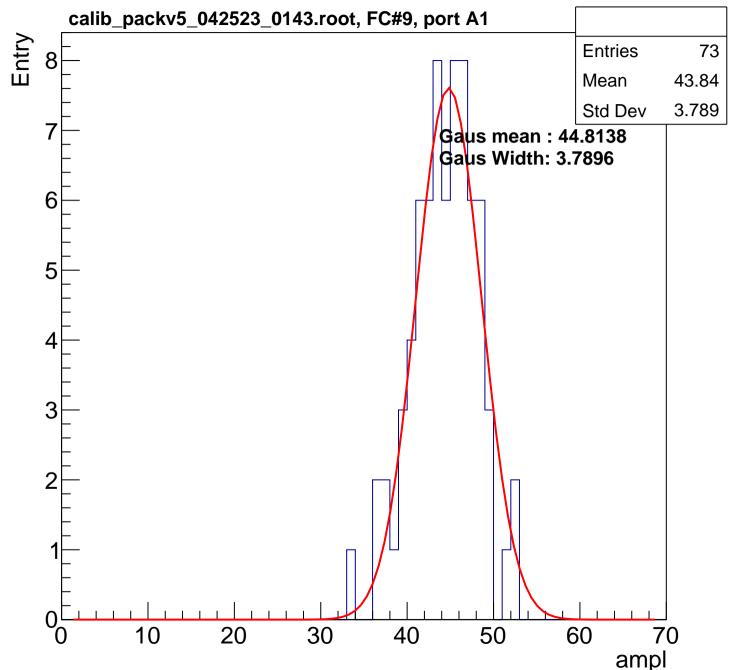


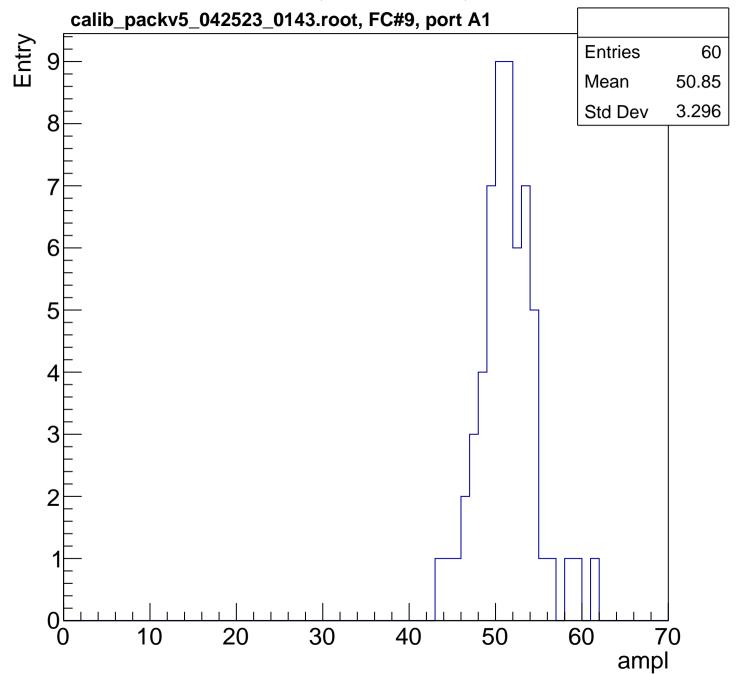


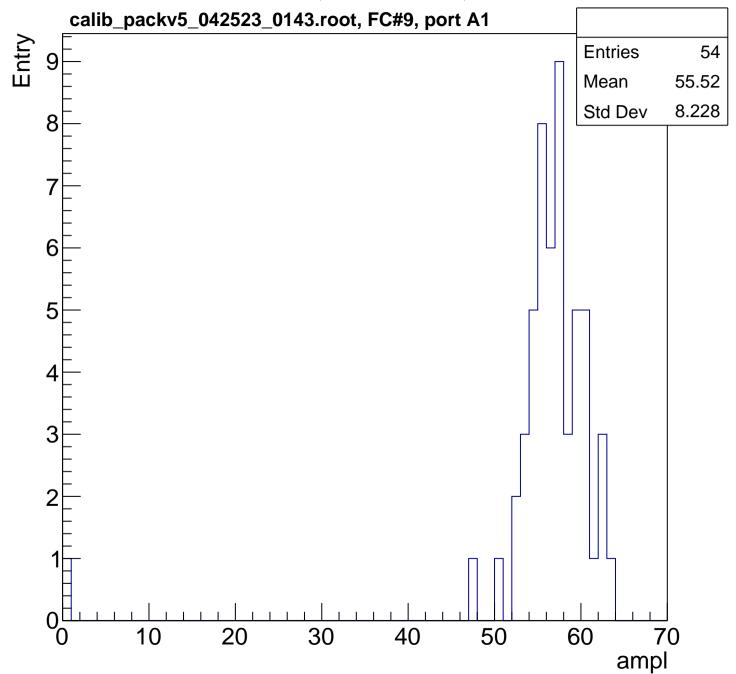


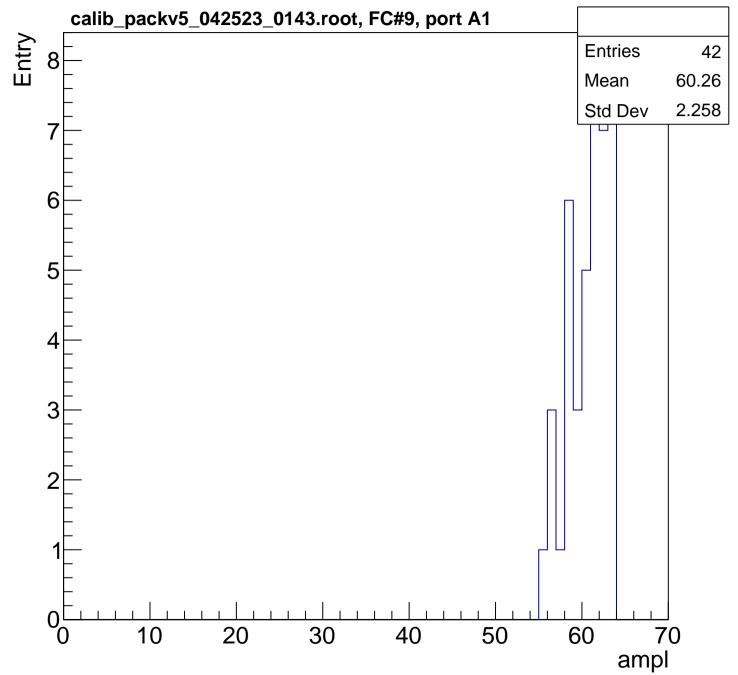


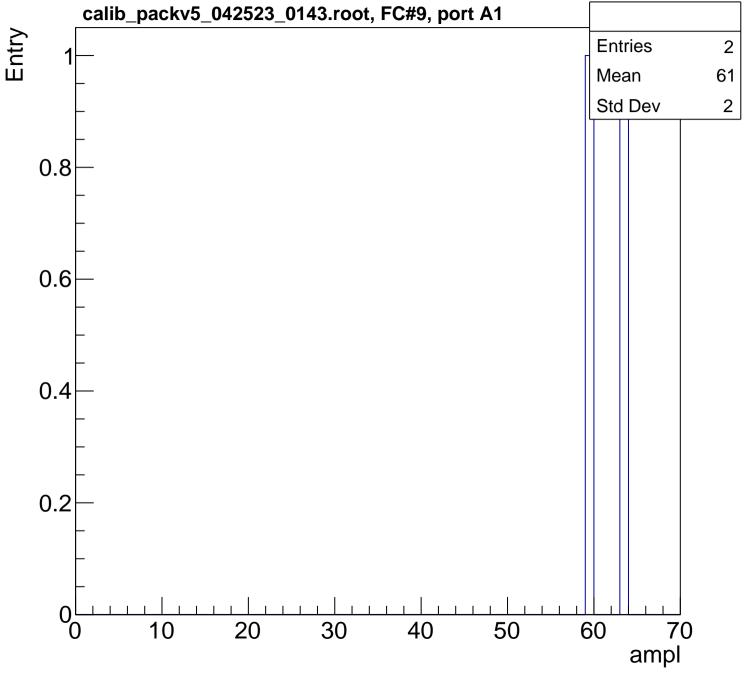


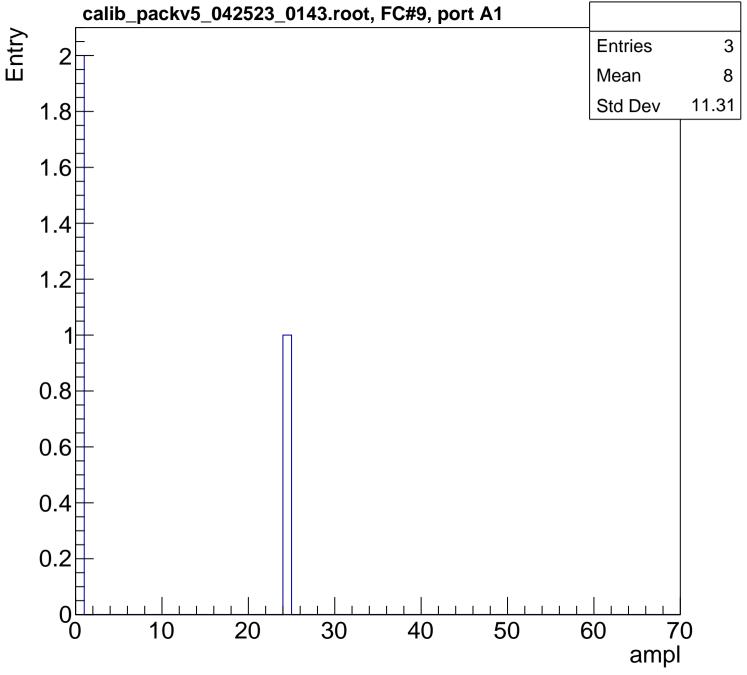


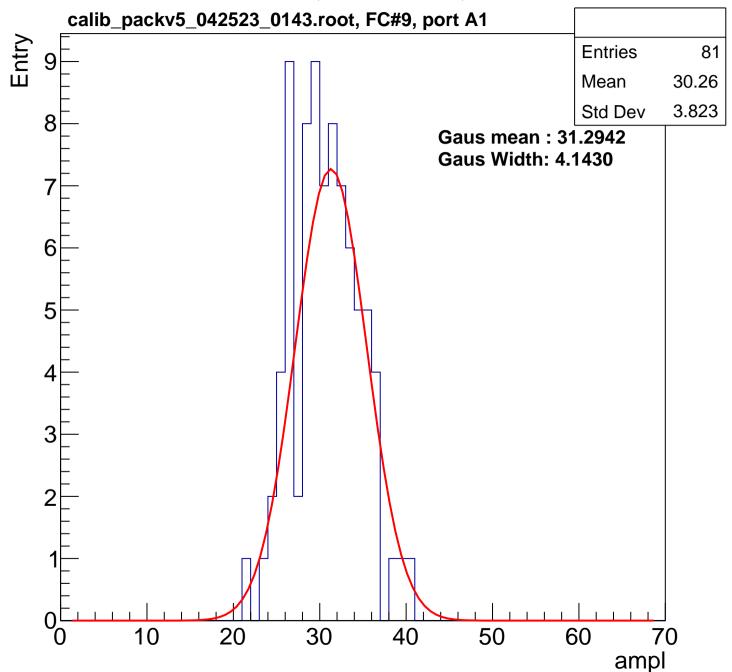


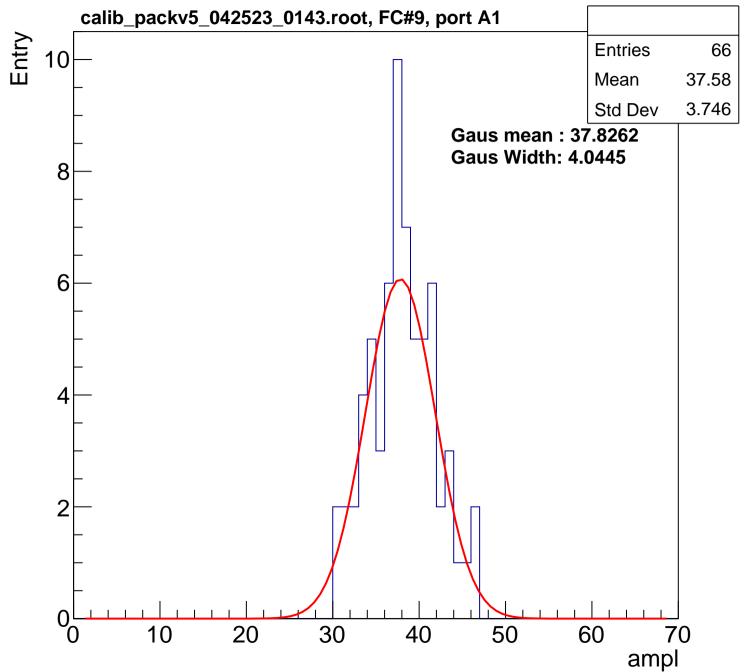


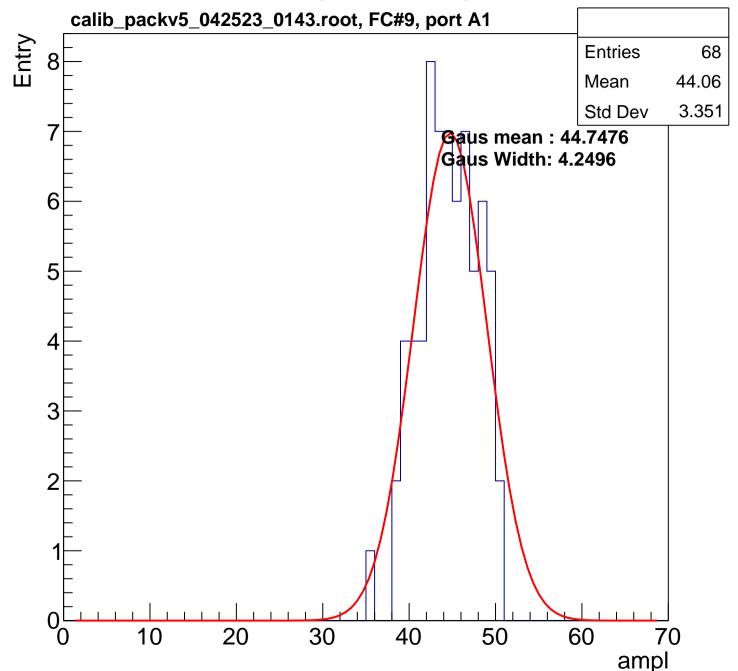


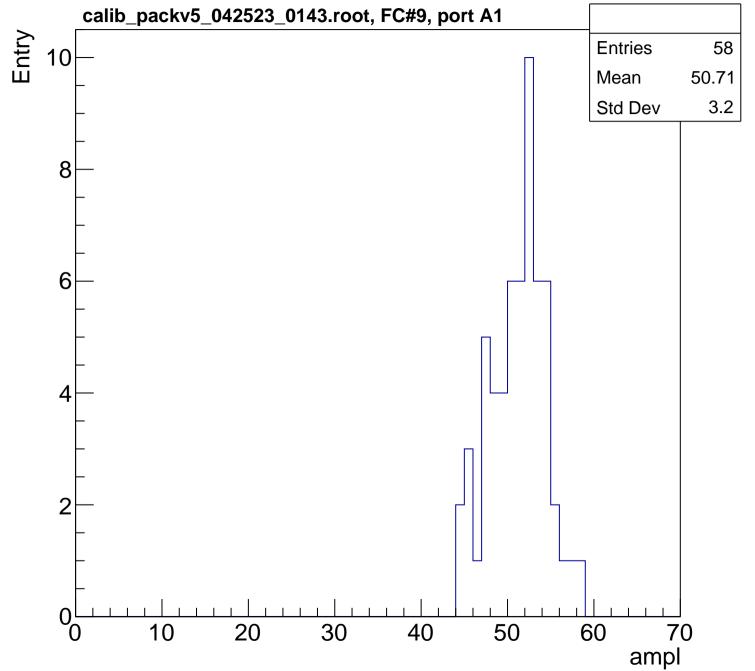


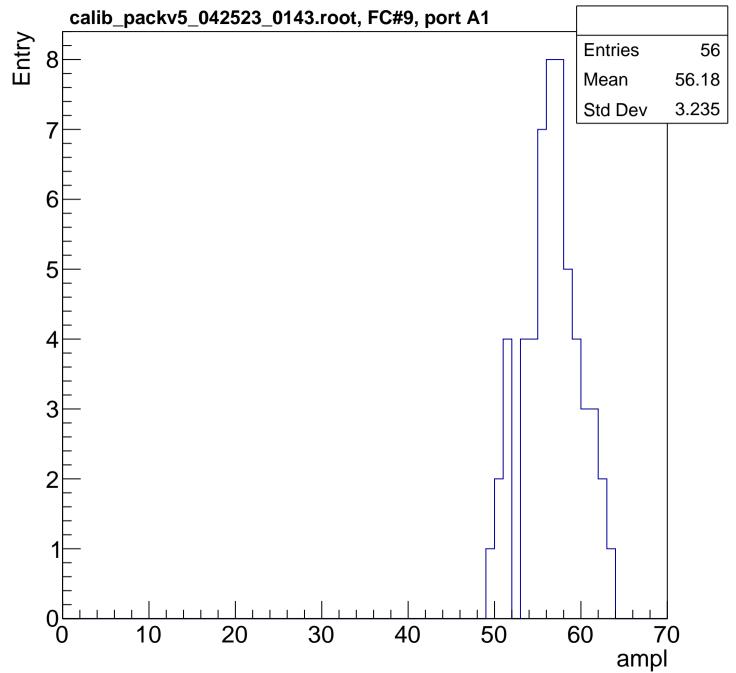


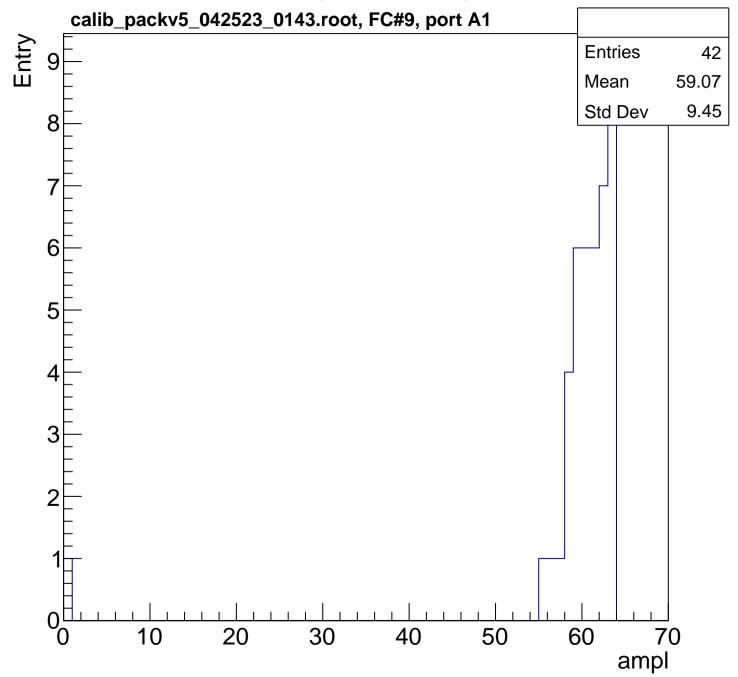


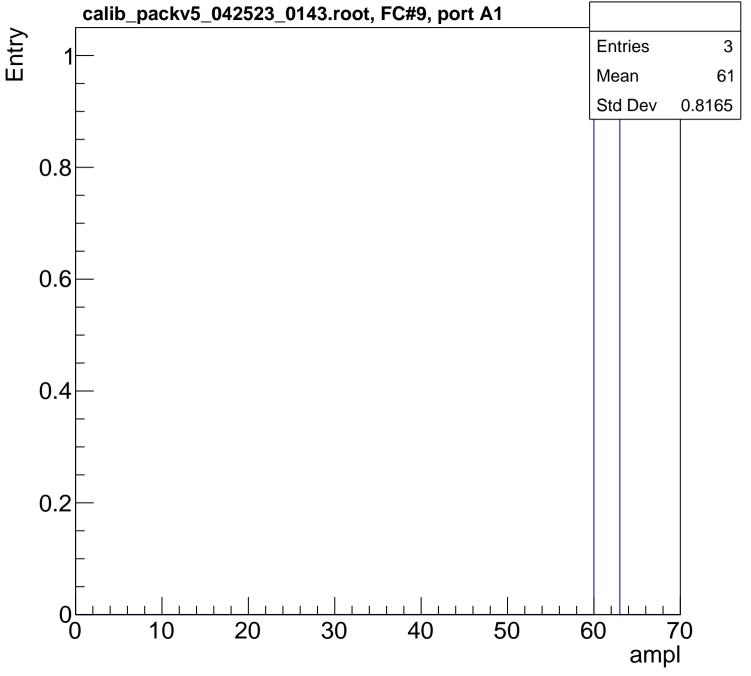




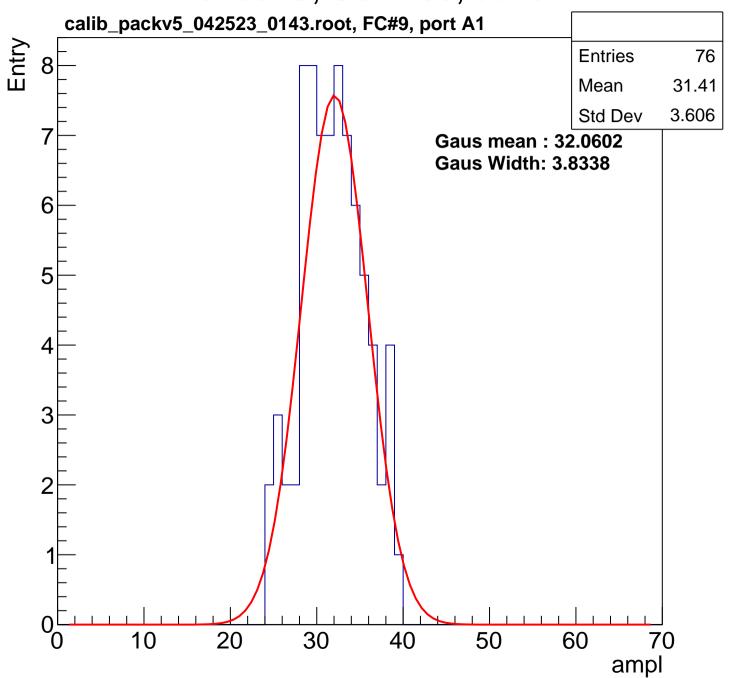


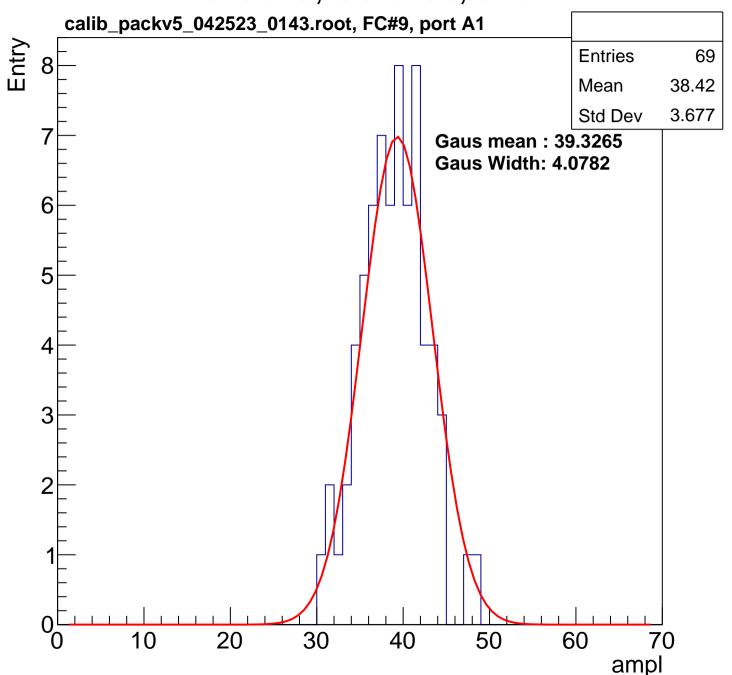


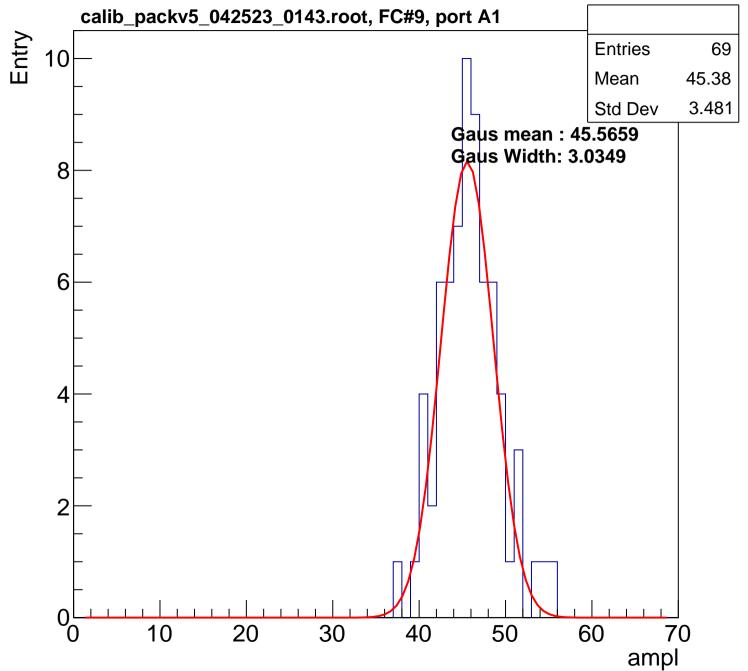


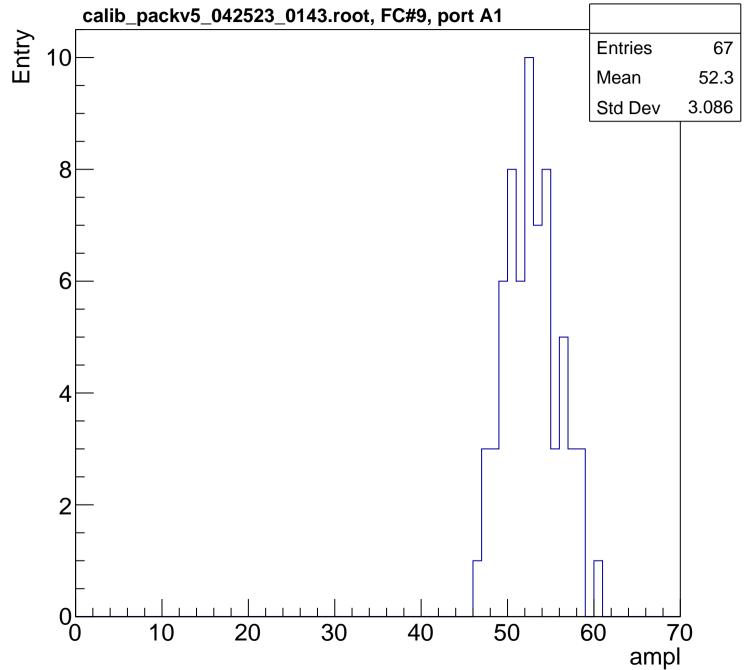


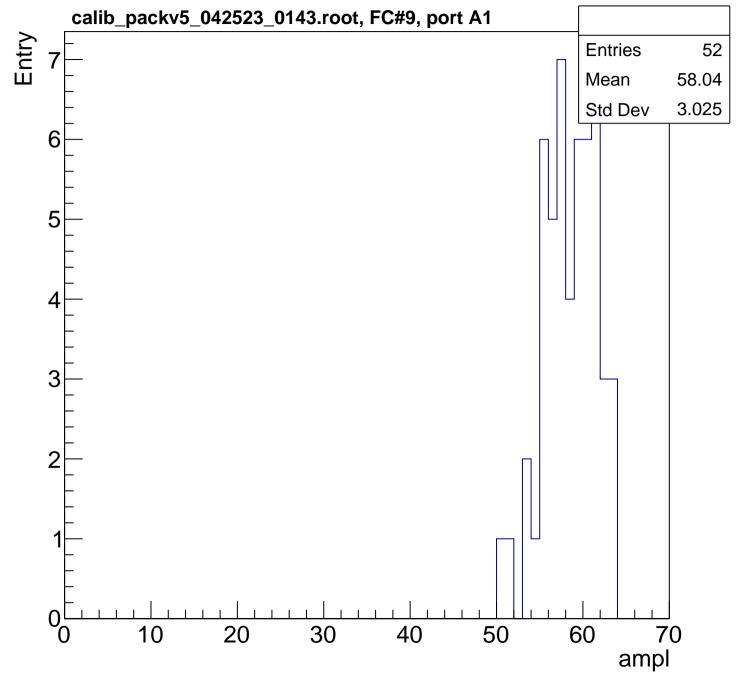


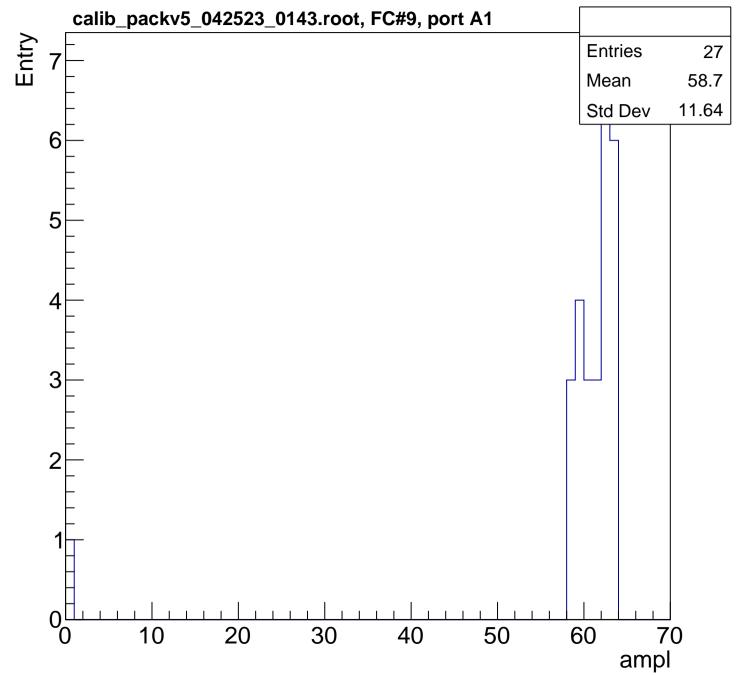


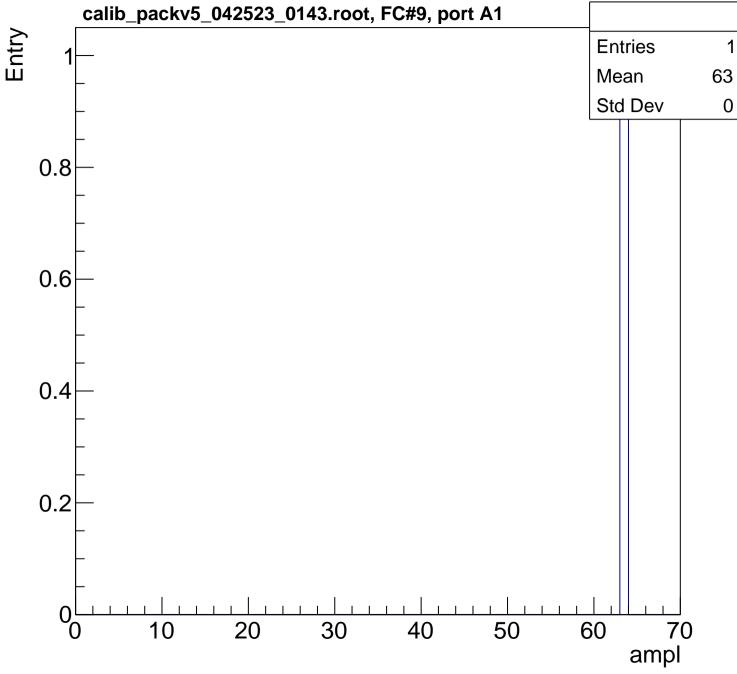




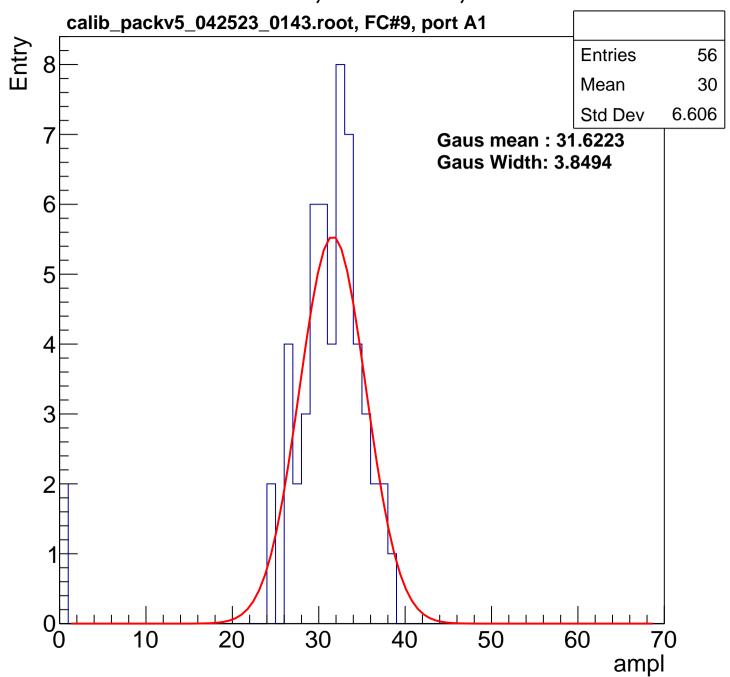


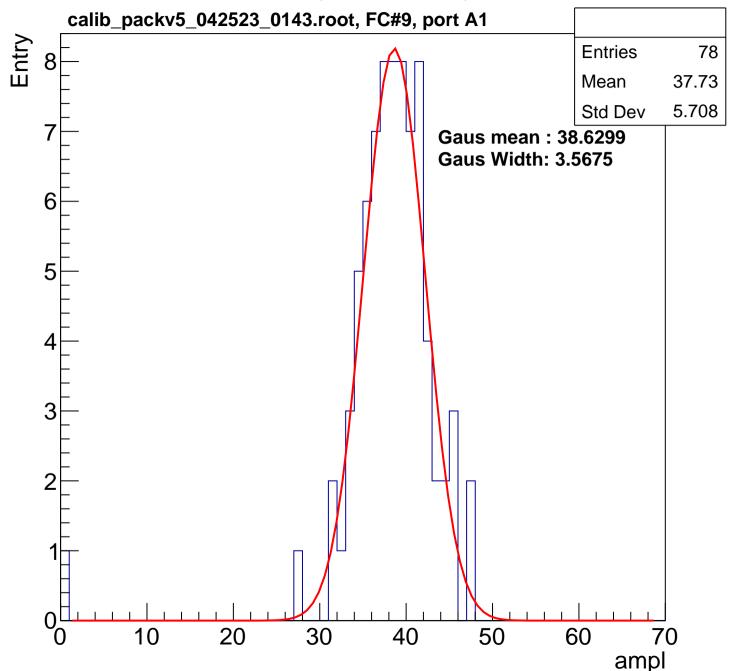


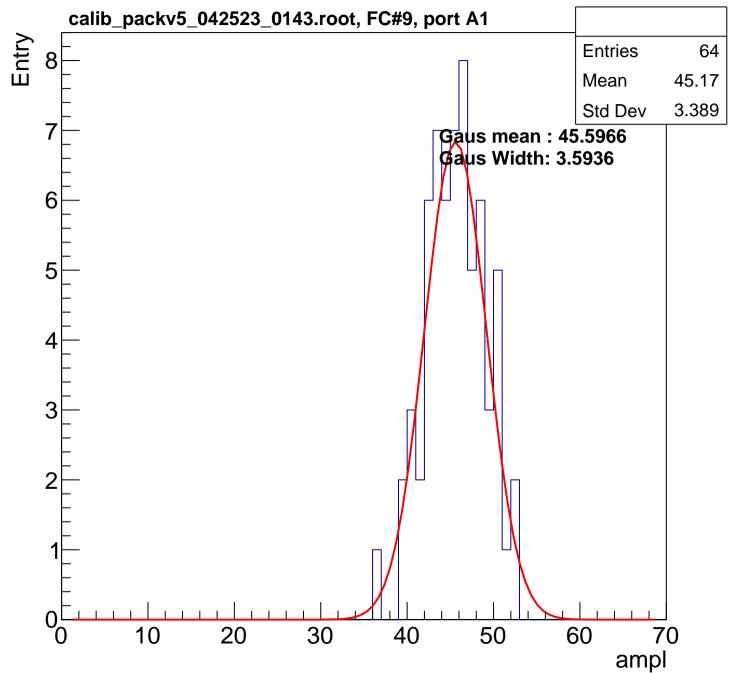


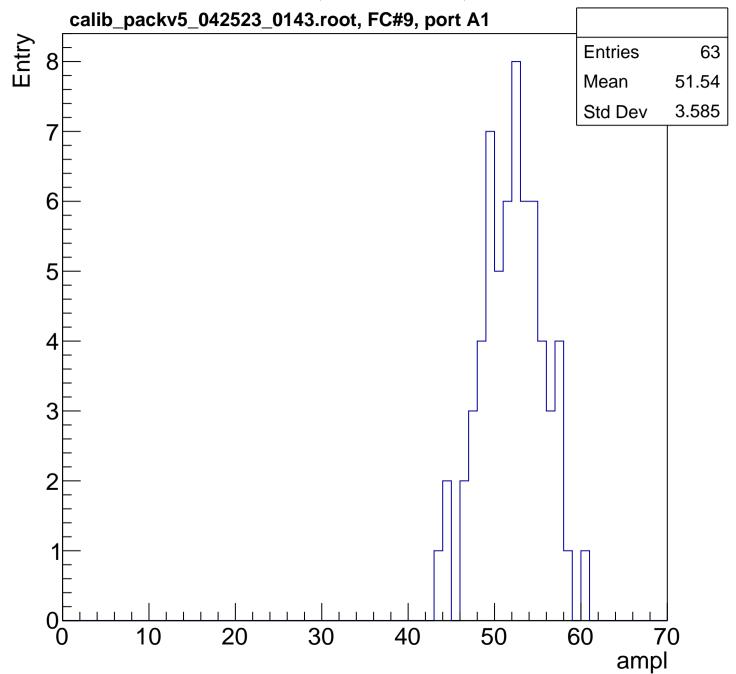


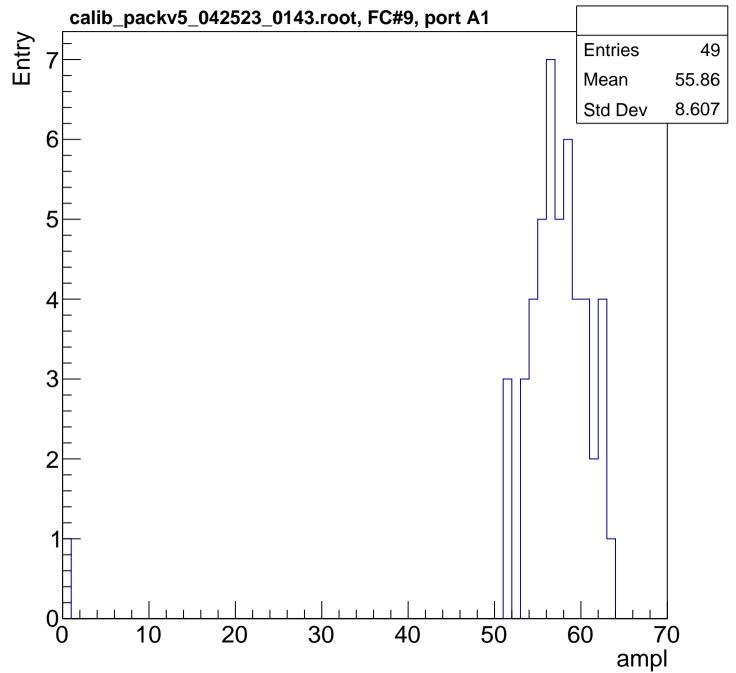


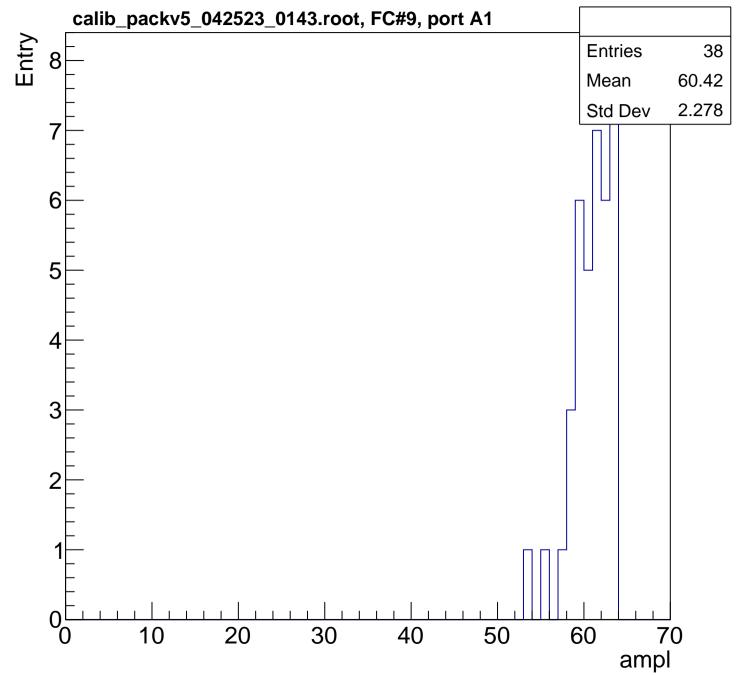


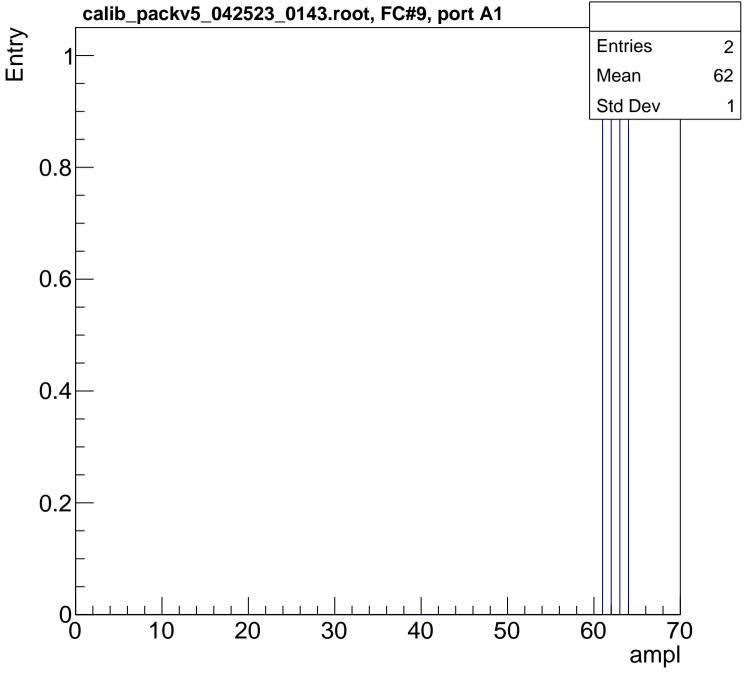


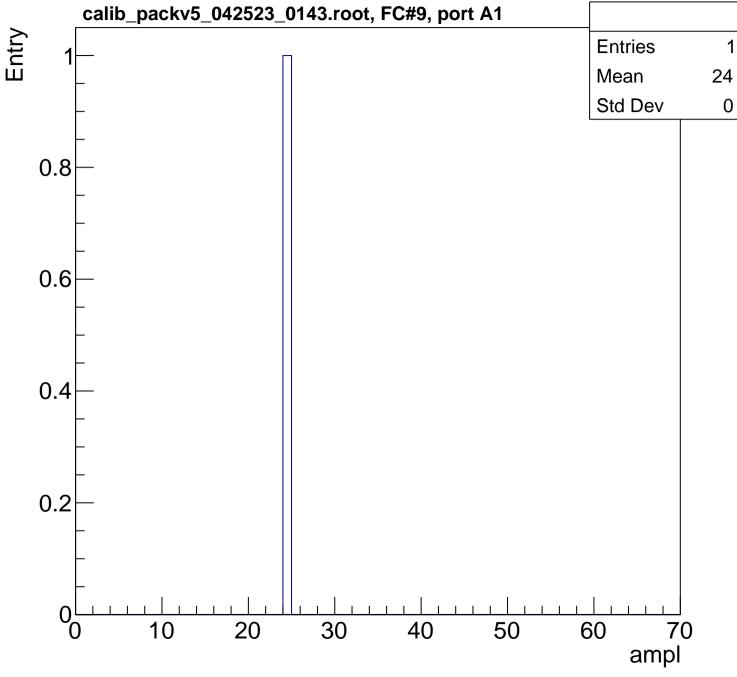


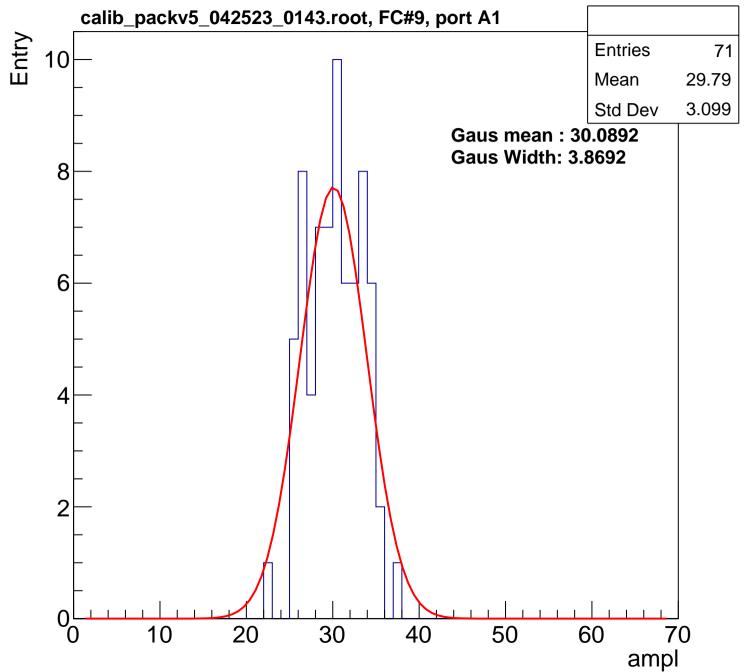


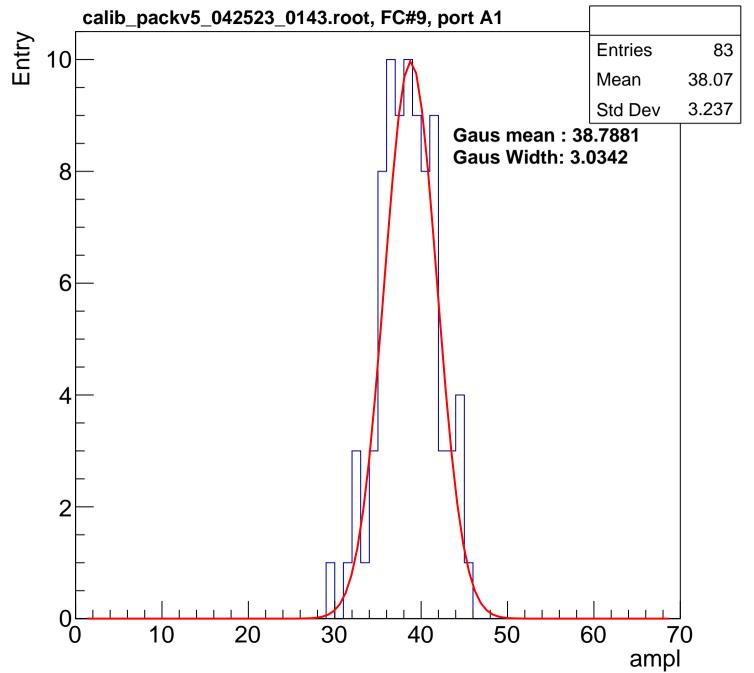


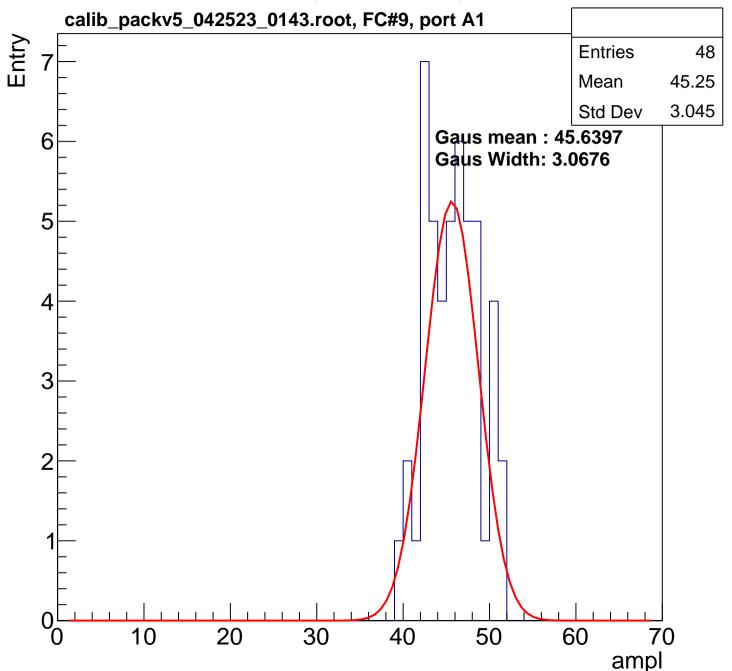


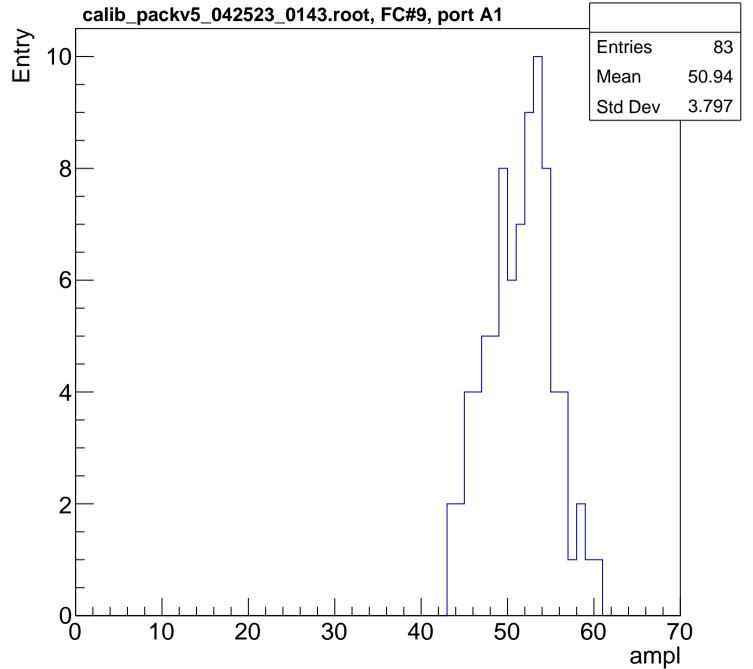


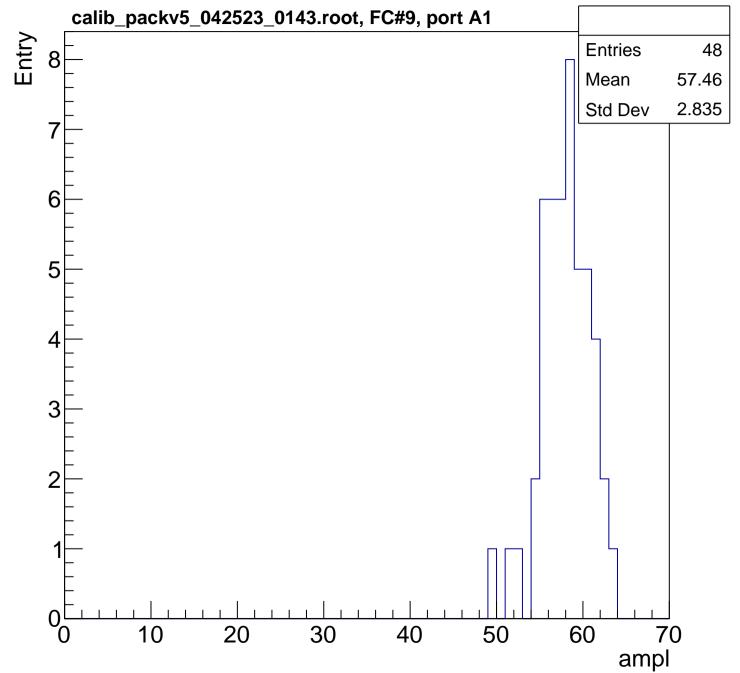


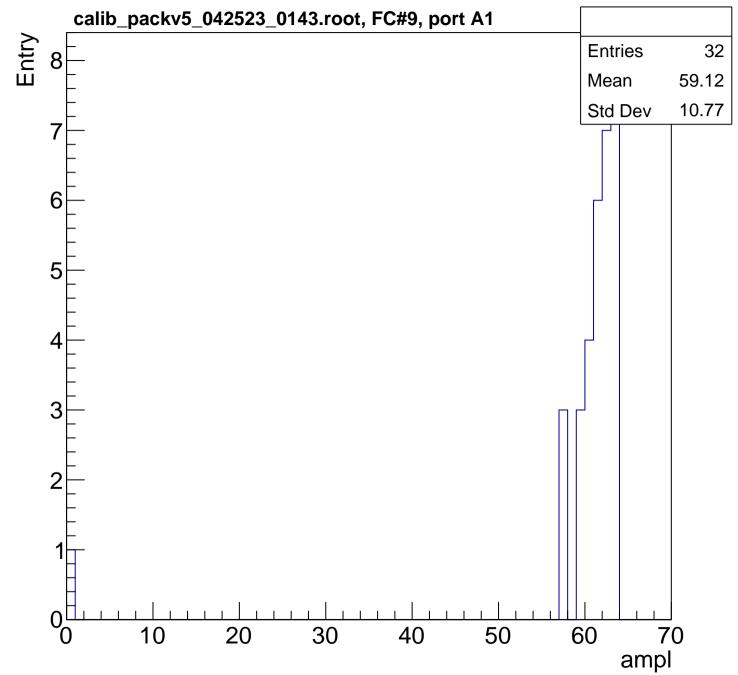


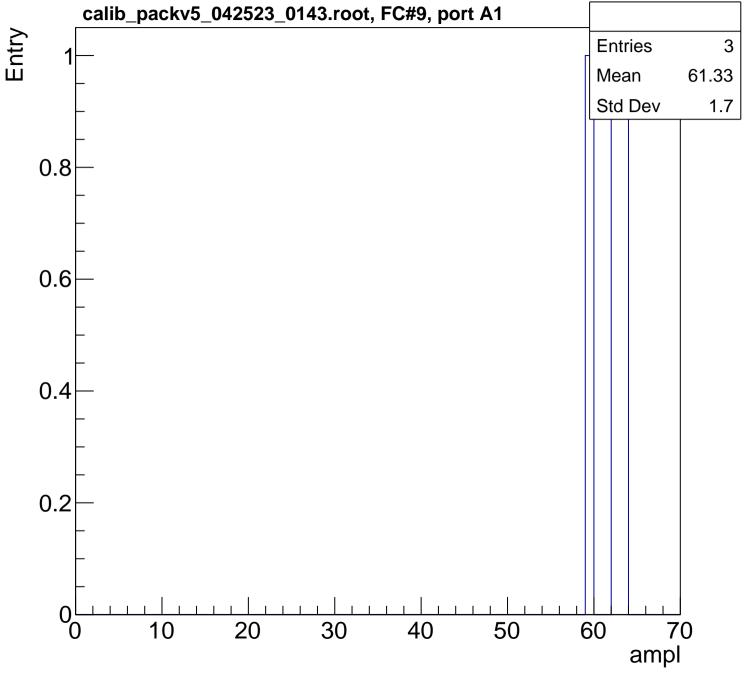




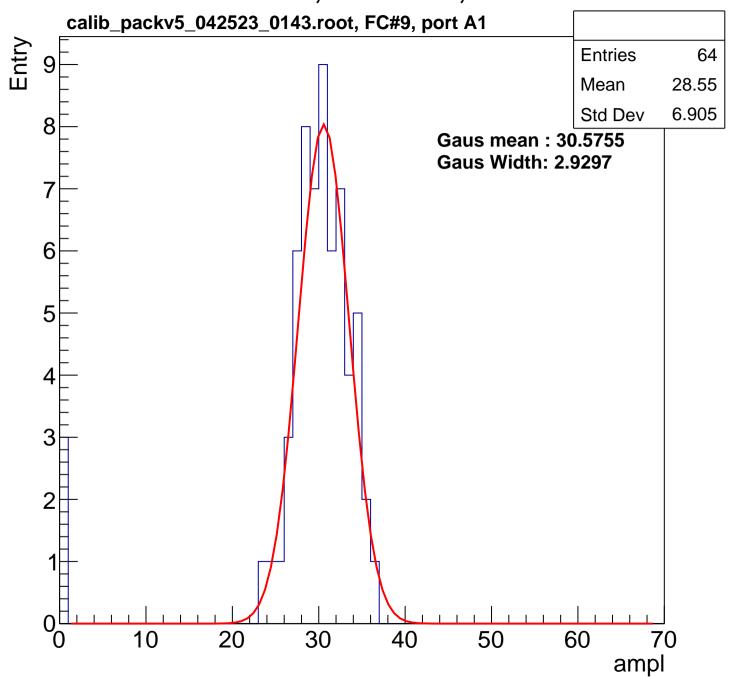


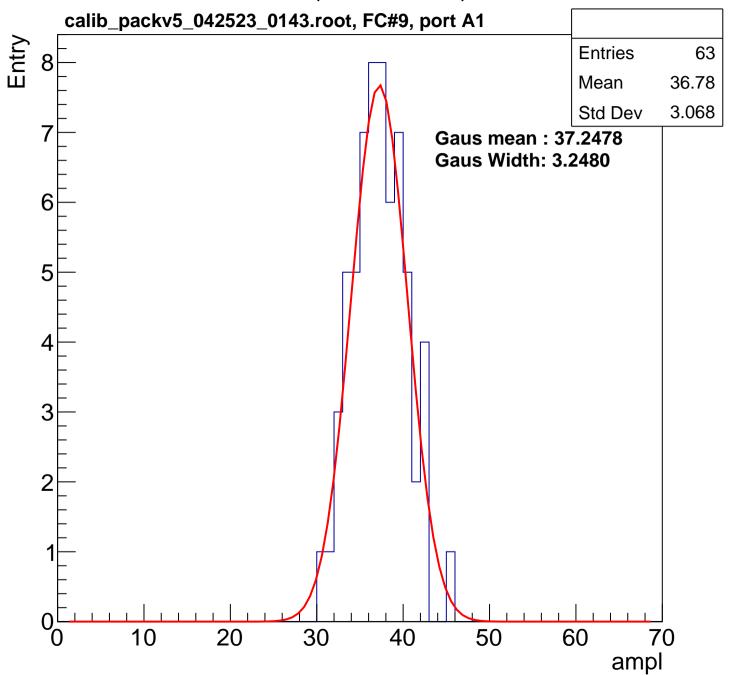


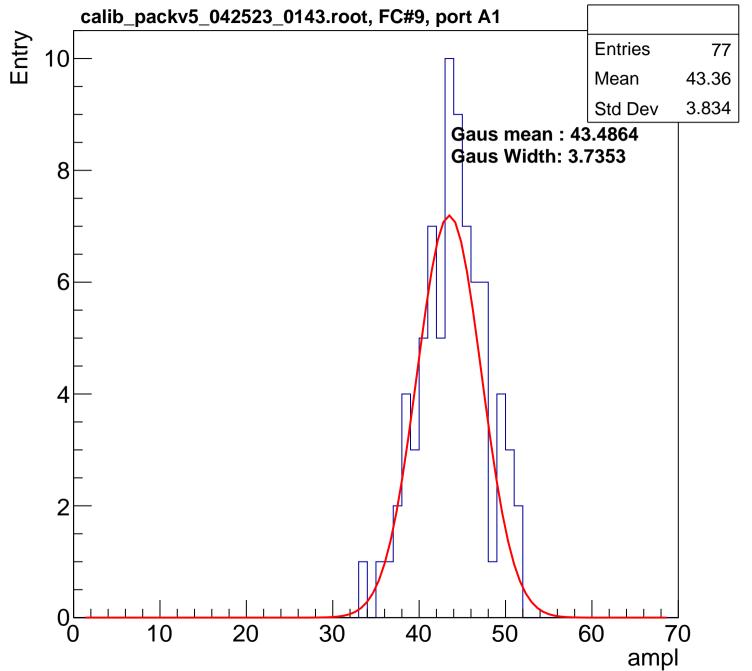


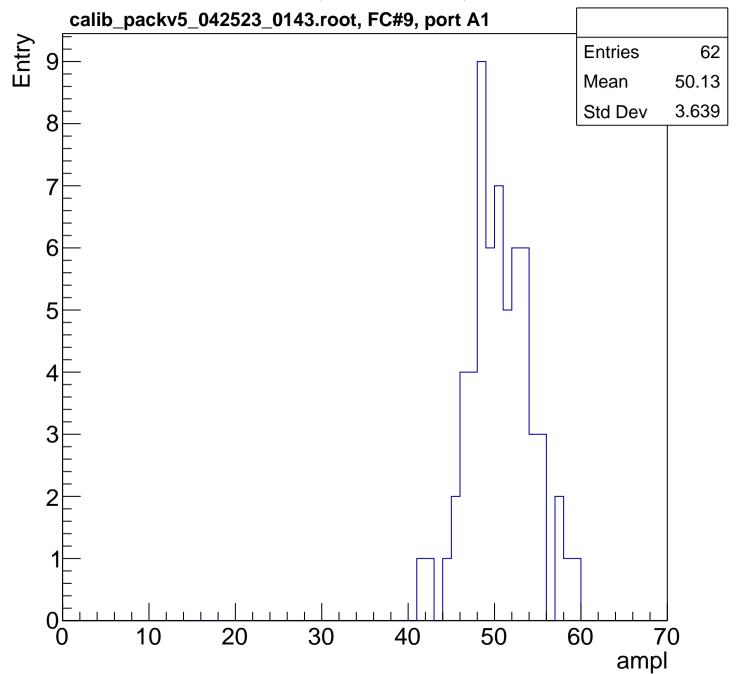


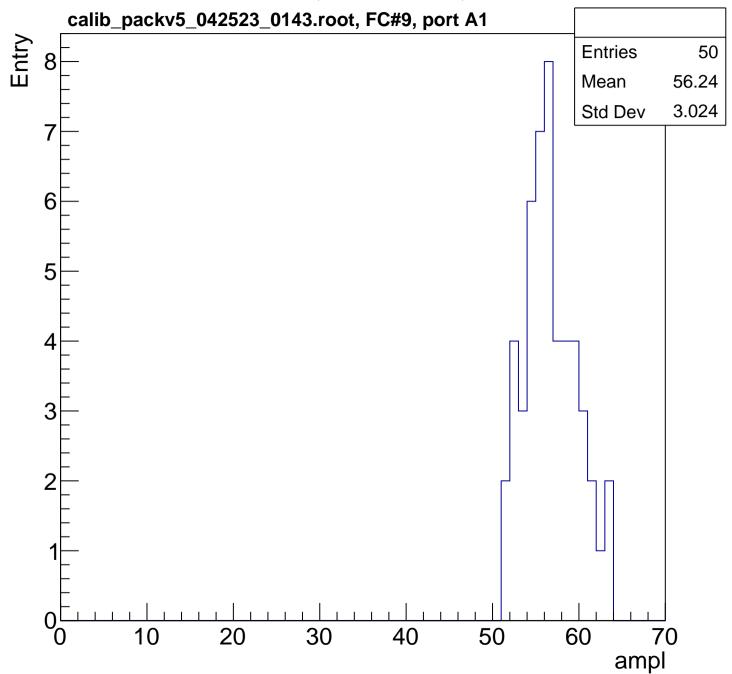


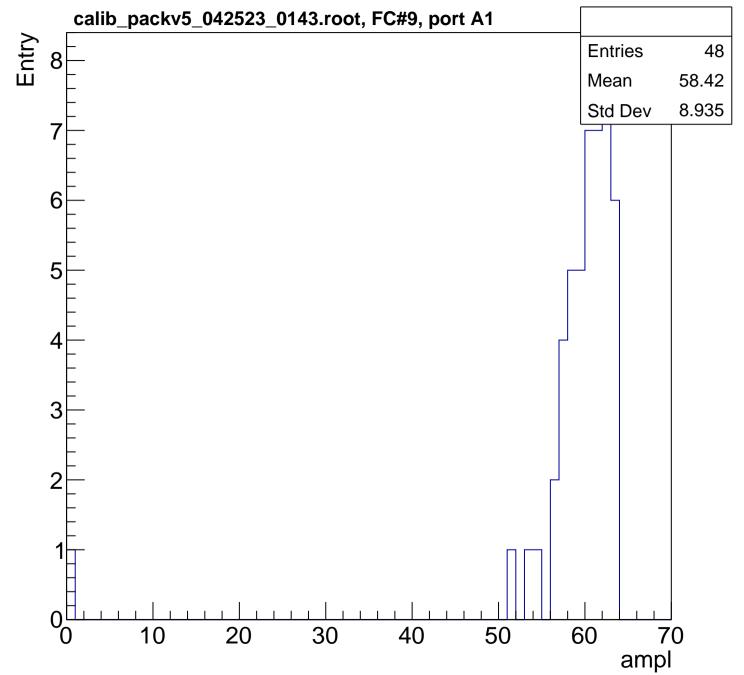


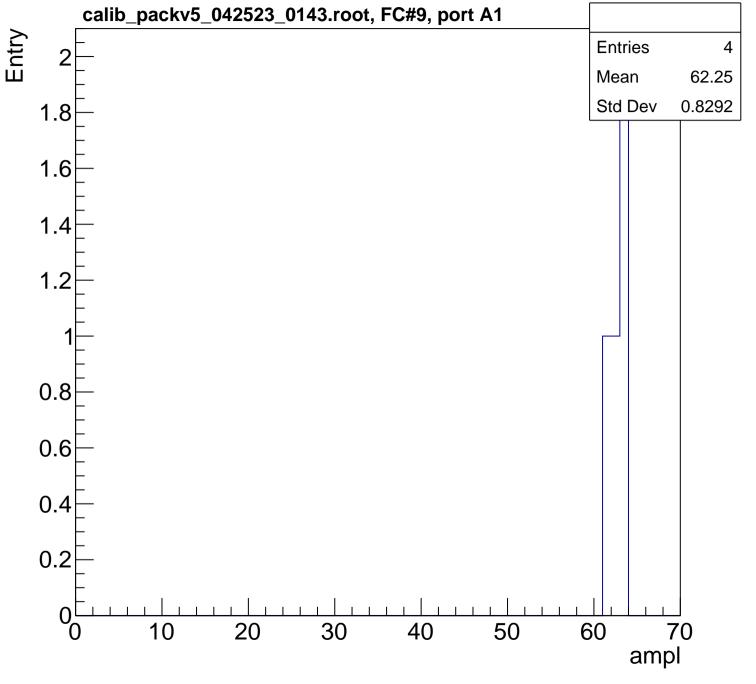












B0L001S, U3-ch38, adc7 calib_packv5_042523_0143.root, FC#9, port A1 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2

30

40

50

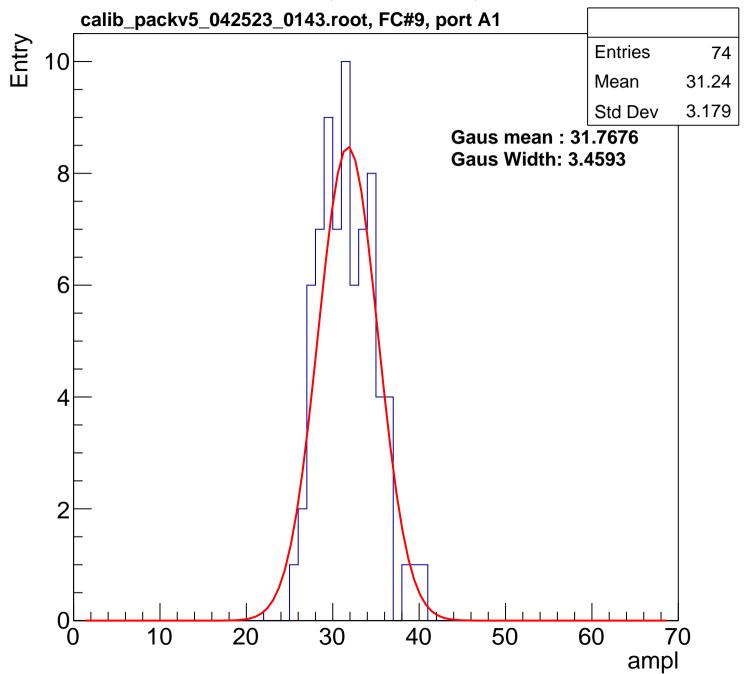
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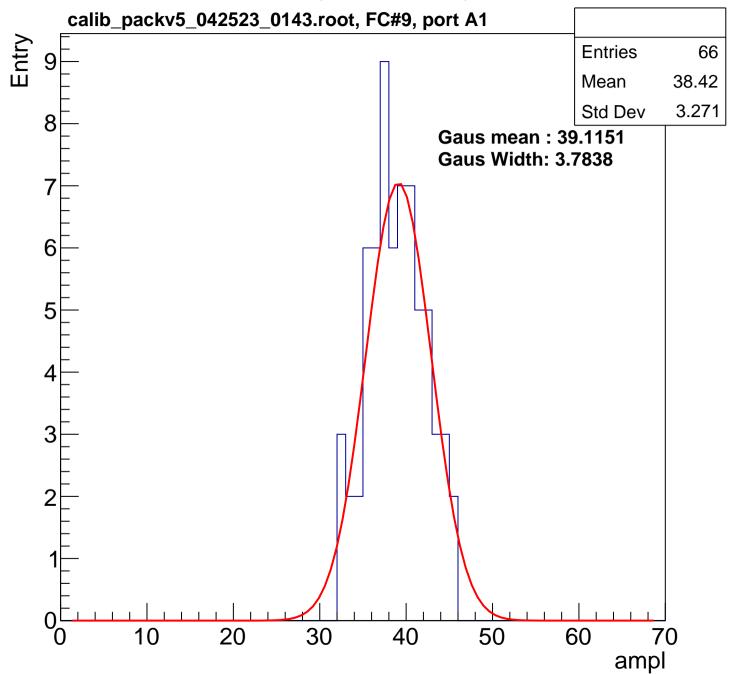
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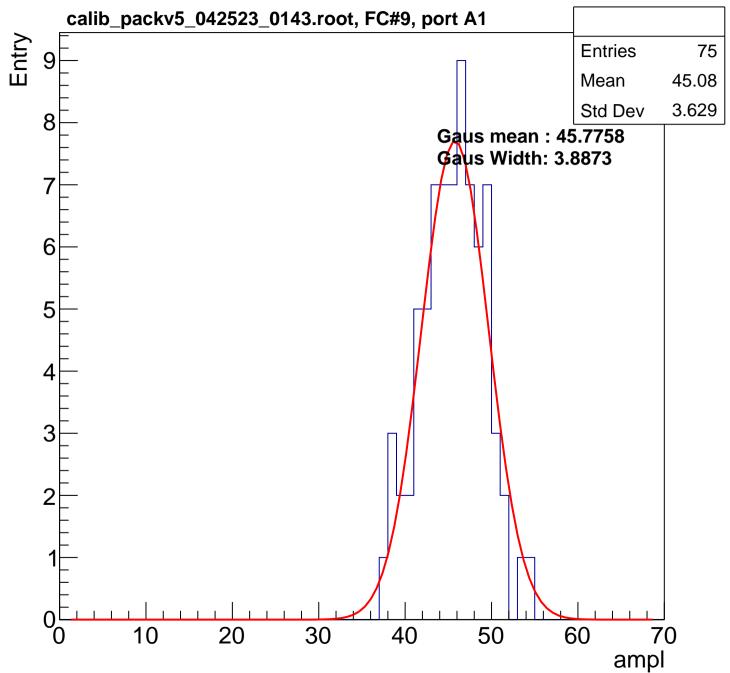
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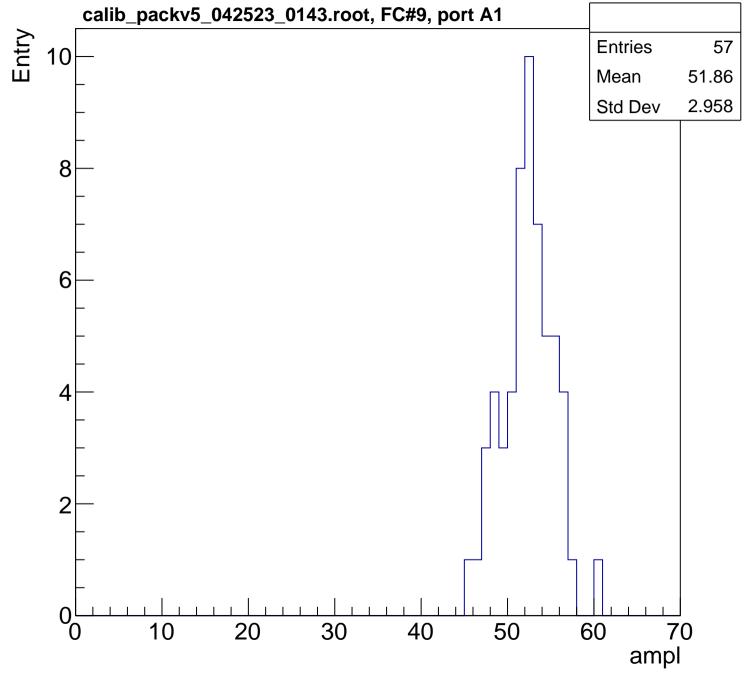
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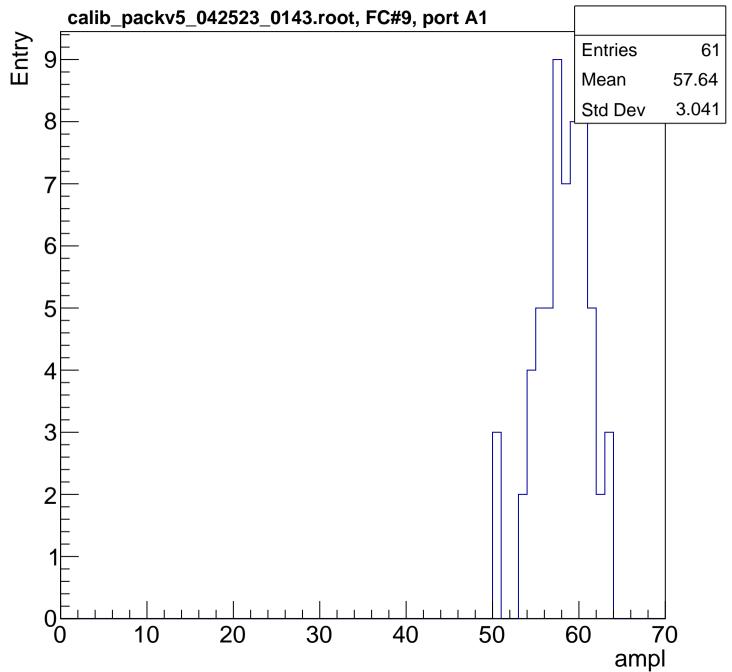
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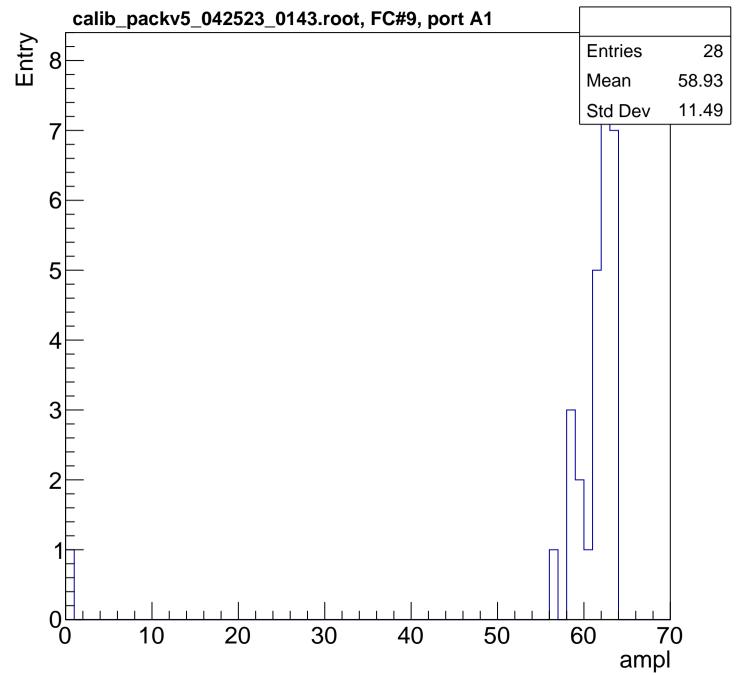


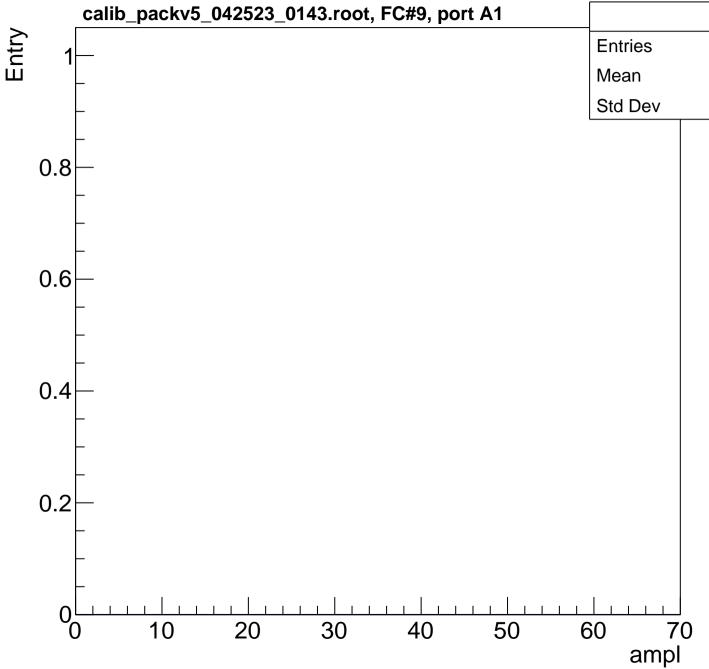




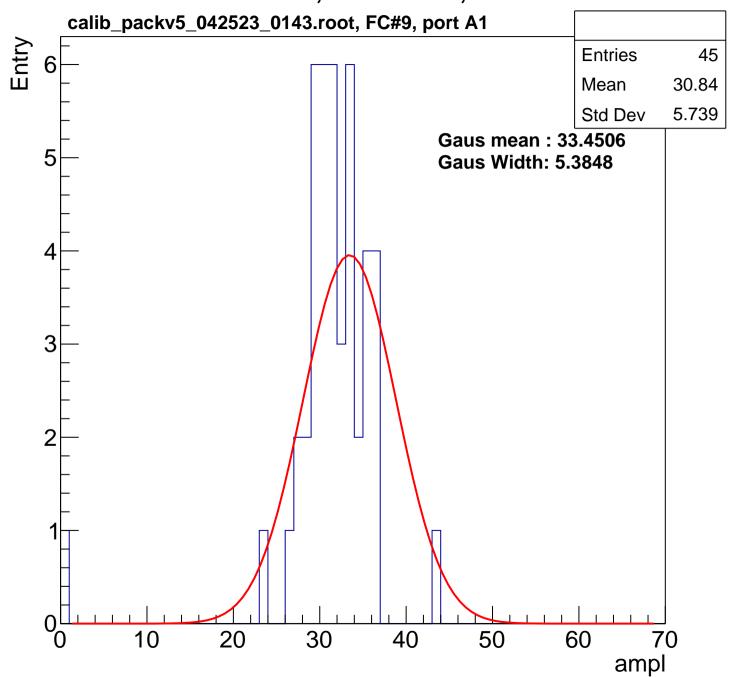


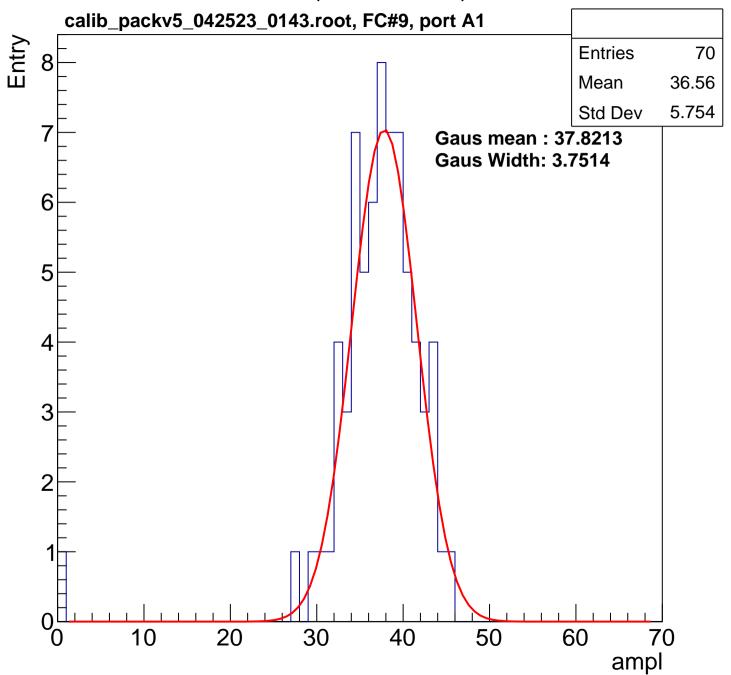


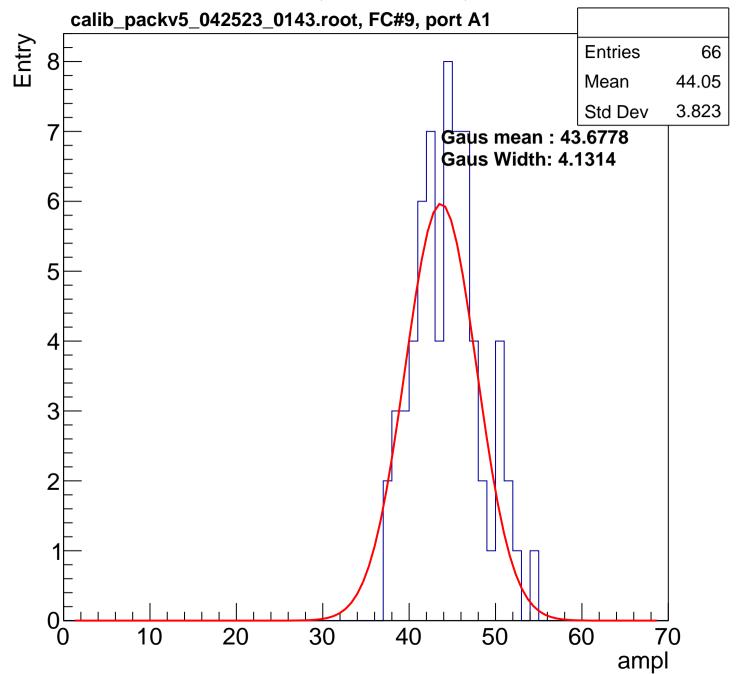


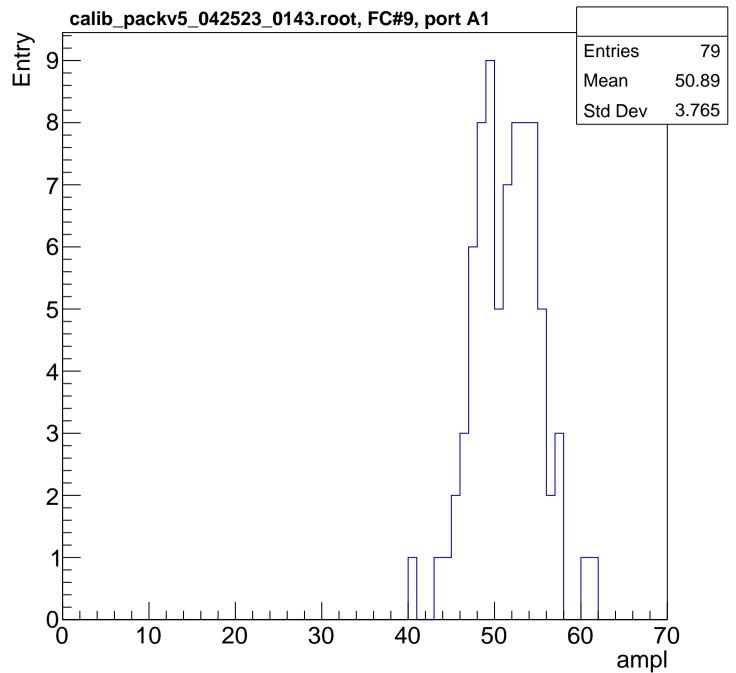


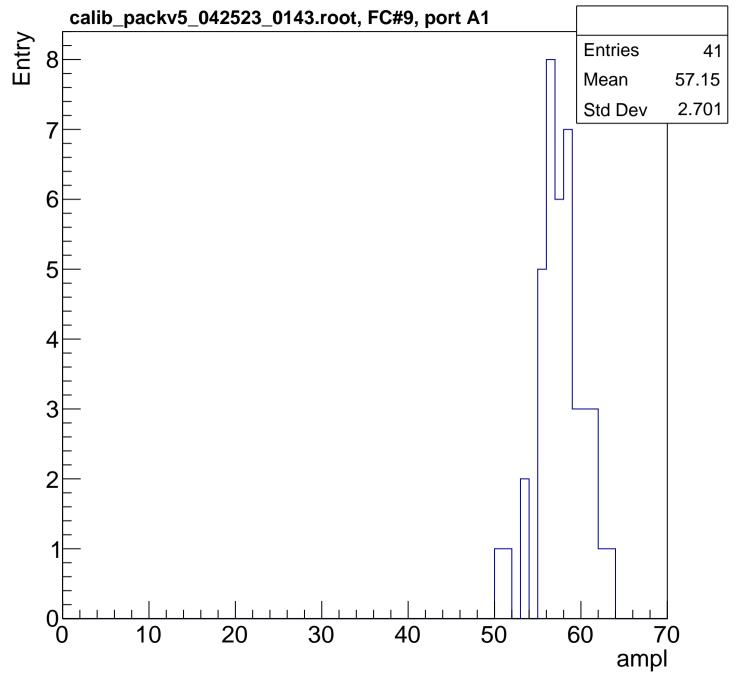


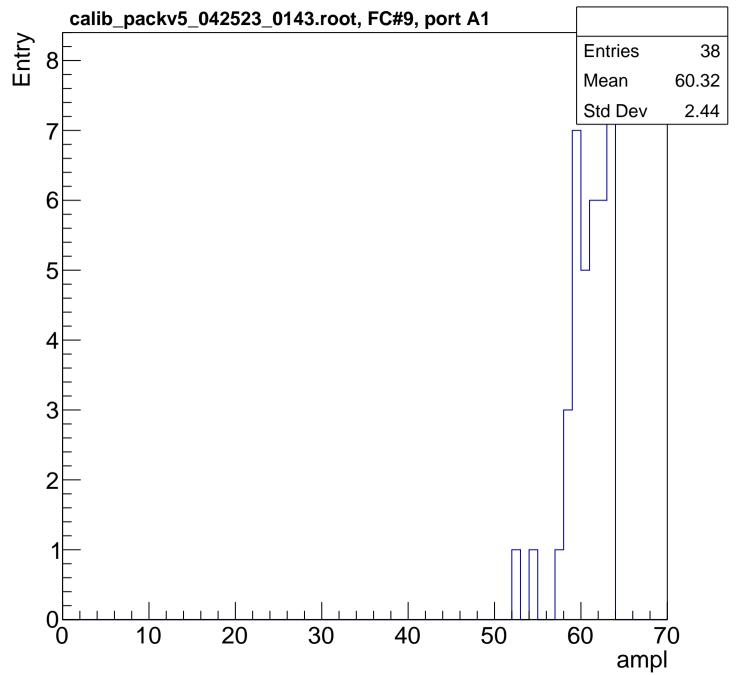


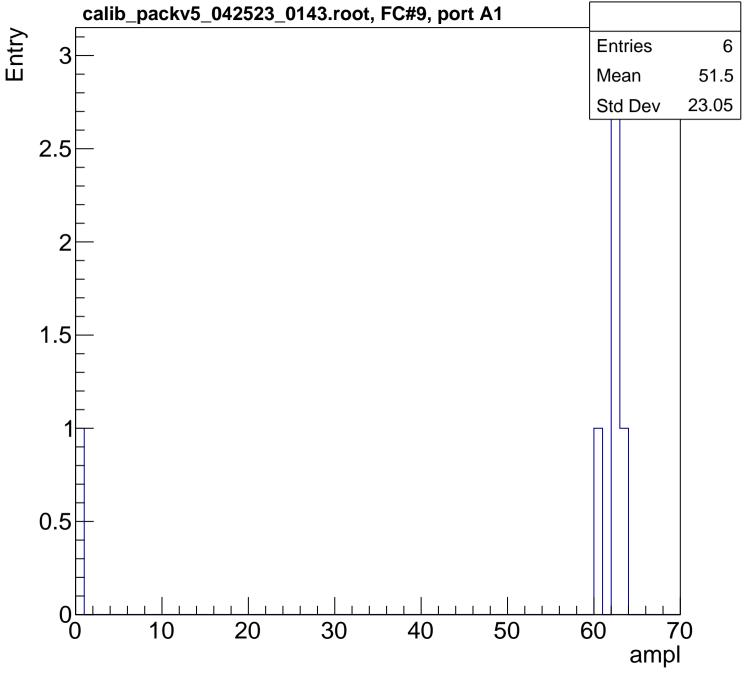




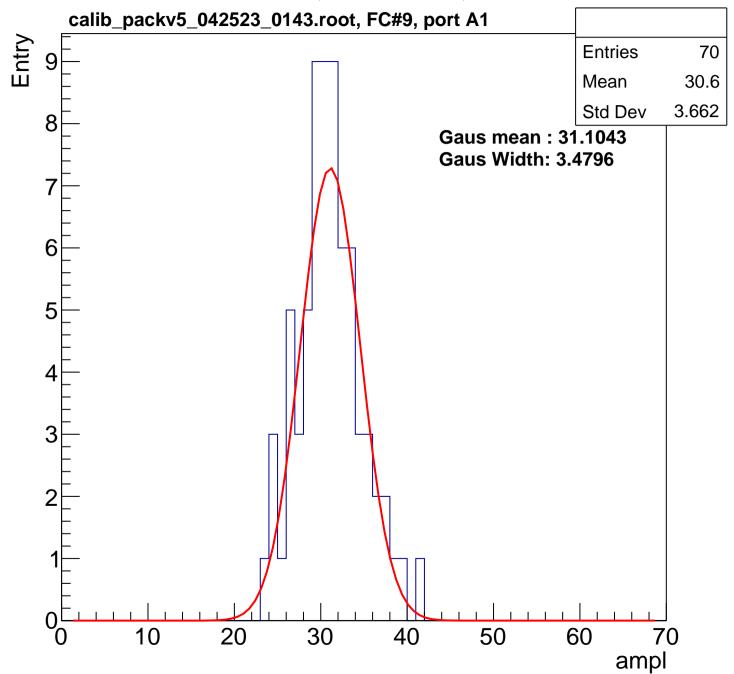


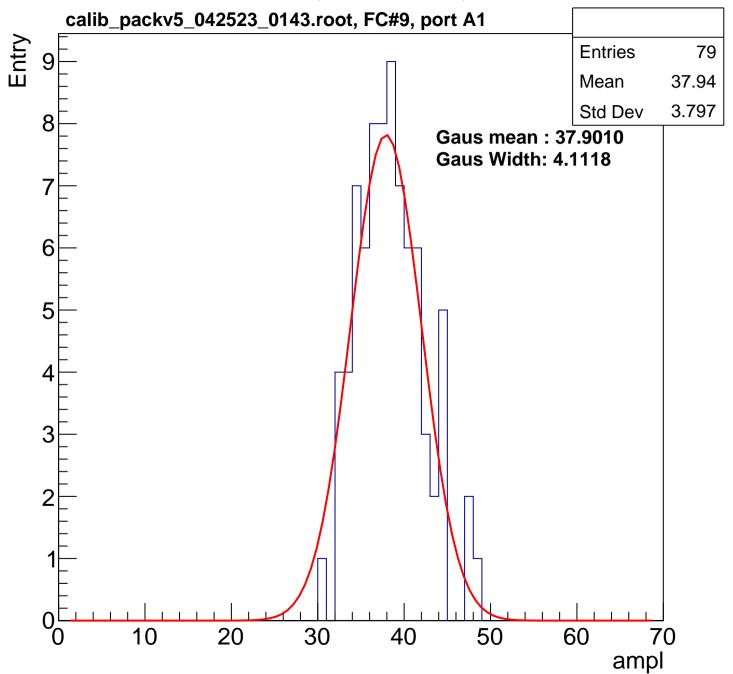


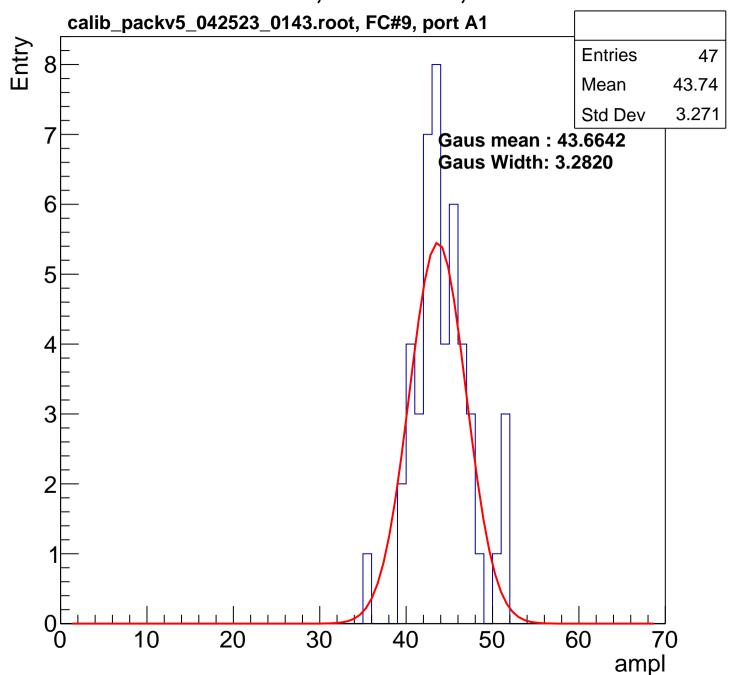


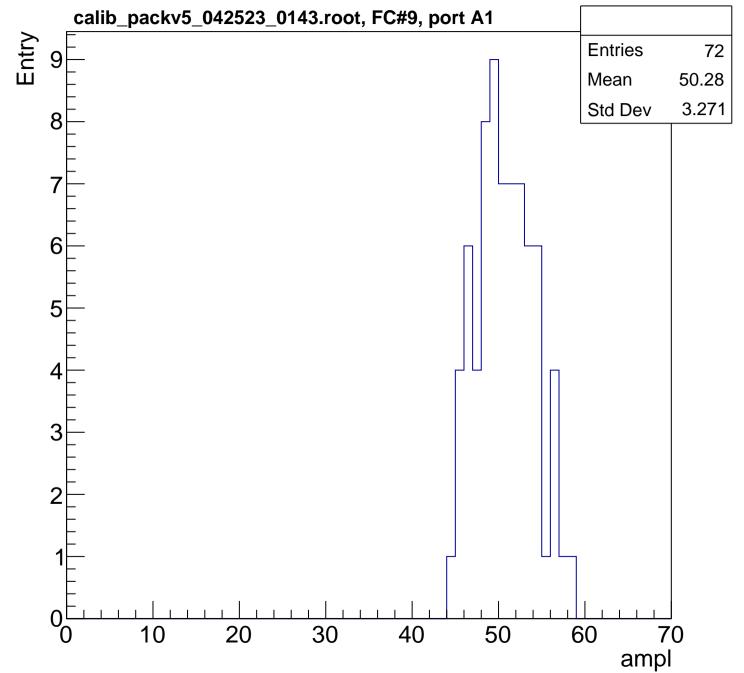


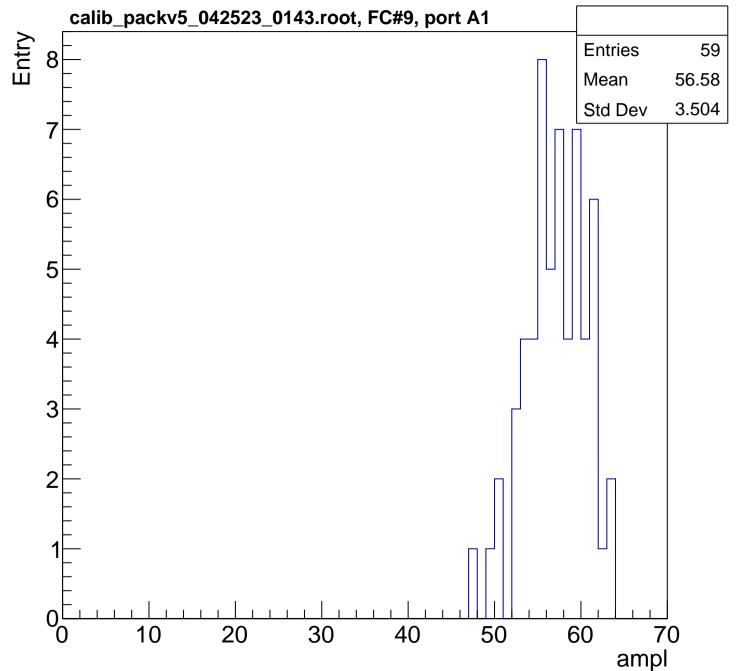
B0L001S, U3-ch40, adc7 calib_packv5_042523_0143.root, FC#9, port A1 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

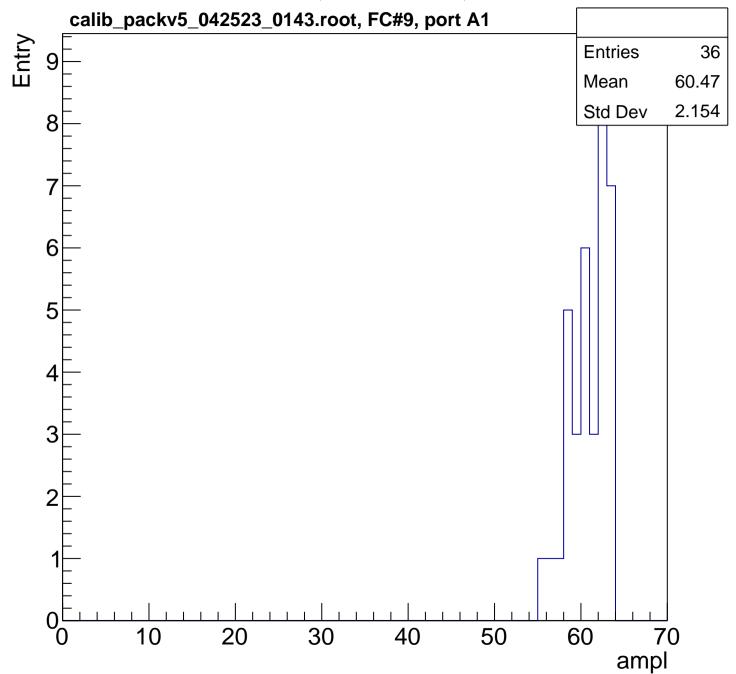


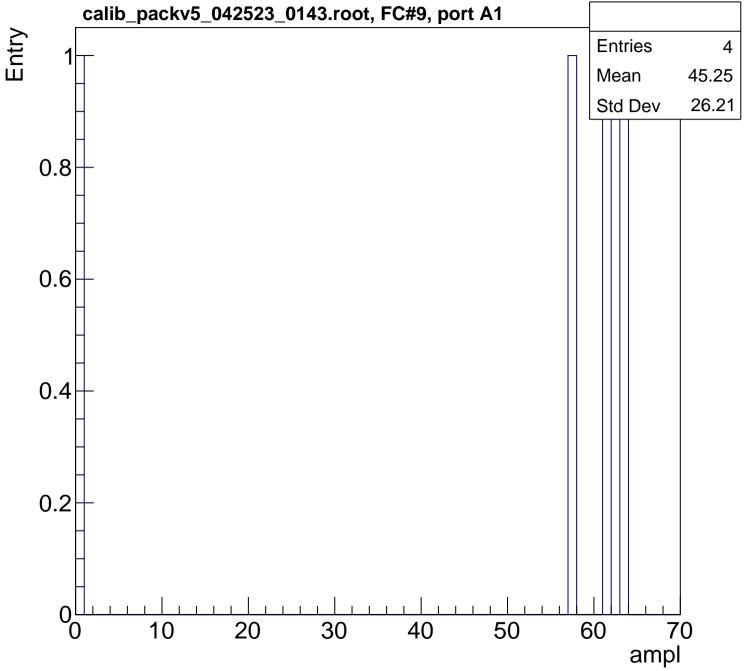


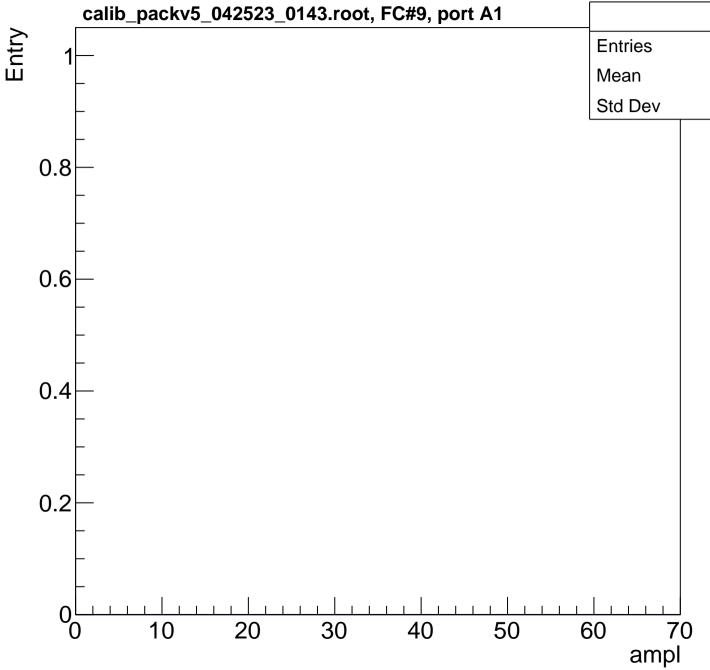


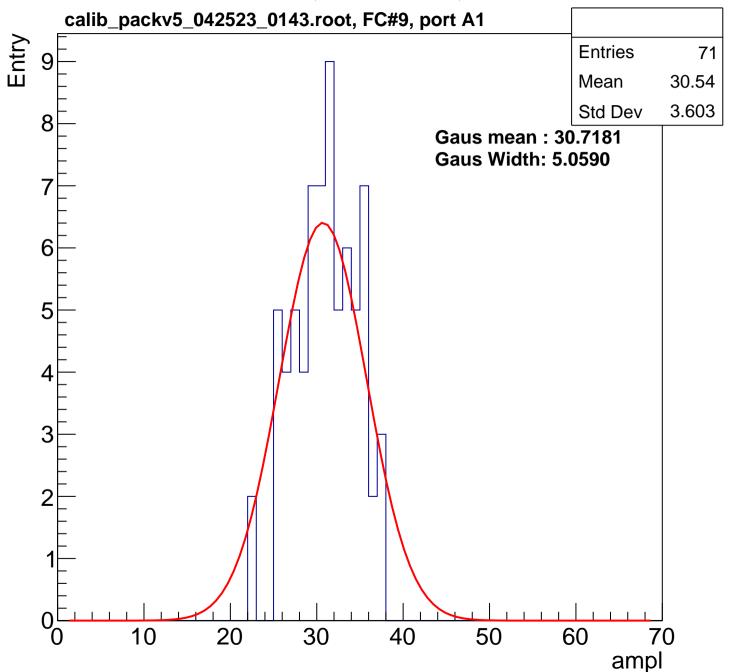


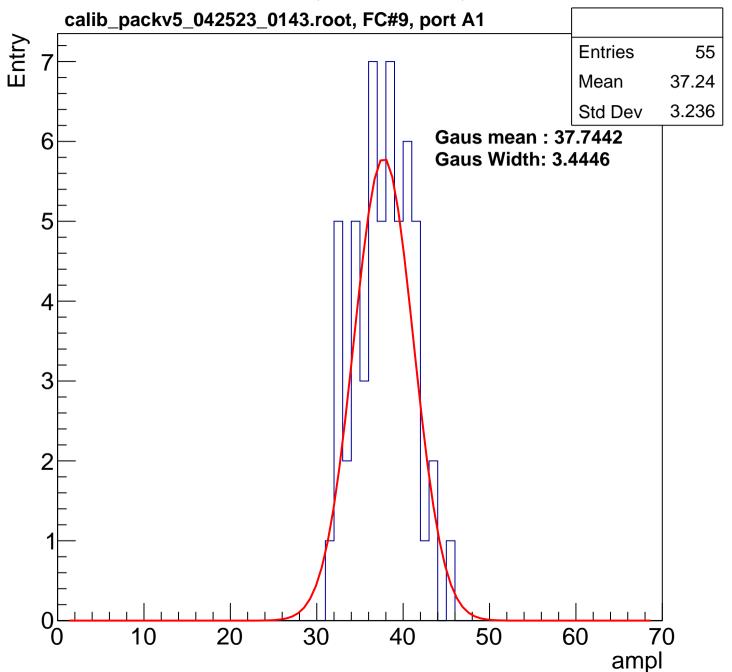


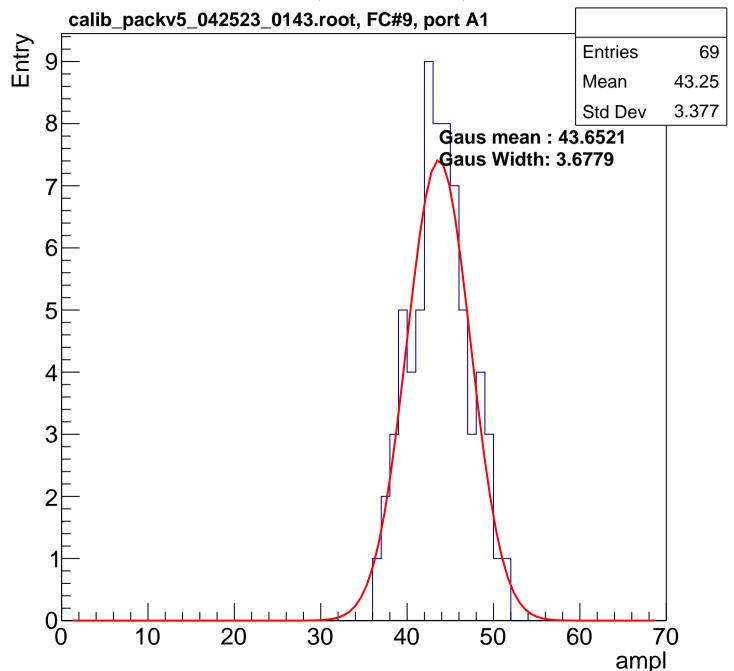


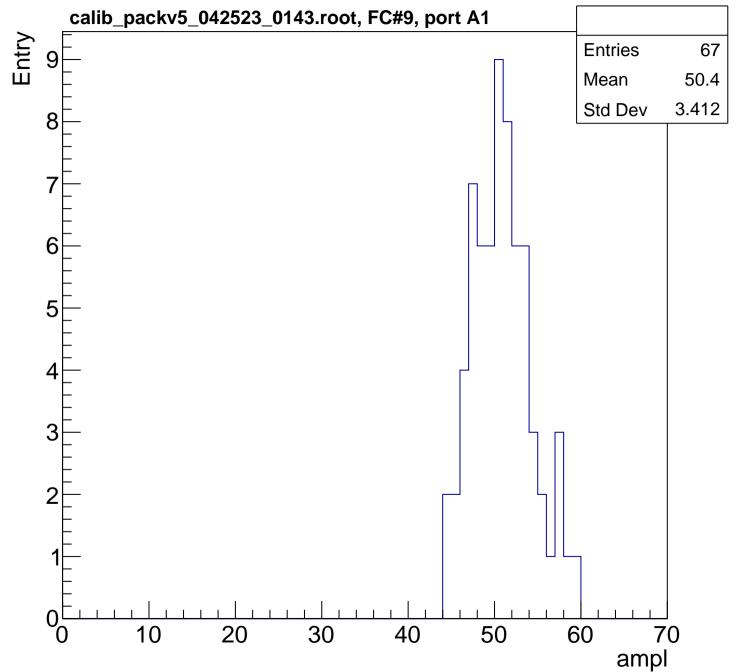


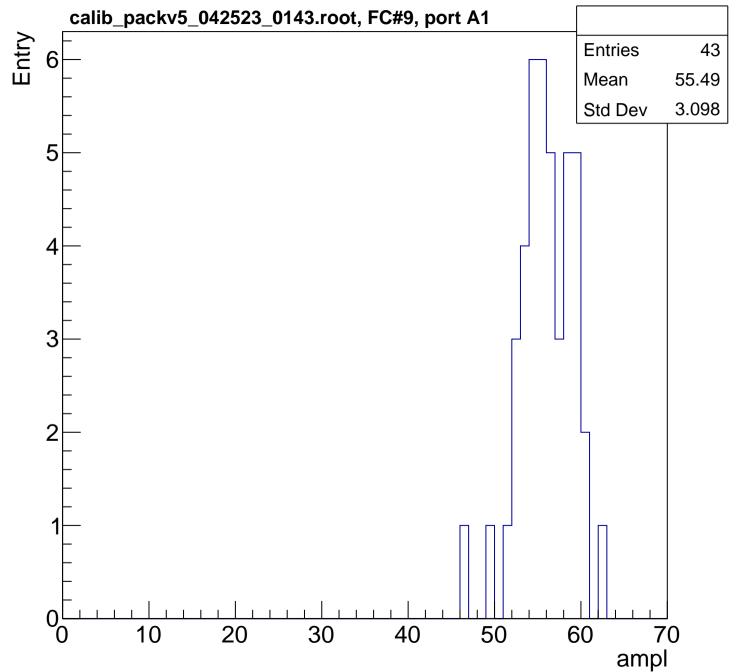


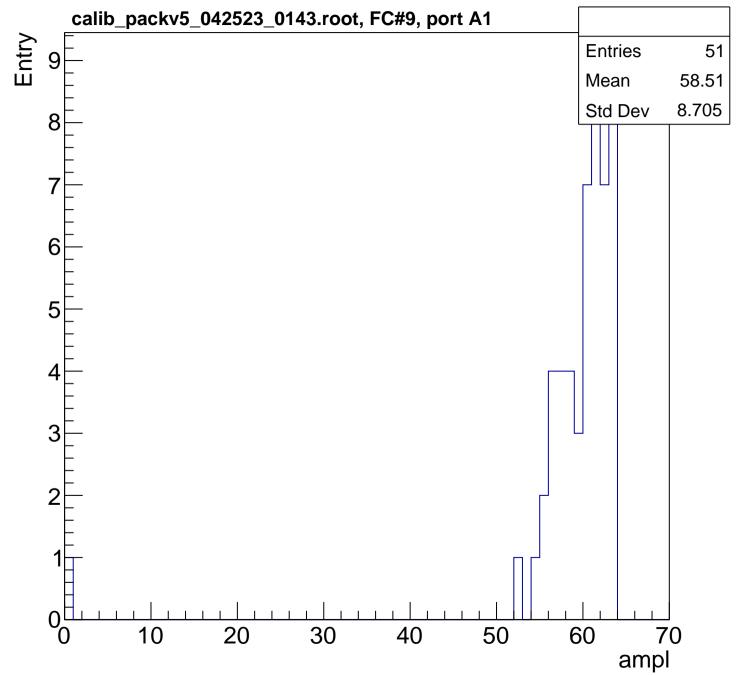


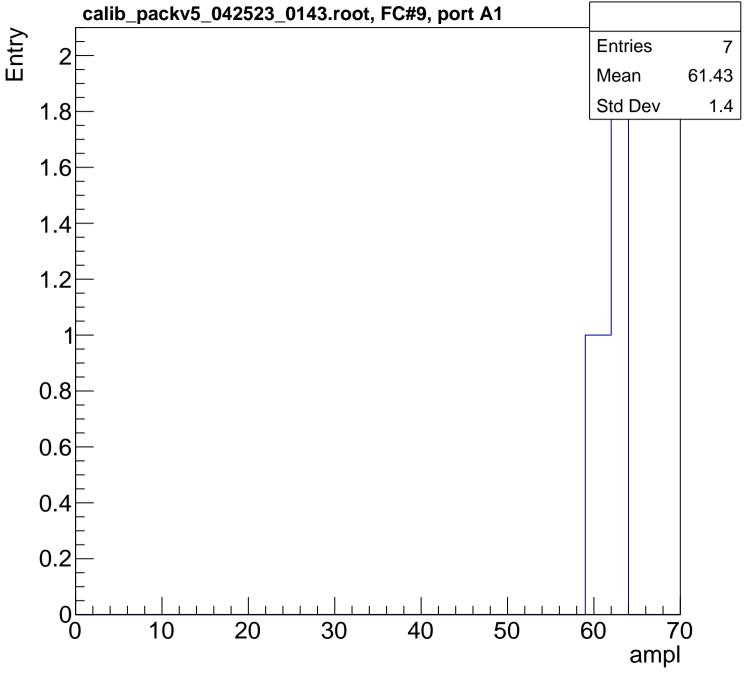






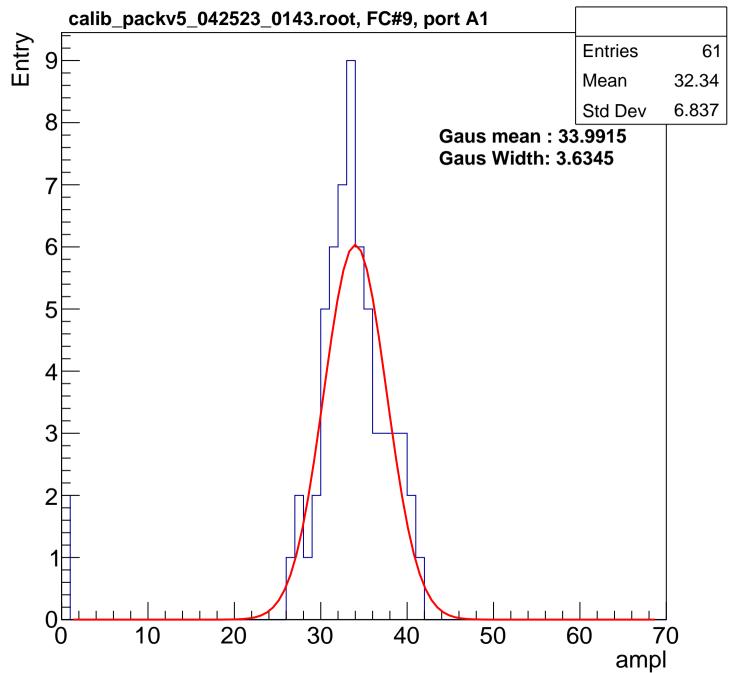


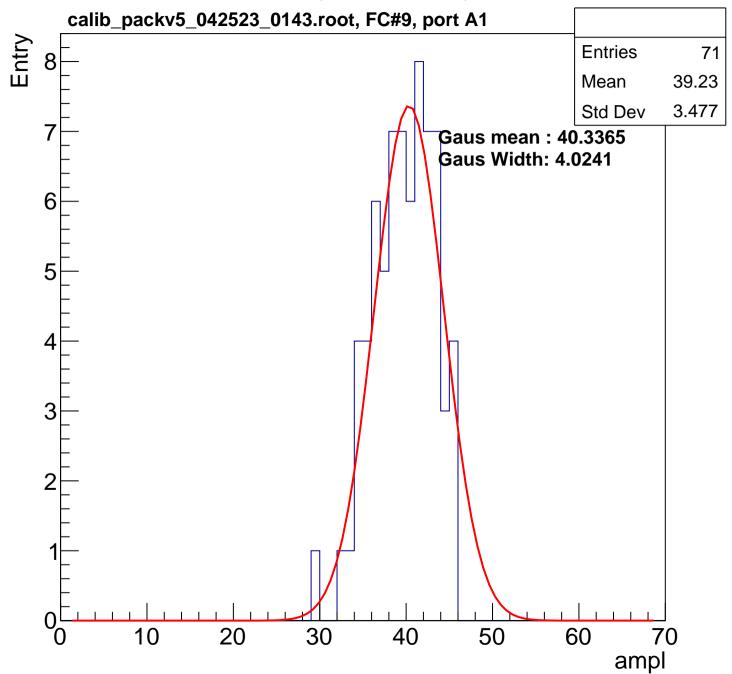


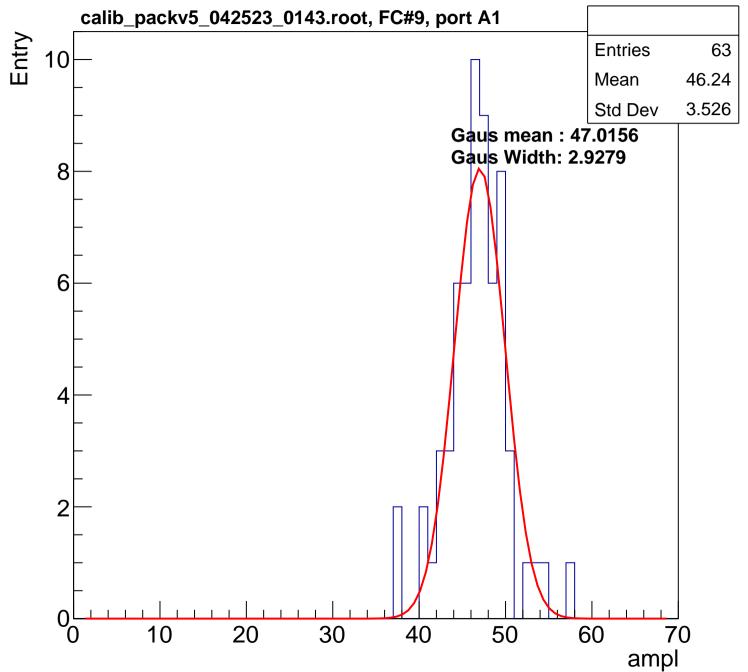


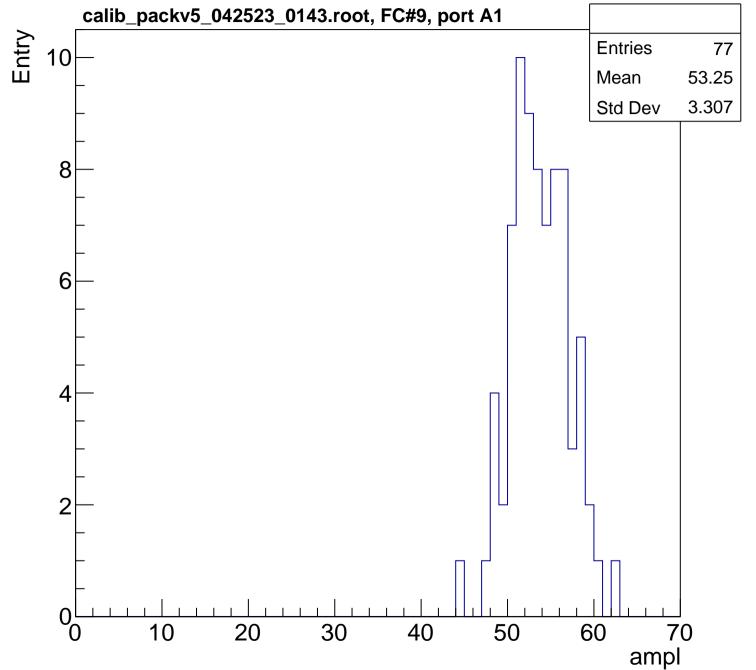
B0L001S, U3-ch42, adc7 calib_packv5_042523_0143.root, FC#9, port A1 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70

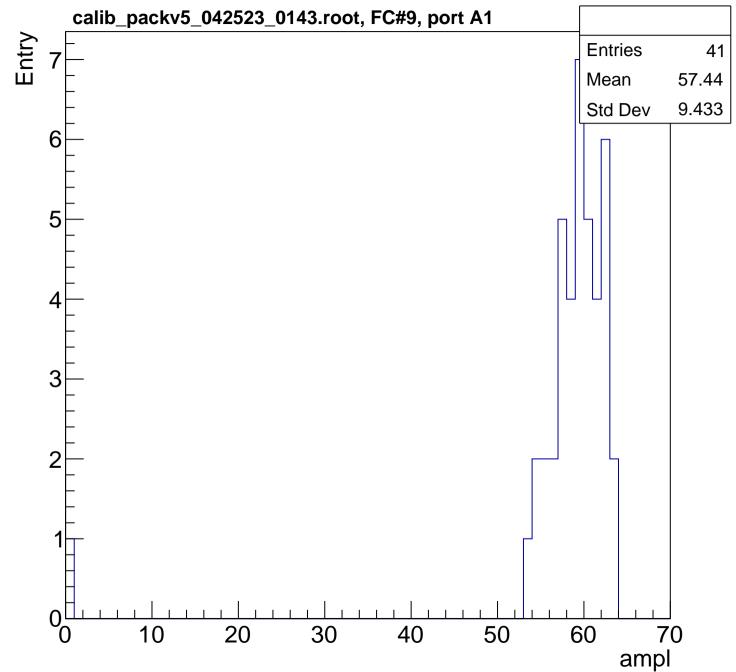
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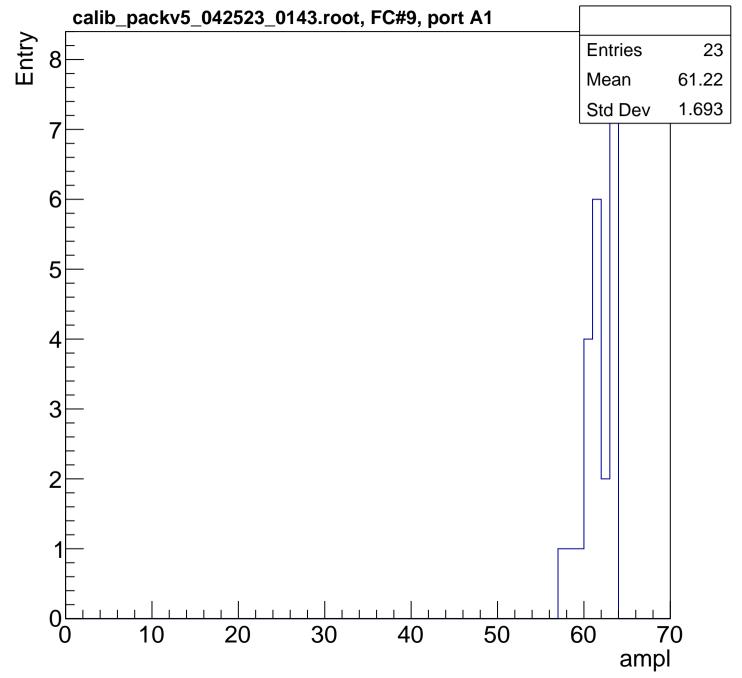




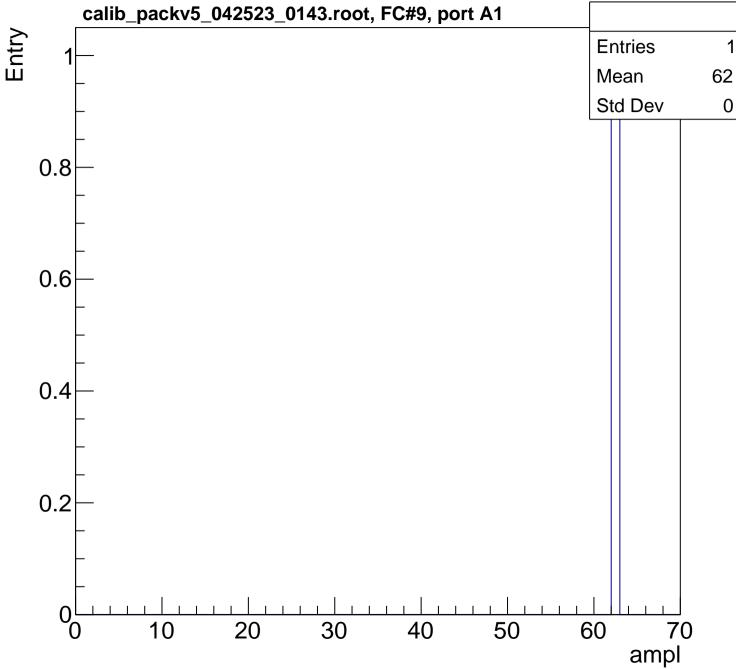




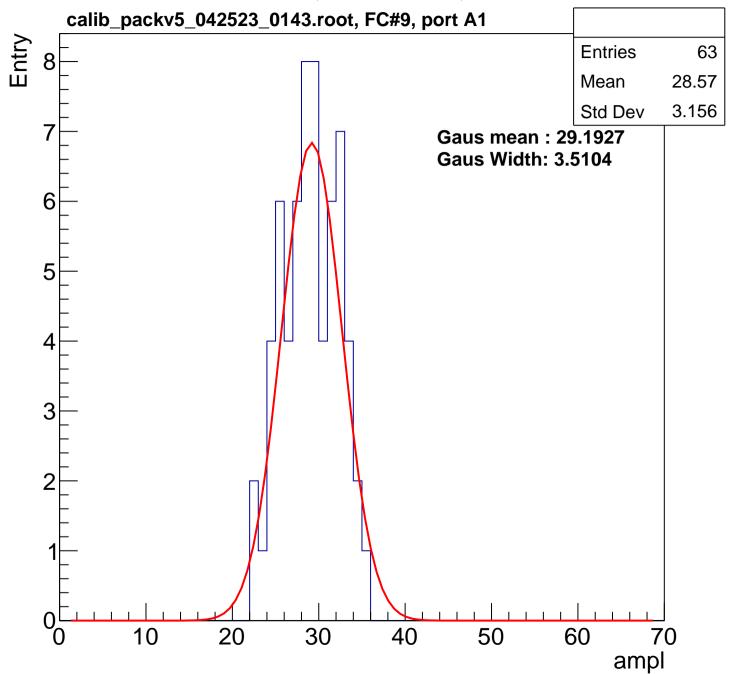


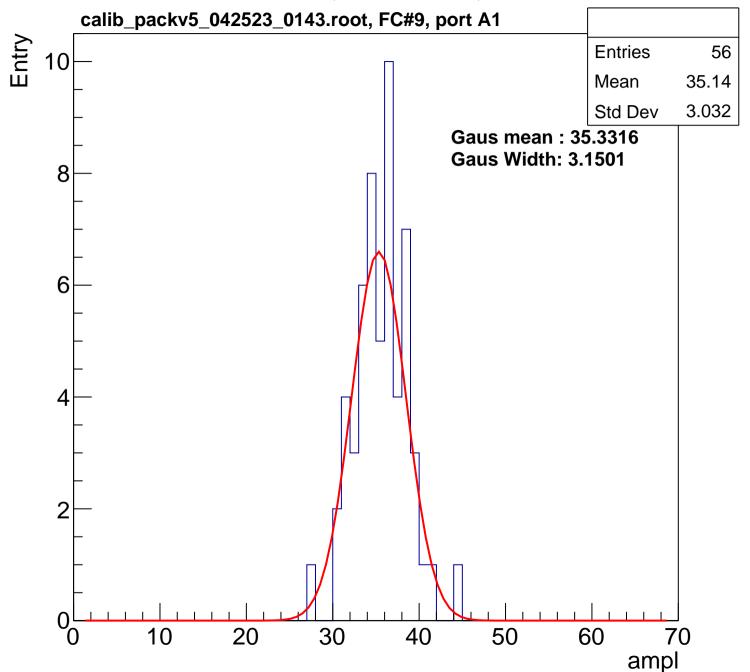


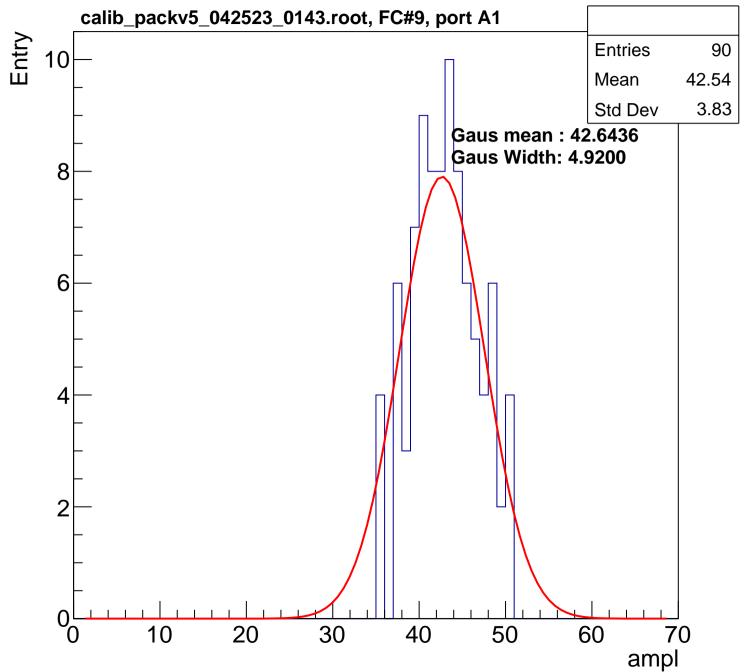
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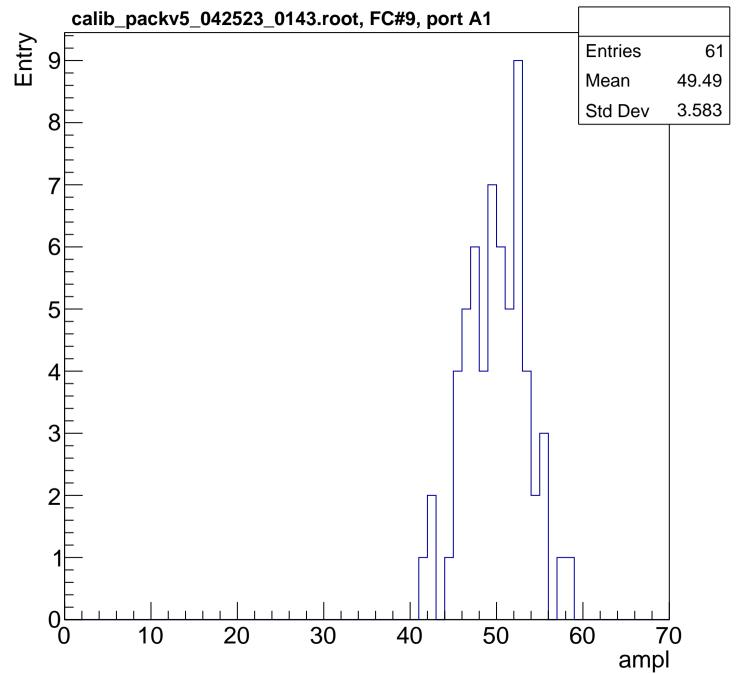


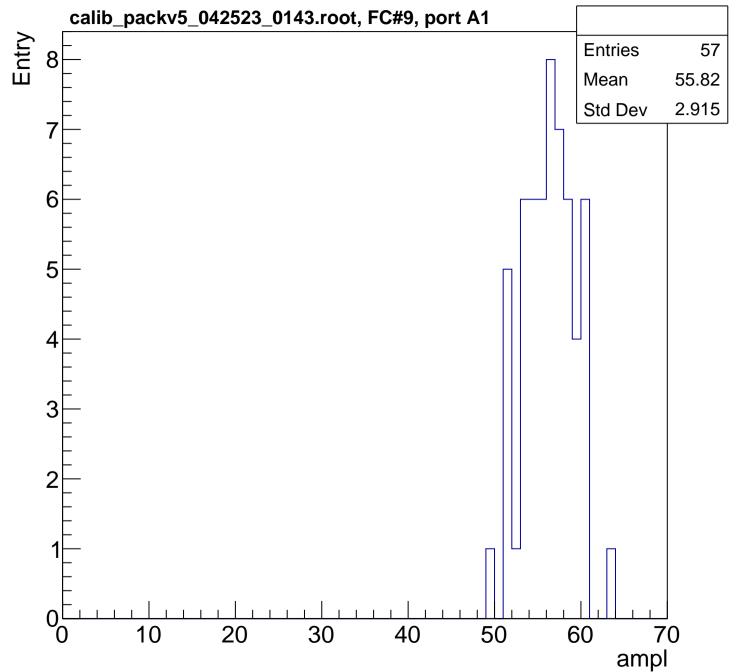
B0L001S, U3-ch43, adc7 calib_packv5_042523_0143.root, FC#9, port A1 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

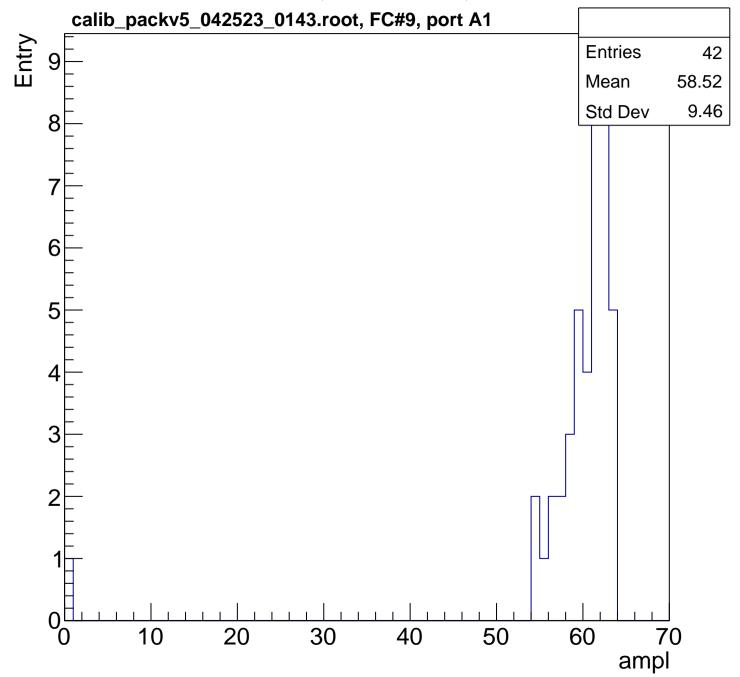


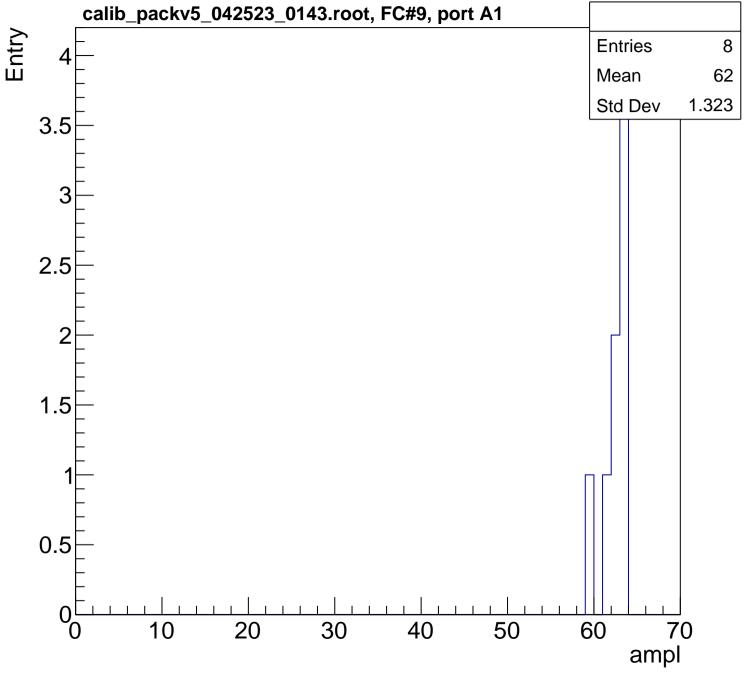


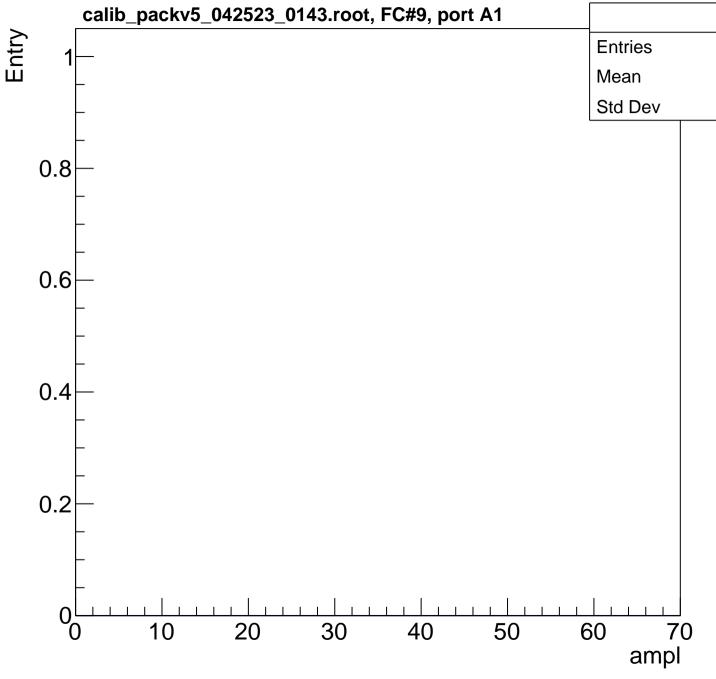


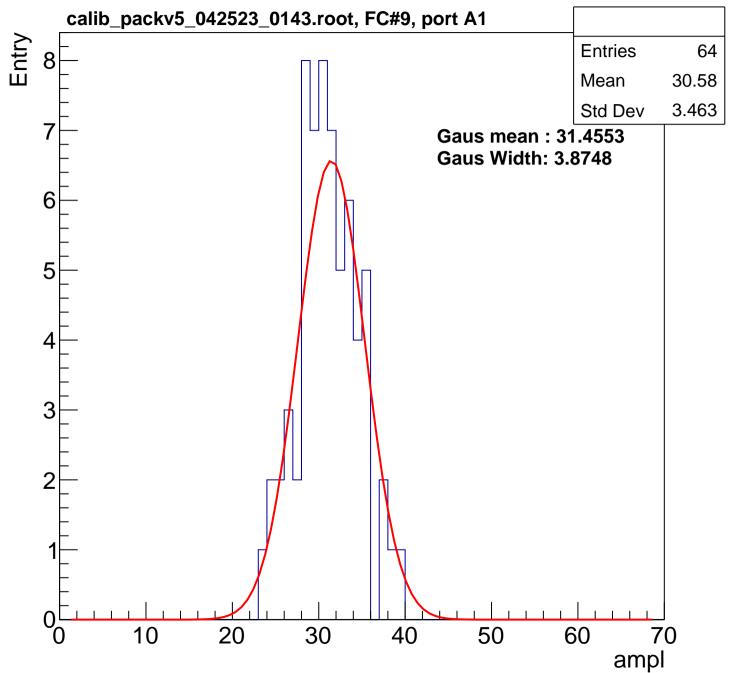


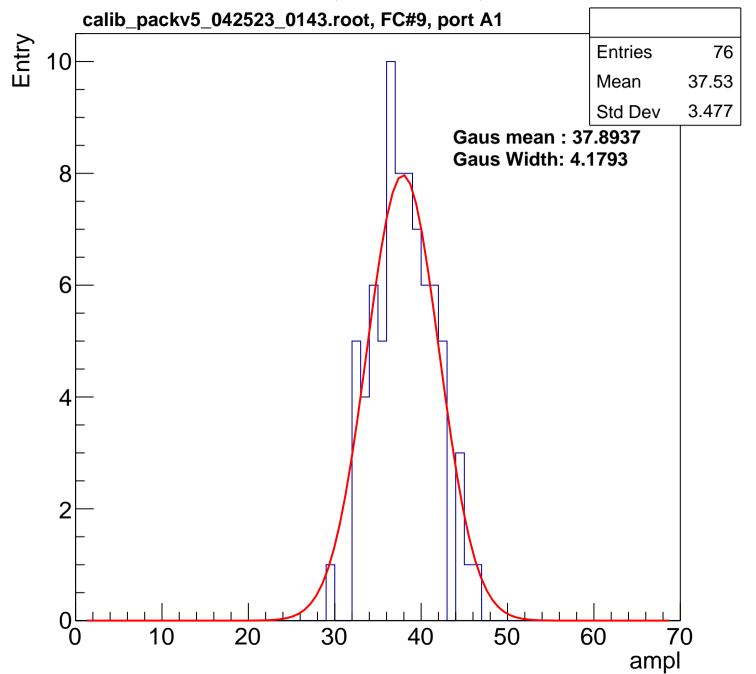


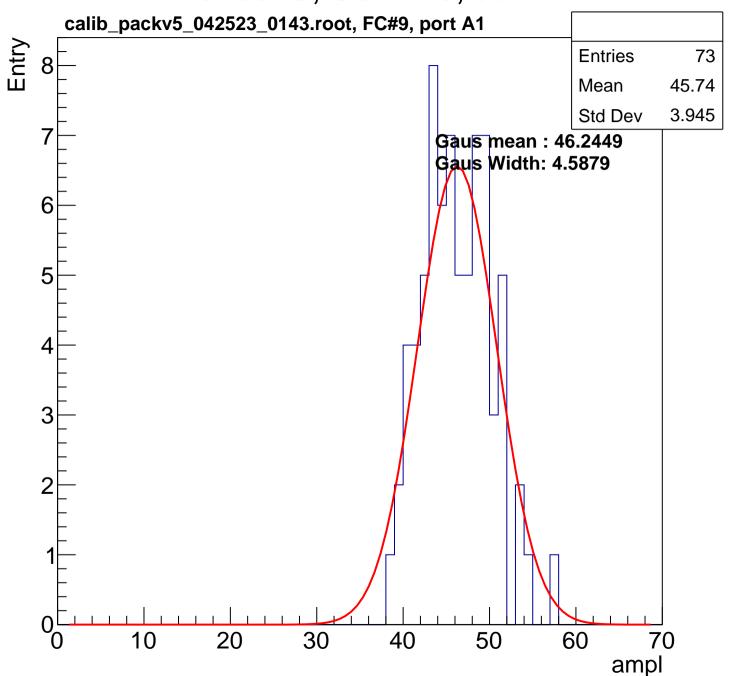


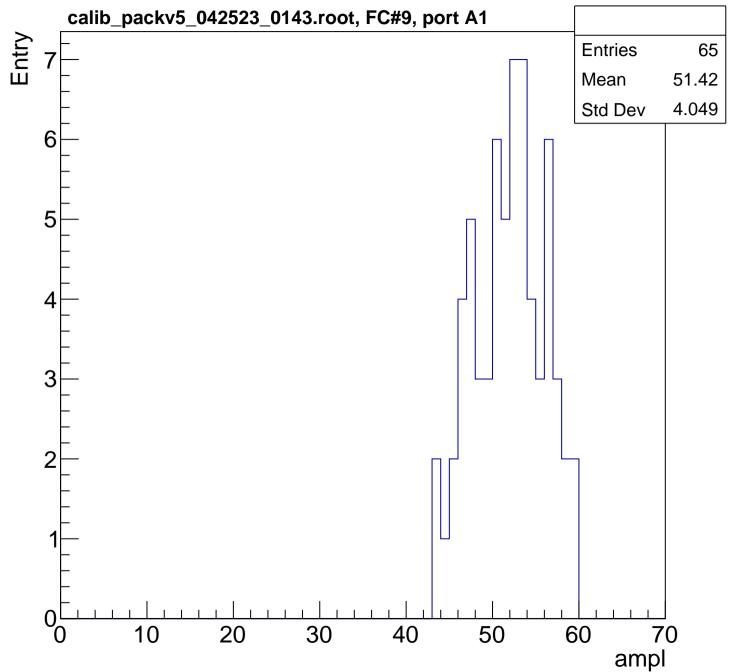


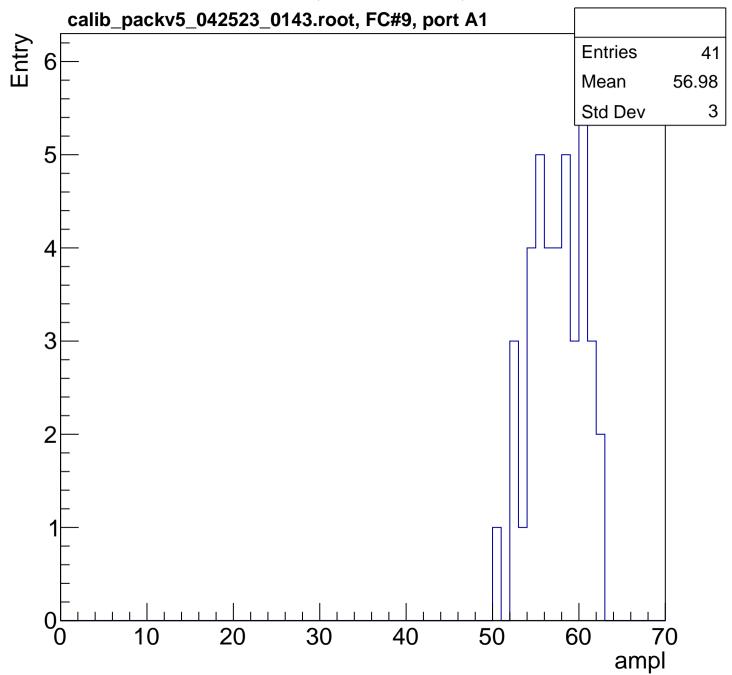


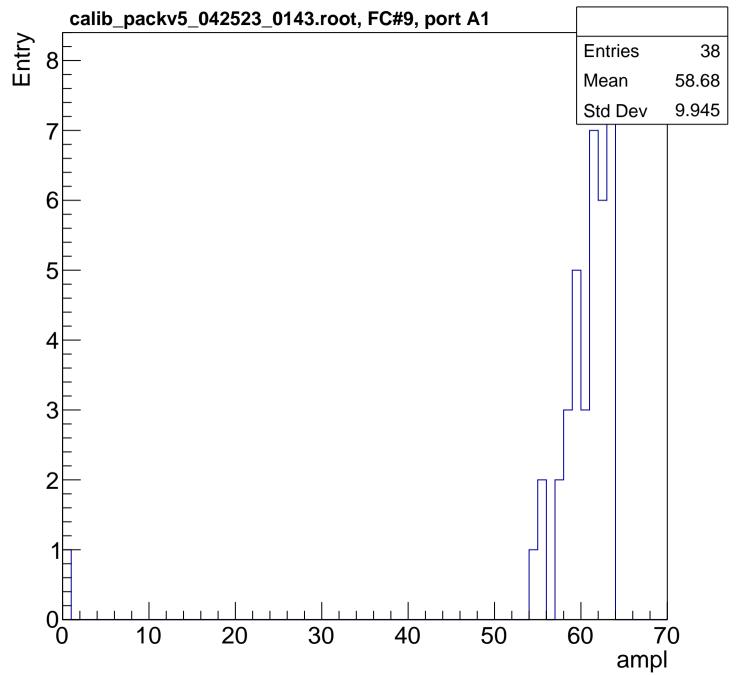


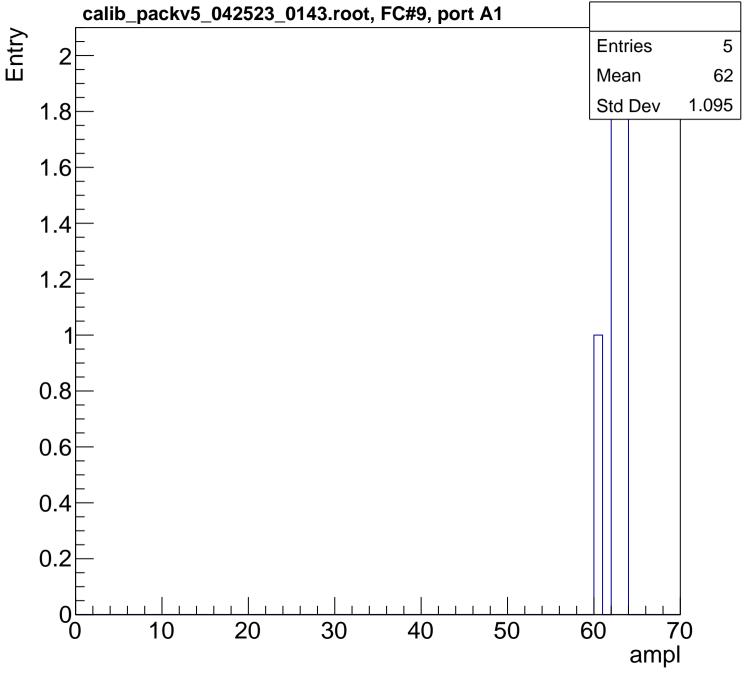


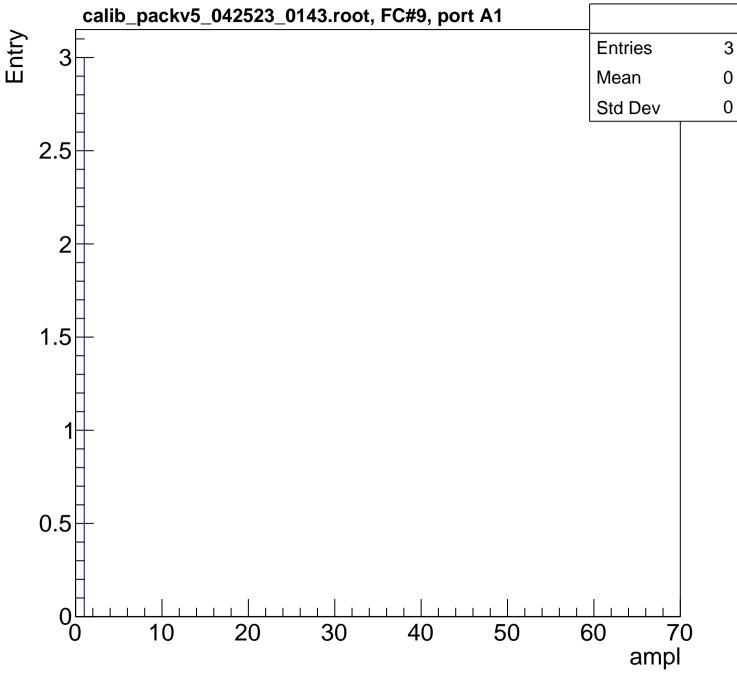


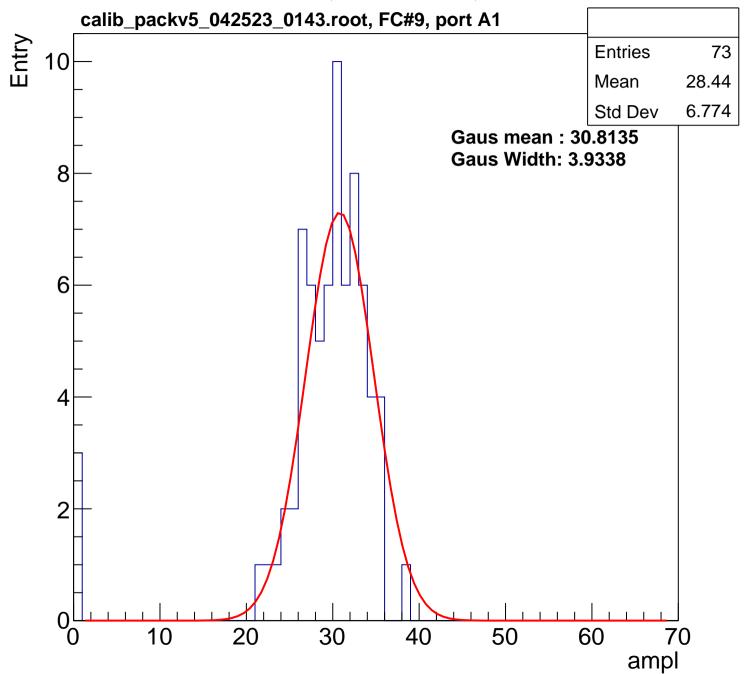


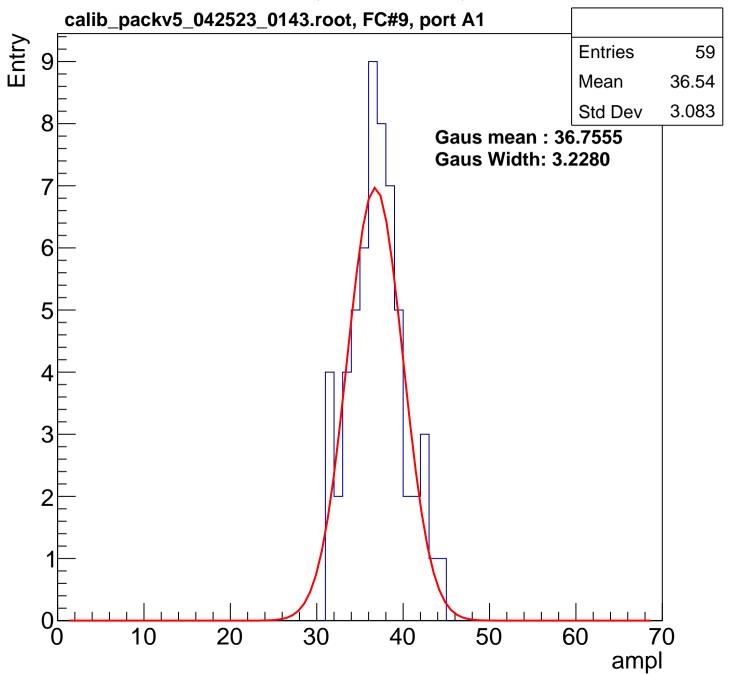


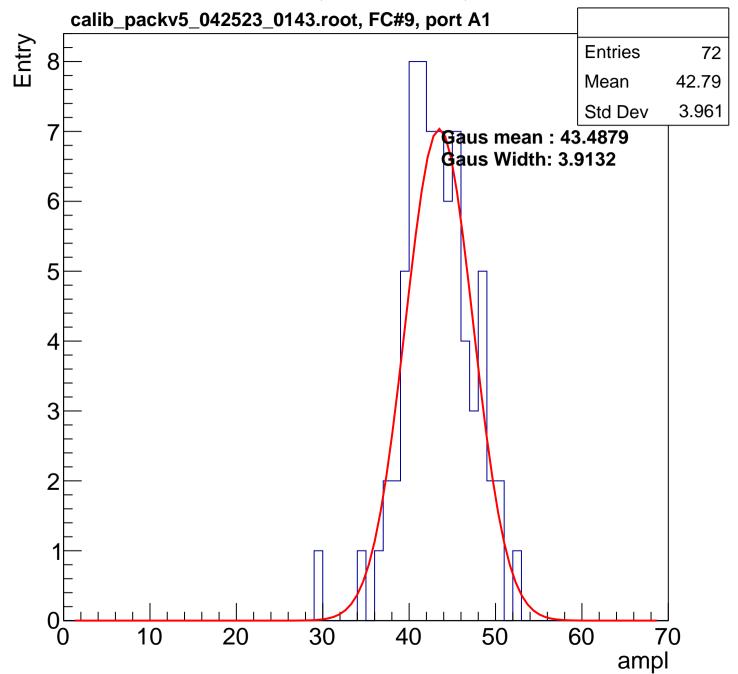


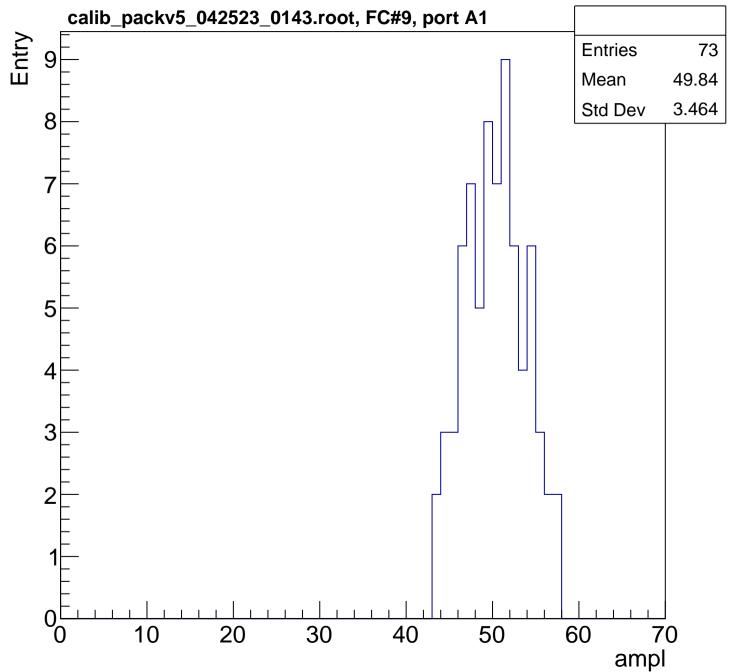


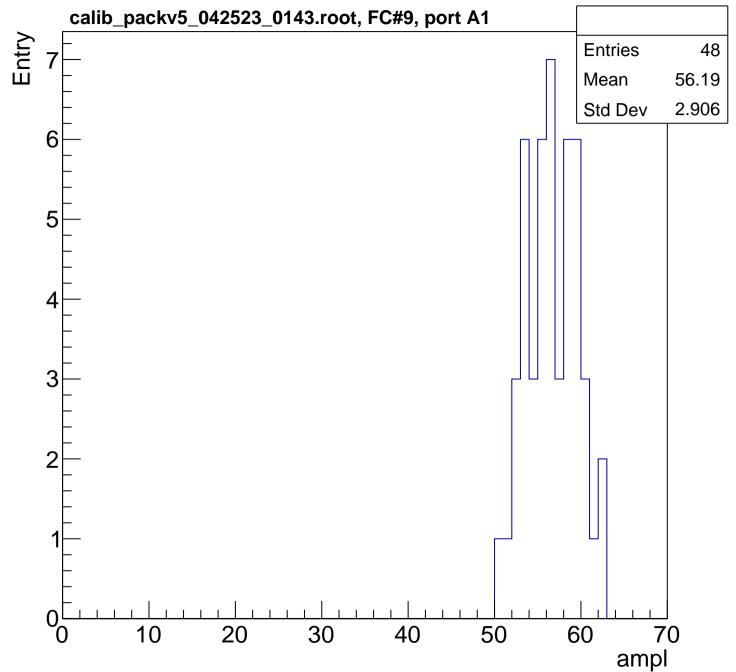


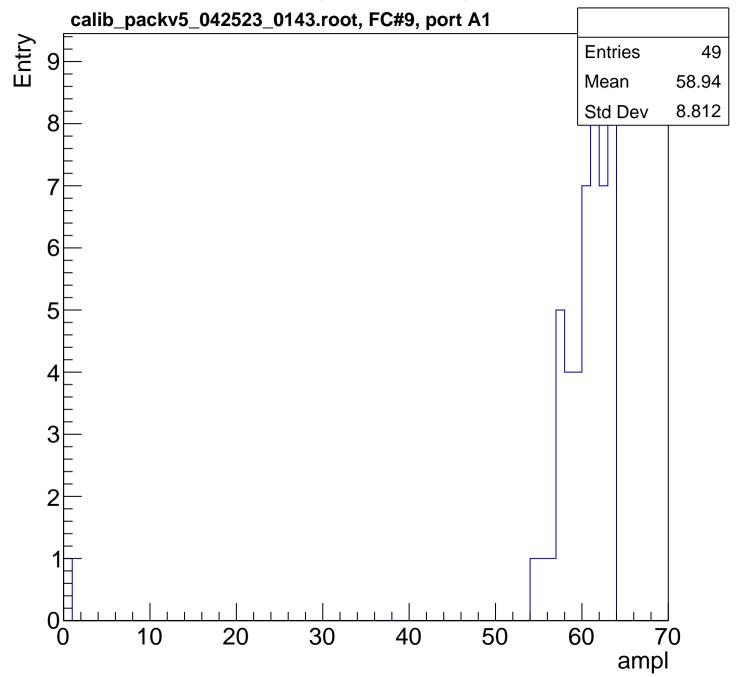


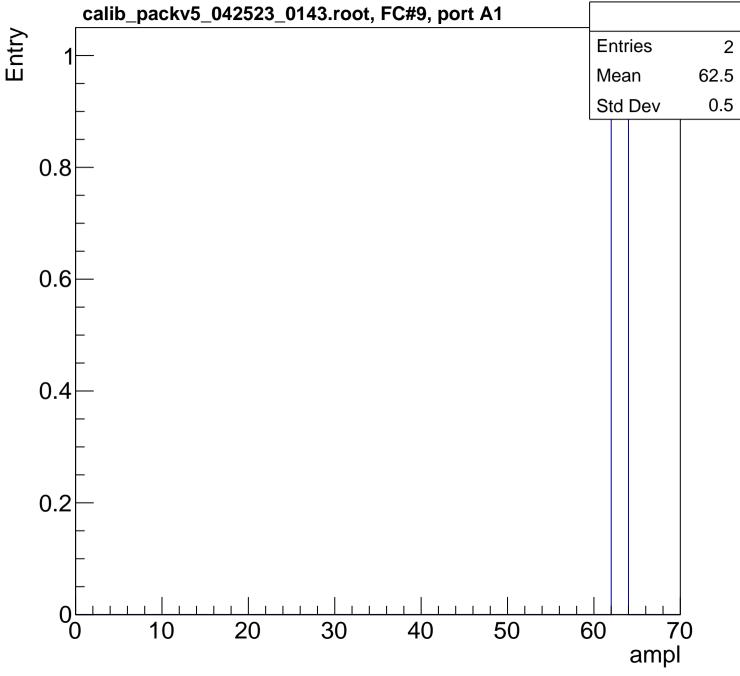


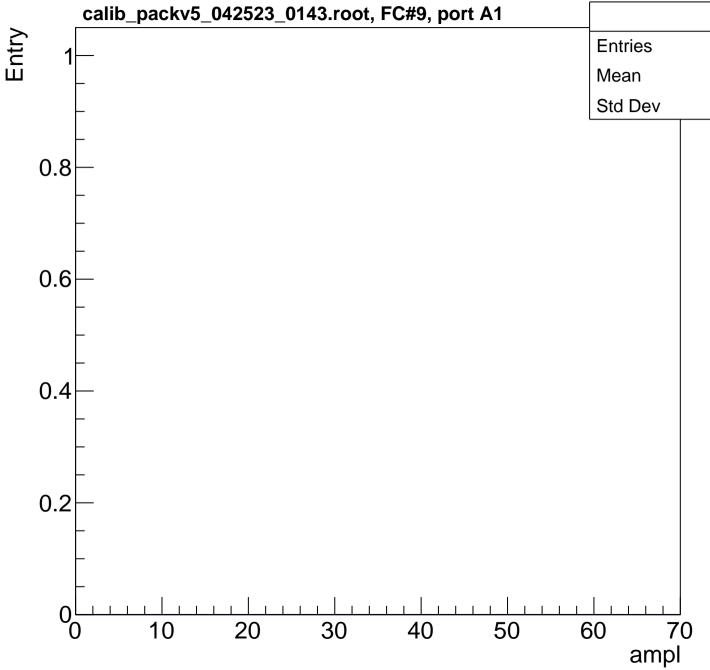


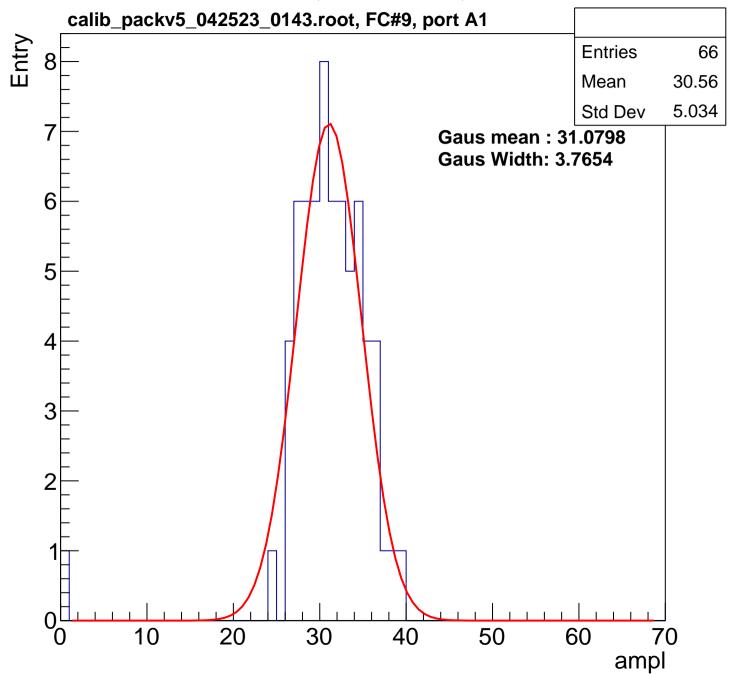


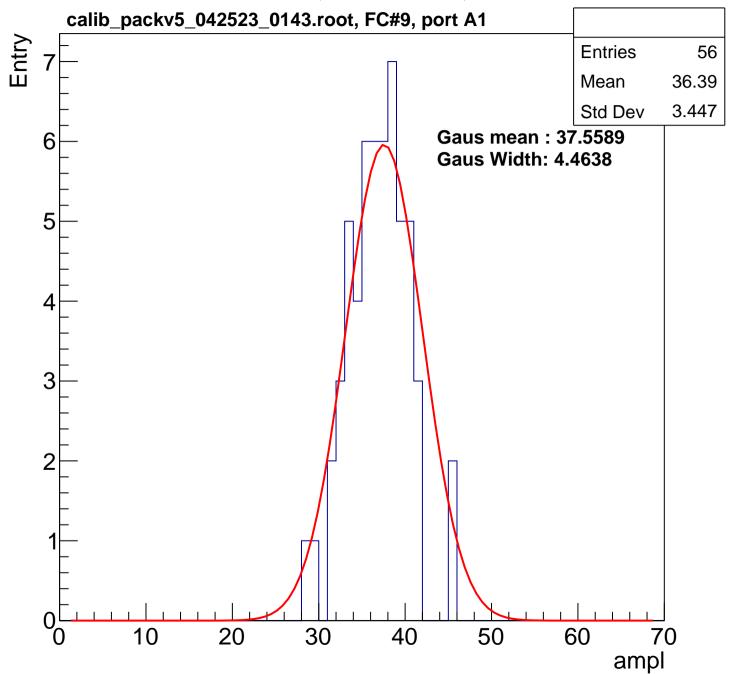


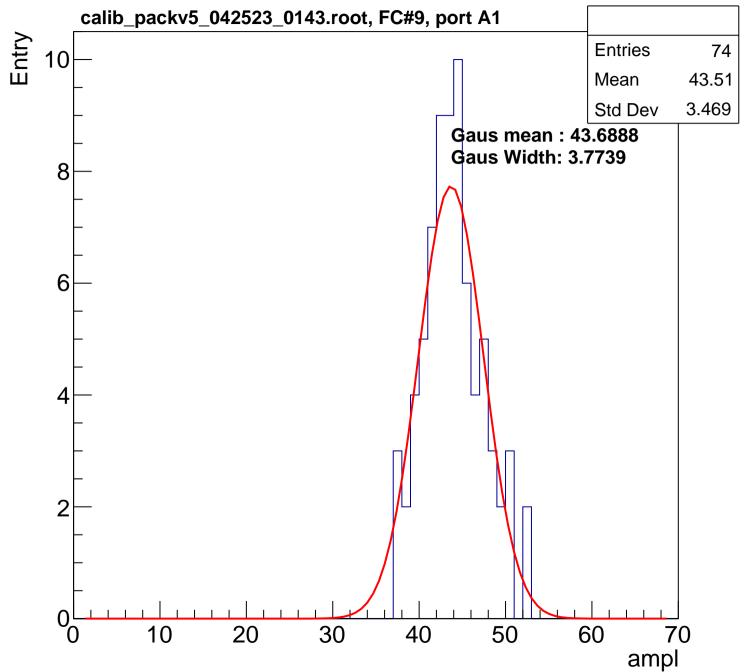


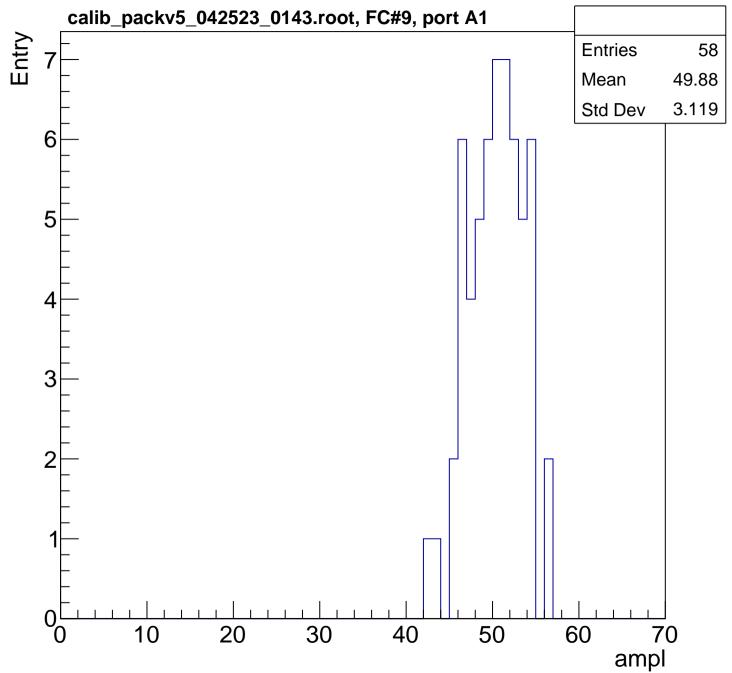


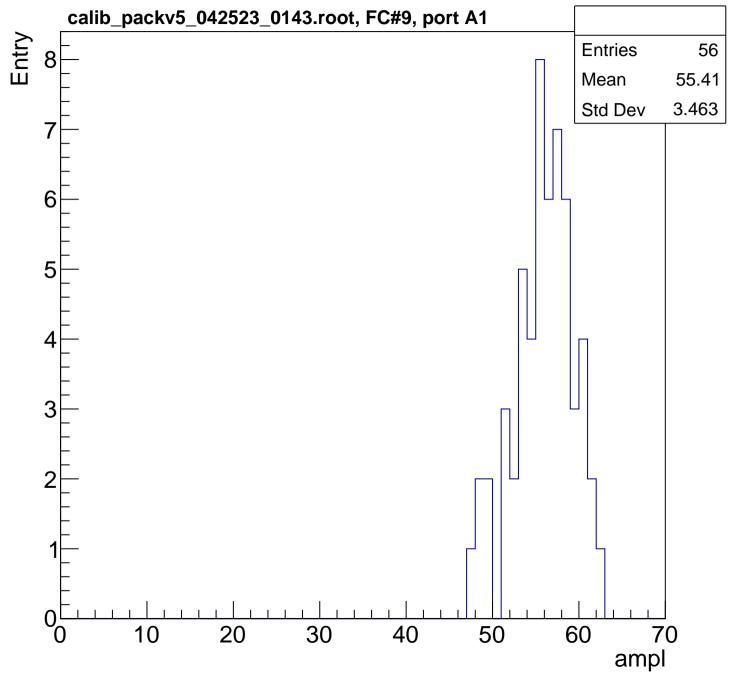


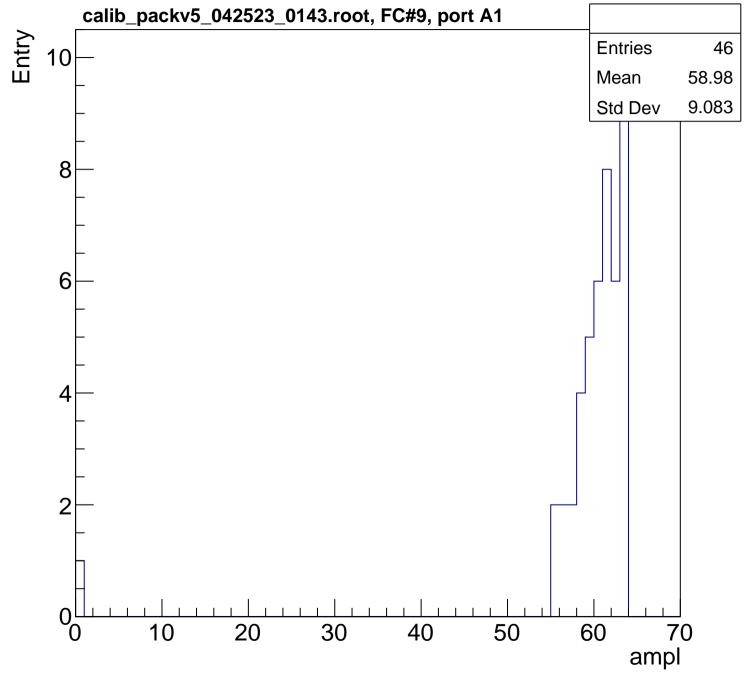


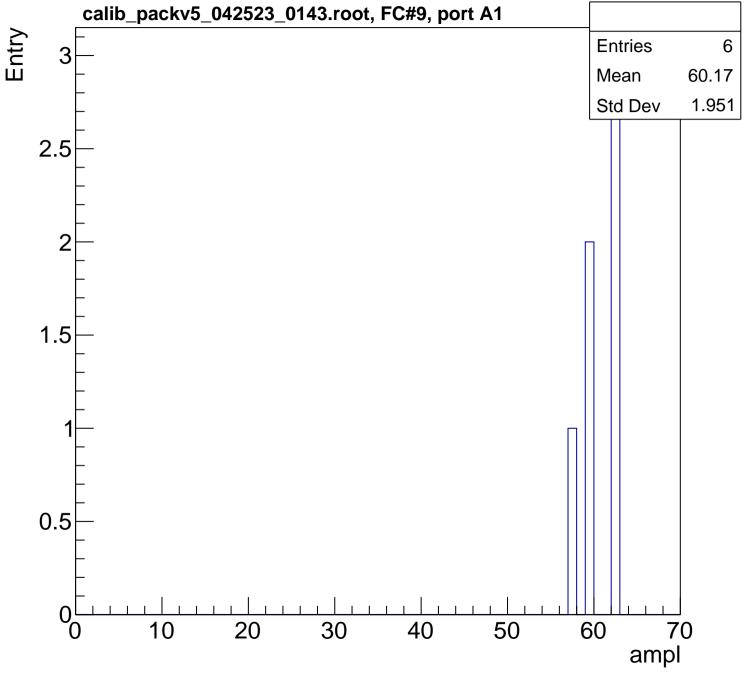




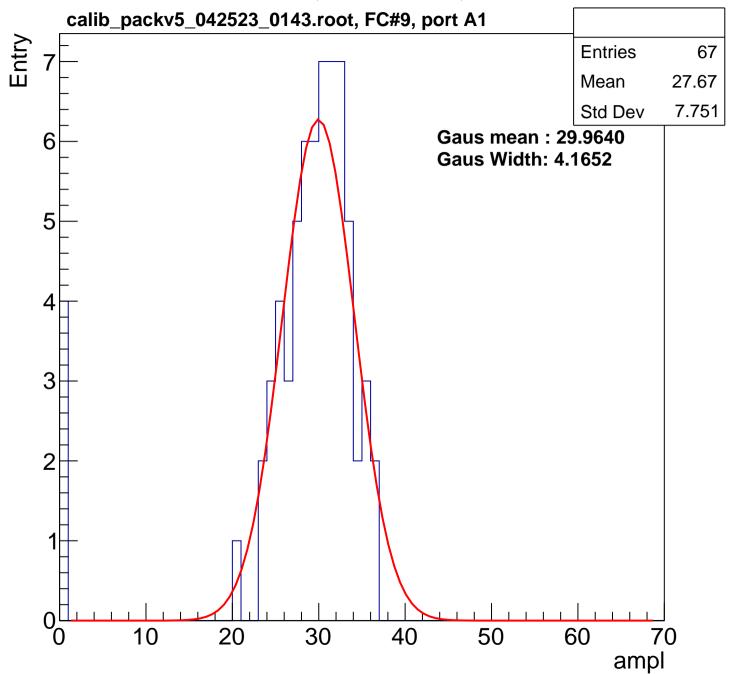


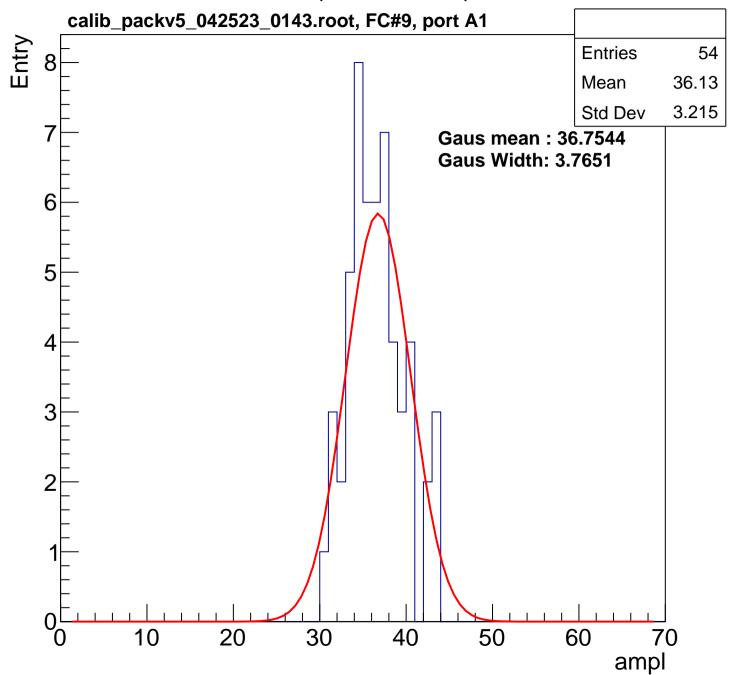


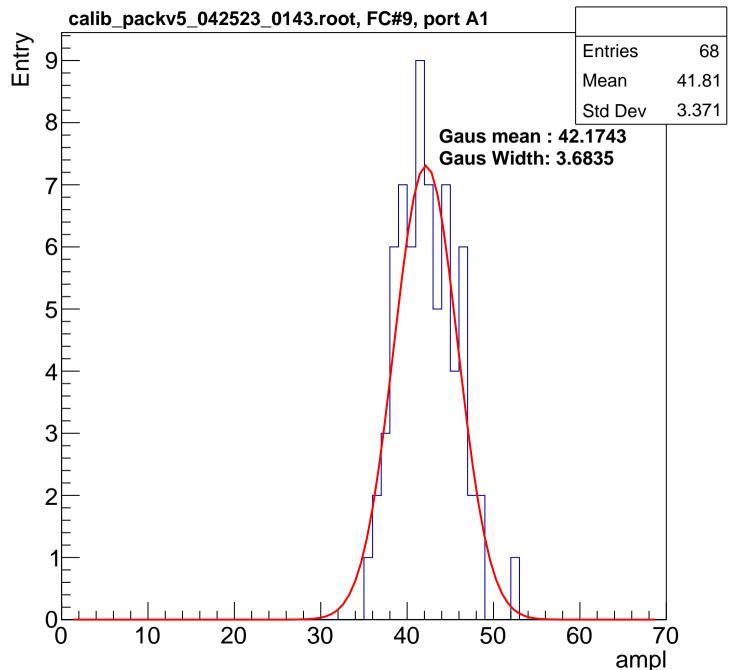


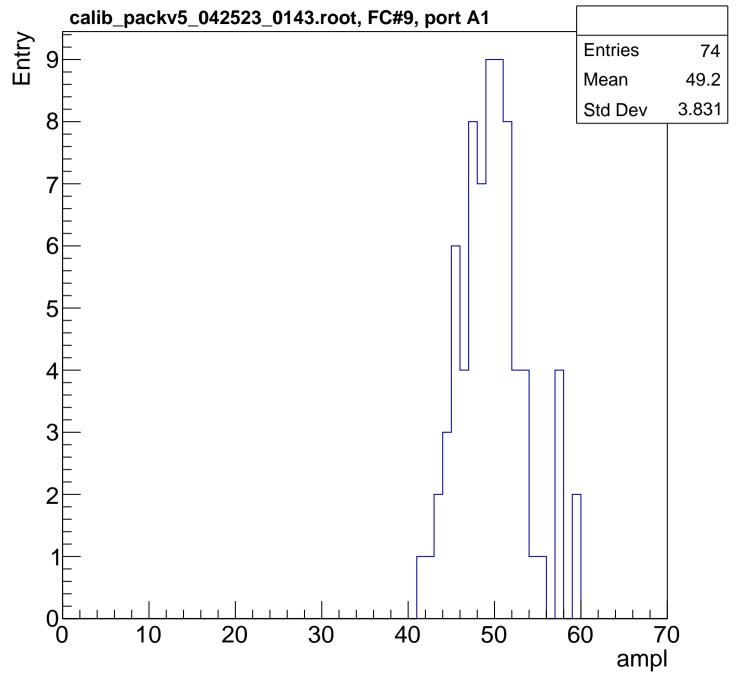


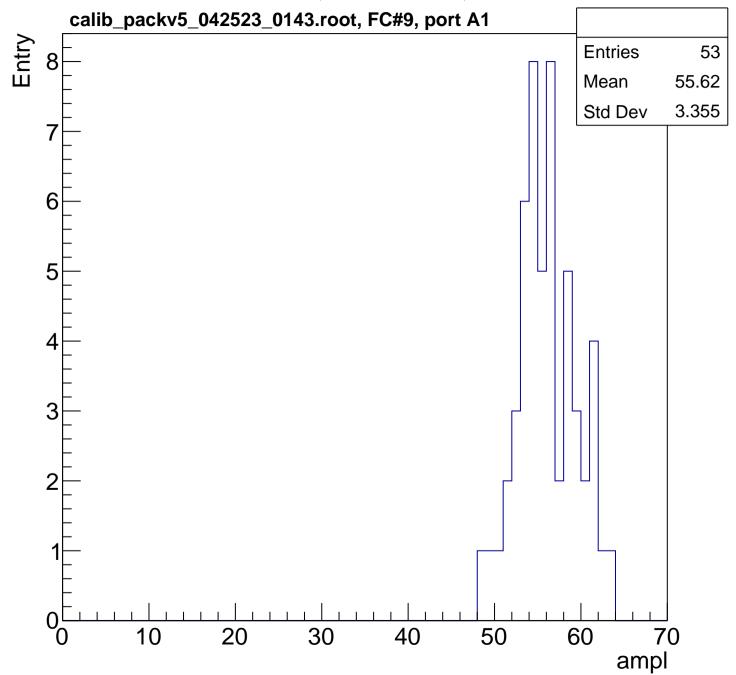
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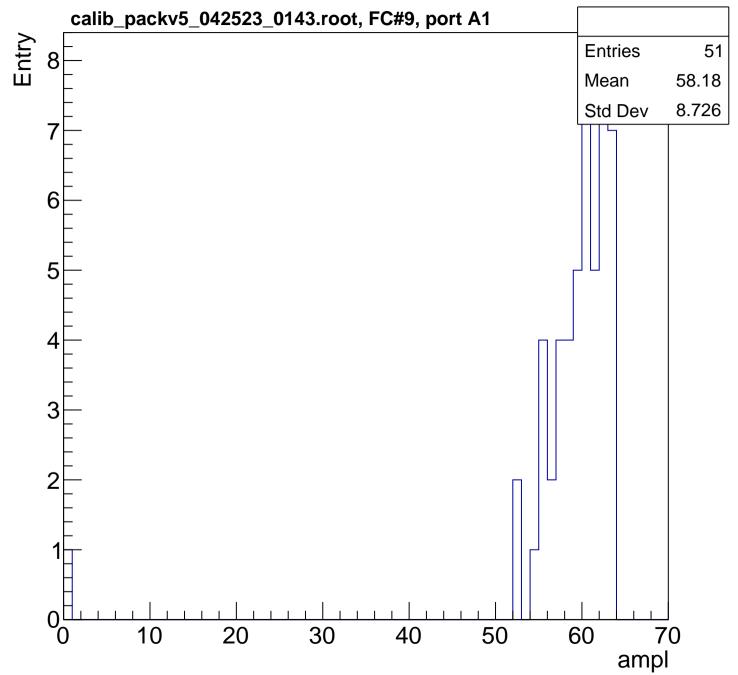


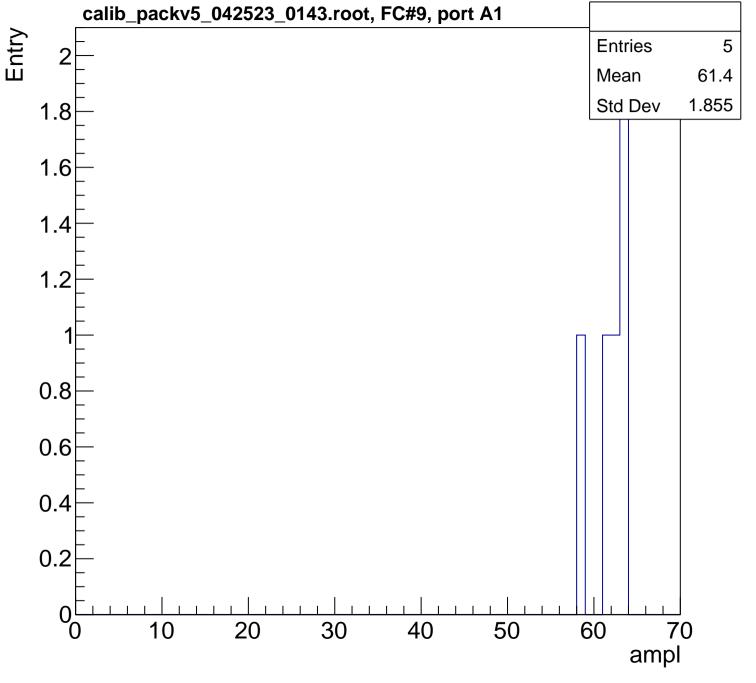




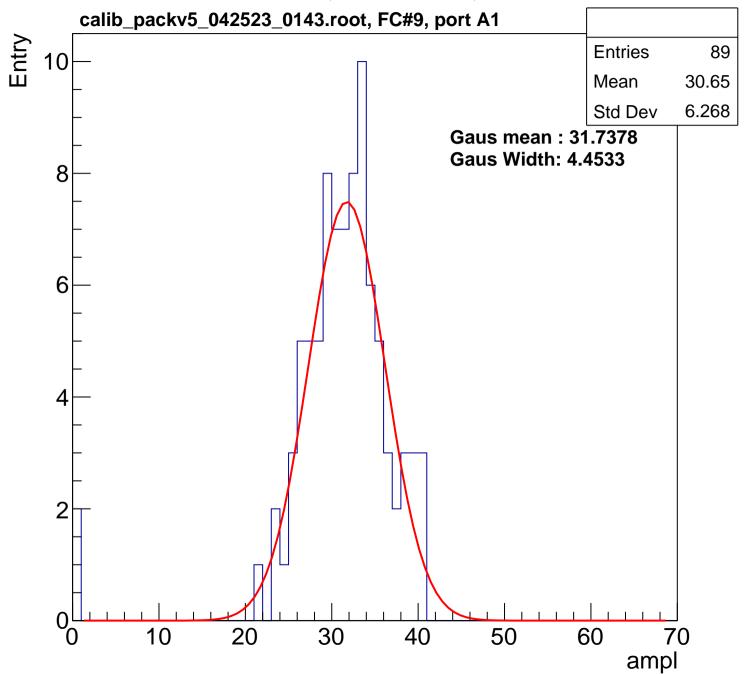


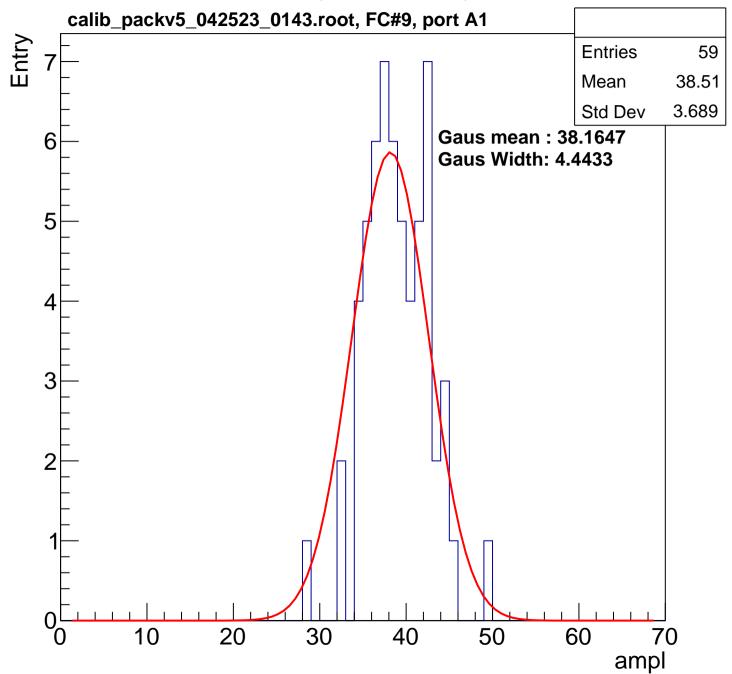


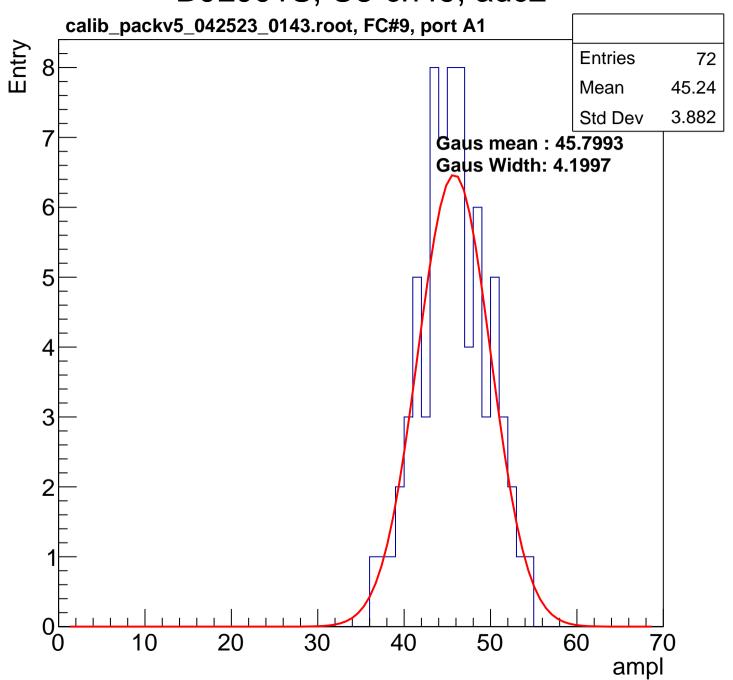


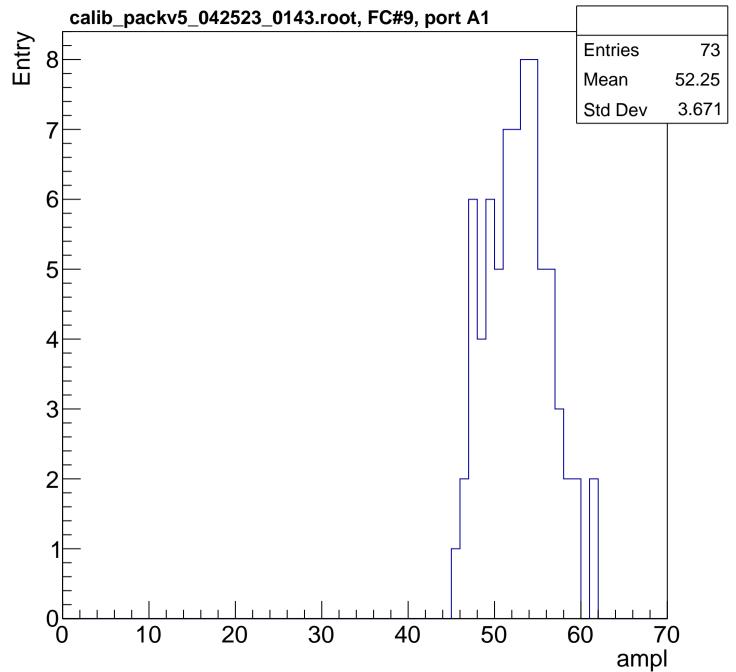


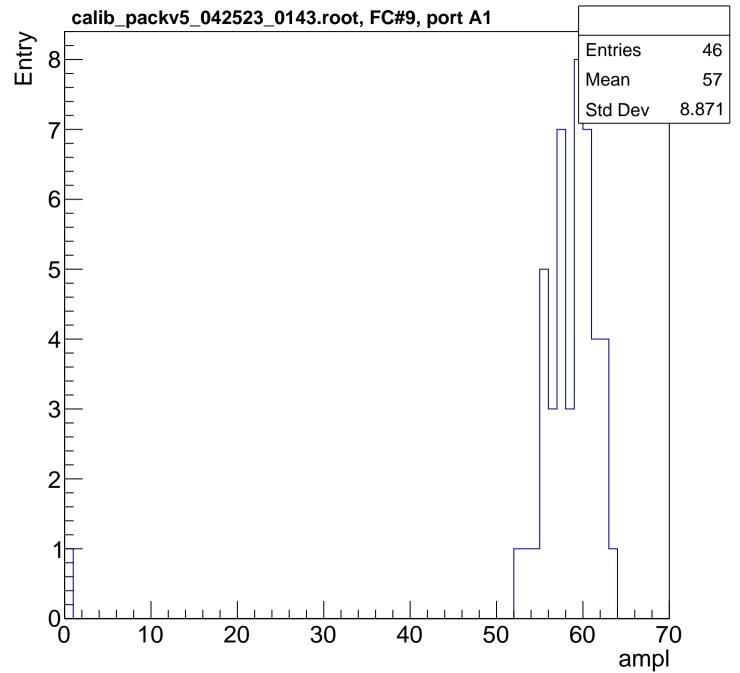
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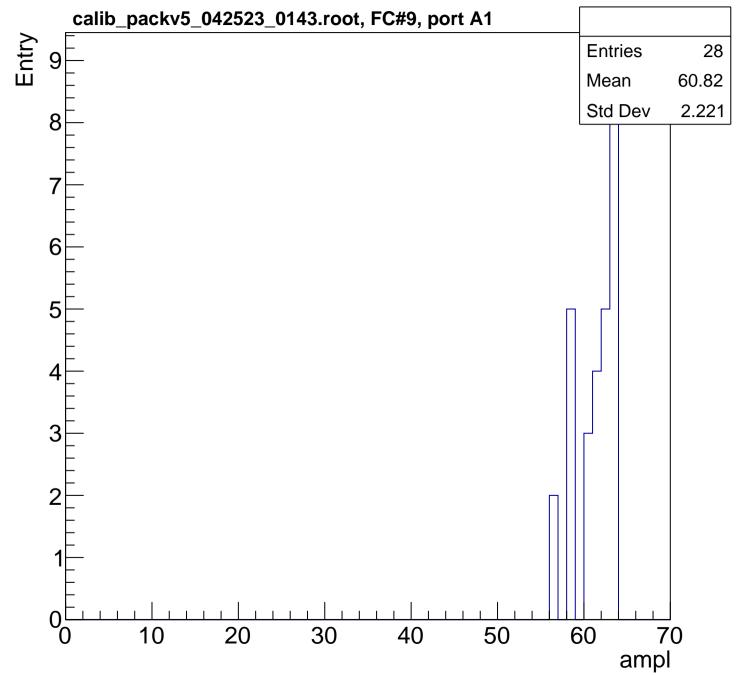


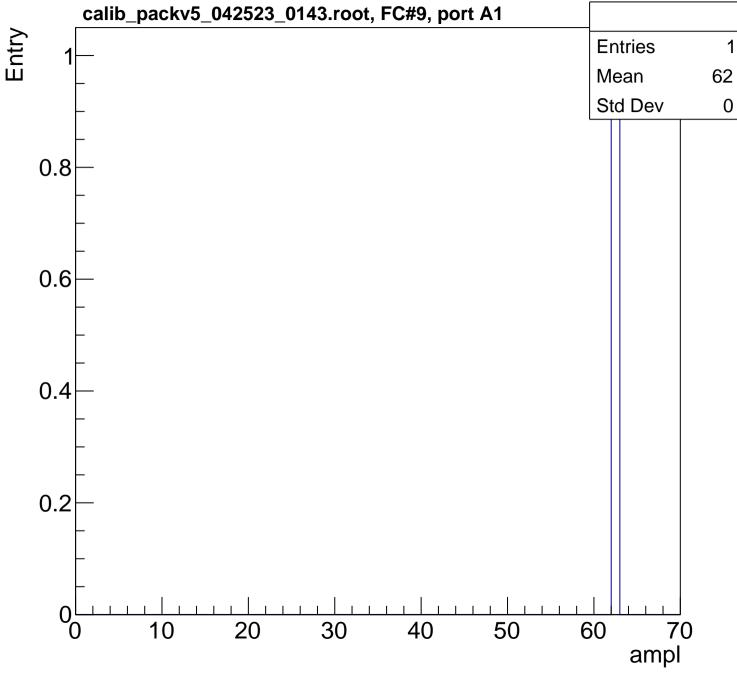










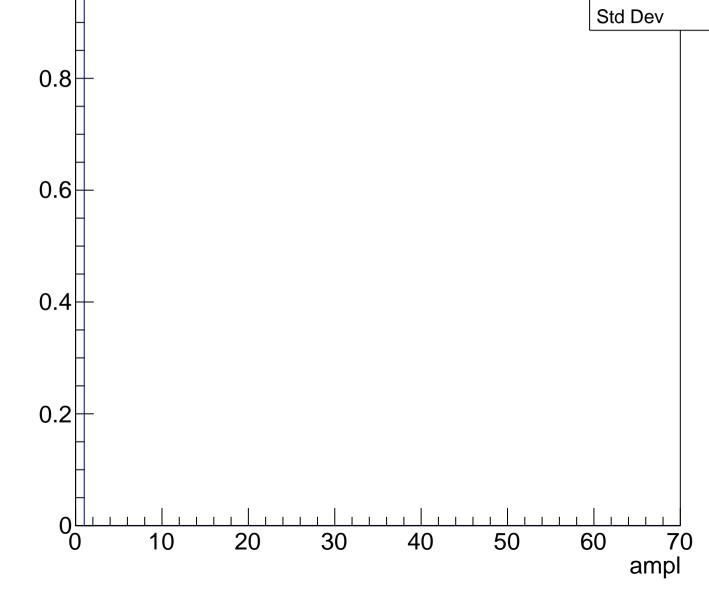


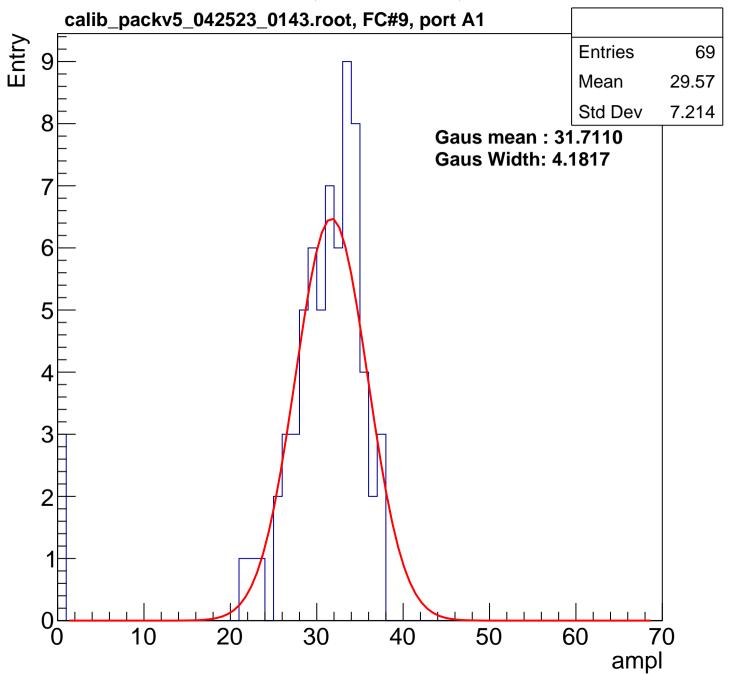
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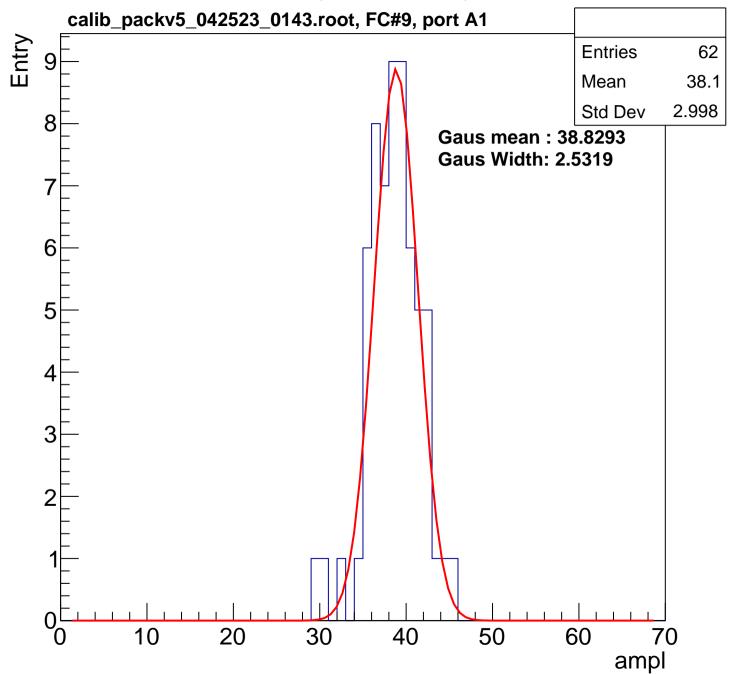
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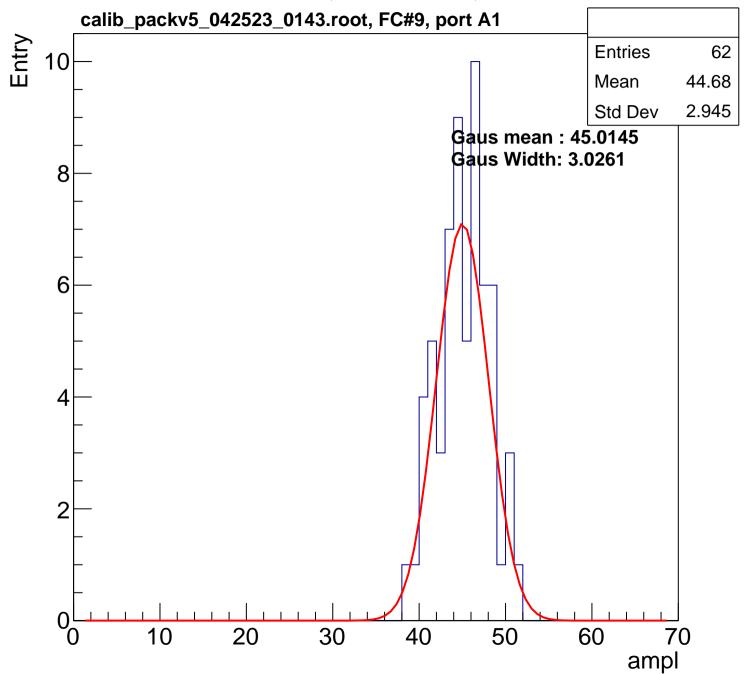
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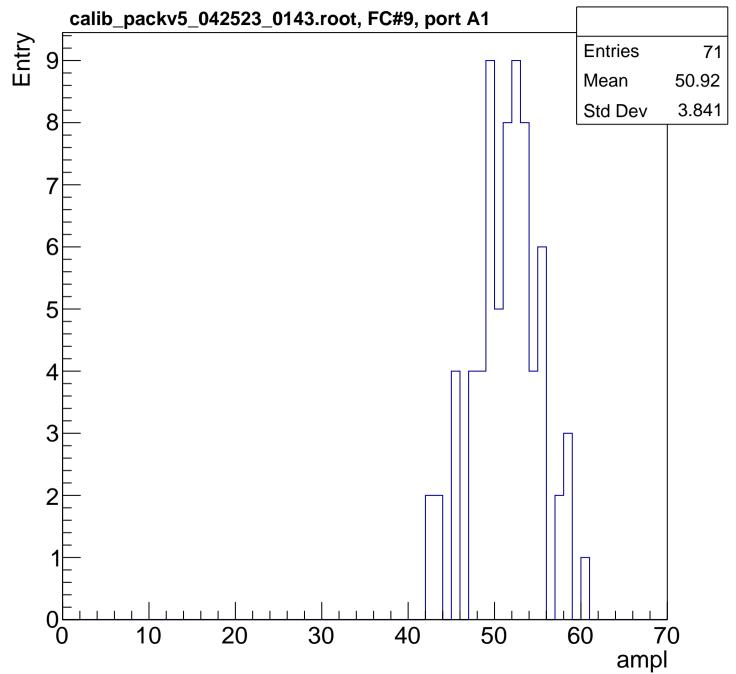
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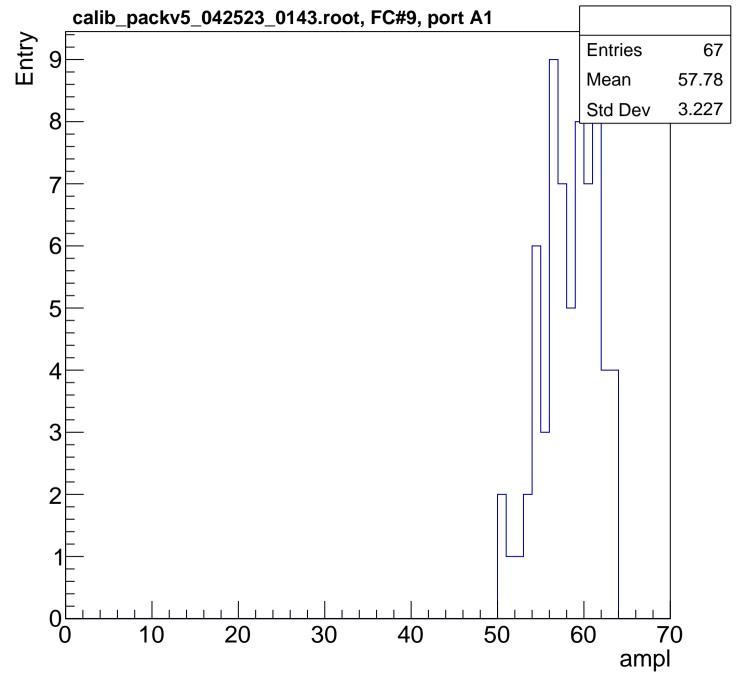


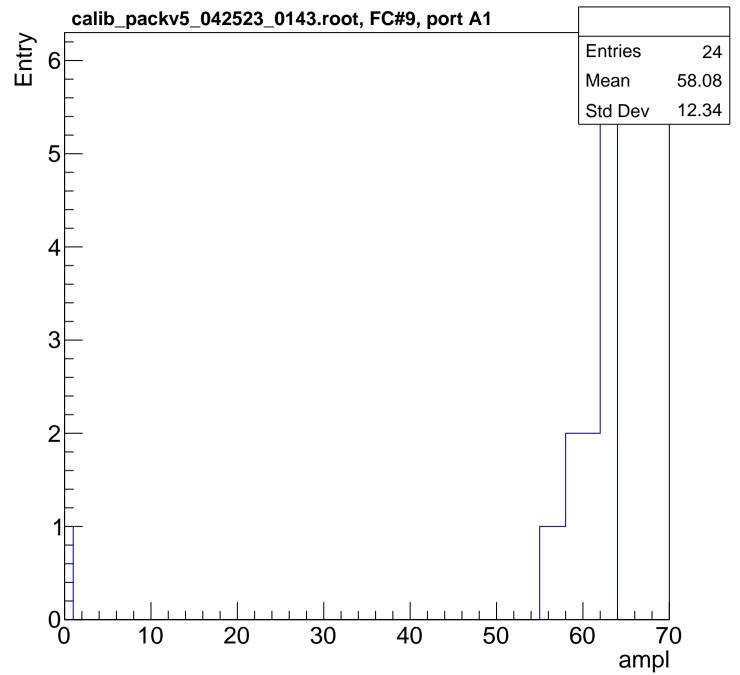


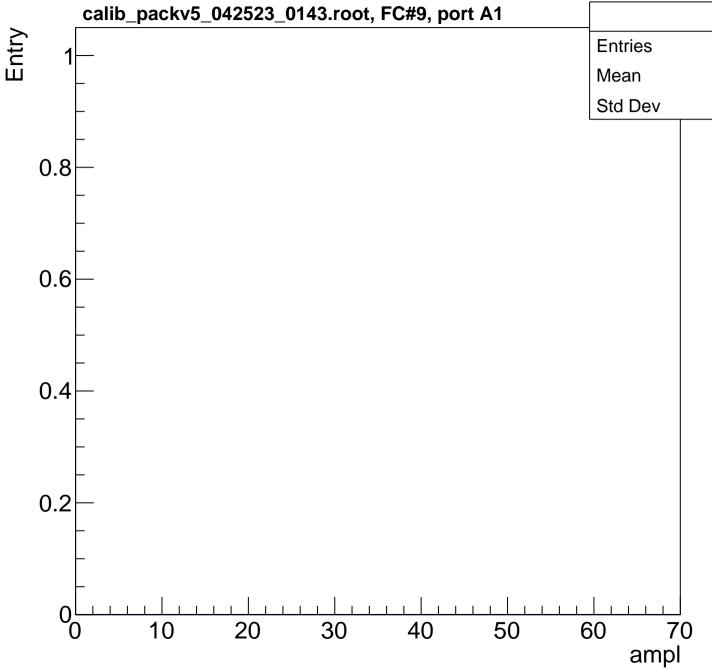






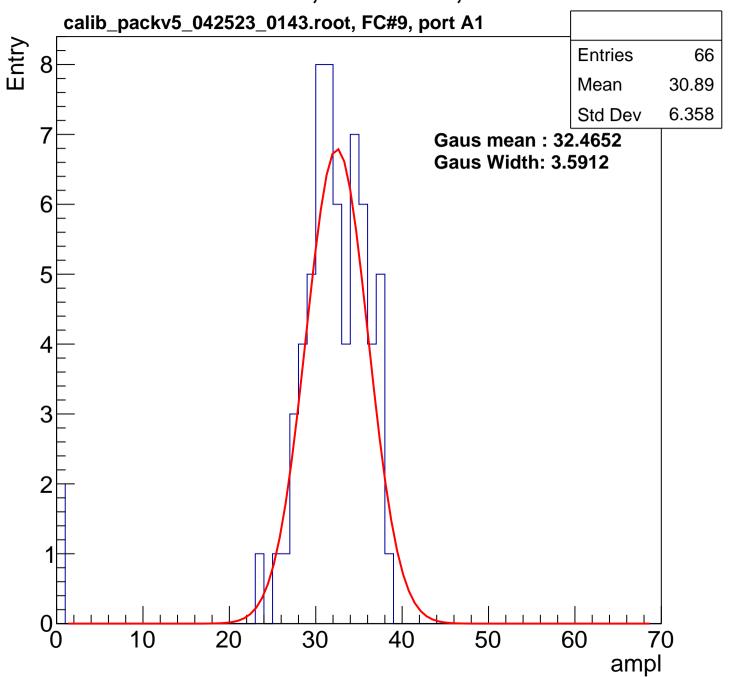


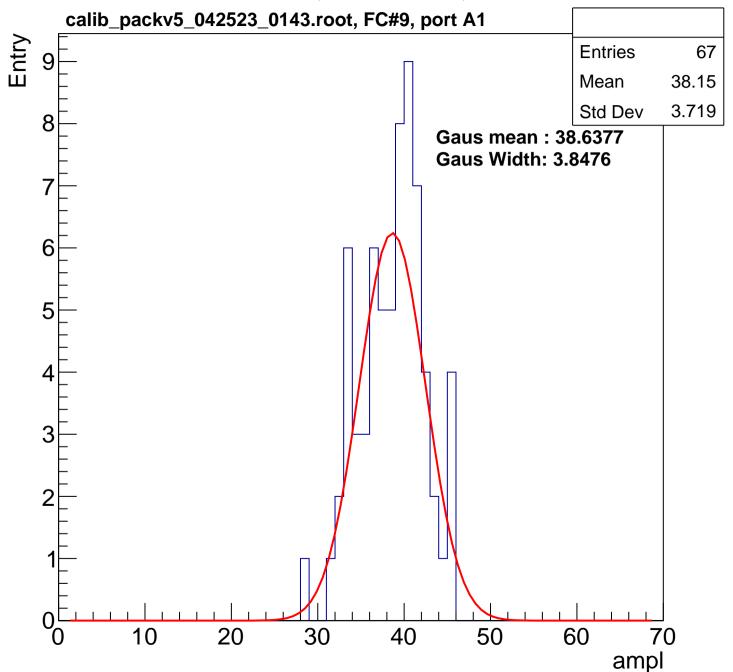


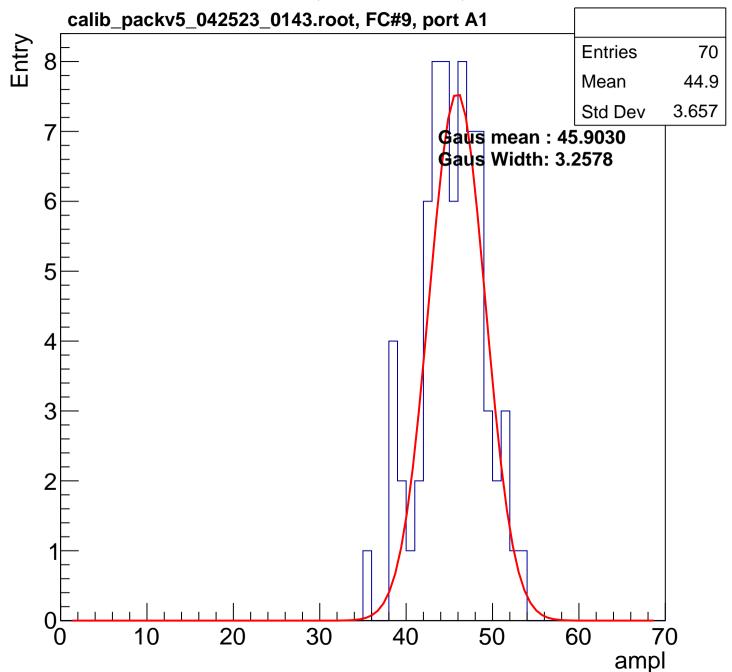


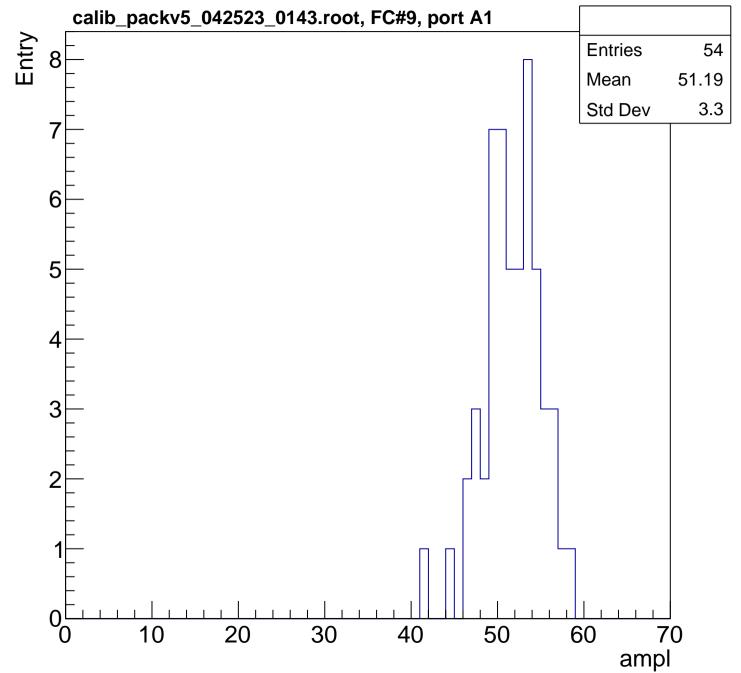
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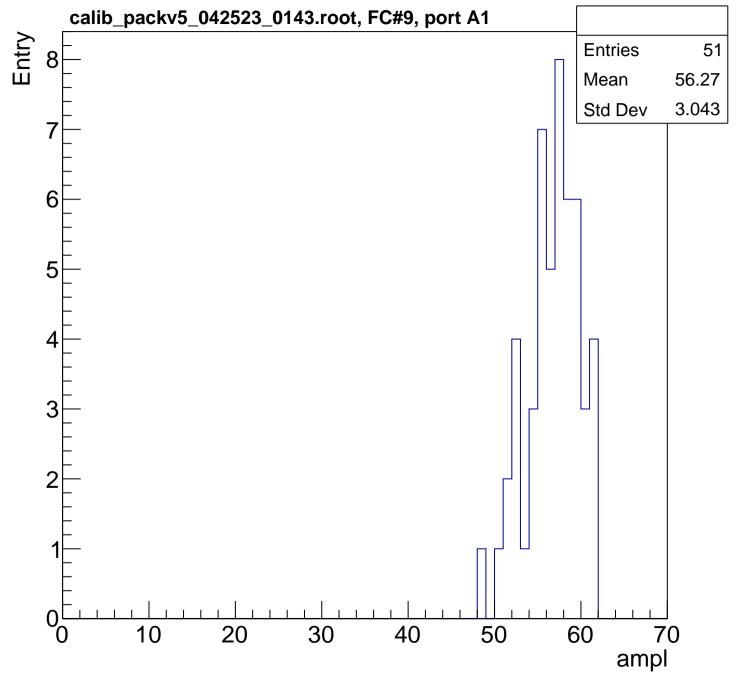


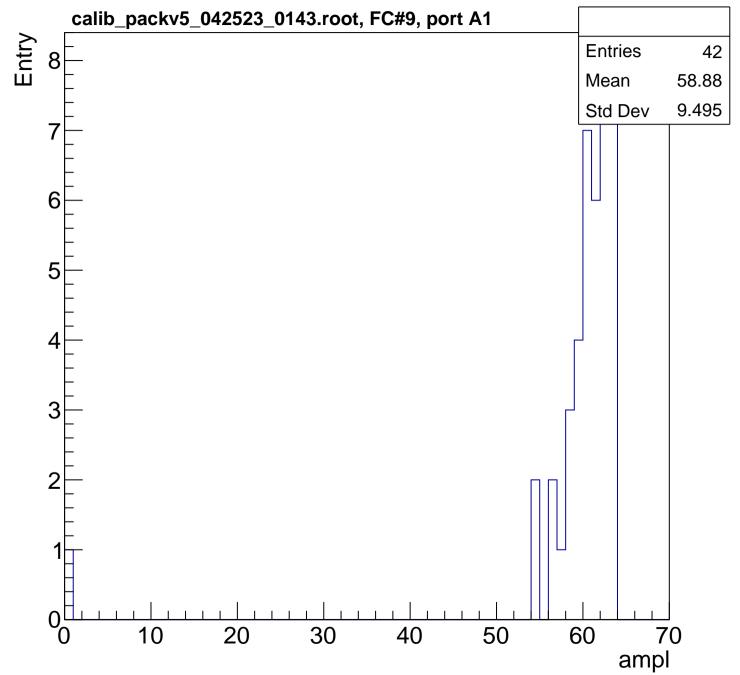


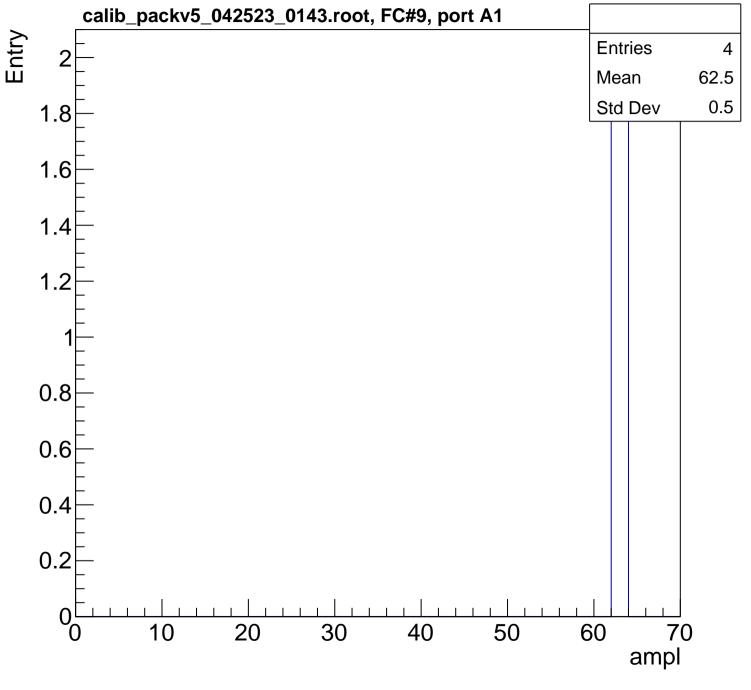


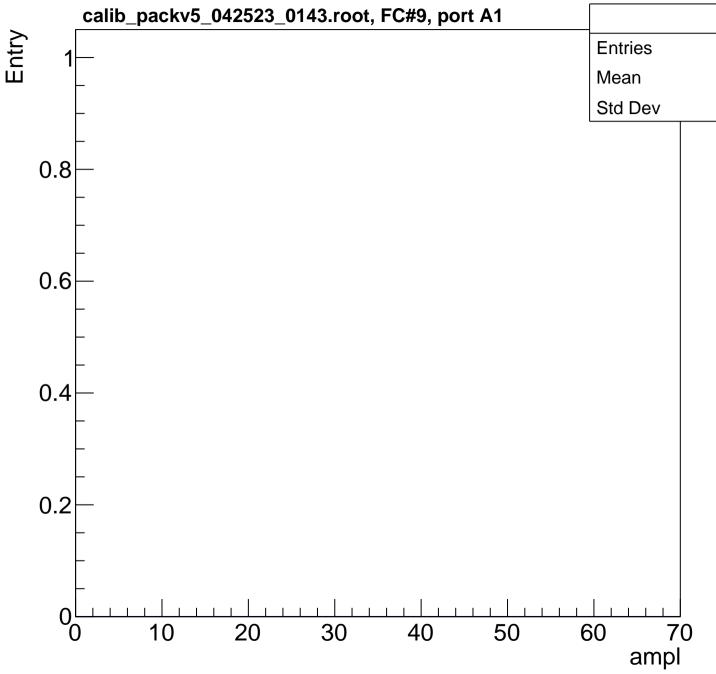


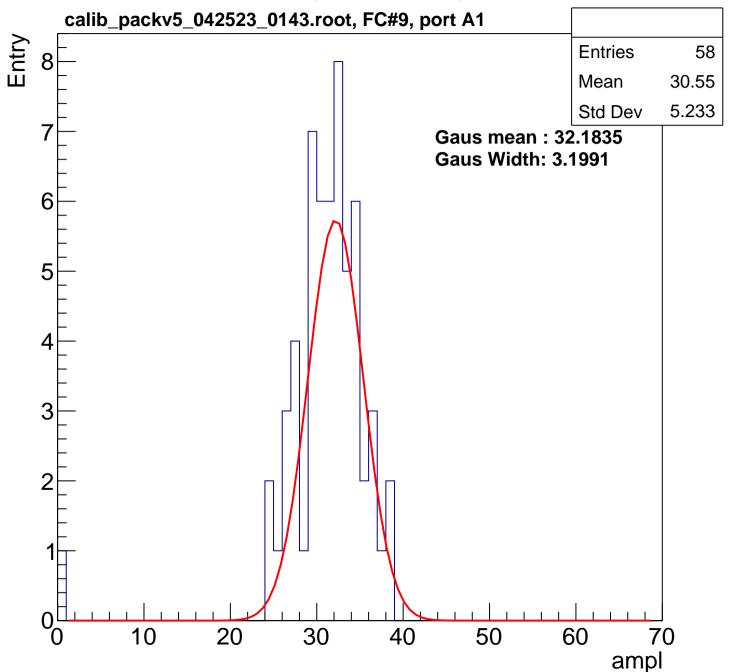


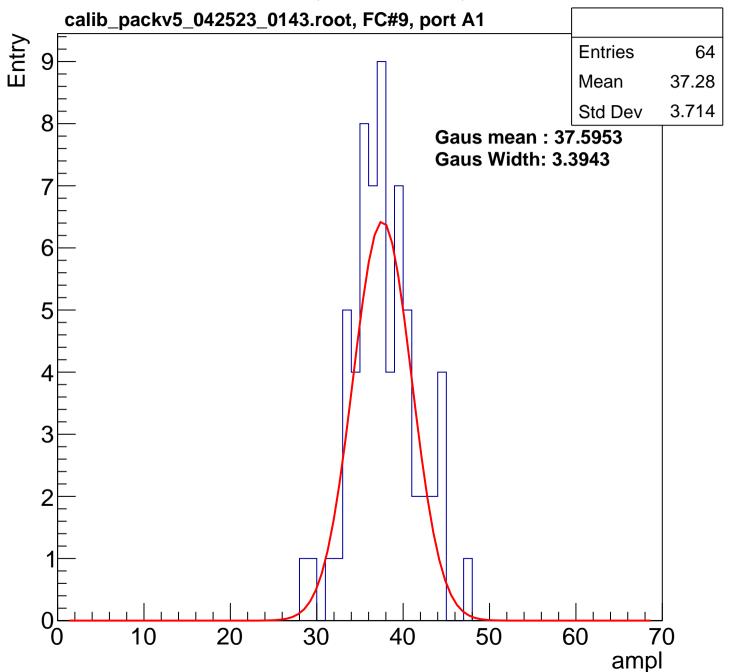


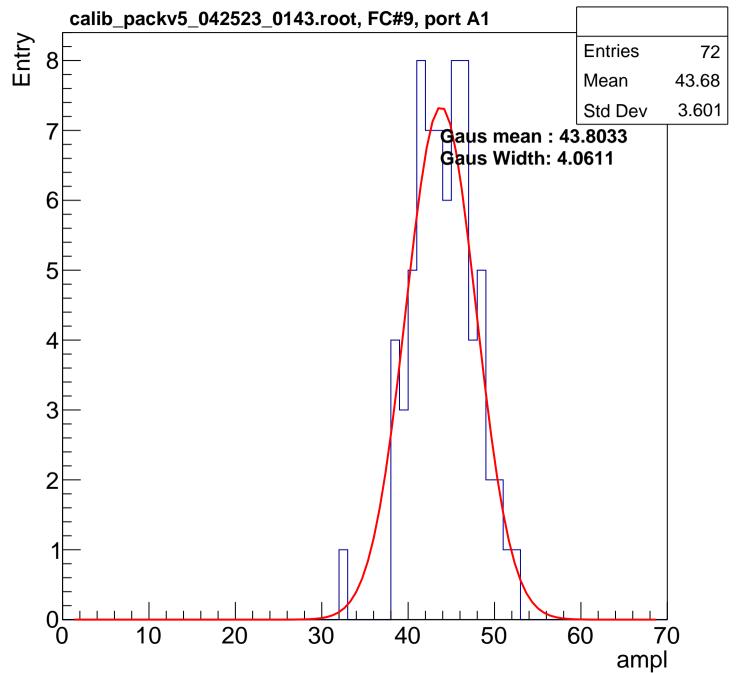


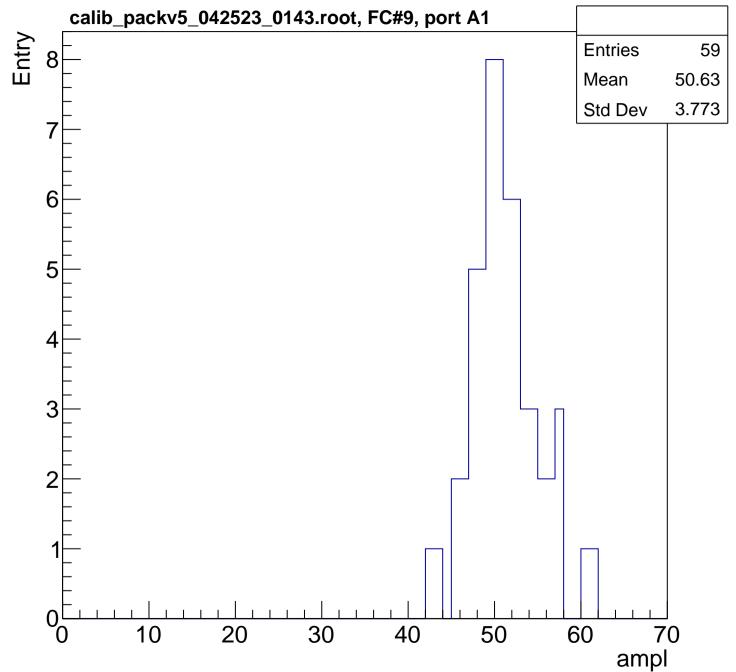


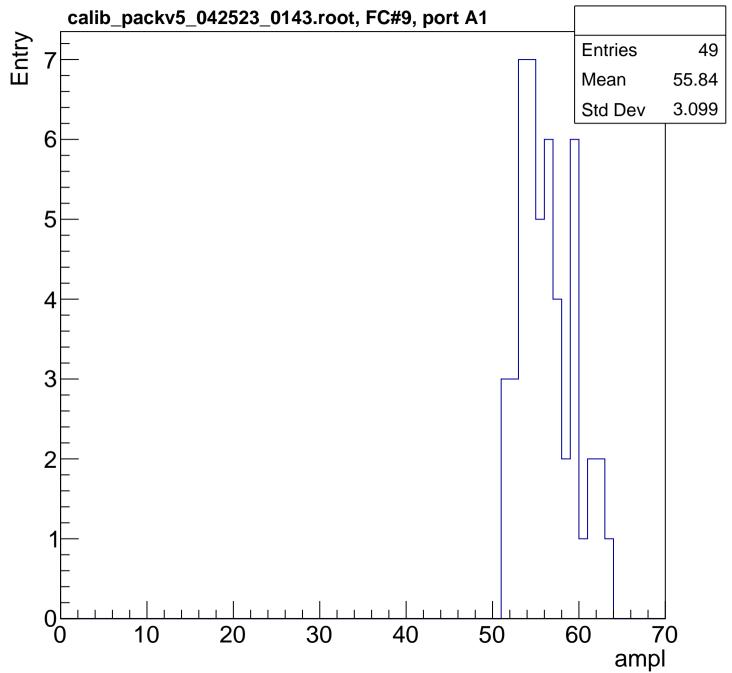


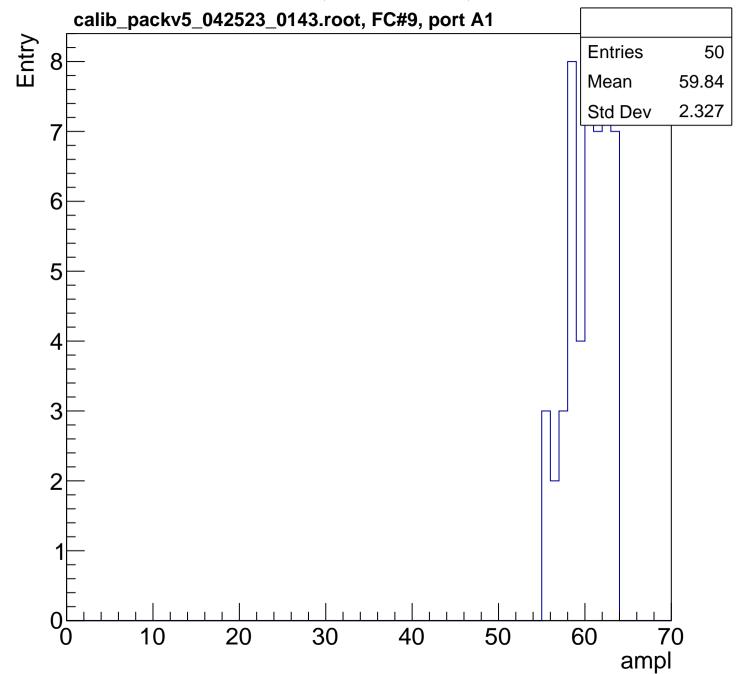


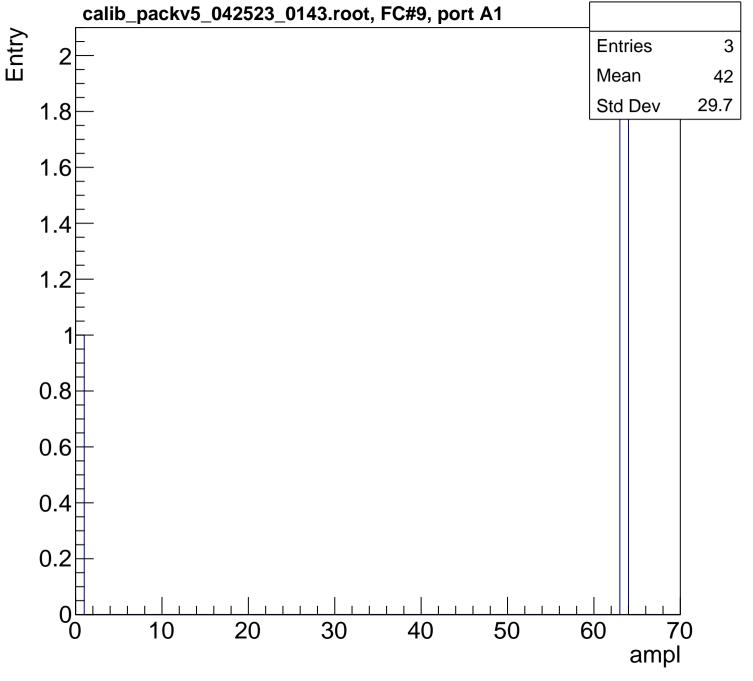




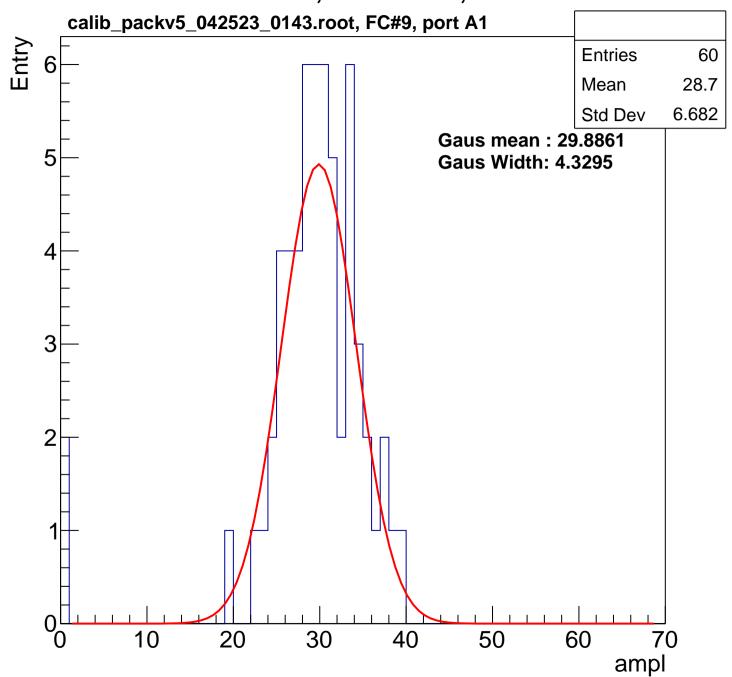


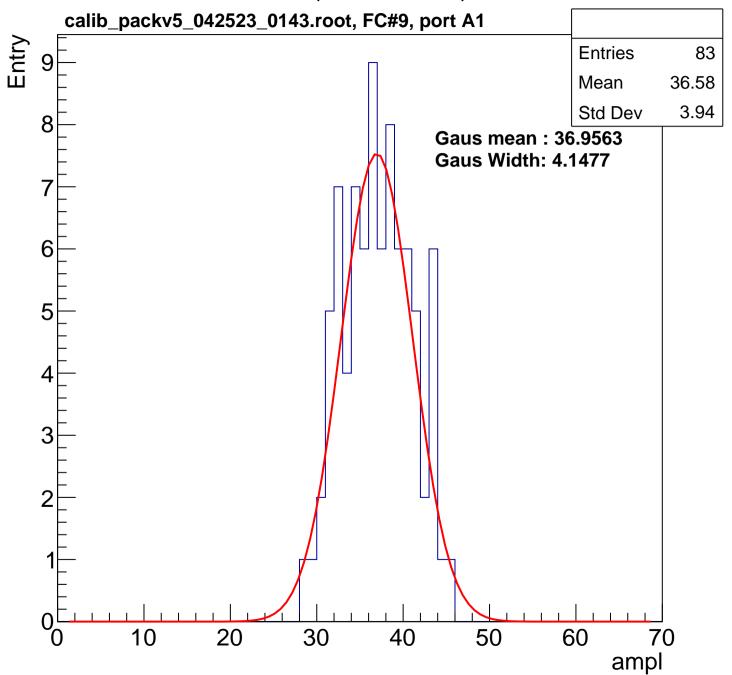


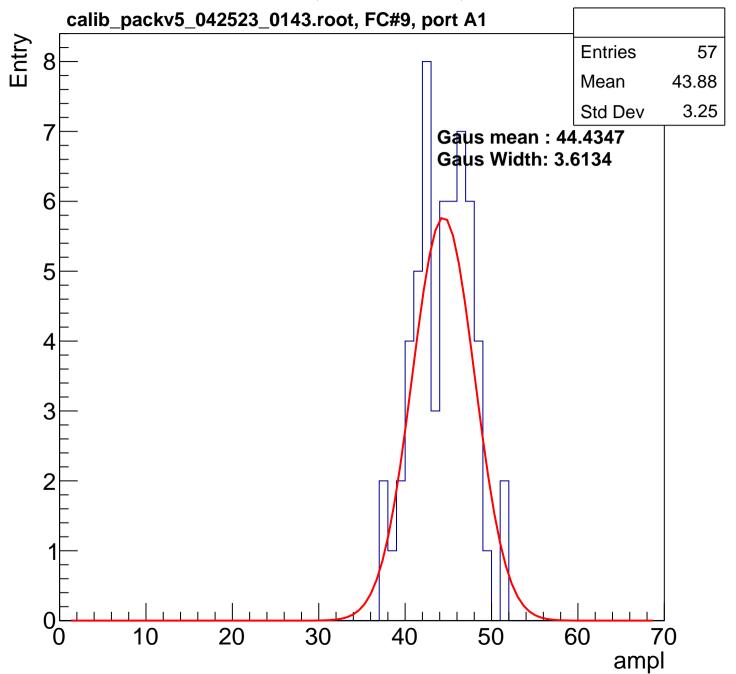


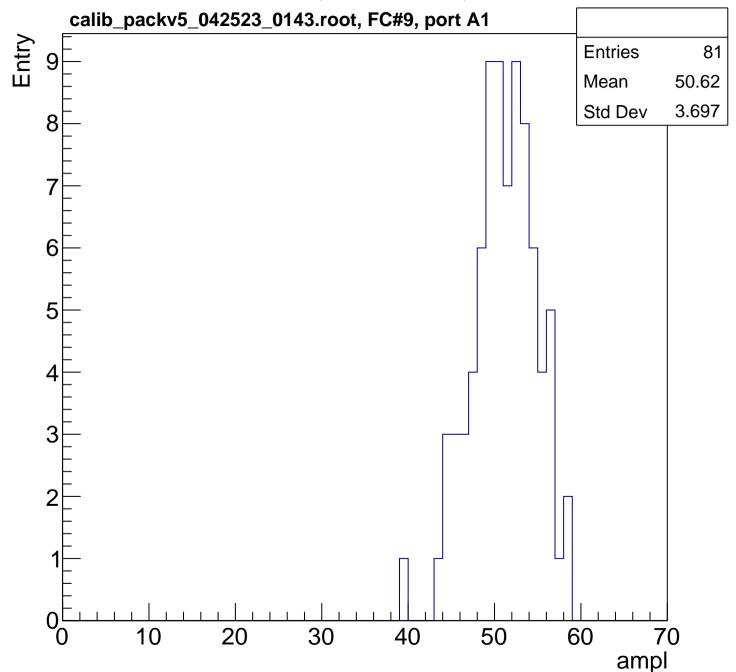


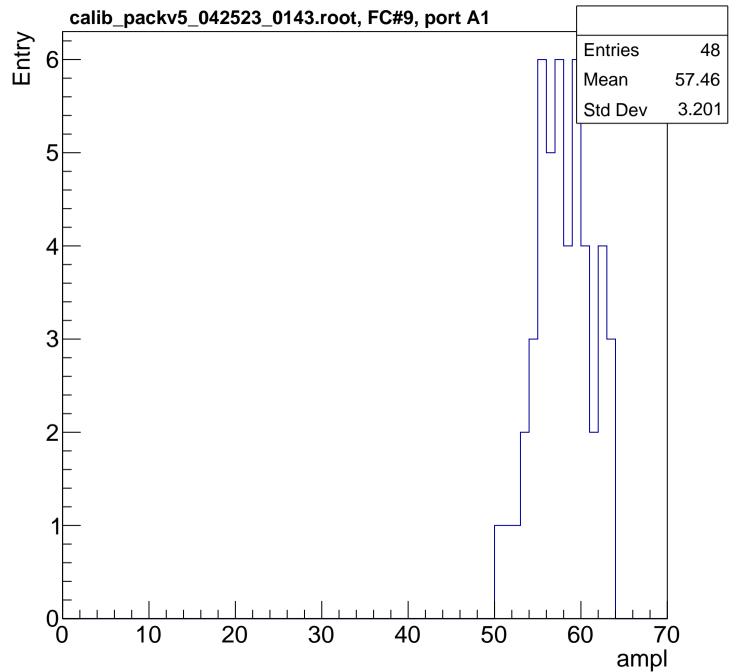


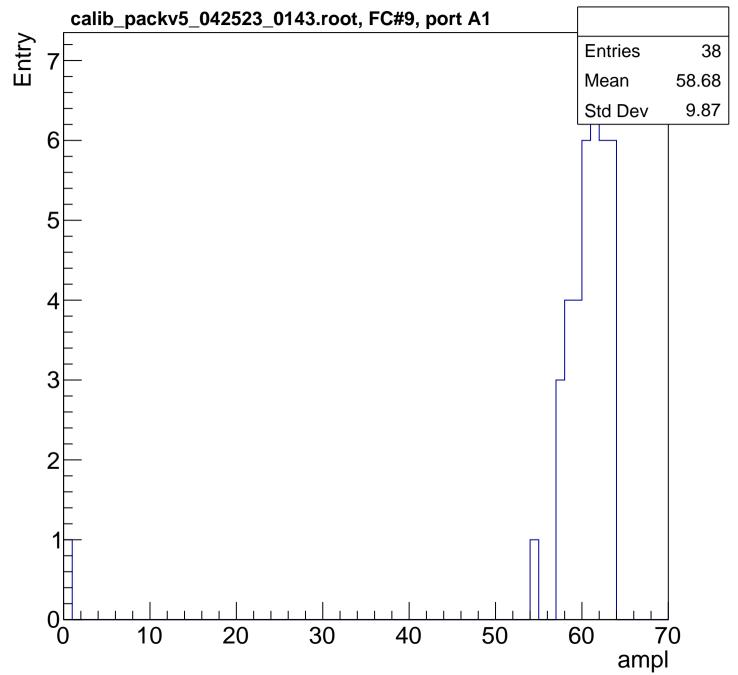


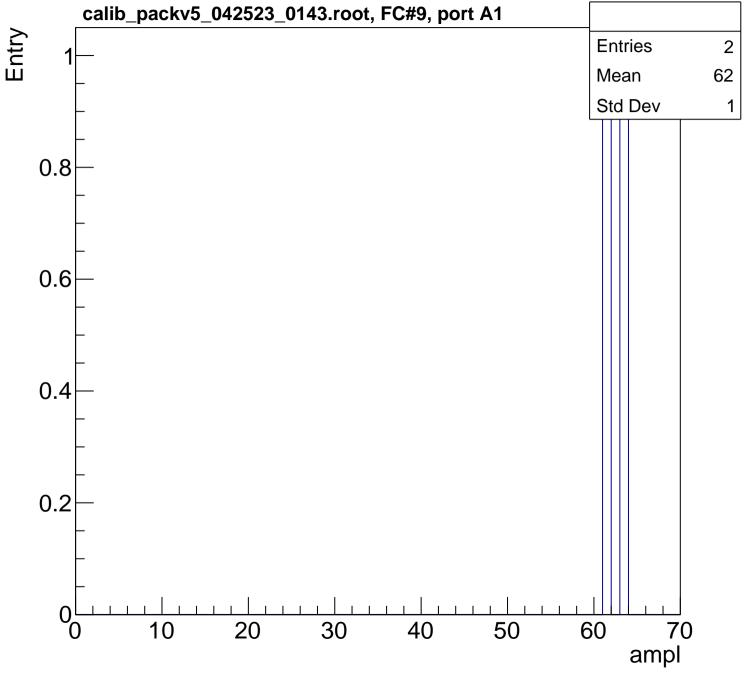




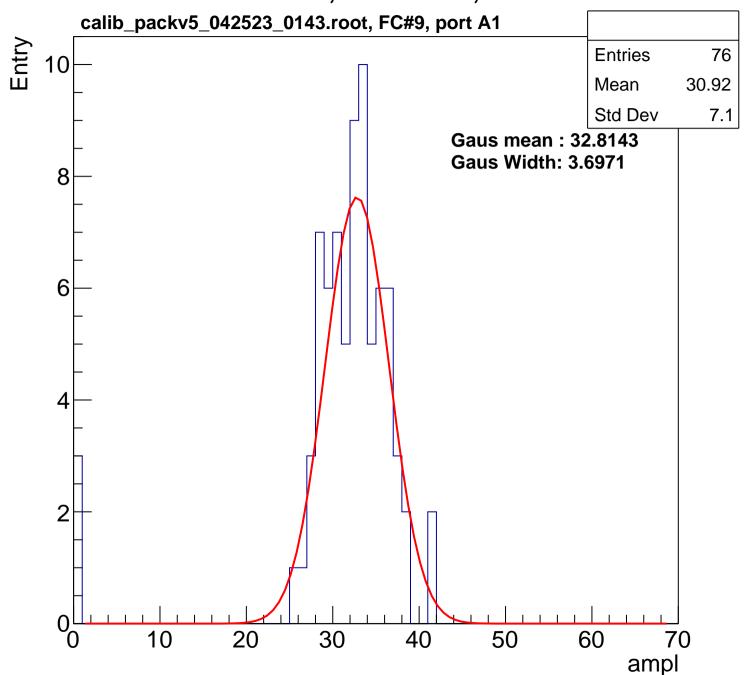


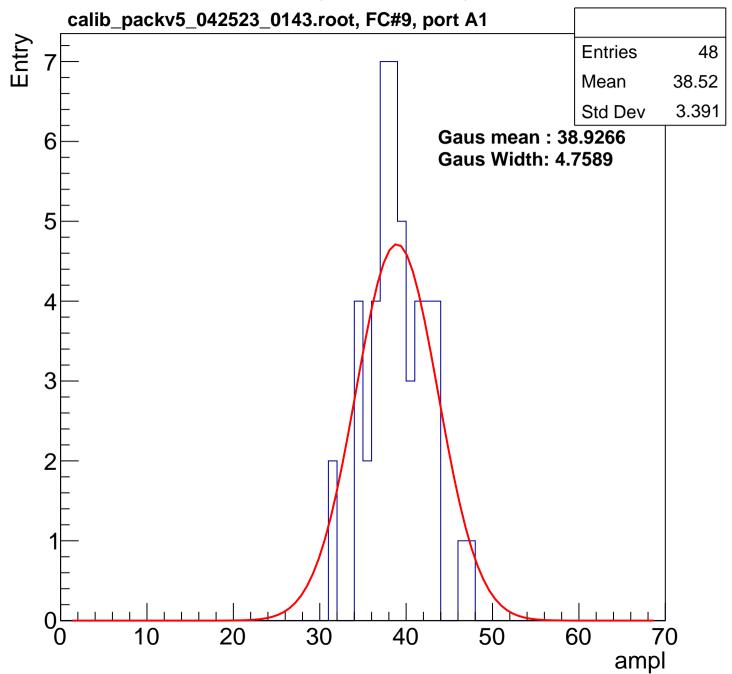


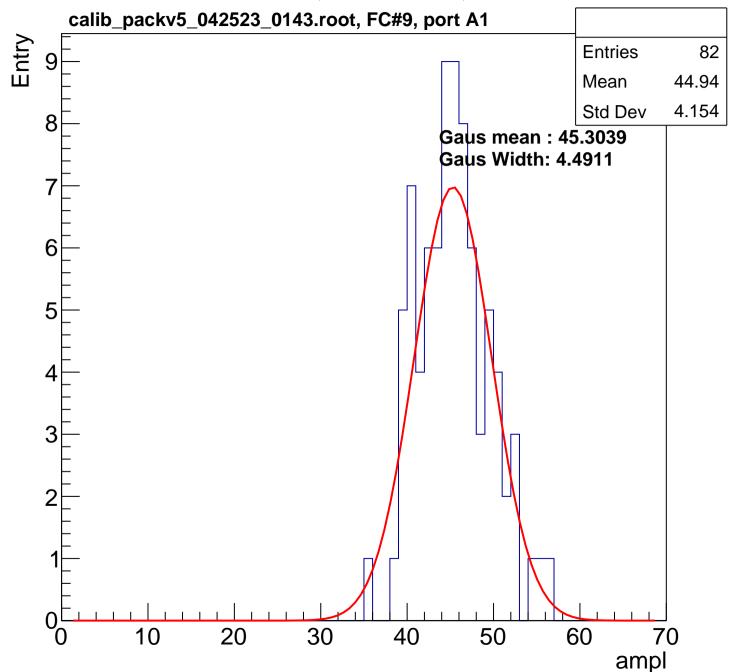


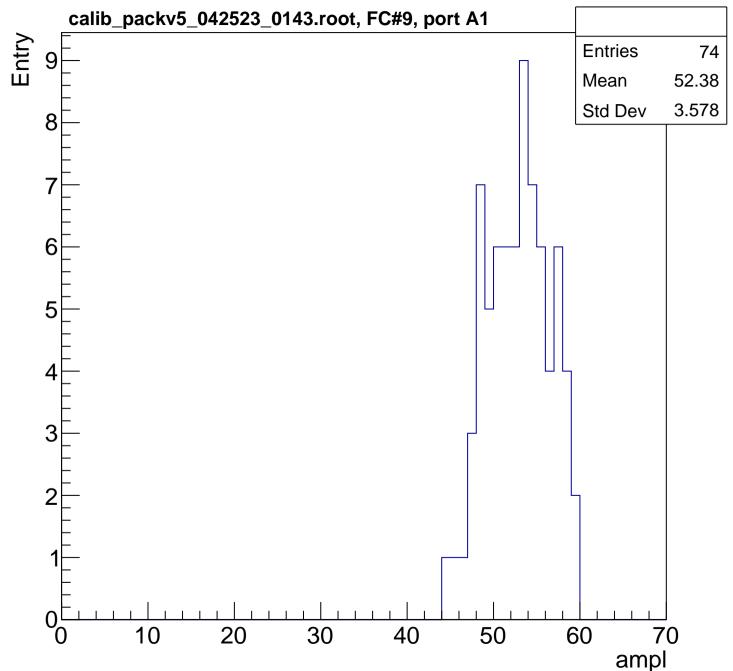


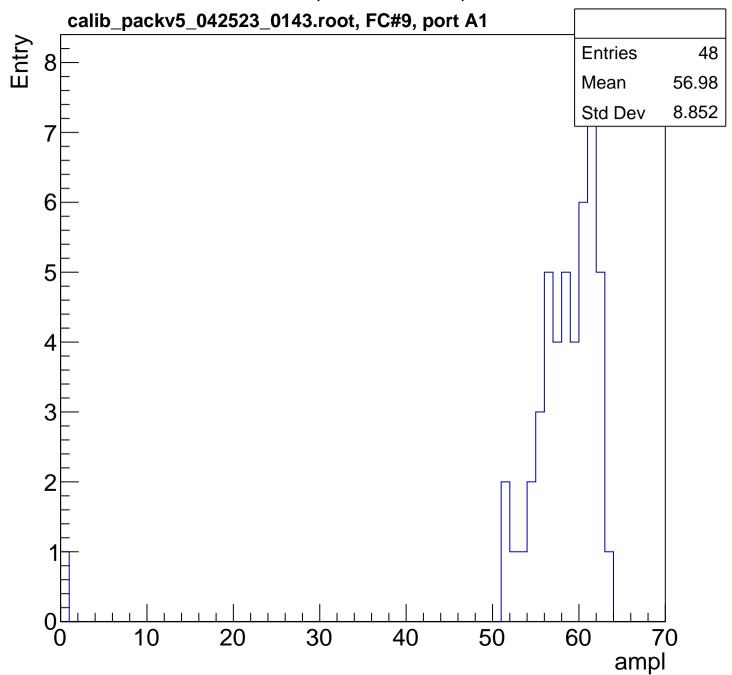


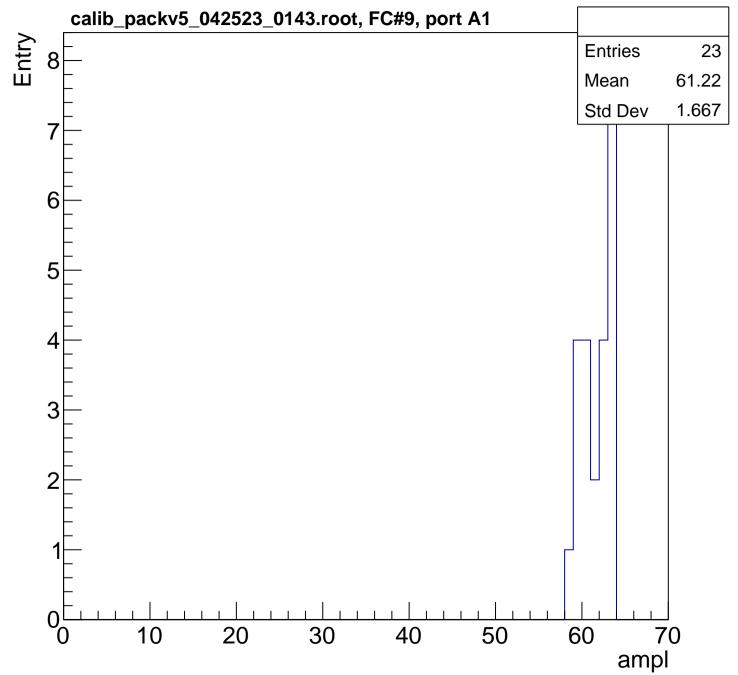


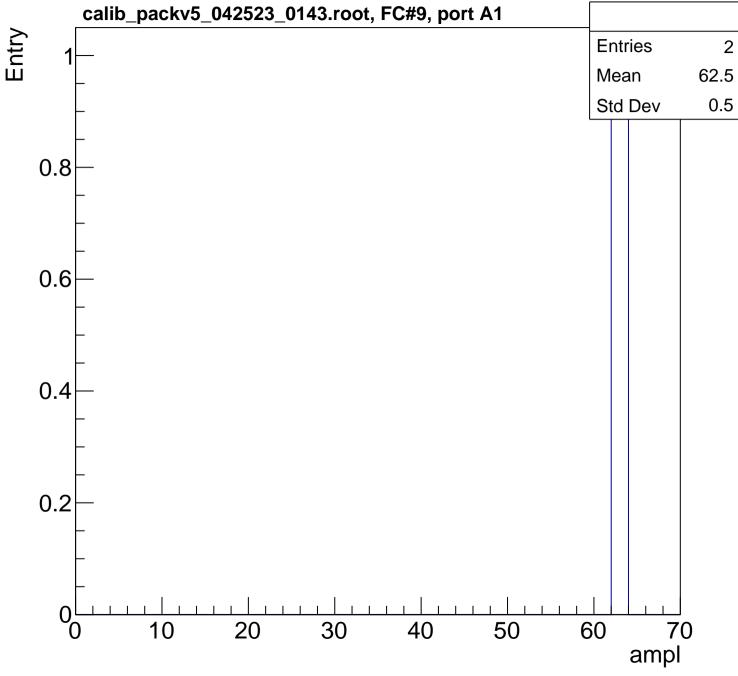


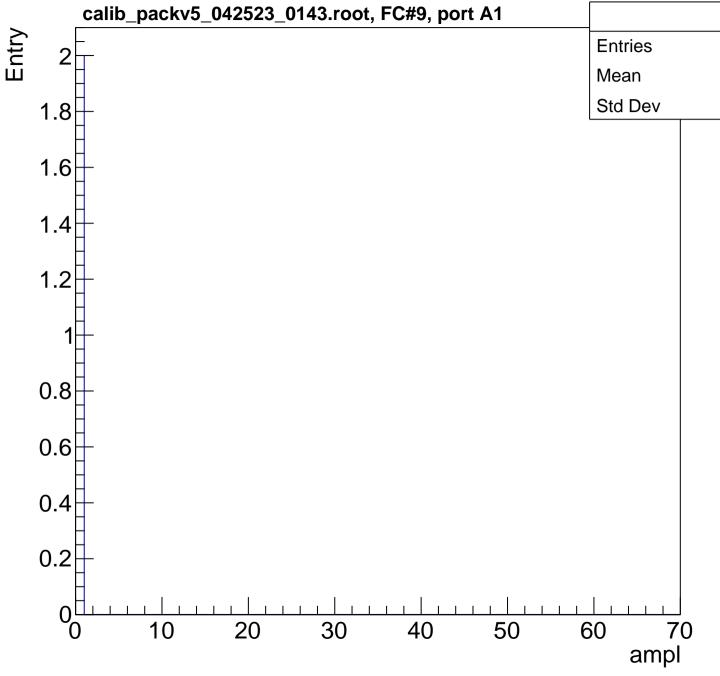


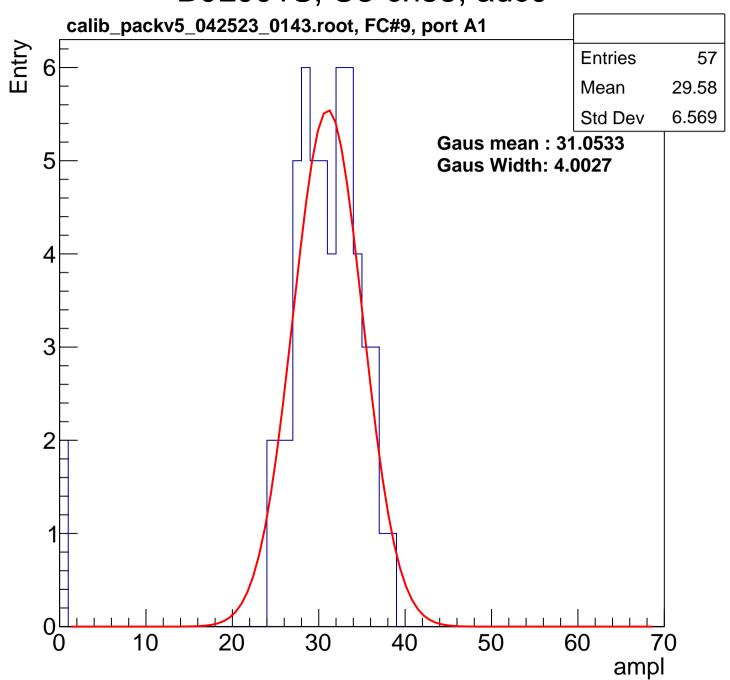


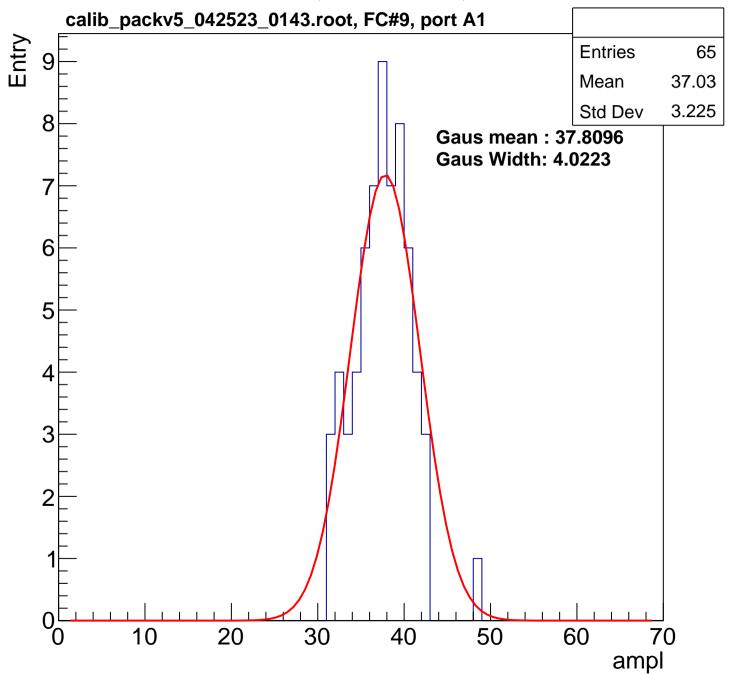


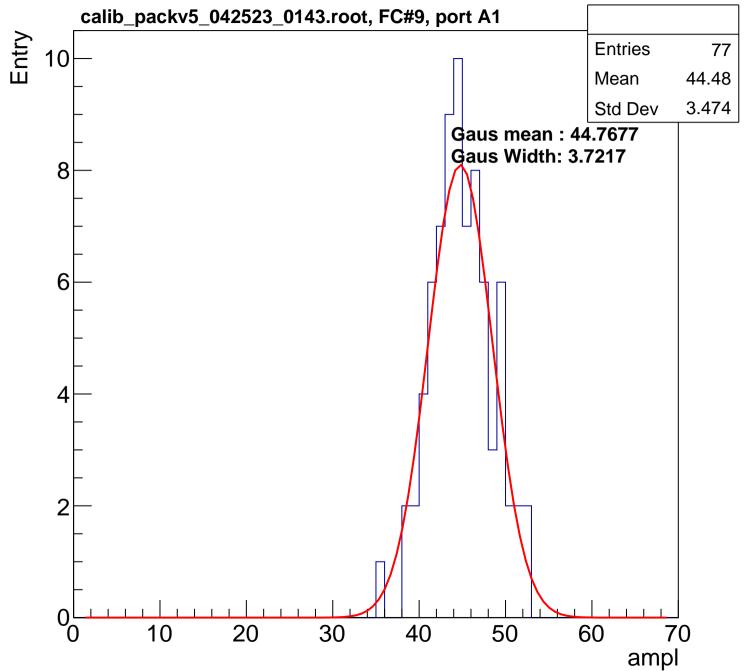


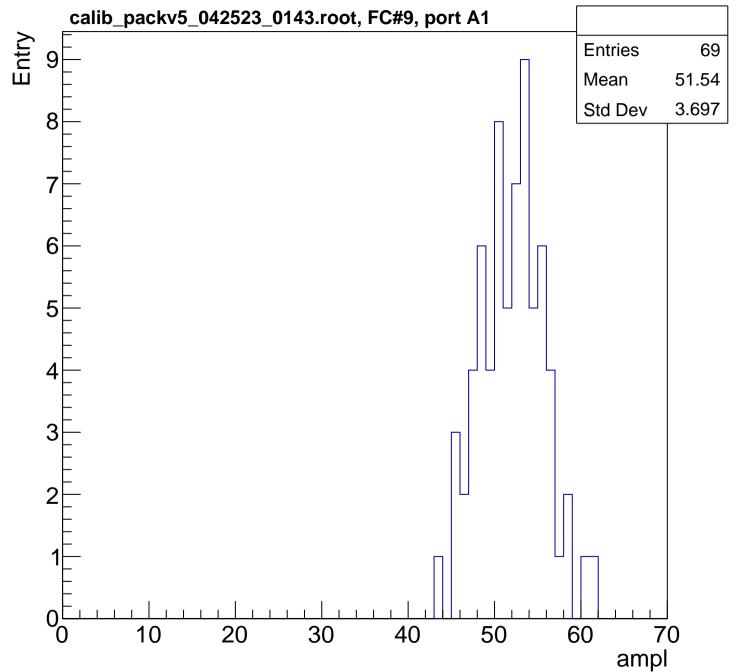


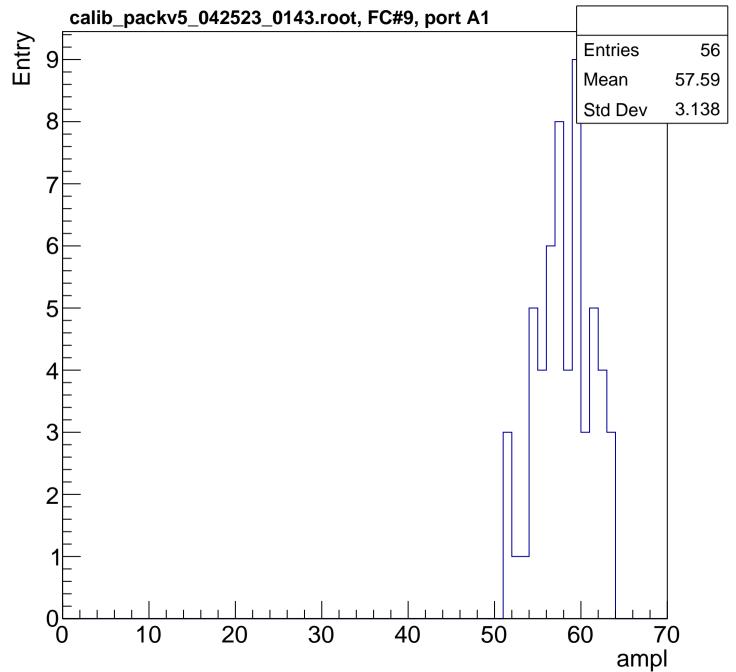


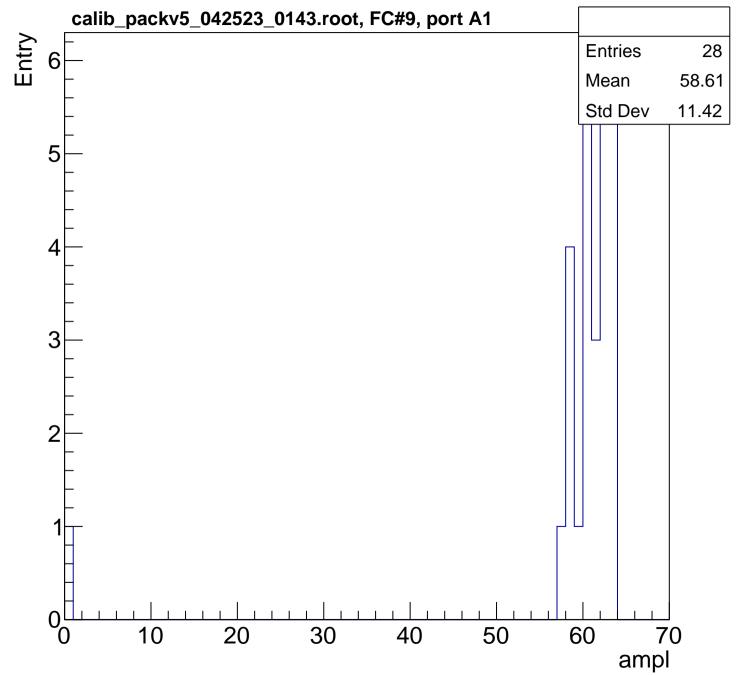


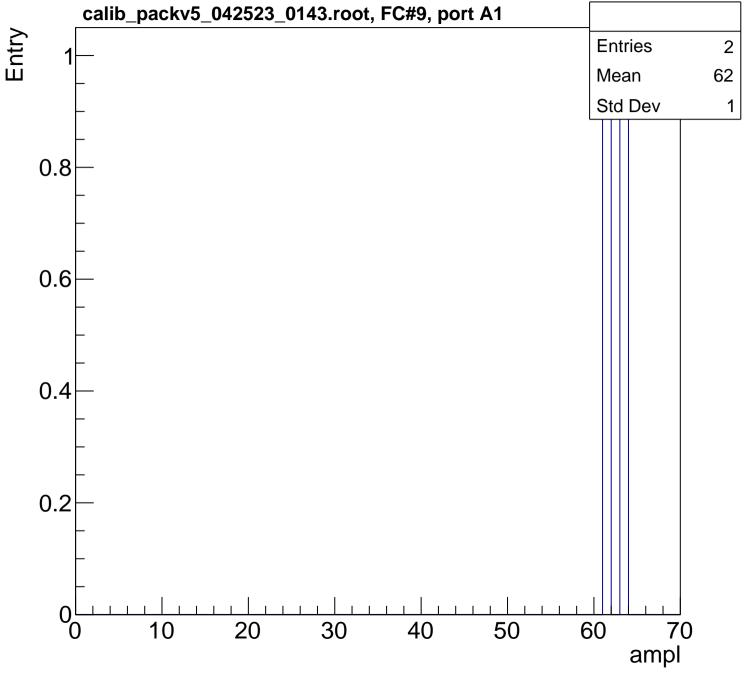




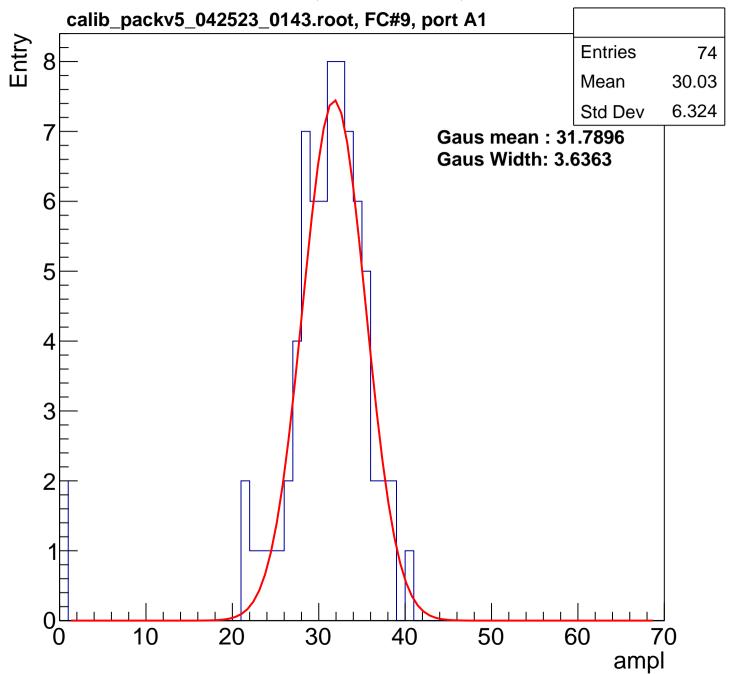


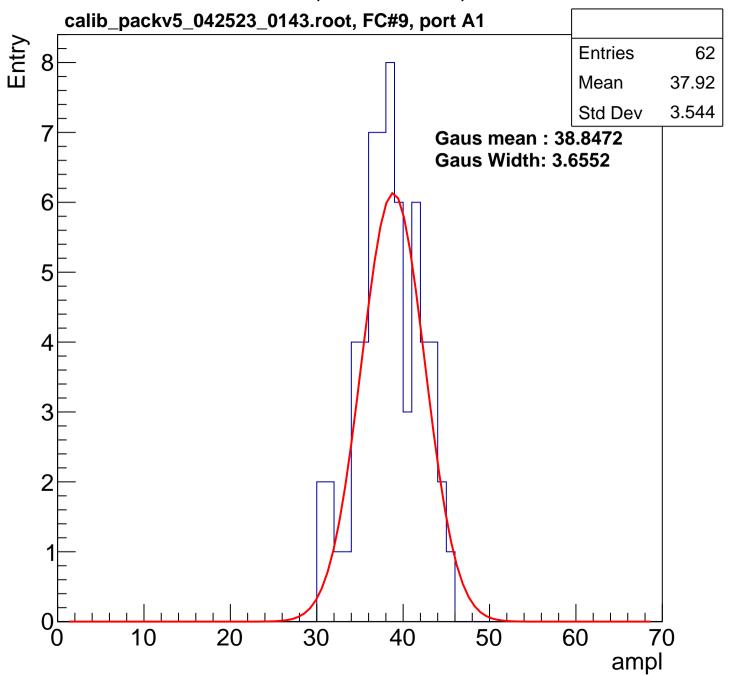


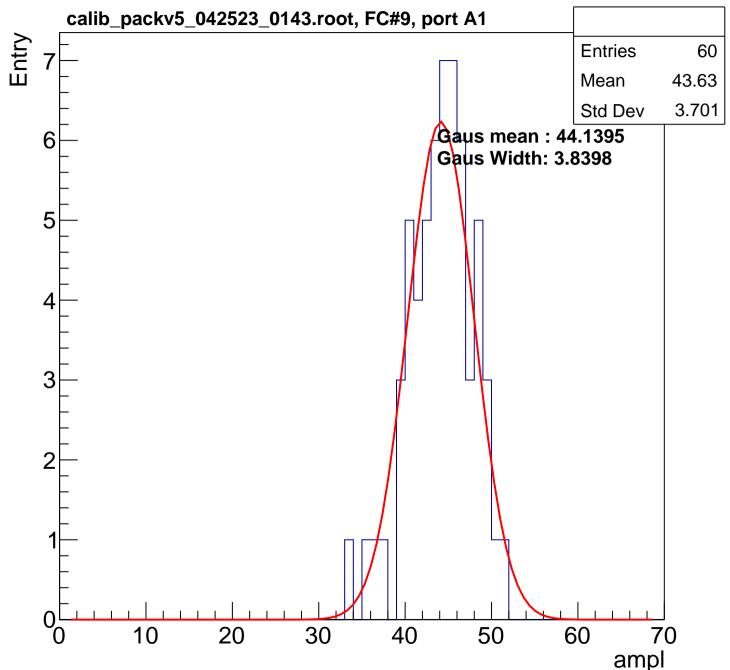


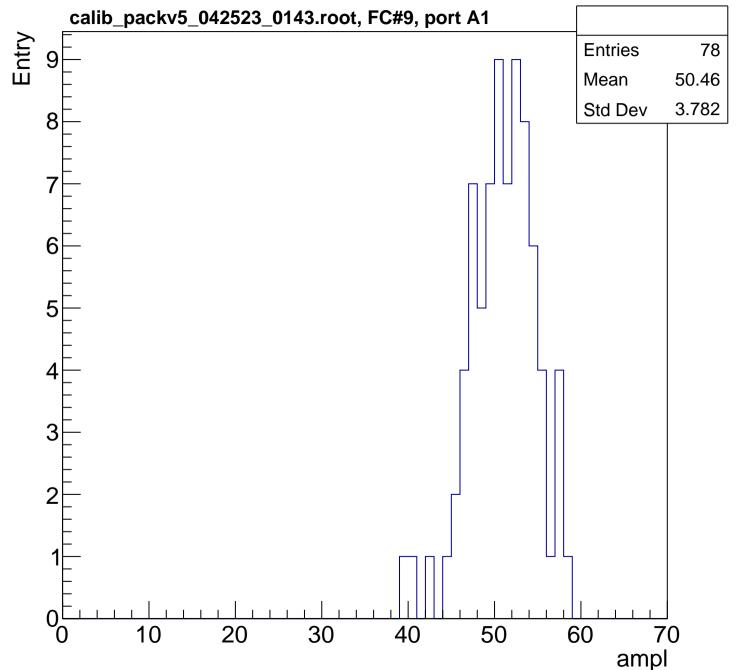


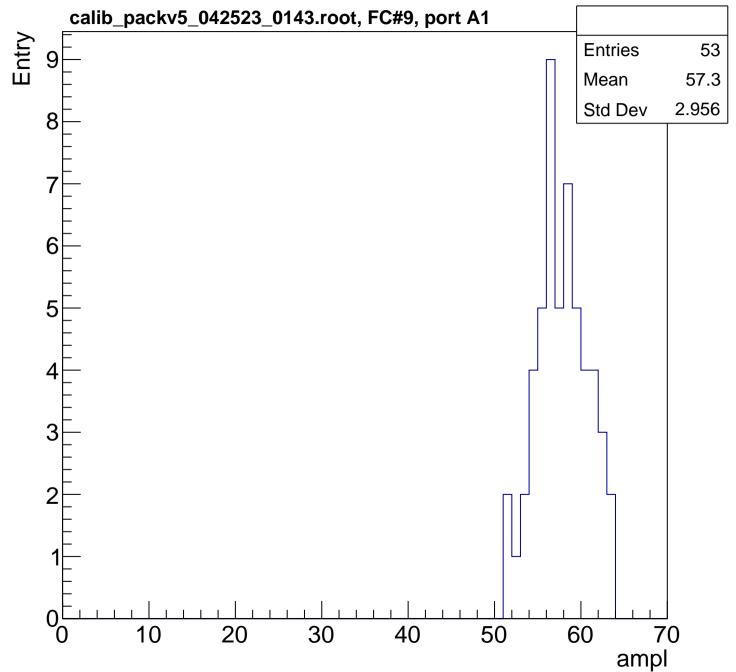


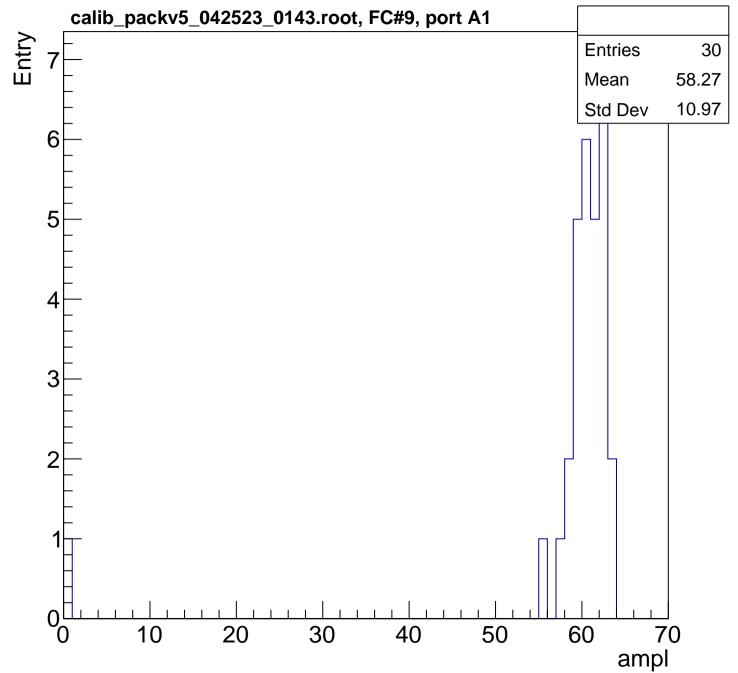


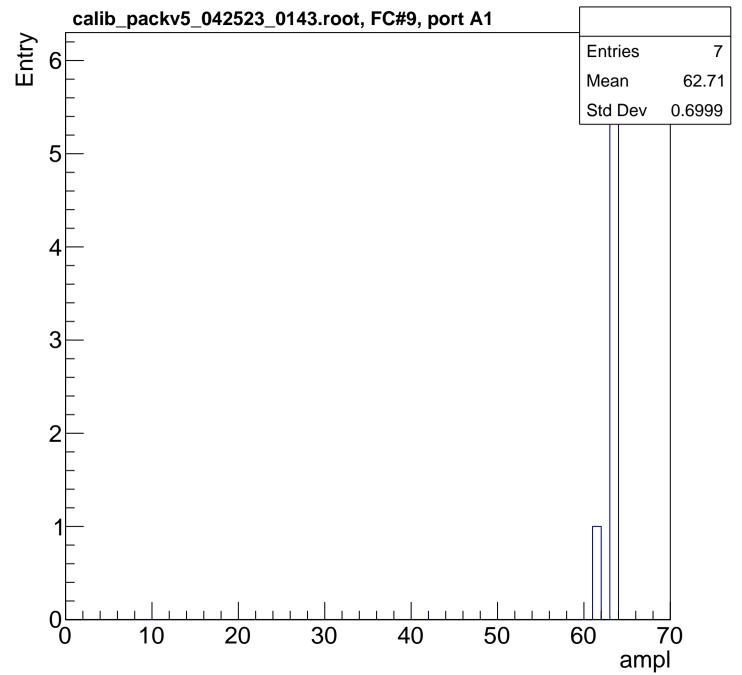


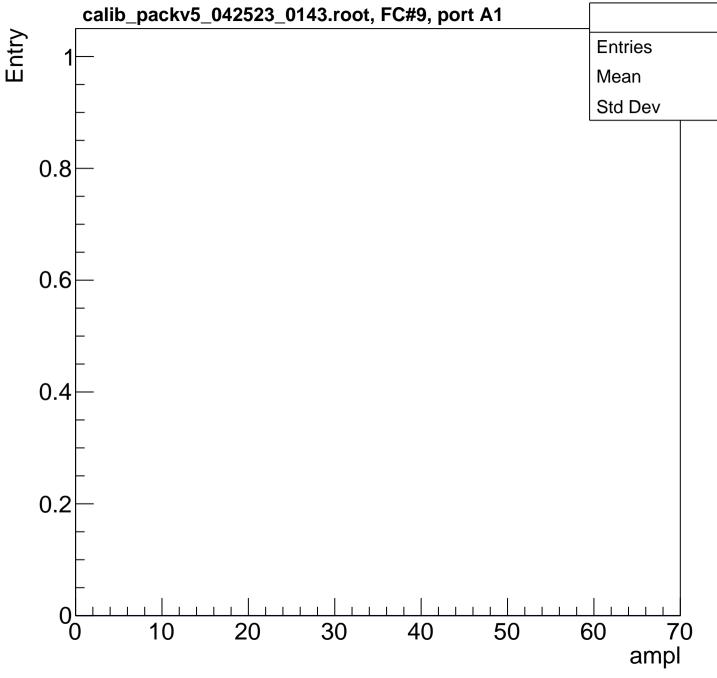


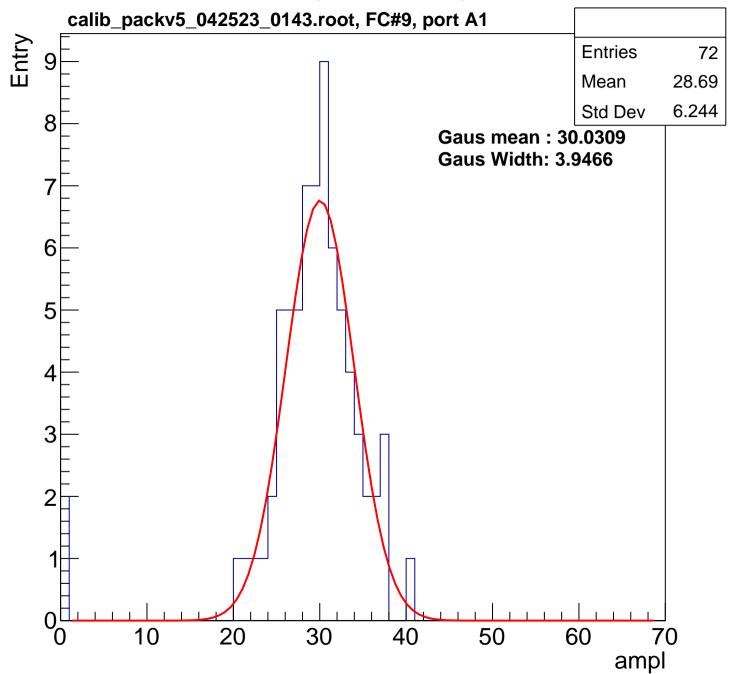


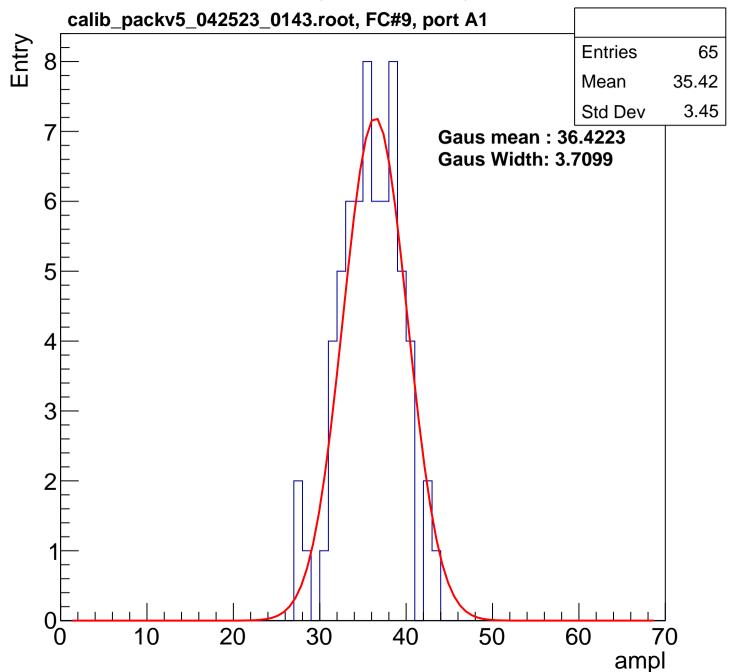


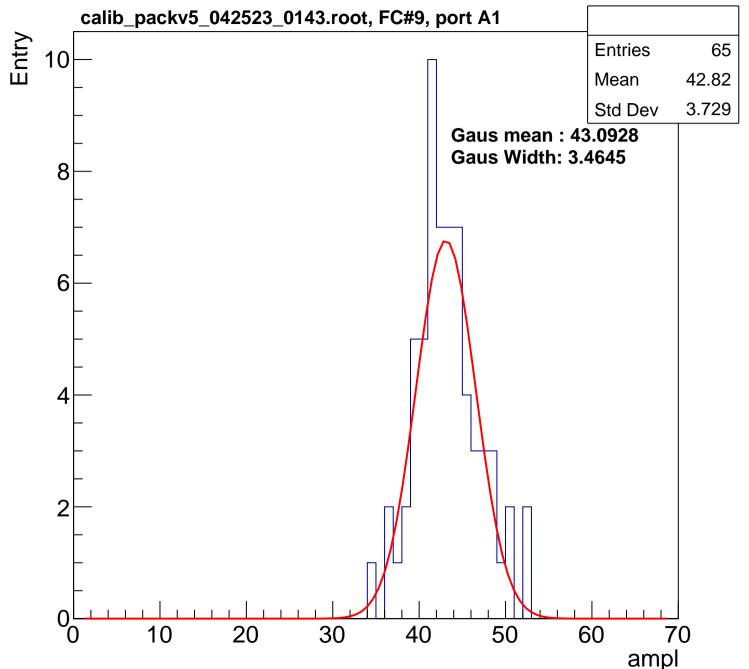


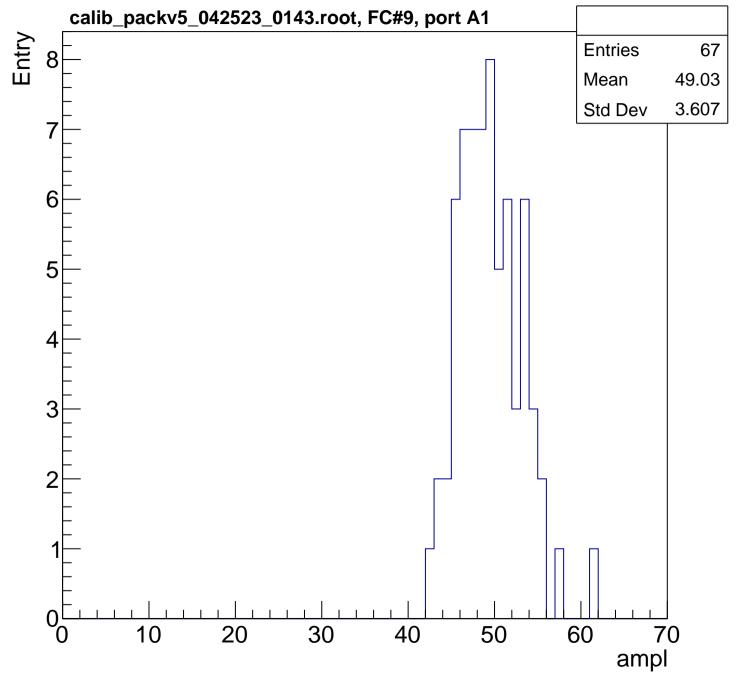


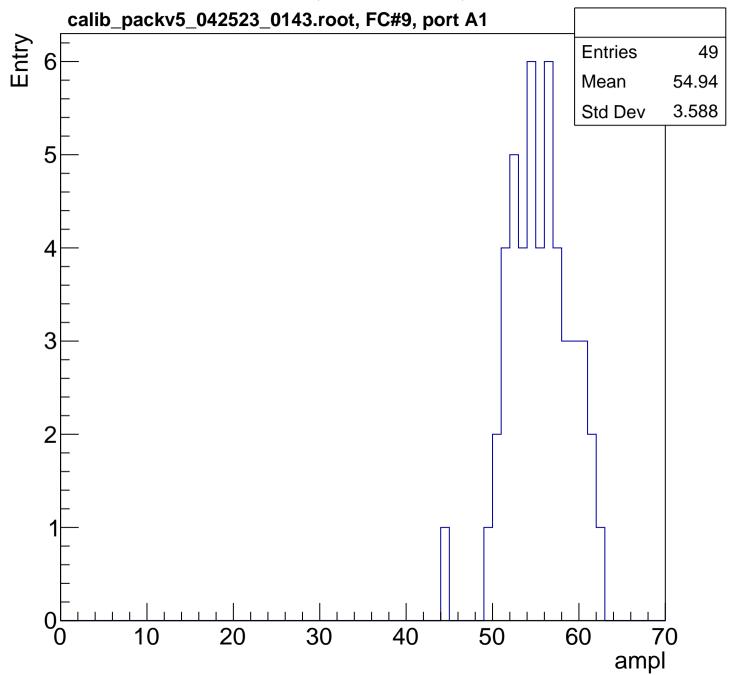


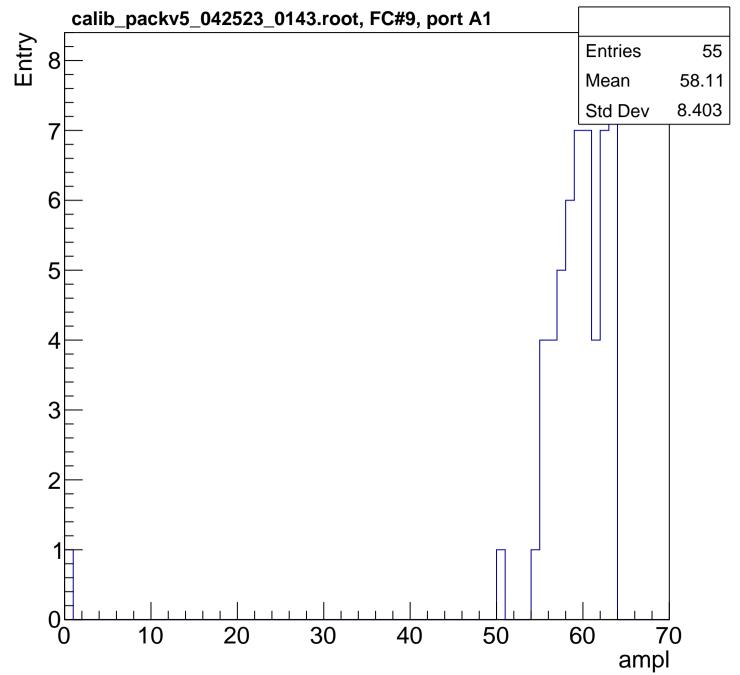


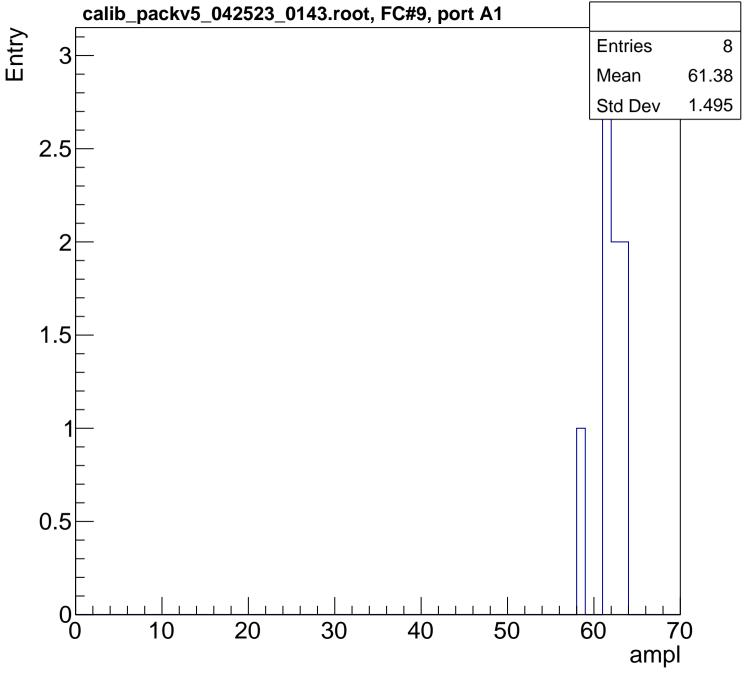




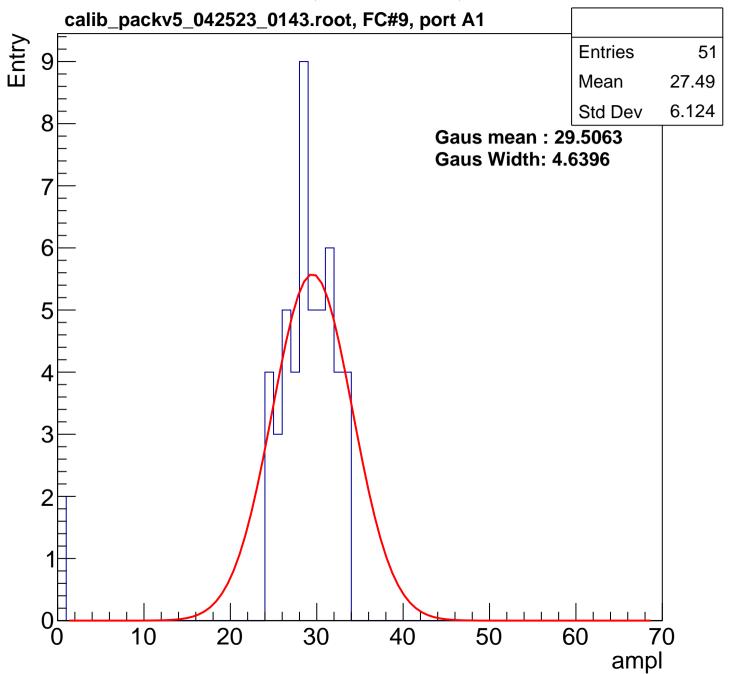


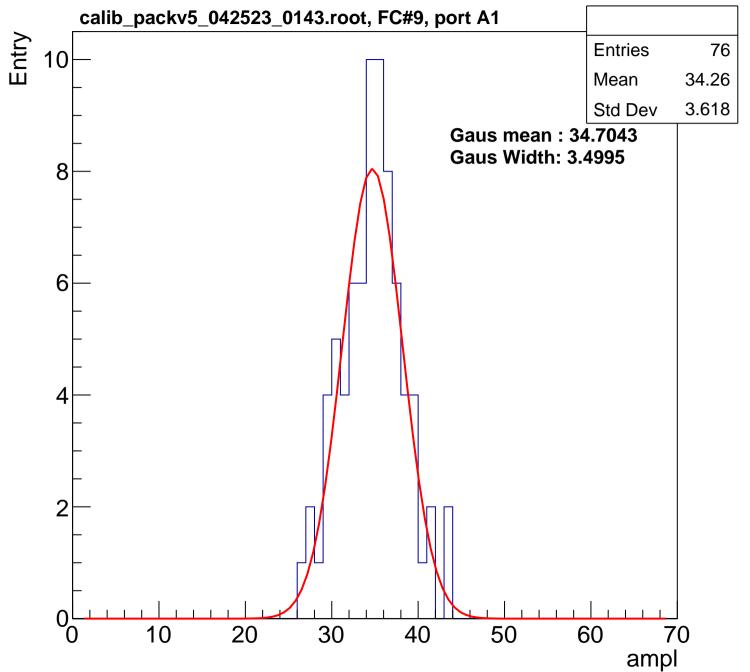


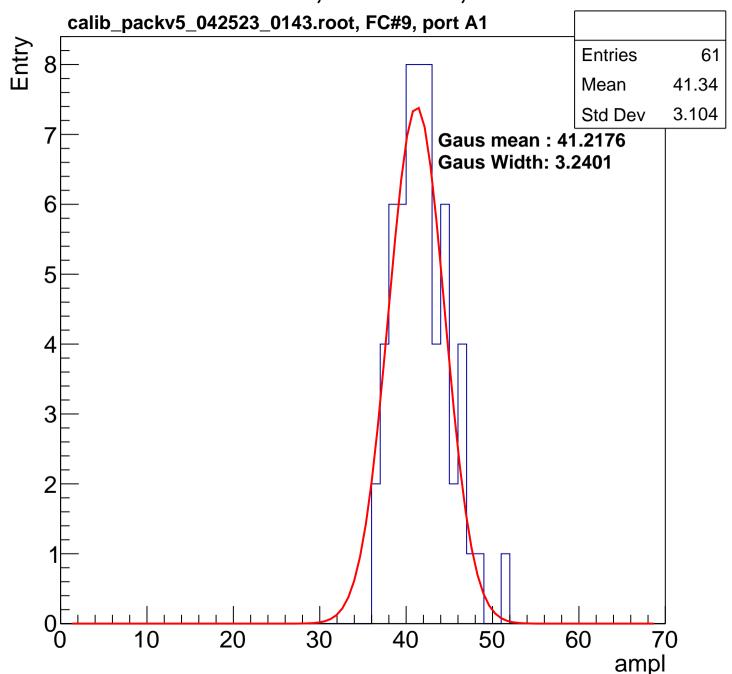


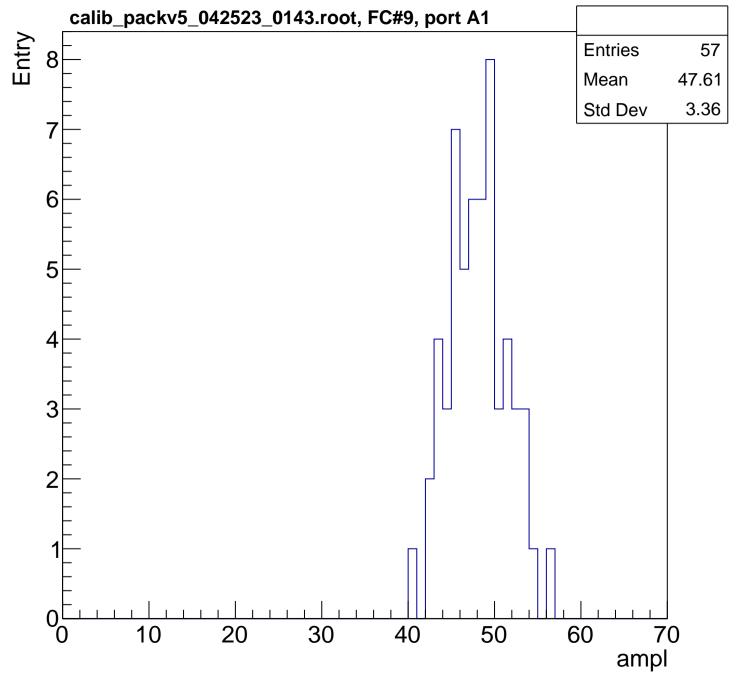


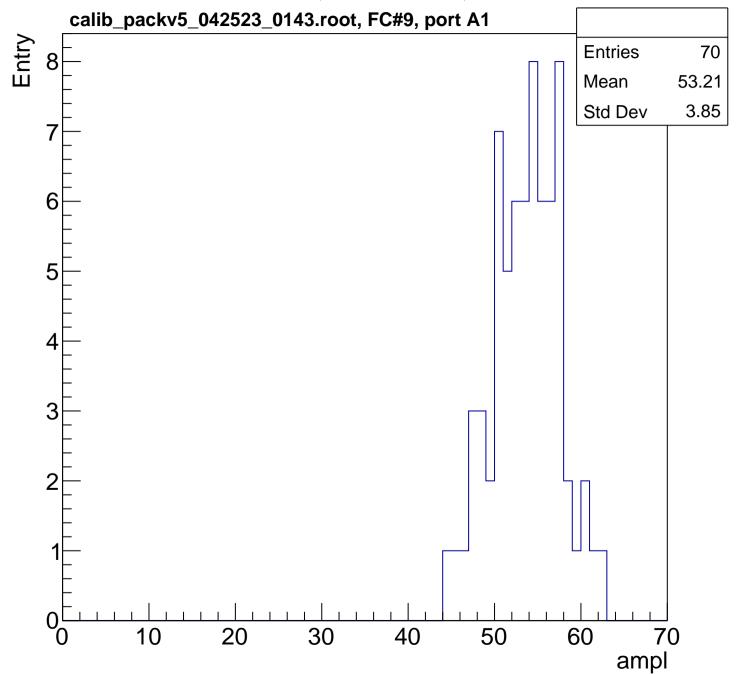


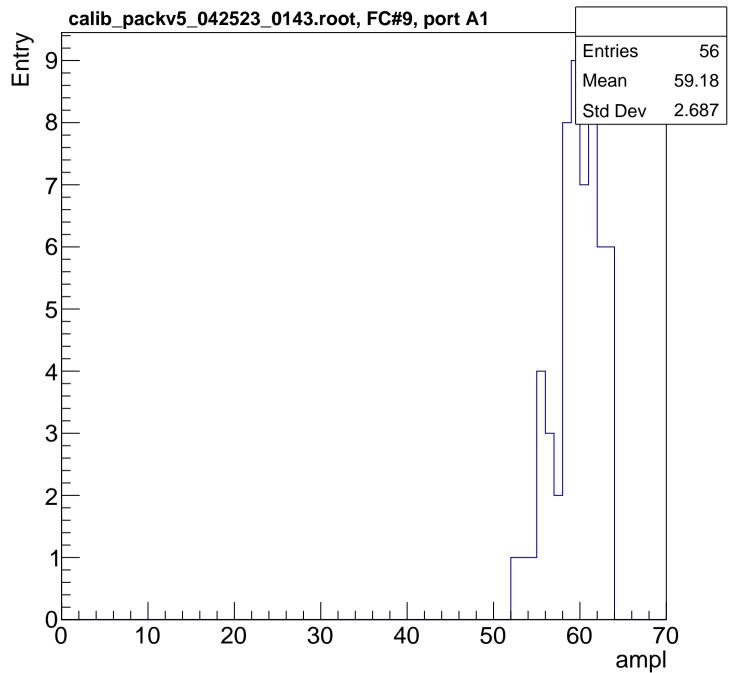


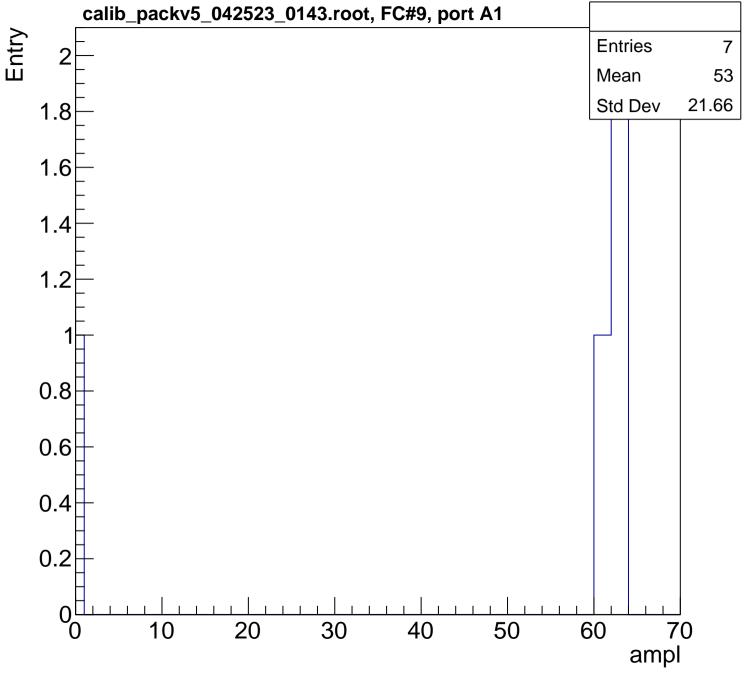


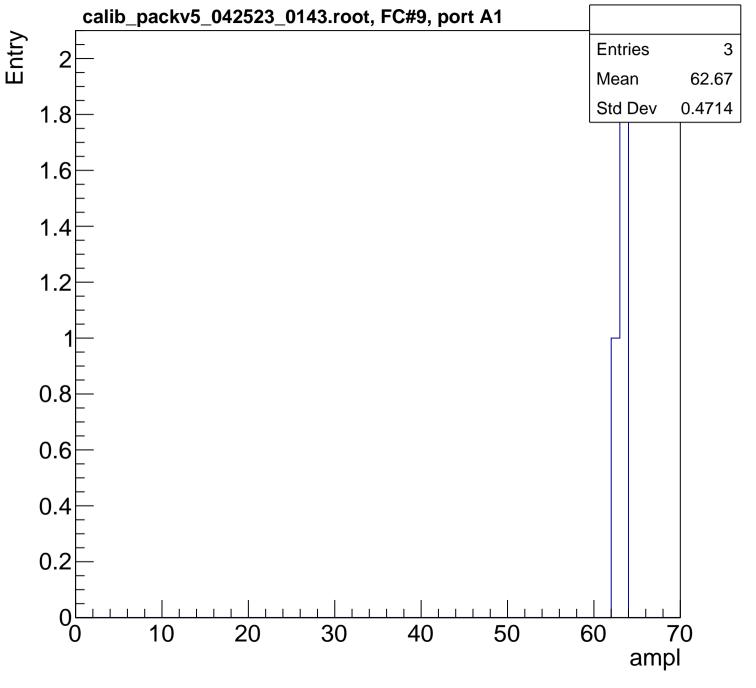


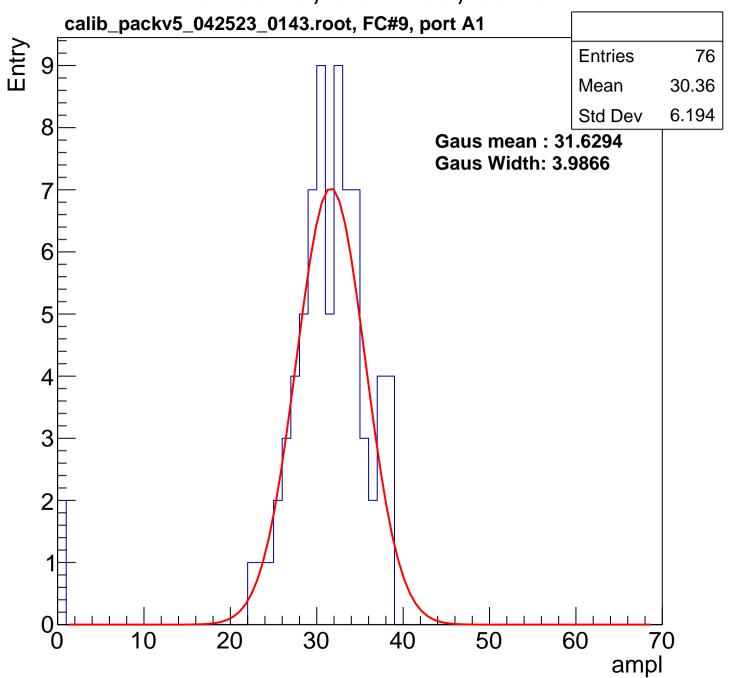


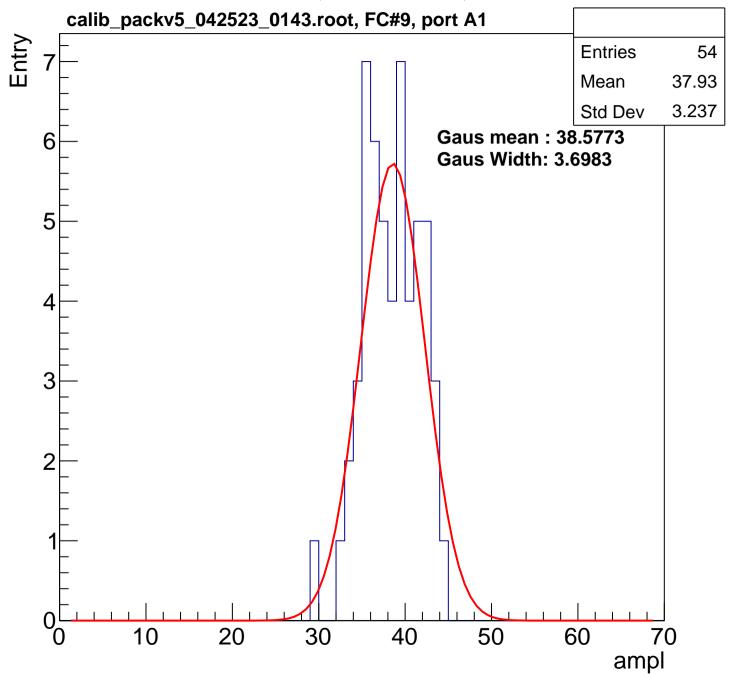


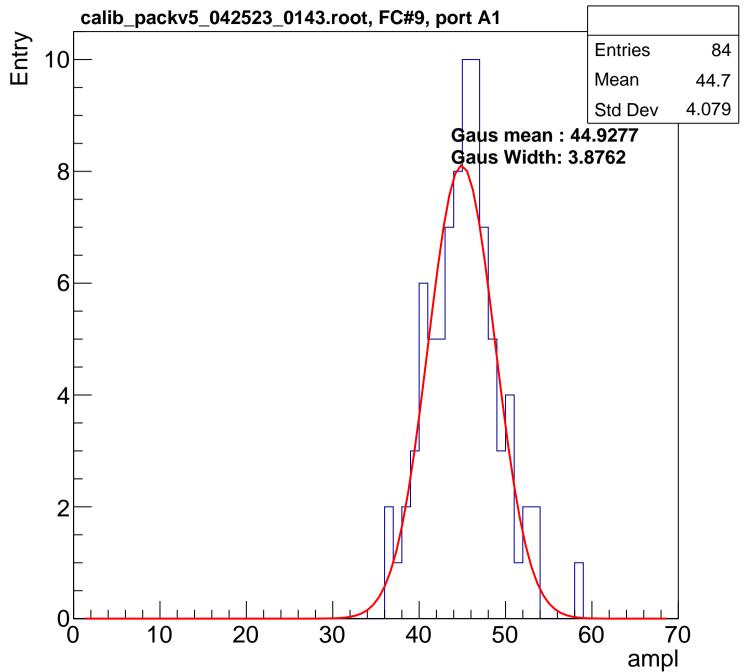


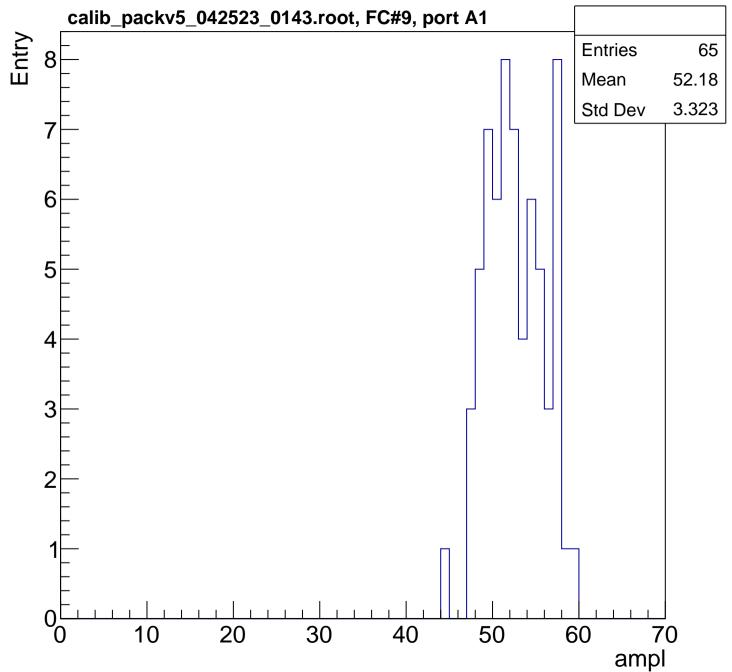


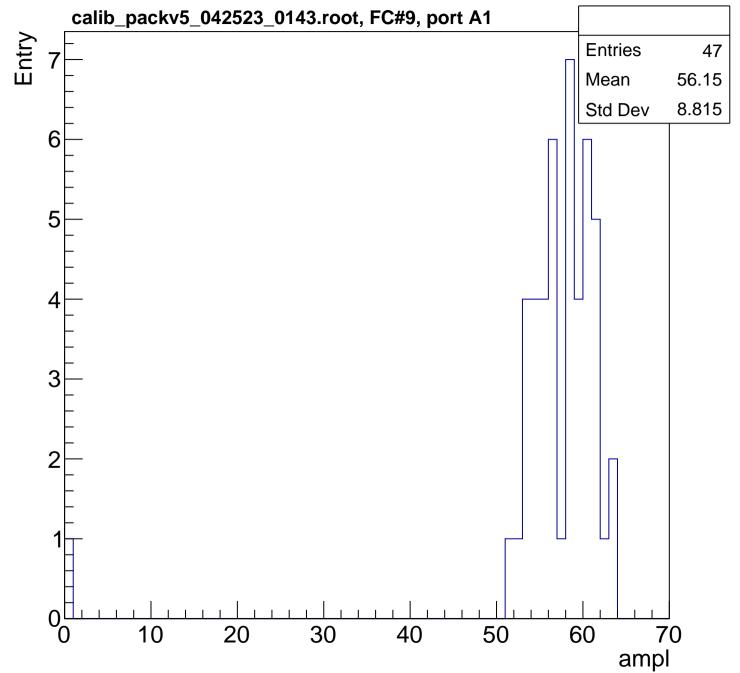


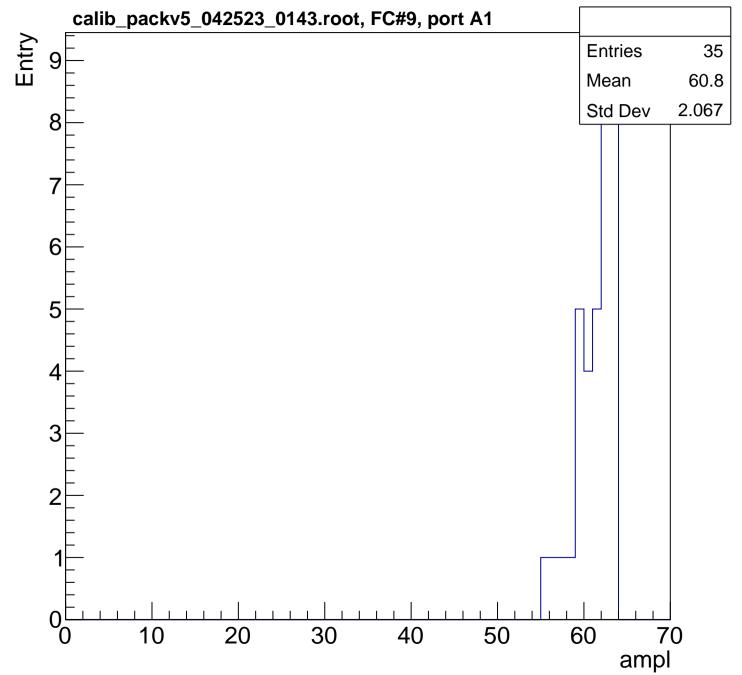


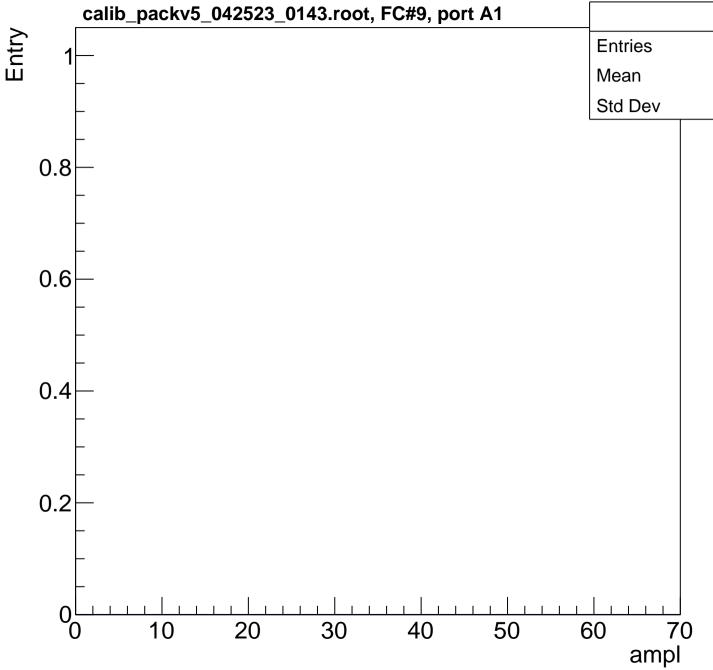




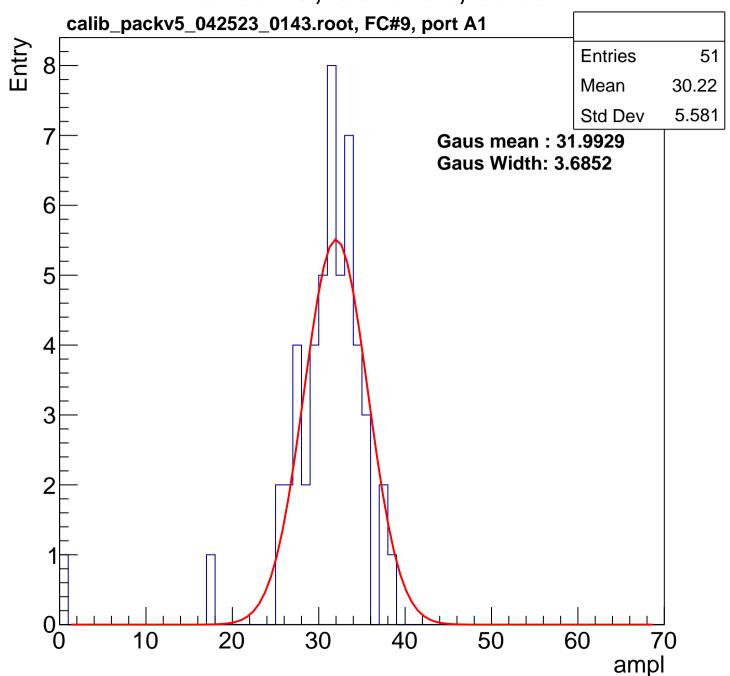


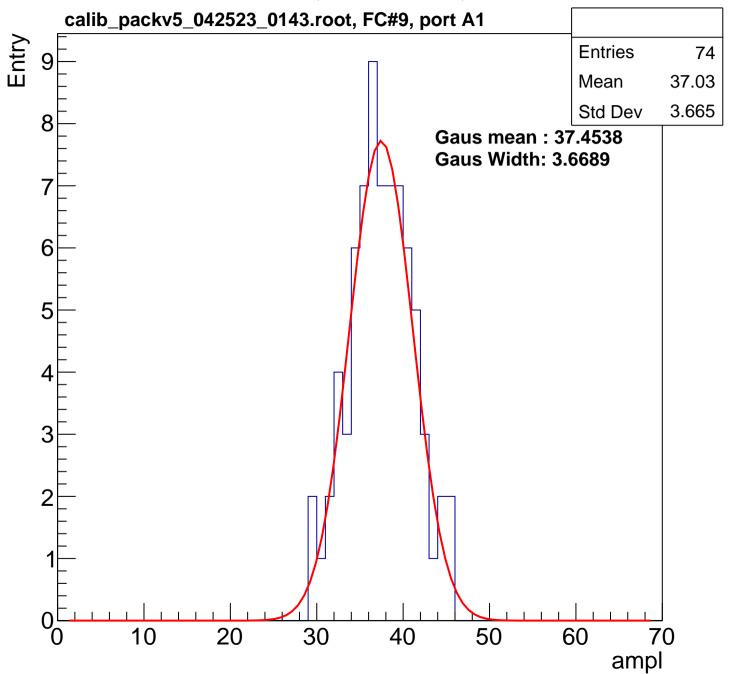


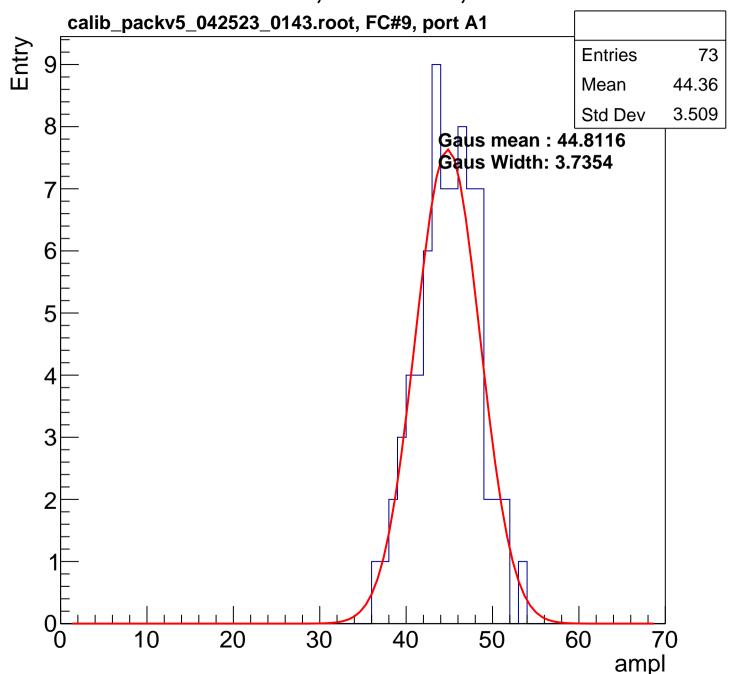


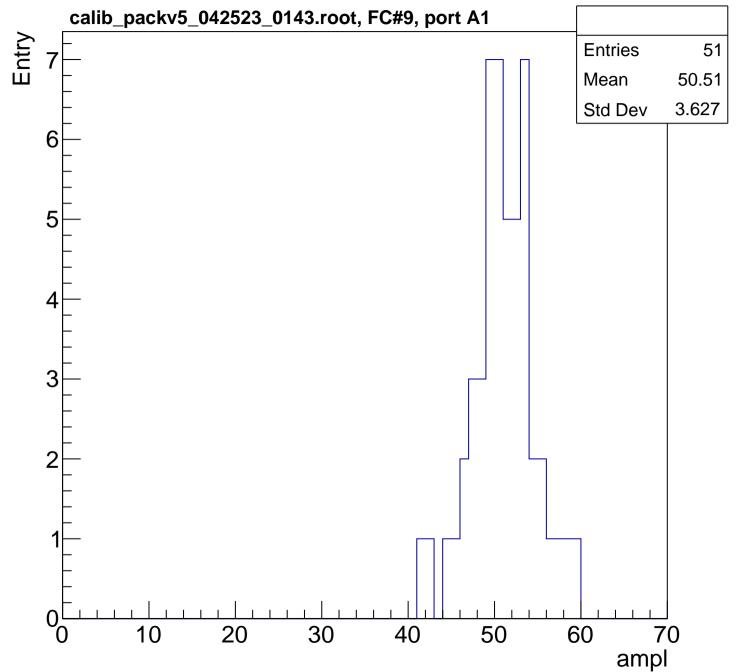


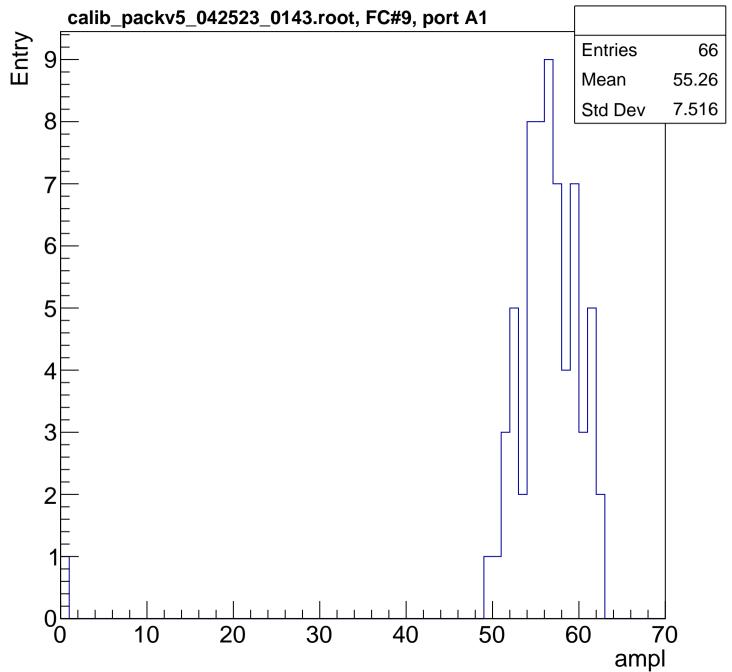


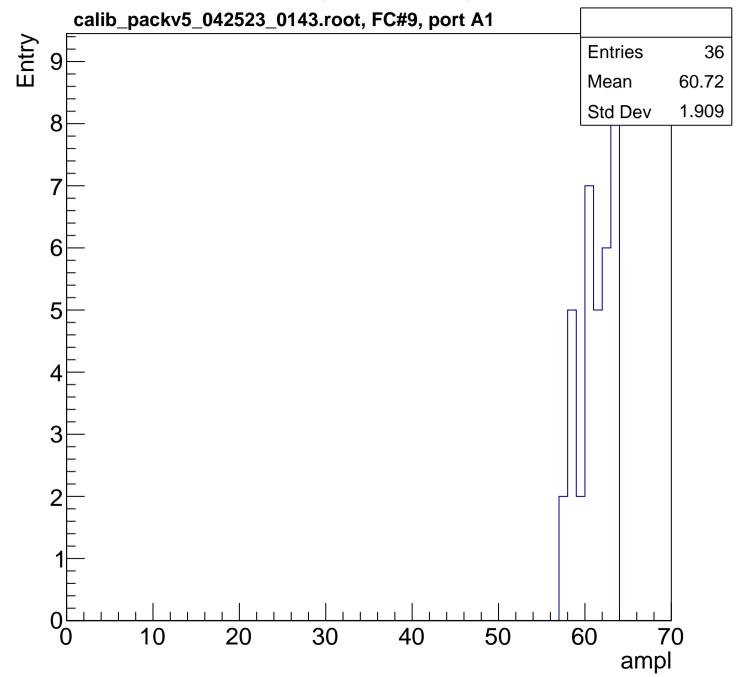


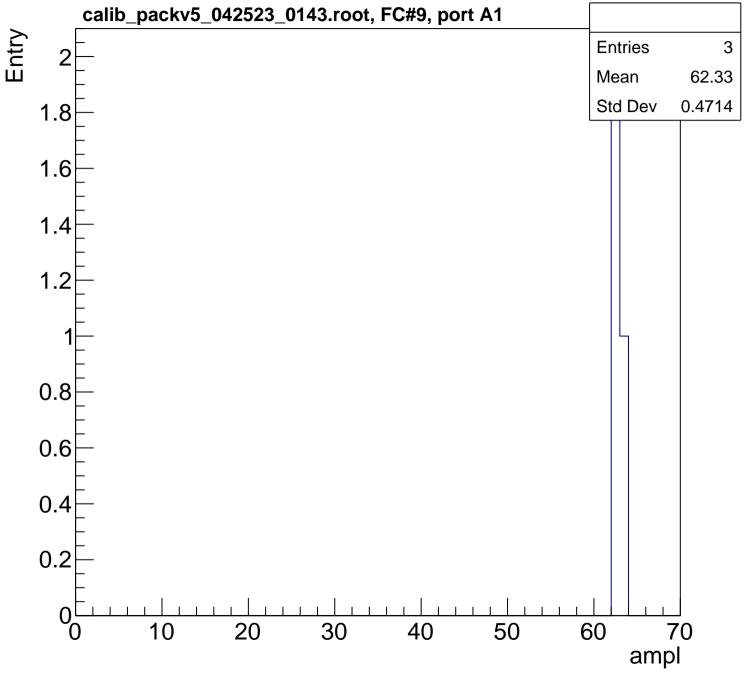


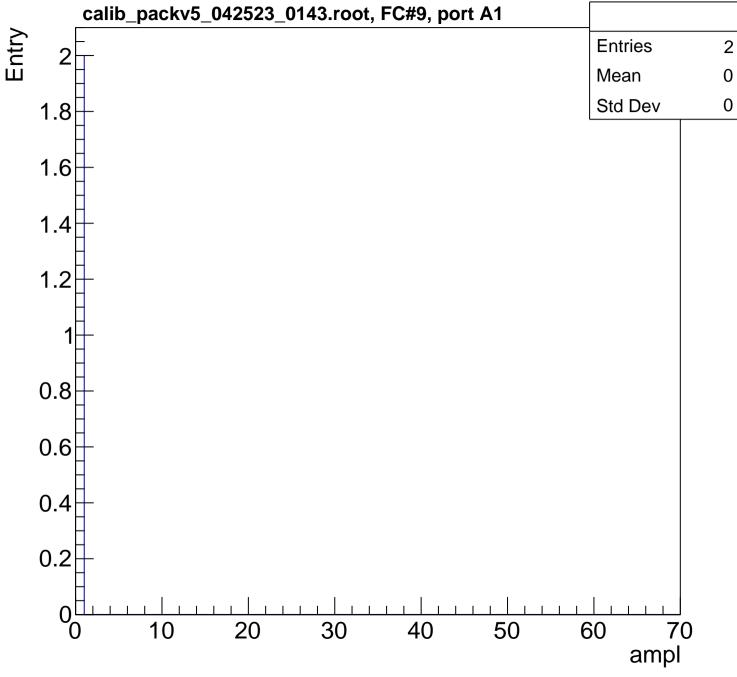


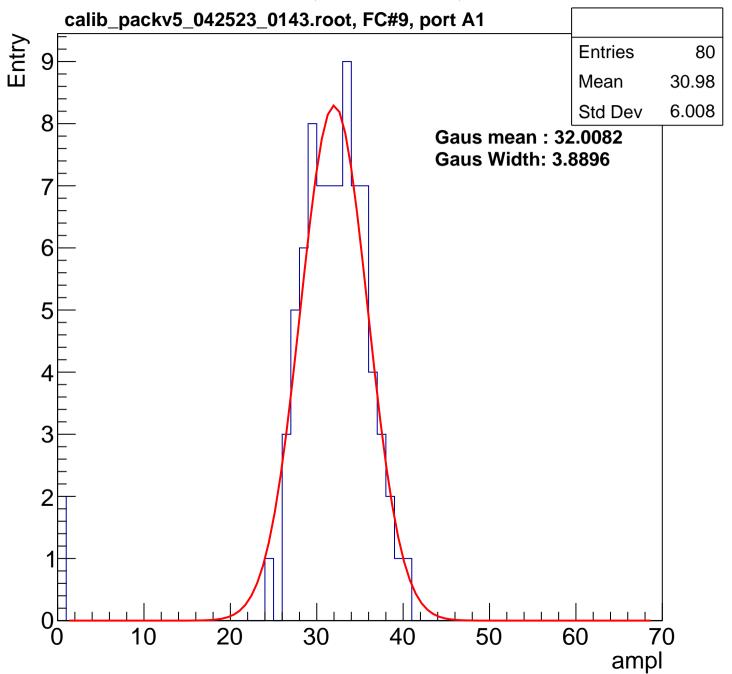


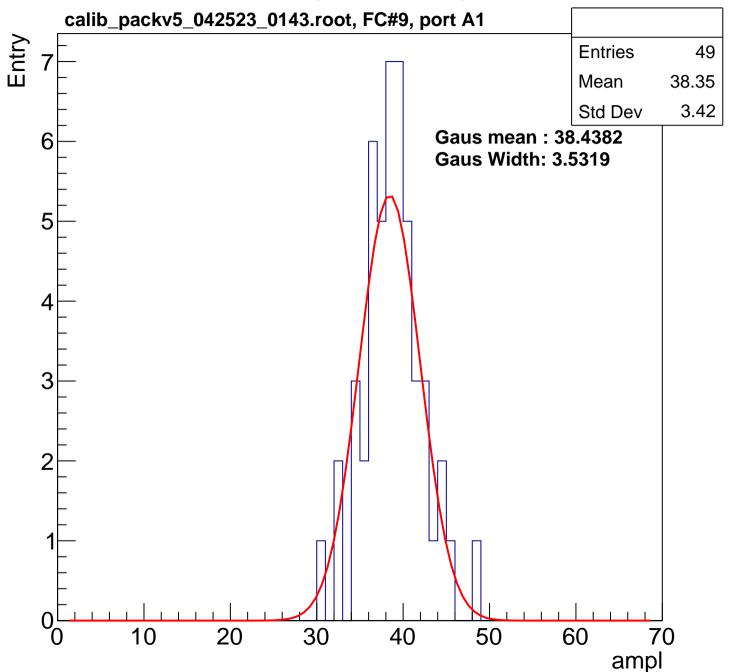


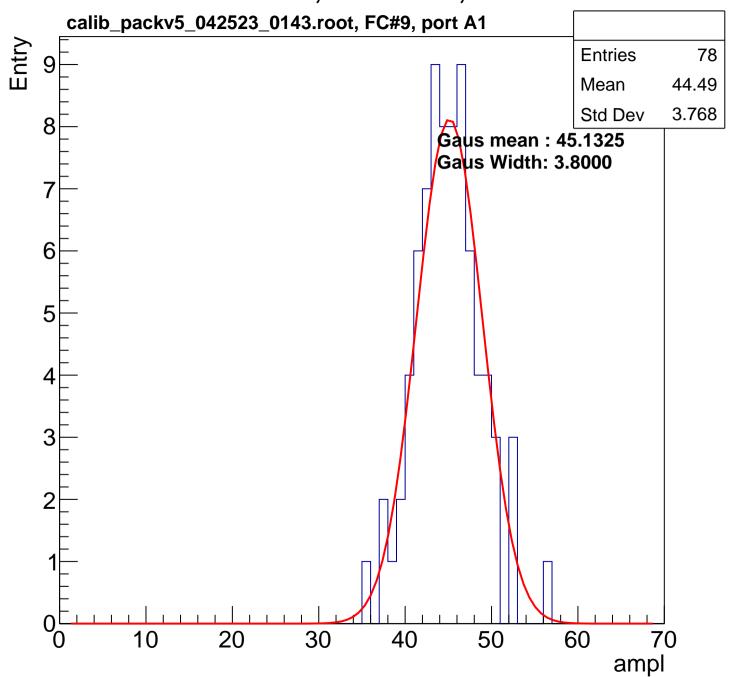


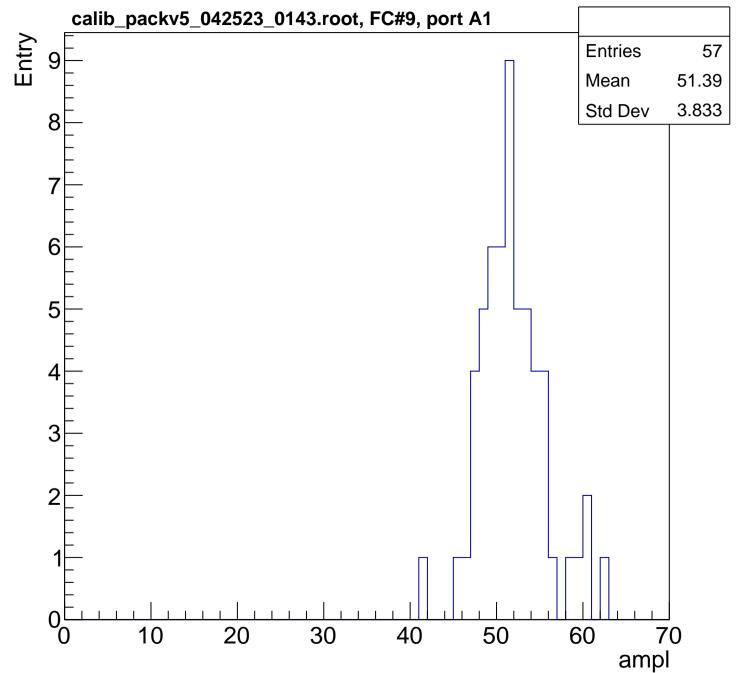


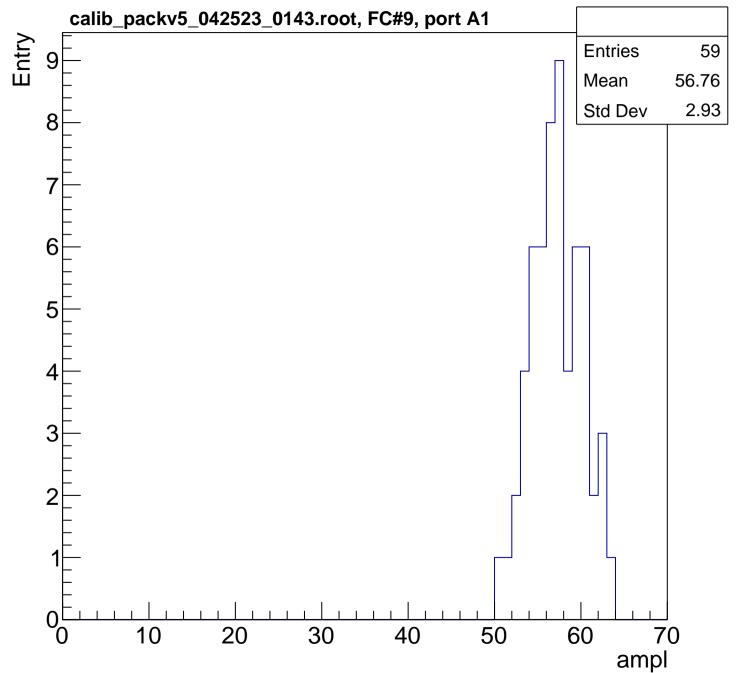


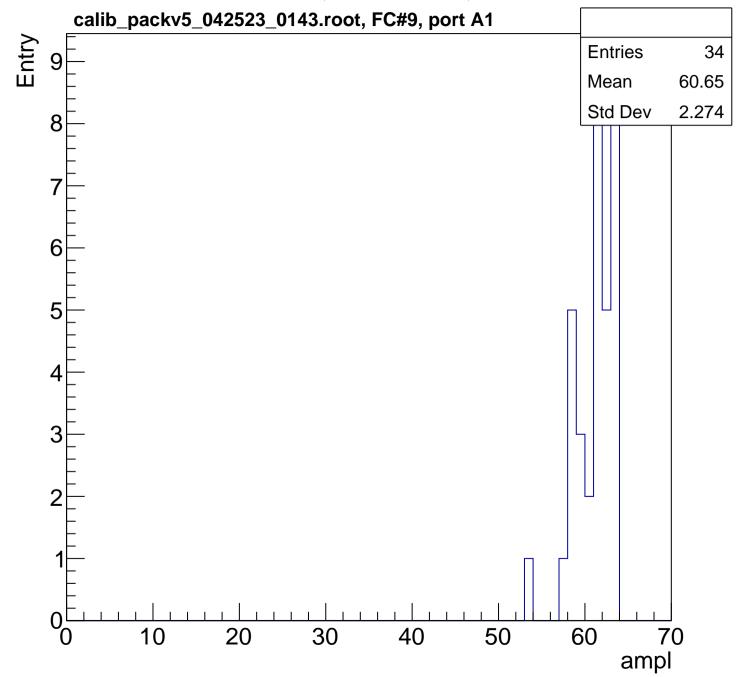


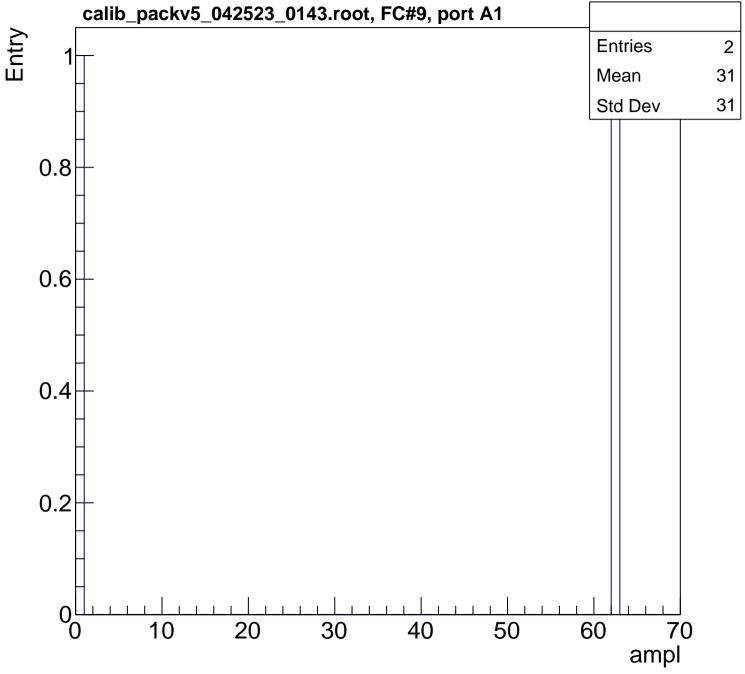


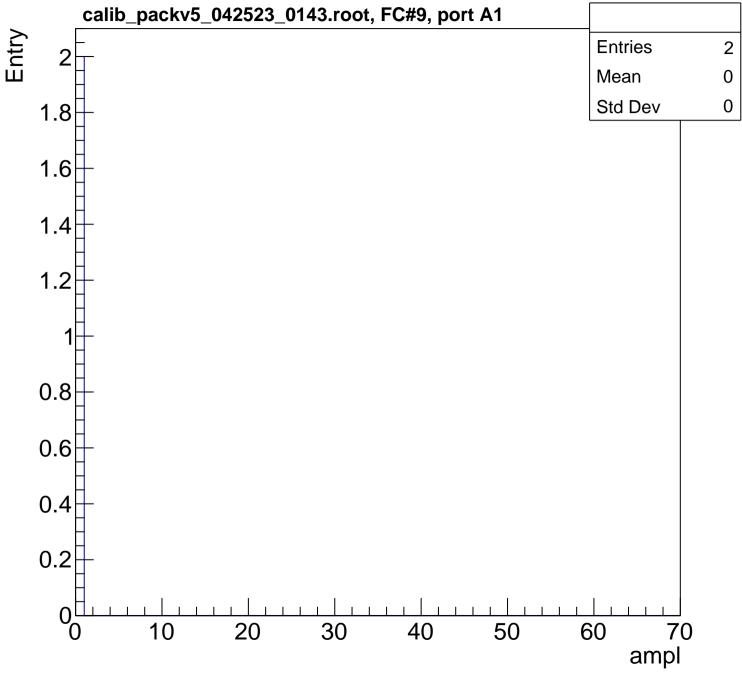


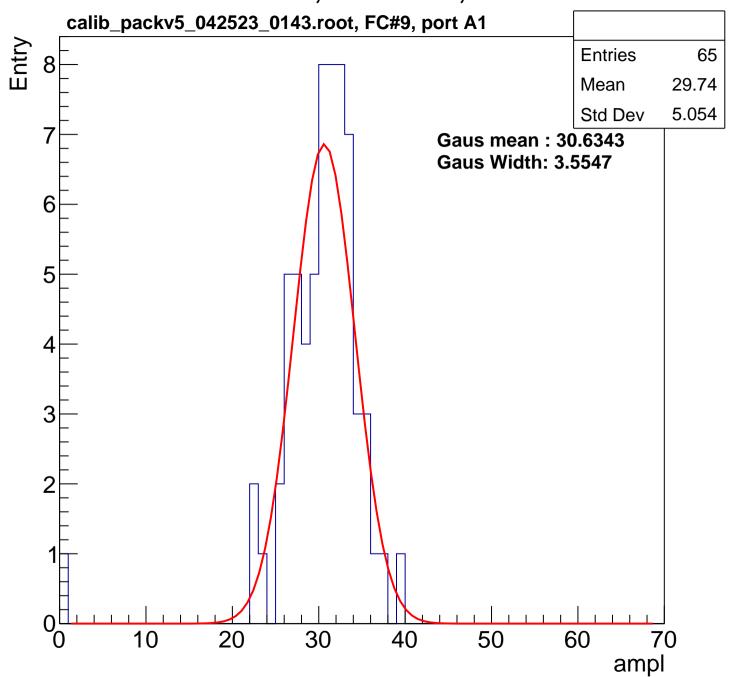


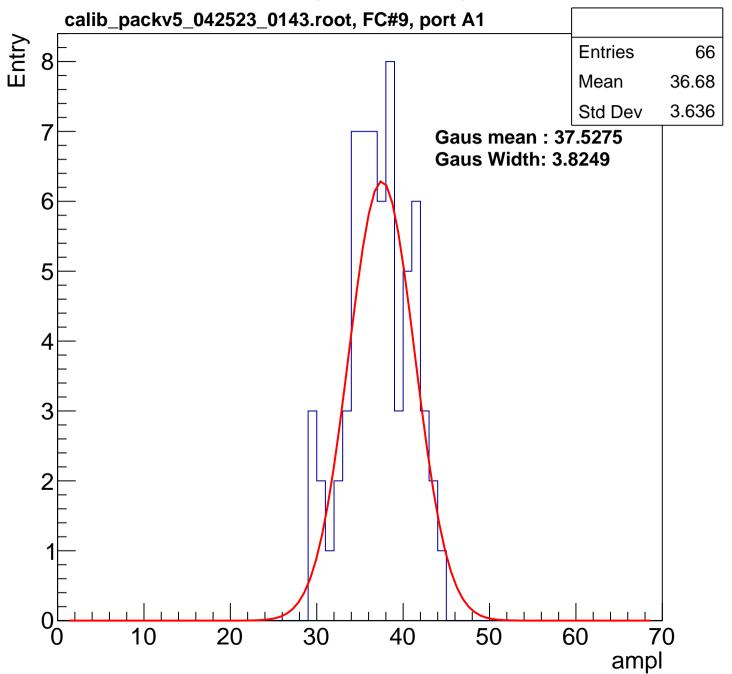


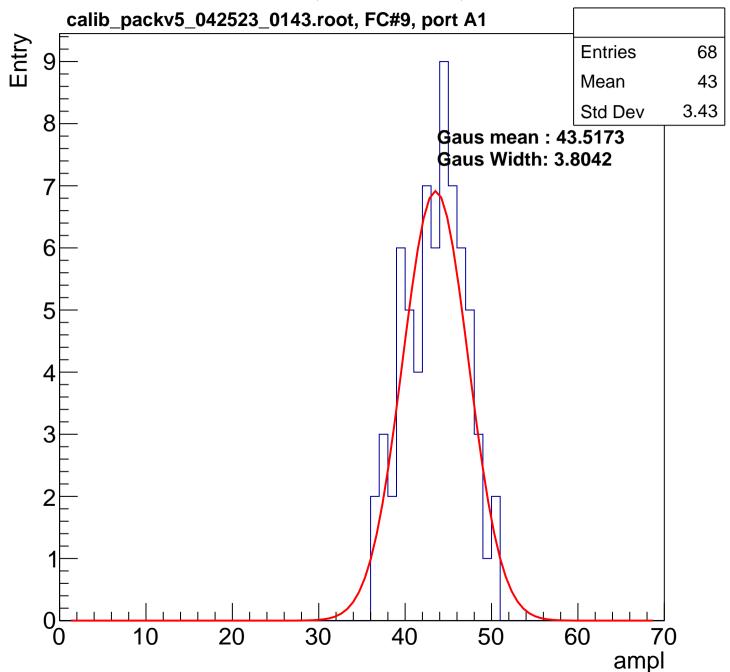


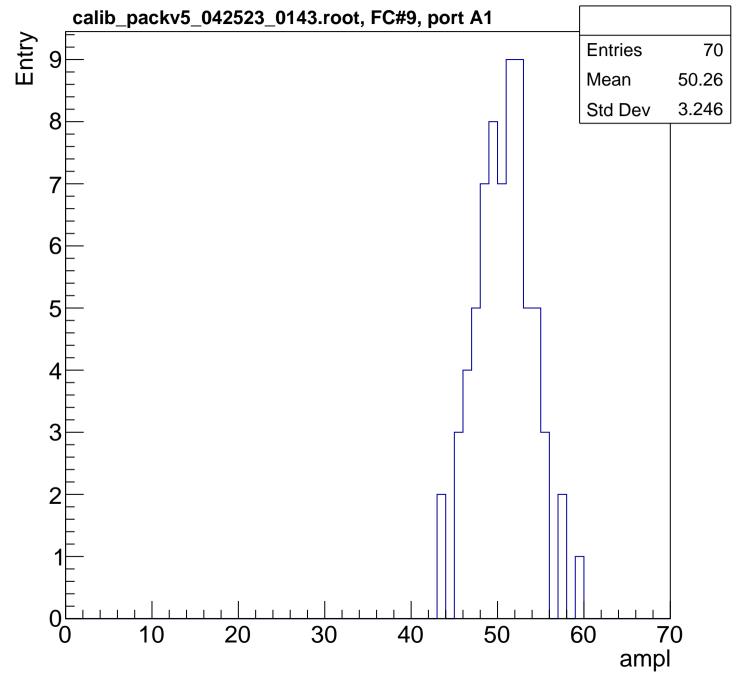


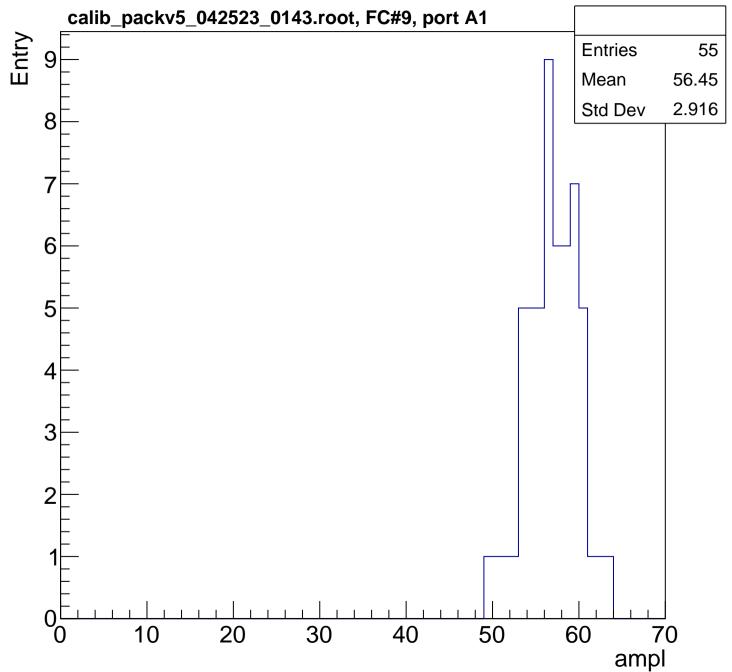


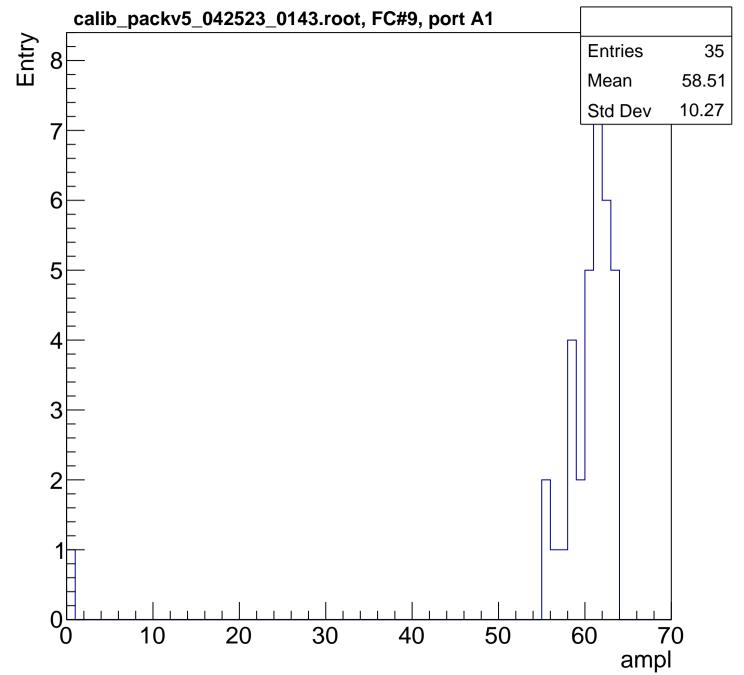


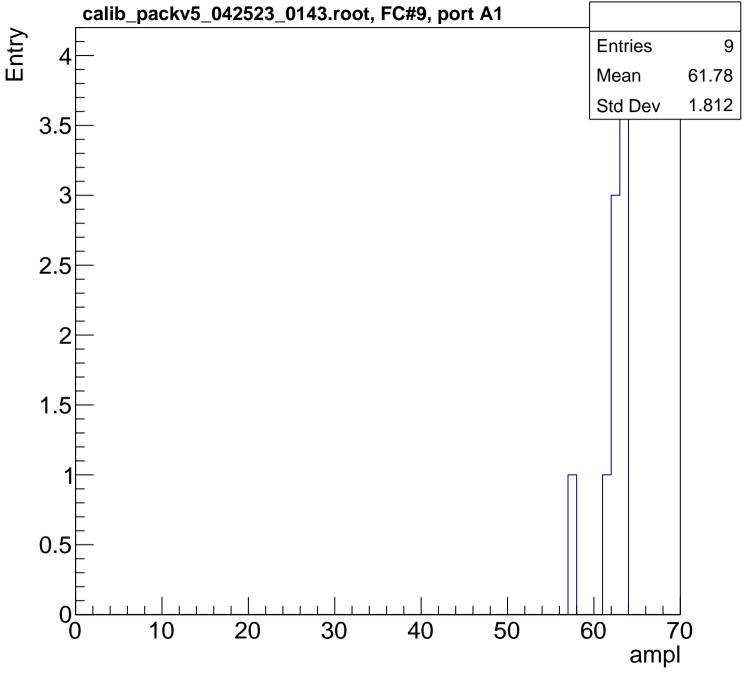




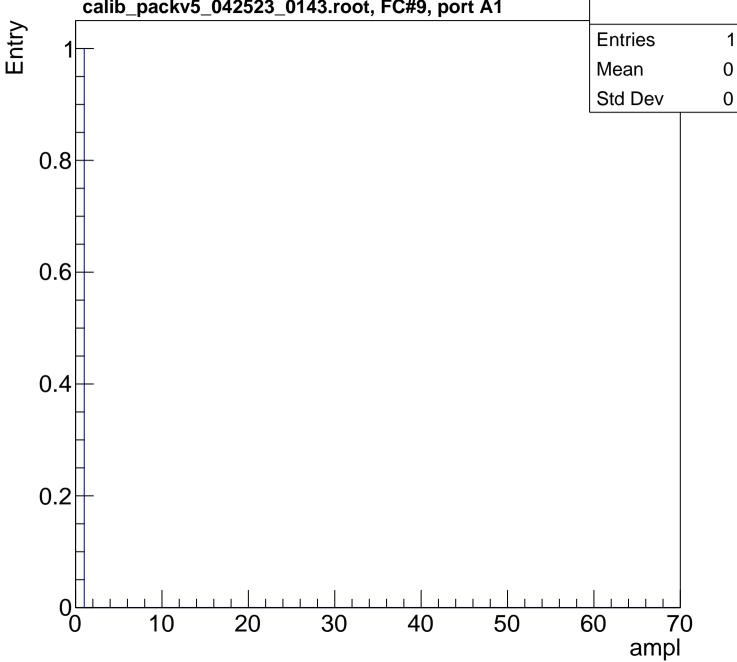


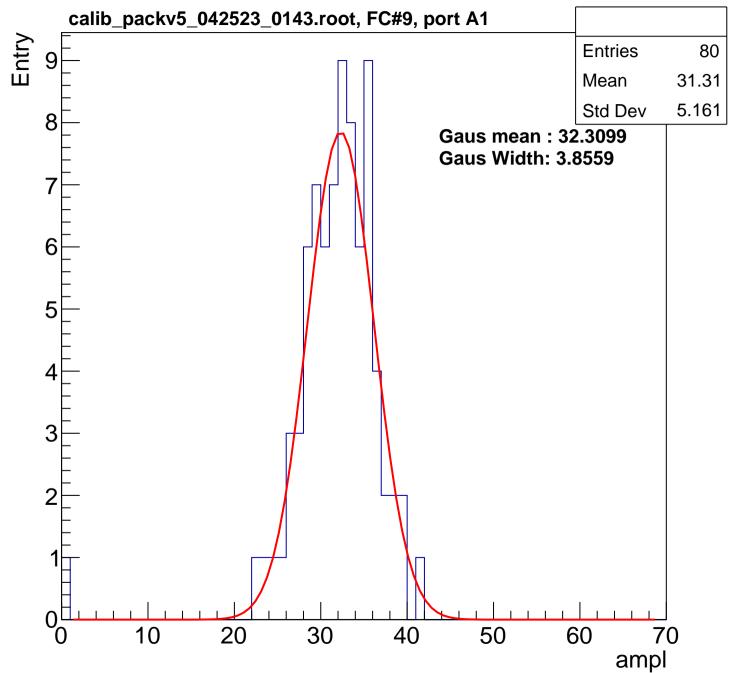


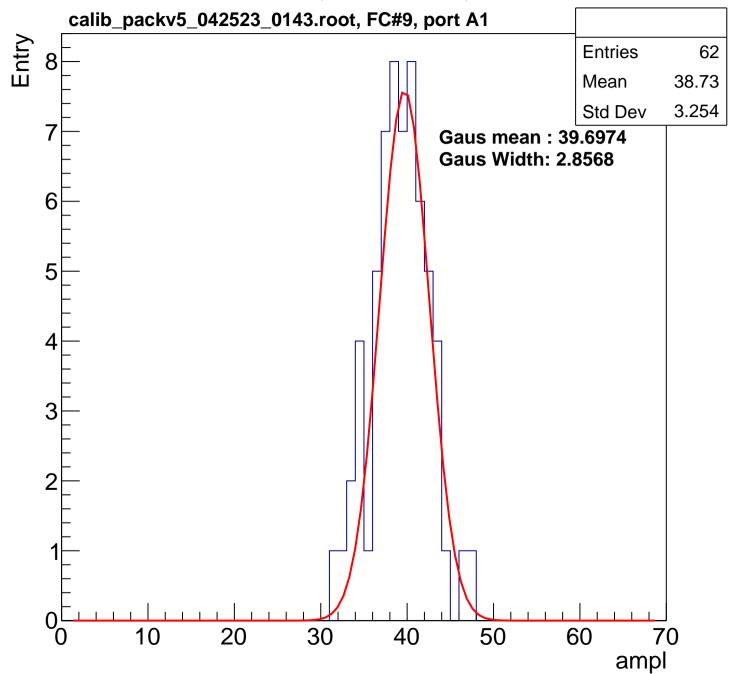


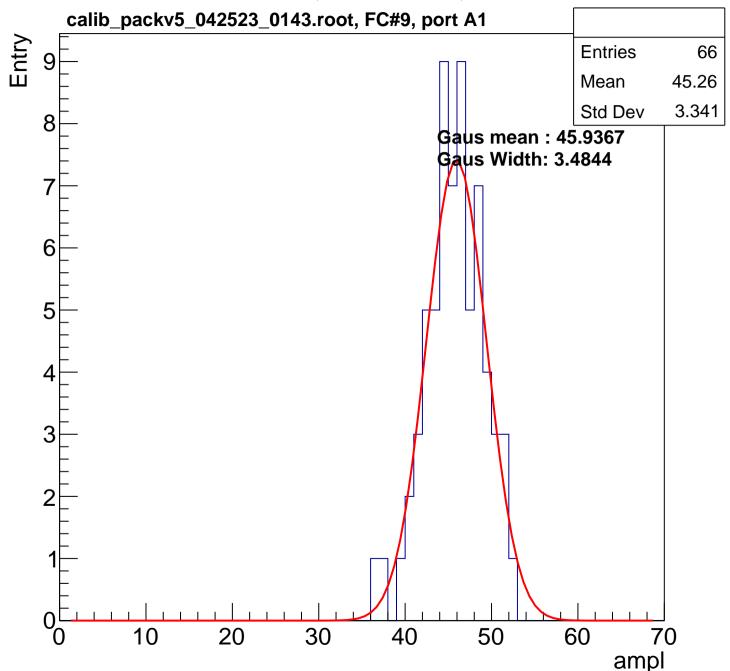


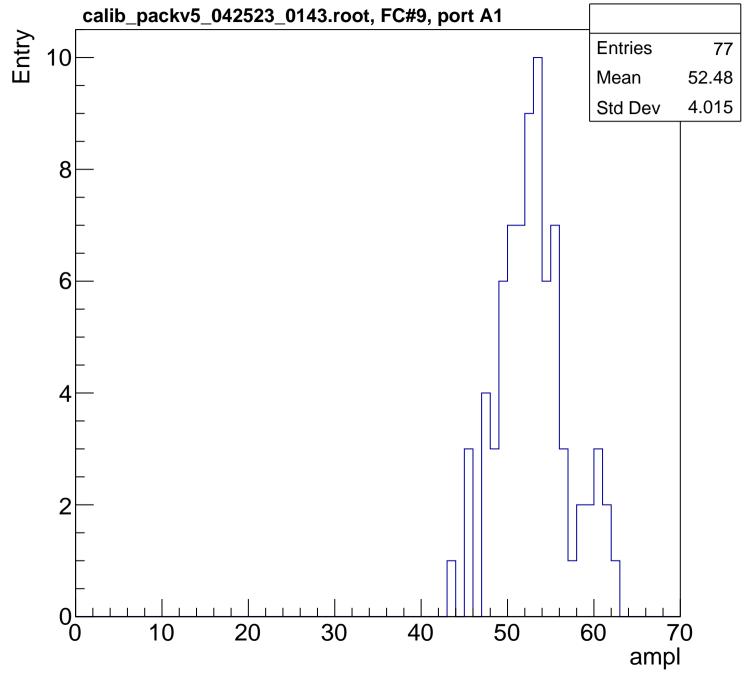
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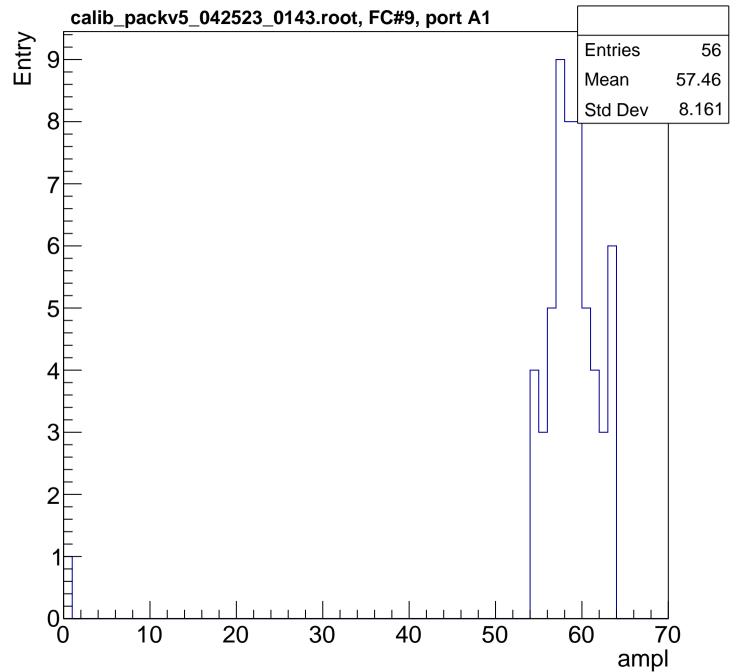


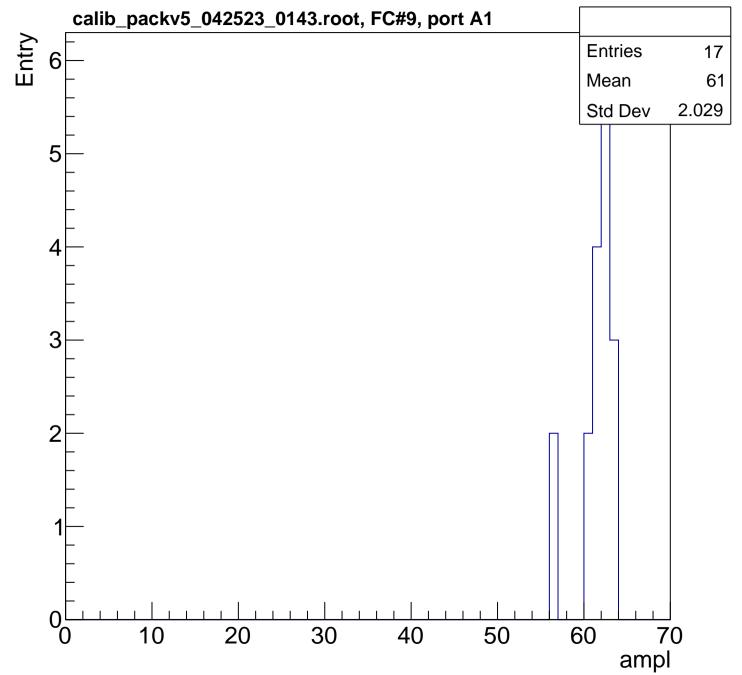




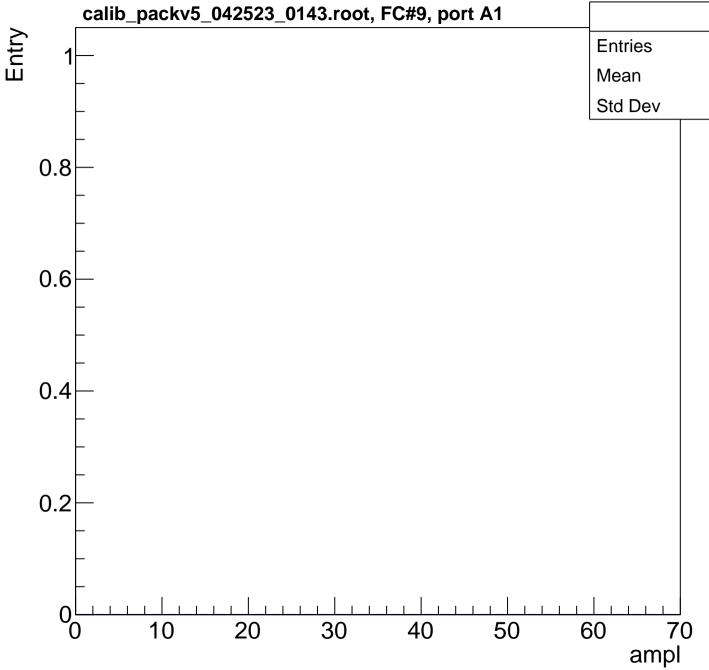


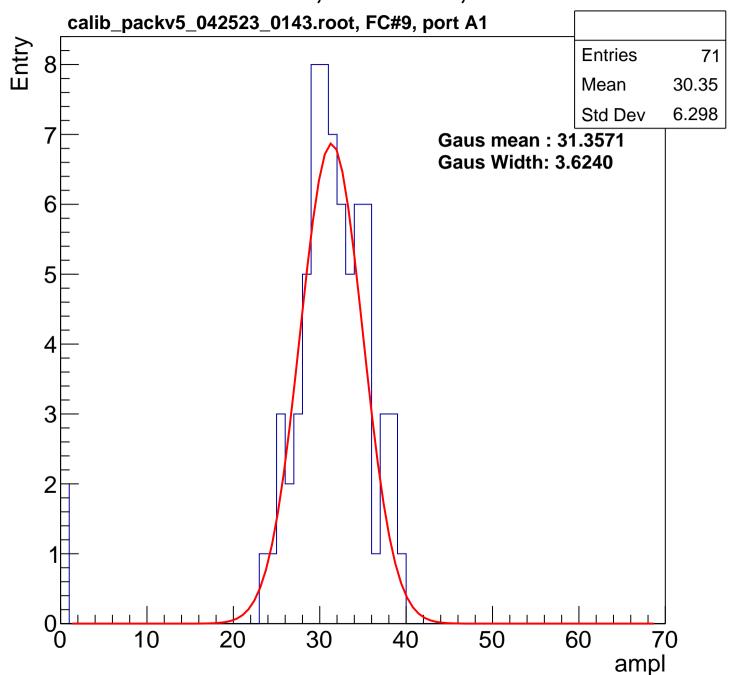


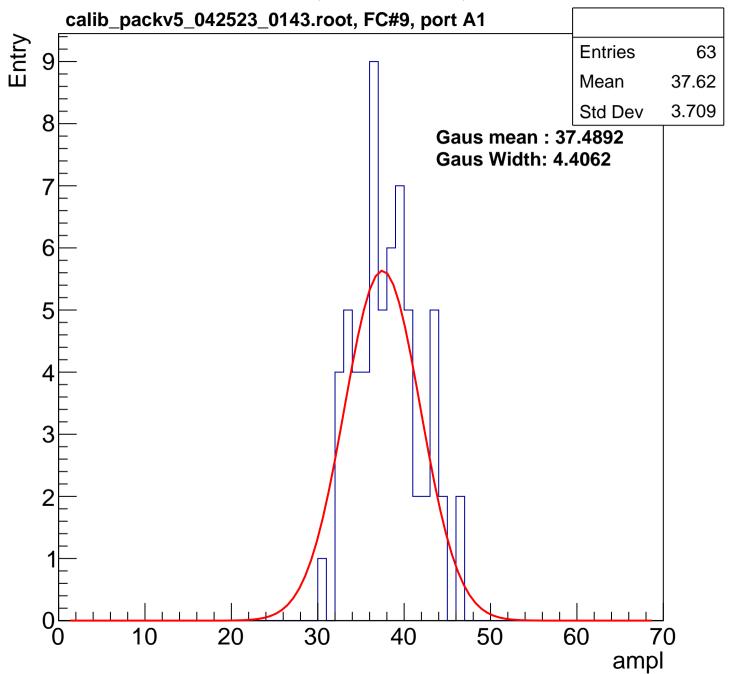


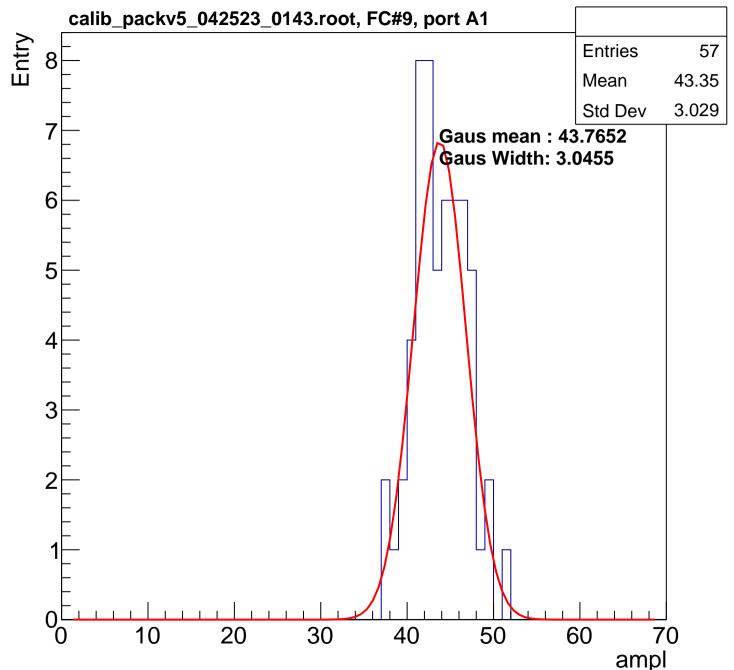


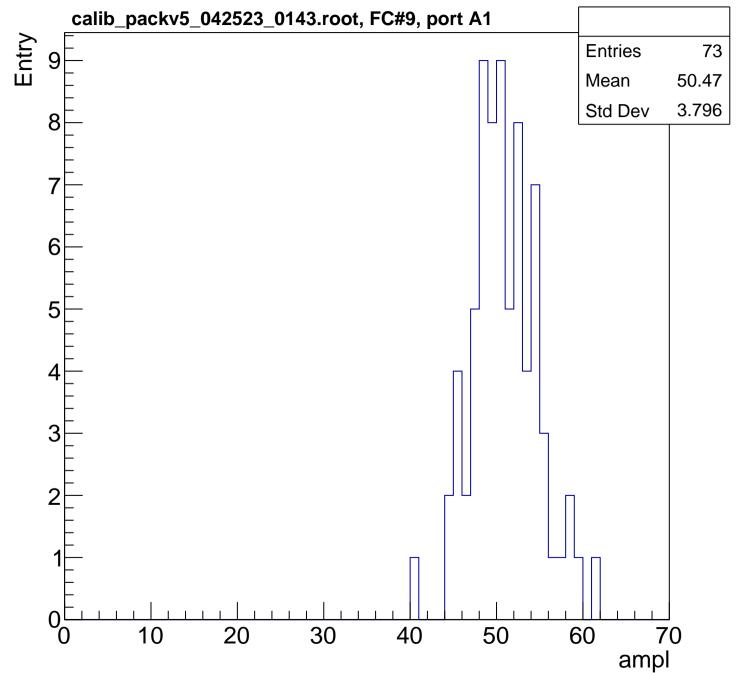


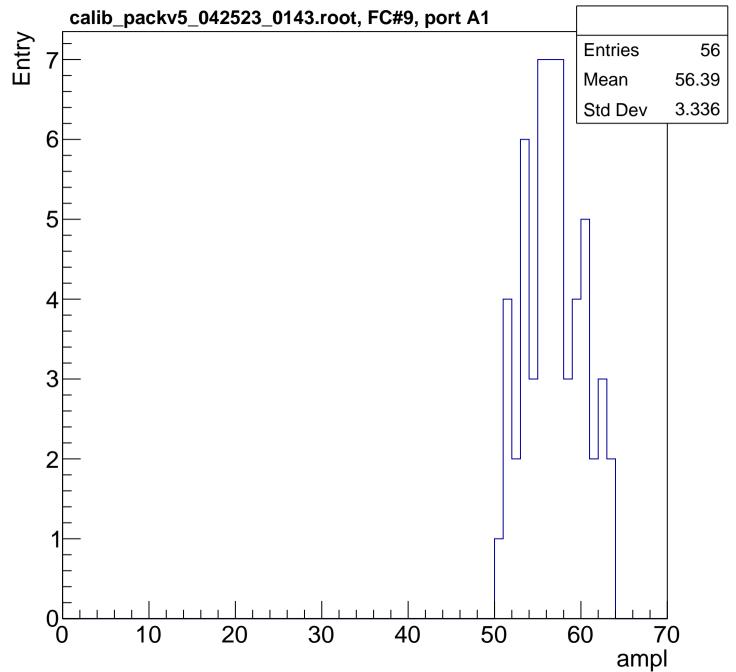


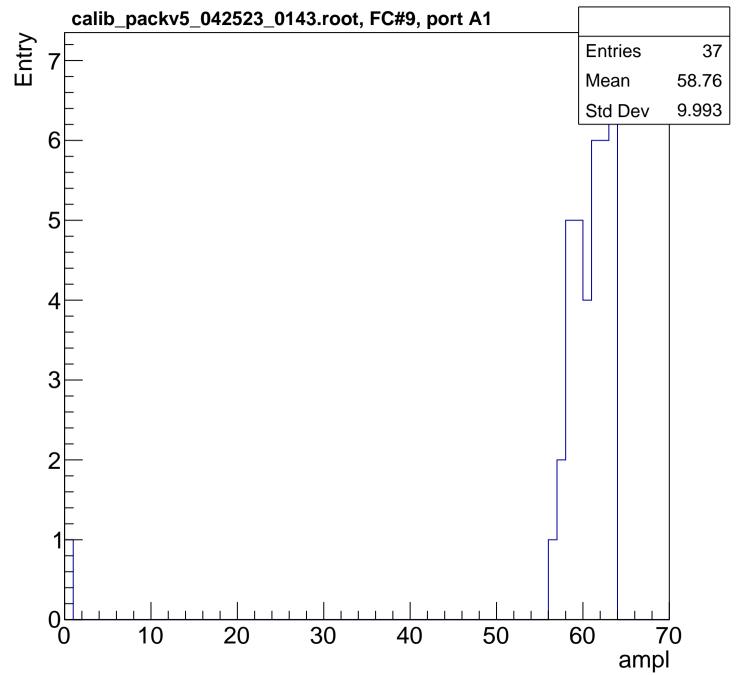


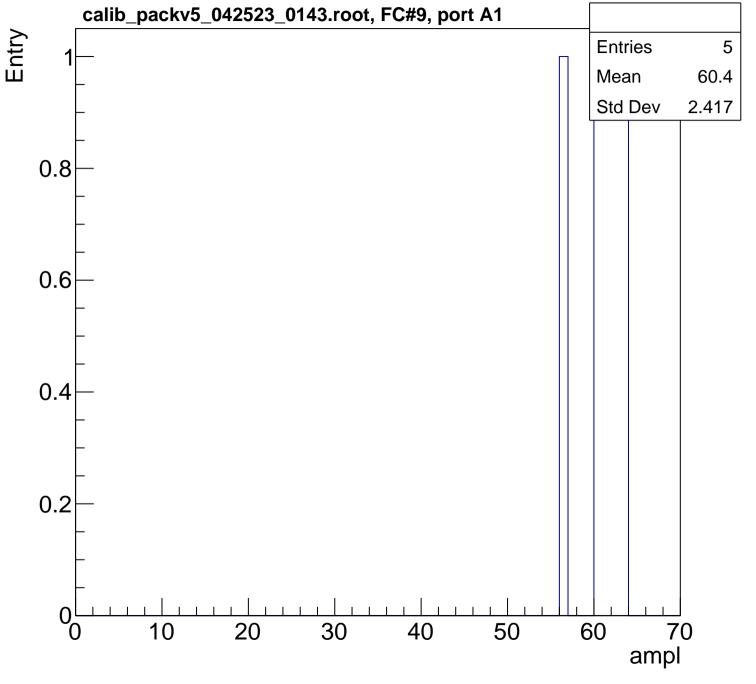




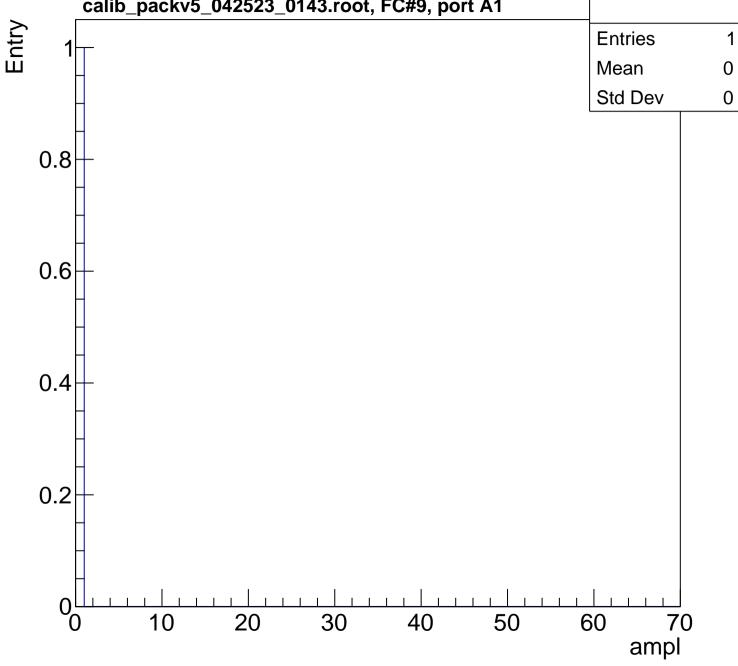


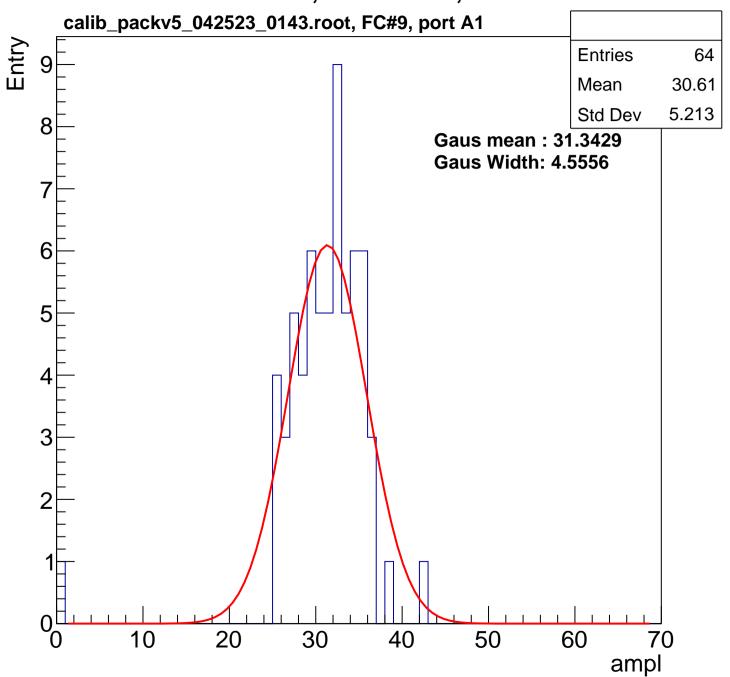


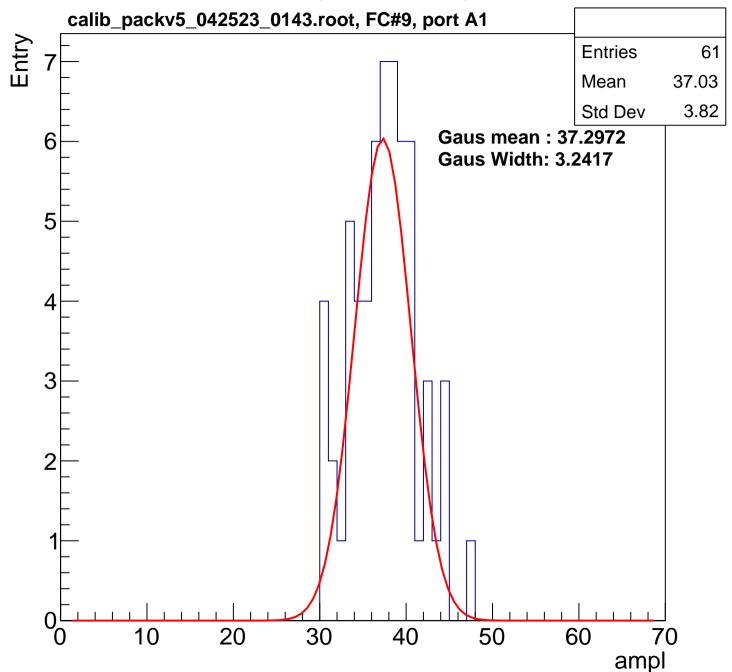


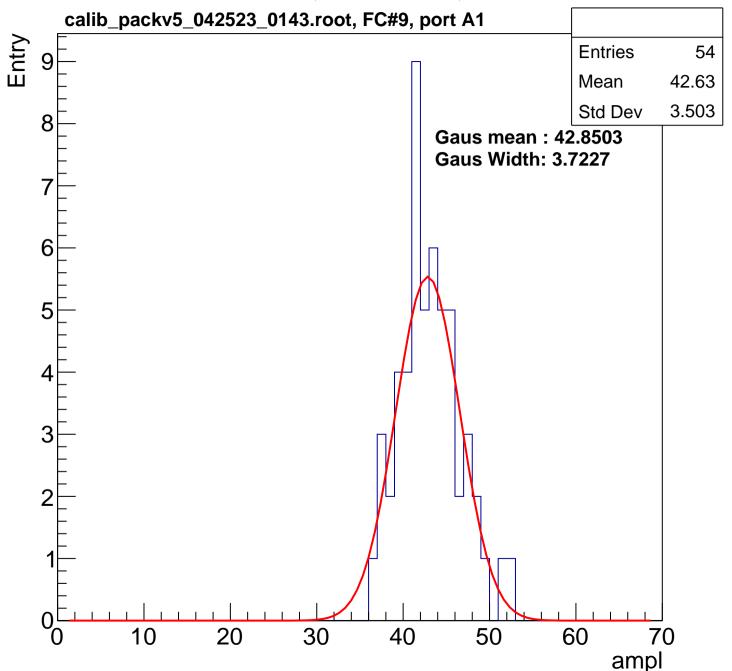


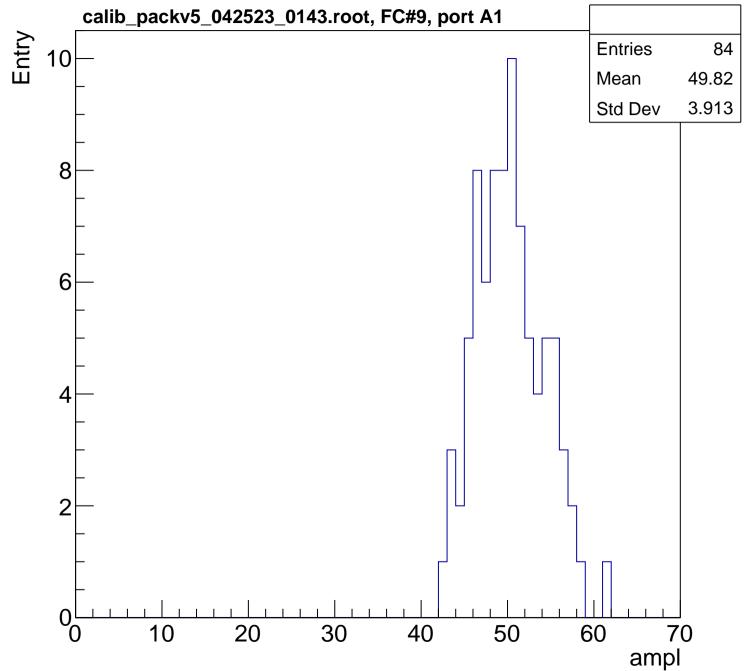
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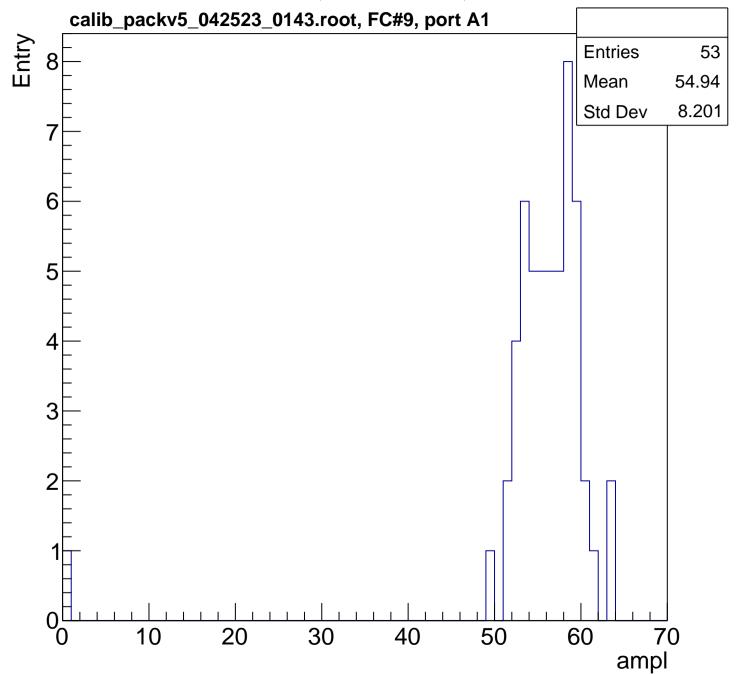


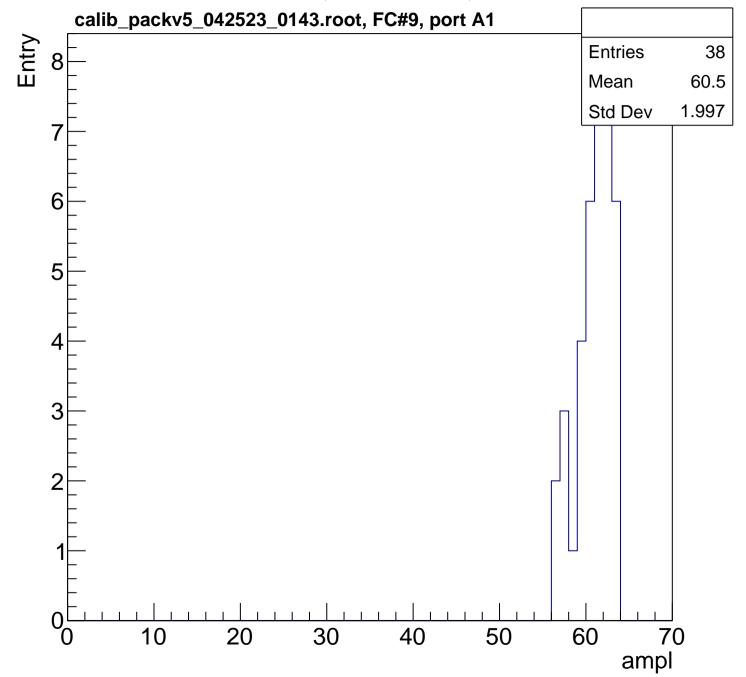


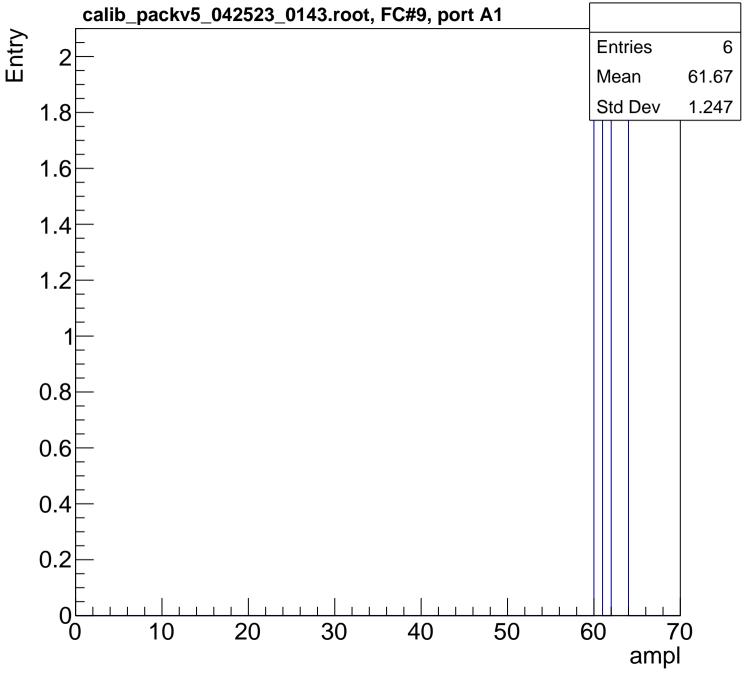


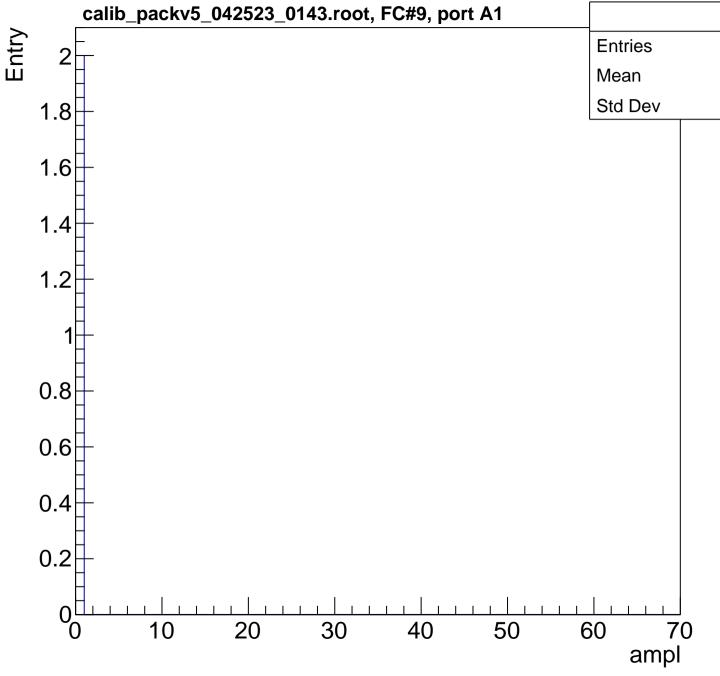


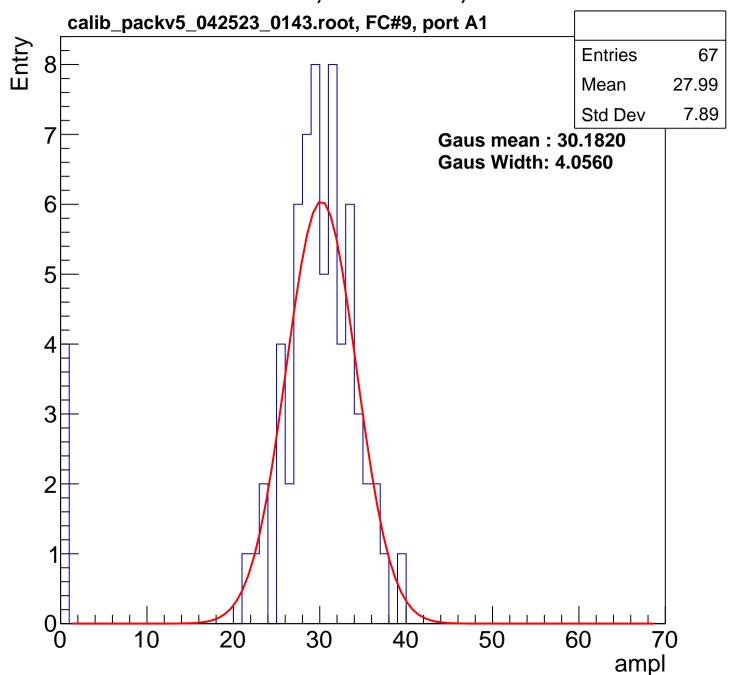


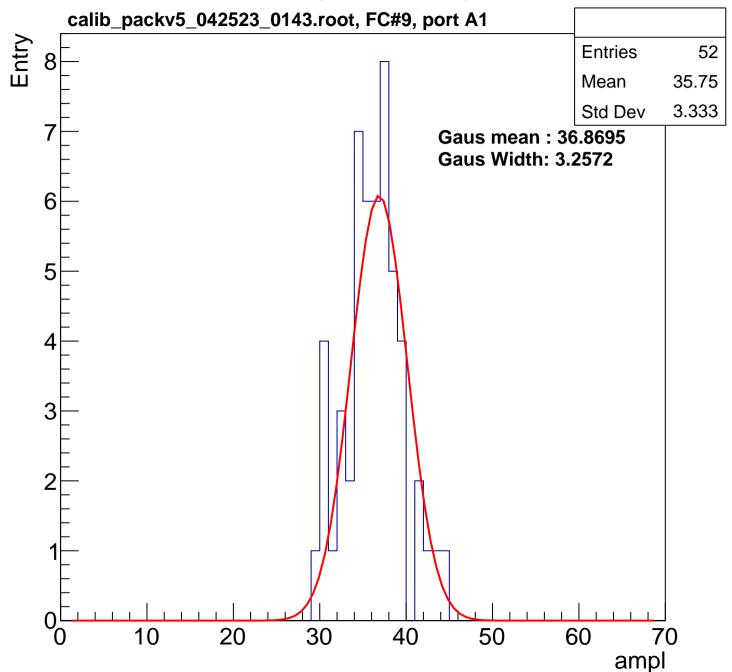


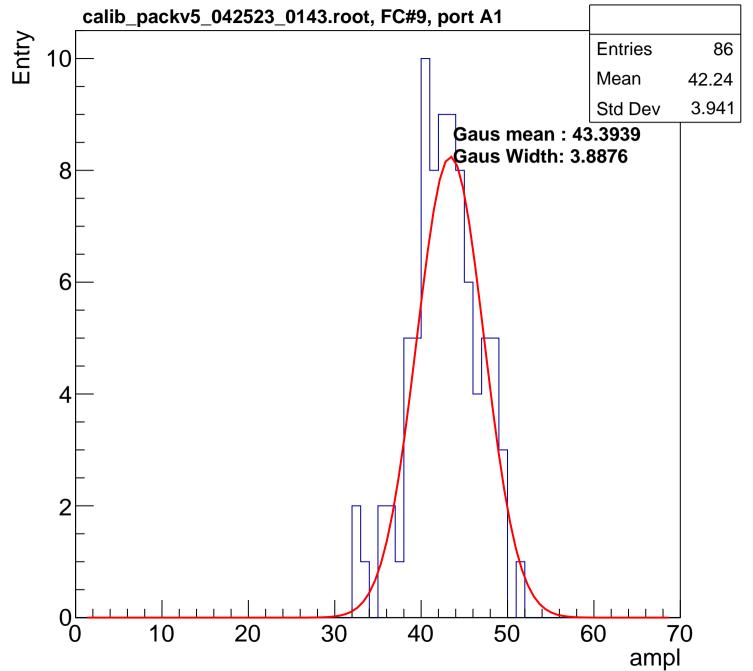


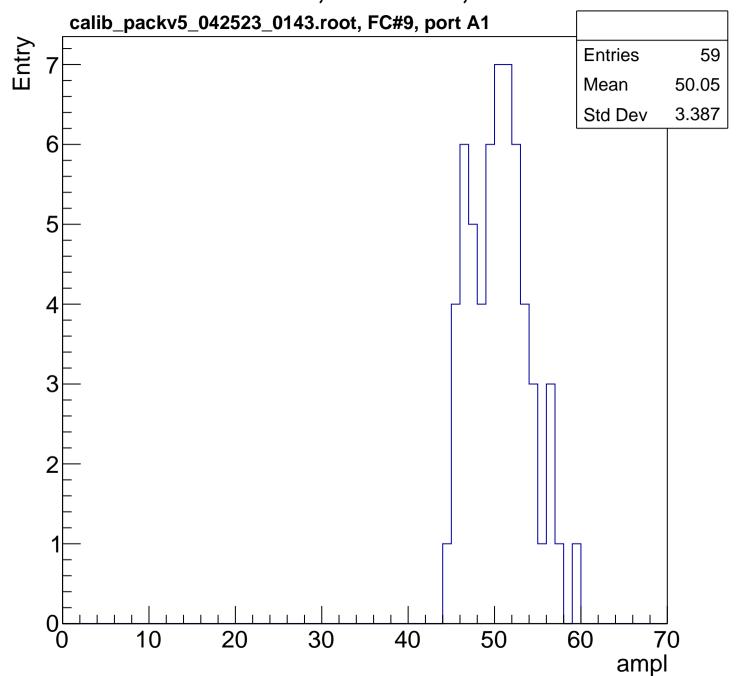


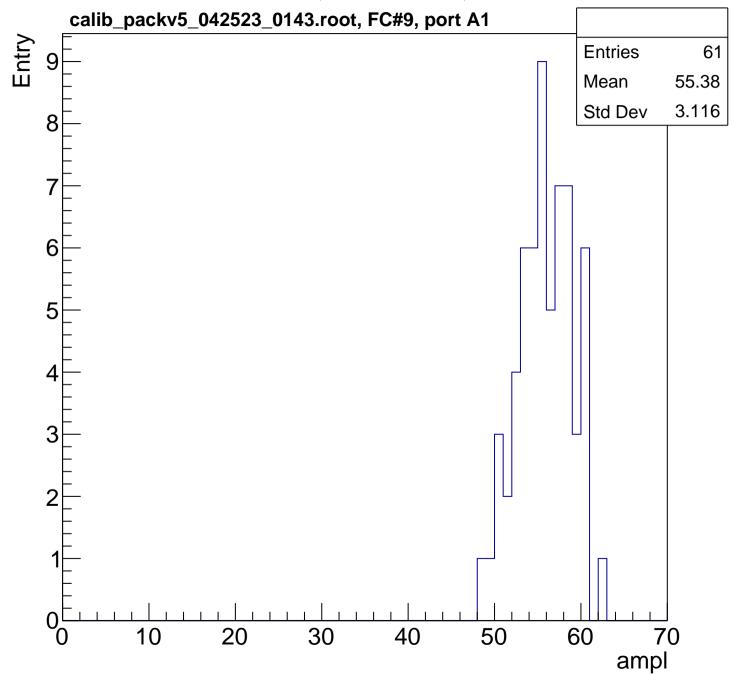


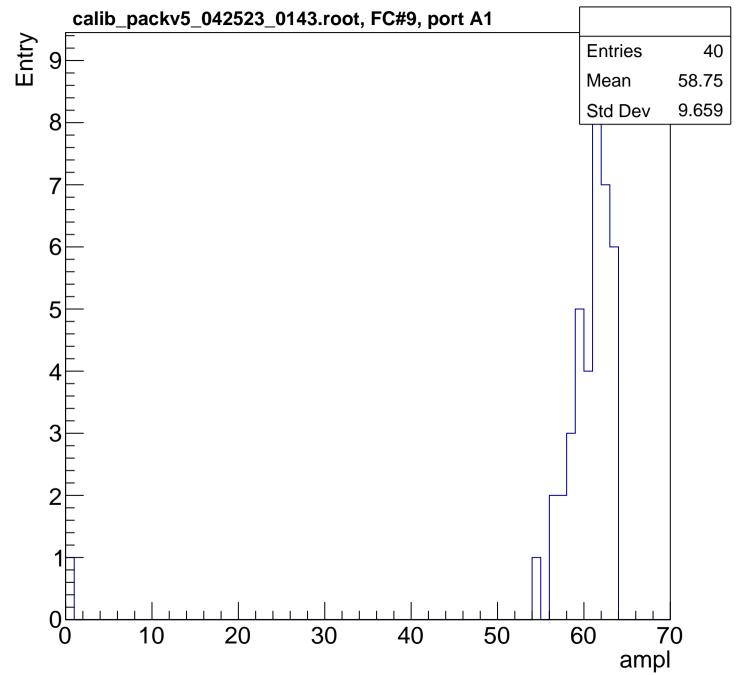


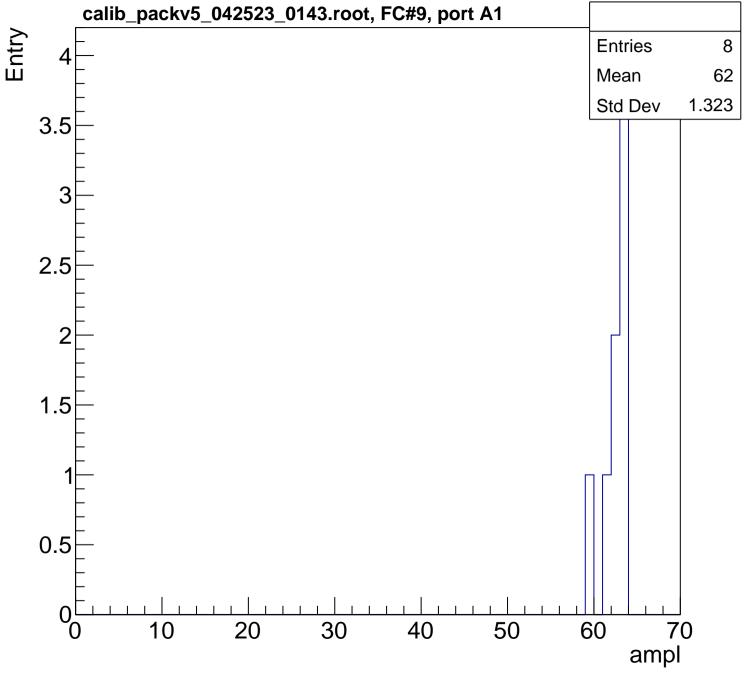


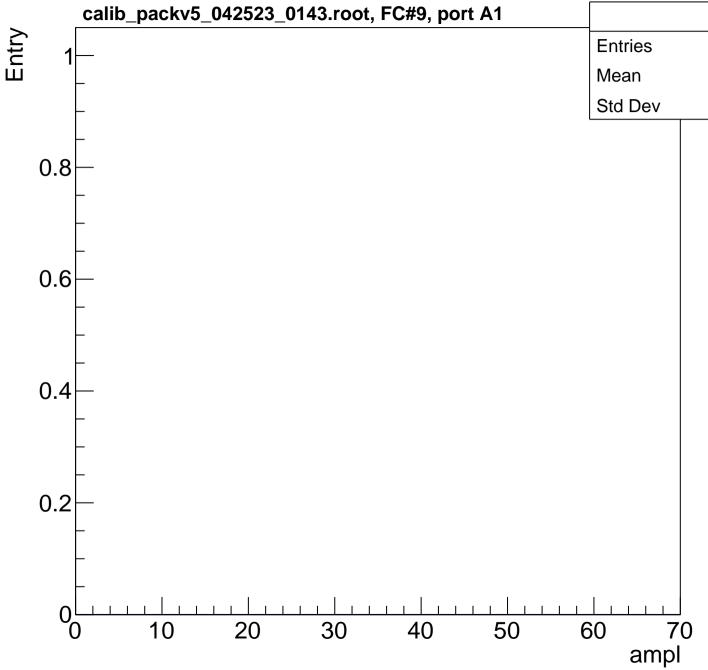


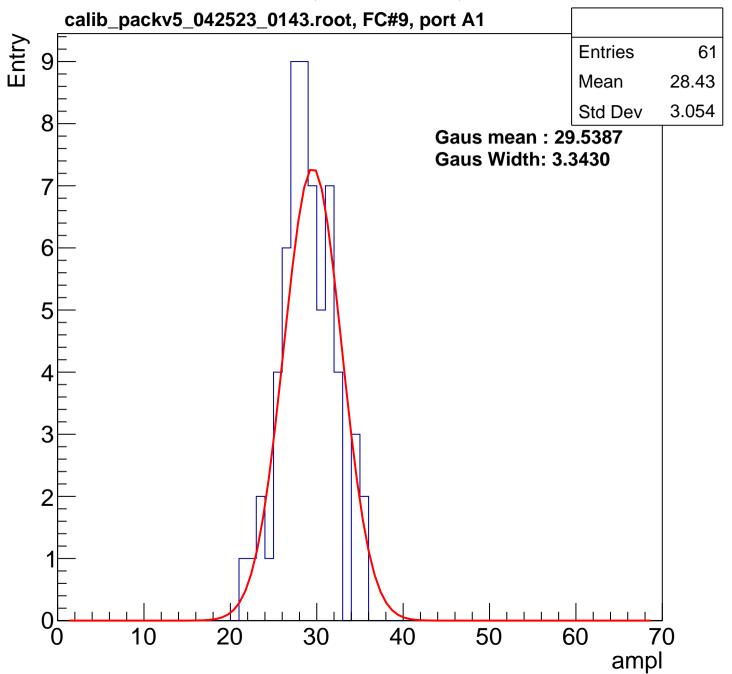


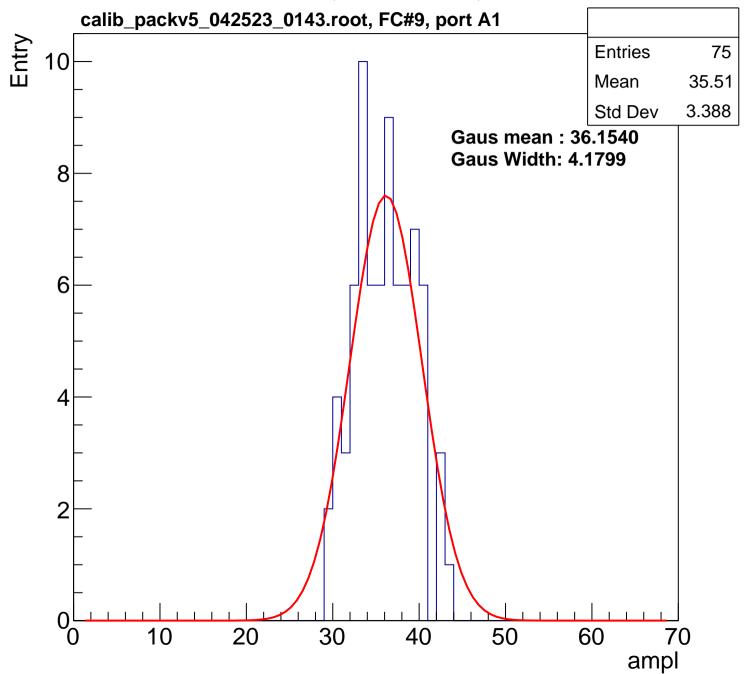


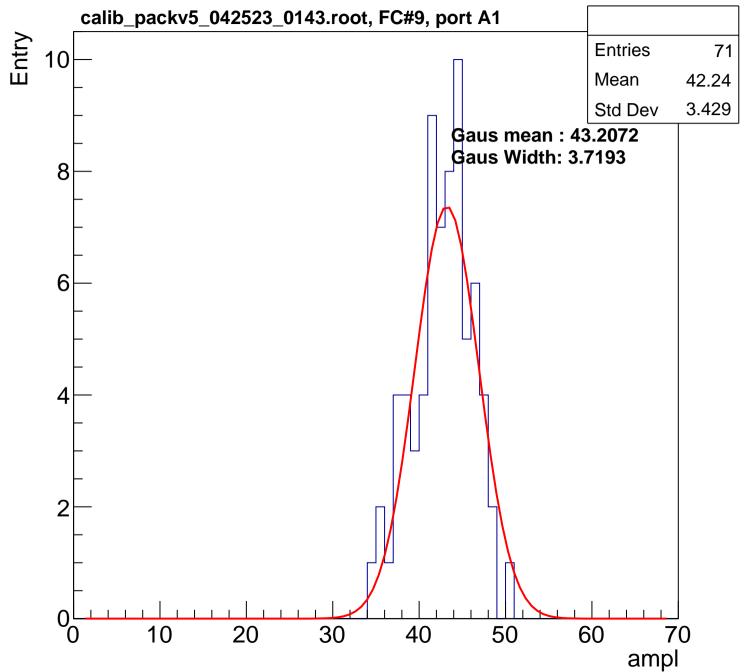


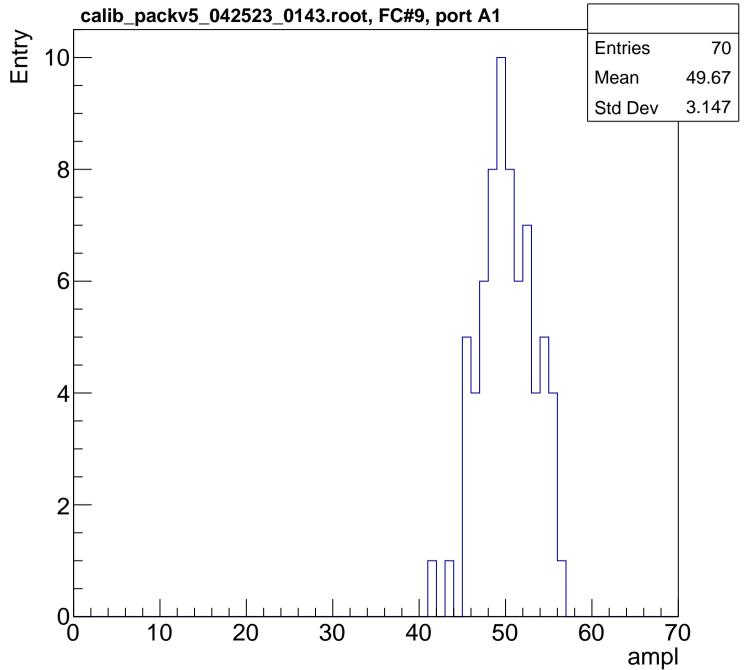


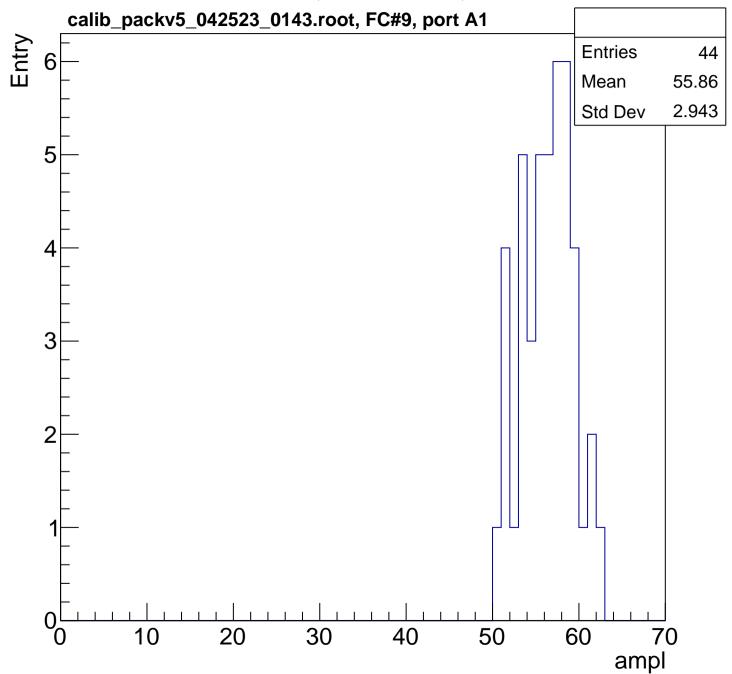


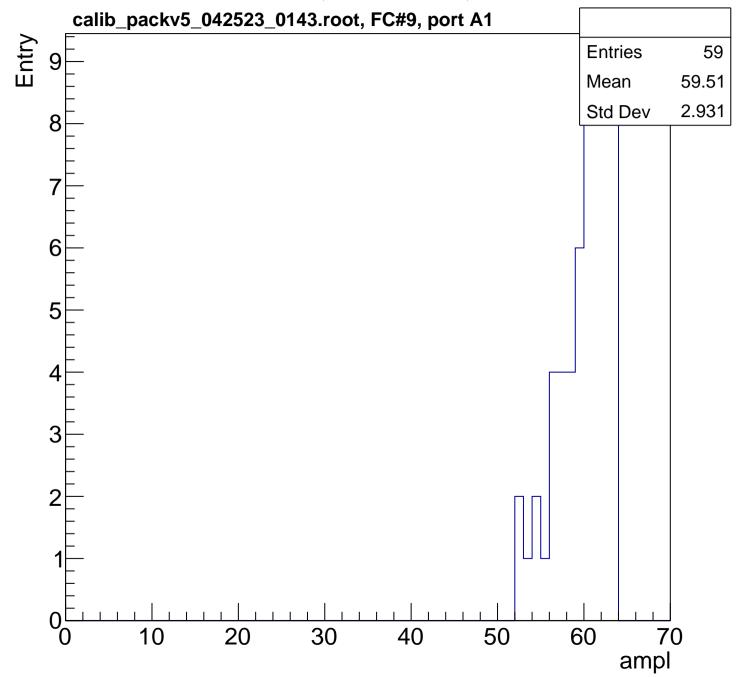


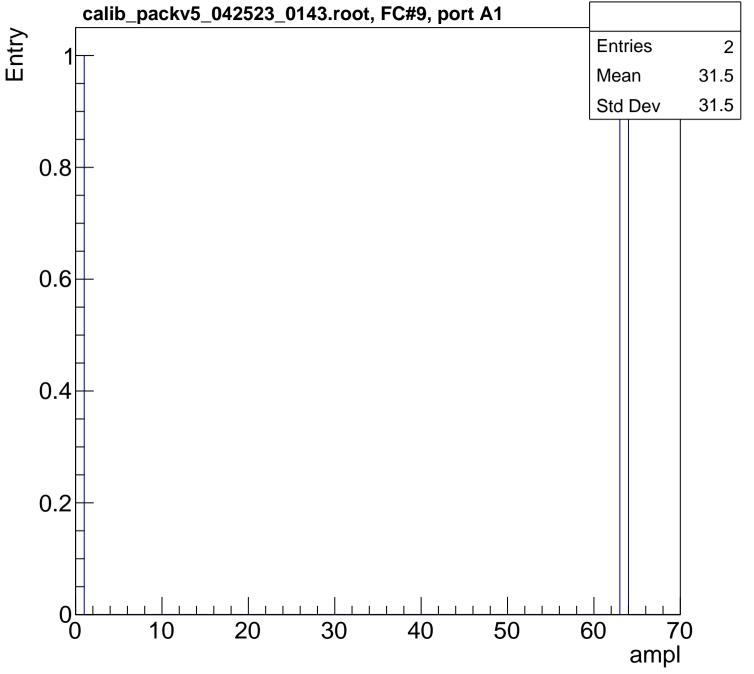




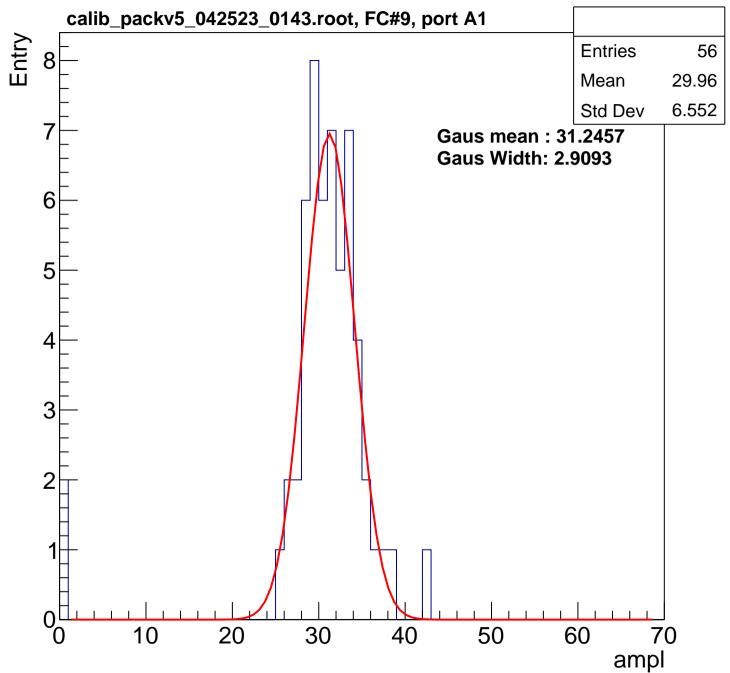


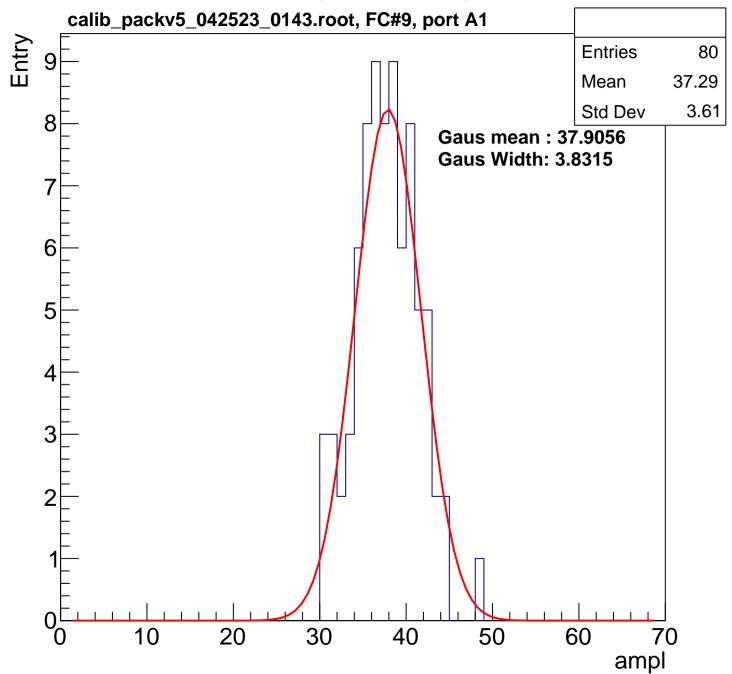


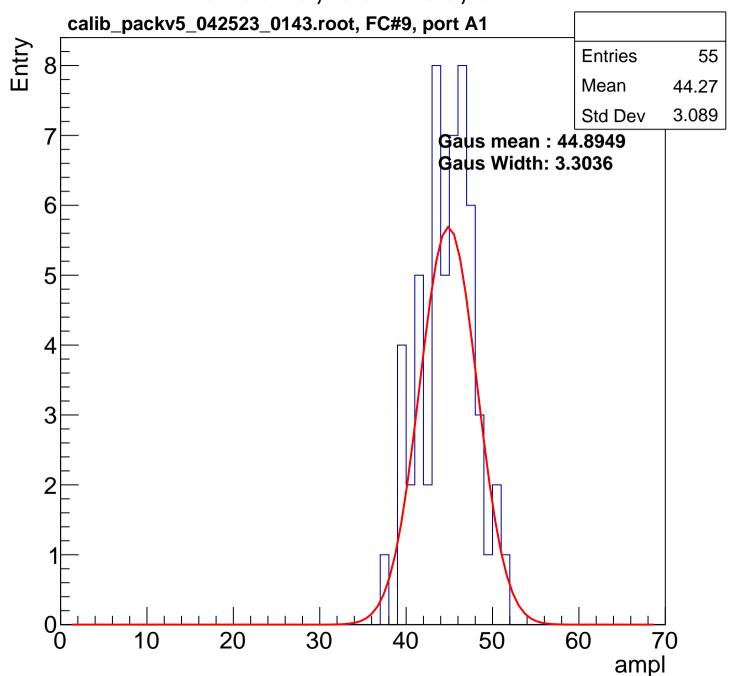


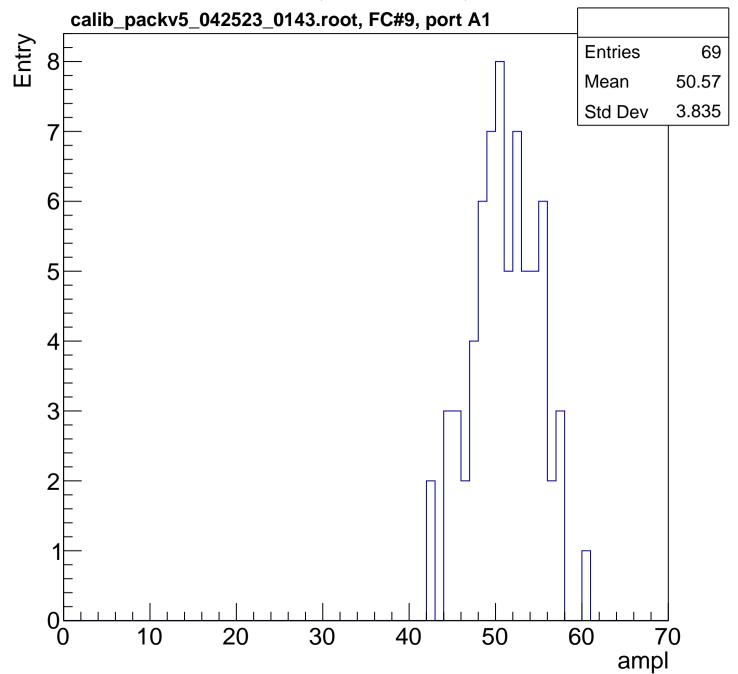


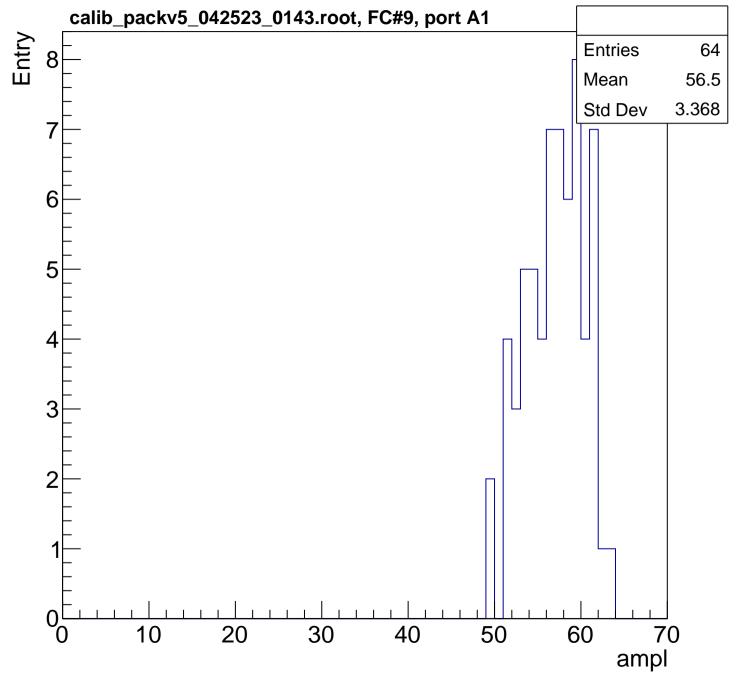


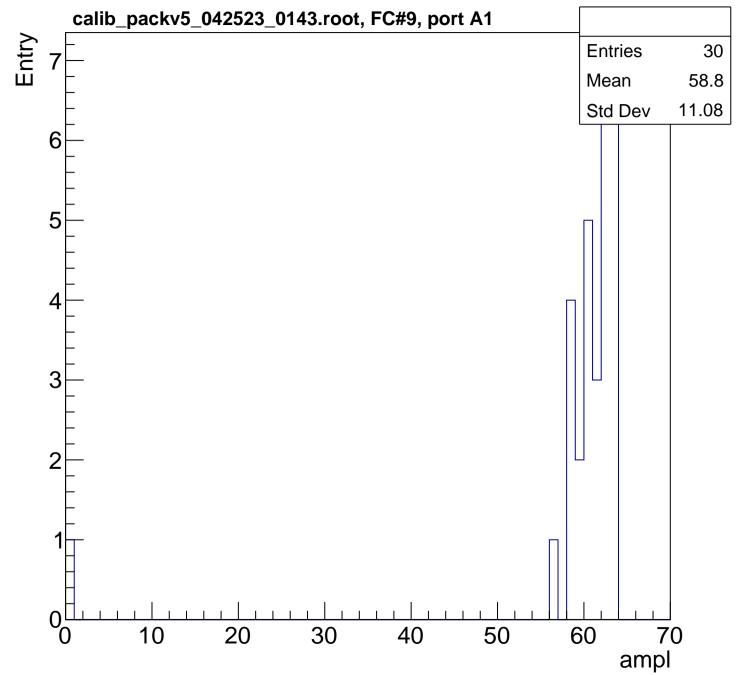


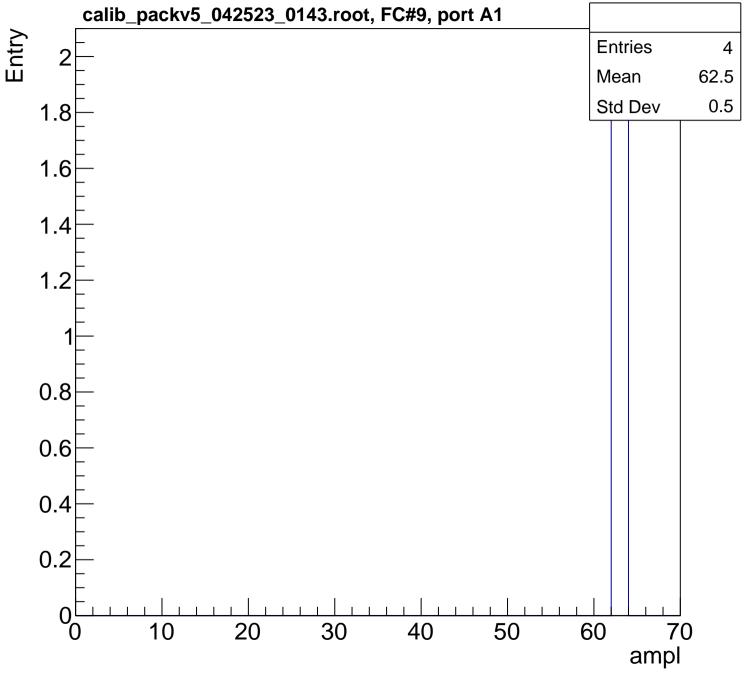


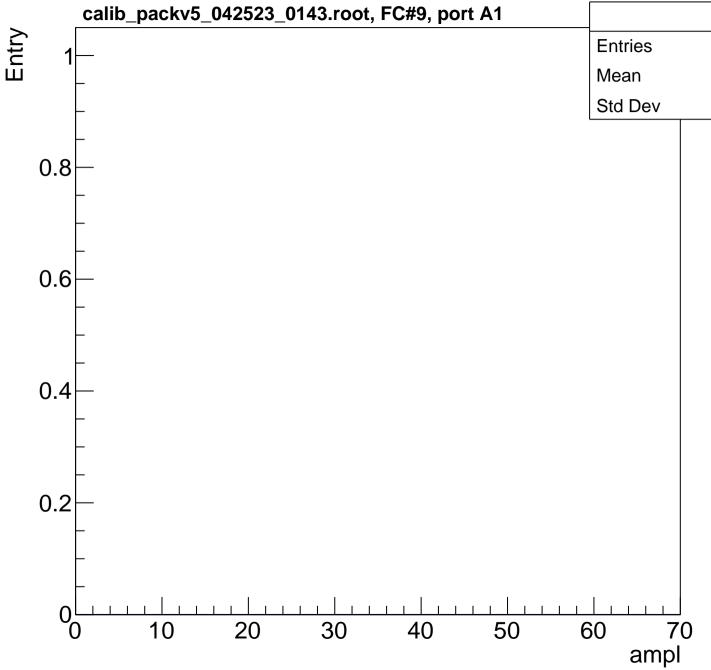


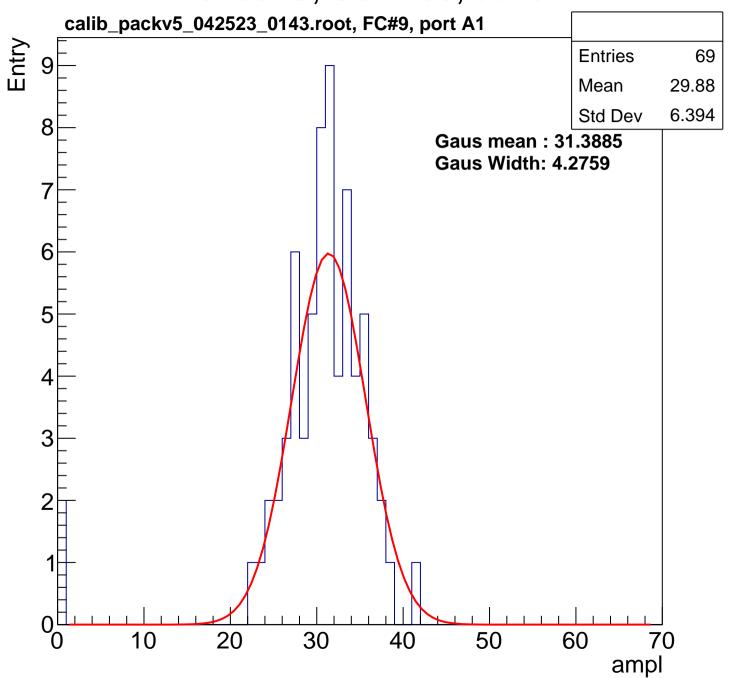


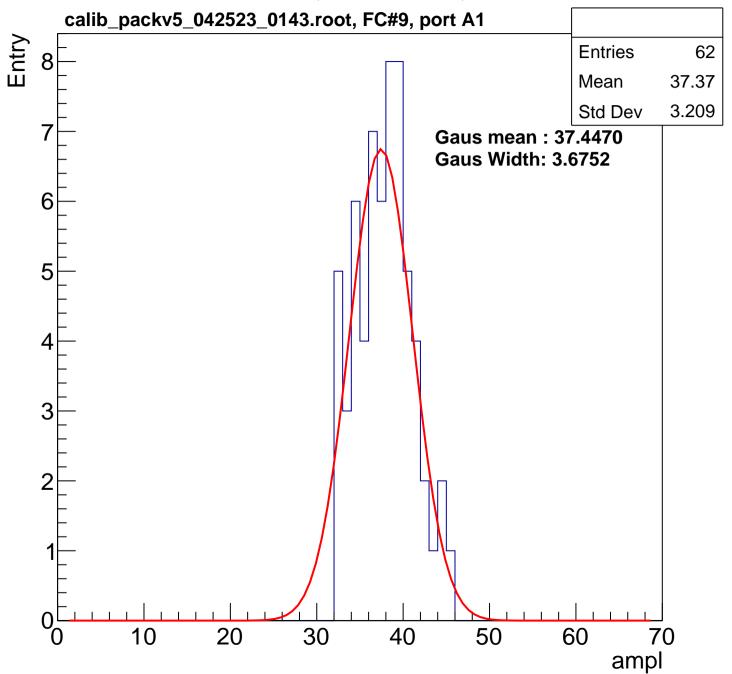


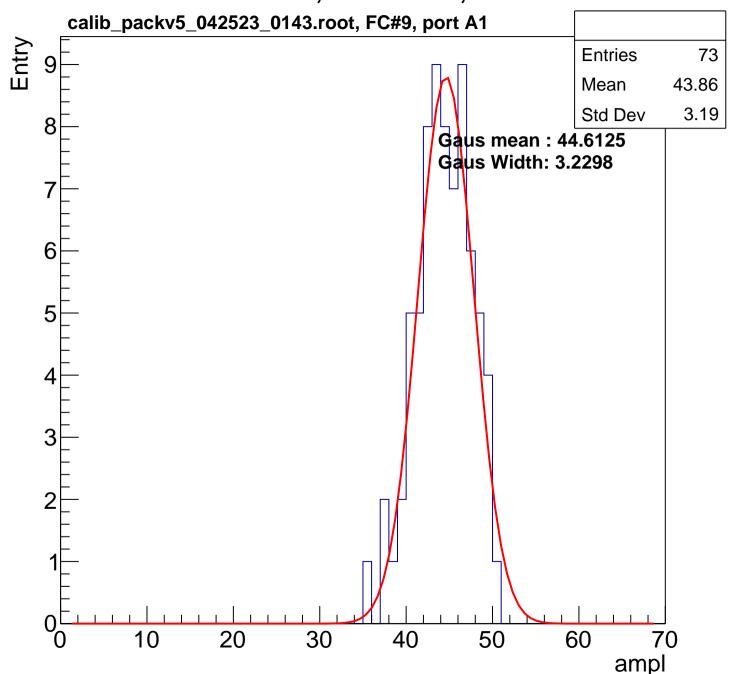


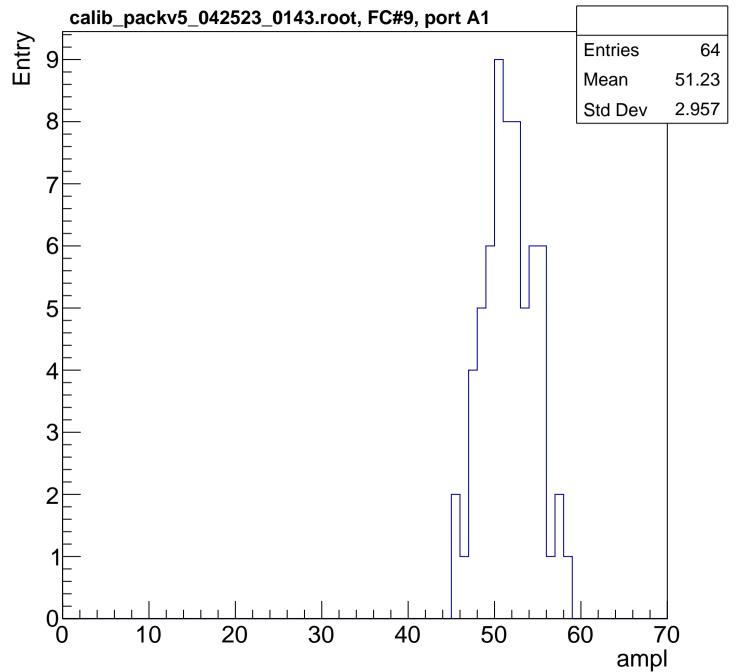


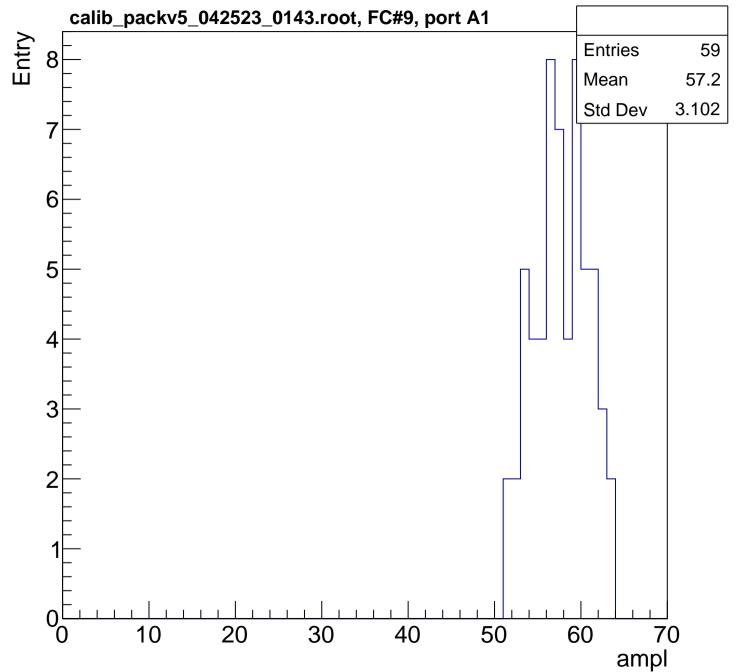


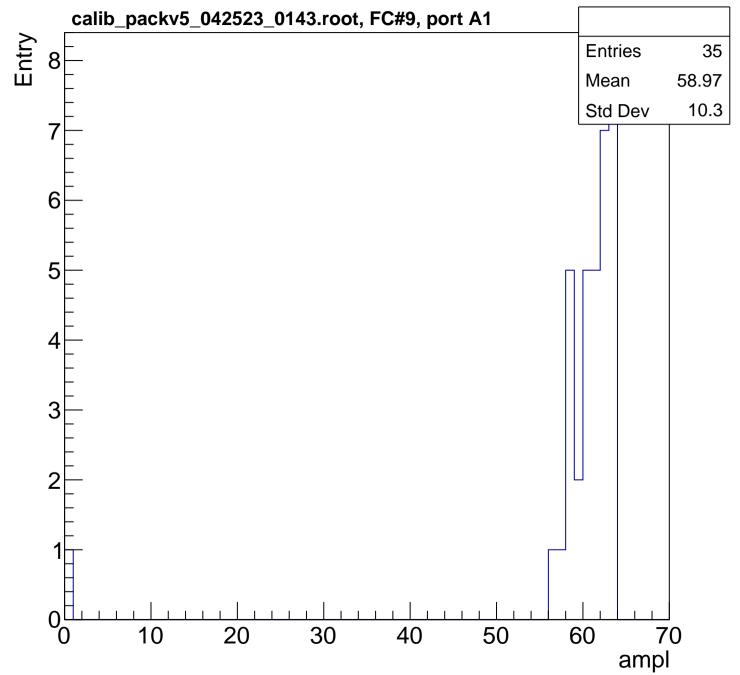


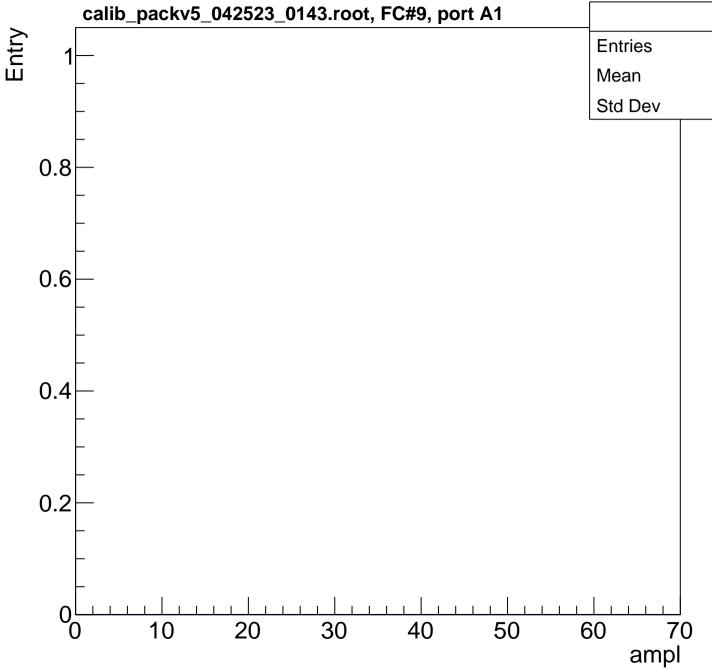




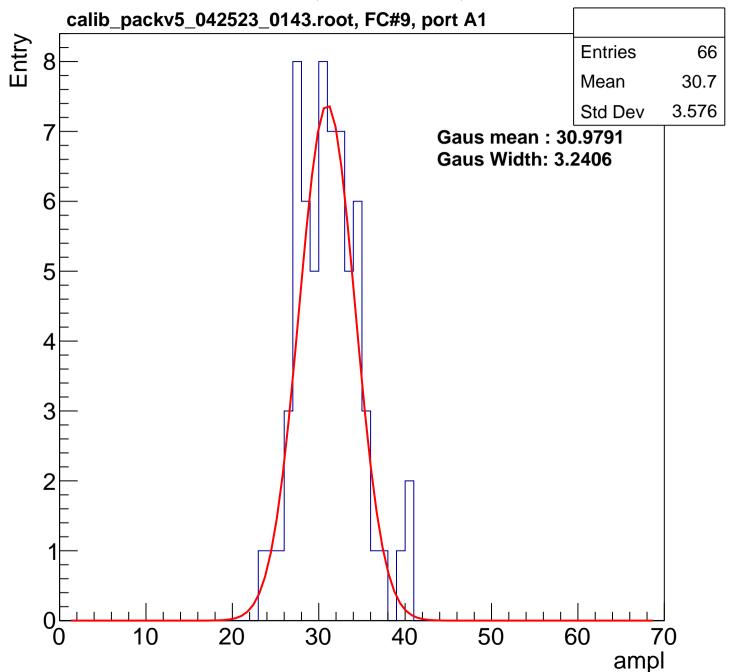


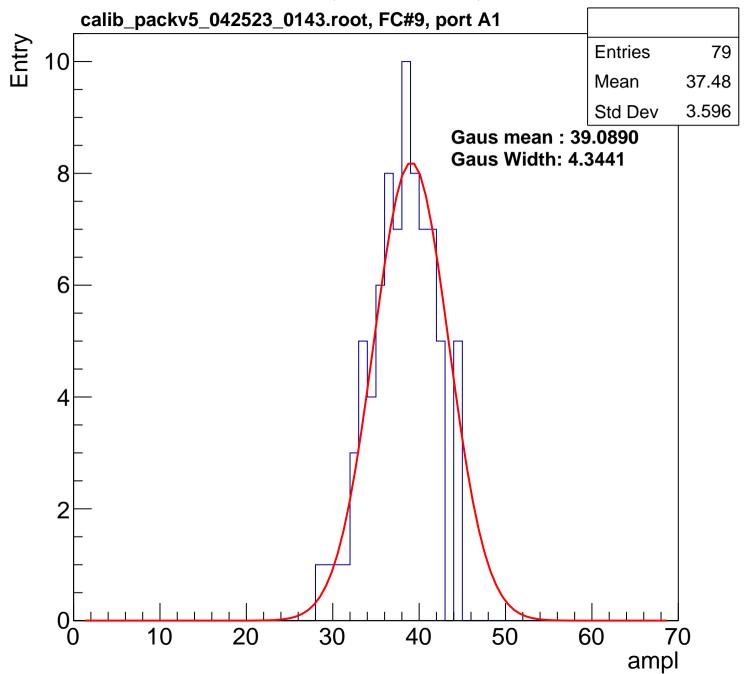


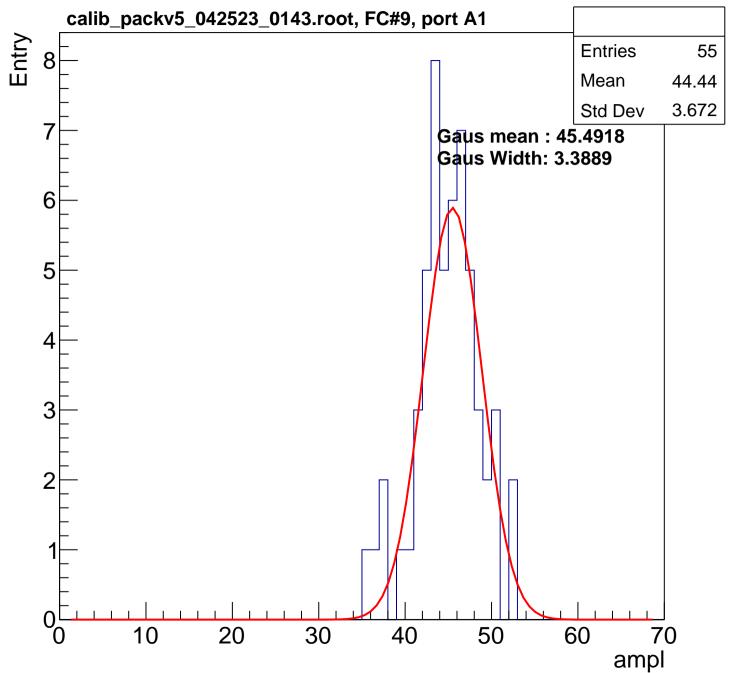


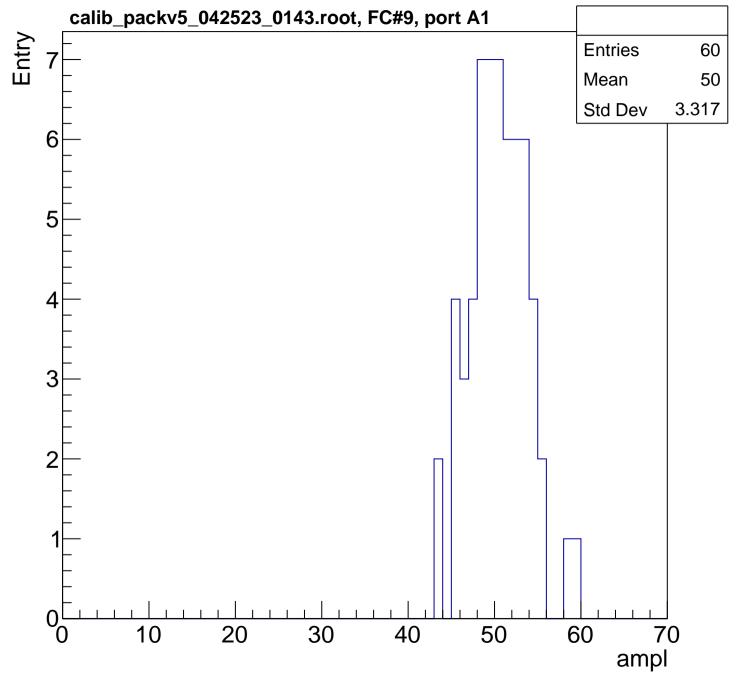


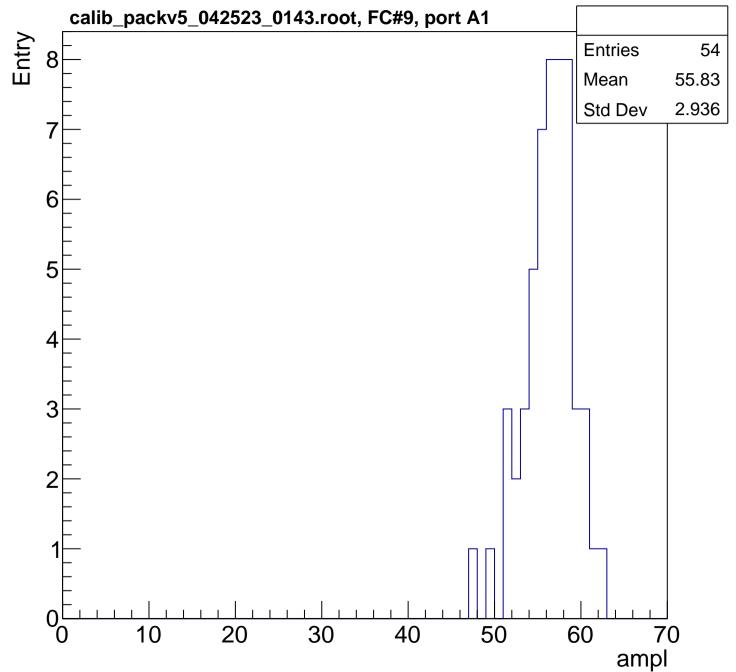


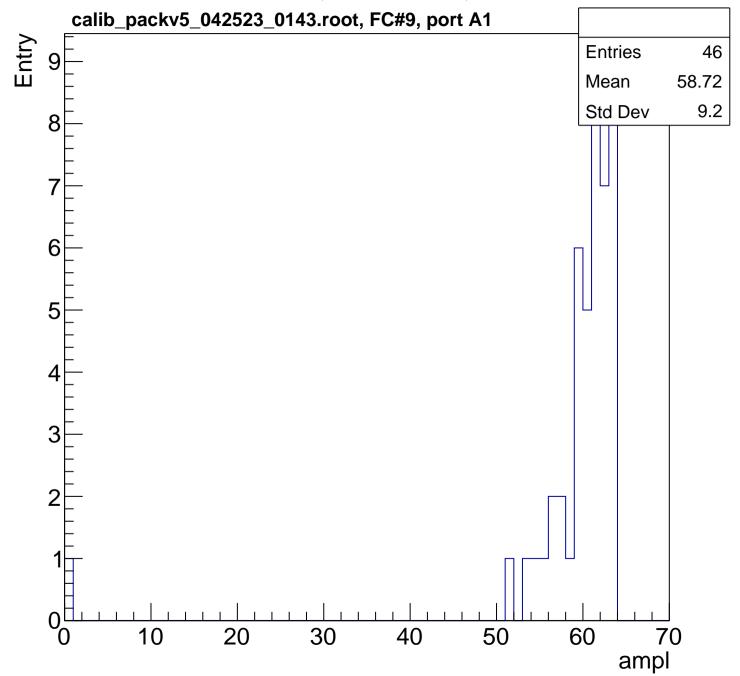


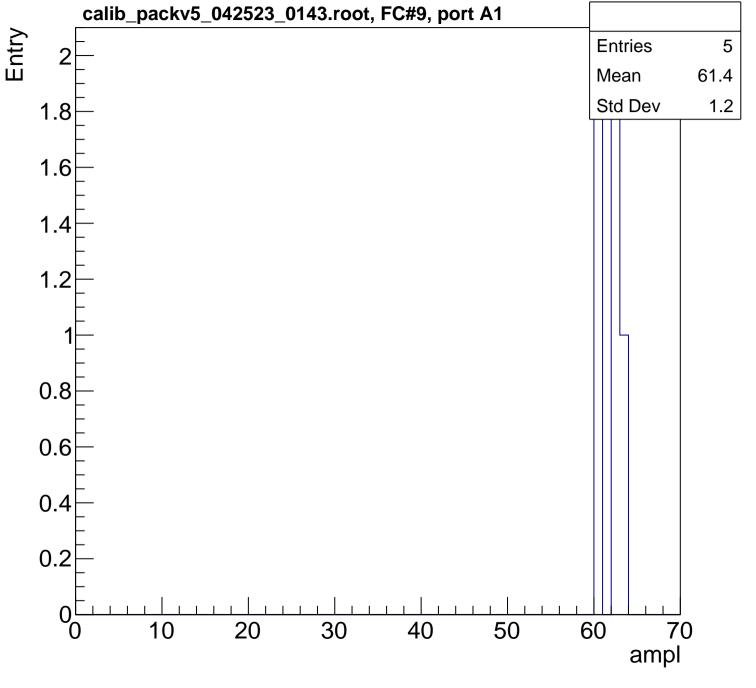




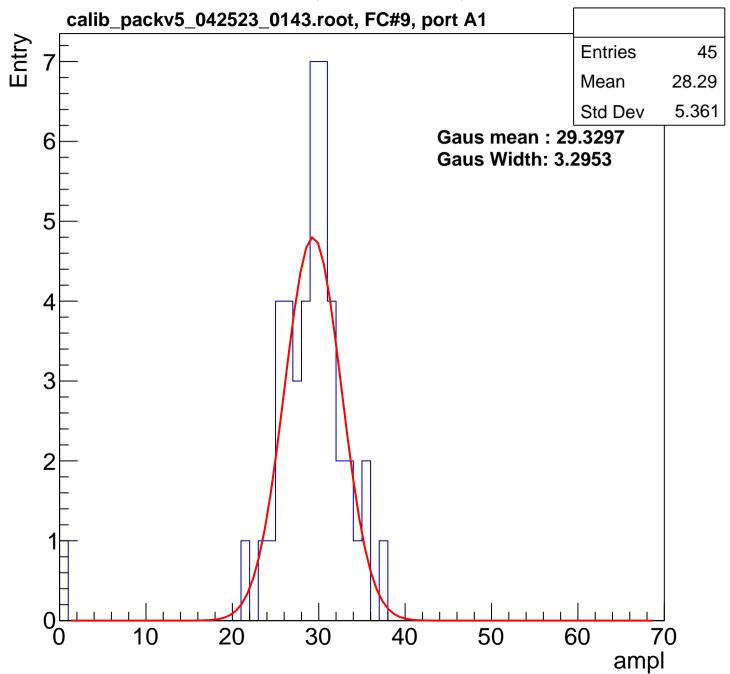


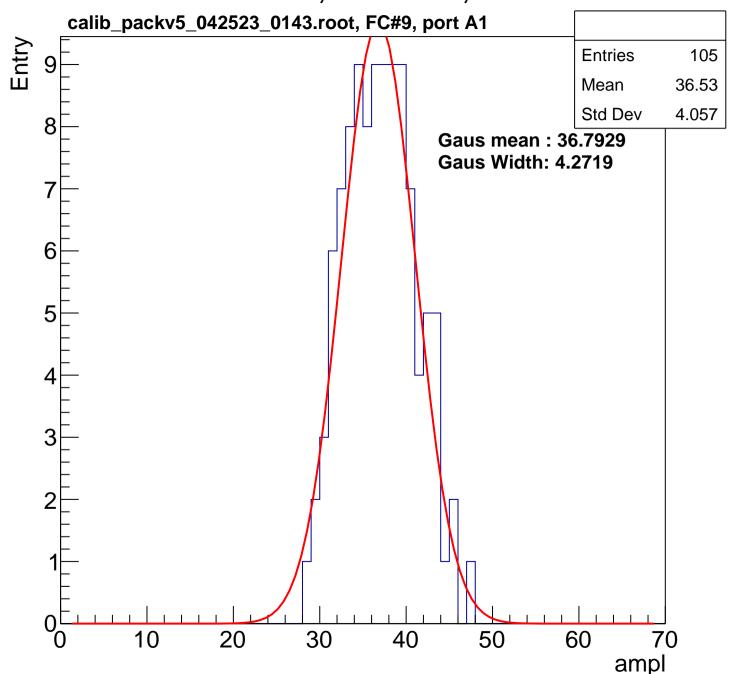


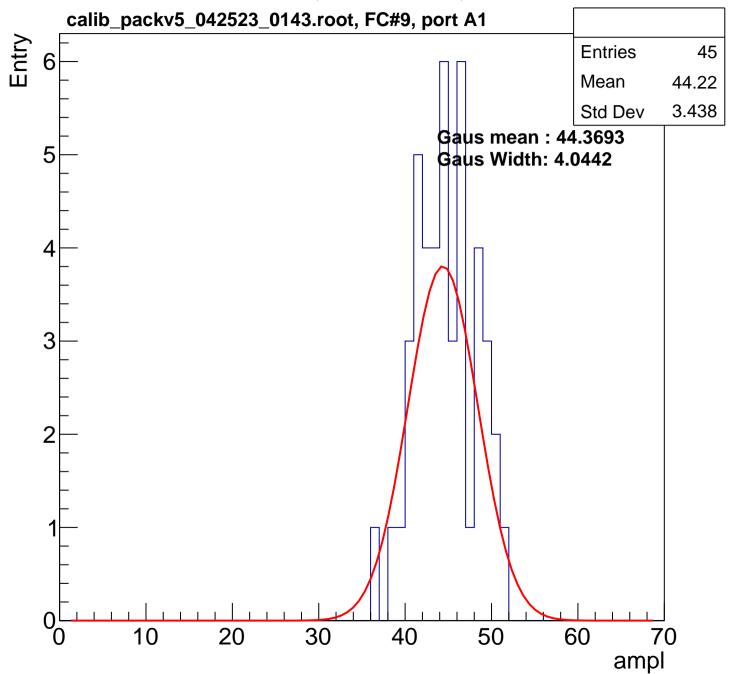


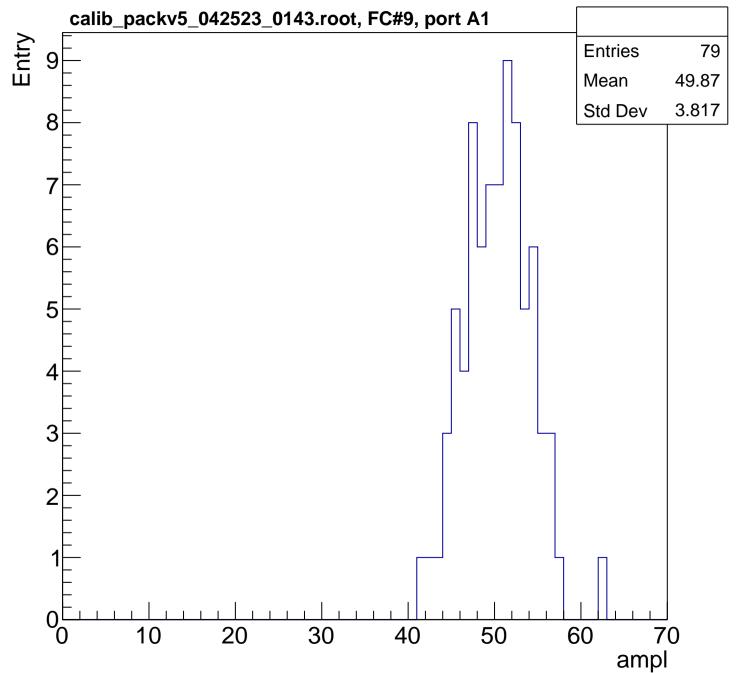


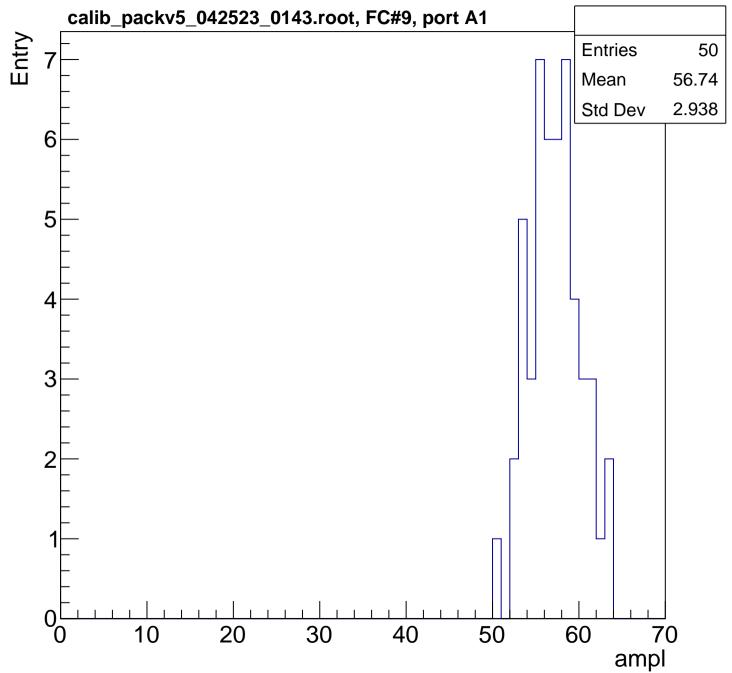
B0L001S, U3-ch70, adc7 calib_packv5_042523_0143.root, FC#9, port A1 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

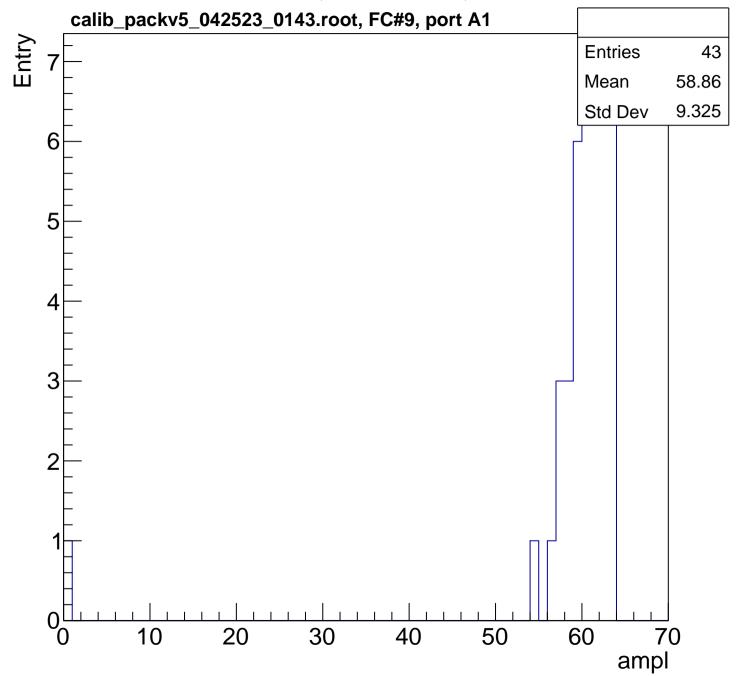


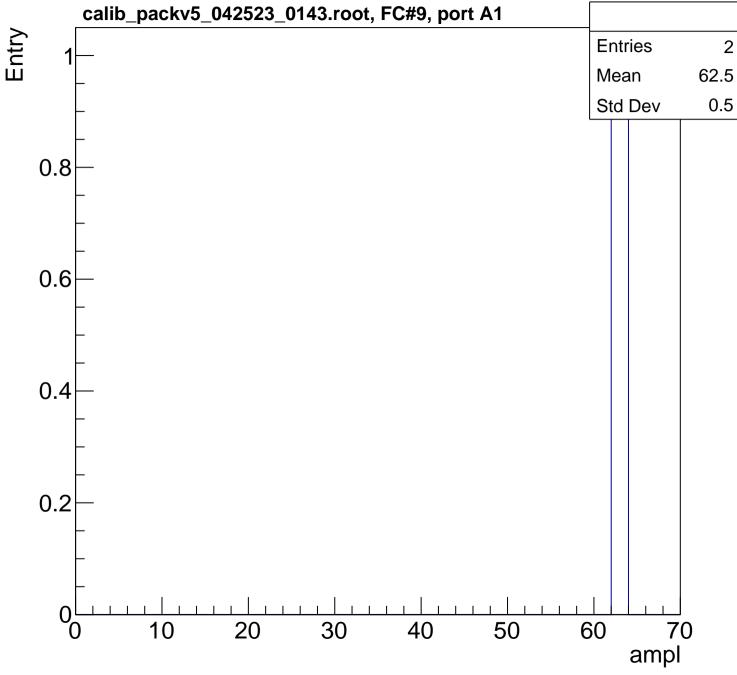




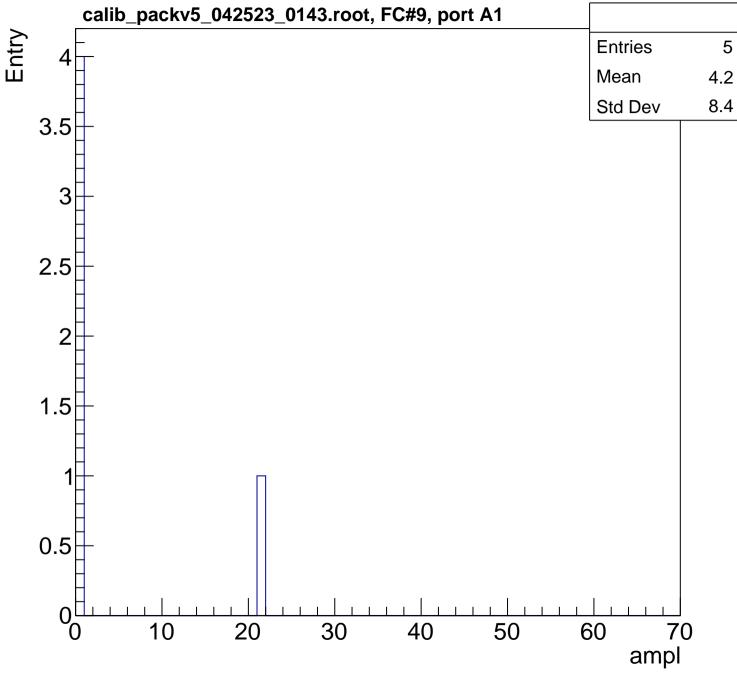


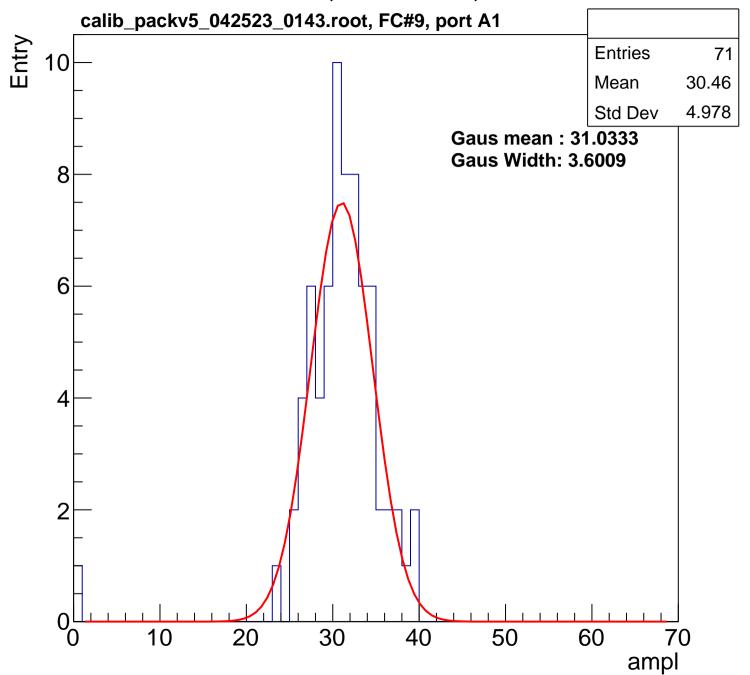


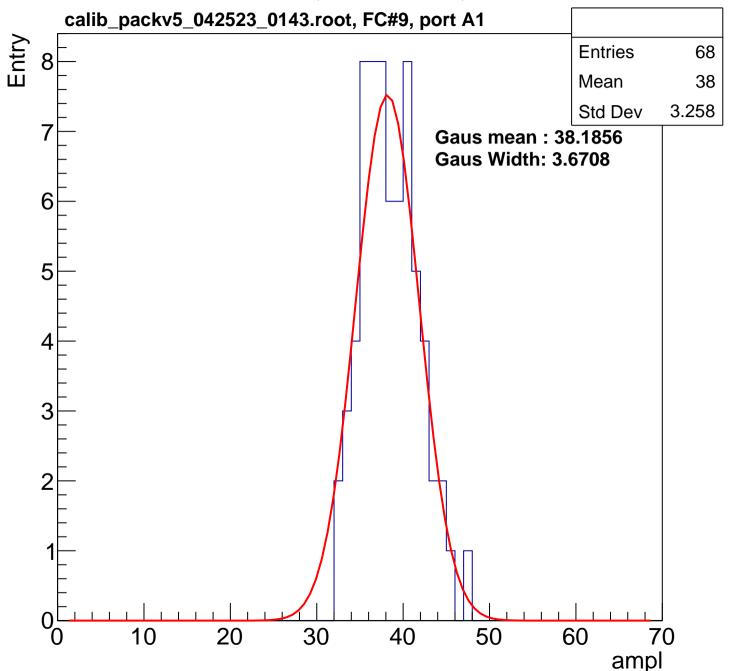


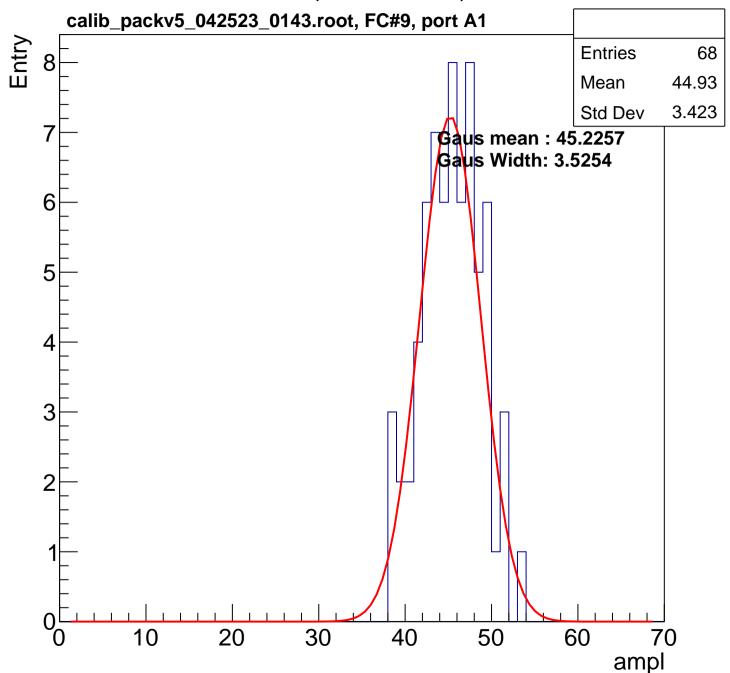


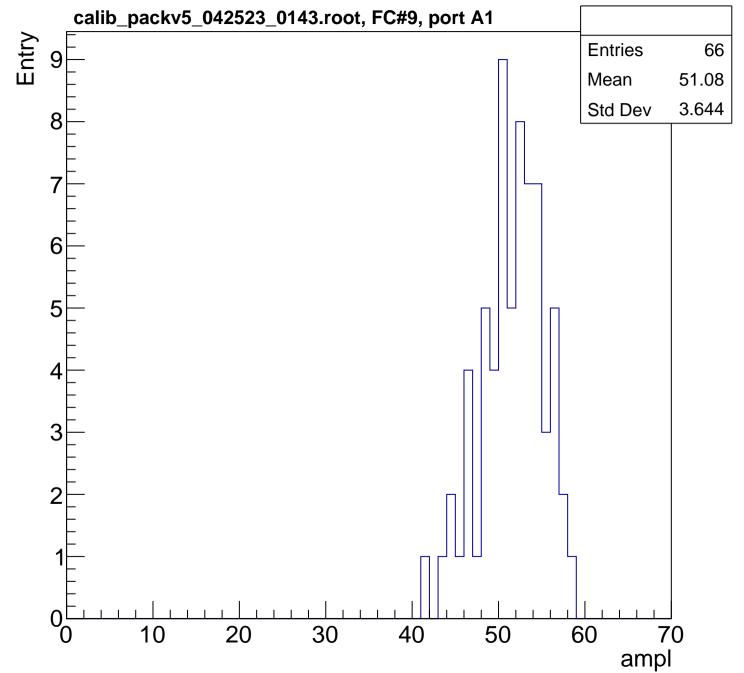
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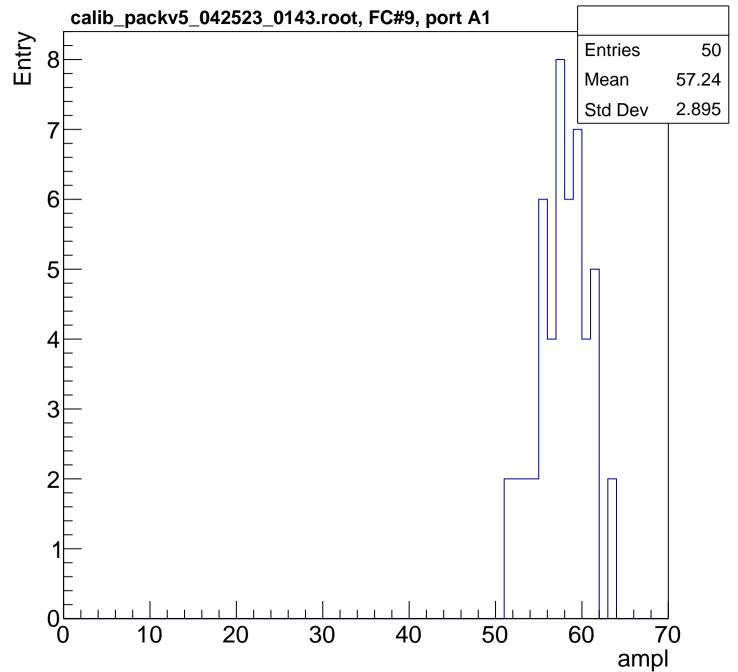


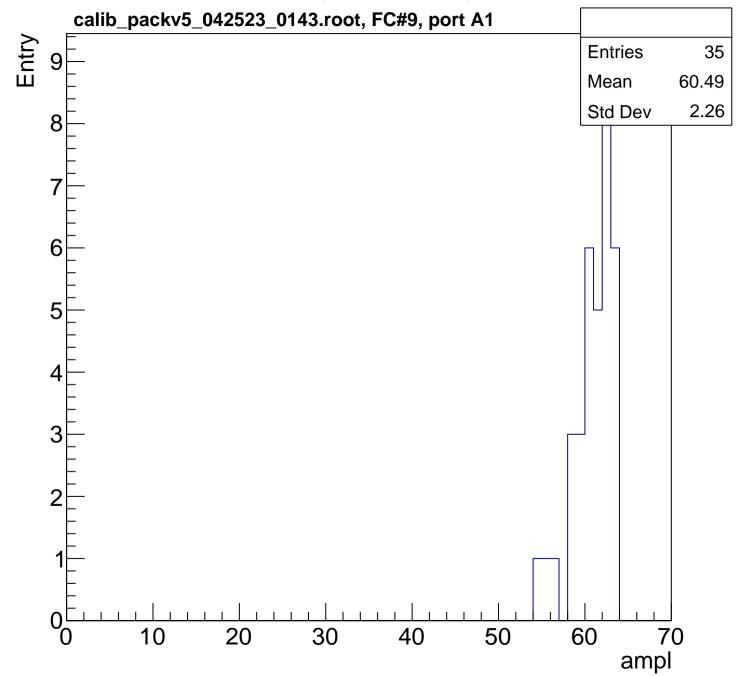


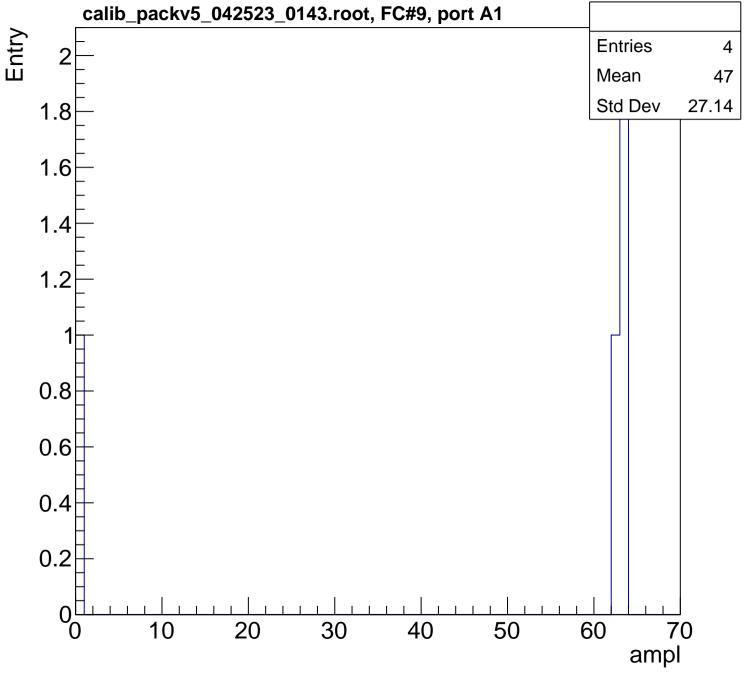










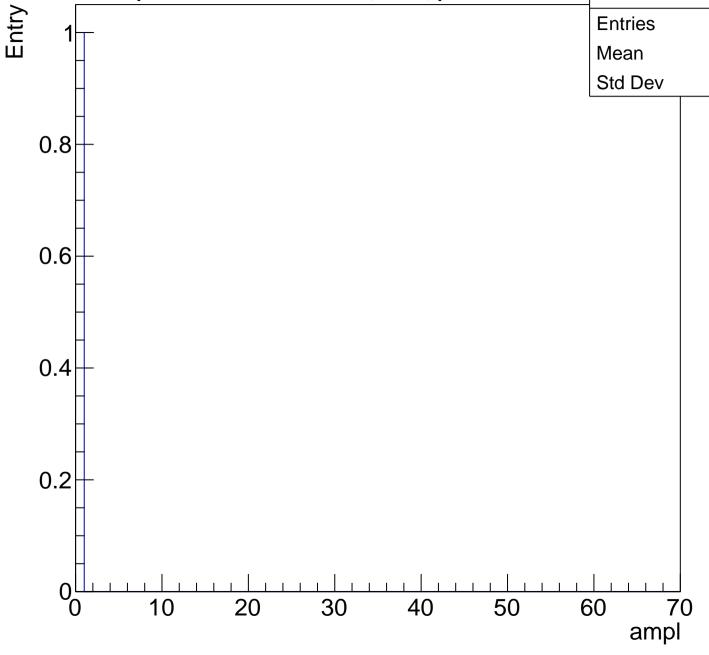


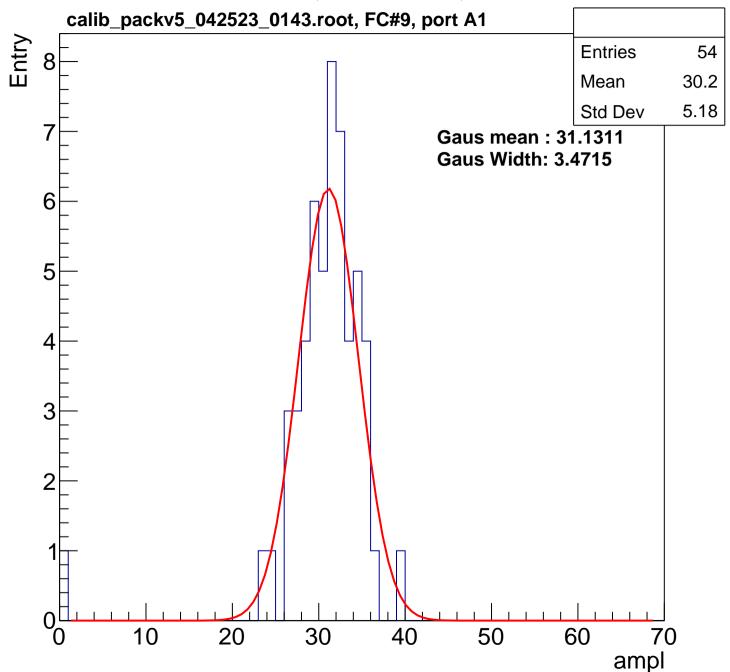
B0L001S, U3-ch72, adc7 calib_packv5_042523_0143.root, FC#9, port A1 **Entries** Mean

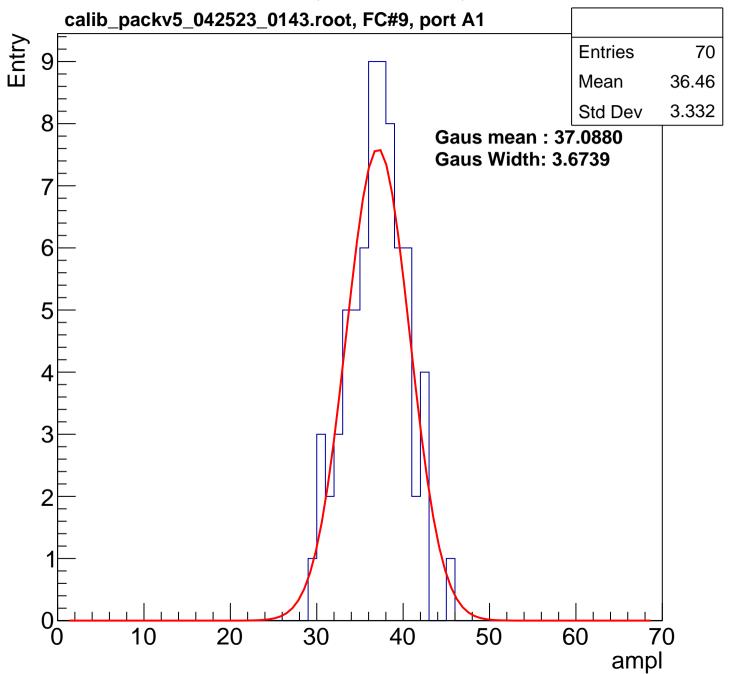
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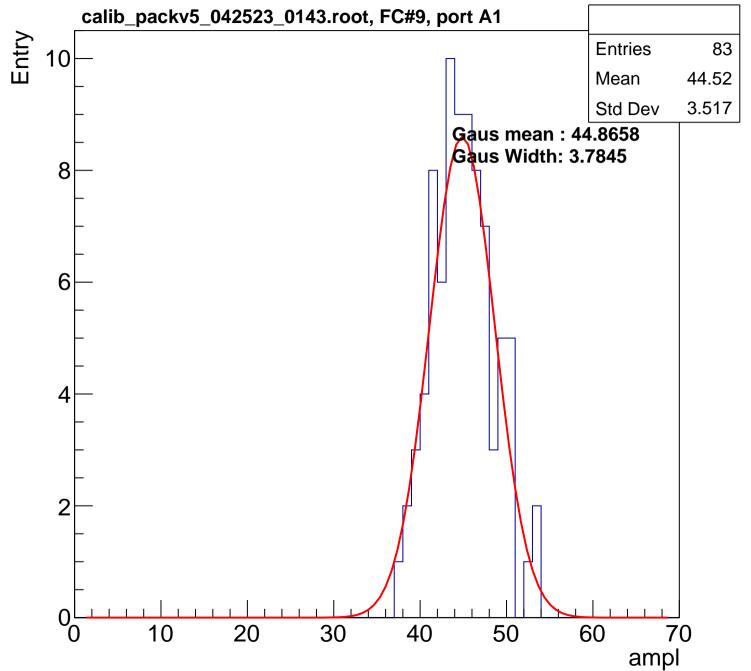
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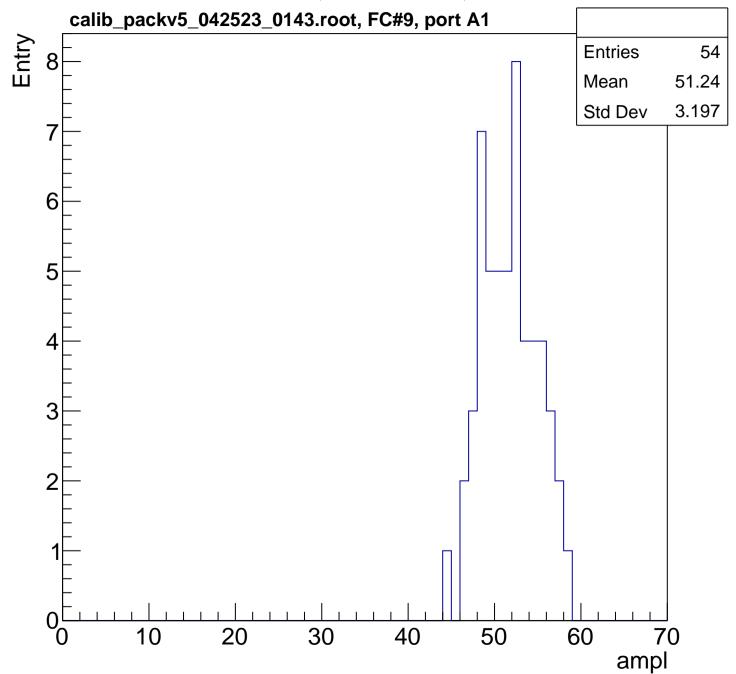
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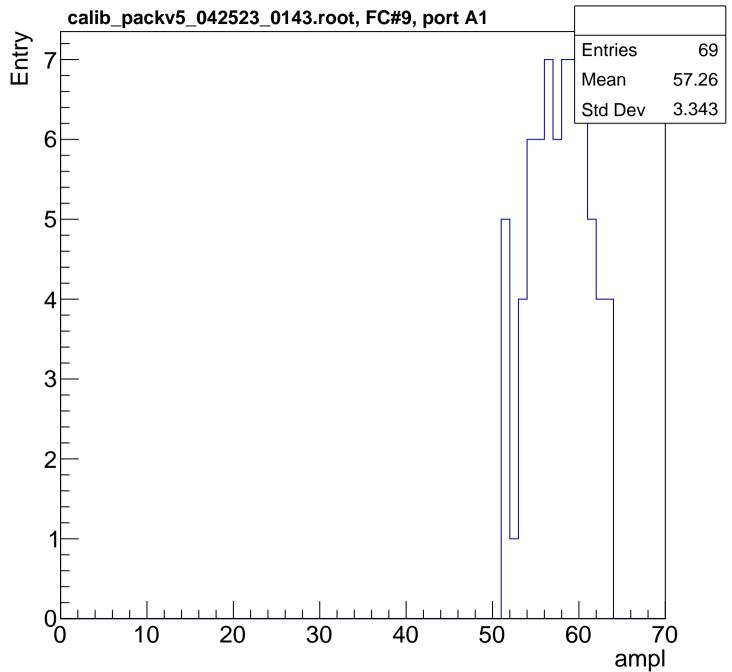


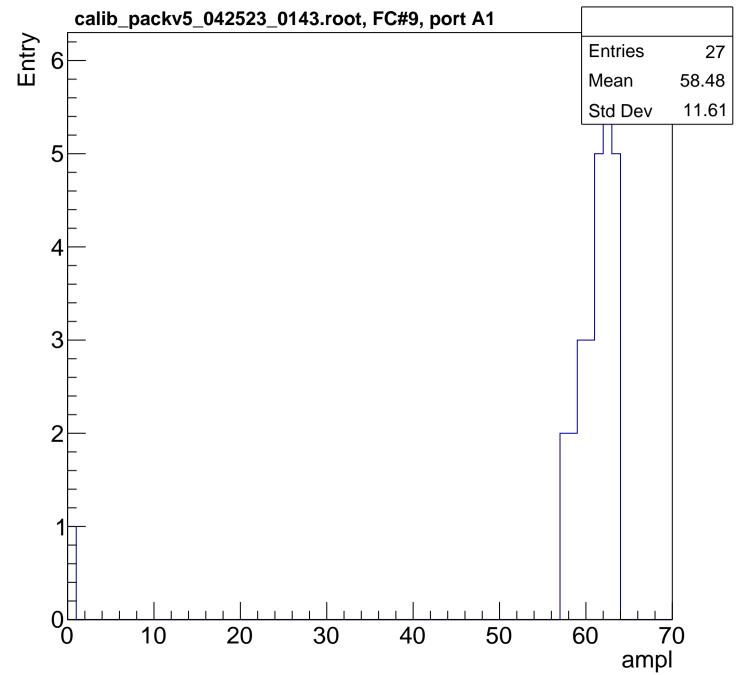


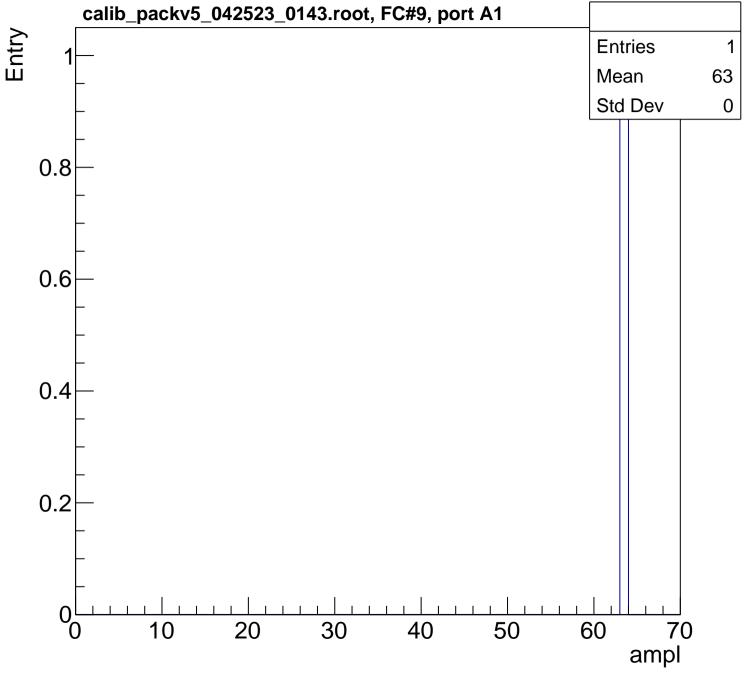


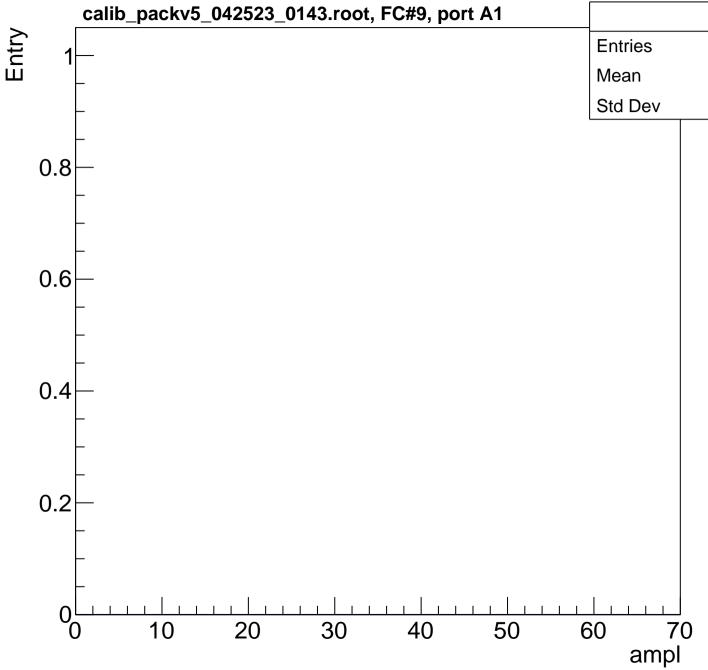


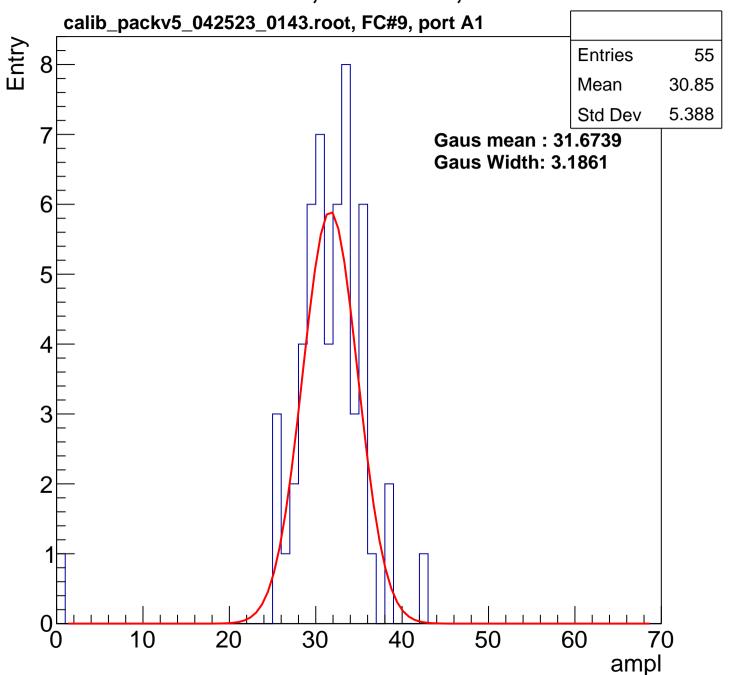


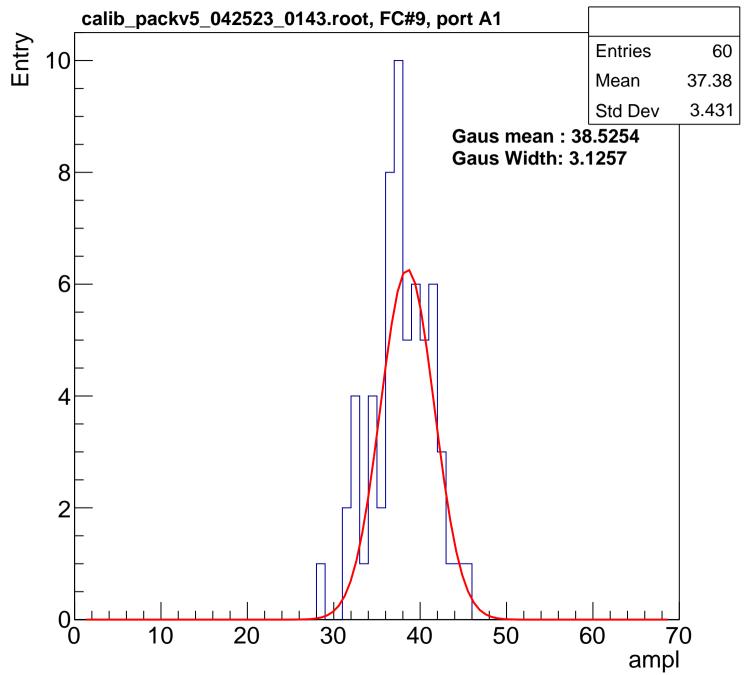


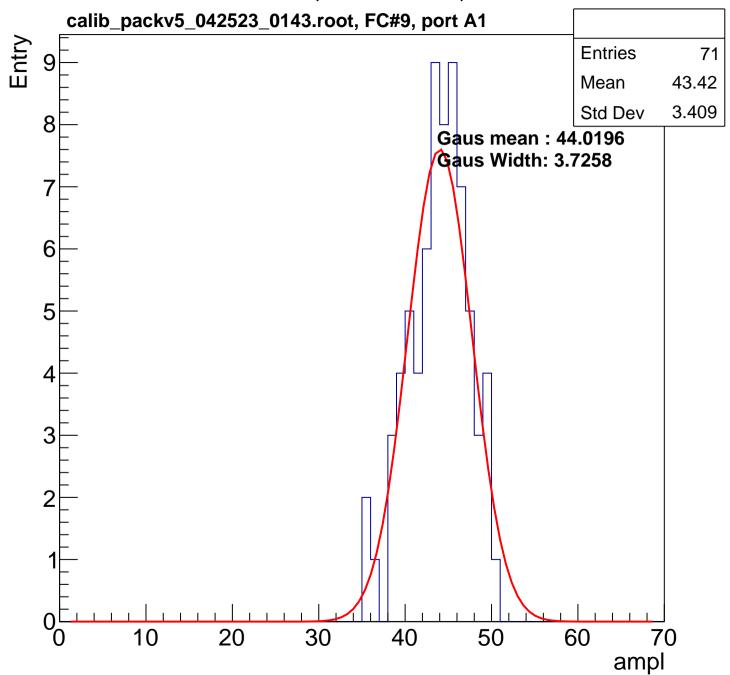


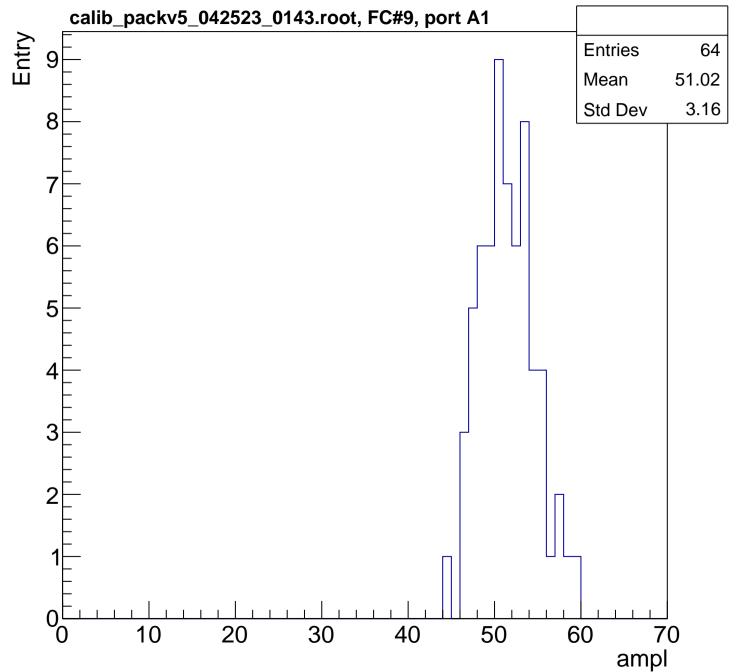


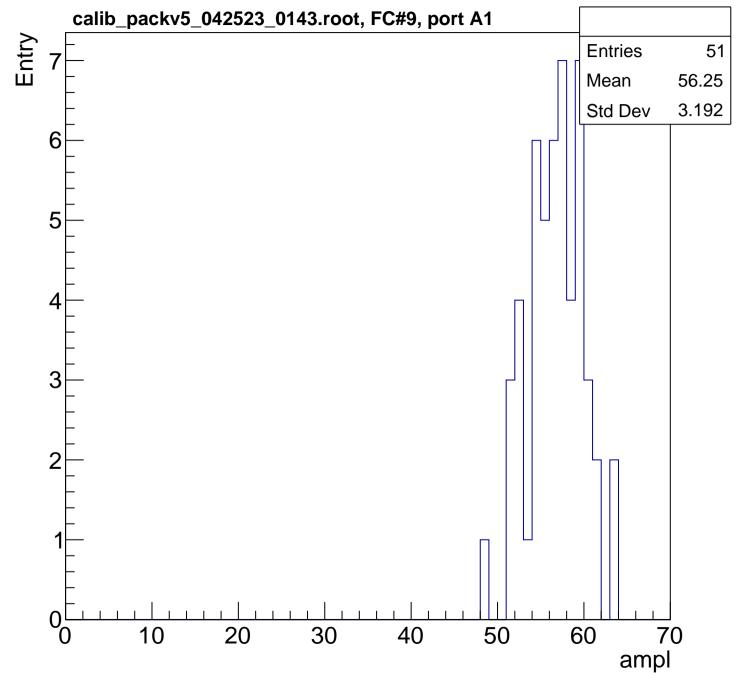


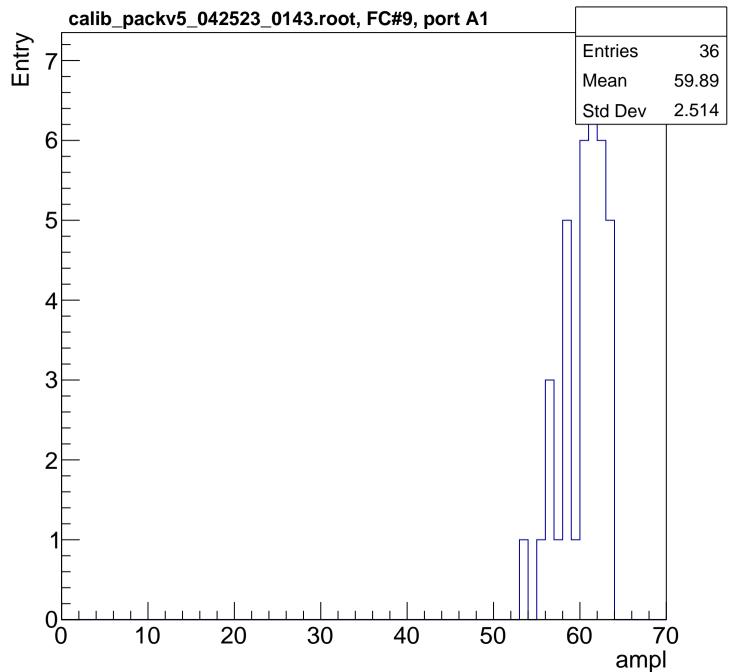


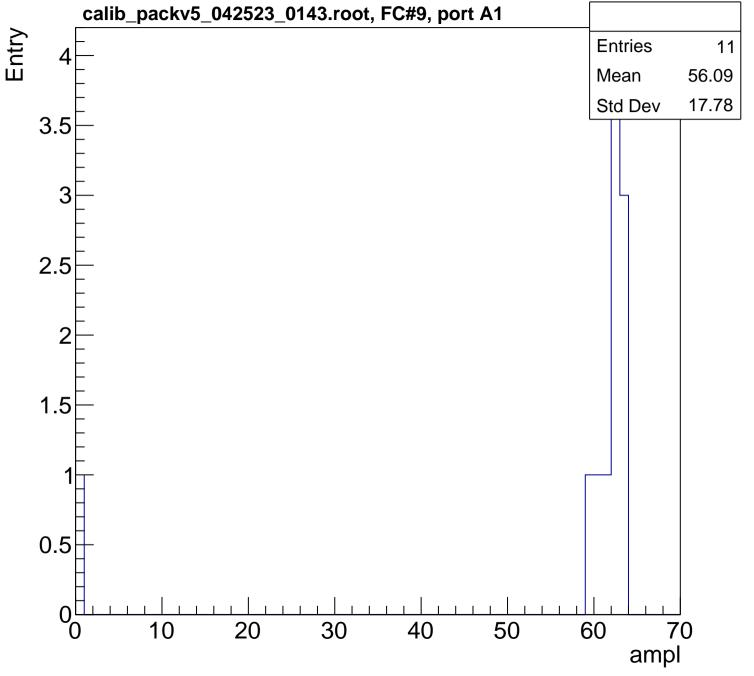




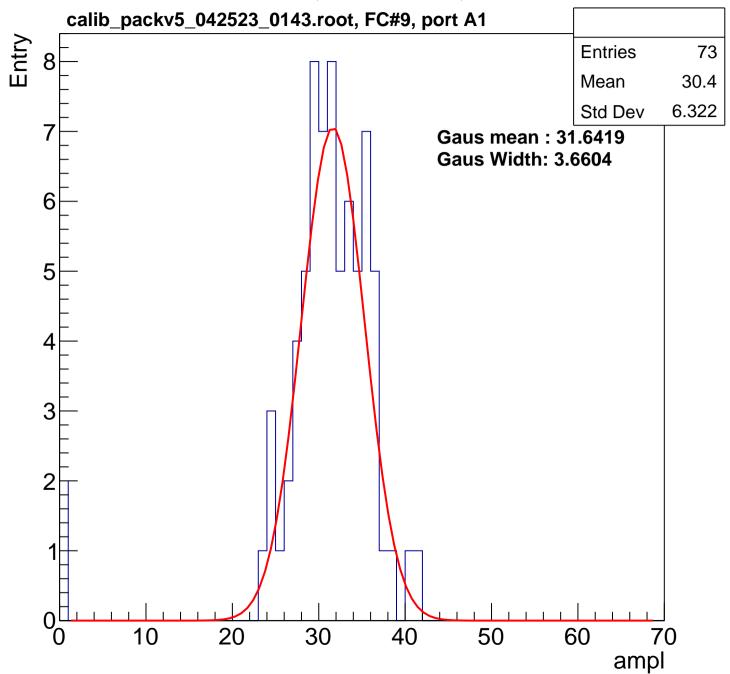


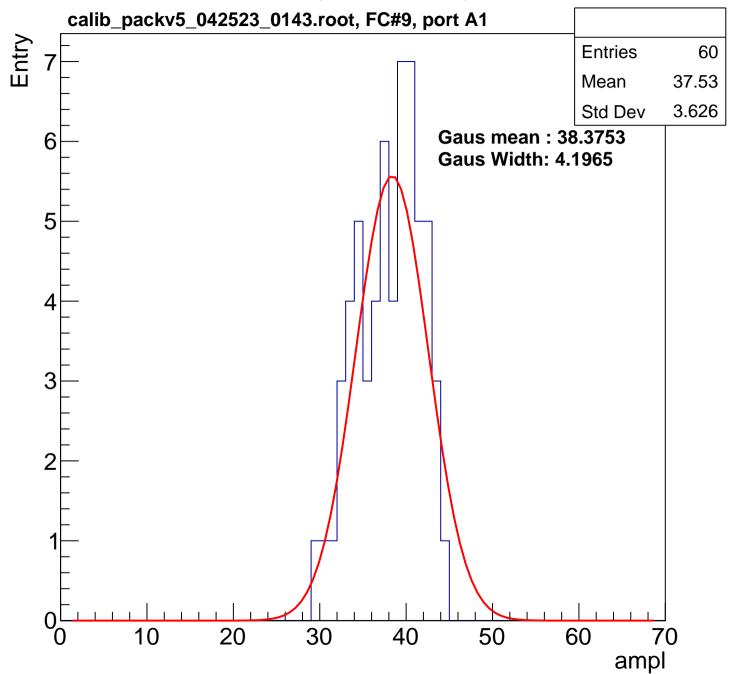


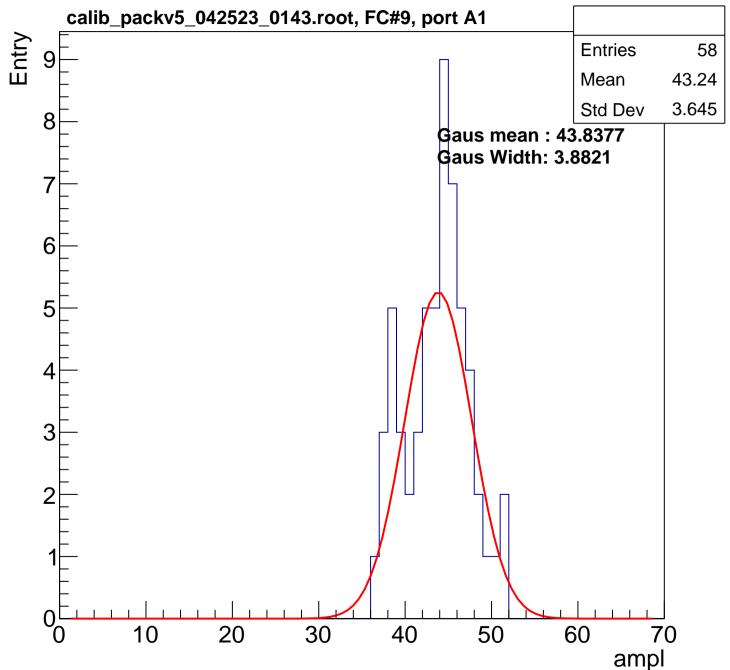


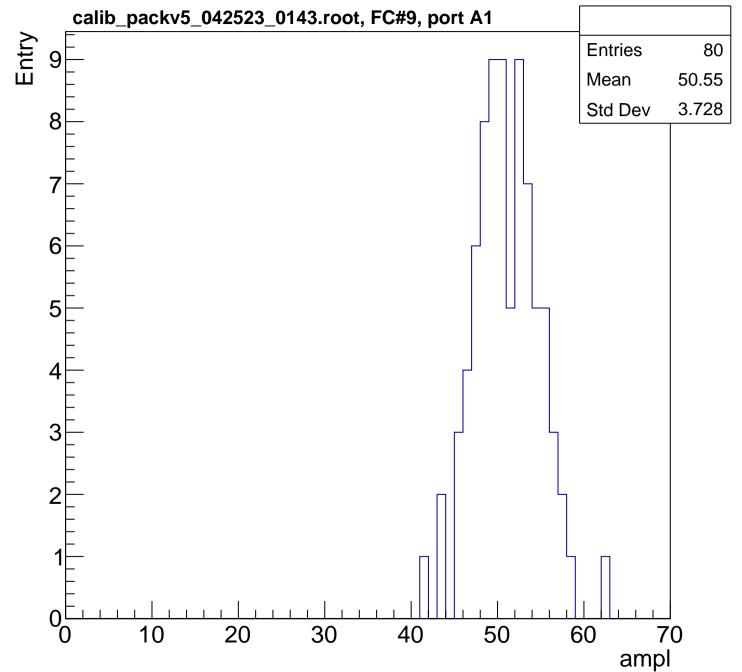


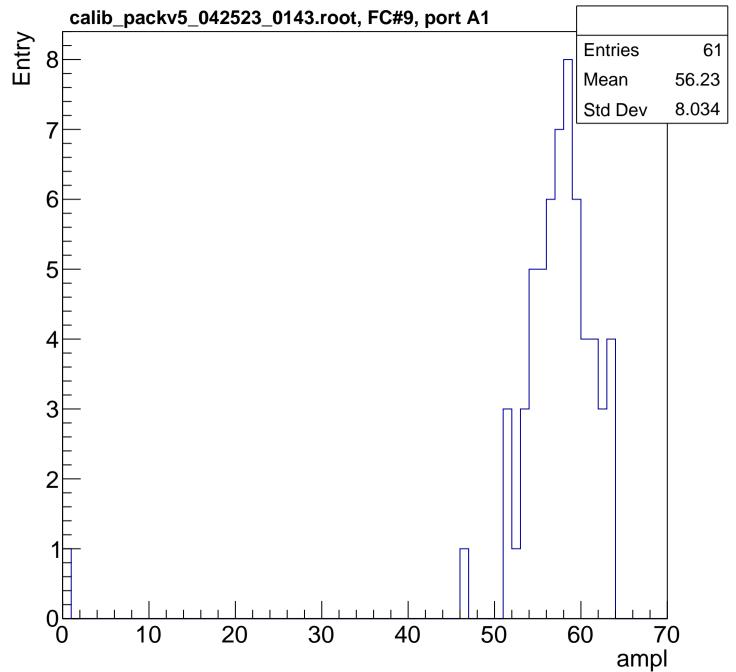


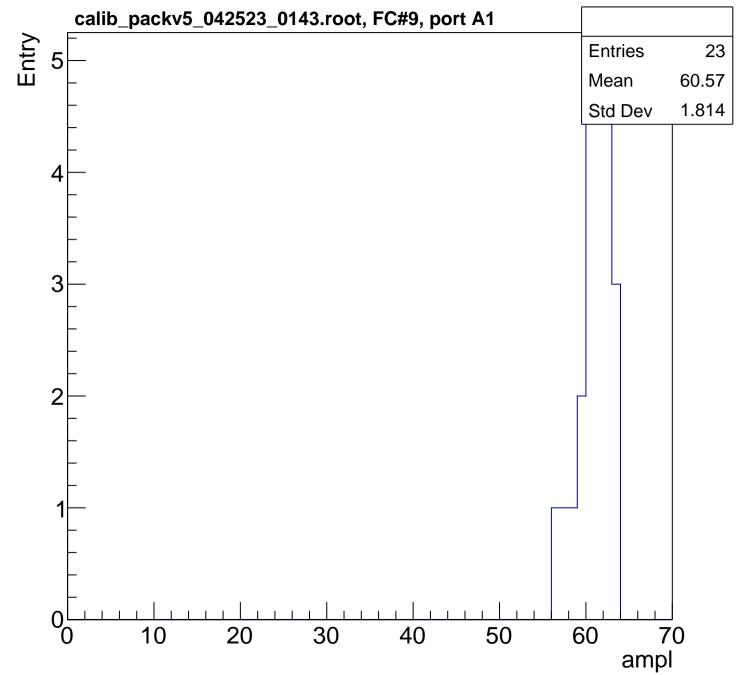


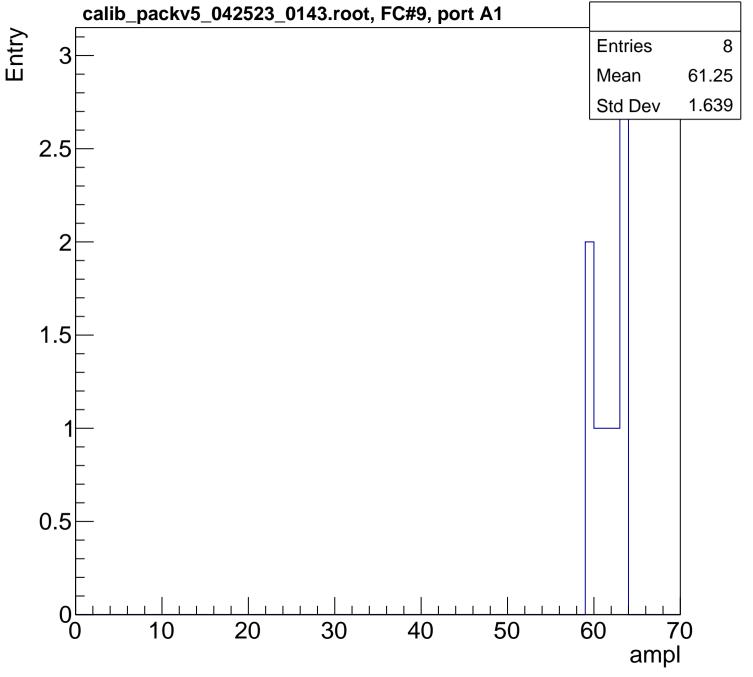


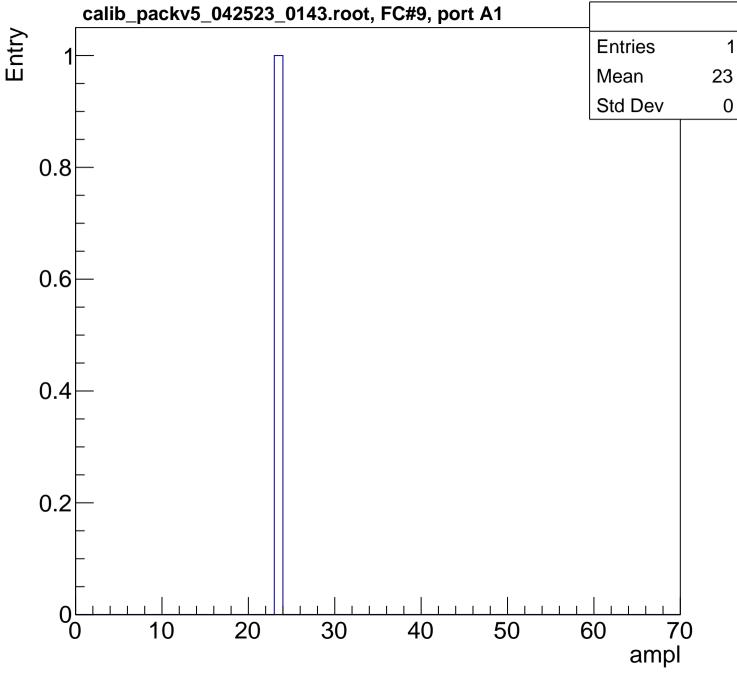


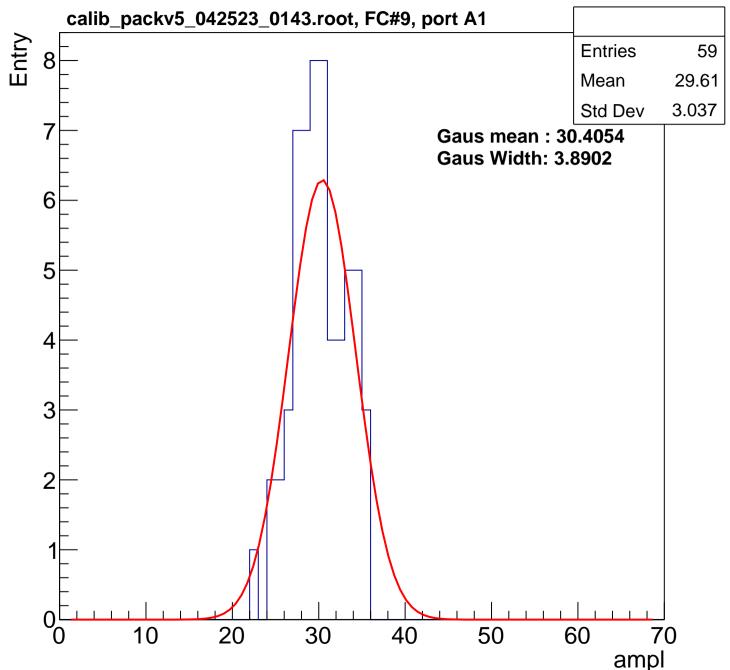


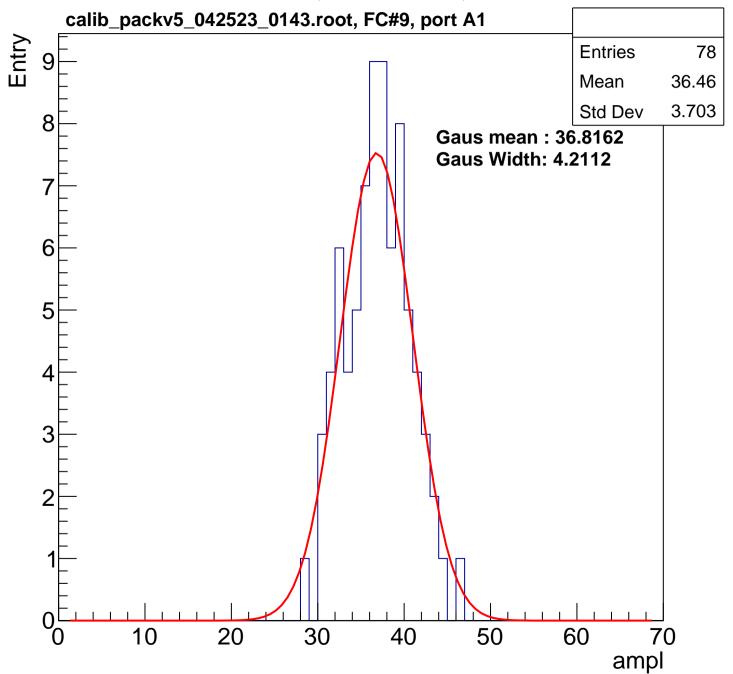


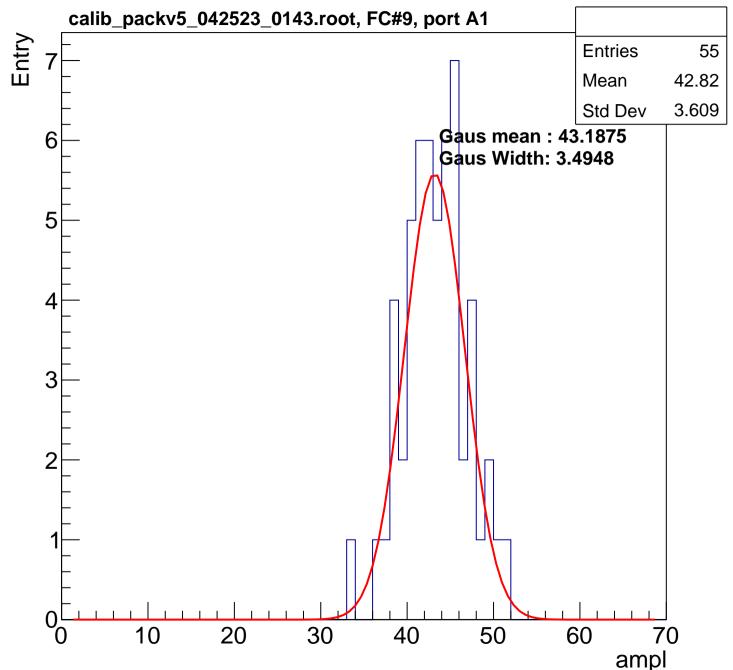


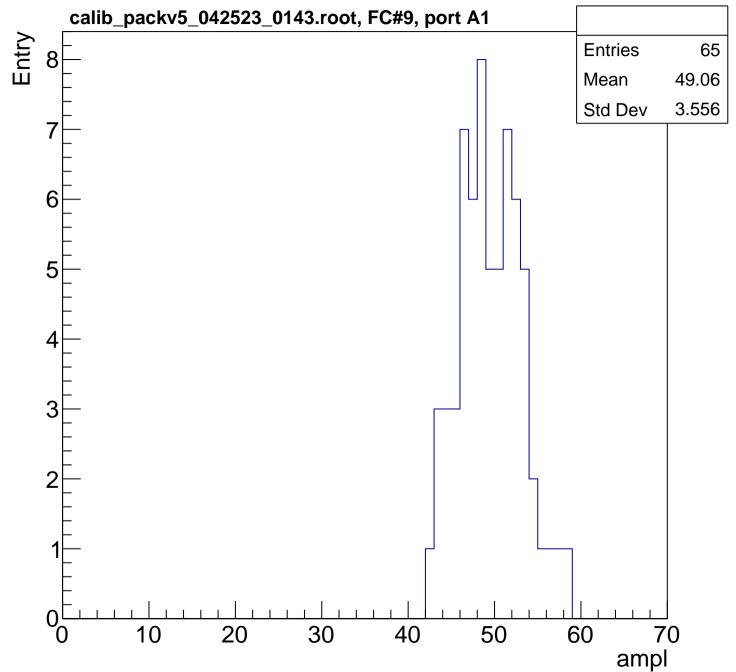


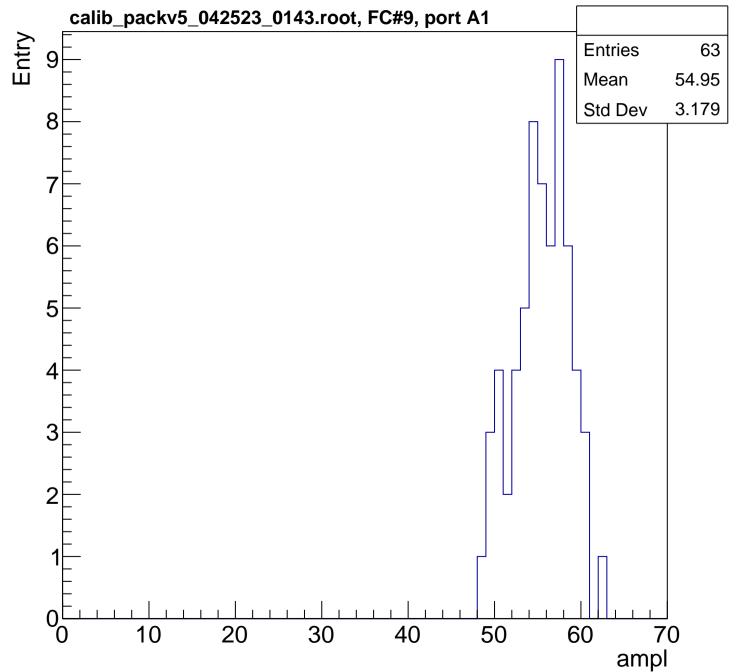


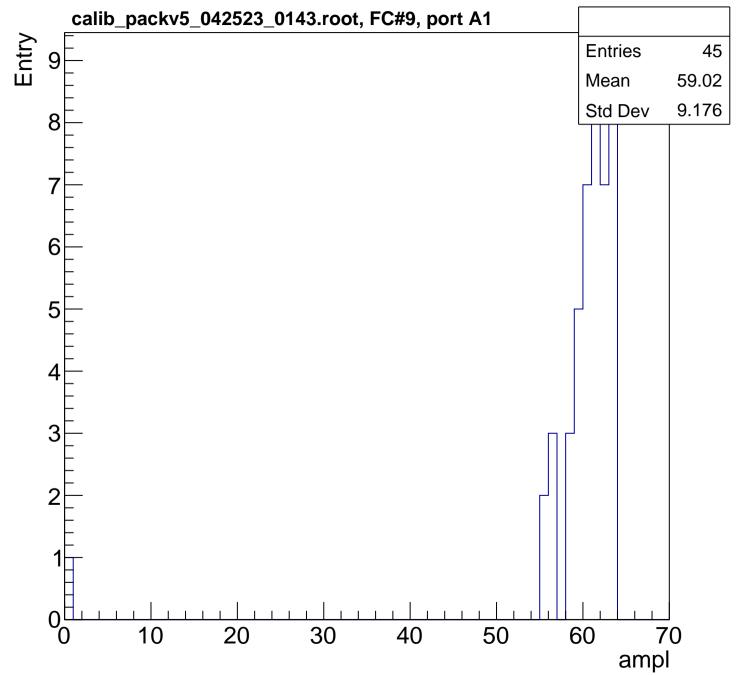


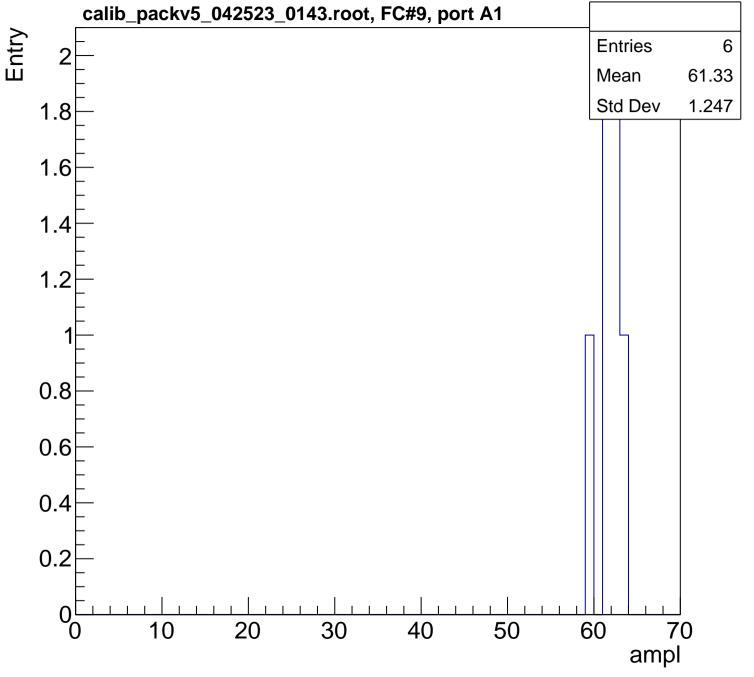


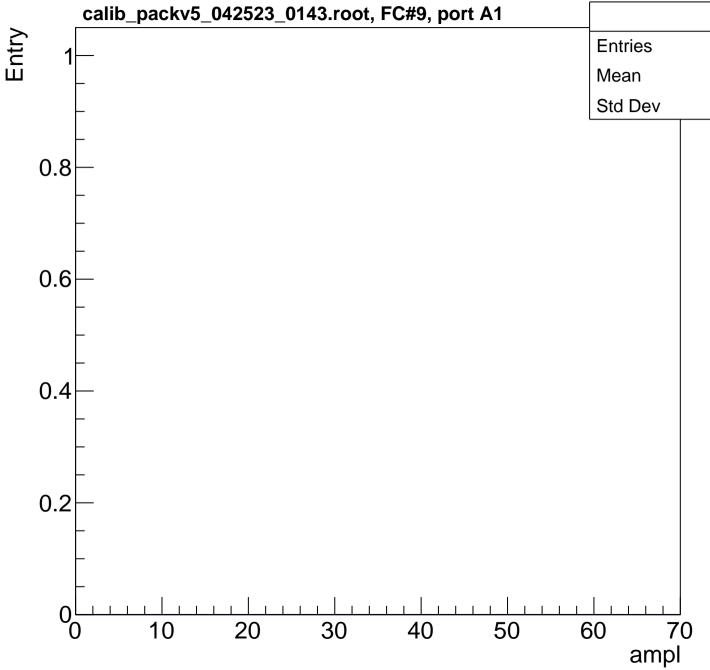


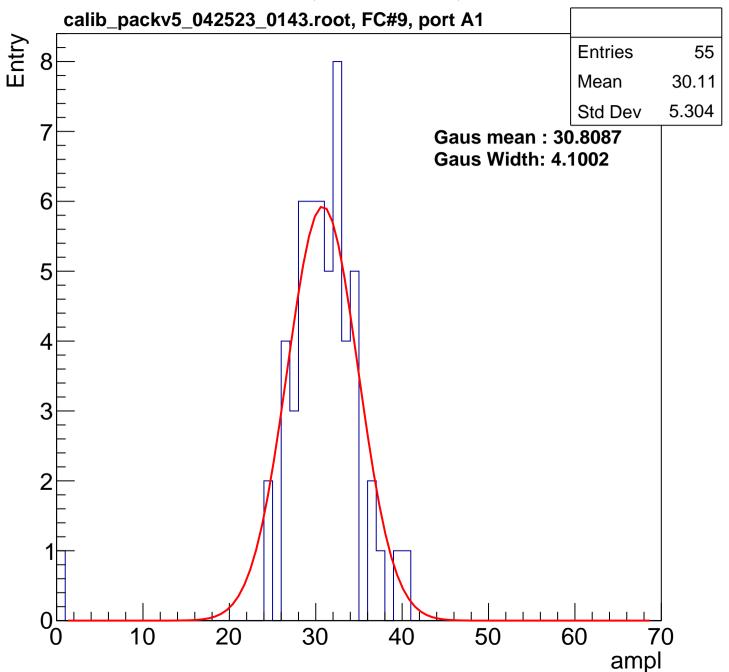


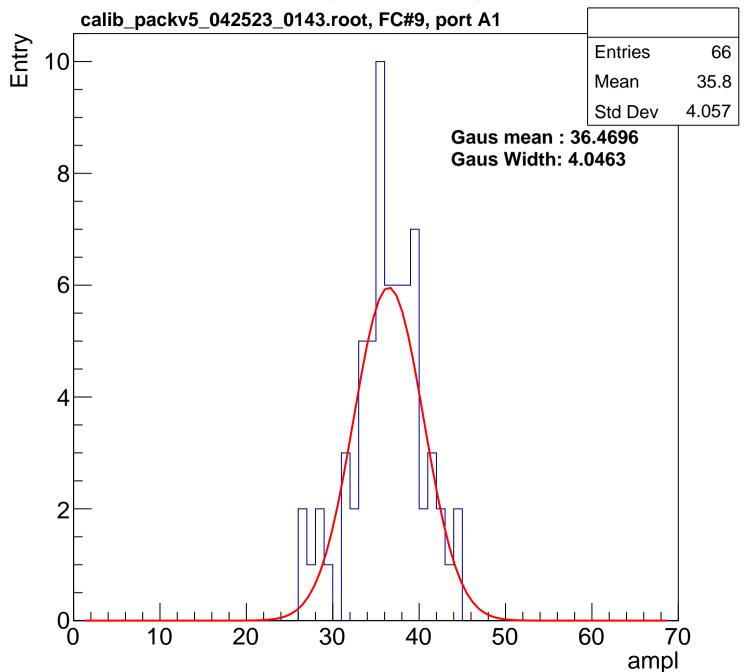


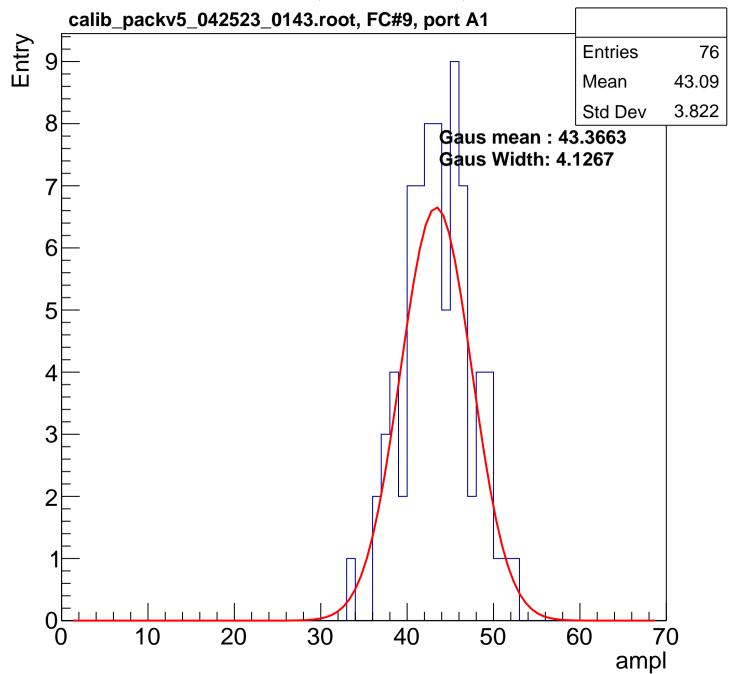


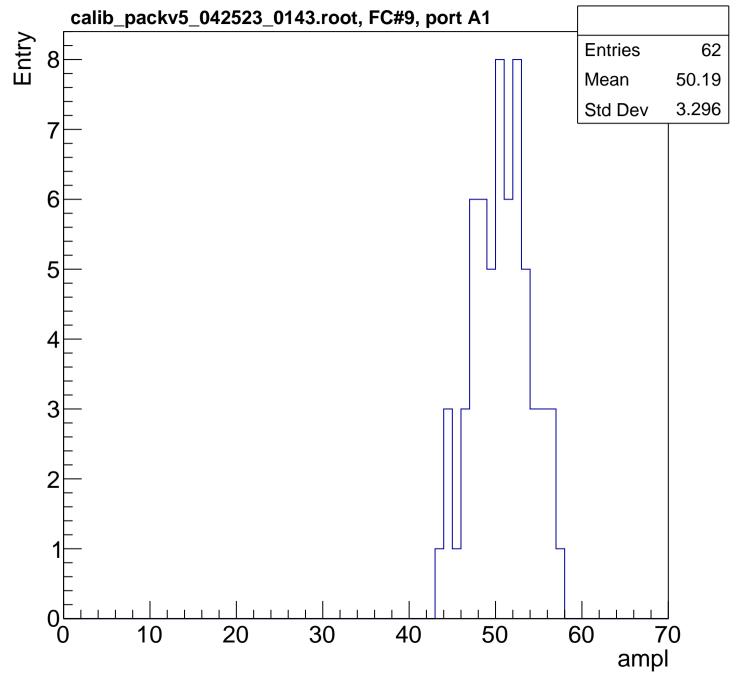


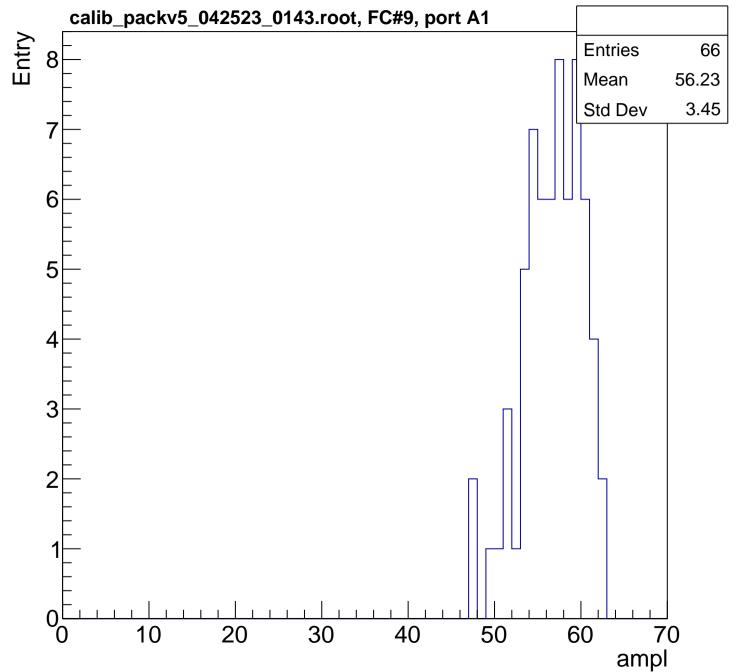


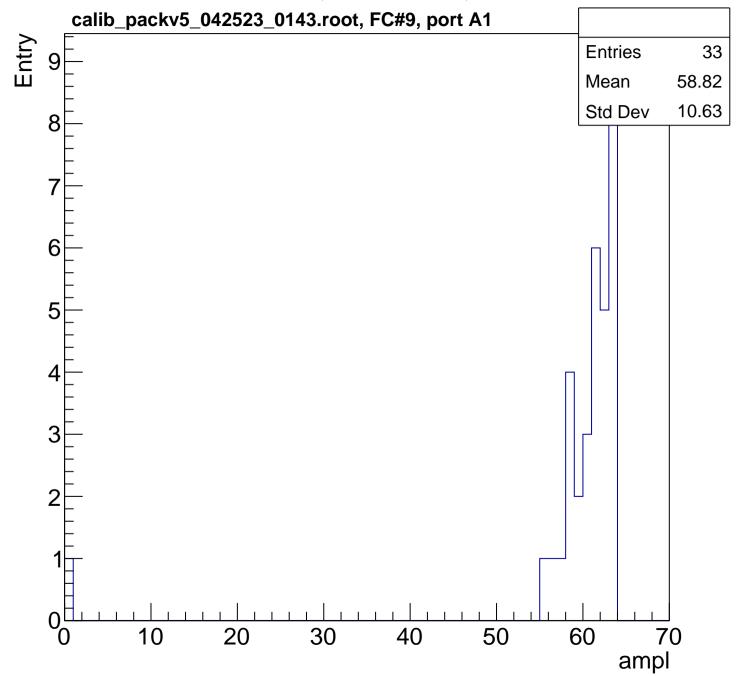


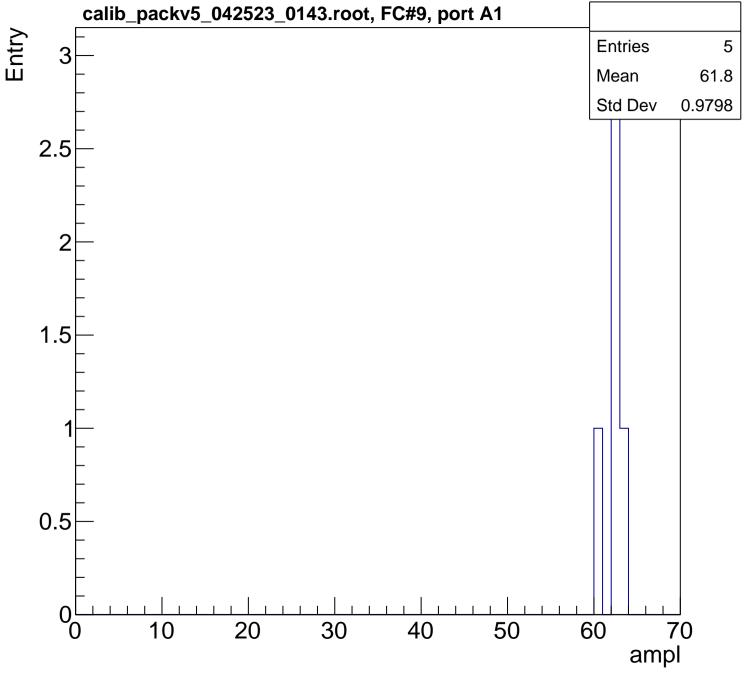




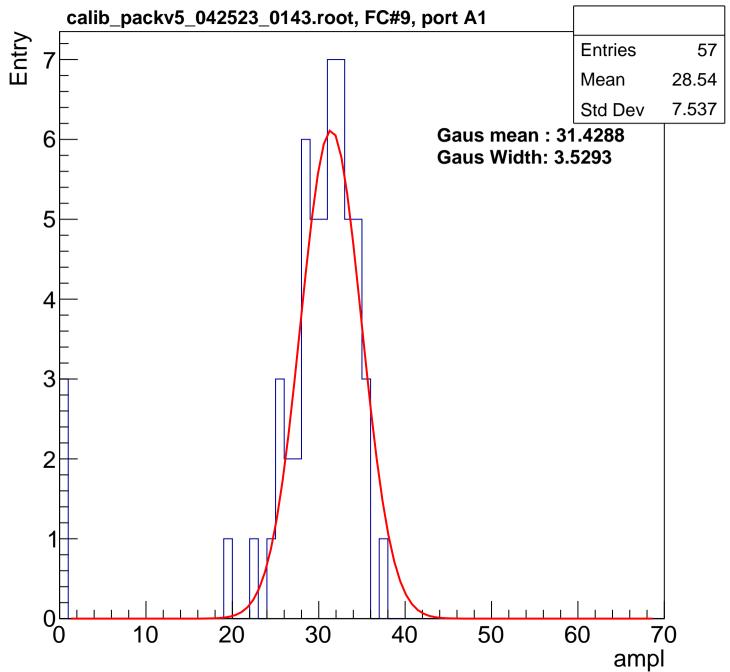


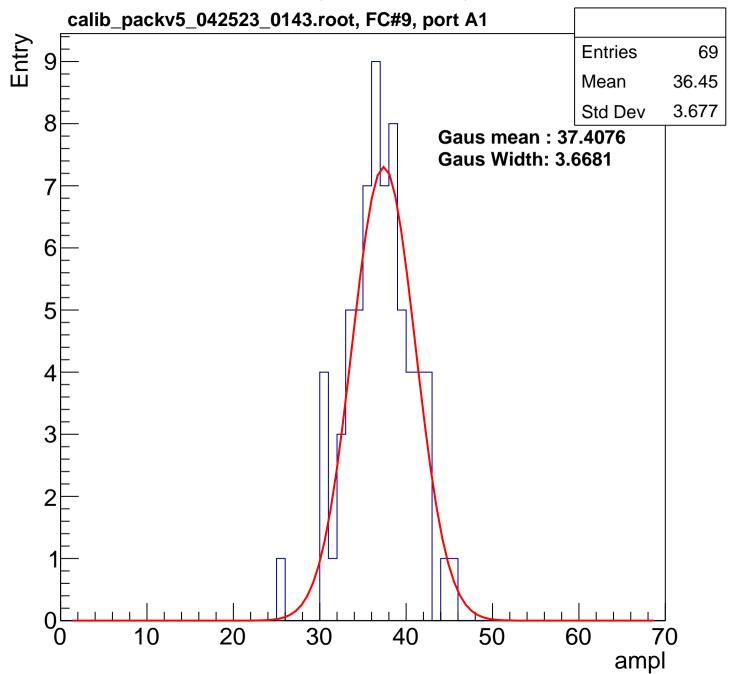


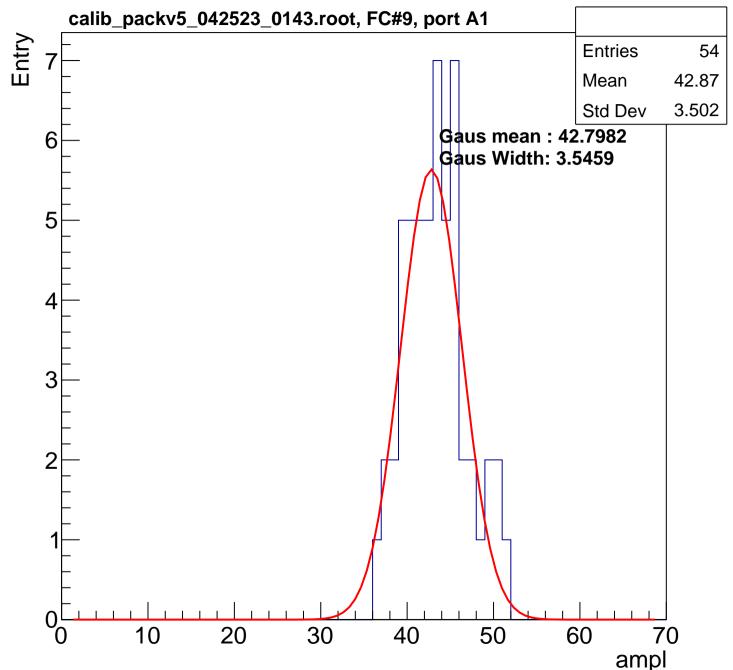


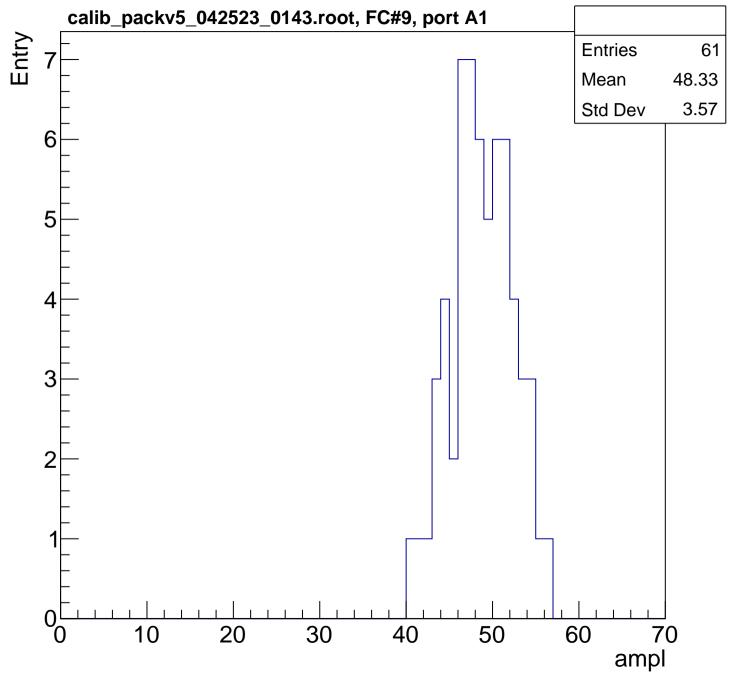


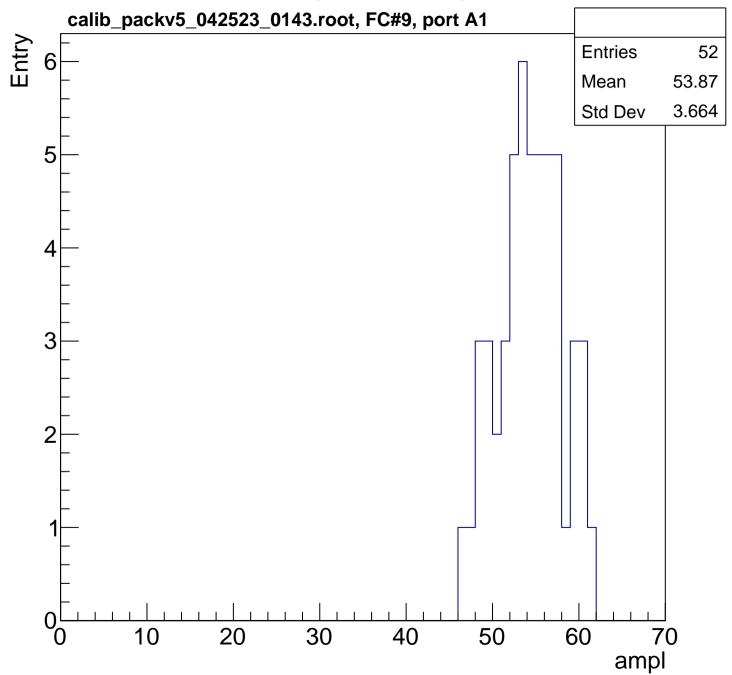
B0L001S, U3-ch77, adc7 calib_packv5_042523_0143.root, FC#9, port A1 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

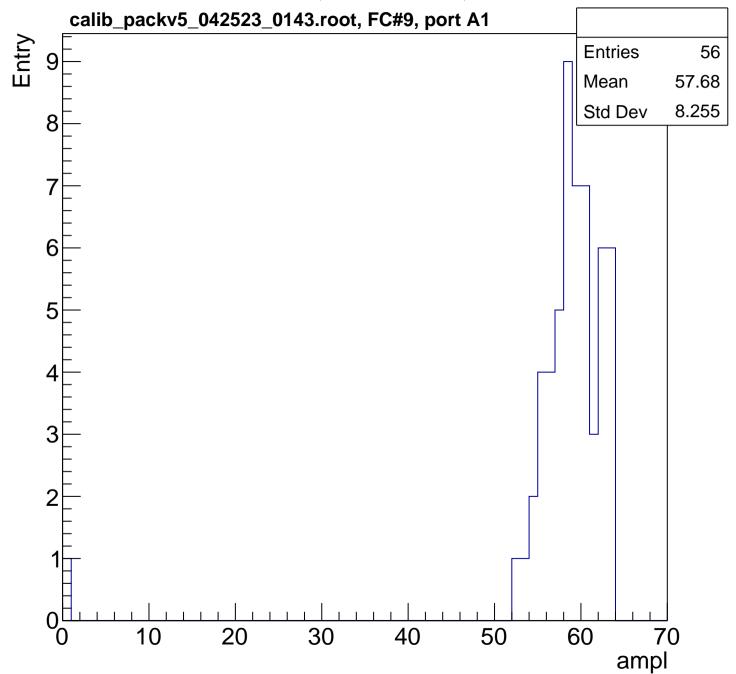


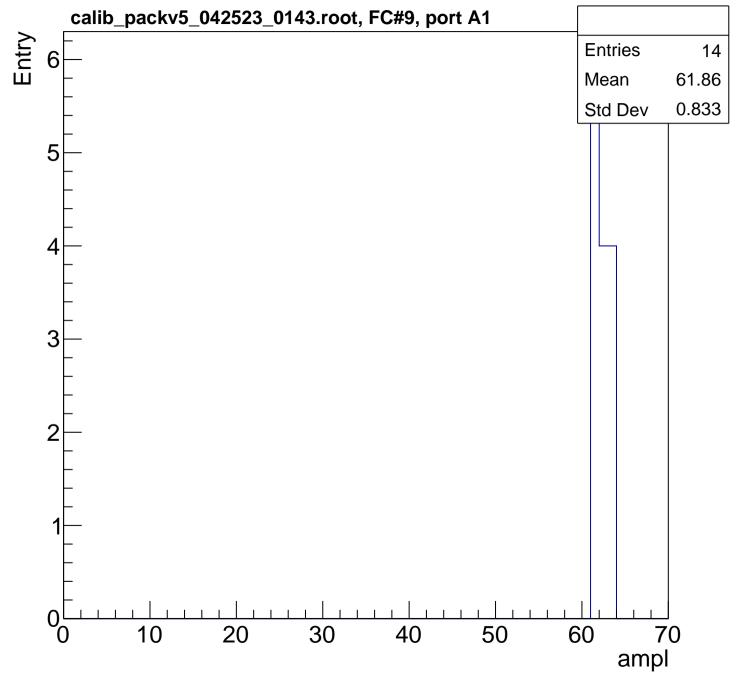


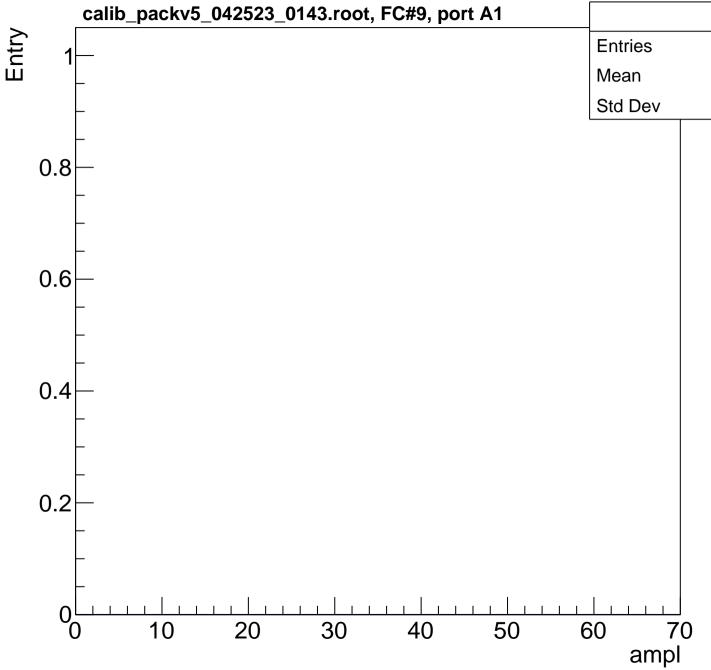


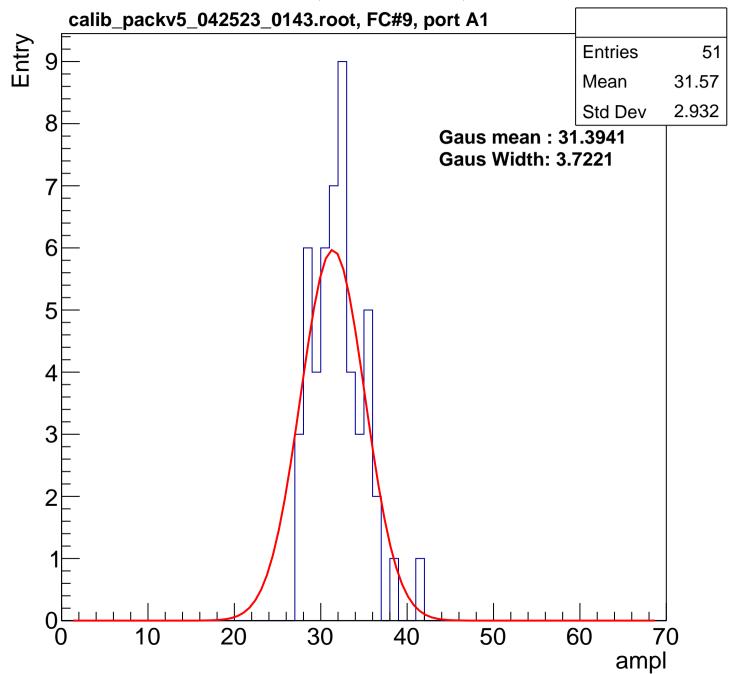


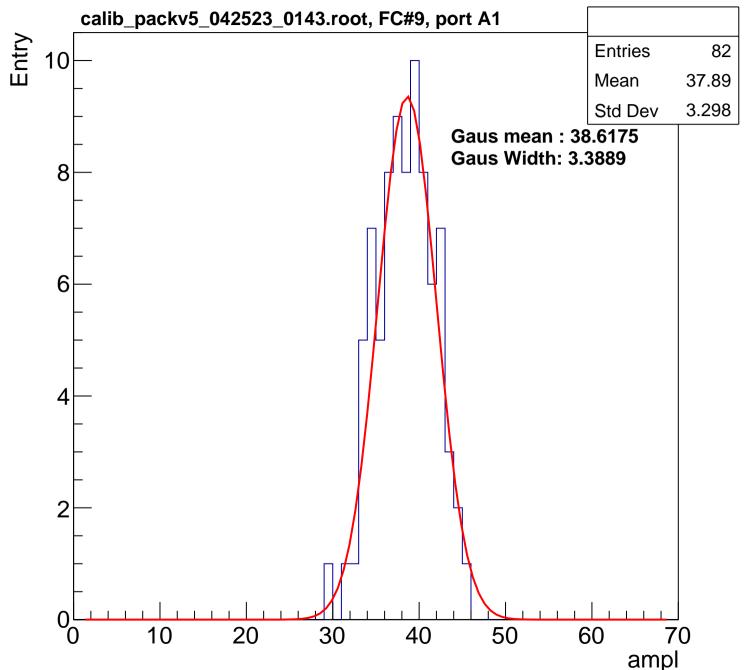


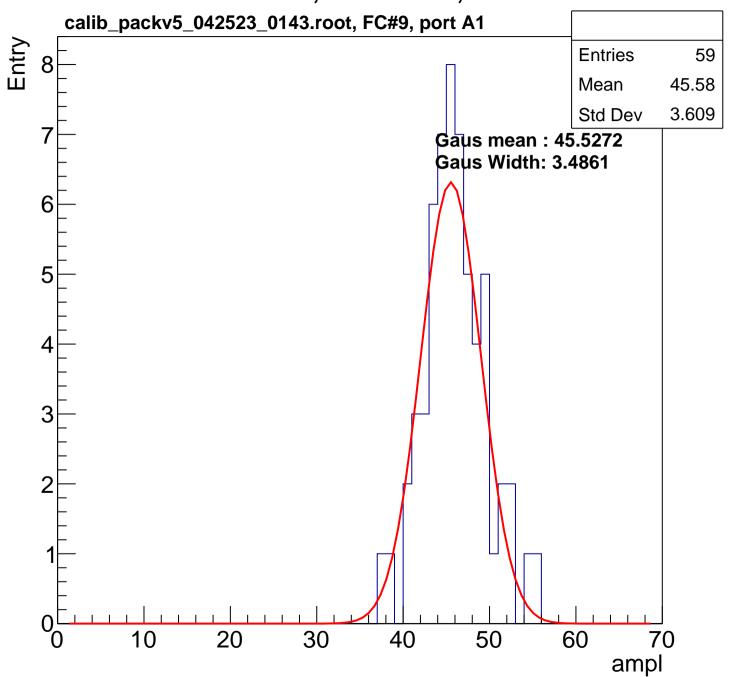


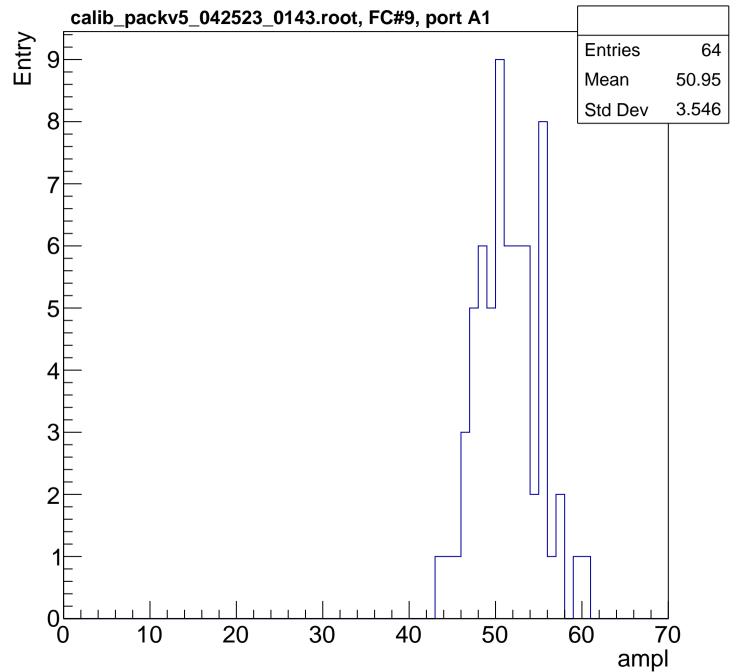


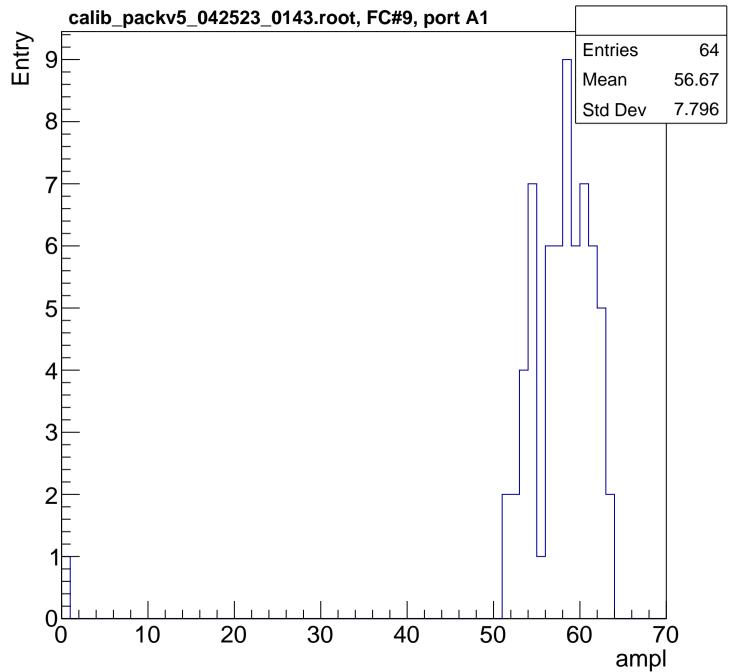


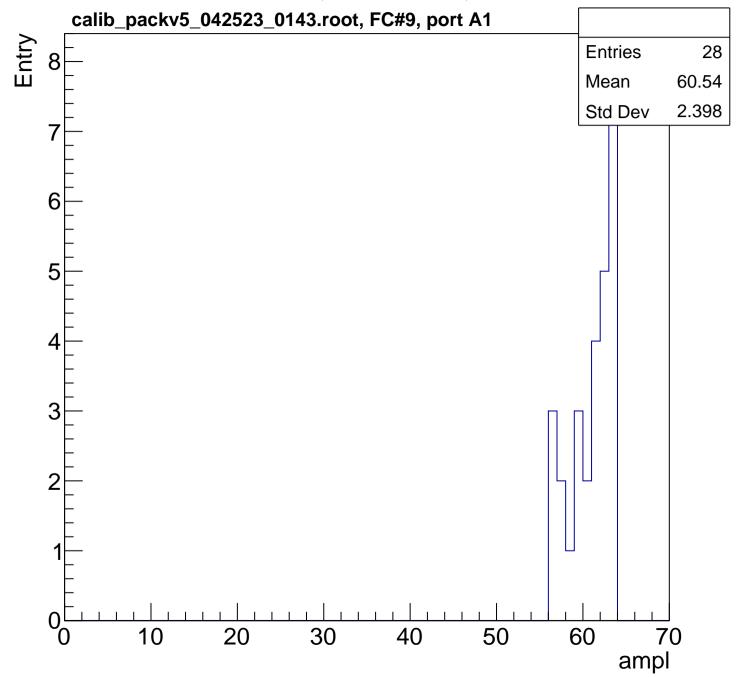


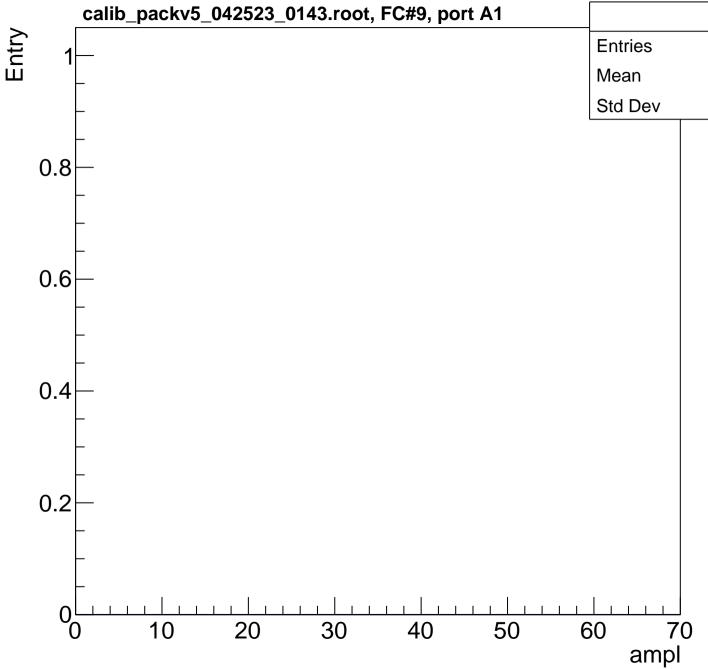




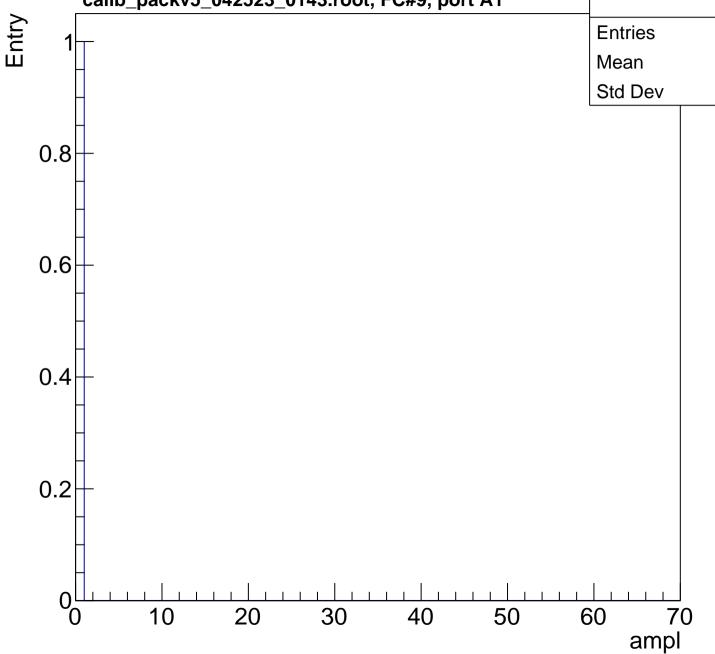


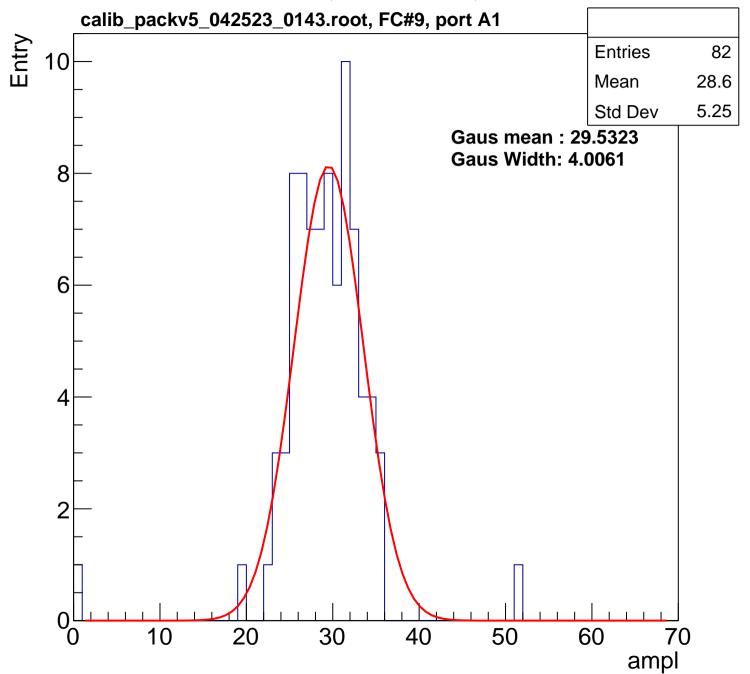


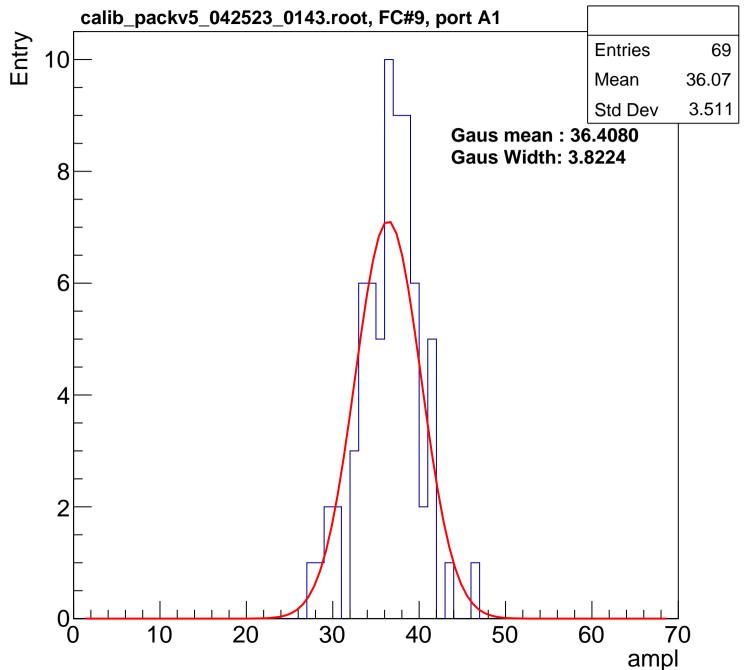


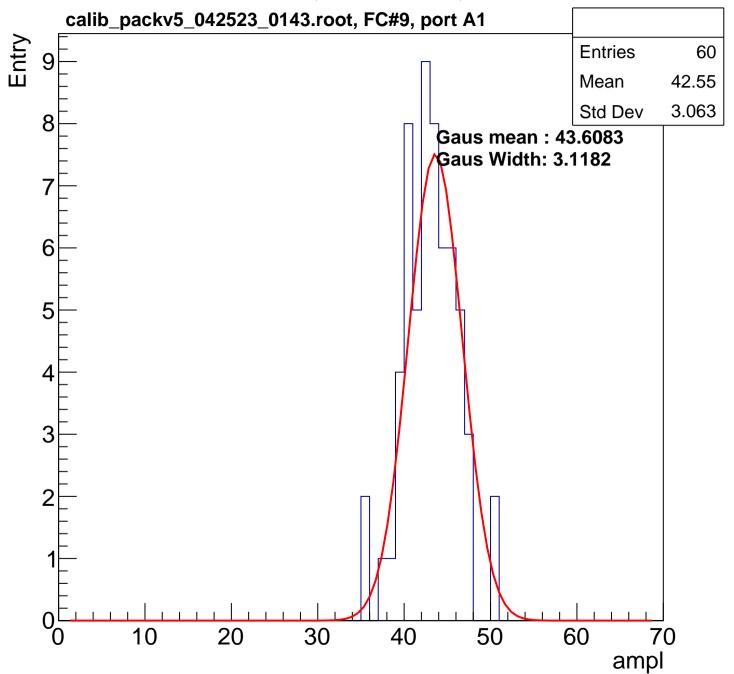


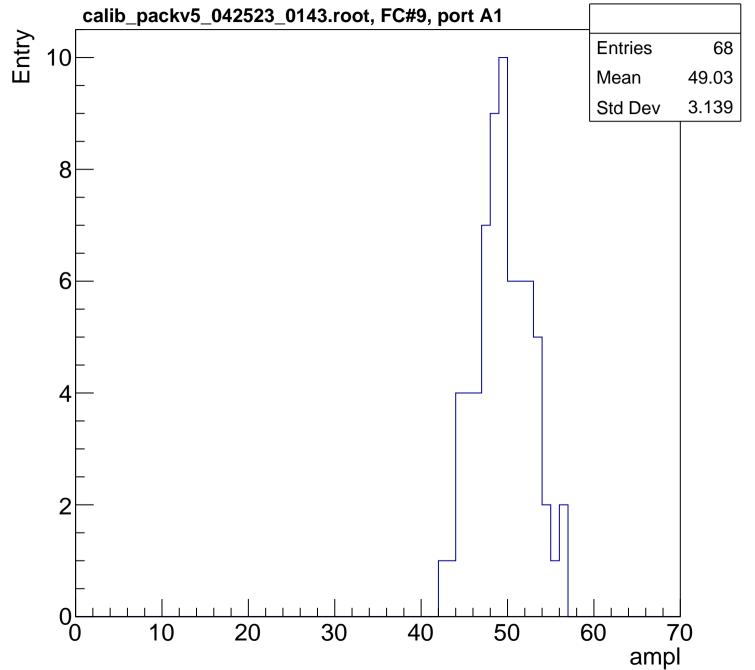
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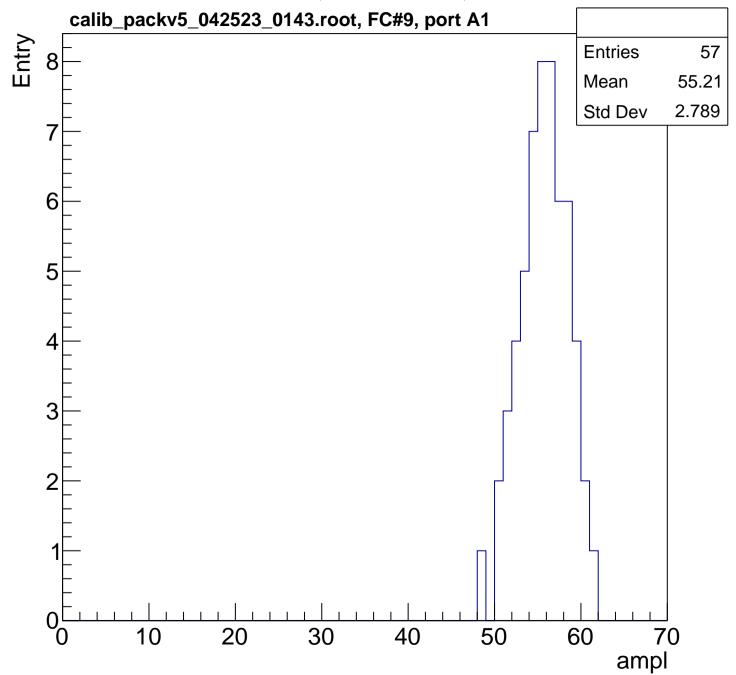


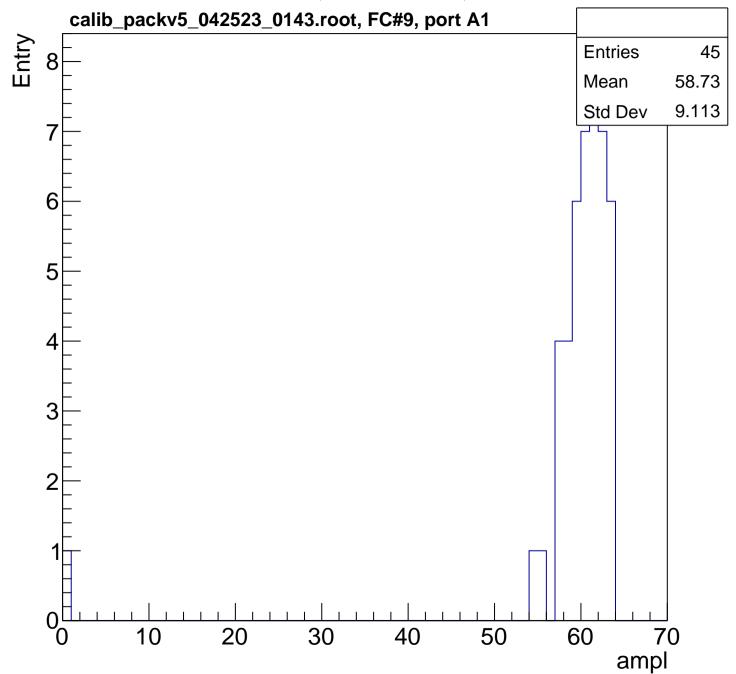


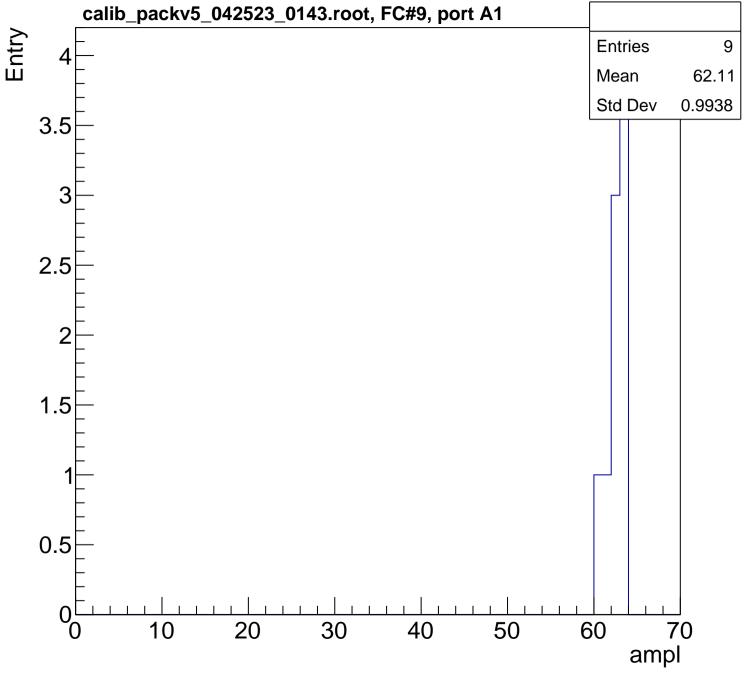




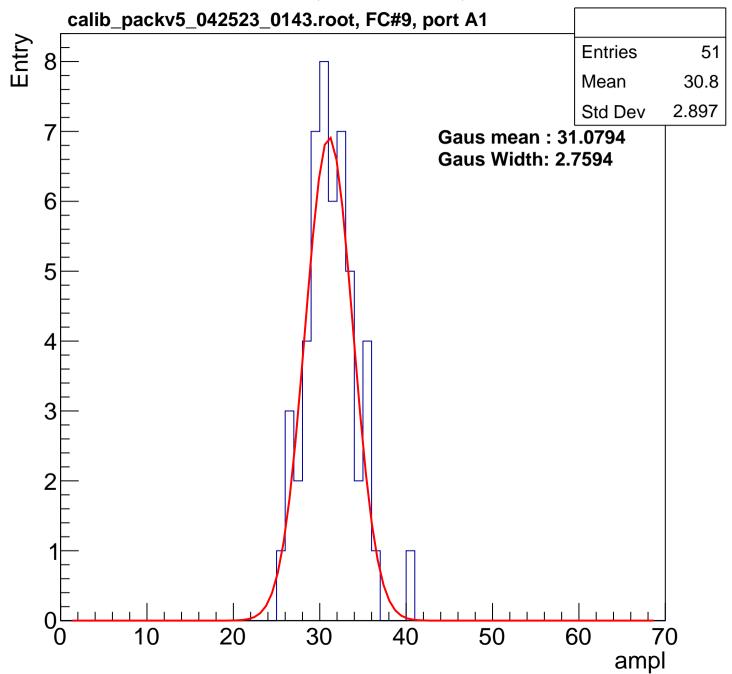


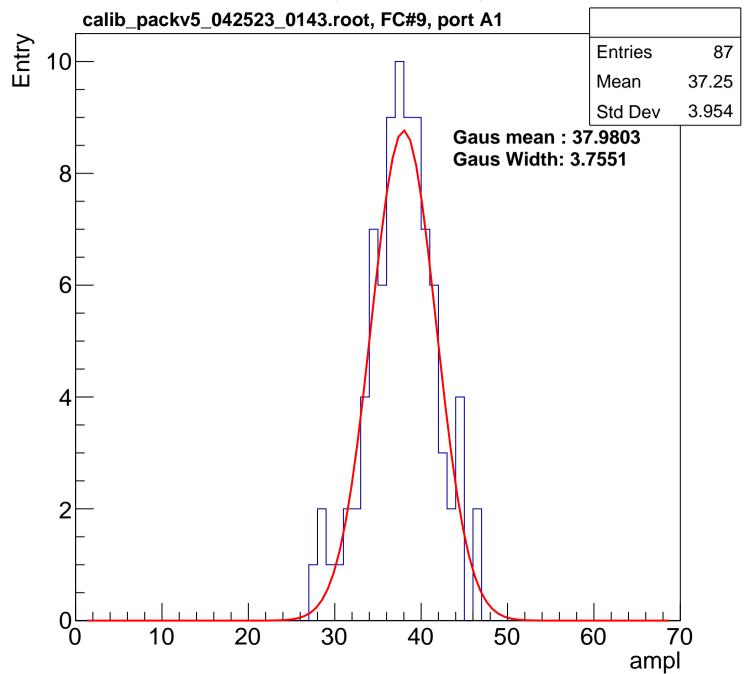


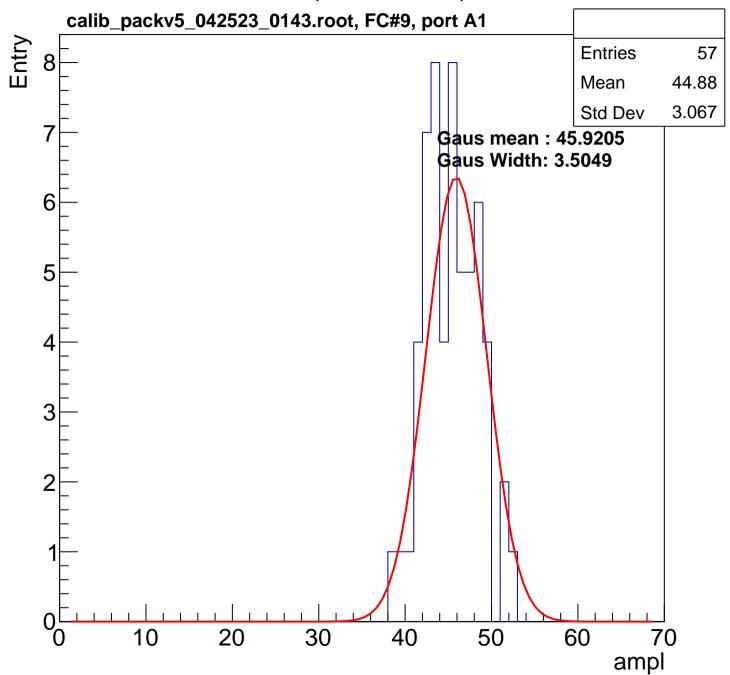


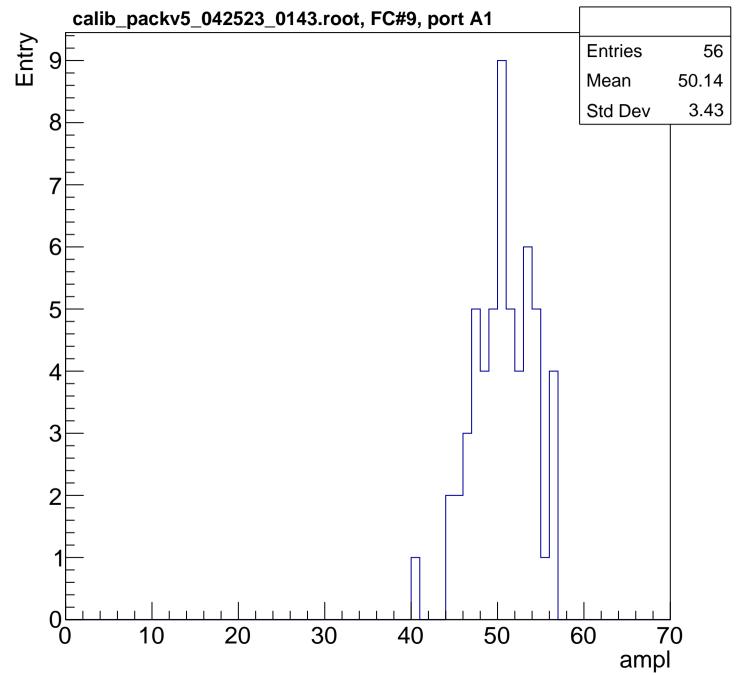


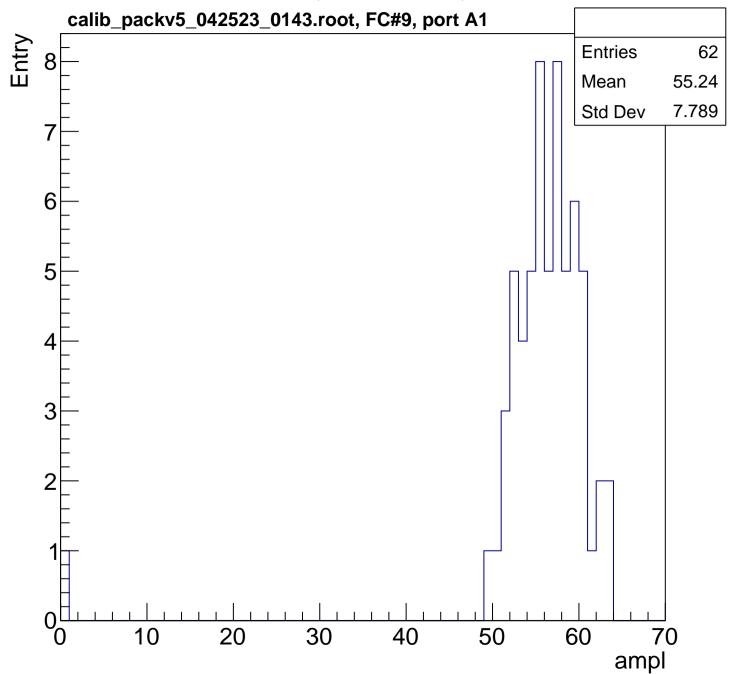
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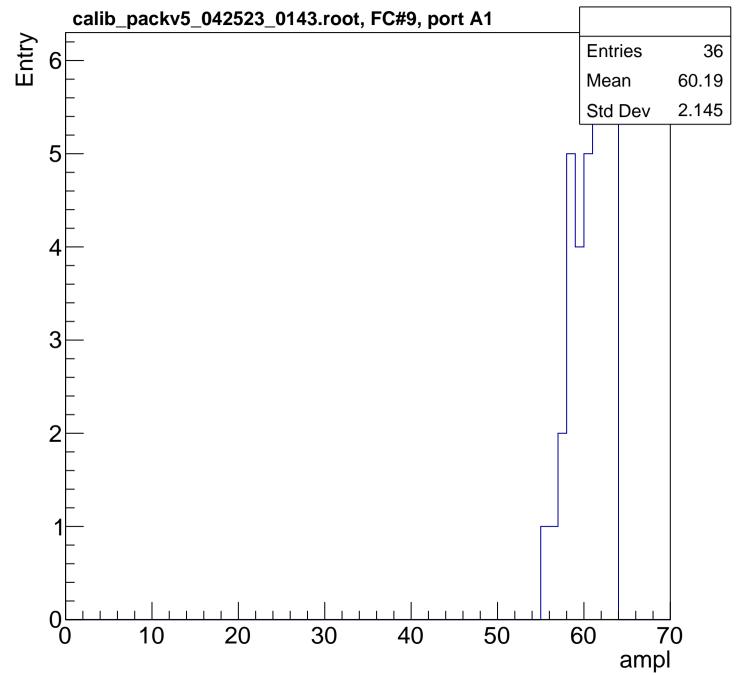


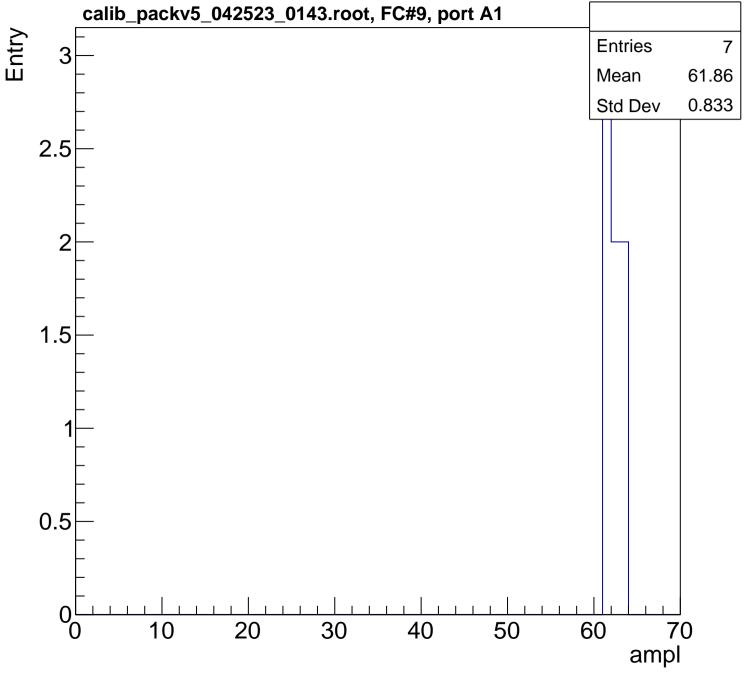


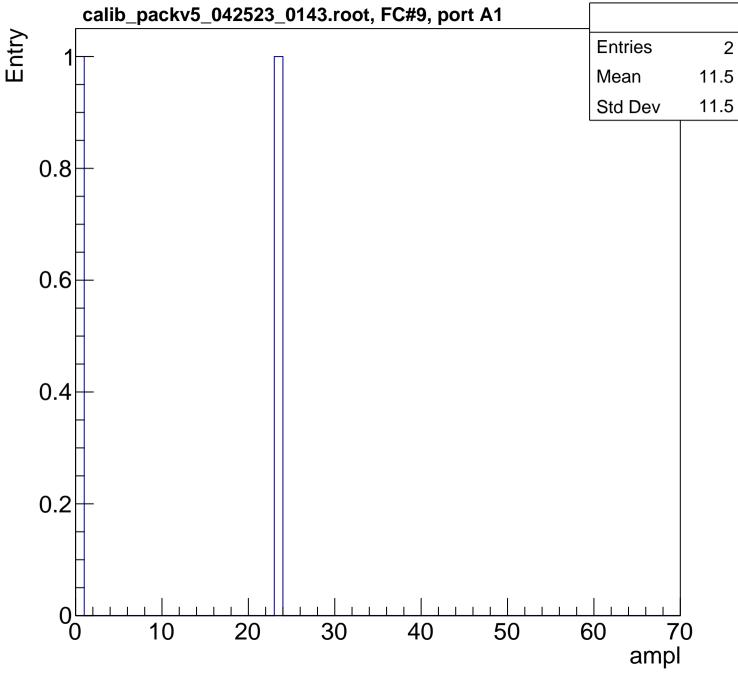


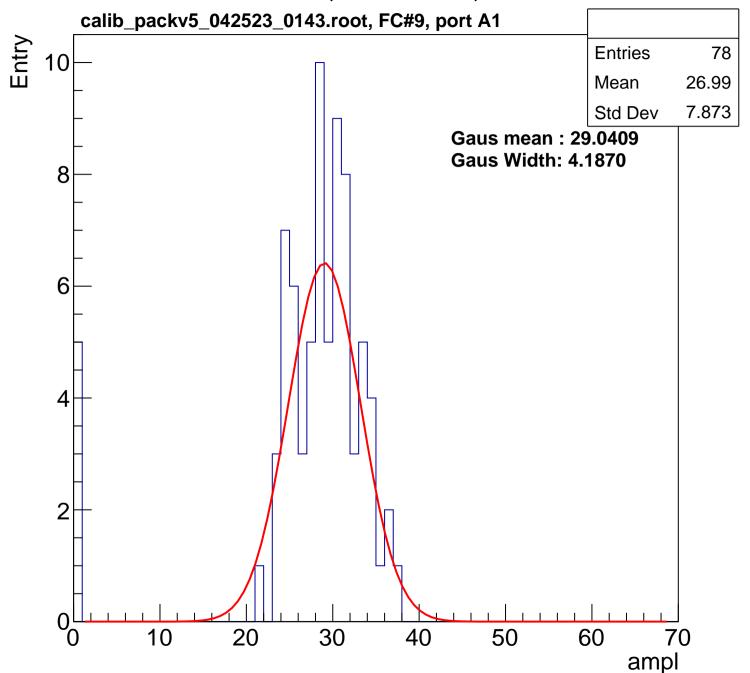


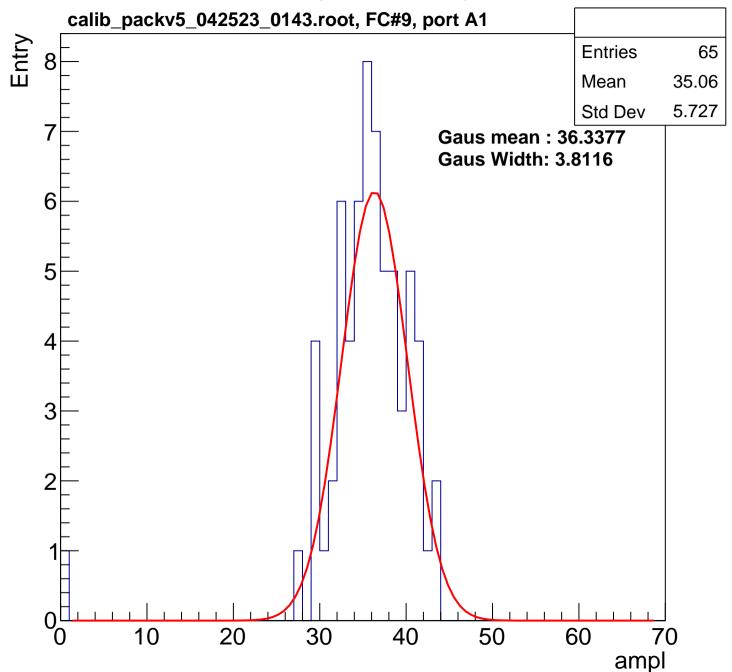


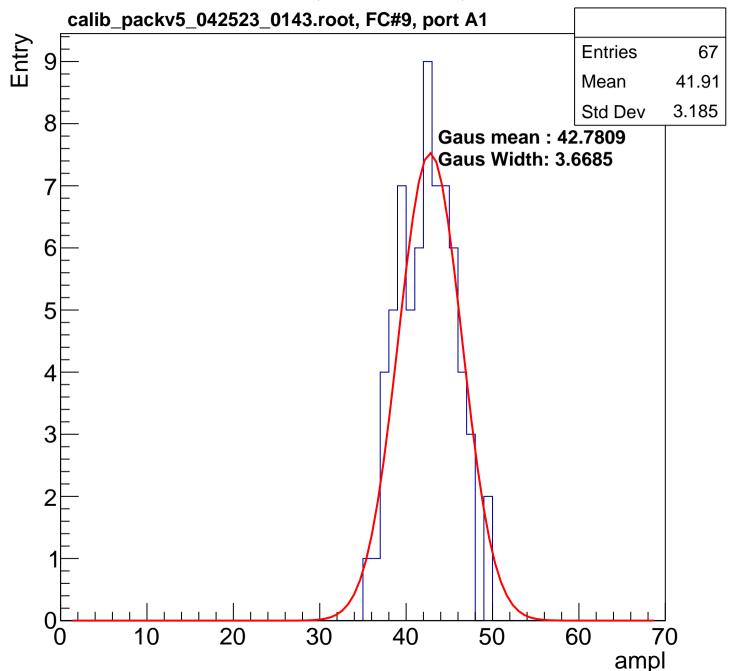


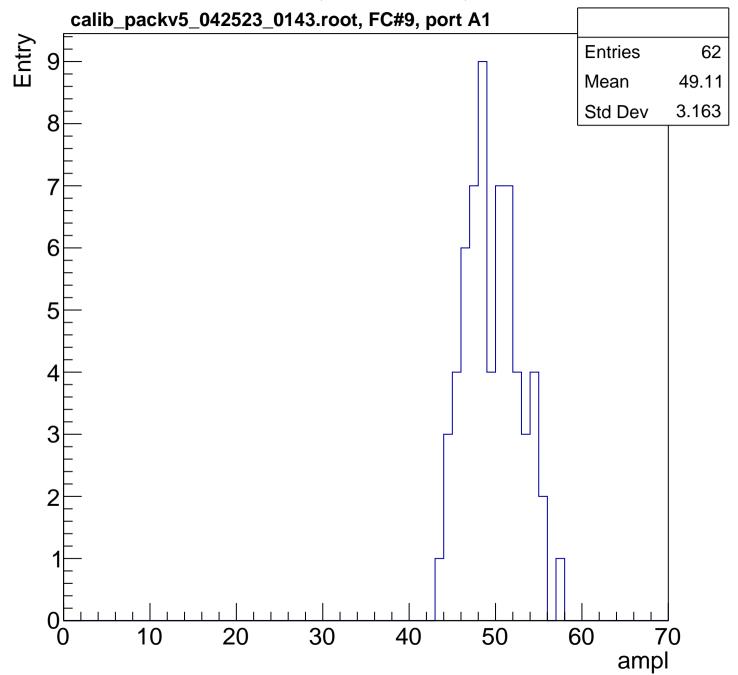


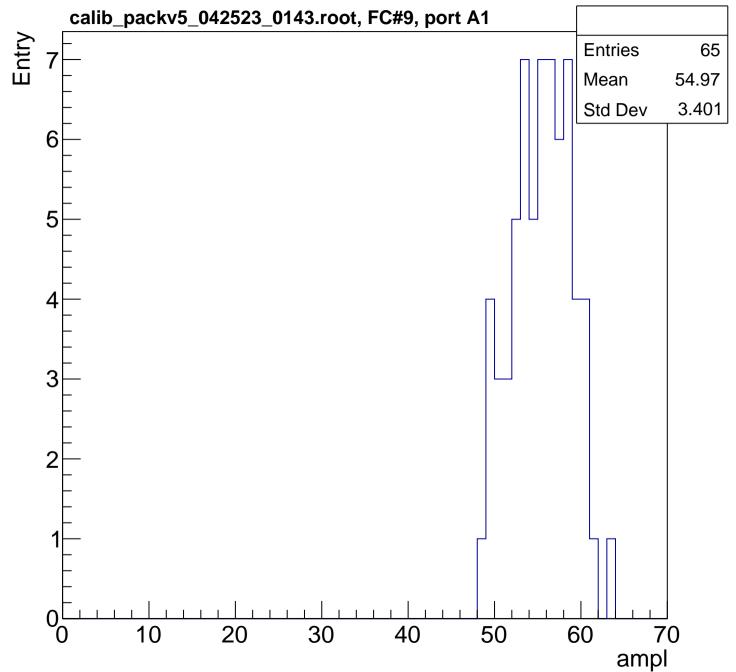


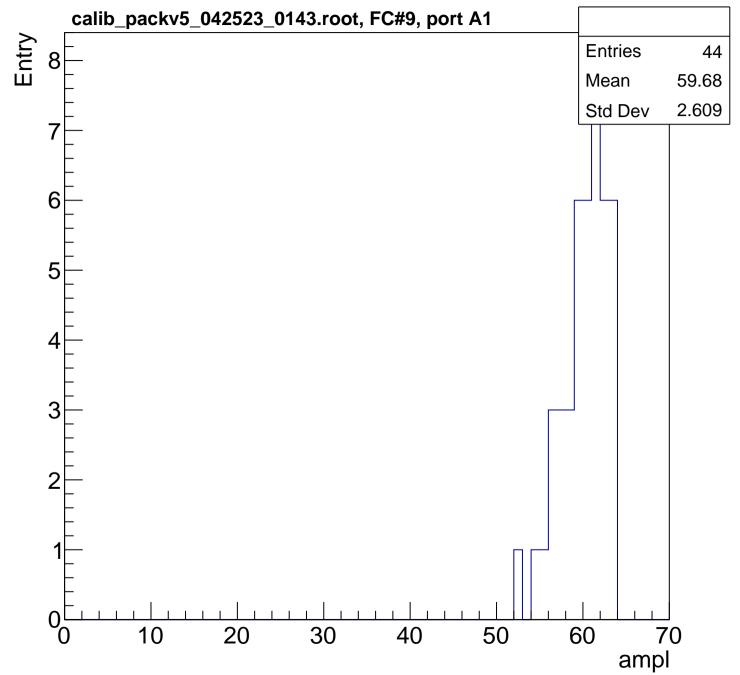


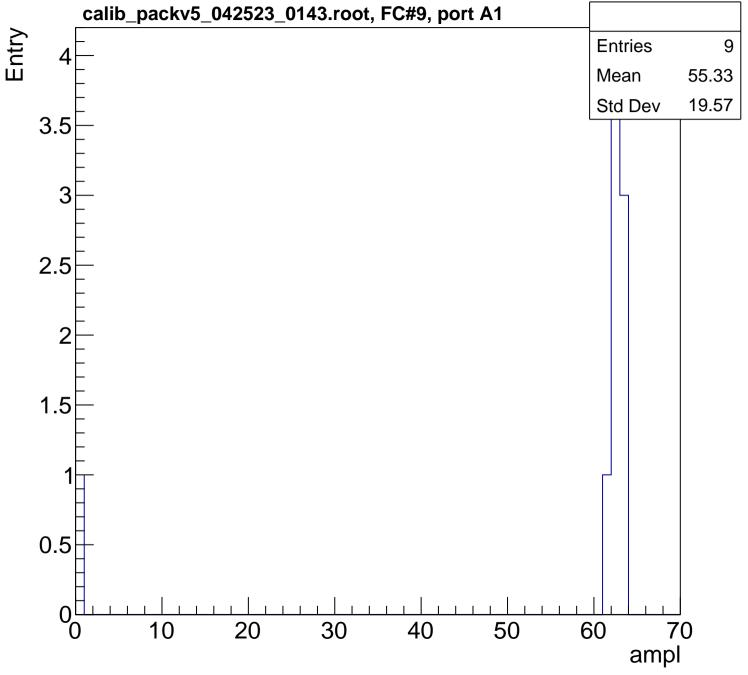




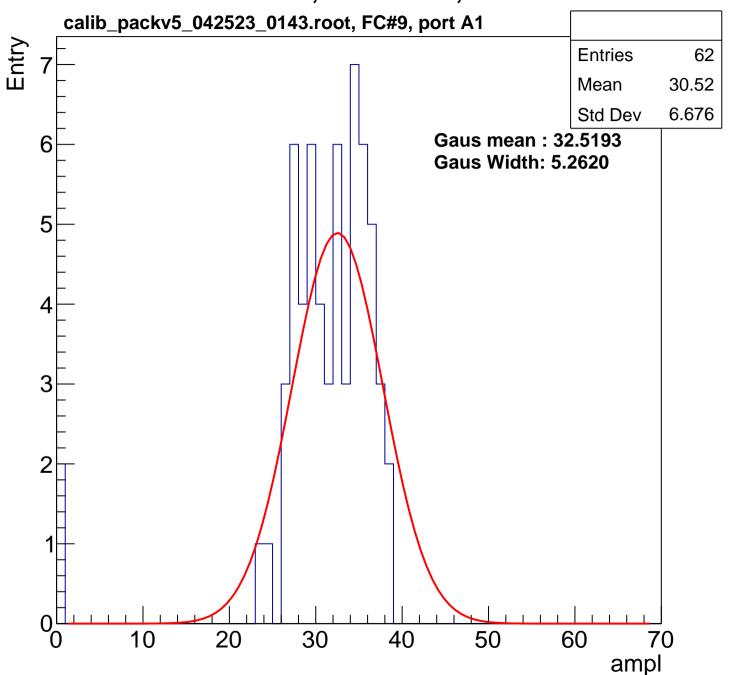


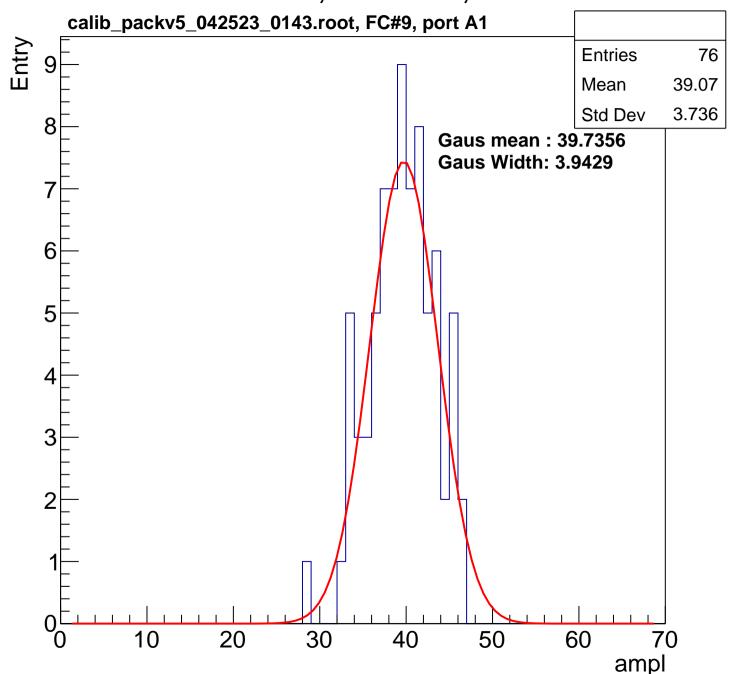


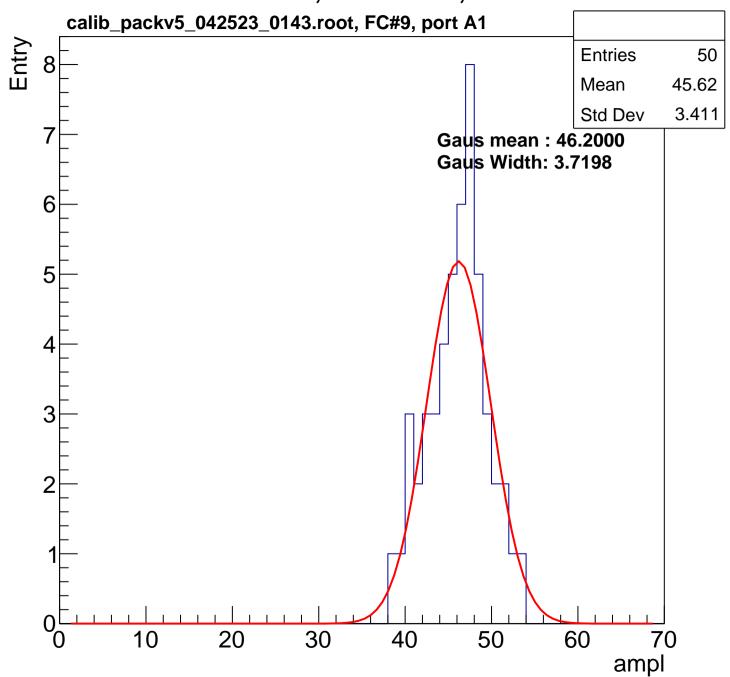


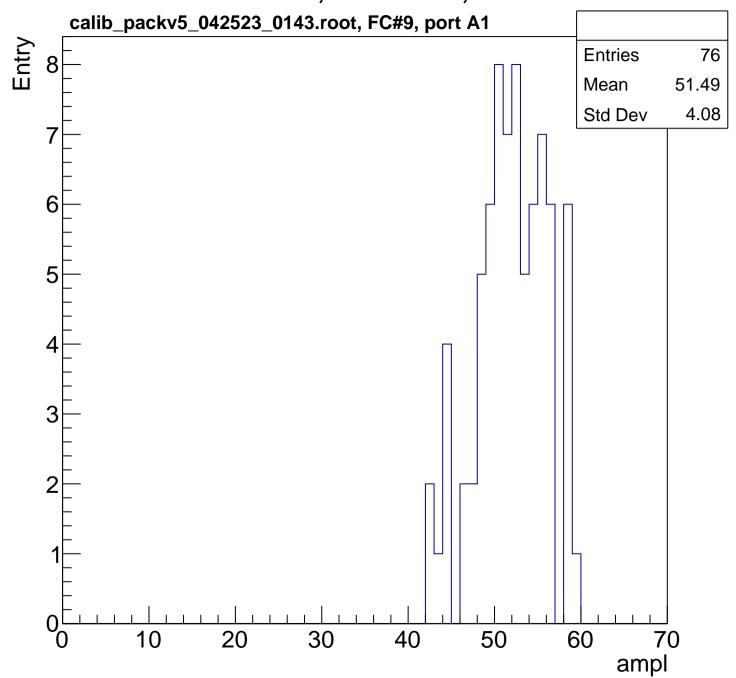


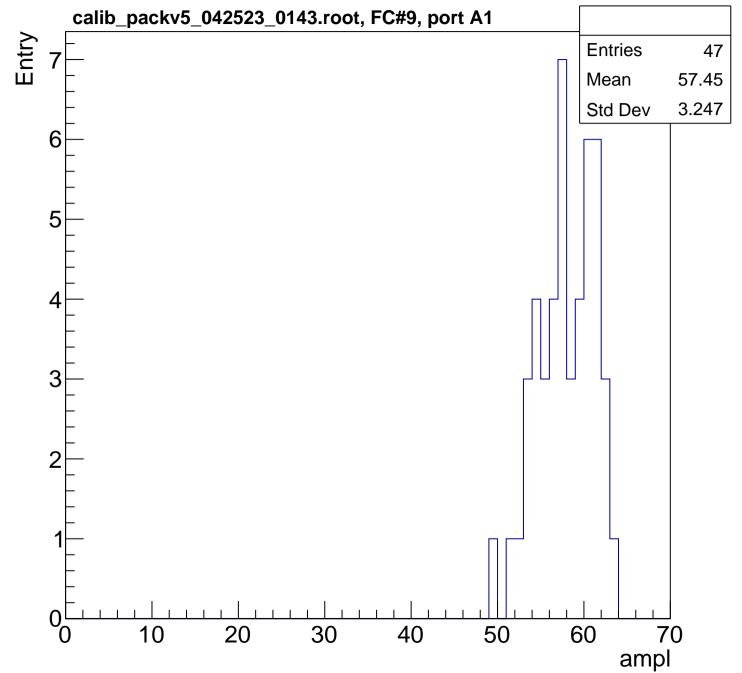


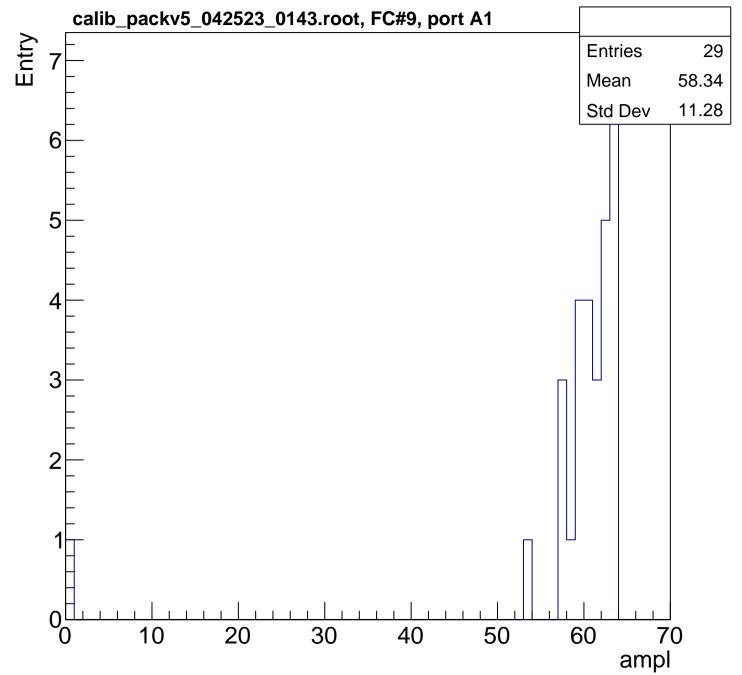


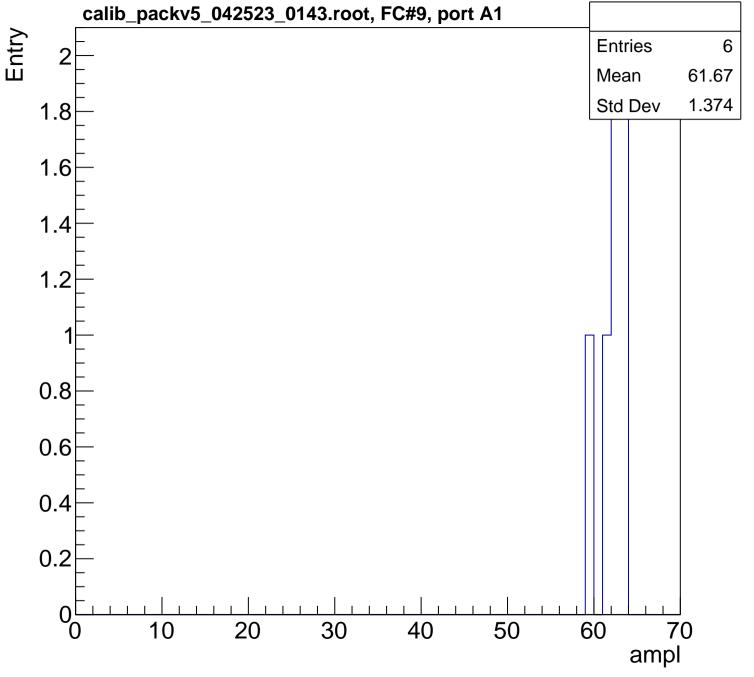


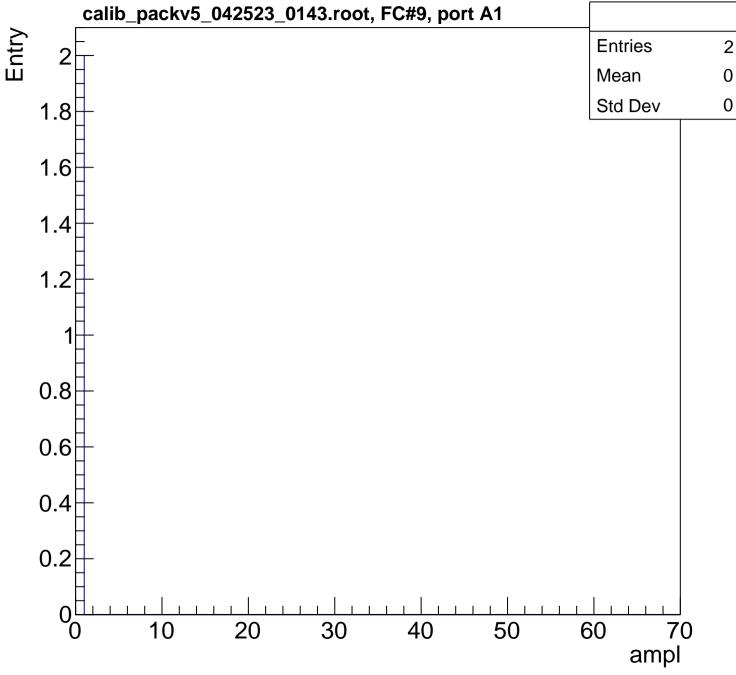


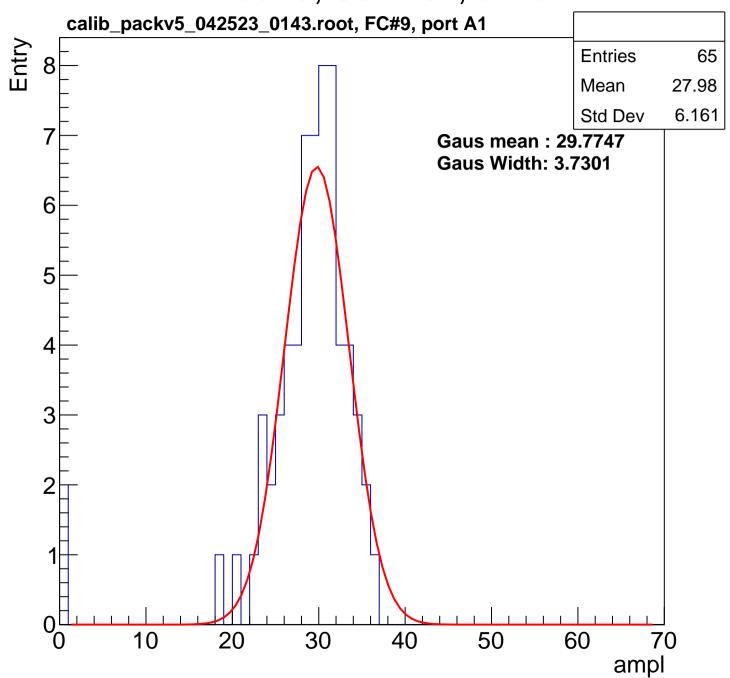


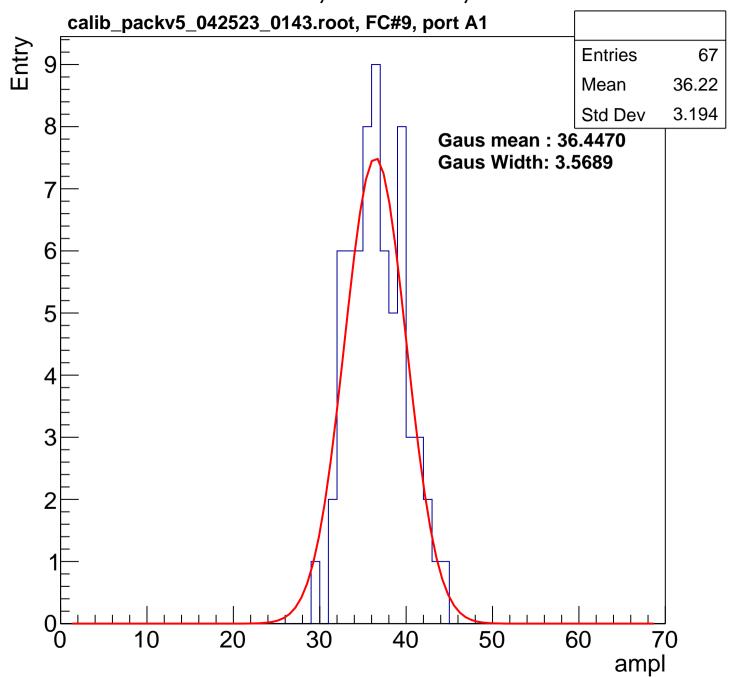


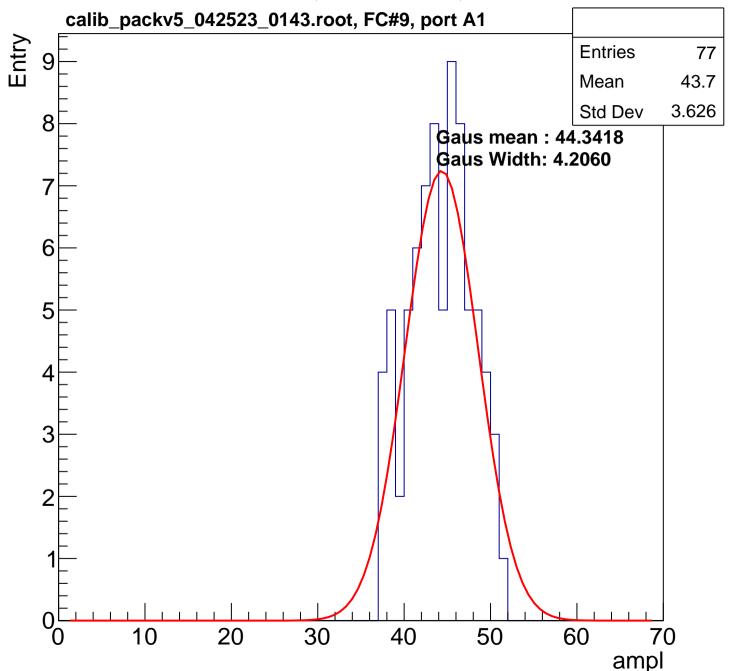


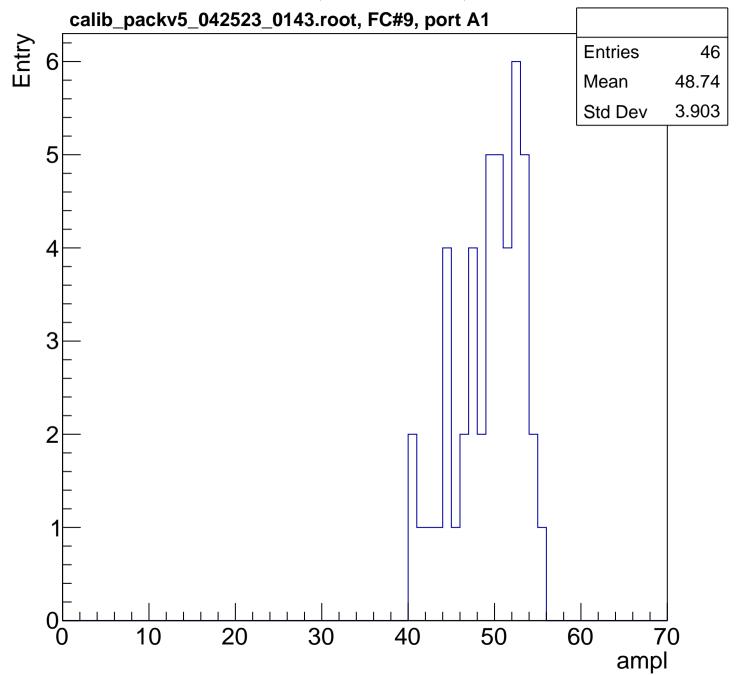


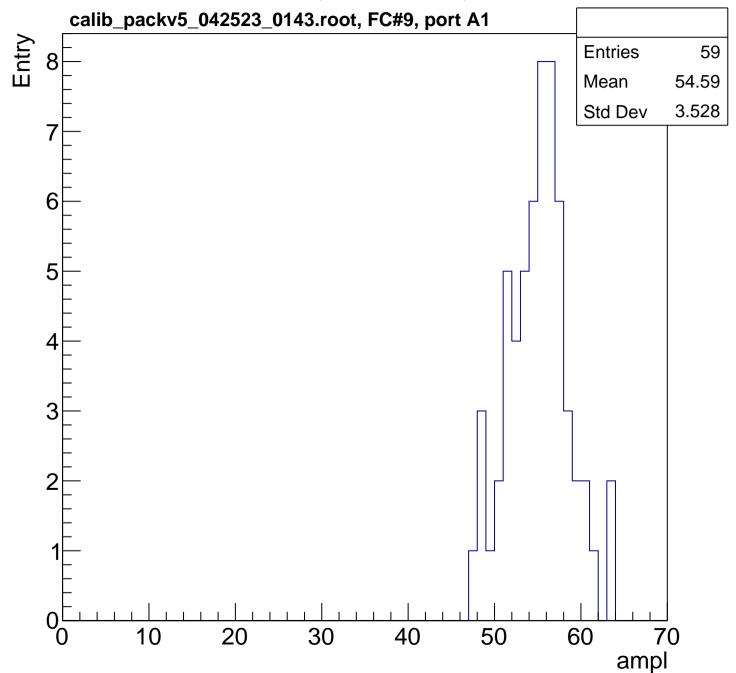


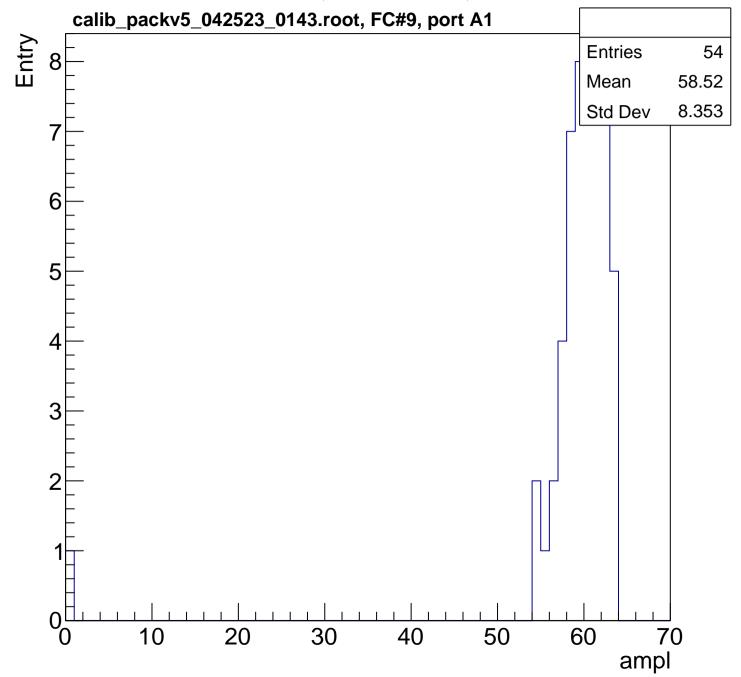


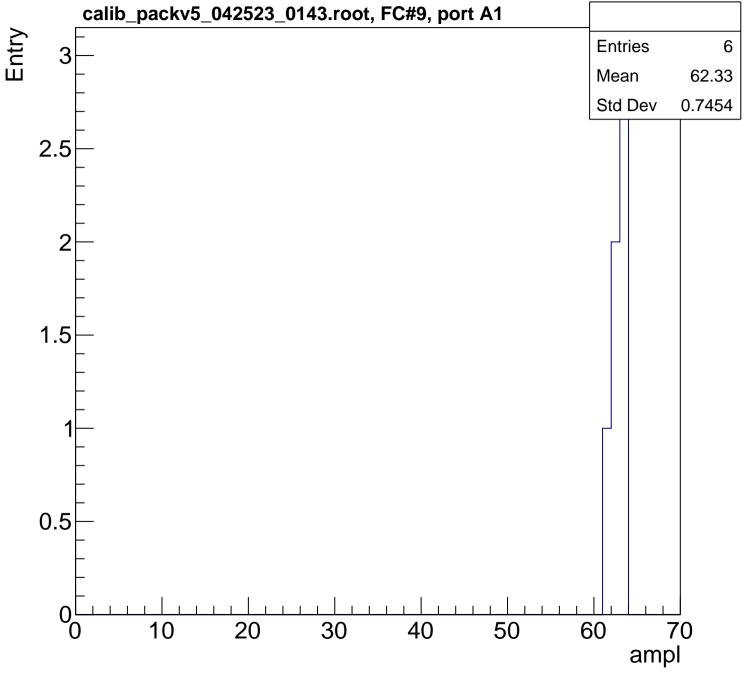






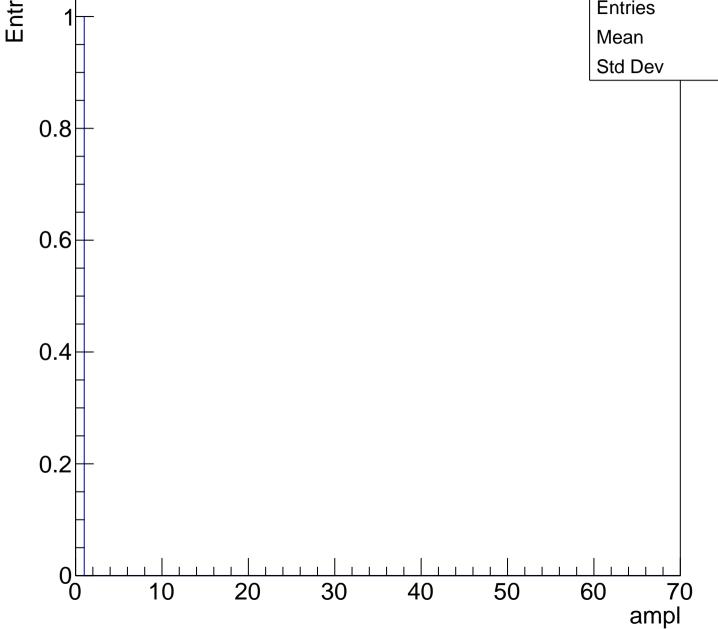


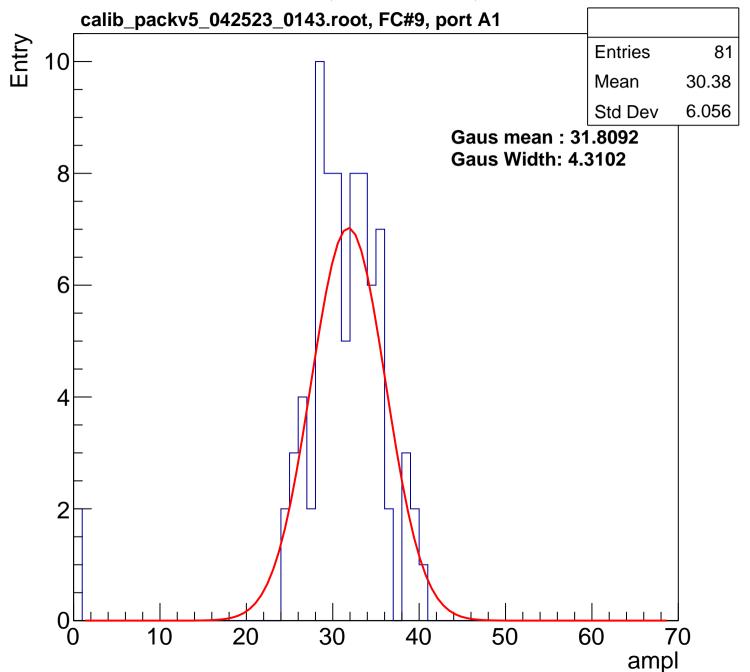


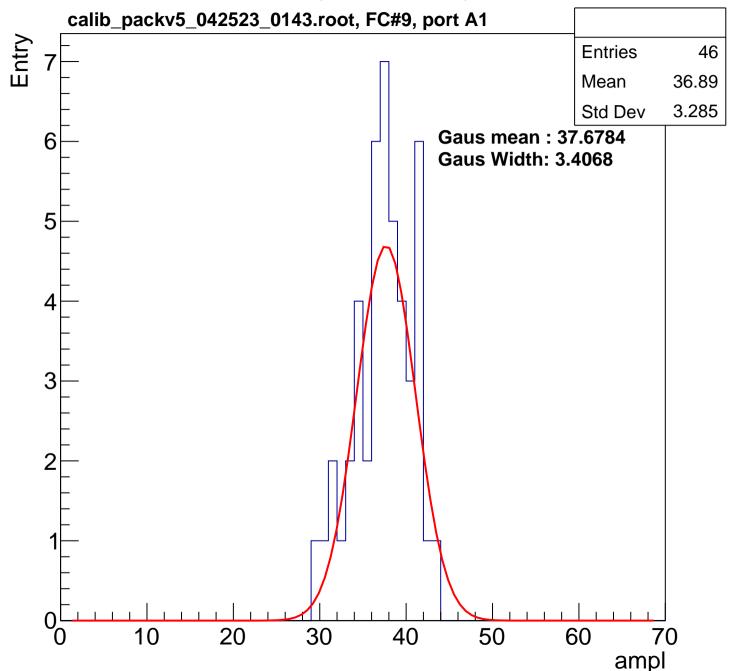


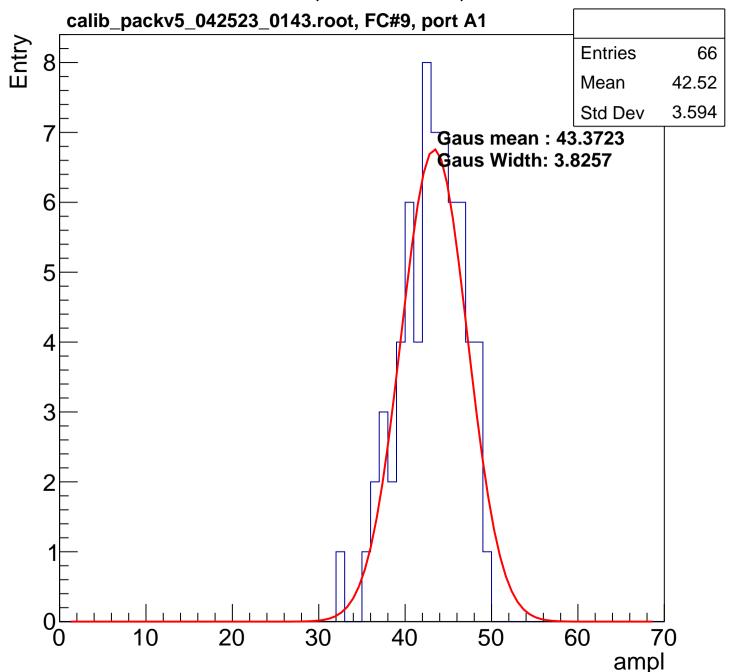
B0L001S, U3-ch84, adc7 calib_packv5_042523_0143.root, FC#9, port A1 Entry **Entries** Mean 0 Std Dev 0 8.0 0.6 0.4

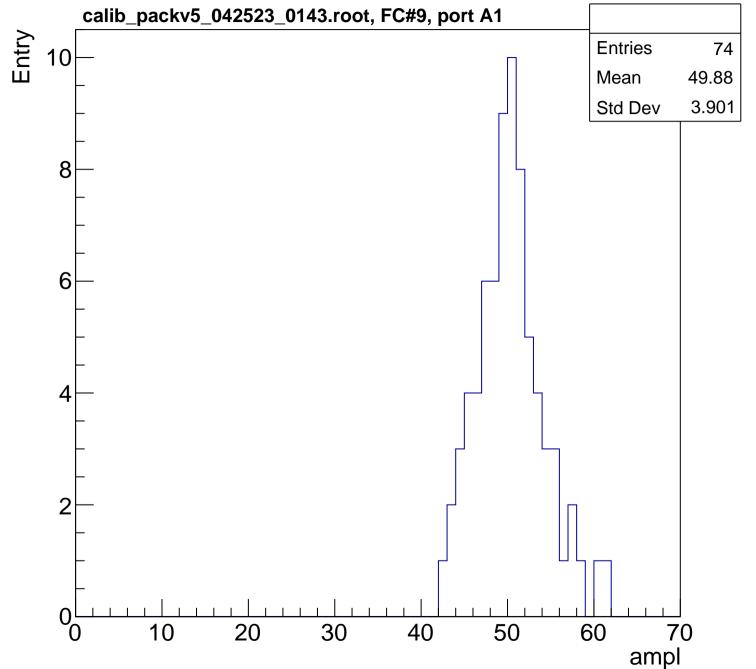
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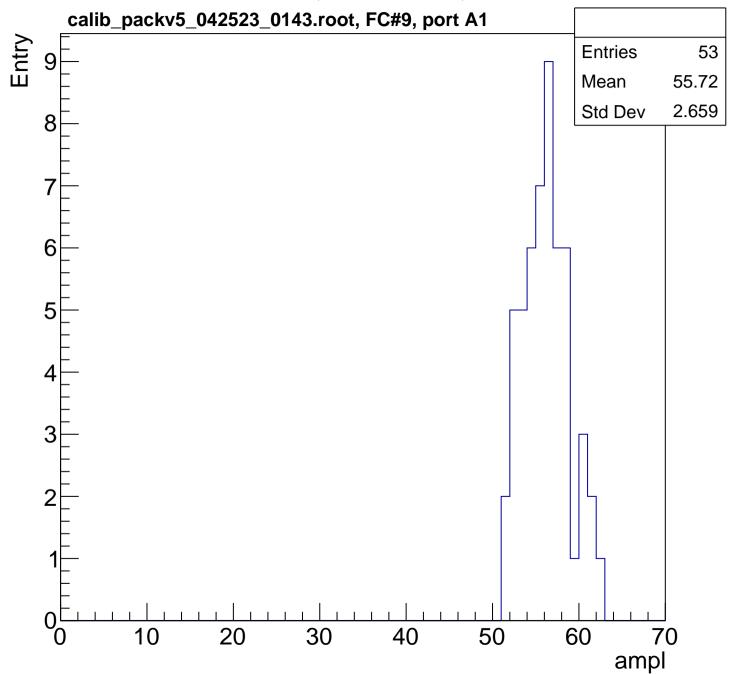


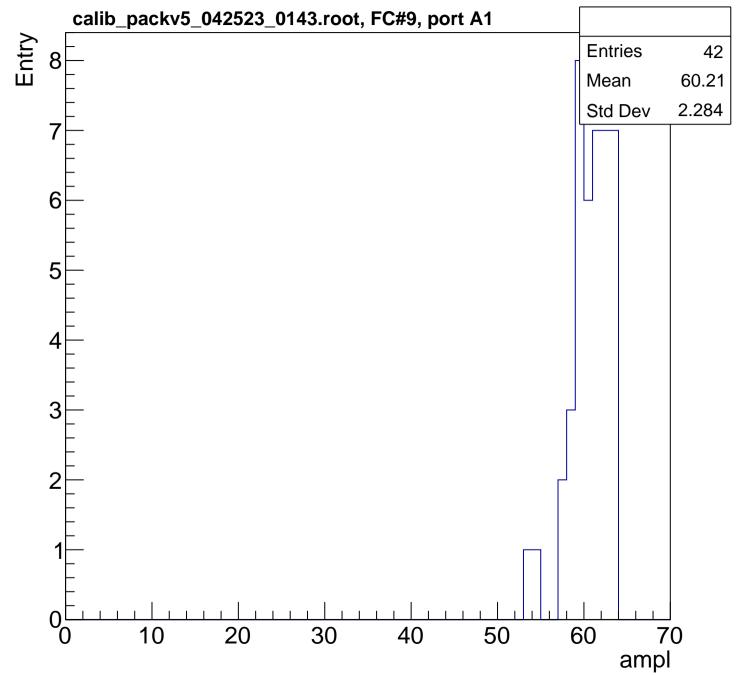


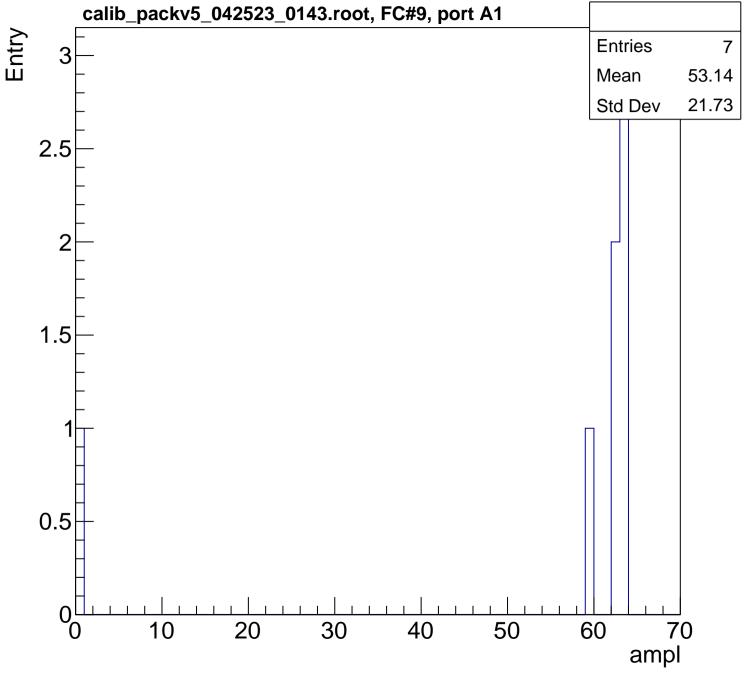


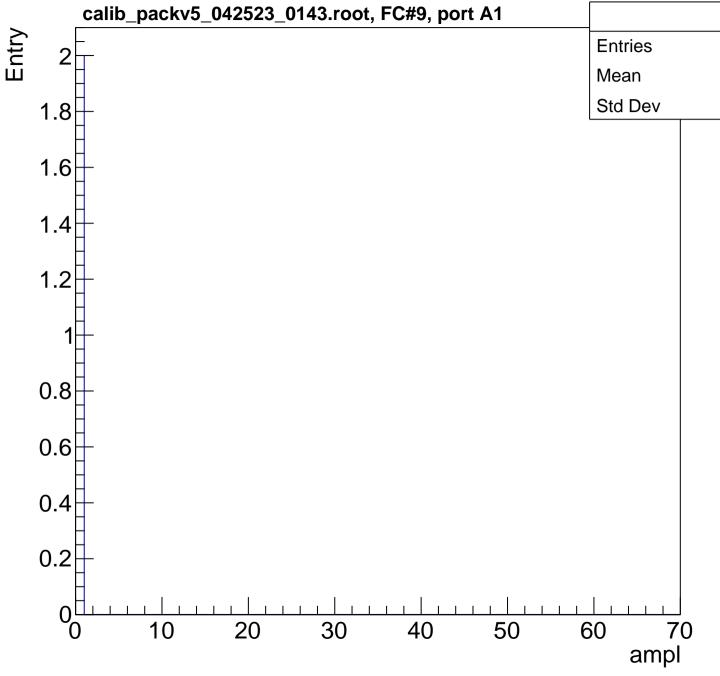


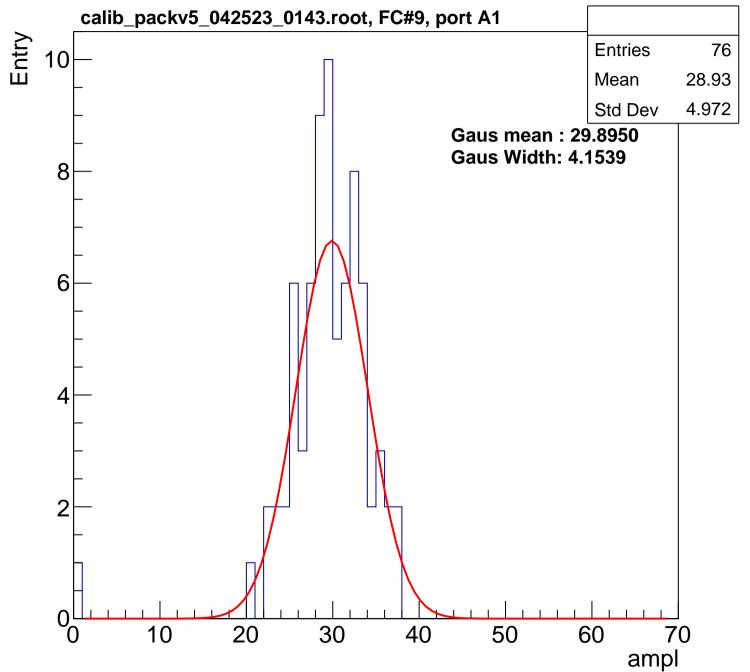


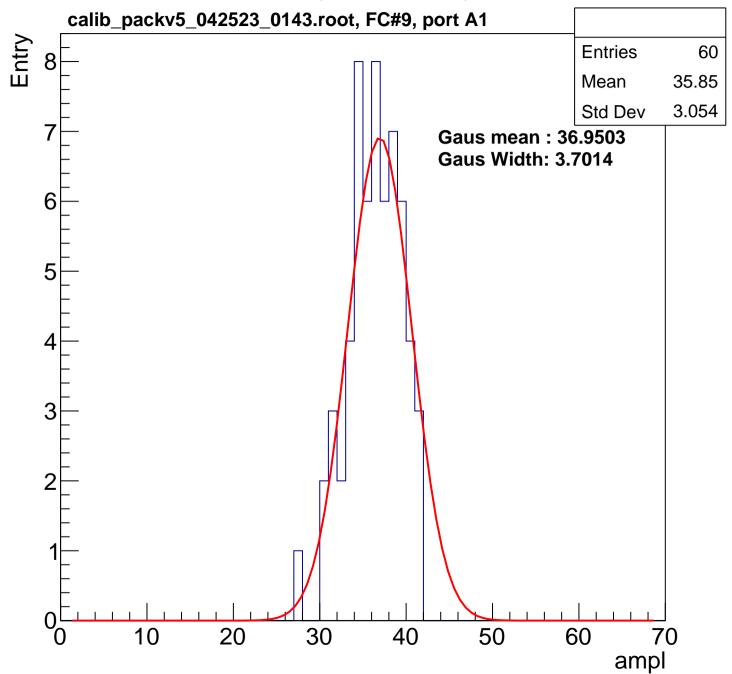


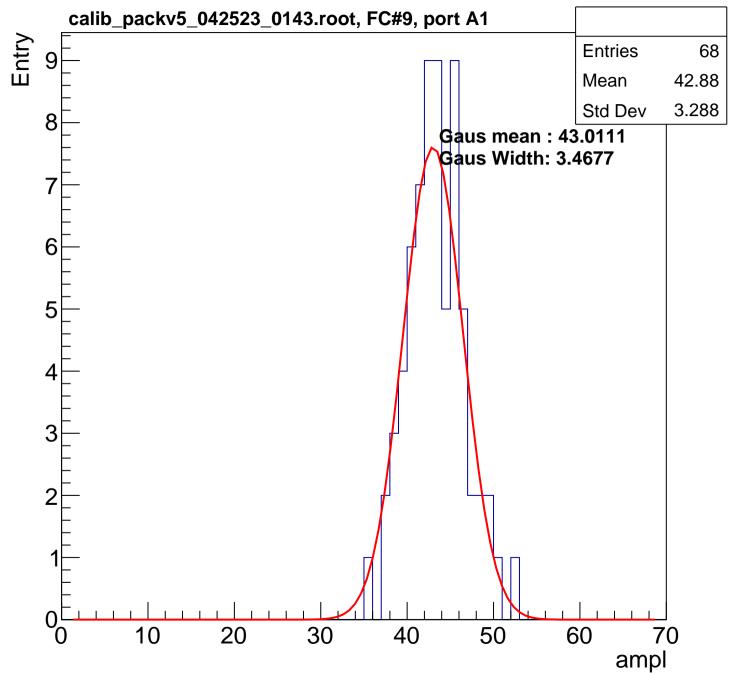


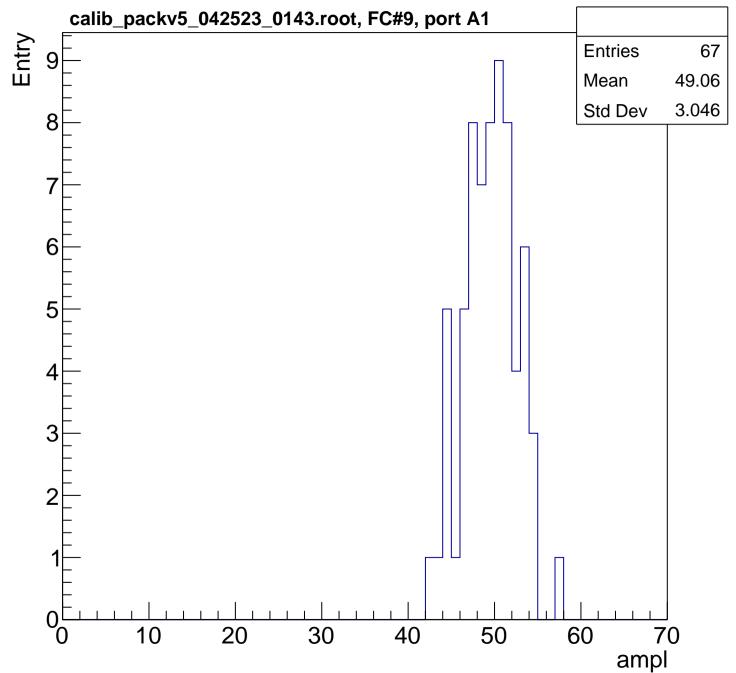


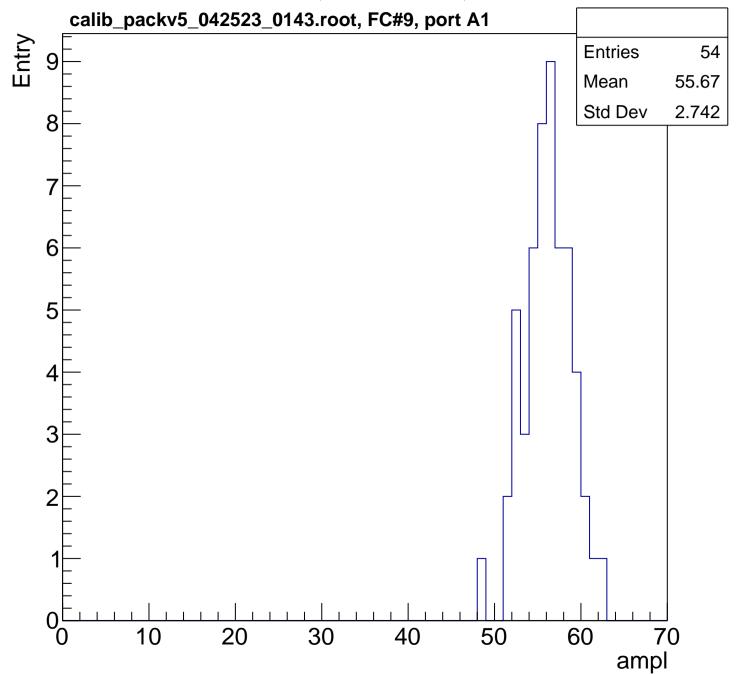


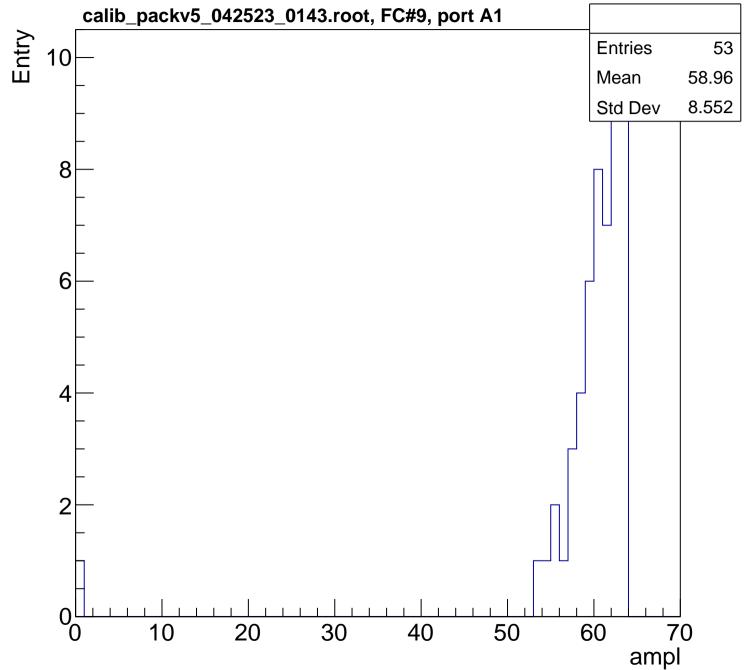


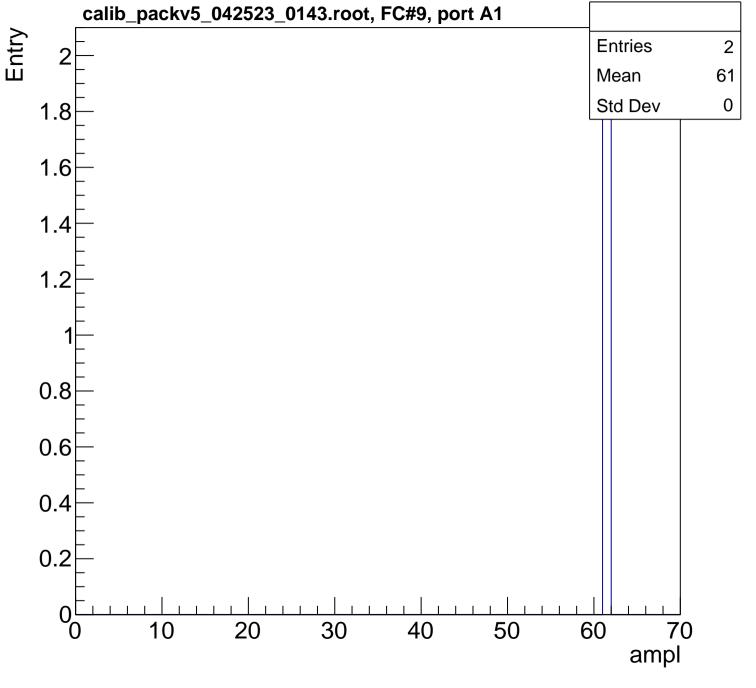


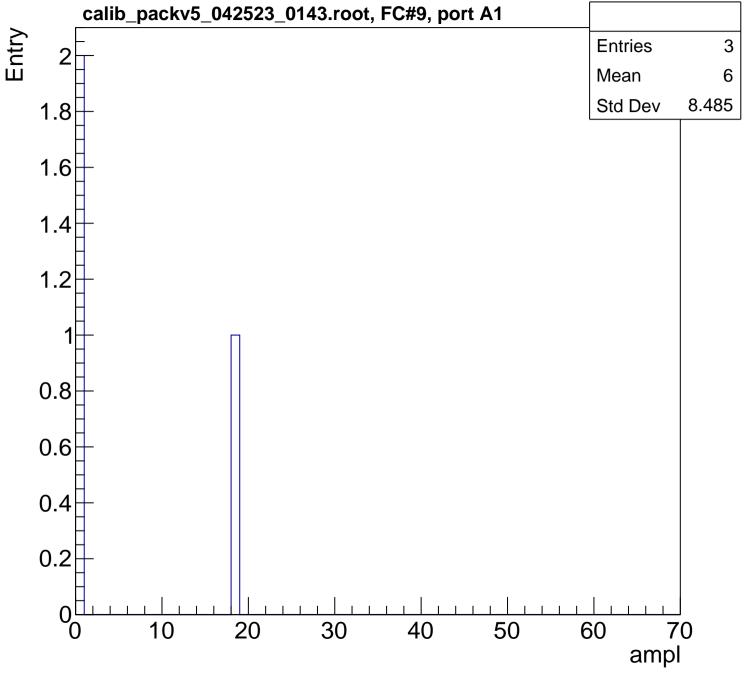


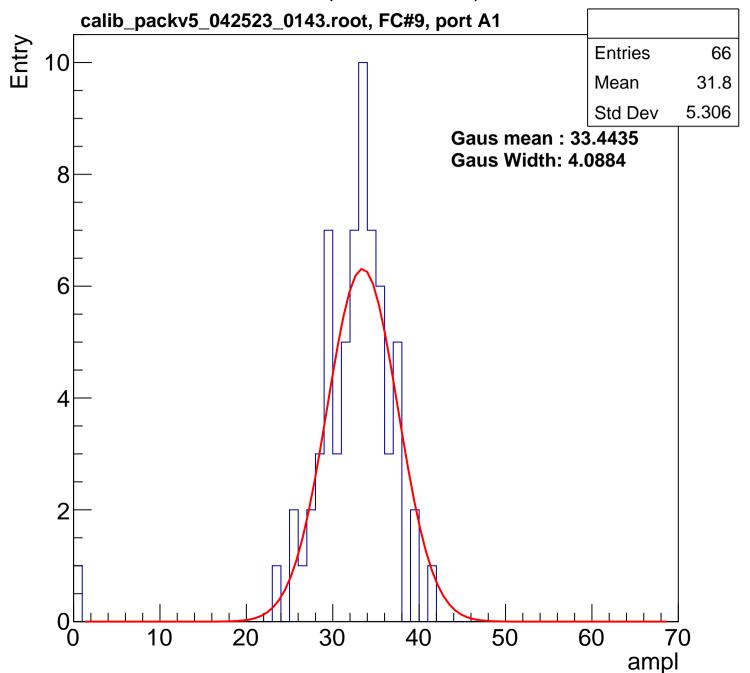


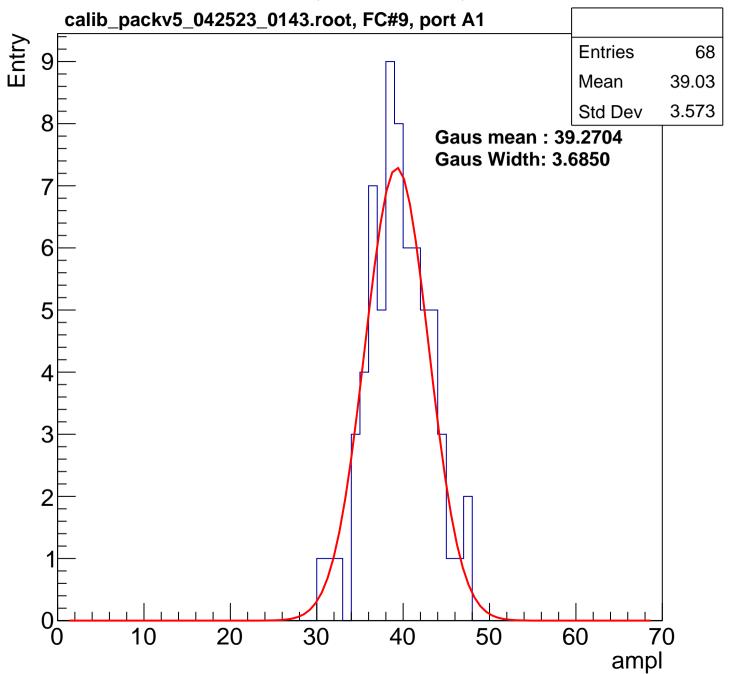


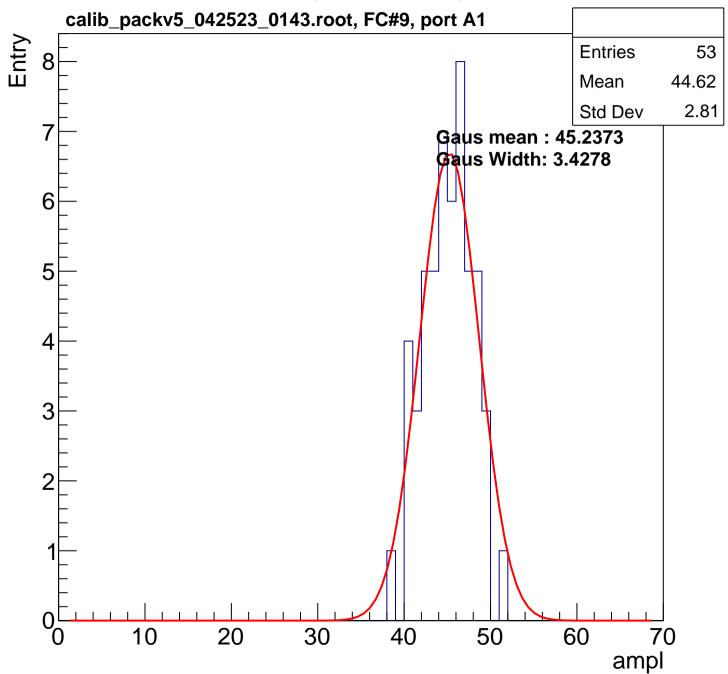


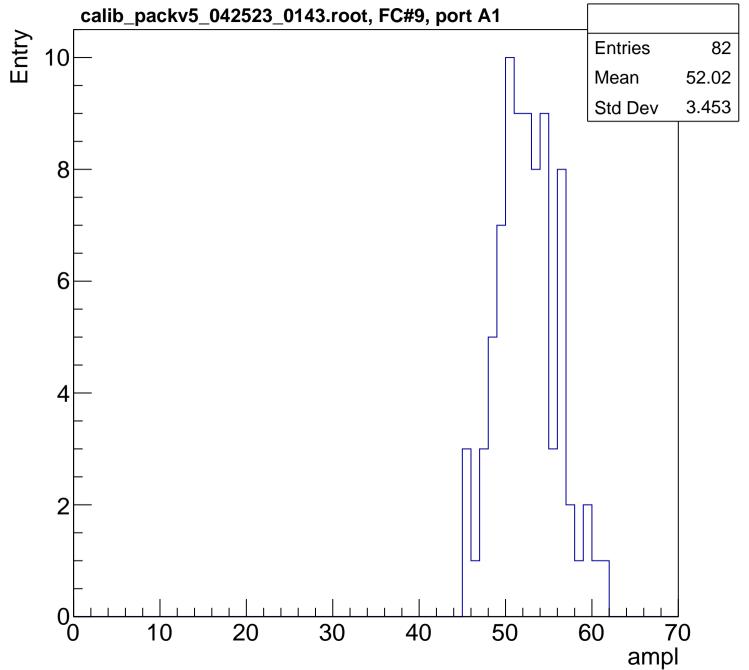


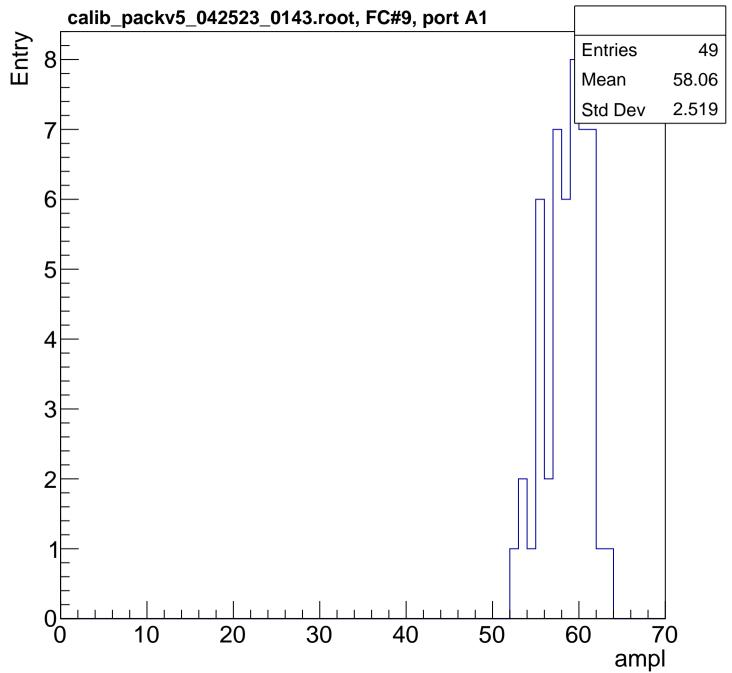


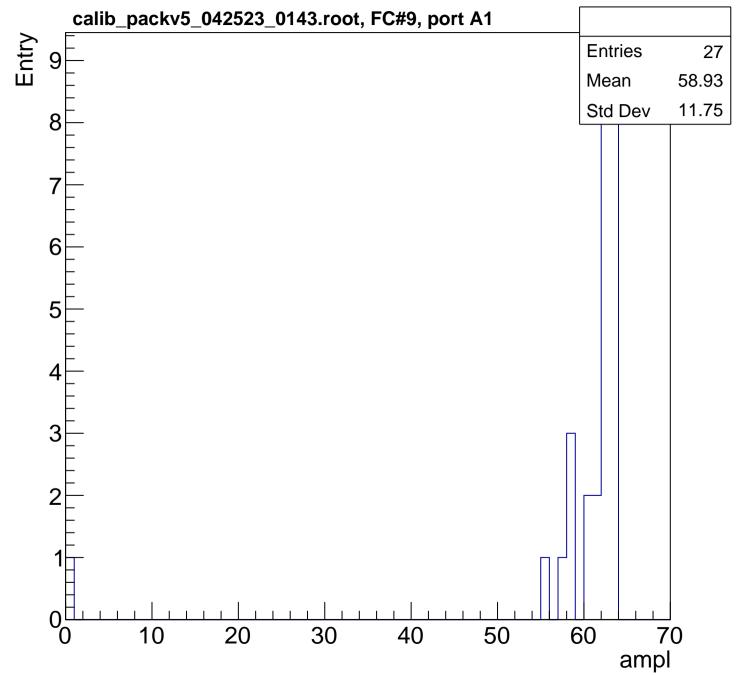




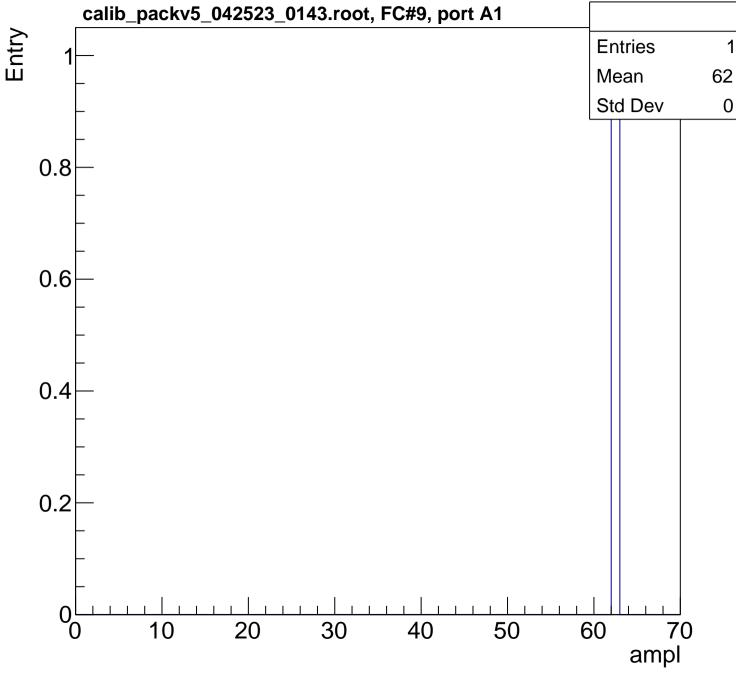


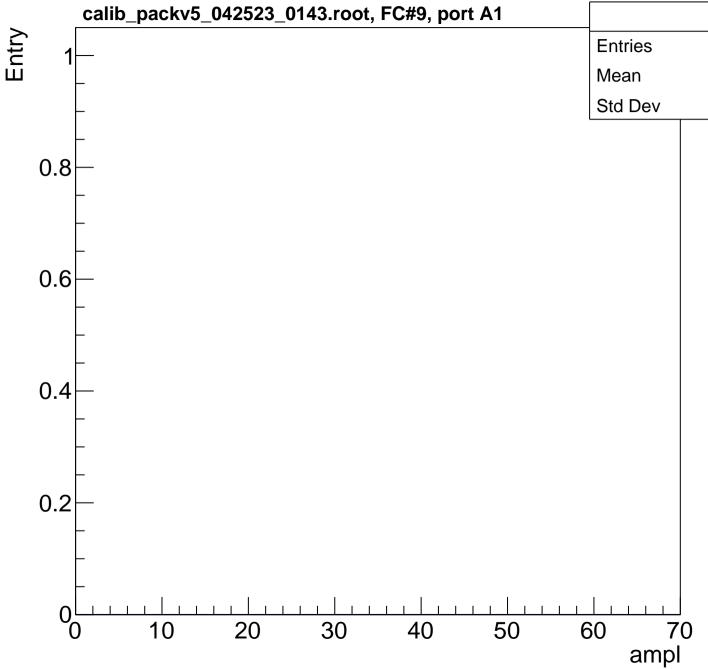


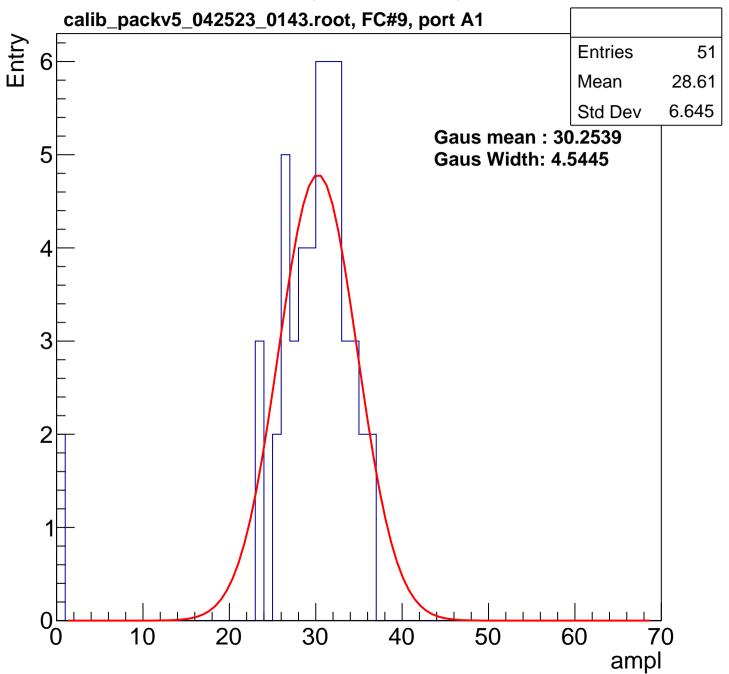


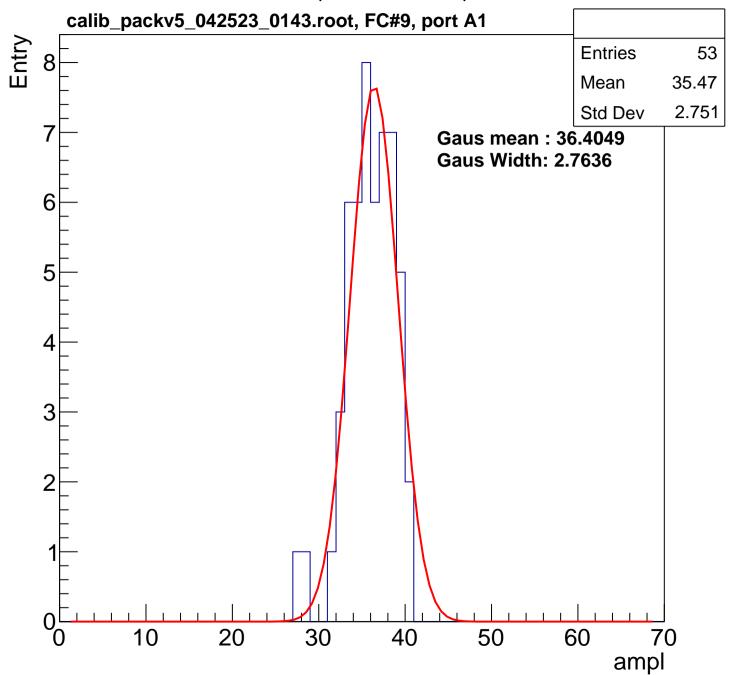


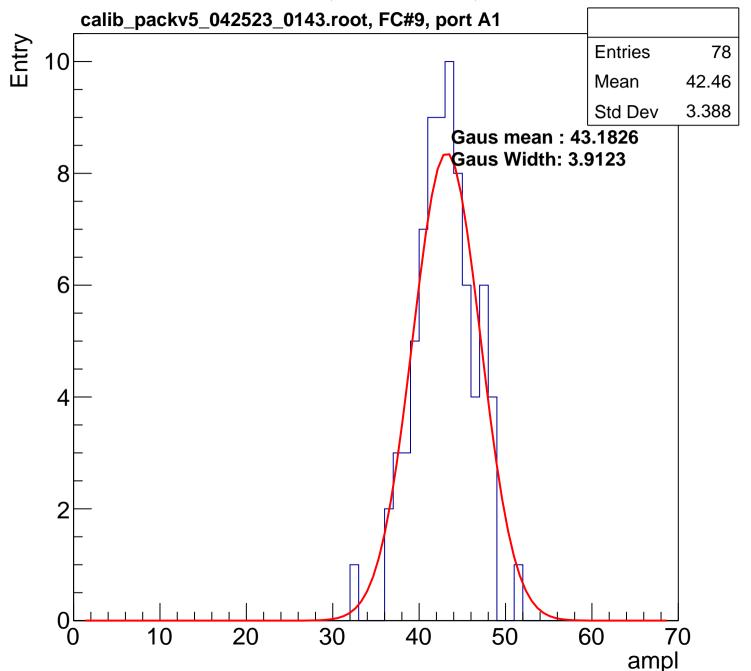
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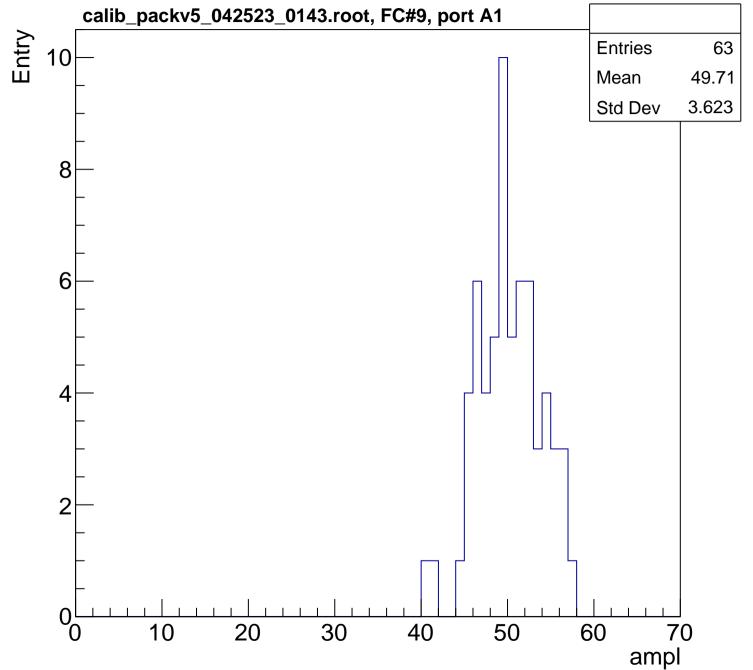


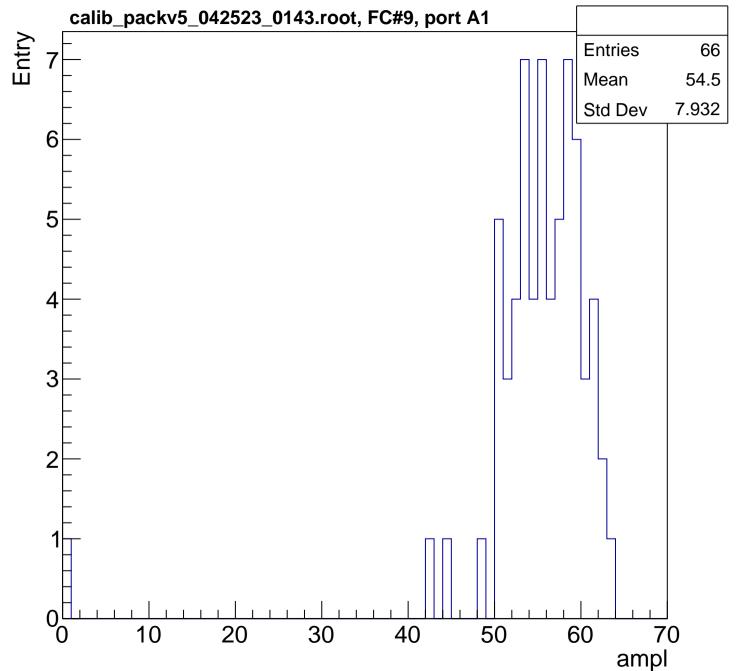


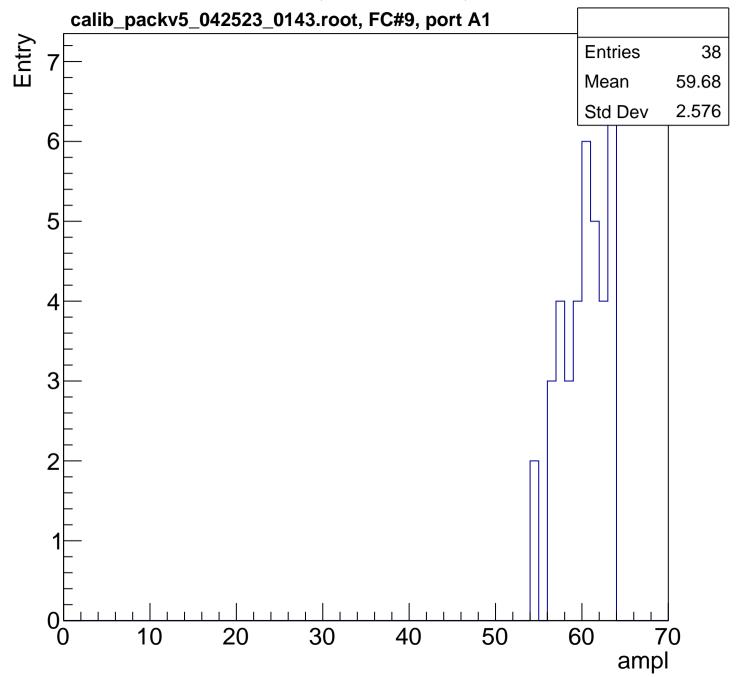


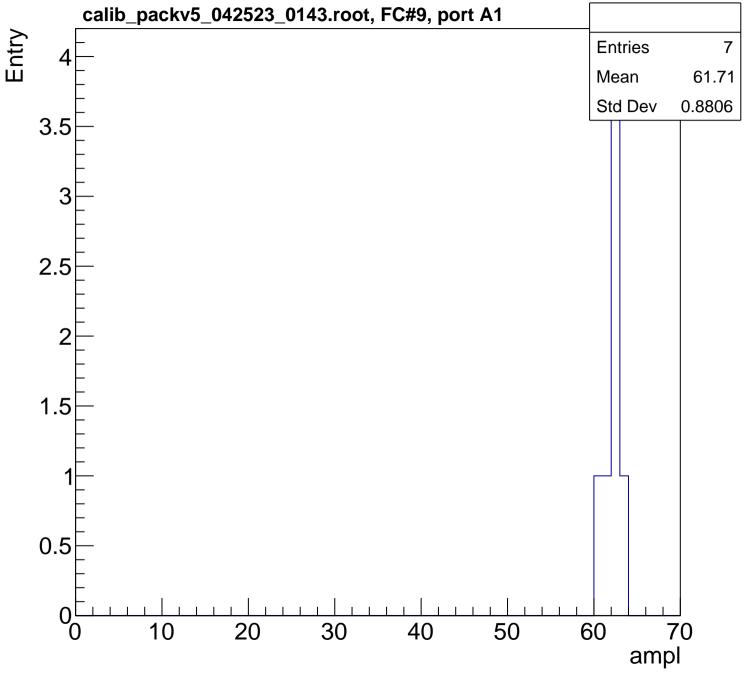




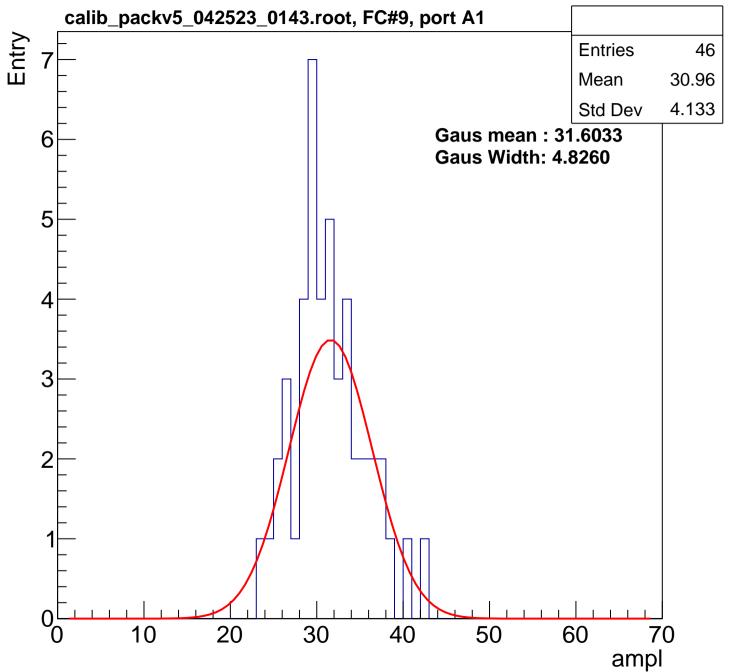


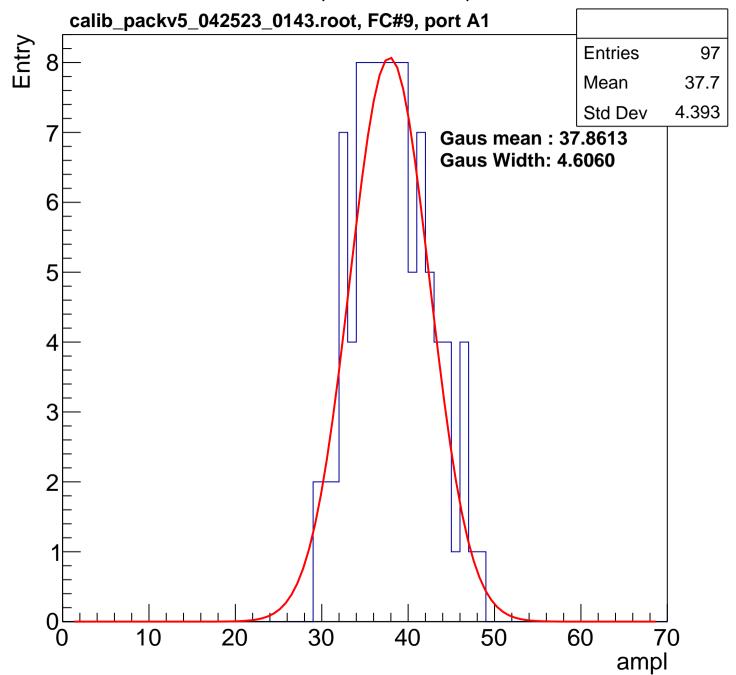


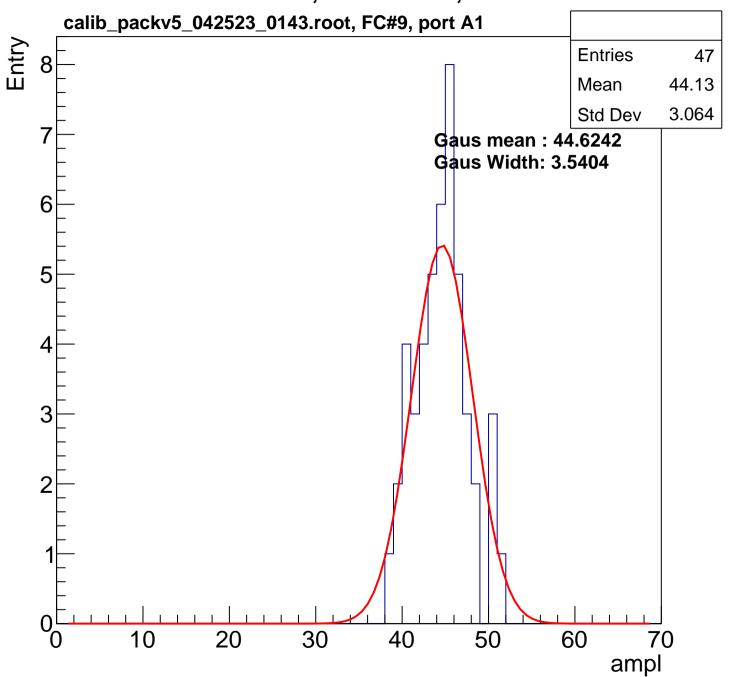


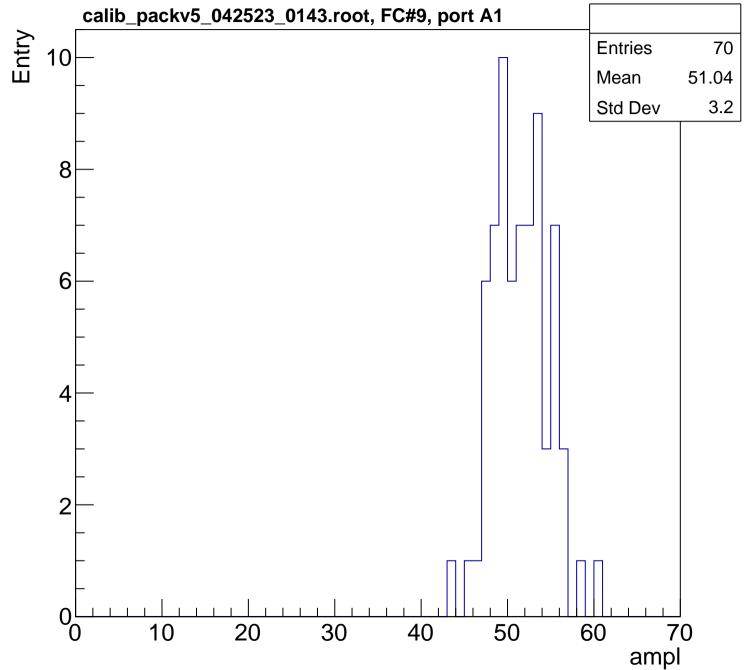


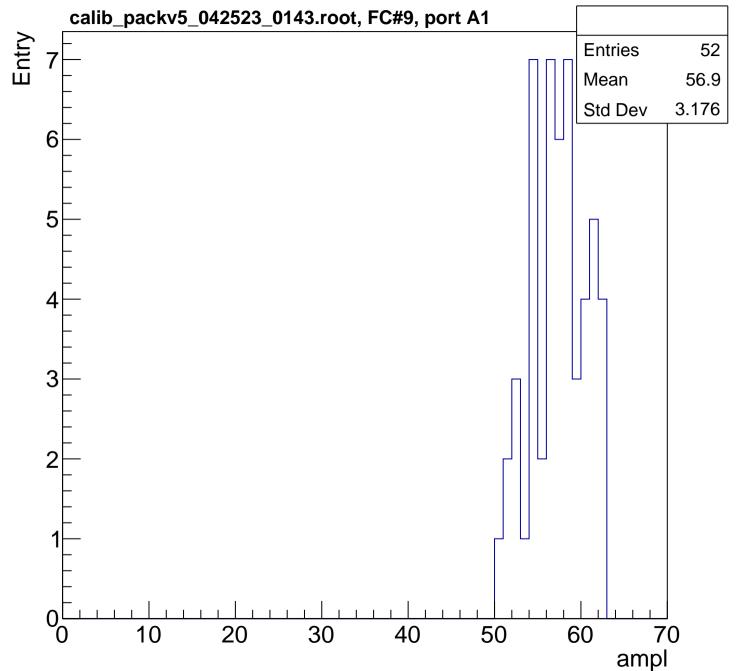


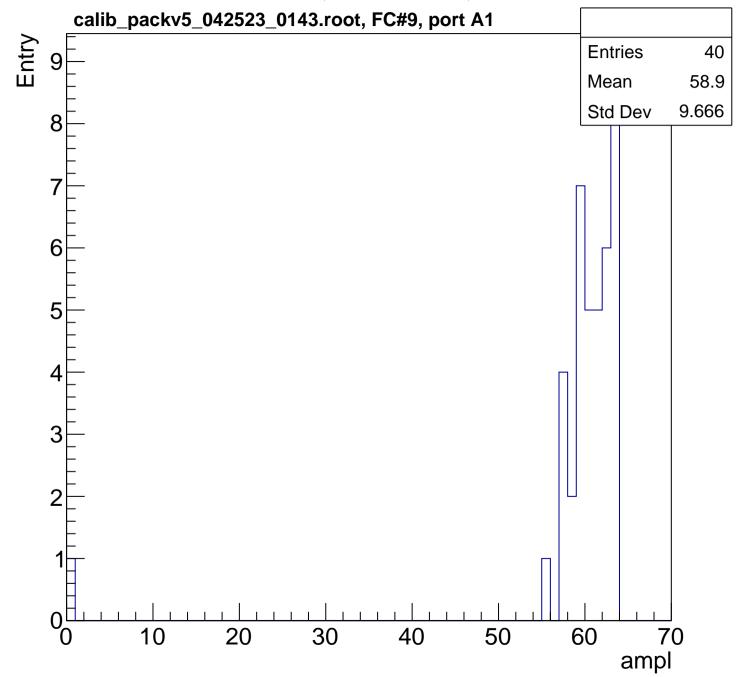


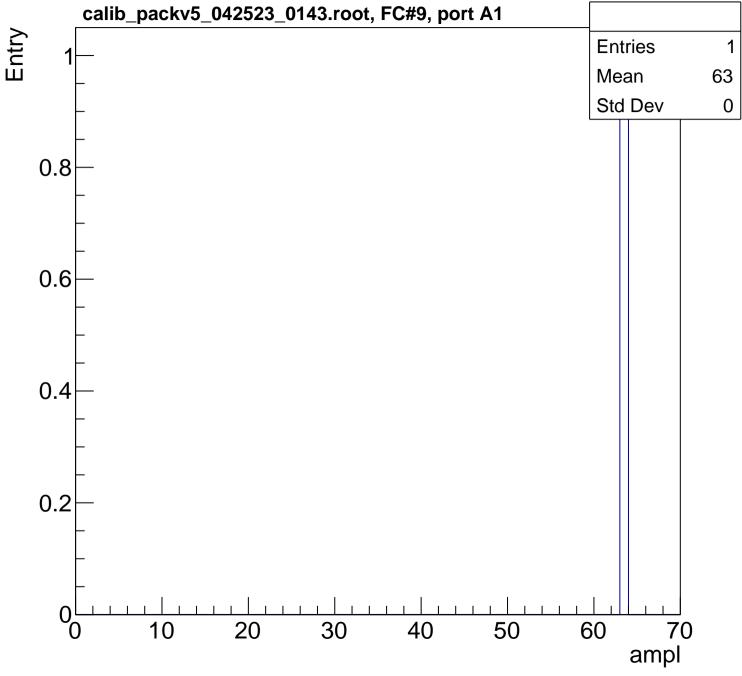


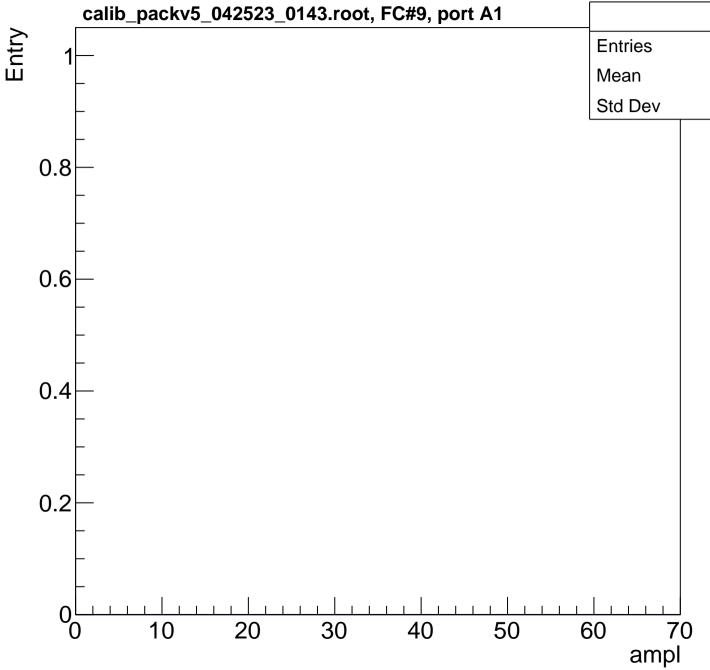


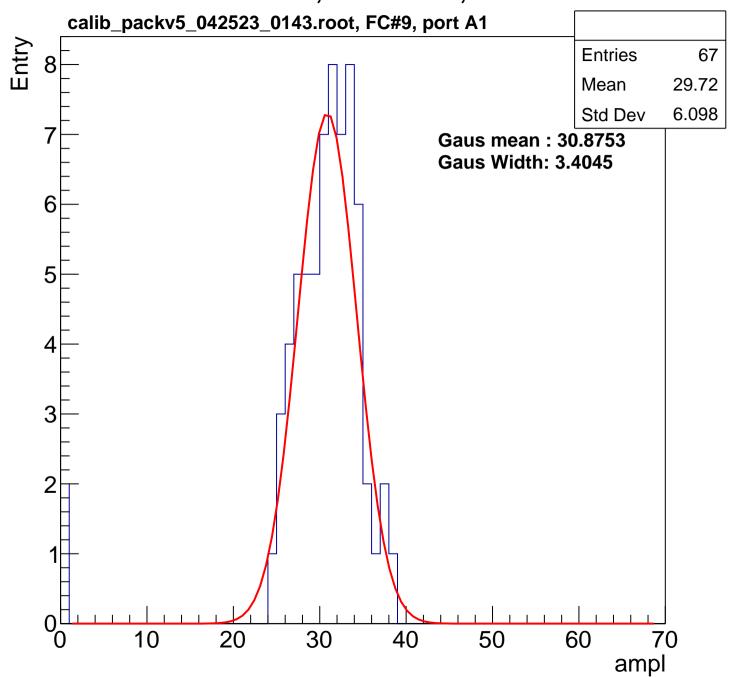


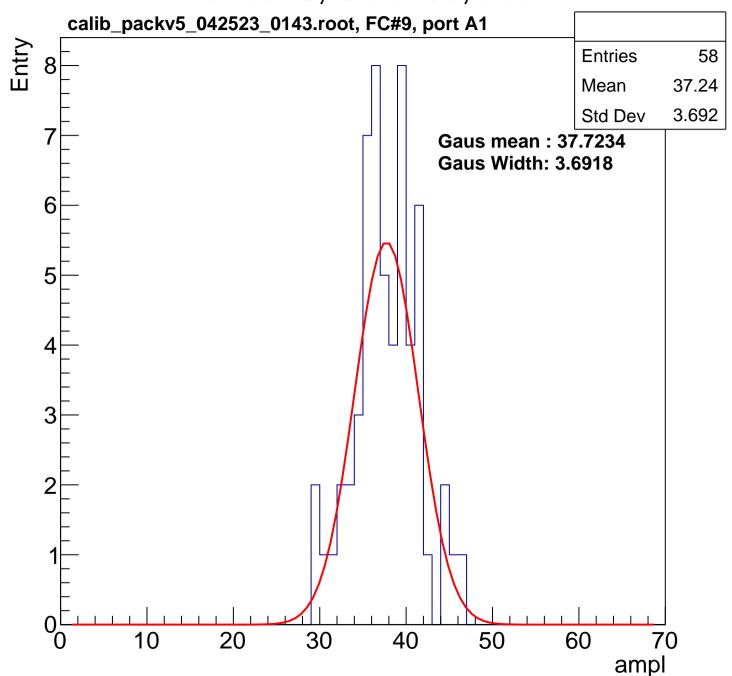


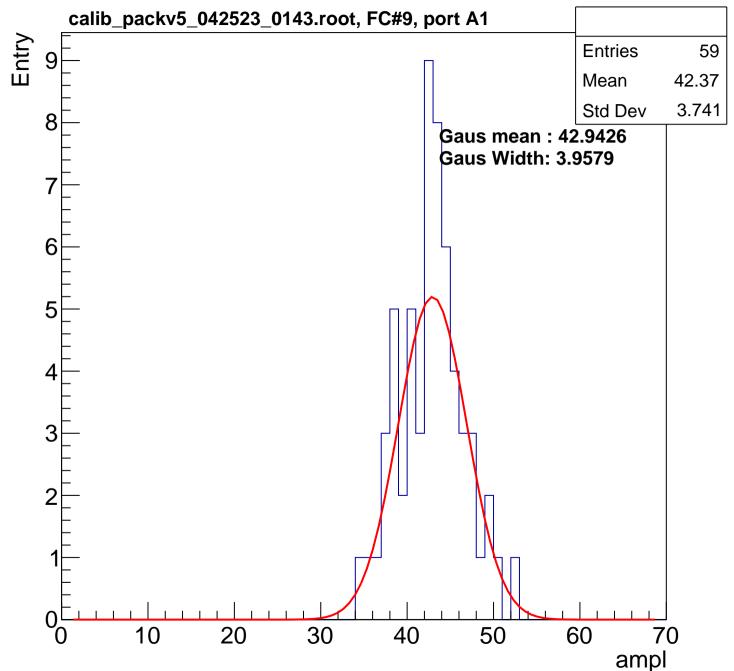


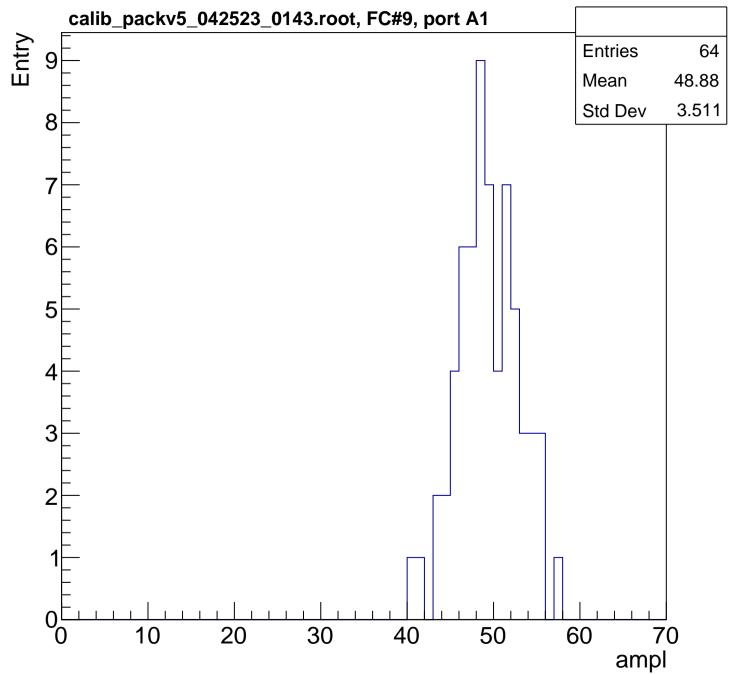


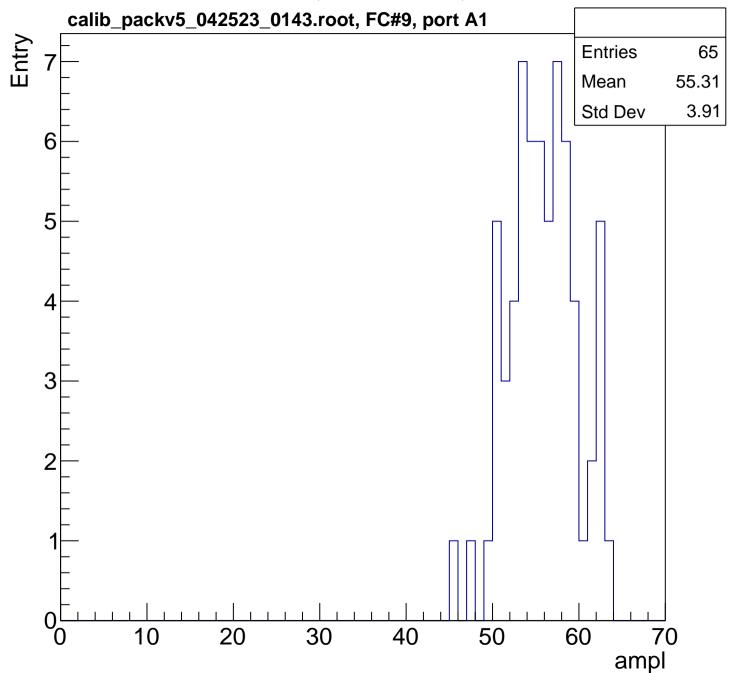


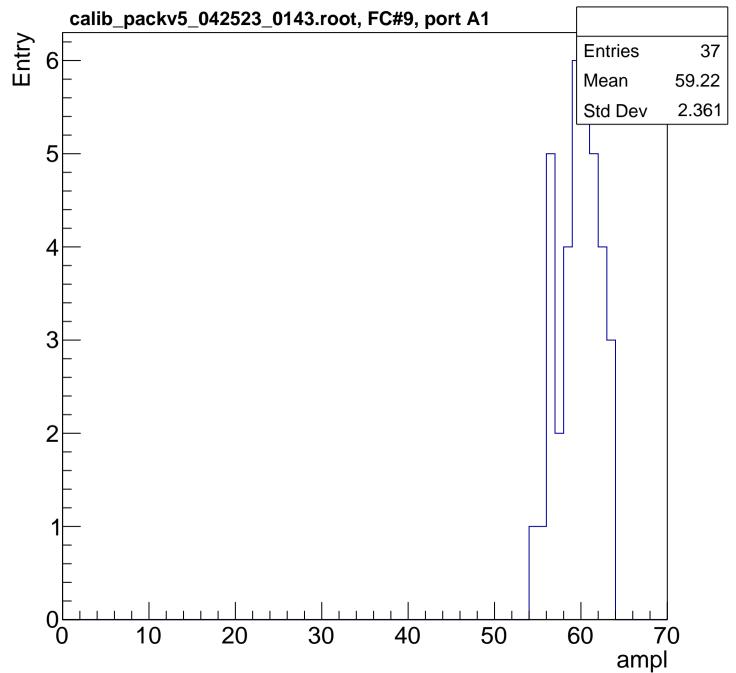


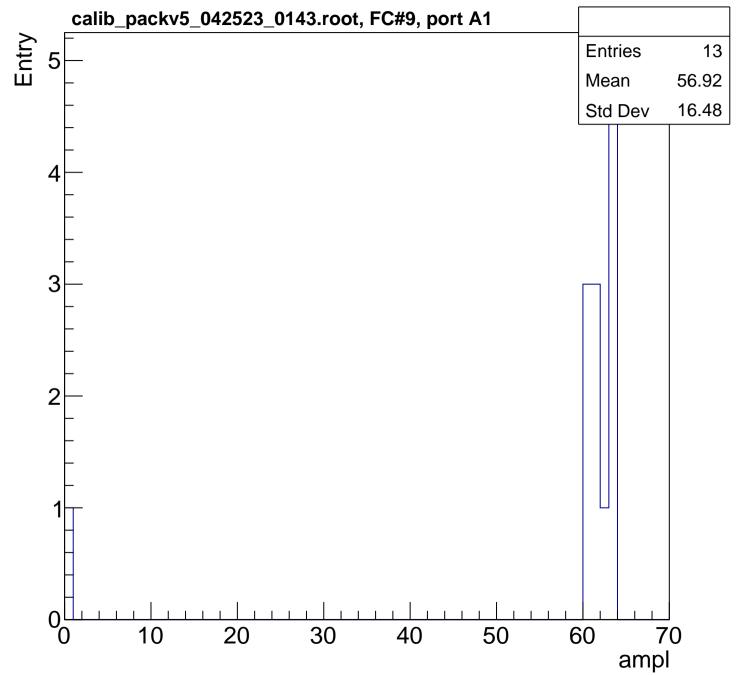


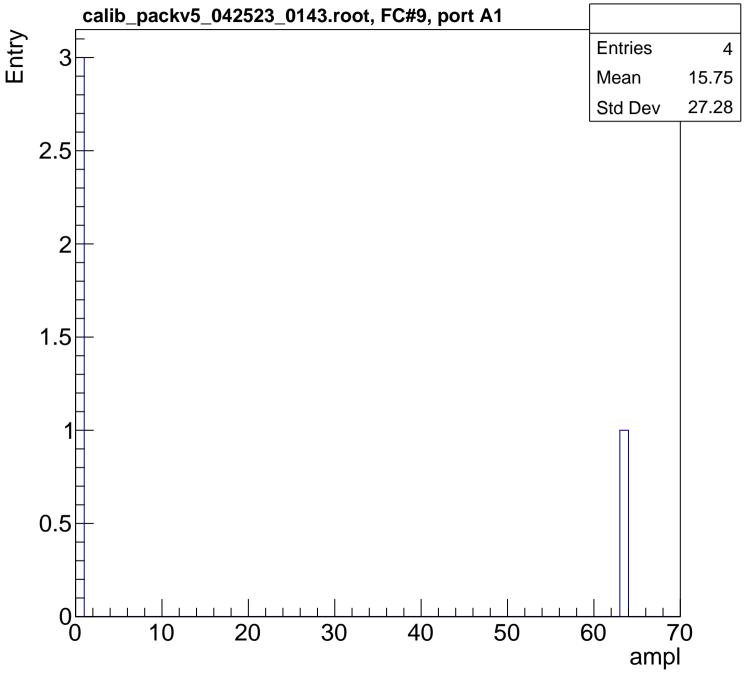


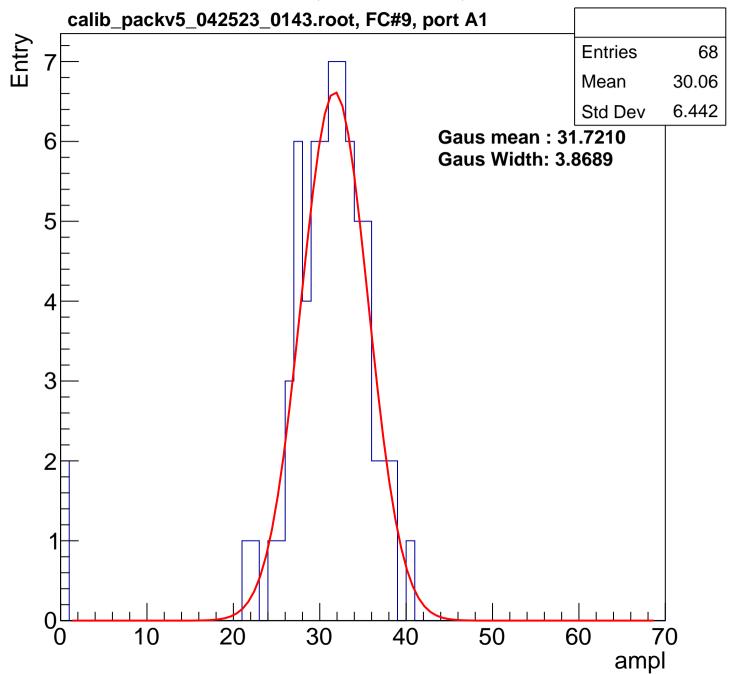


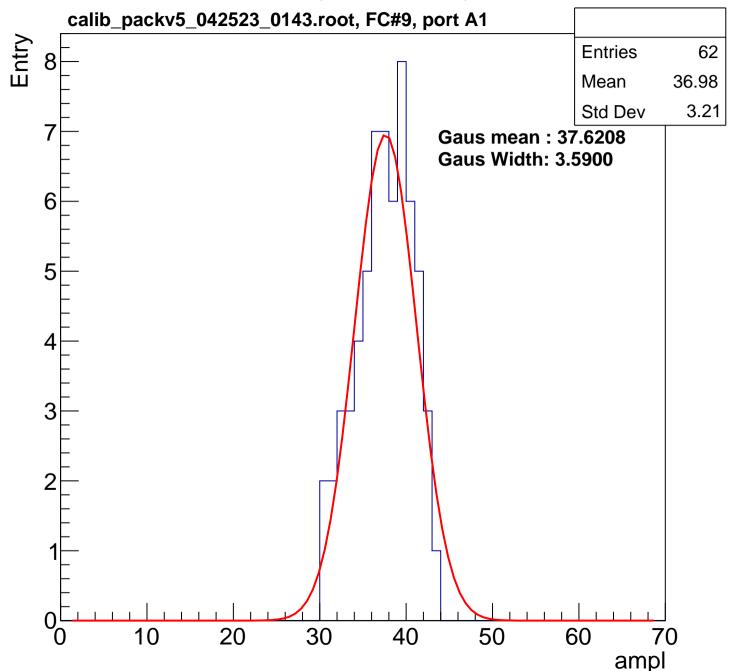


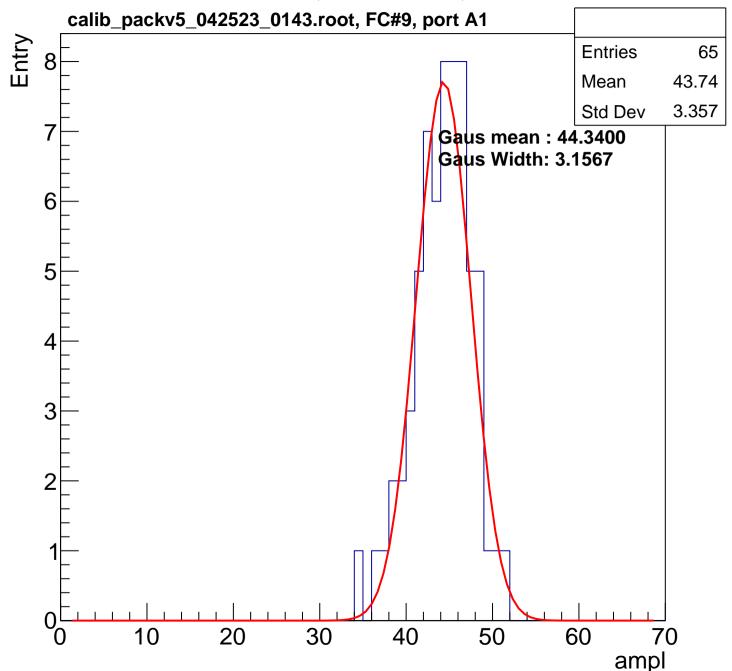


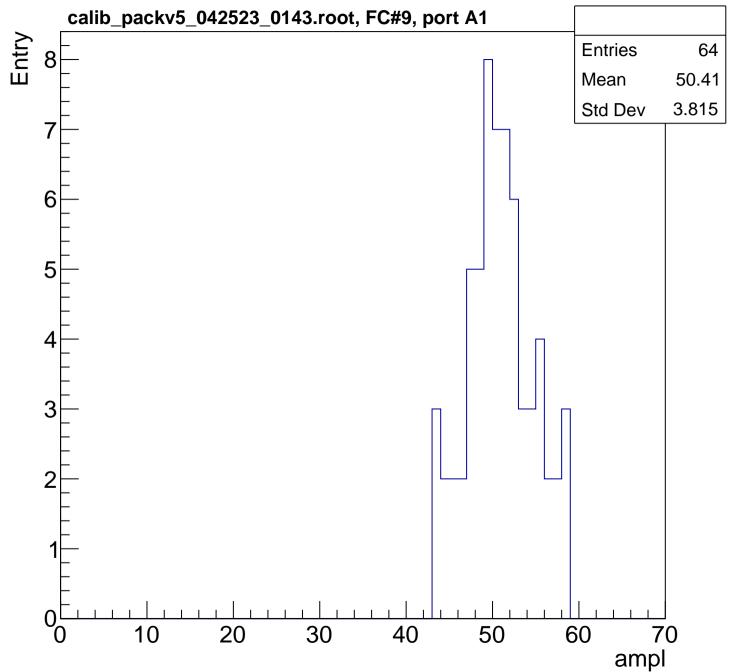


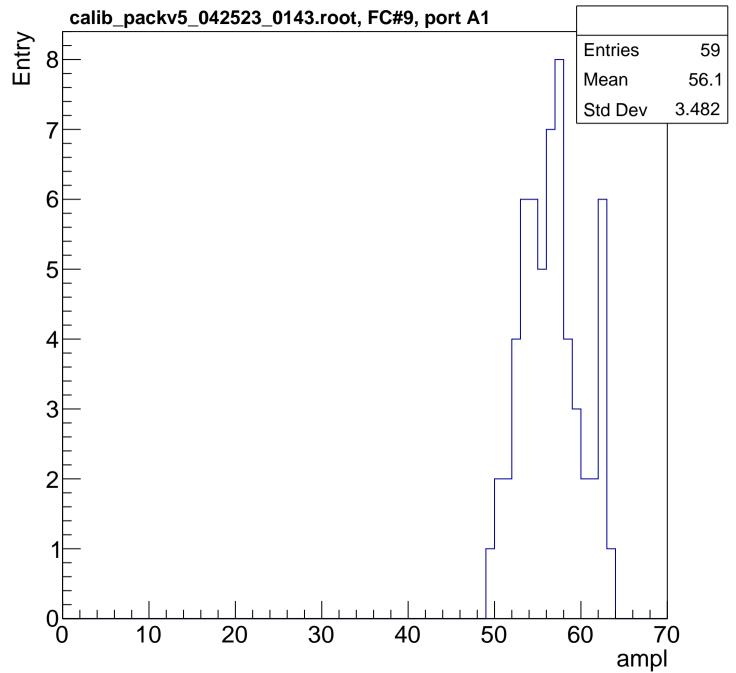


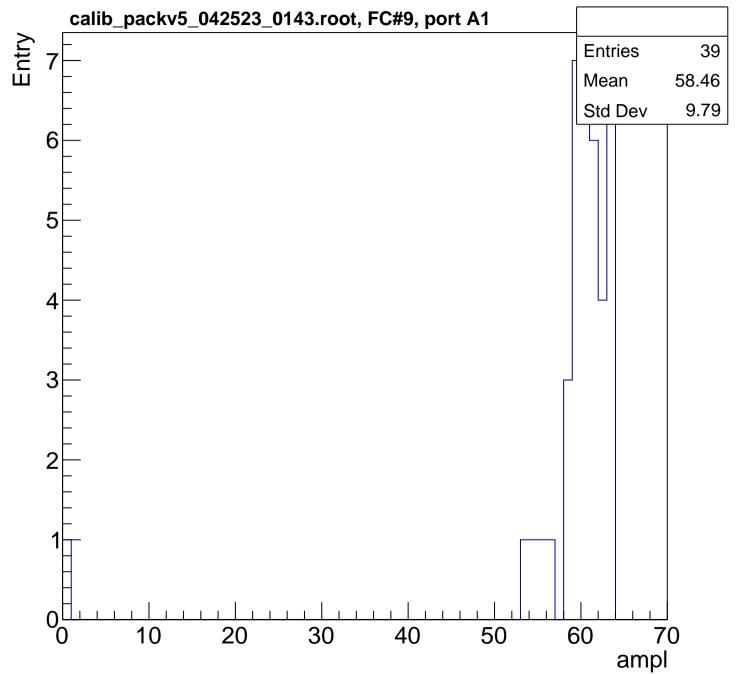


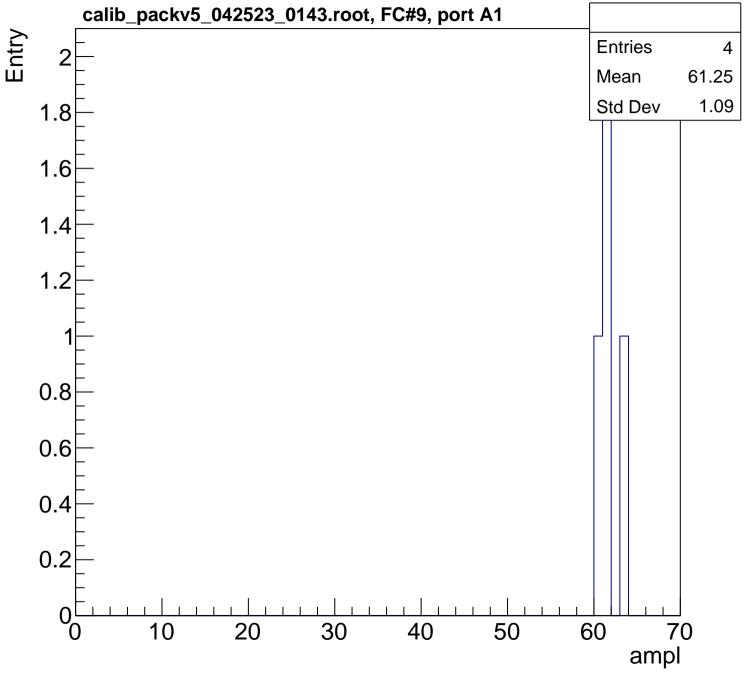


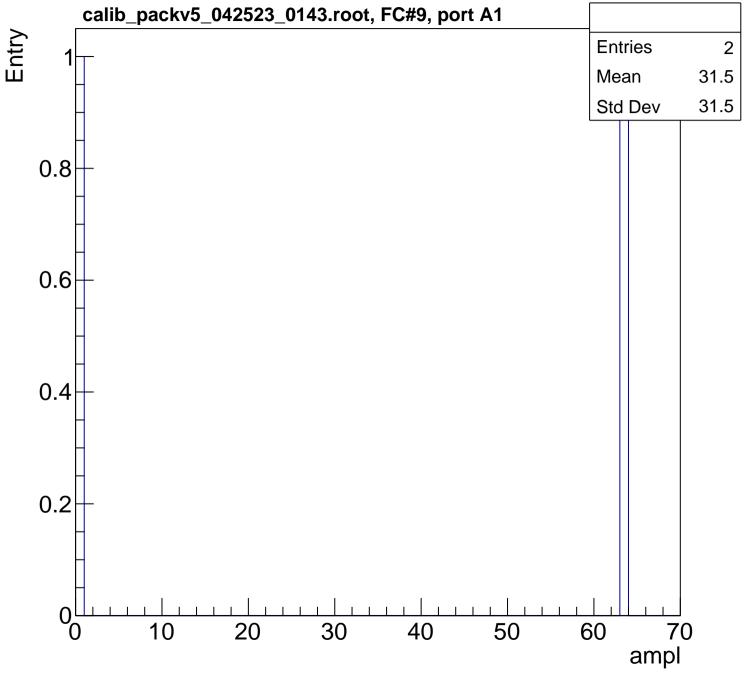


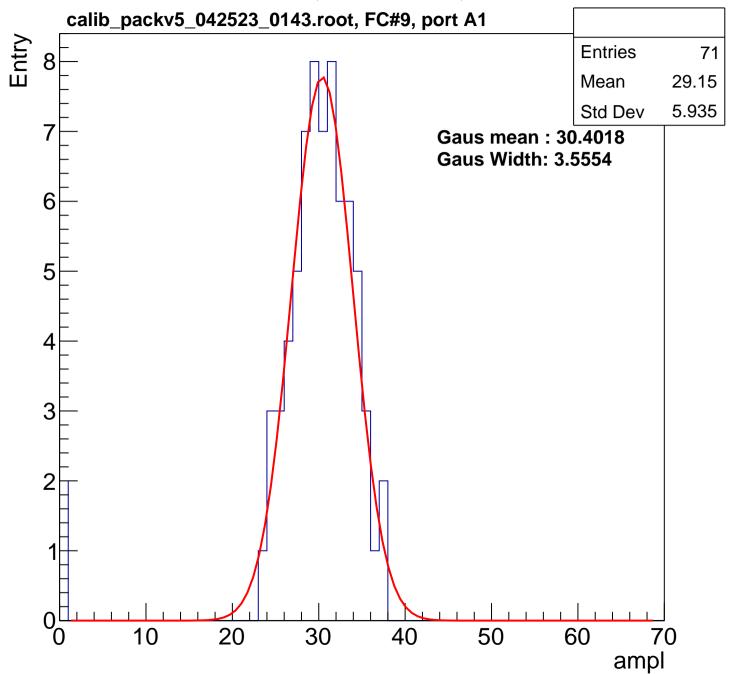


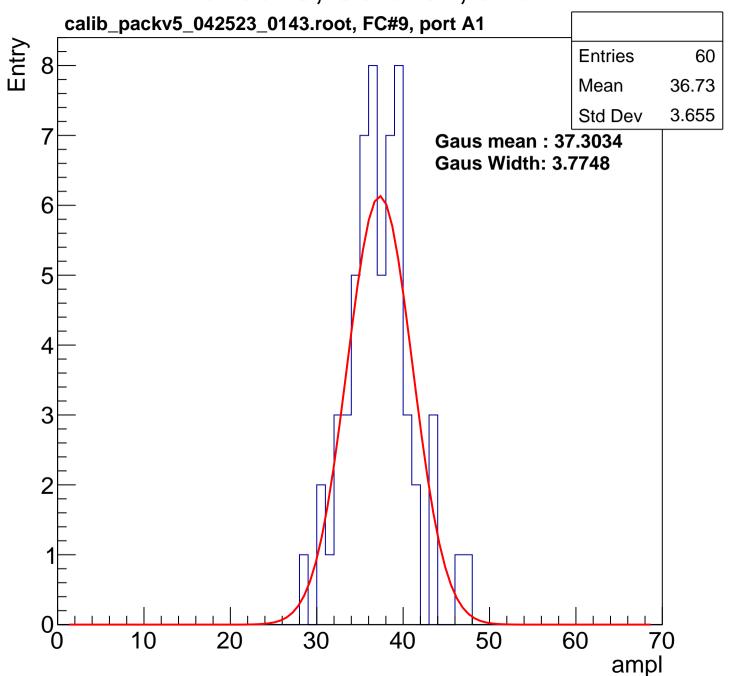


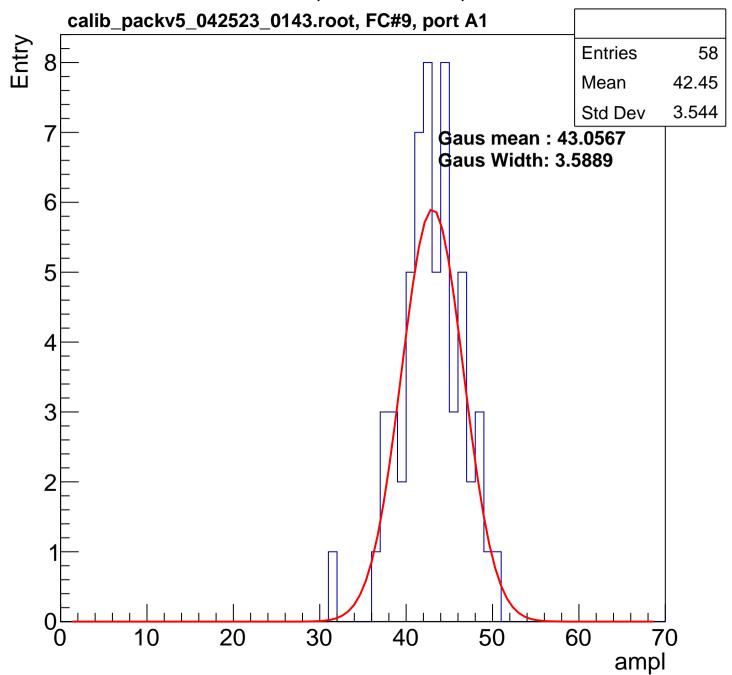


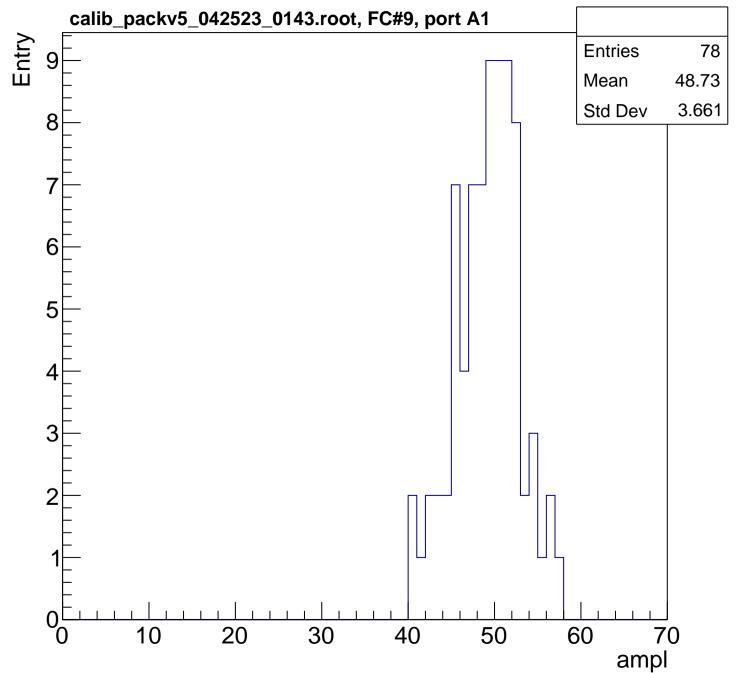


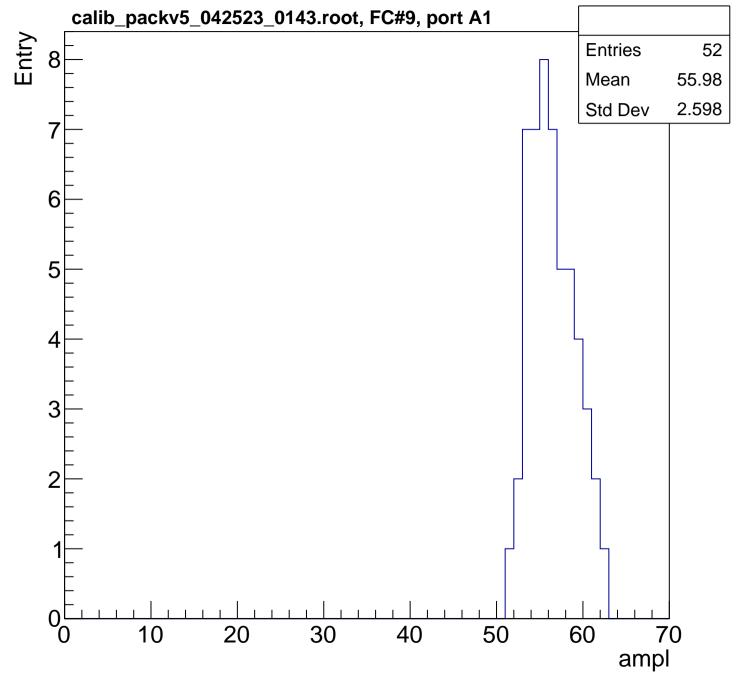


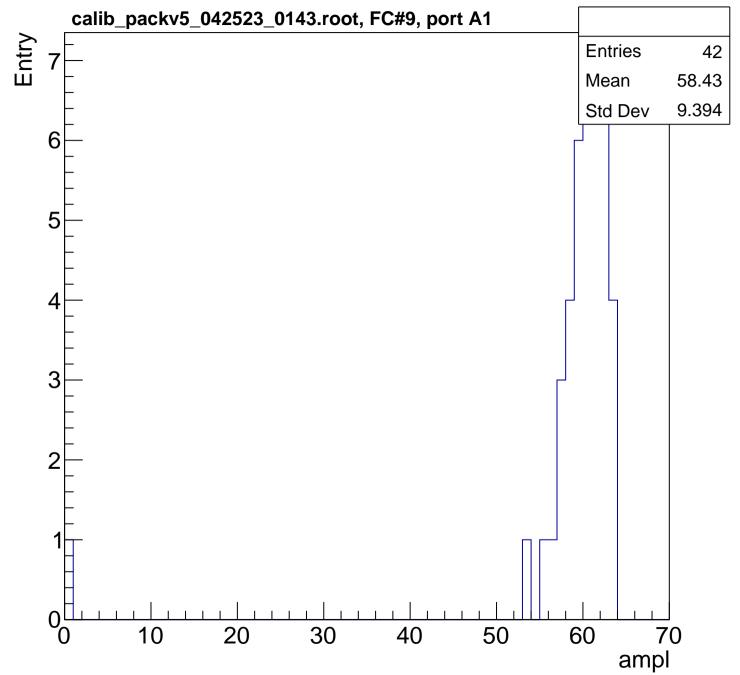


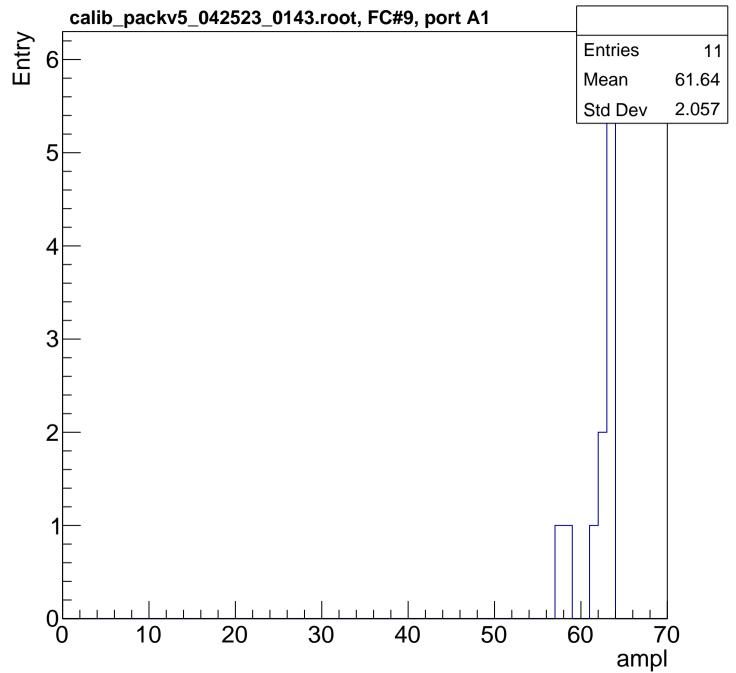




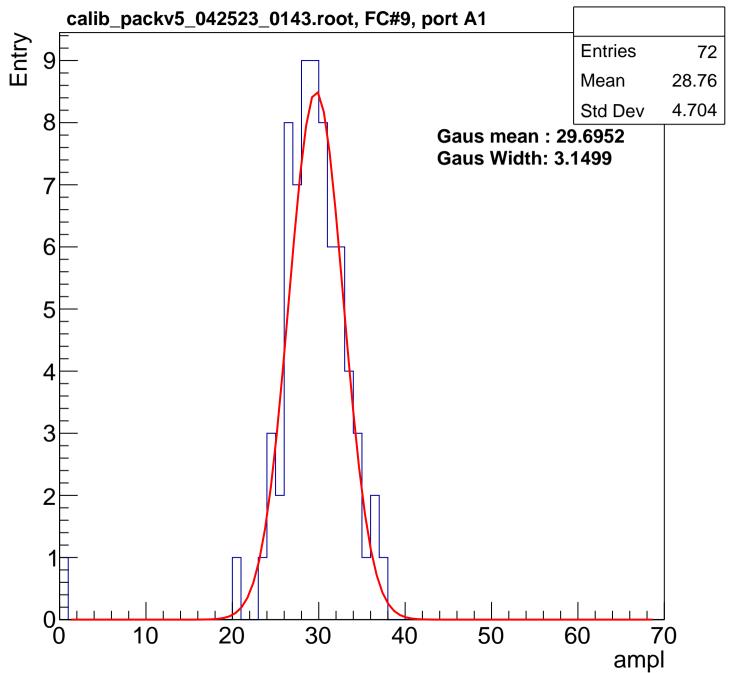


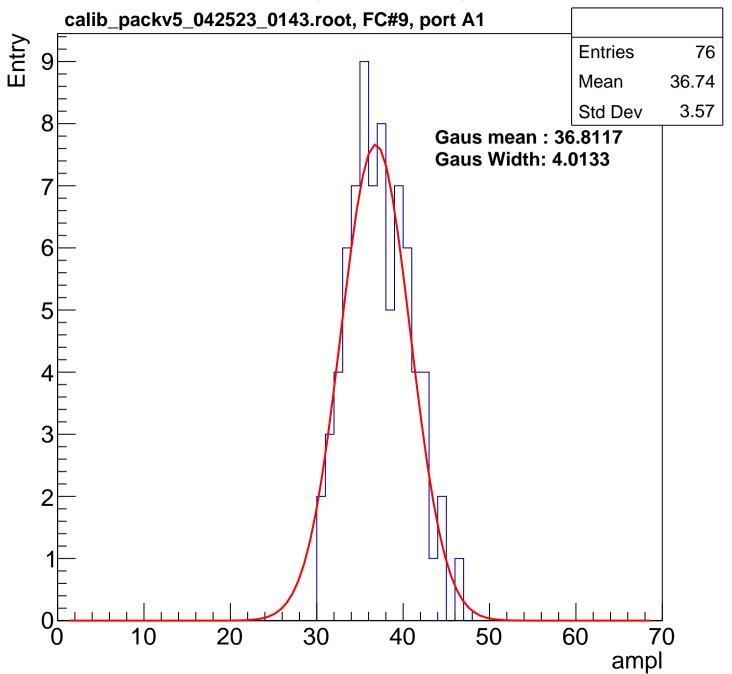


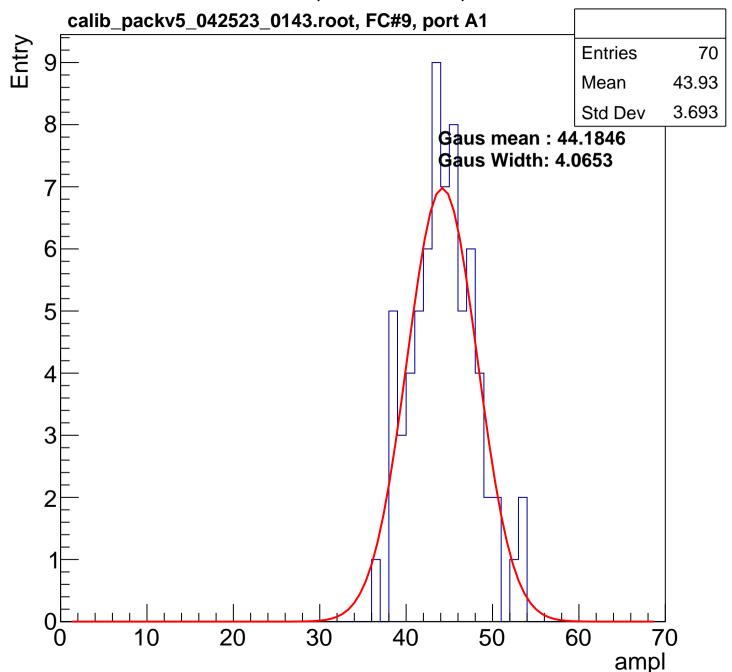


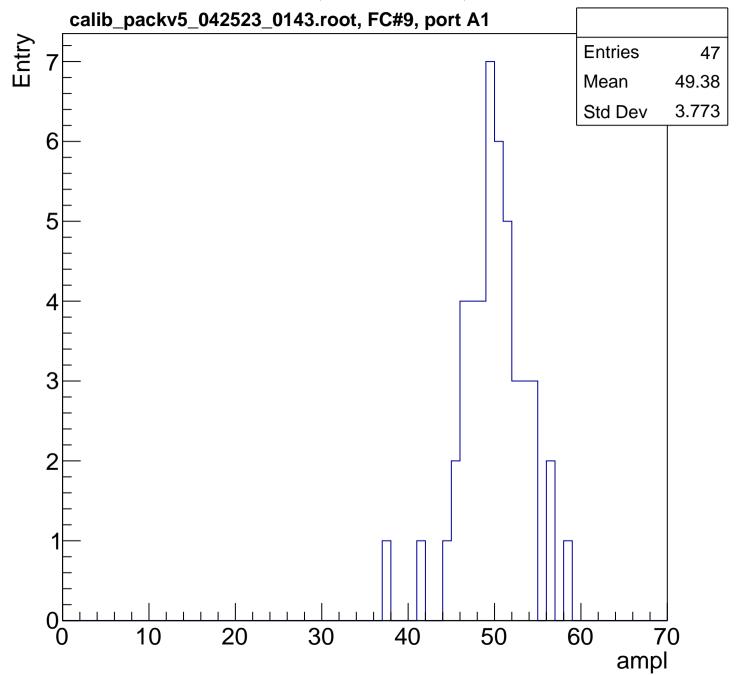


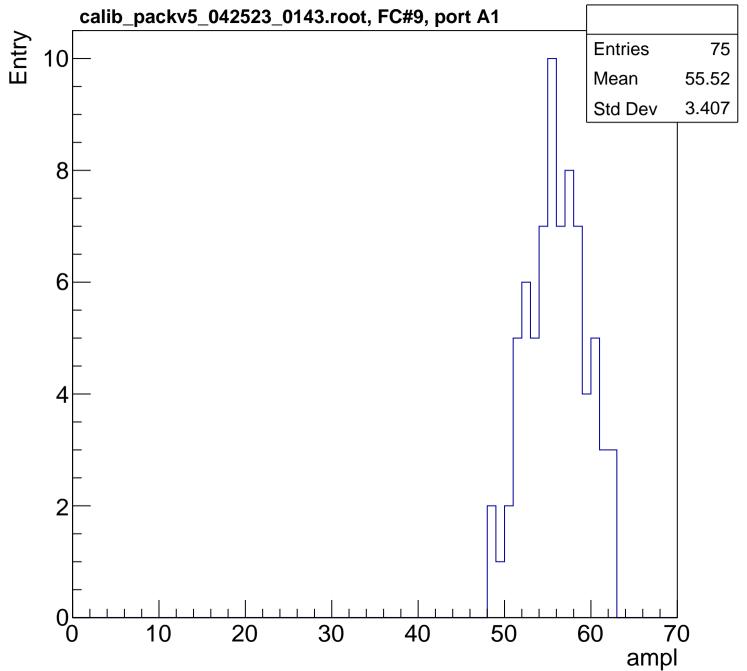


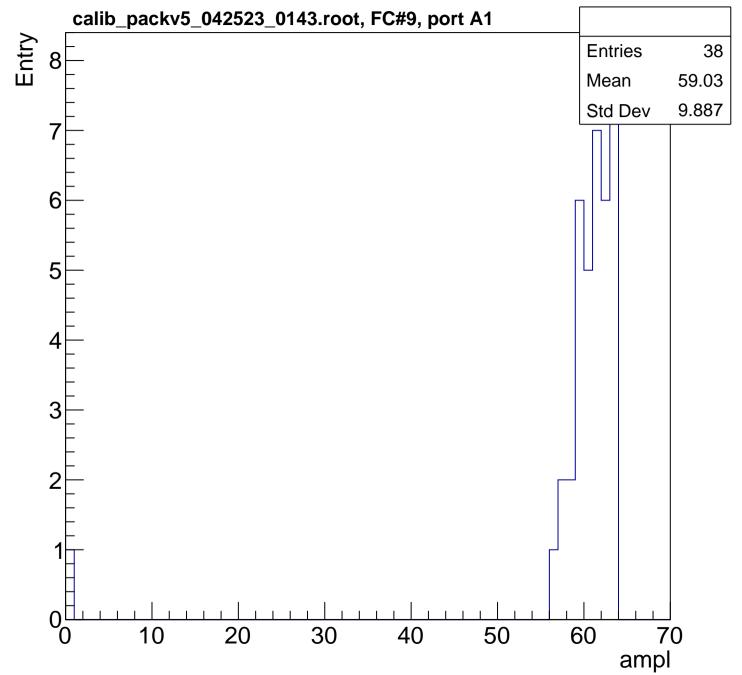


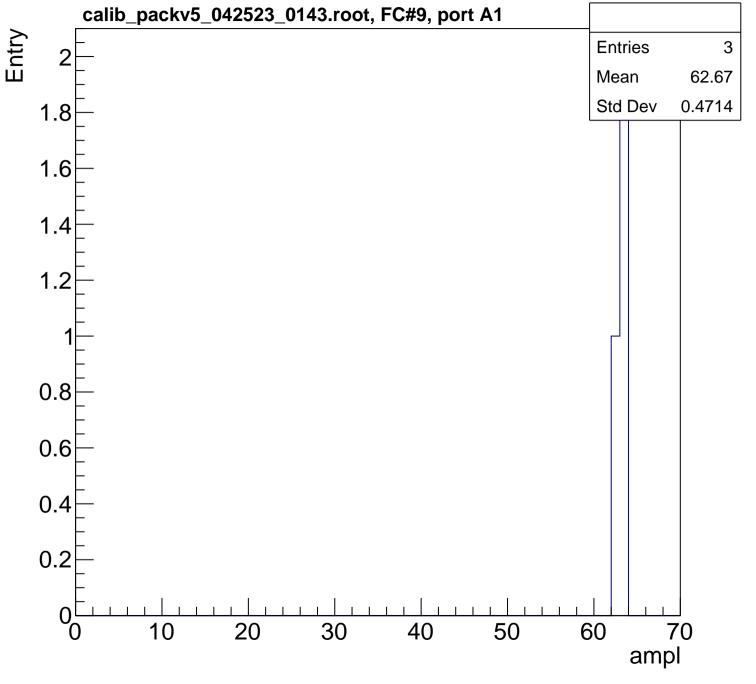


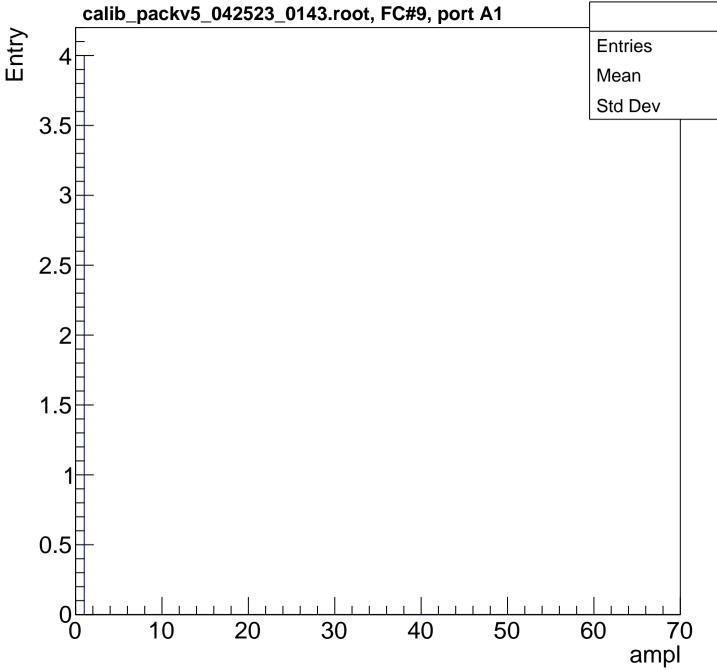


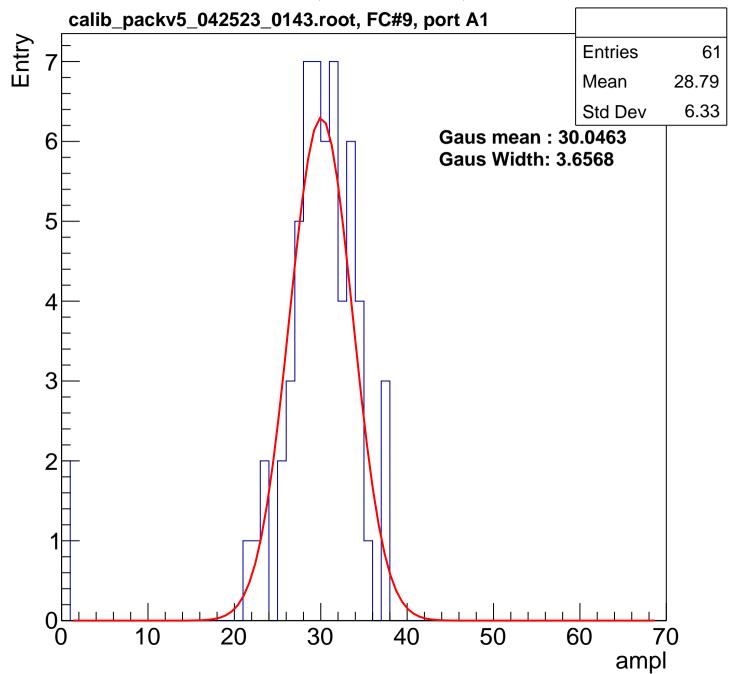


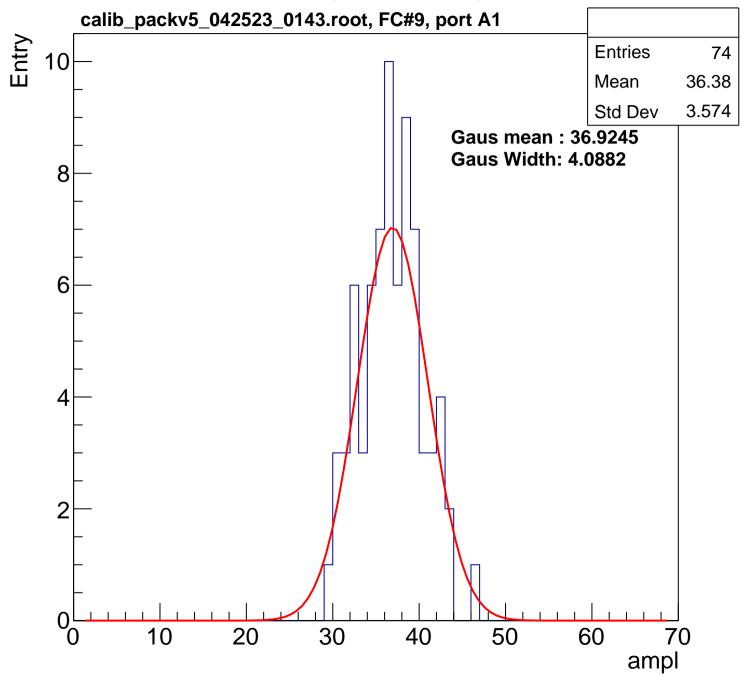


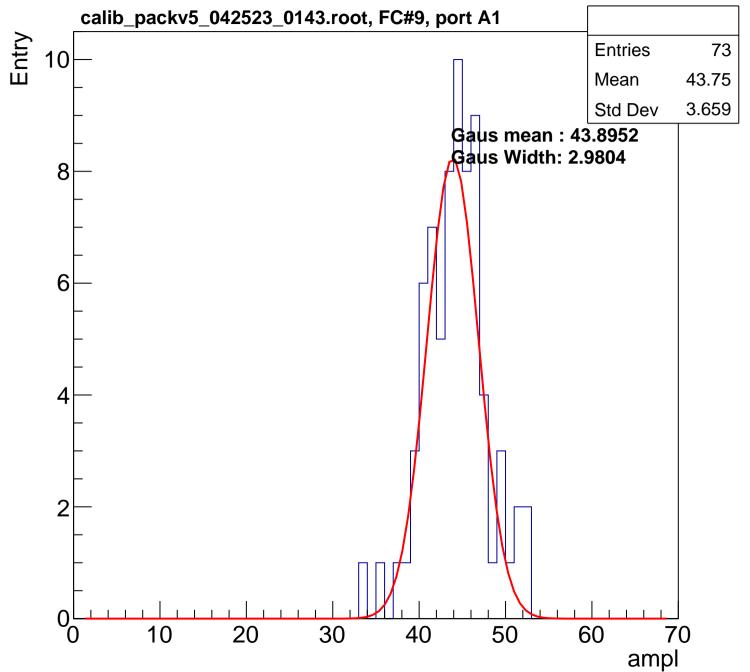


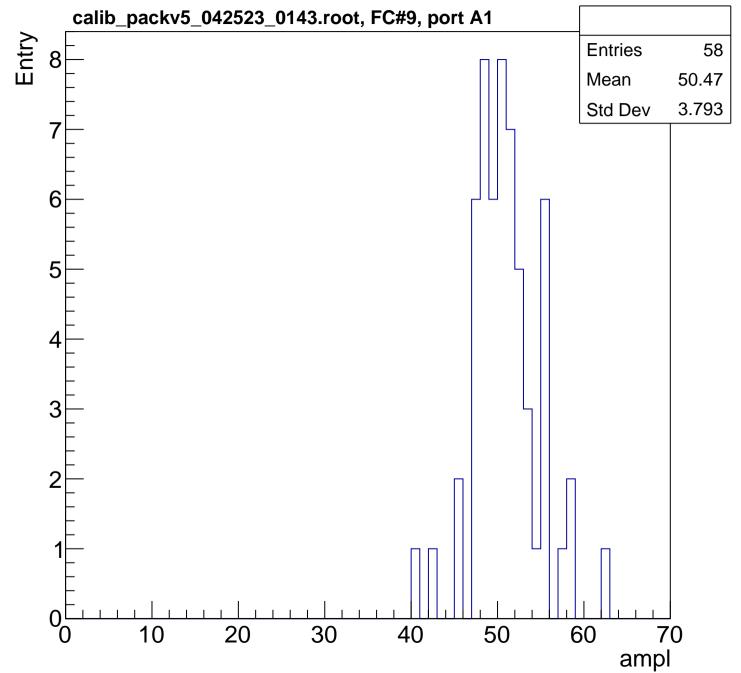


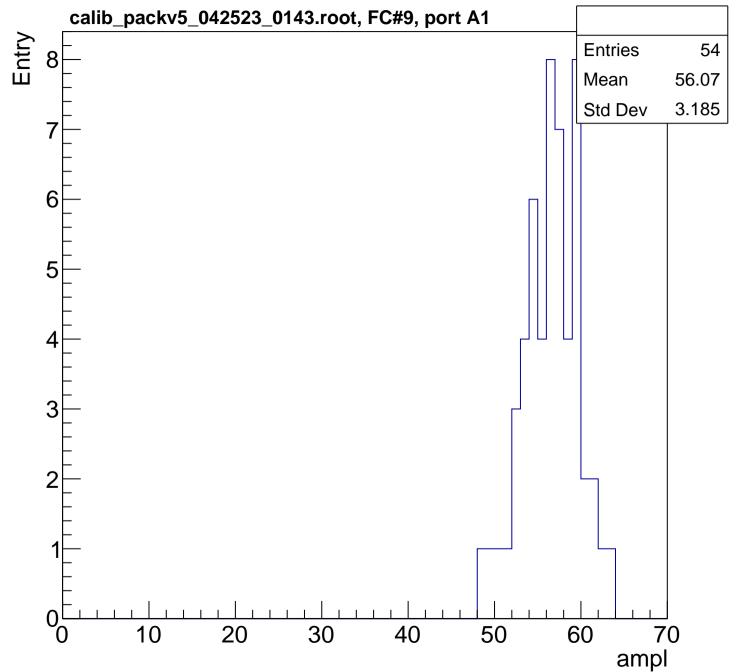


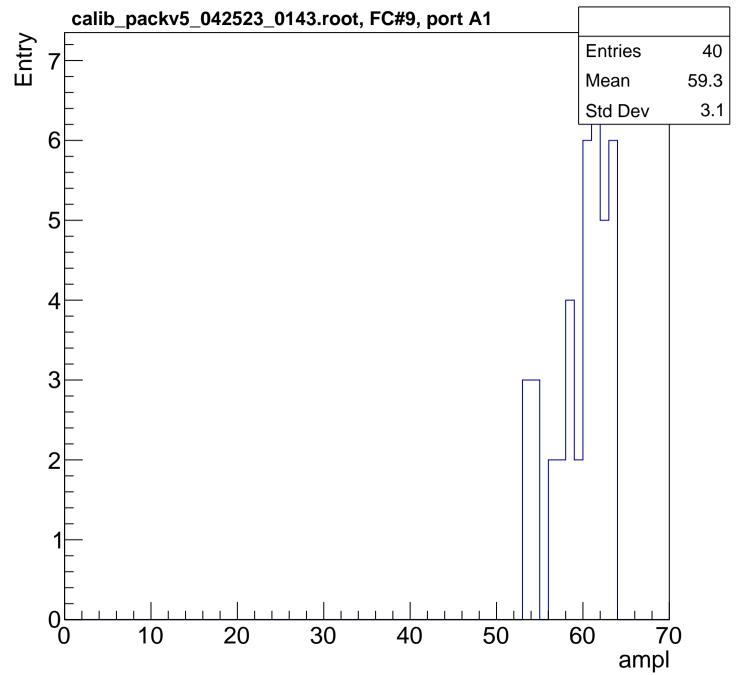


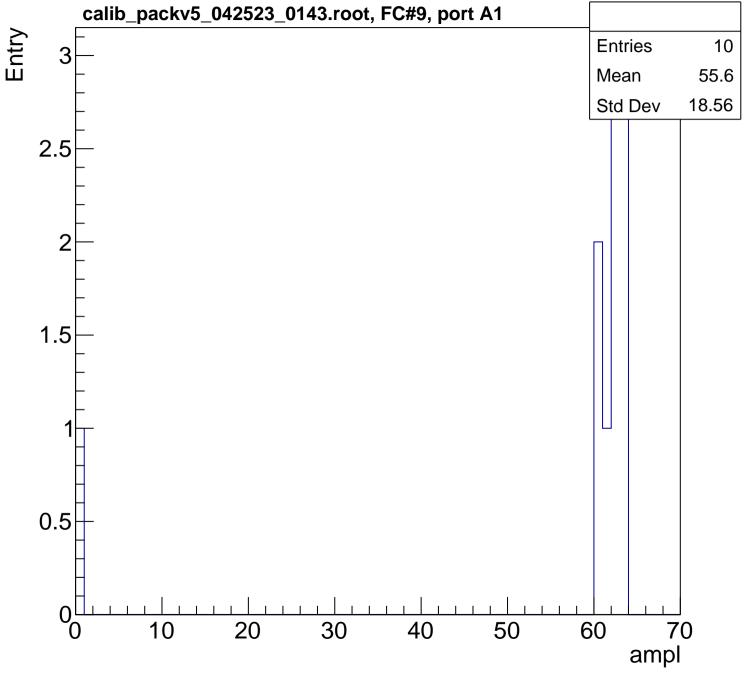


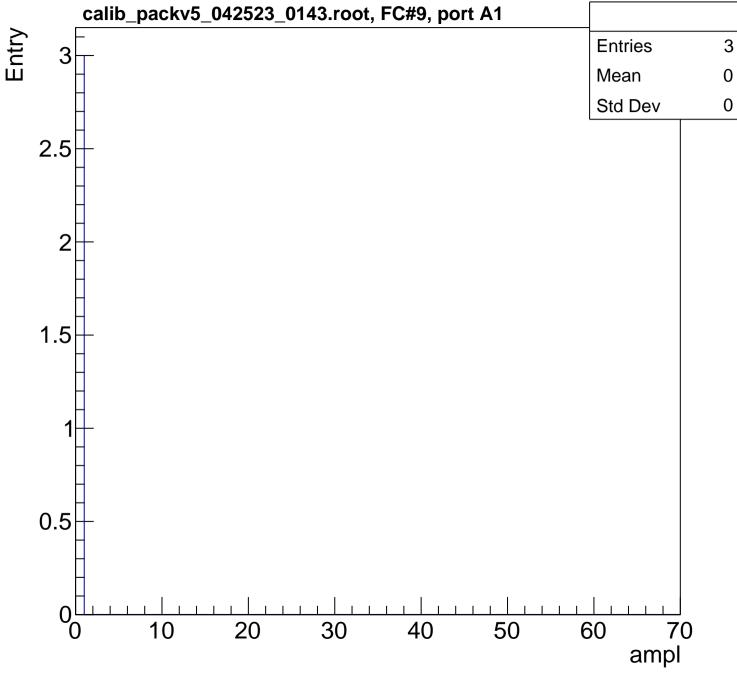


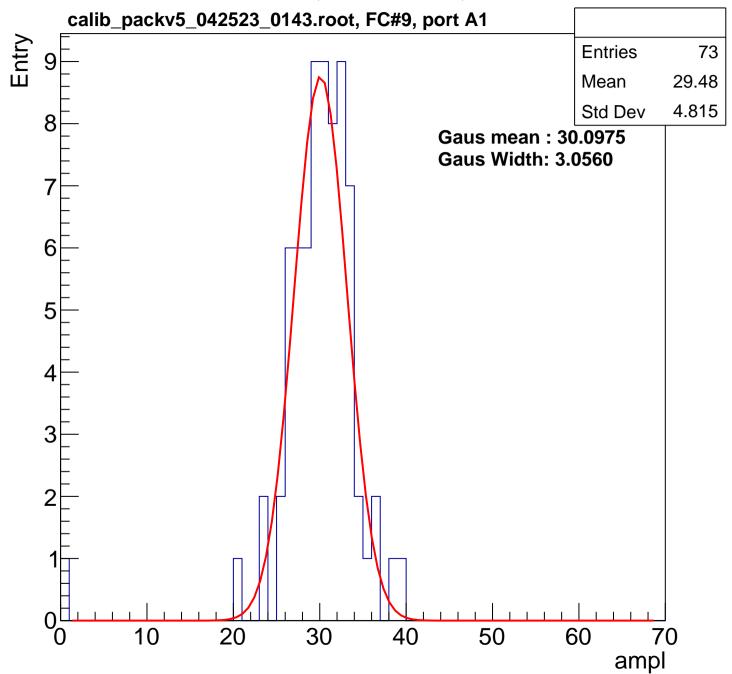


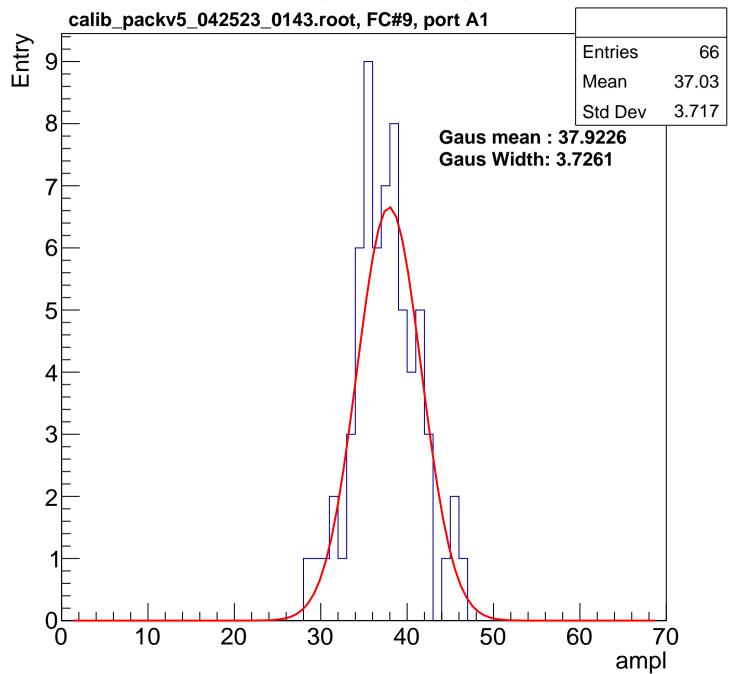


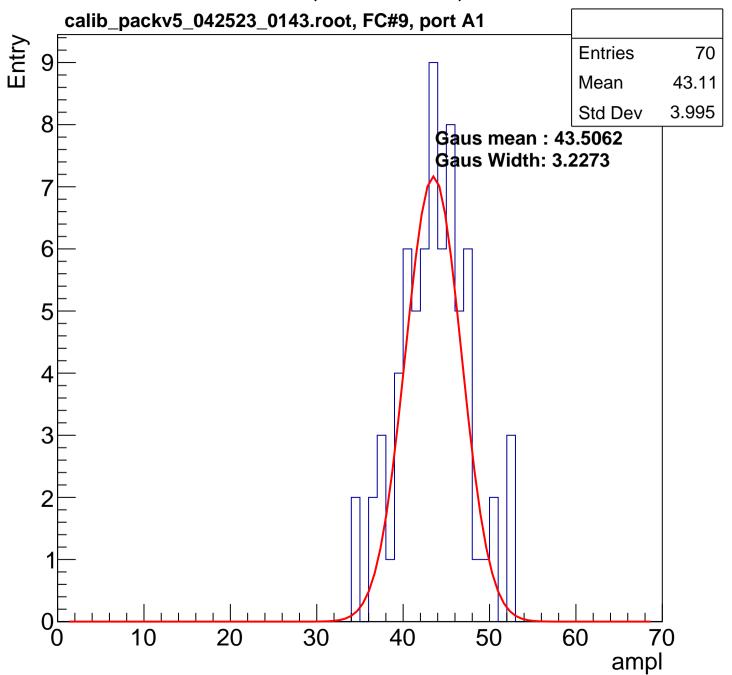


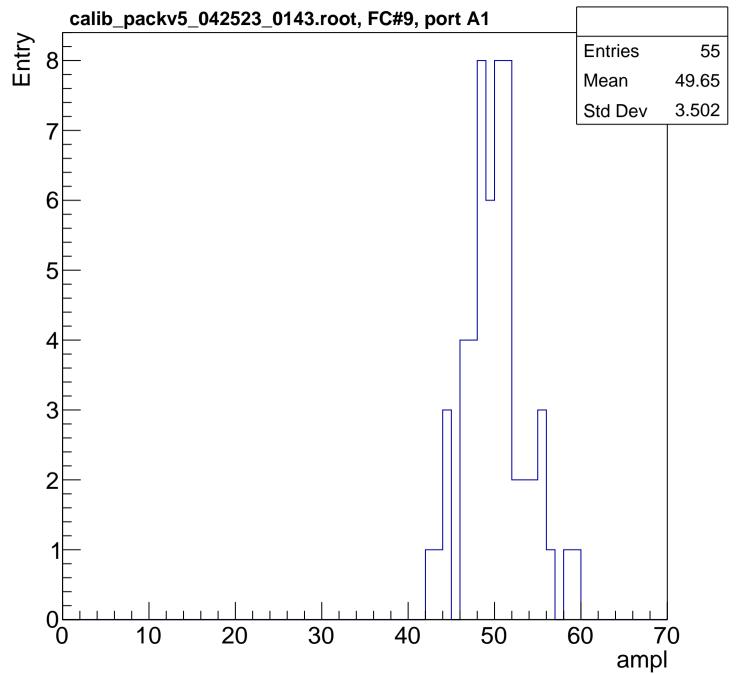


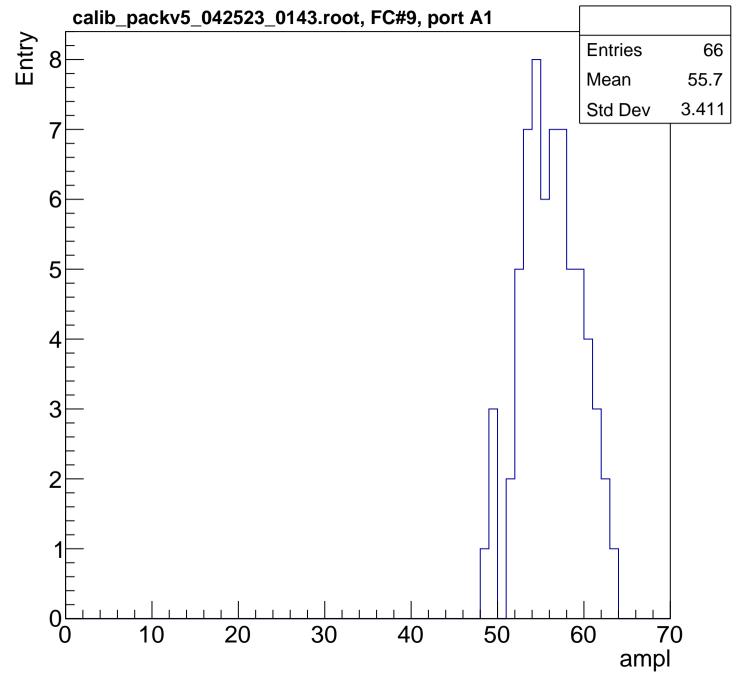


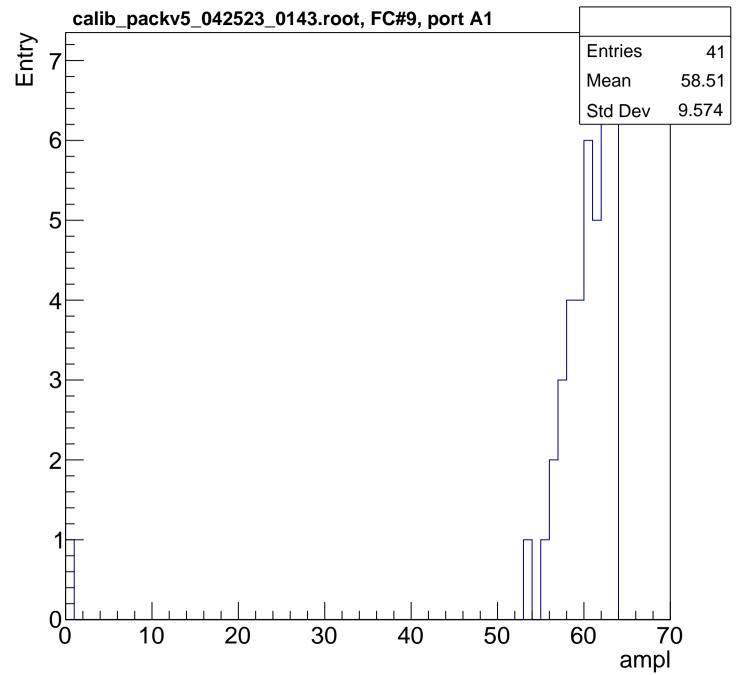


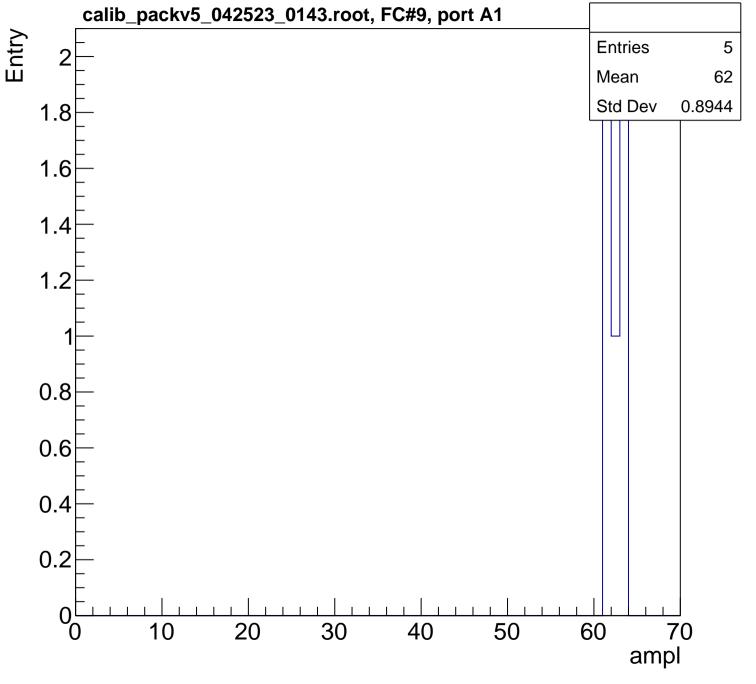




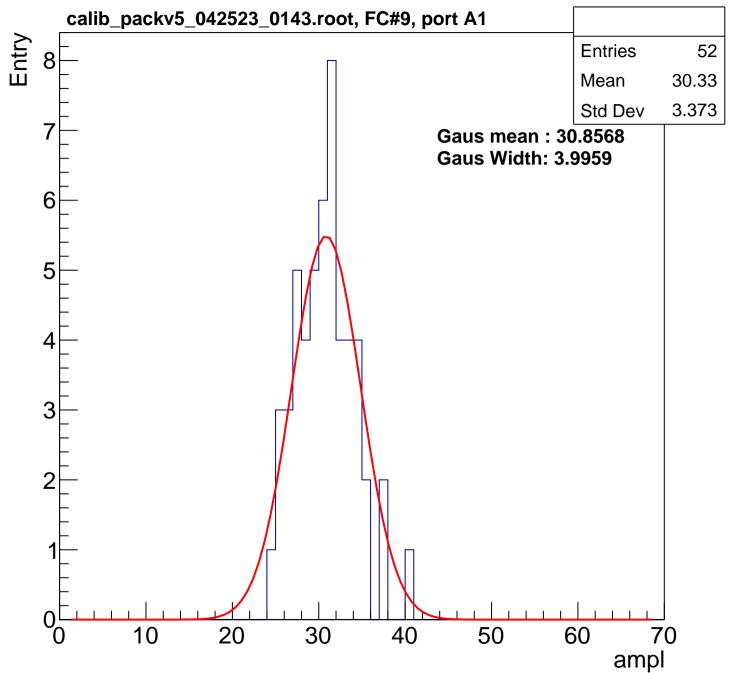


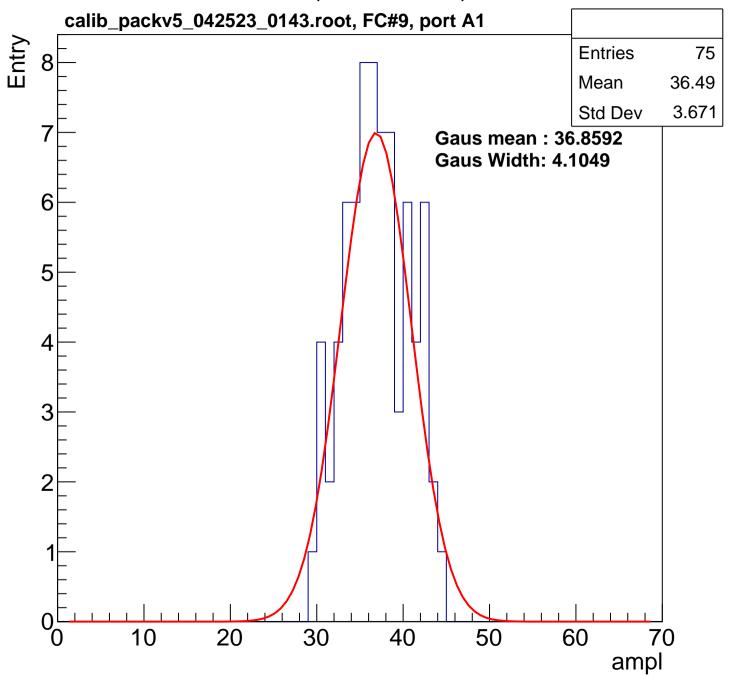


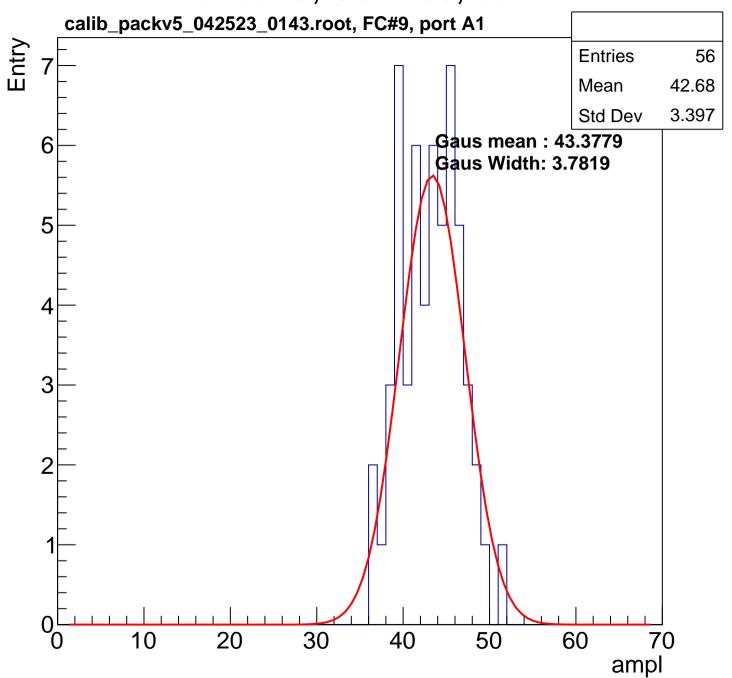


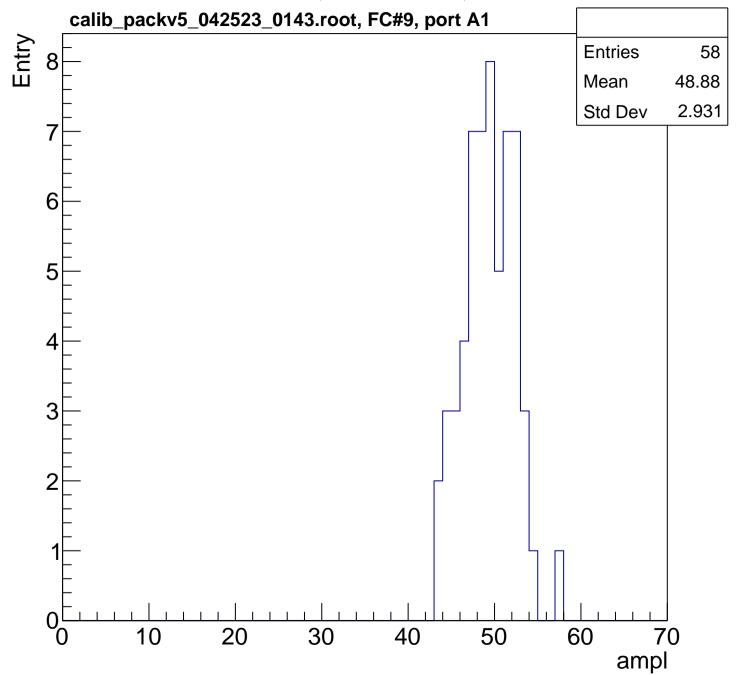


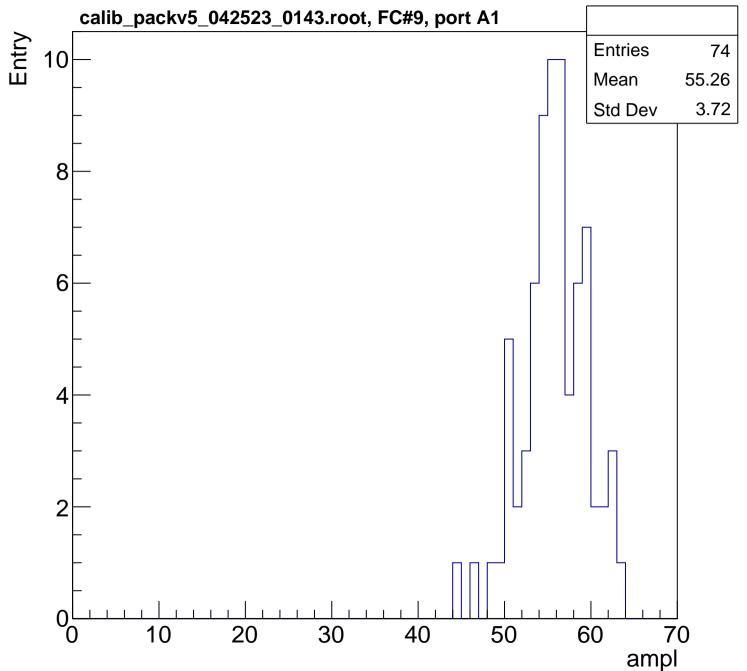


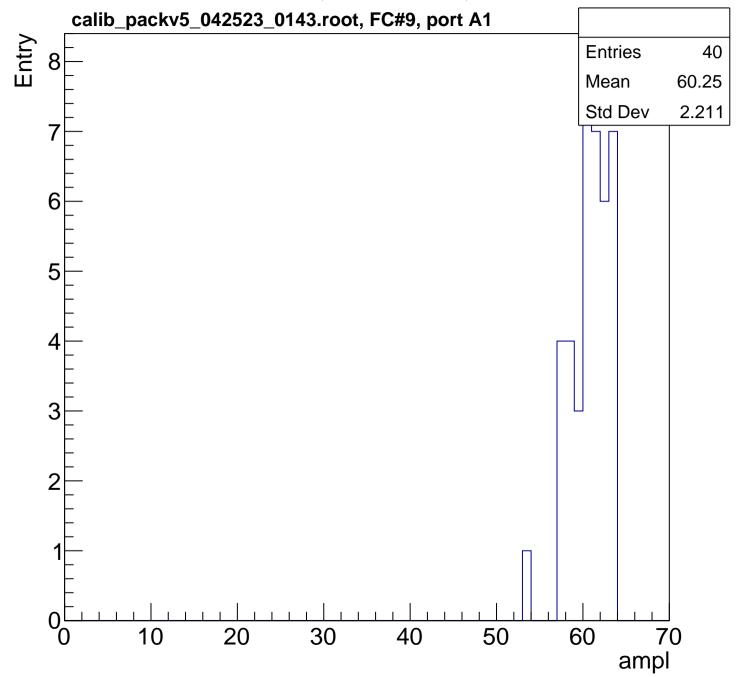


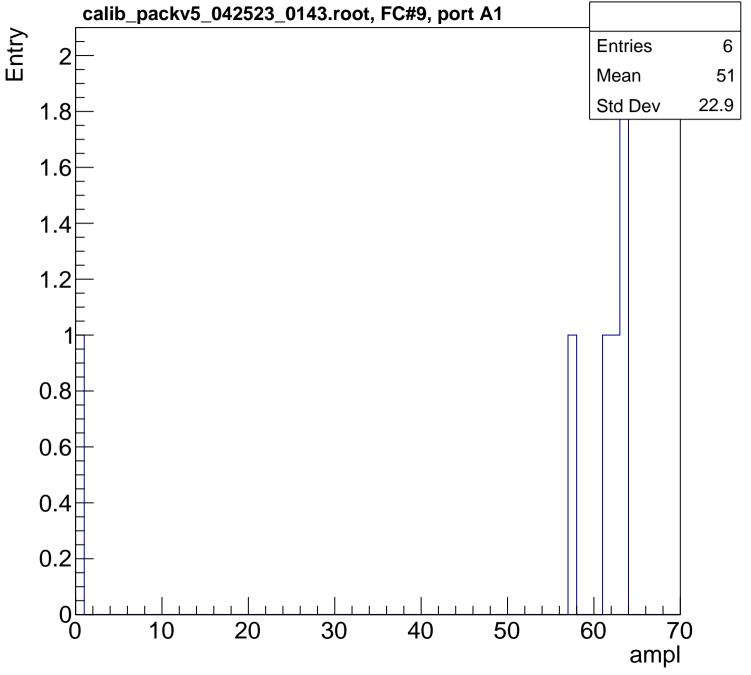












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