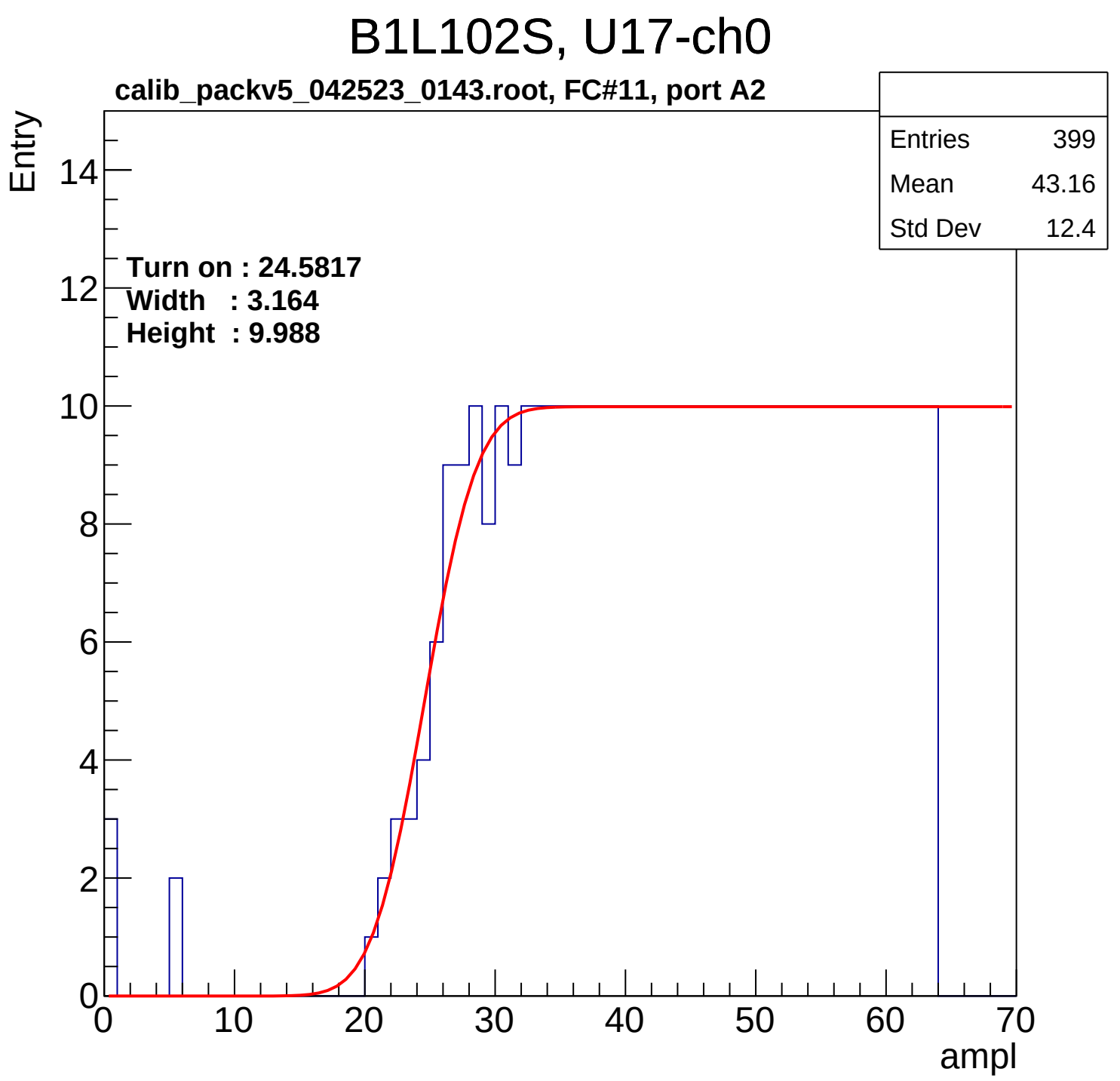
B1L102S, U17-ch0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 399
Mean 43.16
Std Dev 12.4
Turn on : 24.5817
Width : 3.164
Height : 9.988
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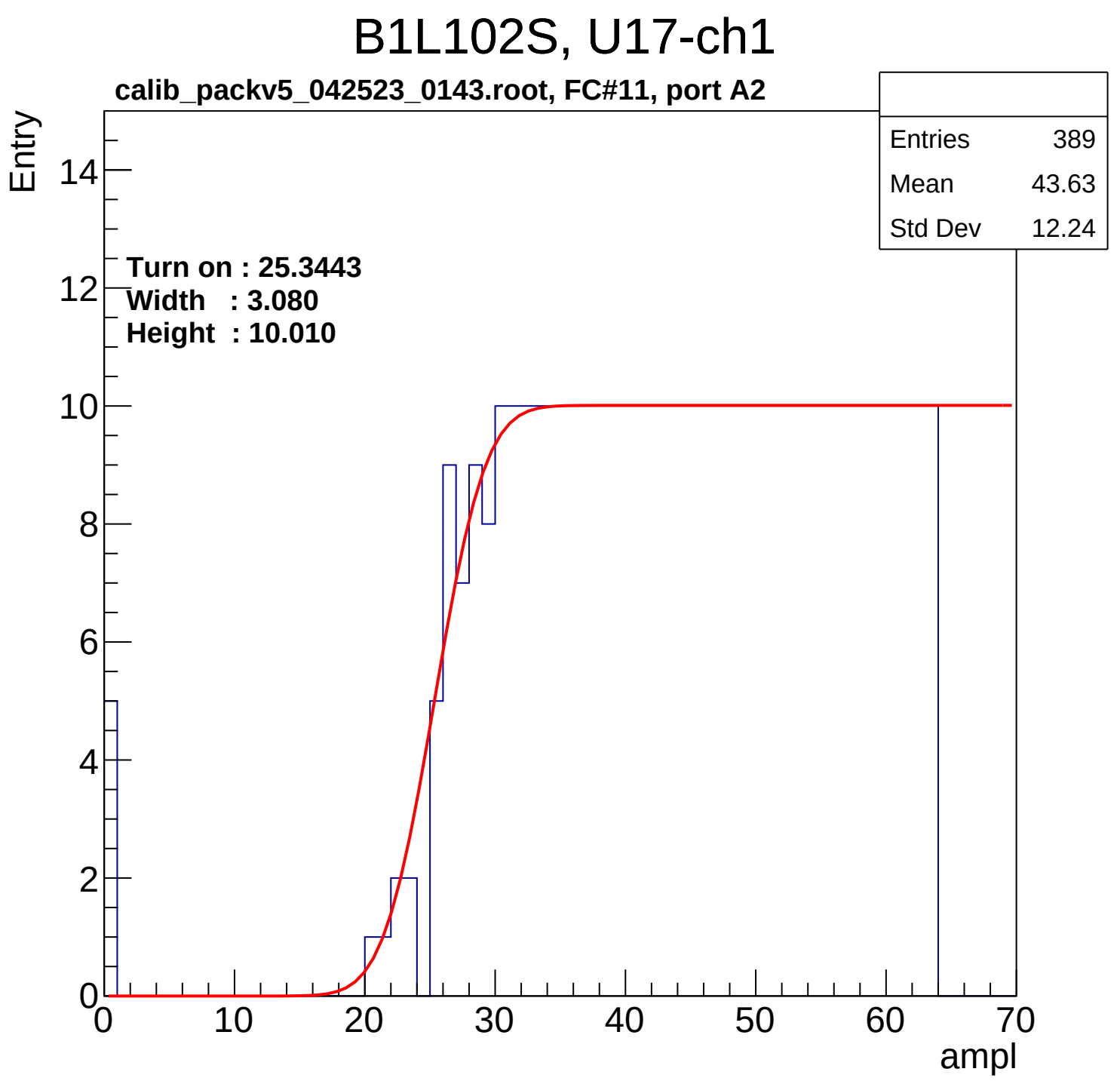
B1L102S, U17-ch1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 389
Mean 43.63
Std Dev 12.24
Turn on : 25.3443
Width : 3.080
Height : 10.010
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ampl
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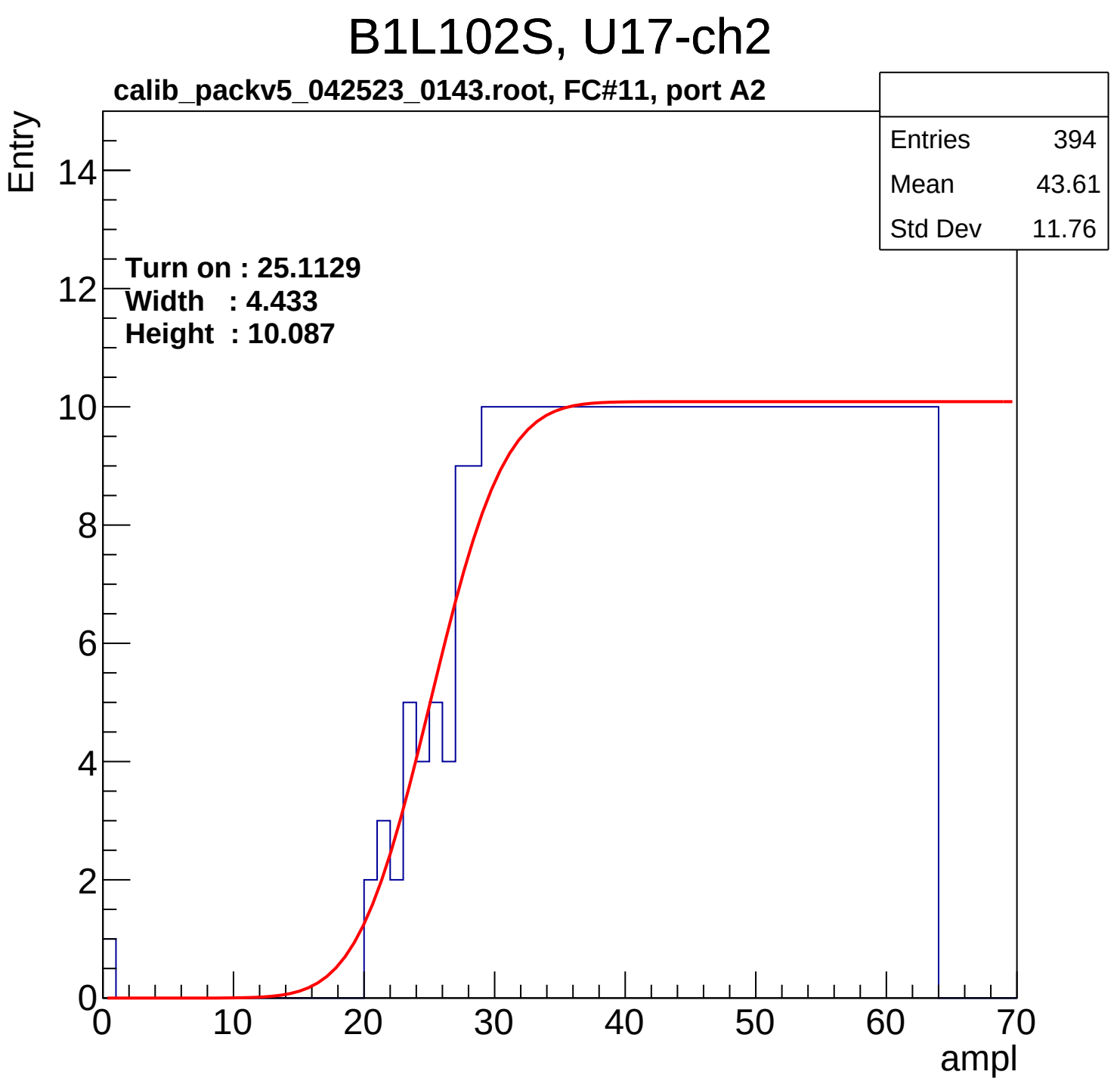
B1L102S, U17-ch2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 394
Mean 43.61
Std Dev 11.76
Turn on : 25.1129
Width : 4.433
Height : 10.087
Entry
ampl
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2
4
6
8
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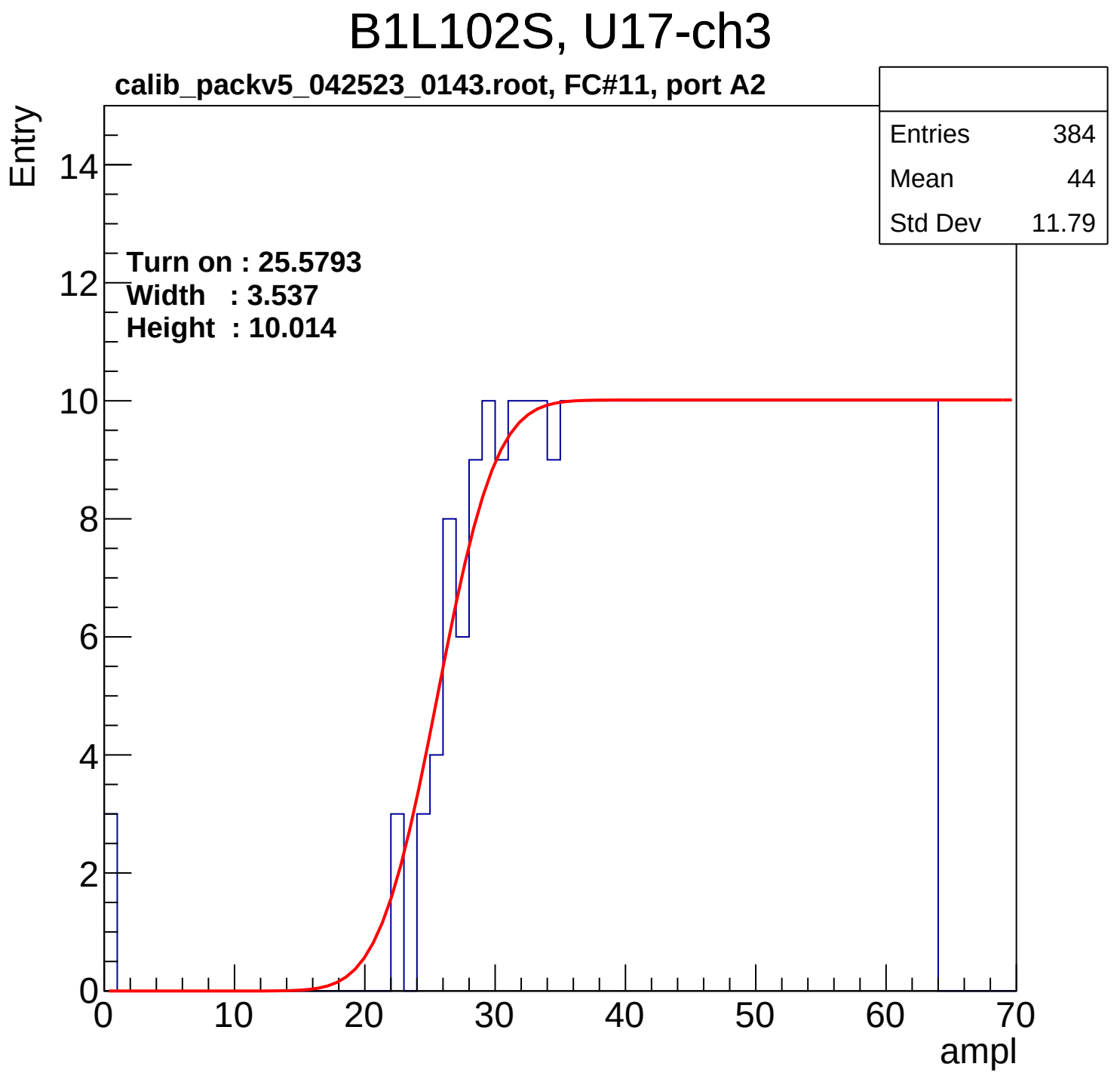
B1L102S, U17-ch3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 384
Mean 44
Std Dev 11.79
Turn on : 25.5793
Width : 3.537
Height : 10.014
Entry
ampl
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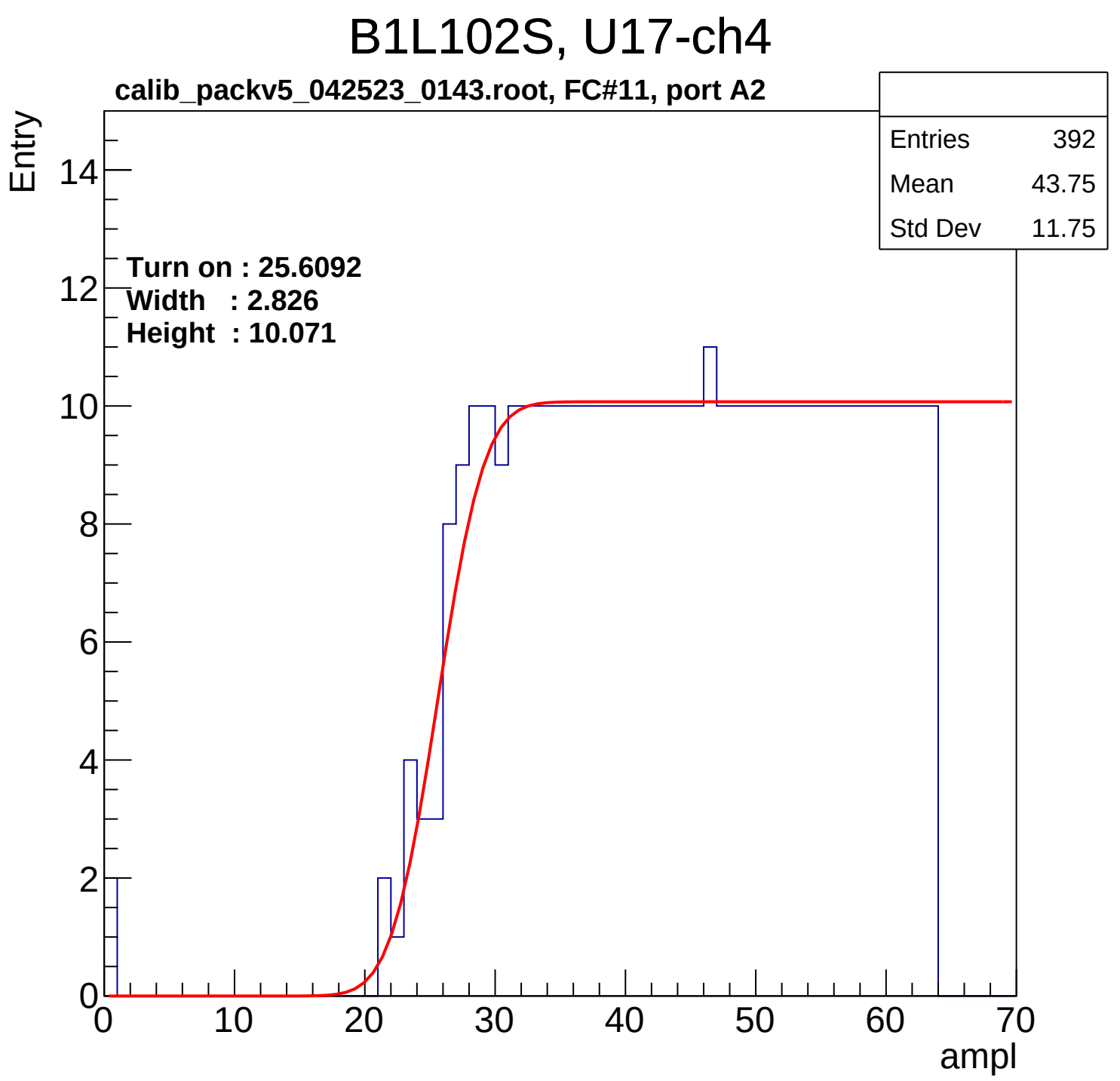
B1L102S, U17-ch4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 392
Mean 43.75
Std Dev 11.75
Turn on : 25.6092
Width : 2.826
Height : 10.071
Entry
ampl
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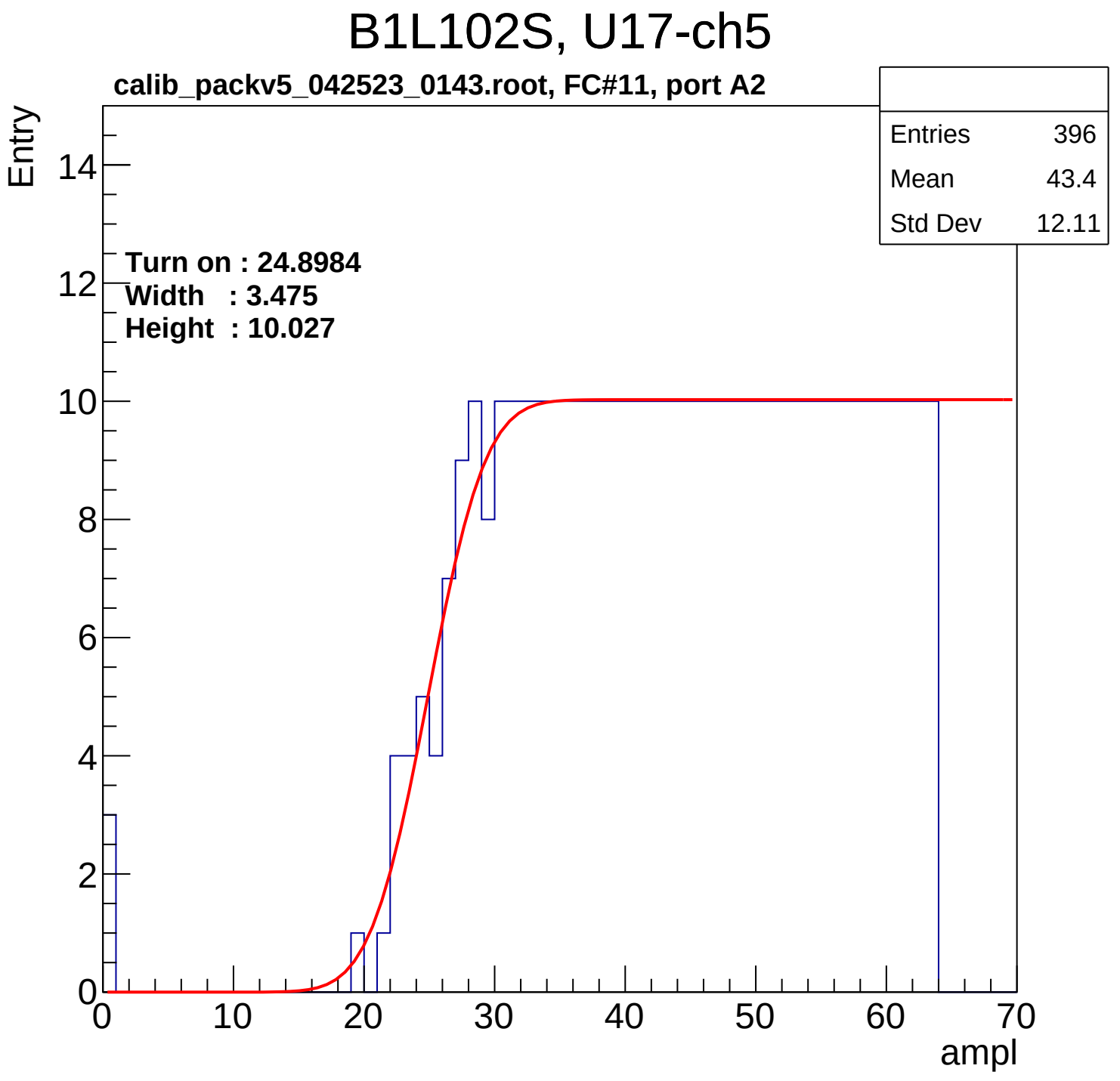
B1L102S, U17-ch5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 396
Mean 43.4
Std Dev 12.11
Turn on : 24.8984
Width : 3.475
Height : 10.027
Entry
ampl
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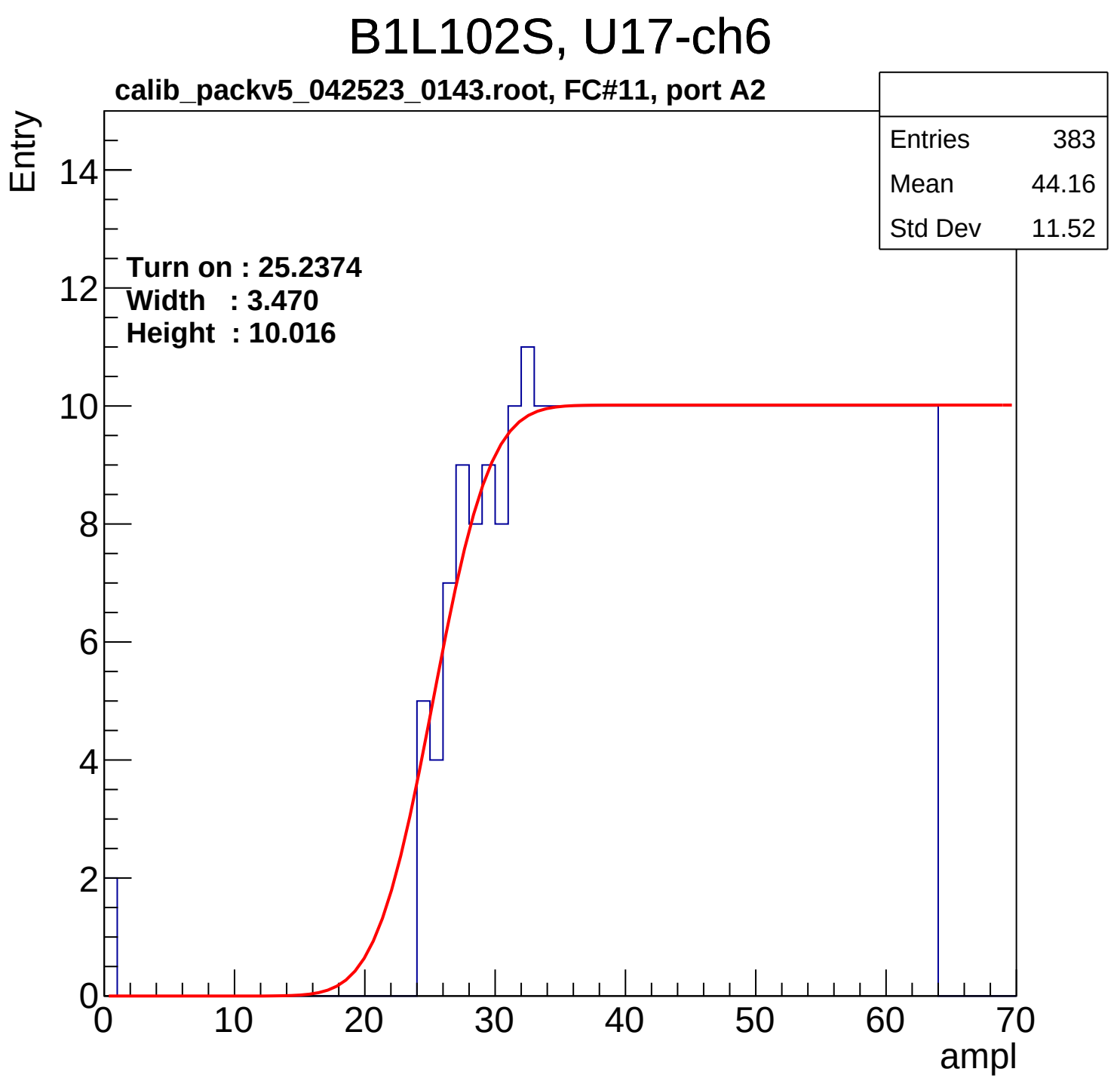
B1L102S, U17-ch6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 383
Mean 44.16
Std Dev 11.52
Turn on : 25.2374
Width : 3.470
Height : 10.016
Entry
ampl
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6
8
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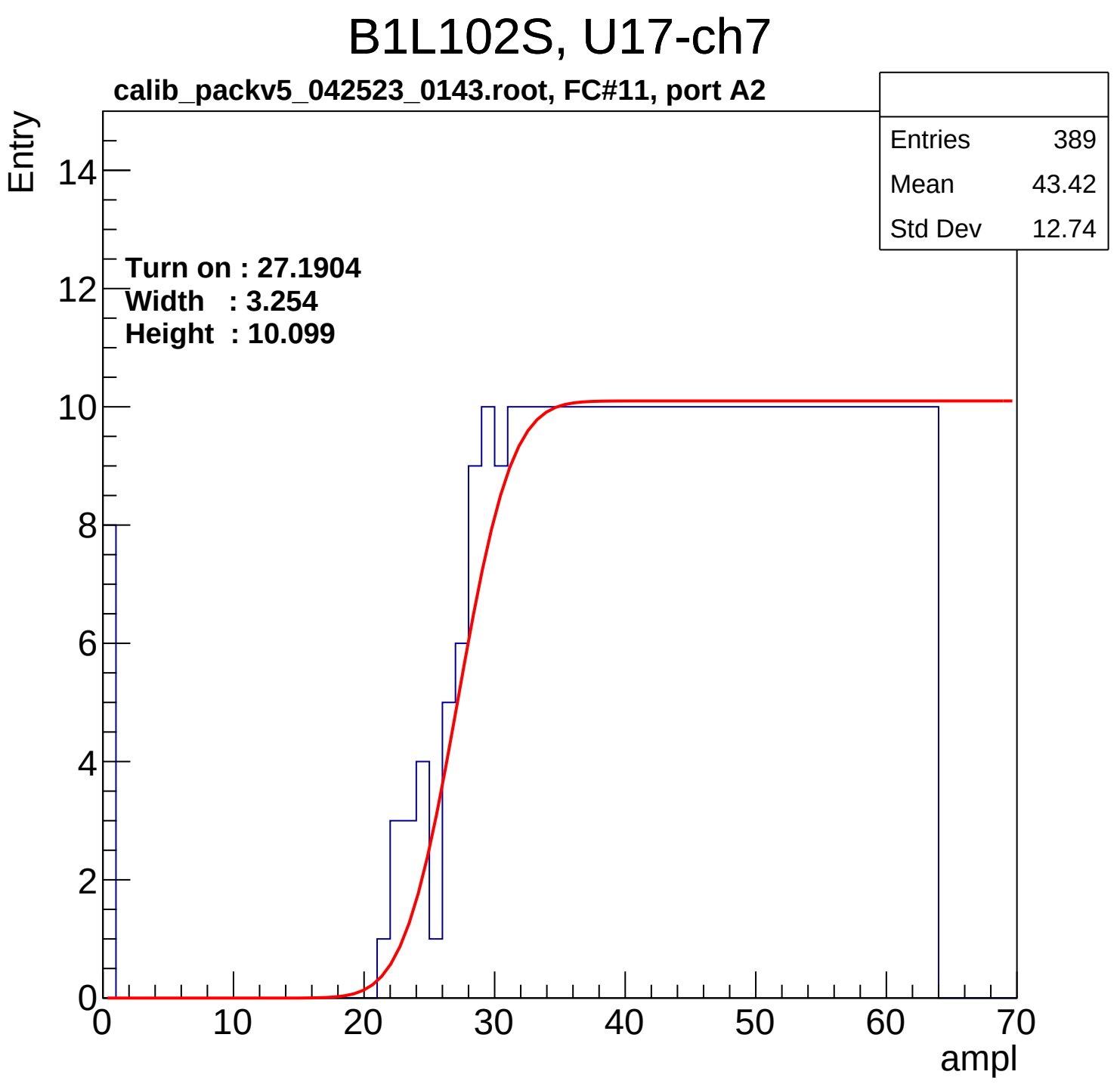
B1L102S, U17-ch7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 389
Mean 43.42
Std Dev 12.74
Turn on : 27.1904
Width : 3.254
Height : 10.099
Entry
ampl
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4
6
8
10
12
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0
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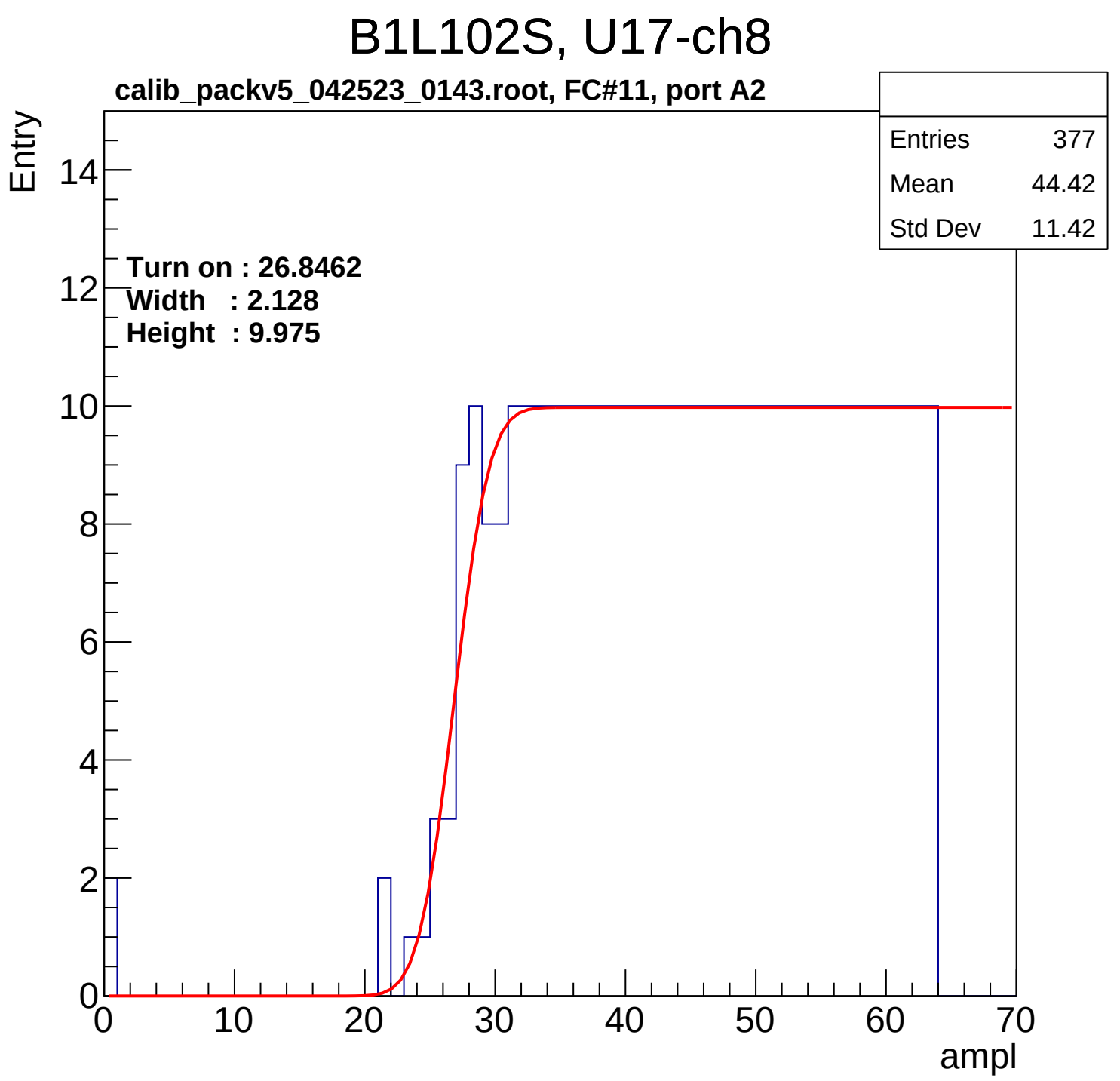
B1L102S, U17-ch8
calib_packv5_042523_0143.root, FC#11, port A2
Entries 377
Mean 44.42
Std Dev 11.42
Turn on : 26.8462
Width : 2.128
Height : 9.975
Entry
ampl
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6
8
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0
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60
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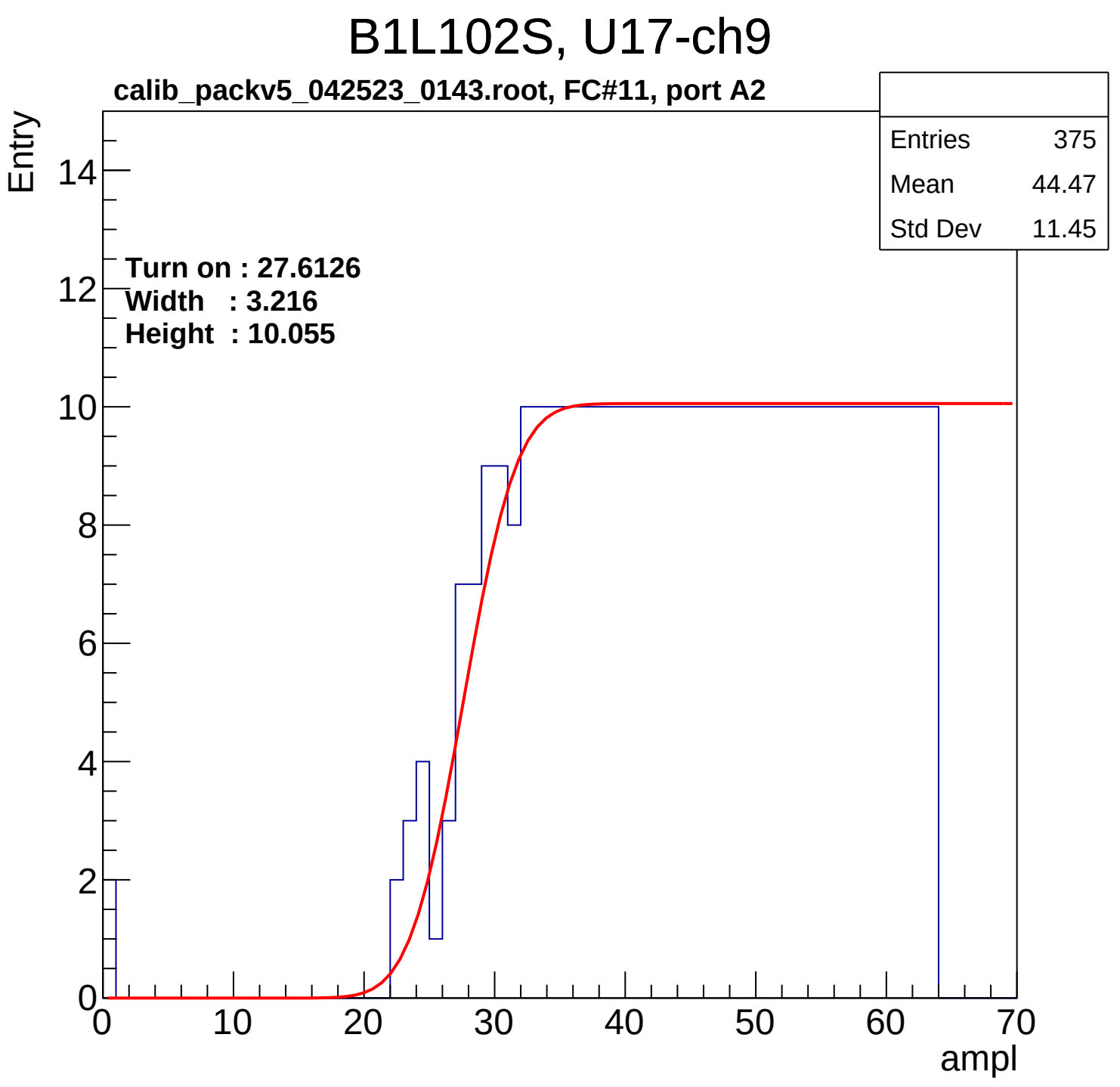
B1L102S, U17-ch9
calib_packv5_042523_0143.root, FC#11, port A2
Entries 375
Mean 44.47
Std Dev 11.45
Turn on : 27.6126
Width : 3.216
Height : 10.055
Entry
ampl
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6
8
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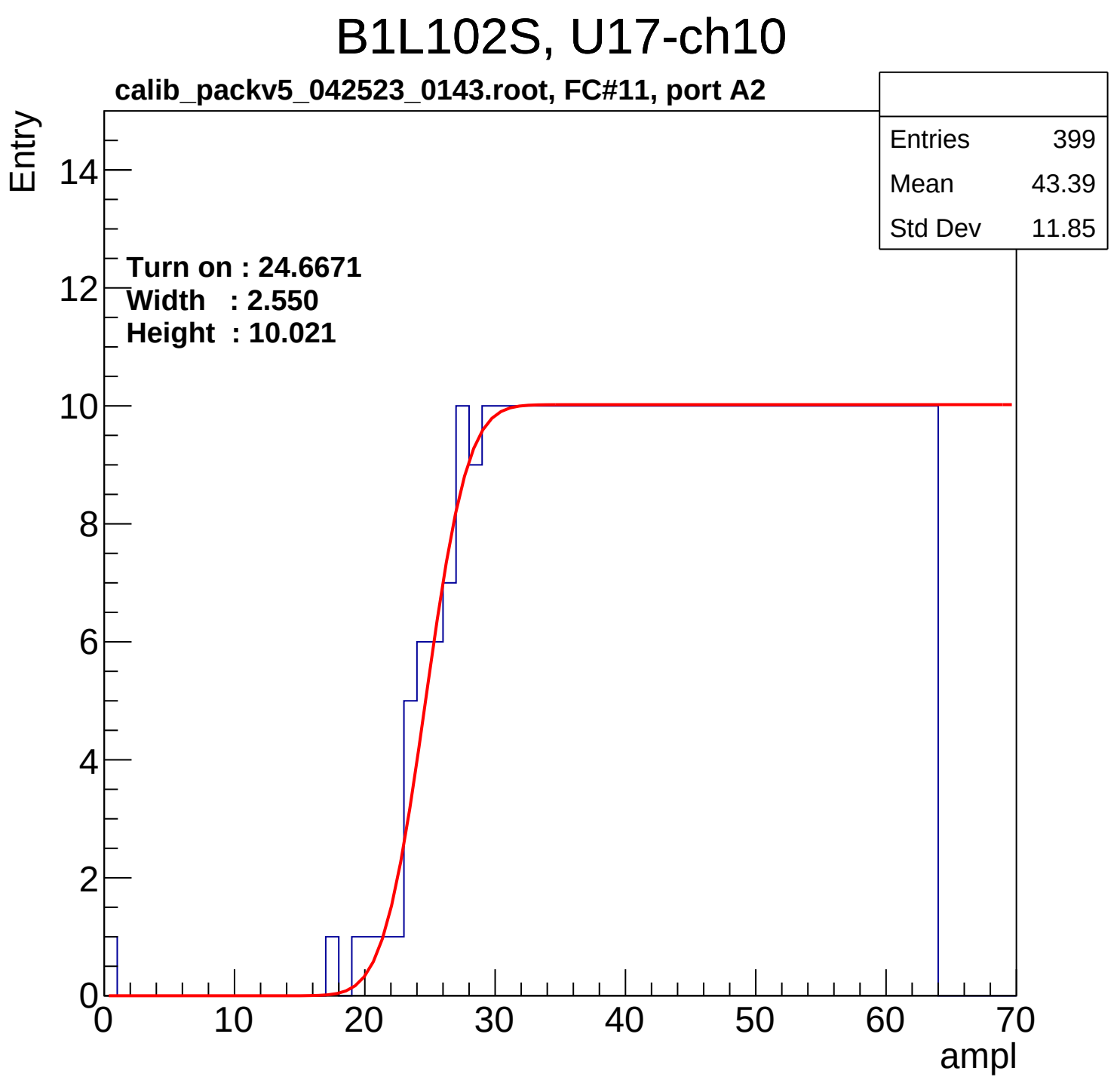
B1L102S, U17-ch10
calib_packv5_042523_0143.root, FC#11, port A2
Entries 399
Mean 43.39
Std Dev 11.85
Turn on : 24.6671
Width : 2.550
Height : 10.021
Entry
ampl
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6
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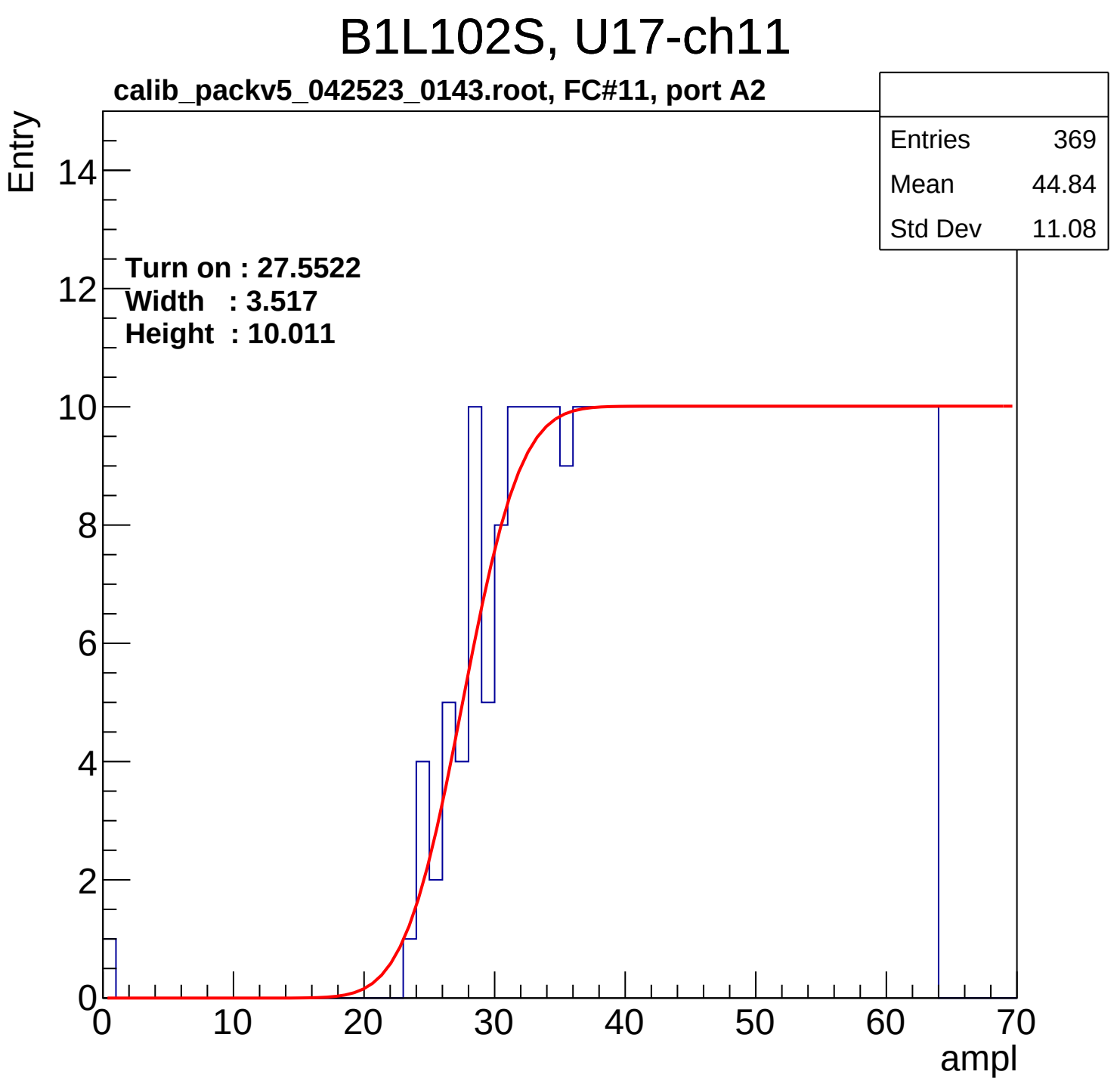
B1L102S, U17-ch11
calib_packv5_042523_0143.root, FC#11, port A2
Entries 369
Mean 44.84
Std Dev 11.08
Turn on : 27.5522
Width : 3.517
Height : 10.011
Entry
ampl
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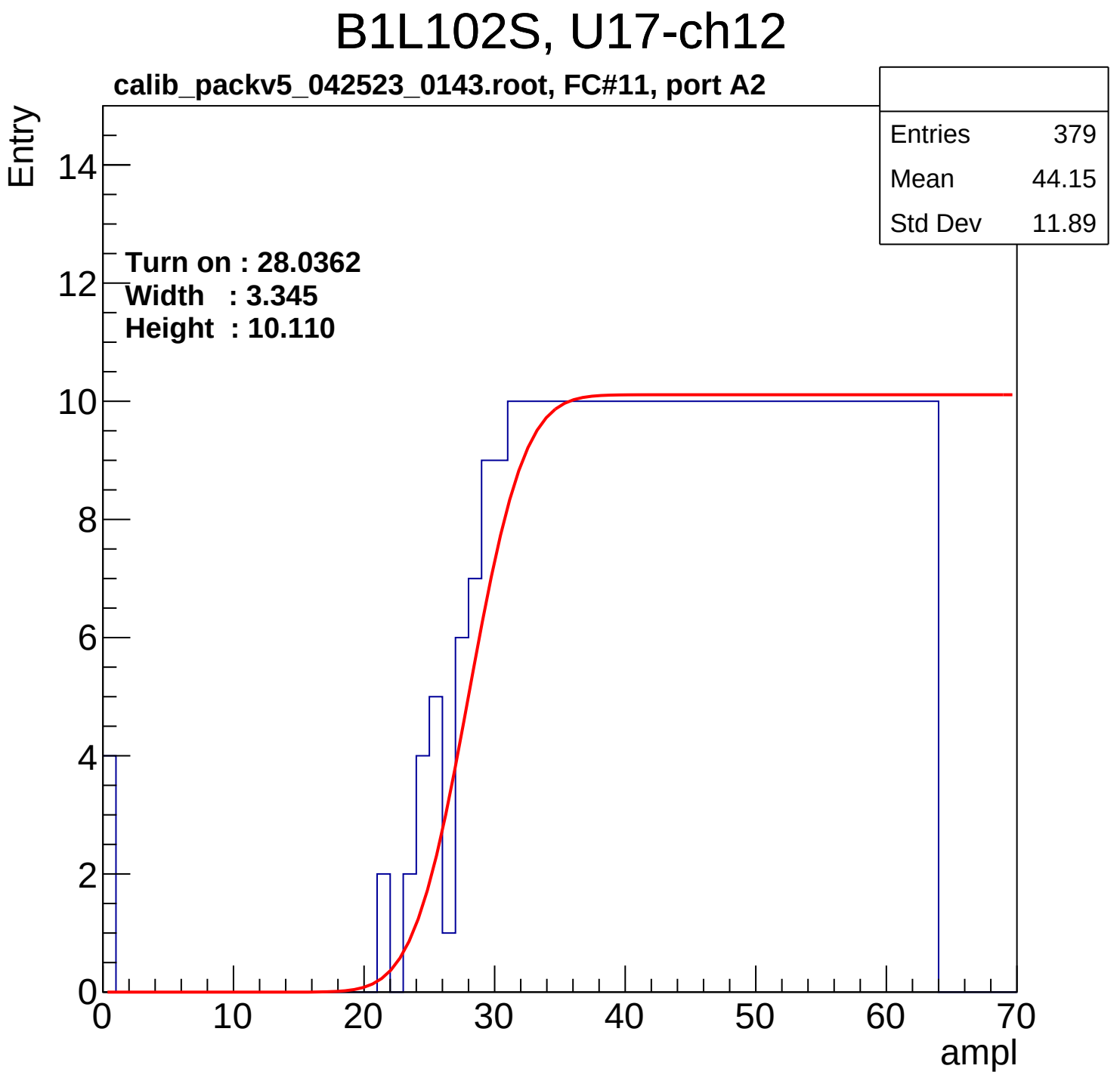
B1L102S, U17-ch12
calib_packv5_042523_0143.root, FC#11, port A2
Entries 379
Mean 44.15
Std Dev 11.89
Turn on : 28.0362
Width : 3.345
Height : 10.110
Entry
ampl
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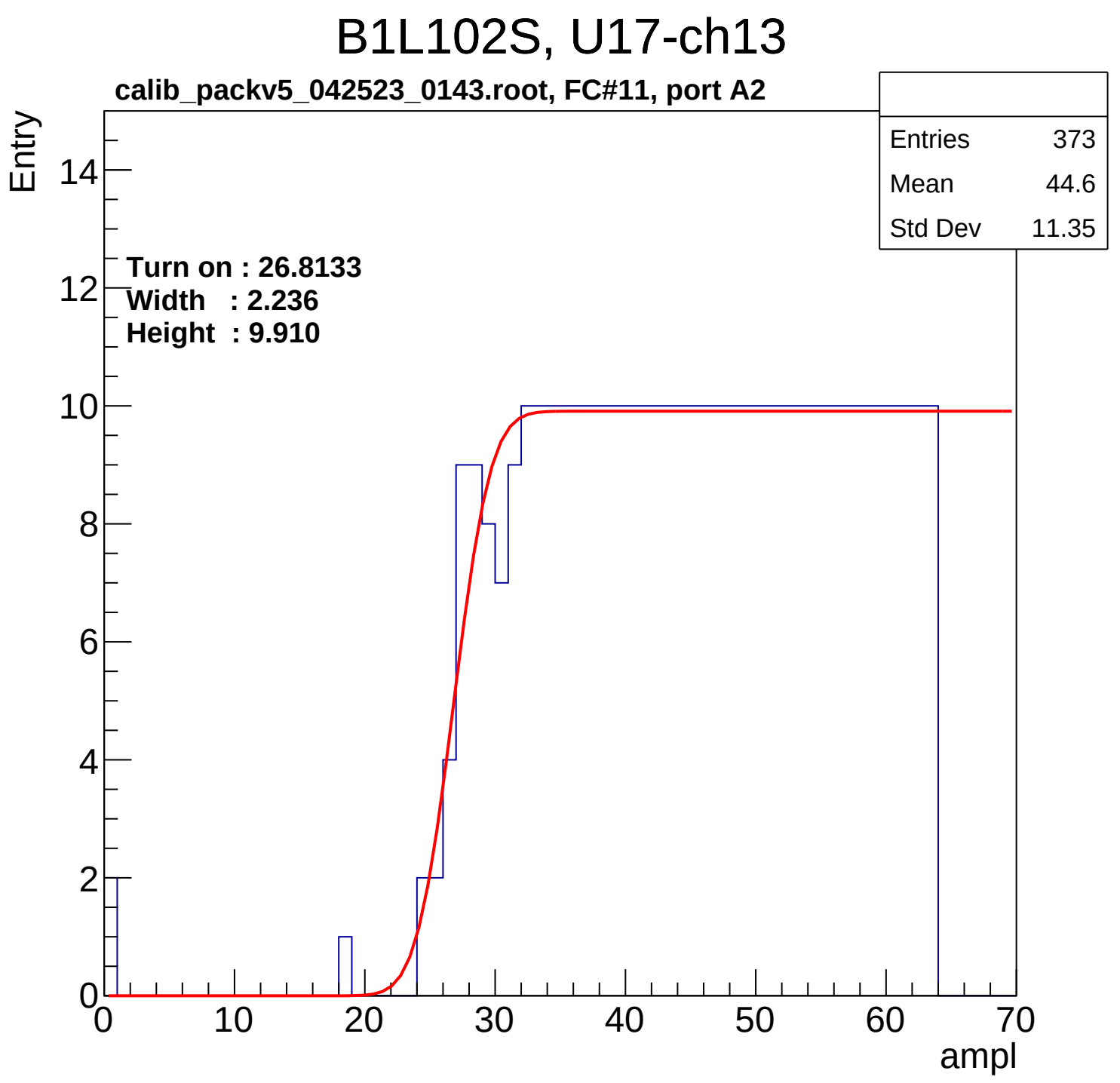
B1L102S, U17-ch13
calib_packv5_042523_0143.root, FC#11, port A2
Entries 373
Mean 44.6
Std Dev 11.35
Turn on : 26.8133
Width : 2.236
Height : 9.910
Entry
ampl
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4
6
8
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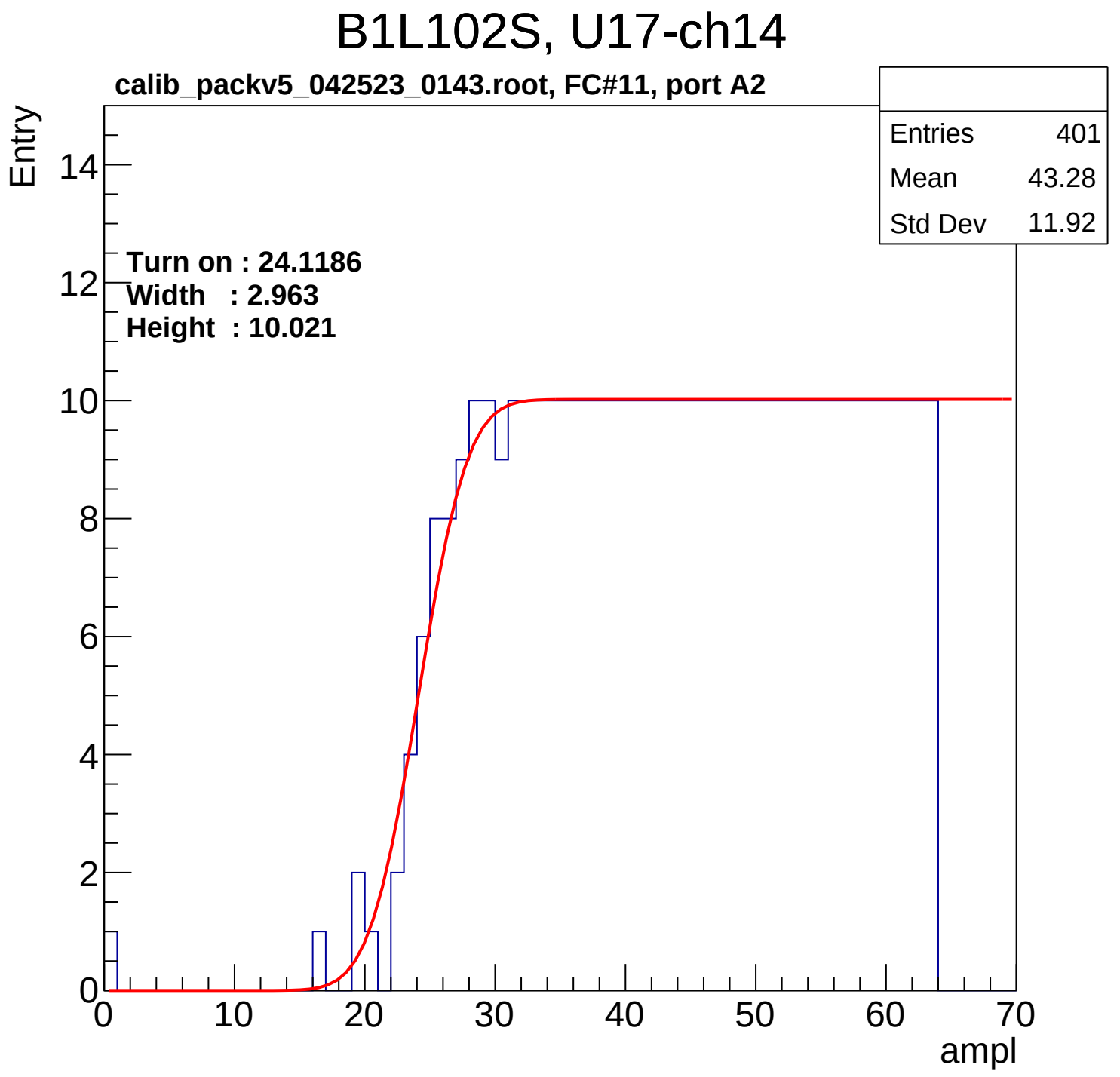
B1L102S, U17-ch14
calib_packv5_042523_0143.root, FC#11, port A2
Entries 401
Mean 43.28
Std Dev 11.92
Turn on : 24.1186
Width : 2.963
Height : 10.021
Entry
ampl
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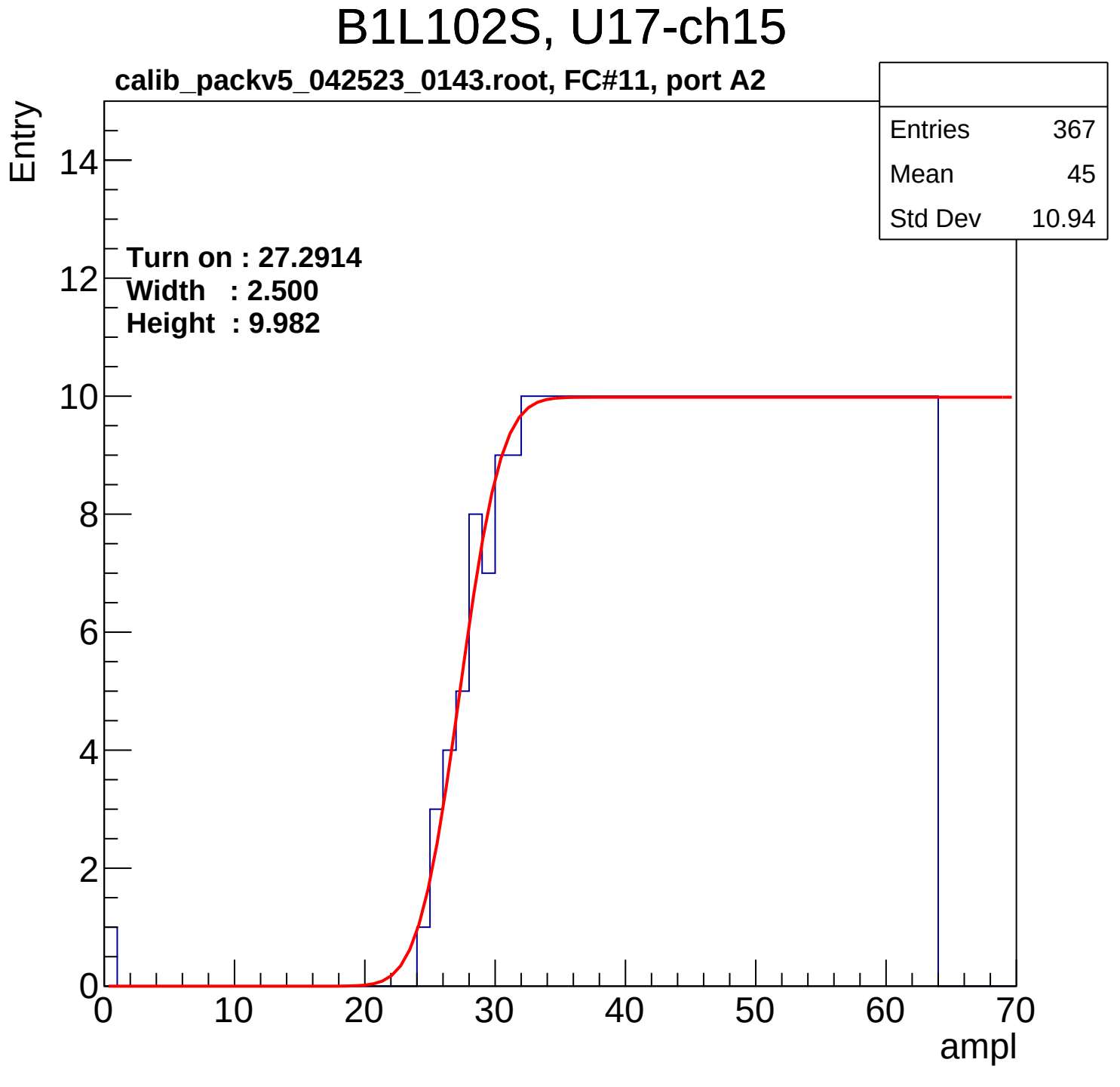
B1L102S, U17-ch15
calib_packv5_042523_0143.root, FC#11, port A2
Entries 367
Mean 45
Std Dev 10.94
Turn on : 27.2914
Width : 2.500
Height : 9.982
Entry
ampl
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2
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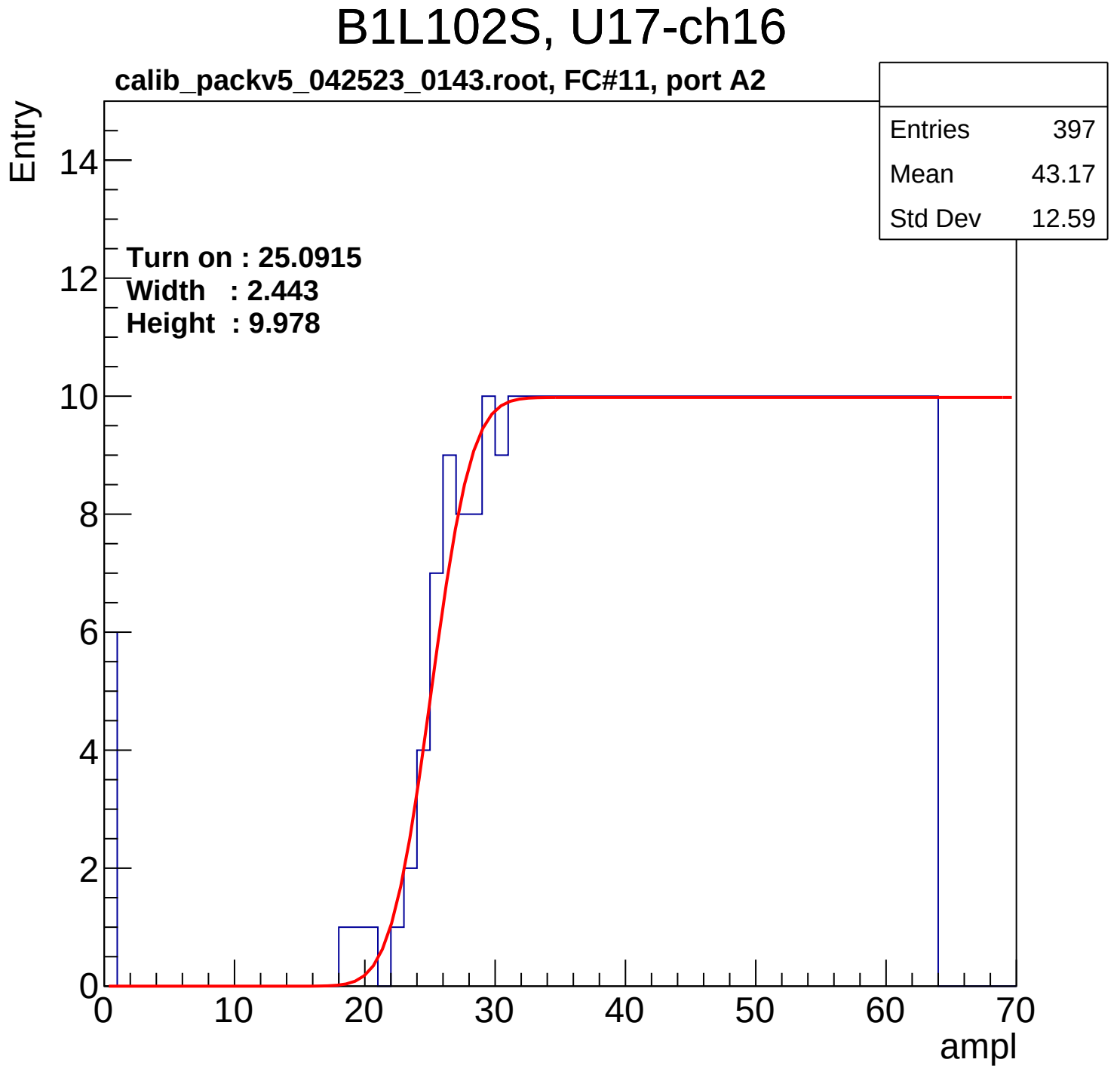
B1L102S, U17-ch16
calib_packv5_042523_0143.root, FC#11, port A2
Entries 397
Mean 43.17
Std Dev 12.59
Turn on : 25.0915
Width : 2.443
Height : 9.978
Entry
ampl
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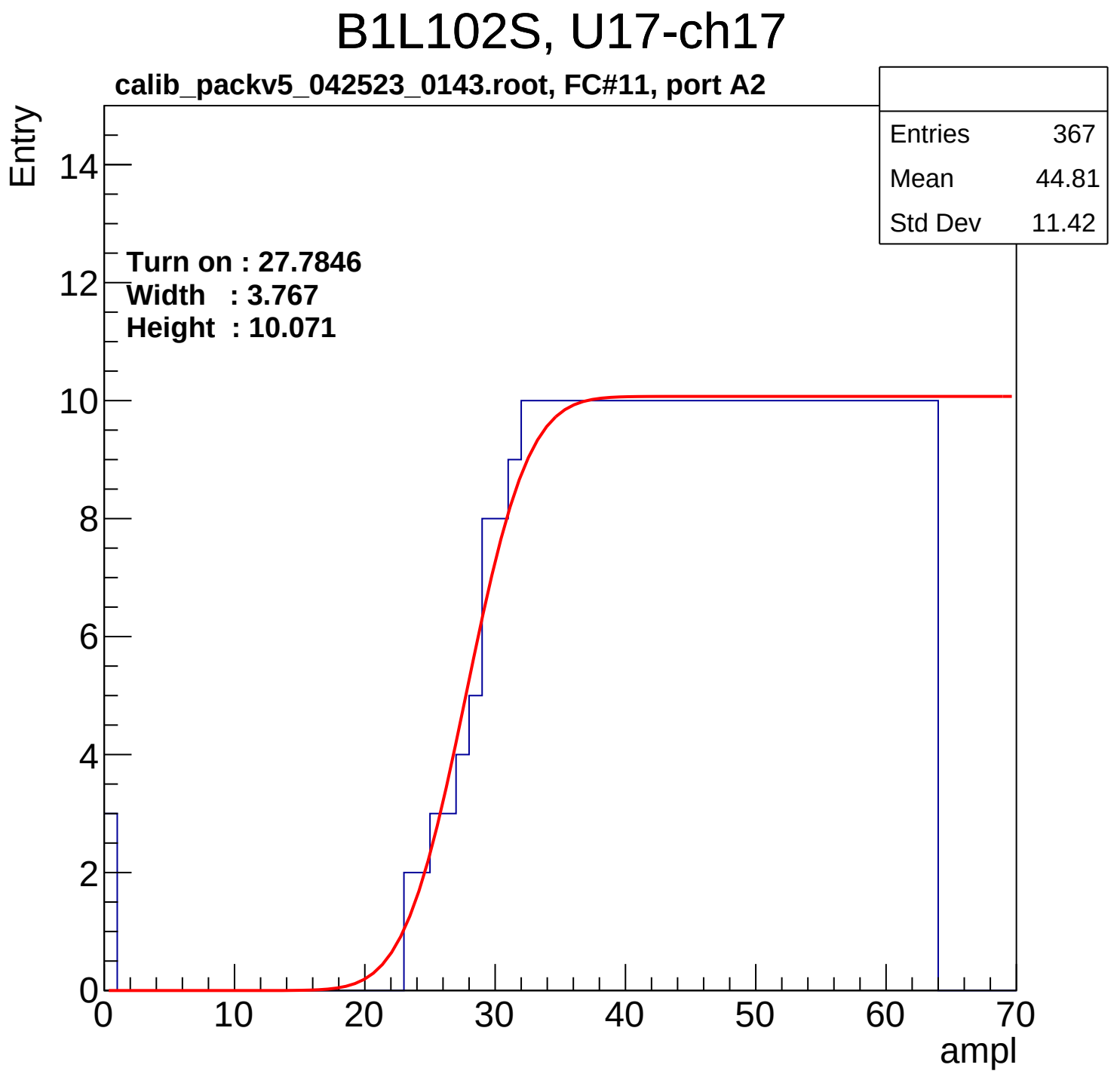
B1L102S, U17-ch17
calib_packv5_042523_0143.root, FC#11, port A2
Entries 367
Mean 44.81
Std Dev 11.42
Turn on : 27.7846
Width : 3.767
Height : 10.071
Entry
ampl
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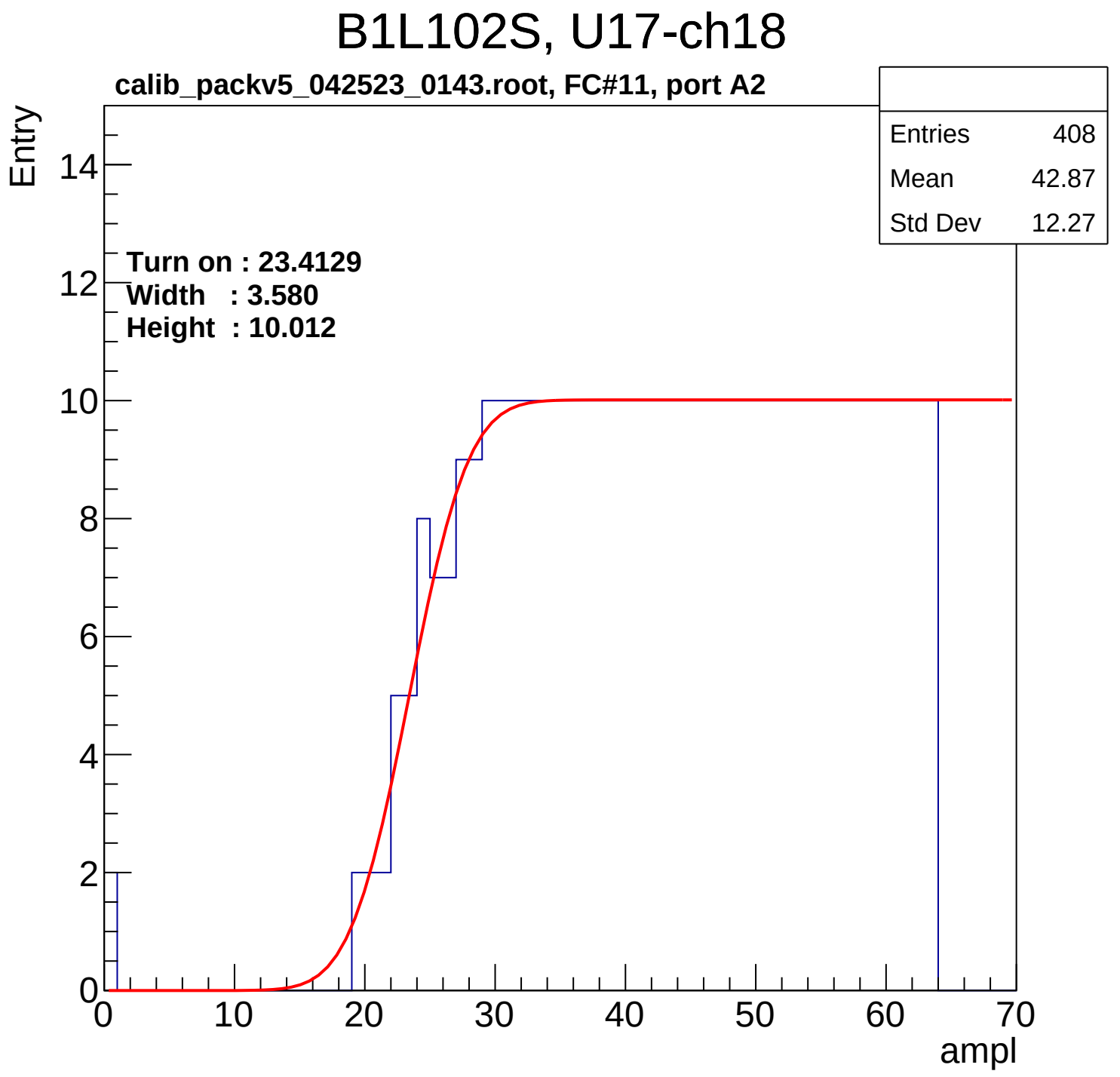
B1L102S, U17-ch18
calib_packv5_042523_0143.root, FC#11, port A2
Entries 408
Mean 42.87
Std Dev 12.27
Turn on : 23.4129
Width : 3.580
Height : 10.012
Entry
ampl
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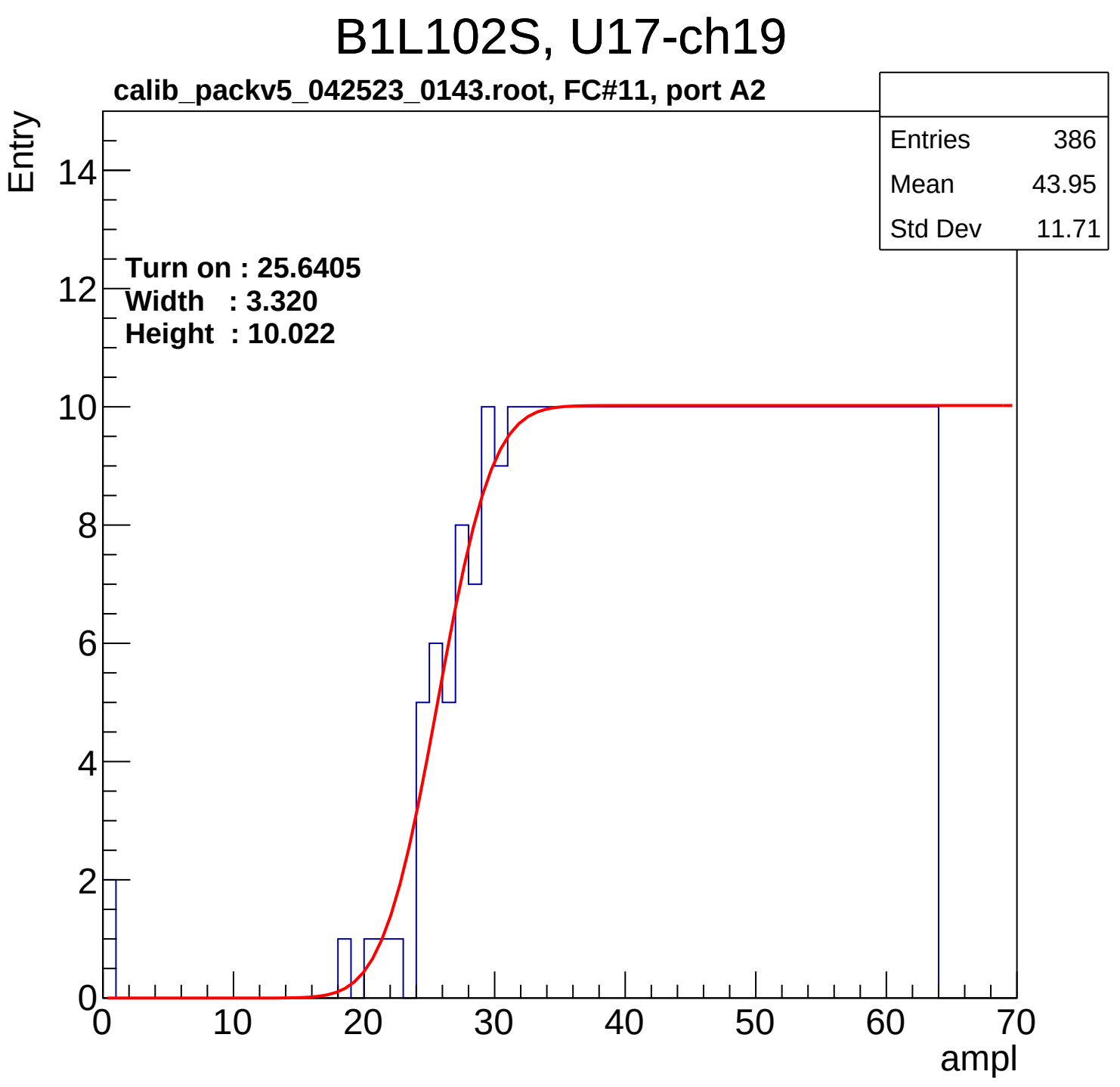
B1L102S, U17-ch19
calib_packv5_042523_0143.root, FC#11, port A2
Entries 386
Mean 43.95
Std Dev 11.71
Turn on : 25.6405
Width : 3.320
Height : 10.022
Entry
ampl
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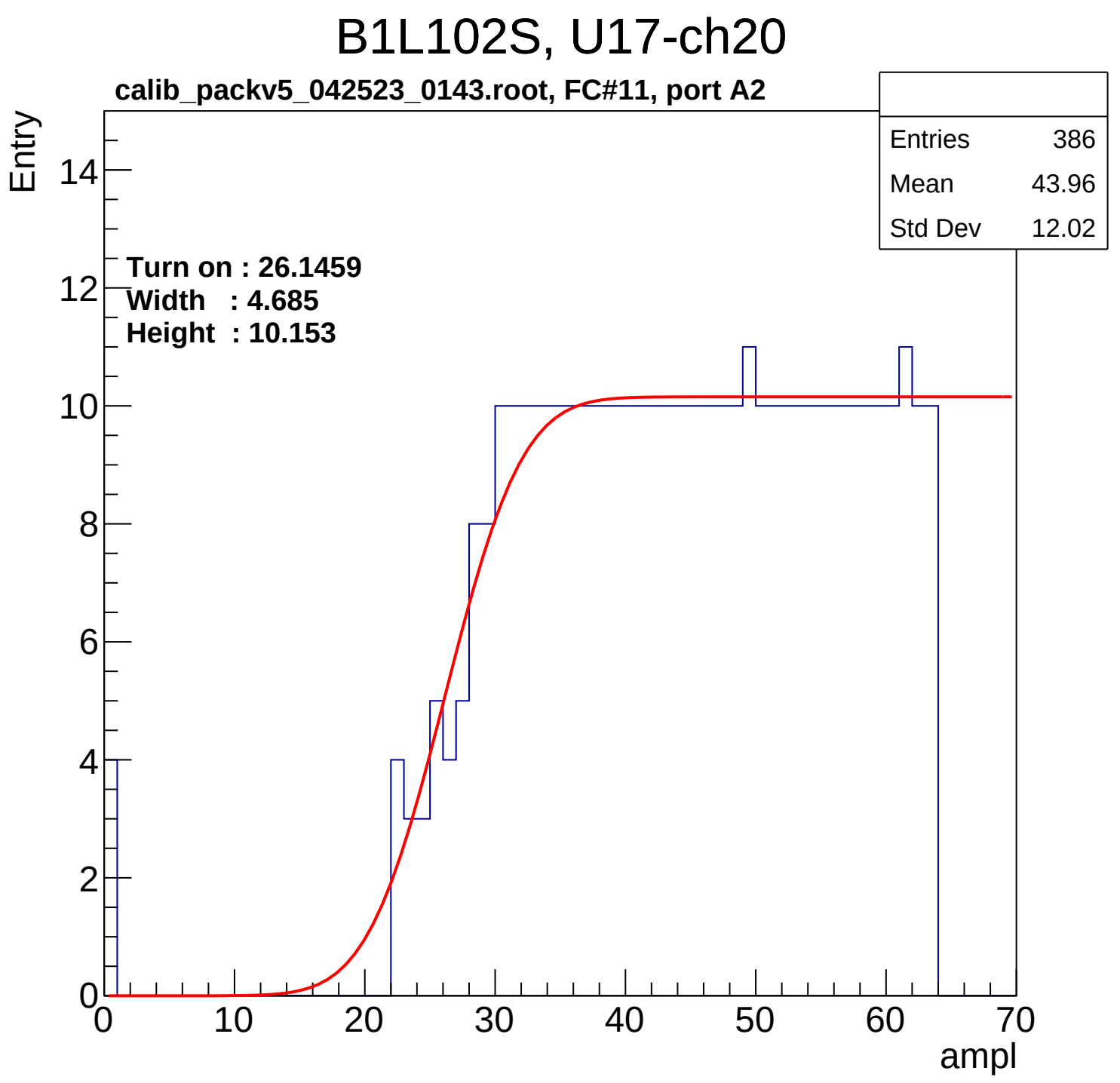
B1L102S, U17-ch20
calib_packv5_042523_0143.root, FC#11, port A2
Entries 386
Mean 43.96
Std Dev 12.02
Turn on : 26.1459
Width : 4.685
Height : 10.153
Entry
ampl
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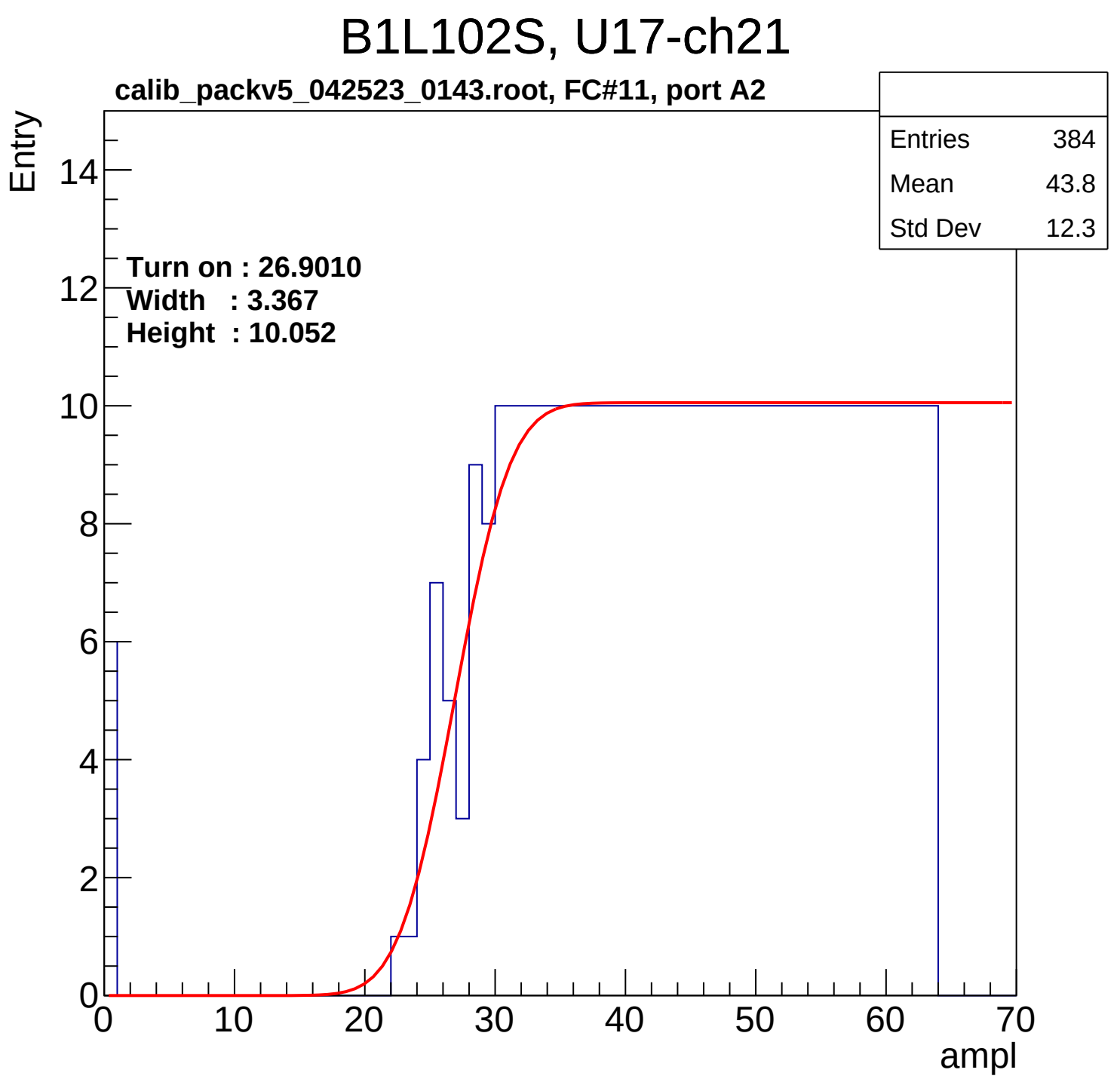
B1L102S, U17-ch21
calib_packv5_042523_0143.root, FC#11, port A2
Entries 384
Mean 43.8
Std Dev 12.3
Turn on : 26.9010
Width : 3.367
Height : 10.052
Entry
ampl
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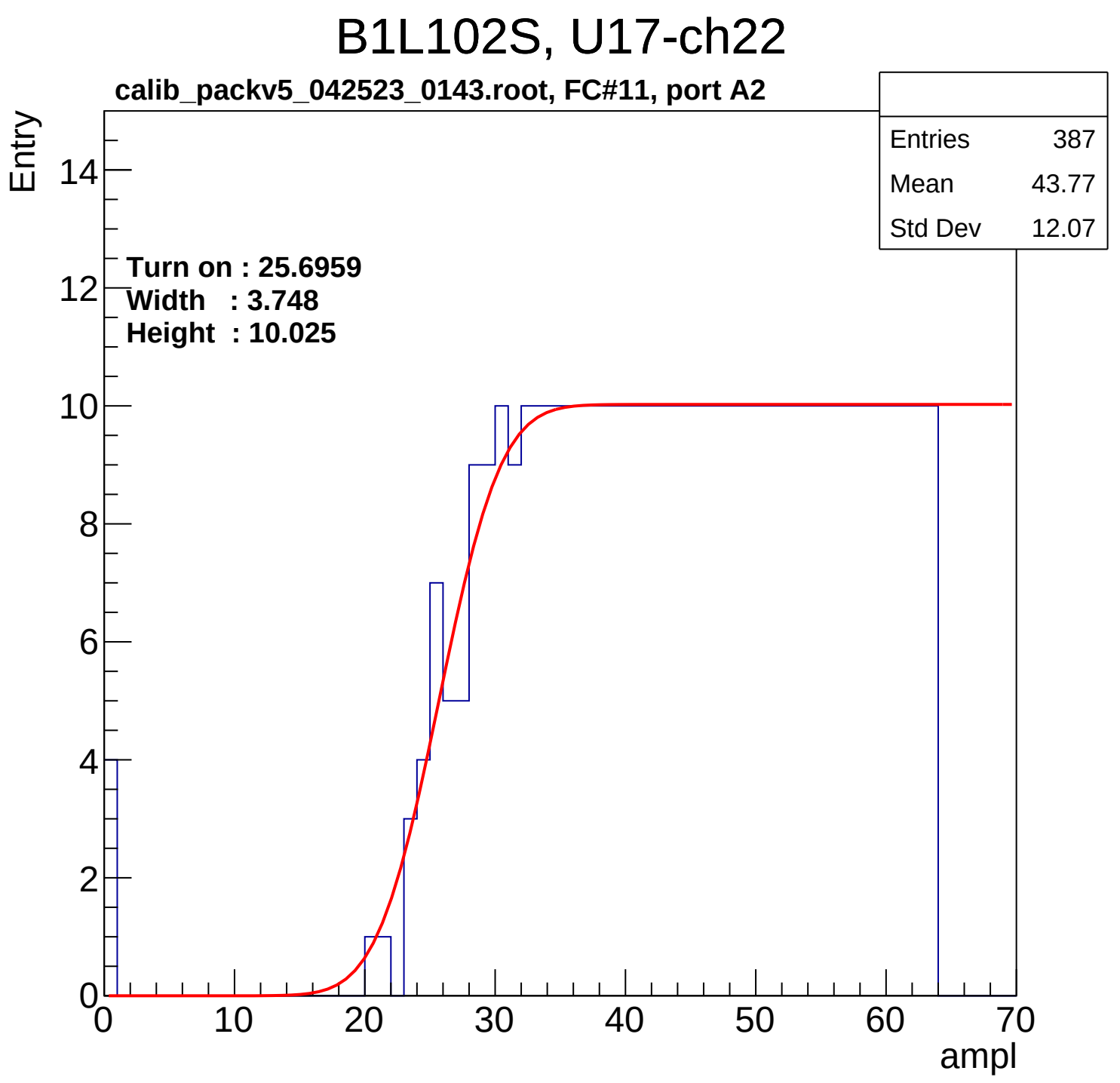
B1L102S, U17-ch22
calib_packv5_042523_0143.root, FC#11, port A2
Entries 387
Mean 43.77
Std Dev 12.07
Turn on : 25.6959
Width : 3.748
Height : 10.025
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ampl
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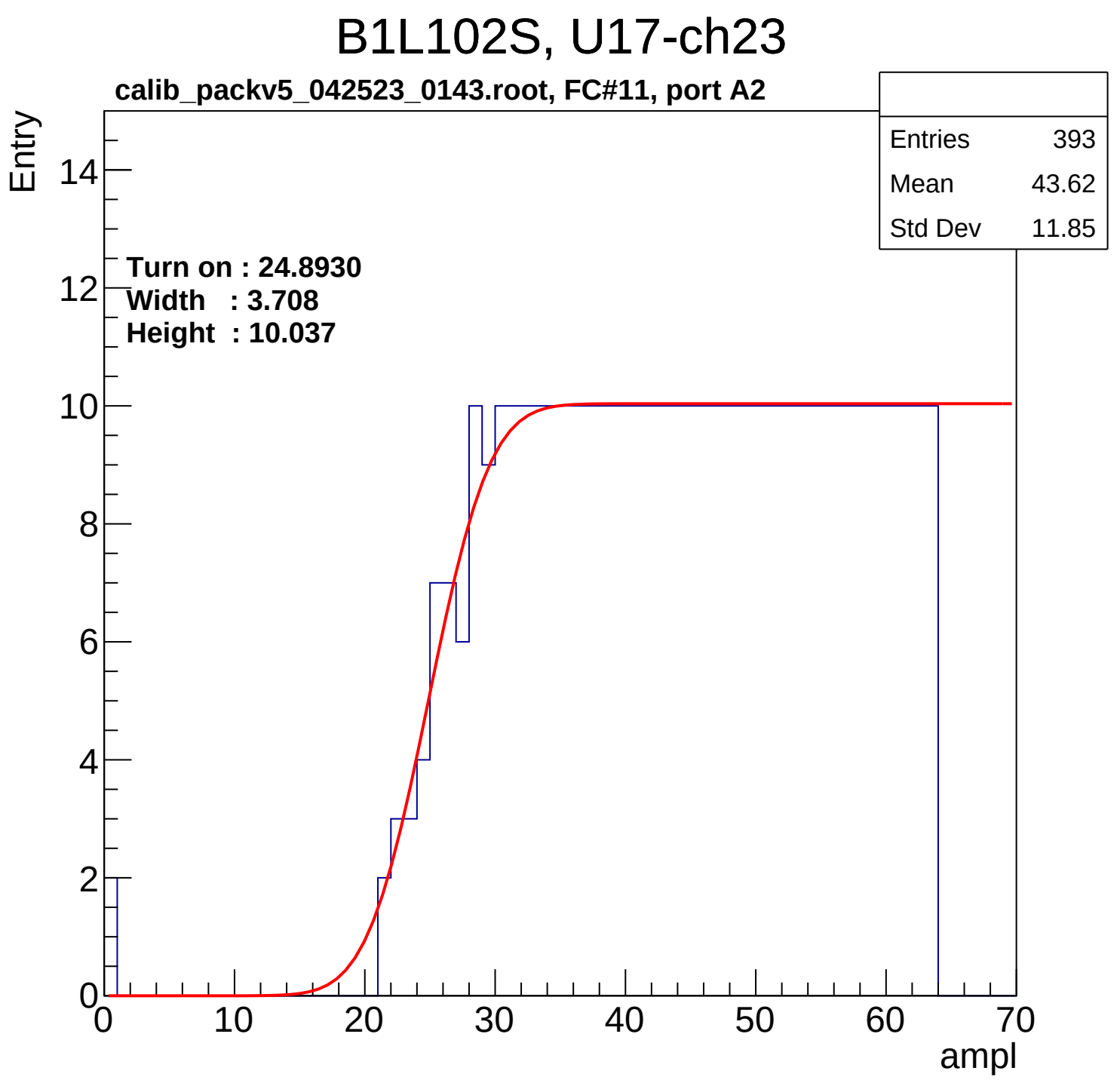
B1L102S, U17-ch23
calib_packv5_042523_0143.root, FC#11, port A2
Entries 393
Mean 43.62
Std Dev 11.85
Turn on : 24.8930
Width : 3.708
Height : 10.037
Entry
ampl
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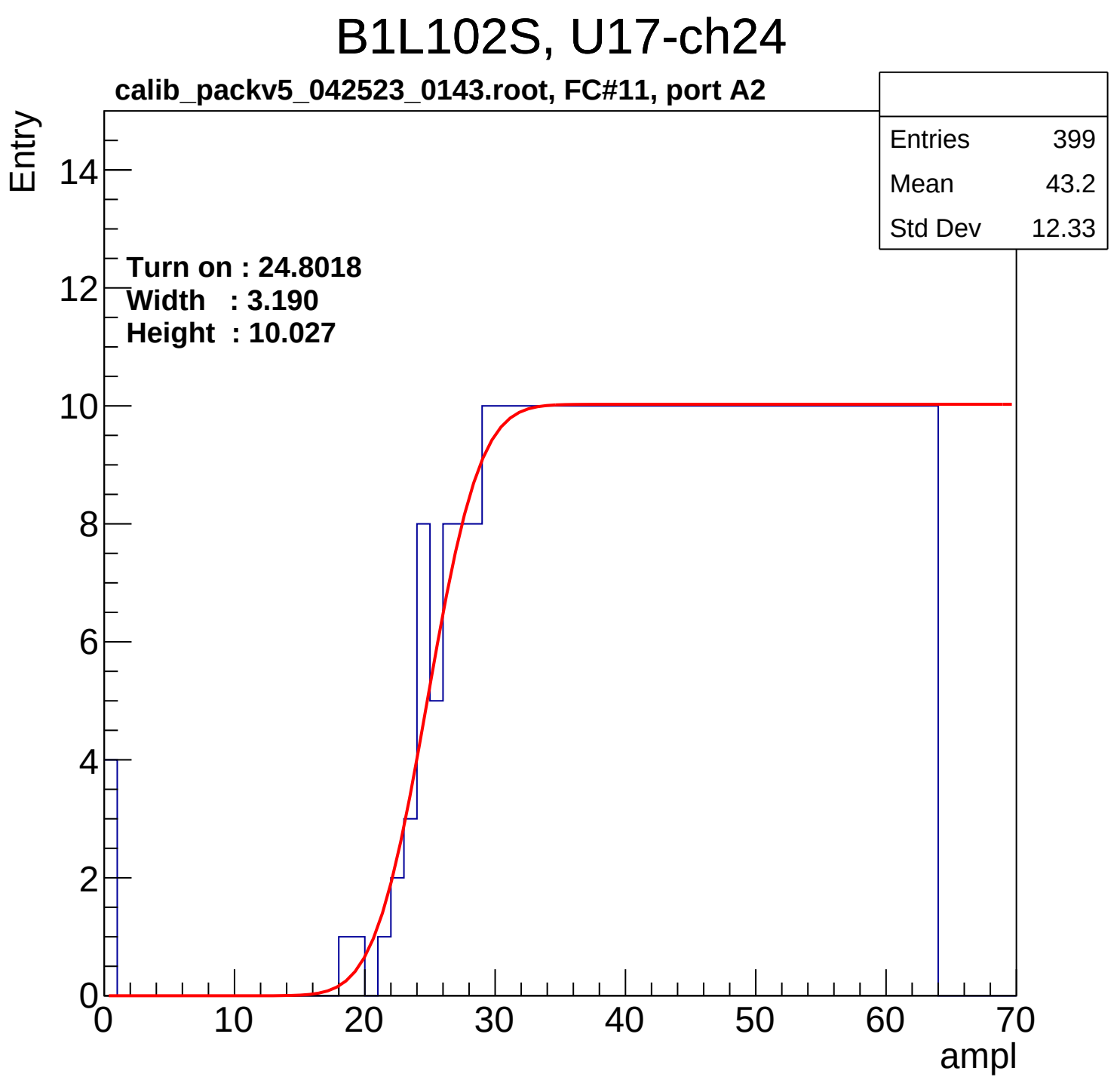
B1L102S, U17-ch24
calib_packv5_042523_0143.root, FC#11, port A2
Entries 399
Mean 43.2
Std Dev 12.33
Turn on : 24.8018
Width : 3.190
Height : 10.027
Entry
ampl
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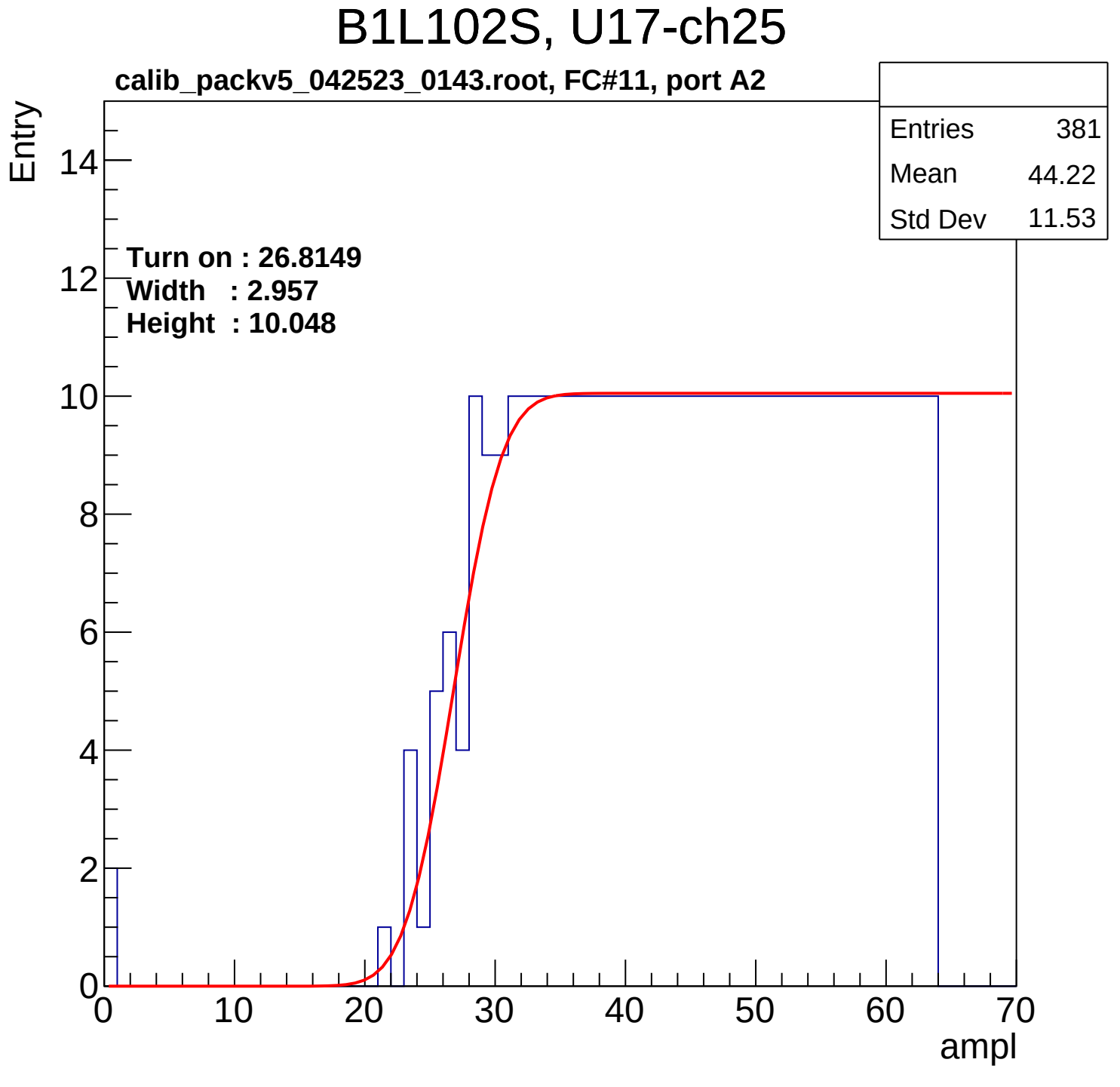
B1L102S, U17-ch25
calib_packv5_042523_0143.root, FC#11, port A2
Entries 381
Mean 44.22
Std Dev 11.53
Turn on : 26.8149
Width : 2.957
Height : 10.048
Entry
ampl
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6
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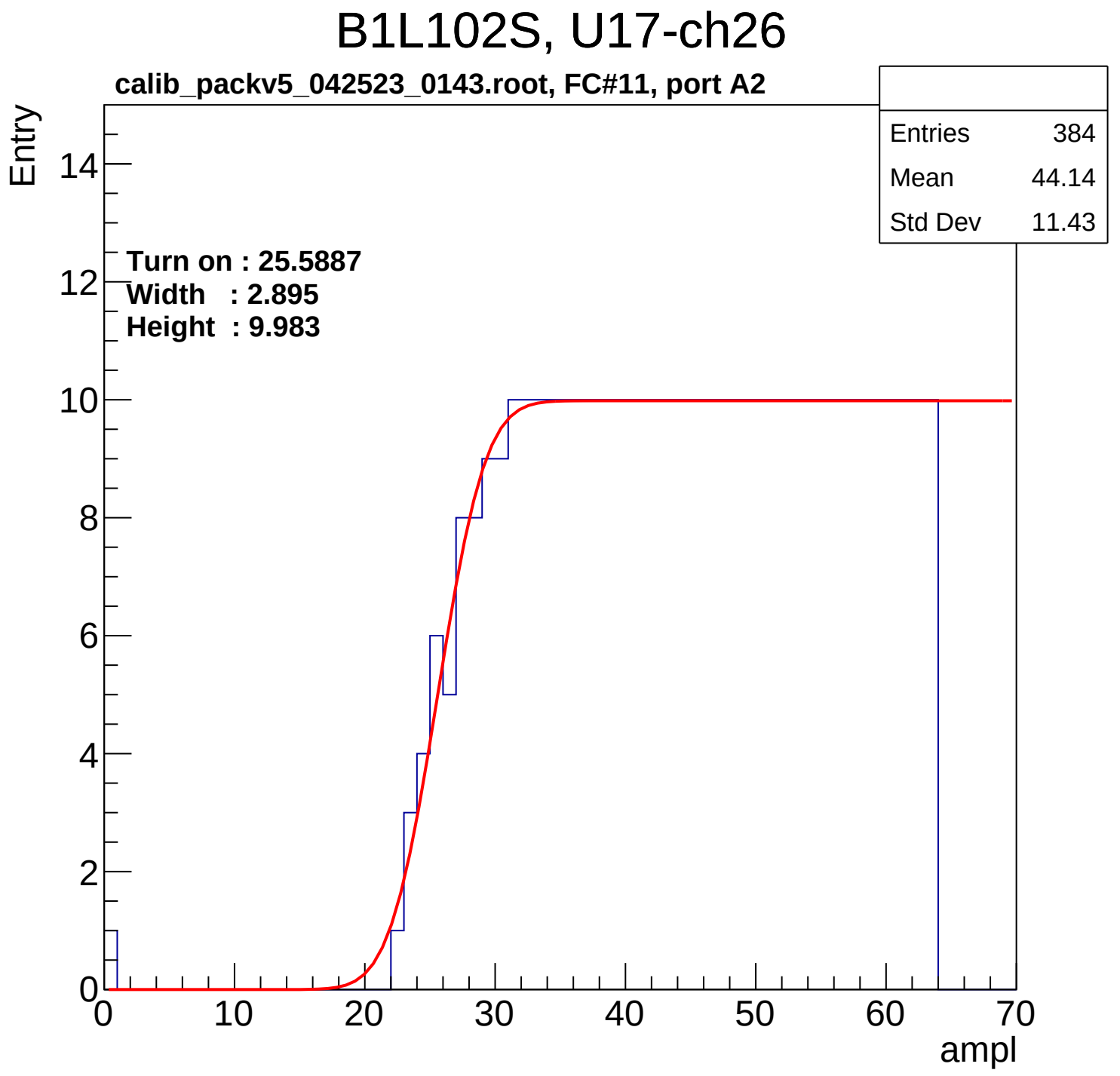
B1L102S, U17-ch26
calib_packv5_042523_0143.root, FC#11, port A2
Entries 384
Mean 44.14
Std Dev 11.43
Turn on : 25.5887
Width : 2.895
Height : 9.983
Entry
ampl
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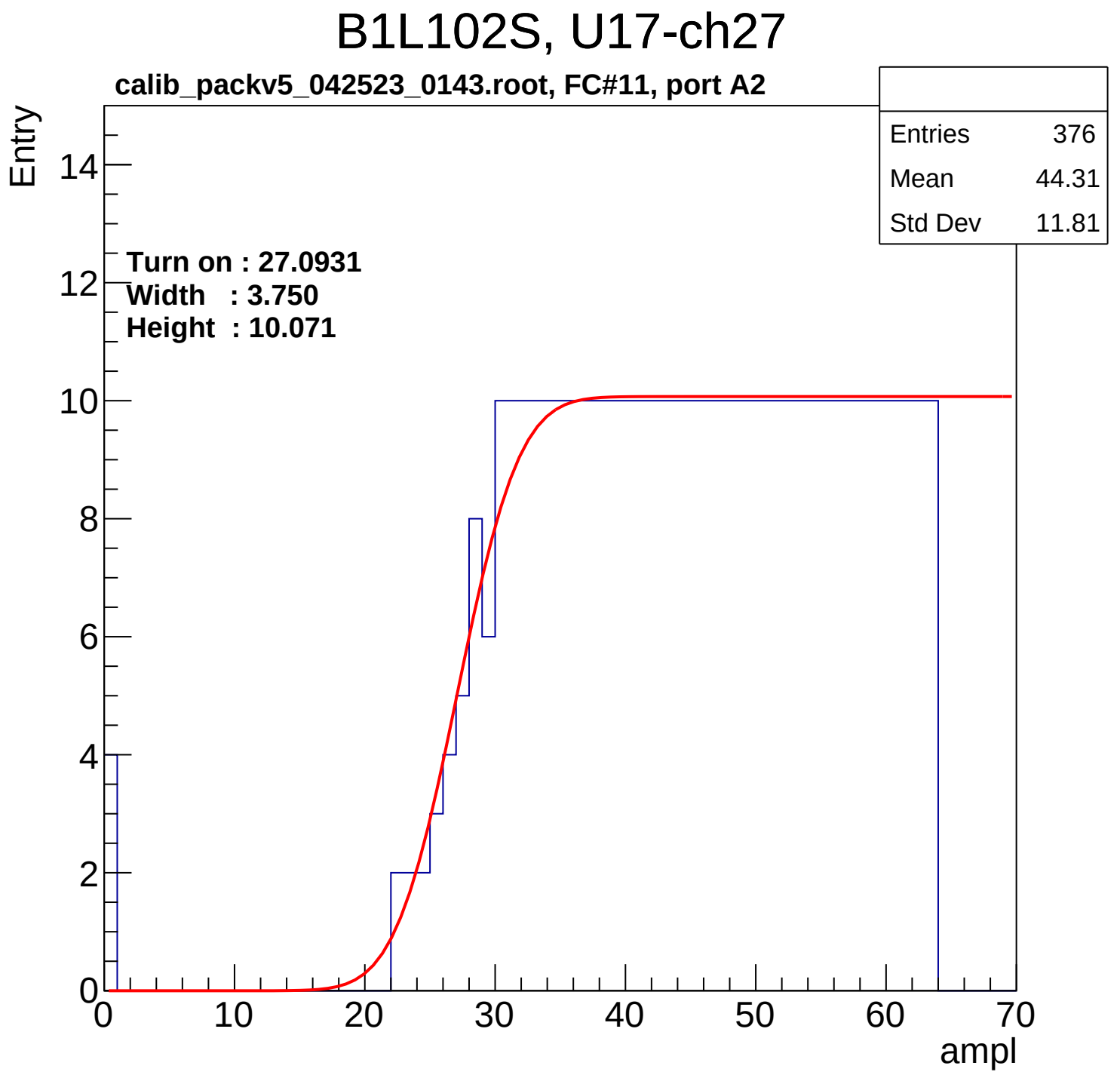
B1L102S, U17-ch27
calib_packv5_042523_0143.root, FC#11, port A2
Entries 376
Mean 44.31
Std Dev 11.81
Turn on : 27.0931
Width : 3.750
Height : 10.071
Entry
ampl
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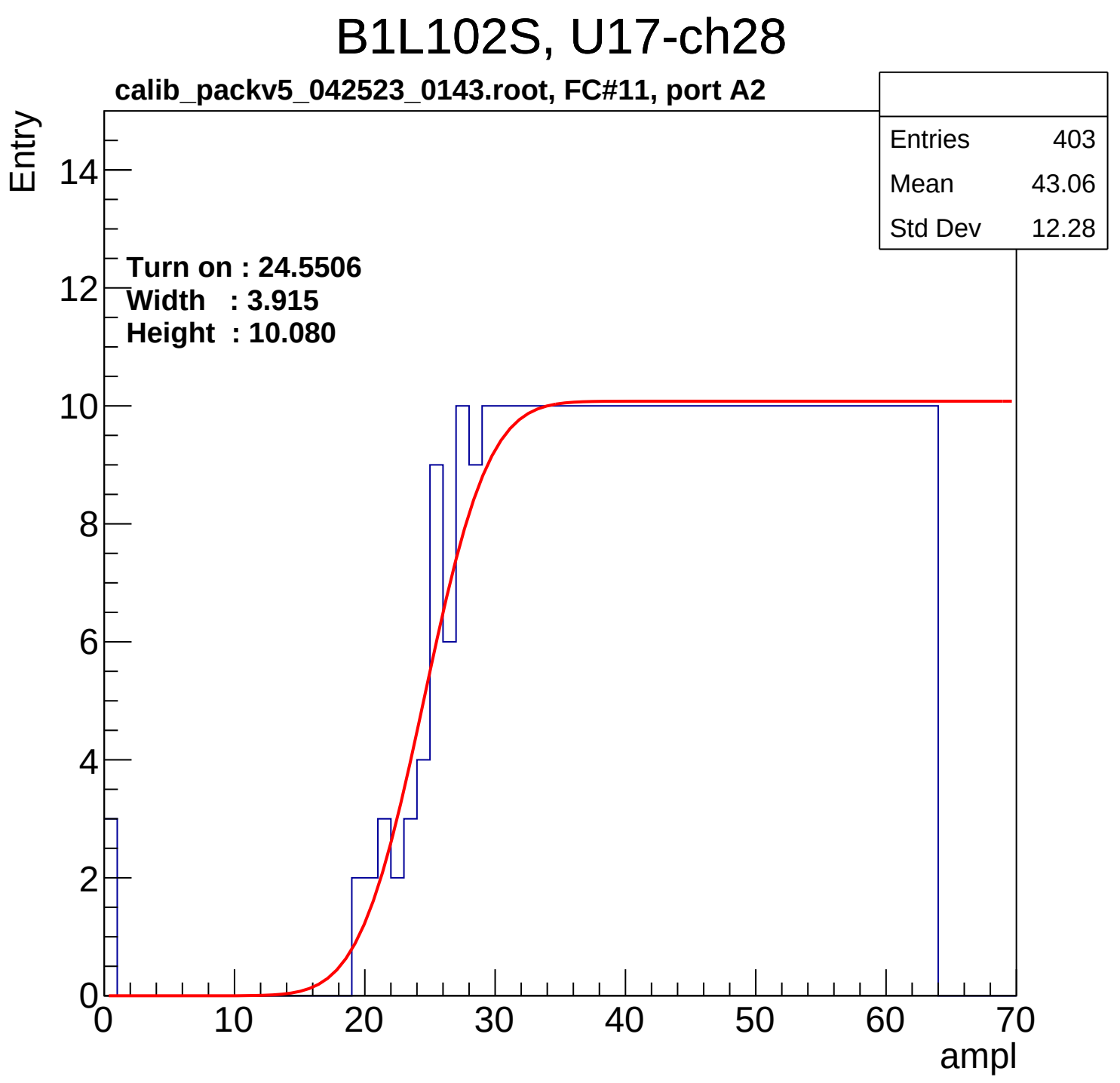
B1L102S, U17-ch28
calib_packv5_042523_0143.root, FC#11, port A2
Entries 403
Mean 43.06
Std Dev 12.28
Turn on : 24.5506
Width : 3.915
Height : 10.080
Entry
ampl
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4
6
8
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12
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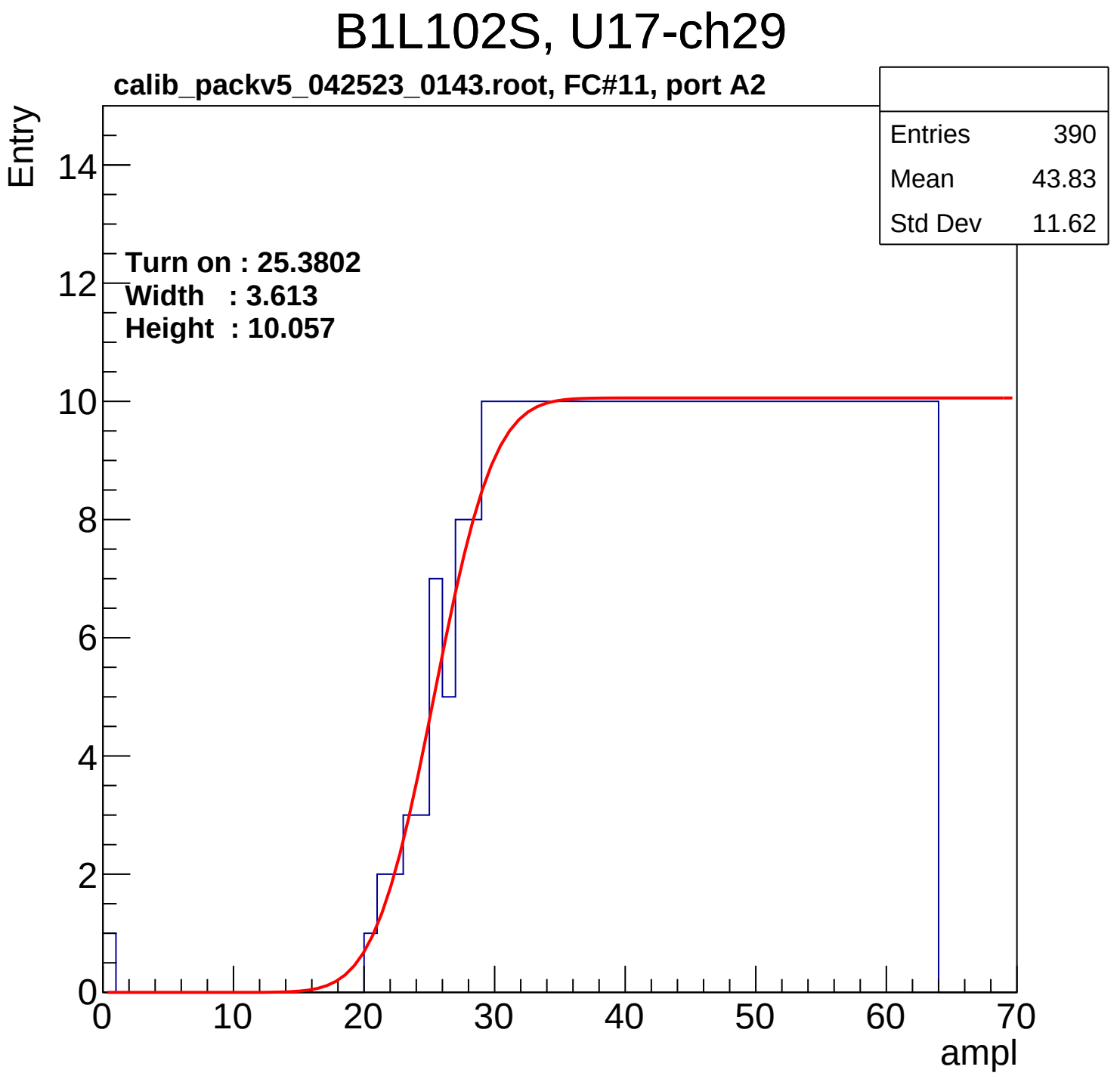
B1L102S, U17-ch29
calib_packv5_042523_0143.root, FC#11, port A2
Entries 390
Mean 43.83
Std Dev 11.62
Turn on : 25.3802
Width : 3.613
Height : 10.057
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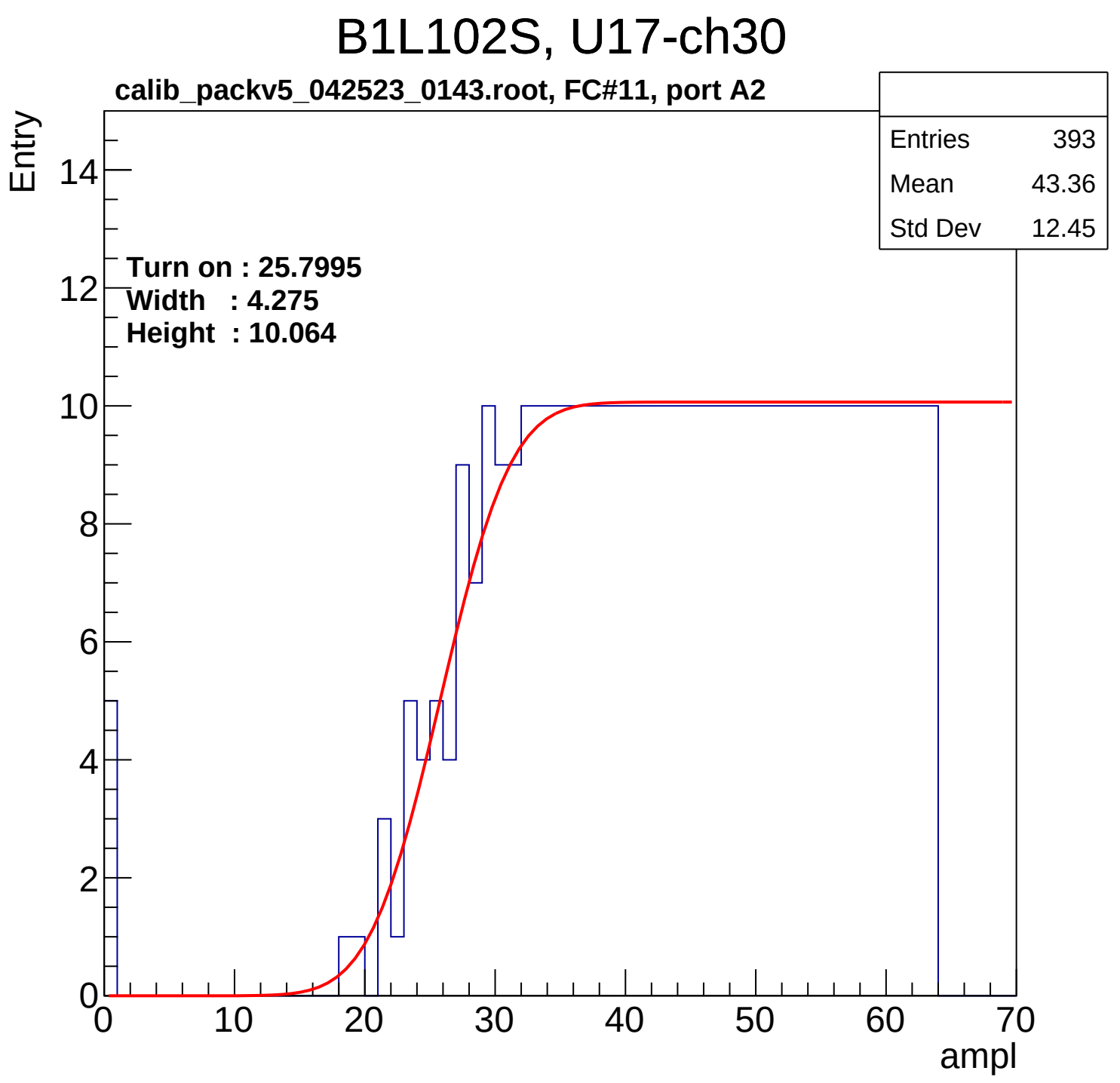
B1L102S, U17-ch30
calib_packv5_042523_0143.root, FC#11, port A2
Entries 393
Mean 43.36
Std Dev 12.45
Turn on : 25.7995
Width : 4.275
Height : 10.064
Entry
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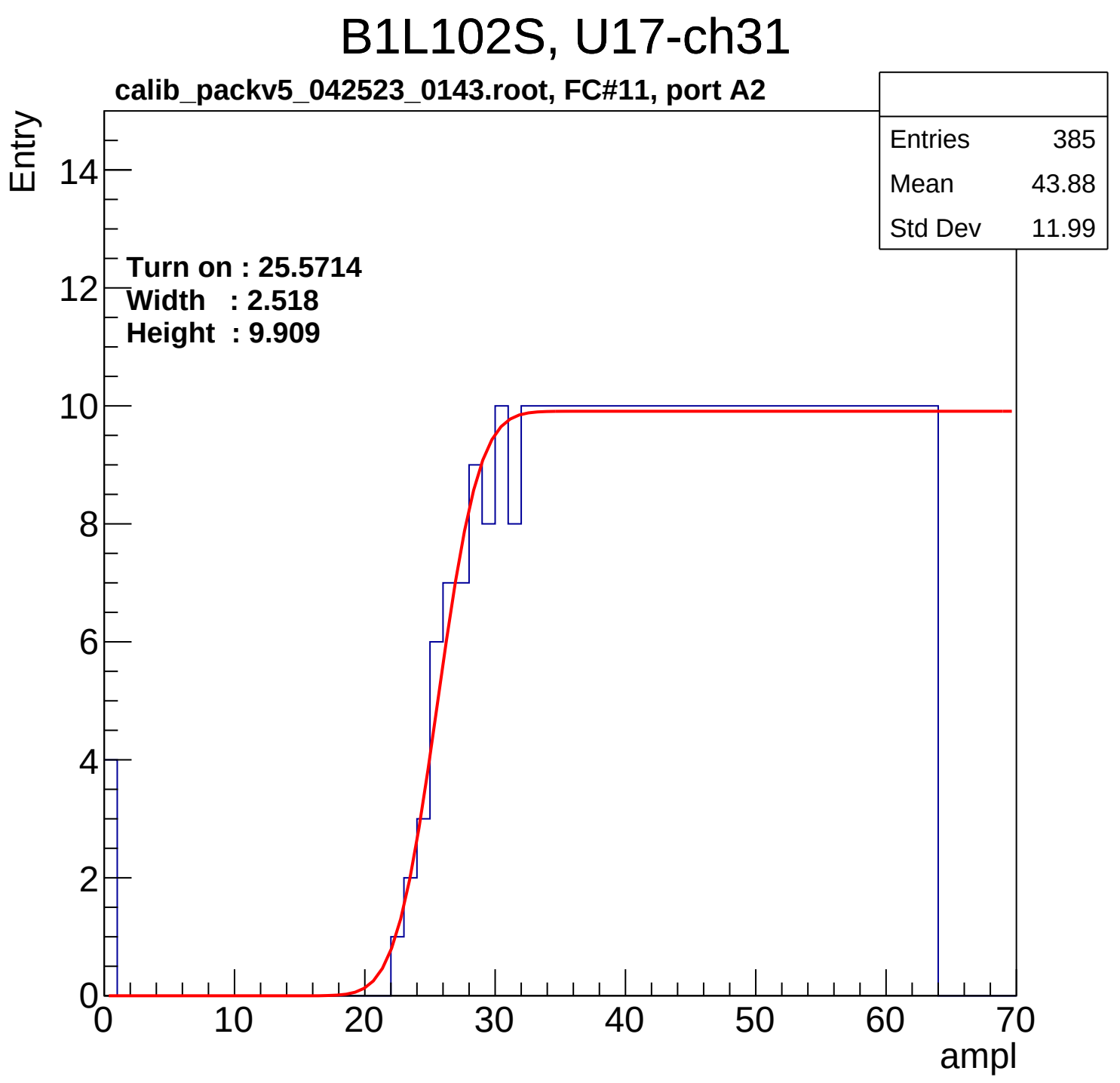
B1L102S, U17-ch31
calib_packv5_042523_0143.root, FC#11, port A2
Entries 385
Mean 43.88
Std Dev 11.99
Turn on : 25.5714
Width : 2.518
Height : 9.909
Entry
ampl
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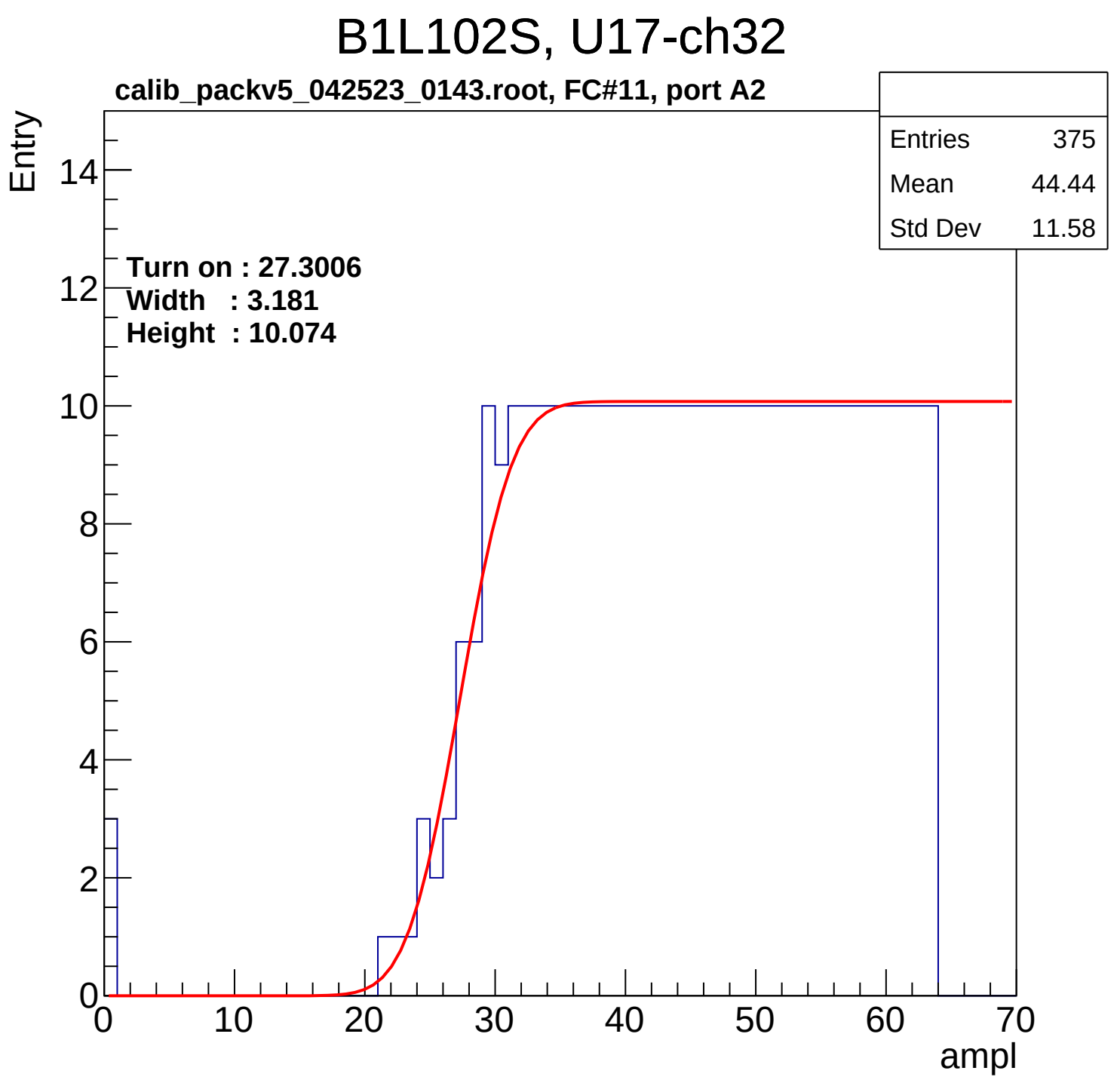
B1L102S, U17-ch32
calib_packv5_042523_0143.root, FC#11, port A2
Entries 375
Mean 44.44
Std Dev 11.58
Turn on : 27.3006
Width : 3.181
Height : 10.074
Entry
ampl
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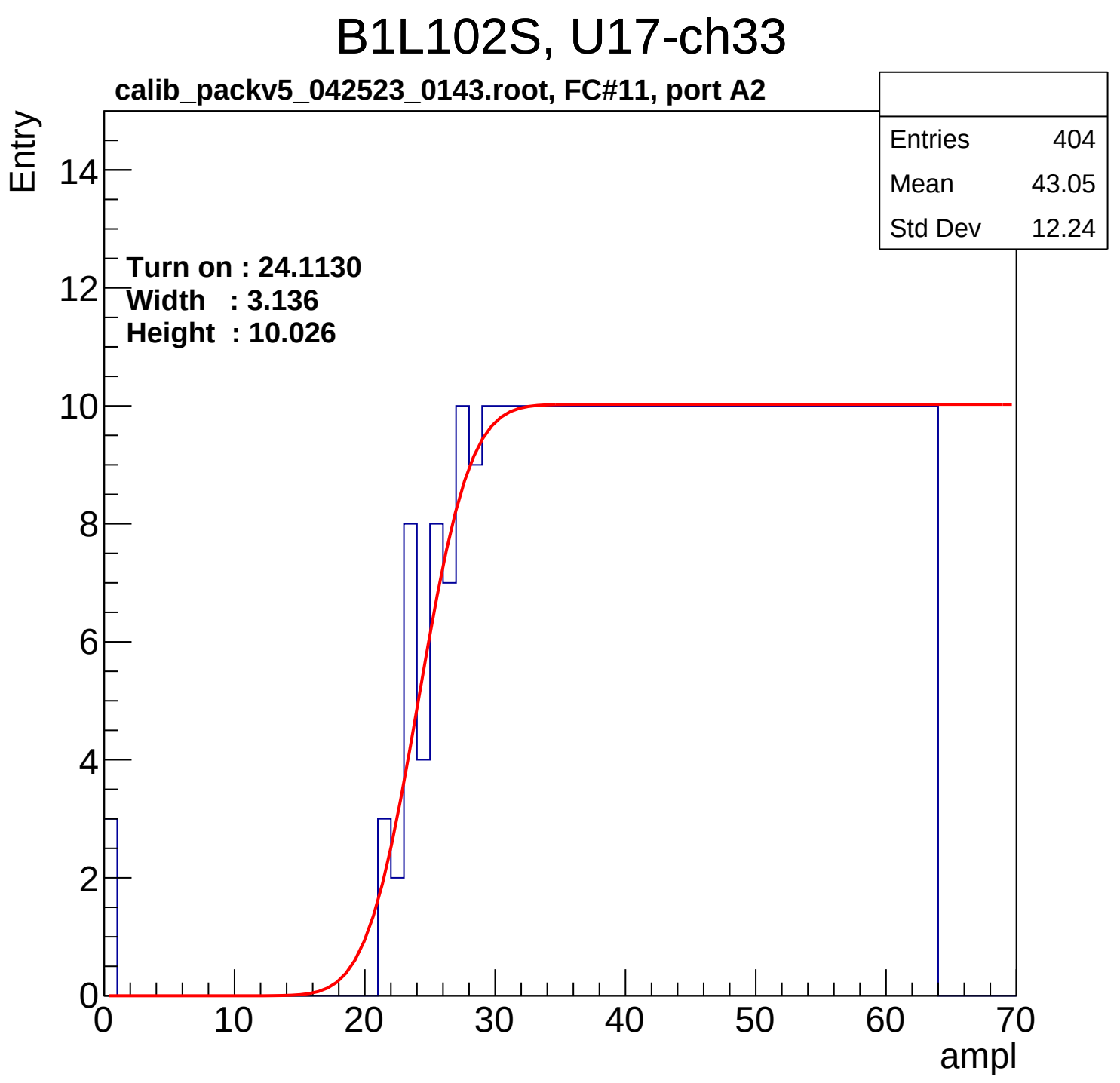
B1L102S, U17-ch33
calib_packv5_042523_0143.root, FC#11, port A2
Entries 404
Mean 43.05
Std Dev 12.24
Turn on : 24.1130
Width : 3.136
Height : 10.026
Entry
ampl
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2
4
6
8
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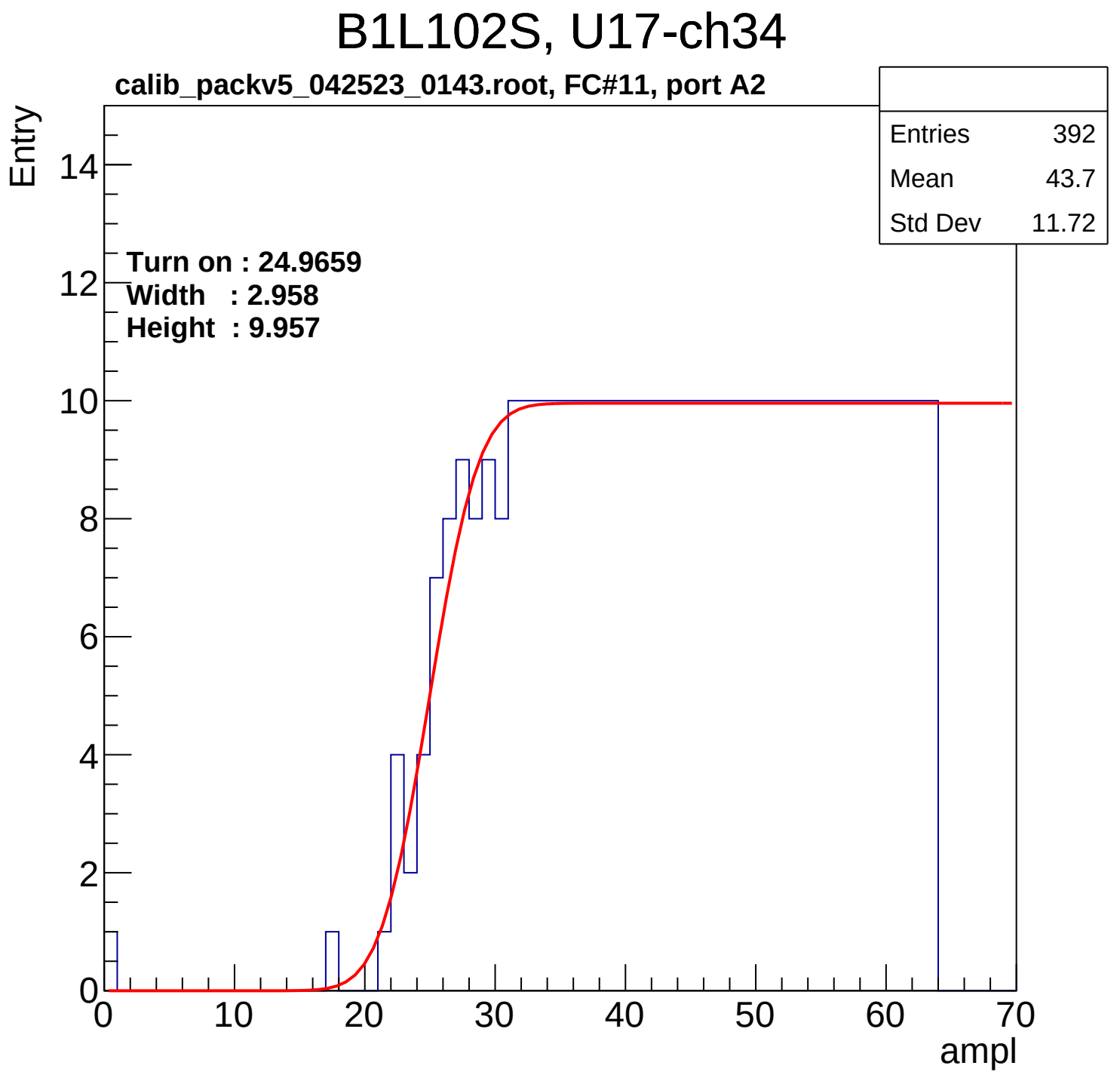
B1L102S, U17-ch34
calib_packv5_042523_0143.root, FC#11, port A2
Entries 392
Mean 43.7
Std Dev 11.72
Turn on : 24.9659
Width : 2.958
Height : 9.957
Entry
ampl
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6
8
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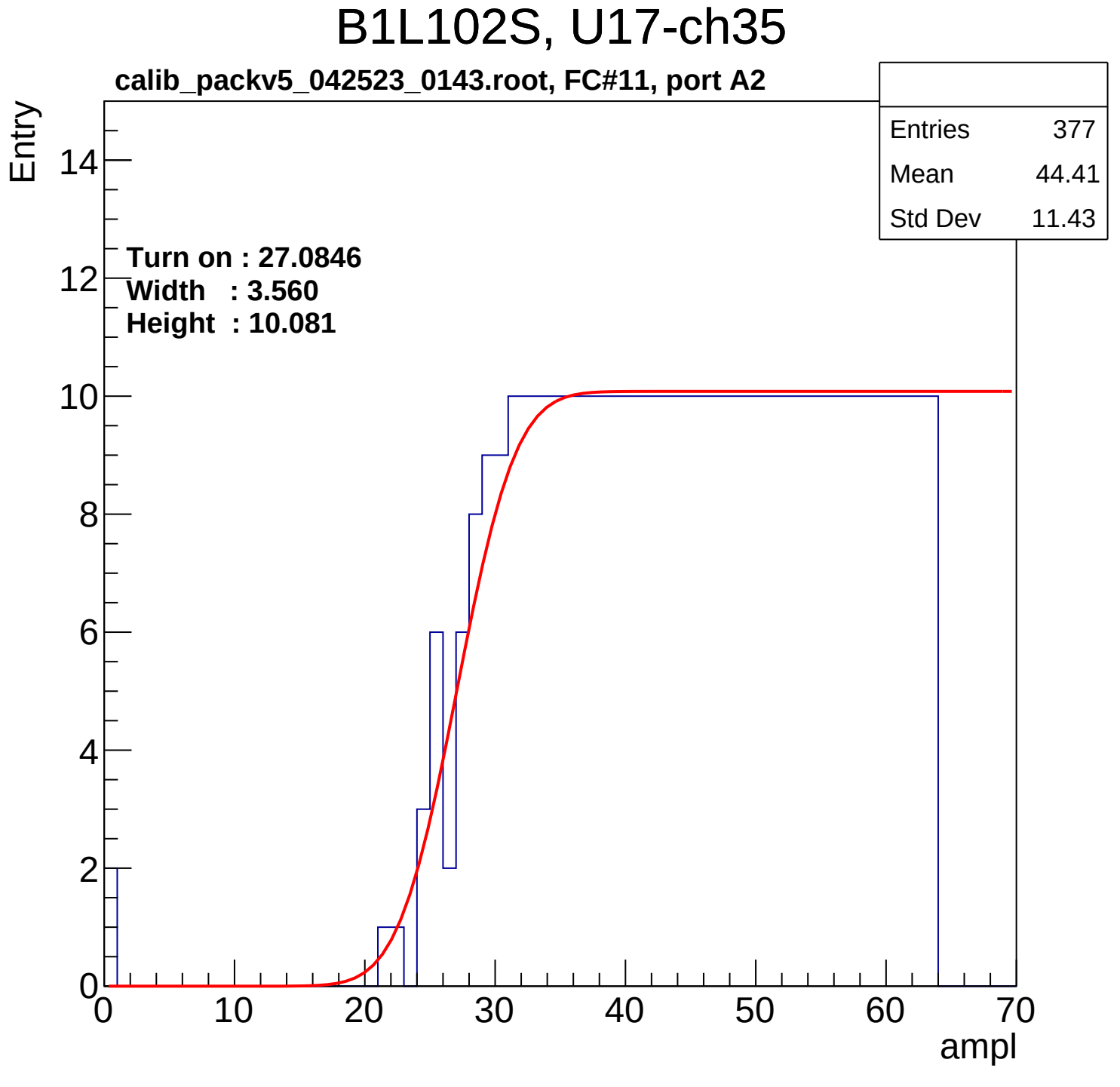
B1L102S, U17-ch35
calib_packv5_042523_0143.root, FC#11, port A2
Entries 377
Mean 44.41
Std Dev 11.43
Turn on : 27.0846
Width : 3.560
Height : 10.081
Entry
ampl
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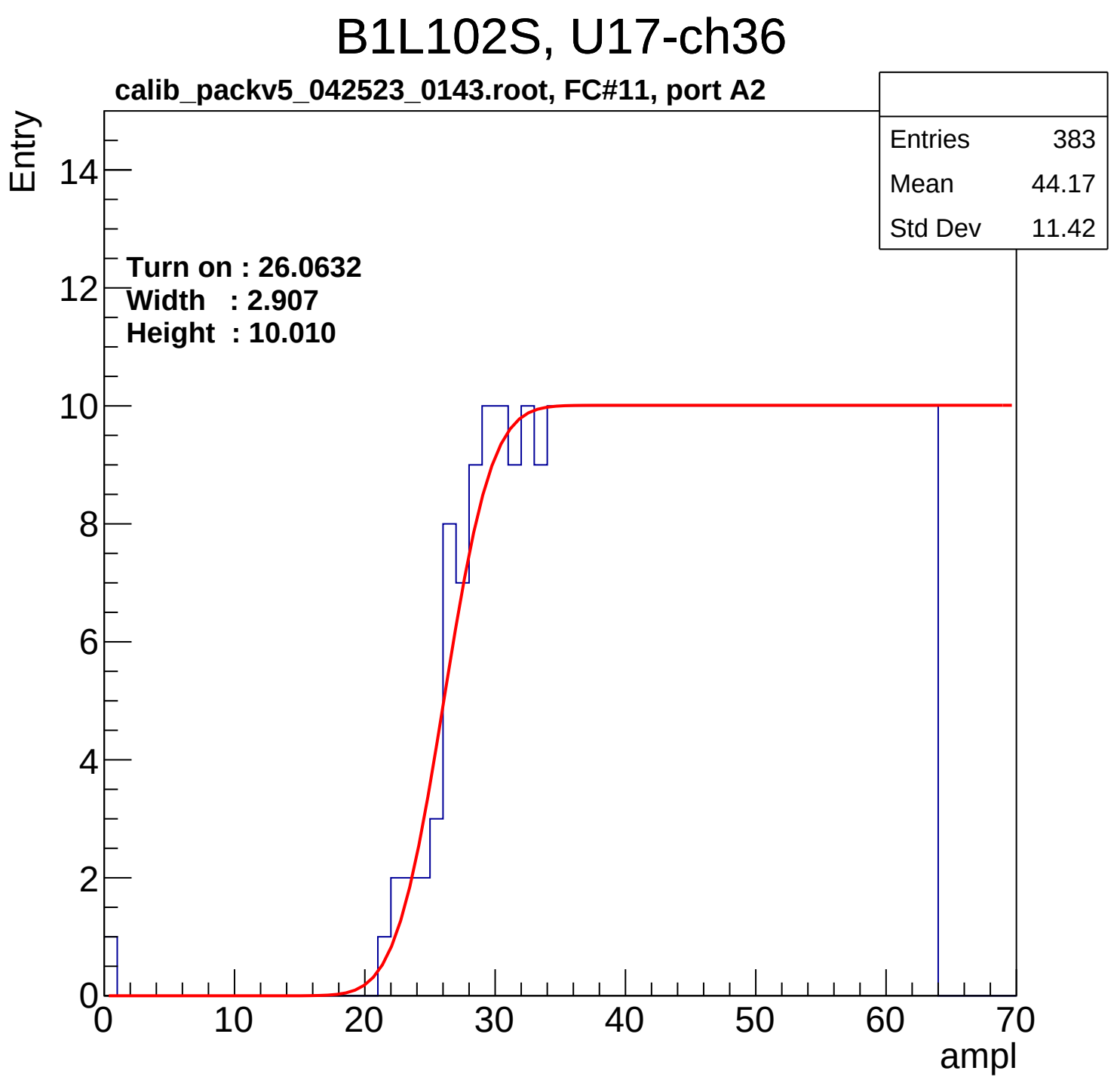
B1L102S, U17-ch36
calib_packv5_042523_0143.root, FC#11, port A2
Entries 383
Mean 44.17
Std Dev 11.42
Turn on : 26.0632
Width : 2.907
Height : 10.010
Entry
ampl
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4
6
8
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12
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0
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60
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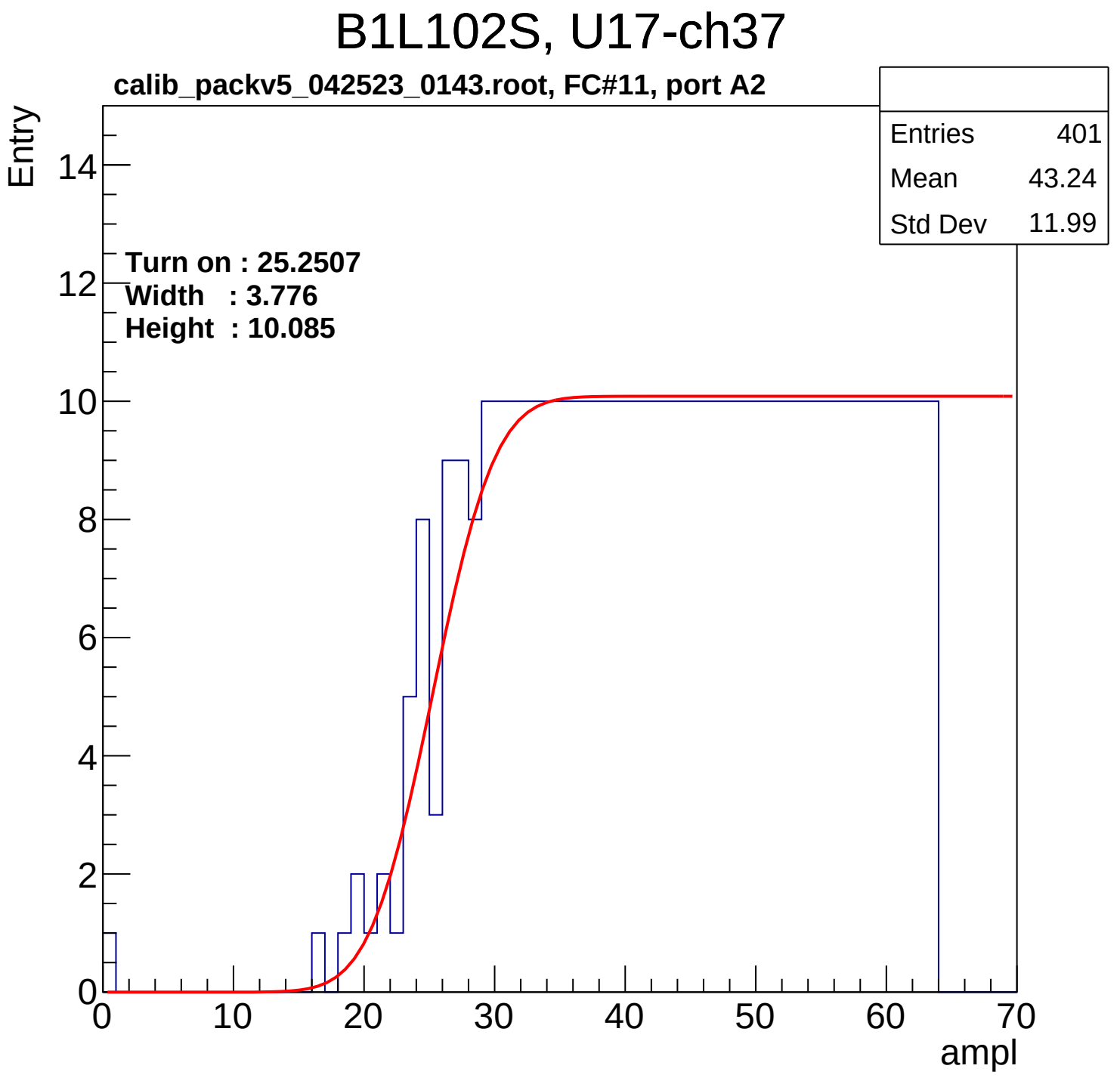
B1L102S, U17-ch37
calib_packv5_042523_0143.root, FC#11, port A2
Entries 401
Mean 43.24
Std Dev 11.99
Turn on : 25.2507
Width : 3.776
Height : 10.085
Entry
ampl
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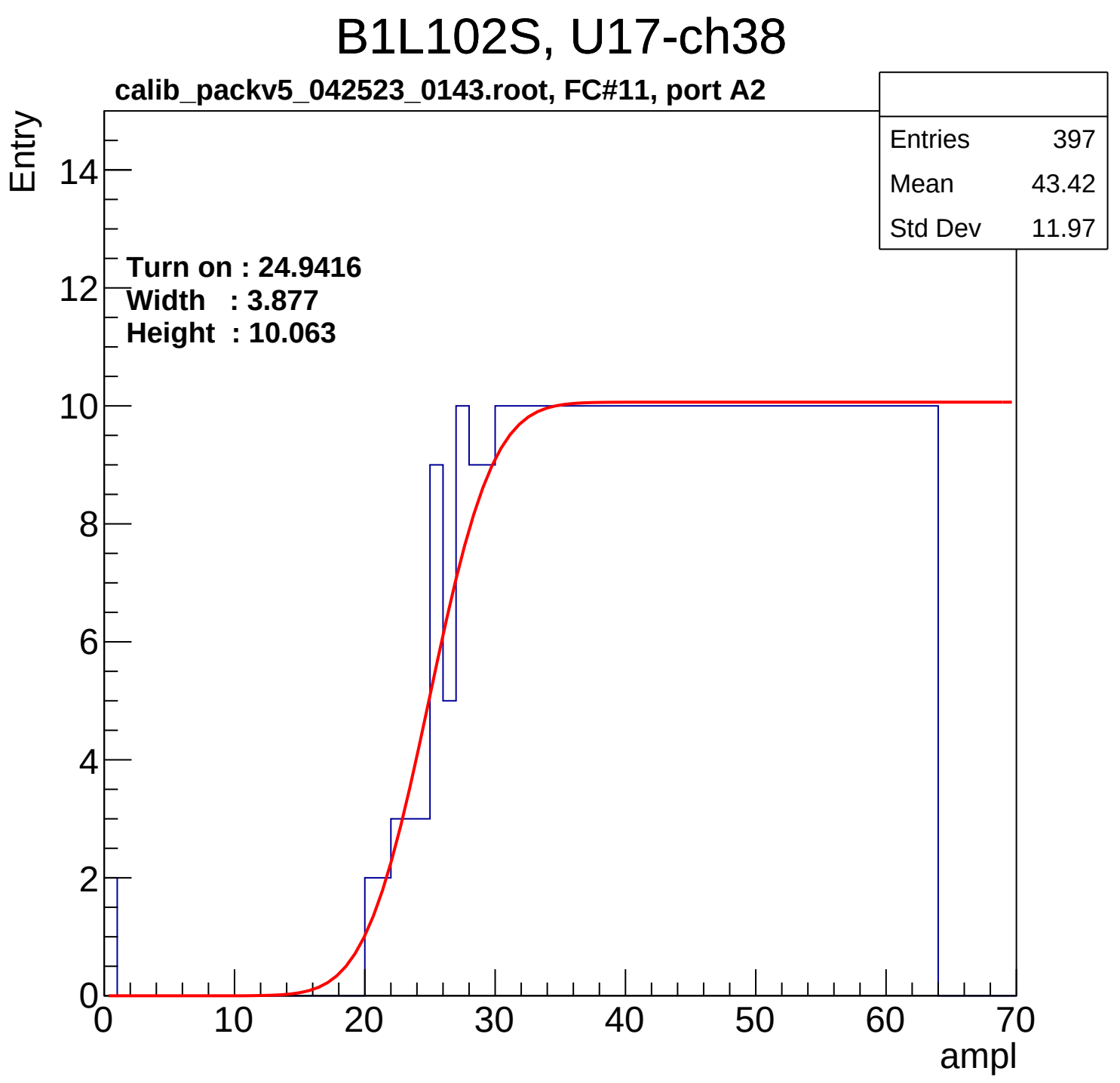
B1L102S, U17-ch38
calib_packv5_042523_0143.root, FC#11, port A2
Entries 397
Mean 43.42
Std Dev 11.97
Turn on : 24.9416
Width : 3.877
Height : 10.063
Entry
ampl
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2
4
6
8
10
12
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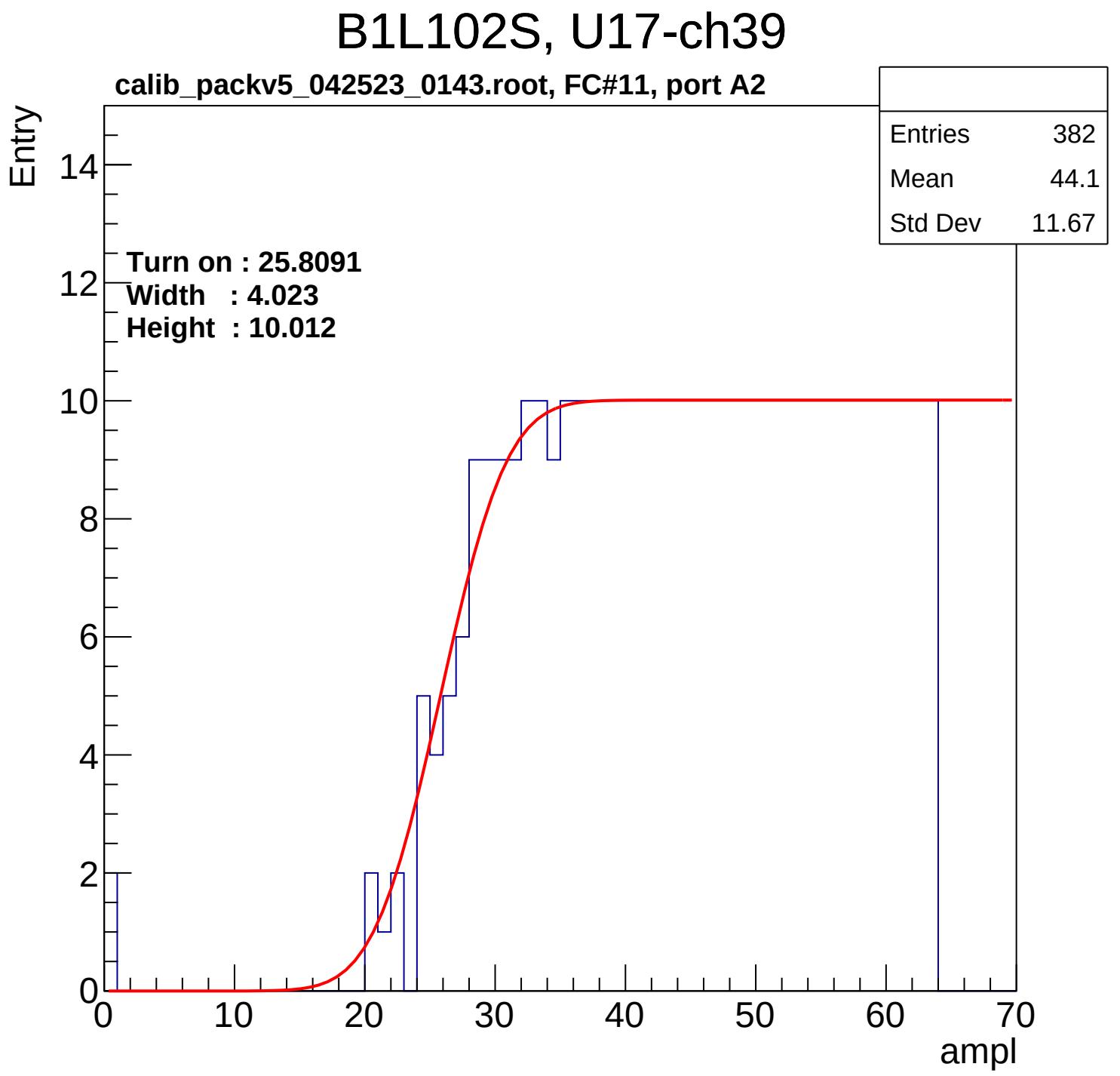
B1L102S, U17-ch39
calib_packv5_042523_0143.root, FC#11, port A2
Entries 382
Mean 44.1
Std Dev 11.67
Turn on : 25.8091
Width : 4.023
Height : 10.012
Entry
ampl
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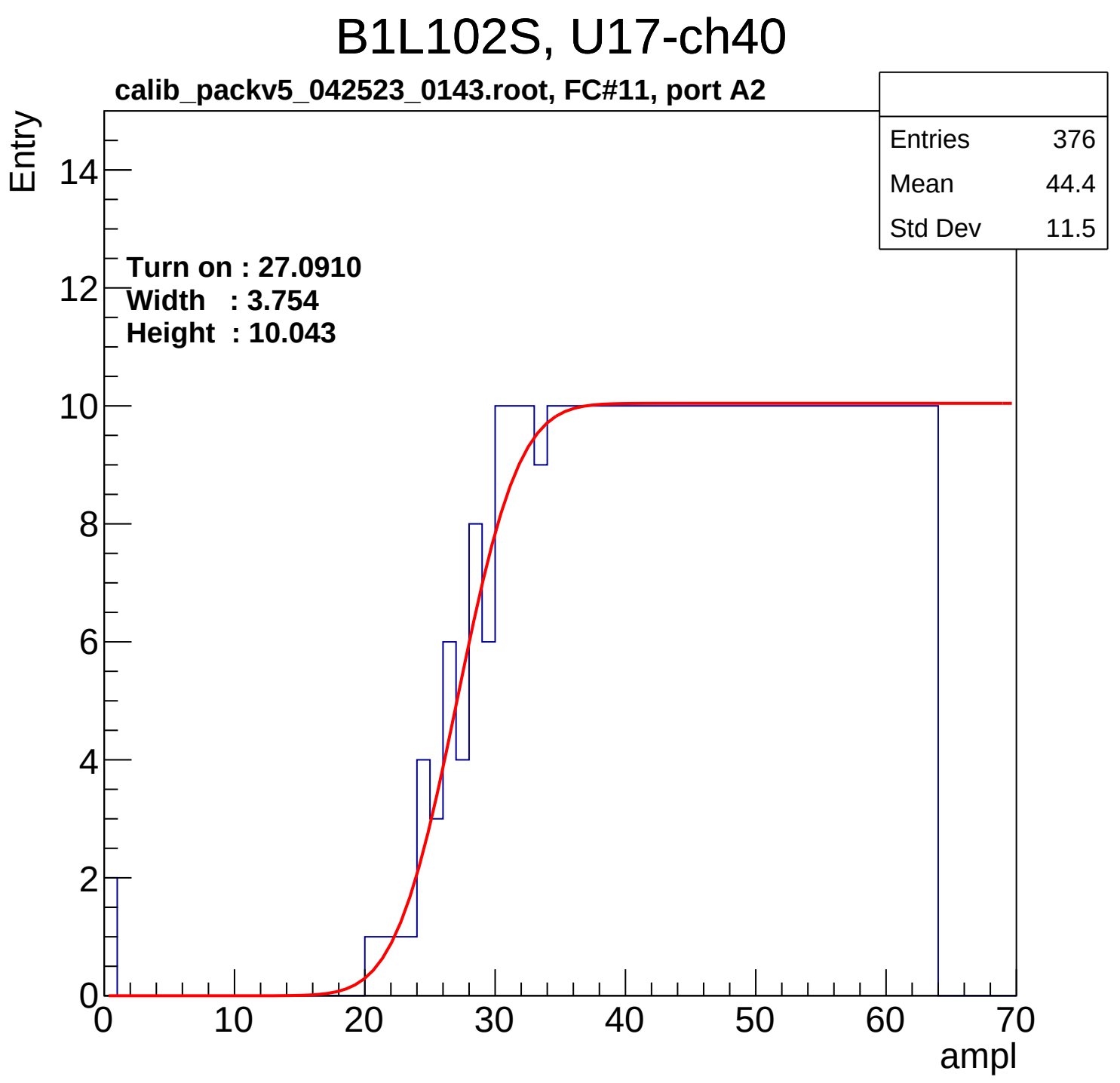
B1L102S, U17-ch40
calib_packv5_042523_0143.root, FC#11, port A2
Entries 376
Mean 44.4
Std Dev 11.5
Turn on : 27.0910
Width : 3.754
Height : 10.043
Entry
ampl
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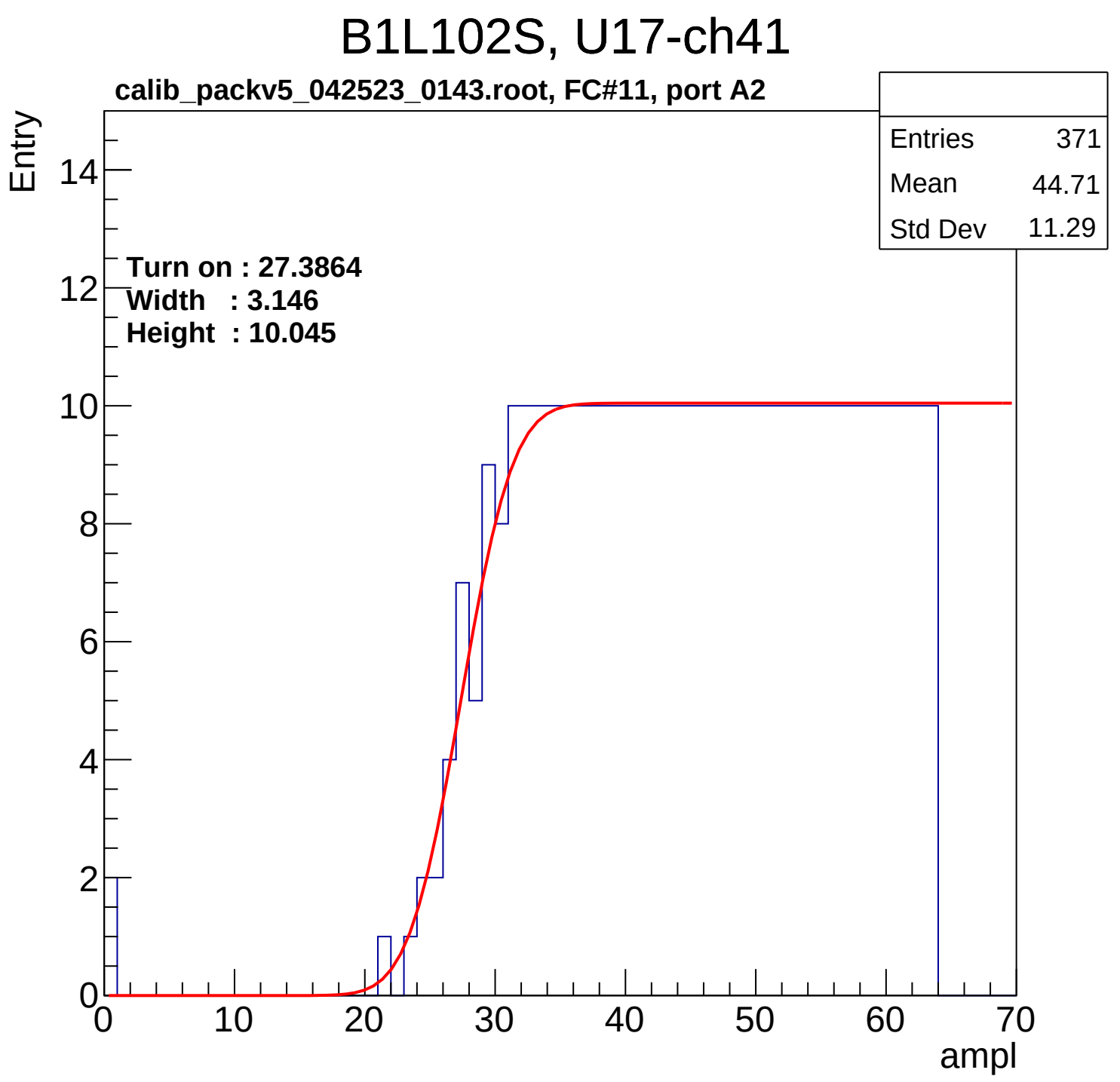
B1L102S, U17-ch41
calib_packv5_042523_0143.root, FC#11, port A2
Entries 371
Mean 44.71
Std Dev 11.29
Turn on : 27.3864
Width : 3.146
Height : 10.045
Entry
ampl
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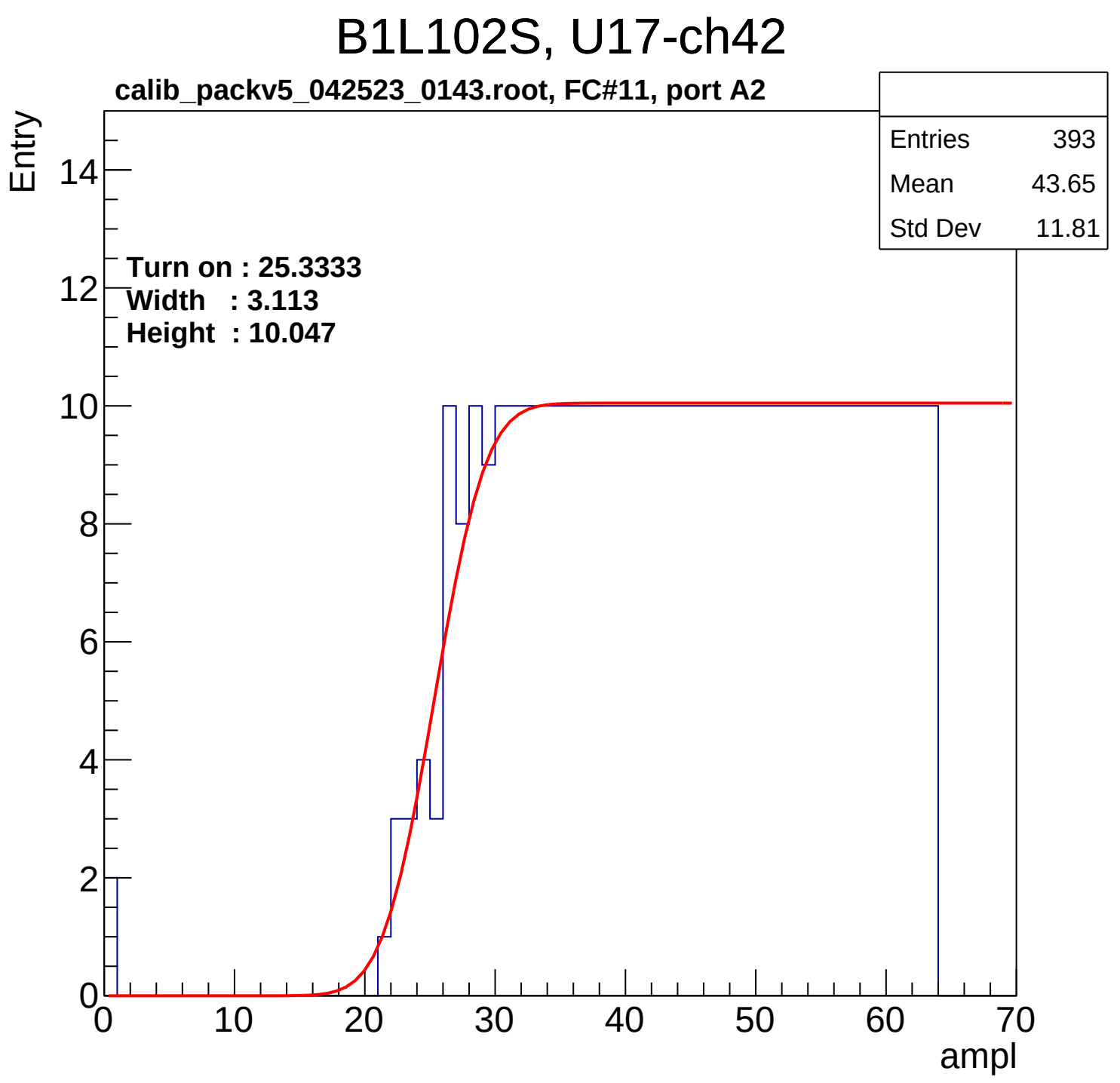
B1L102S, U17-ch42
calib_packv5_042523_0143.root, FC#11, port A2
Entries 393
Mean 43.65
Std Dev 11.81
Turn on : 25.3333
Width : 3.113
Height : 10.047
Entry
ampl
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6
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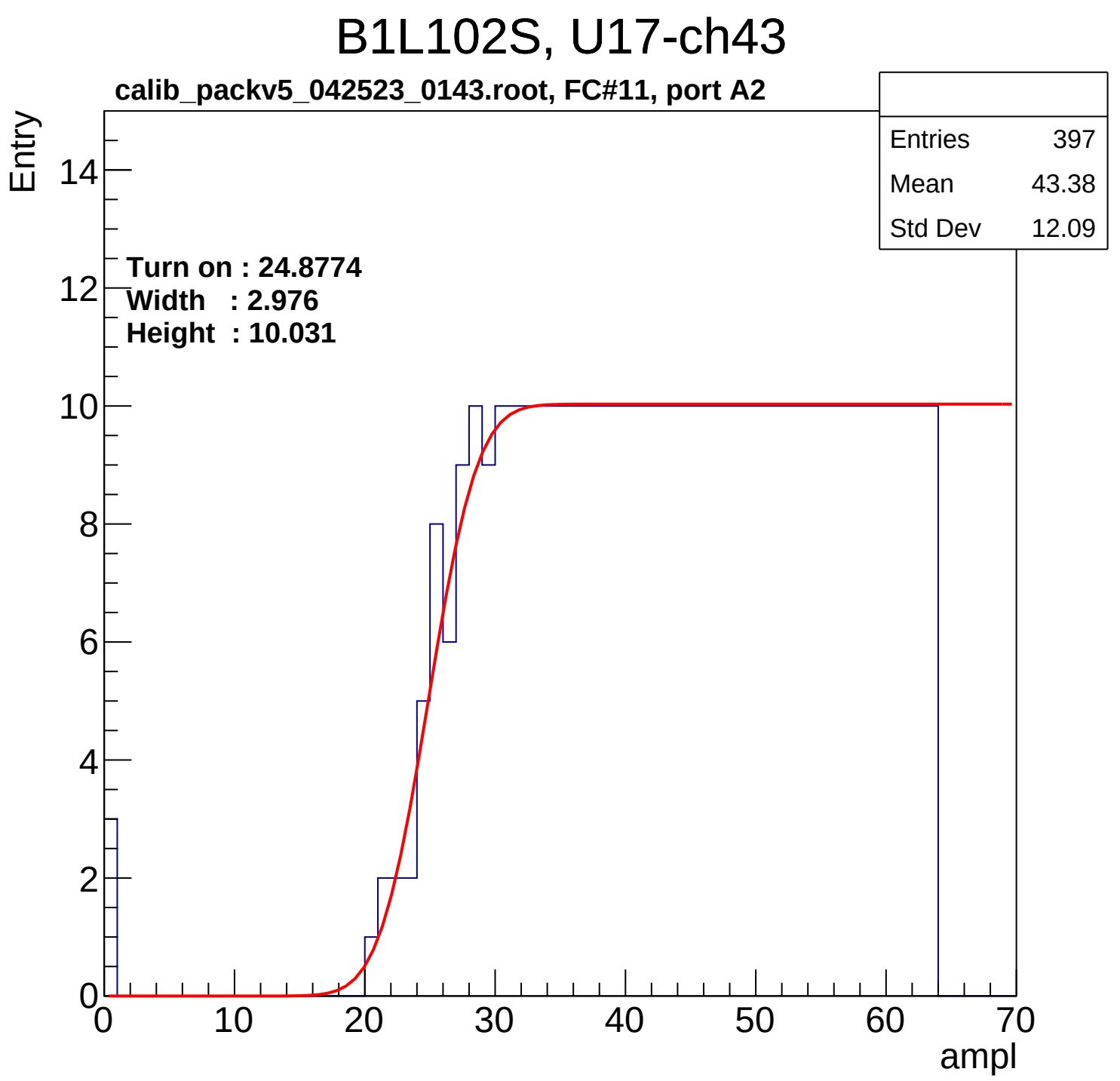
B1L102S, U17-ch43
calib_packv5_042523_0143.root, FC#11, port A2
Entries 397
Mean 43.38
Std Dev 12.09
Turn on : 24.8774
Width : 2.976
Height : 10.031
Entry
ampl
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6
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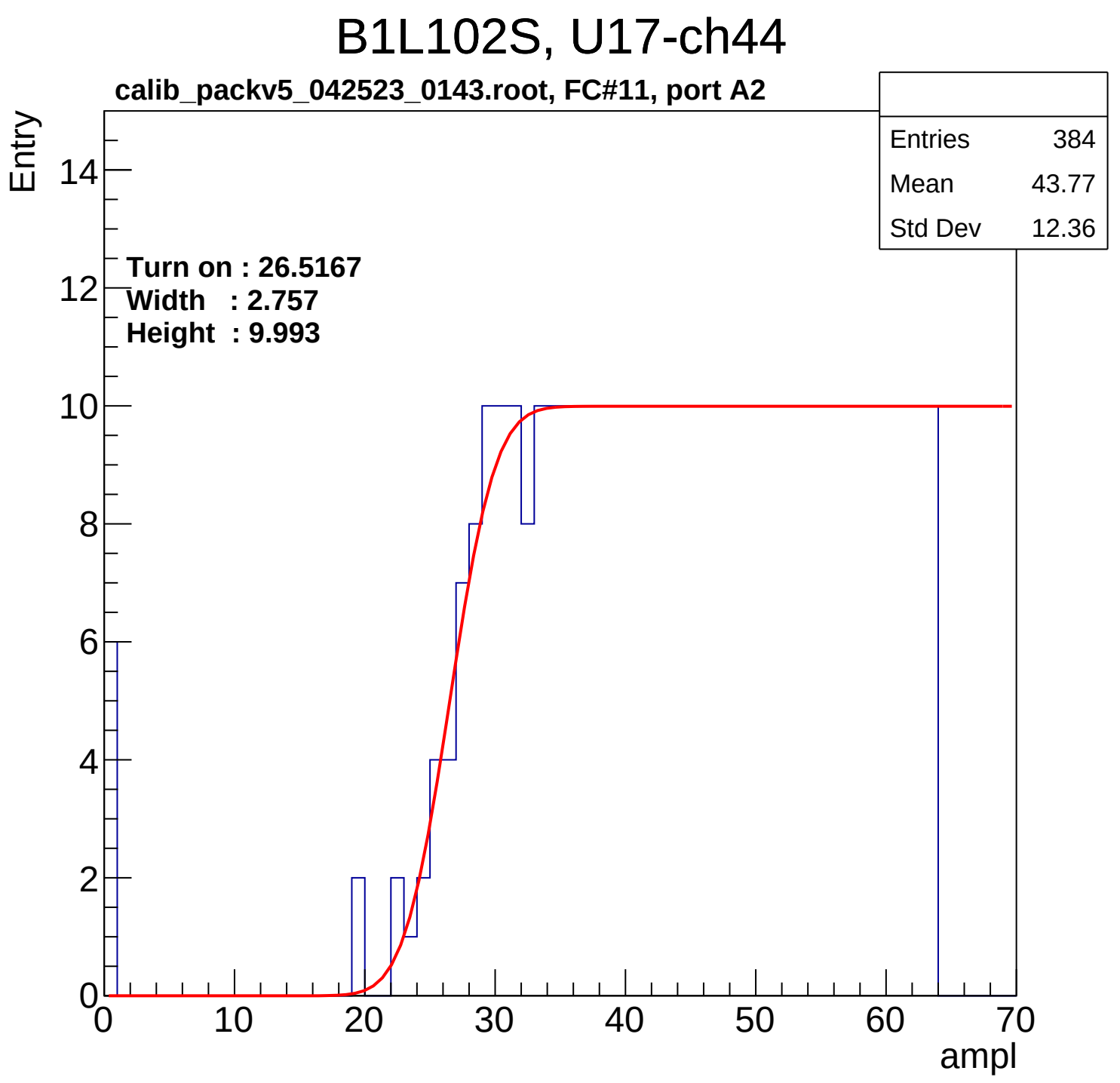
B1L102S, U17-ch44
calib_packv5_042523_0143.root, FC#11, port A2
Entries 384
Mean 43.77
Std Dev 12.36
Turn on : 26.5167
Width : 2.757
Height : 9.993
Entry
ampl
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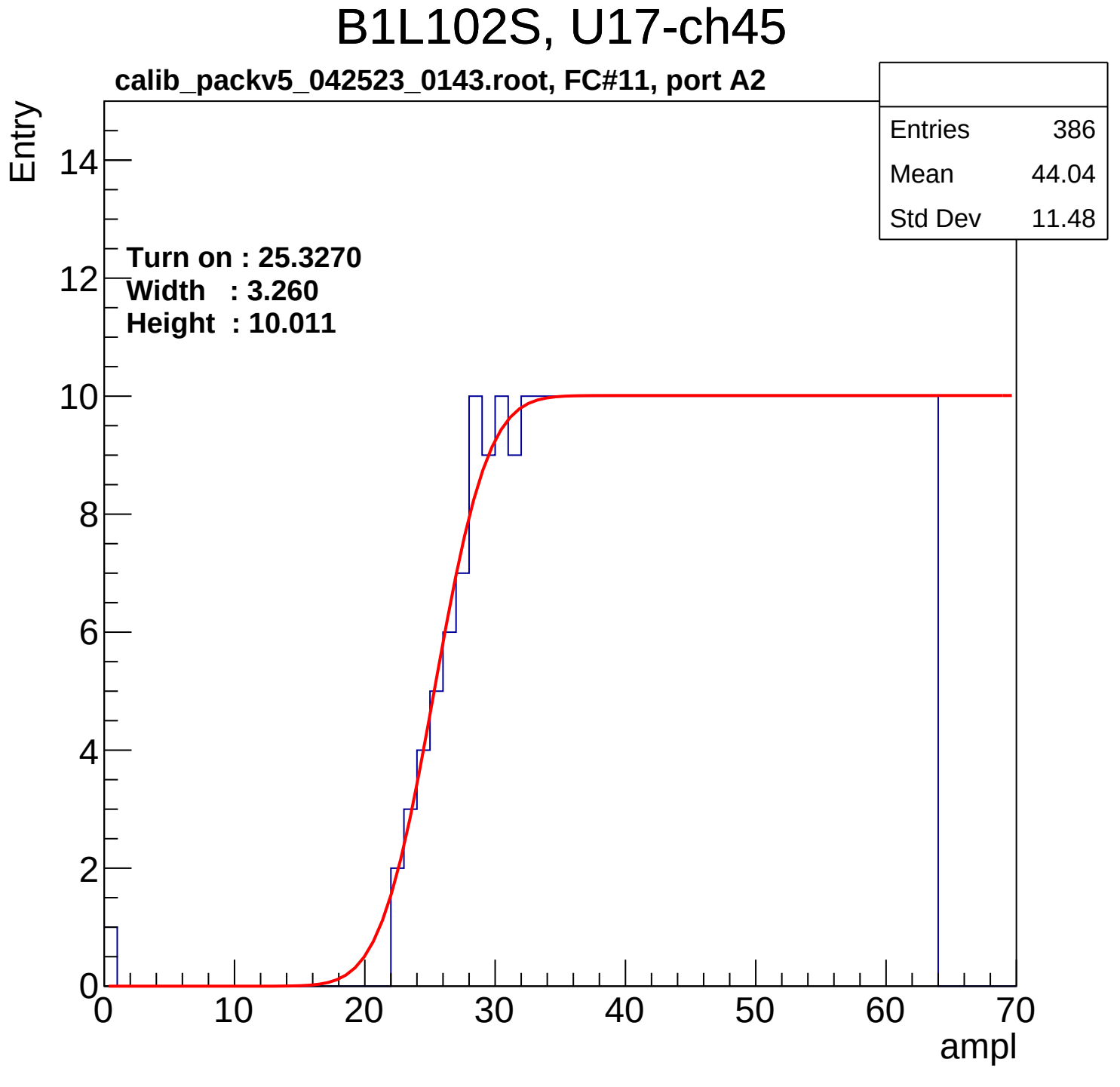
B1L102S, U17-ch45
calib_packv5_042523_0143.root, FC#11, port A2
Entries 386
Mean 44.04
Std Dev 11.48
Turn on : 25.3270
Width : 3.260
Height : 10.011
Entry
ampl
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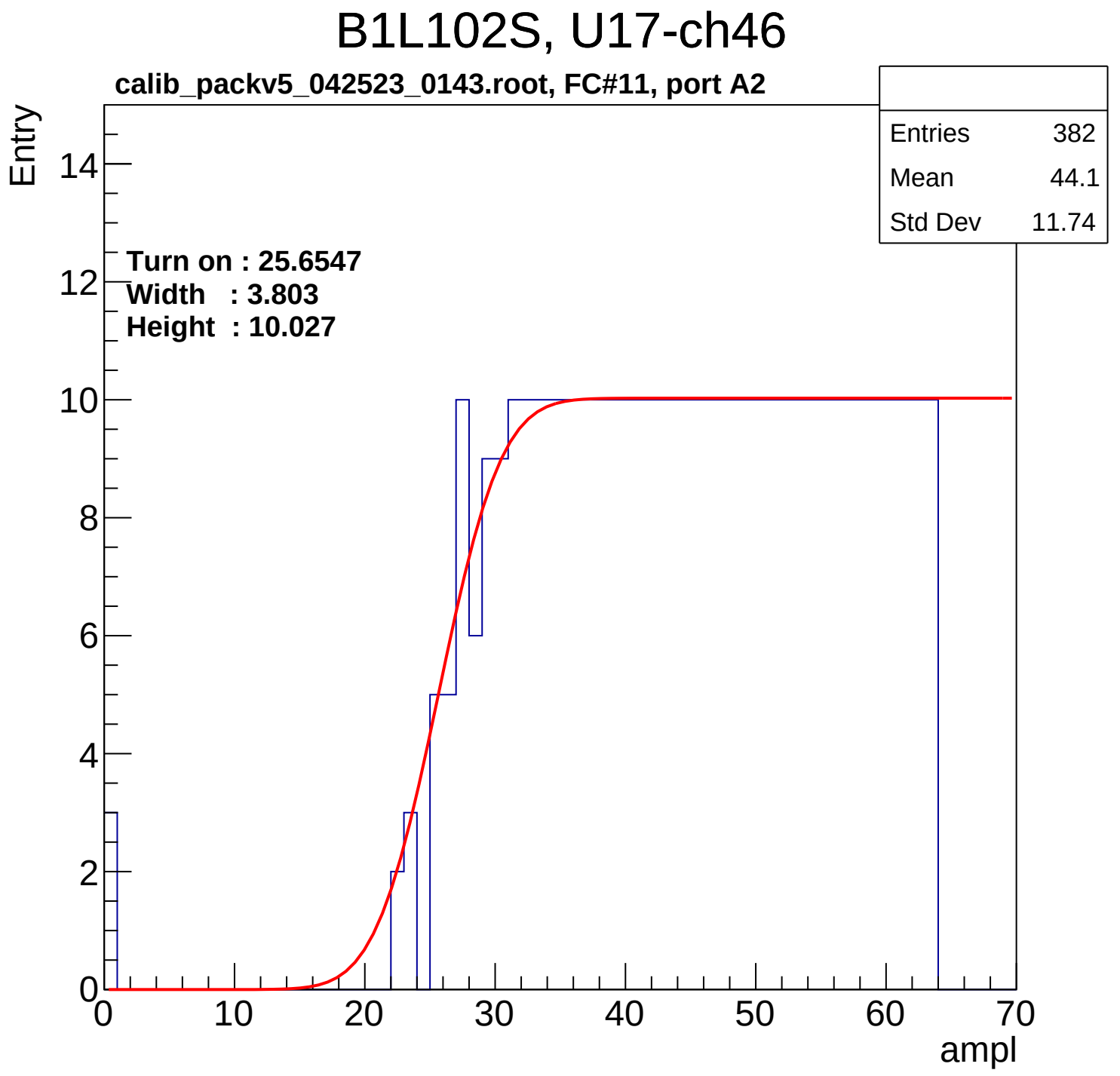
B1L102S, U17-ch46
calib_packv5_042523_0143.root, FC#11, port A2
Entries 382
Mean 44.1
Std Dev 11.74
Turn on : 25.6547
Width : 3.803
Height : 10.027
Entry
ampl
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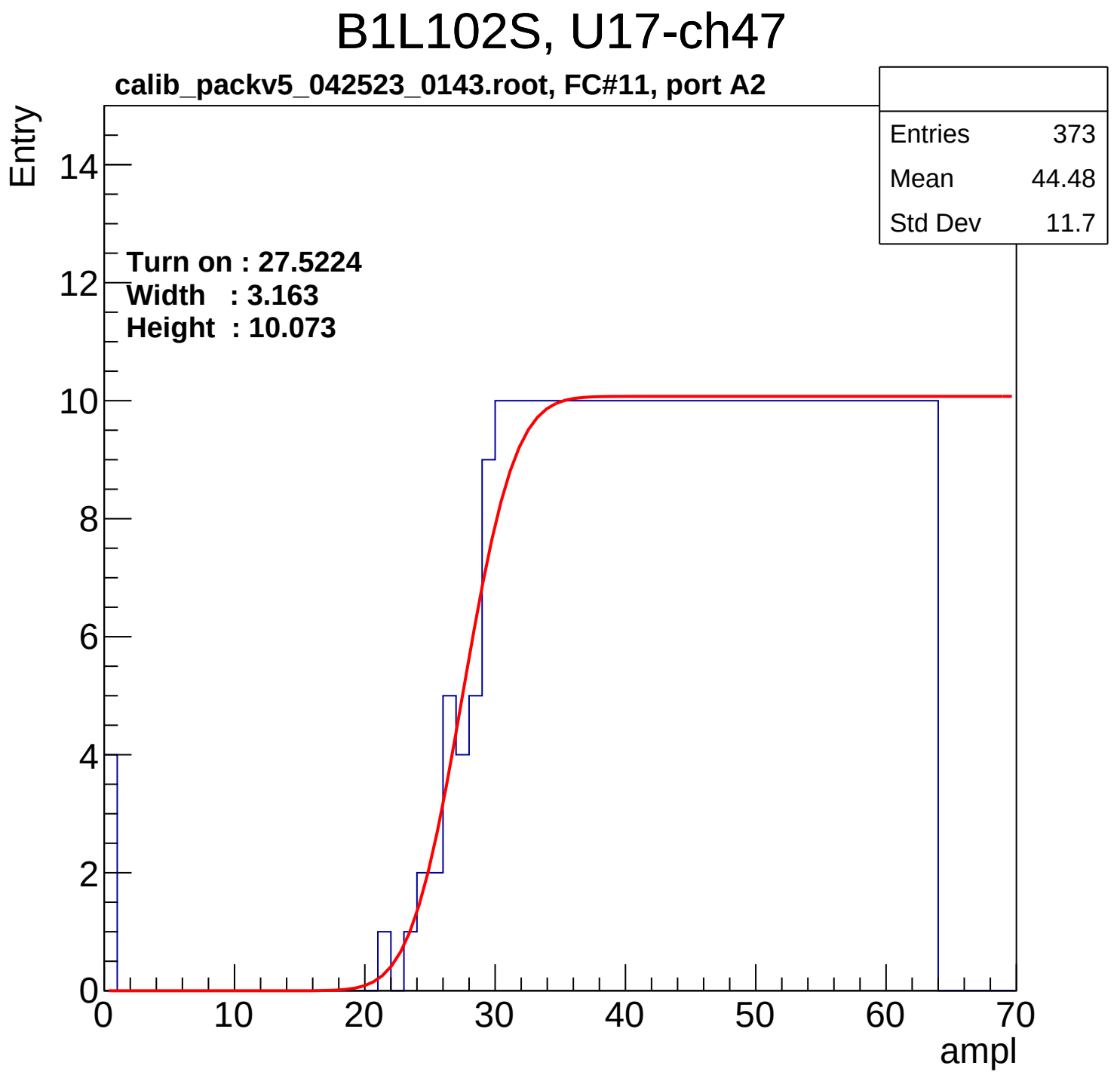
B1L102S, U17-ch47
calib_packv5_042523_0143.root, FC#11, port A2
Entries 373
Mean 44.48
Std Dev 11.7
Turn on : 27.5224
Width : 3.163
Height : 10.073
Entry
ampl
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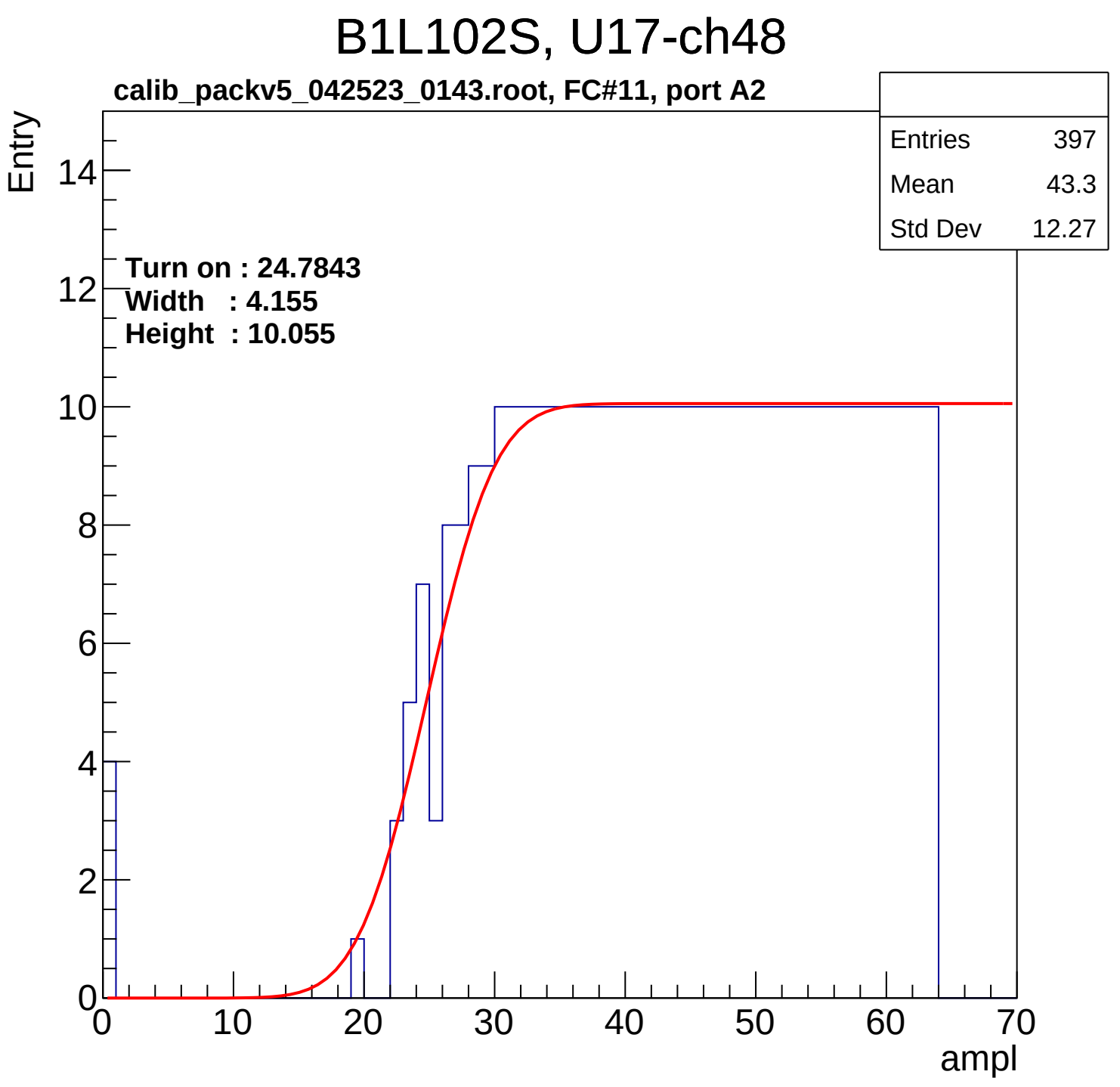
B1L102S, U17-ch48
calib_packv5_042523_0143.root, FC#11, port A2
Entries 397
Mean 43.3
Std Dev 12.27
Turn on : 24.7843
Width : 4.155
Height : 10.055
Entry
ampl
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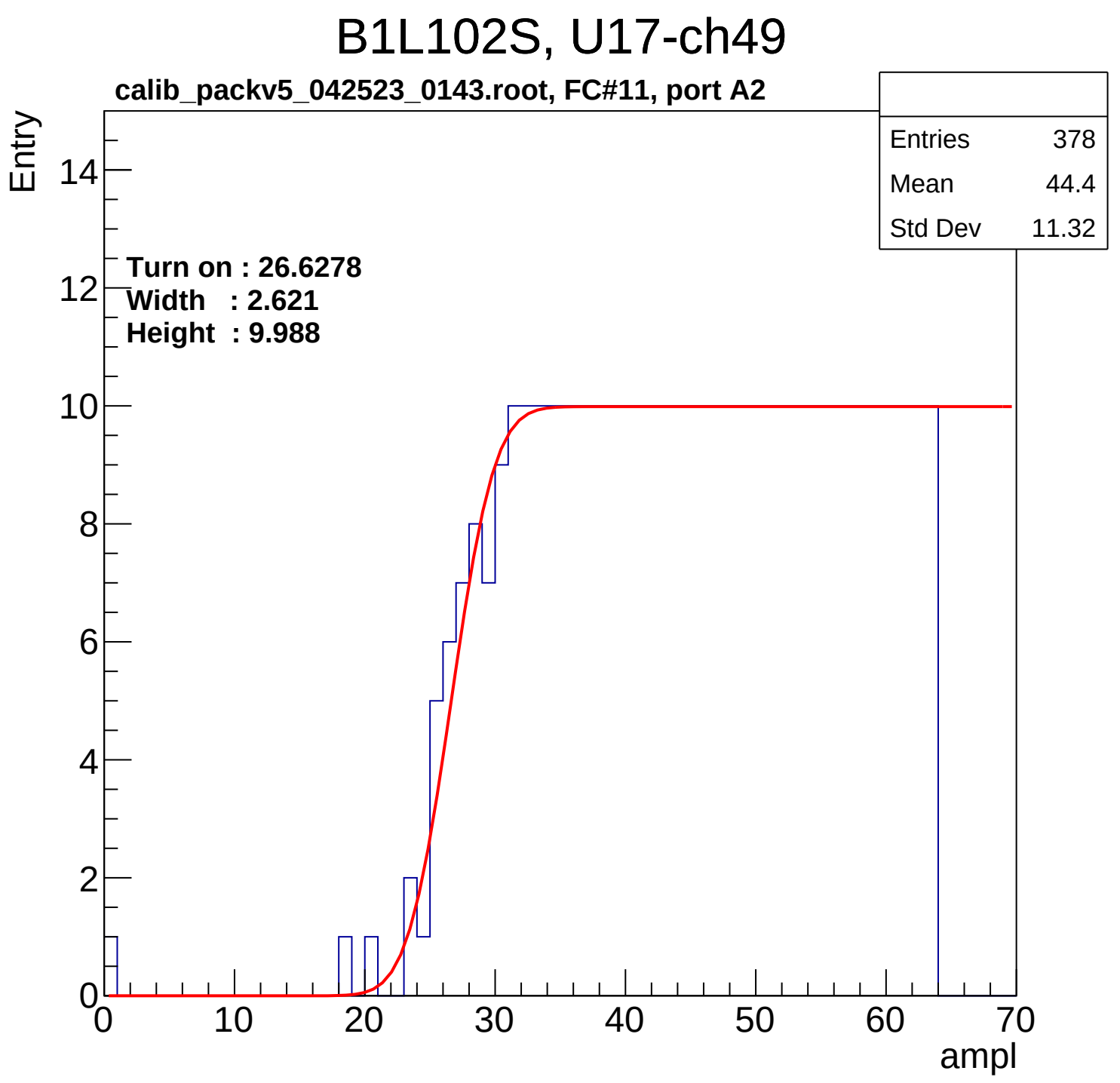
B1L102S, U17-ch49
calib_packv5_042523_0143.root, FC#11, port A2
Entries 378
Mean 44.4
Std Dev 11.32
Turn on : 26.6278
Width : 2.621
Height : 9.988
Entry
ampl
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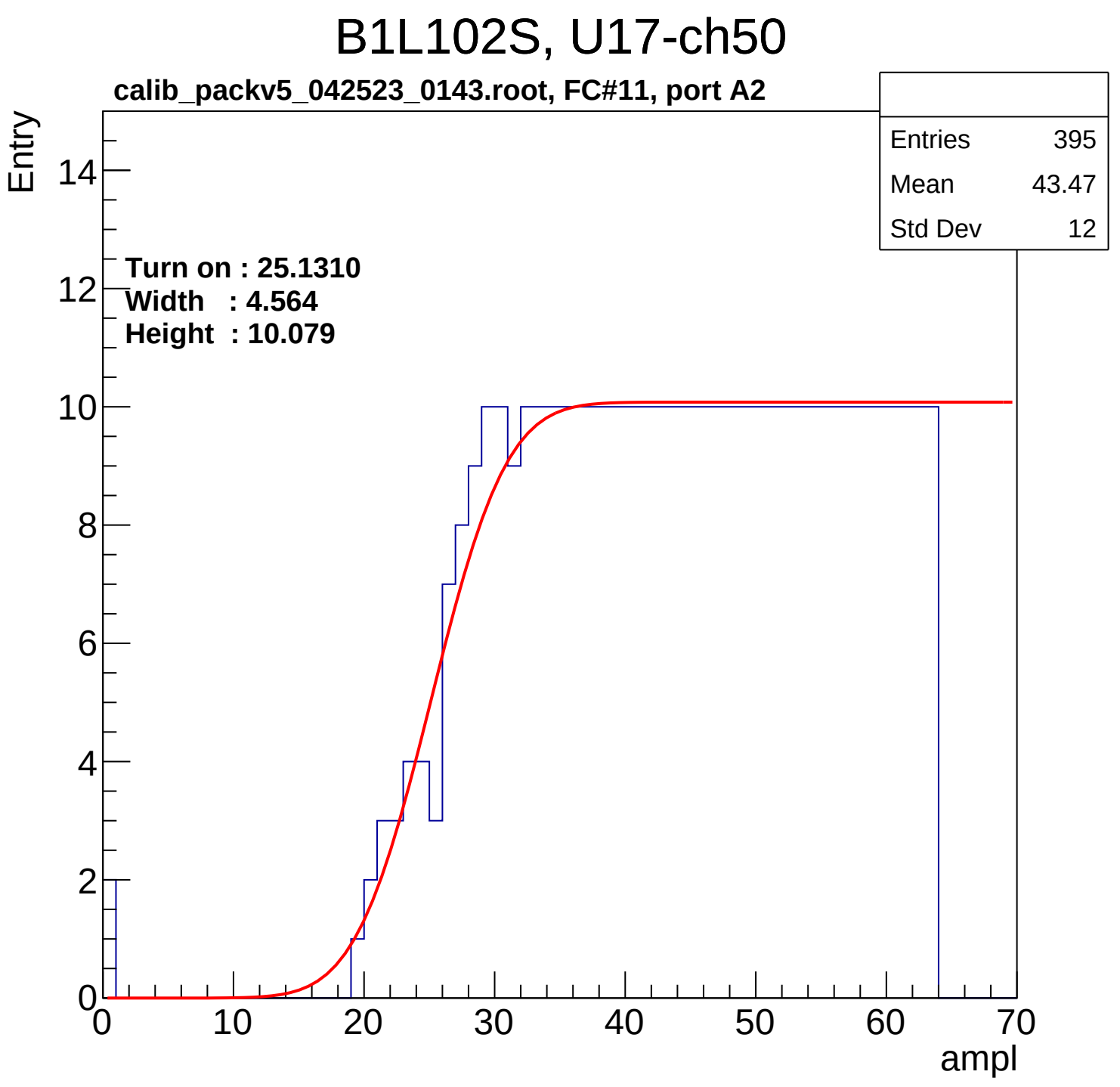
B1L102S, U17-ch50
calib_packv5_042523_0143.root, FC#11, port A2
Entries 395
Mean 43.47
Std Dev 12
Turn on : 25.1310
Width : 4.564
Height : 10.079
Entry
ampl
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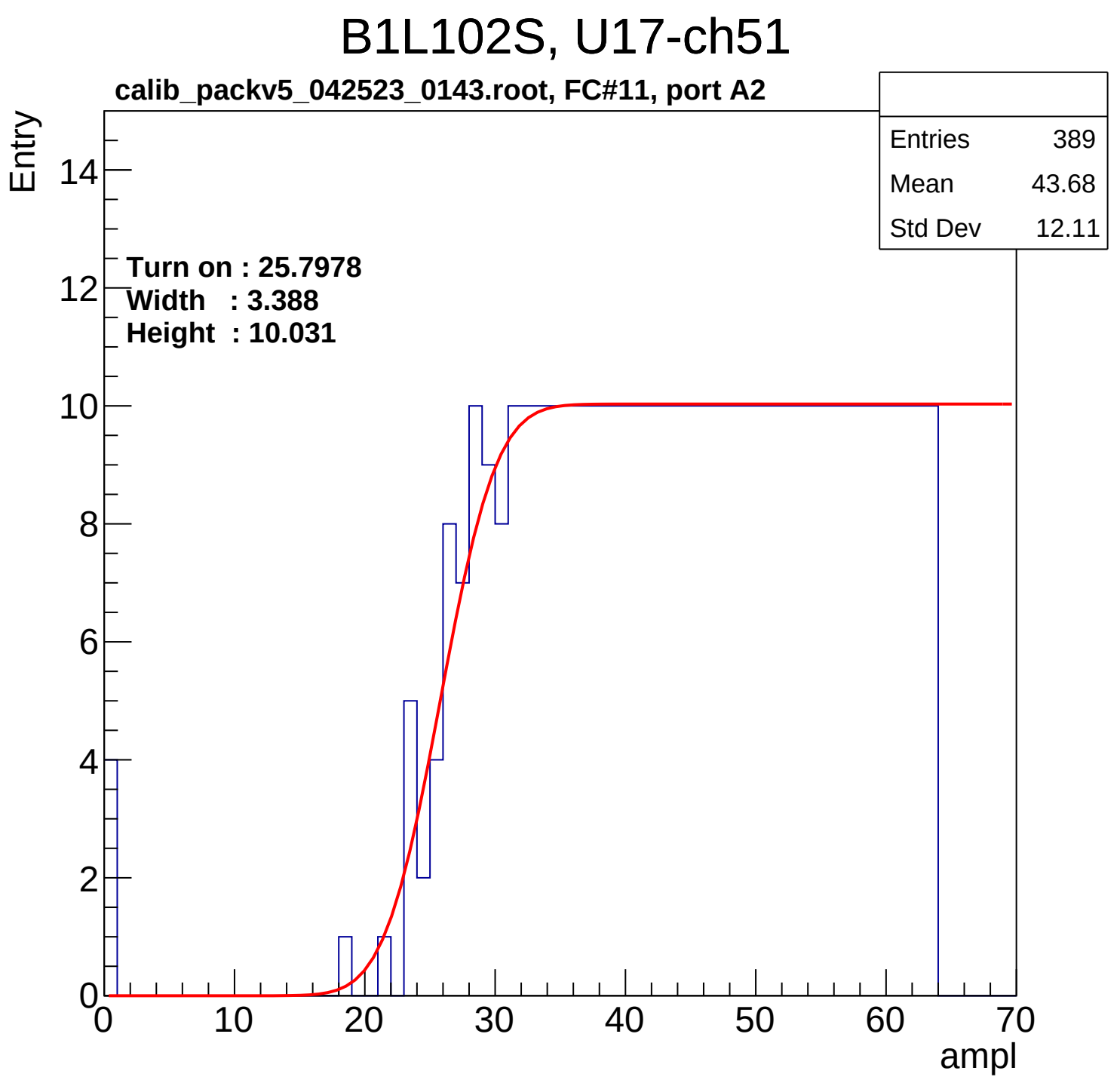
B1L102S, U17-ch51
calib_packv5_042523_0143.root, FC#11, port A2
Entries 389
Mean 43.68
Std Dev 12.11
Turn on : 25.7978
Width : 3.388
Height : 10.031
Entry
ampl
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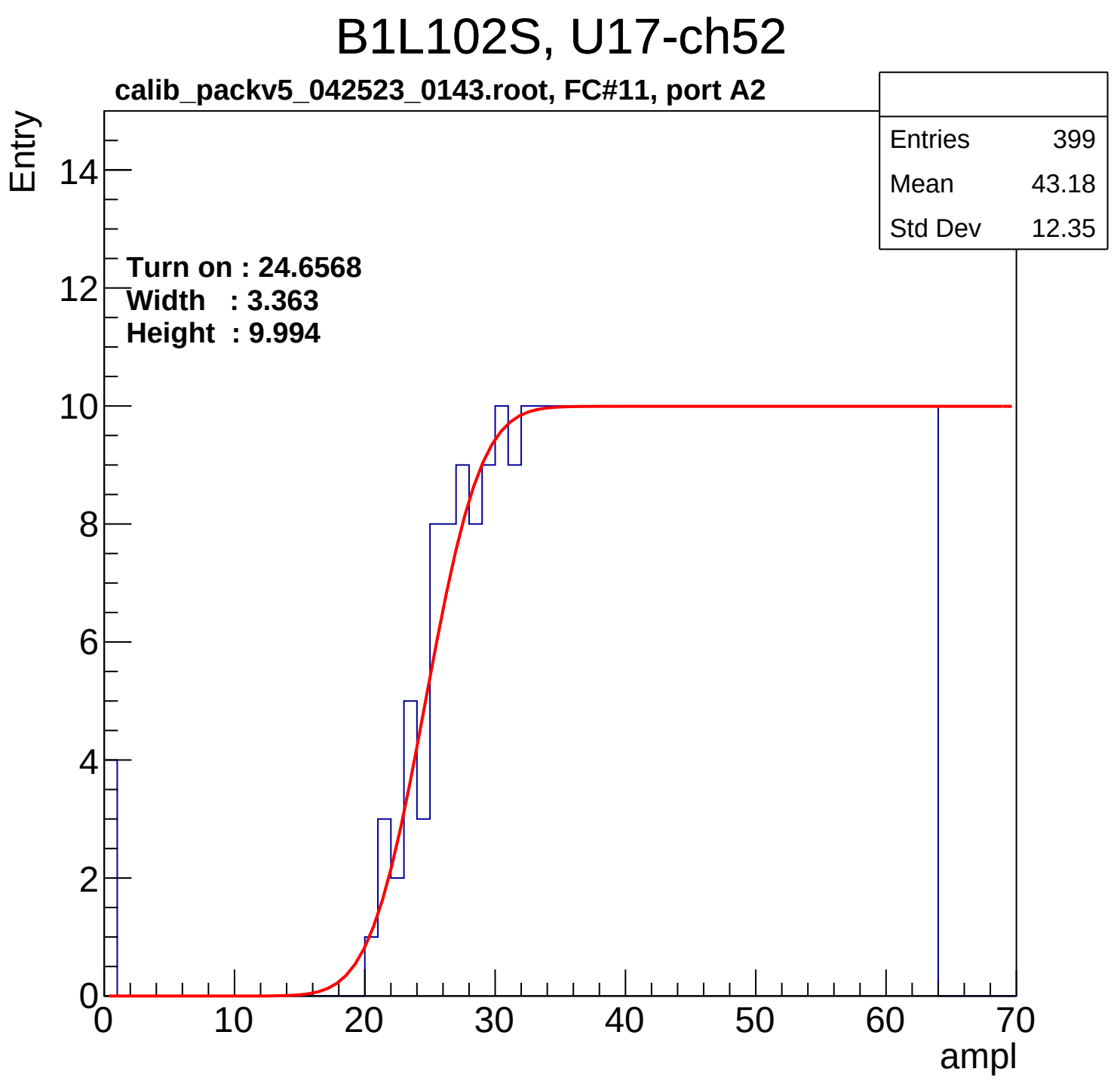
B1L102S, U17-ch52
calib_packv5_042523_0143.root, FC#11, port A2
Entries 399
Mean 43.18
Std Dev 12.35
Turn on : 24.6568
Width : 3.363
Height : 9.994
Entry
ampl
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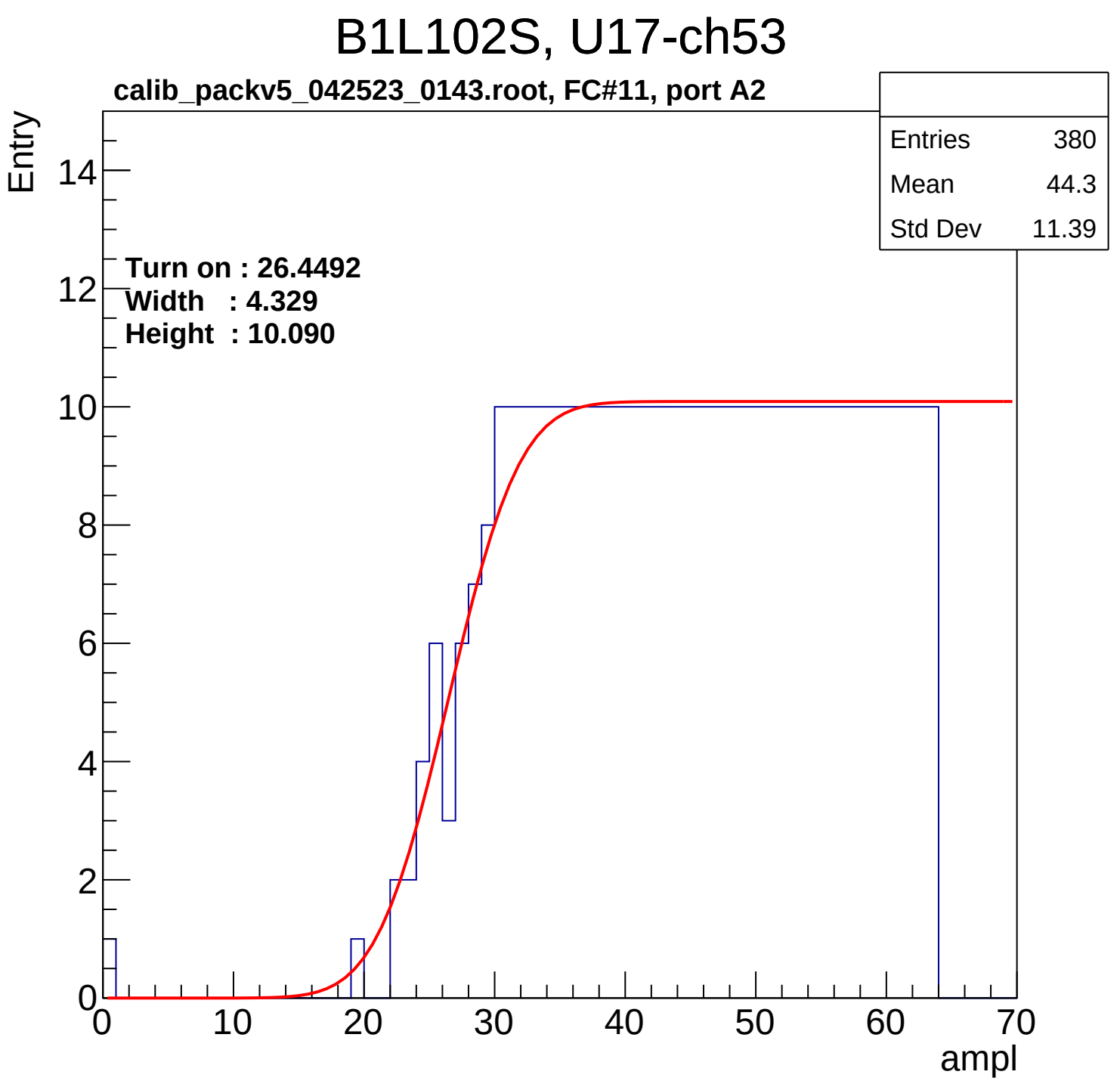
B1L102S, U17-ch53
calib_packv5_042523_0143.root, FC#11, port A2
Entries 380
Mean 44.3
Std Dev 11.39
Turn on : 26.4492
Width : 4.329
Height : 10.090
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ampl
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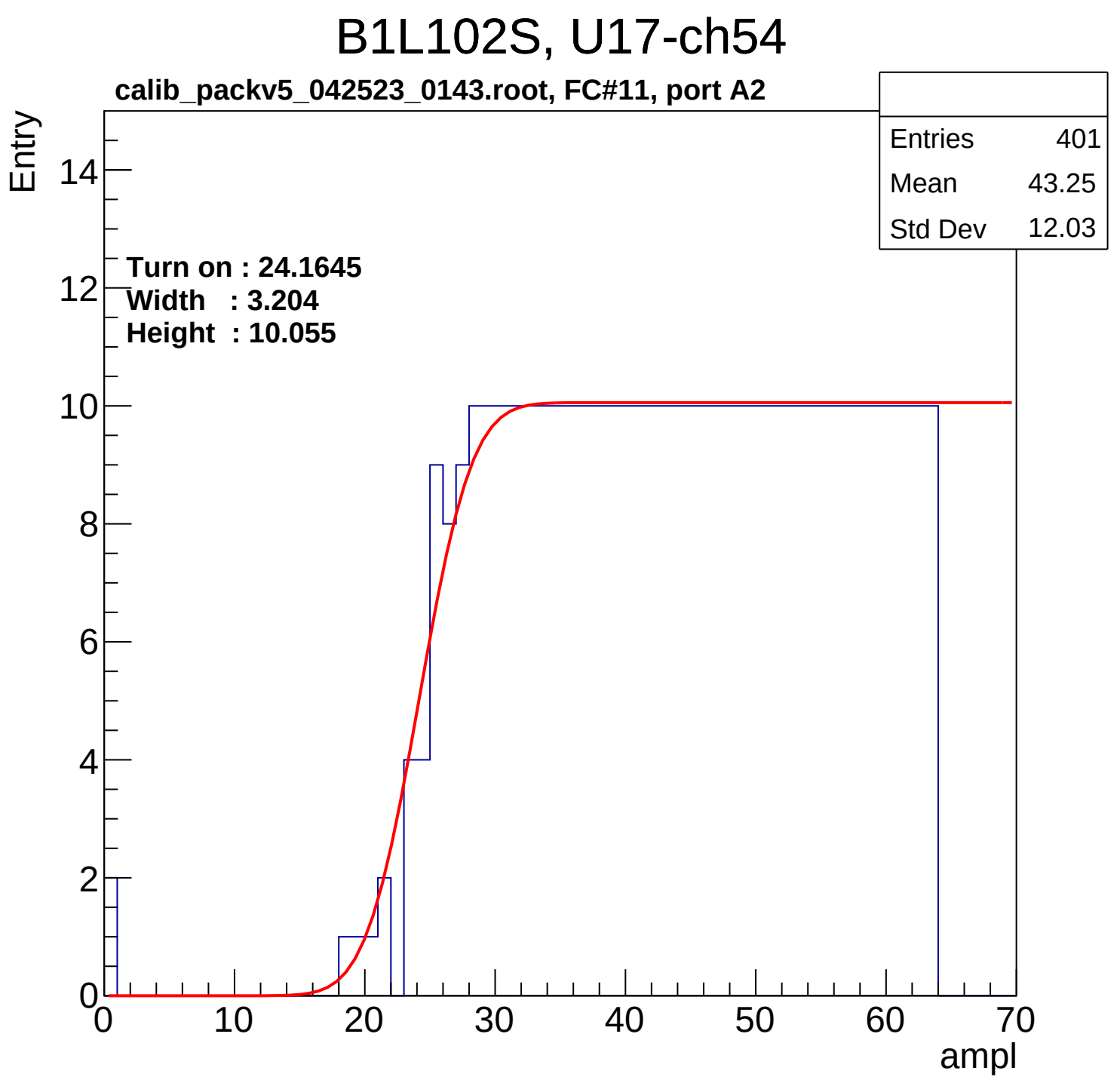
B1L102S, U17-ch54
calib_packv5_042523_0143.root, FC#11, port A2
Entries 401
Mean 43.25
Std Dev 12.03
Turn on : 24.1645
Width : 3.204
Height : 10.055
Entry
ampl
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8
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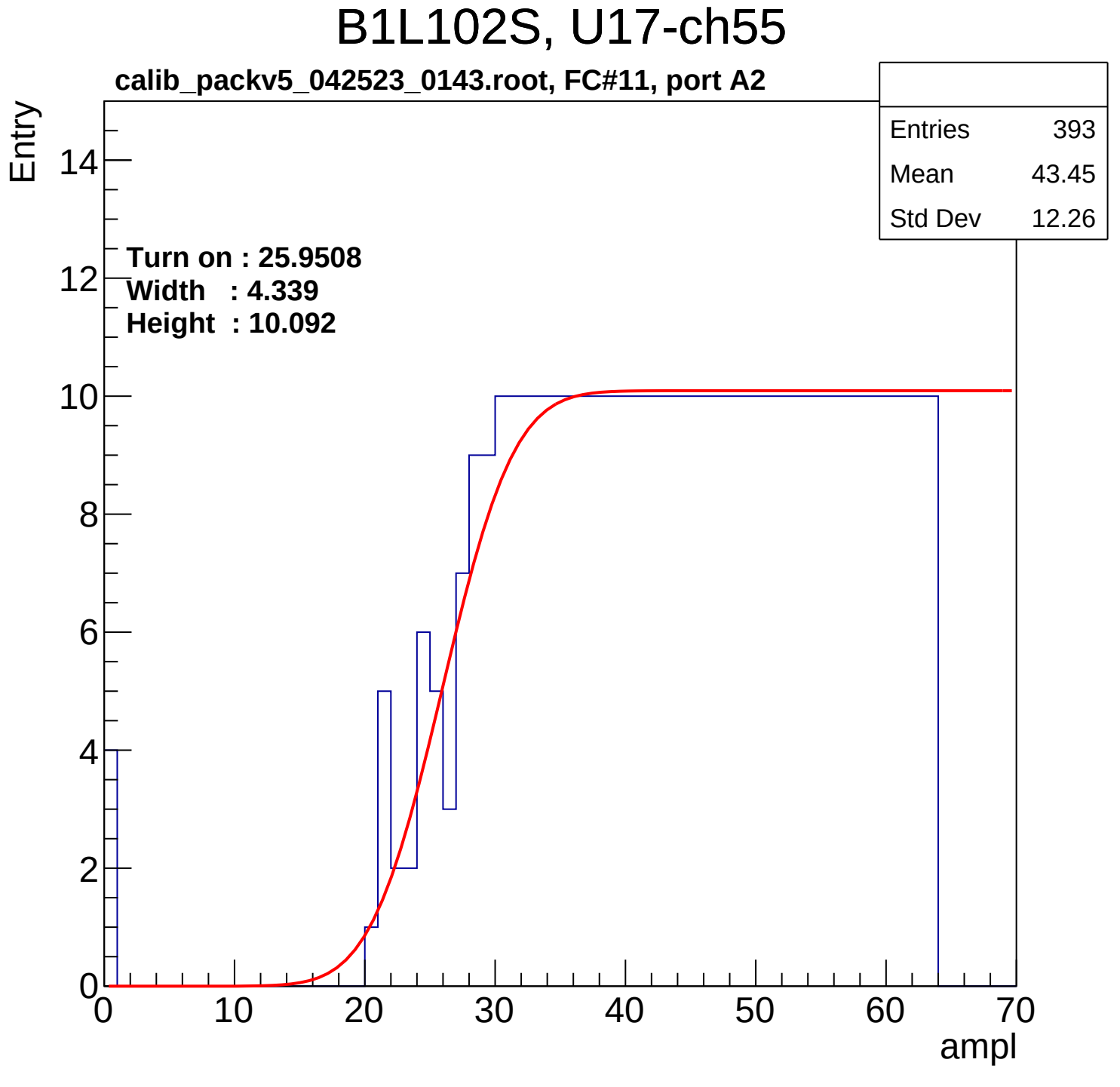
B1L102S, U17-ch55
calib_packv5_042523_0143.root, FC#11, port A2
Entries 393
Mean 43.45
Std Dev 12.26
Turn on : 25.9508
Width : 4.339
Height : 10.092
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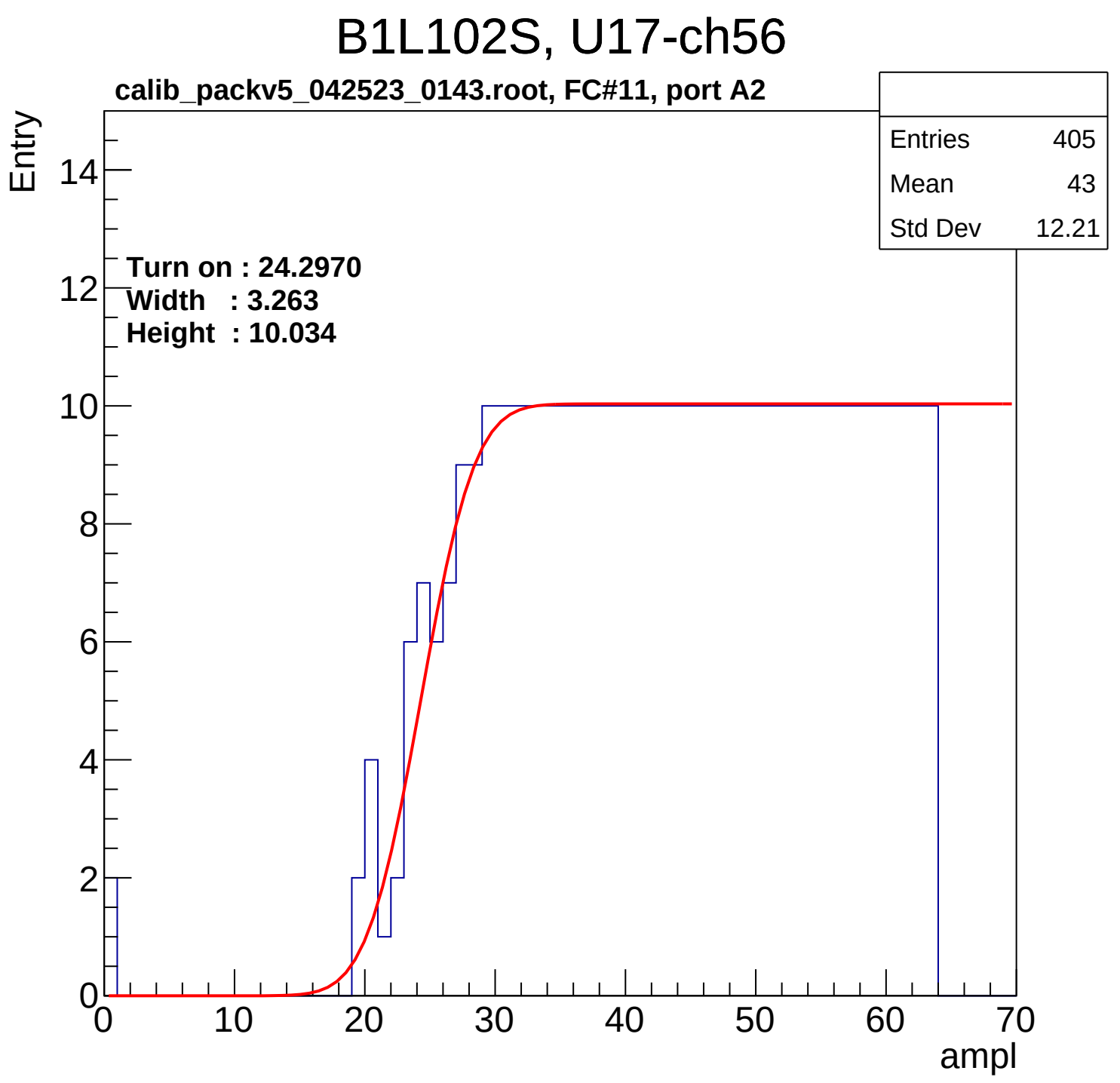
B1L102S, U17-ch56
calib_packv5_042523_0143.root, FC#11, port A2
Entries 405
Mean 43
Std Dev 12.21
Turn on : 24.2970
Width : 3.263
Height : 10.034
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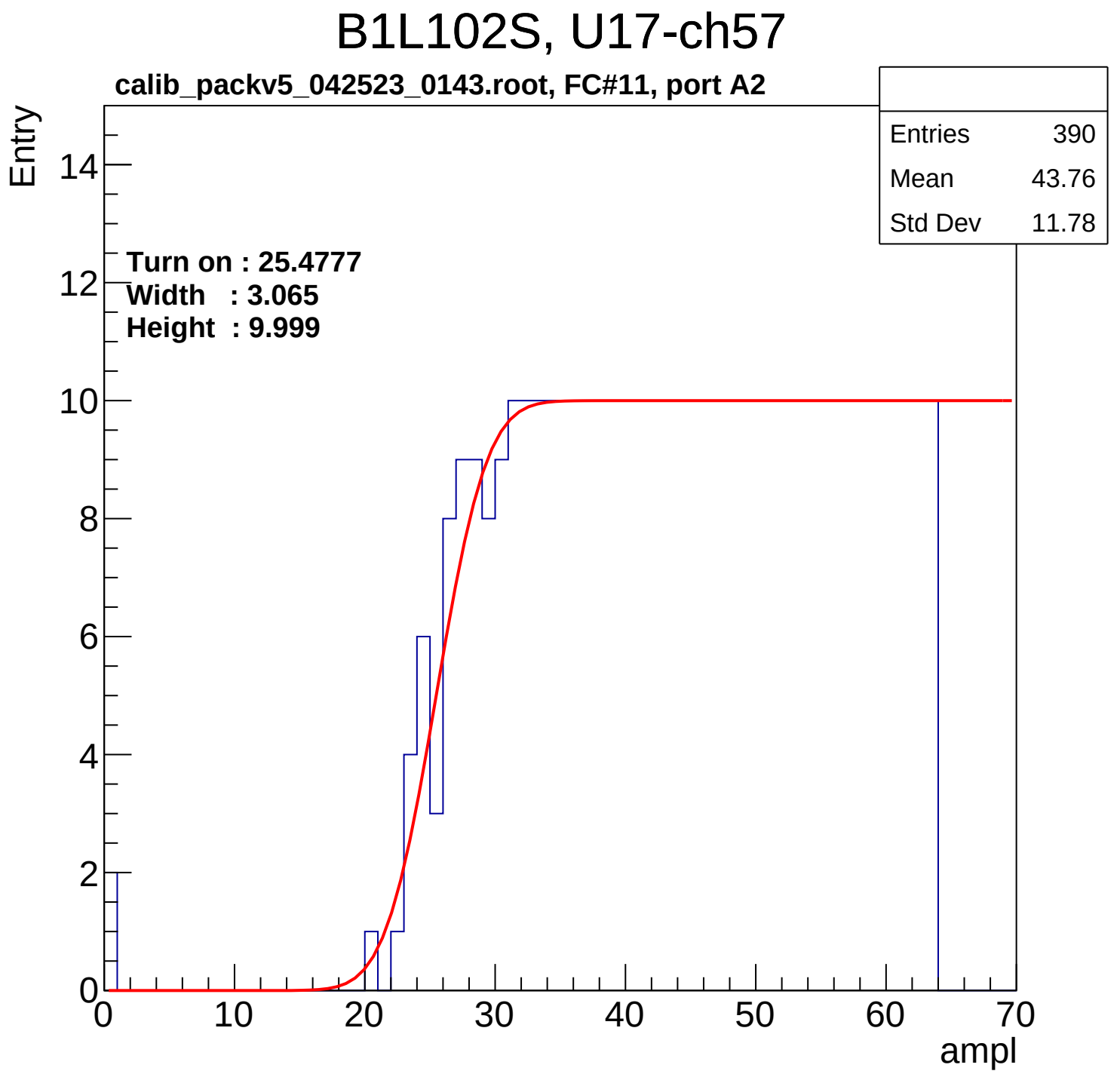
B1L102S, U17-ch57
calib_packv5_042523_0143.root, FC#11, port A2
Entries 390
Mean 43.76
Std Dev 11.78
Turn on : 25.4777
Width : 3.065
Height : 9.999
Entry
ampl
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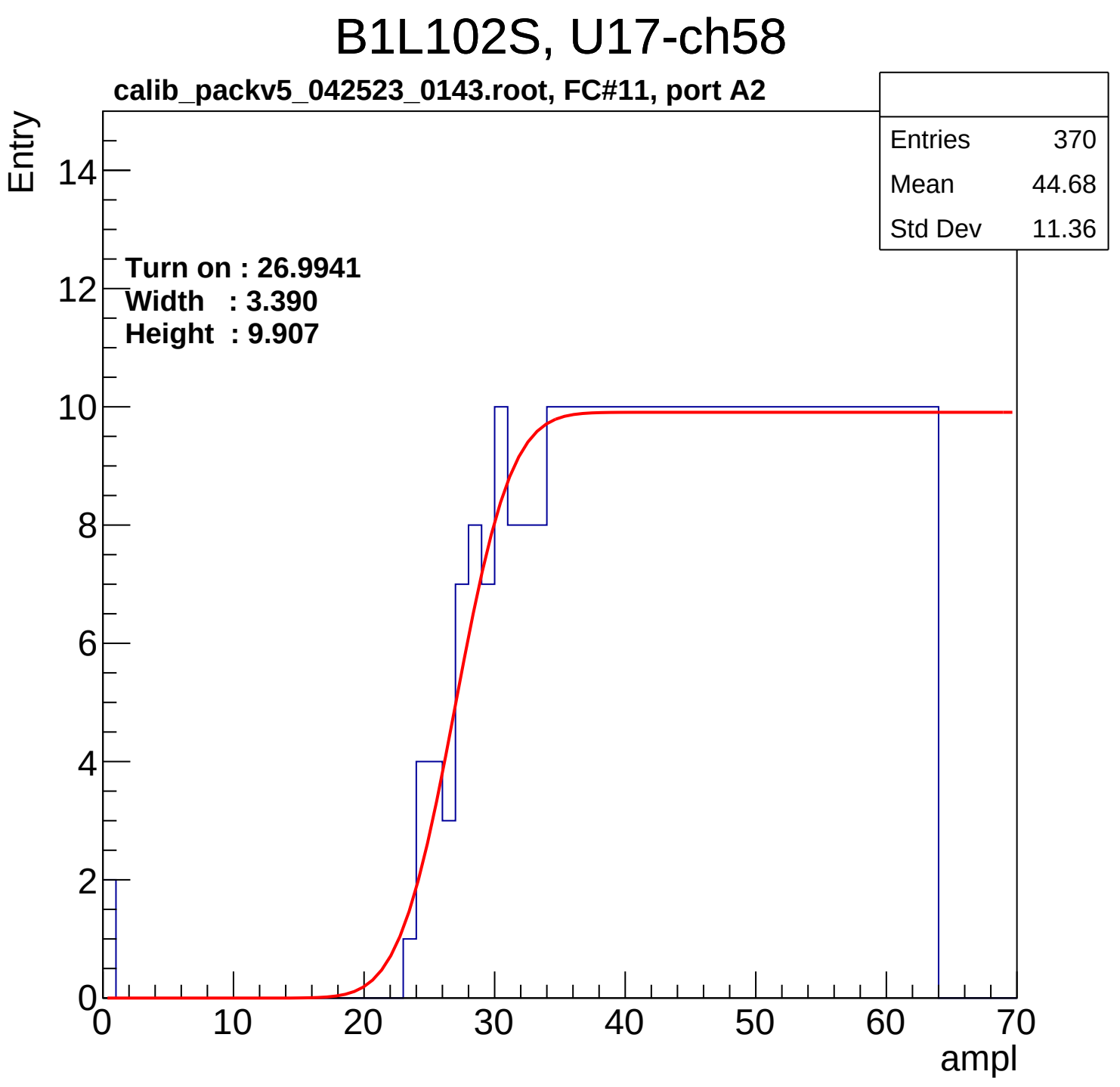
B1L102S, U17-ch58
calib_packv5_042523_0143.root, FC#11, port A2
Entries 370
Mean 44.68
Std Dev 11.36
Turn on : 26.9941
Width : 3.390
Height : 9.907
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ampl
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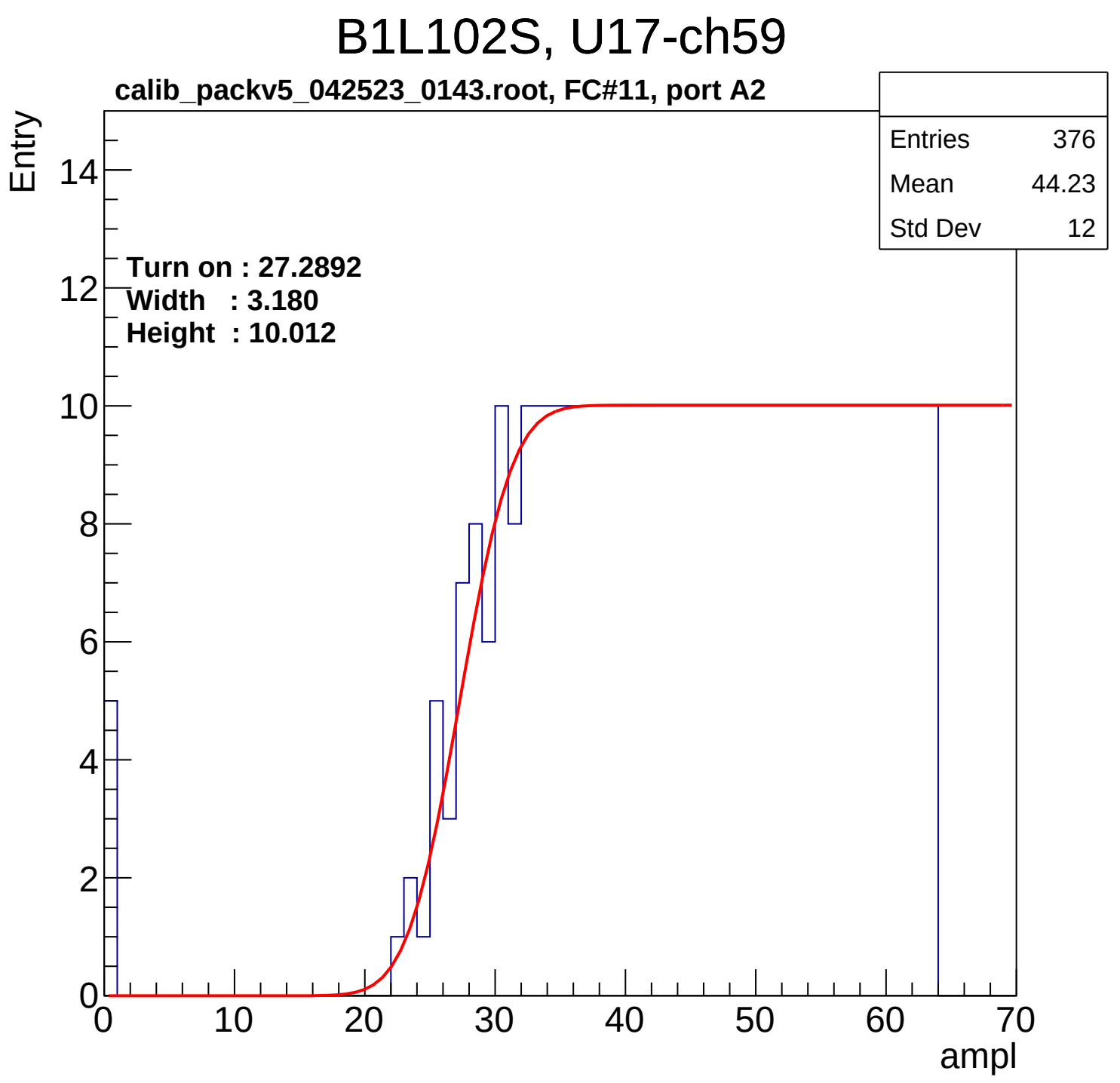
B1L102S, U17-ch59
calib_packv5_042523_0143.root, FC#11, port A2
Entries 376
Mean 44.23
Std Dev 12
Turn on : 27.2892
Width : 3.180
Height : 10.012
Entry
ampl
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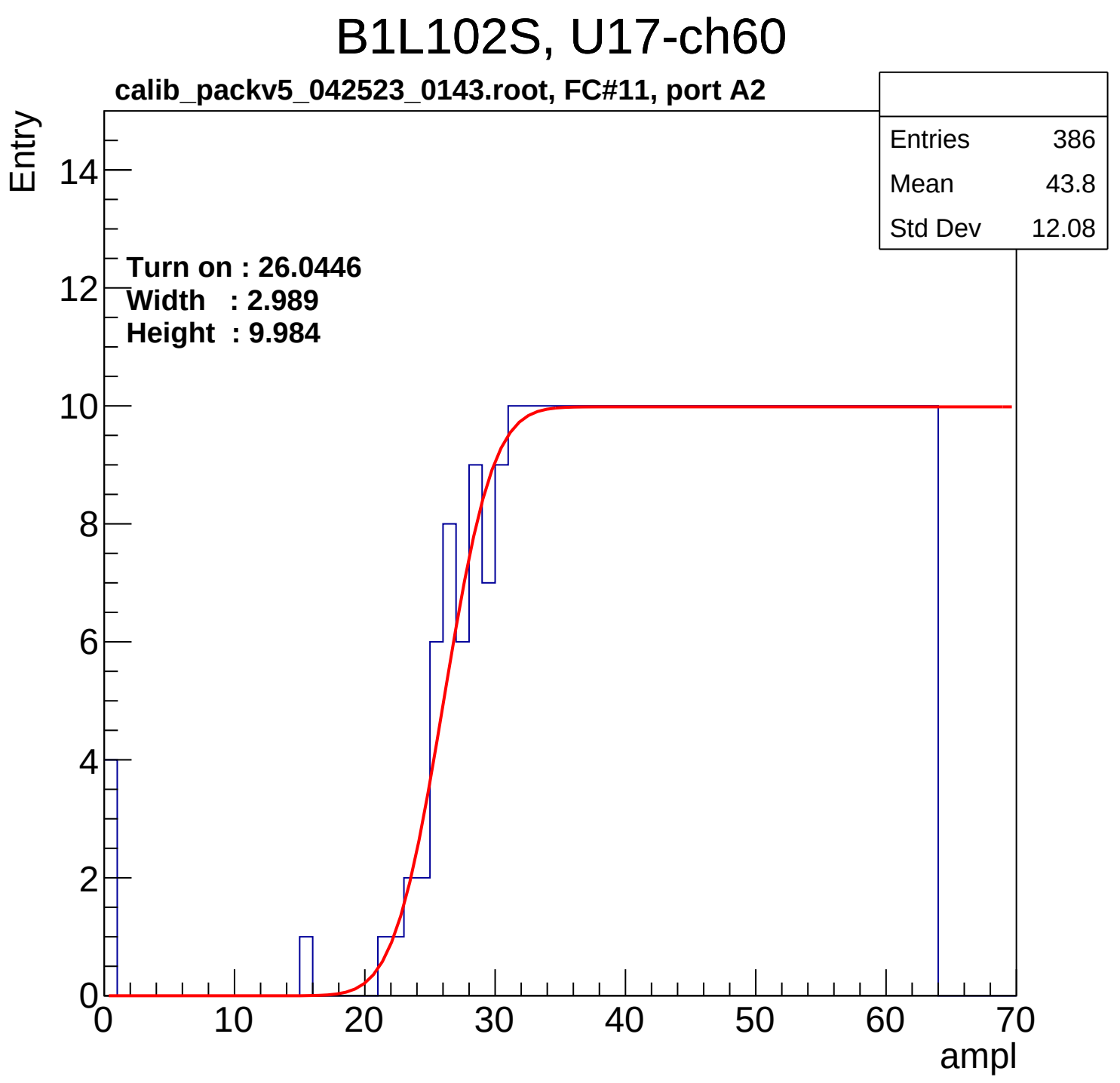
B1L102S, U17-ch60
calib_packv5_042523_0143.root, FC#11, port A2
Entries 386
Mean 43.8
Std Dev 12.08
Turn on : 26.0446
Width : 2.989
Height : 9.984
Entry
ampl
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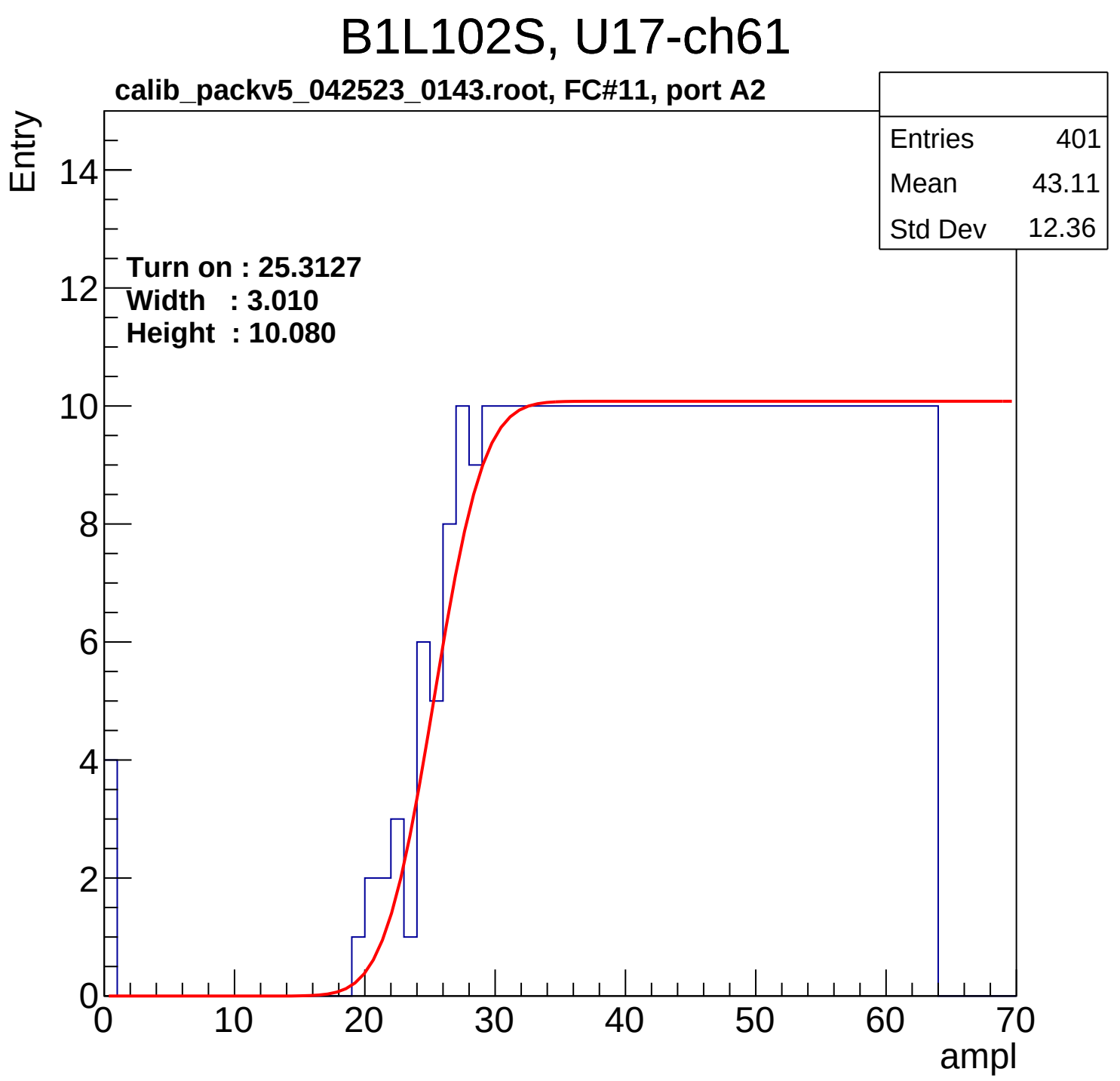
B1L102S, U17-ch61
calib_packv5_042523_0143.root, FC#11, port A2
Entries 401
Mean 43.11
Std Dev 12.36
Turn on : 25.3127
Width : 3.010
Height : 10.080
Entry
ampl
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2
4
6
8
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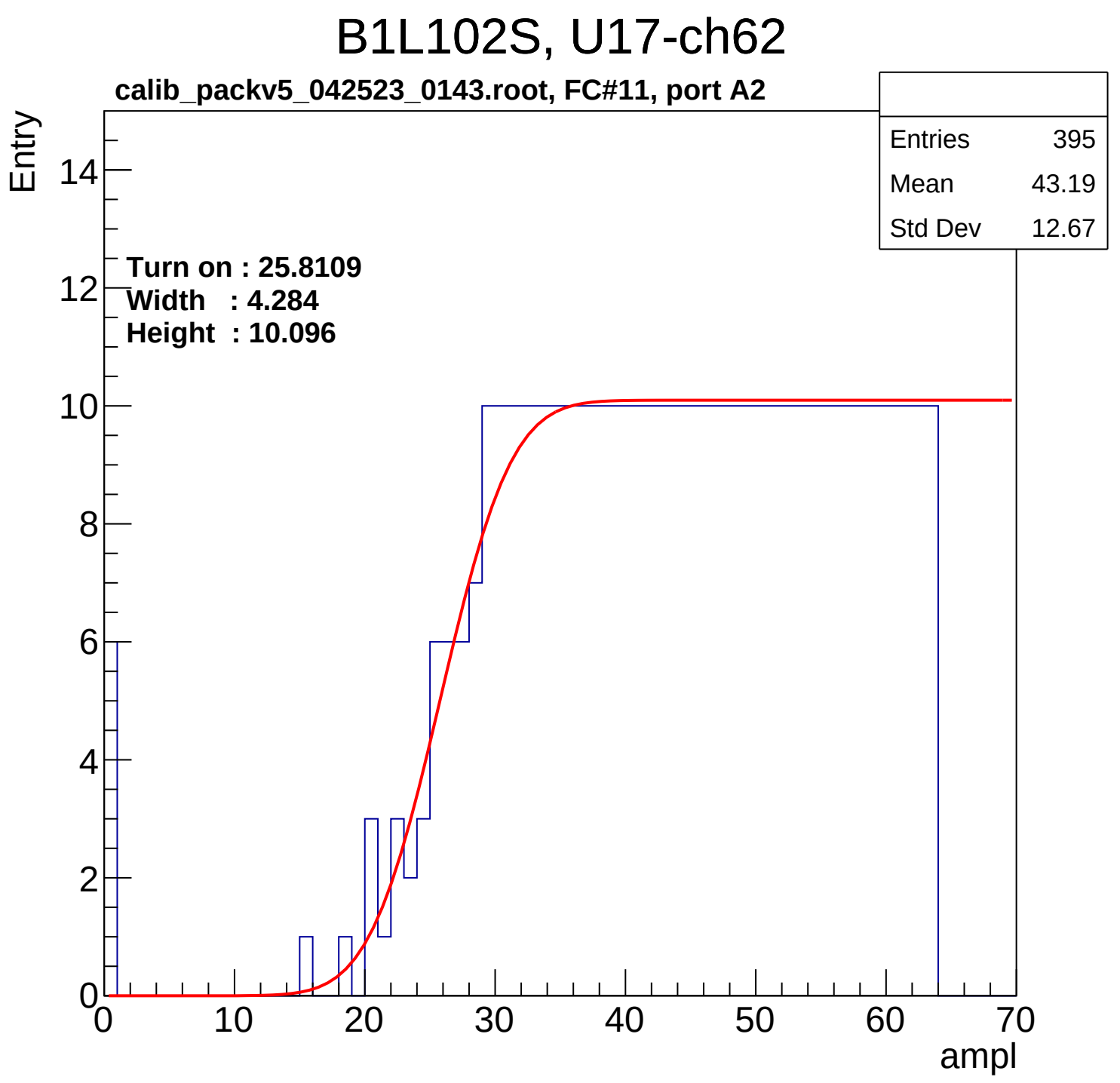
B1L102S, U17-ch62
calib_packv5_042523_0143.root, FC#11, port A2
Entries 395
Mean 43.19
Std Dev 12.67
Turn on : 25.8109
Width : 4.284
Height : 10.096
Entry
ampl
0
2
4
6
8
10
12
14
0
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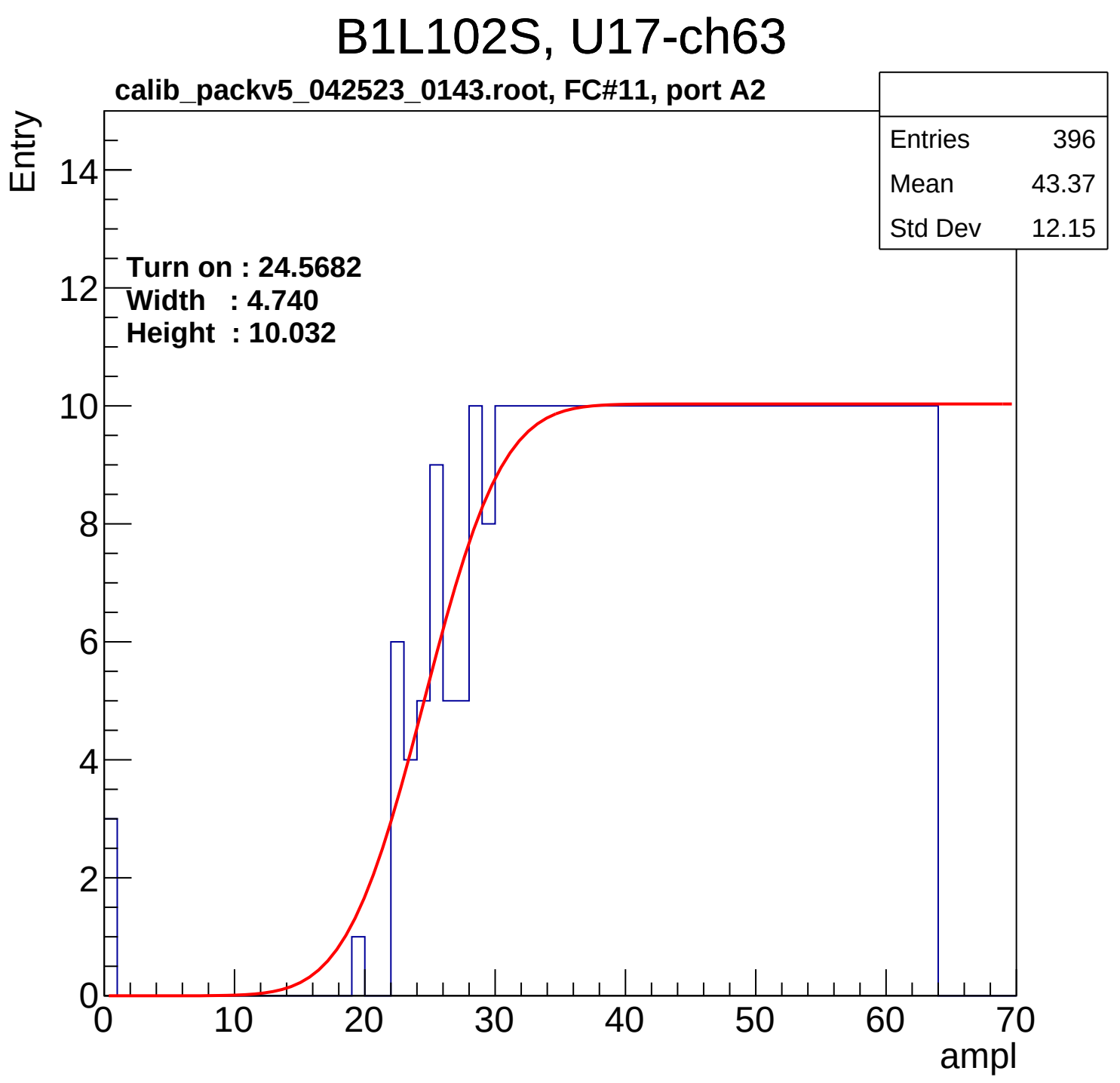
B1L102S, U17-ch63
calib_packv5_042523_0143.root, FC#11, port A2
Entries 396
Mean 43.37
Std Dev 12.15
Turn on : 24.5682
Width : 4.740
Height : 10.032
Entry
ampl
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2
4
6
8
10
12
14
0
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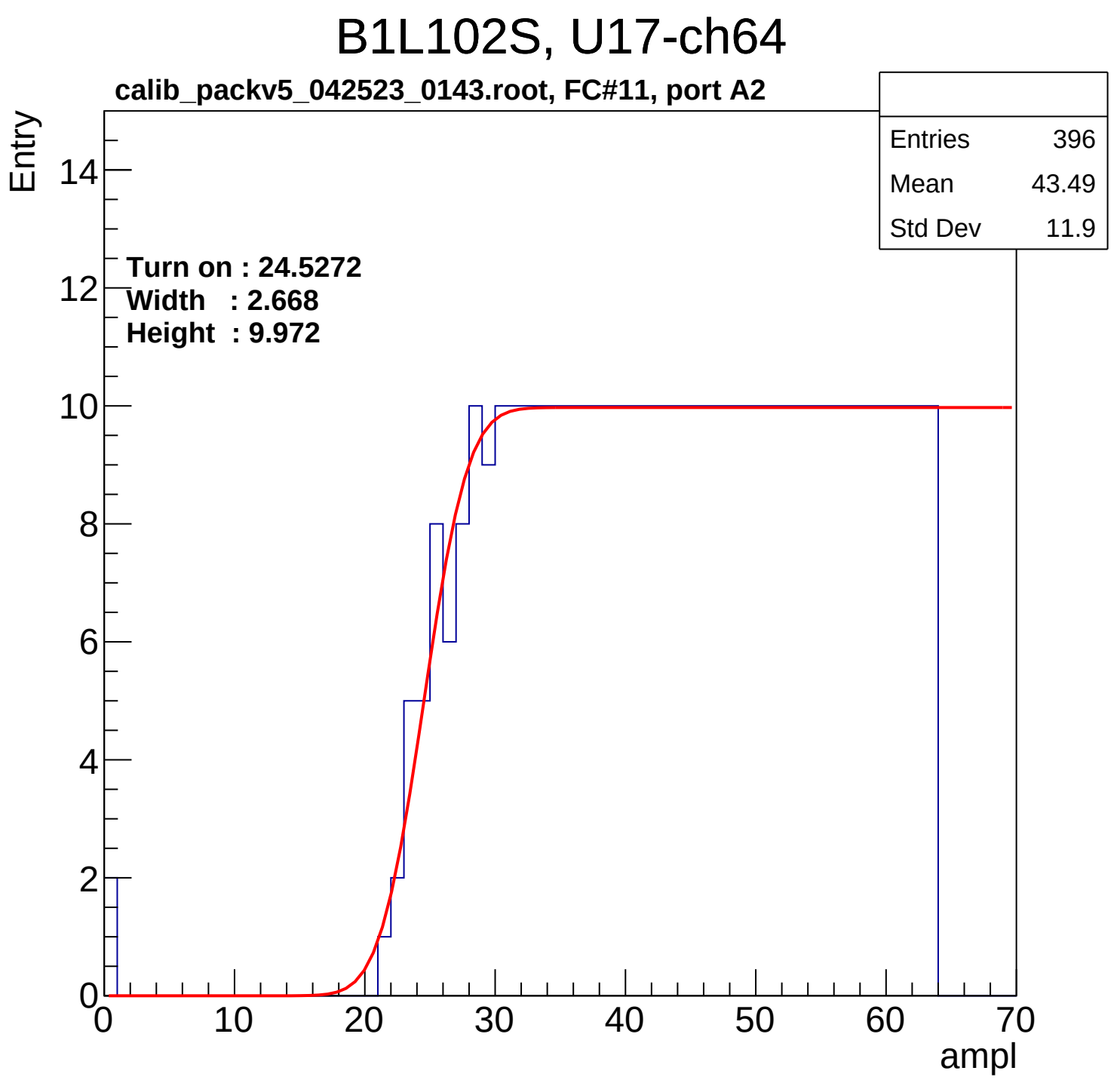
B1L102S, U17-ch64
calib_packv5_042523_0143.root, FC#11, port A2
Entries 396
Mean 43.49
Std Dev 11.9
Turn on : 24.5272
Width : 2.668
Height : 9.972
Entry
ampl
0
2
4
6
8
10
12
14
0
10
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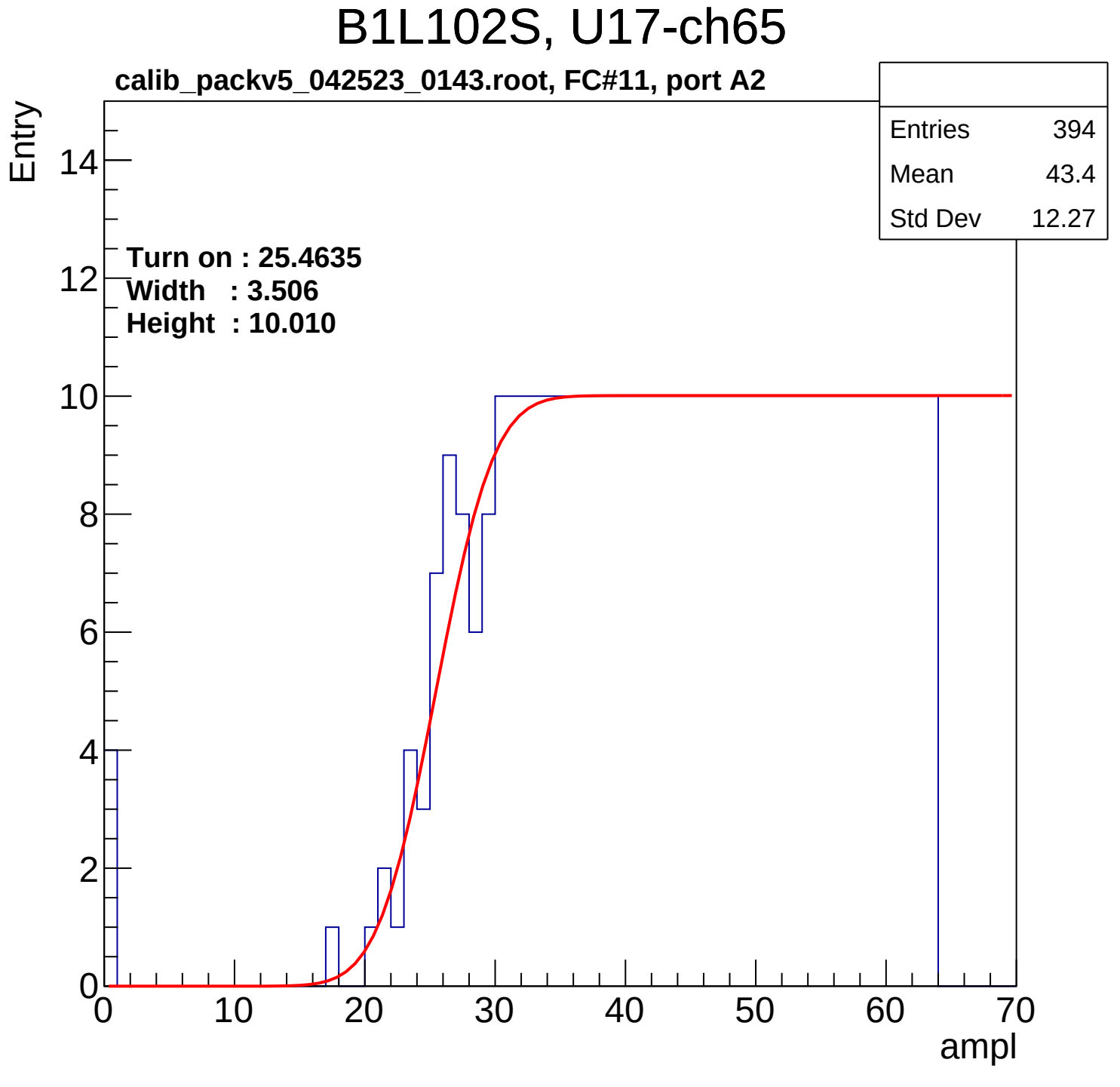
B1L102S, U17-ch65
calib_packv5_042523_0143.root, FC#11, port A2
Entries 394
Mean 43.4
Std Dev 12.27
Turn on : 25.4635
Width : 3.506
Height : 10.010
Entry
ampl
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2
4
6
8
10
12
14
0
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60
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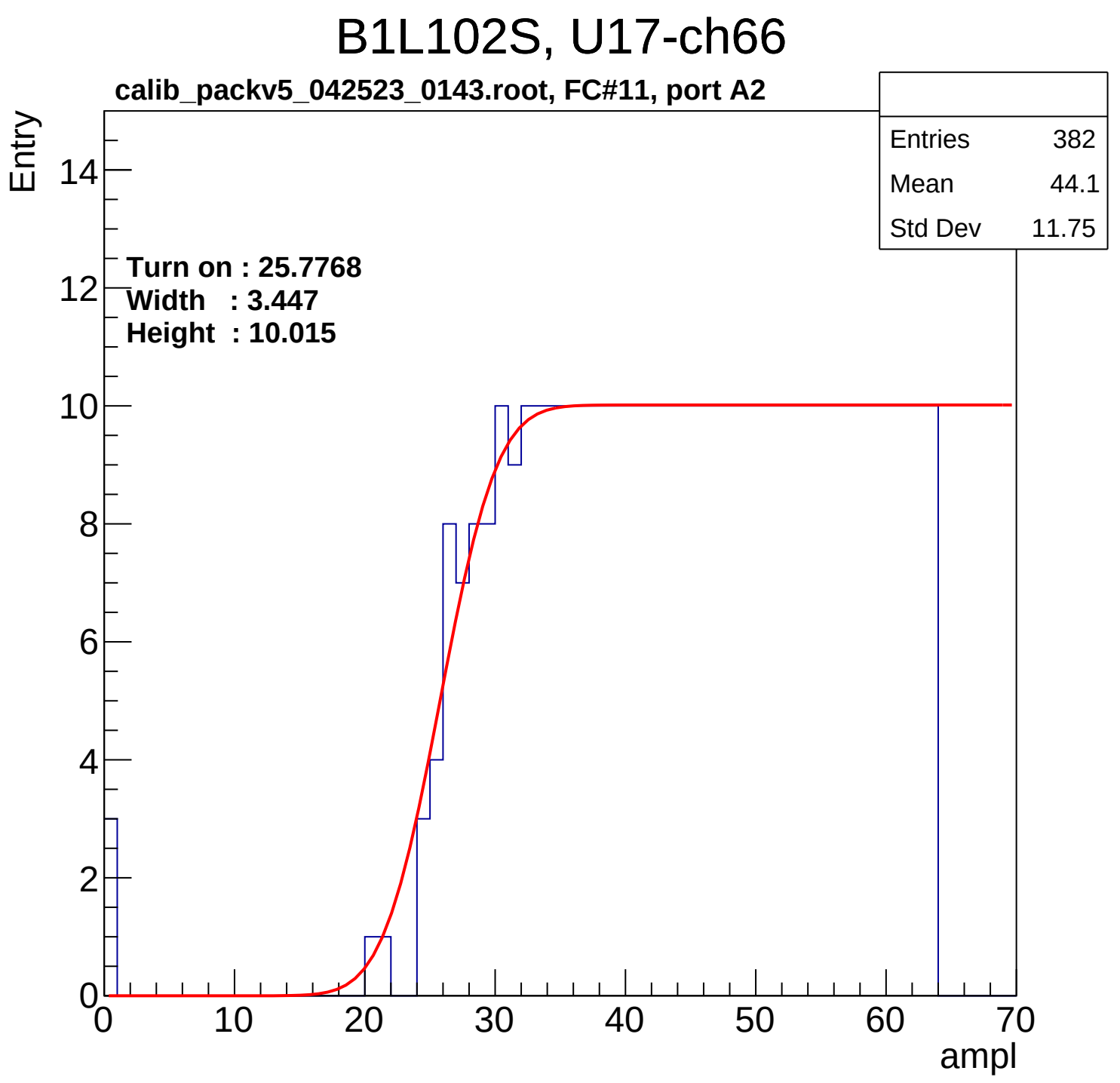
B1L102S, U17-ch66
calib_packv5_042523_0143.root, FC#11, port A2
Entries 382
Mean 44.1
Std Dev 11.75
Turn on : 25.7768
Width : 3.447
Height : 10.015
Entry
ampl
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2
4
6
8
10
12
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0
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20
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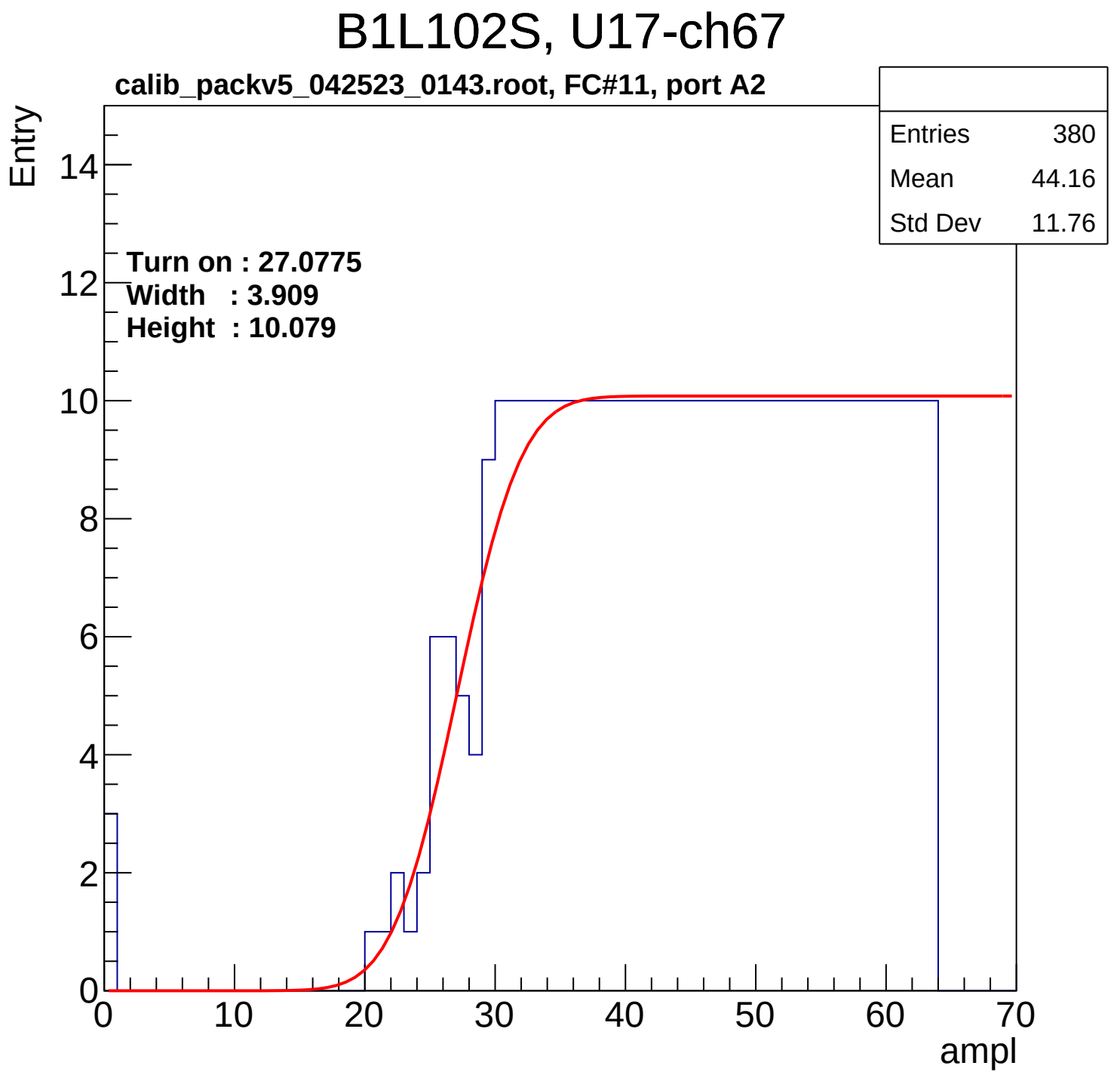
B1L102S, U17-ch67
calib_packv5_042523_0143.root, FC#11, port A2
Entries 380
Mean 44.16
Std Dev 11.76
Turn on : 27.0775
Width : 3.909
Height : 10.079
Entry
ampl
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2
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6
8
10
12
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0
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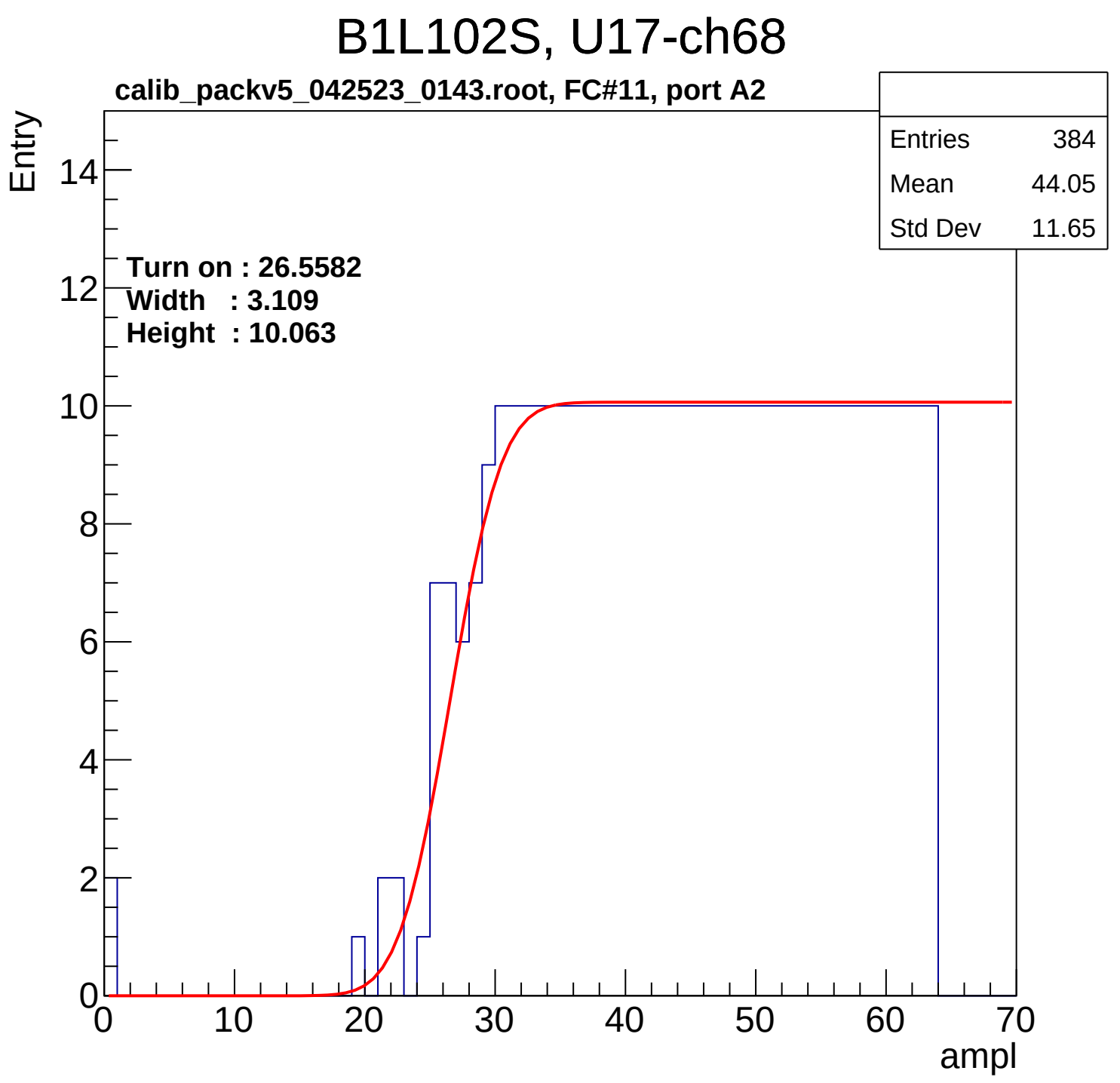
B1L102S, U17-ch68
calib_packv5_042523_0143.root, FC#11, port A2
Entries 384
Mean 44.05
Std Dev 11.65
Turn on : 26.5582
Width : 3.109
Height : 10.063
Entry
ampl
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6
8
10
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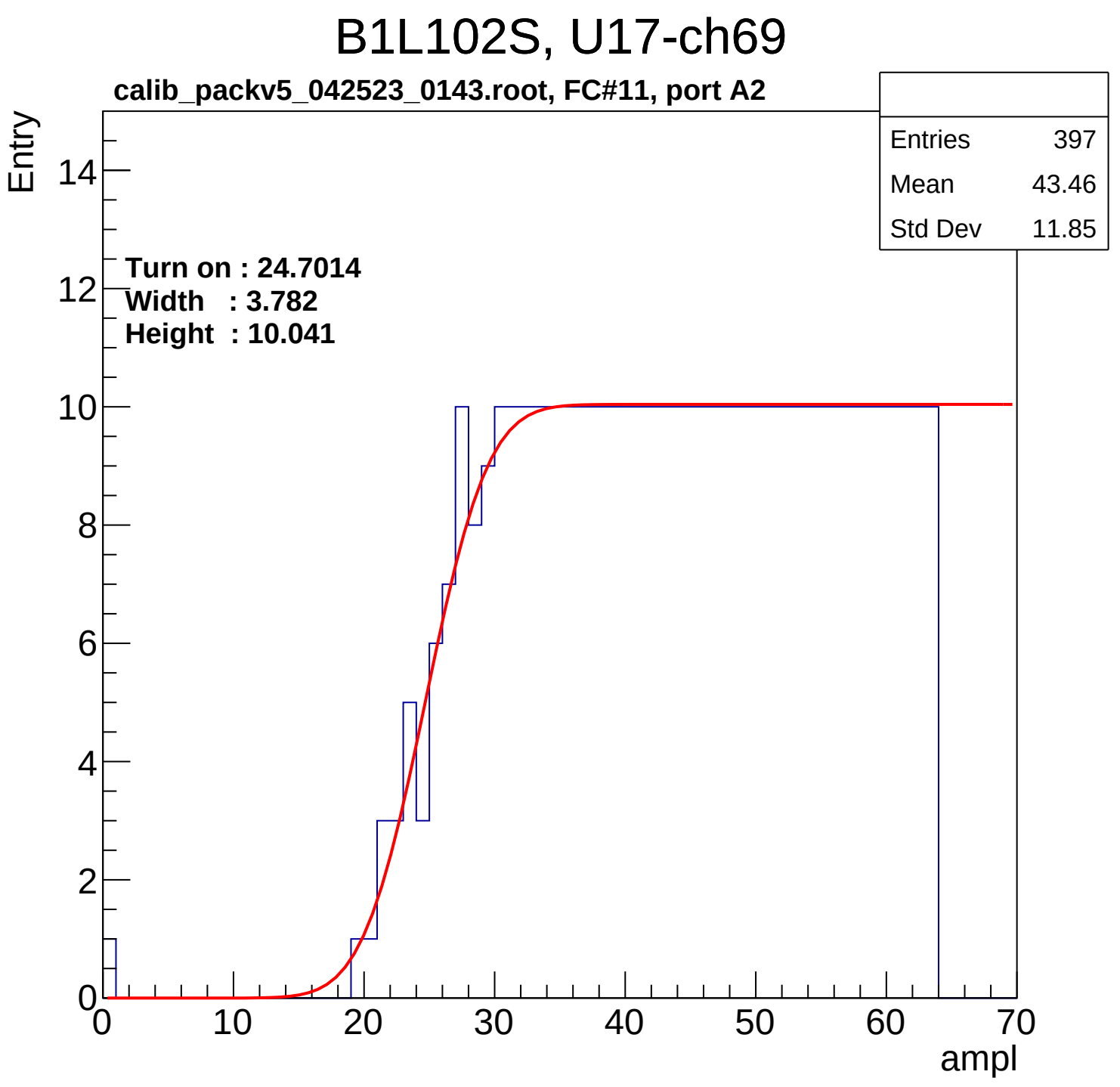
B1L102S, U17-ch69
calib_packv5_042523_0143.root, FC#11, port A2
Entries 397
Mean 43.46
Std Dev 11.85
Turn on : 24.7014
Width : 3.782
Height : 10.041
Entry
ampl
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6
8
10
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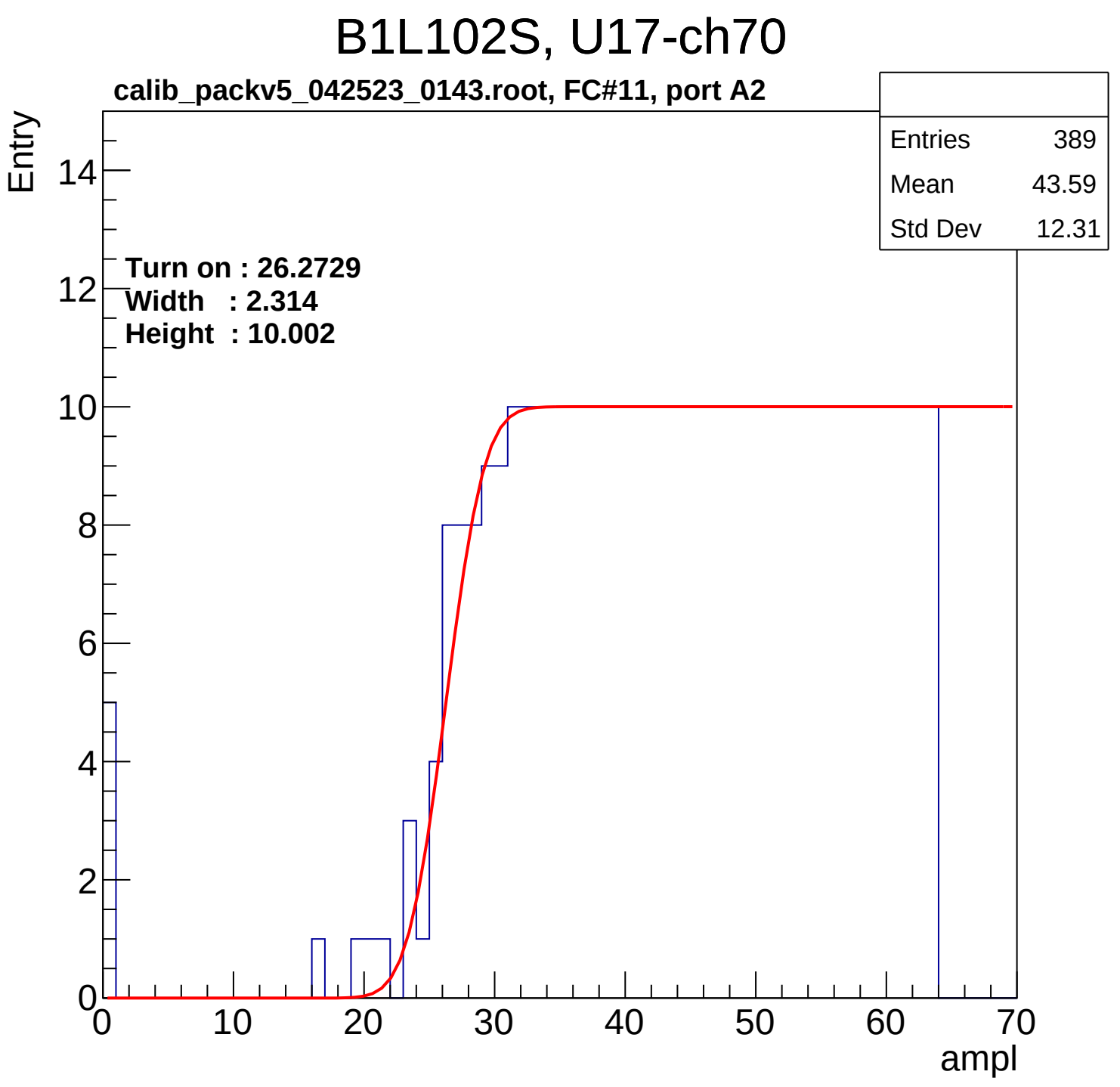
B1L102S, U17-ch70
calib_packv5_042523_0143.root, FC#11, port A2
Entries 389
Mean 43.59
Std Dev 12.31
Turn on : 26.2729
Width : 2.314
Height : 10.002
Entry
ampl
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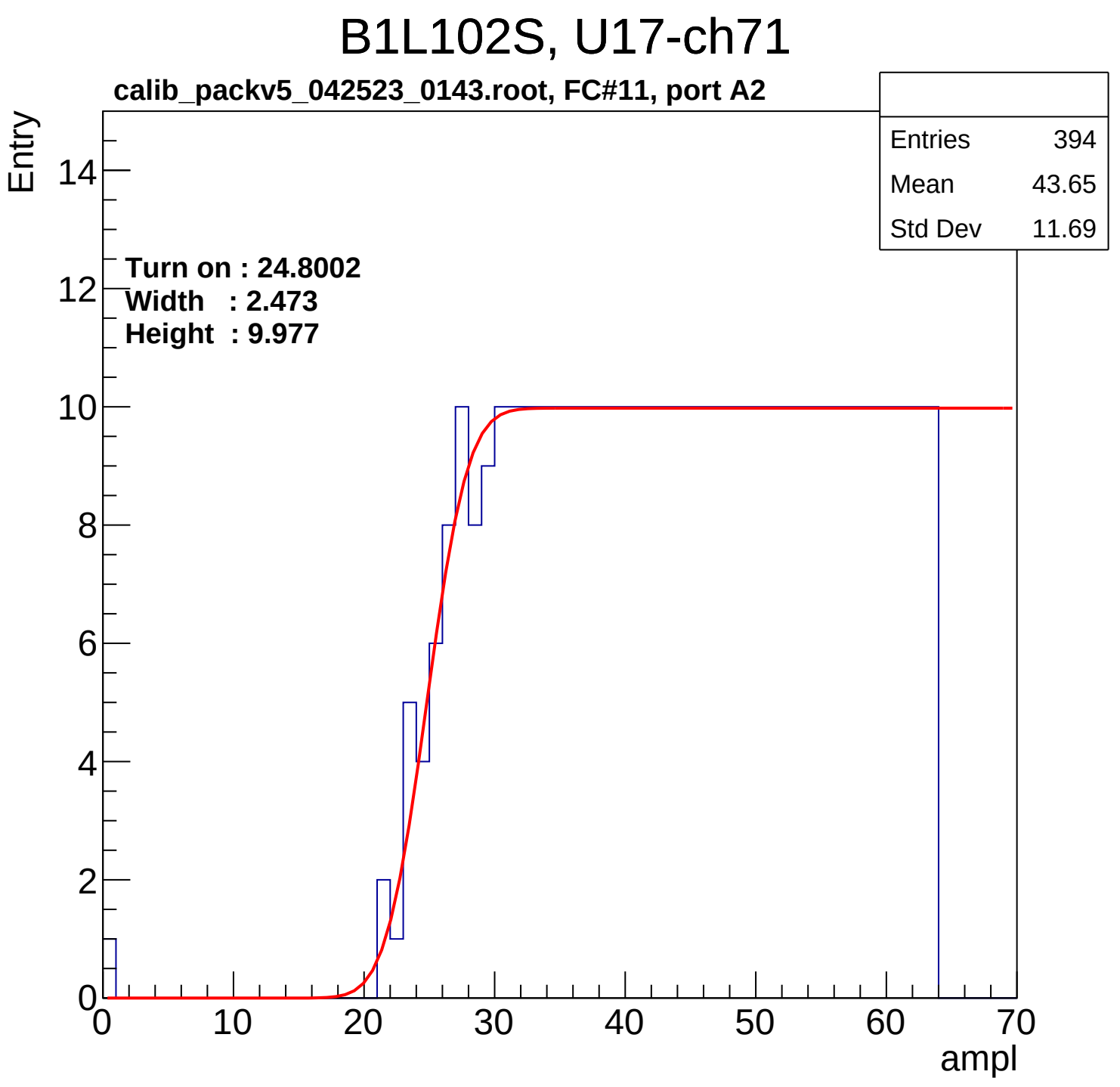
B1L102S, U17-ch71
calib_packv5_042523_0143.root, FC#11, port A2
Entries 394
Mean 43.65
Std Dev 11.69
Turn on : 24.8002
Width : 2.473
Height : 9.977
Entry
ampl
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8
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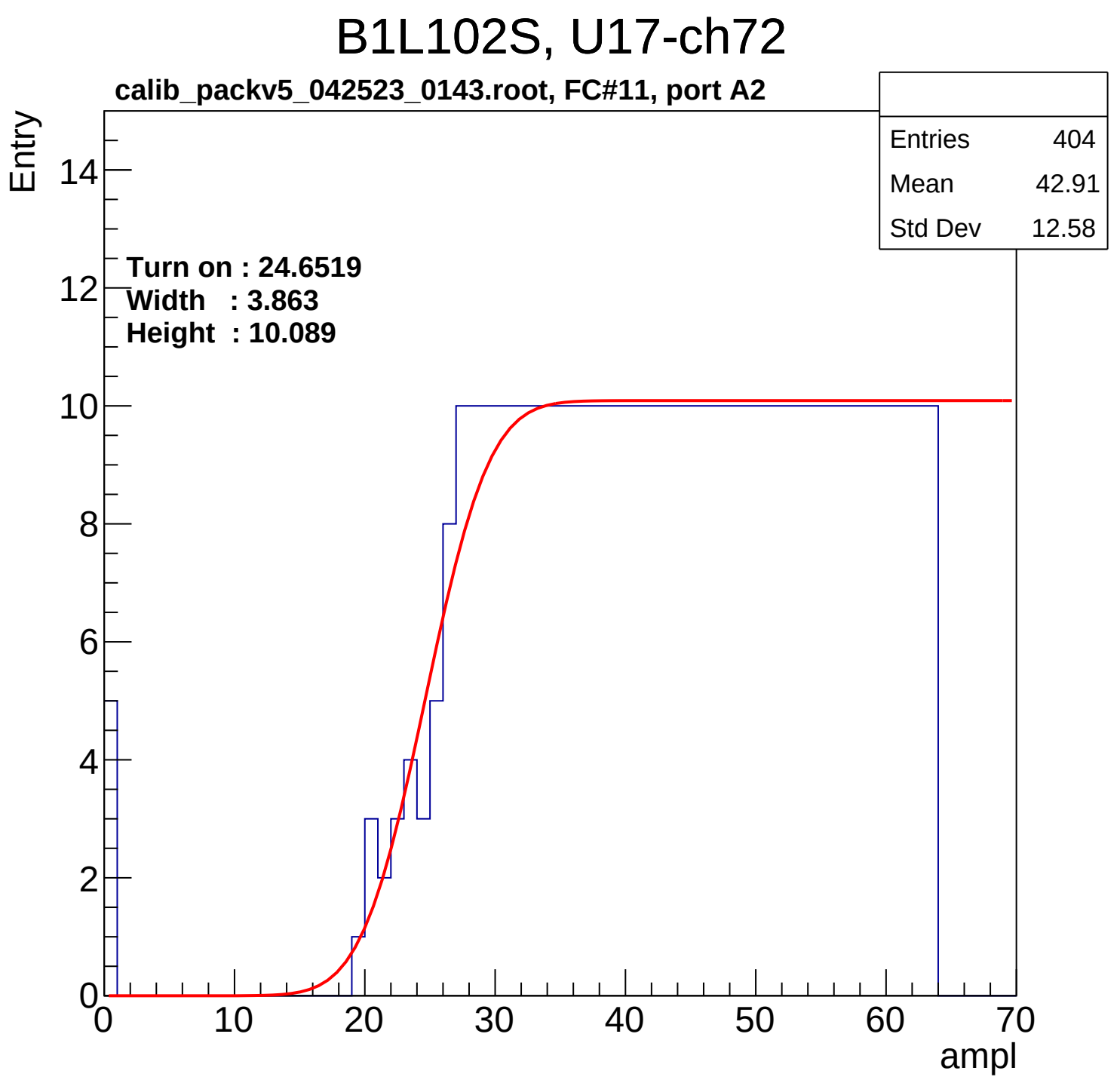
B1L102S, U17-ch72
calib_packv5_042523_0143.root, FC#11, port A2
Entries 404
Mean 42.91
Std Dev 12.58
Turn on : 24.6519
Width : 3.863
Height : 10.089
Entry
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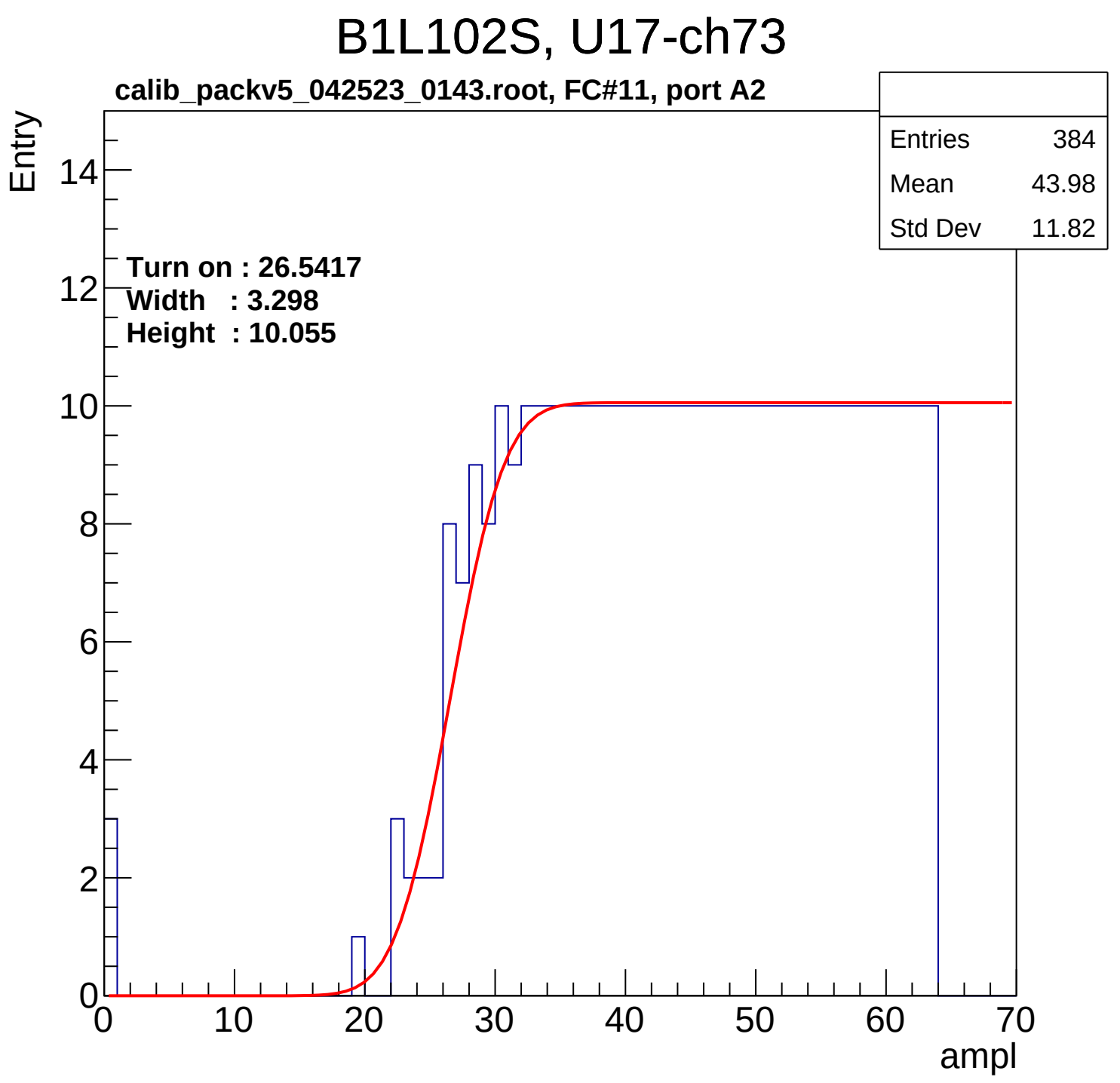
B1L102S, U17-ch73
calib_packv5_042523_0143.root, FC#11, port A2
Entries 384
Mean 43.98
Std Dev 11.82
Turn on : 26.5417
Width : 3.298
Height : 10.055
Entry
ampl
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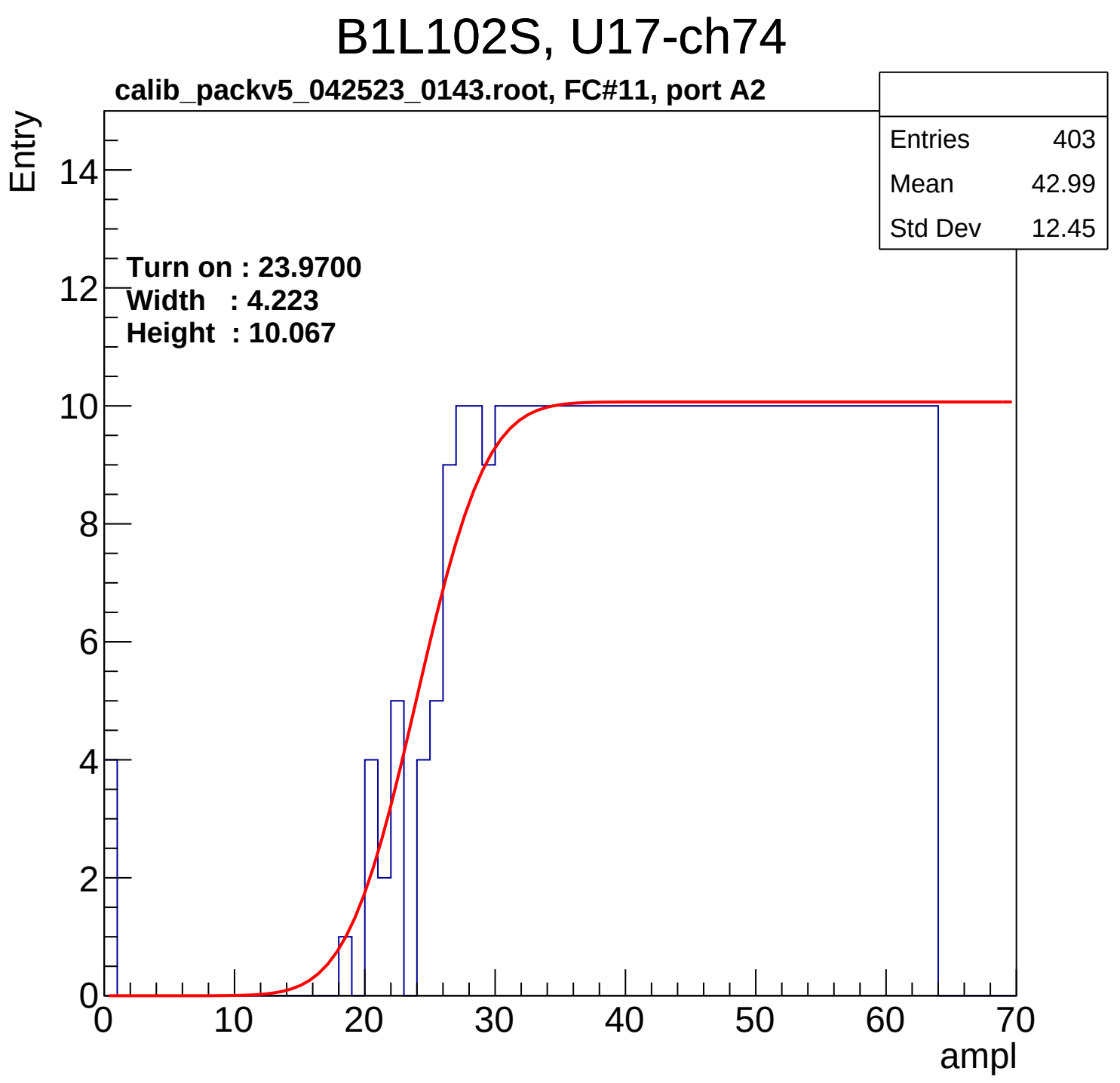
B1L102S, U17-ch74
calib_packv5_042523_0143.root, FC#11, port A2
Entries 403
Mean 42.99
Std Dev 12.45
Turn on : 23.9700
Width : 4.223
Height : 10.067
Entry
ampl
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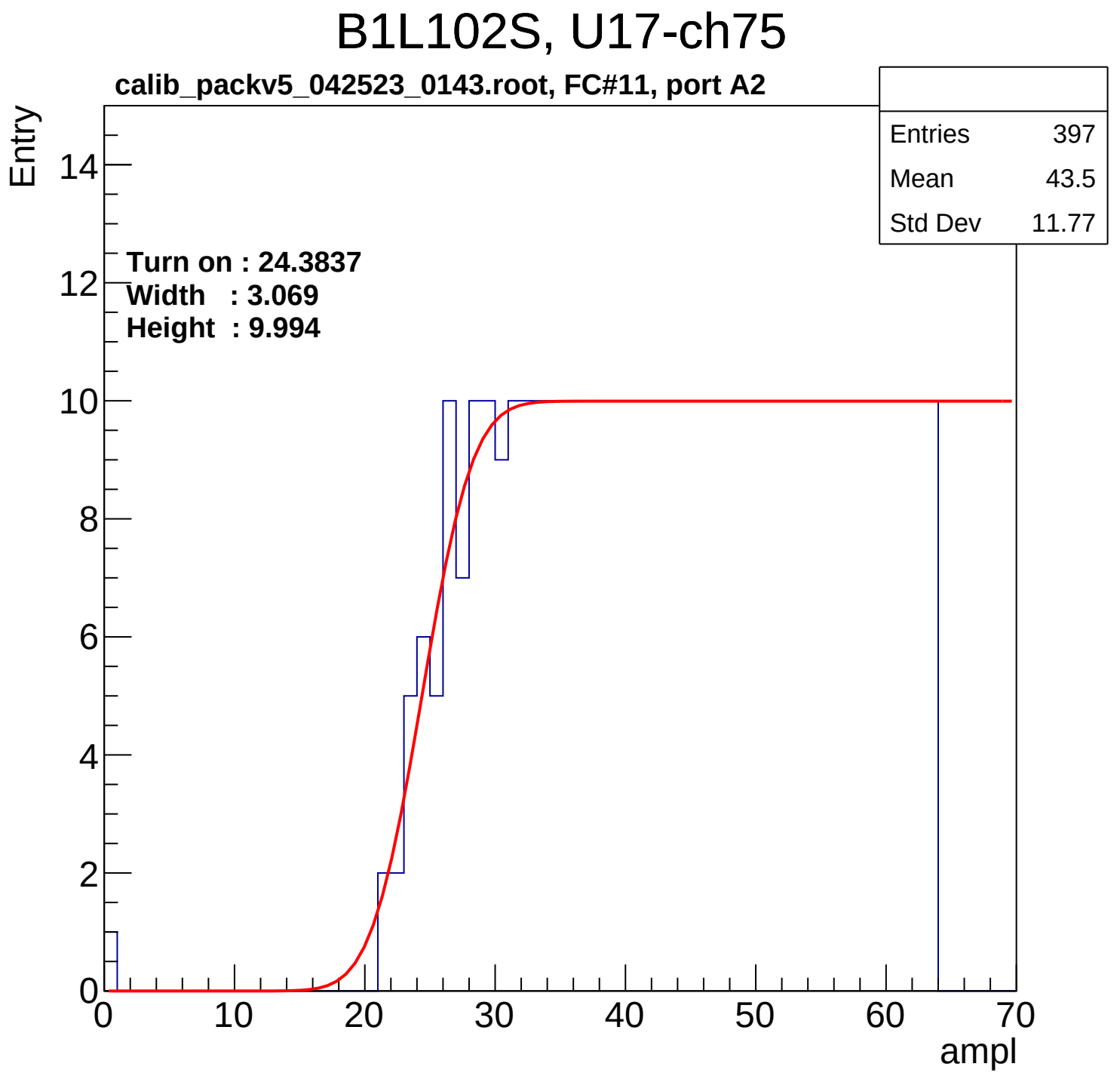
B1L102S, U17-ch75
calib_packv5_042523_0143.root, FC#11, port A2
Entries 397
Mean 43.5
Std Dev 11.77
Turn on : 24.3837
Width : 3.069
Height : 9.994
Entry
ampl
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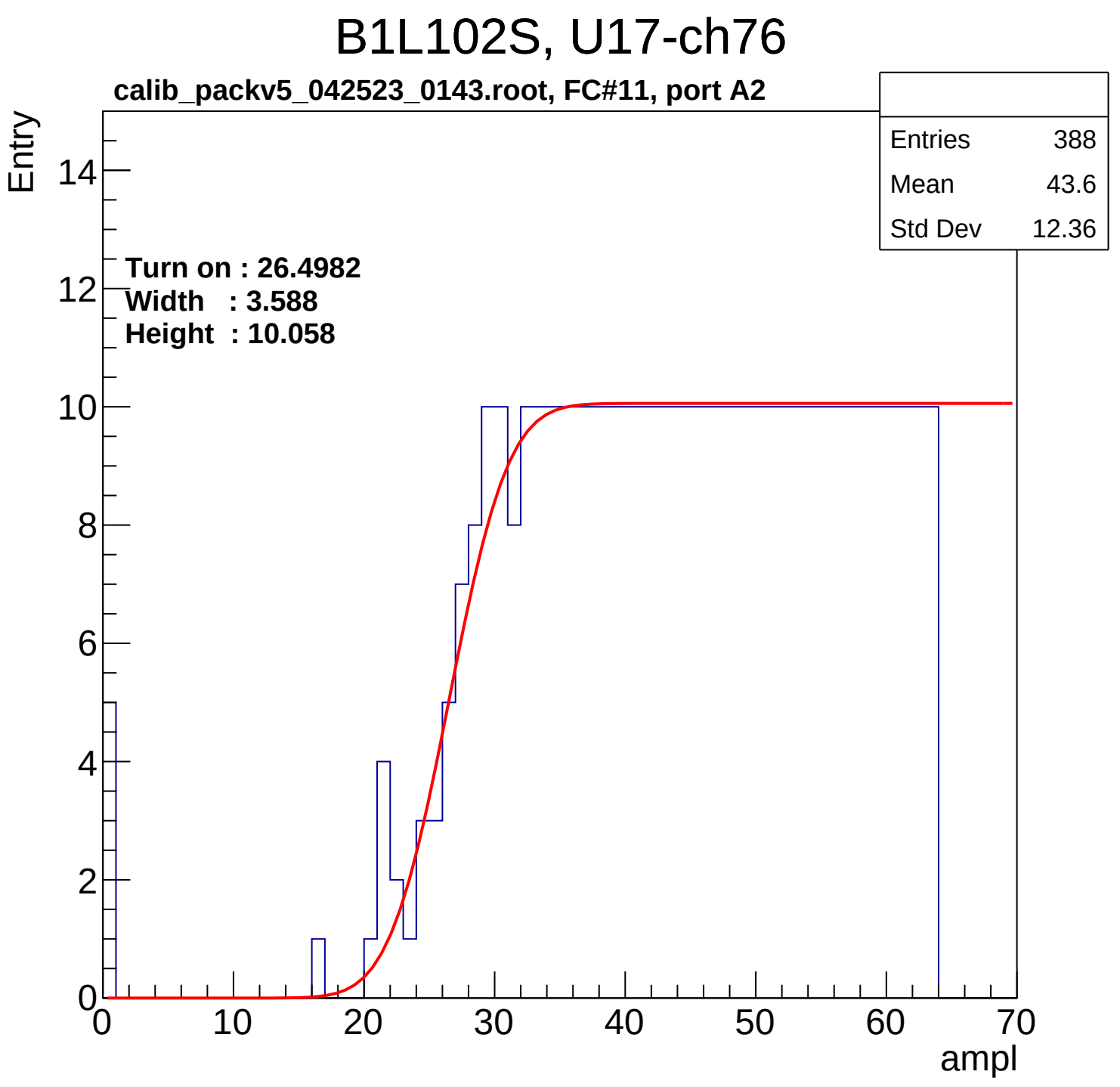
B1L102S, U17-ch76
calib_packv5_042523_0143.root, FC#11, port A2
Entries 388
Mean 43.6
Std Dev 12.36
Turn on : 26.4982
Width : 3.588
Height : 10.058
Entry
ampl
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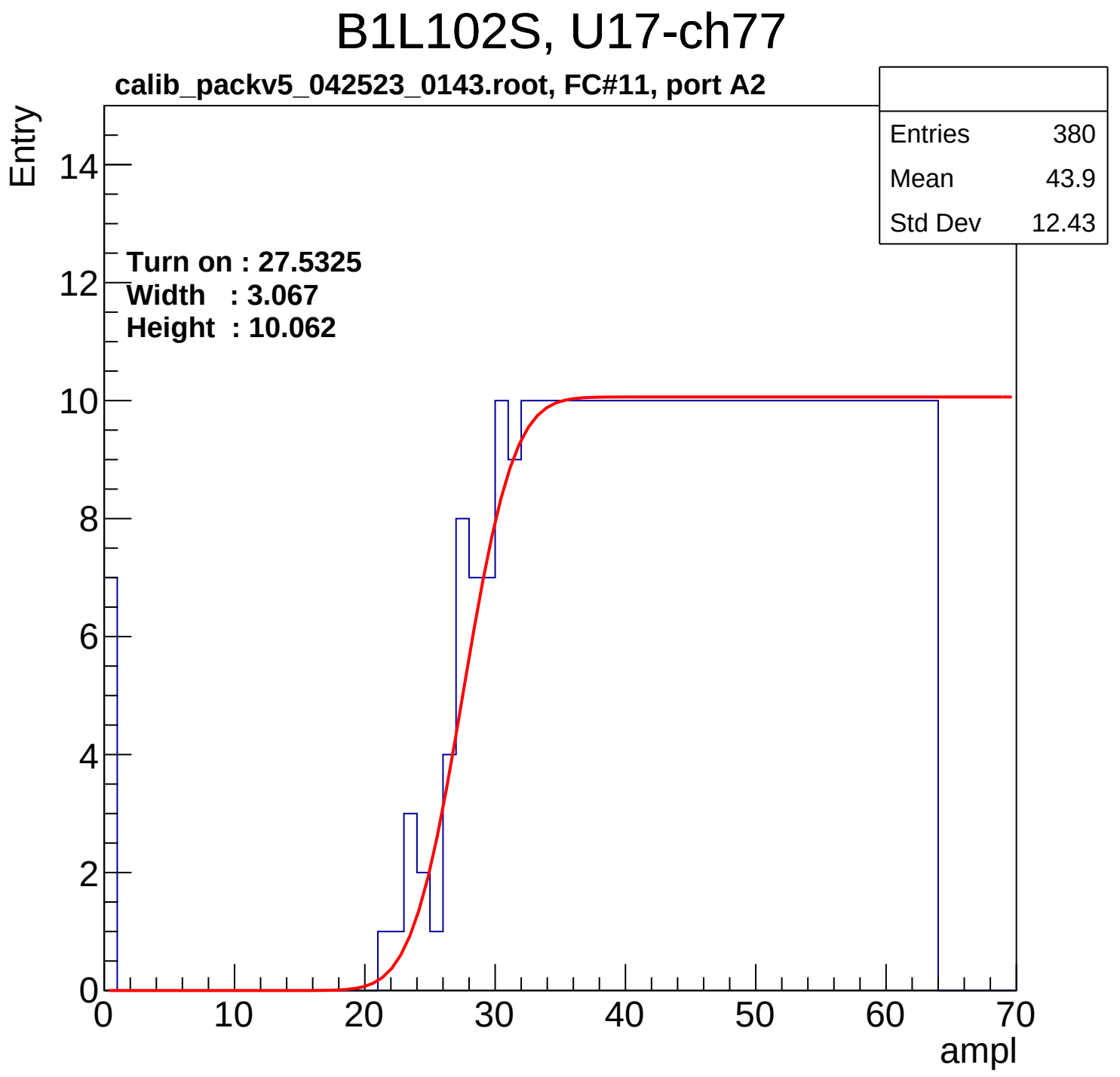
B1L102S, U17-ch77
calib_packv5_042523_0143.root, FC#11, port A2
Entries 380
Mean 43.9
Std Dev 12.43
Turn on : 27.5325
Width : 3.067
Height : 10.062
Entry
ampl
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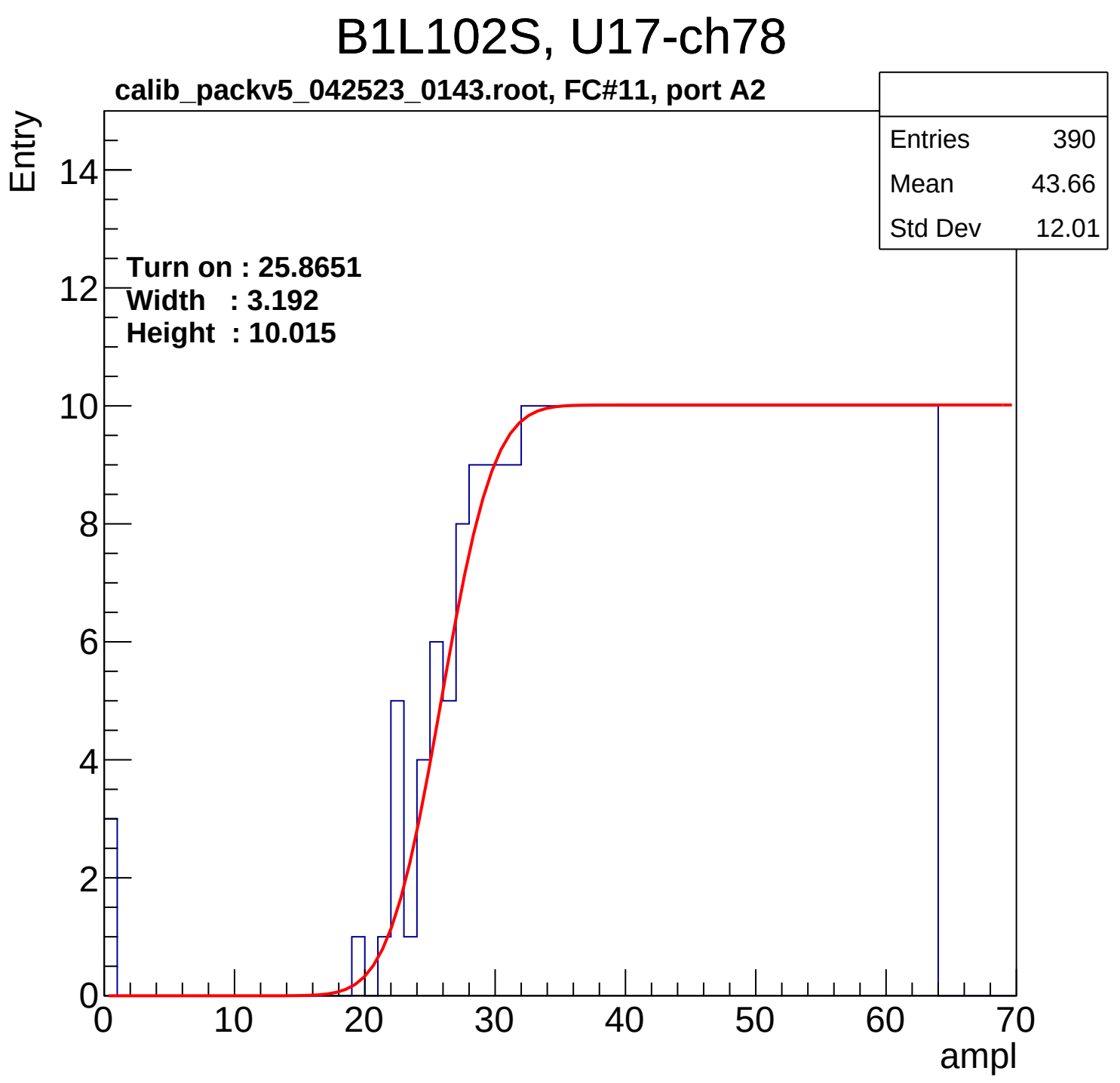
B1L102S, U17-ch78
calib_packv5_042523_0143.root, FC#11, port A2
Entries 390
Mean 43.66
Std Dev 12.01
Turn on : 25.8651
Width : 3.192
Height : 10.015
Entry
ampl
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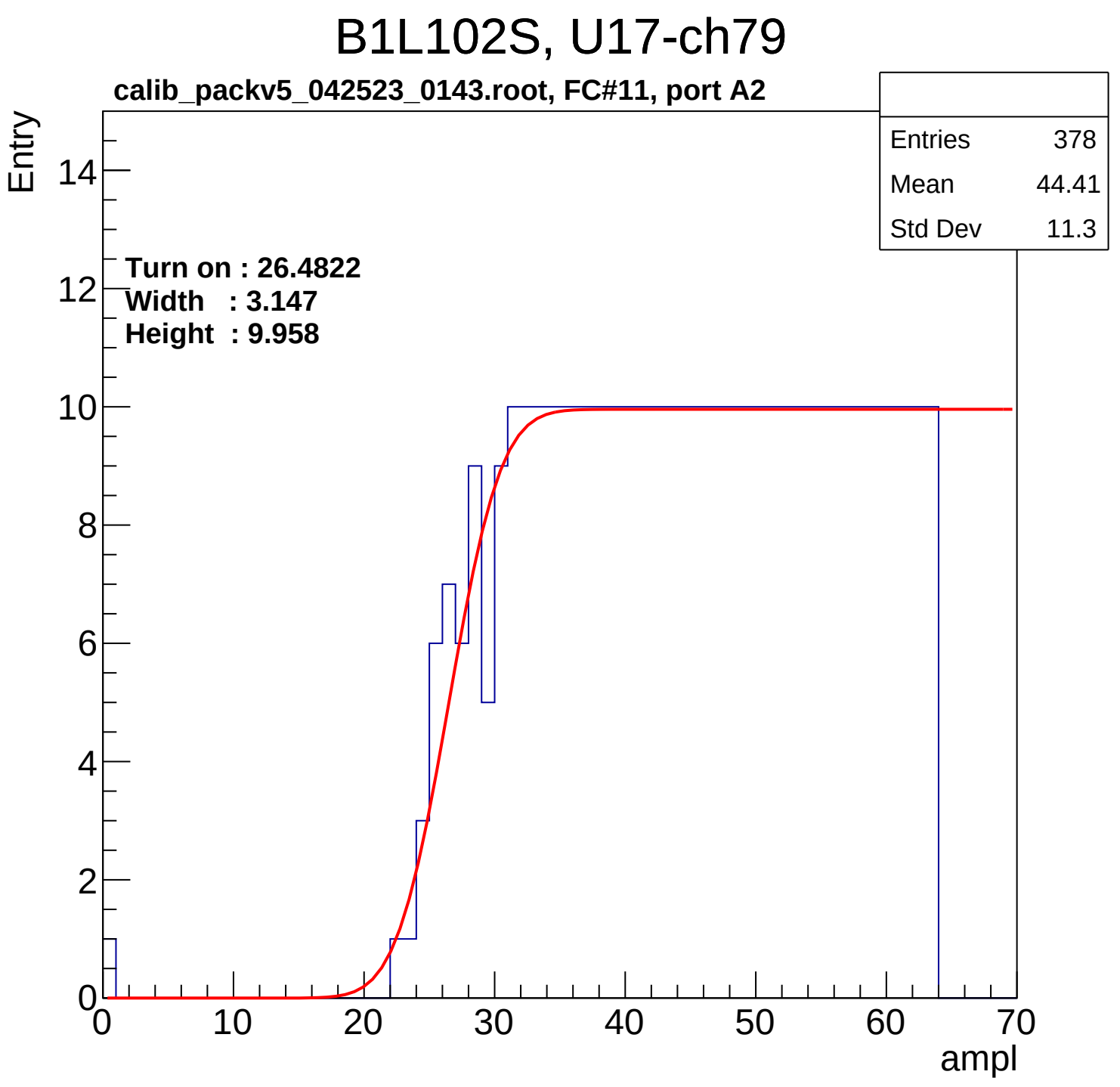
B1L102S, U17-ch79
calib_packv5_042523_0143.root, FC#11, port A2
Entries 378
Mean 44.41
Std Dev 11.3
Turn on : 26.4822
Width : 3.147
Height : 9.958
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ampl
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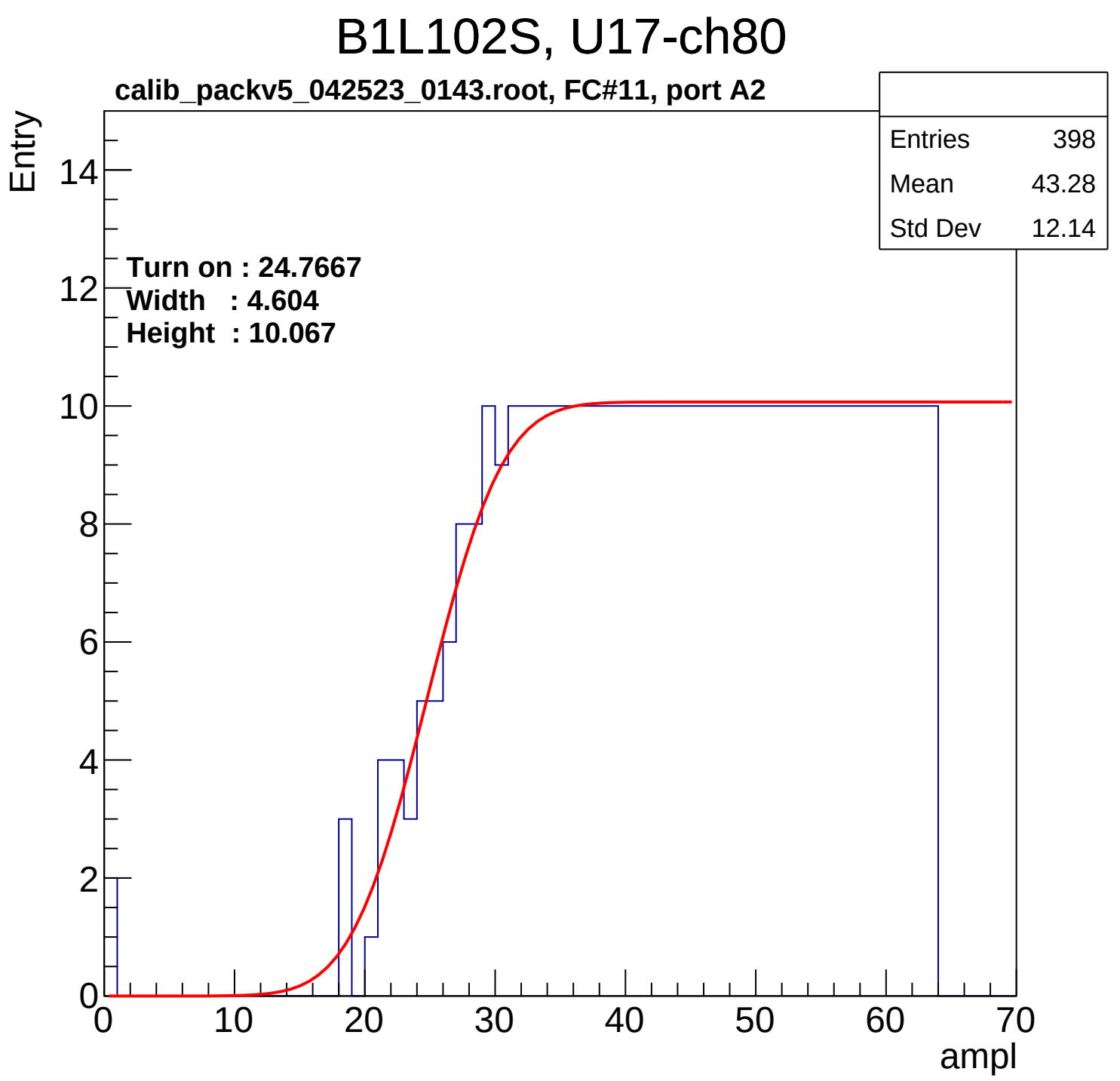
B1L102S, U17-ch80
calib_packv5_042523_0143.root, FC#11, port A2
Entries 398
Mean 43.28
Std Dev 12.14
Turn on : 24.7667
Width : 4.604
Height : 10.067
Entry
ampl
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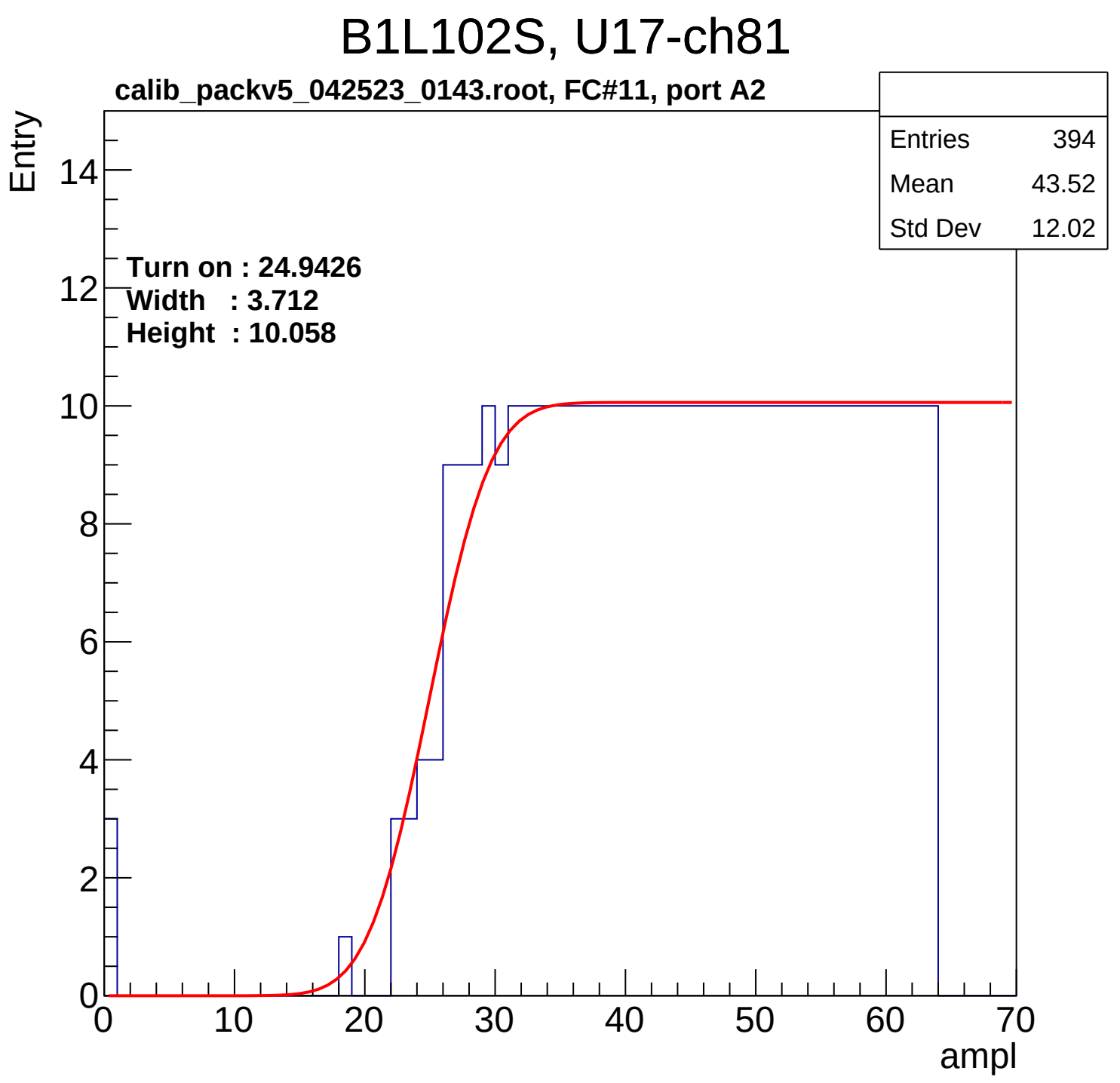
B1L102S, U17-ch81
calib_packv5_042523_0143.root, FC#11, port A2
Entries 394
Mean 43.52
Std Dev 12.02
Turn on : 24.9426
Width : 3.712
Height : 10.058
Entry
ampl
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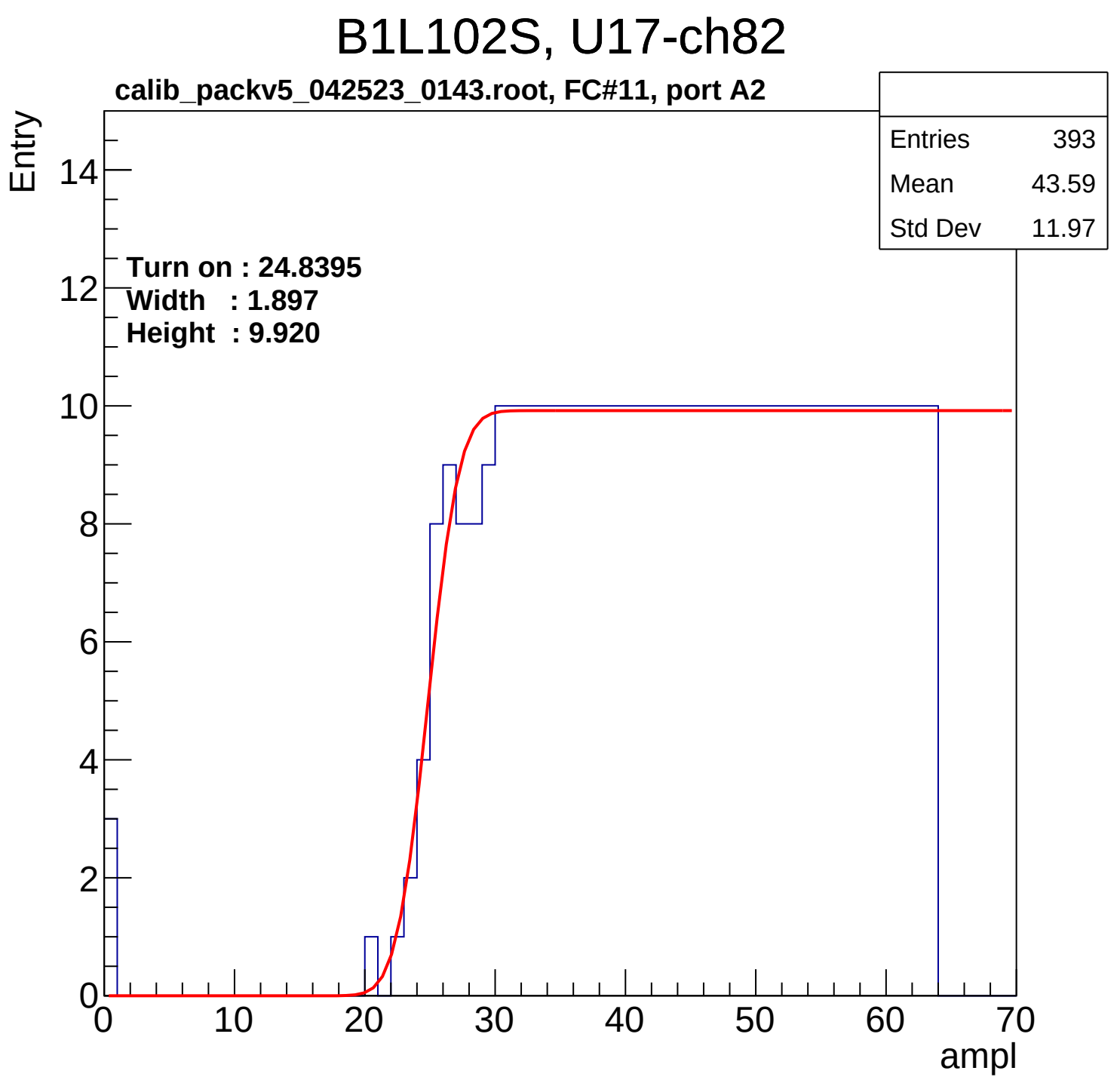
B1L102S, U17-ch82
calib_packv5_042523_0143.root, FC#11, port A2
Entries 393
Mean 43.59
Std Dev 11.97
Turn on : 24.8395
Width : 1.897
Height : 9.920
Entry
ampl
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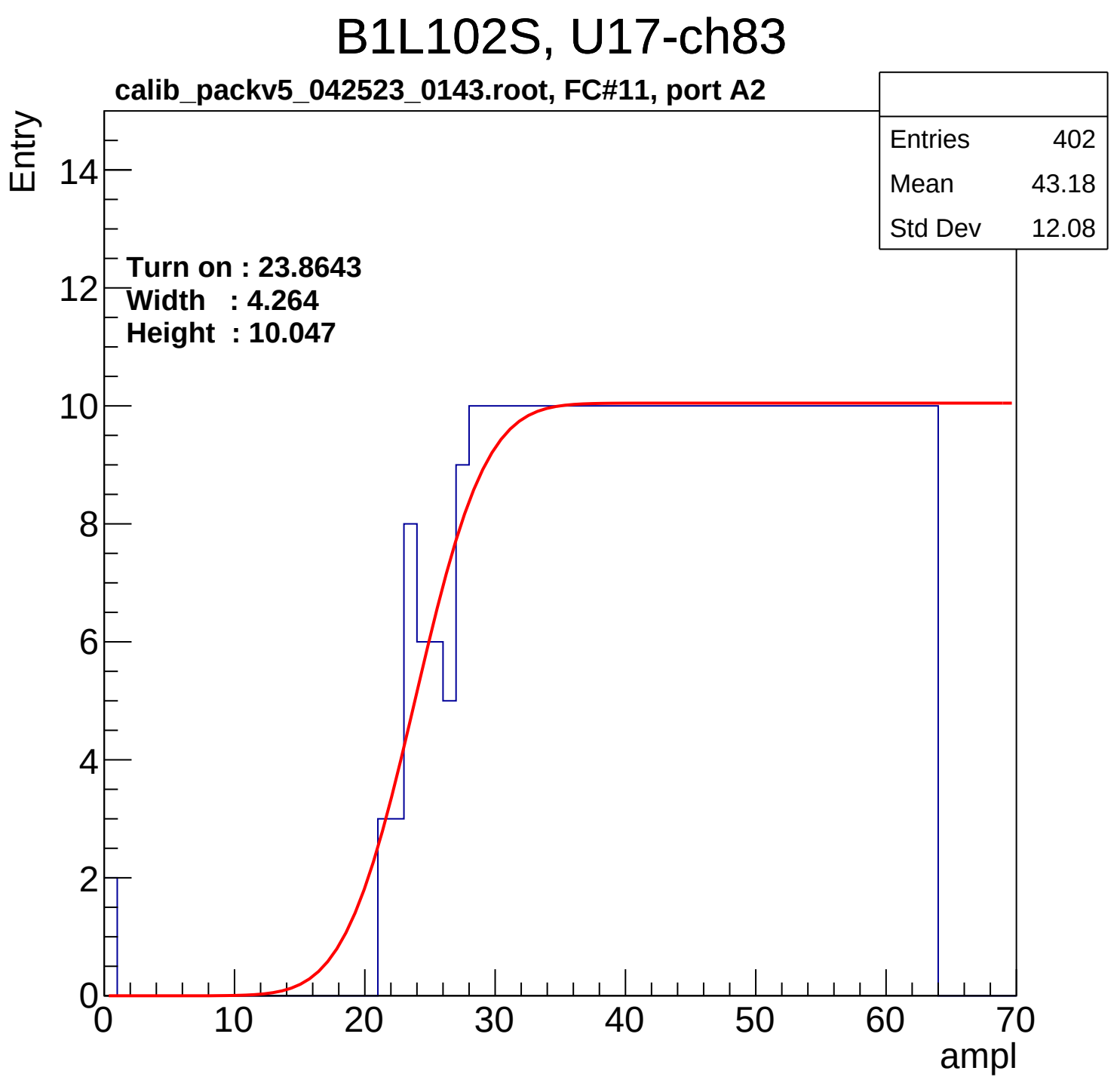
B1L102S, U17-ch83
calib_packv5_042523_0143.root, FC#11, port A2
Entries 402
Mean 43.18
Std Dev 12.08
Turn on : 23.8643
Width : 4.264
Height : 10.047
Entry
ampl
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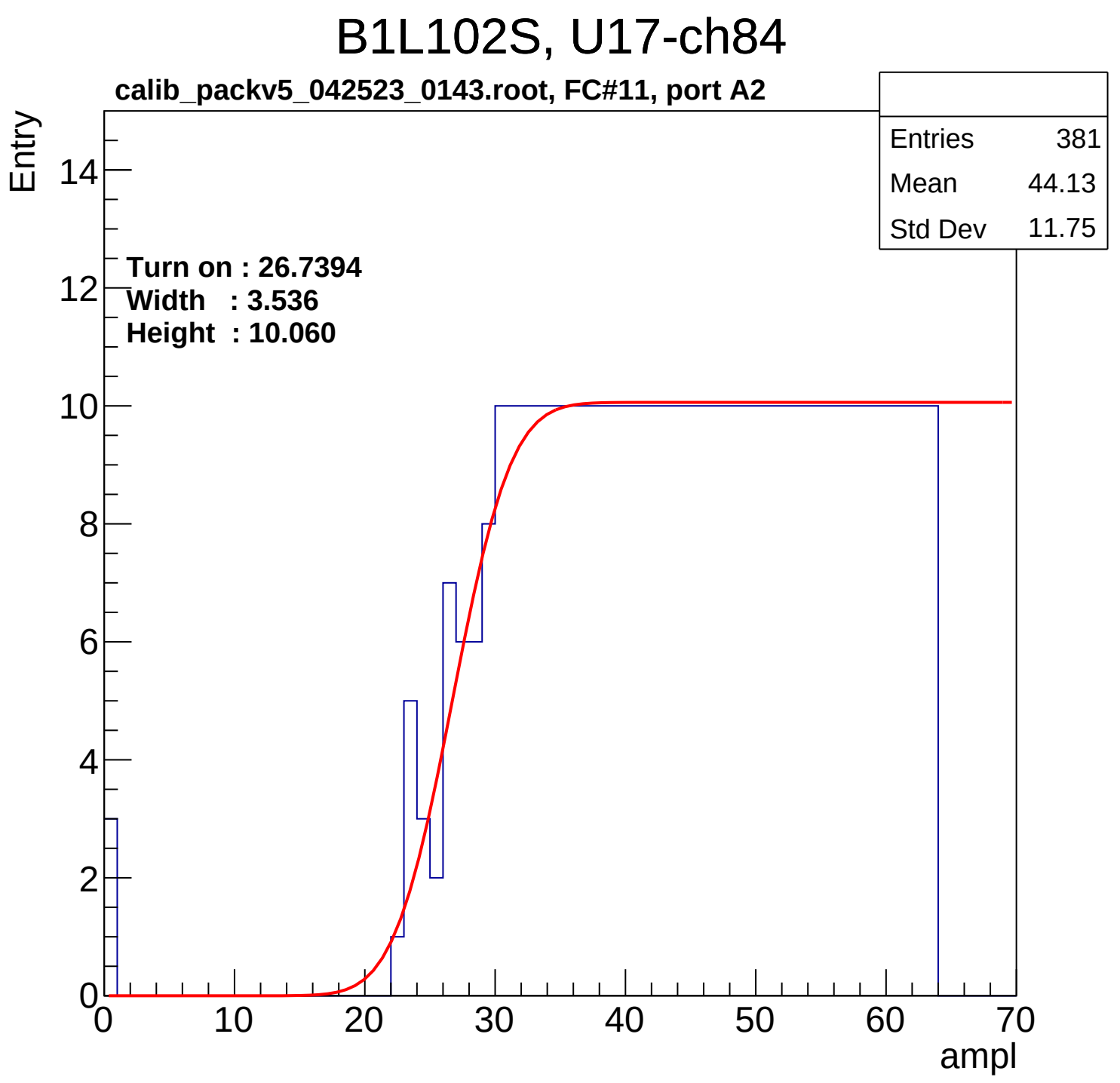
B1L102S, U17-ch84
calib_packv5_042523_0143.root, FC#11, port A2
Entries 381
Mean 44.13
Std Dev 11.75
Turn on : 26.7394
Width : 3.536
Height : 10.060
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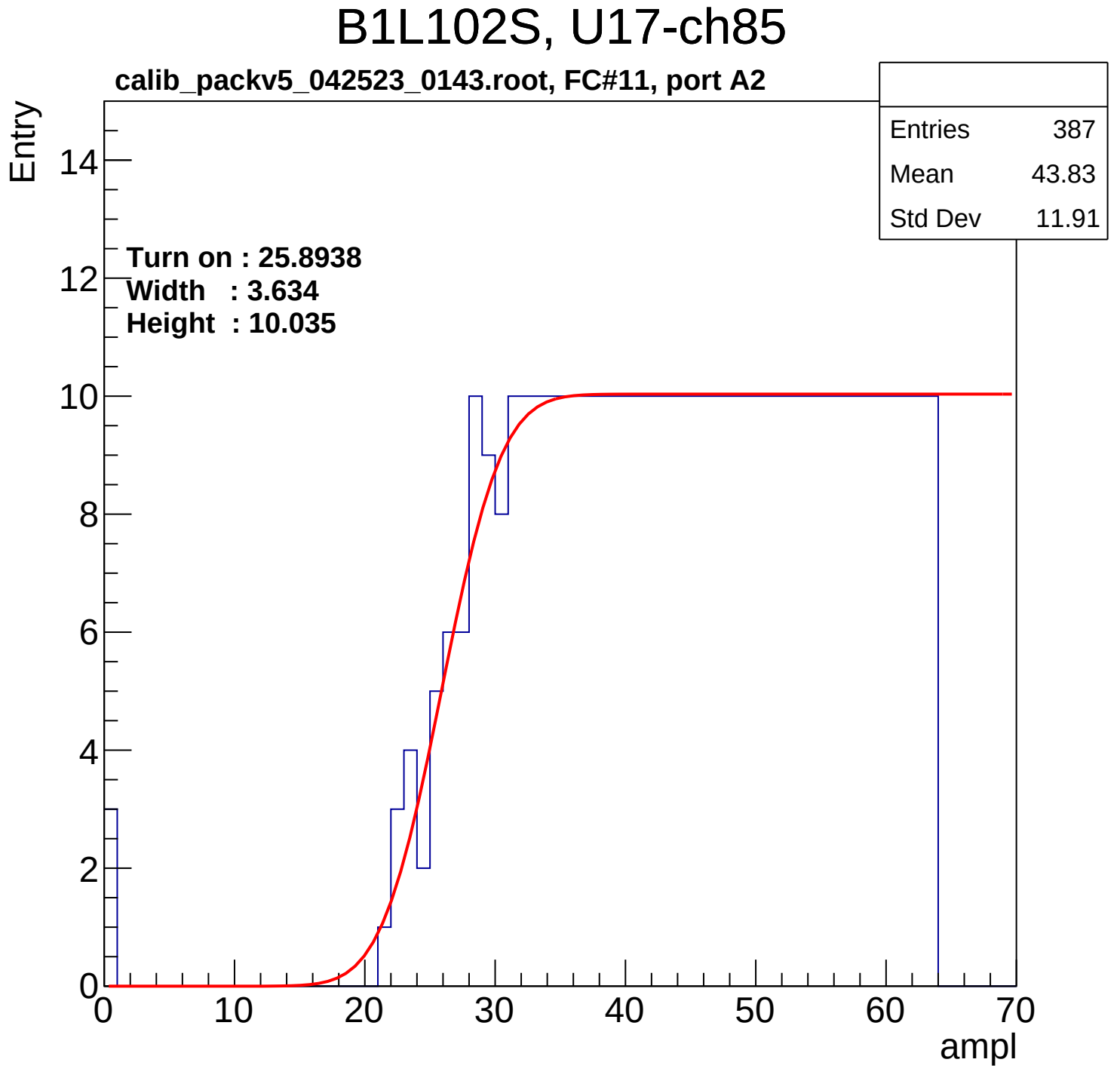
B1L102S, U17-ch85
calib_packv5_042523_0143.root, FC#11, port A2
Entries 387
Mean 43.83
Std Dev 11.91
Turn on : 25.8938
Width : 3.634
Height : 10.035
Entry
ampl
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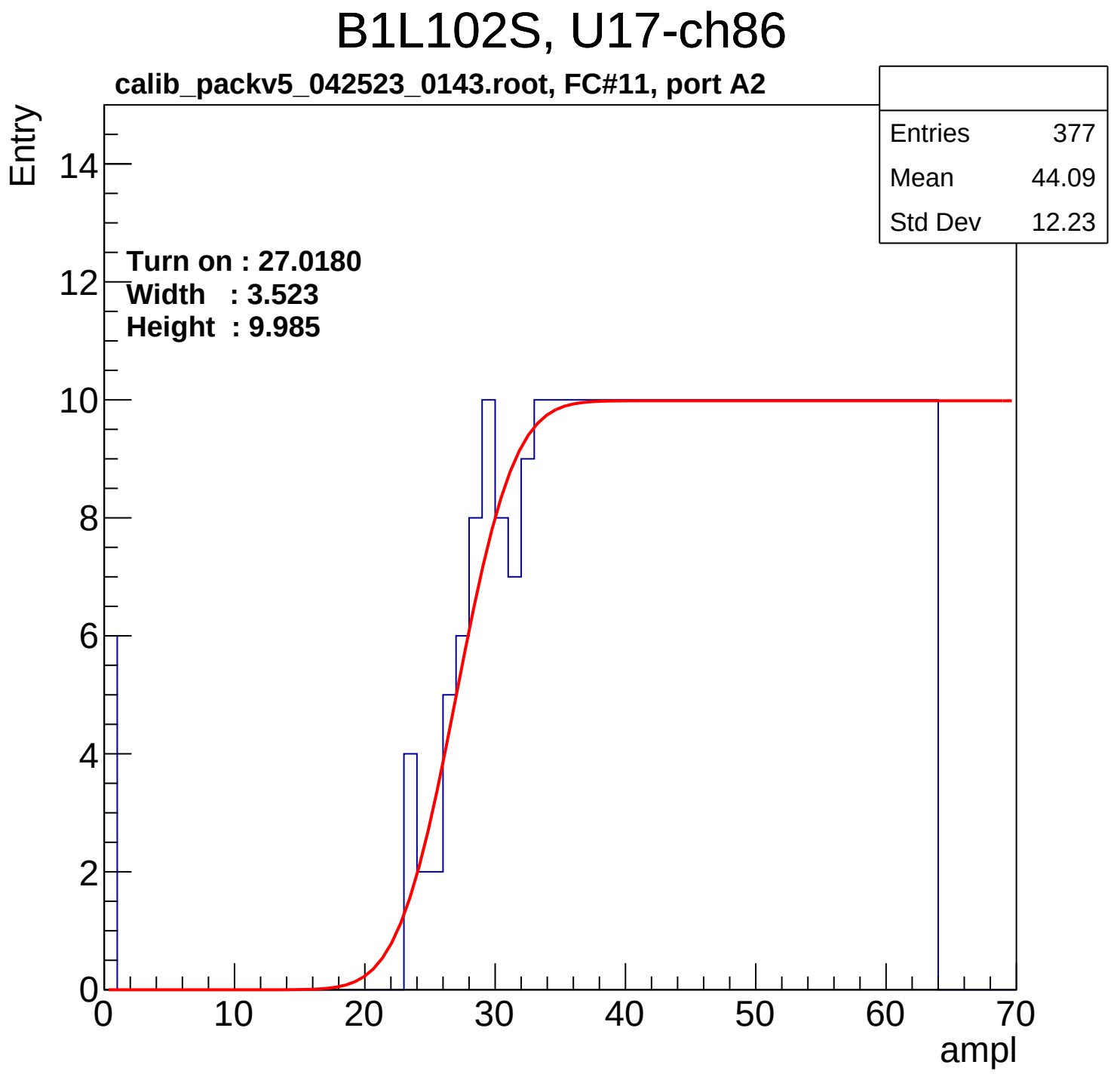
B1L102S, U17-ch86
calib_packv5_042523_0143.root, FC#11, port A2
Entries 377
Mean 44.09
Std Dev 12.23
Turn on : 27.0180
Width : 3.523
Height : 9.985
Entry
ampl
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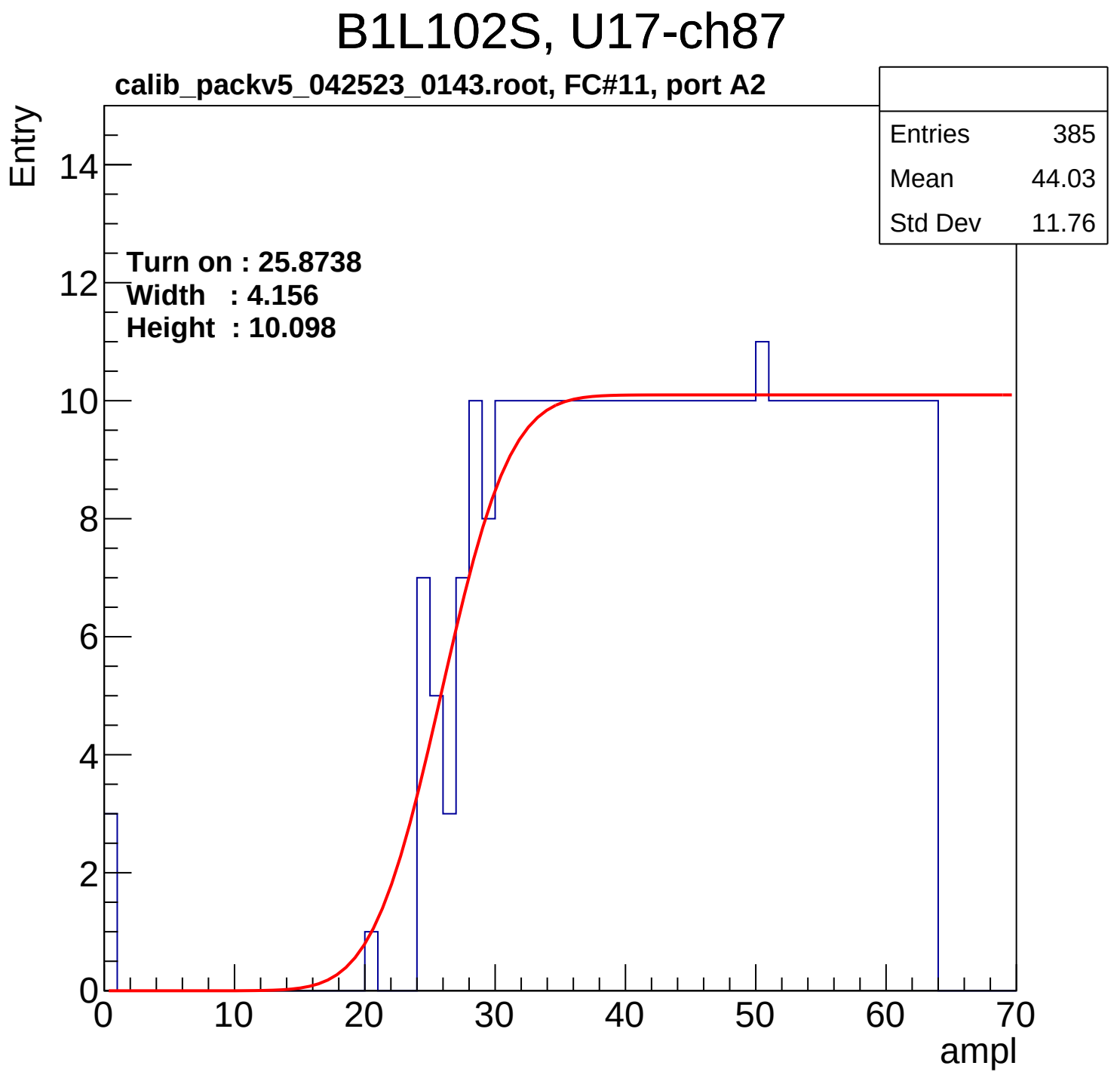
B1L102S, U17-ch87
calib_packv5_042523_0143.root, FC#11, port A2
Entries 385
Mean 44.03
Std Dev 11.76
Turn on : 25.8738
Width : 4.156
Height : 10.098
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ampl
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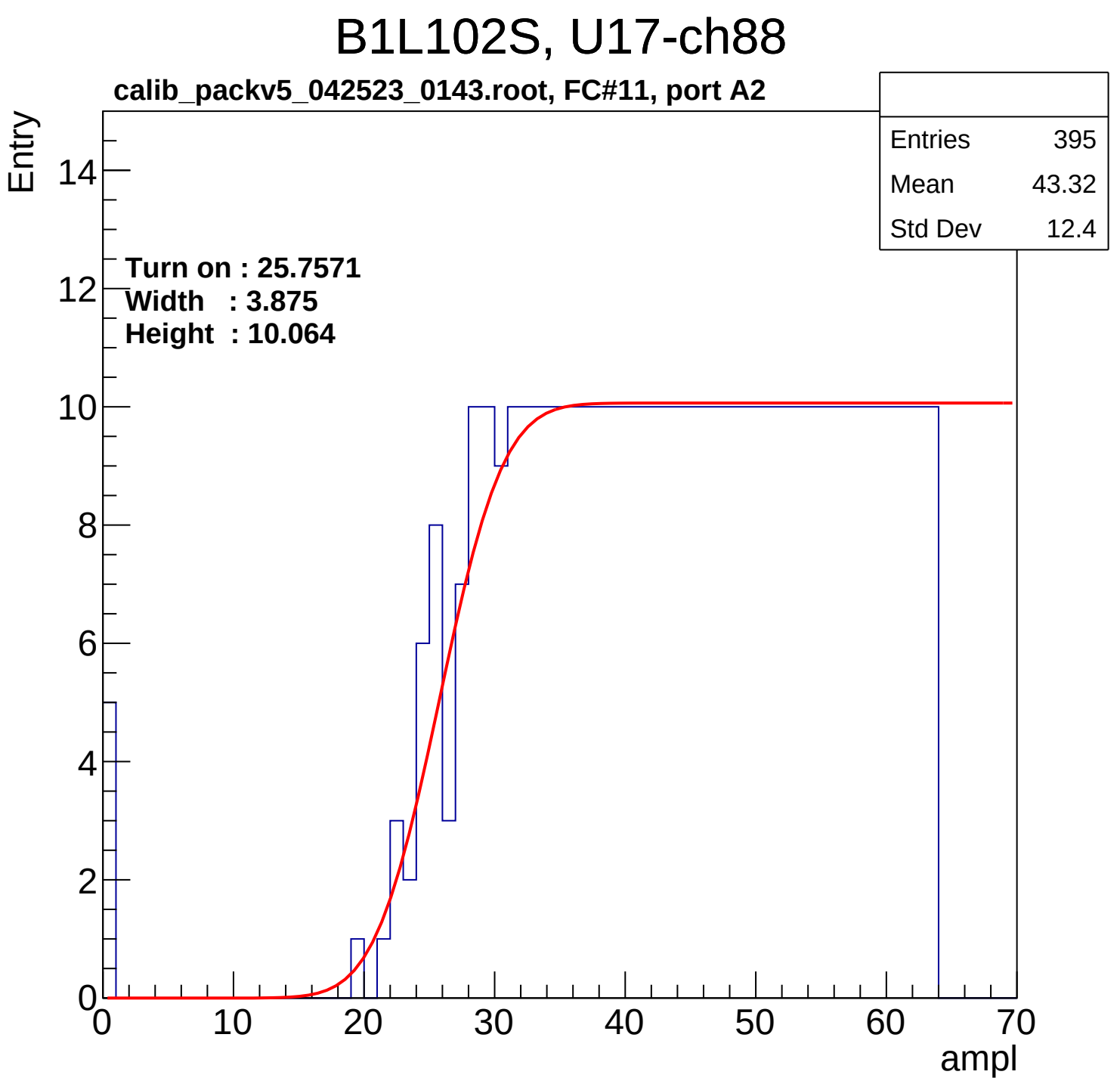
B1L102S, U17-ch88
calib_packv5_042523_0143.root, FC#11, port A2
Entries 395
Mean 43.32
Std Dev 12.4
Turn on : 25.7571
Width : 3.875
Height : 10.064
Entry
ampl
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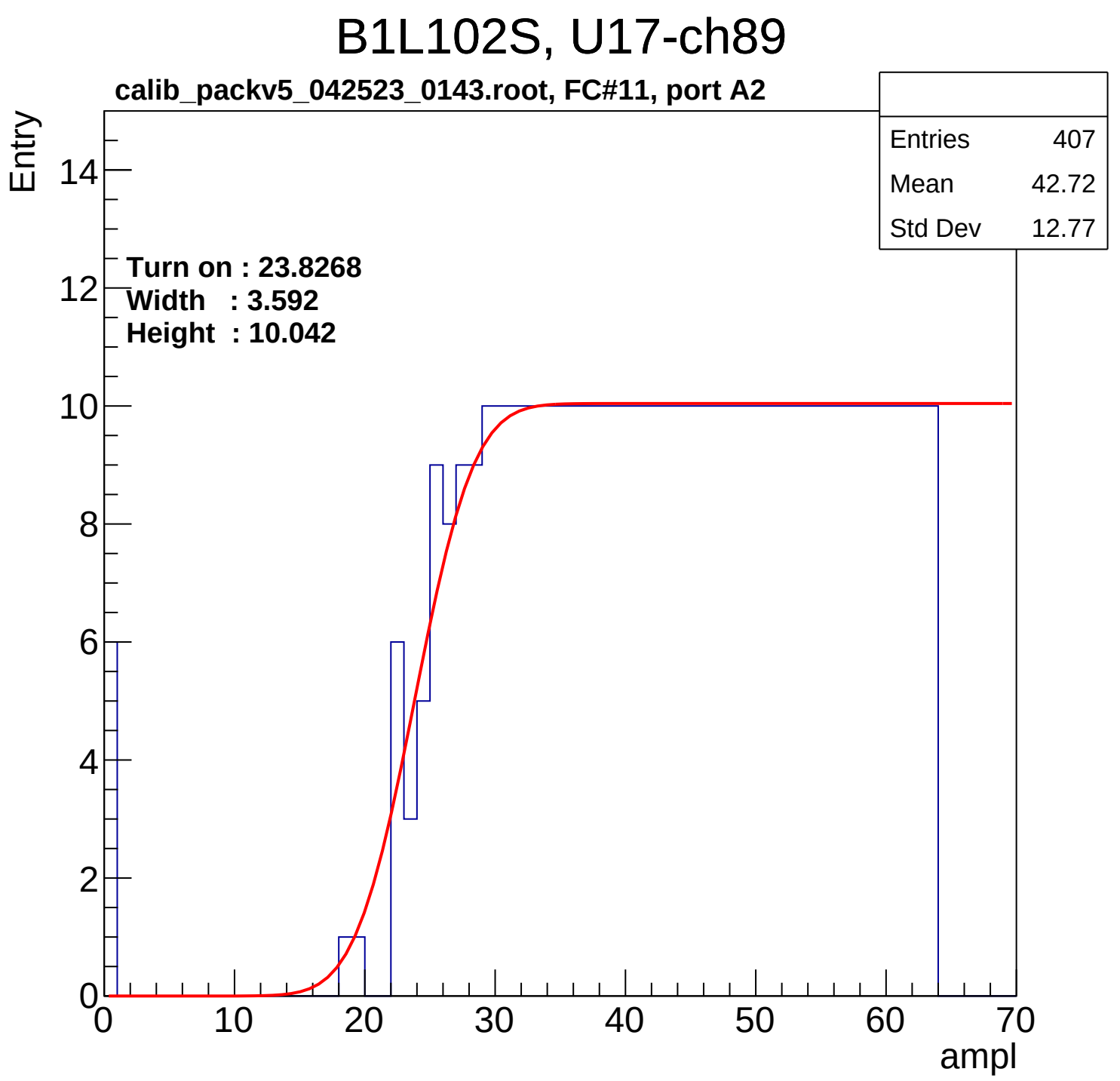
B1L102S, U17-ch89
calib_packv5_042523_0143.root, FC#11, port A2
Entries 407
Mean 42.72
Std Dev 12.77
Turn on : 23.8268
Width : 3.592
Height : 10.042
Entry
ampl
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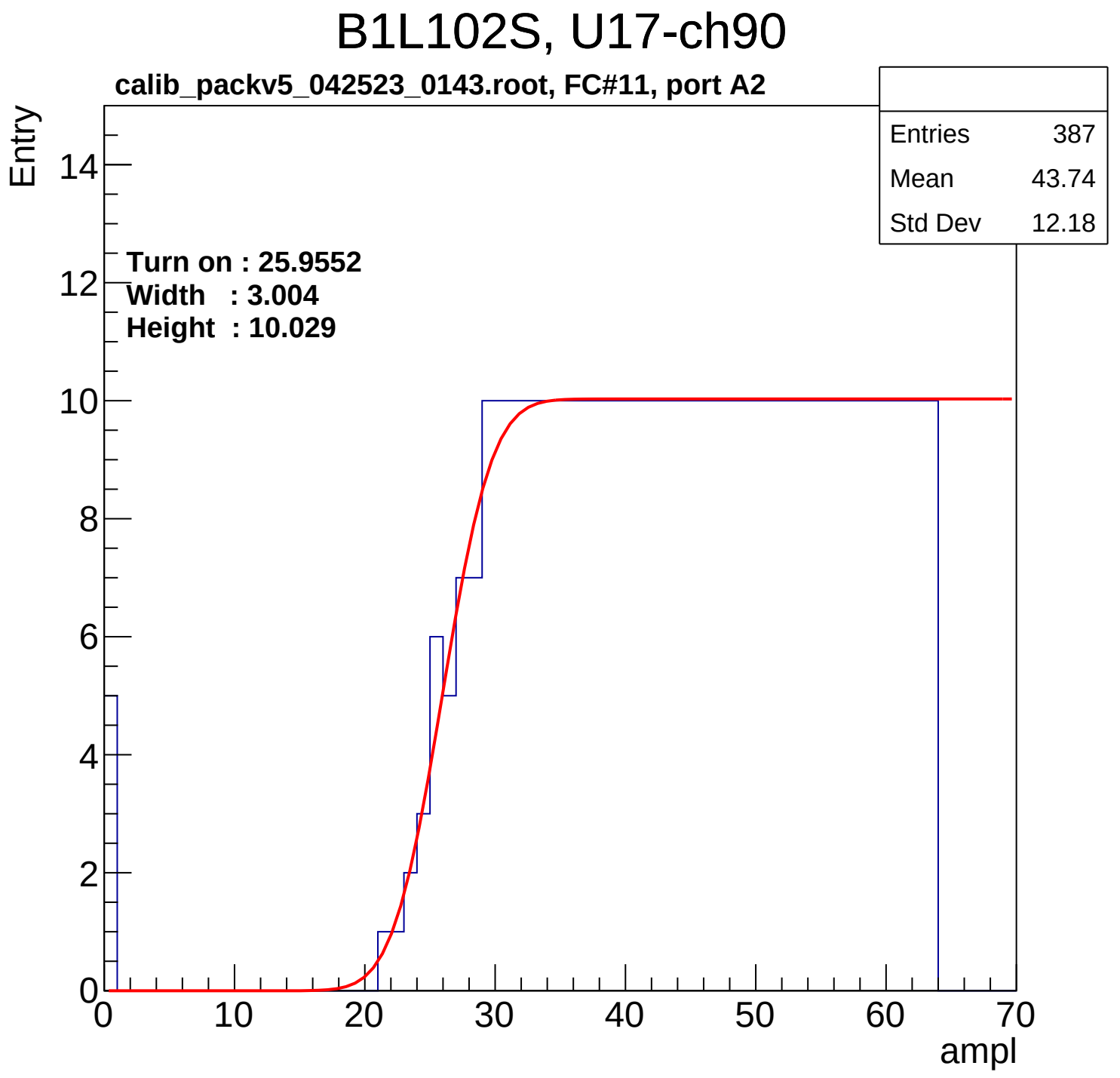
B1L102S, U17-ch90
calib_packv5_042523_0143.root, FC#11, port A2
Entries 387
Mean 43.74
Std Dev 12.18
Turn on : 25.9552
Width : 3.004
Height : 10.029
Entry
ampl
0
2
4
6
8
10
12
14
0
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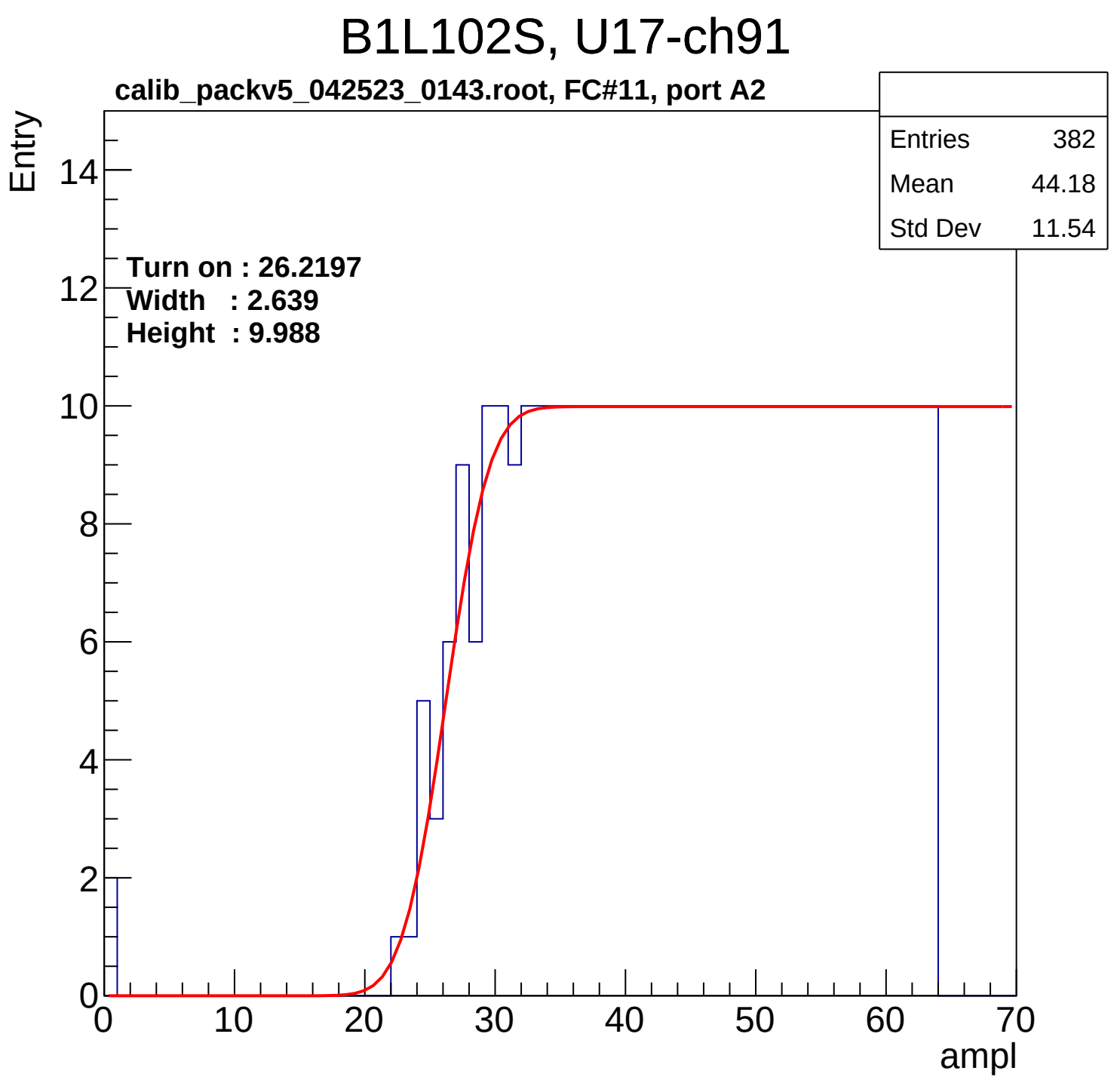
B1L102S, U17-ch91
calib_packv5_042523_0143.root, FC#11, port A2
Entries 382
Mean 44.18
Std Dev 11.54
Turn on : 26.2197
Width : 2.639
Height : 9.988
Entry
ampl
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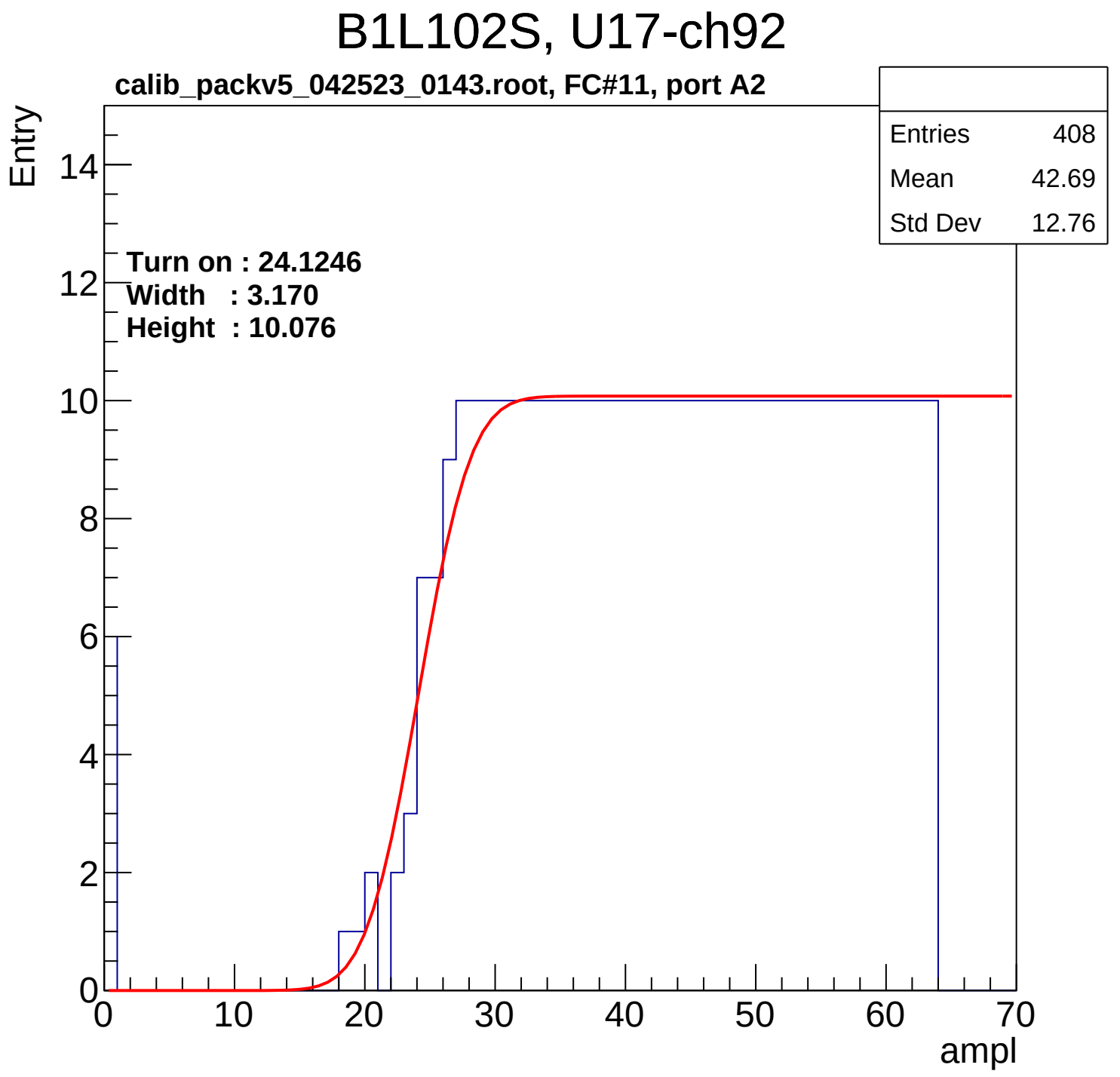
B1L102S, U17-ch92
calib_packv5_042523_0143.root, FC#11, port A2
Entries 408
Mean 42.69
Std Dev 12.76
Turn on : 24.1246
Width : 3.170
Height : 10.076
Entry
ampl
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2
4
6
8
10
12
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0
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20
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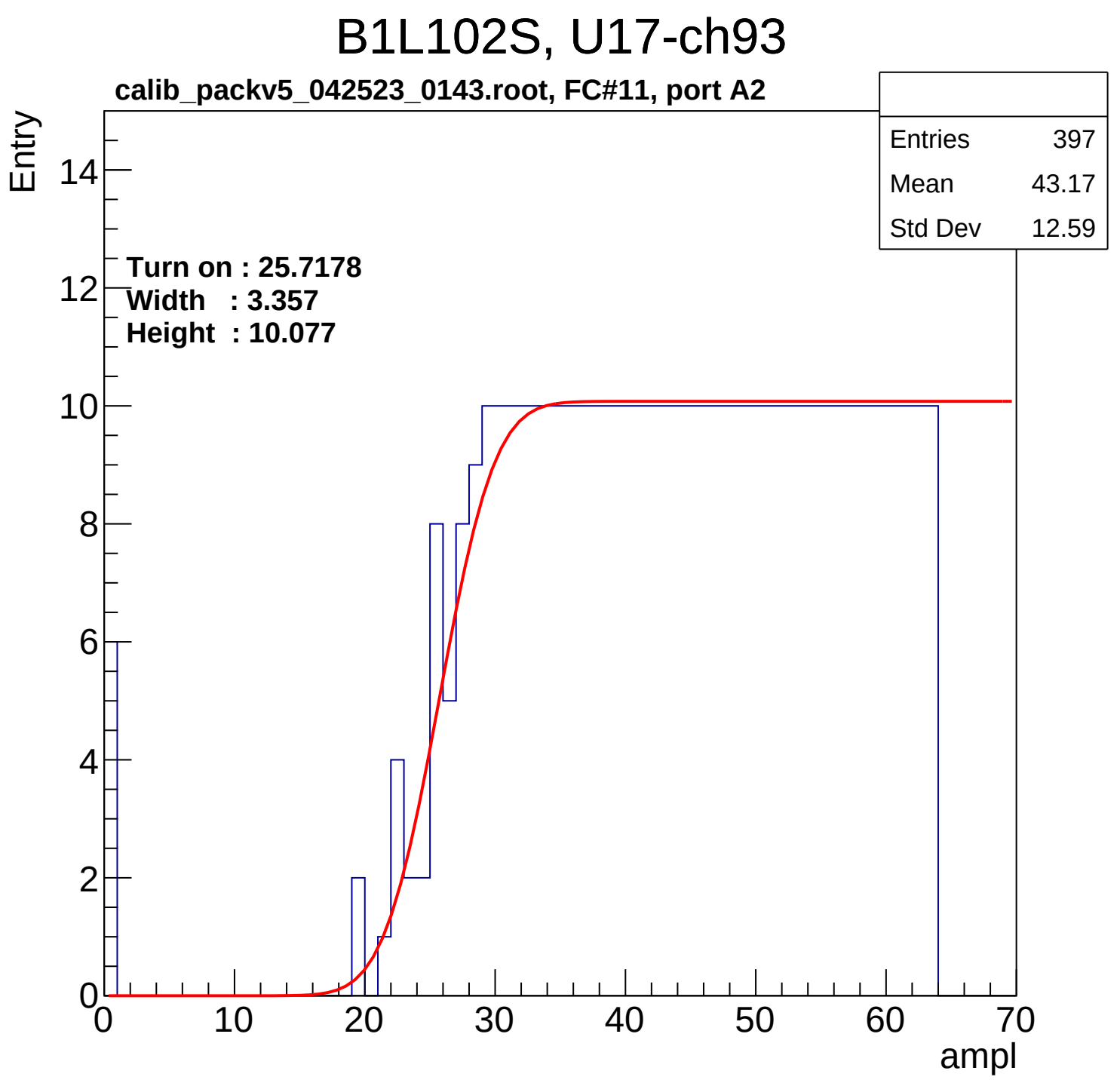
B1L102S, U17-ch93
calib_packv5_042523_0143.root, FC#11, port A2
Entries 397
Mean 43.17
Std Dev 12.59
Turn on : 25.7178
Width : 3.357
Height : 10.077
Entry
ampl
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6
8
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12
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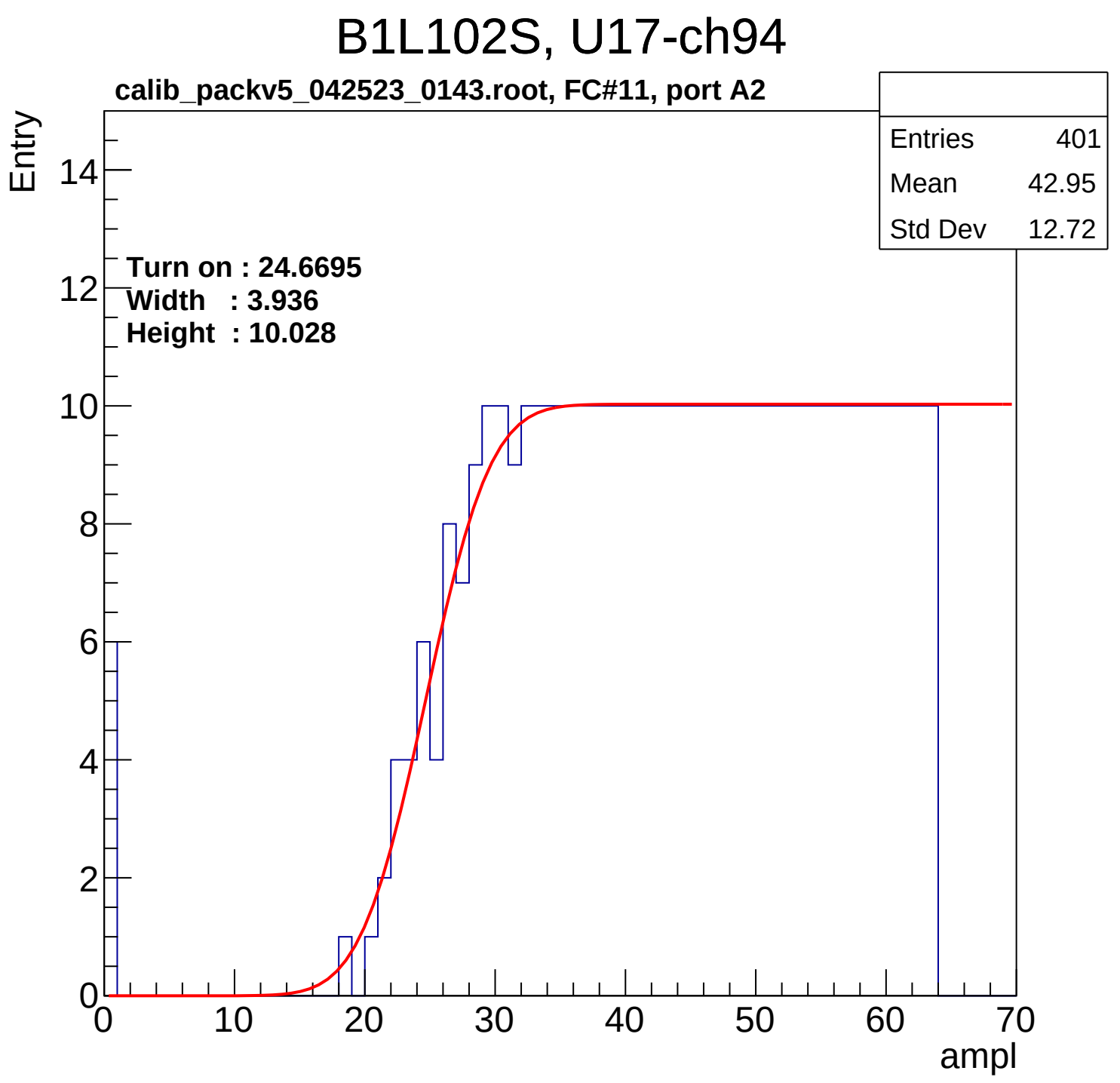
B1L102S, U17-ch94
calib_packv5_042523_0143.root, FC#11, port A2
Entries 401
Mean 42.95
Std Dev 12.72
Turn on : 24.6695
Width : 3.936
Height : 10.028
Entry
ampl
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6
8
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60
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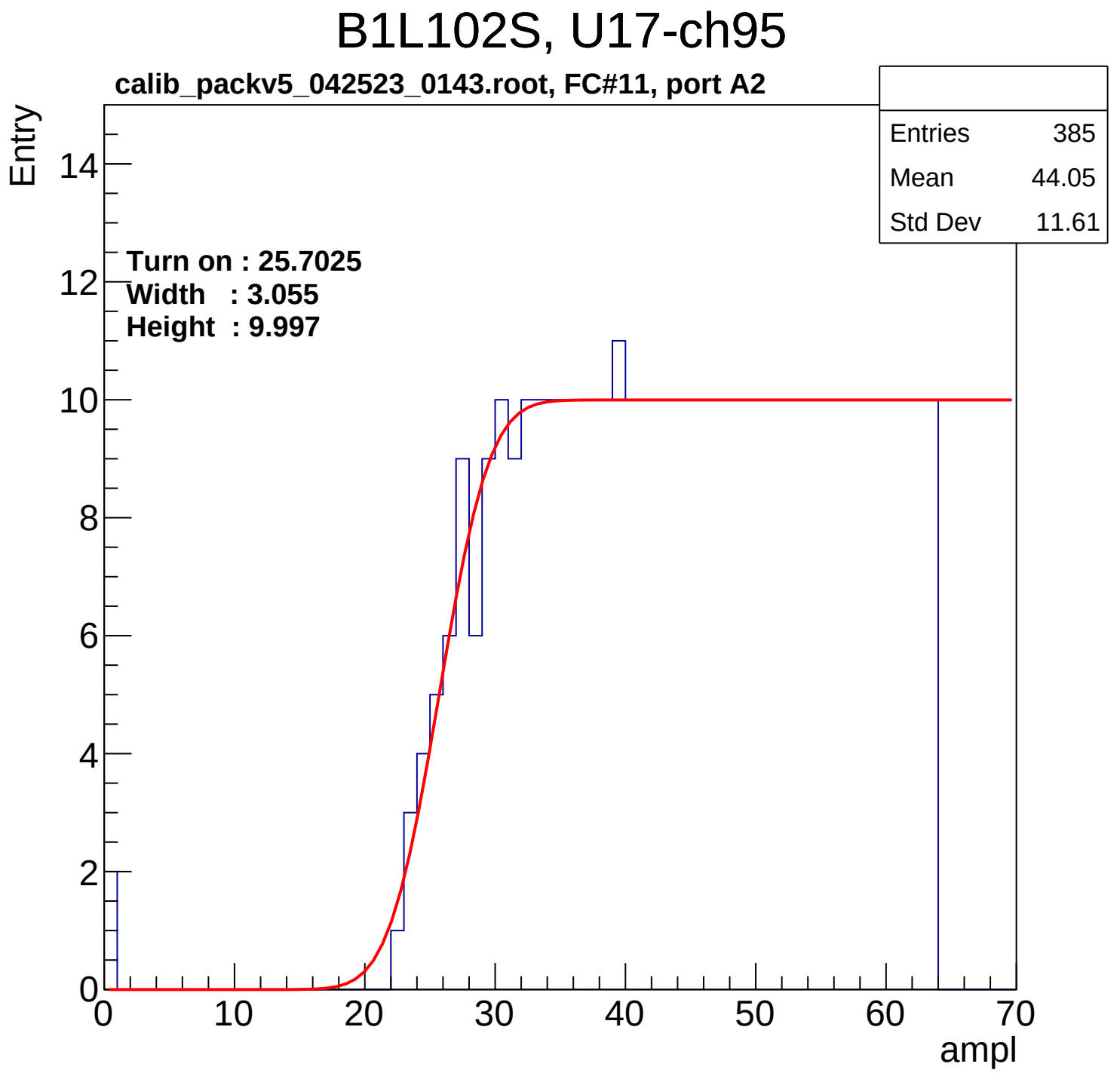
B1L102S, U17-ch95
calib_packv5_042523_0143.root, FC#11, port A2
Entries 385
Mean 44.05
Std Dev 11.61
Turn on : 25.7025
Width : 3.055
Height : 9.997
Entry
ampl
0
2
4
6
8
10
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0
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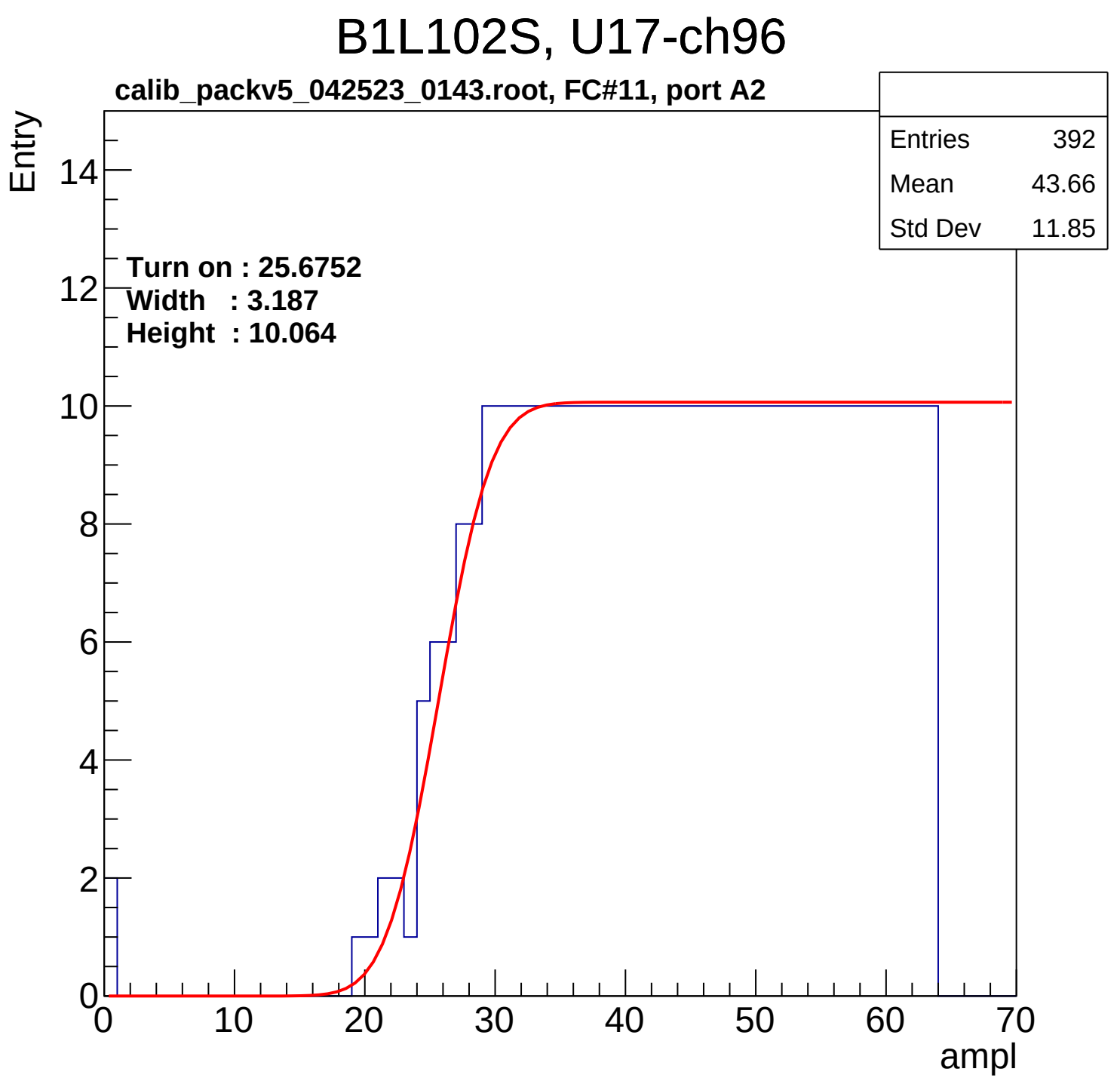
B1L102S, U17-ch96
calib_packv5_042523_0143.root, FC#11, port A2
Entries 392
Mean 43.66
Std Dev 11.85
Turn on : 25.6752
Width : 3.187
Height : 10.064
Entry
ampl
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6
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10
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0
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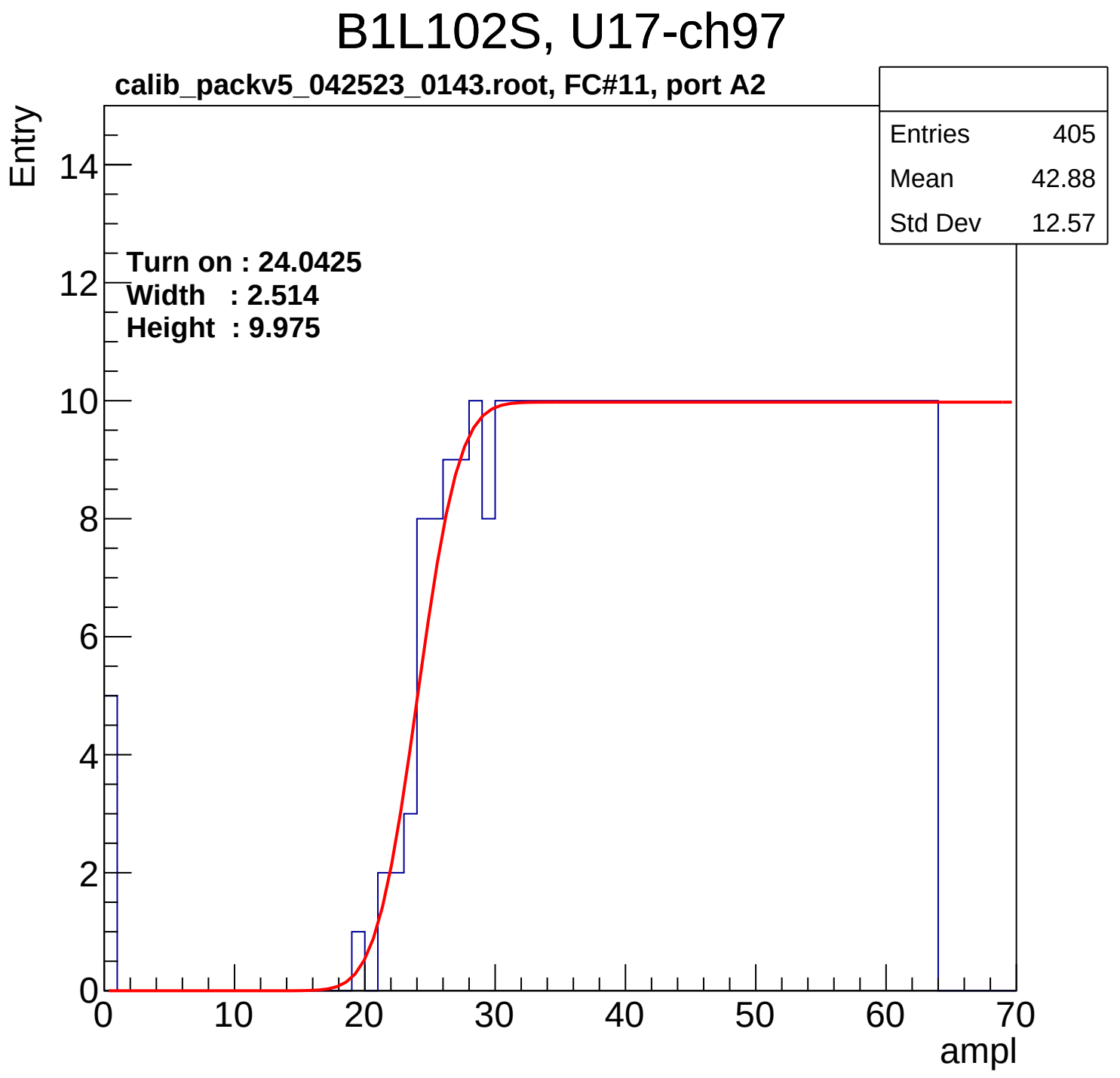
B1L102S, U17-ch97
calib_packv5_042523_0143.root, FC#11, port A2
Entries 405
Mean 42.88
Std Dev 12.57
Turn on : 24.0425
Width : 2.514
Height : 9.975
Entry
ampl
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6
8
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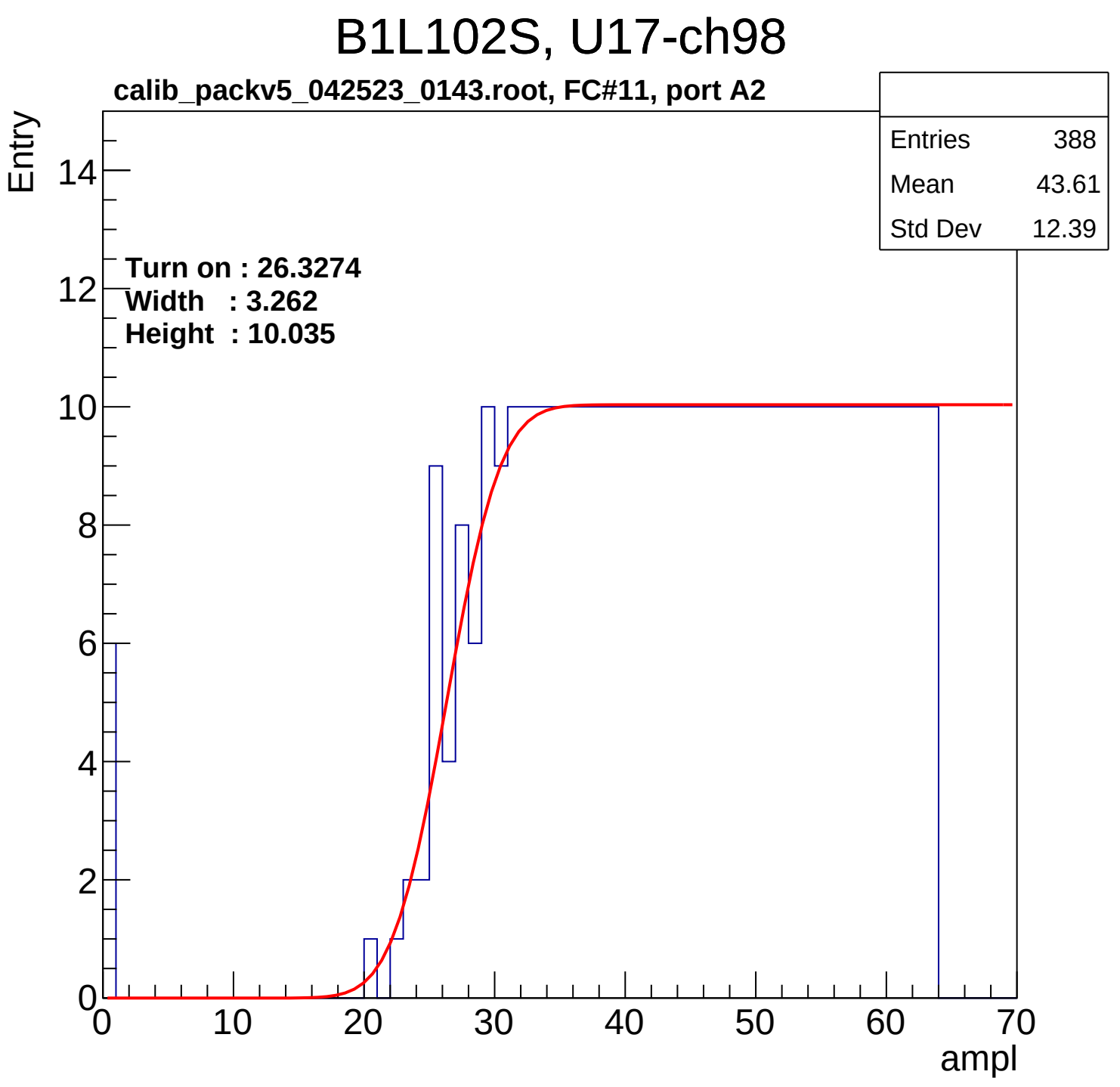
B1L102S, U17-ch98
calib_packv5_042523_0143.root, FC#11, port A2
Entries 388
Mean 43.61
Std Dev 12.39
Turn on : 26.3274
Width : 3.262
Height : 10.035
Entry
ampl
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6
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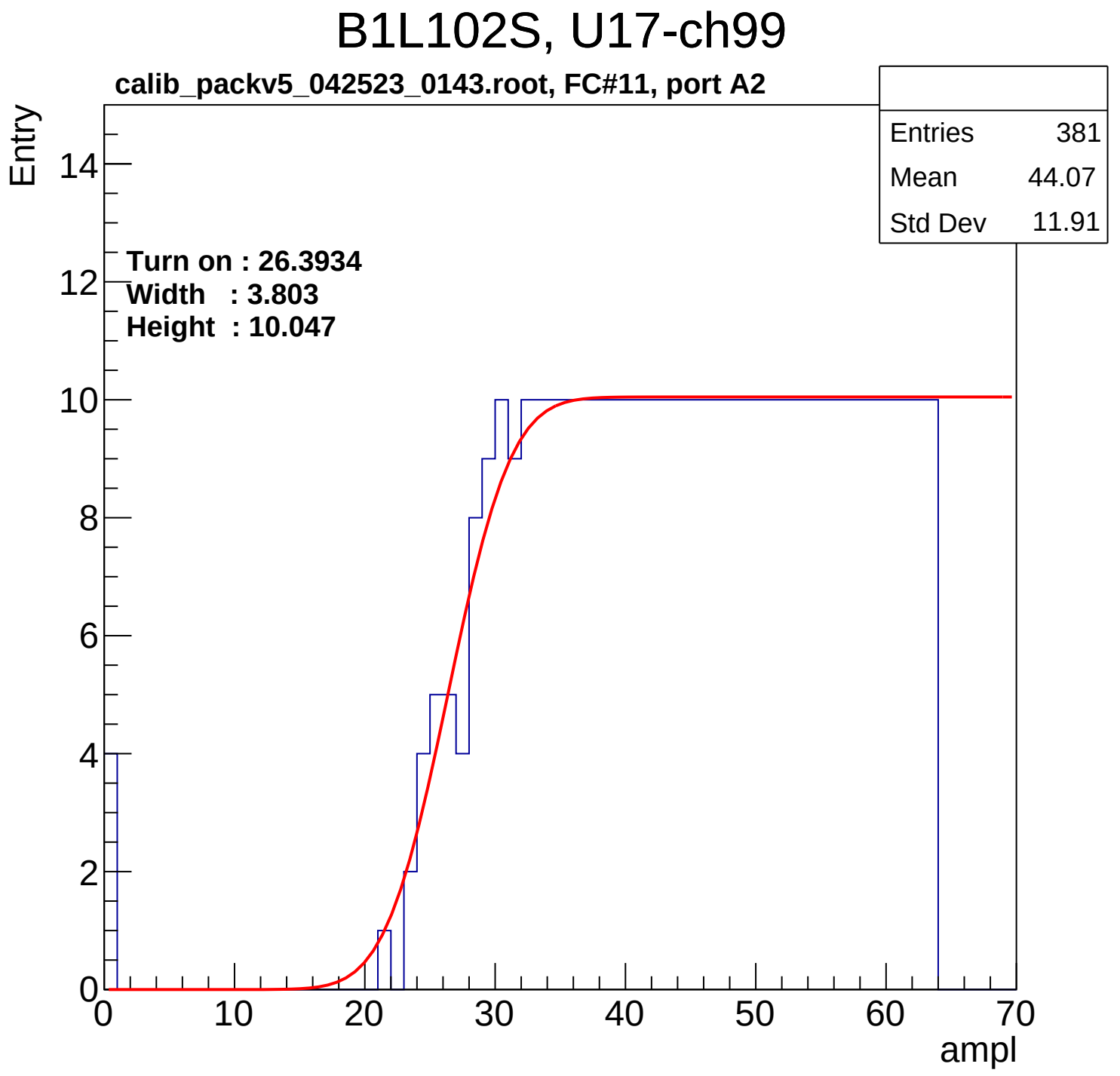
B1L102S, U17-ch99
calib_packv5_042523_0143.root, FC#11, port A2
Entries 381
Mean 44.07
Std Dev 11.91
Turn on : 26.3934
Width : 3.803
Height : 10.047
Entry
ampl
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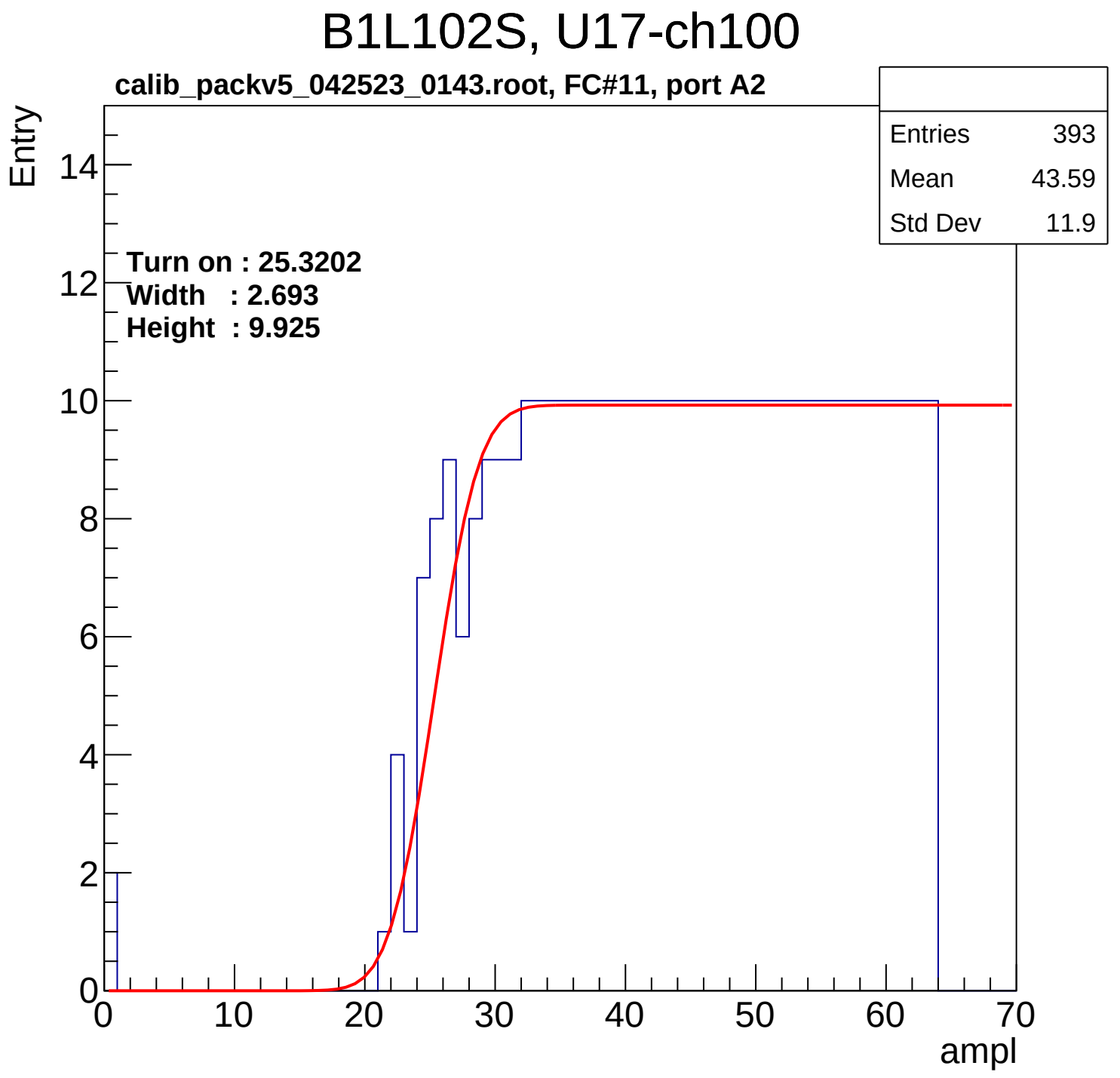
B1L102S, U17-ch100
calib_packv5_042523_0143.root, FC#11, port A2
Entries 393
Mean 43.59
Std Dev 11.9
Turn on : 25.3202
Width : 2.693
Height : 9.925
Entry
ampl
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6
8
10
12
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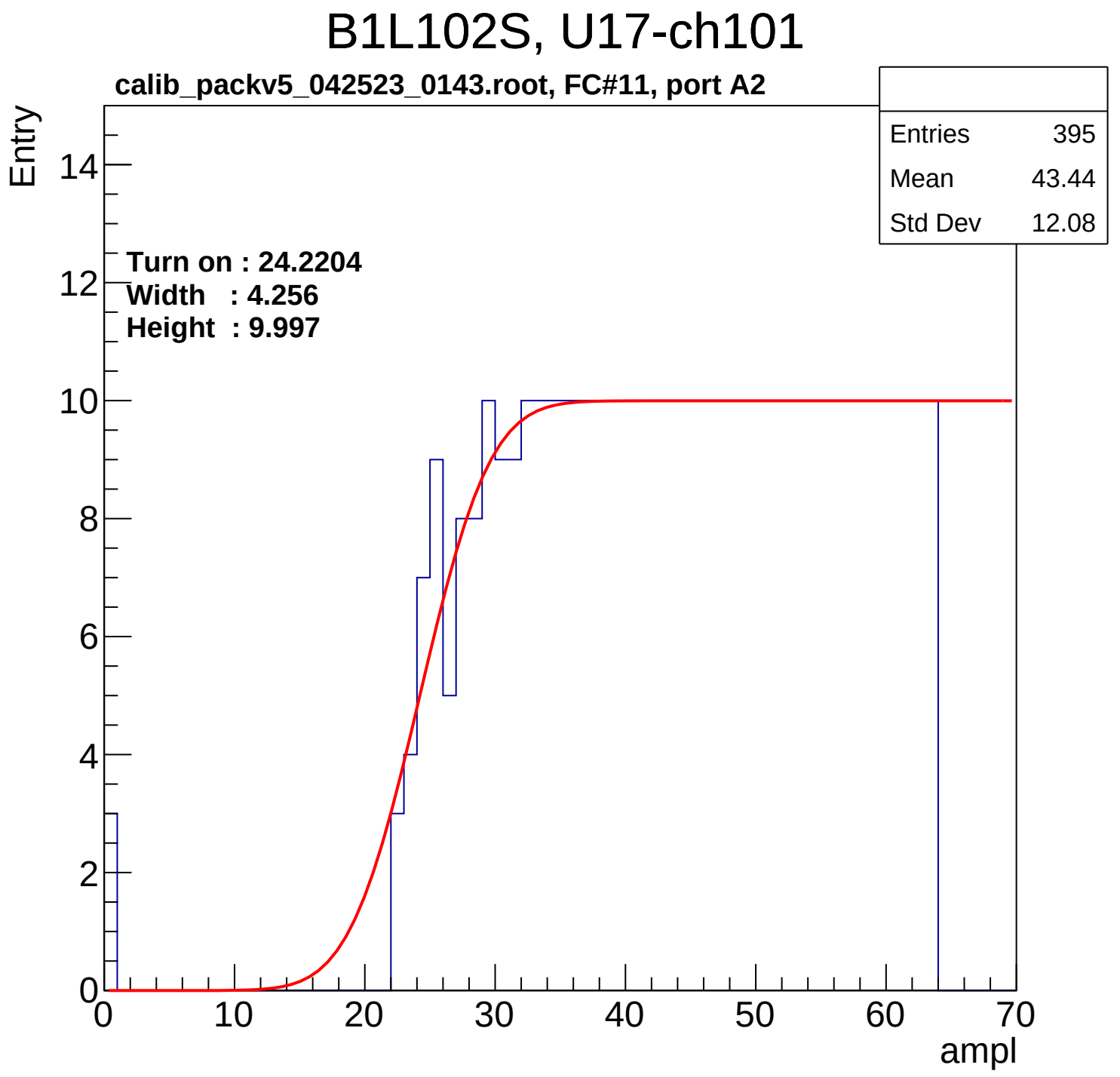
B1L102S, U17-ch101
calib_packv5_042523_0143.root, FC#11, port A2
Entries 395
Mean 43.44
Std Dev 12.08
Turn on : 24.2204
Width : 4.256
Height : 9.997
Entry
ampl
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4
6
8
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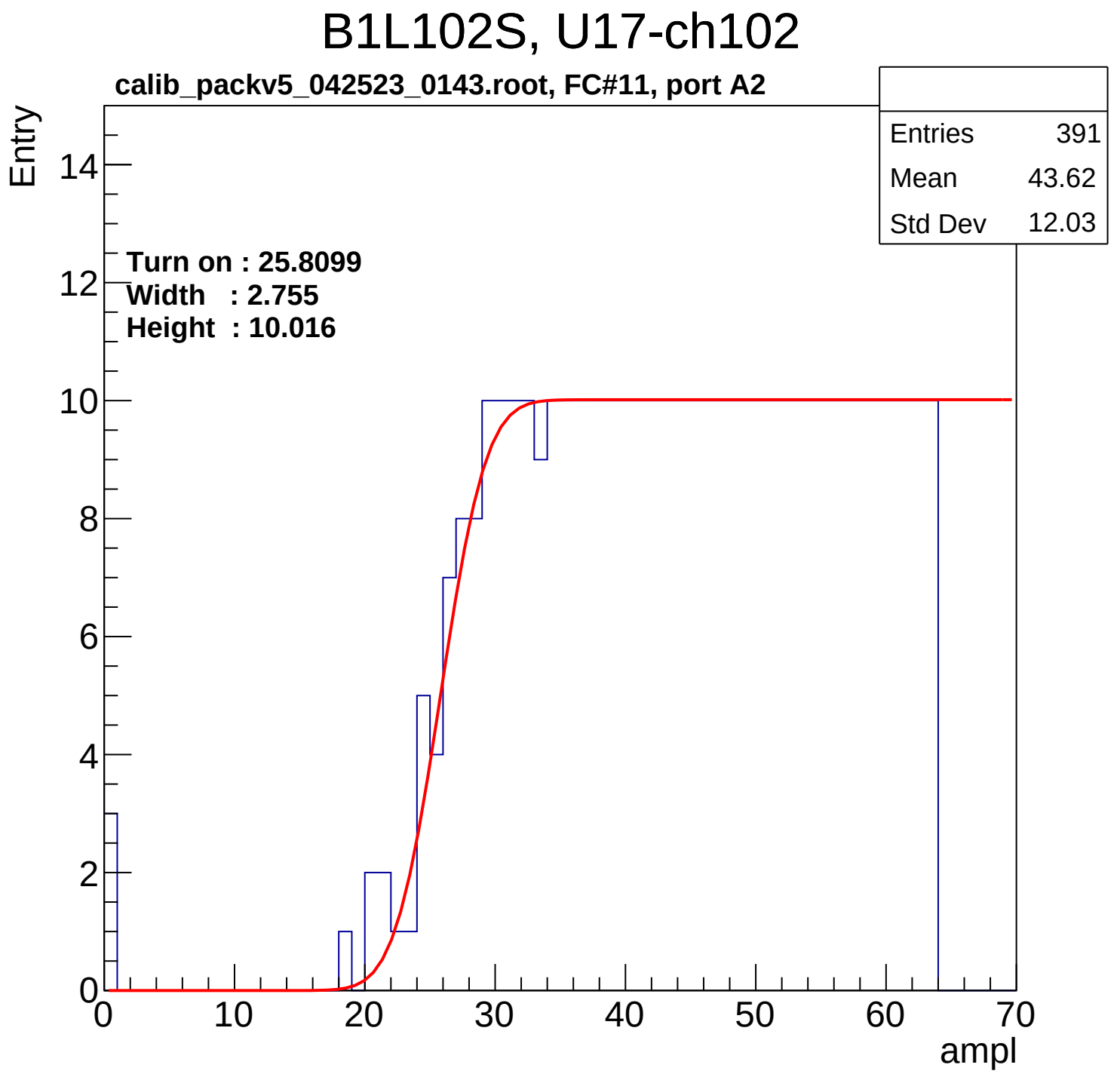
B1L102S, U17-ch102
calib_packv5_042523_0143.root, FC#11, port A2
Entries 391
Mean 43.62
Std Dev 12.03
Turn on : 25.8099
Width : 2.755
Height : 10.016
Entry
ampl
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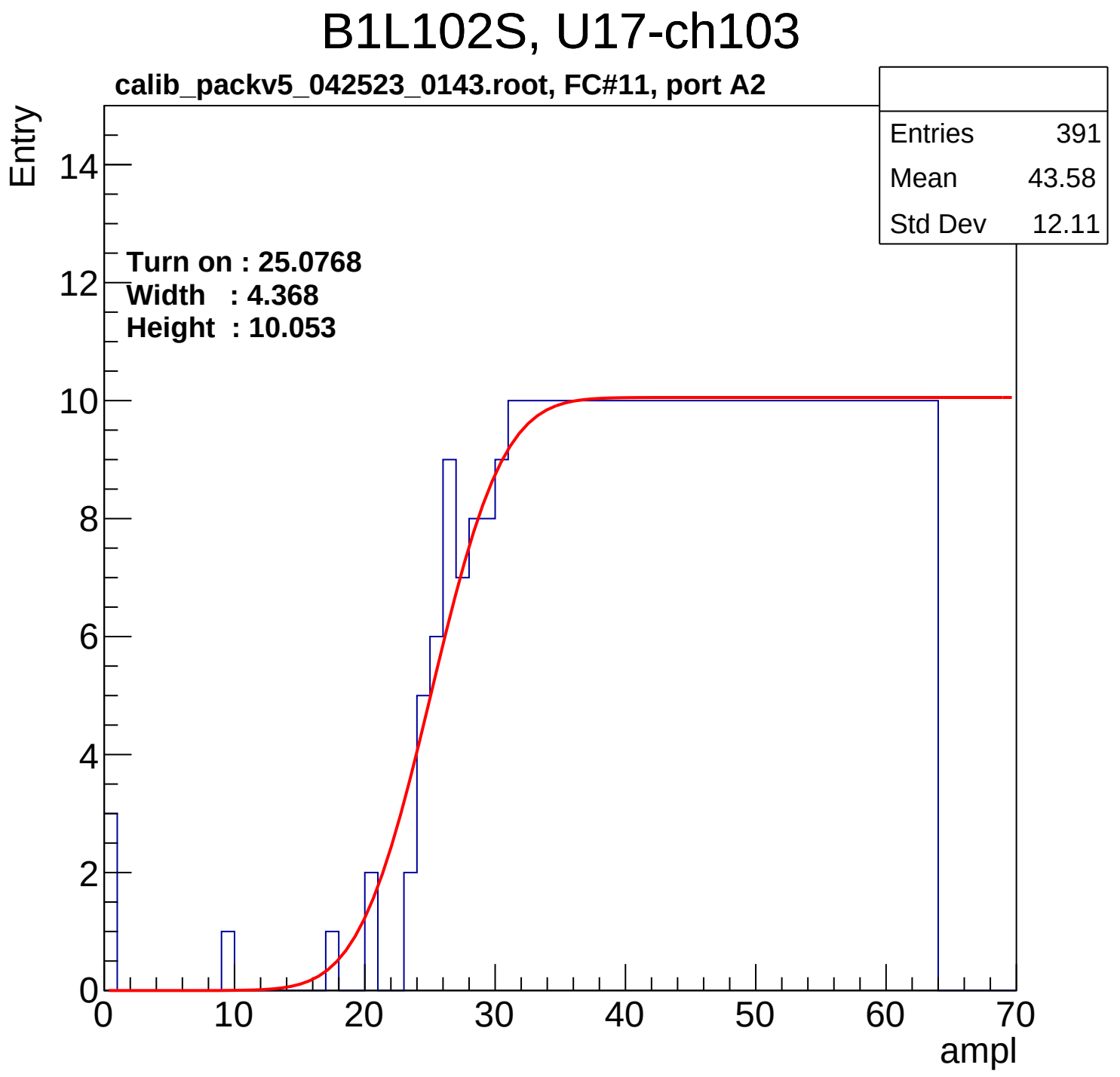
B1L102S, U17-ch103
calib_packv5_042523_0143.root, FC#11, port A2
Entries 391
Mean 43.58
Std Dev 12.11
Turn on : 25.0768
Width : 4.368
Height : 10.053
Entry
ampl
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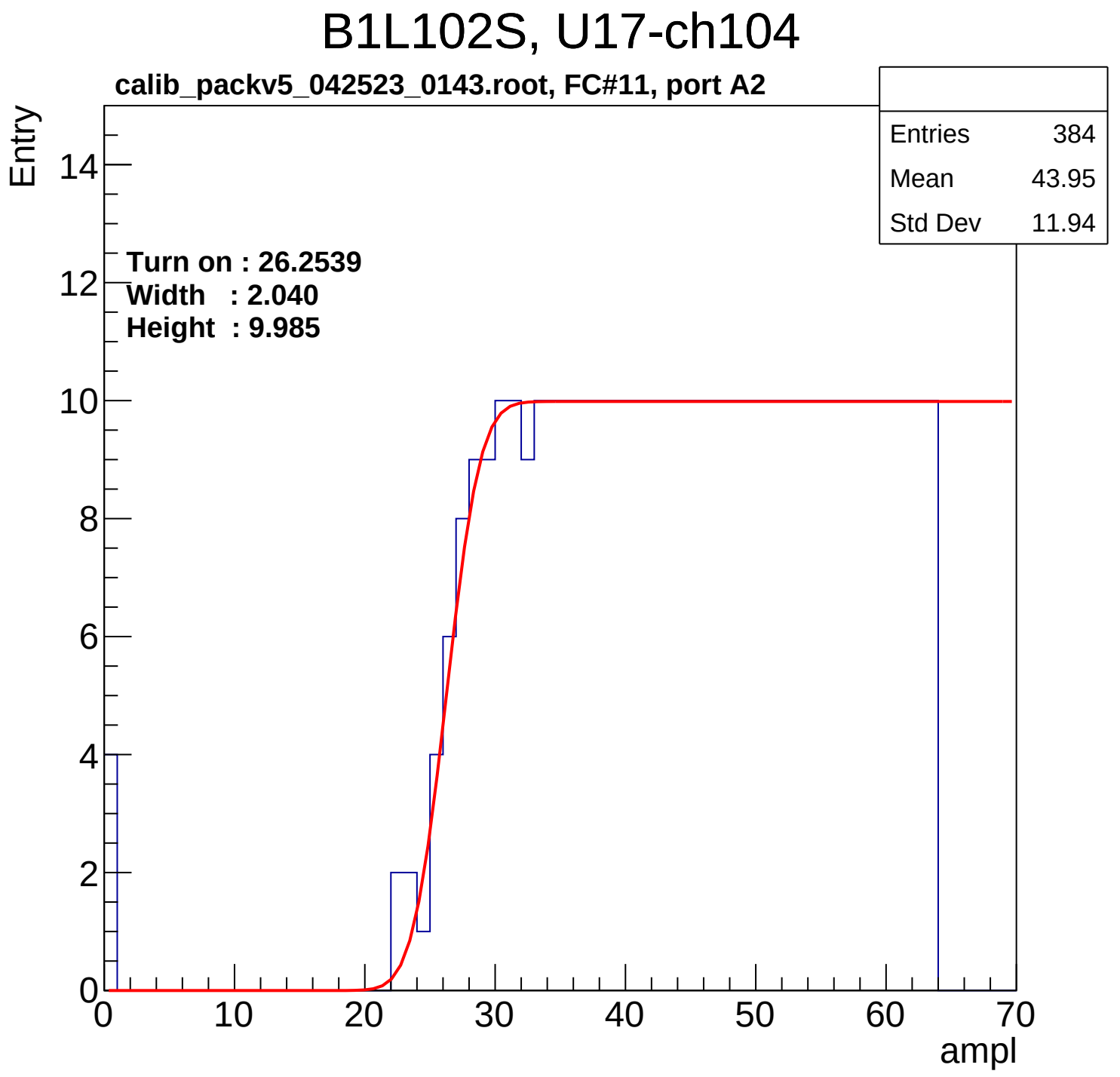
B1L102S, U17-ch104
calib_packv5_042523_0143.root, FC#11, port A2
Entries 384
Mean 43.95
Std Dev 11.94
Turn on : 26.2539
Width : 2.040
Height : 9.985
Entry
ampl
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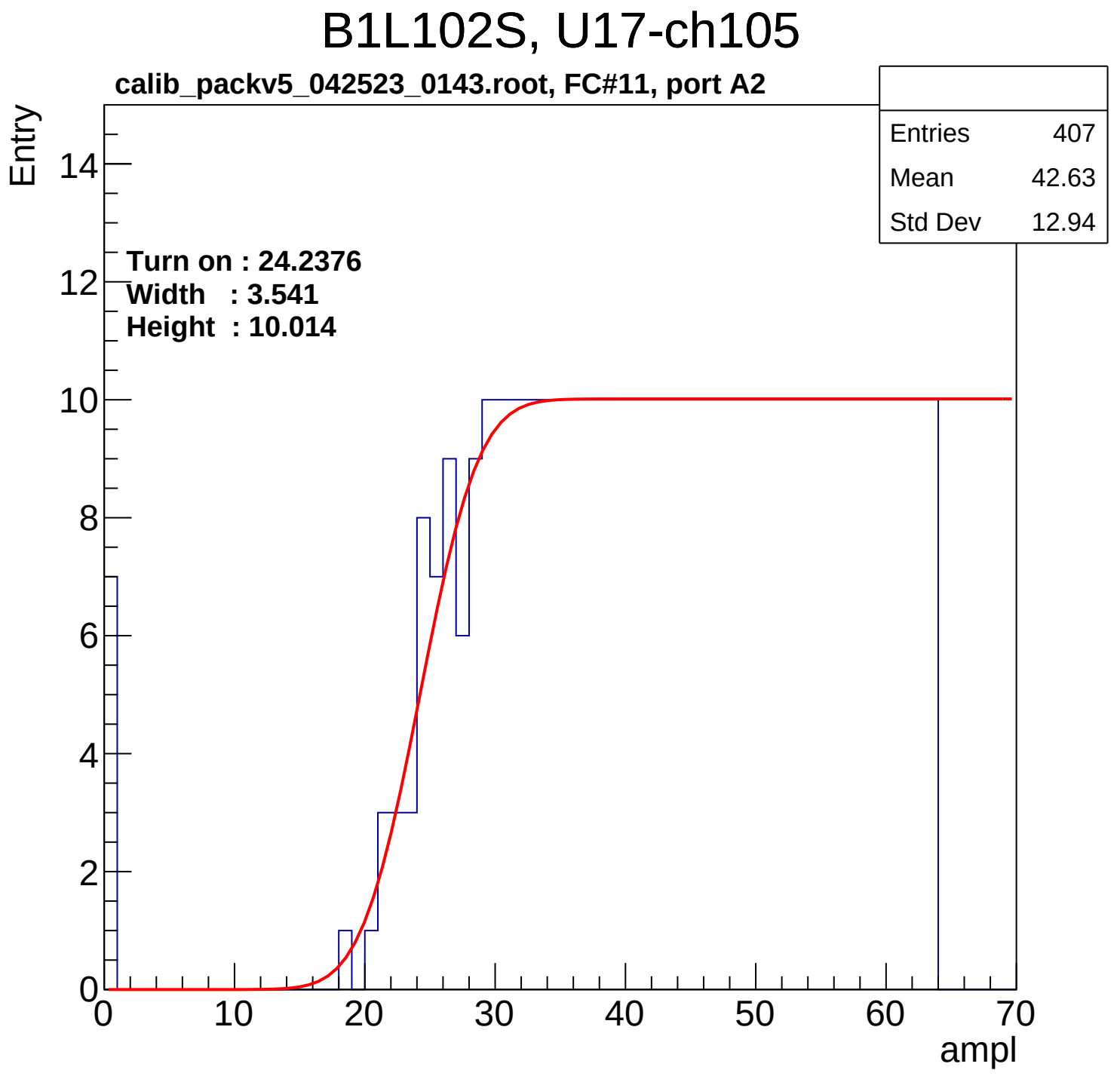
B1L102S, U17-ch105
calib_packv5_042523_0143.root, FC#11, port A2
Entries 407
Mean 42.63
Std Dev 12.94
Turn on : 24.2376
Width : 3.541
Height : 10.014
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ampl
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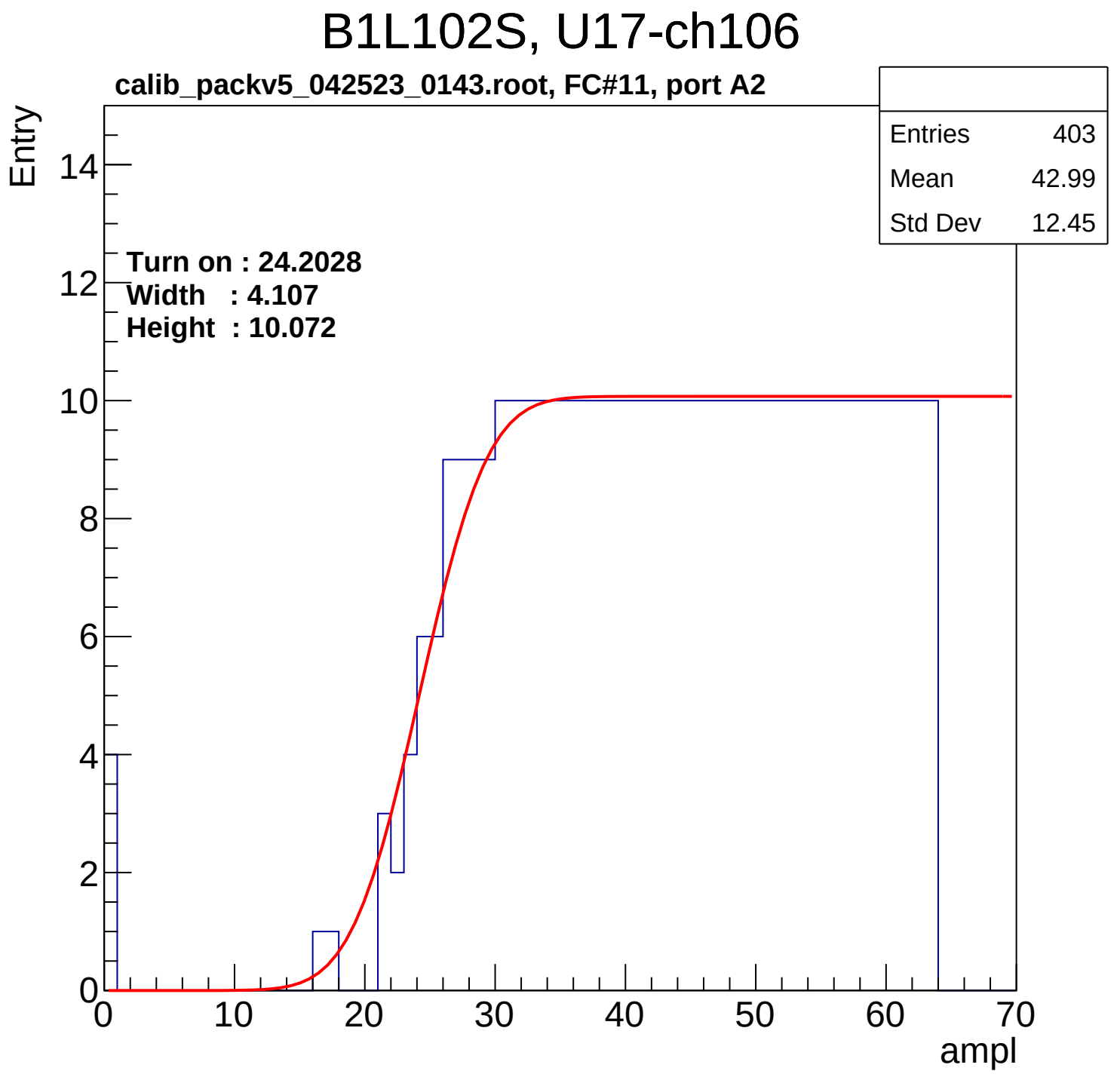
B1L102S, U17-ch106
calib_packv5_042523_0143.root, FC#11, port A2
Entries 403
Mean 42.99
Std Dev 12.45
Turn on : 24.2028
Width : 4.107
Height : 10.072
Entry
ampl
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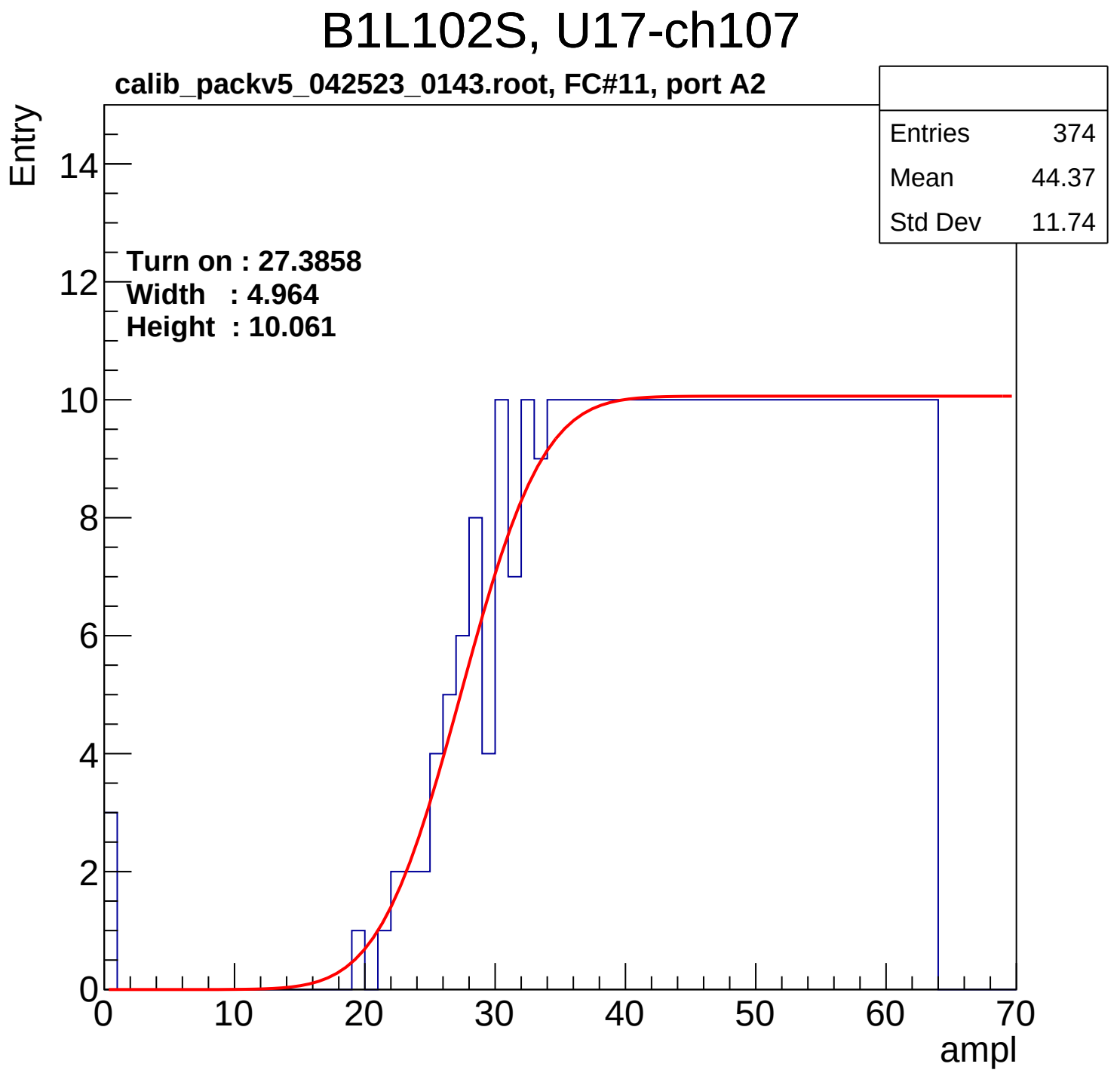
B1L102S, U17-ch107
calib_packv5_042523_0143.root, FC#11, port A2
Entries 374
Mean 44.37
Std Dev 11.74
Turn on : 27.3858
Width : 4.964
Height : 10.061
Entry
ampl
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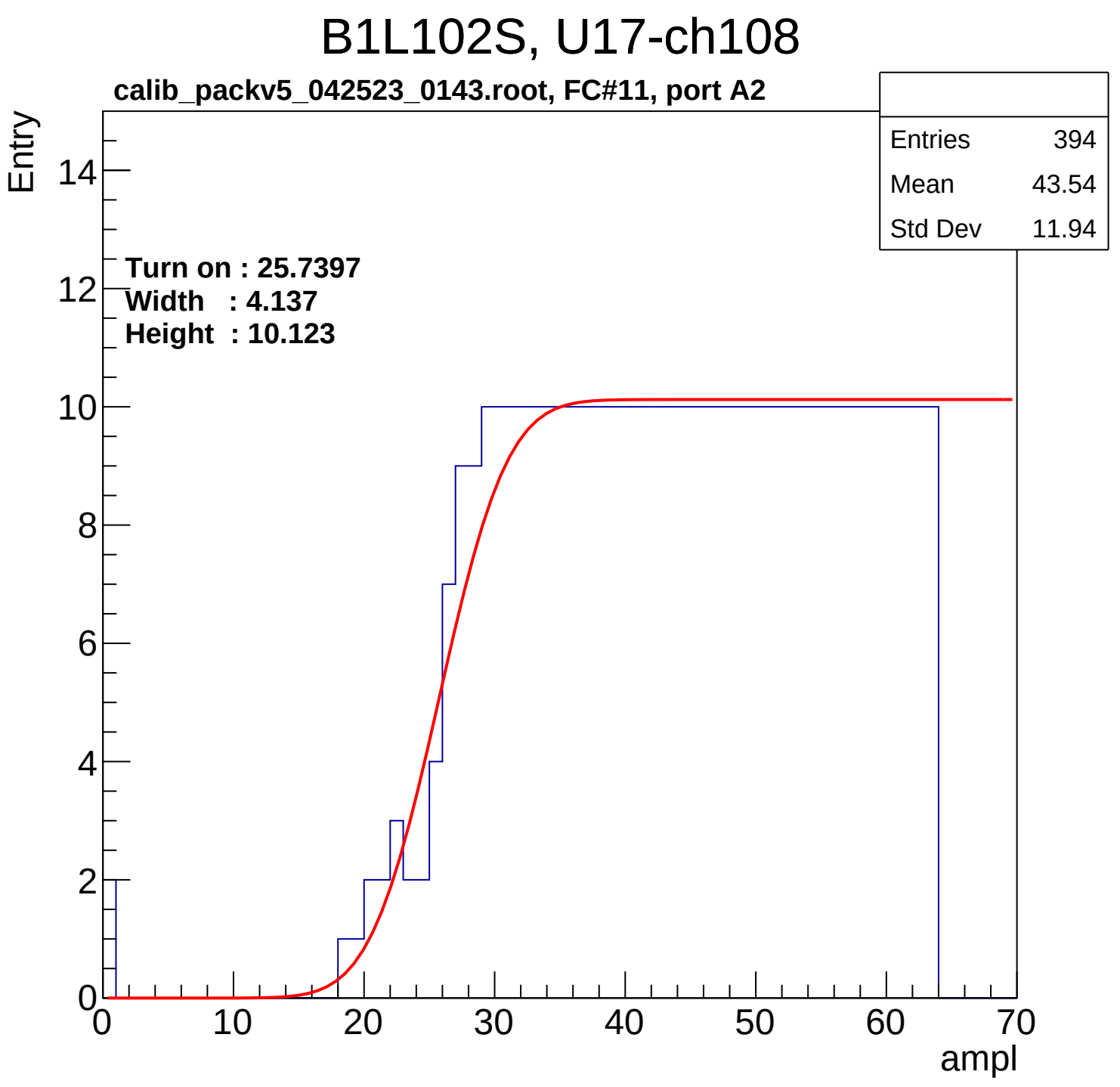
B1L102S, U17-ch108
calib_packv5_042523_0143.root, FC#11, port A2
Entries 394
Mean 43.54
Std Dev 11.94
Turn on : 25.7397
Width : 4.137
Height : 10.123
Entry
ampl
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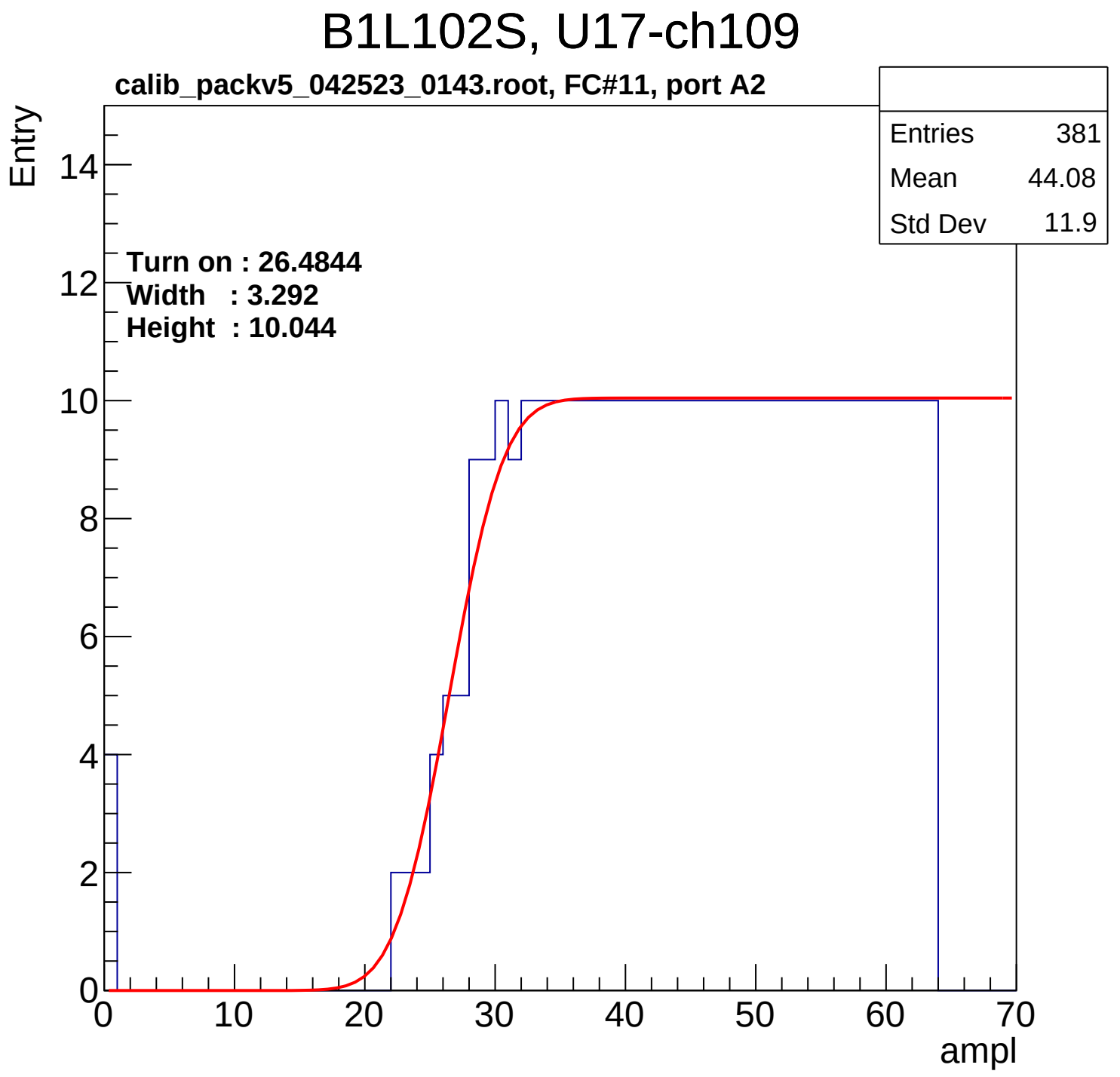
B1L102S, U17-ch109
calib_packv5_042523_0143.root, FC#11, port A2
Entries 381
Mean 44.08
Std Dev 11.9
Turn on : 26.4844
Width : 3.292
Height : 10.044
Entry
ampl
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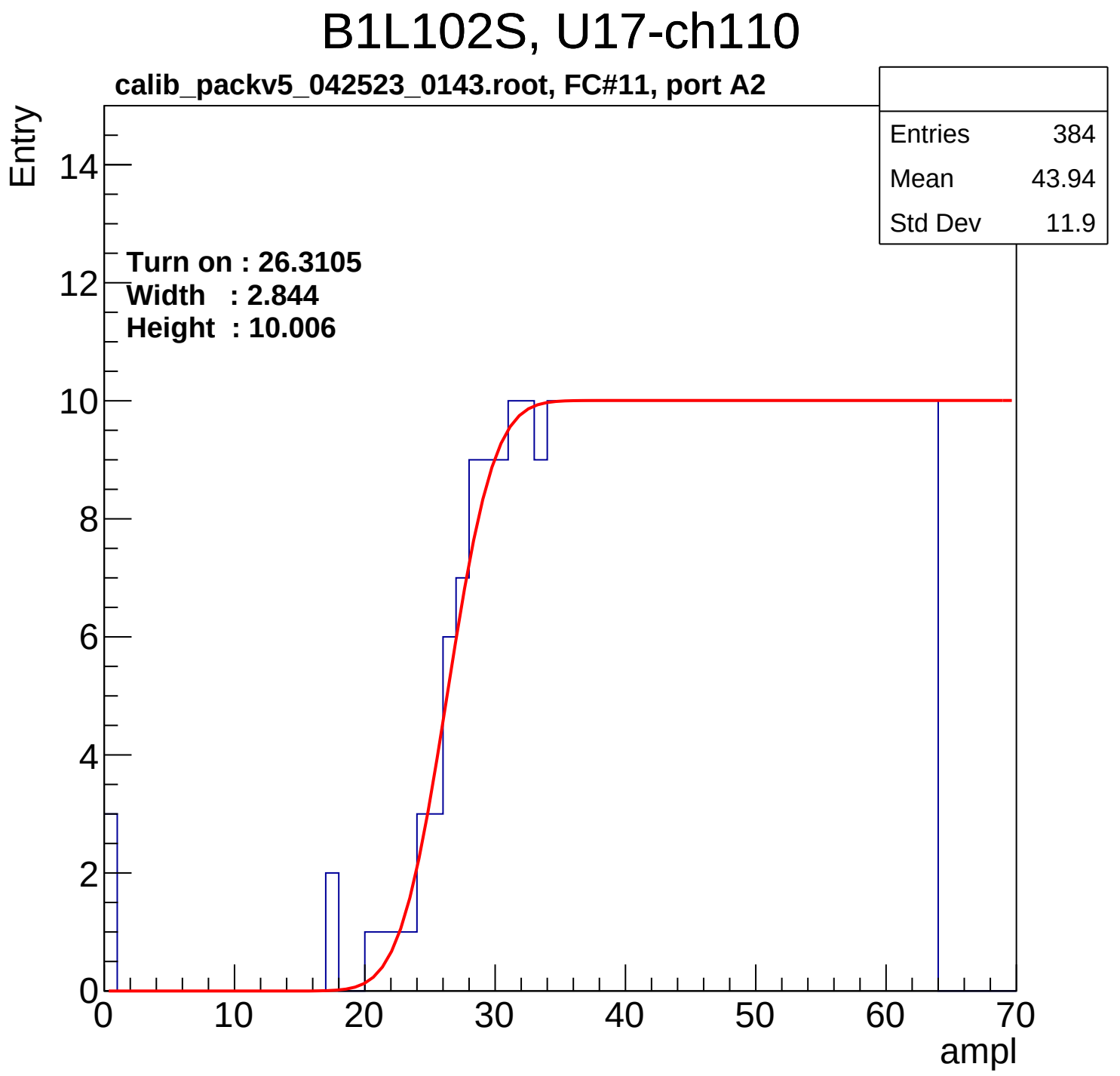
B1L102S, U17-ch110
calib_packv5_042523_0143.root, FC#11, port A2
Entries 384
Mean 43.94
Std Dev 11.9
Turn on : 26.3105
Width : 2.844
Height : 10.006
Entry
ampl
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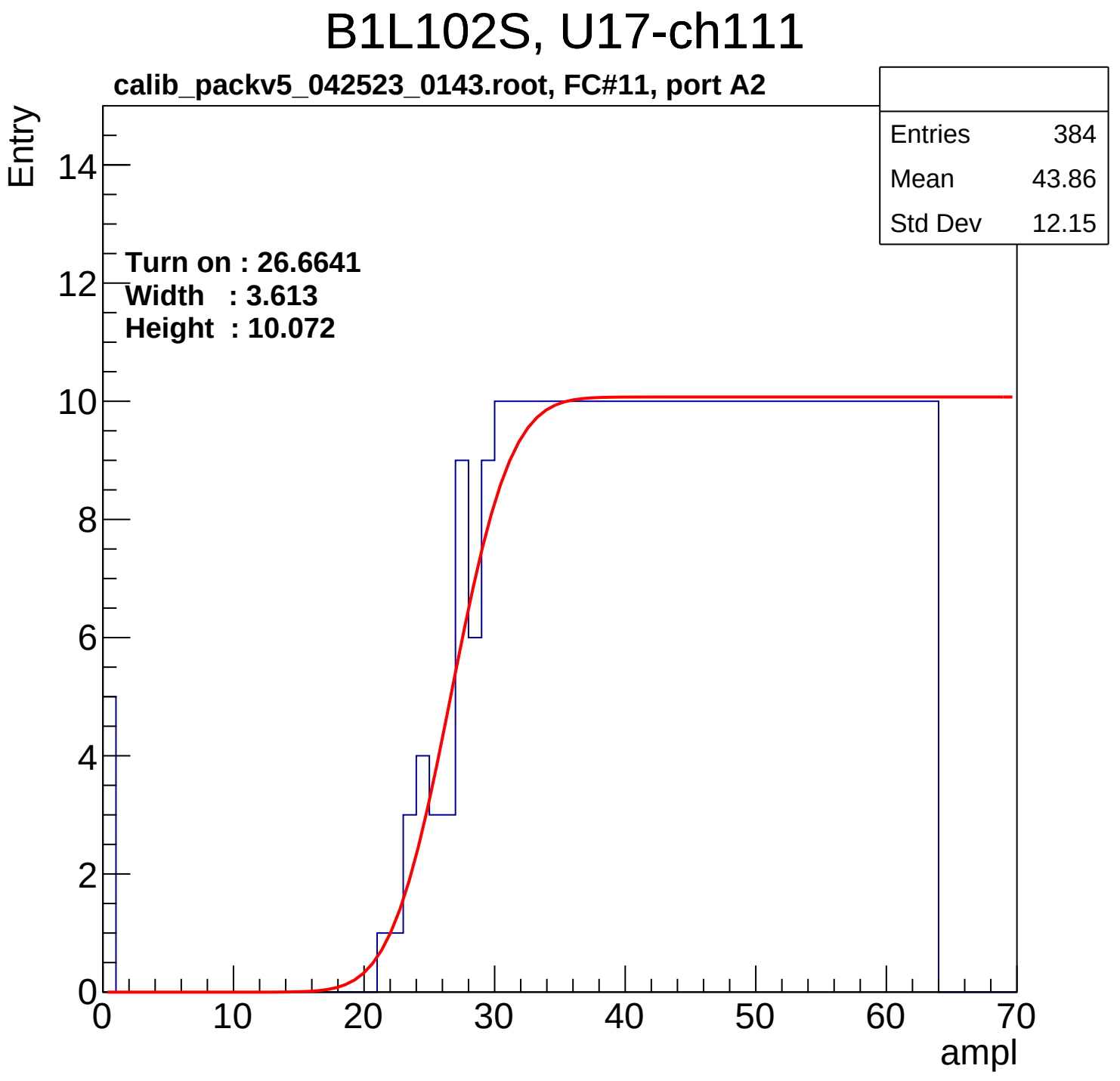
B1L102S, U17-ch111
calib_packv5_042523_0143.root, FC#11, port A2
Entries 384
Mean 43.86
Std Dev 12.15
Turn on : 26.6641
Width : 3.613
Height : 10.072
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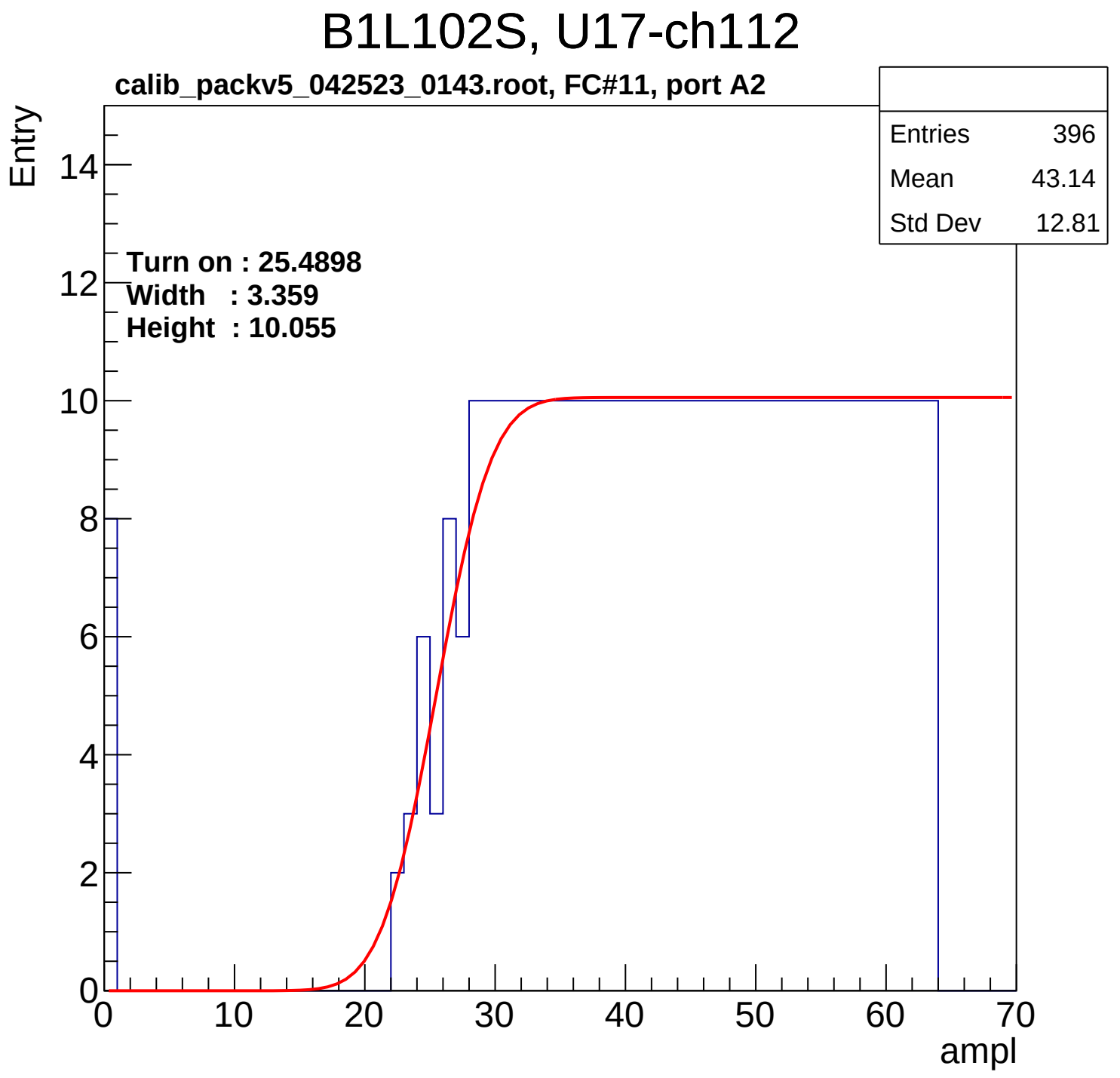
B1L102S, U17-ch112
calib_packv5_042523_0143.root, FC#11, port A2
Entries 396
Mean 43.14
Std Dev 12.81
Turn on : 25.4898
Width : 3.359
Height : 10.055
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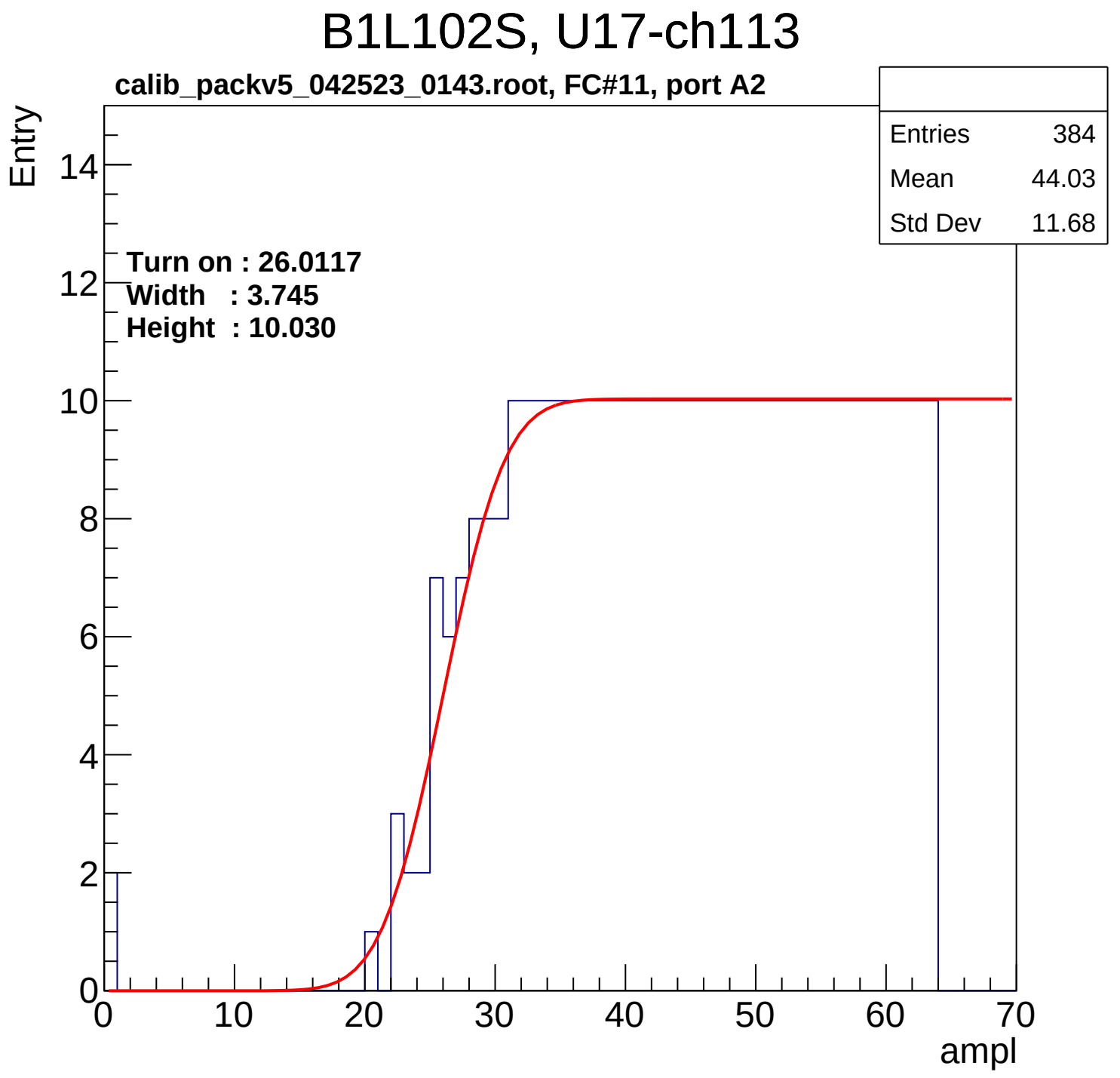
B1L102S, U17-ch113
calib_packv5_042523_0143.root, FC#11, port A2
Entries 384
Mean 44.03
Std Dev 11.68
Turn on : 26.0117
Width : 3.745
Height : 10.030
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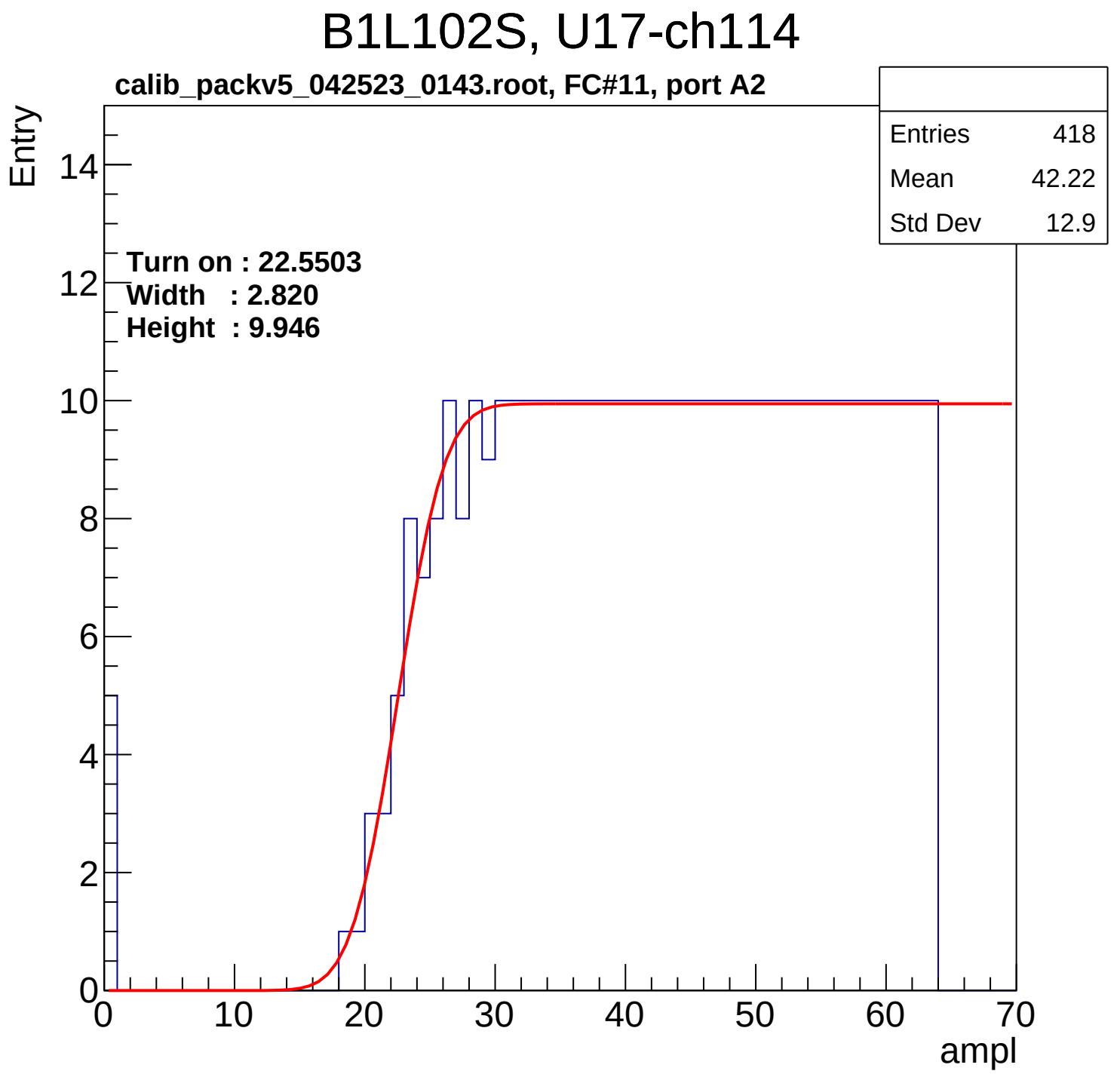
B1L102S, U17-ch114
calib_packv5_042523_0143.root, FC#11, port A2
Entries 418
Mean 42.22
Std Dev 12.9
Turn on : 22.5503
Width : 2.820
Height : 9.946
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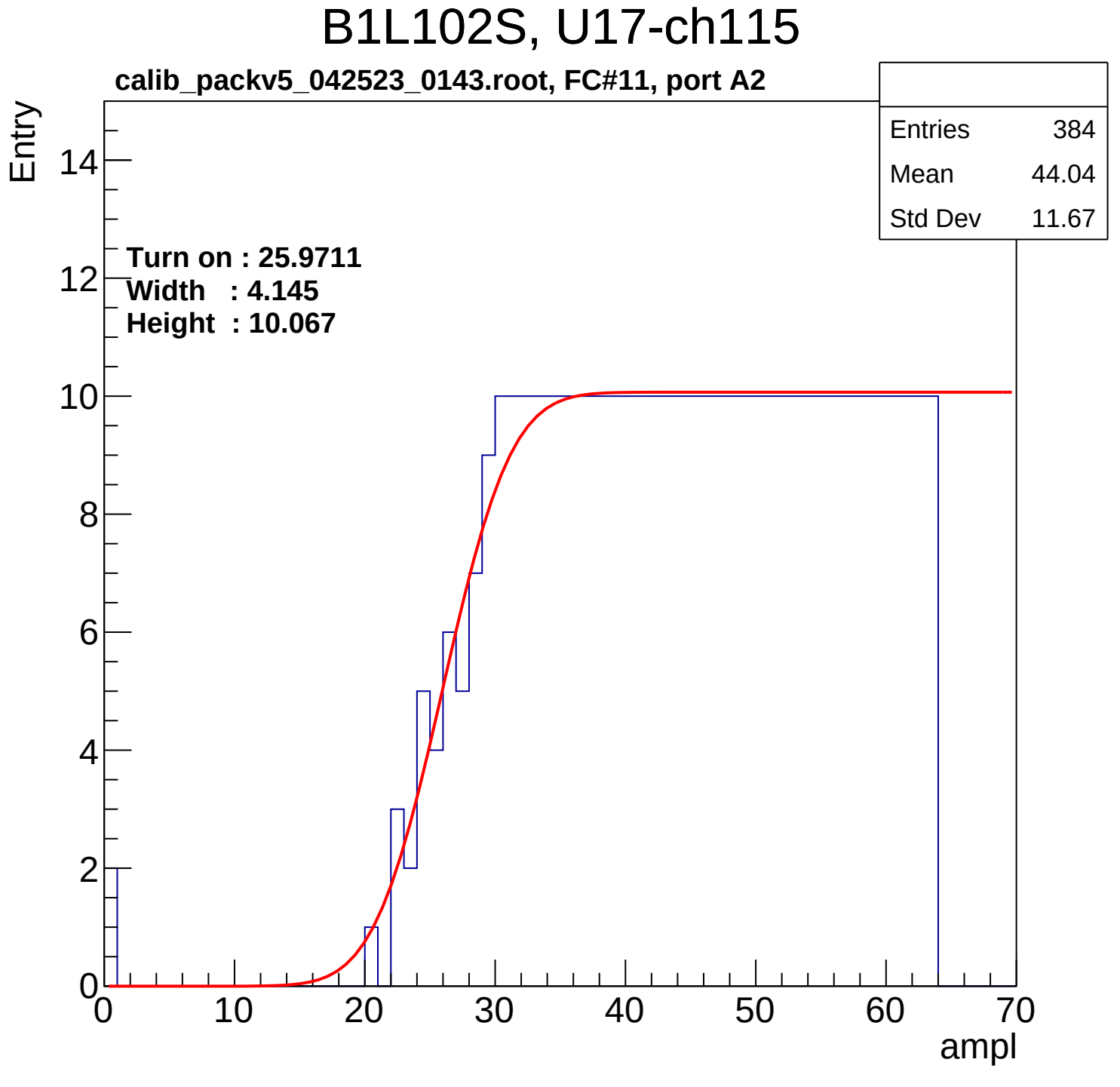
B1L102S, U17-ch115
calib_packv5_042523_0143.root, FC#11, port A2
Entries 384
Mean 44.04
Std Dev 11.67
Turn on : 25.9711
Width : 4.145
Height : 10.067
Entry
ampl
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6
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20
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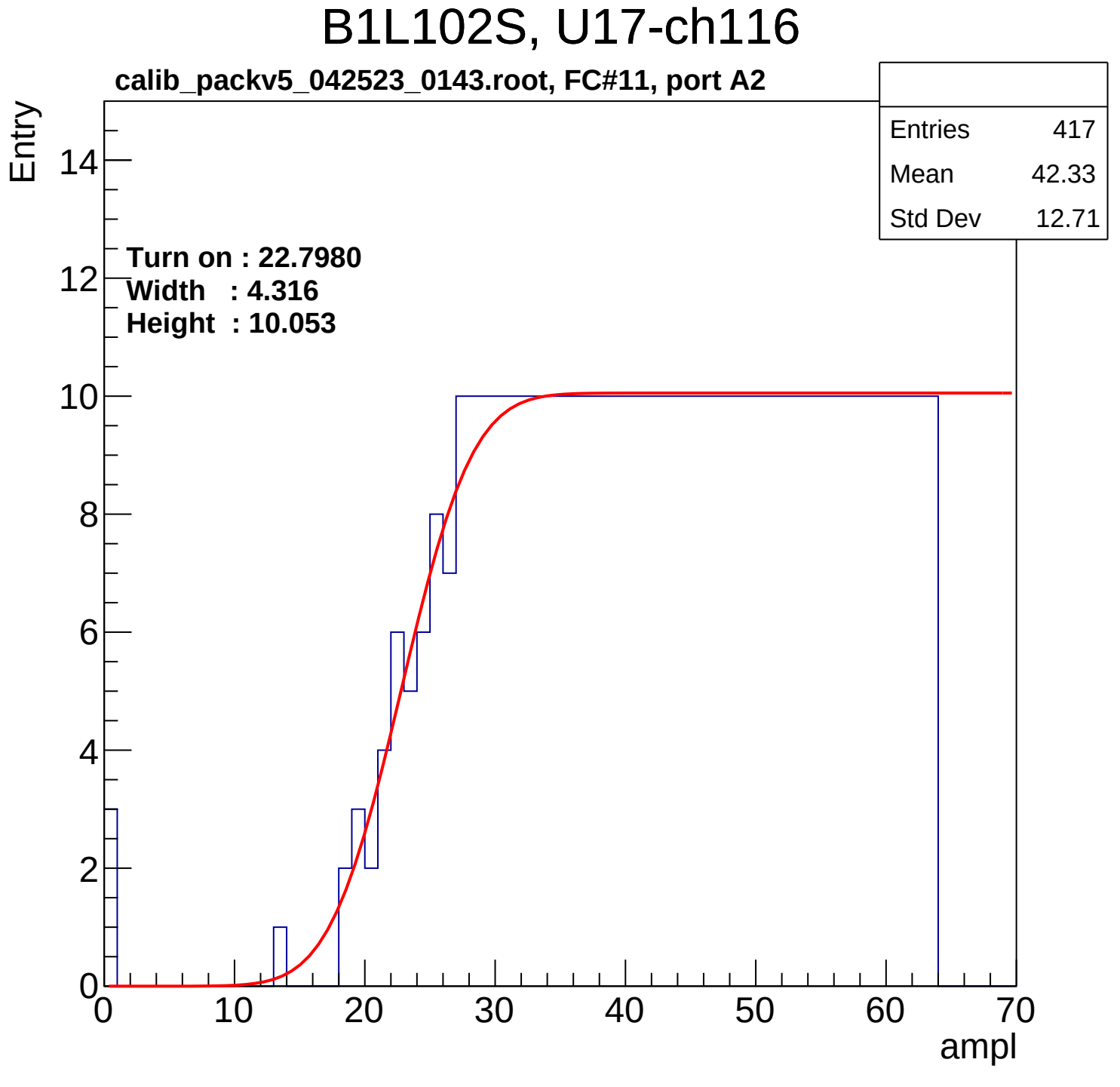
B1L102S, U17-ch116
calib_packv5_042523_0143.root, FC#11, port A2
Entries 417
Mean 42.33
Std Dev 12.71
Turn on : 22.7980
Width : 4.316
Height : 10.053
Entry
ampl
0
2
4
6
8
10
12
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0
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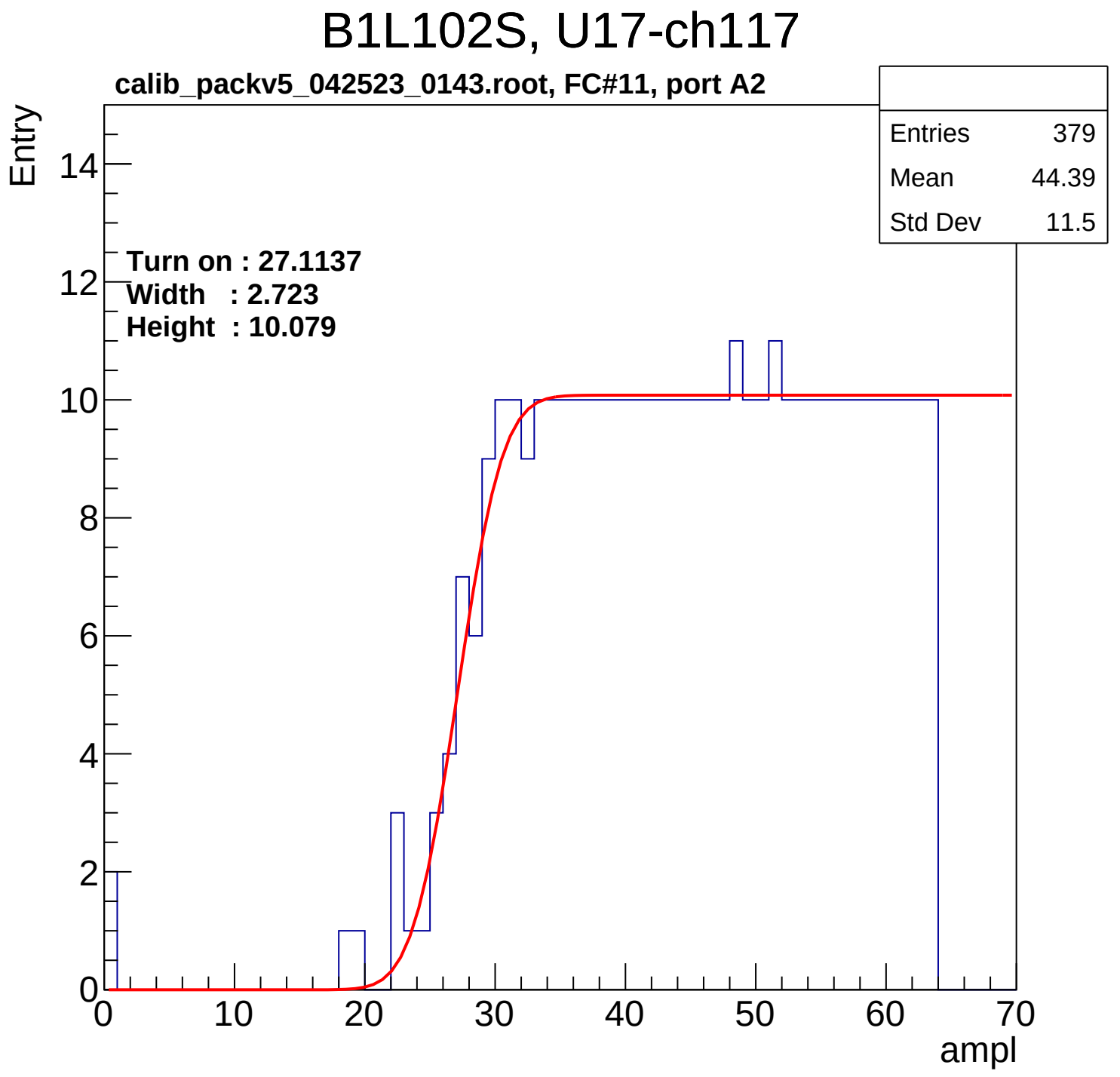
B1L102S, U17-ch117
calib_packv5_042523_0143.root, FC#11, port A2
Entries 379
Mean 44.39
Std Dev 11.5
Turn on : 27.1137
Width : 2.723
Height : 10.079
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
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60
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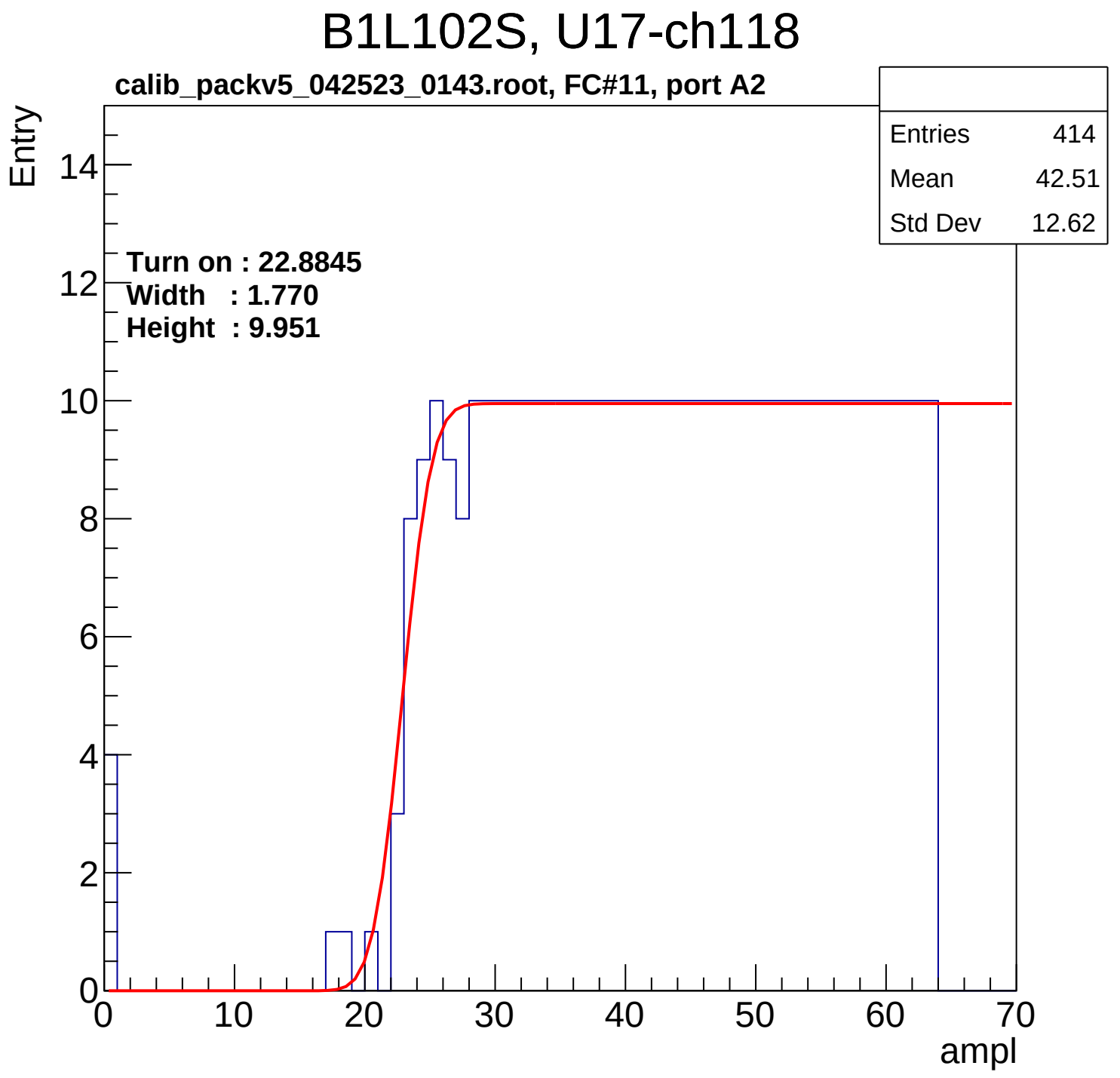
B1L102S, U17-ch118
calib_packv5_042523_0143.root, FC#11, port A2
Entries 414
Mean 42.51
Std Dev 12.62
Turn on : 22.8845
Width : 1.770
Height : 9.951
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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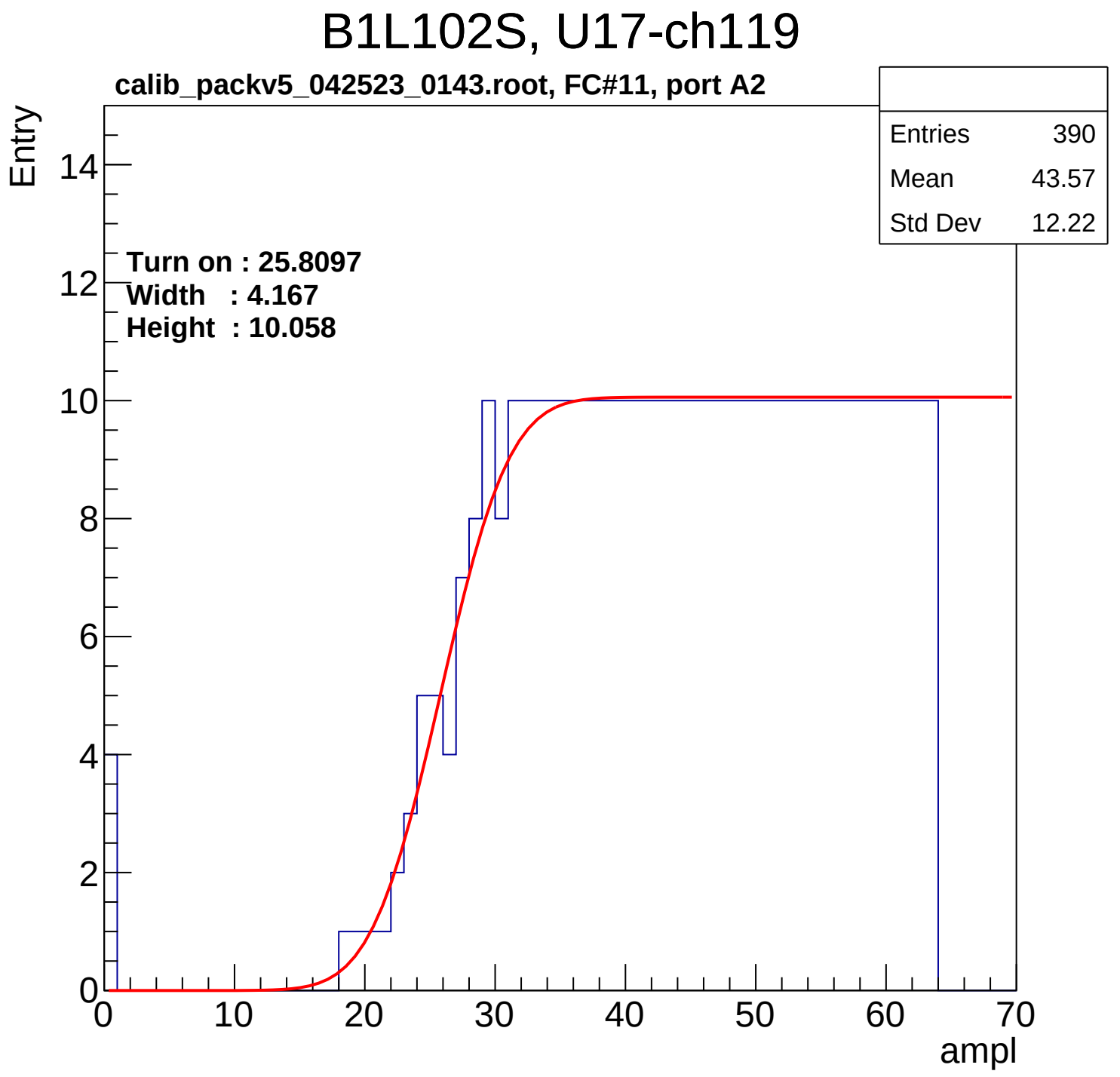
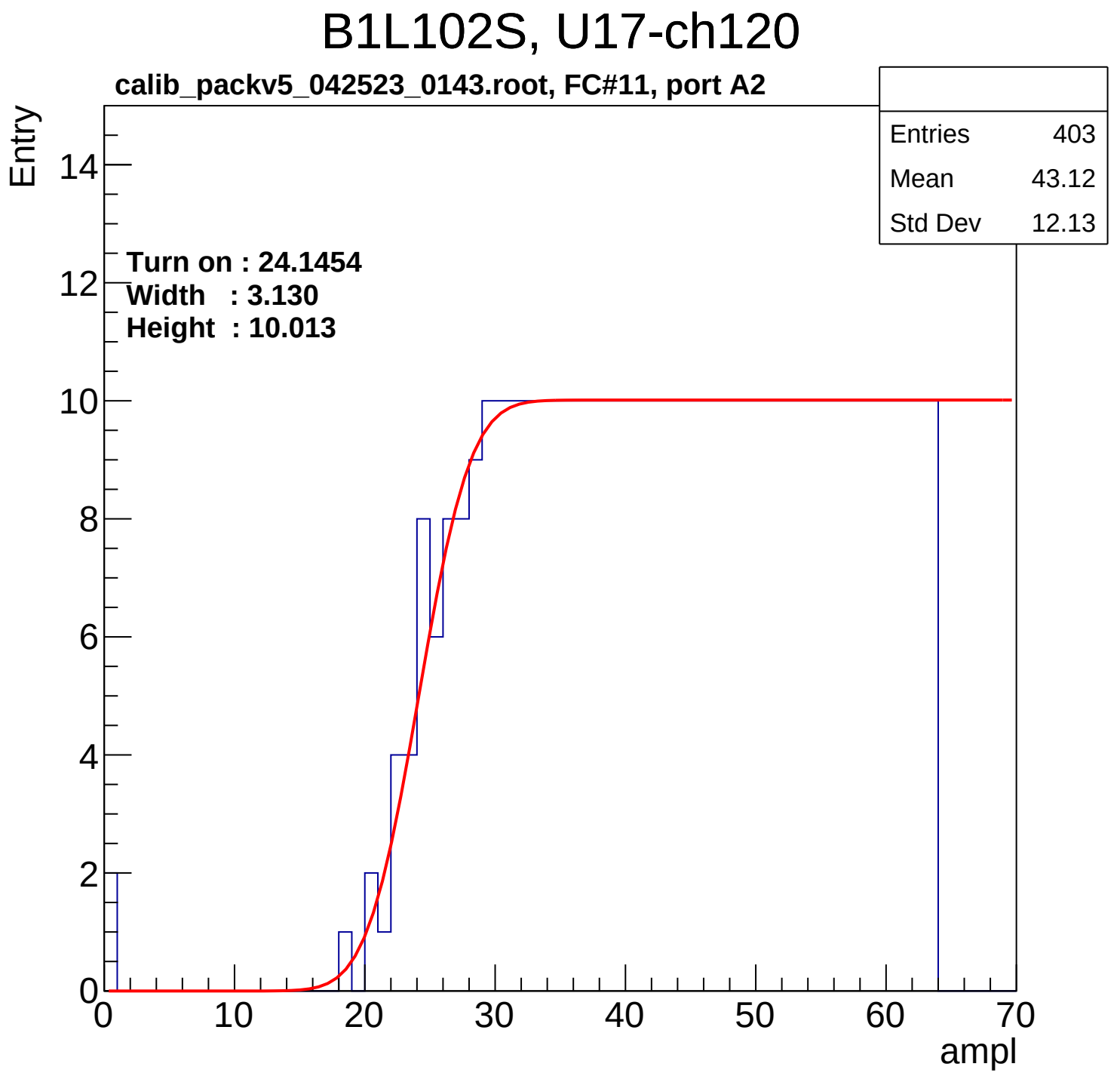
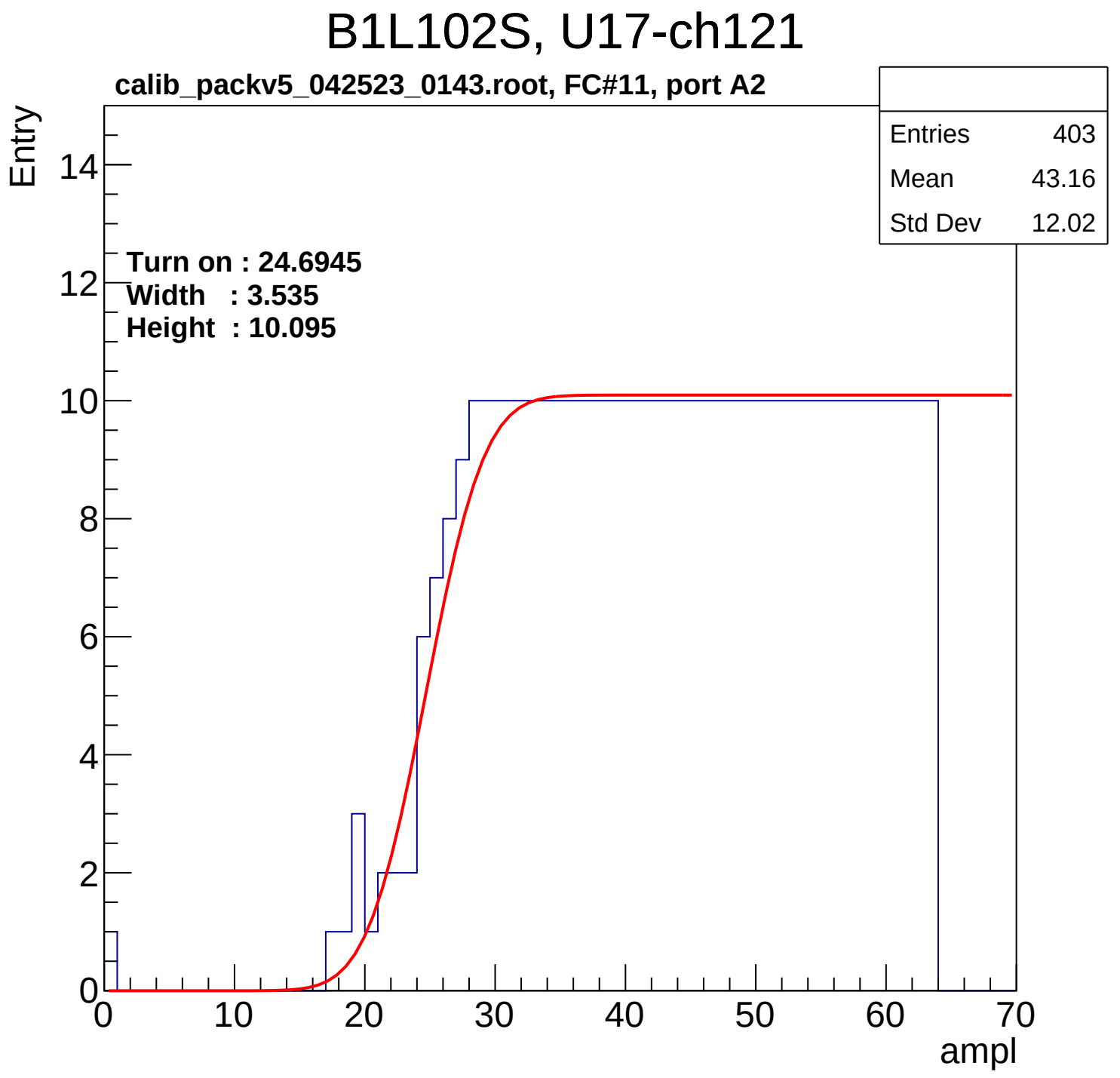
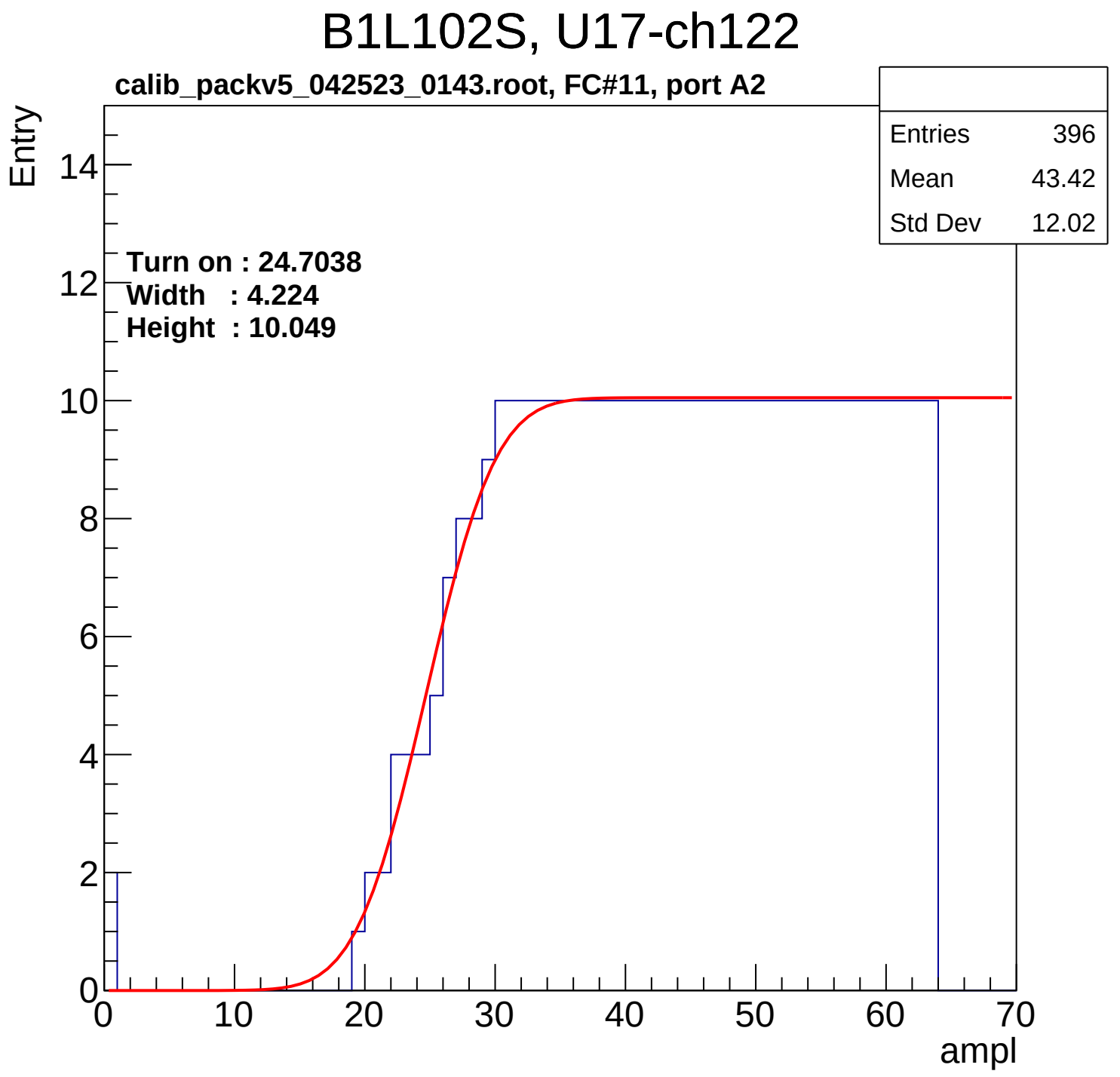
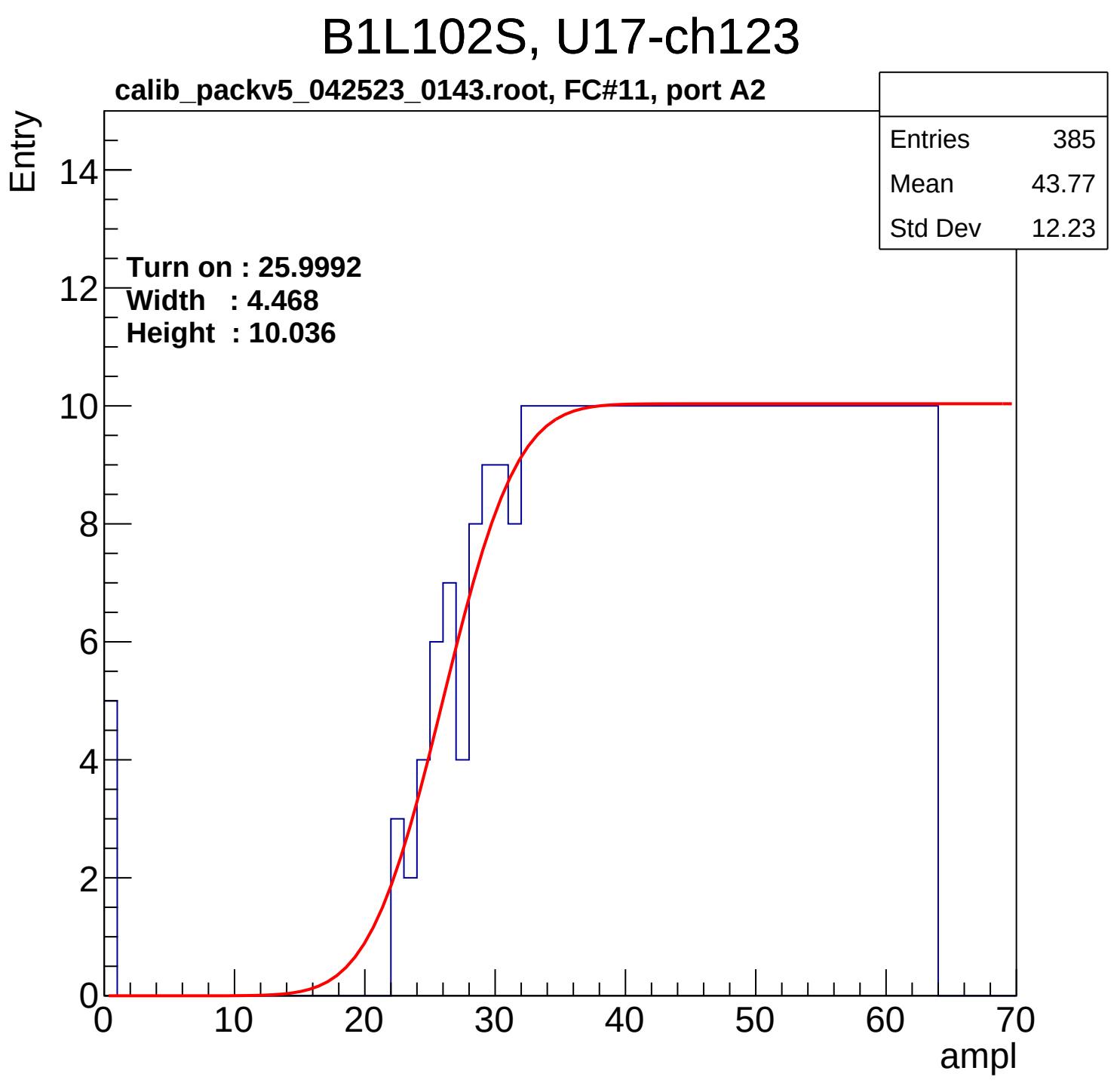
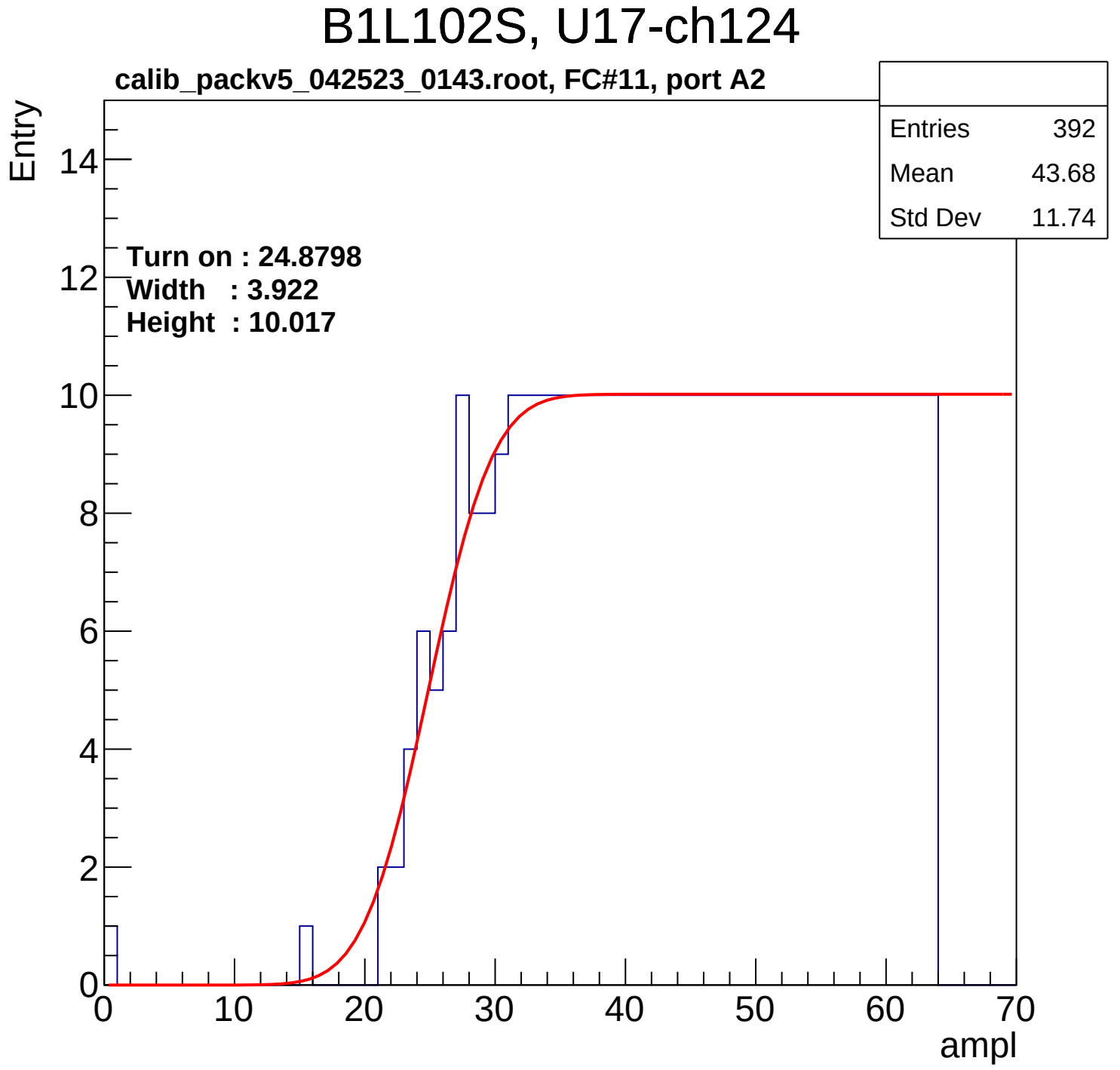

B1L102S, U17-ch119
calib_packv5_042523_0143.root, FC#11, port A2
Entries 390
Mean 43.57
Std Dev 12.22
Turn on : 25.8097
Width : 4.167
Height : 10.058
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

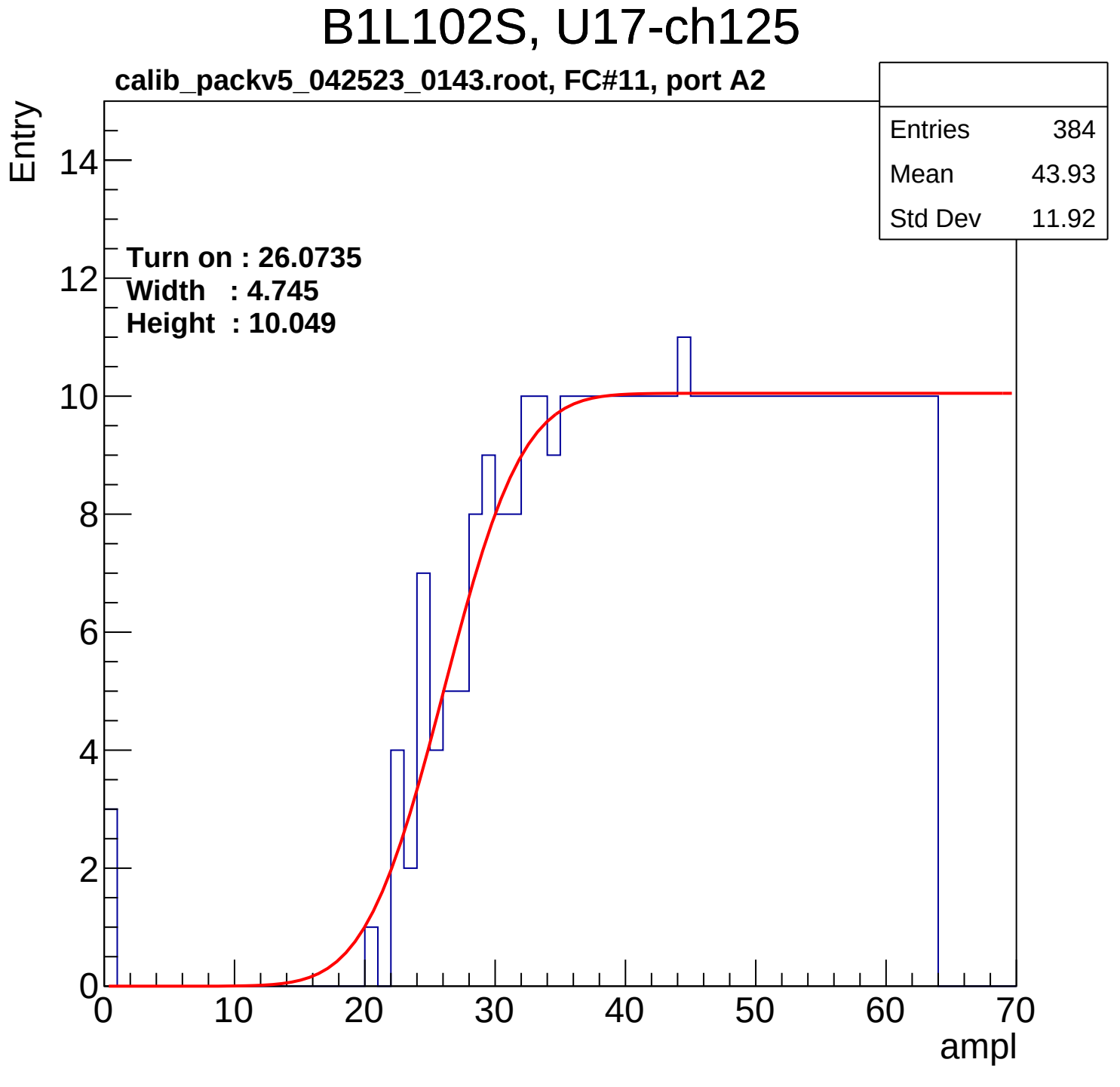

B1L102S, U17-ch120
calib_packv5_042523_0143.root, FC#11, port A2
Entries 403
Mean 43.12
Std Dev 12.13
Turn on : 24.1454
Width : 3.130
Height : 10.013
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

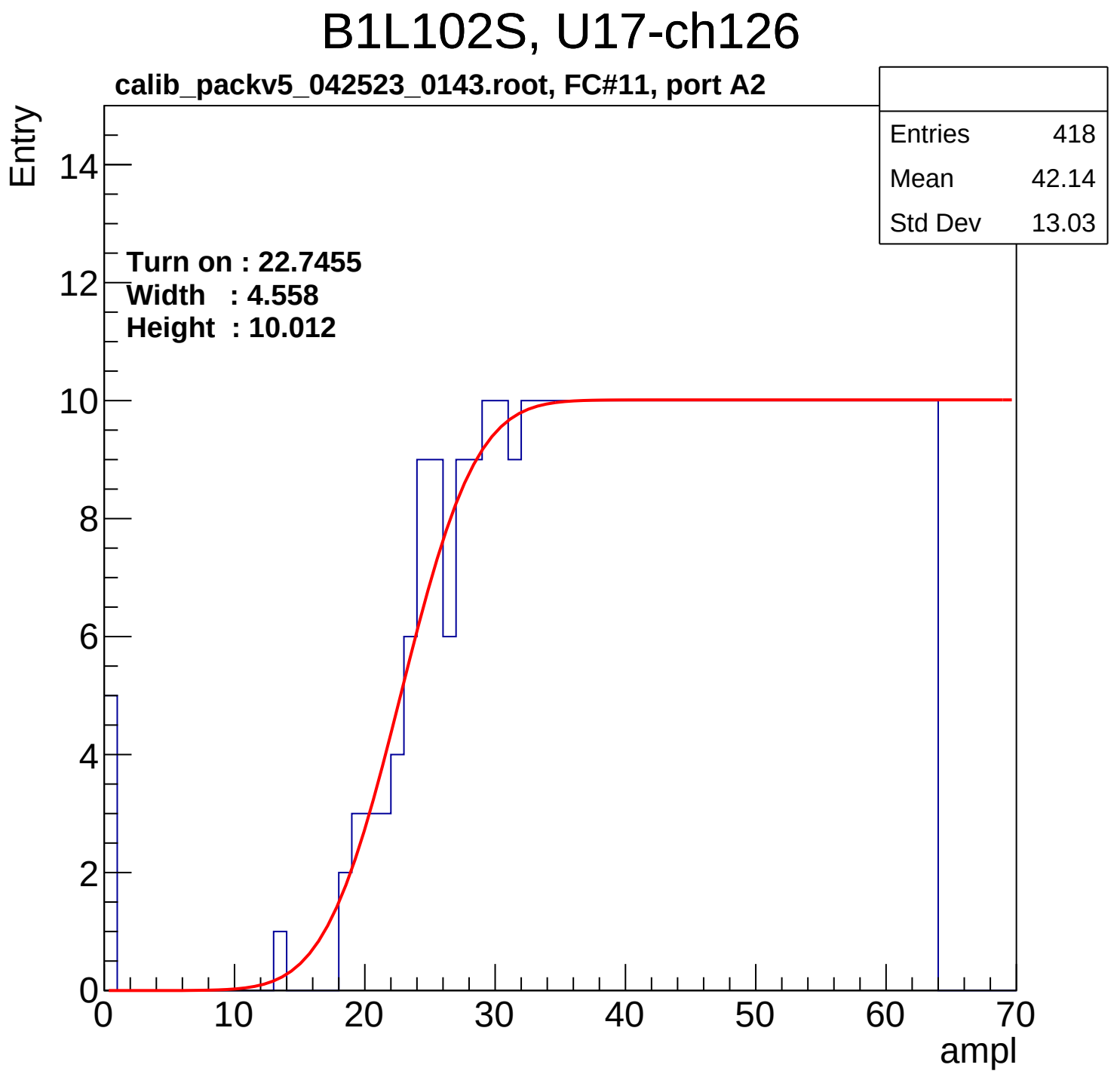

B1L102S, U17-ch121
calib_packv5_042523_0143.root, FC#11, port A2
Entries 403
Mean 43.16
Std Dev 12.02
Turn on : 24.6945
Width : 3.535
Height : 10.095
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L102S, U17-ch122
calib_packv5_042523_0143.root, FC#11, port A2
Entries 396
Mean 43.42
Std Dev 12.02
Turn on : 24.7038
Width : 4.224
Height : 10.049
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L102S, U17-ch123
calib_packv5_042523_0143.root, FC#11, port A2
Entries 385
Mean 43.77
Std Dev 12.23
Turn on : 25.9992
Width : 4.468
Height : 10.036
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L102S, U17-ch124
calib_packv5_042523_0143.root, FC#11, port A2
Entries 392
Mean 43.68
Std Dev 11.74
Turn on : 24.8798
Width : 3.922
Height : 10.017
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L102S, U17-ch125
calib_packv5_042523_0143.root, FC#11, port A2
Entries 384
Mean 43.93
Std Dev 11.92
Turn on : 26.0735
Width : 4.745
Height : 10.049
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L102S, U17-ch126
calib_packv5_042523_0143.root, FC#11, port A2
Entries 418
Mean 42.14
Std Dev 13.03
Turn on : 22.7455
Width : 4.558
Height : 10.012
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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40
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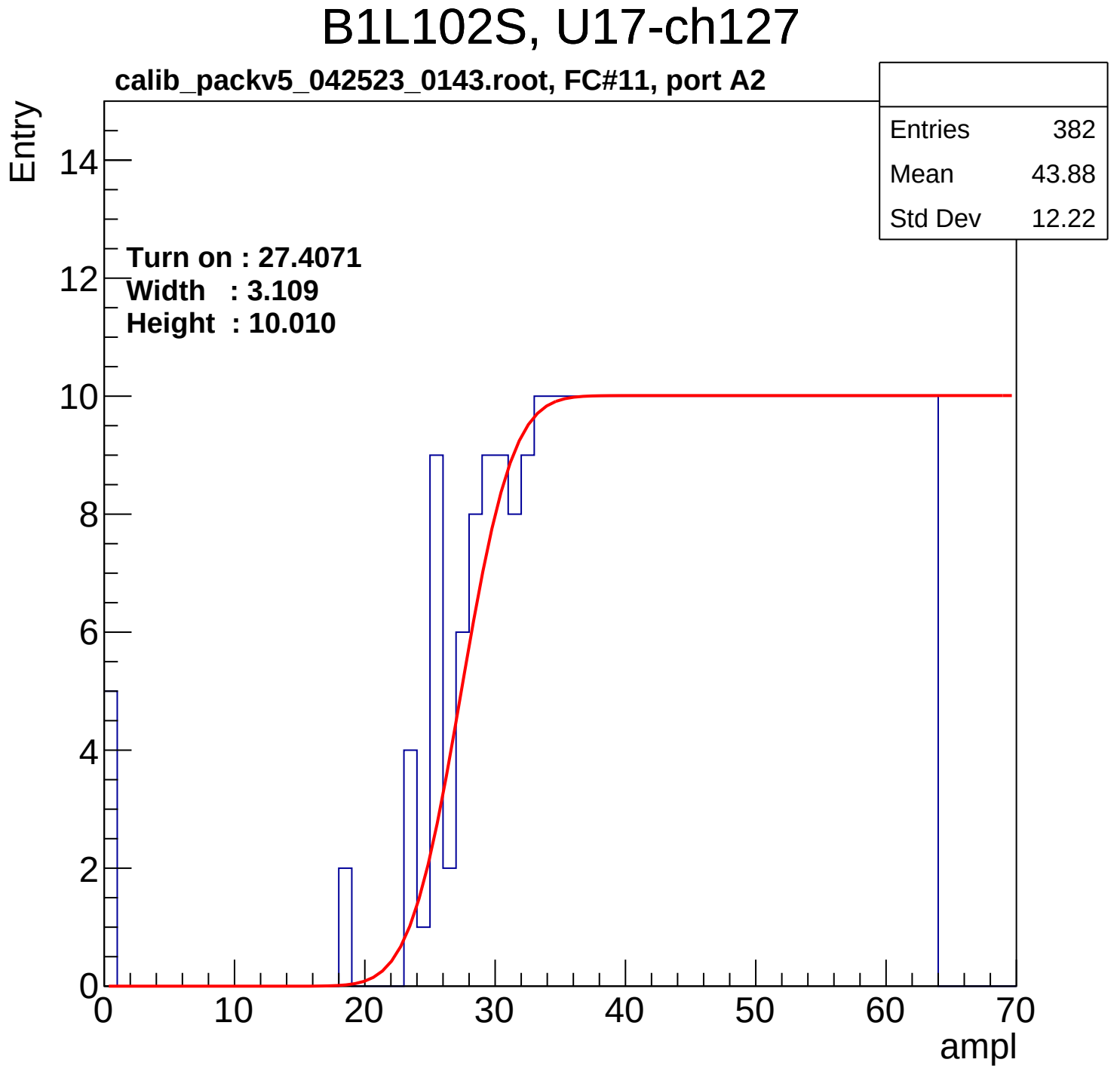
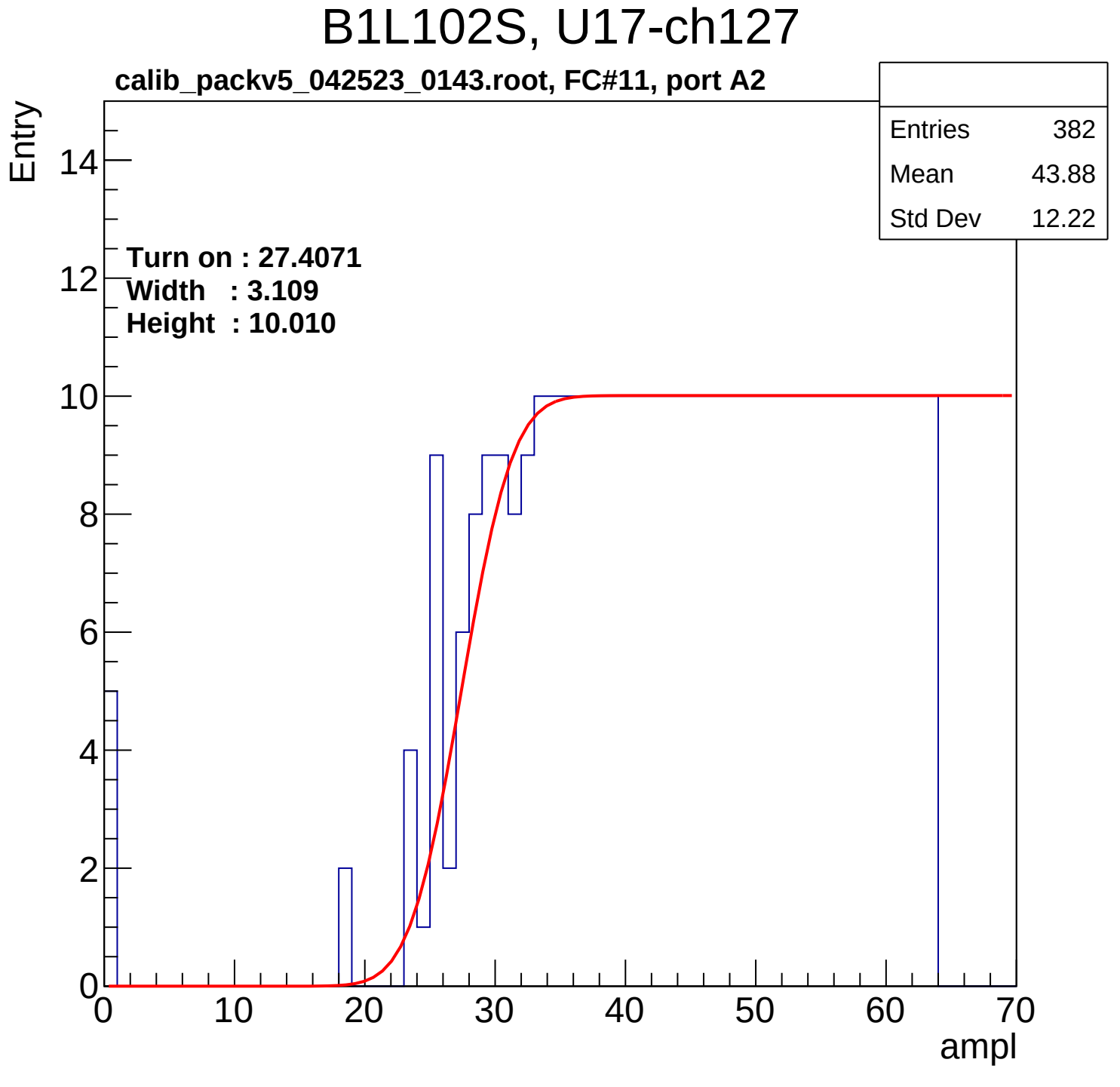
60
70


B1L102S, U17-ch127
calib_packv5_042523_0143.root, FC#11, port A2
Entries 382
Mean 43.88
Std Dev 12.22
Turn on : 27.4071
Width : 3.109
Height : 10.010
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L102S, U17-ch127
calib_packv5_042523_0143.root, FC#11, port A2
Entries 382
Mean 43.88
Std Dev 12.22
Turn on : 27.4071
Width : 3.109
Height : 10.010
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70