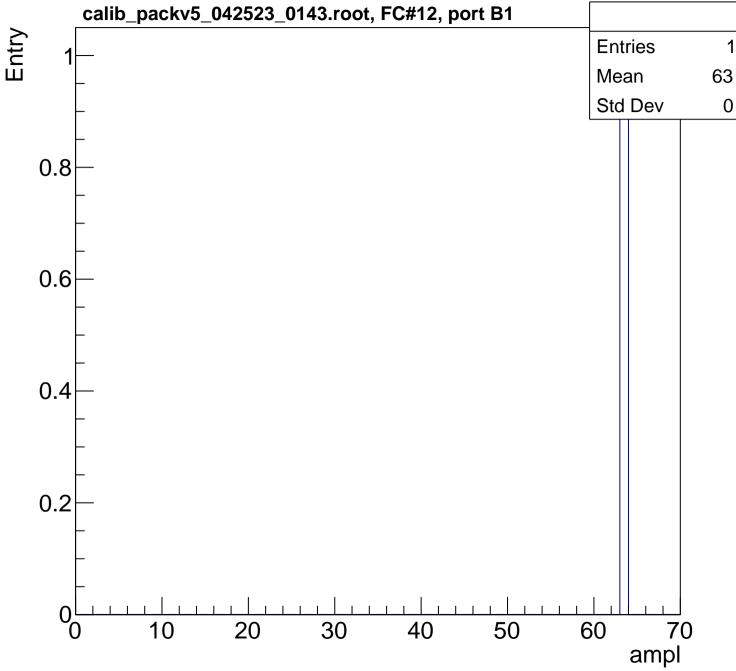
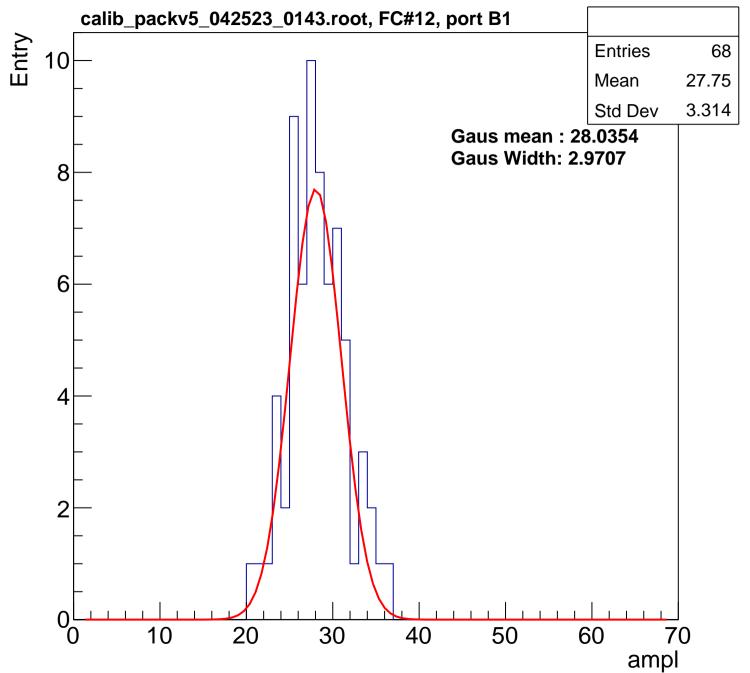
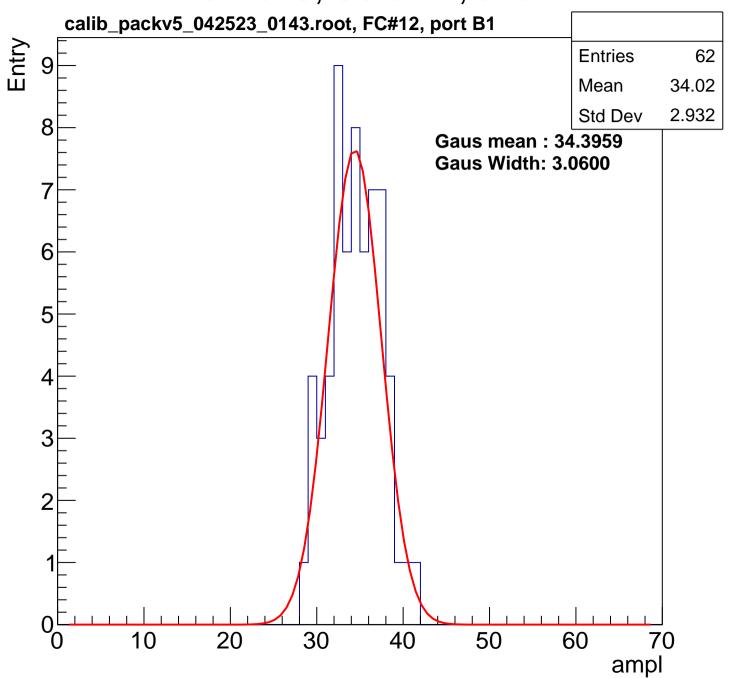
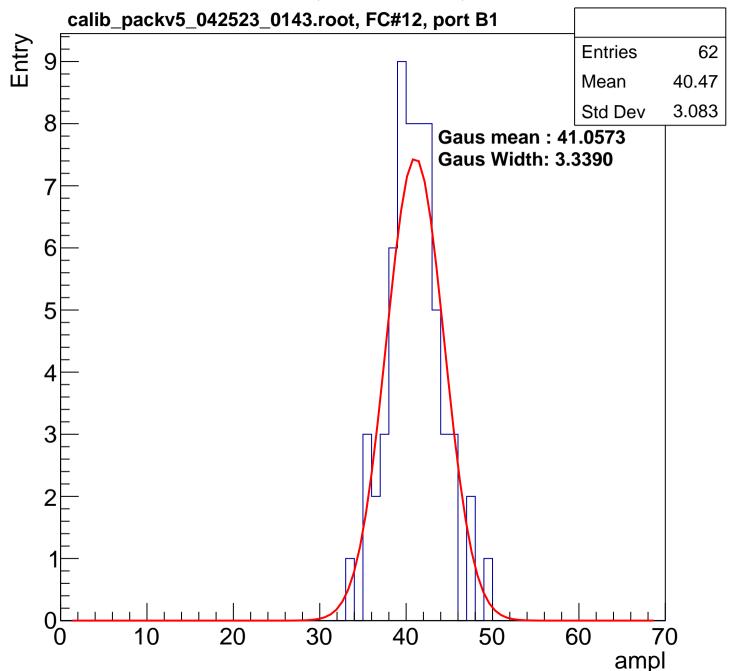


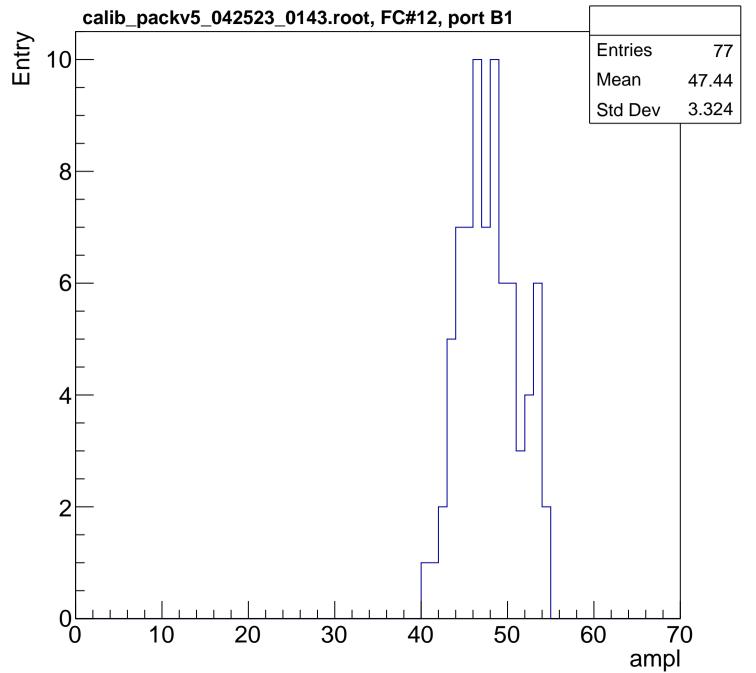
0

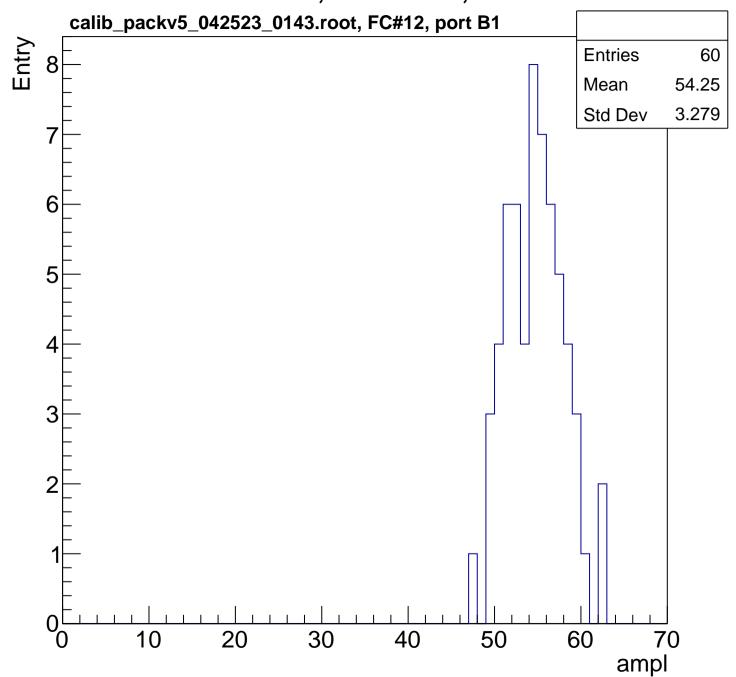


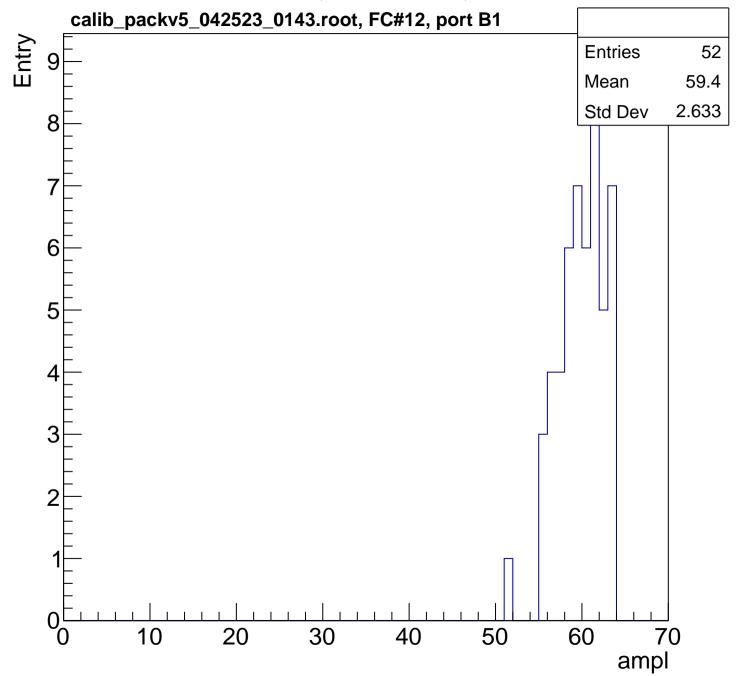


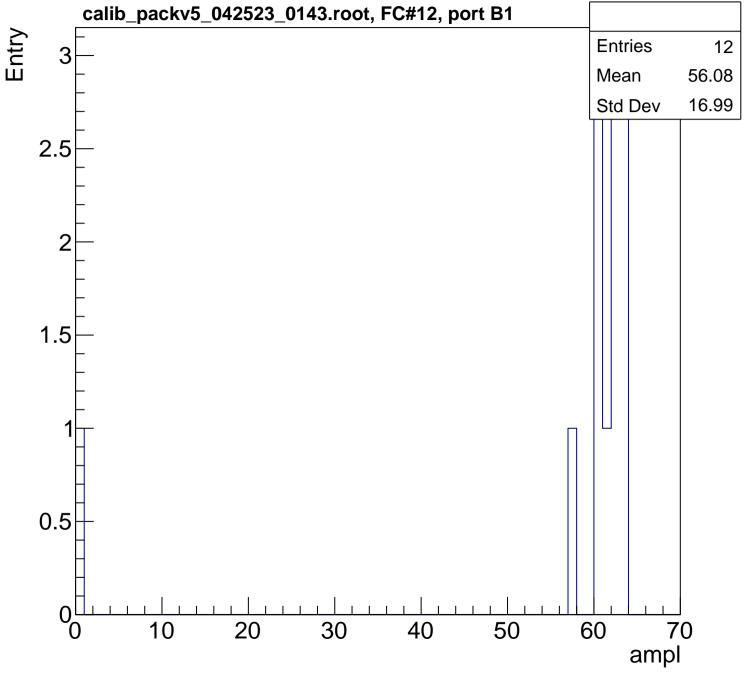




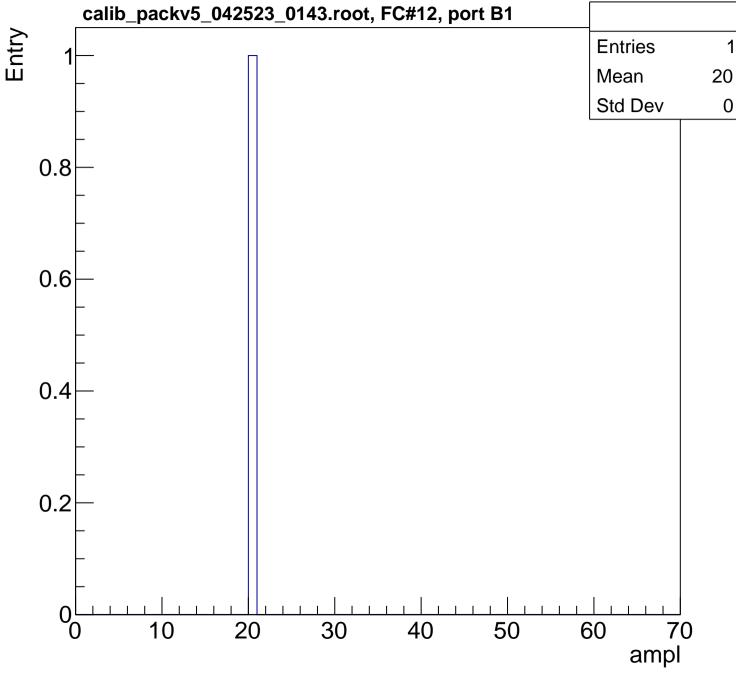


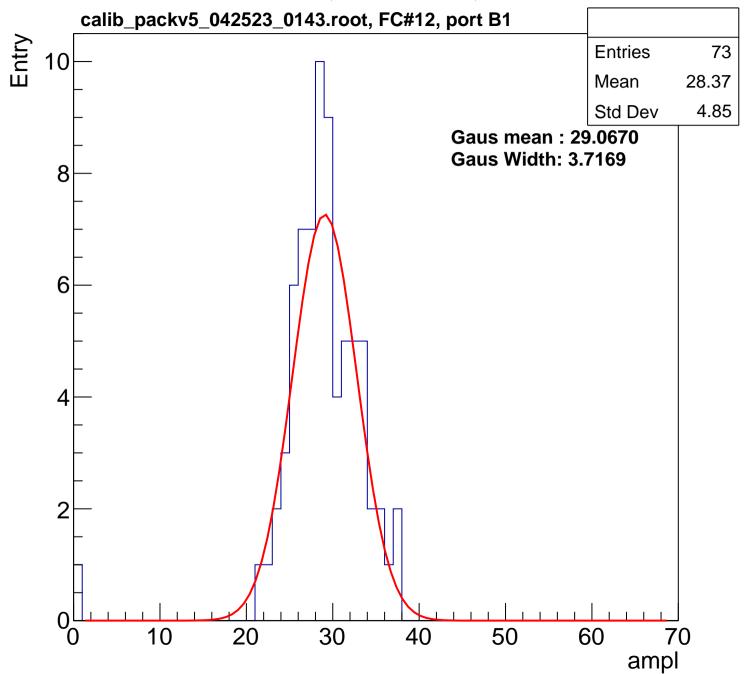


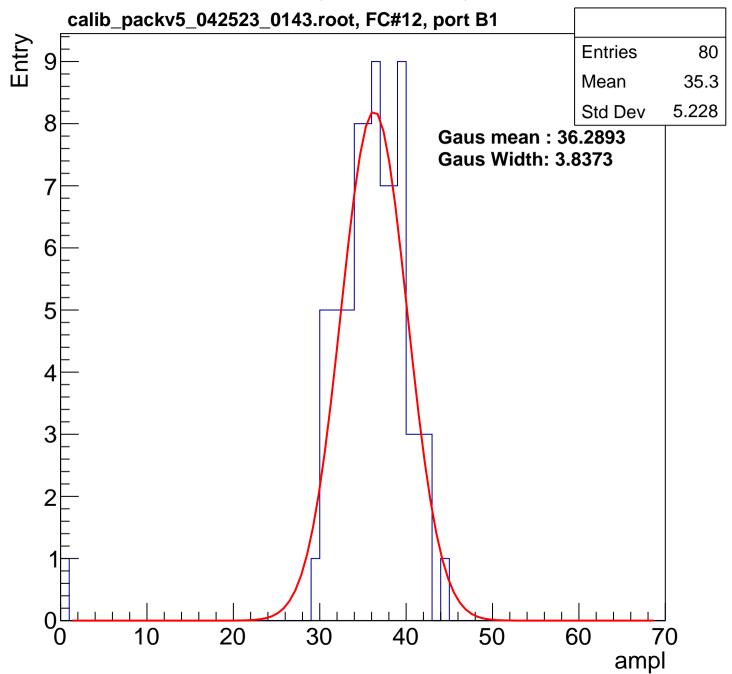


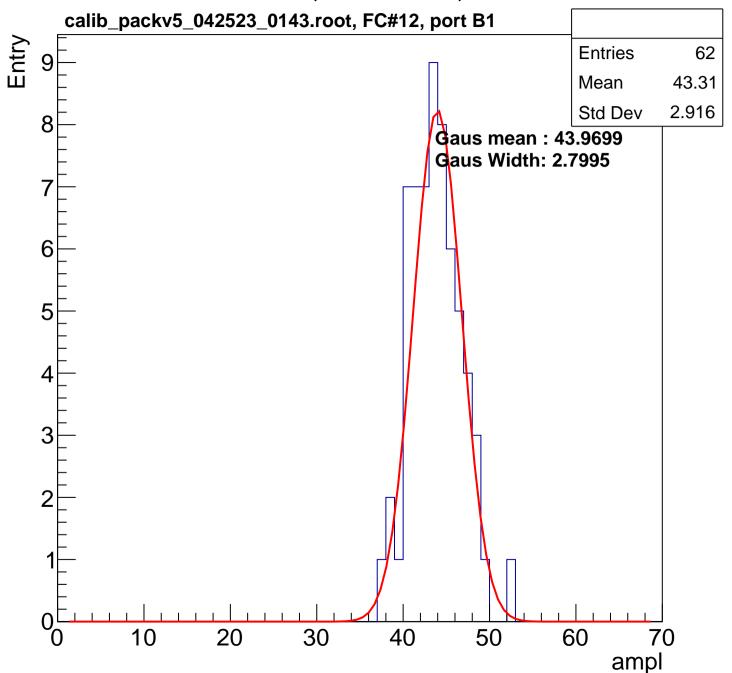


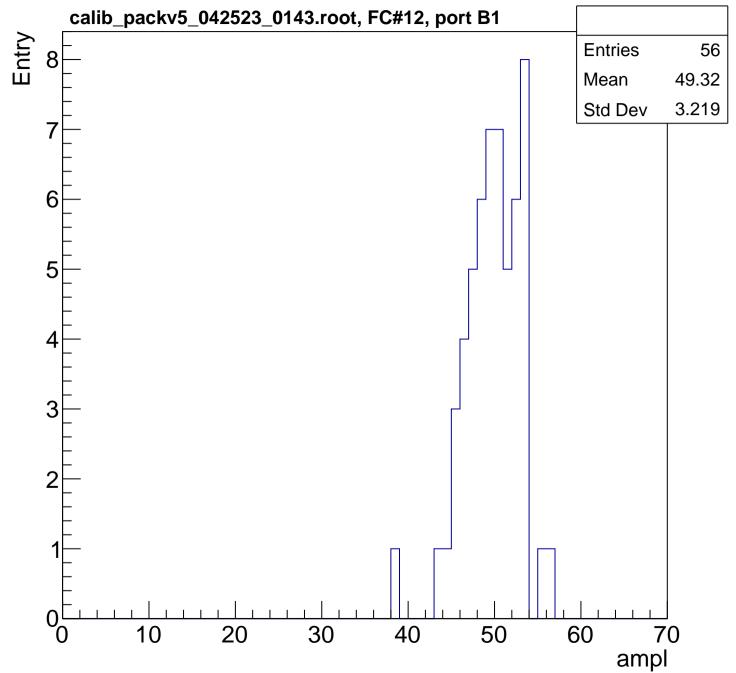
0

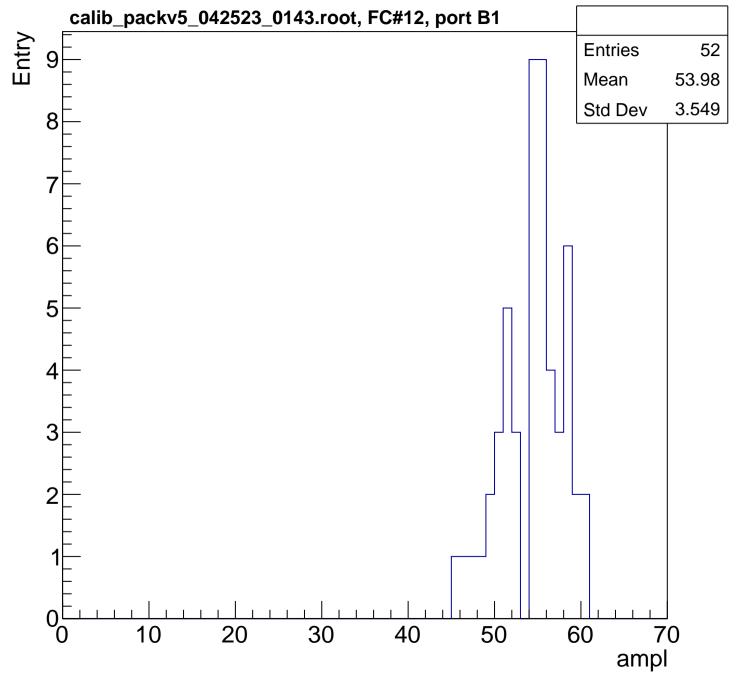


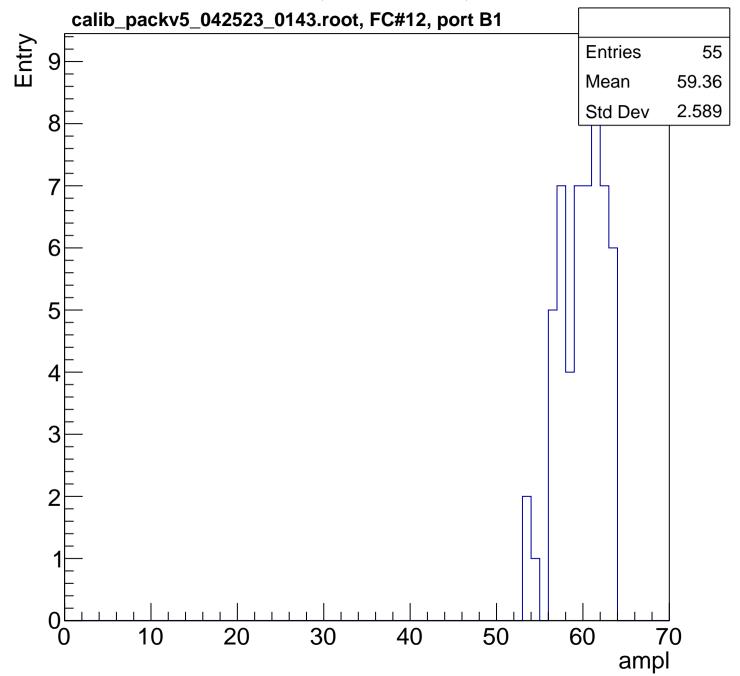


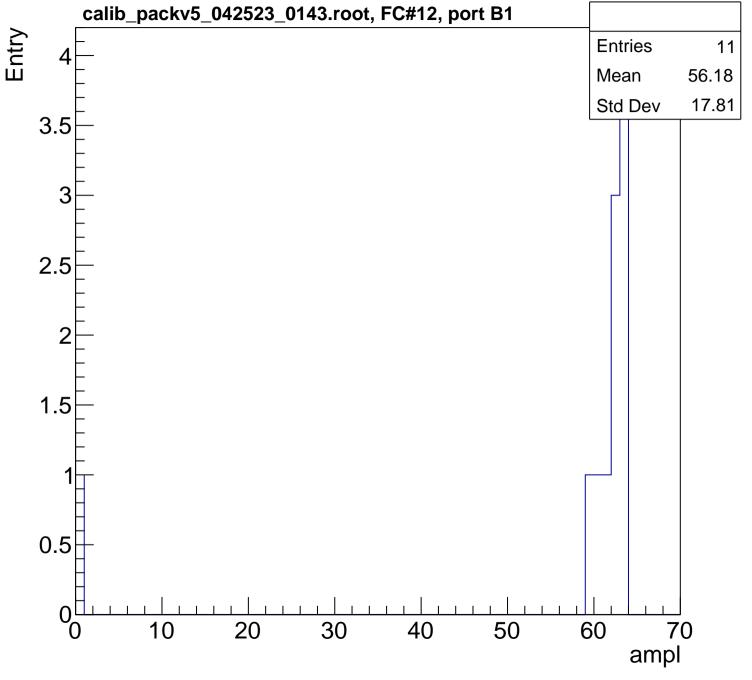


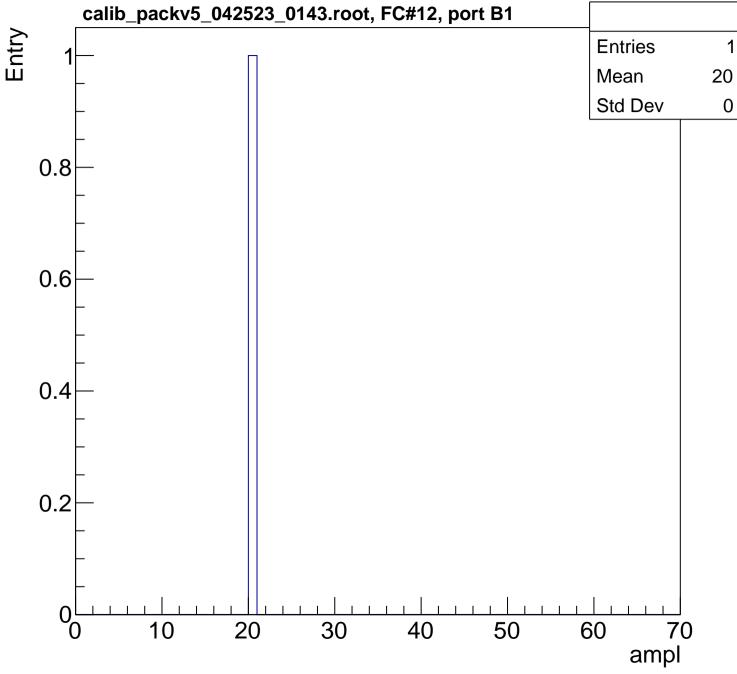


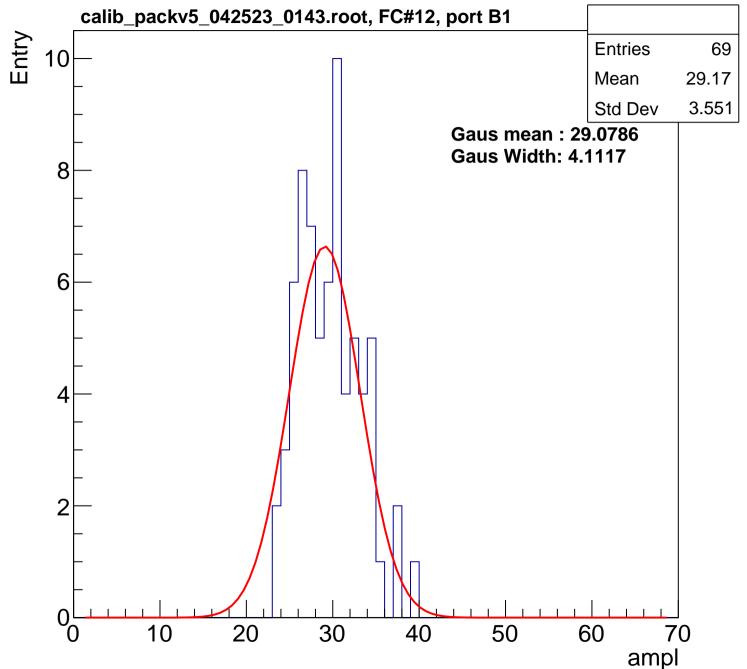


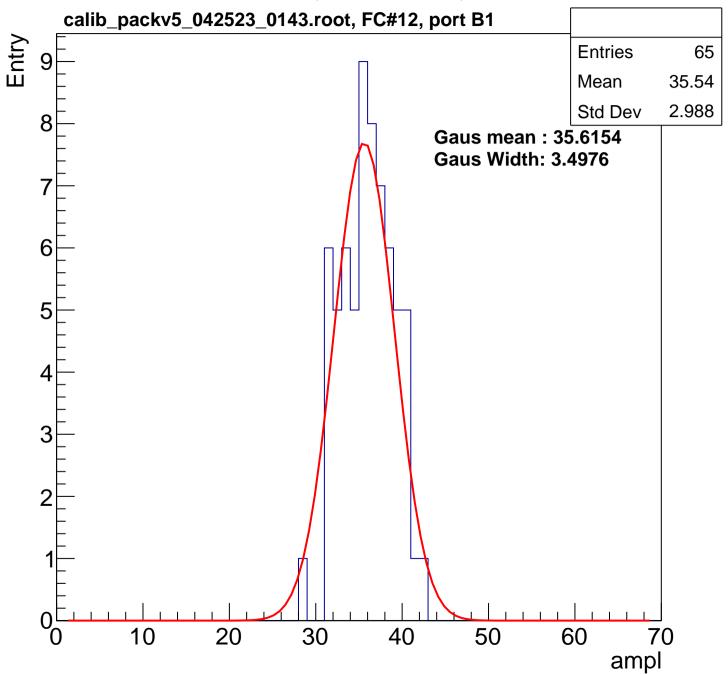


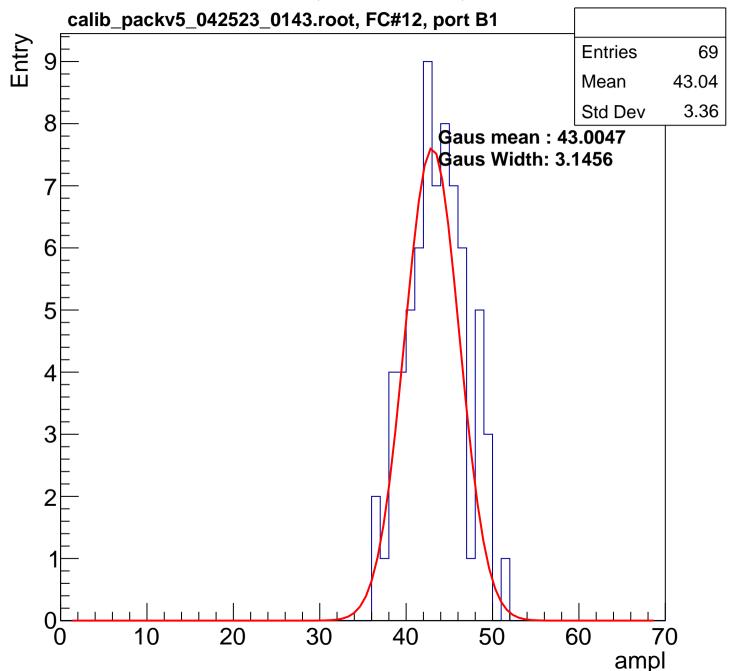


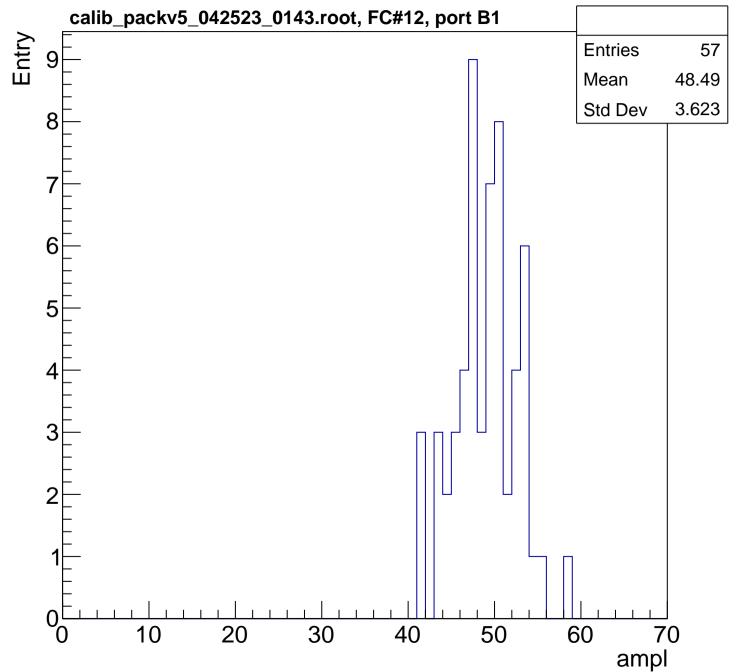


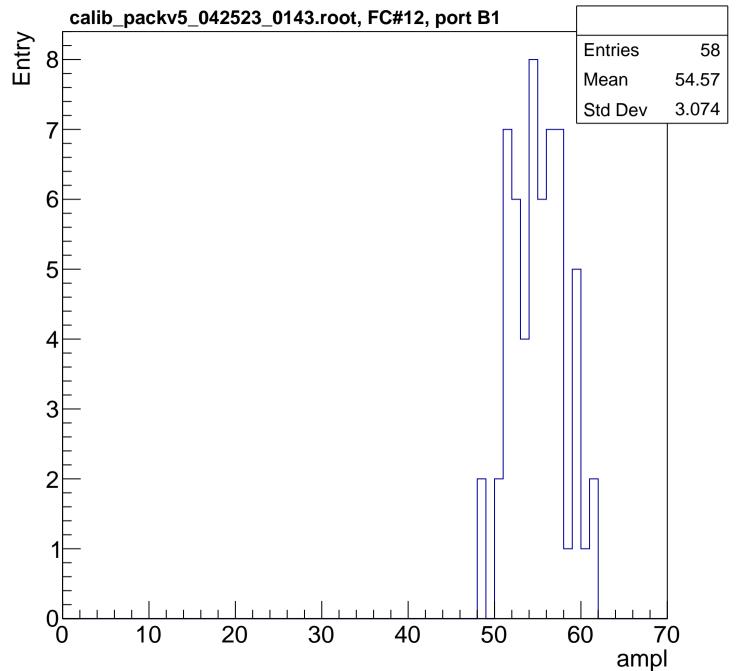


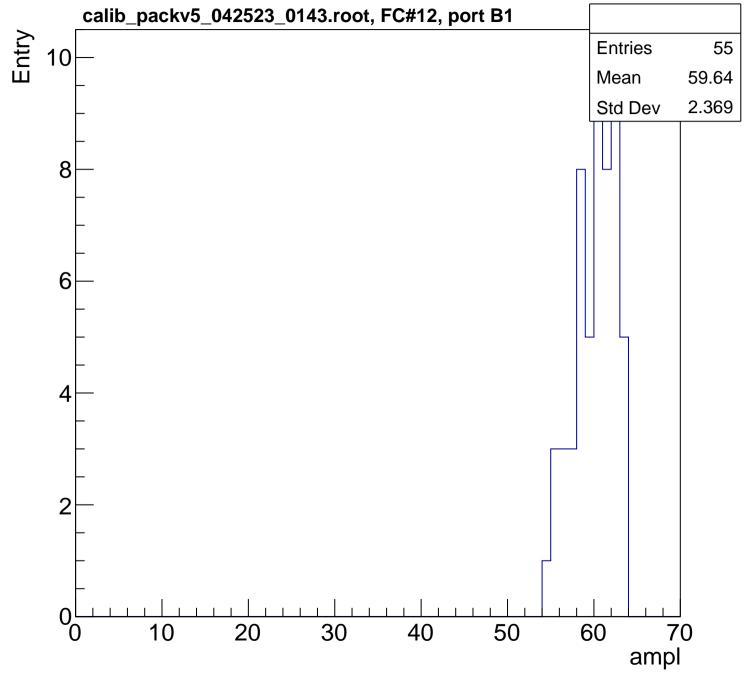


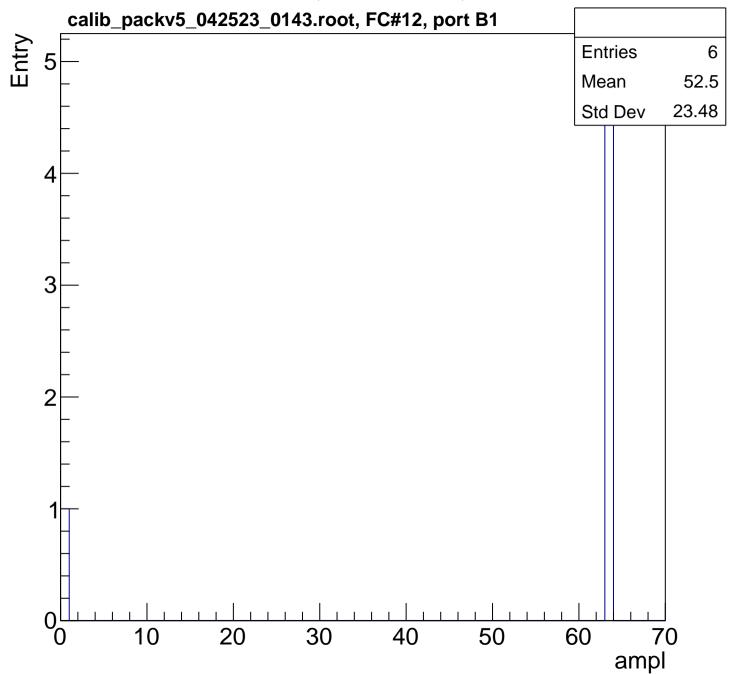




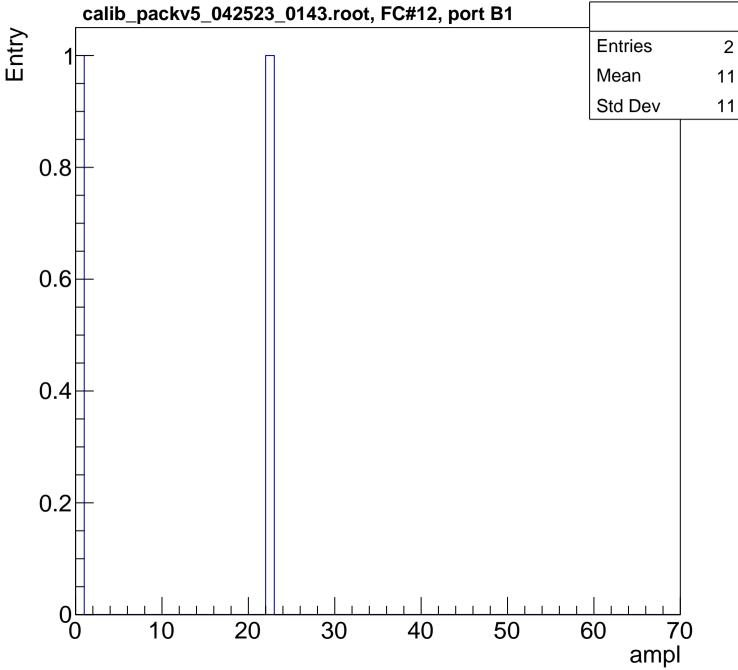


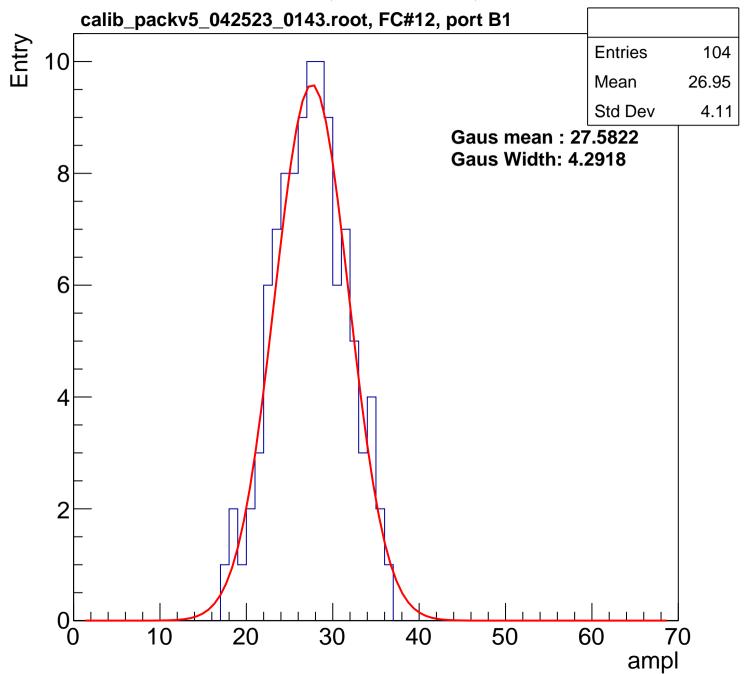


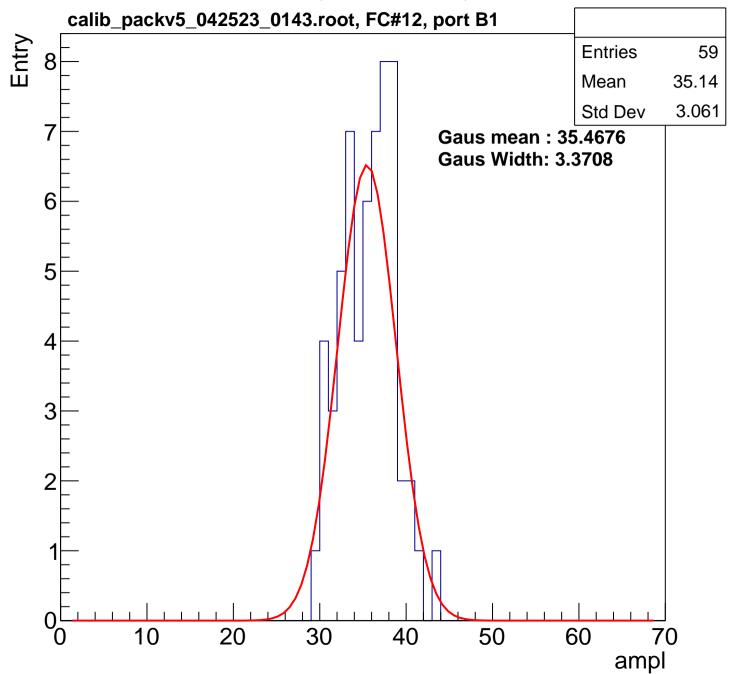


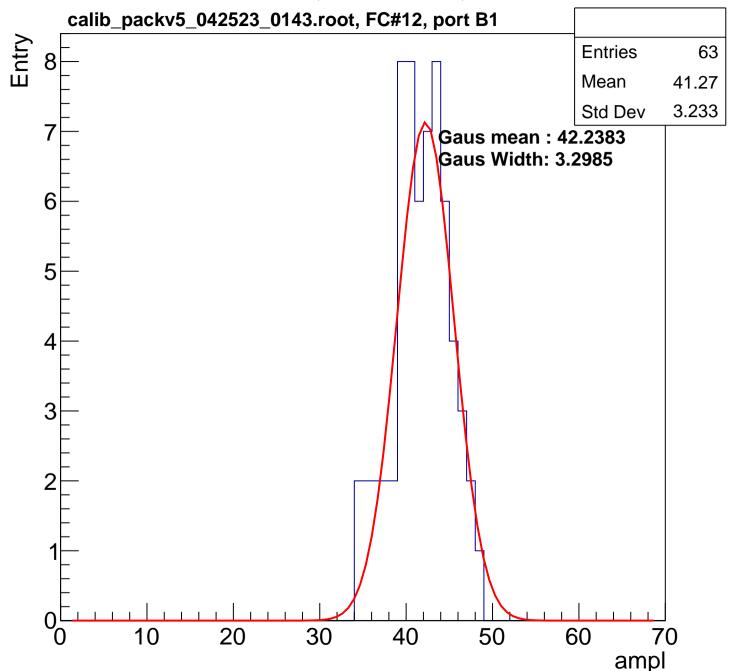


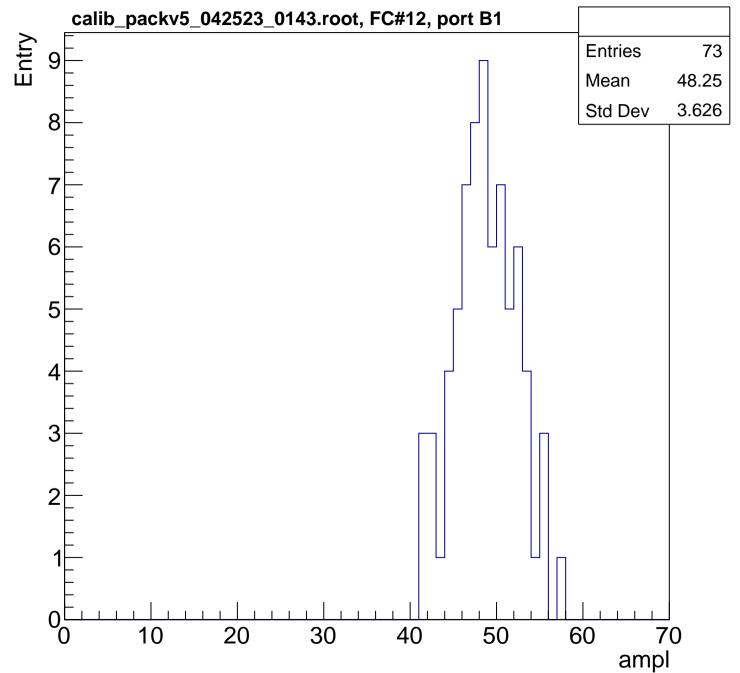
2

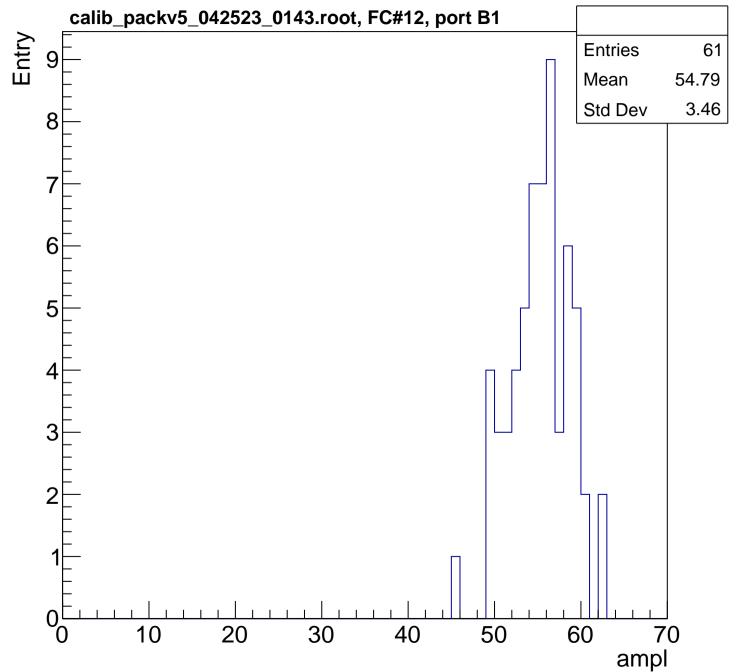


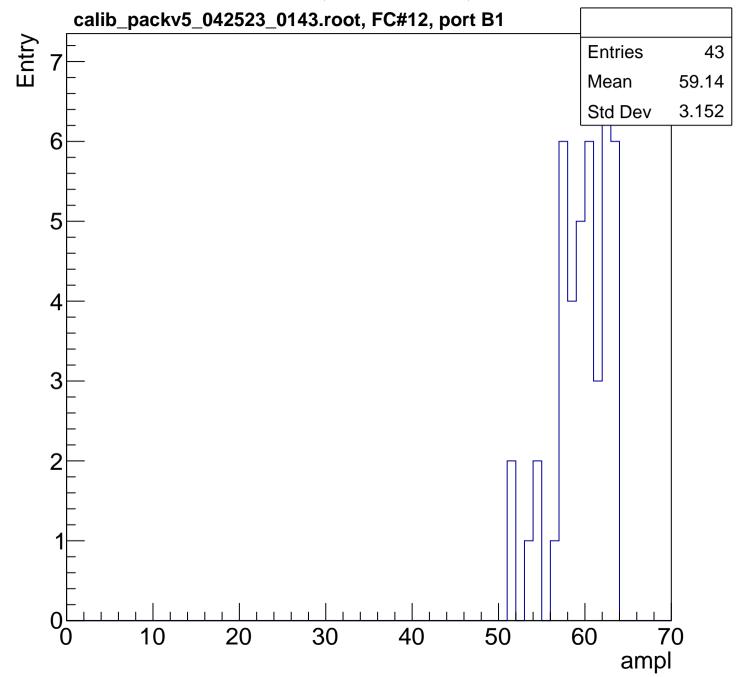


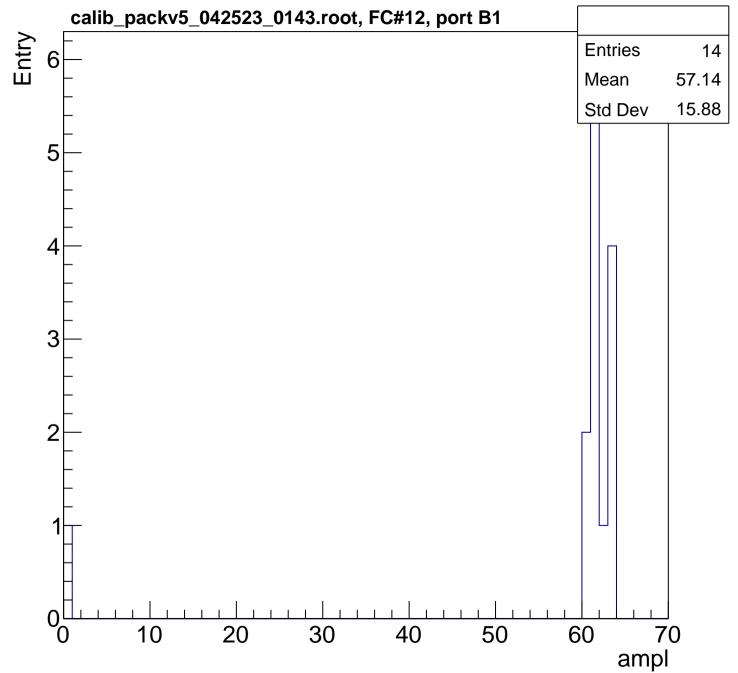


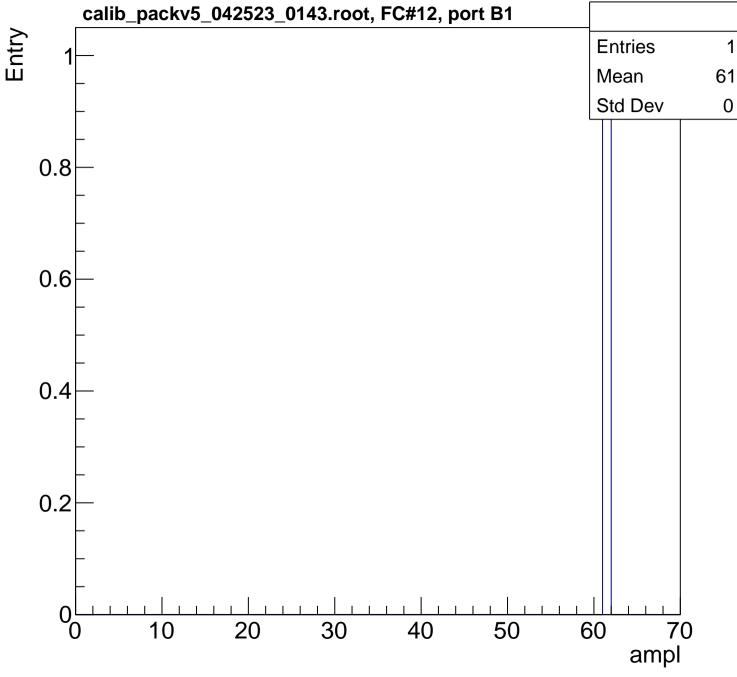


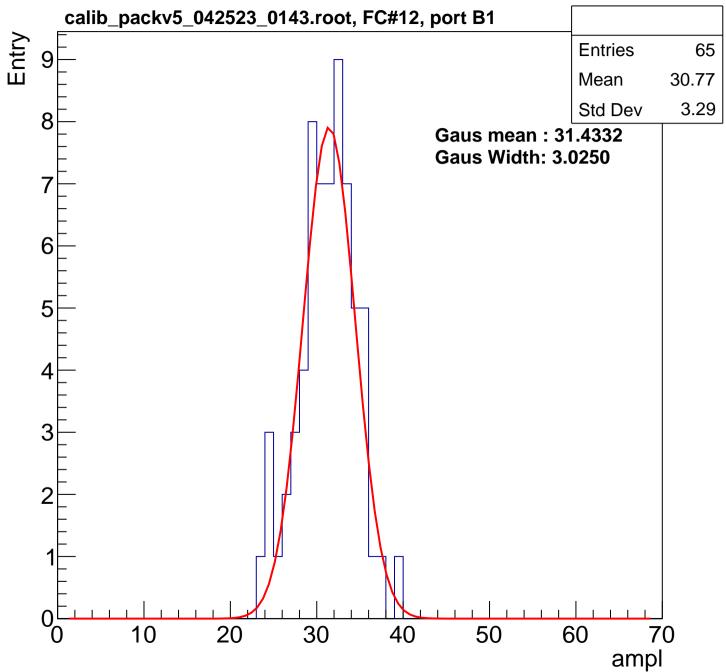


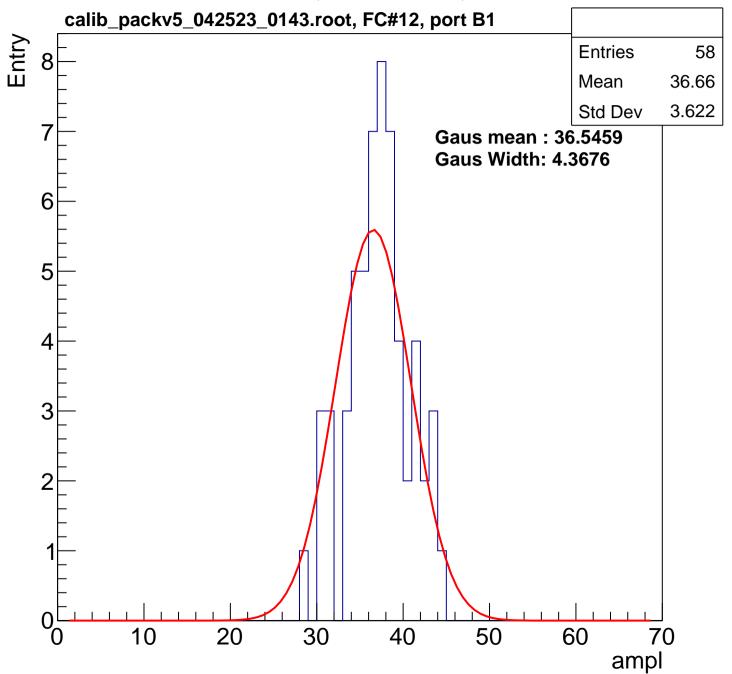


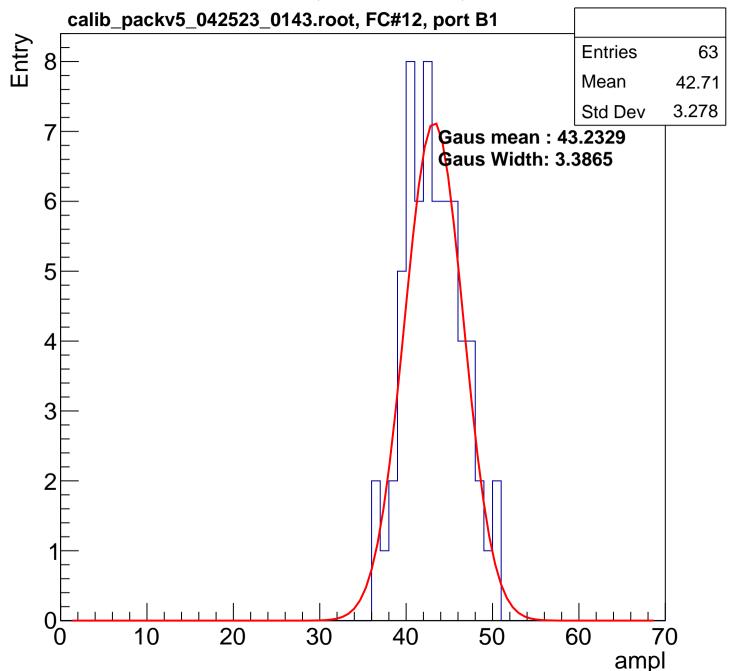


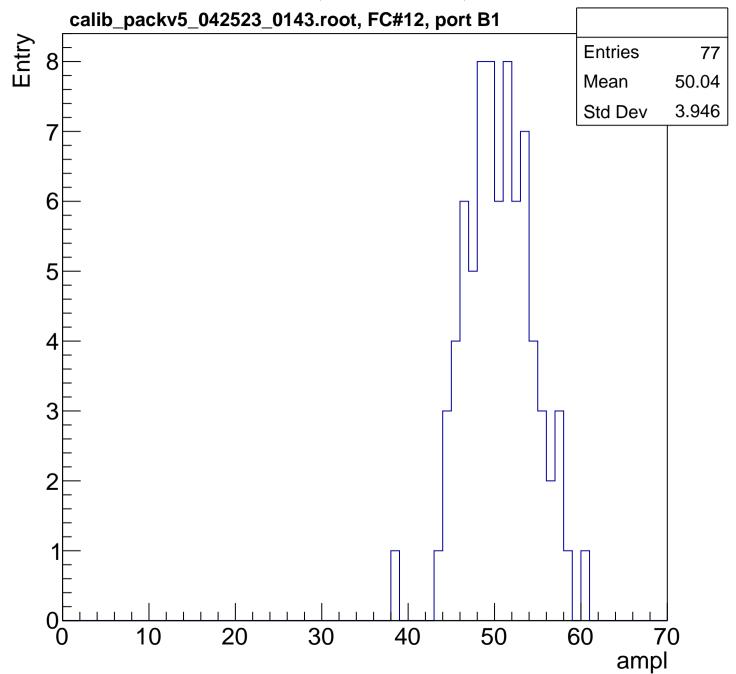


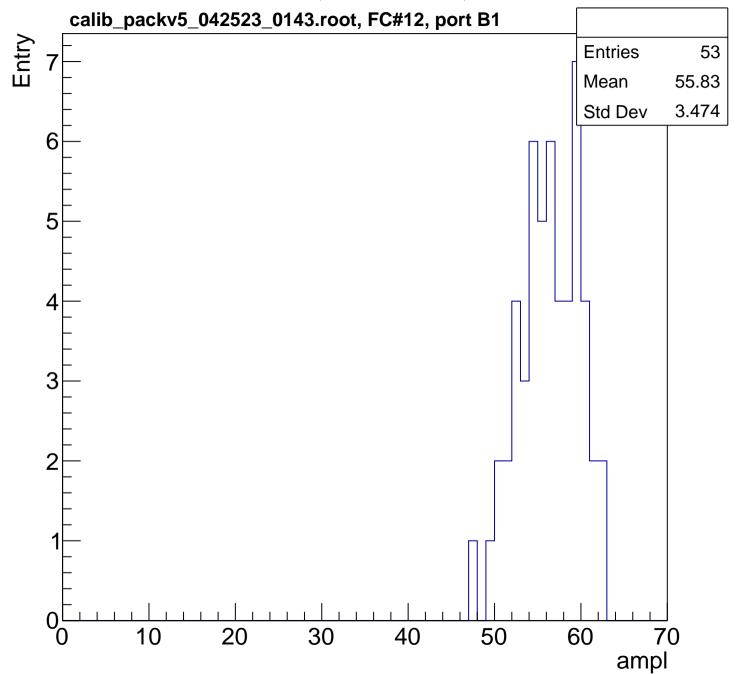


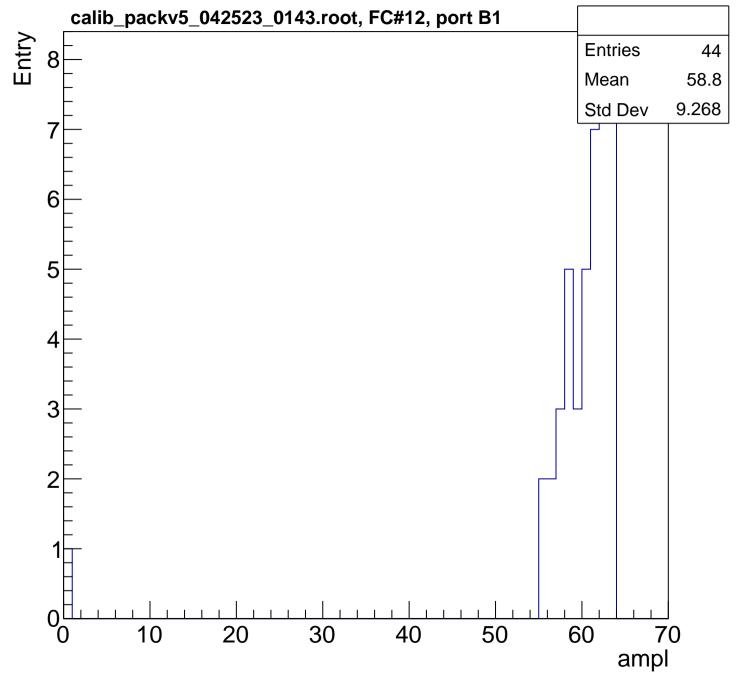


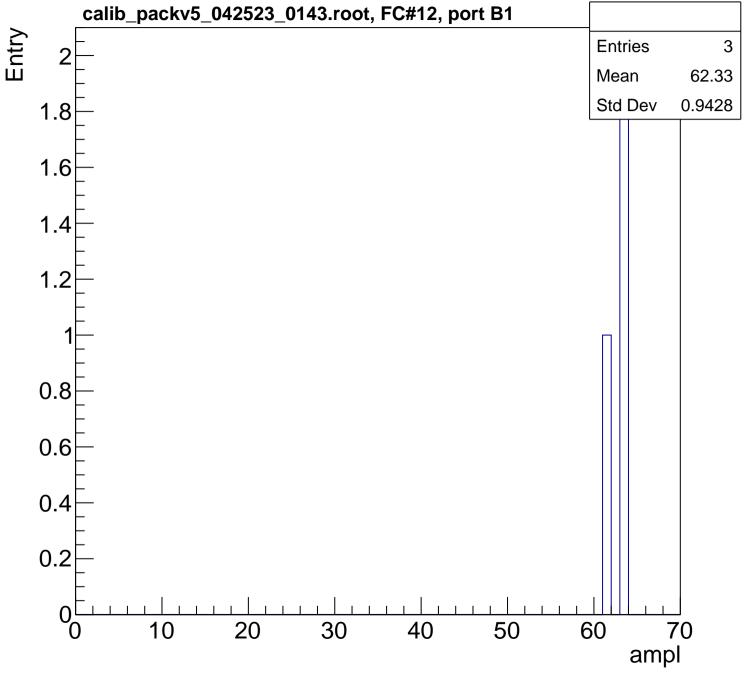












B0L102S, U3-ch15, adc7 calib_packv5_042523_0143.root, FC#12, port B1 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2

30

40

50

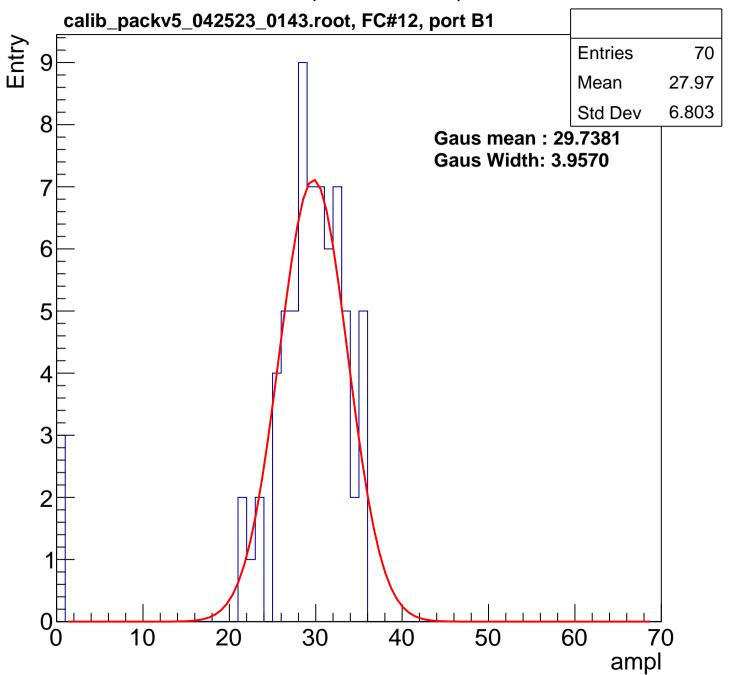
60

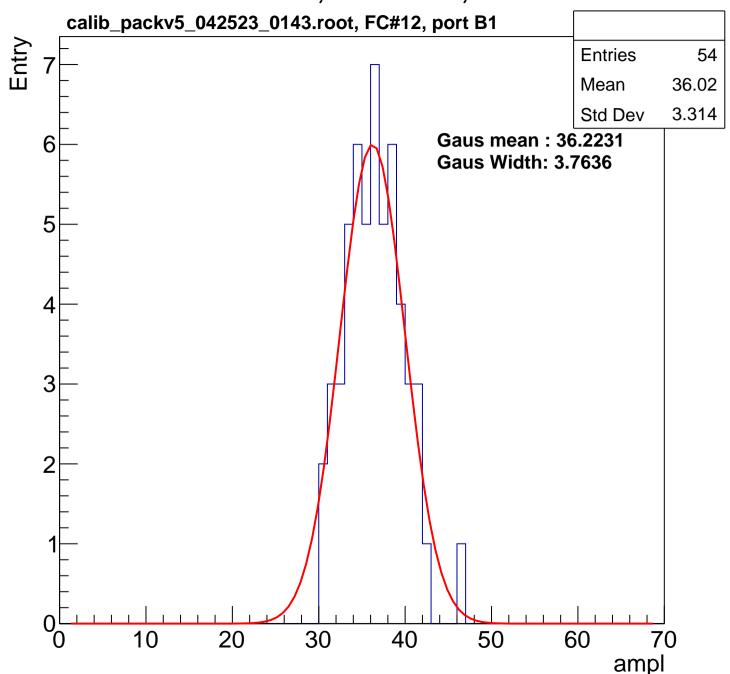
70

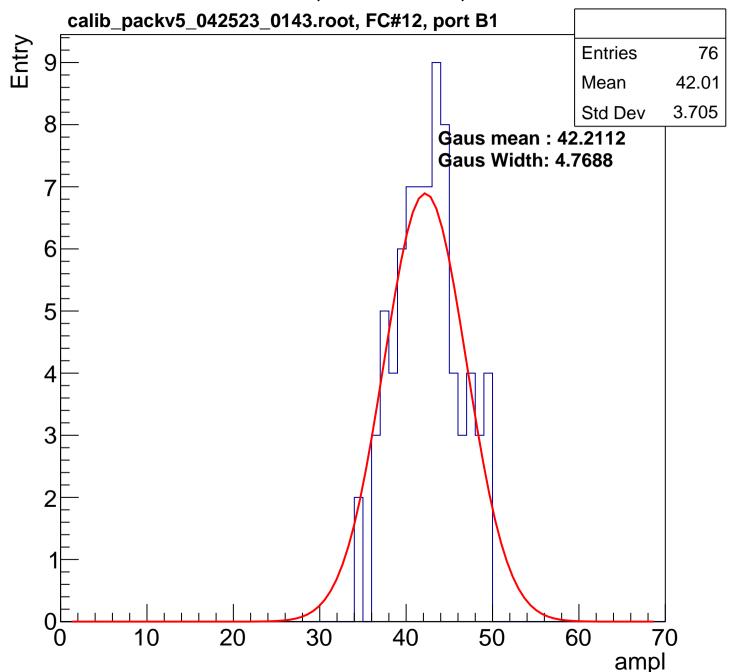
ampl

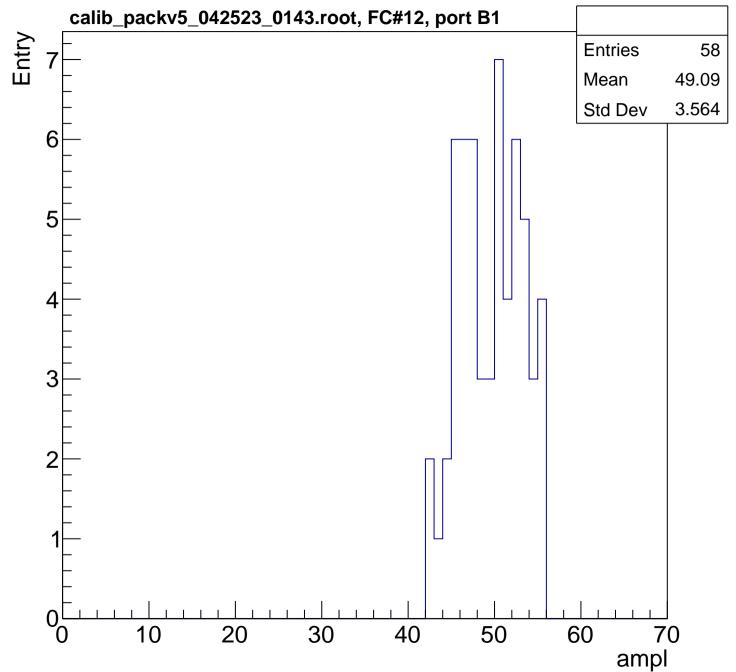
10

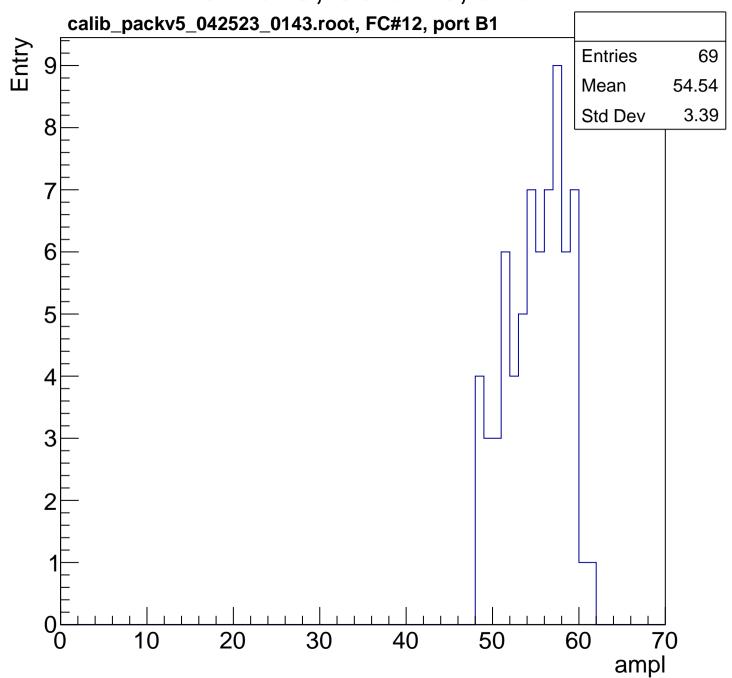
20

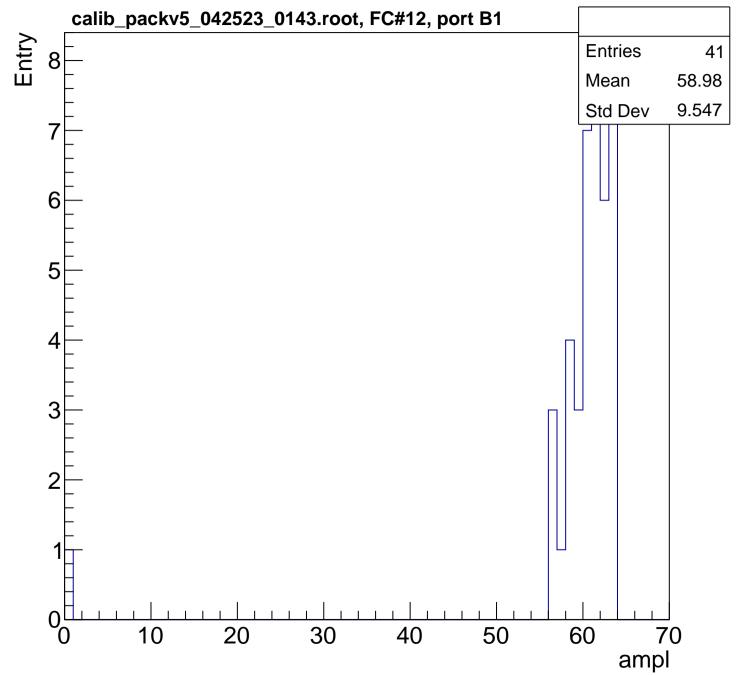


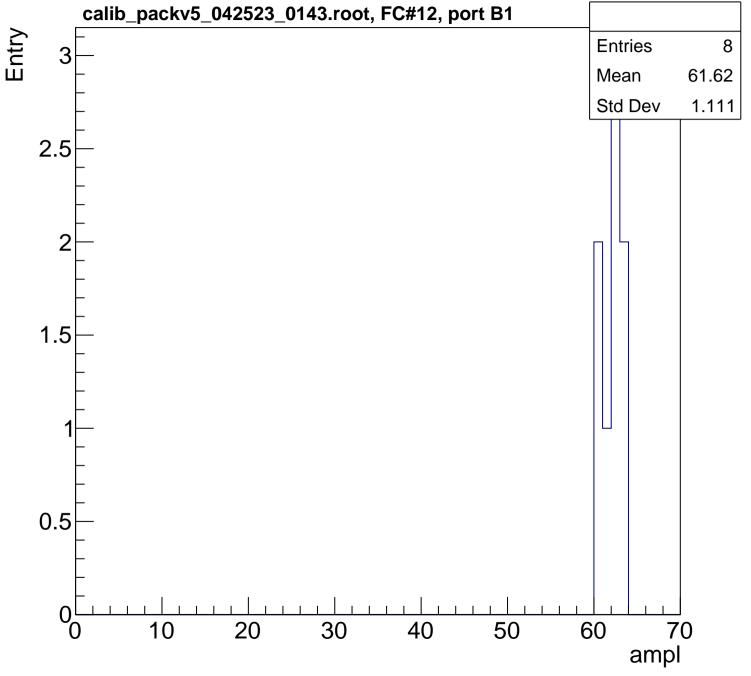


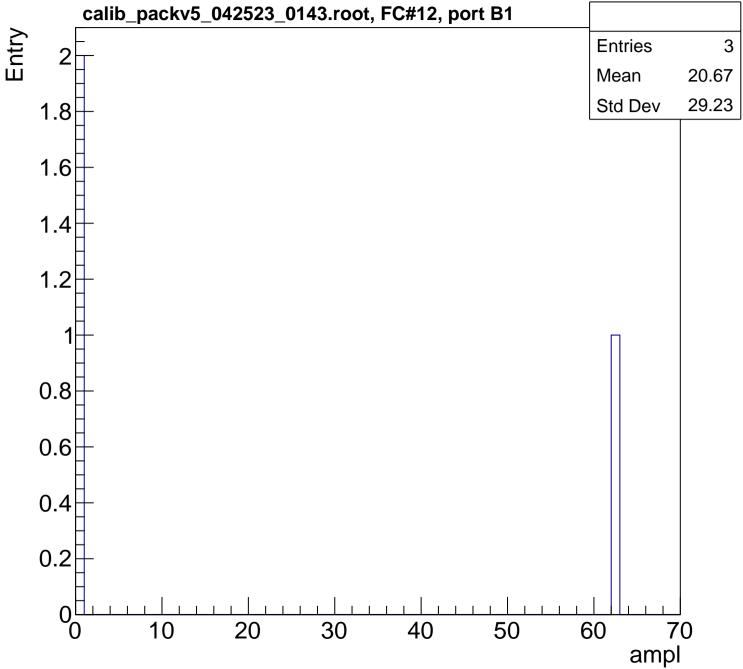


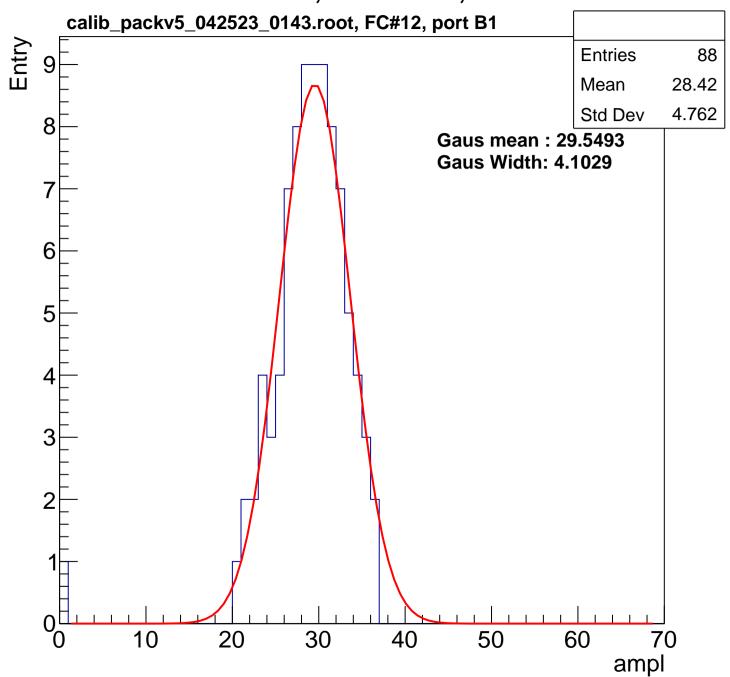


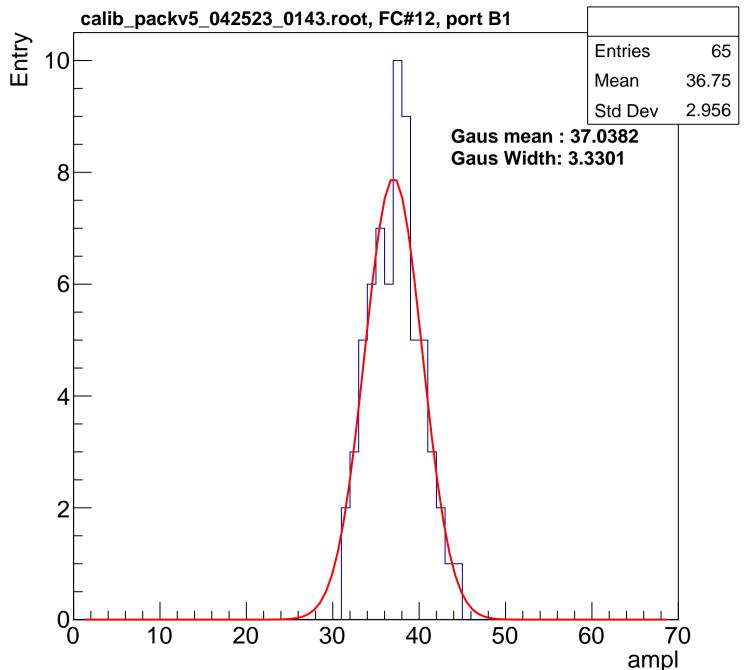


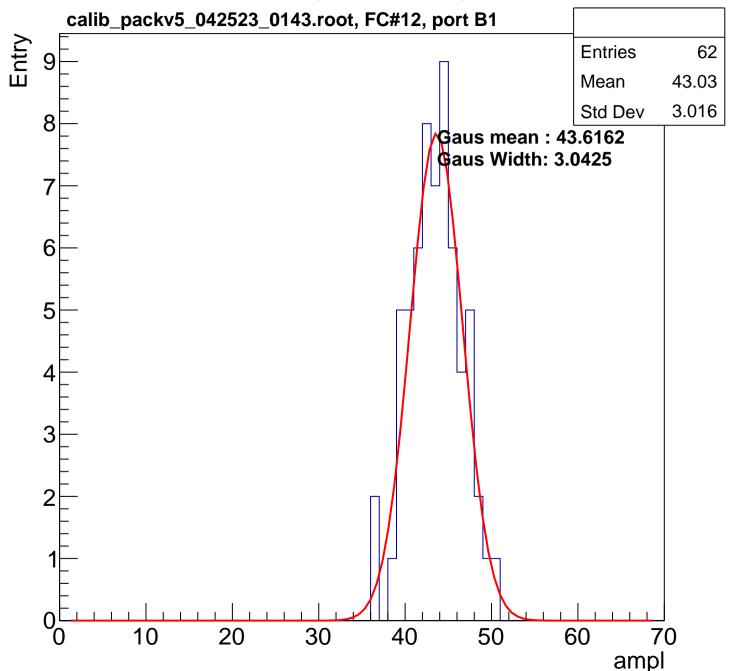


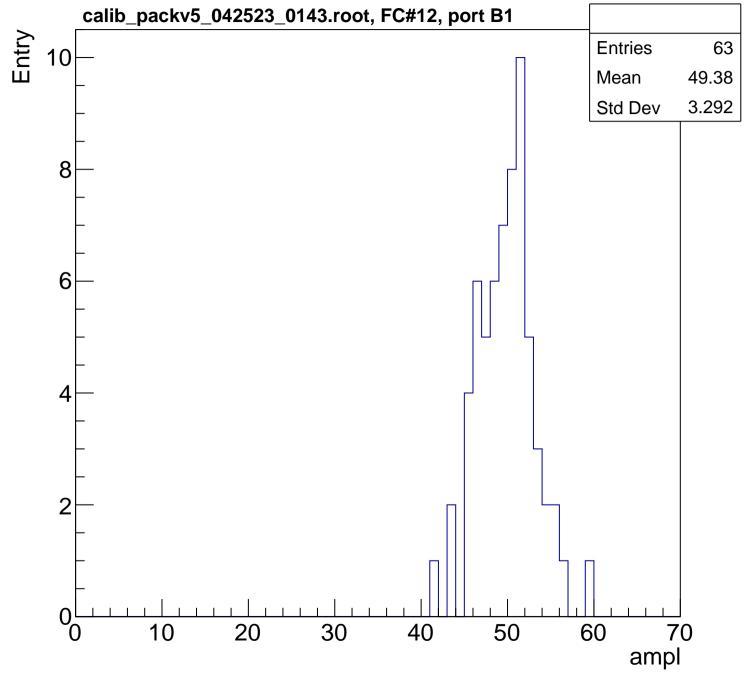


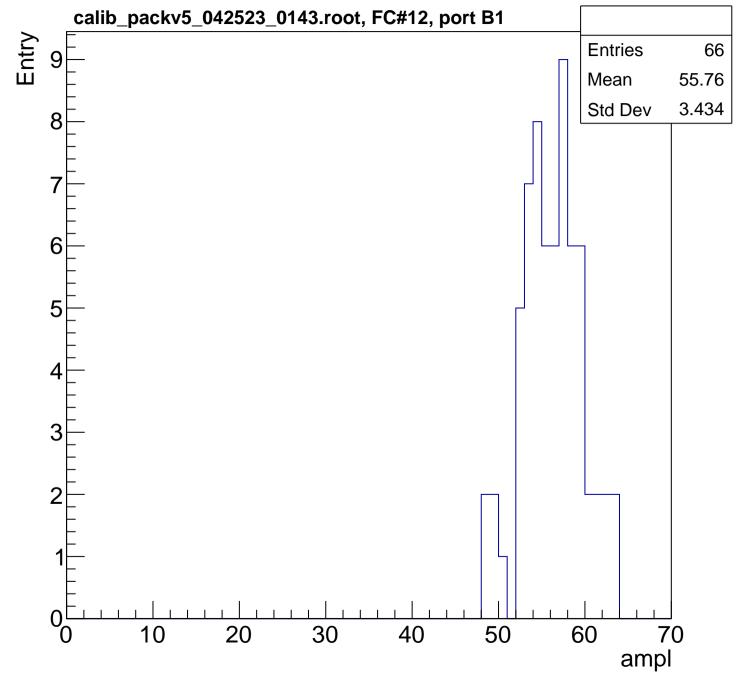


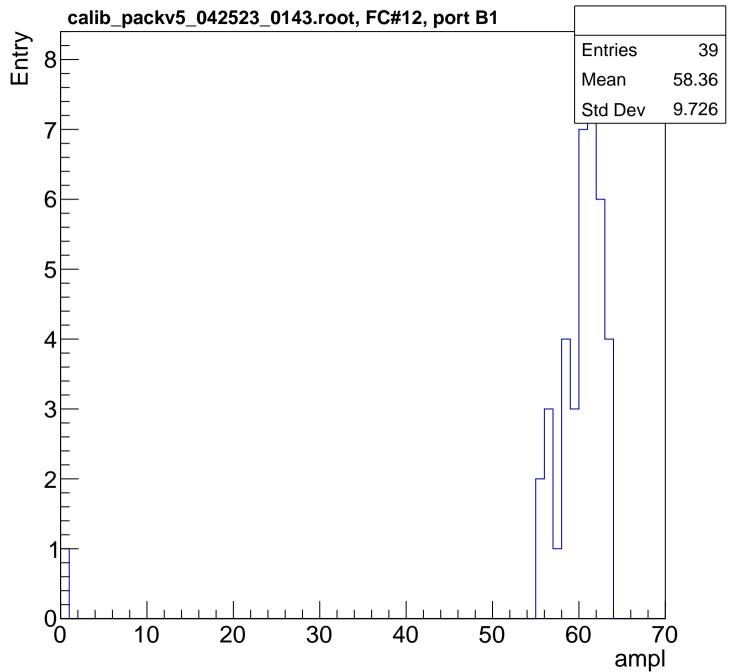


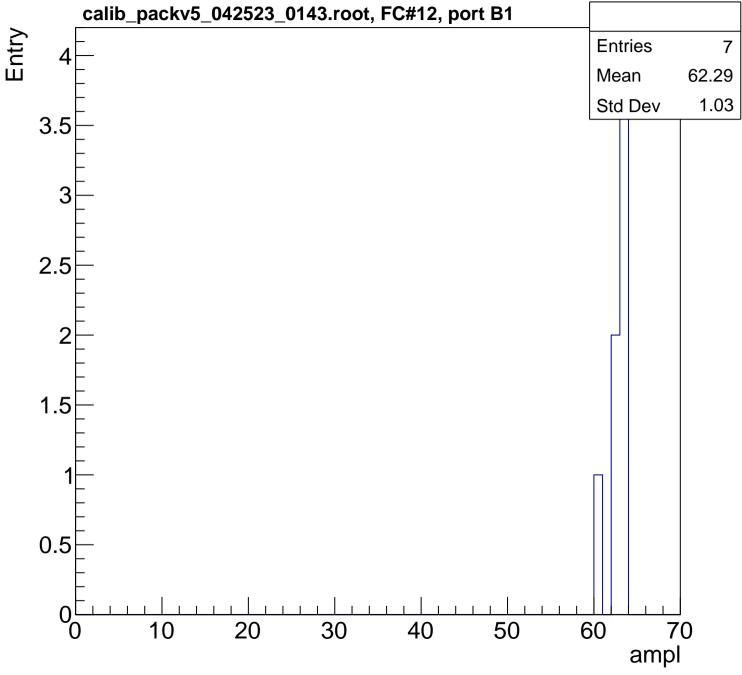




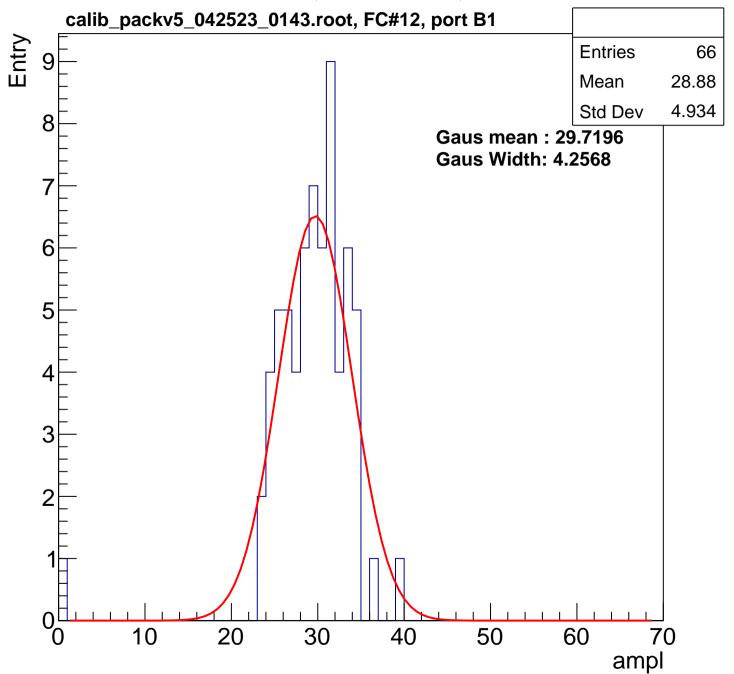


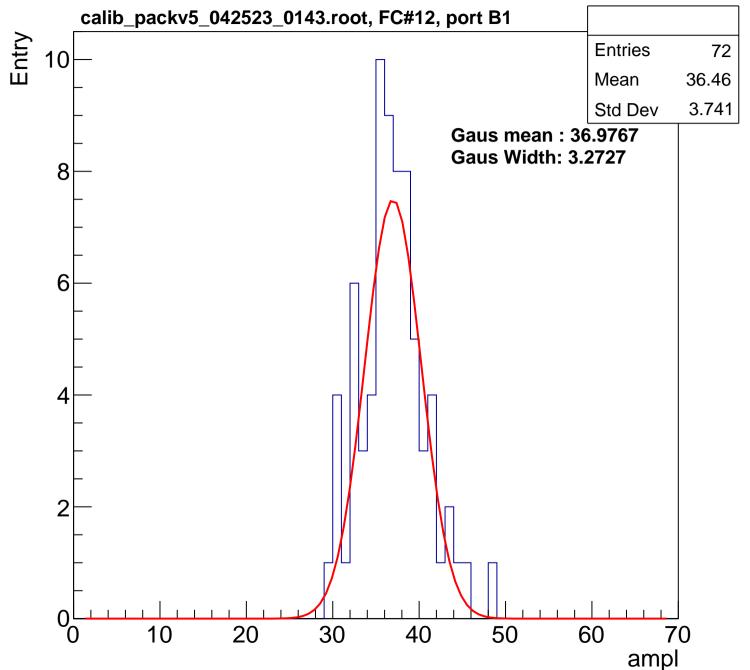


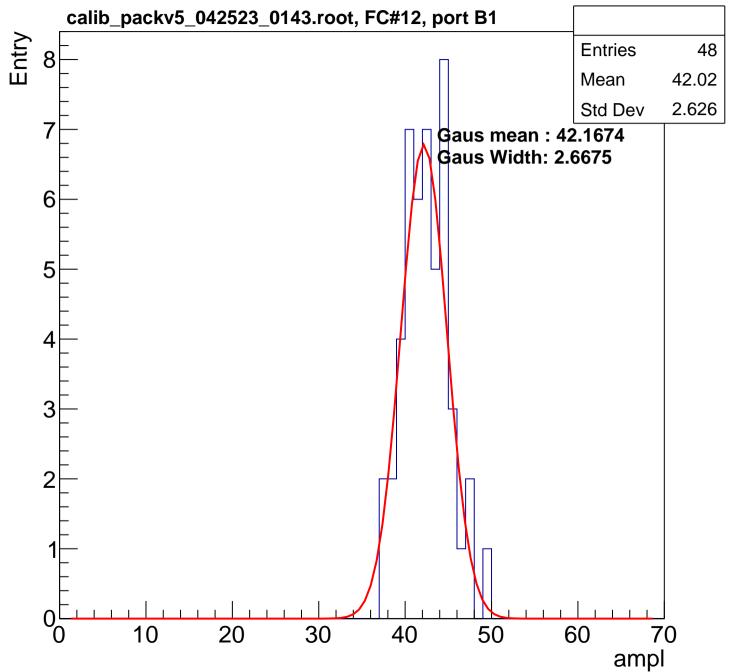


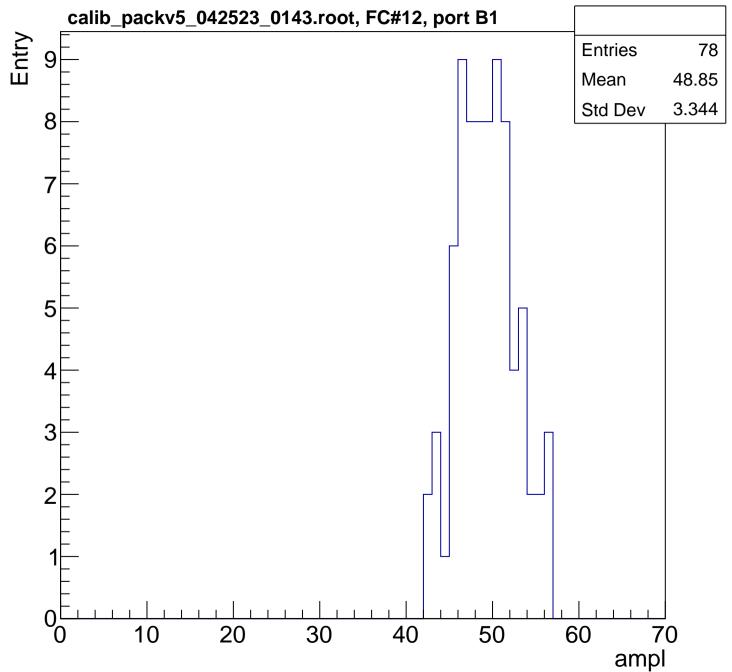


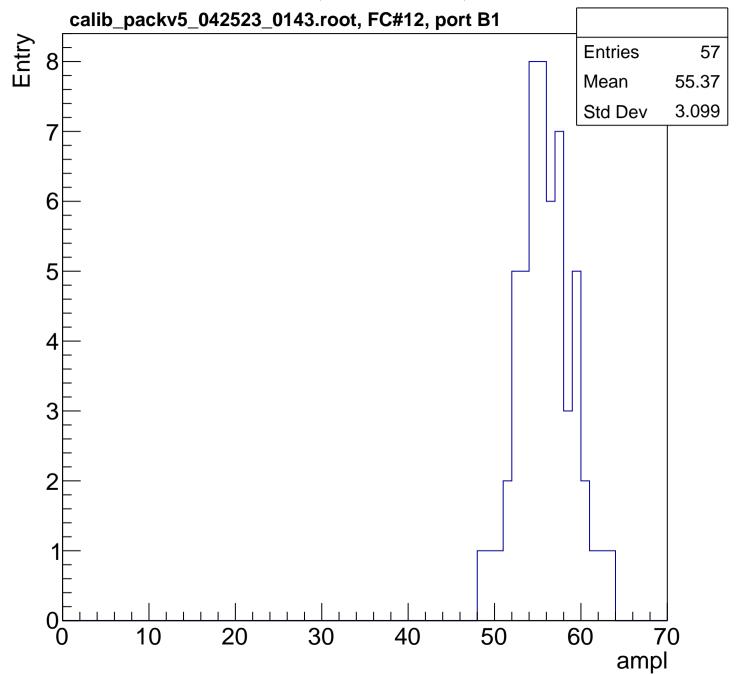
B0L102S, U3-ch17, adc7 calib_packv5_042523_0143.root, FC#12, port B1 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

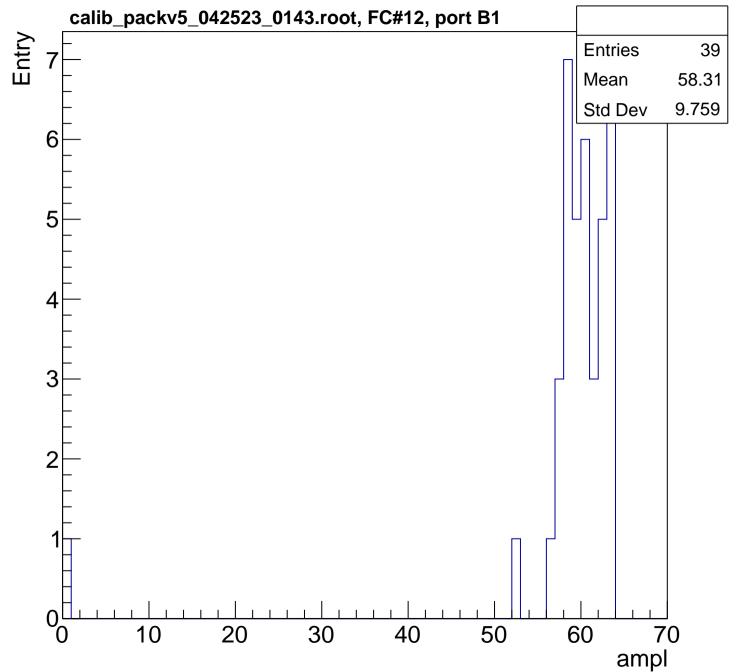


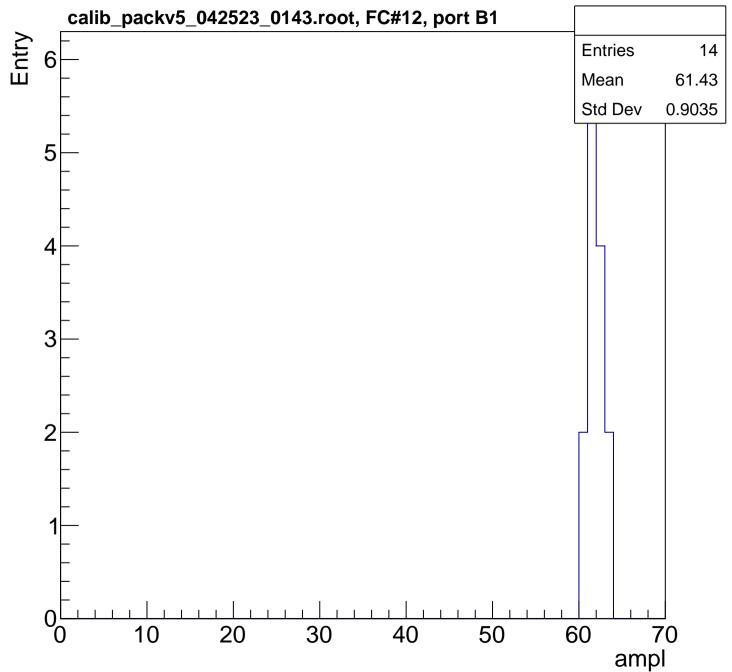




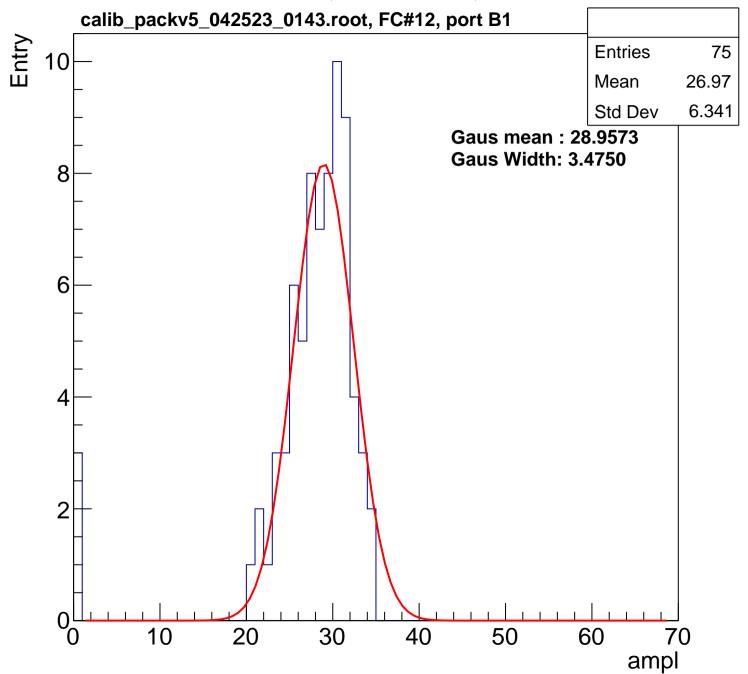


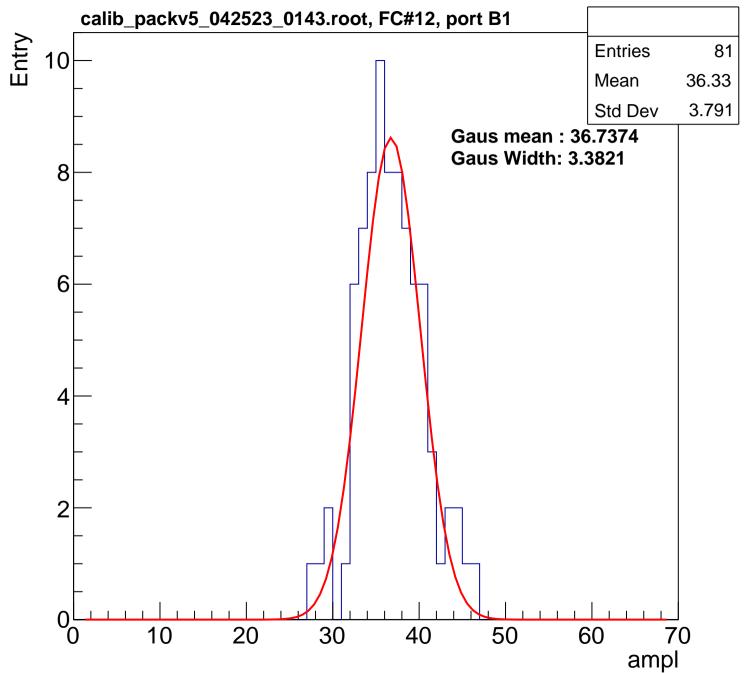


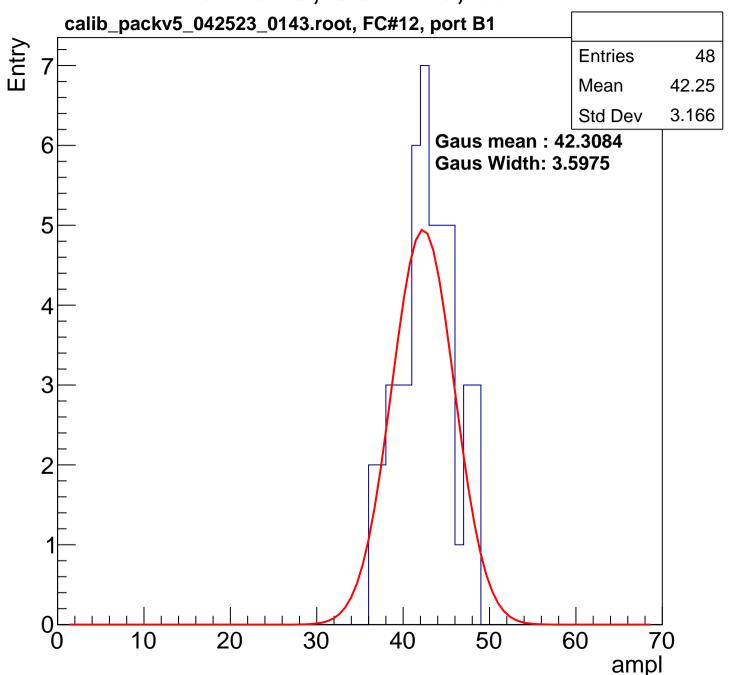


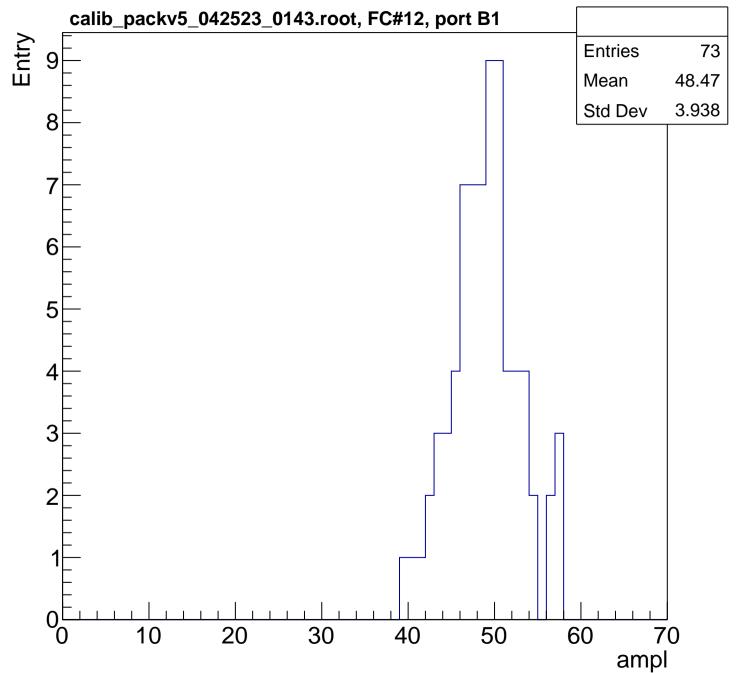


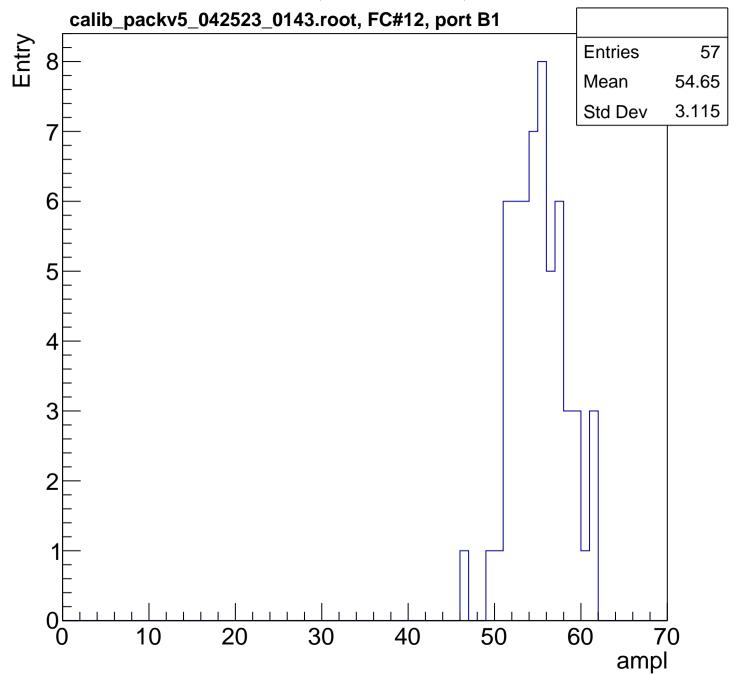
B0L102S, U3-ch18, adc7 calib_packv5_042523_0143.root, FC#12, port B1 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

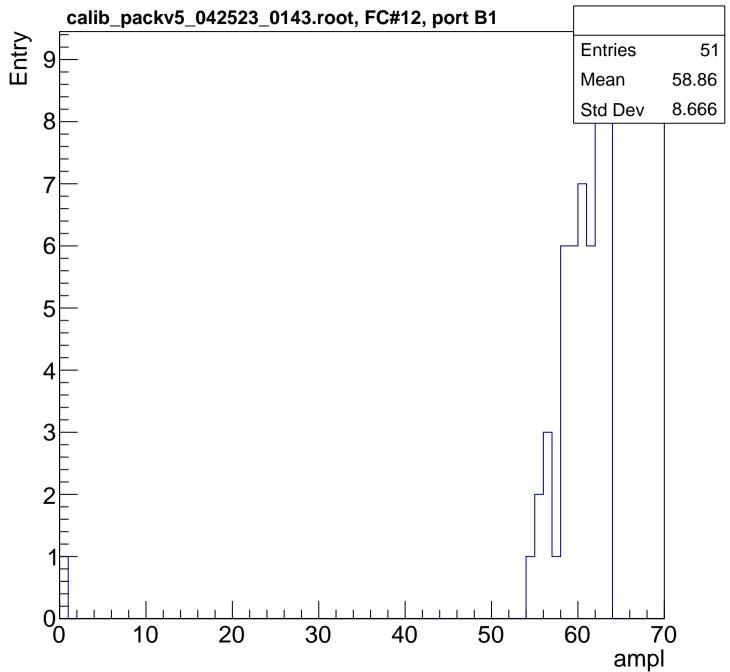


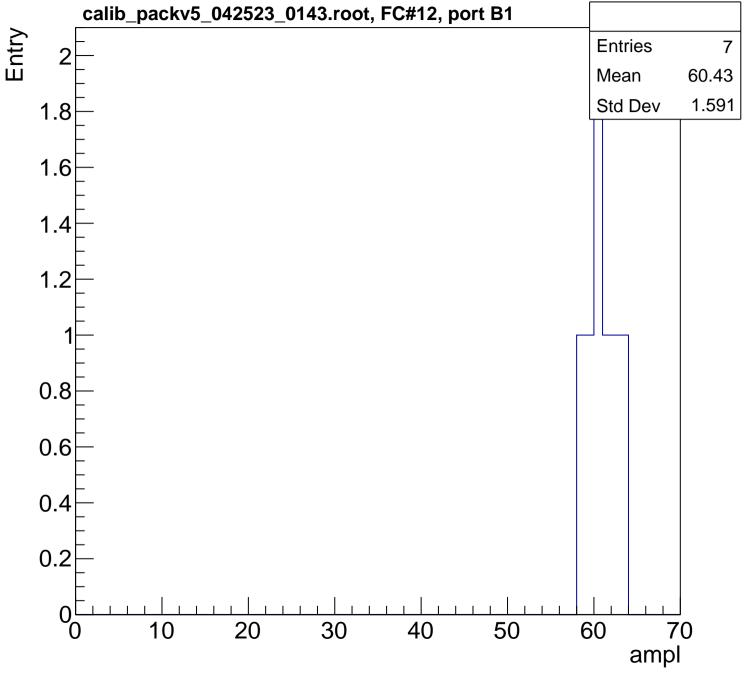


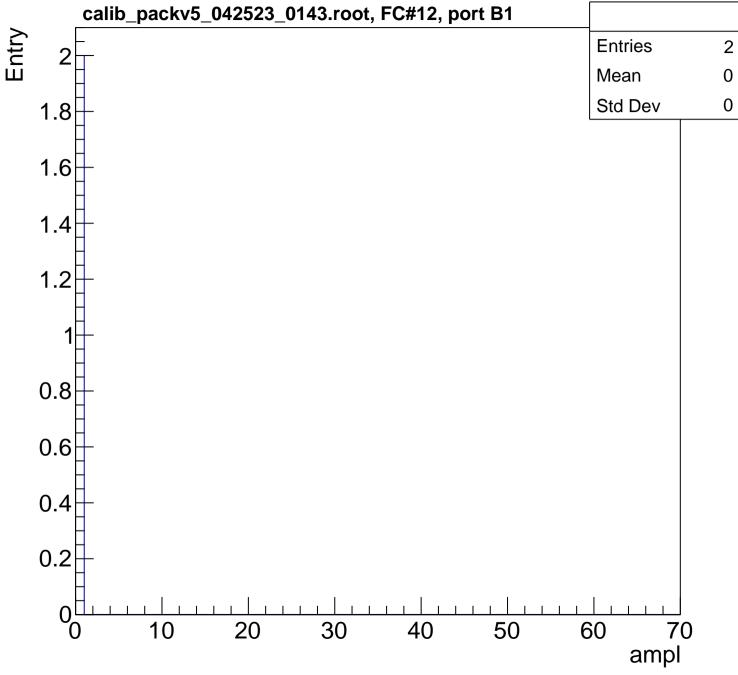


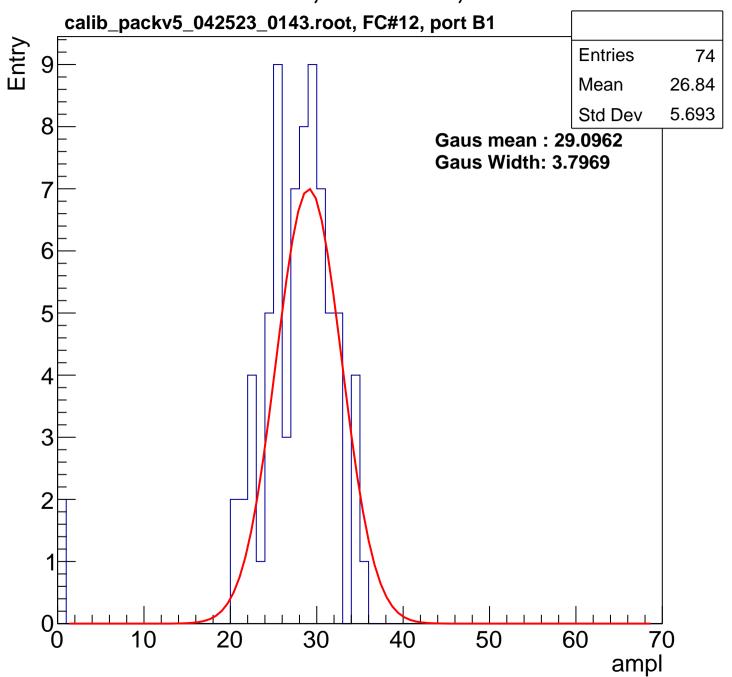


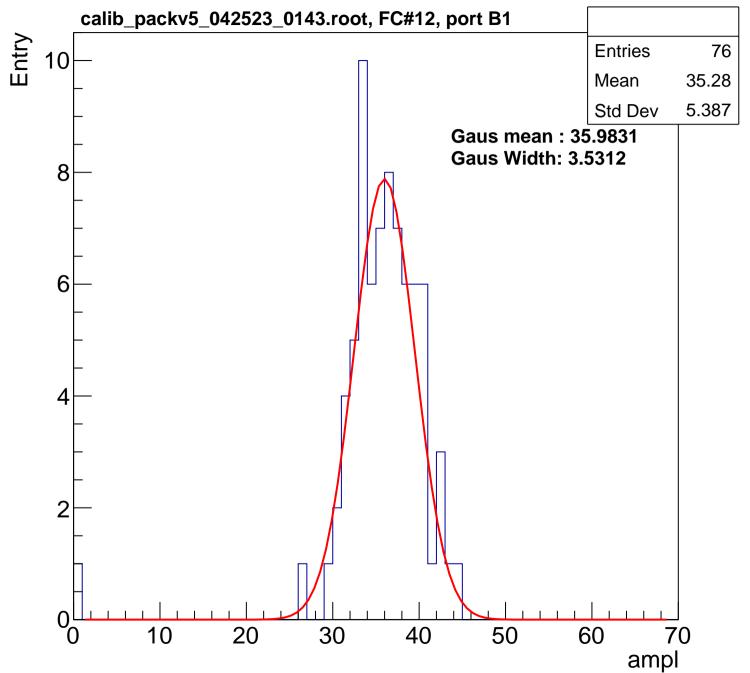


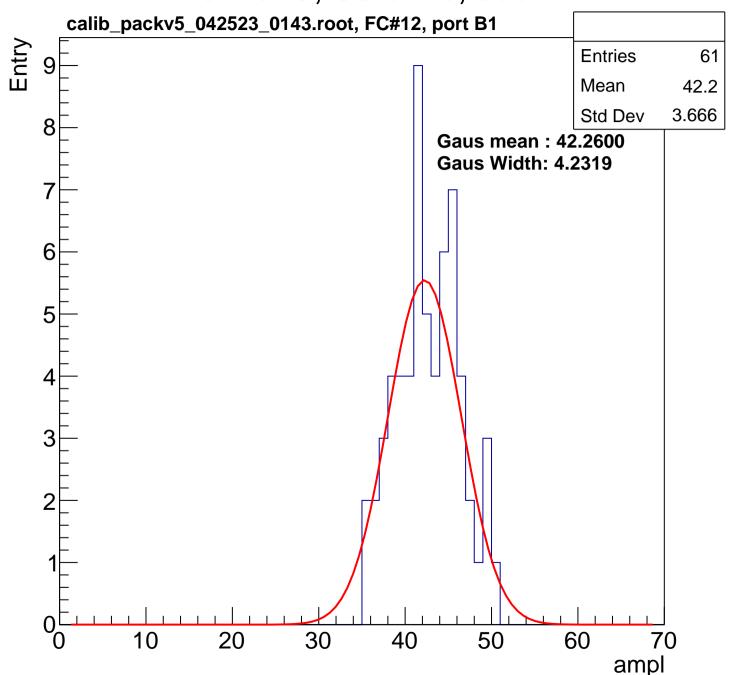


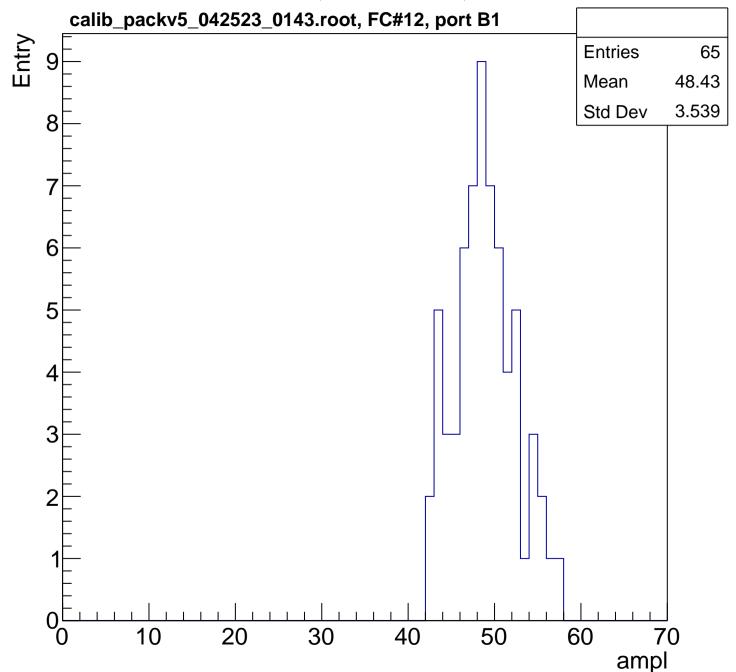


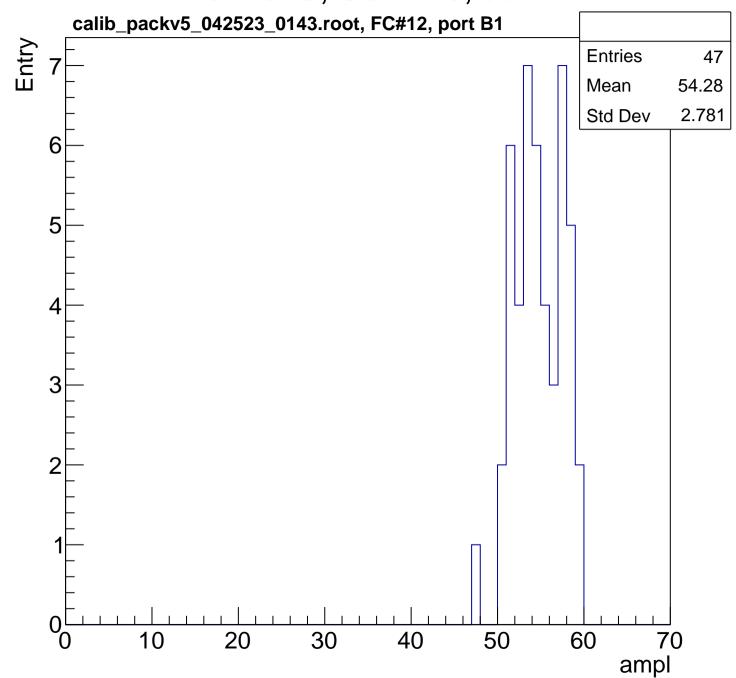


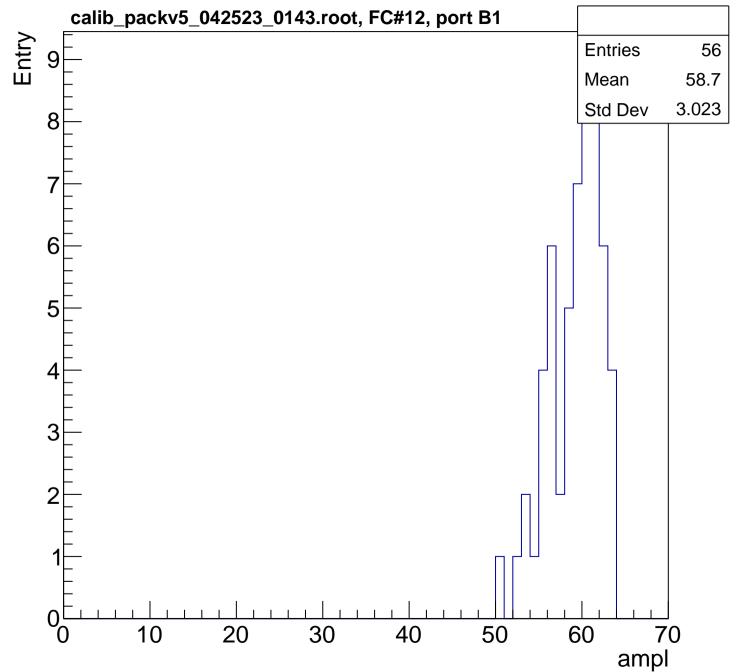


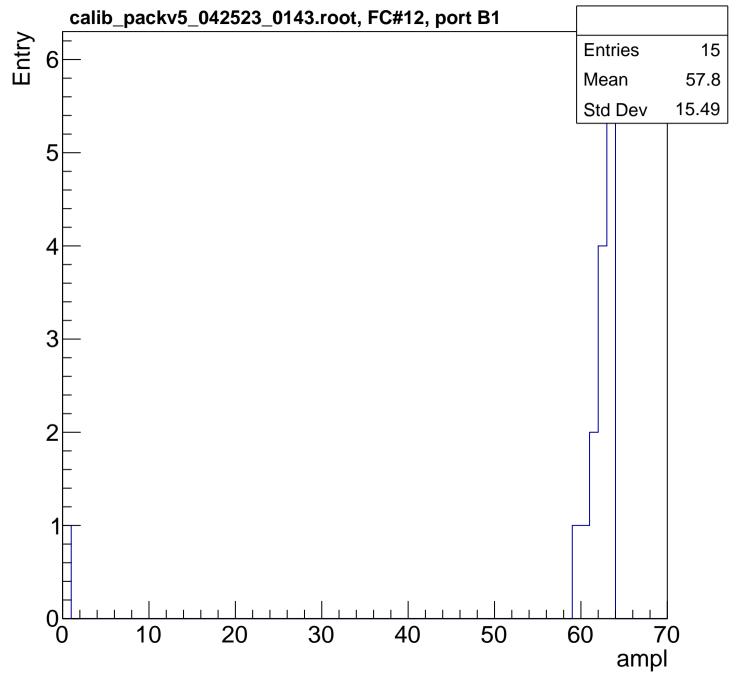




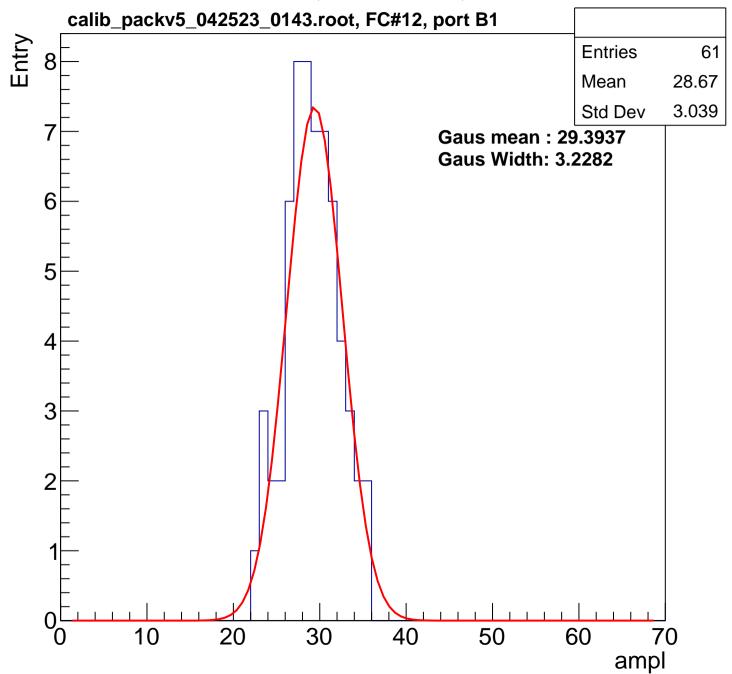


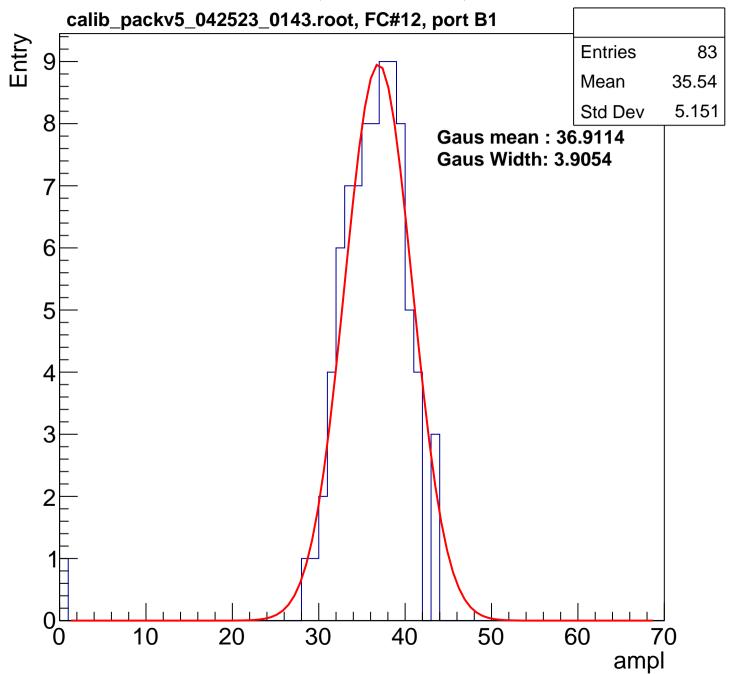


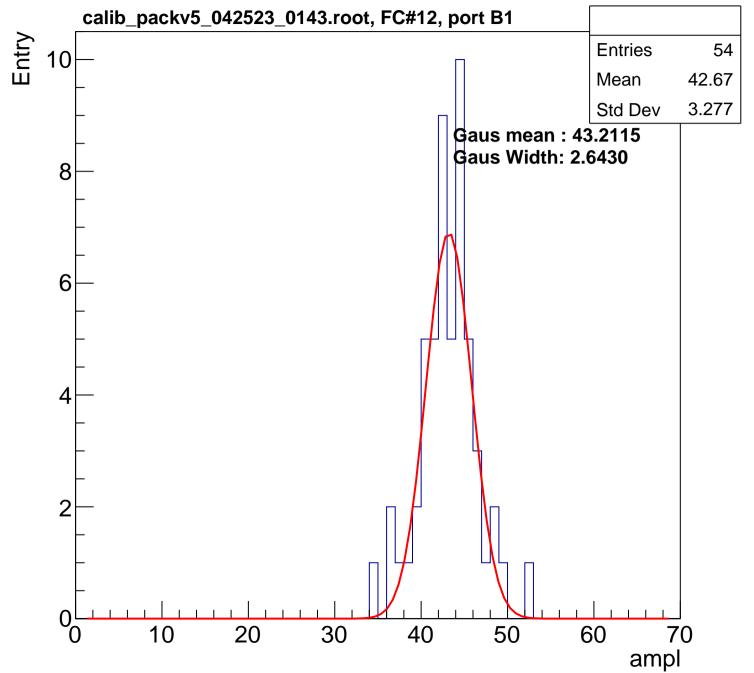


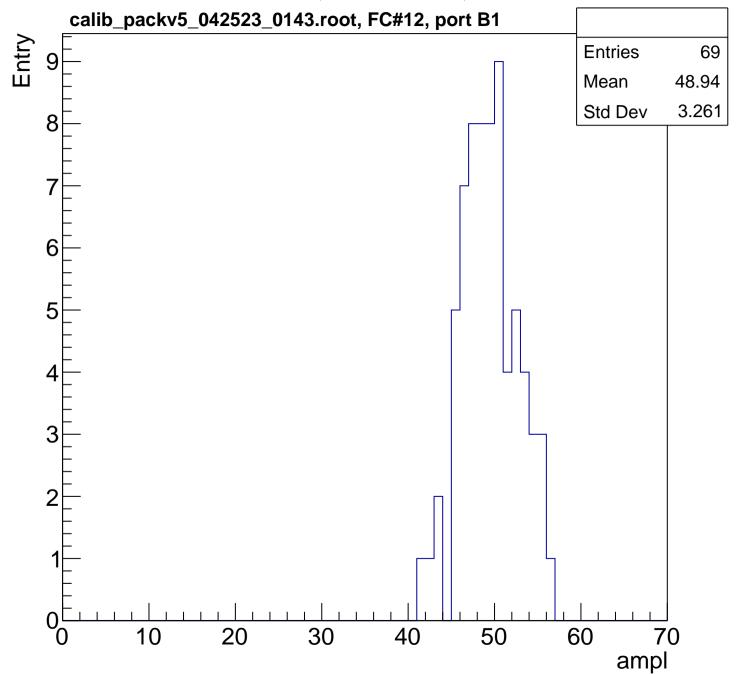


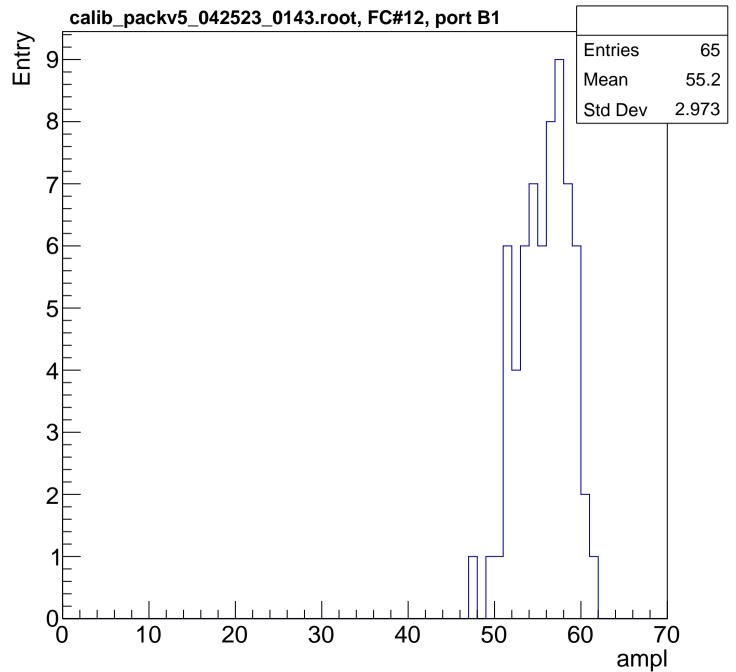


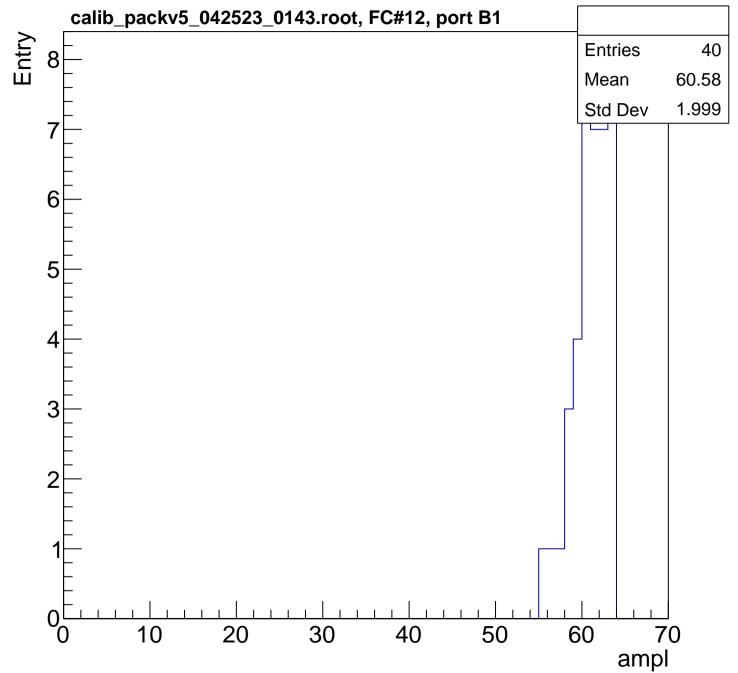


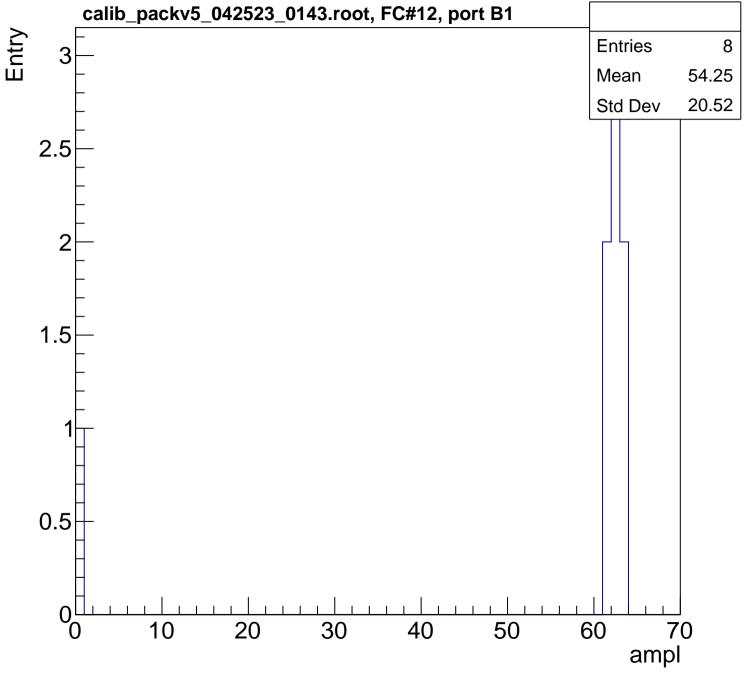


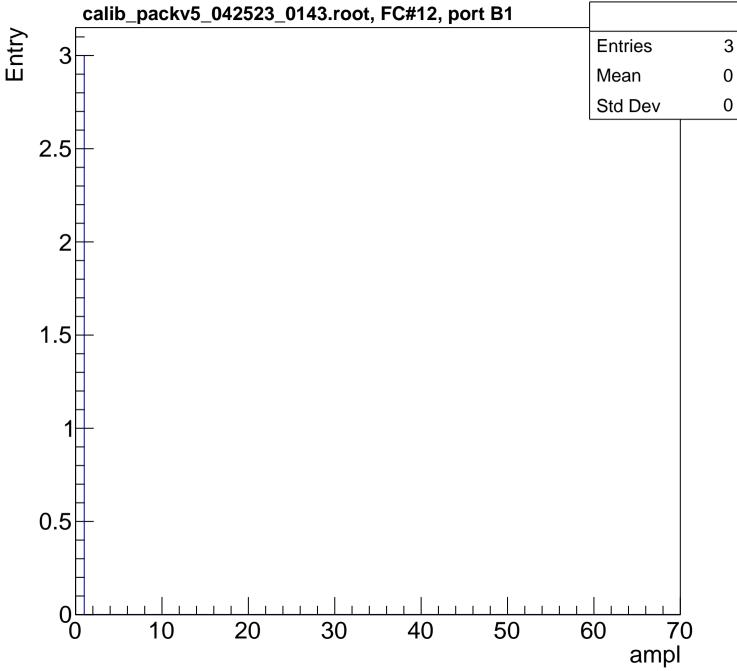


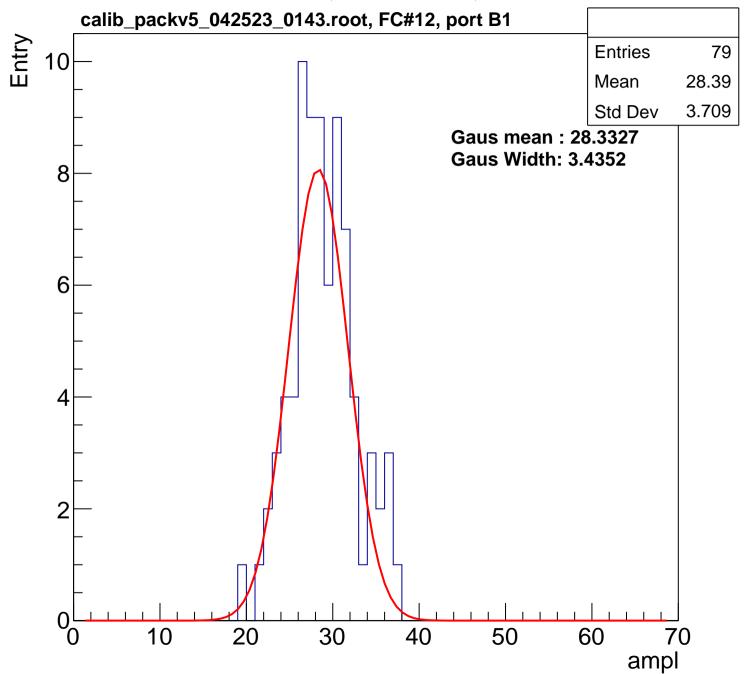


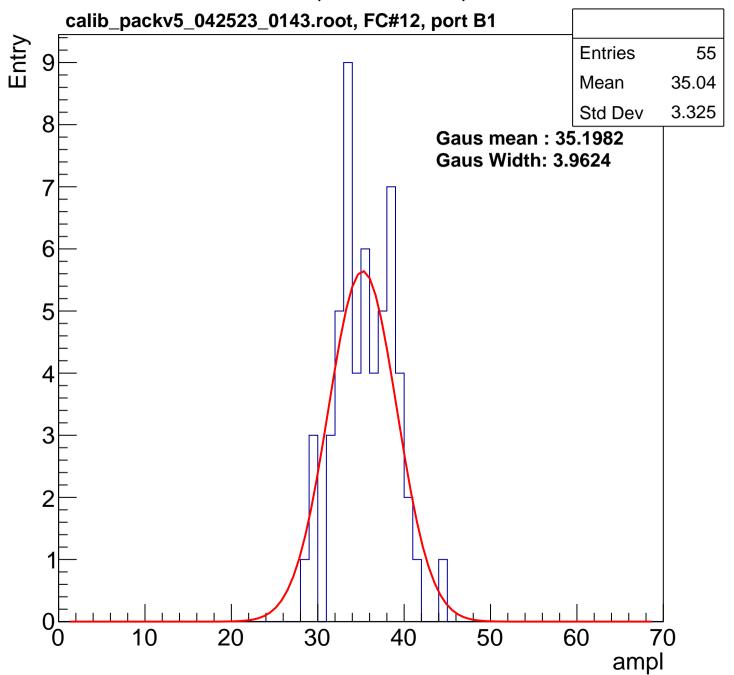


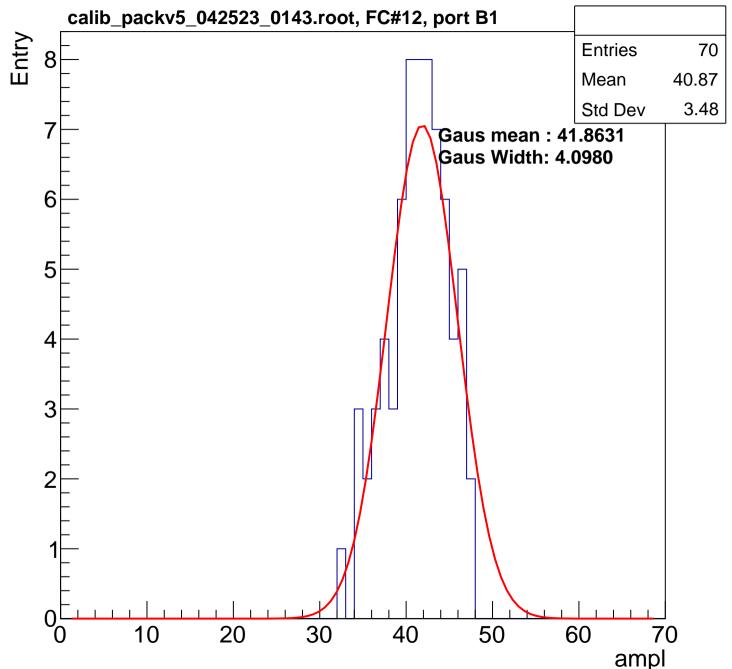


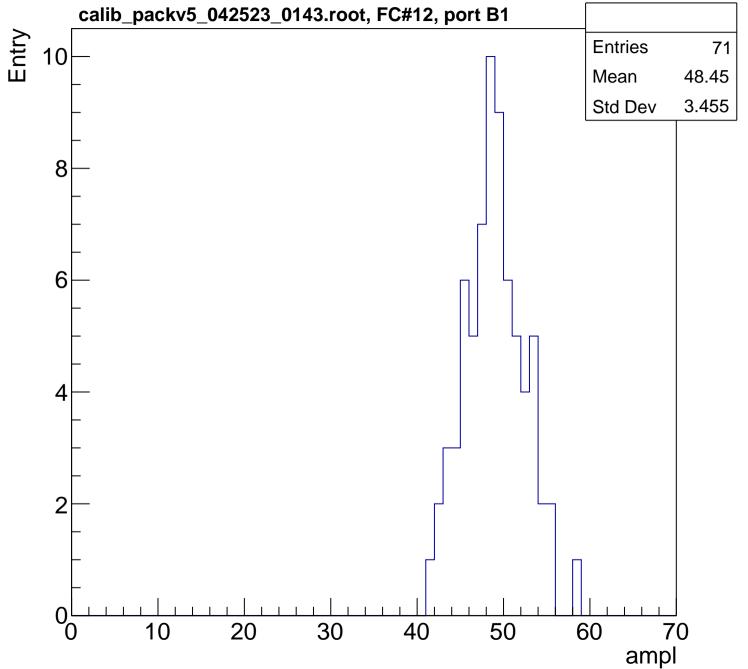


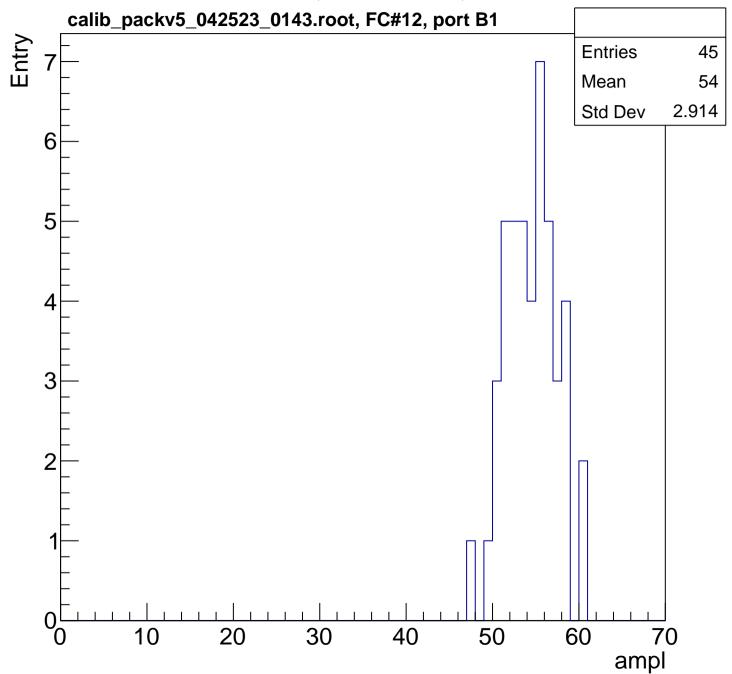


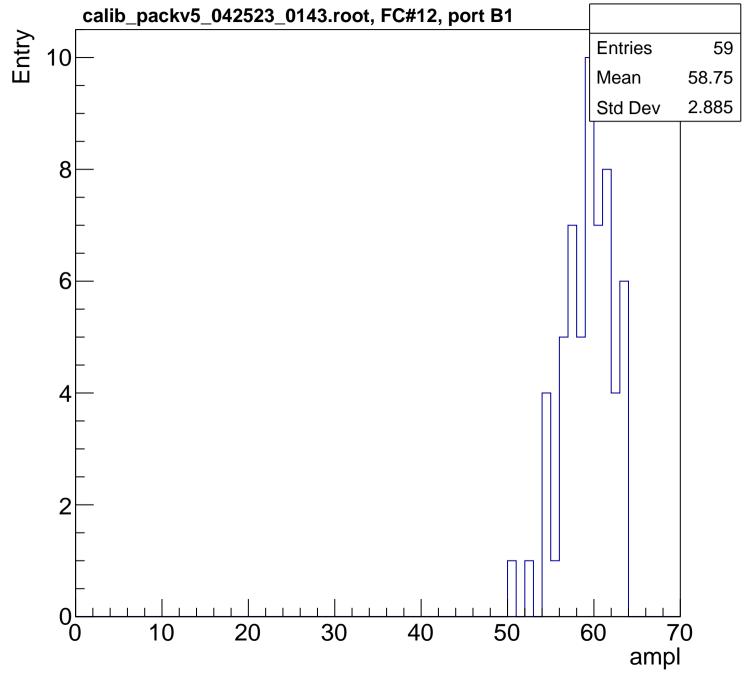


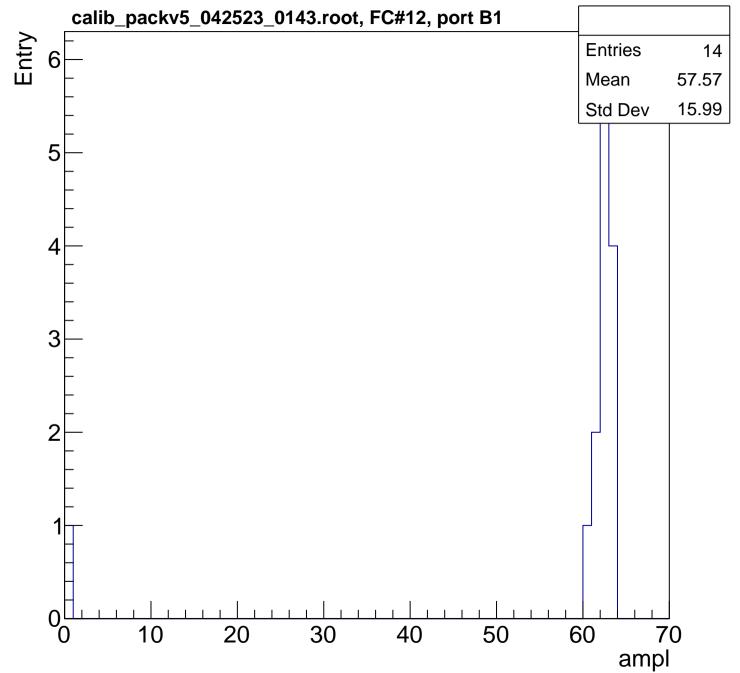


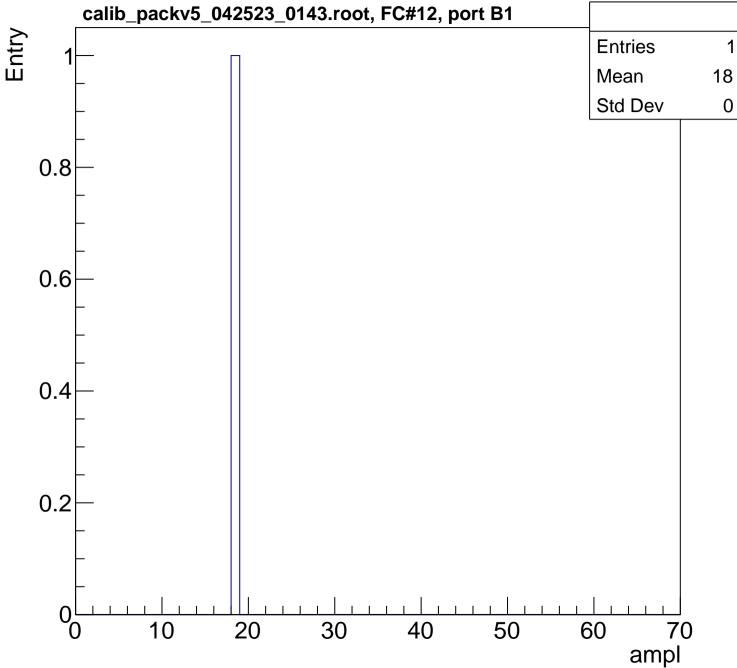


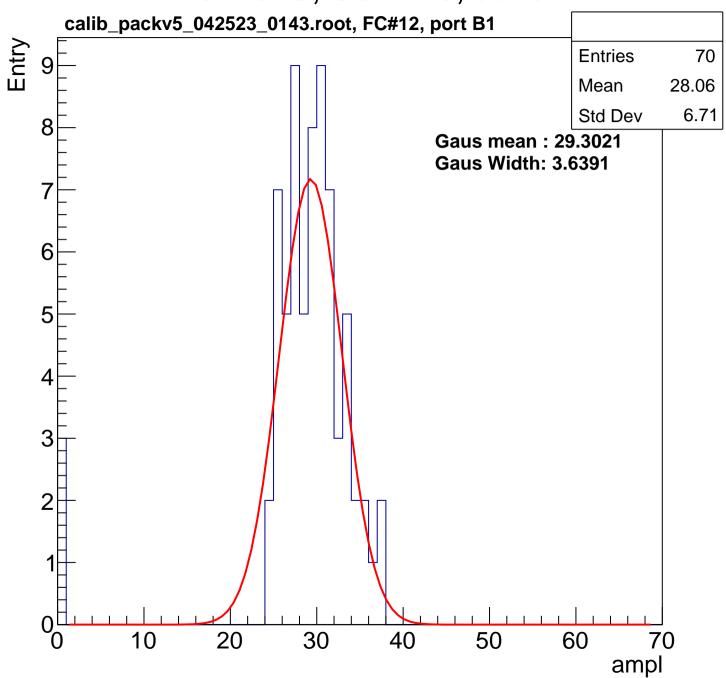


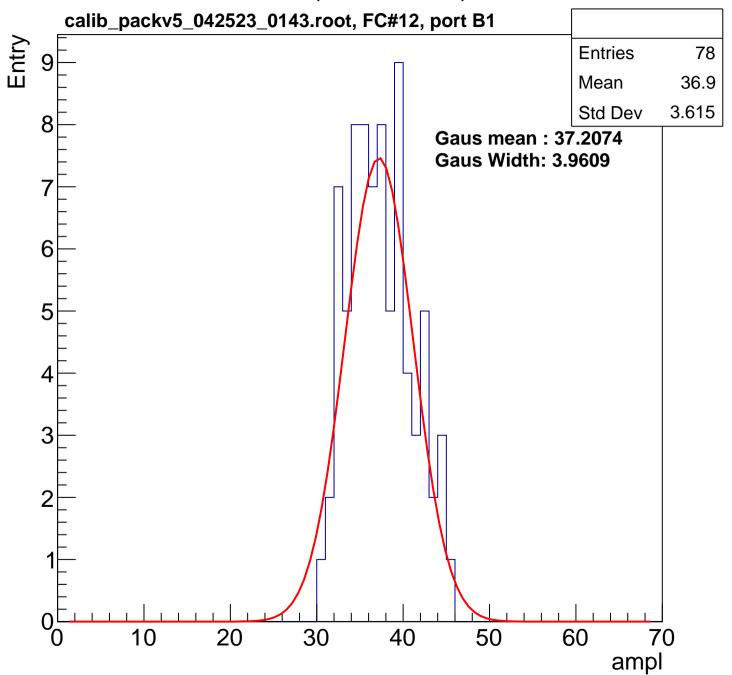


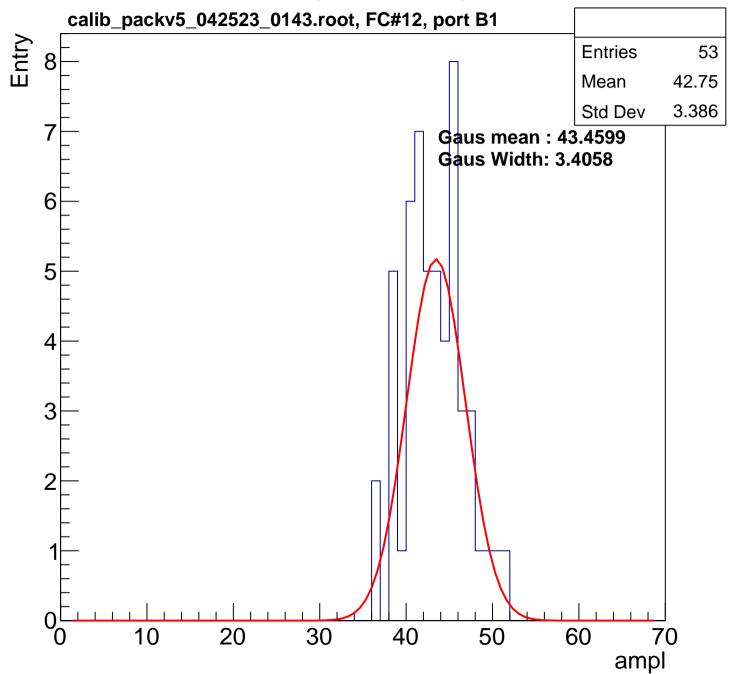


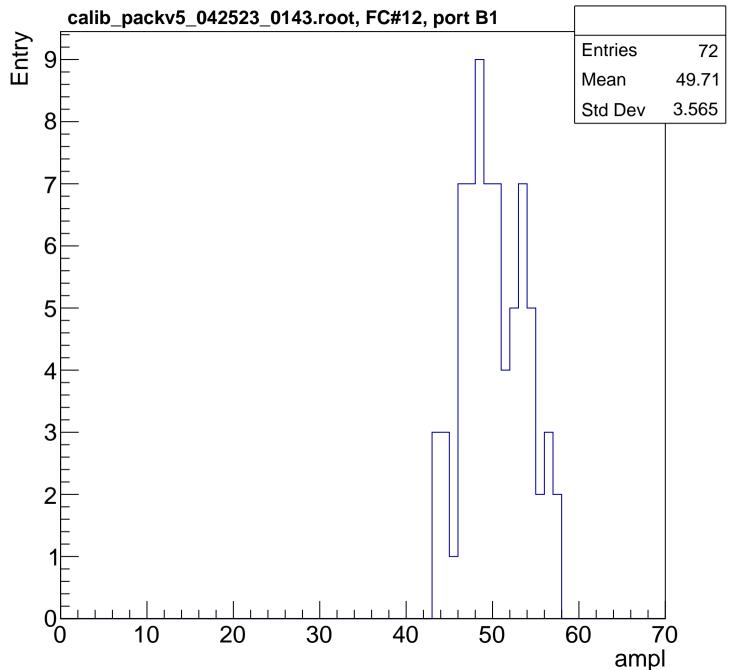


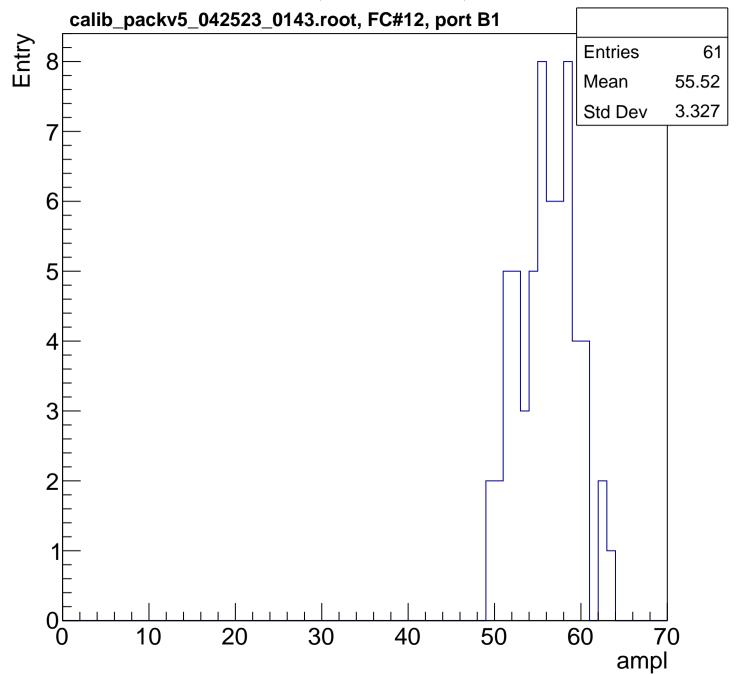


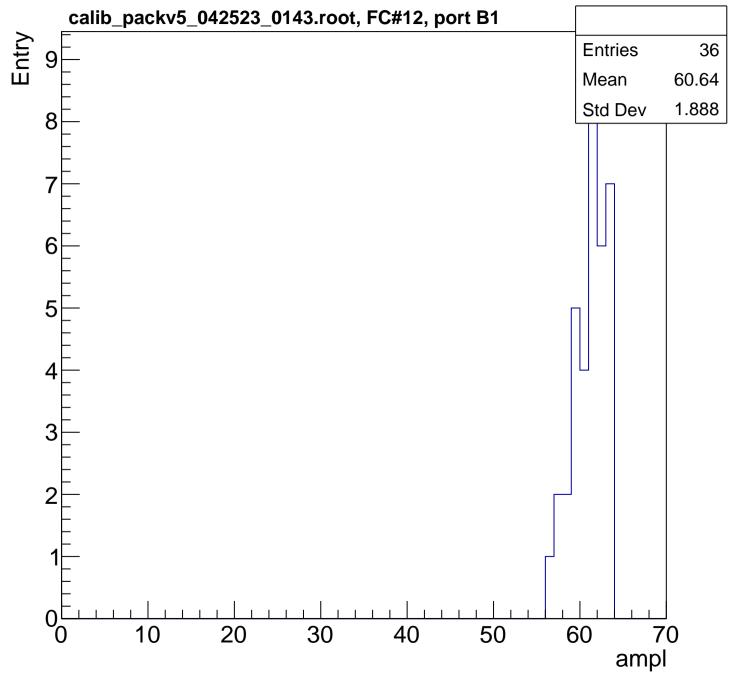


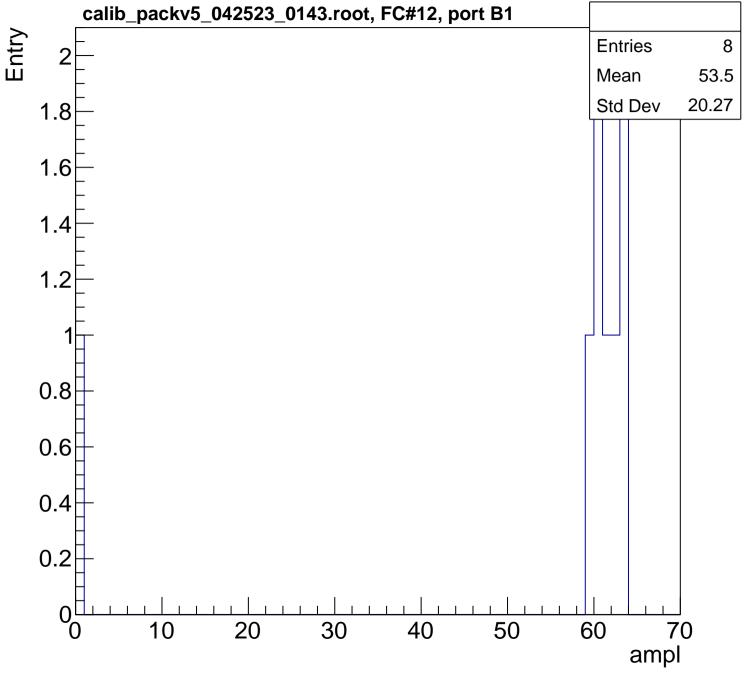


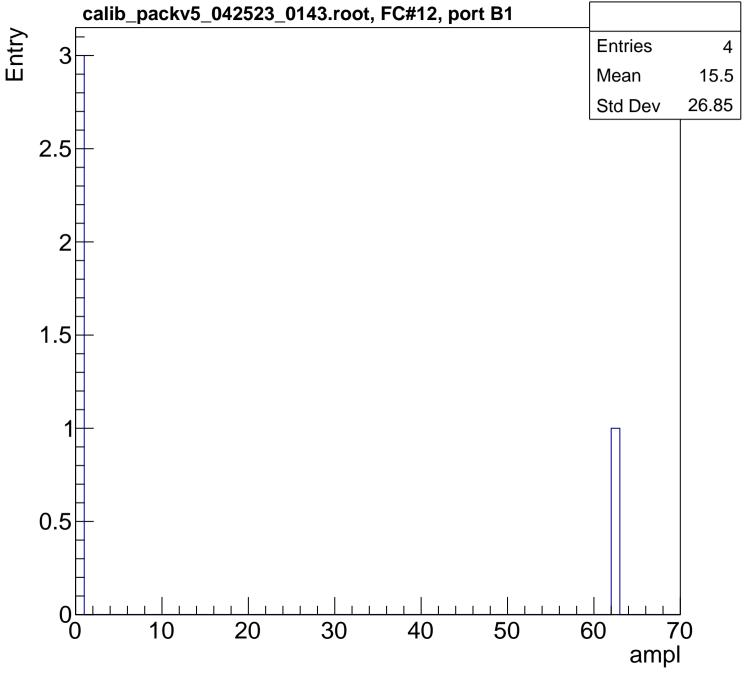


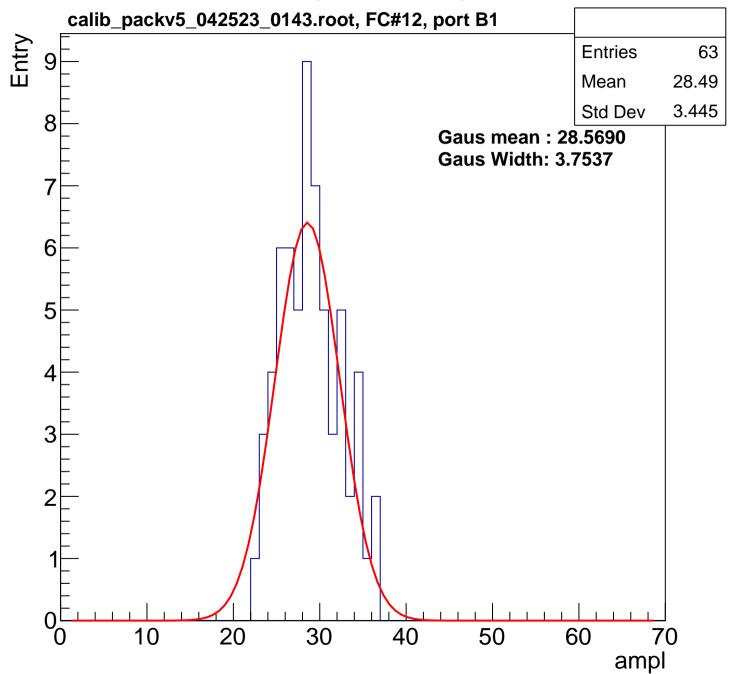


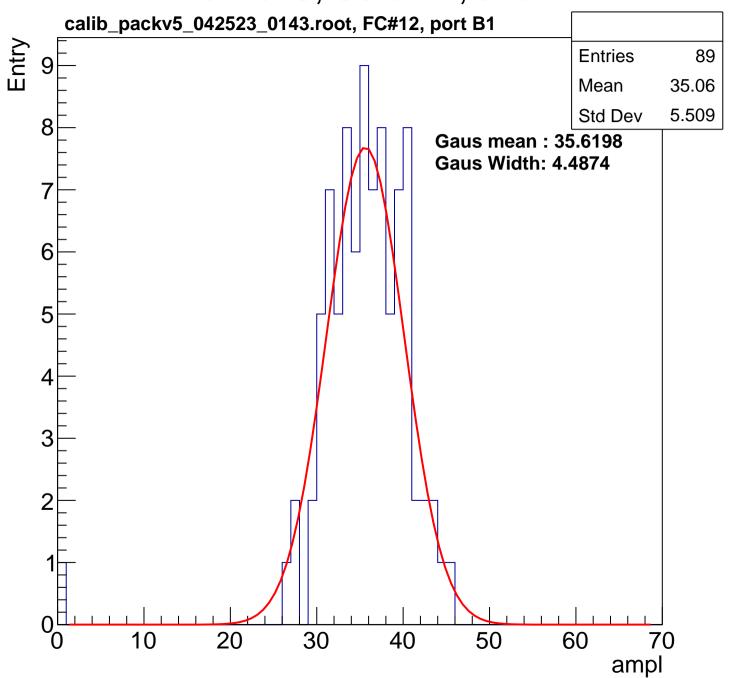


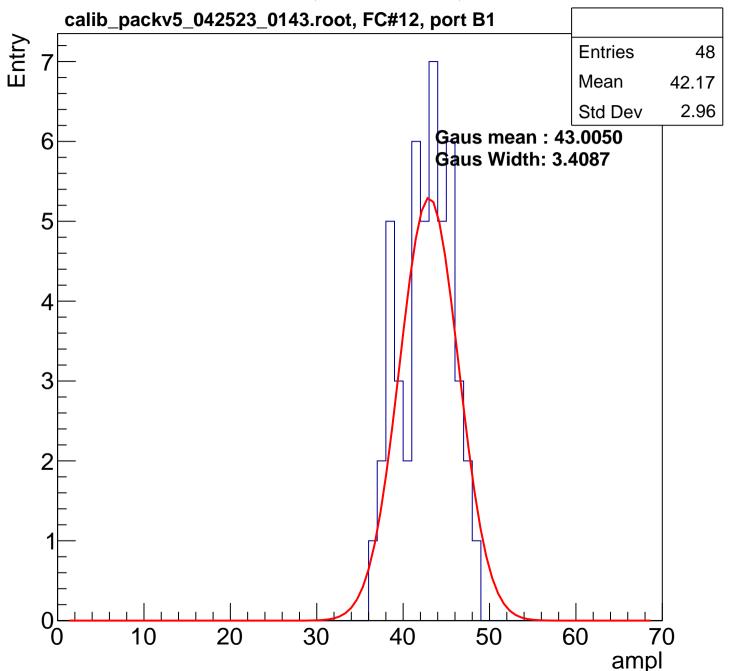


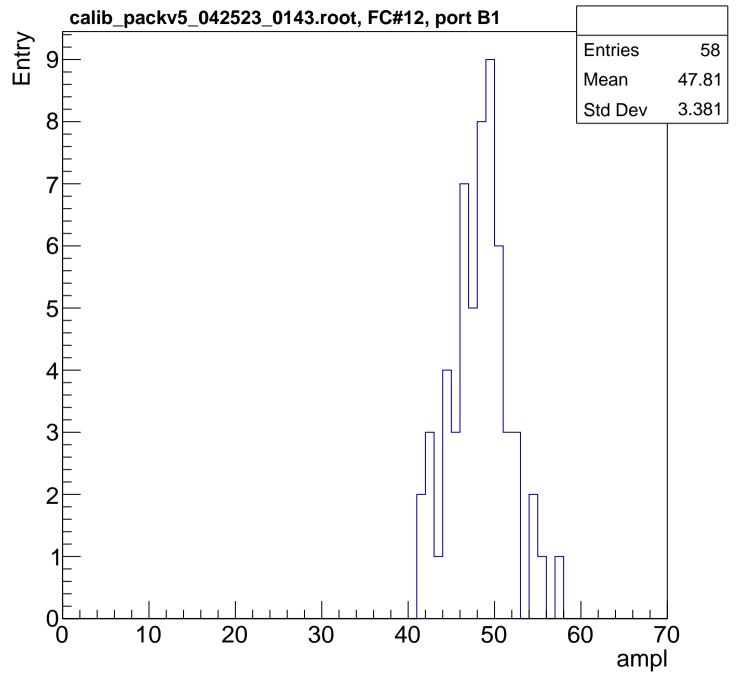


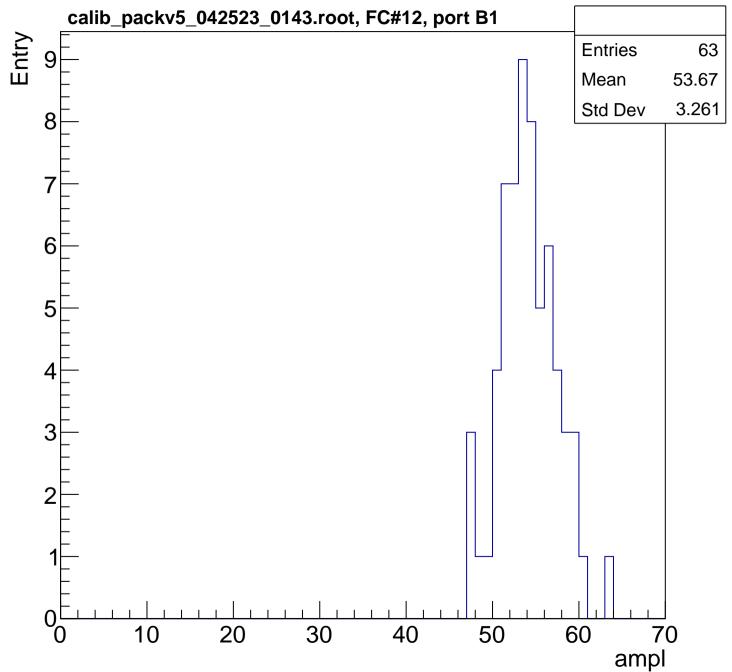


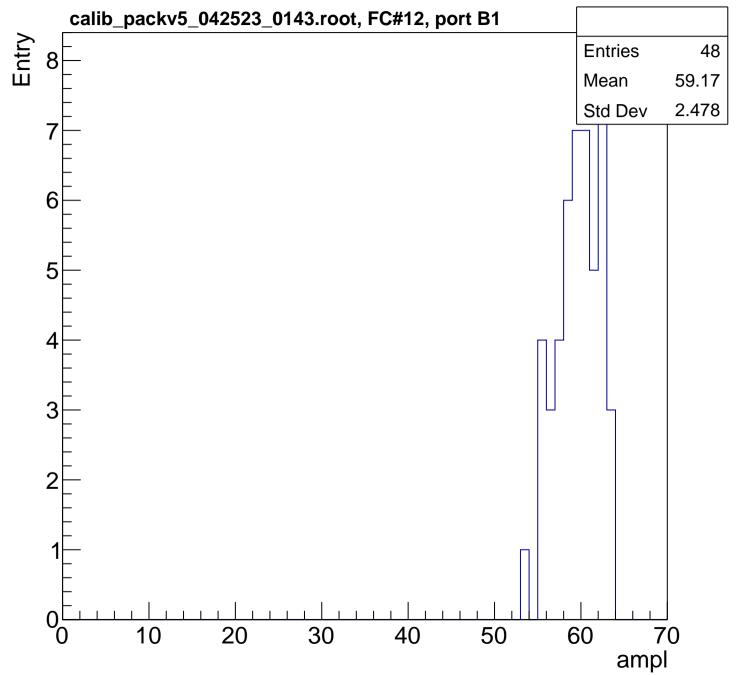


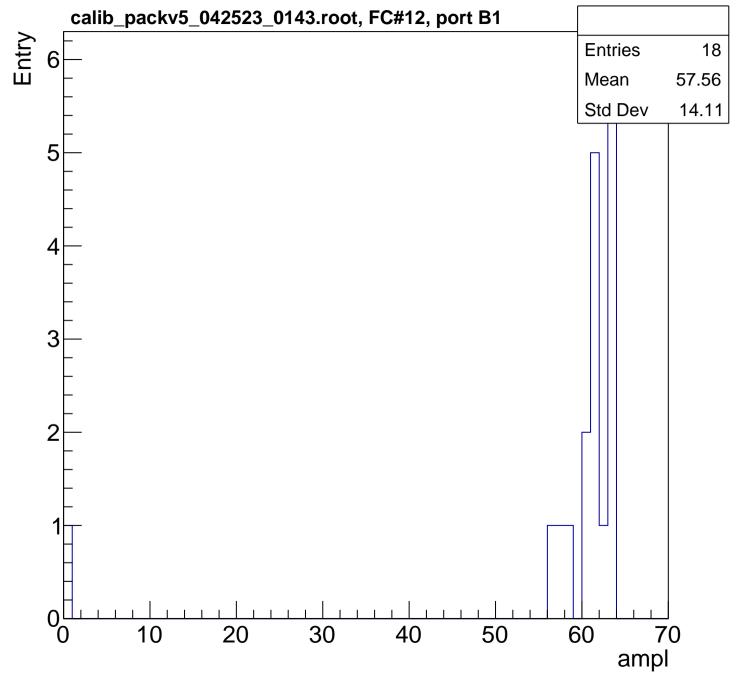


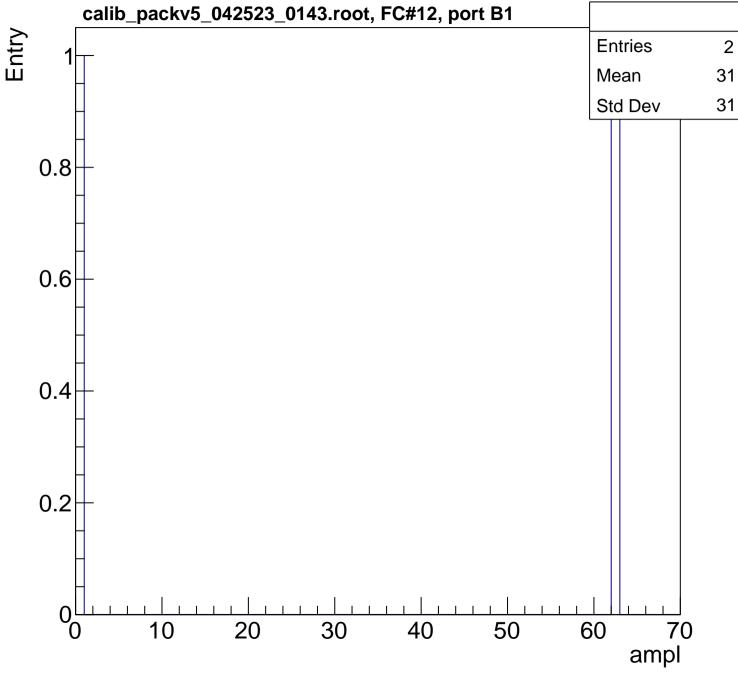


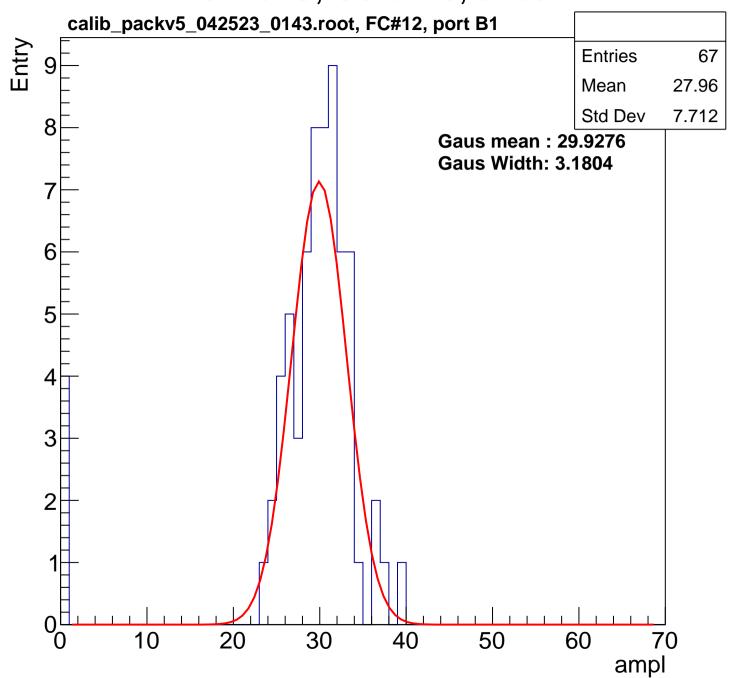


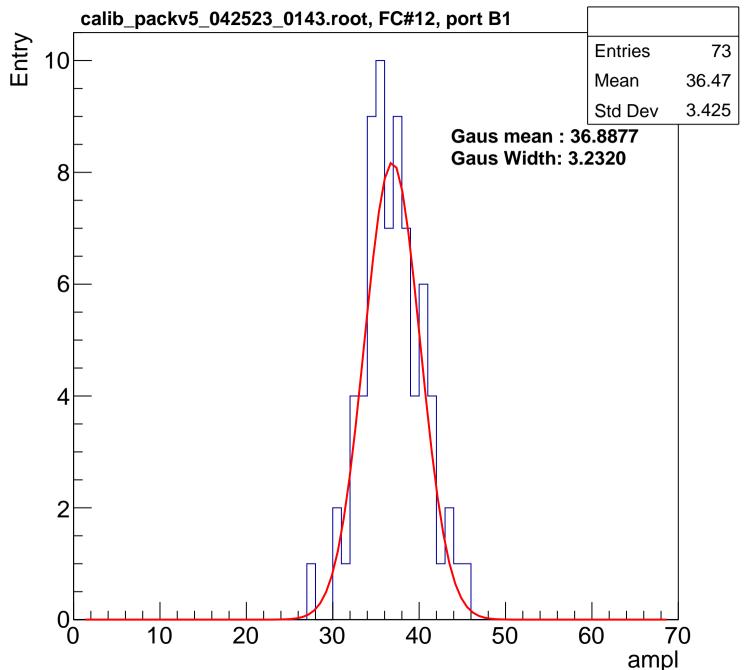


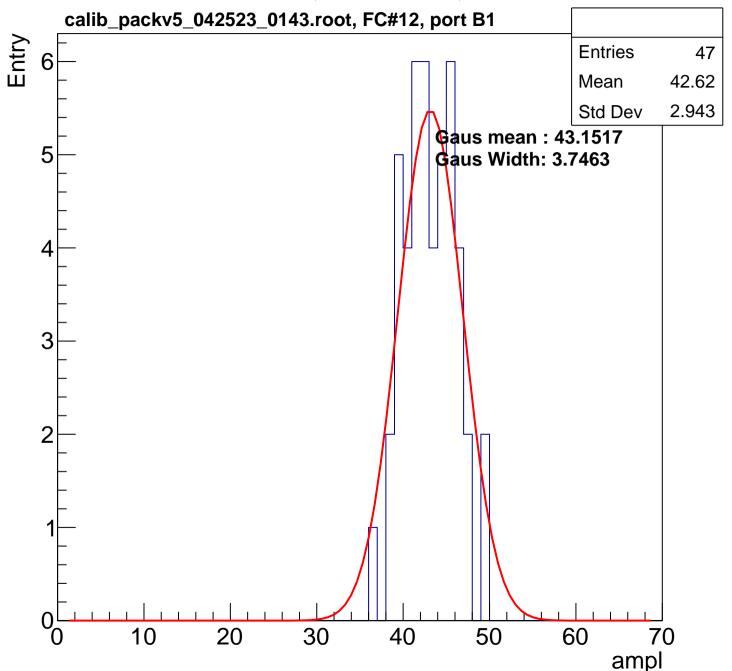


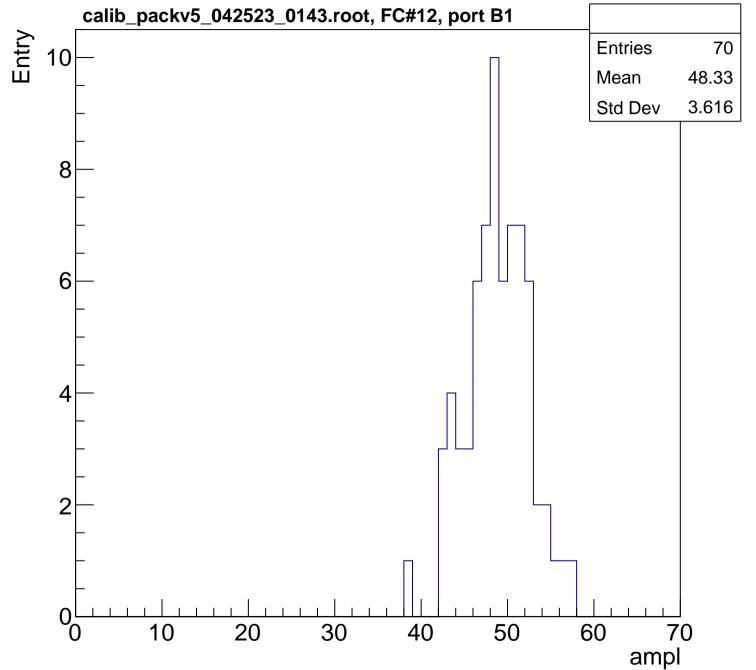


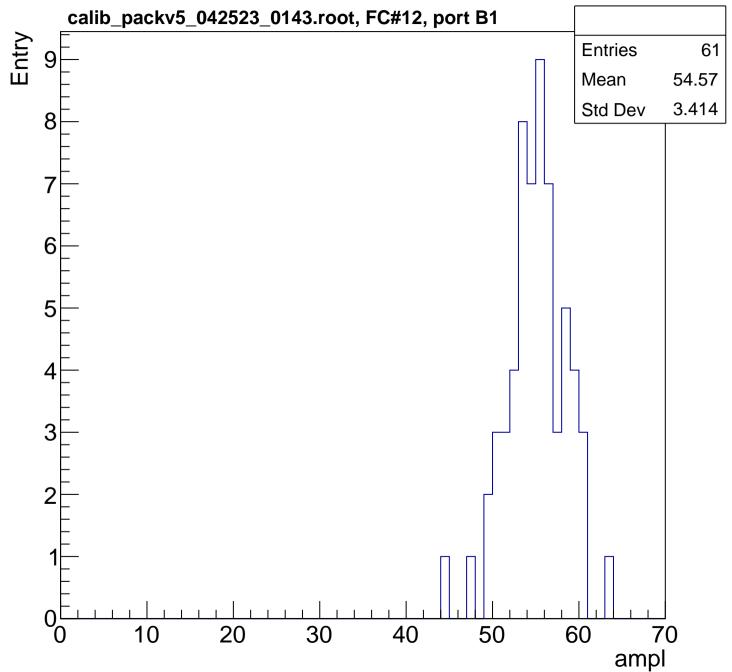


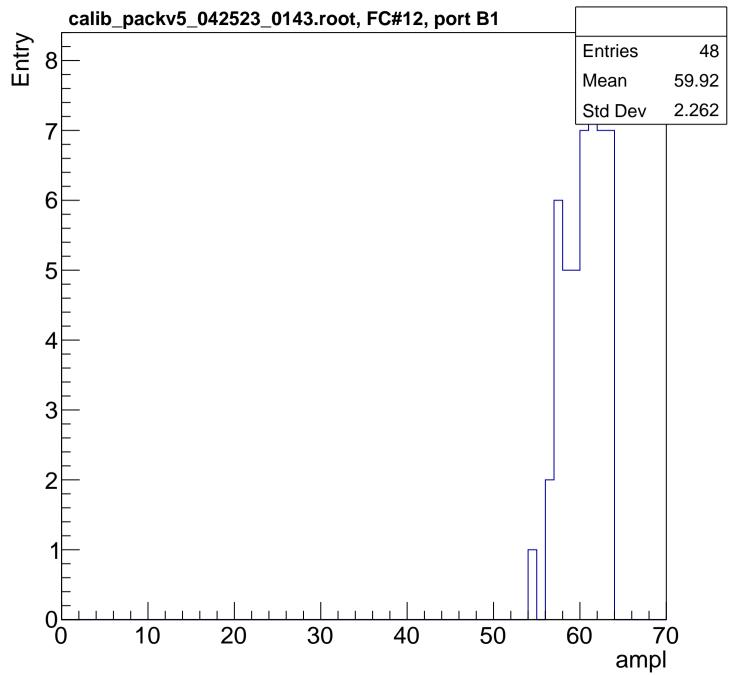


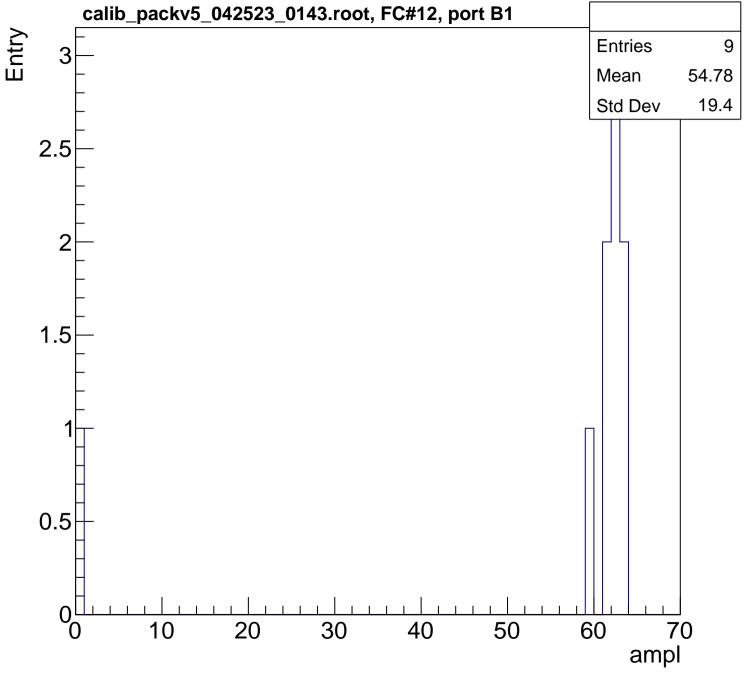




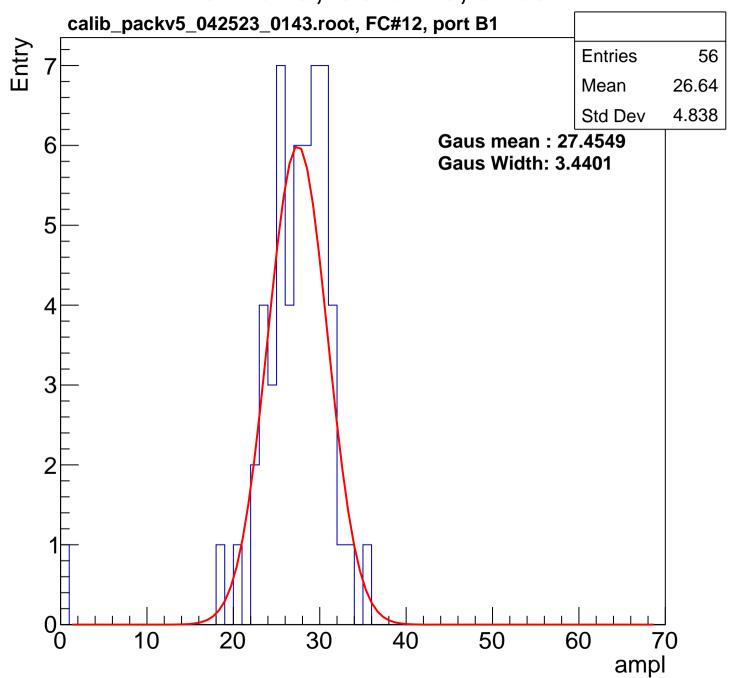


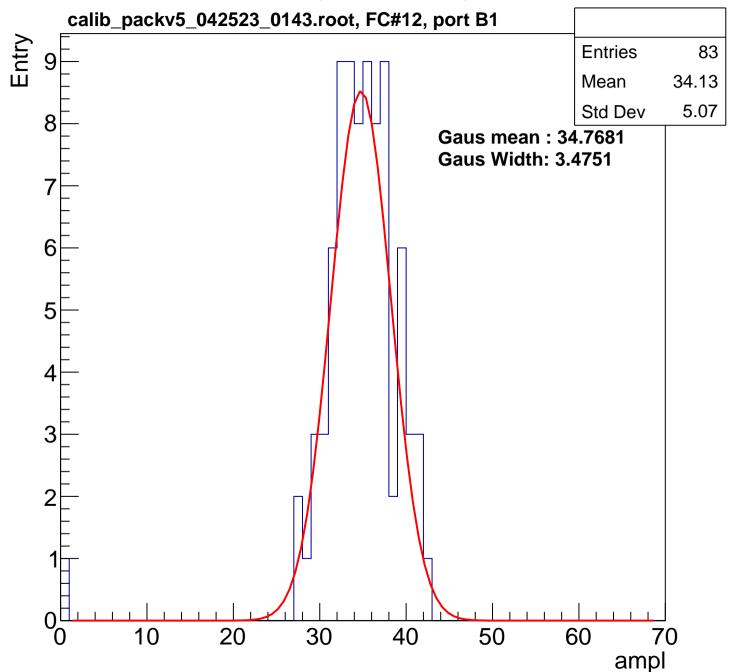


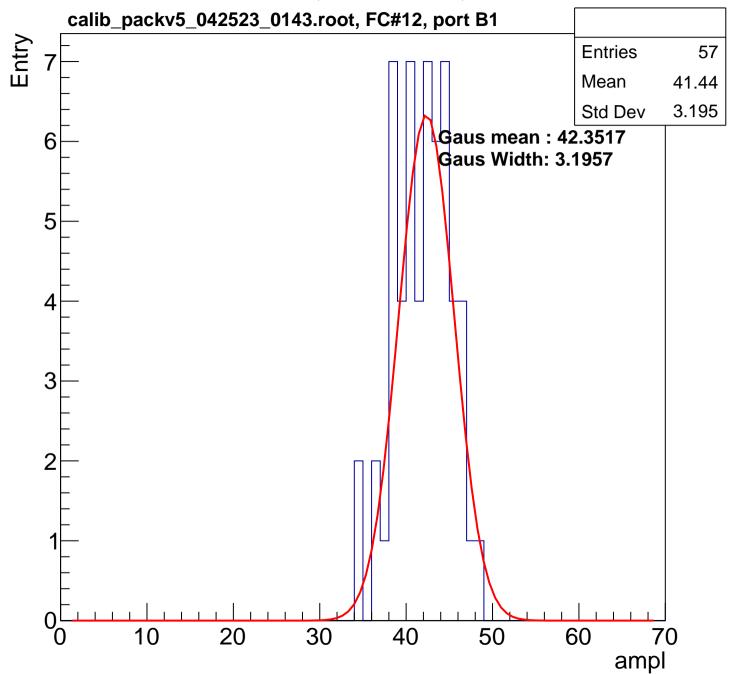


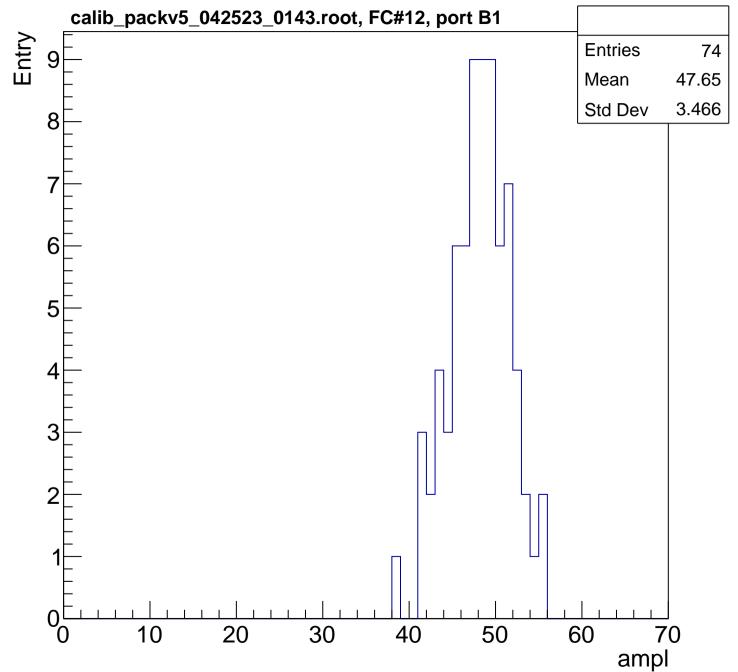


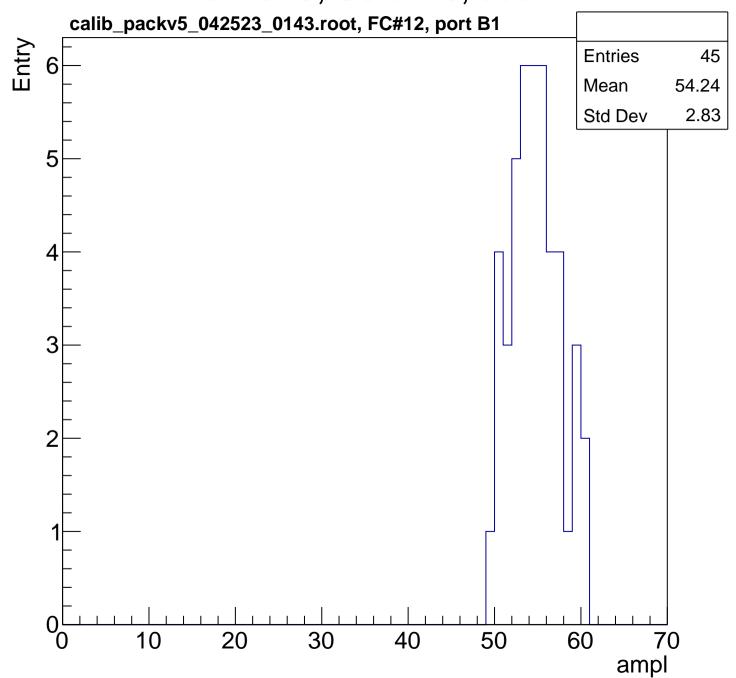


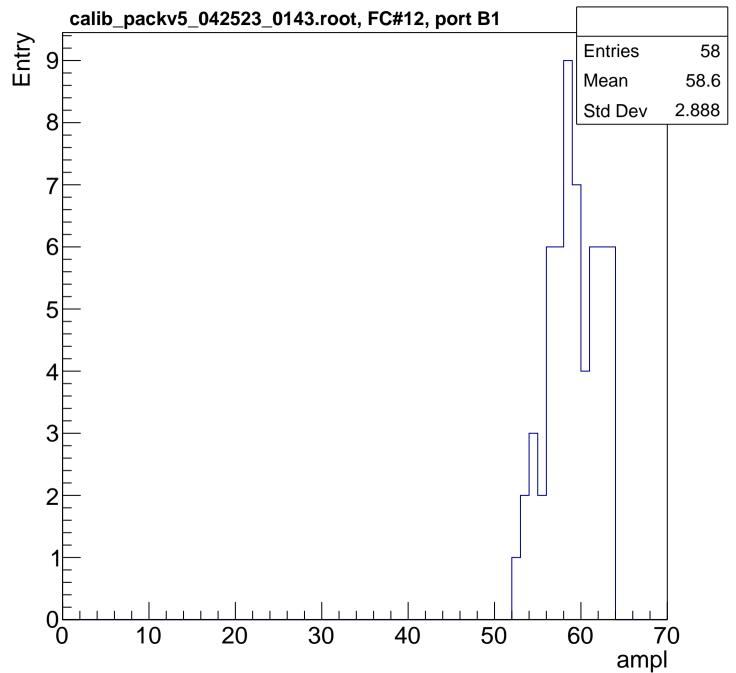


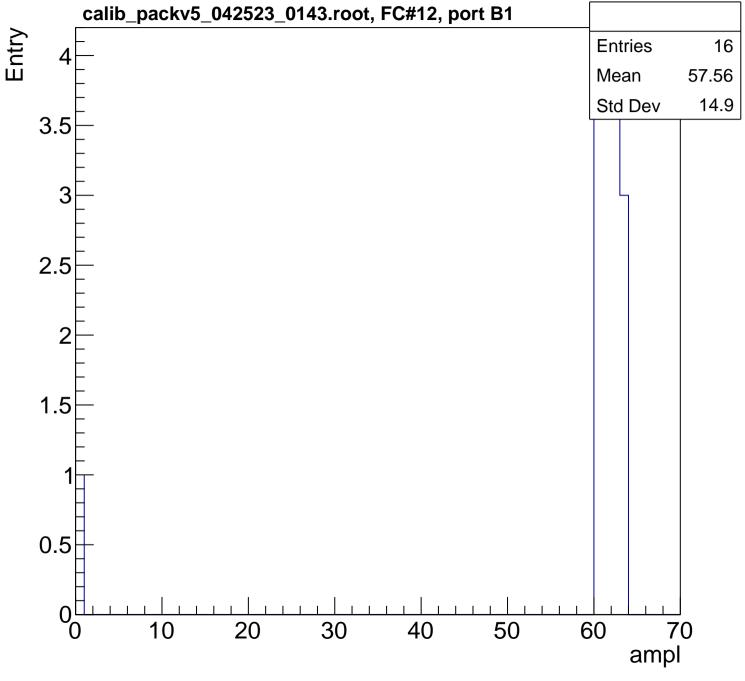


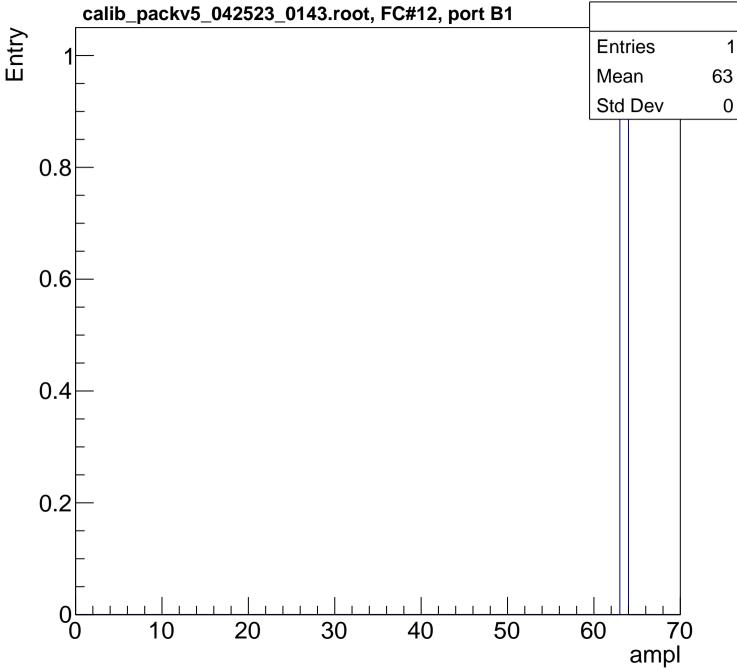


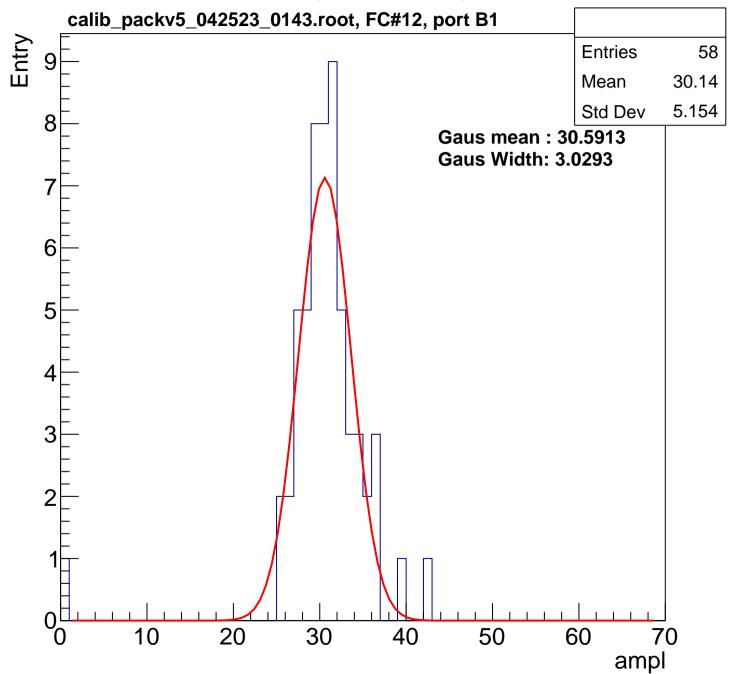


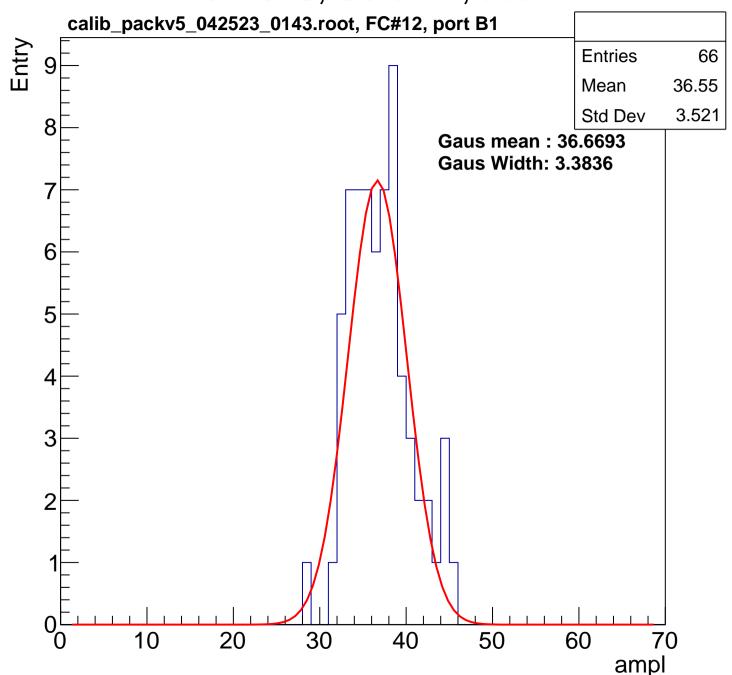


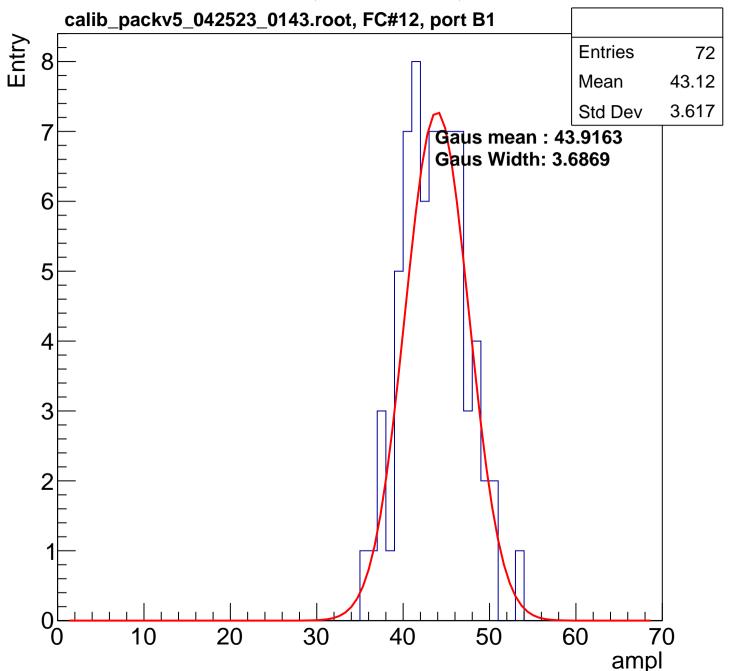


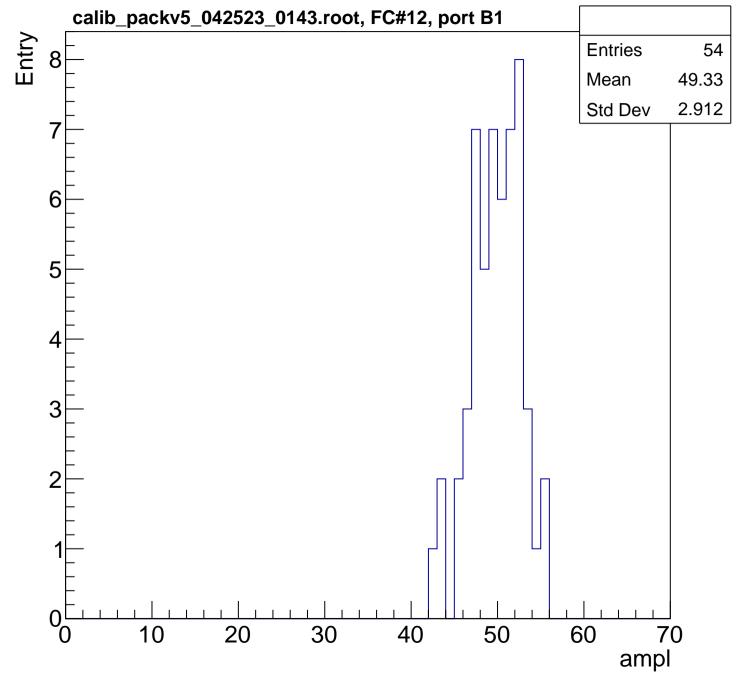


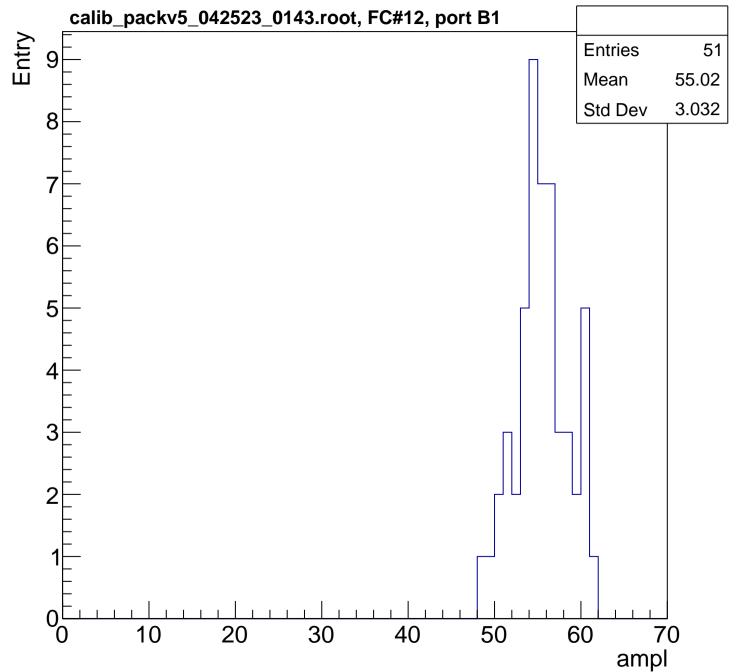


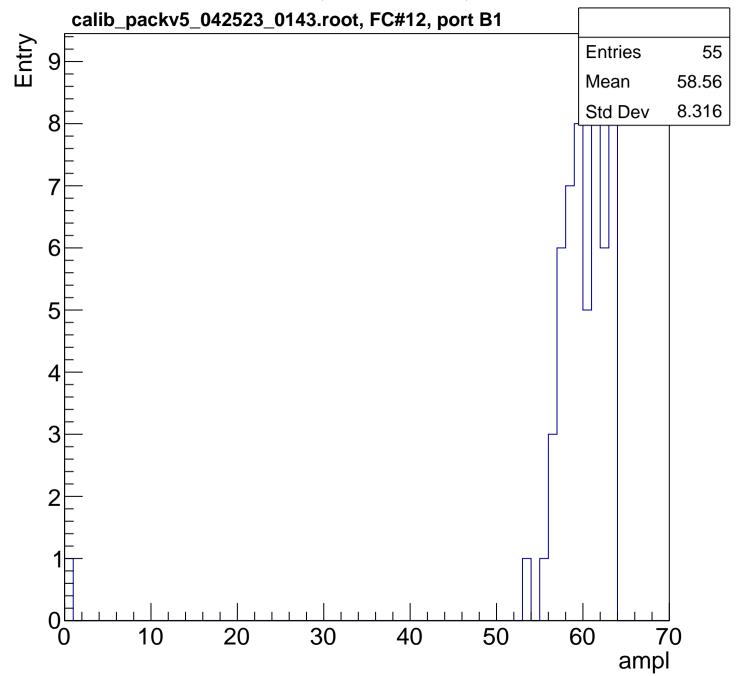


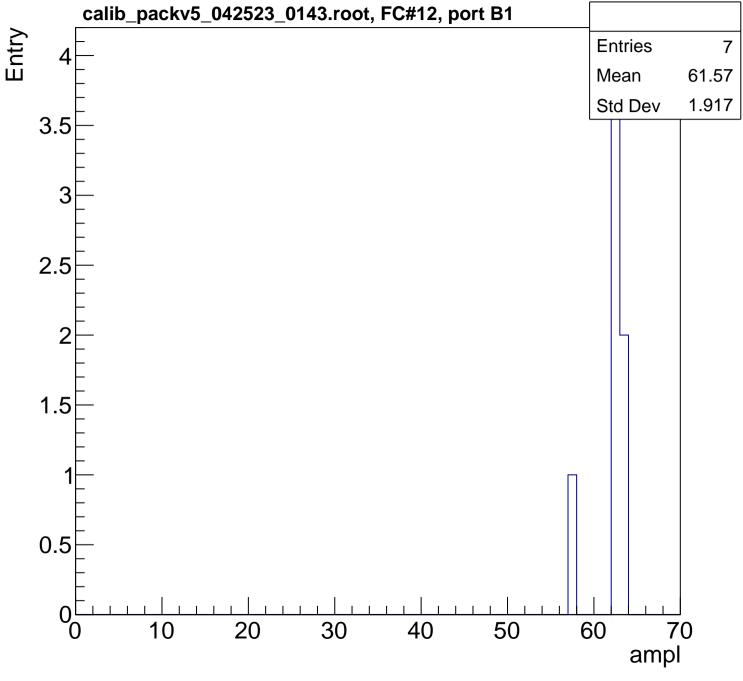




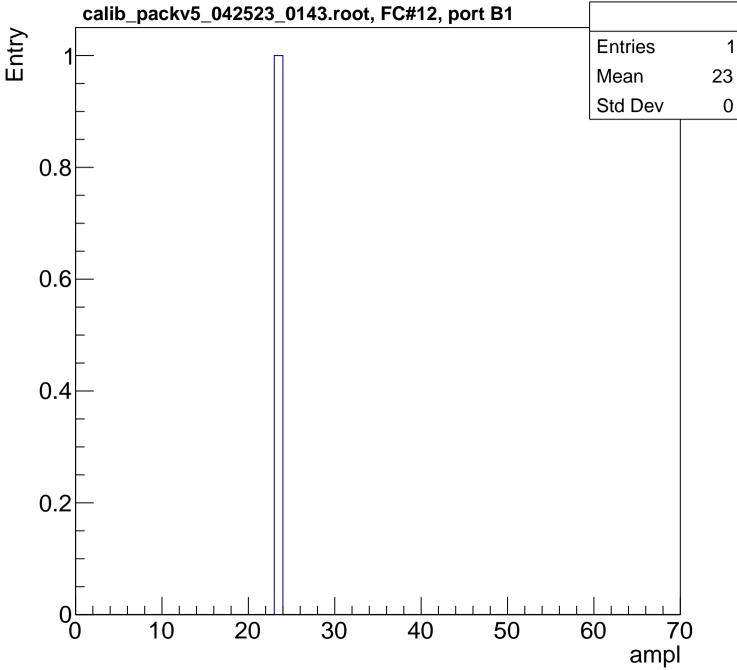


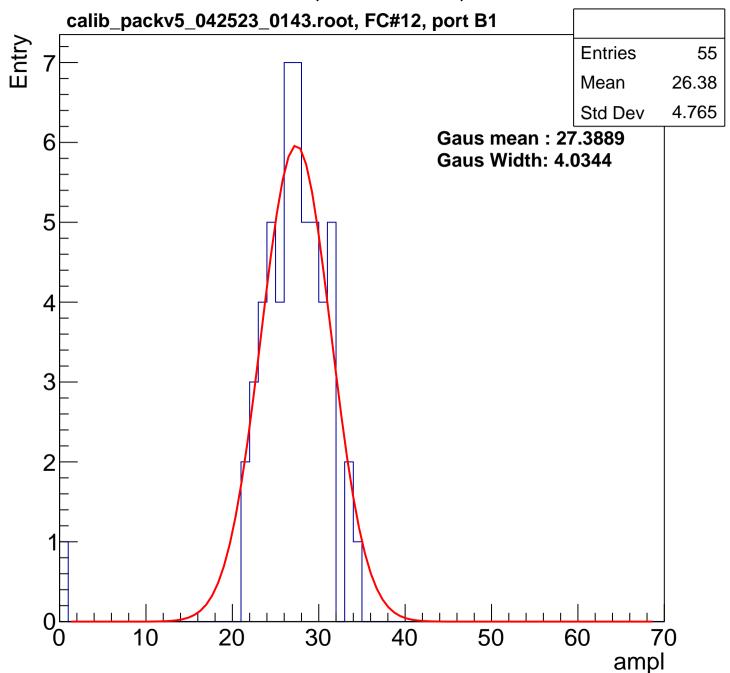


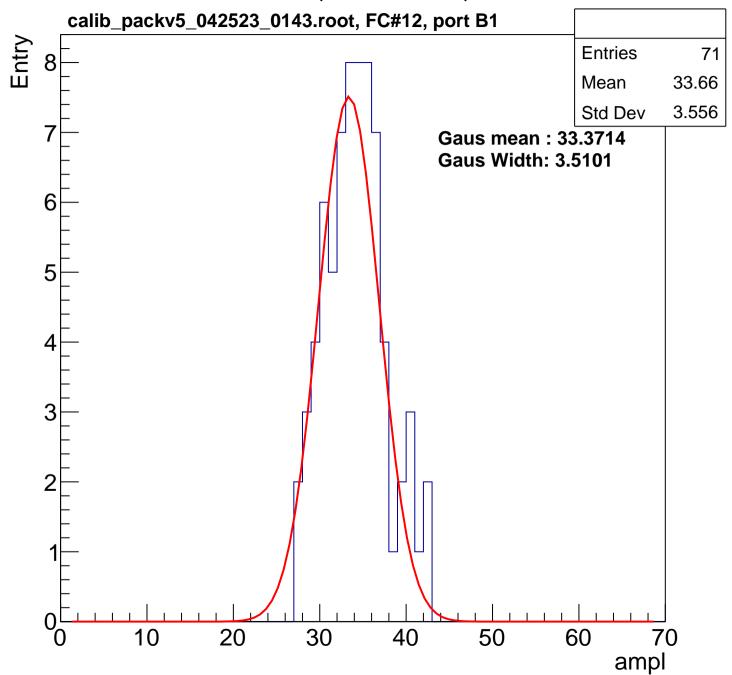


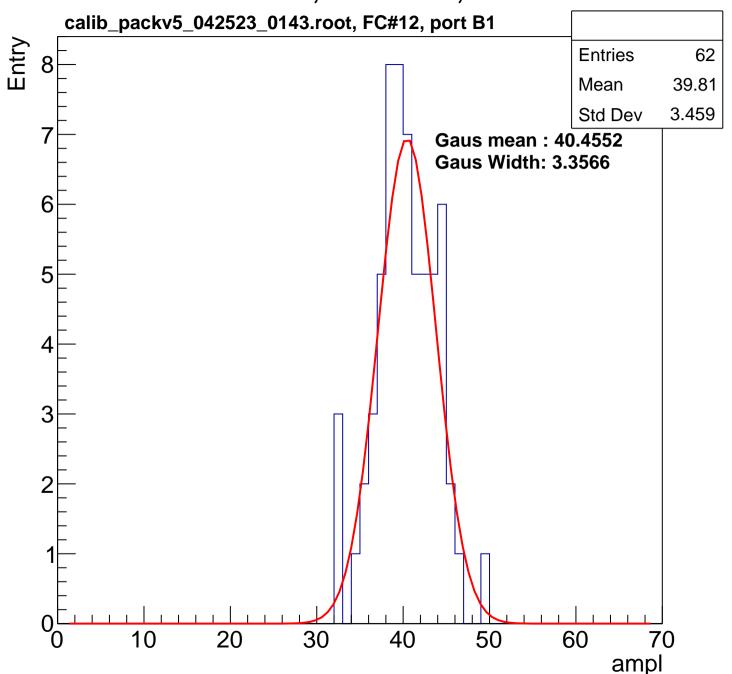


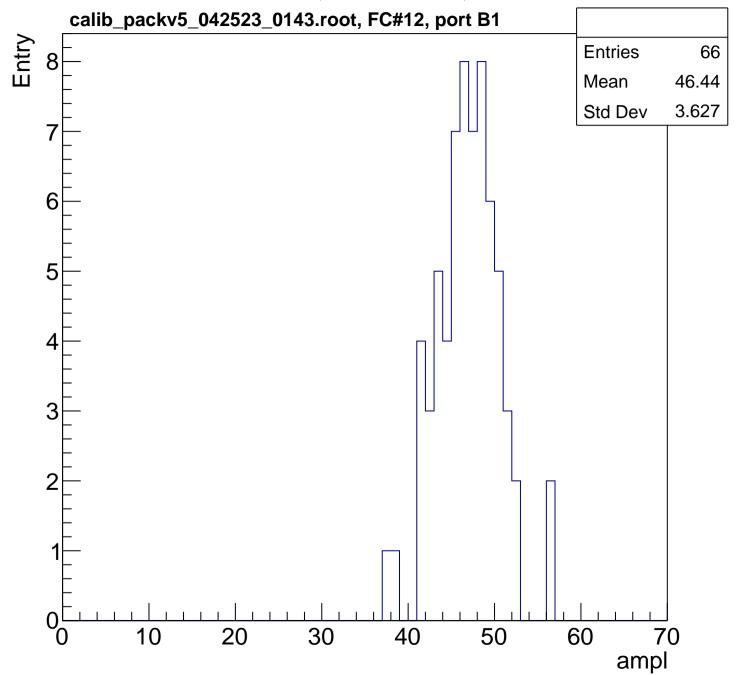
0

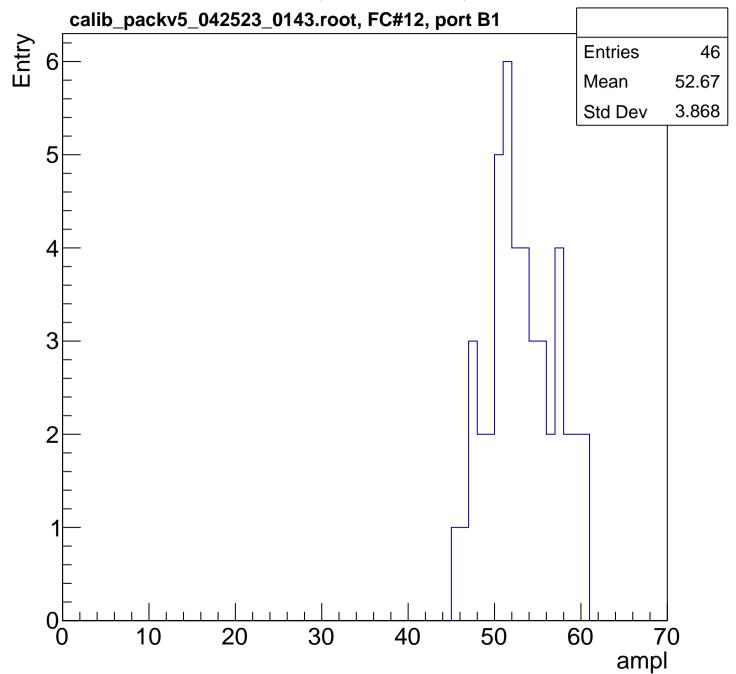


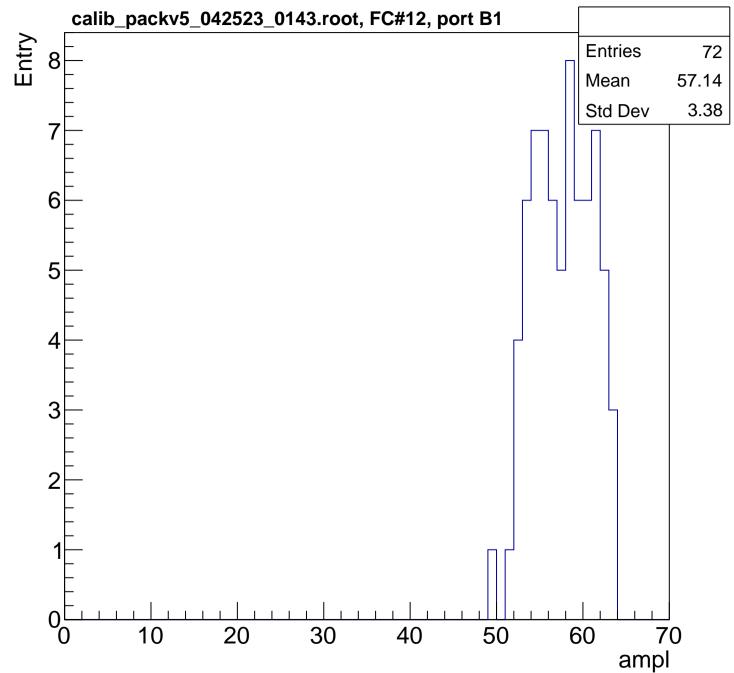


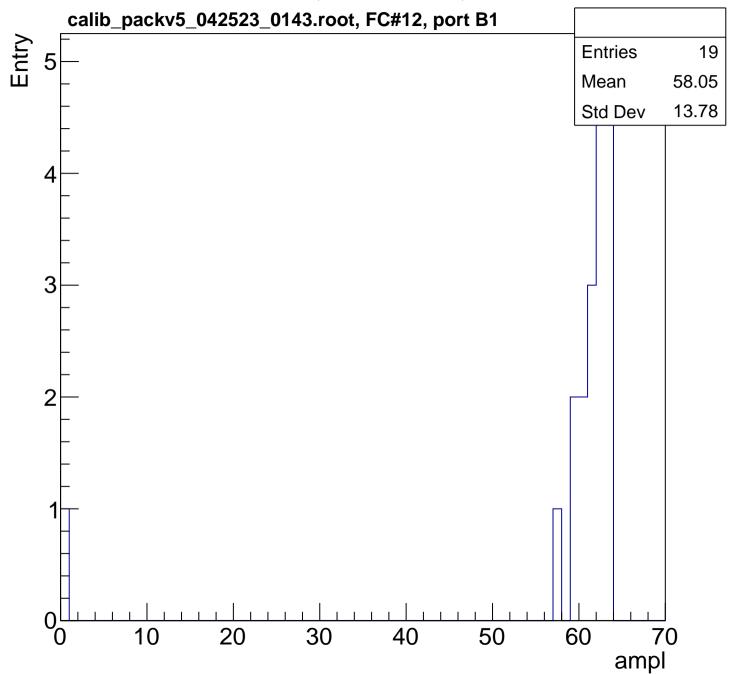


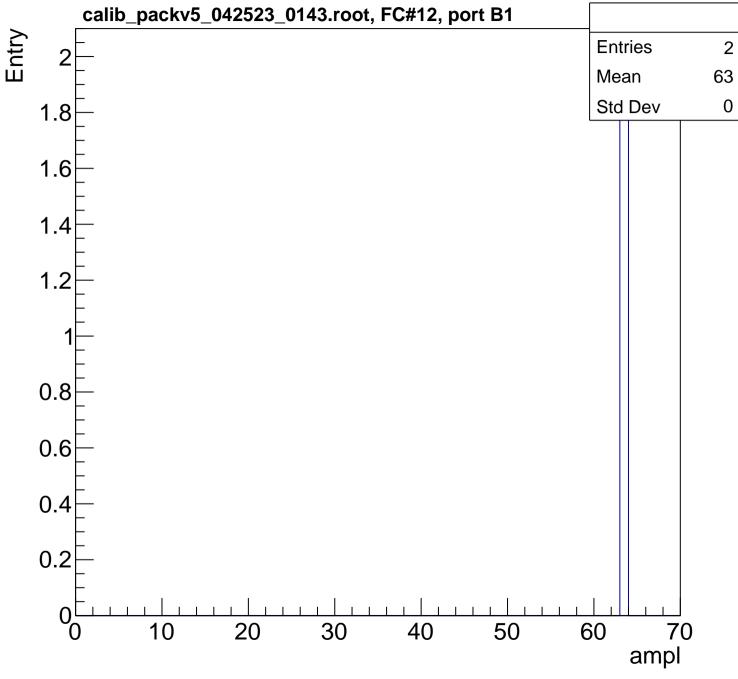


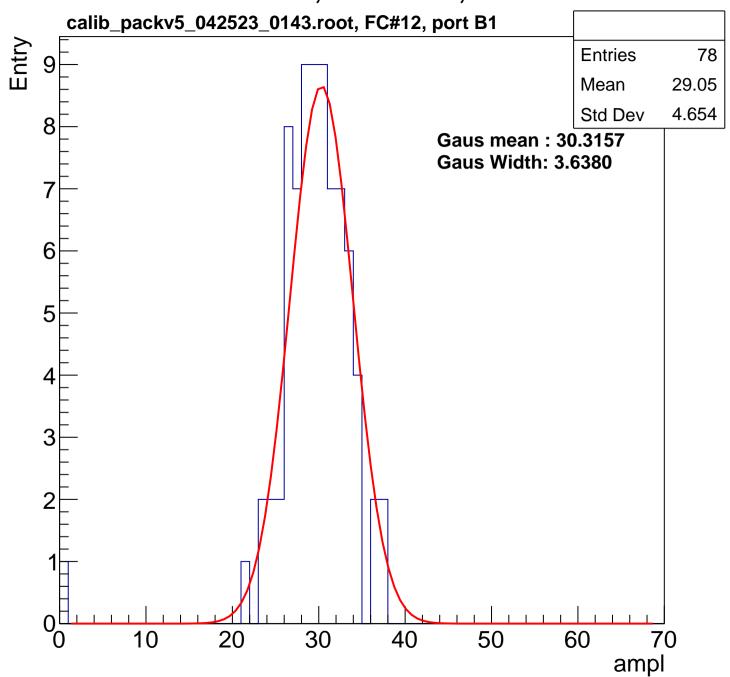


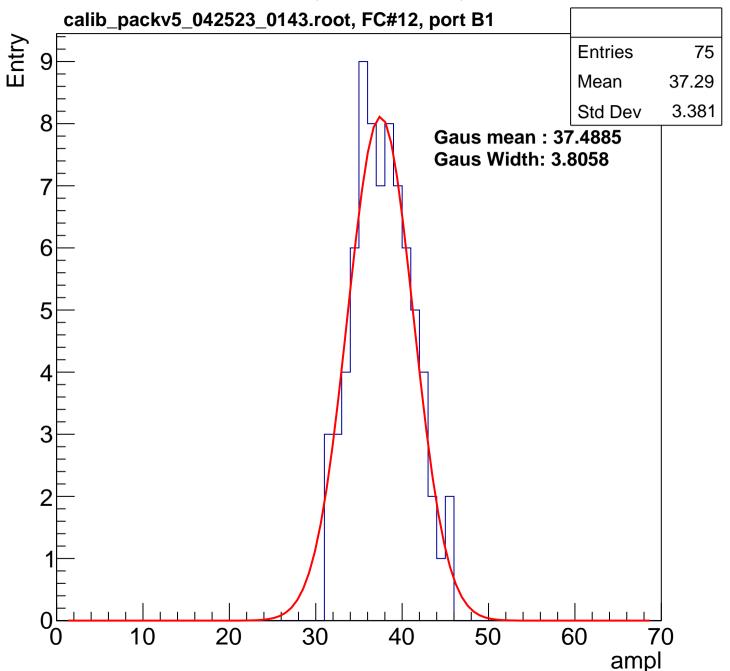


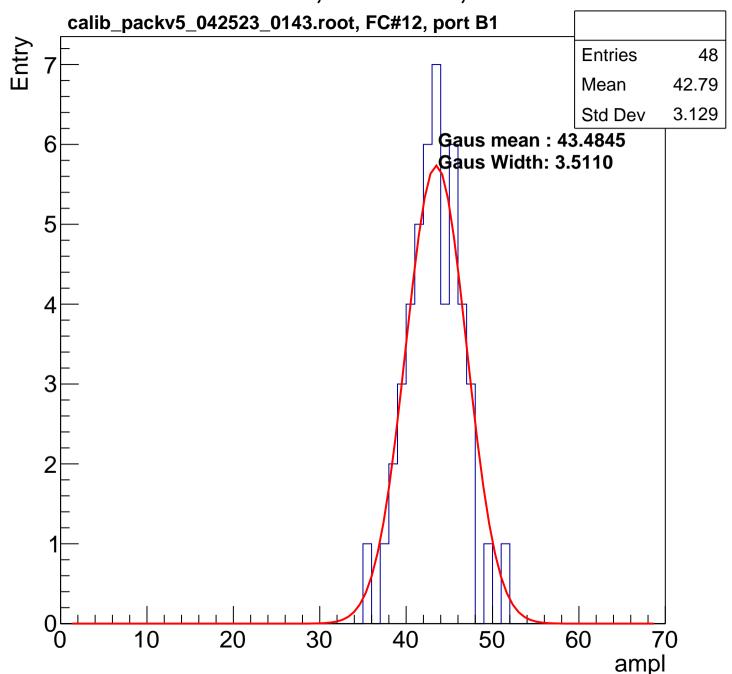


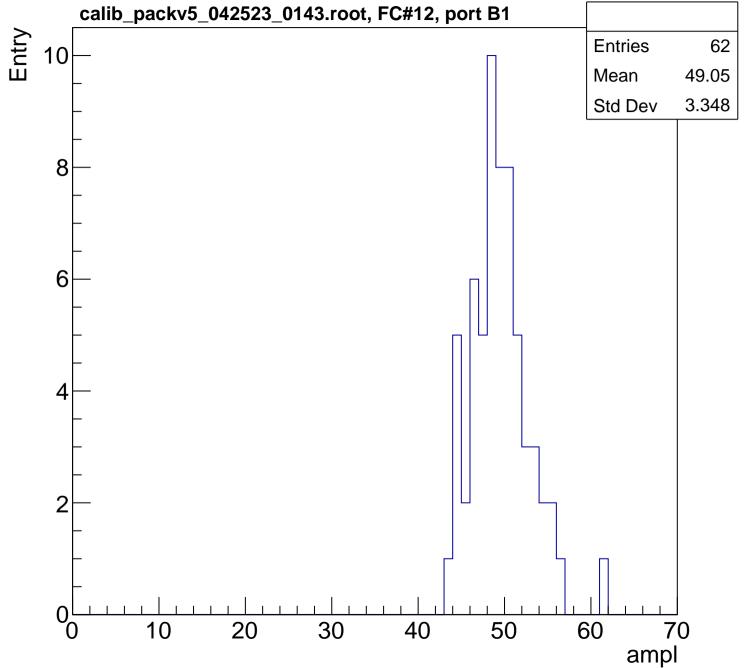


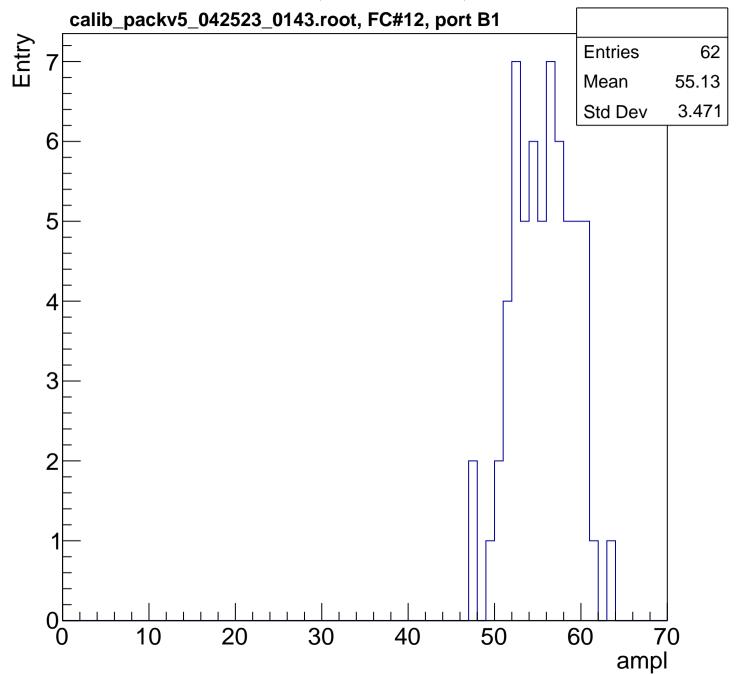


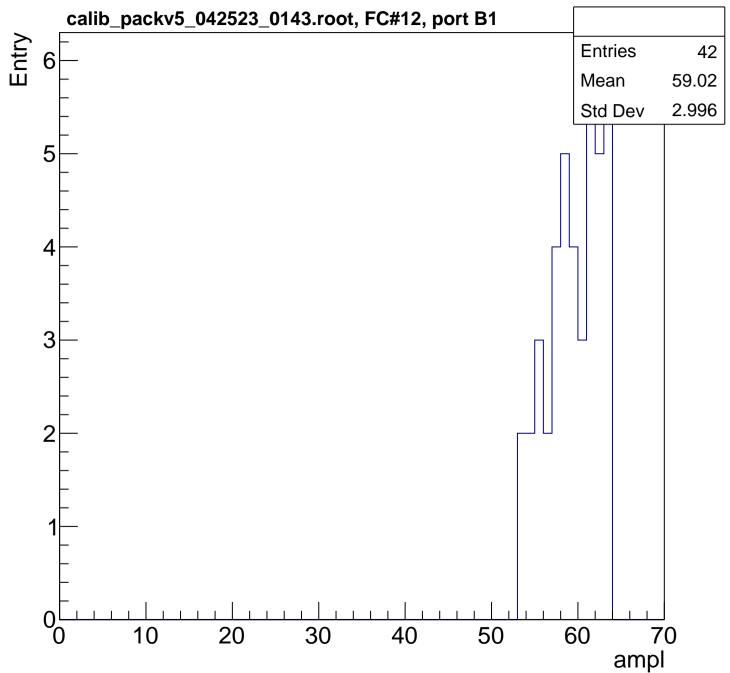


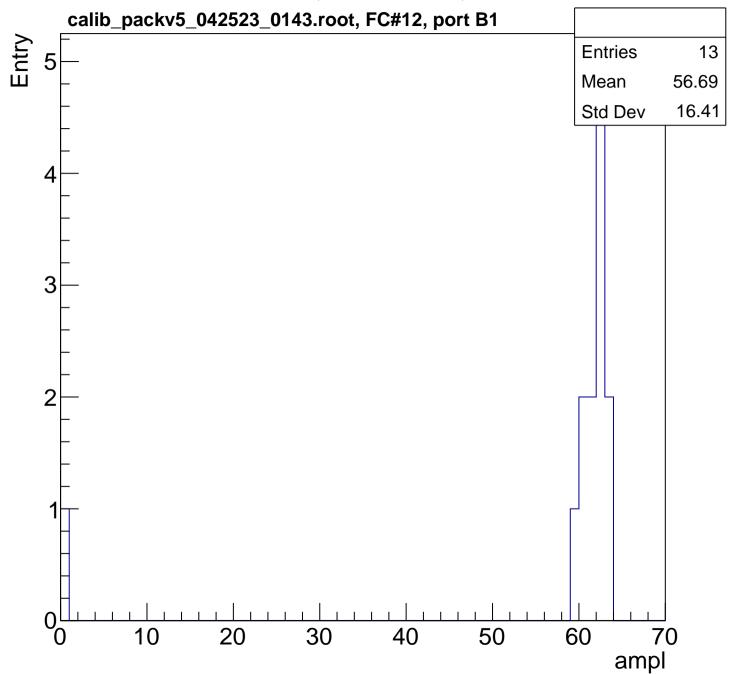




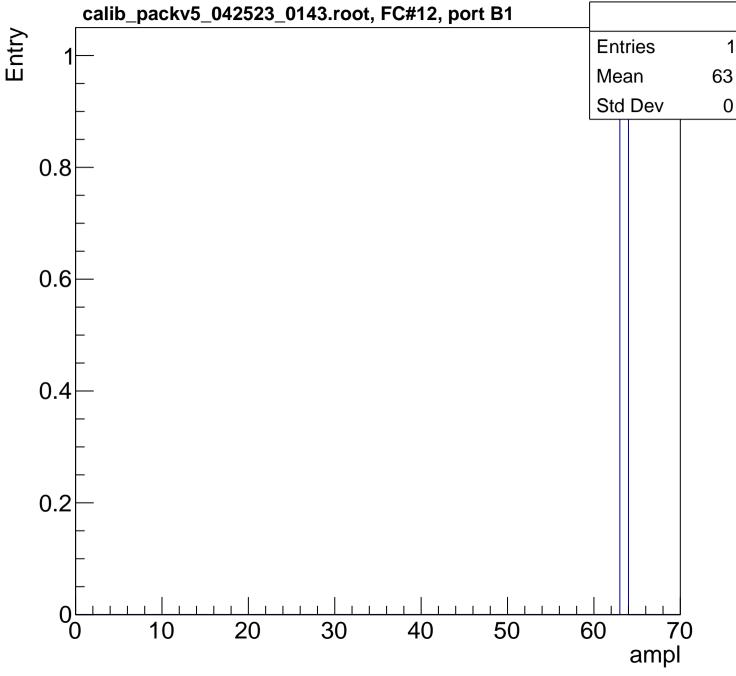


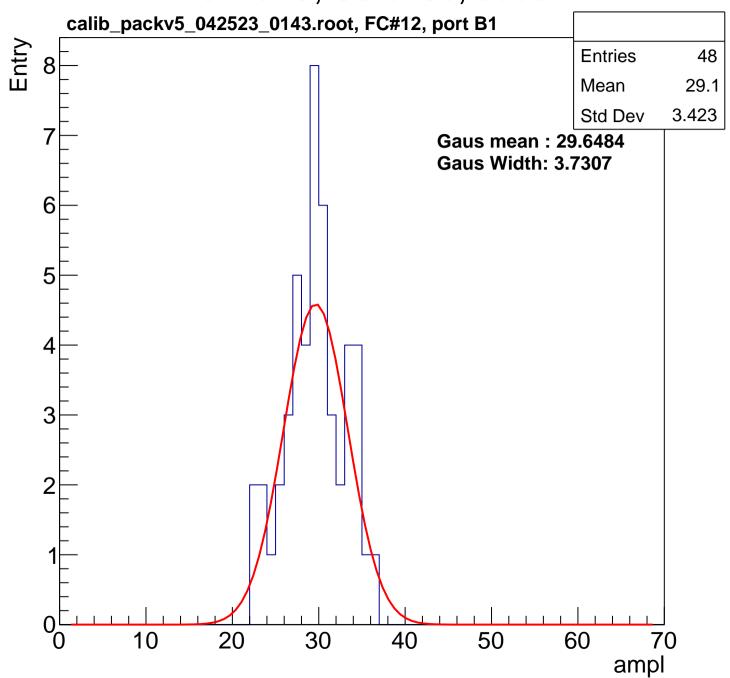


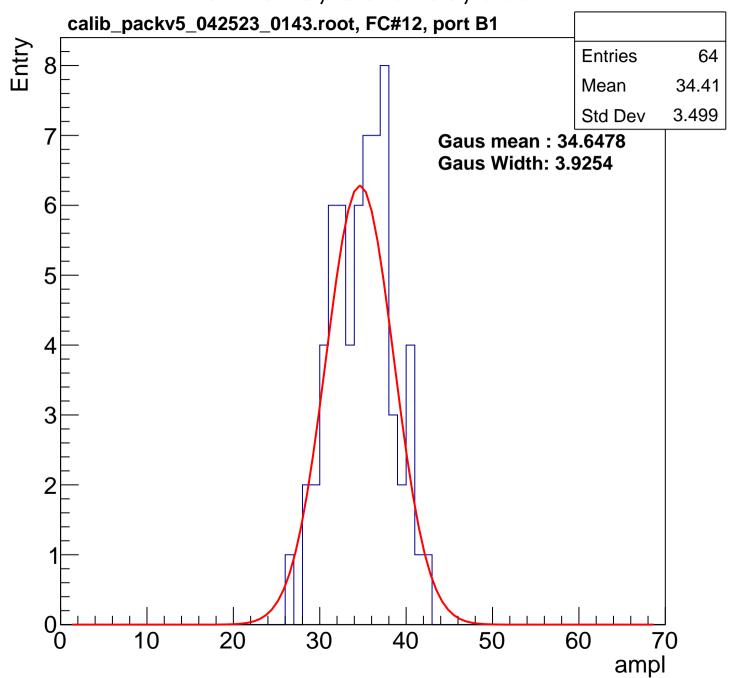


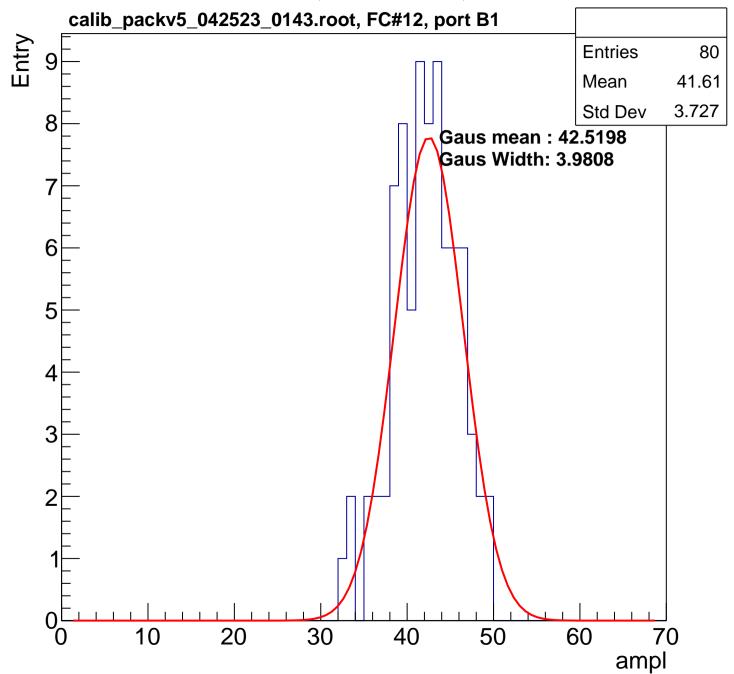


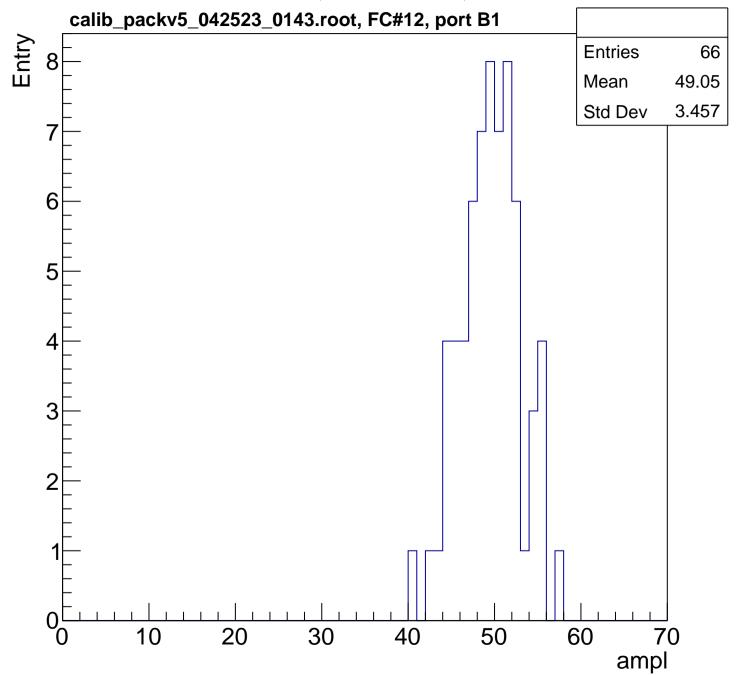
0

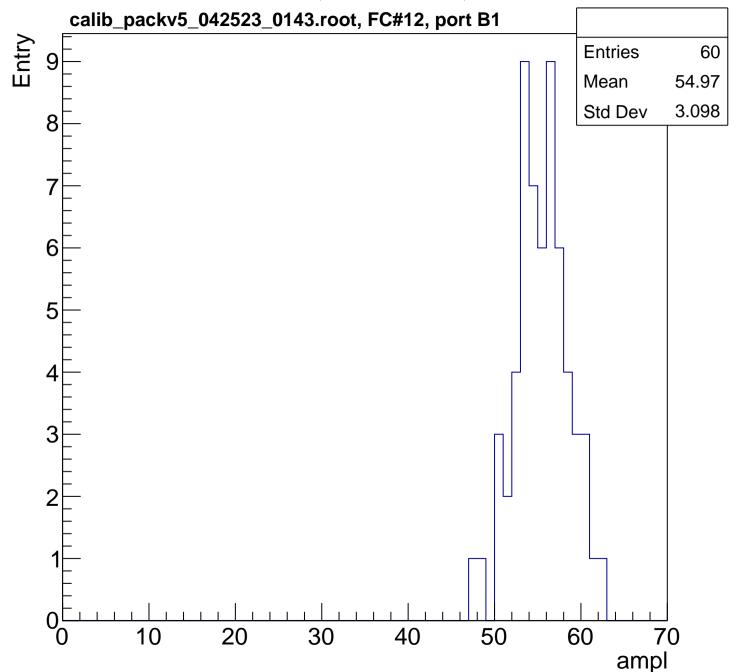


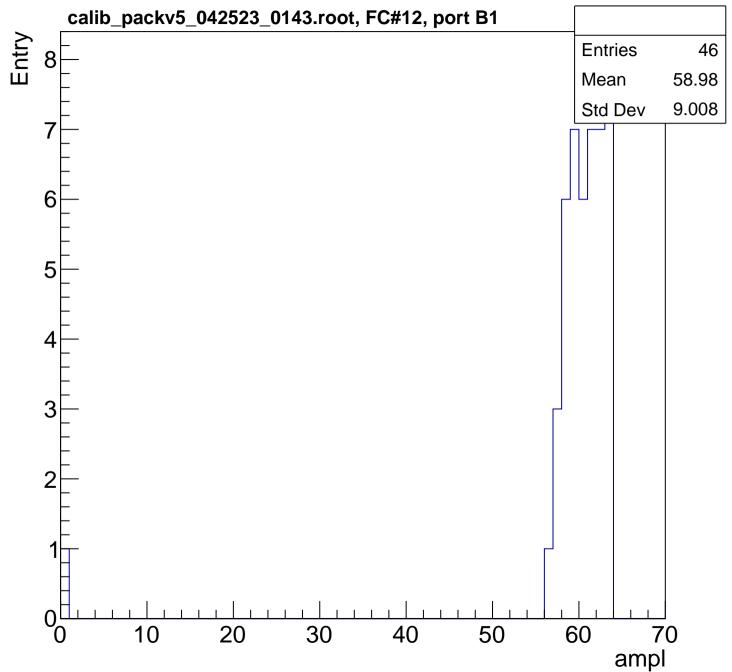


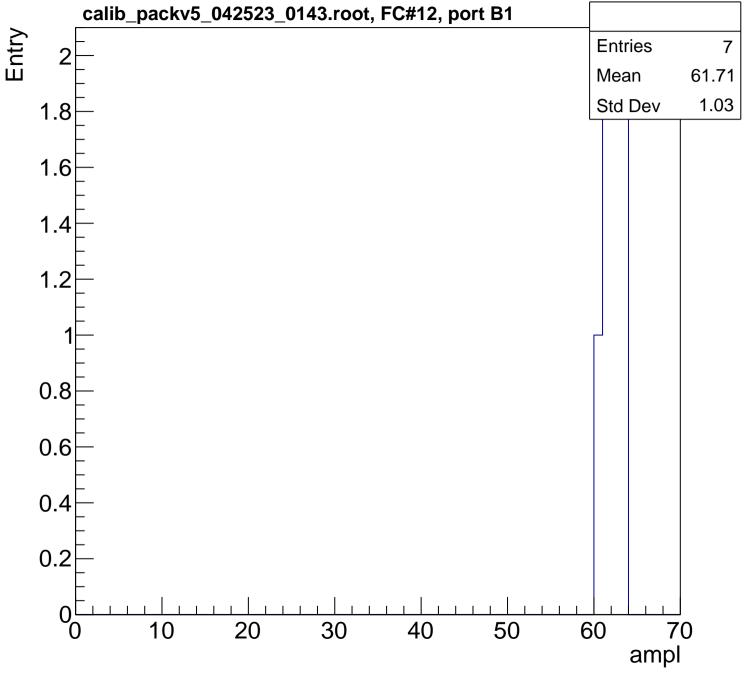




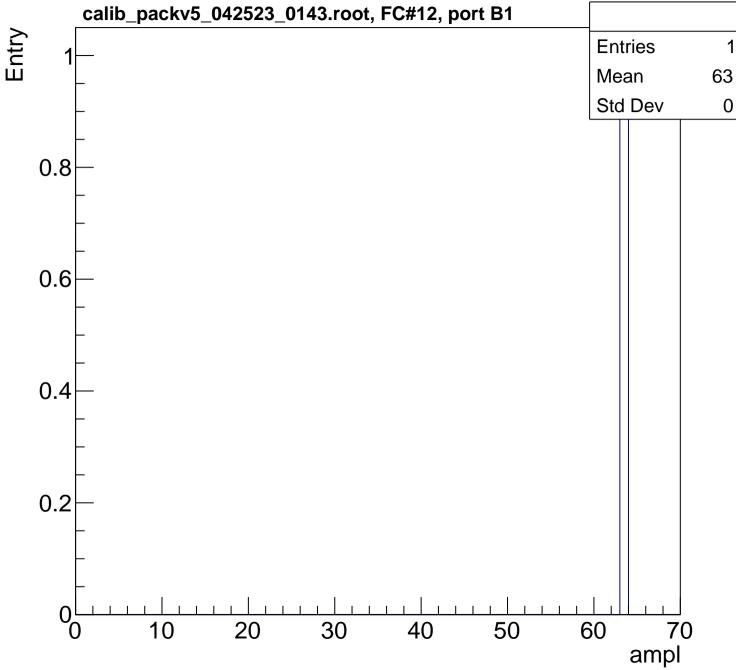


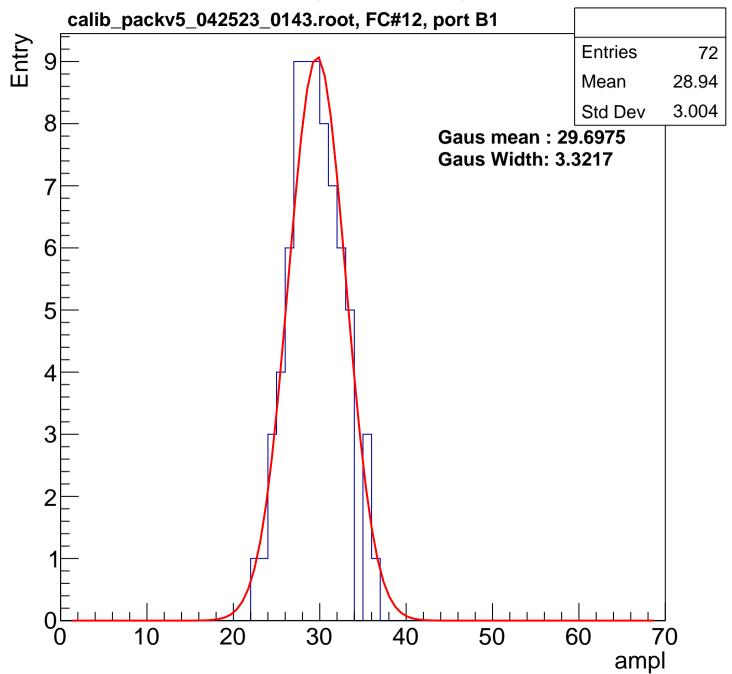


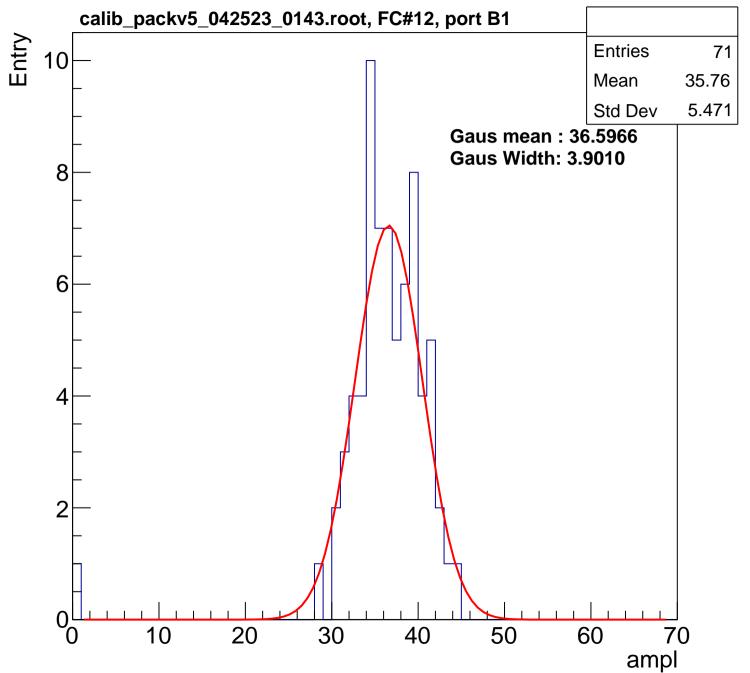


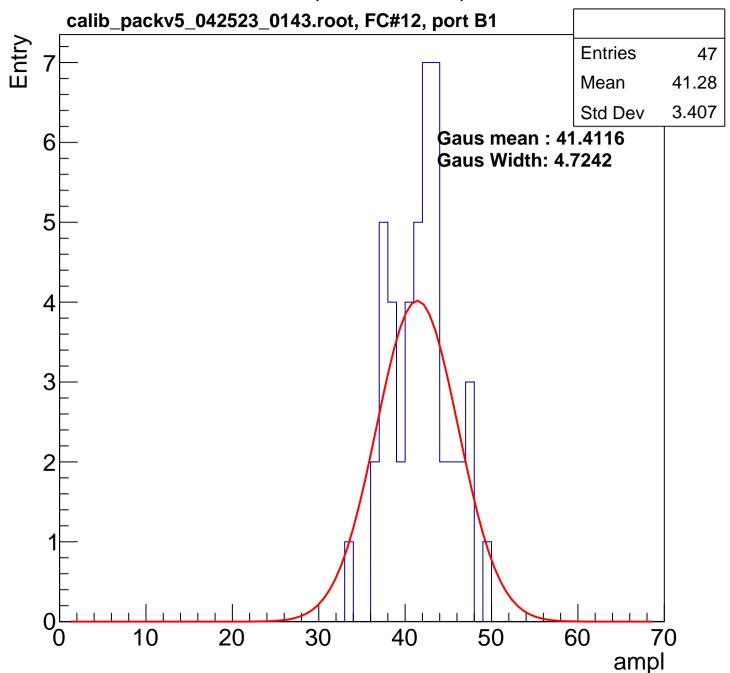


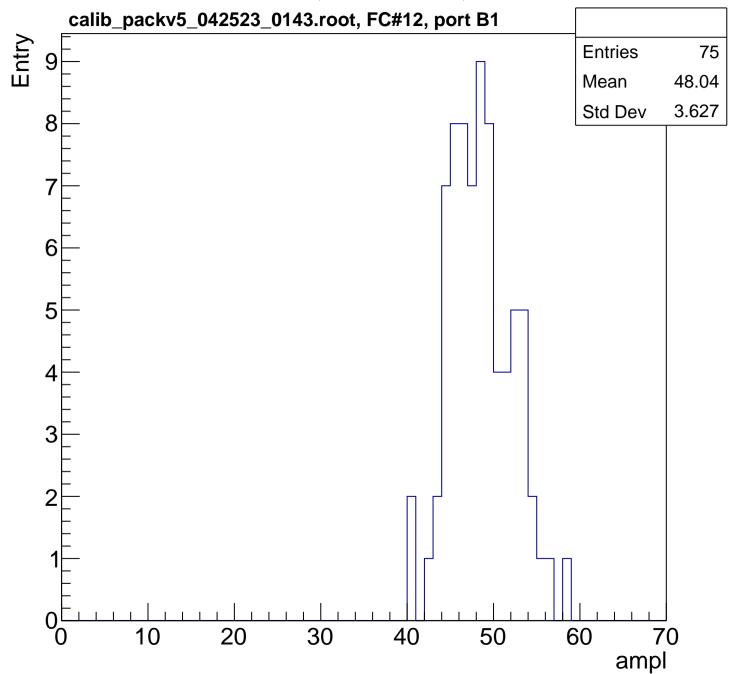
0

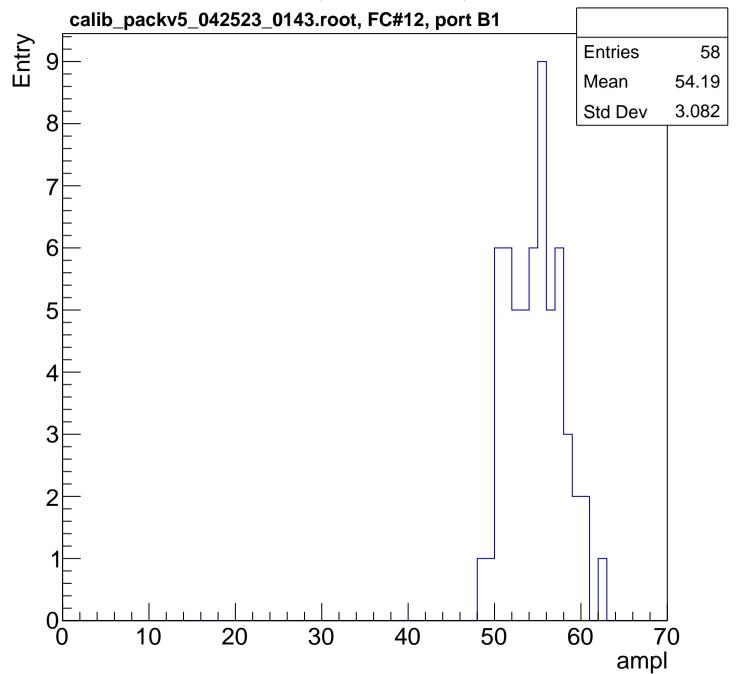


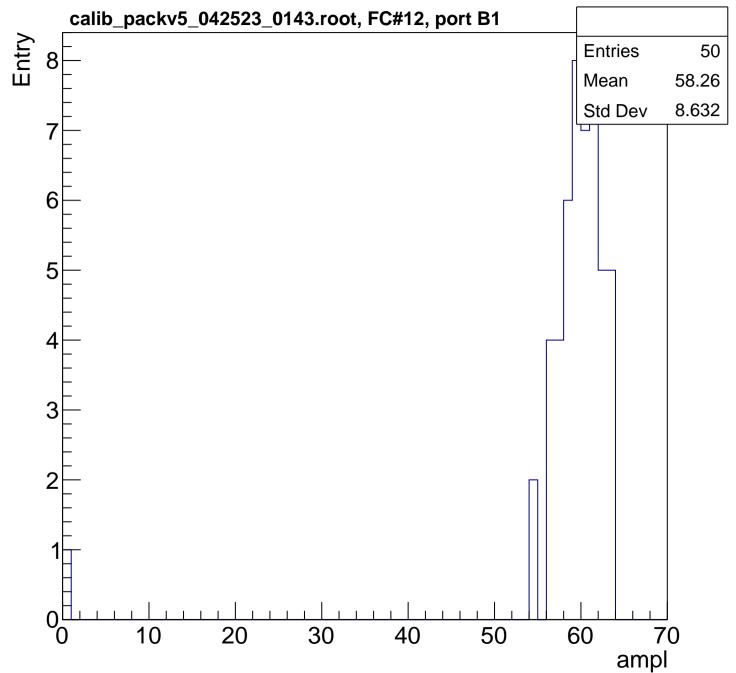


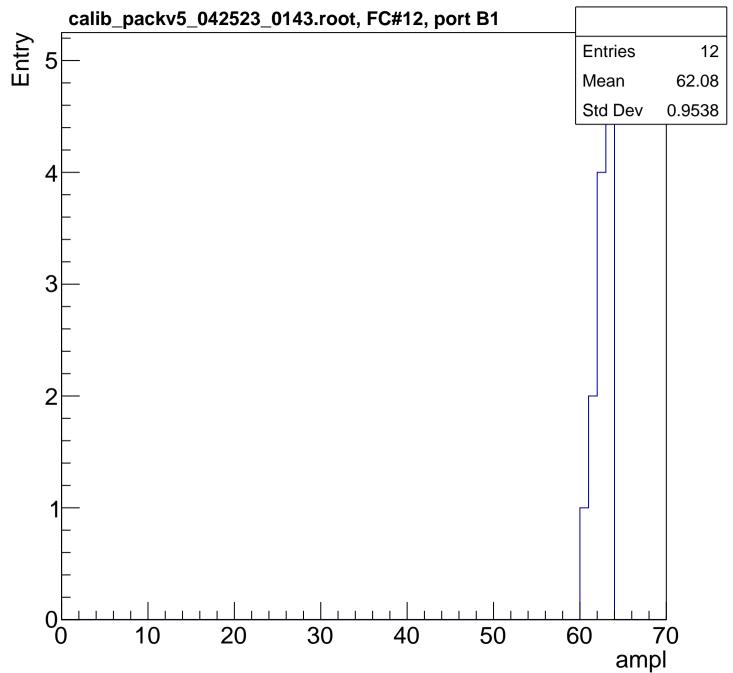


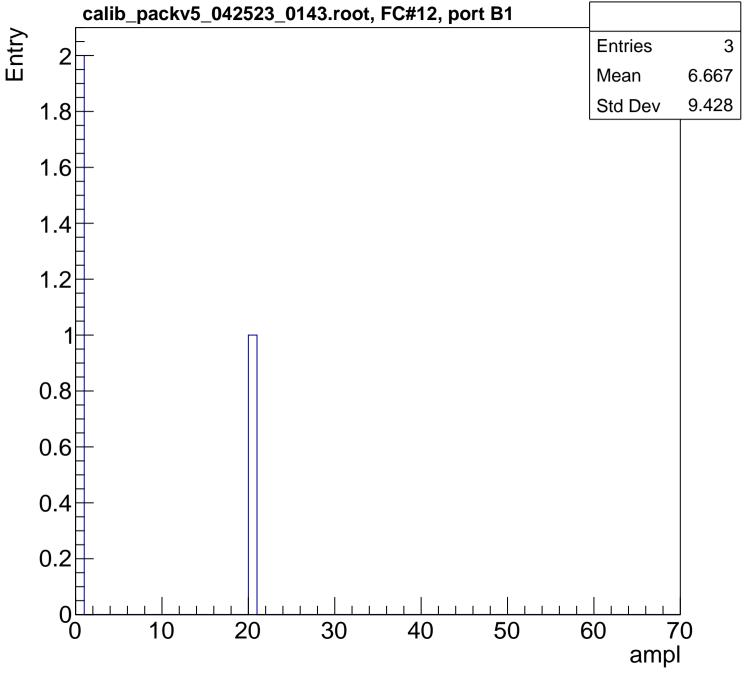


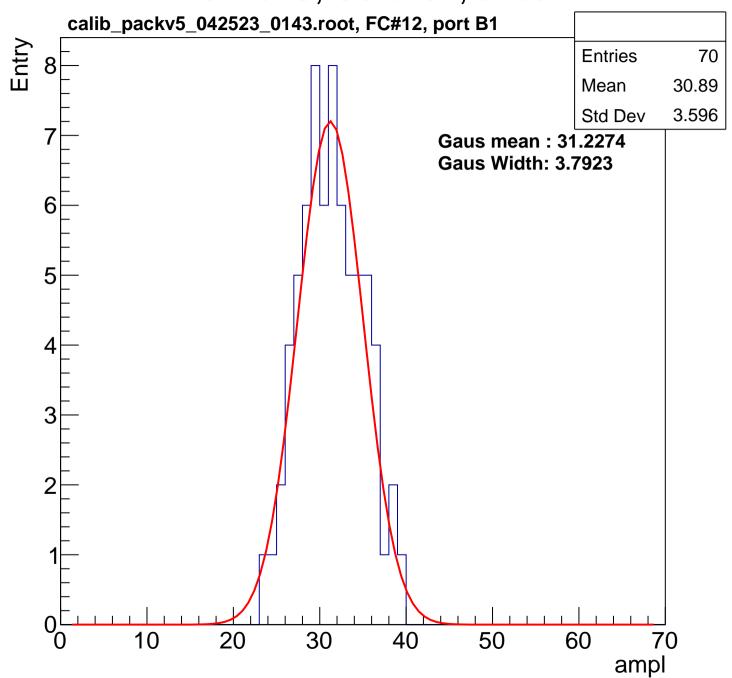


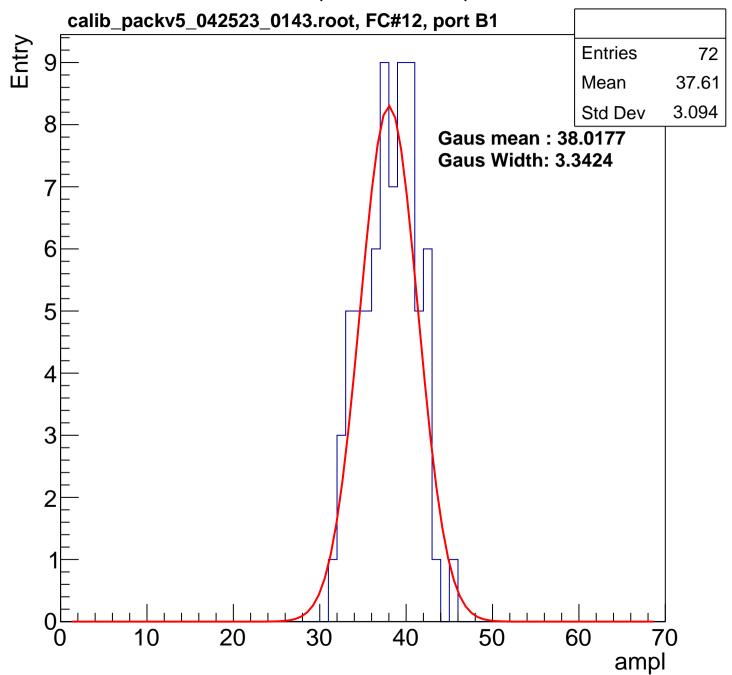


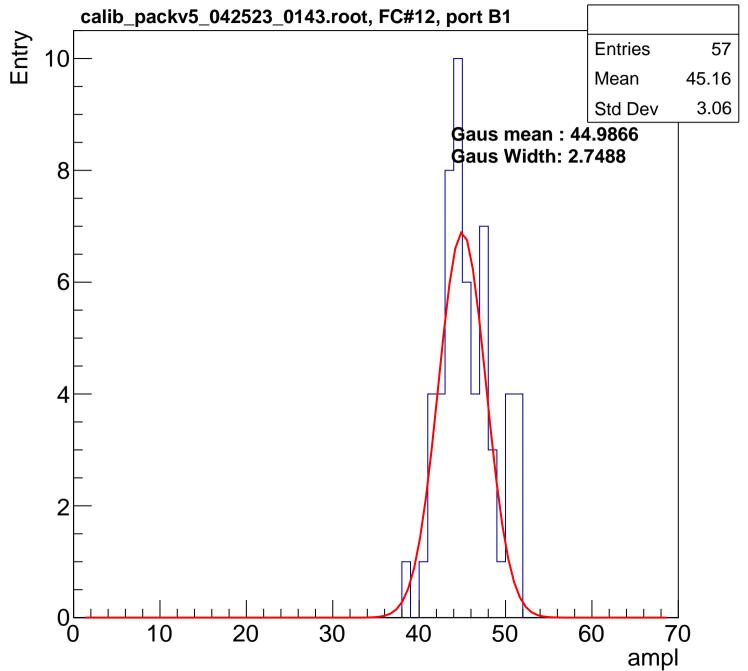


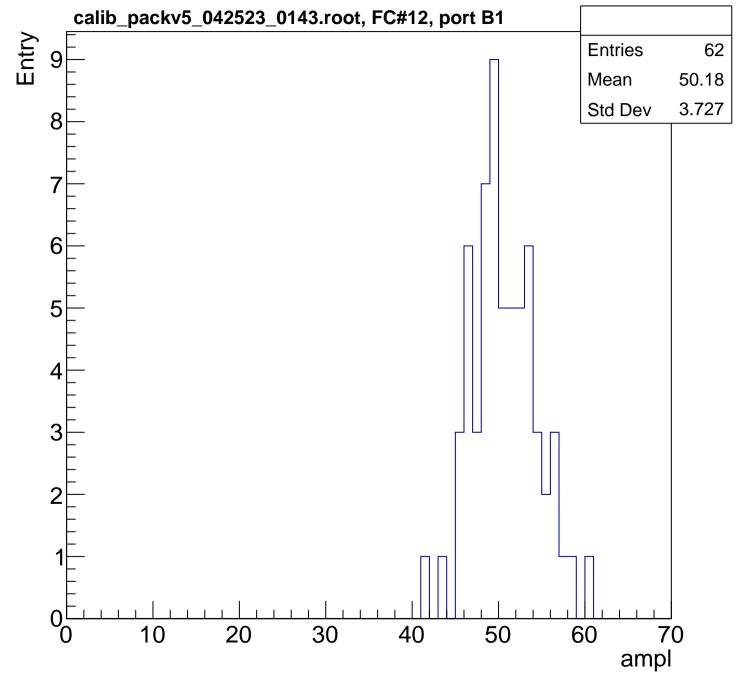


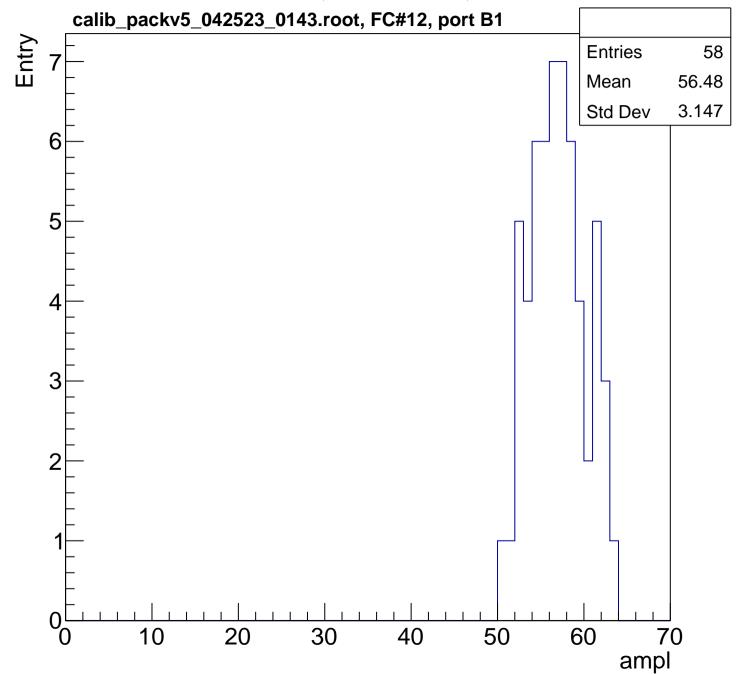


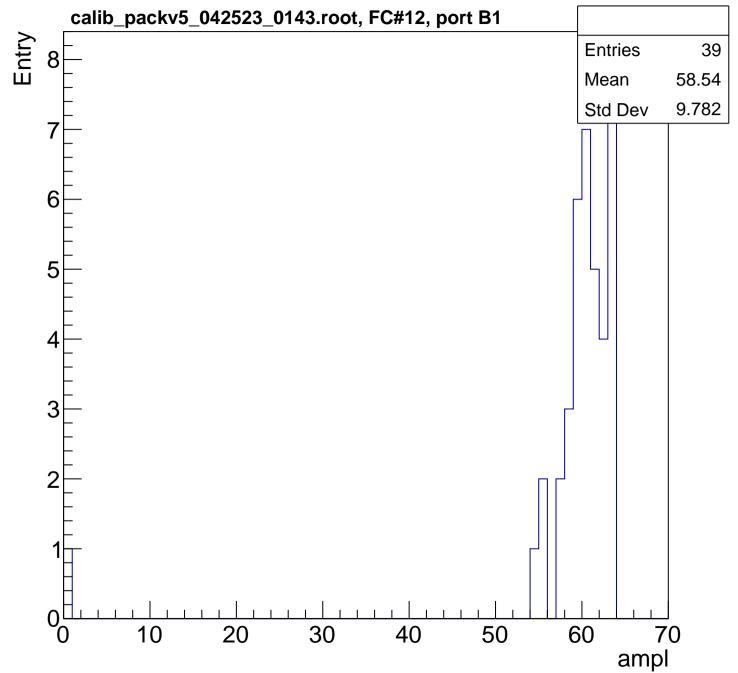


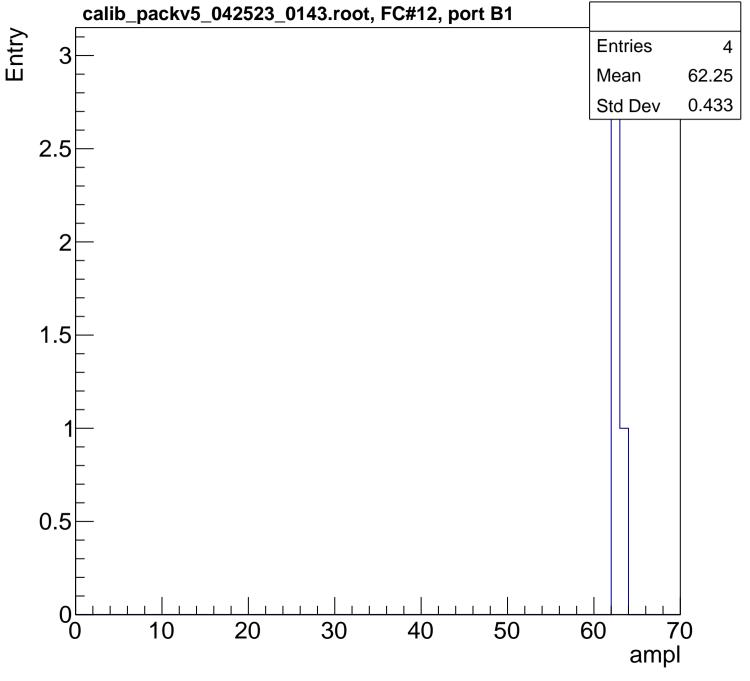


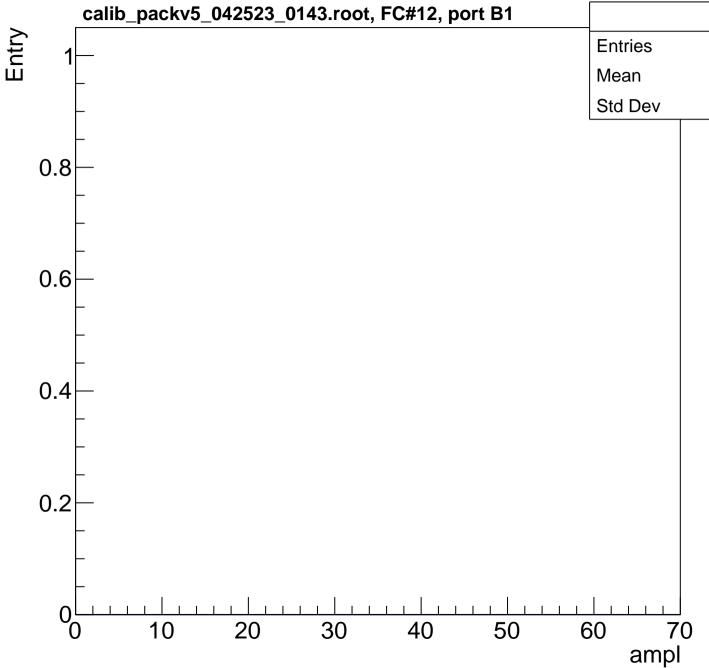


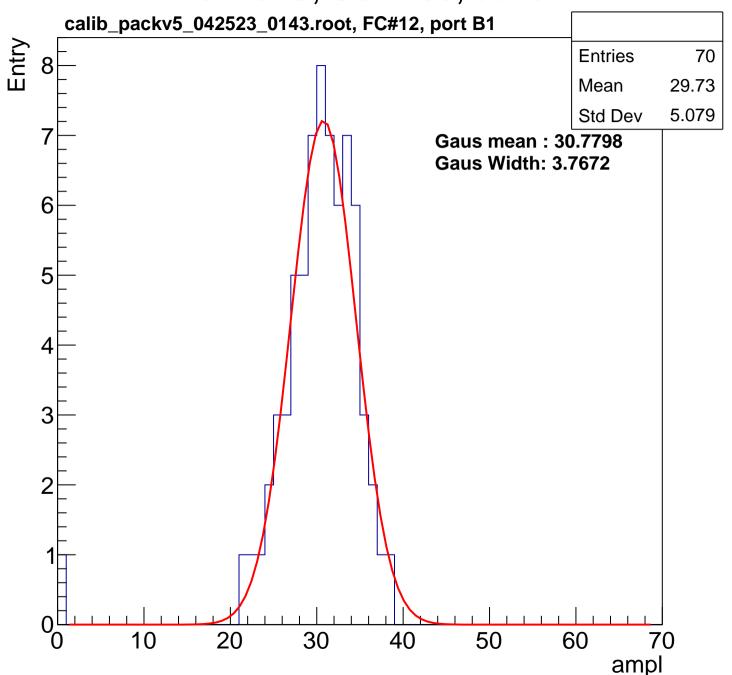


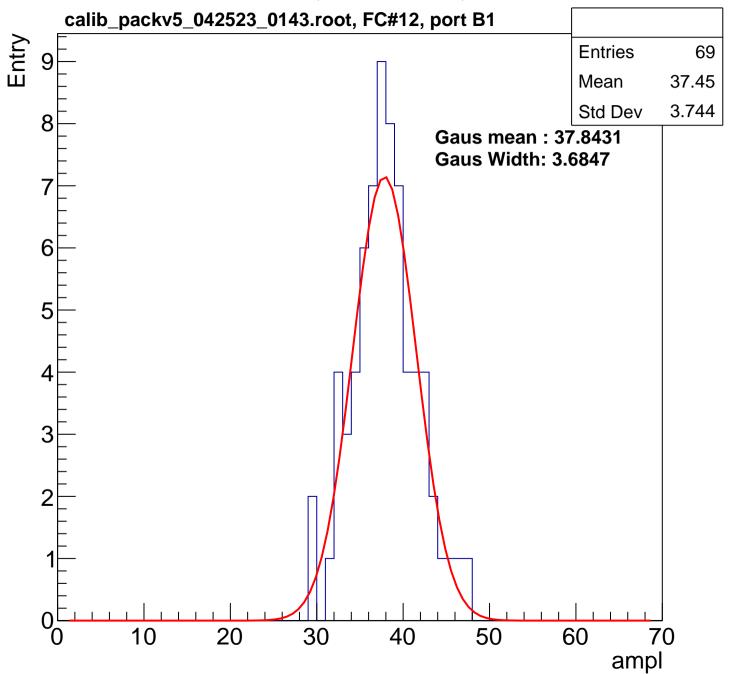


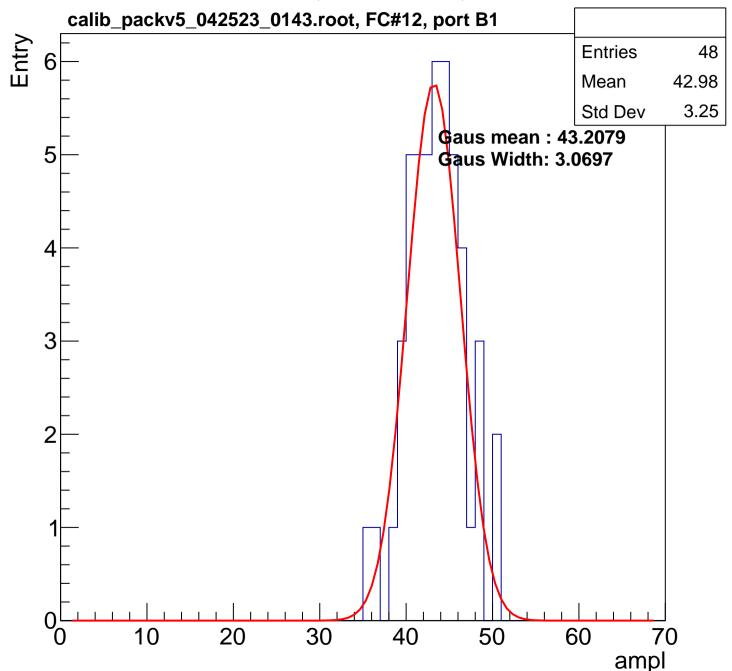


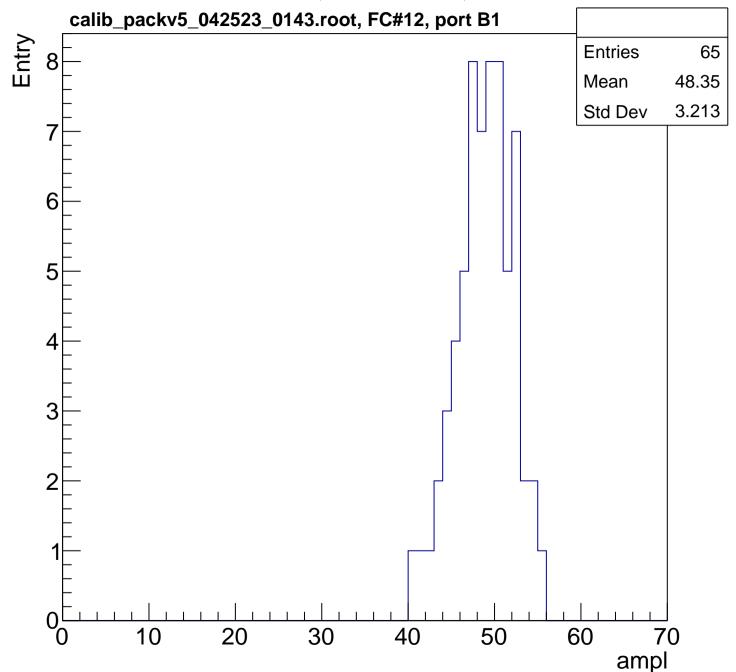


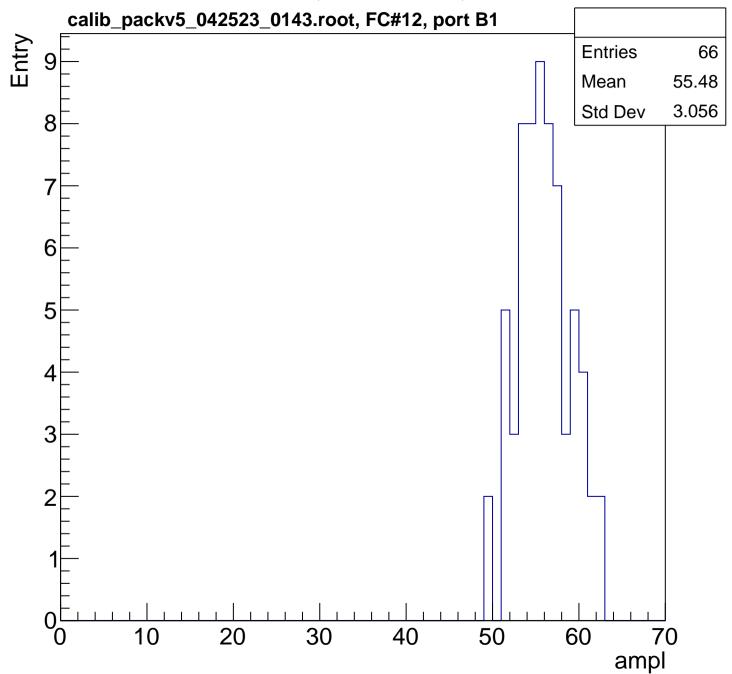


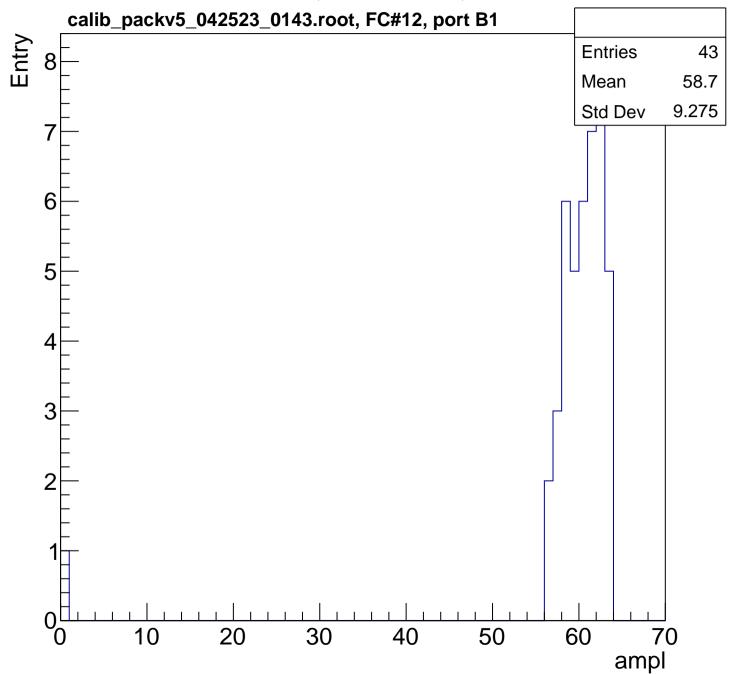


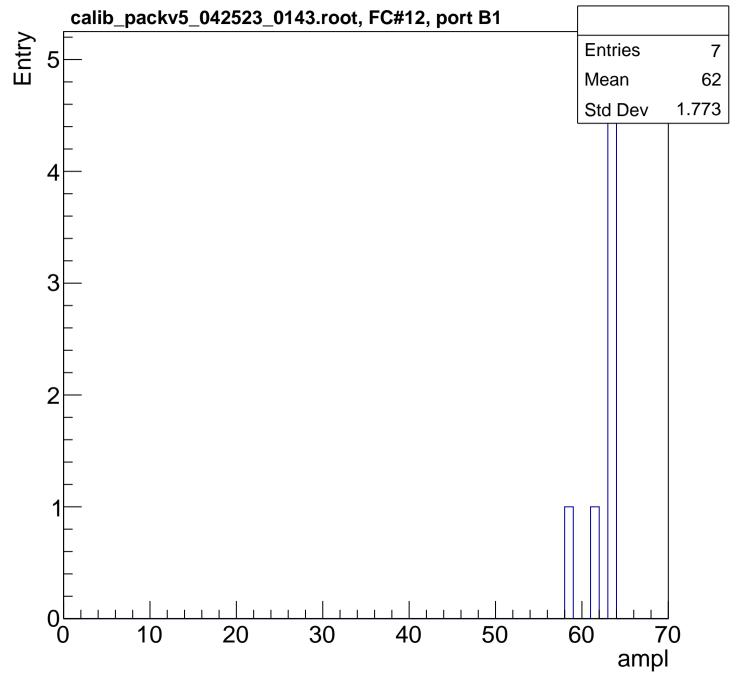


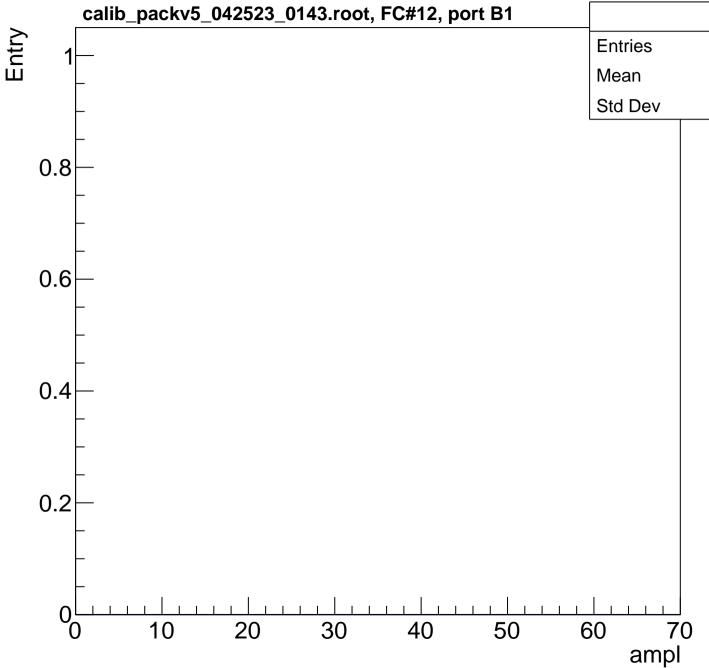


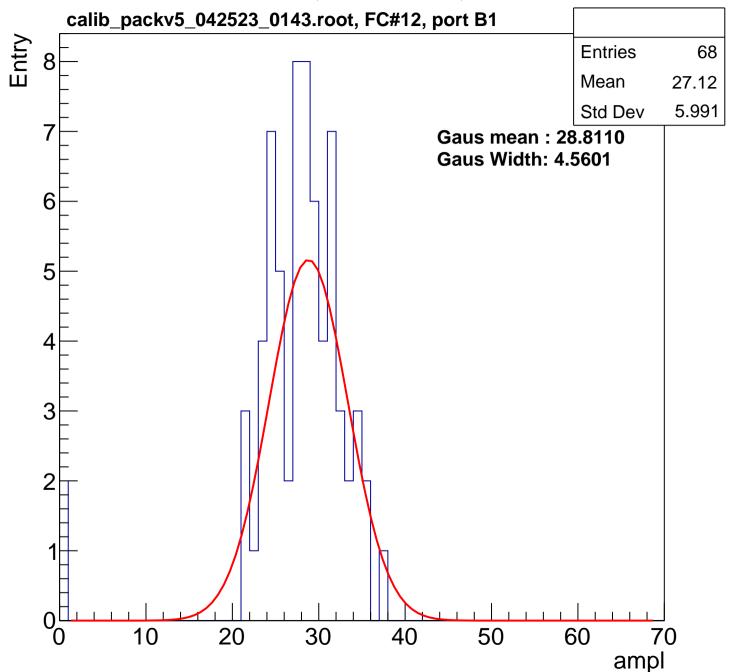


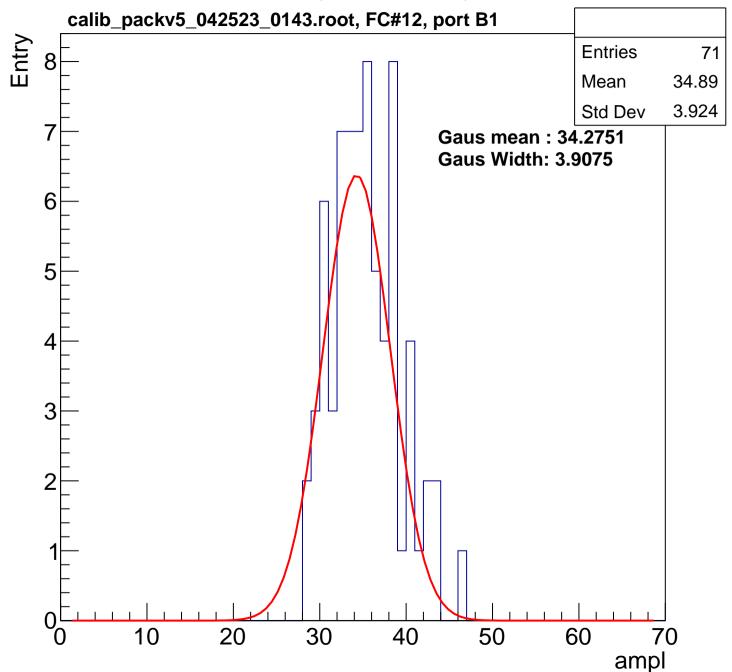


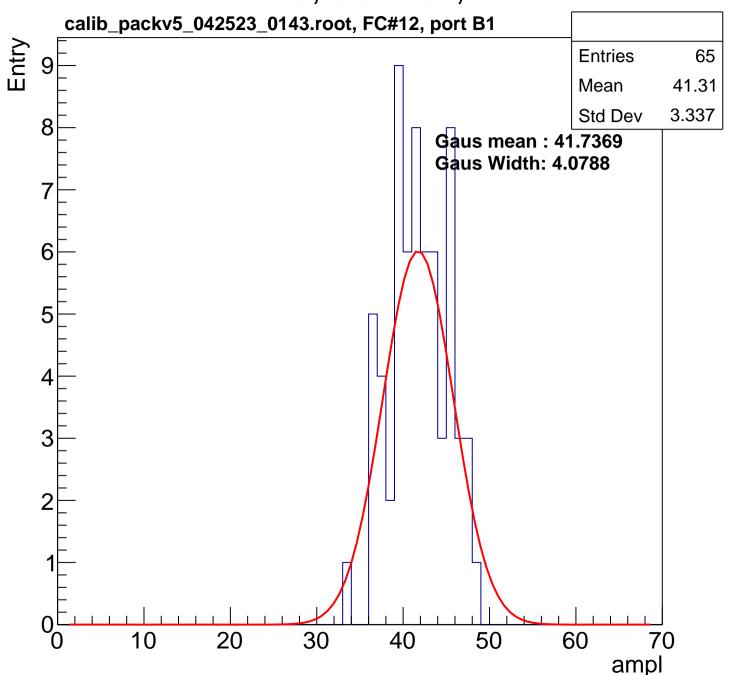


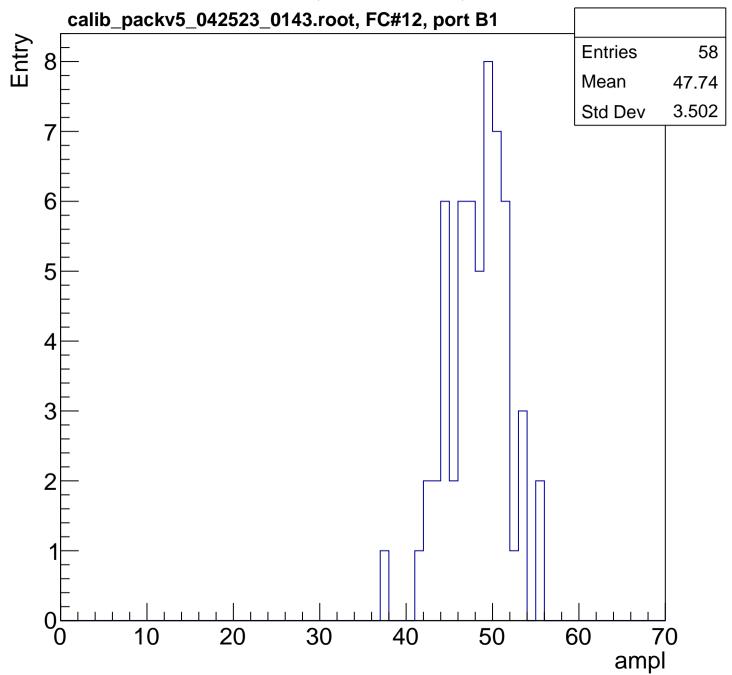


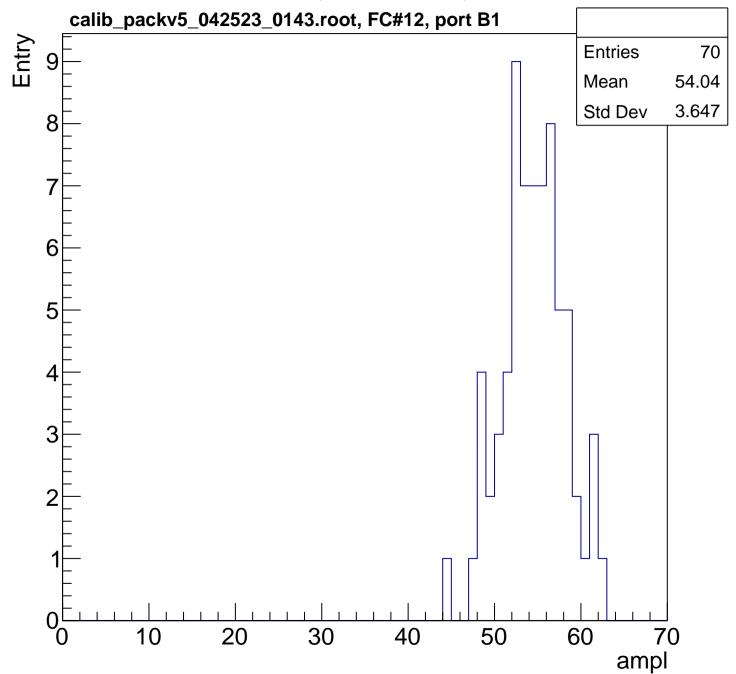


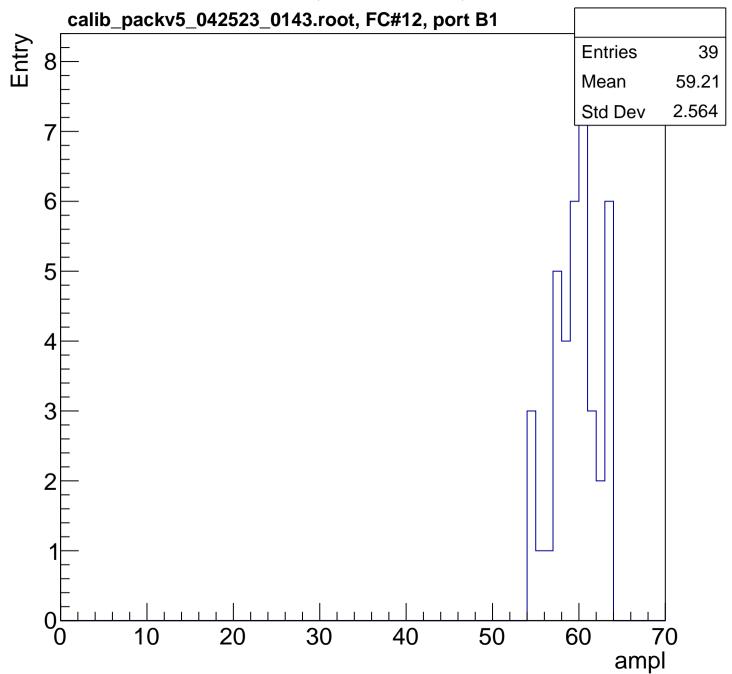


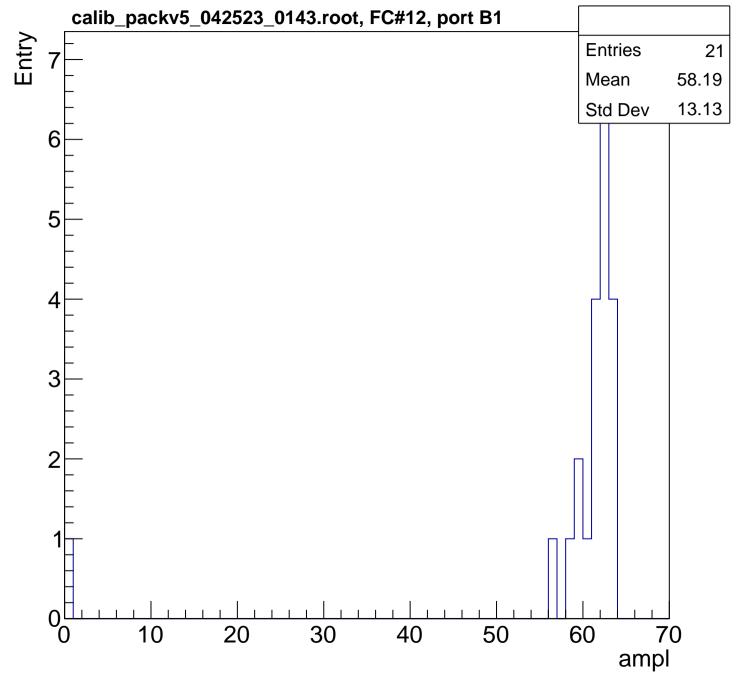


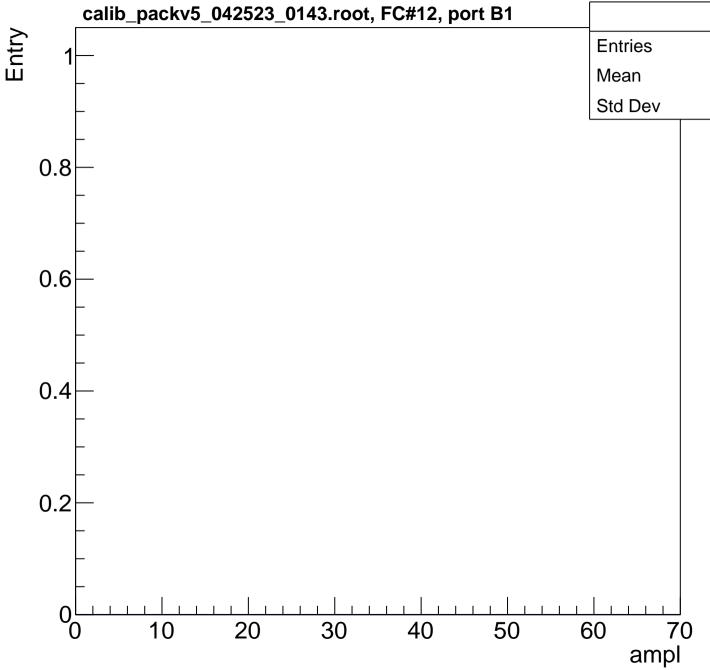


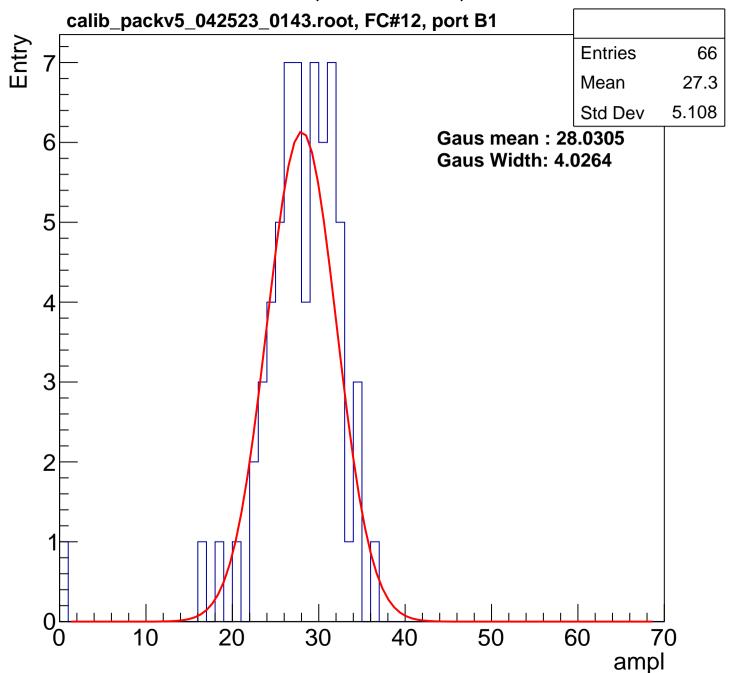


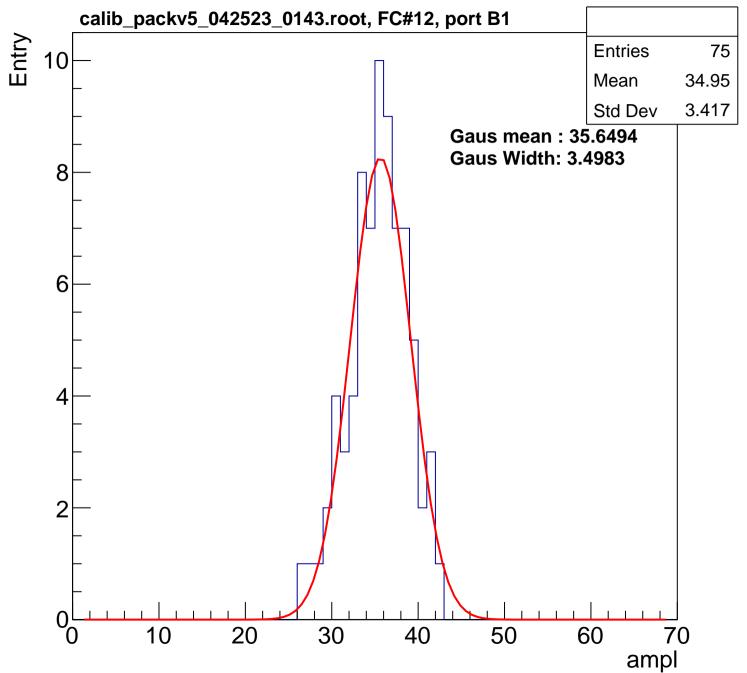


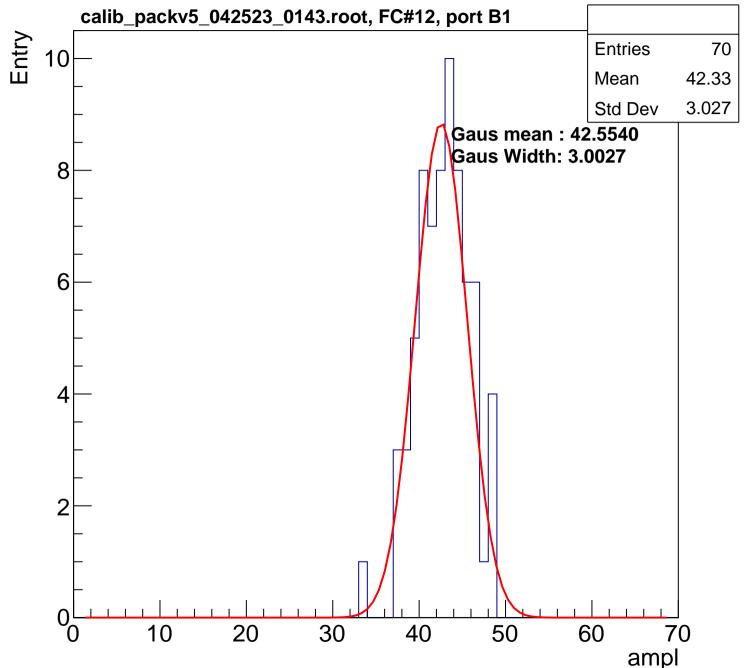


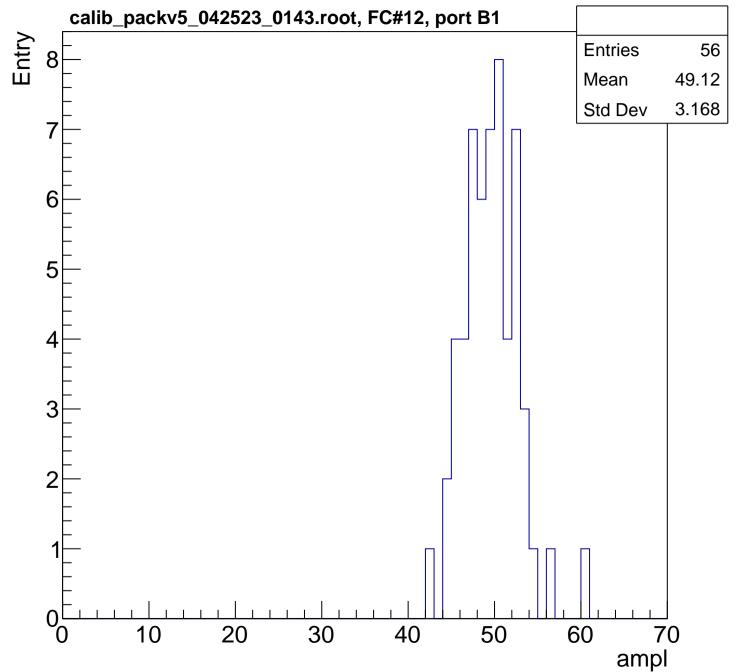


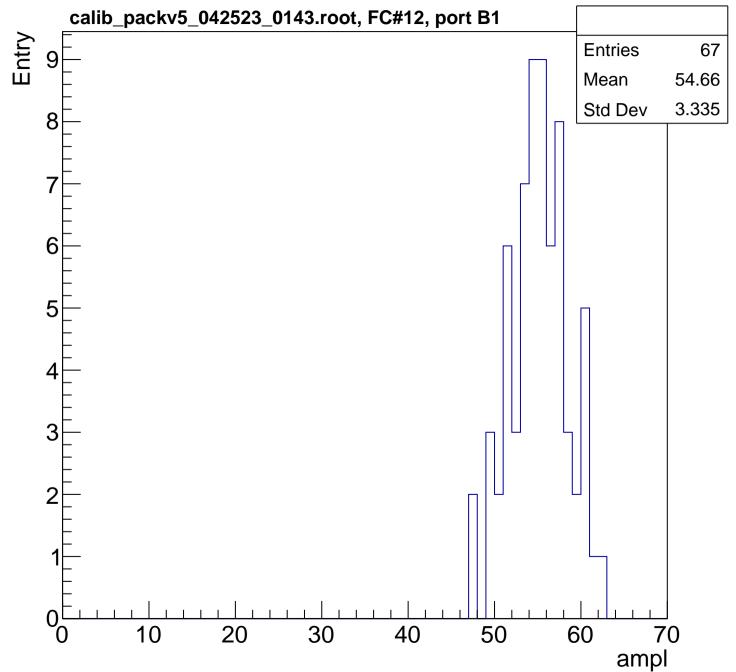


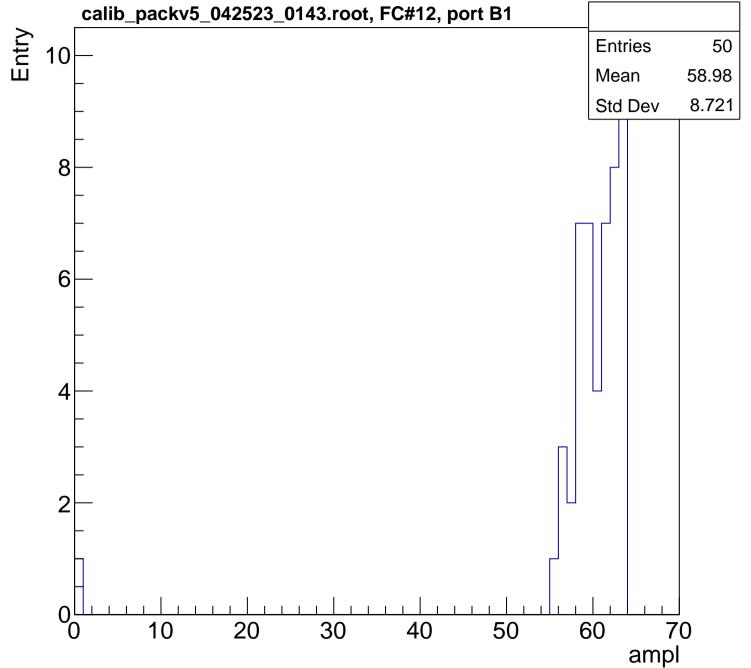


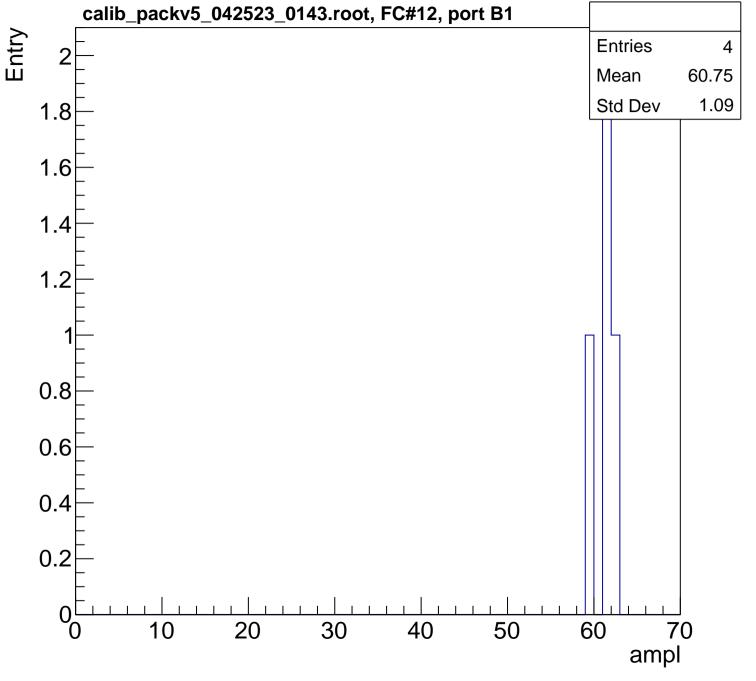




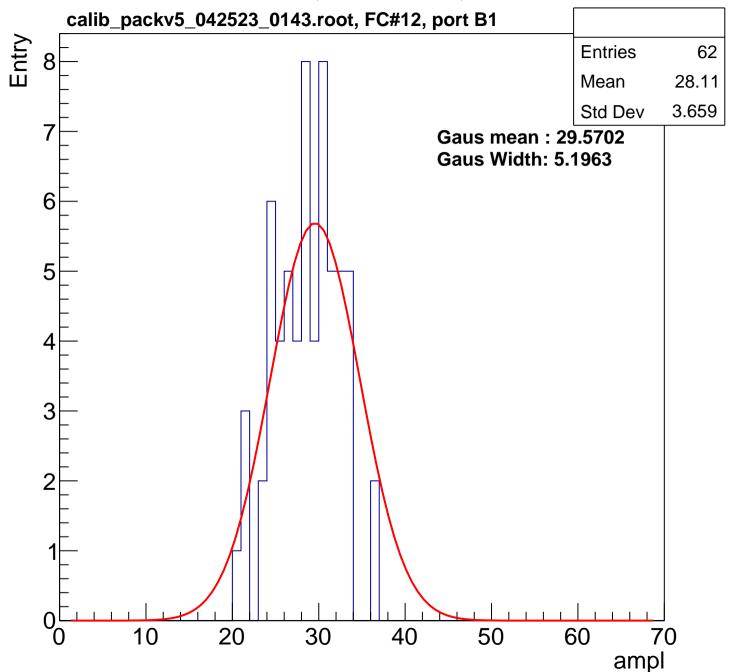


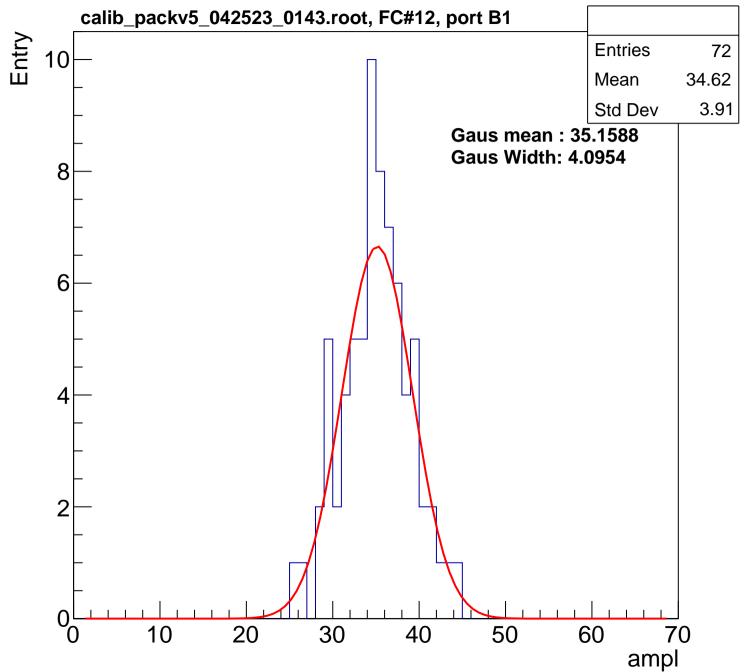


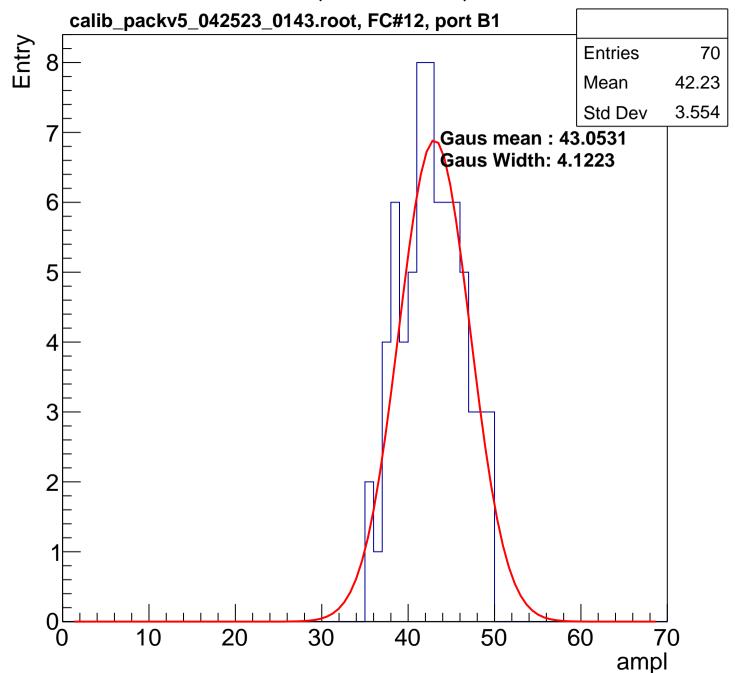


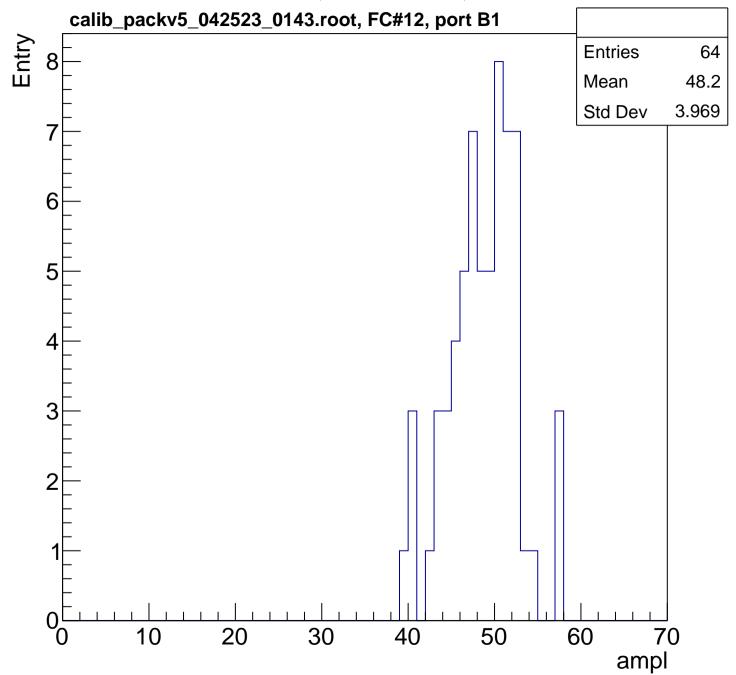


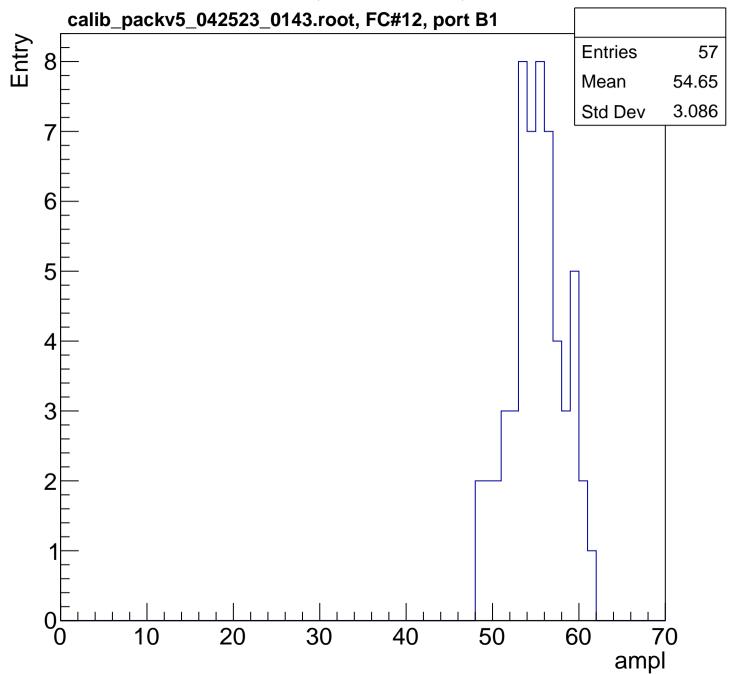
B0L102S, U3-ch35, adc7 calib_packv5_042523_0143.root, FC#12, port B1 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

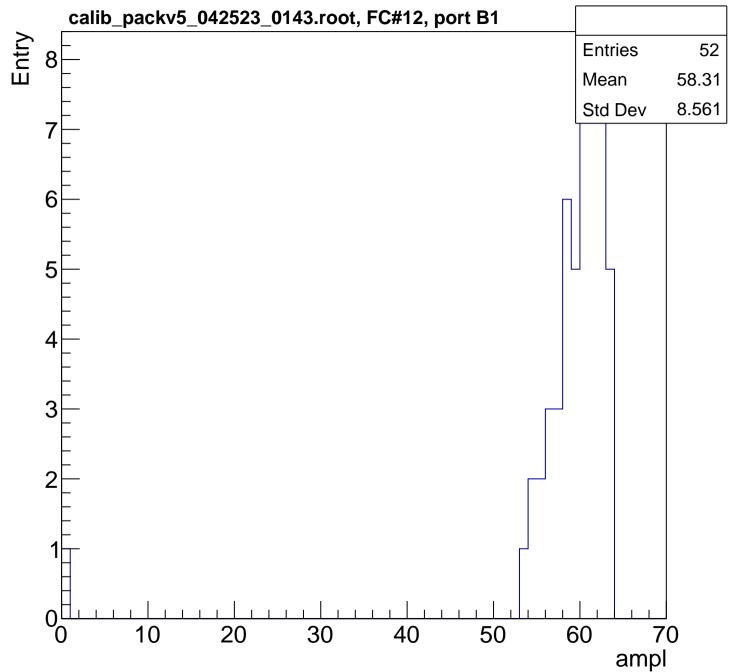


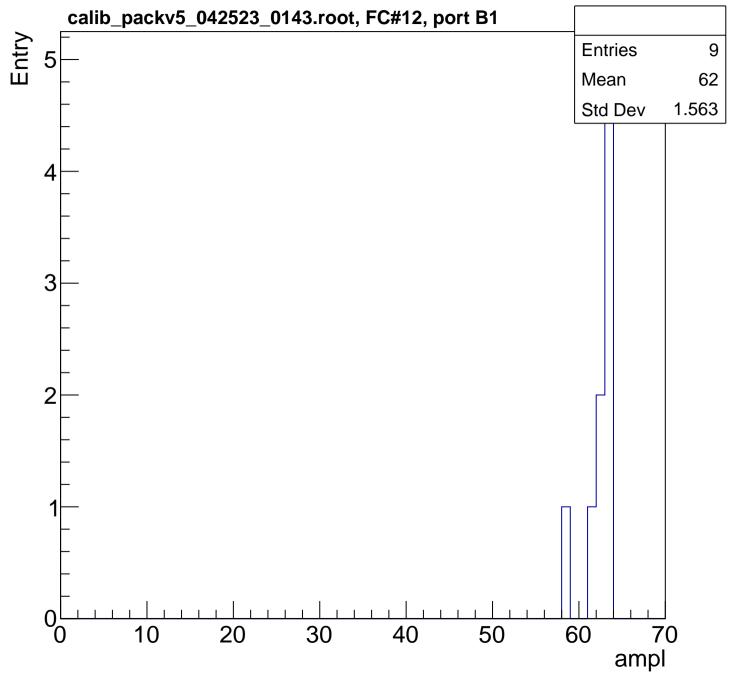


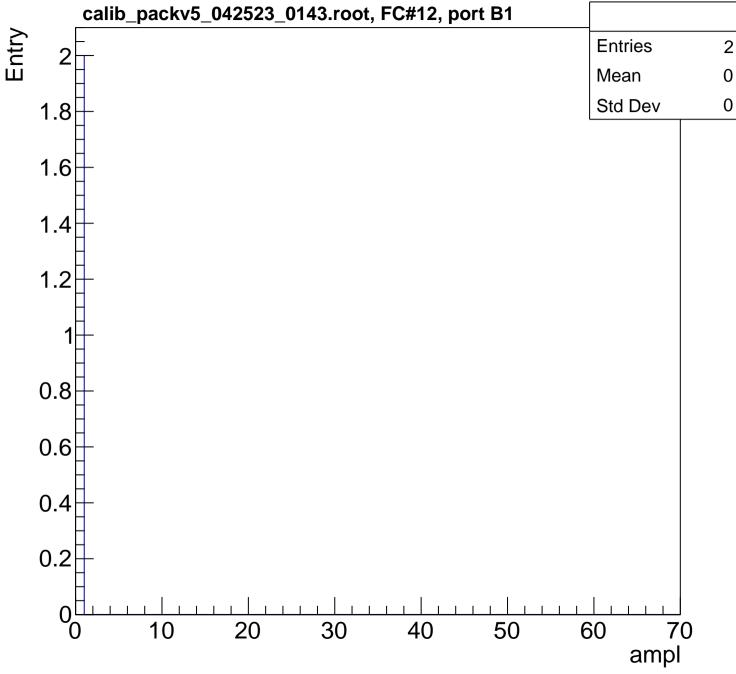


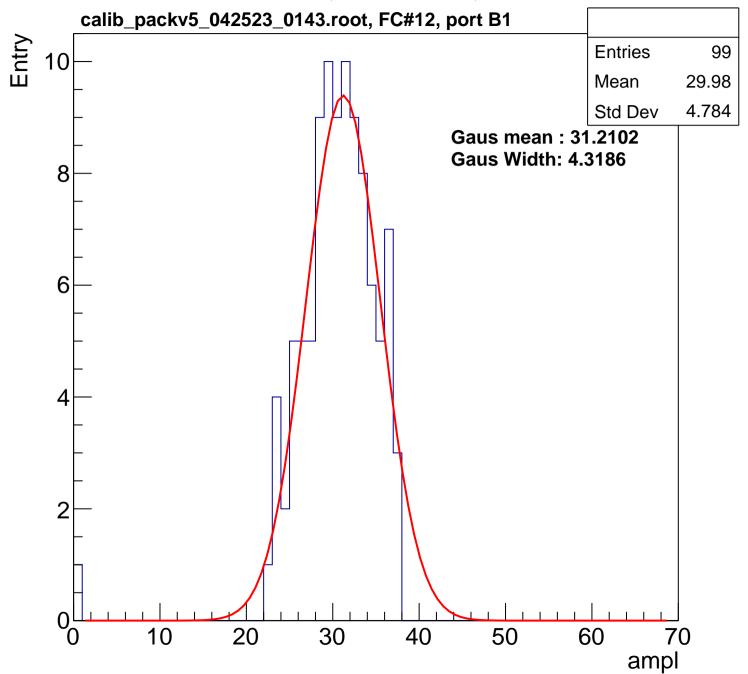


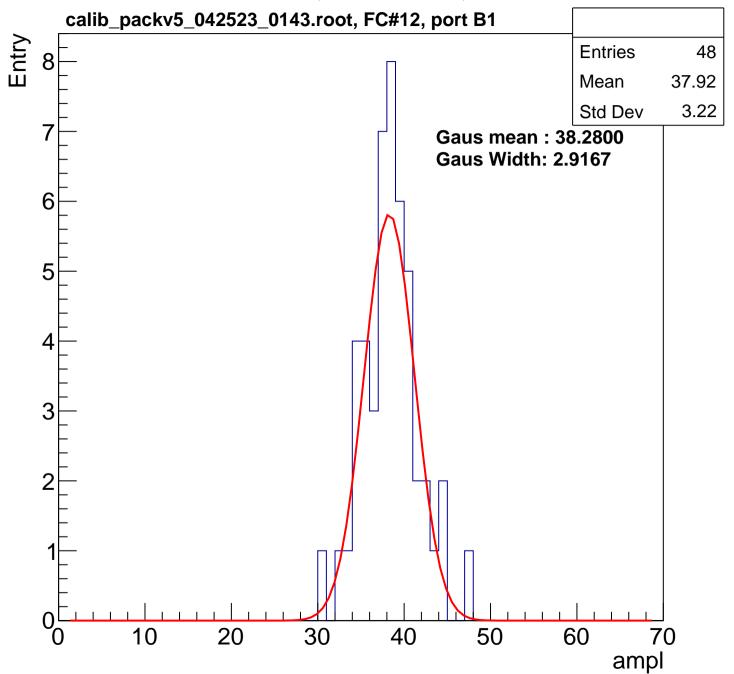


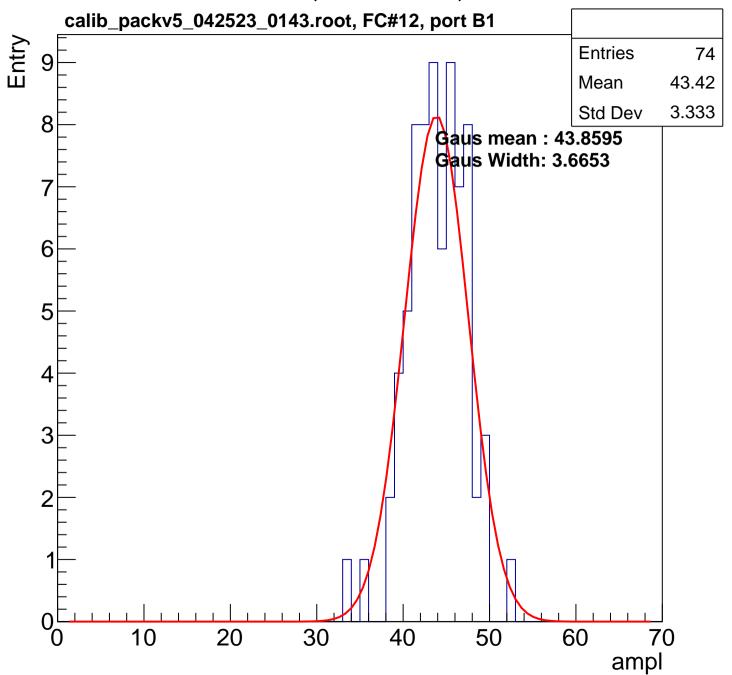


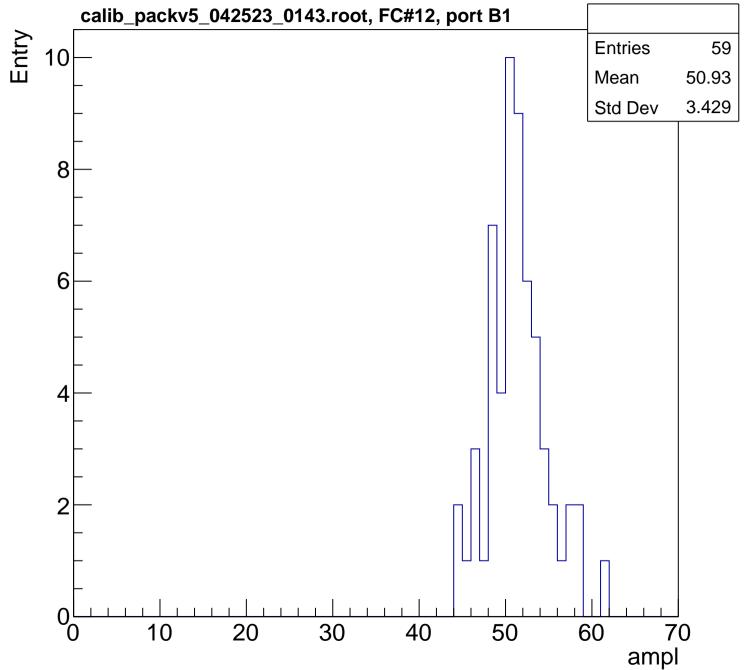


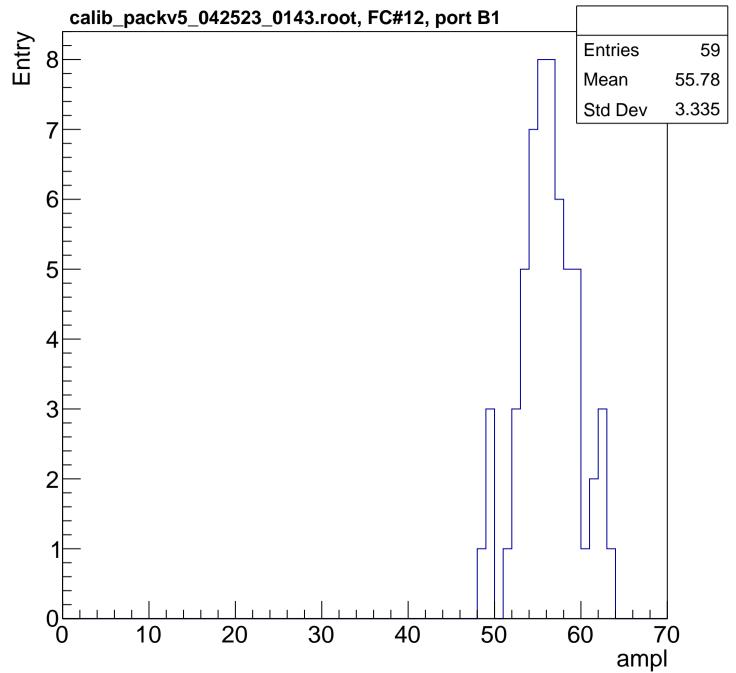


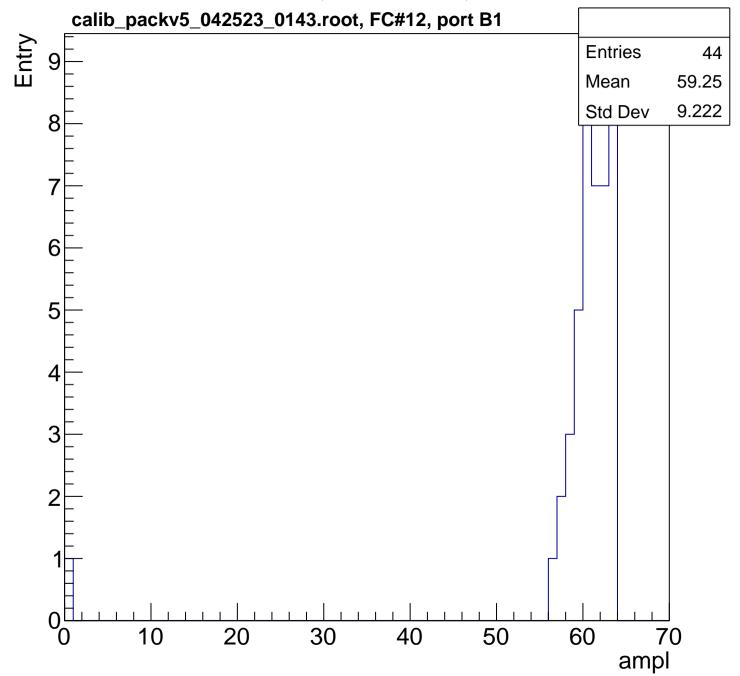


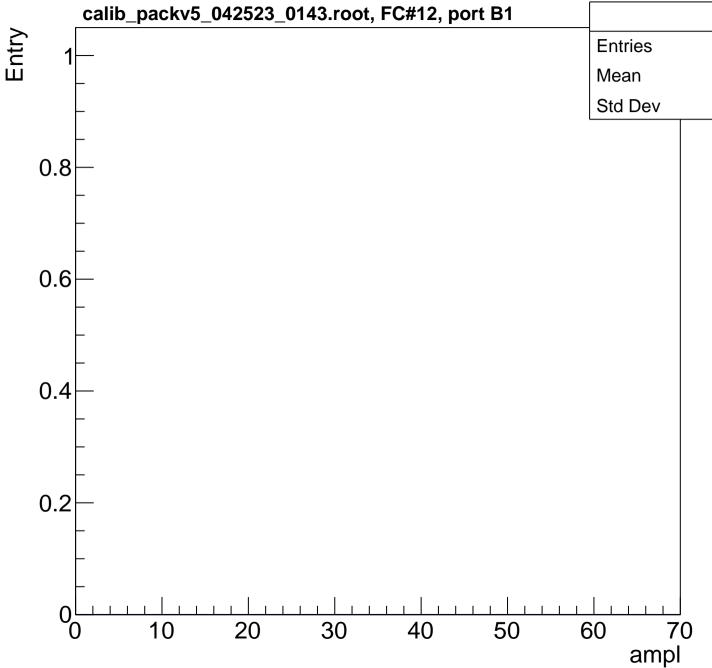


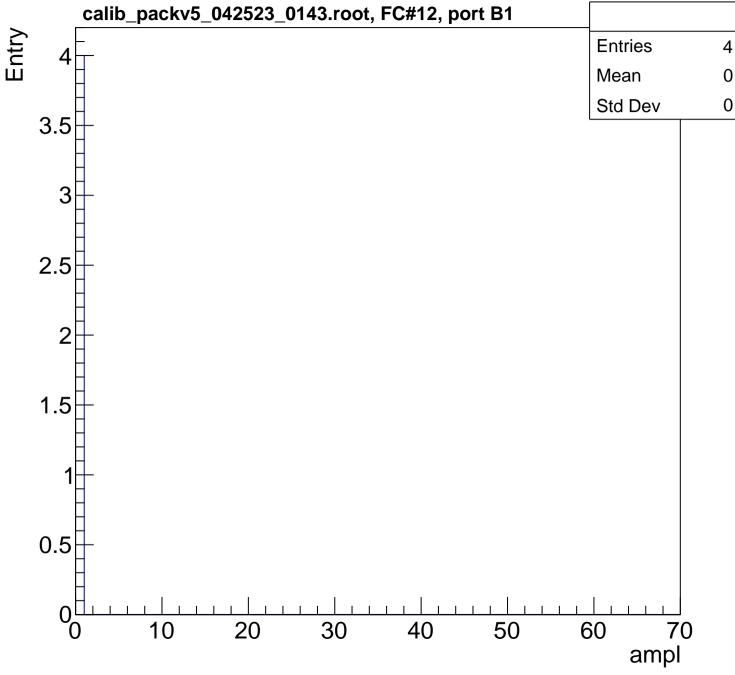


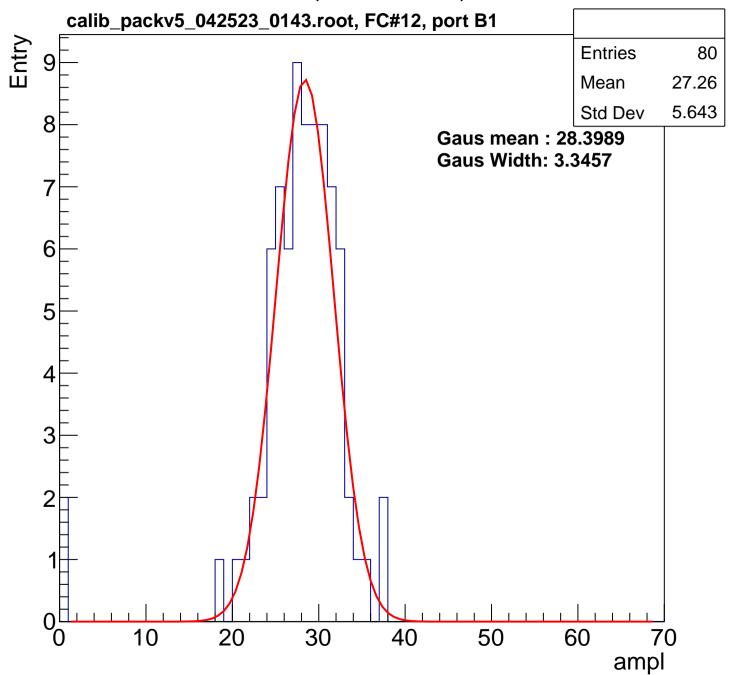


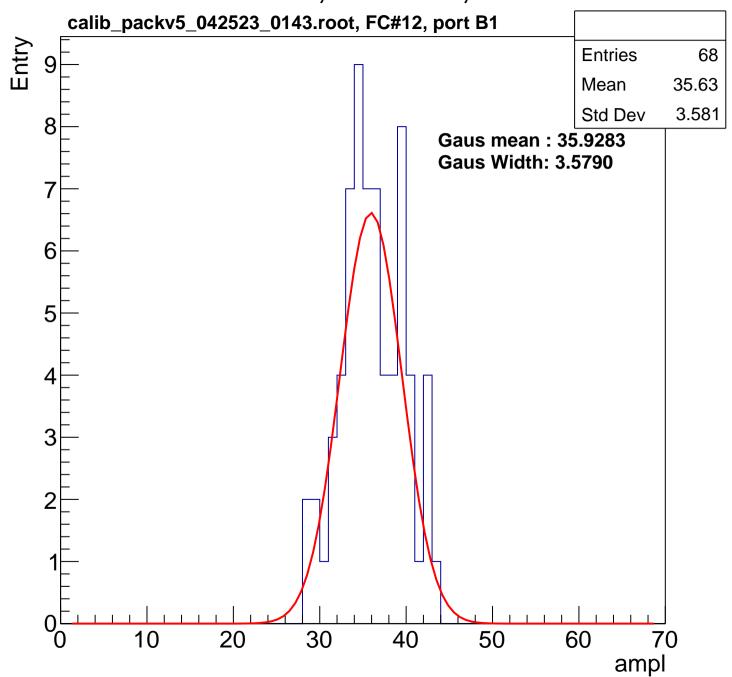


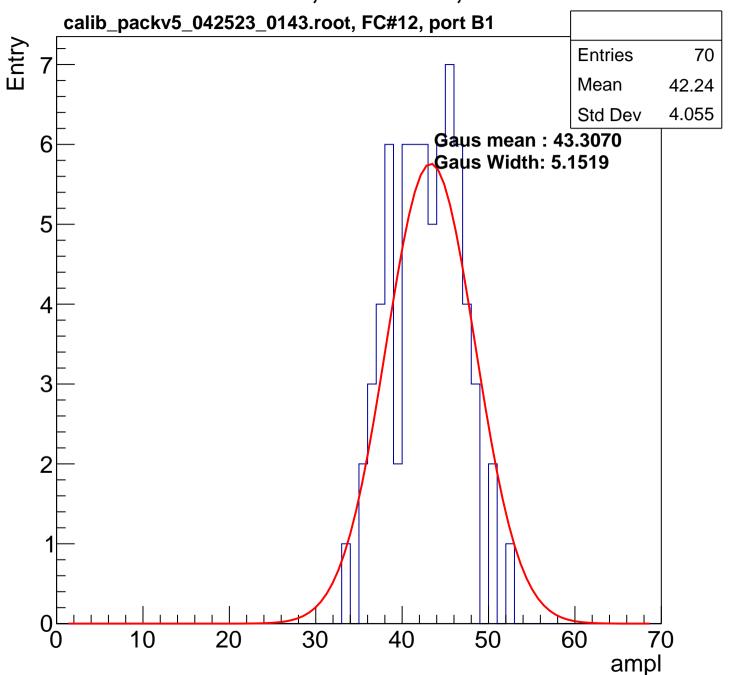


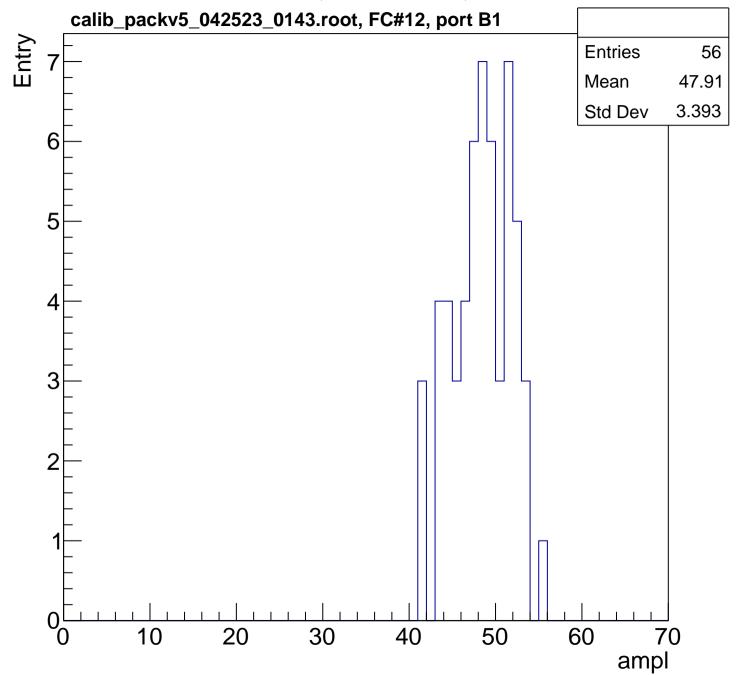


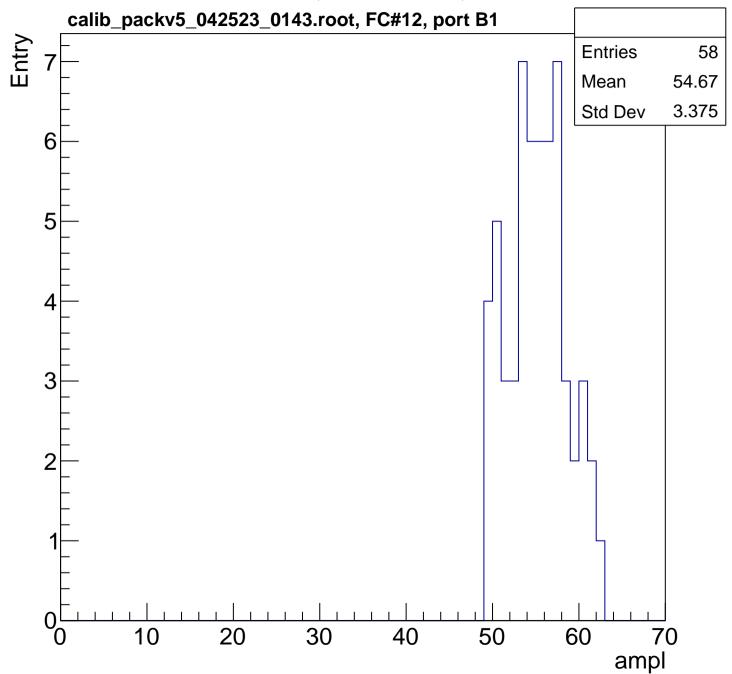


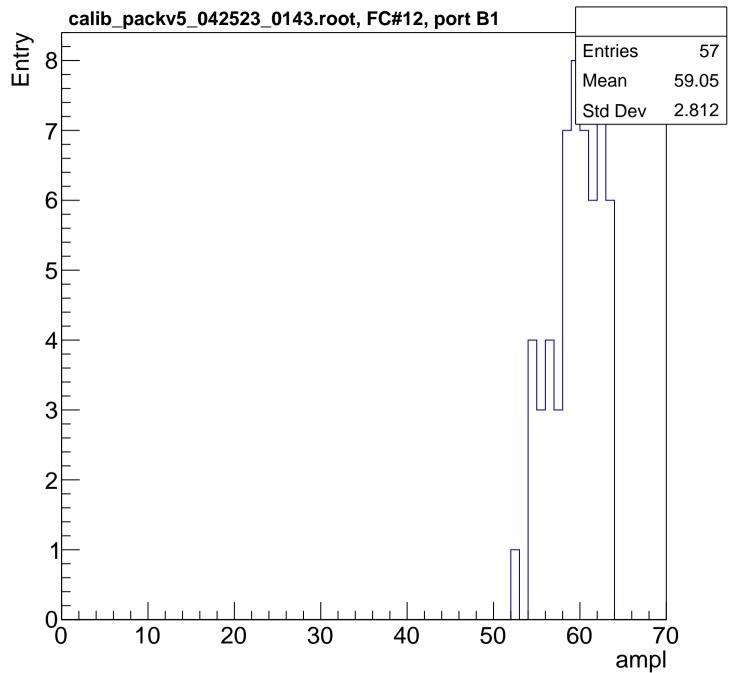


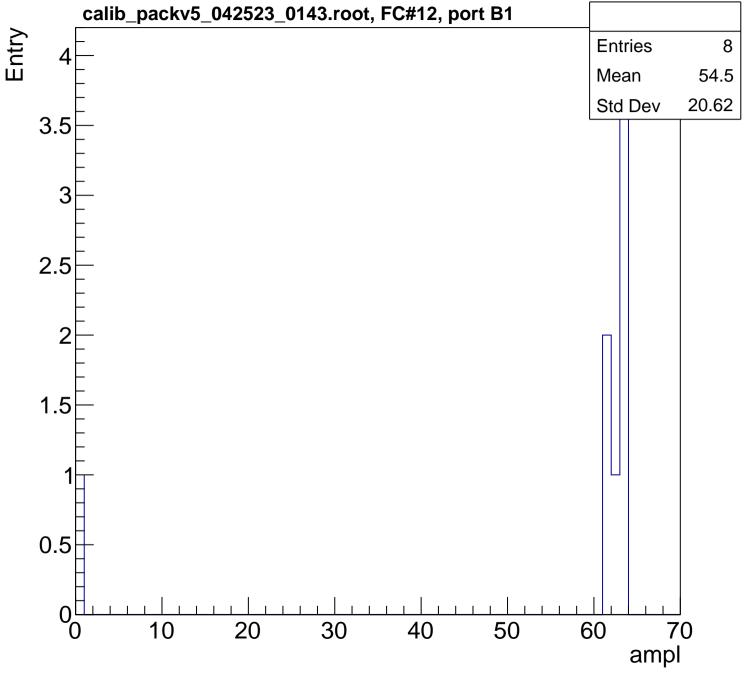




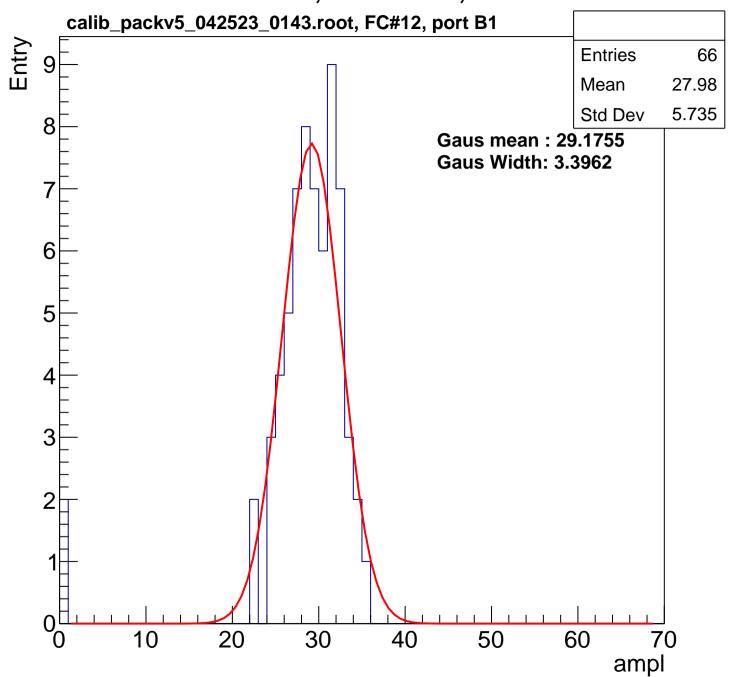


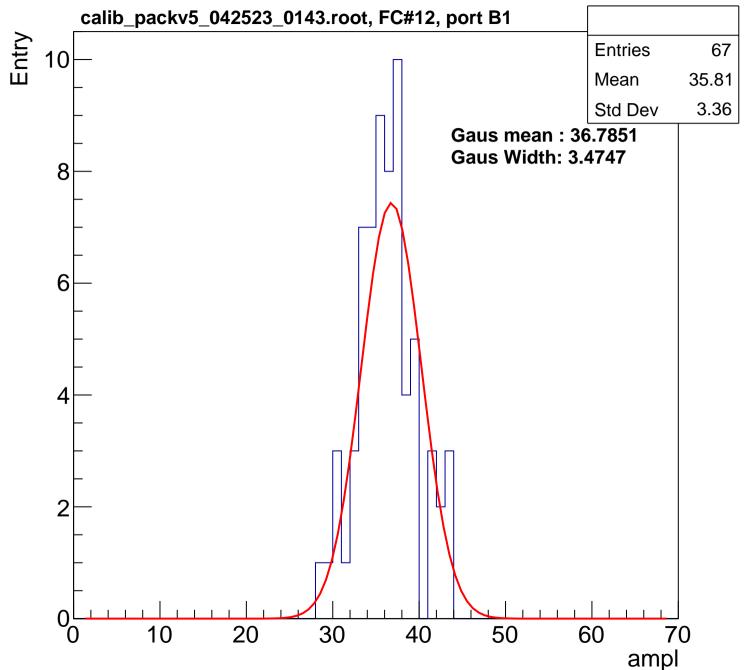


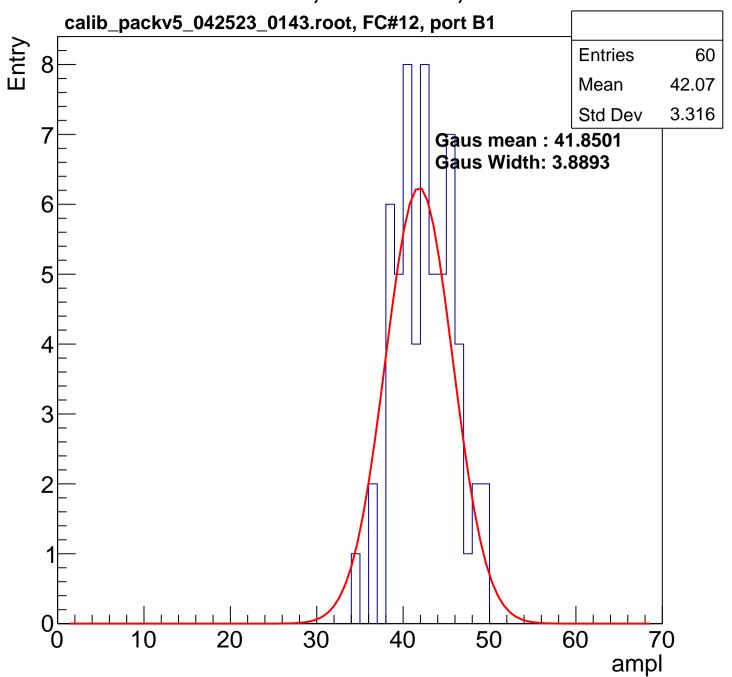


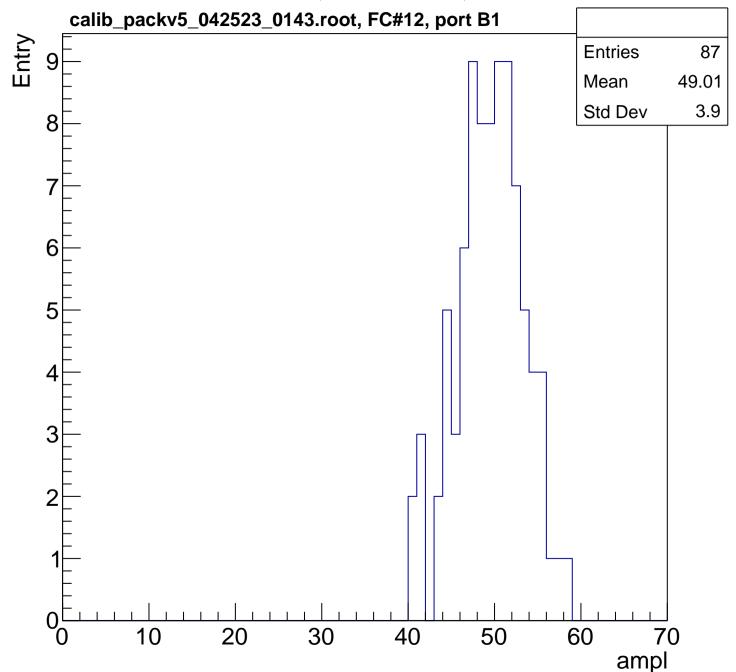


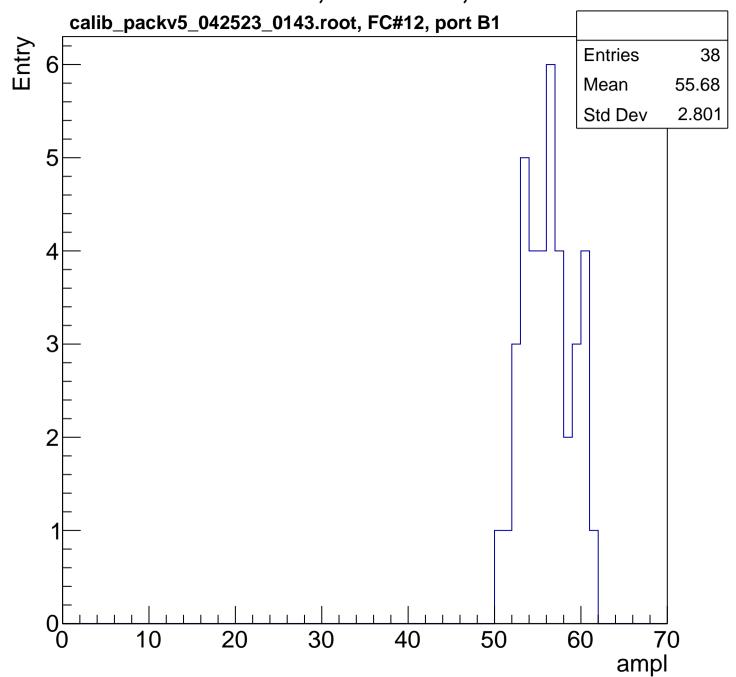
B0L102S, U3-ch38, adc7 calib_packv5_042523_0143.root, FC#12, port B1 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

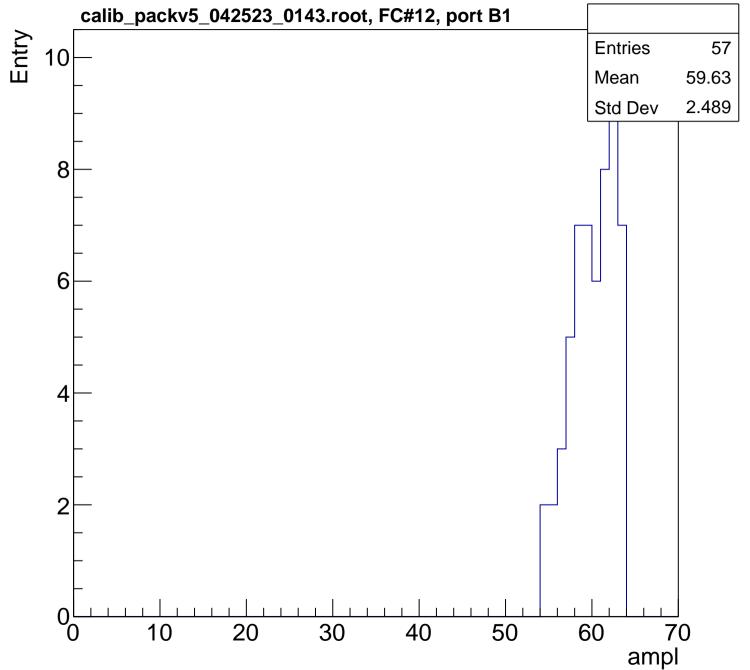


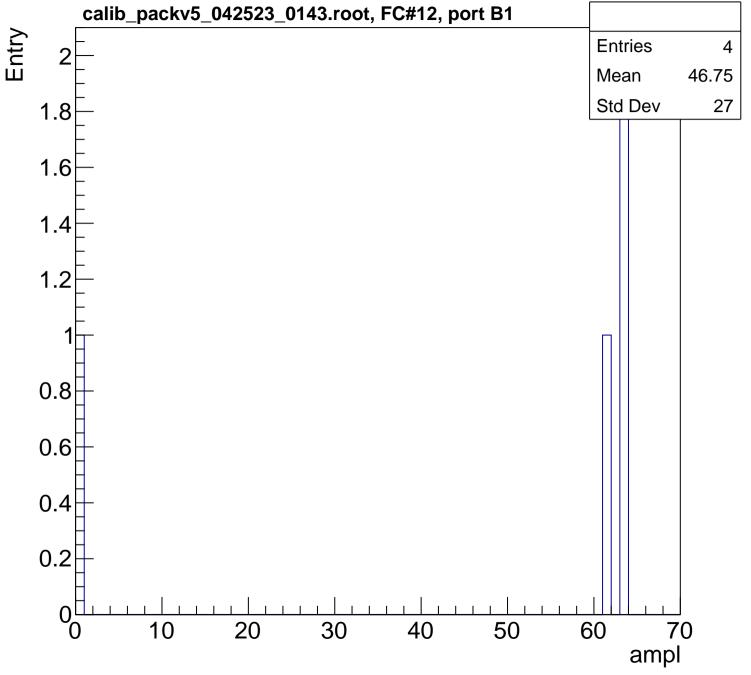


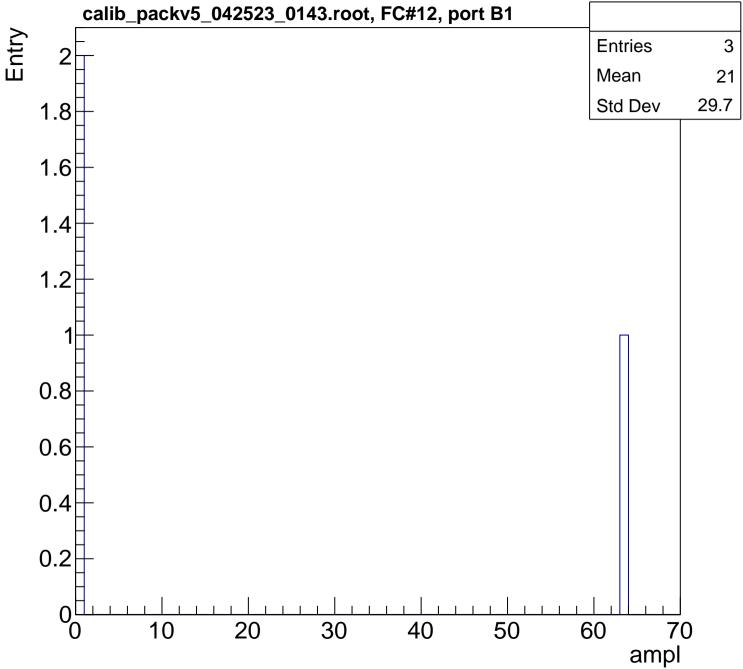


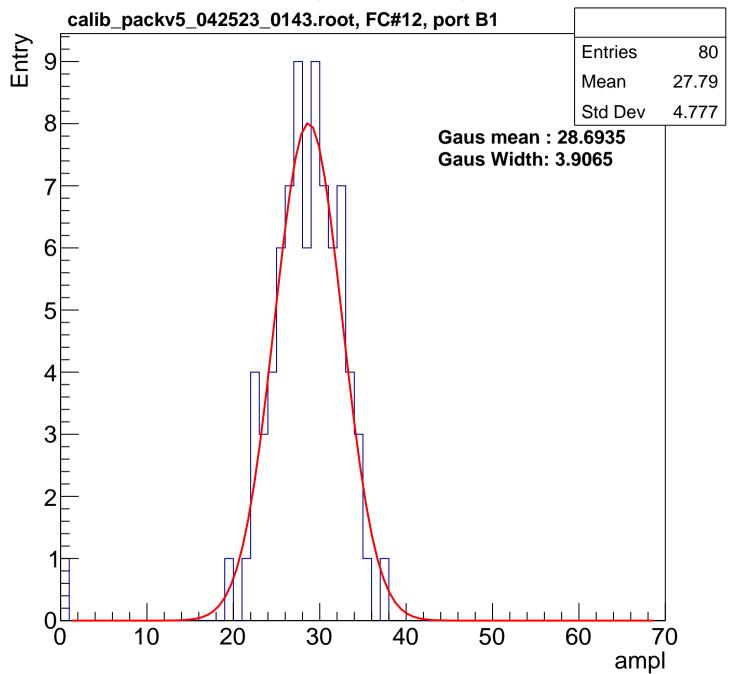


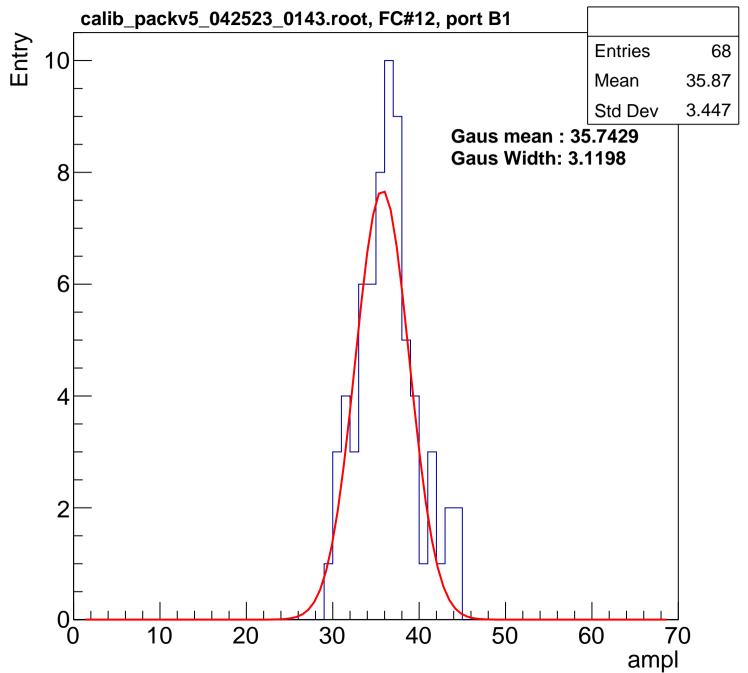


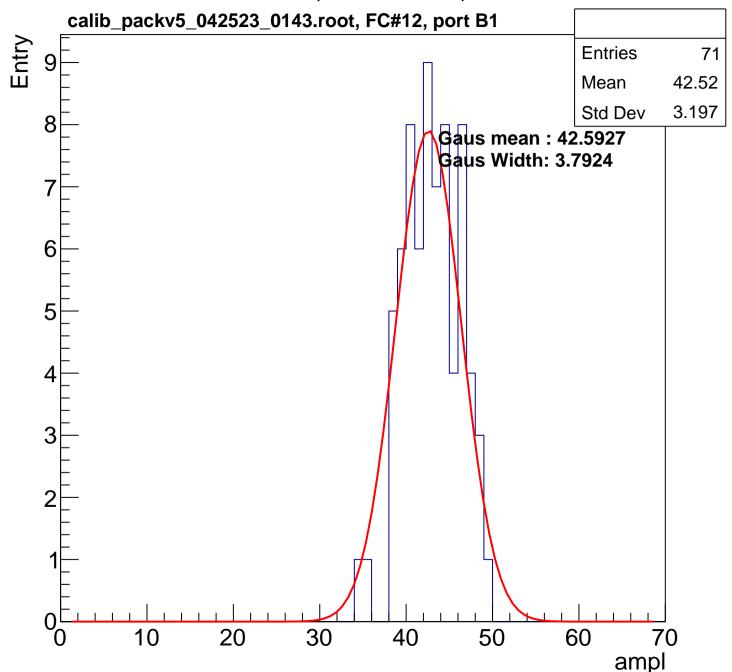


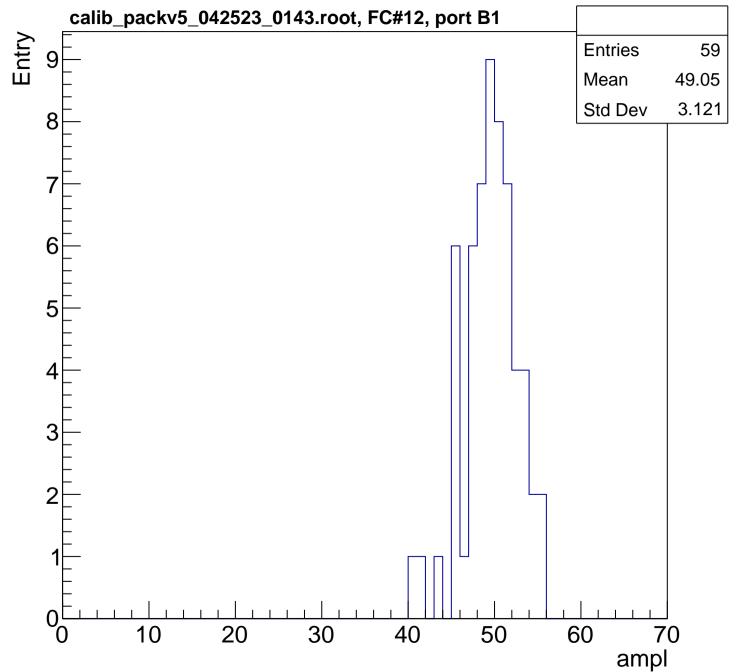


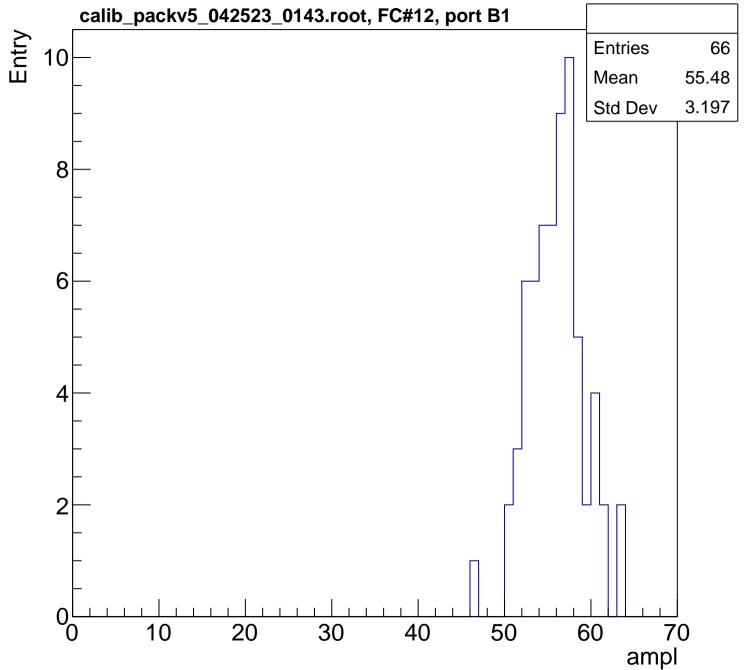


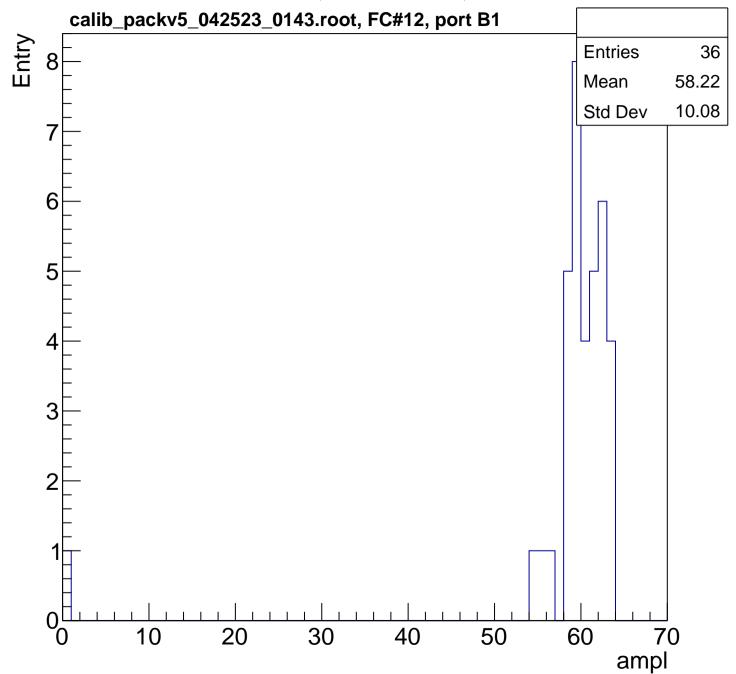


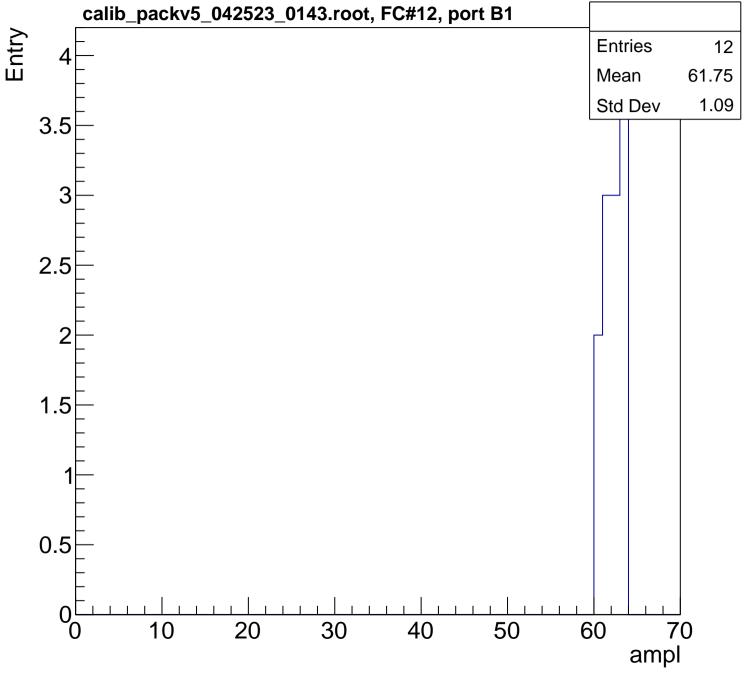




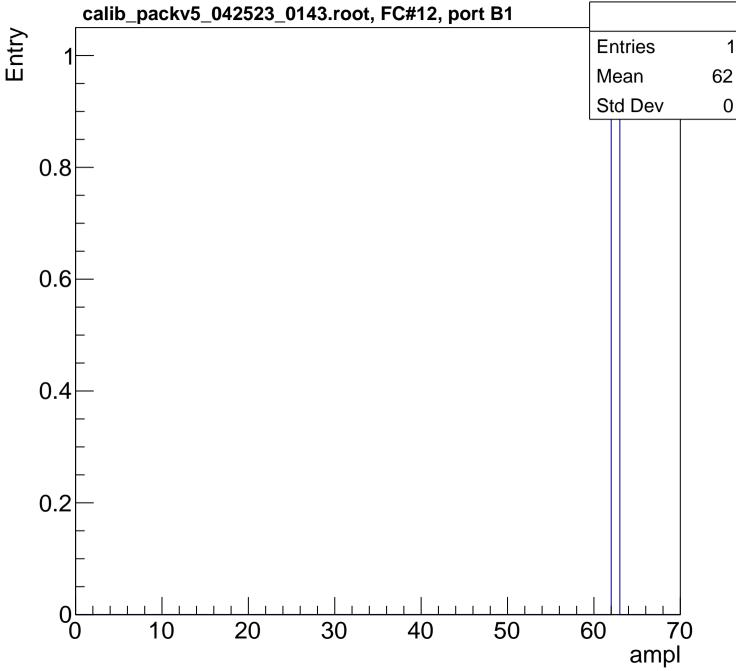


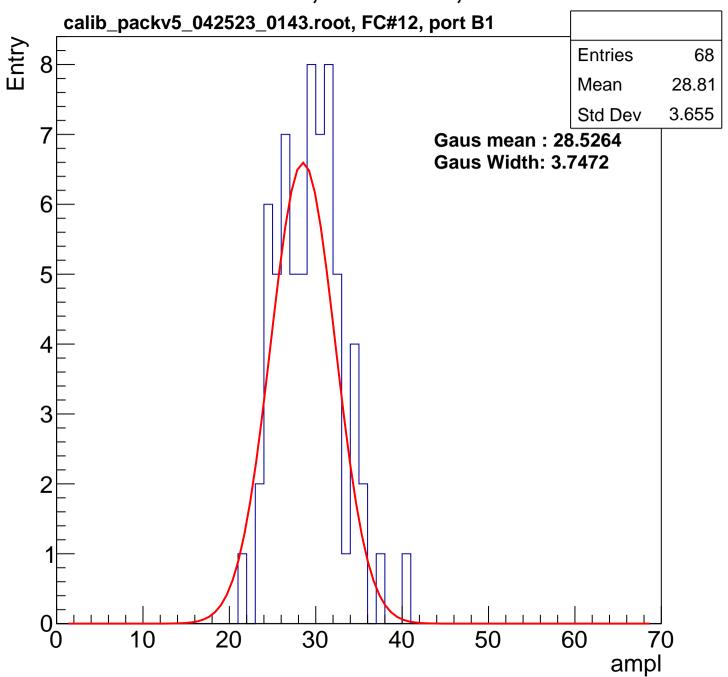


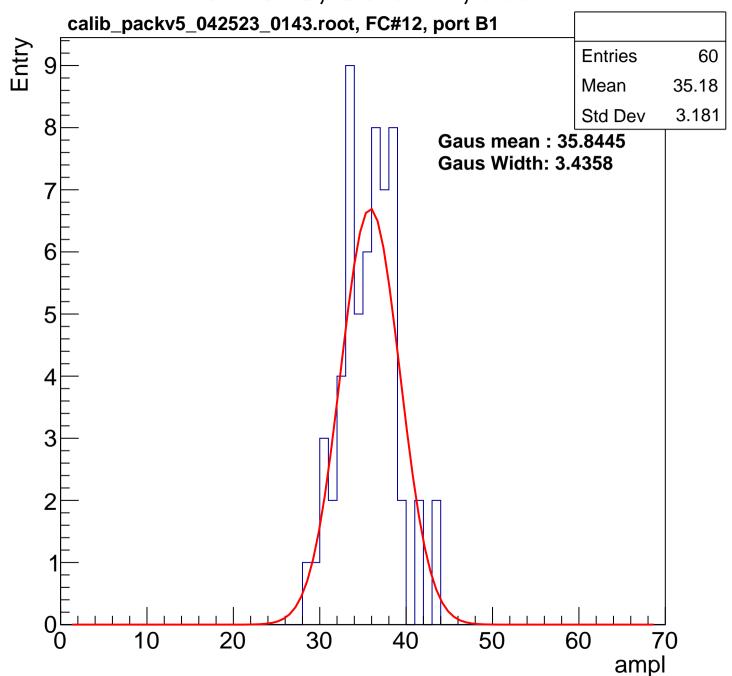


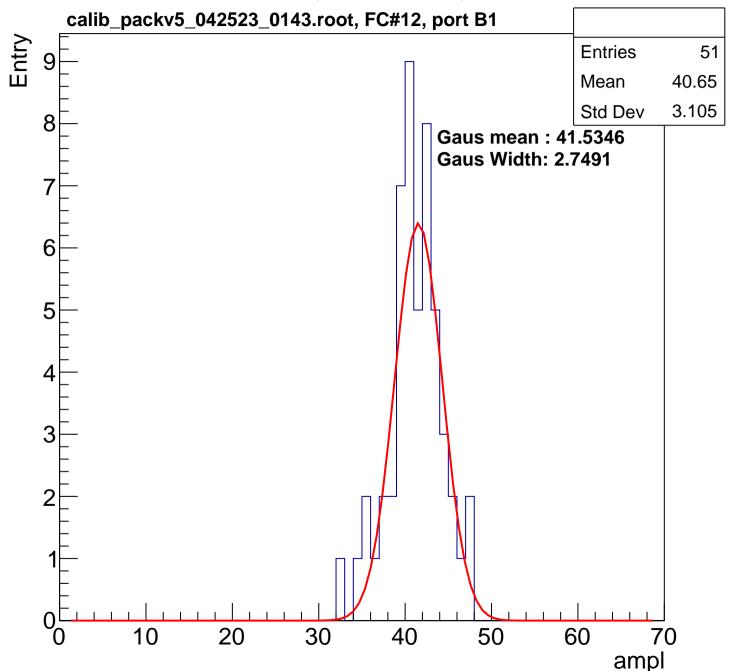


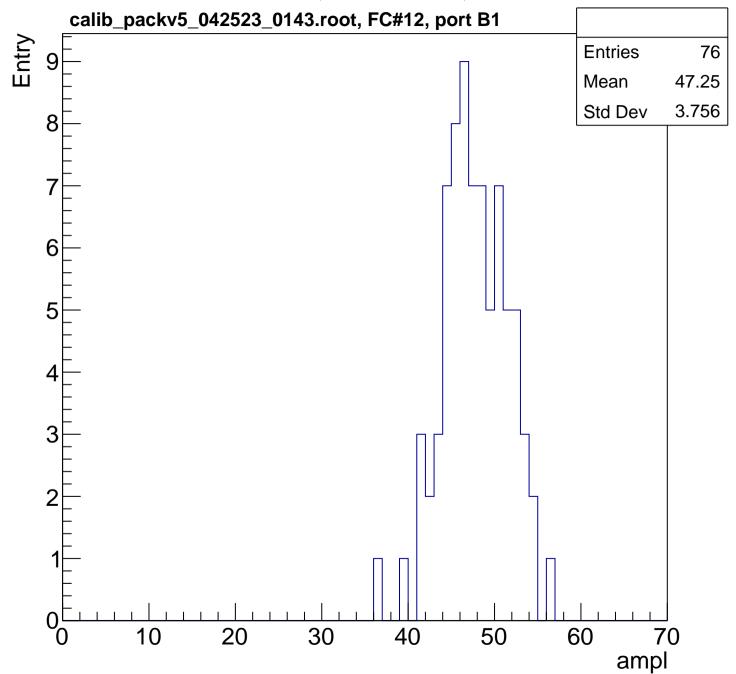
0

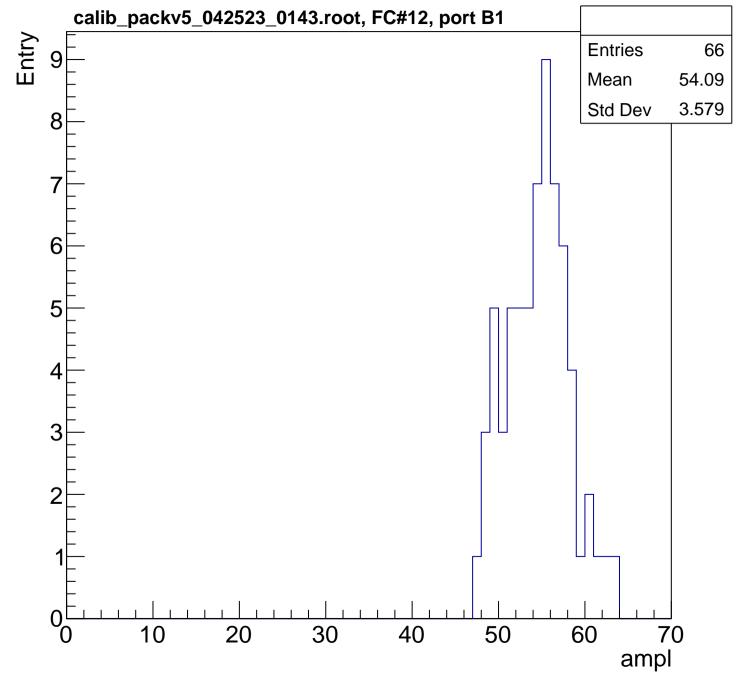


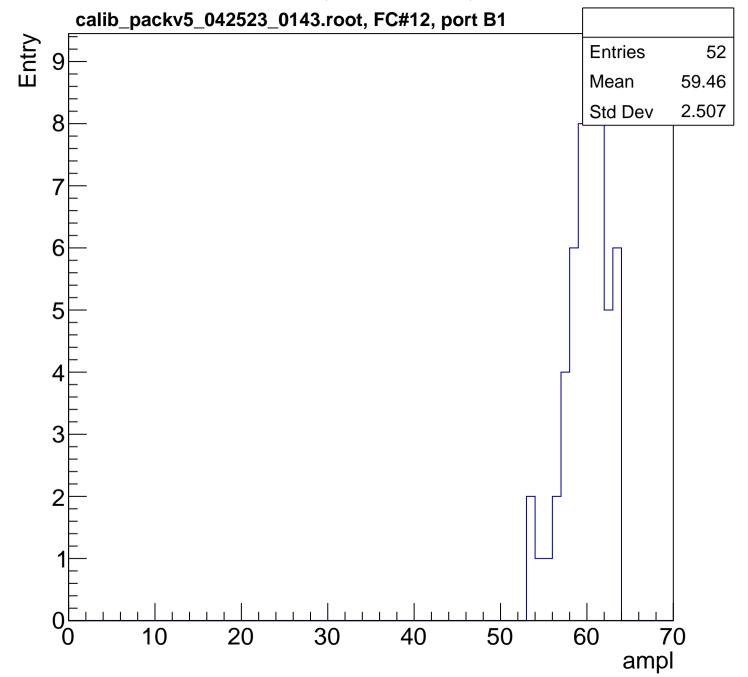


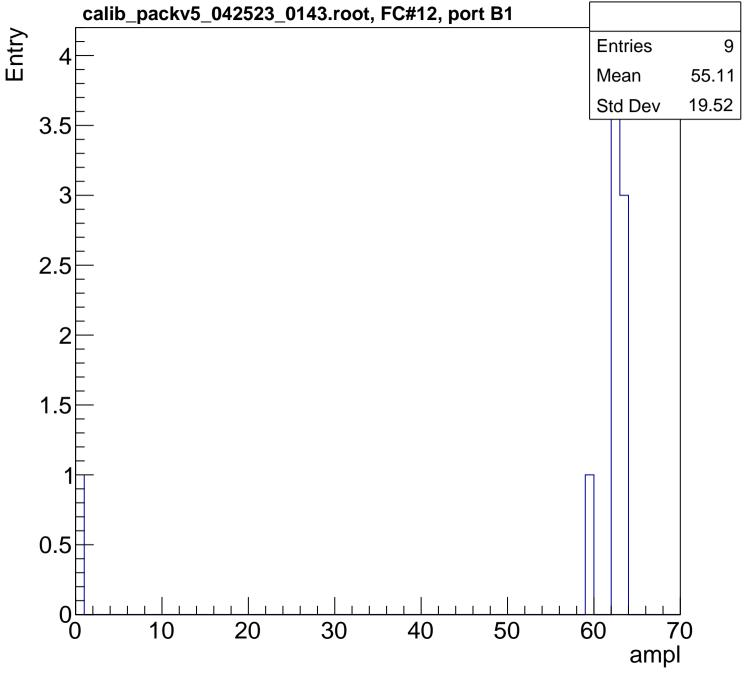




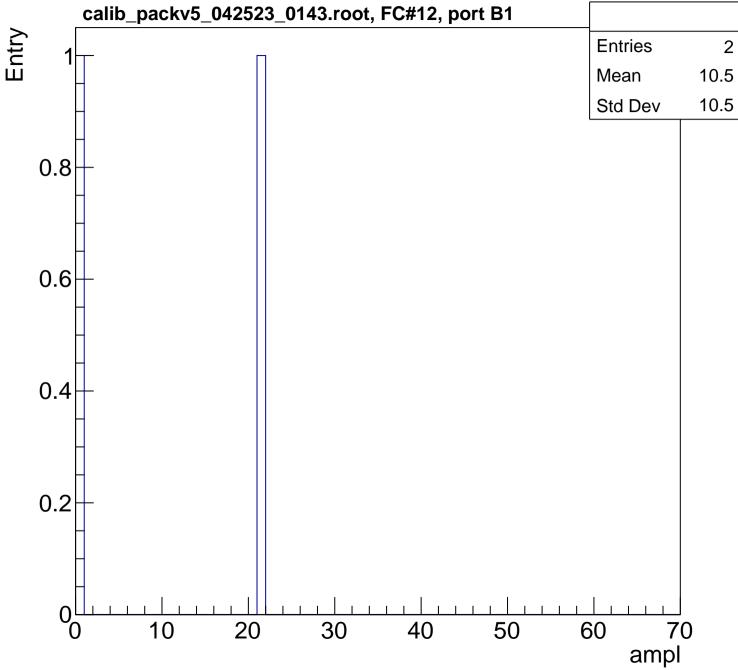


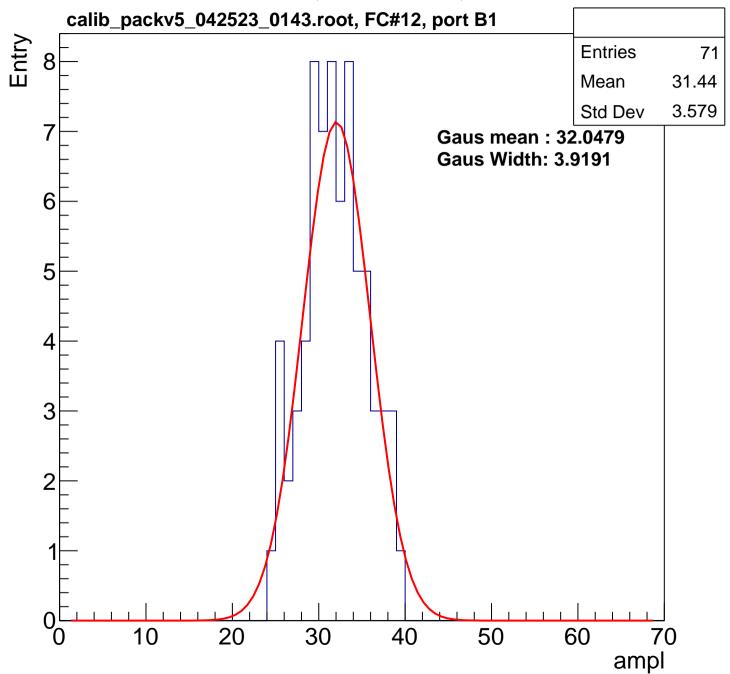


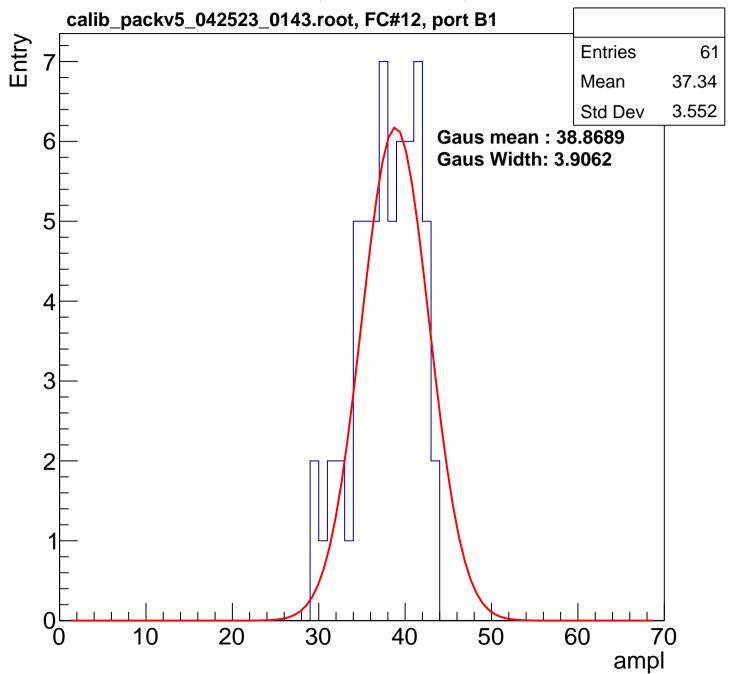


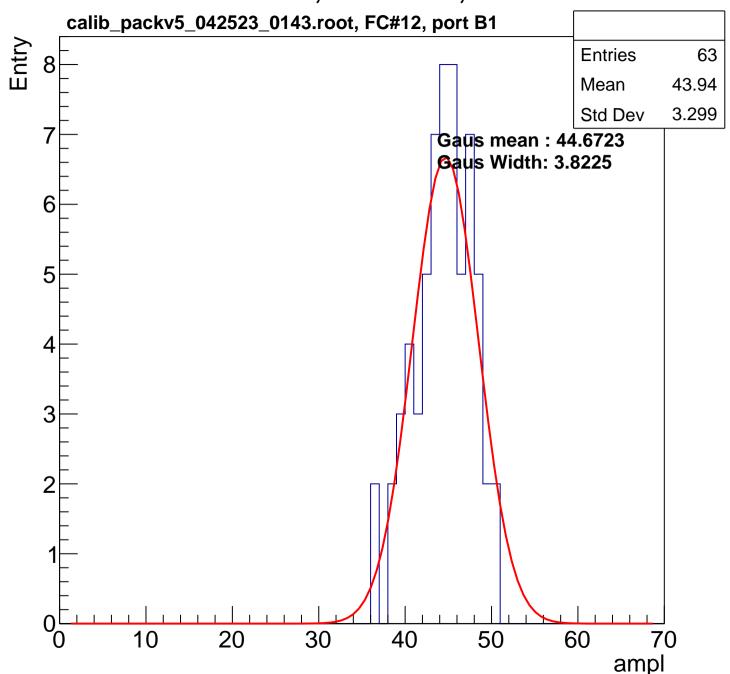


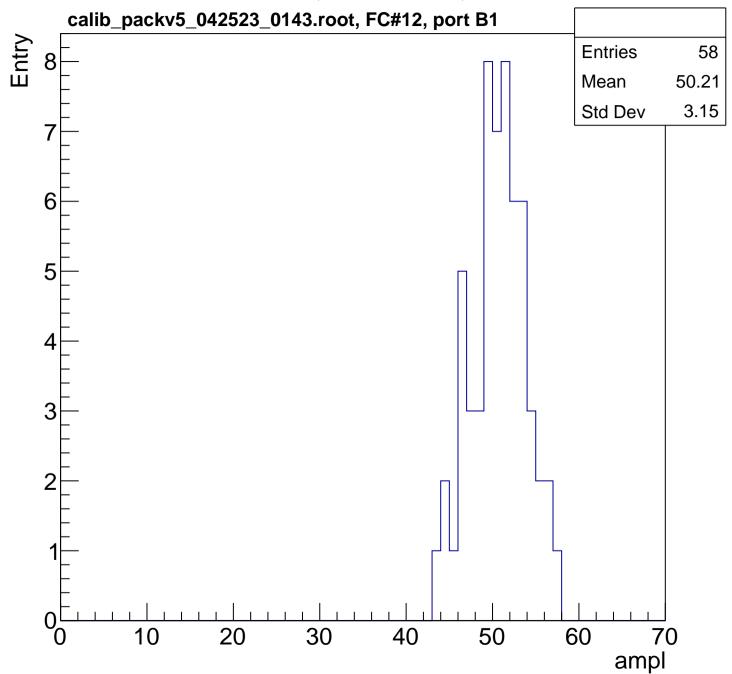
2

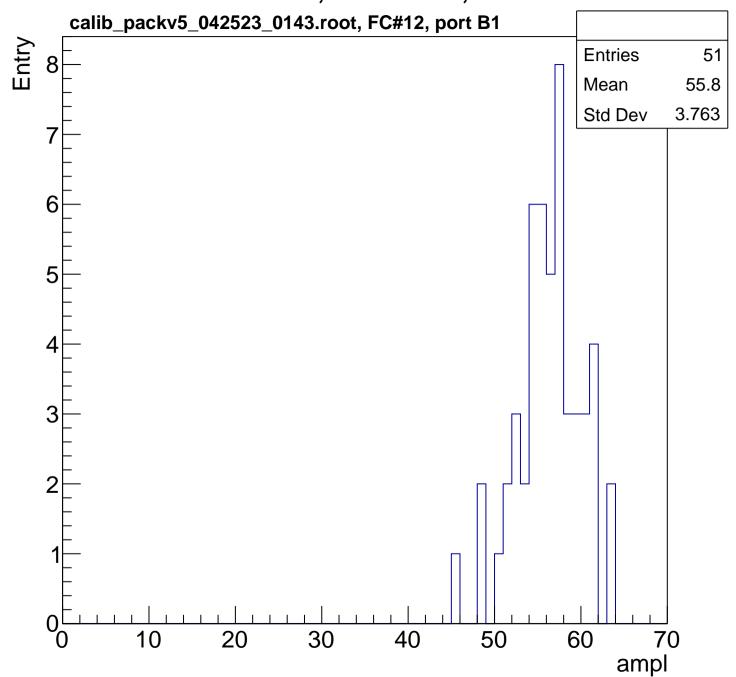


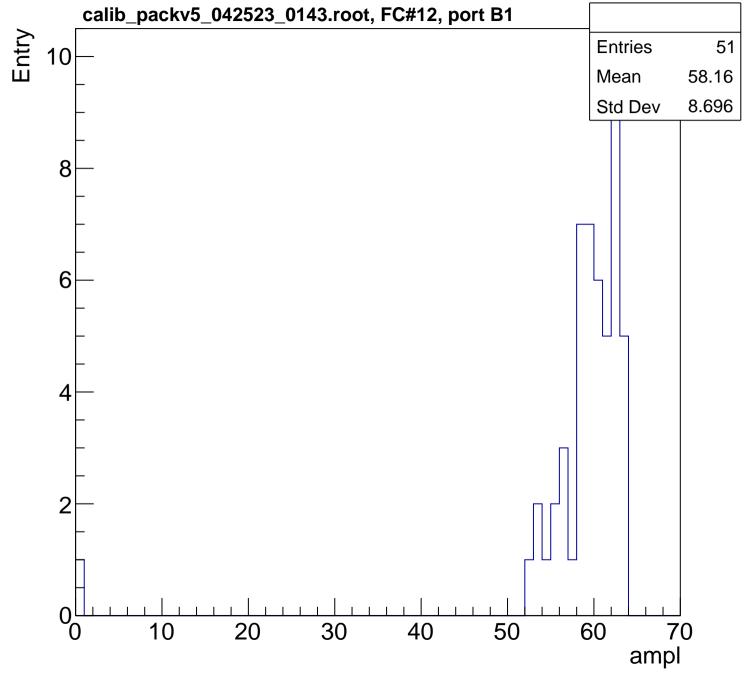


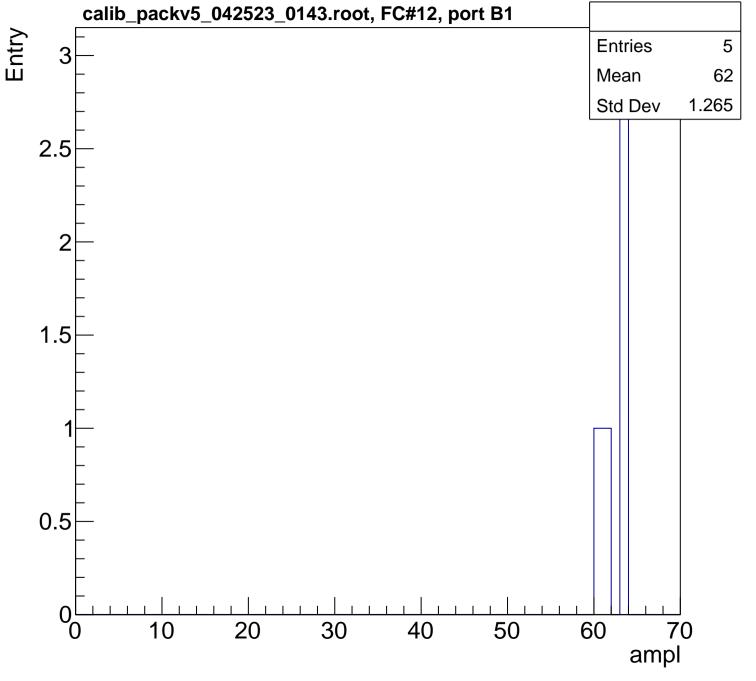


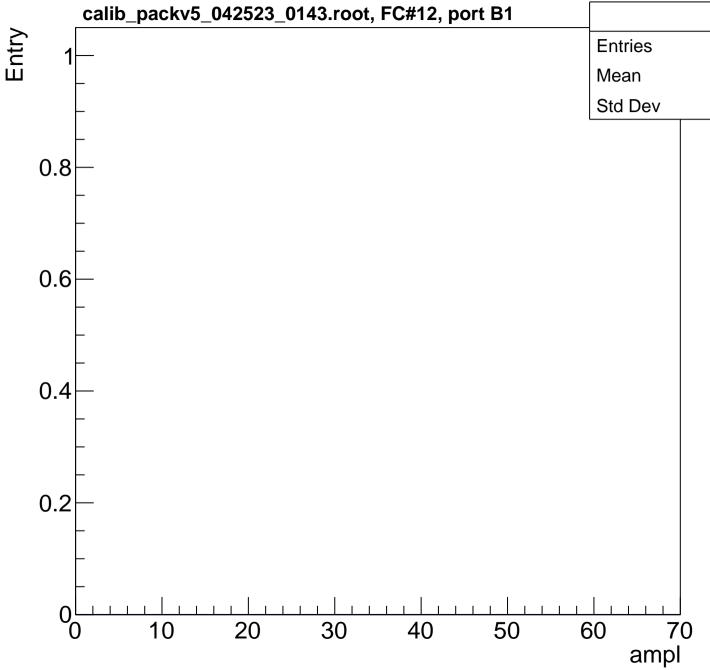


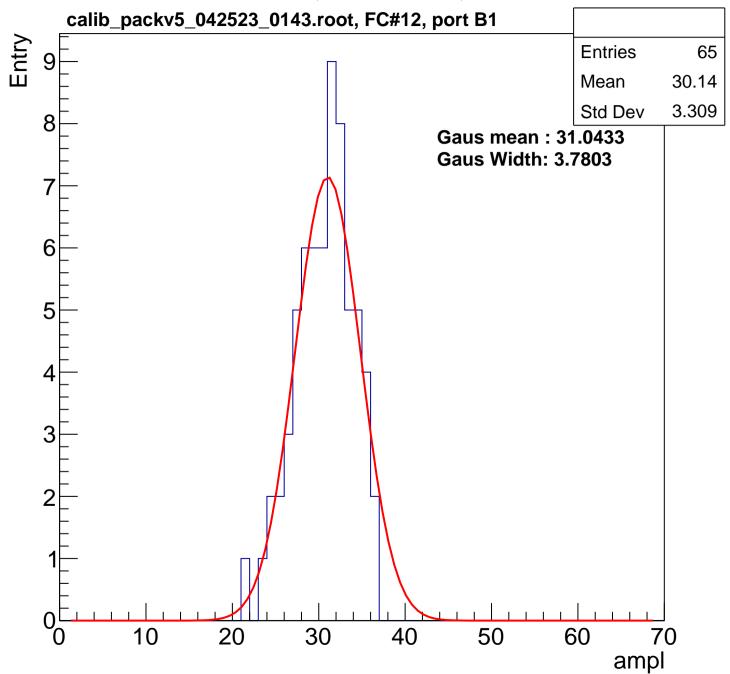


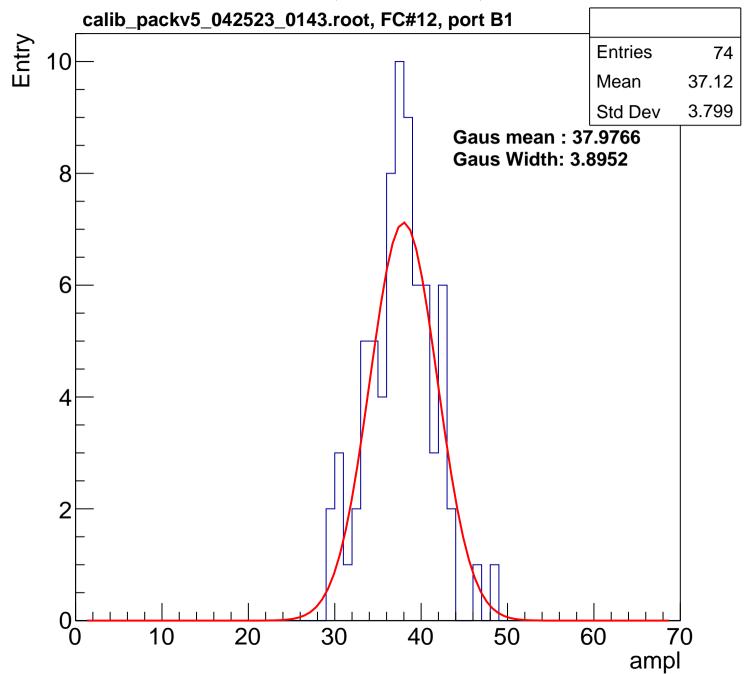


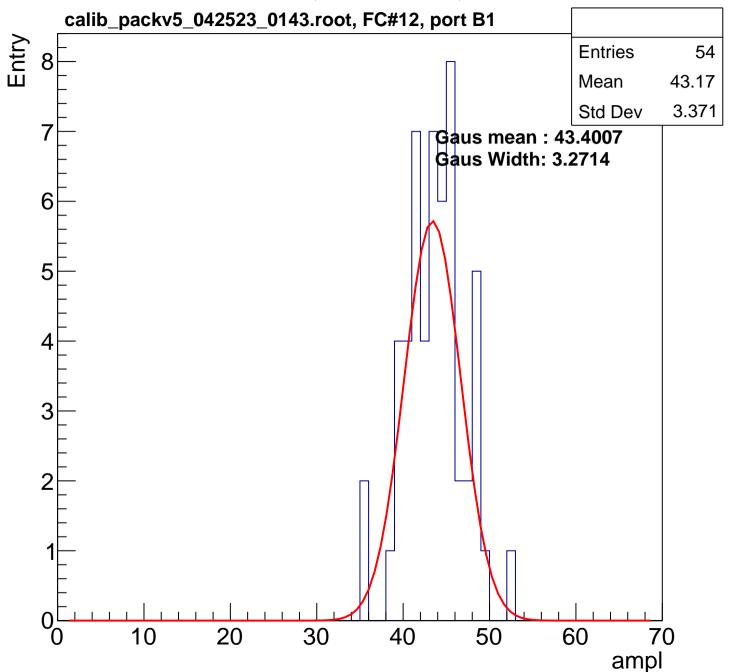


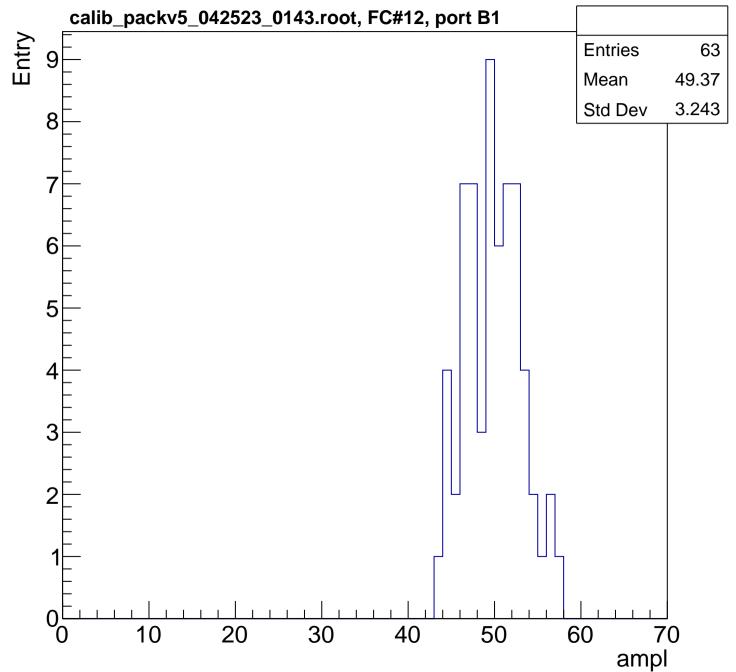


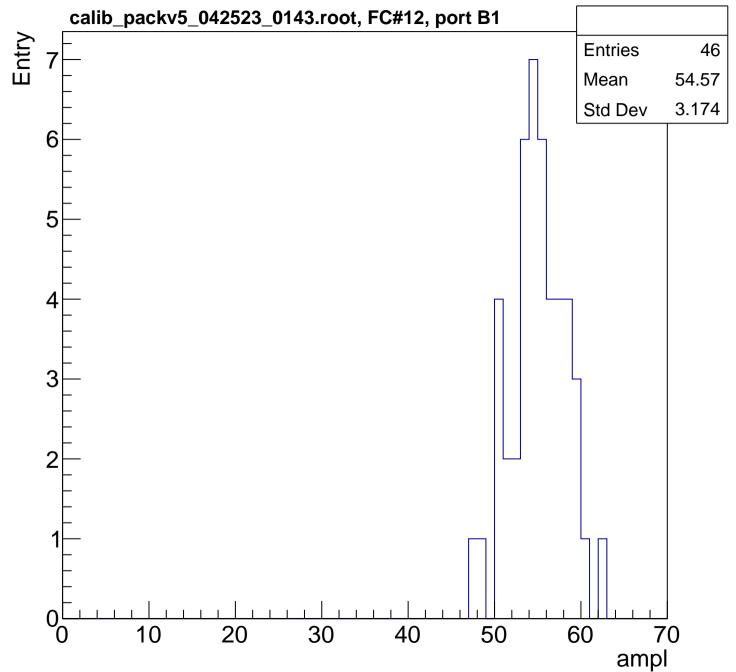


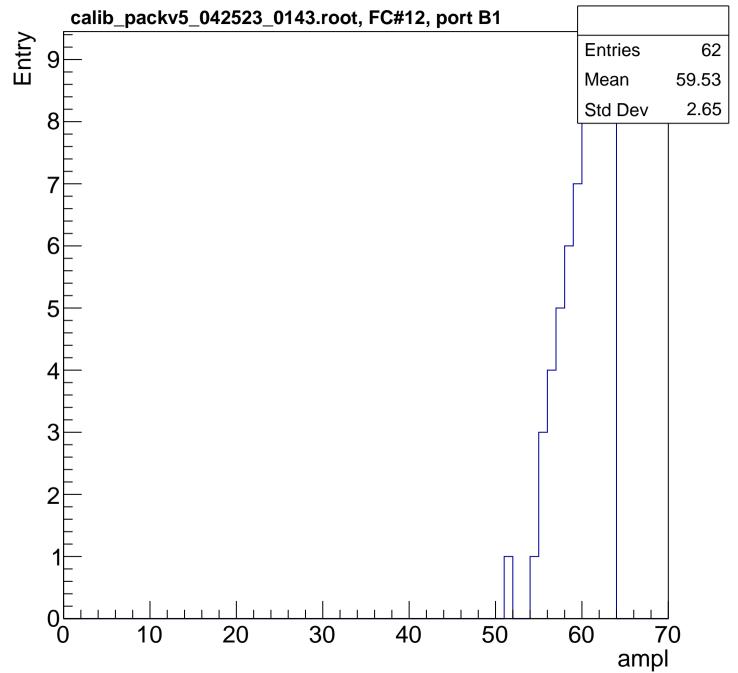


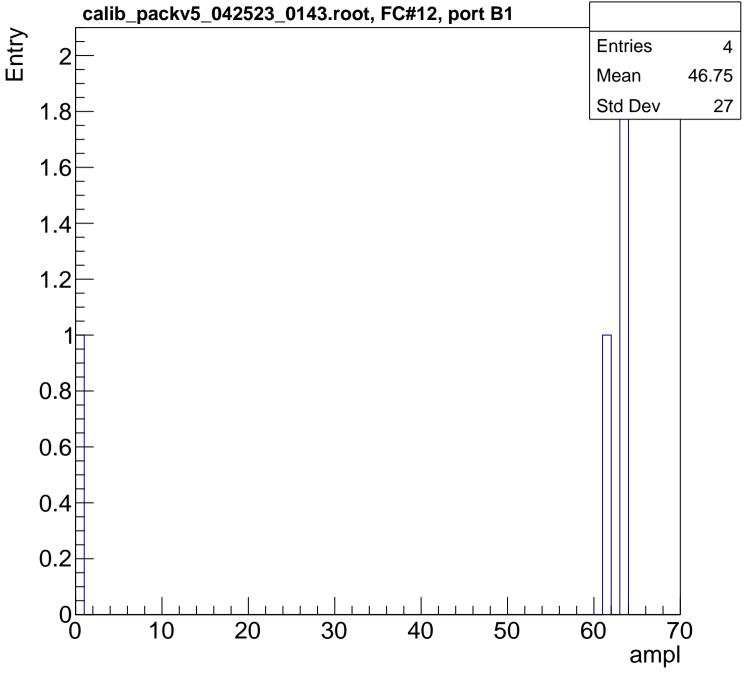


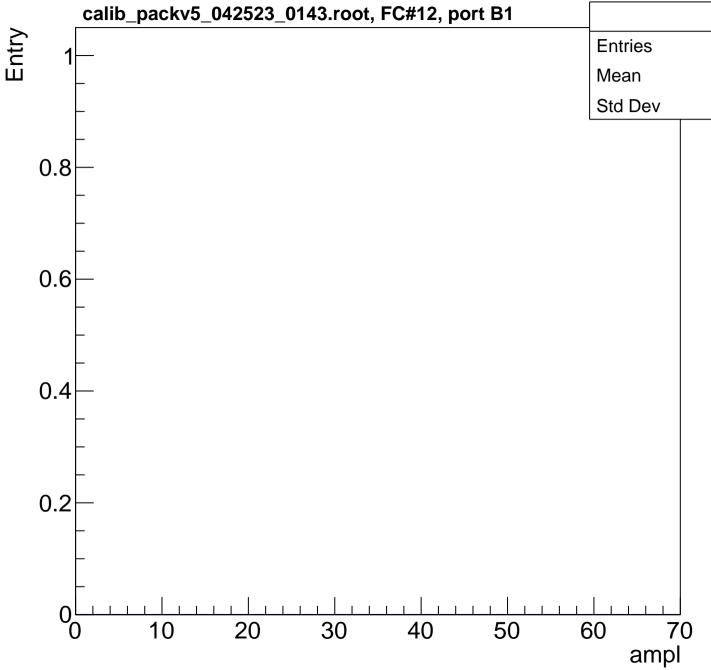


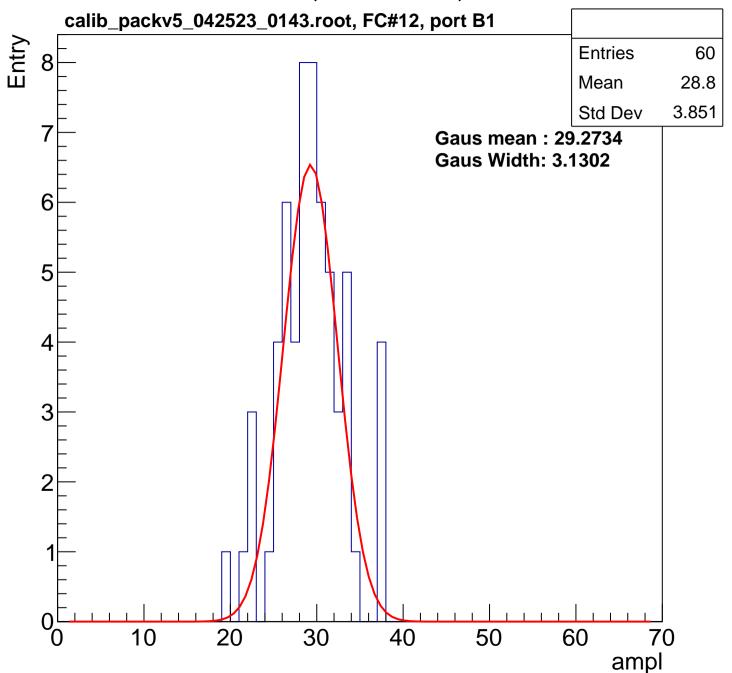


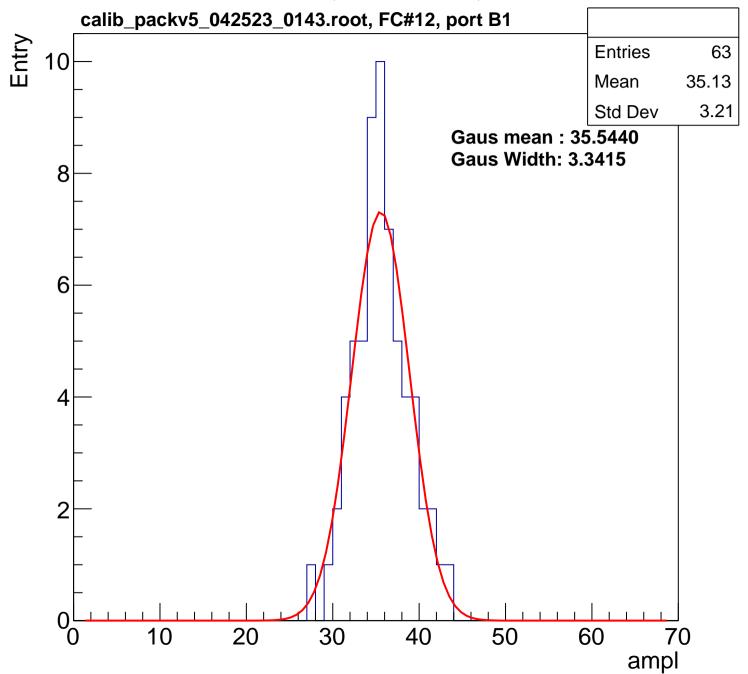


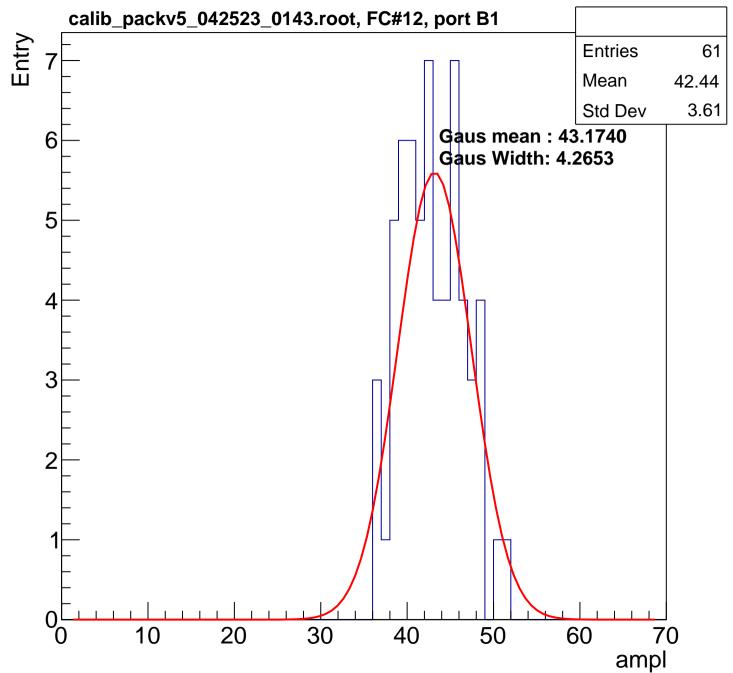


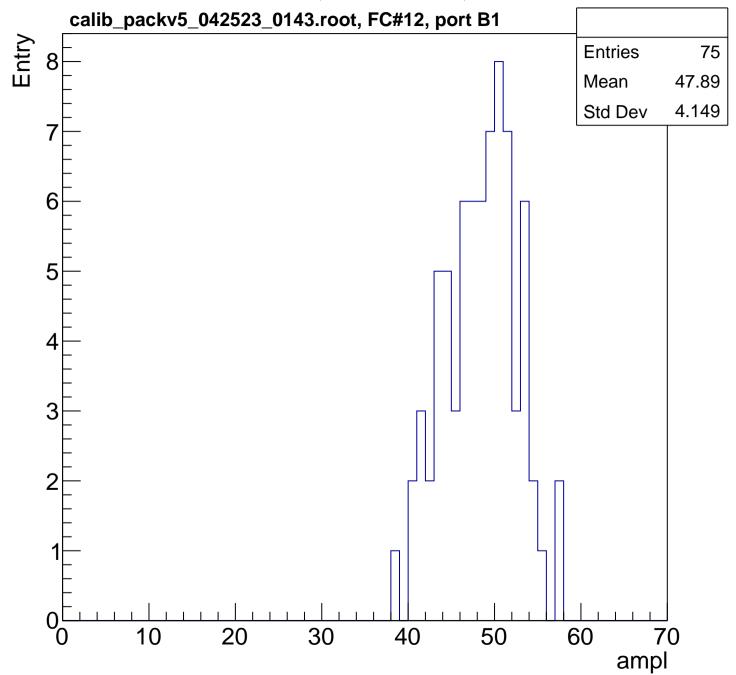


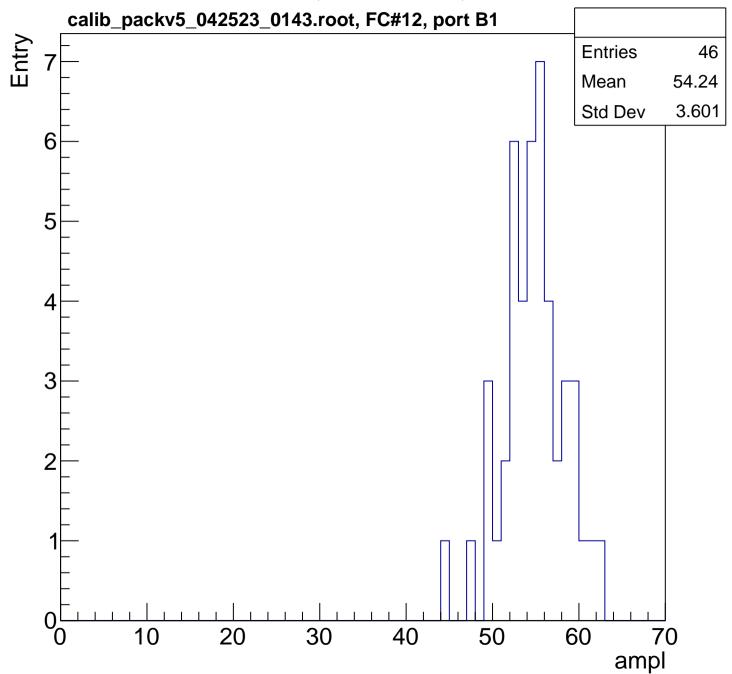


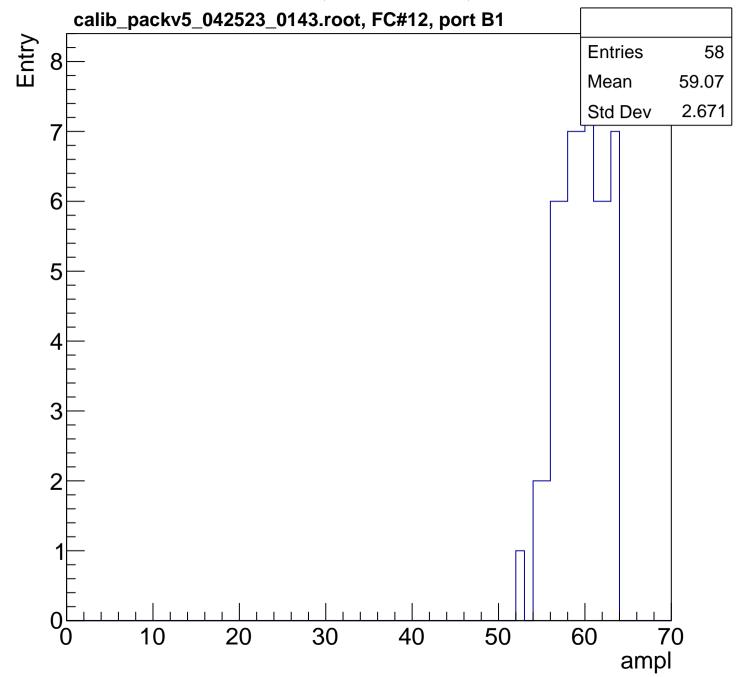


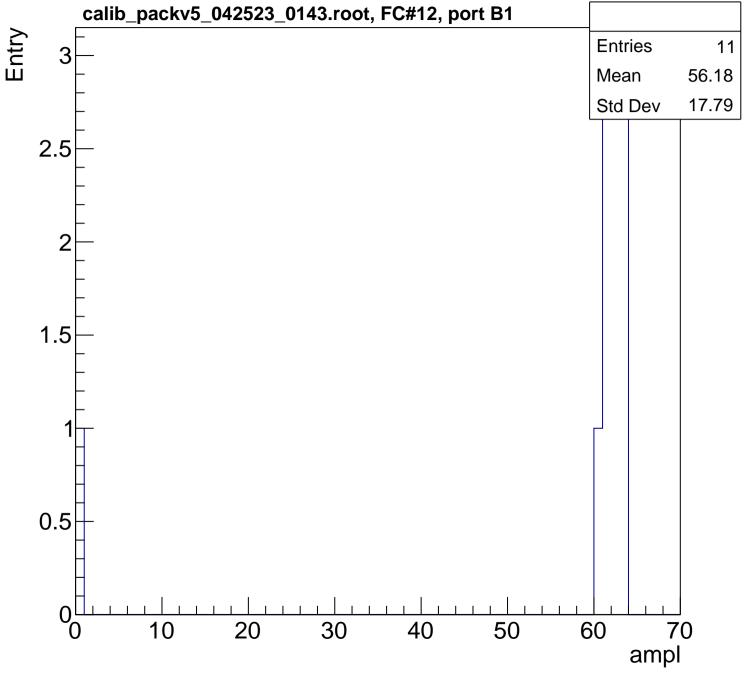


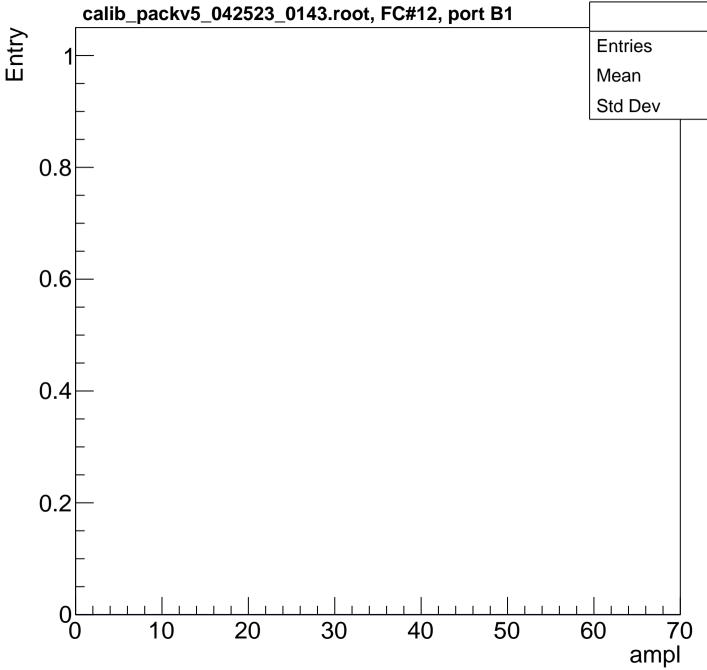


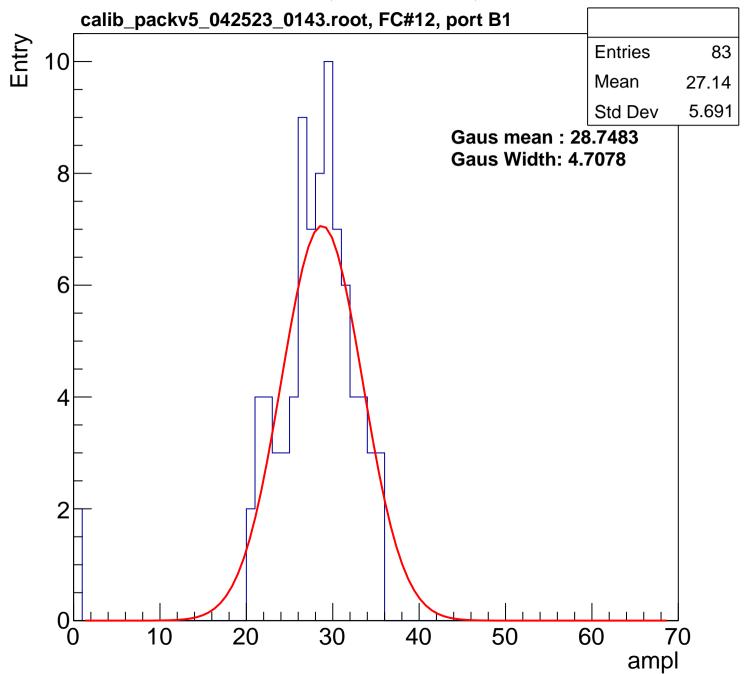


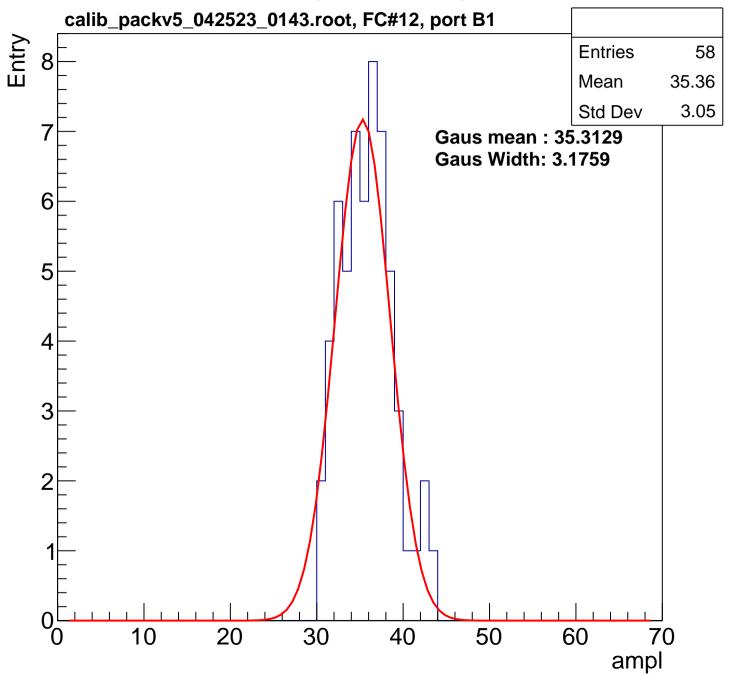


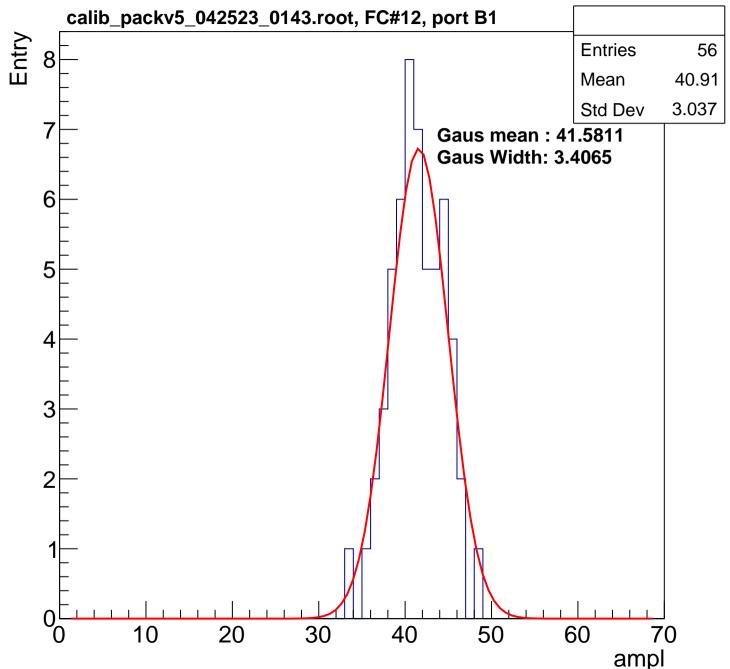


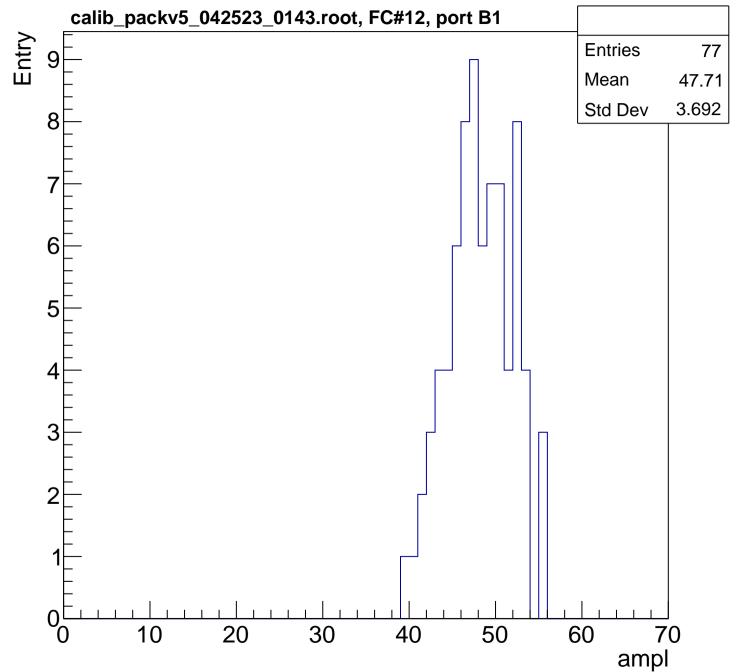


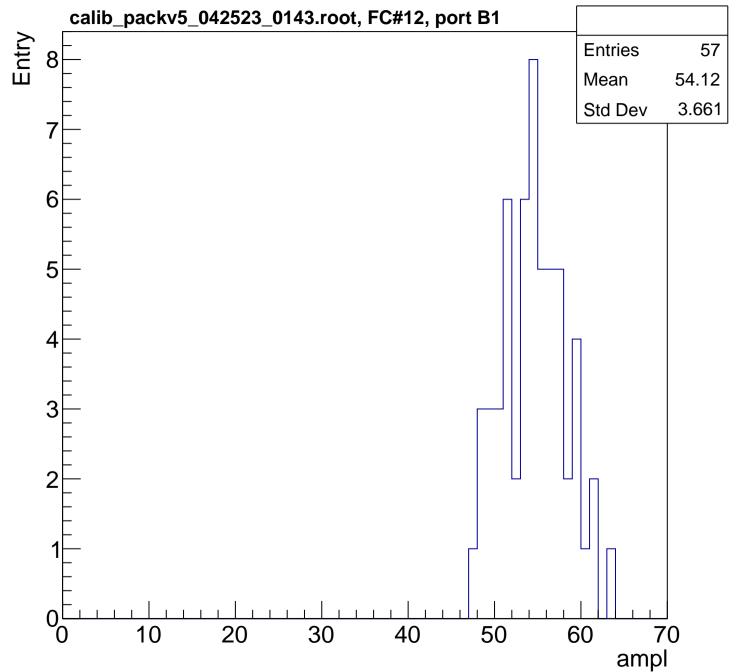


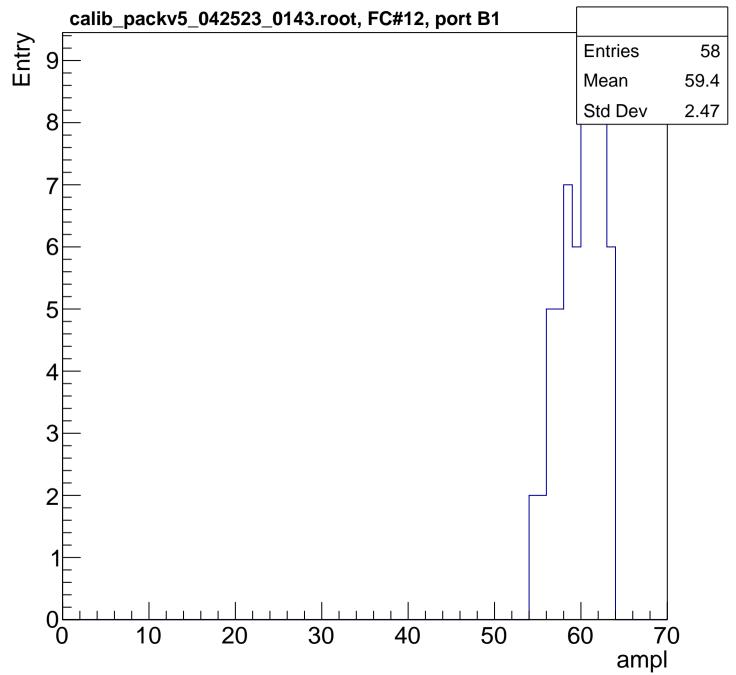


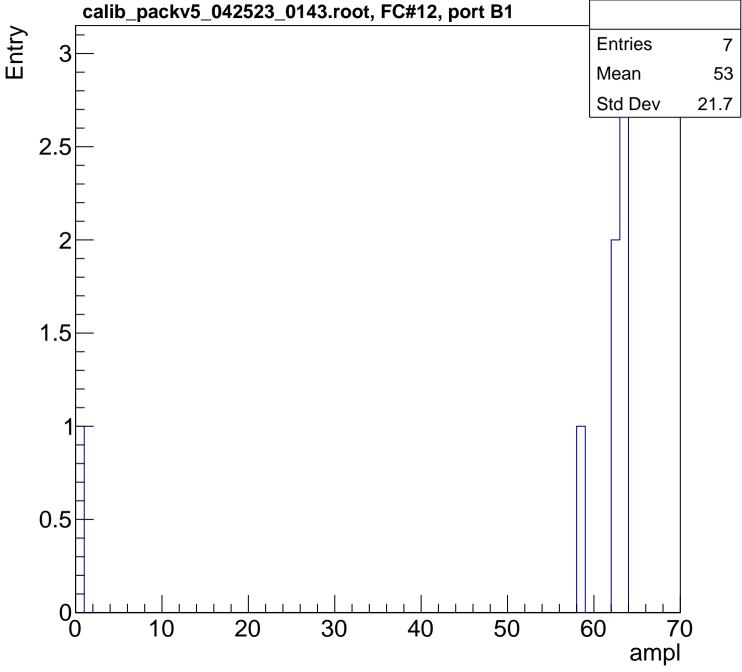




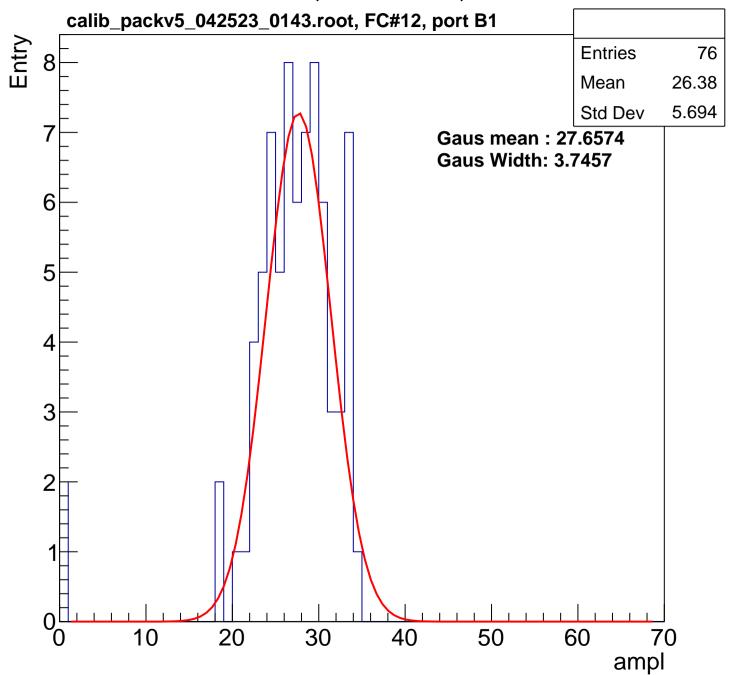


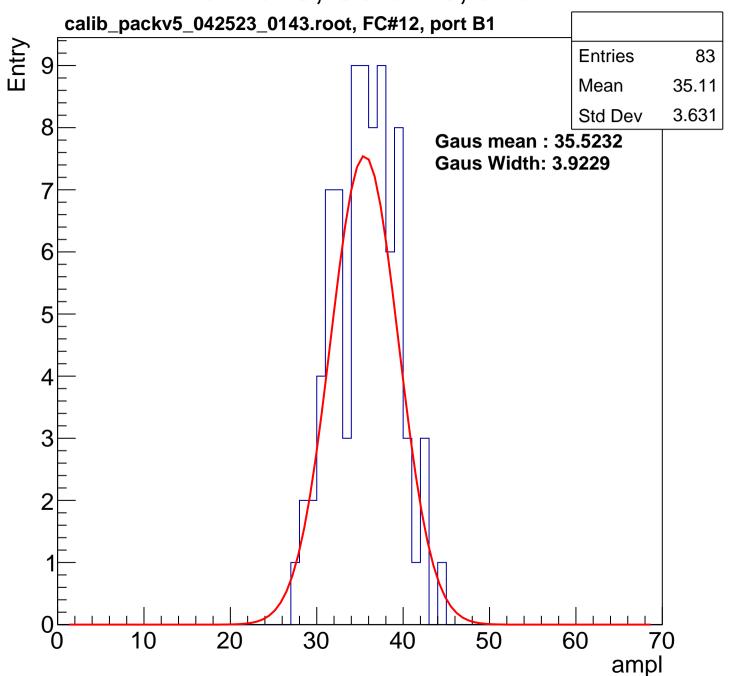


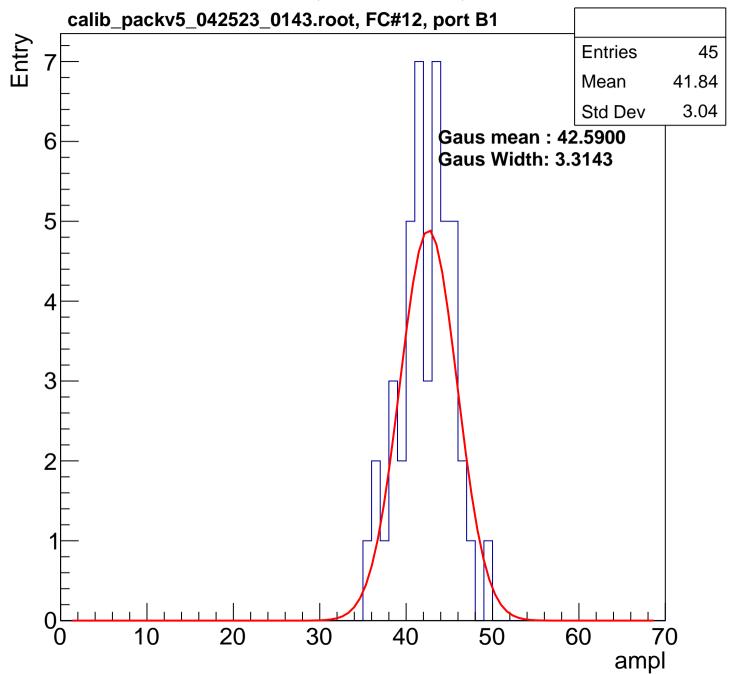


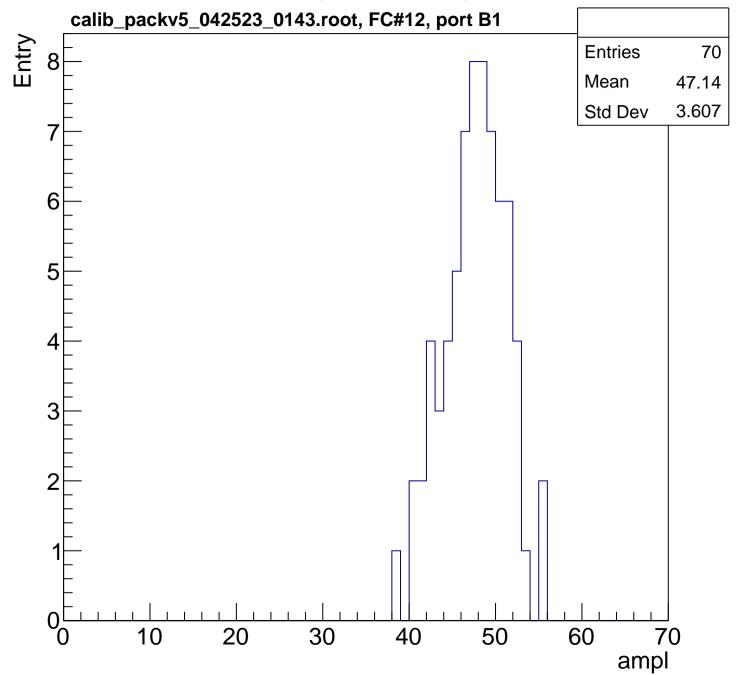


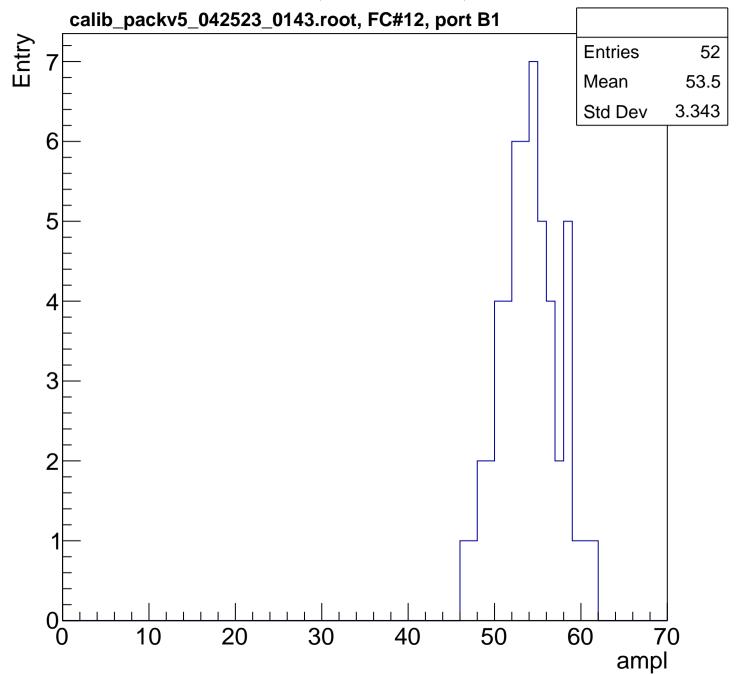
B0L102S, U3-ch45, adc7 calib_packv5_042523_0143.root, FC#12, port B1 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

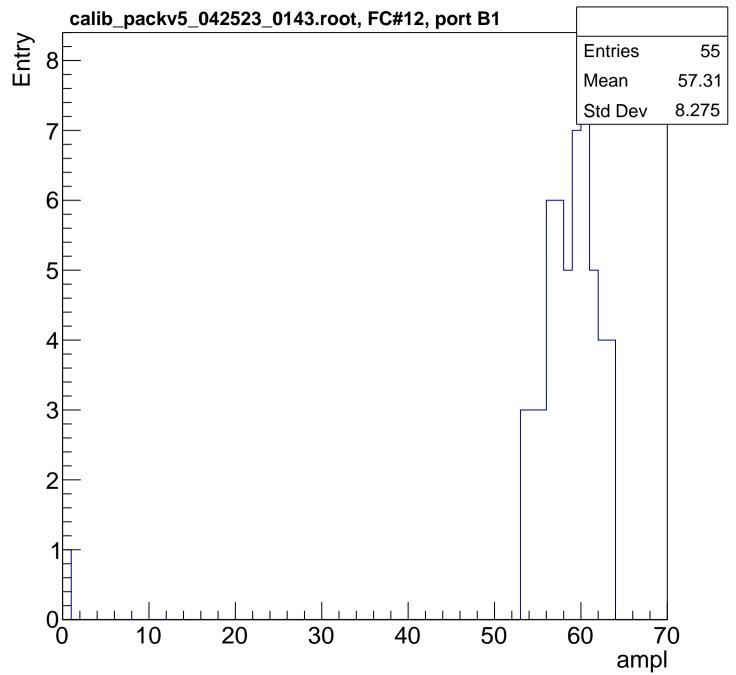


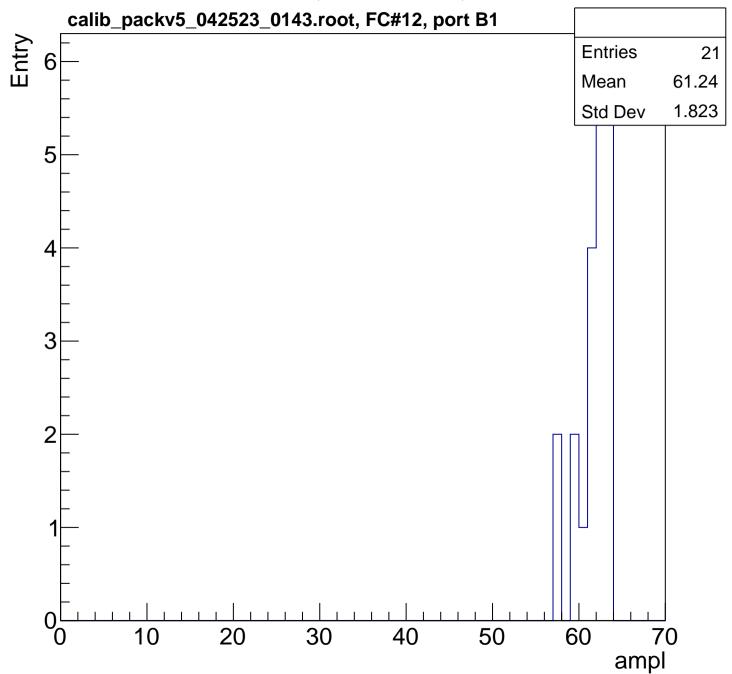


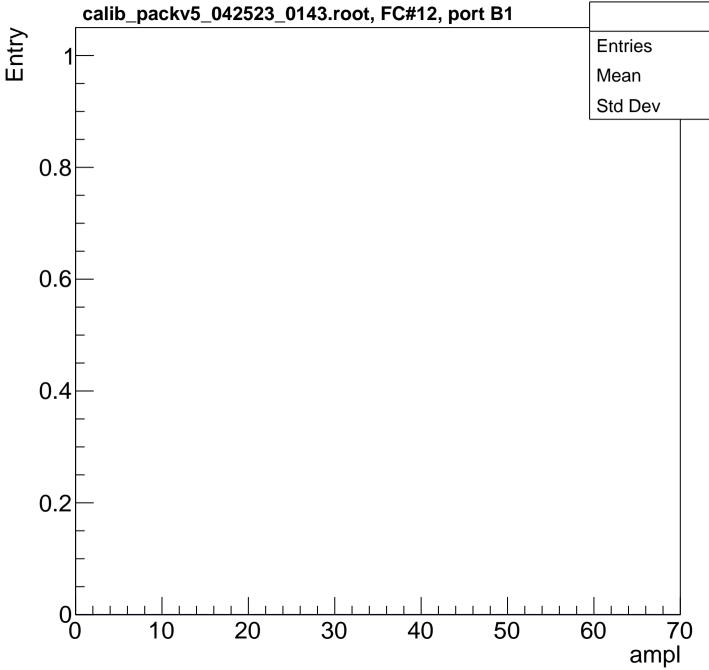


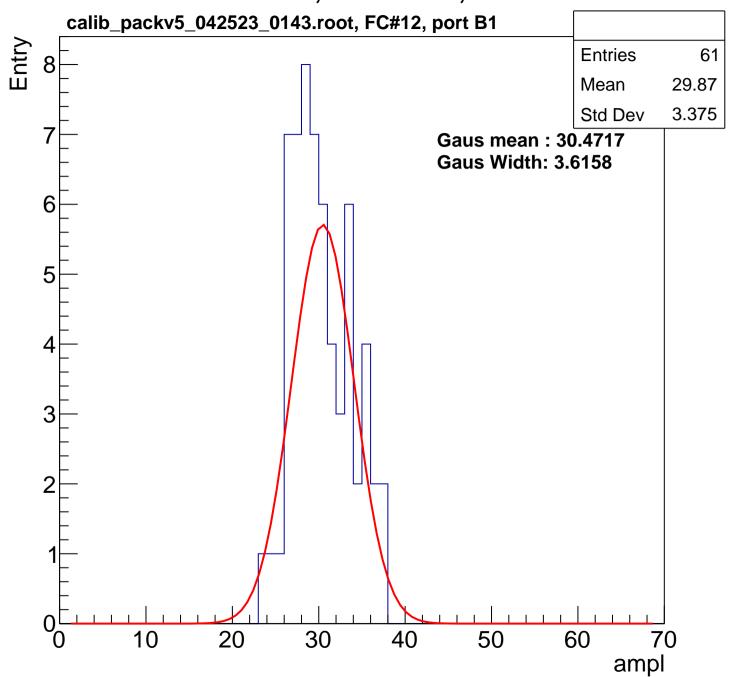


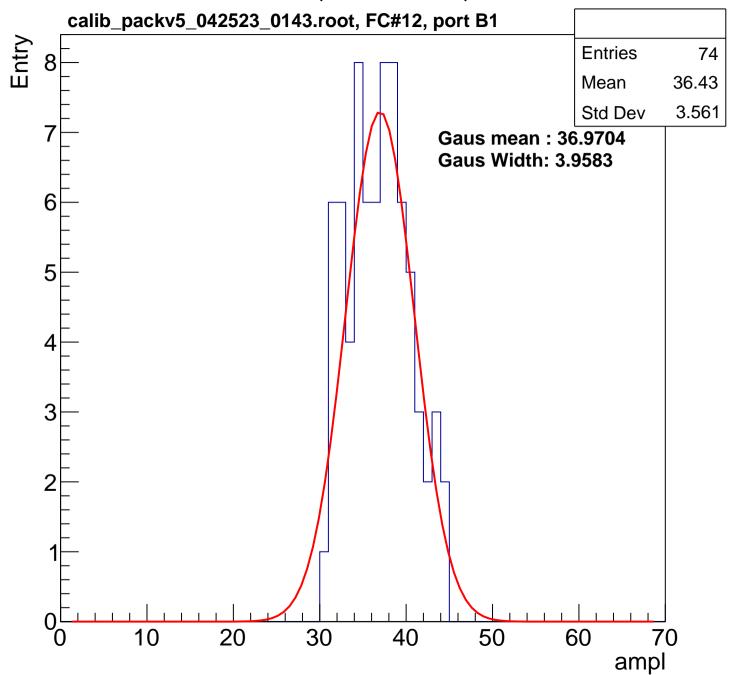


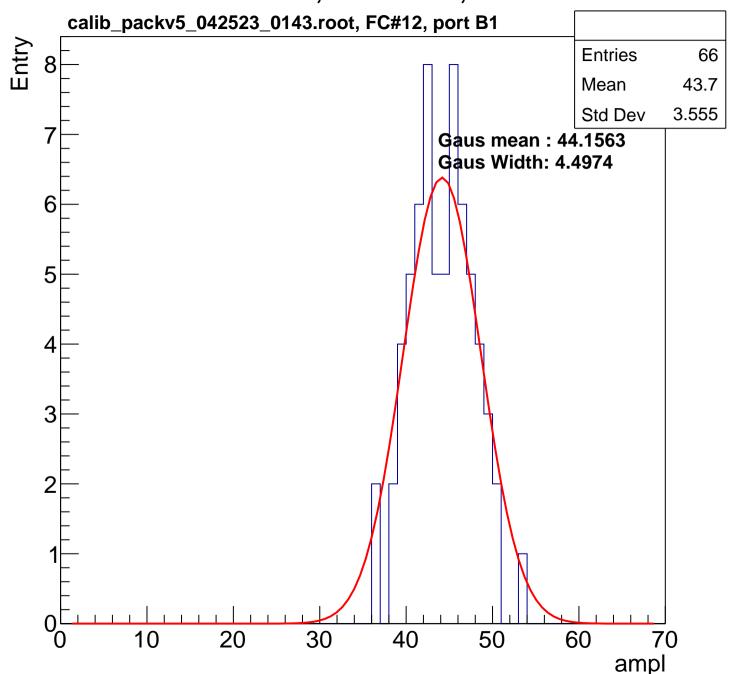


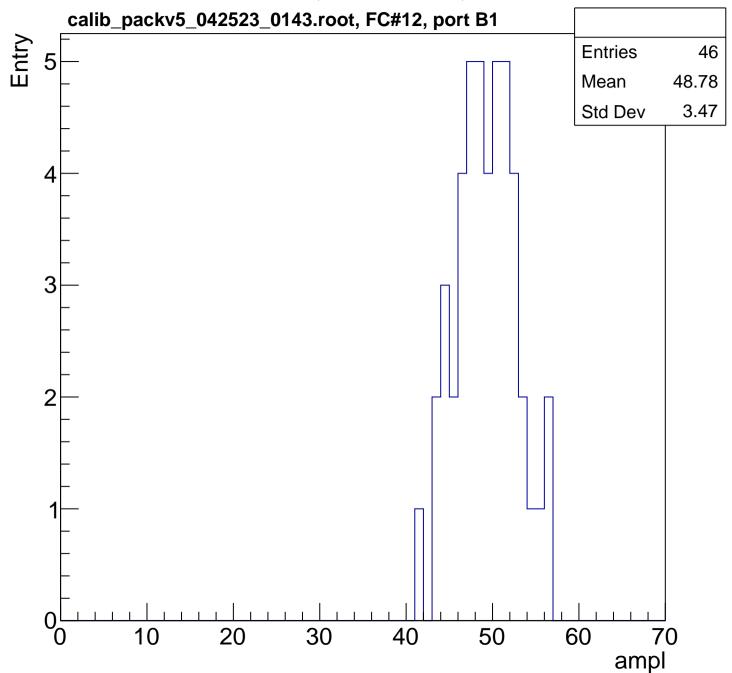


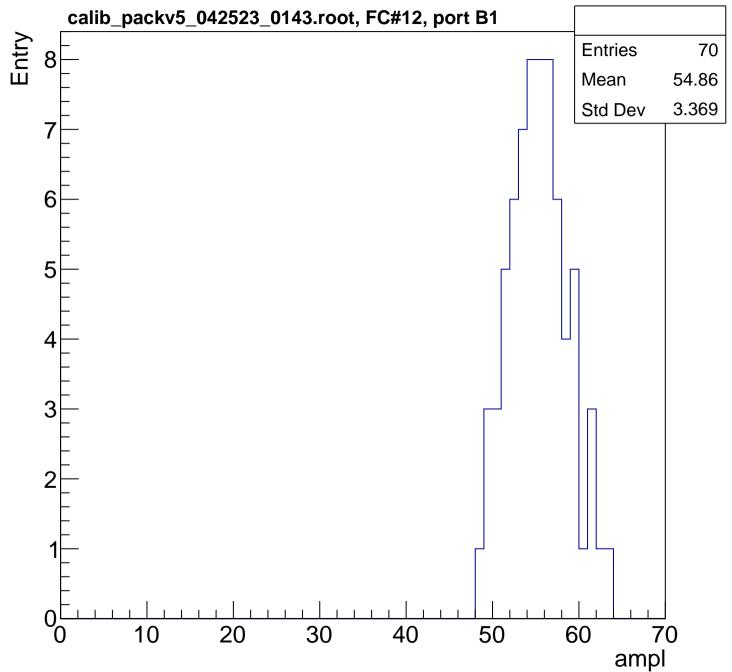


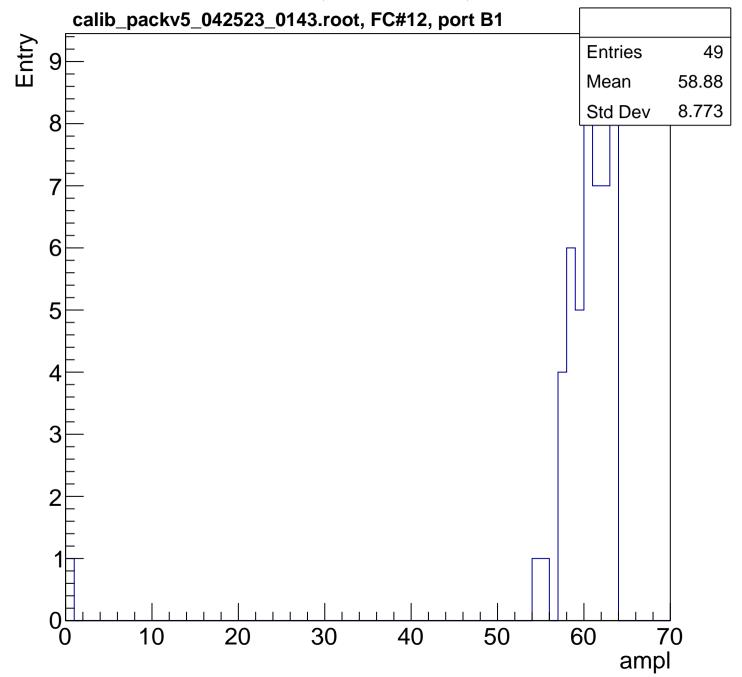


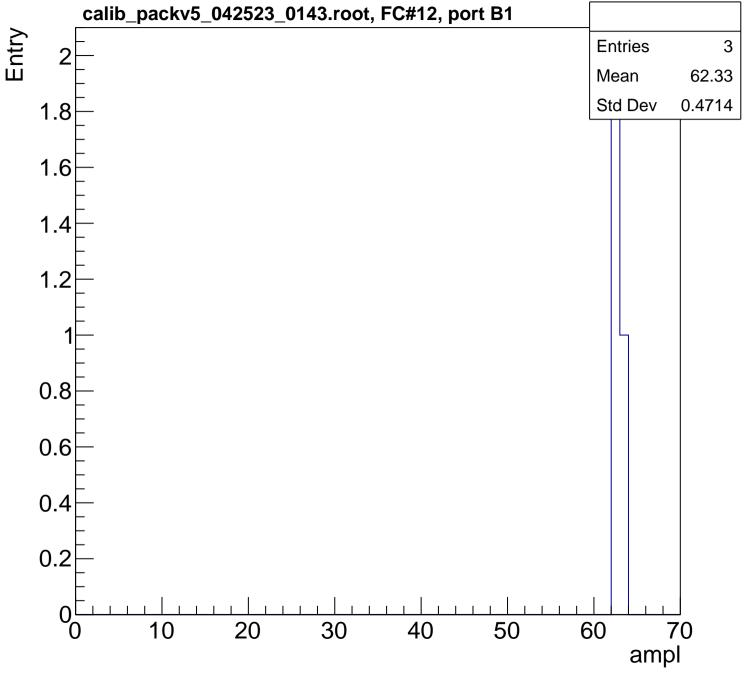




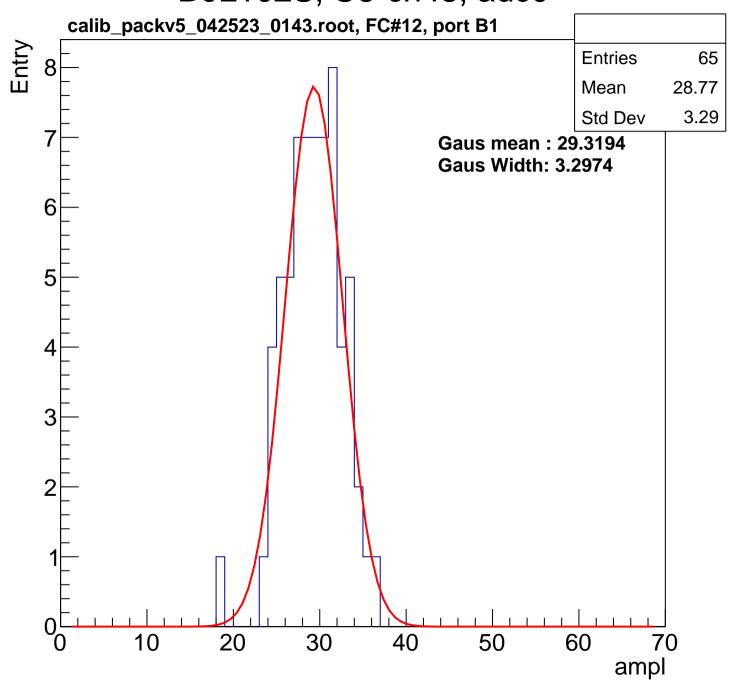


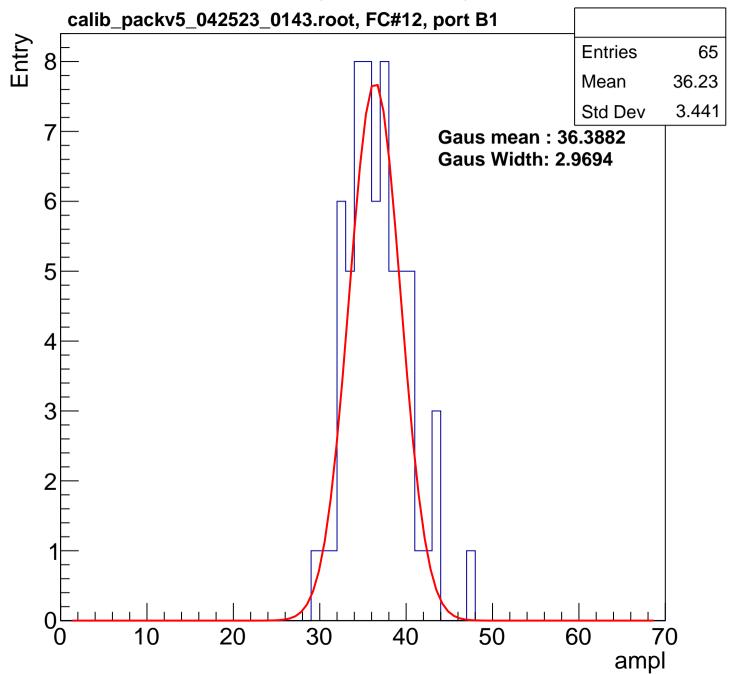


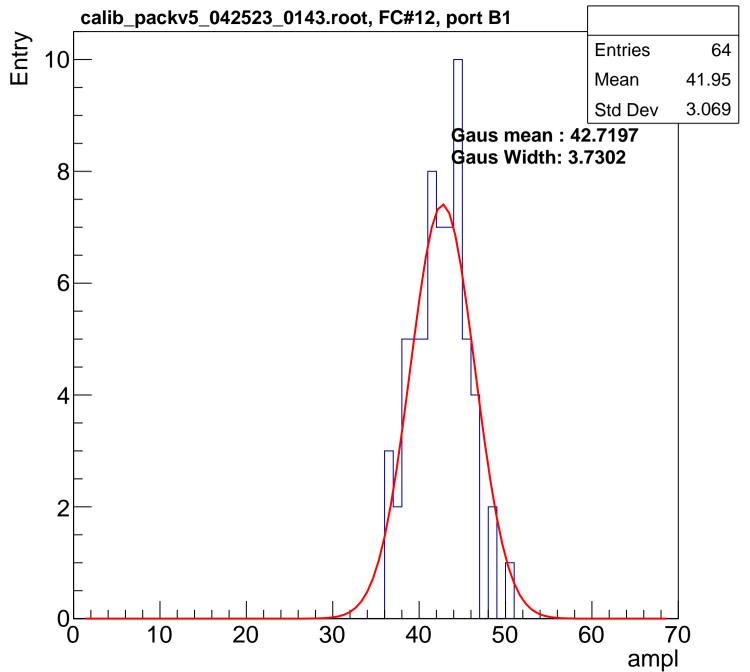


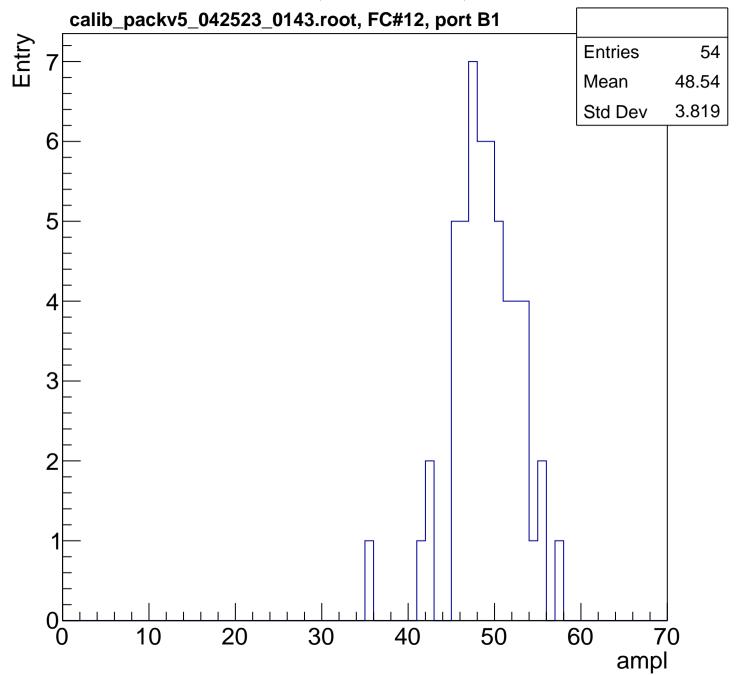


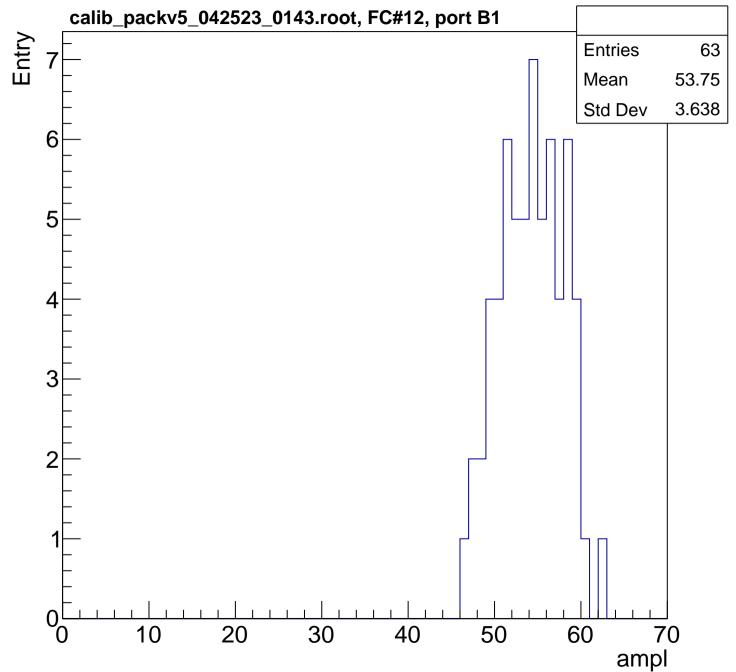
B0L102S, U3-ch47, adc7 calib_packv5_042523_0143.root, FC#12, port B1 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

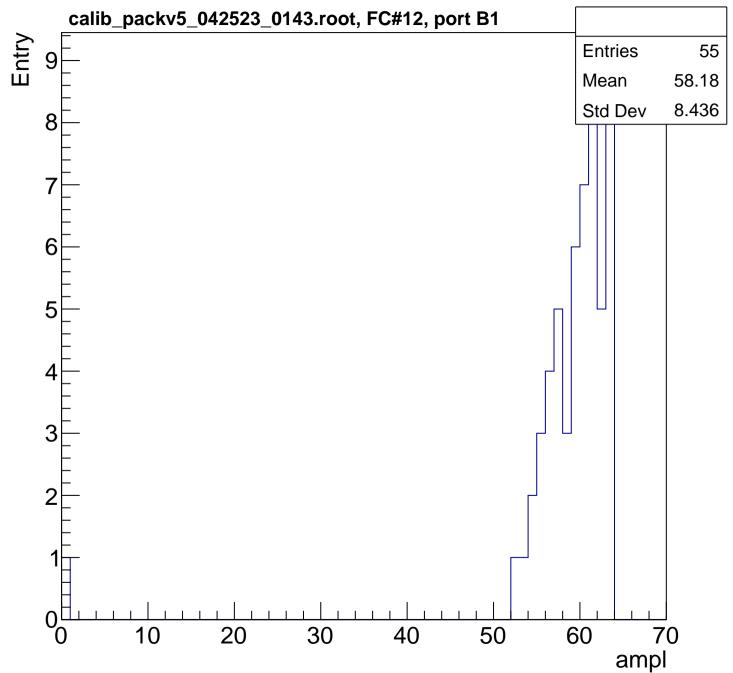


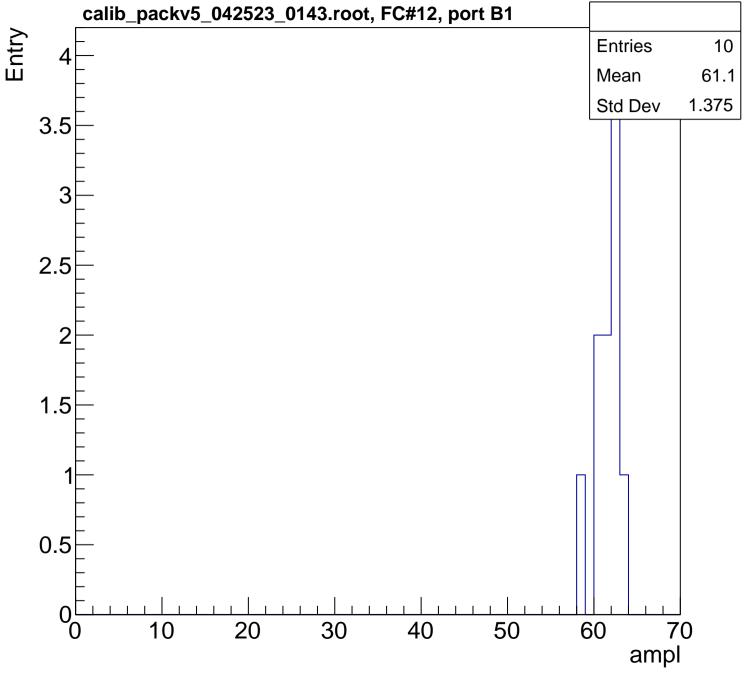




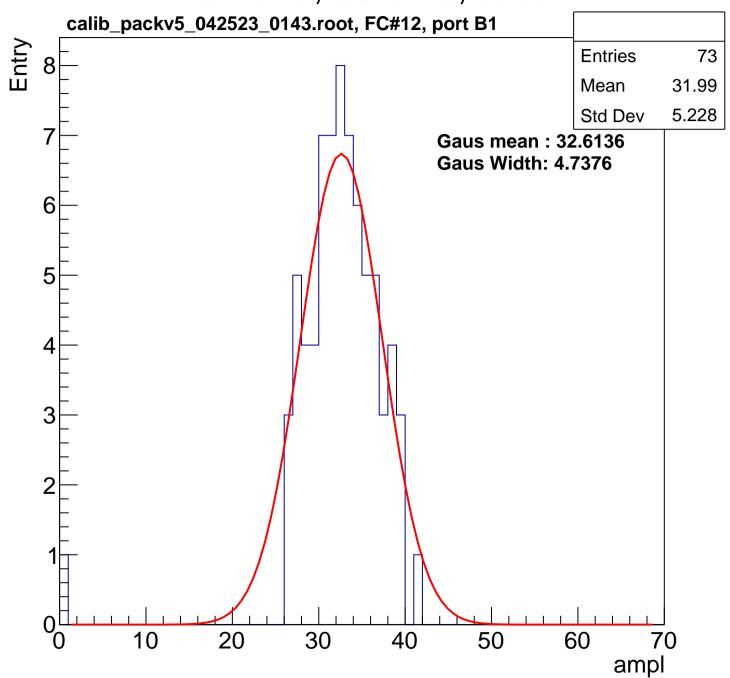


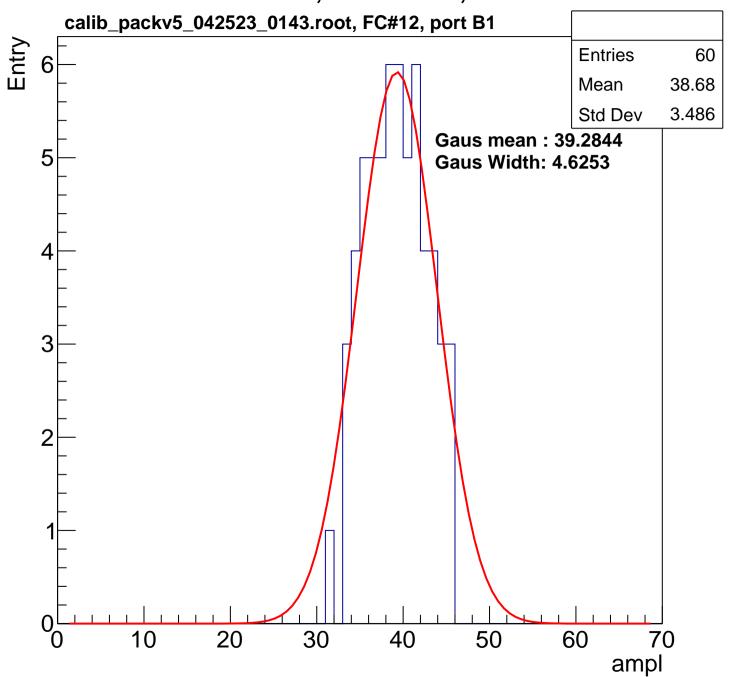


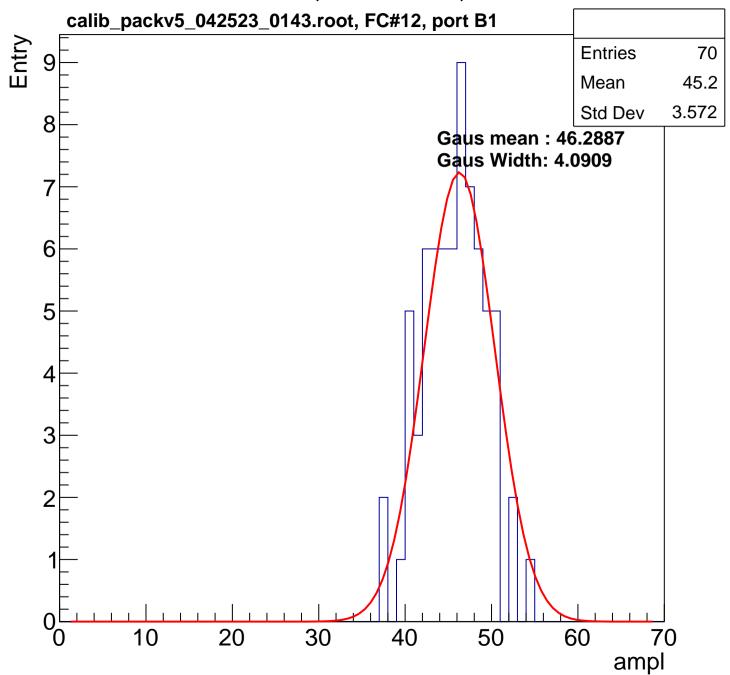


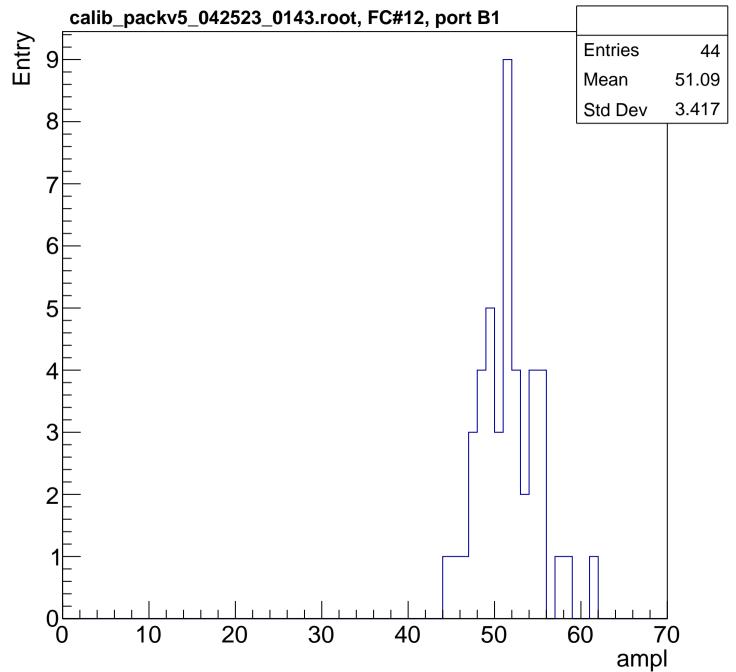


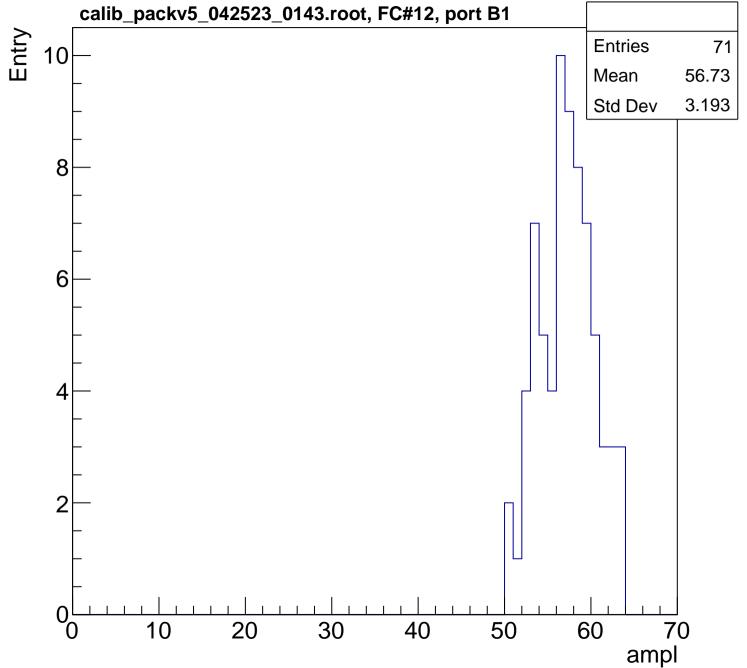
B0L102S, U3-ch48, adc7 calib_packv5_042523_0143.root, FC#12, port B1 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

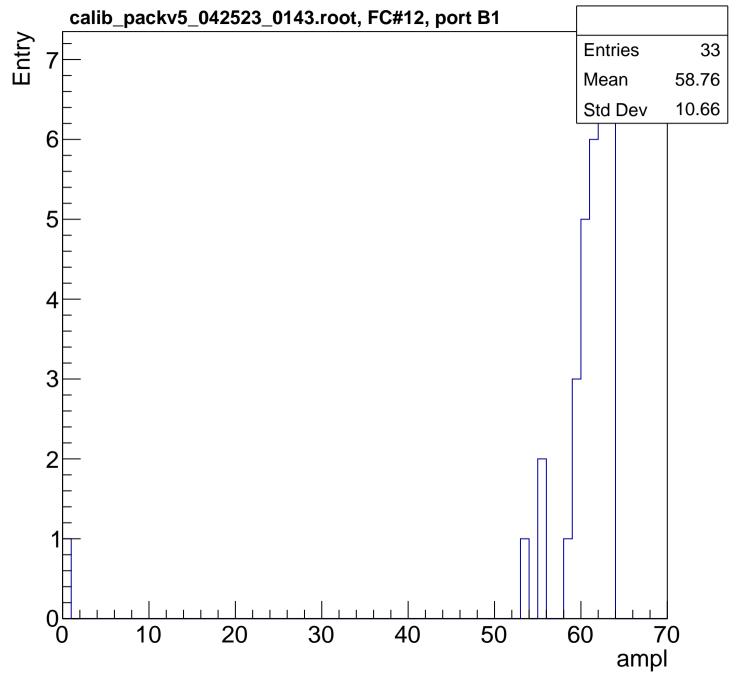


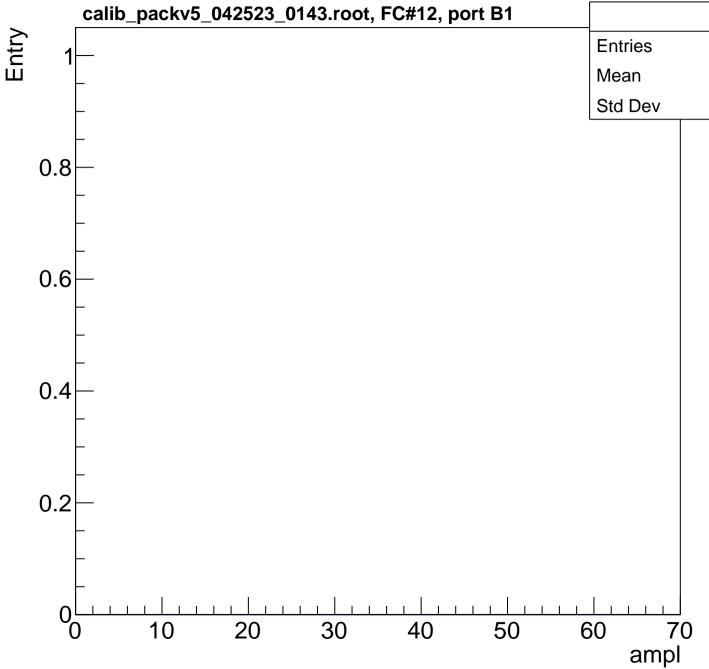


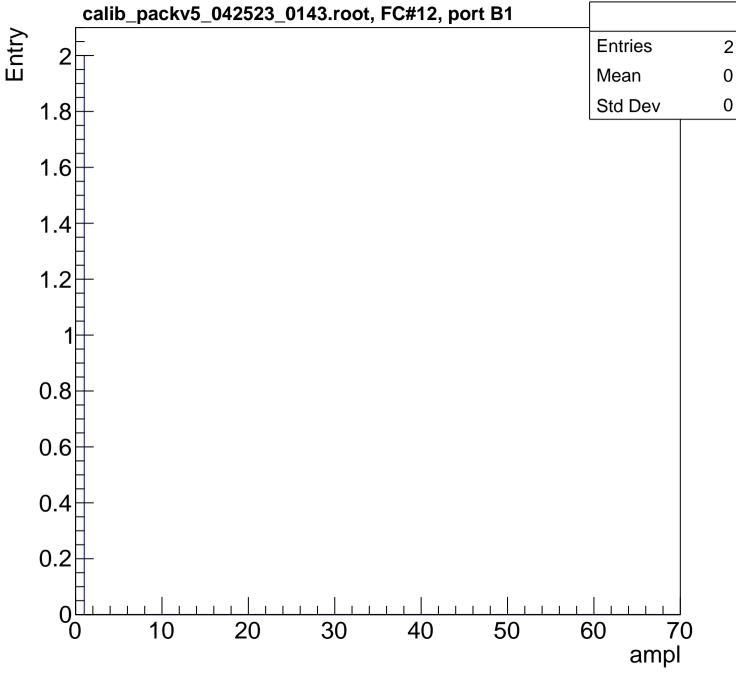


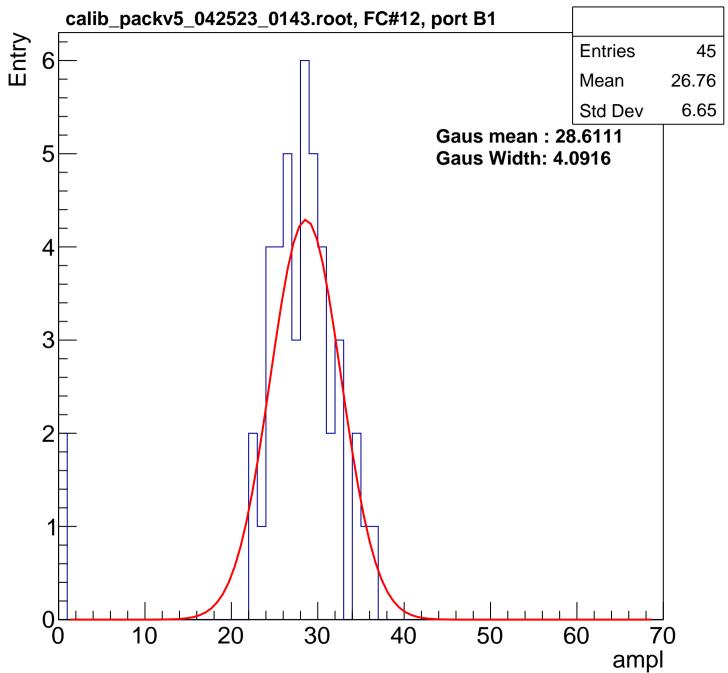


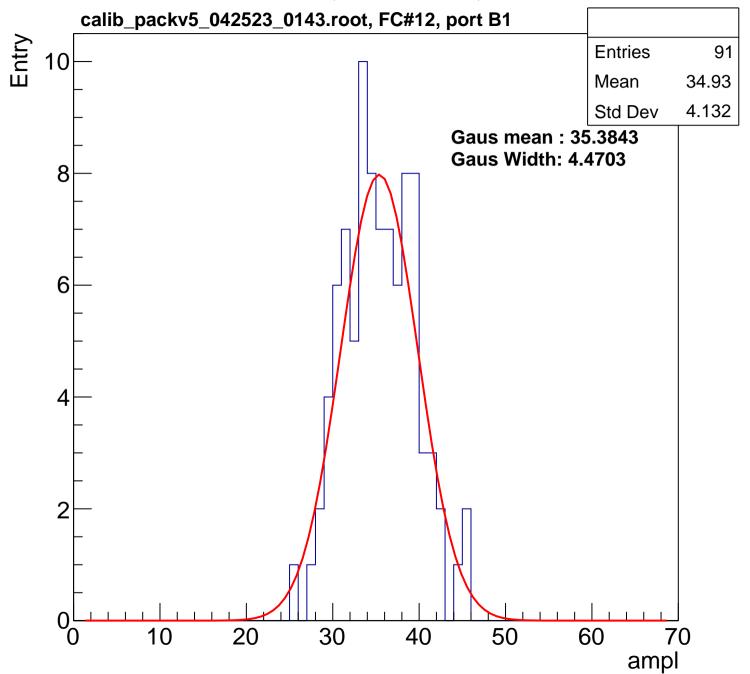


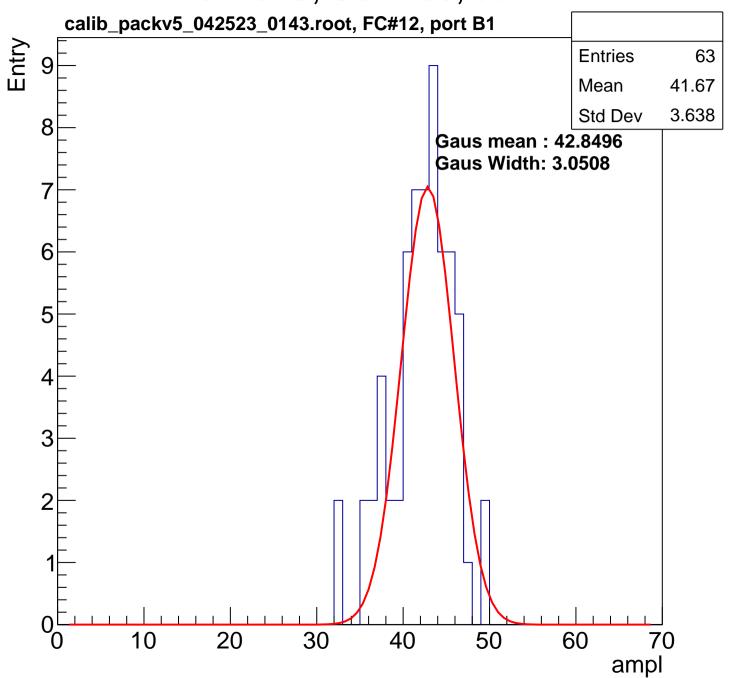


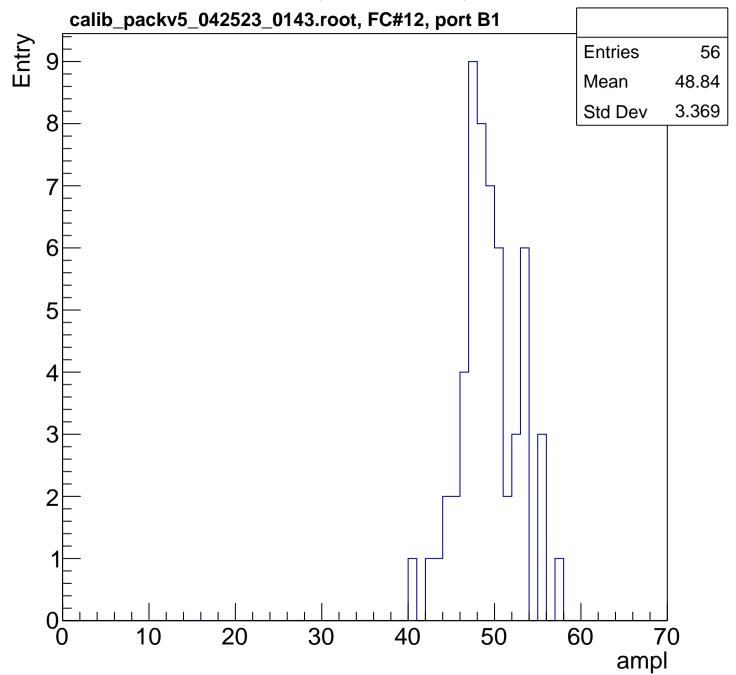


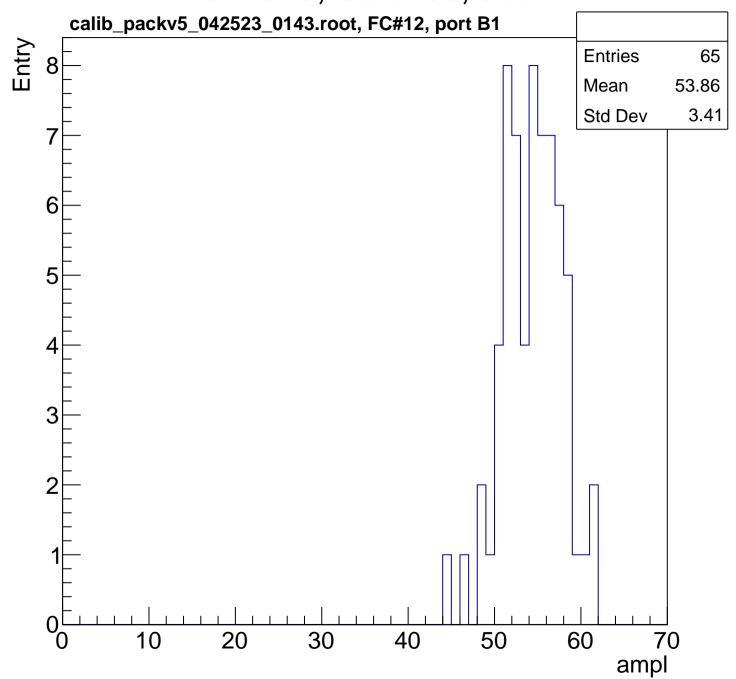


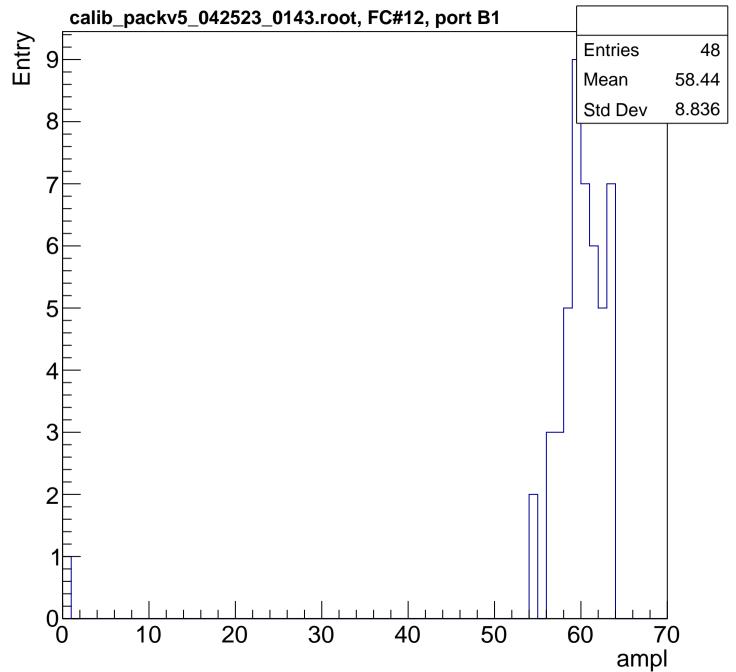


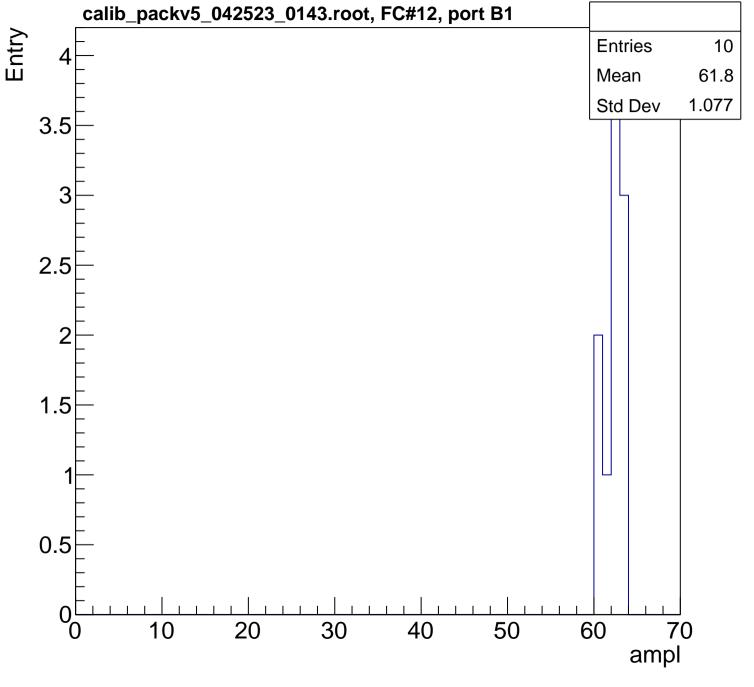


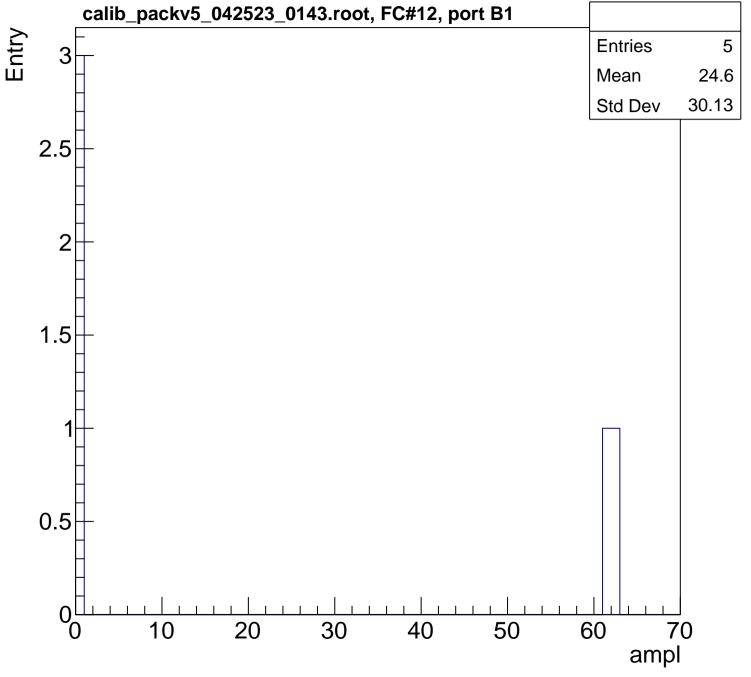


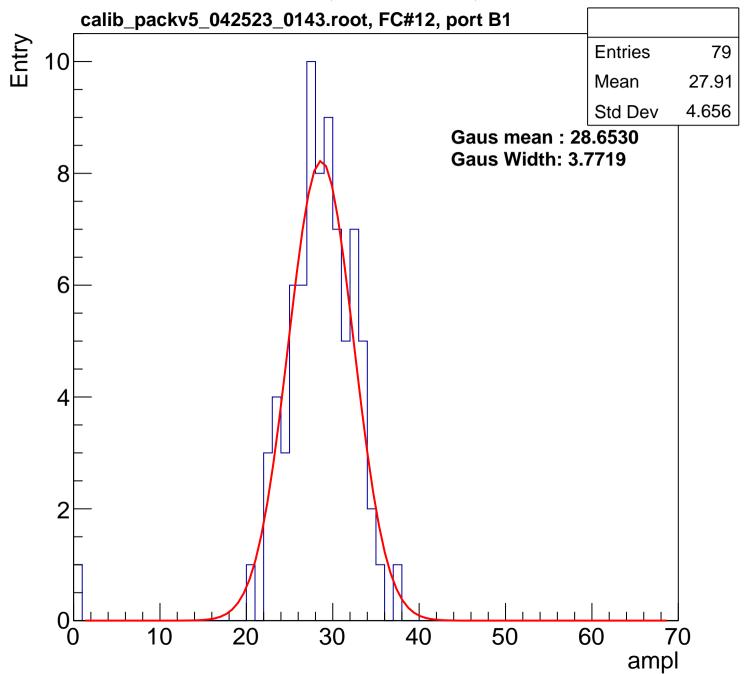


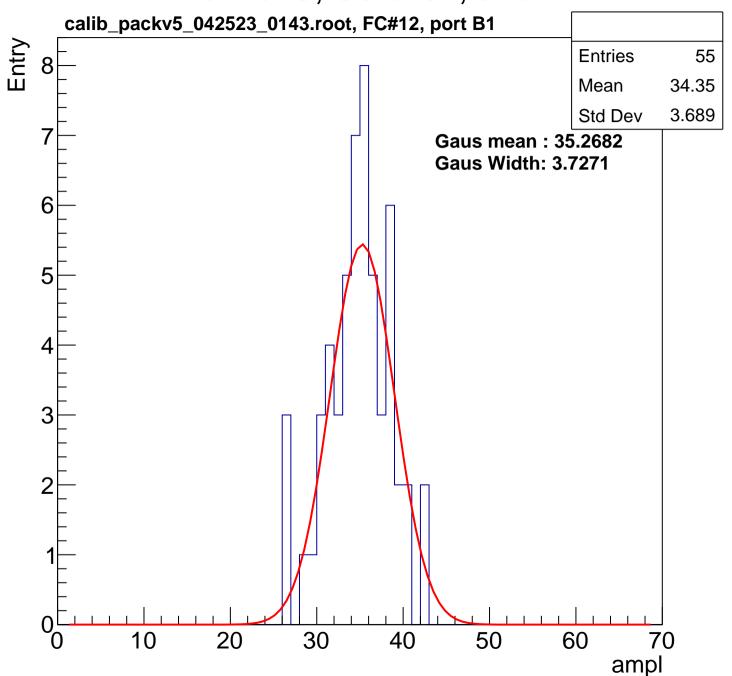


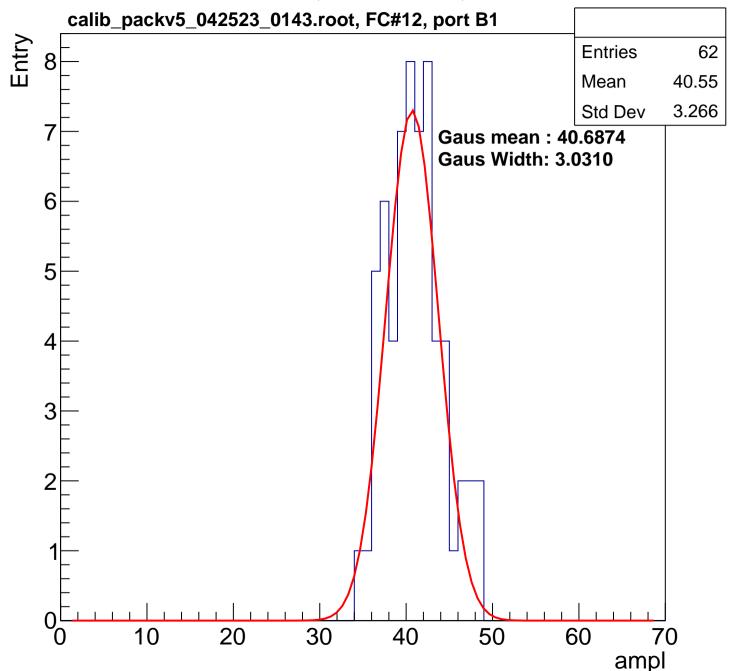


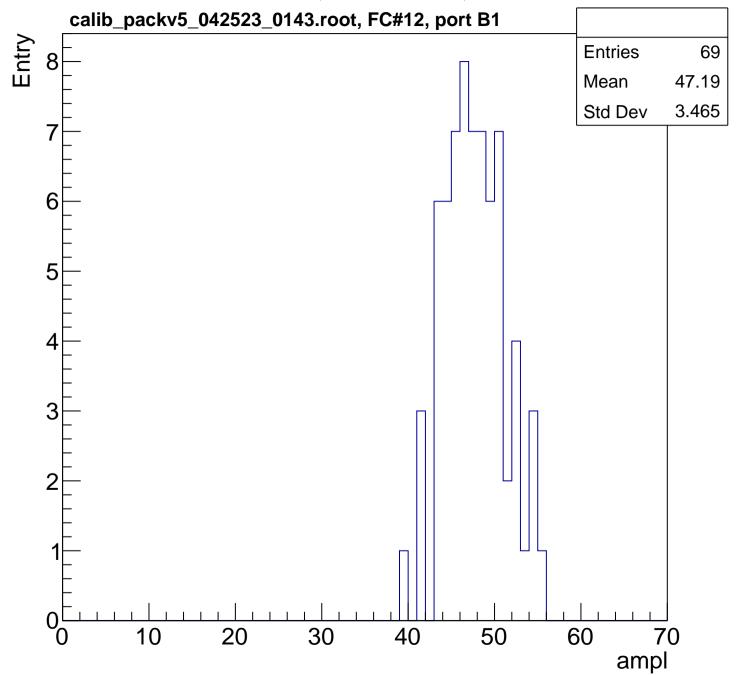


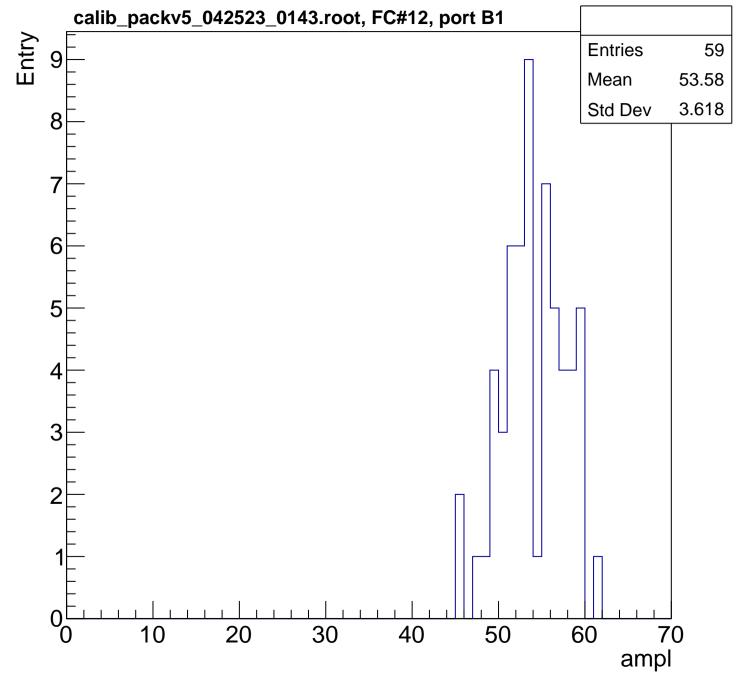


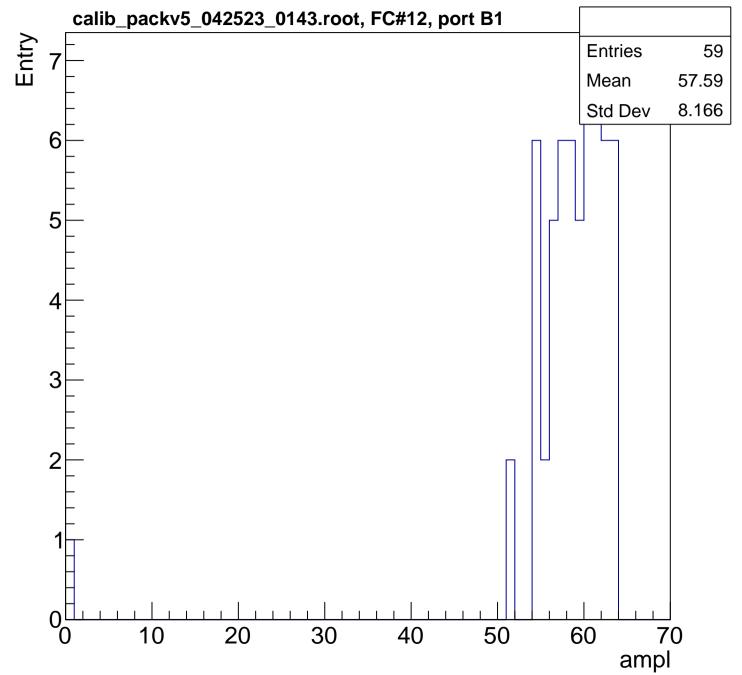


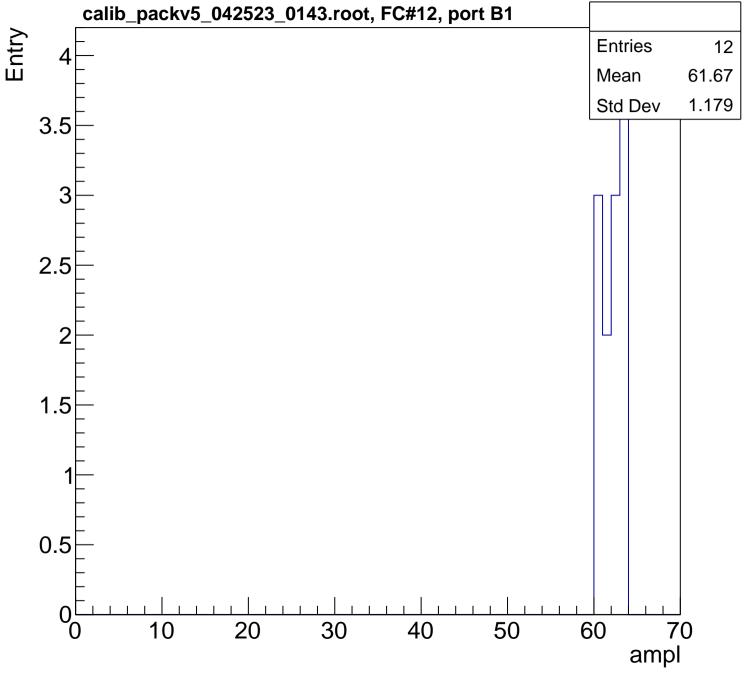


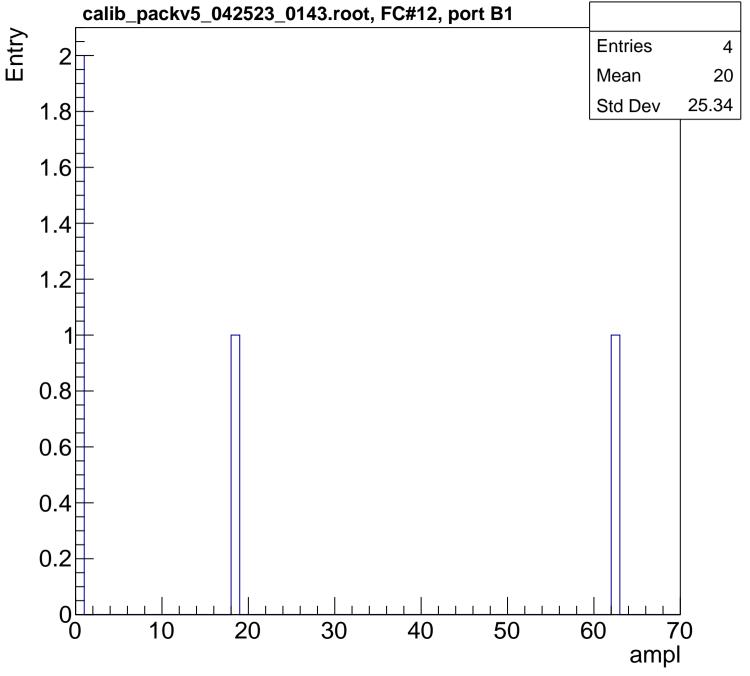


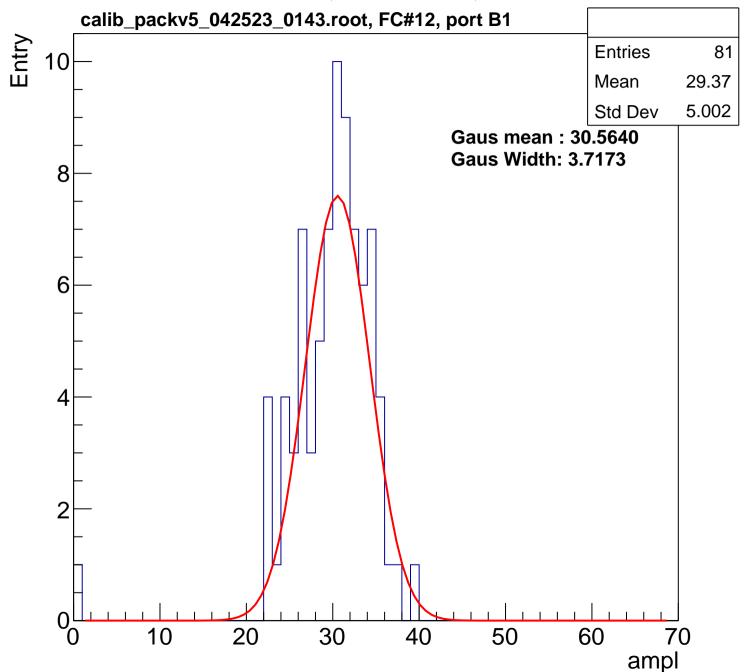


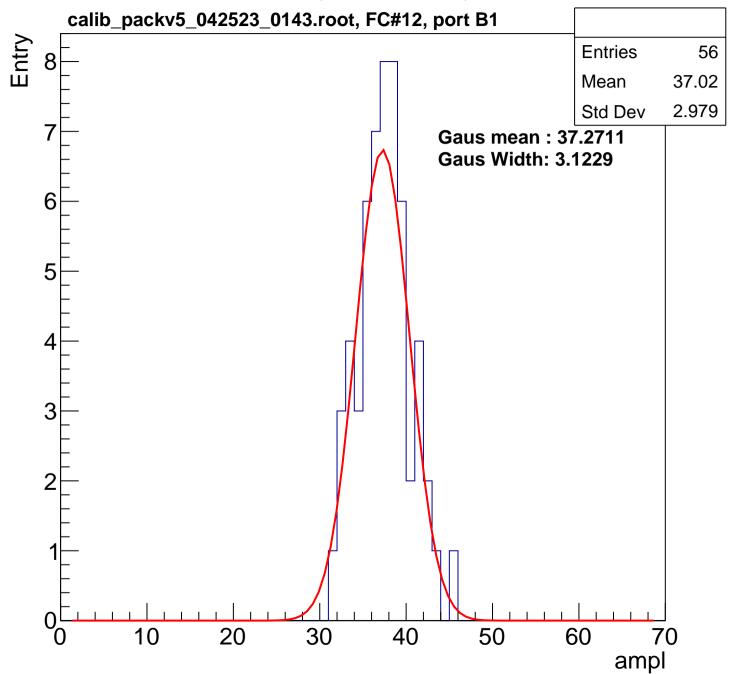


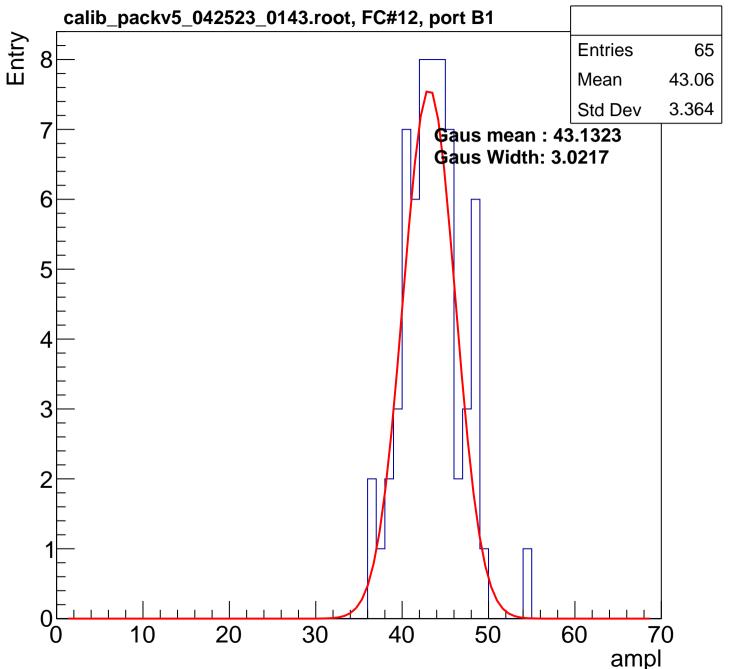


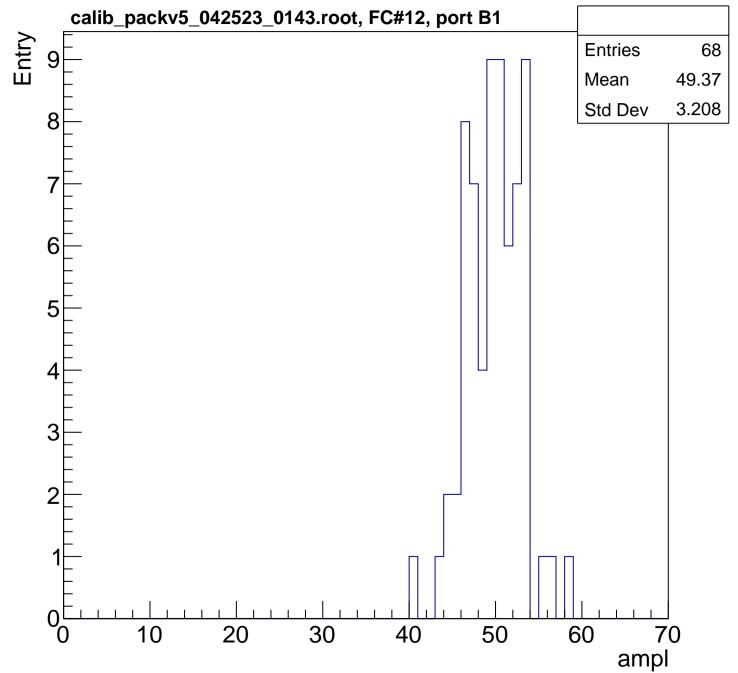


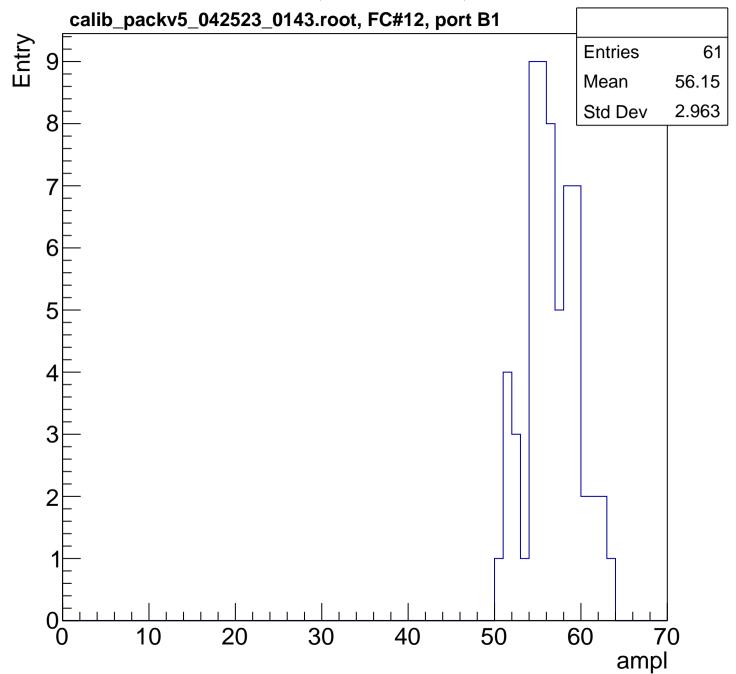


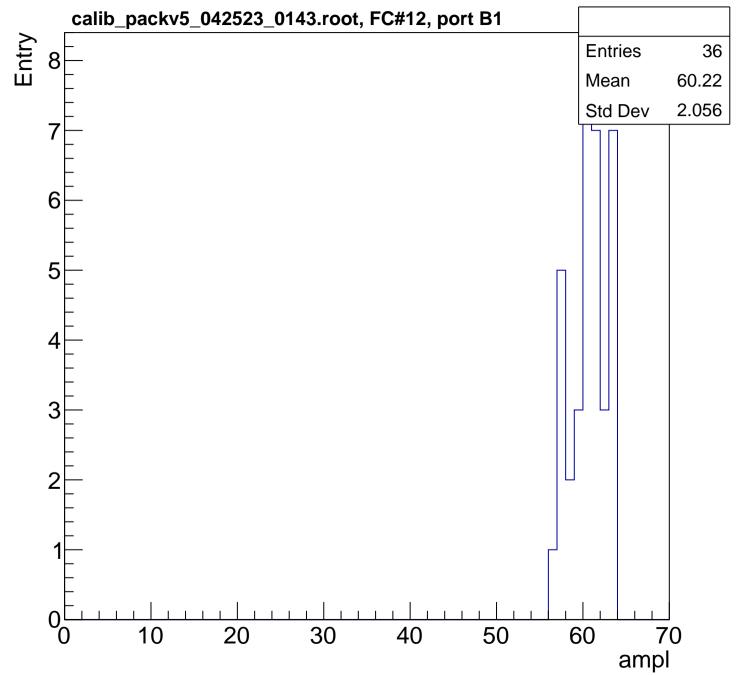


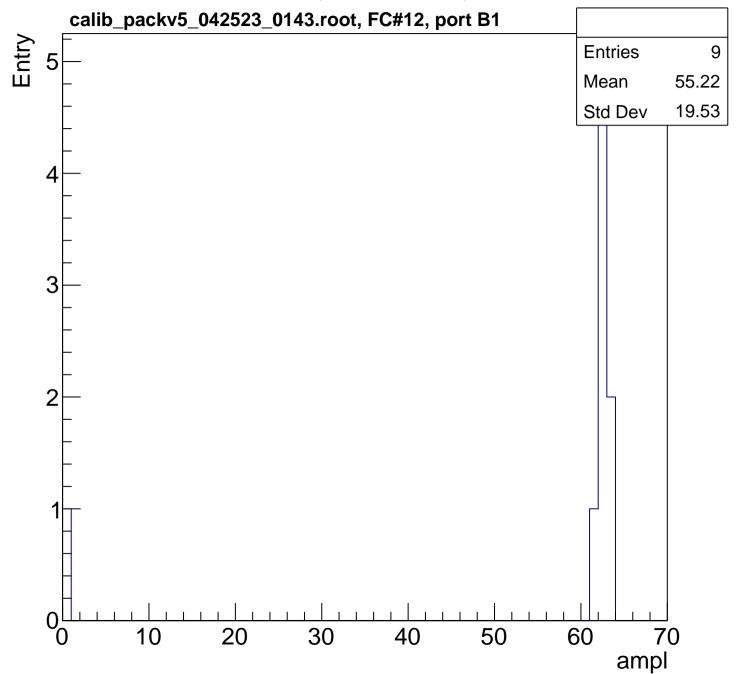


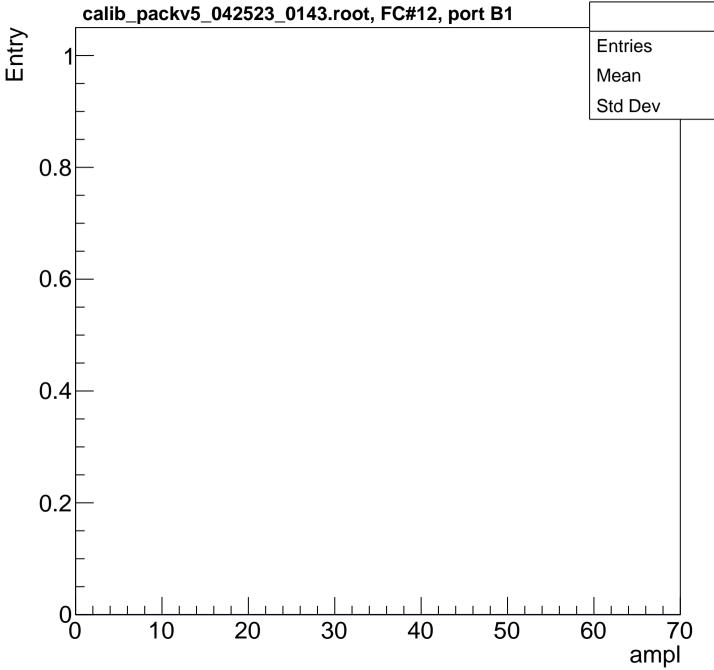


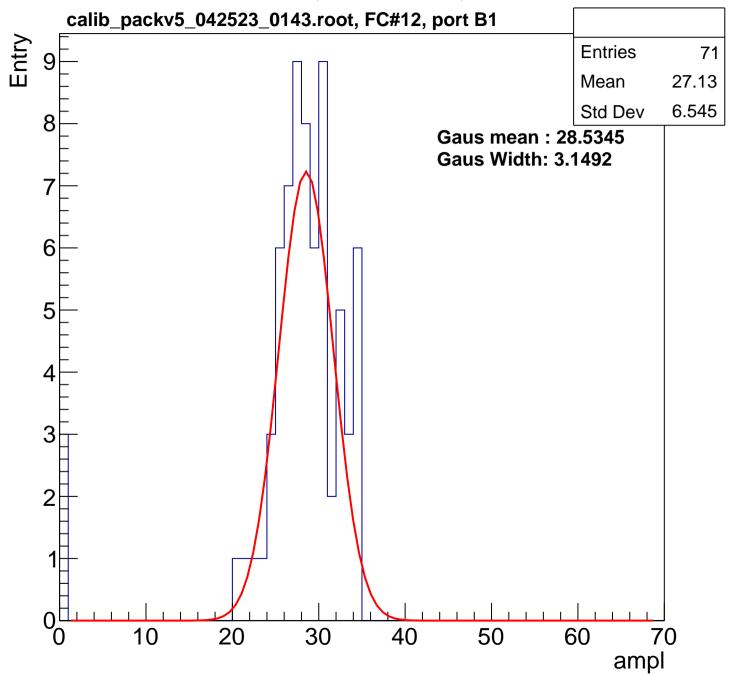


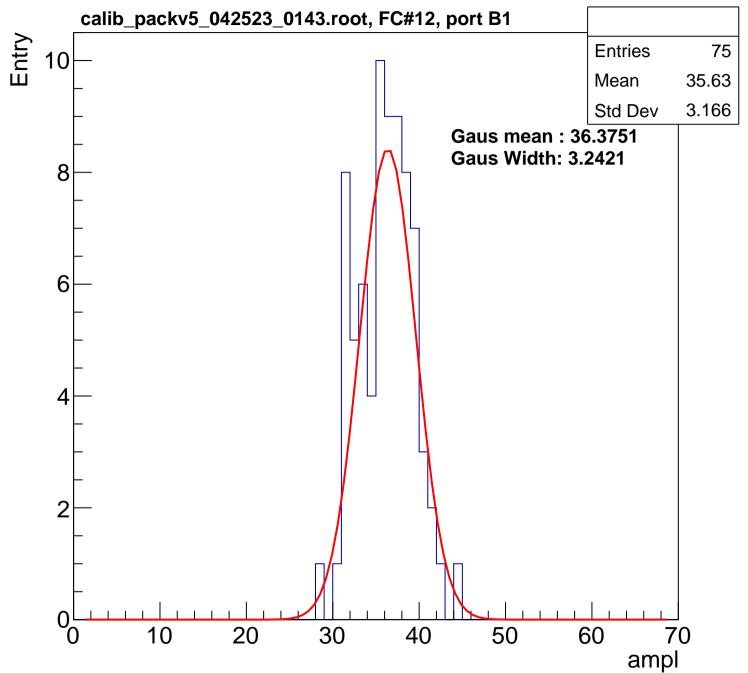


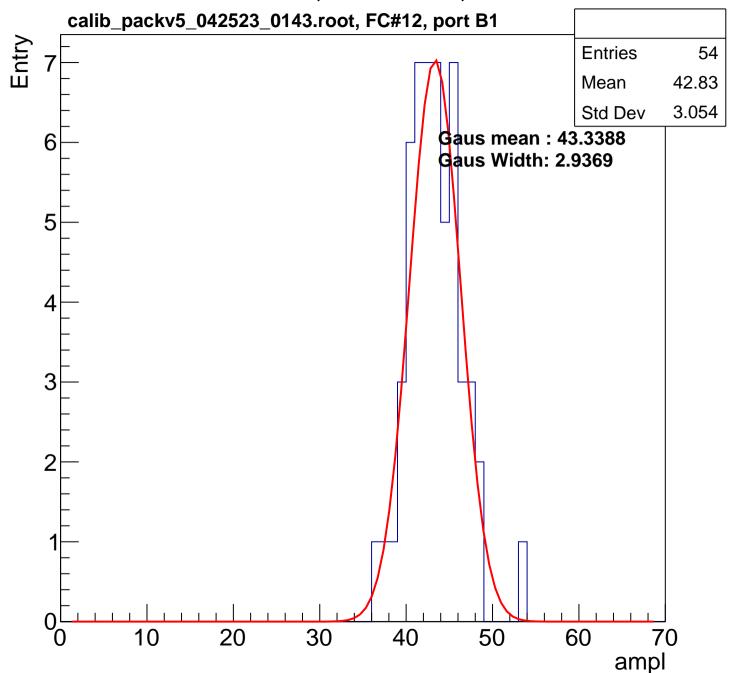


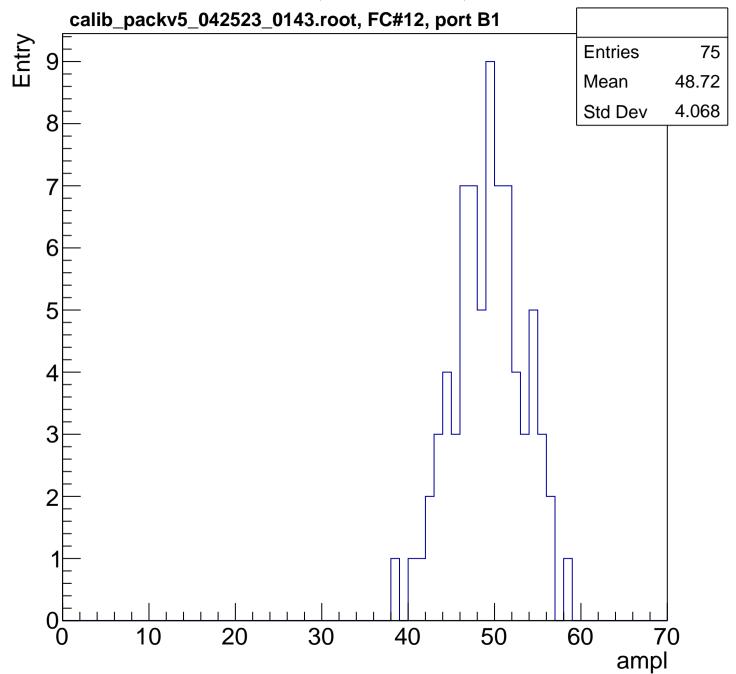


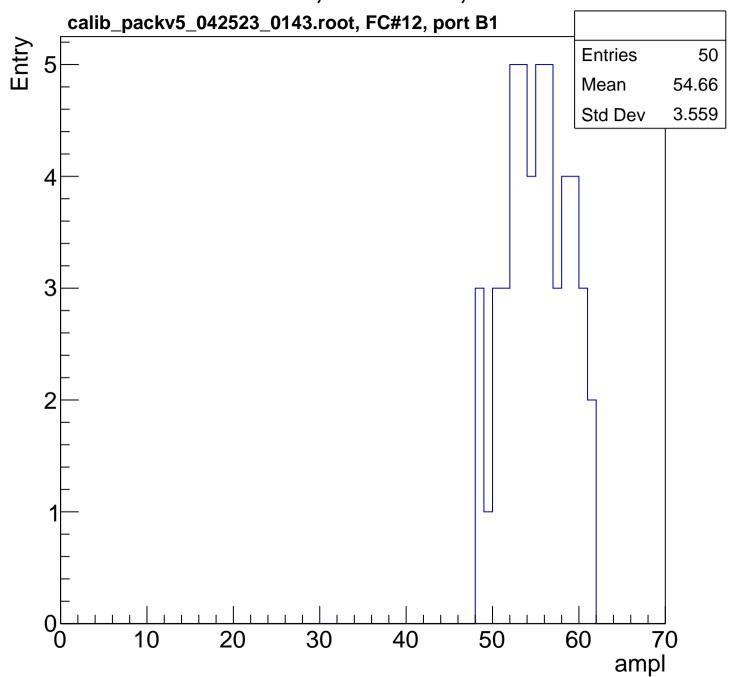


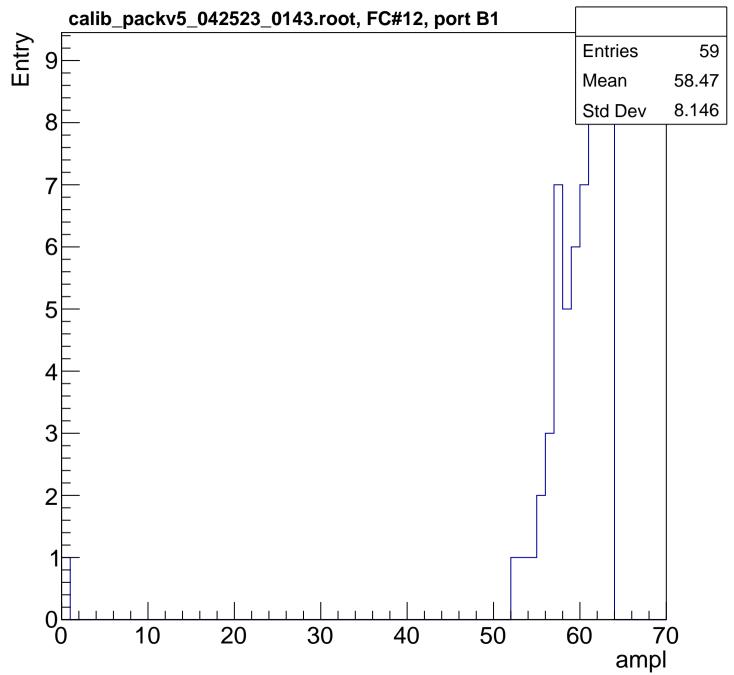


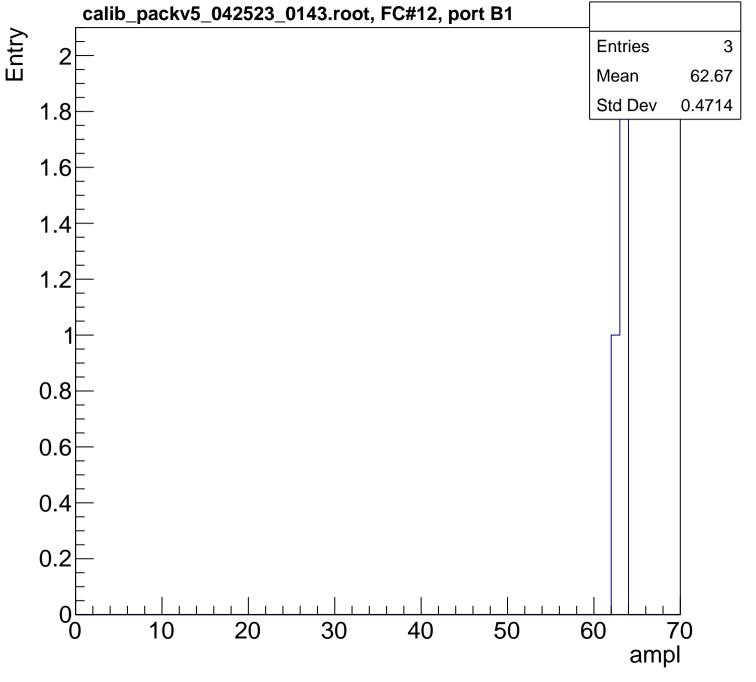


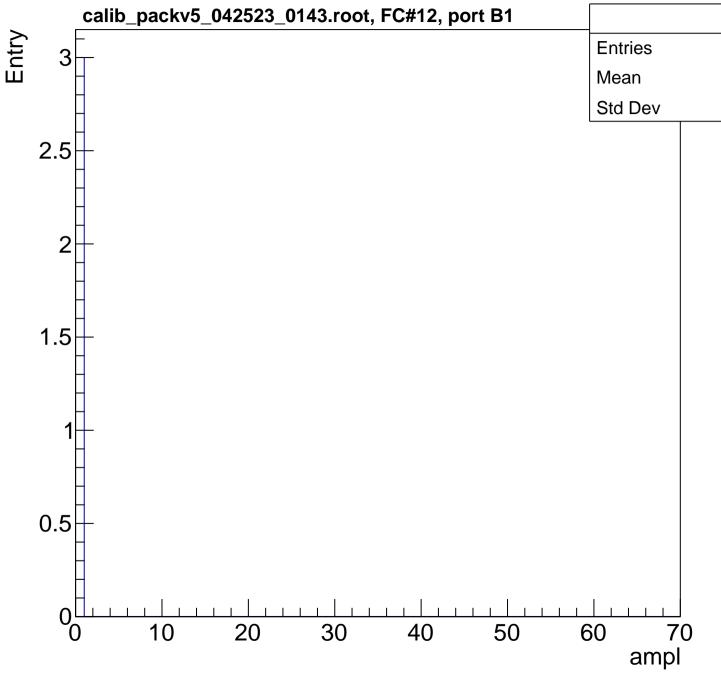


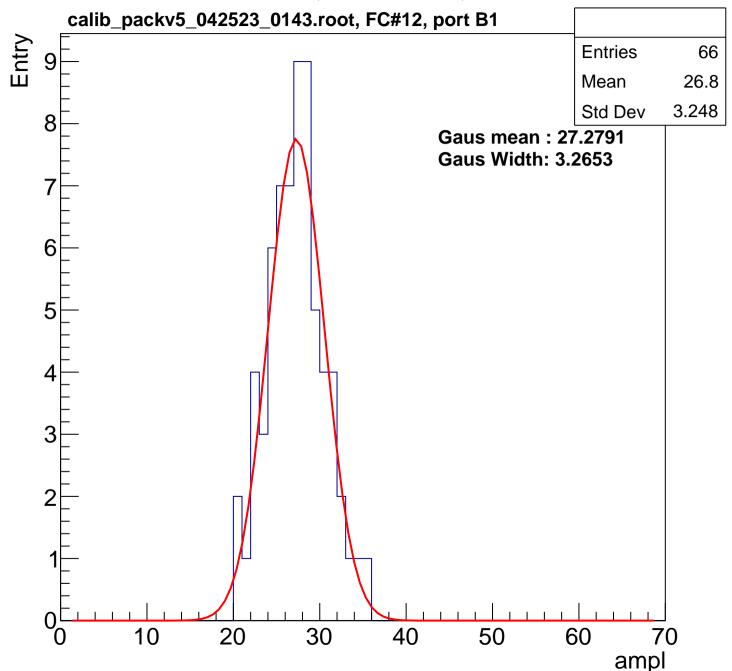


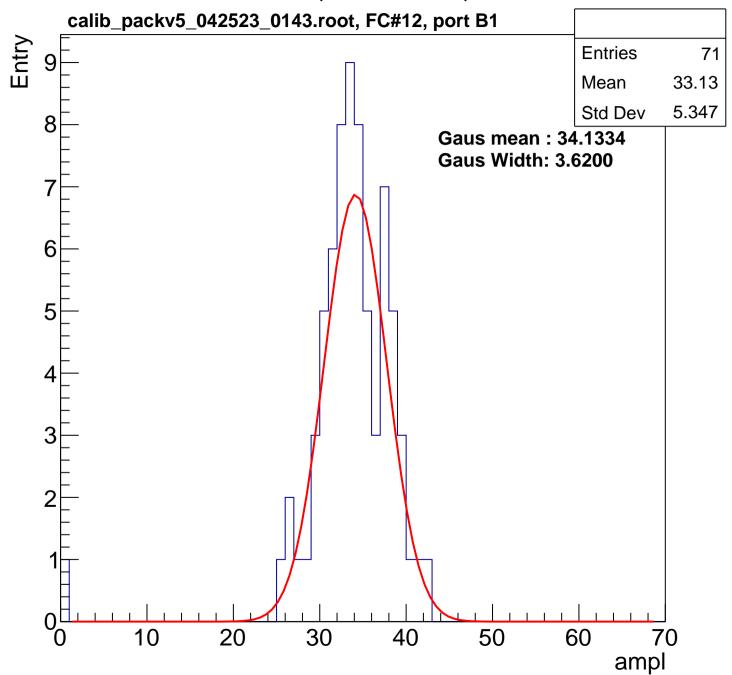


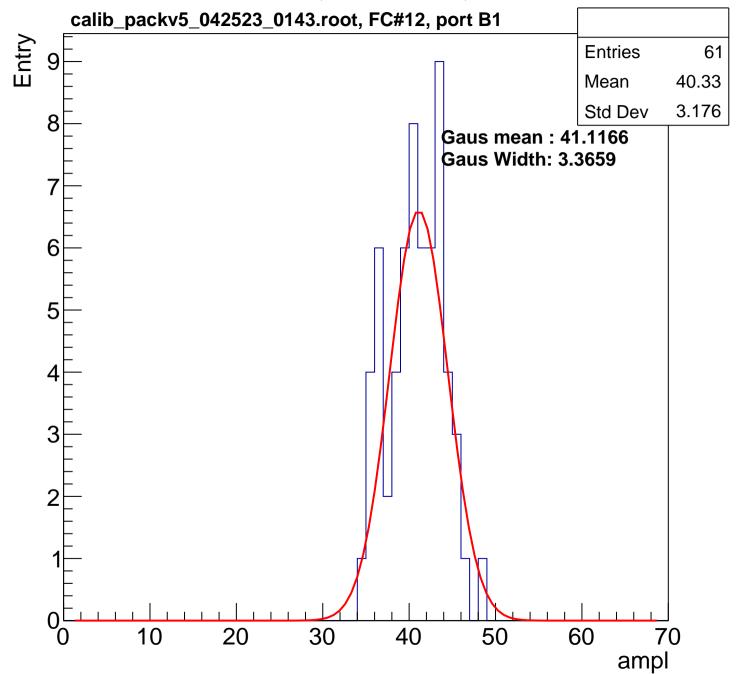


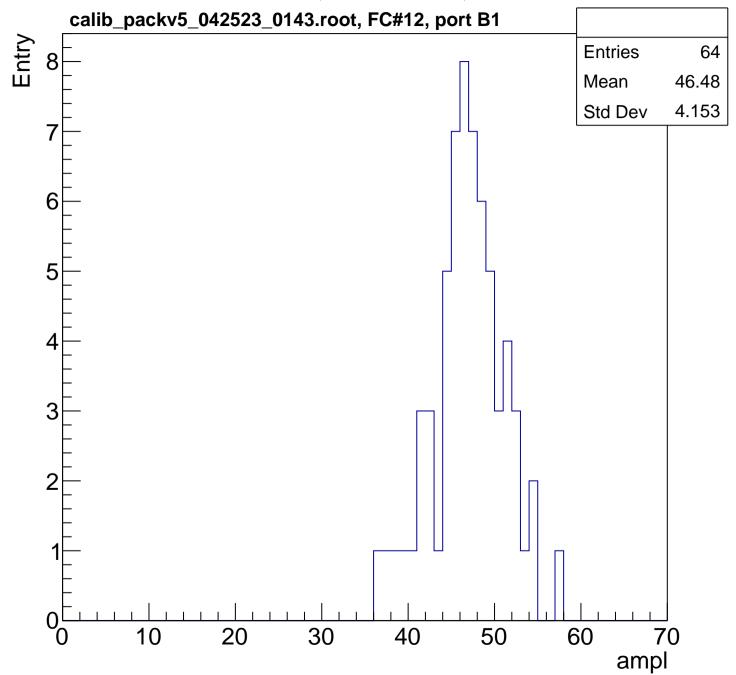


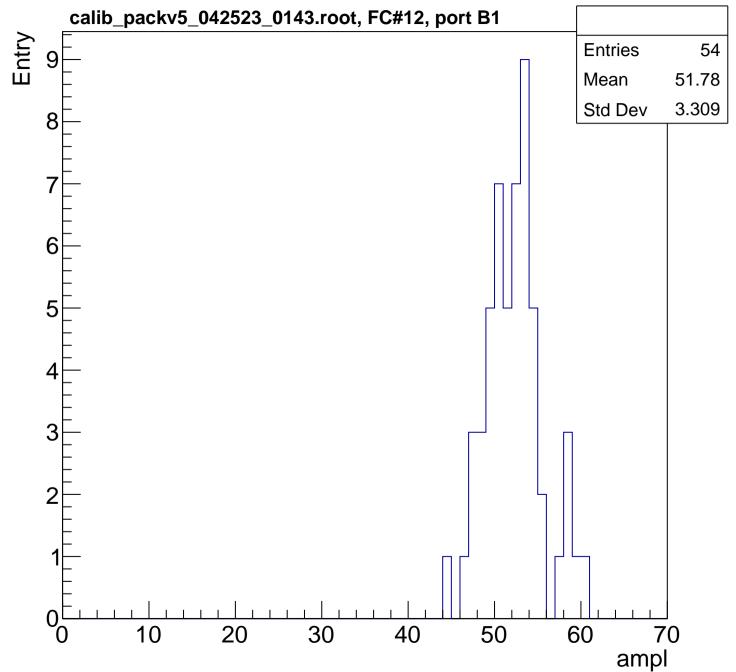


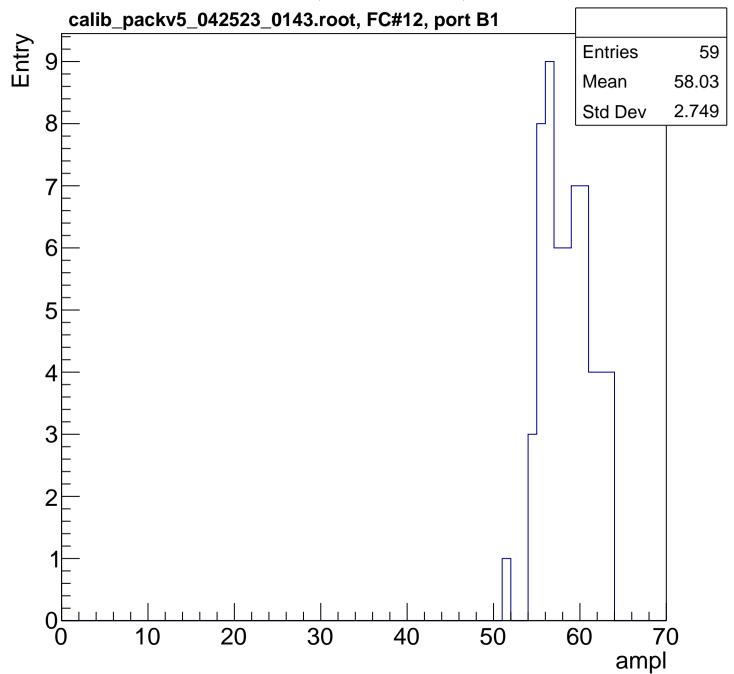


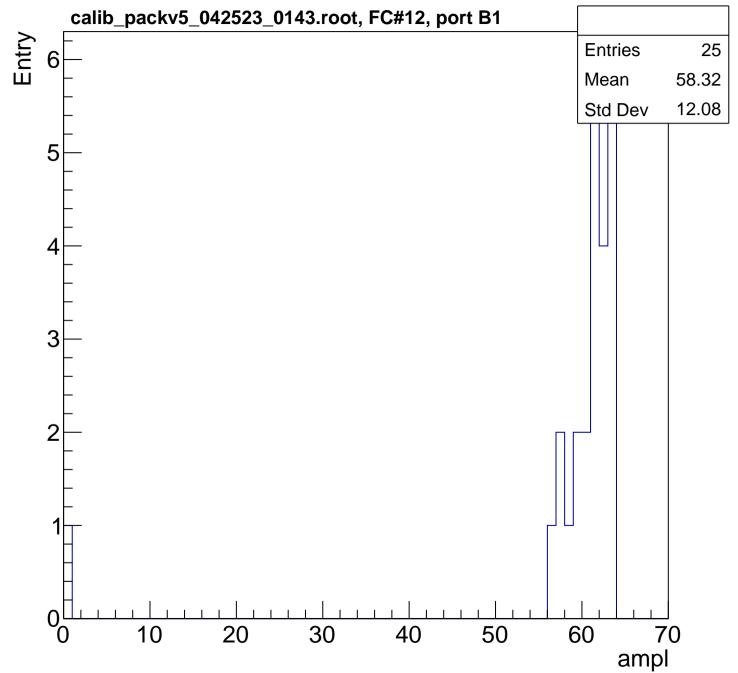


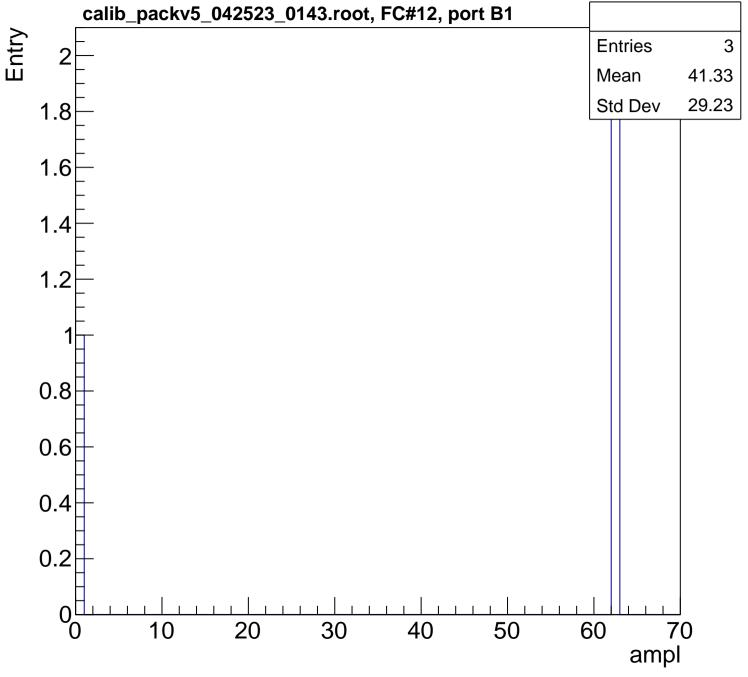


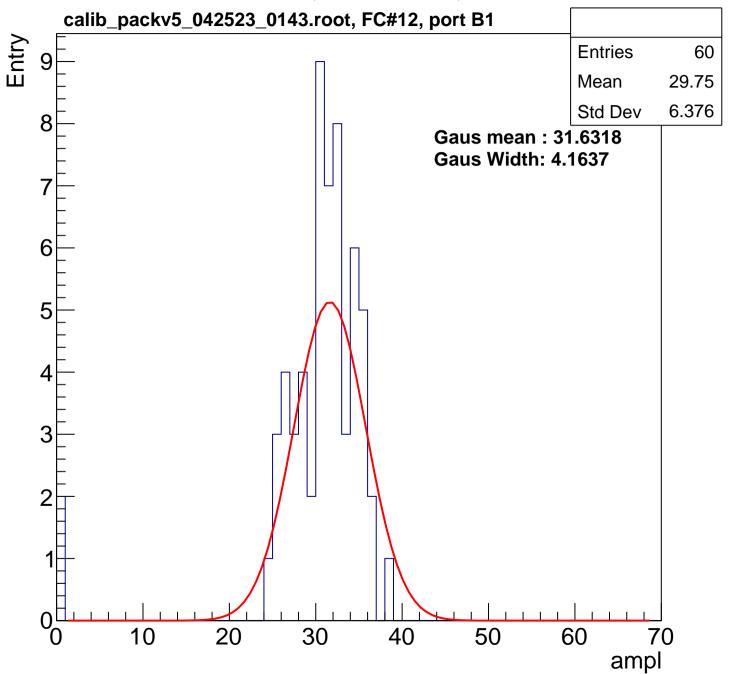


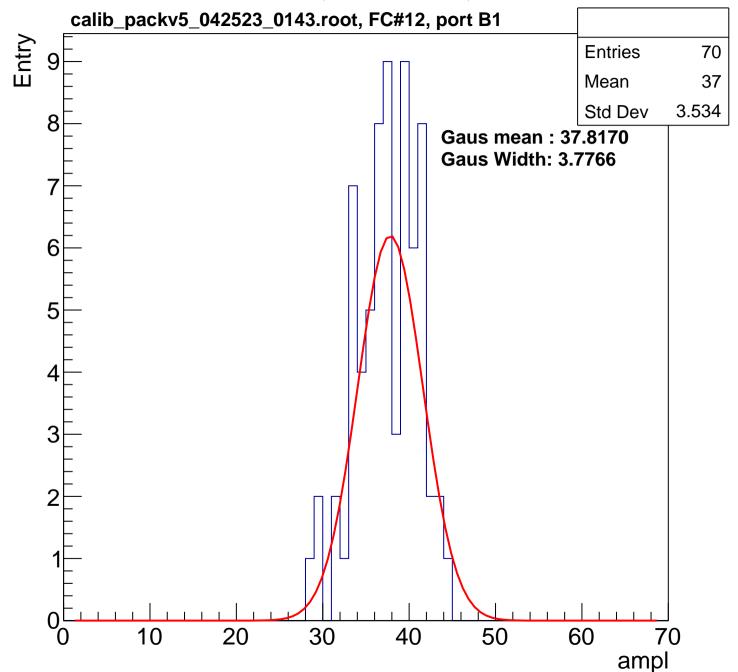


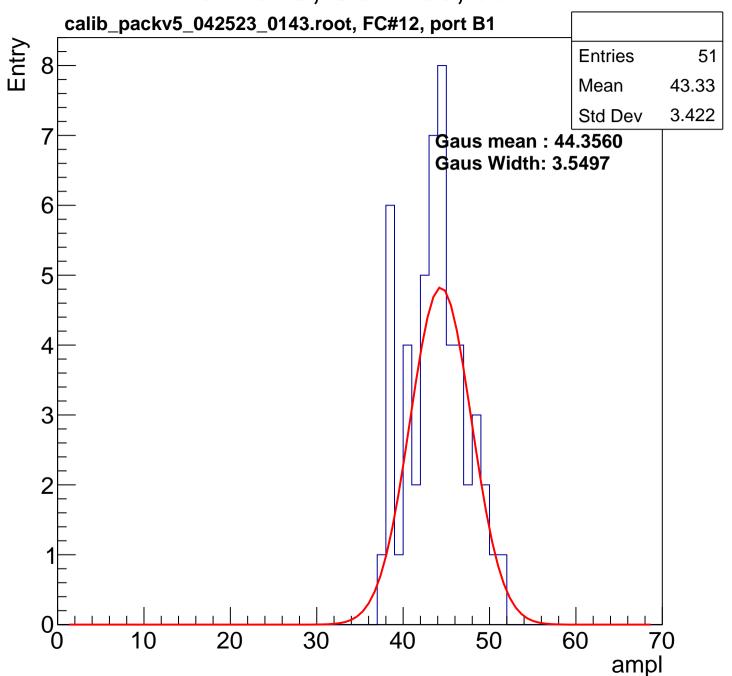


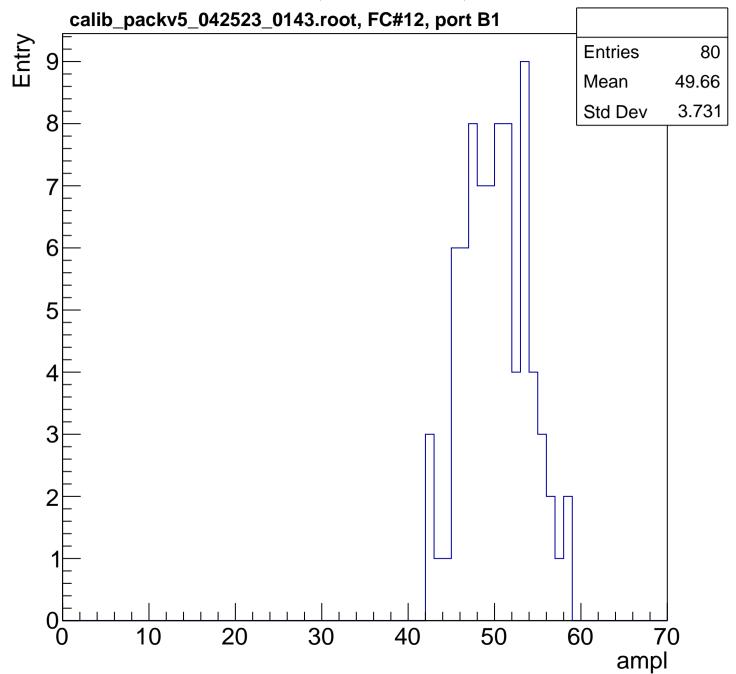


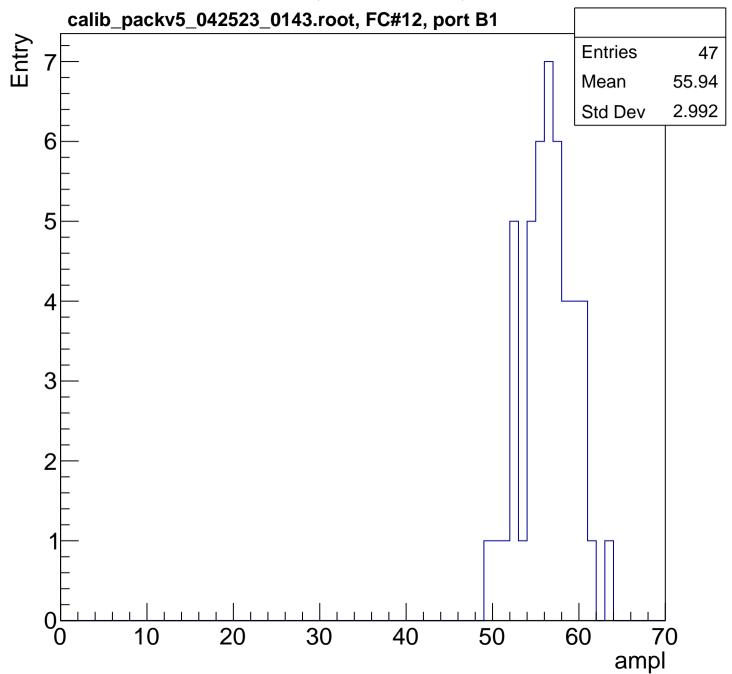


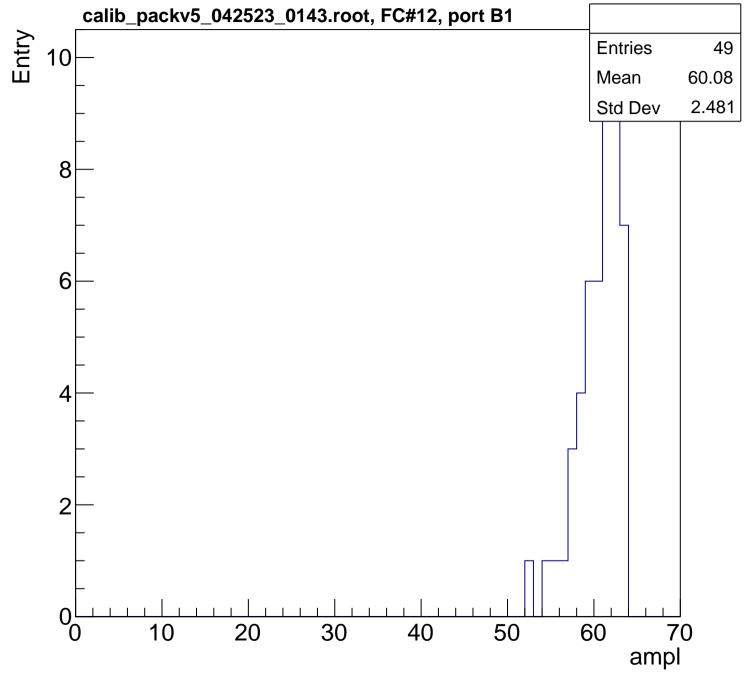


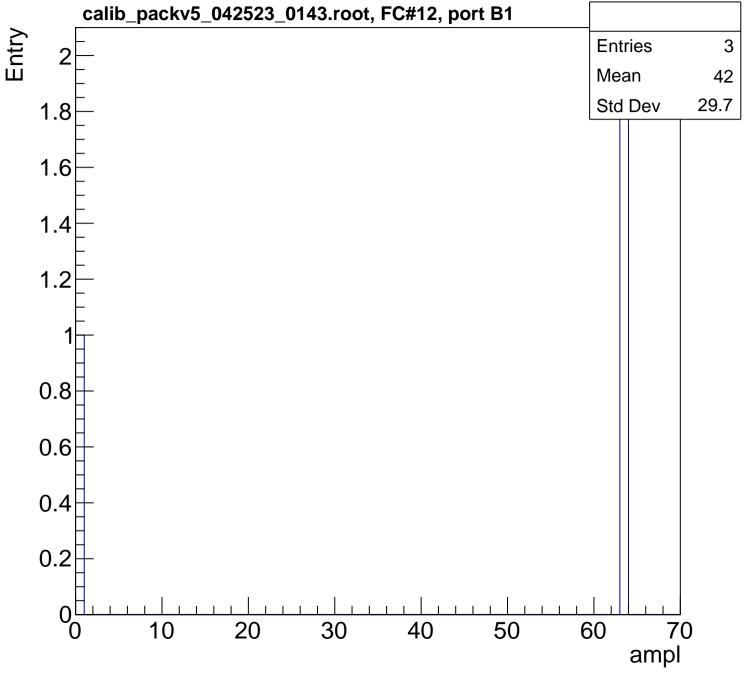




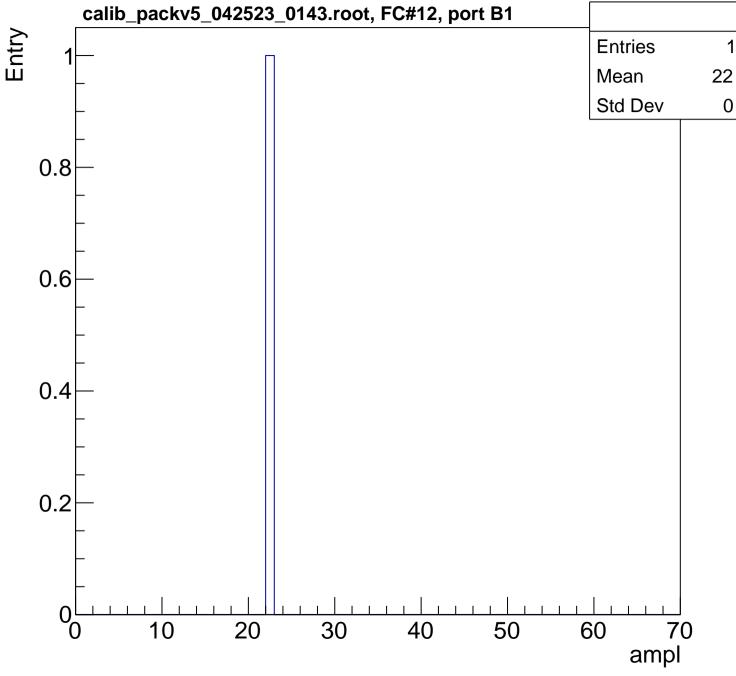


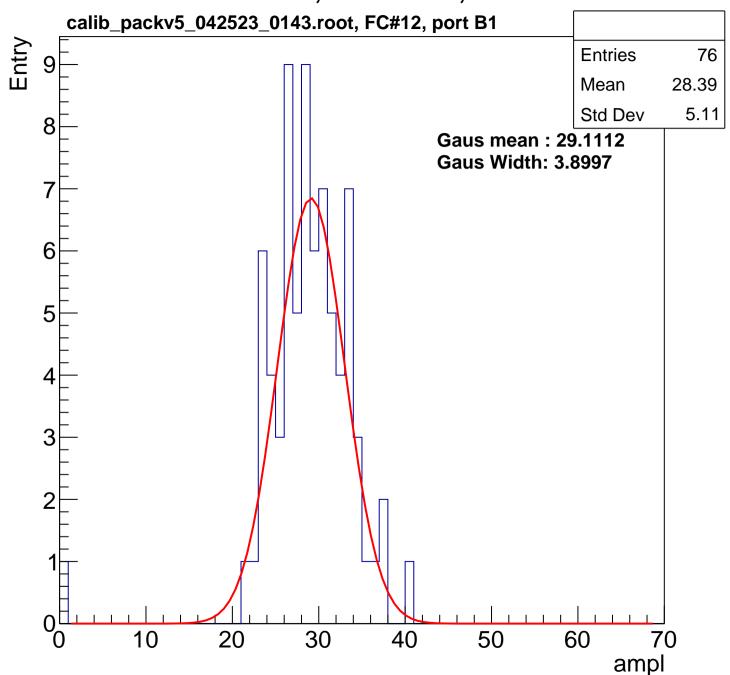


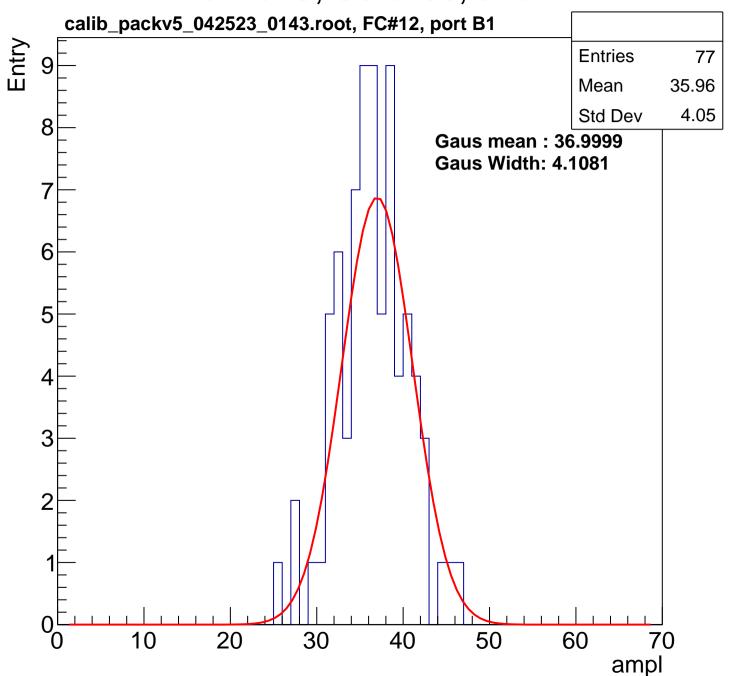


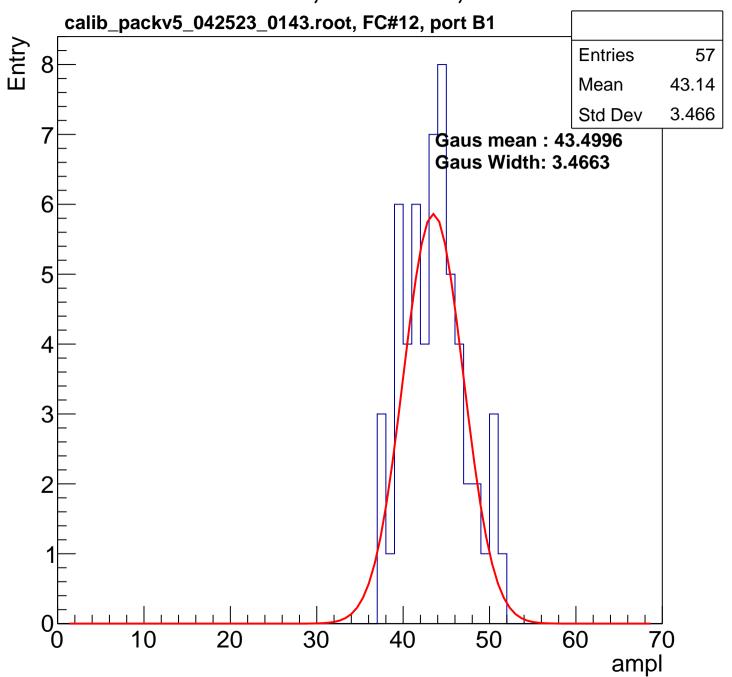


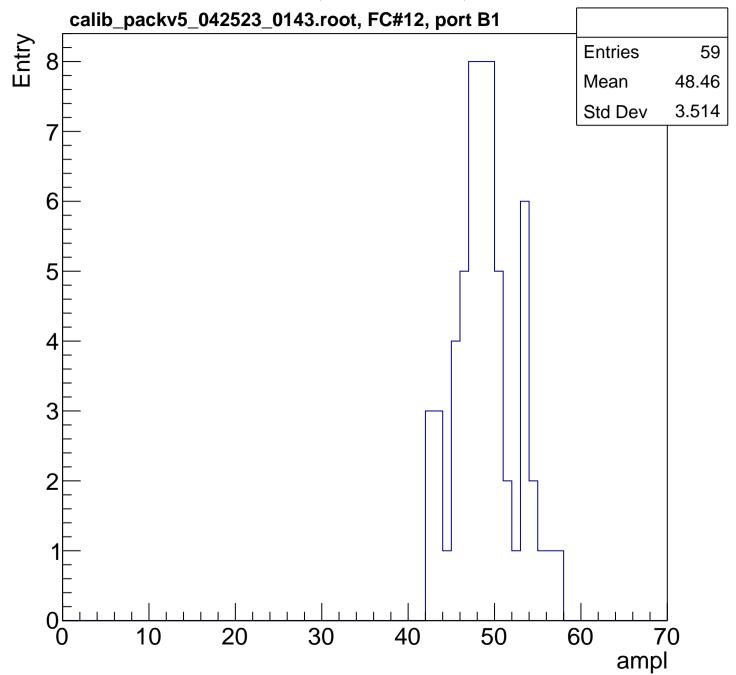
0

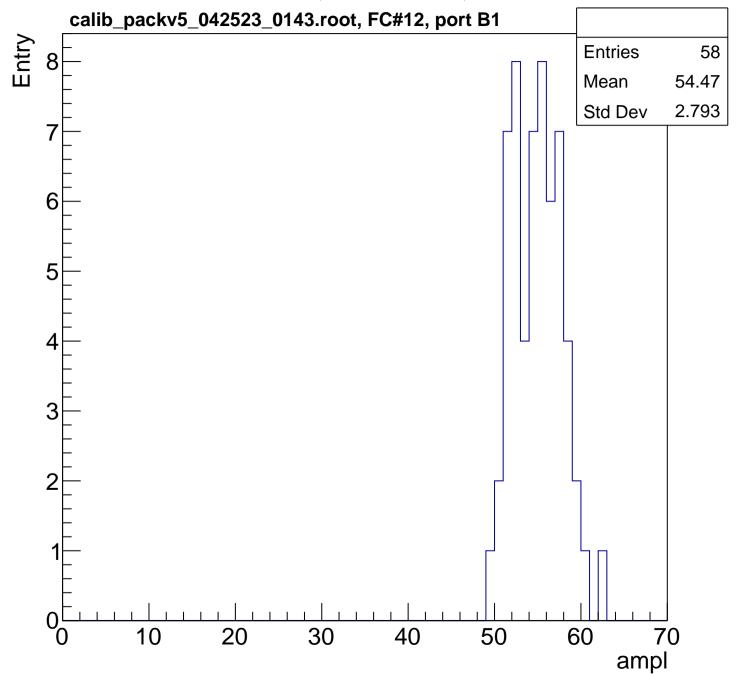


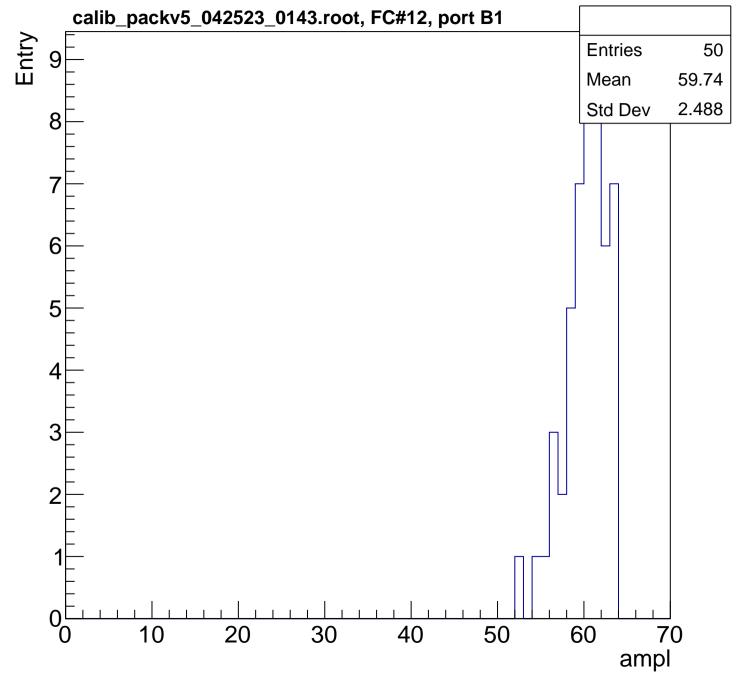


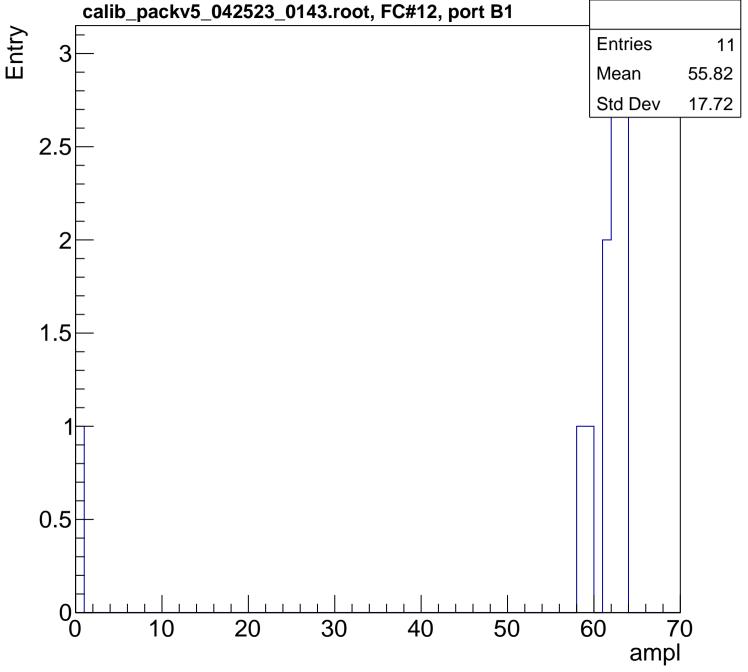




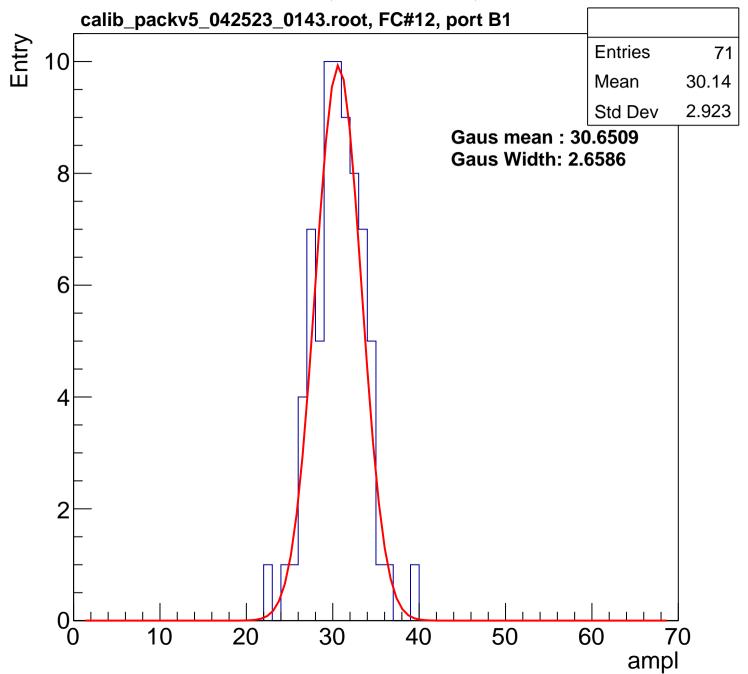


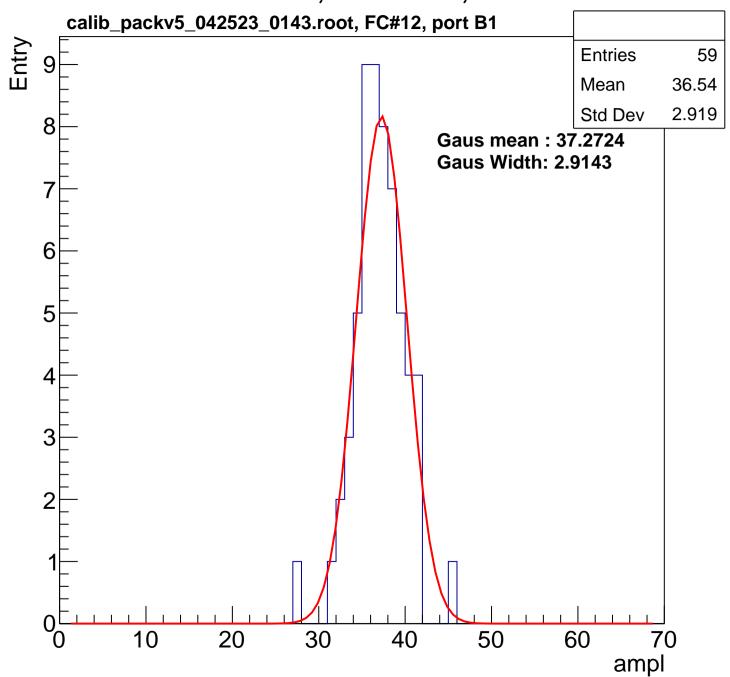


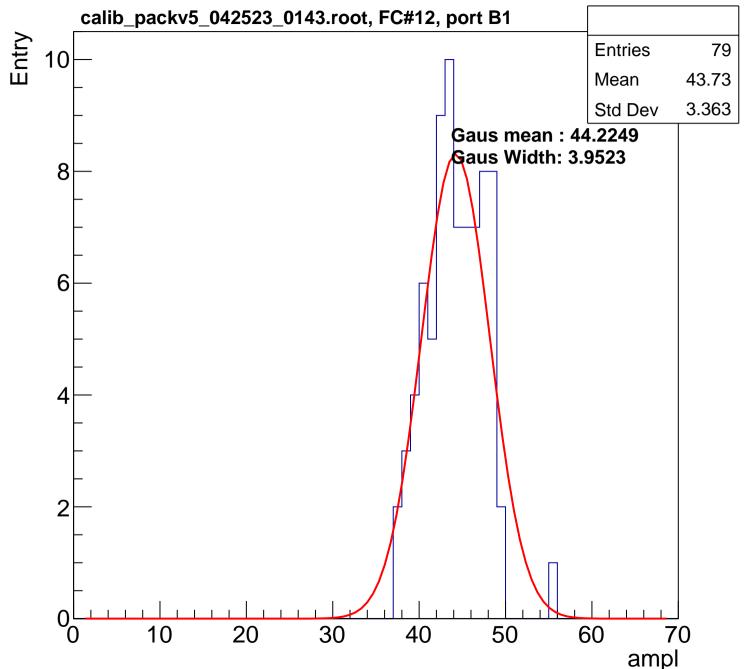


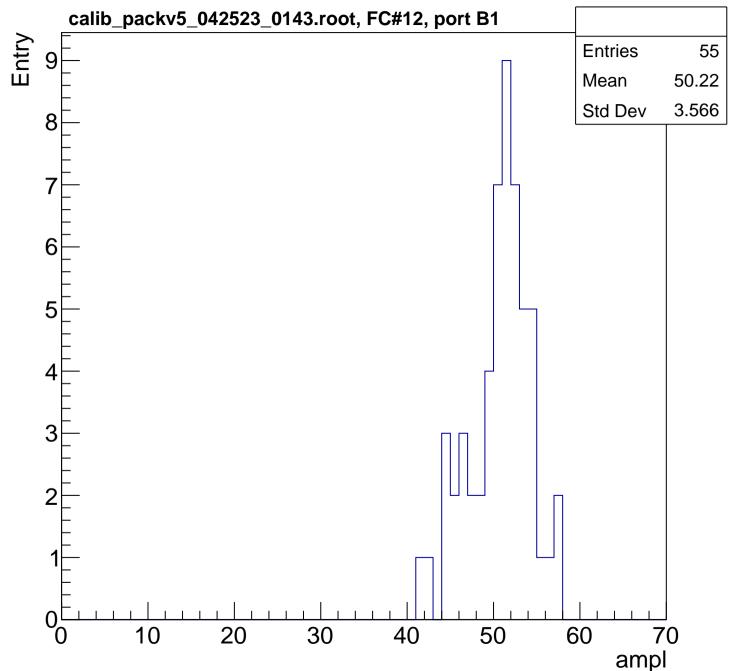


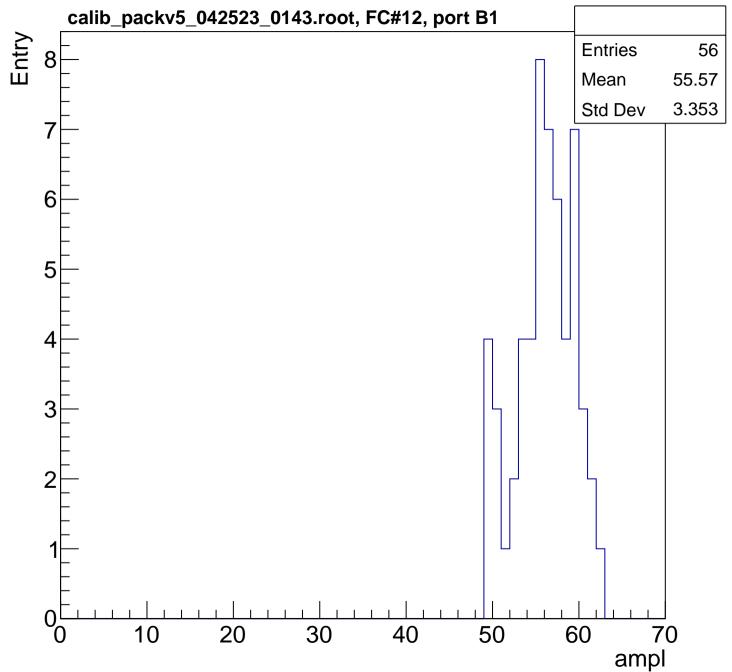
B0L102S, U3-ch56, adc7 calib_packv5_042523_0143.root, FC#12, port B1 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

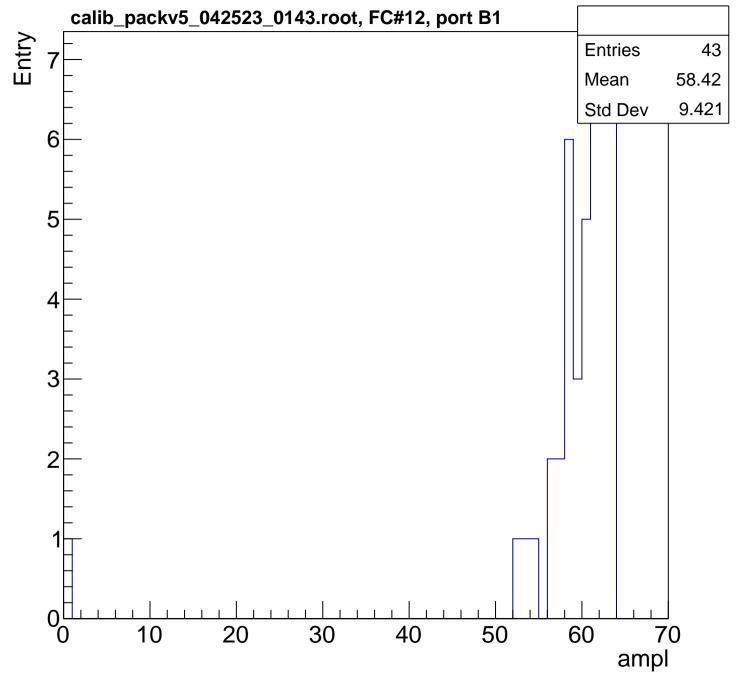


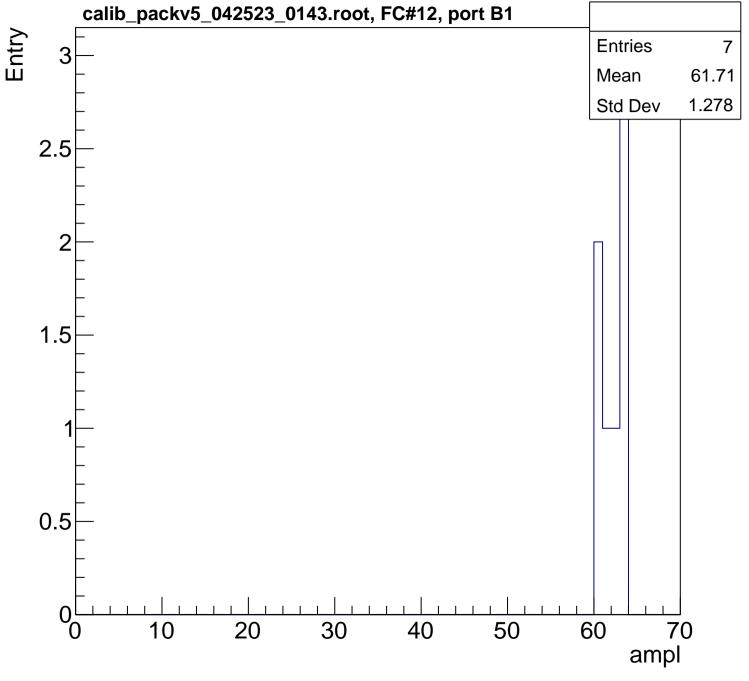




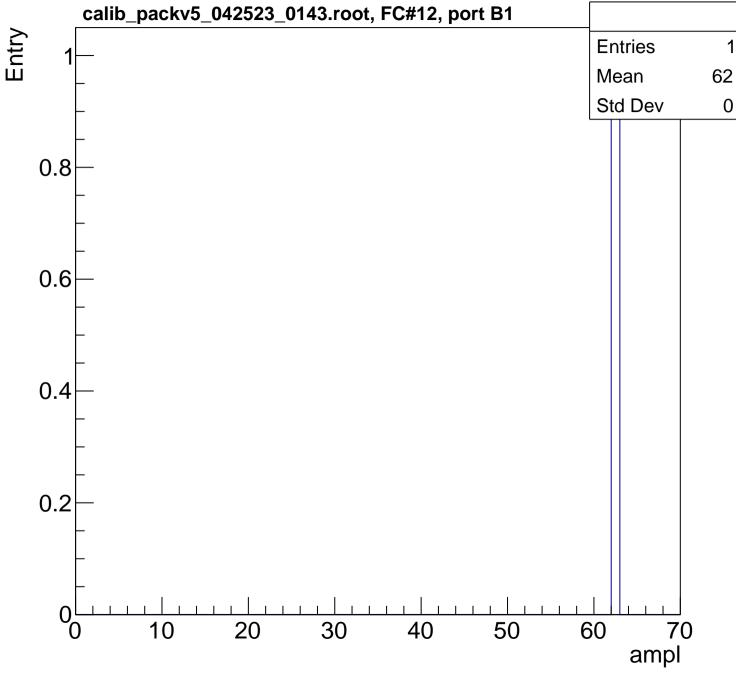


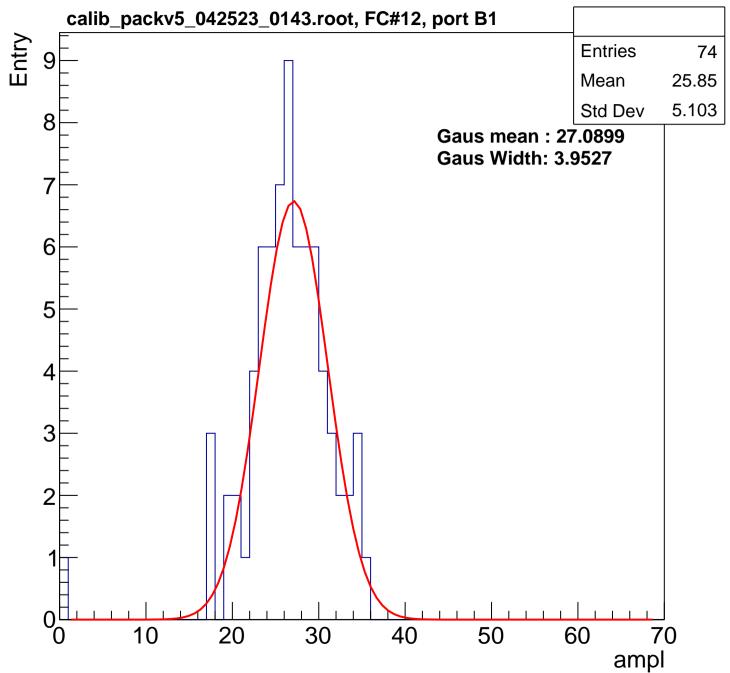


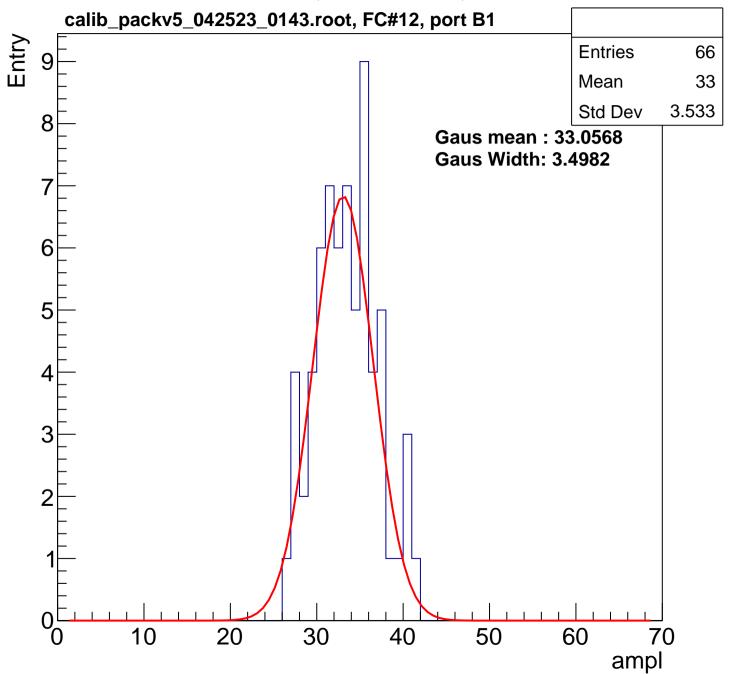


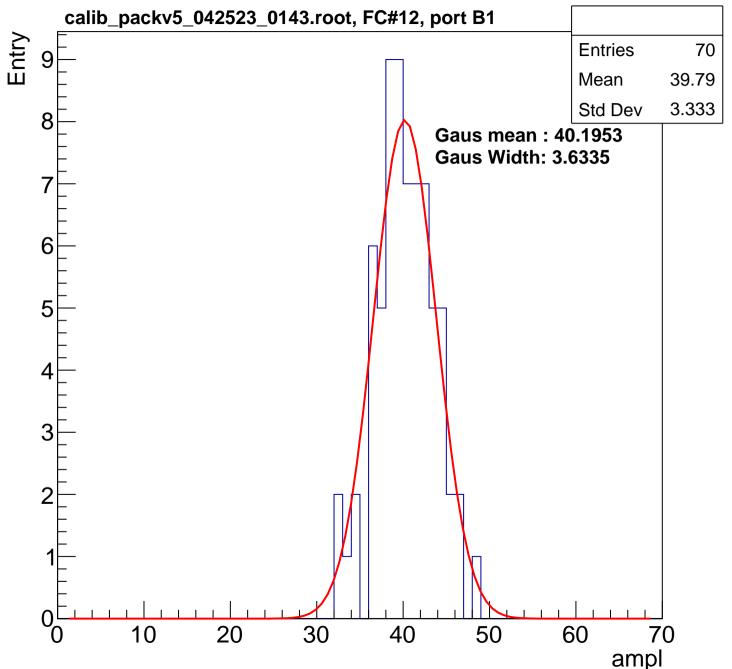


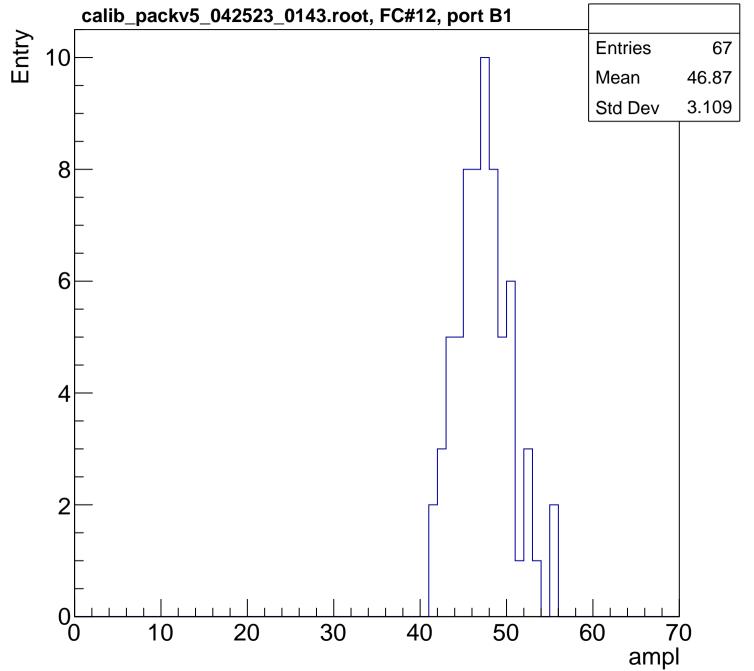
0

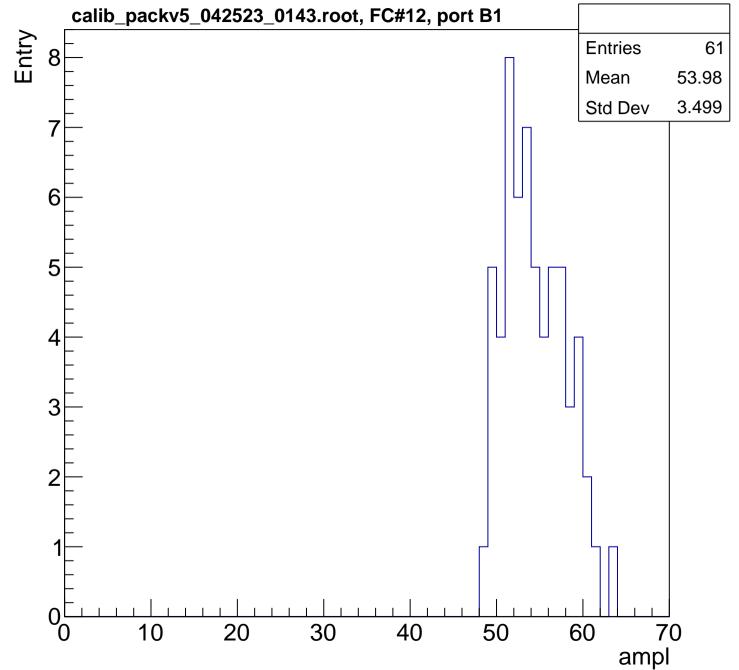


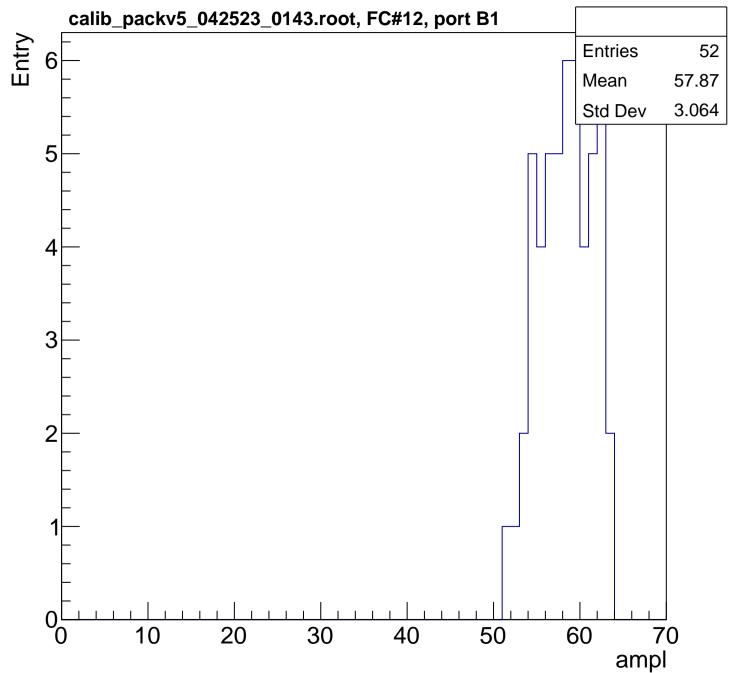


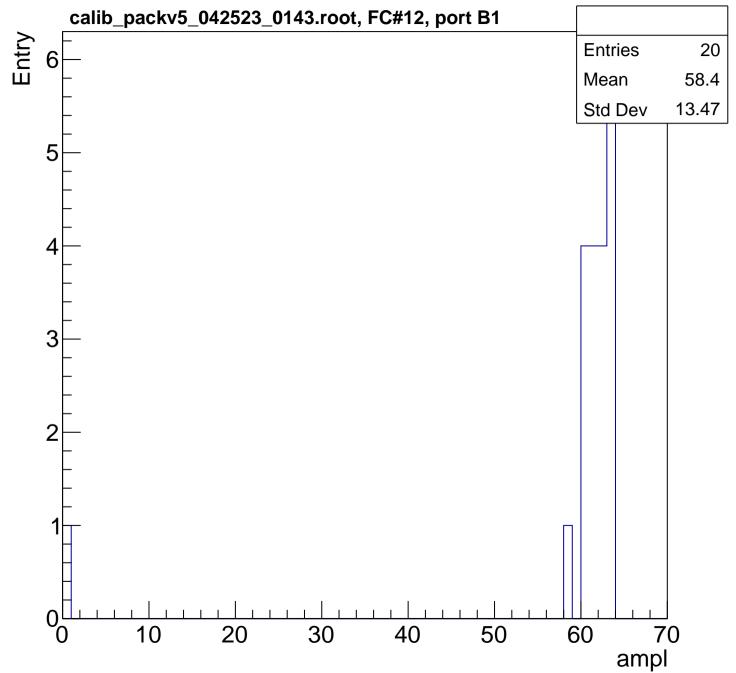




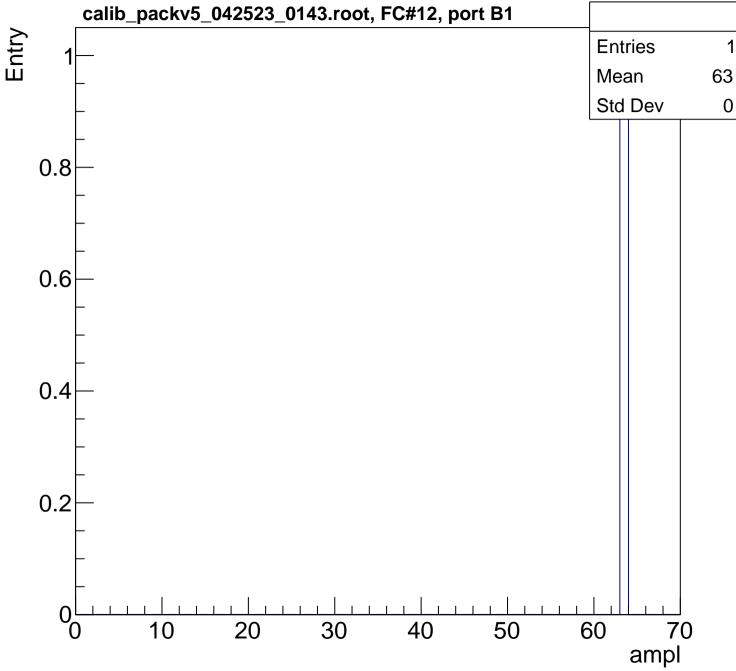


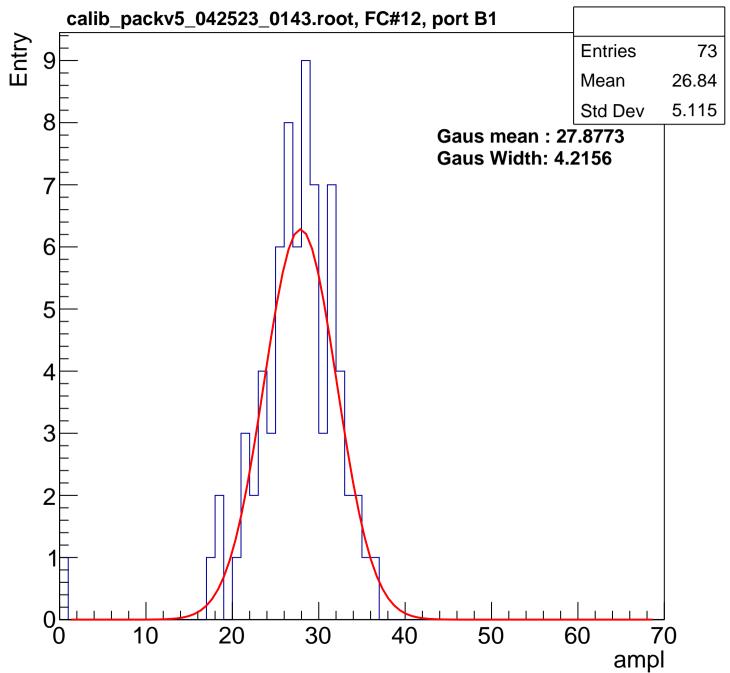


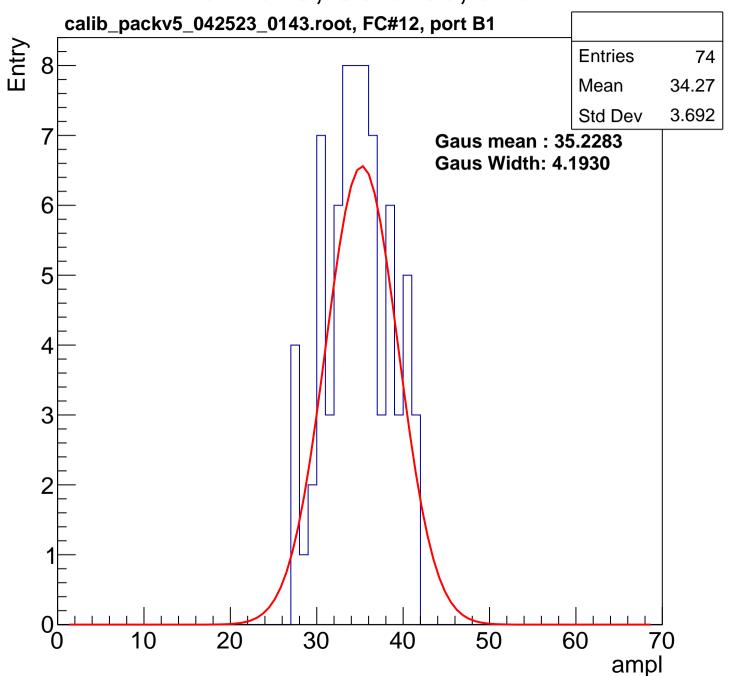


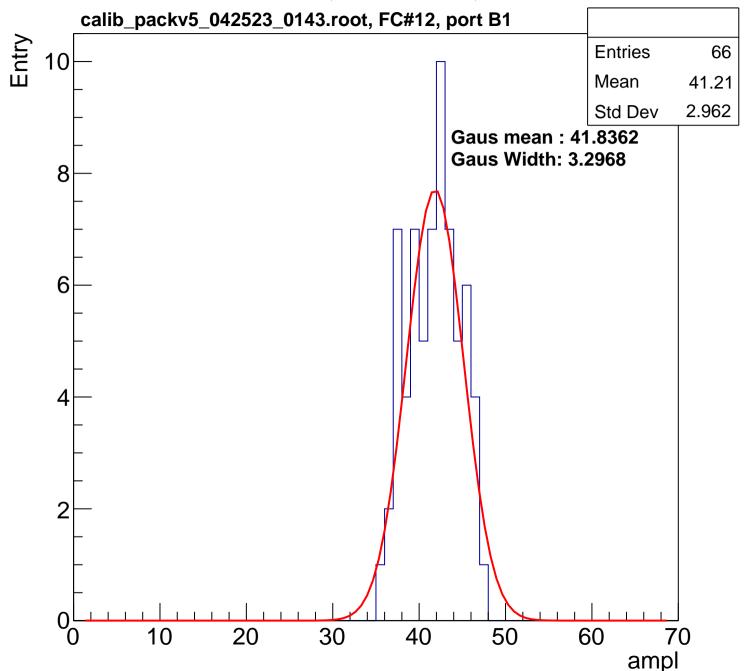


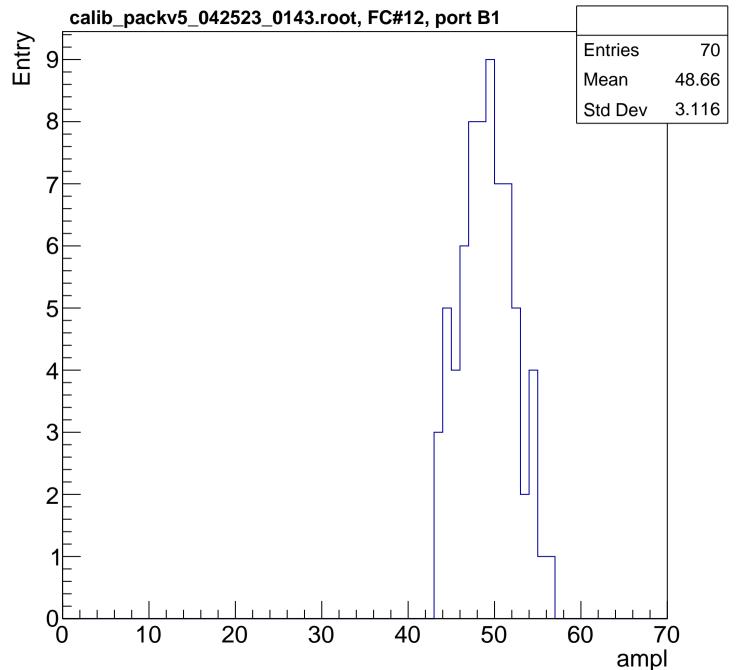
0

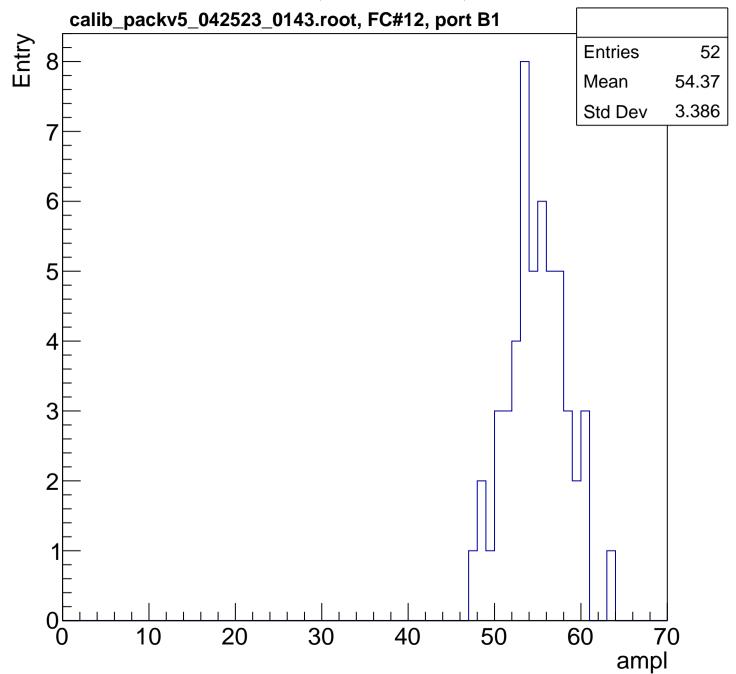


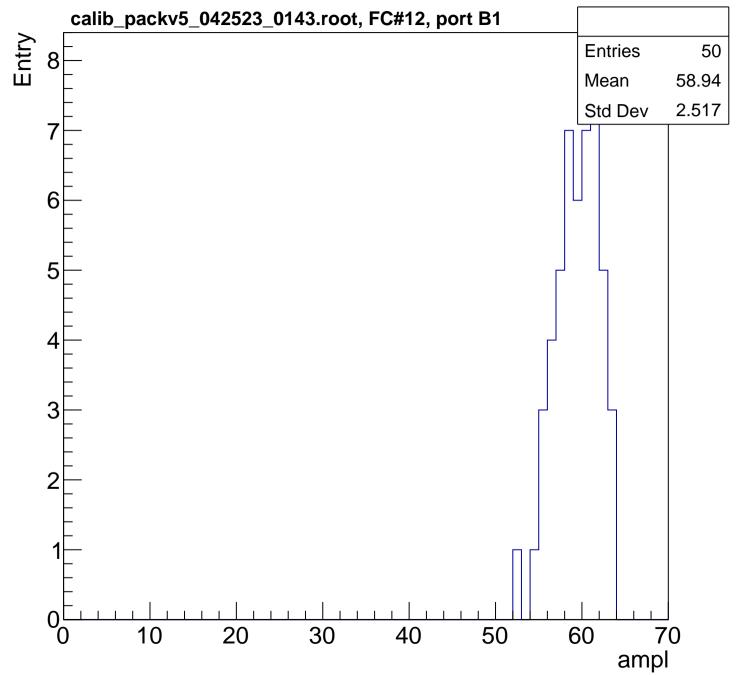


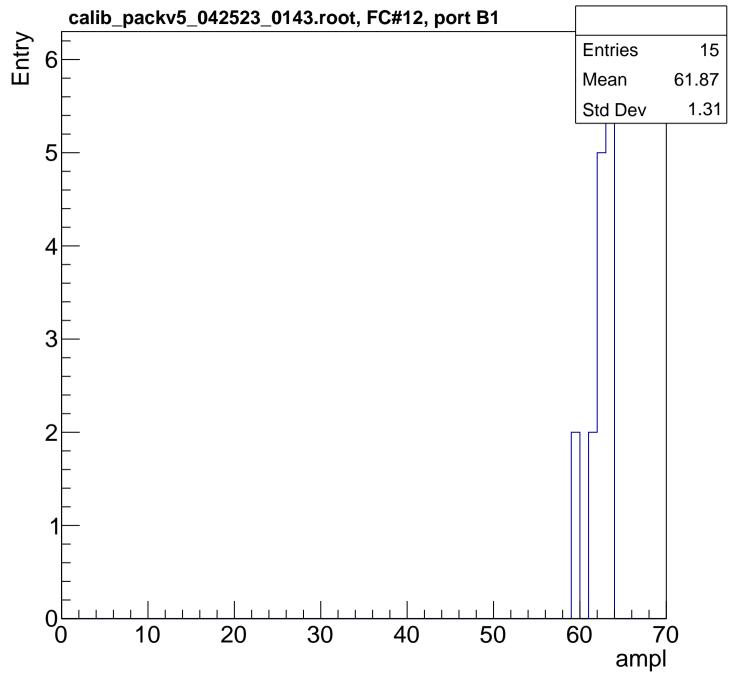




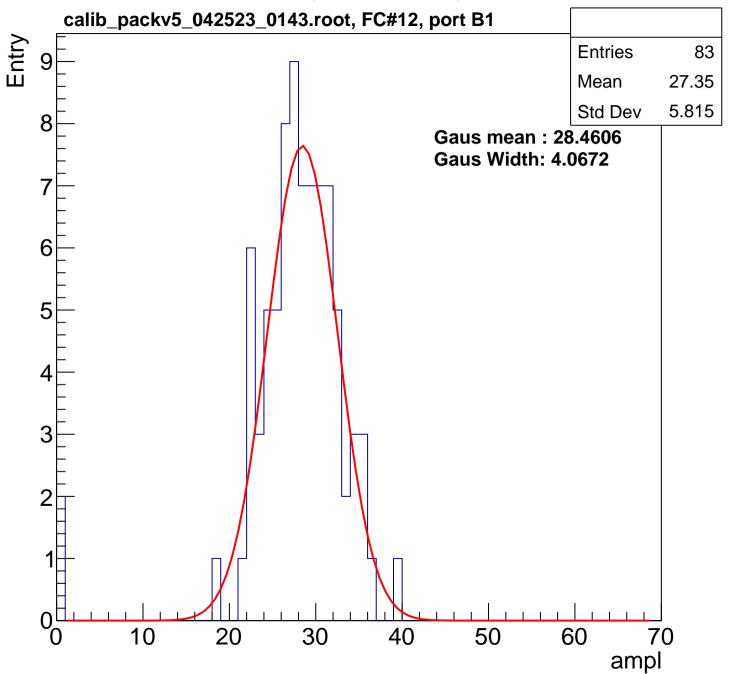


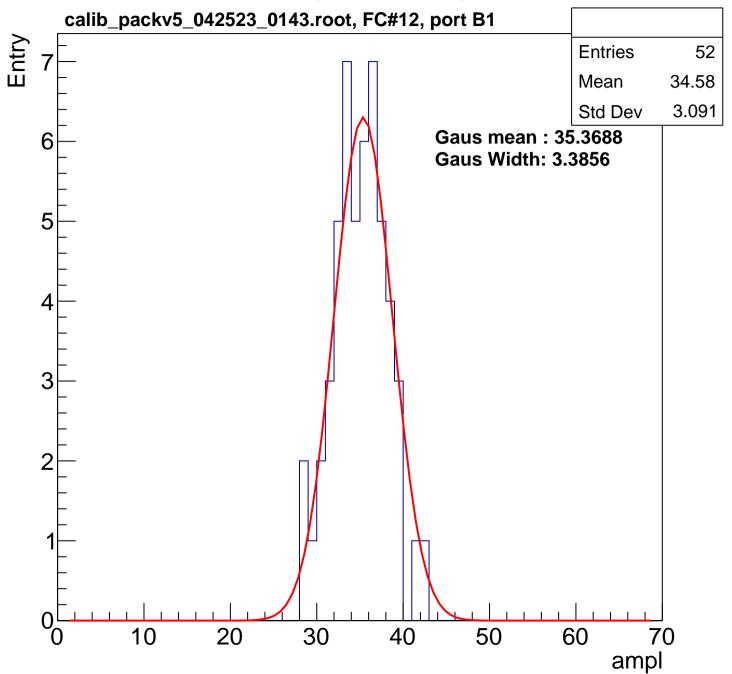


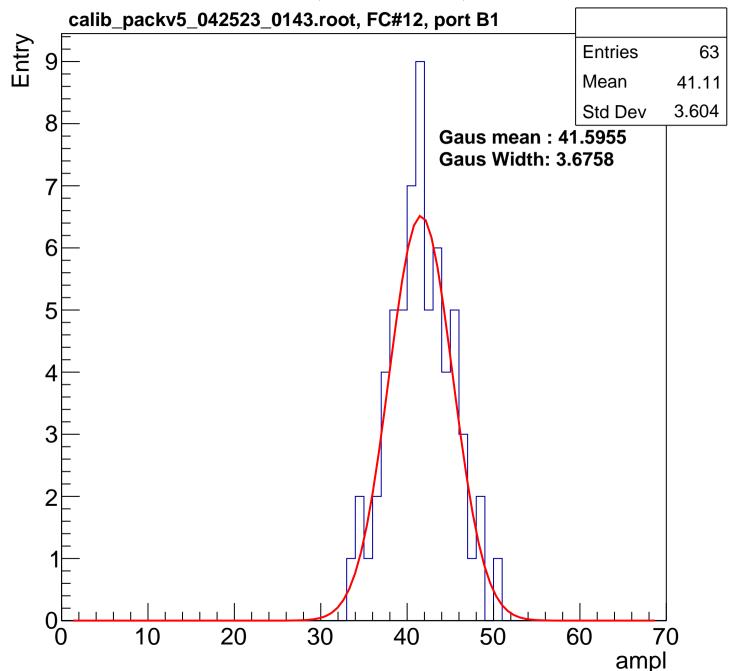


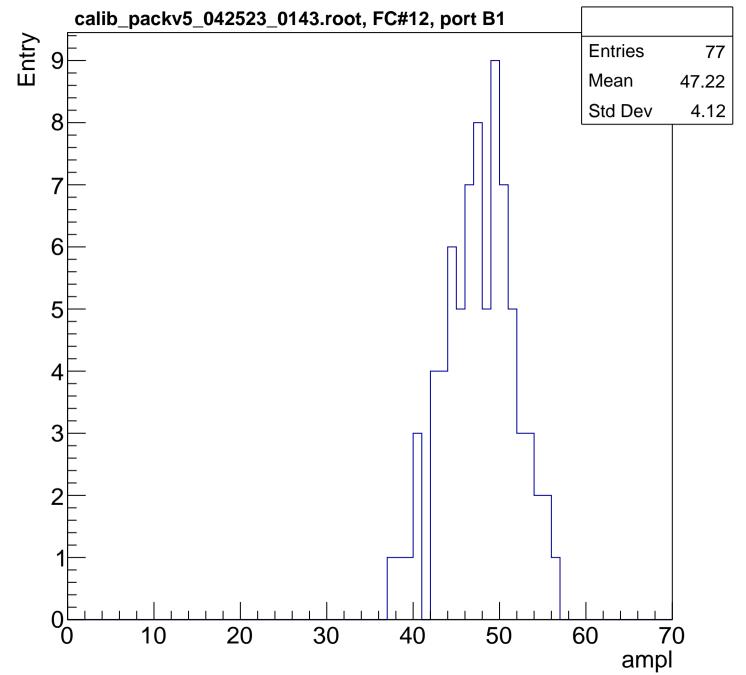


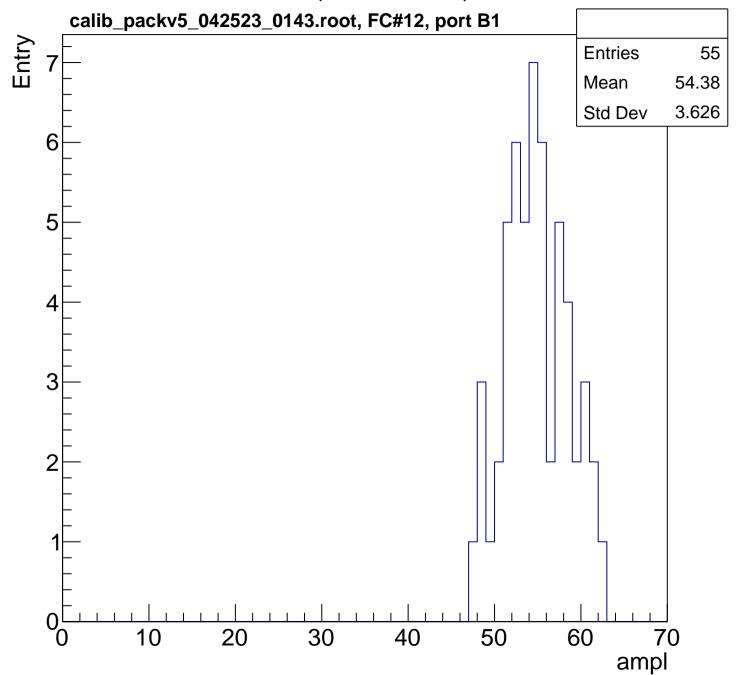


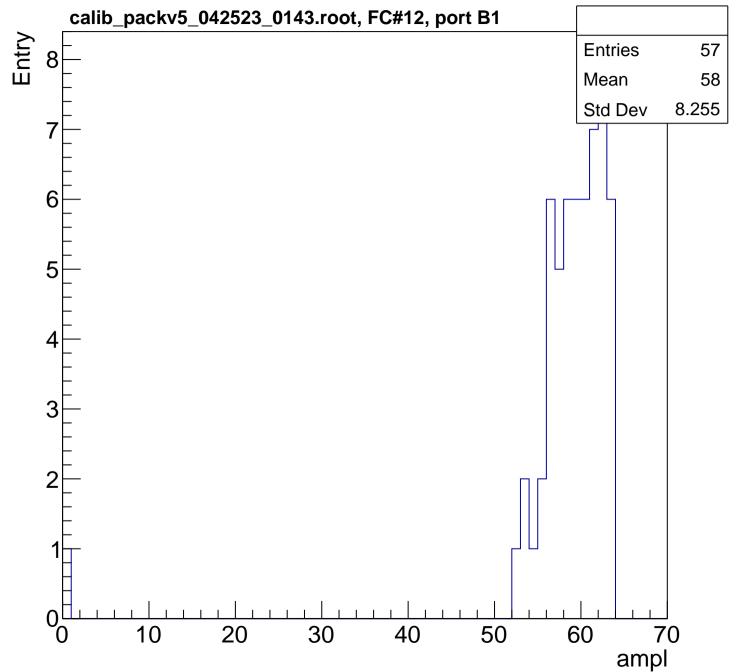


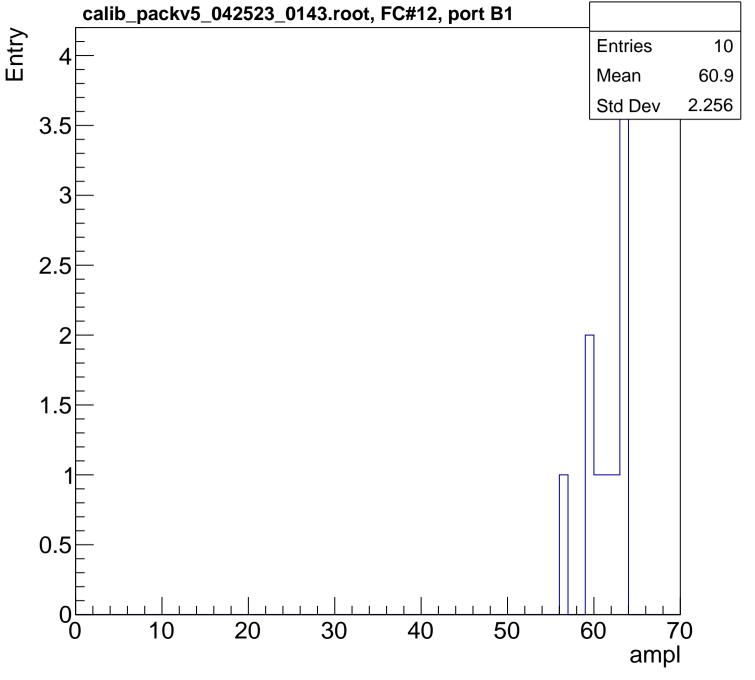




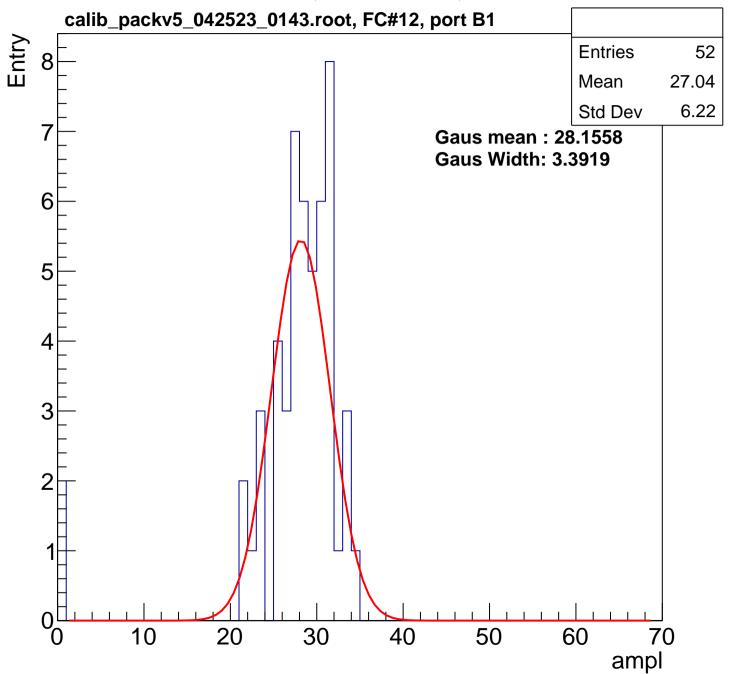


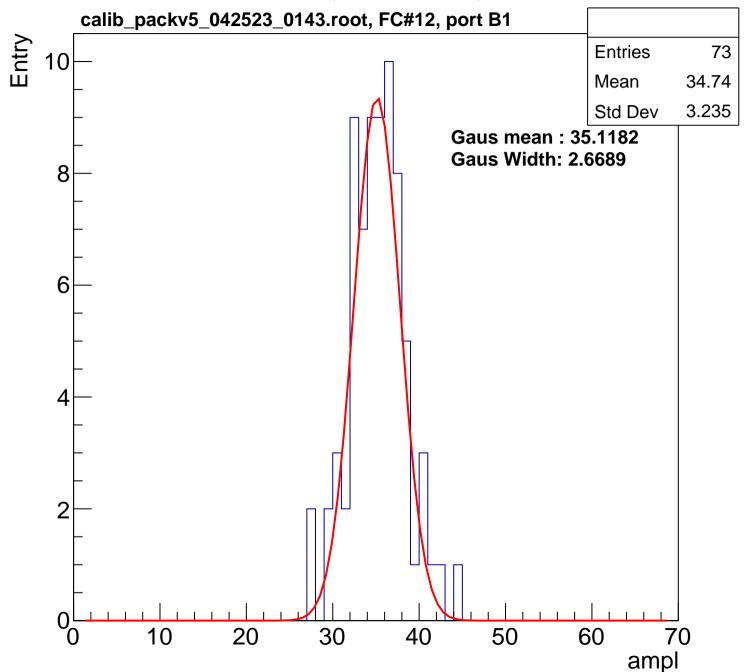


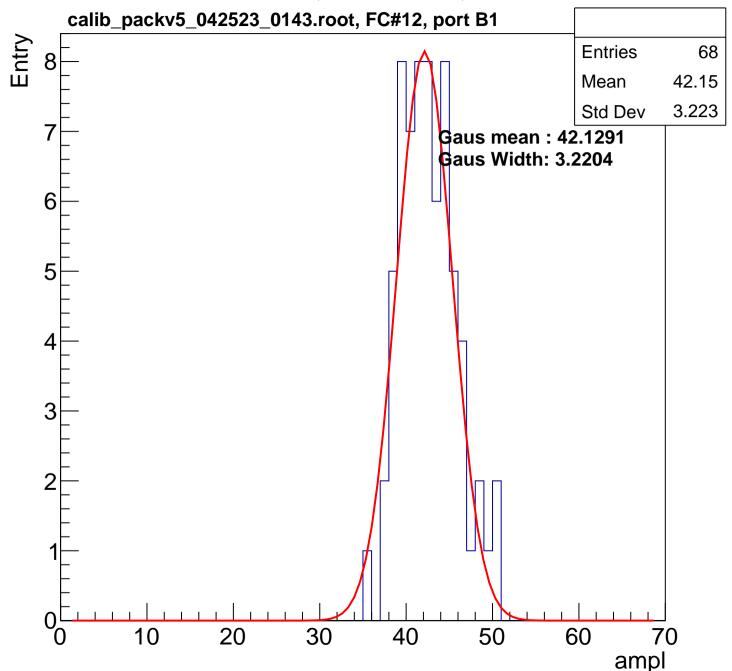


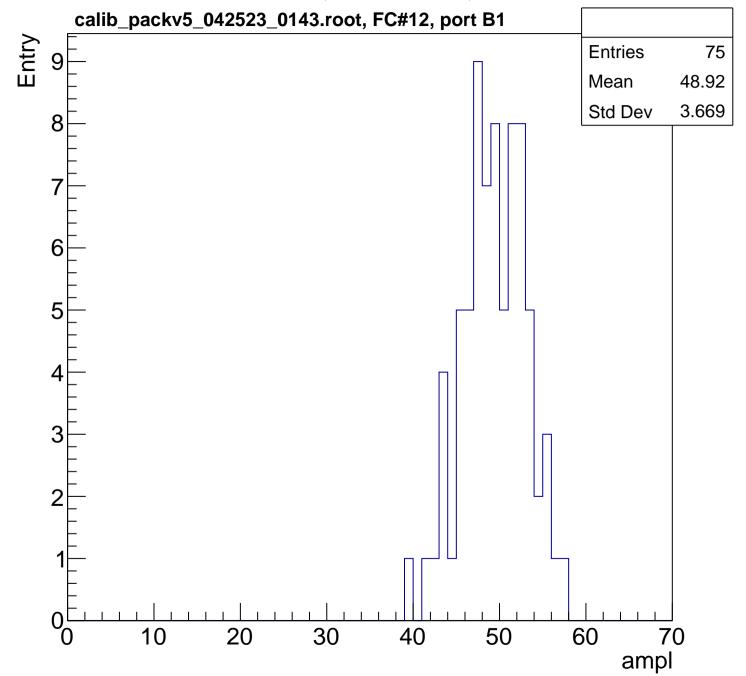


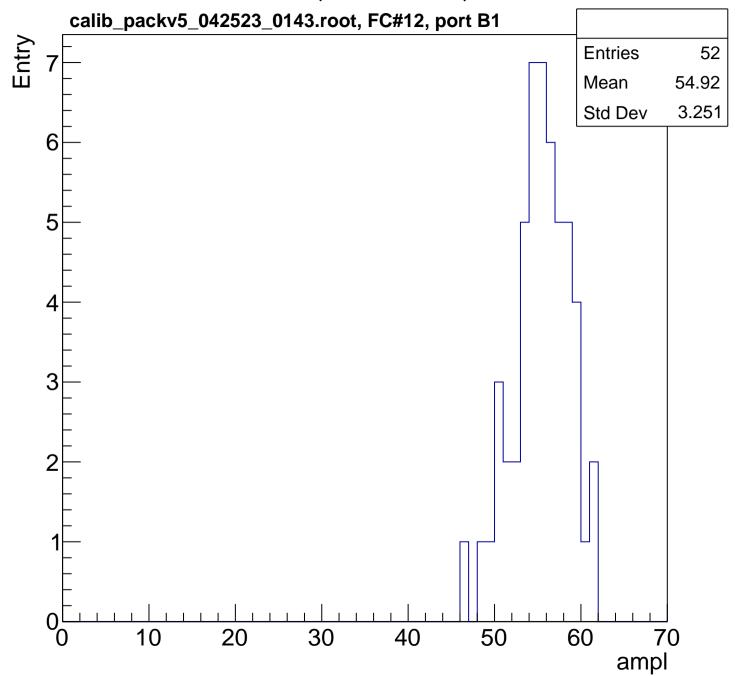


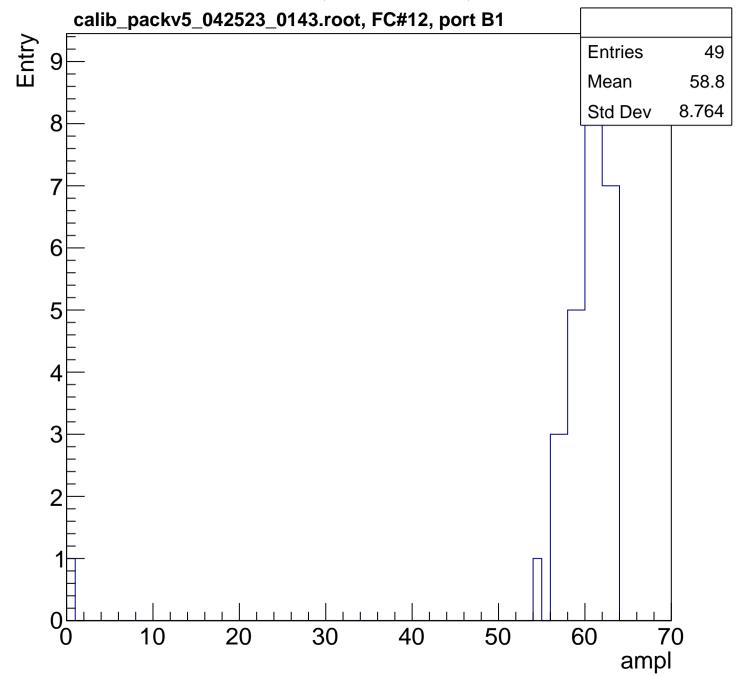


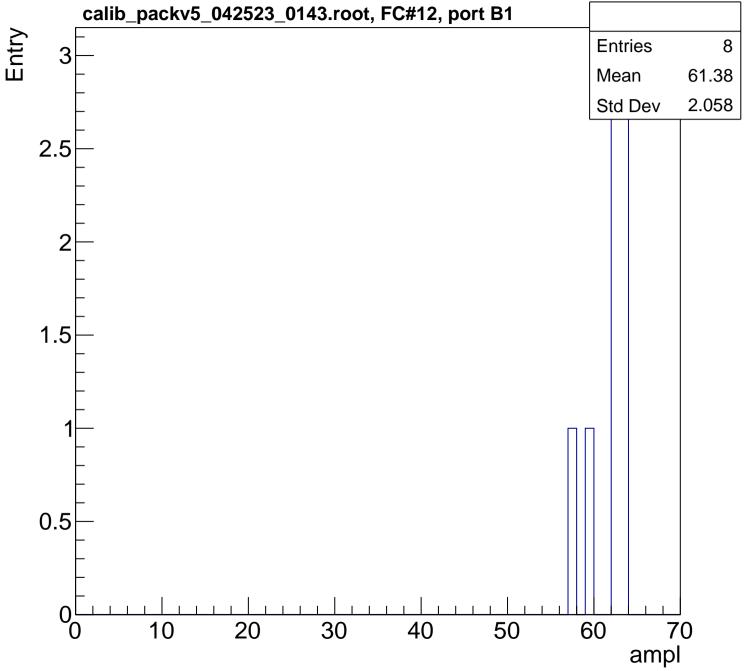




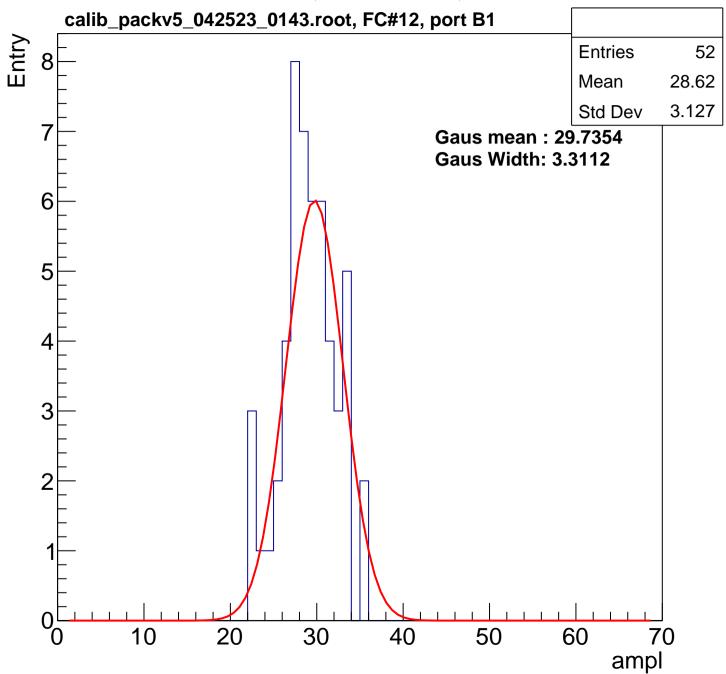


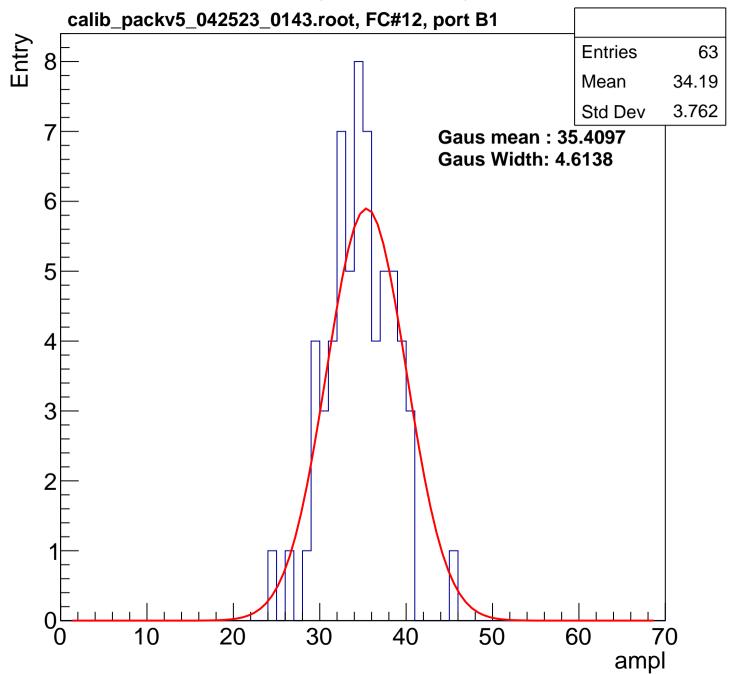


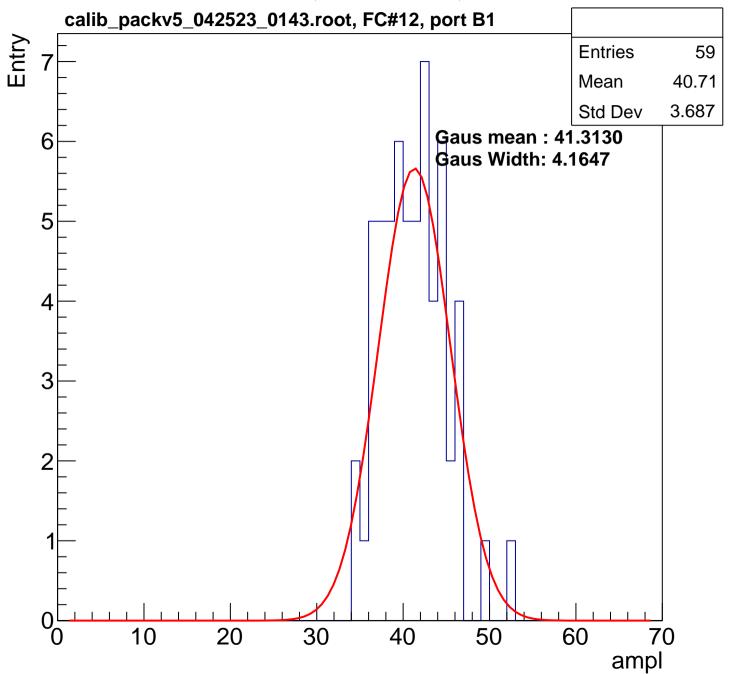


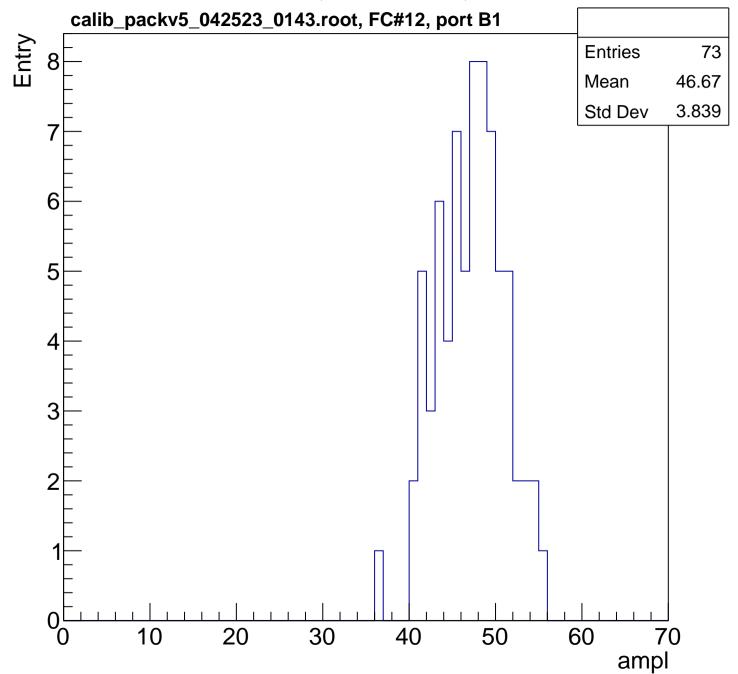


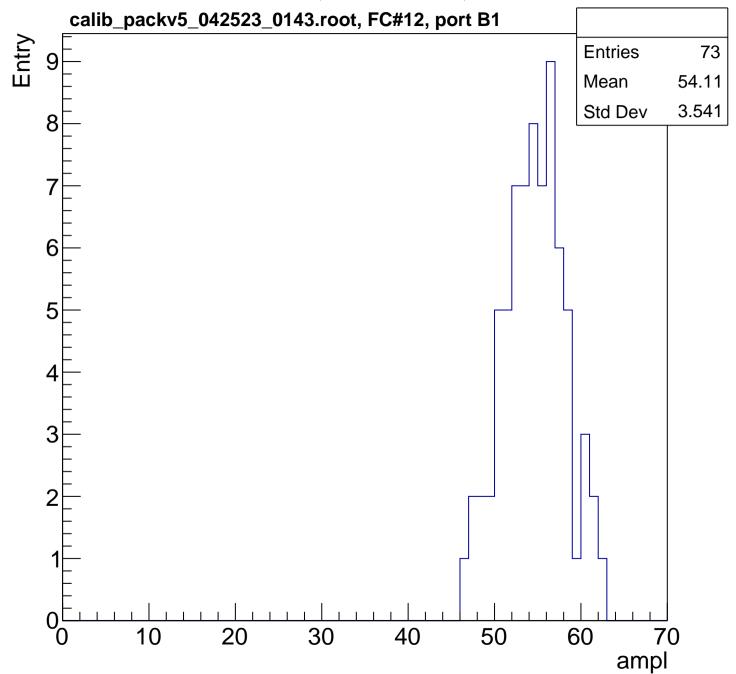
B0L102S, U3-ch61, adc7 calib_packv5_042523_0143.root, FC#12, port B1 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

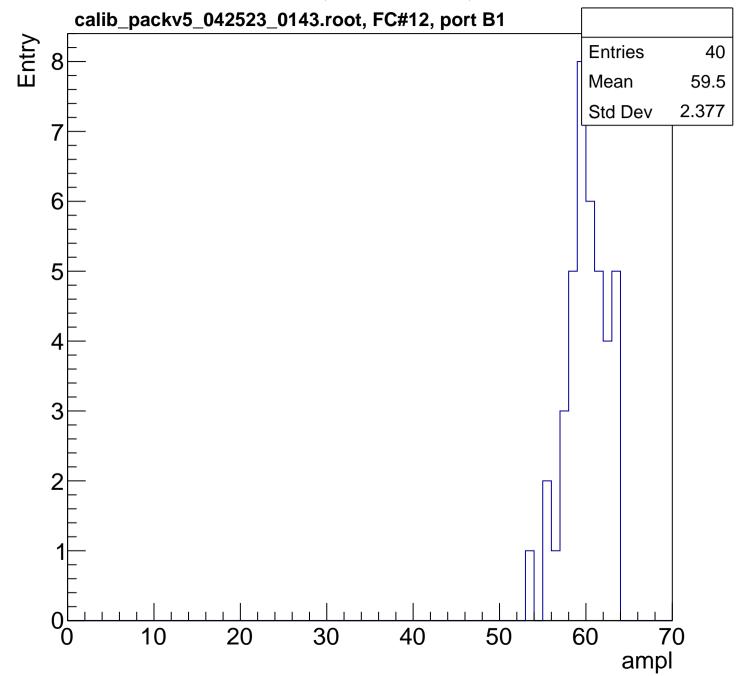


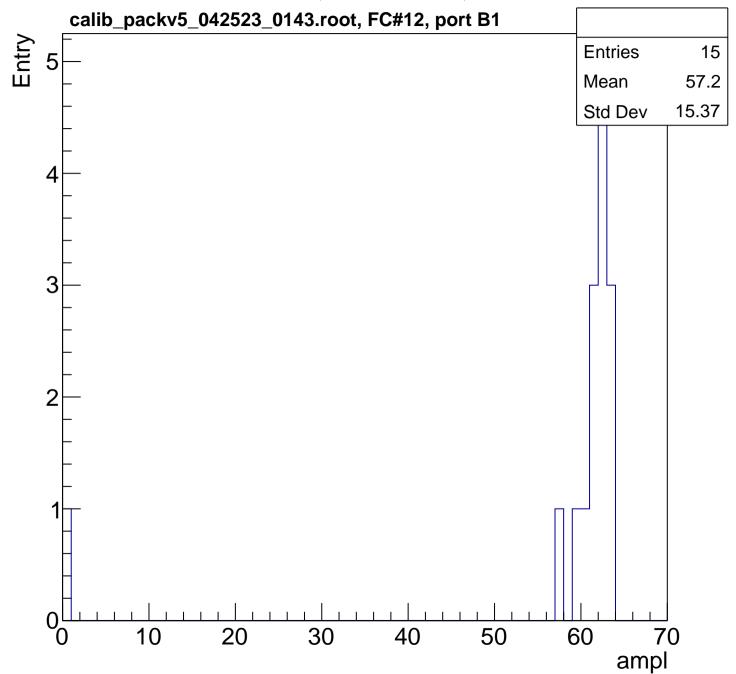


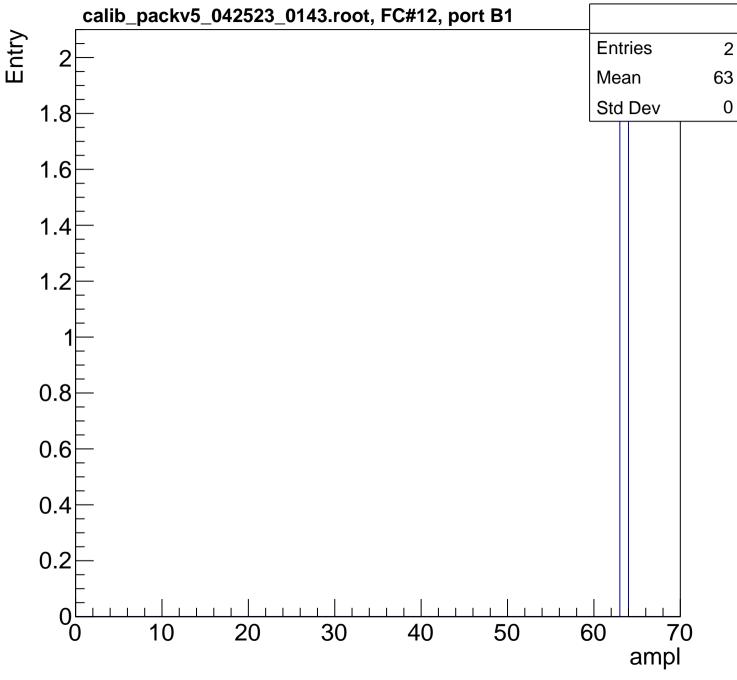


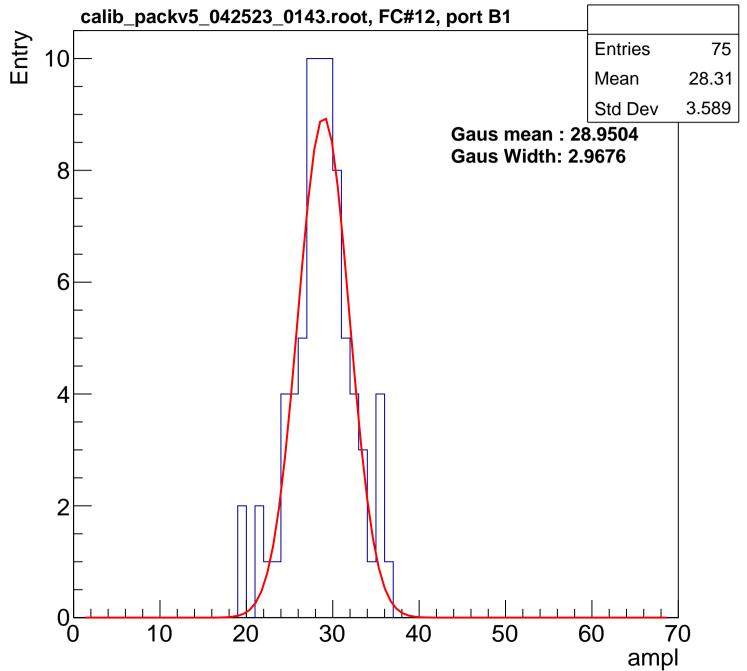


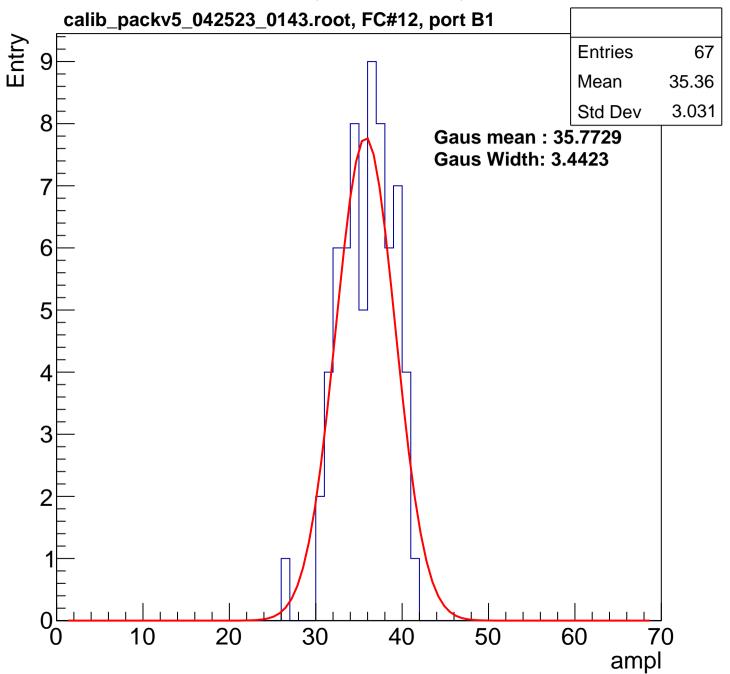


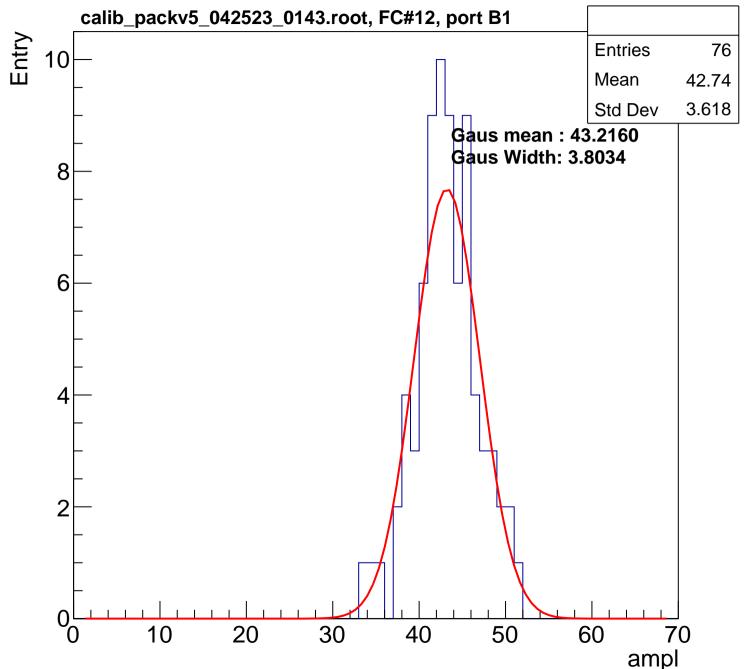


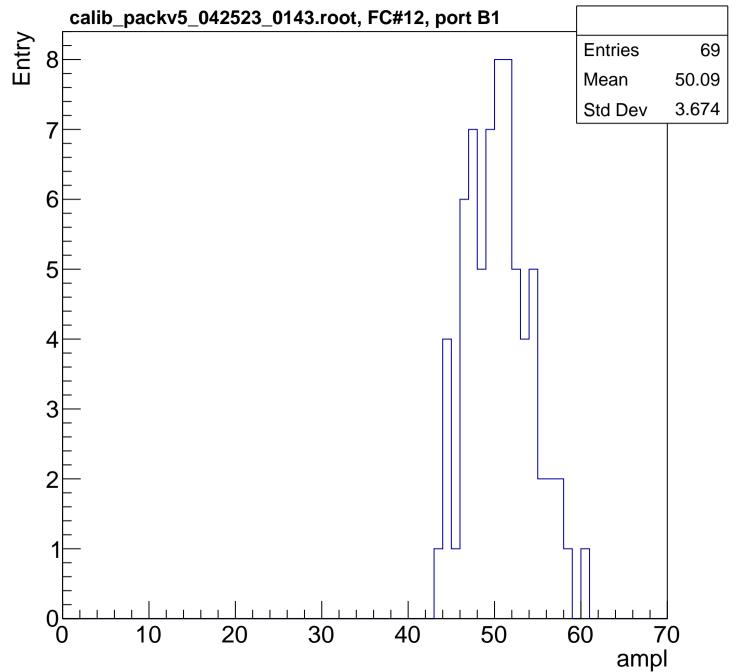


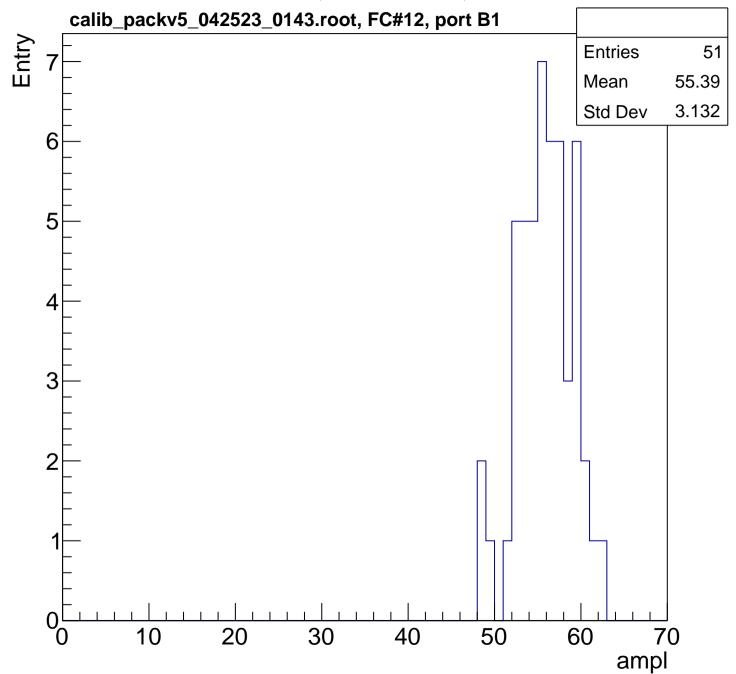


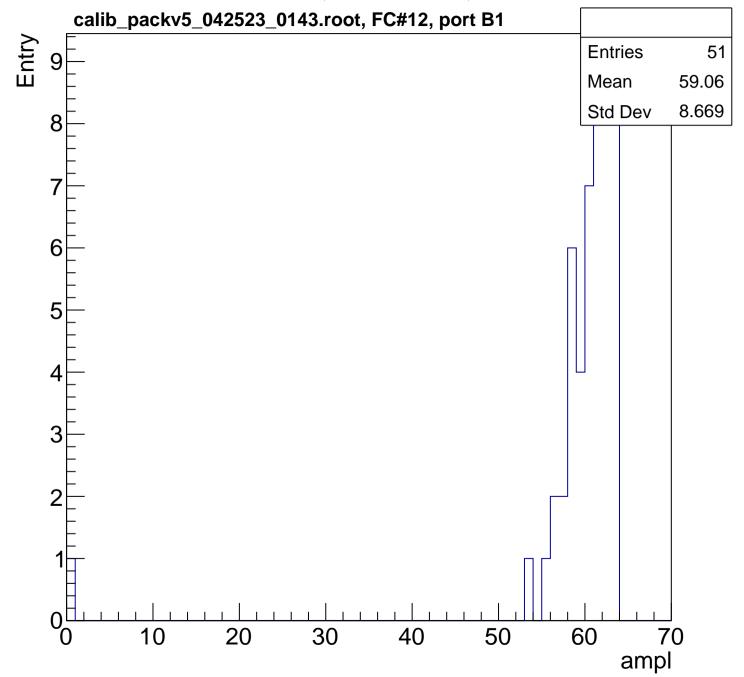


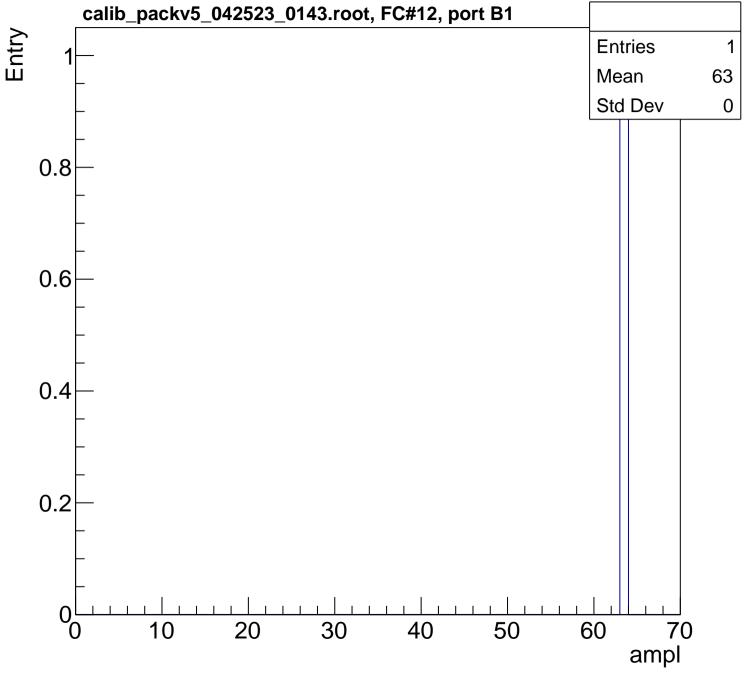


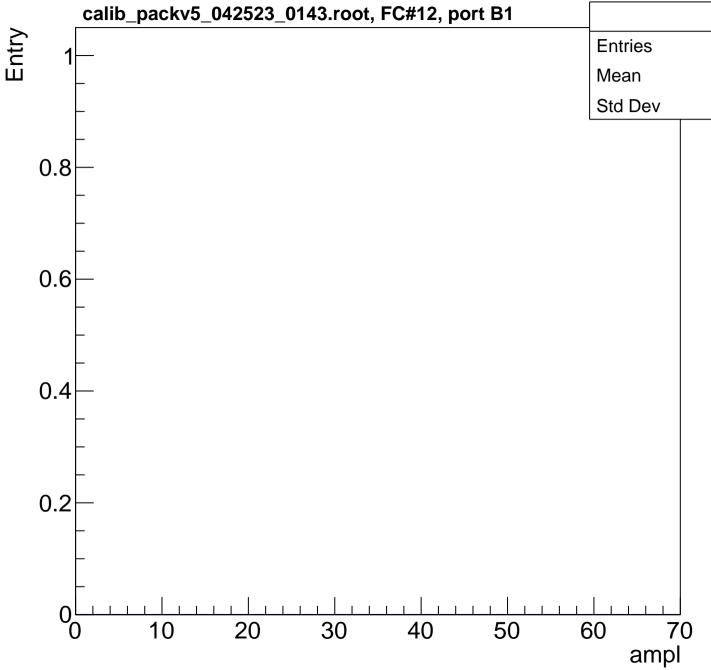


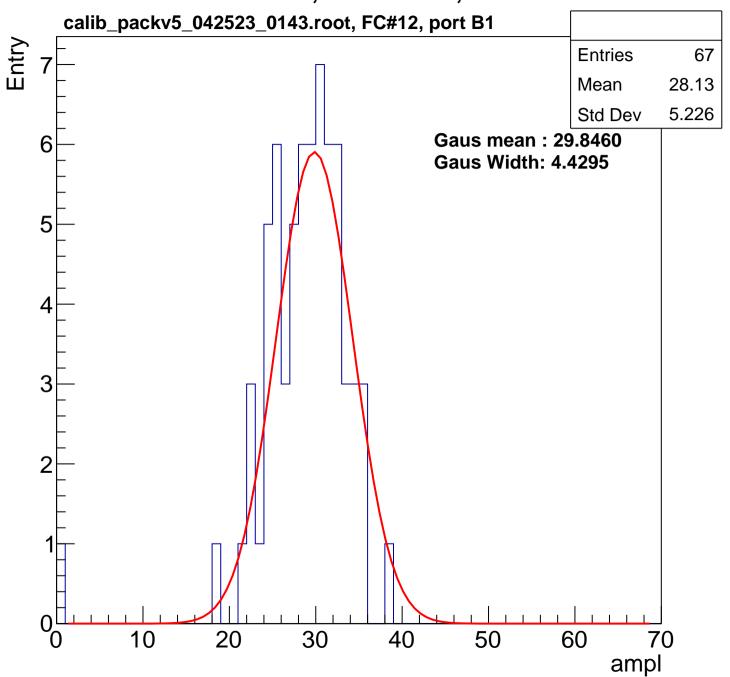


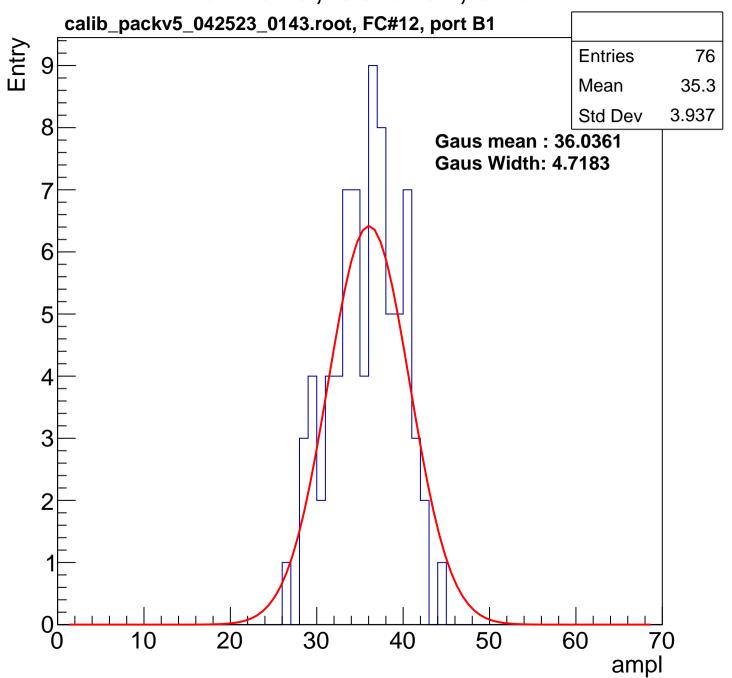


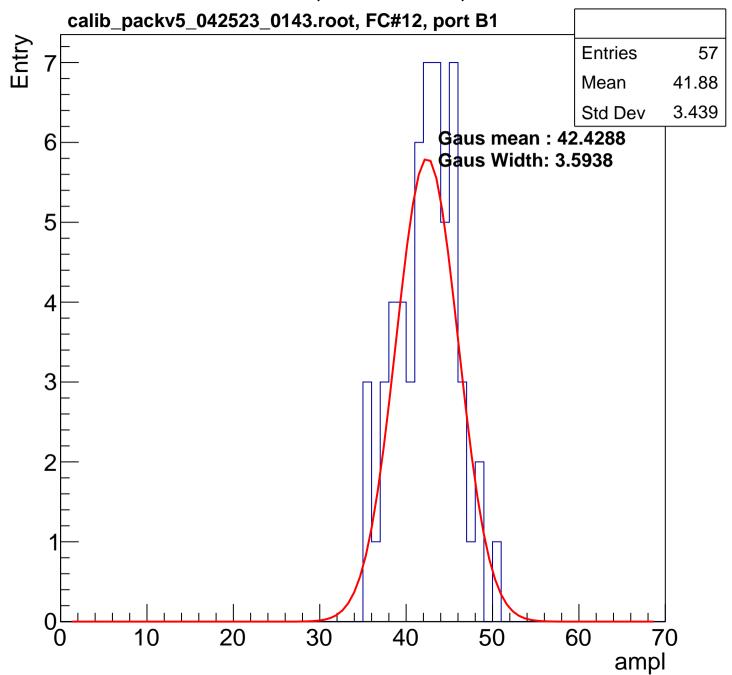


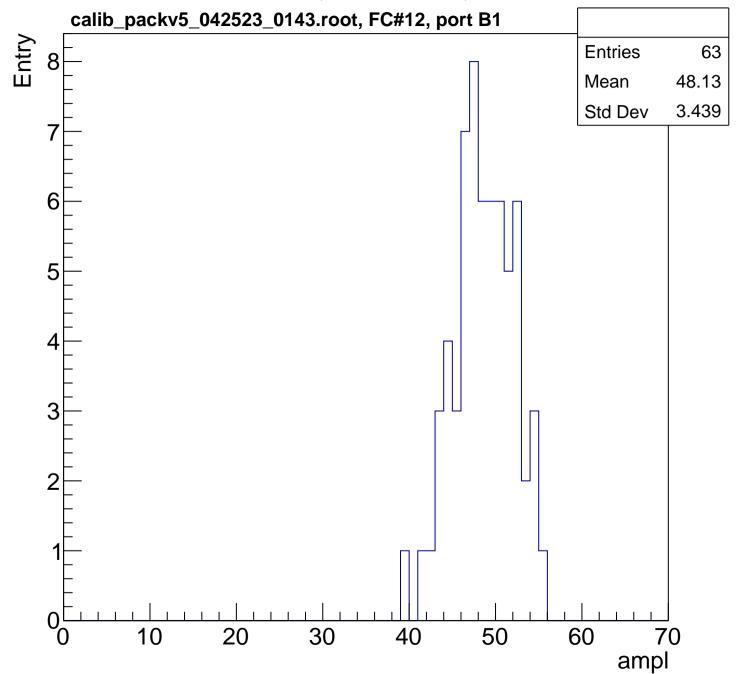


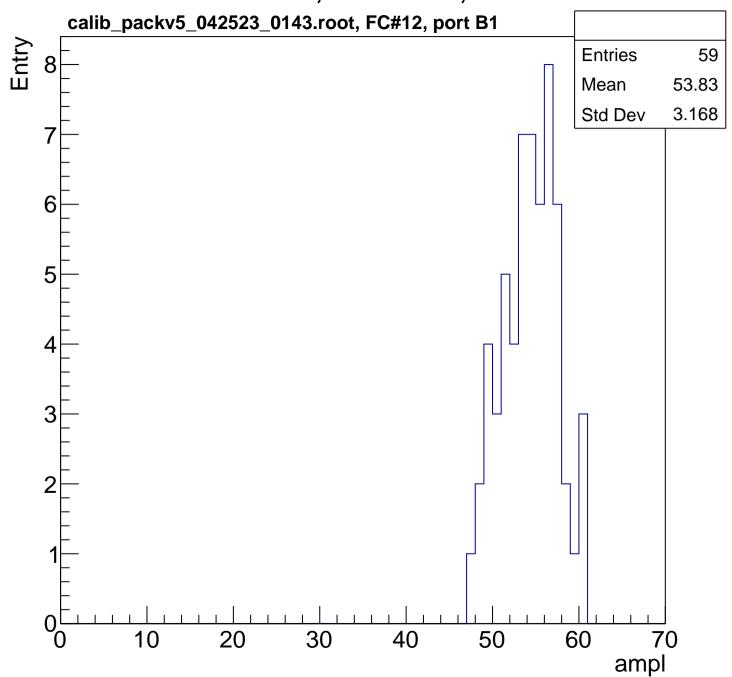


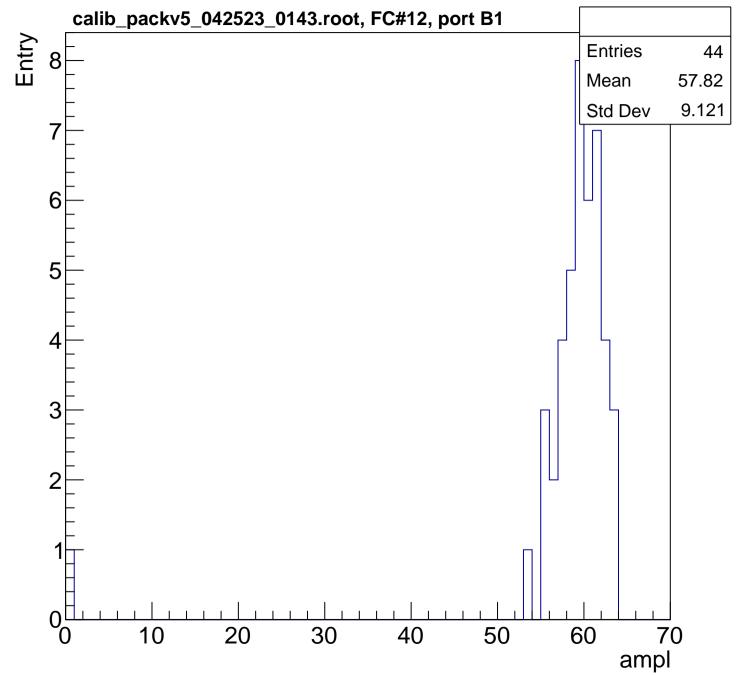


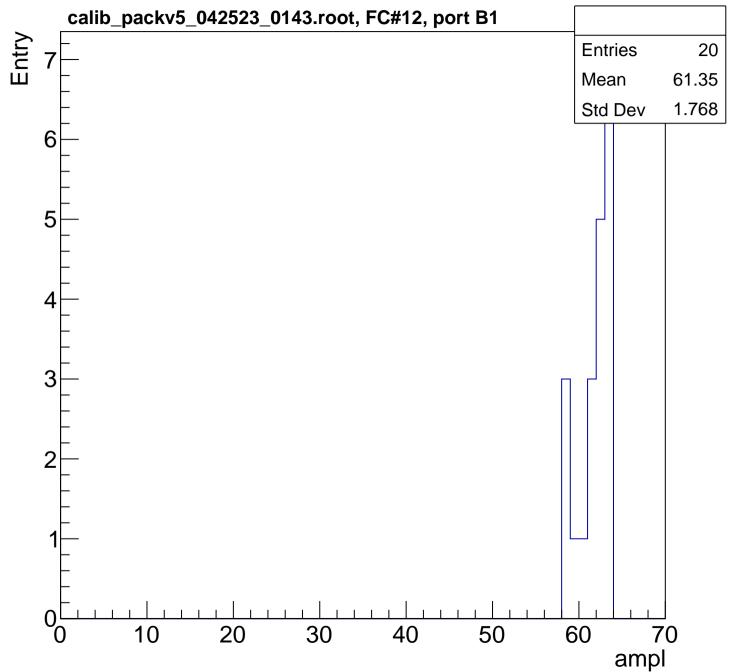




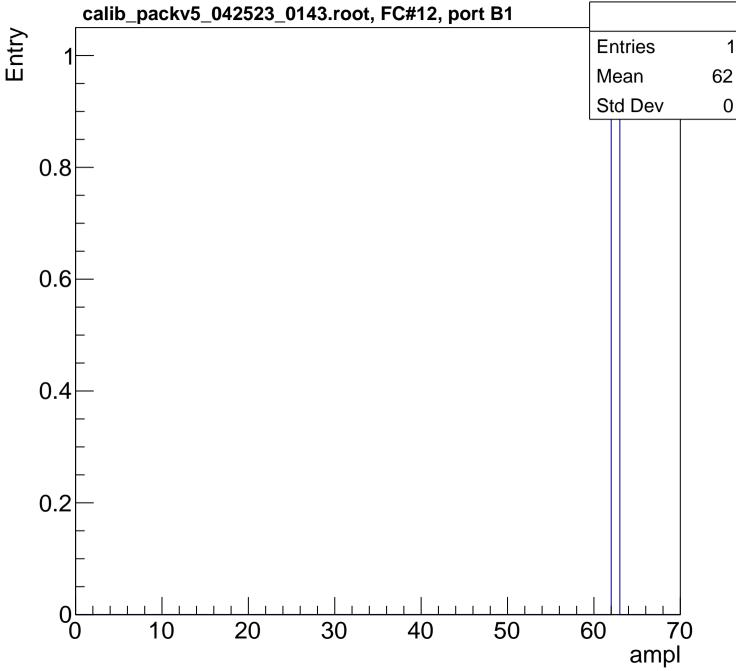


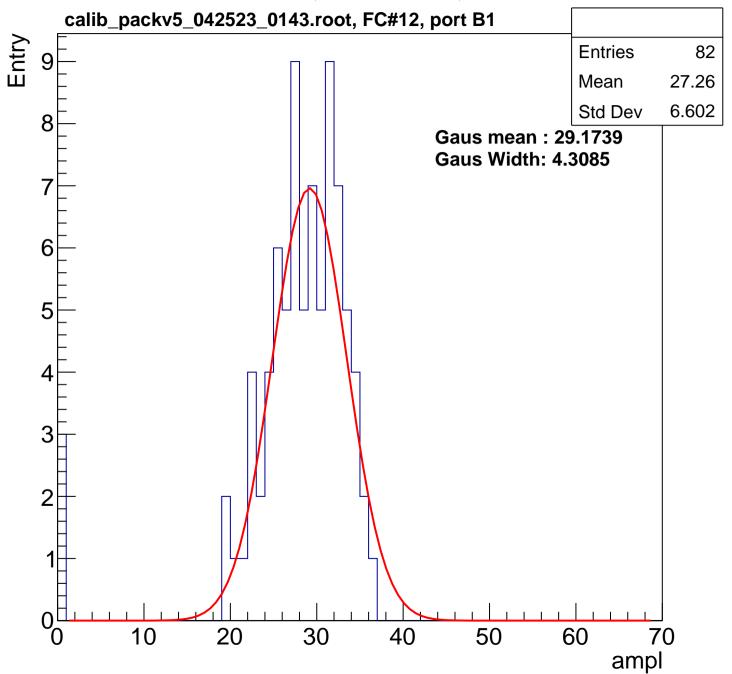


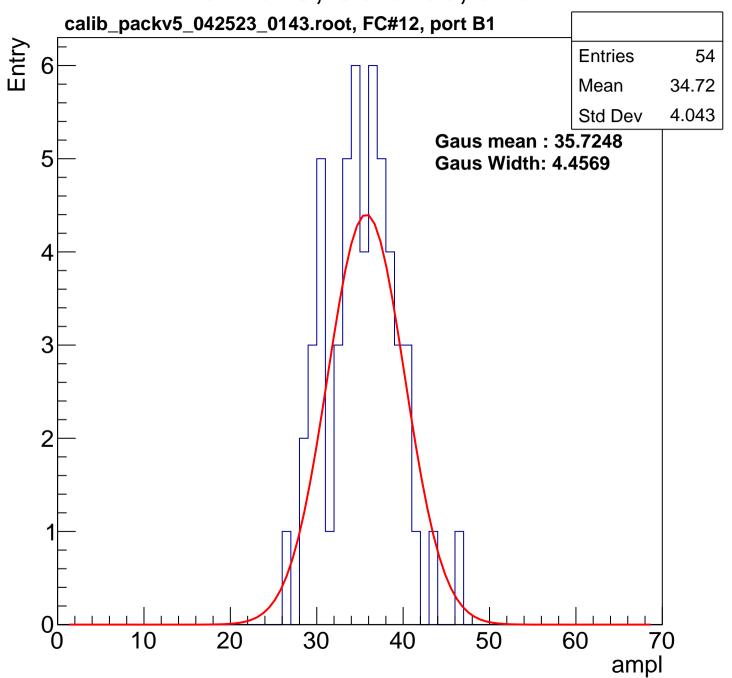


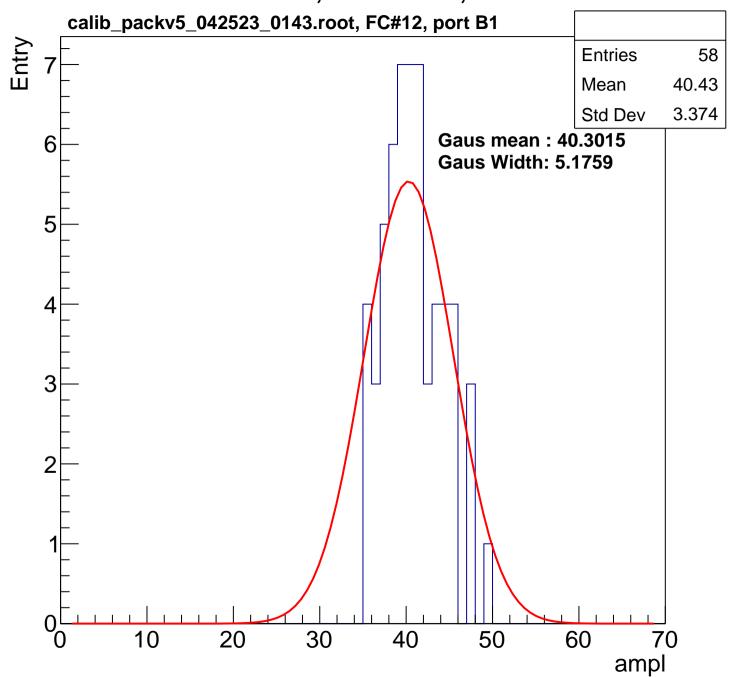


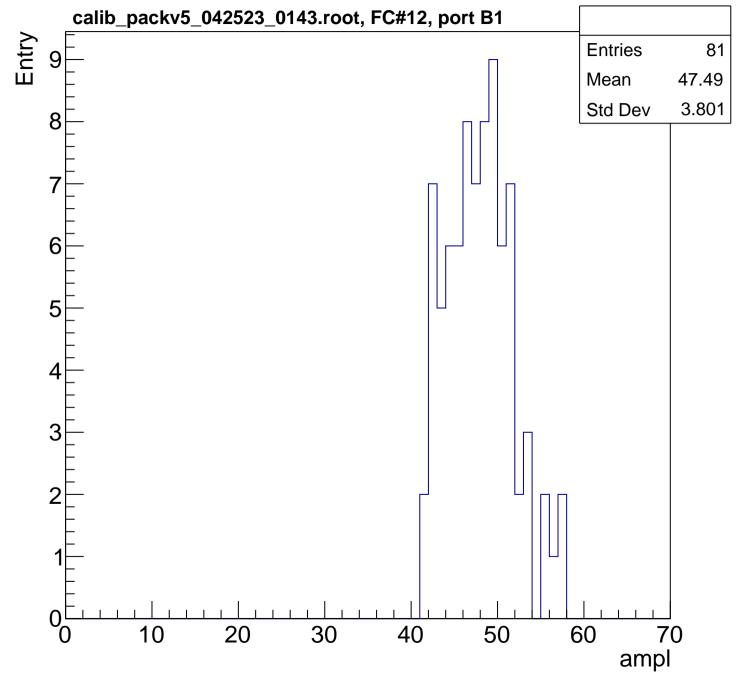
0

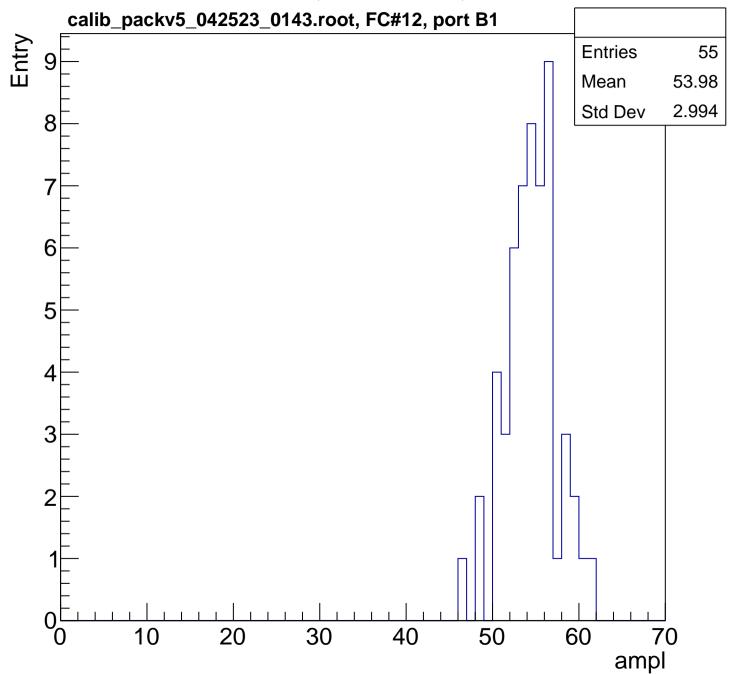


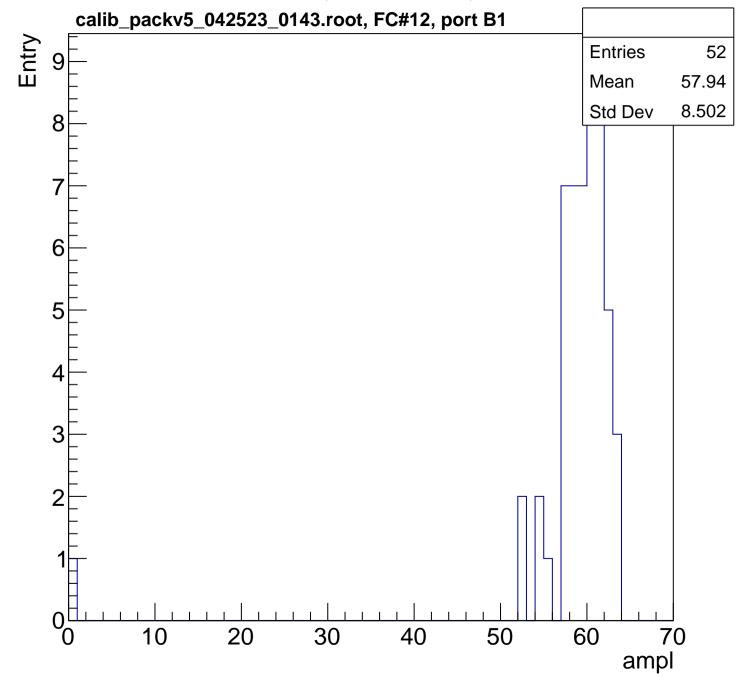


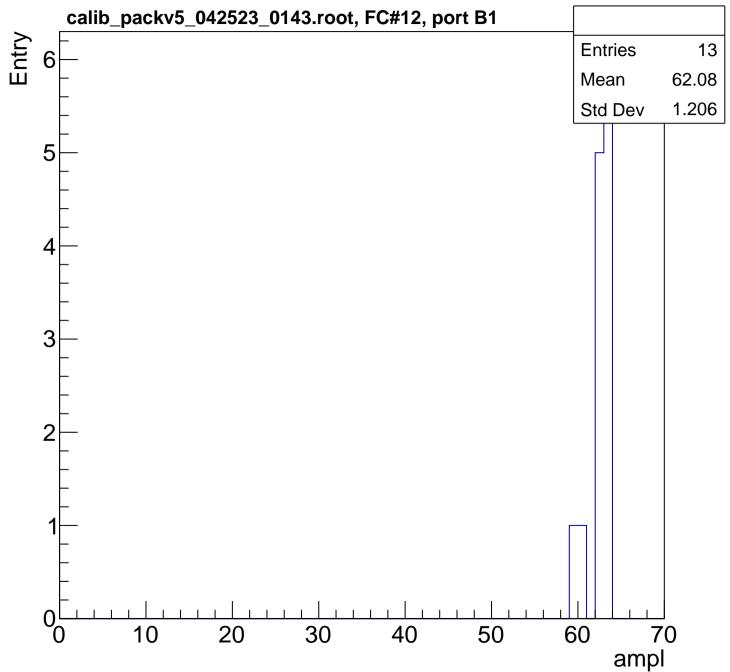


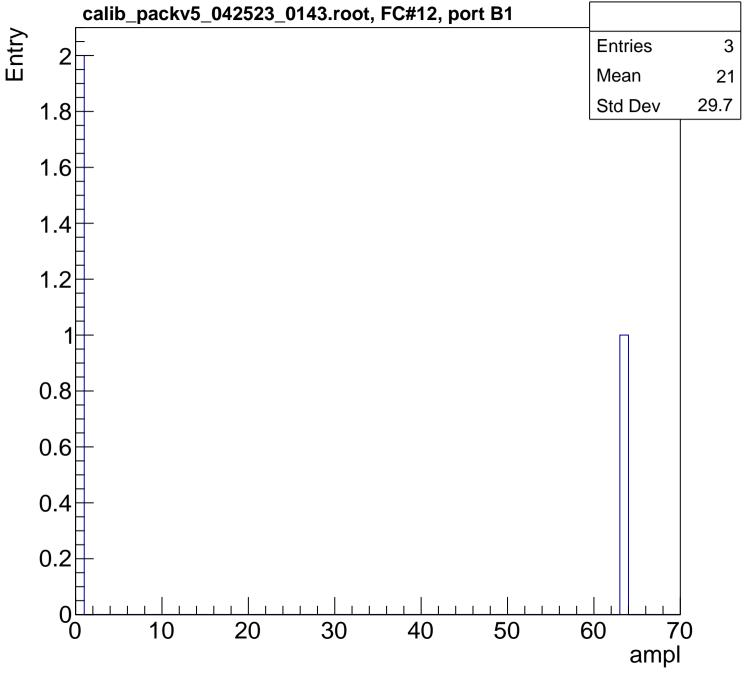


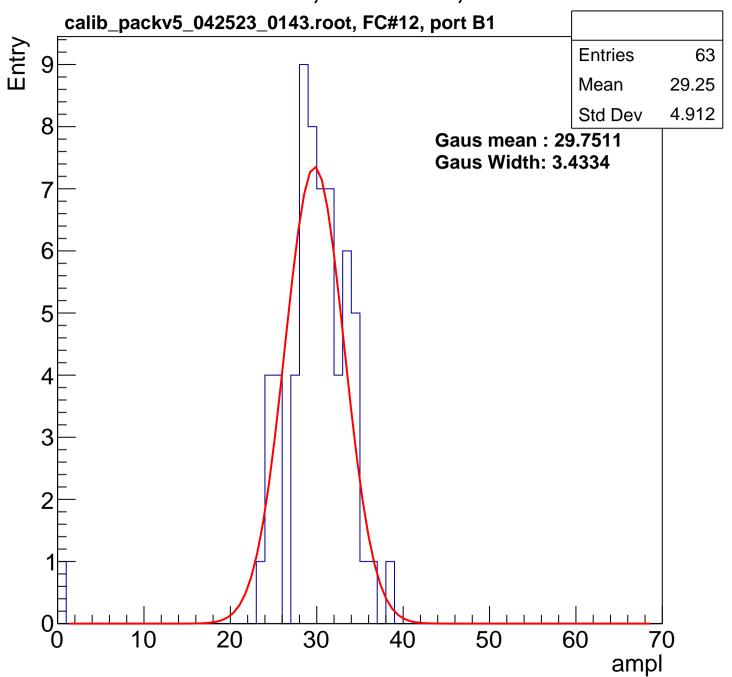


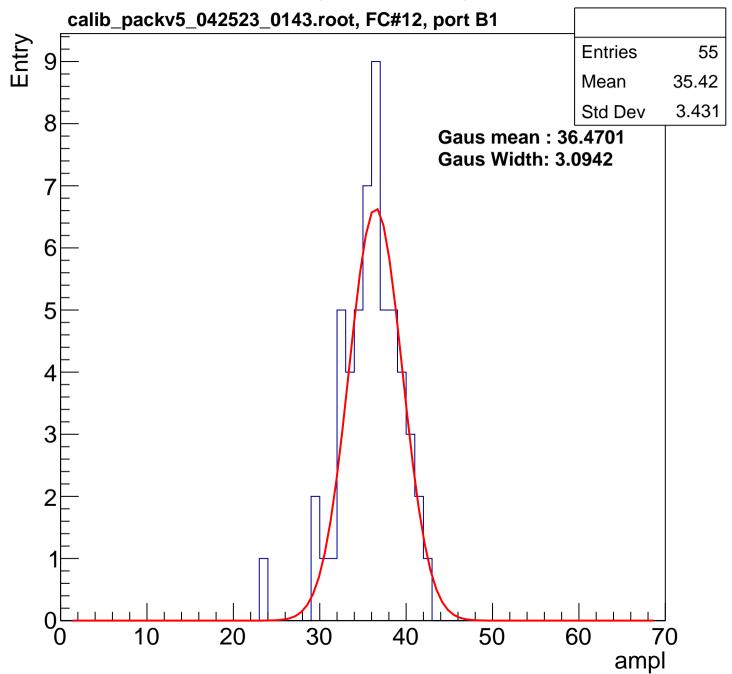


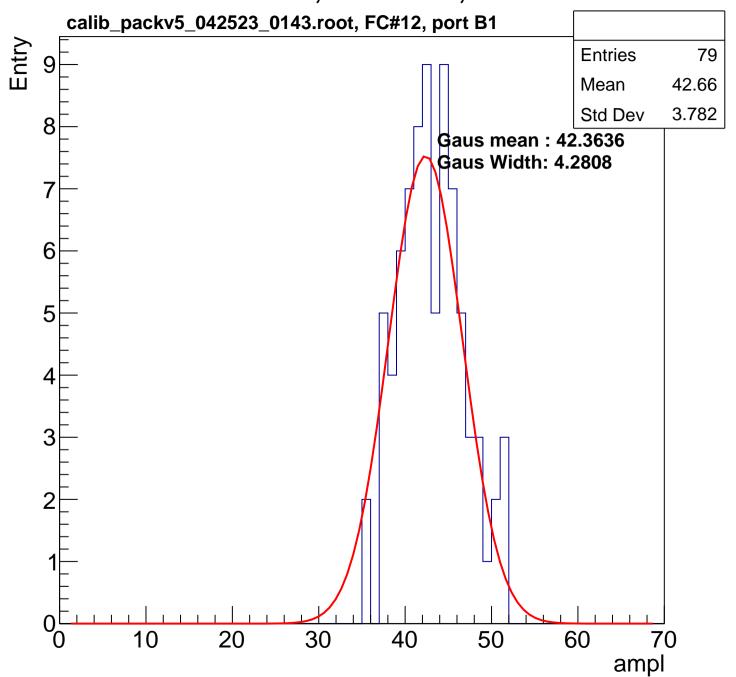


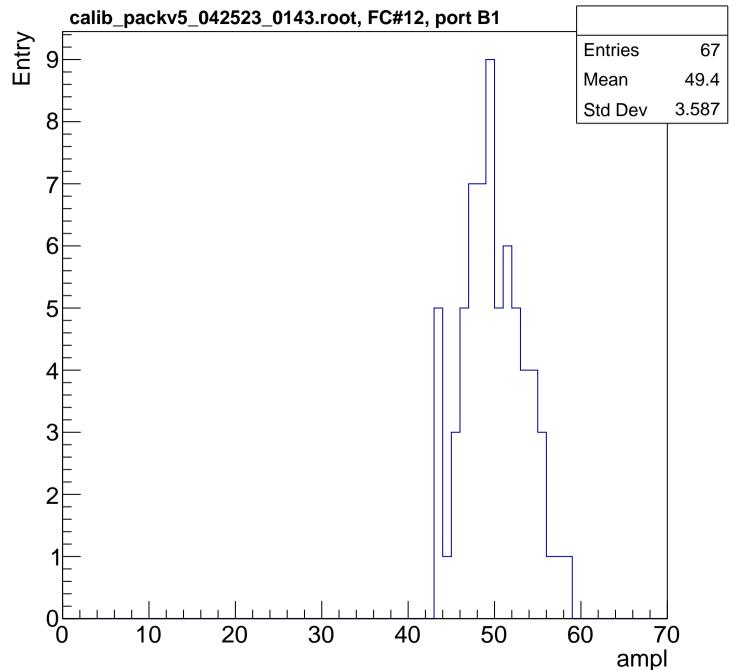


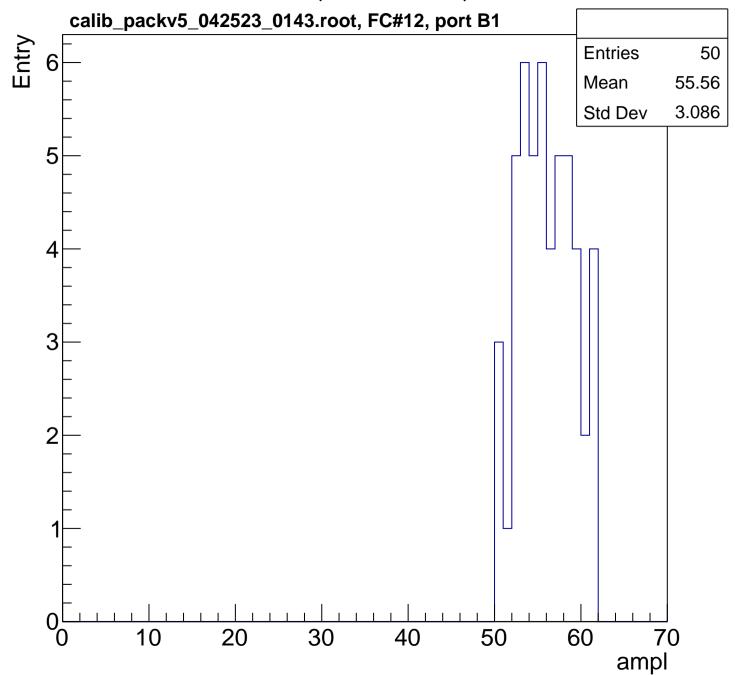


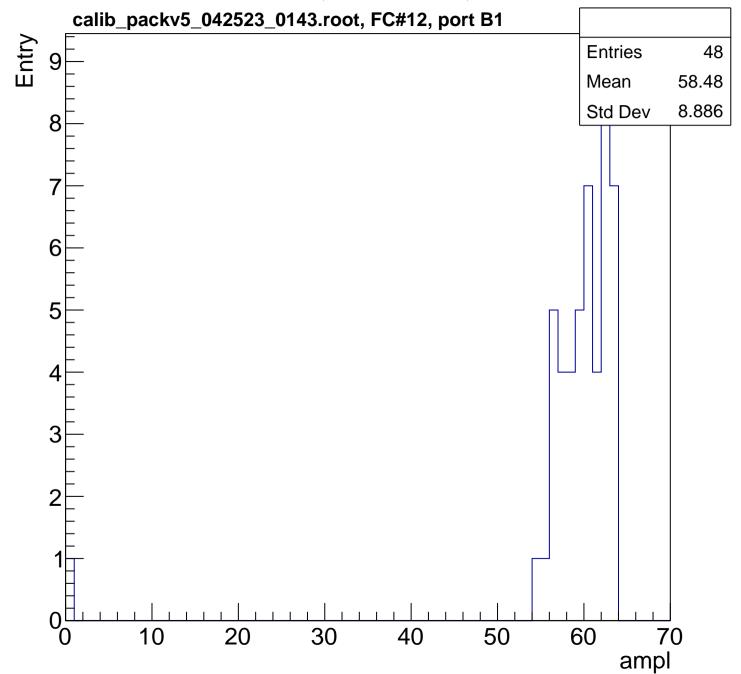


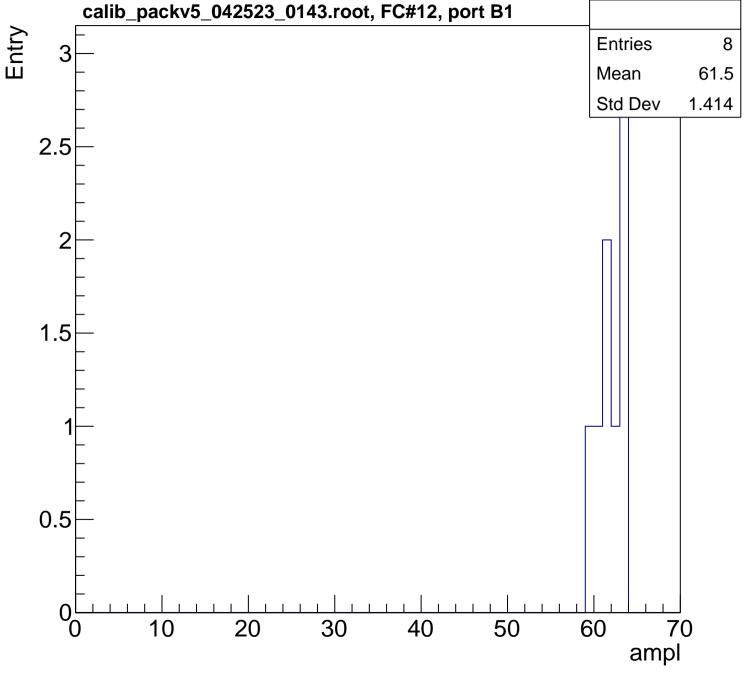




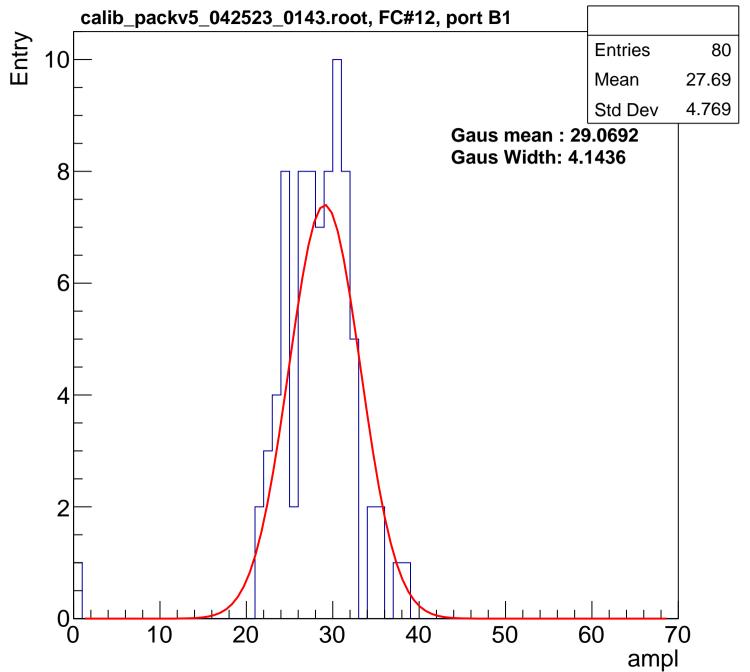


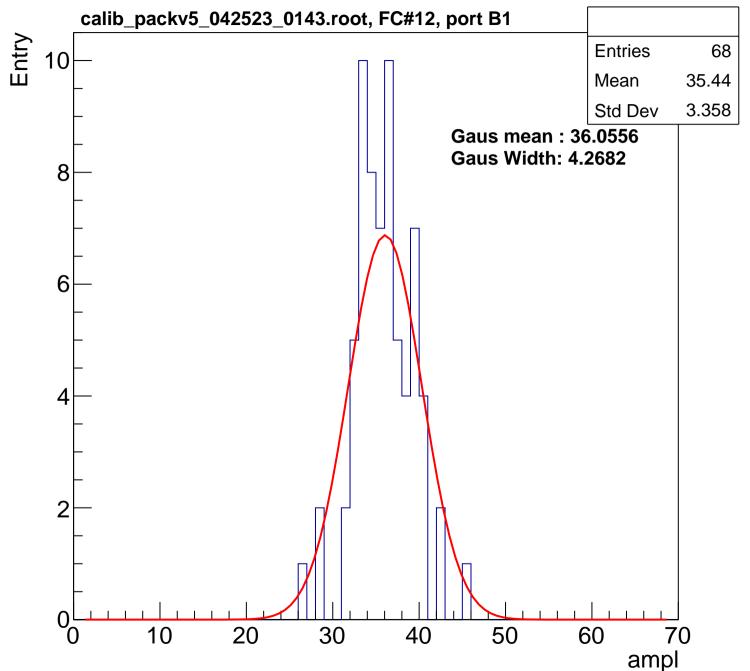


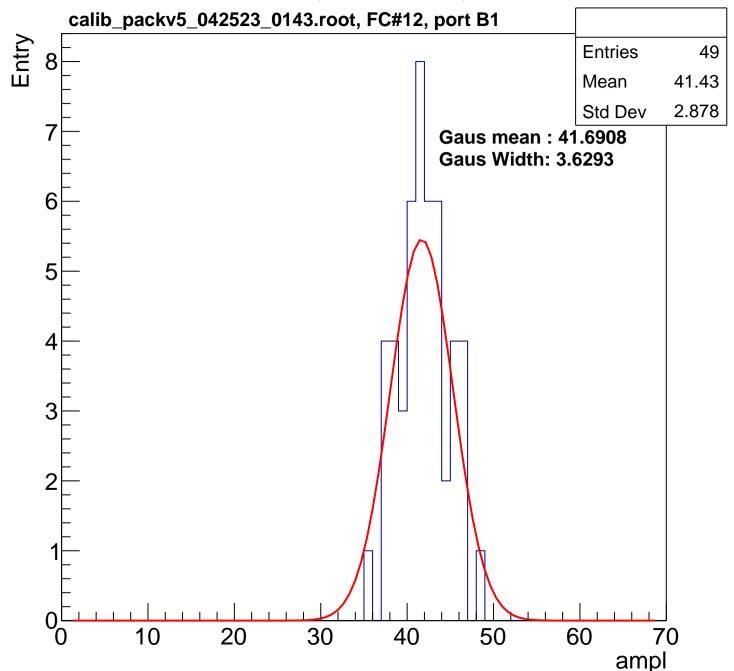


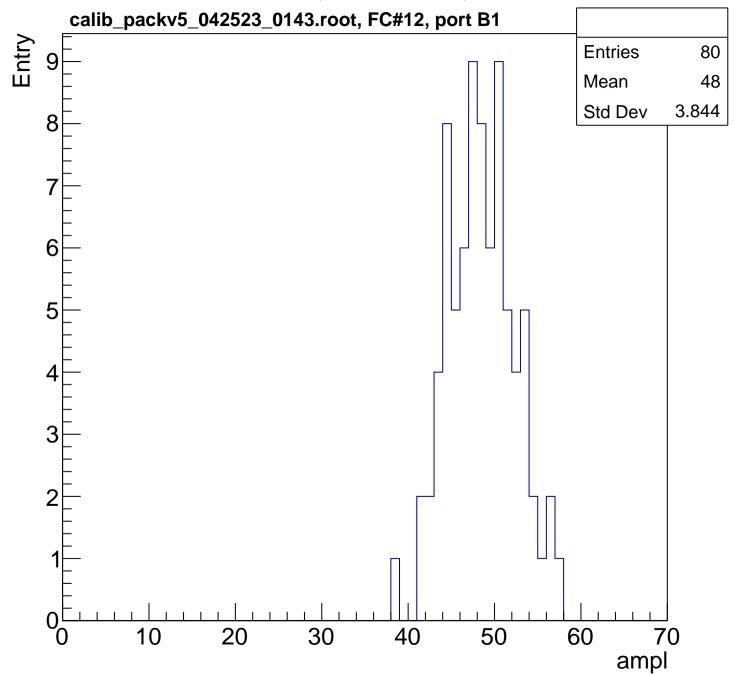


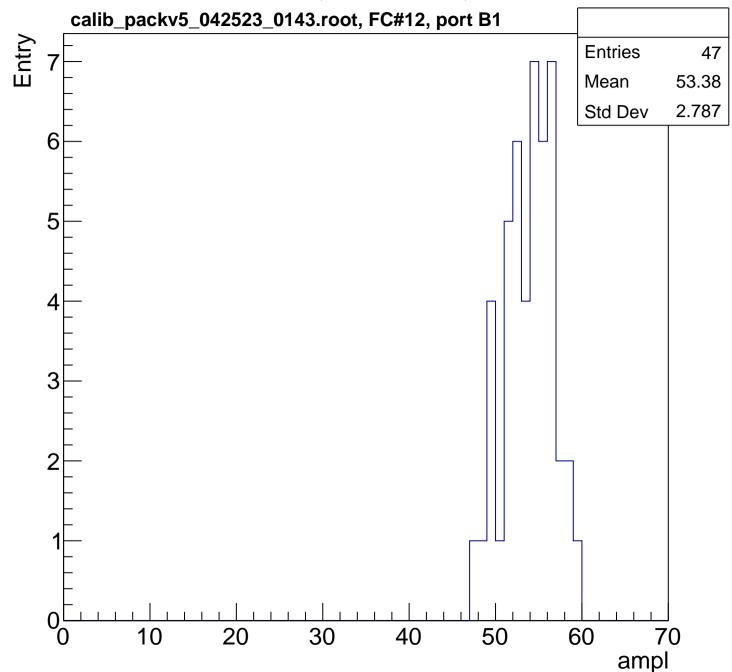
B0L102S, U3-ch66, adc7 calib_packv5_042523_0143.root, FC#12, port B1 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

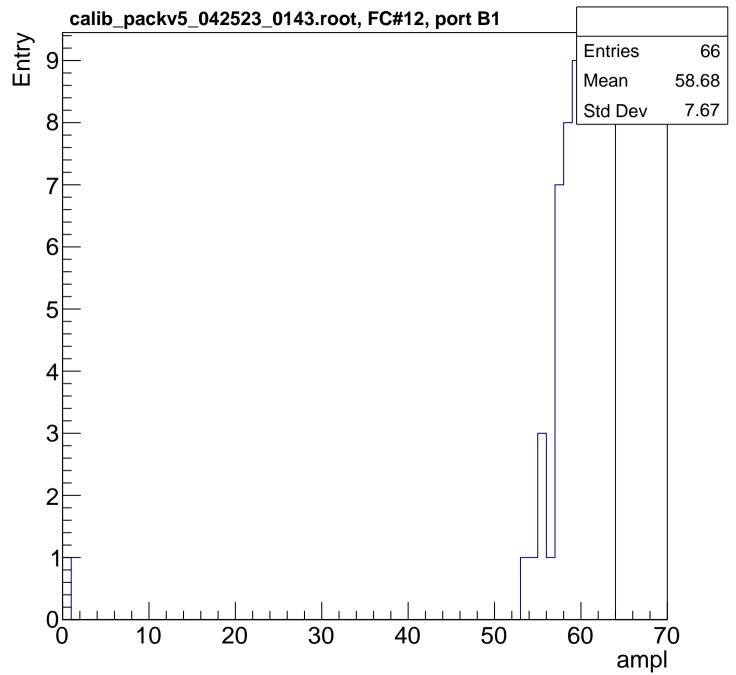


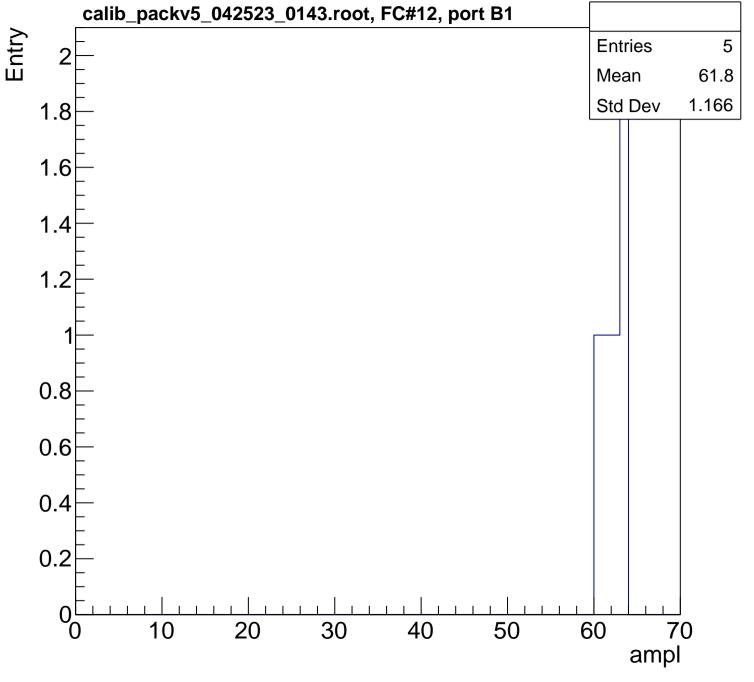


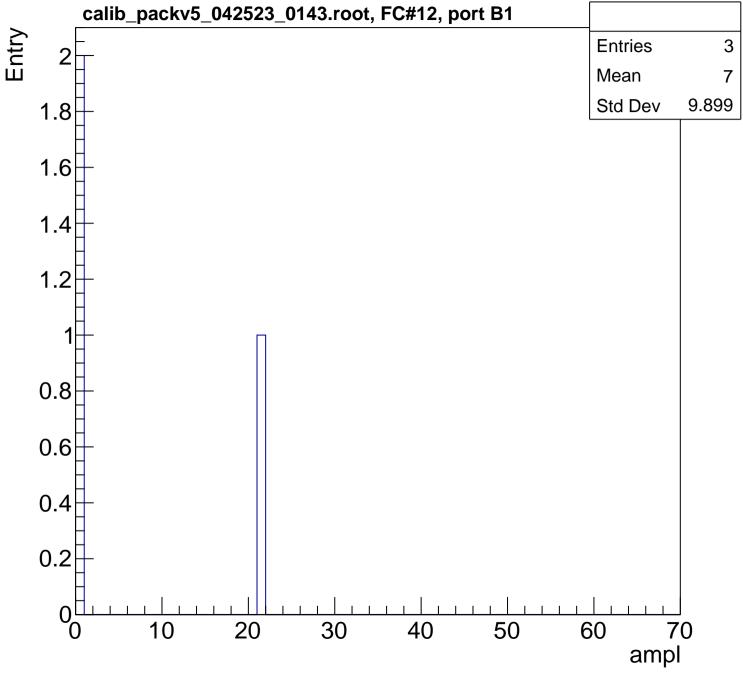


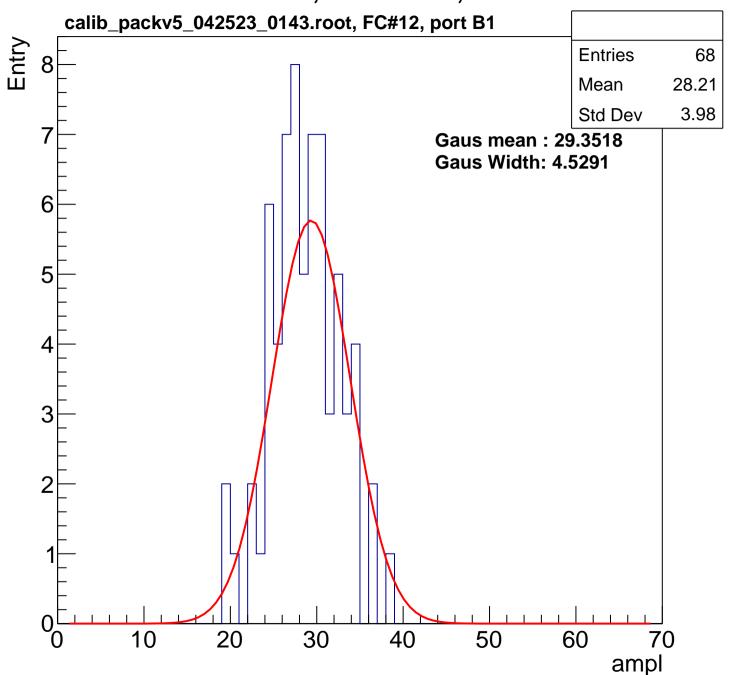


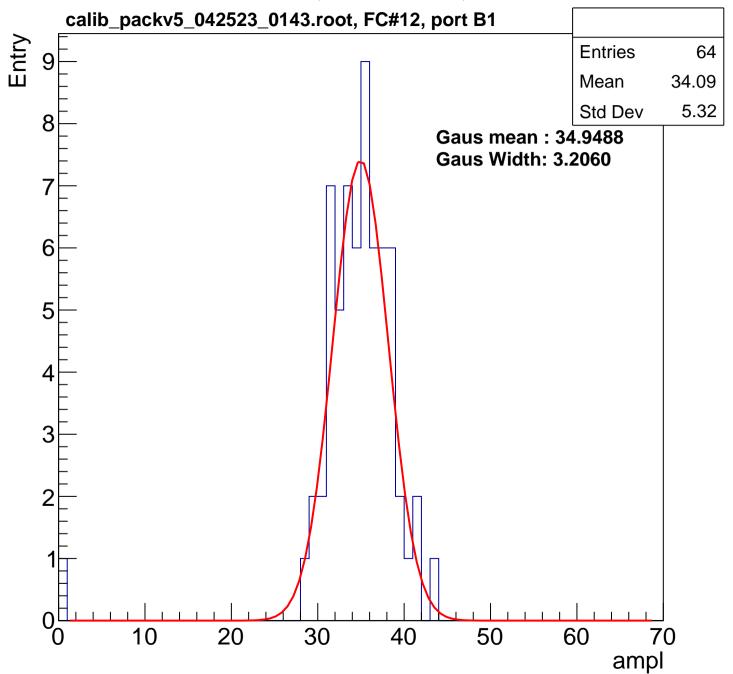


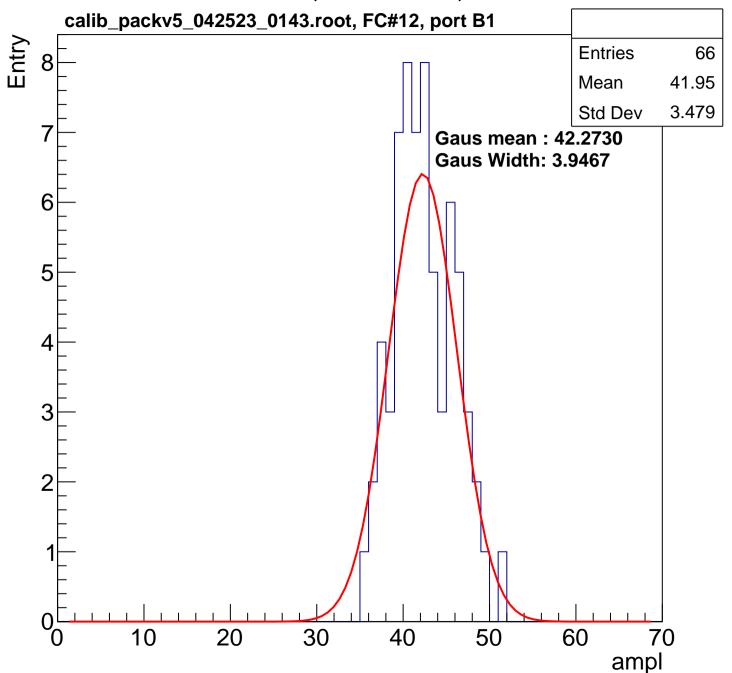


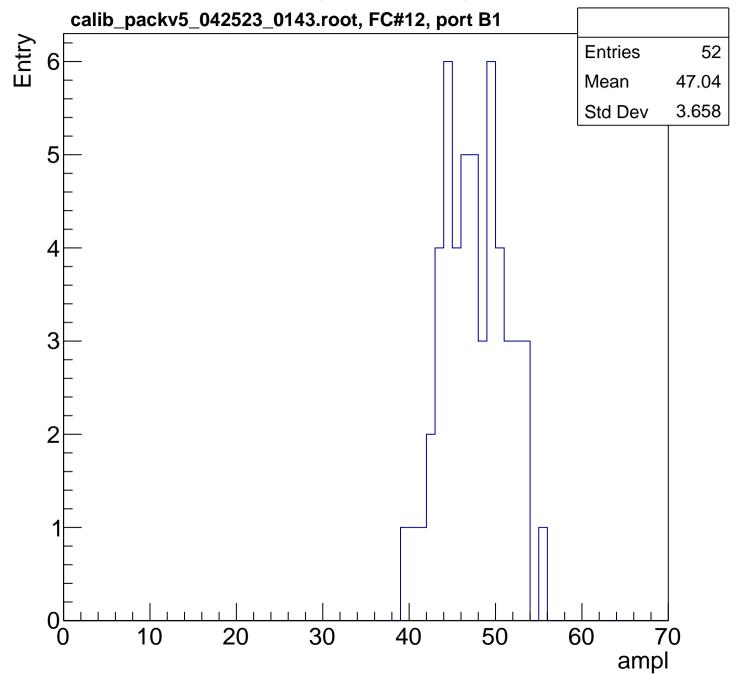


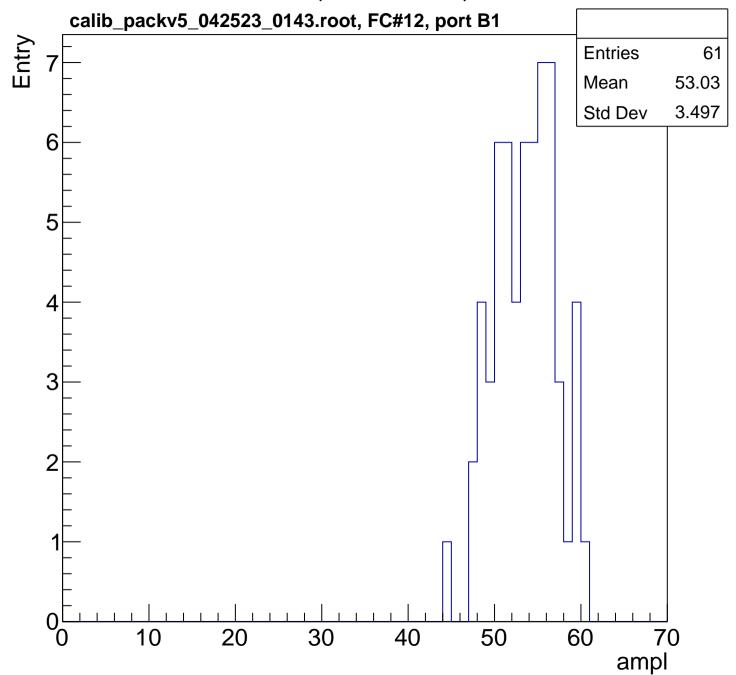


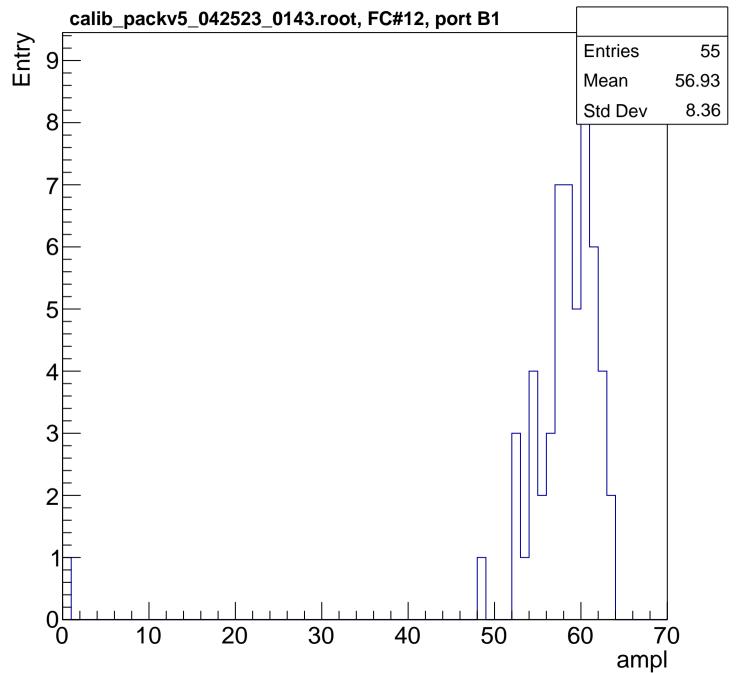


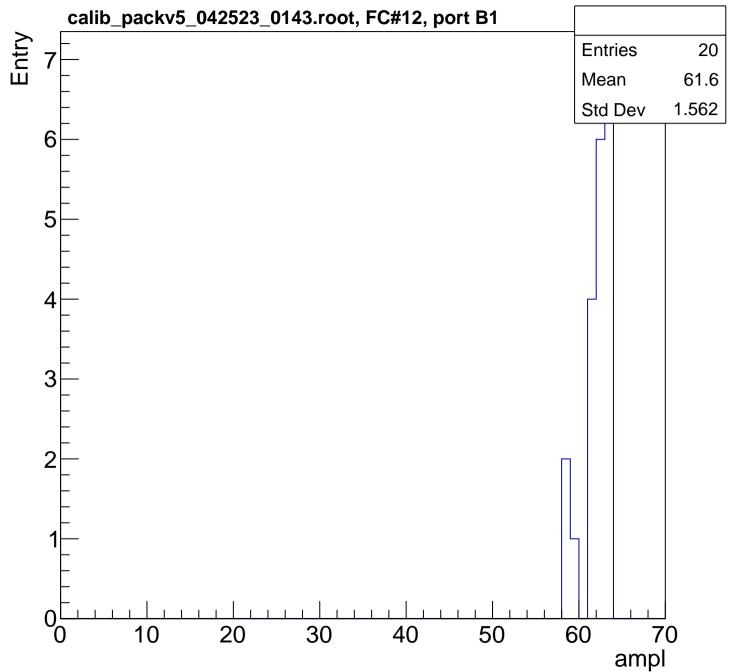


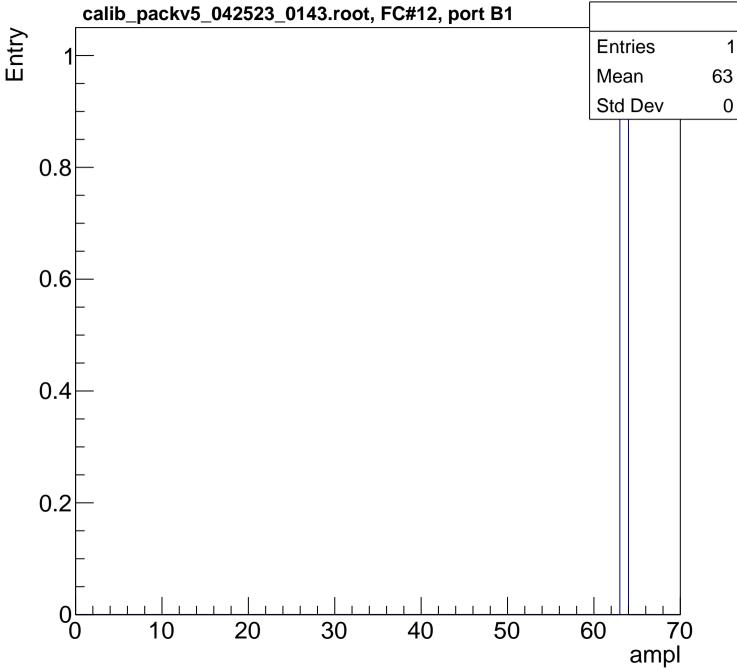


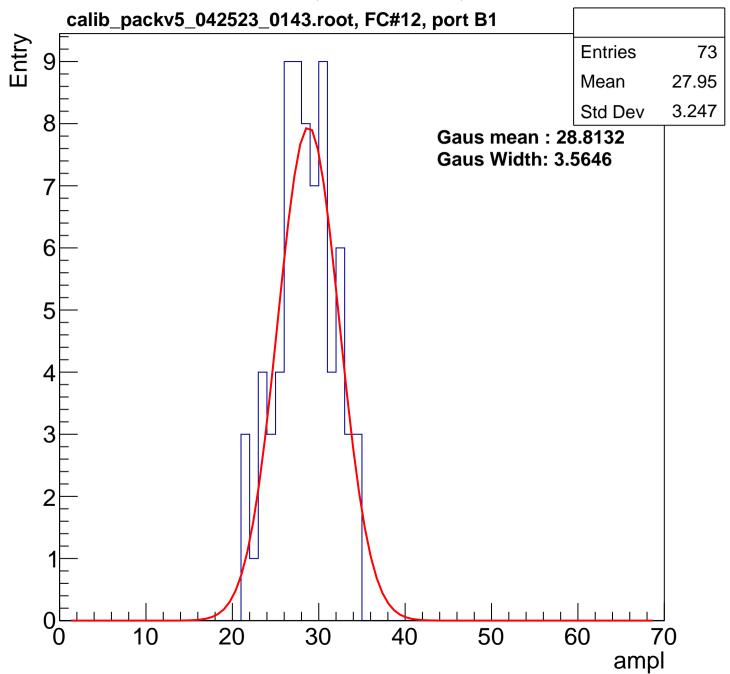


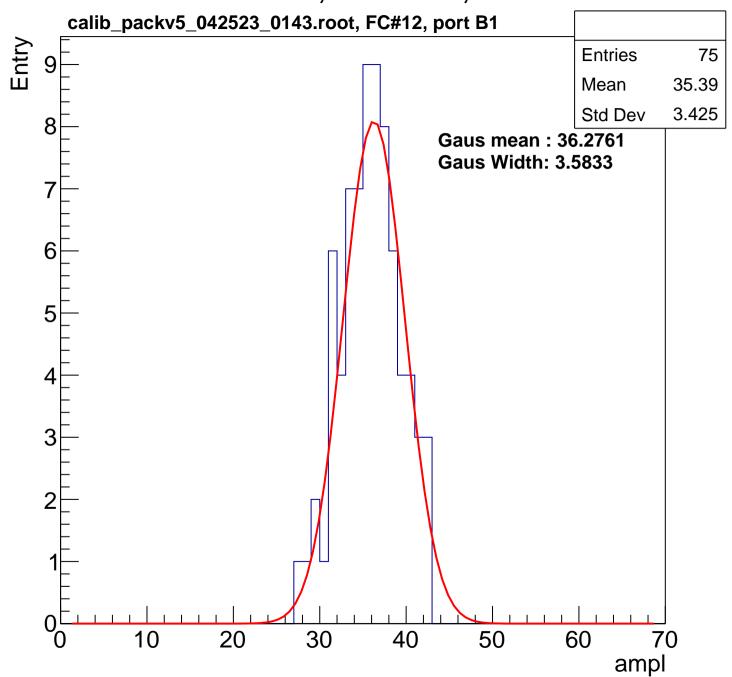


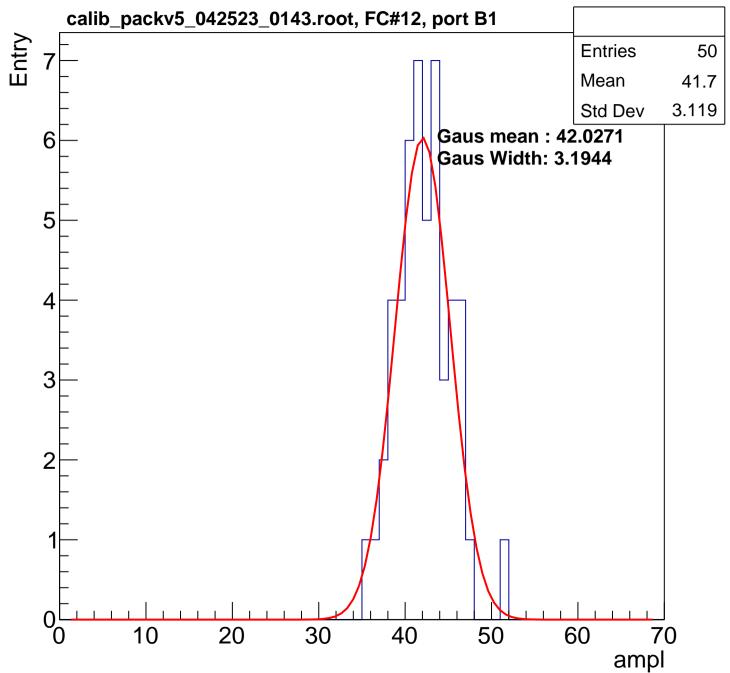


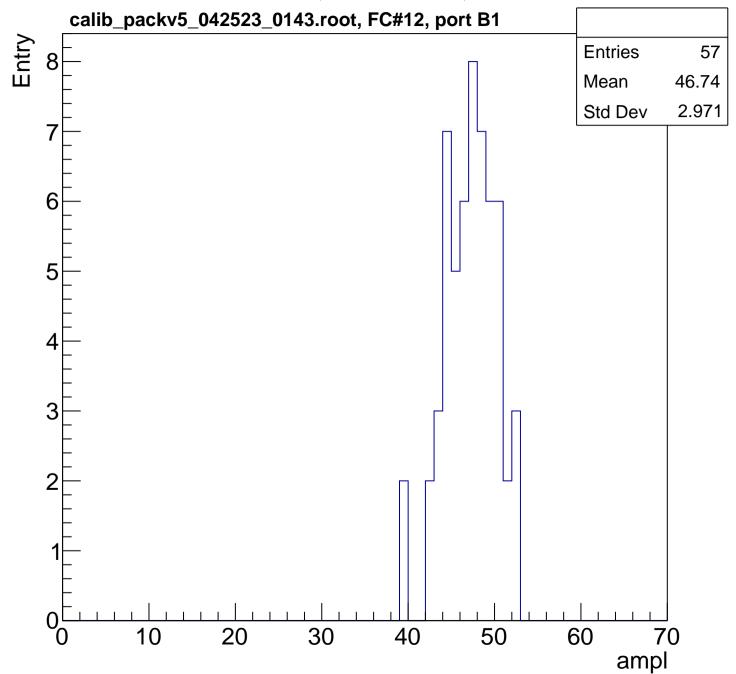


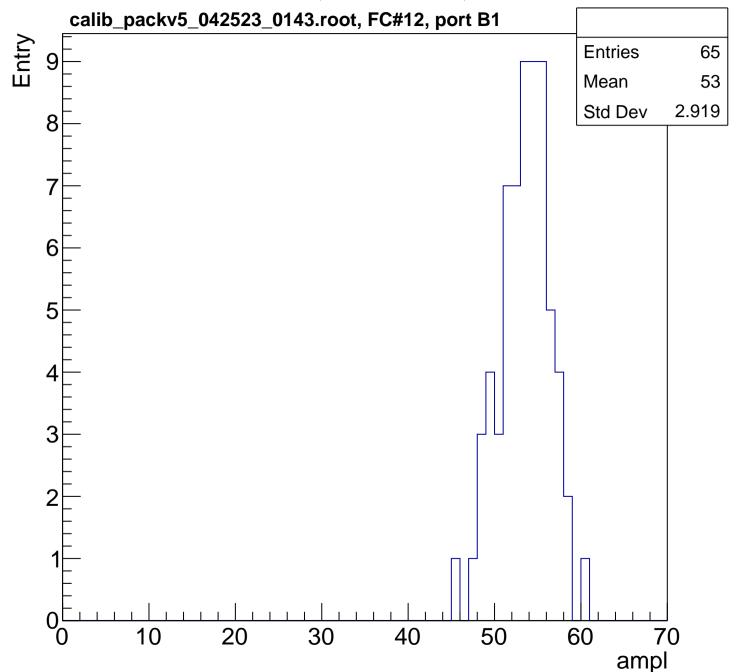


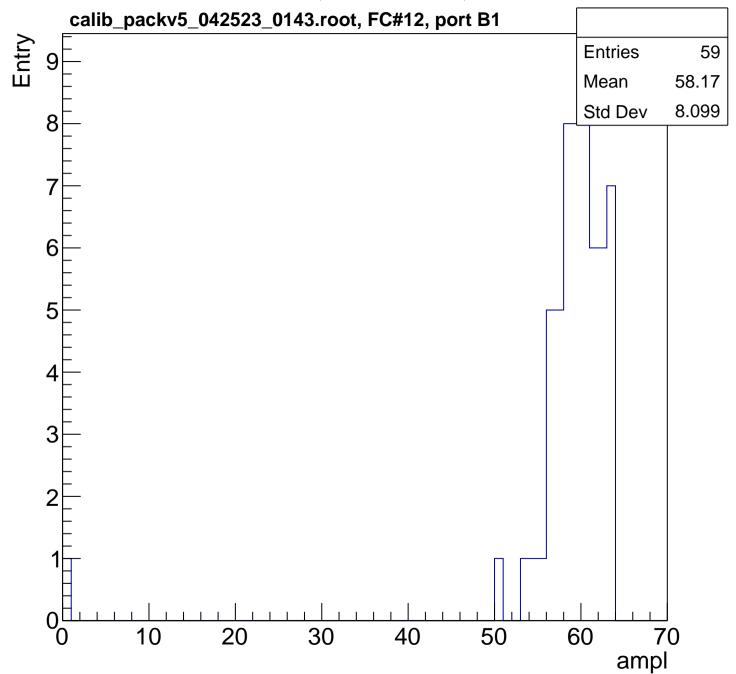


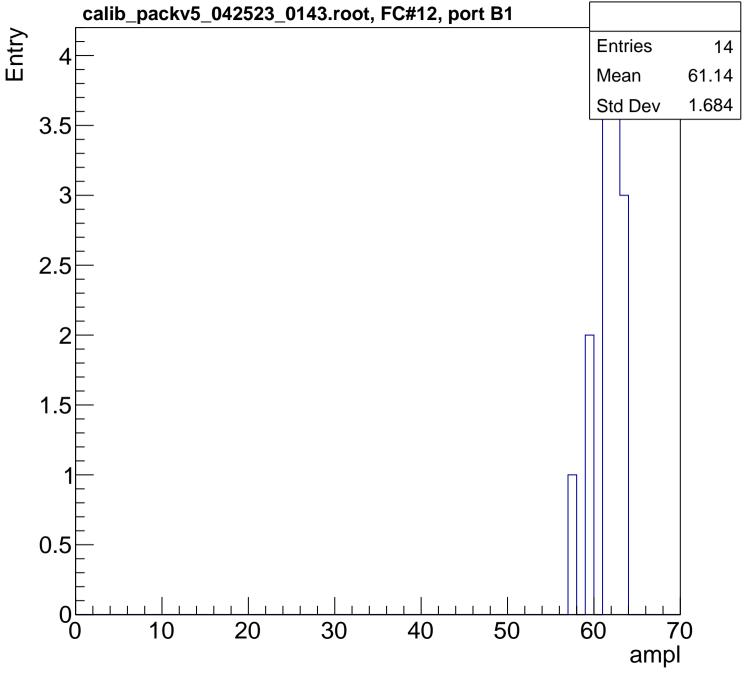


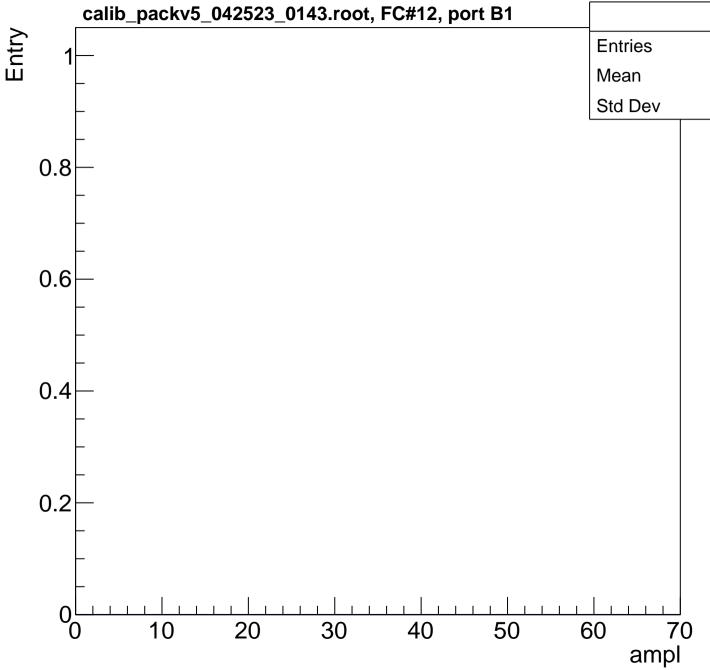


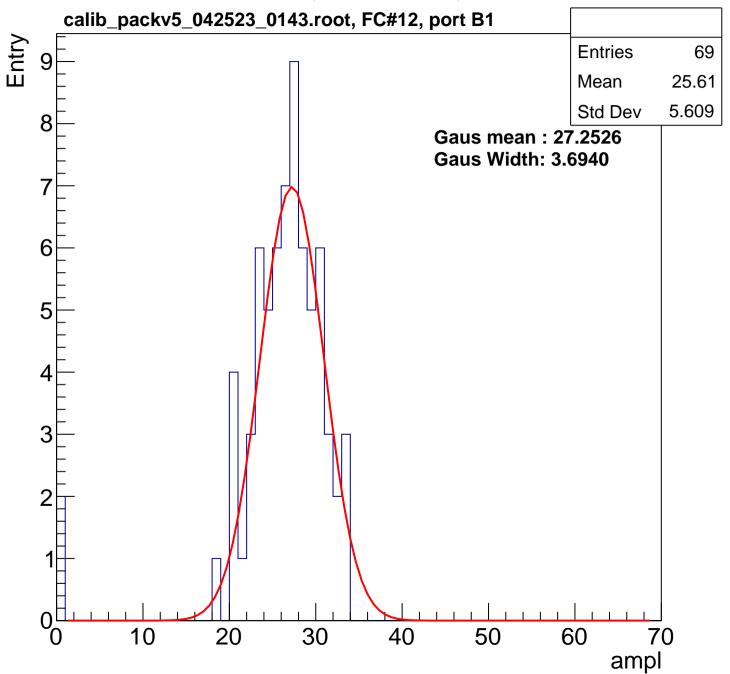


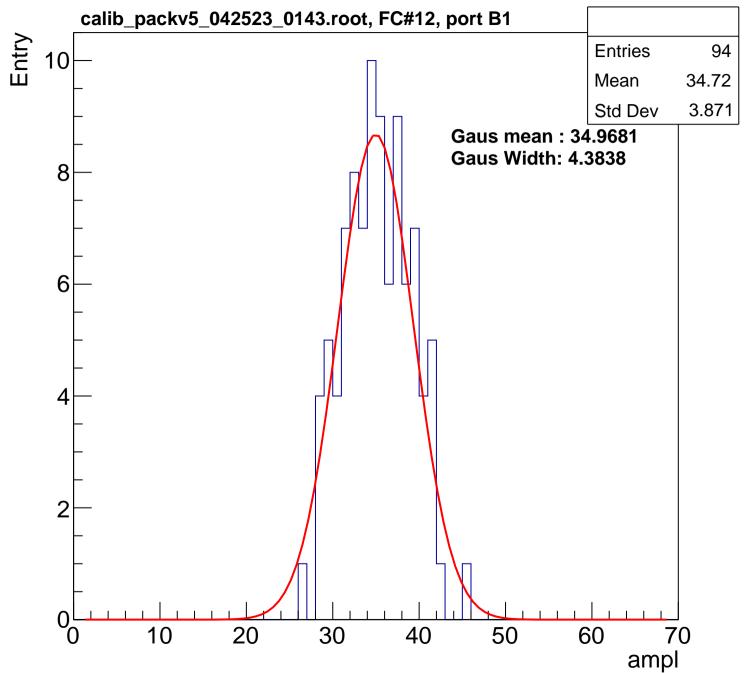


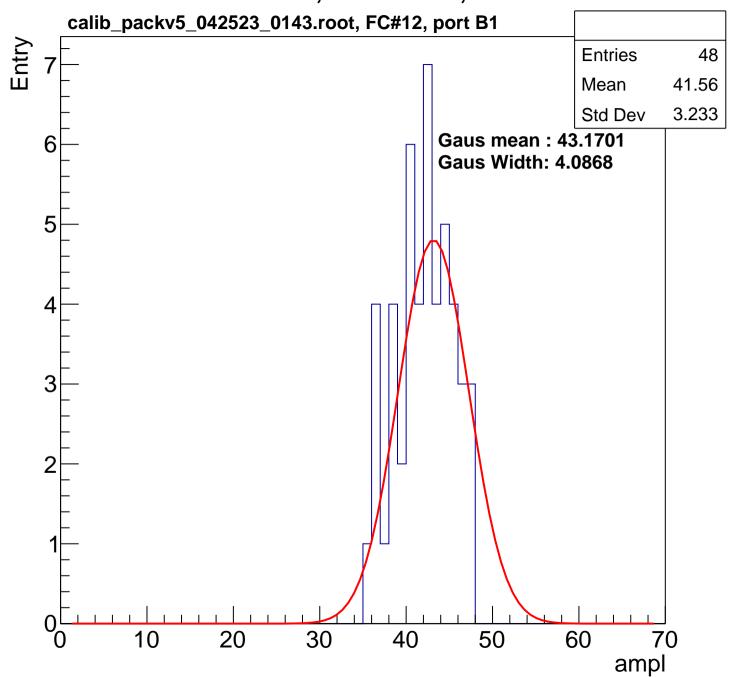


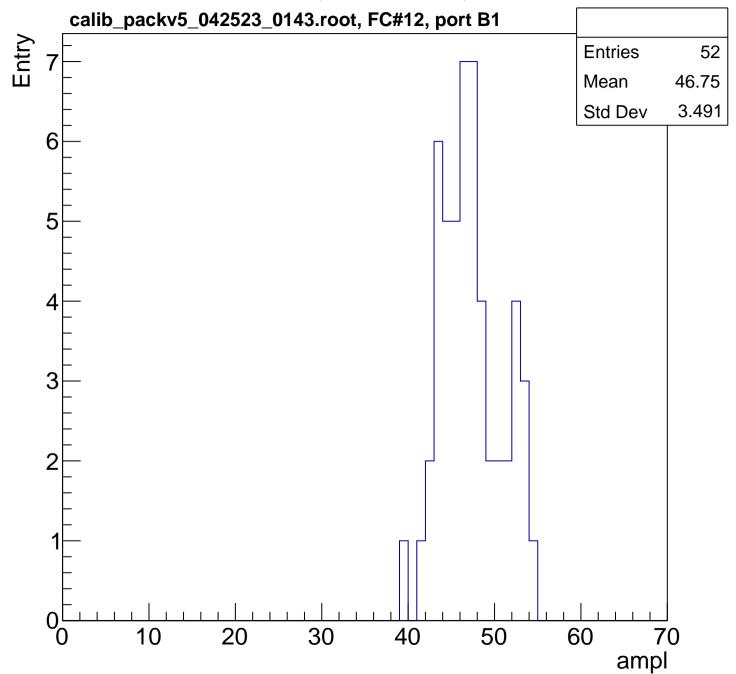


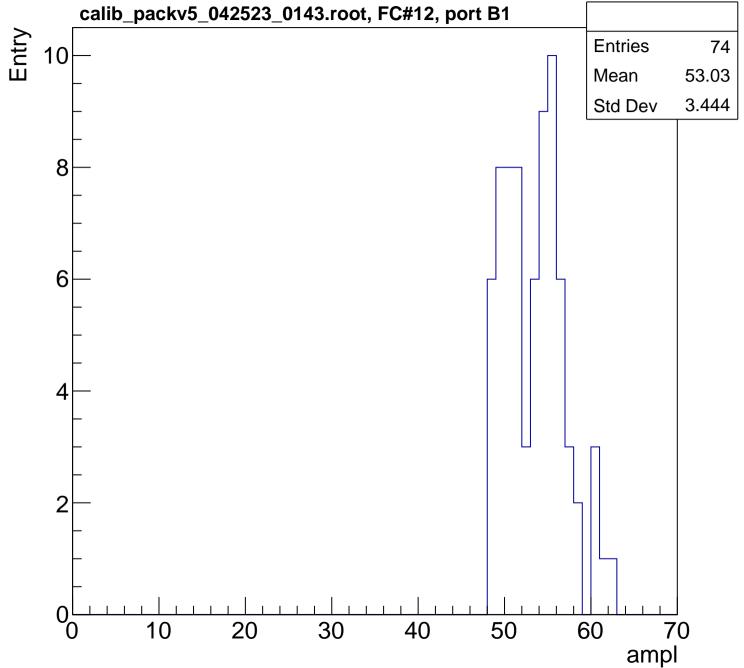


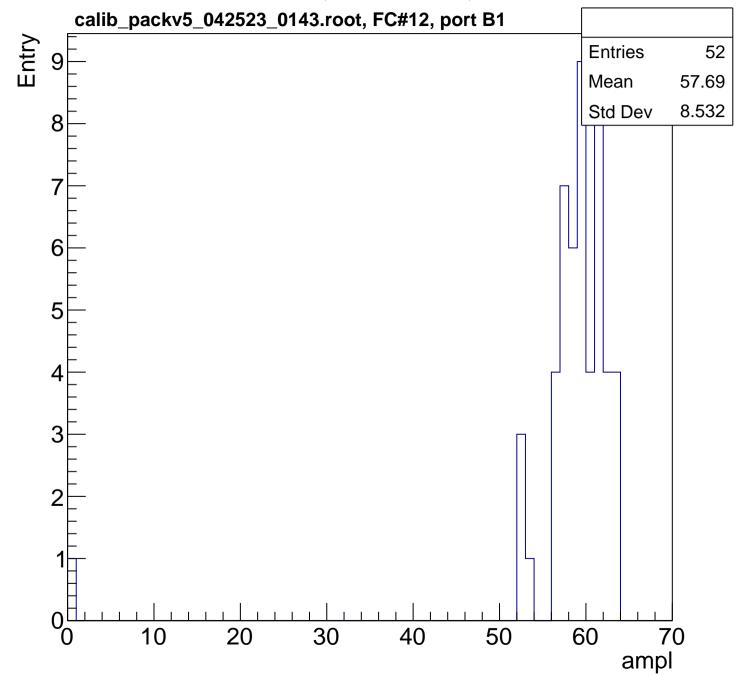


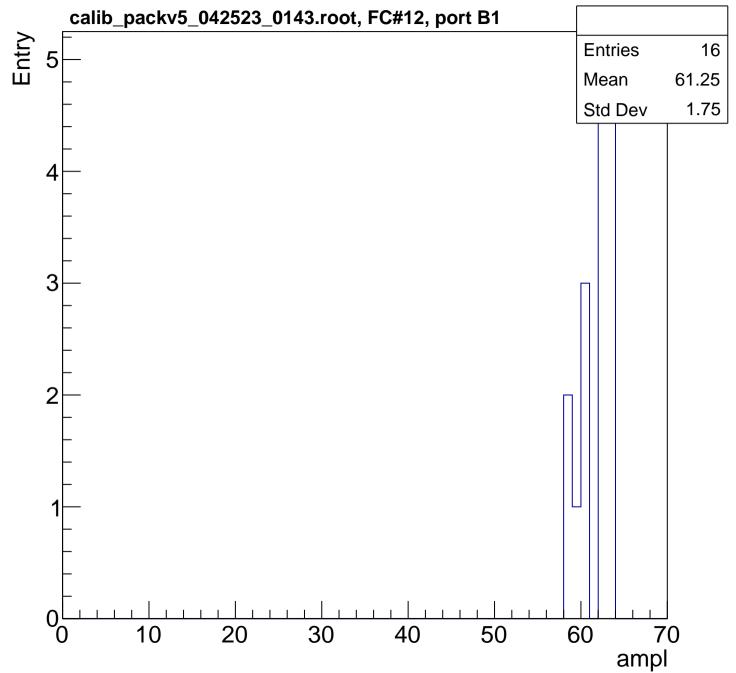




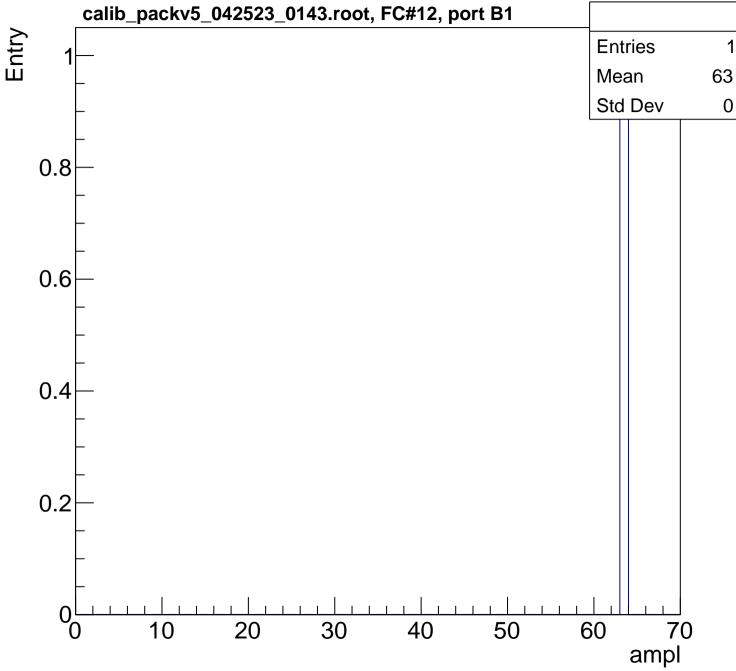


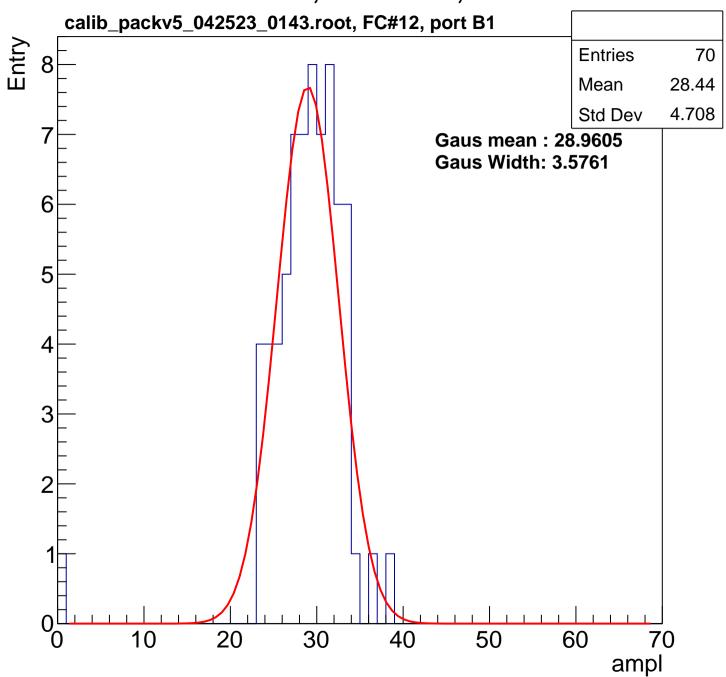


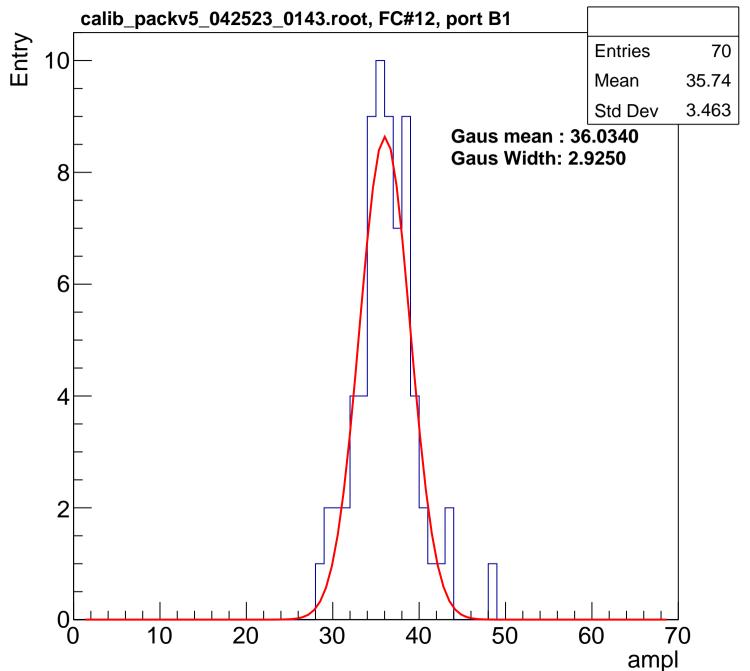


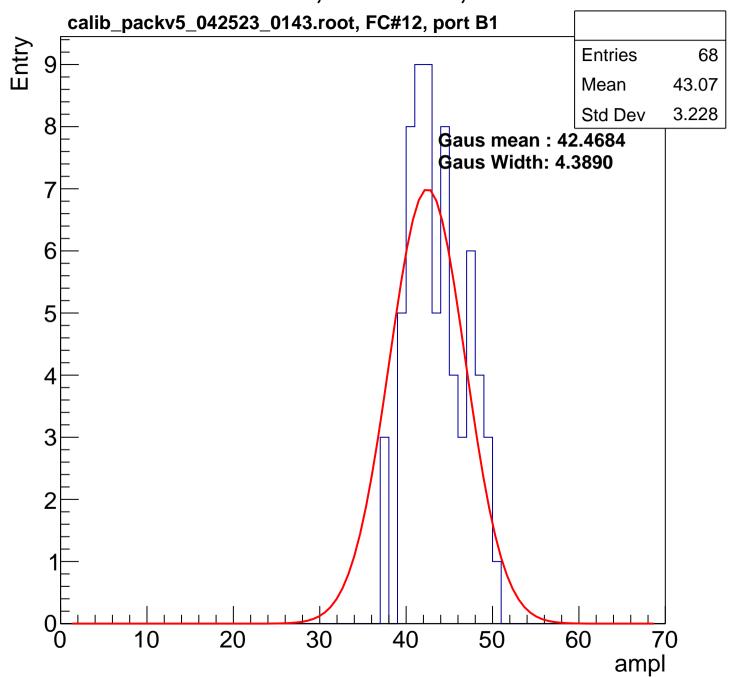


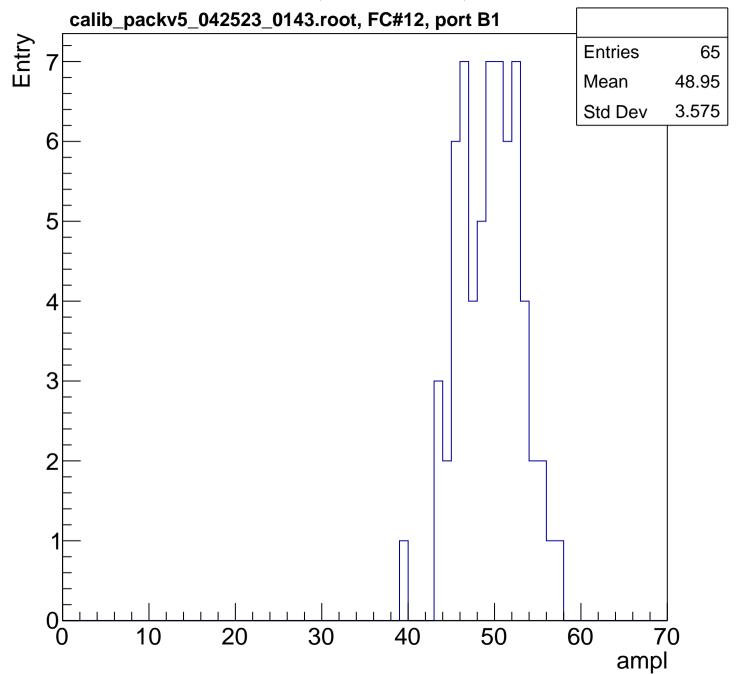
0

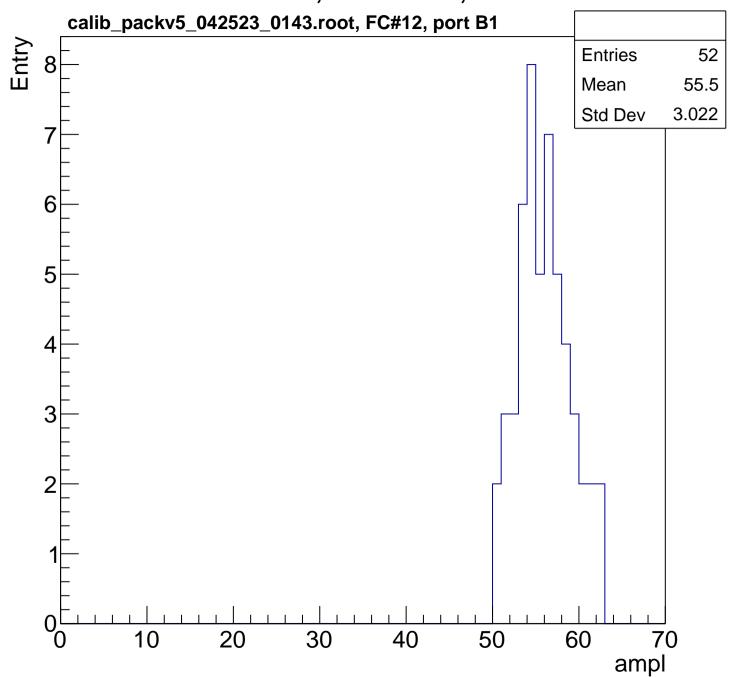


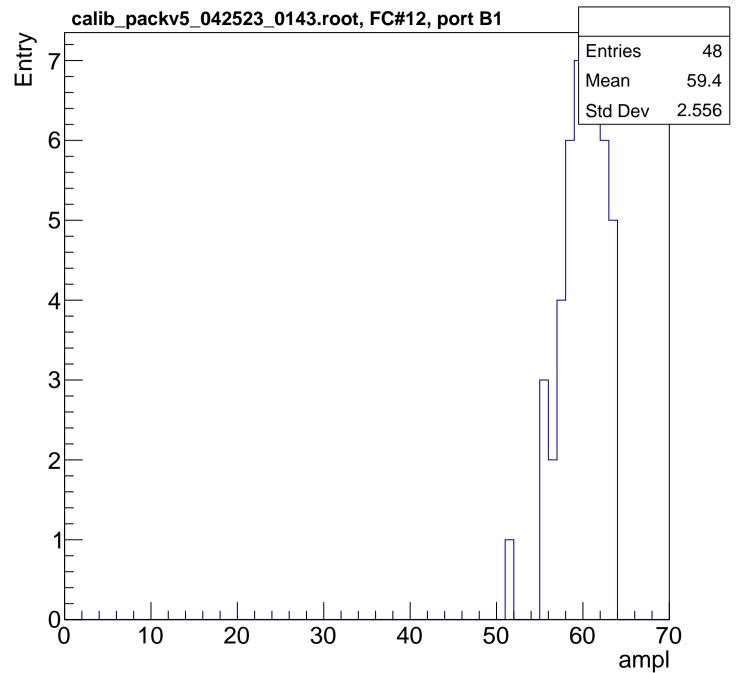


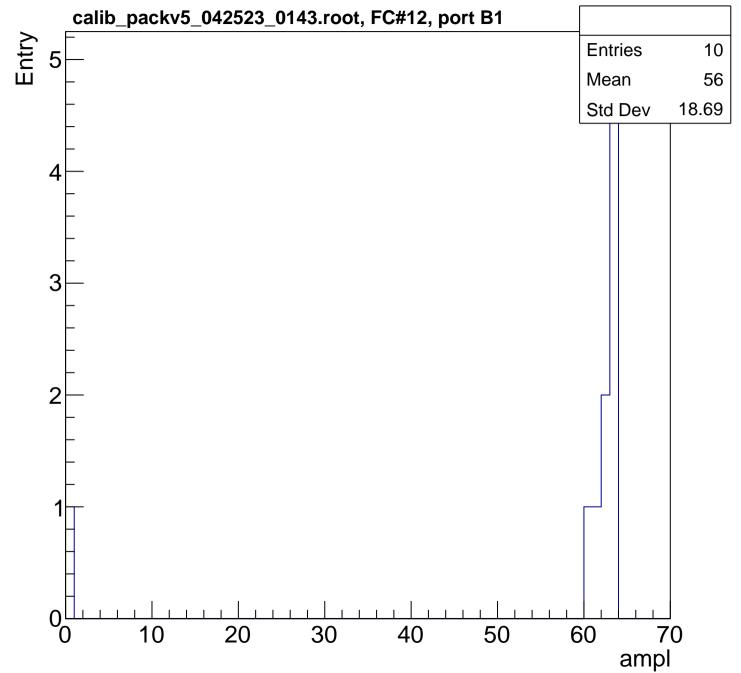




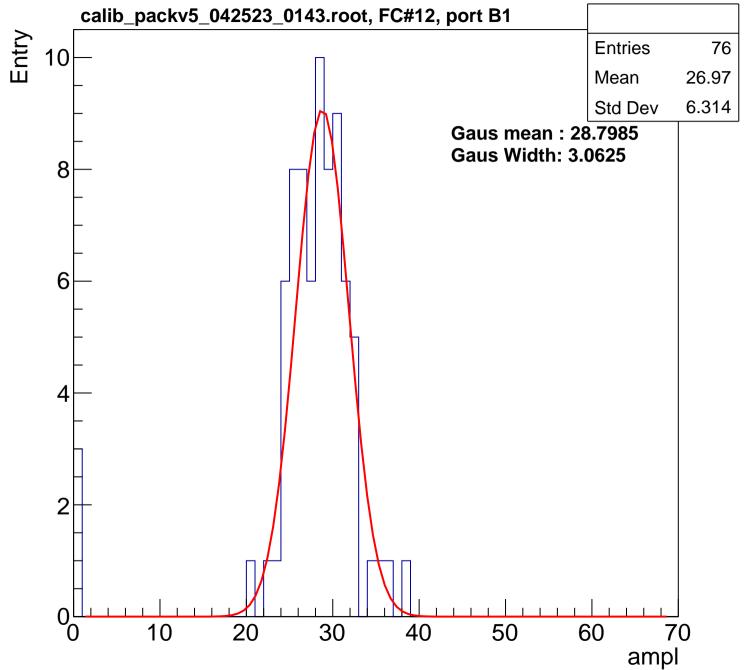


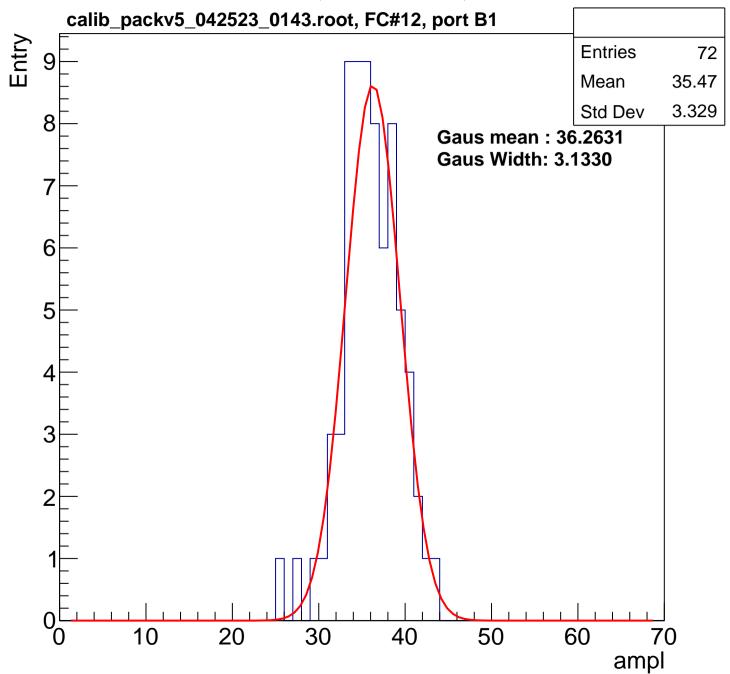


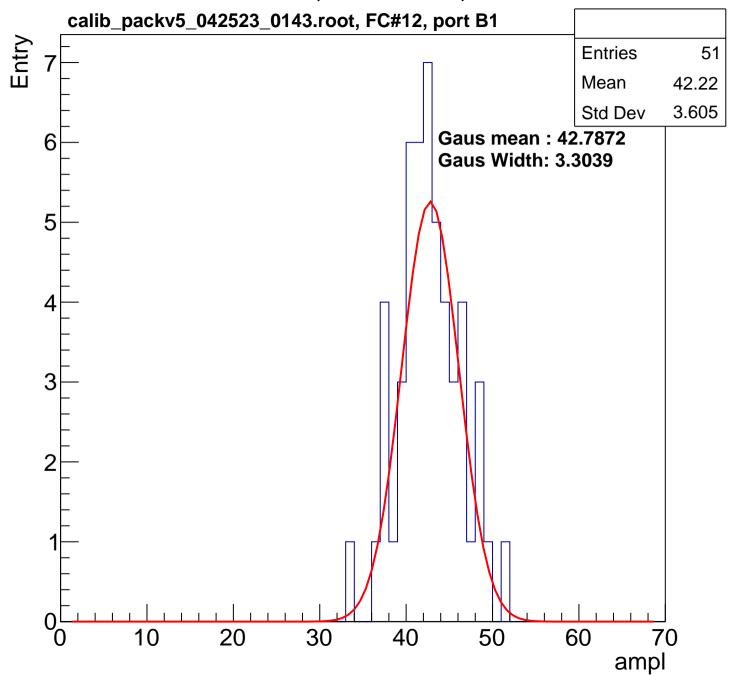


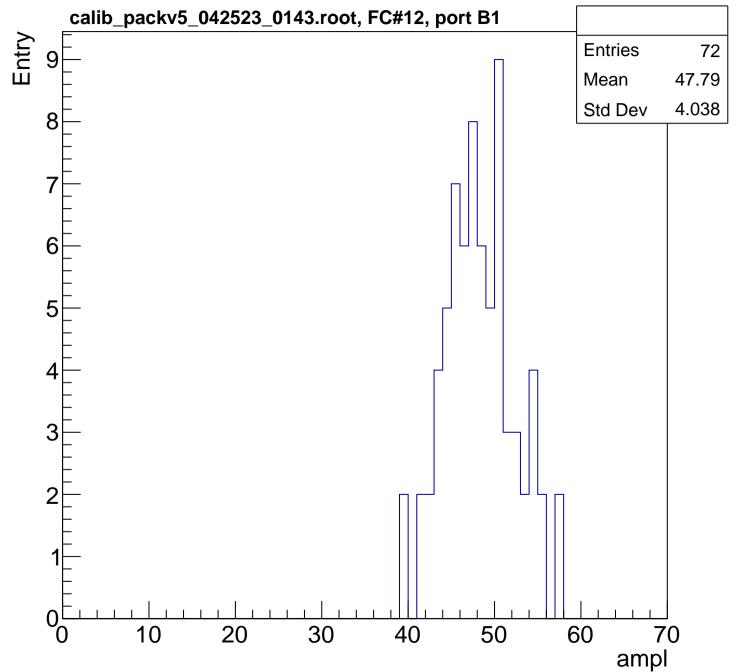


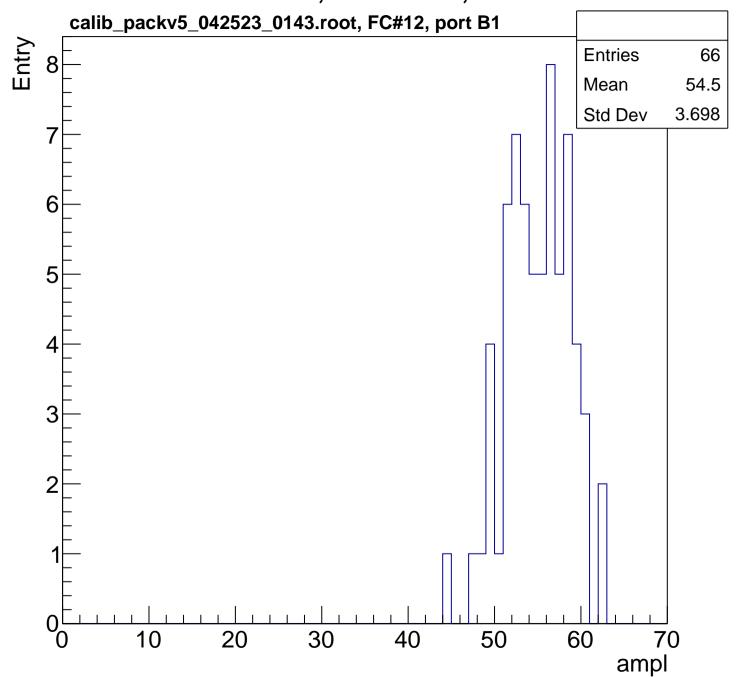


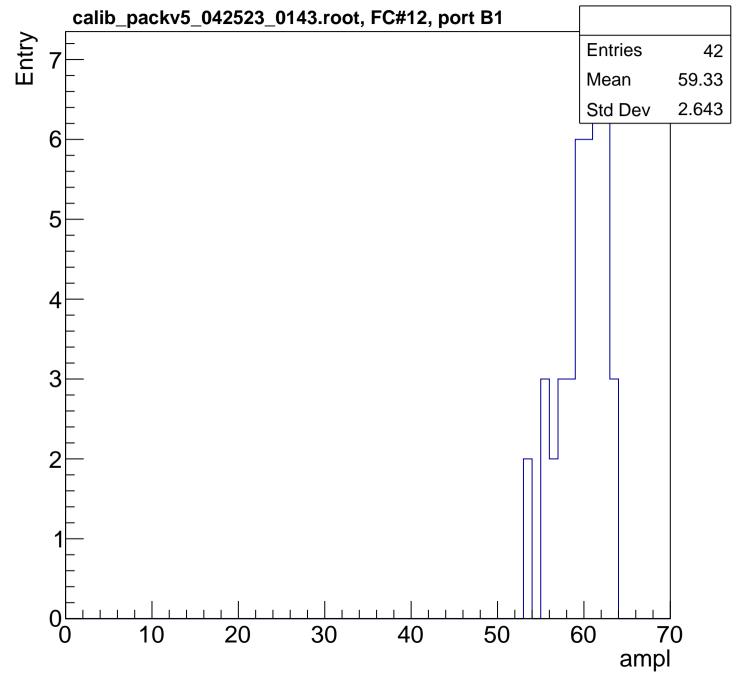


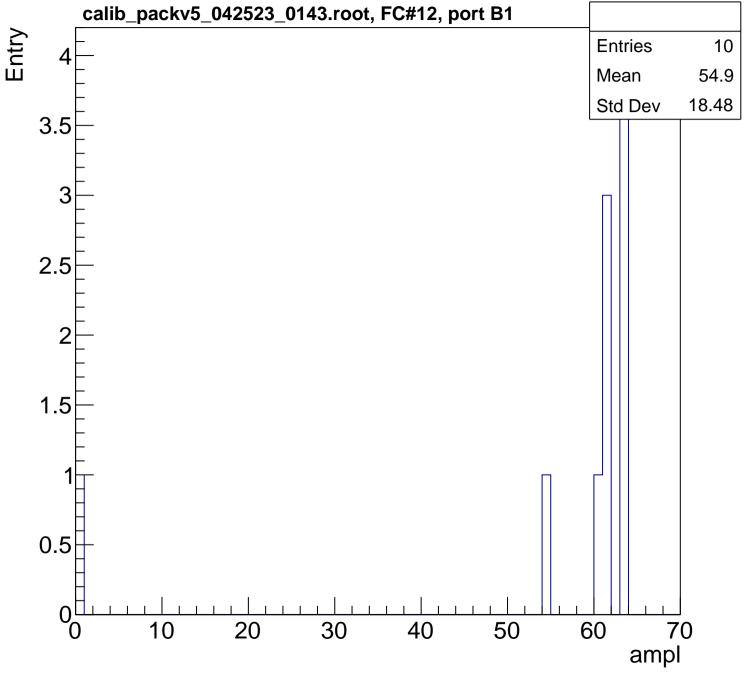


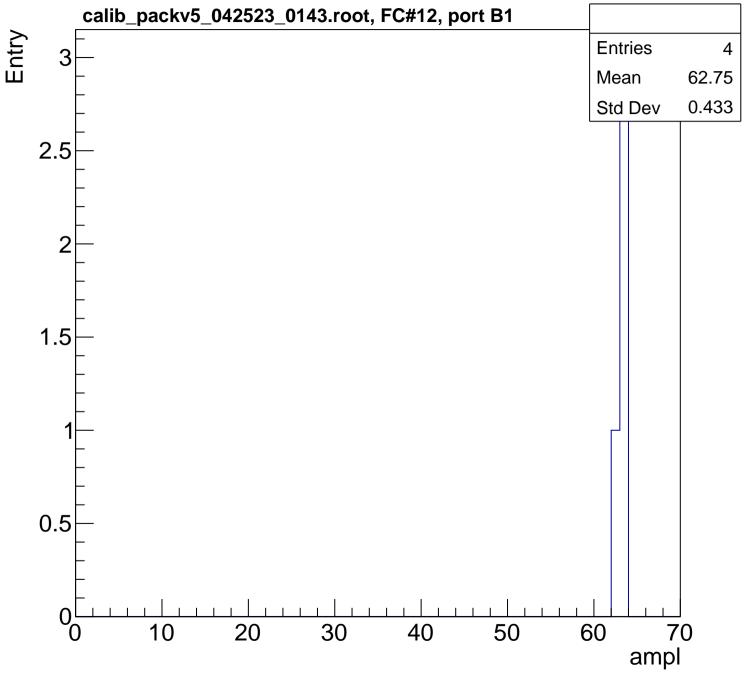


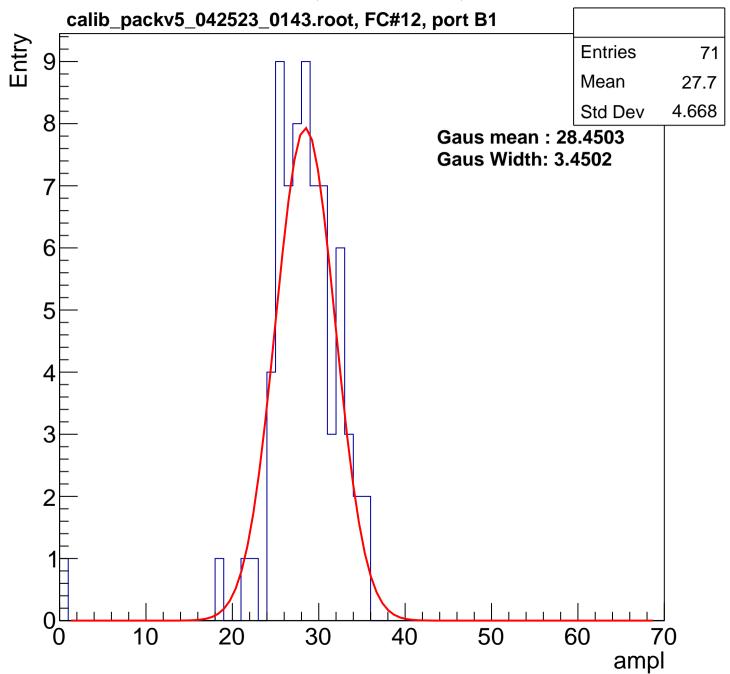


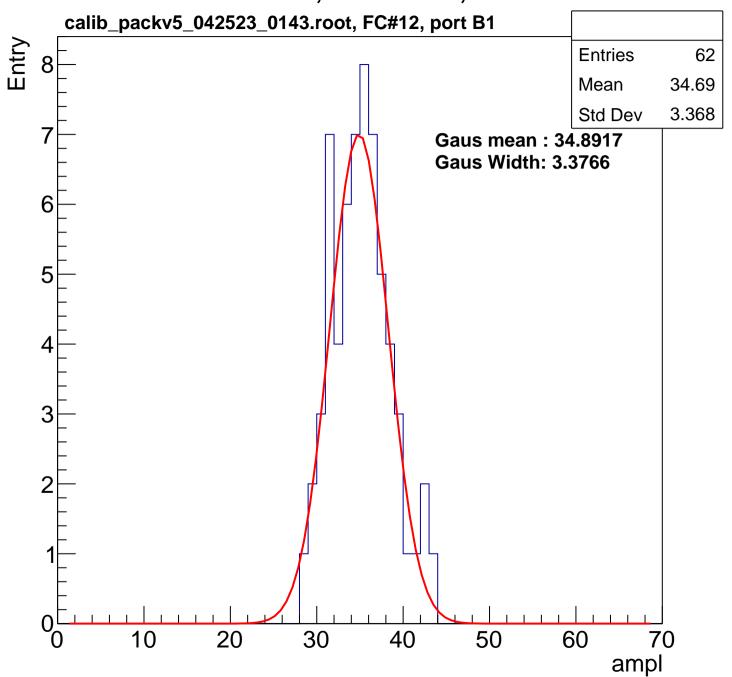


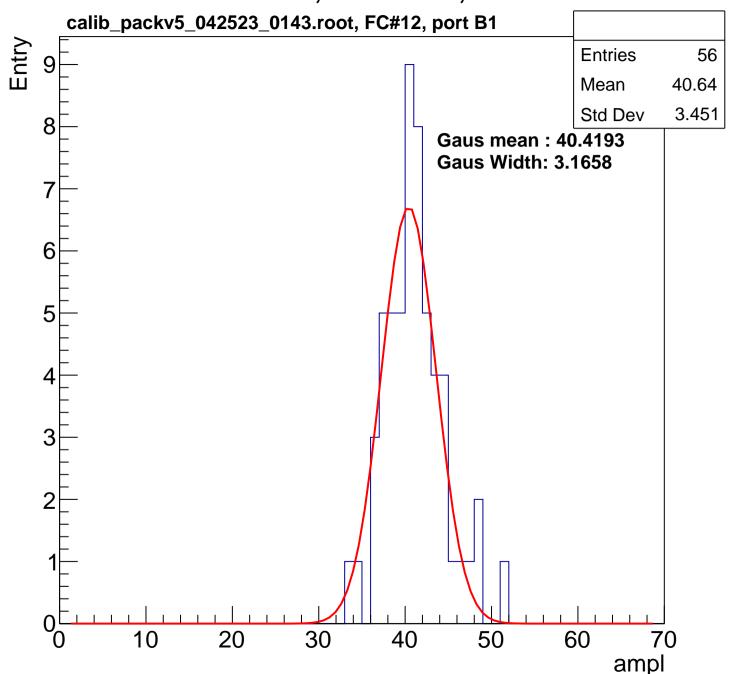


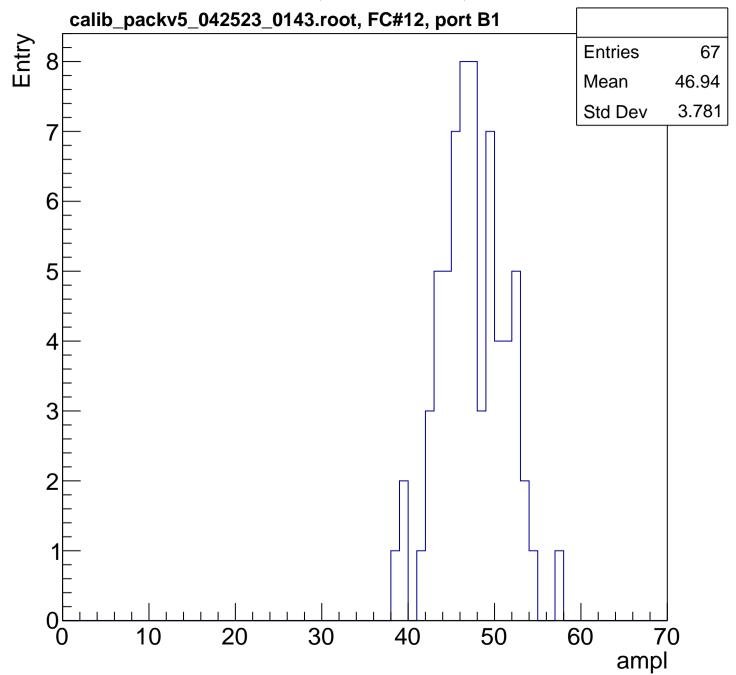


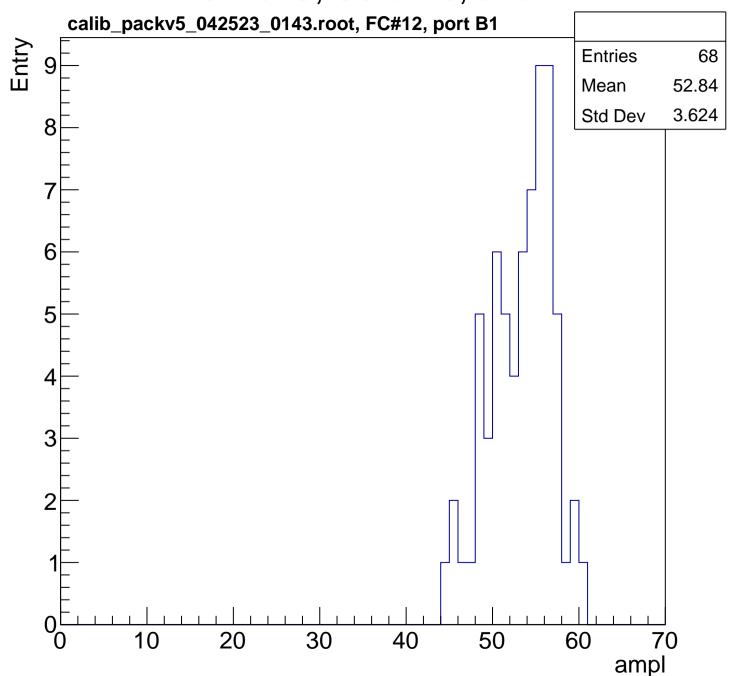


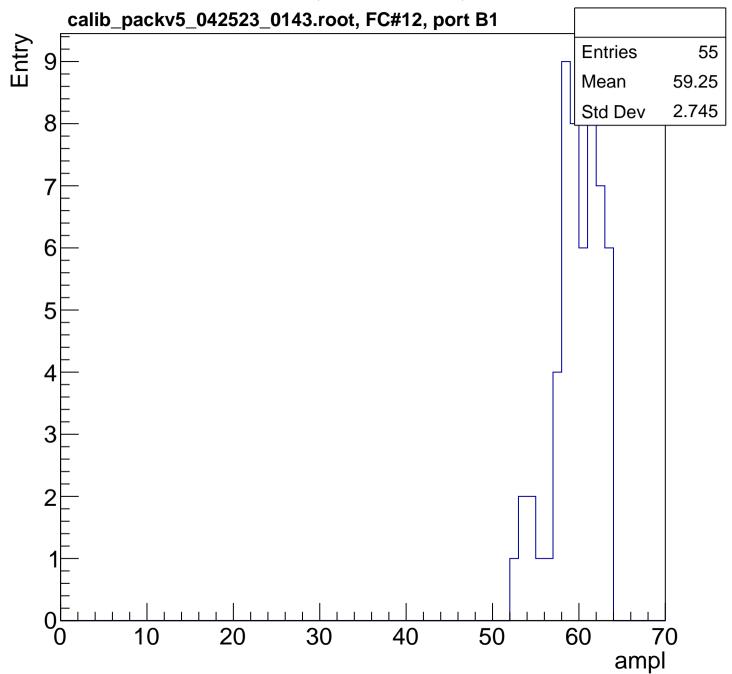


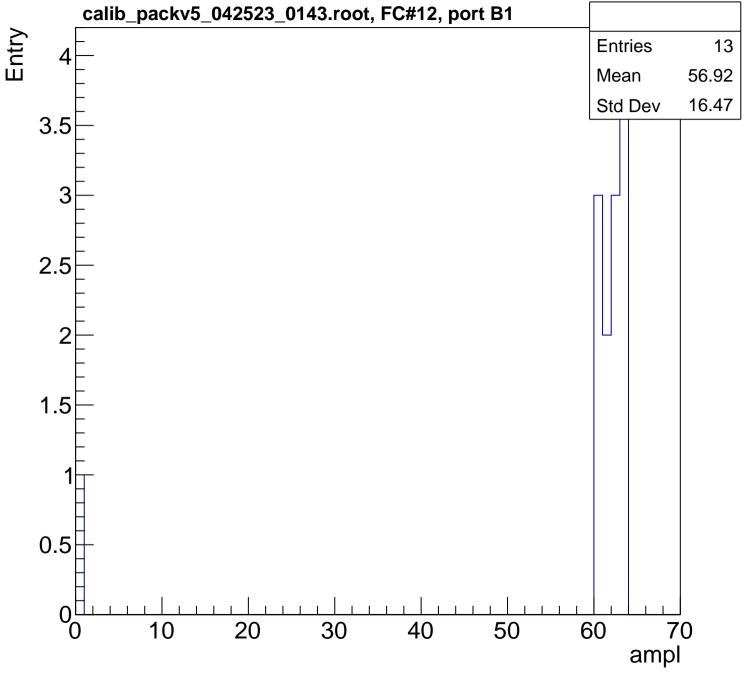


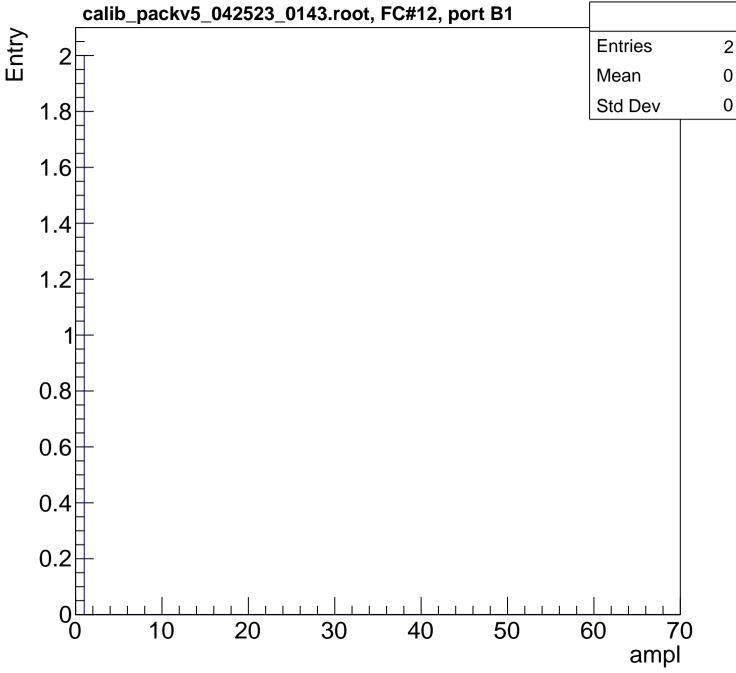


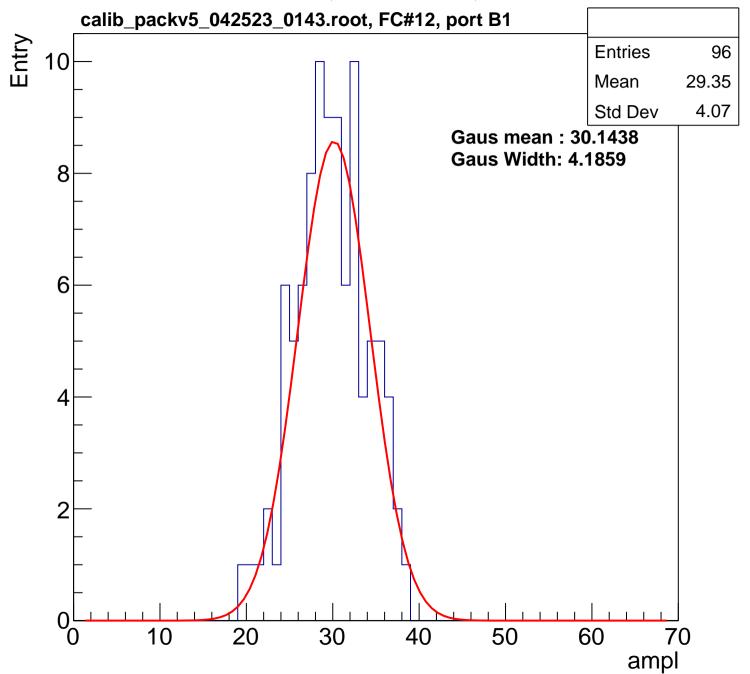


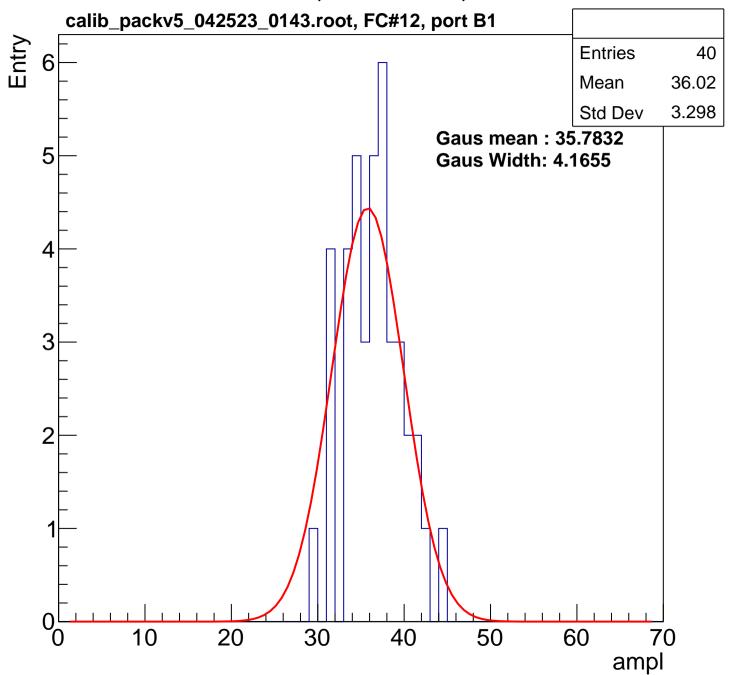


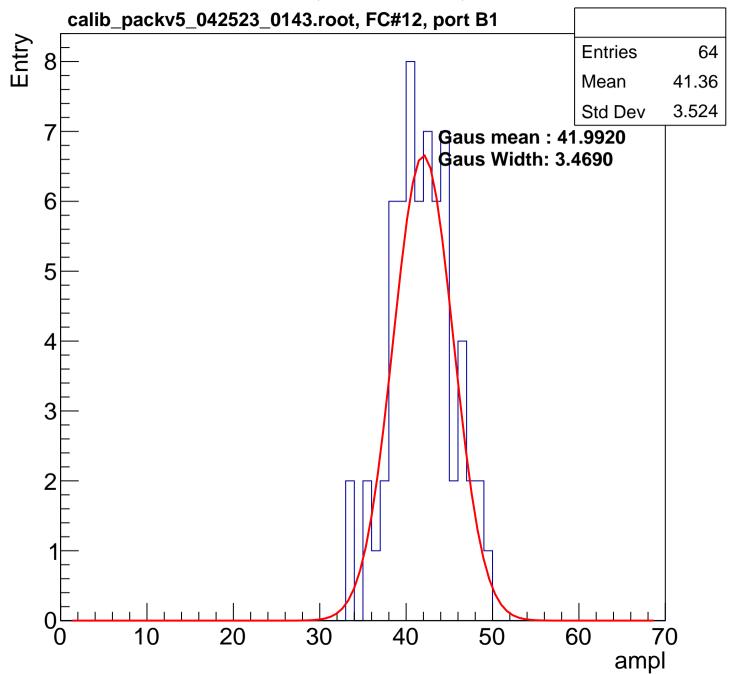


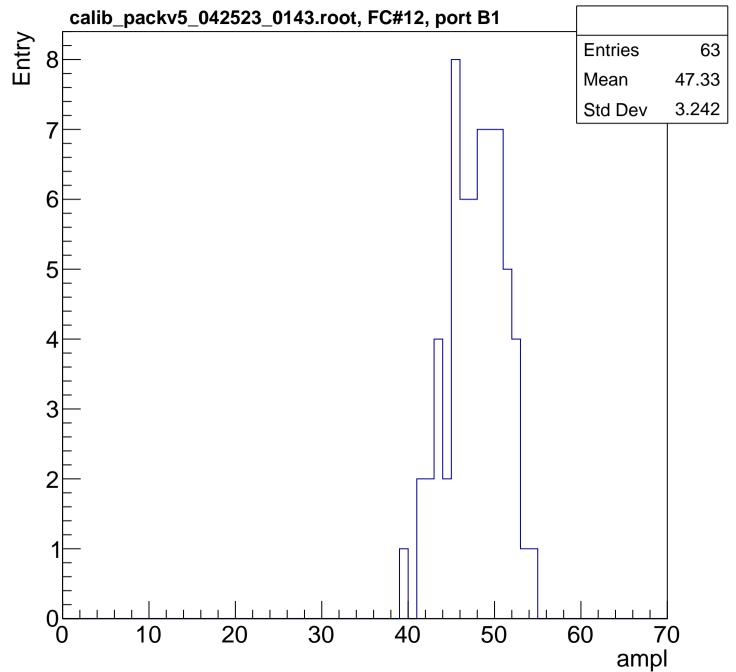


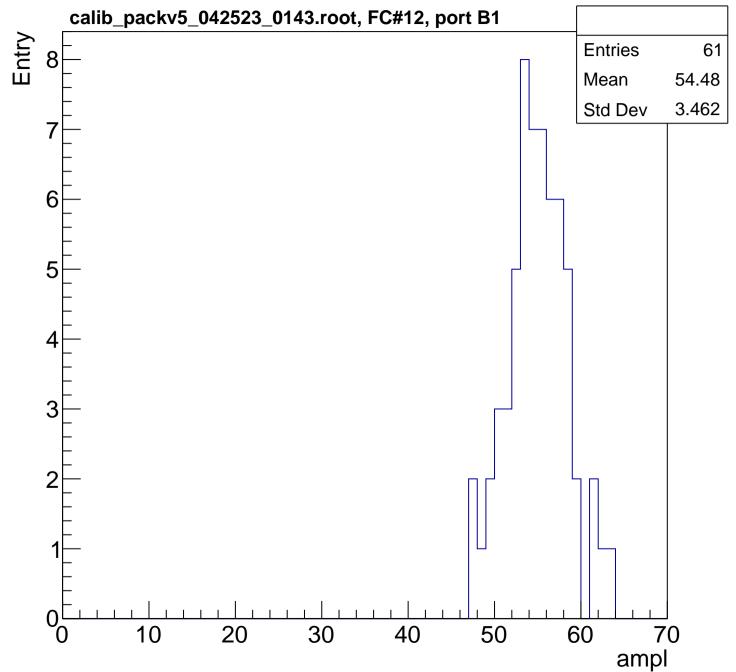


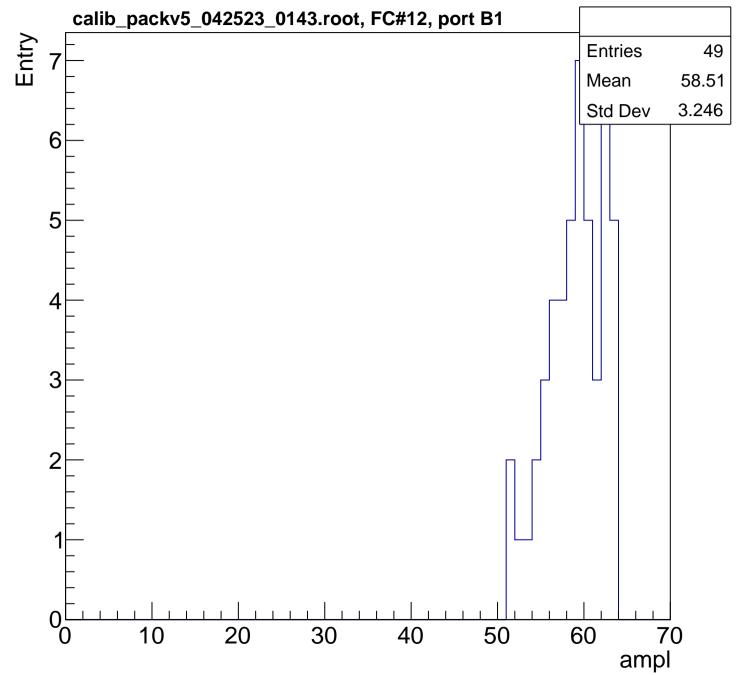


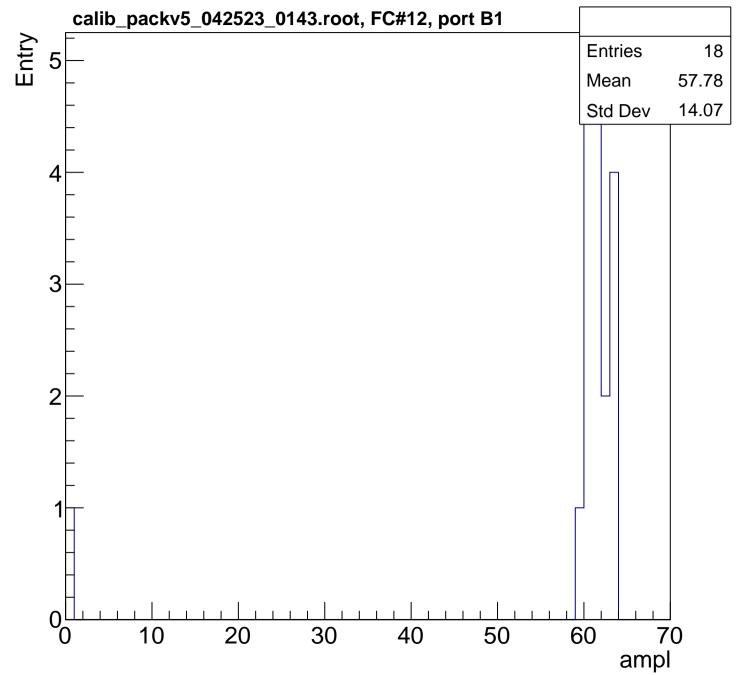


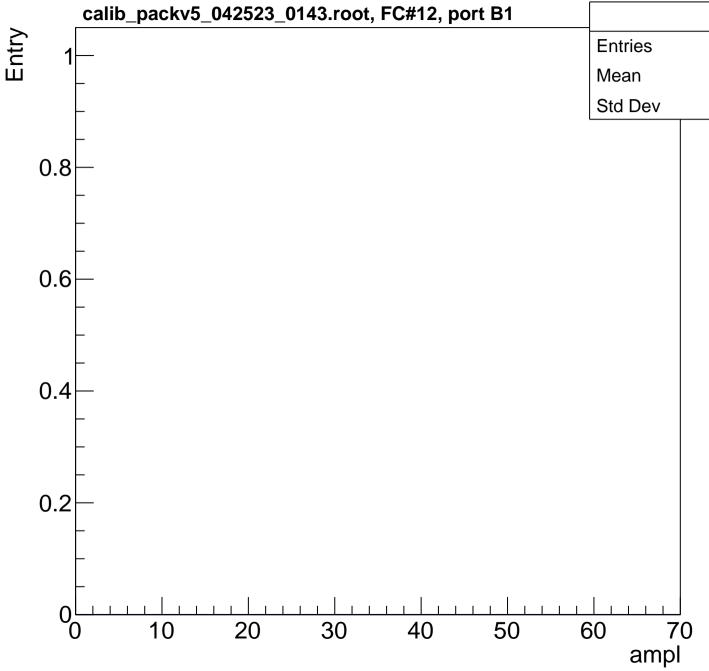


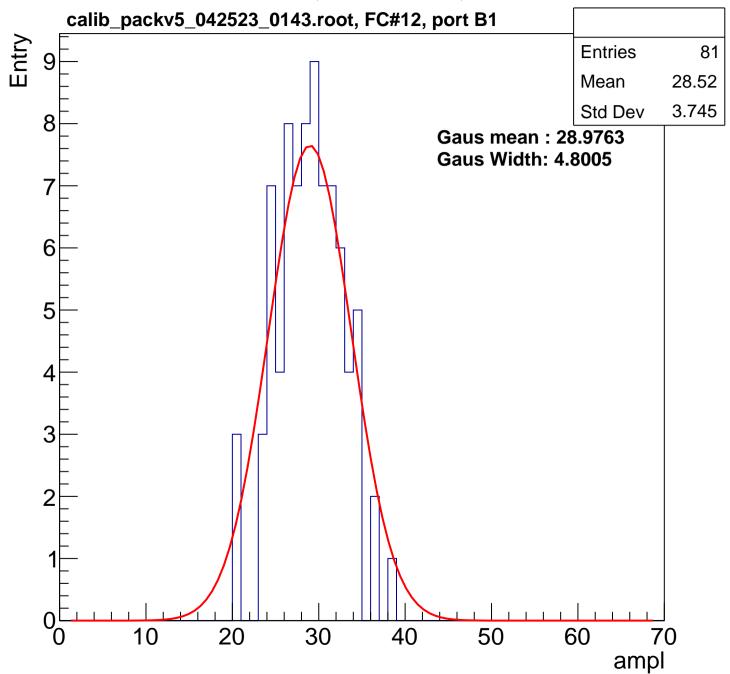


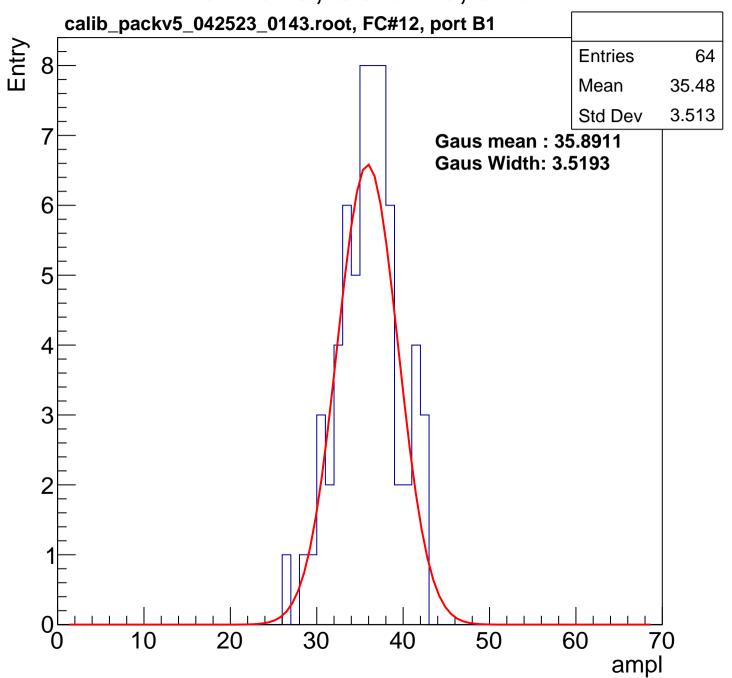


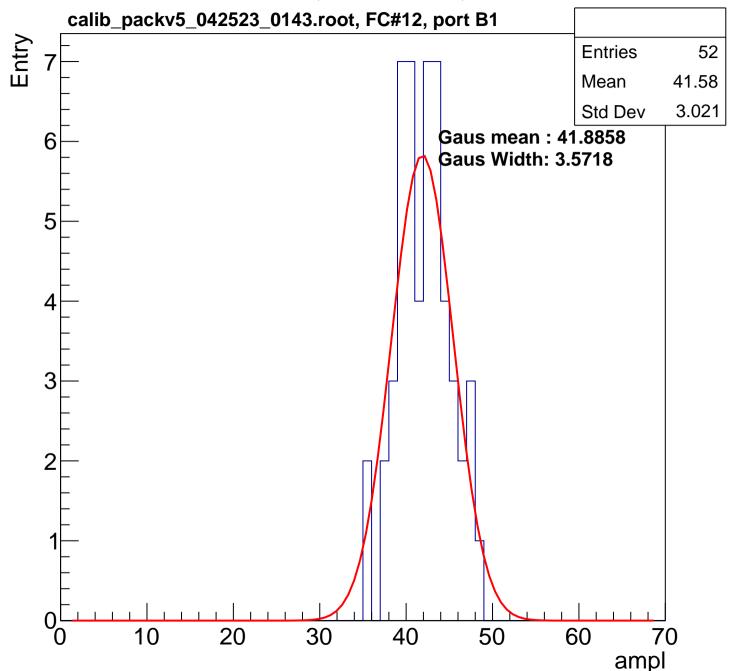


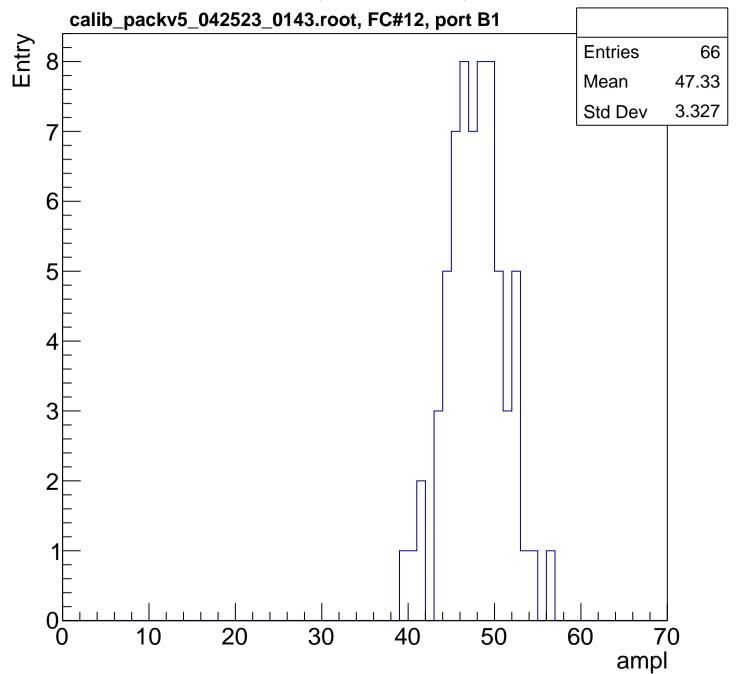


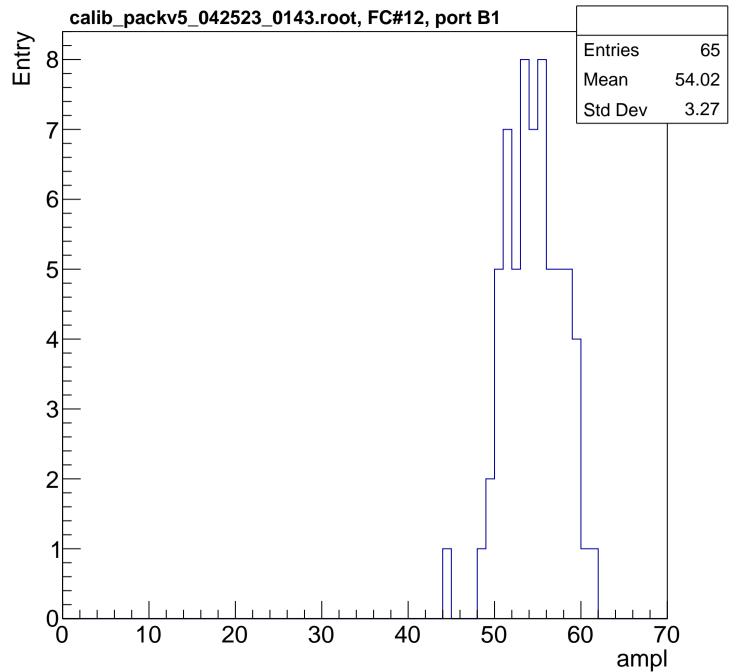


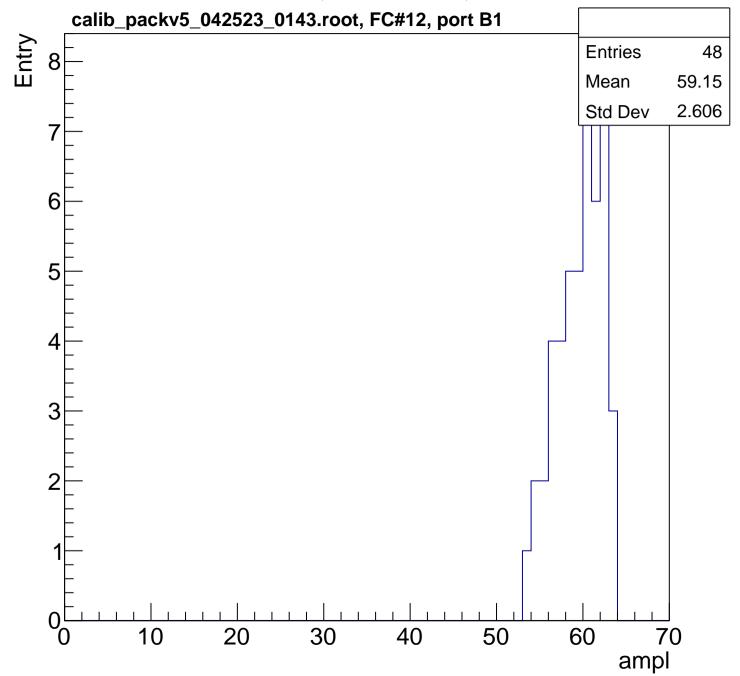


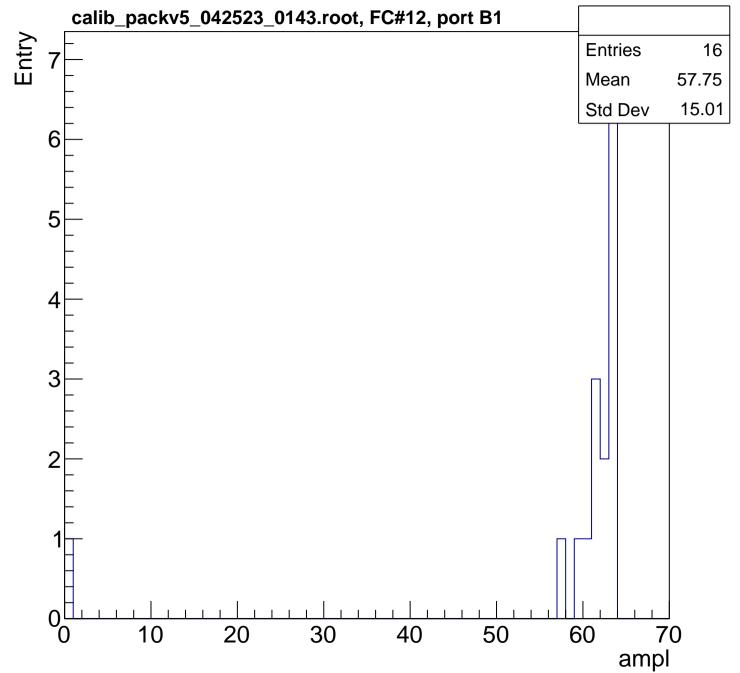




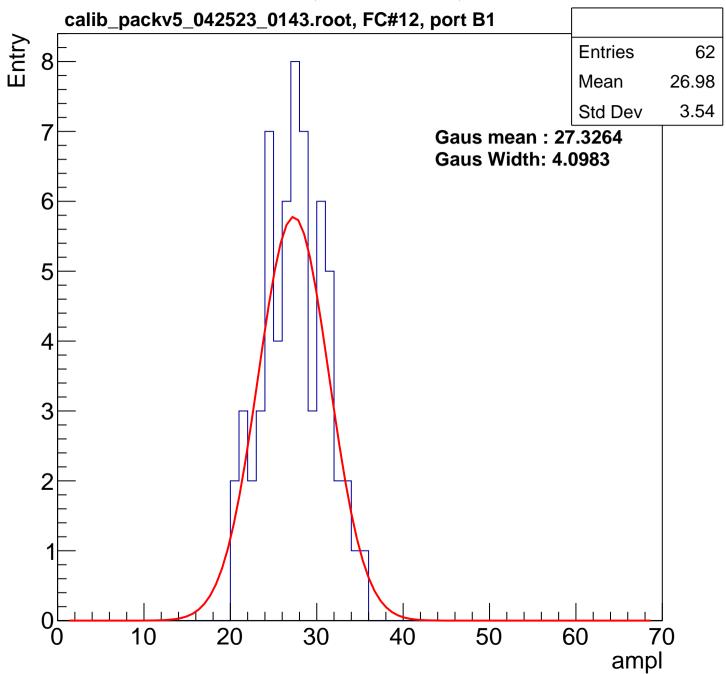


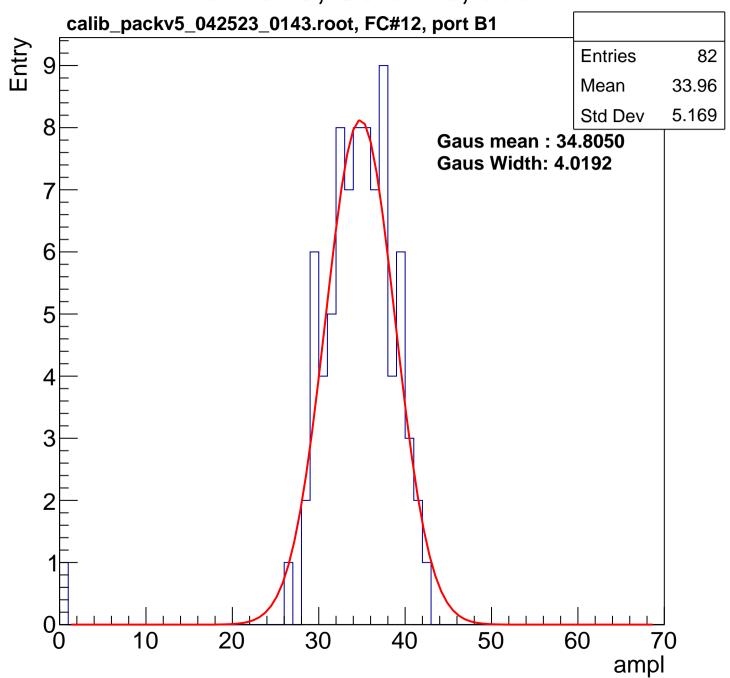


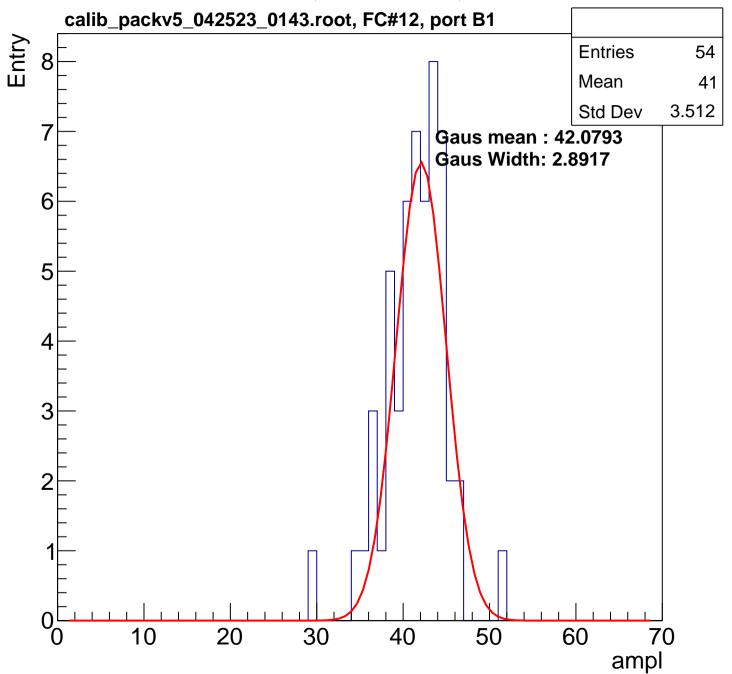


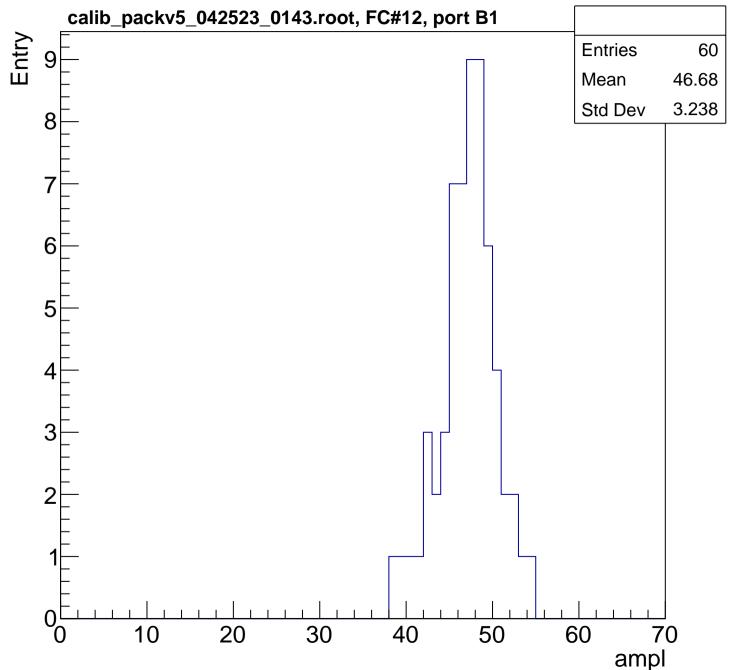


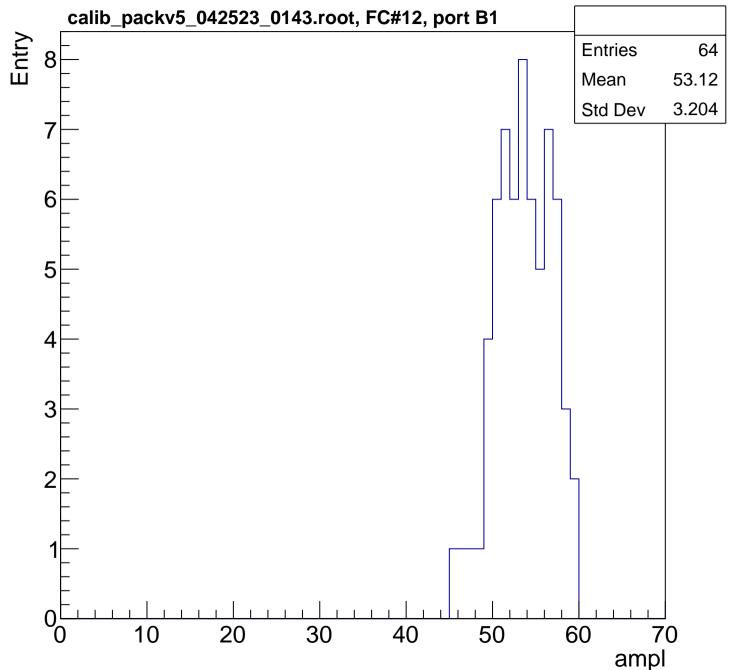
B0L102S, U3-ch75, adc7 calib_packv5_042523_0143.root, FC#12, port B1 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

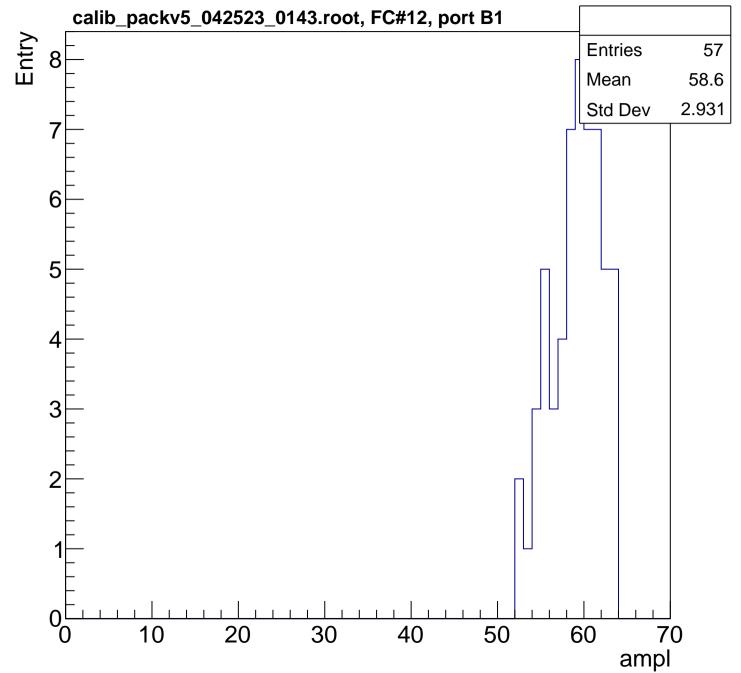


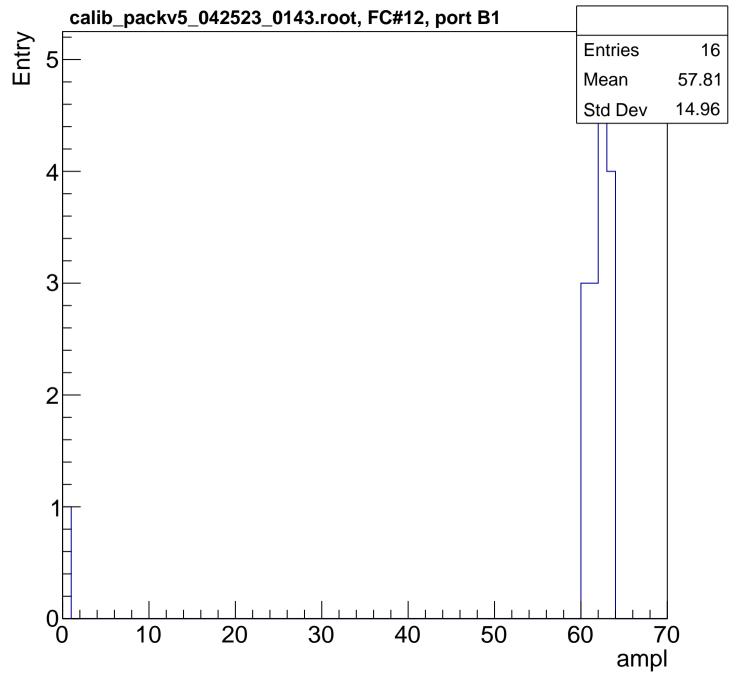




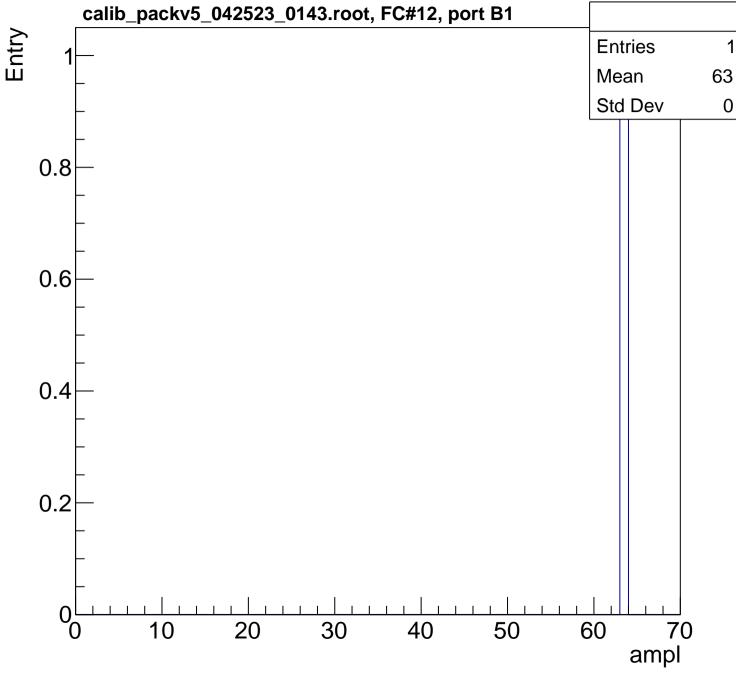


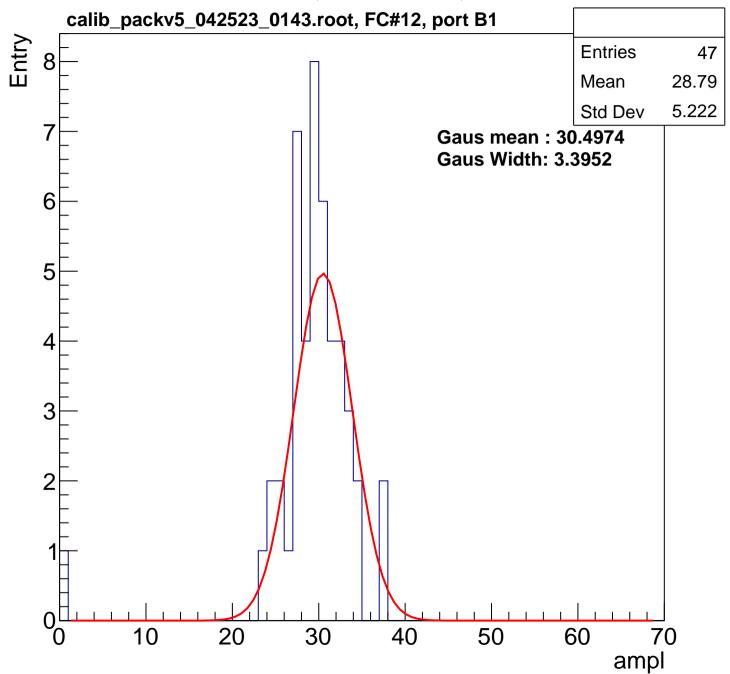


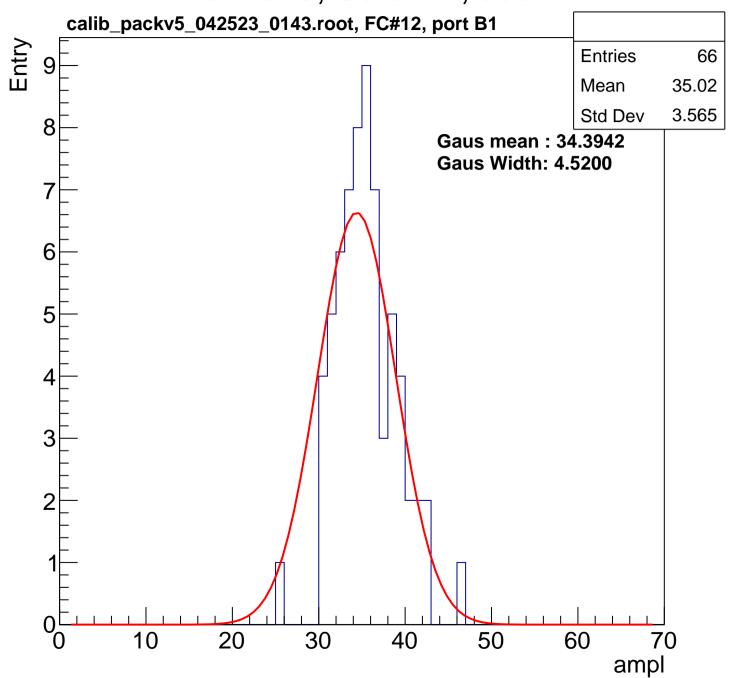


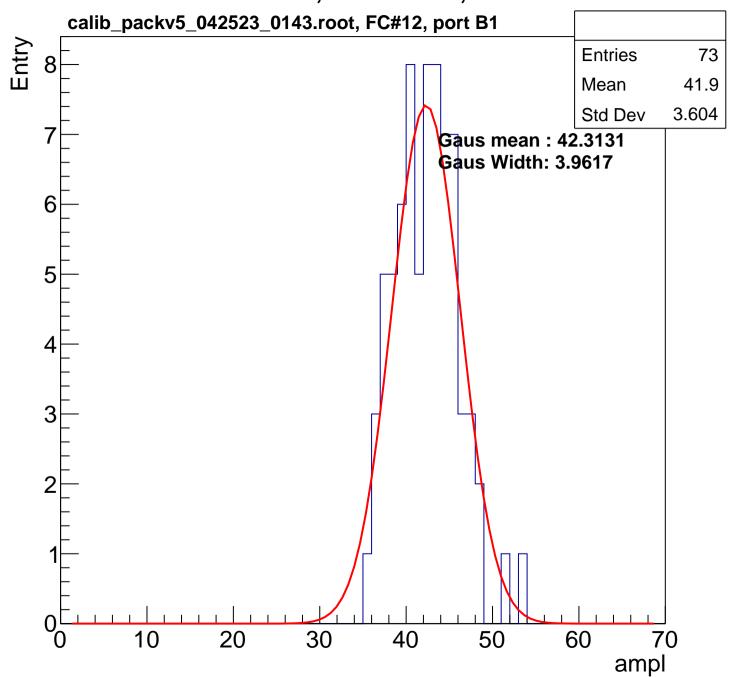


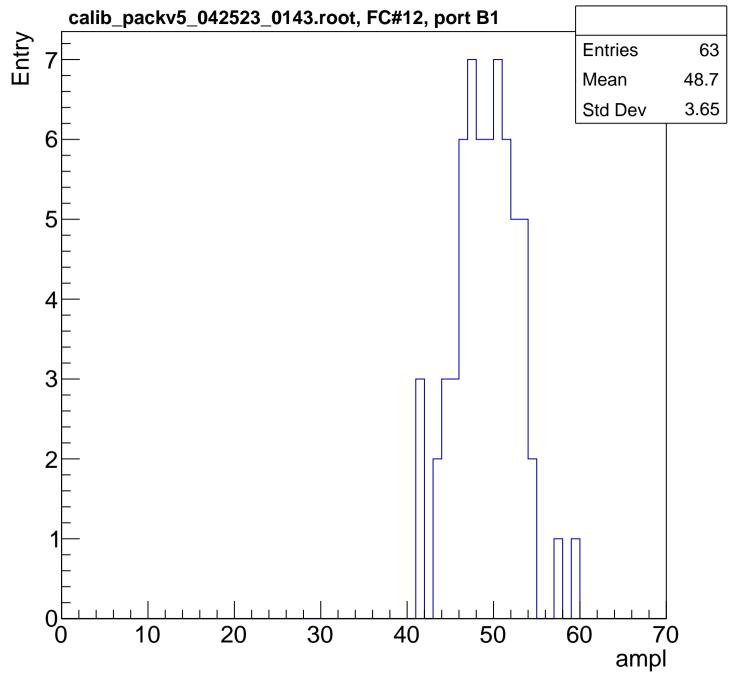
0

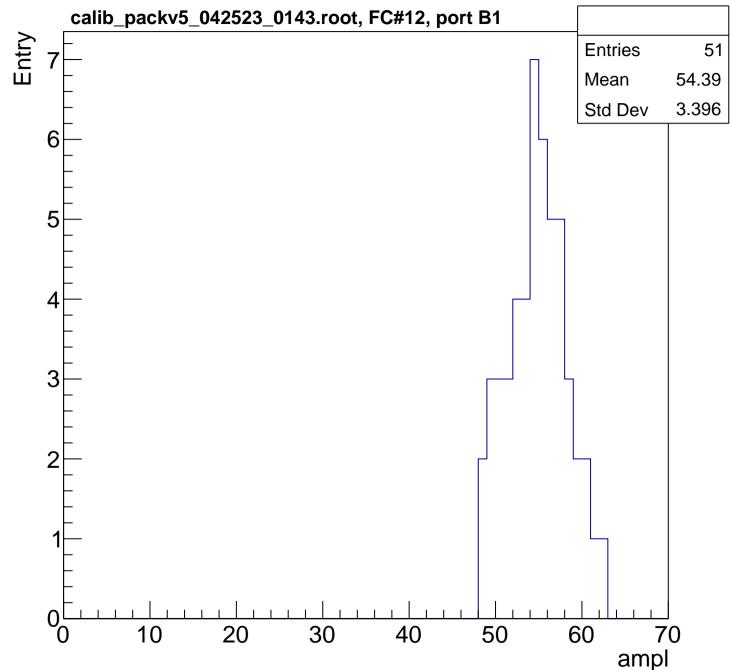


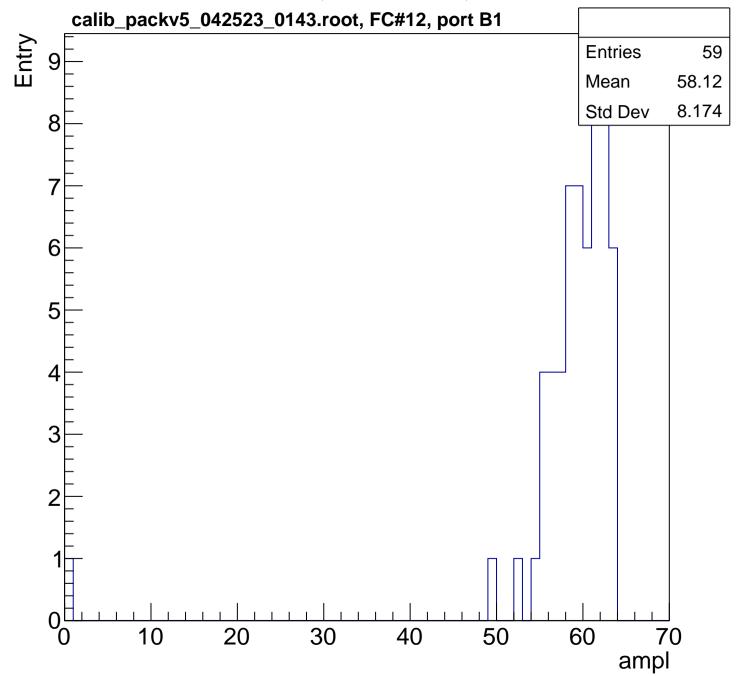


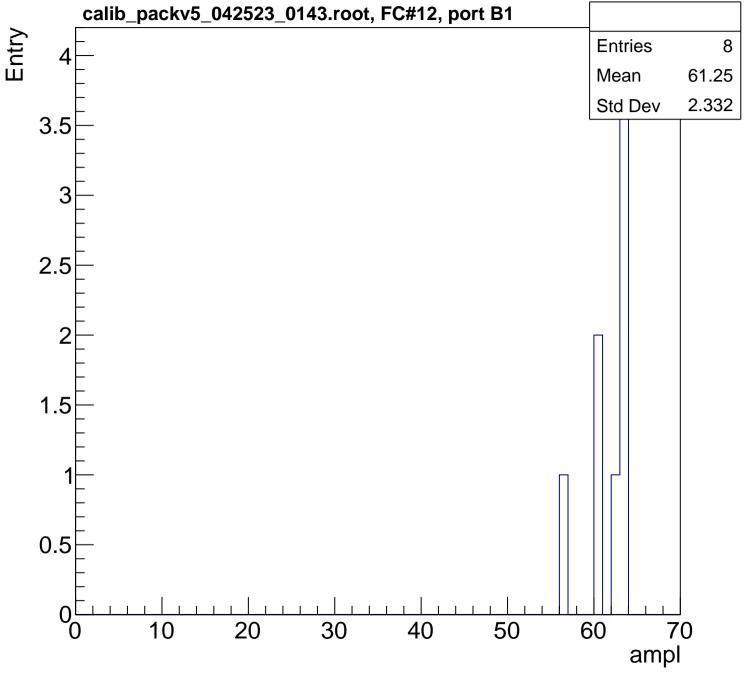




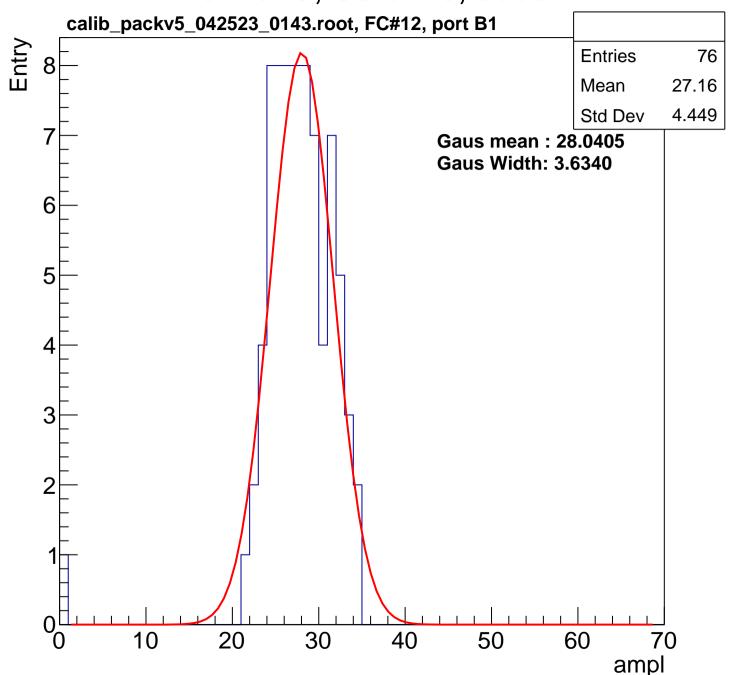


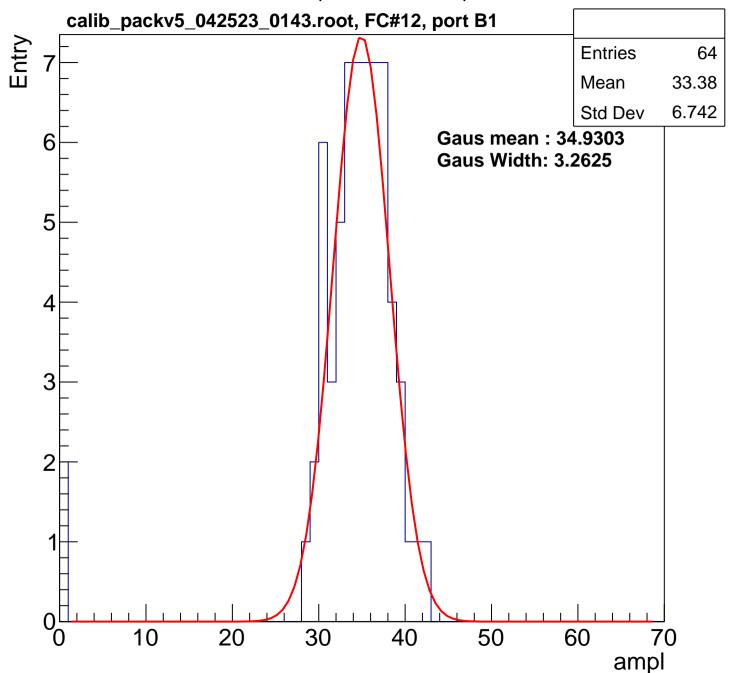


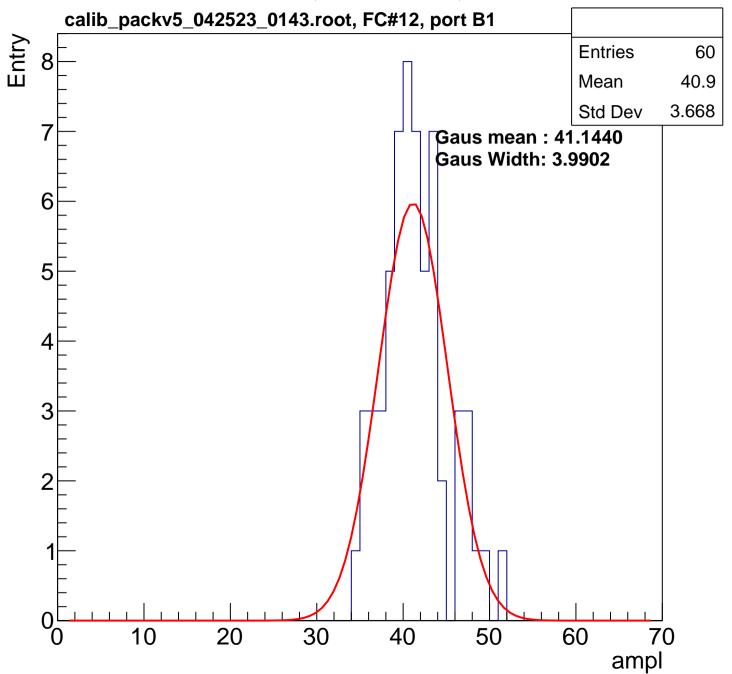


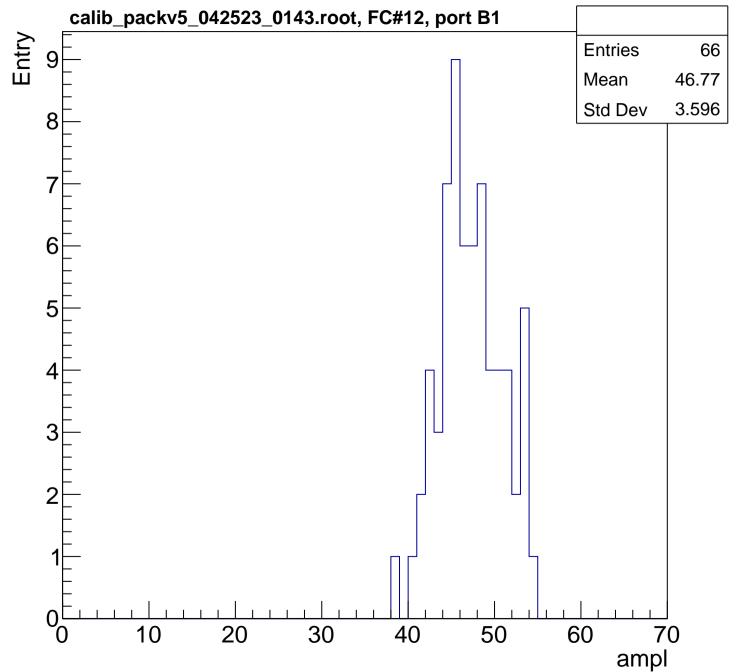


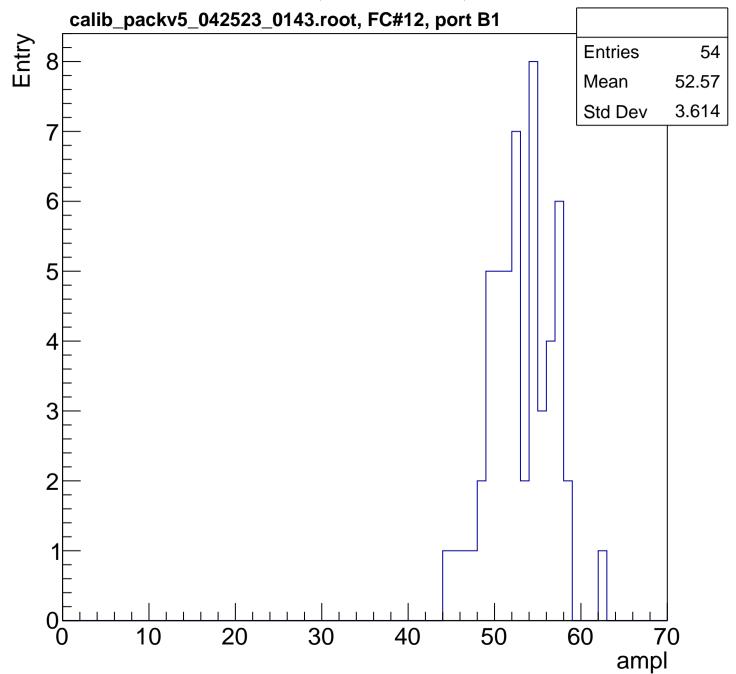
B0L102S, U3-ch77, adc7 calib_packv5_042523_0143.root, FC#12, port B1 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

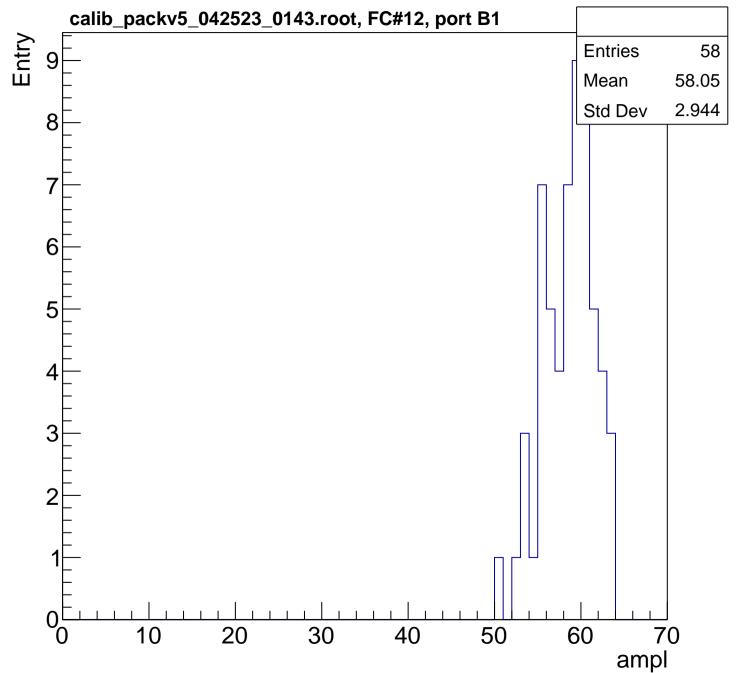


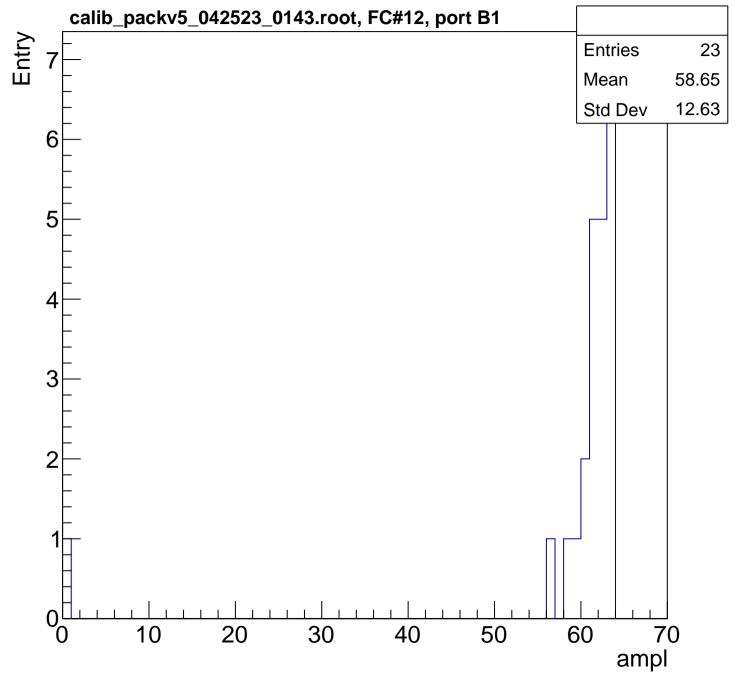




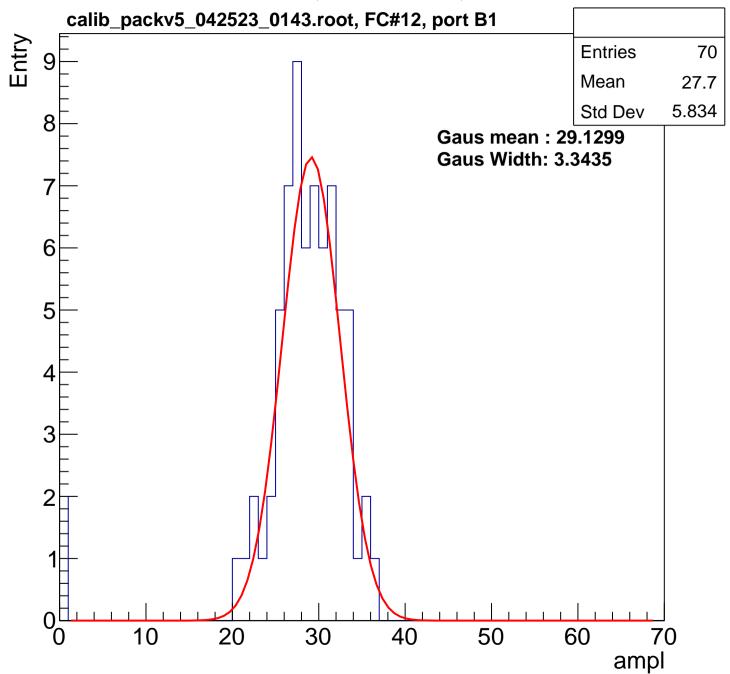


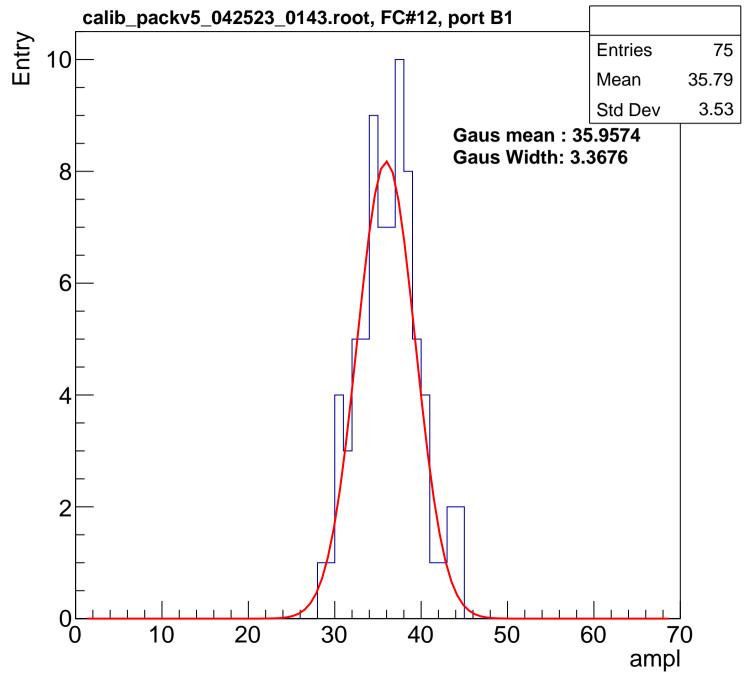


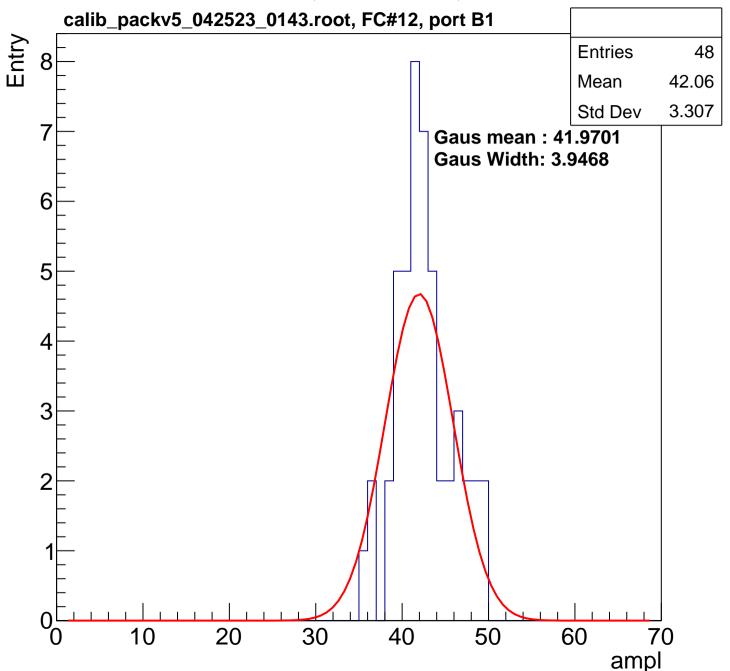


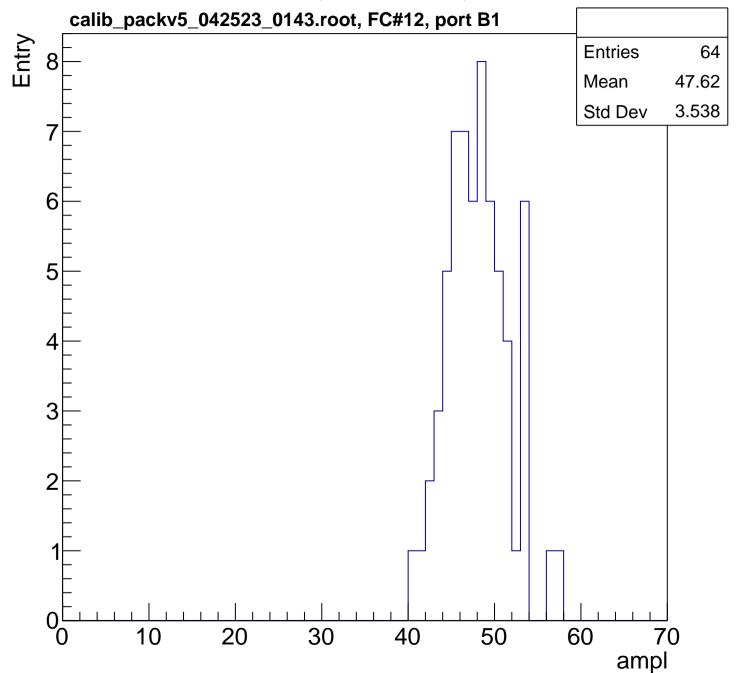


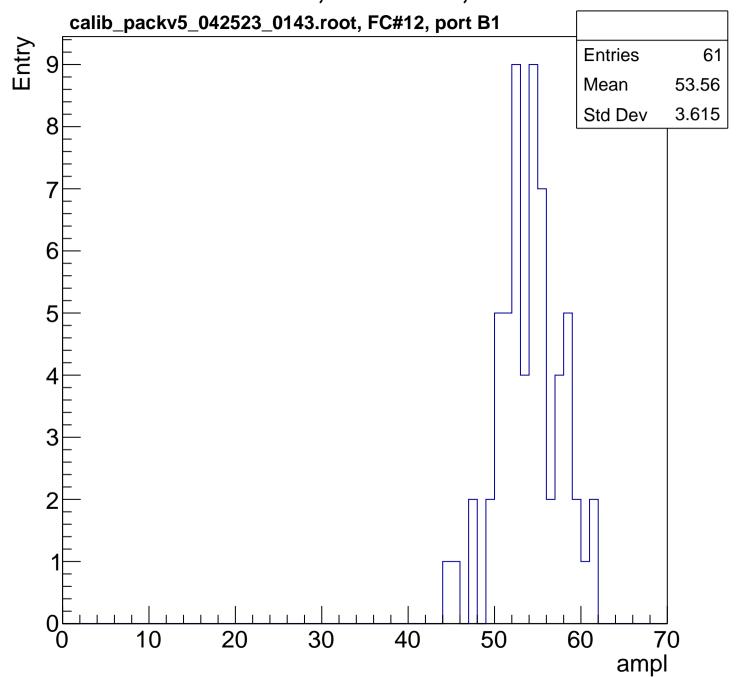
B0L102S, U3-ch78, adc7 calib_packv5_042523_0143.root, FC#12, port B1 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

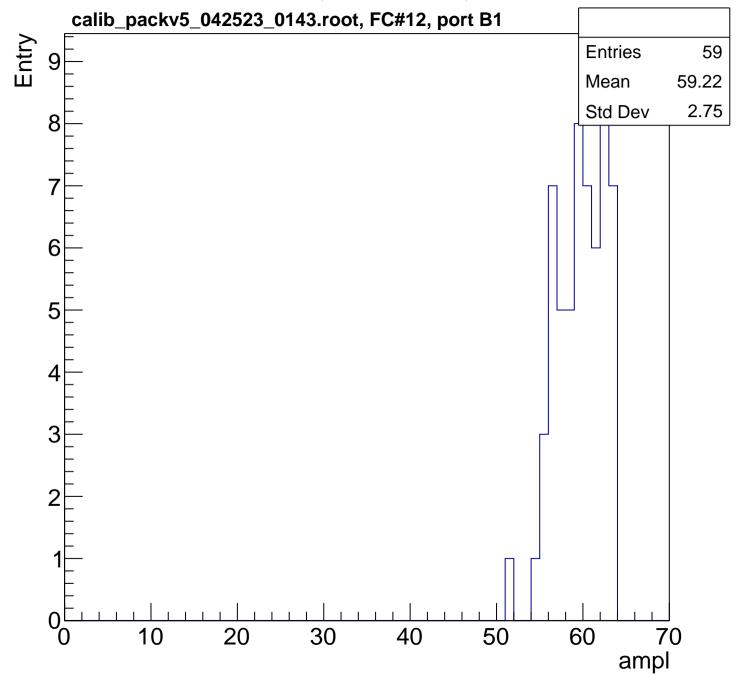


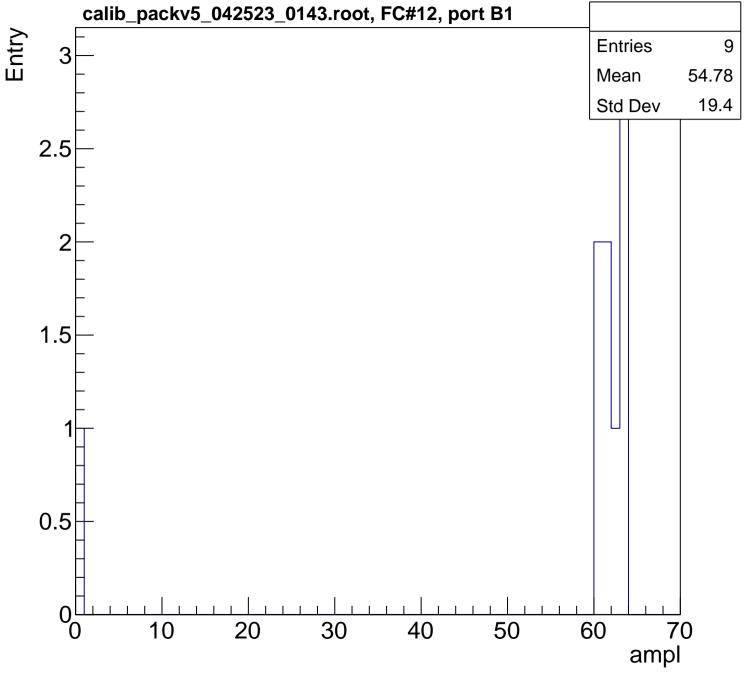






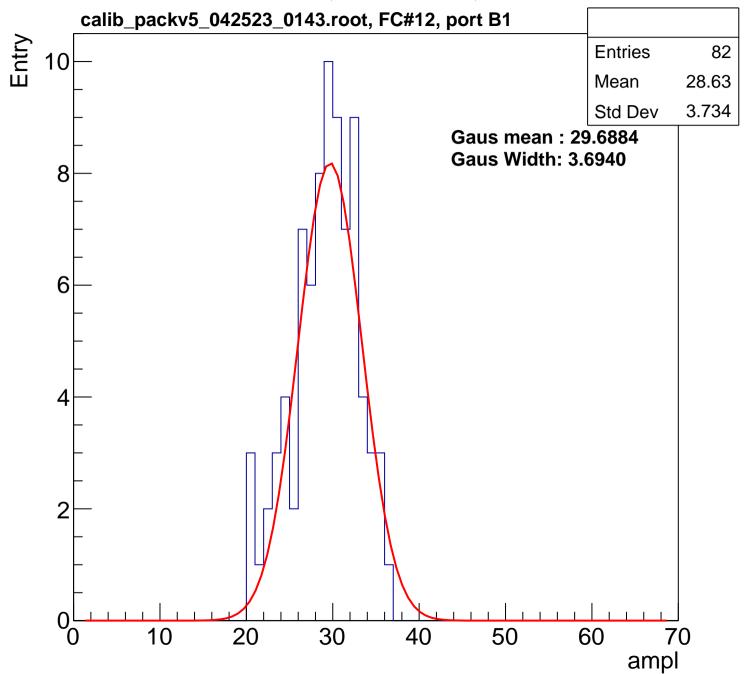


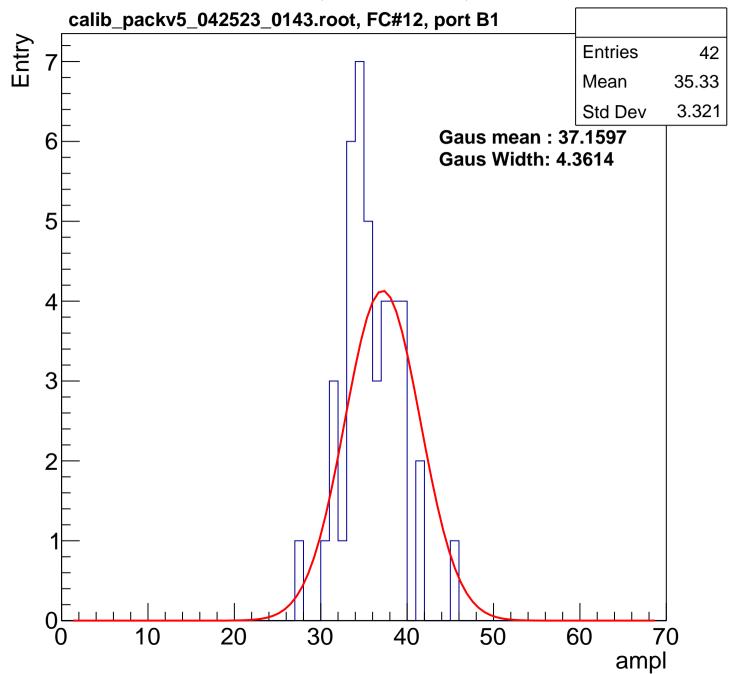


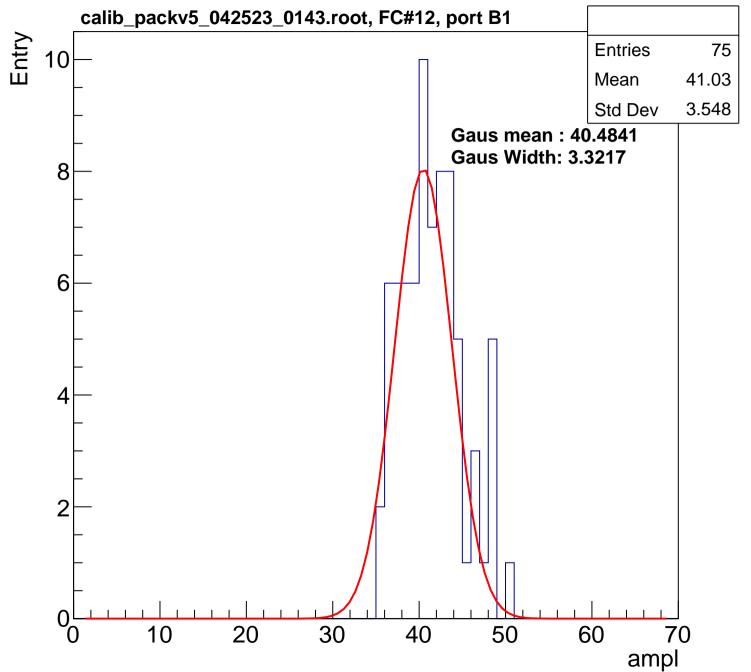


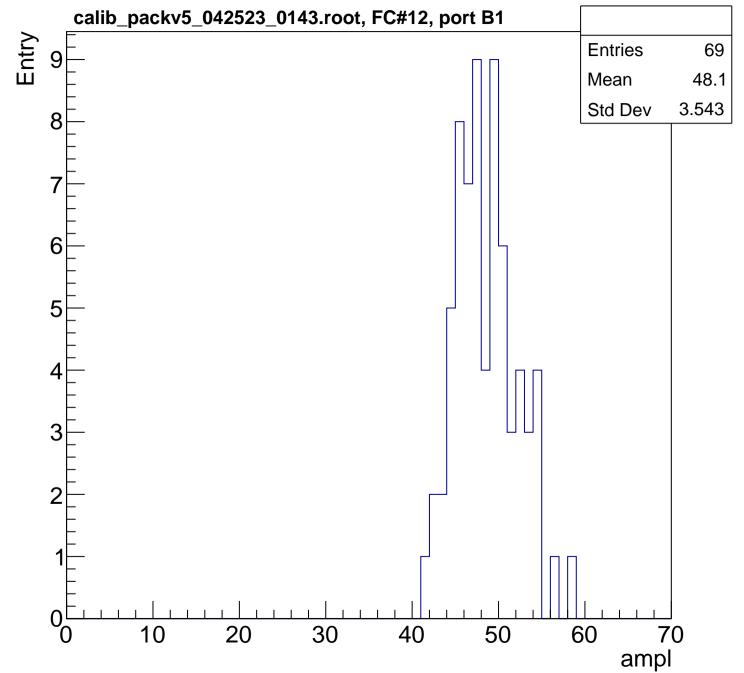
B0L102S, U3-ch79, adc7 calib_packv5_042523_0143.root, FC#12, port B1 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70

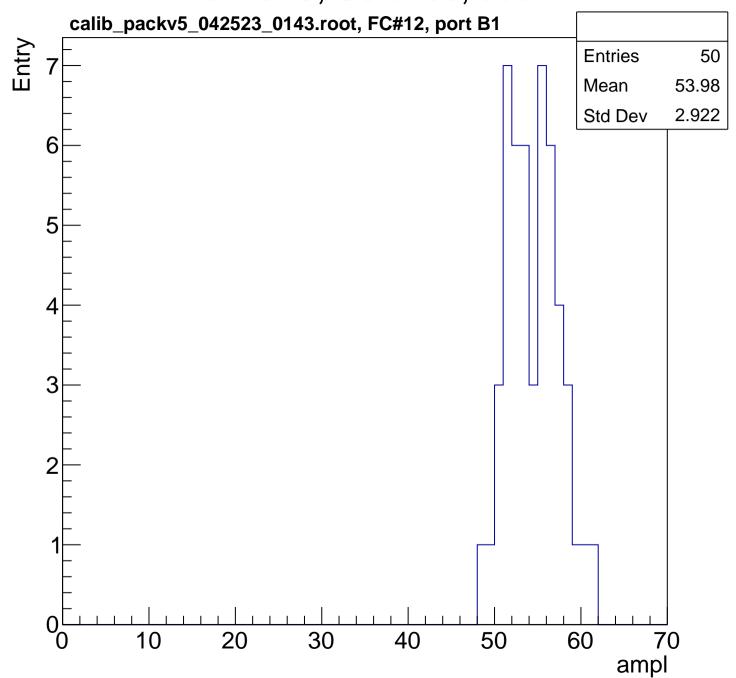
ampl

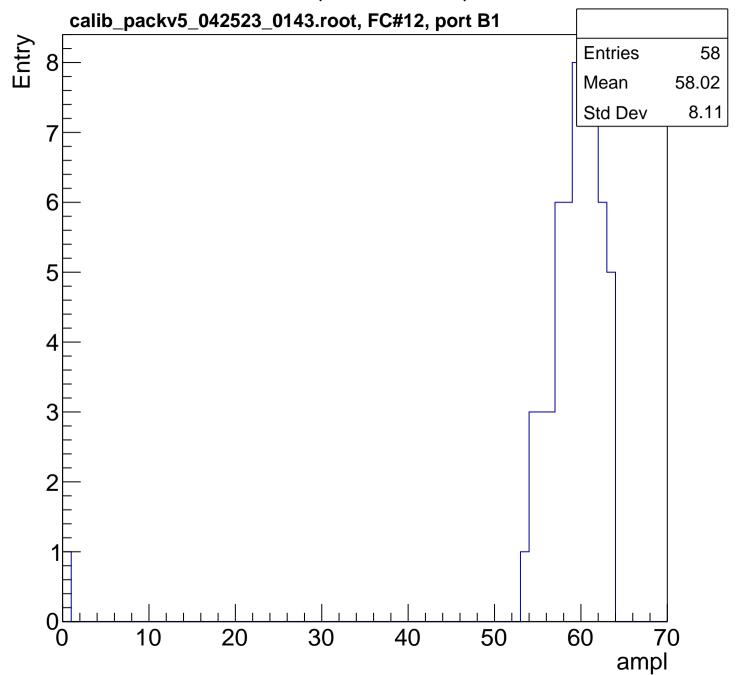


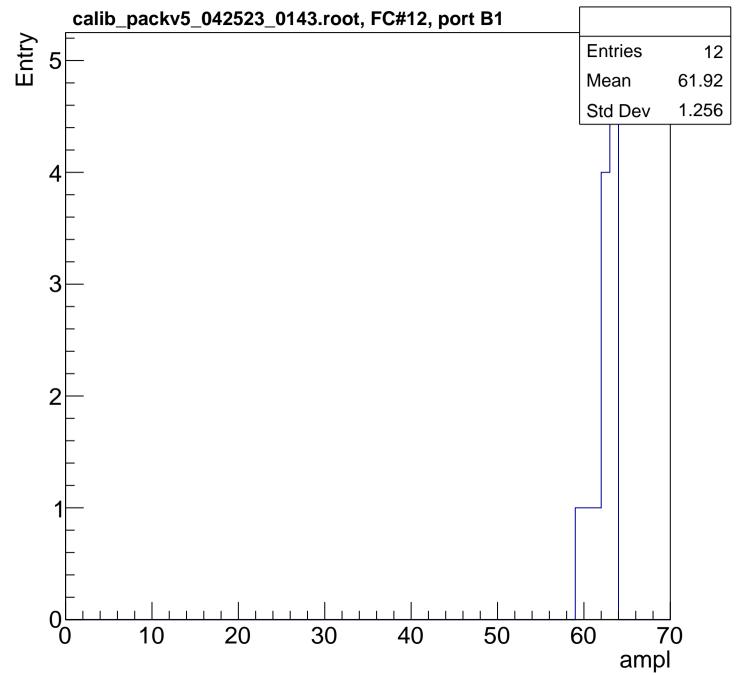


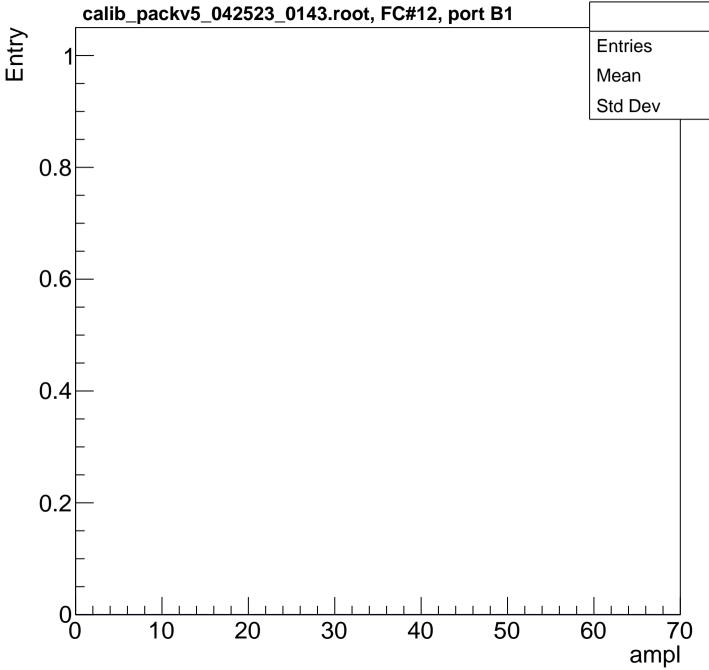


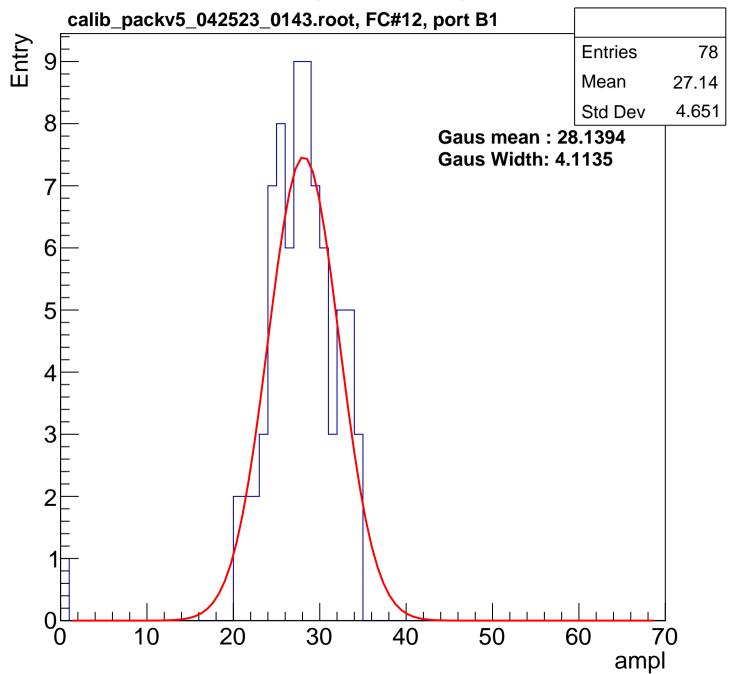


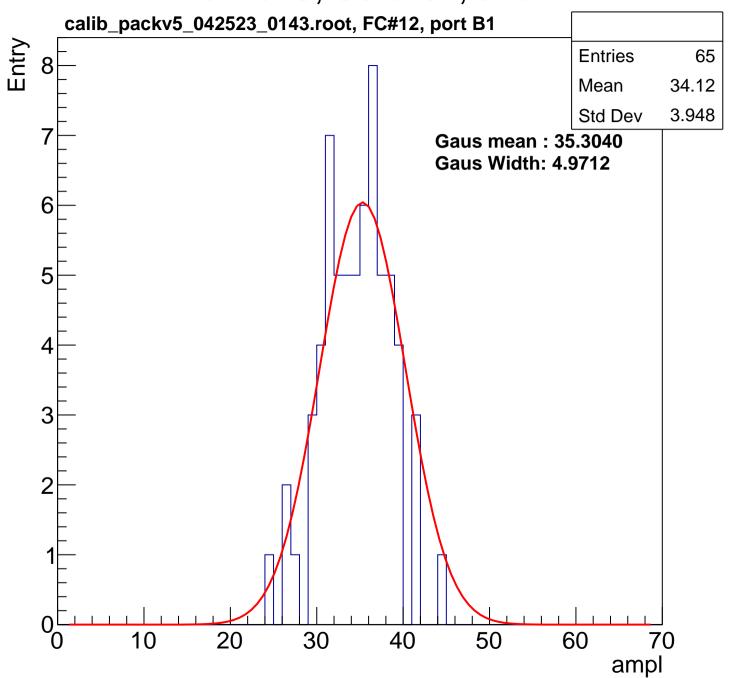


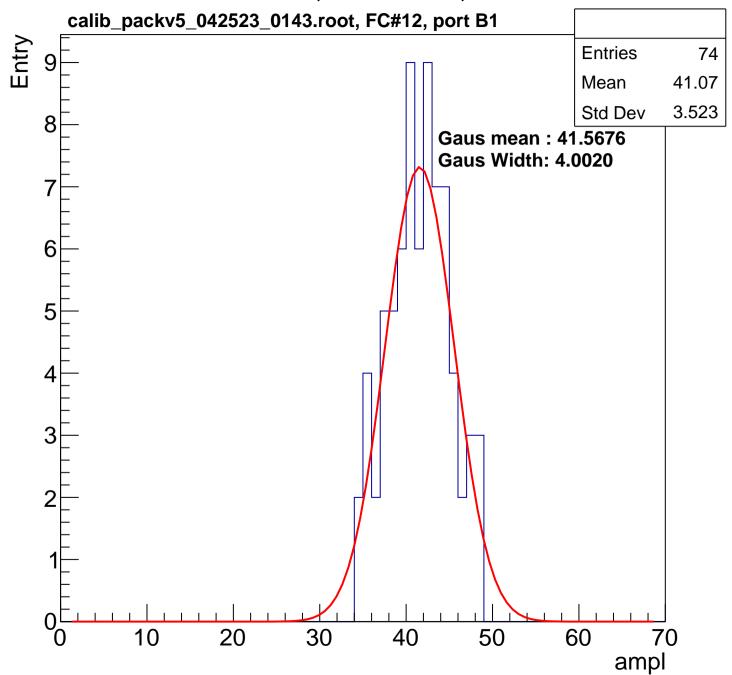


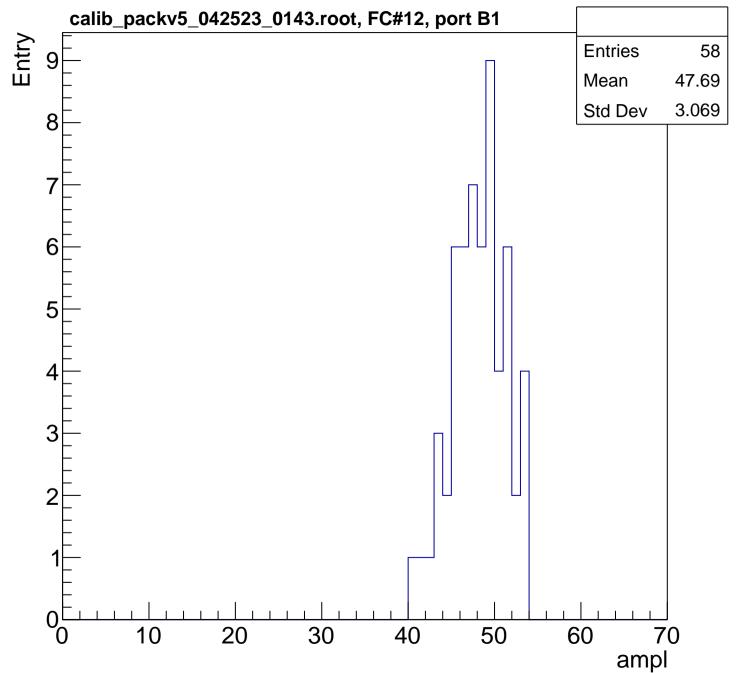


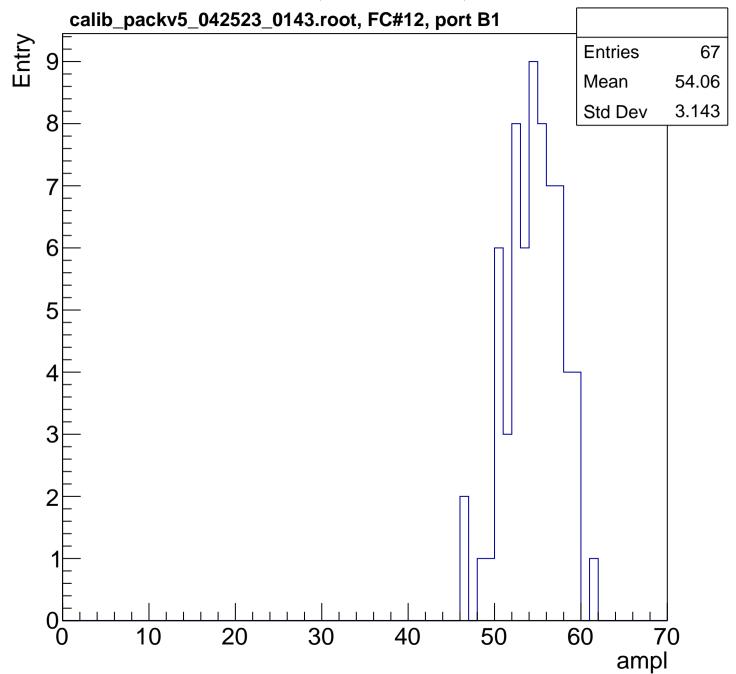


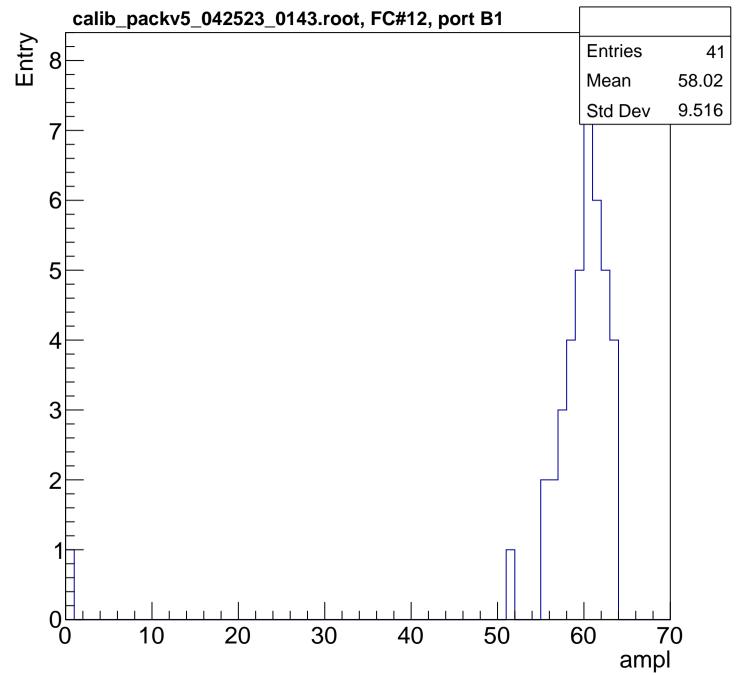


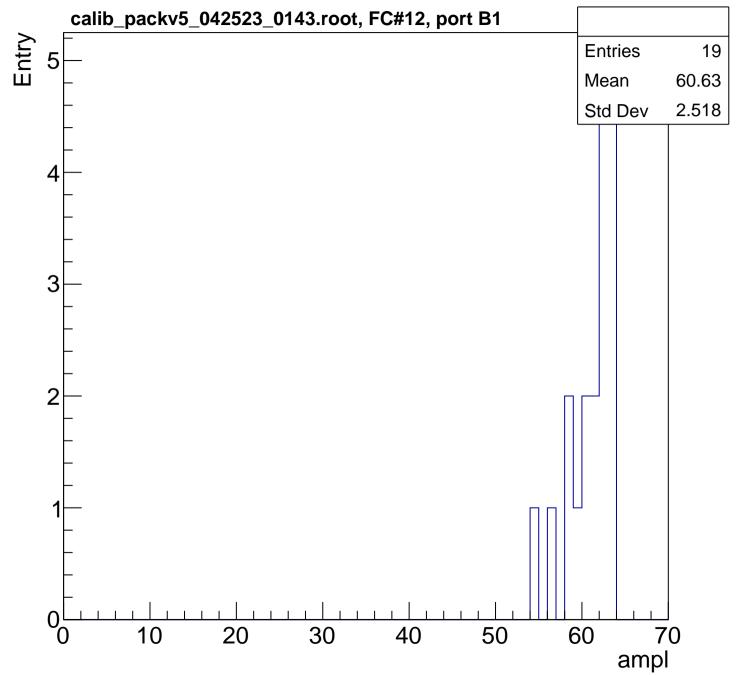


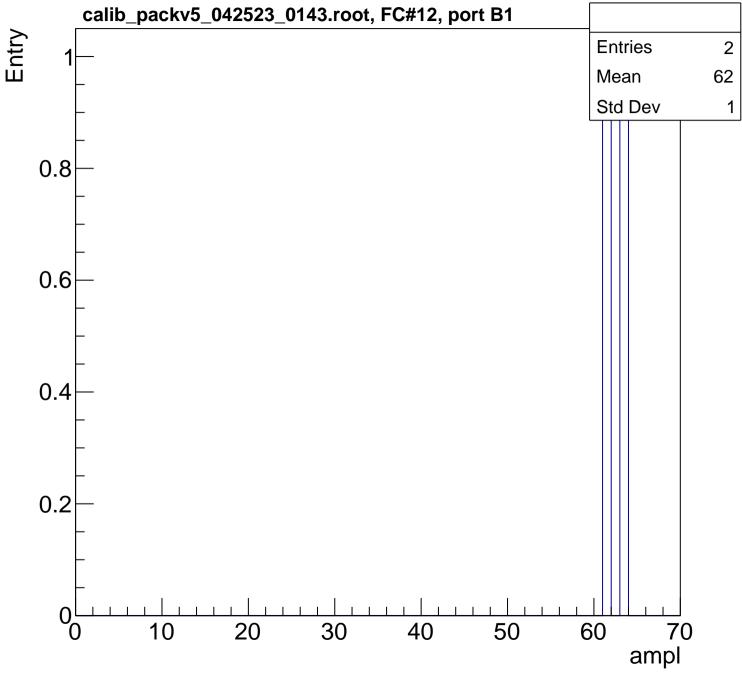


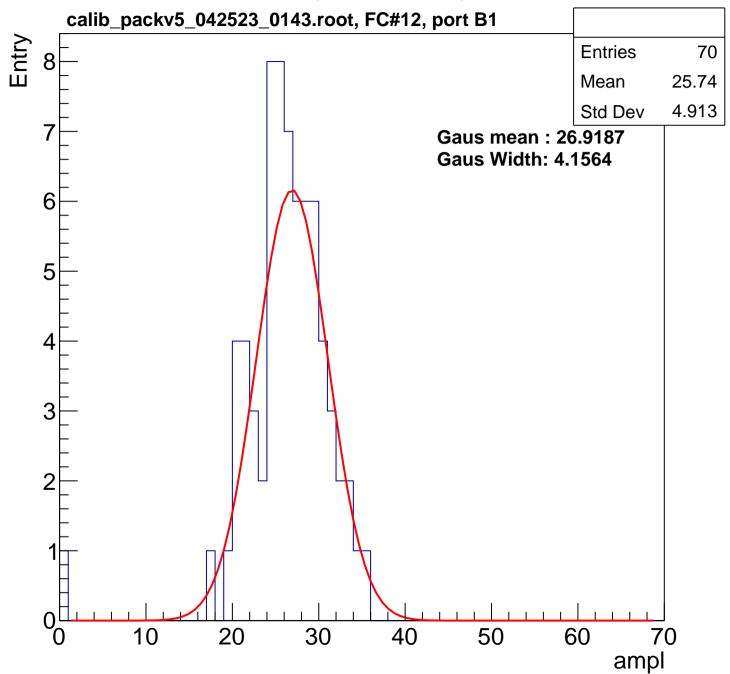


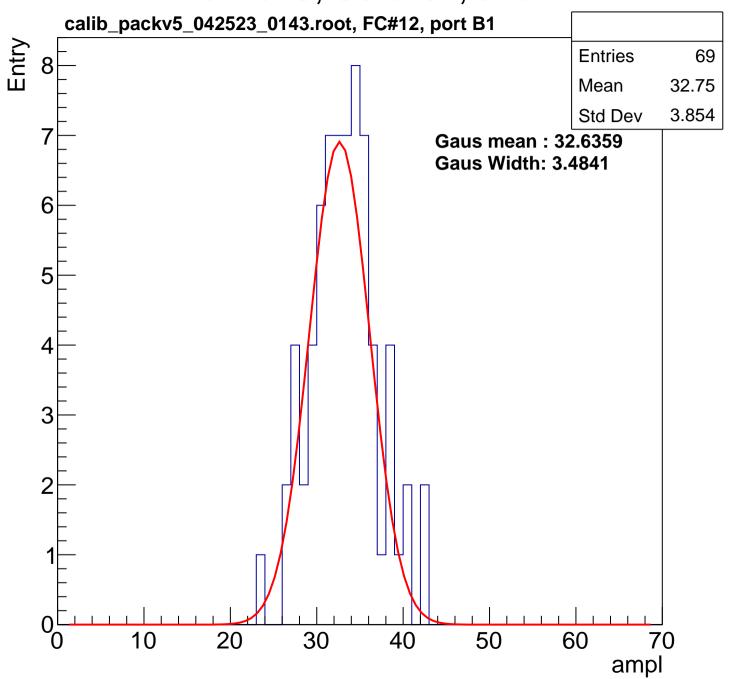


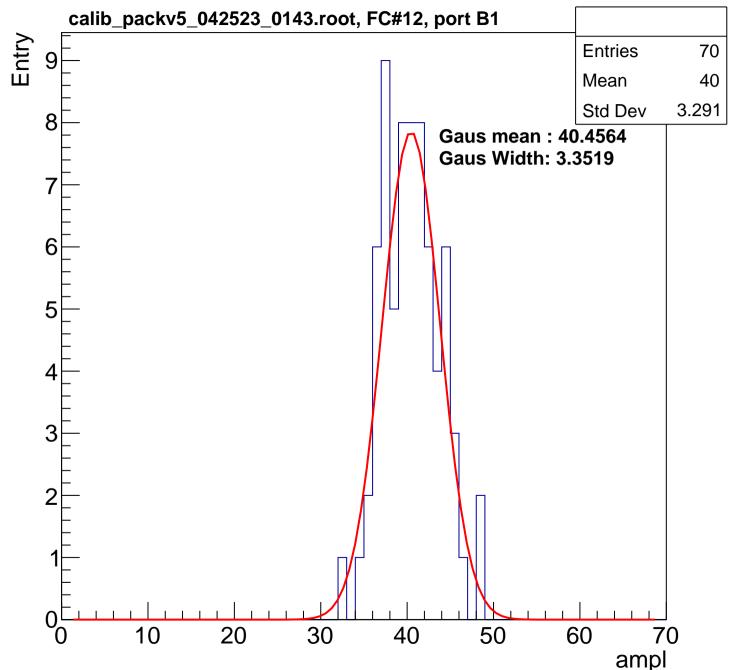


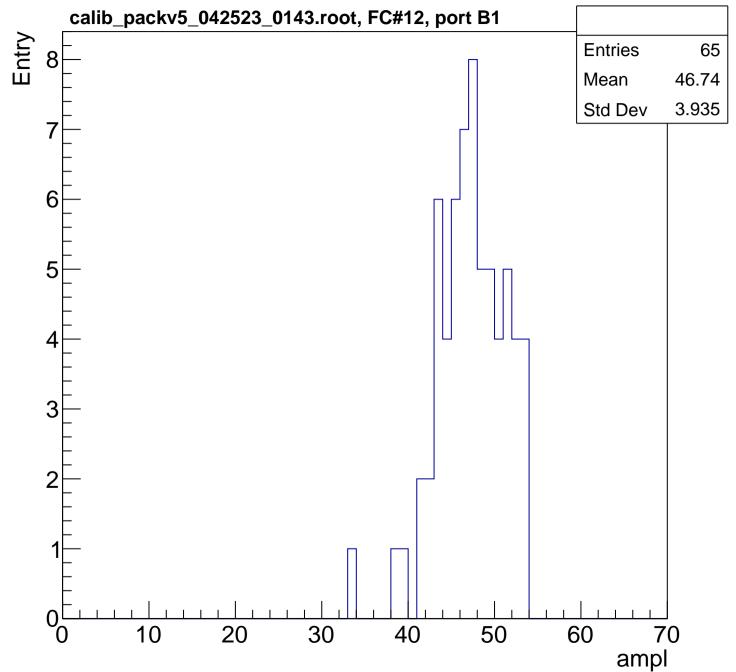


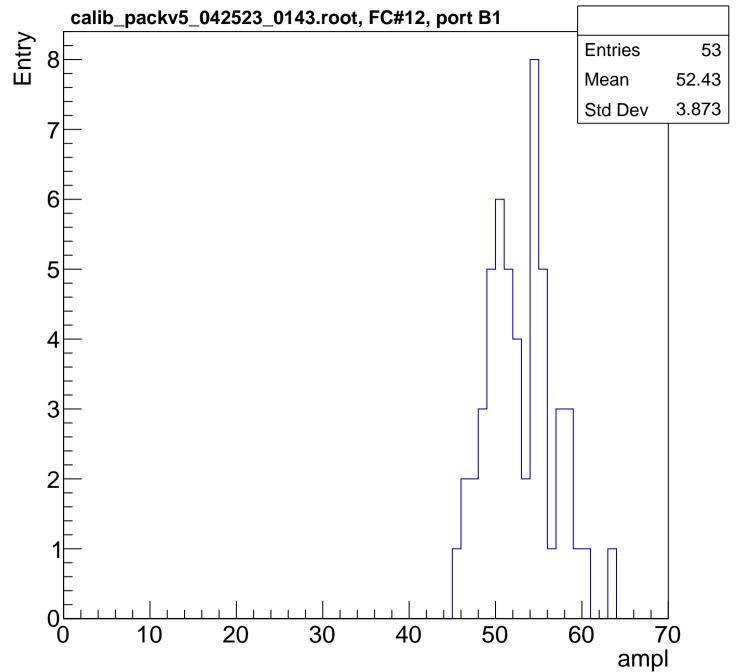


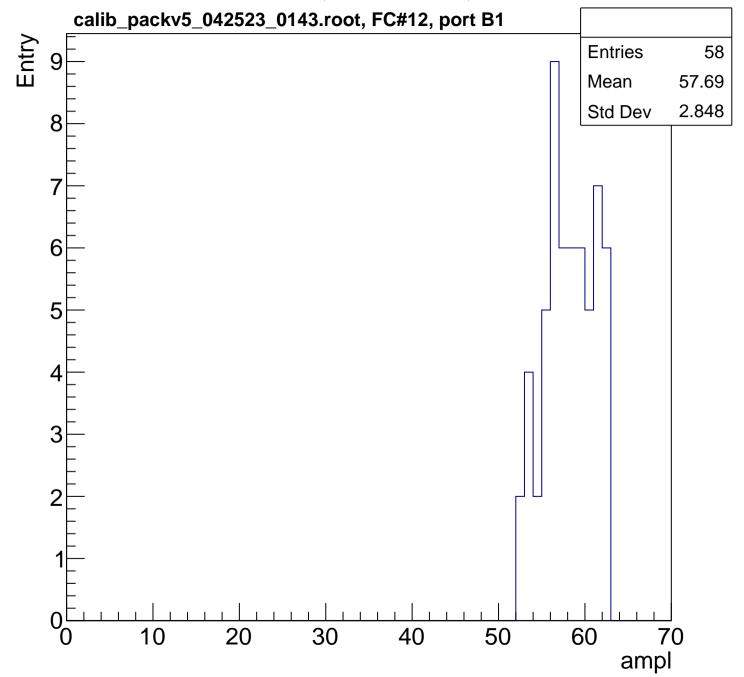


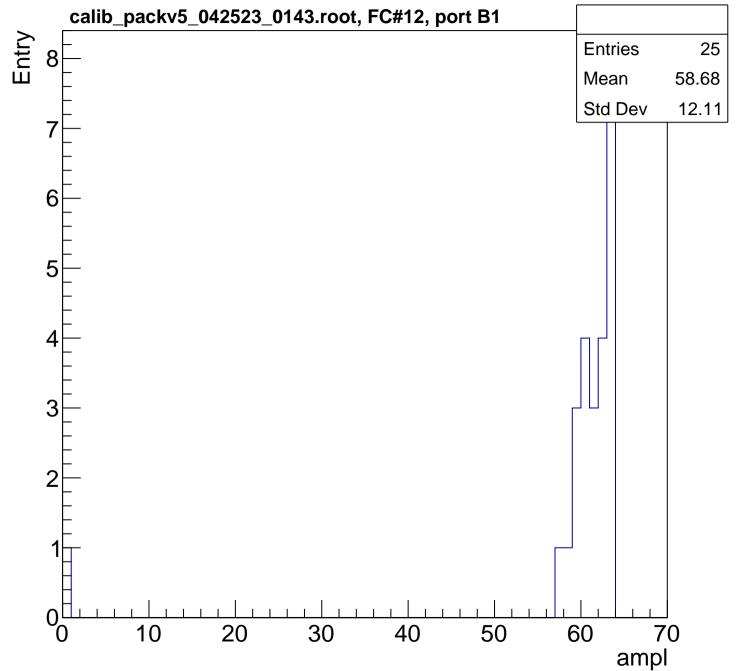




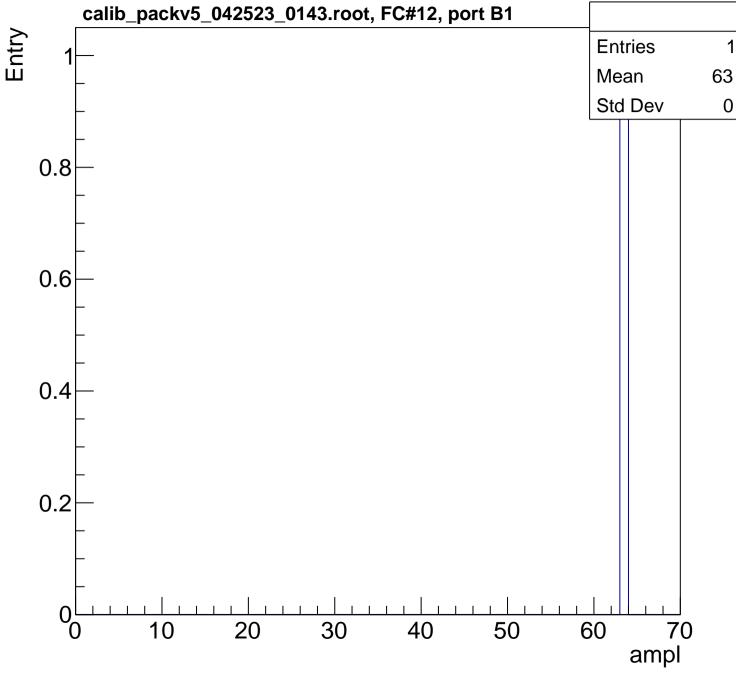


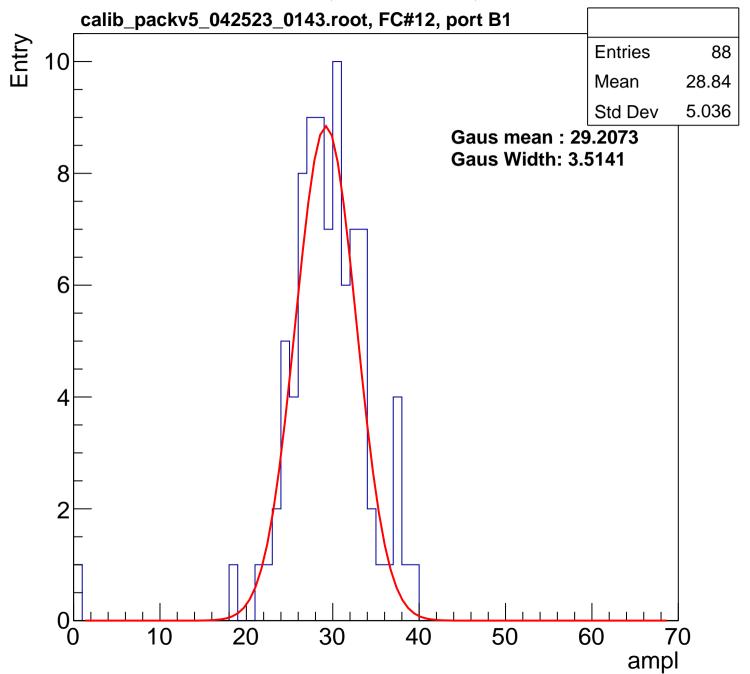


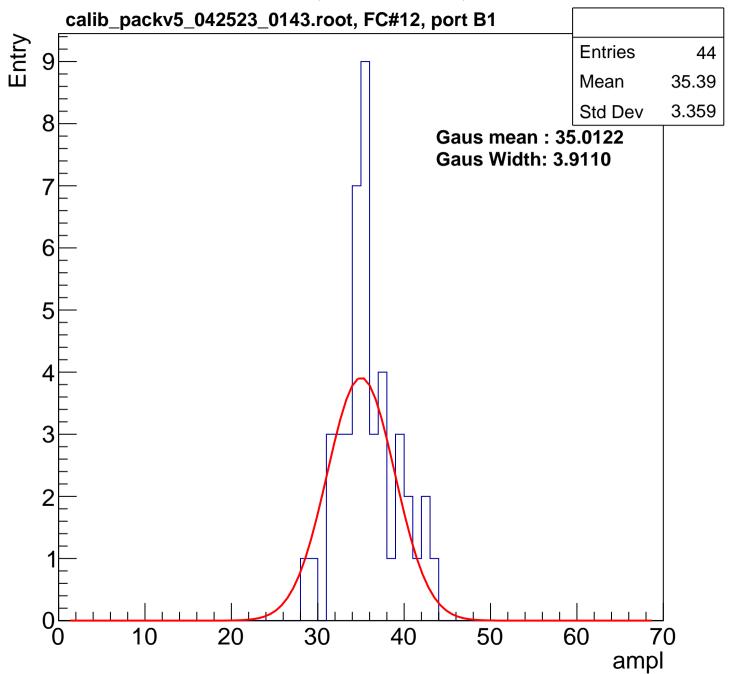


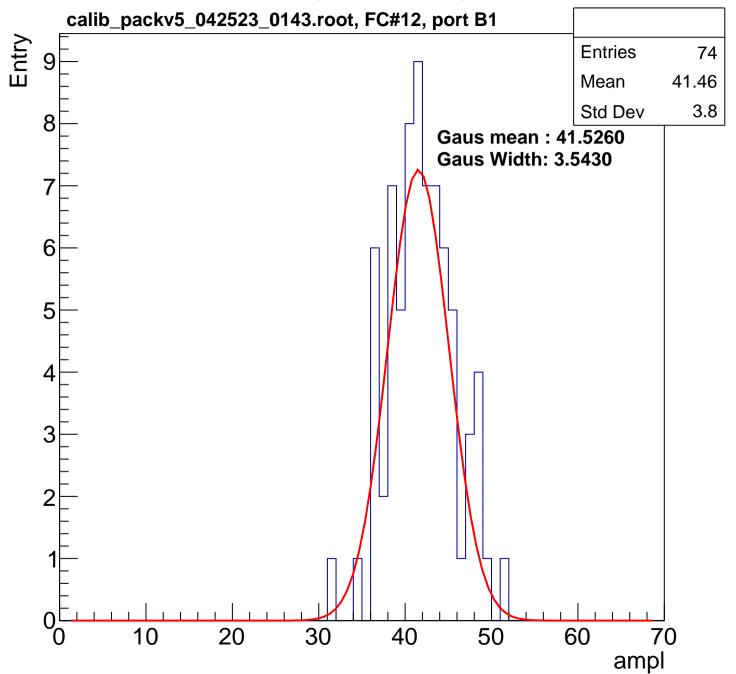


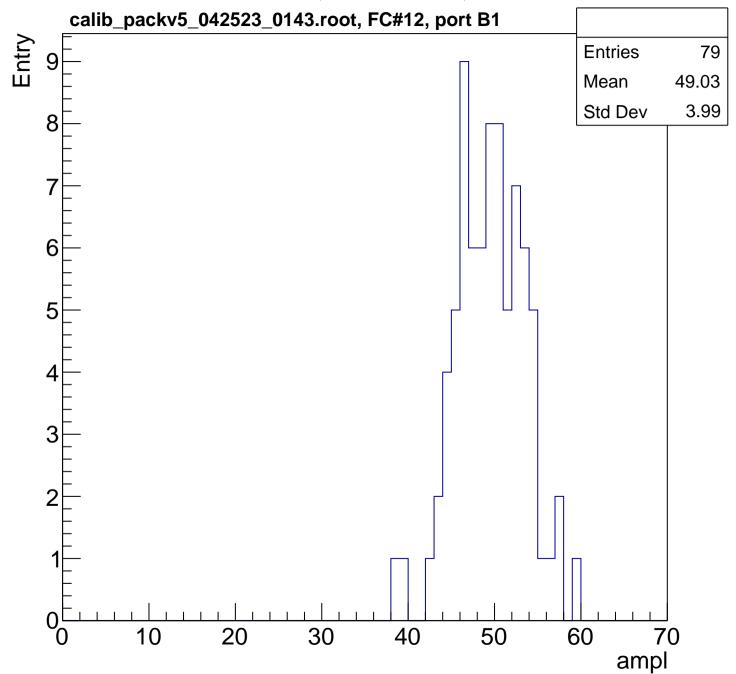
0

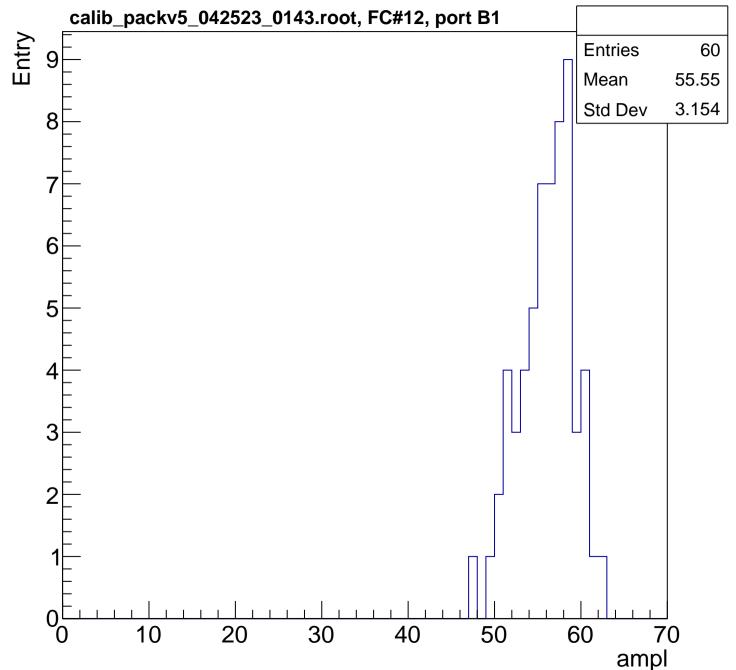


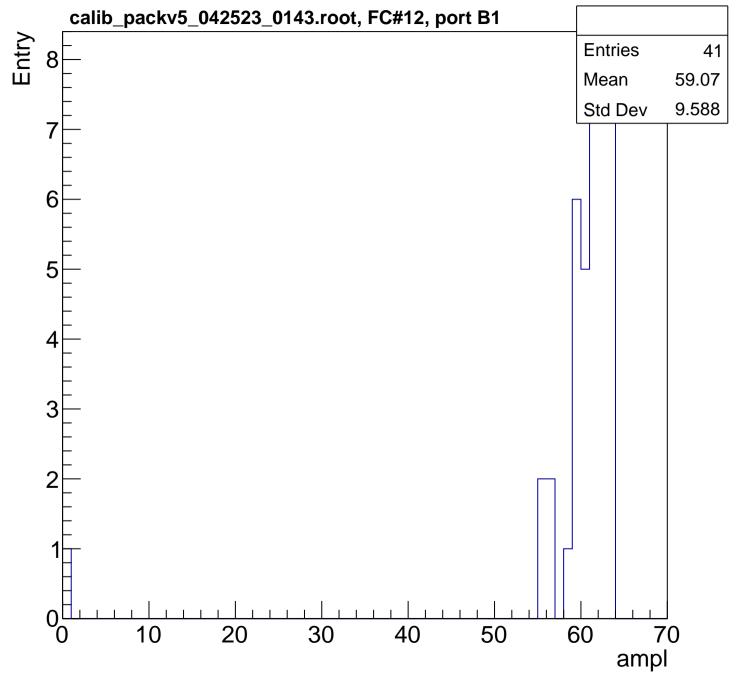


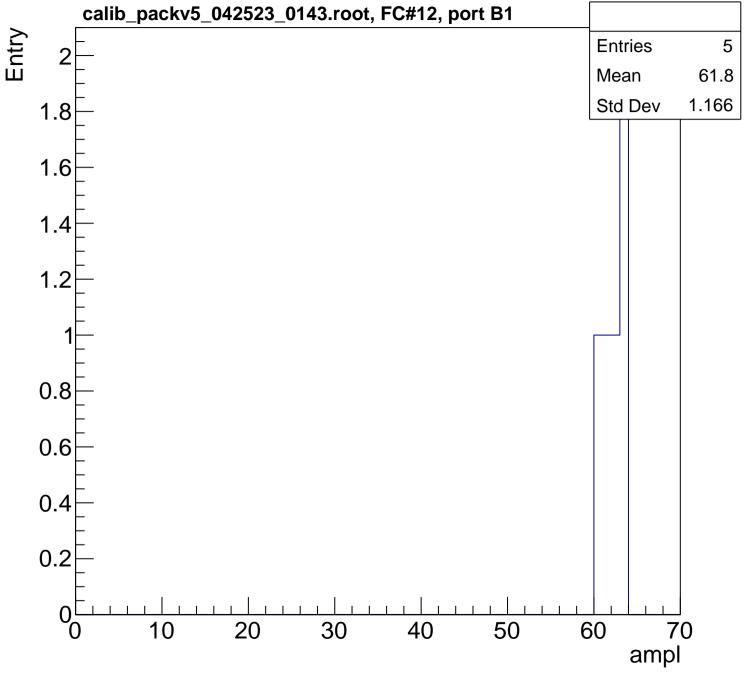


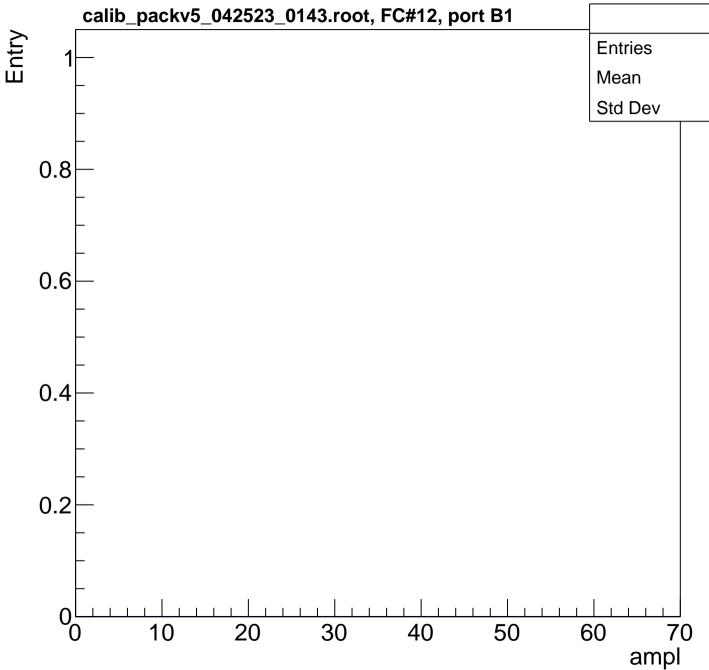


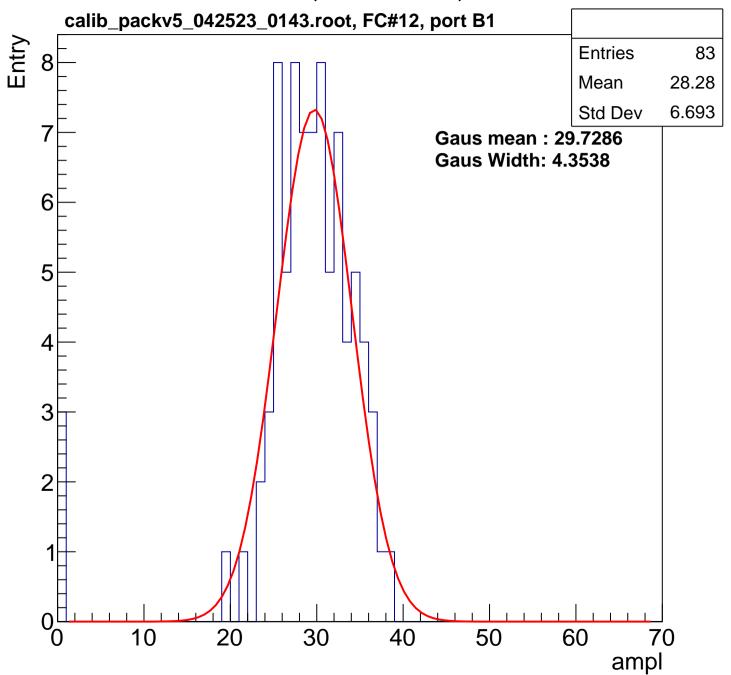


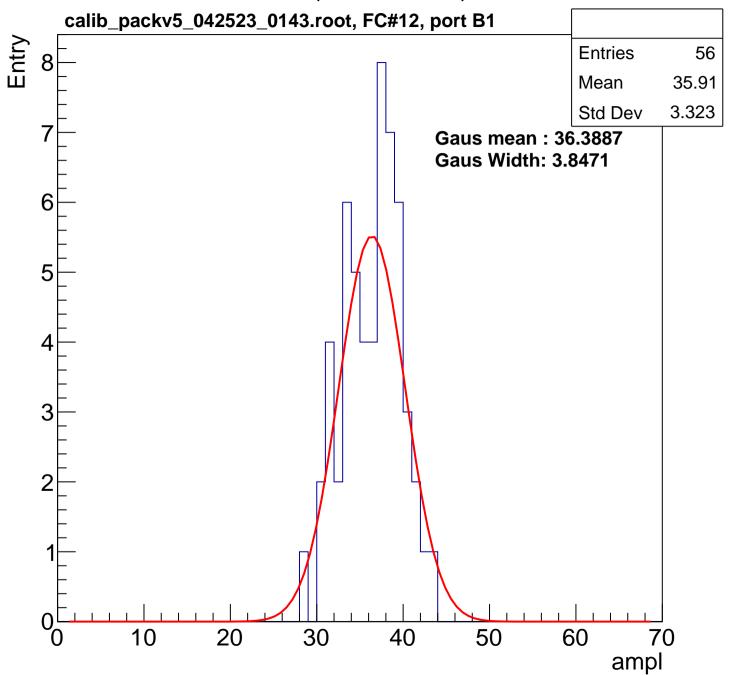


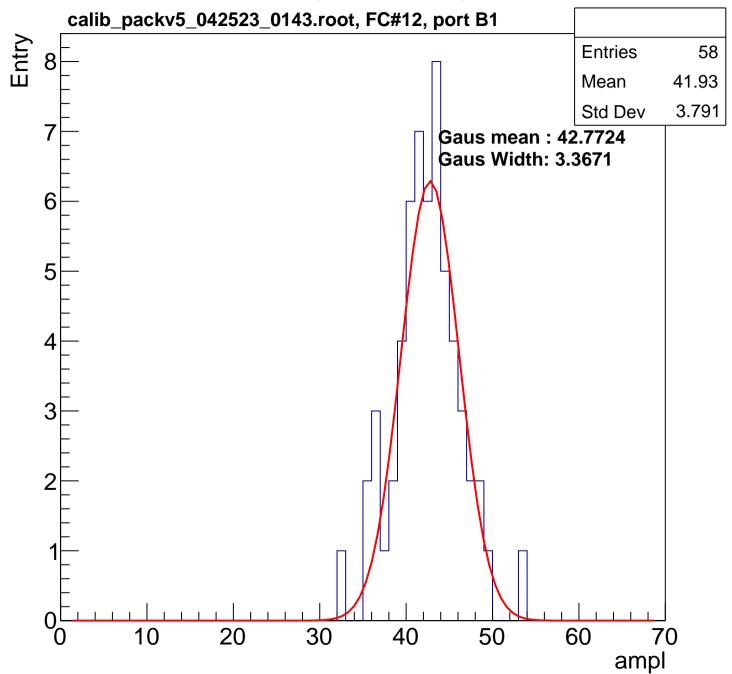


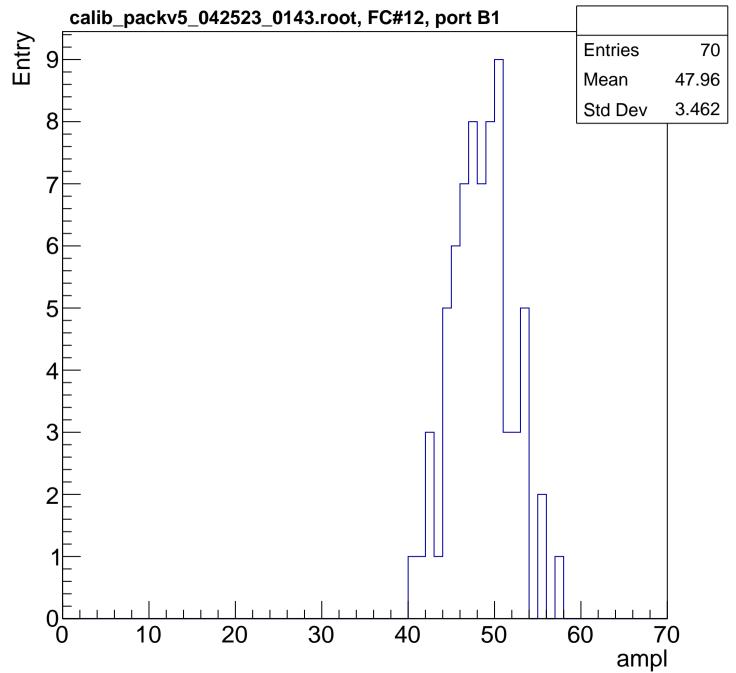


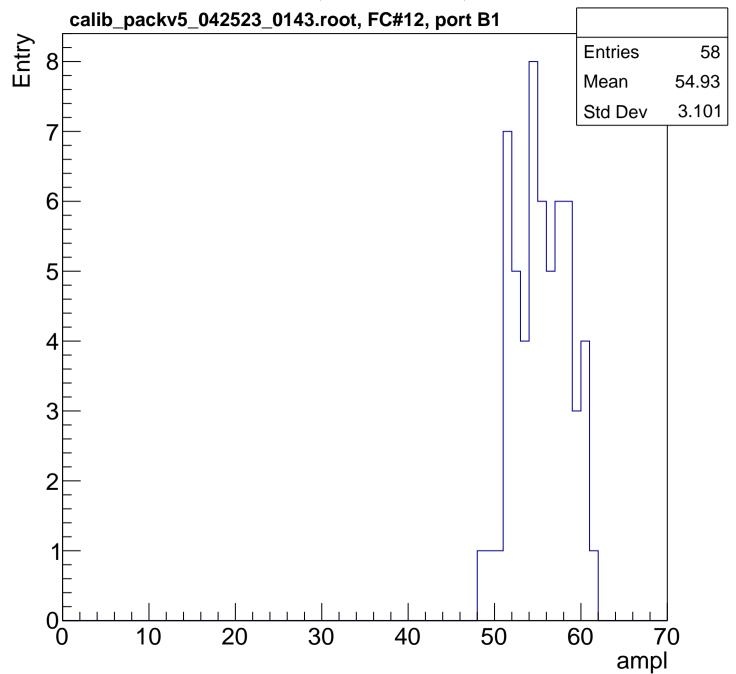


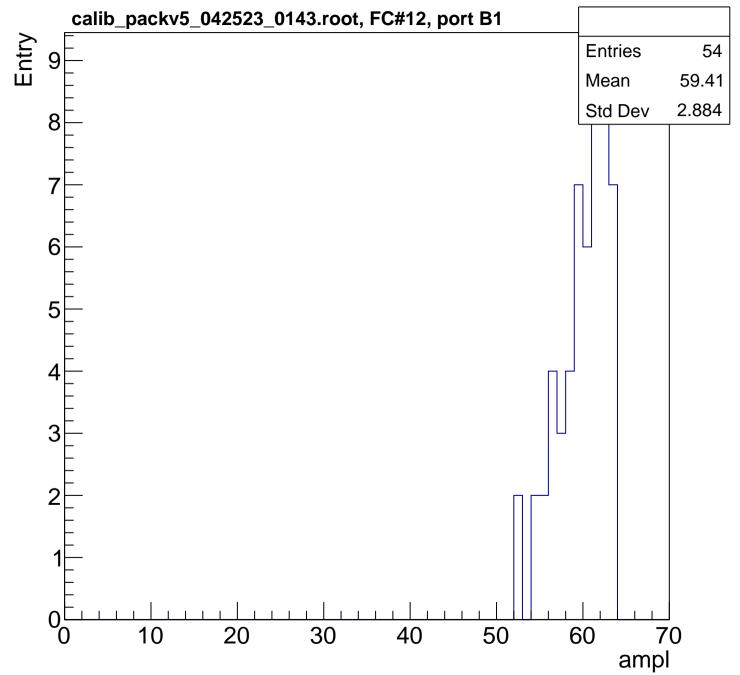


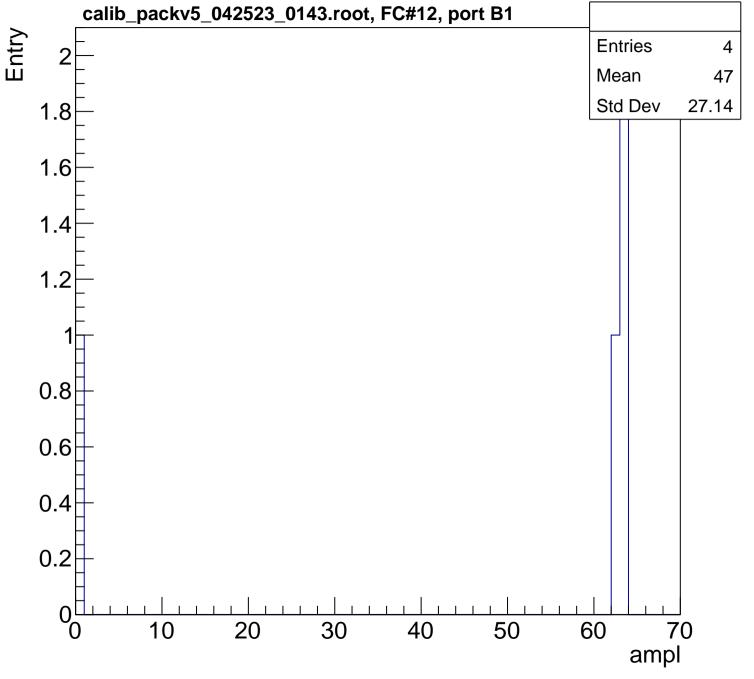


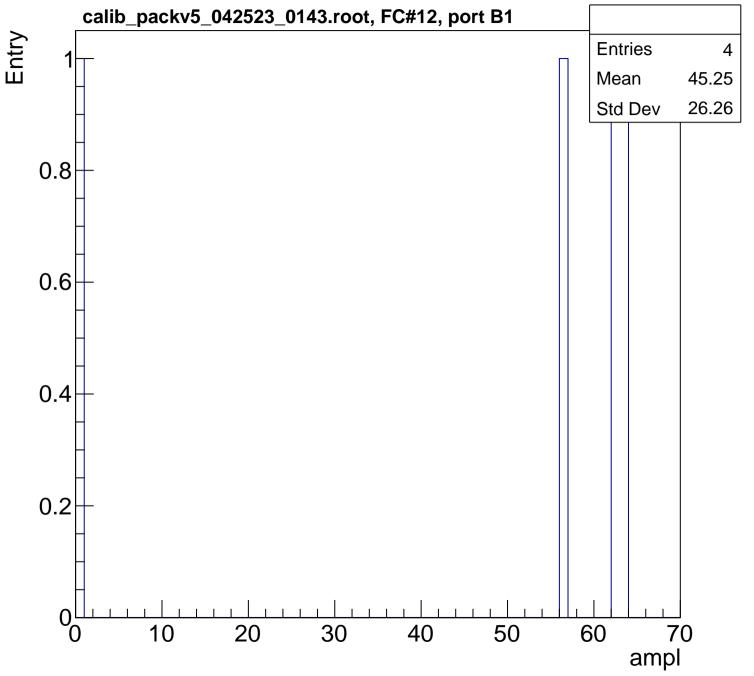


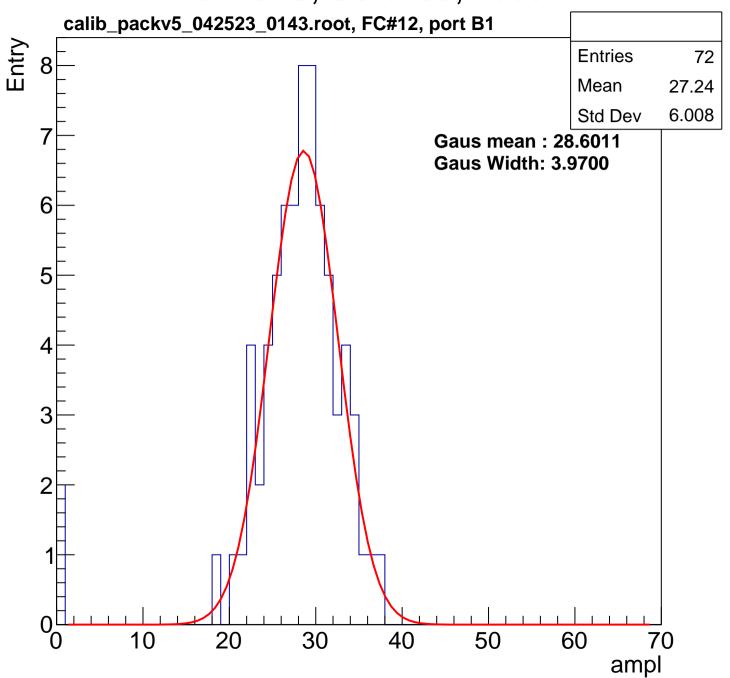


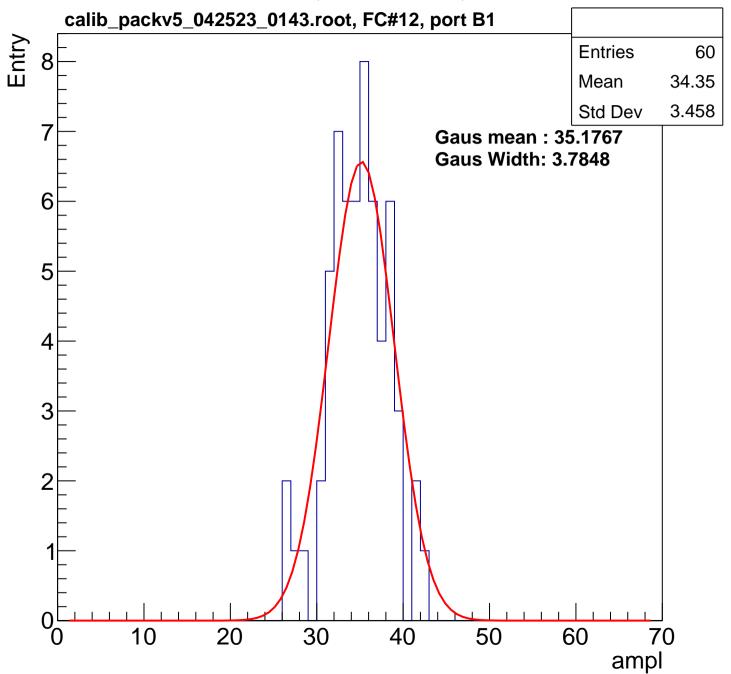


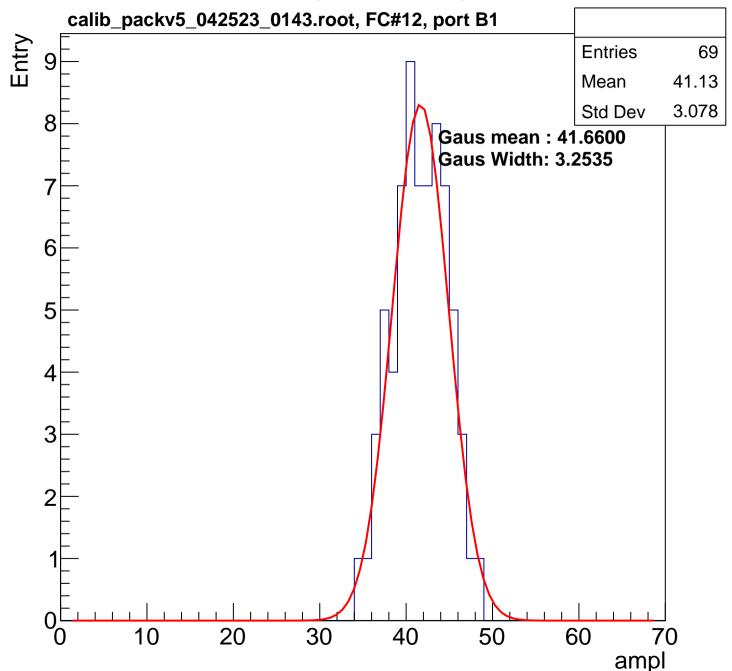


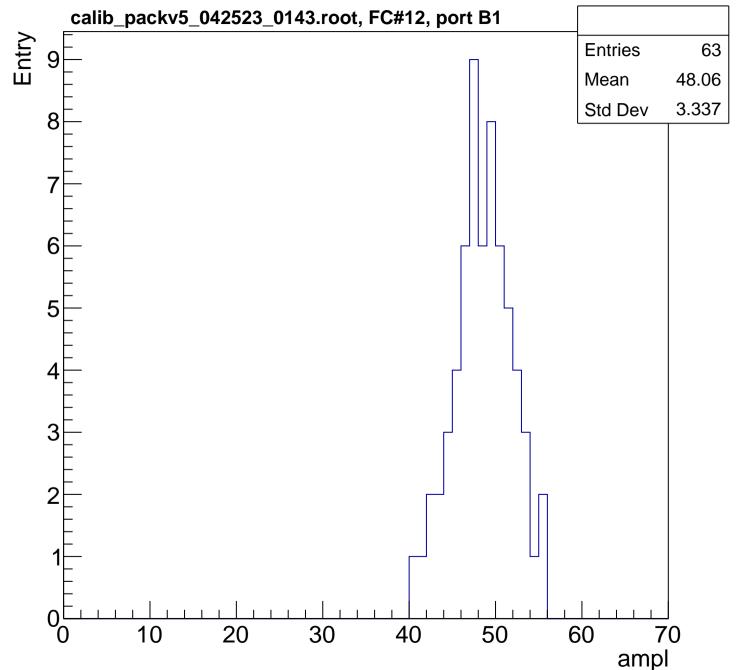


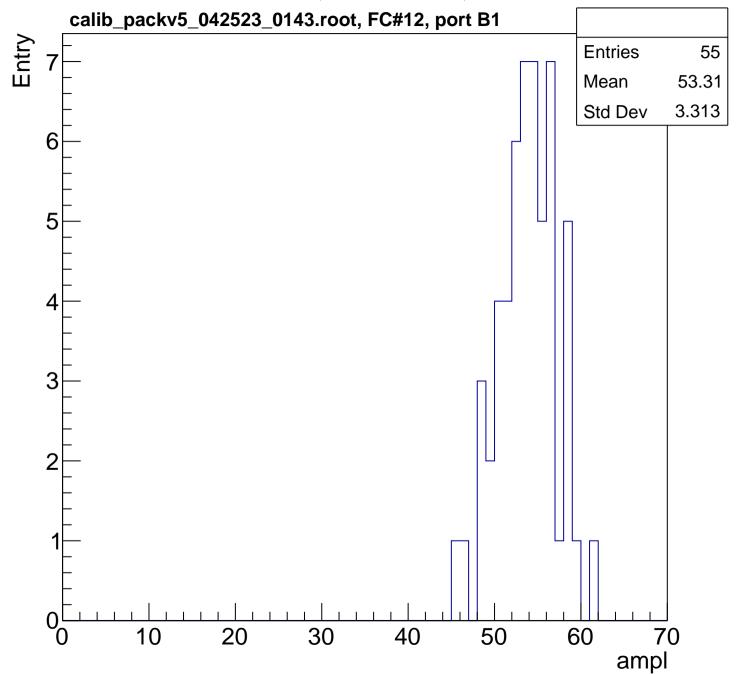


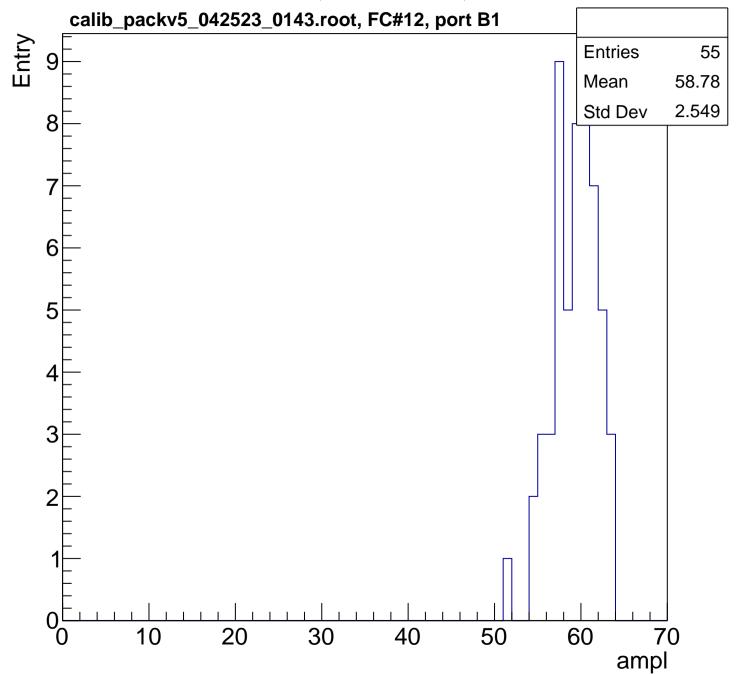


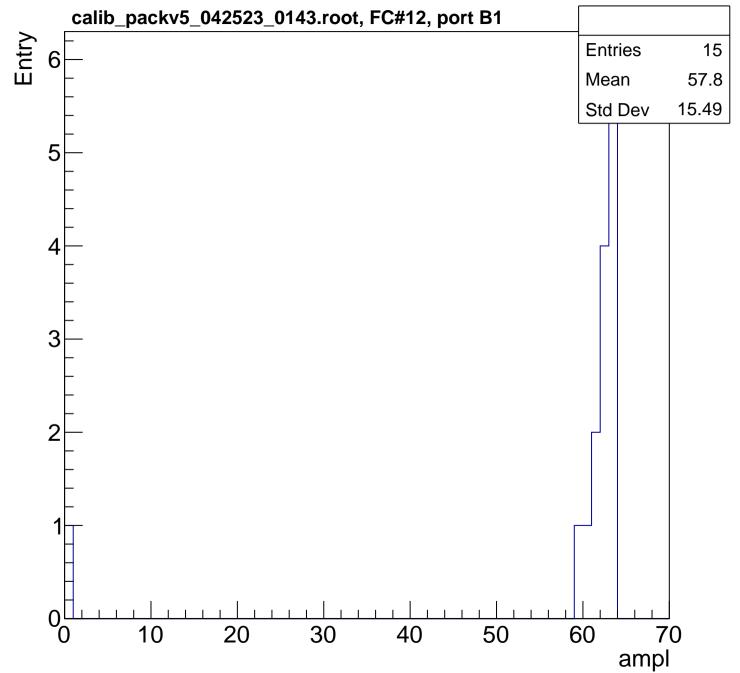


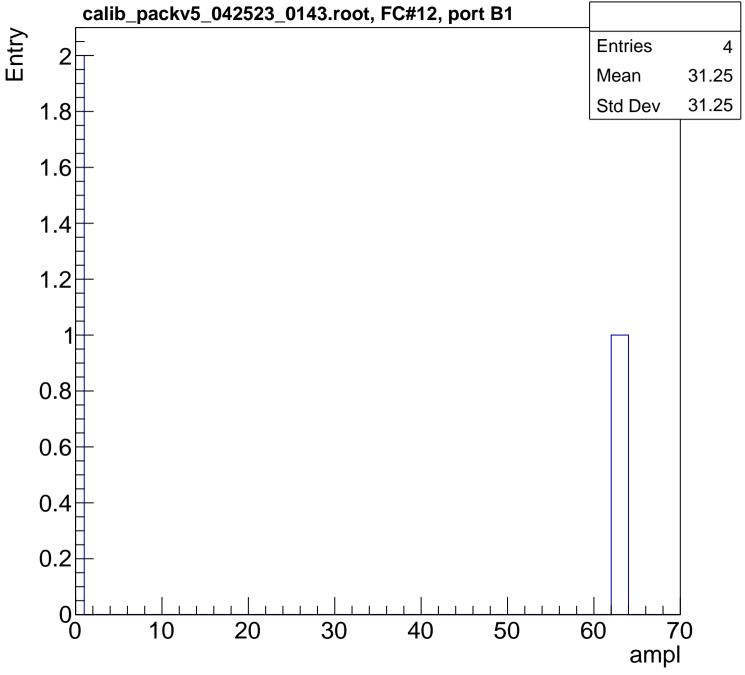


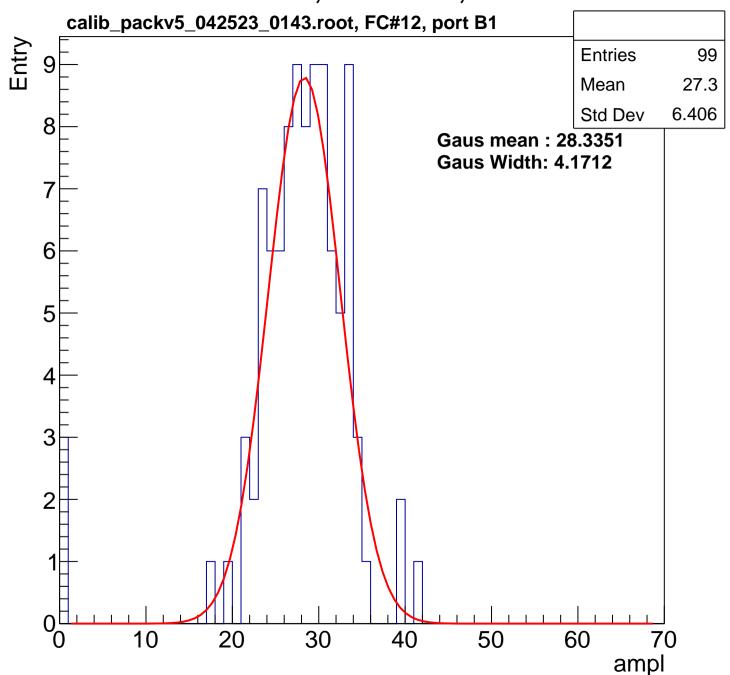


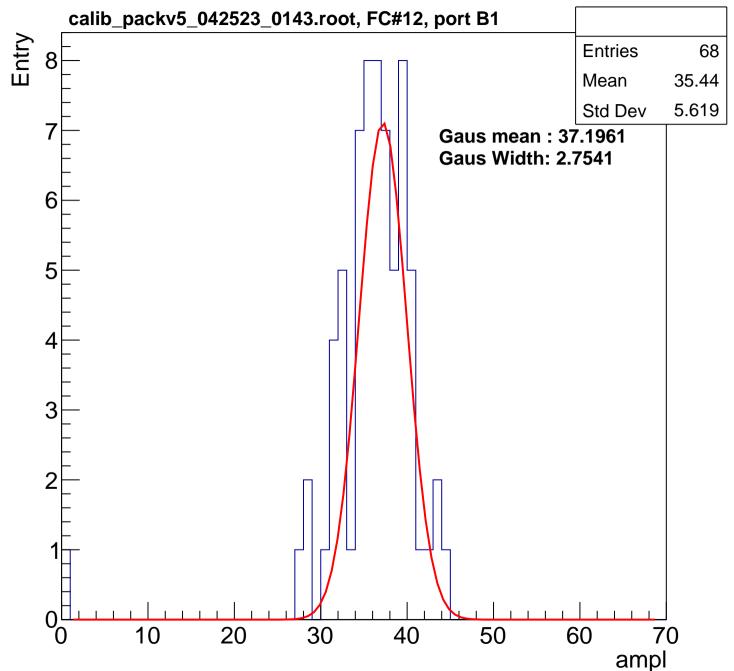


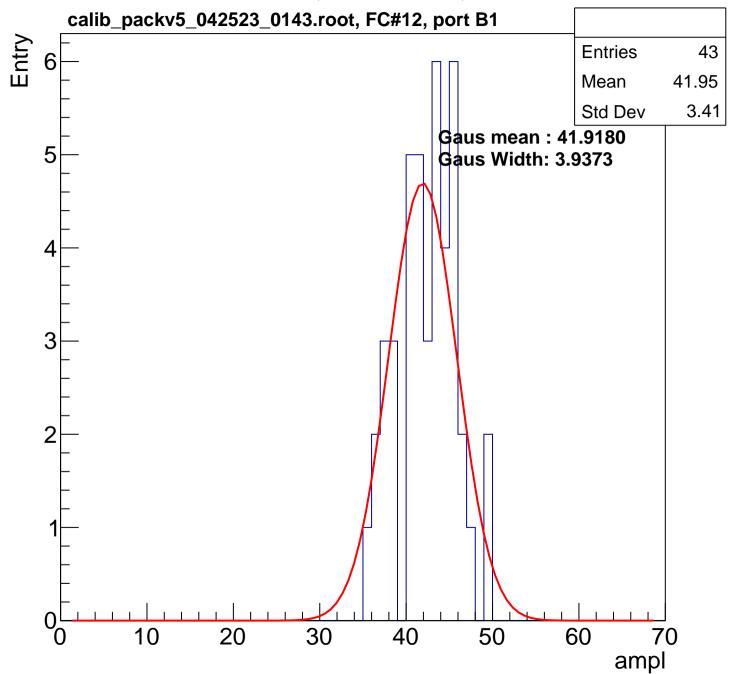


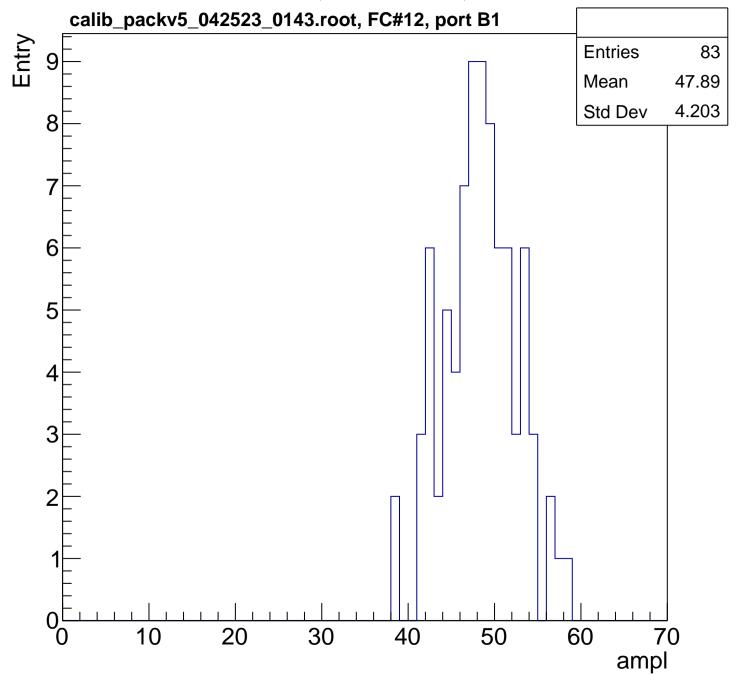


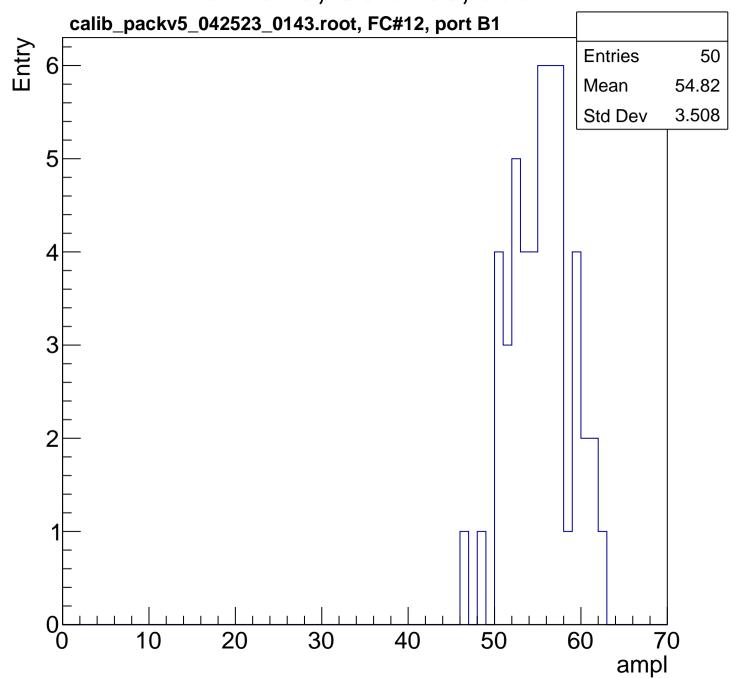


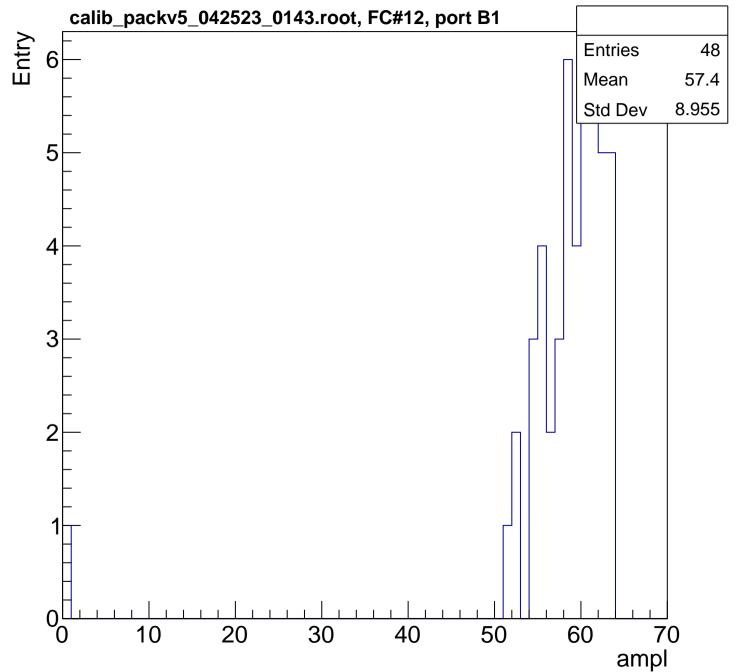


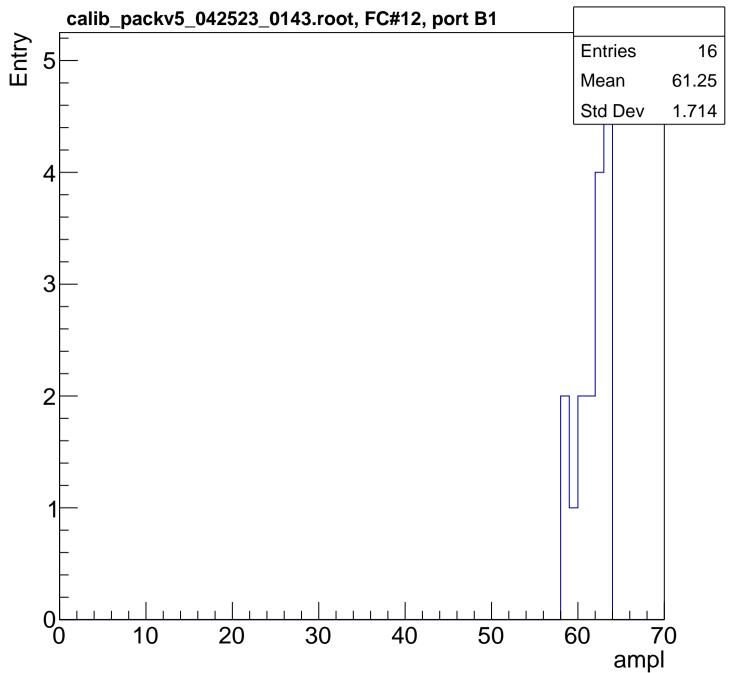


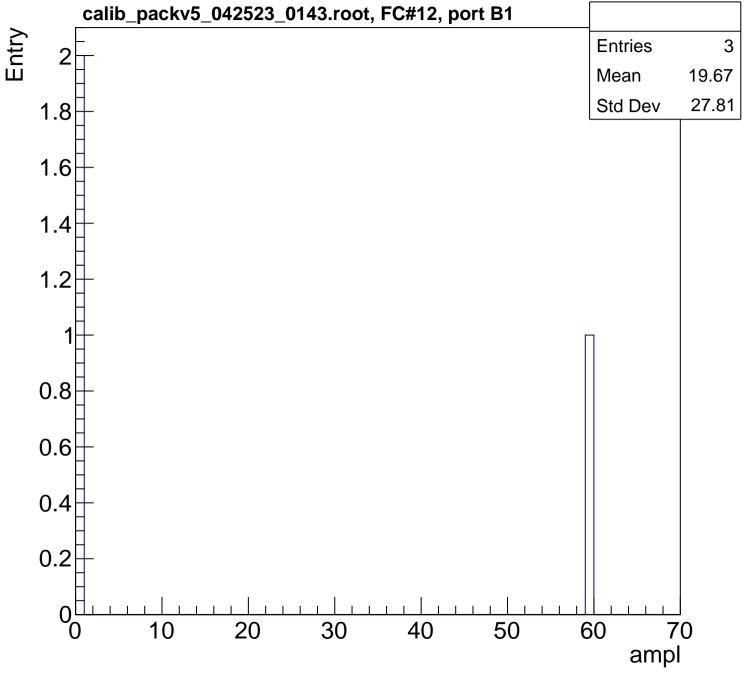


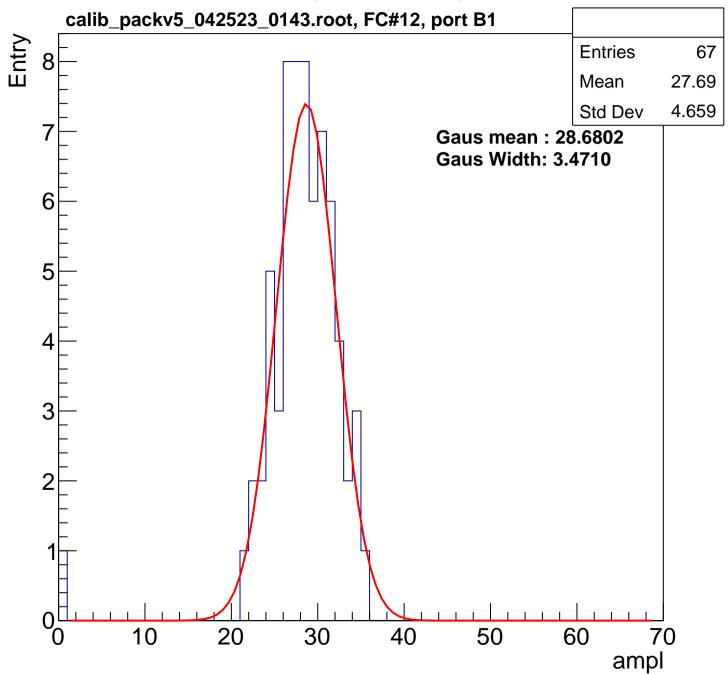


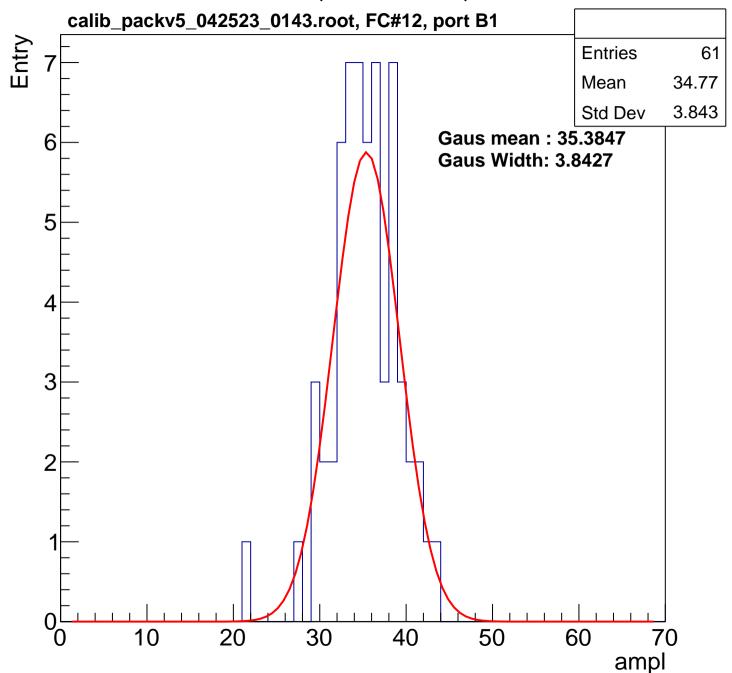


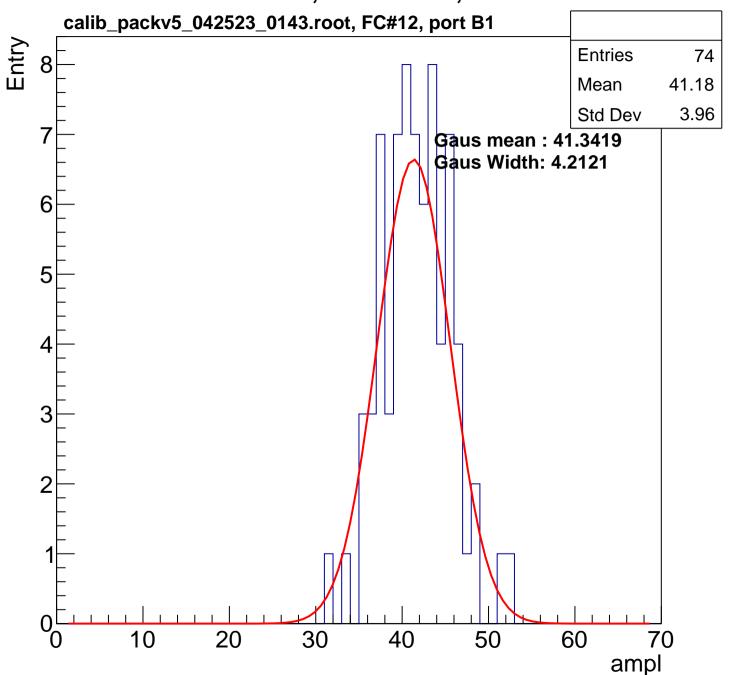


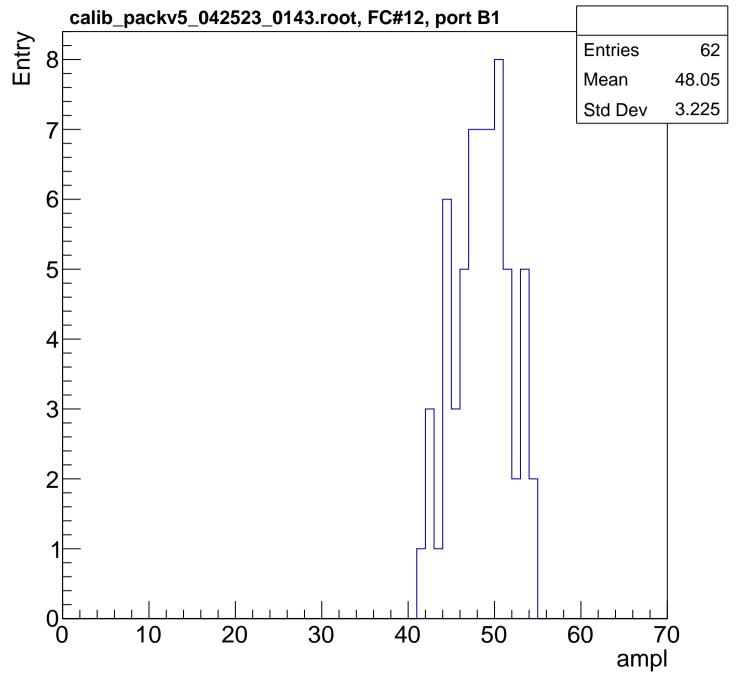


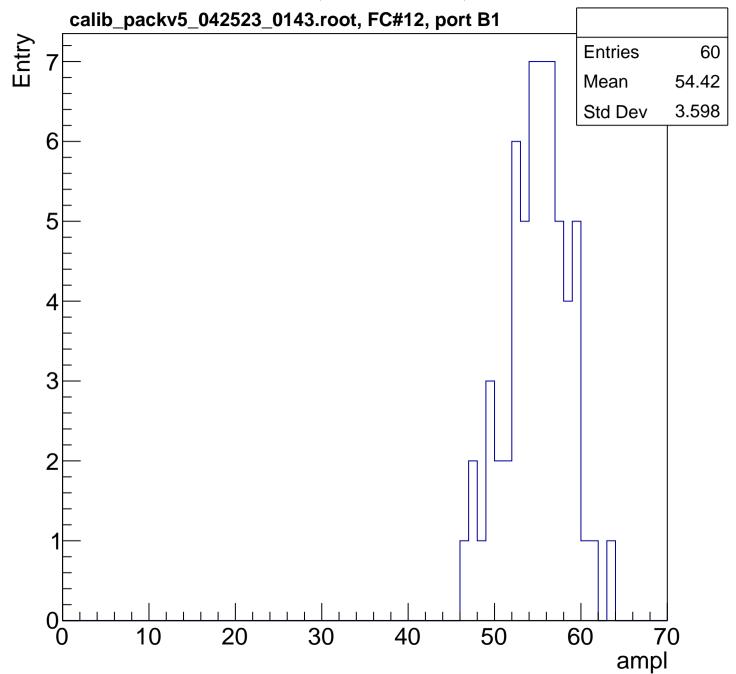


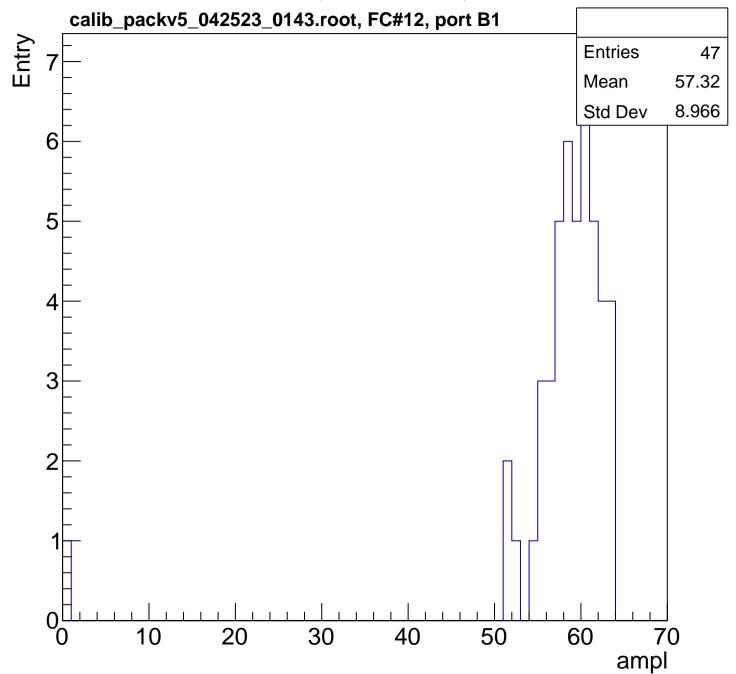


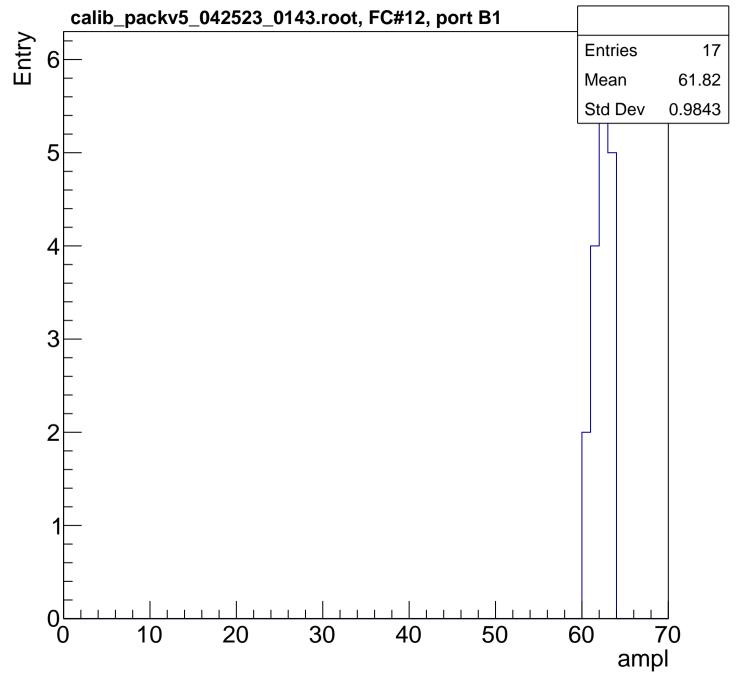


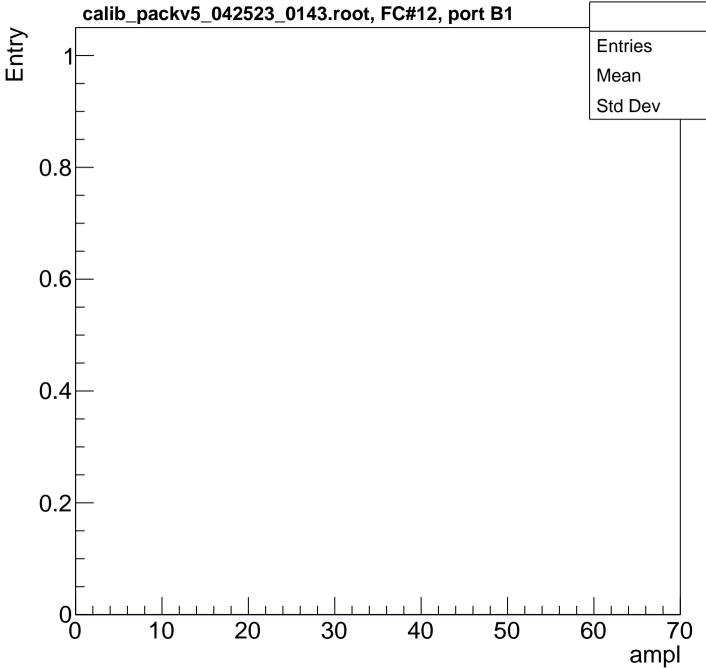


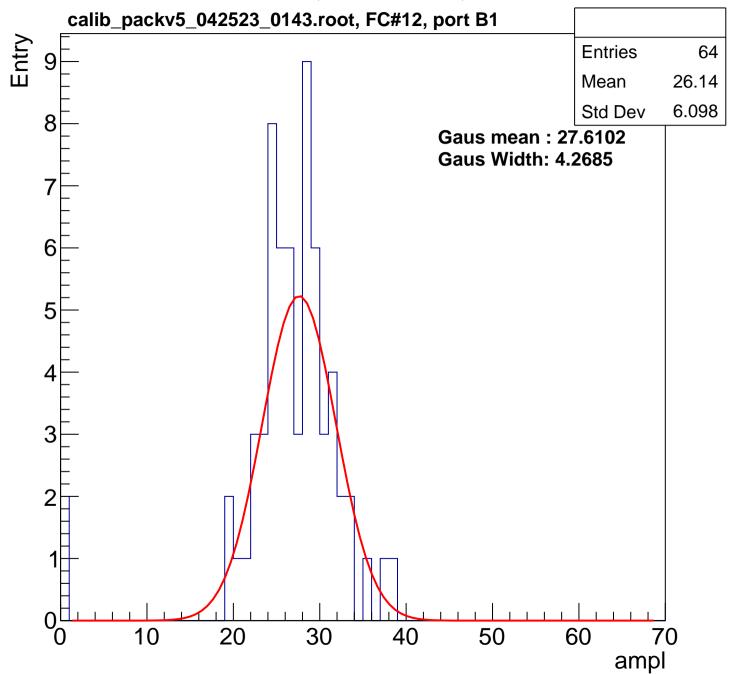


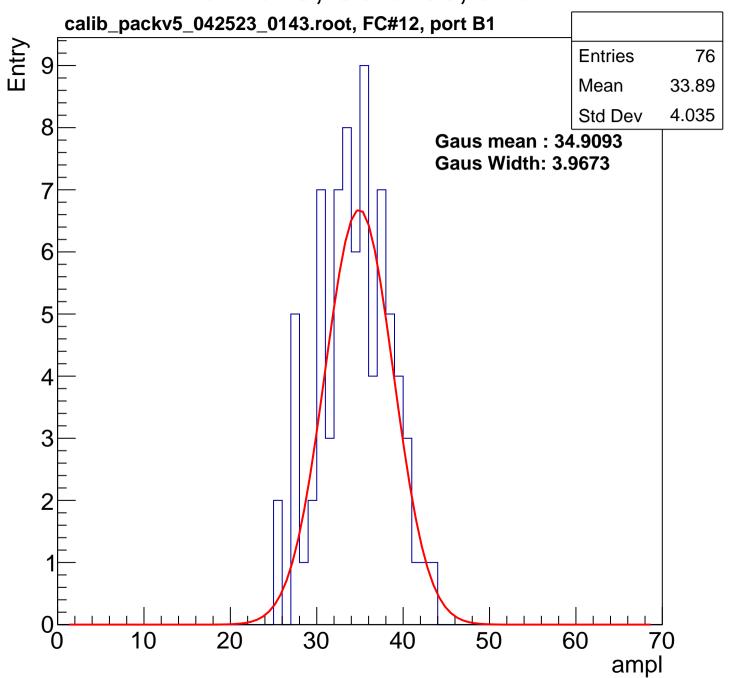


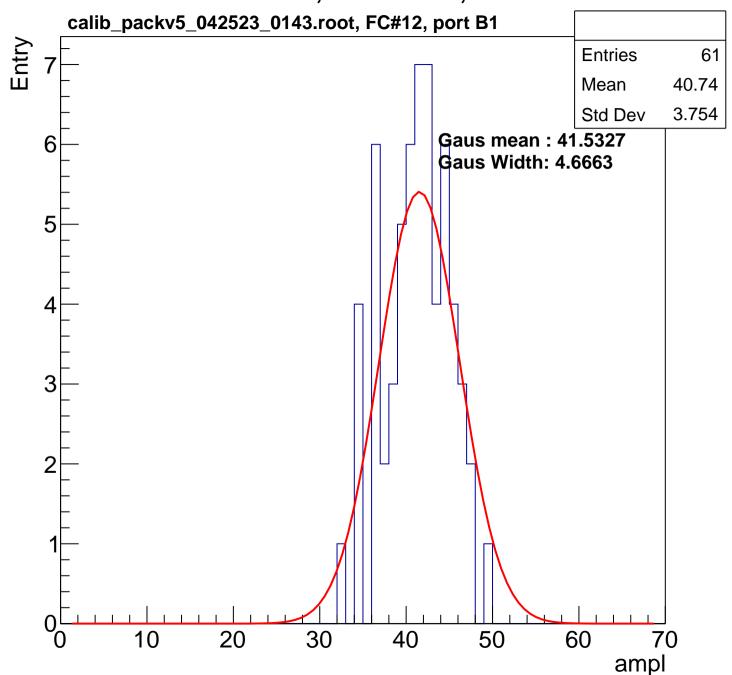


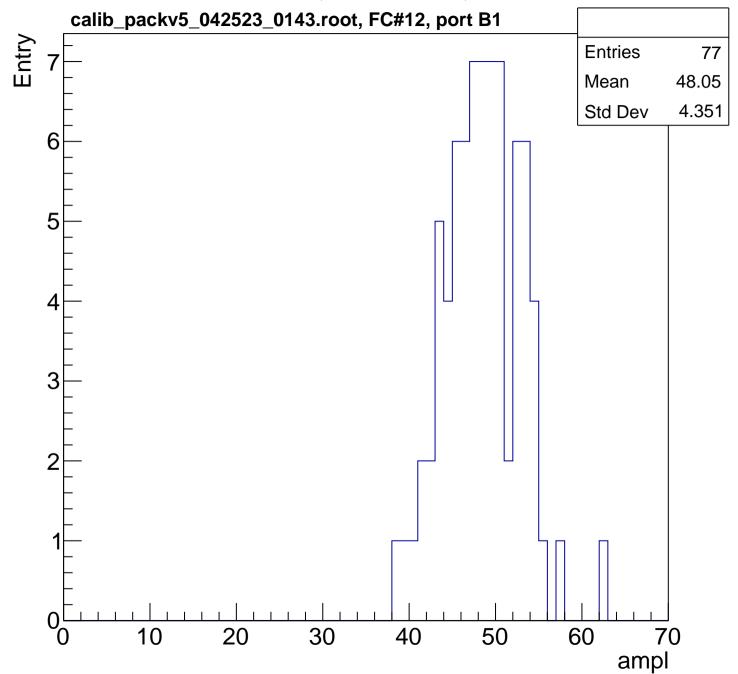


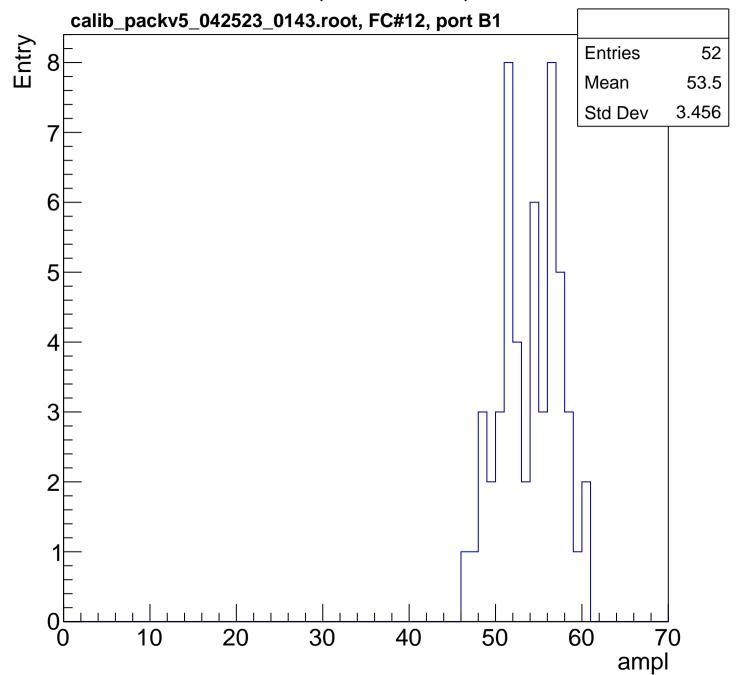


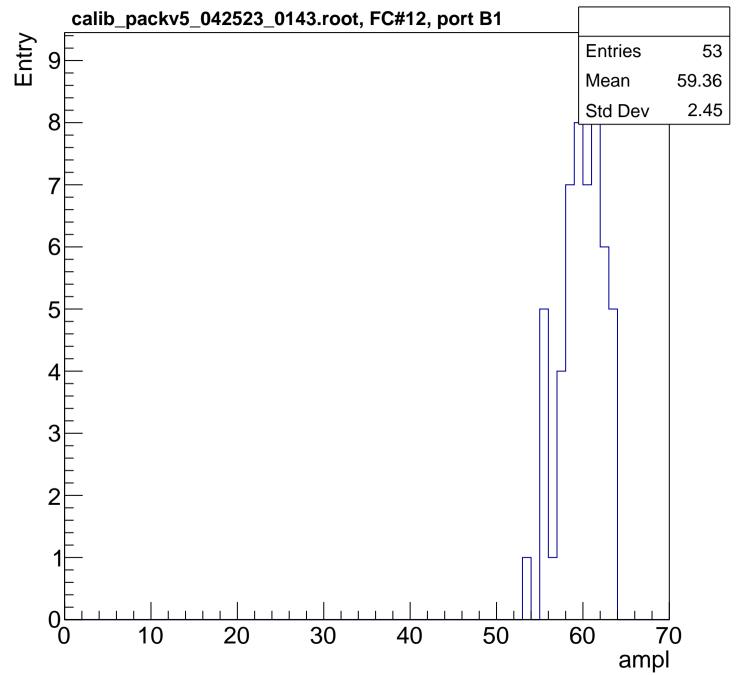


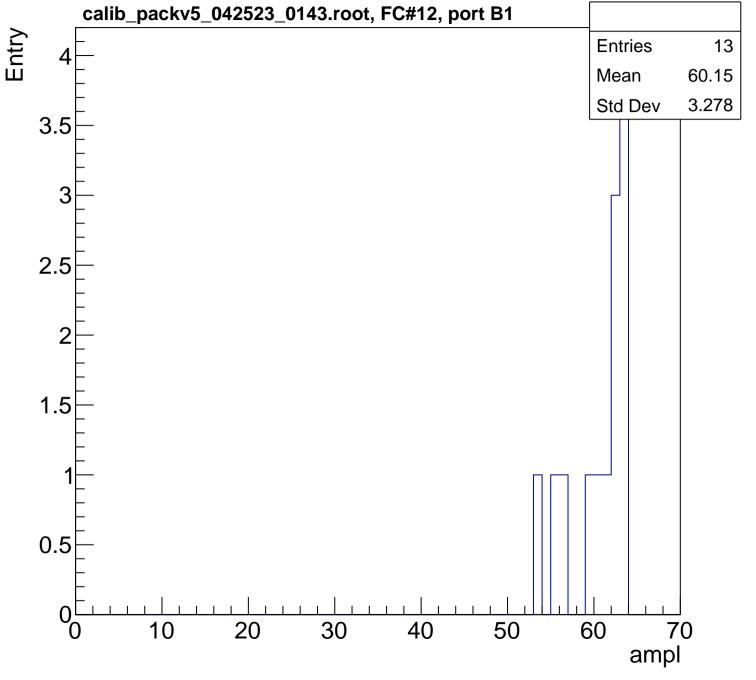


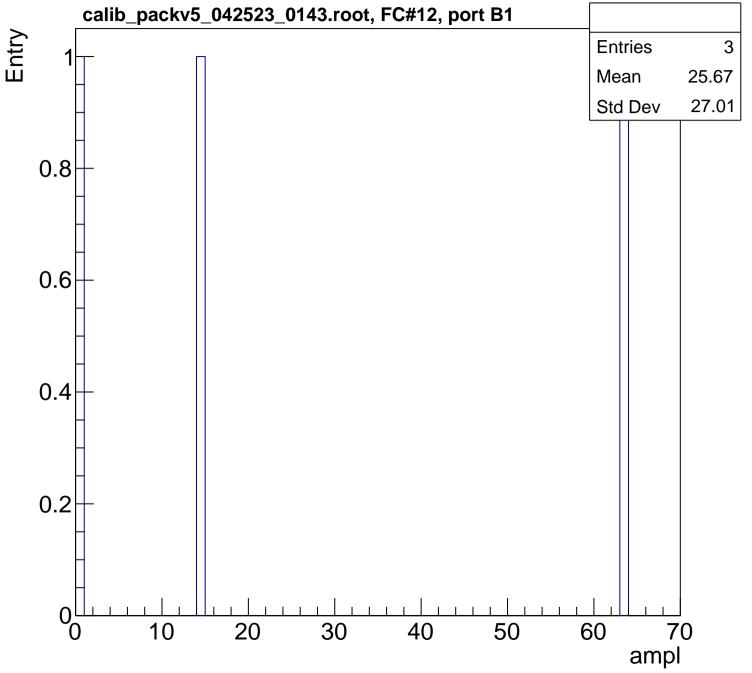


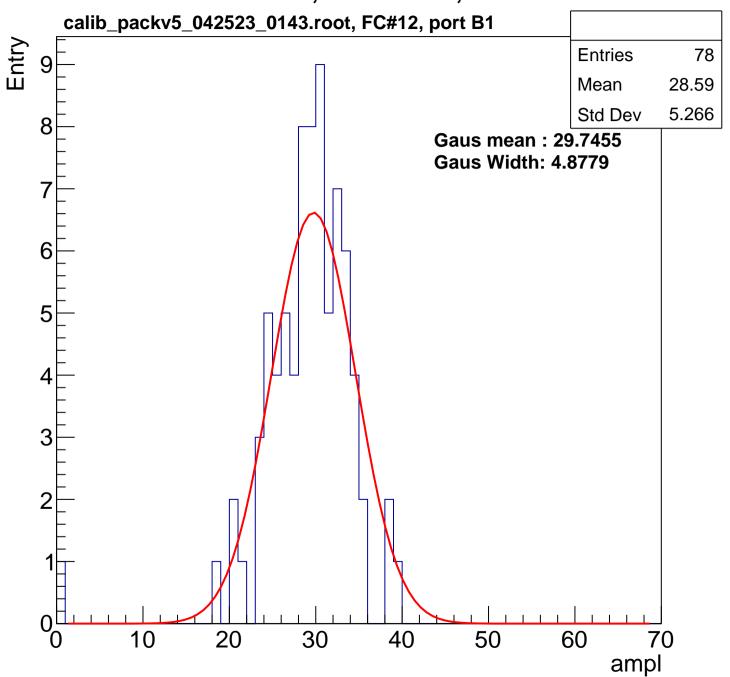


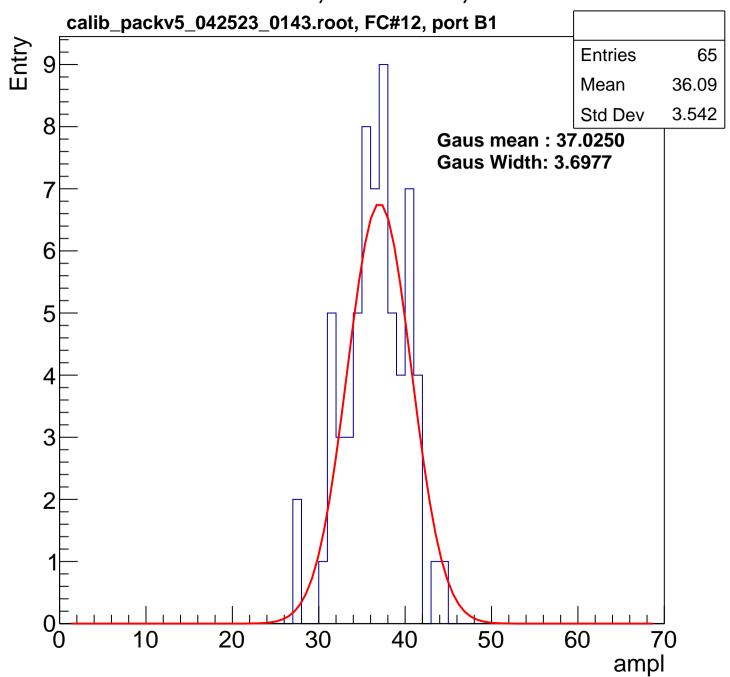


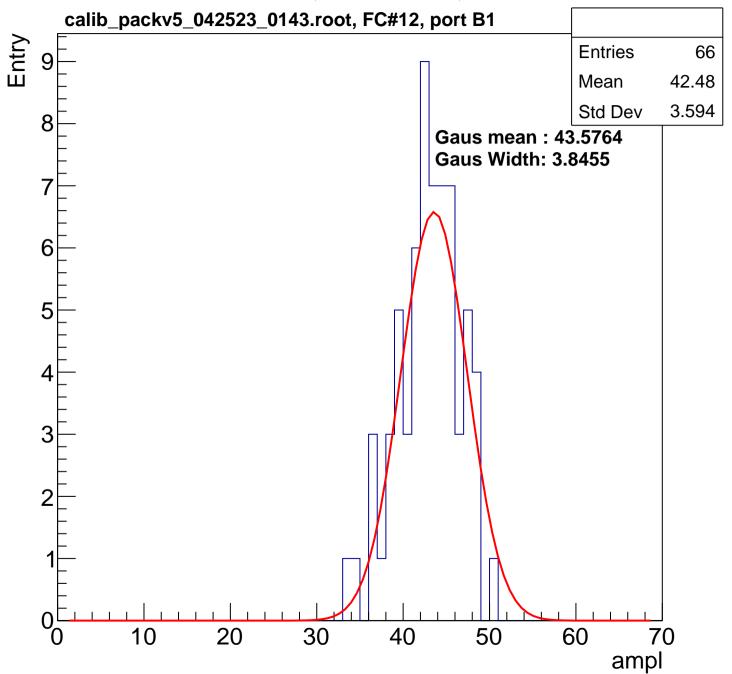


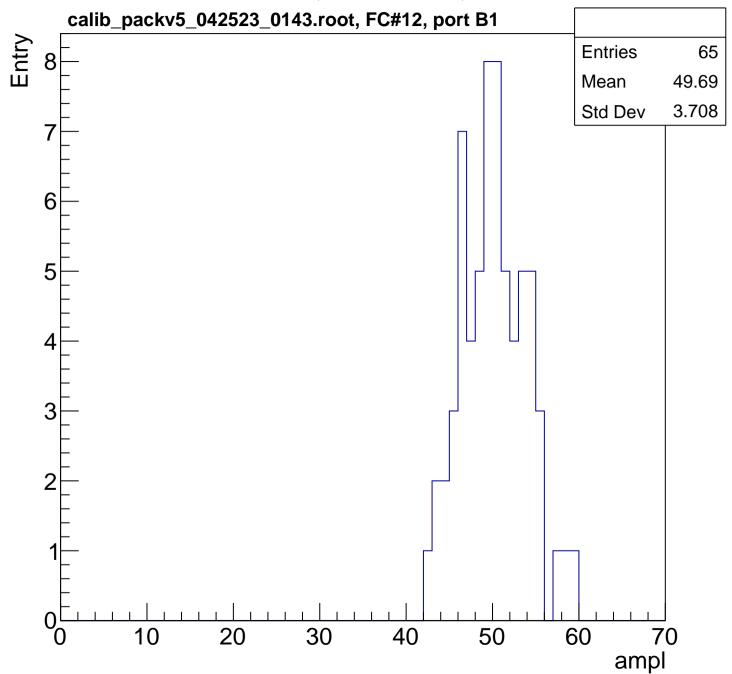


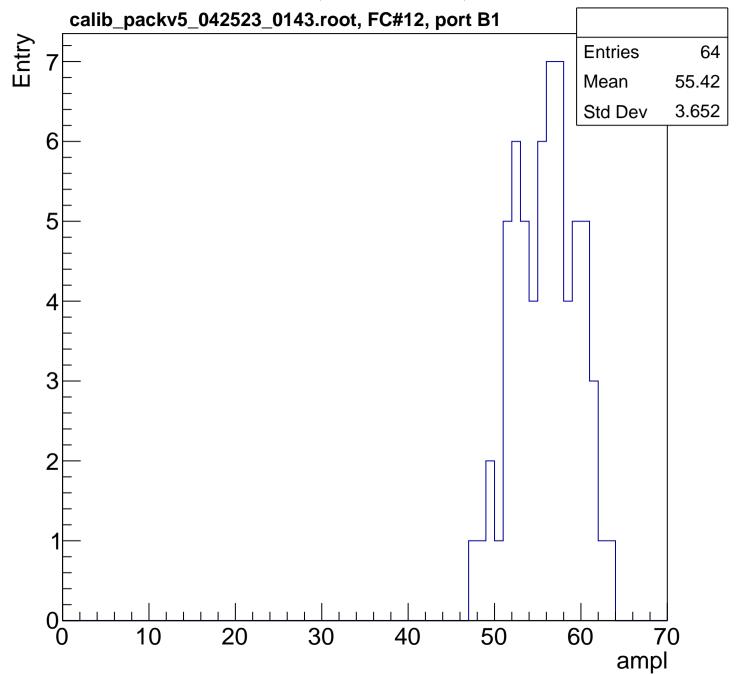


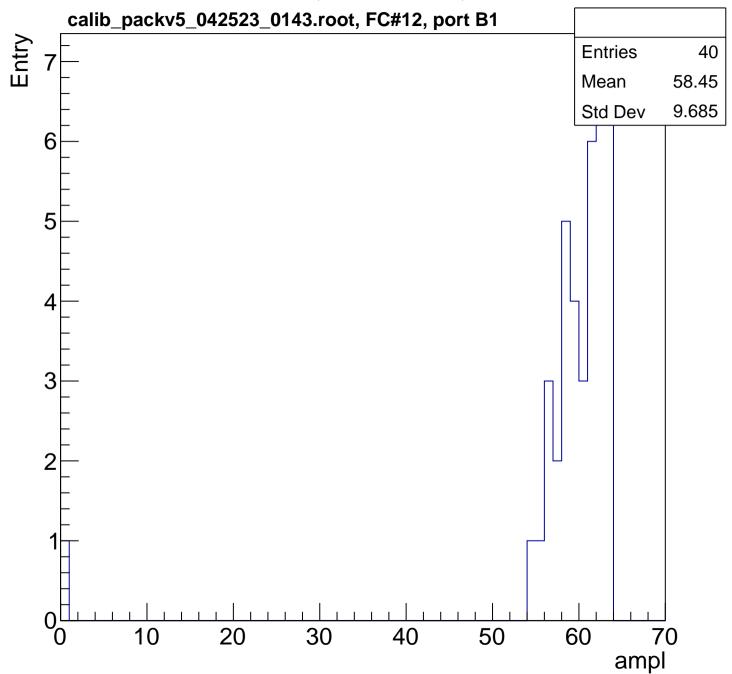


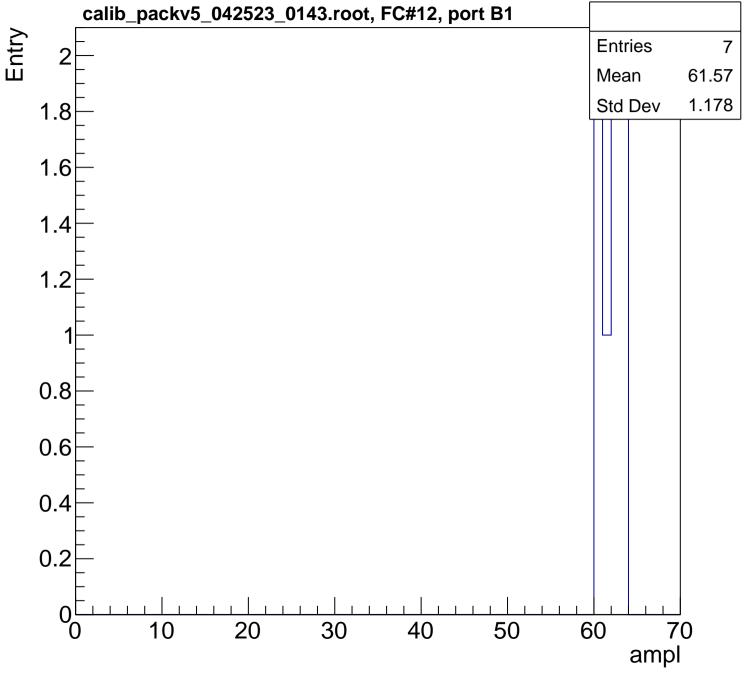


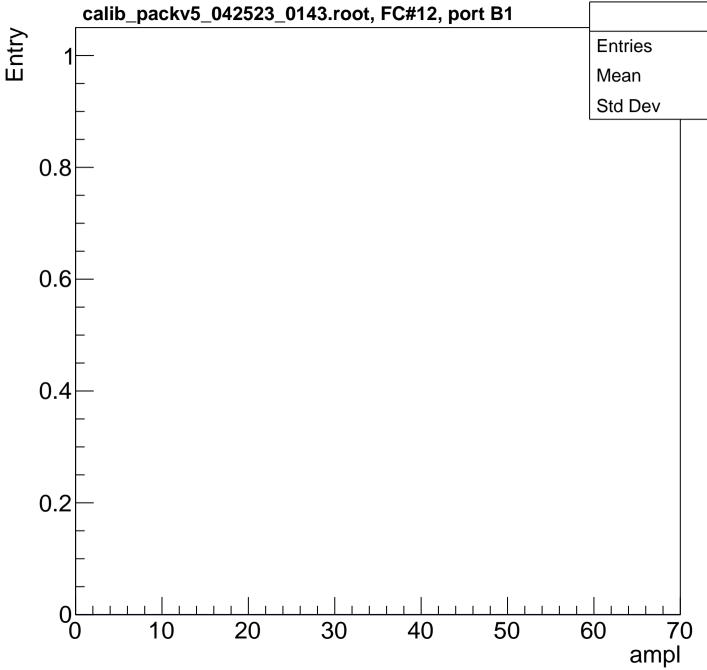


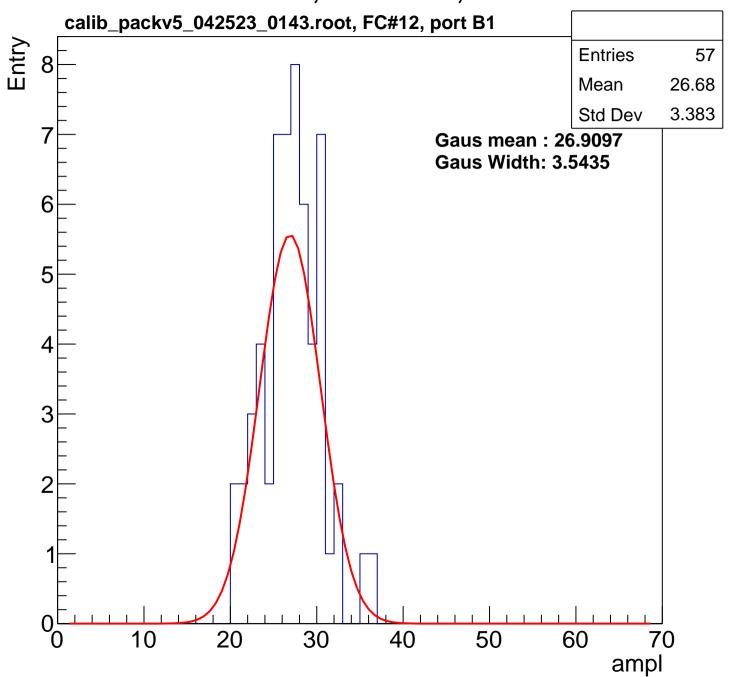


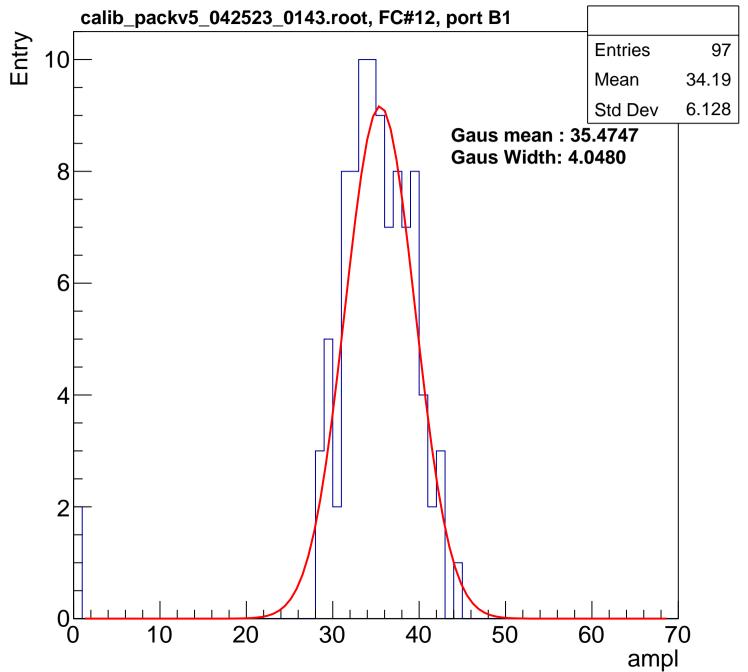


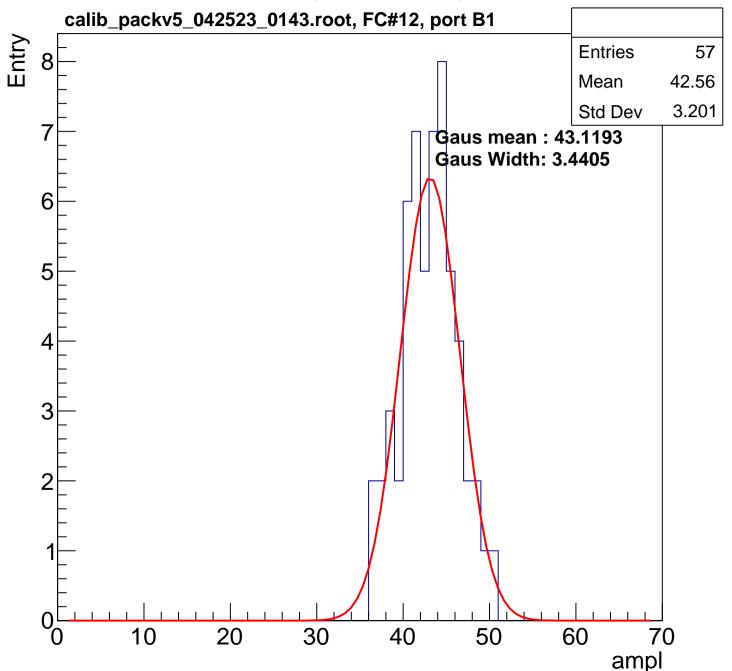


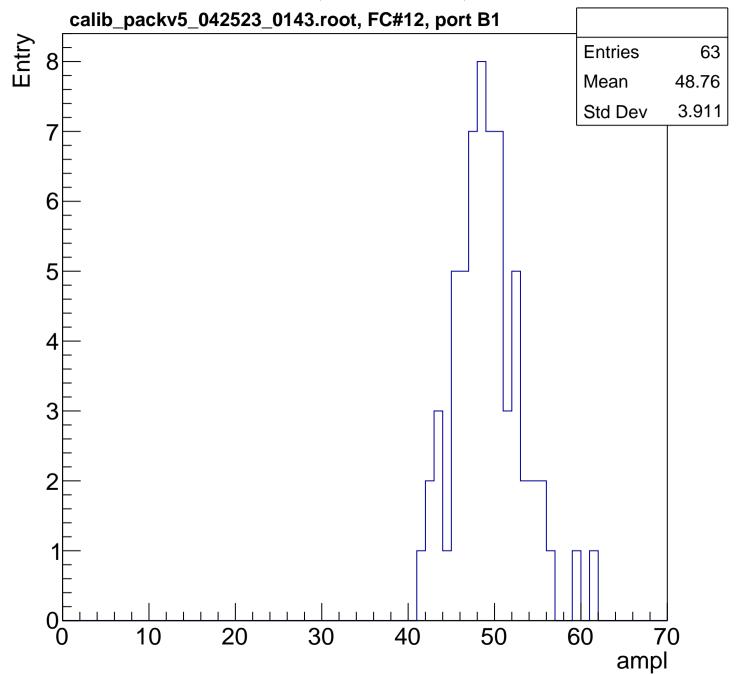


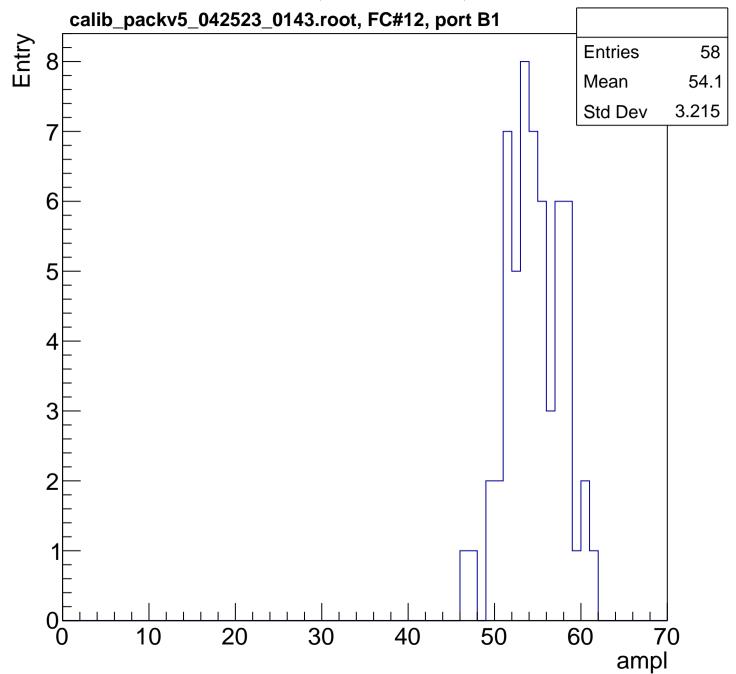


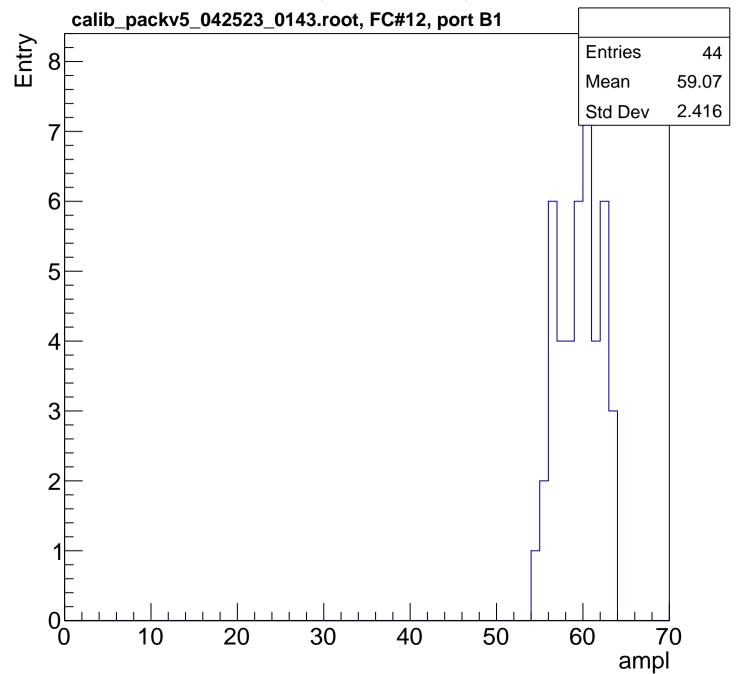


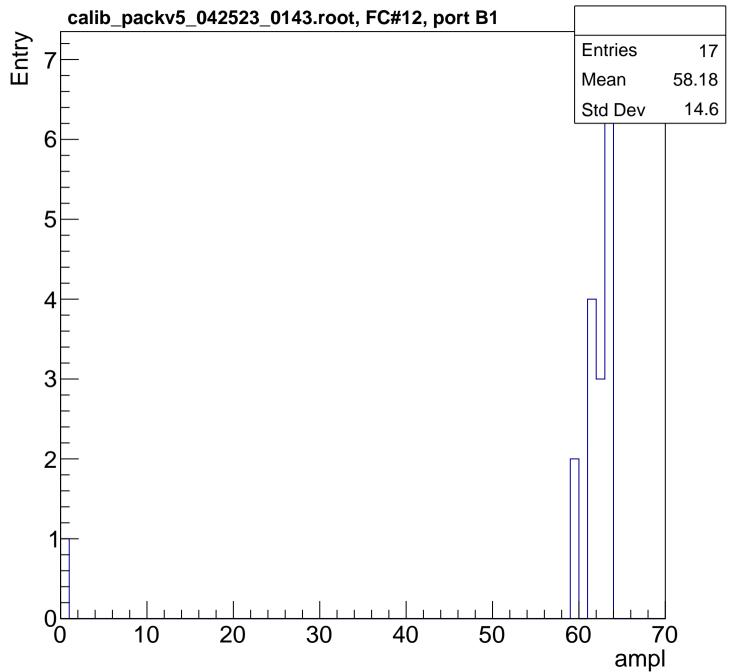




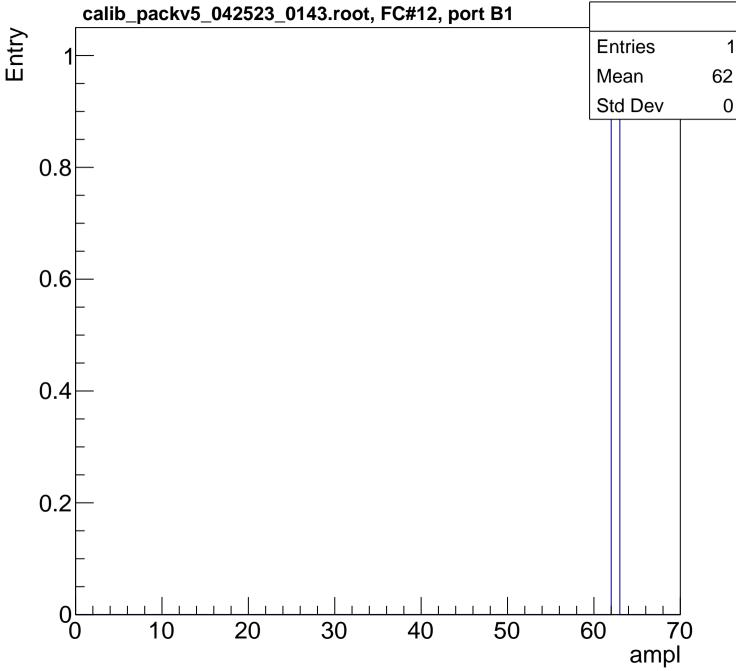


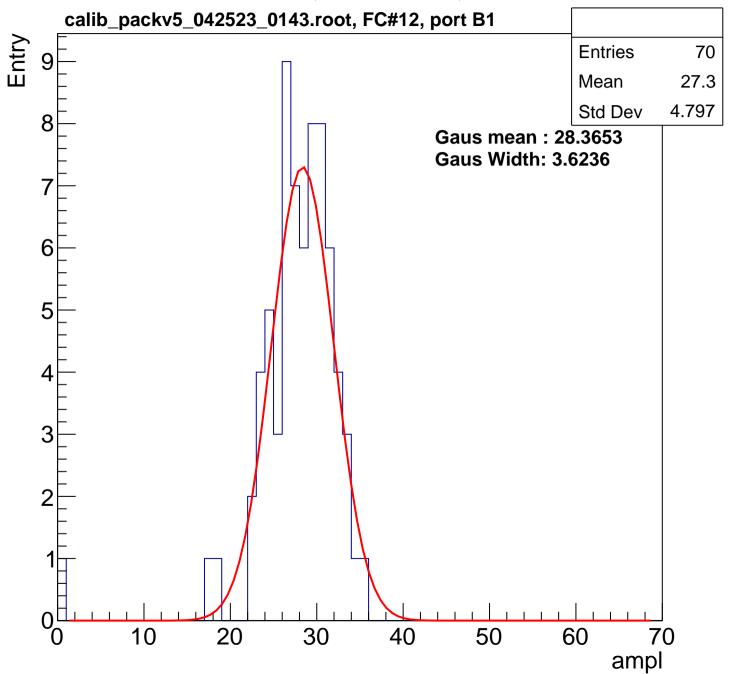


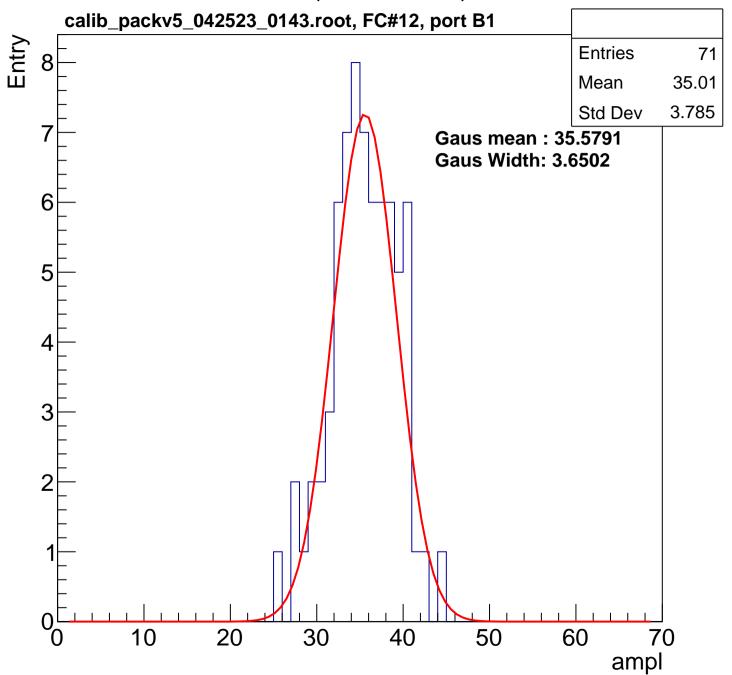


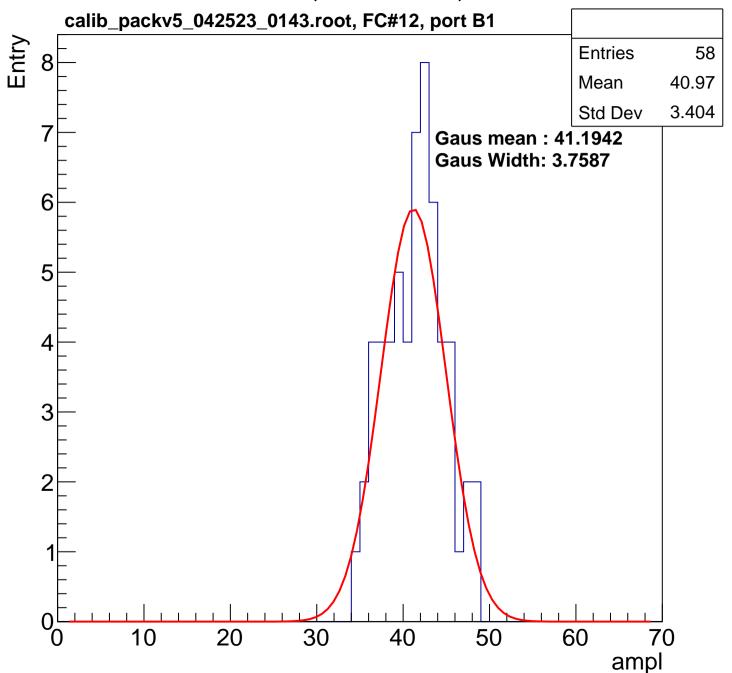


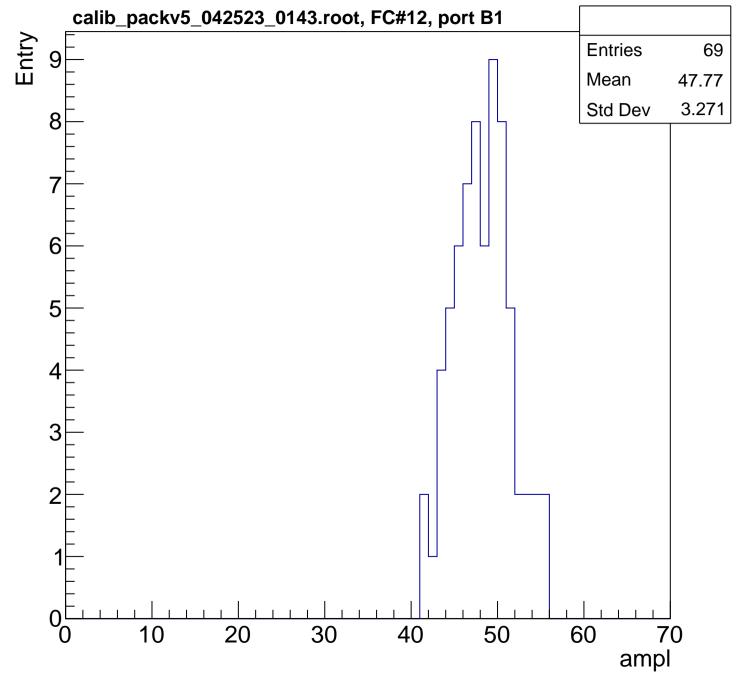
0

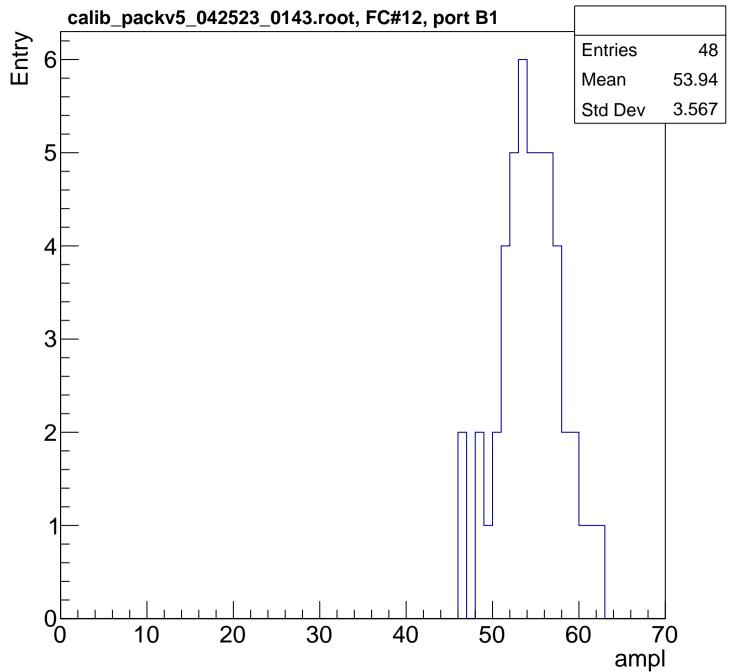


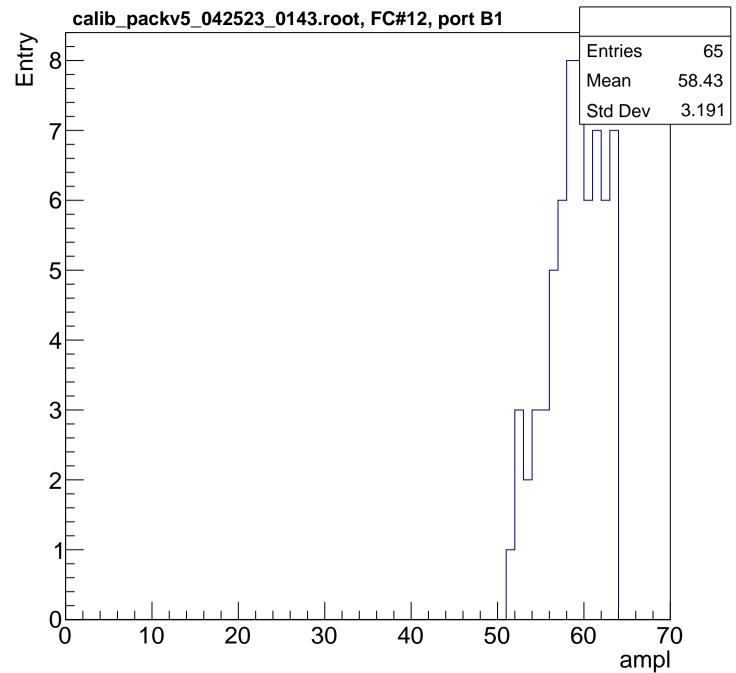


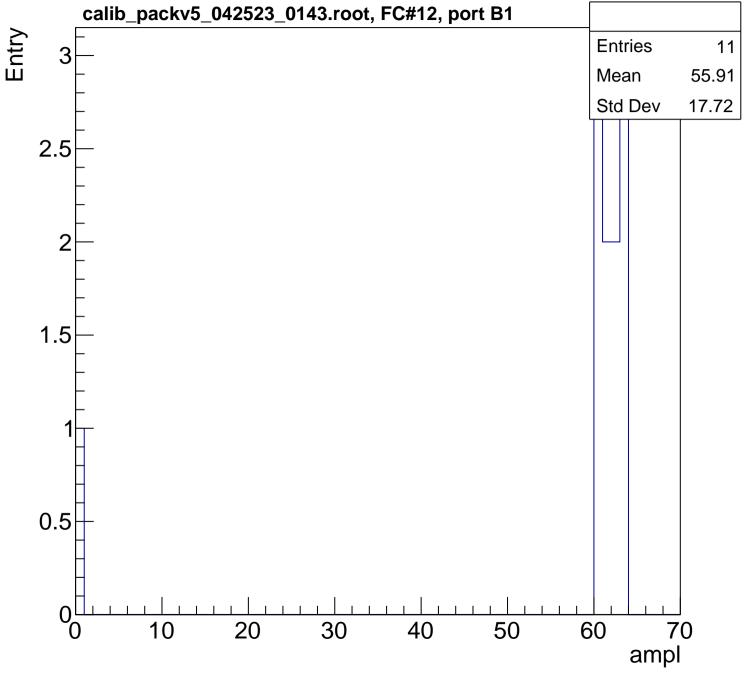


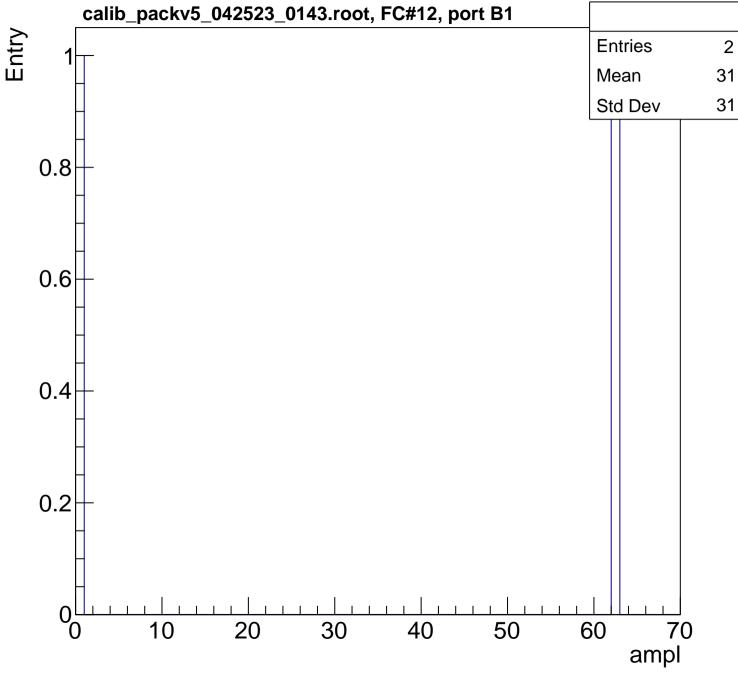


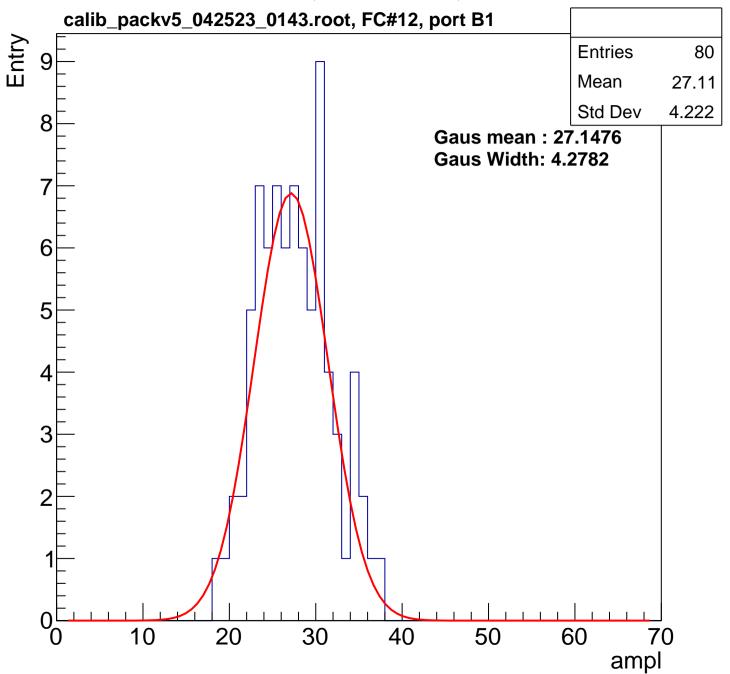


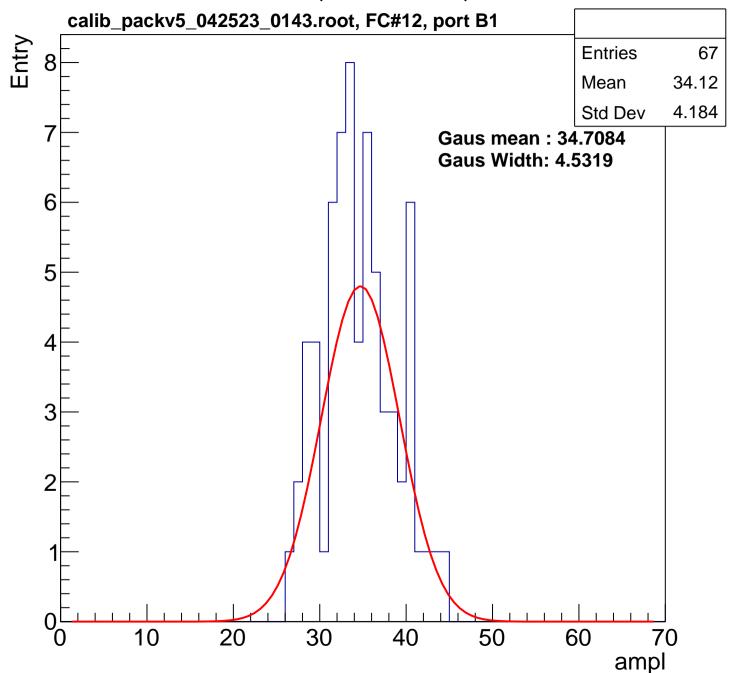


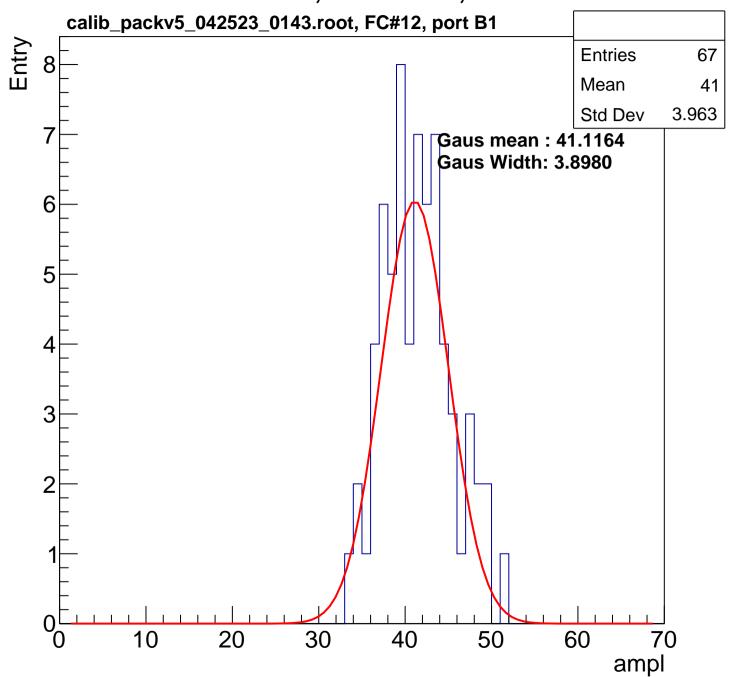


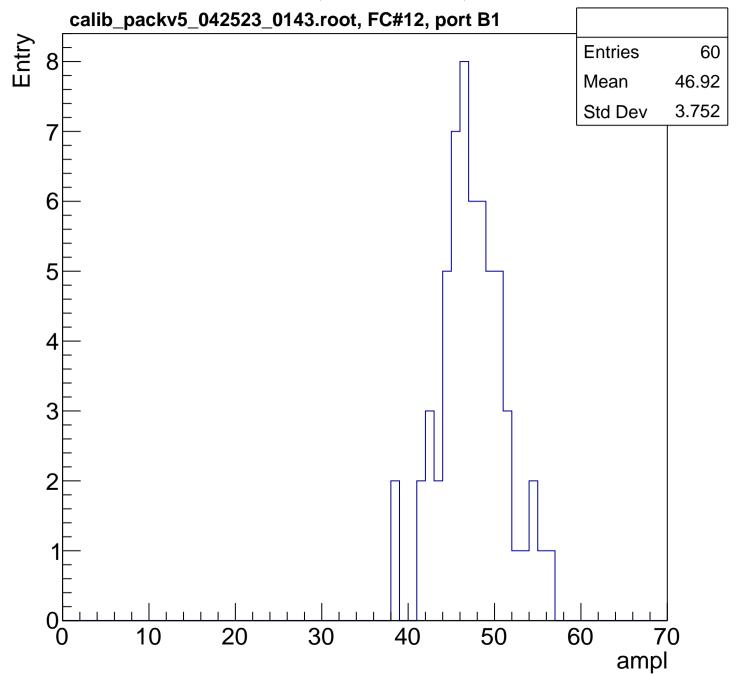


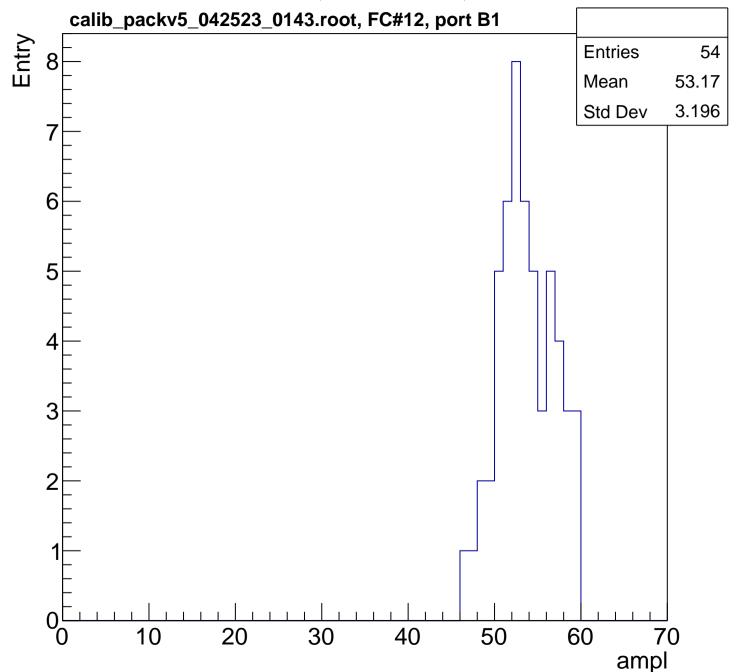


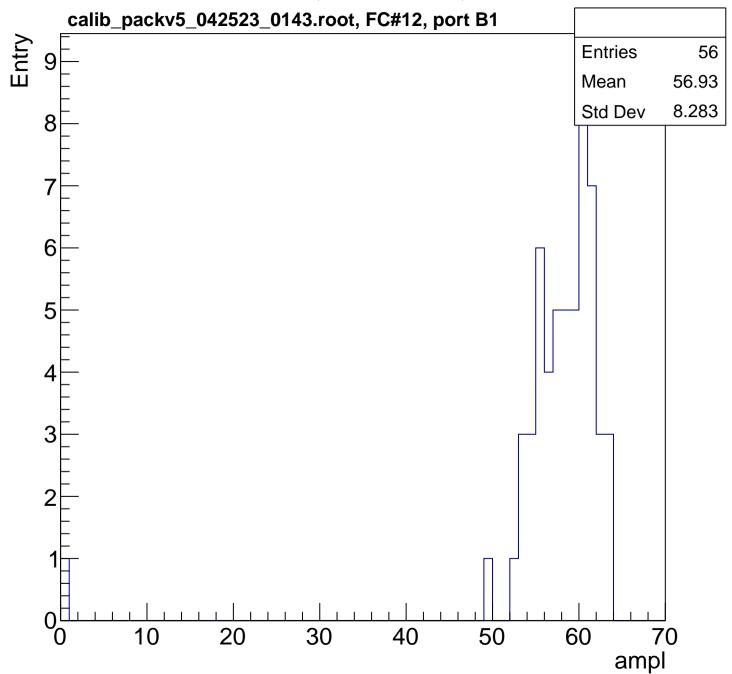


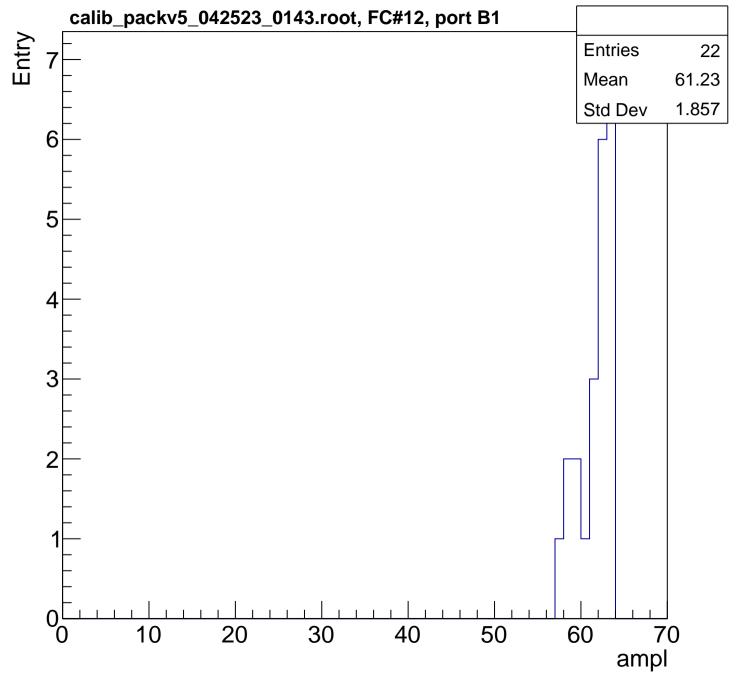


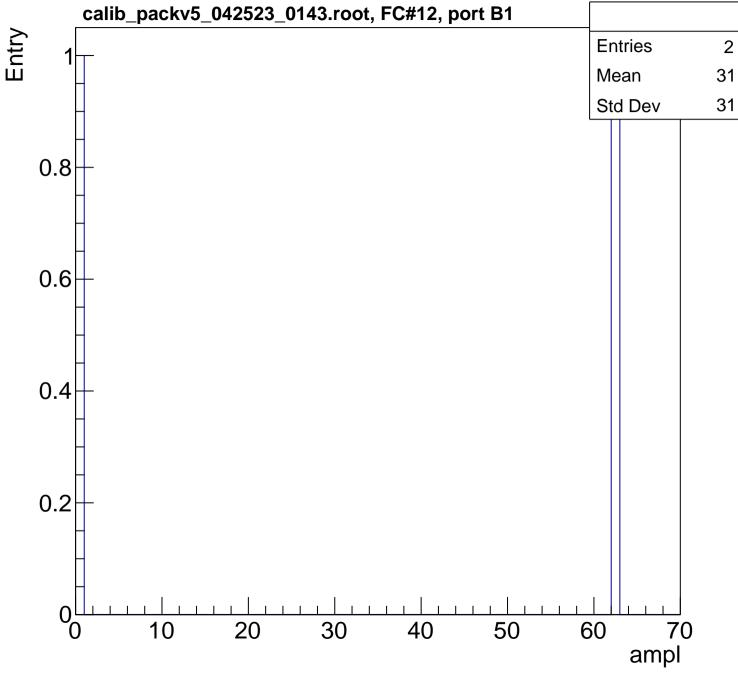


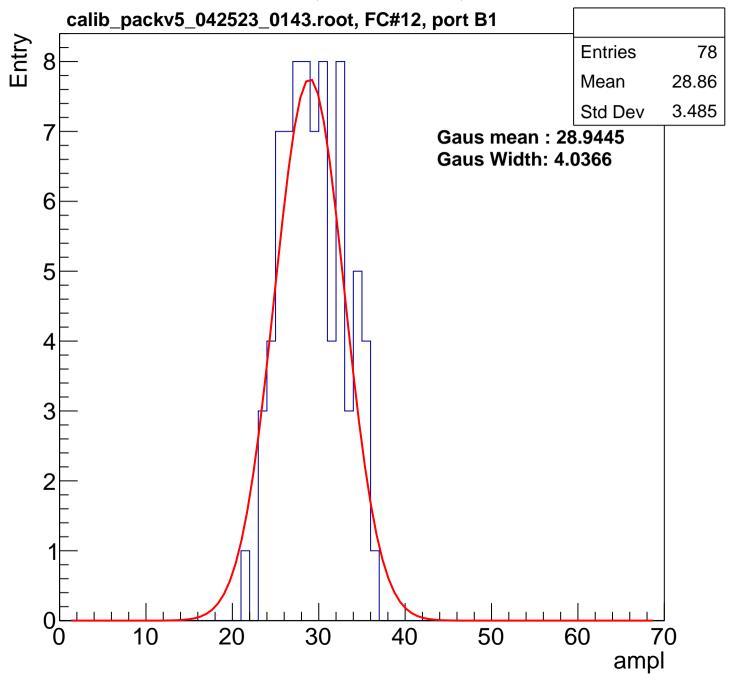


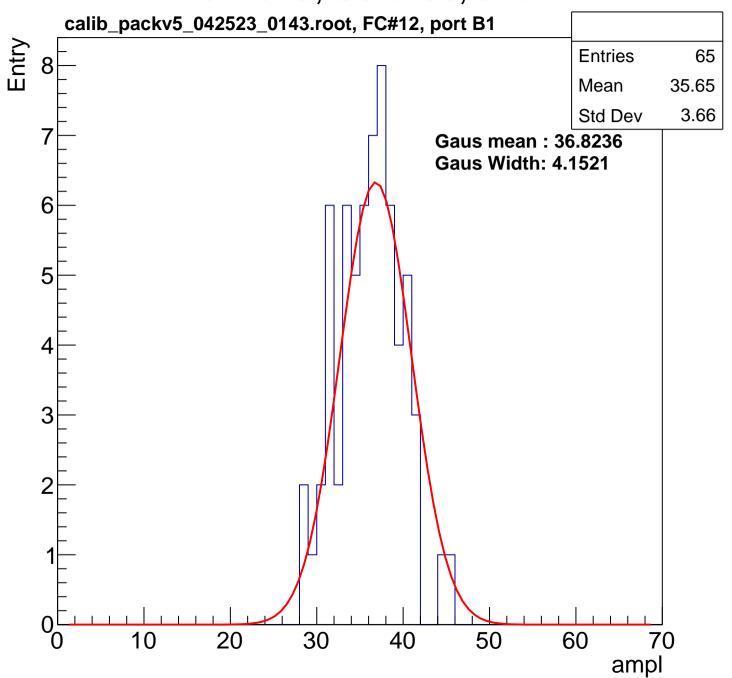


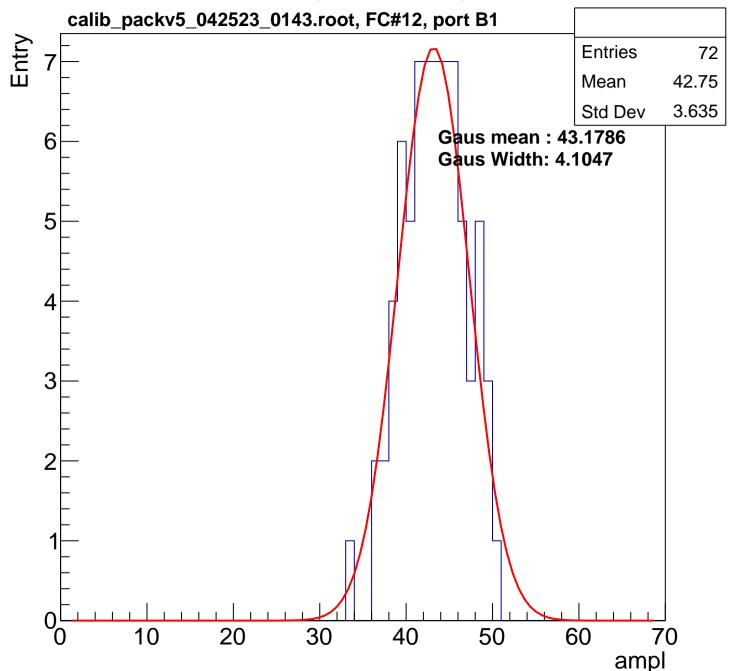


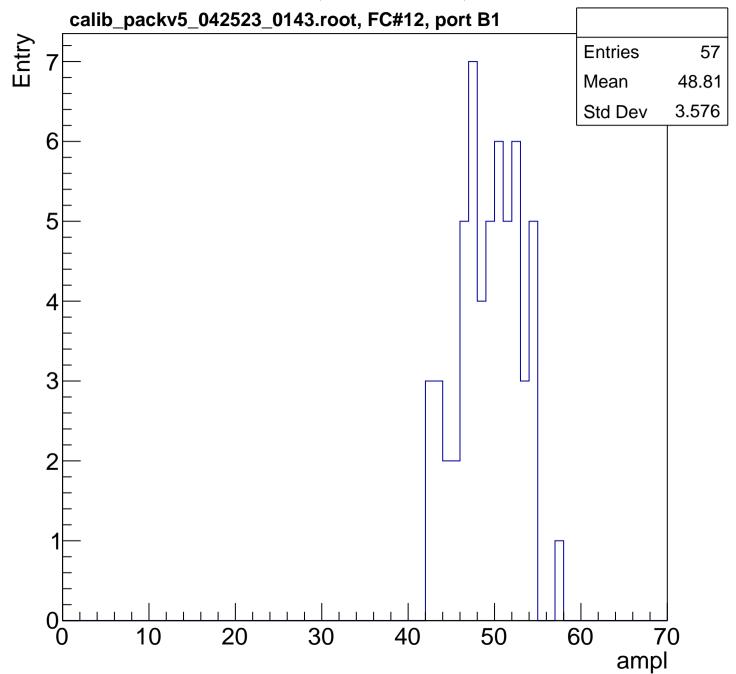


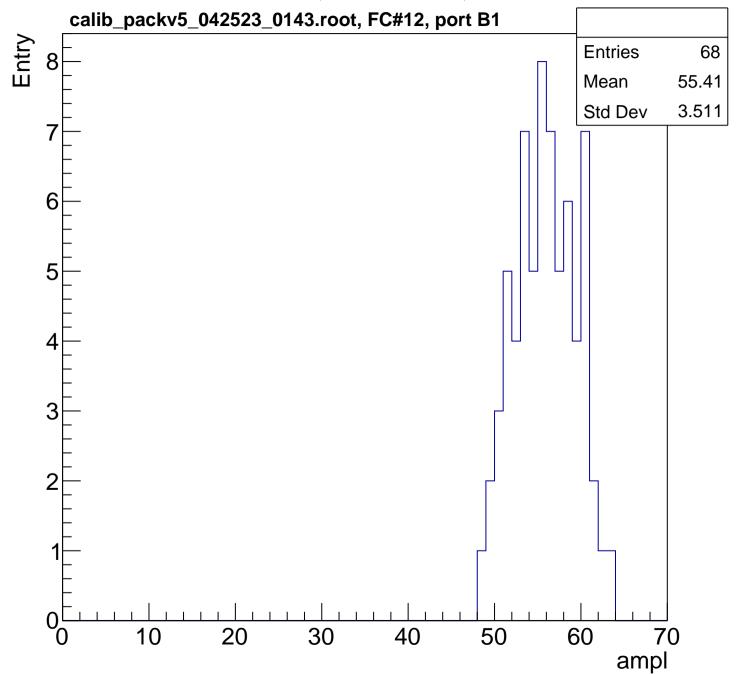


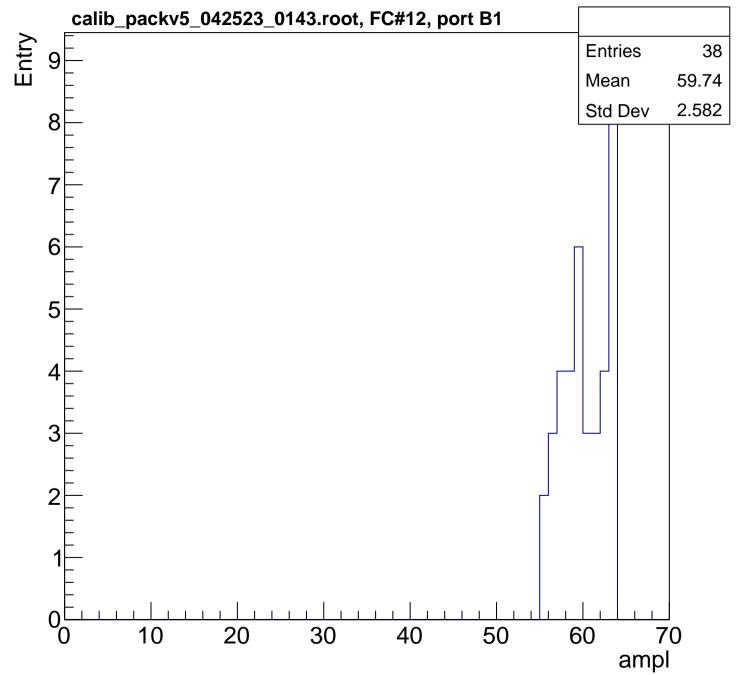


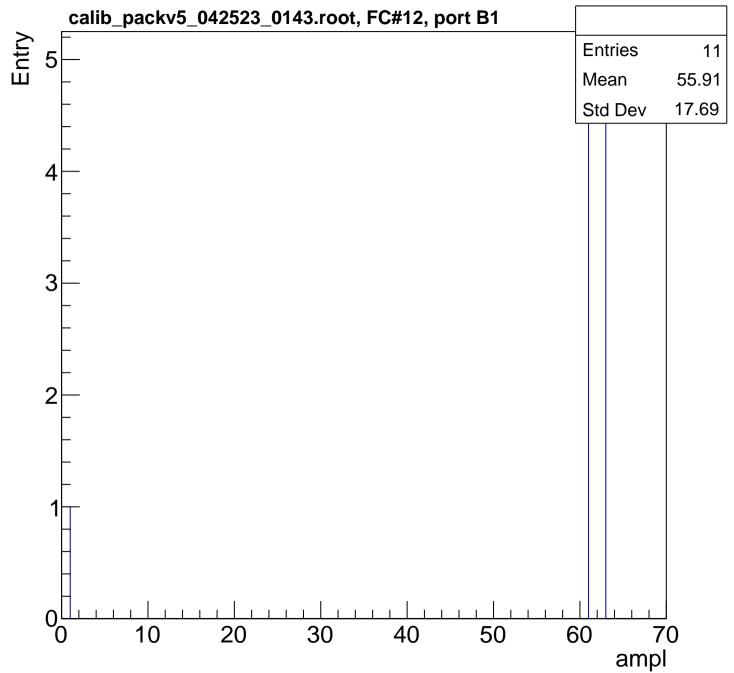




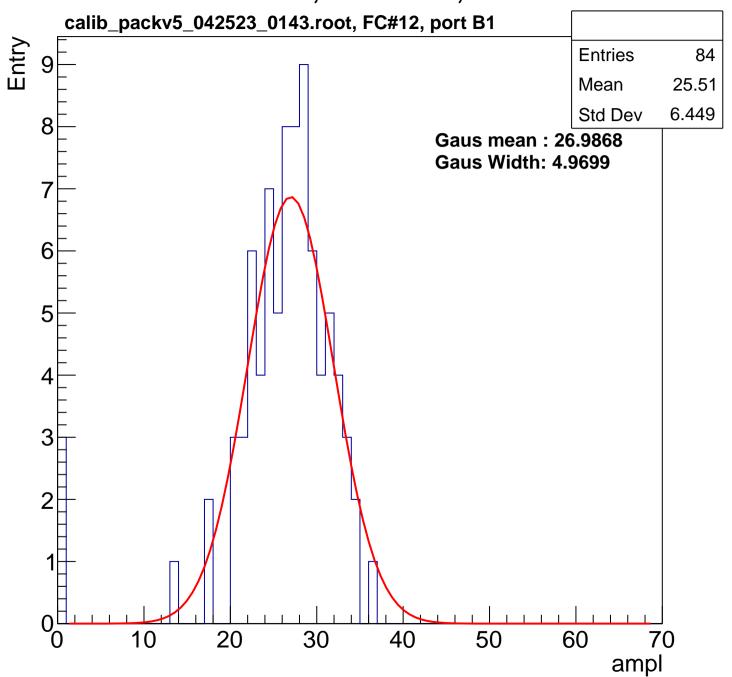


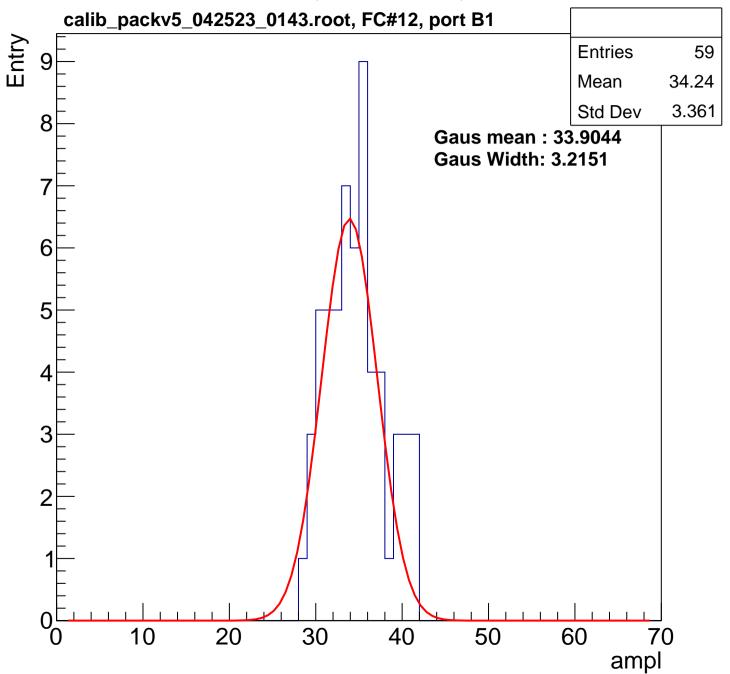


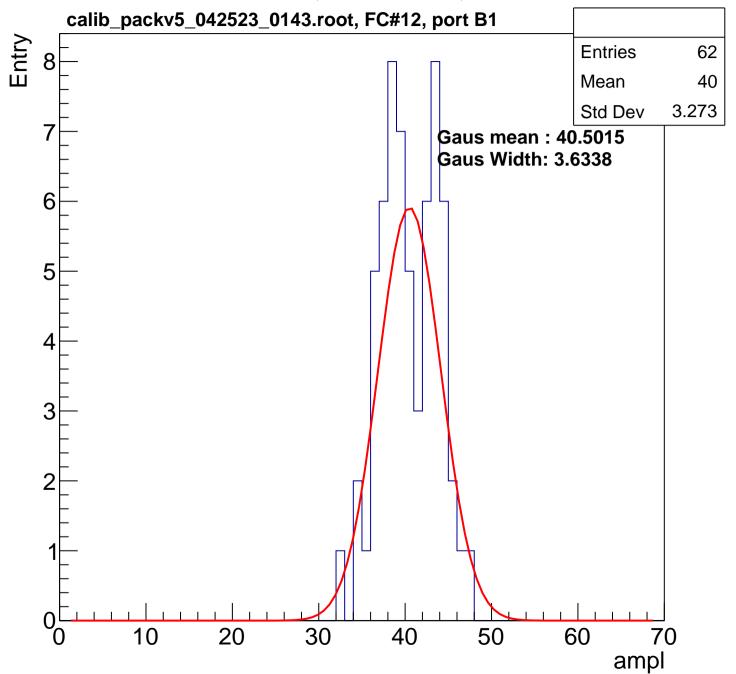


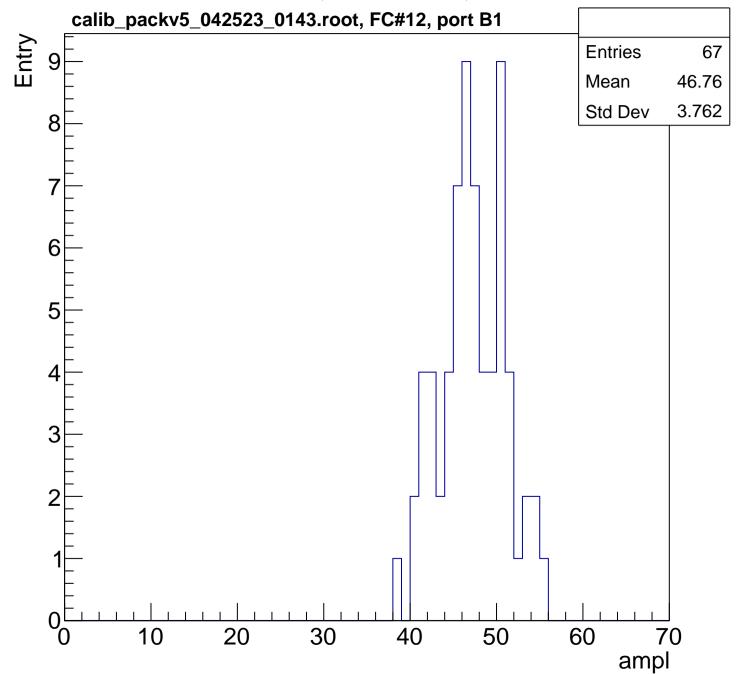


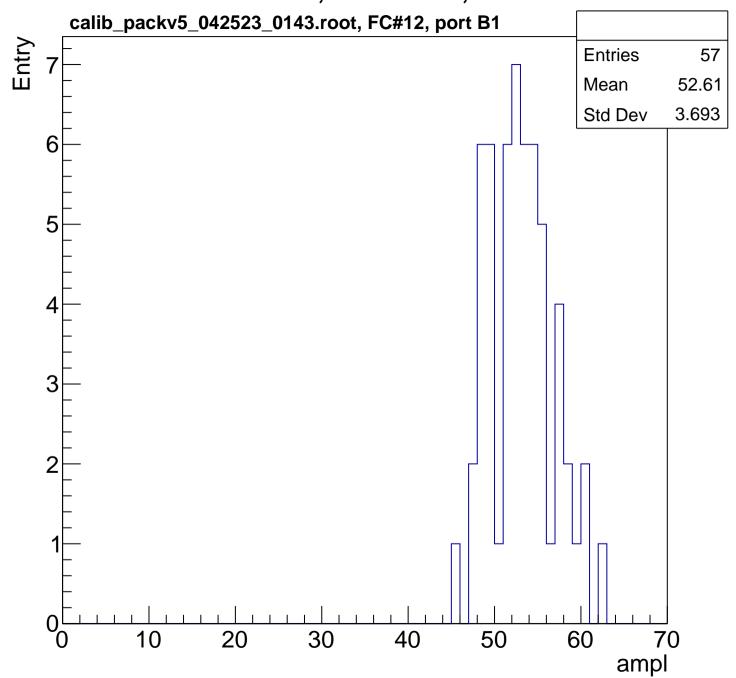
B0L102S, U3-ch93, adc7 calib_packv5_042523_0143.root, FC#12, port B1 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

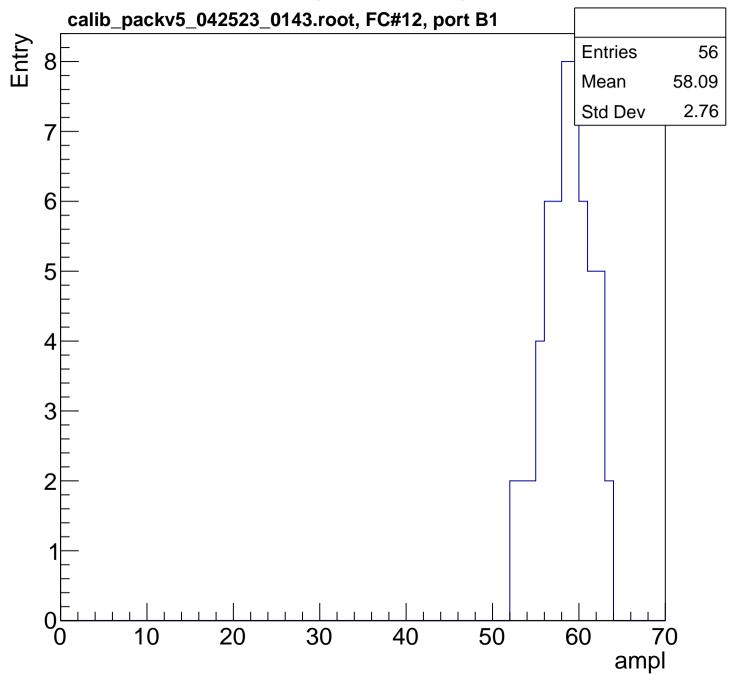


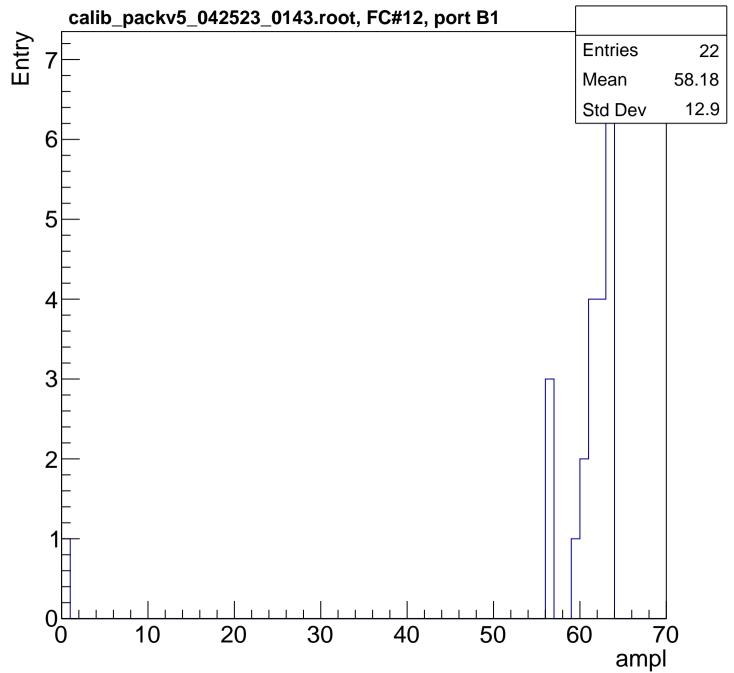


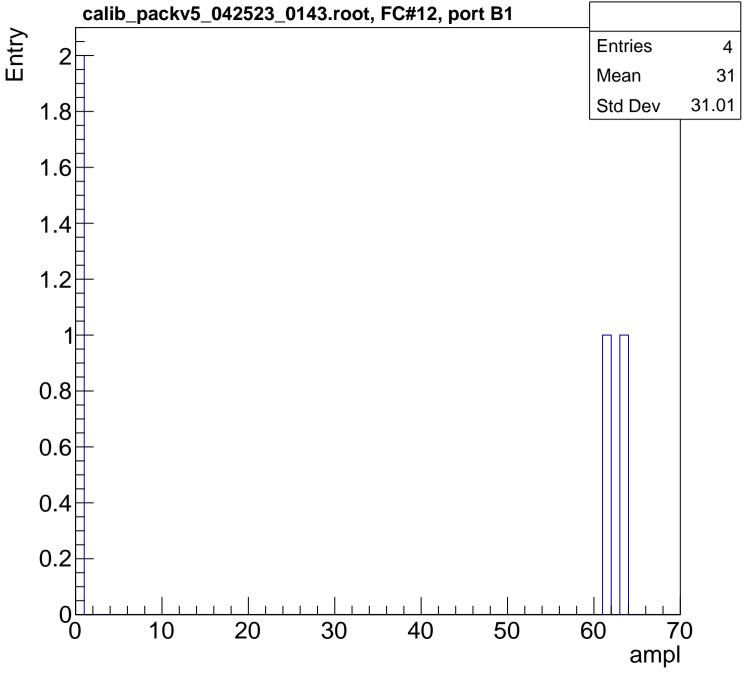


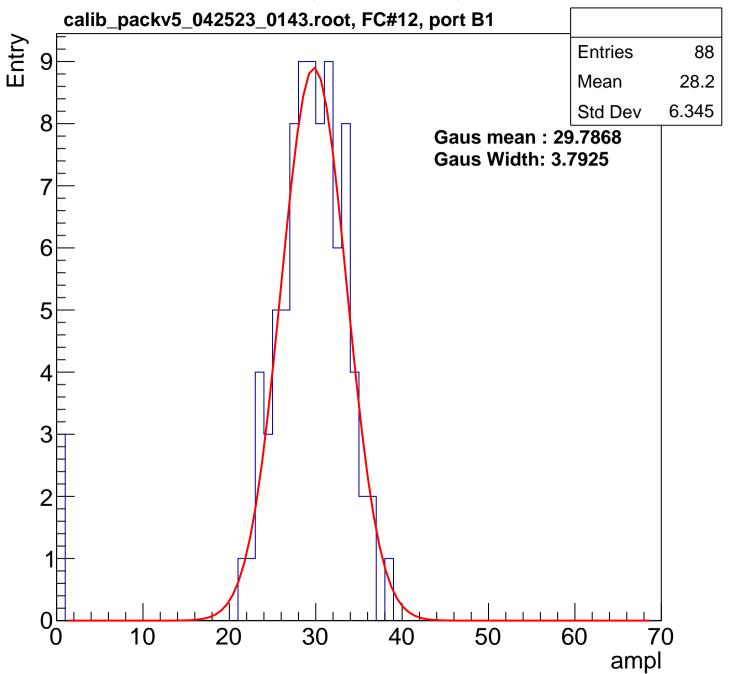


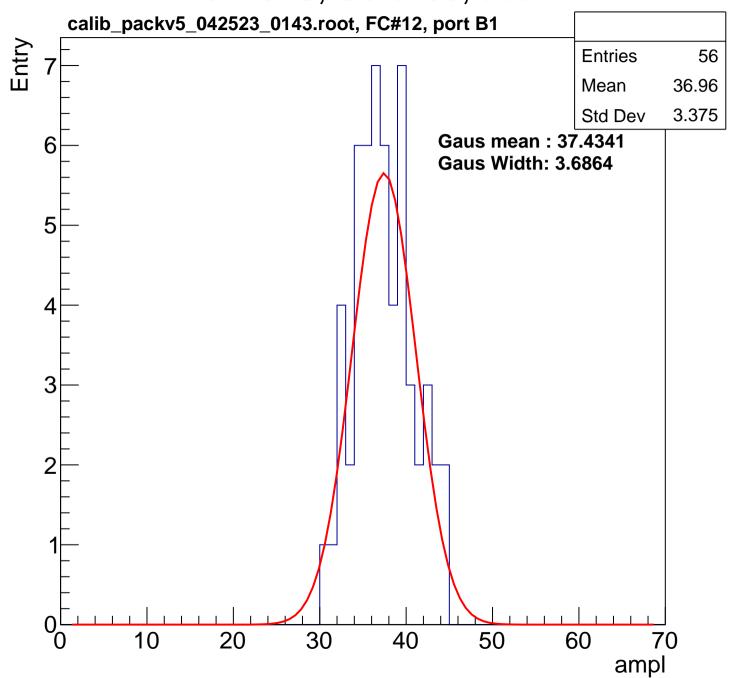


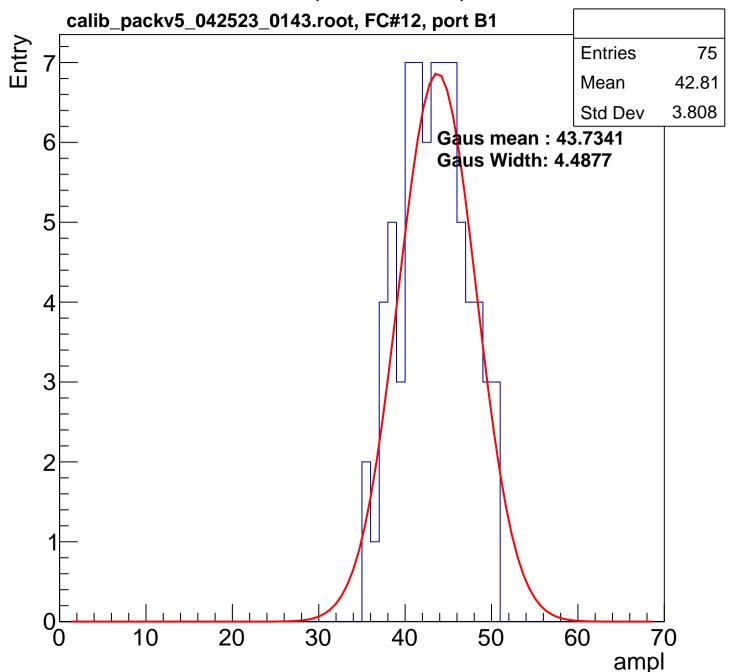


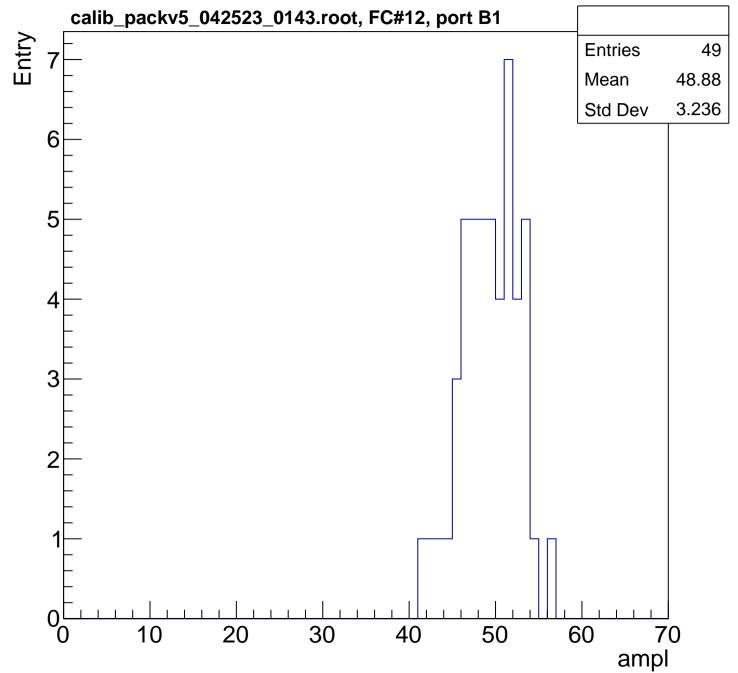


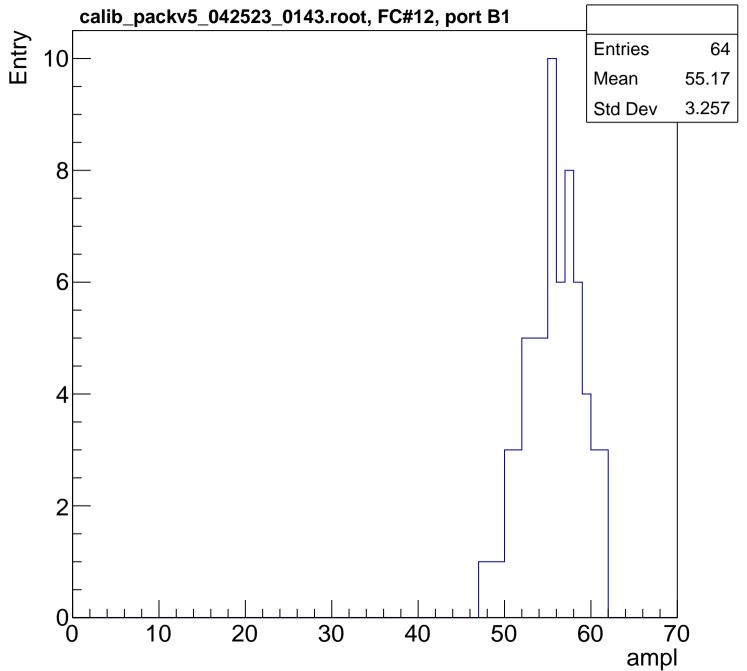


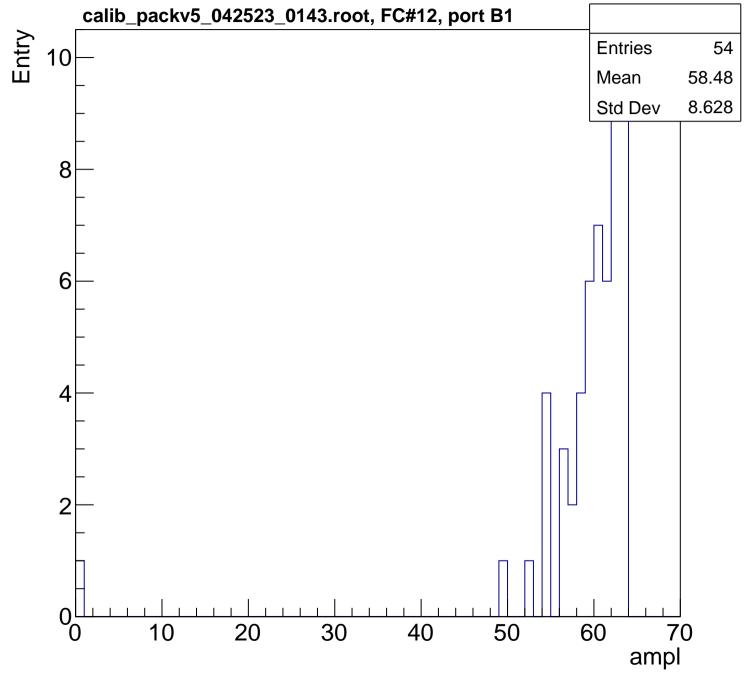


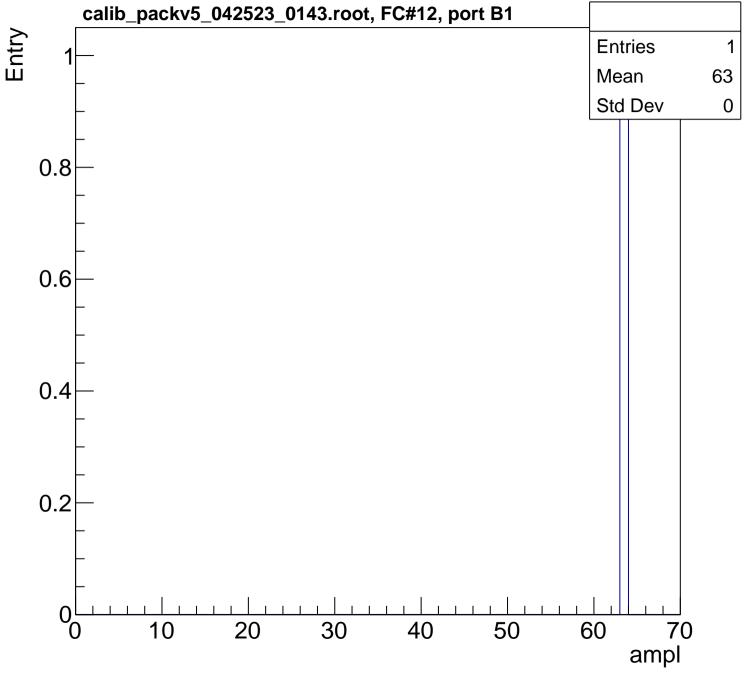




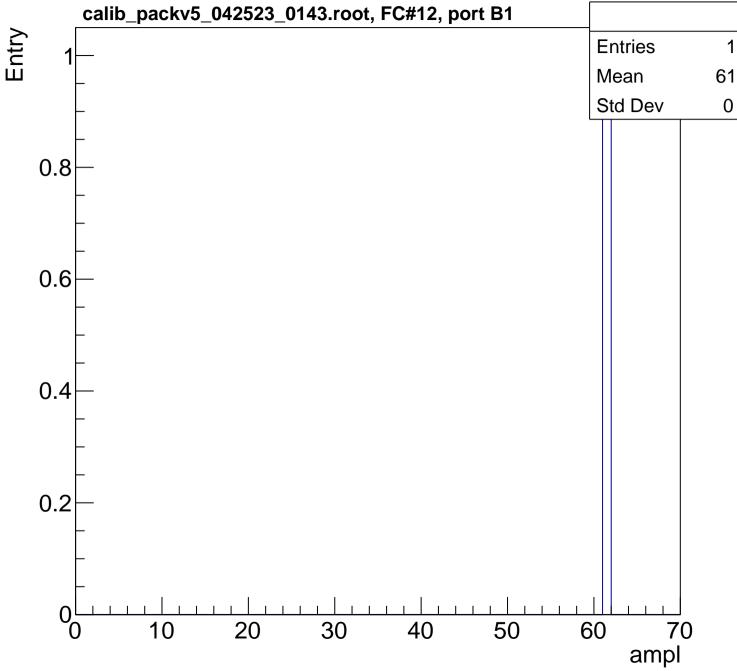


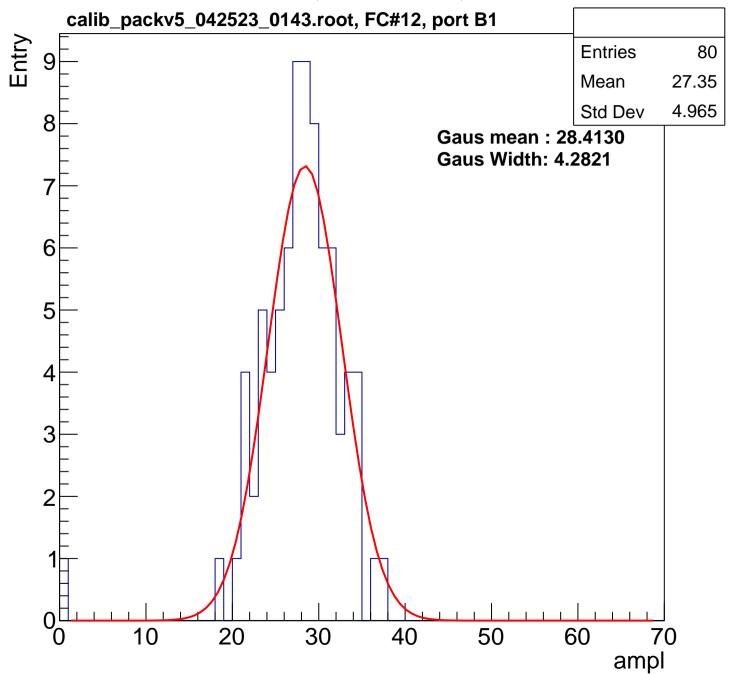


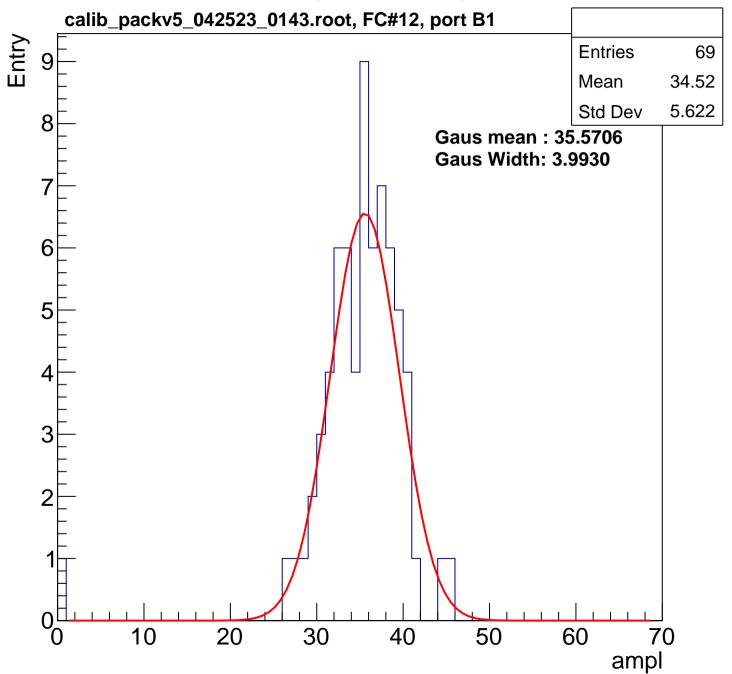


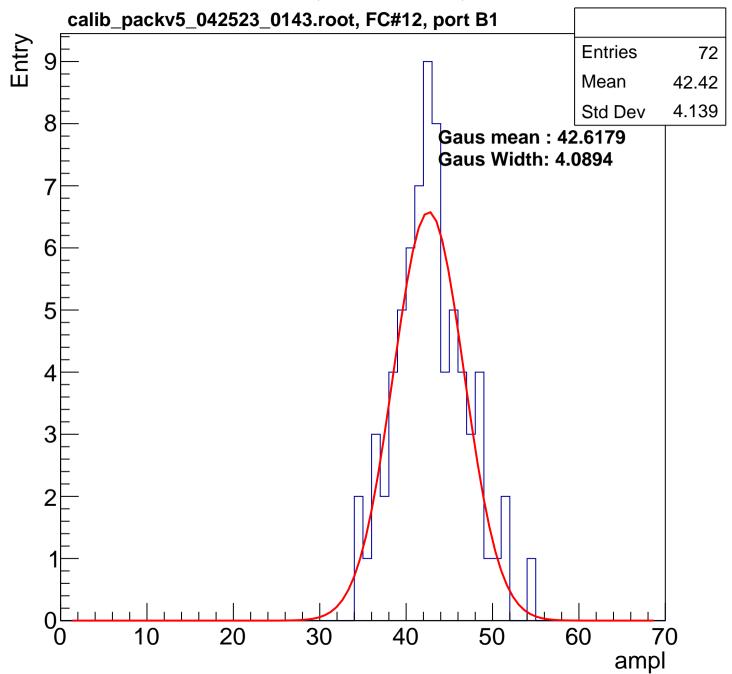


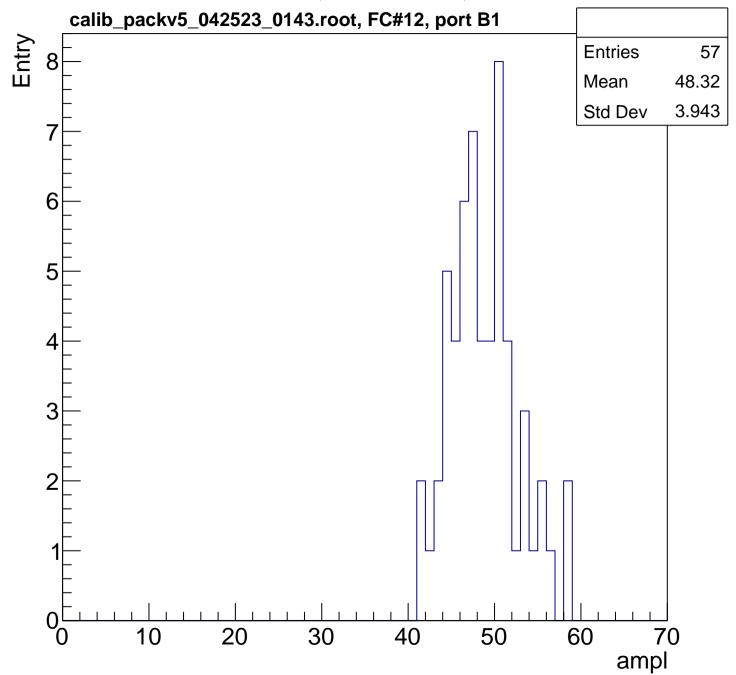
1

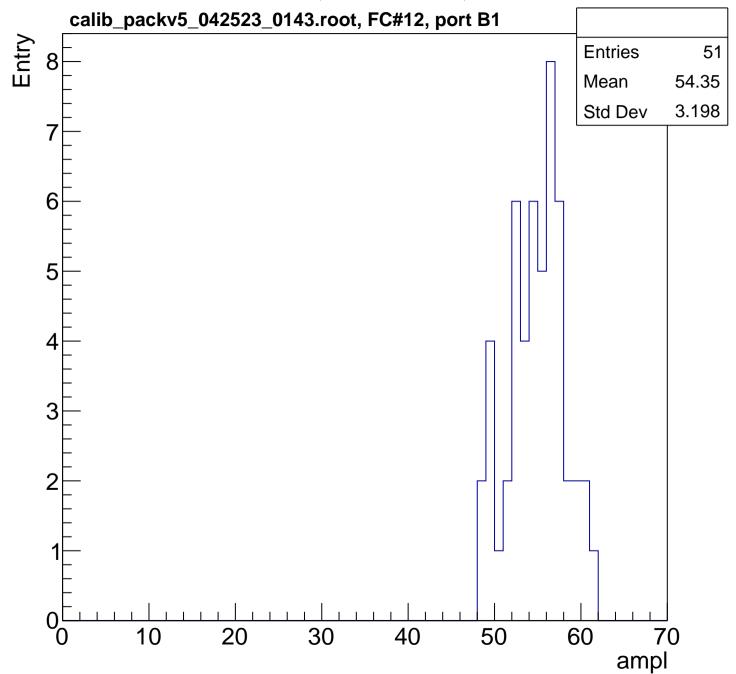


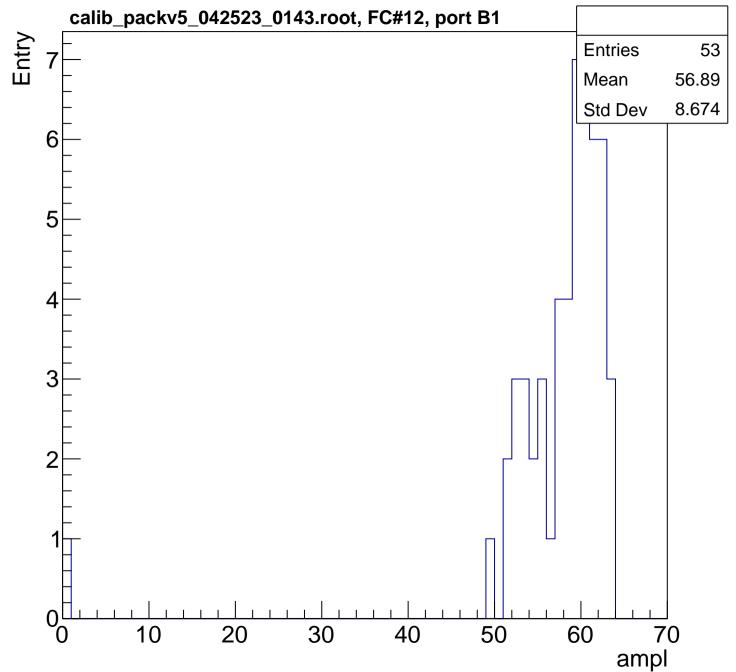


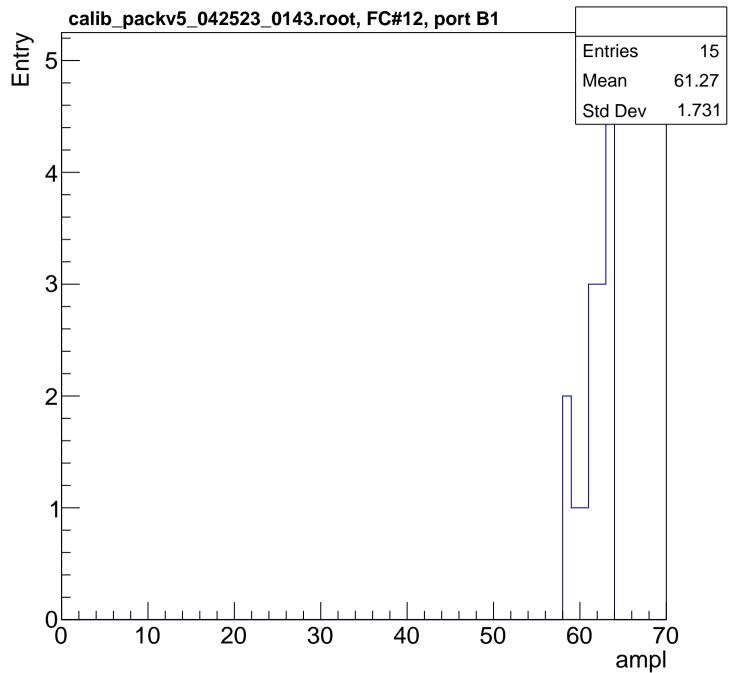


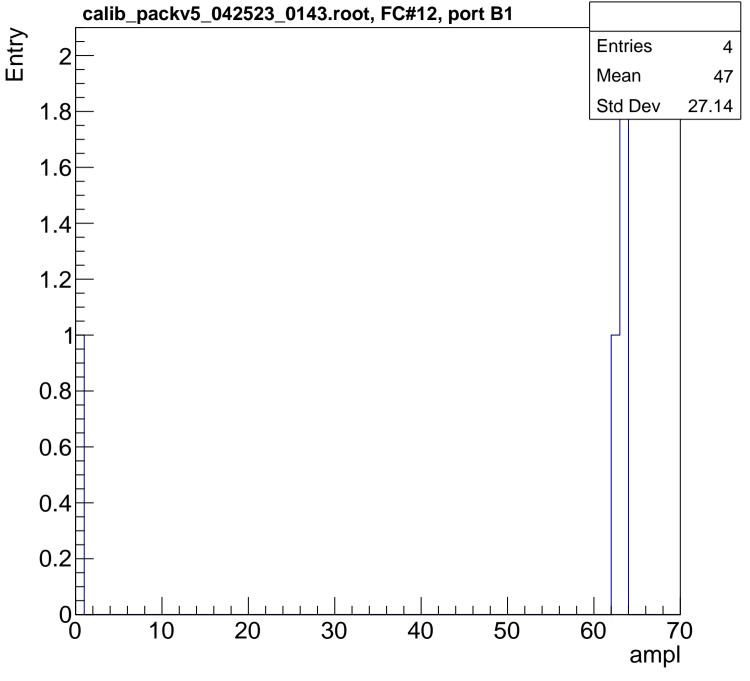


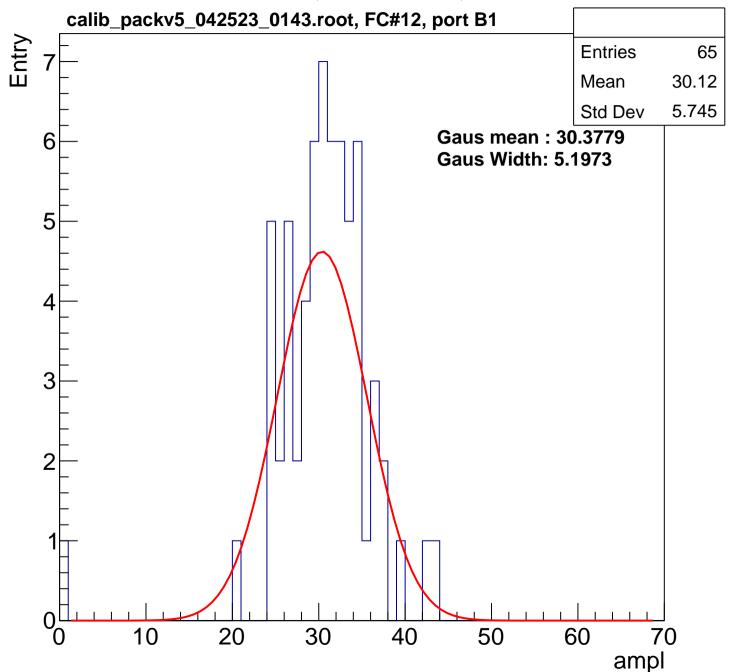


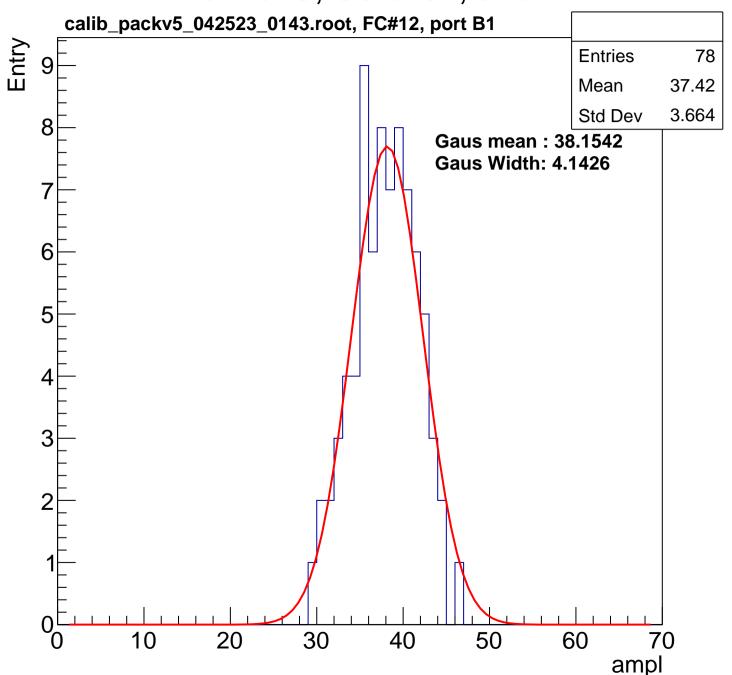


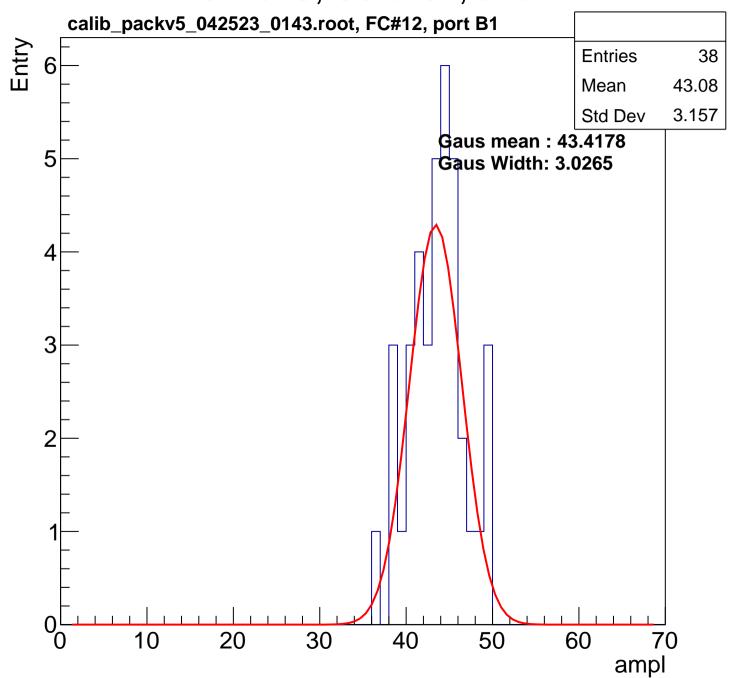


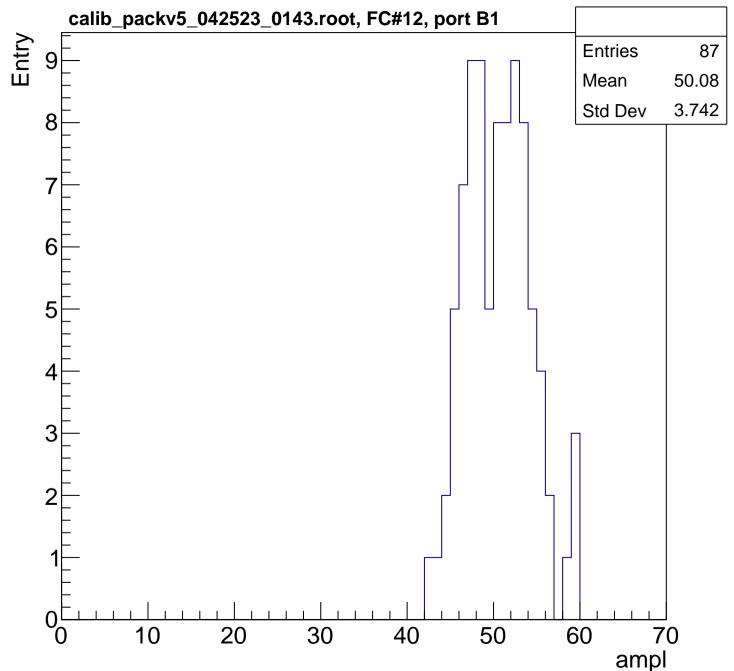


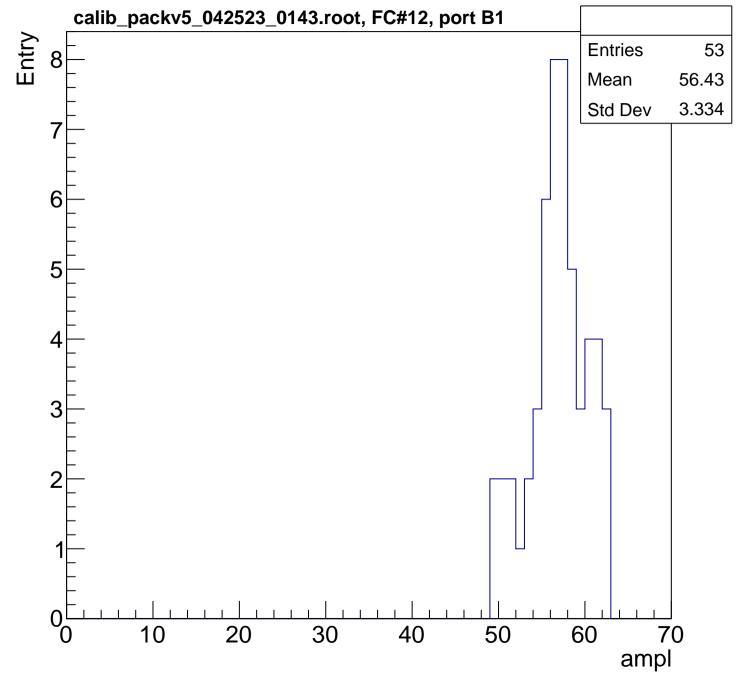


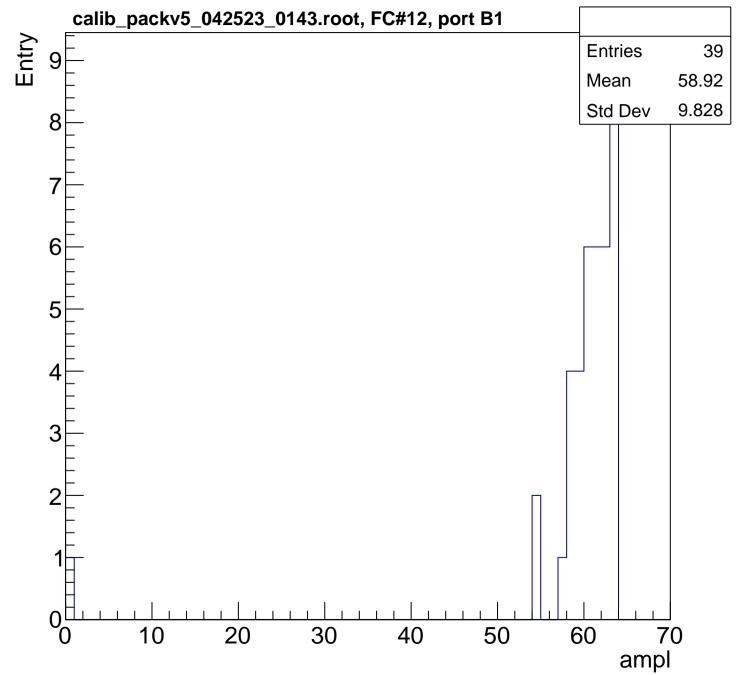


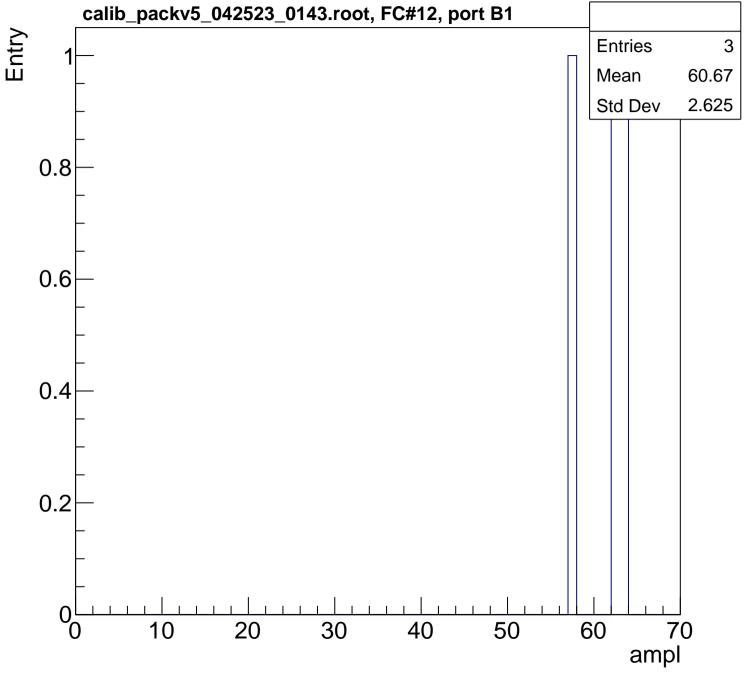




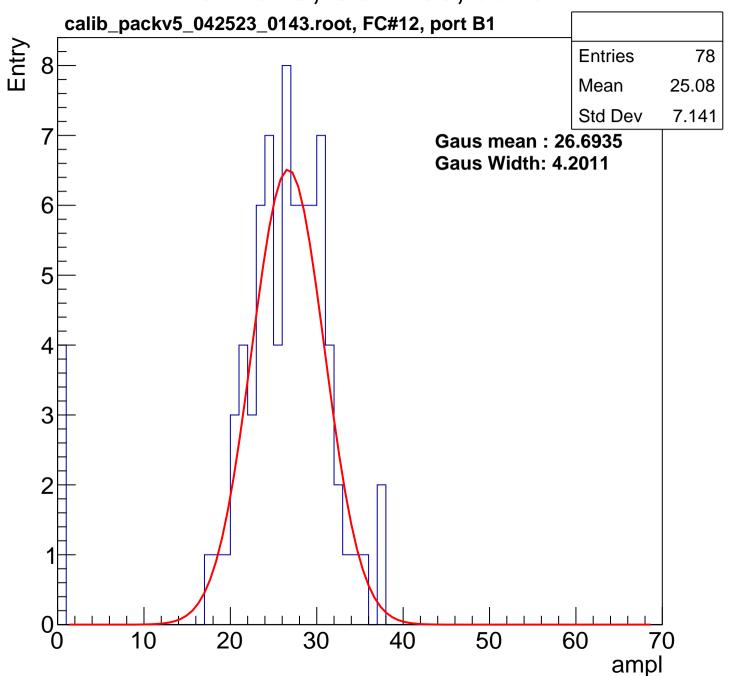


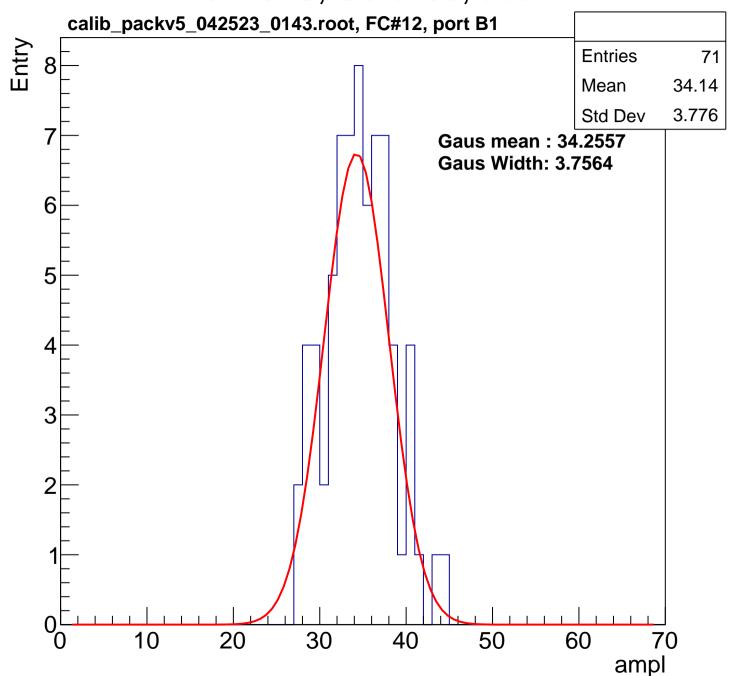


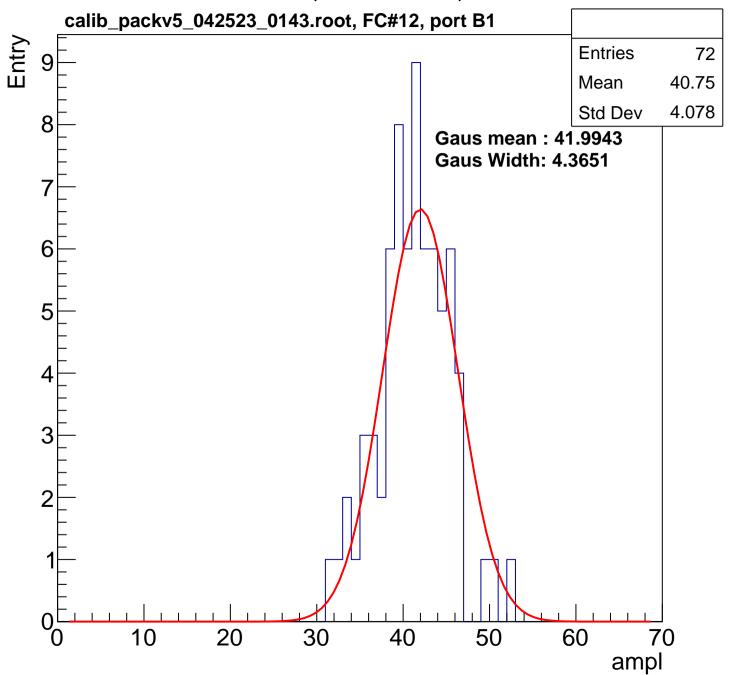


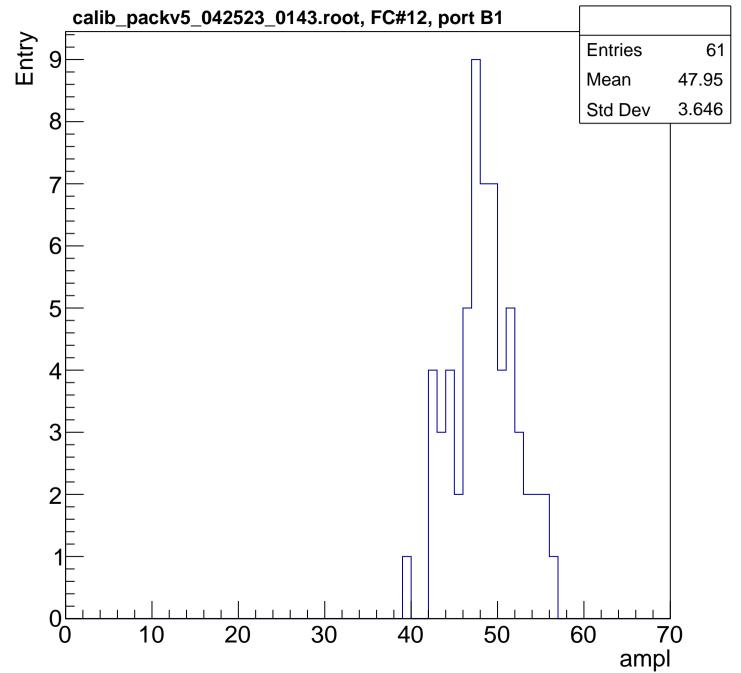


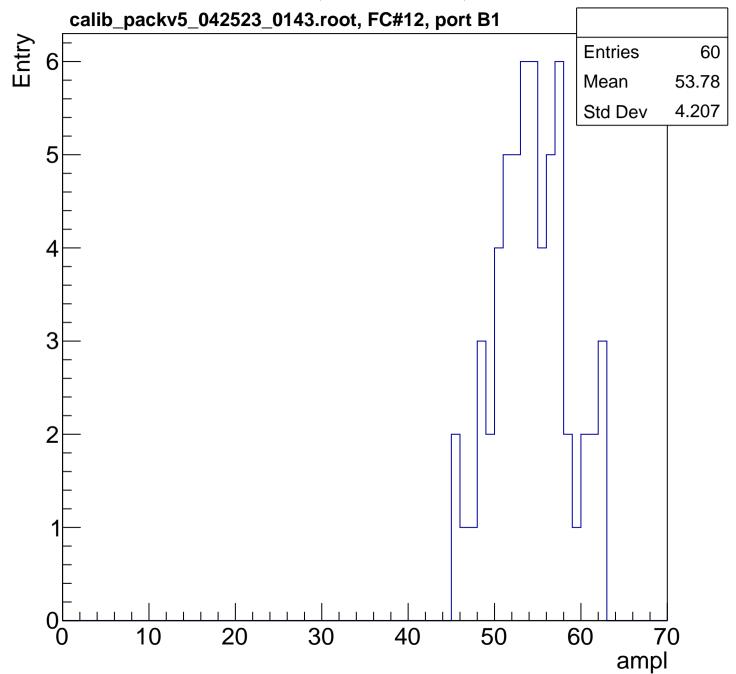
B0L102S, U3-ch97, adc7 calib_packv5_042523_0143.root, FC#12, port B1 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

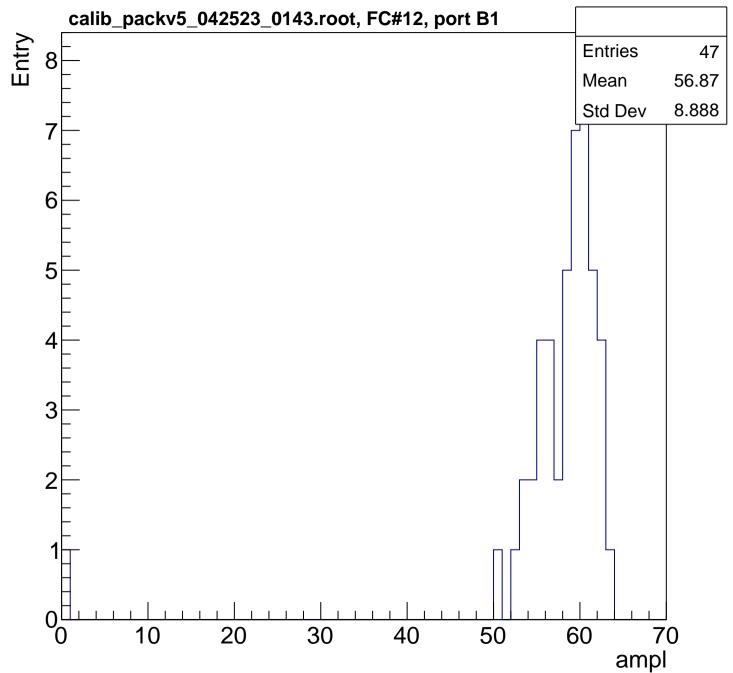


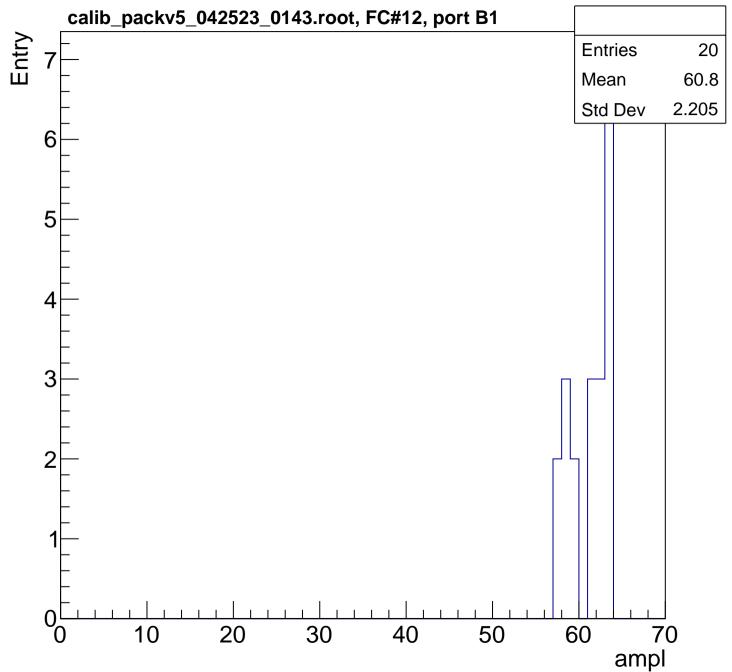


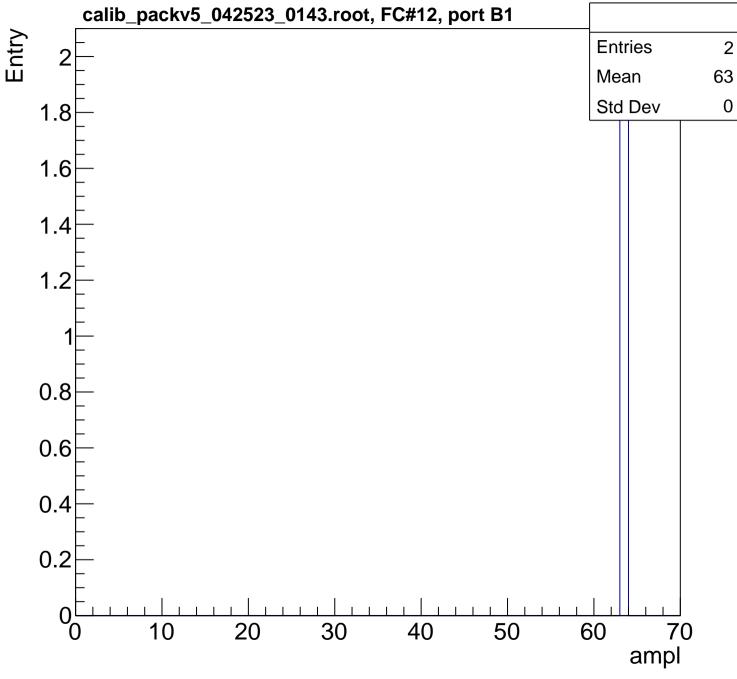


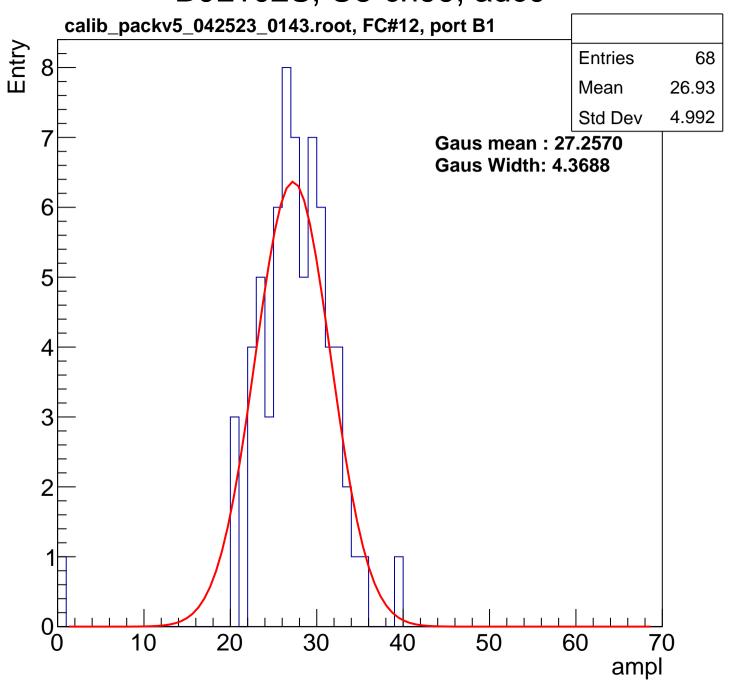


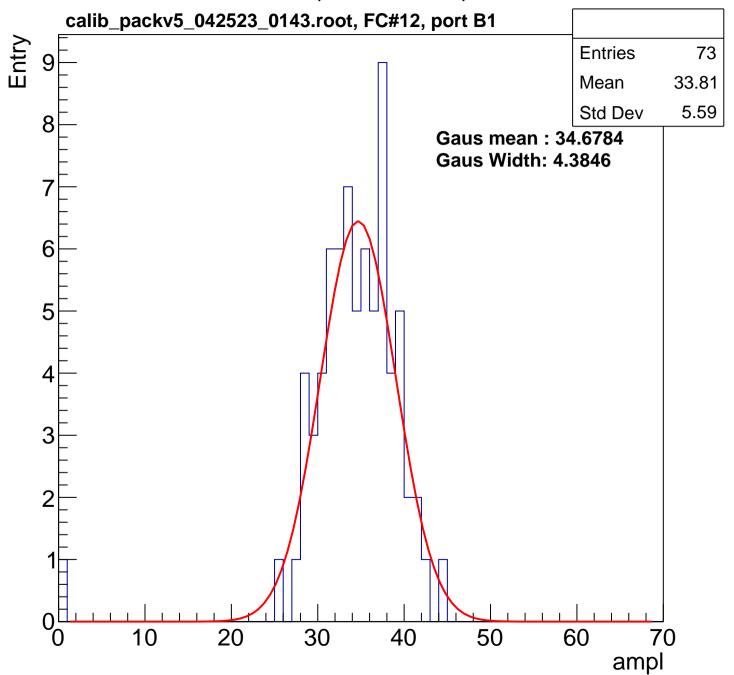


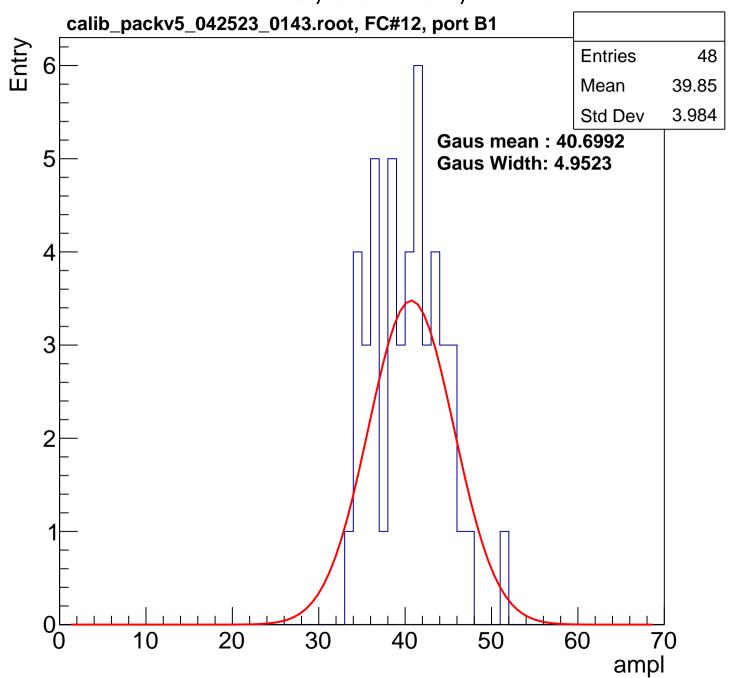


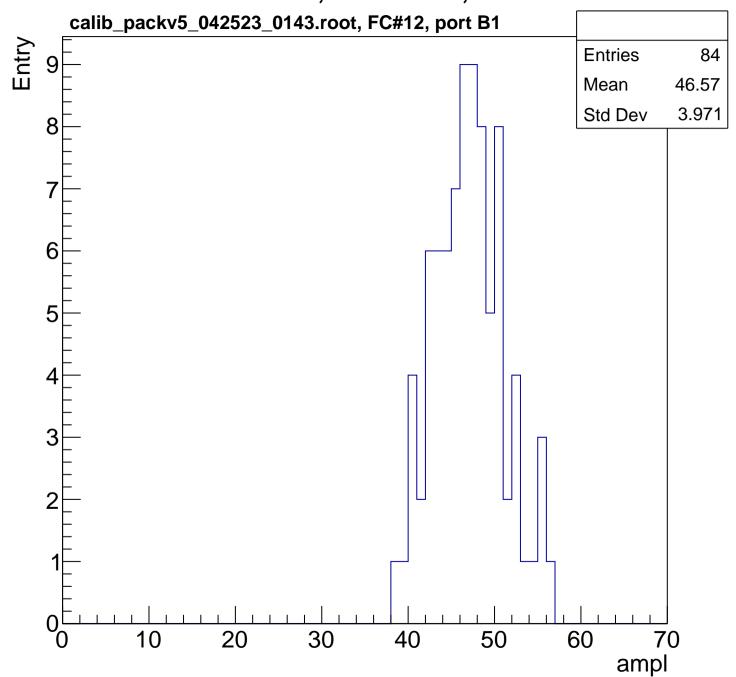


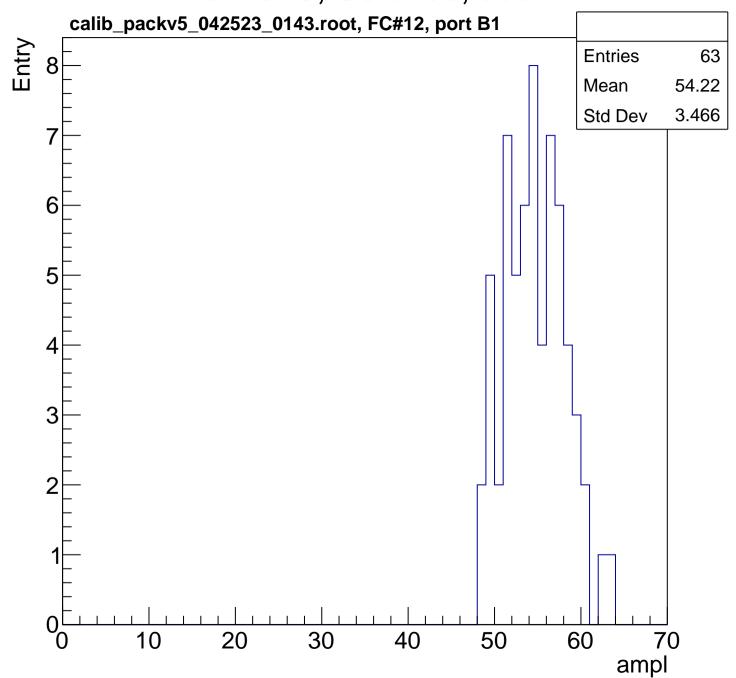


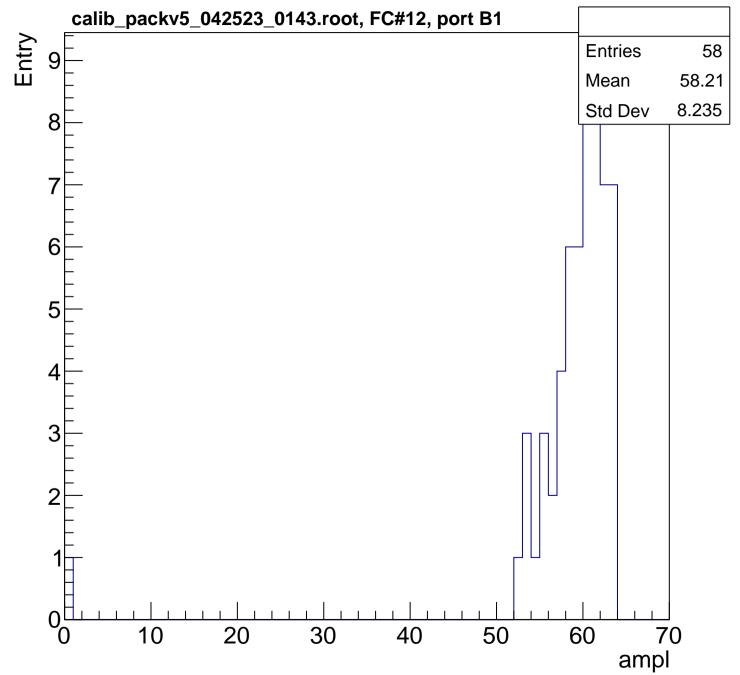


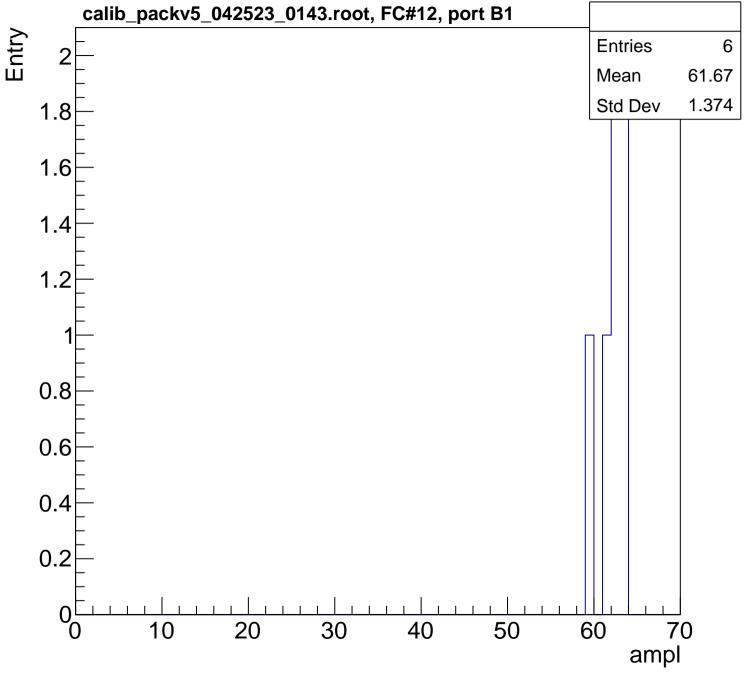


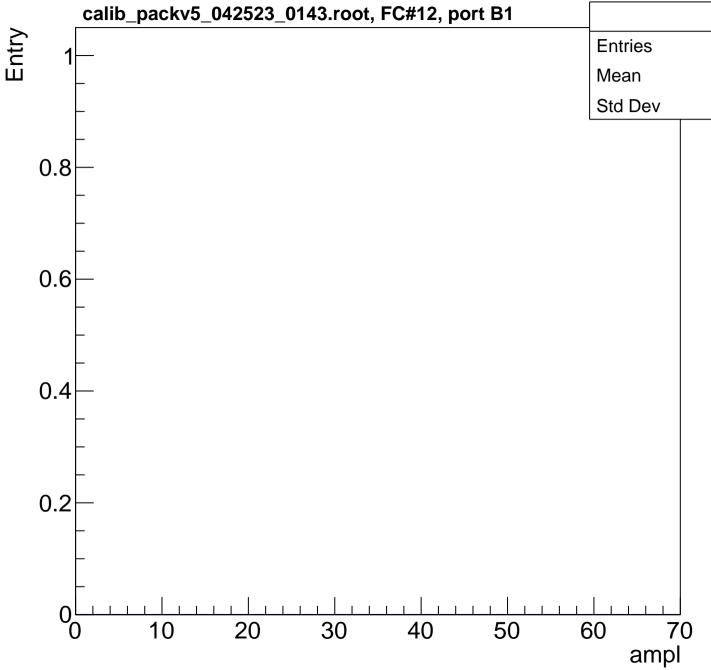


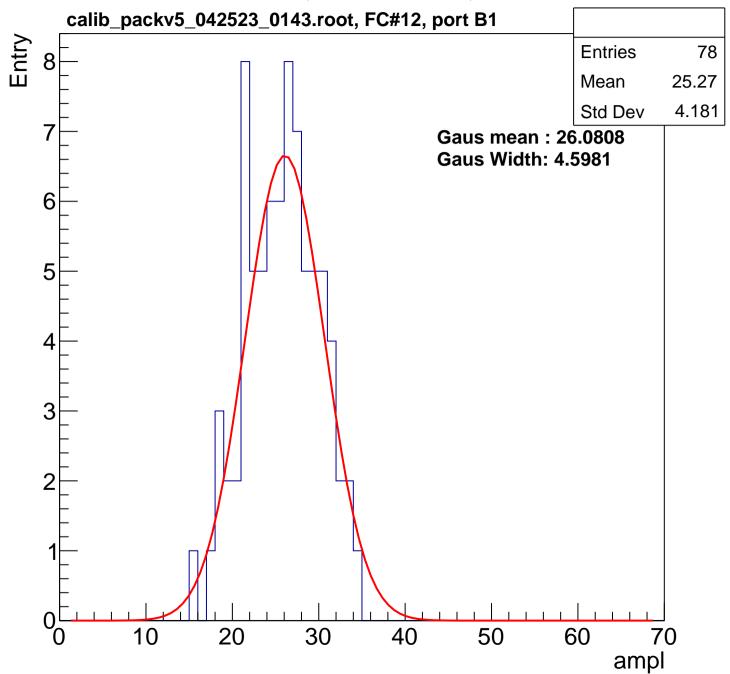


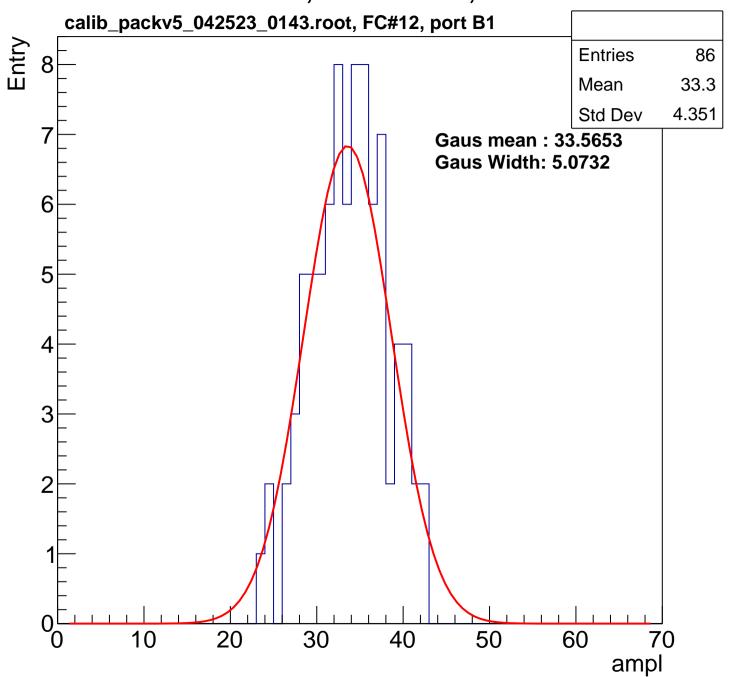


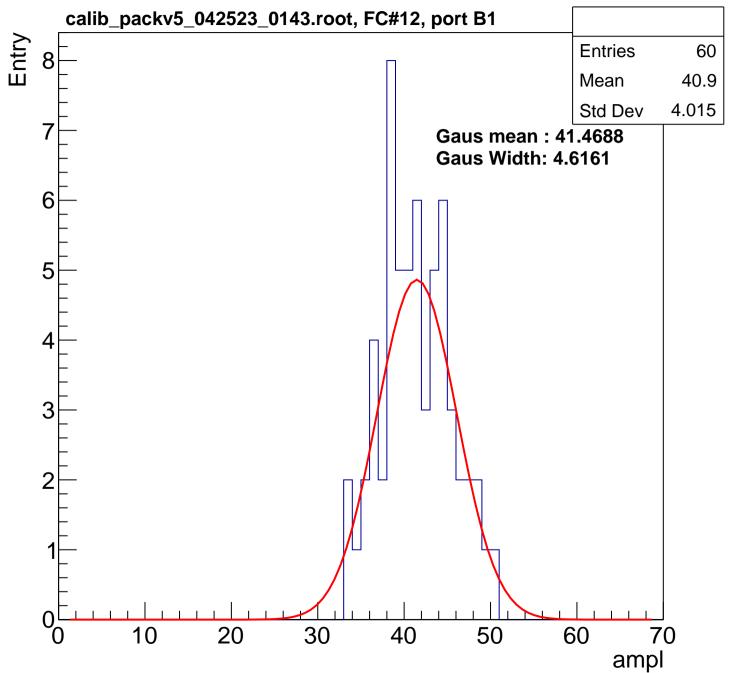


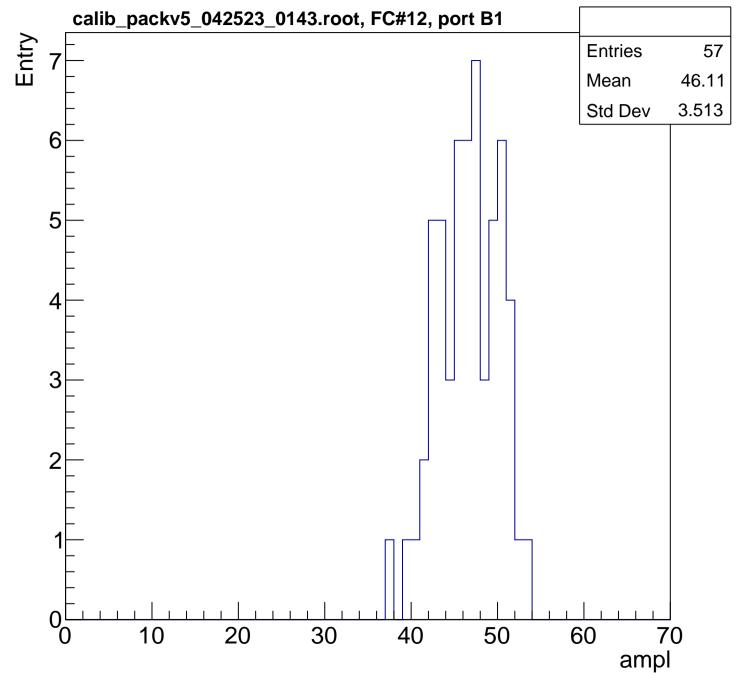


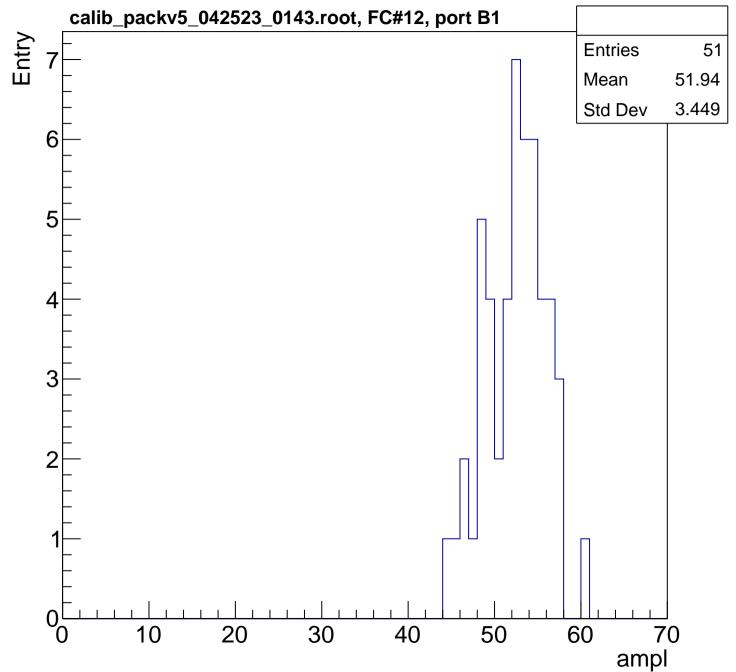


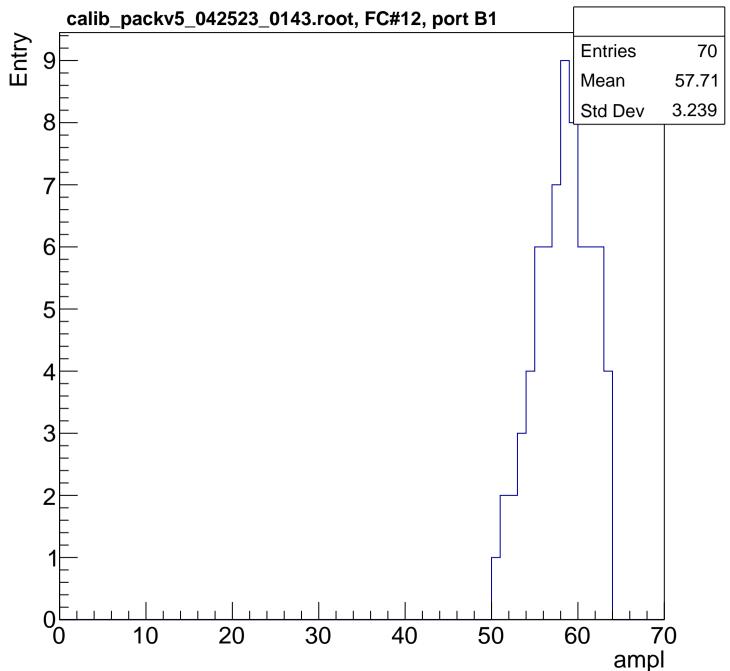


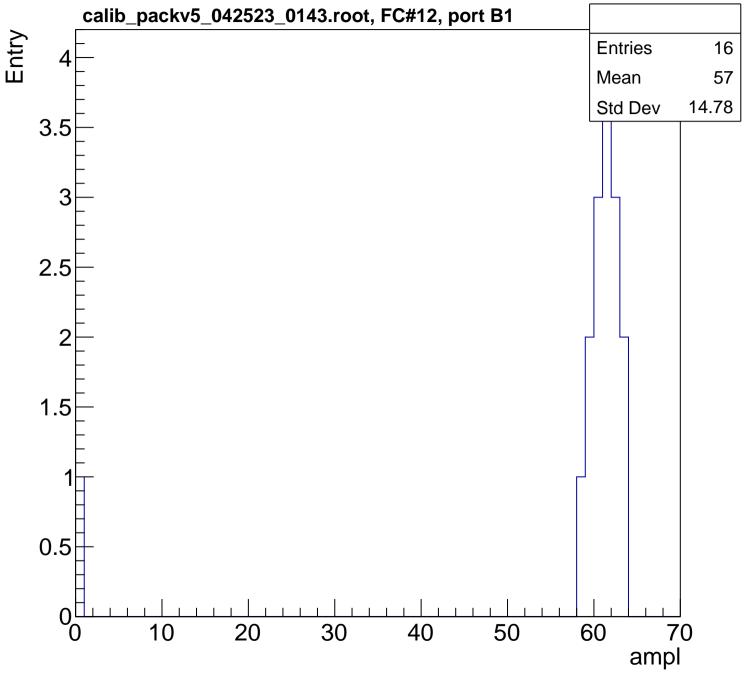


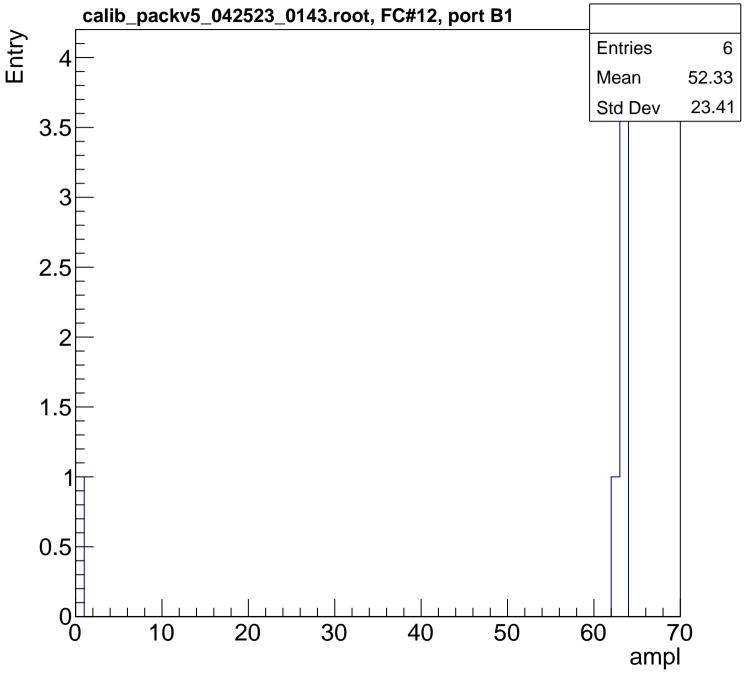


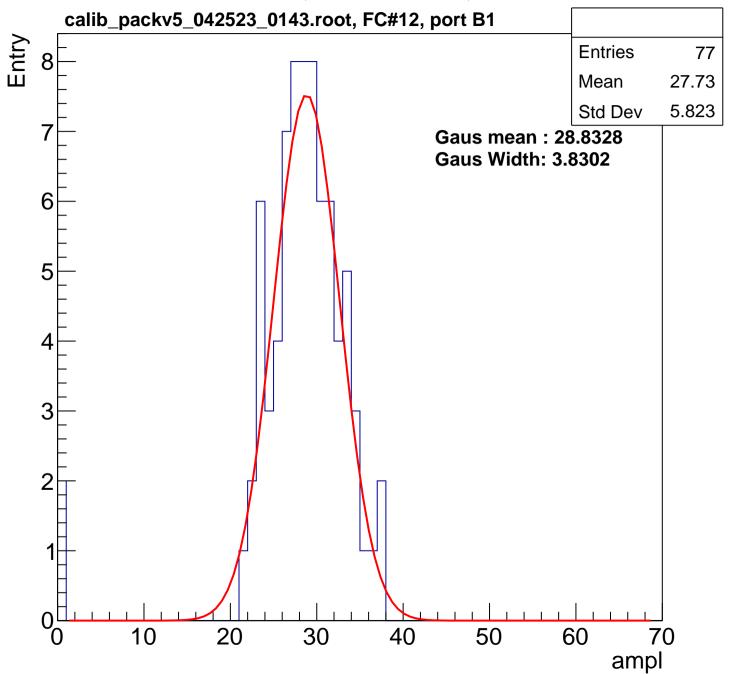


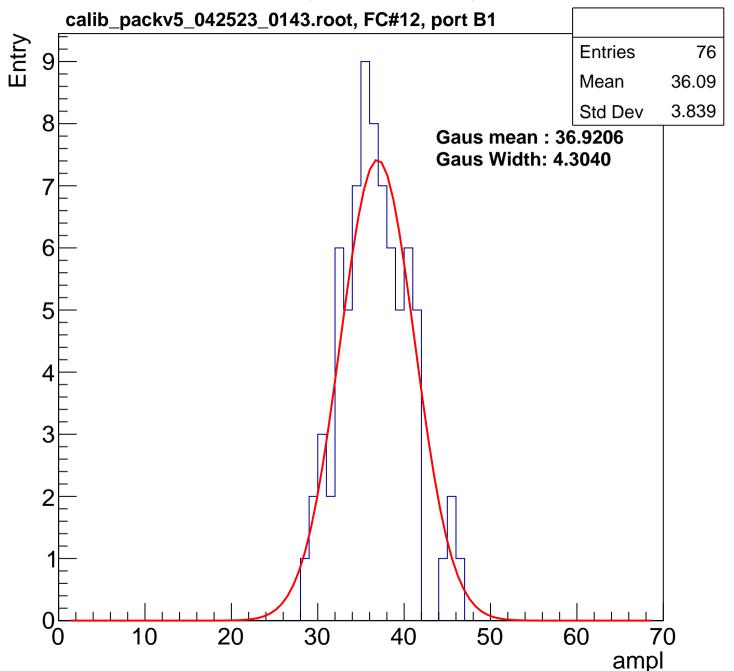


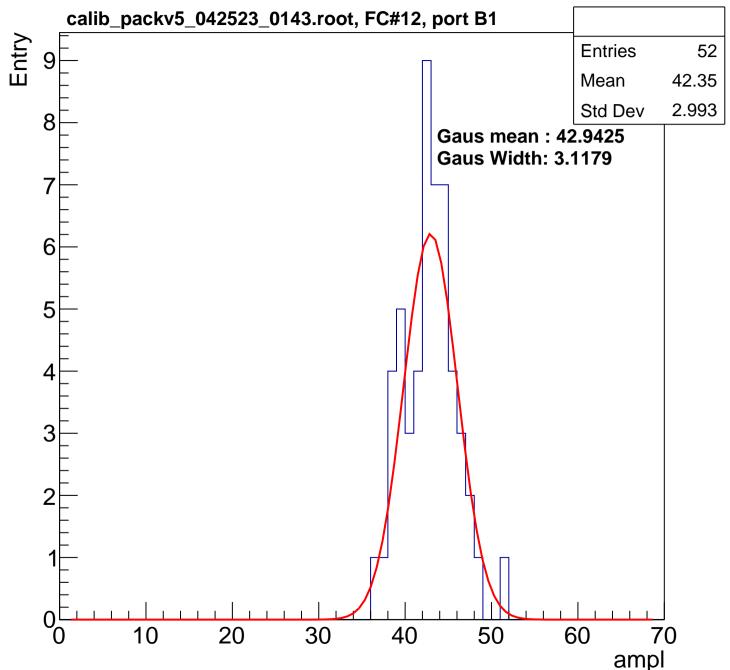


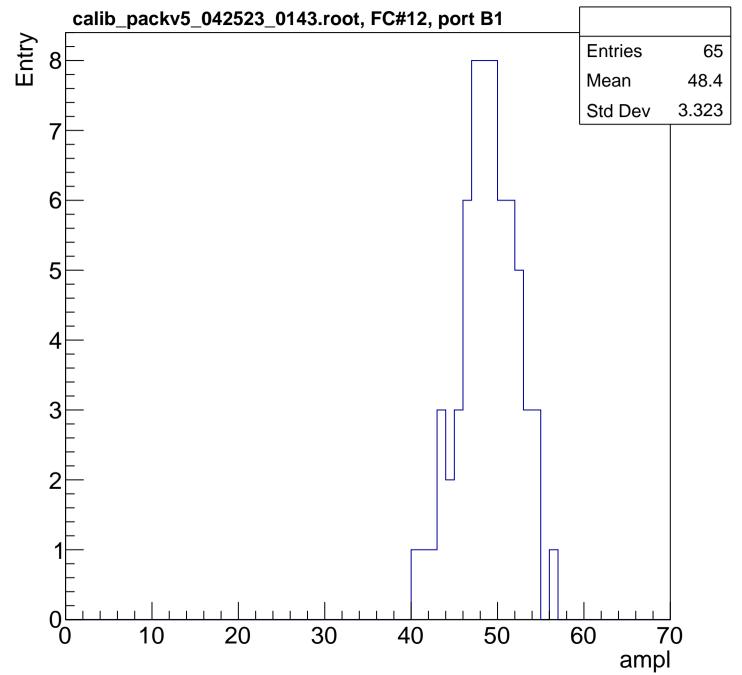


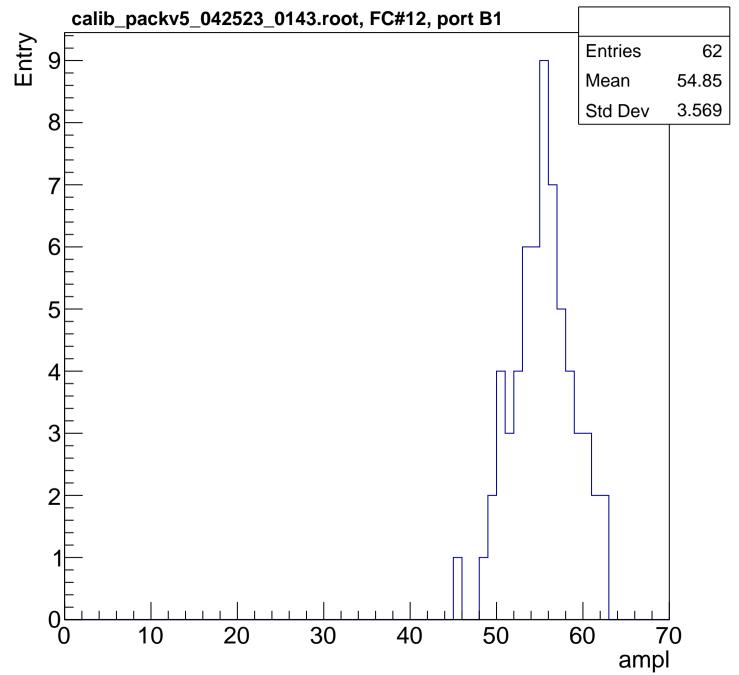


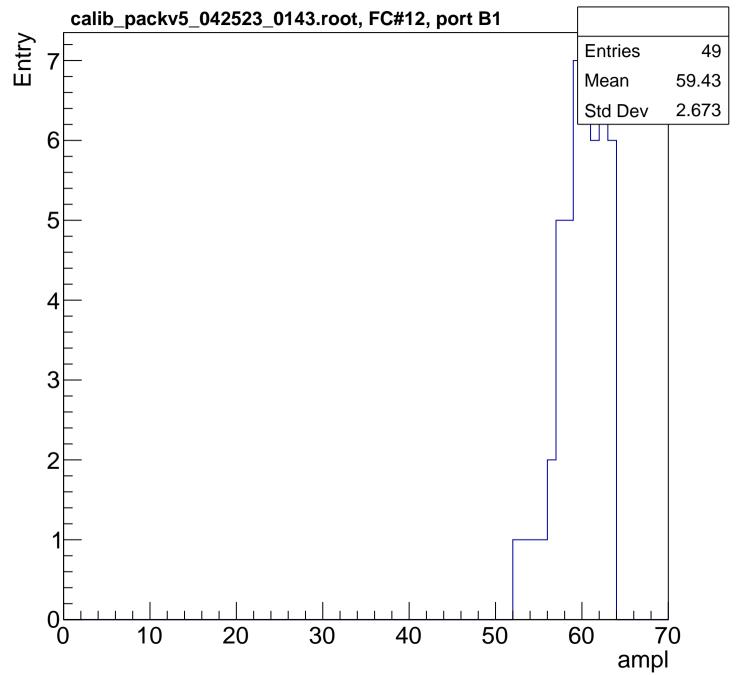


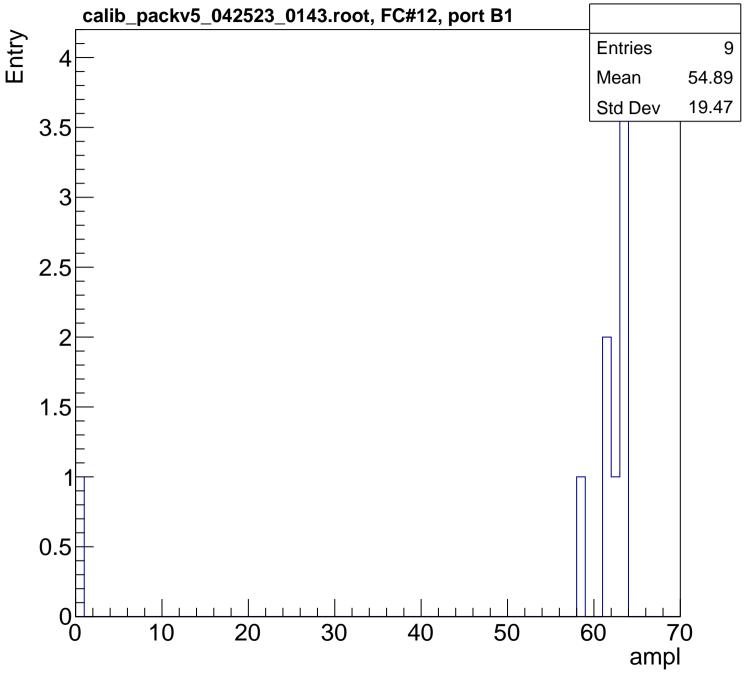


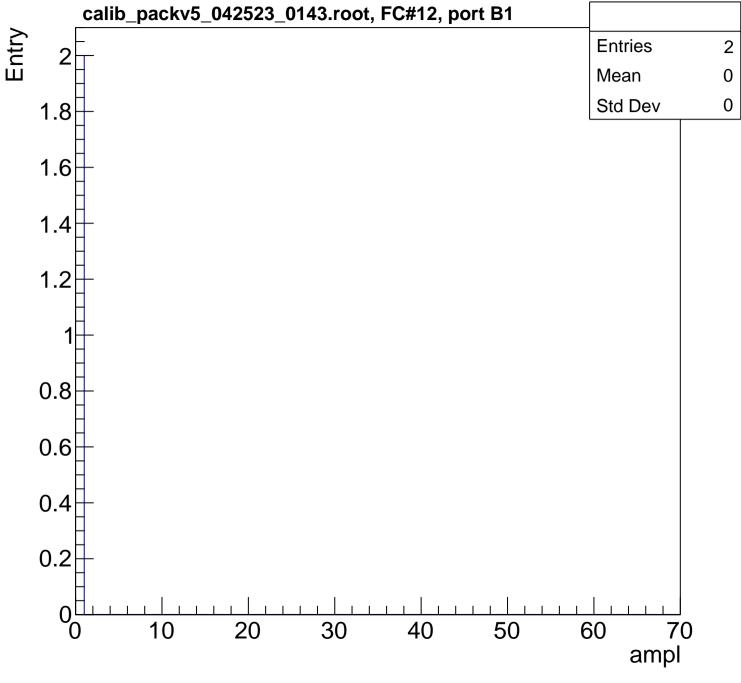


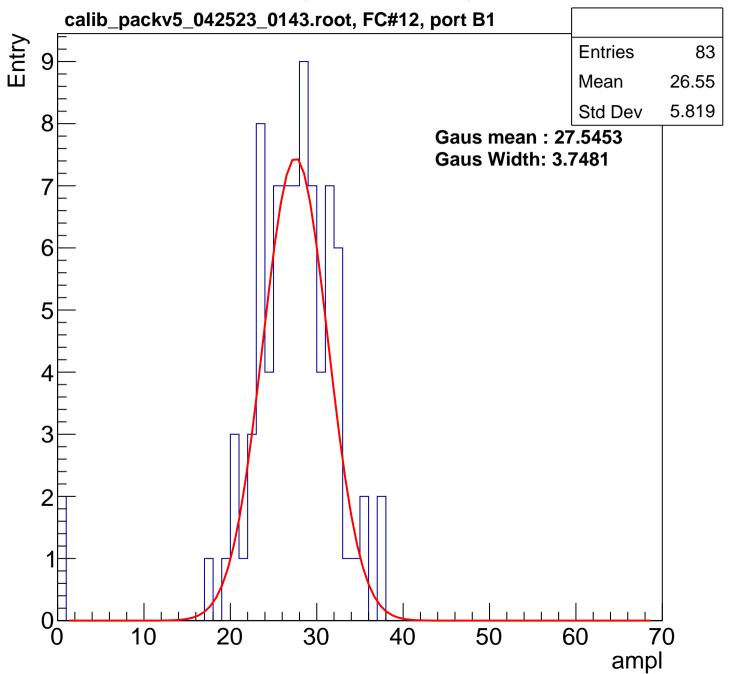


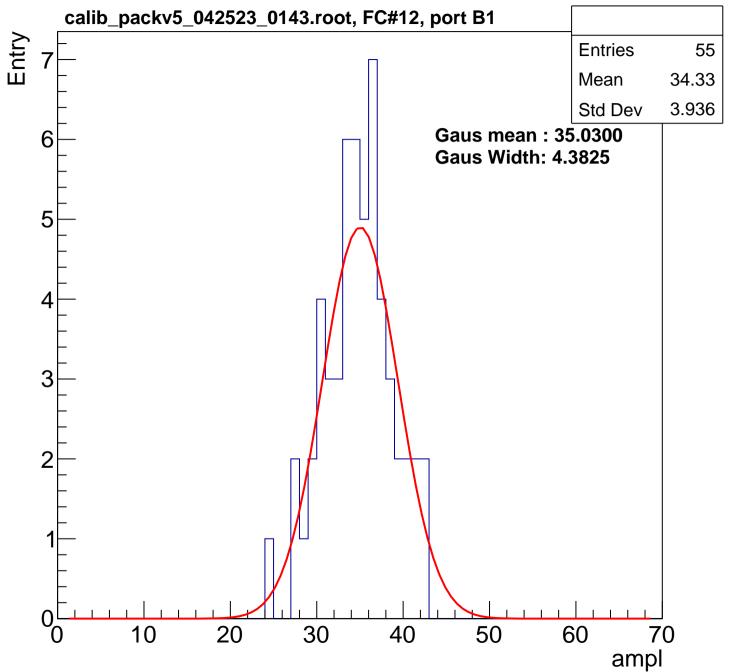


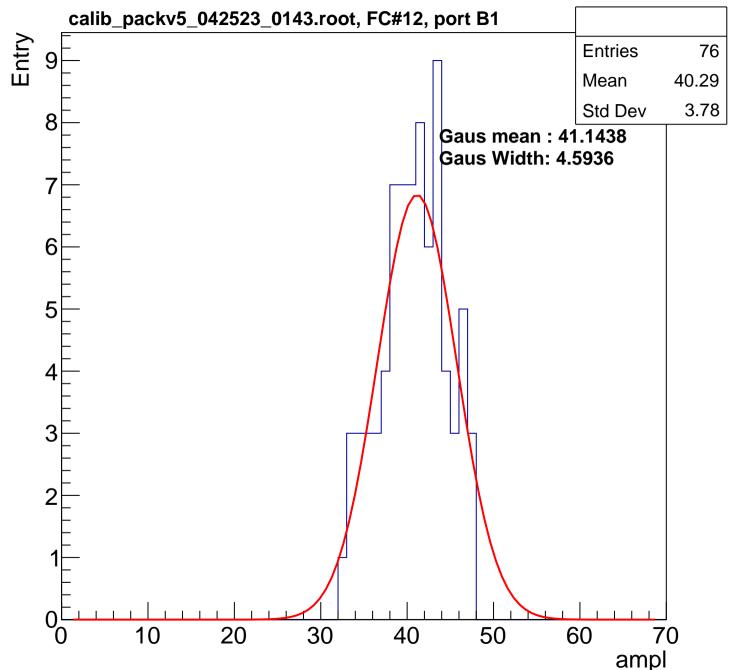


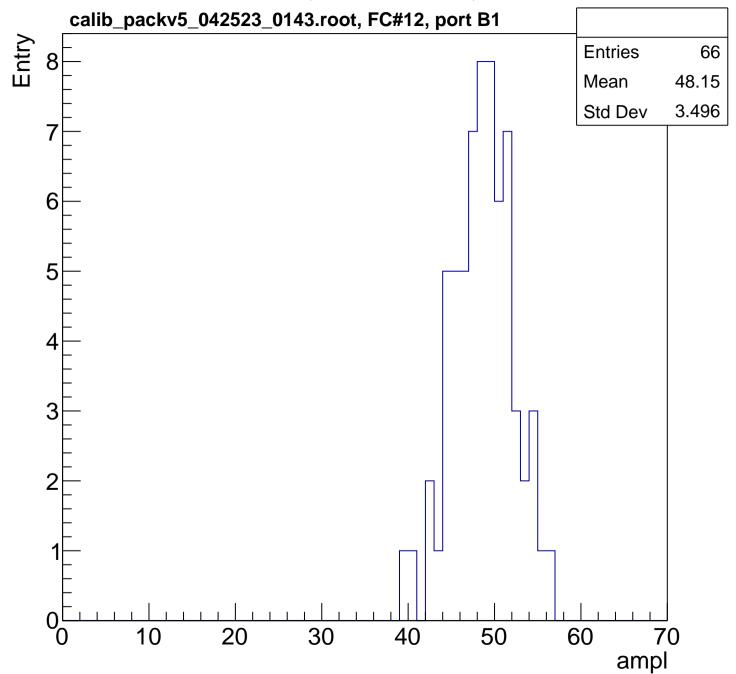


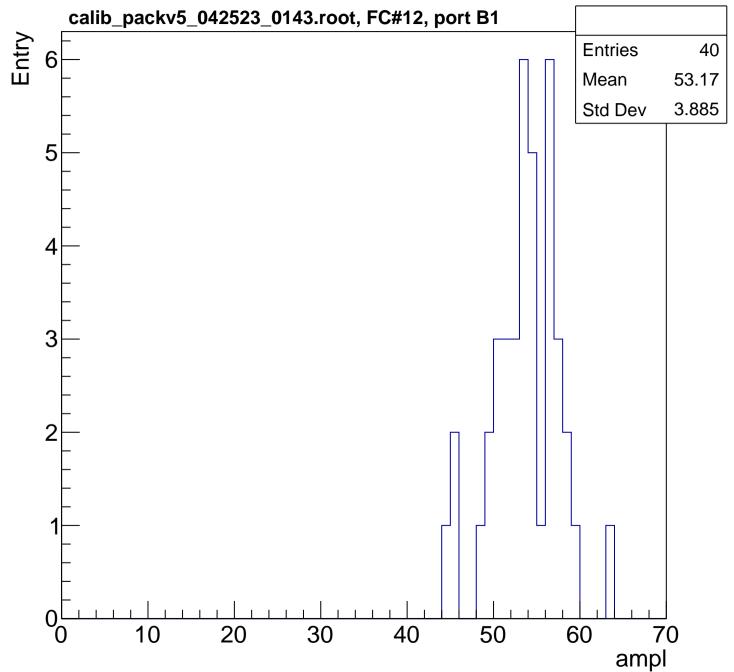


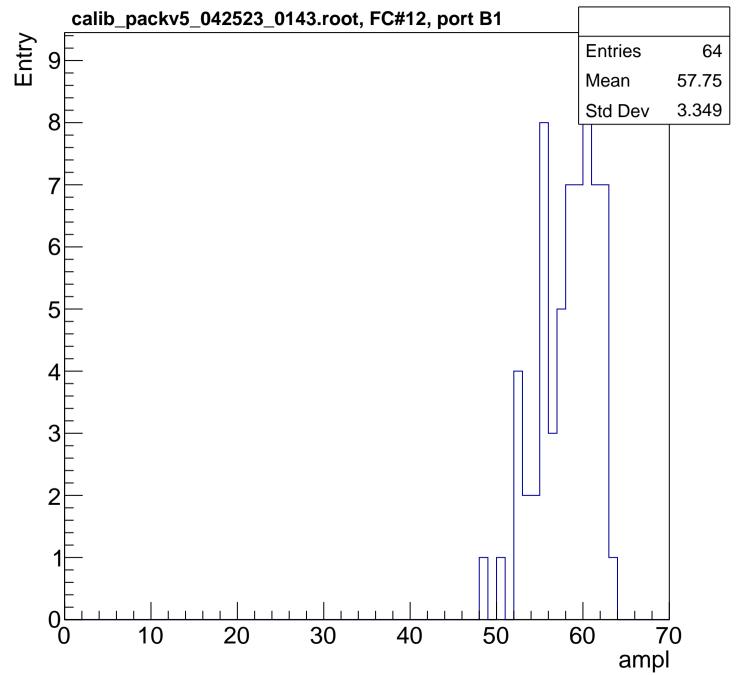


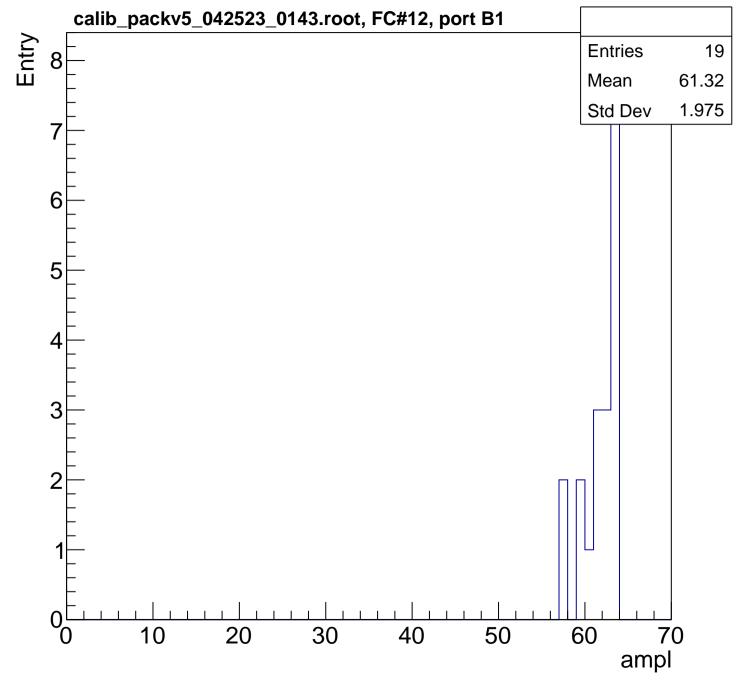


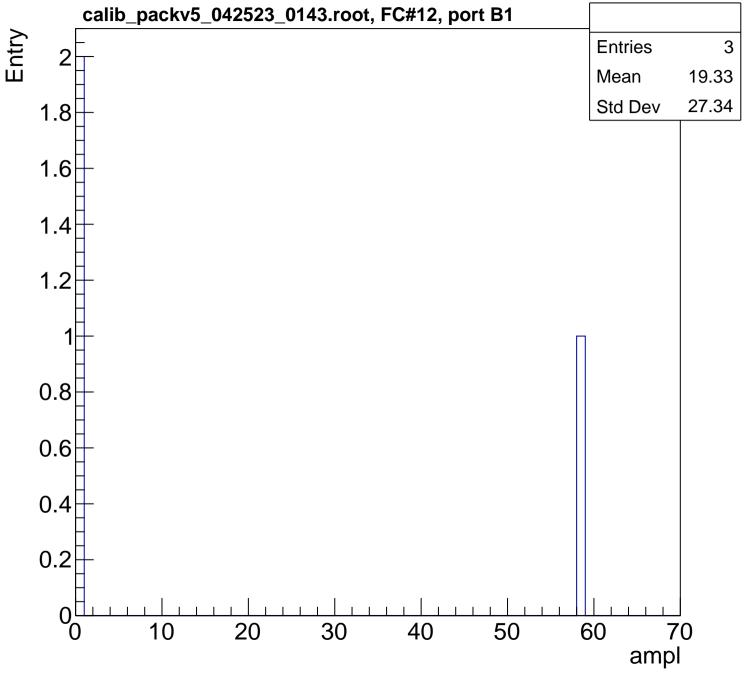


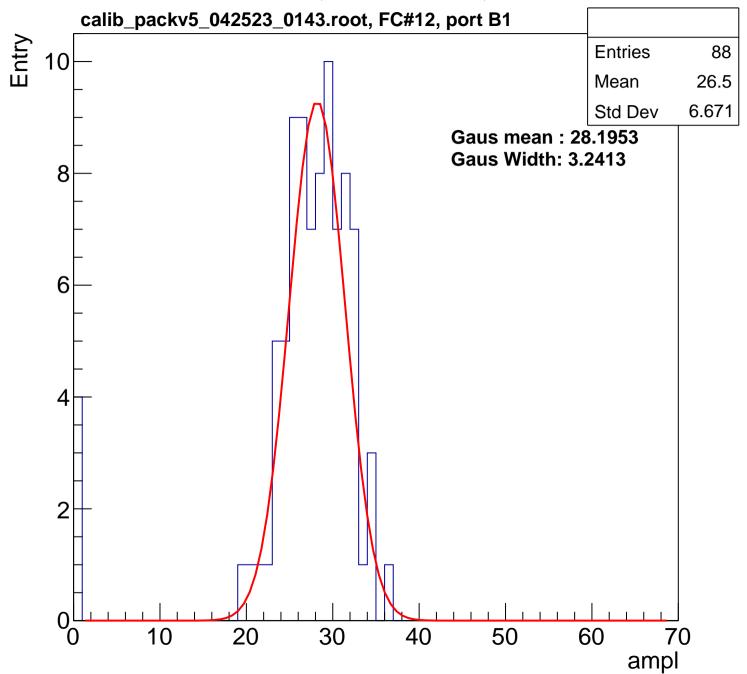


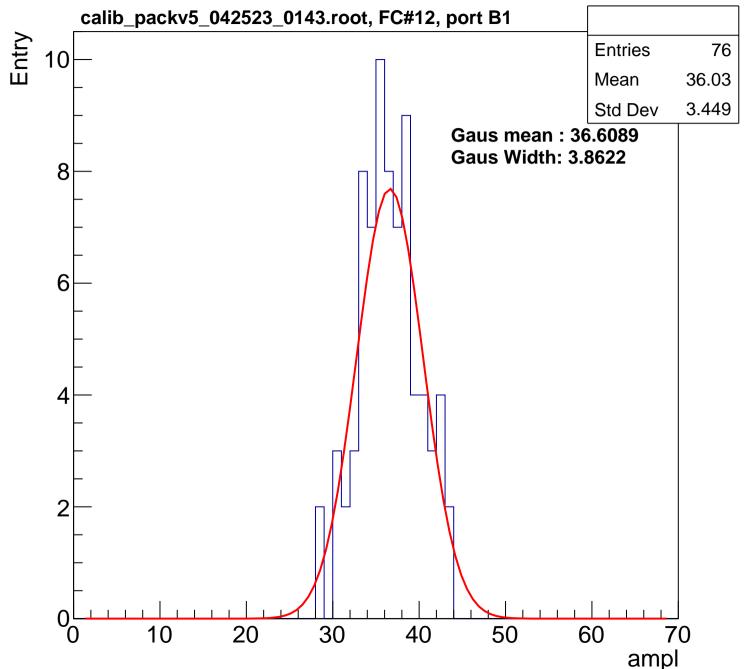


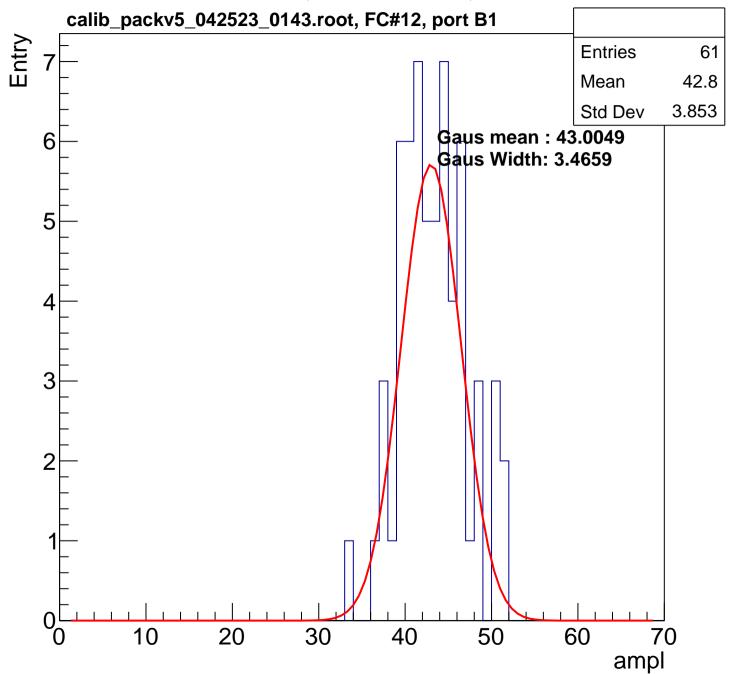


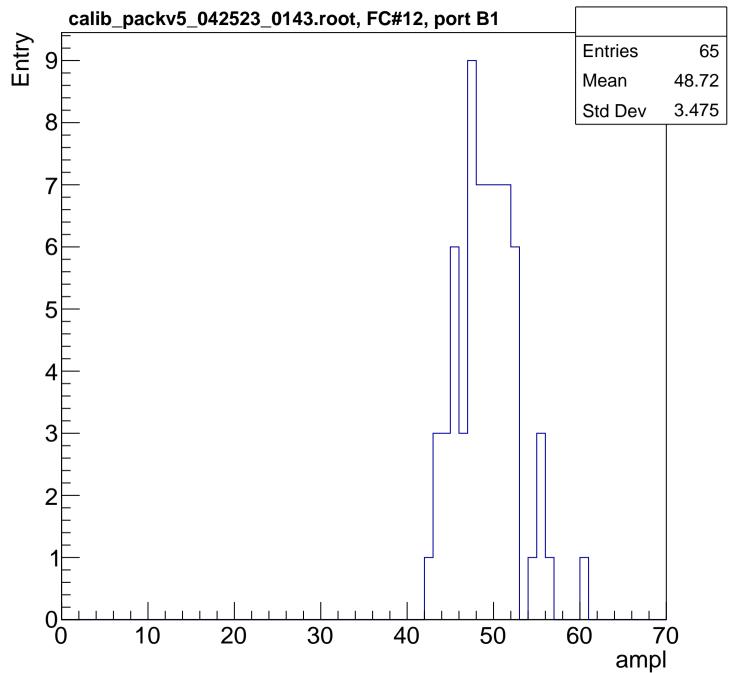


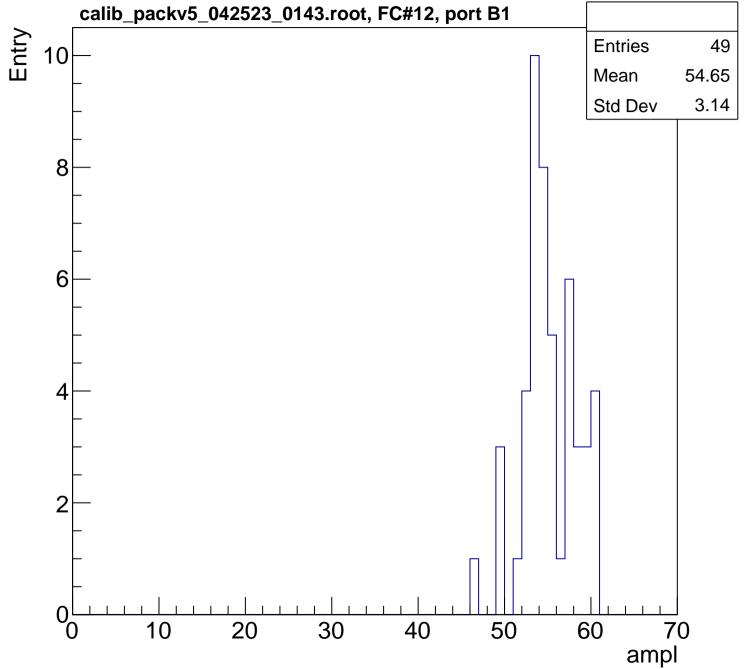


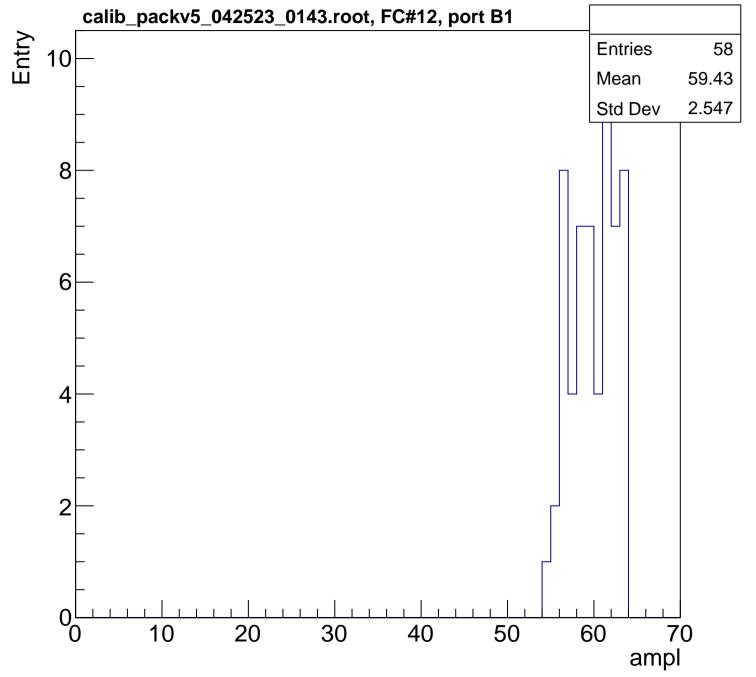


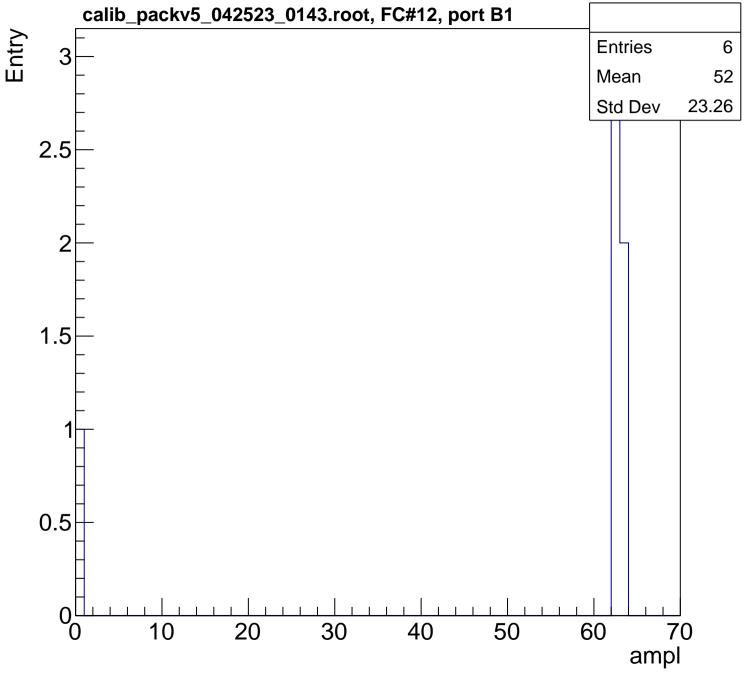


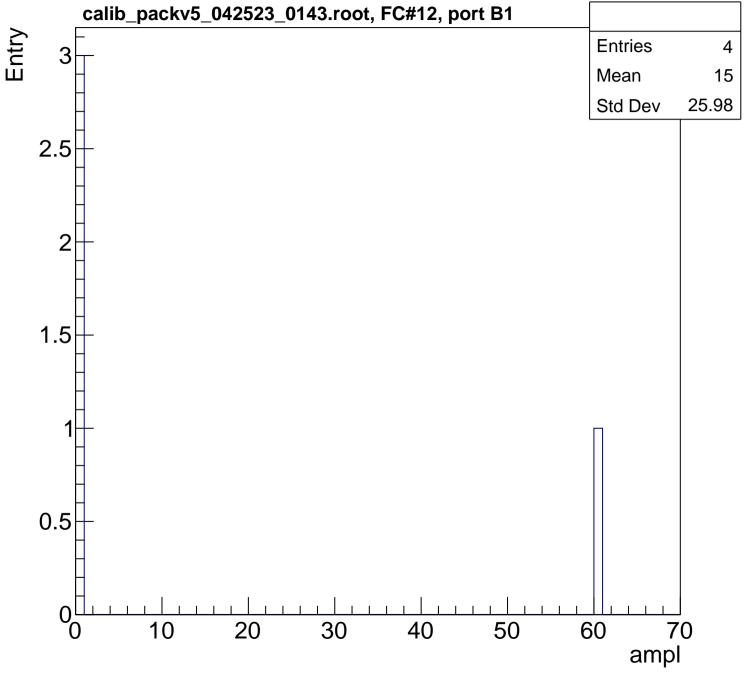


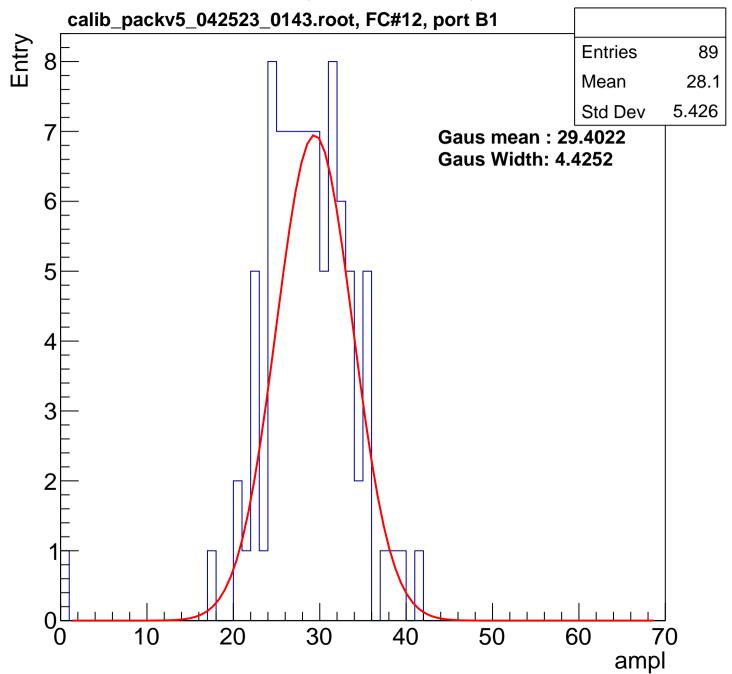


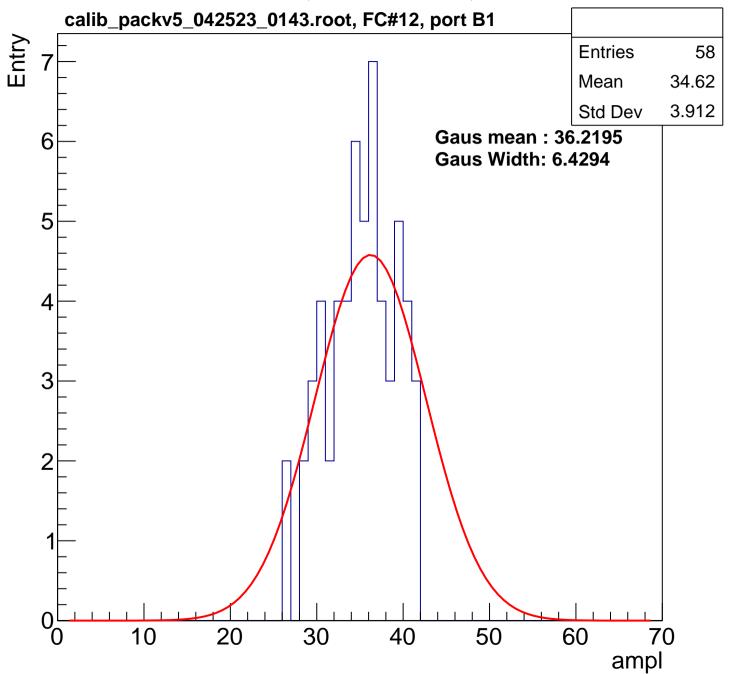


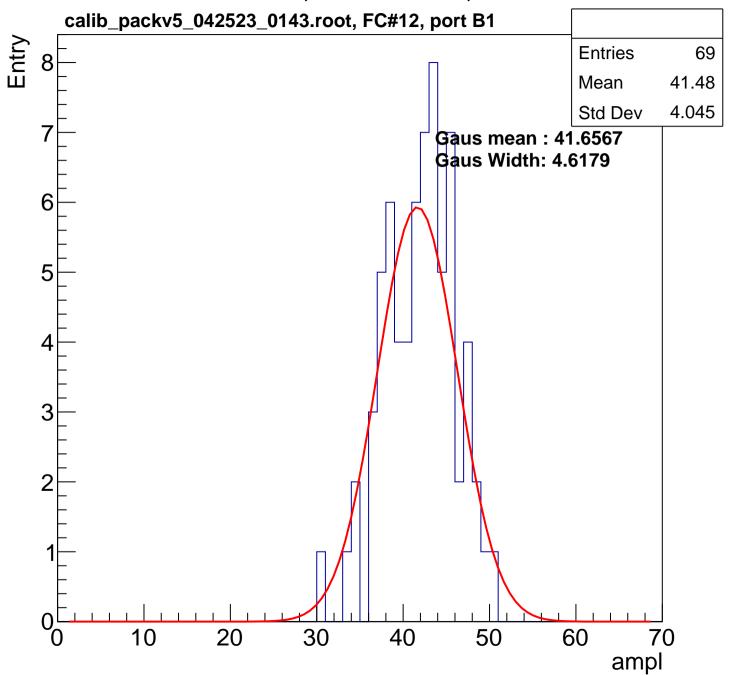


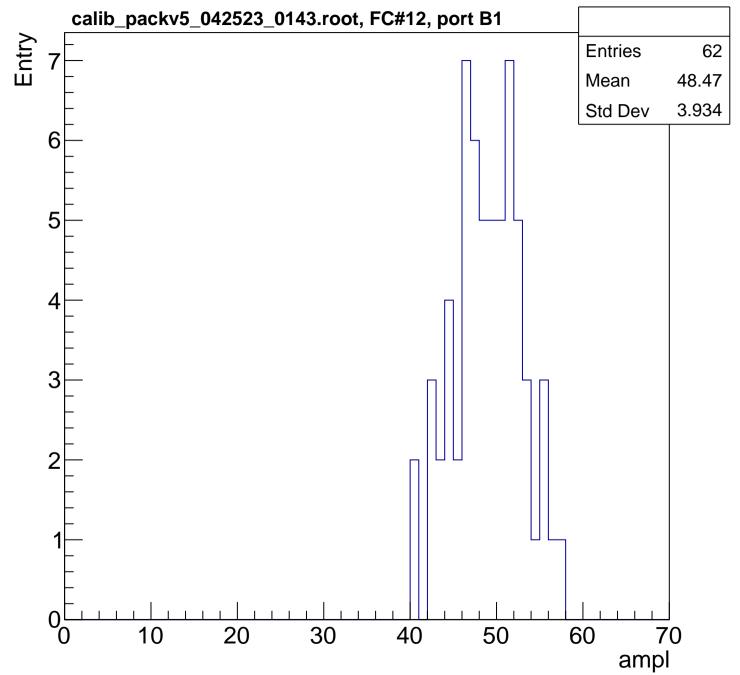


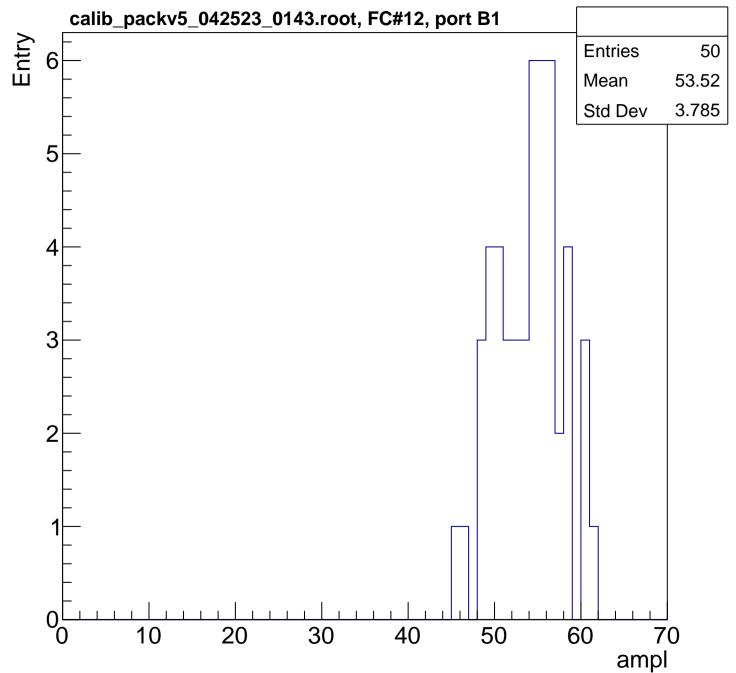


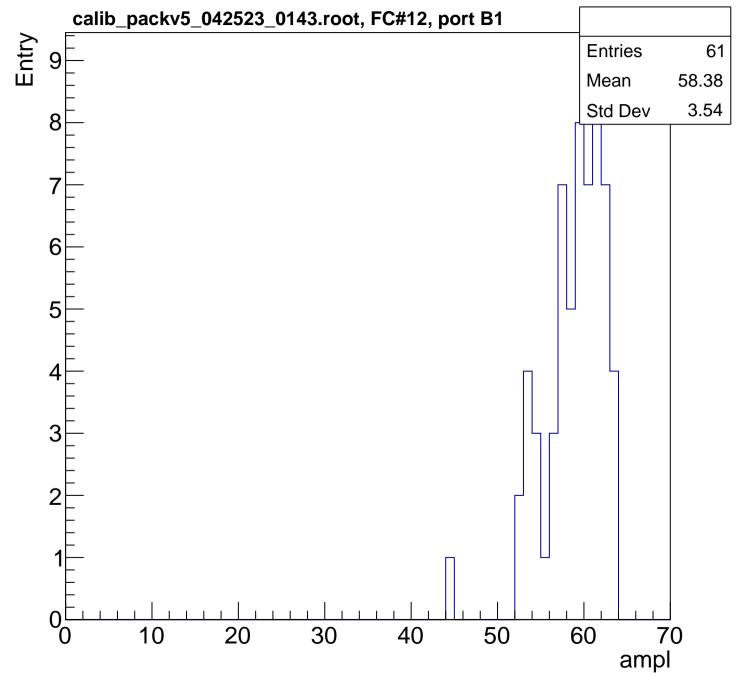


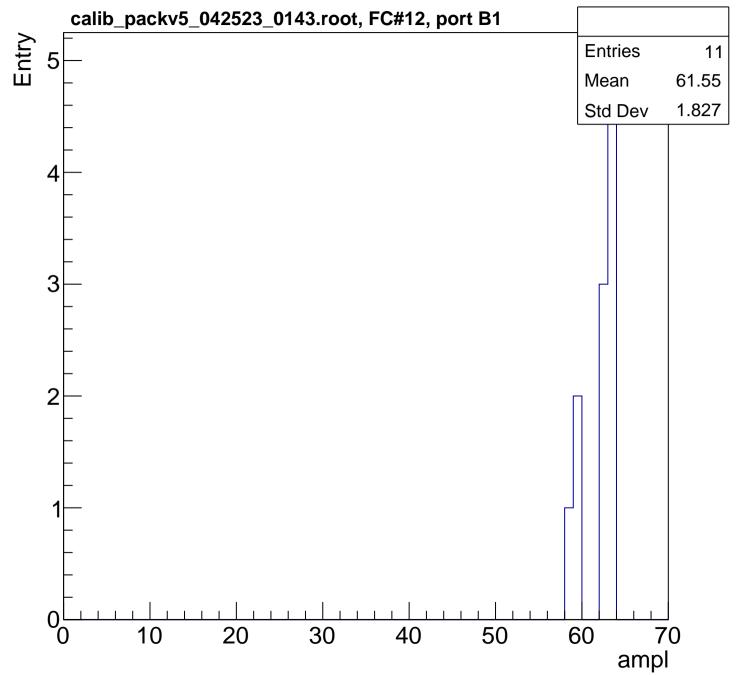


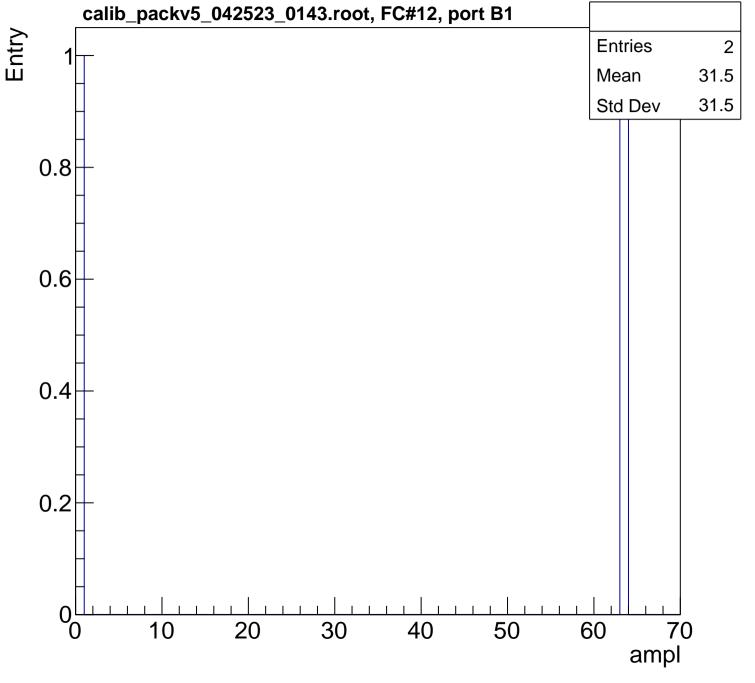


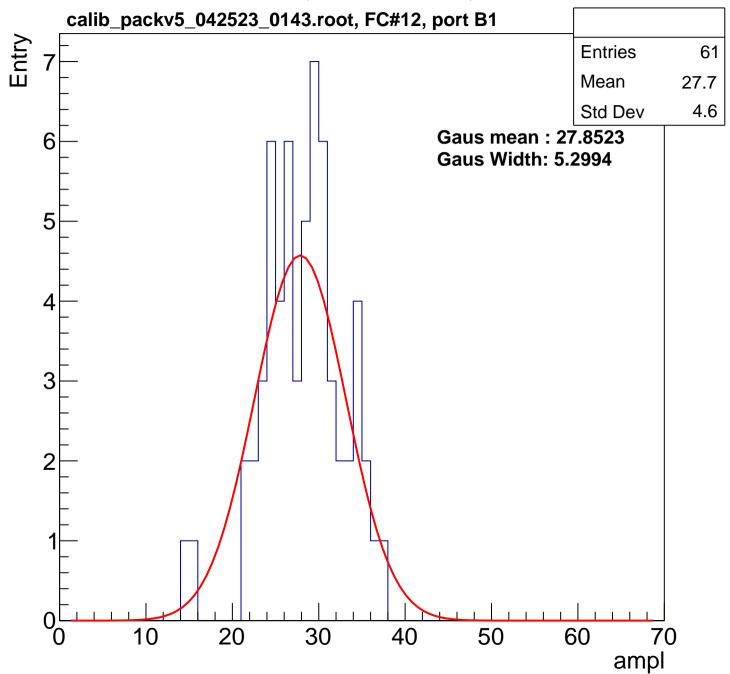


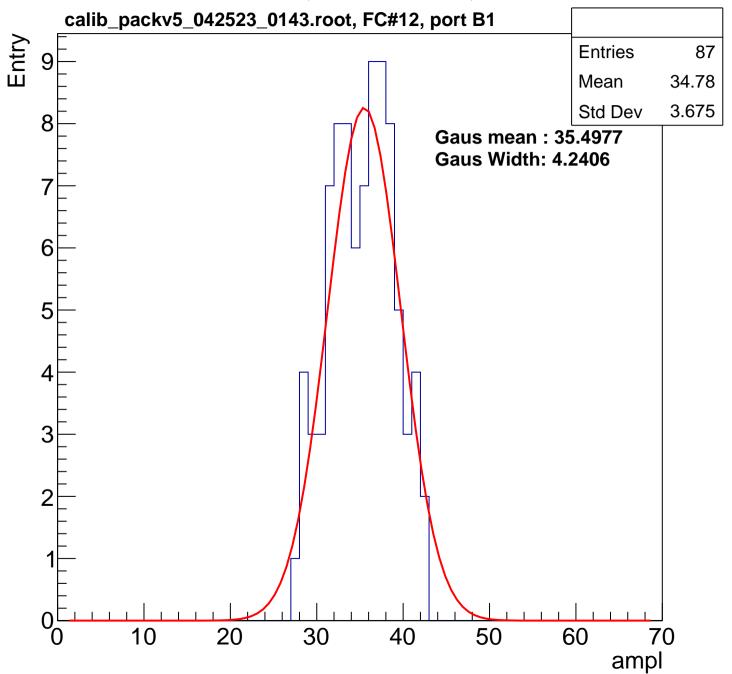


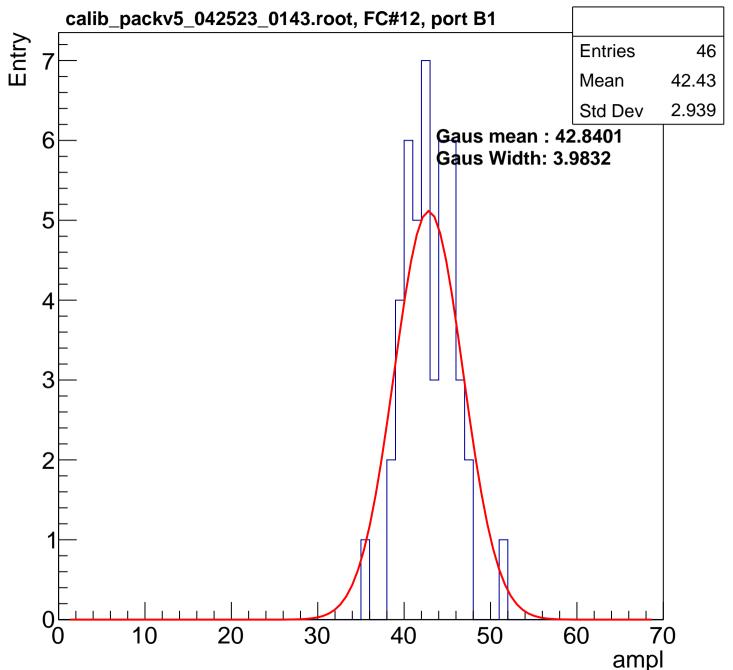


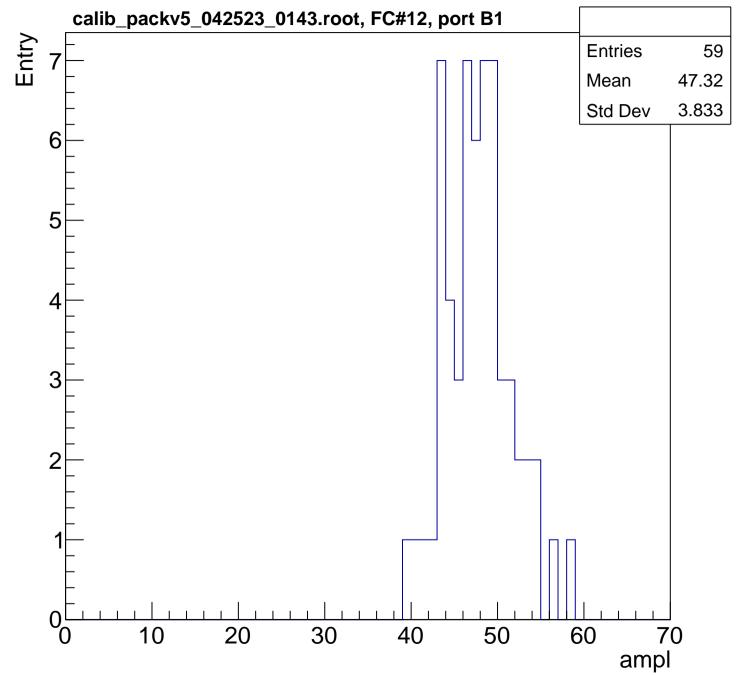


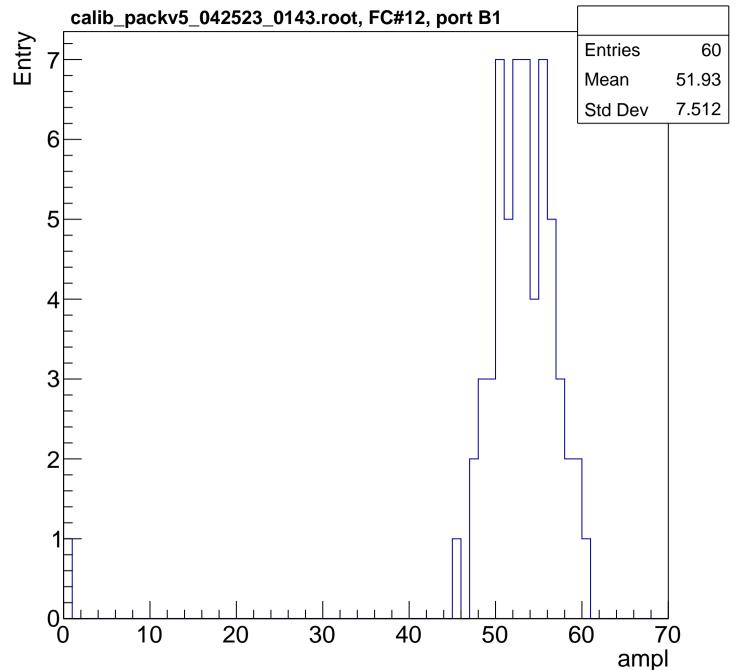


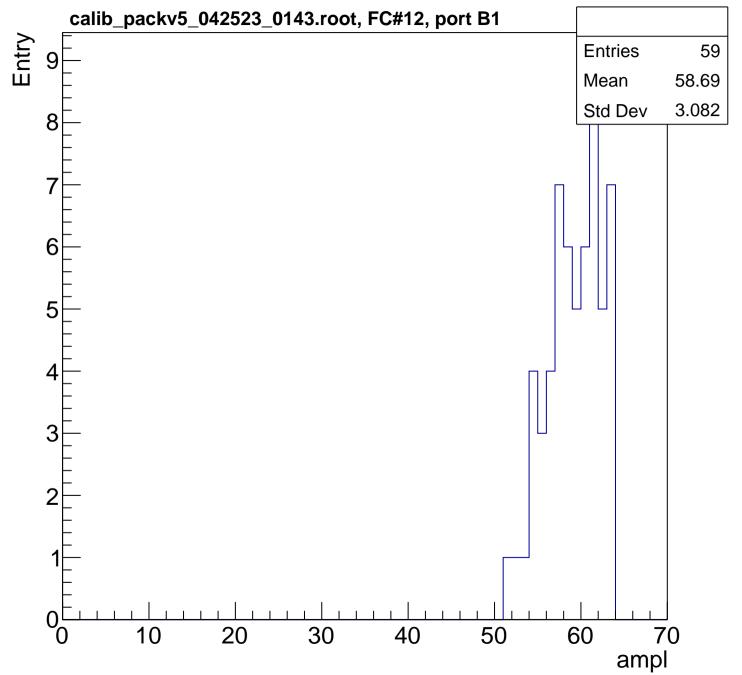


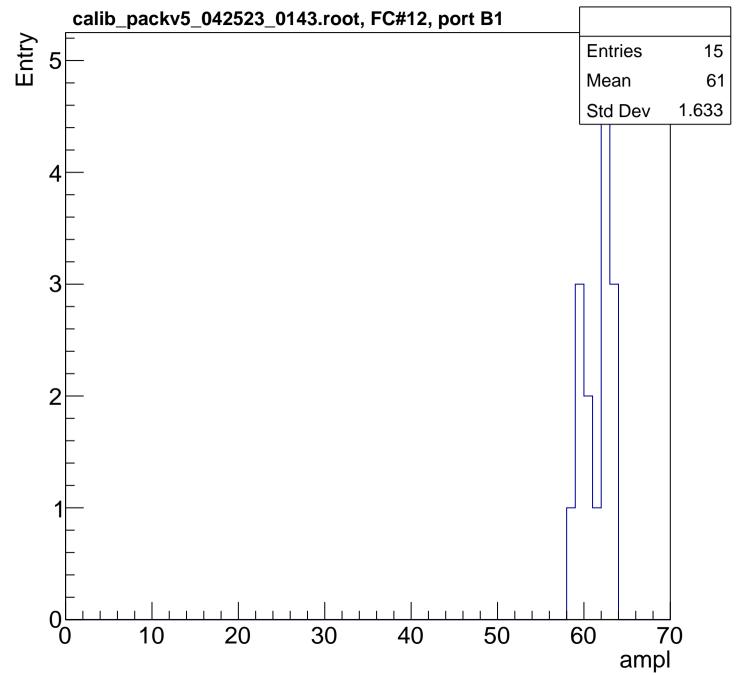


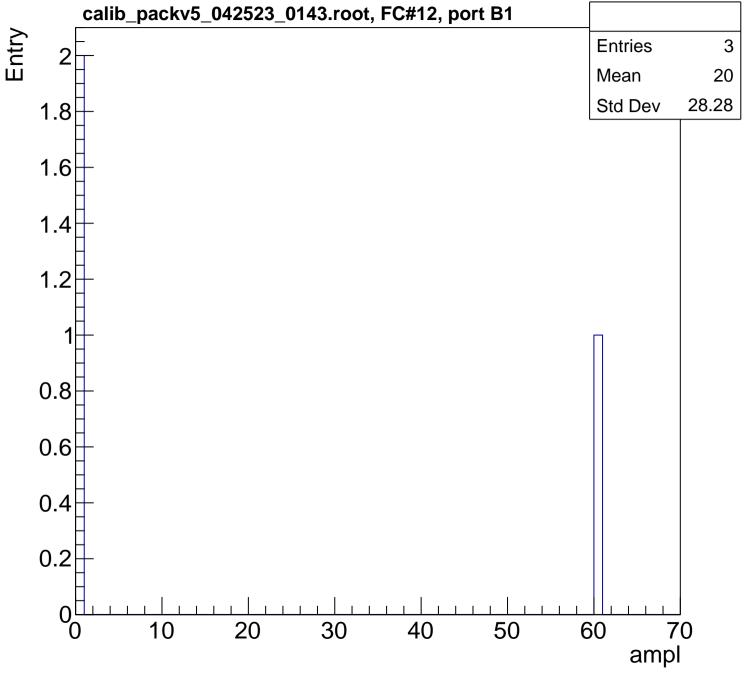


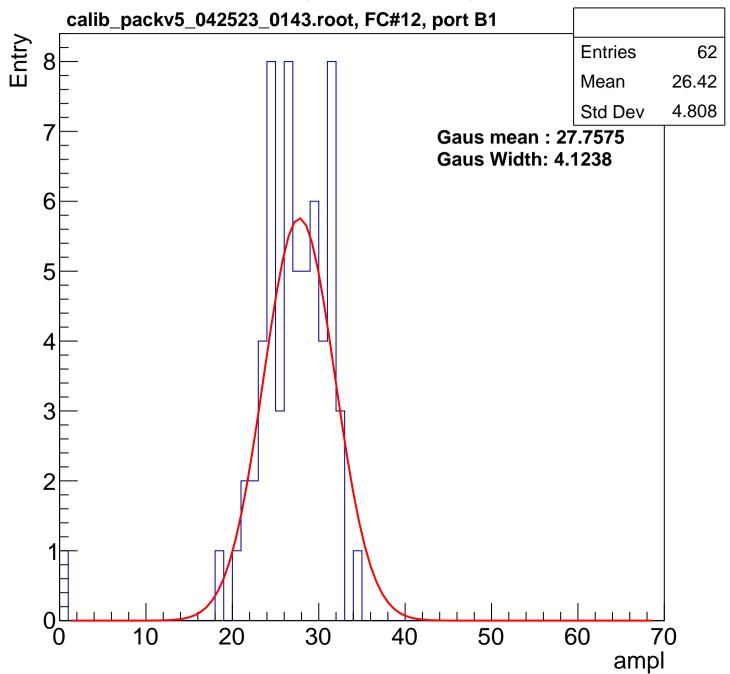


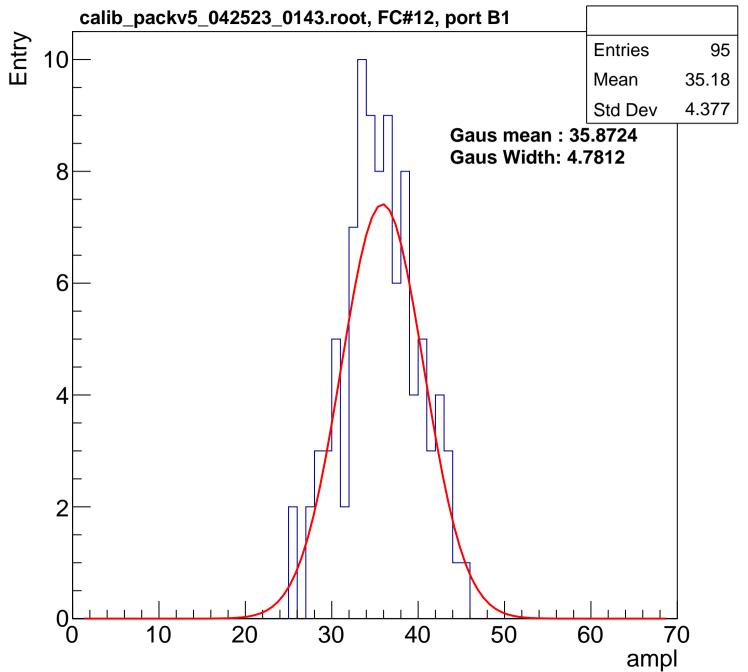


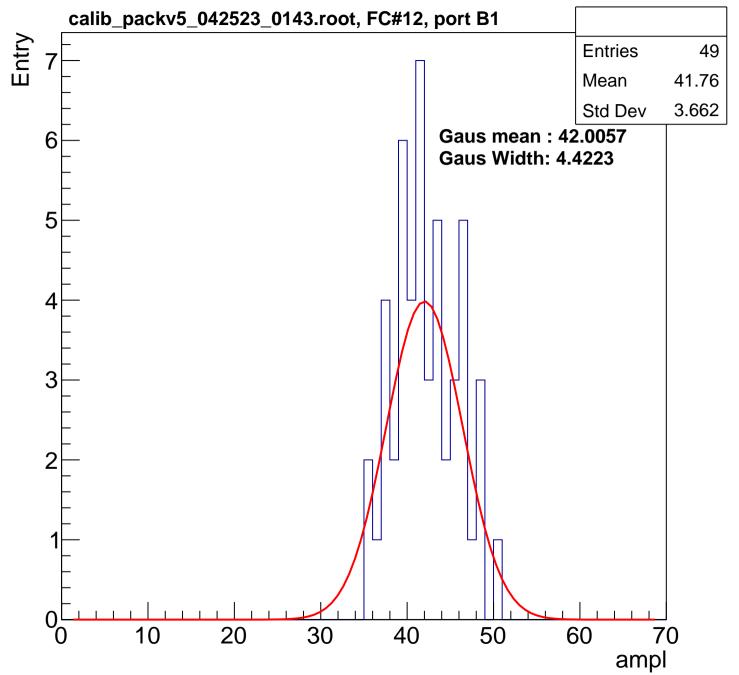


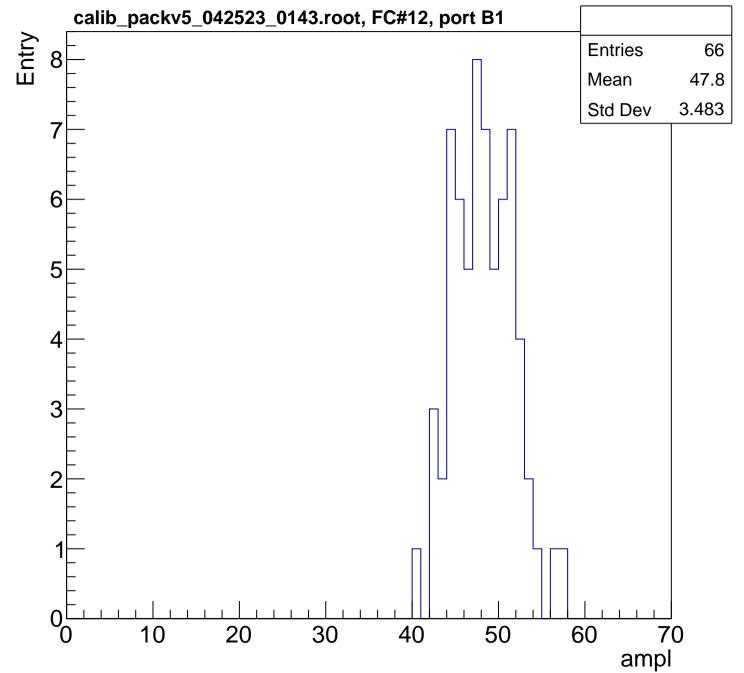


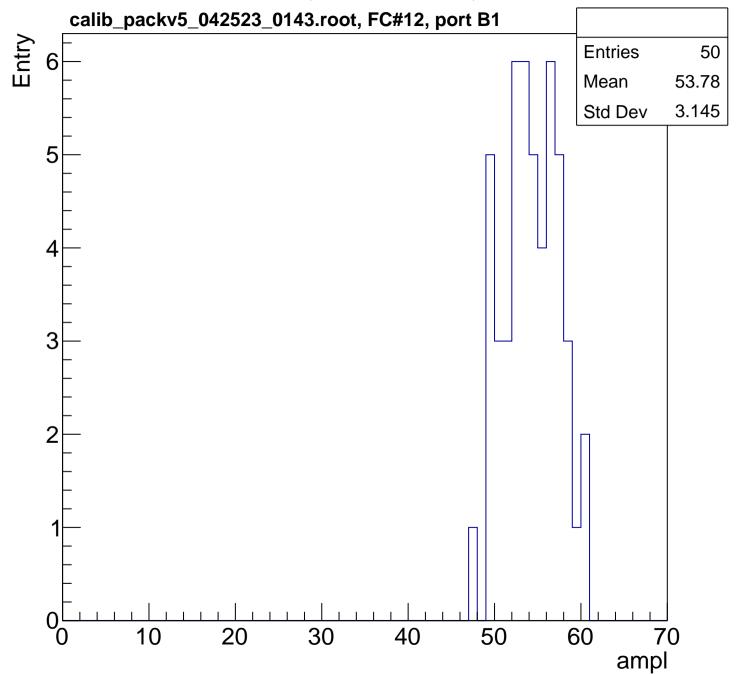


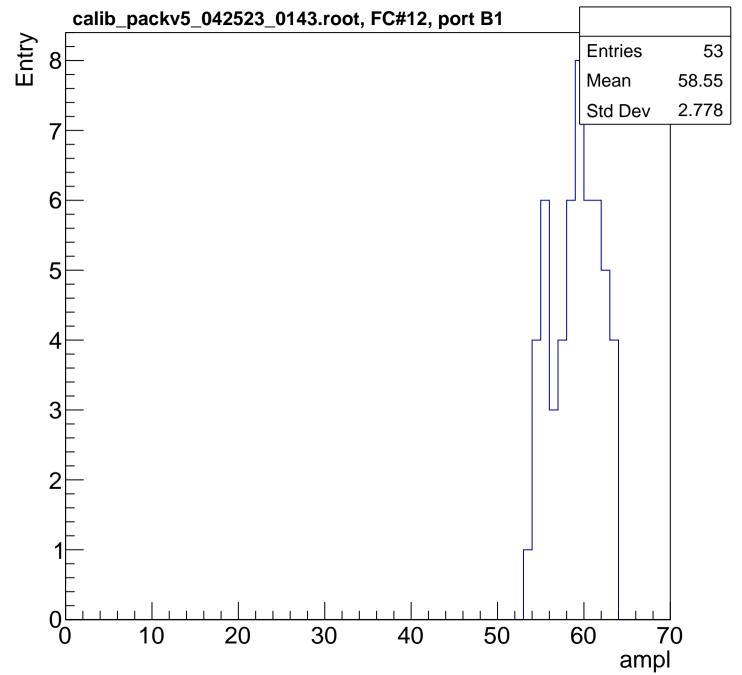


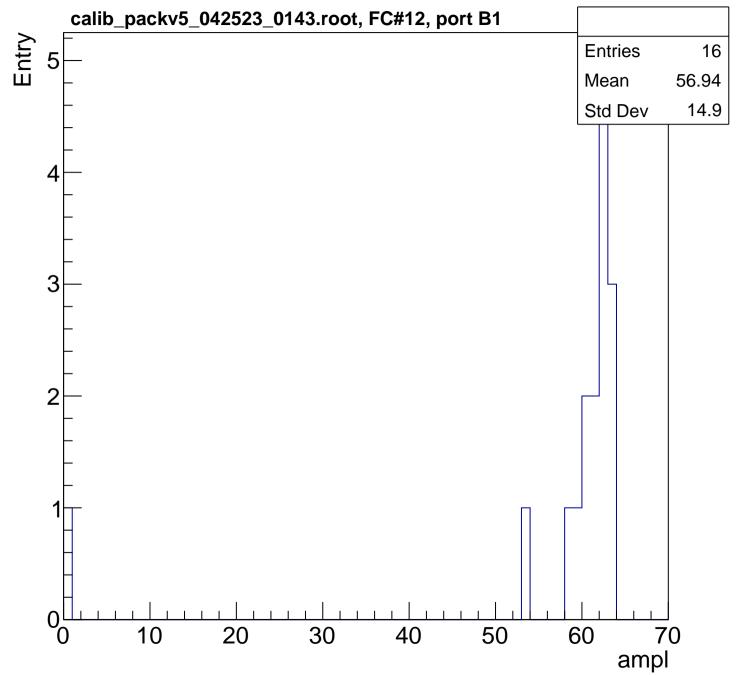


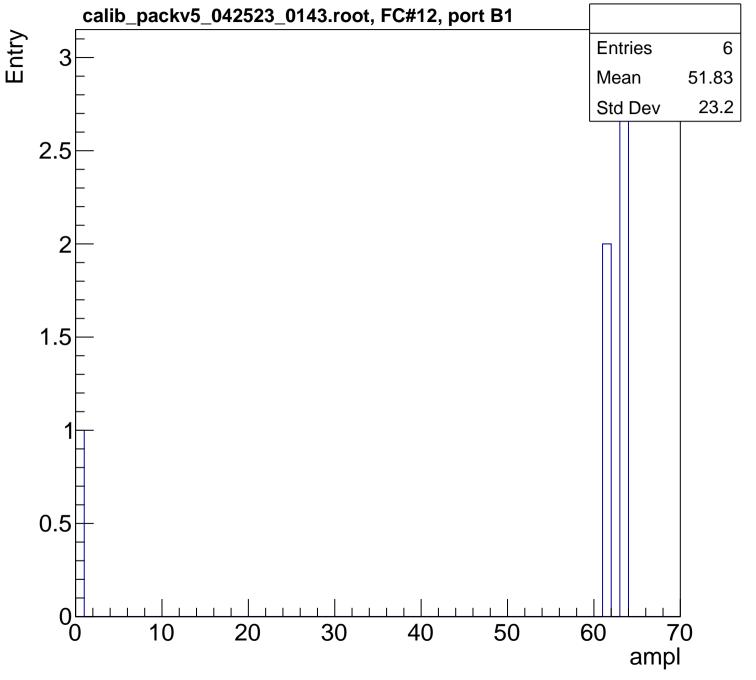


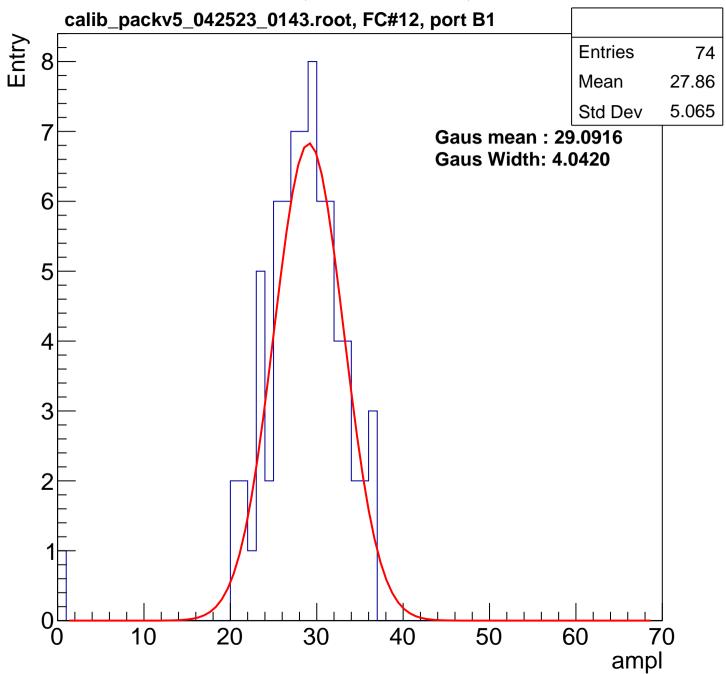


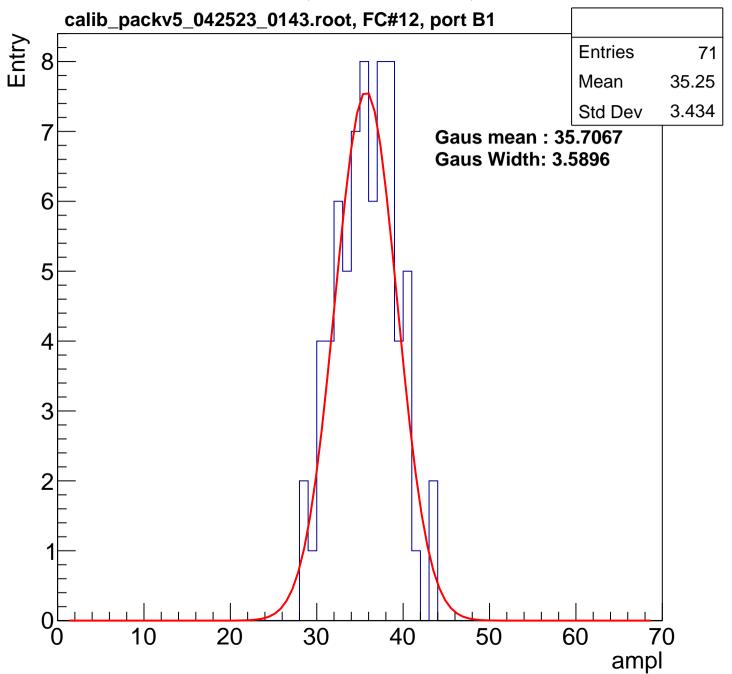


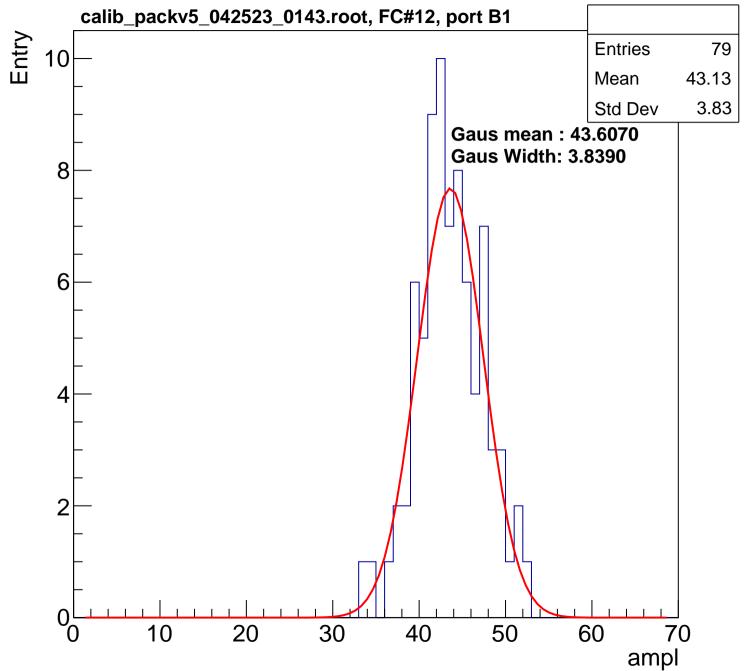


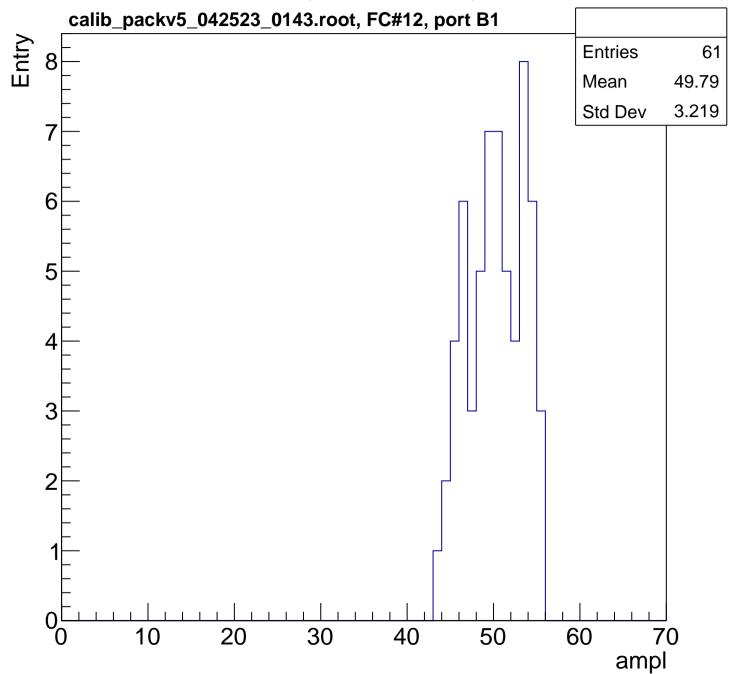


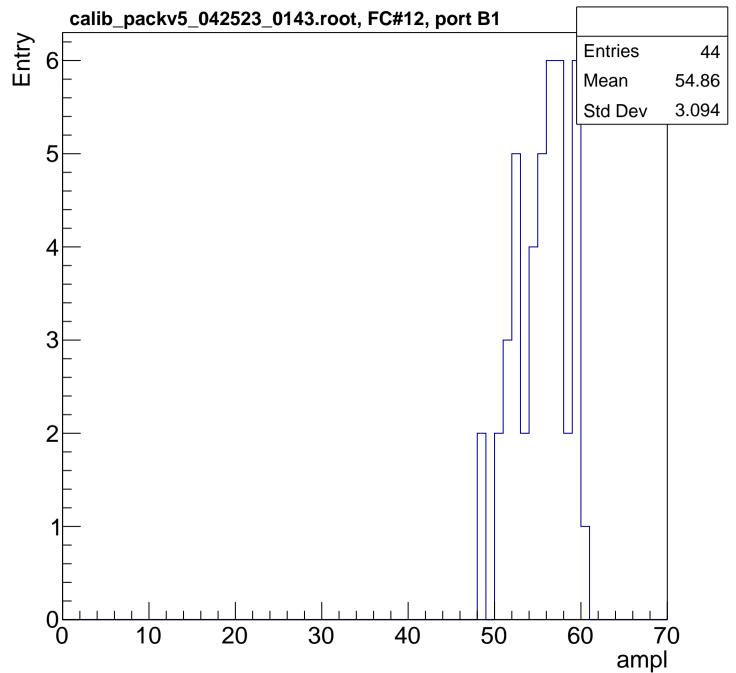


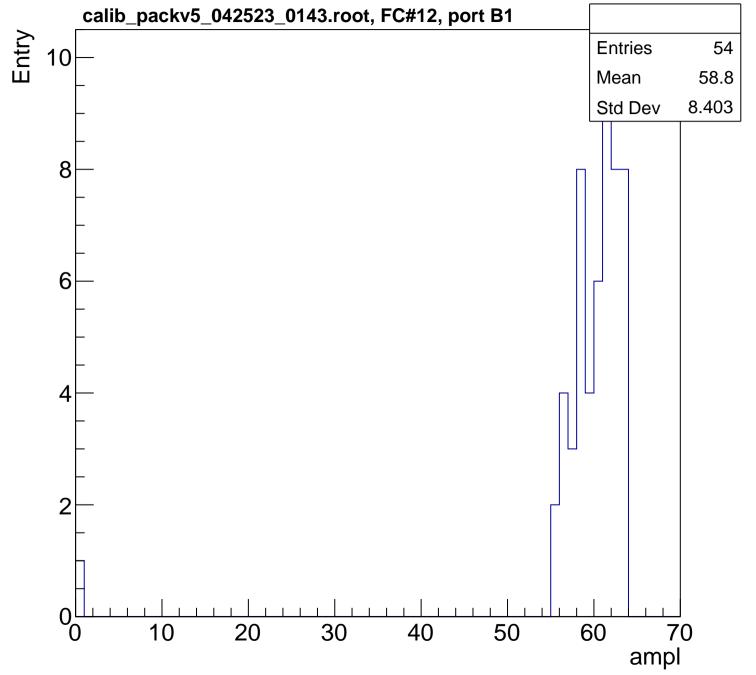


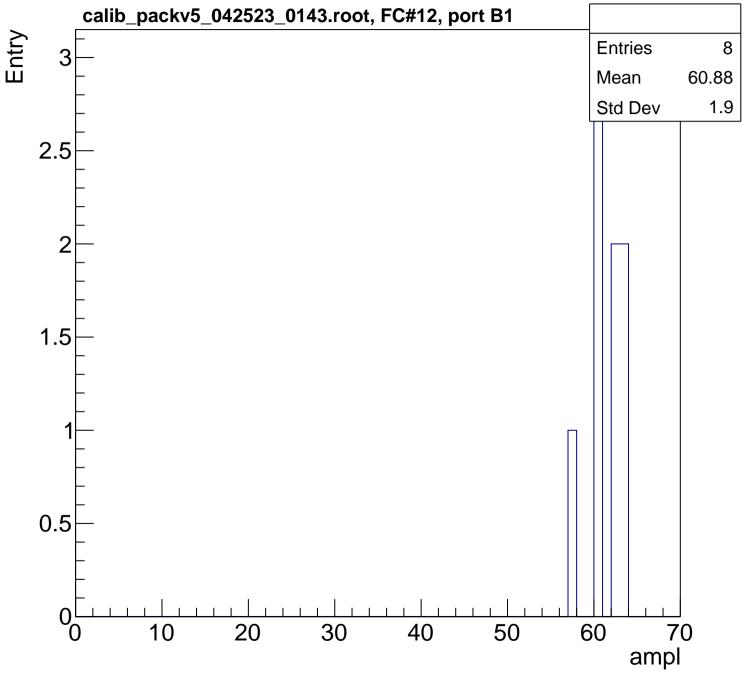




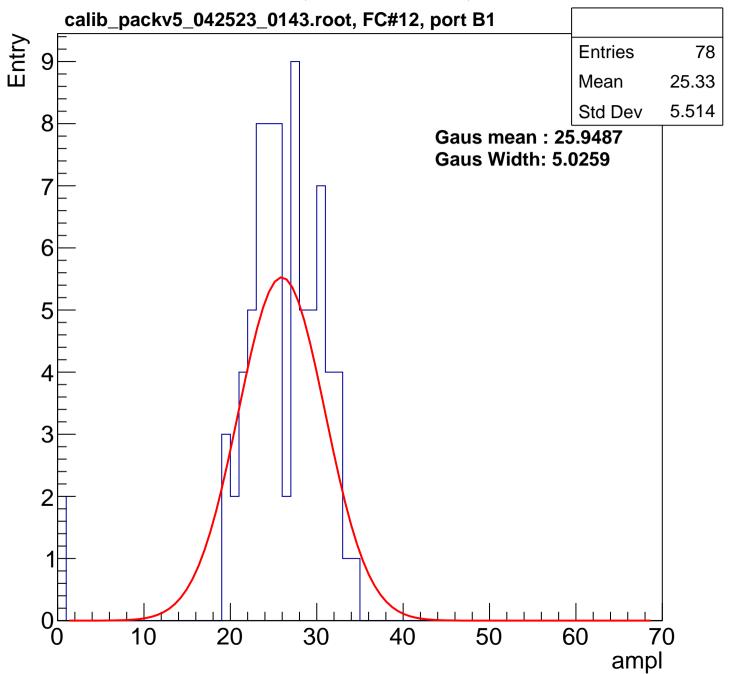


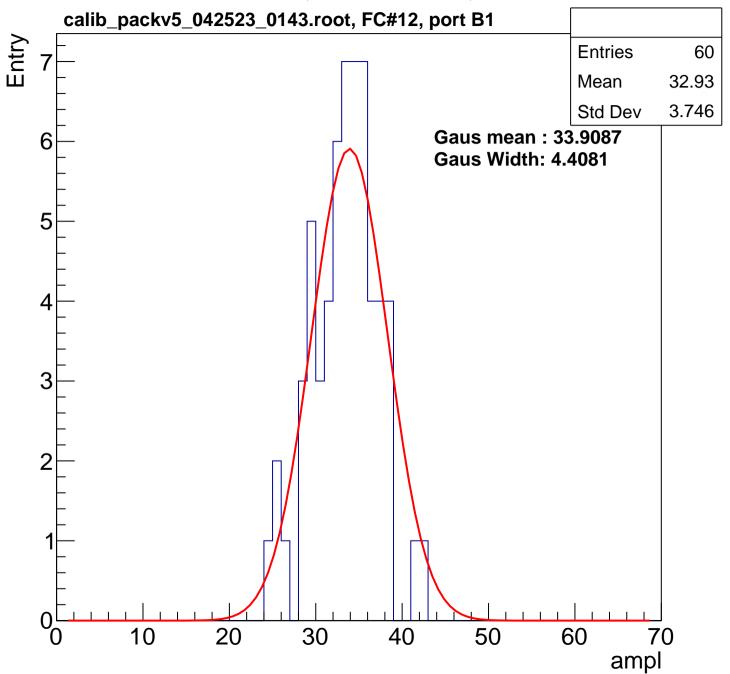


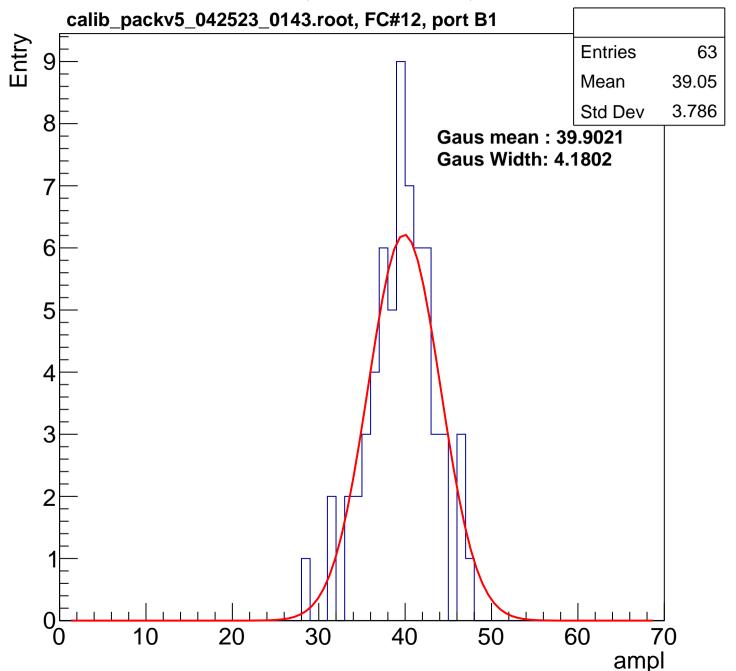


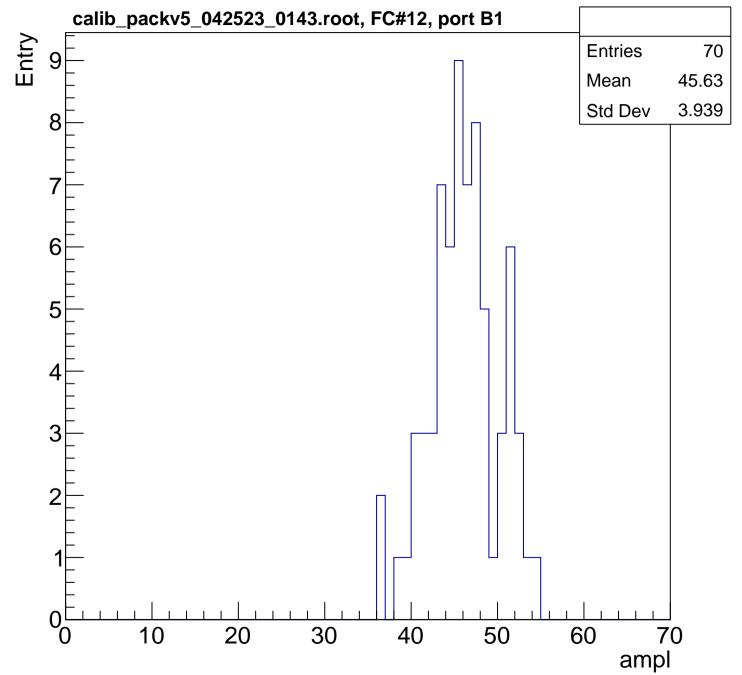


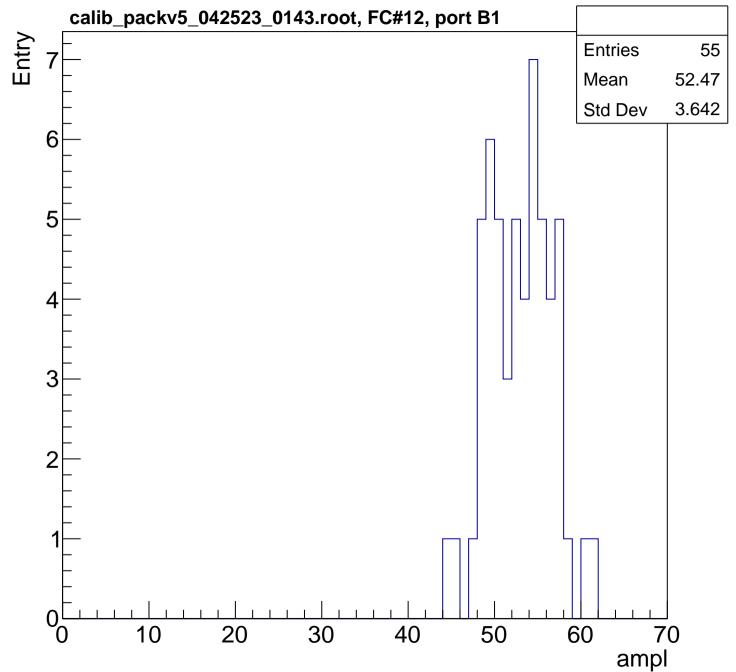


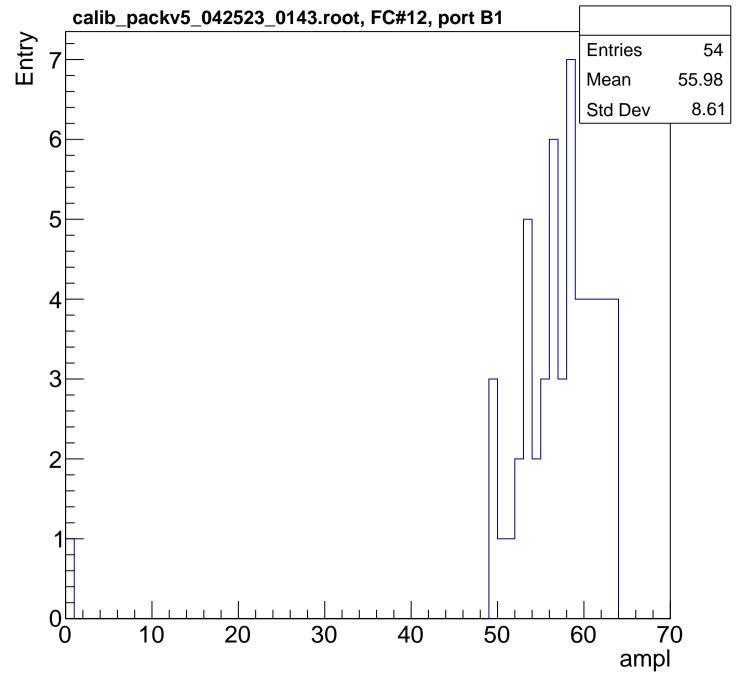


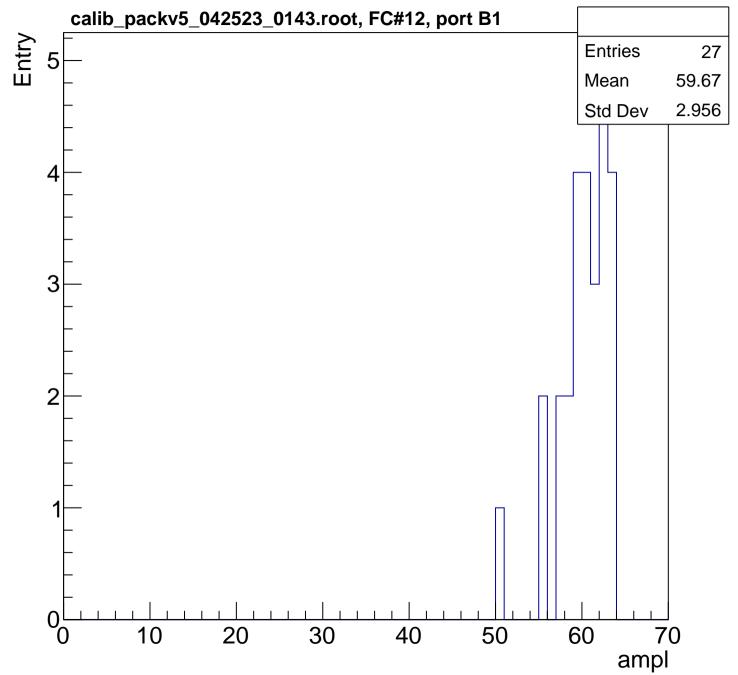


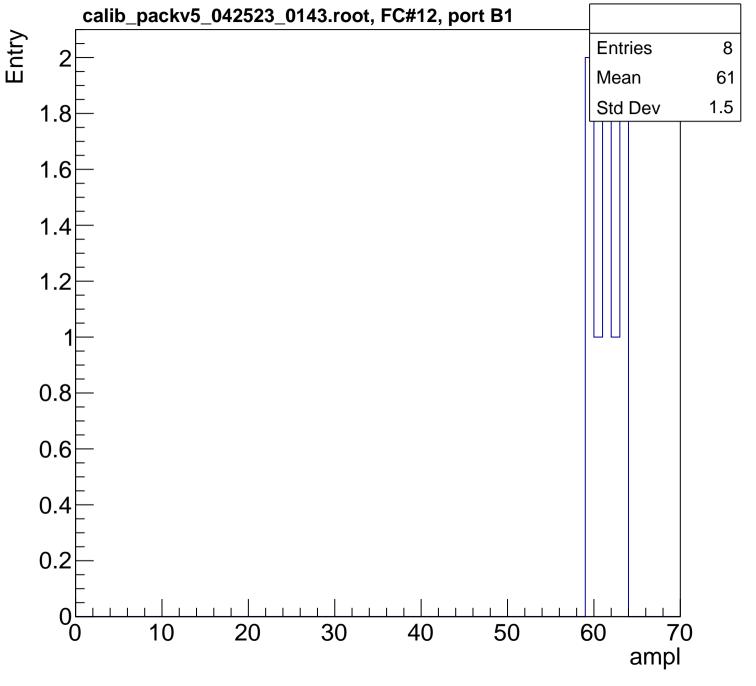


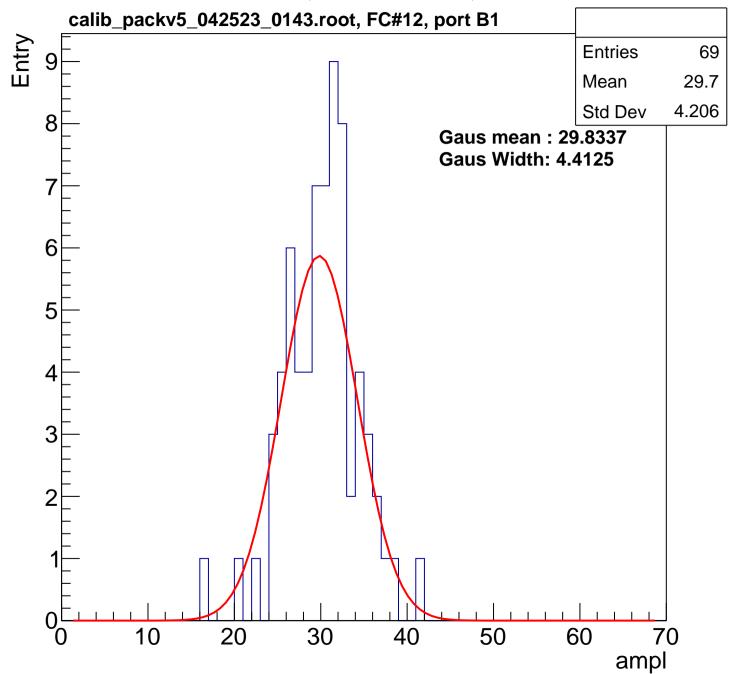


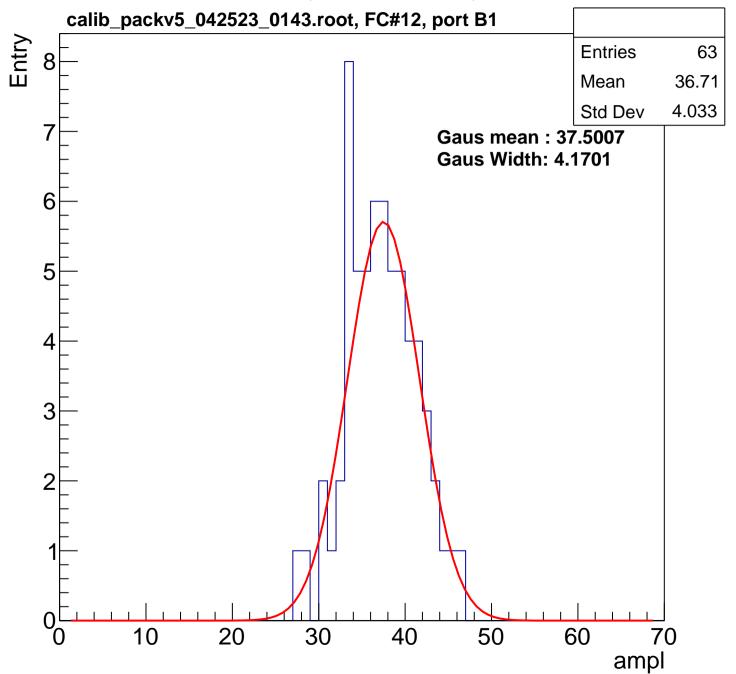


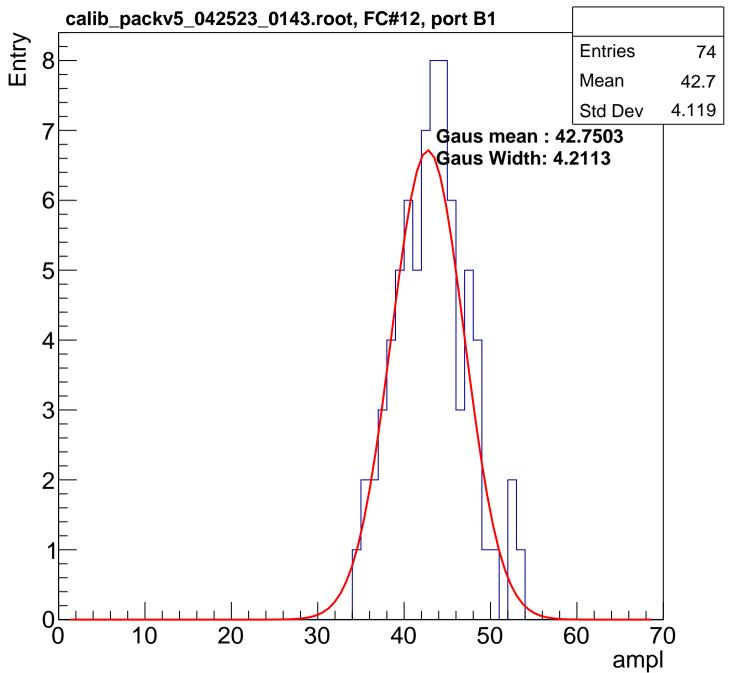


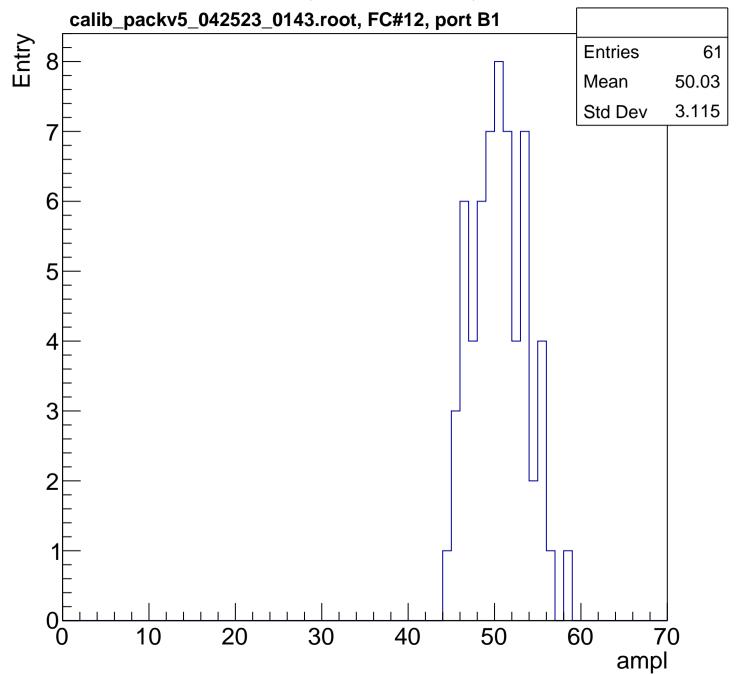


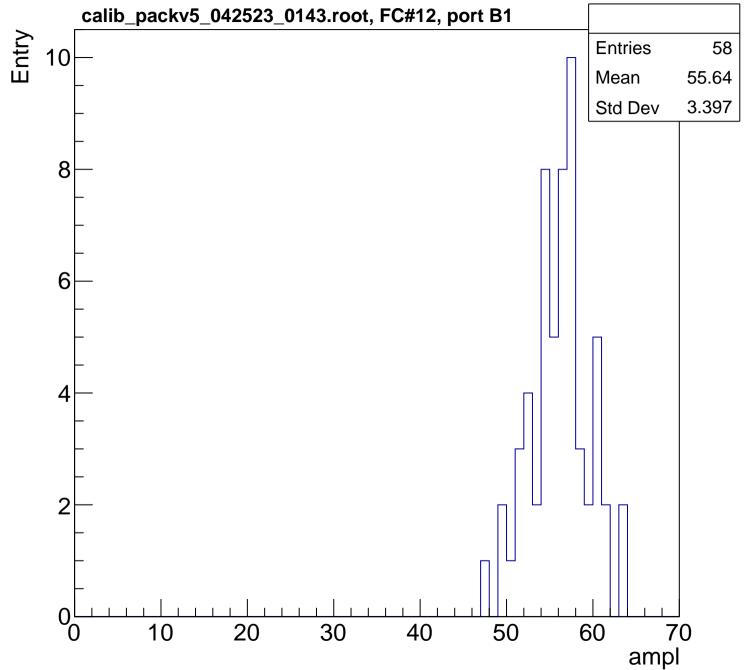


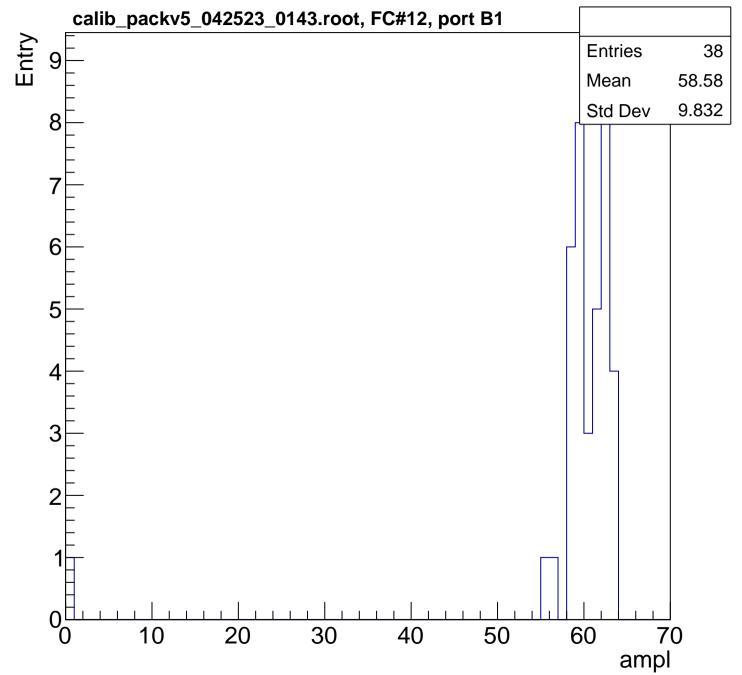


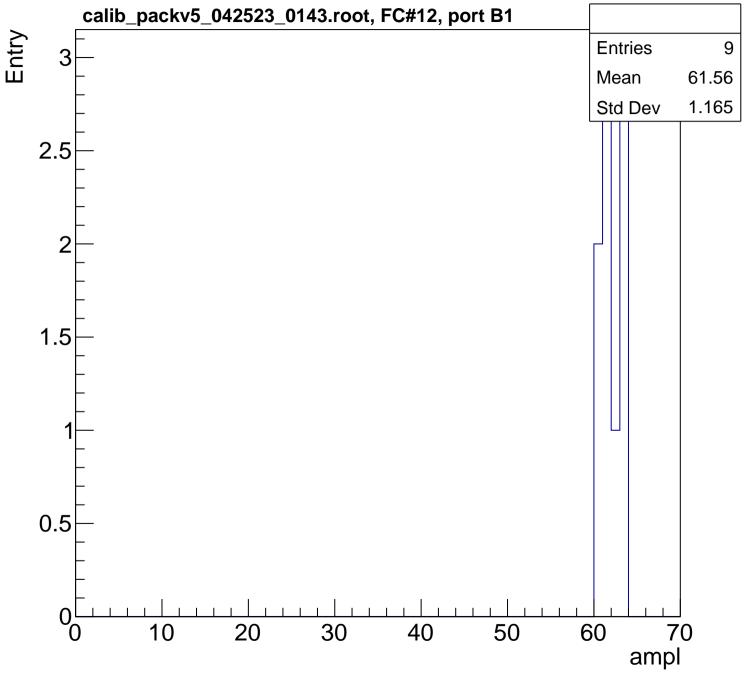


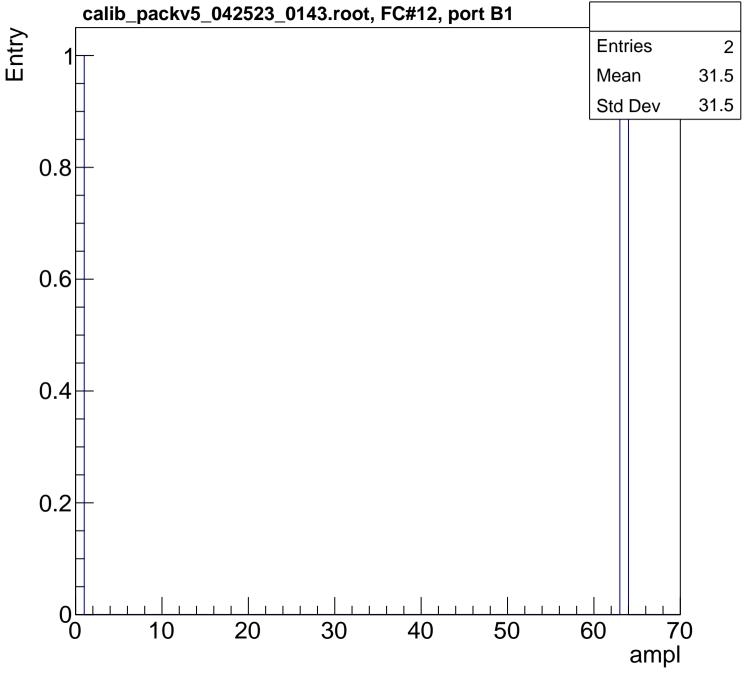


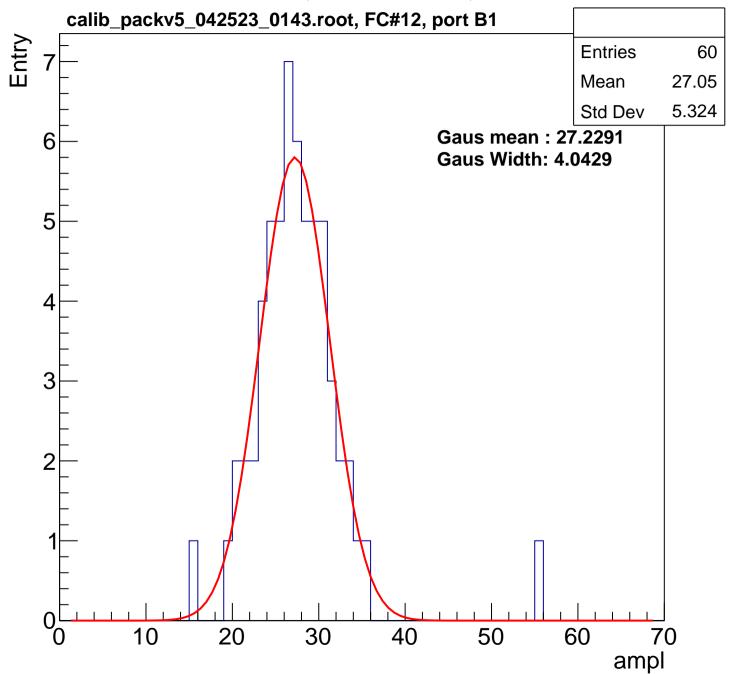


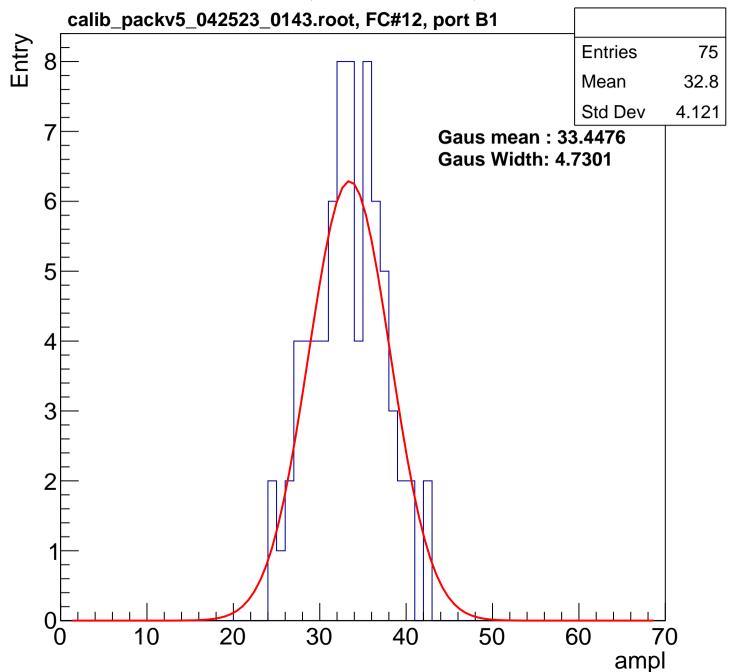


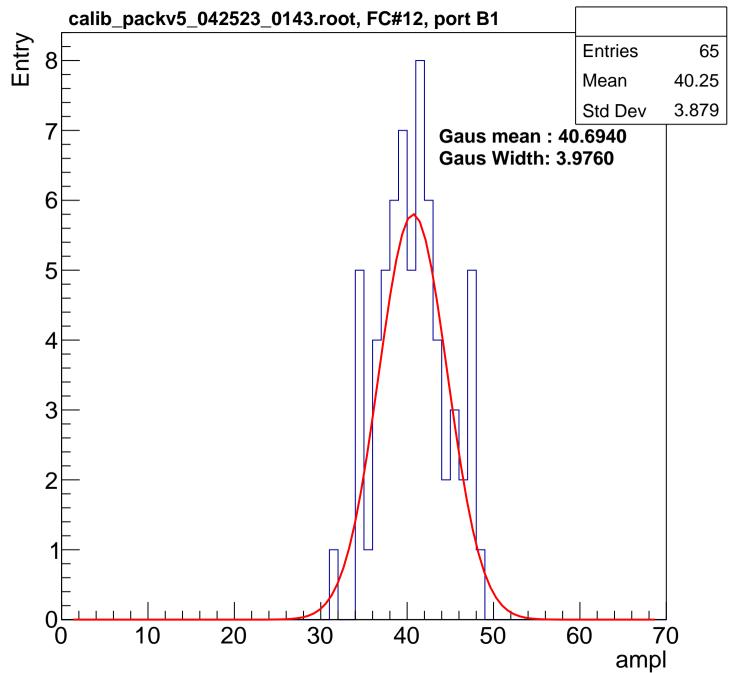


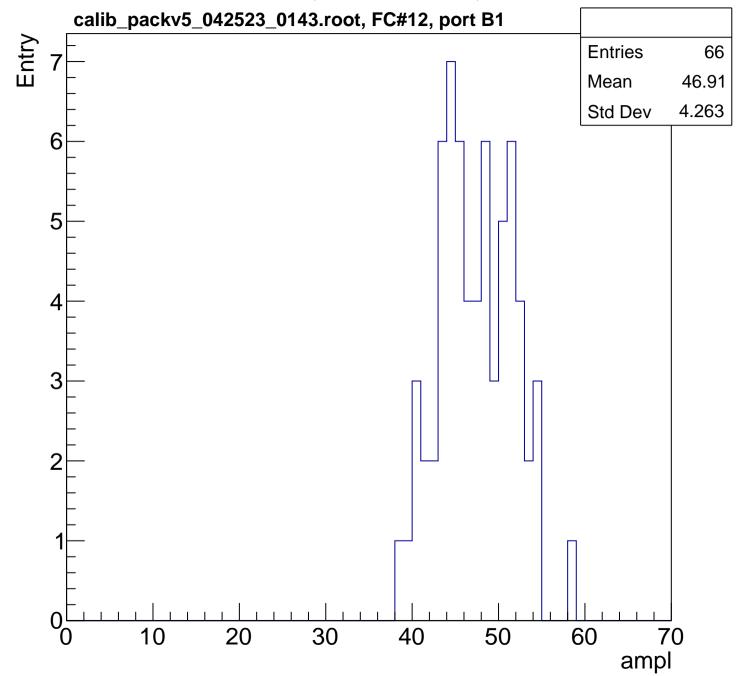


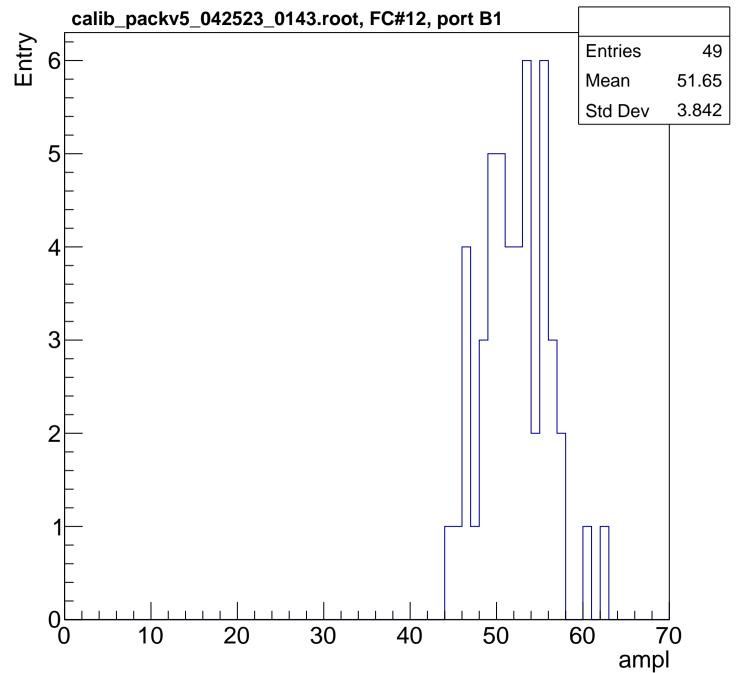


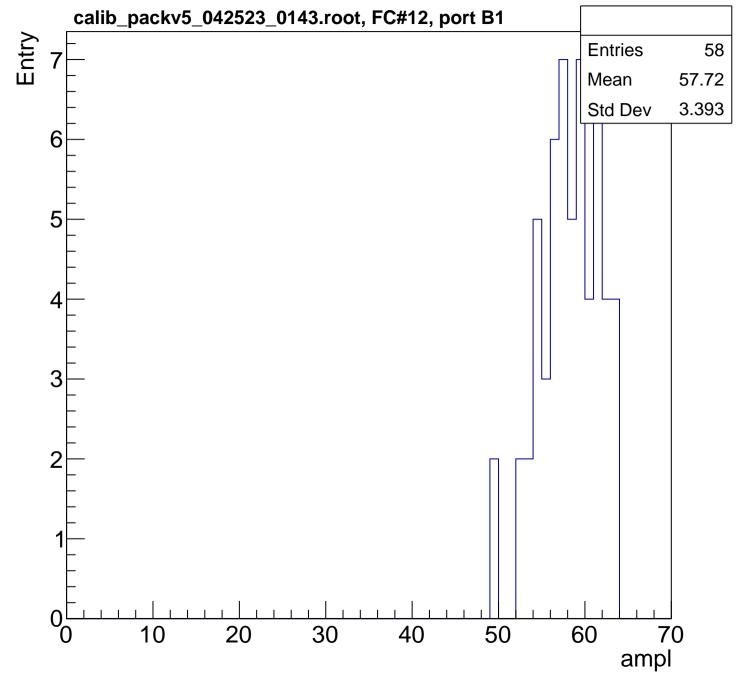


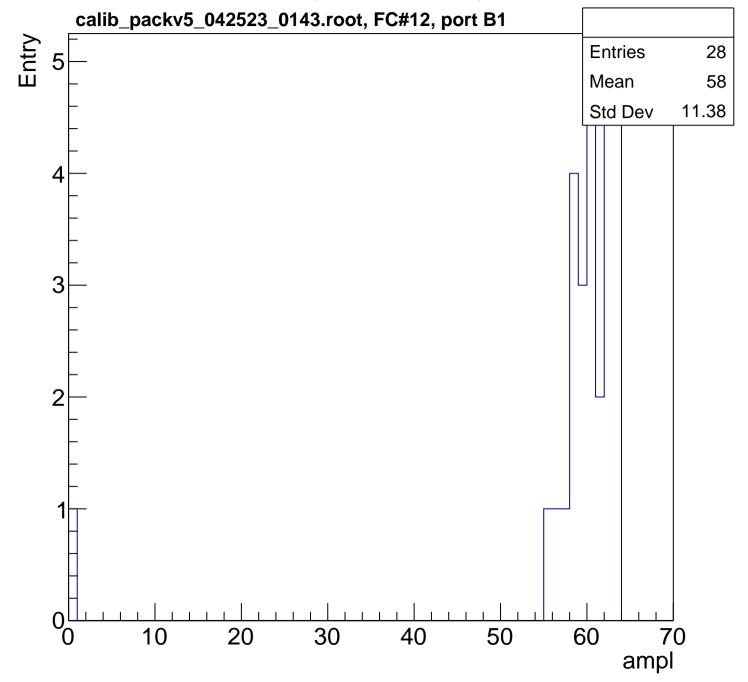


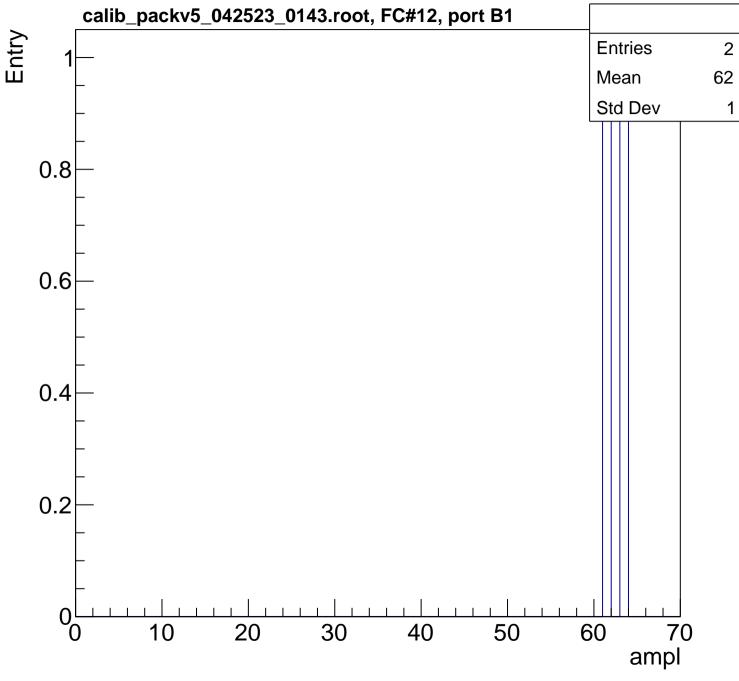


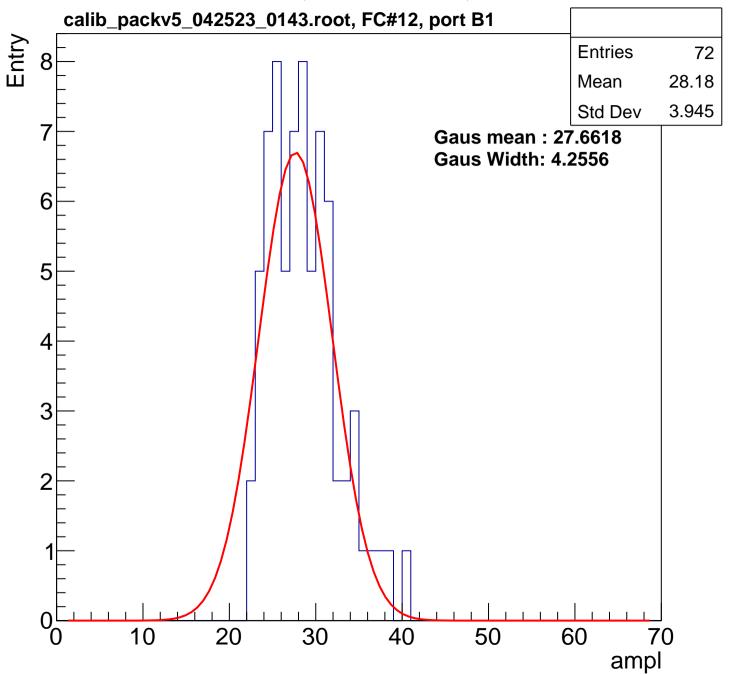


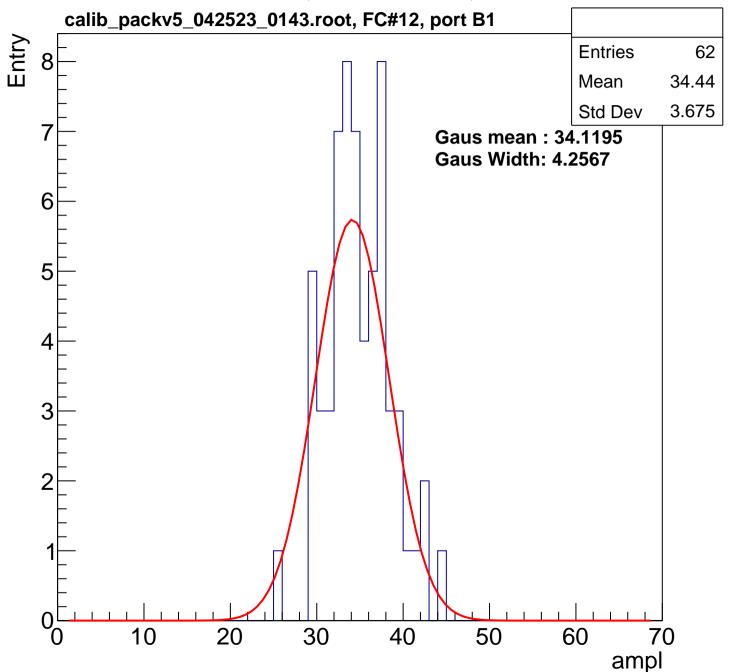


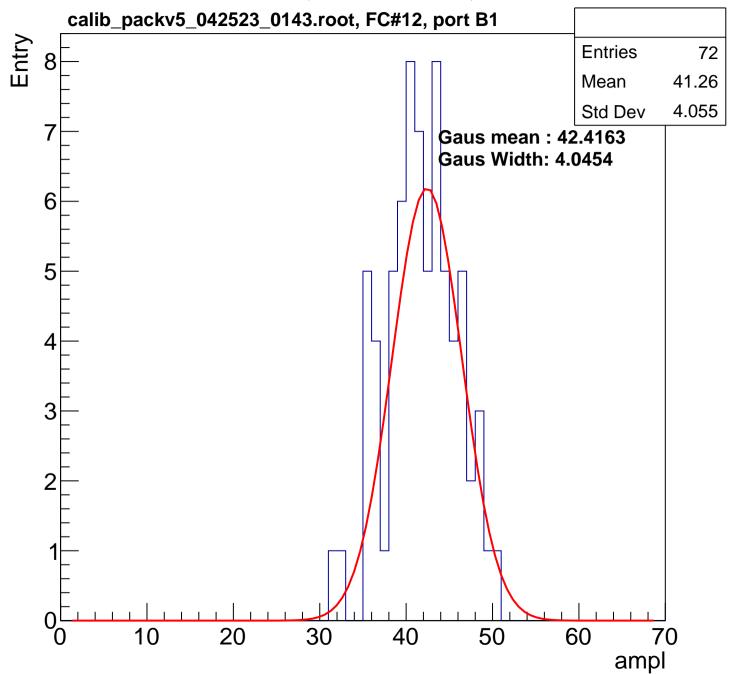


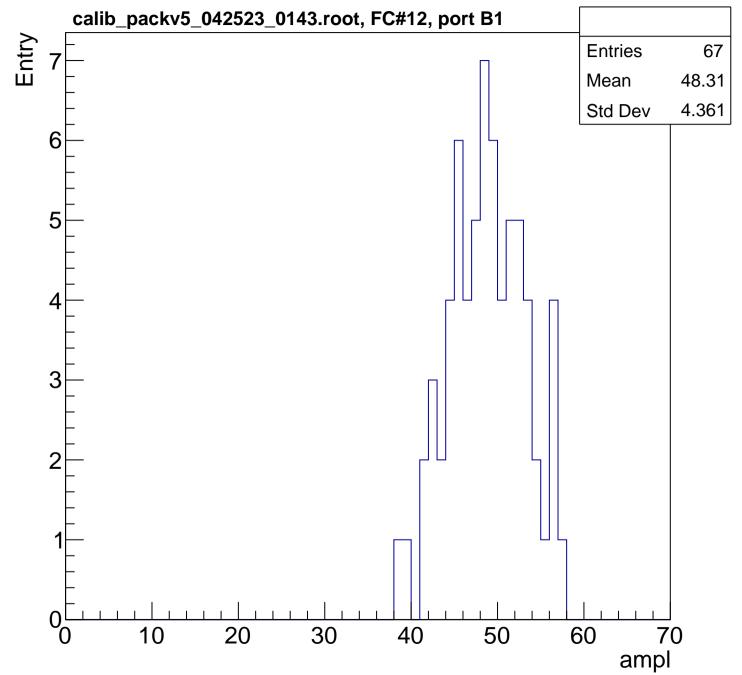


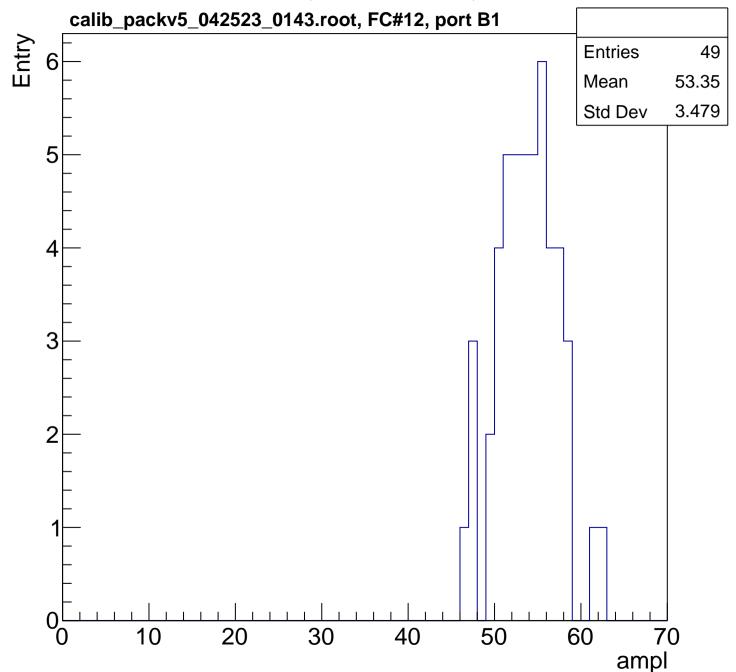


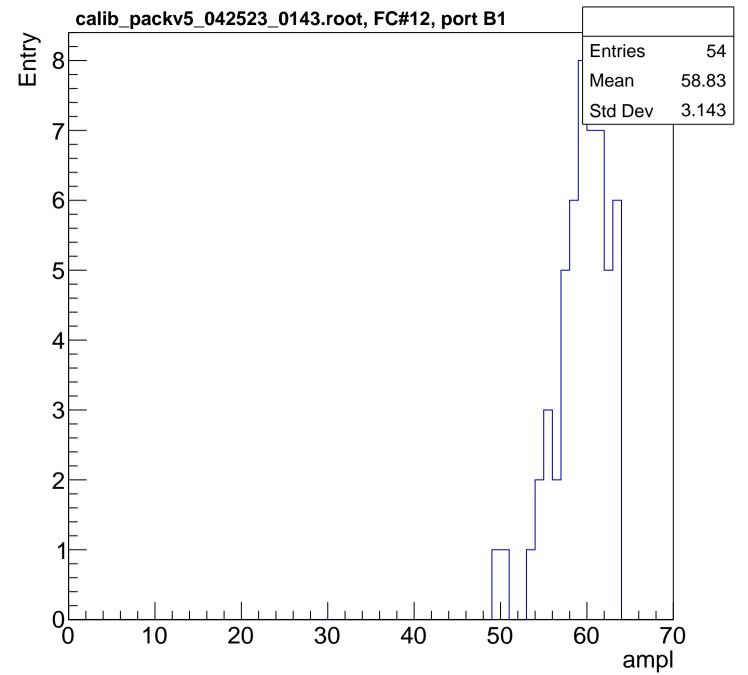


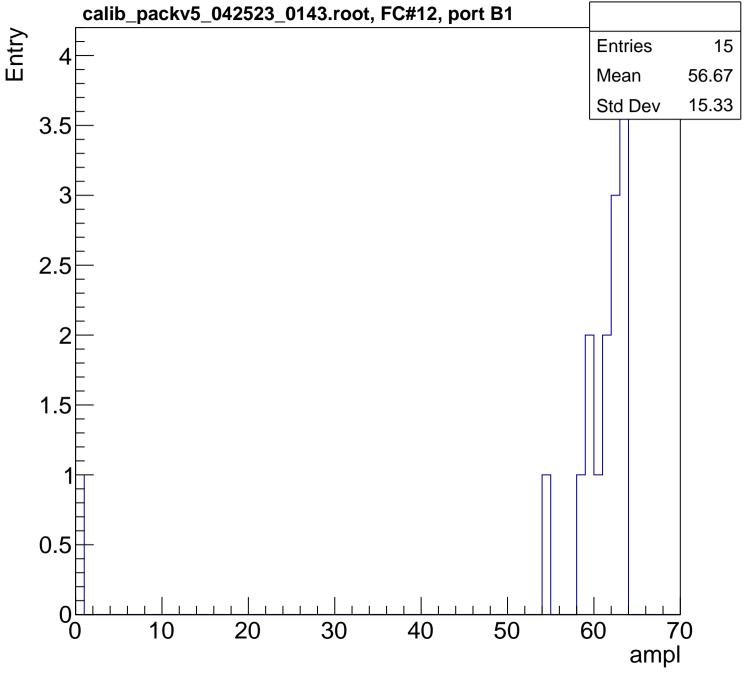


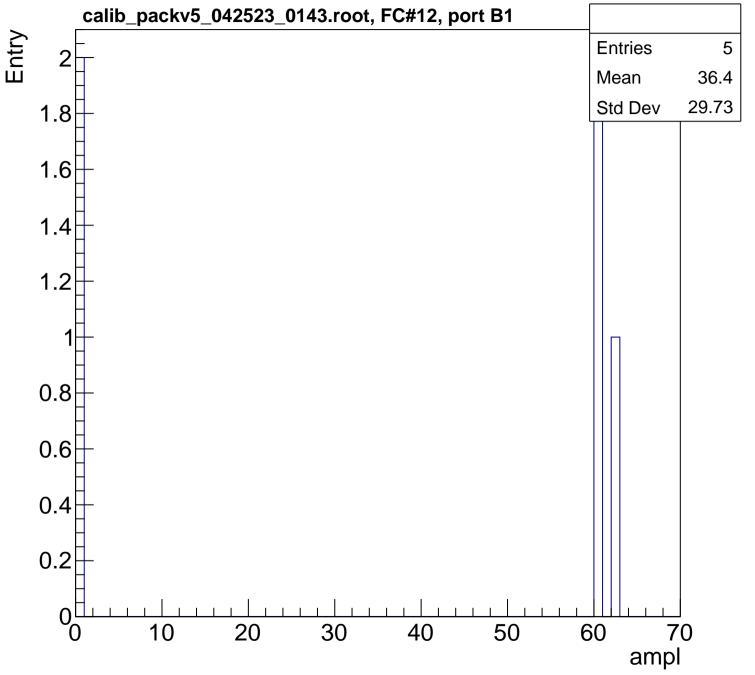


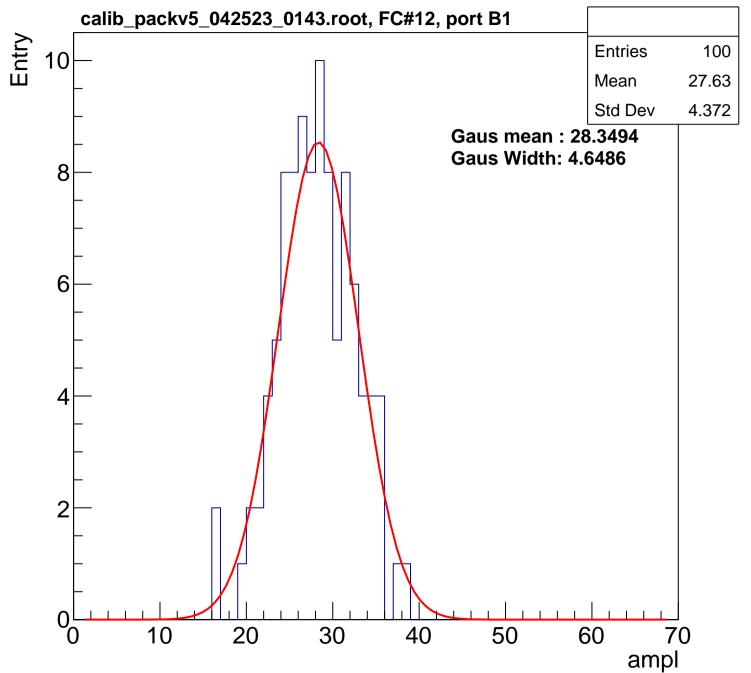


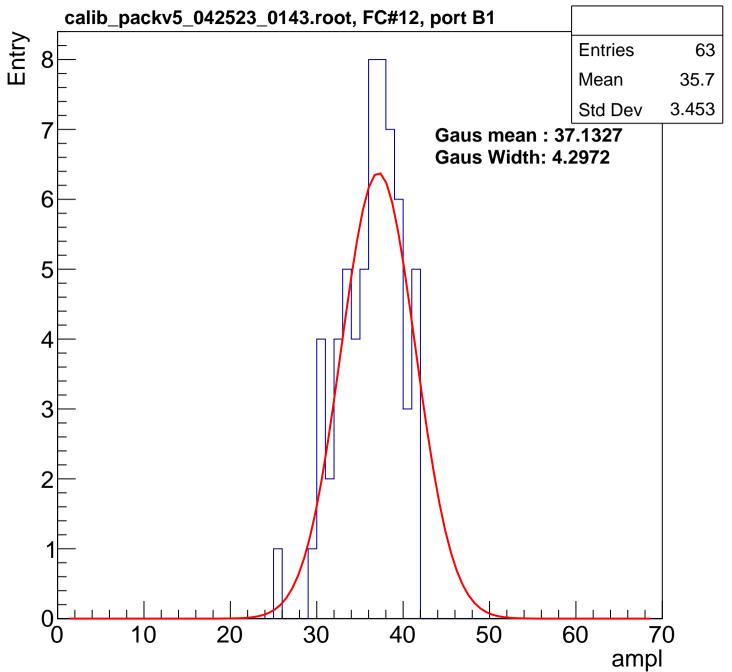


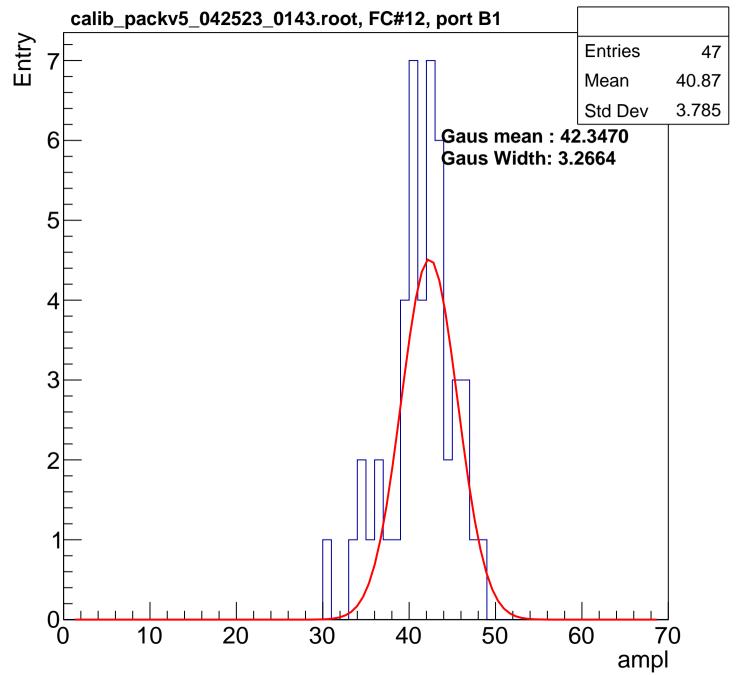


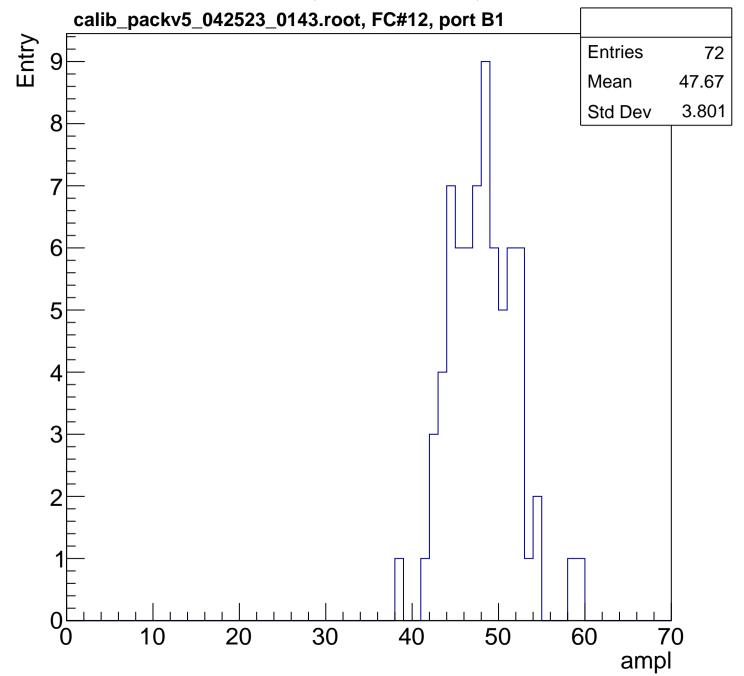


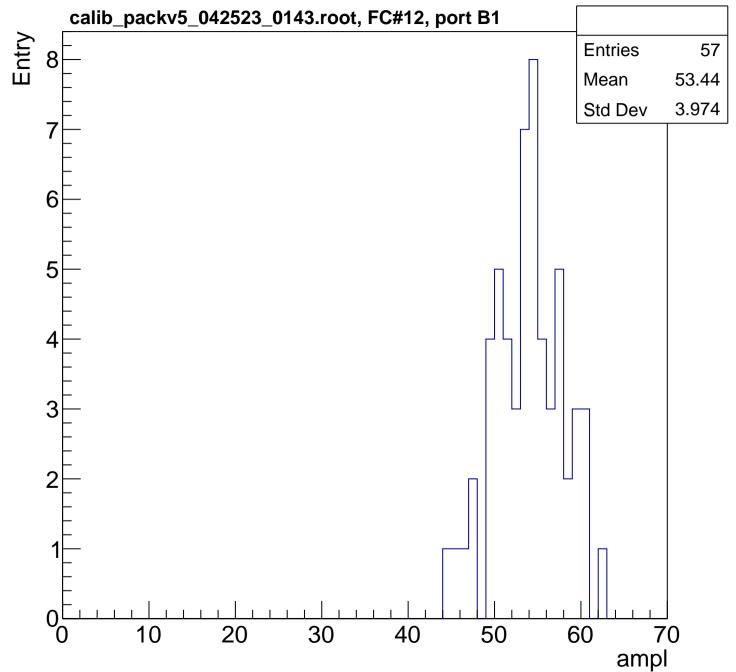


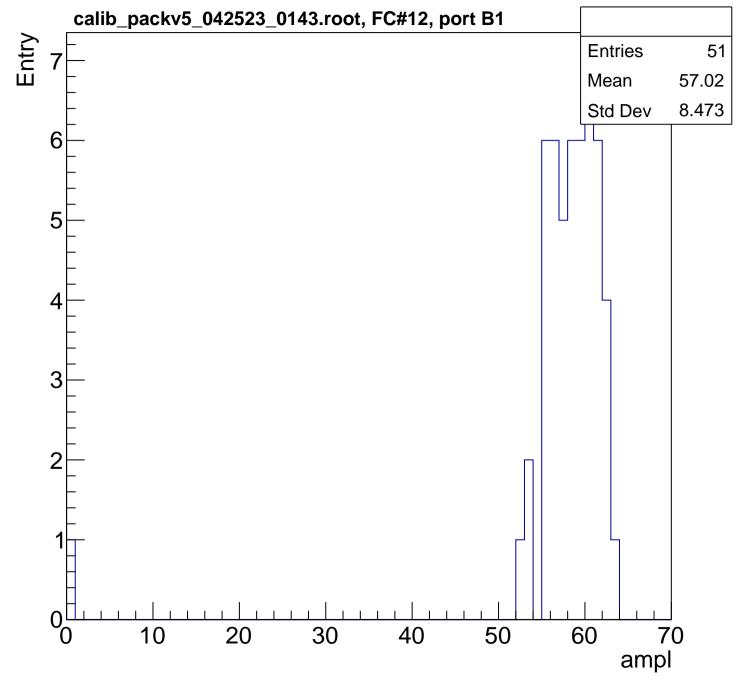


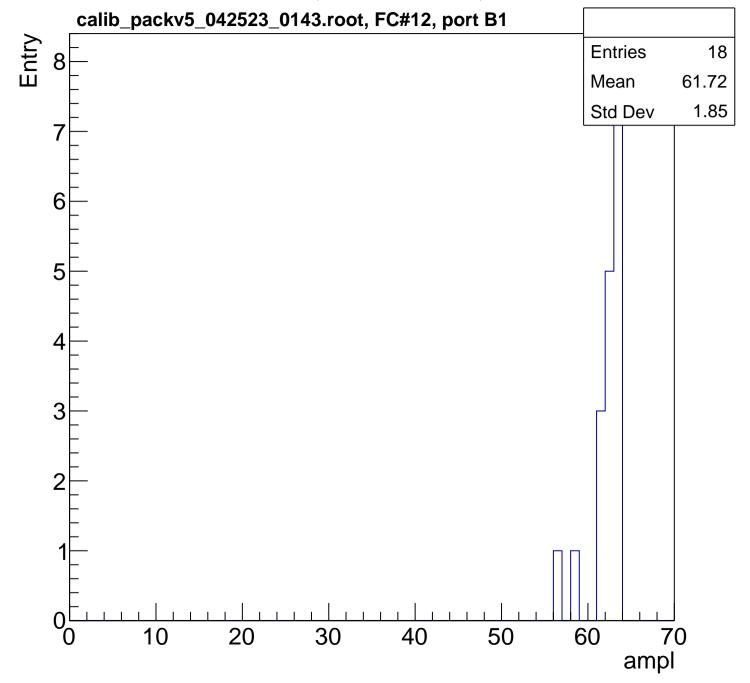


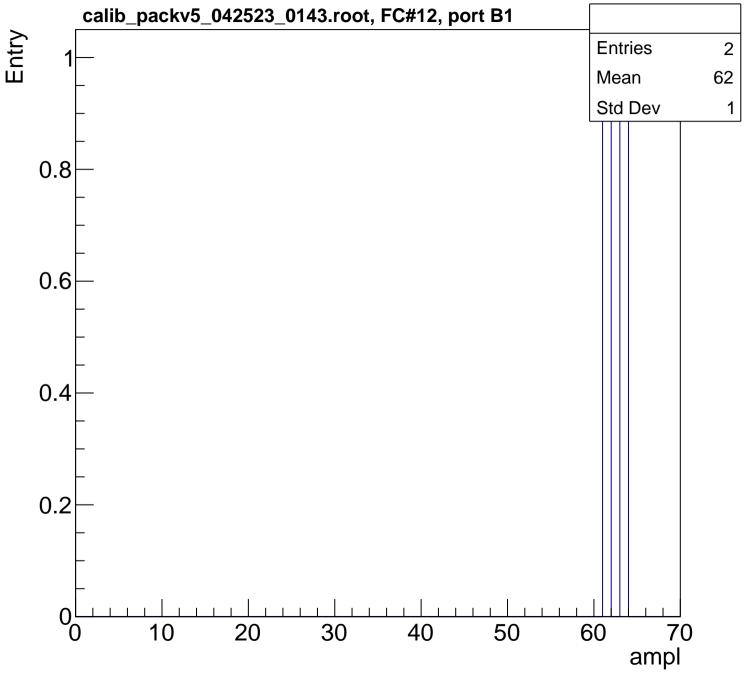


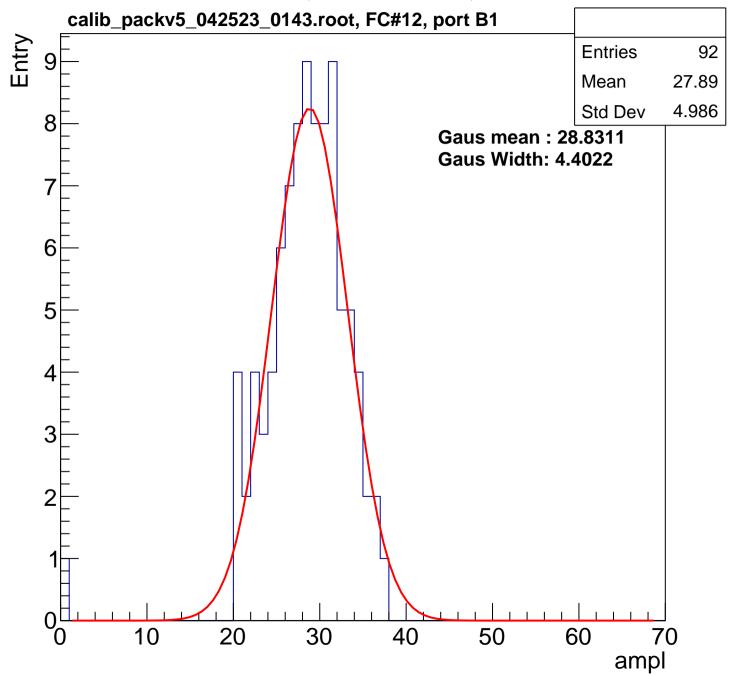


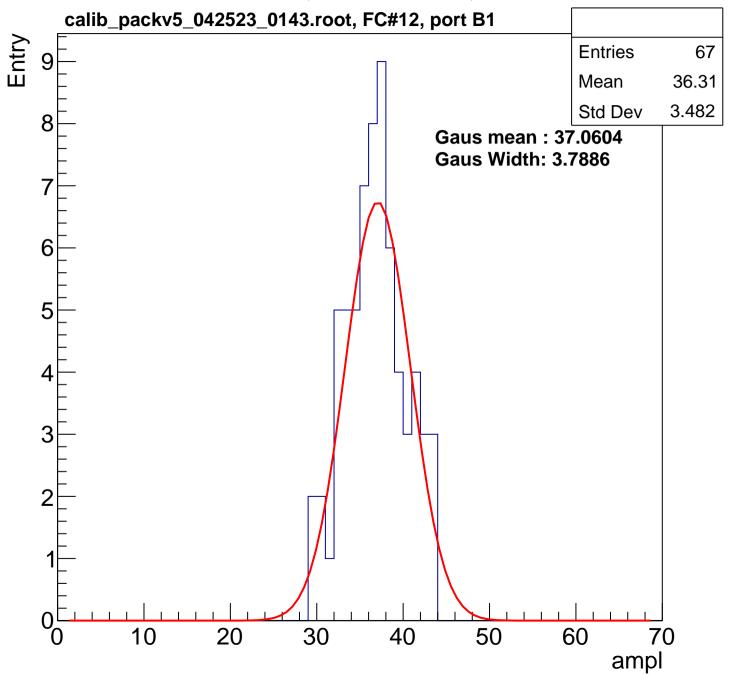


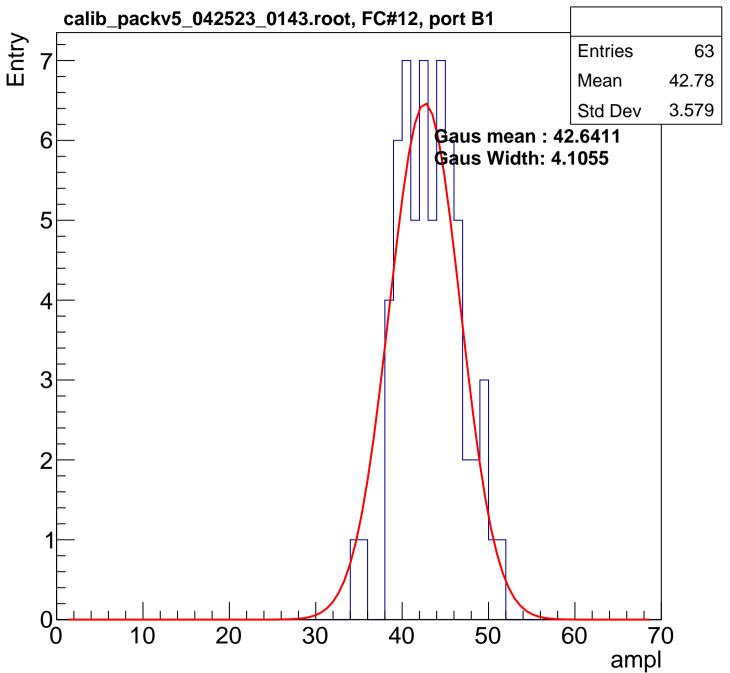


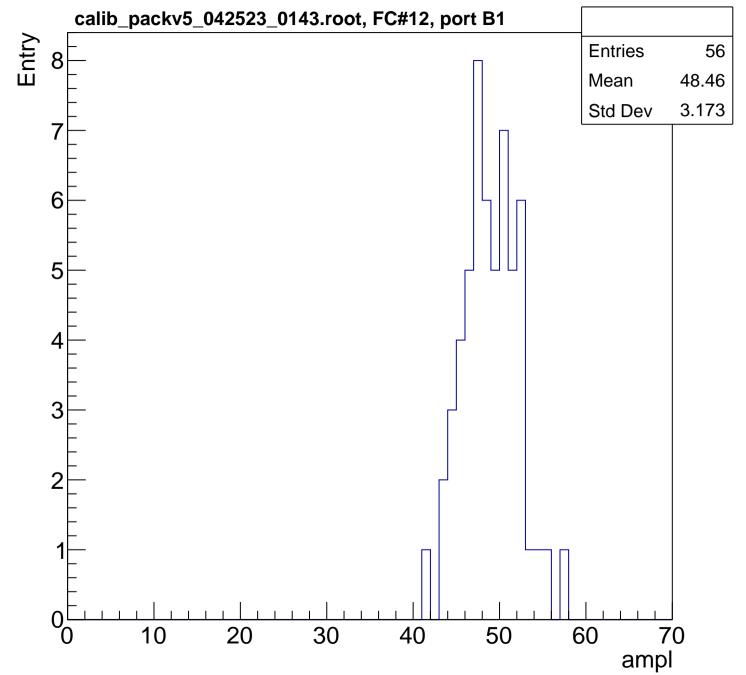


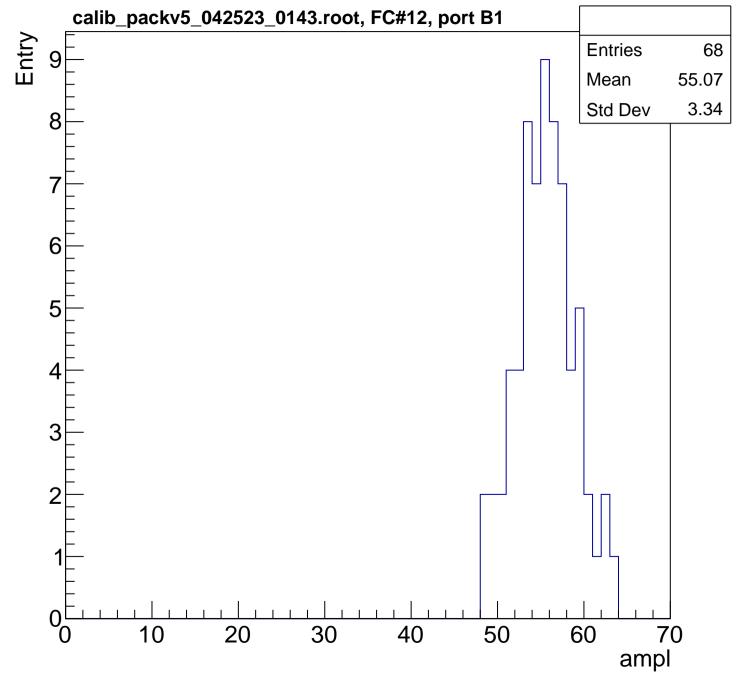


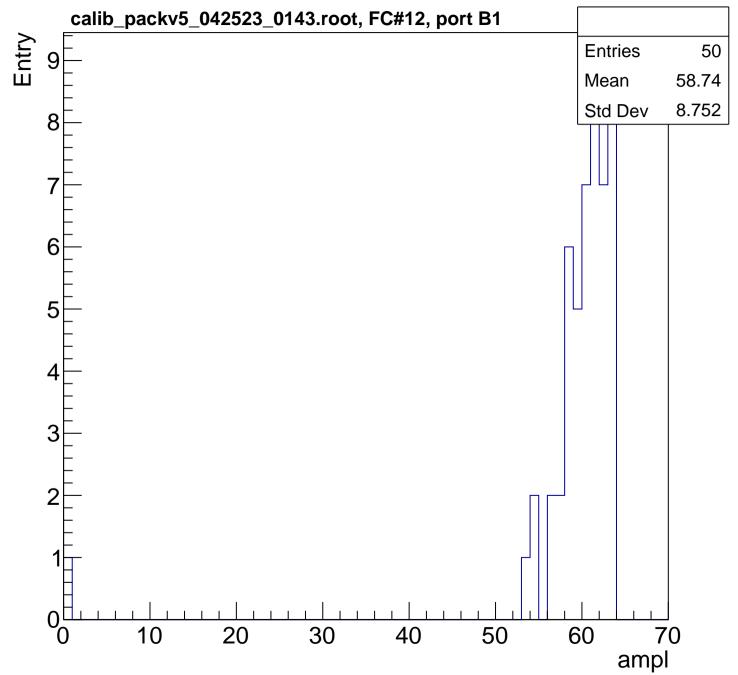


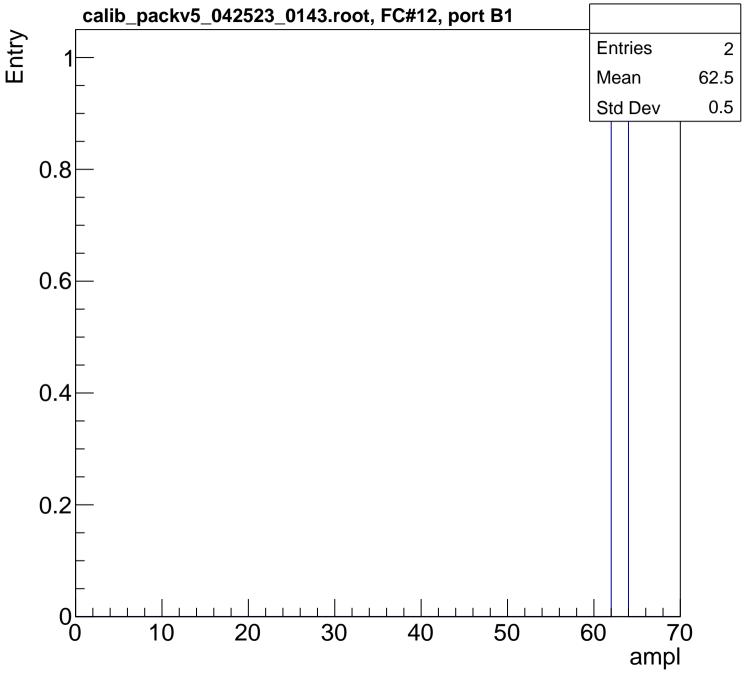




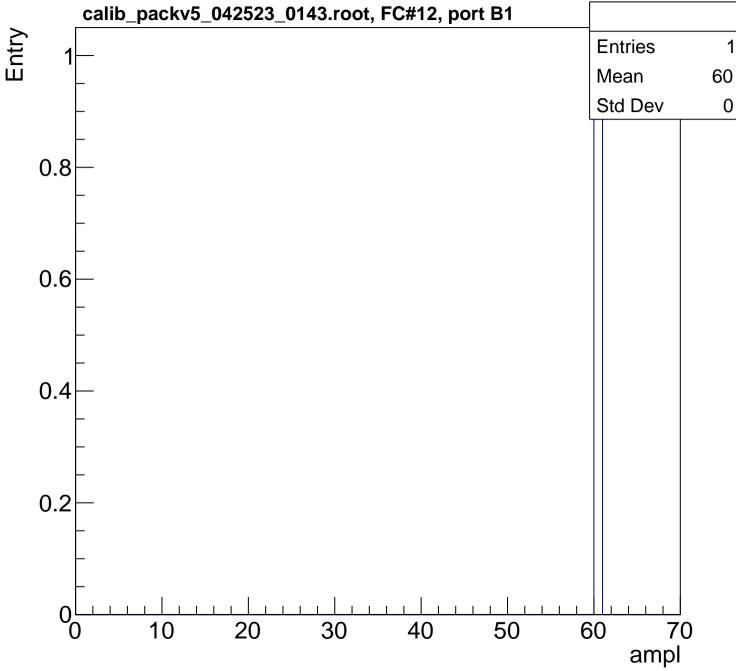


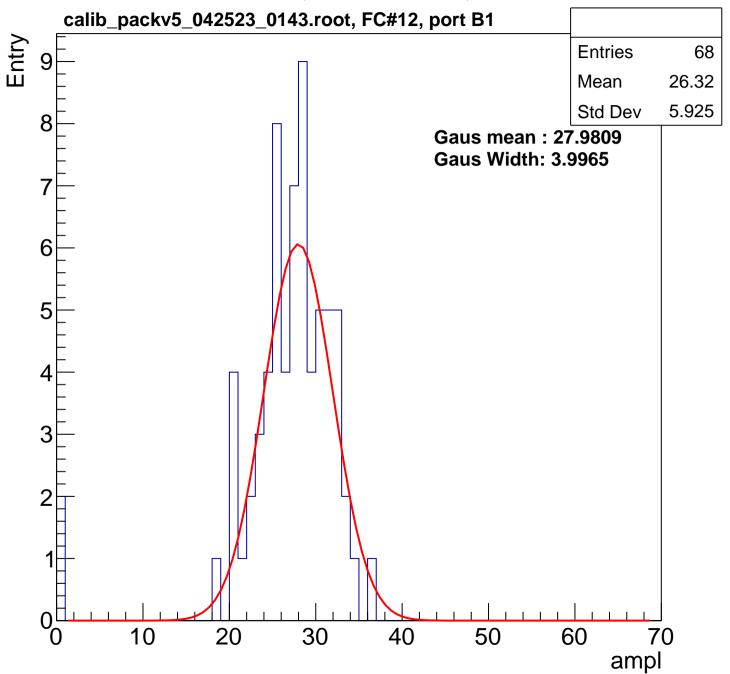


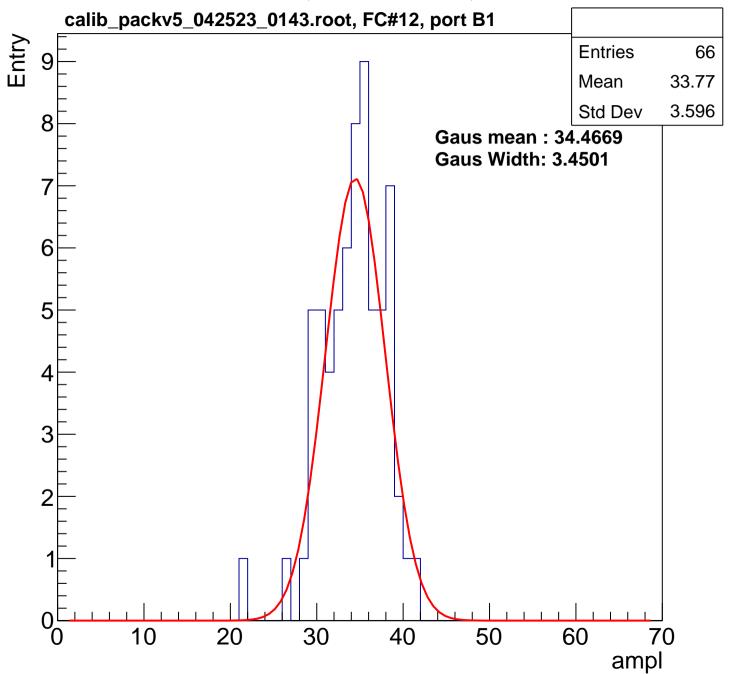


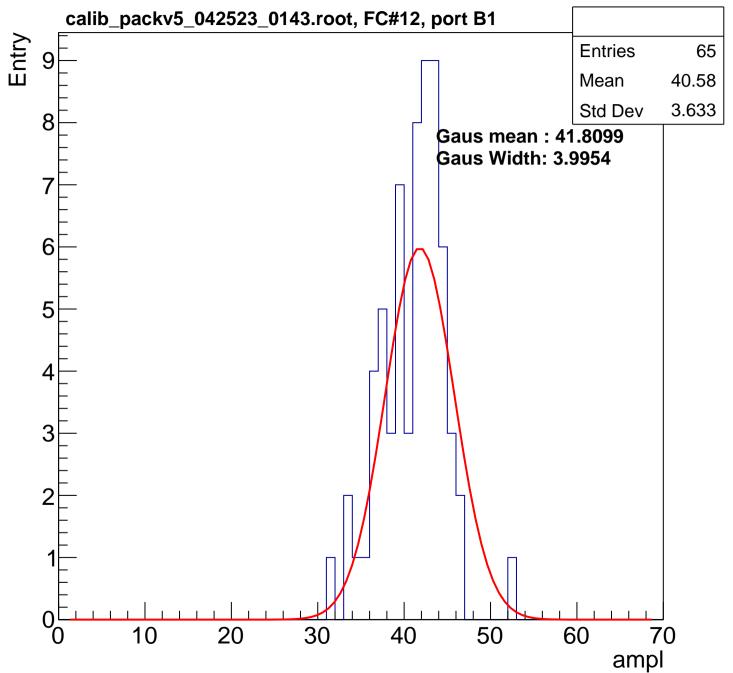


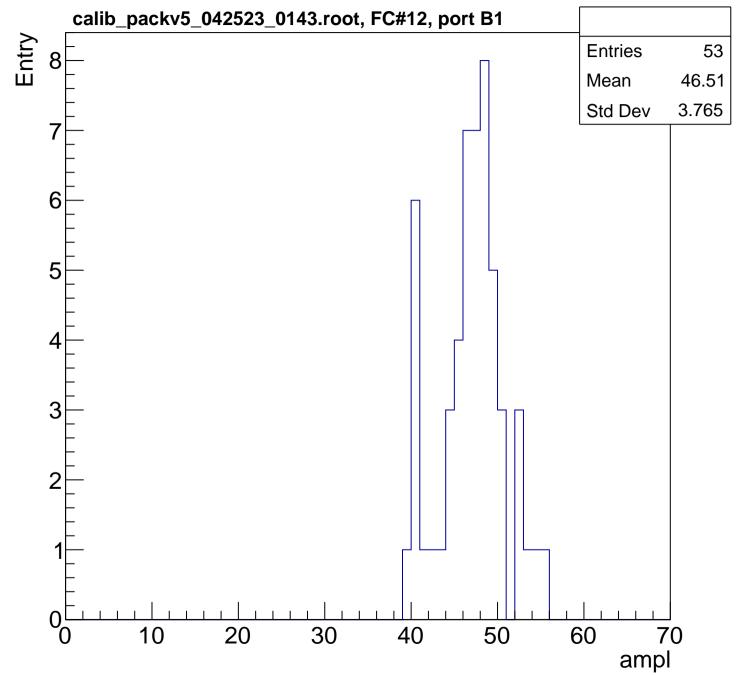
0

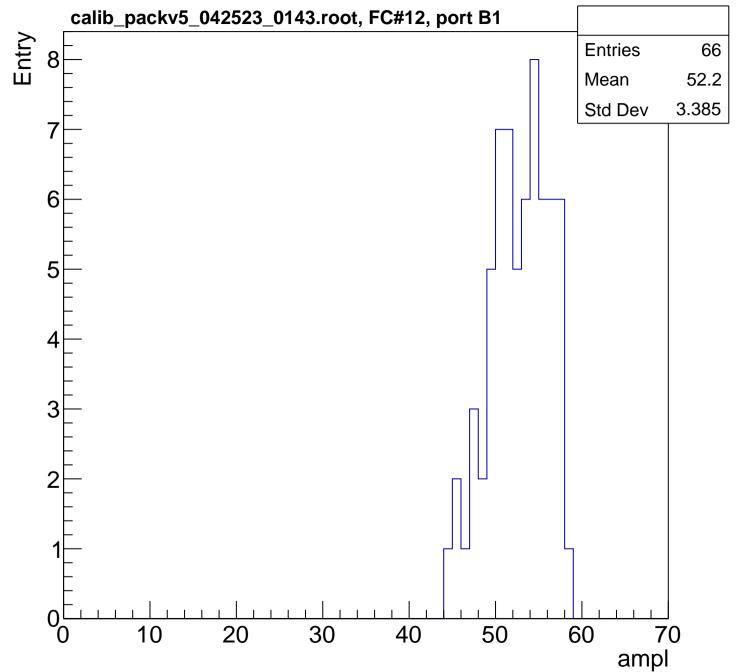


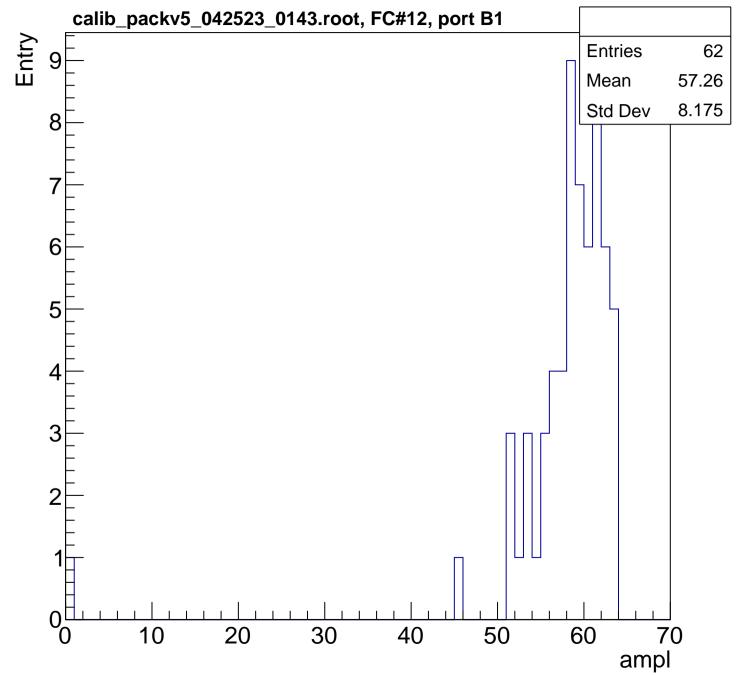


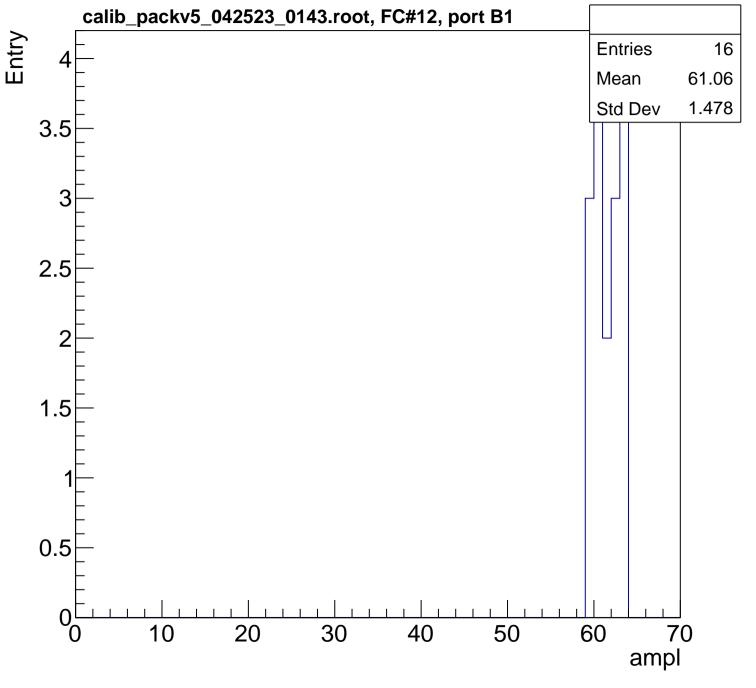


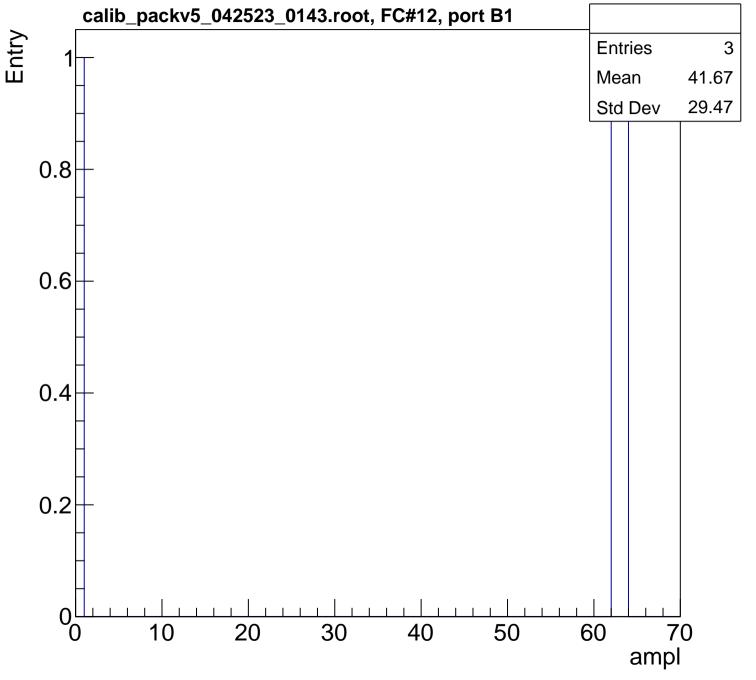


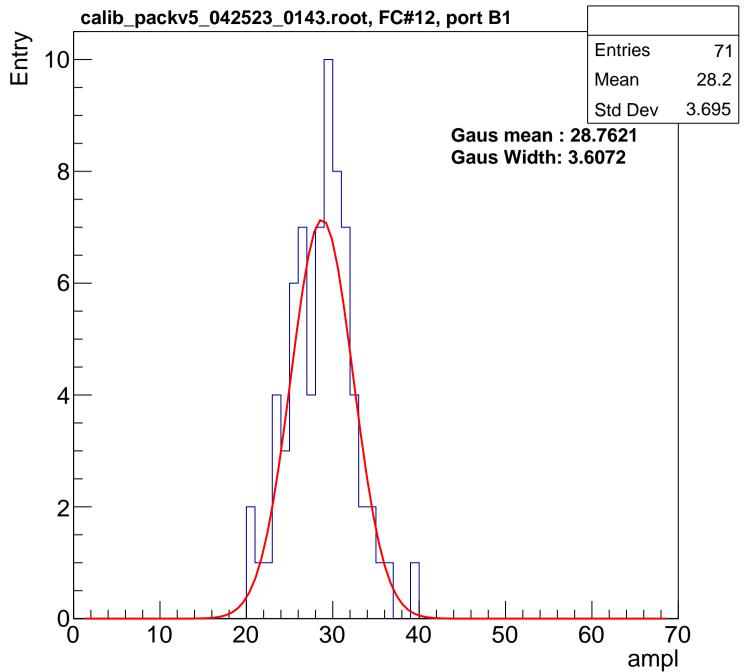


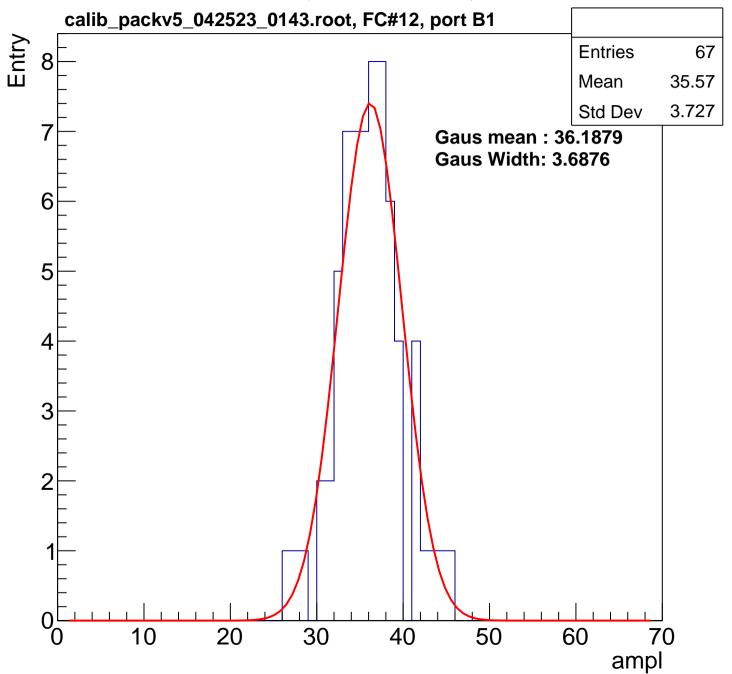


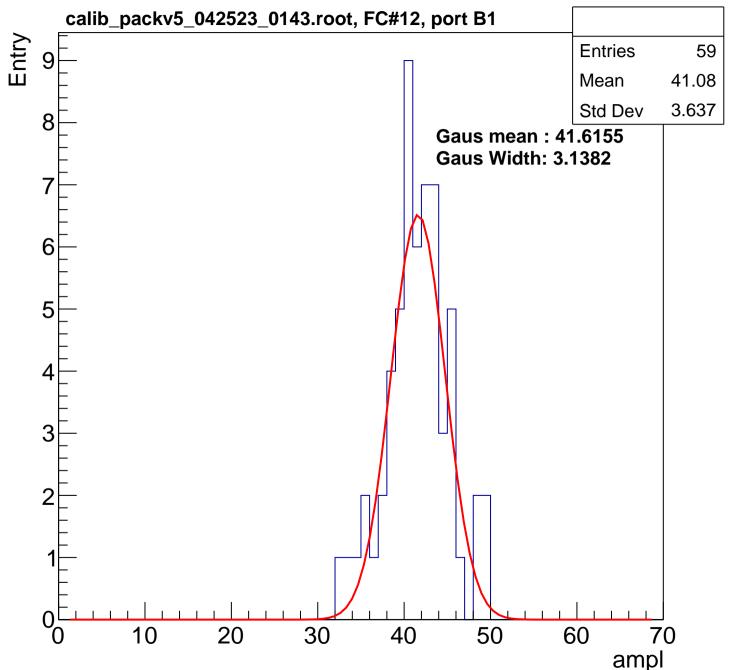


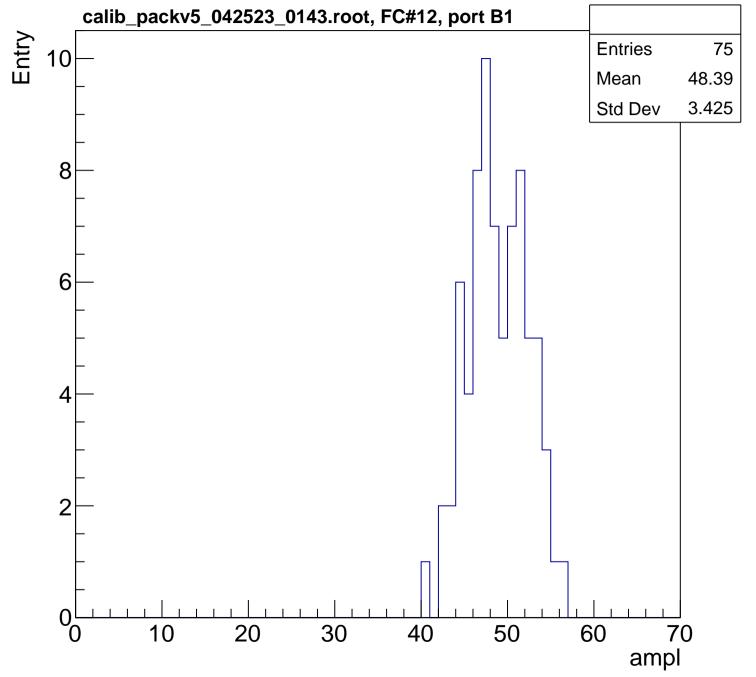


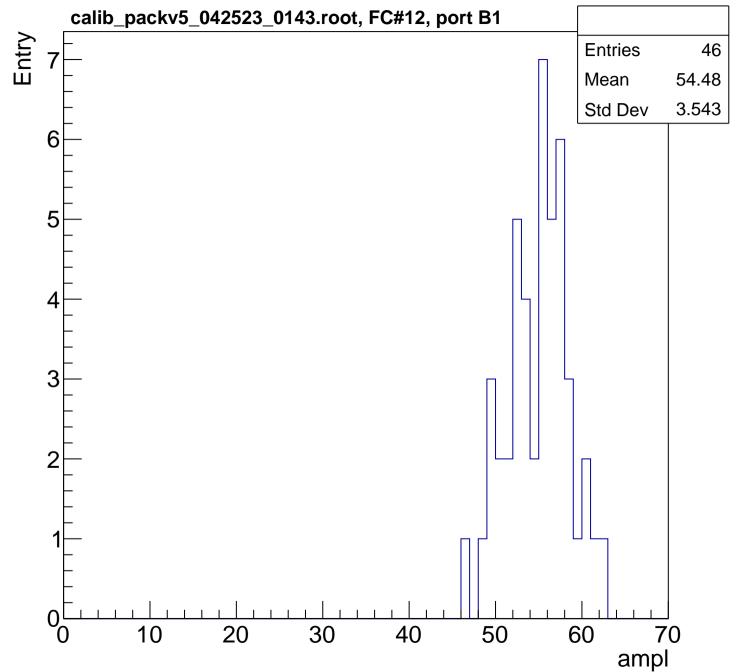


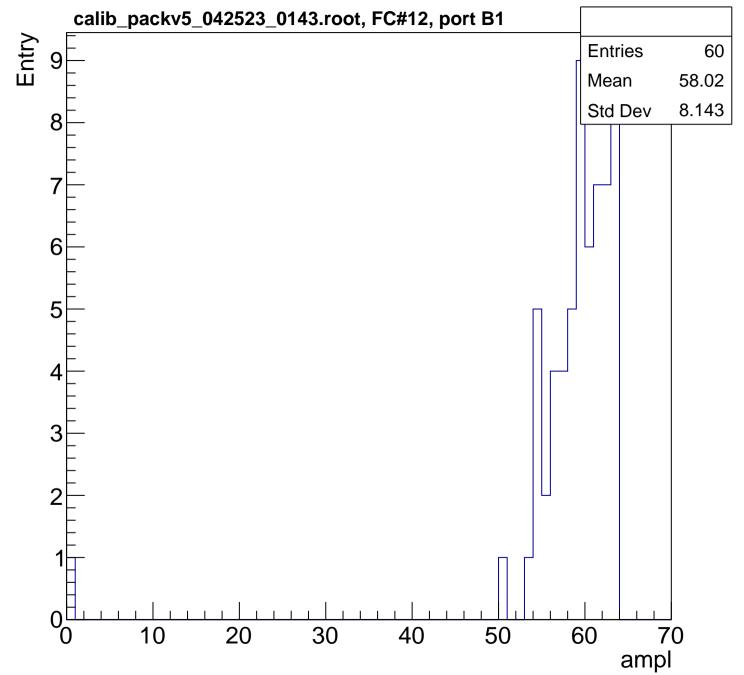


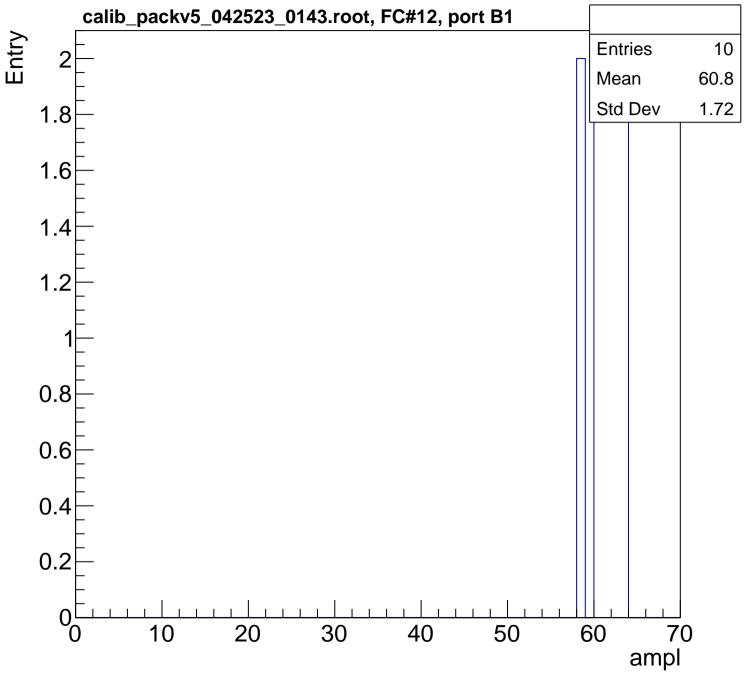


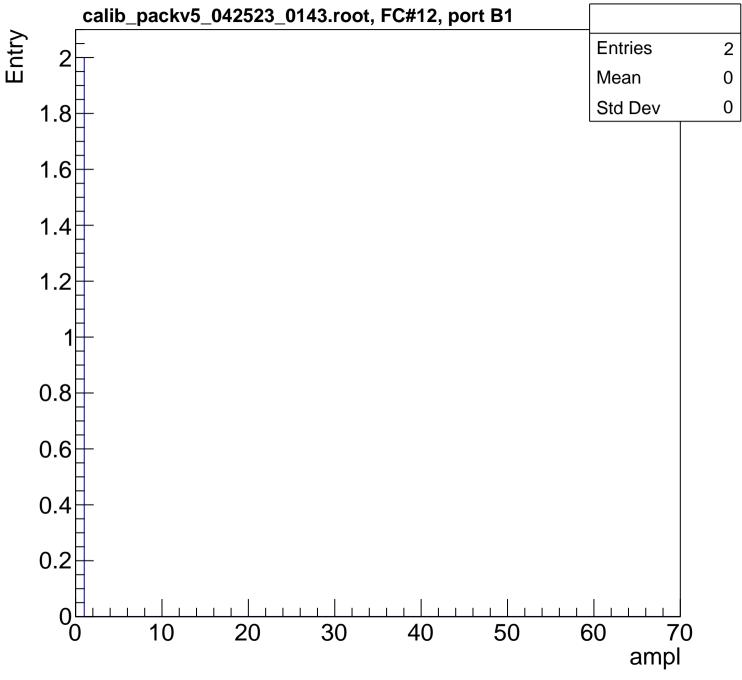


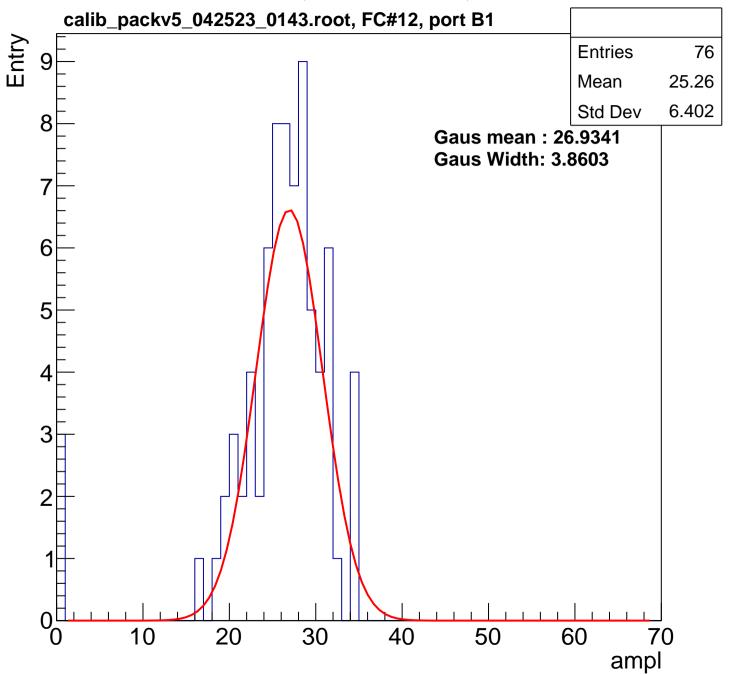


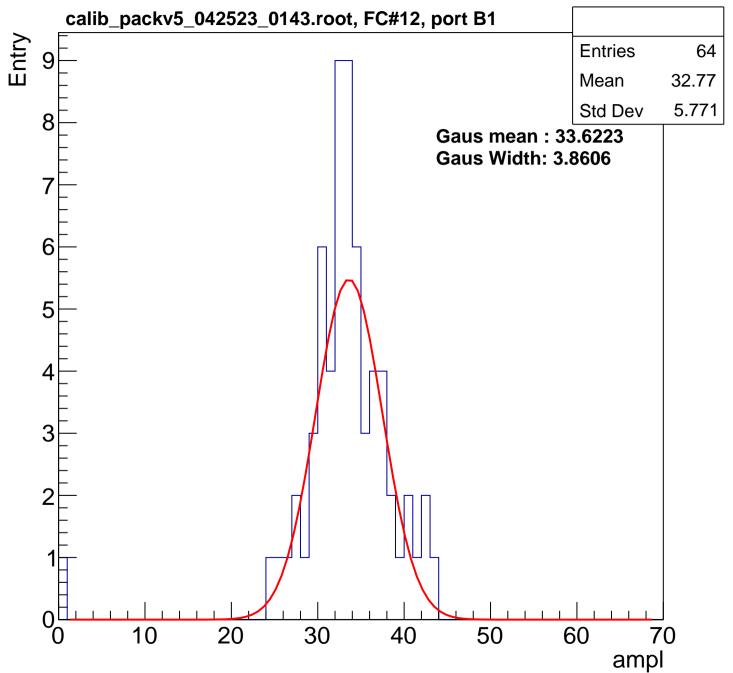


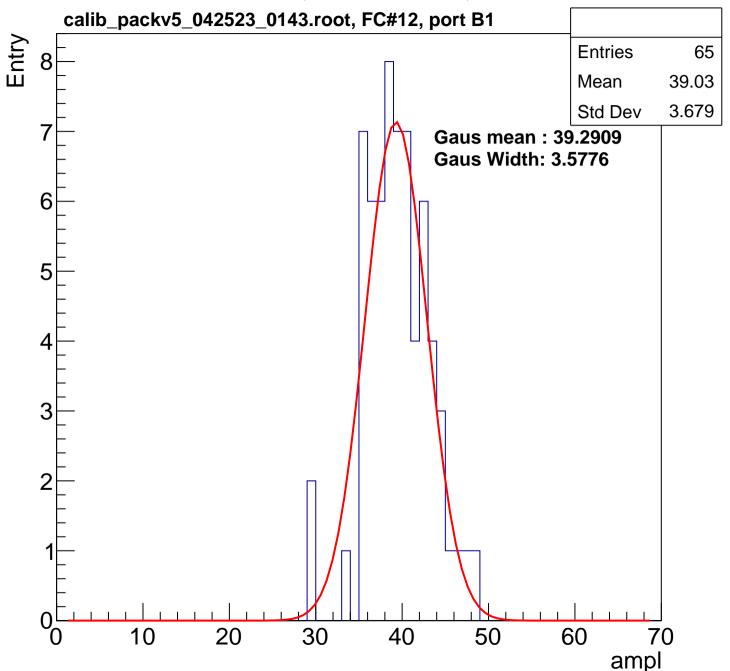


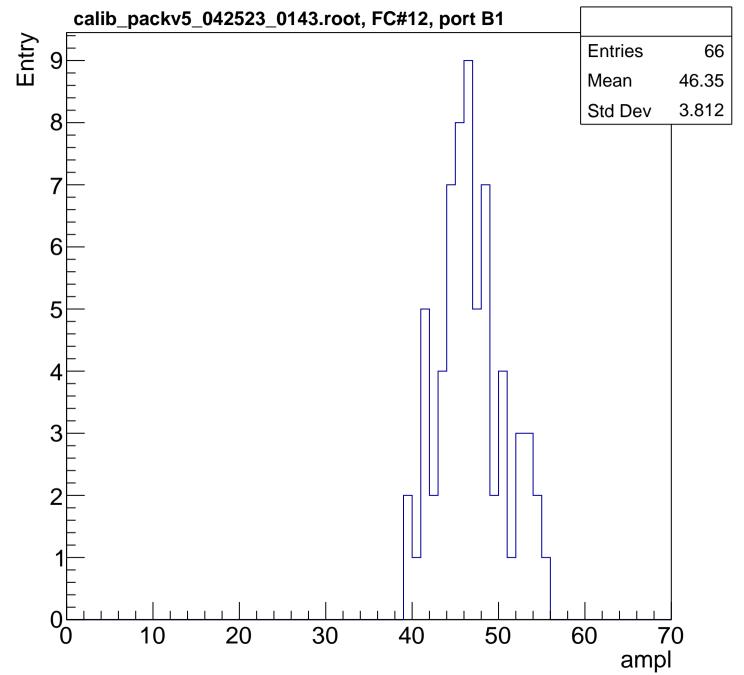


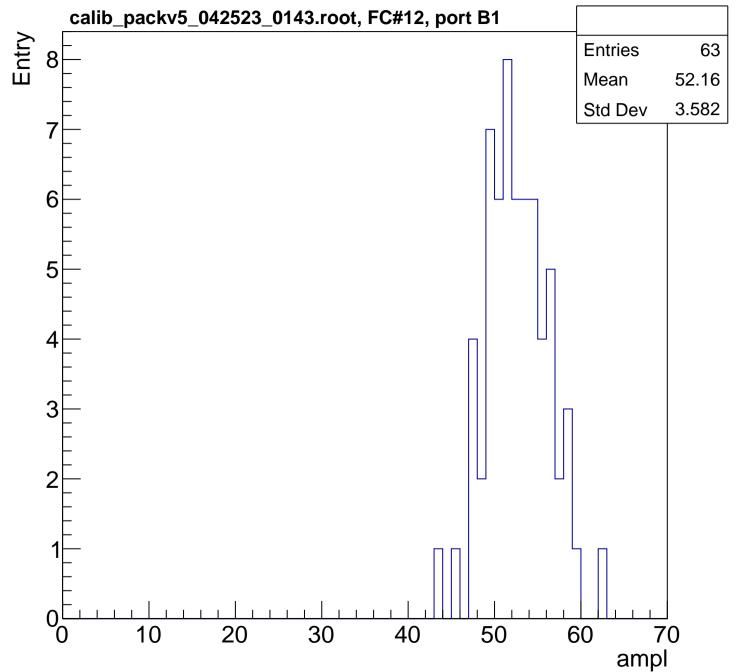


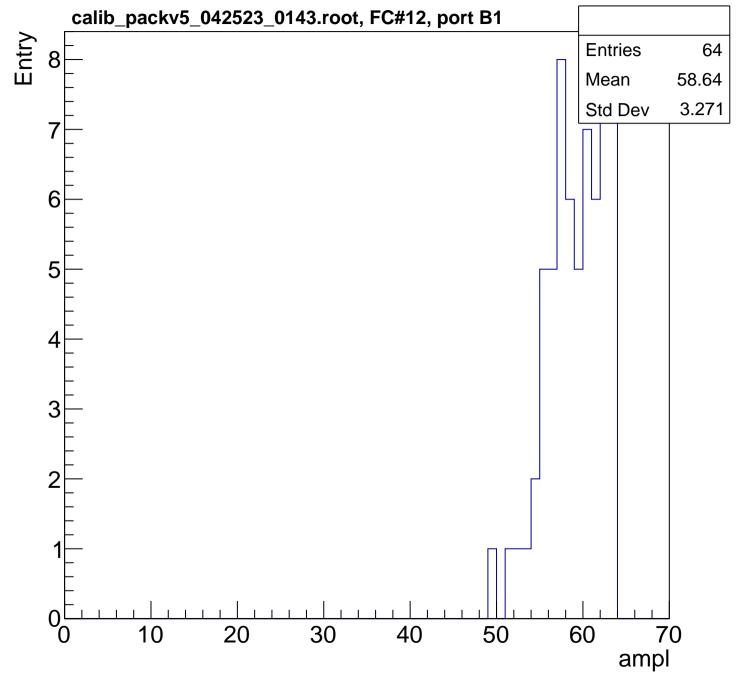


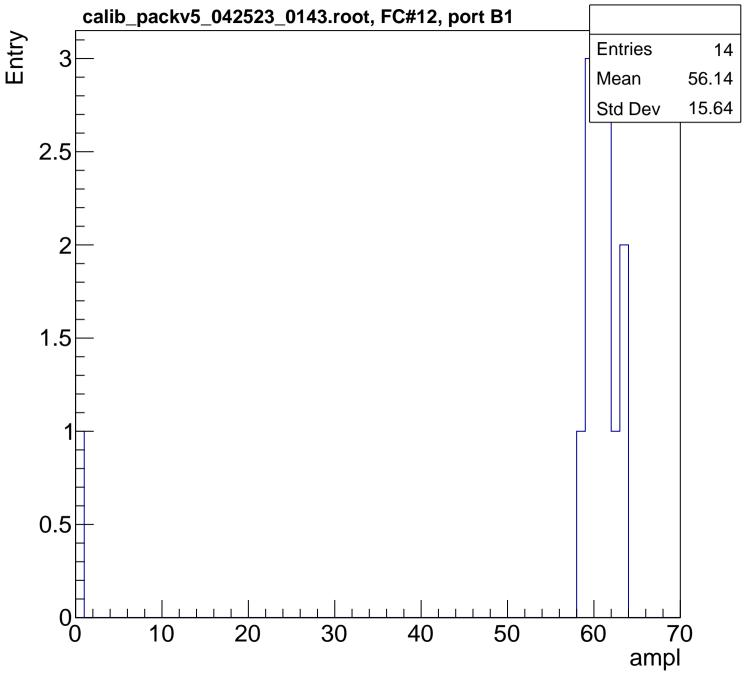


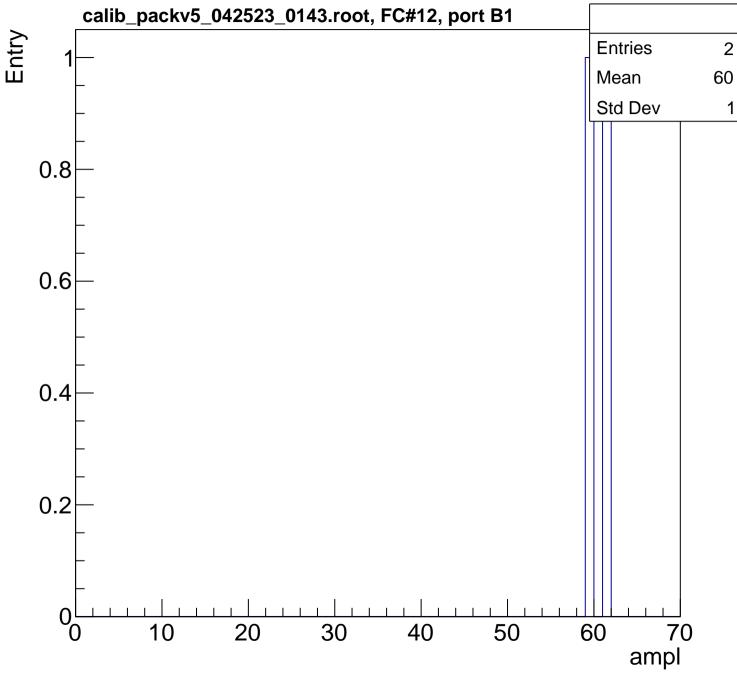


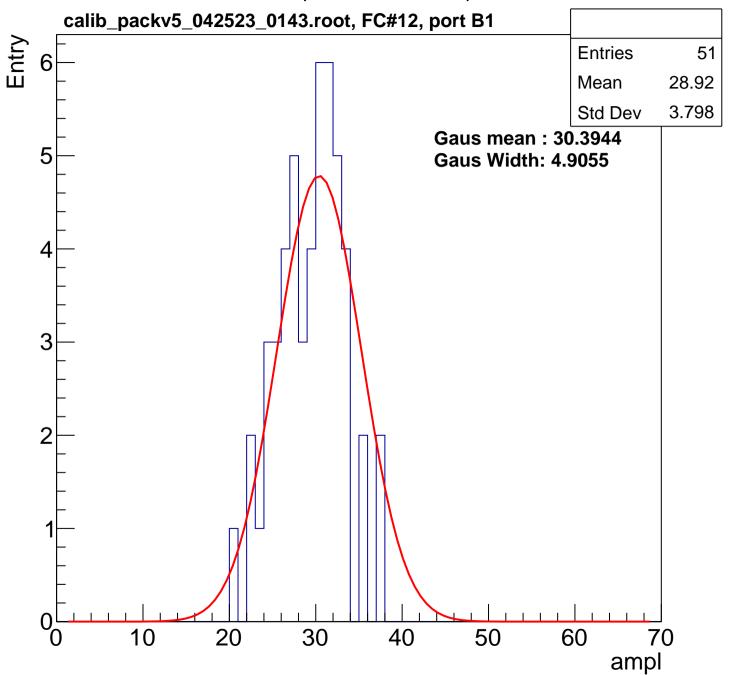


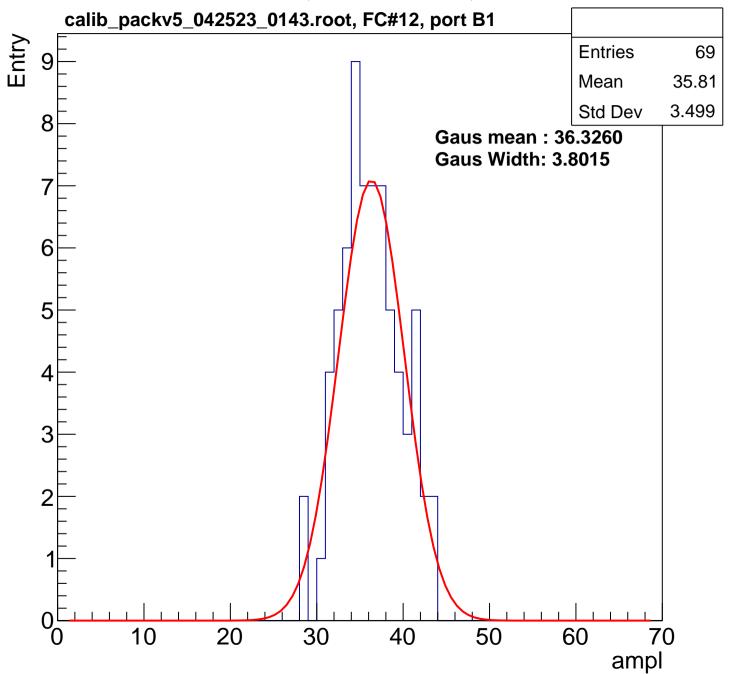


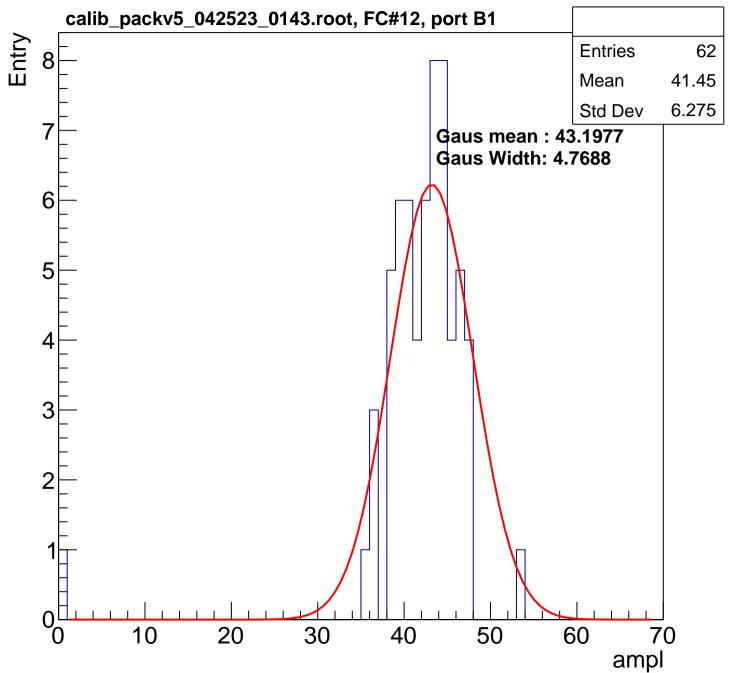


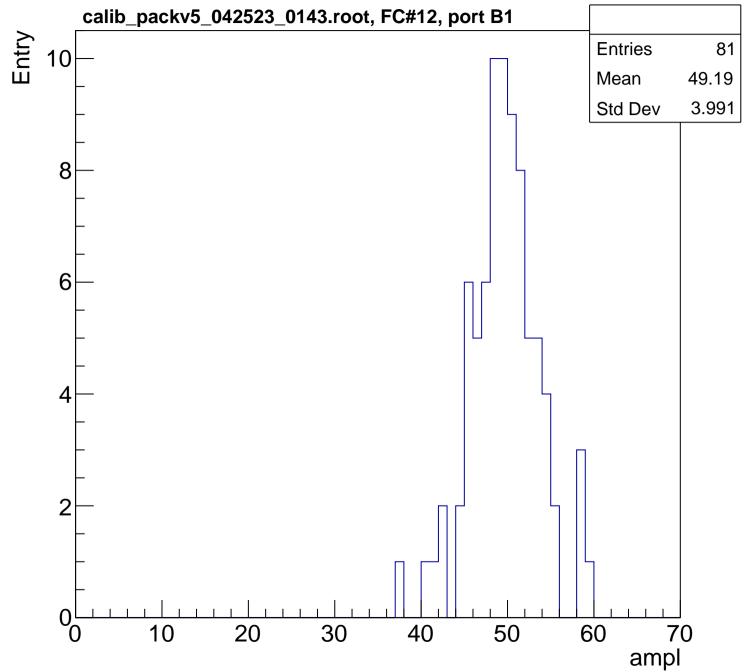


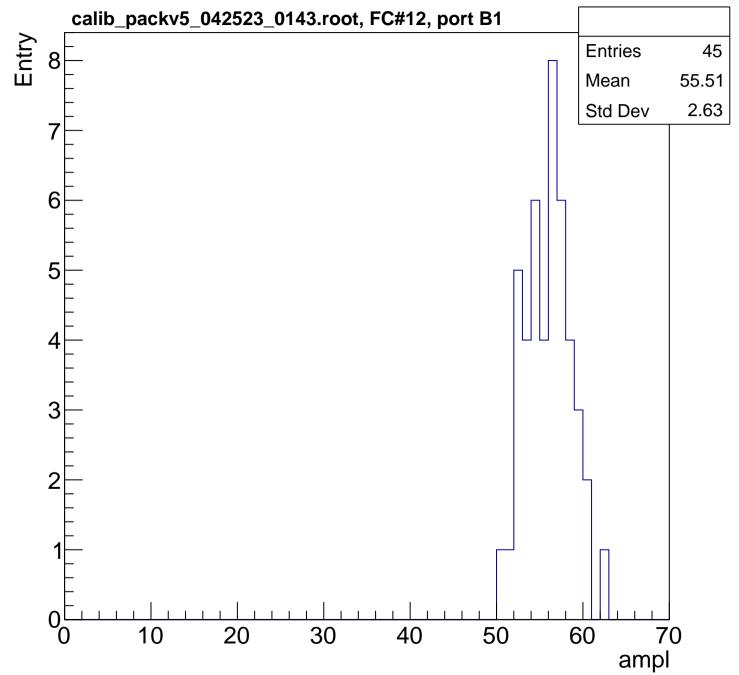


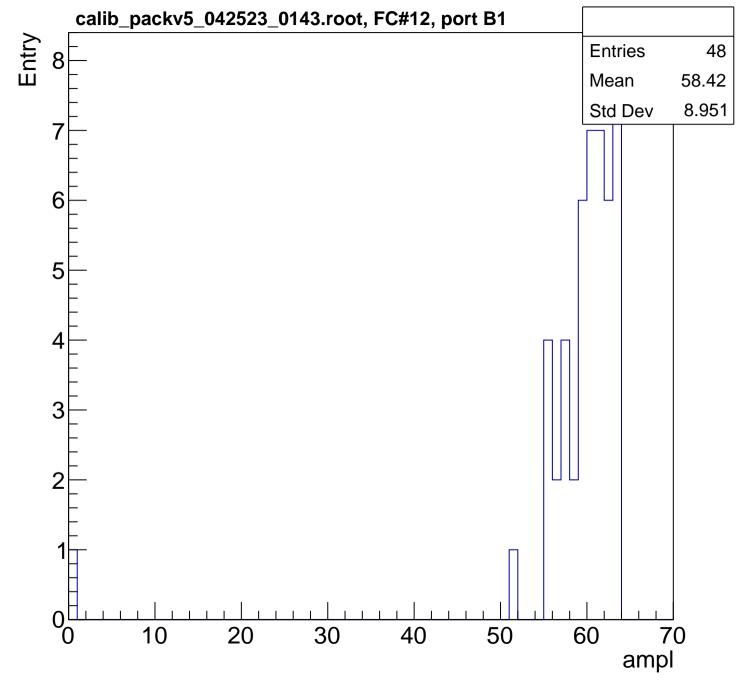


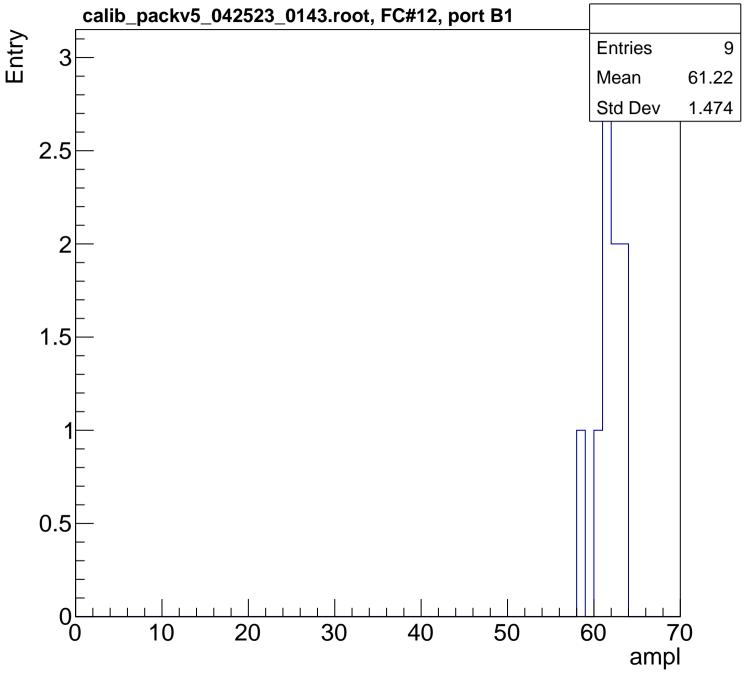


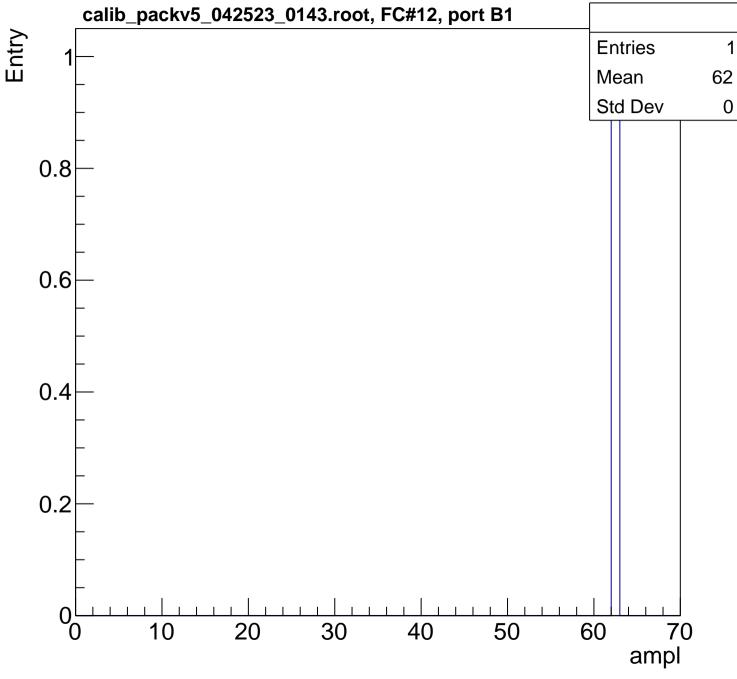


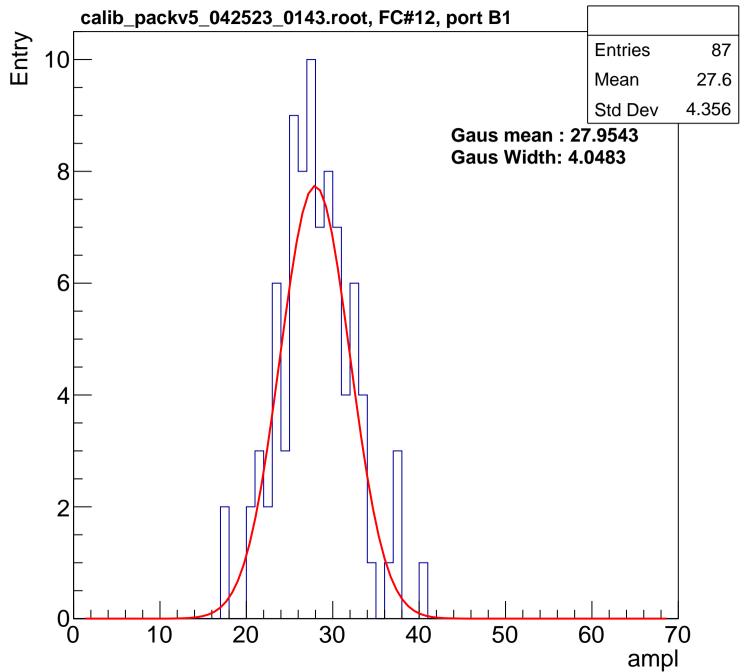


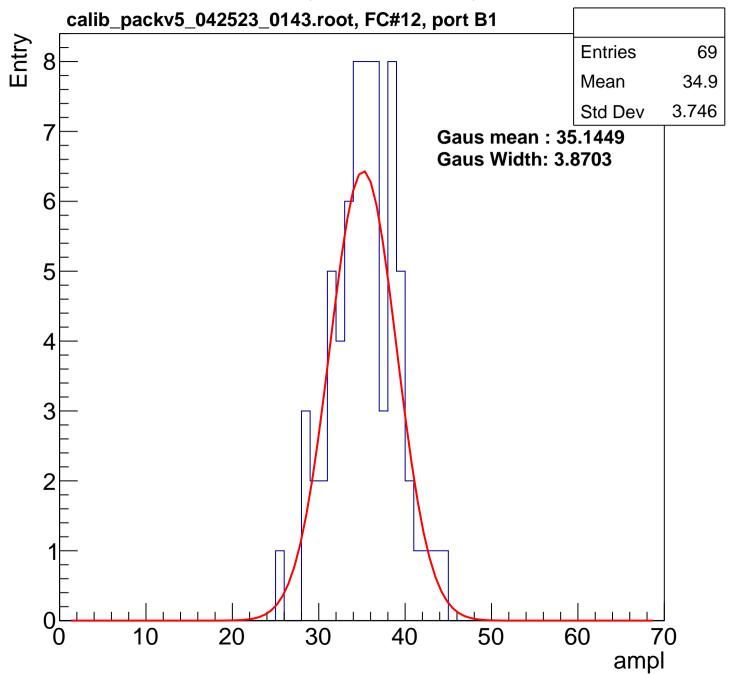


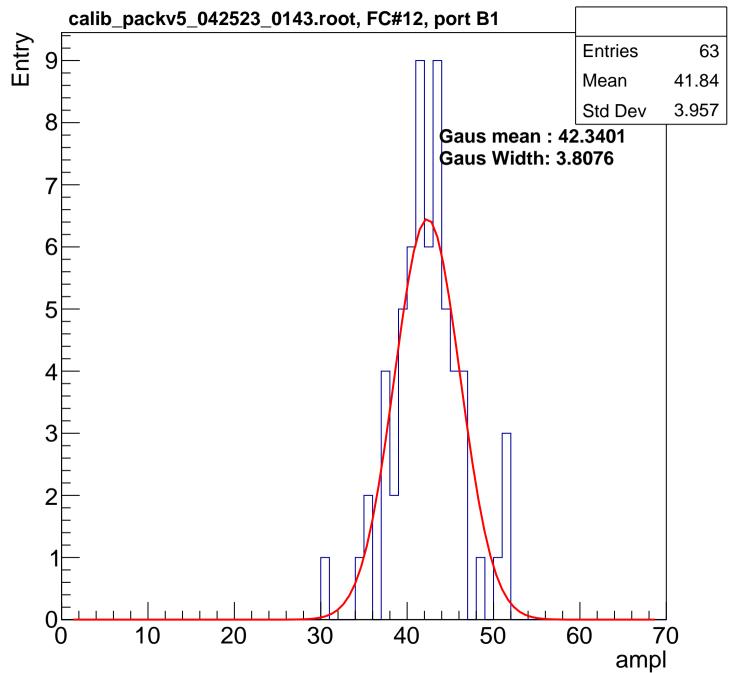


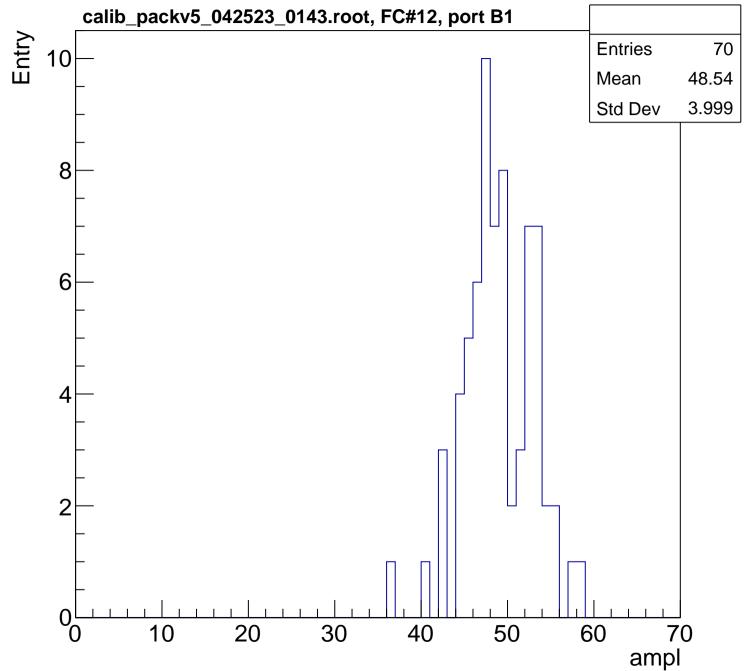


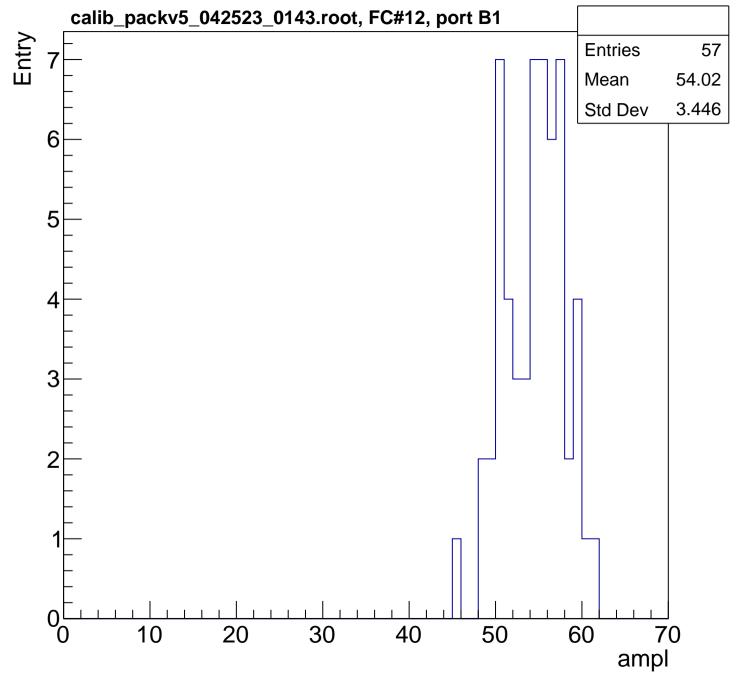


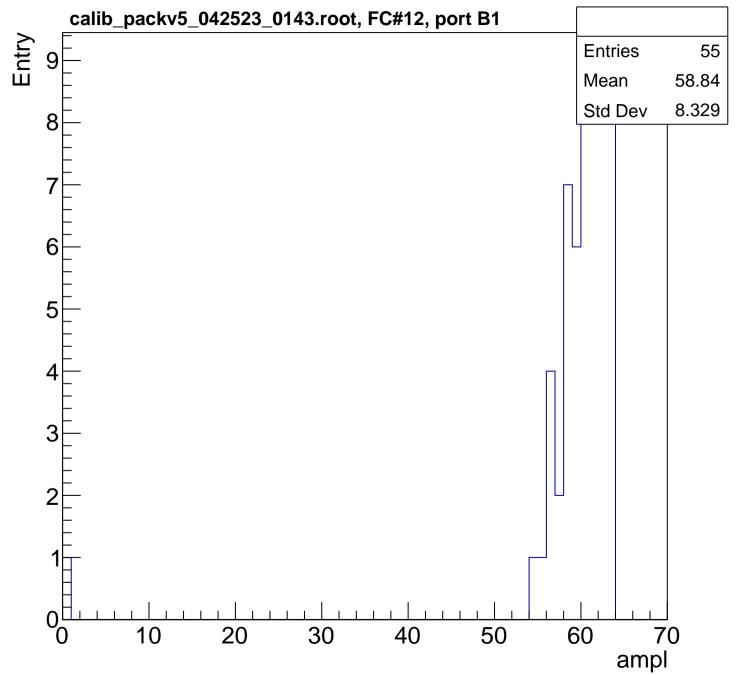


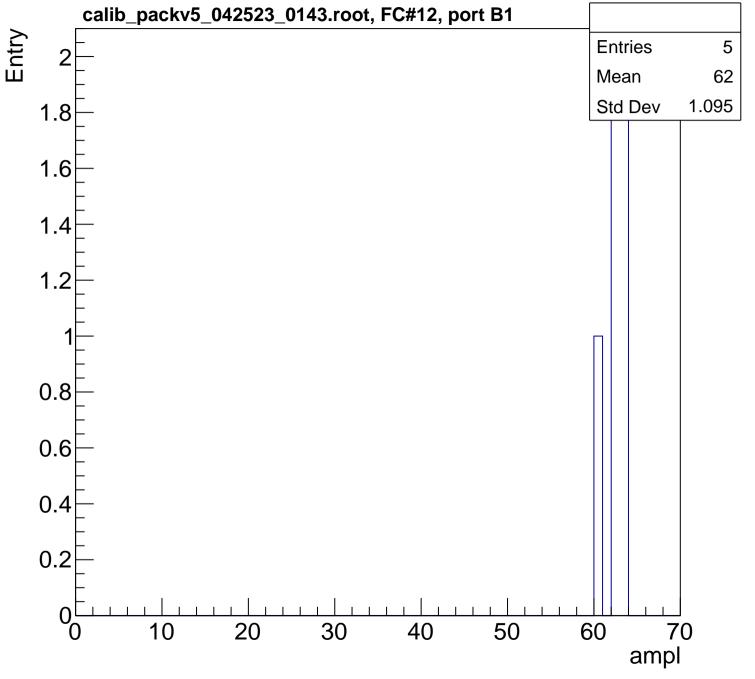


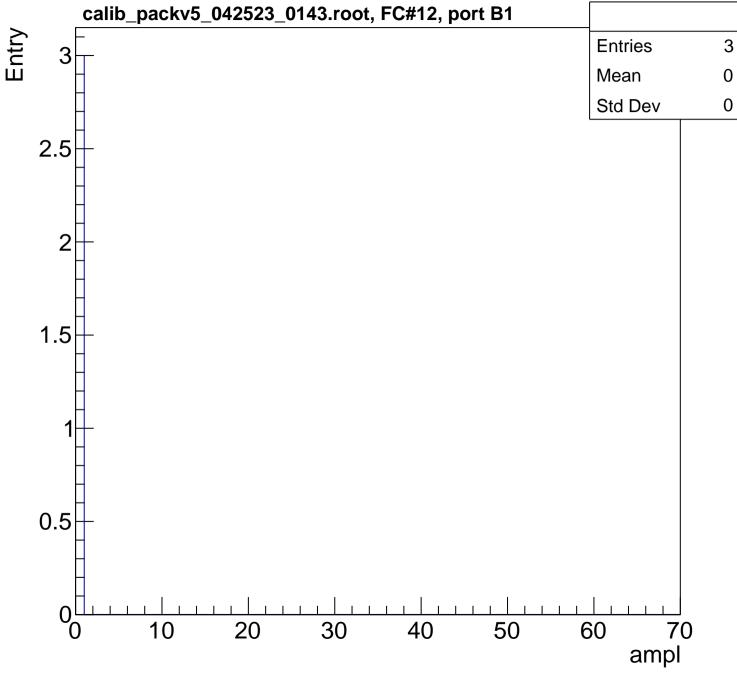


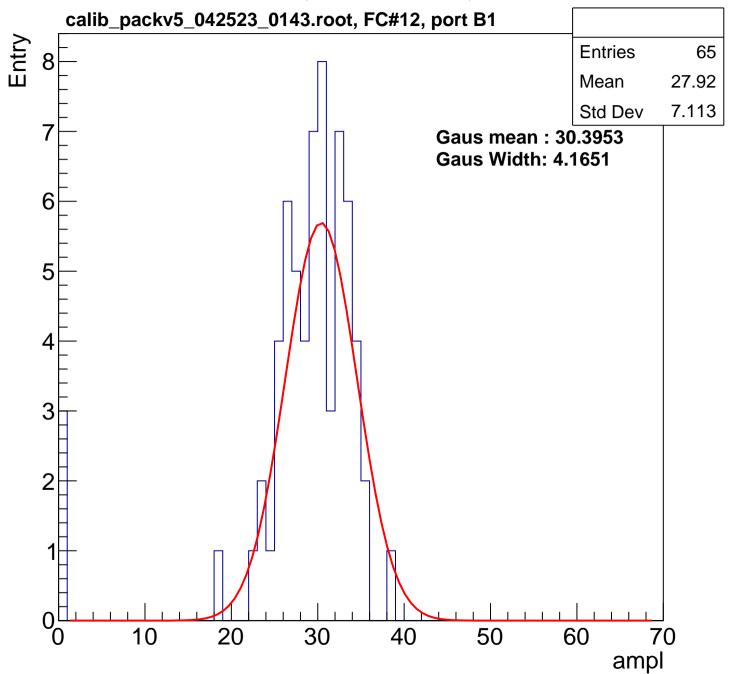


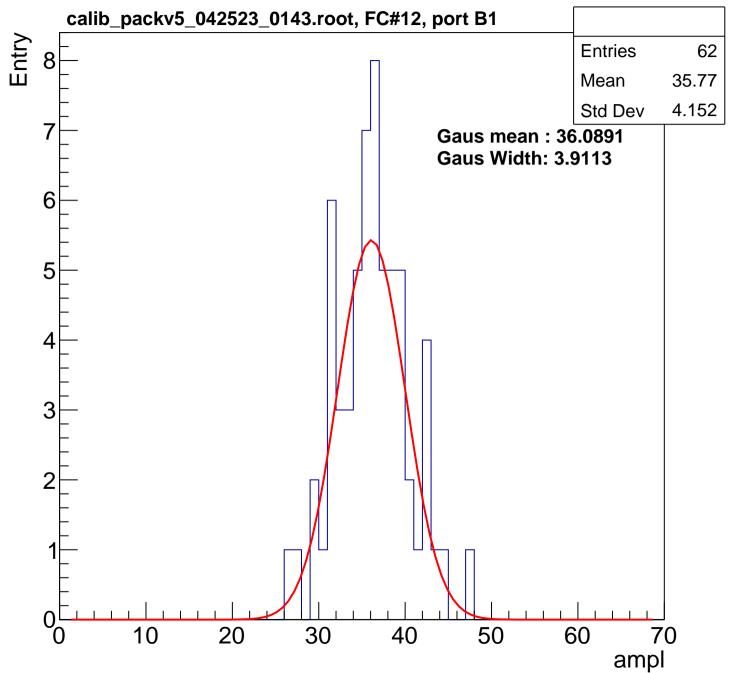


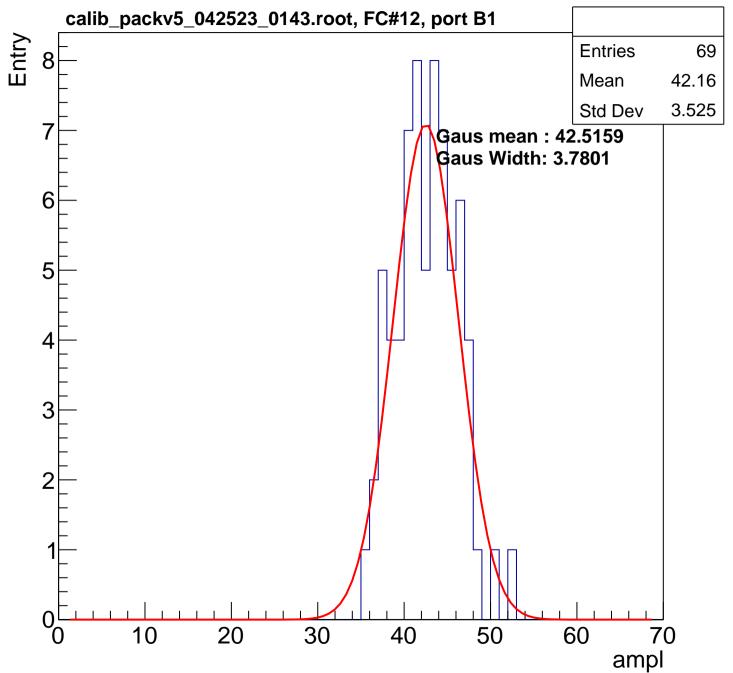


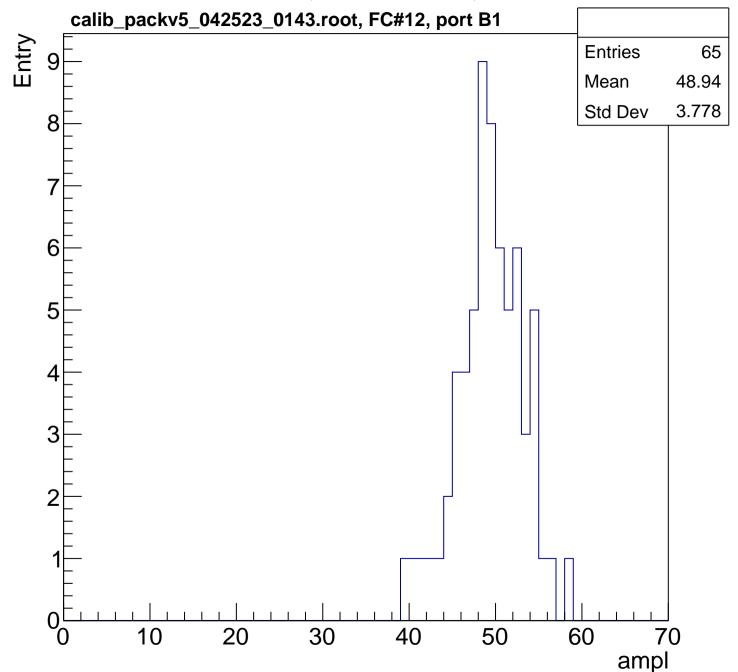


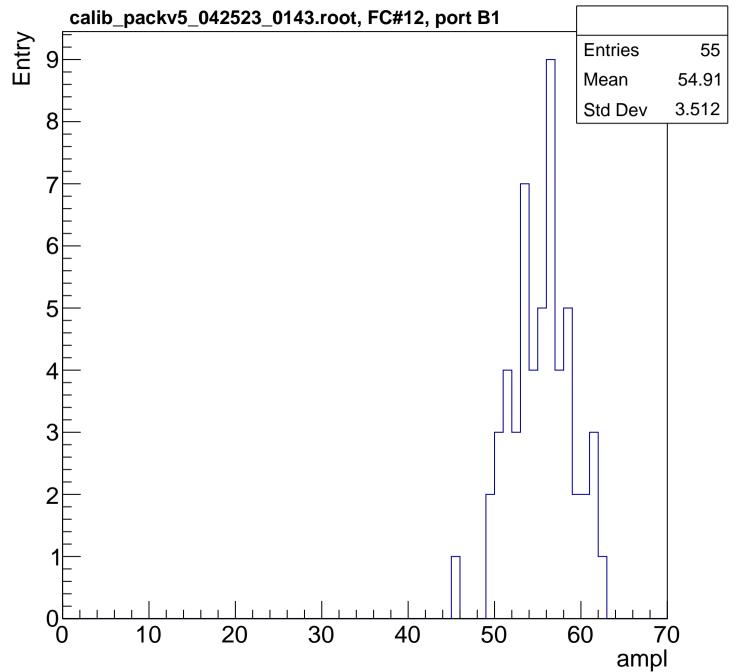


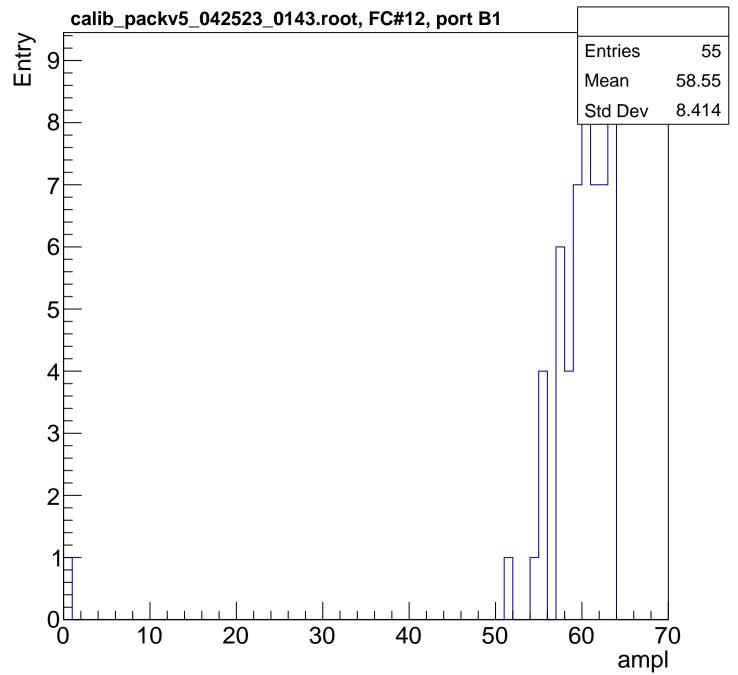


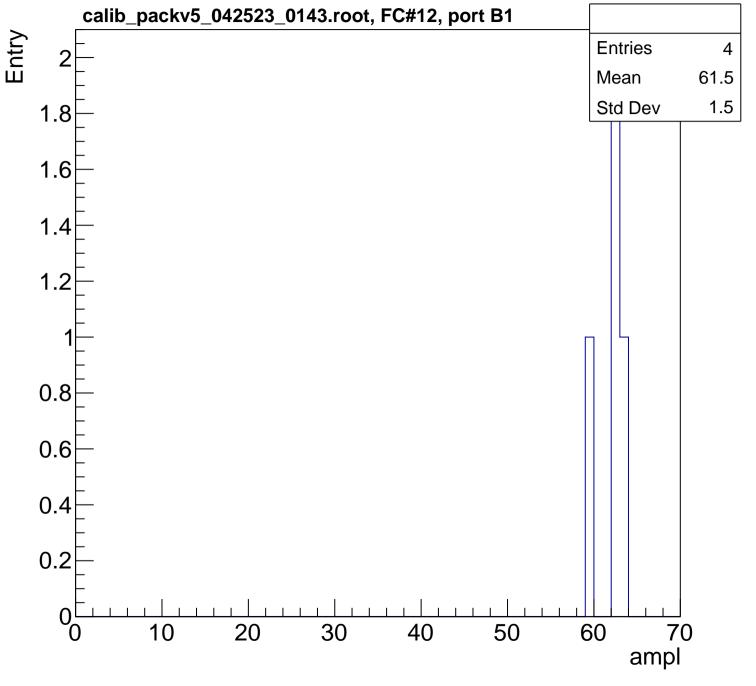




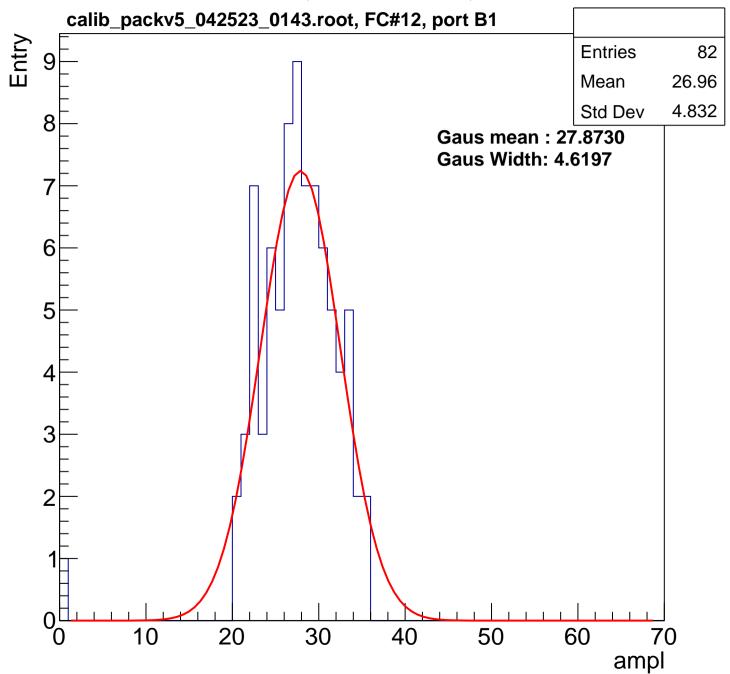


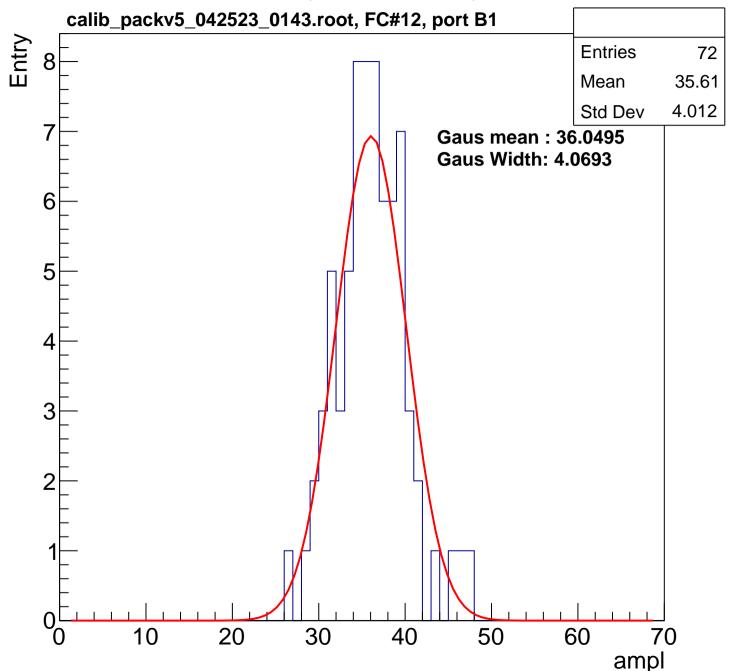


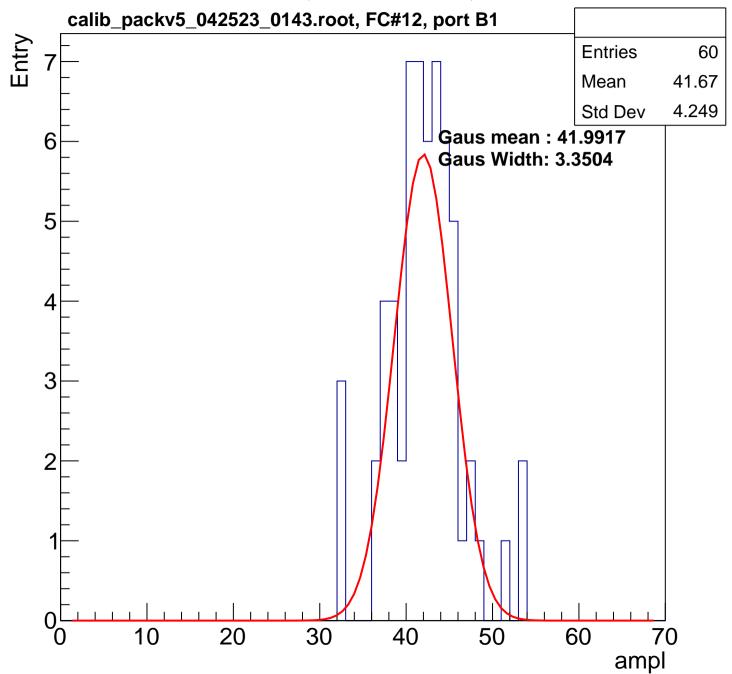


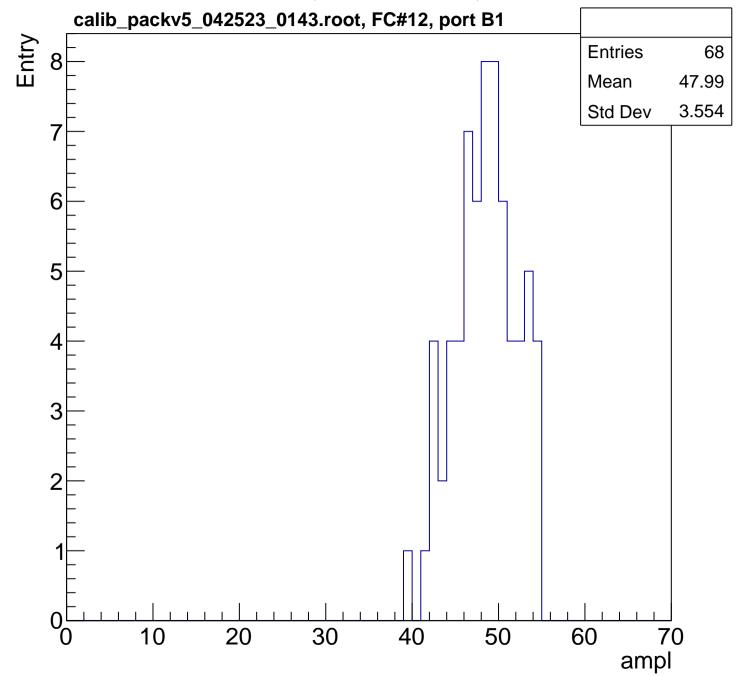


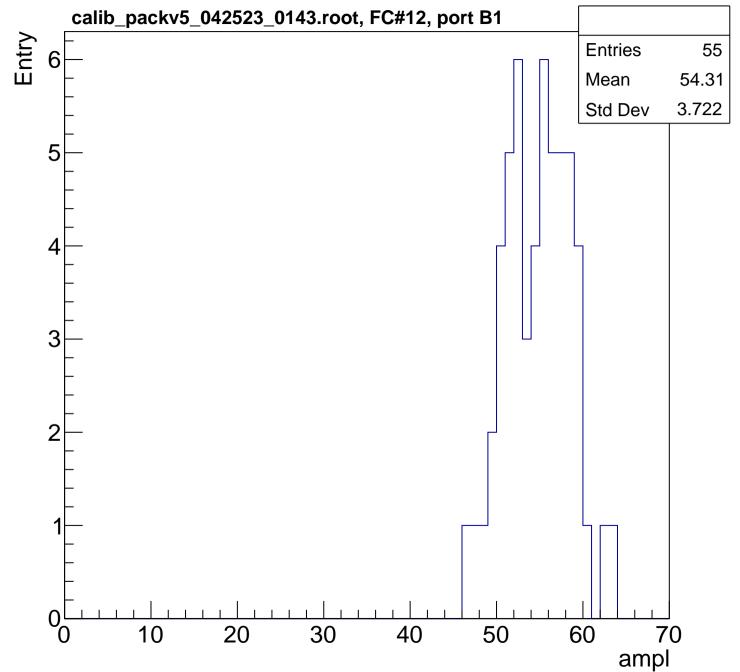


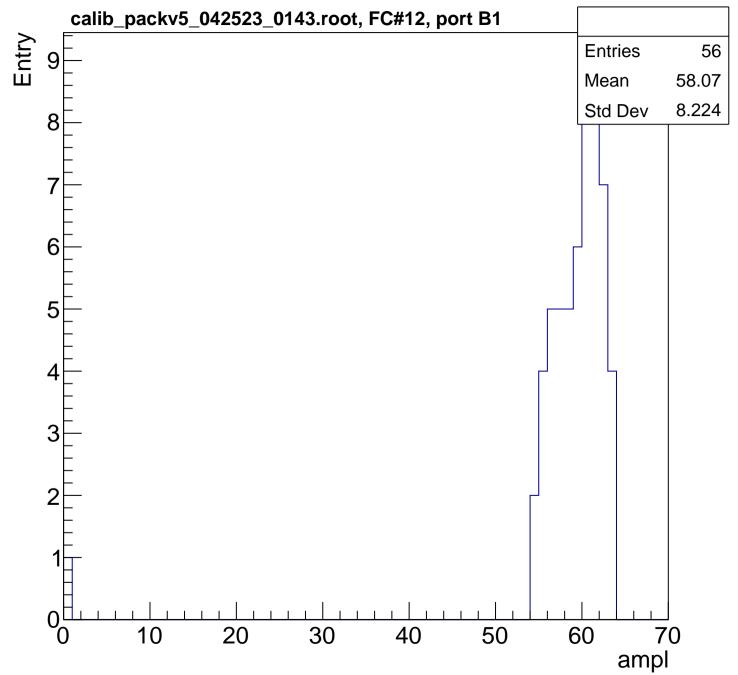


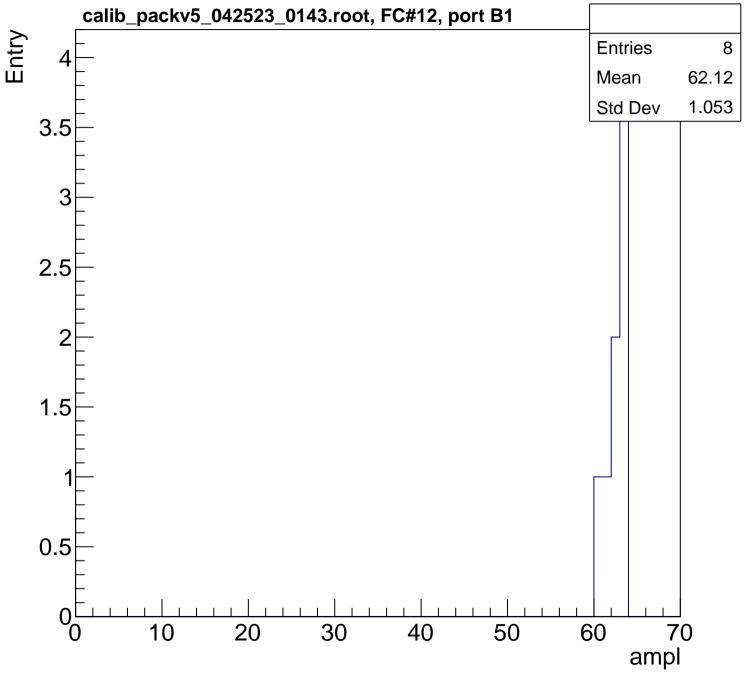


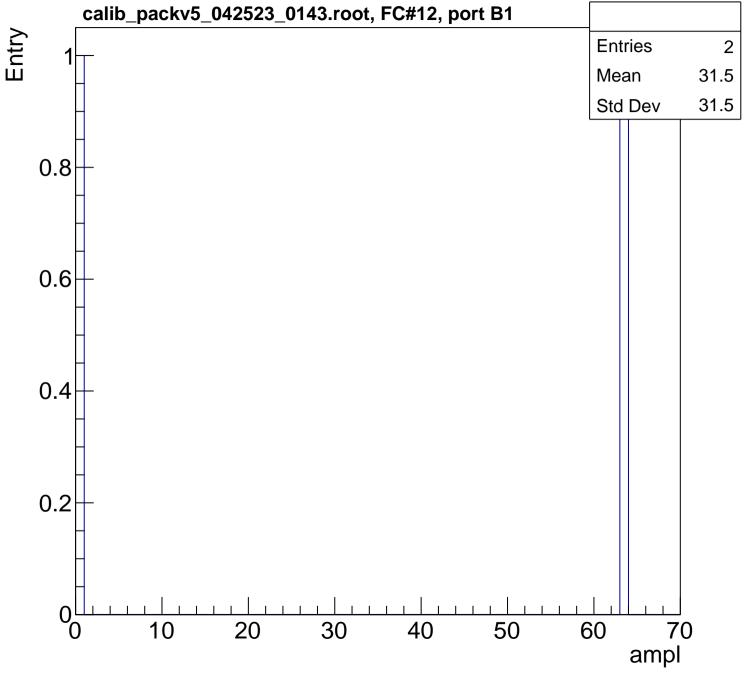


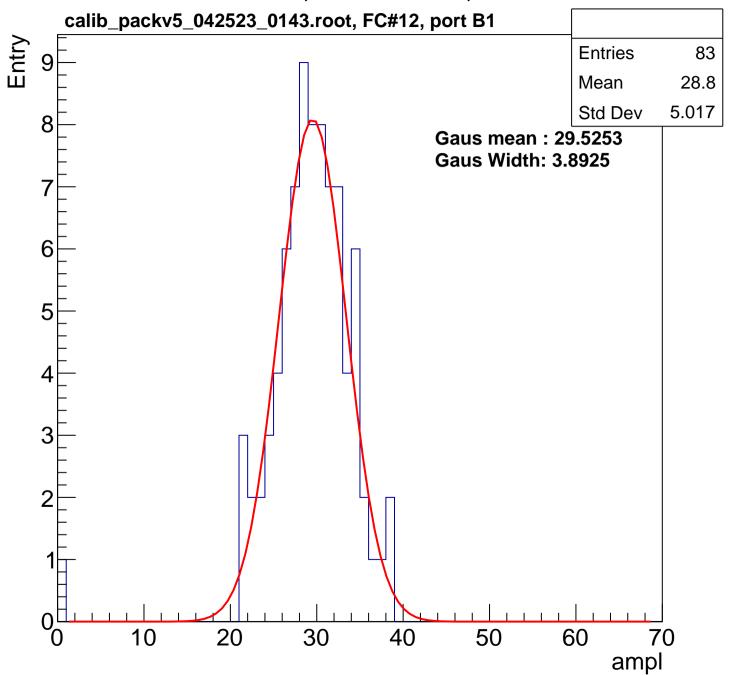


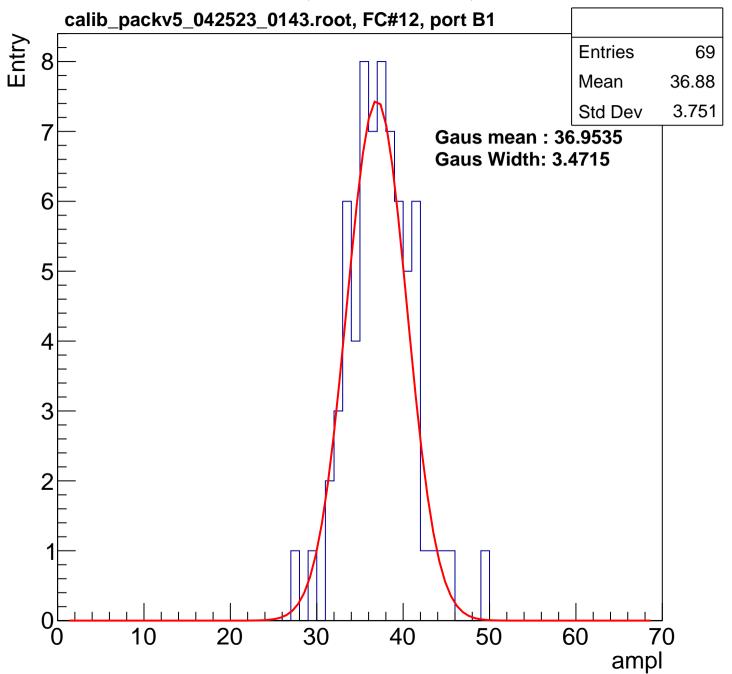


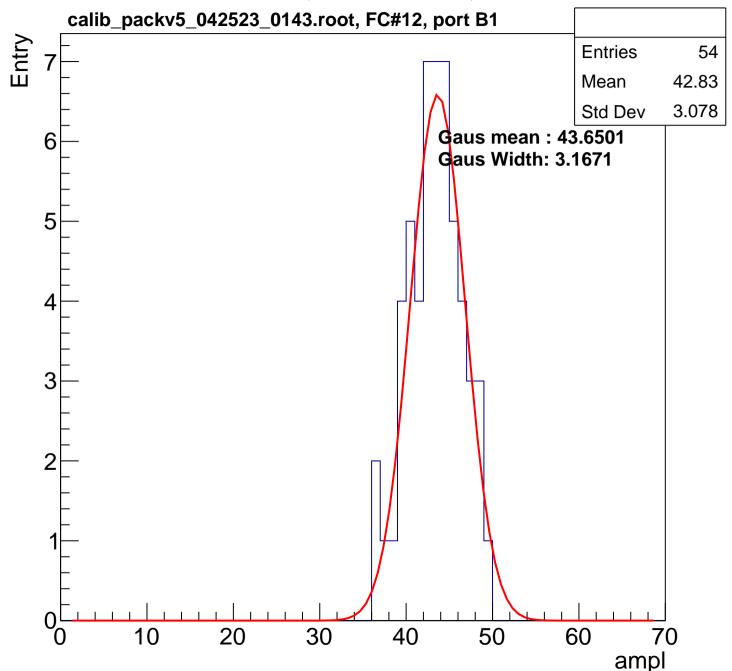


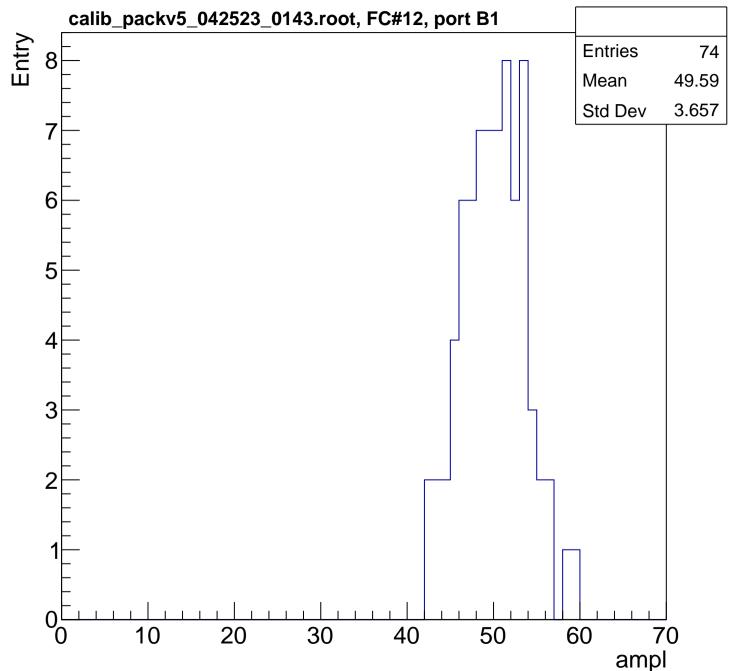


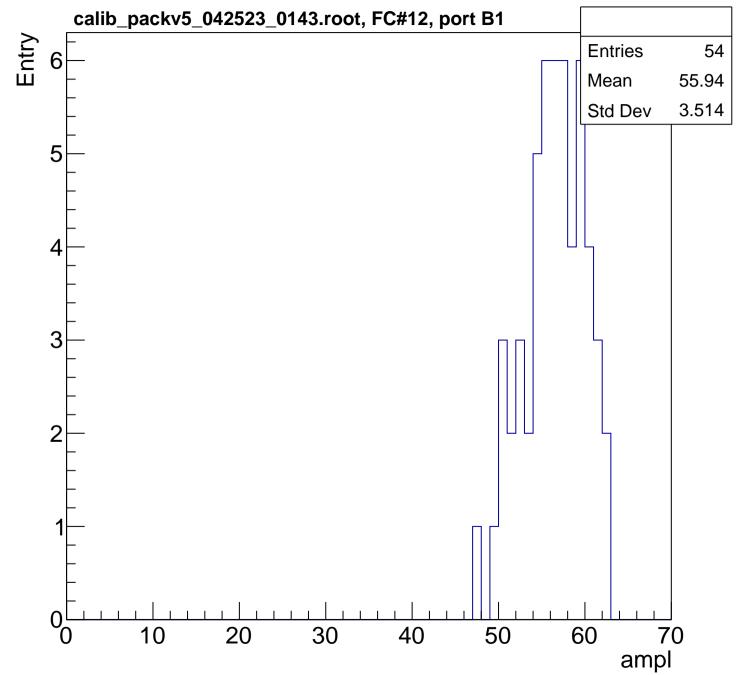


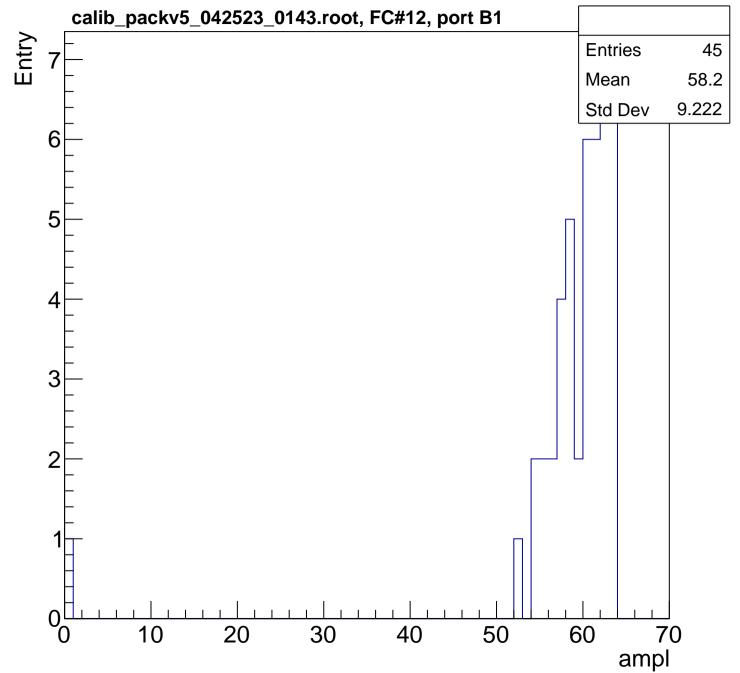


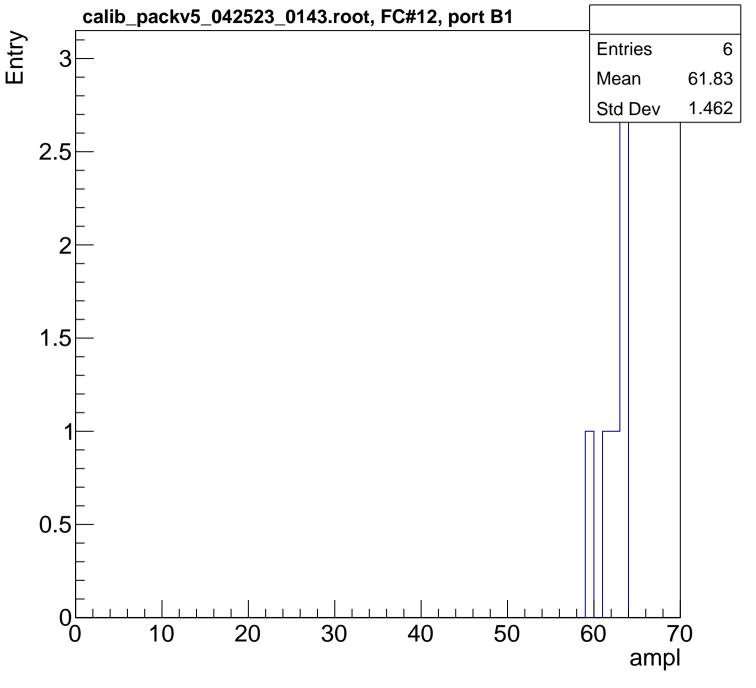




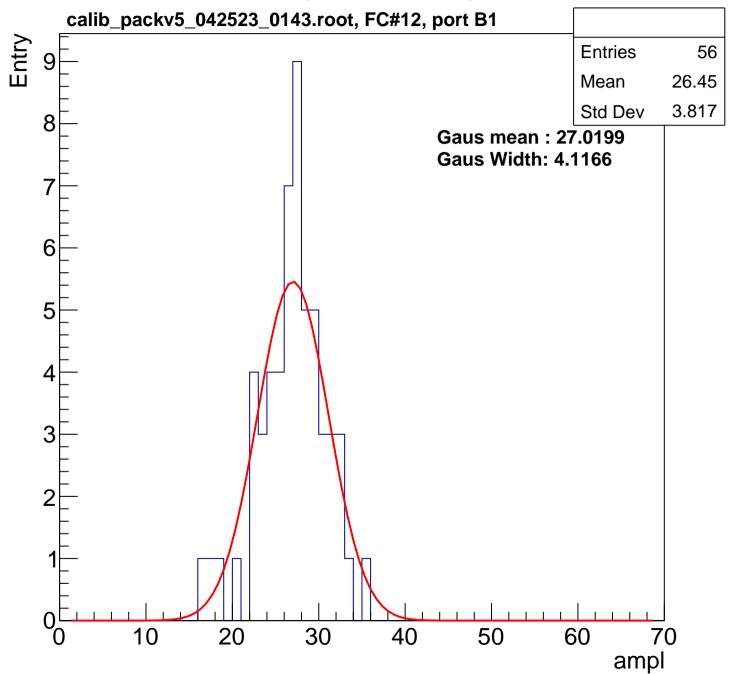


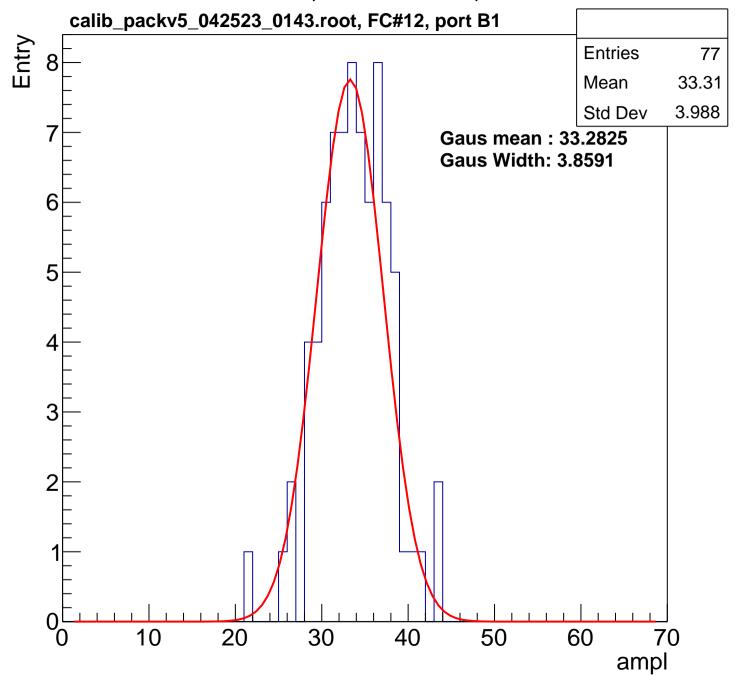


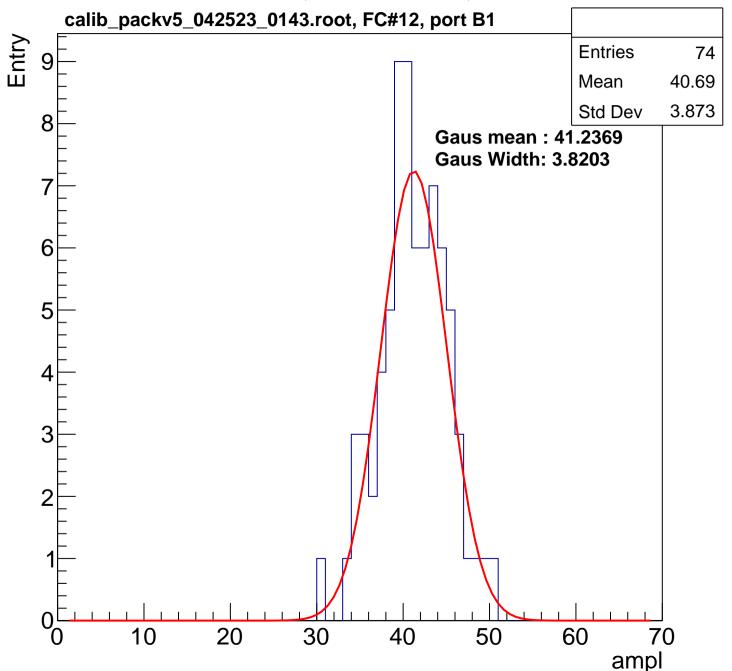


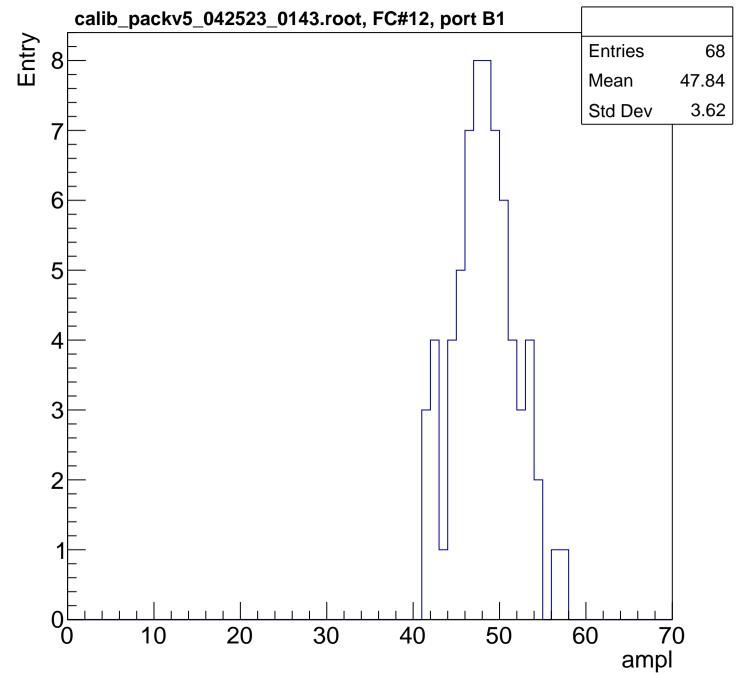


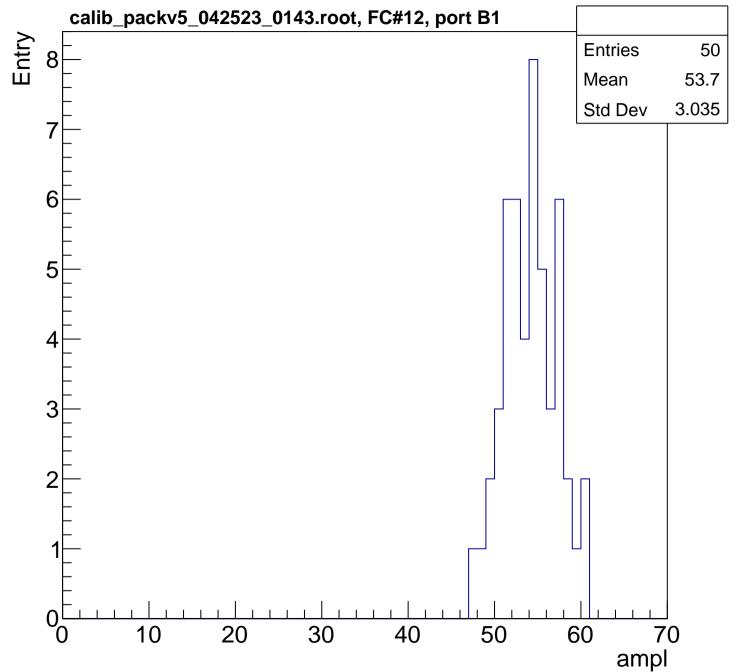


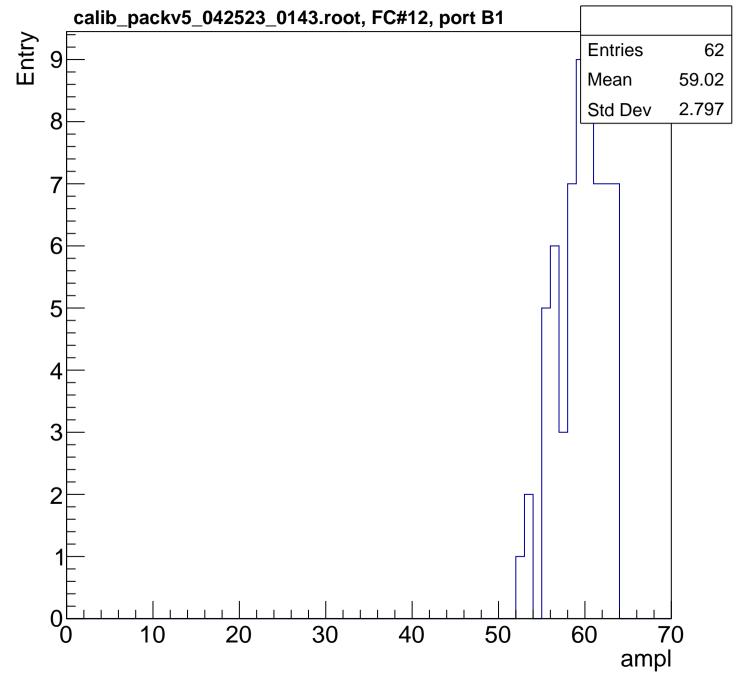


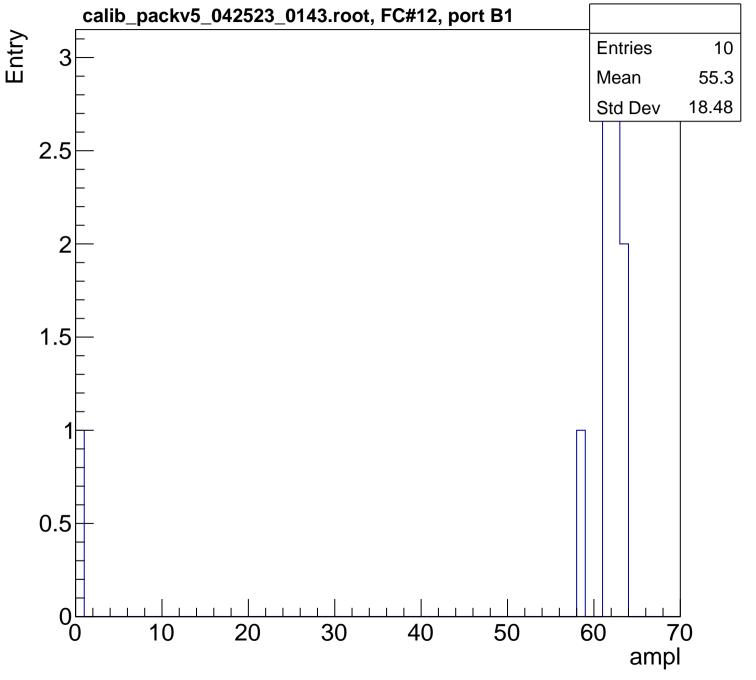


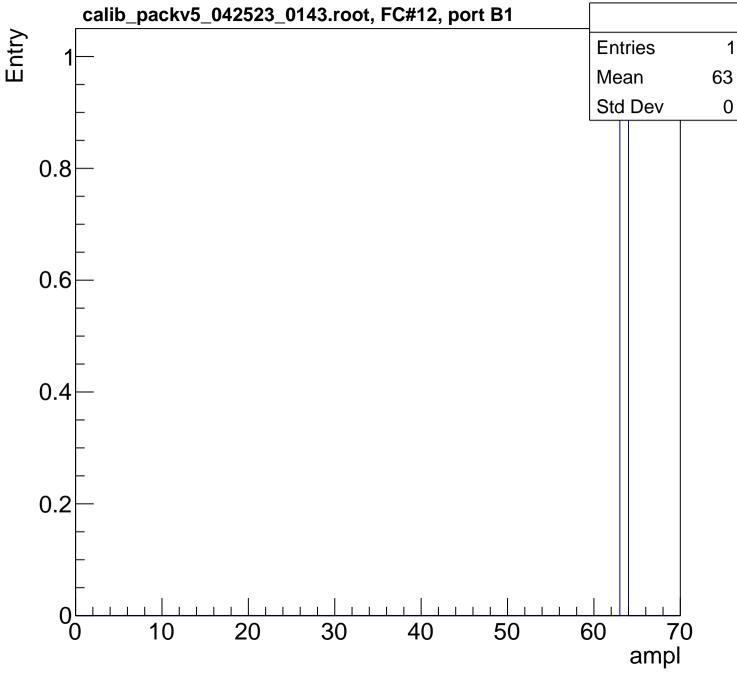


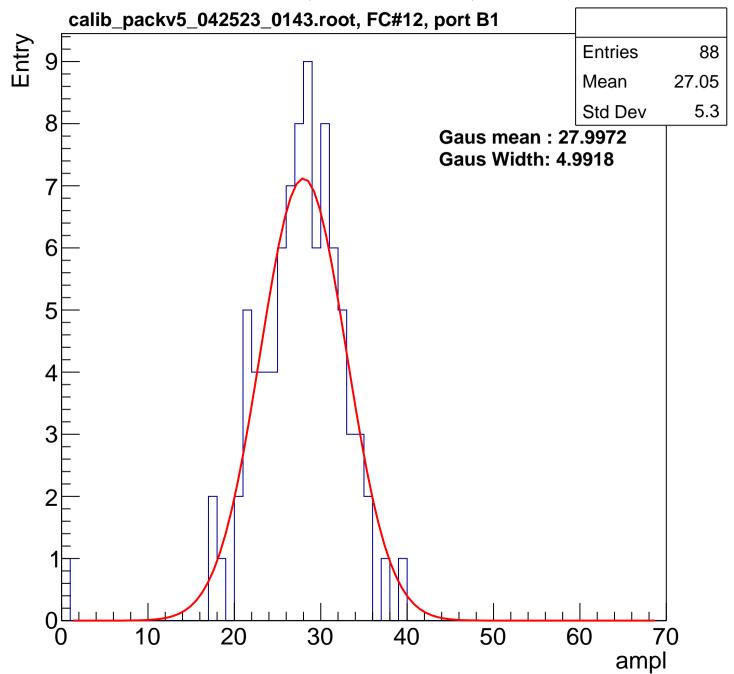


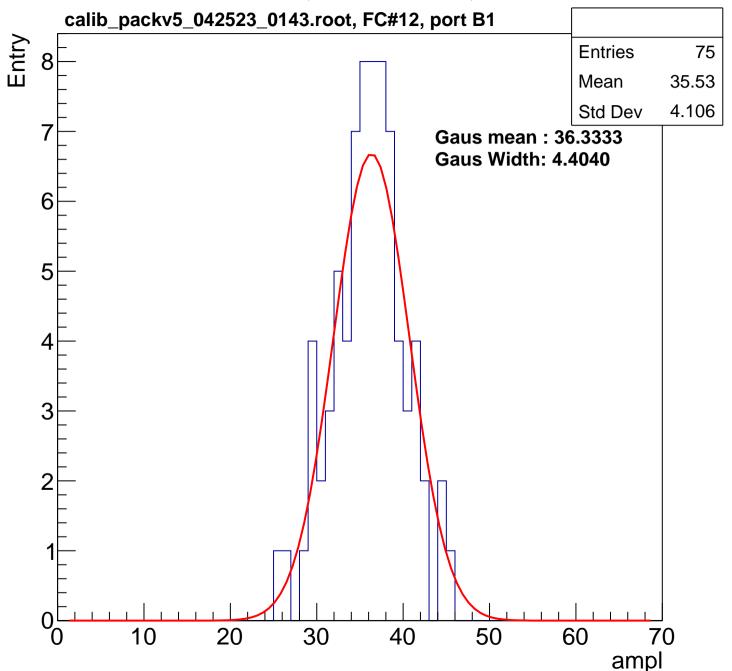


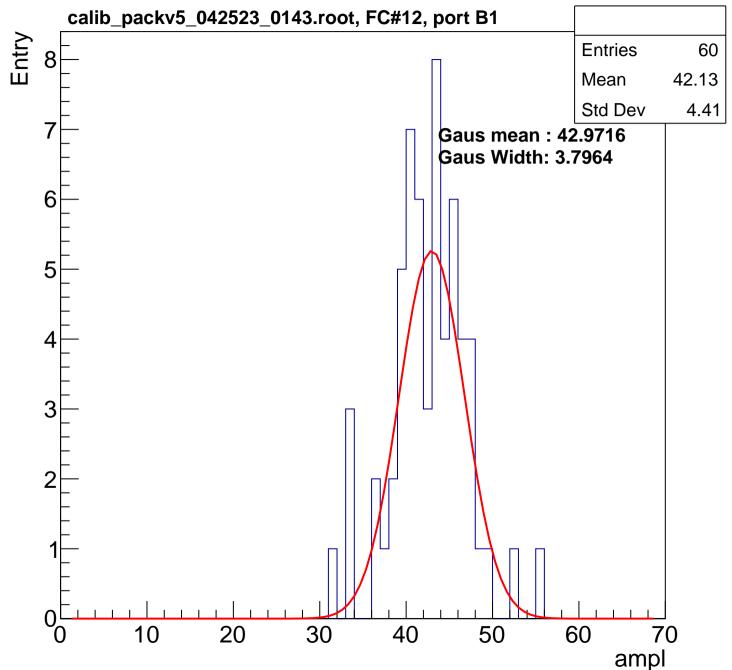


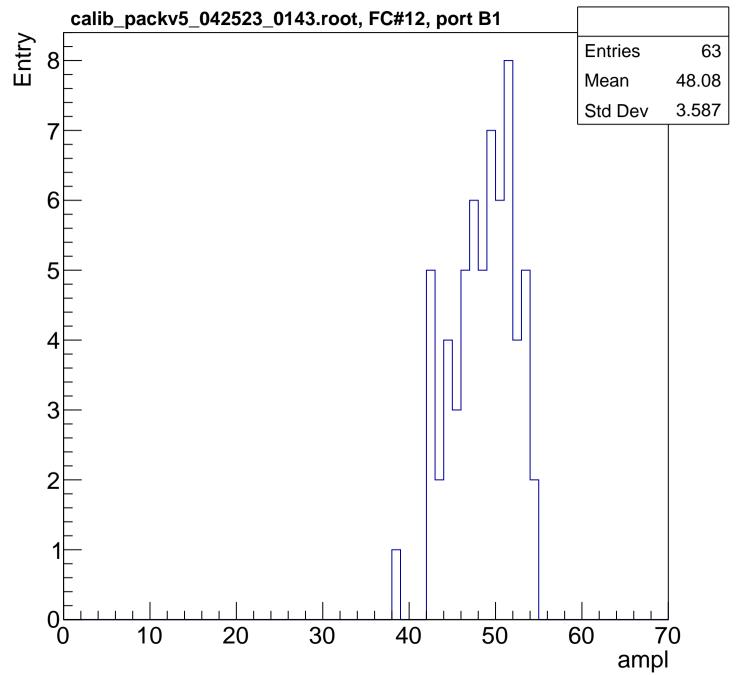


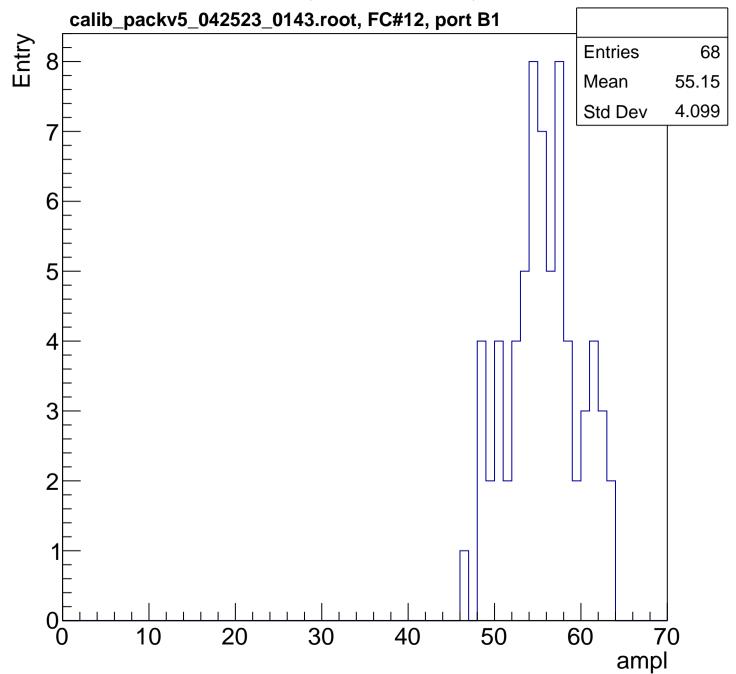


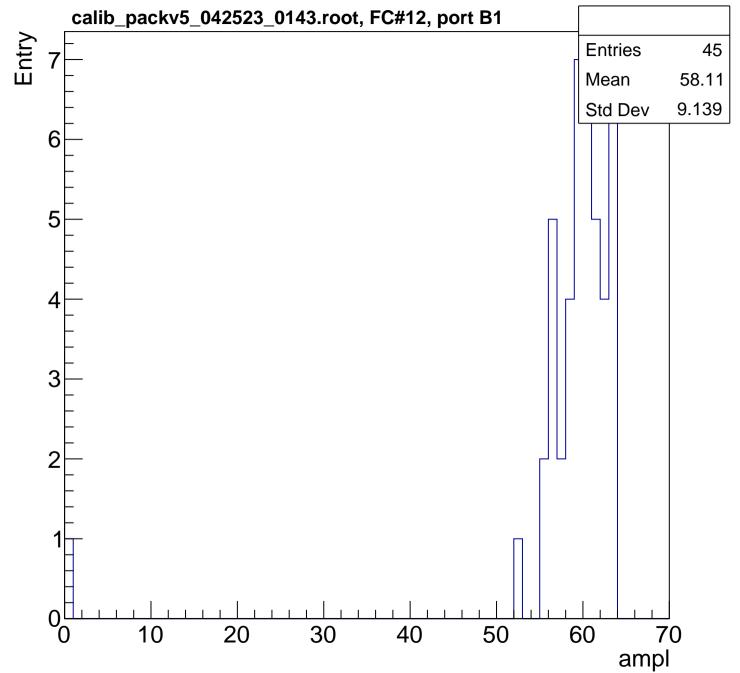


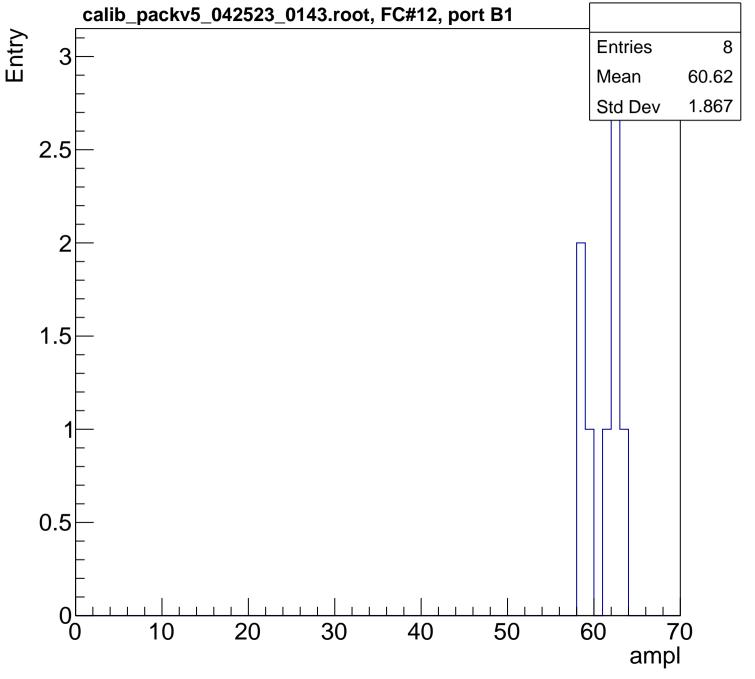




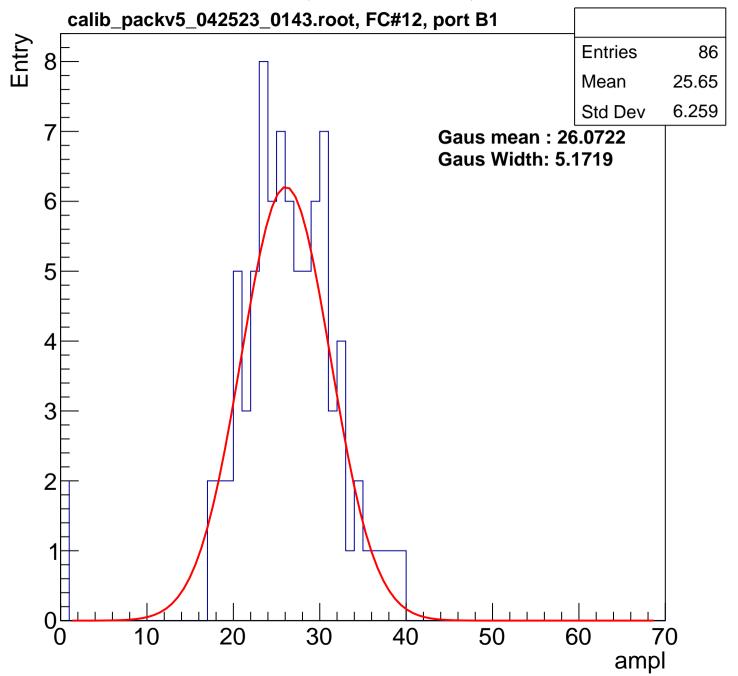


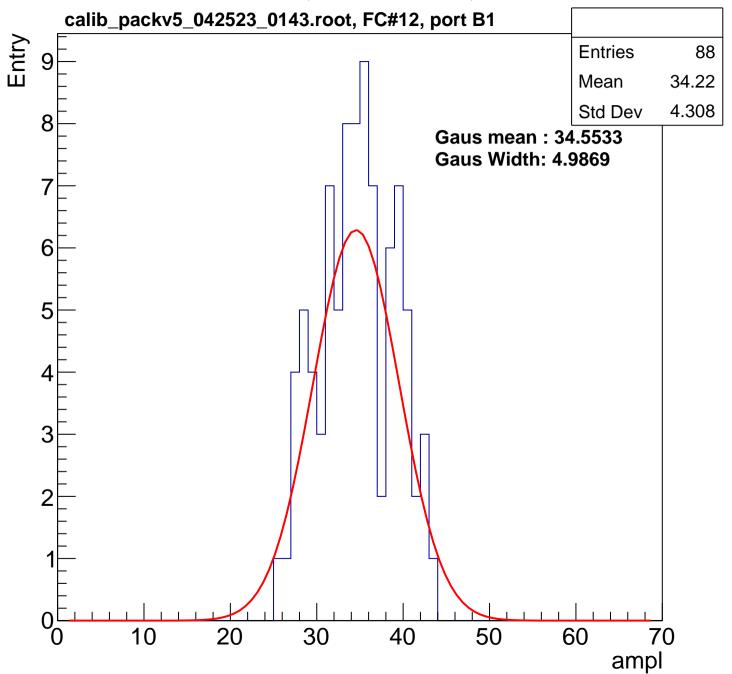


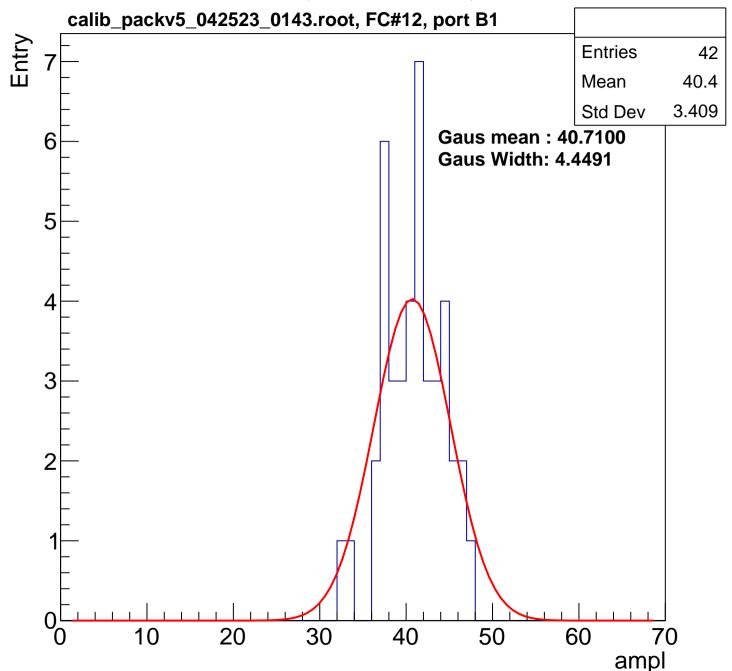


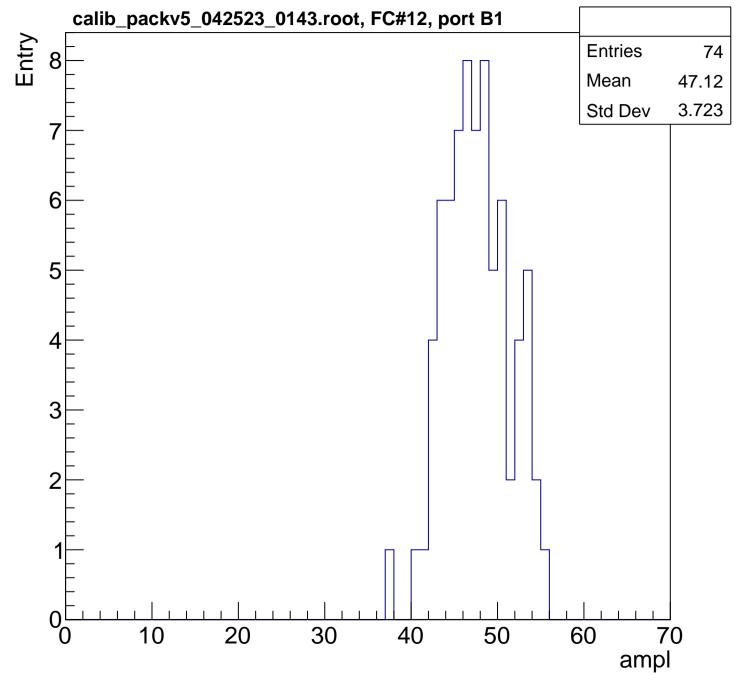


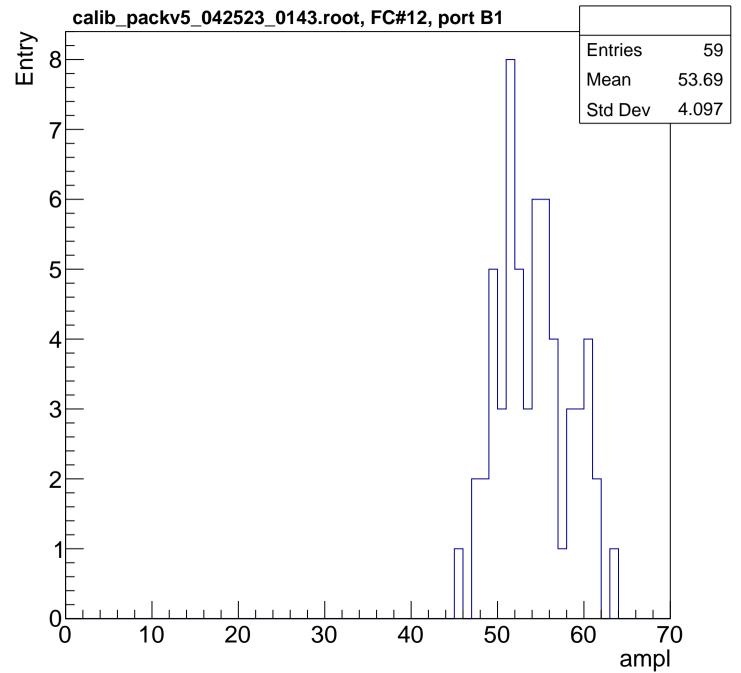


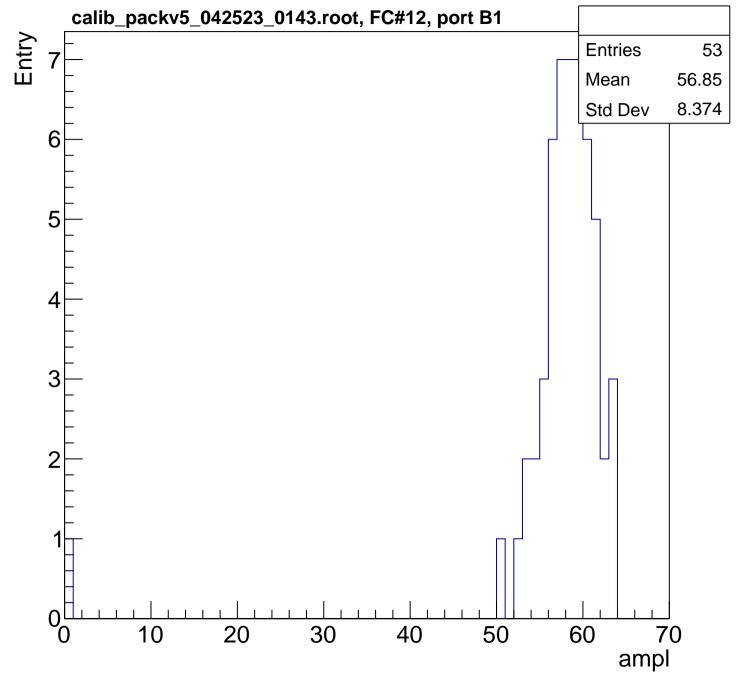


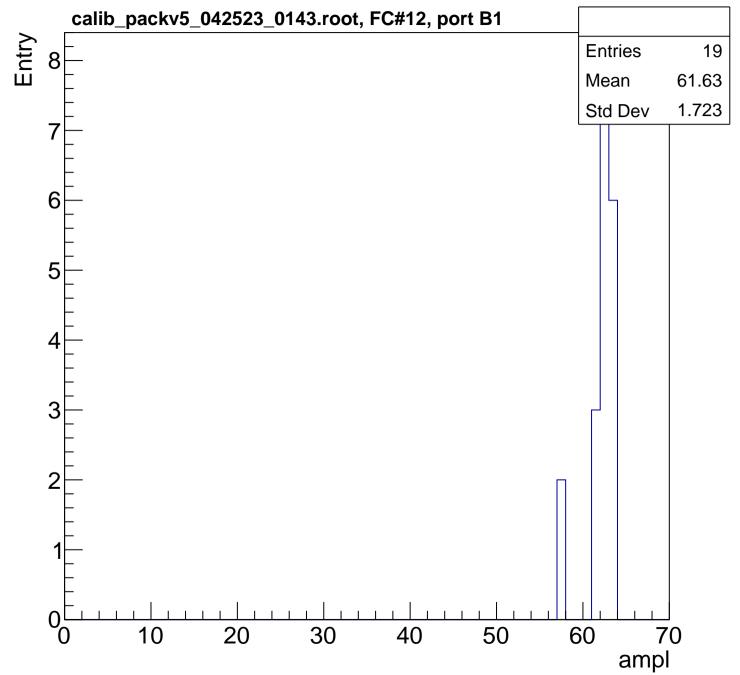


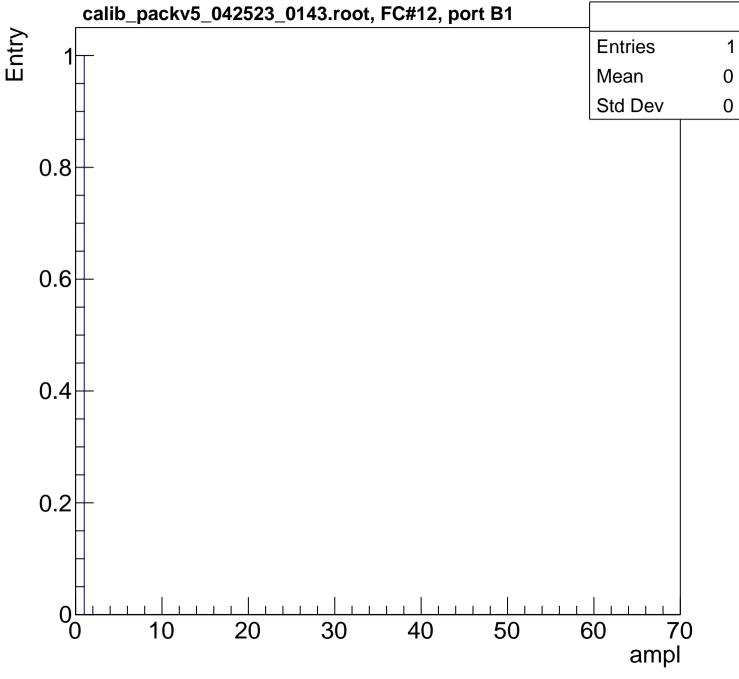


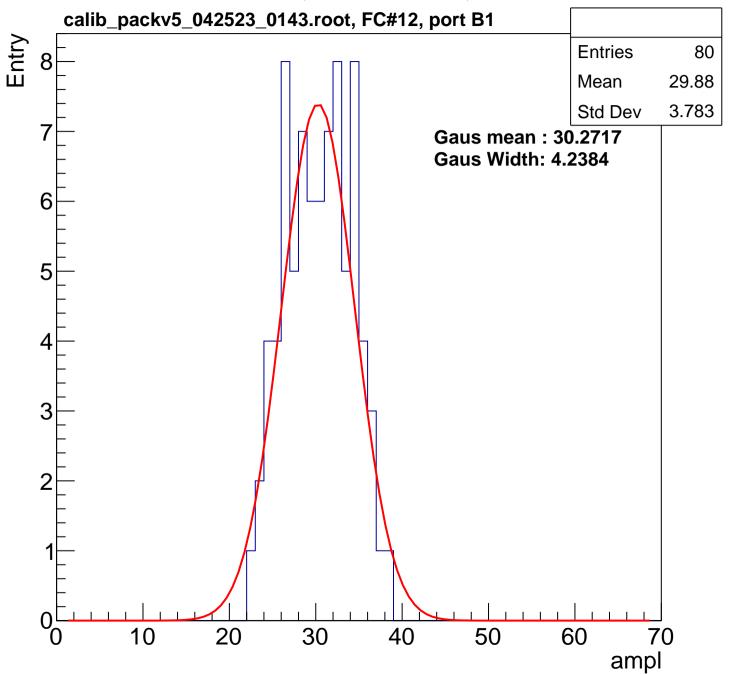


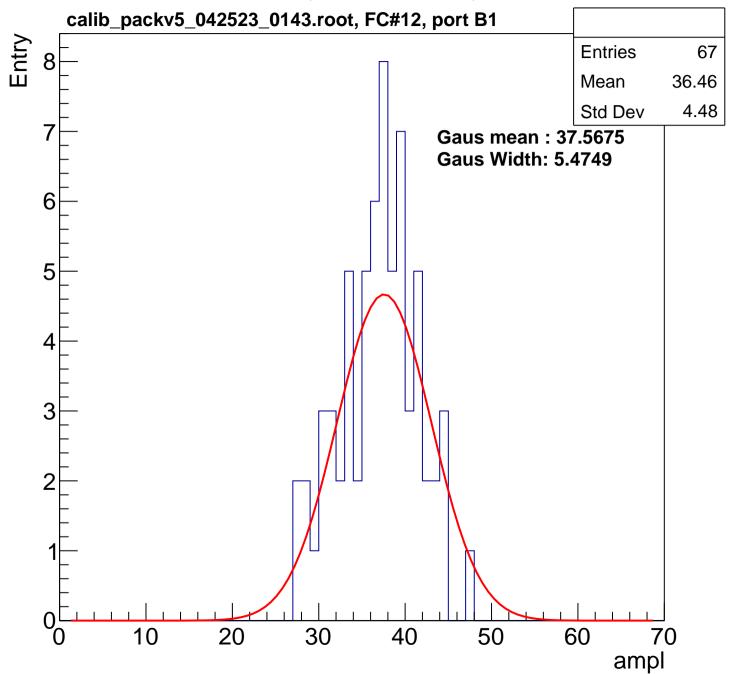


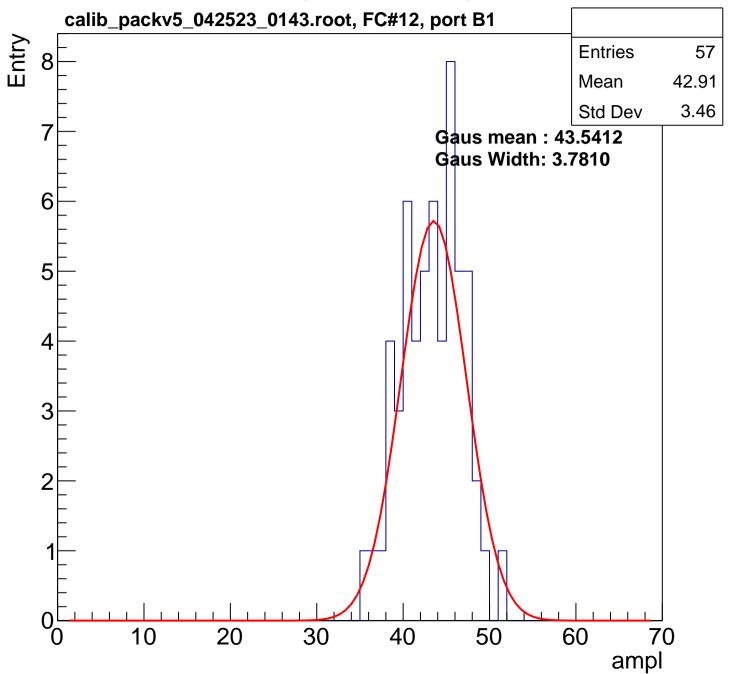


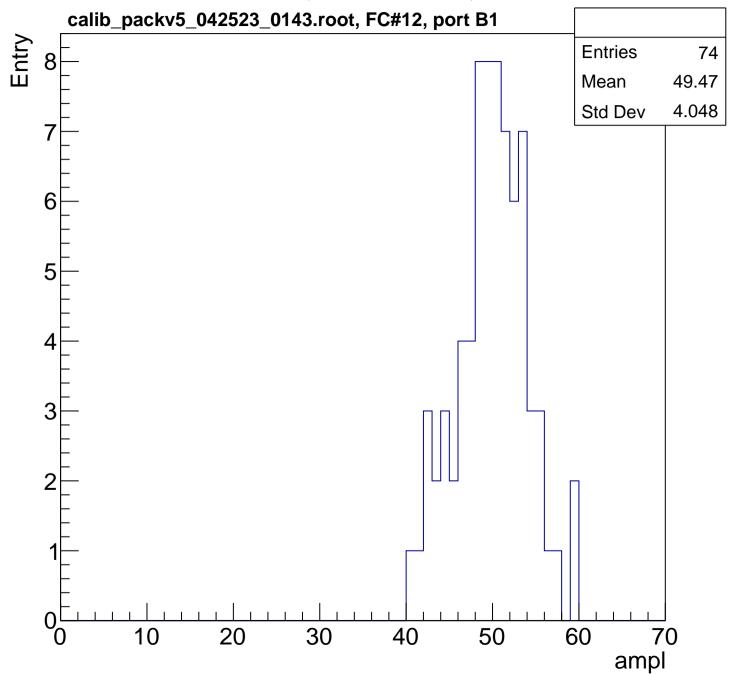


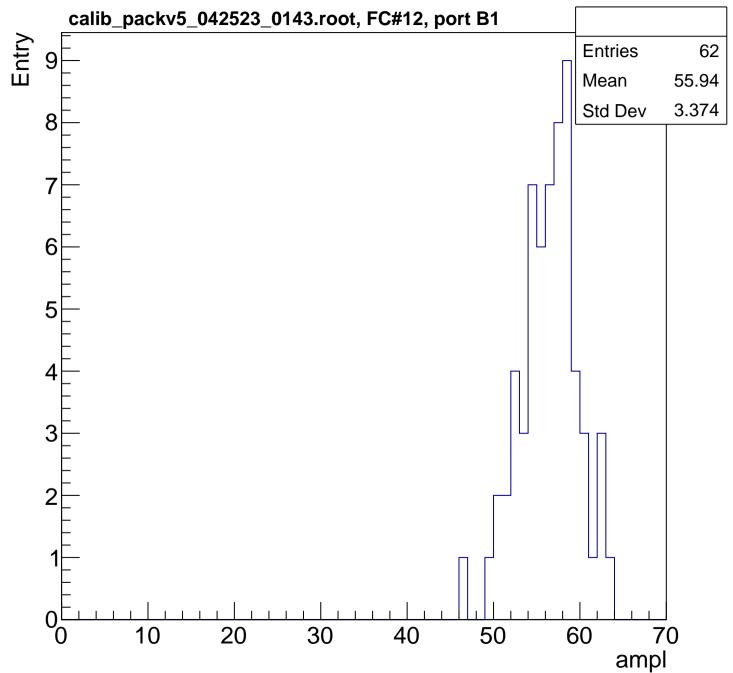


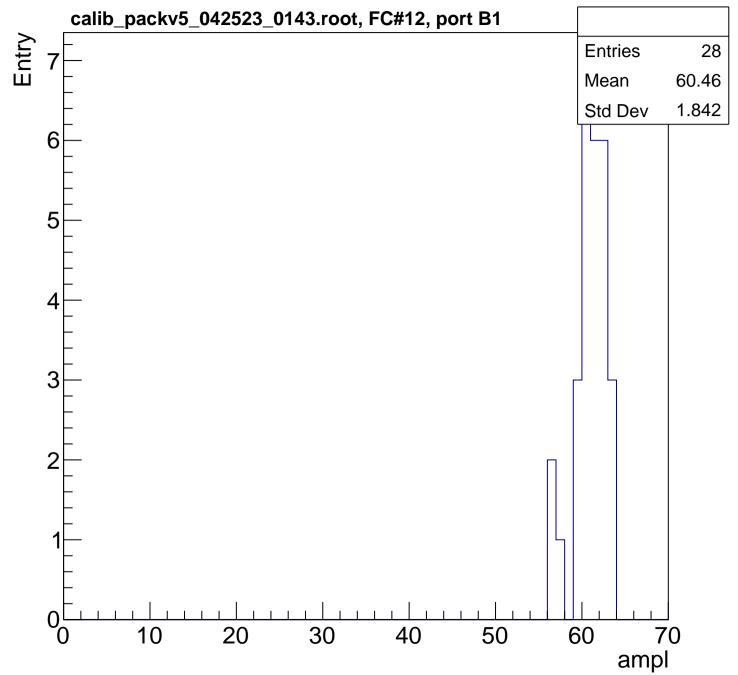


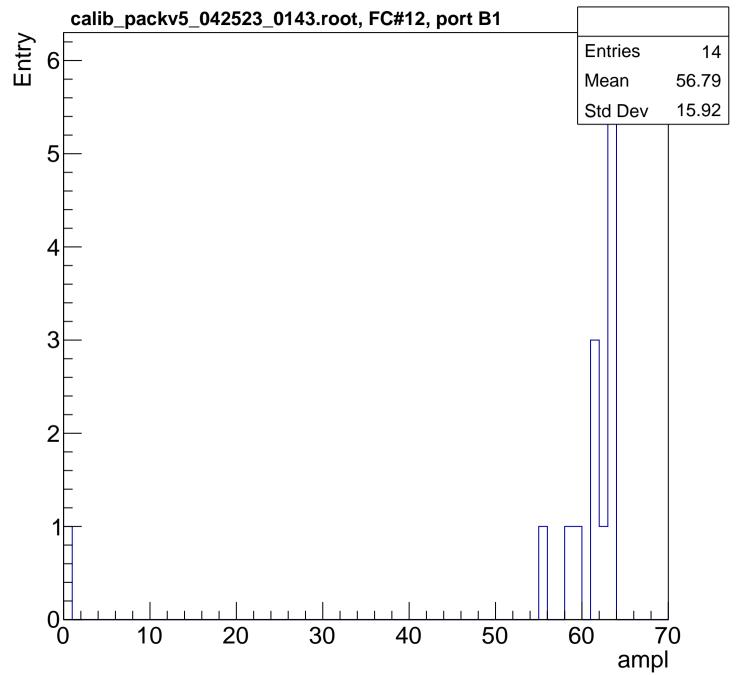




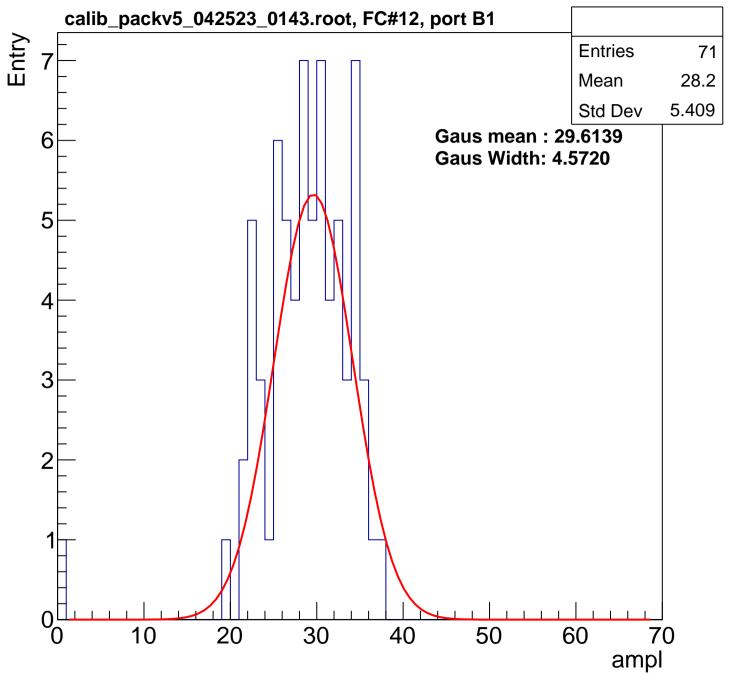


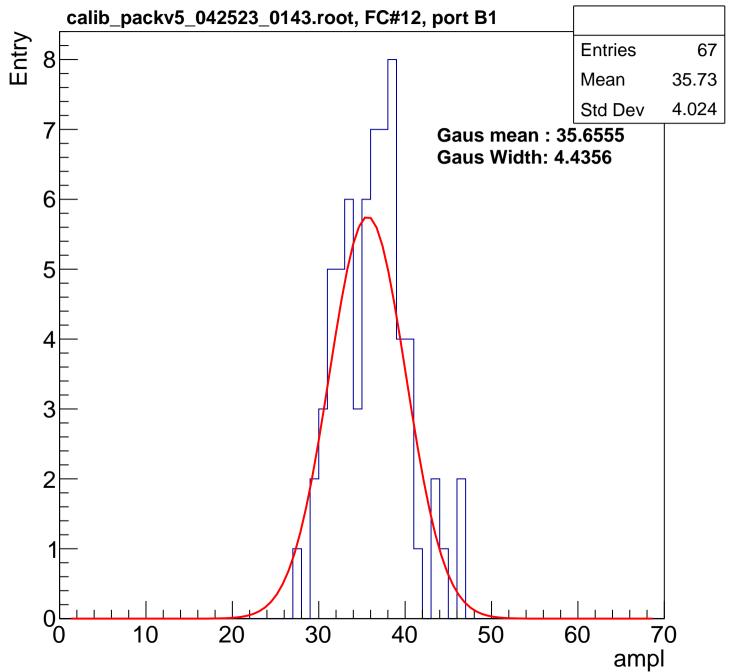


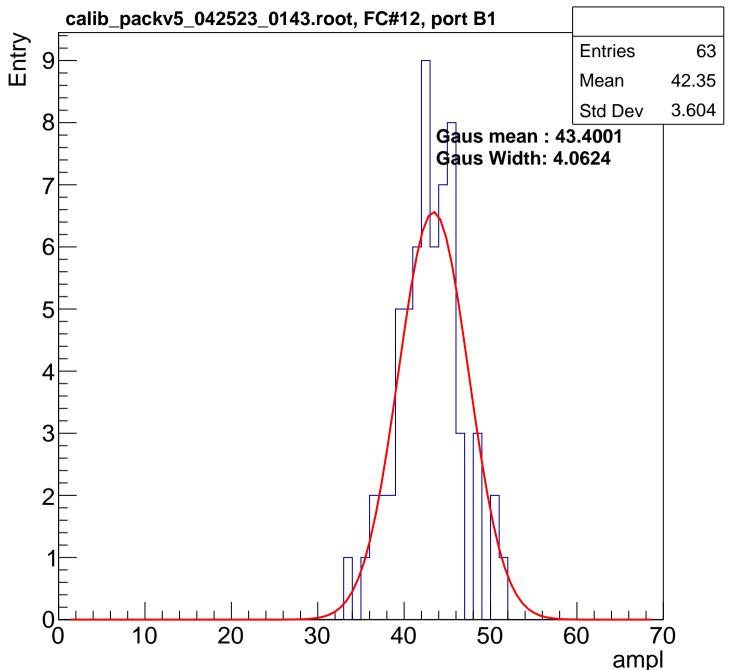


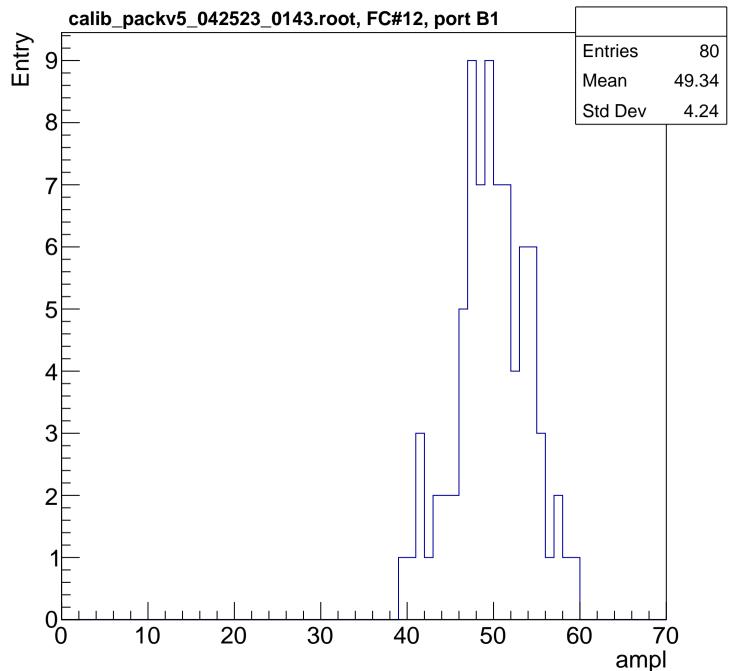


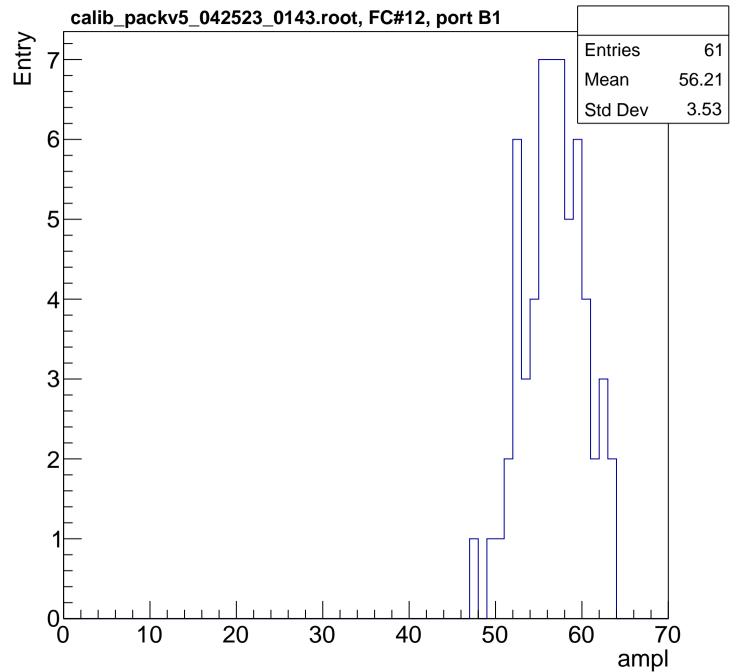


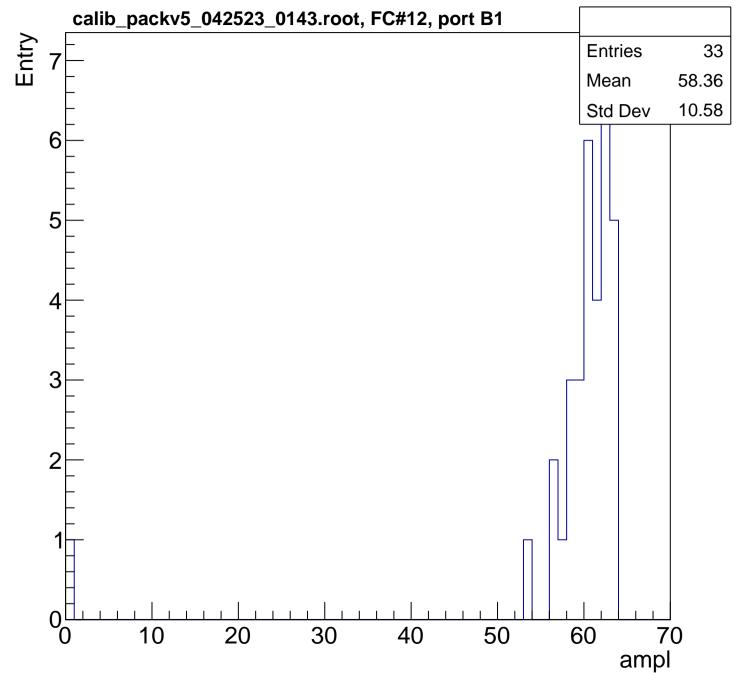


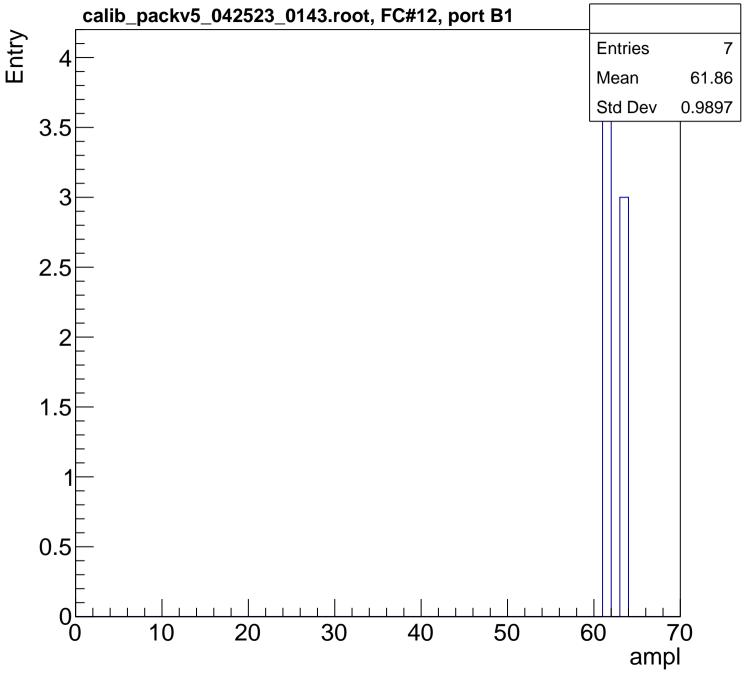


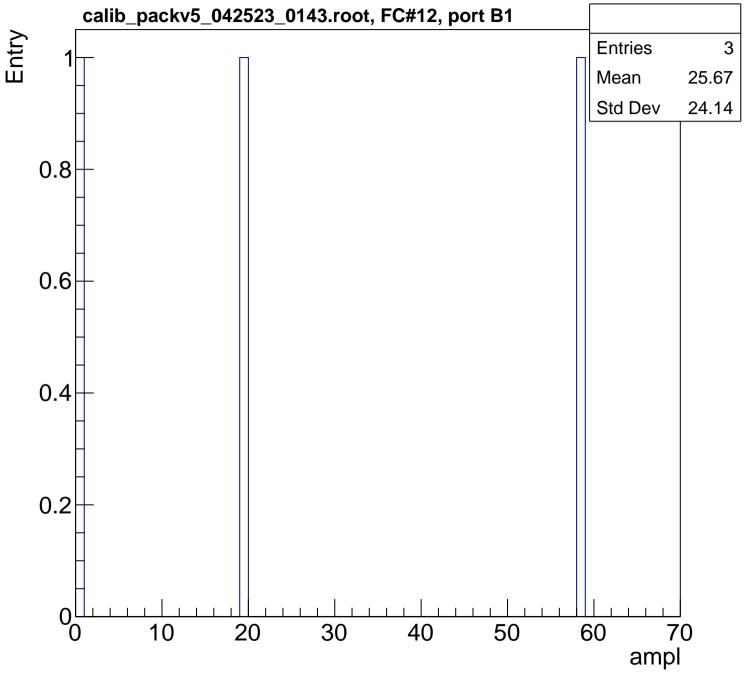


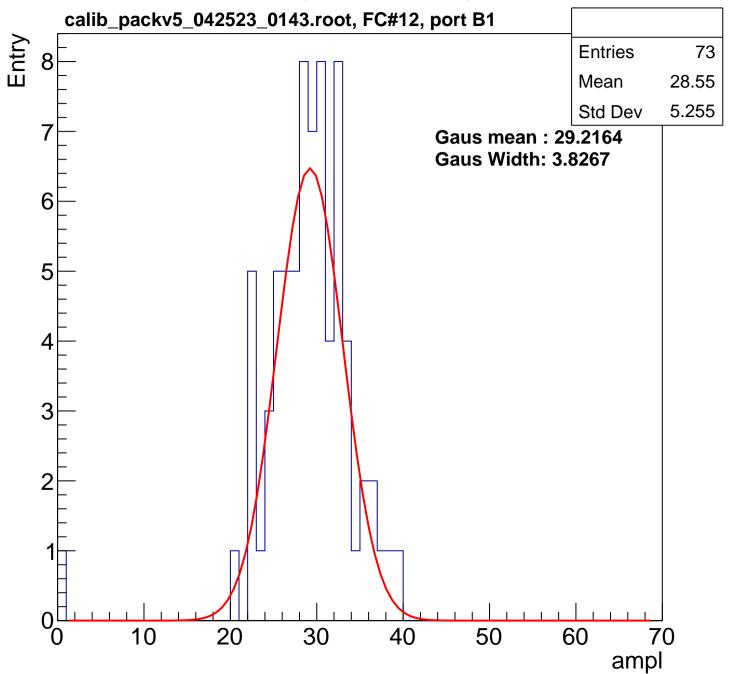


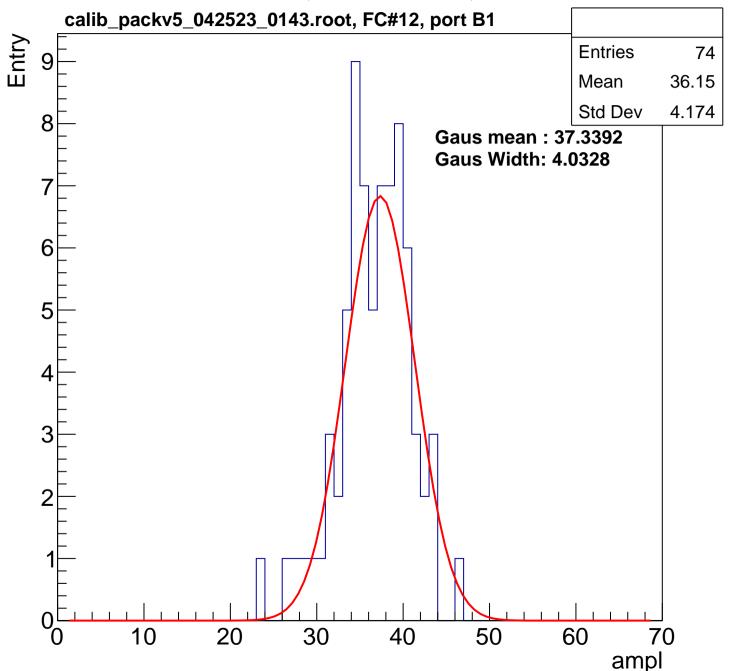


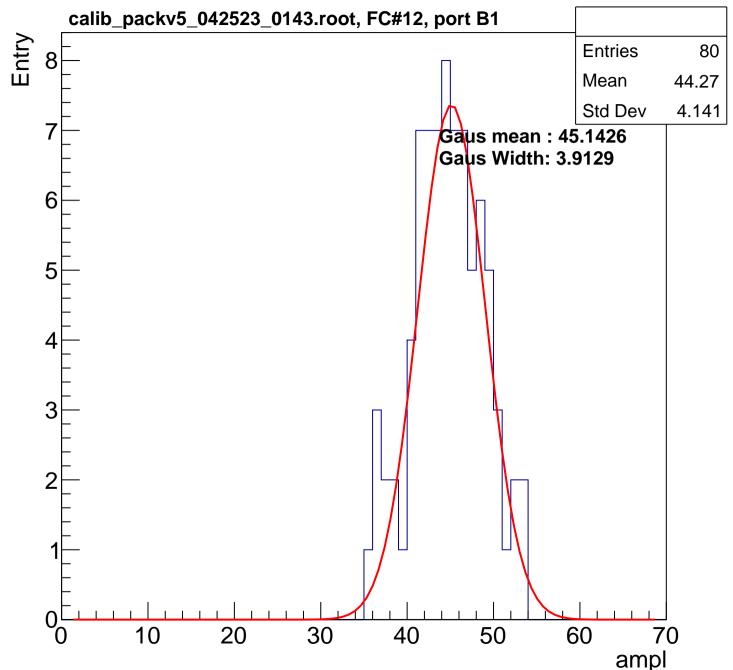


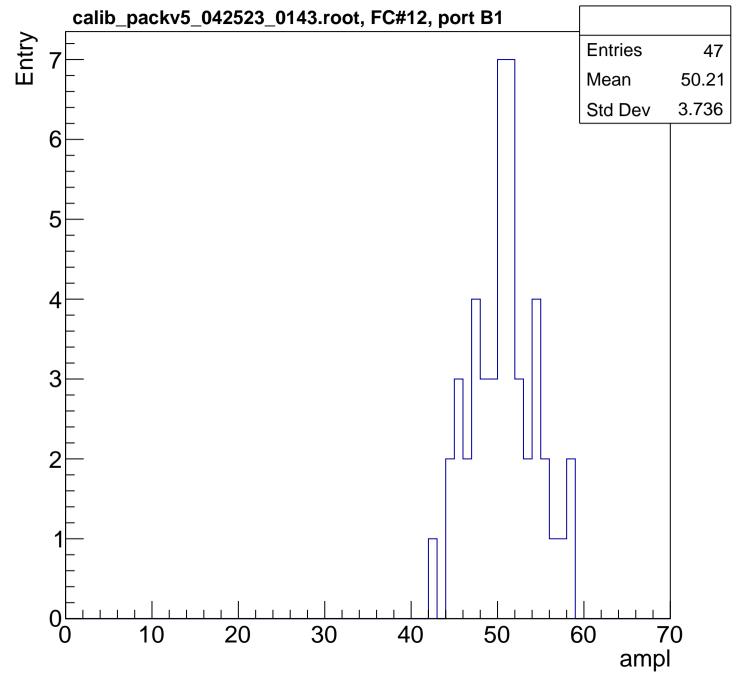


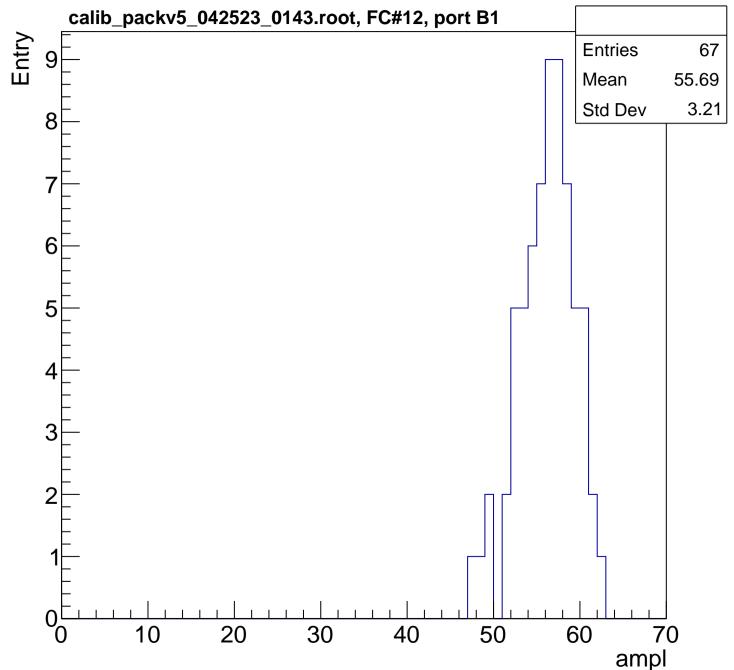


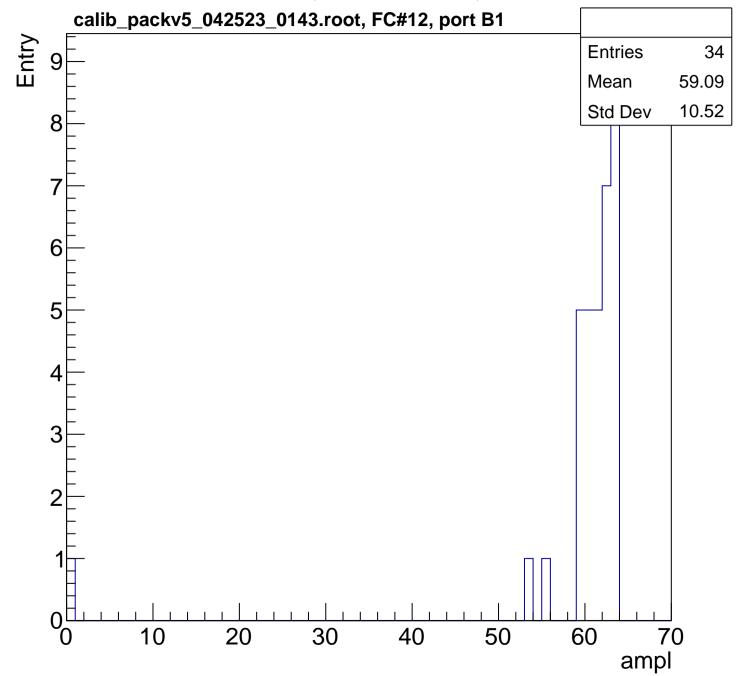


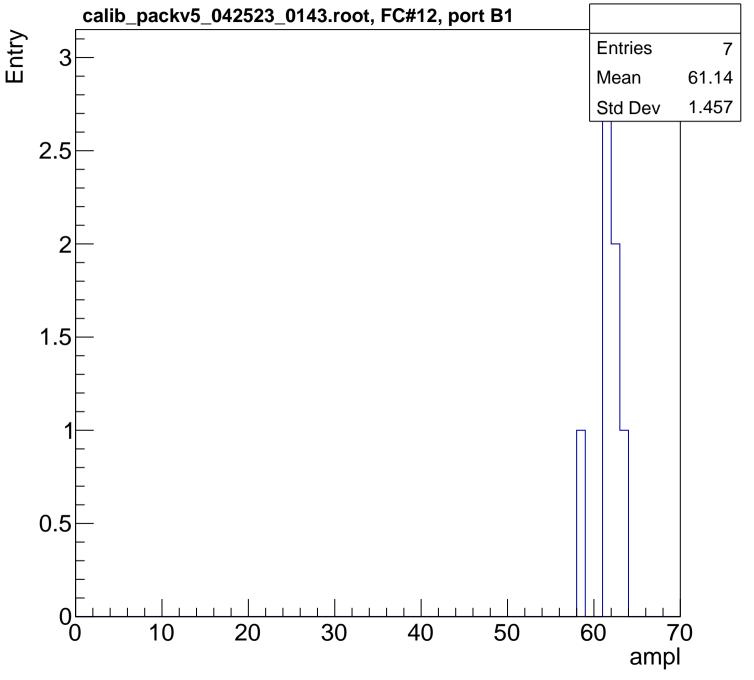


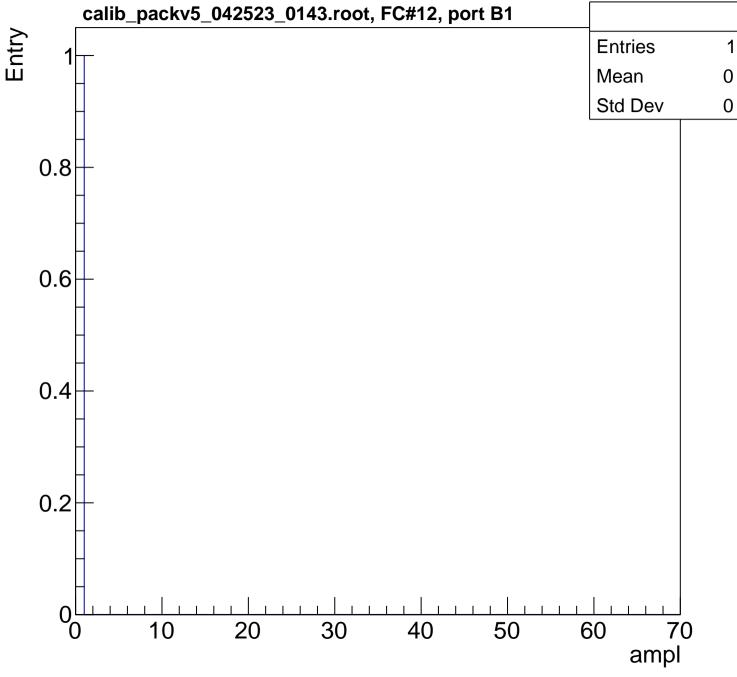












B0L102S, U3-ch127, adc7 calib_packv5_042523_0143.root, FC#12, port B1

