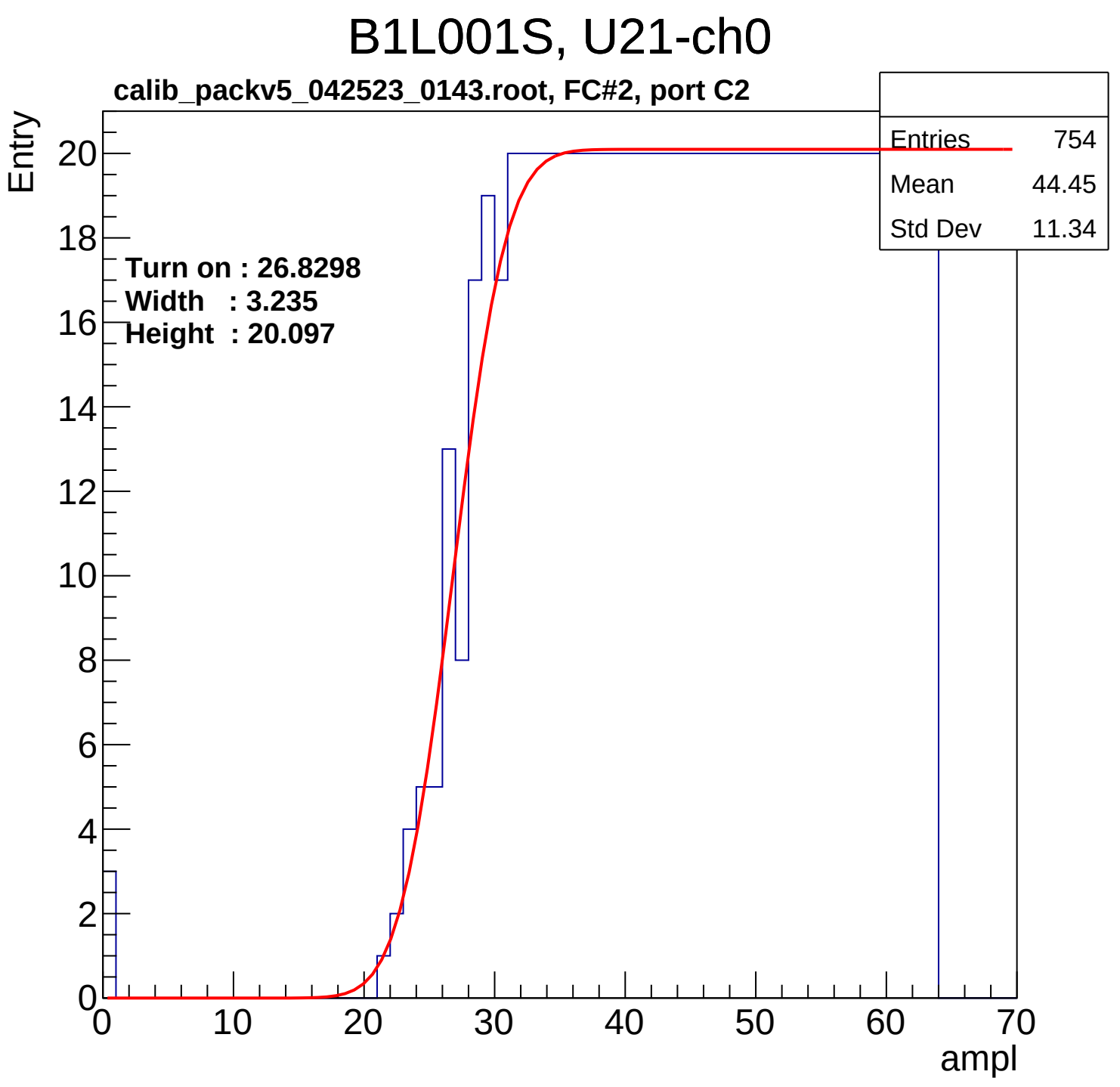
B1L001S, U21-ch0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 754
Mean 44.45
Std Dev 11.34
Turn on : 26.8298
Width : 3.235
Height : 20.097
Entry
ampl
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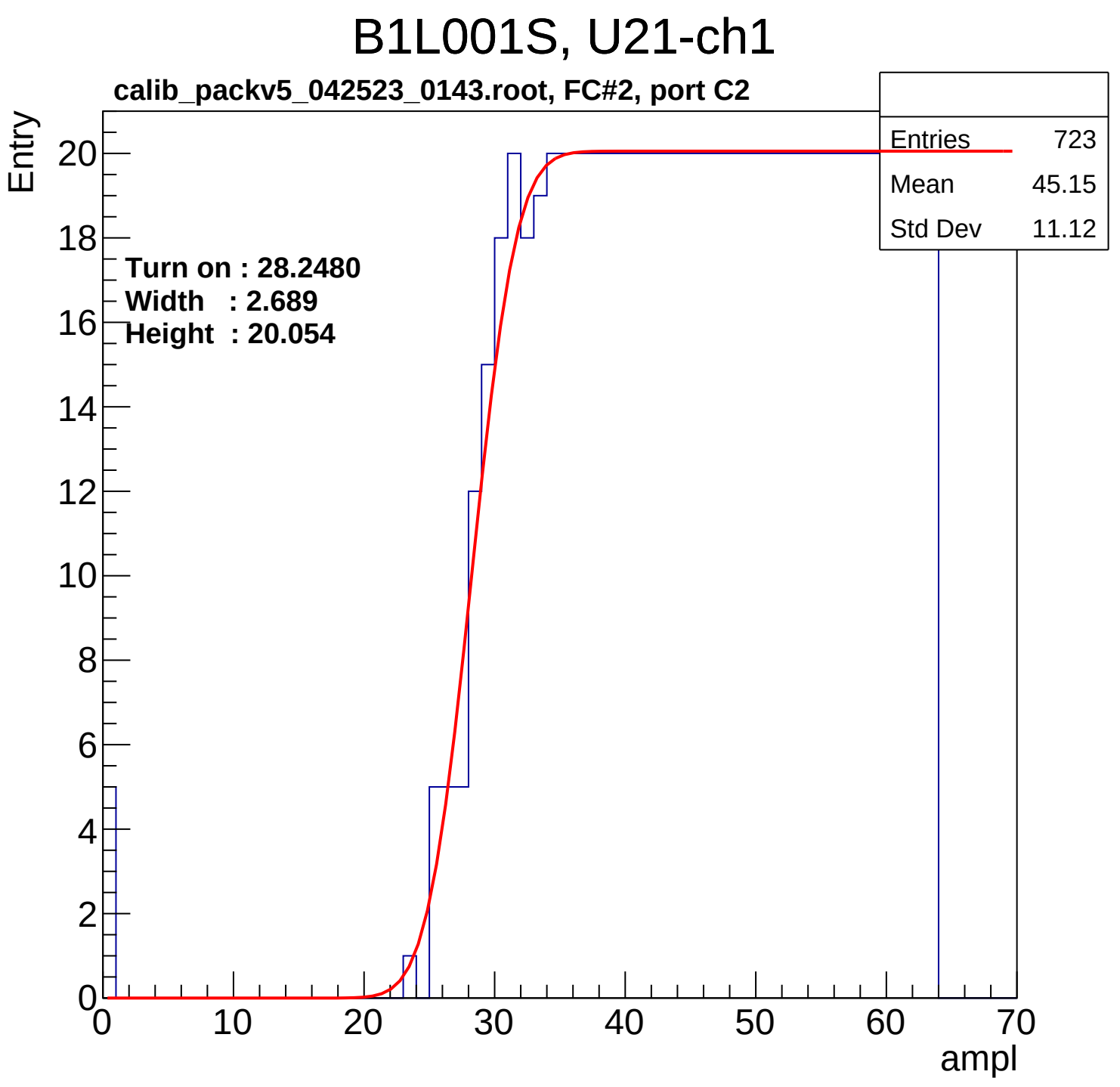
B1L001S, U21-ch1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 723
Mean 45.15
Std Dev 11.12
Turn on : 28.2480
Width : 2.689
Height : 20.054
Entry
ampl
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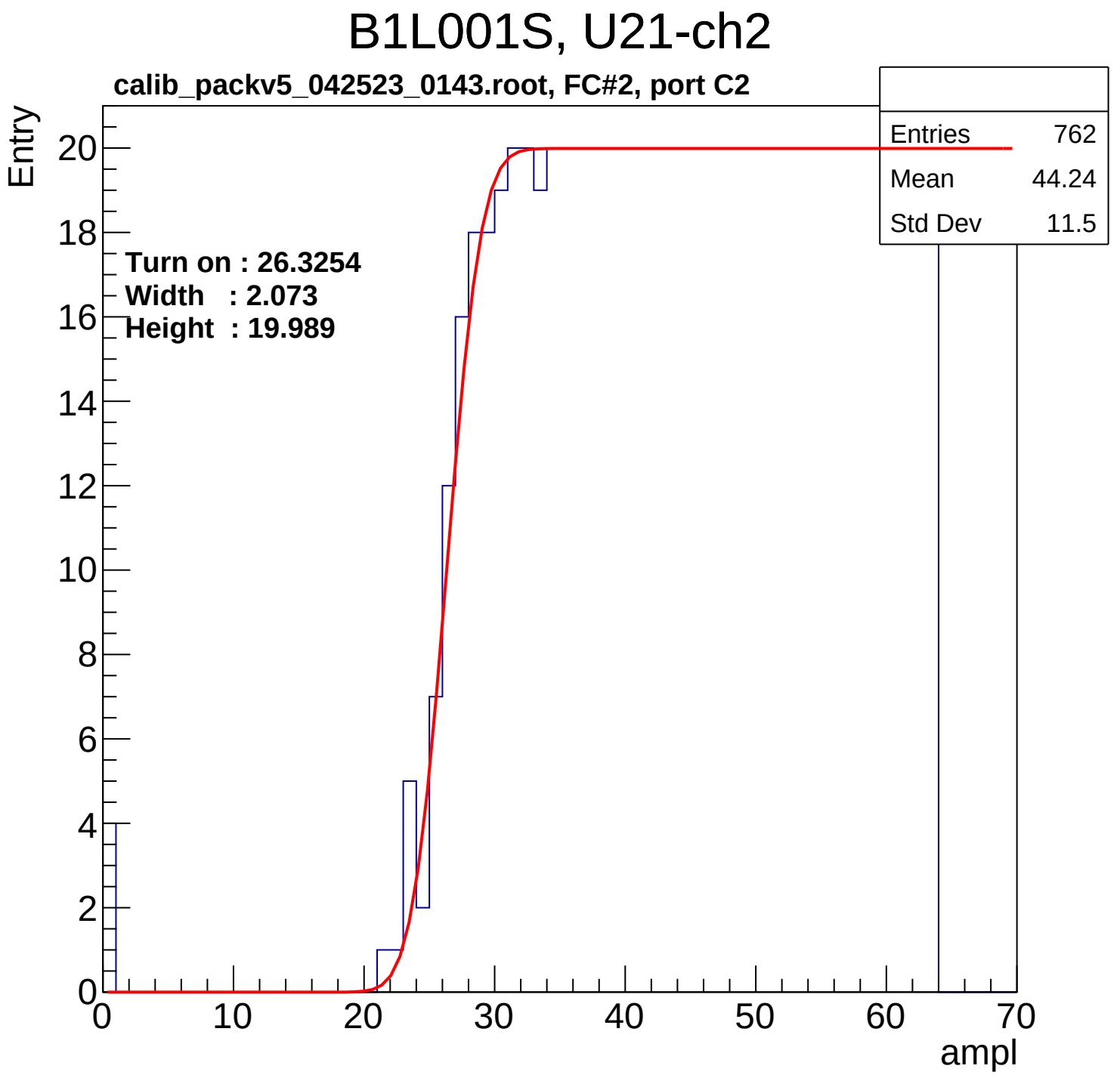
B1L001S, U21-ch2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 762
Mean 44.24
Std Dev 11.5
Turn on : 26.3254
Width : 2.073
Height : 19.989
Entry
ampl
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6
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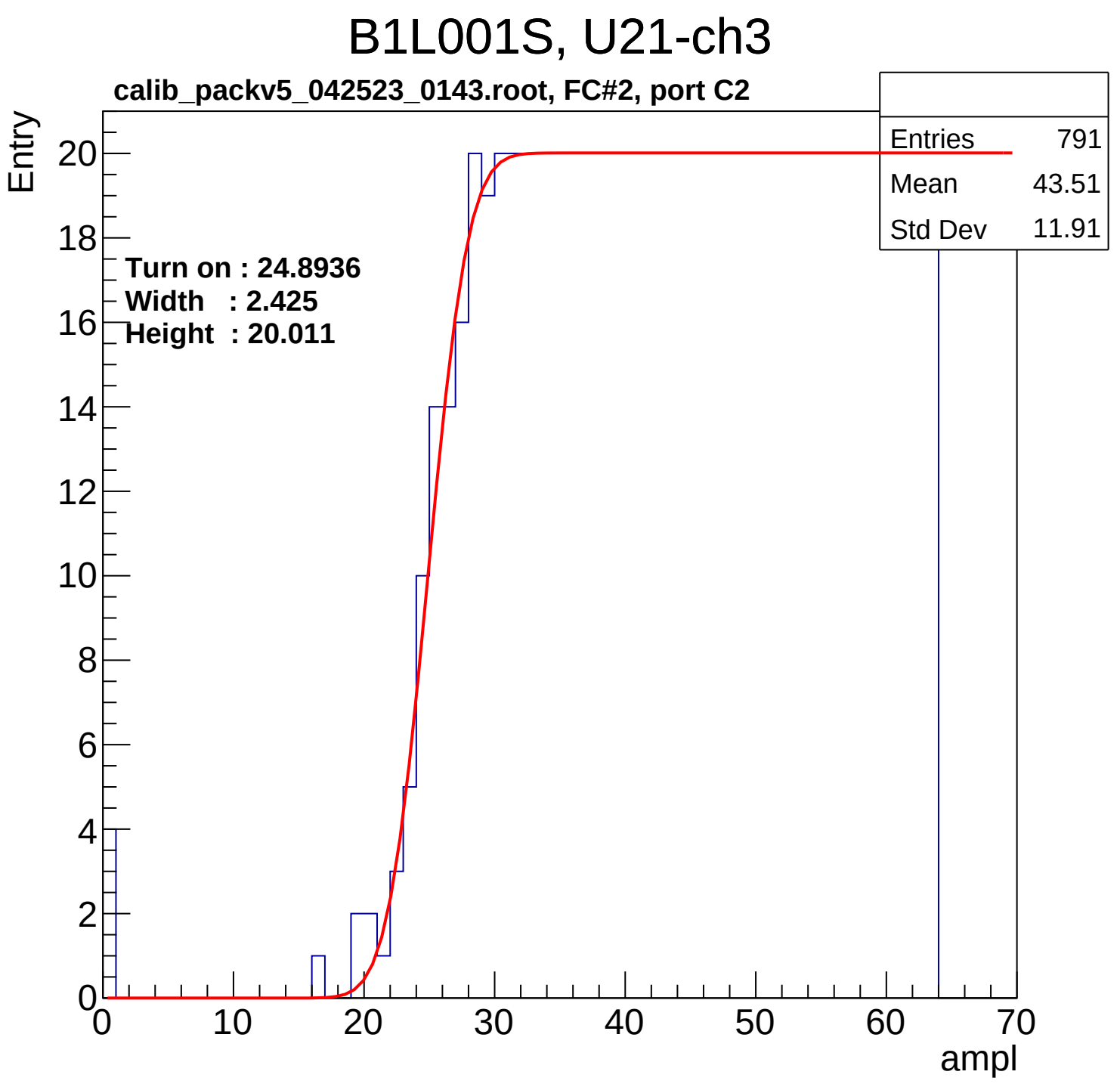
B1L001S, U21-ch3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 791
Mean 43.51
Std Dev 11.91
Turn on : 24.8936
Width : 2.425
Height : 20.011
Entry
ampl
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6
8
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12
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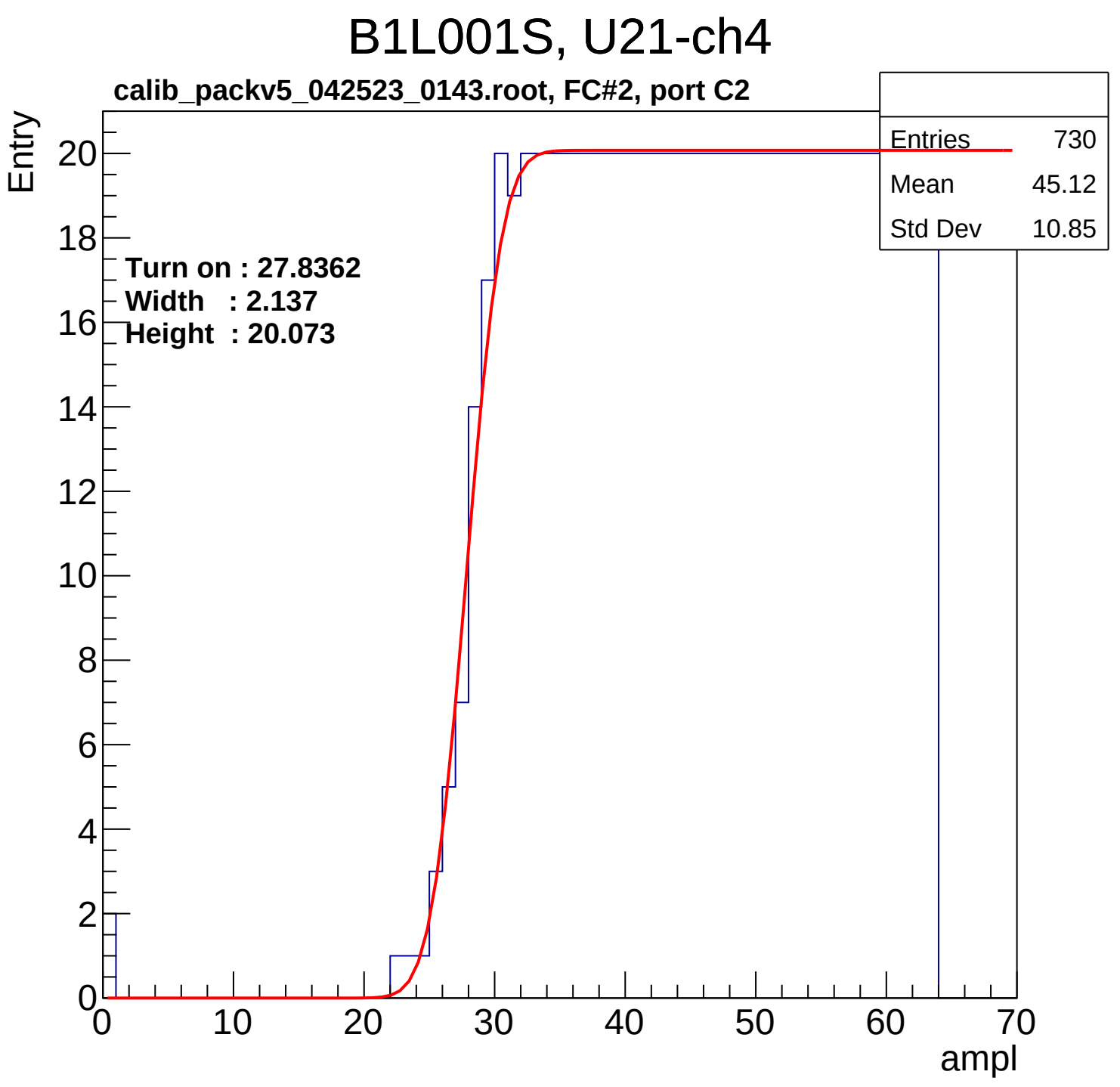
B1L001S, U21-ch4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 730
Mean 45.12
Std Dev 10.85
Turn on : 27.8362
Width : 2.137
Height : 20.073
Entry
ampl
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6
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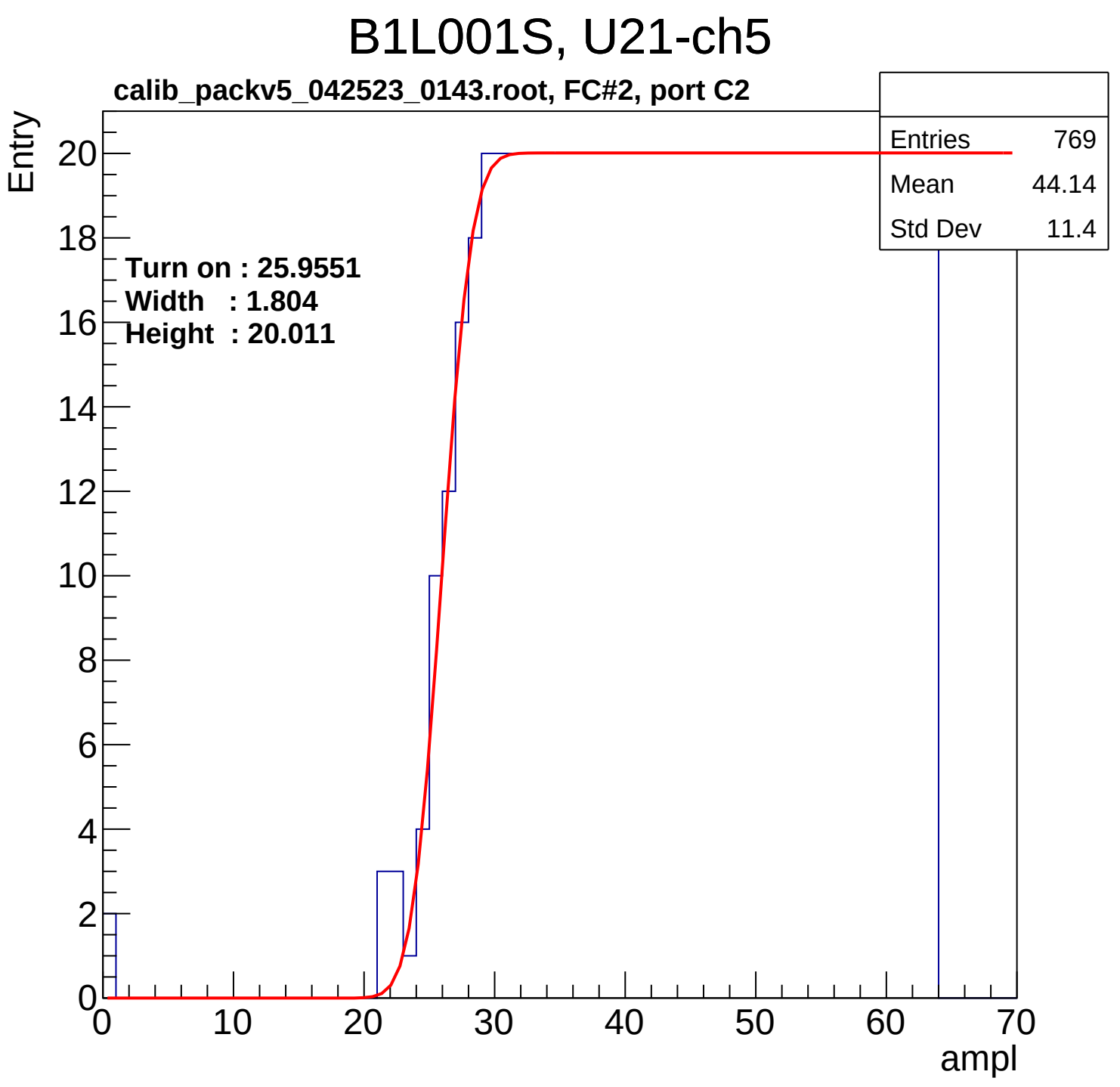
B1L001S, U21-ch5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 769
Mean 44.14
Std Dev 11.4
Turn on : 25.9551
Width : 1.804
Height : 20.011
Entry
ampl
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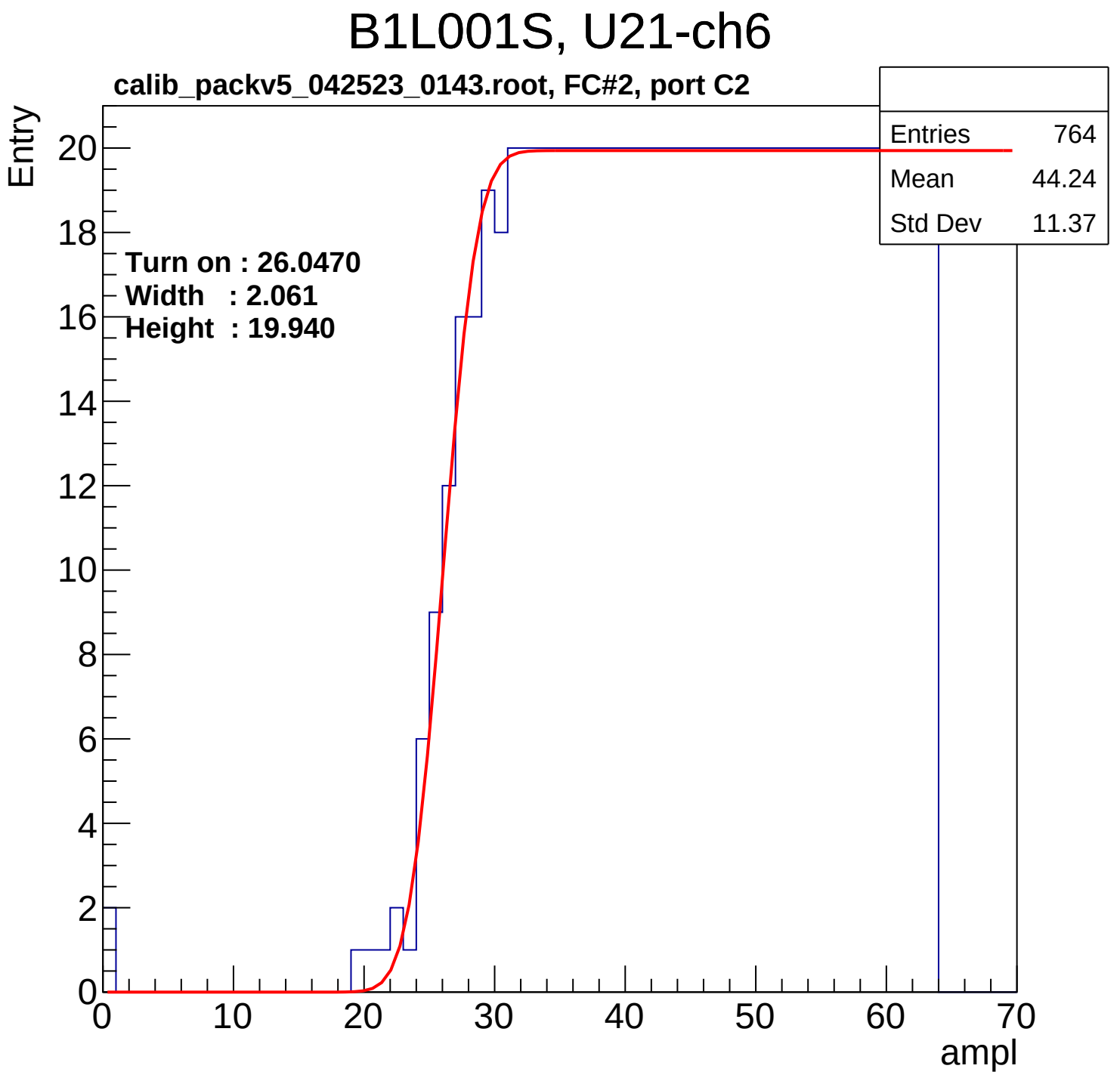
B1L001S, U21-ch6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 764
Mean 44.24
Std Dev 11.37
Turn on : 26.0470
Width : 2.061
Height : 19.940
Entry
ampl
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6
8
10
12
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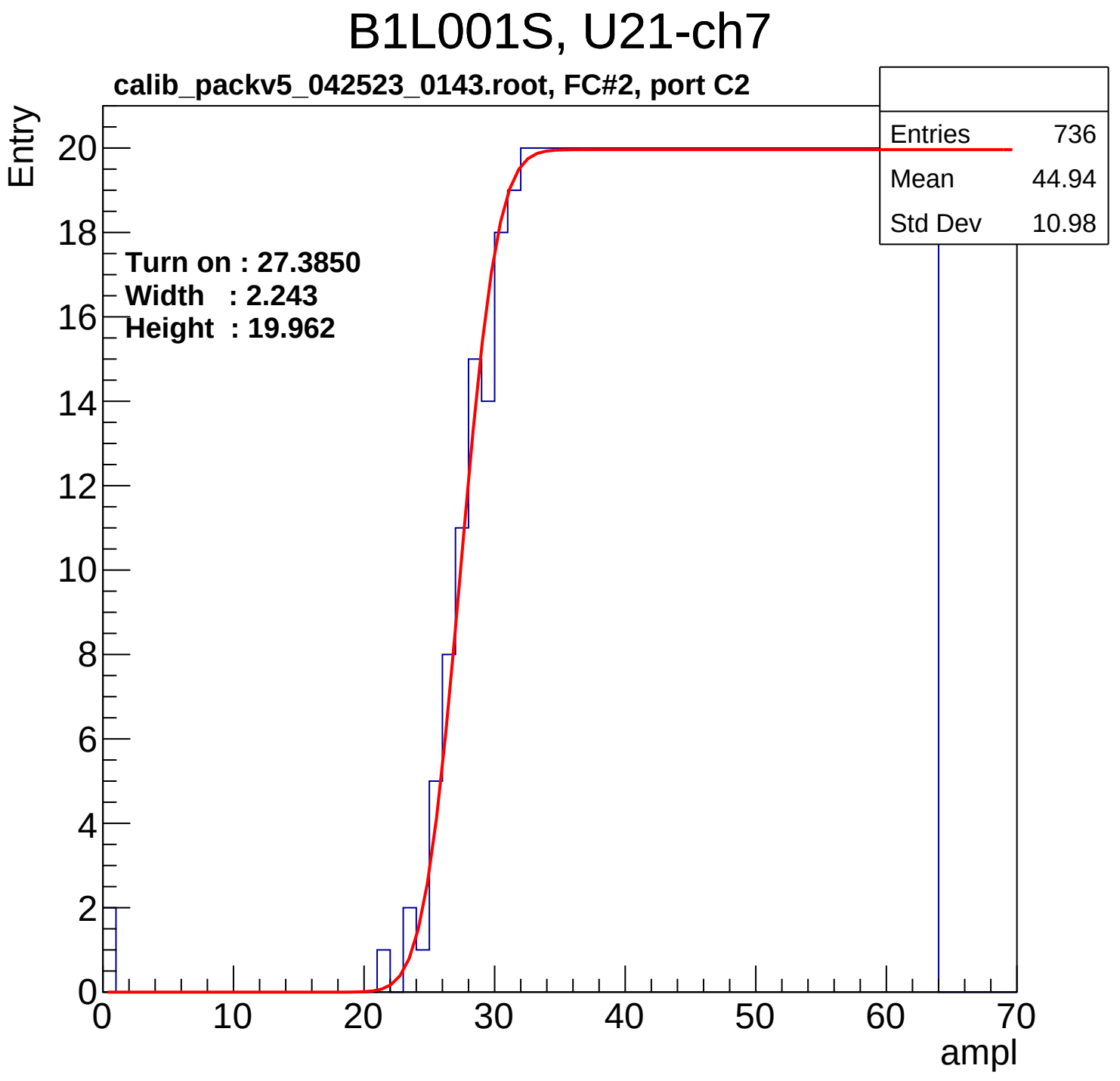
B1L001S, U21-ch7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 736
Mean 44.94
Std Dev 10.98
Turn on : 27.3850
Width : 2.243
Height : 19.962
Entry
ampl
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6
8
10
12
14
16
18
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0
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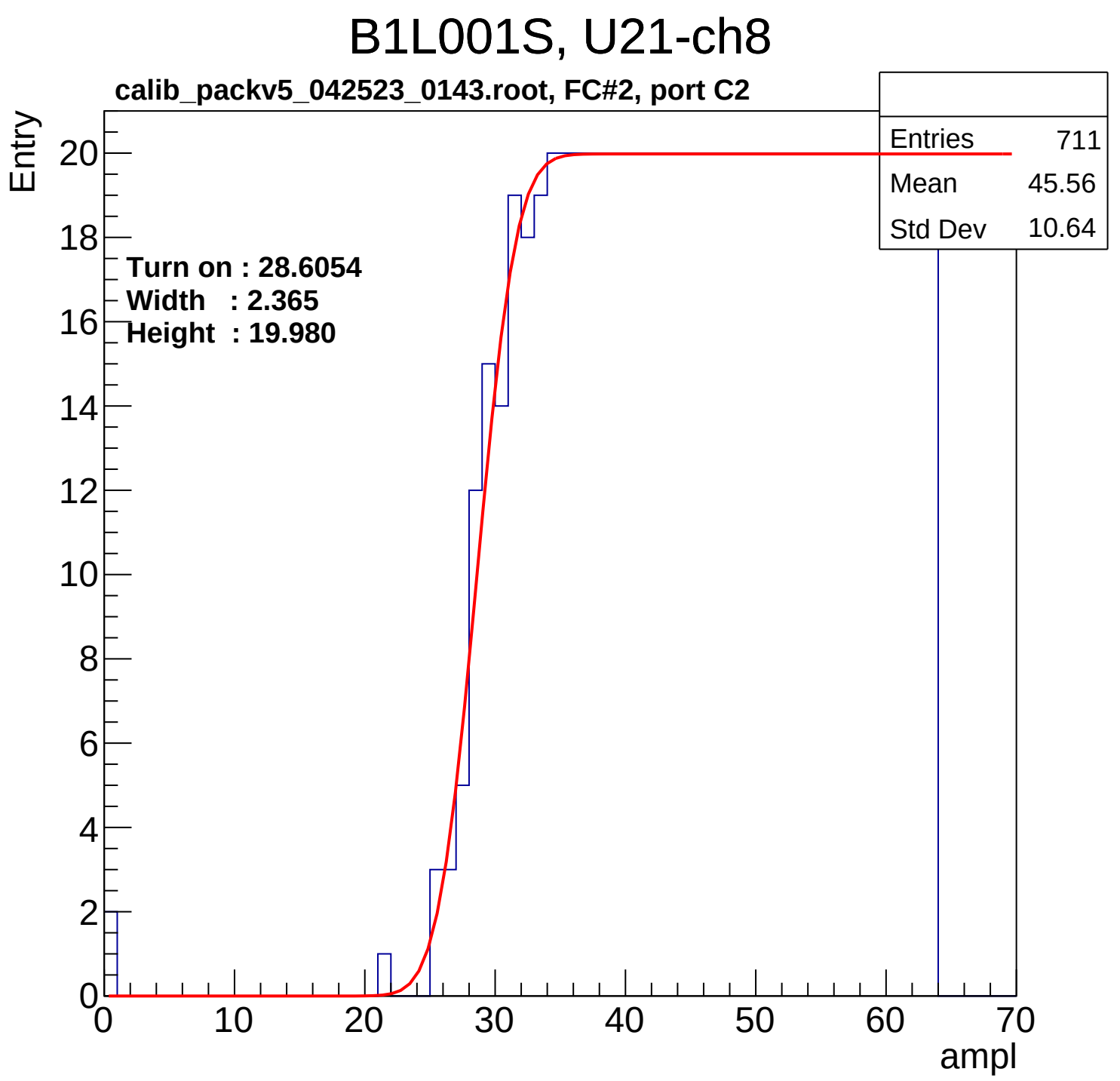
B1L001S, U21-ch8
calib_packv5_042523_0143.root, FC#2, port C2
Entries 711
Mean 45.56
Std Dev 10.64
Turn on : 28.6054
Width : 2.365
Height : 19.980
Entry
ampl
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6
8
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12
14
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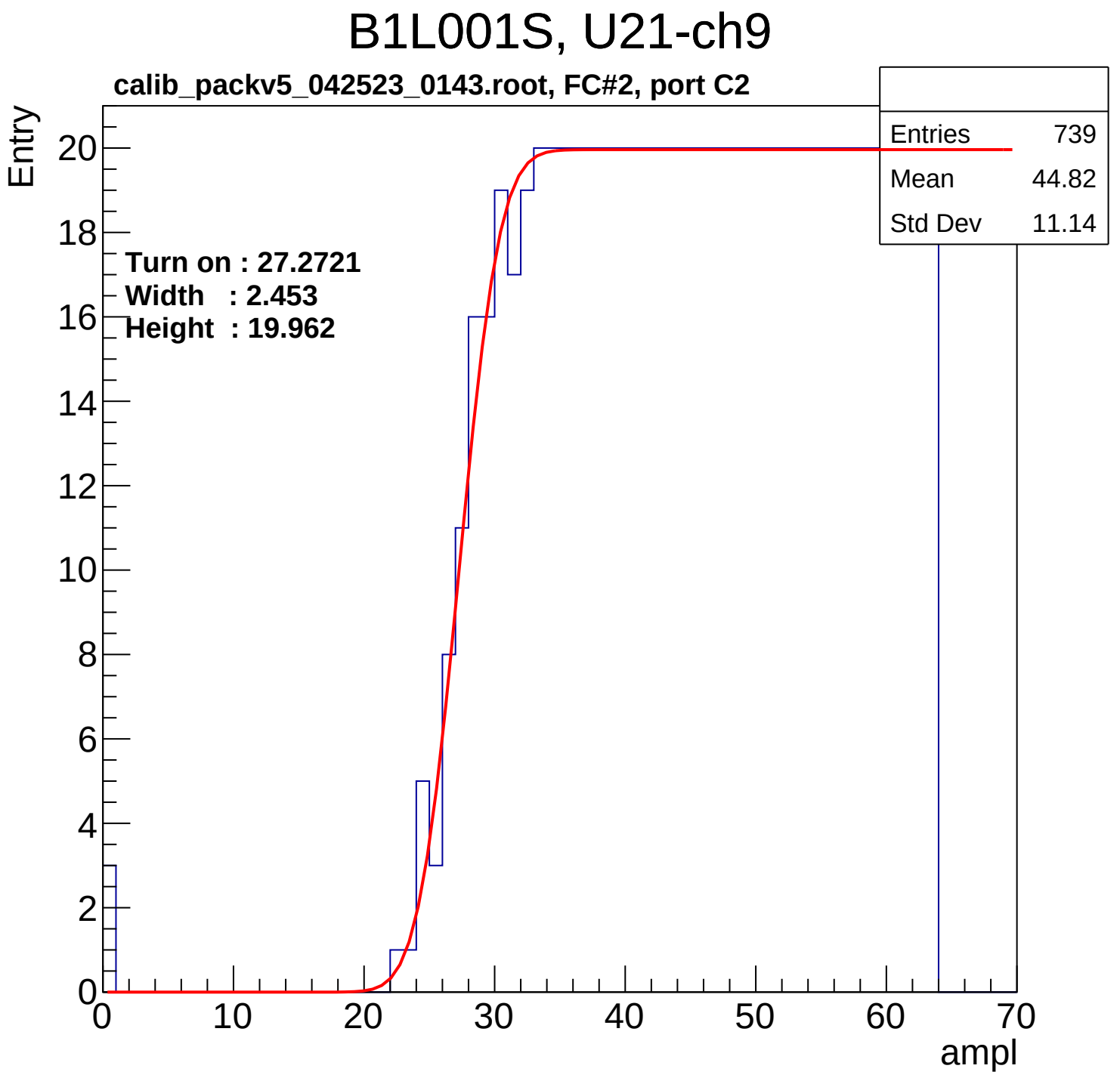
B1L001S, U21-ch9
calib_packv5_042523_0143.root, FC#2, port C2
Entries 739
Mean 44.82
Std Dev 11.14
Turn on : 27.2721
Width : 2.453
Height : 19.962
Entry
ampl
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6
8
10
12
14
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18
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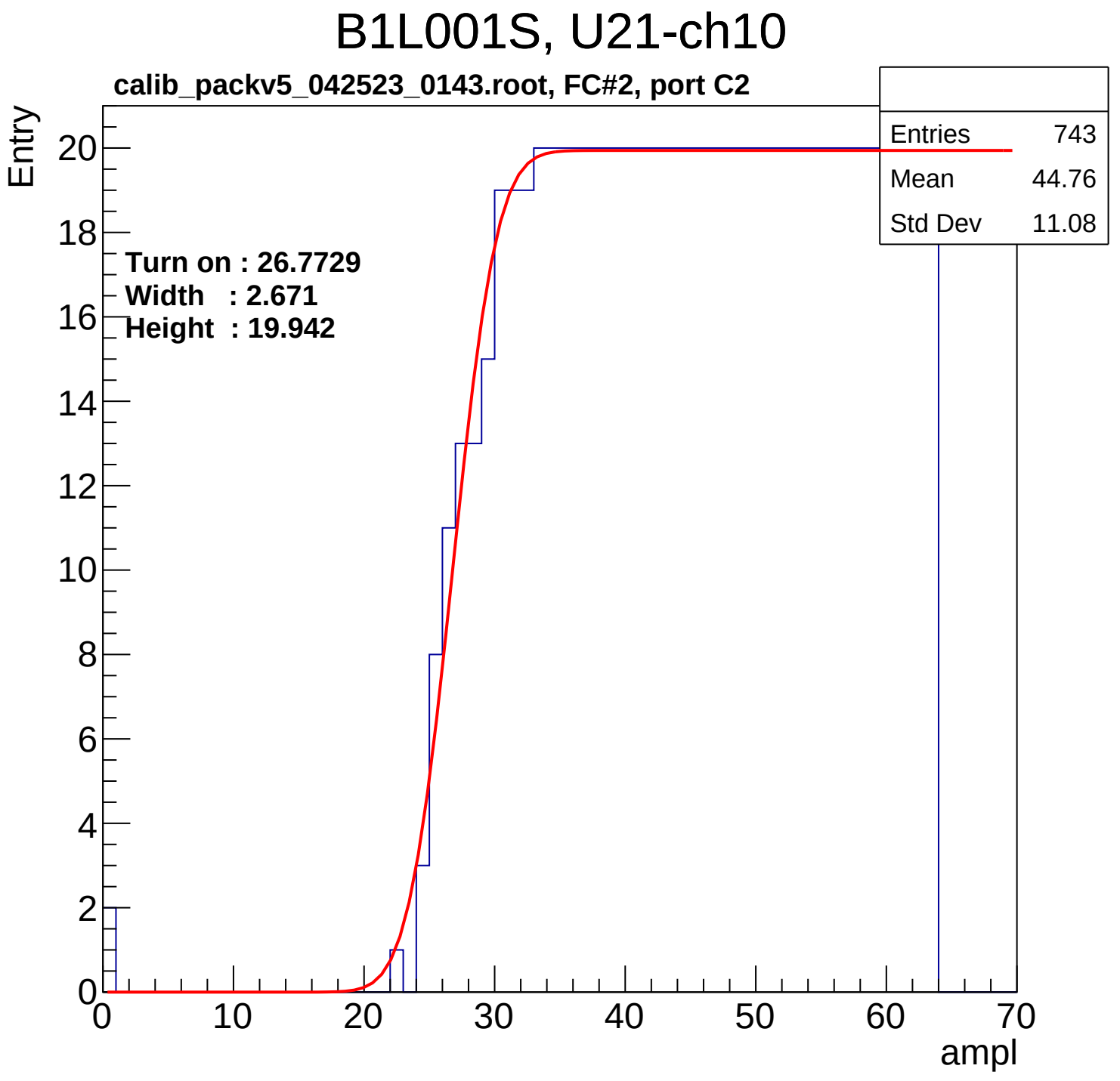
B1L001S, U21-ch10
calib_packv5_042523_0143.root, FC#2, port C2
Entries 743
Mean 44.76
Std Dev 11.08
Turn on : 26.7729
Width : 2.671
Height : 19.942
Entry
ampl
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6
8
10
12
14
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18
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0
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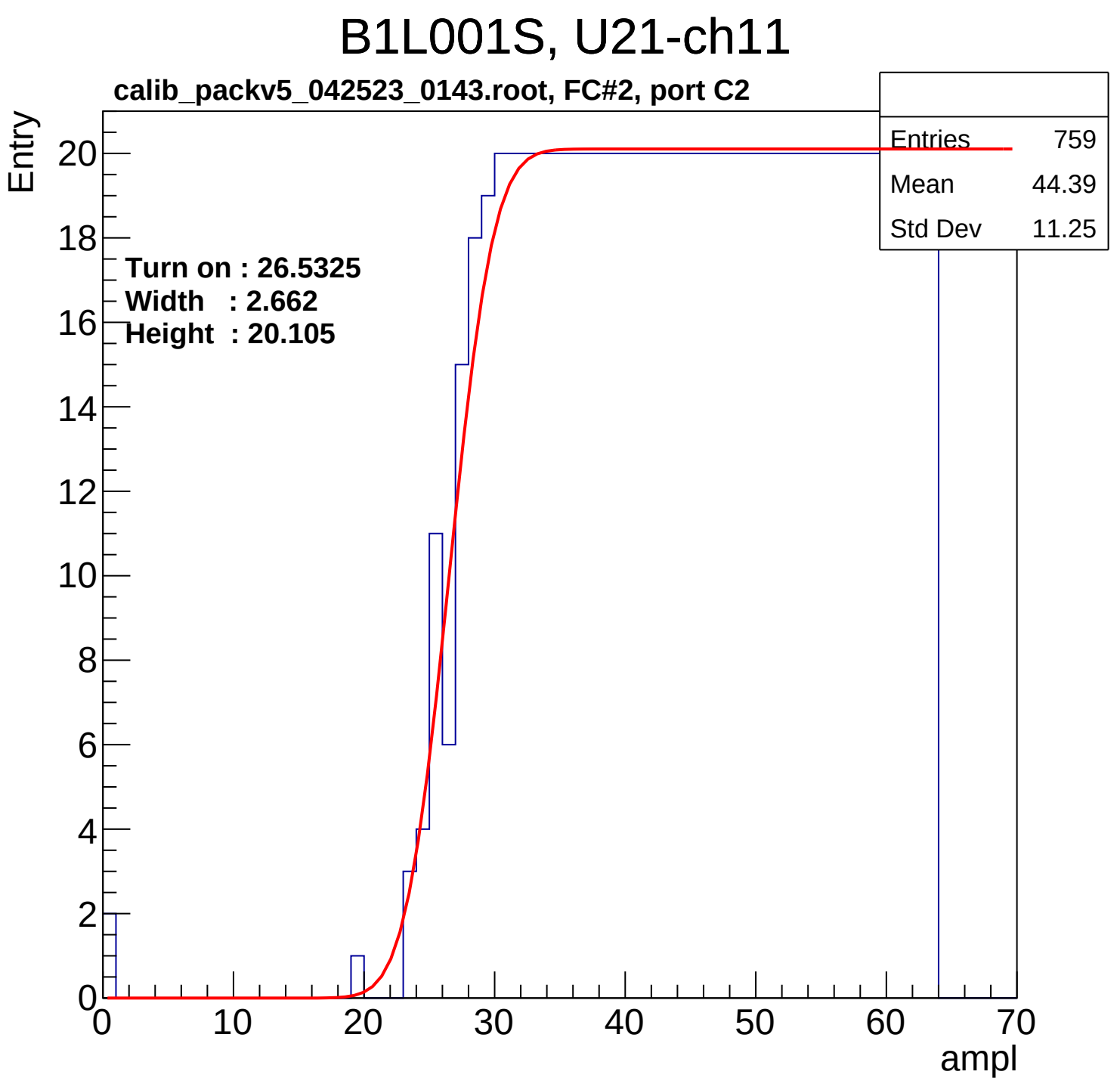
B1L001S, U21-ch11
calib_packv5_042523_0143.root, FC#2, port C2
Entries 759
Mean 44.39
Std Dev 11.25
Turn on : 26.5325
Width : 2.662
Height : 20.105
Entry
ampl
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6
8
10
12
14
16
18
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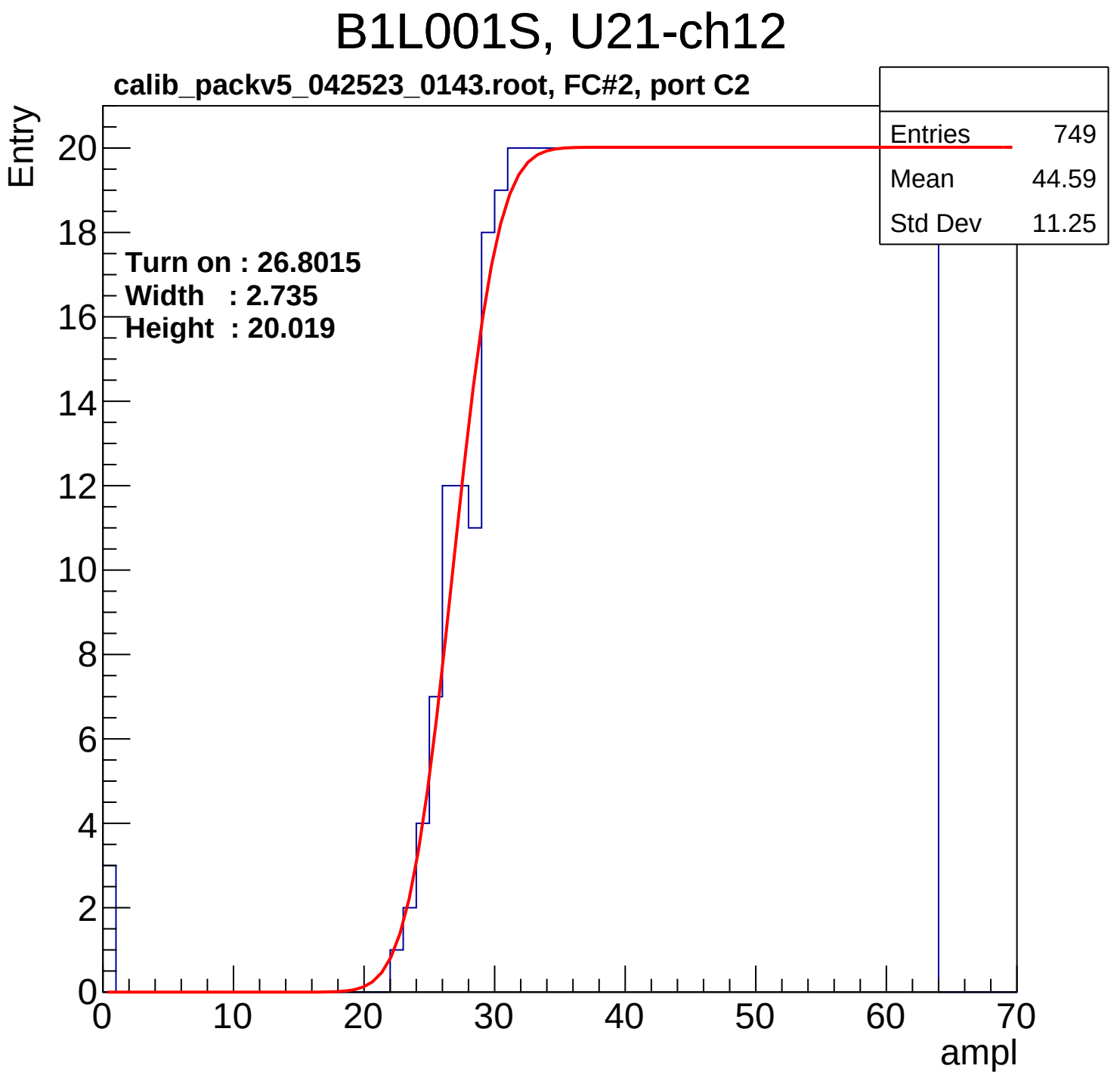
B1L001S, U21-ch12
calib_packv5_042523_0143.root, FC#2, port C2
Entries 749
Mean 44.59
Std Dev 11.25
Turn on : 26.8015
Width : 2.735
Height : 20.019
Entry
ampl
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6
8
10
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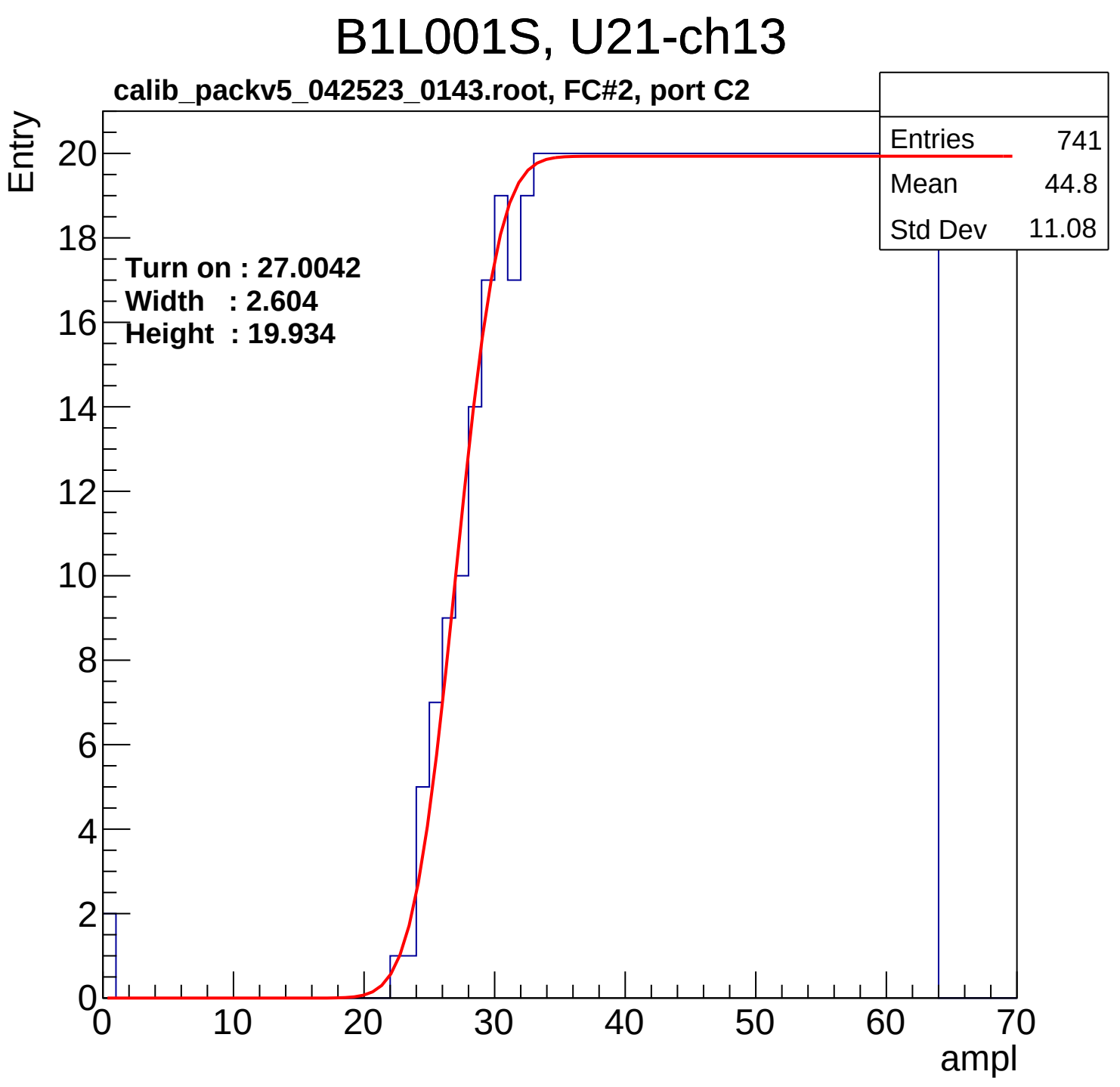
B1L001S, U21-ch13
calib_packv5_042523_0143.root, FC#2, port C2
Entries 741
Mean 44.8
Std Dev 11.08
Turn on : 27.0042
Width : 2.604
Height : 19.934
Entry
ampl
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8
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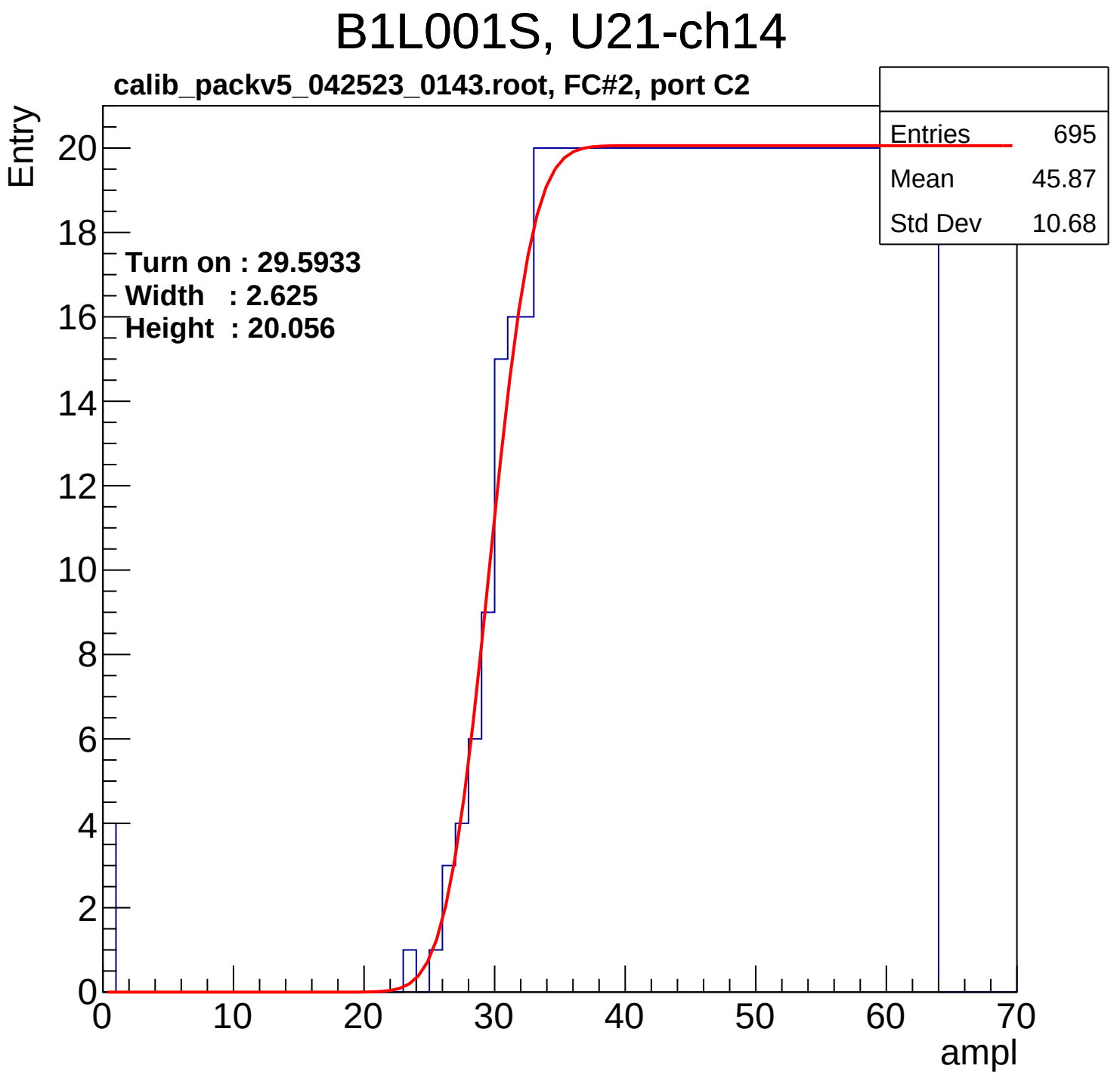
B1L001S, U21-ch14
calib_packv5_042523_0143.root, FC#2, port C2
Entries 695
Mean 45.87
Std Dev 10.68
Turn on : 29.5933
Width : 2.625
Height : 20.056
Entry
ampl
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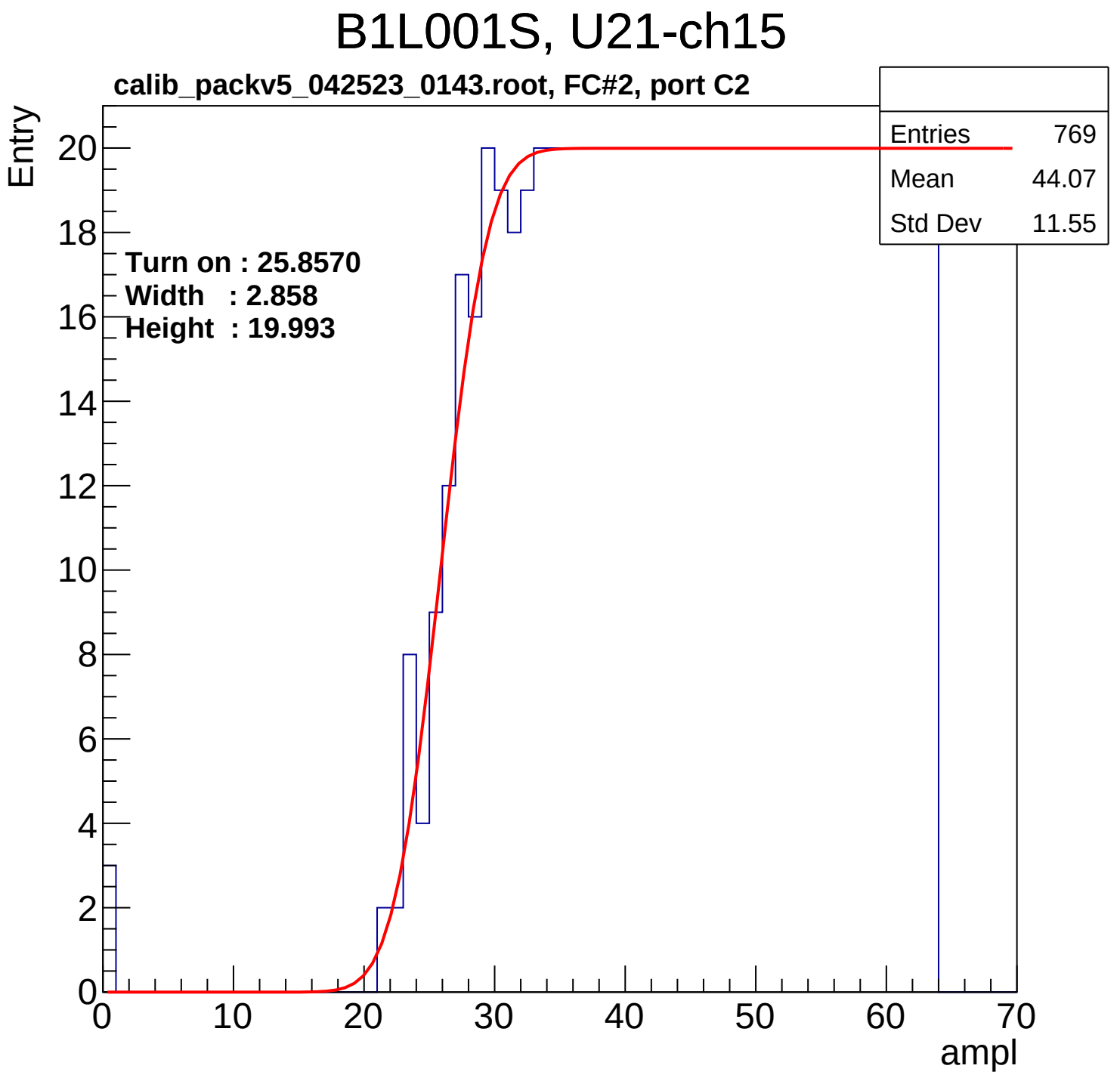
B1L001S, U21-ch15
calib_packv5_042523_0143.root, FC#2, port C2
Entries 769
Mean 44.07
Std Dev 11.55
Turn on : 25.8570
Width : 2.858
Height : 19.993
Entry
ampl
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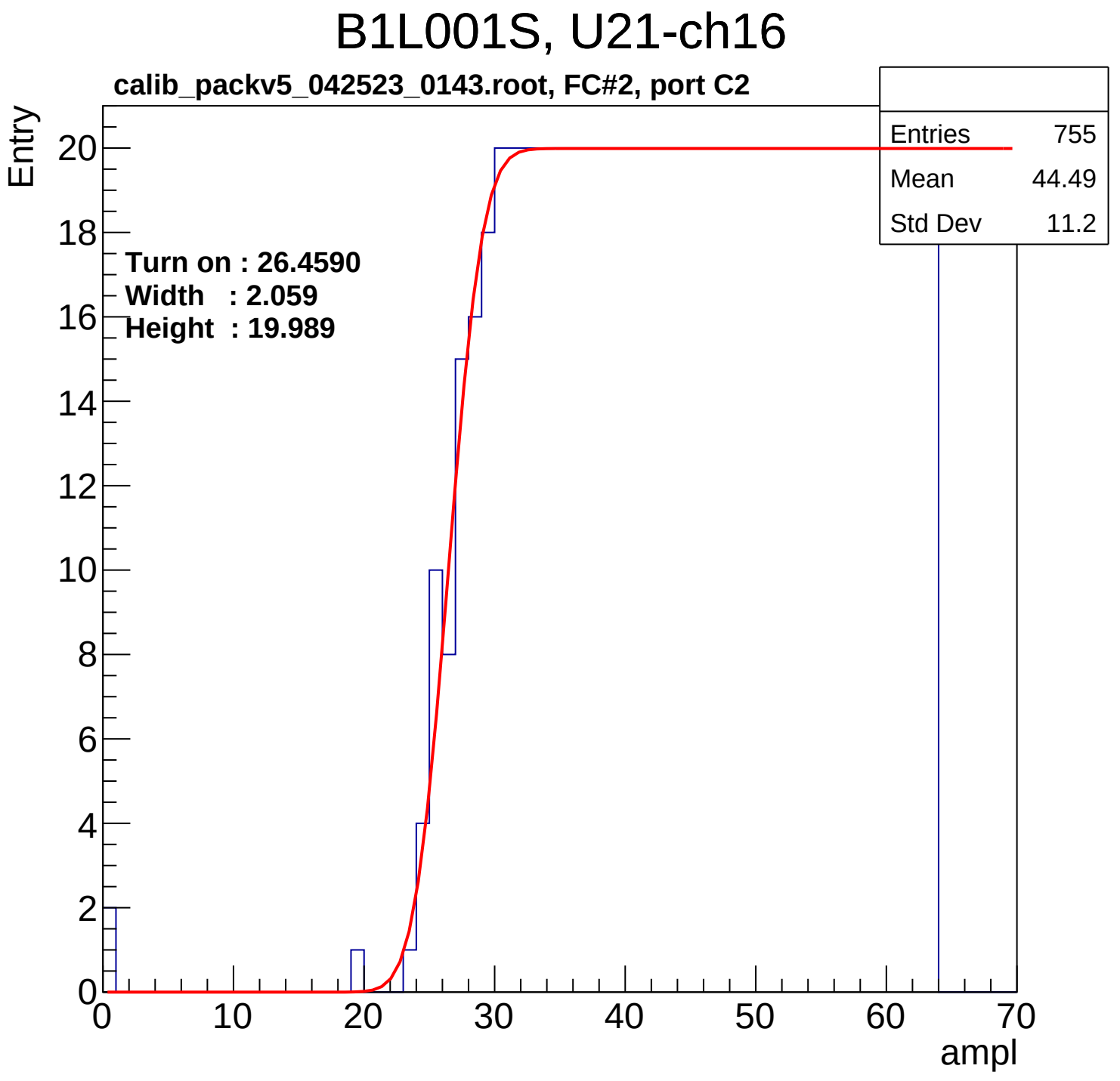
B1L001S, U21-ch16
calib_packv5_042523_0143.root, FC#2, port C2
Entries 755
Mean 44.49
Std Dev 11.2
Turn on : 26.4590
Width : 2.059
Height : 19.989
Entry
ampl
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6
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10
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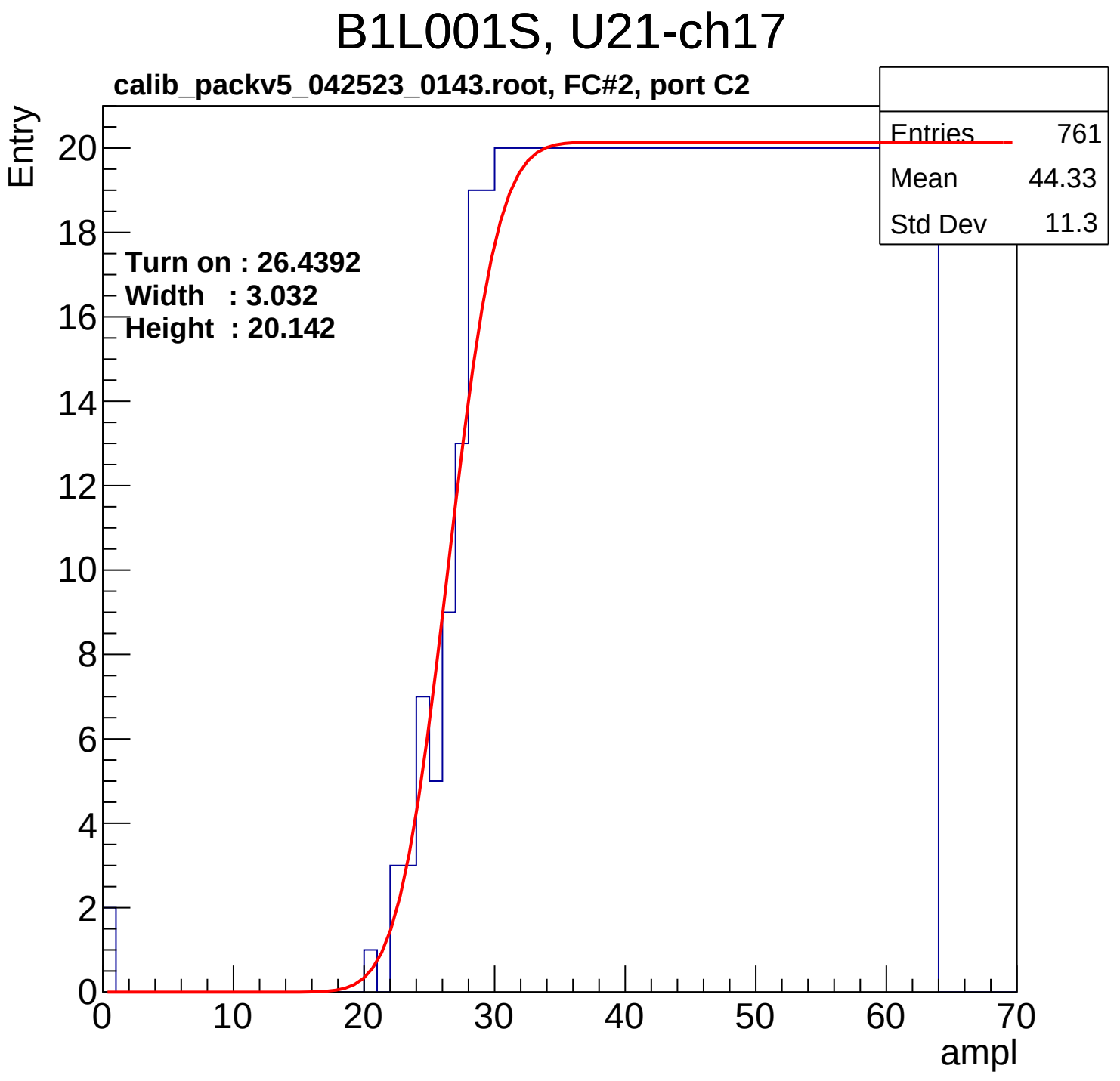
B1L001S, U21-ch17
calib_packv5_042523_0143.root, FC#2, port C2
Entries 761
Mean 44.33
Std Dev 11.3
Turn on : 26.4392
Width : 3.032
Height : 20.142
Entry
ampl
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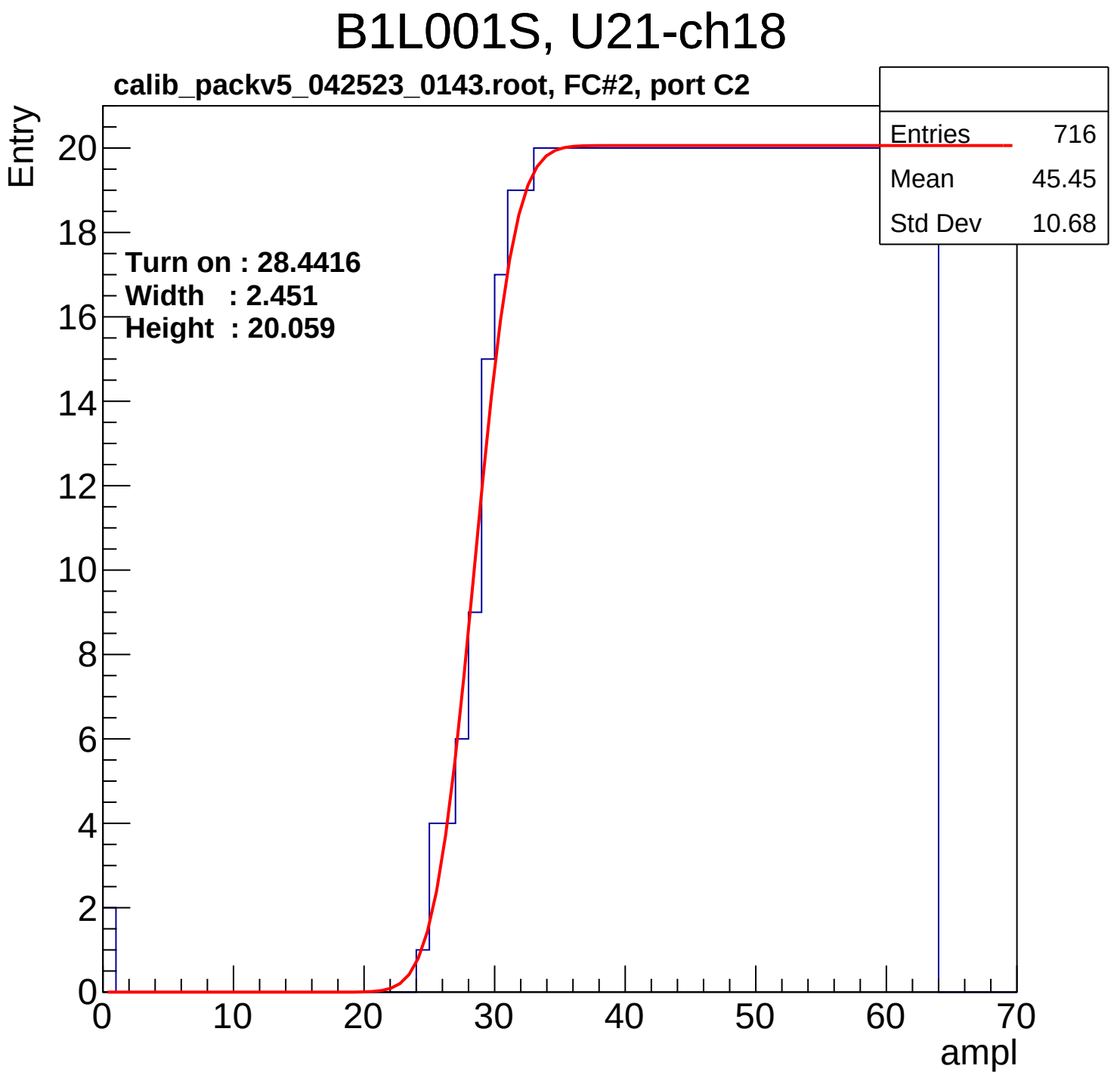
B1L001S, U21-ch18
calib_packv5_042523_0143.root, FC#2, port C2
Entries 716
Mean 45.45
Std Dev 10.68
Turn on : 28.4416
Width : 2.451
Height : 20.059
Entry
ampl
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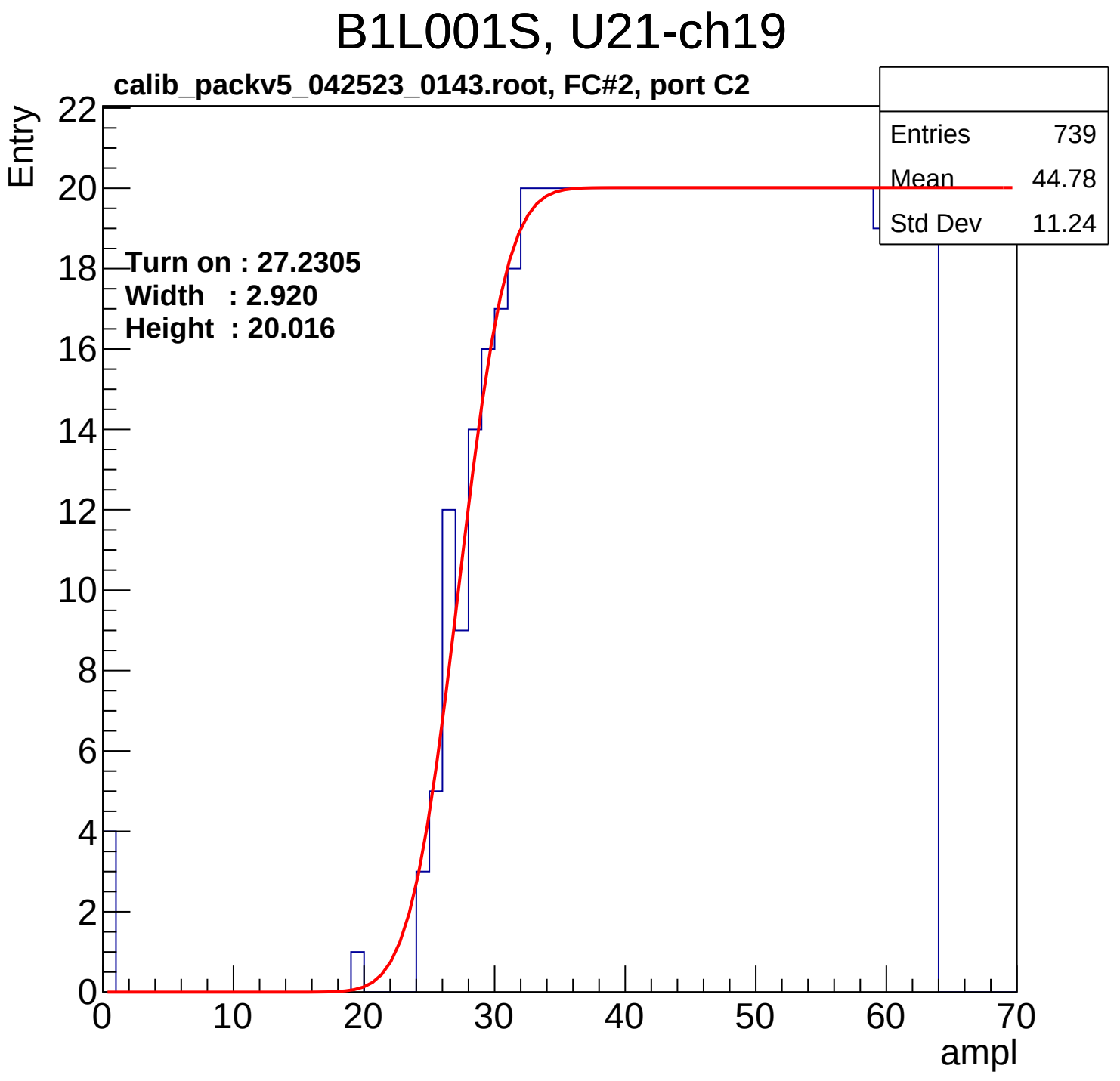
B1L001S, U21-ch19
calib_packv5_042523_0143.root, FC#2, port C2
Entries 739
Mean 44.78
Std Dev 11.24
Turn on : 27.2305
Width : 2.920
Height : 20.016
Entry
ampl
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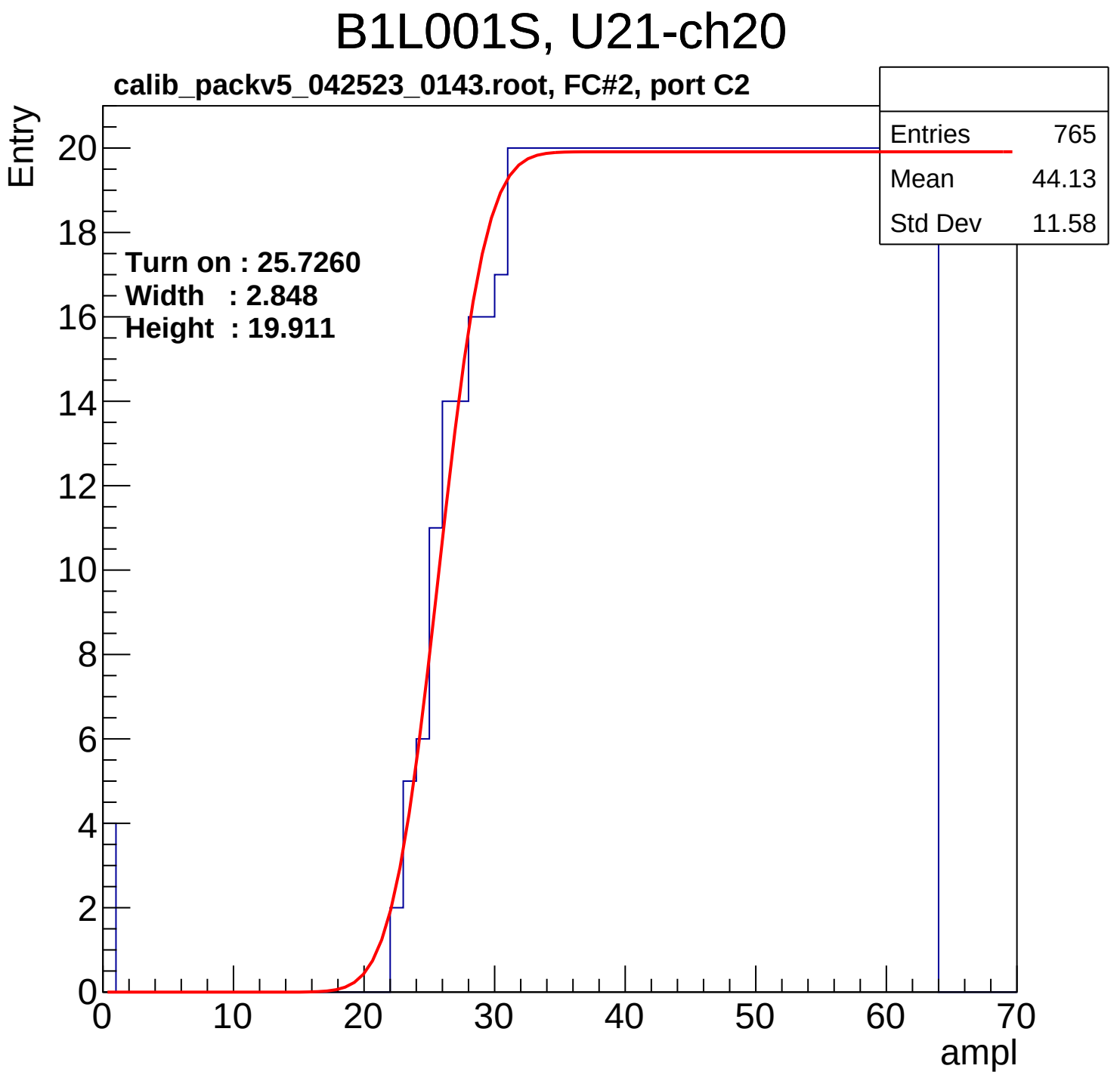
B1L001S, U21-ch20
calib_packv5_042523_0143.root, FC#2, port C2
Entries 765
Mean 44.13
Std Dev 11.58
Turn on : 25.7260
Width : 2.848
Height : 19.911
Entry
ampl
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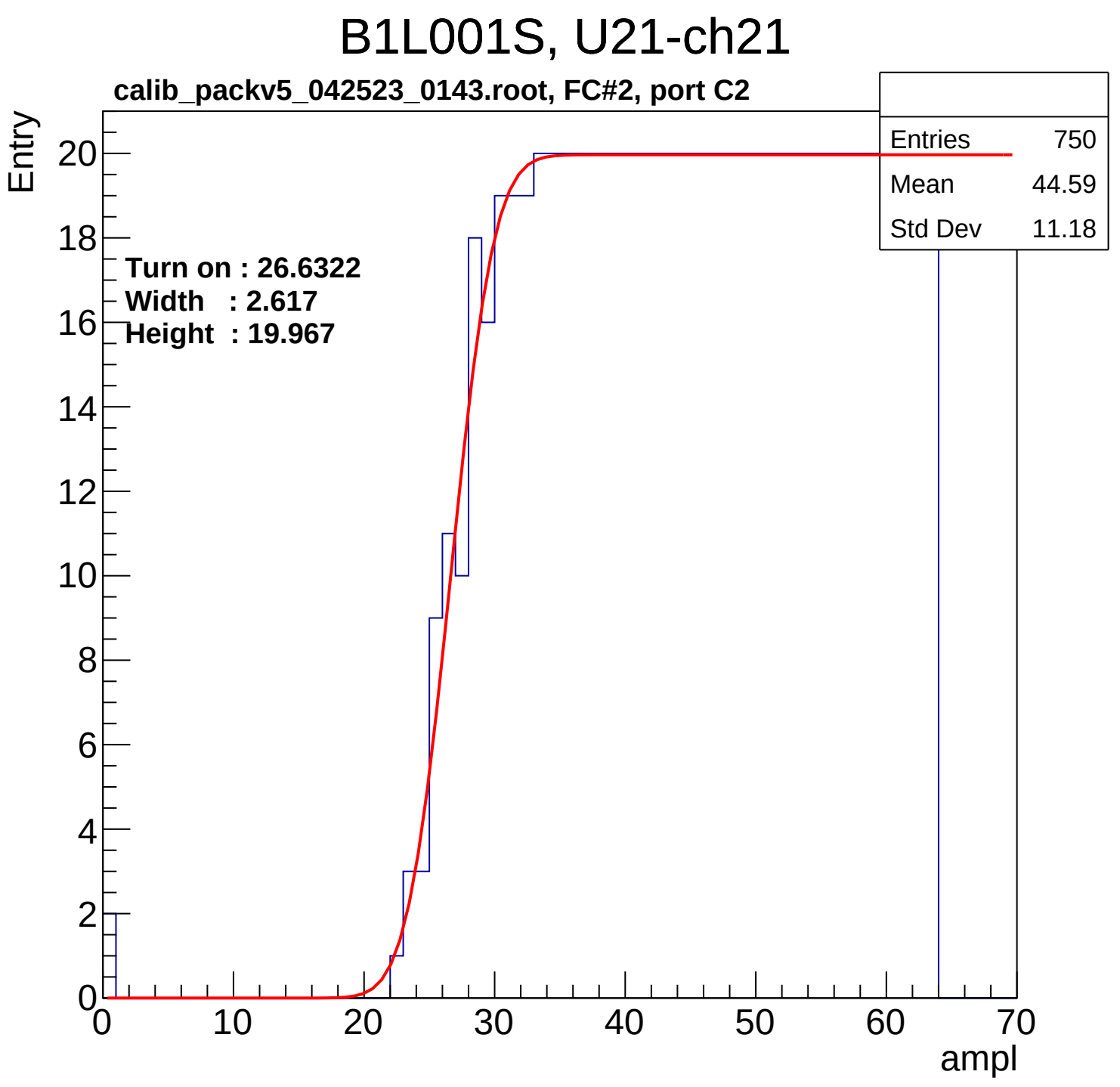
B1L001S, U21-ch21
calib_packv5_042523_0143.root, FC#2, port C2
Entries 750
Mean 44.59
Std Dev 11.18
Turn on : 26.6322
Width : 2.617
Height : 19.967
Entry
ampl
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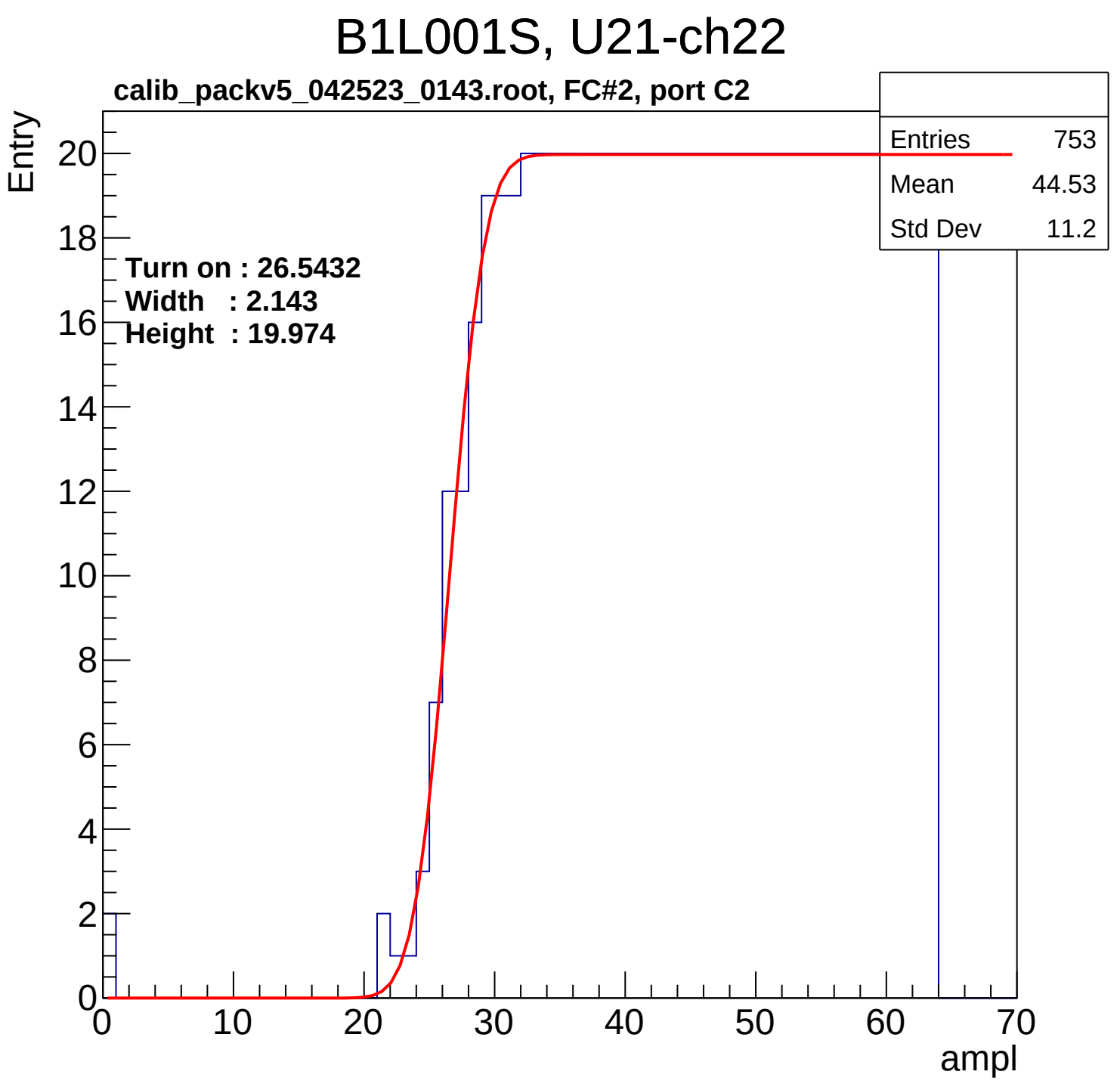
B1L001S, U21-ch22
calib_packv5_042523_0143.root, FC#2, port C2
Entries 753
Mean 44.53
Std Dev 11.2
Turn on : 26.5432
Width : 2.143
Height : 19.974
Entry
ampl
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8
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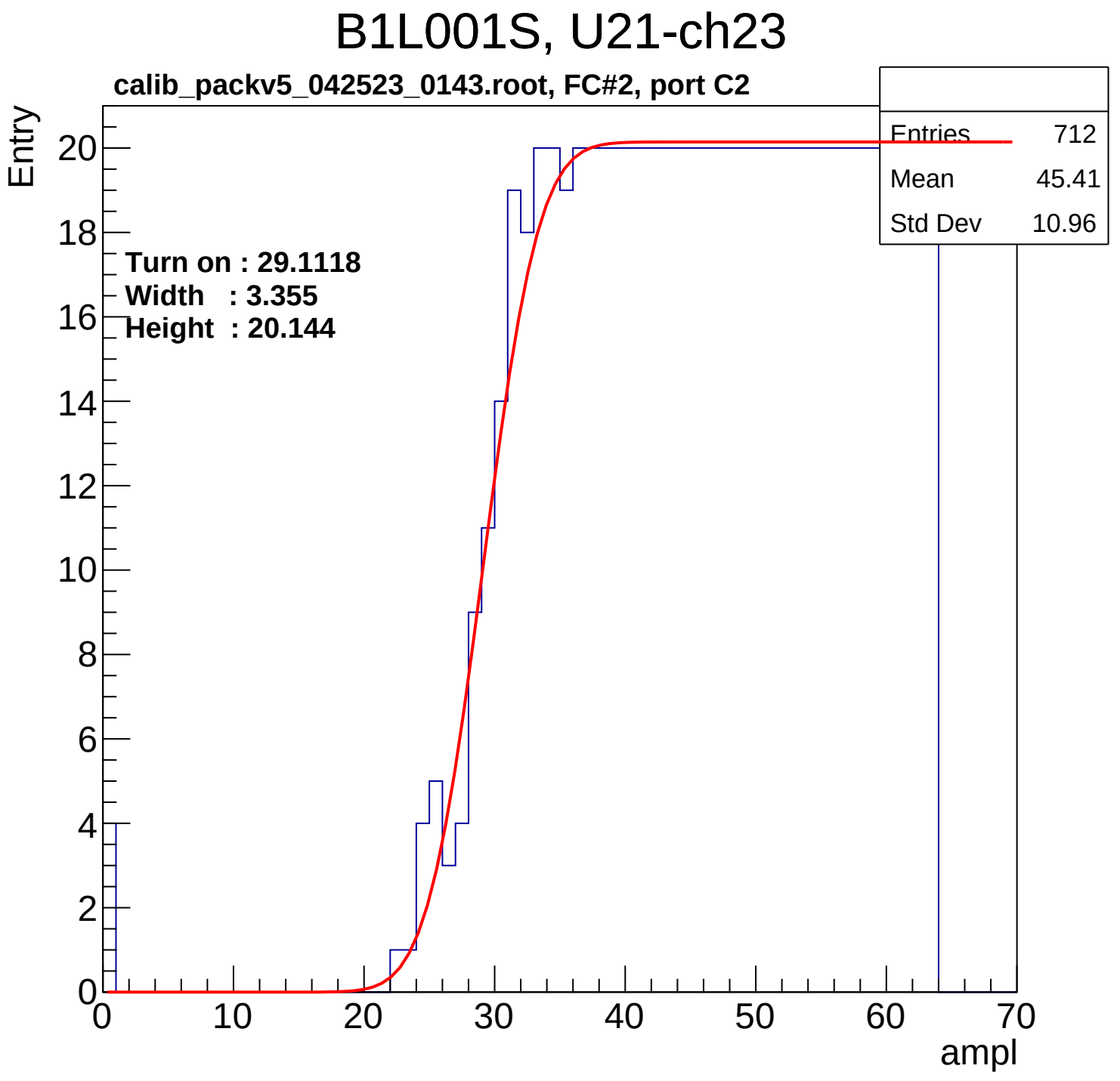
B1L001S, U21-ch23
calib_packv5_042523_0143.root, FC#2, port C2
Entries 712
Mean 45.41
Std Dev 10.96
Turn on : 29.1118
Width : 3.355
Height : 20.144
Entry
ampl
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6
8
10
12
14
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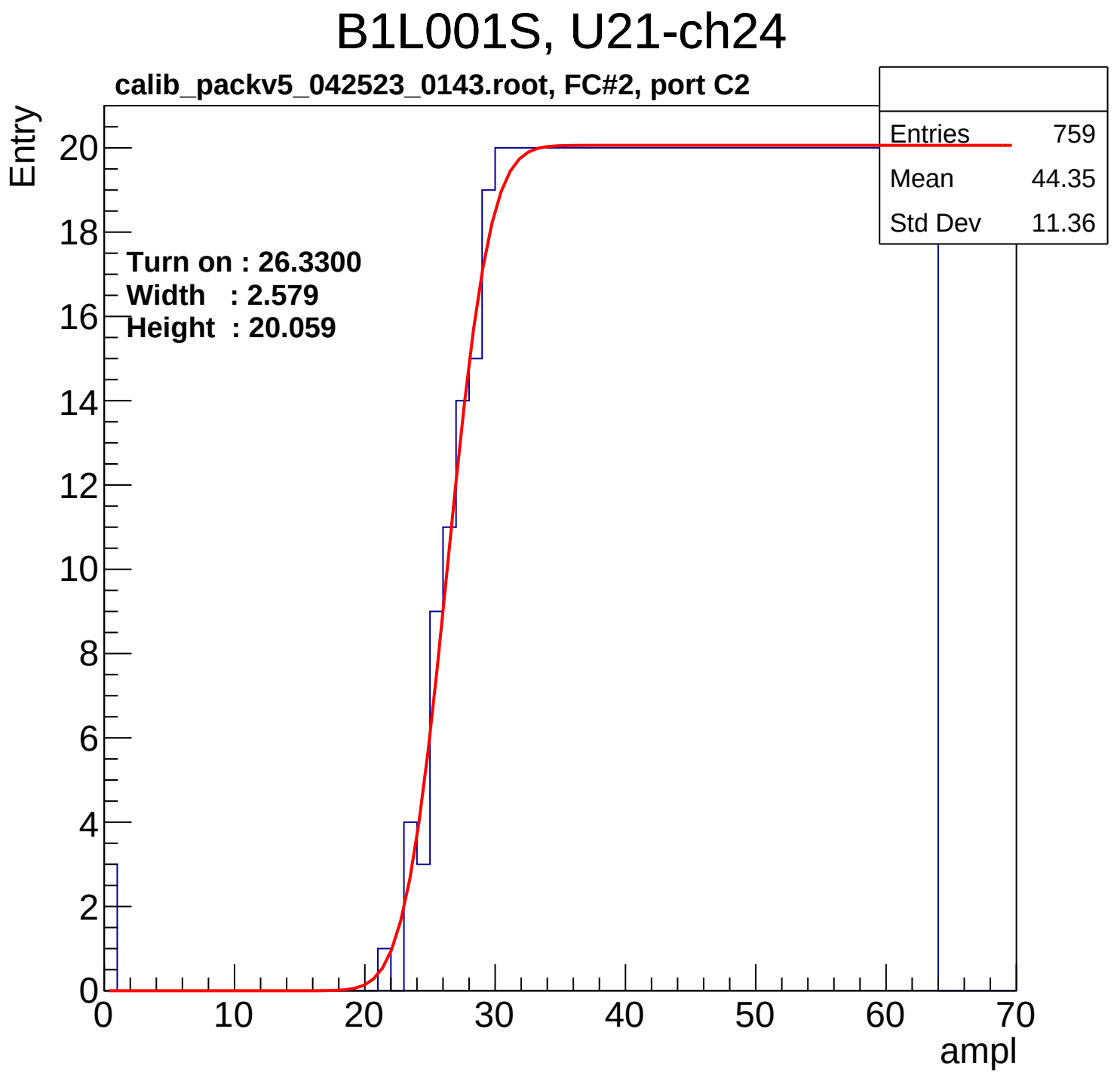
B1L001S, U21-ch24
calib_packv5_042523_0143.root, FC#2, port C2
Entries 759
Mean 44.35
Std Dev 11.36
Turn on : 26.3300
Width : 2.579
Height : 20.059
Entry
ampl
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6
8
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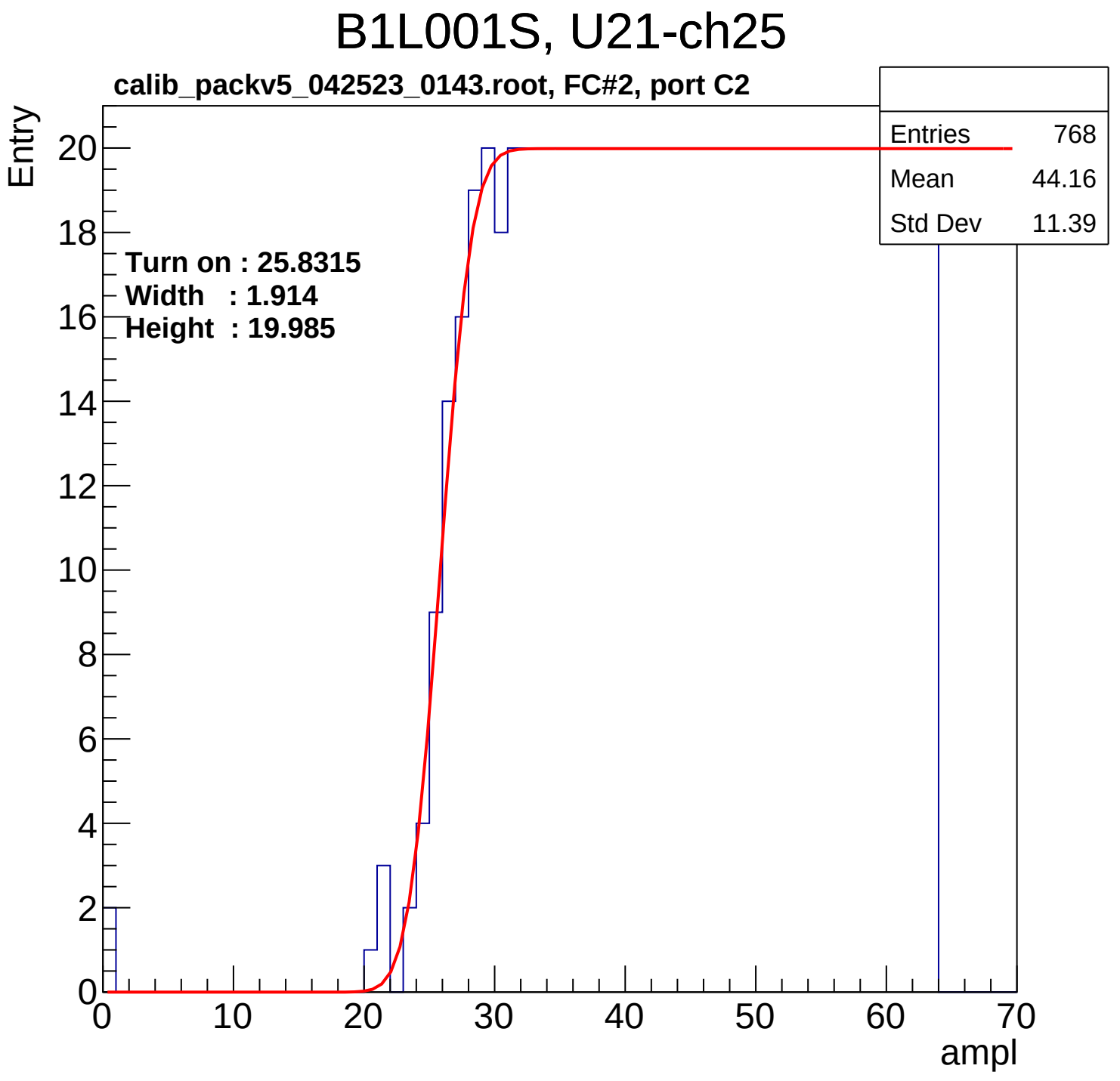
B1L001S, U21-ch25
calib_packv5_042523_0143.root, FC#2, port C2
Entries 768
Mean 44.16
Std Dev 11.39
Turn on : 25.8315
Width : 1.914
Height : 19.985
Entry
ampl
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6
8
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16
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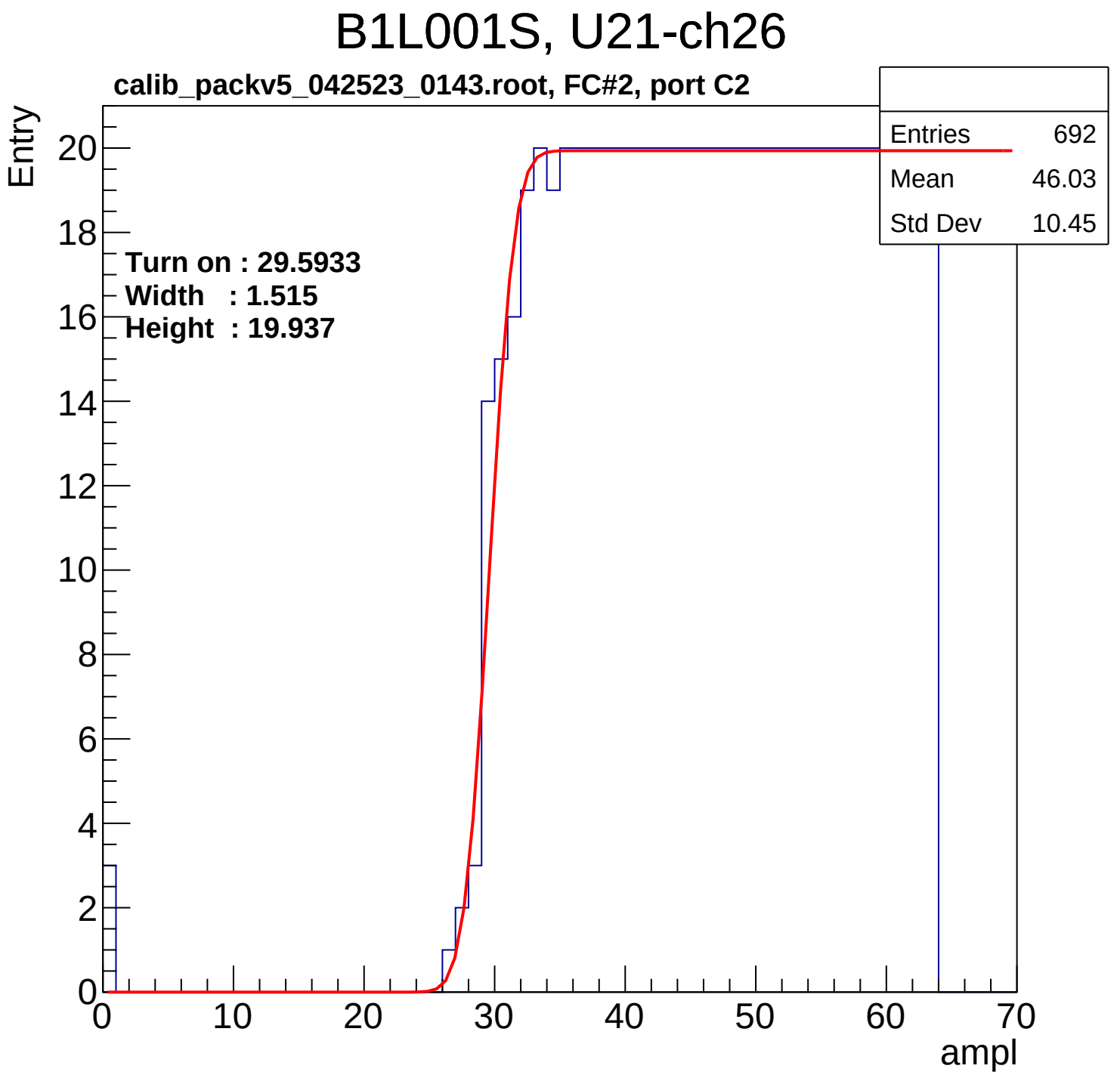
B1L001S, U21-ch26
calib_packv5_042523_0143.root, FC#2, port C2
Entries 692
Mean 46.03
Std Dev 10.45
Turn on : 29.5933
Width : 1.515
Height : 19.937
Entry
ampl
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6
8
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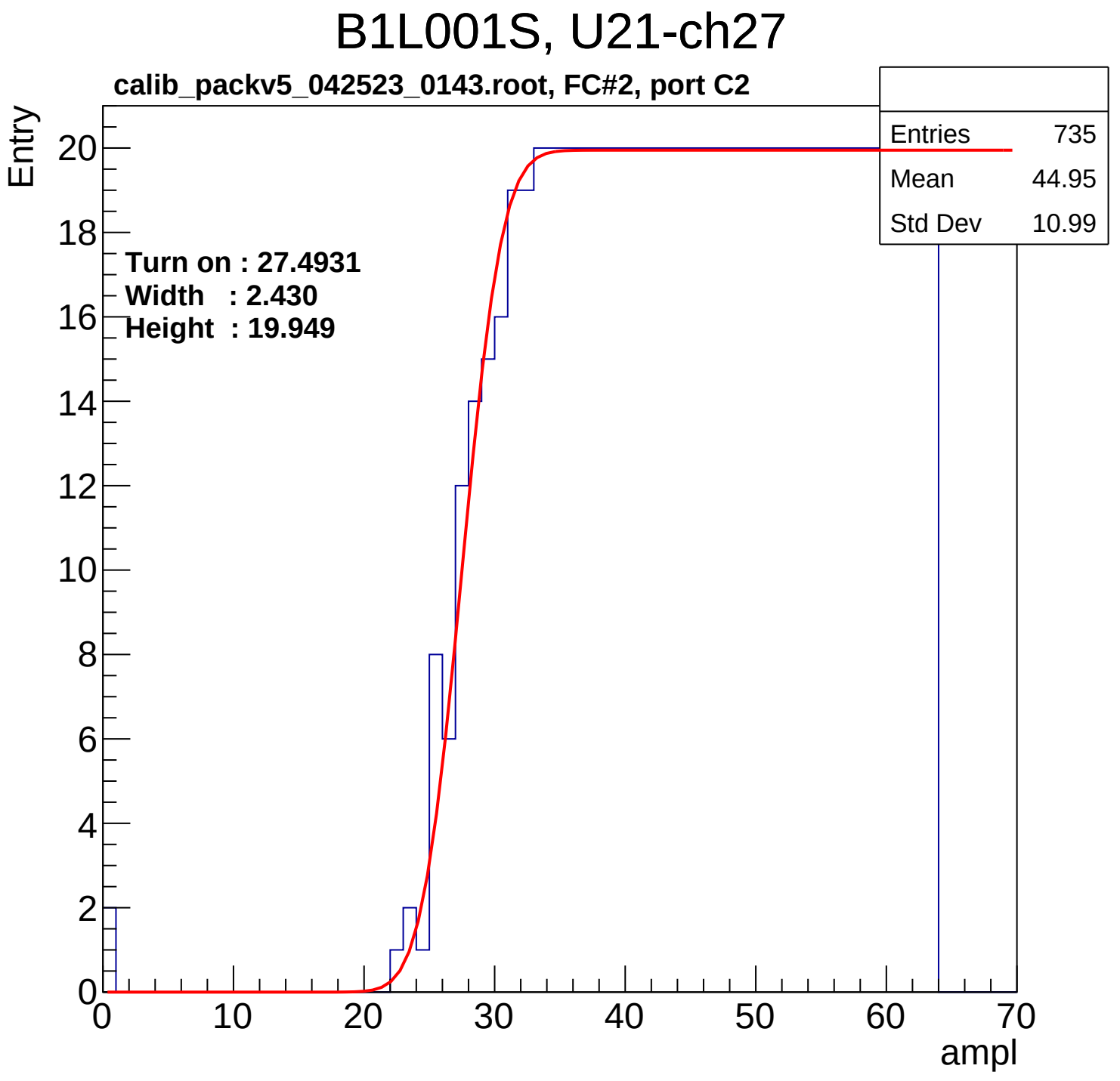
B1L001S, U21-ch27
calib_packv5_042523_0143.root, FC#2, port C2
Entries 735
Mean 44.95
Std Dev 10.99
Turn on : 27.4931
Width : 2.430
Height : 19.949
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
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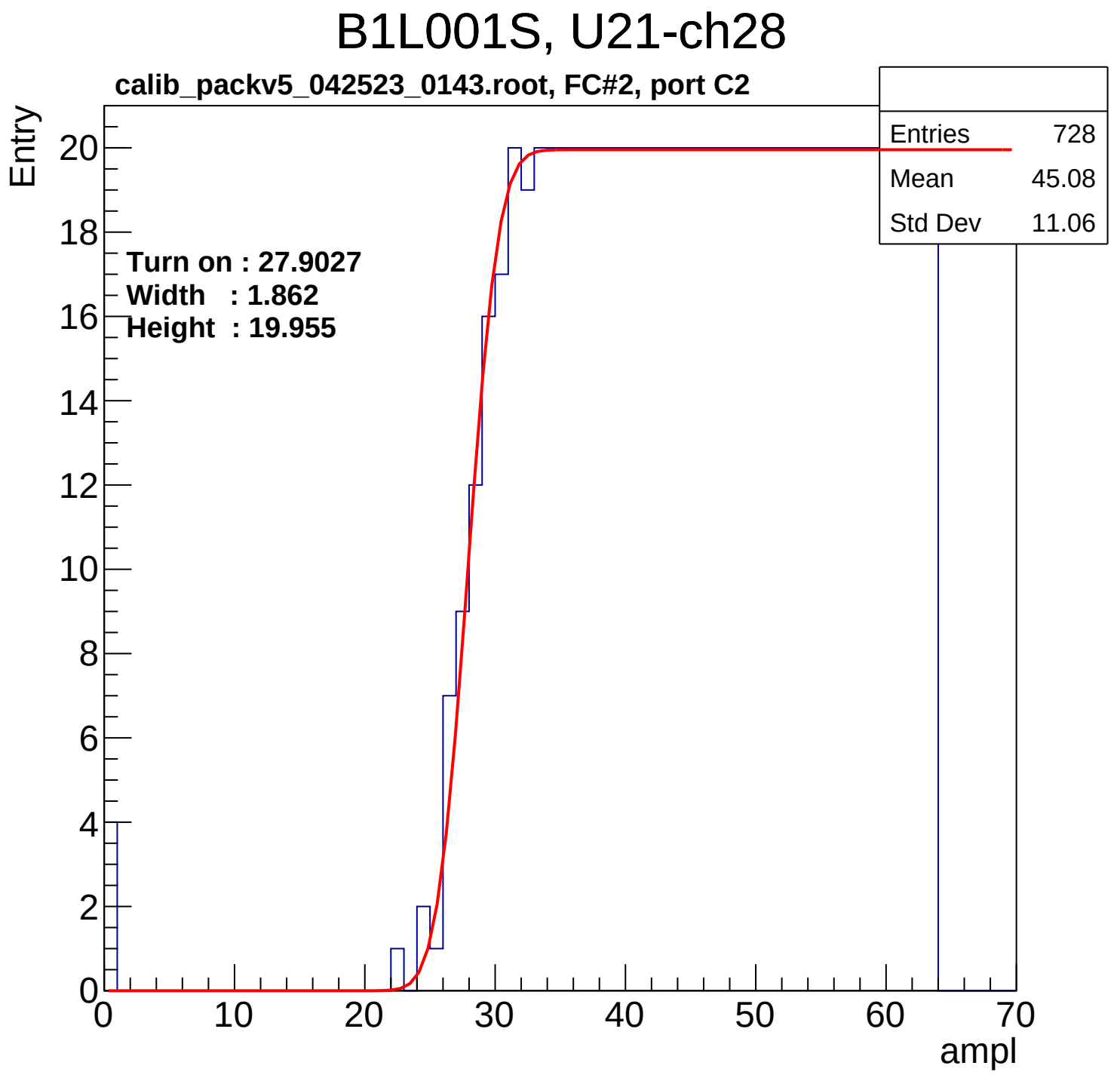
B1L001S, U21-ch28
calib_packv5_042523_0143.root, FC#2, port C2
Entries 728
Mean 45.08
Std Dev 11.06
Turn on : 27.9027
Width : 1.862
Height : 19.955
Entry
ampl
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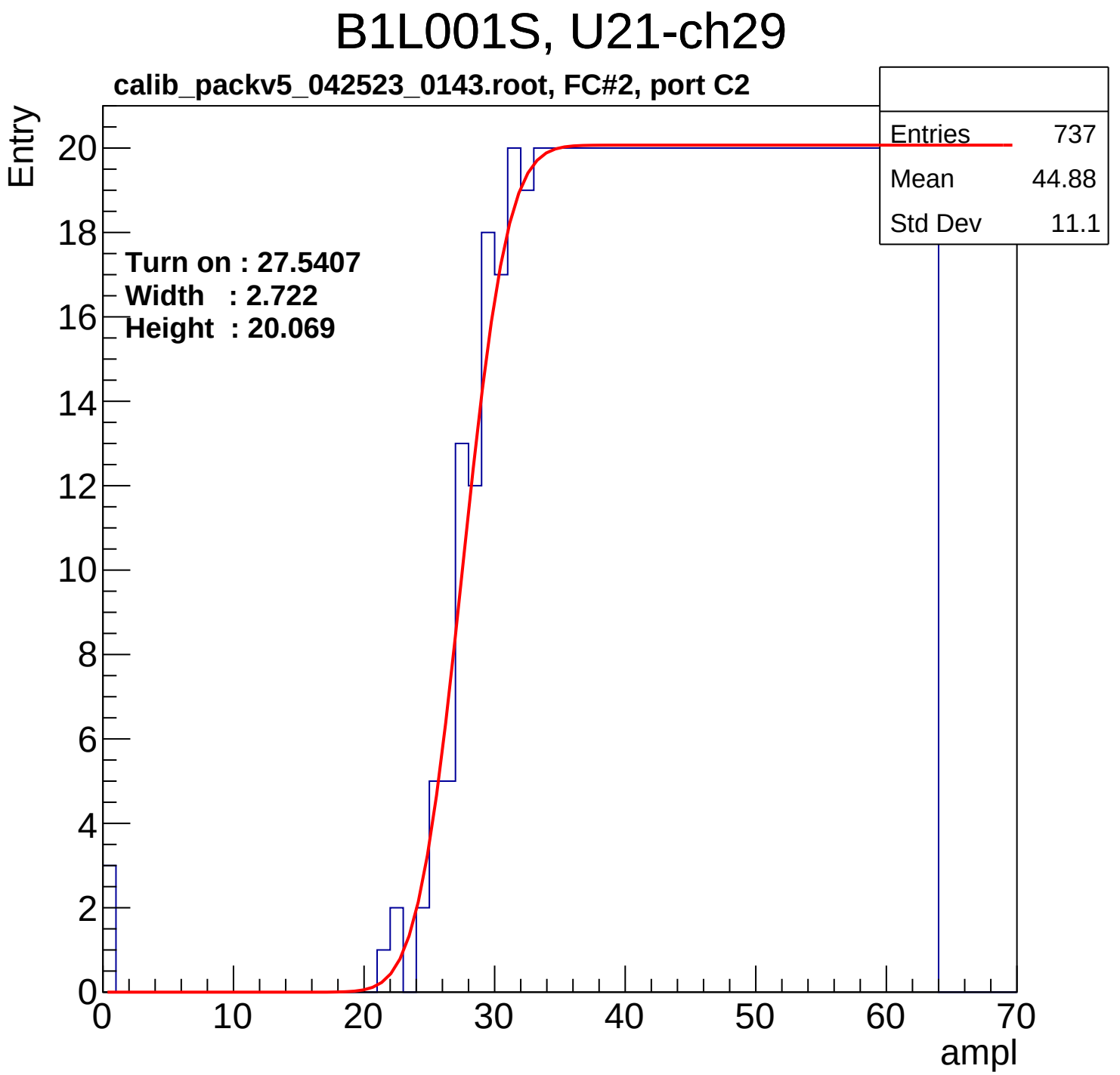
B1L001S, U21-ch29
calib_packv5_042523_0143.root, FC#2, port C2
Entries 737
Mean 44.88
Std Dev 11.1
Turn on : 27.5407
Width : 2.722
Height : 20.069
Entry
ampl
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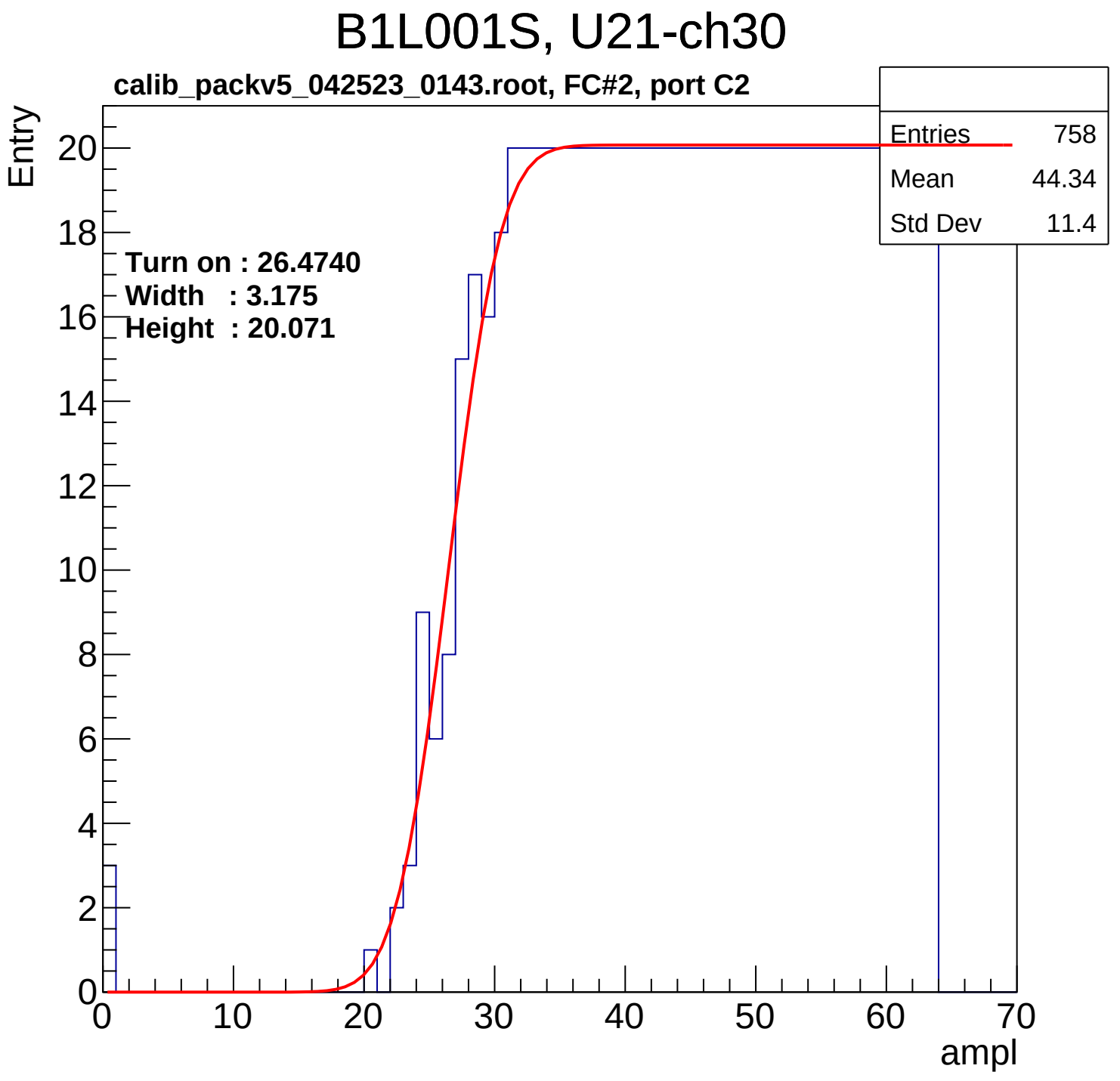
B1L001S, U21-ch30
calib_packv5_042523_0143.root, FC#2, port C2
Entries 758
Mean 44.34
Std Dev 11.4
Turn on : 26.4740
Width : 3.175
Height : 20.071
Entry
ampl
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6
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14
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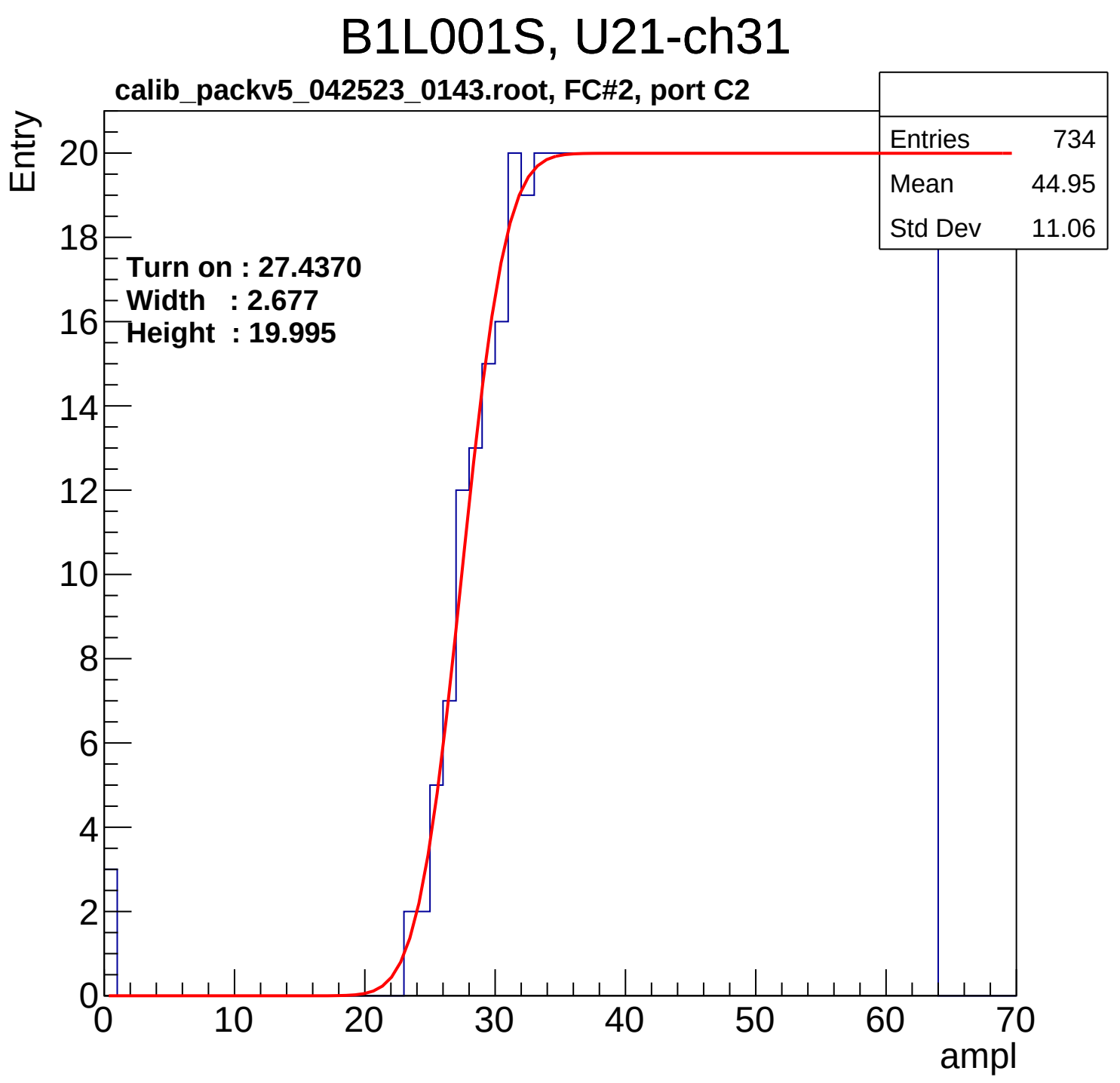
B1L001S, U21-ch31
calib_packv5_042523_0143.root, FC#2, port C2
Entries 734
Mean 44.95
Std Dev 11.06
Turn on : 27.4370
Width : 2.677
Height : 19.995
Entry
ampl
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6
8
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14
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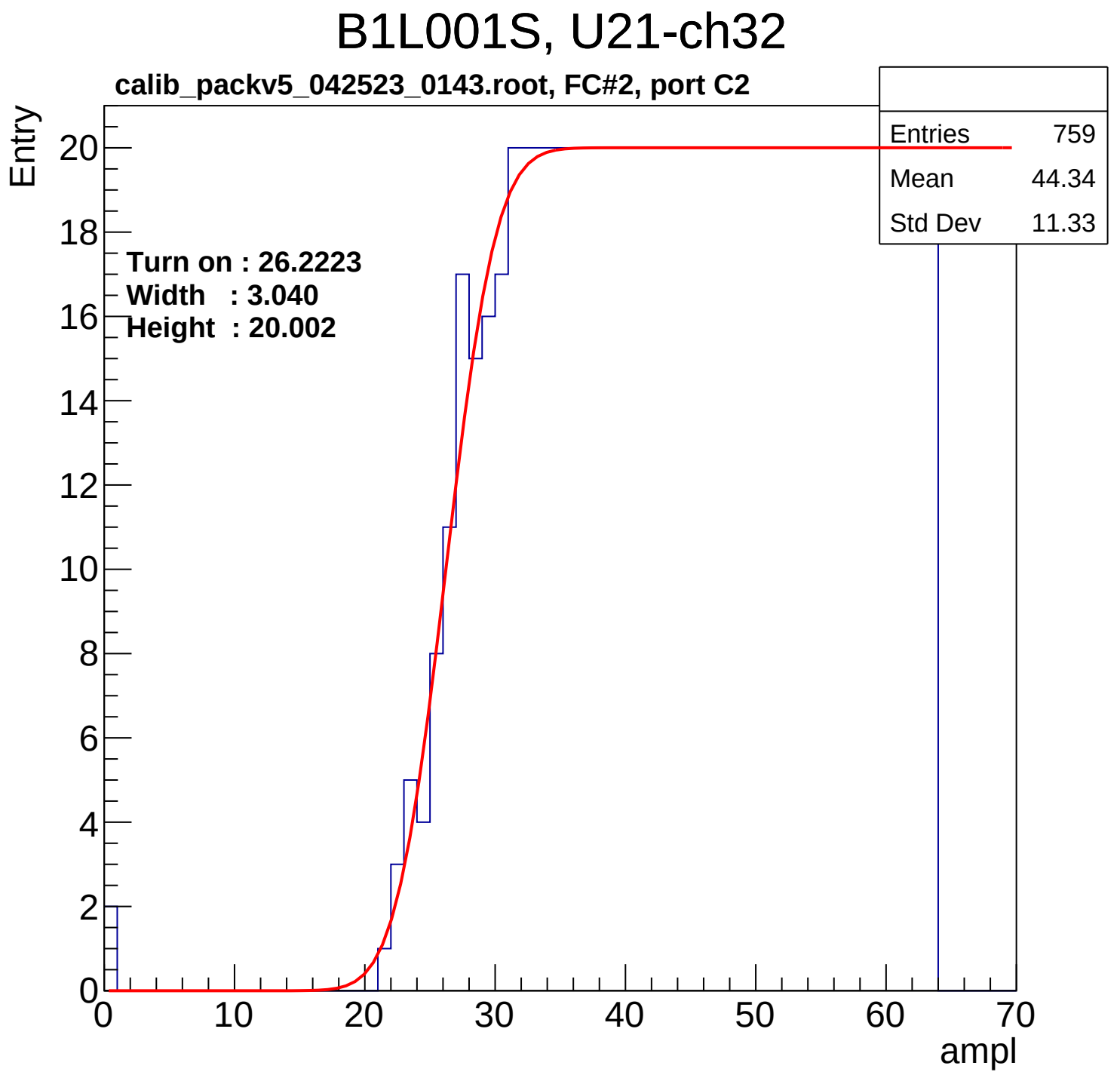
B1L001S, U21-ch32
calib_packv5_042523_0143.root, FC#2, port C2
Entries 759
Mean 44.34
Std Dev 11.33
Turn on : 26.2223
Width : 3.040
Height : 20.002
Entry
ampl
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6
8
10
12
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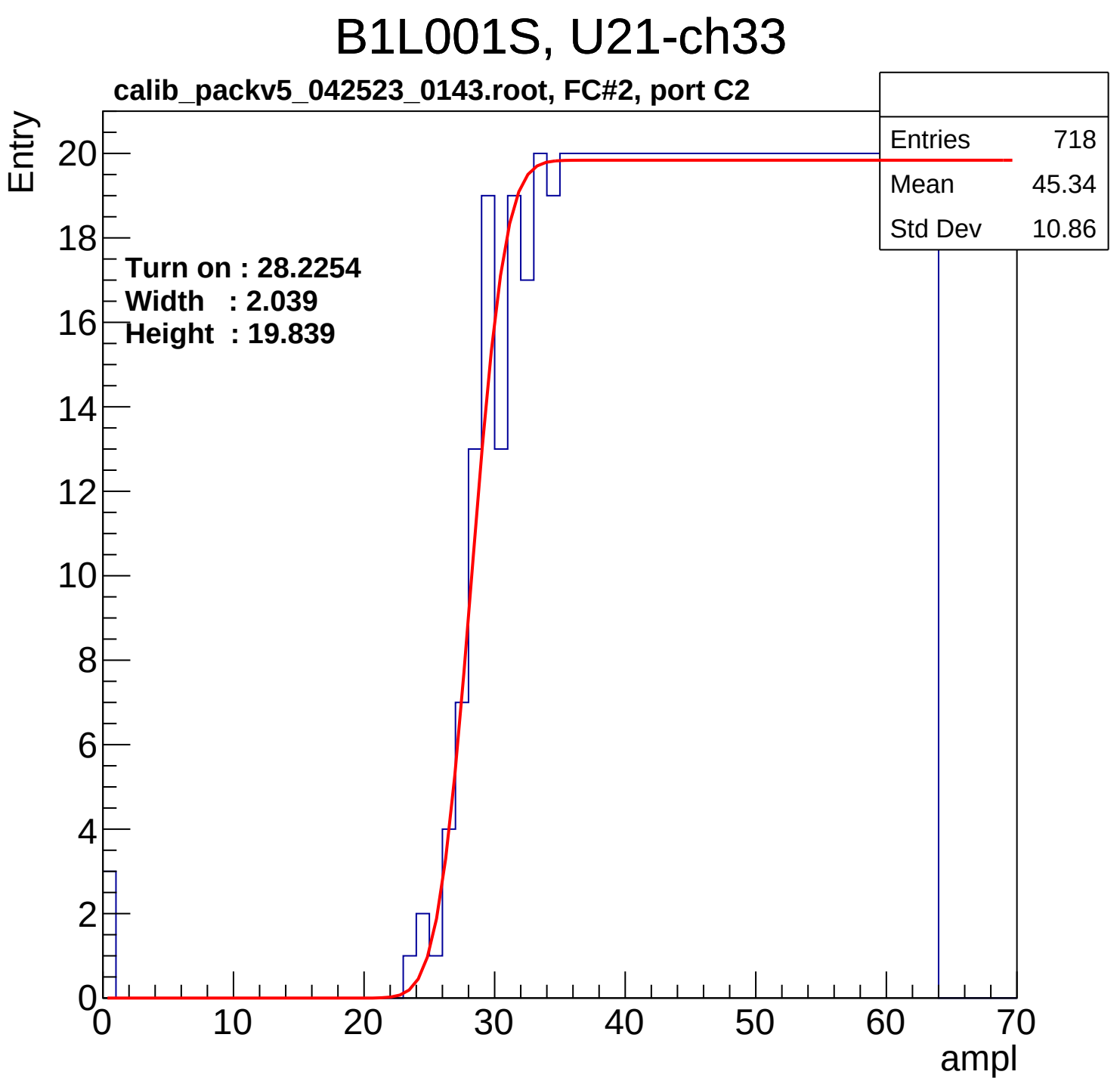
B1L001S, U21-ch33
calib_packv5_042523_0143.root, FC#2, port C2
Entries 718
Mean 45.34
Std Dev 10.86
Turn on : 28.2254
Width : 2.039
Height : 19.839
Entry
ampl
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6
8
10
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14
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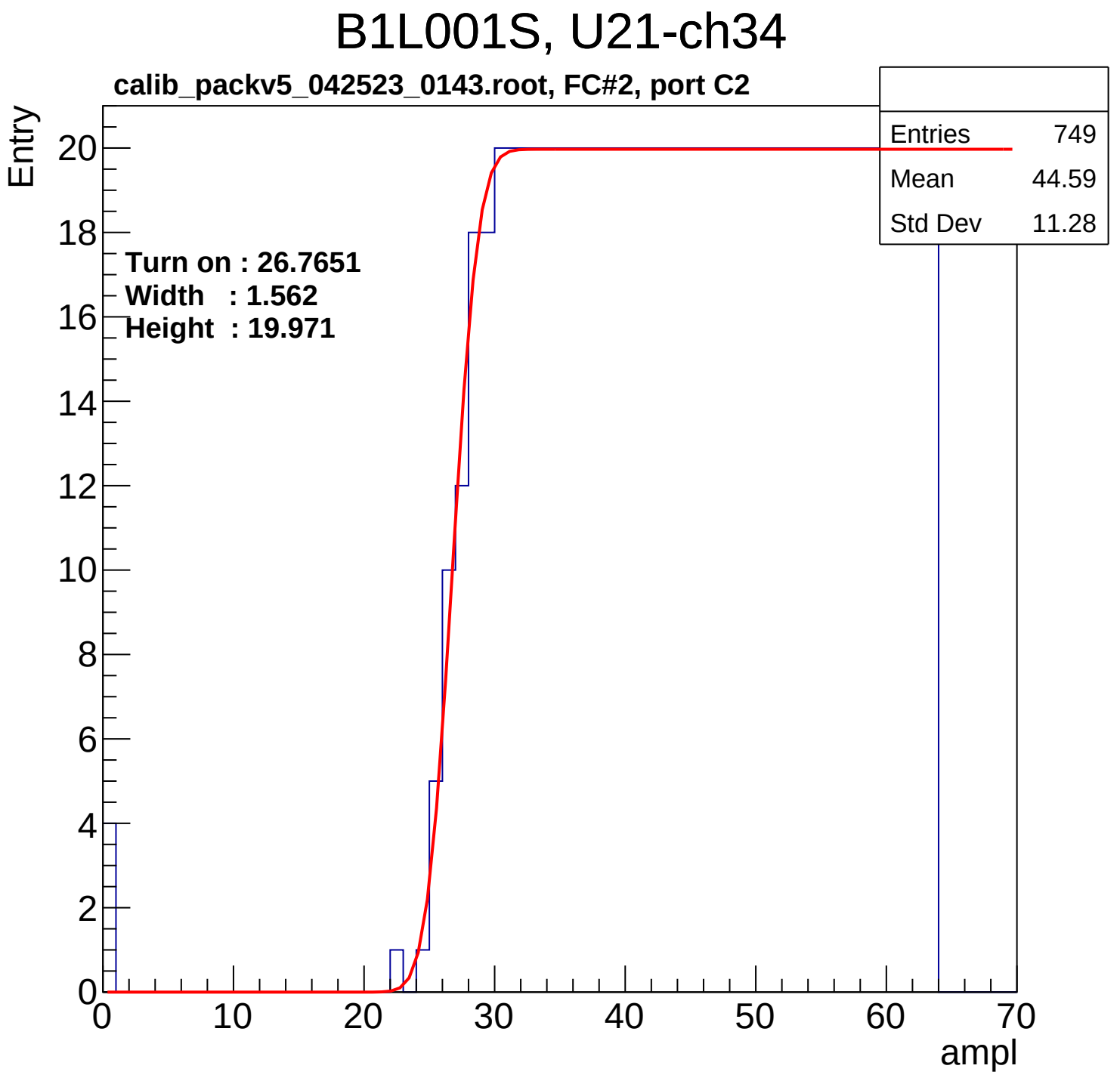
B1L001S, U21-ch34
calib_packv5_042523_0143.root, FC#2, port C2
Entries 749
Mean 44.59
Std Dev 11.28
Turn on : 26.7651
Width : 1.562
Height : 19.971
Entry
ampl
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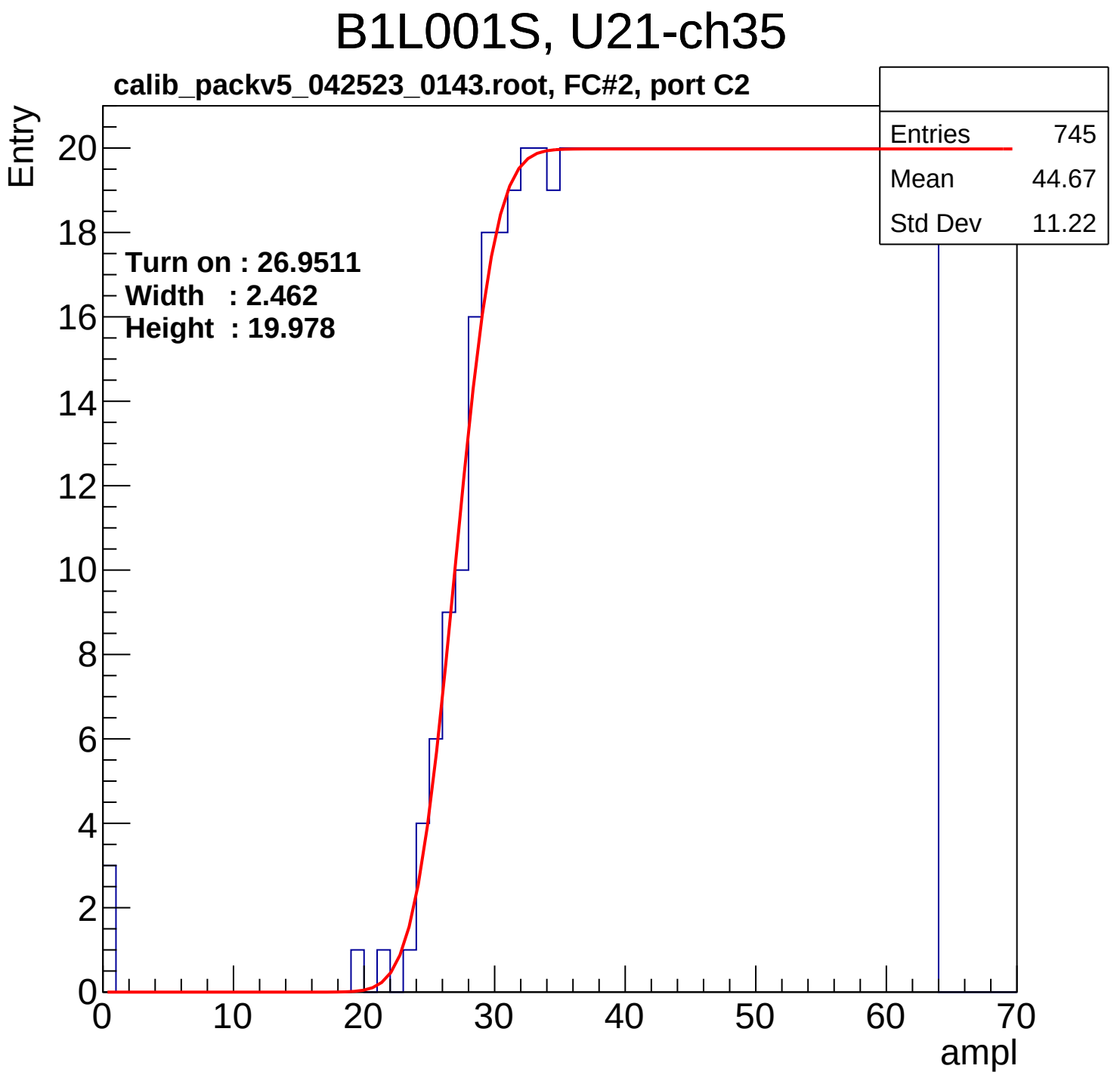
B1L001S, U21-ch35
calib_packv5_042523_0143.root, FC#2, port C2
Entries 745
Mean 44.67
Std Dev 11.22
Turn on : 26.9511
Width : 2.462
Height : 19.978
Entry
ampl
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6
8
10
12
14
16
18
20
0
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20
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60
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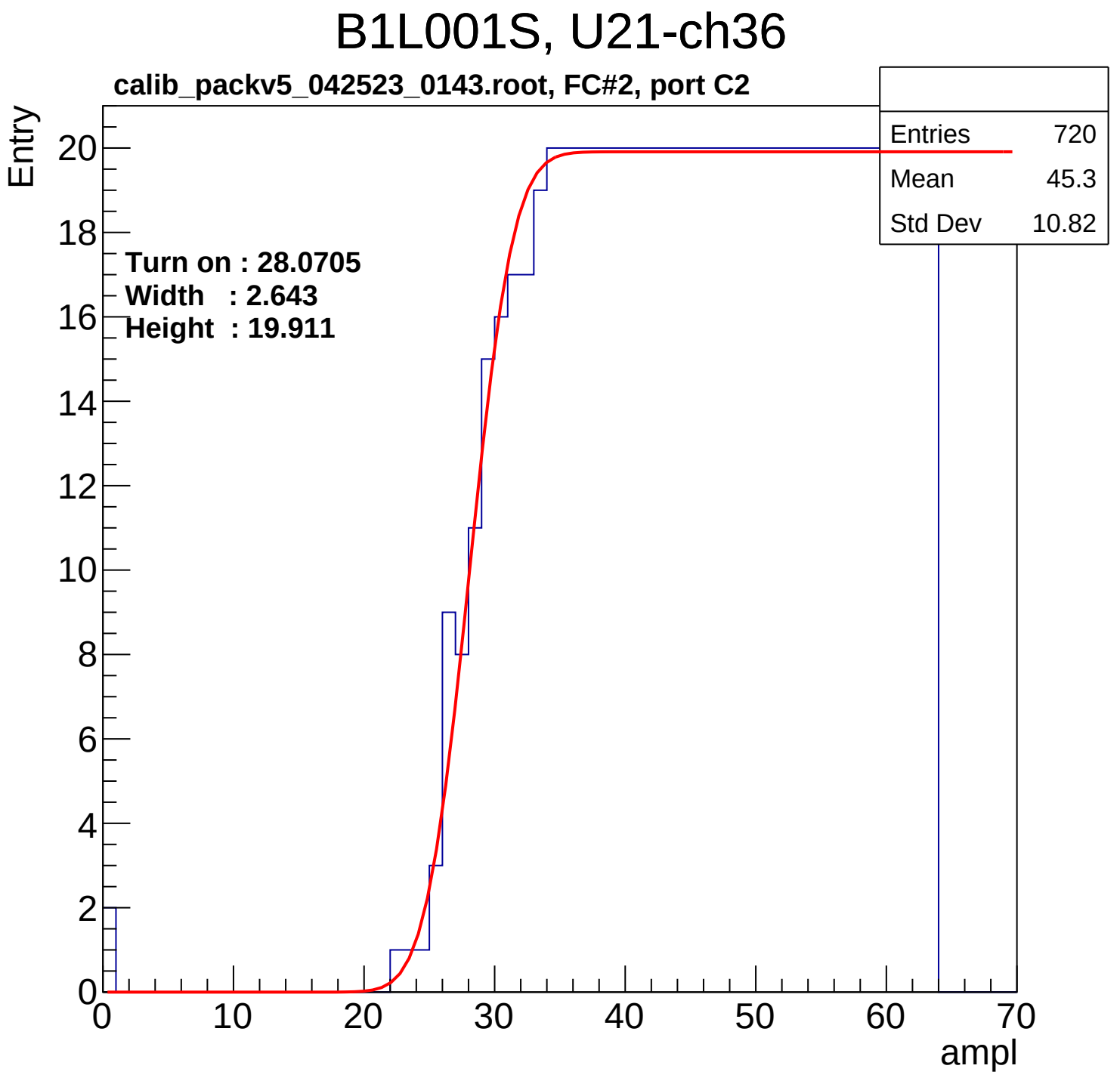
B1L001S, U21-ch36
calib_packv5_042523_0143.root, FC#2, port C2
Entries 720
Mean 45.3
Std Dev 10.82
Turn on : 28.0705
Width : 2.643
Height : 19.911
Entry
ampl
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6
8
10
12
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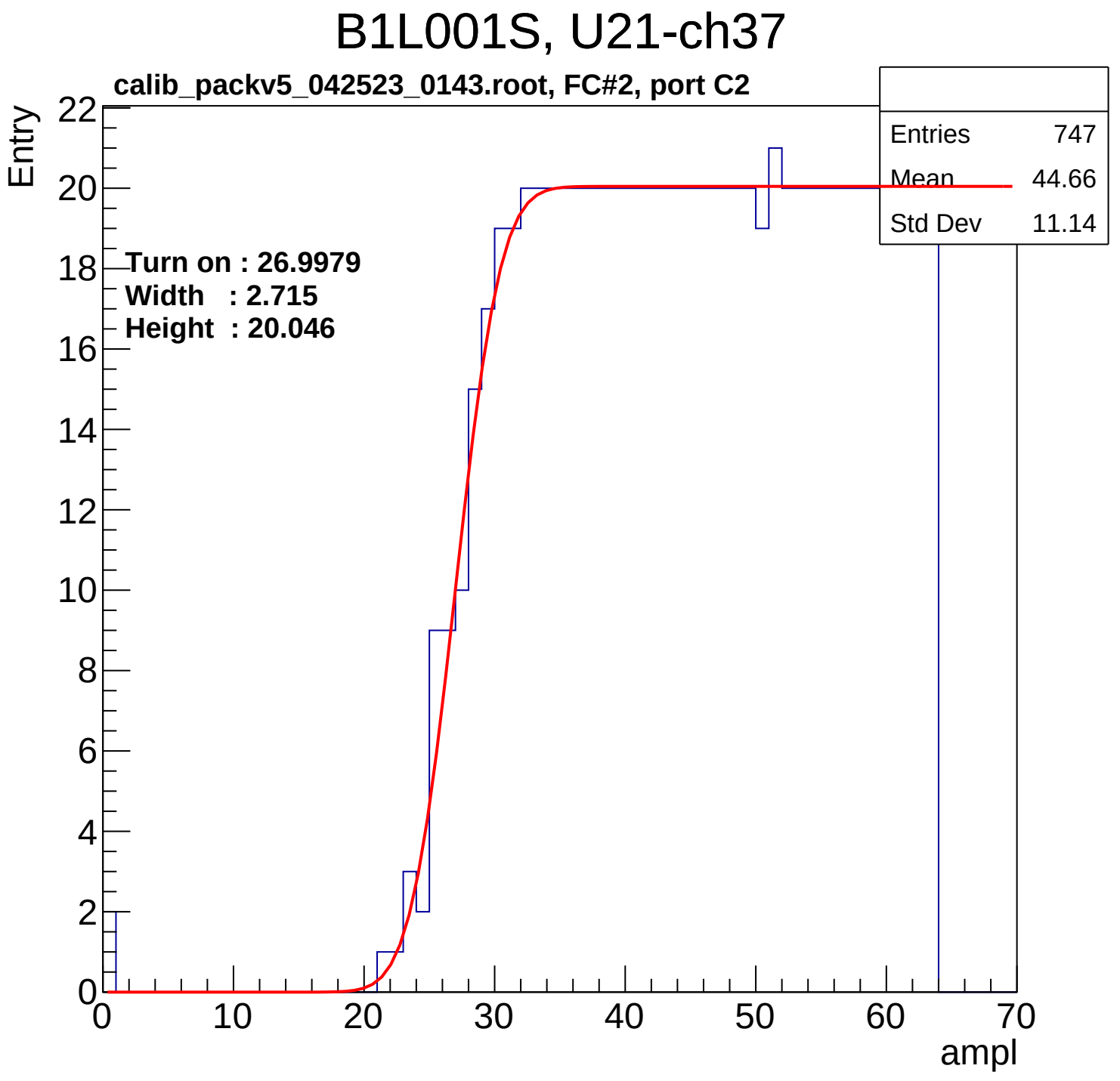
B1L001S, U21-ch37
calib_packv5_042523_0143.root, FC#2, port C2
Entries 747
Mean 44.66
Std Dev 11.14
Turn on : 26.9979
Width : 2.715
Height : 20.046
Entry
ampl
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8
10
12
14
16
18
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0
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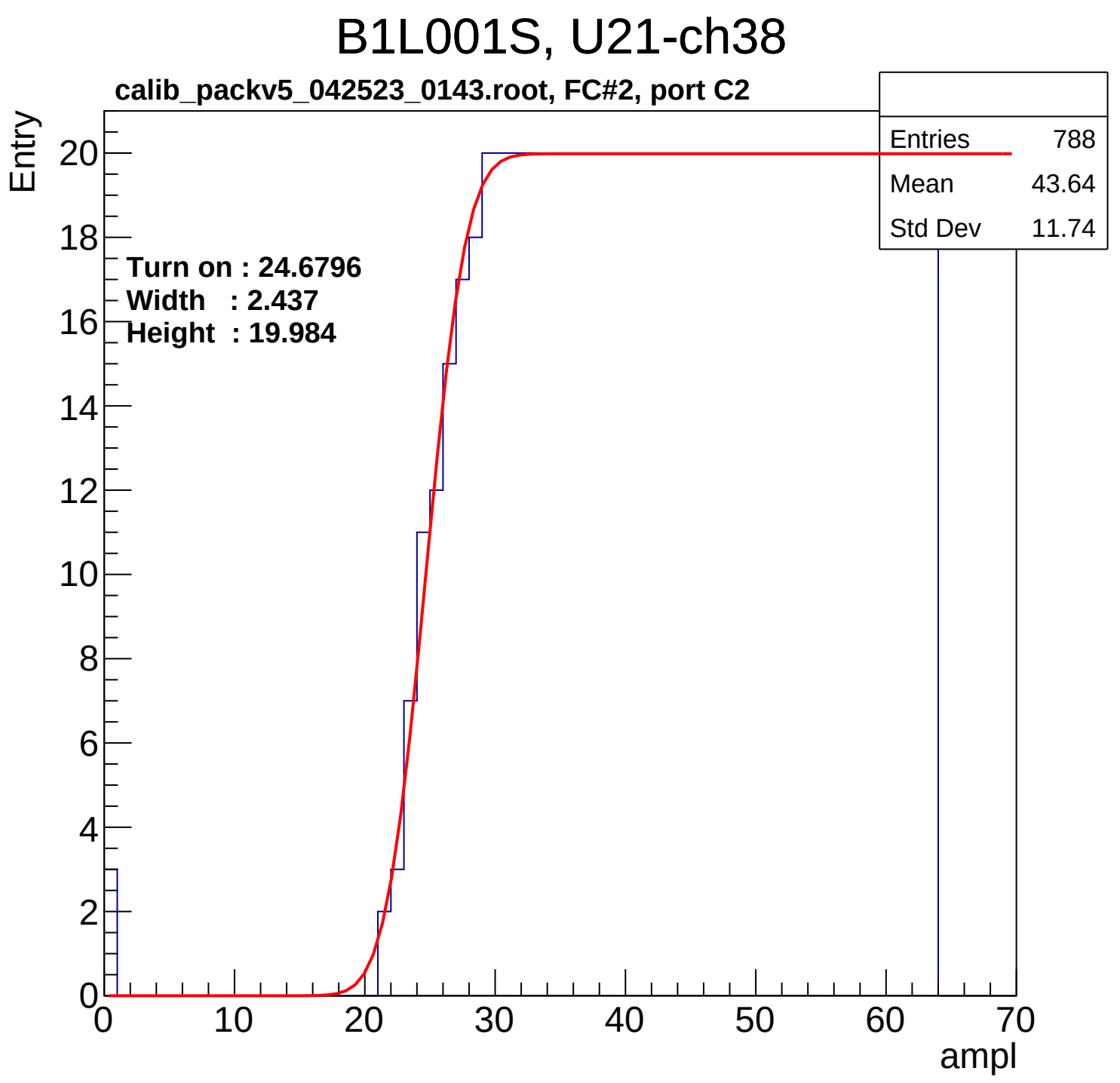
B1L001S, U21-ch38
calib_packv5_042523_0143.root, FC#2, port C2
Entries 788
Mean 43.64
Std Dev 11.74
Turn on : 24.6796
Width : 2.437
Height : 19.984
Entry
ampl
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6
8
10
12
14
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0
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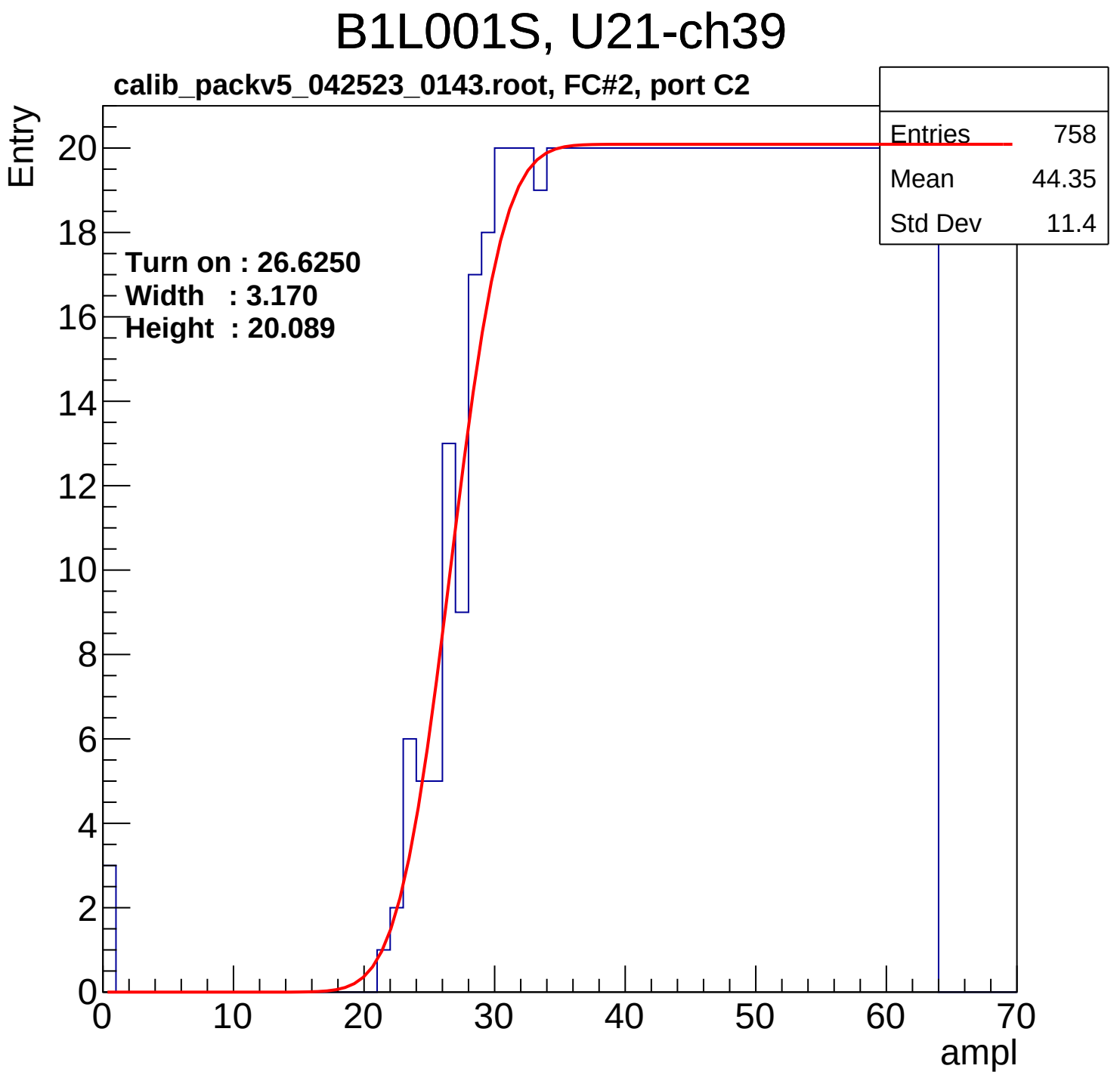
B1L001S, U21-ch39
calib_packv5_042523_0143.root, FC#2, port C2
Entries 758
Mean 44.35
Std Dev 11.4
Turn on : 26.6250
Width : 3.170
Height : 20.089
Entry
ampl
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6
8
10
12
14
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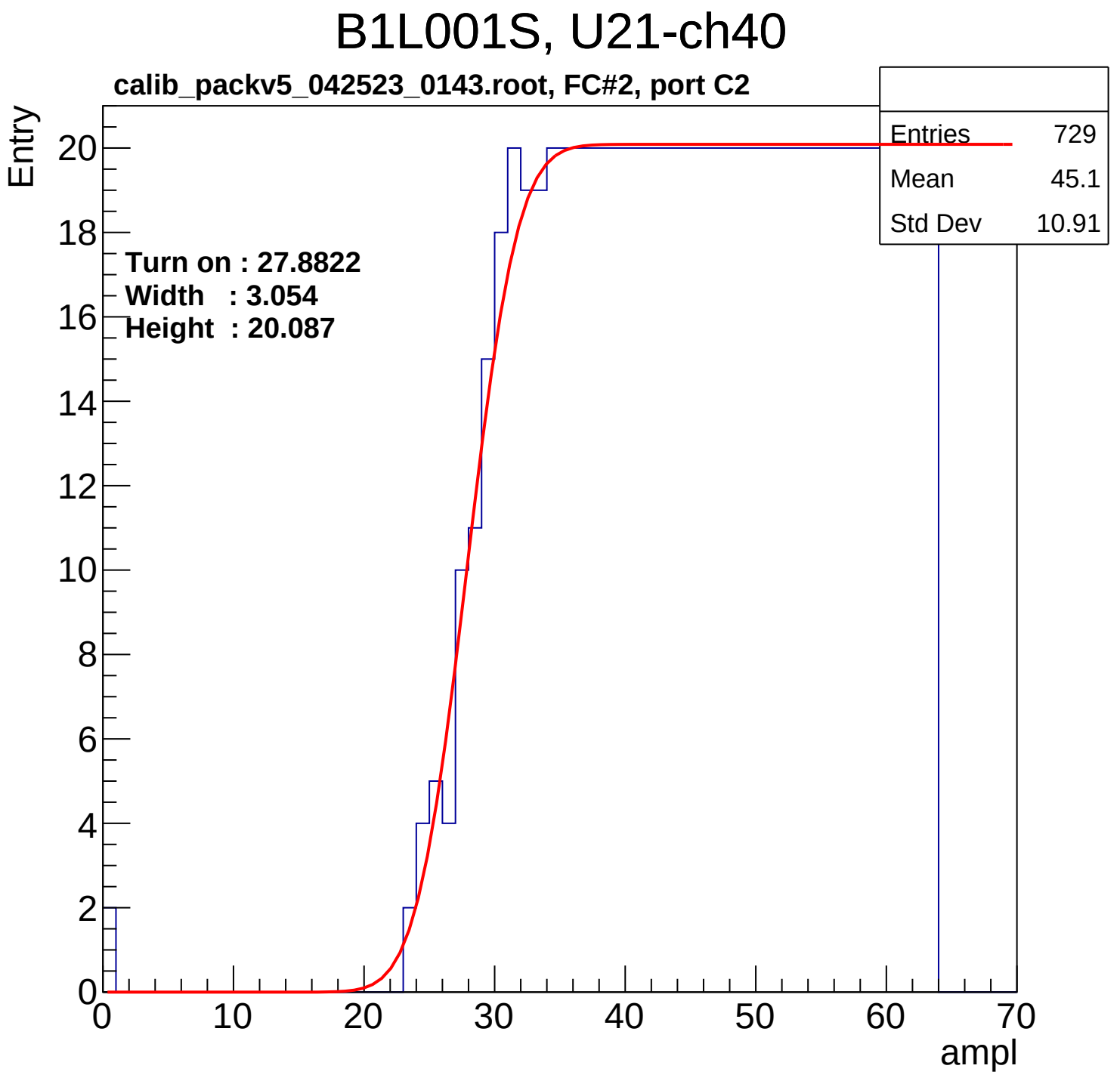
B1L001S, U21-ch40
calib_packv5_042523_0143.root, FC#2, port C2
Entries 729
Mean 45.1
Std Dev 10.91
Turn on : 27.8822
Width : 3.054
Height : 20.087
Entry
ampl
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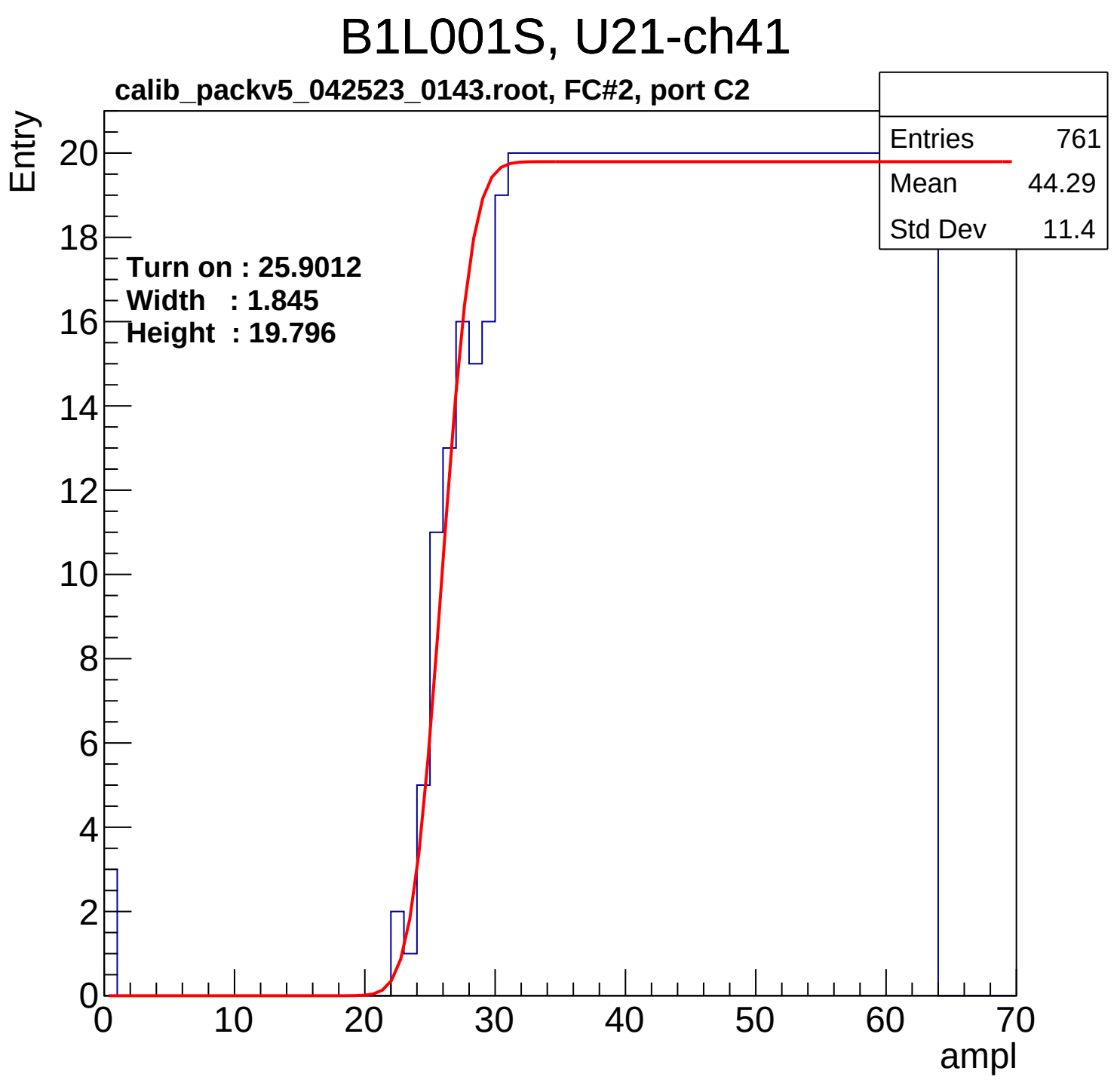
B1L001S, U21-ch41
calib_packv5_042523_0143.root, FC#2, port C2
Entries 761
Mean 44.29
Std Dev 11.4
Turn on : 25.9012
Width : 1.845
Height : 19.796
Entry
ampl
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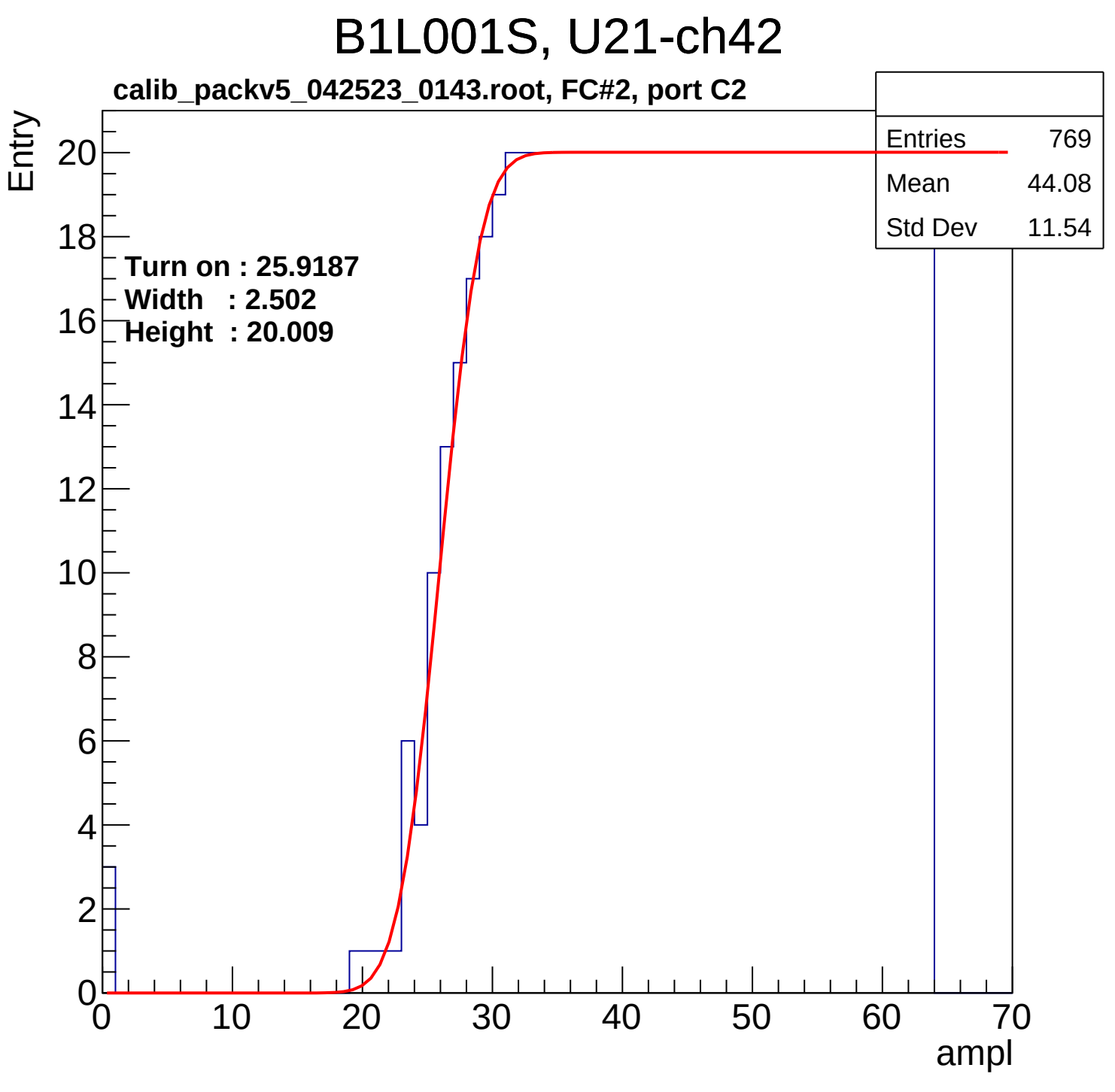
B1L001S, U21-ch42
calib_packv5_042523_0143.root, FC#2, port C2
Entries 769
Mean 44.08
Std Dev 11.54
Turn on : 25.9187
Width : 2.502
Height : 20.009
Entry
ampl
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6
8
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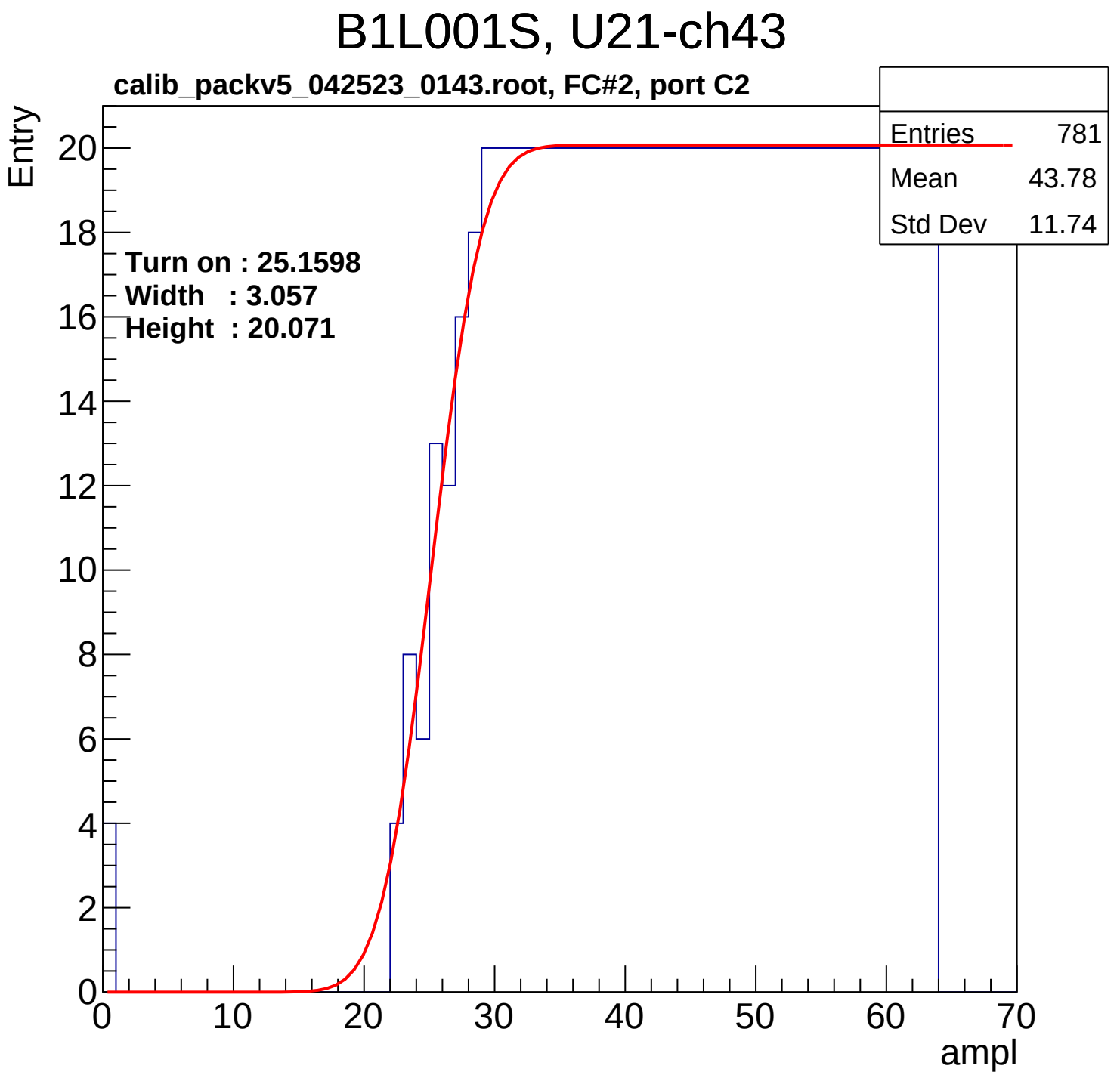
B1L001S, U21-ch43
calib_packv5_042523_0143.root, FC#2, port C2
Entries 781
Mean 43.78
Std Dev 11.74
Turn on : 25.1598
Width : 3.057
Height : 20.071
Entry
ampl
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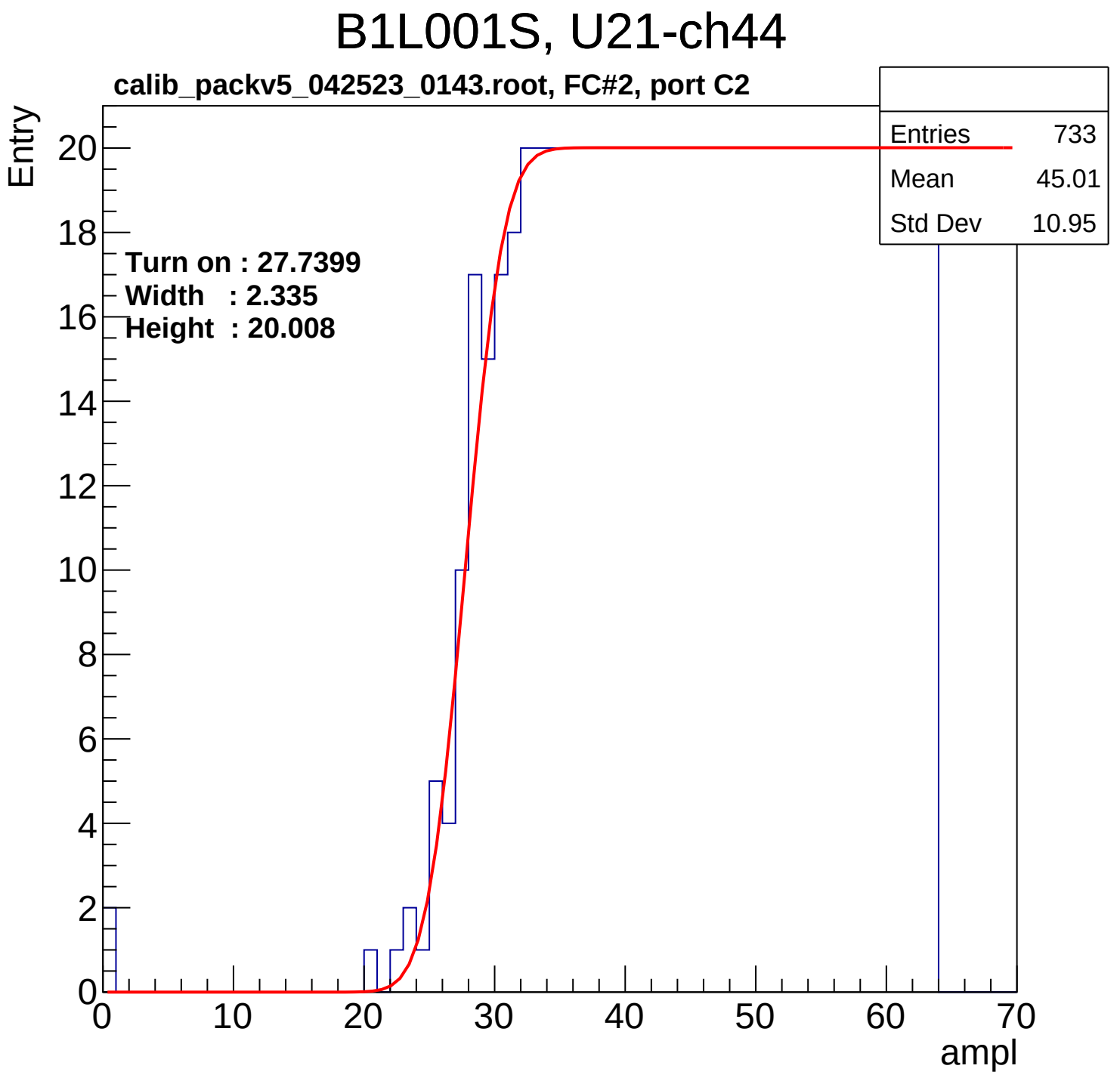
B1L001S, U21-ch44
calib_packv5_042523_0143.root, FC#2, port C2
Entries 733
Mean 45.01
Std Dev 10.95
Turn on : 27.7399
Width : 2.335
Height : 20.008
Entry
ampl
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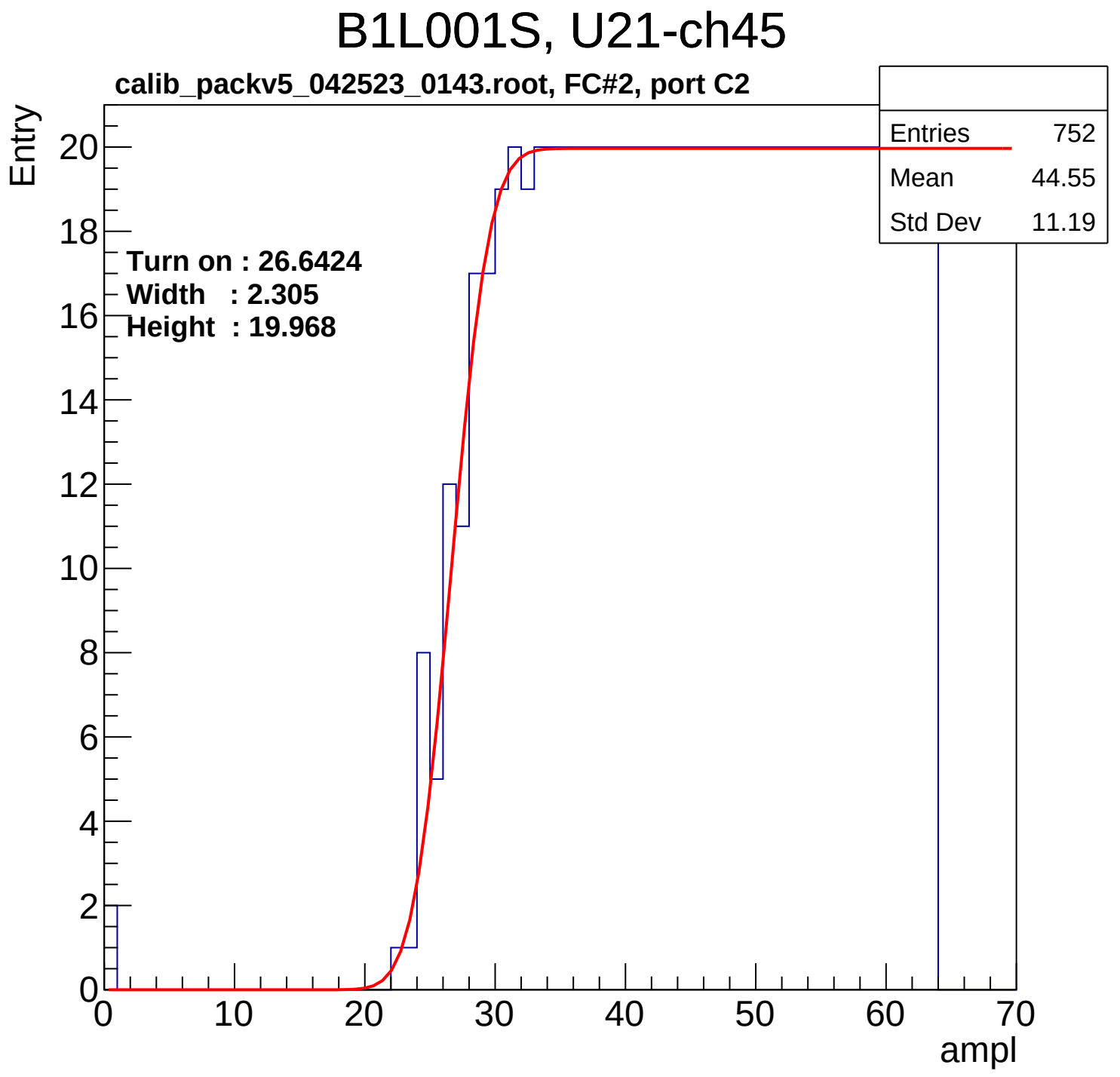
B1L001S, U21-ch45
calib_packv5_042523_0143.root, FC#2, port C2
Entries 752
Mean 44.55
Std Dev 11.19
Turn on : 26.6424
Width : 2.305
Height : 19.968
Entry
ampl
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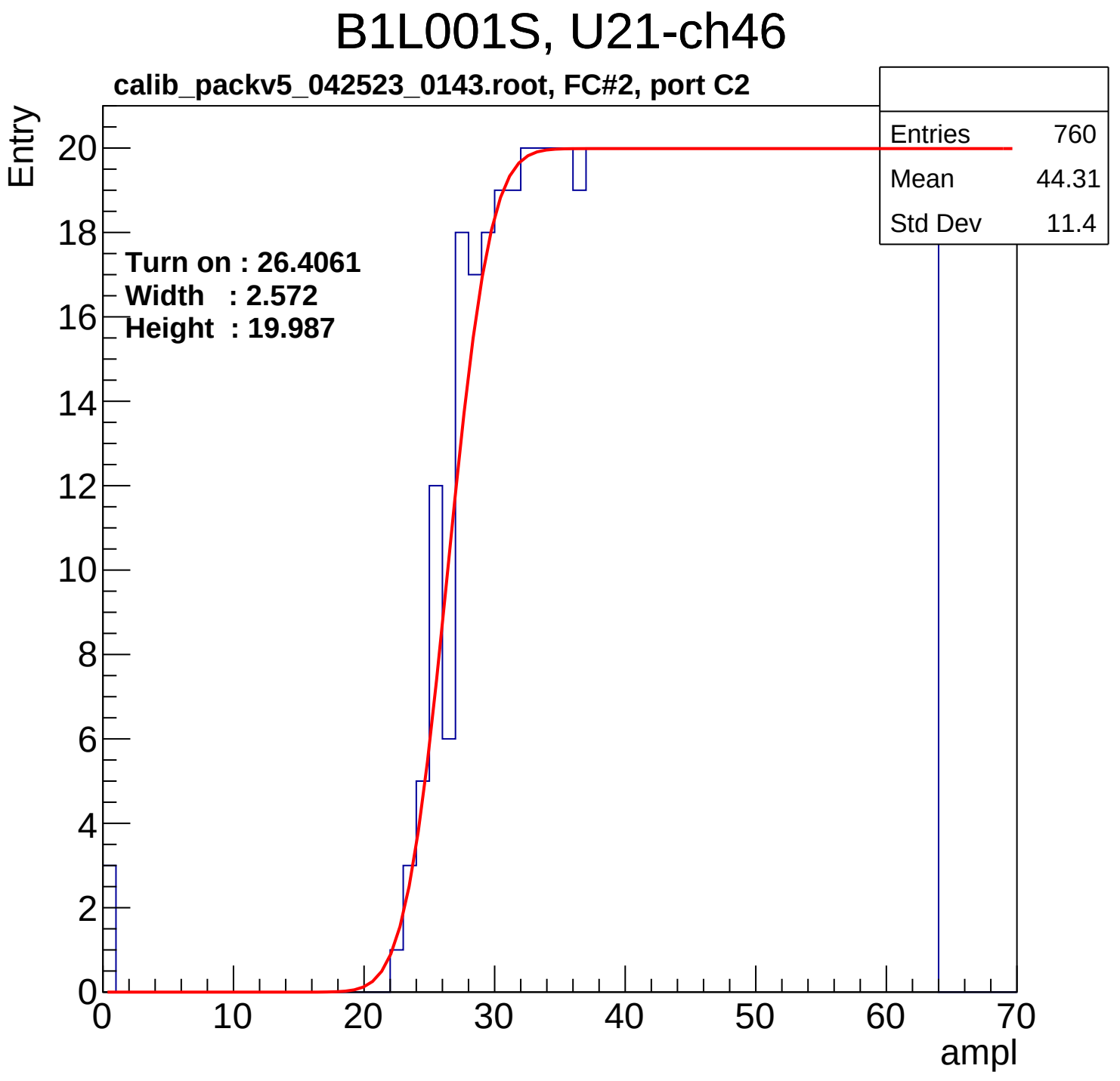
B1L001S, U21-ch46
calib_packv5_042523_0143.root, FC#2, port C2
Entries 760
Mean 44.31
Std Dev 11.4
Turn on : 26.4061
Width : 2.572
Height : 19.987
Entry
ampl
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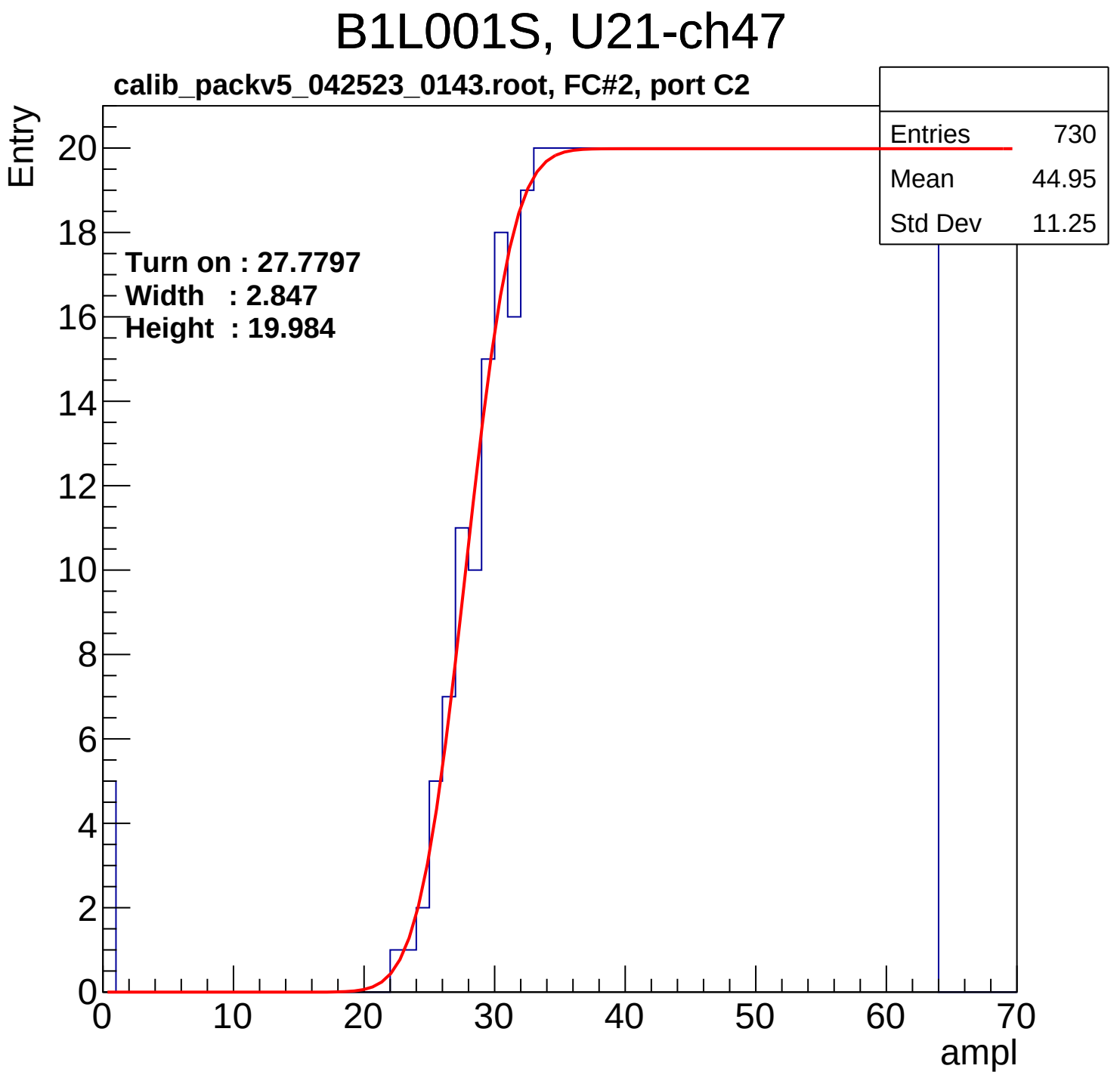
B1L001S, U21-ch47
calib_packv5_042523_0143.root, FC#2, port C2
Entries 730
Mean 44.95
Std Dev 11.25
Turn on : 27.7797
Width : 2.847
Height : 19.984
Entry
ampl
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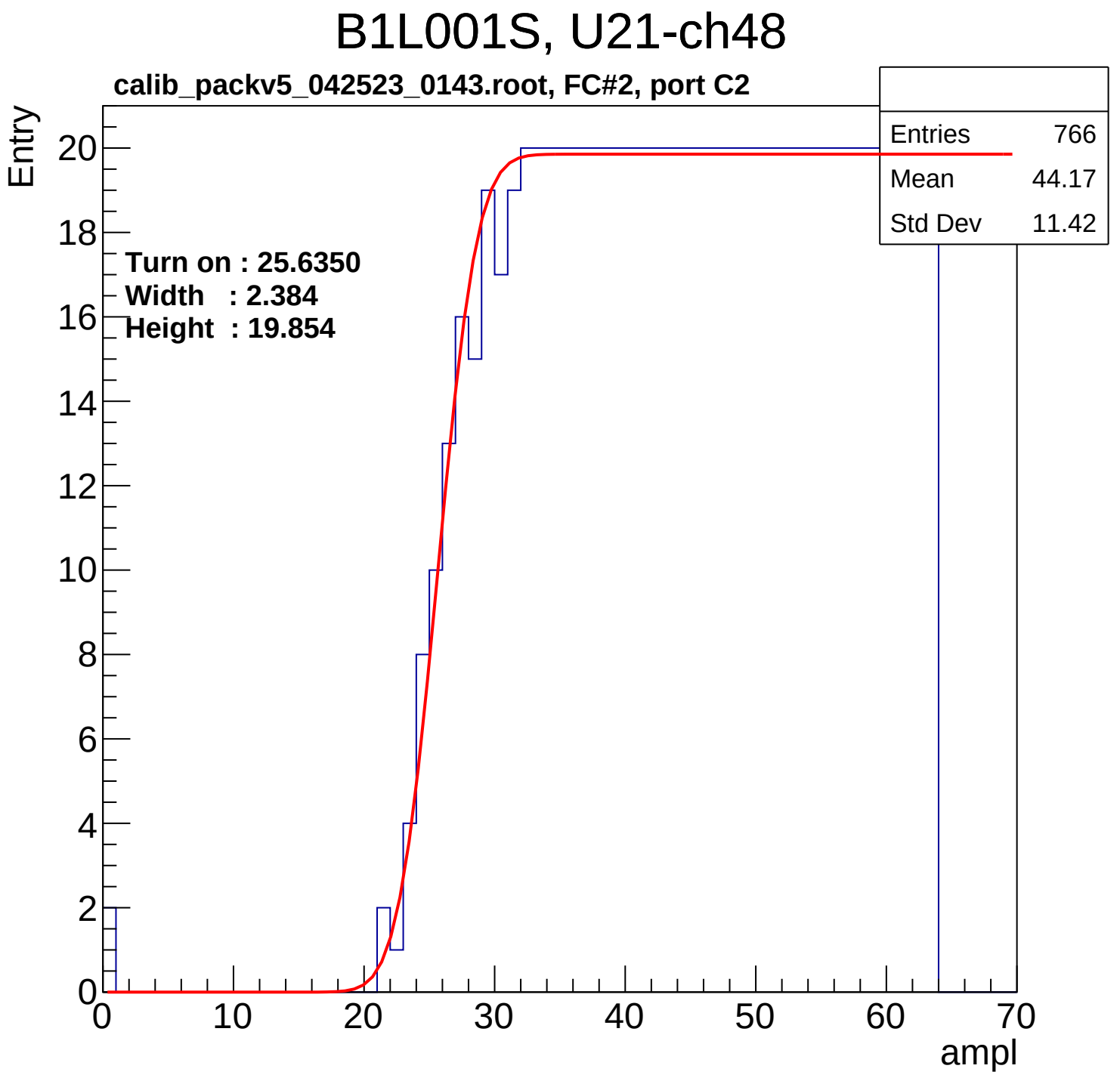
B1L001S, U21-ch48
calib_packv5_042523_0143.root, FC#2, port C2
Entries 766
Mean 44.17
Std Dev 11.42
Turn on : 25.6350
Width : 2.384
Height : 19.854
Entry
ampl
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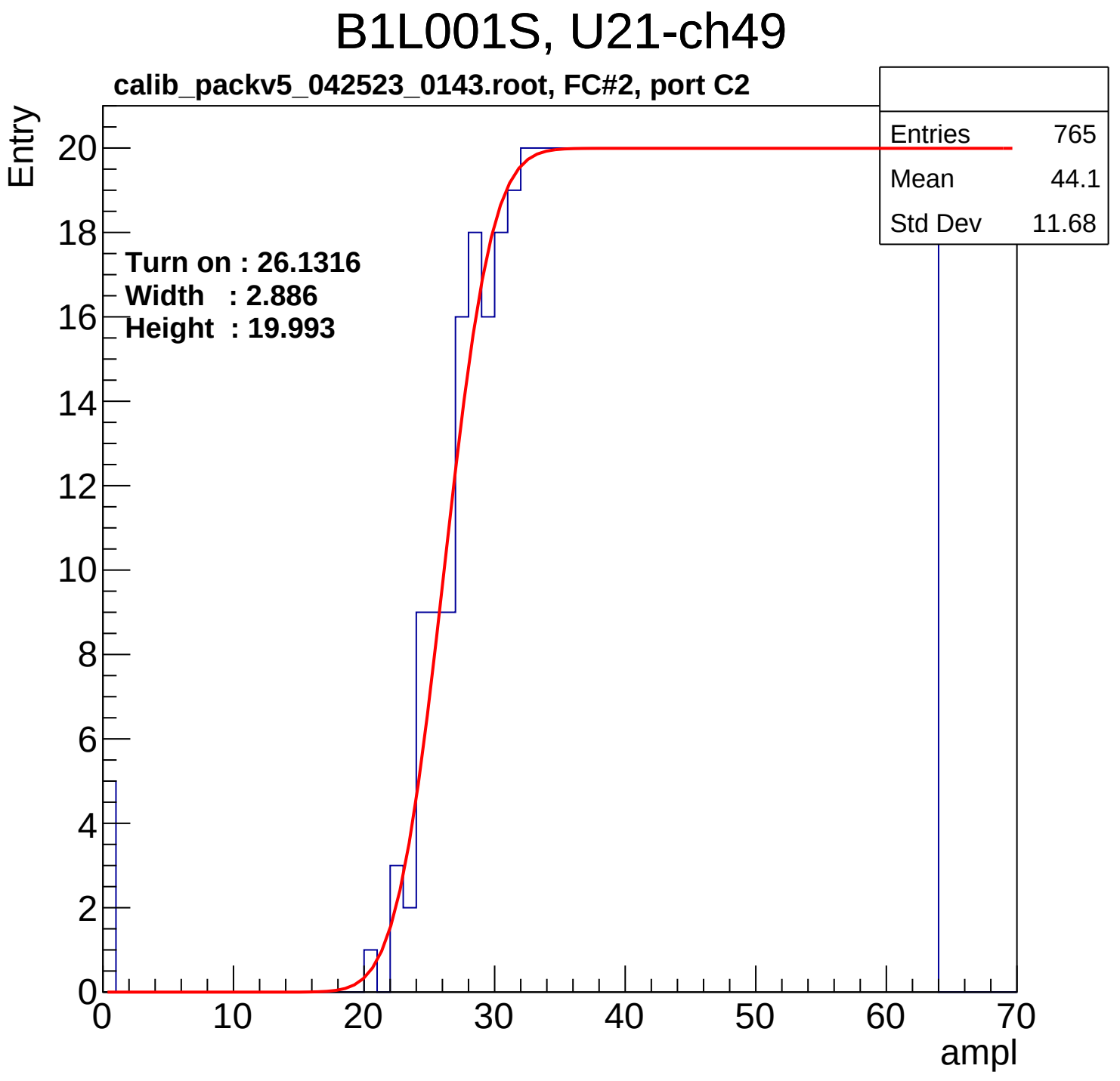
B1L001S, U21-ch49
calib_packv5_042523_0143.root, FC#2, port C2
Entries 765
Mean 44.1
Std Dev 11.68
Turn on : 26.1316
Width : 2.886
Height : 19.993
Entry
ampl
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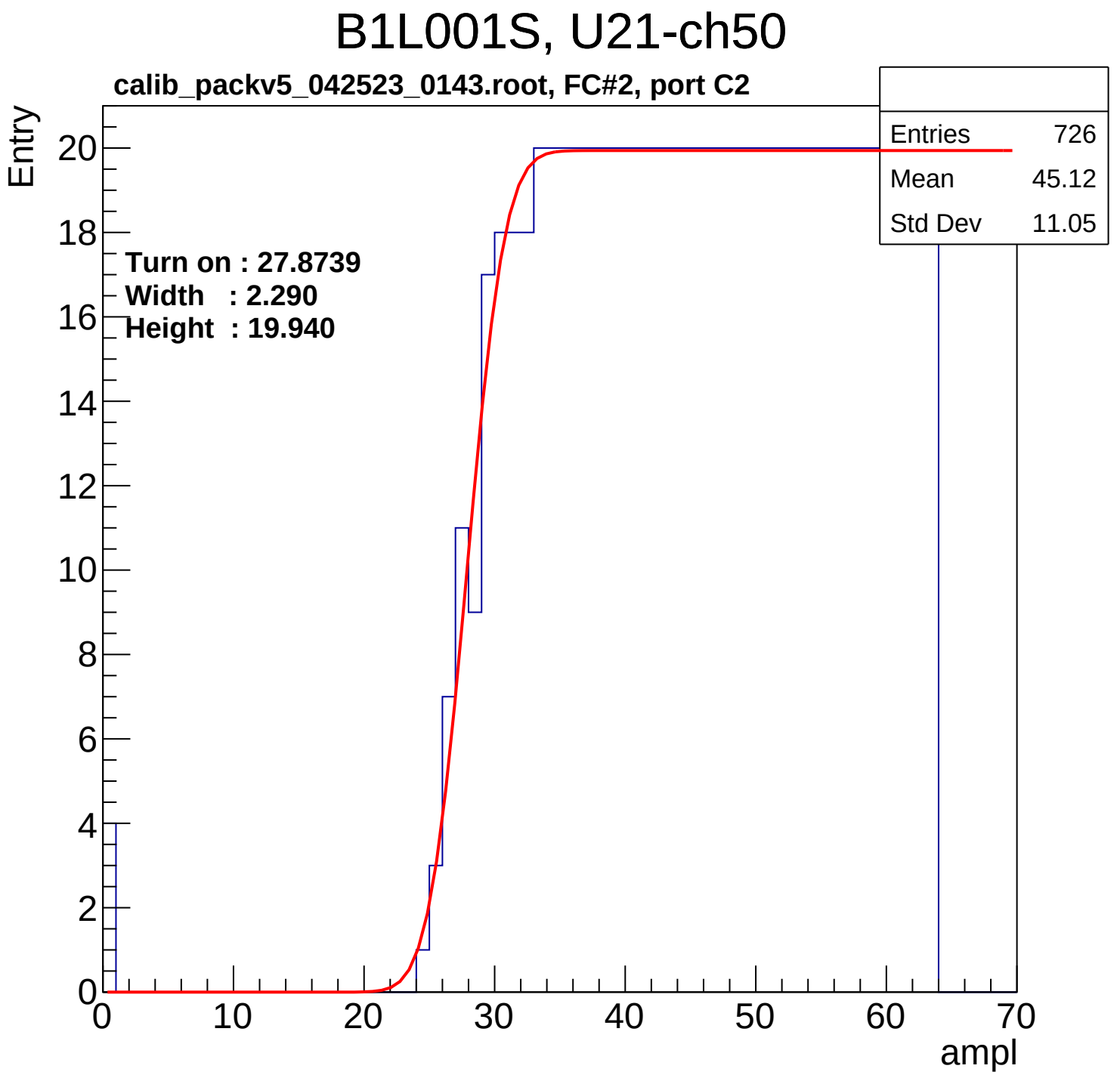
B1L001S, U21-ch50
calib_packv5_042523_0143.root, FC#2, port C2
Entries 726
Mean 45.12
Std Dev 11.05
Turn on : 27.8739
Width : 2.290
Height : 19.940
Entry
ampl
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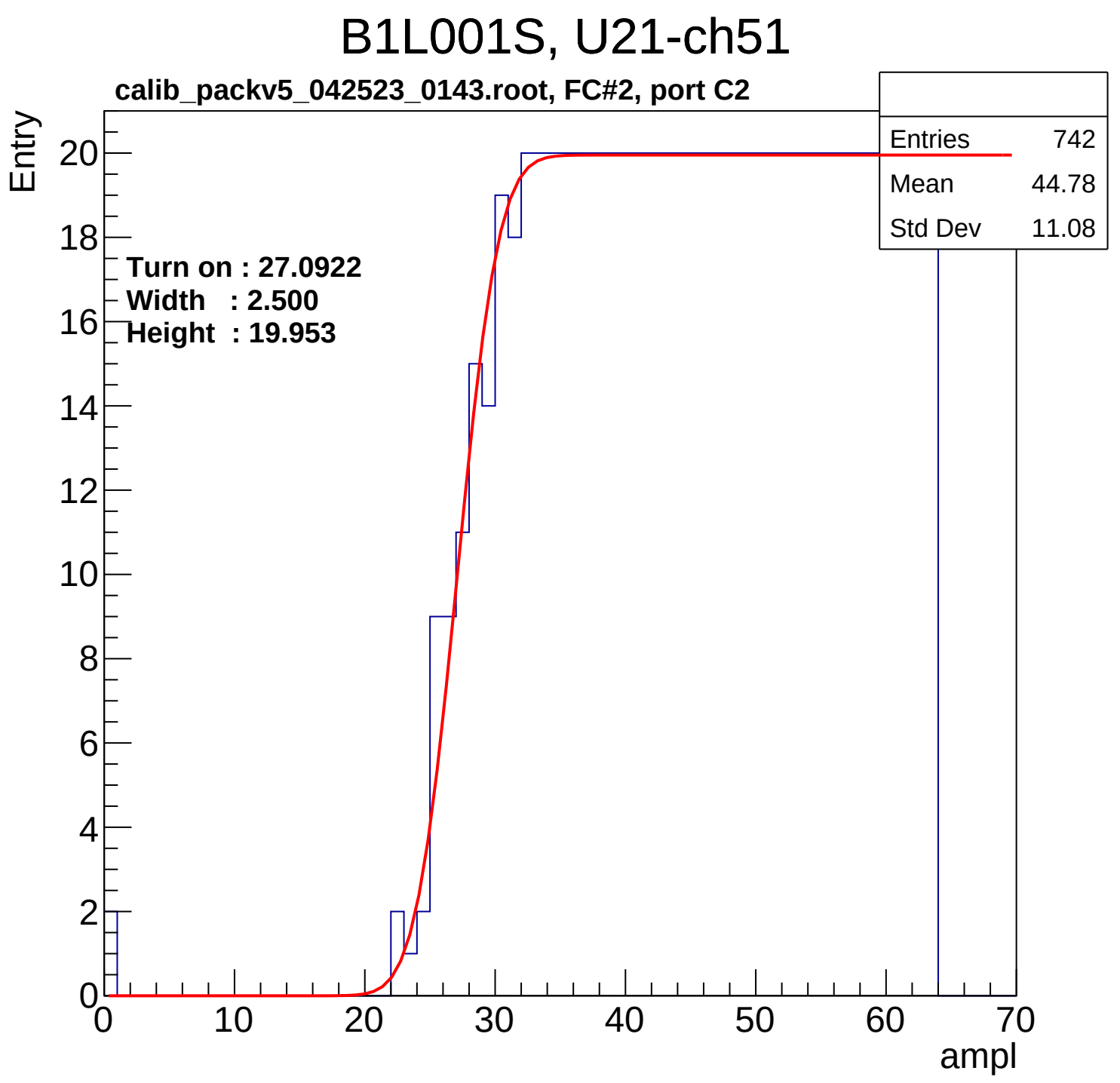
B1L001S, U21-ch51
calib_packv5_042523_0143.root, FC#2, port C2
Entries 742
Mean 44.78
Std Dev 11.08
Turn on : 27.0922
Width : 2.500
Height : 19.953
Entry
ampl
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8
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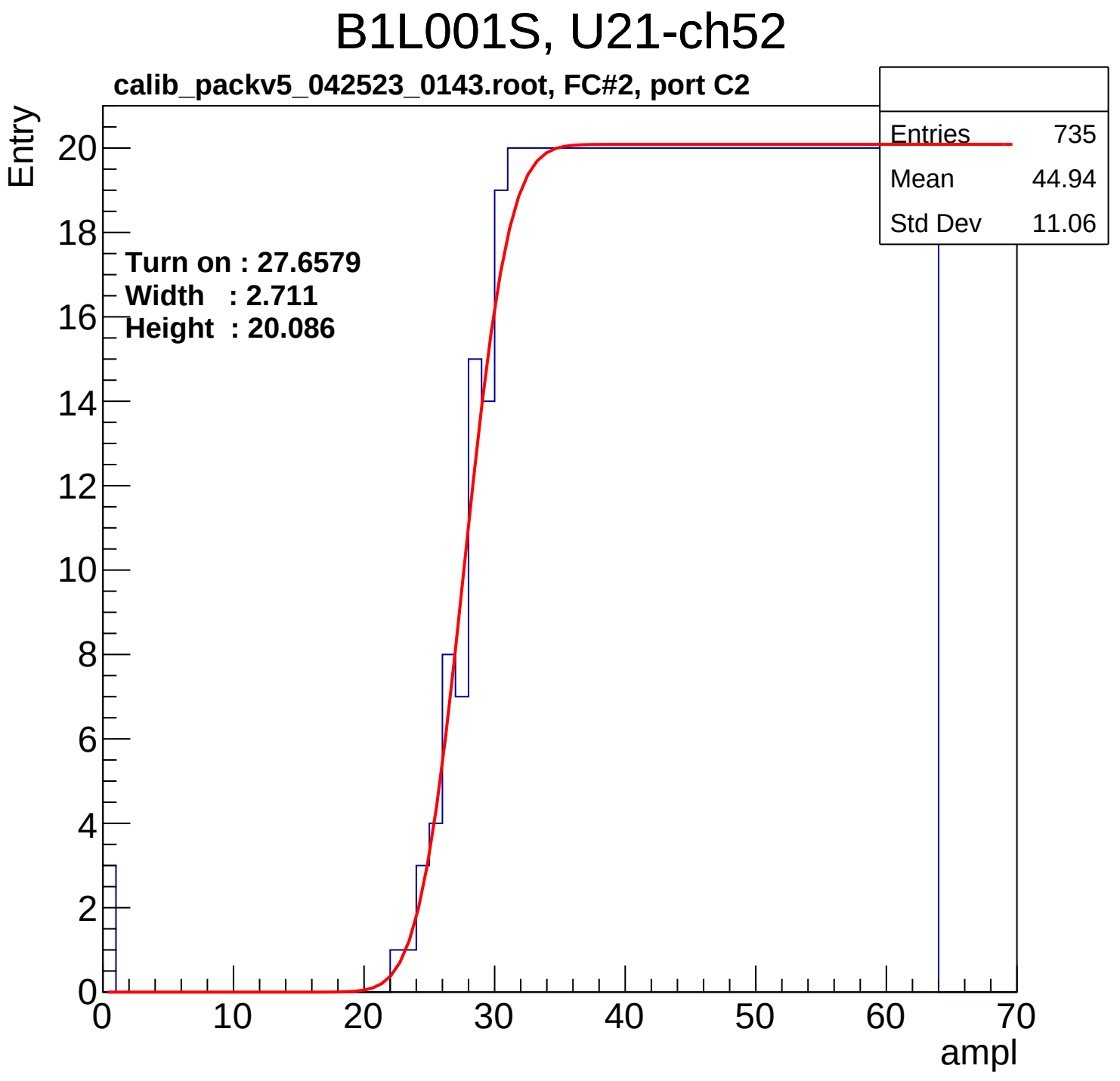
B1L001S, U21-ch52
calib_packv5_042523_0143.root, FC#2, port C2
Entries 735
Mean 44.94
Std Dev 11.06
Turn on : 27.6579
Width : 2.711
Height : 20.086
Entry
ampl
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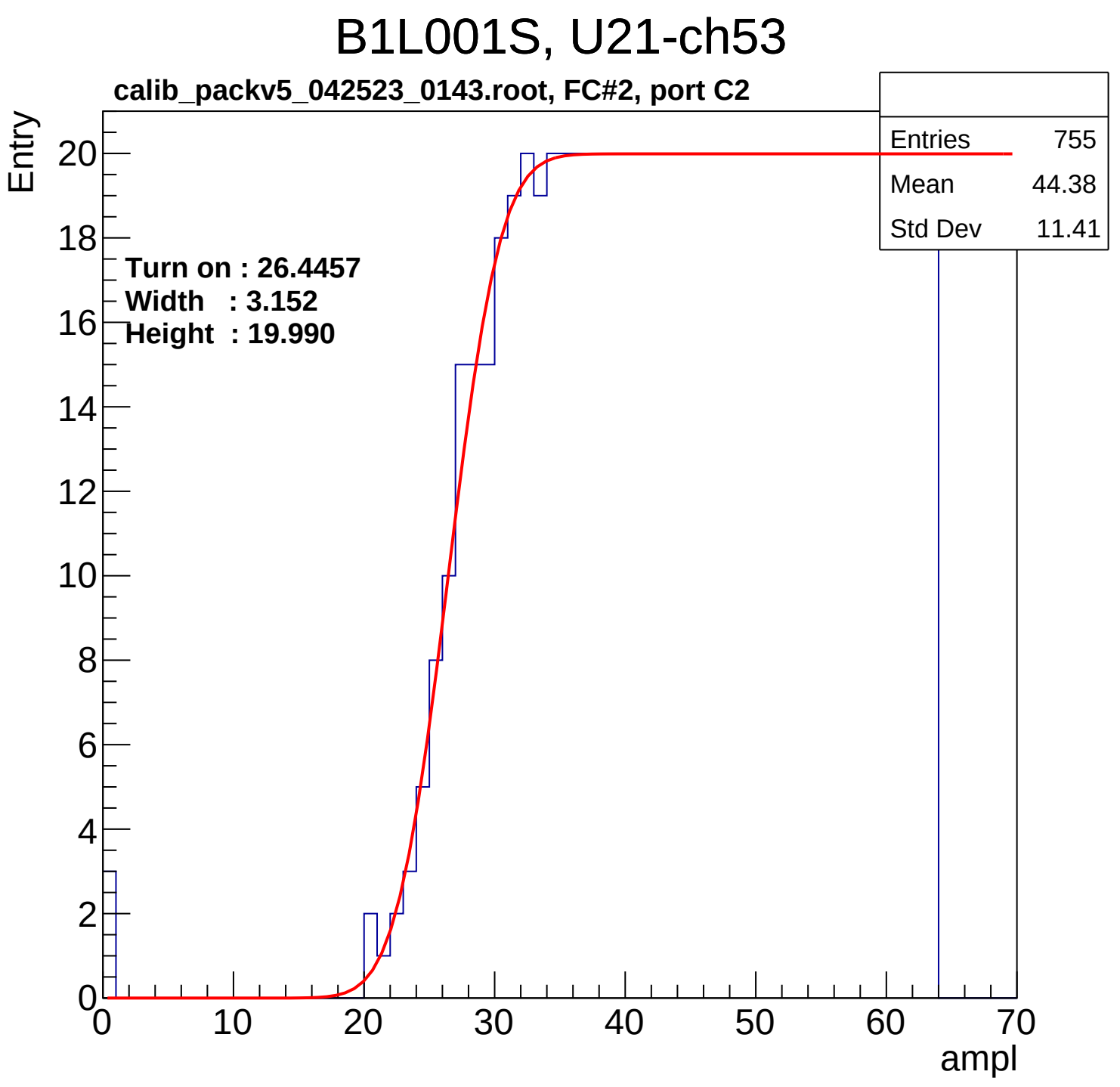
B1L001S, U21-ch53
calib_packv5_042523_0143.root, FC#2, port C2
Entries 755
Mean 44.38
Std Dev 11.41
Turn on : 26.4457
Width : 3.152
Height : 19.990
Entry
ampl
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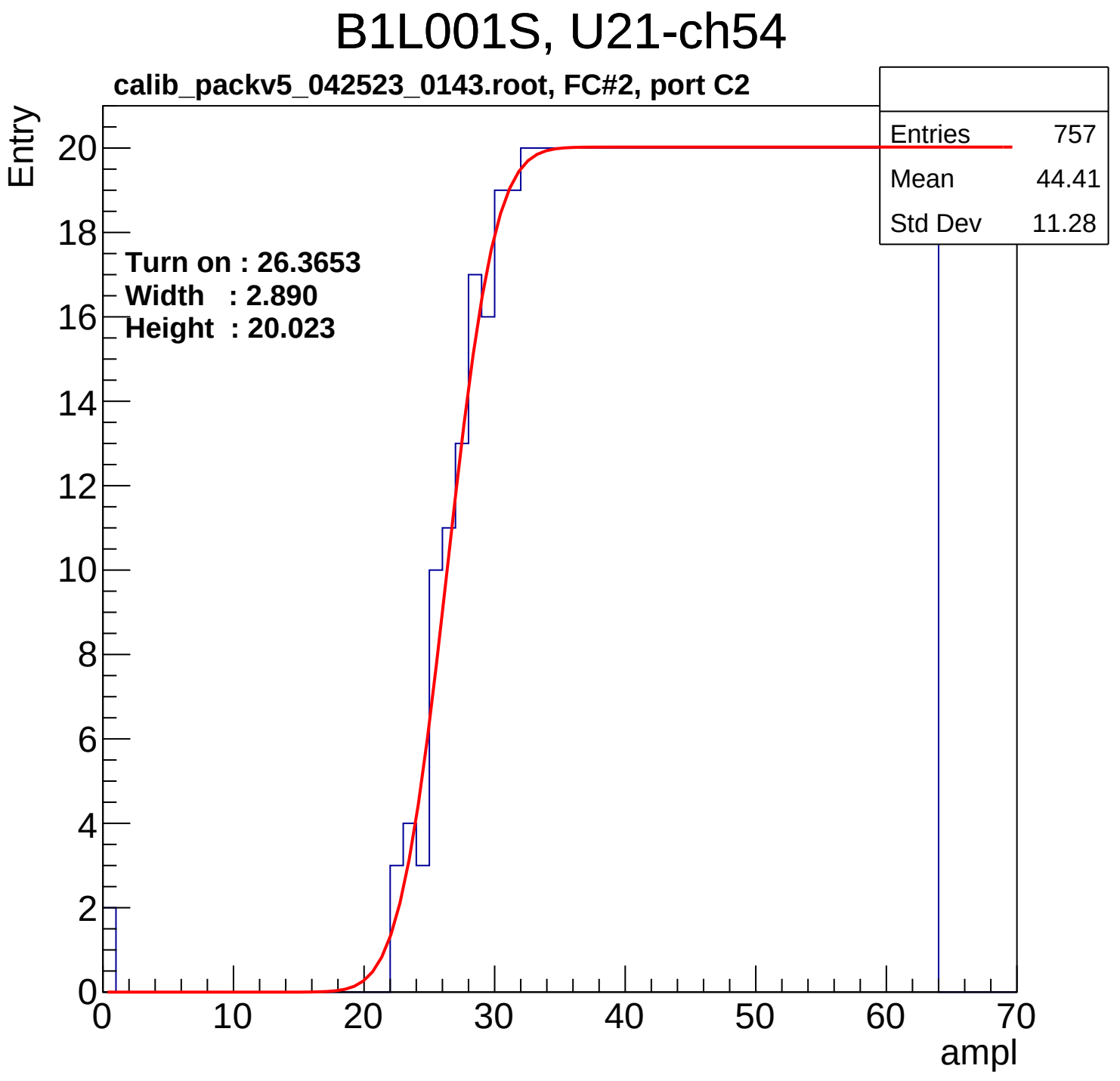
B1L001S, U21-ch54
calib_packv5_042523_0143.root, FC#2, port C2
Entries 757
Mean 44.41
Std Dev 11.28
Turn on : 26.3653
Width : 2.890
Height : 20.023
Entry
ampl
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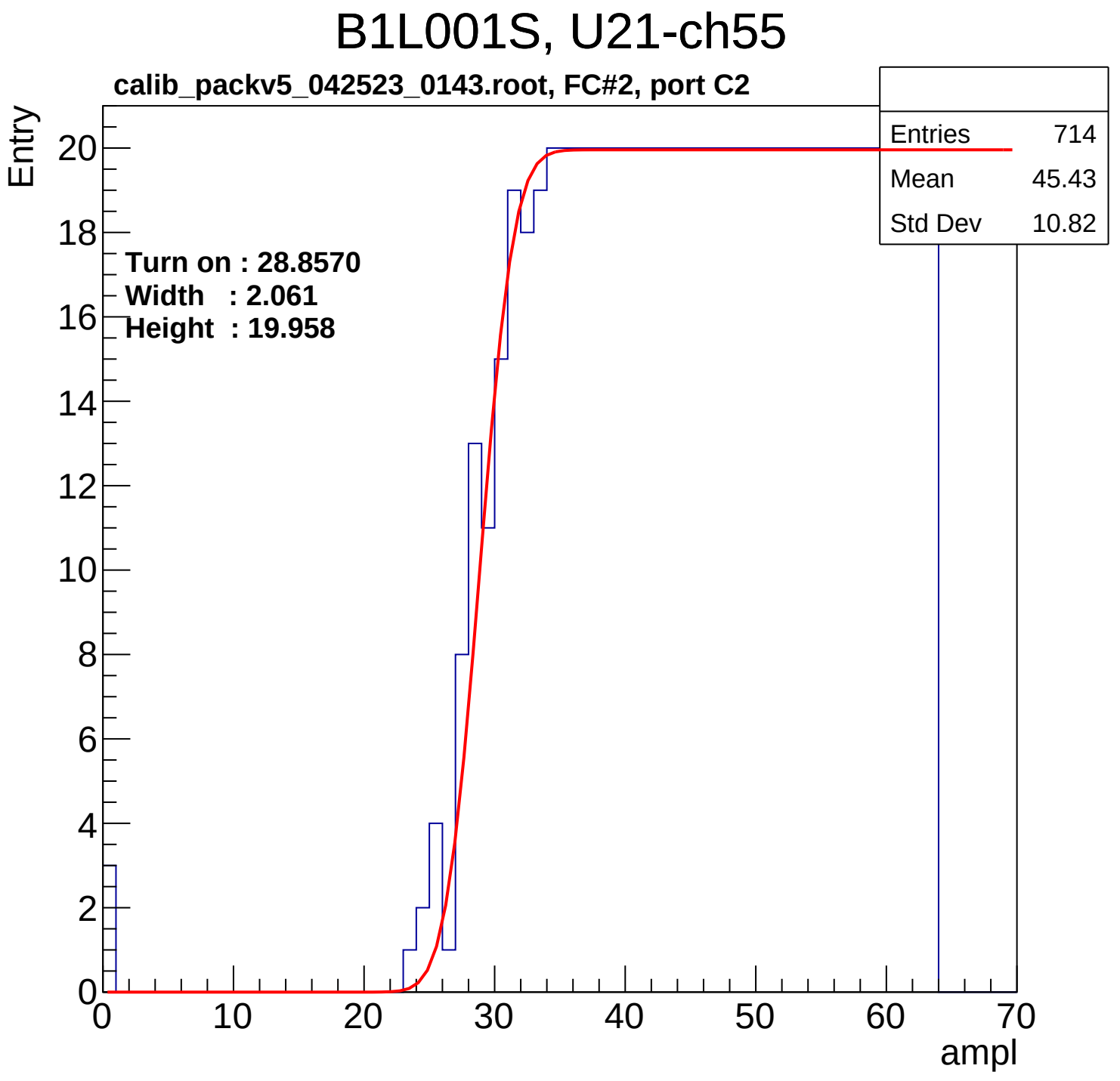
B1L001S, U21-ch55
calib_packv5_042523_0143.root, FC#2, port C2
Entries 714
Mean 45.43
Std Dev 10.82
Turn on : 28.8570
Width : 2.061
Height : 19.958
Entry
ampl
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2
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6
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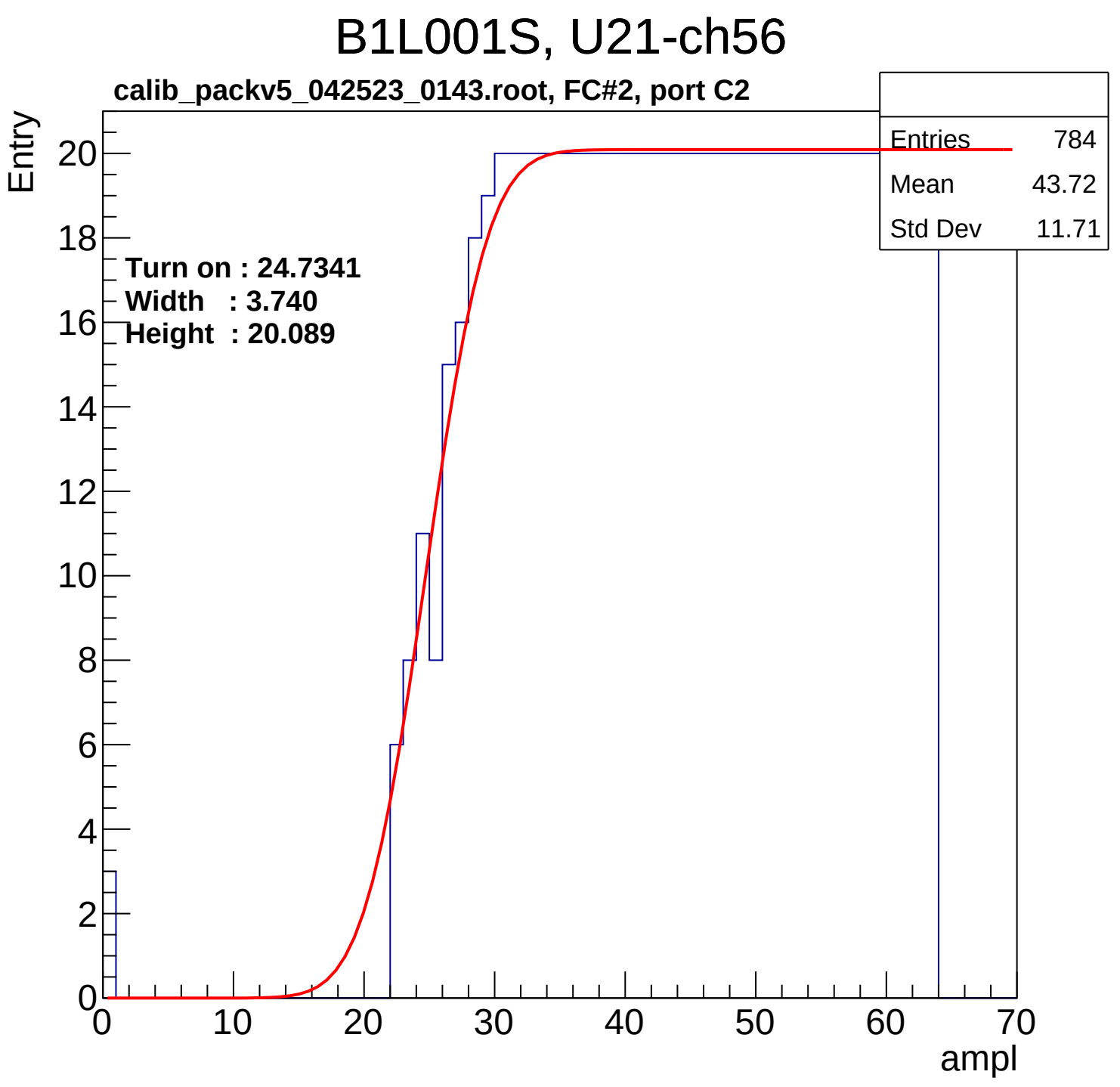
B1L001S, U21-ch56
calib_packv5_042523_0143.root, FC#2, port C2
Entries 784
Mean 43.72
Std Dev 11.71
Turn on : 24.7341
Width : 3.740
Height : 20.089
Entry
ampl
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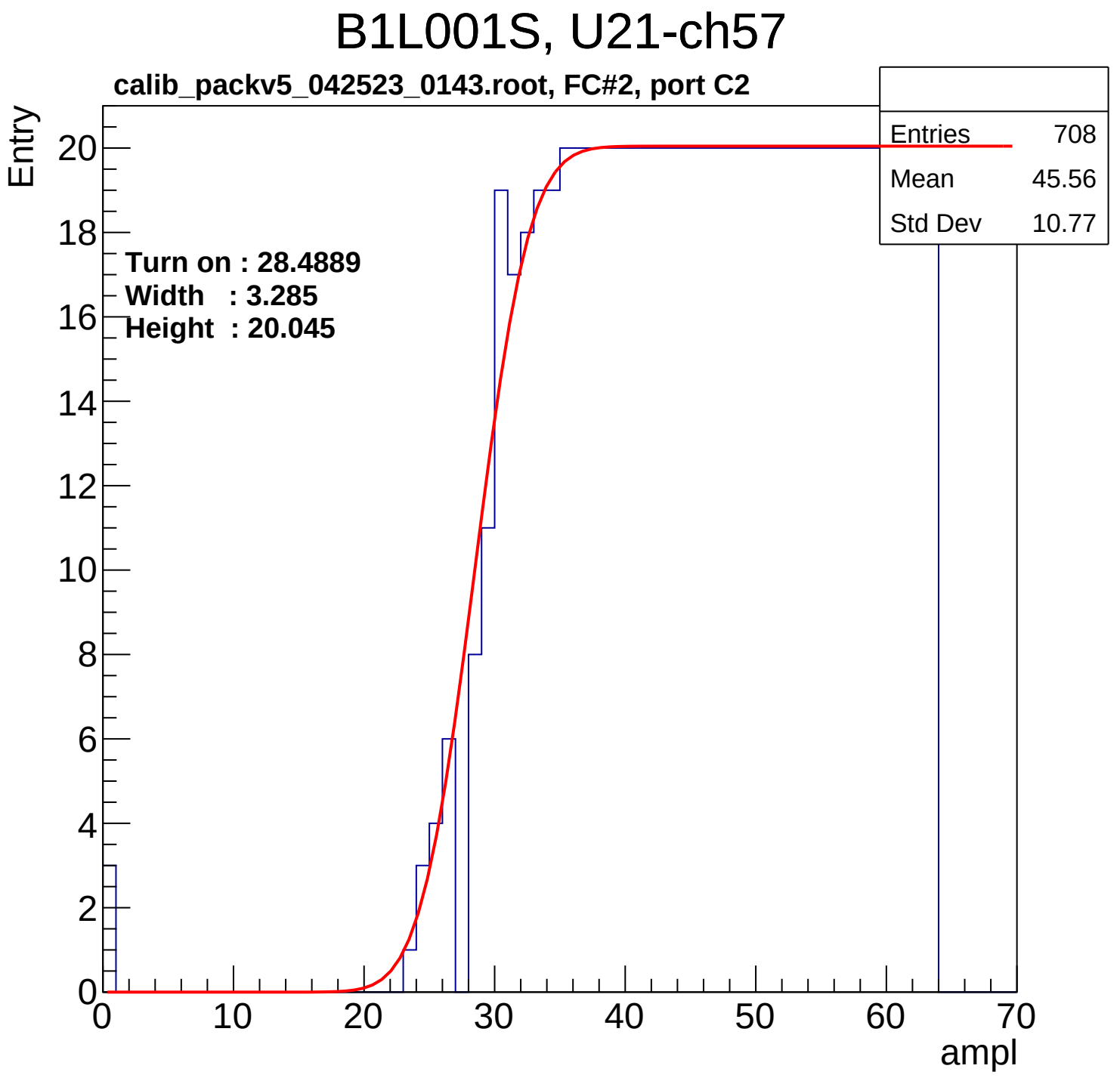
B1L001S, U21-ch57
calib_packv5_042523_0143.root, FC#2, port C2
Entries 708
Mean 45.56
Std Dev 10.77
Turn on : 28.4889
Width : 3.285
Height : 20.045
Entry
ampl
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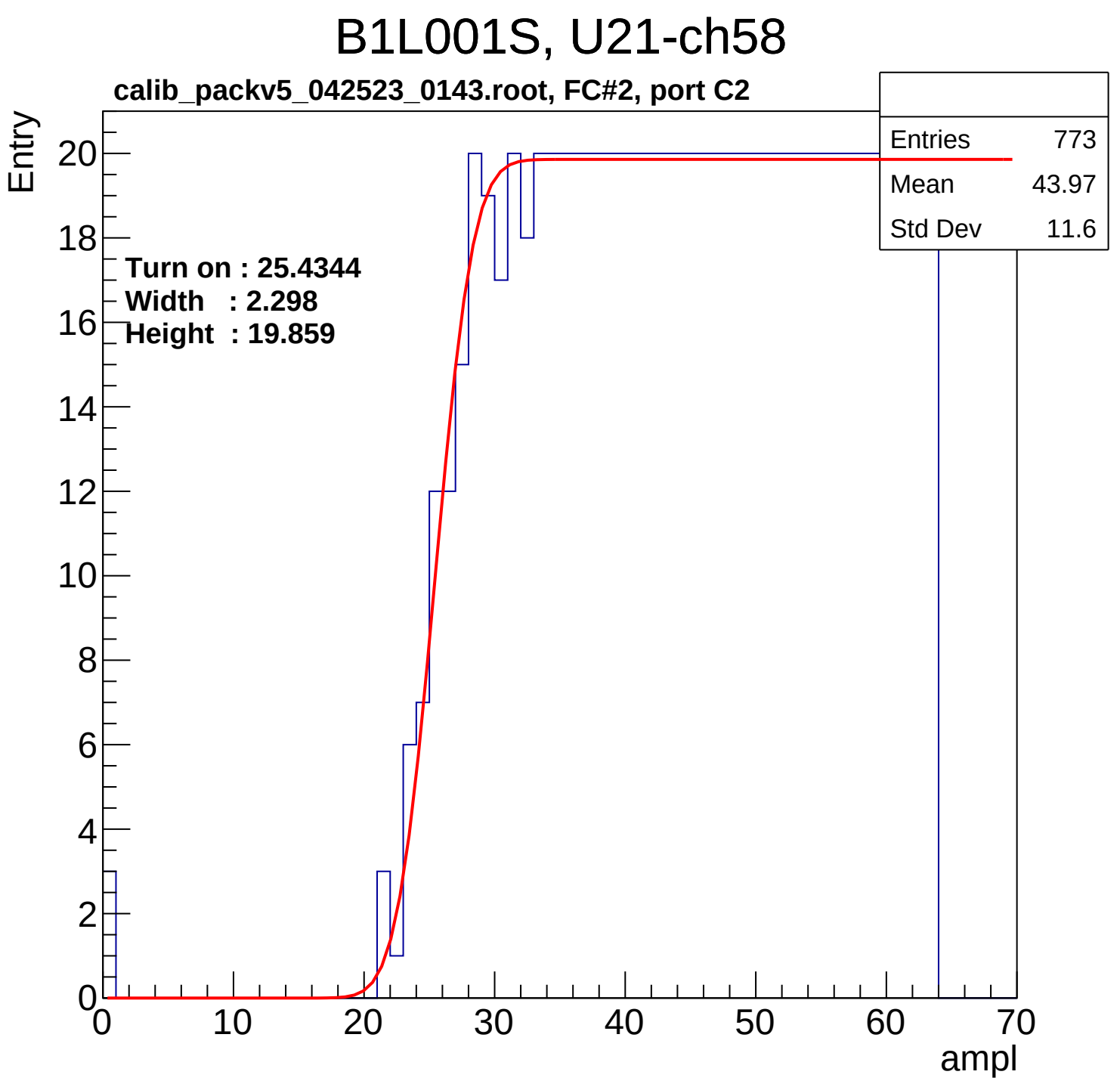
B1L001S, U21-ch58
calib_packv5_042523_0143.root, FC#2, port C2
Entries 773
Mean 43.97
Std Dev 11.6
Turn on : 25.4344
Width : 2.298
Height : 19.859
Entry
ampl
0
2
4
6
8
10
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14
16
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0
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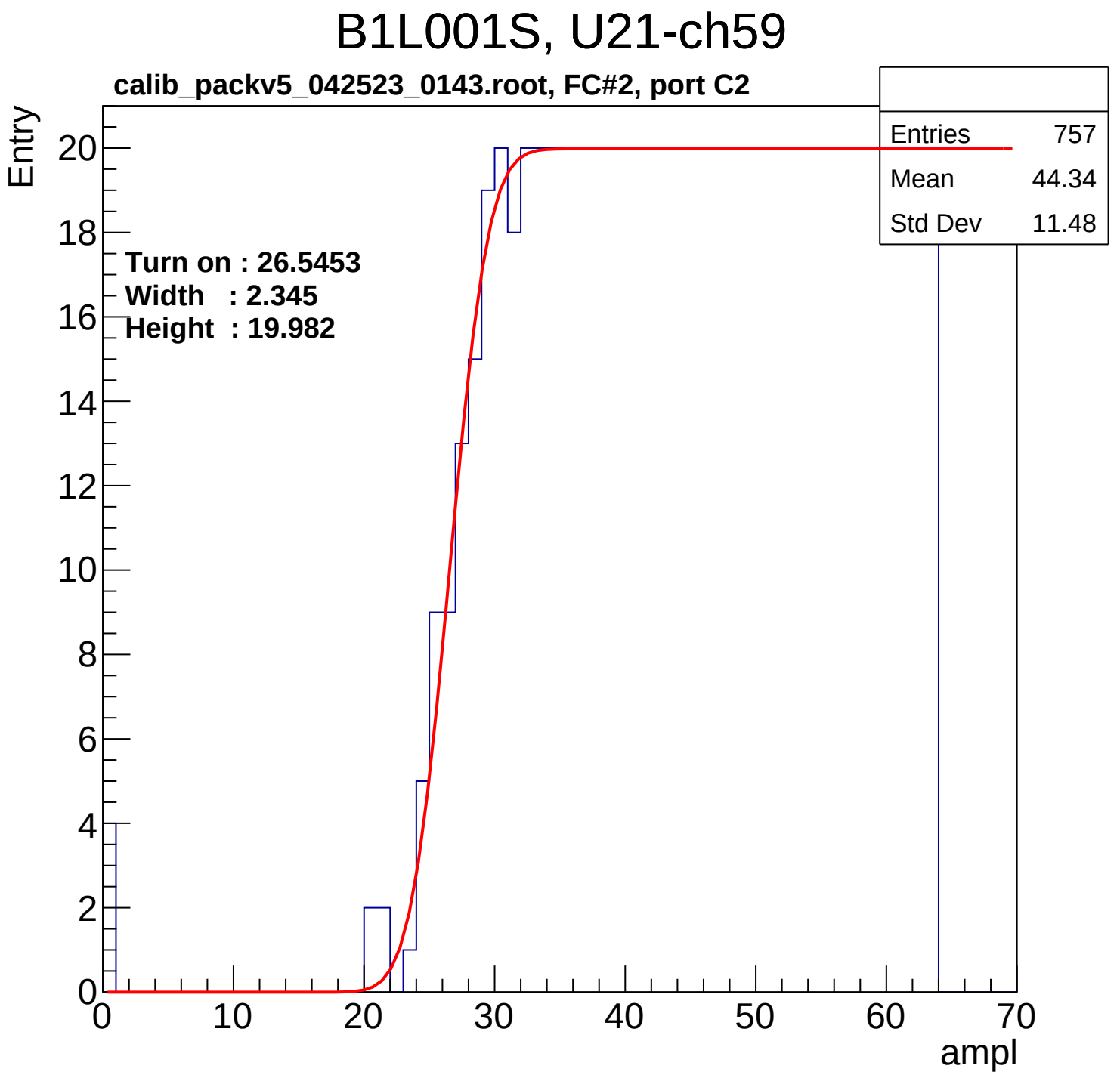
B1L001S, U21-ch59
calib_packv5_042523_0143.root, FC#2, port C2
Entries 757
Mean 44.34
Std Dev 11.48
Turn on : 26.5453
Width : 2.345
Height : 19.982
Entry
ampl
0
2
4
6
8
10
12
14
16
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0
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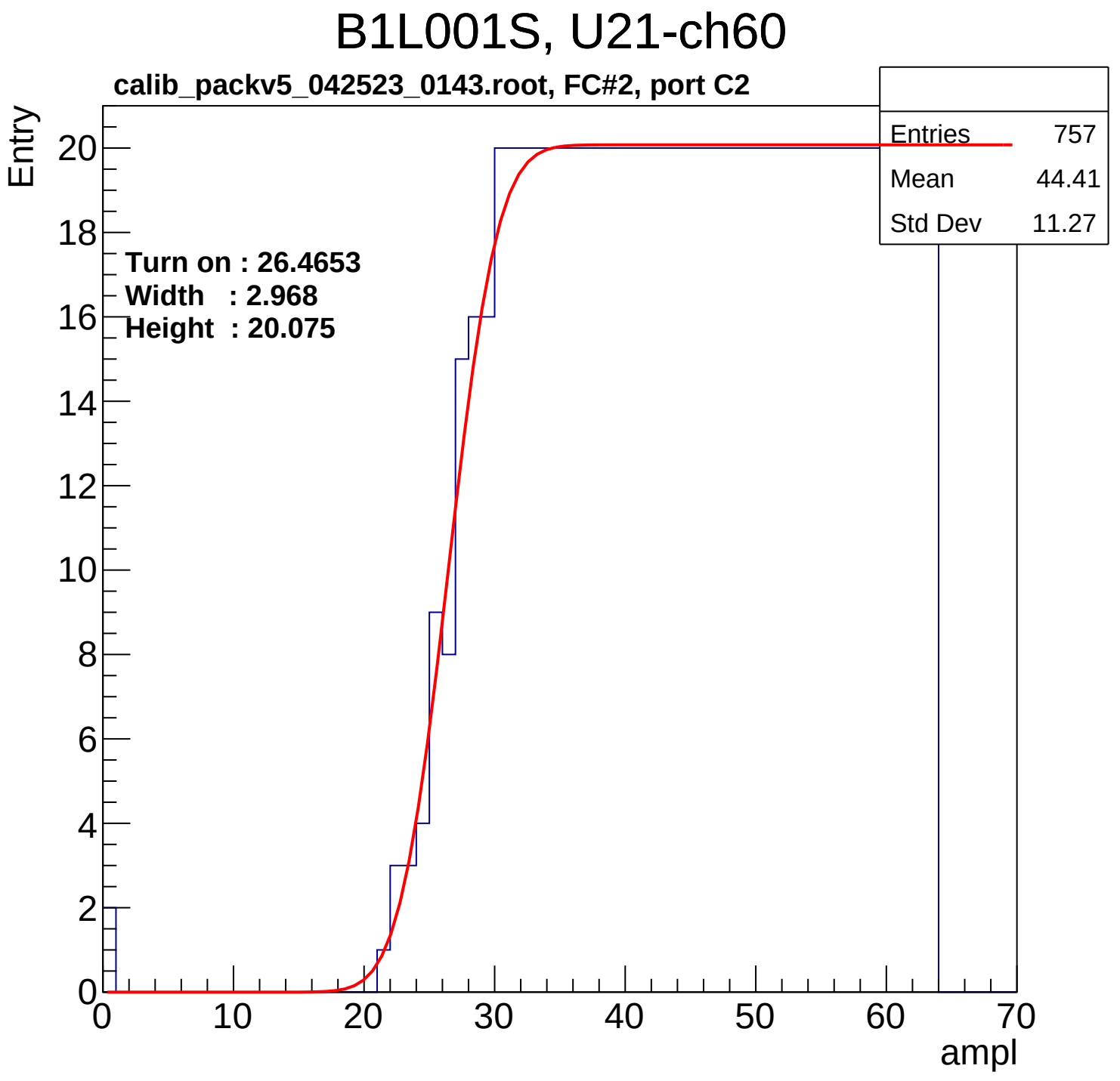
B1L001S, U21-ch60
calib_packv5_042523_0143.root, FC#2, port C2
Entries 757
Mean 44.41
Std Dev 11.27
Turn on : 26.4653
Width : 2.968
Height : 20.075
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
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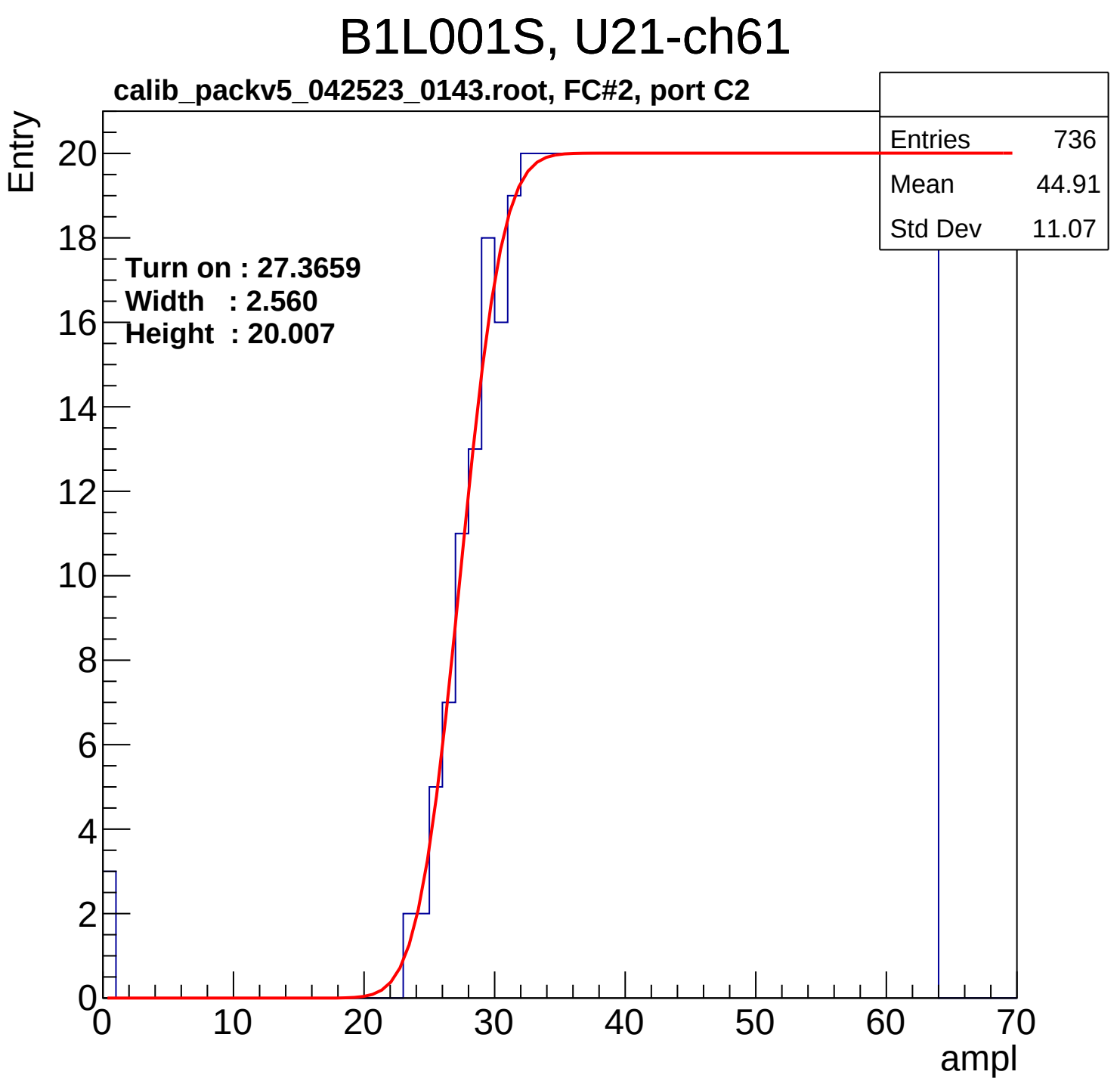
B1L001S, U21-ch61
calib_packv5_042523_0143.root, FC#2, port C2
Entries 736
Mean 44.91
Std Dev 11.07
Turn on : 27.3659
Width : 2.560
Height : 20.007
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
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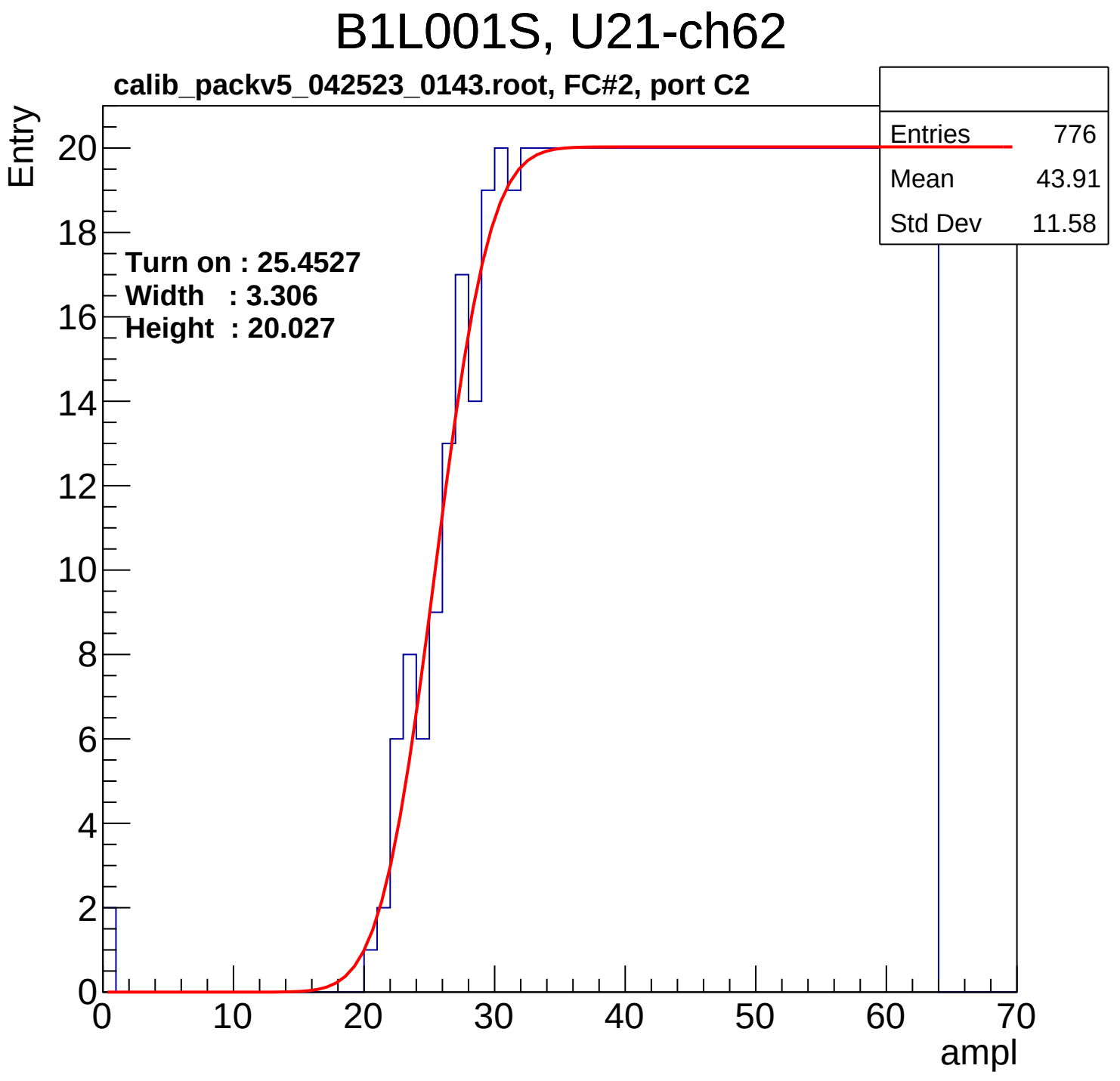
B1L001S, U21-ch62
calib_packv5_042523_0143.root, FC#2, port C2
Entries 776
Mean 43.91
Std Dev 11.58
Turn on : 25.4527
Width : 3.306
Height : 20.027
Entry
ampl
0
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6
8
10
12
14
16
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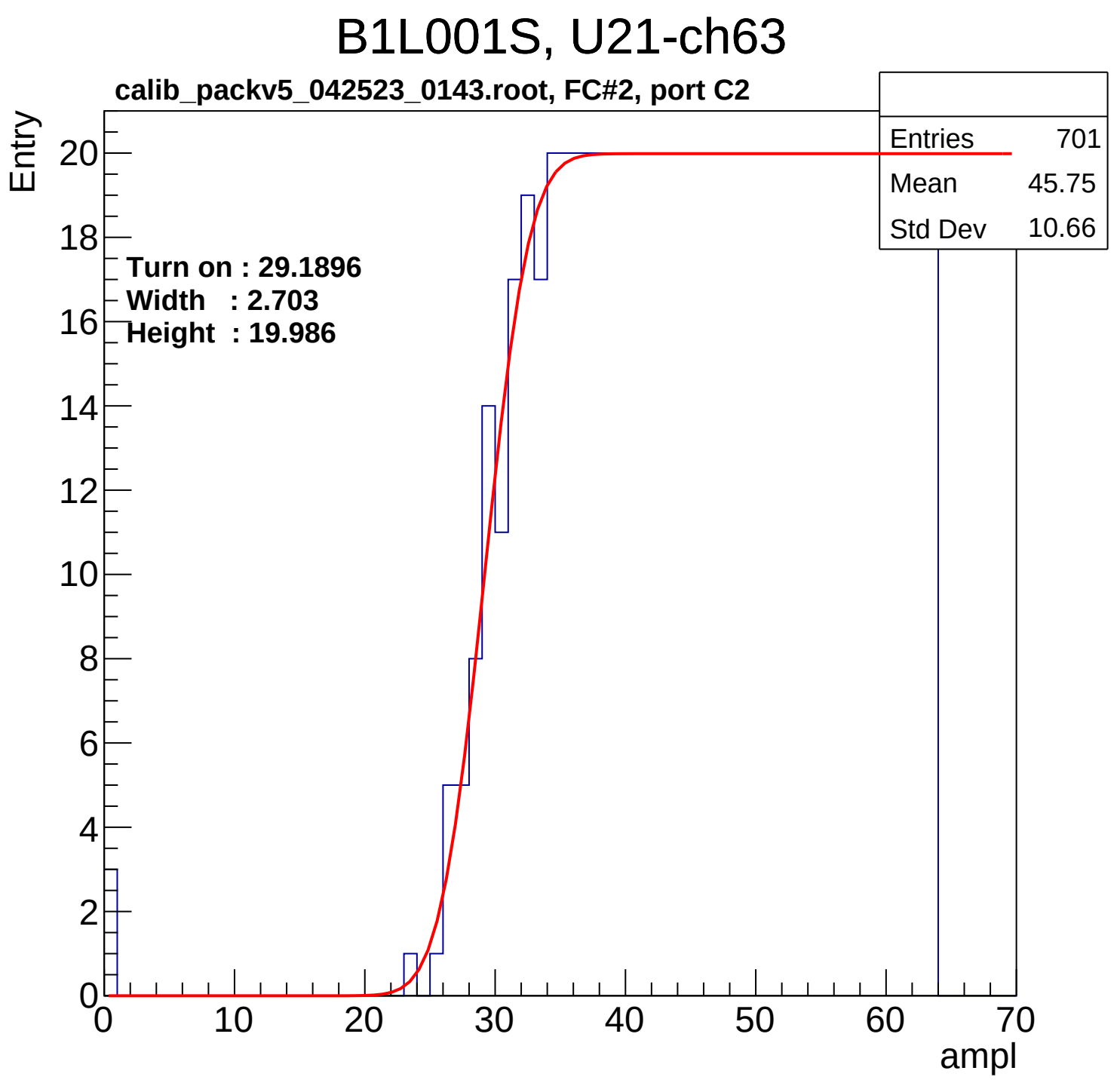
B1L001S, U21-ch63
calib_packv5_042523_0143.root, FC#2, port C2
Entries 701
Mean 45.75
Std Dev 10.66
Turn on : 29.1896
Width : 2.703
Height : 19.986
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
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20
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40
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60
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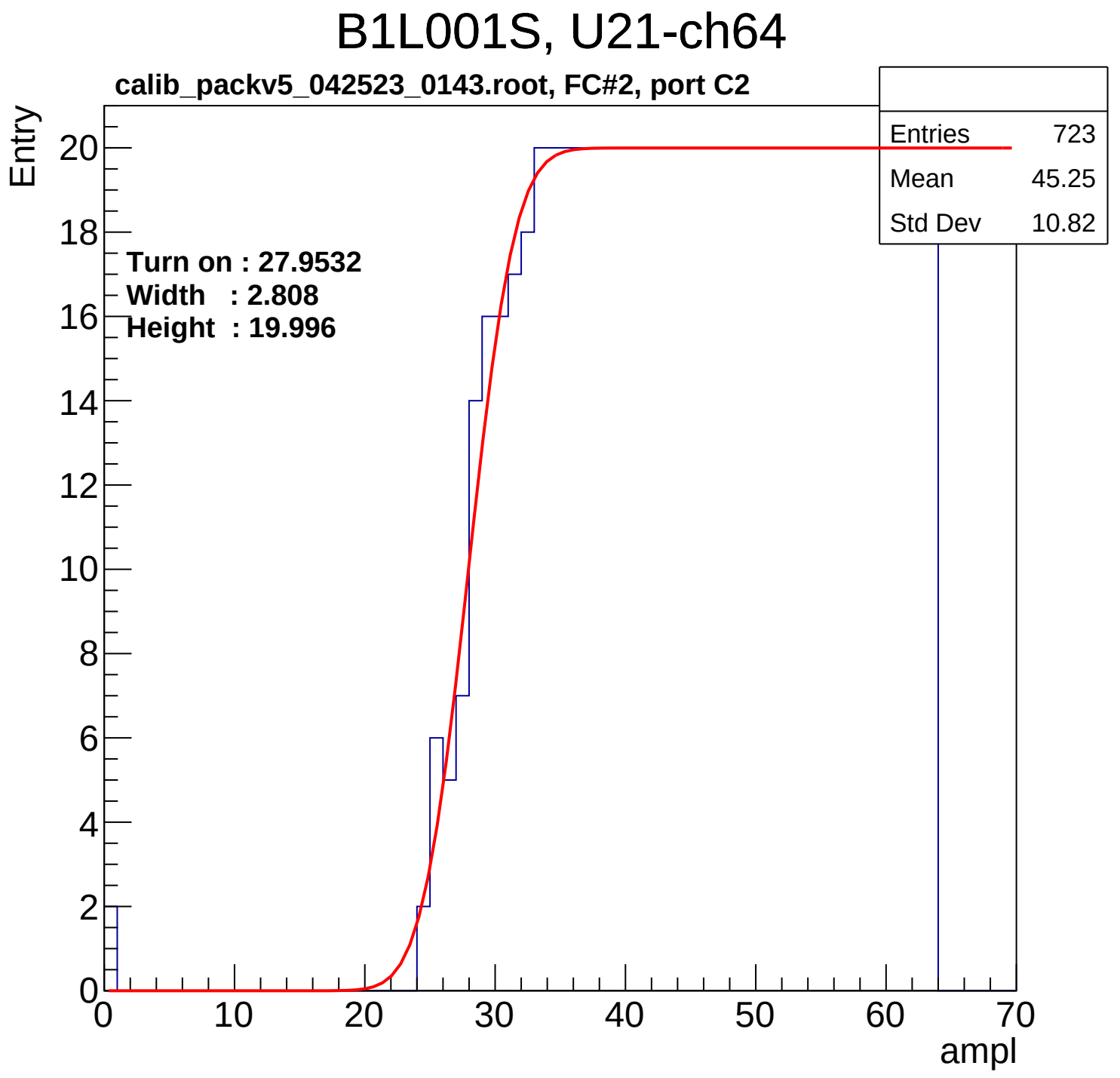
B1L001S, U21-ch64
calib_packv5_042523_0143.root, FC#2, port C2
Entries 723
Mean 45.25
Std Dev 10.82
Turn on : 27.9532
Width : 2.808
Height : 19.996
Entry
ampl
0
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4
6
8
10
12
14
16
18
20
0
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20
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40
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60
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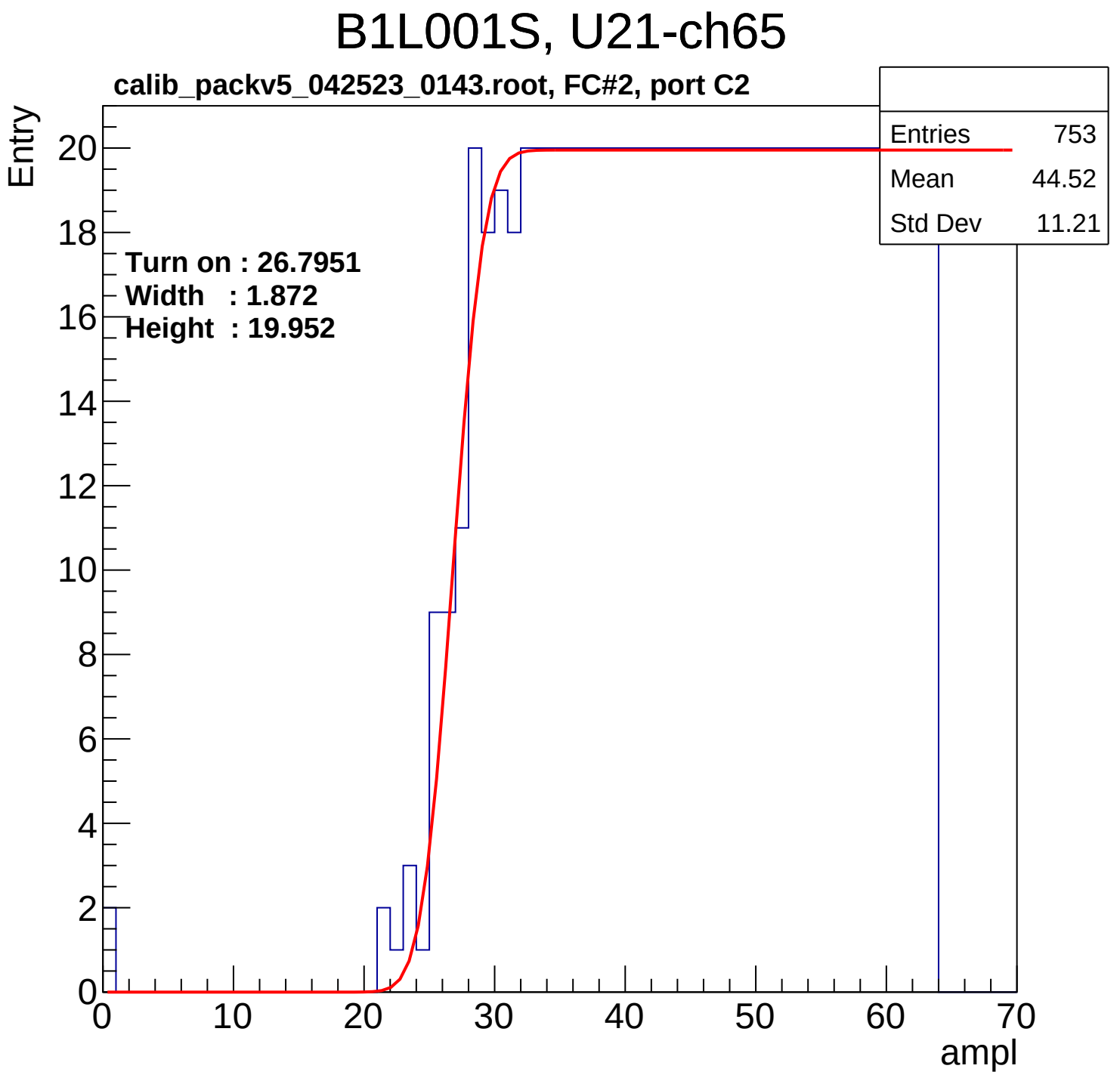
B1L001S, U21-ch65
calib_packv5_042523_0143.root, FC#2, port C2
Entries 753
Mean 44.52
Std Dev 11.21
Turn on : 26.7951
Width : 1.872
Height : 19.952
Entry
ampl
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6
8
10
12
14
16
18
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0
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60
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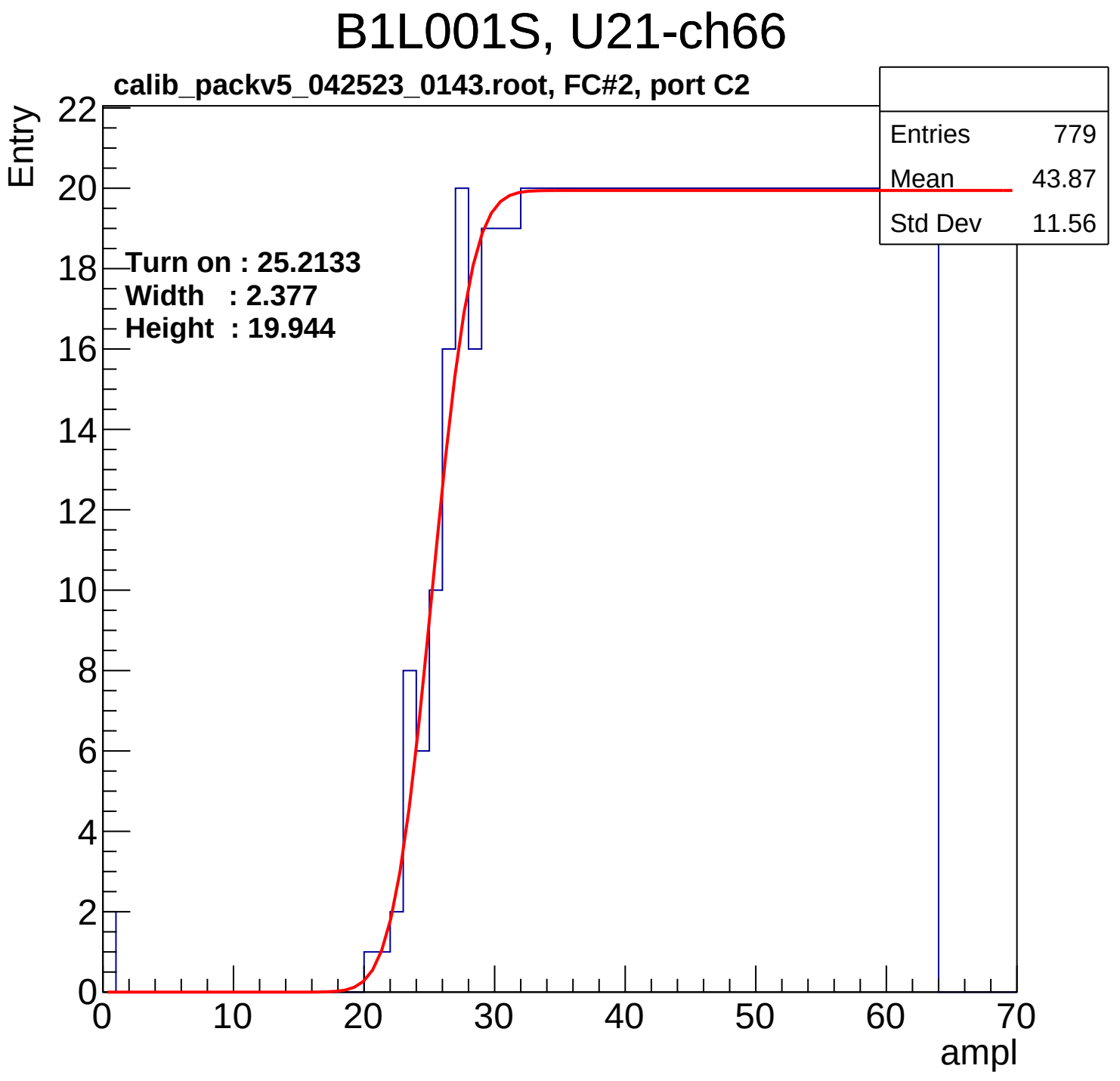
B1L001S, U21-ch66
calib_packv5_042523_0143.root, FC#2, port C2
Entries 779
Mean 43.87
Std Dev 11.56
Turn on : 25.2133
Width : 2.377
Height : 19.944
Entry
ampl
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6
8
10
12
14
16
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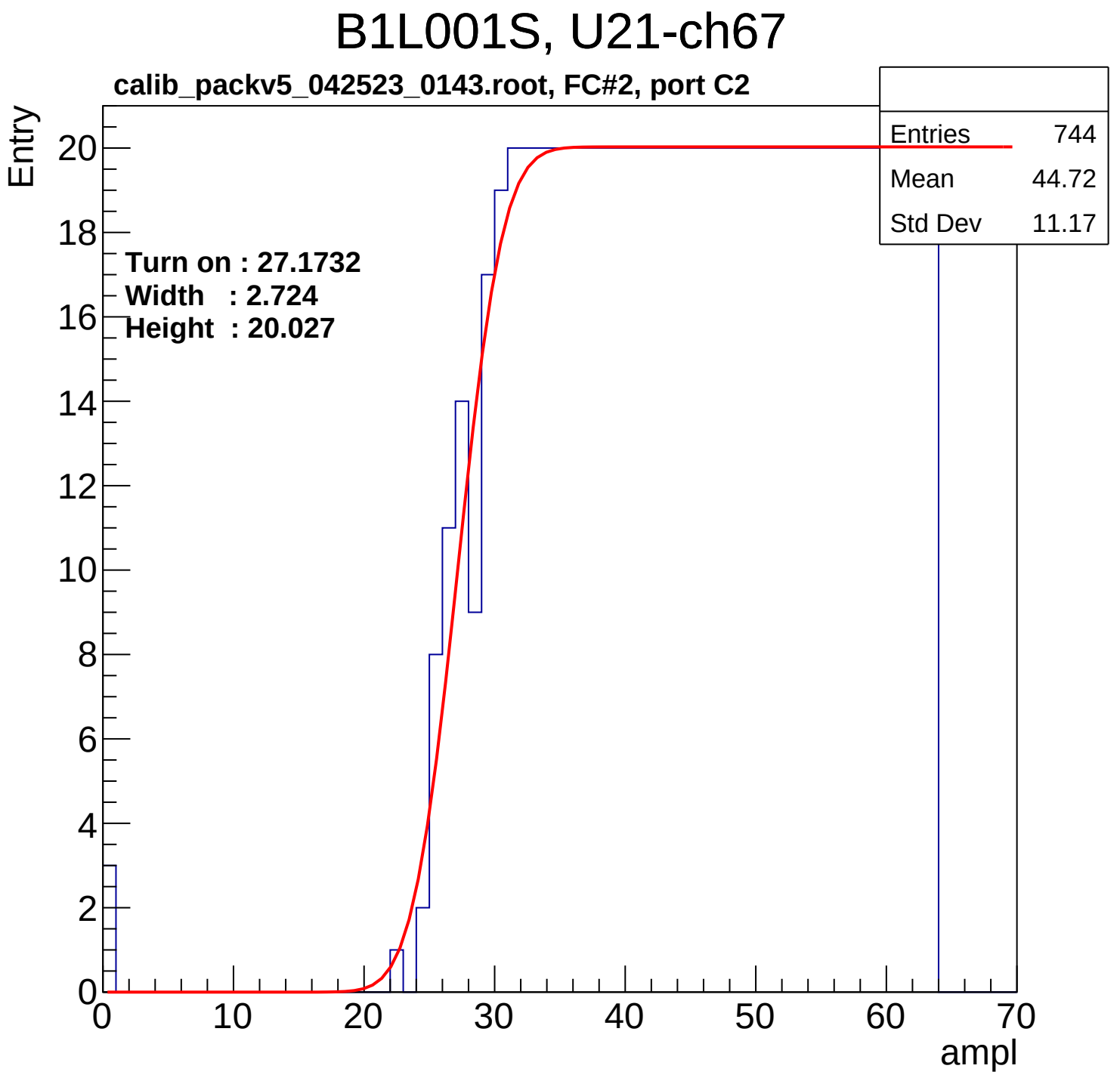
B1L001S, U21-ch67
calib_packv5_042523_0143.root, FC#2, port C2
Entries 744
Mean 44.72
Std Dev 11.17
Turn on : 27.1732
Width : 2.724
Height : 20.027
Entry
ampl
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6
8
10
12
14
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18
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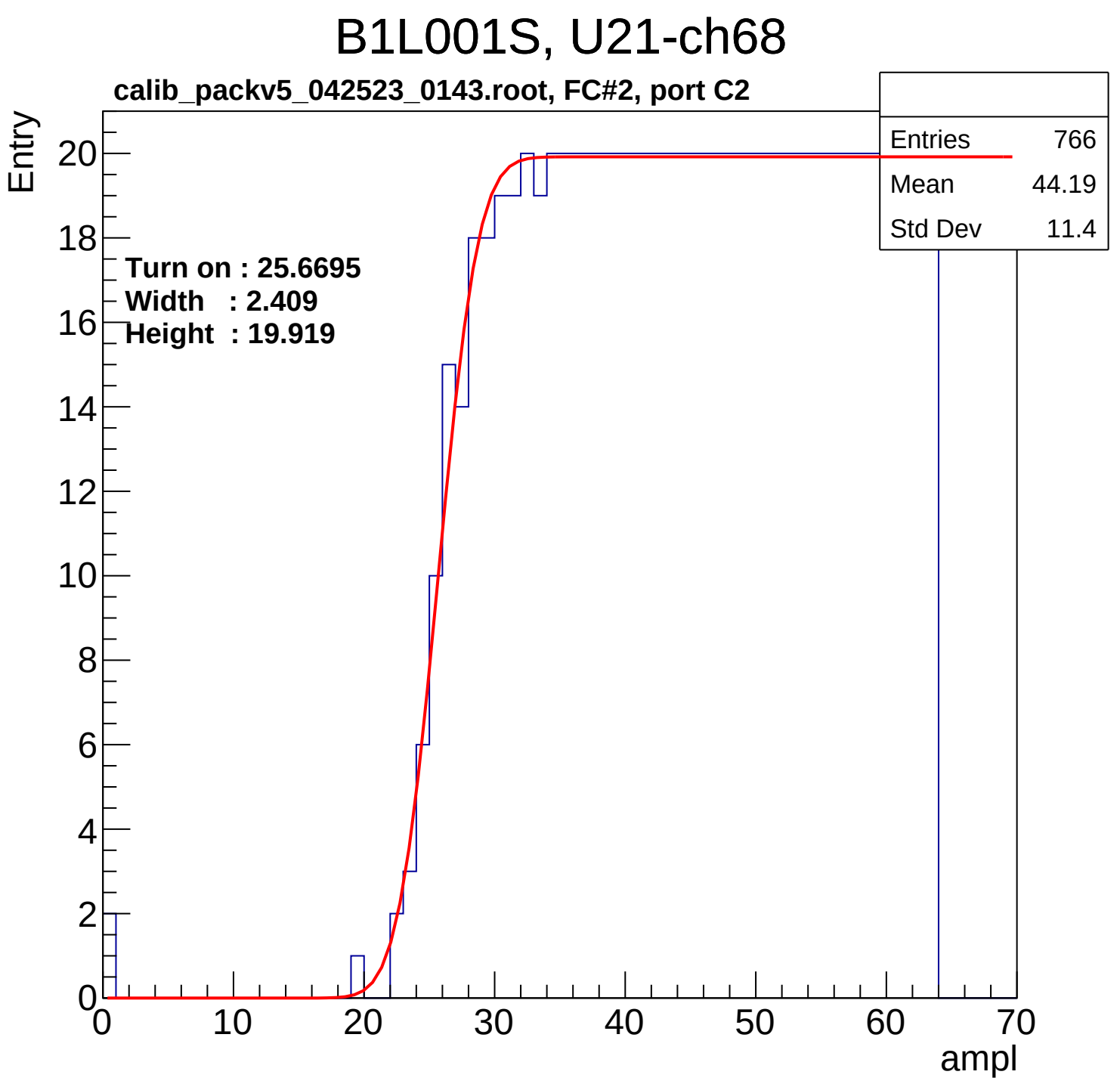
B1L001S, U21-ch68
calib_packv5_042523_0143.root, FC#2, port C2
Entries 766
Mean 44.19
Std Dev 11.4
Turn on : 25.6695
Width : 2.409
Height : 19.919
Entry
ampl
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6
8
10
12
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16
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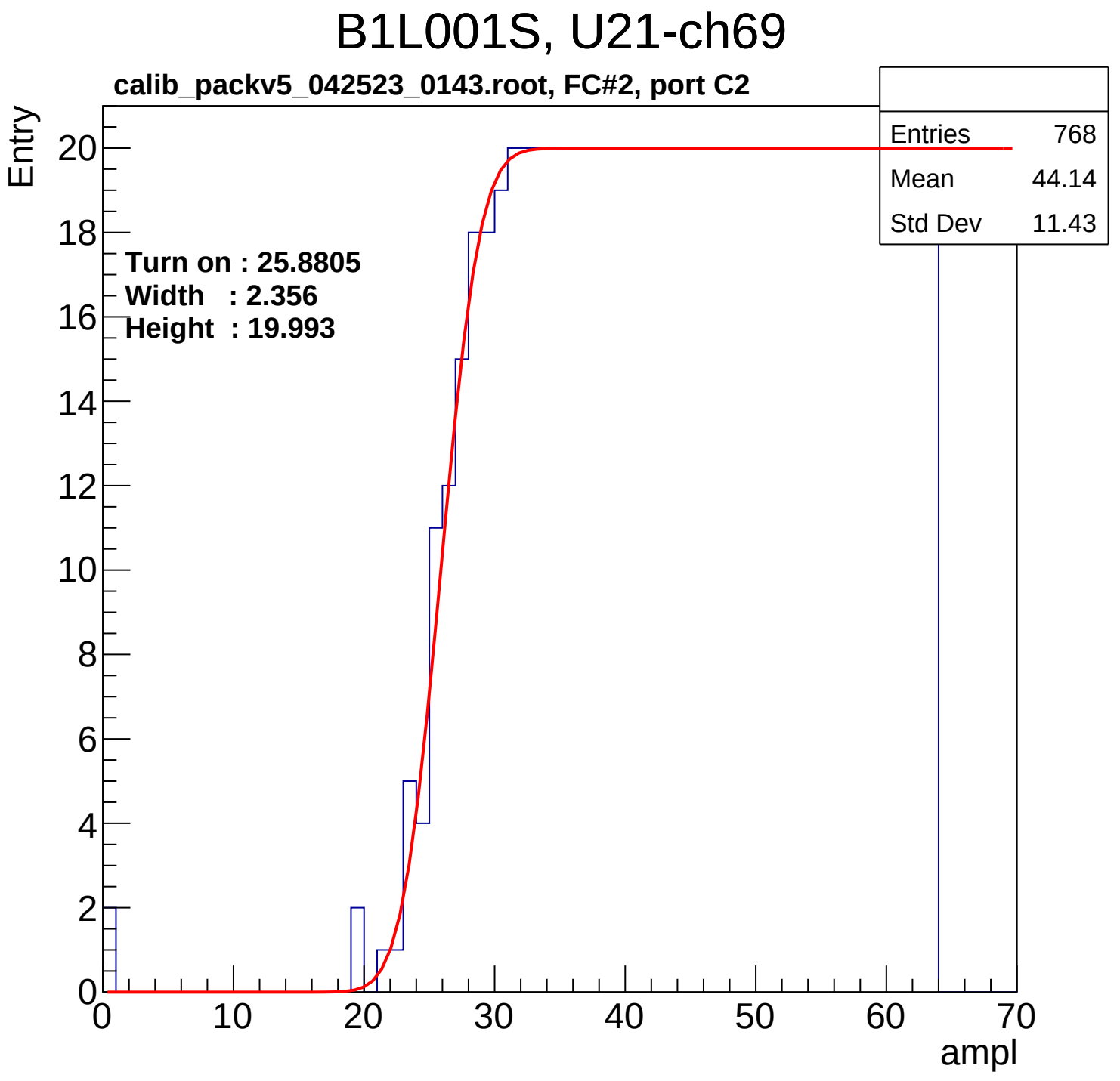
B1L001S, U21-ch69
calib_packv5_042523_0143.root, FC#2, port C2
Entries 768
Mean 44.14
Std Dev 11.43
Turn on : 25.8805
Width : 2.356
Height : 19.993
Entry
ampl
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6
8
10
12
14
16
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0
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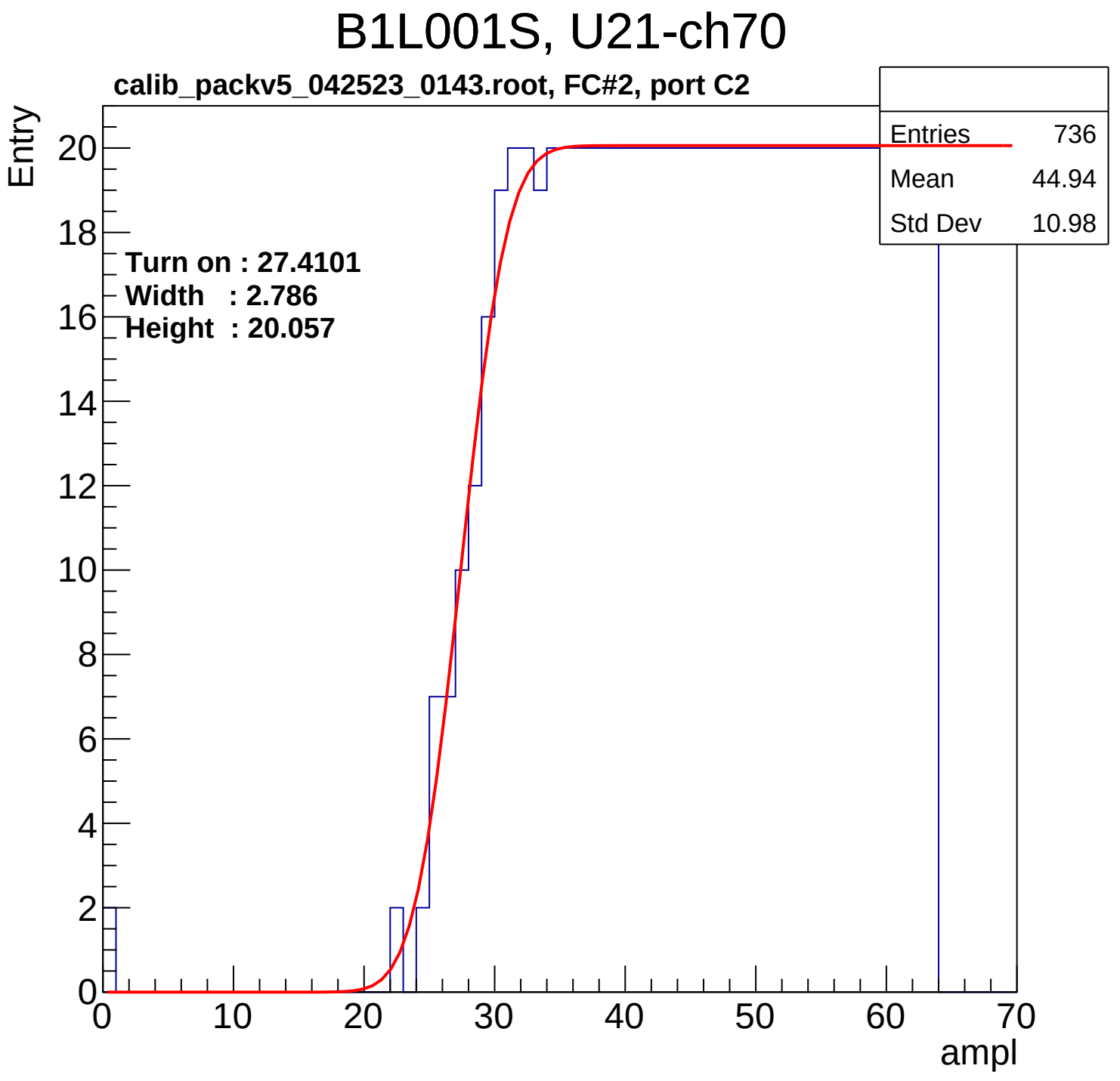
B1L001S, U21-ch70
calib_packv5_042523_0143.root, FC#2, port C2
Entries 736
Mean 44.94
Std Dev 10.98
Turn on : 27.4101
Width : 2.786
Height : 20.057
Entry
ampl
0
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6
8
10
12
14
16
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0
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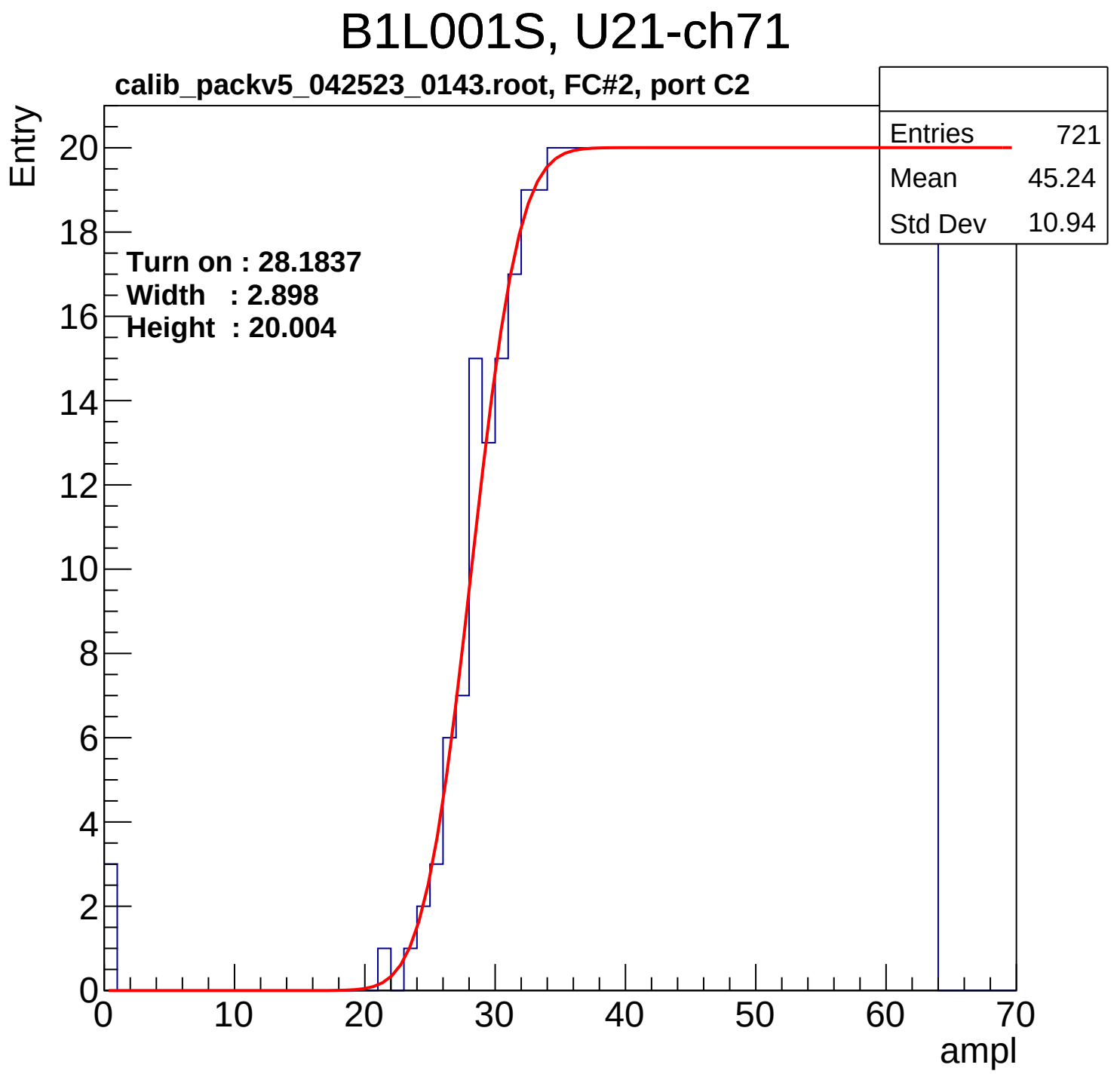
B1L001S, U21-ch71
calib_packv5_042523_0143.root, FC#2, port C2
Entries 721
Mean 45.24
Std Dev 10.94
Turn on : 28.1837
Width : 2.898
Height : 20.004
Entry
ampl
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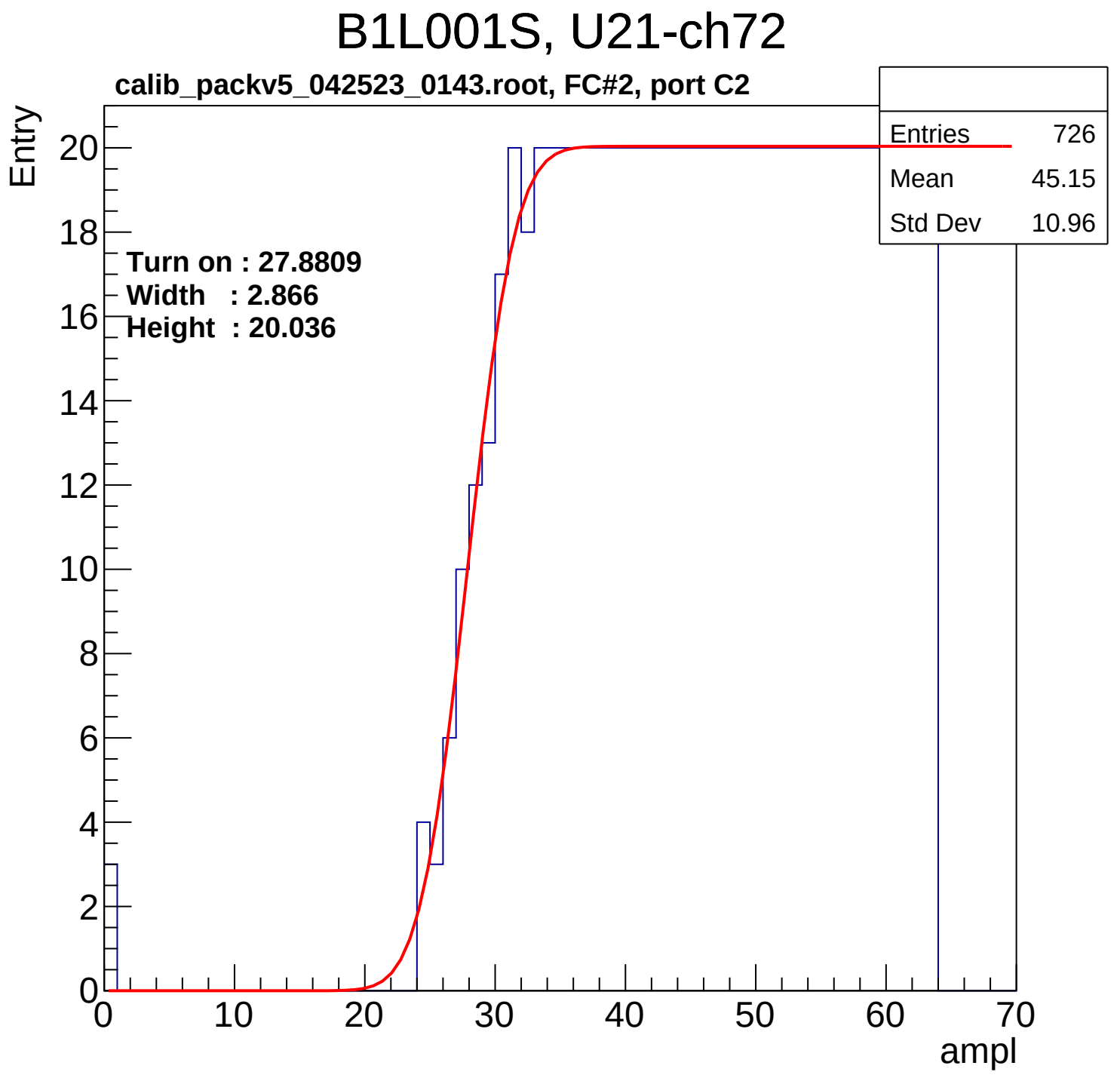
B1L001S, U21-ch72
calib_packv5_042523_0143.root, FC#2, port C2
Entries 726
Mean 45.15
Std Dev 10.96
Turn on : 27.8809
Width : 2.866
Height : 20.036
Entry
ampl
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14
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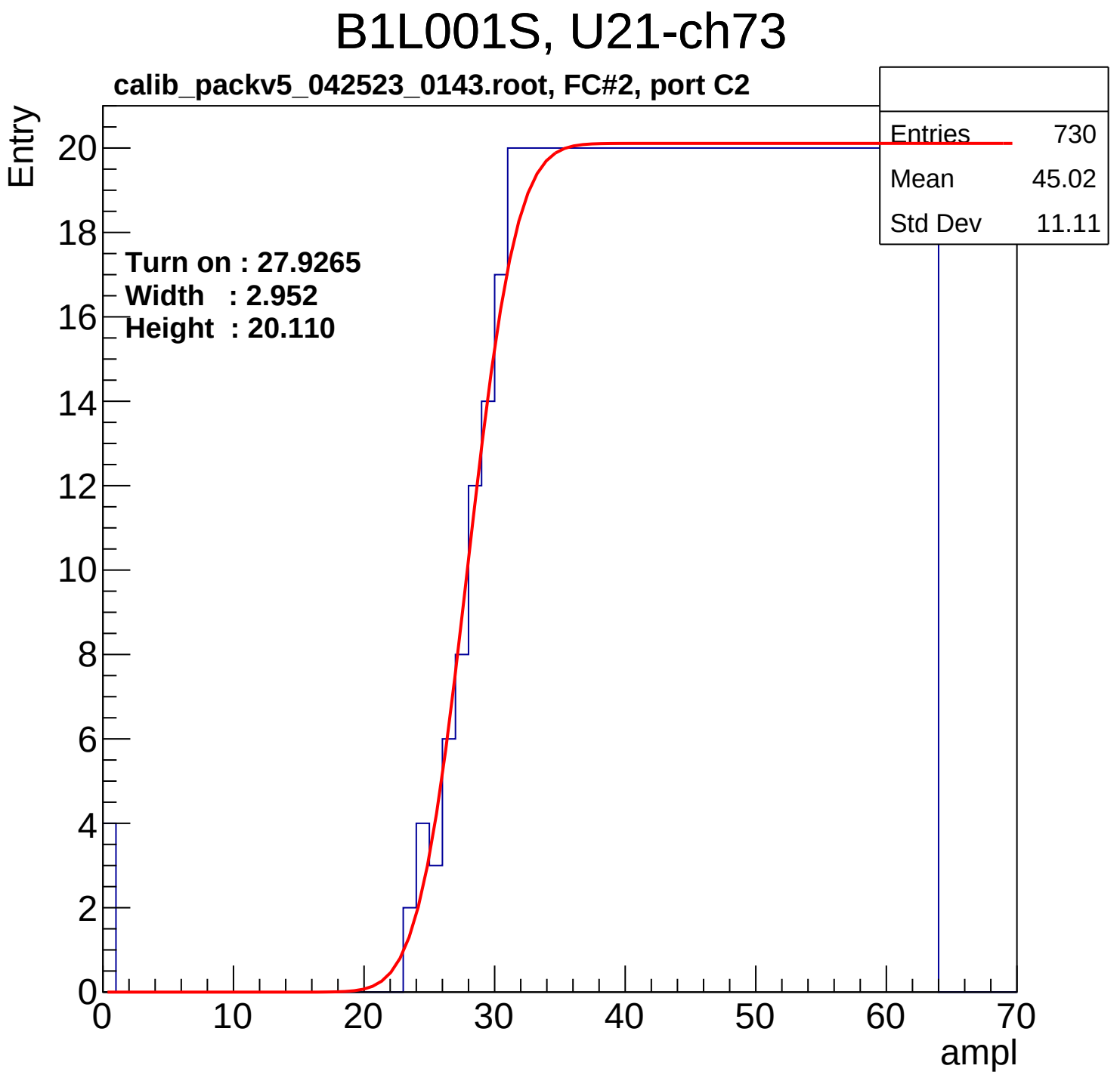
B1L001S, U21-ch73
calib_packv5_042523_0143.root, FC#2, port C2
Entries 730
Mean 45.02
Std Dev 11.11
Turn on : 27.9265
Width : 2.952
Height : 20.110
Entry
ampl
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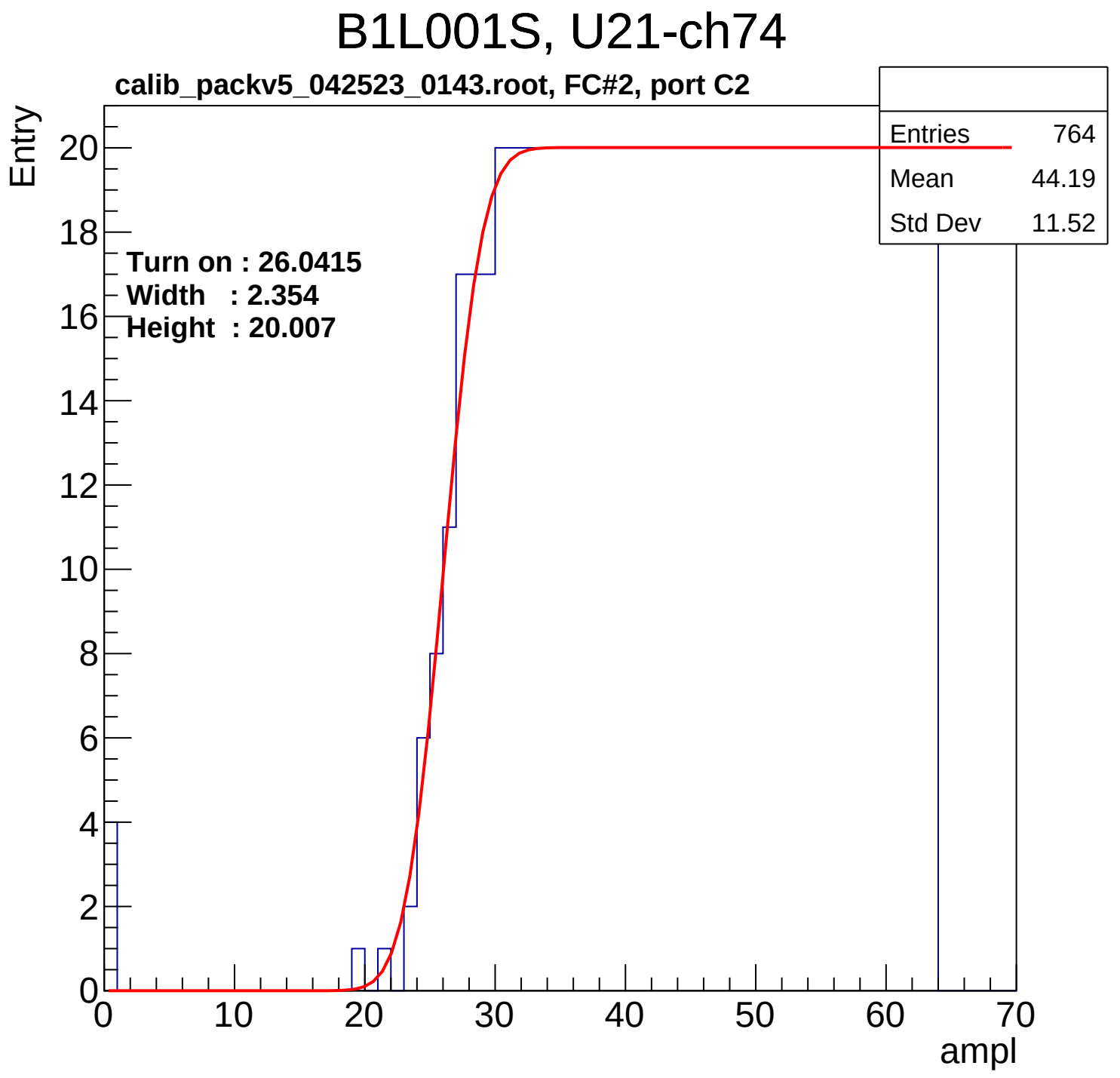
B1L001S, U21-ch74
calib_packv5_042523_0143.root, FC#2, port C2
Entries 764
Mean 44.19
Std Dev 11.52
Turn on : 26.0415
Width : 2.354
Height : 20.007
Entry
ampl
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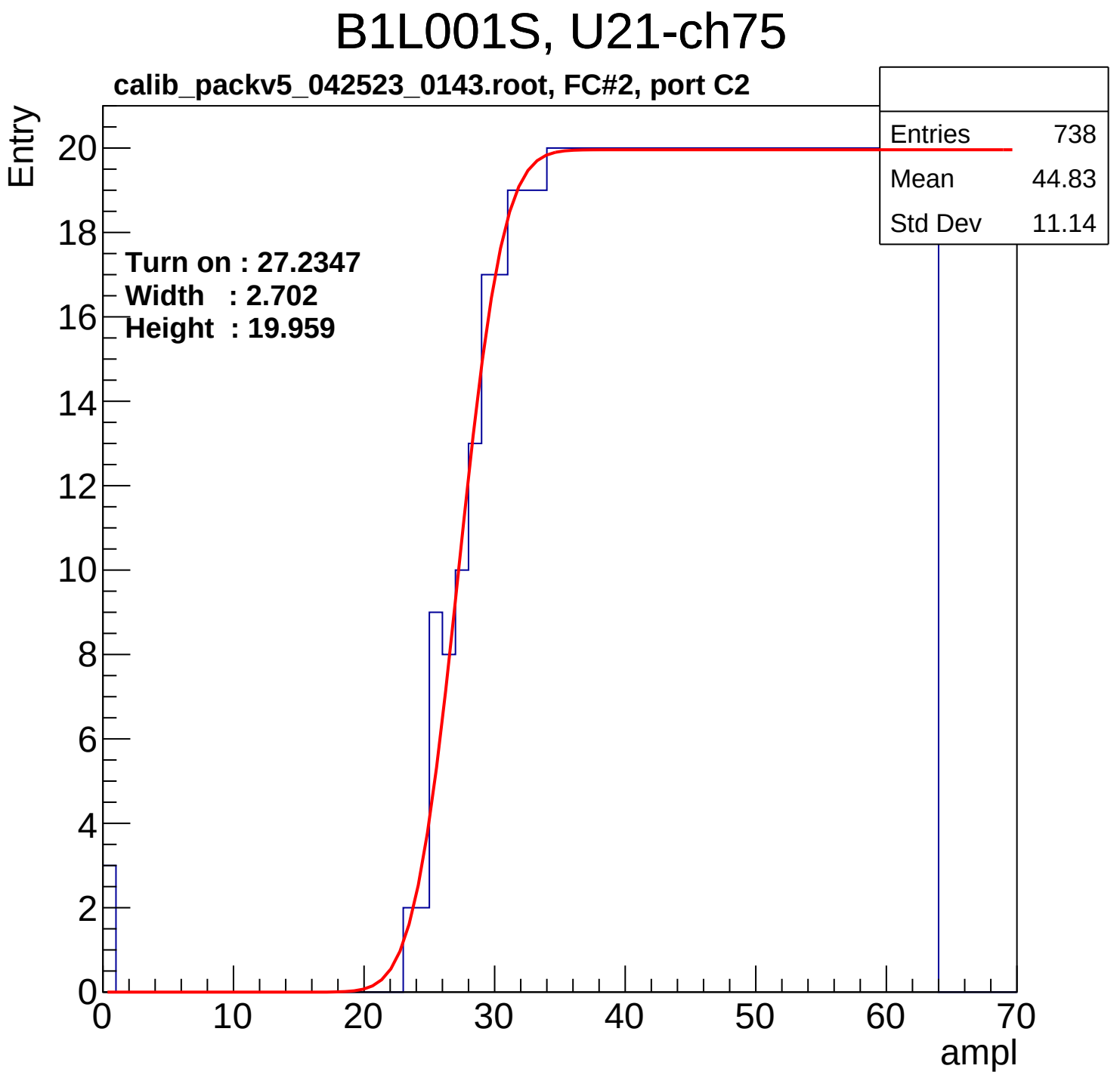
B1L001S, U21-ch75
calib_packv5_042523_0143.root, FC#2, port C2
Entries 738
Mean 44.83
Std Dev 11.14
Turn on : 27.2347
Width : 2.702
Height : 19.959
Entry
ampl
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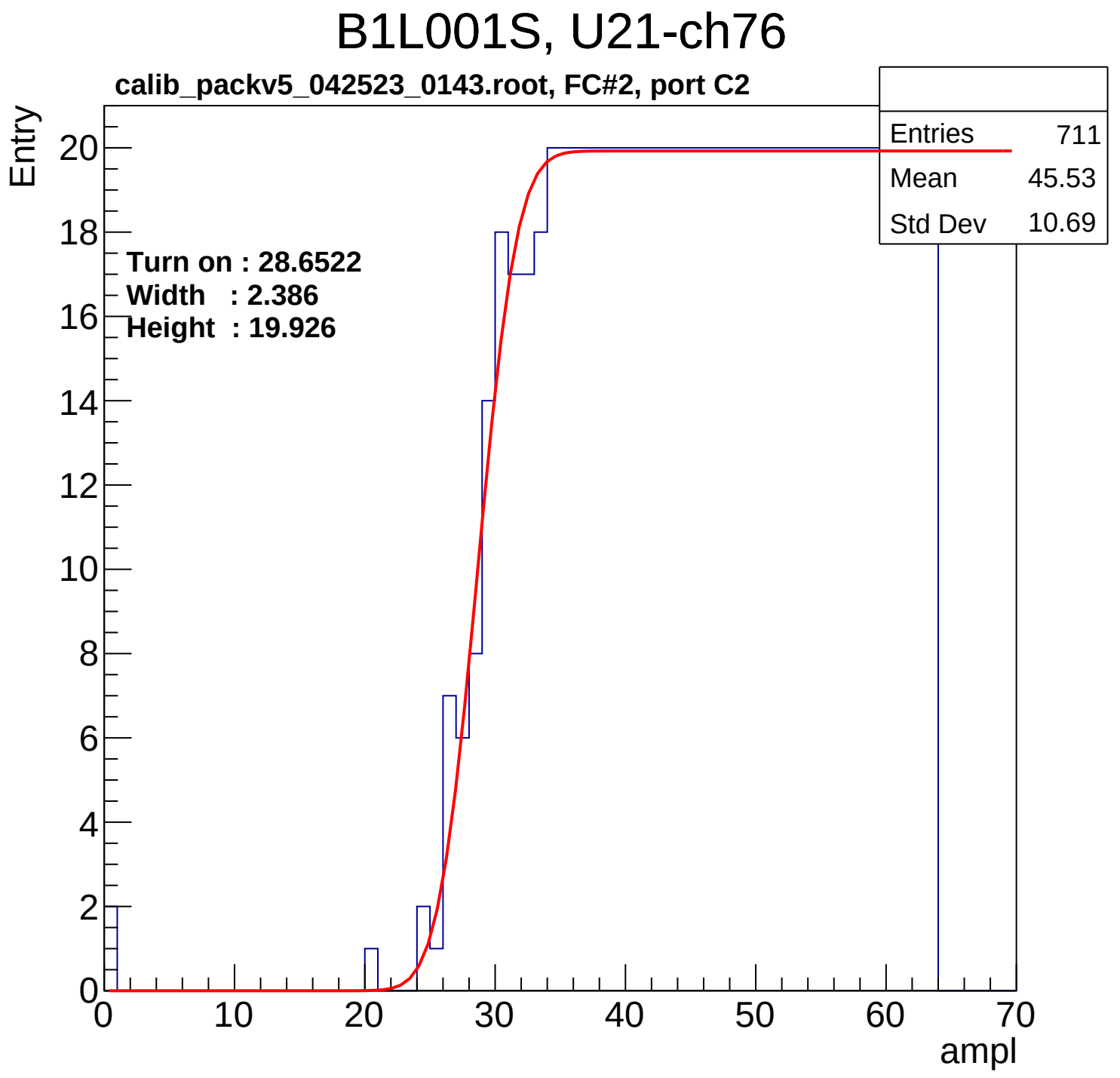
B1L001S, U21-ch76
calib_packv5_042523_0143.root, FC#2, port C2
Entries 711
Mean 45.53
Std Dev 10.69
Turn on : 28.6522
Width : 2.386
Height : 19.926
Entry
ampl
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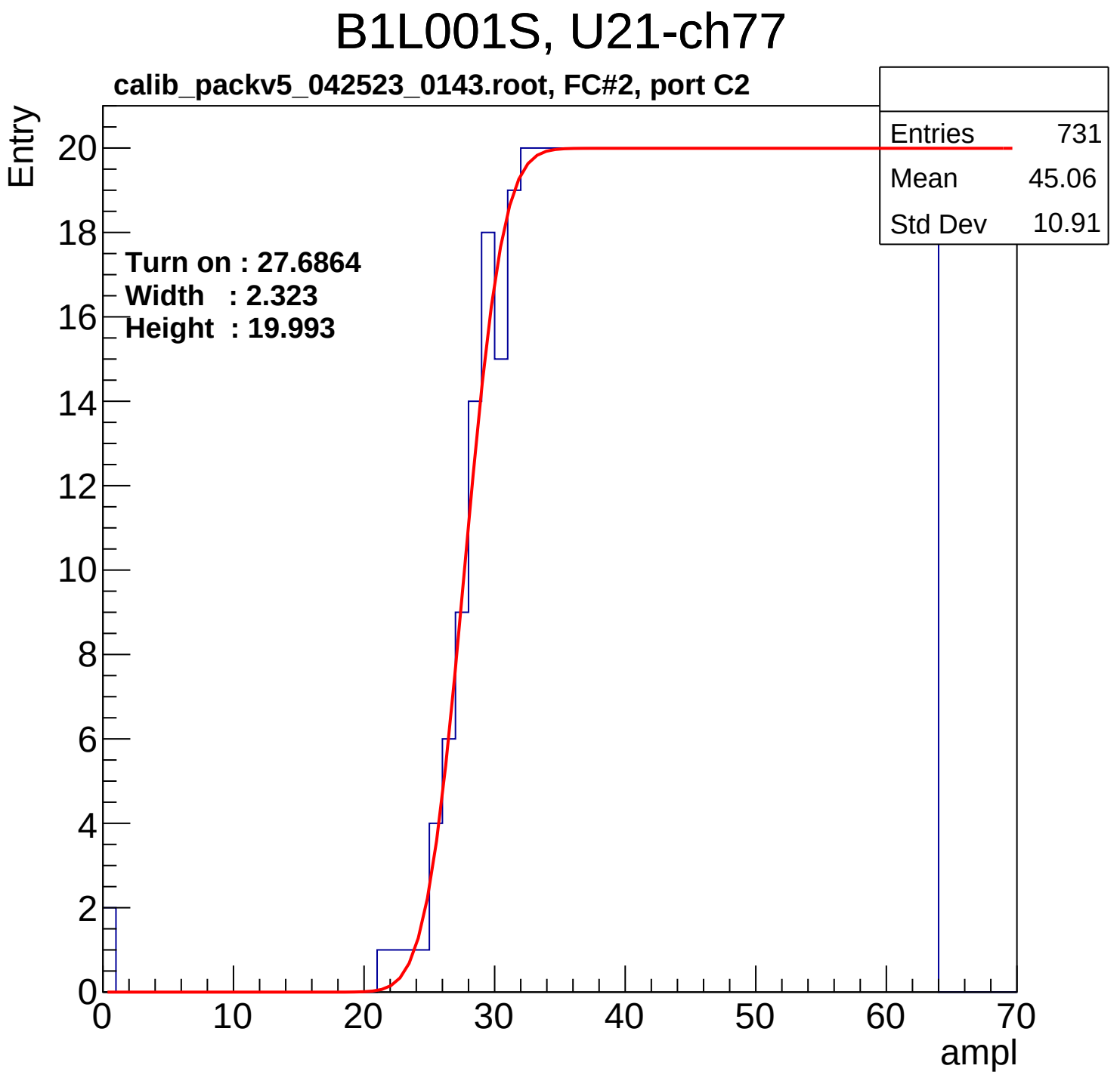
B1L001S, U21-ch77
calib_packv5_042523_0143.root, FC#2, port C2
Entries 731
Mean 45.06
Std Dev 10.91
Turn on : 27.6864
Width : 2.323
Height : 19.993
Entry
ampl
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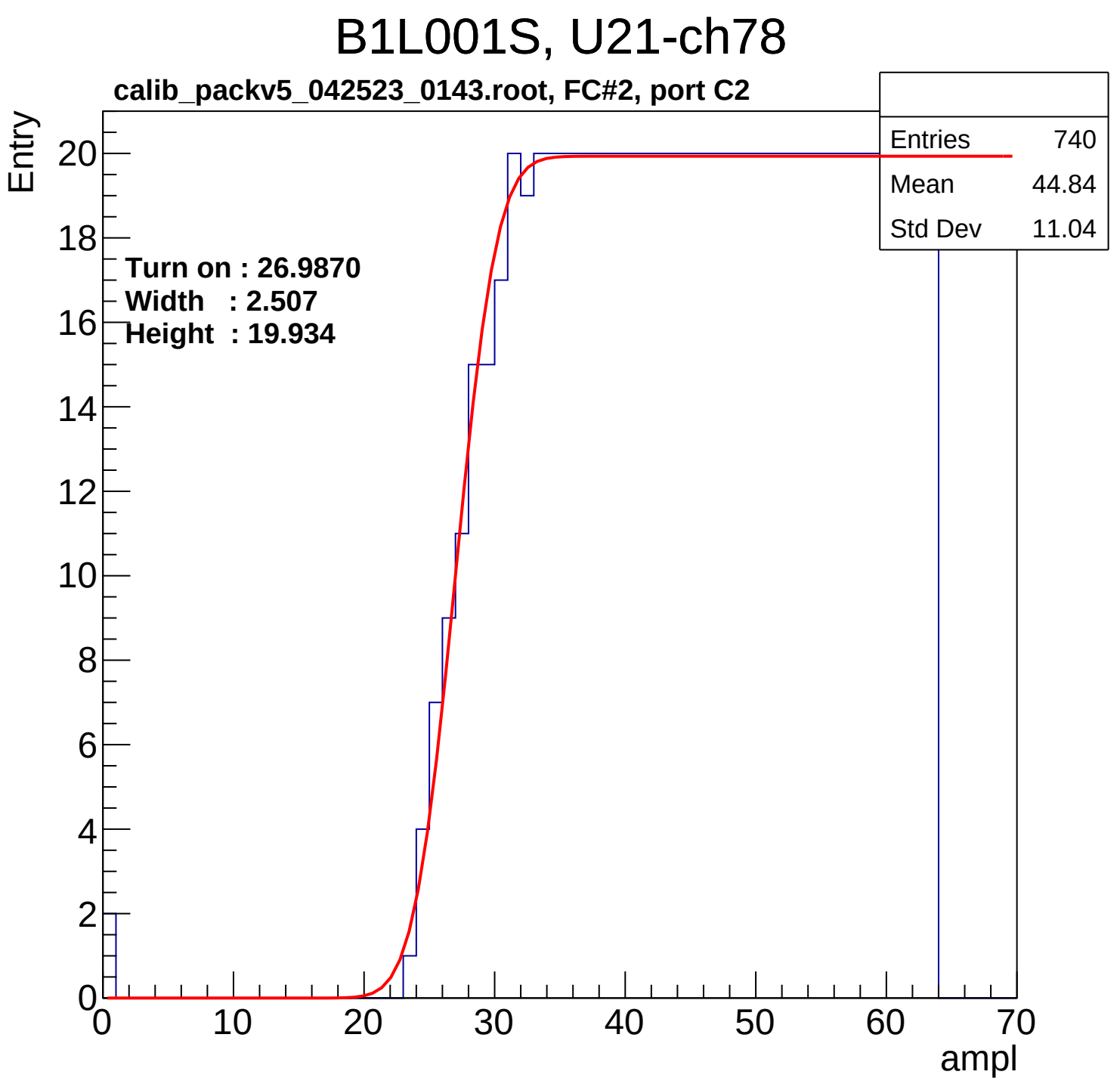
B1L001S, U21-ch78
calib_packv5_042523_0143.root, FC#2, port C2
Entries 740
Mean 44.84
Std Dev 11.04
Turn on : 26.9870
Width : 2.507
Height : 19.934
Entry
ampl
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6
8
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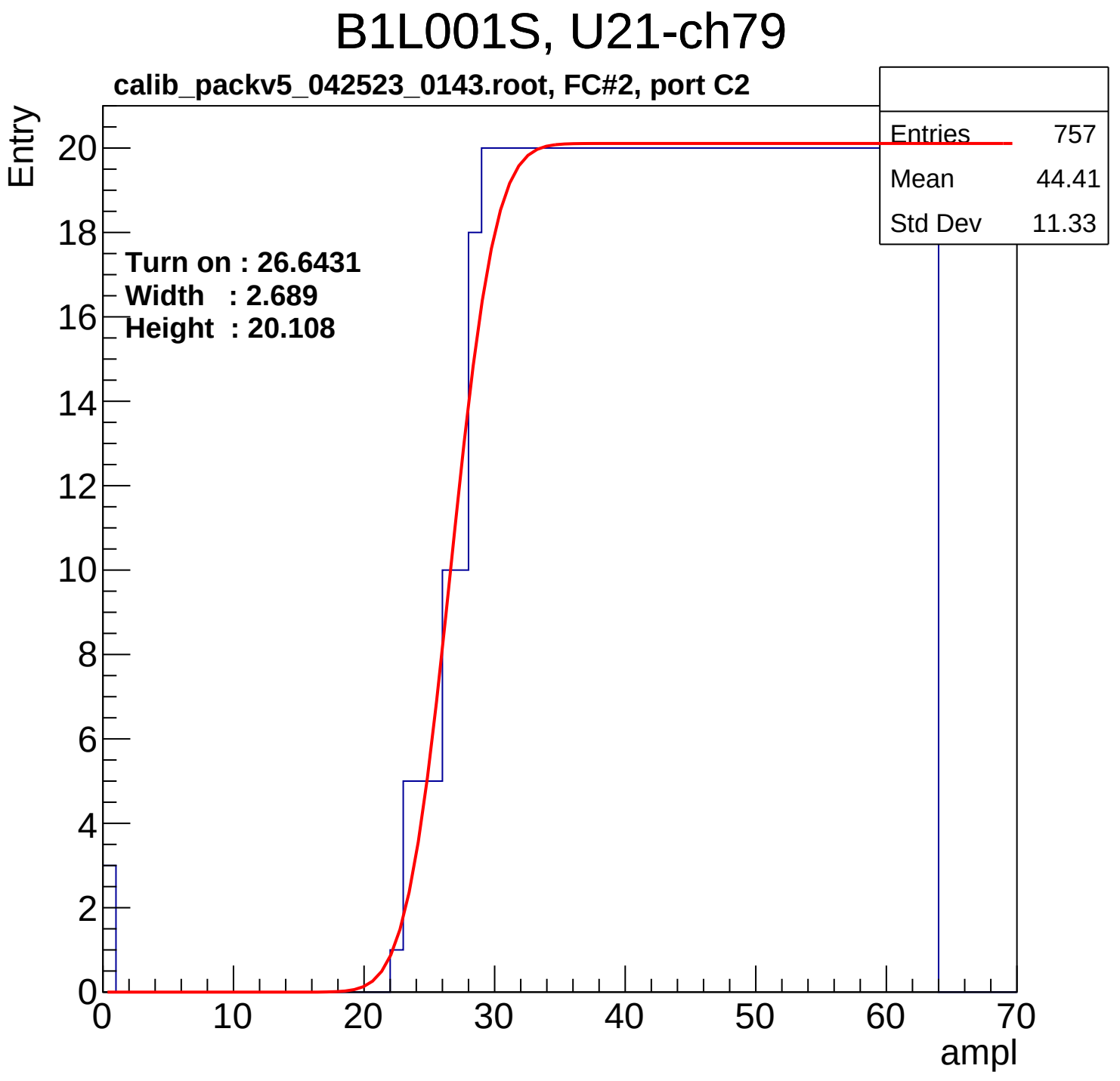
B1L001S, U21-ch79
calib_packv5_042523_0143.root, FC#2, port C2
Entries 757
Mean 44.41
Std Dev 11.33
Turn on : 26.6431
Width : 2.689
Height : 20.108
Entry
ampl
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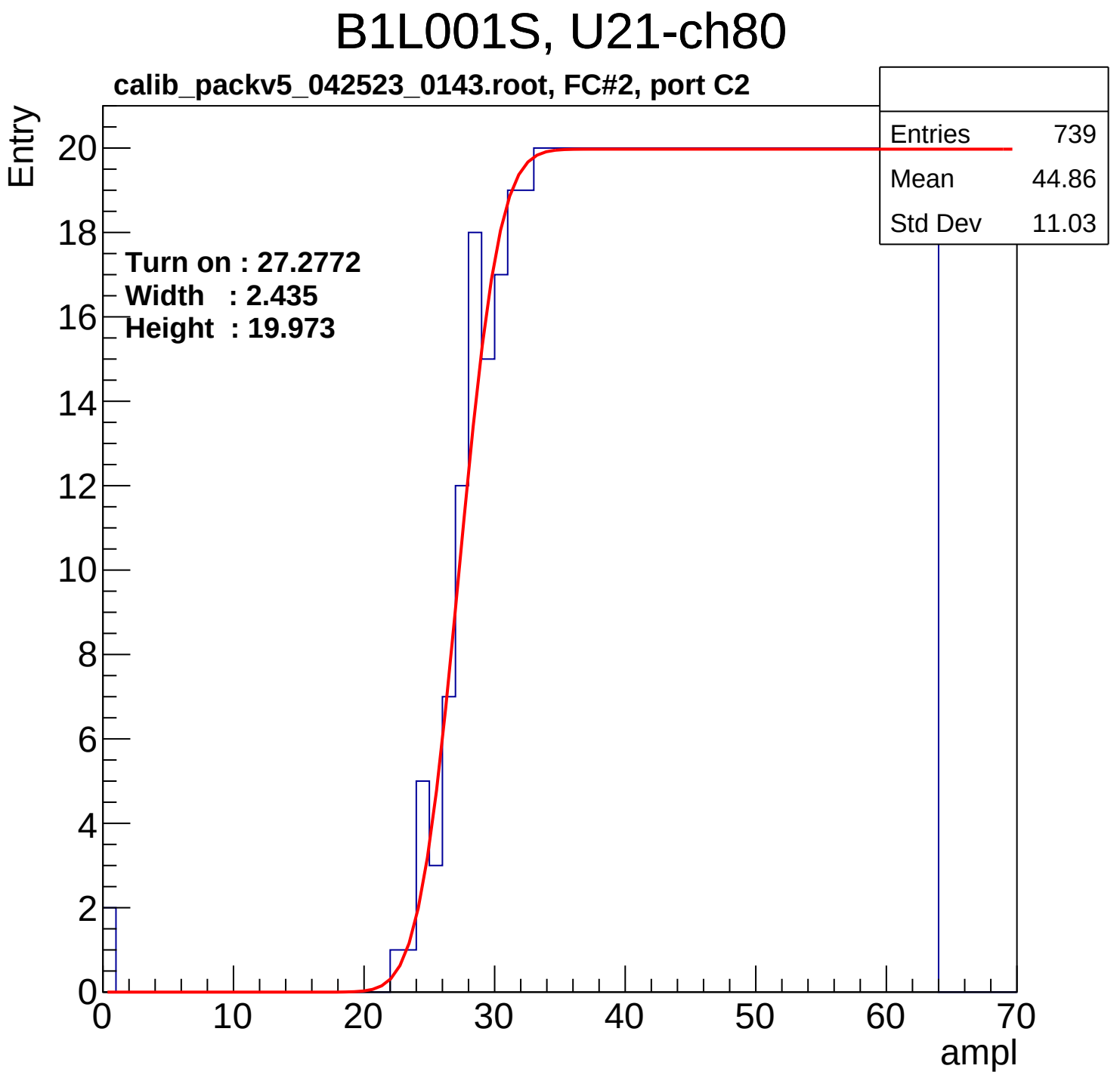
B1L001S, U21-ch80
calib_packv5_042523_0143.root, FC#2, port C2
Entries 739
Mean 44.86
Std Dev 11.03
Turn on : 27.2772
Width : 2.435
Height : 19.973
Entry
ampl
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6
8
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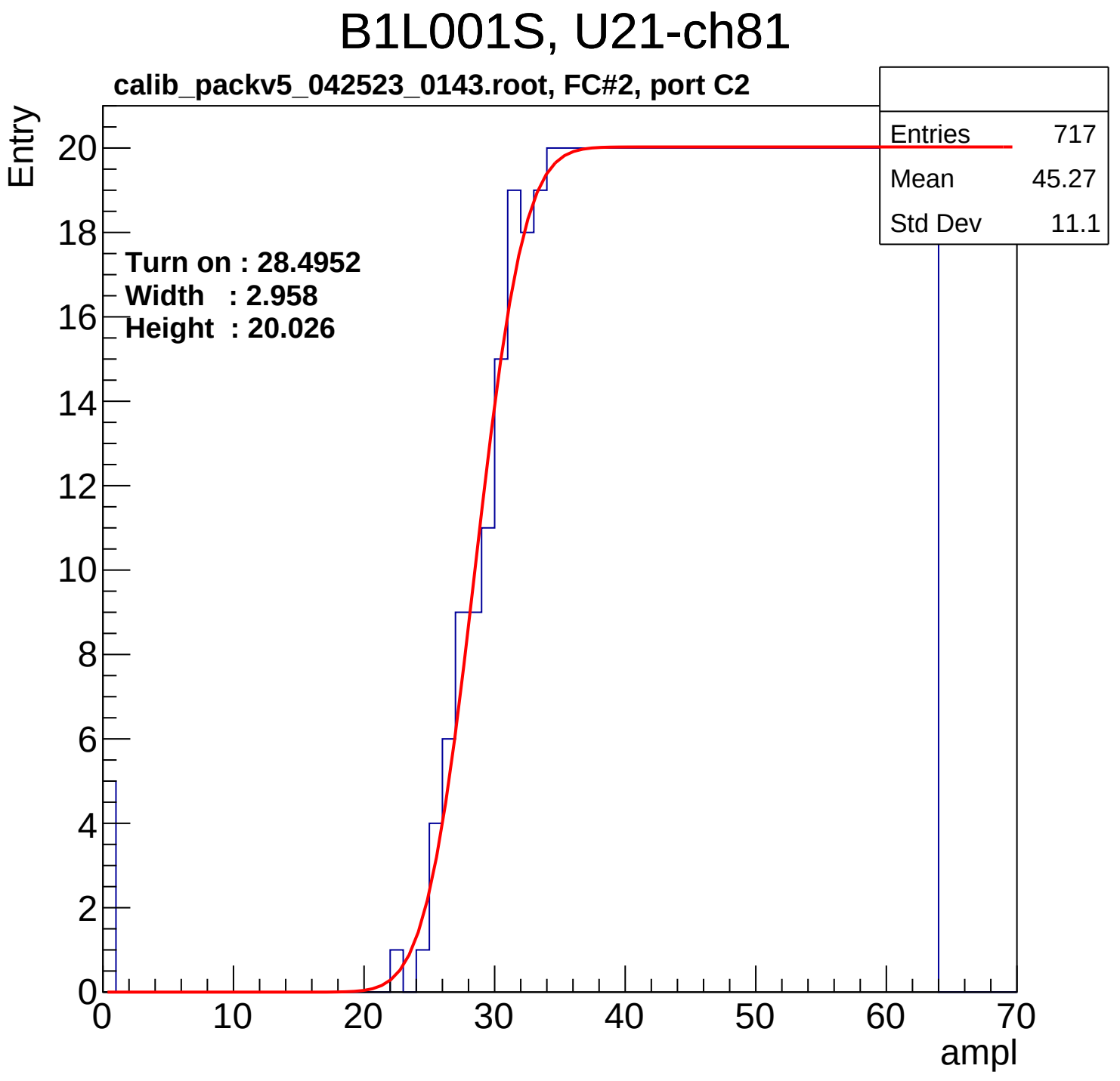
B1L001S, U21-ch81
calib_packv5_042523_0143.root, FC#2, port C2
Entries 717
Mean 45.27
Std Dev 11.1
Turn on : 28.4952
Width : 2.958
Height : 20.026
Entry
ampl
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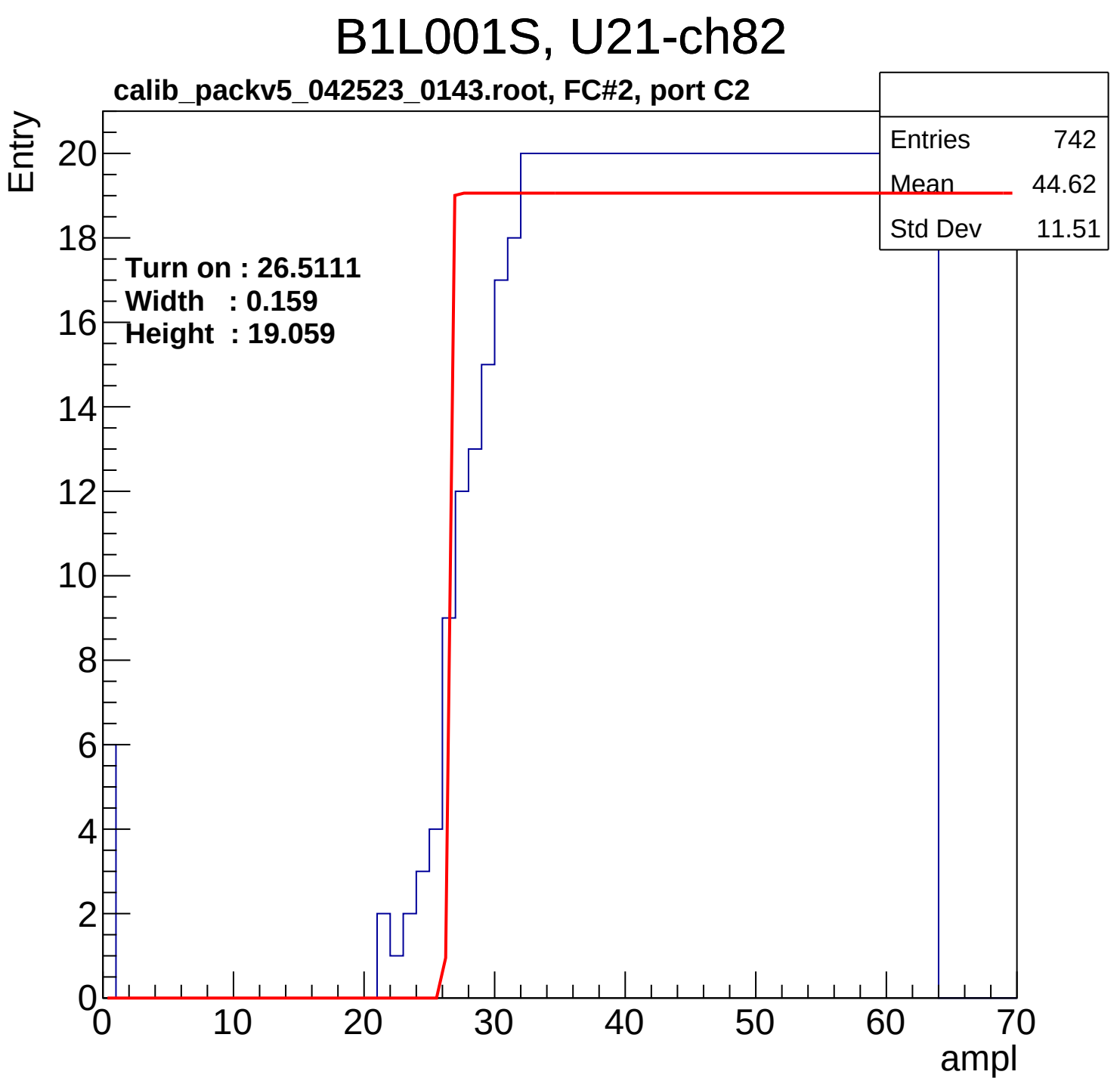
B1L001S, U21-ch82
calib_packv5_042523_0143.root, FC#2, port C2
Entries 742
Mean 44.62
Std Dev 11.51
Turn on : 26.5111
Width : 0.159
Height : 19.059
Entry
ampl
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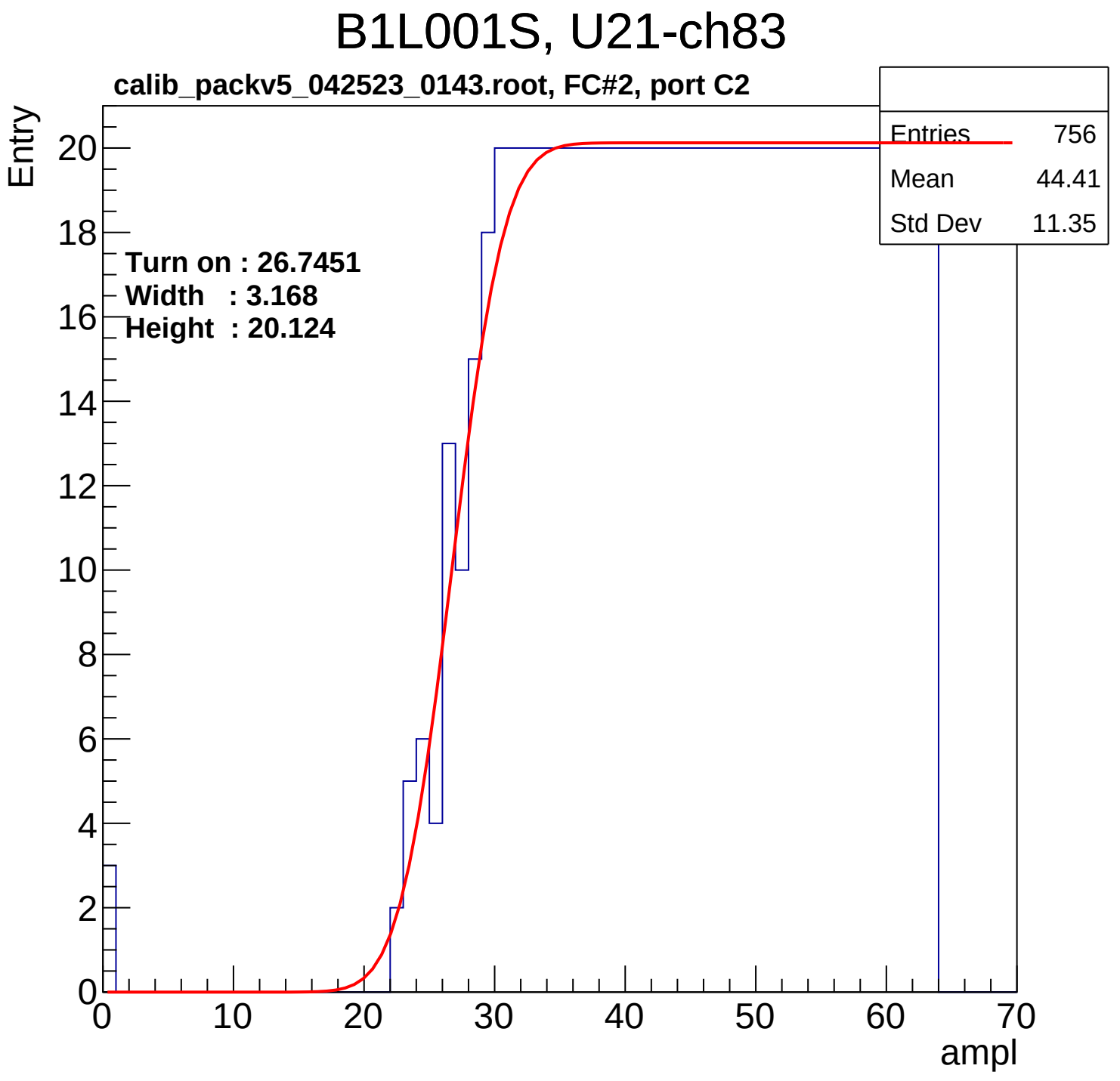
B1L001S, U21-ch83
calib_packv5_042523_0143.root, FC#2, port C2
Entries 756
Mean 44.41
Std Dev 11.35
Turn on : 26.7451
Width : 3.168
Height : 20.124
Entry
ampl
0
2
4
6
8
10
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18
20
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10
20
30
40
50
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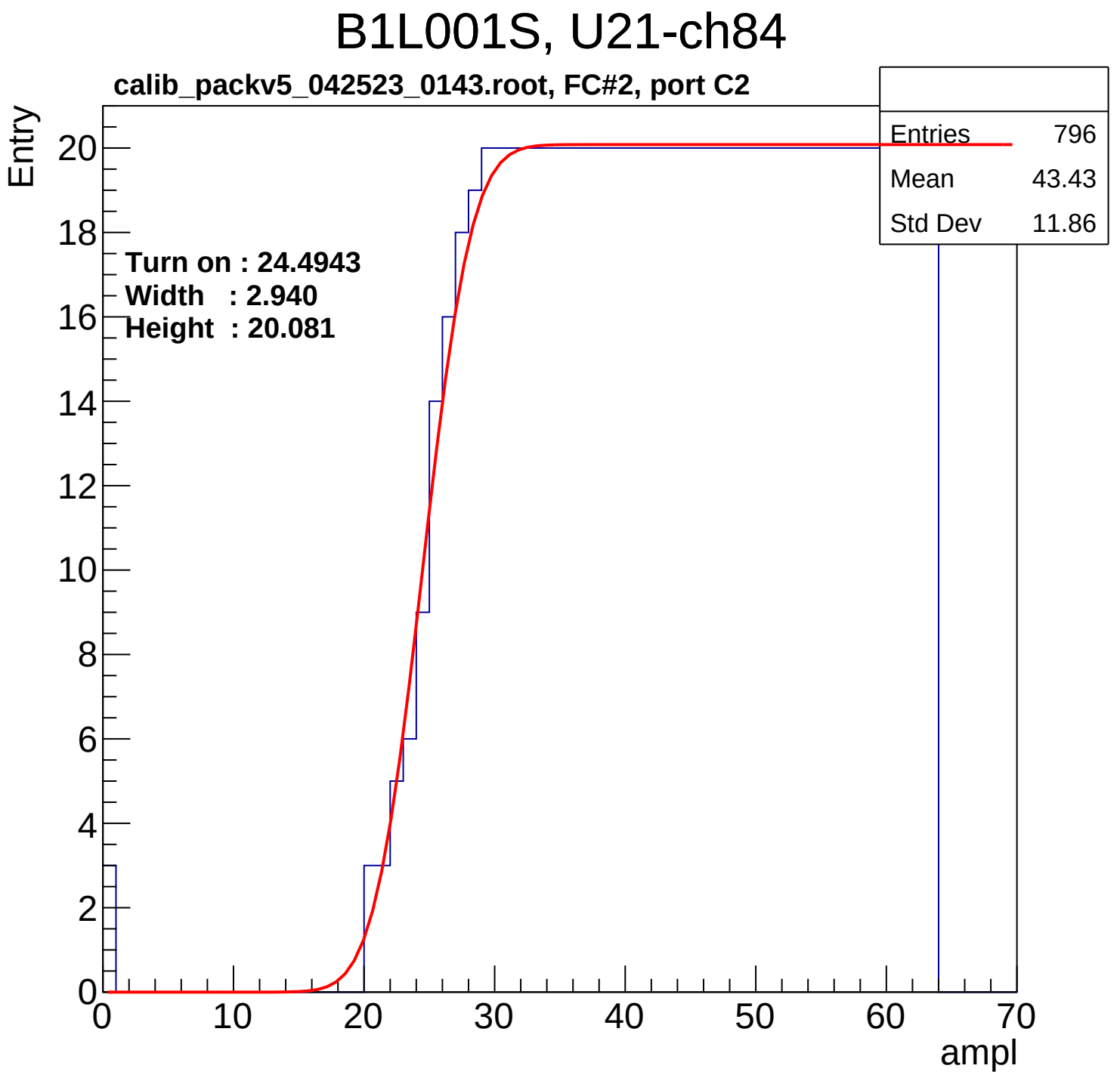
B1L001S, U21-ch84
calib_packv5_042523_0143.root, FC#2, port C2
Entries 796
Mean 43.43
Std Dev 11.86
Turn on : 24.4943
Width : 2.940
Height : 20.081
Entry
ampl
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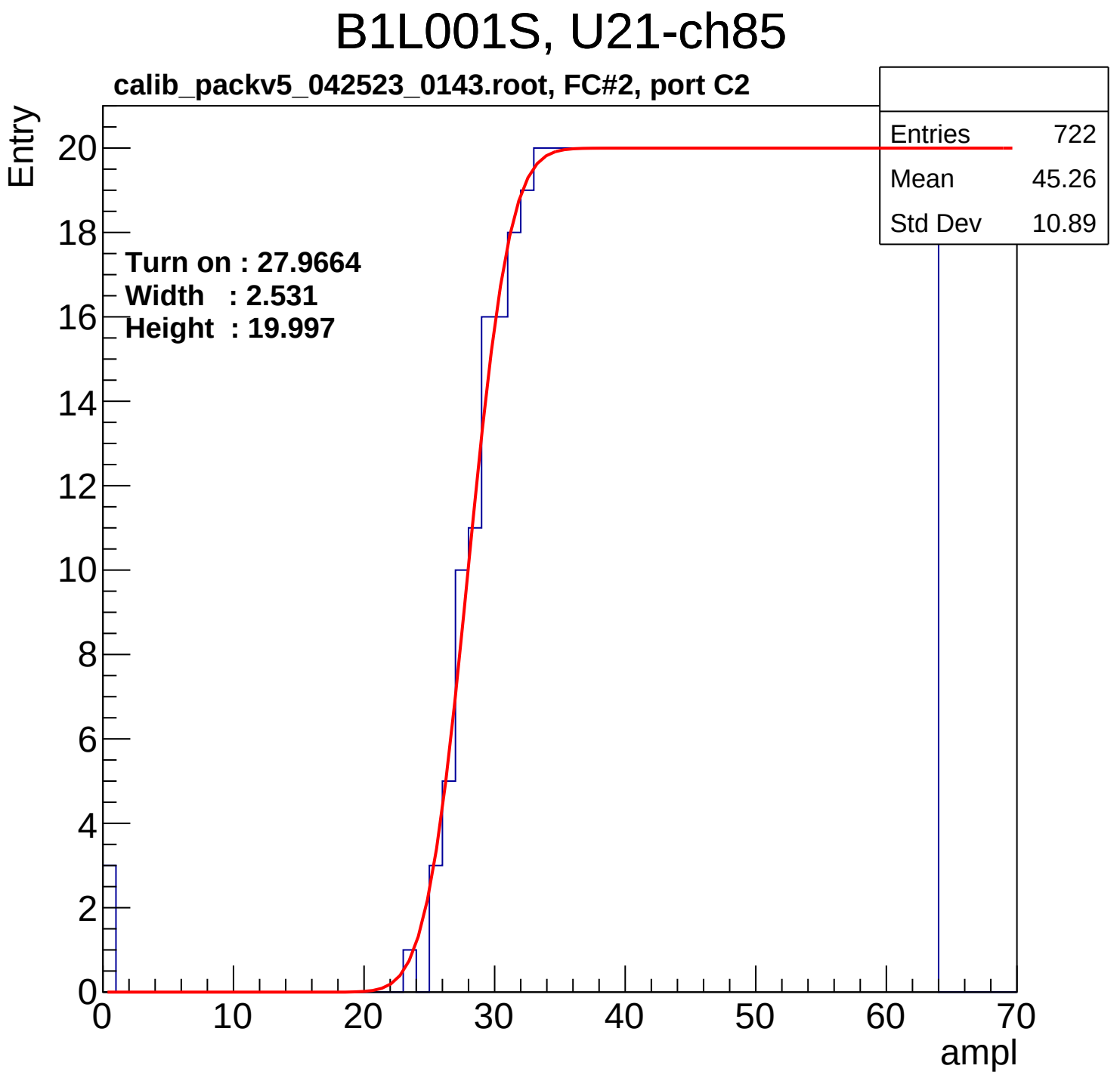
B1L001S, U21-ch85
calib_packv5_042523_0143.root, FC#2, port C2
Entries 722
Mean 45.26
Std Dev 10.89
Turn on : 27.9664
Width : 2.531
Height : 19.997
Entry
ampl
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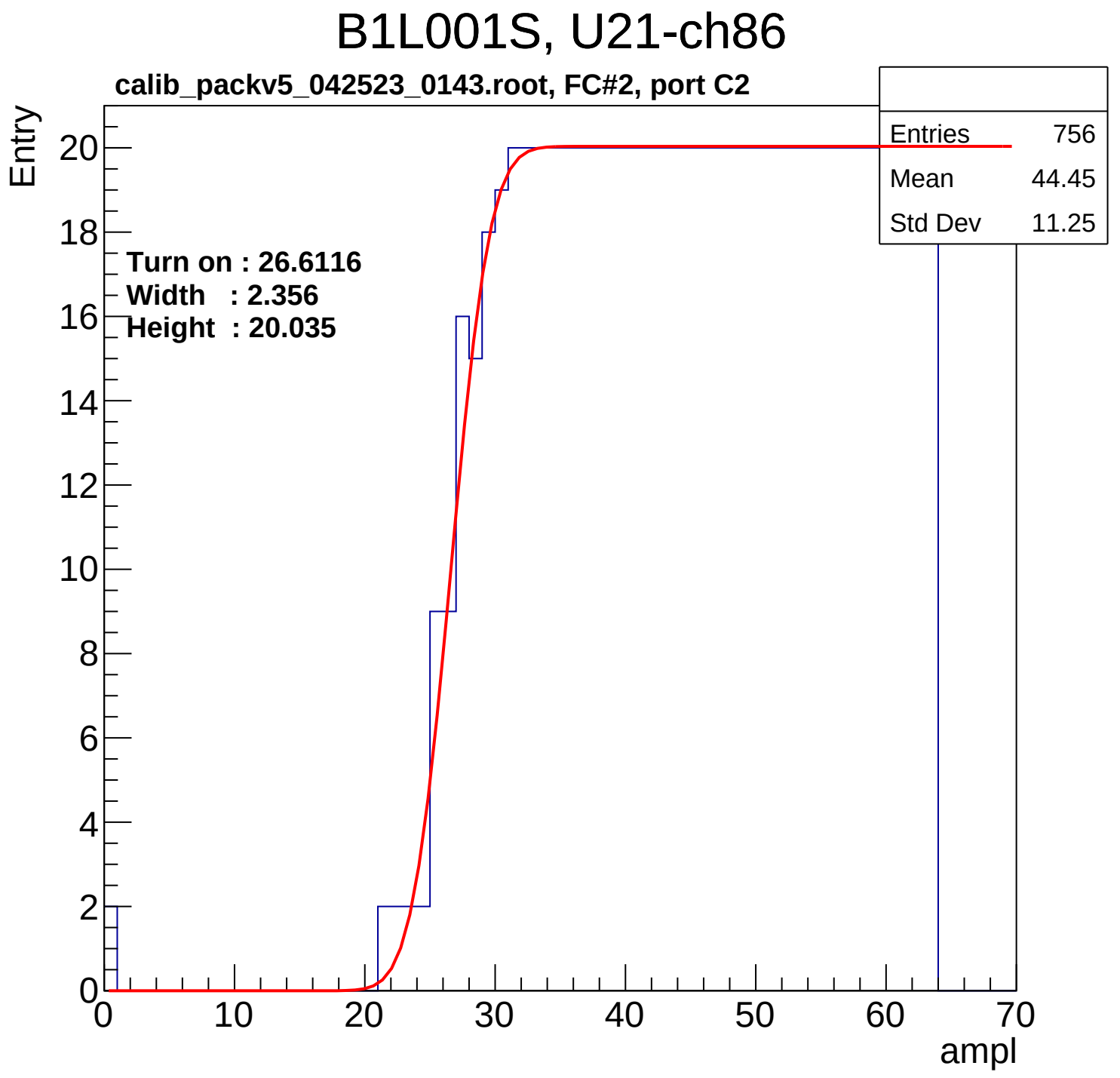
B1L001S, U21-ch86
calib_packv5_042523_0143.root, FC#2, port C2
Entries 756
Mean 44.45
Std Dev 11.25
Turn on : 26.6116
Width : 2.356
Height : 20.035
Entry
ampl
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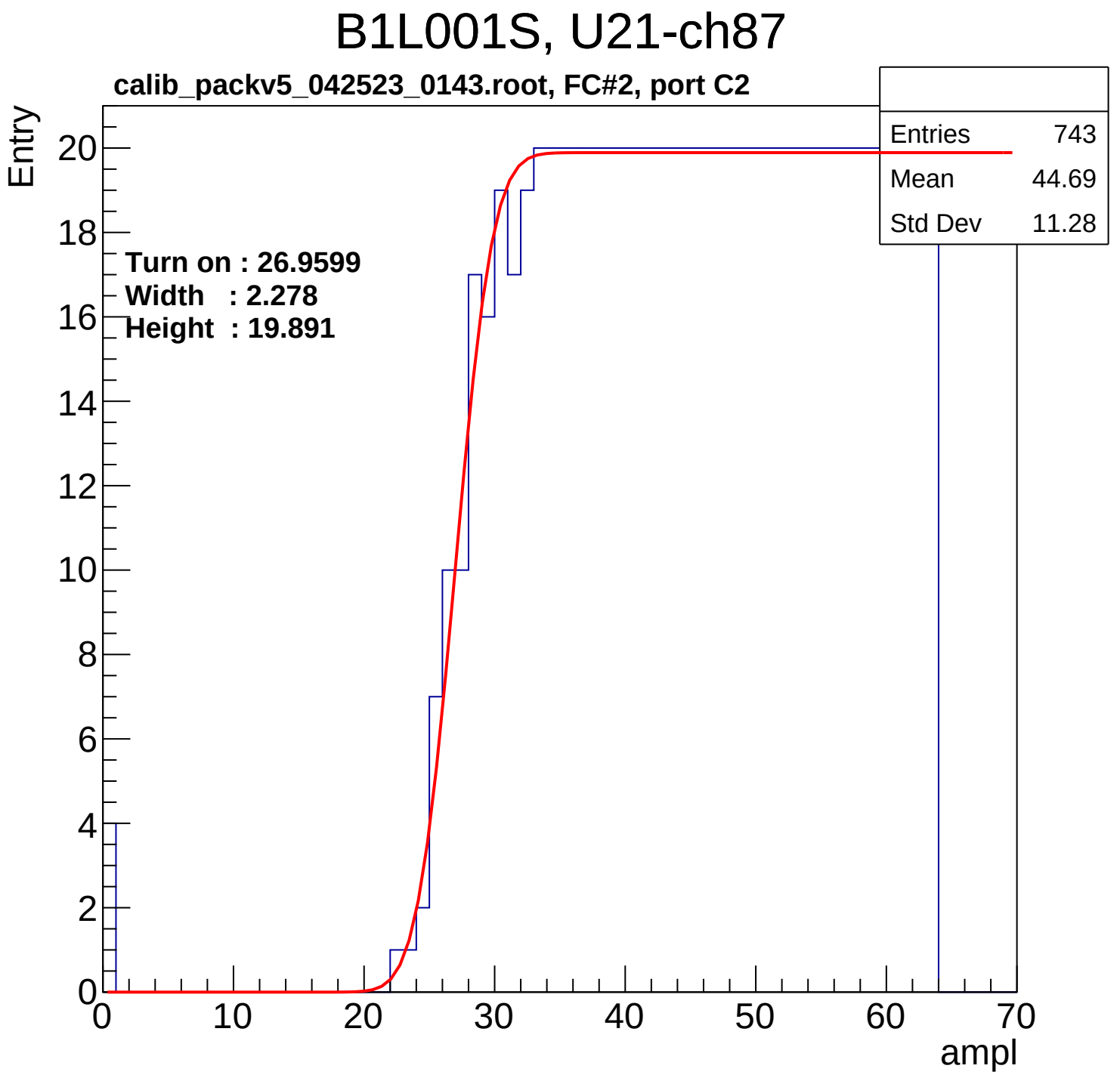
B1L001S, U21-ch87
calib_packv5_042523_0143.root, FC#2, port C2
Entries 743
Mean 44.69
Std Dev 11.28
Turn on : 26.9599
Width : 2.278
Height : 19.891
Entry
ampl
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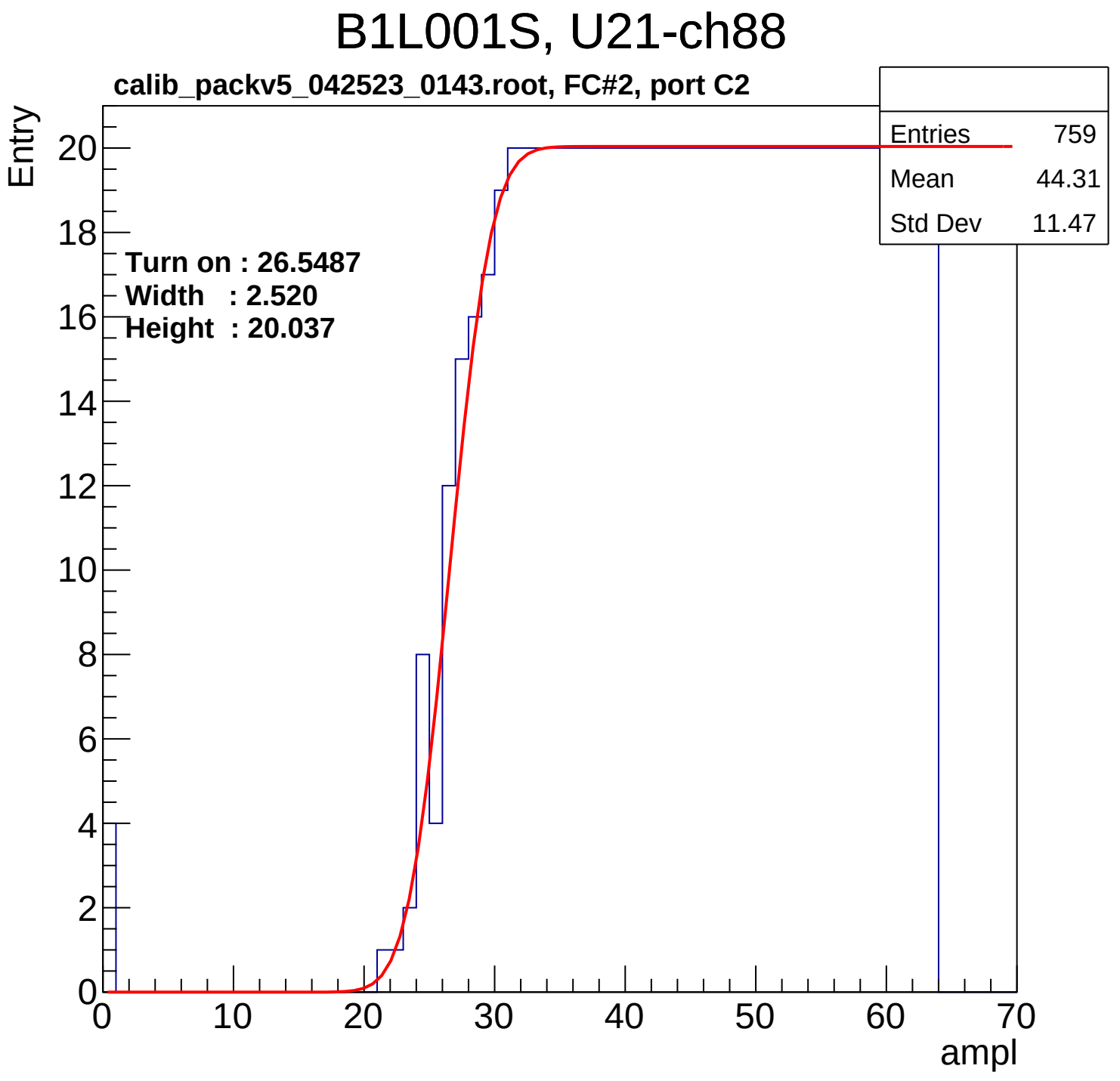
B1L001S, U21-ch88
calib_packv5_042523_0143.root, FC#2, port C2
Entries 759
Mean 44.31
Std Dev 11.47
Turn on : 26.5487
Width : 2.520
Height : 20.037
Entry
ampl
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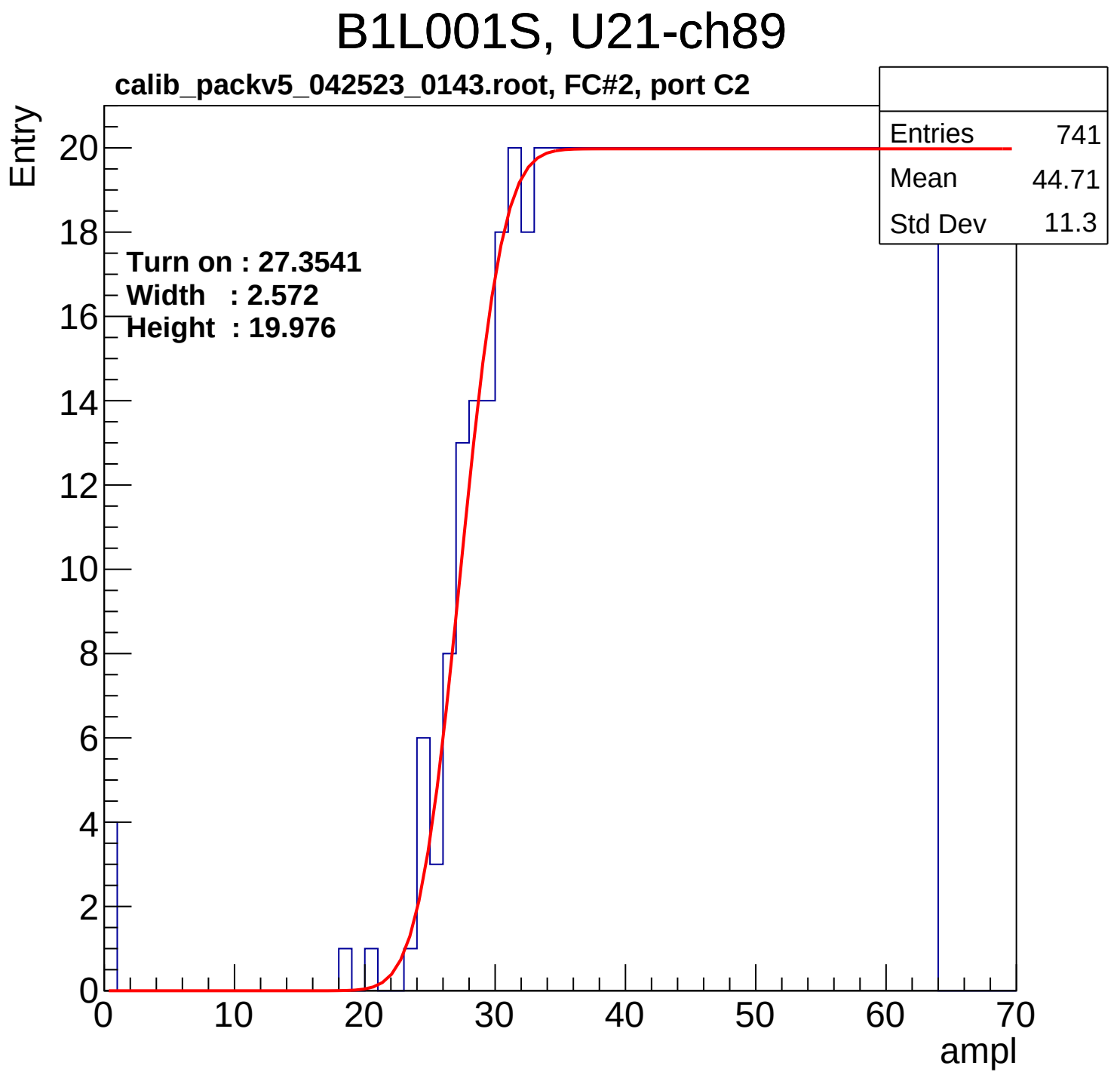
B1L001S, U21-ch89
calib_packv5_042523_0143.root, FC#2, port C2
Entries 741
Mean 44.71
Std Dev 11.3
Turn on : 27.3541
Width : 2.572
Height : 19.976
Entry
ampl
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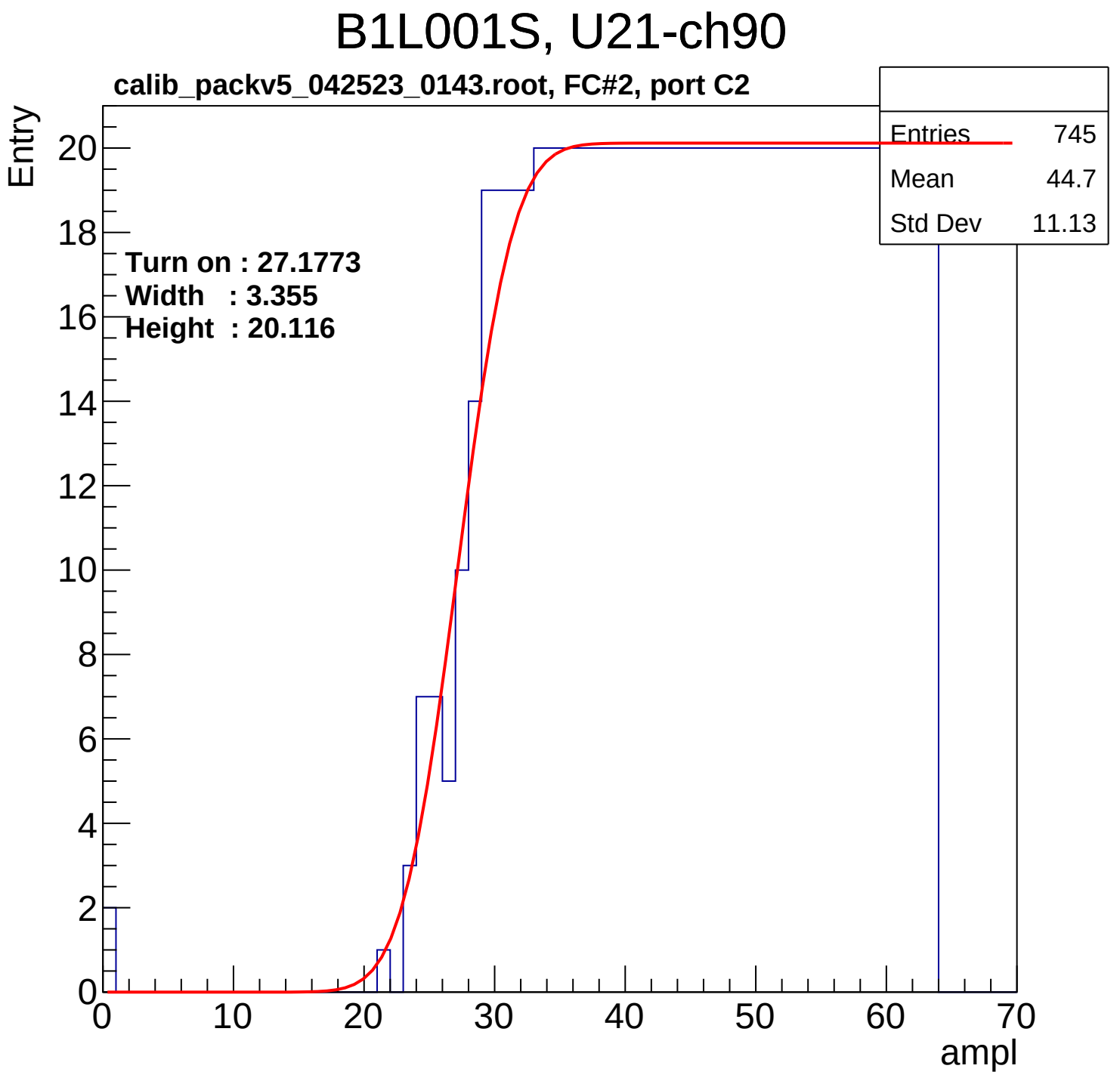
B1L001S, U21-ch90
calib_packv5_042523_0143.root, FC#2, port C2
Entries 745
Mean 44.7
Std Dev 11.13
Turn on : 27.1773
Width : 3.355
Height : 20.116
Entry
ampl
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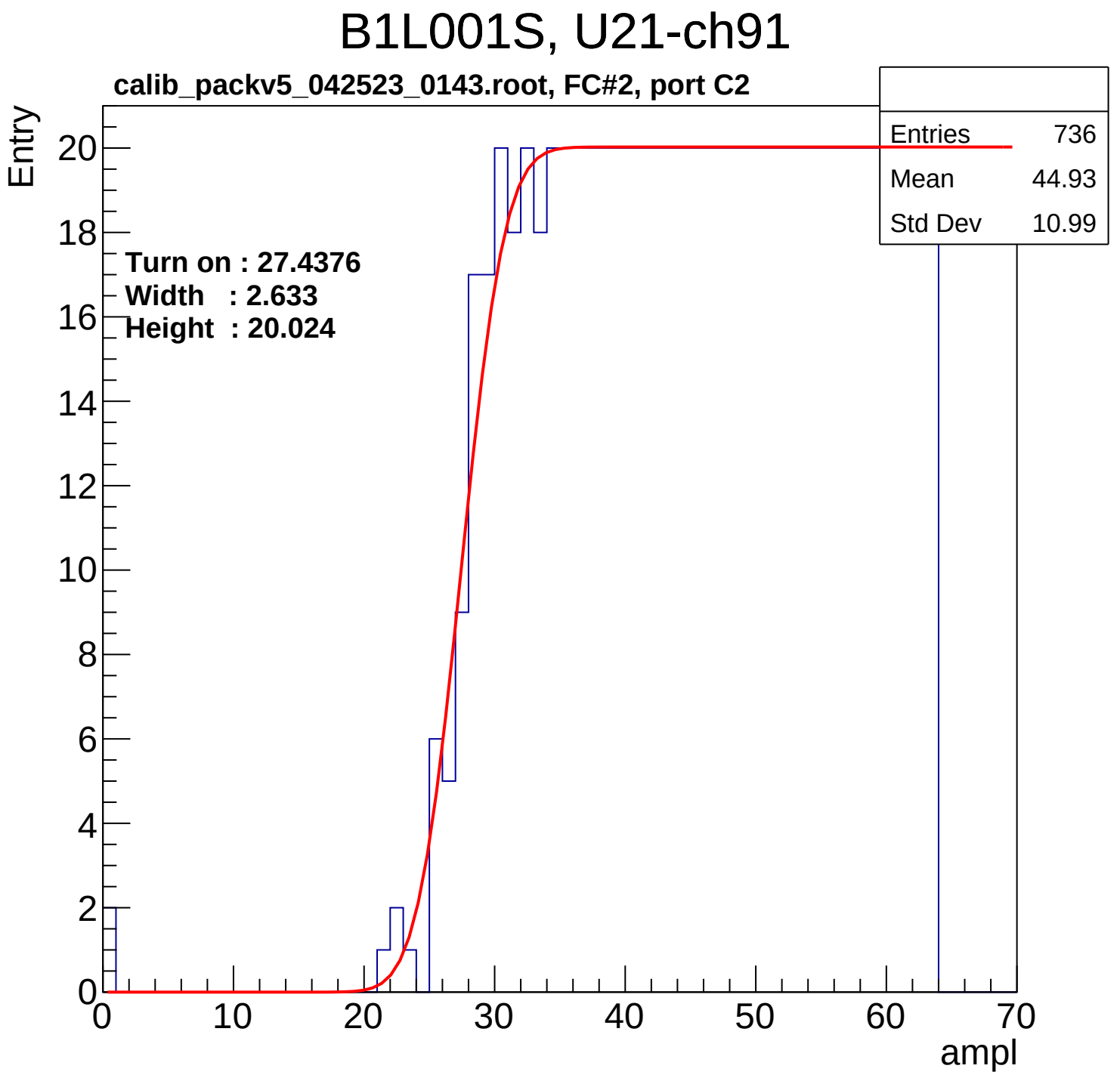
B1L001S, U21-ch91
calib_packv5_042523_0143.root, FC#2, port C2
Entries 736
Mean 44.93
Std Dev 10.99
Turn on : 27.4376
Width : 2.633
Height : 20.024
Entry
ampl
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6
8
10
12
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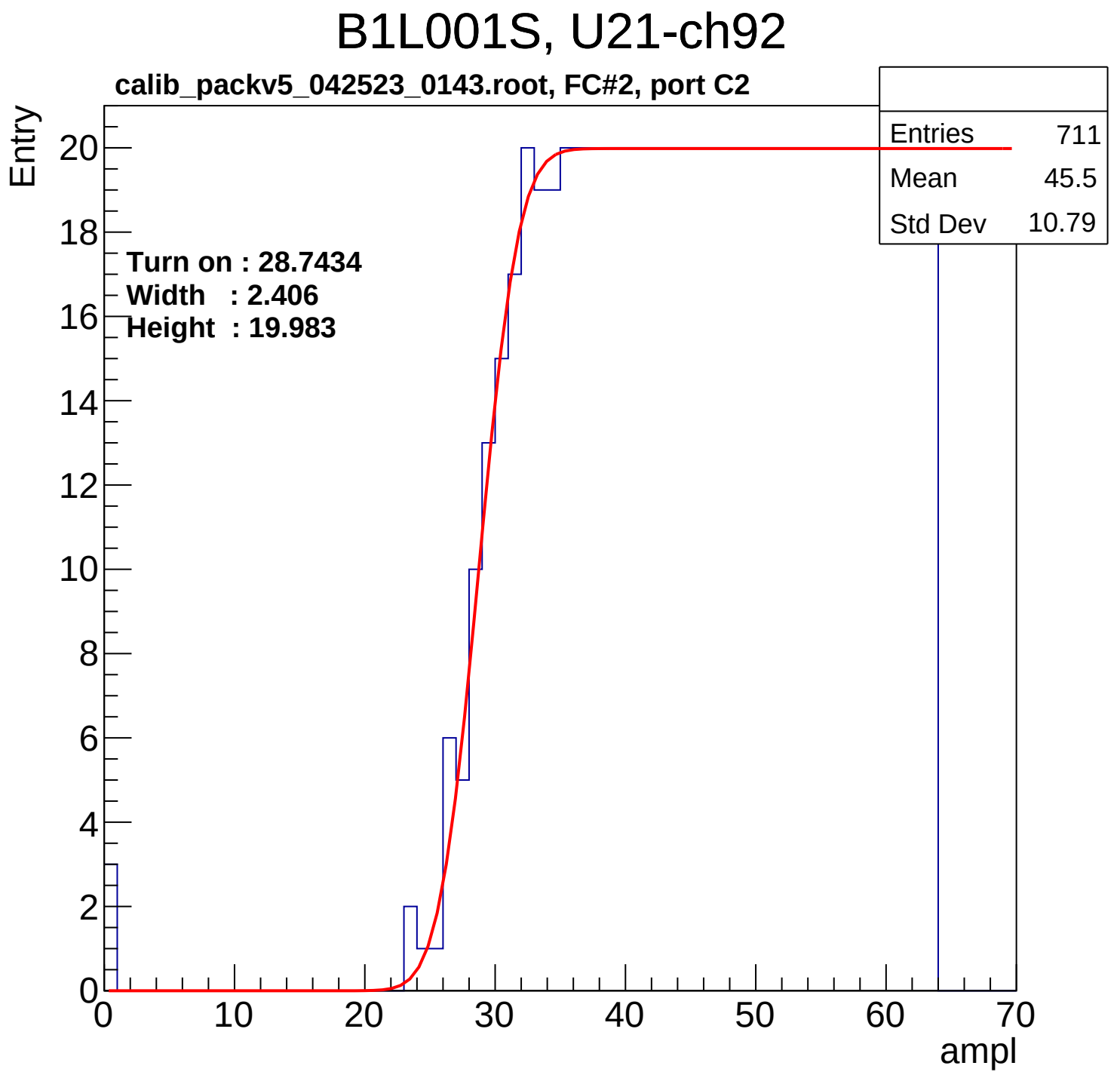
B1L001S, U21-ch92
calib_packv5_042523_0143.root, FC#2, port C2
Entries 711
Mean 45.5
Std Dev 10.79
Turn on : 28.7434
Width : 2.406
Height : 19.983
Entry
ampl
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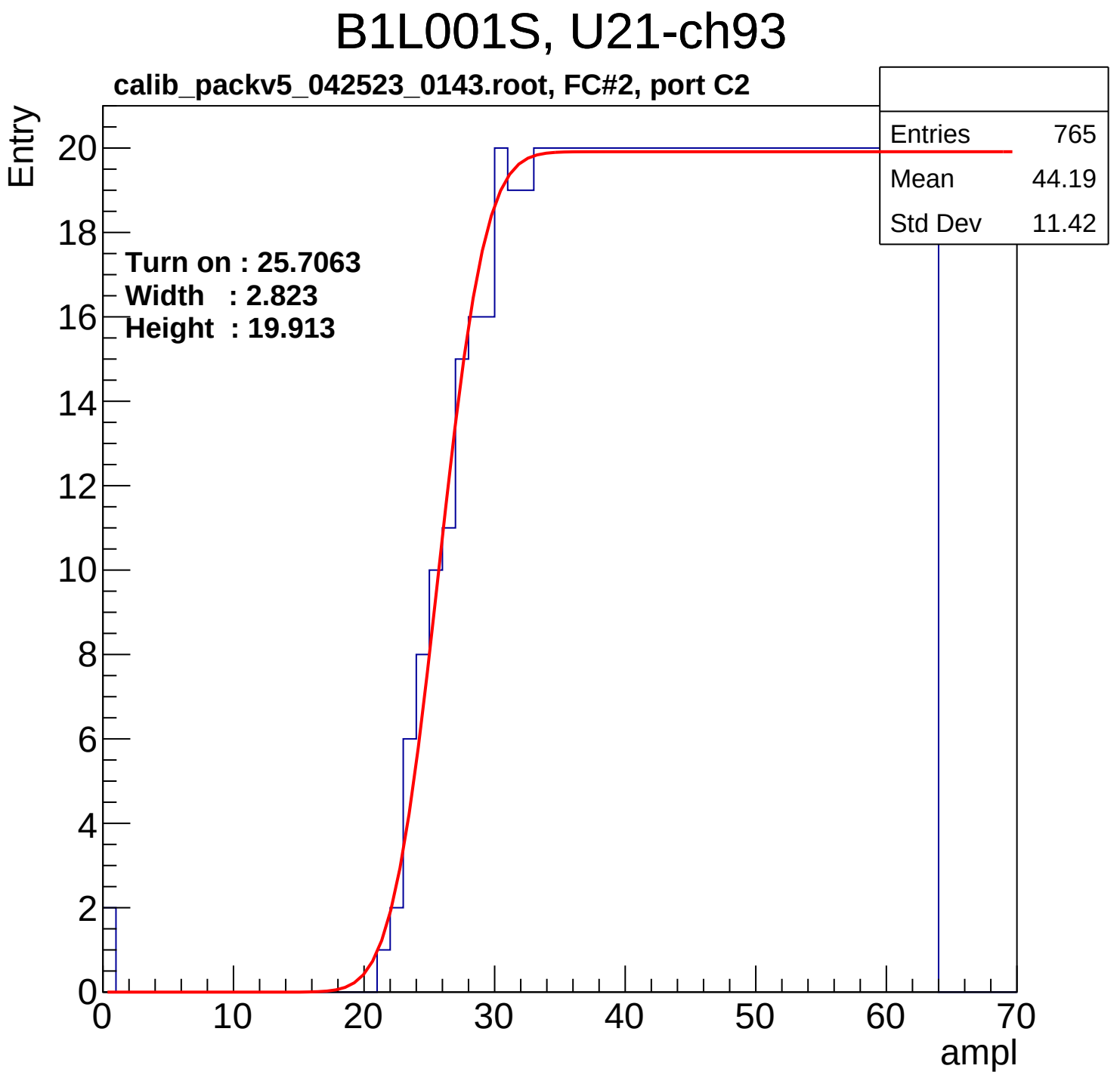
B1L001S, U21-ch93
calib_packv5_042523_0143.root, FC#2, port C2
Entries 765
Mean 44.19
Std Dev 11.42
Turn on : 25.7063
Width : 2.823
Height : 19.913
Entry
ampl
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6
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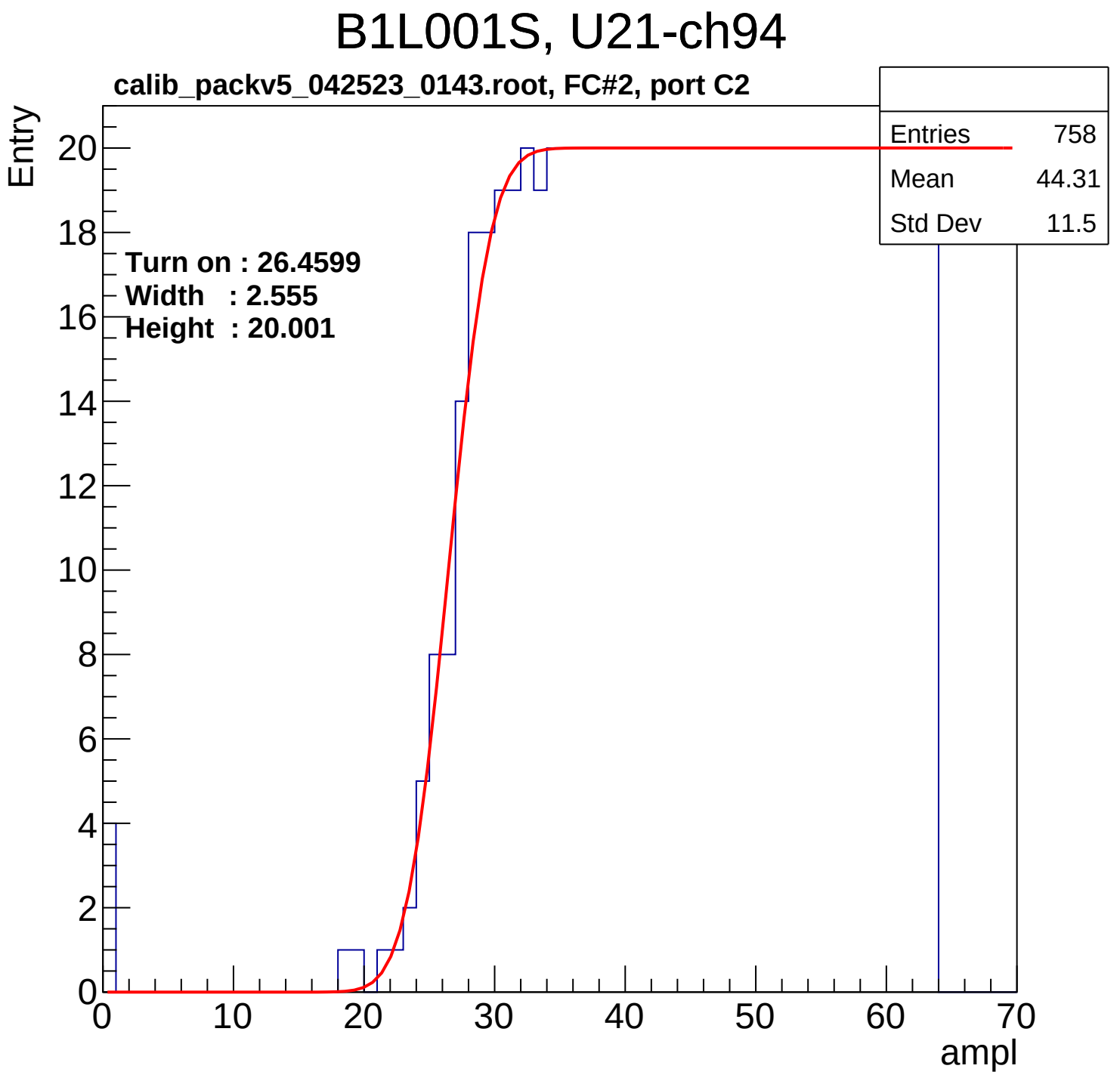
B1L001S, U21-ch94
calib_packv5_042523_0143.root, FC#2, port C2
Entries 758
Mean 44.31
Std Dev 11.5
Turn on : 26.4599
Width : 2.555
Height : 20.001
Entry
ampl
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6
8
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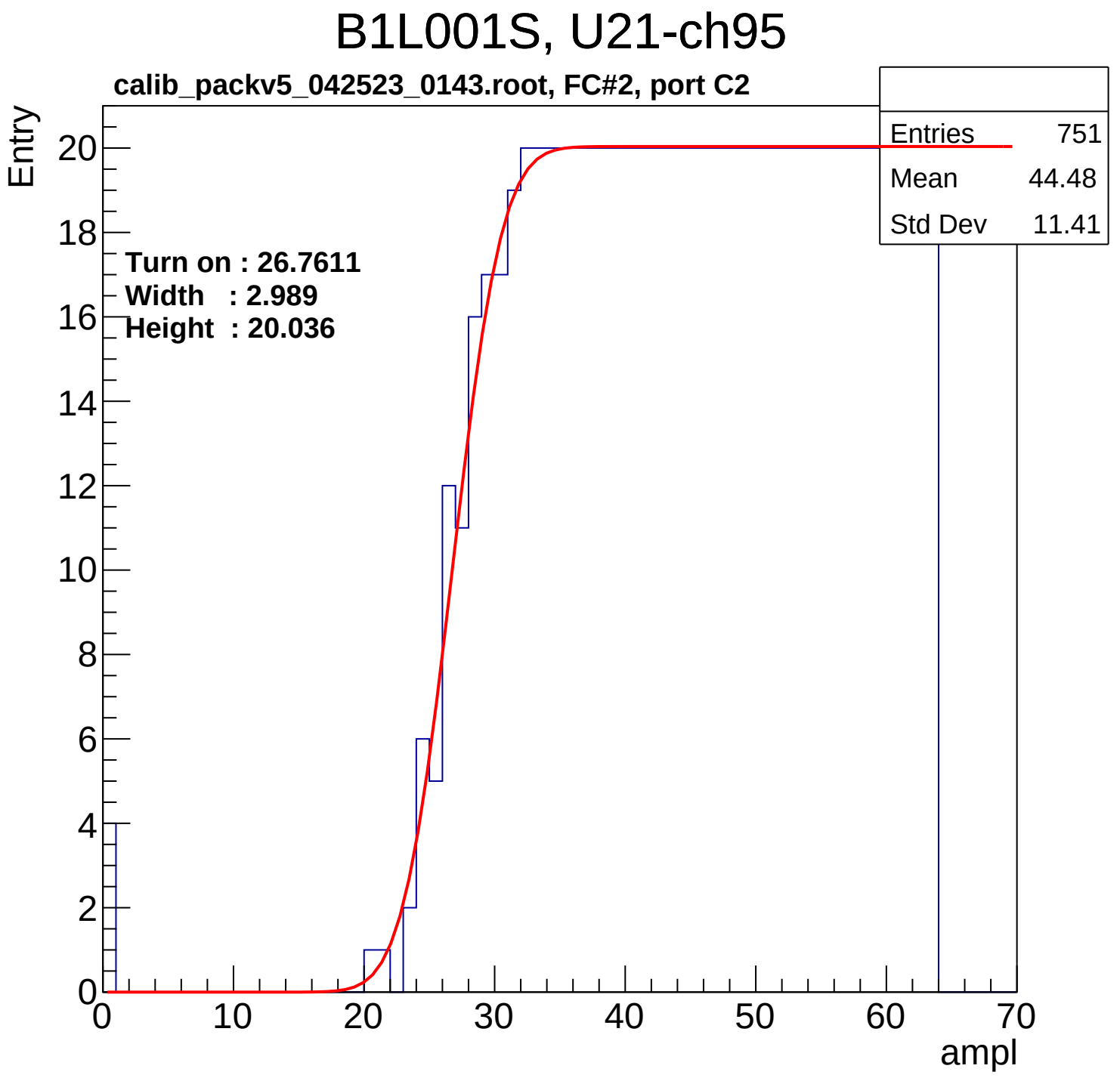
B1L001S, U21-ch95
calib_packv5_042523_0143.root, FC#2, port C2
Entries 751
Mean 44.48
Std Dev 11.41
Turn on : 26.7611
Width : 2.989
Height : 20.036
Entry
ampl
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8
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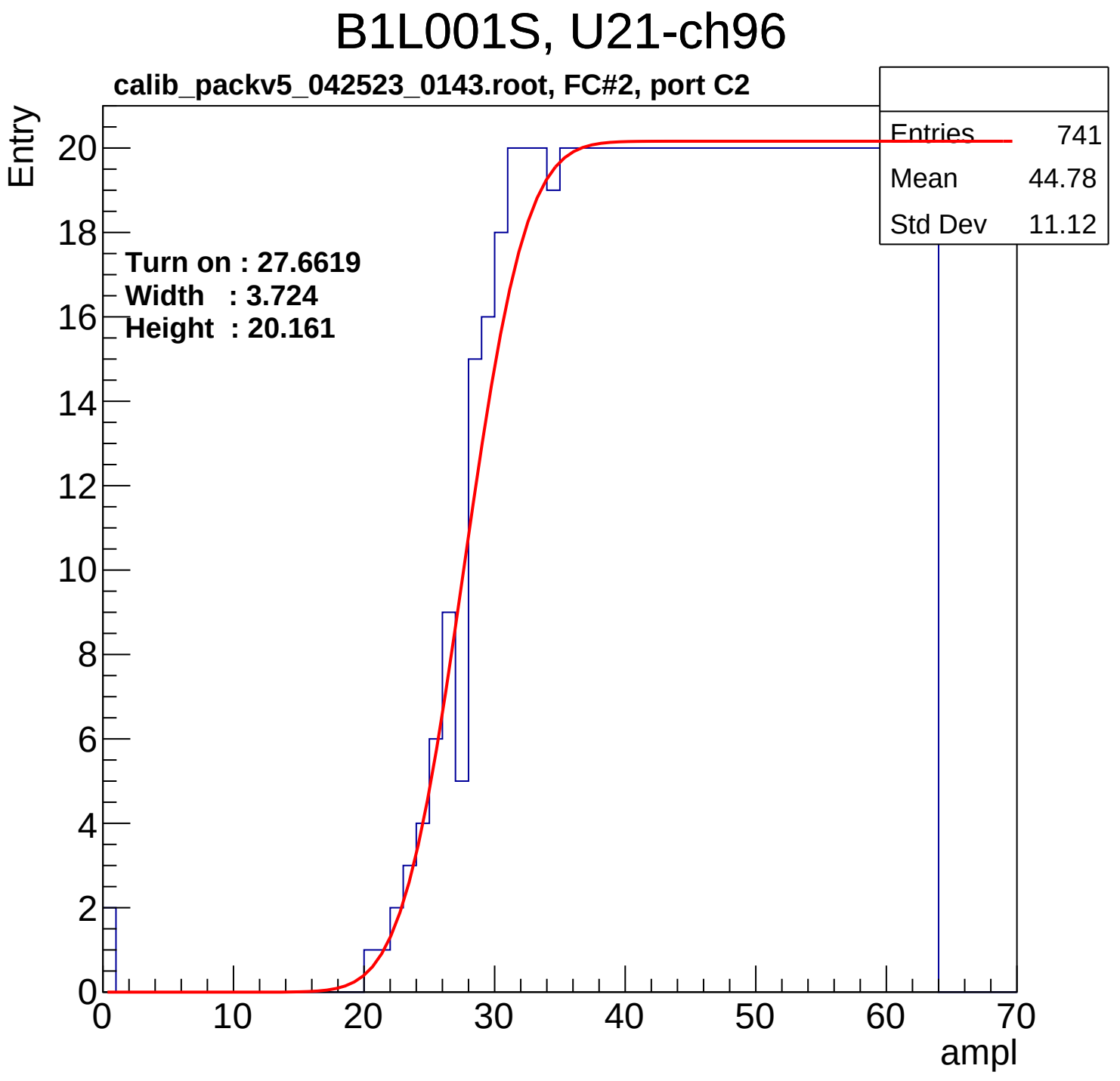
B1L001S, U21-ch96
calib_packv5_042523_0143.root, FC#2, port C2
Entries 741
Mean 44.78
Std Dev 11.12
Turn on : 27.6619
Width : 3.724
Height : 20.161
Entry
ampl
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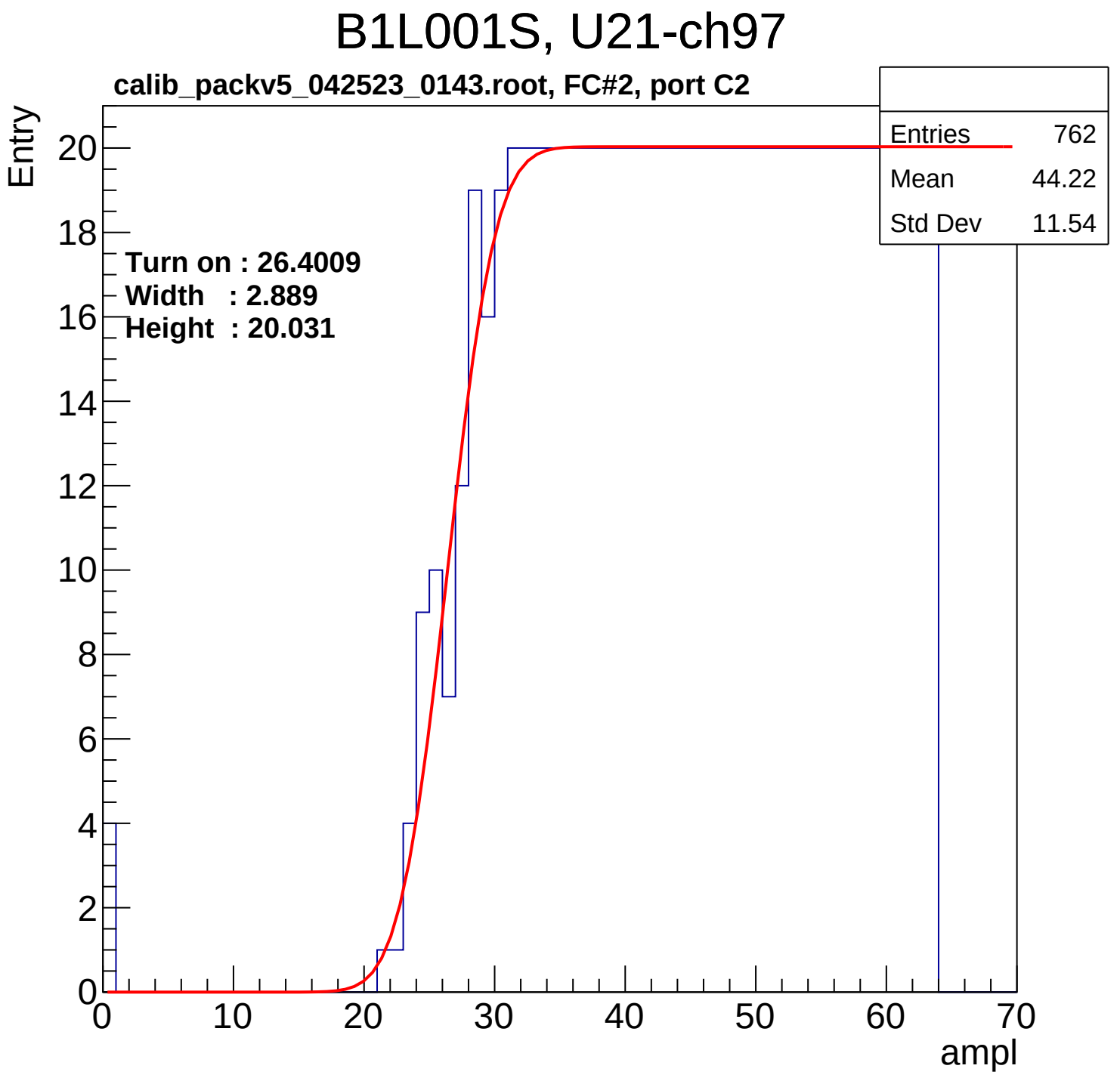
B1L001S, U21-ch97
calib_packv5_042523_0143.root, FC#2, port C2
Entries 762
Mean 44.22
Std Dev 11.54
Turn on : 26.4009
Width : 2.889
Height : 20.031
Entry
ampl
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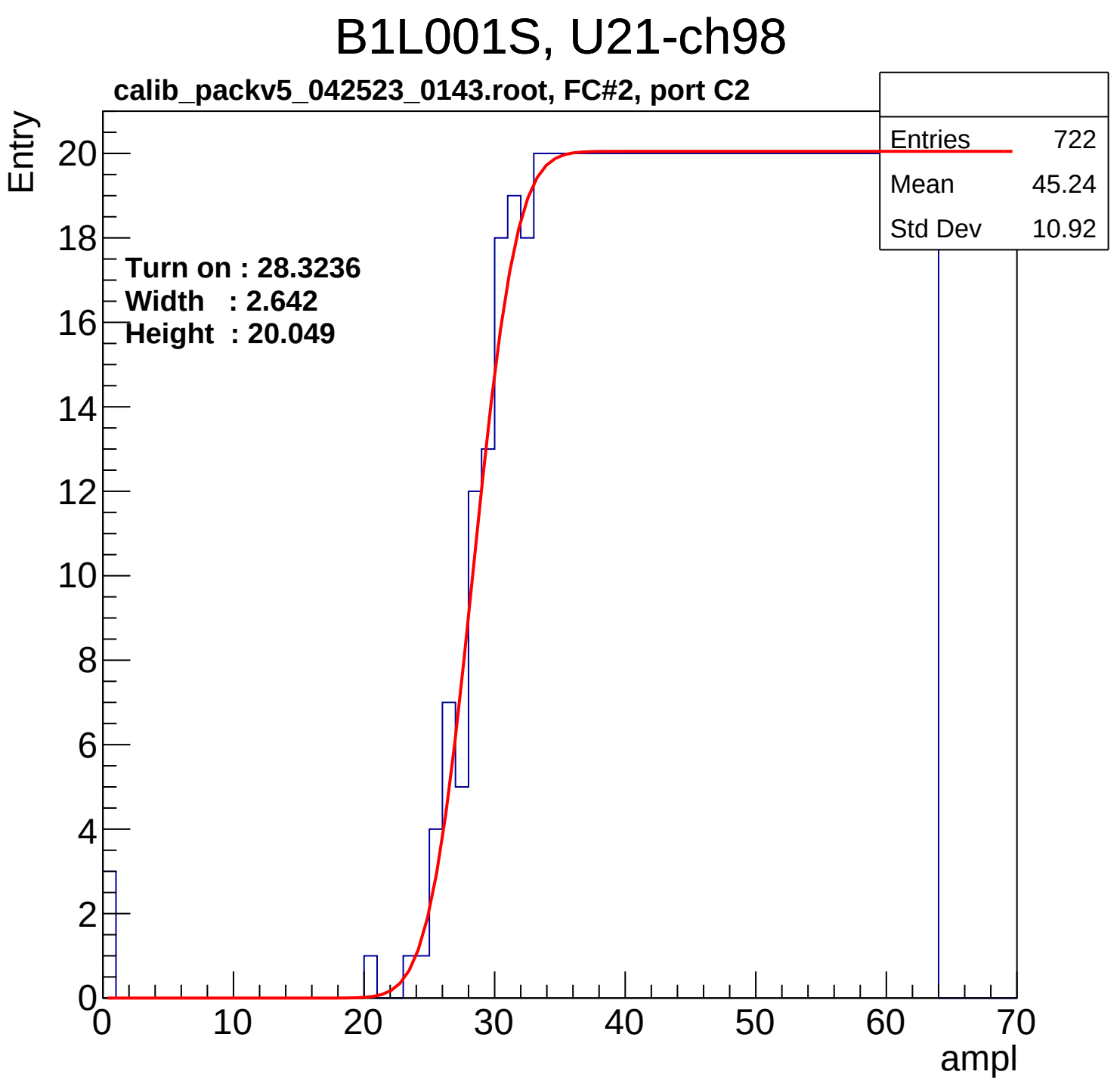
B1L001S, U21-ch98
calib_packv5_042523_0143.root, FC#2, port C2
Entries 722
Mean 45.24
Std Dev 10.92
Turn on : 28.3236
Width : 2.642
Height : 20.049
Entry
ampl
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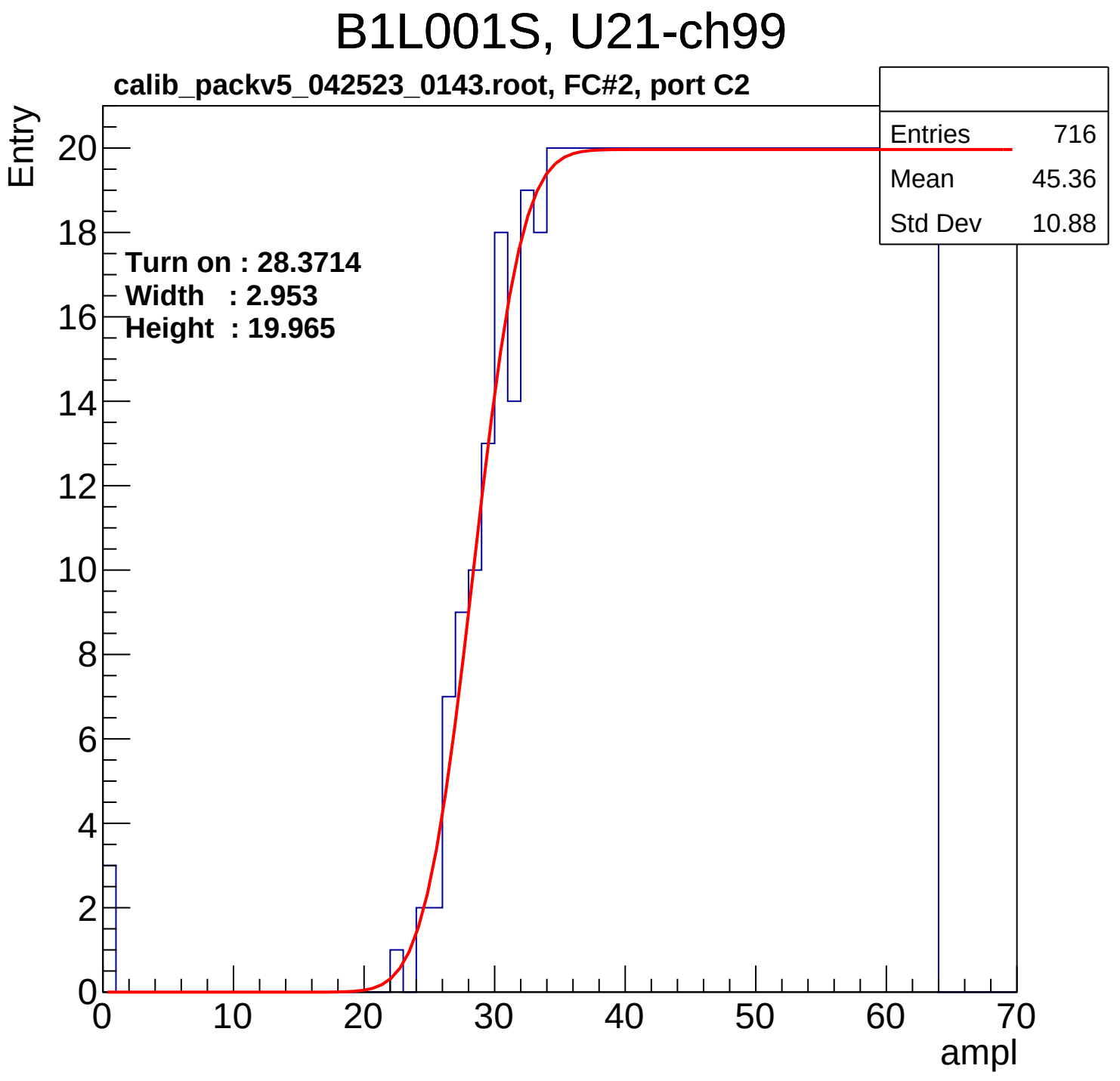
B1L001S, U21-ch99
calib_packv5_042523_0143.root, FC#2, port C2
Entries 716
Mean 45.36
Std Dev 10.88
Turn on : 28.3714
Width : 2.953
Height : 19.965
Entry
ampl
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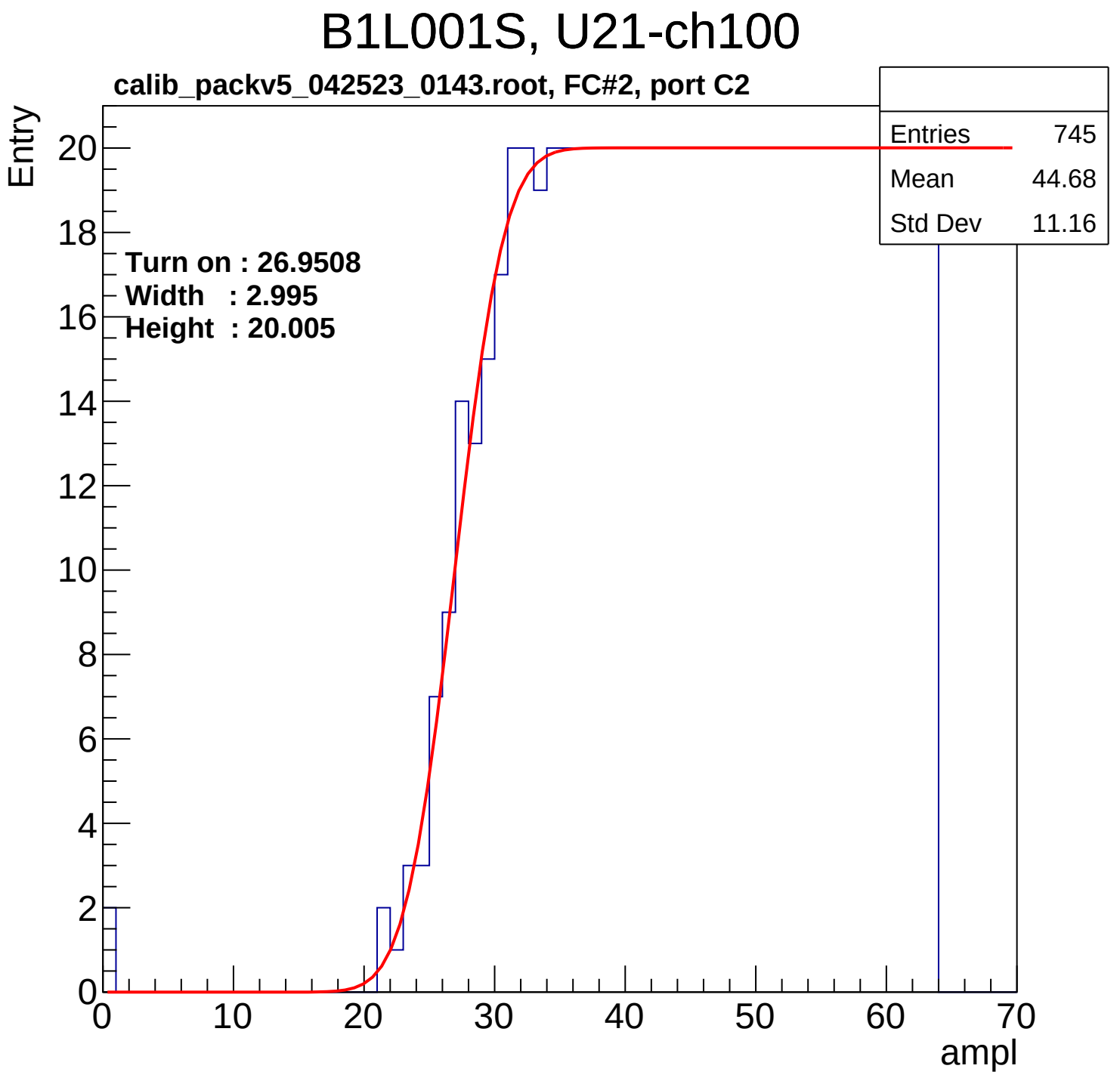
B1L001S, U21-ch100
calib_packv5_042523_0143.root, FC#2, port C2
Entries 745
Mean 44.68
Std Dev 11.16
Turn on : 26.9508
Width : 2.995
Height : 20.005
Entry
ampl
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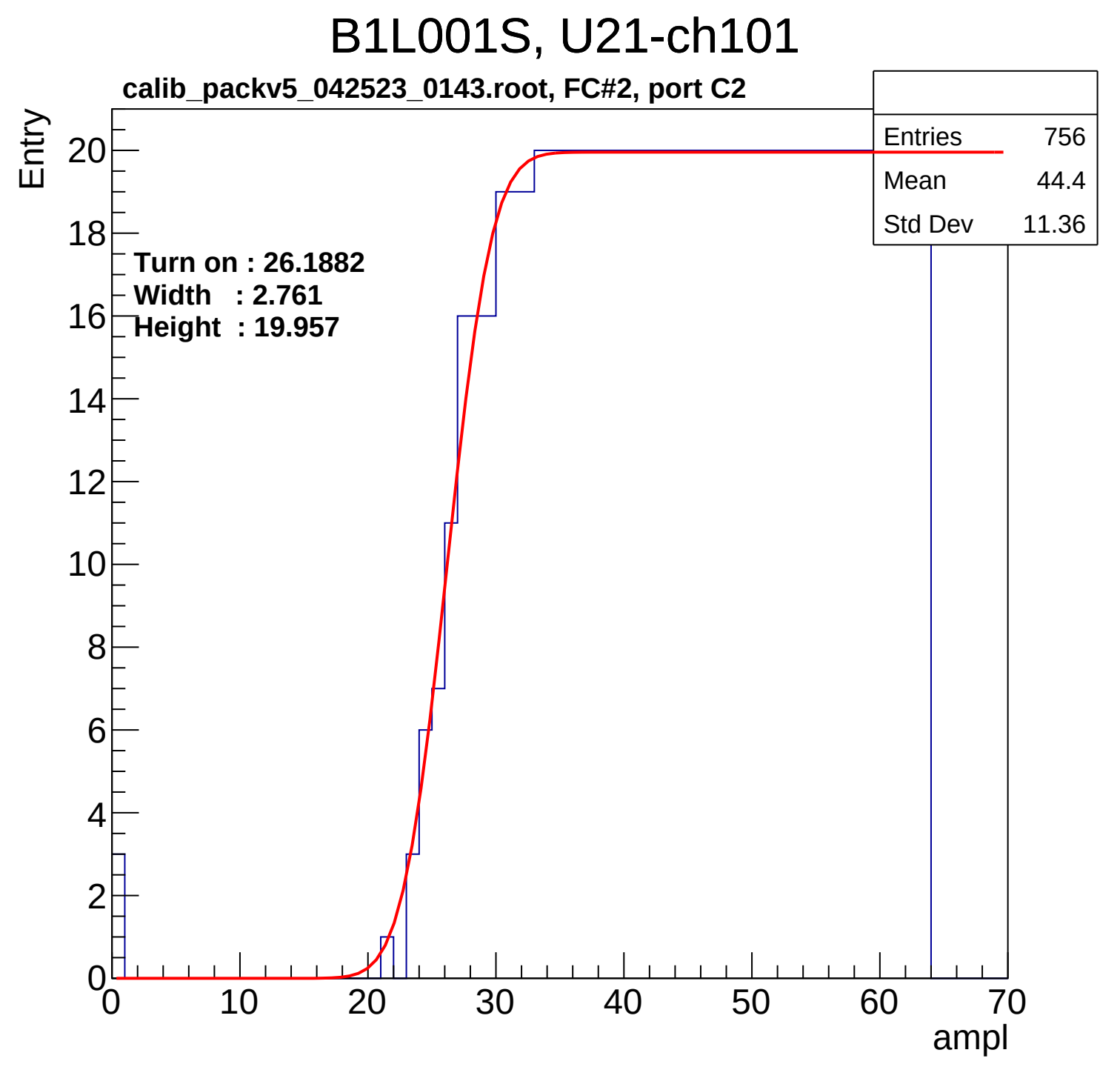
B1L001S, U21-ch101
calib_packv5_042523_0143.root, FC#2, port C2
Entries 756
Mean 44.4
Std Dev 11.36
Turn on : 26.1882
Width : 2.761
Height : 19.957
Entry
ampl
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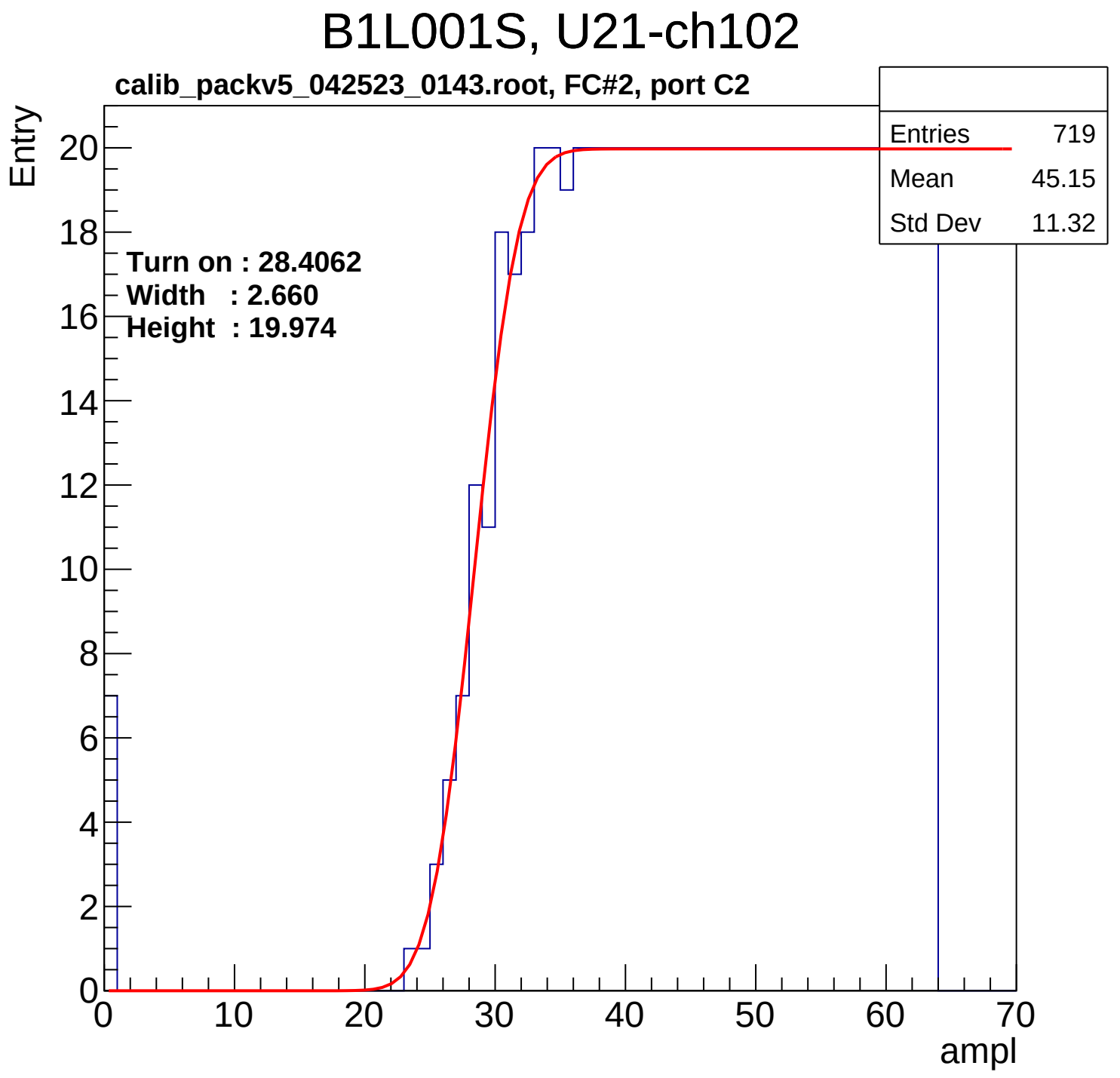
B1L001S, U21-ch102
calib_packv5_042523_0143.root, FC#2, port C2
Entries 719
Mean 45.15
Std Dev 11.32
Turn on : 28.4062
Width : 2.660
Height : 19.974
Entry
ampl
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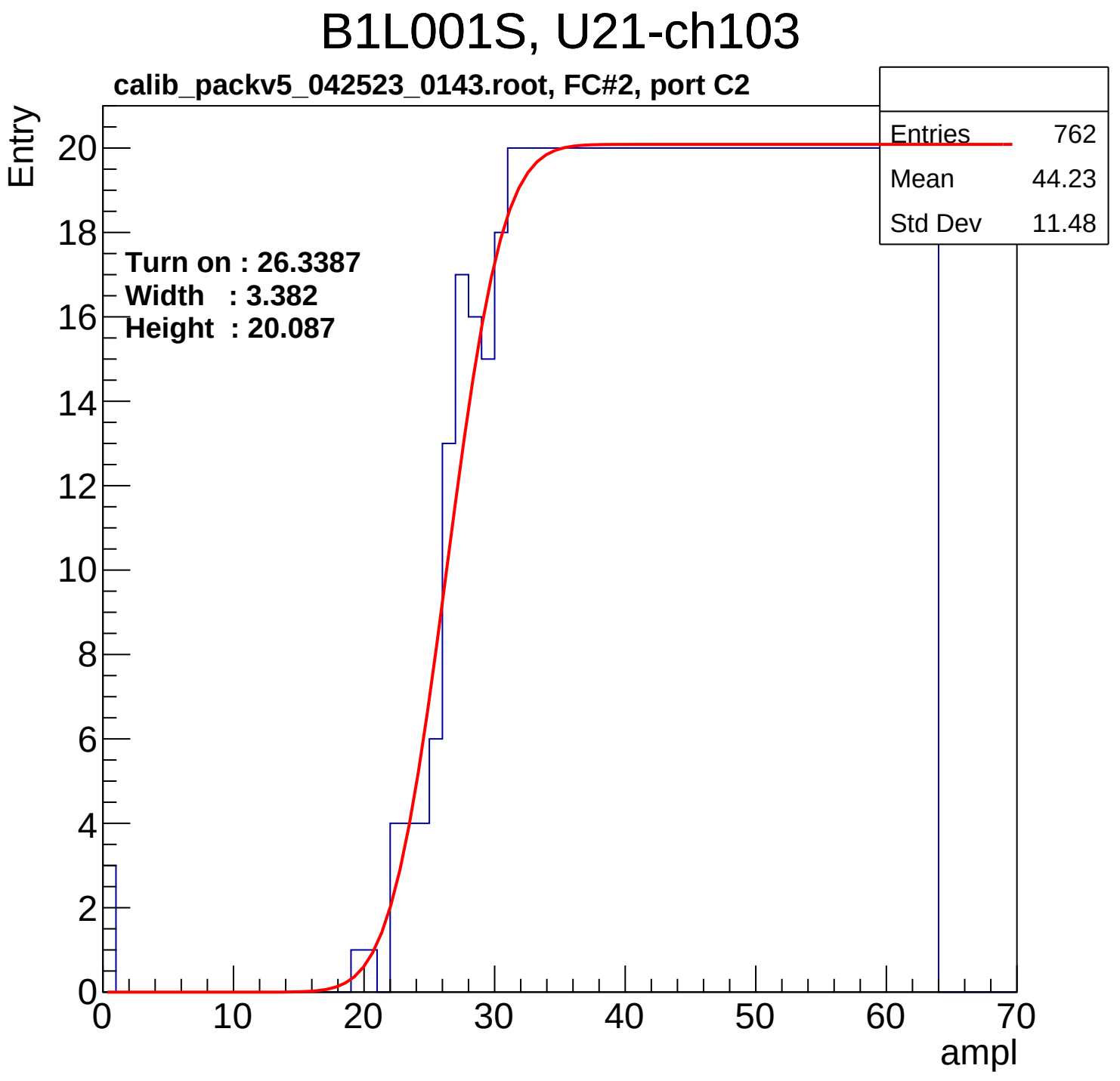
B1L001S, U21-ch103
calib_packv5_042523_0143.root, FC#2, port C2
Entries 762
Mean 44.23
Std Dev 11.48
Turn on : 26.3387
Width : 3.382
Height : 20.087
Entry
ampl
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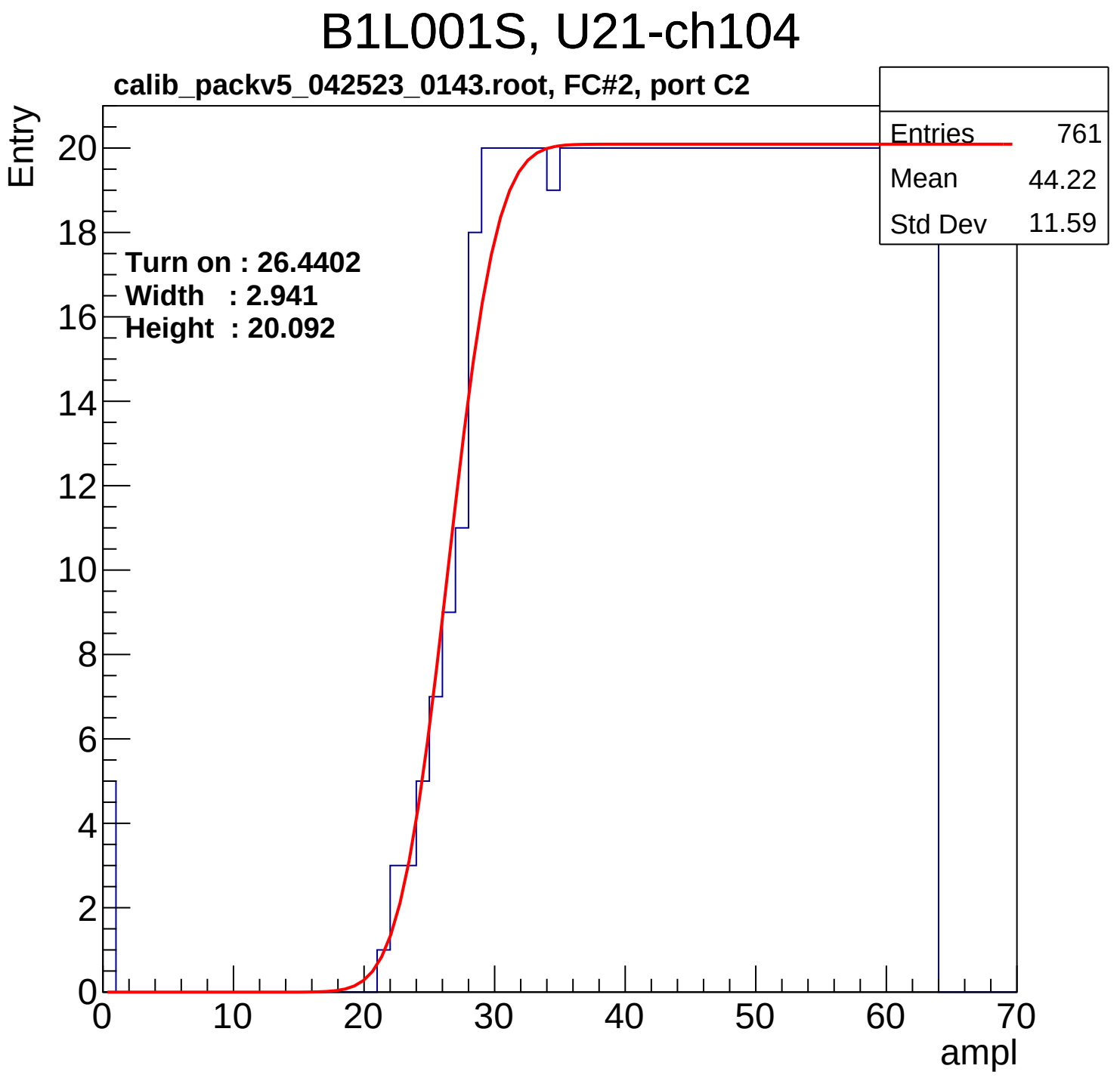
B1L001S, U21-ch104
calib_packv5_042523_0143.root, FC#2, port C2
Entries 761
Mean 44.22
Std Dev 11.59
Turn on : 26.4402
Width : 2.941
Height : 20.092
Entry
ampl
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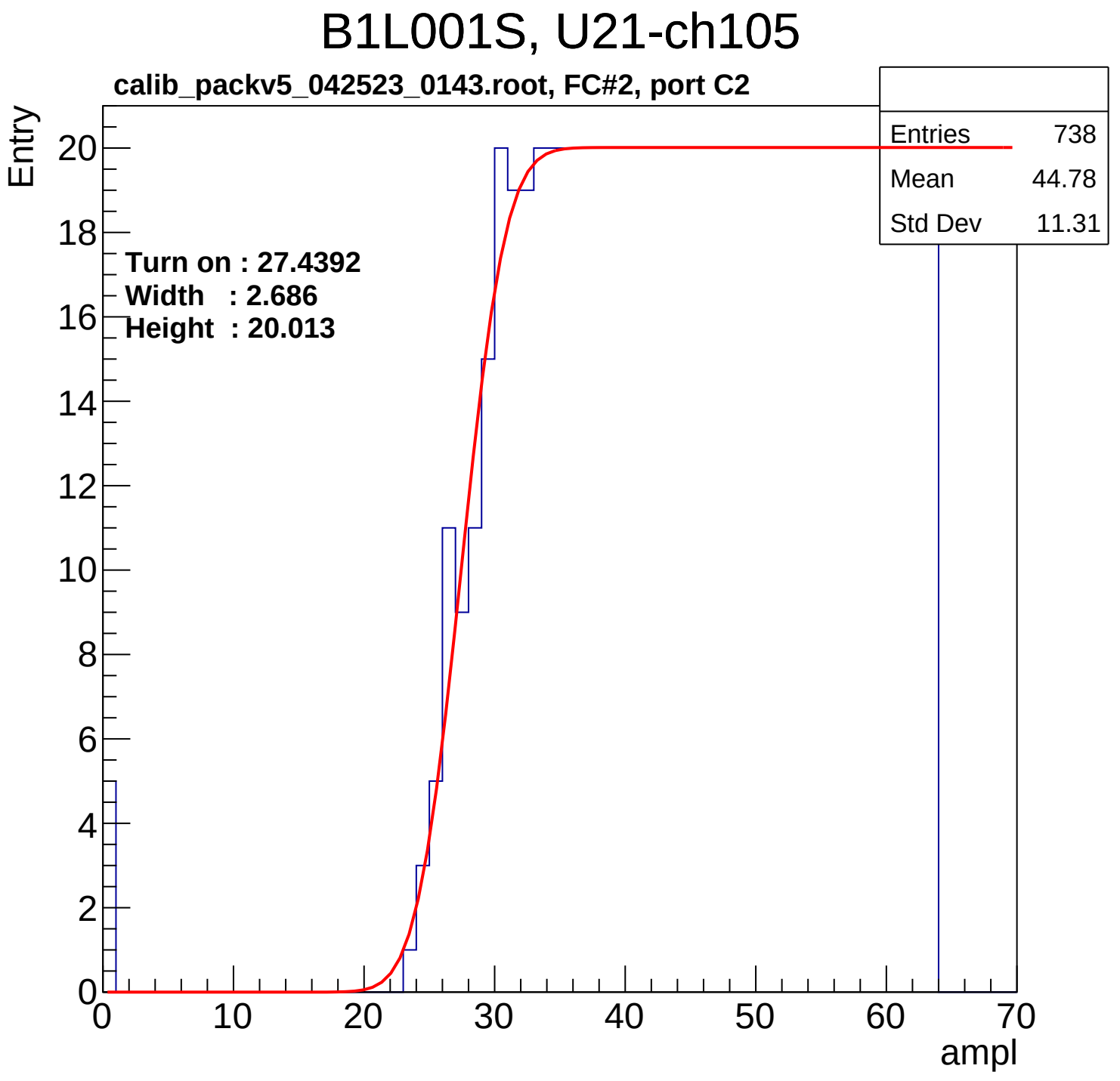
B1L001S, U21-ch105
calib_packv5_042523_0143.root, FC#2, port C2
Entries 738
Mean 44.78
Std Dev 11.31
Turn on : 27.4392
Width : 2.686
Height : 20.013
Entry
ampl
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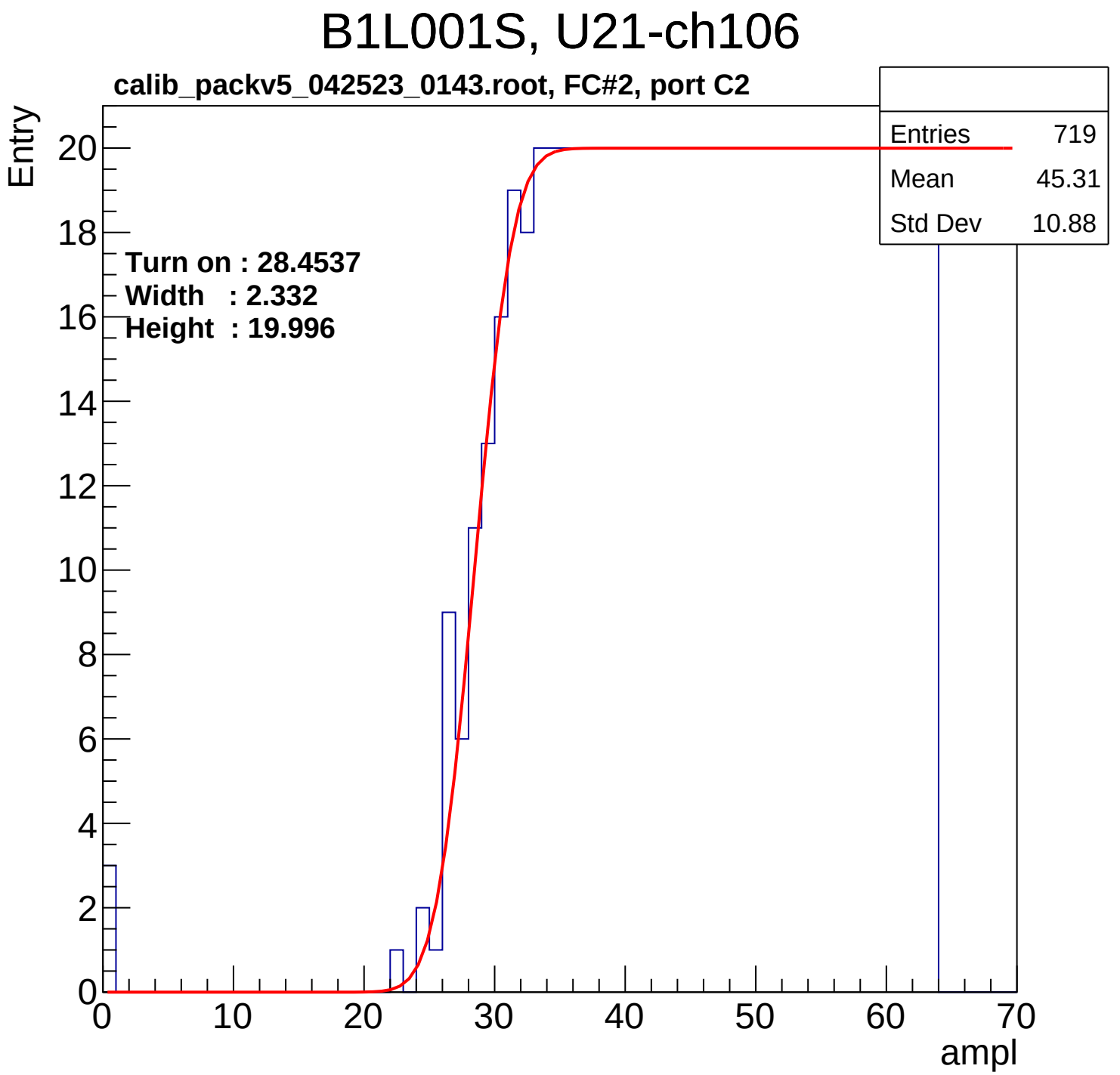
B1L001S, U21-ch106
calib_packv5_042523_0143.root, FC#2, port C2
Entries 719
Mean 45.31
Std Dev 10.88
Turn on : 28.4537
Width : 2.332
Height : 19.996
Entry
ampl
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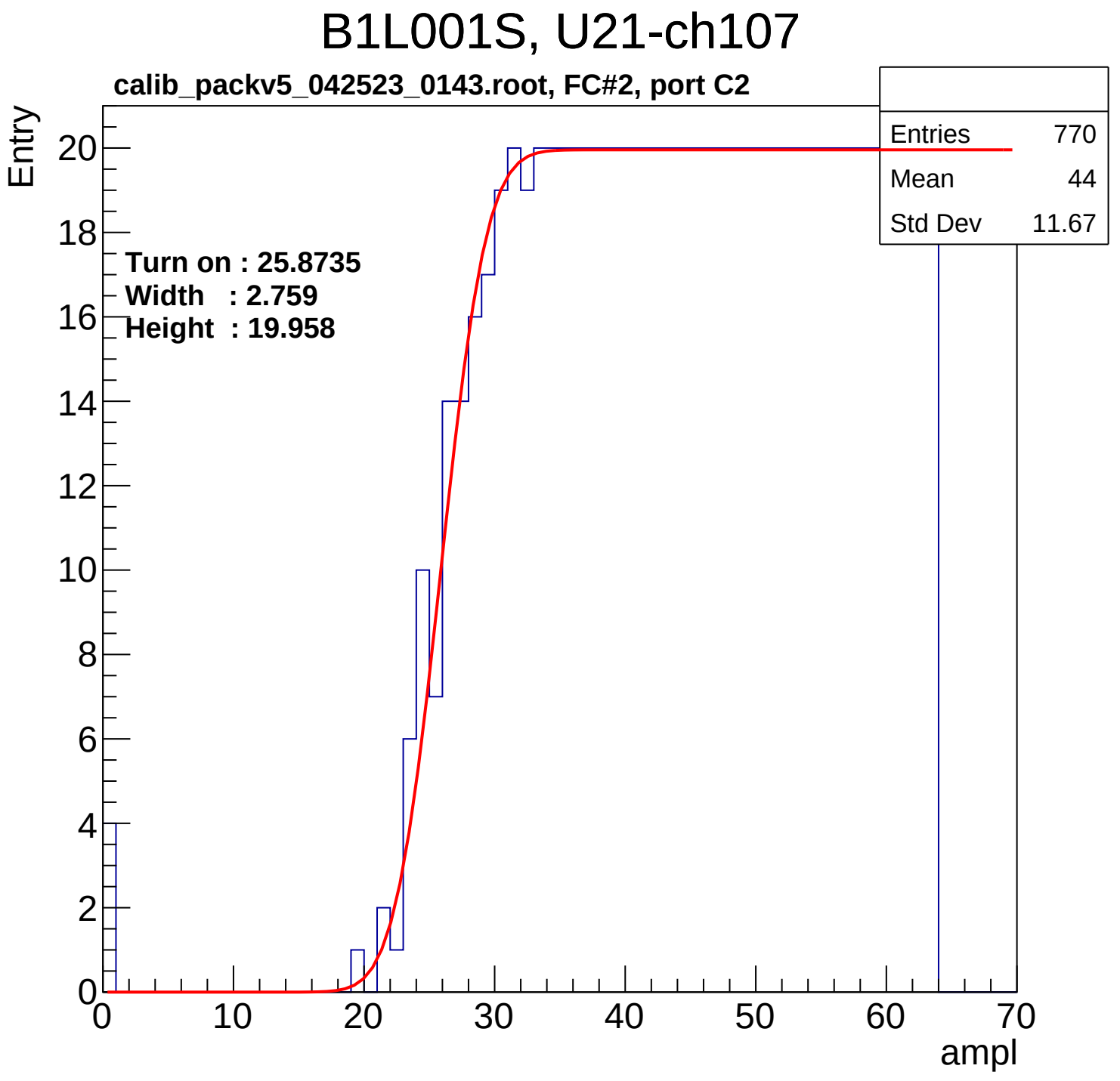
B1L001S, U21-ch107
calib_packv5_042523_0143.root, FC#2, port C2
Entries 770
Mean 44
Std Dev 11.67
Turn on : 25.8735
Width : 2.759
Height : 19.958
Entry
ampl
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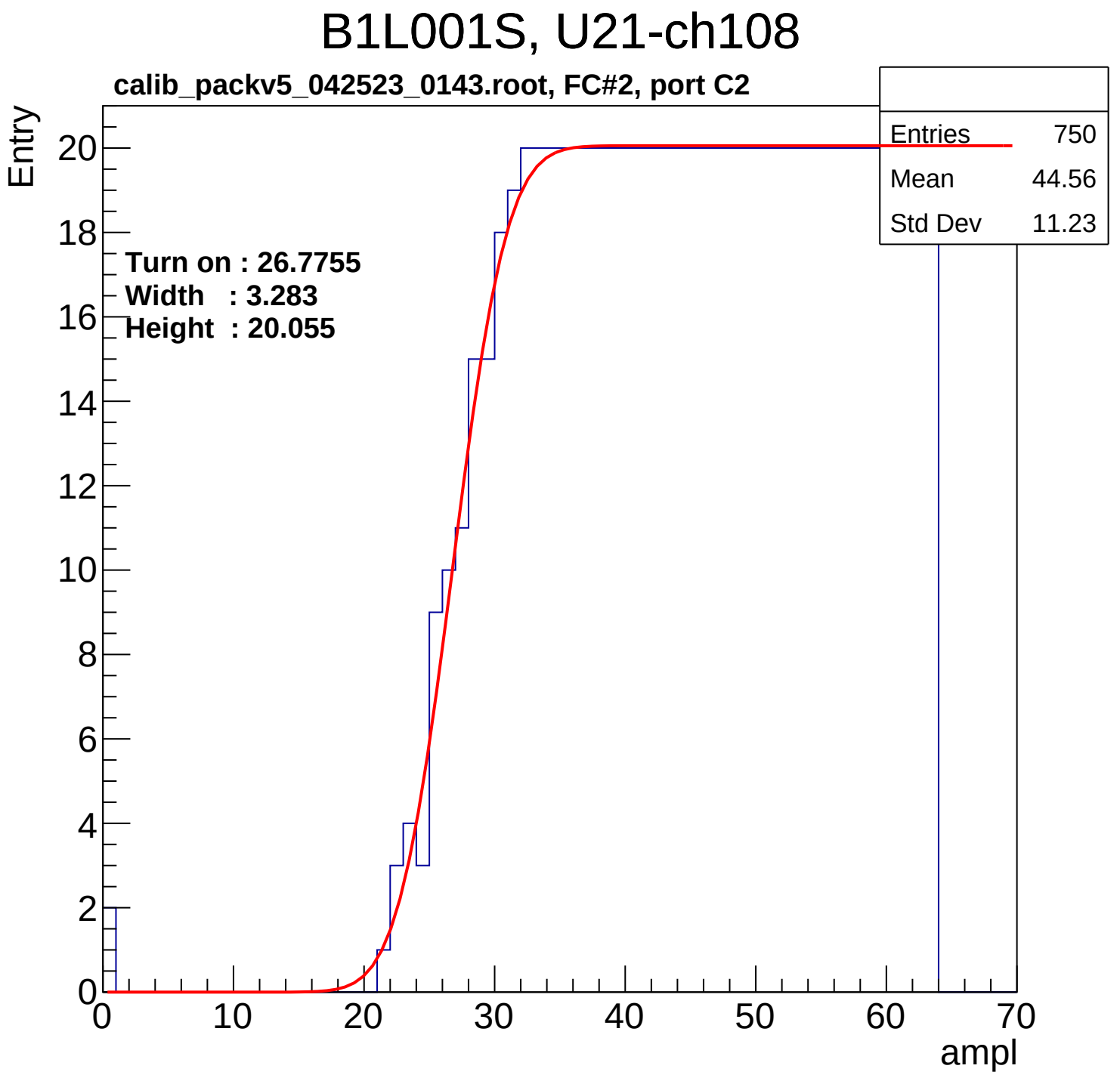
B1L001S, U21-ch108
calib_packv5_042523_0143.root, FC#2, port C2
Entries 750
Mean 44.56
Std Dev 11.23
Turn on : 26.7755
Width : 3.283
Height : 20.055
Entry
ampl
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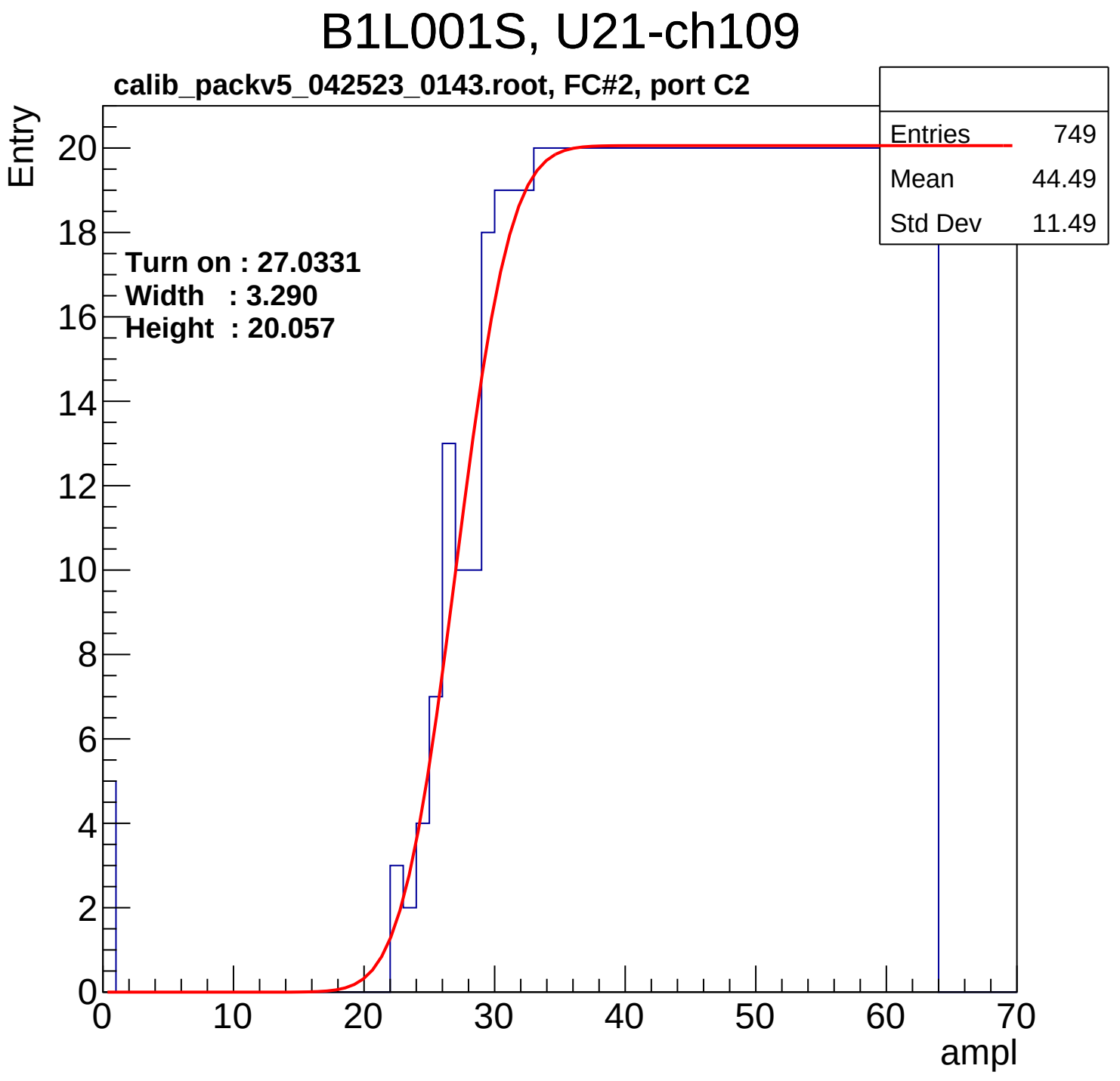
B1L001S, U21-ch109
calib_packv5_042523_0143.root, FC#2, port C2
Entries 749
Mean 44.49
Std Dev 11.49
Turn on : 27.0331
Width : 3.290
Height : 20.057
Entry
ampl
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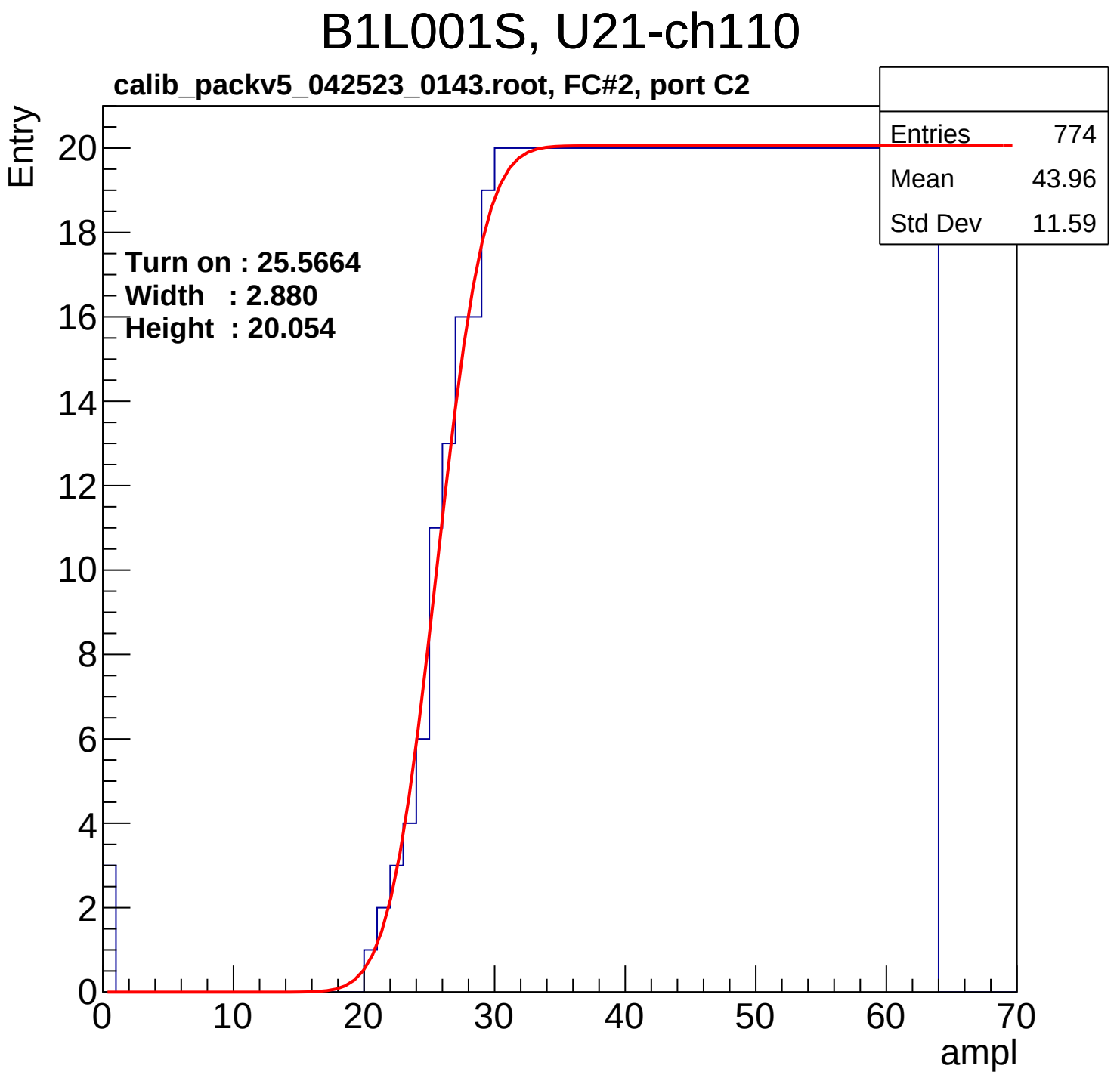
B1L001S, U21-ch110
calib_packv5_042523_0143.root, FC#2, port C2
Entries 774
Mean 43.96
Std Dev 11.59
Turn on : 25.5664
Width : 2.880
Height : 20.054
Entry
ampl
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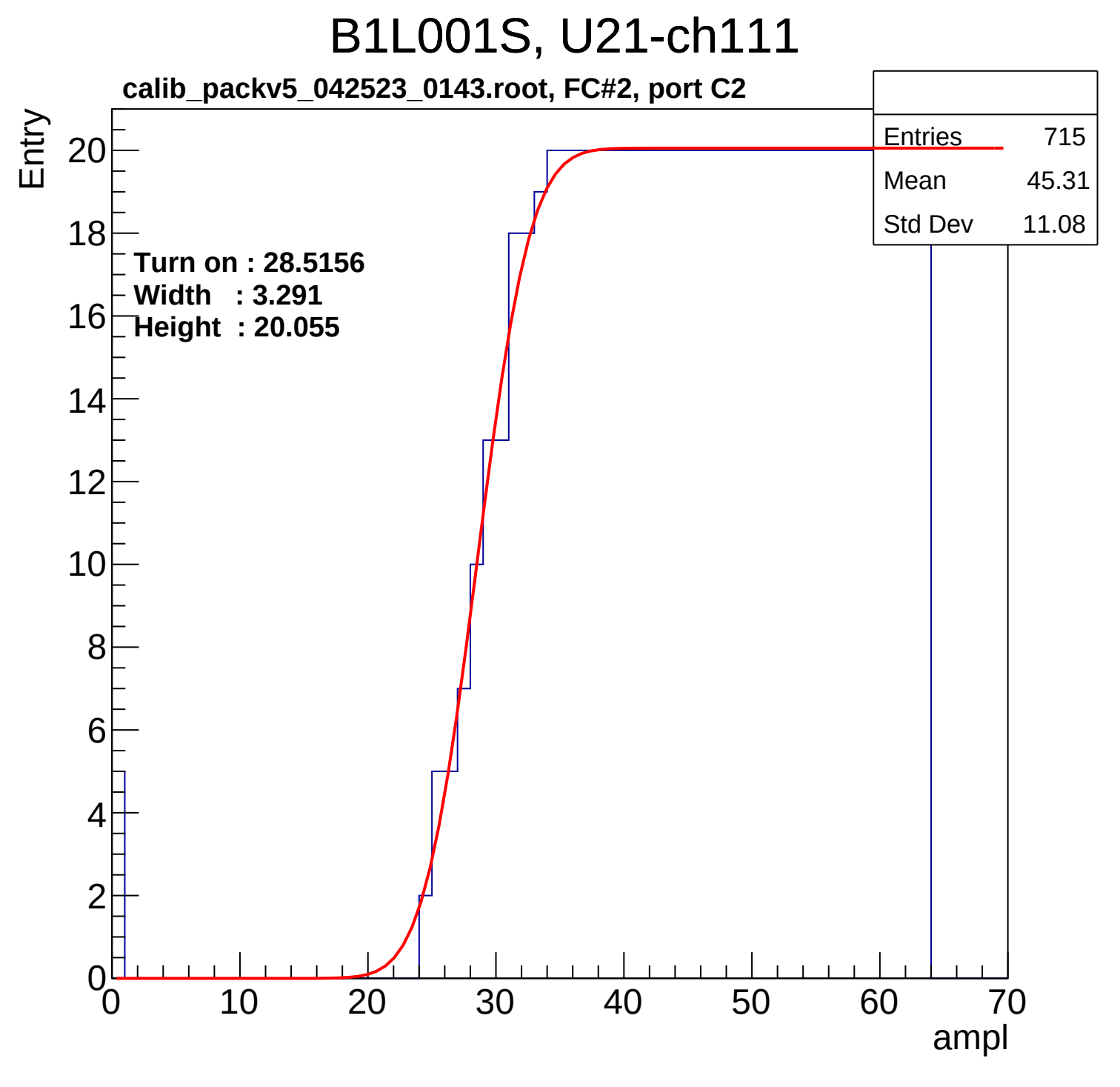
B1L001S, U21-ch111
calib_packv5_042523_0143.root, FC#2, port C2
Entries 715
Mean 45.31
Std Dev 11.08
Turn on : 28.5156
Width : 3.291
Height : 20.055
Entry
ampl
0
2
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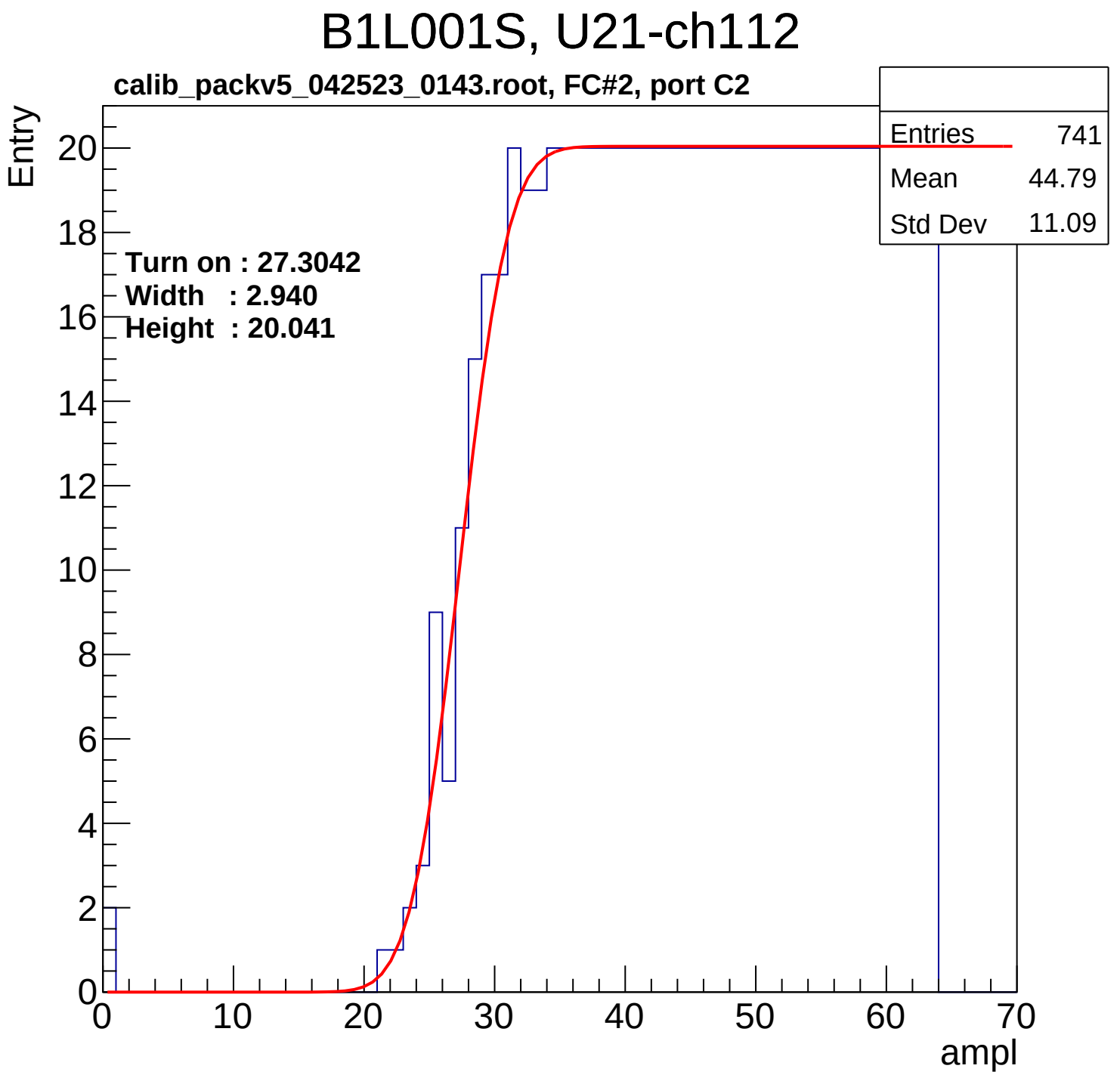
B1L001S, U21-ch112
calib_packv5_042523_0143.root, FC#2, port C2
Entries 741
Mean 44.79
Std Dev 11.09
Turn on : 27.3042
Width : 2.940
Height : 20.041
Entry
ampl
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6
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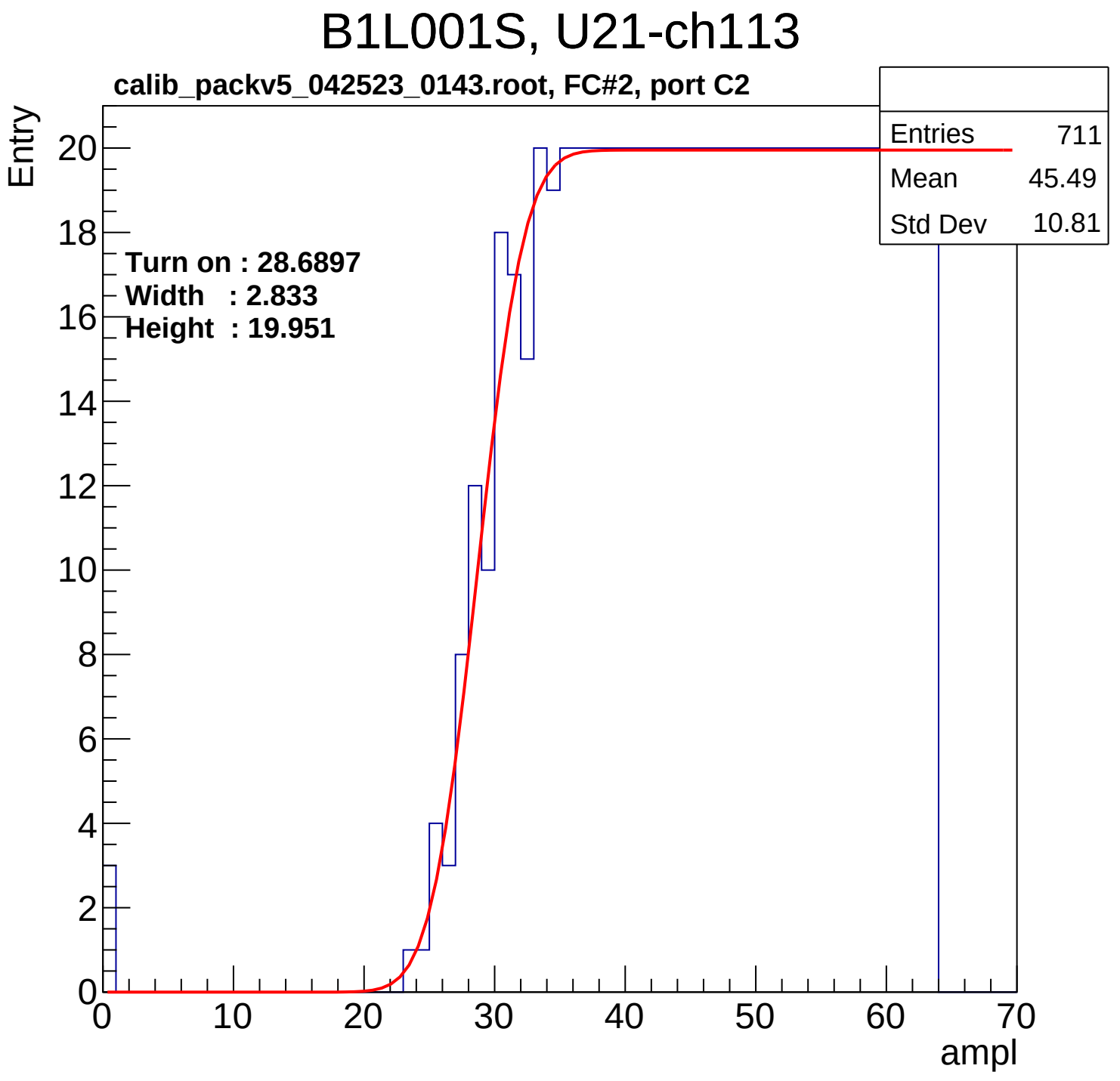
B1L001S, U21-ch113
calib_packv5_042523_0143.root, FC#2, port C2
Entries 711
Mean 45.49
Std Dev 10.81
Turn on : 28.6897
Width : 2.833
Height : 19.951
Entry
ampl
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2
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6
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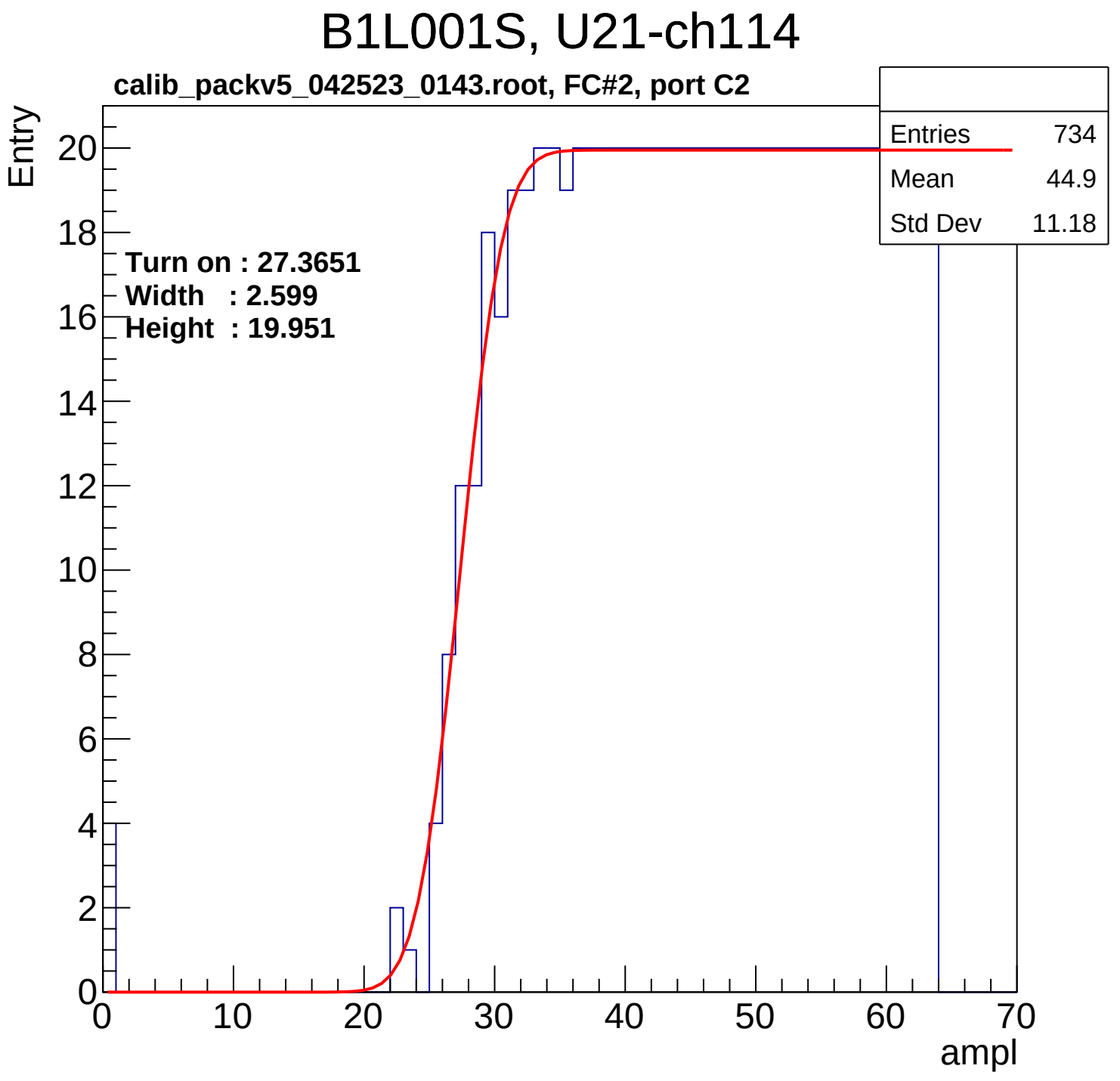
B1L001S, U21-ch114
calib_packv5_042523_0143.root, FC#2, port C2
Entries 734
Mean 44.9
Std Dev 11.18
Turn on : 27.3651
Width : 2.599
Height : 19.951
Entry
ampl
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6
8
10
12
14
16
18
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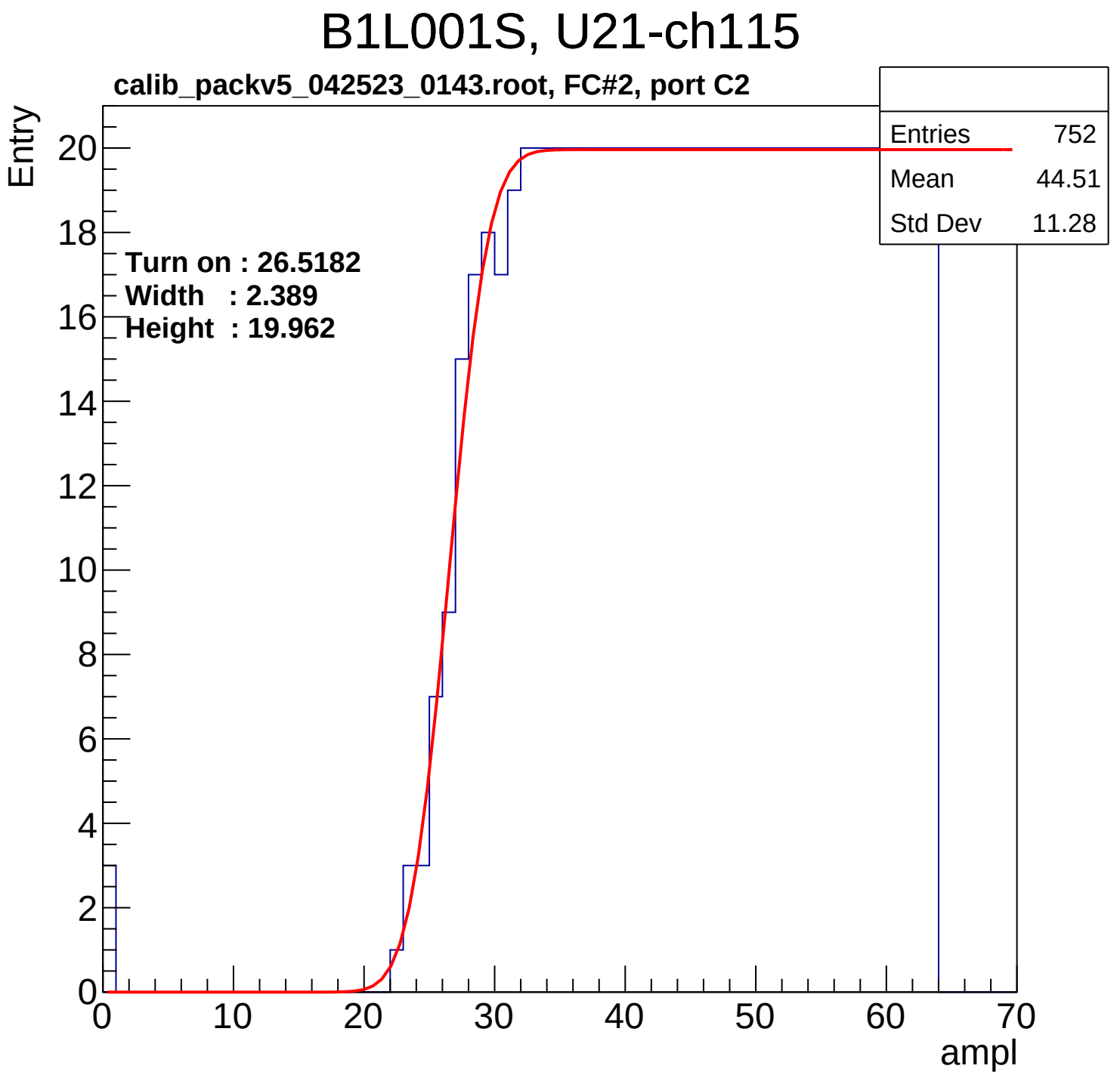
B1L001S, U21-ch115
calib_packv5_042523_0143.root, FC#2, port C2
Entries 752
Mean 44.51
Std Dev 11.28
Turn on : 26.5182
Width : 2.389
Height : 19.962
Entry
ampl
0
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4
6
8
10
12
14
16
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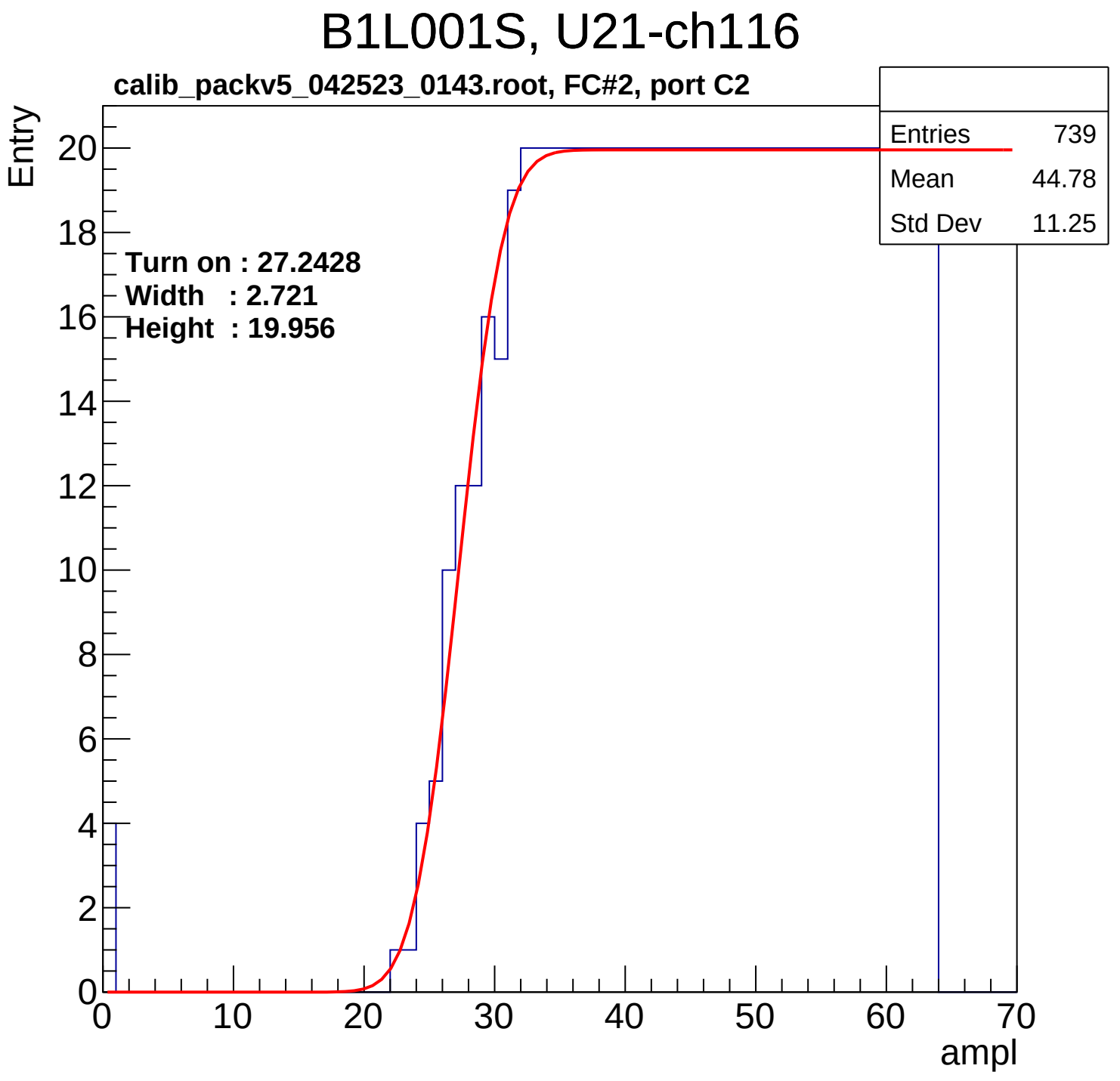
B1L001S, U21-ch116
calib_packv5_042523_0143.root, FC#2, port C2
Entries 739
Mean 44.78
Std Dev 11.25
Turn on : 27.2428
Width : 2.721
Height : 19.956
Entry
ampl
0
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6
8
10
12
14
16
18
20
0
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20
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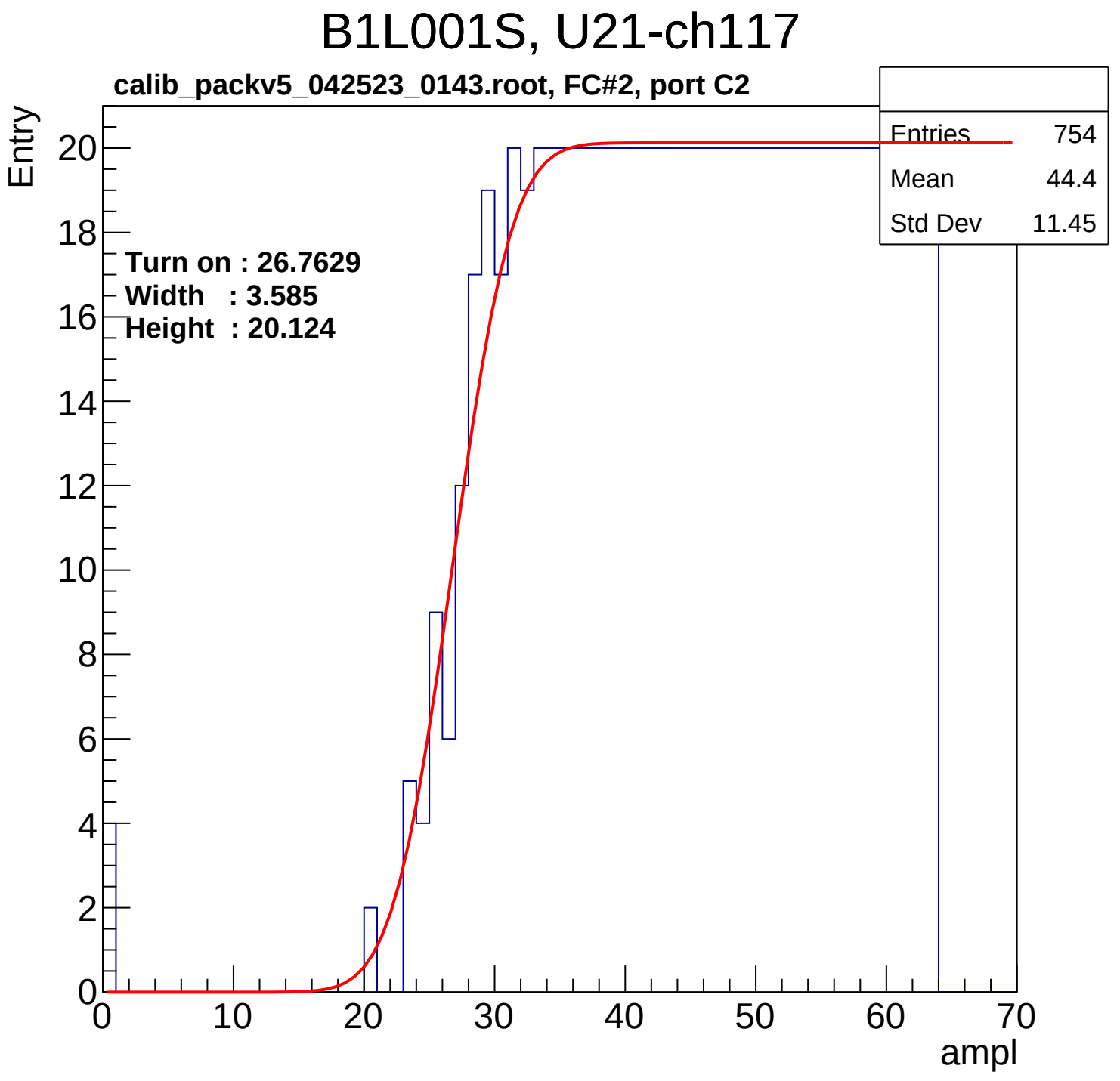
B1L001S, U21-ch117
calib_packv5_042523_0143.root, FC#2, port C2
Entries 754
Mean 44.4
Std Dev 11.45
Turn on : 26.7629
Width : 3.585
Height : 20.124
Entry
ampl
0
2
4
6
8
10
12
14
16
18
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0
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20
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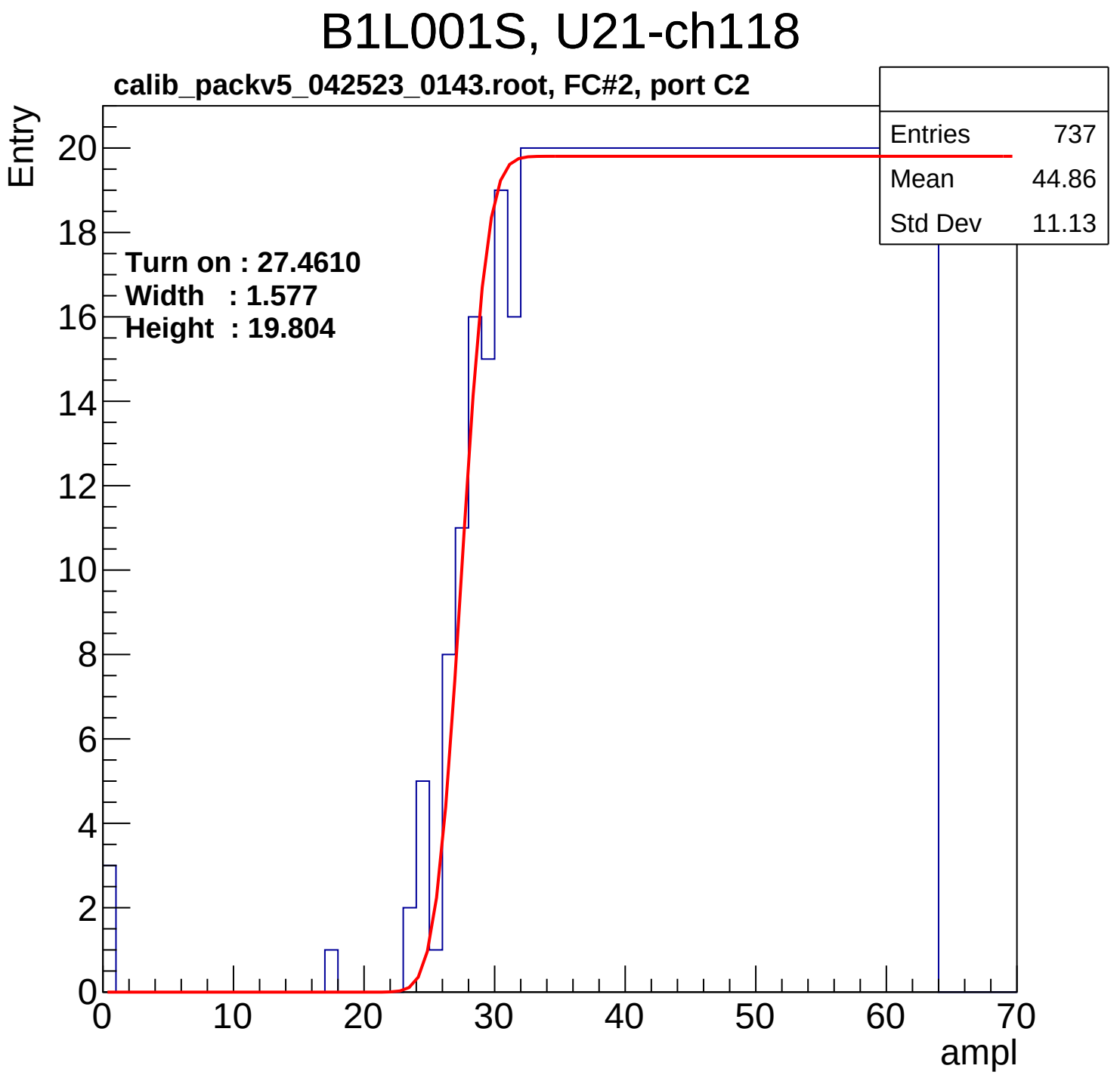
B1L001S, U21-ch118
calib_packv5_042523_0143.root, FC#2, port C2
Entries 737
Mean 44.86
Std Dev 11.13
Turn on : 27.4610
Width : 1.577
Height : 19.804
Entry
ampl
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6
8
10
12
14
16
18
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0
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60
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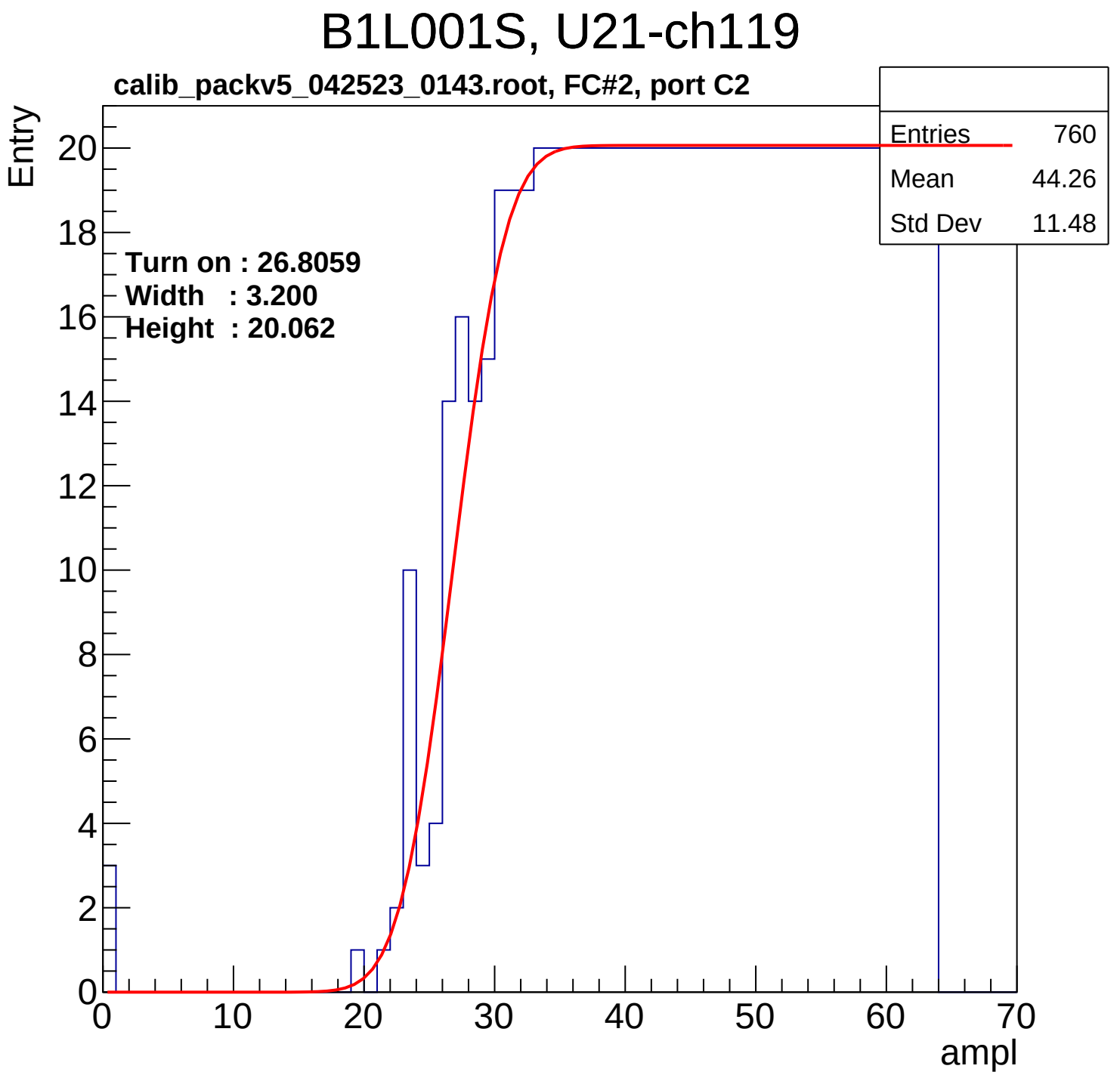
B1L001S, U21-ch119
calib_packv5_042523_0143.root, FC#2, port C2
Entries 760
Mean 44.26
Std Dev 11.48
Turn on : 26.8059
Width : 3.200
Height : 20.062
Entry
ampl
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6
8
10
12
14
16
18
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0
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60
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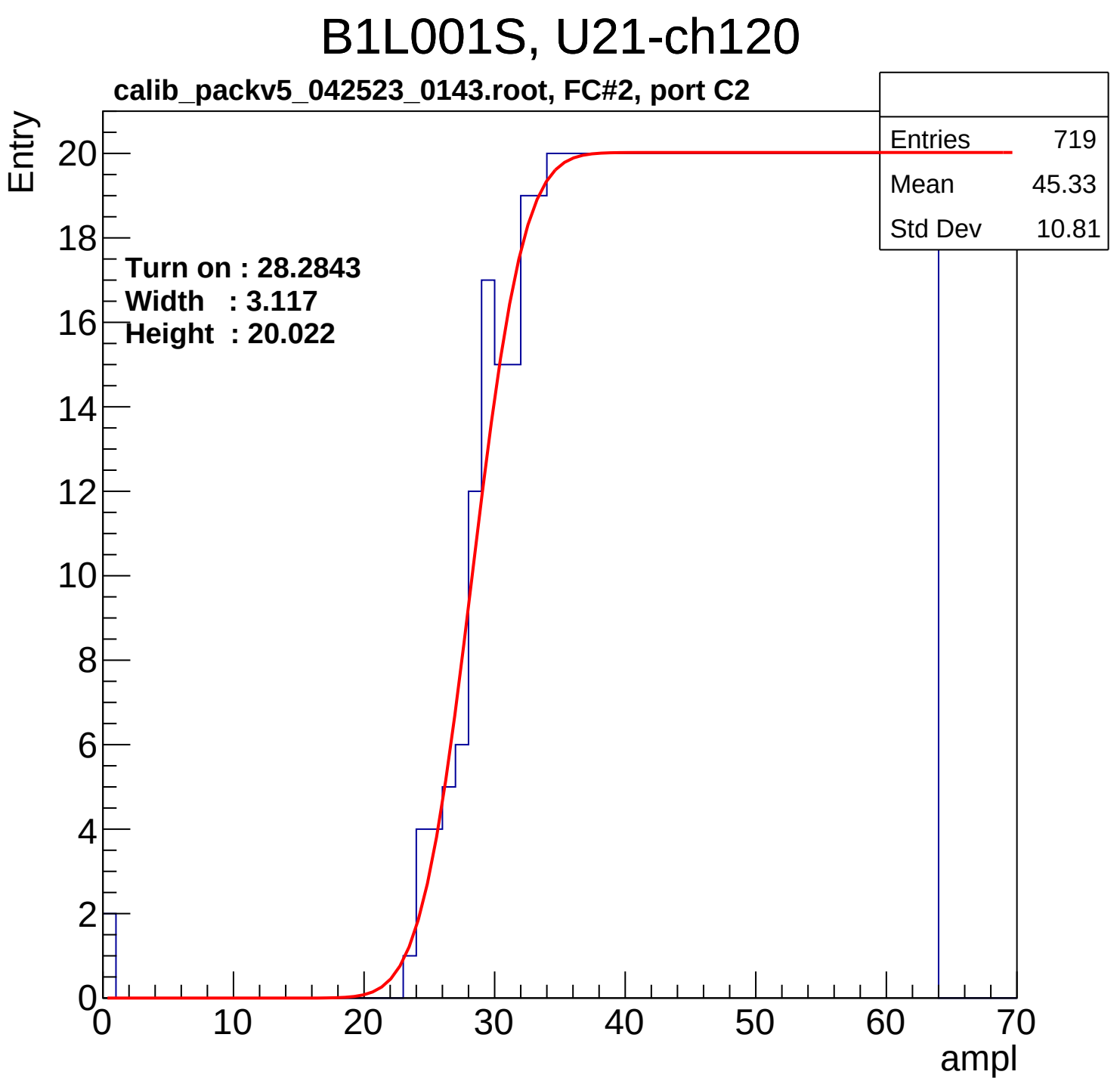
B1L001S, U21-ch120
calib_packv5_042523_0143.root, FC#2, port C2
Entries 719
Mean 45.33
Std Dev 10.81
Turn on : 28.2843
Width : 3.117
Height : 20.022
Entry
ampl
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6
8
10
12
14
16
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20
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60
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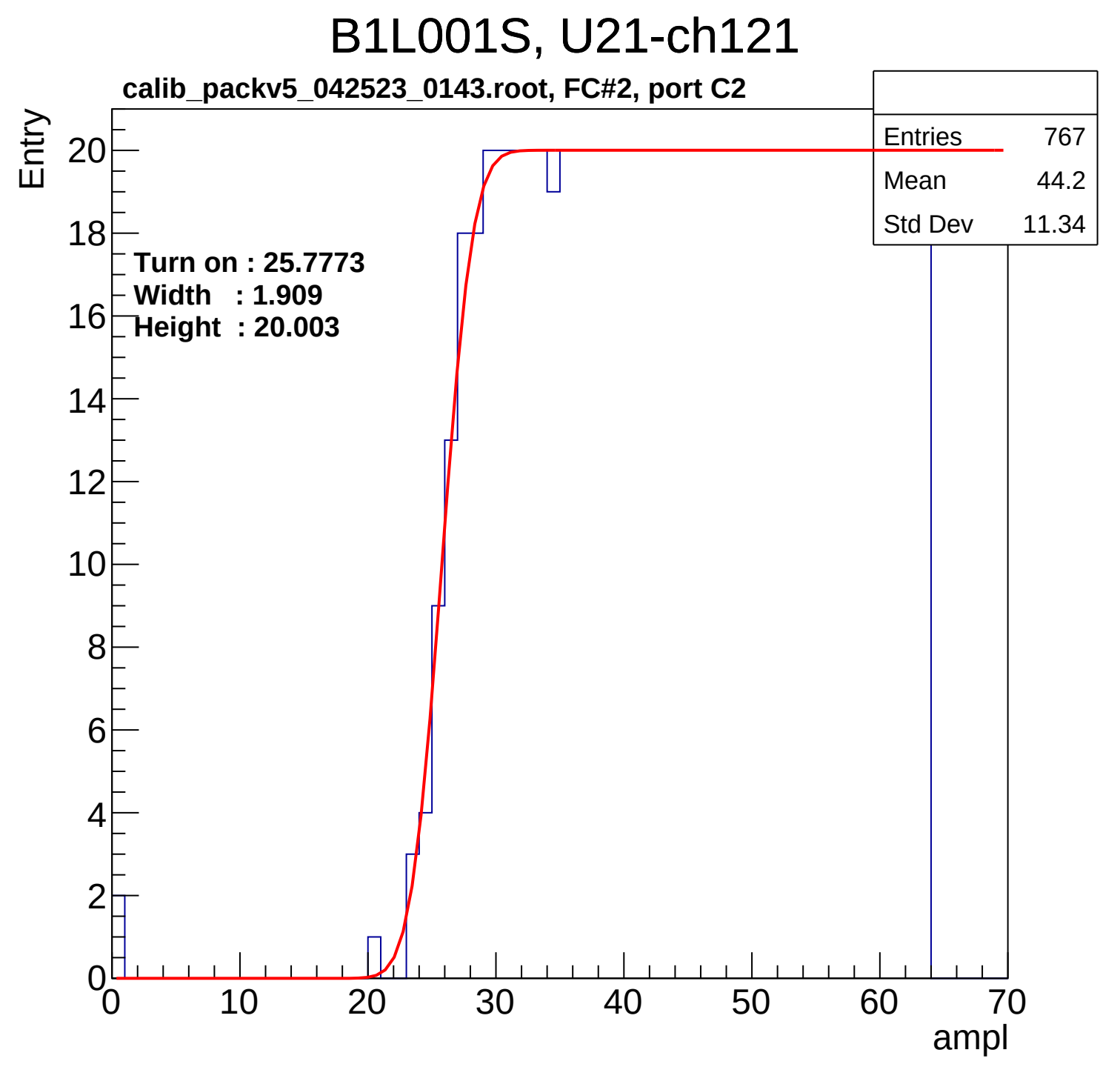
B1L001S, U21-ch121
calib_packv5_042523_0143.root, FC#2, port C2
Entries 767
Mean 44.2
Std Dev 11.34
Turn on : 25.7773
Width : 1.909
Height : 20.003
Entry
ampl
0
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4
6
8
10
12
14
16
18
20
0
10
20
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40
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60
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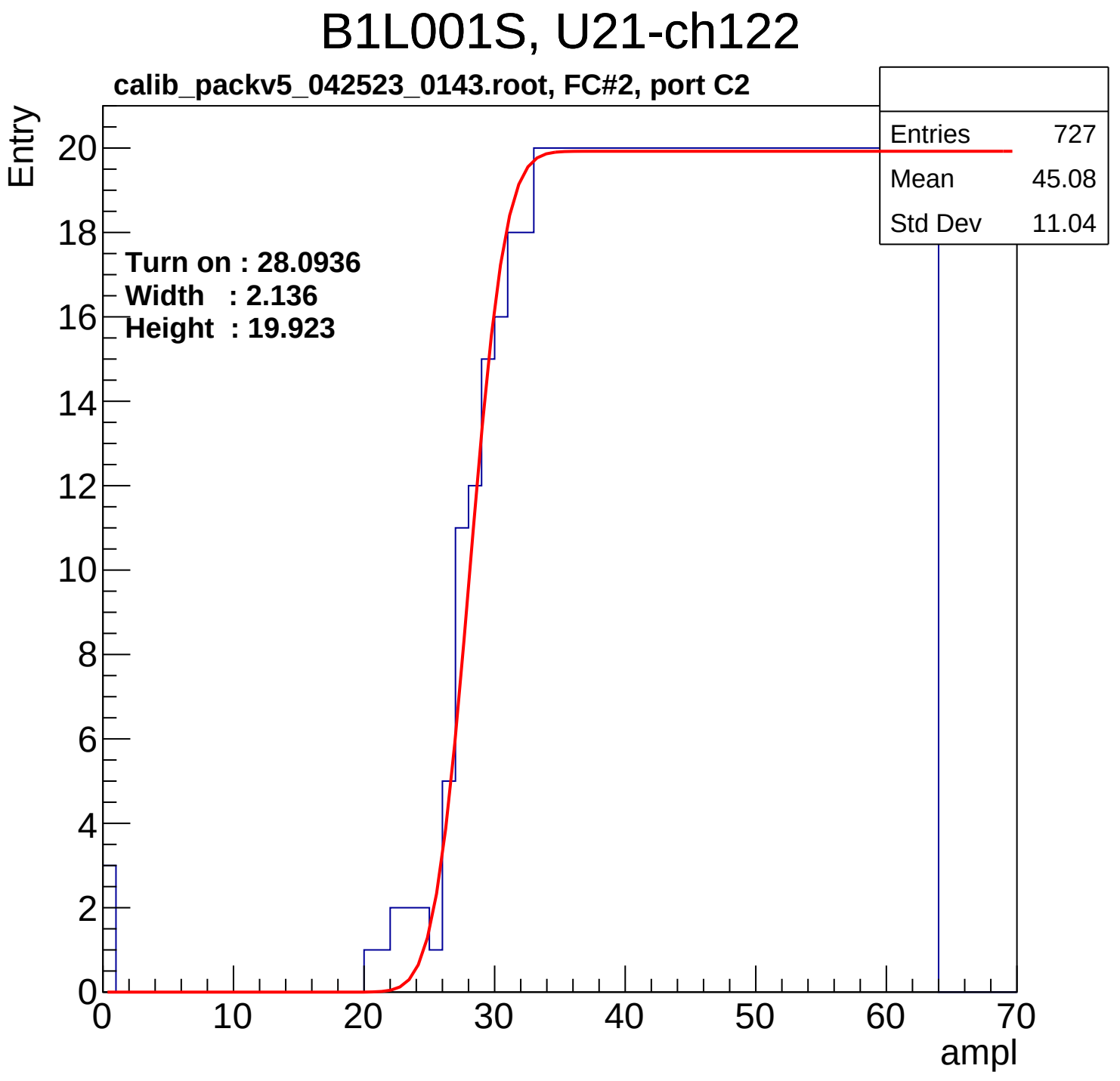
B1L001S, U21-ch122
calib_packv5_042523_0143.root, FC#2, port C2
Entries 727
Mean 45.08
Std Dev 11.04
Turn on : 28.0936
Width : 2.136
Height : 19.923
Entry
ampl
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6
8
10
12
14
16
18
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0
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20
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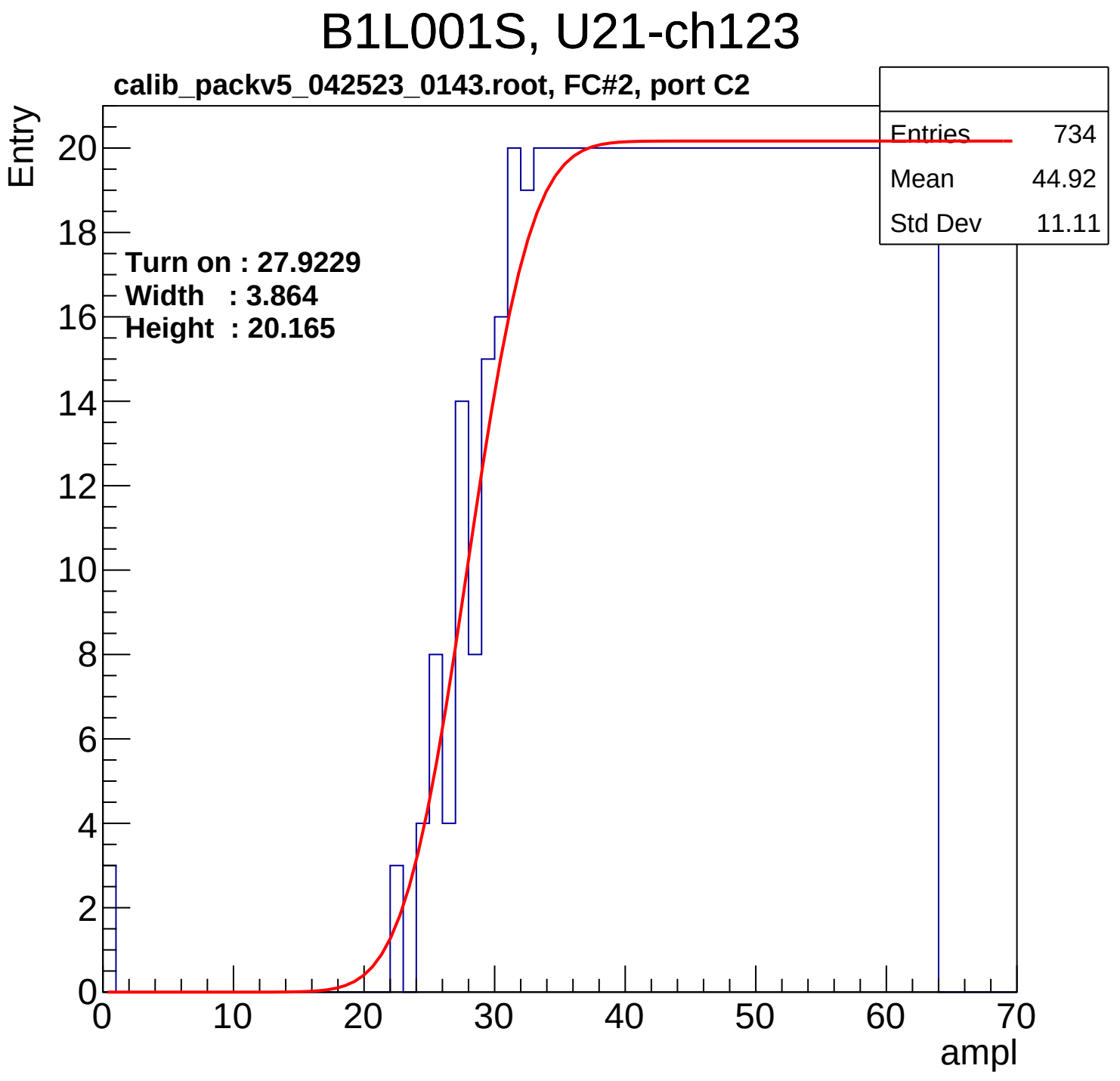
B1L001S, U21-ch123
calib_packv5_042523_0143.root, FC#2, port C2
Entries 734
Mean 44.92
Std Dev 11.11
Turn on : 27.9229
Width : 3.864
Height : 20.165
Entry
ampl
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6
8
10
12
14
16
18
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0
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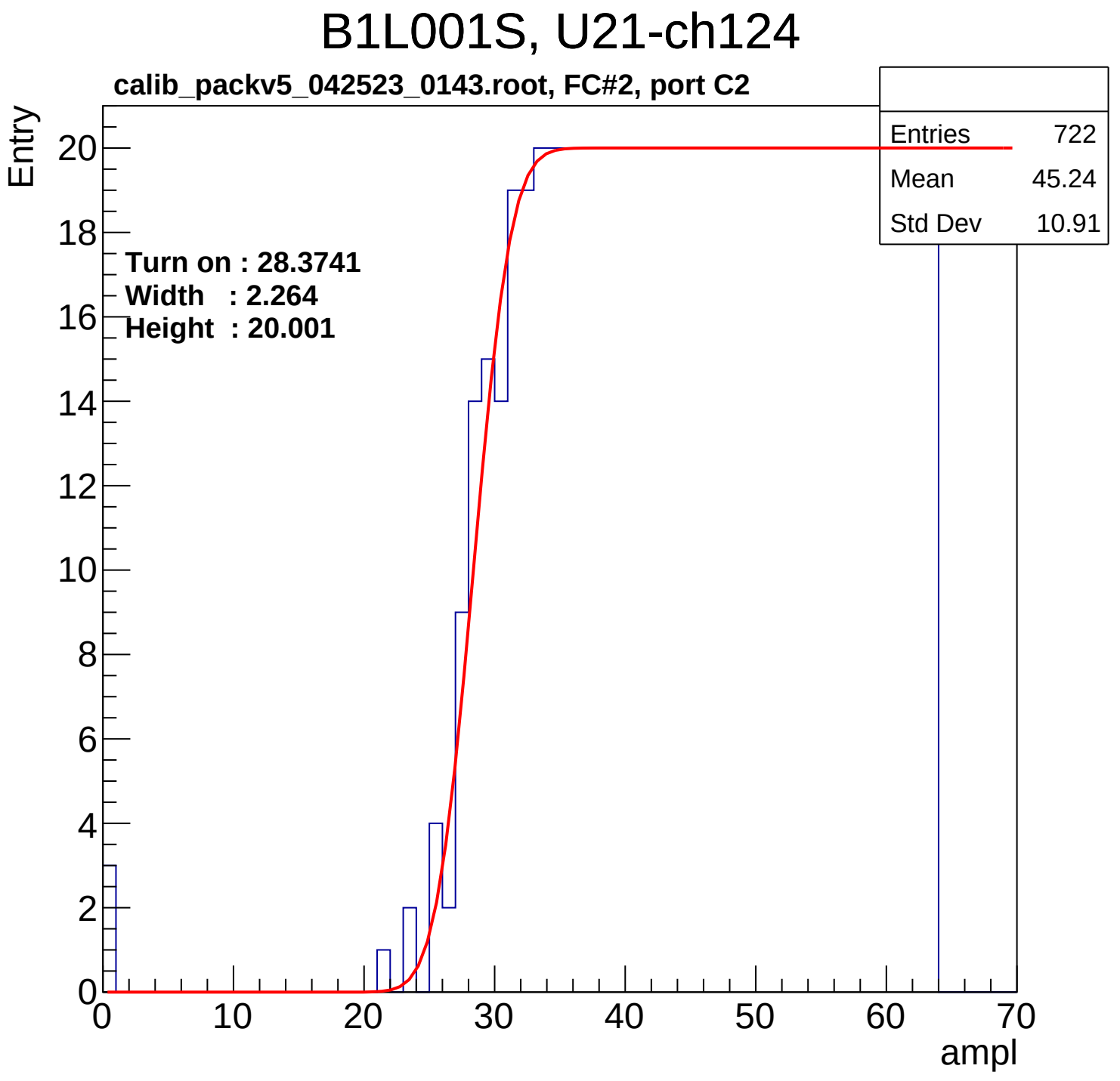
B1L001S, U21-ch124
calib_packv5_042523_0143.root, FC#2, port C2
Entries 722
Mean 45.24
Std Dev 10.91
Turn on : 28.3741
Width : 2.264
Height : 20.001
Entry
ampl
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6
8
10
12
14
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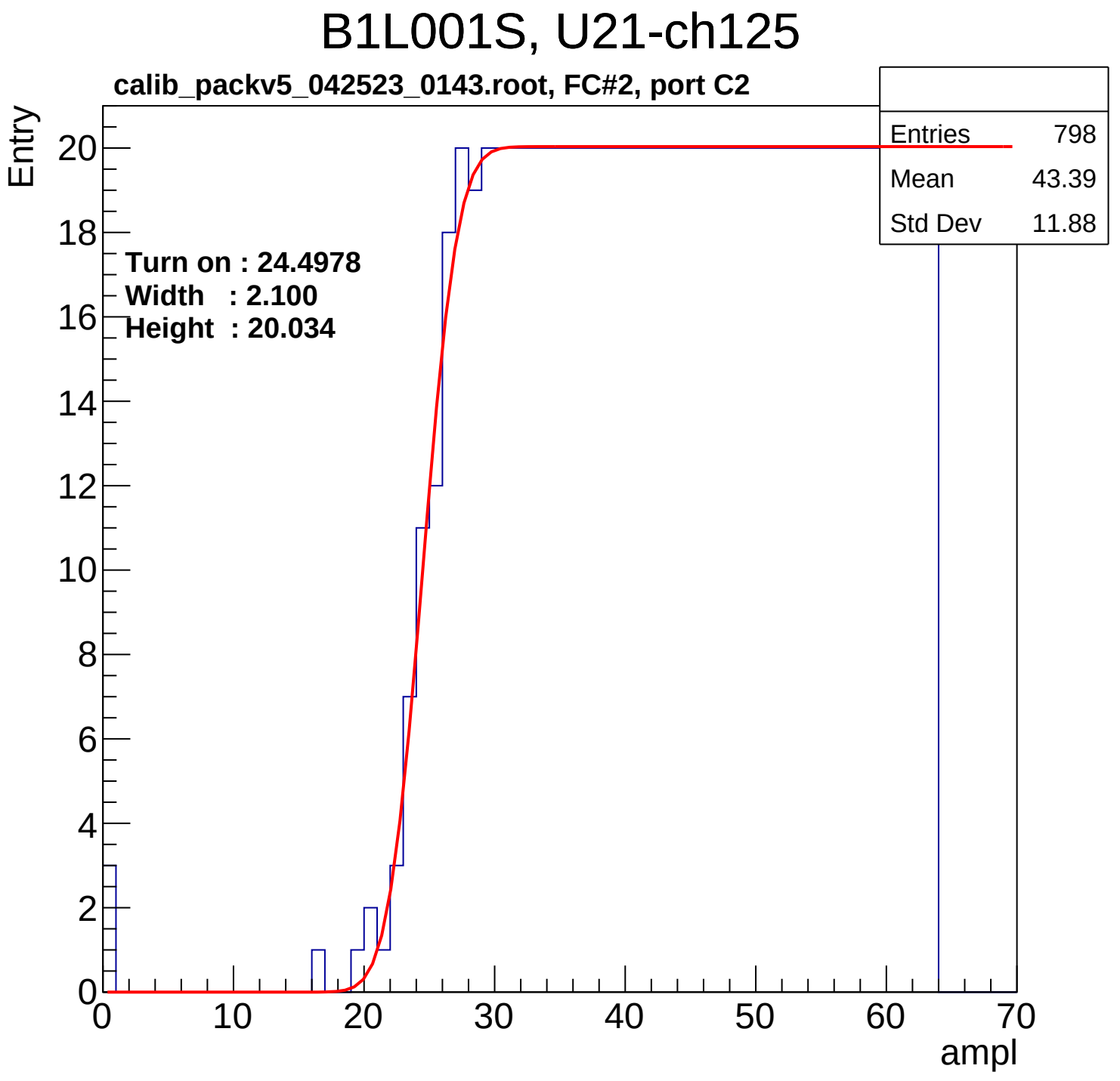
B1L001S, U21-ch125
calib_packv5_042523_0143.root, FC#2, port C2
Entries 798
Mean 43.39
Std Dev 11.88
Turn on : 24.4978
Width : 2.100
Height : 20.034
Entry
ampl
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6
8
10
12
14
16
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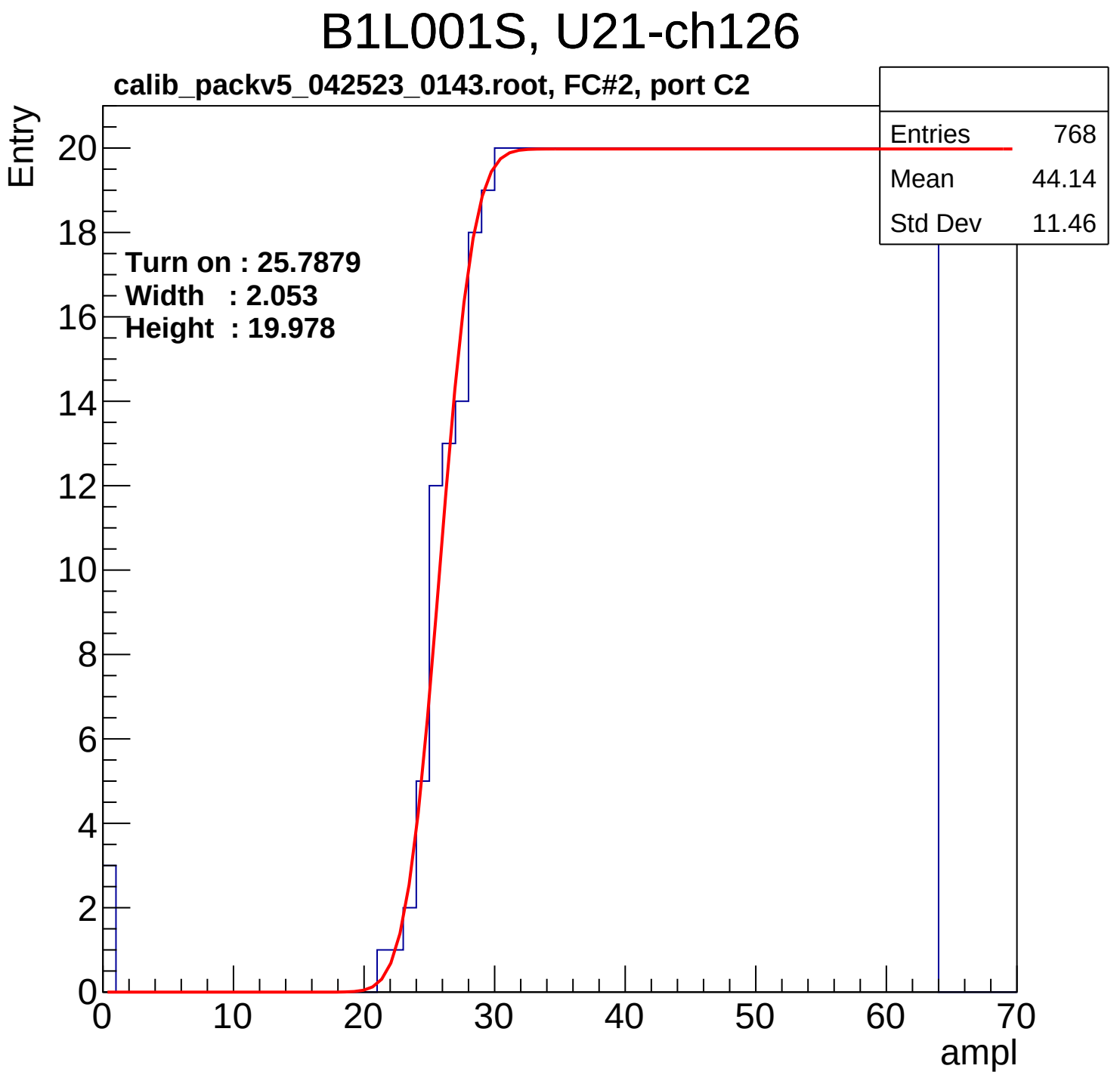
B1L001S, U21-ch126
calib_packv5_042523_0143.root, FC#2, port C2
Entries 768
Mean 44.14
Std Dev 11.46
Turn on : 25.7879
Width : 2.053
Height : 19.978
Entry
ampl
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8
10
12
14
16
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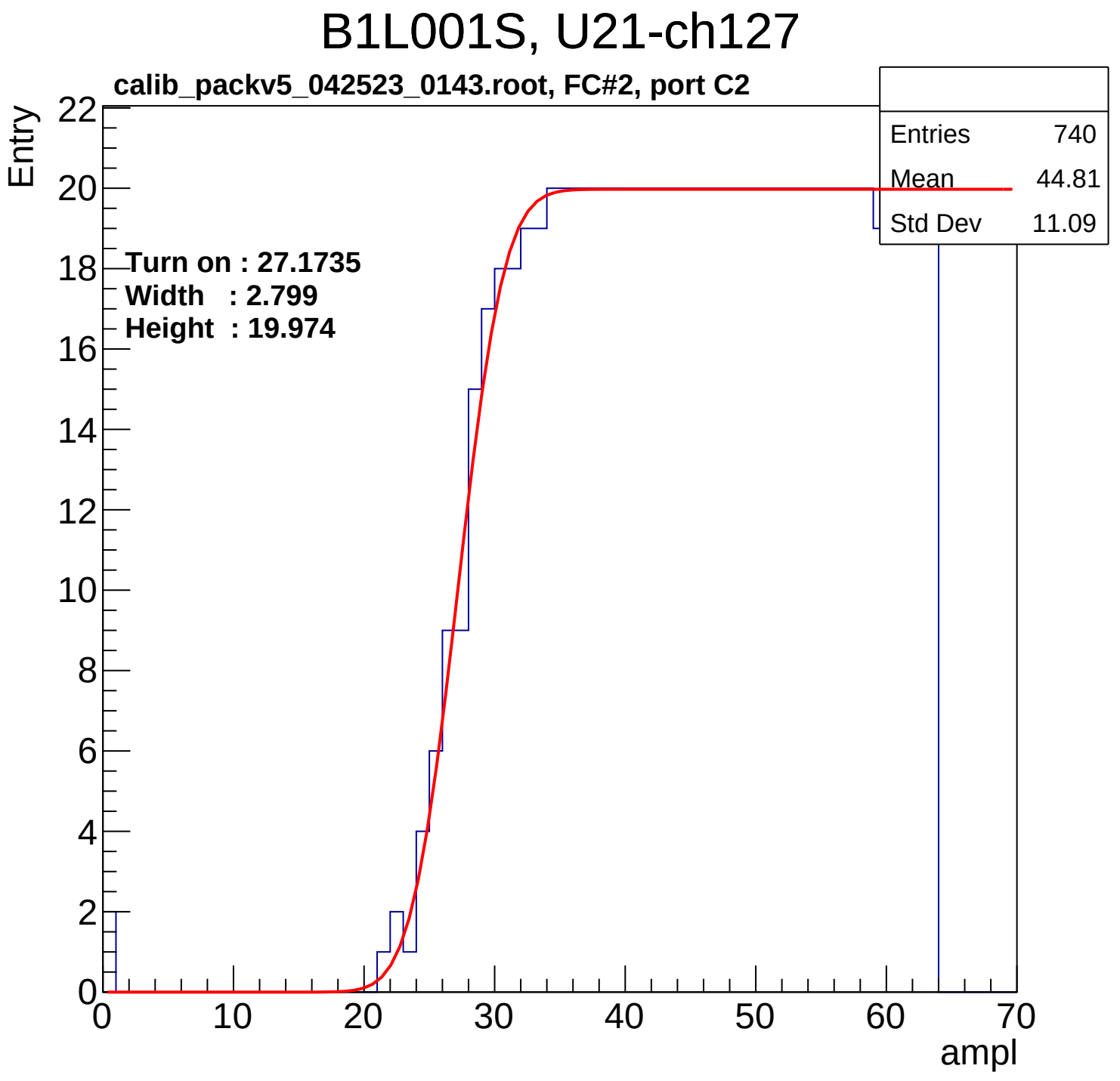
B1L001S, U21-ch127
calib_packv5_042523_0143.root, FC#2, port C2
Entries 740
Mean 44.81
Std Dev 11.09
Turn on : 27.1735
Width : 2.799
Height : 19.974
Entry
ampl
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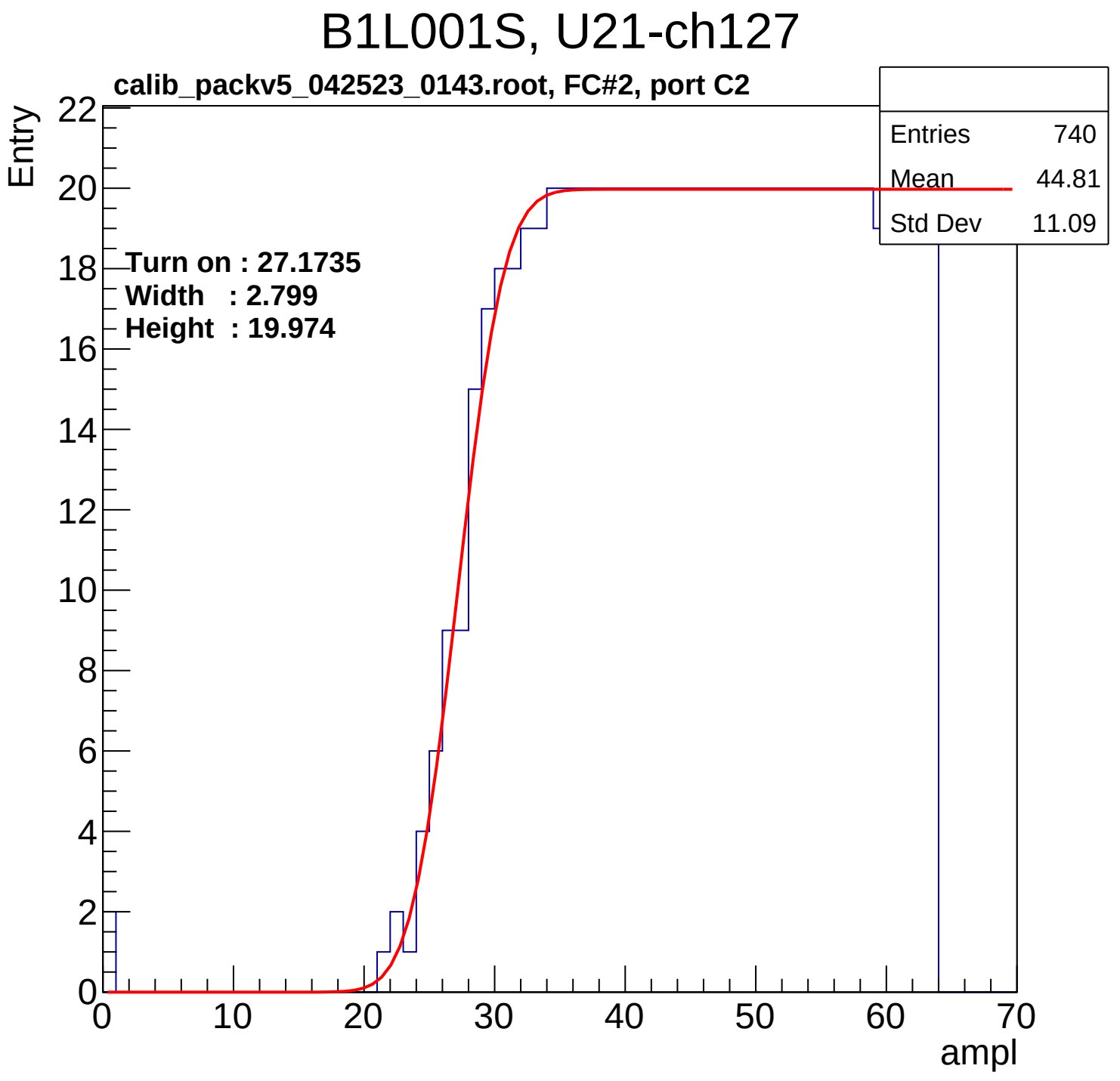
B1L001S, U21-ch127
calib_packv5_042523_0143.root, FC#2, port C2
Entries 740
Mean 44.81
Std Dev 11.09
Turn on : 27.1735
Width : 2.799
Height : 19.974
Entry
ampl
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6
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