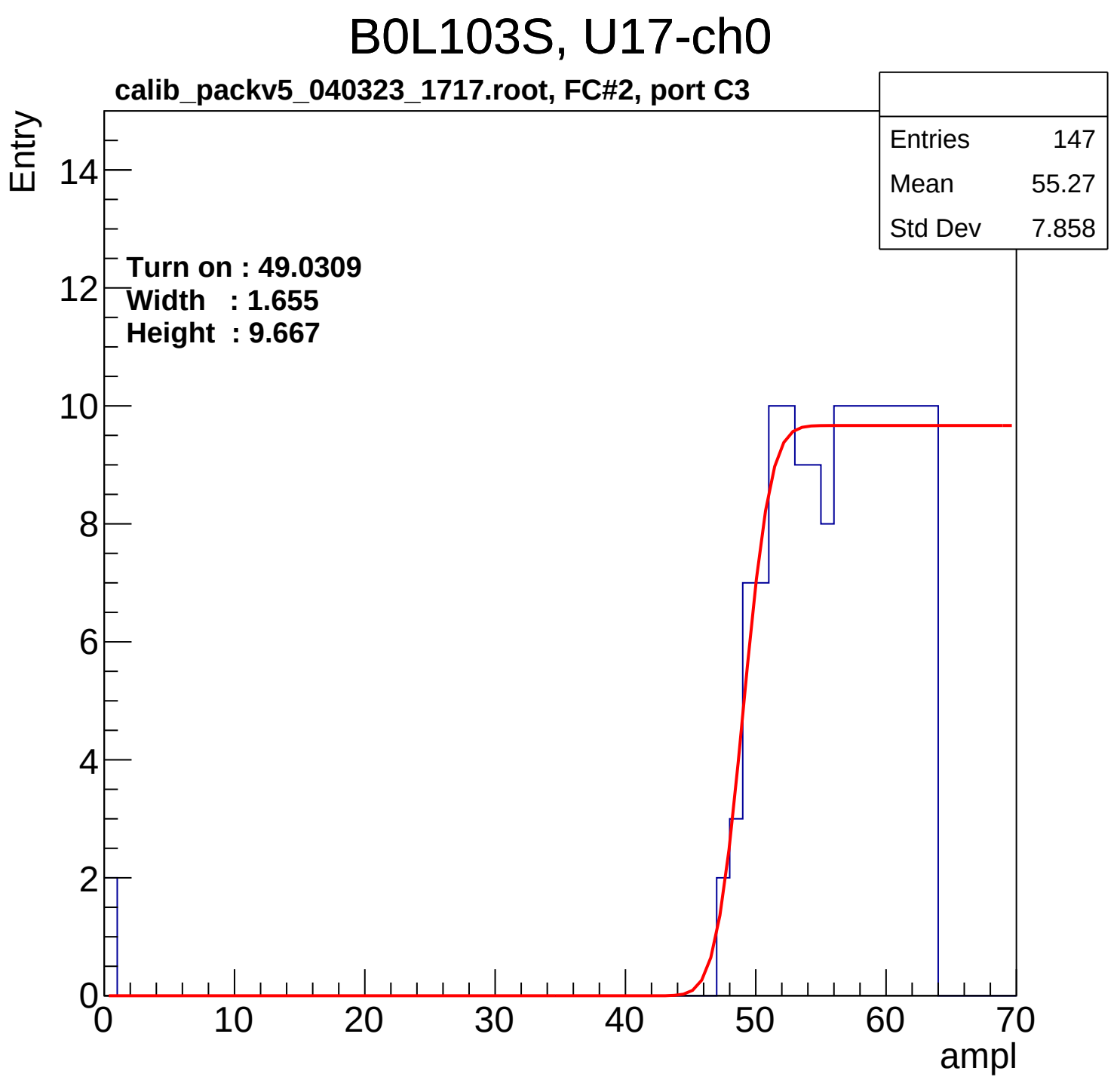
B0L103S, U17-ch0
calib_packv5_040323_1717.root, FC#2, port C3
Entries 147
Mean 55.27
Std Dev 7.858
Turn on : 49.0309
Width : 1.655
Height : 9.667
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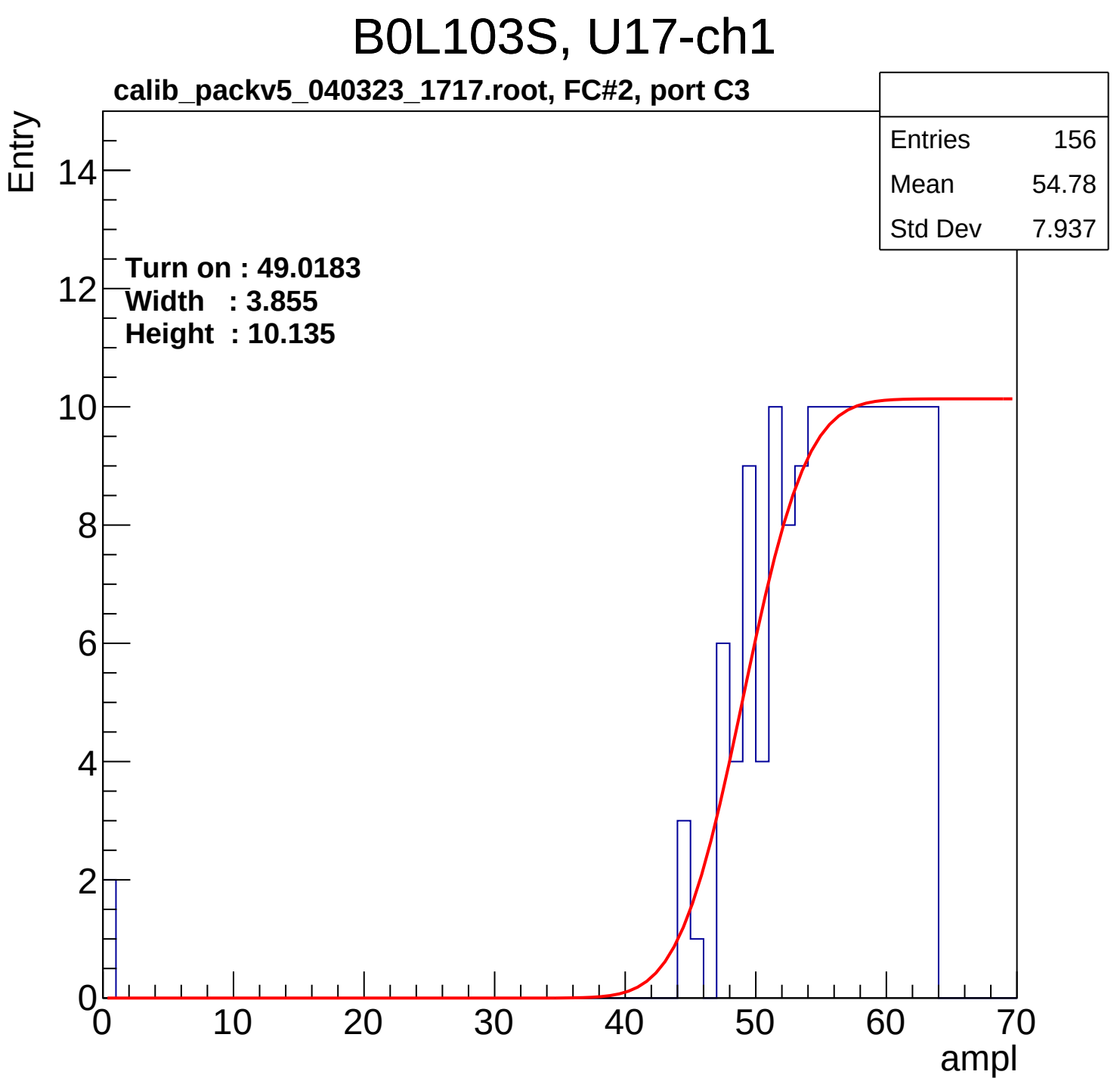
B0L103S, U17-ch1
calib_packv5_040323_1717.root, FC#2, port C3
Entries 156
Mean 54.78
Std Dev 7.937
Turn on : 49.0183
Width : 3.855
Height : 10.135
Entry
ampl
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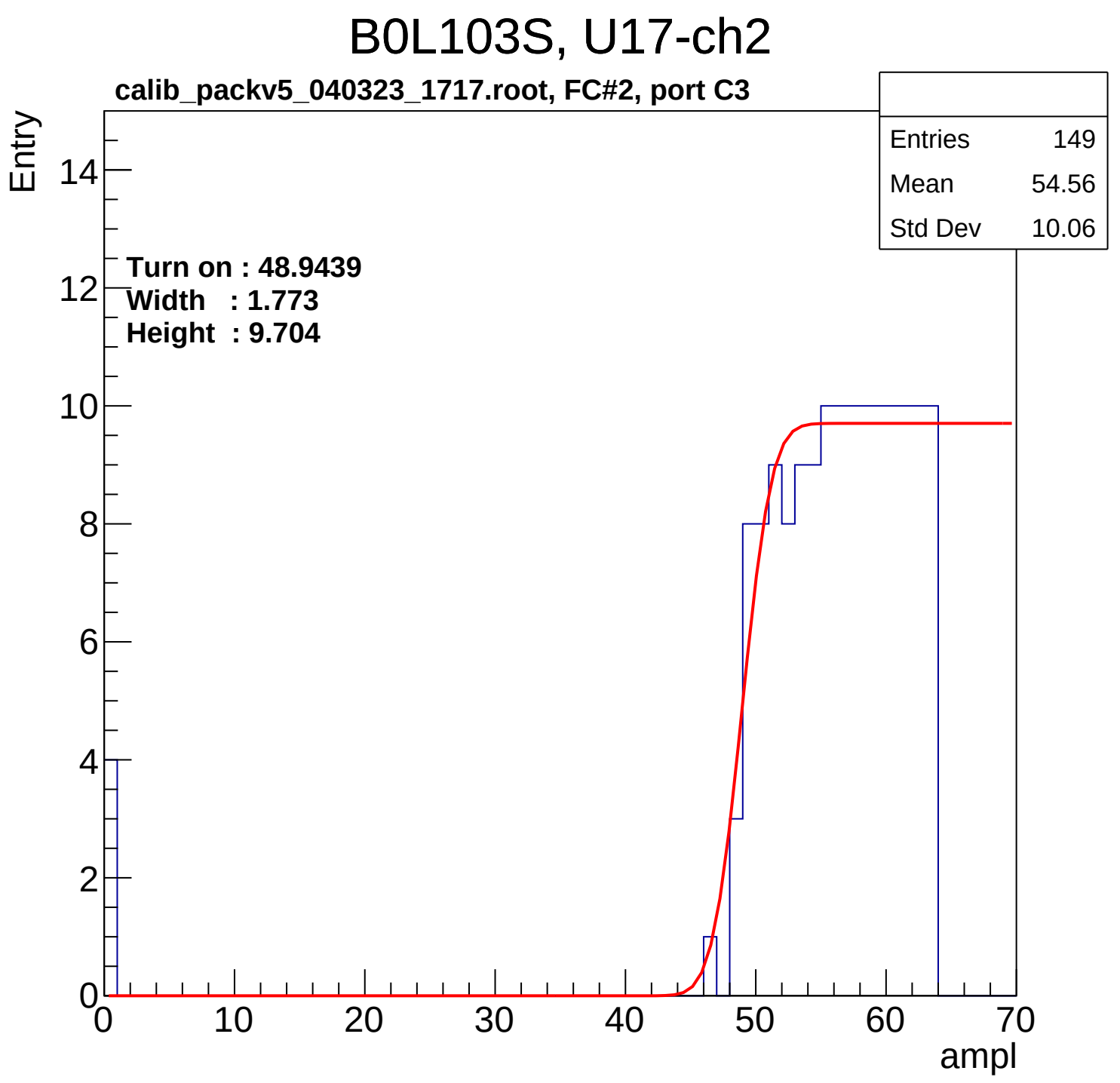
B0L103S, U17-ch2
calib_packv5_040323_1717.root, FC#2, port C3
Entries 149
Mean 54.56
Std Dev 10.06
Turn on : 48.9439
Width : 1.773
Height : 9.704
Entry
ampl
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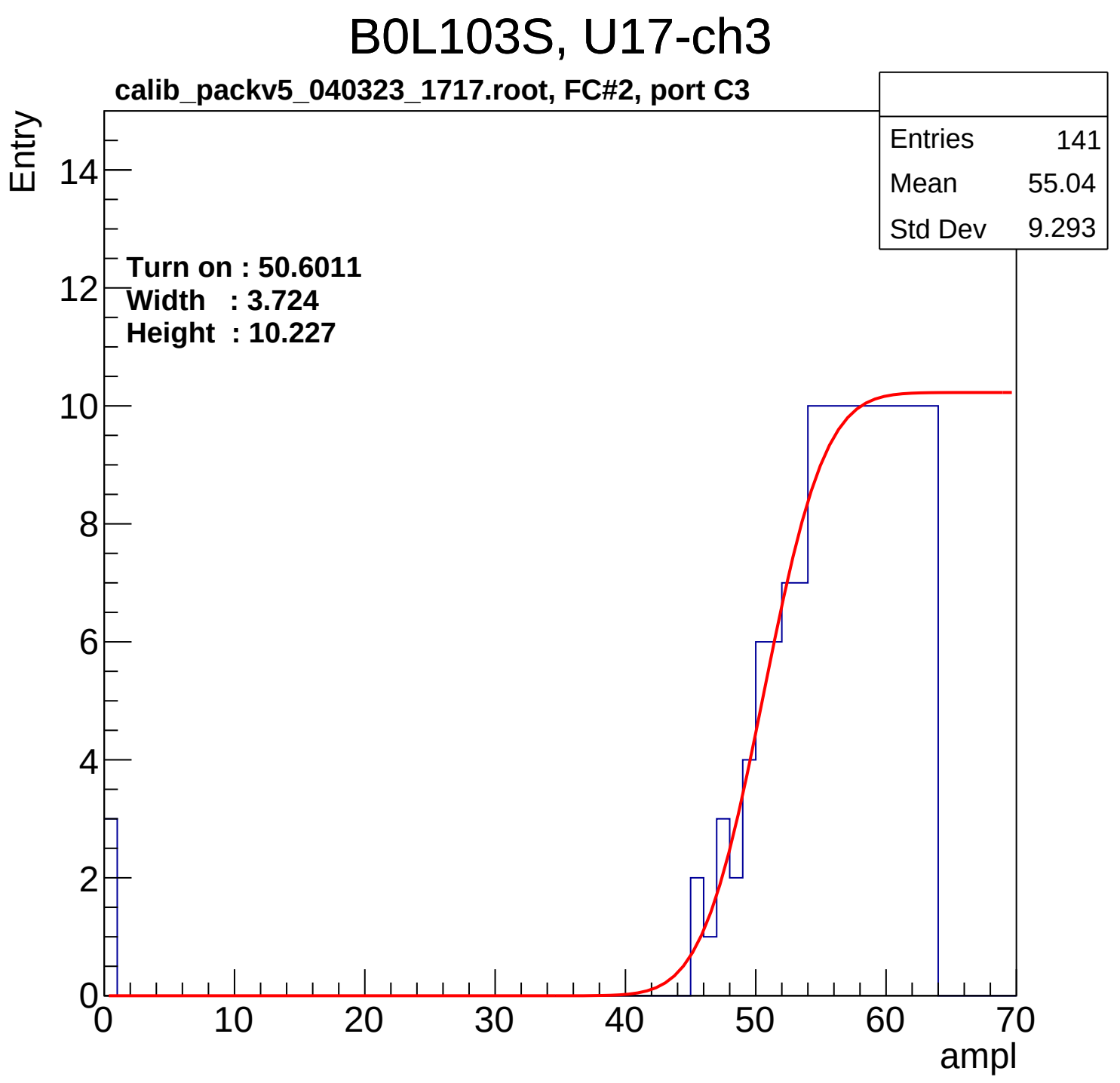
B0L103S, U17-ch3
calib_packv5_040323_1717.root, FC#2, port C3
Entries 141
Mean 55.04
Std Dev 9.293
Turn on : 50.6011
Width : 3.724
Height : 10.227
Entry
ampl
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6
8
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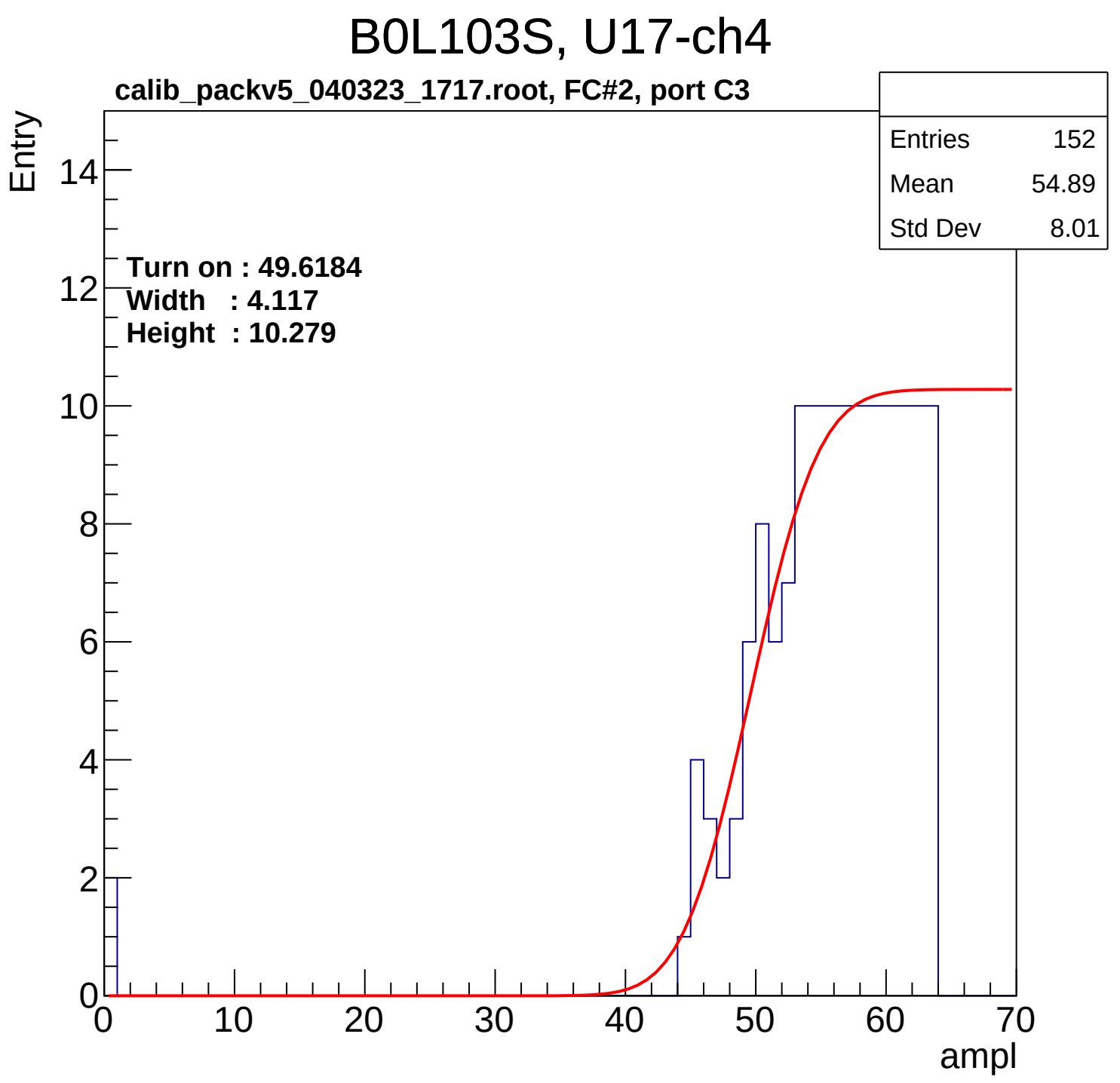
B0L103S, U17-ch4
calib_packv5_040323_1717.root, FC#2, port C3
Entries 152
Mean 54.89
Std Dev 8.01
Turn on : 49.6184
Width : 4.117
Height : 10.279
Entry
ampl
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4
6
8
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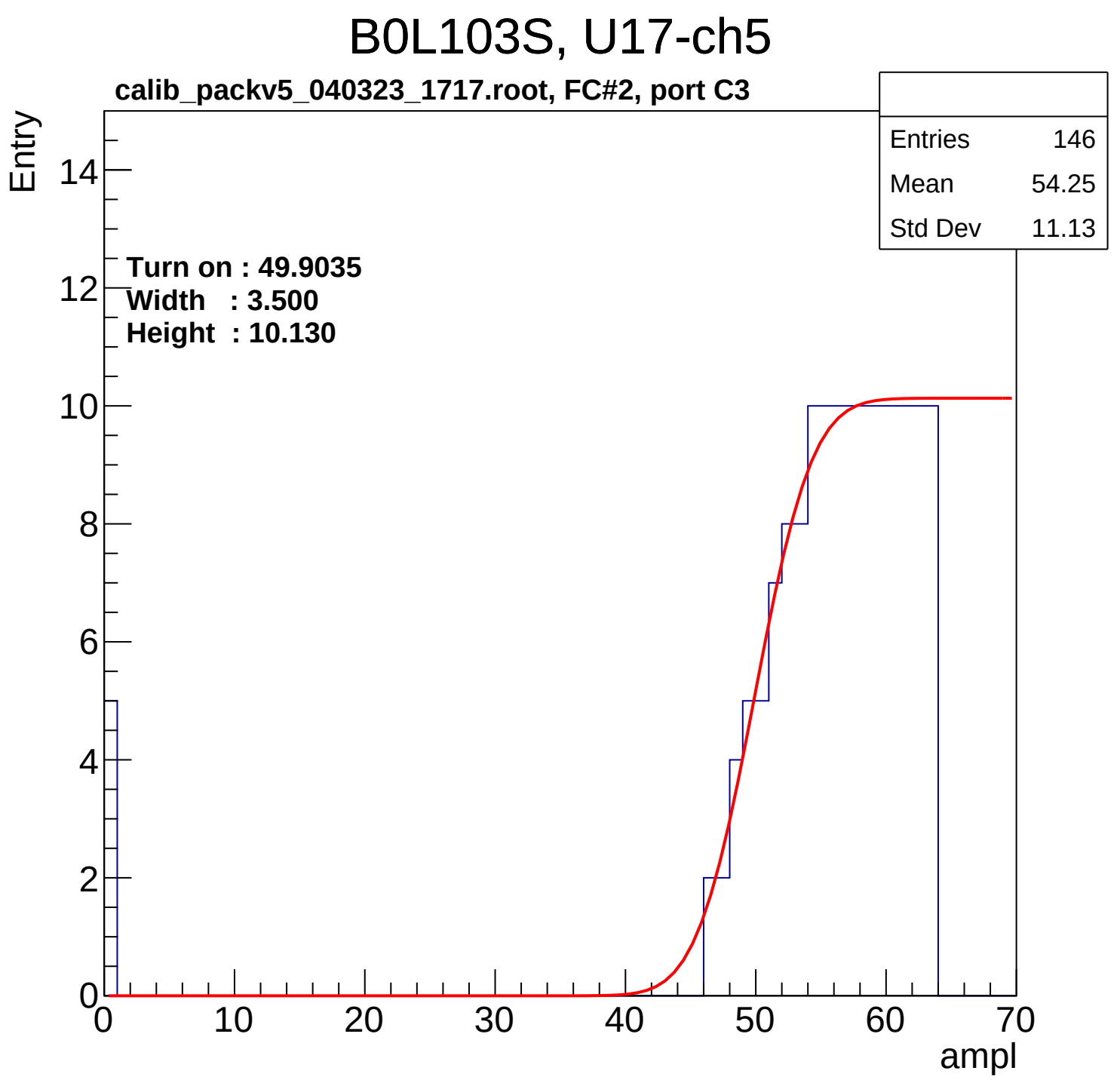
B0L103S, U17-ch5
calib_packv5_040323_1717.root, FC#2, port C3
Entries 146
Mean 54.25
Std Dev 11.13
Turn on : 49.9035
Width : 3.500
Height : 10.130
Entry
ampl
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2
4
6
8
10
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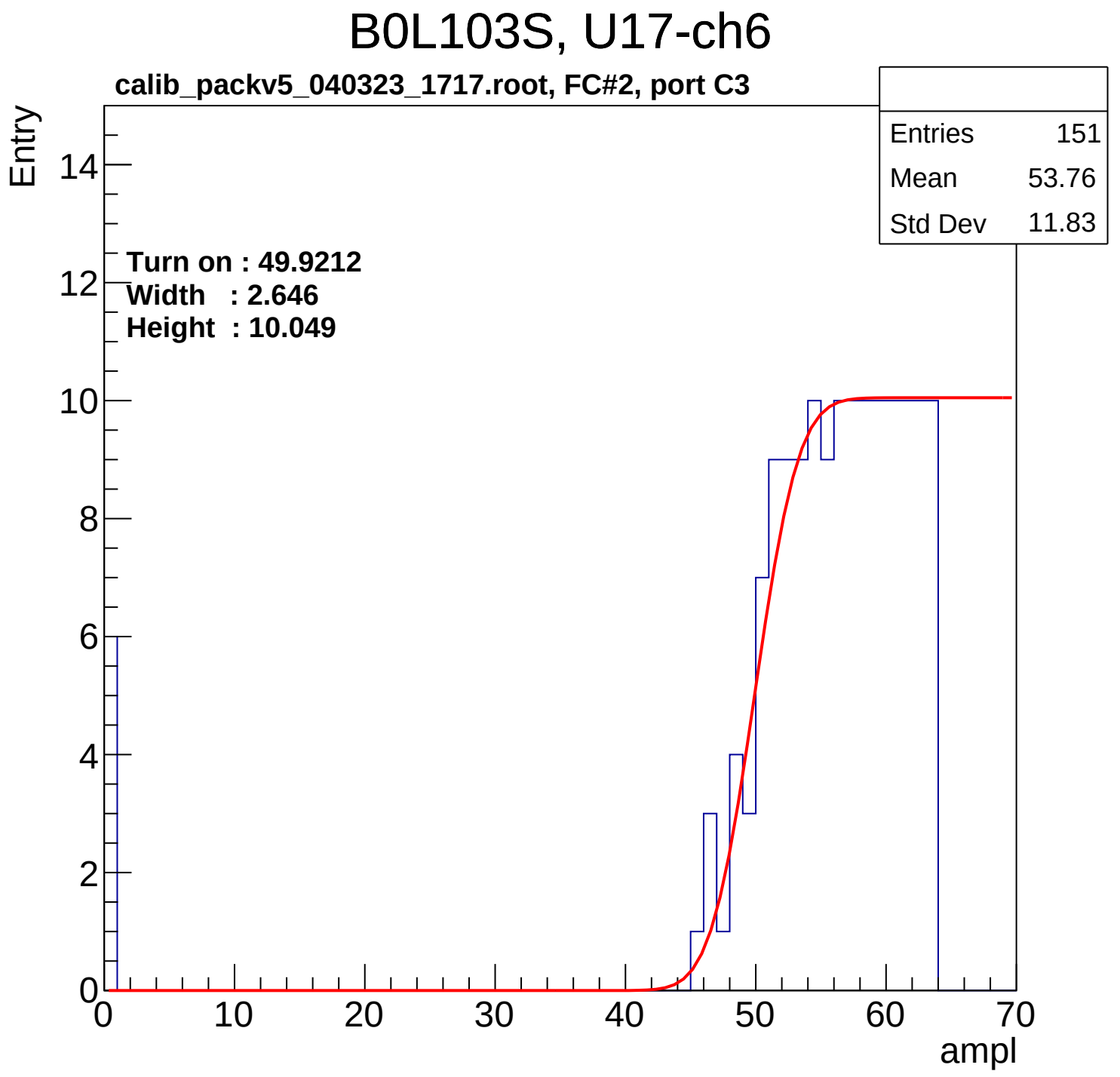
B0L103S, U17-ch6
calib_packv5_040323_1717.root, FC#2, port C3
Entries 151
Mean 53.76
Std Dev 11.83
Turn on : 49.9212
Width : 2.646
Height : 10.049
Entry
ampl
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2
4
6
8
10
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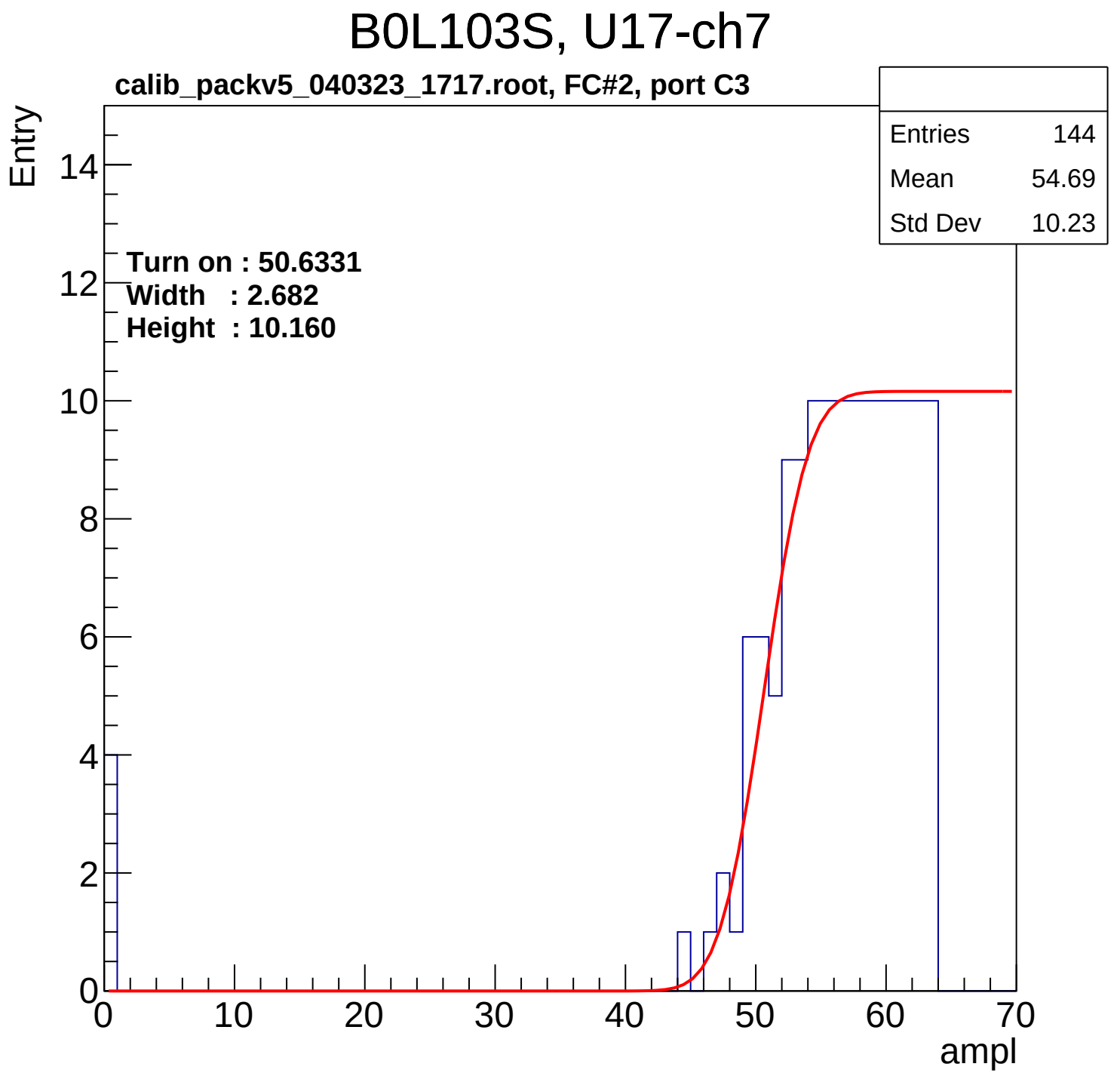
B0L103S, U17-ch7
calib_packv5_040323_1717.root, FC#2, port C3
Entries 144
Mean 54.69
Std Dev 10.23
Turn on : 50.6331
Width : 2.682
Height : 10.160
Entry
ampl
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2
4
6
8
10
12
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20
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60
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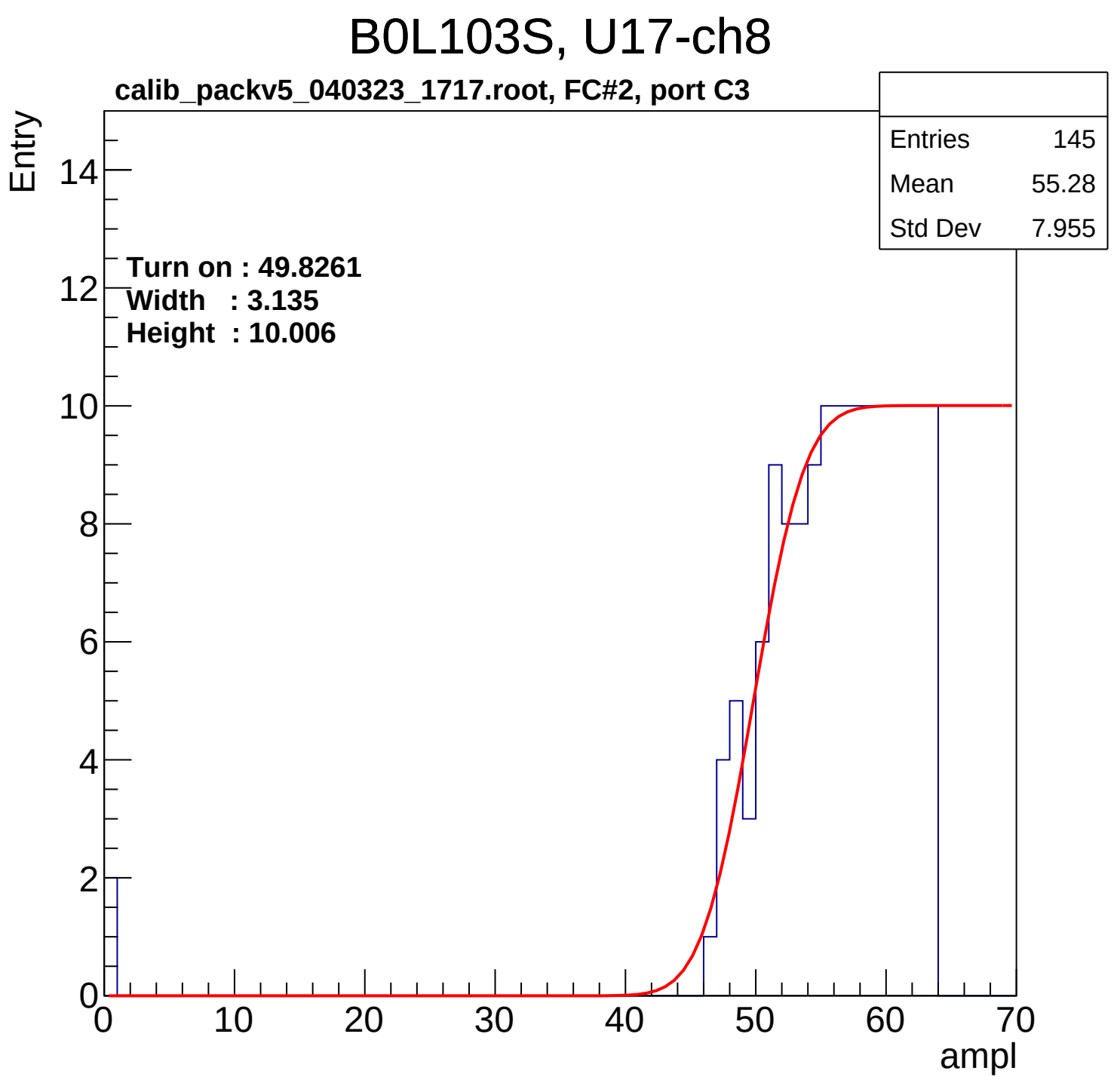
B0L103S, U17-ch8
calib_packv5_040323_1717.root, FC#2, port C3
Entries 145
Mean 55.28
Std Dev 7.955
Turn on : 49.8261
Width : 3.135
Height : 10.006
Entry
ampl
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6
8
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0
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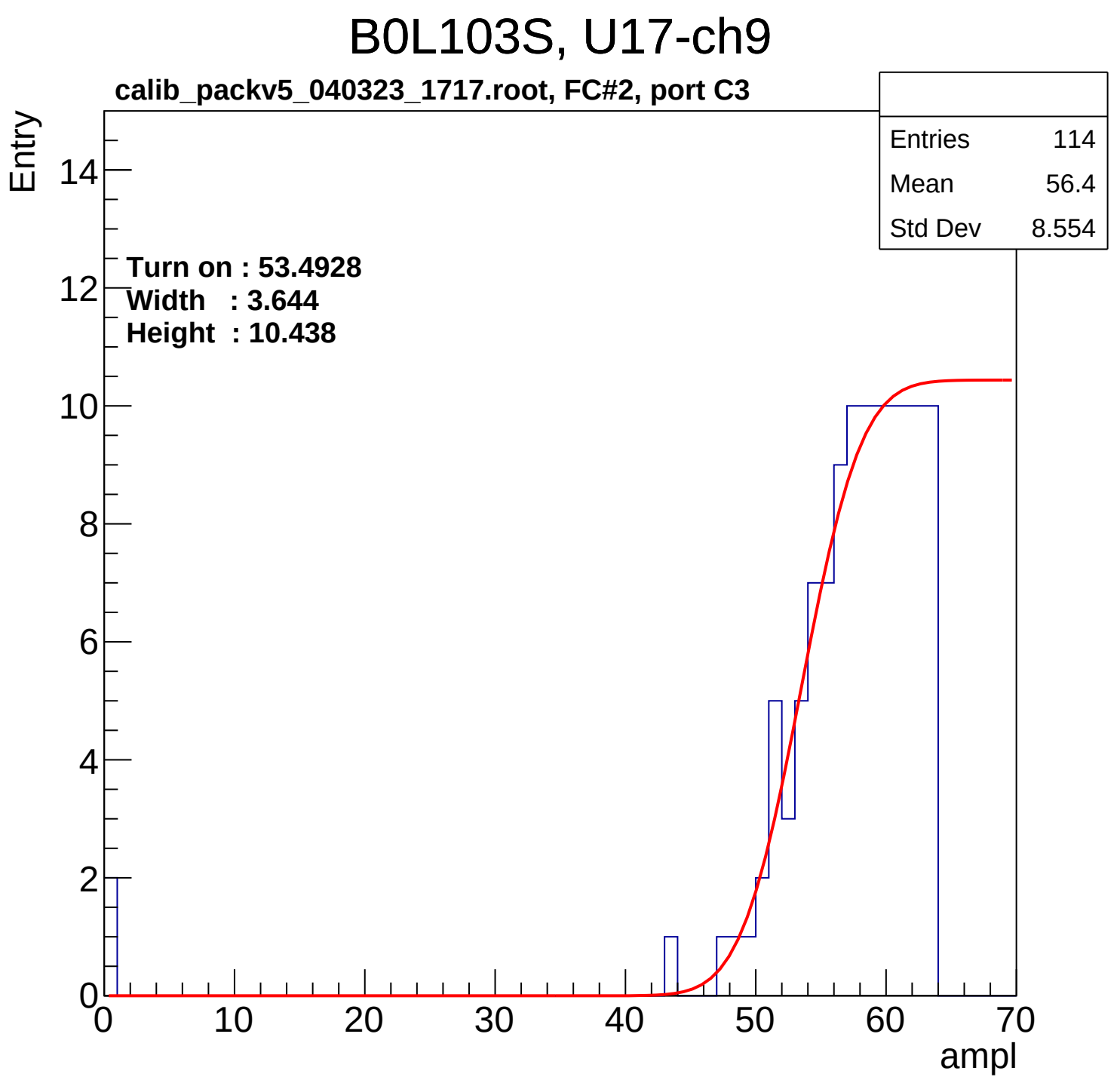
B0L103S, U17-ch9
calib_packv5_040323_1717.root, FC#2, port C3
Entries 114
Mean 56.4
Std Dev 8.554
Turn on : 53.4928
Width : 3.644
Height : 10.438
Entry
ampl
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6
8
10
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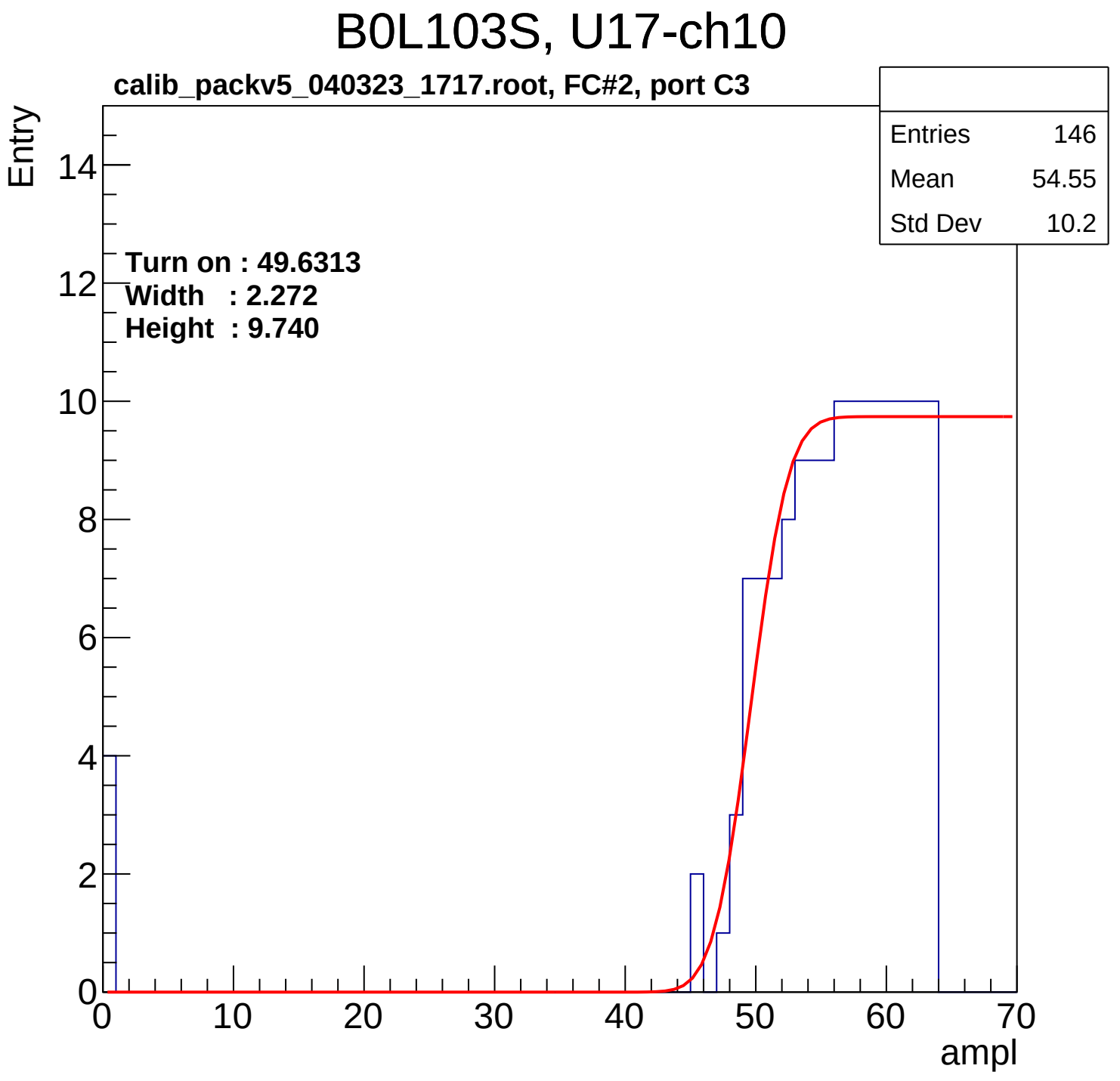
B0L103S, U17-ch10
calib_packv5_040323_1717.root, FC#2, port C3
Entries 146
Mean 54.55
Std Dev 10.2
Turn on : 49.6313
Width : 2.272
Height : 9.740
Entry
ampl
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6
8
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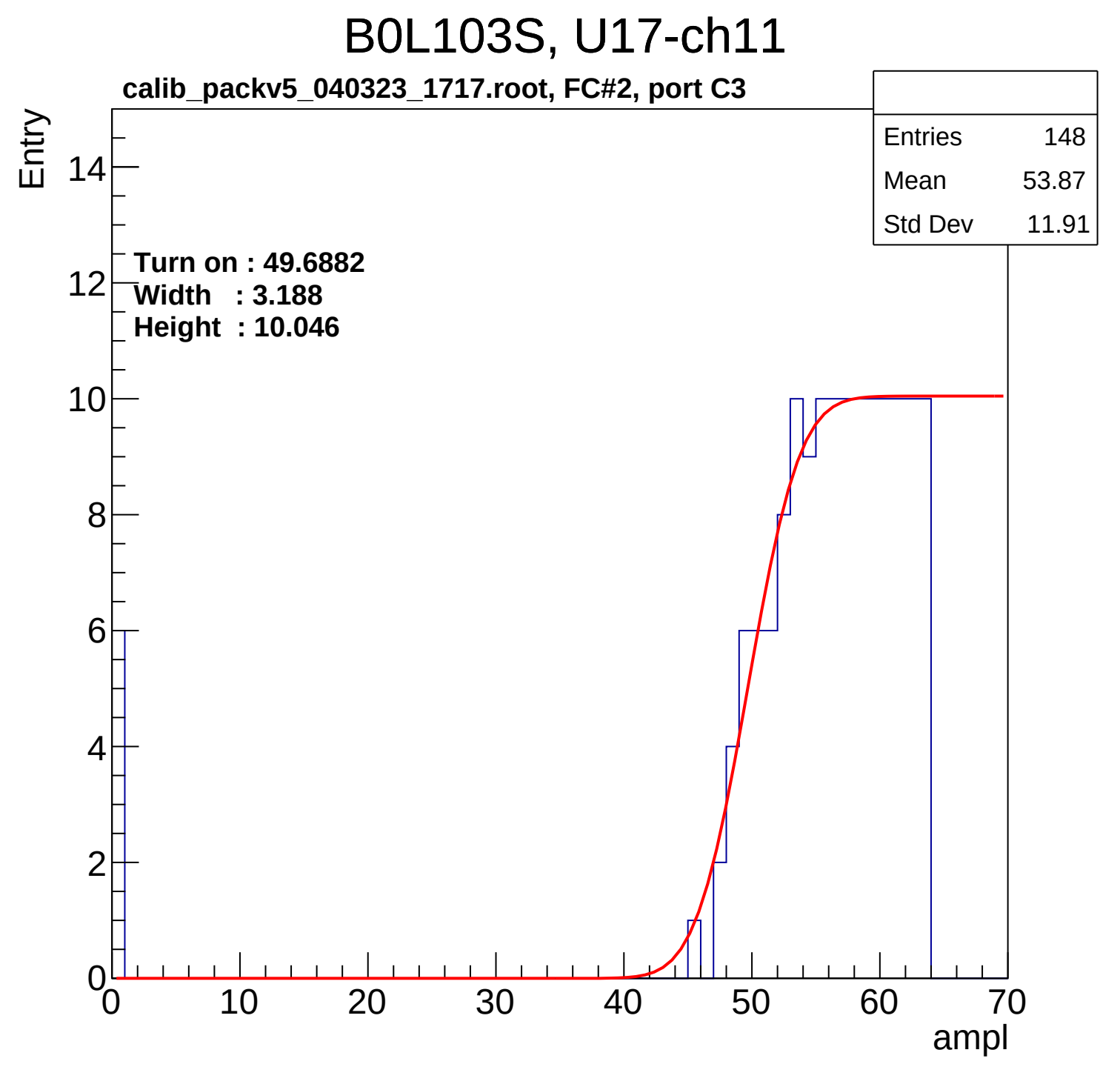
B0L103S, U17-ch11
calib_packv5_040323_1717.root, FC#2, port C3
Entries 148
Mean 53.87
Std Dev 11.91
Turn on : 49.6882
Width : 3.188
Height : 10.046
Entry
ampl
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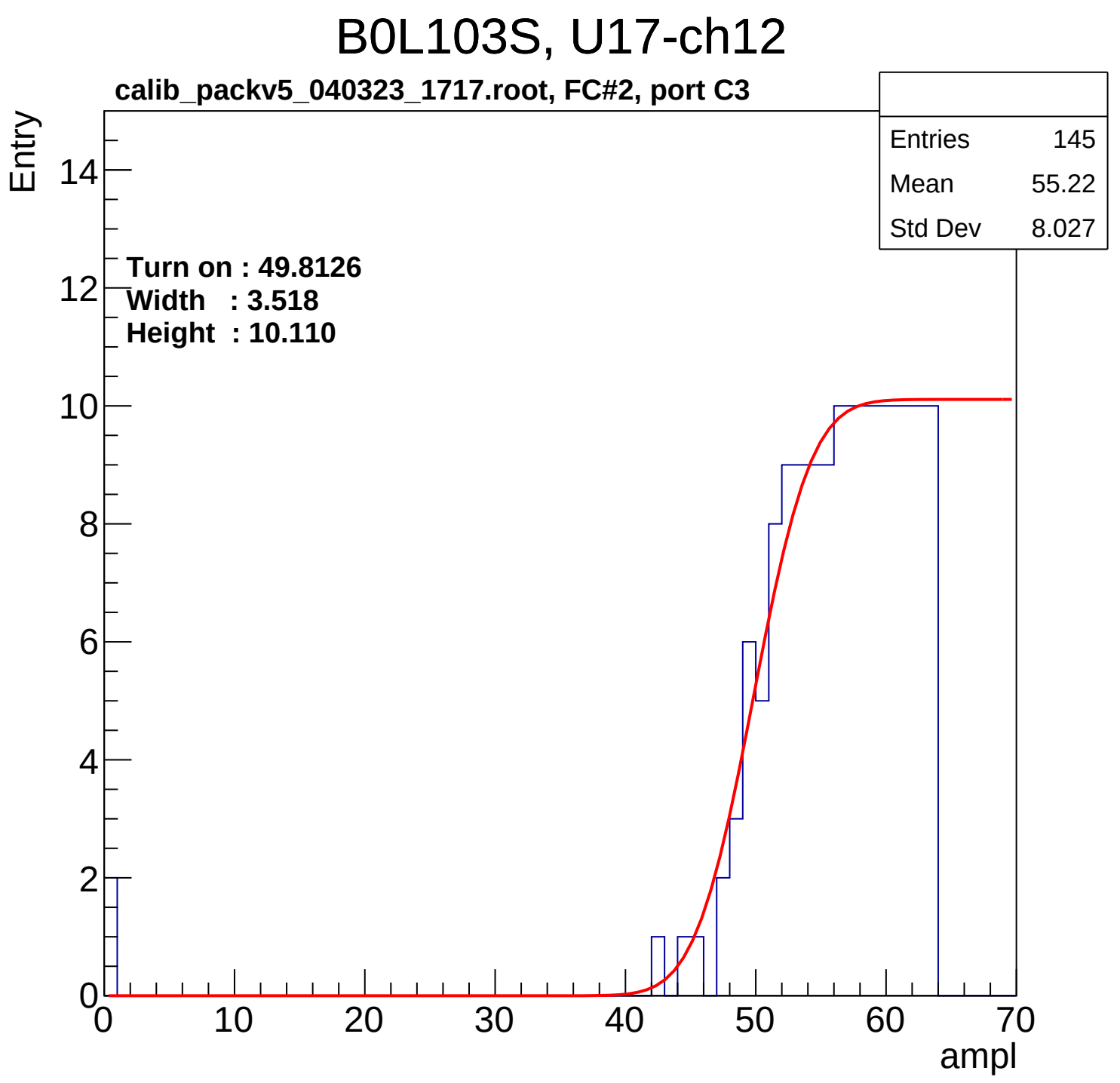
B0L103S, U17-ch12
calib_packv5_040323_1717.root, FC#2, port C3
Entries 145
Mean 55.22
Std Dev 8.027
Turn on : 49.8126
Width : 3.518
Height : 10.110
Entry
ampl
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6
8
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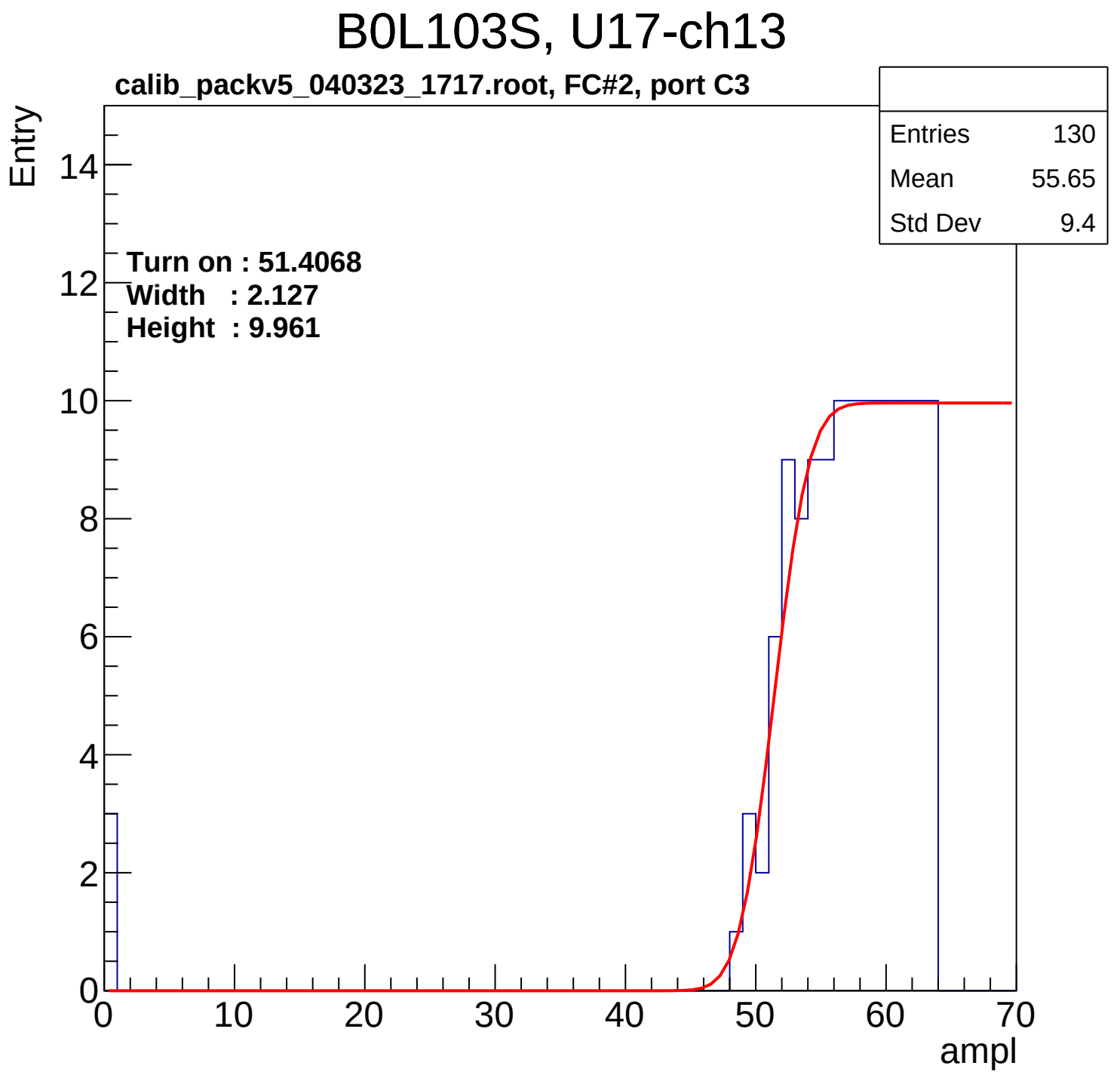
B0L103S, U17-ch13
calib_packv5_040323_1717.root, FC#2, port C3
Entries 130
Mean 55.65
Std Dev 9.4
Turn on : 51.4068
Width : 2.127
Height : 9.961
Entry
ampl
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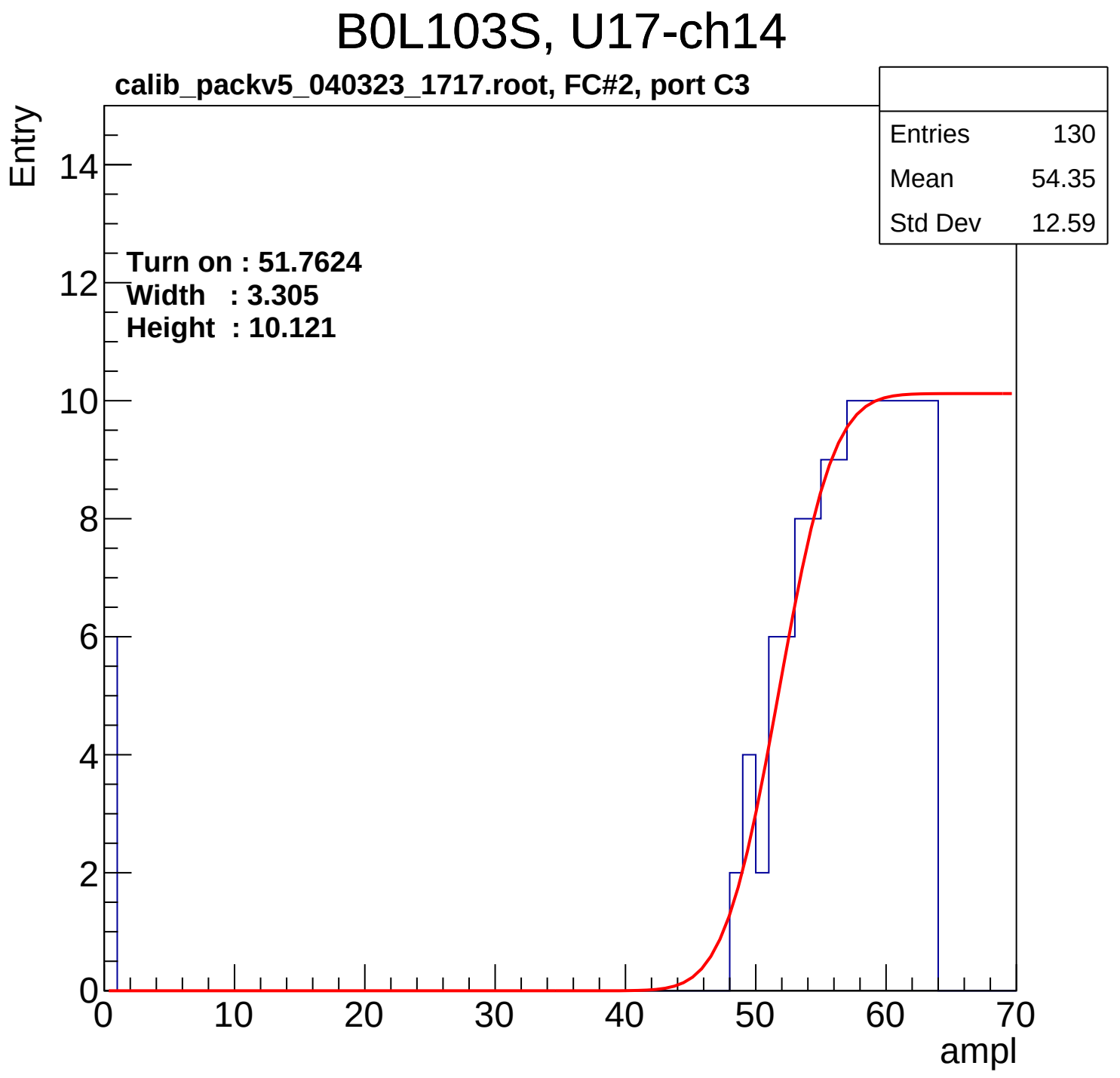
B0L103S, U17-ch14
calib_packv5_040323_1717.root, FC#2, port C3
Entries 130
Mean 54.35
Std Dev 12.59
Turn on : 51.7624
Width : 3.305
Height : 10.121
Entry
ampl
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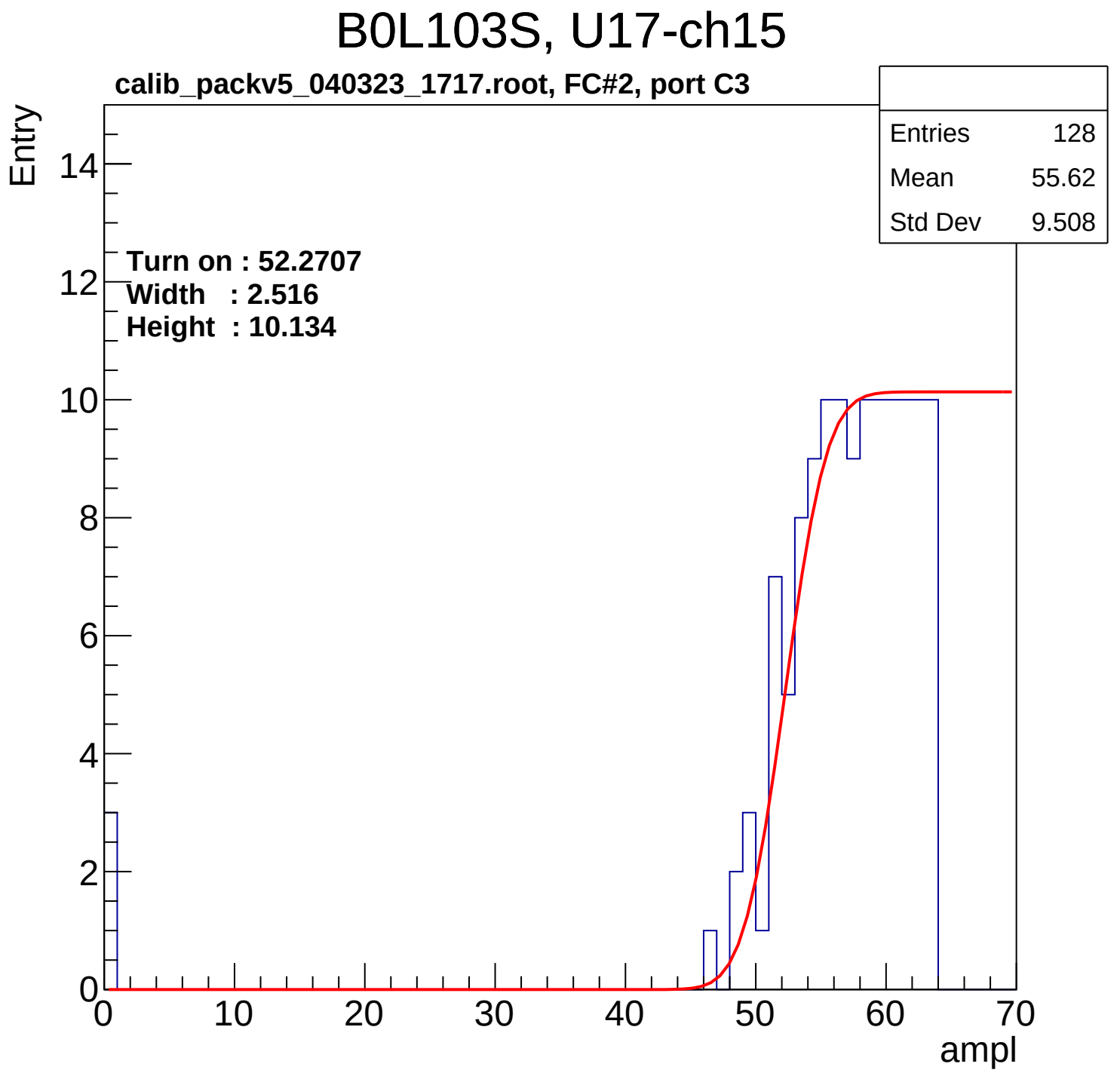
B0L103S, U17-ch15
calib_packv5_040323_1717.root, FC#2, port C3
Entries 128
Mean 55.62
Std Dev 9.508
Turn on : 52.2707
Width : 2.516
Height : 10.134
Entry
ampl
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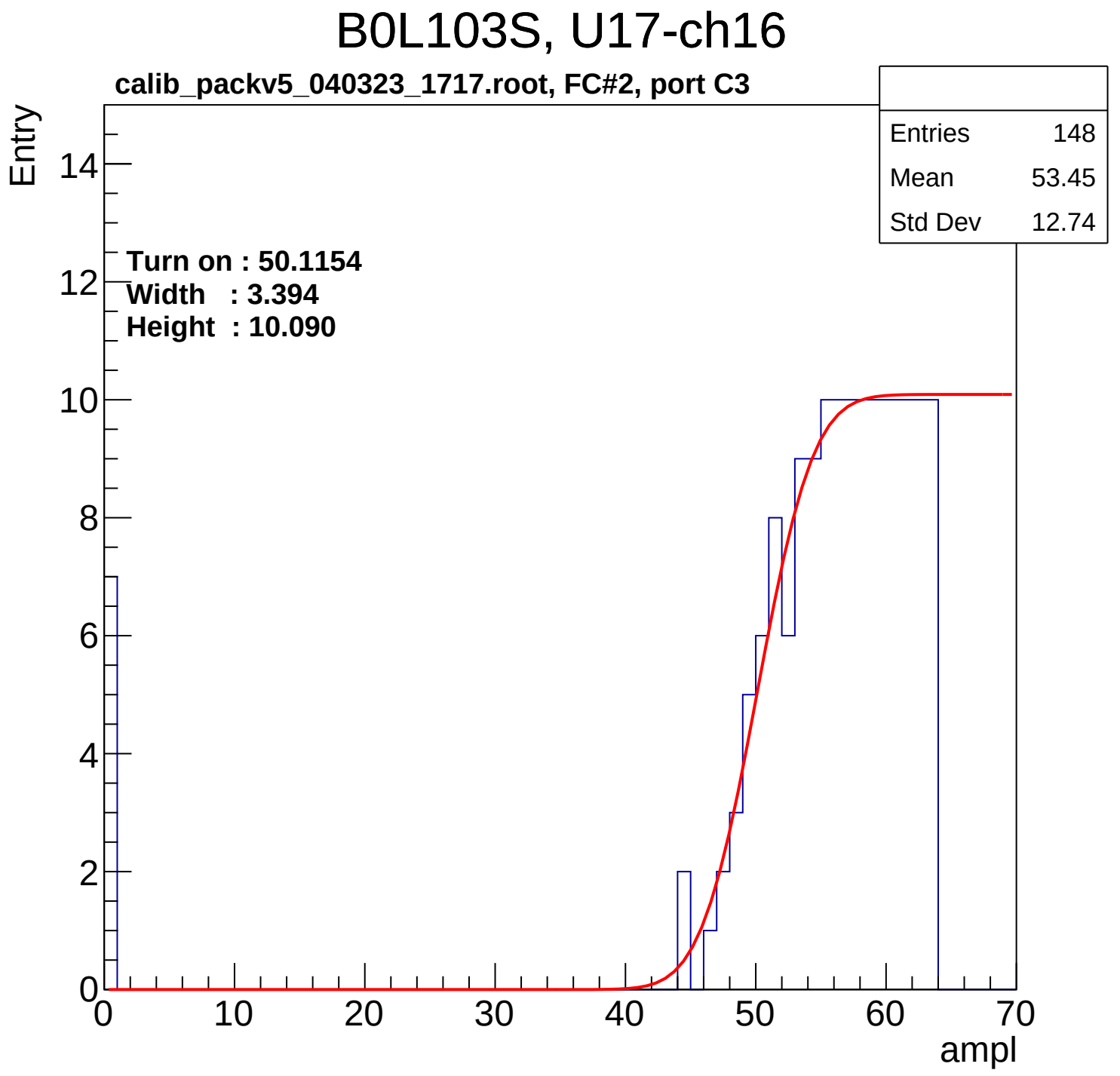
B0L103S, U17-ch16
calib_packv5_040323_1717.root, FC#2, port C3
Entries 148
Mean 53.45
Std Dev 12.74
Turn on : 50.1154
Width : 3.394
Height : 10.090
Entry
ampl
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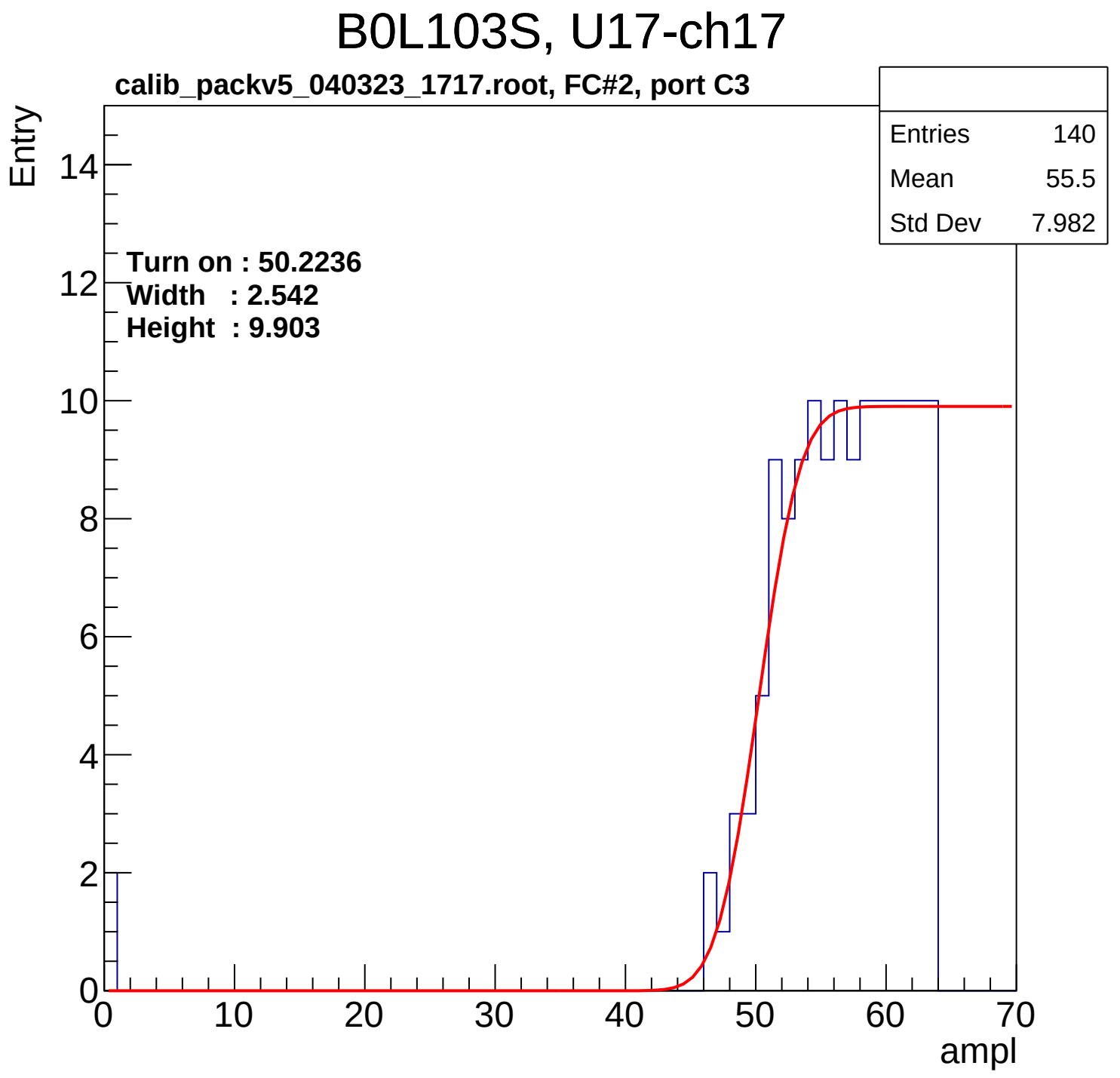
B0L103S, U17-ch17
calib_packv5_040323_1717.root, FC#2, port C3
Entries 140
Mean 55.5
Std Dev 7.982
Turn on : 50.2236
Width : 2.542
Height : 9.903
Entry
ampl
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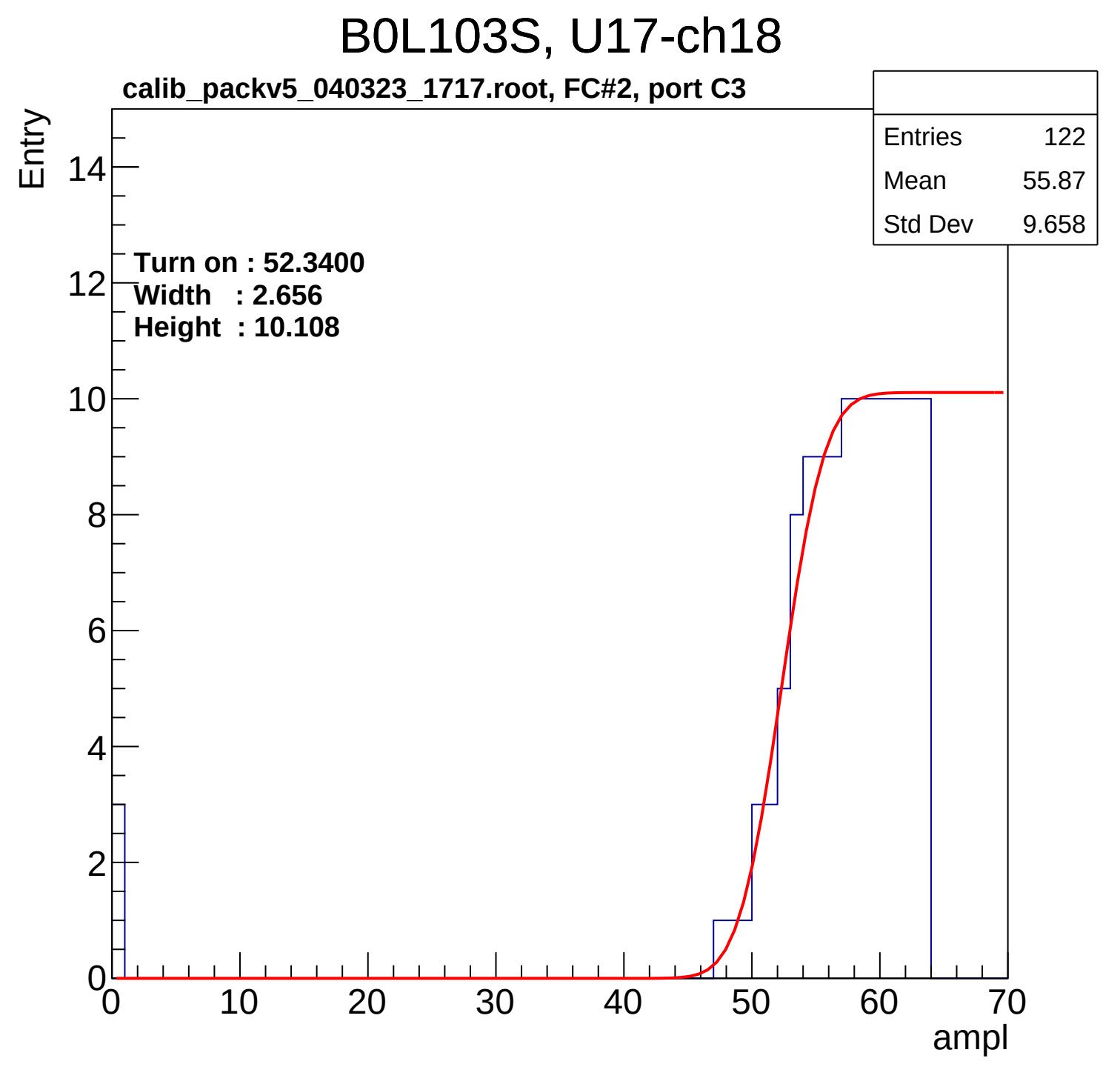
B0L103S, U17-ch18
calib_packv5_040323_1717.root, FC#2, port C3
Entries 122
Mean 55.87
Std Dev 9.658
Turn on : 52.3400
Width : 2.656
Height : 10.108
Entry
ampl
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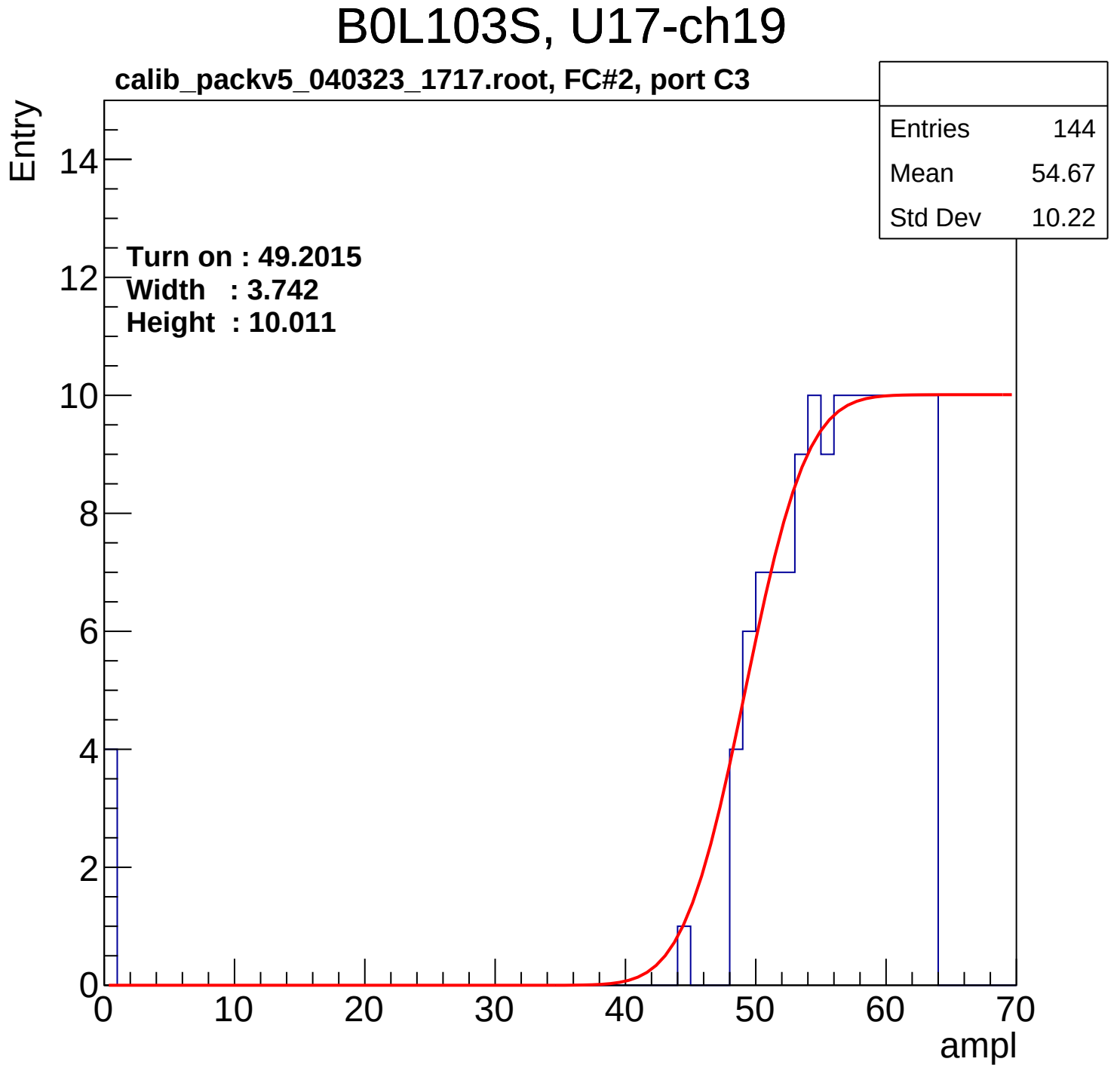
B0L103S, U17-ch19
calib_packv5_040323_1717.root, FC#2, port C3
Entries 144
Mean 54.67
Std Dev 10.22
Turn on : 49.2015
Width : 3.742
Height : 10.011
Entry
ampl
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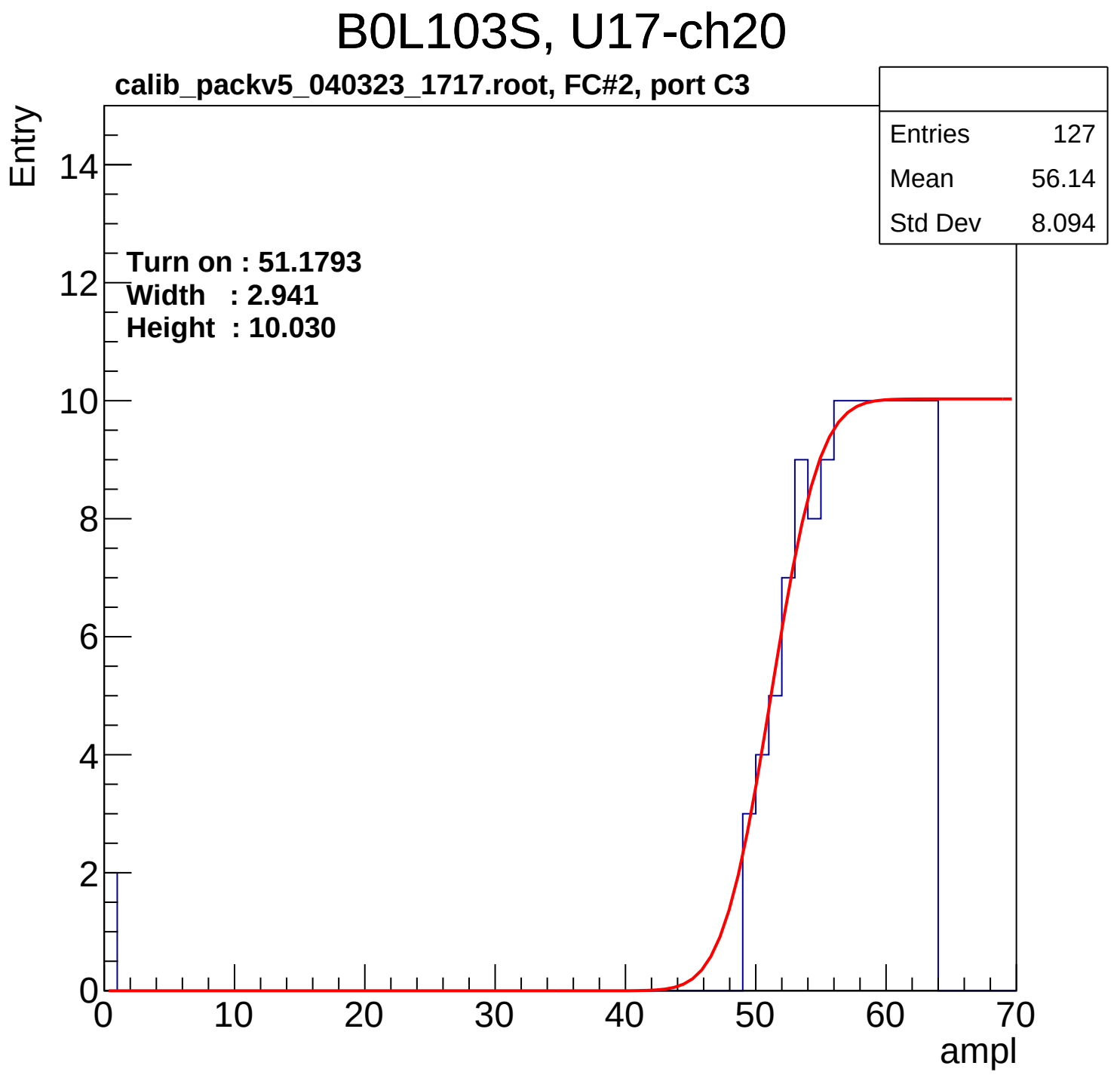
B0L103S, U17-ch20
calib_packv5_040323_1717.root, FC#2, port C3
Entries 127
Mean 56.14
Std Dev 8.094
Turn on : 51.1793
Width : 2.941
Height : 10.030
Entry
ampl
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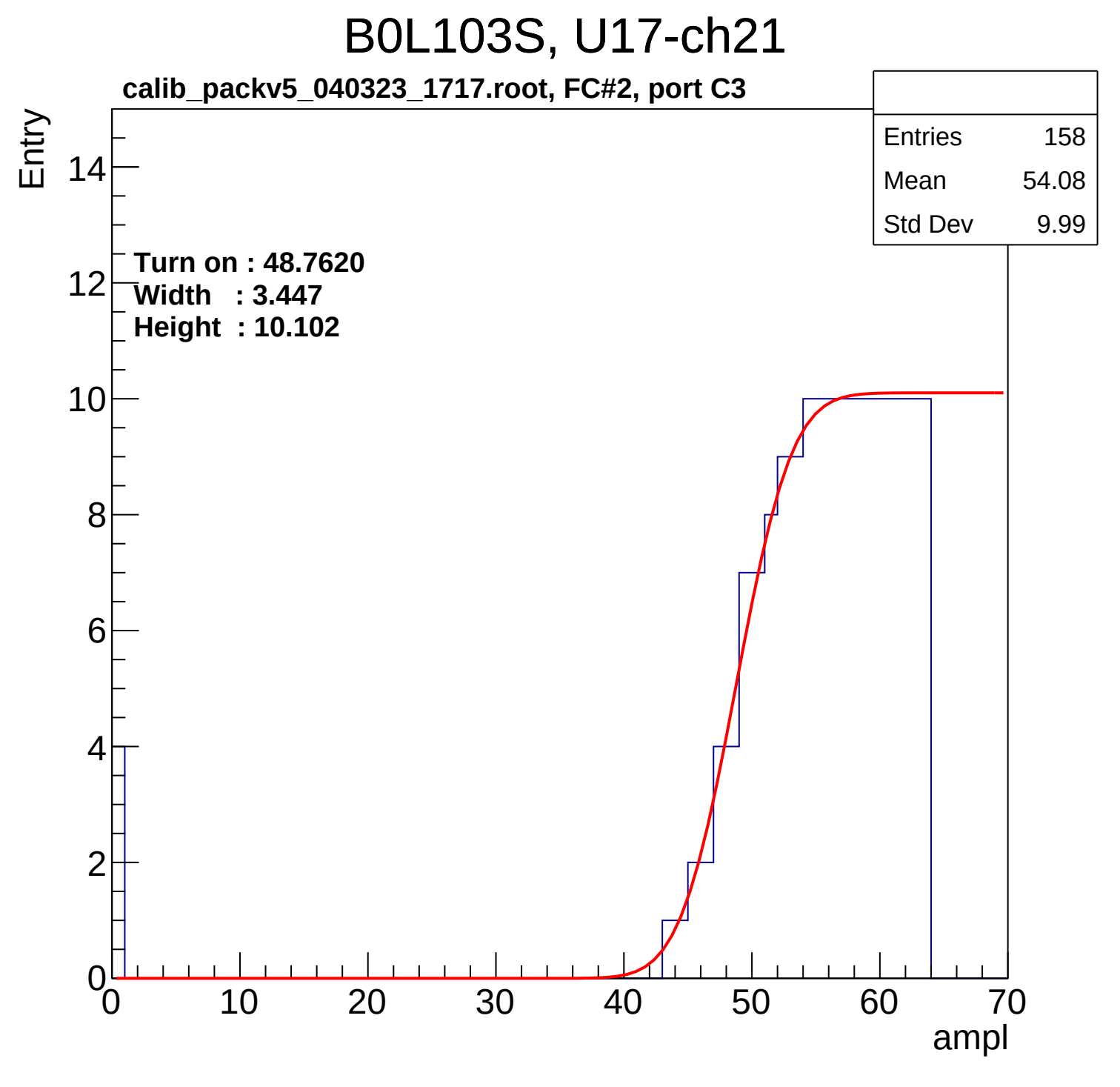
B0L103S, U17-ch21
calib_packv5_040323_1717.root, FC#2, port C3
Entries 158
Mean 54.08
Std Dev 9.99
Turn on : 48.7620
Width : 3.447
Height : 10.102
Entry
ampl
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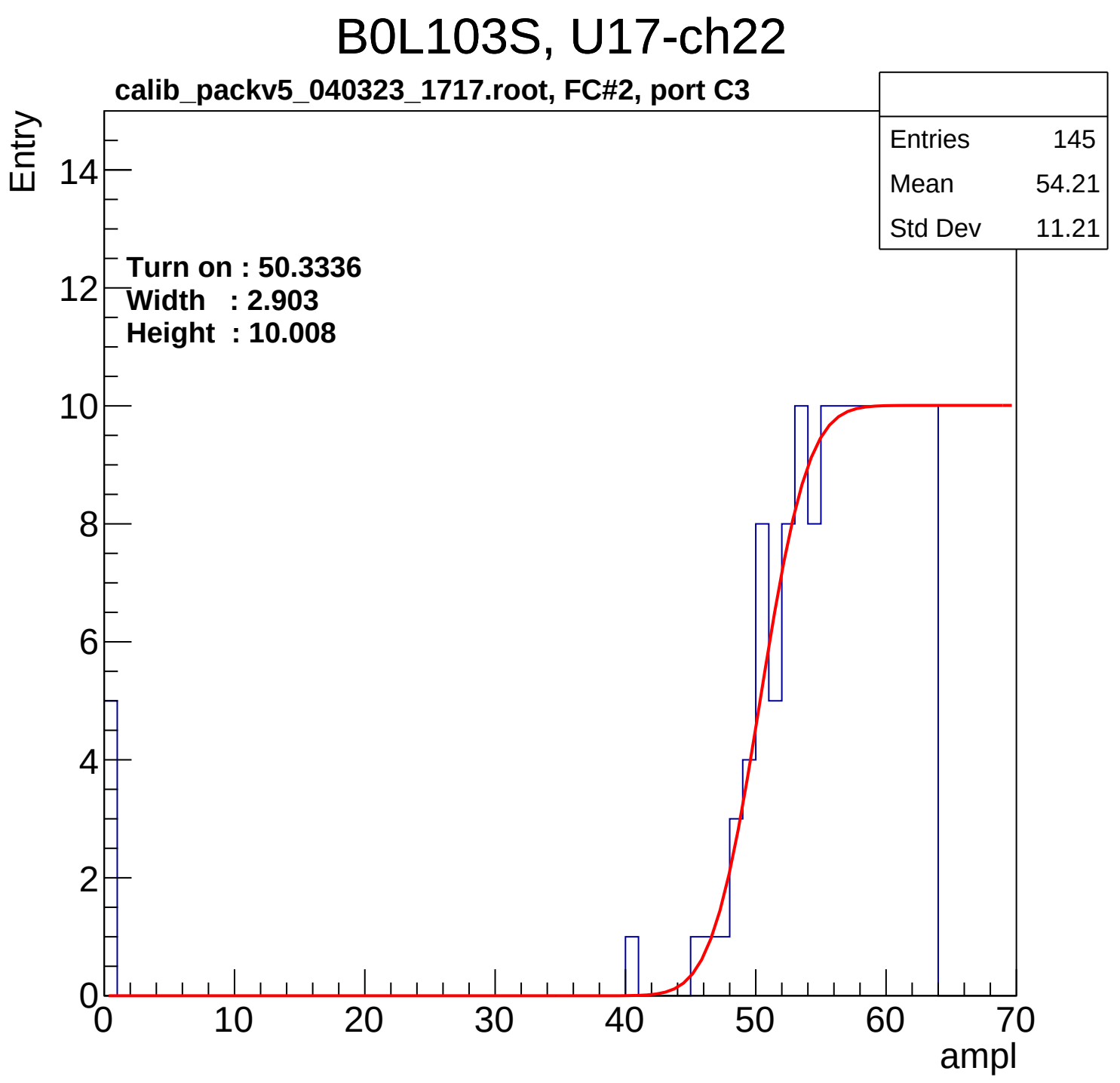
B0L103S, U17-ch22
calib_packv5_040323_1717.root, FC#2, port C3
Entries 145
Mean 54.21
Std Dev 11.21
Turn on : 50.3336
Width : 2.903
Height : 10.008
Entry
ampl
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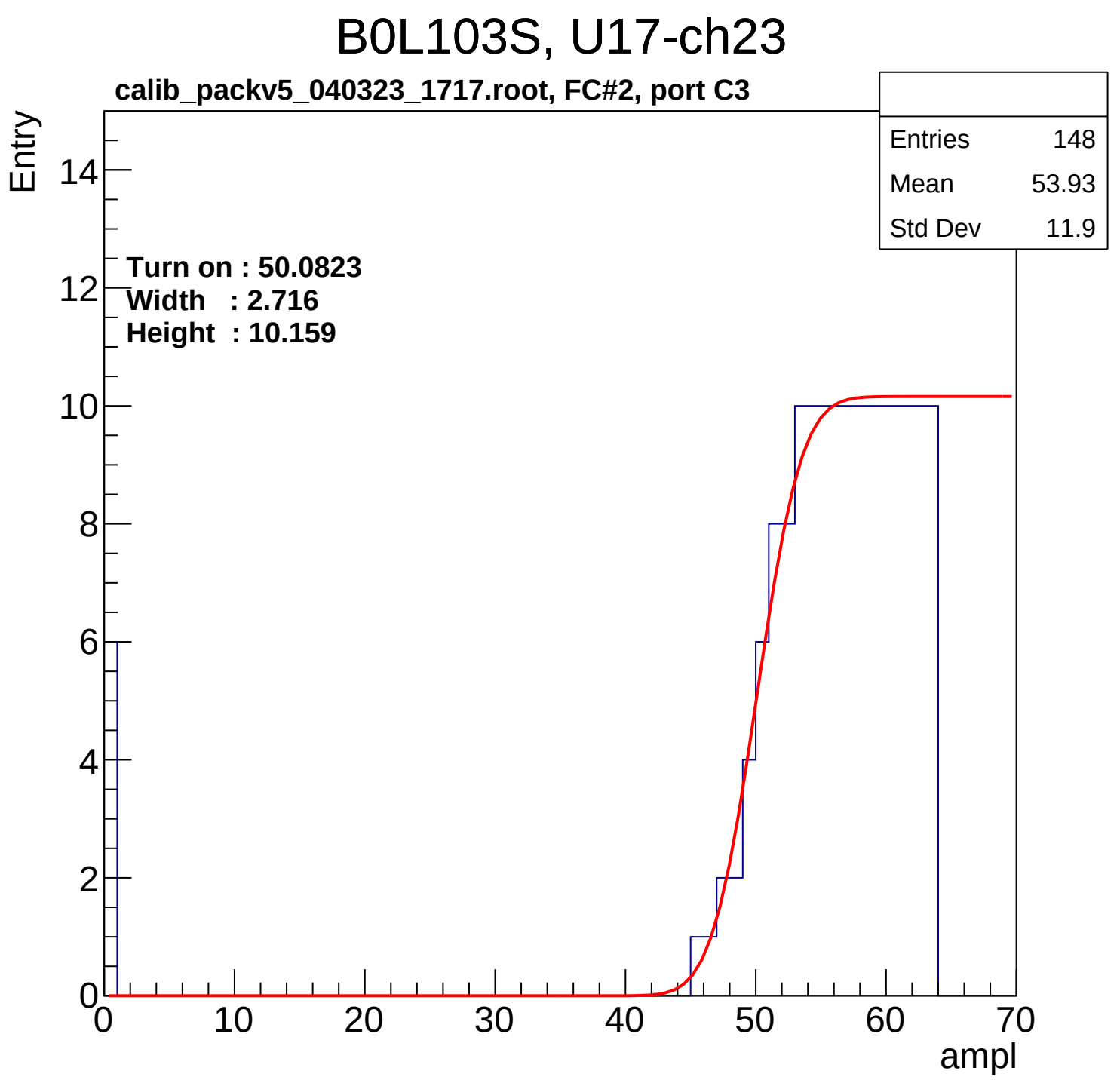
B0L103S, U17-ch23
calib_packv5_040323_1717.root, FC#2, port C3
Entries 148
Mean 53.93
Std Dev 11.9
Turn on : 50.0823
Width : 2.716
Height : 10.159
Entry
ampl
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6
8
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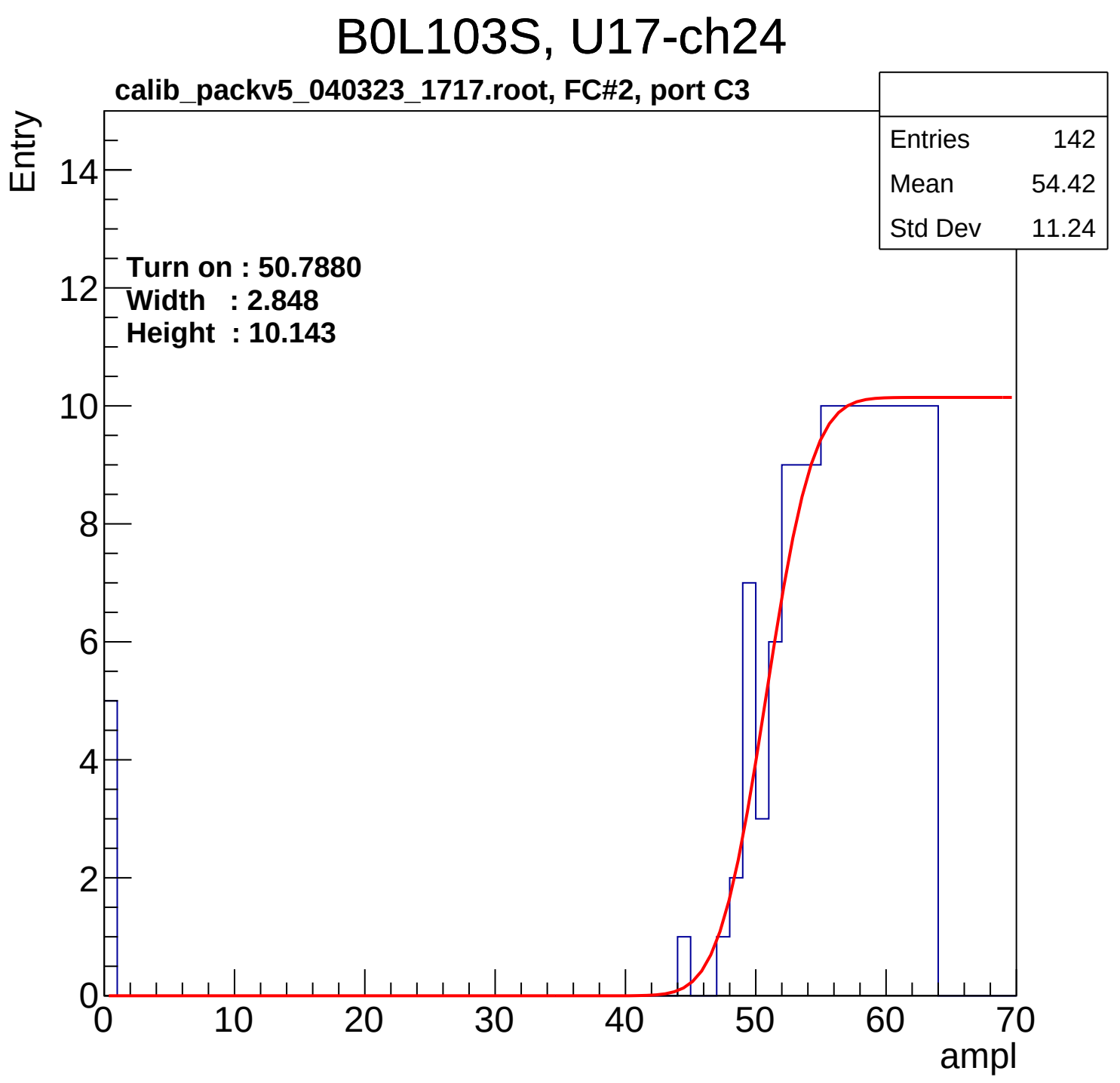
B0L103S, U17-ch24
calib_packv5_040323_1717.root, FC#2, port C3
Entries 142
Mean 54.42
Std Dev 11.24
Turn on : 50.7880
Width : 2.848
Height : 10.143
Entry
ampl
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6
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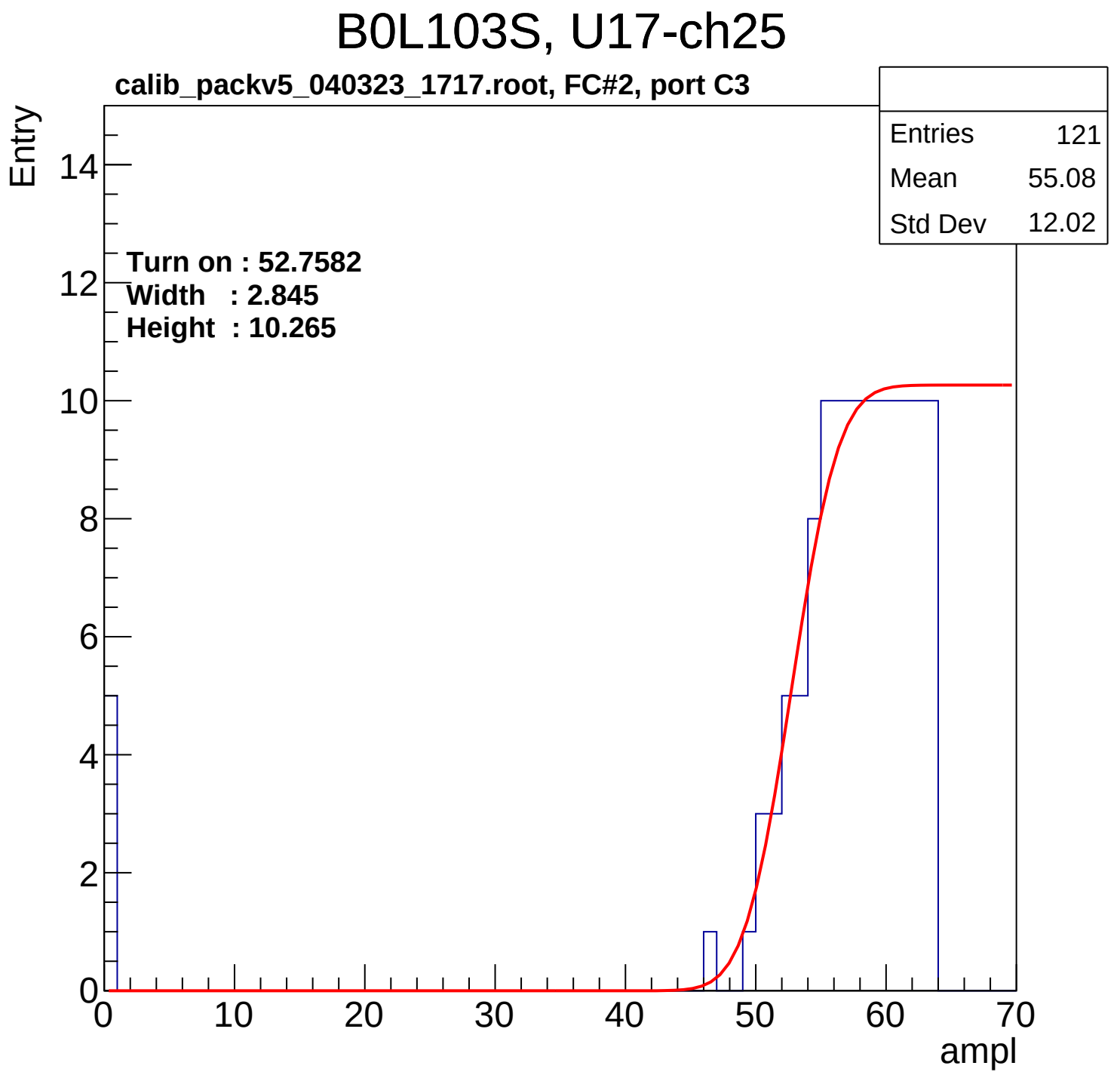
B0L103S, U17-ch25
calib_packv5_040323_1717.root, FC#2, port C3
Entries 121
Mean 55.08
Std Dev 12.02
Turn on : 52.7582
Width : 2.845
Height : 10.265
Entry
ampl
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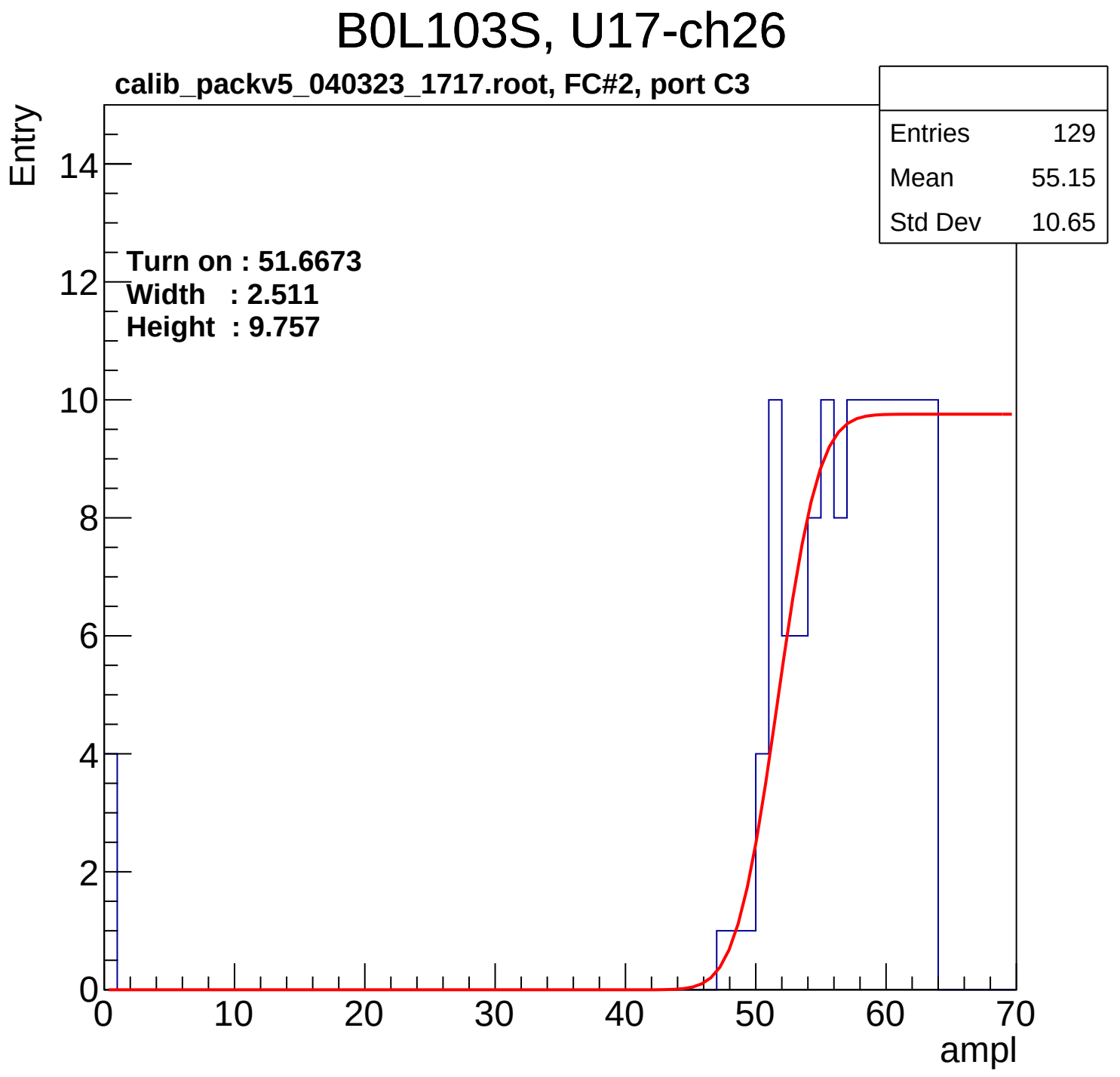
B0L103S, U17-ch26
calib_packv5_040323_1717.root, FC#2, port C3
Entries 129
Mean 55.15
Std Dev 10.65
Turn on : 51.6673
Width : 2.511
Height : 9.757
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ampl
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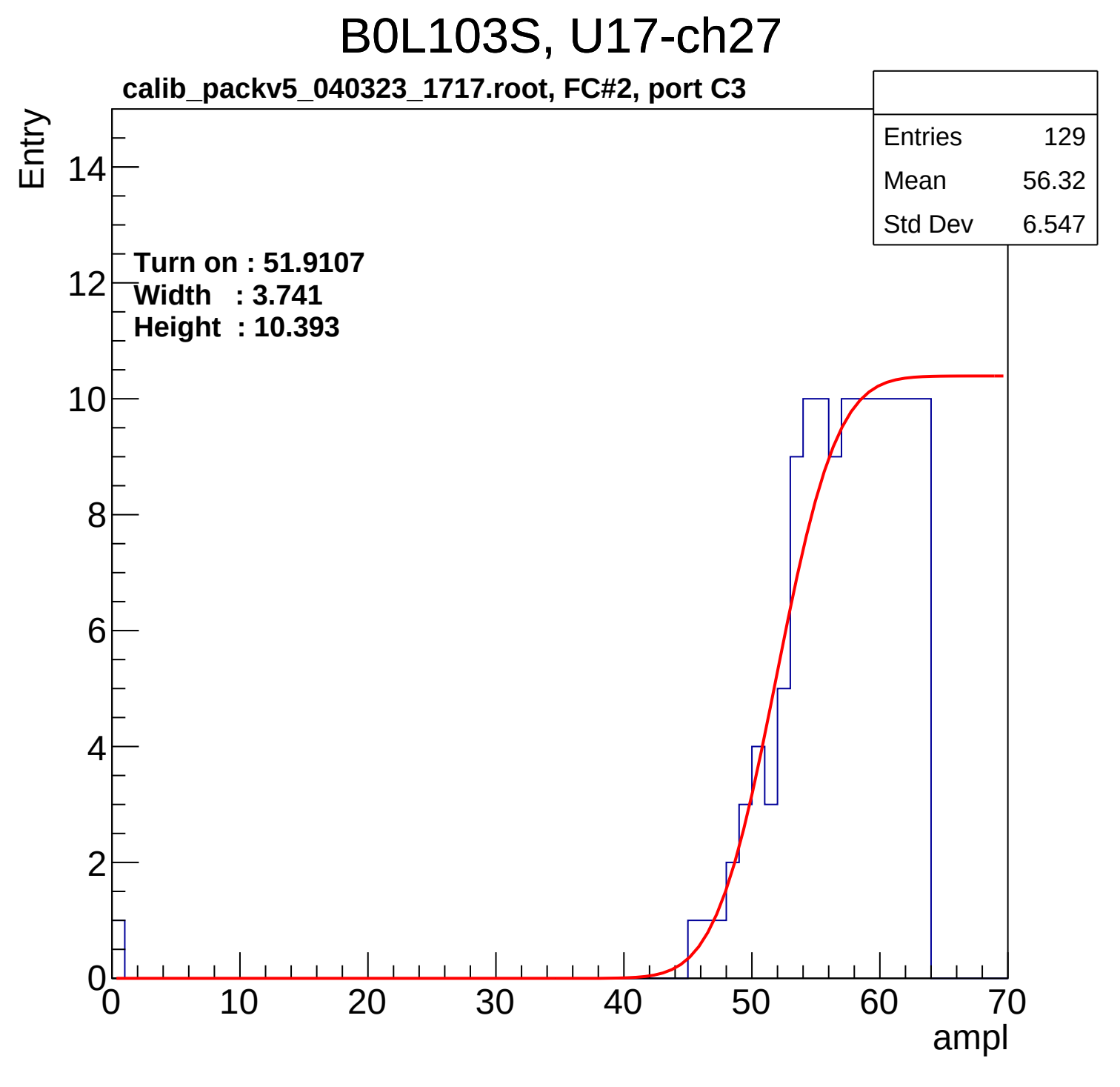
B0L103S, U17-ch27
calib_packv5_040323_1717.root, FC#2, port C3
Entries 129
Mean 56.32
Std Dev 6.547
Turn on : 51.9107
Width : 3.741
Height : 10.393
Entry
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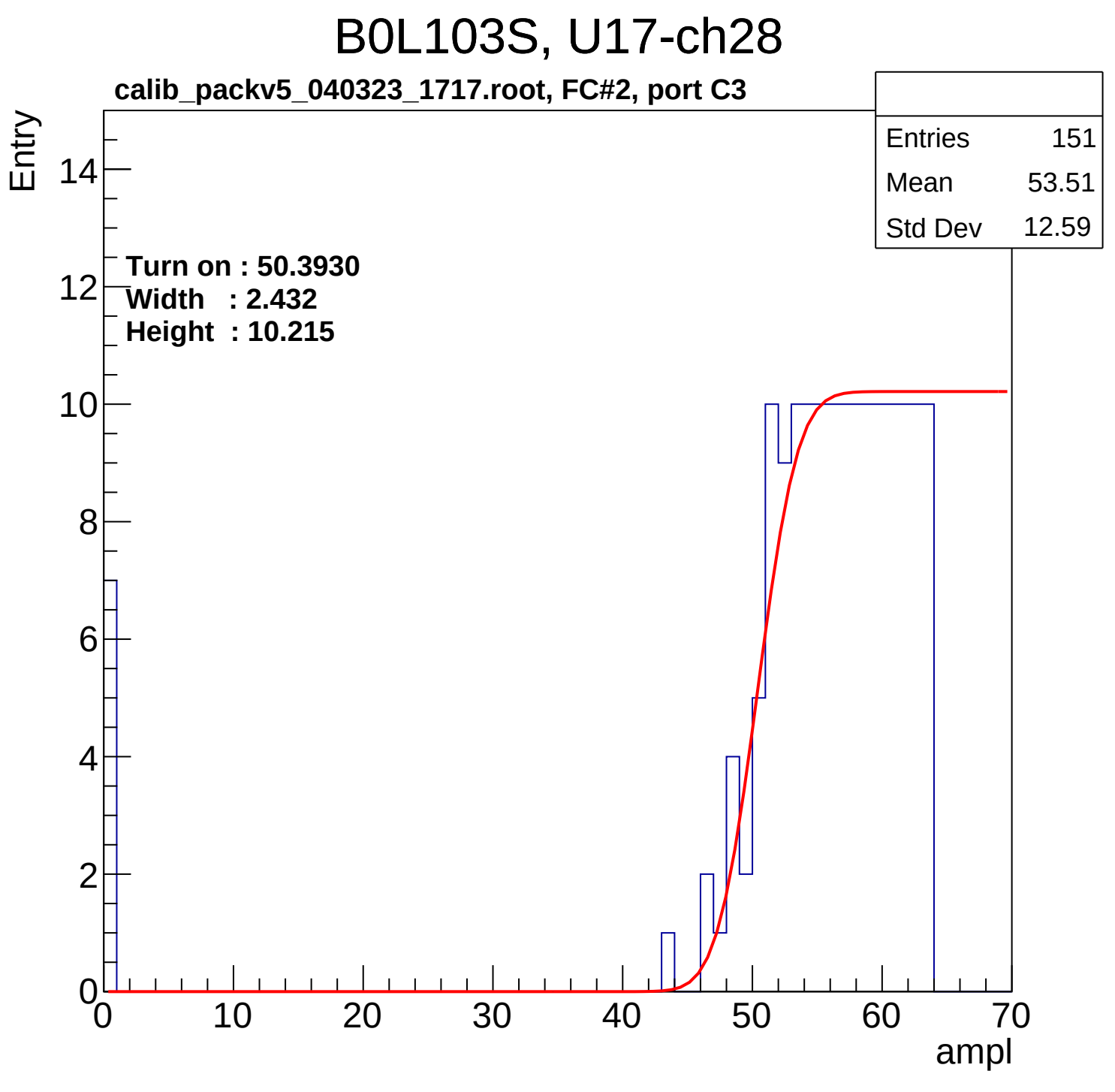
B0L103S, U17-ch28
calib_packv5_040323_1717.root, FC#2, port C3
Entries 151
Mean 53.51
Std Dev 12.59
Turn on : 50.3930
Width : 2.432
Height : 10.215
Entry
ampl
0
2
4
6
8
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12
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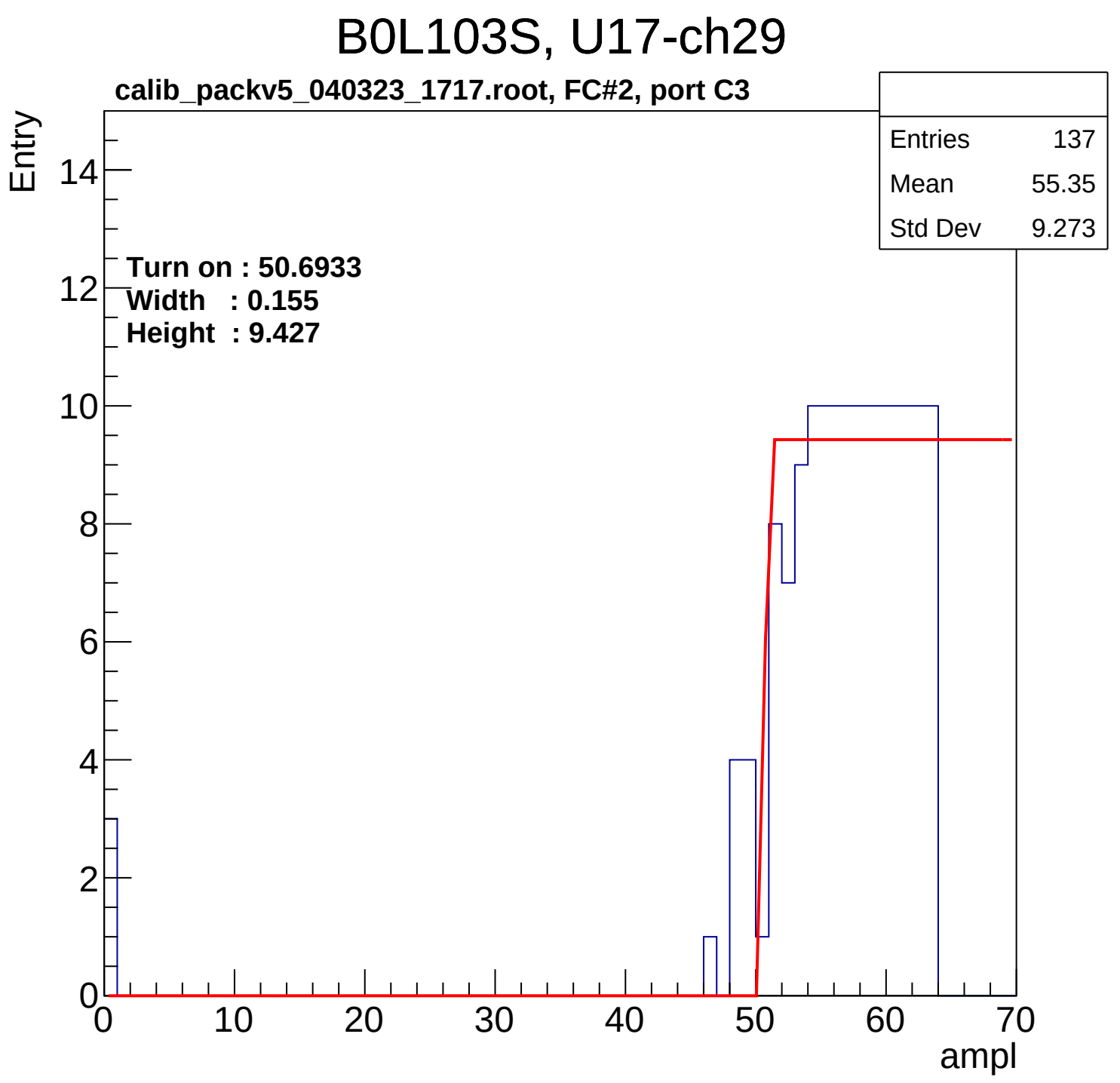
B0L103S, U17-ch29
calib_packv5_040323_1717.root, FC#2, port C3
Entries 137
Mean 55.35
Std Dev 9.273
Turn on : 50.6933
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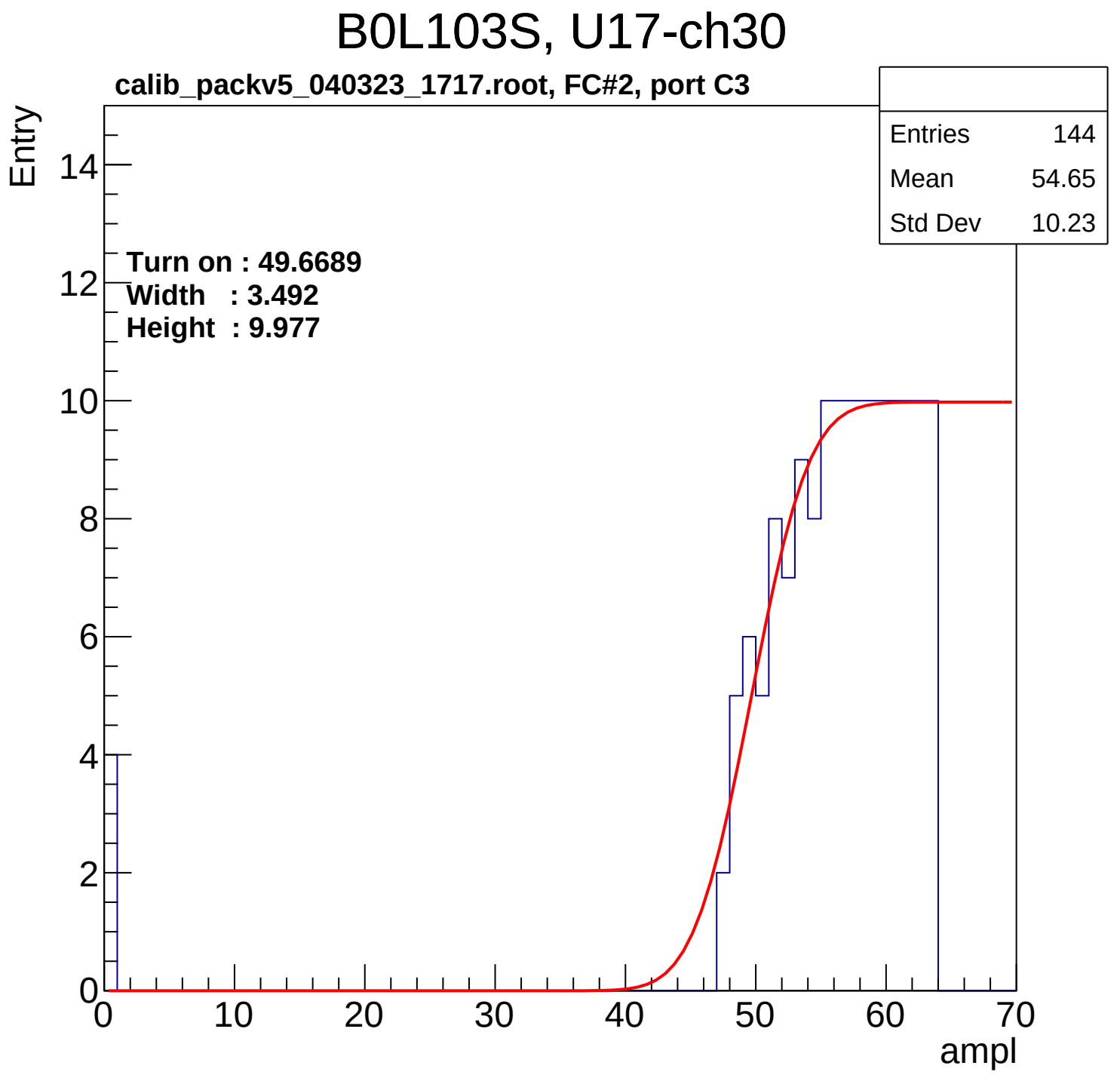
B0L103S, U17-ch30
calib_packv5_040323_1717.root, FC#2, port C3
Entries 144
Mean 54.65
Std Dev 10.23
Turn on : 49.6689
Width : 3.492
Height : 9.977
Entry
ampl
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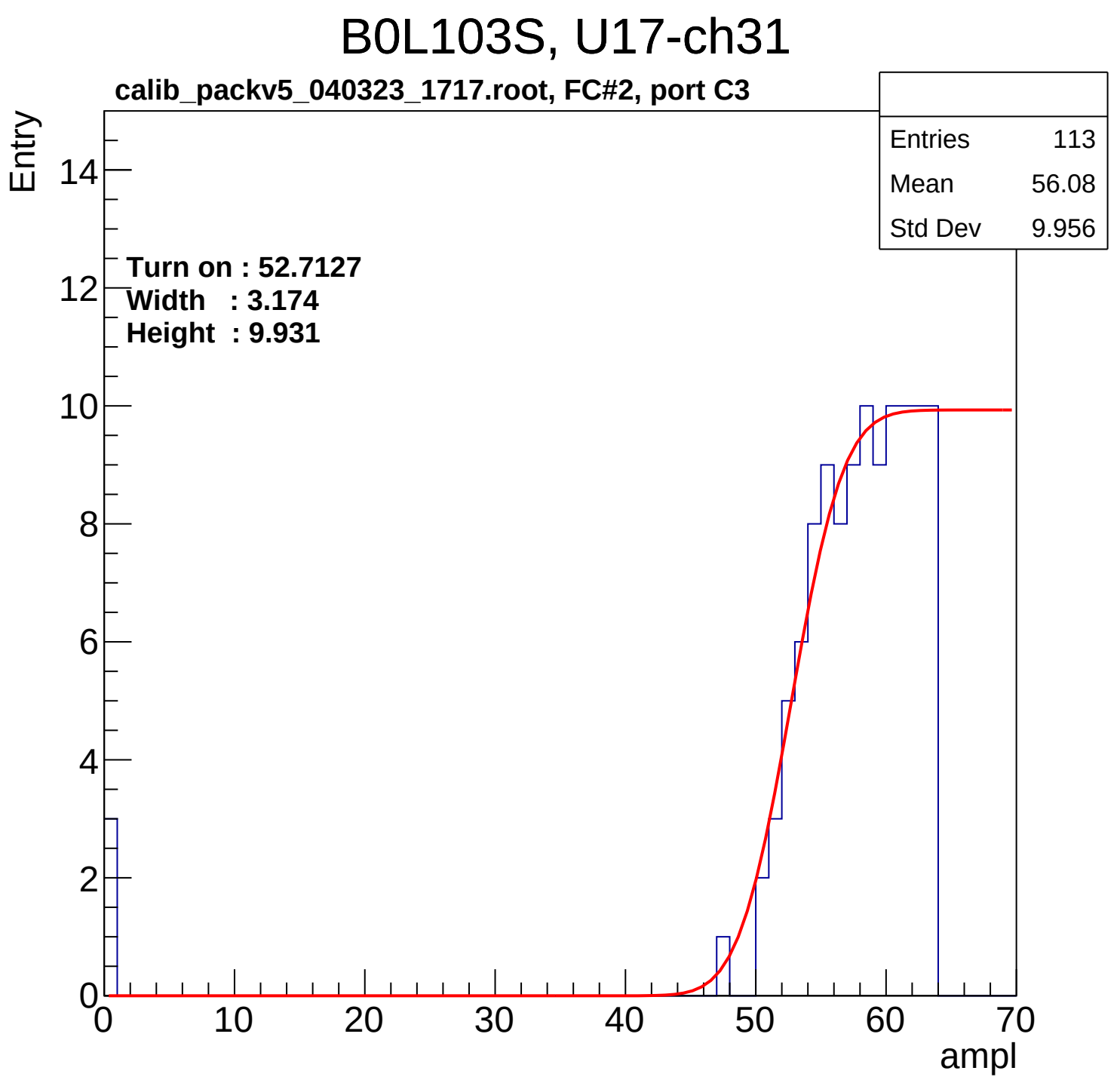
B0L103S, U17-ch31
calib_packv5_040323_1717.root, FC#2, port C3
Entries 113
Mean 56.08
Std Dev 9.956
Turn on : 52.7127
Width : 3.174
Height : 9.931
Entry
ampl
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2
4
6
8
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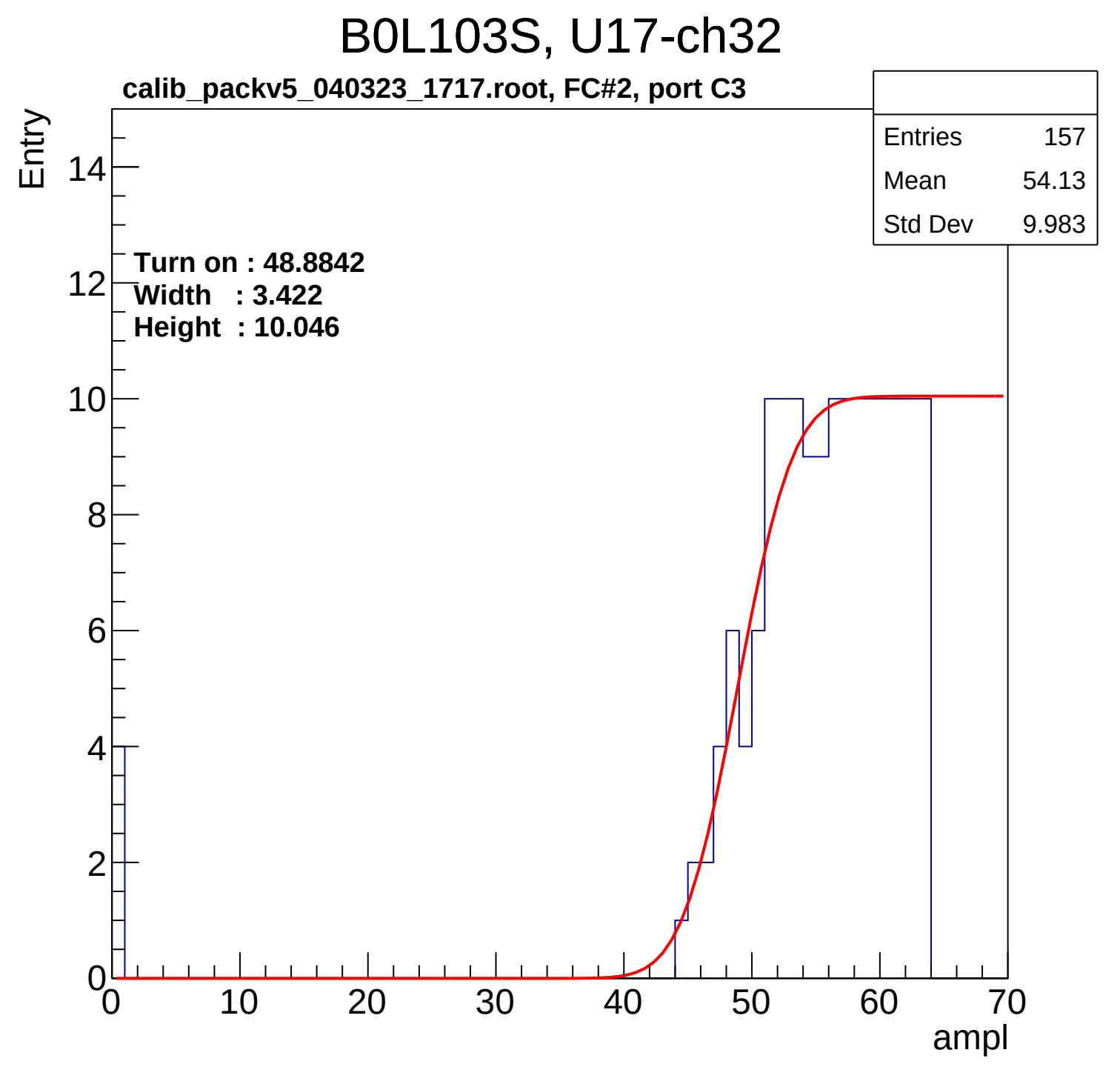
B0L103S, U17-ch32
calib_packv5_040323_1717.root, FC#2, port C3
Entries 157
Mean 54.13
Std Dev 9.983
Turn on : 48.8842
Width : 3.422
Height : 10.046
Entry
ampl
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4
6
8
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12
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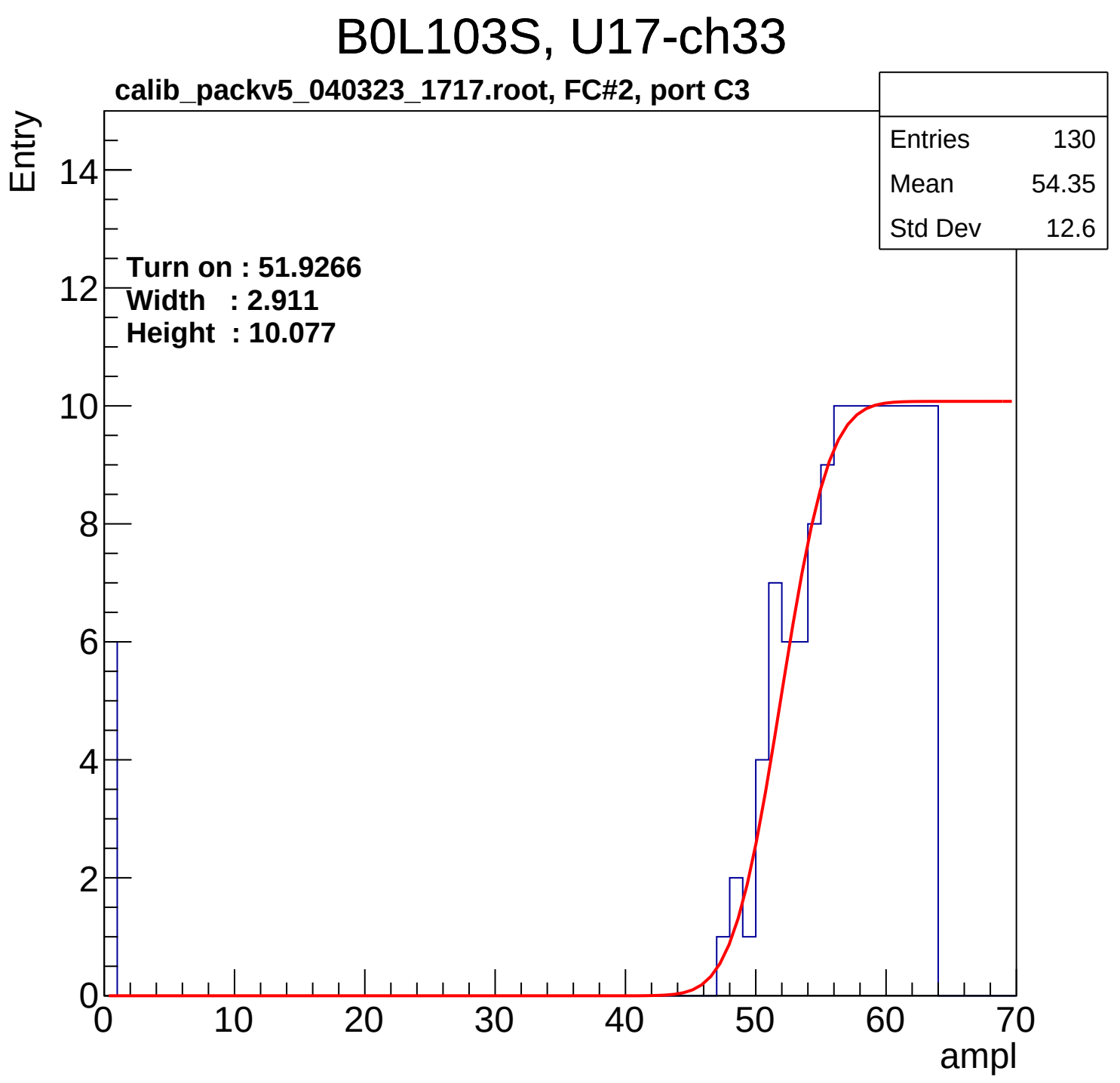
B0L103S, U17-ch33
calib_packv5_040323_1717.root, FC#2, port C3
Entries 130
Mean 54.35
Std Dev 12.6
Turn on : 51.9266
Width : 2.911
Height : 10.077
Entry
ampl
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6
8
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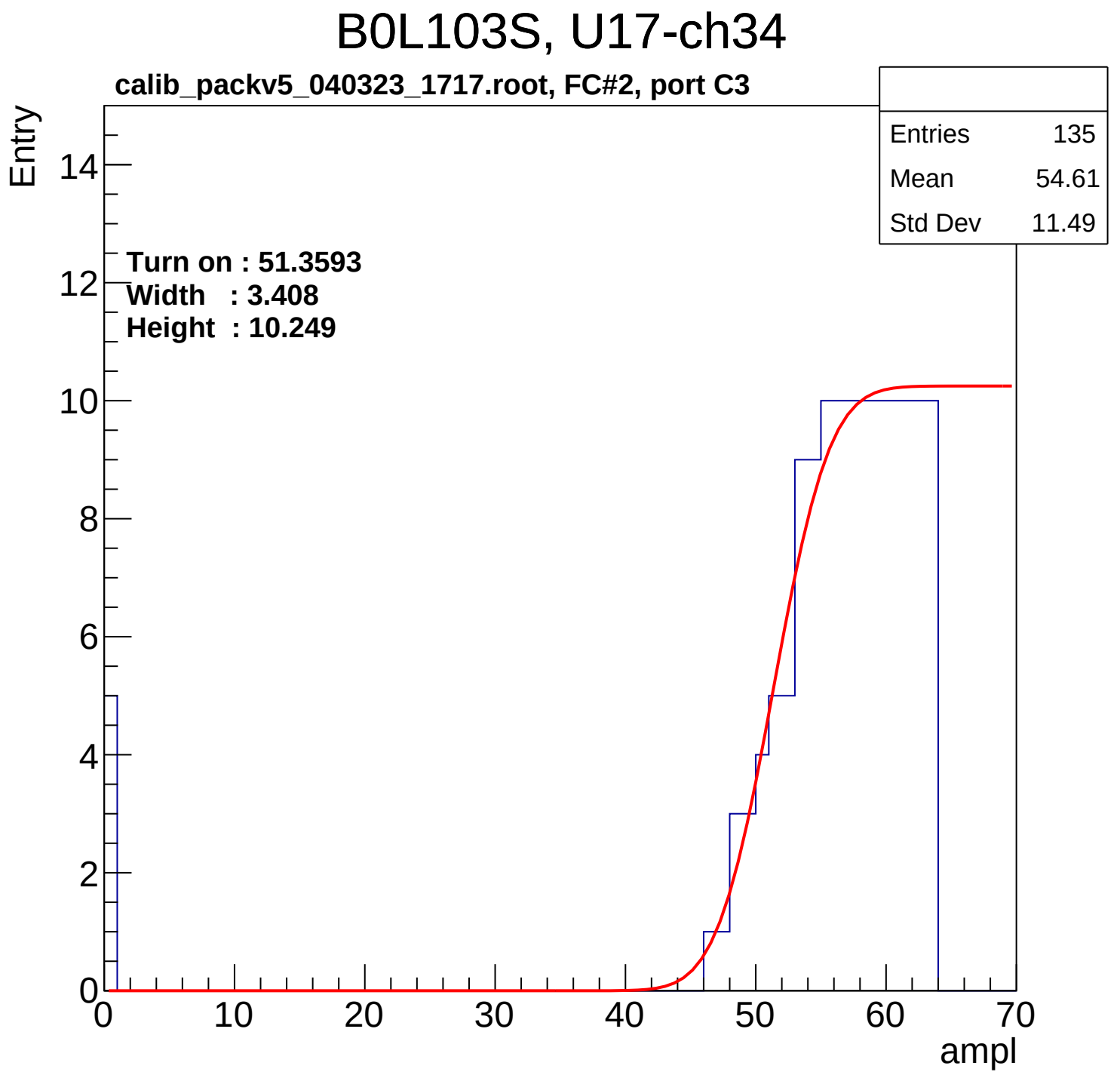
B0L103S, U17-ch34
calib_packv5_040323_1717.root, FC#2, port C3
Entries 135
Mean 54.61
Std Dev 11.49
Turn on : 51.3593
Width : 3.408
Height : 10.249
Entry
ampl
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2
4
6
8
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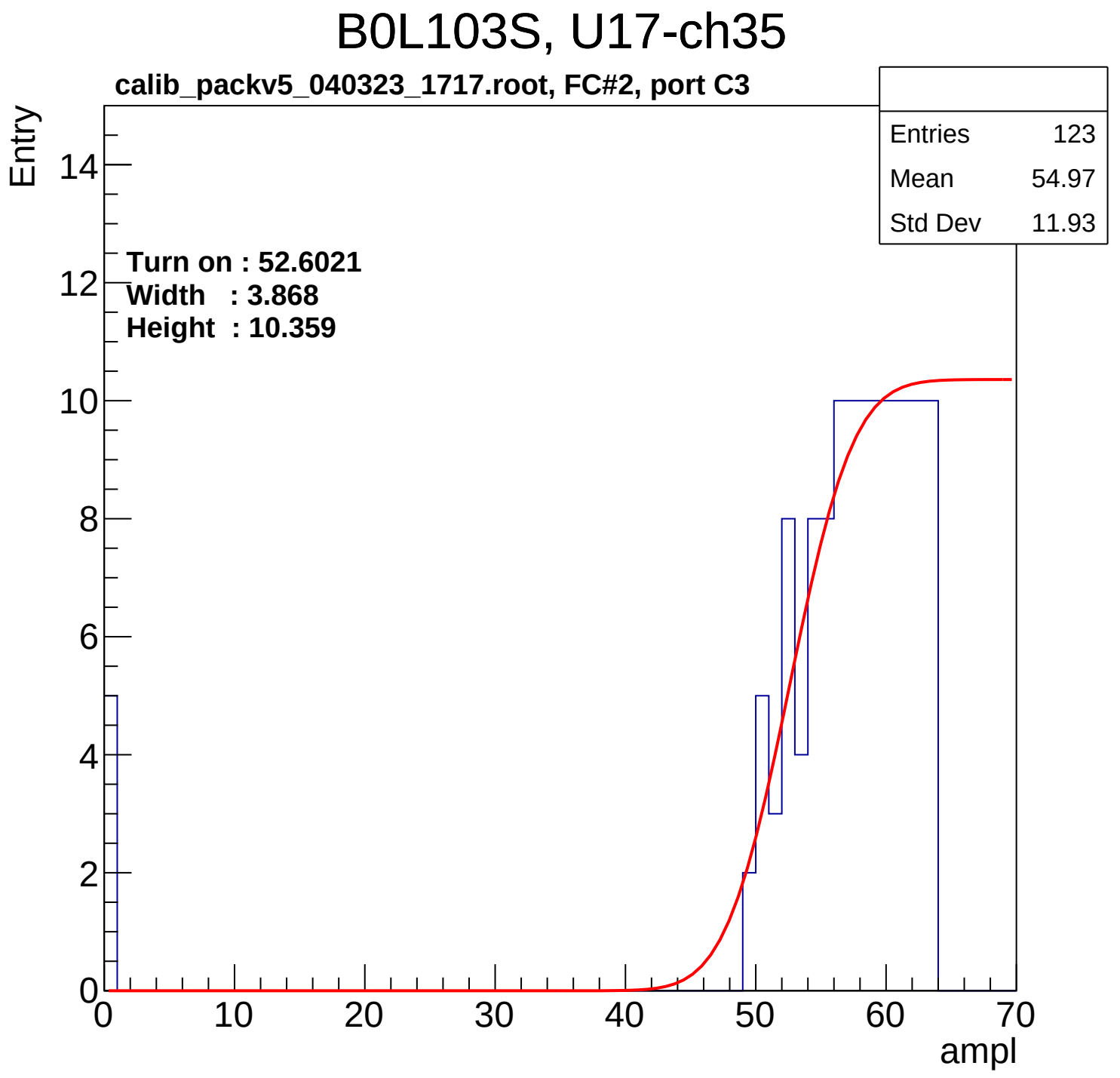
B0L103S, U17-ch35
calib_packv5_040323_1717.root, FC#2, port C3
Entries 123
Mean 54.97
Std Dev 11.93
Turn on : 52.6021
Width : 3.868
Height : 10.359
Entry
ampl
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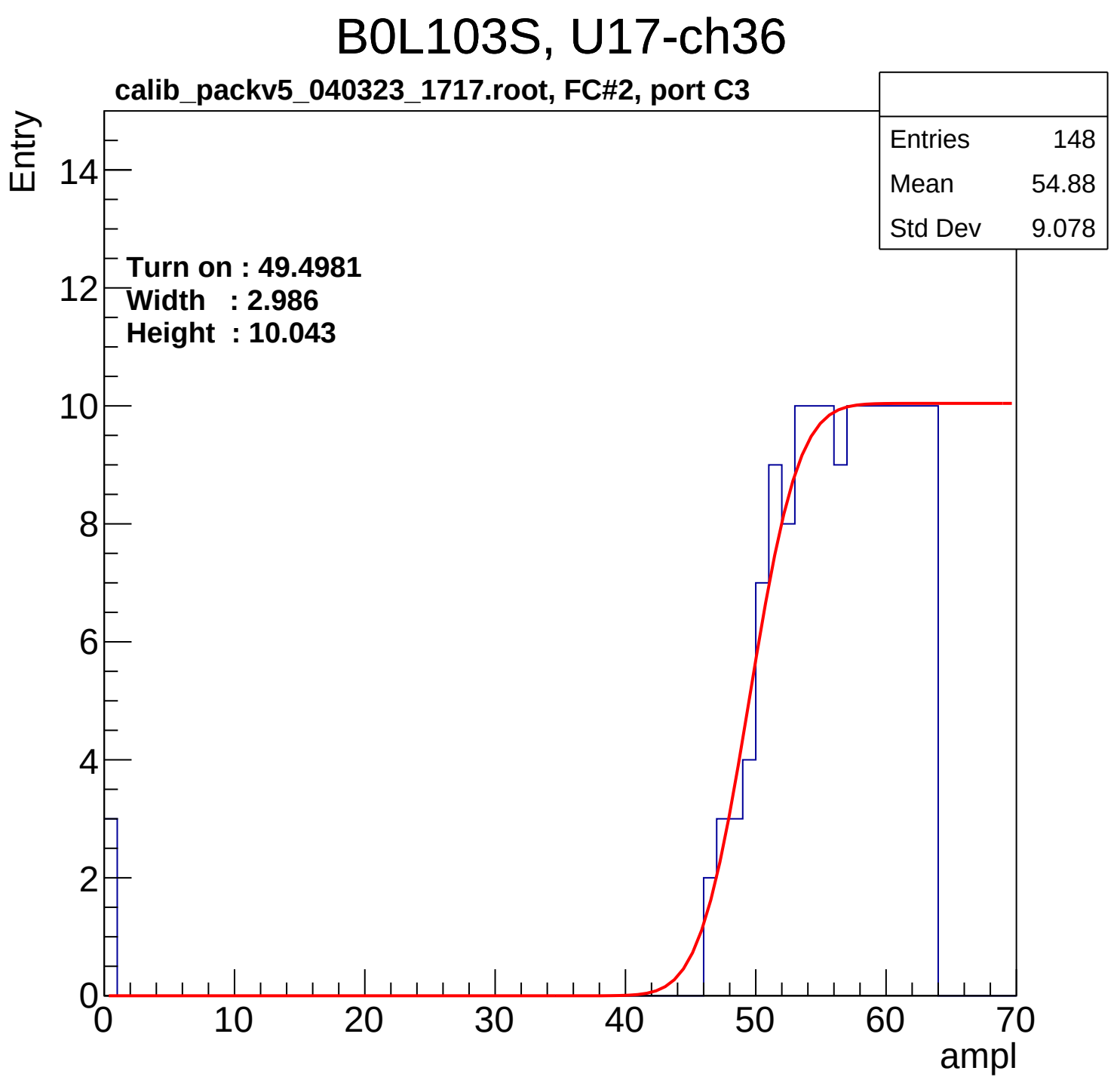
B0L103S, U17-ch36
calib_packv5_040323_1717.root, FC#2, port C3
Entries 148
Mean 54.88
Std Dev 9.078
Turn on : 49.4981
Width : 2.986
Height : 10.043
Entry
ampl
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2
4
6
8
10
12
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40
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60
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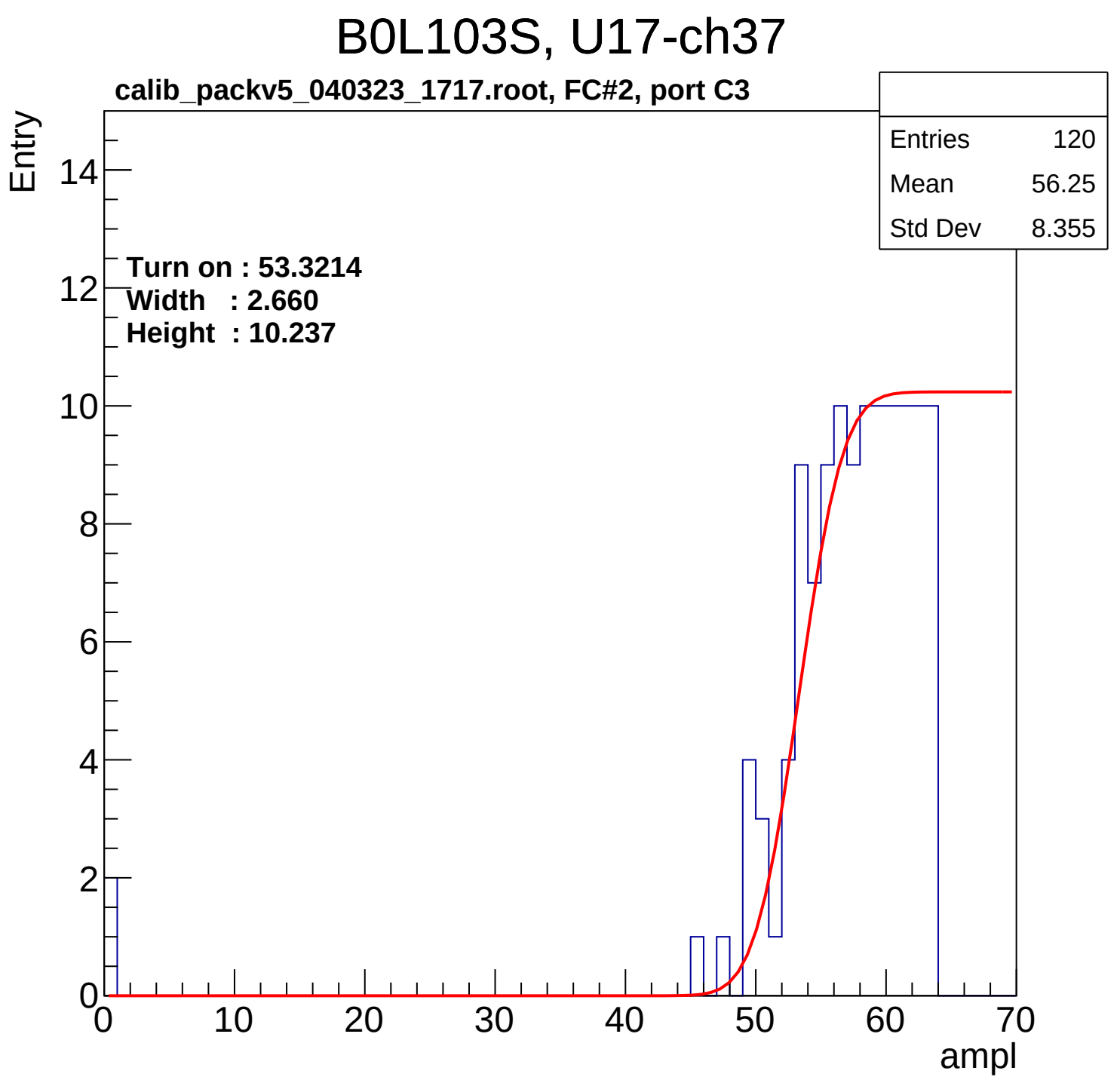
B0L103S, U17-ch37
calib_packv5_040323_1717.root, FC#2, port C3
Entries 120
Mean 56.25
Std Dev 8.355
Turn on : 53.3214
Width : 2.660
Height : 10.237
Entry
ampl
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6
8
10
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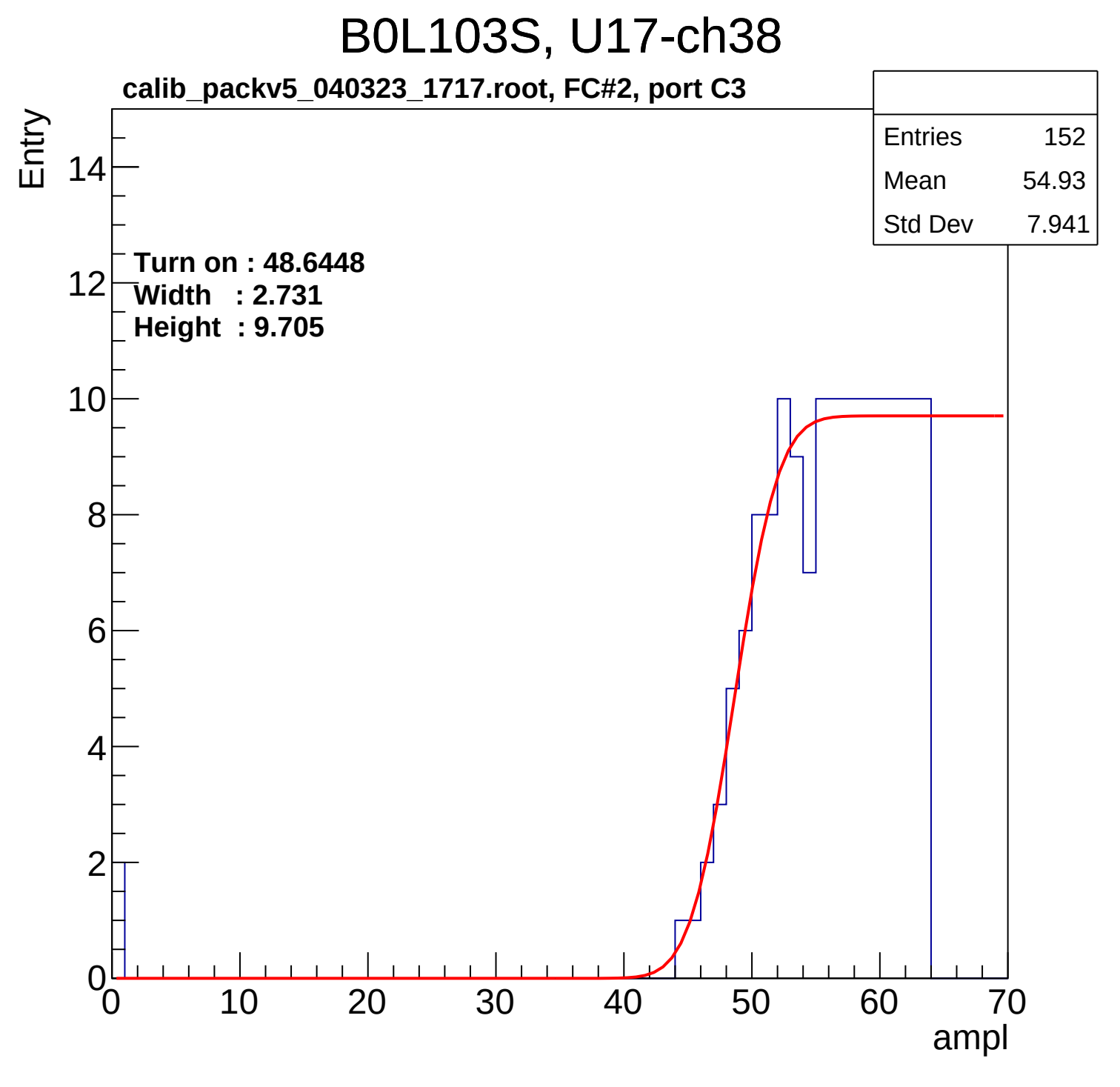
B0L103S, U17-ch38
calib_packv5_040323_1717.root, FC#2, port C3
Entries 152
Mean 54.93
Std Dev 7.941
Turn on : 48.6448
Width : 2.731
Height : 9.705
Entry
ampl
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6
8
10
12
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0
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60
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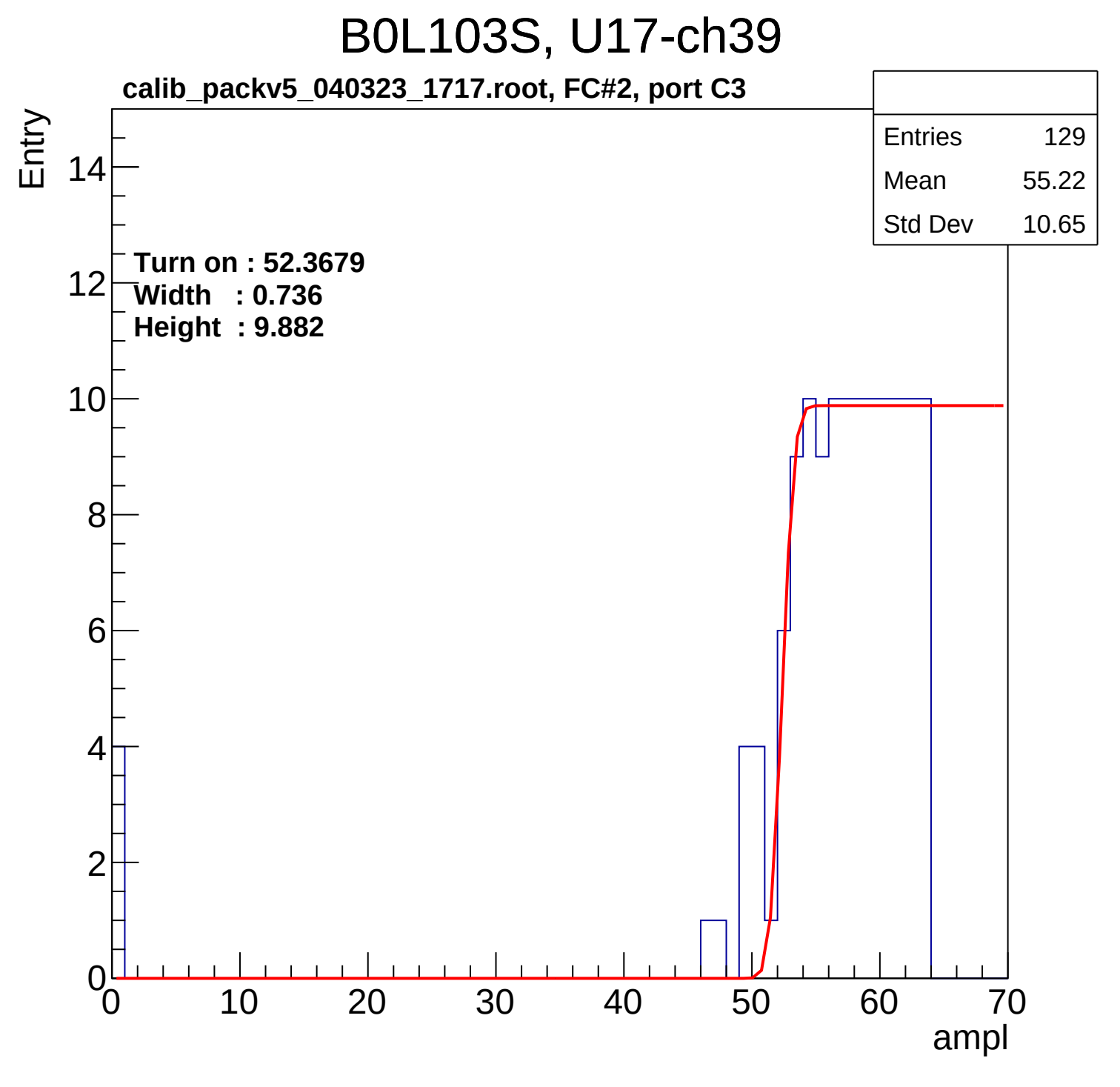
B0L103S, U17-ch39
calib_packv5_040323_1717.root, FC#2, port C3
Entries 129
Mean 55.22
Std Dev 10.65
Turn on : 52.3679
Width : 0.736
Height : 9.882
Entry
ampl
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6
8
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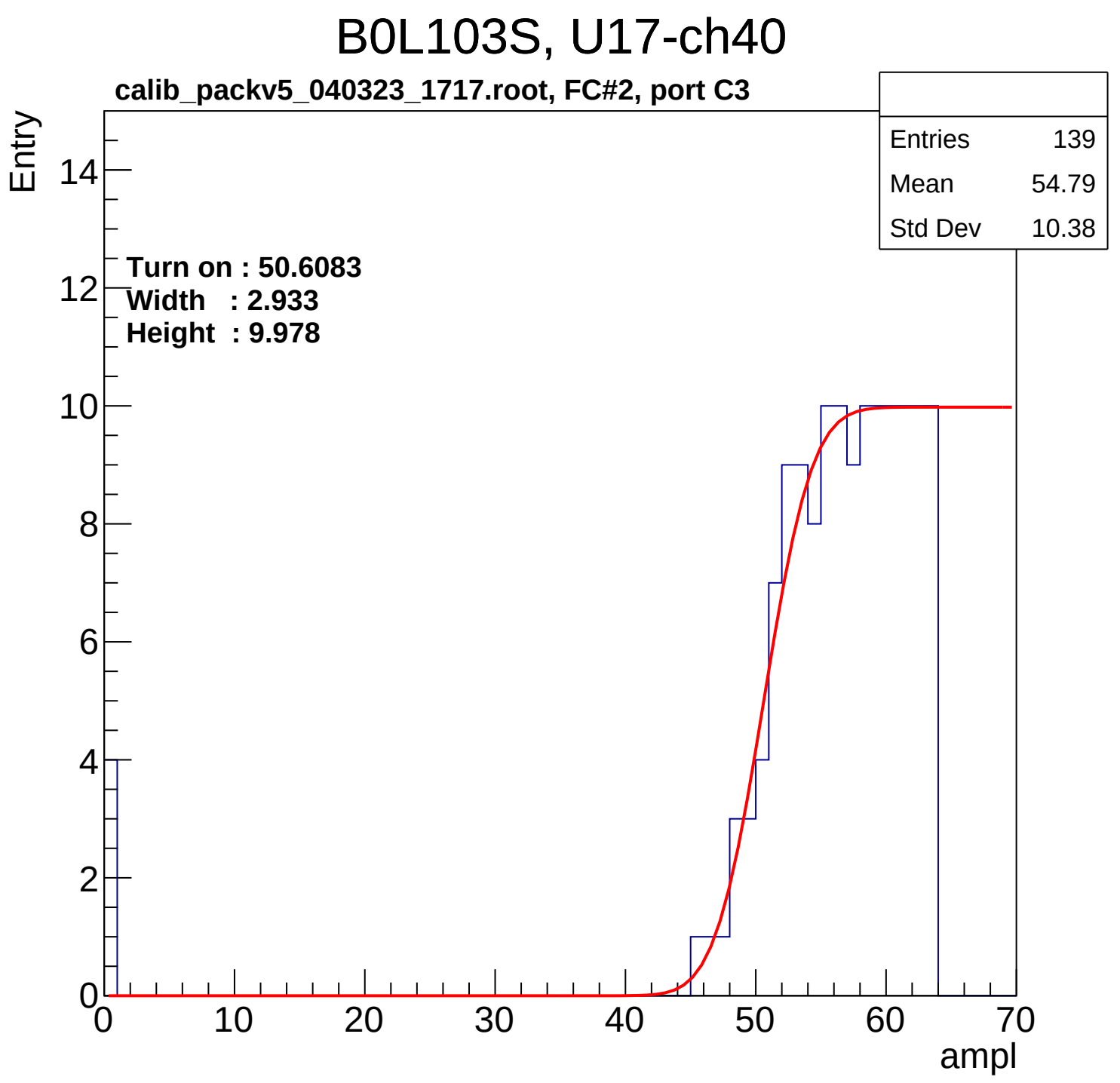
B0L103S, U17-ch40
calib_packv5_040323_1717.root, FC#2, port C3
Entries 139
Mean 54.79
Std Dev 10.38
Turn on : 50.6083
Width : 2.933
Height : 9.978
Entry
ampl
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6
8
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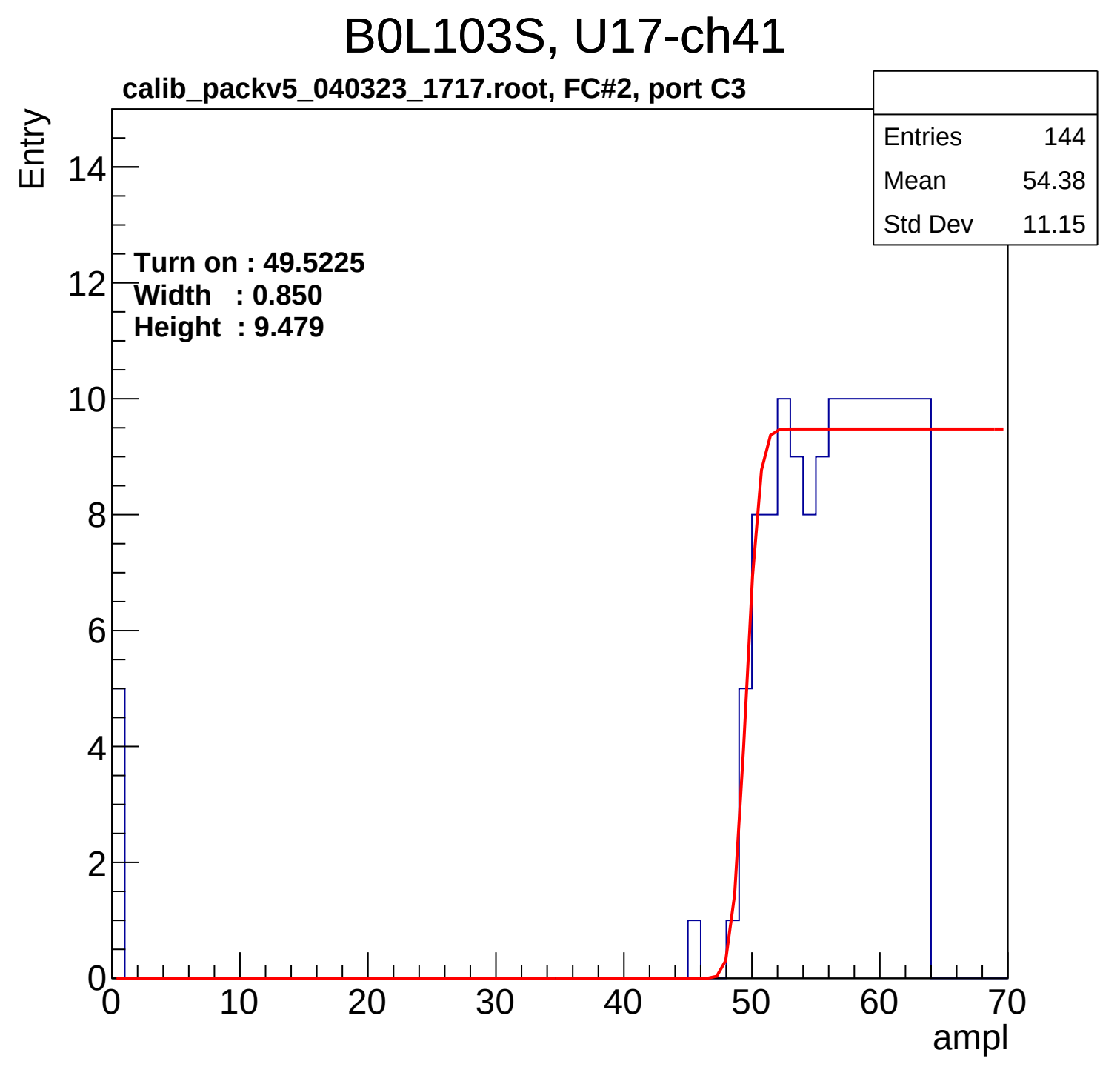
B0L103S, U17-ch41
calib_packv5_040323_1717.root, FC#2, port C3
Entries 144
Mean 54.38
Std Dev 11.15
Turn on : 49.5225
Width : 0.850
Height : 9.479
Entry
ampl
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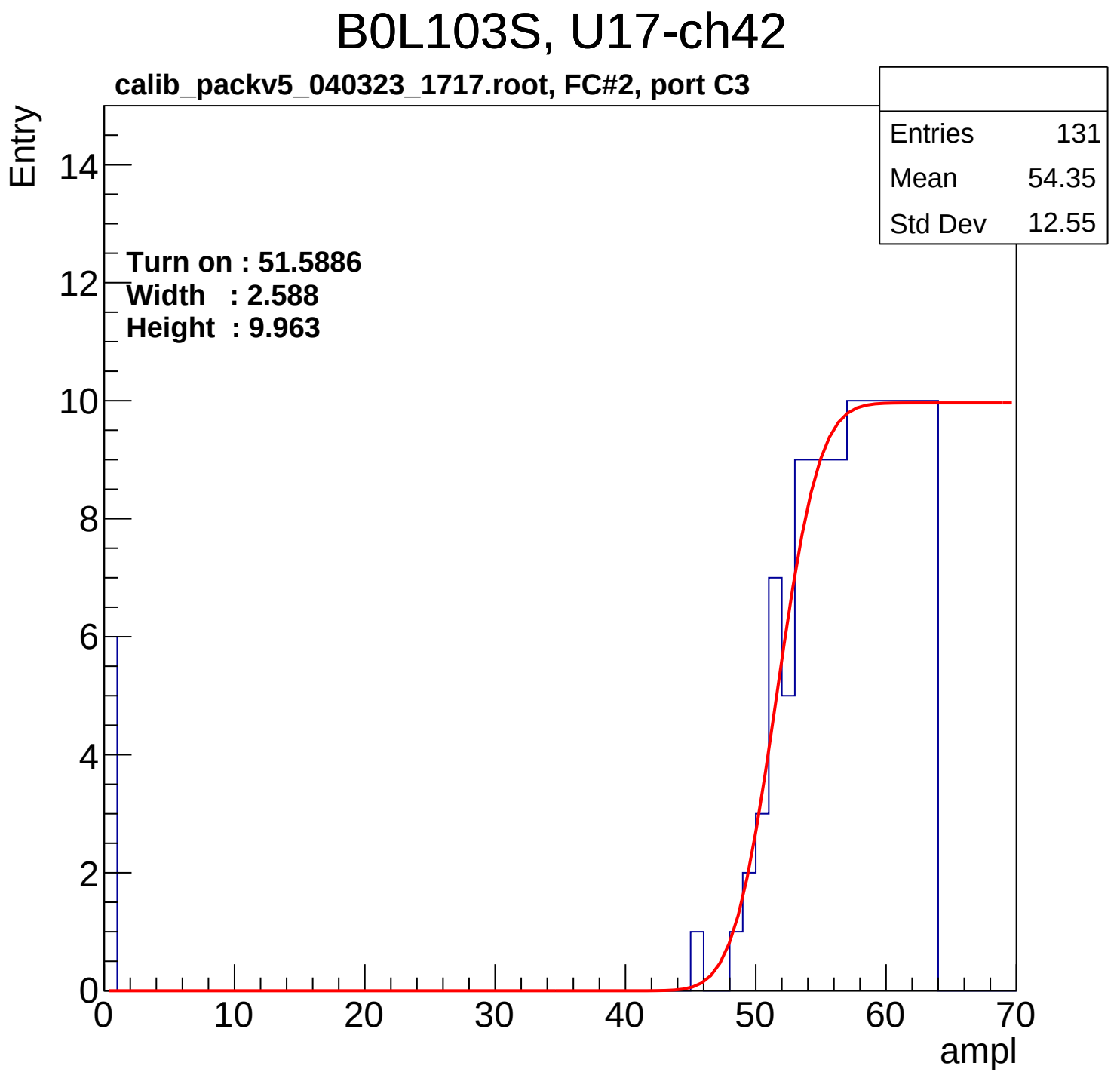
B0L103S, U17-ch42
calib_packv5_040323_1717.root, FC#2, port C3
Entries 131
Mean 54.35
Std Dev 12.55
Turn on : 51.5886
Width : 2.588
Height : 9.963
Entry
ampl
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6
8
10
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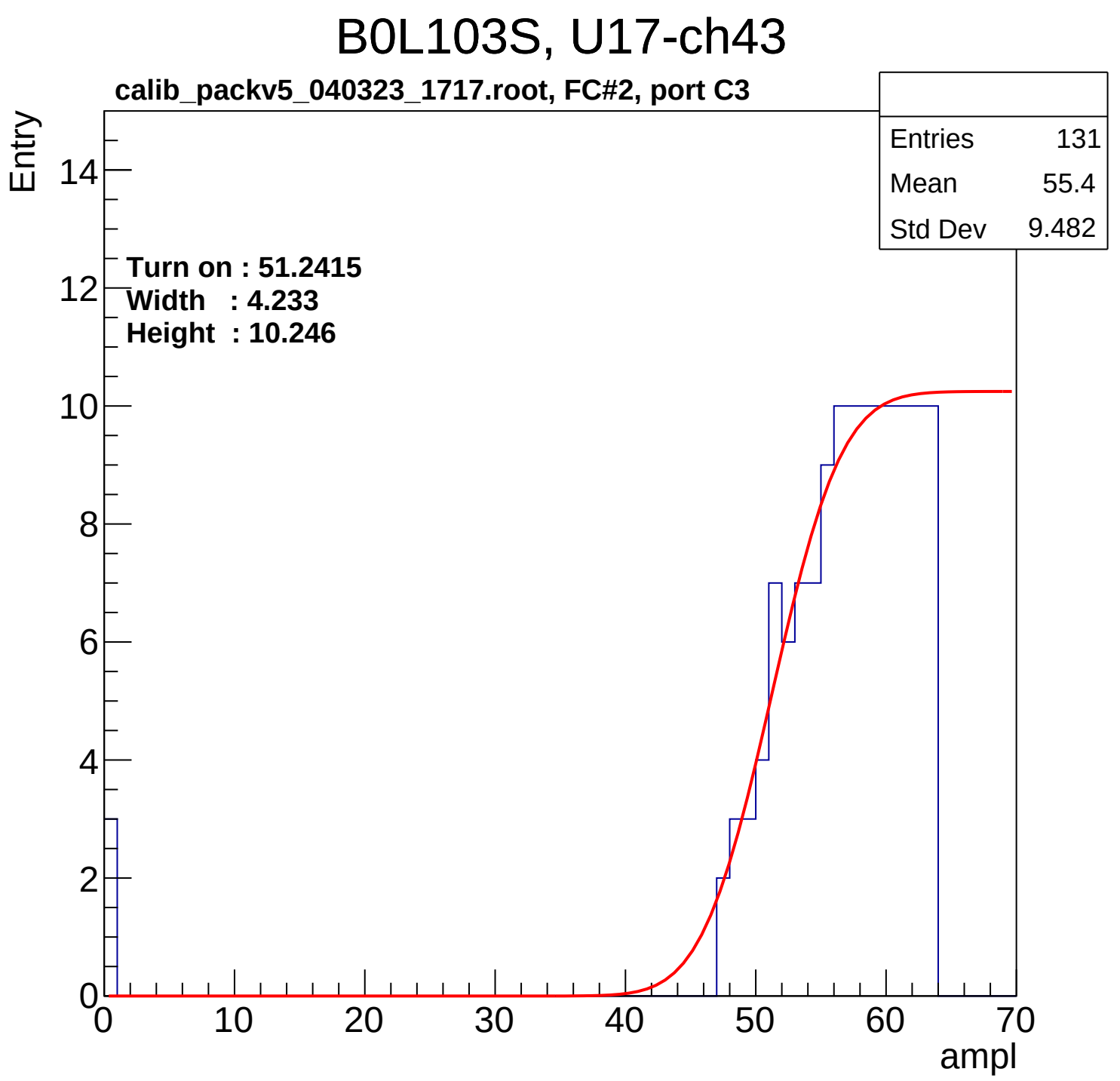
B0L103S, U17-ch43
calib_packv5_040323_1717.root, FC#2, port C3
Entries 131
Mean 55.4
Std Dev 9.482
Turn on : 51.2415
Width : 4.233
Height : 10.246
Entry
ampl
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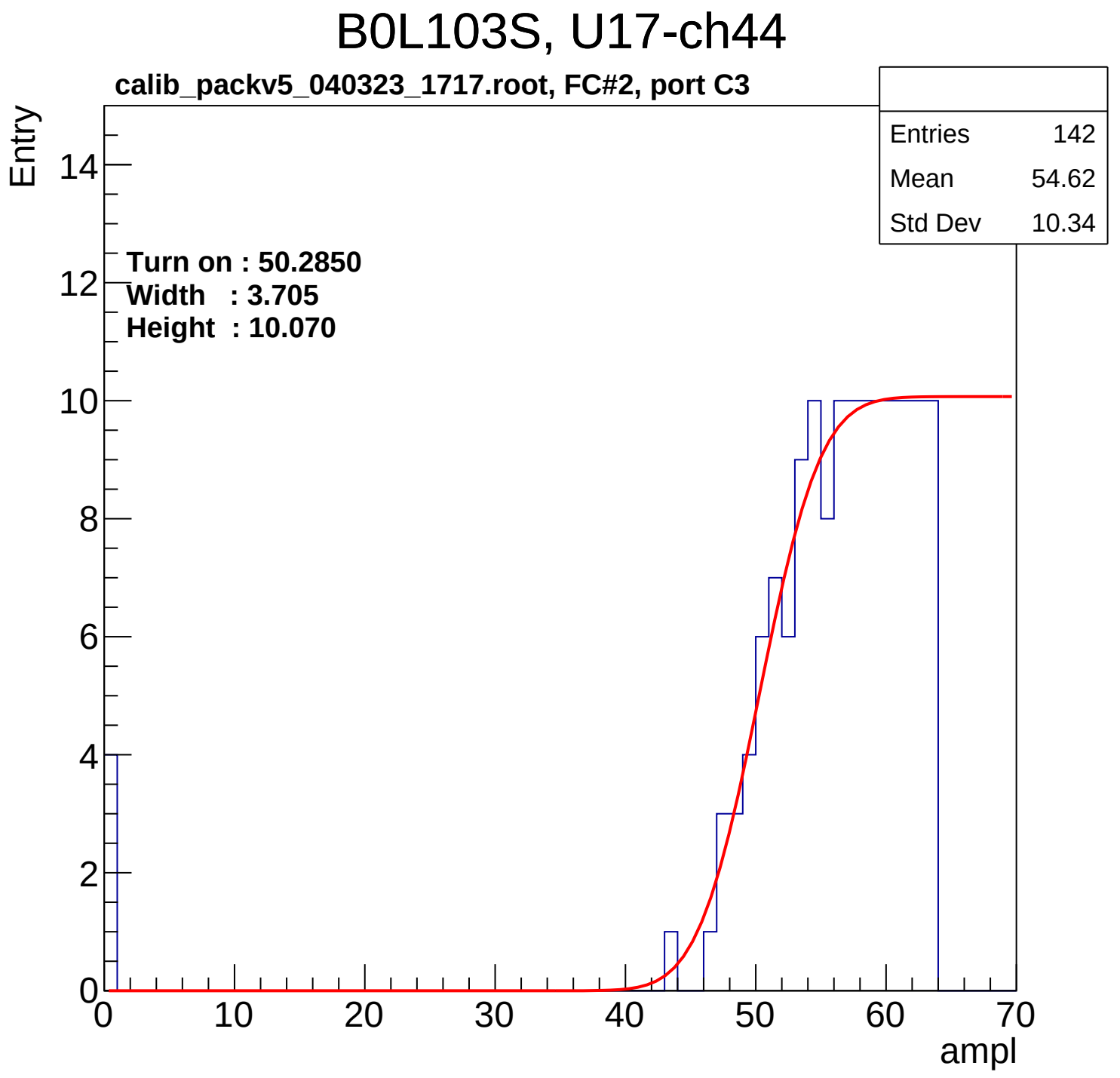
B0L103S, U17-ch44
calib_packv5_040323_1717.root, FC#2, port C3
Entries 142
Mean 54.62
Std Dev 10.34
Turn on : 50.2850
Width : 3.705
Height : 10.070
Entry
ampl
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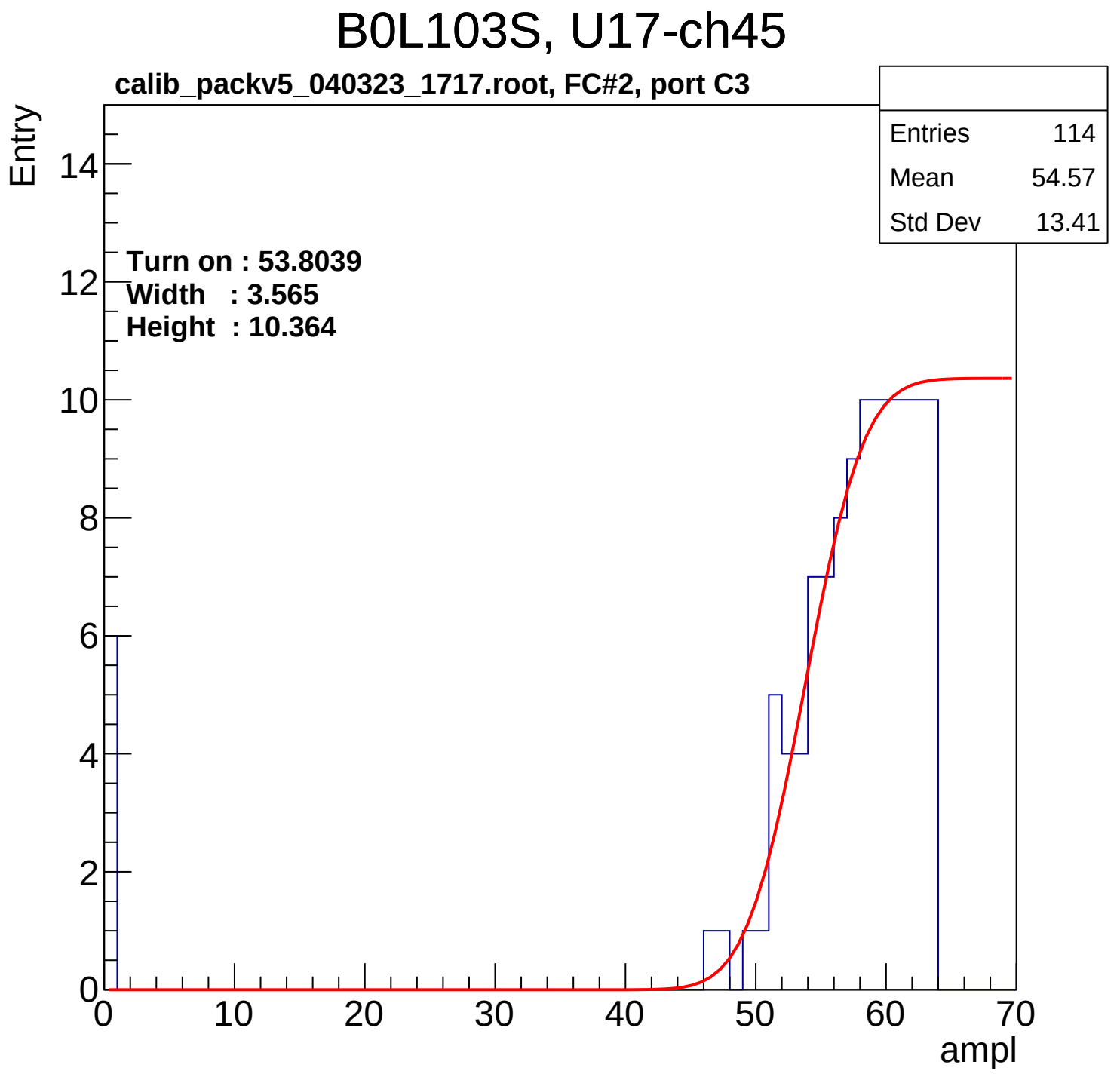
B0L103S, U17-ch45
calib_packv5_040323_1717.root, FC#2, port C3
Entries 114
Mean 54.57
Std Dev 13.41
Turn on : 53.8039
Width : 3.565
Height : 10.364
Entry
ampl
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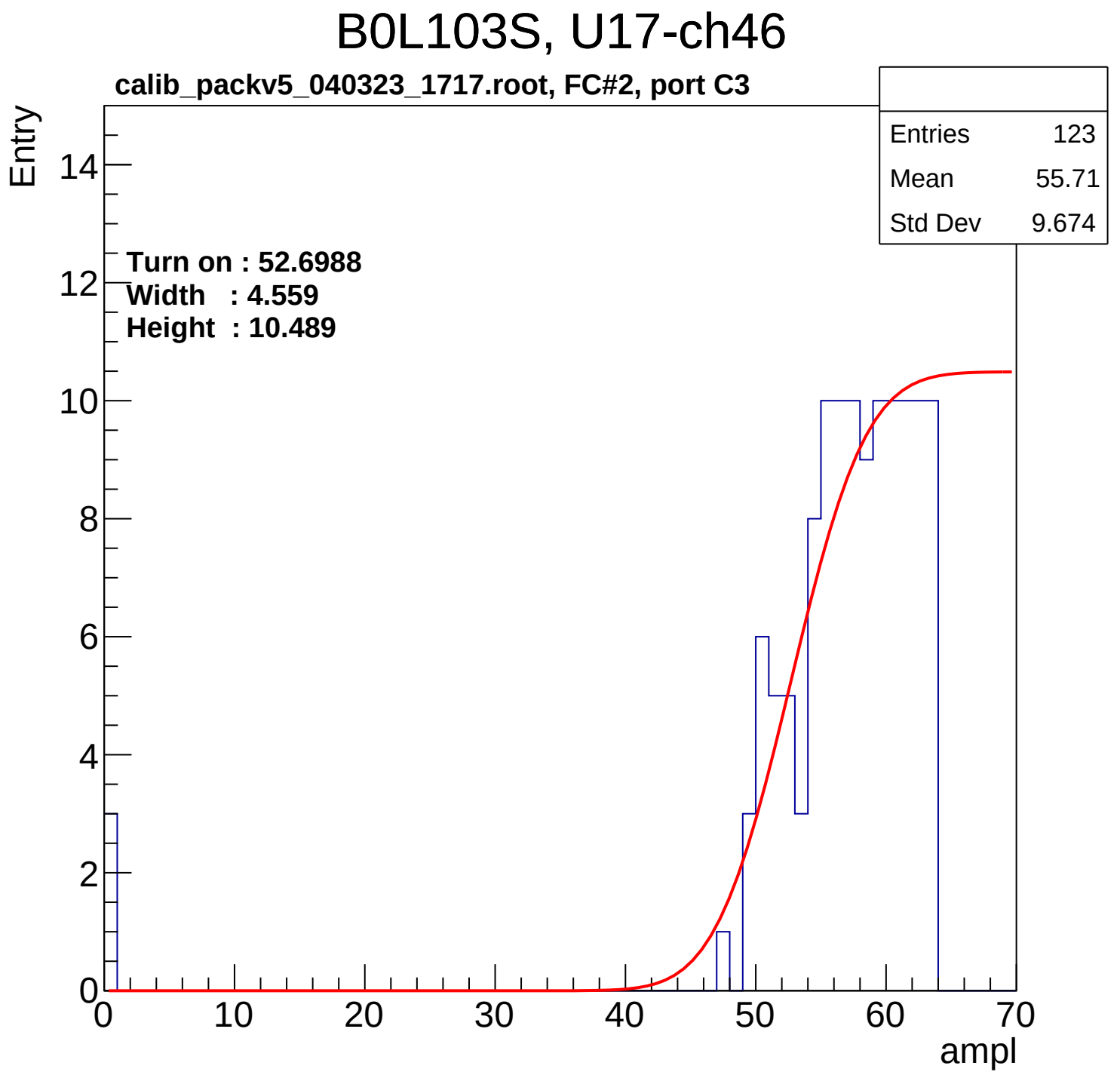
B0L103S, U17-ch46
calib_packv5_040323_1717.root, FC#2, port C3
Entries 123
Mean 55.71
Std Dev 9.674
Turn on : 52.6988
Width : 4.559
Height : 10.489
Entry
ampl
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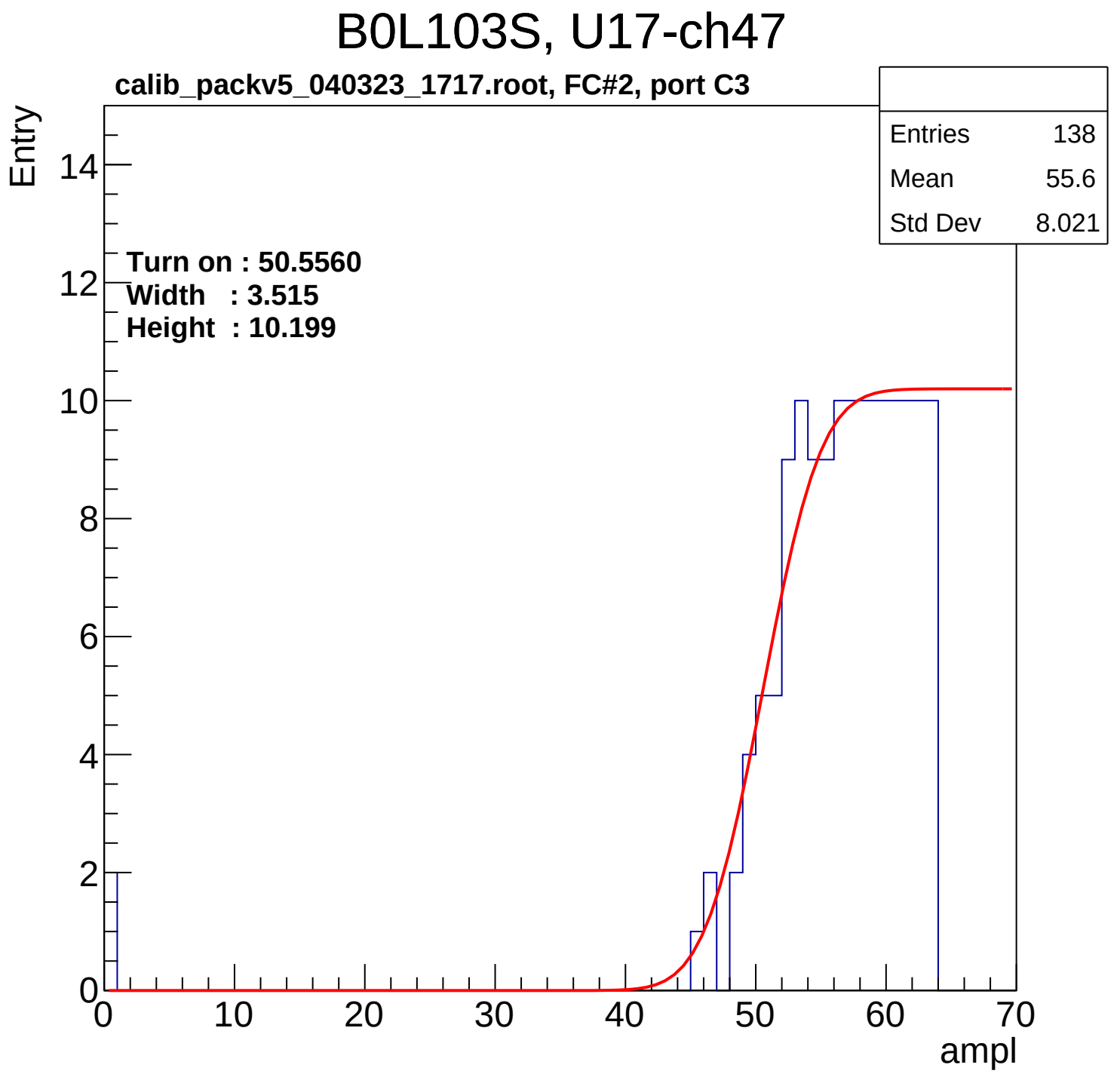
B0L103S, U17-ch47
calib_packv5_040323_1717.root, FC#2, port C3
Entries 138
Mean 55.6
Std Dev 8.021
Turn on : 50.5560
Width : 3.515
Height : 10.199
Entry
ampl
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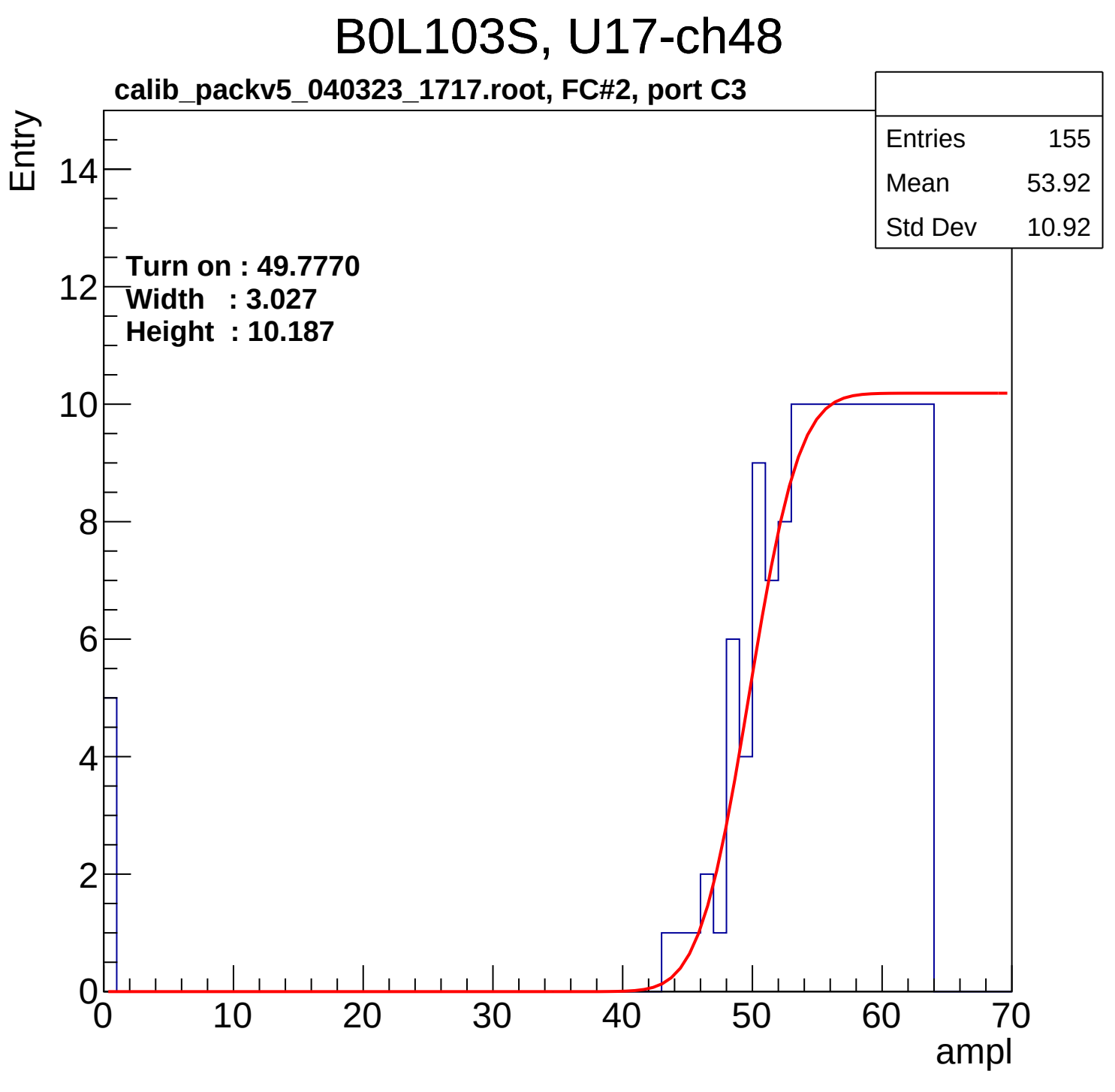
B0L103S, U17-ch48
calib_packv5_040323_1717.root, FC#2, port C3
Entries 155
Mean 53.92
Std Dev 10.92
Turn on : 49.7770
Width : 3.027
Height : 10.187
Entry
ampl
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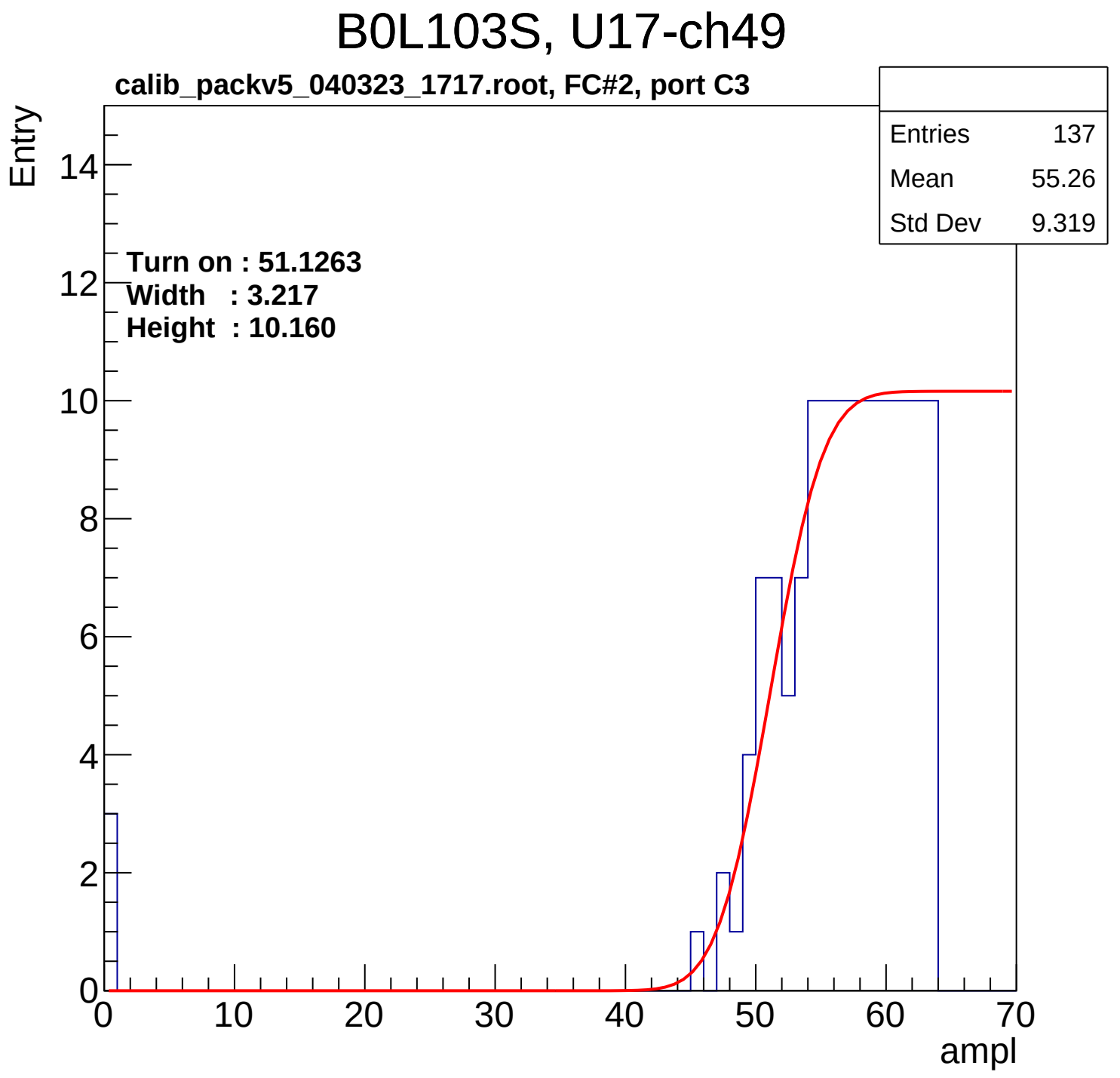
B0L103S, U17-ch49
calib_packv5_040323_1717.root, FC#2, port C3
Entries 137
Mean 55.26
Std Dev 9.319
Turn on : 51.1263
Width : 3.217
Height : 10.160
Entry
ampl
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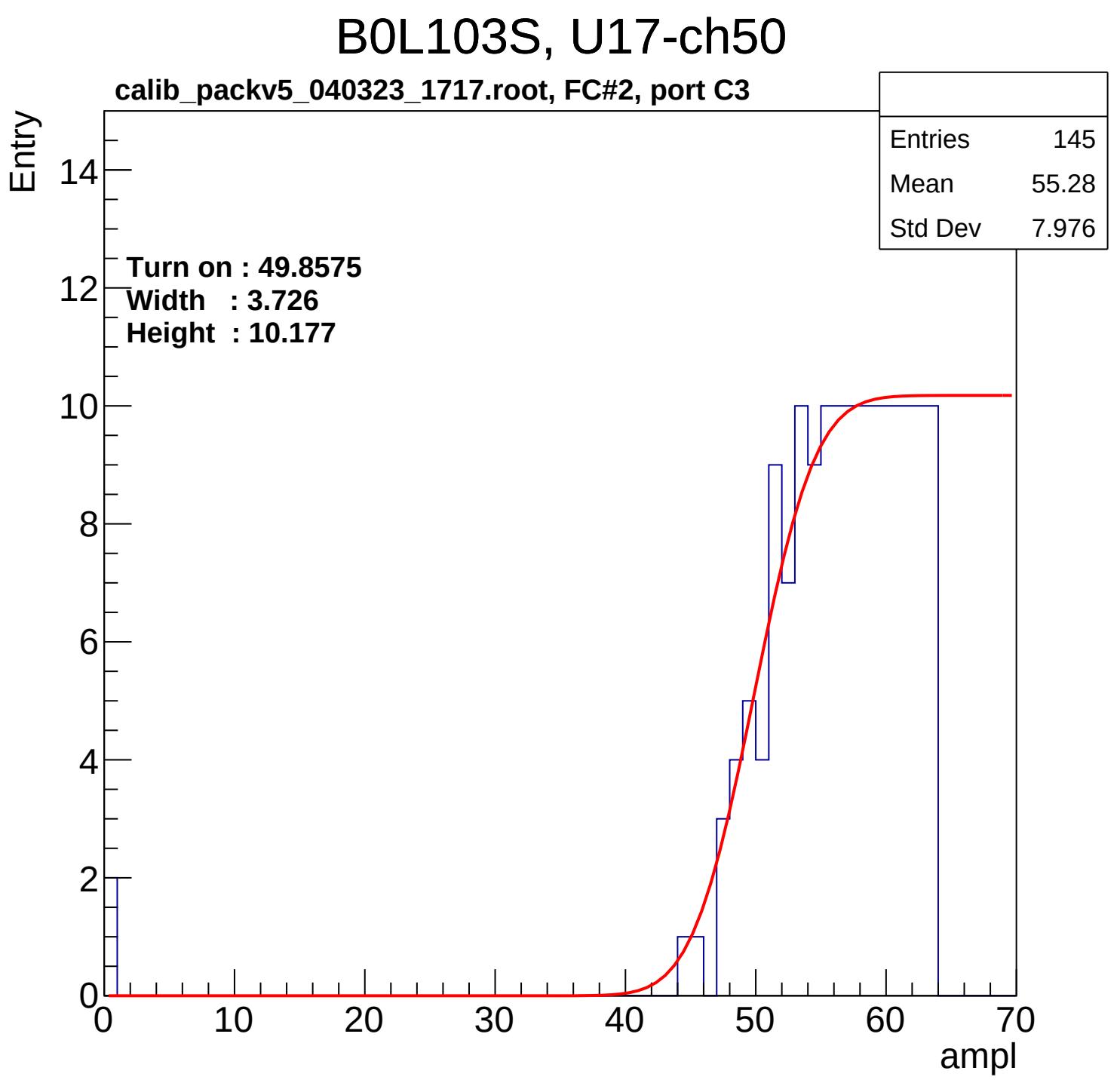
B0L103S, U17-ch50
calib_packv5_040323_1717.root, FC#2, port C3
Entries 145
Mean 55.28
Std Dev 7.976
Turn on : 49.8575
Width : 3.726
Height : 10.177
Entry
ampl
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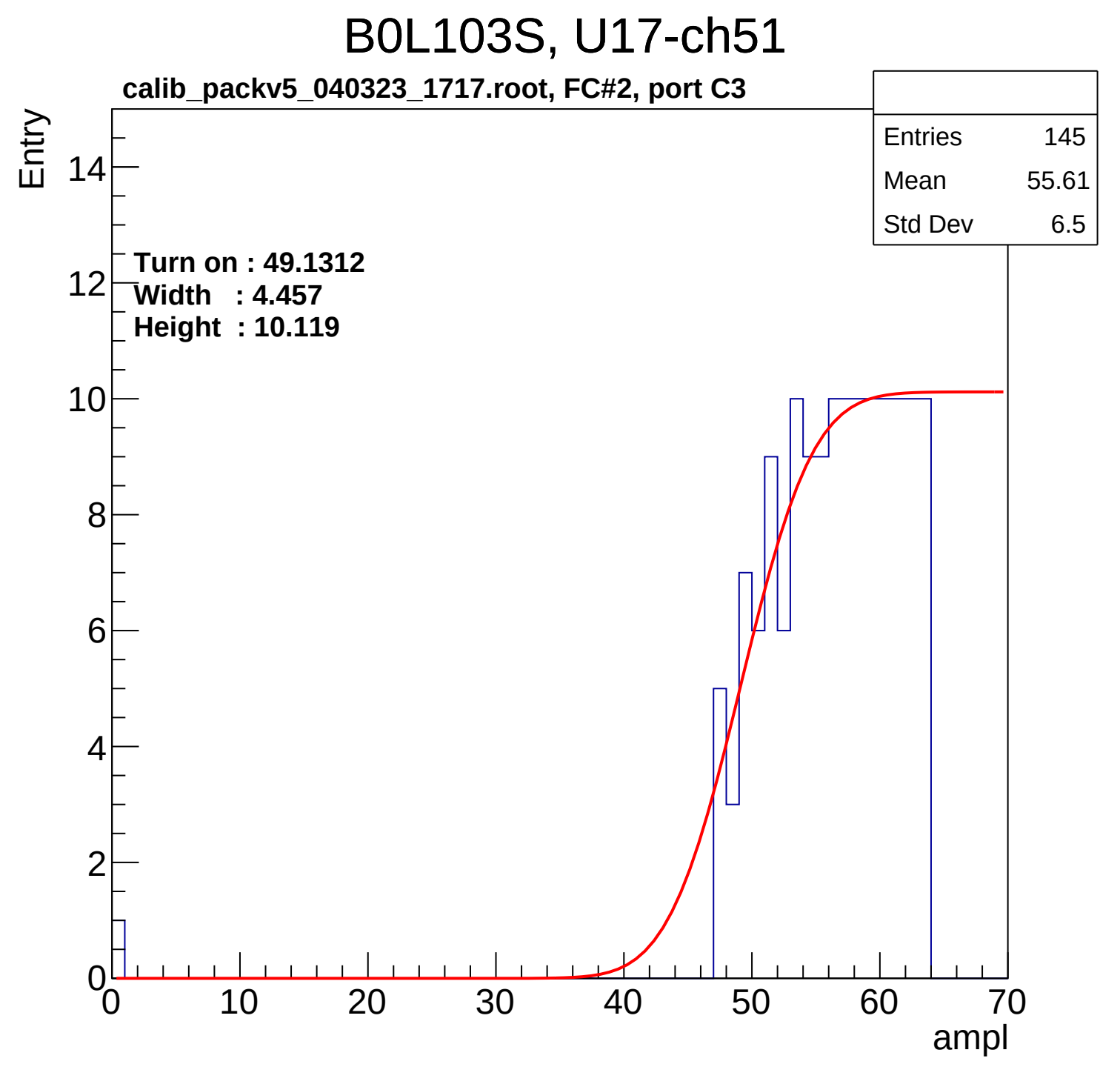
B0L103S, U17-ch51
calib_packv5_040323_1717.root, FC#2, port C3
Entries 145
Mean 55.61
Std Dev 6.5
Turn on : 49.1312
Width : 4.457
Height : 10.119
Entry
ampl
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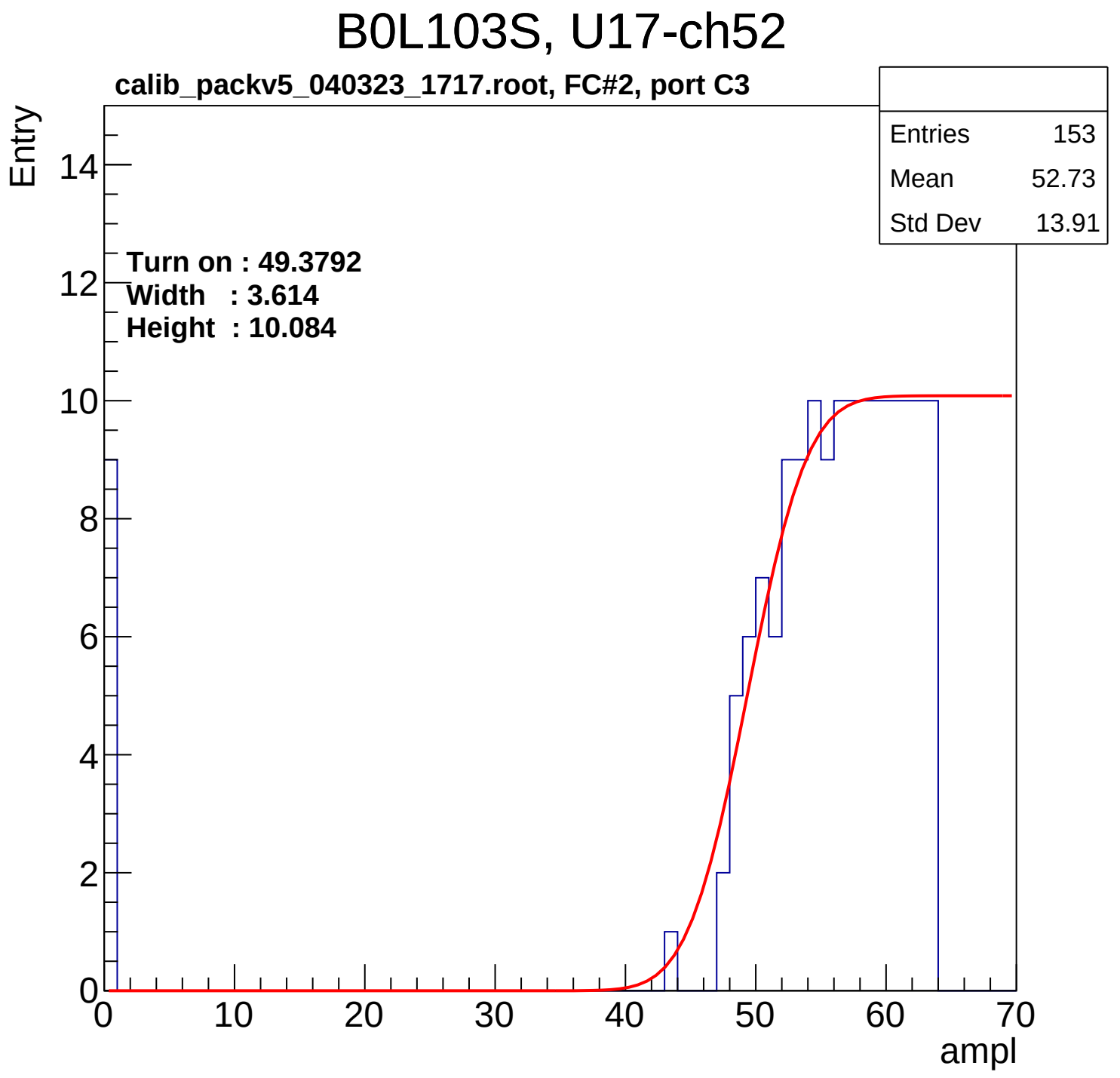
B0L103S, U17-ch52
calib_packv5_040323_1717.root, FC#2, port C3
Entries 153
Mean 52.73
Std Dev 13.91
Turn on : 49.3792
Width : 3.614
Height : 10.084
Entry
ampl
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6
8
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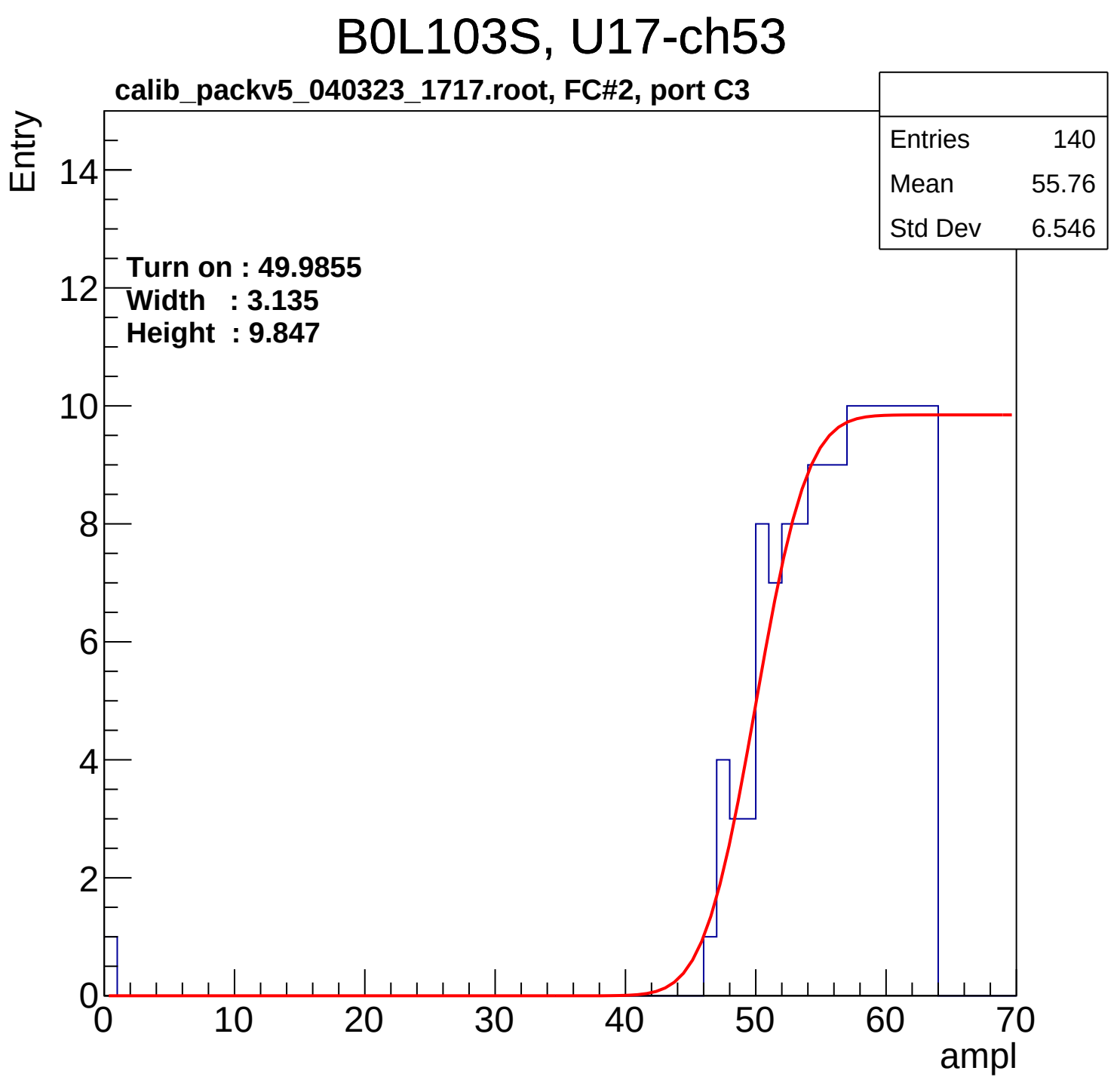
B0L103S, U17-ch53
calib_packv5_040323_1717.root, FC#2, port C3
Entries 140
Mean 55.76
Std Dev 6.546
Turn on : 49.9855
Width : 3.135
Height : 9.847
Entry
ampl
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6
8
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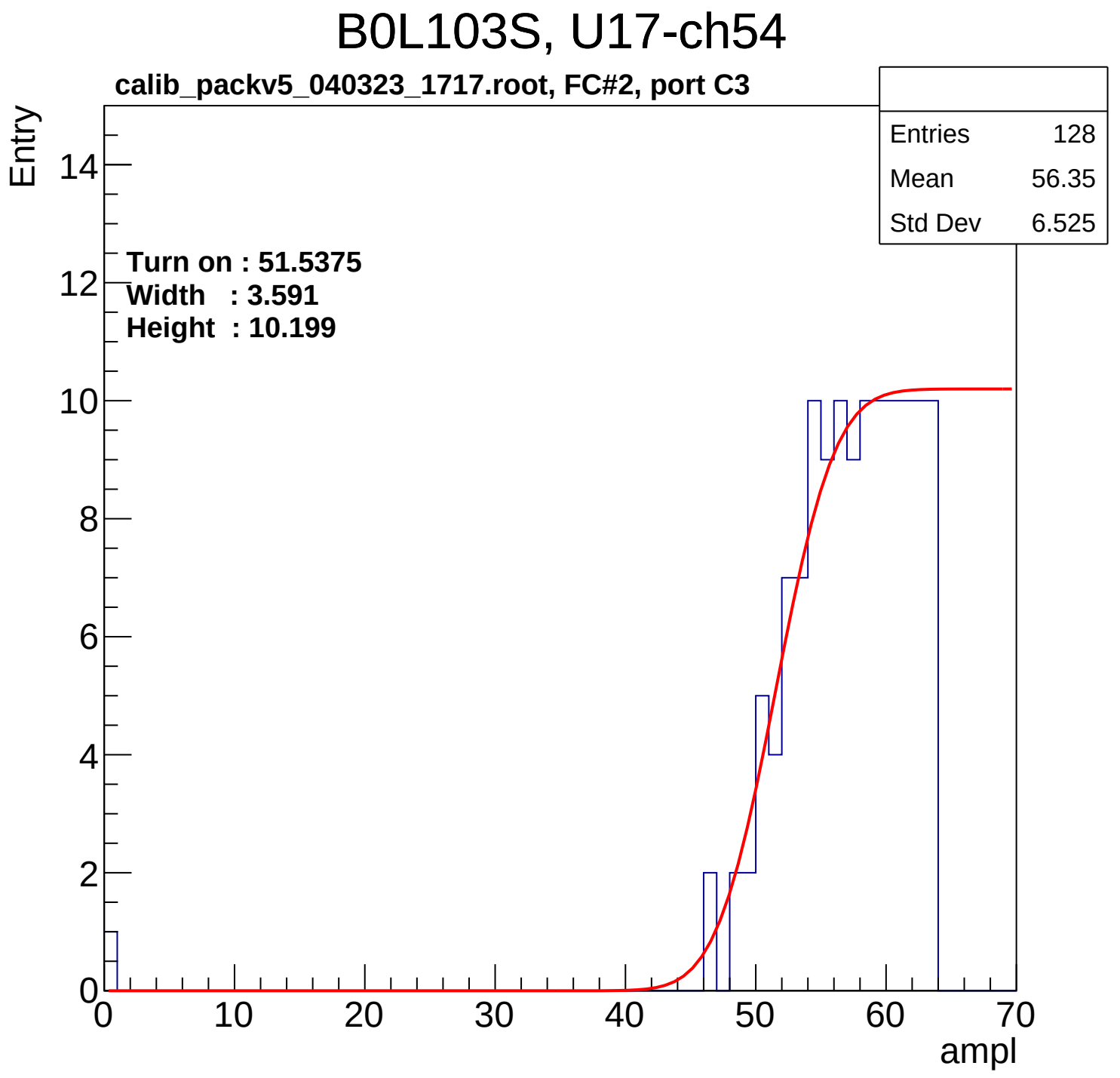
B0L103S, U17-ch54
calib_packv5_040323_1717.root, FC#2, port C3
Entries 128
Mean 56.35
Std Dev 6.525
Turn on : 51.5375
Width : 3.591
Height : 10.199
Entry
ampl
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6
8
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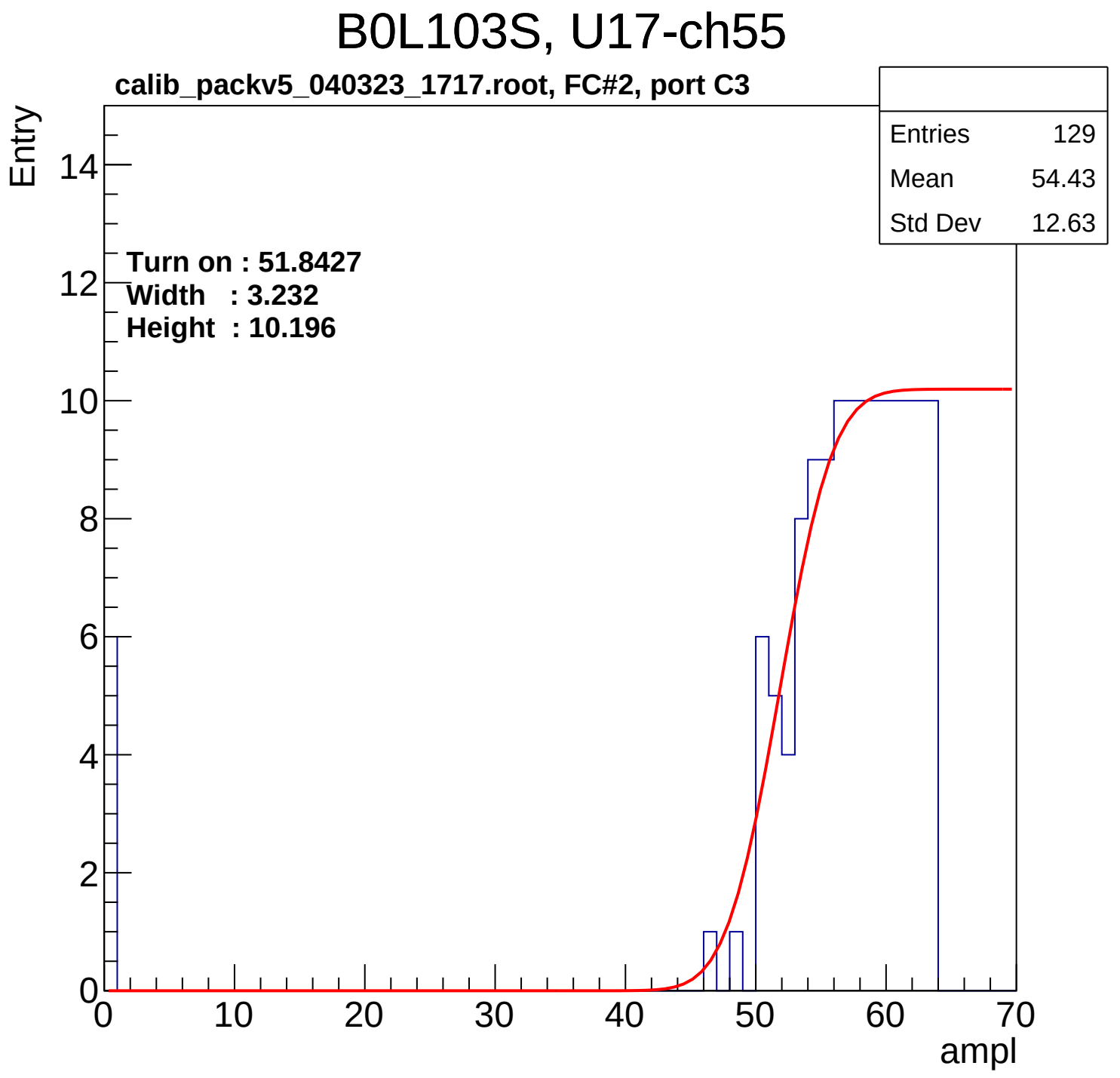
B0L103S, U17-ch55
calib_packv5_040323_1717.root, FC#2, port C3
Entries 129
Mean 54.43
Std Dev 12.63
Turn on : 51.8427
Width : 3.232
Height : 10.196
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ampl
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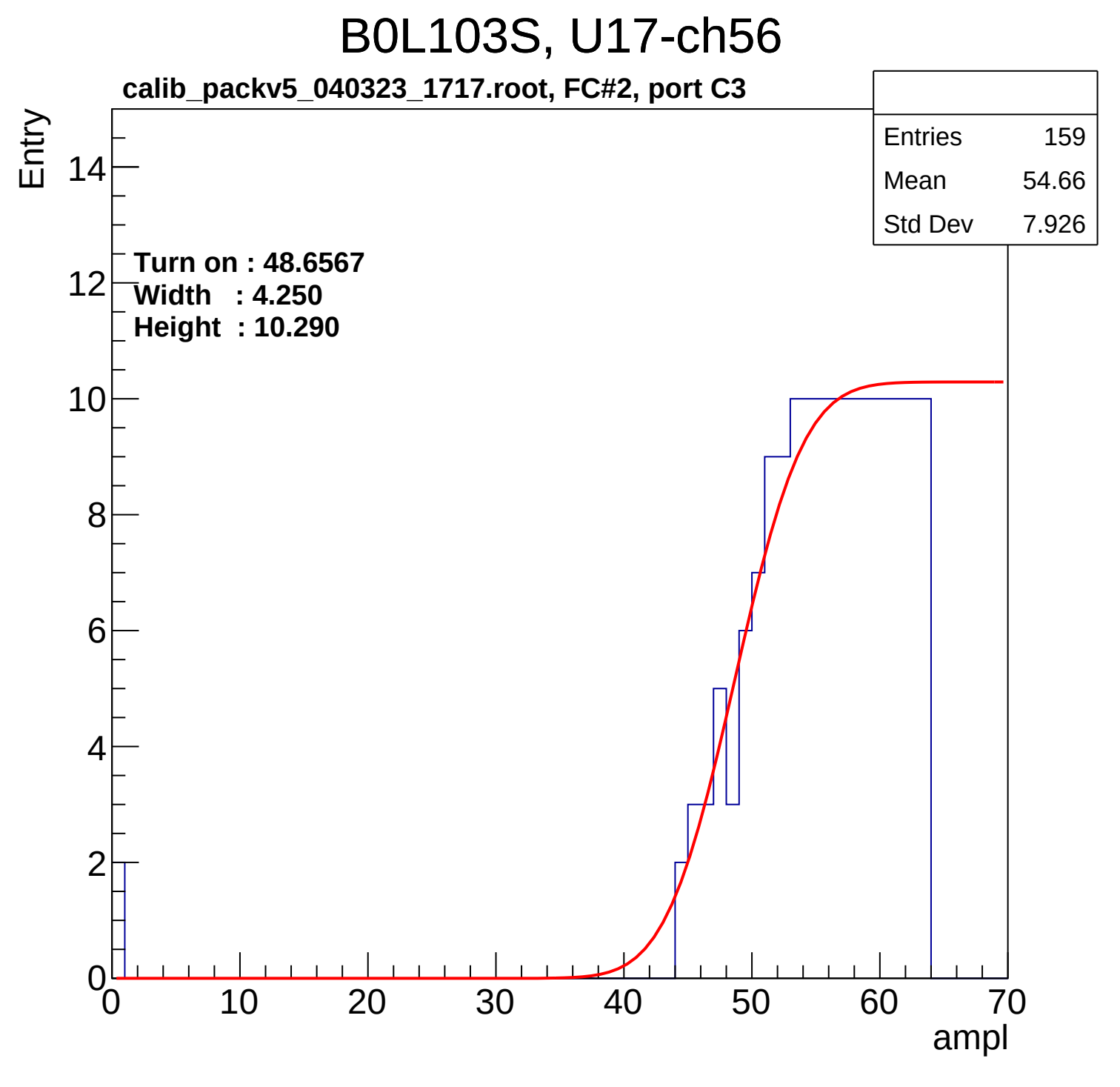
B0L103S, U17-ch56
calib_packv5_040323_1717.root, FC#2, port C3
Entries 159
Mean 54.66
Std Dev 7.926
Turn on : 48.6567
Width : 4.250
Height : 10.290
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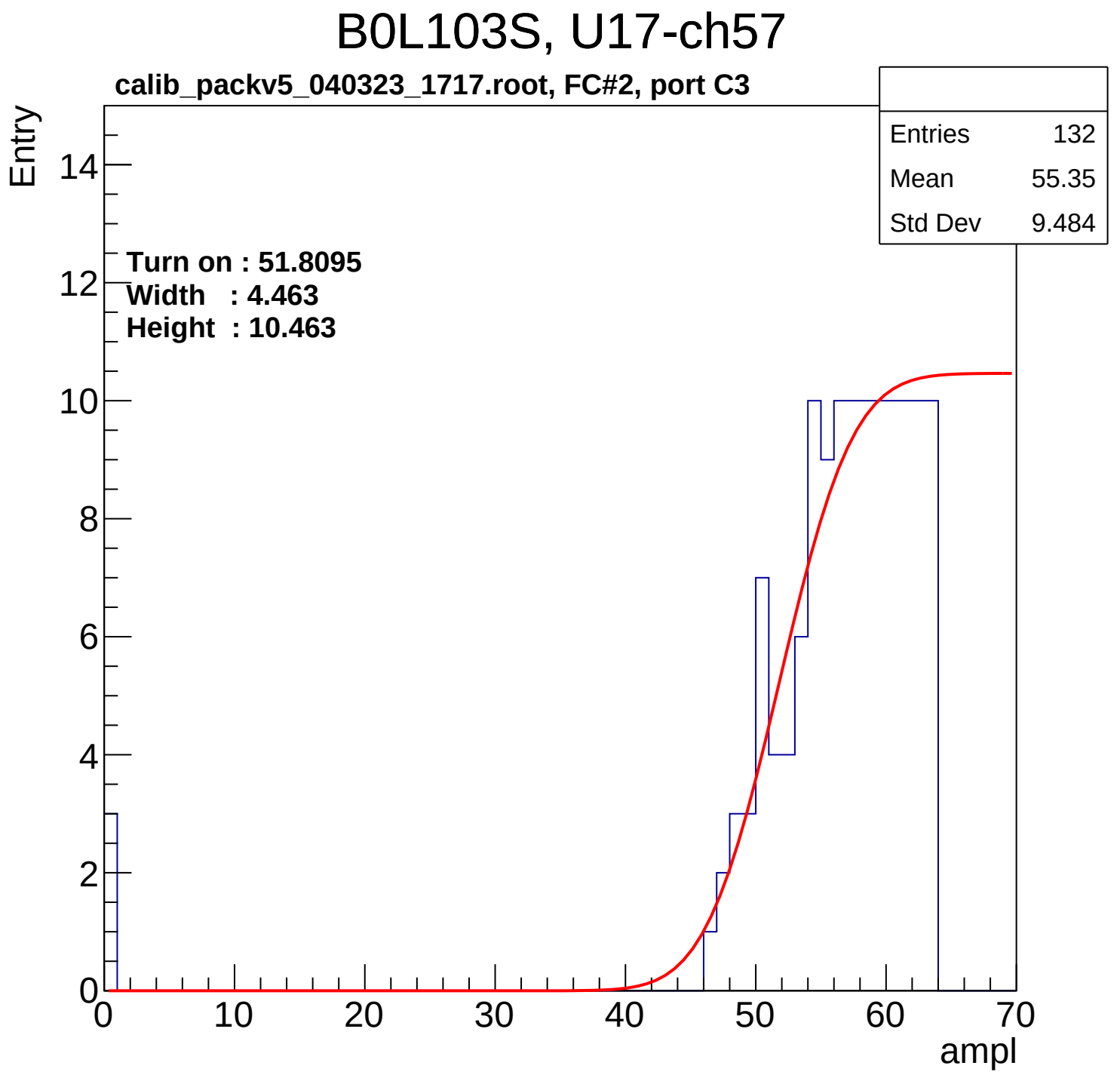
B0L103S, U17-ch57
calib_packv5_040323_1717.root, FC#2, port C3
Entries 132
Mean 55.35
Std Dev 9.484
Turn on : 51.8095
Width : 4.463
Height : 10.463
Entry
ampl
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4
6
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12
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20
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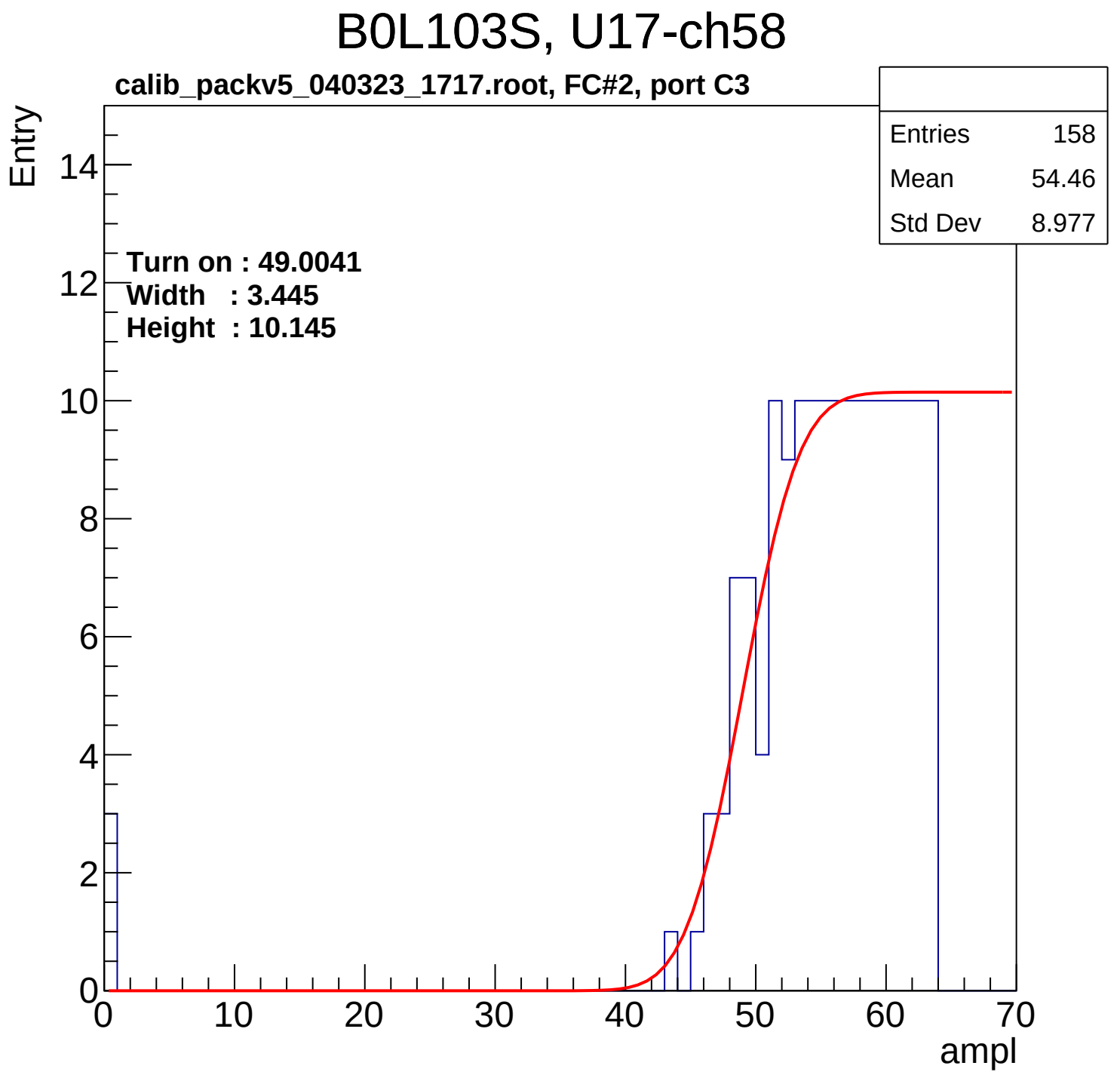
B0L103S, U17-ch58
calib_packv5_040323_1717.root, FC#2, port C3
Entries 158
Mean 54.46
Std Dev 8.977
Turn on : 49.0041
Width : 3.445
Height : 10.145
Entry
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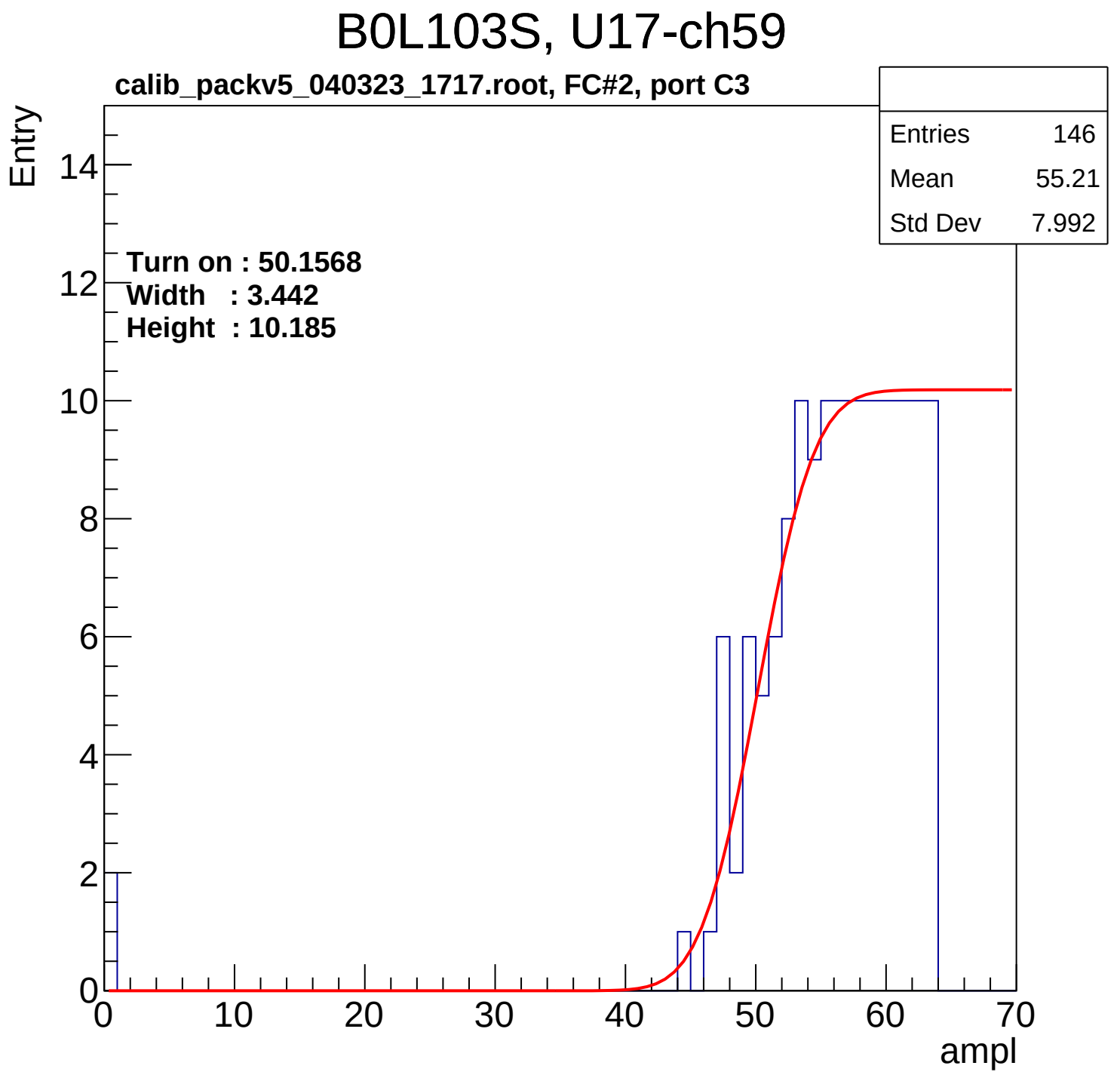
B0L103S, U17-ch59
calib_packv5_040323_1717.root, FC#2, port C3
Entries 146
Mean 55.21
Std Dev 7.992
Turn on : 50.1568
Width : 3.442
Height : 10.185
Entry
ampl
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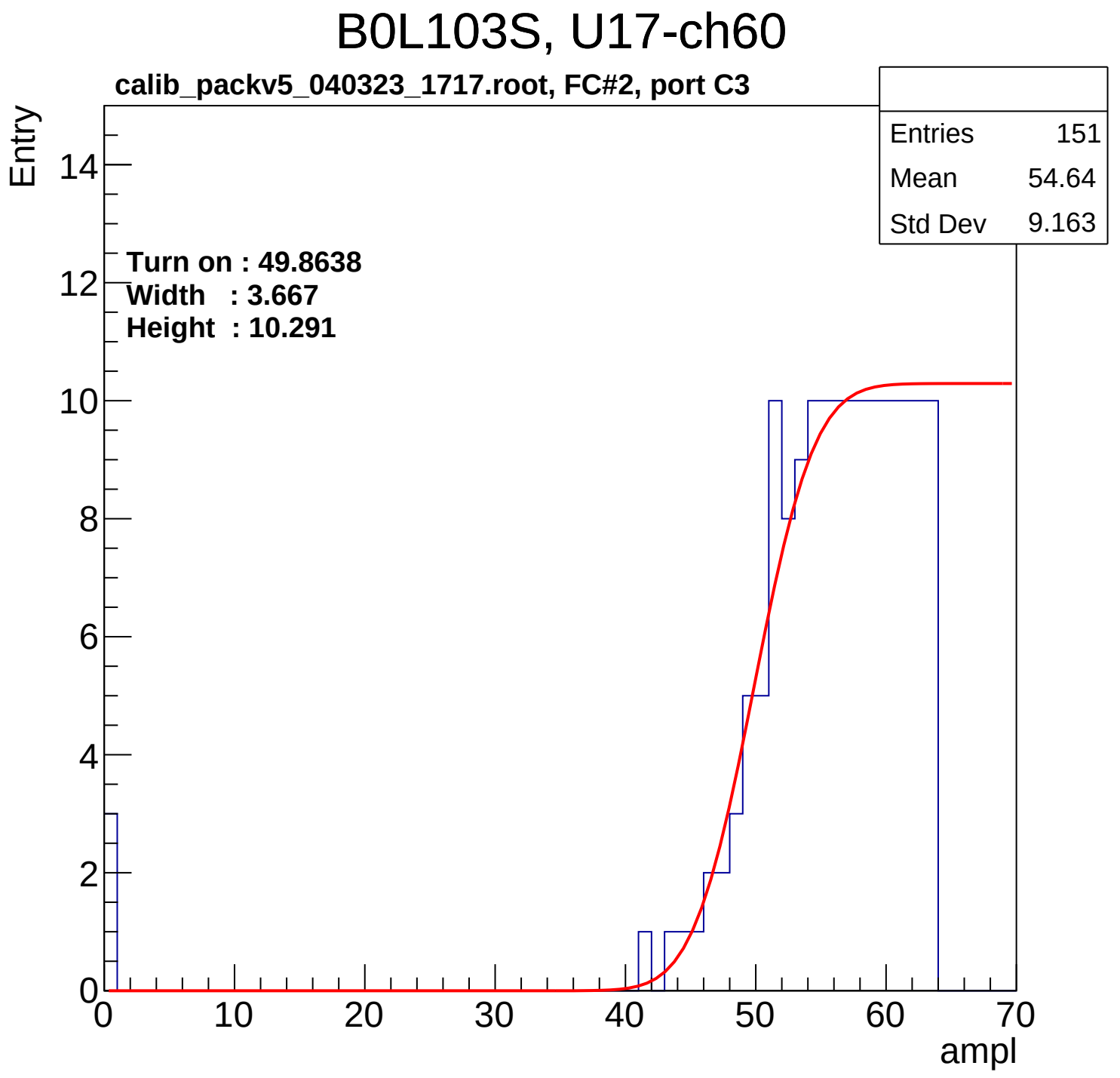
B0L103S, U17-ch60
calib_packv5_040323_1717.root, FC#2, port C3
Entries 151
Mean 54.64
Std Dev 9.163
Turn on : 49.8638
Width : 3.667
Height : 10.291
Entry
ampl
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8
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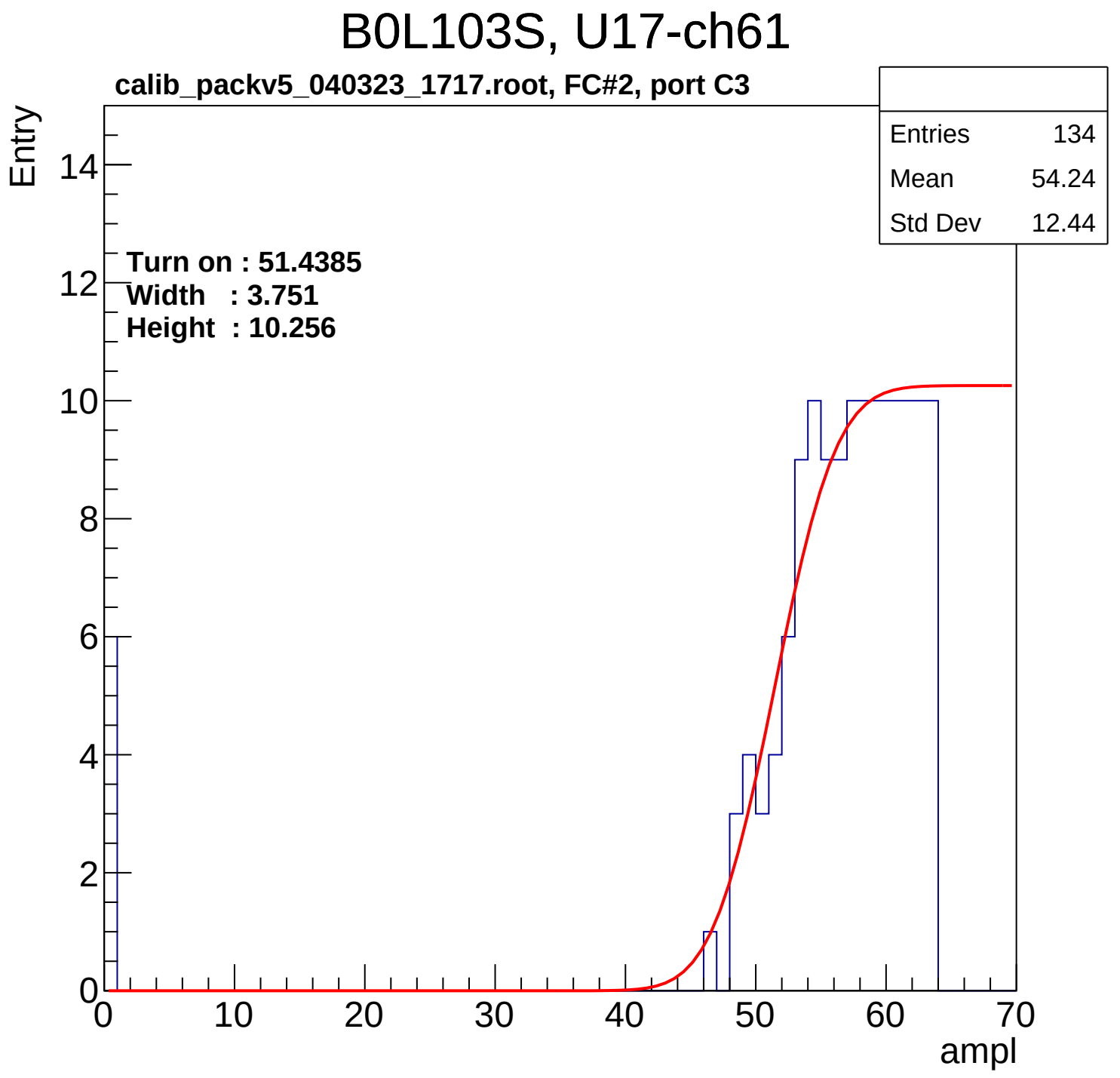
B0L103S, U17-ch61
calib_packv5_040323_1717.root, FC#2, port C3
Entries 134
Mean 54.24
Std Dev 12.44
Turn on : 51.4385
Width : 3.751
Height : 10.256
Entry
ampl
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2
4
6
8
10
12
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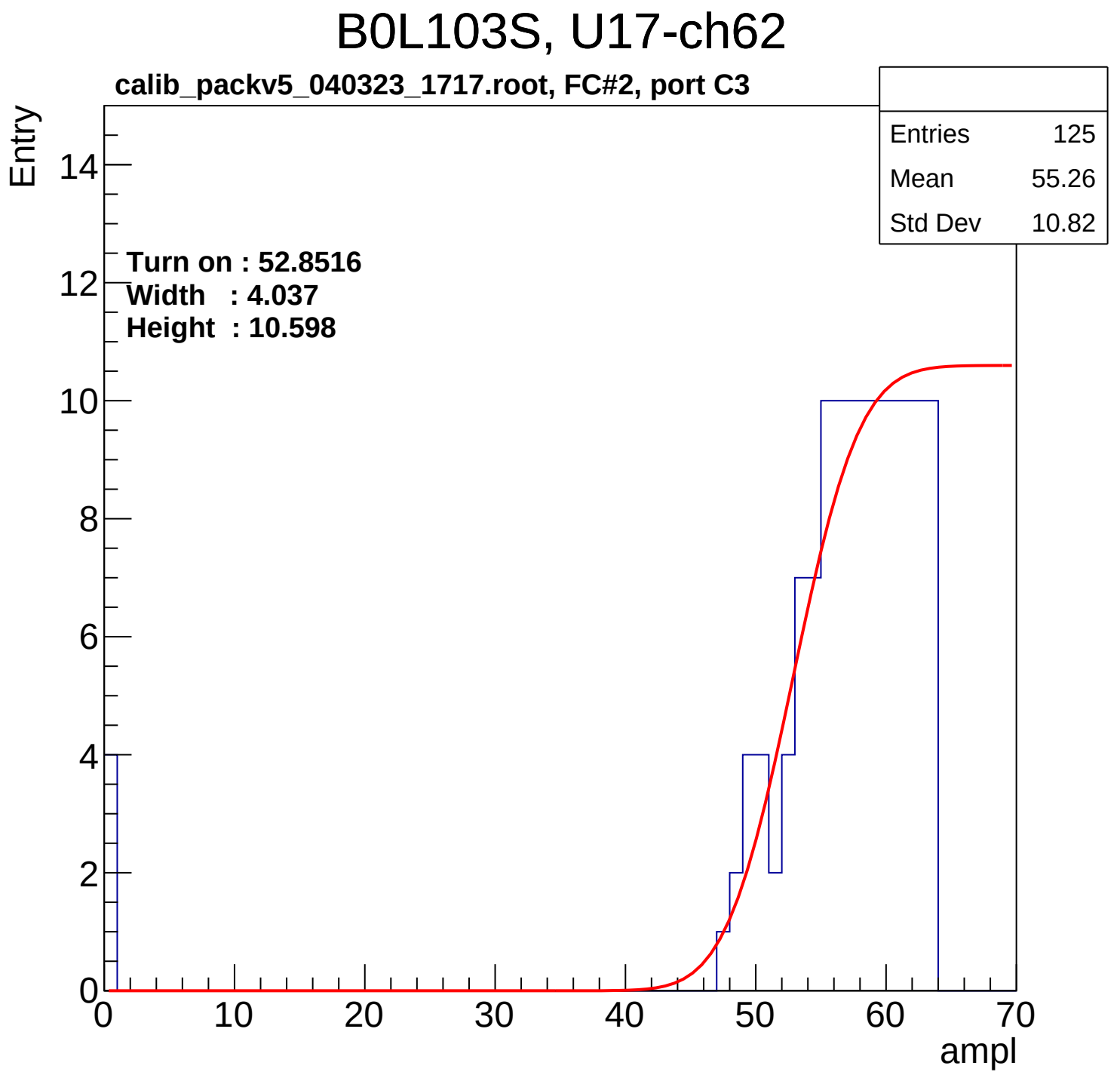
B0L103S, U17-ch62
calib_packv5_040323_1717.root, FC#2, port C3
Entries 125
Mean 55.26
Std Dev 10.82
Turn on : 52.8516
Width : 4.037
Height : 10.598
Entry
ampl
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4
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8
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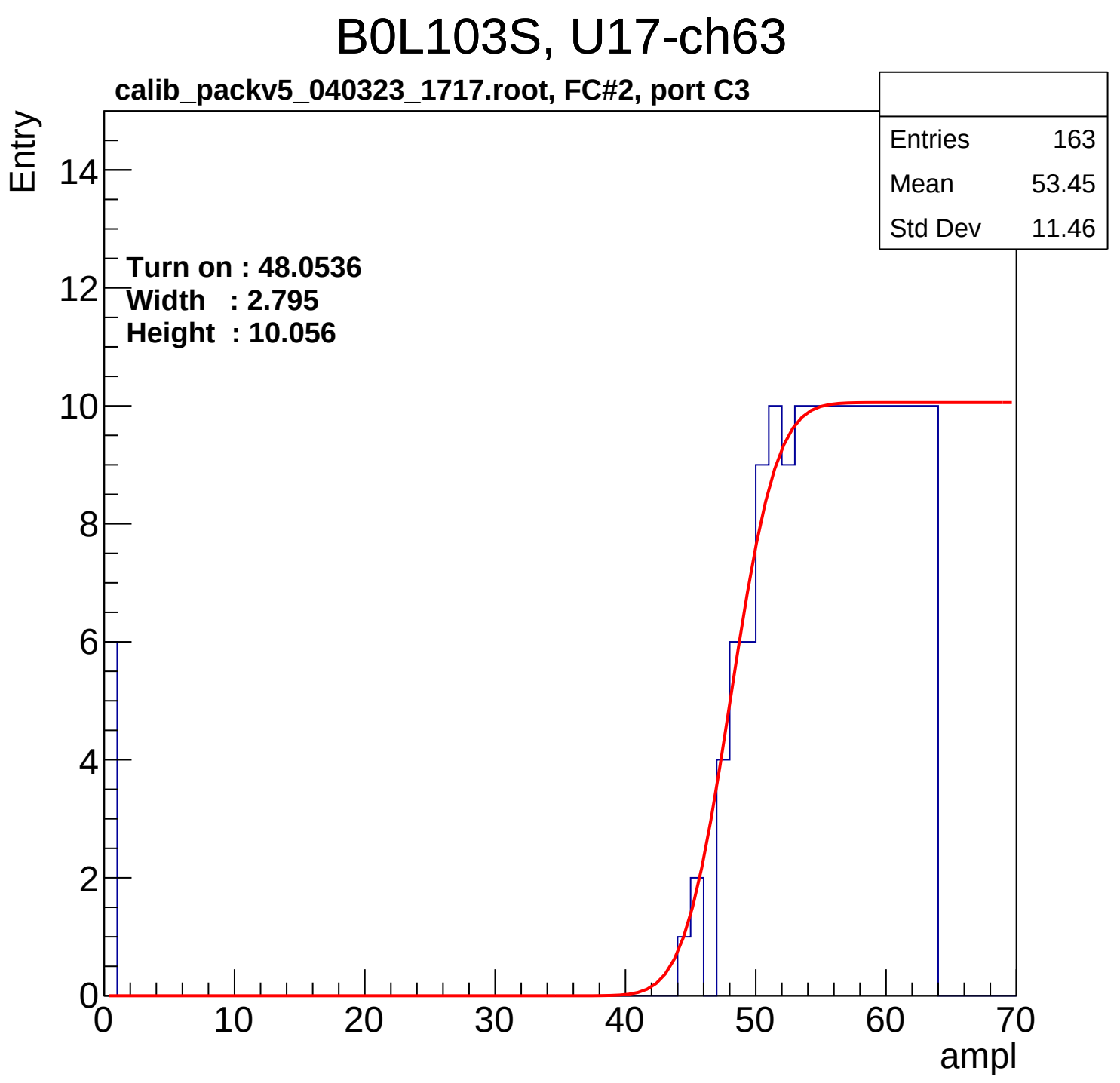
B0L103S, U17-ch63
calib_packv5_040323_1717.root, FC#2, port C3
Entries 163
Mean 53.45
Std Dev 11.46
Turn on : 48.0536
Width : 2.795
Height : 10.056
Entry
ampl
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2
4
6
8
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0
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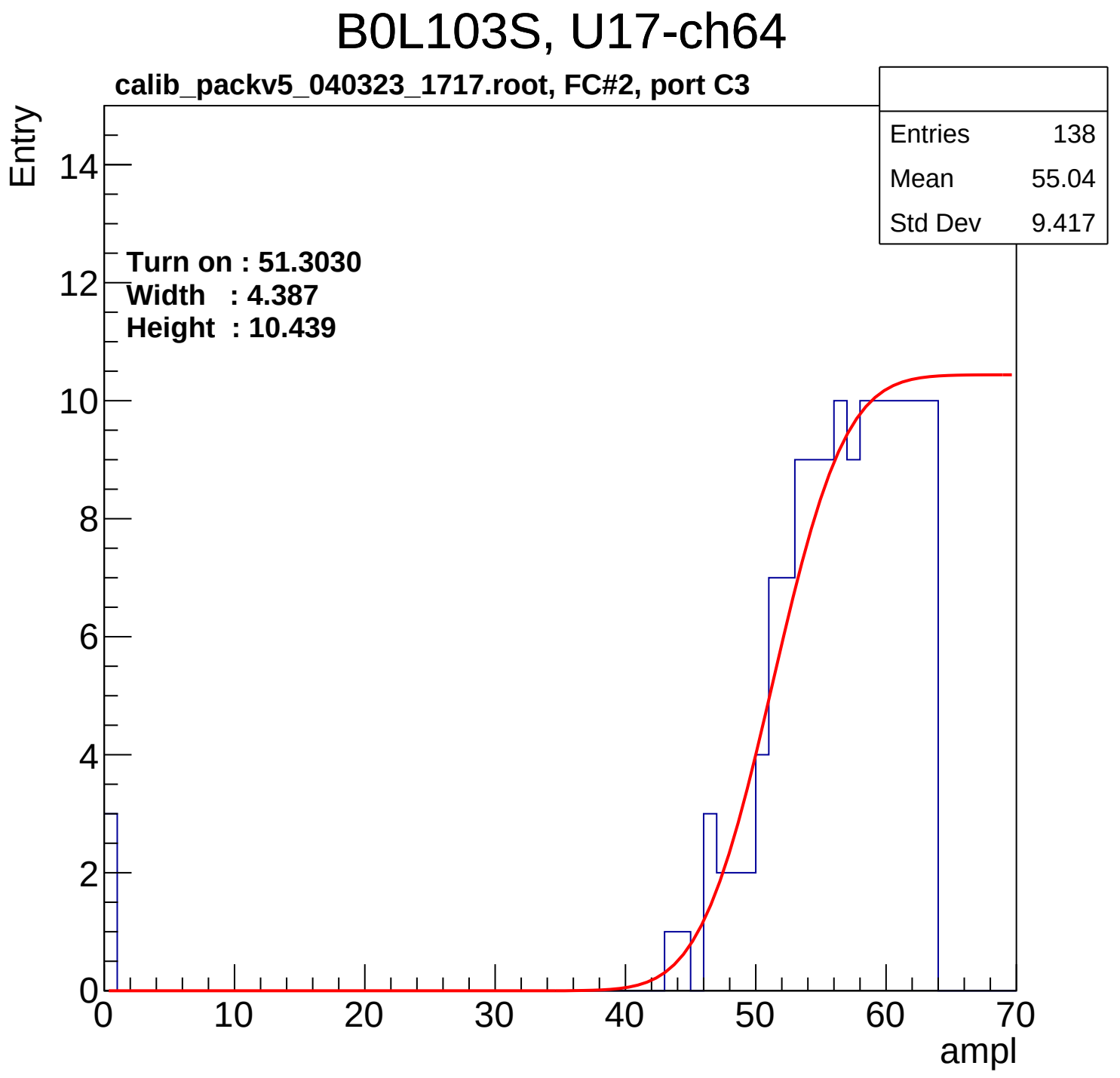
B0L103S, U17-ch64
calib_packv5_040323_1717.root, FC#2, port C3
Entries 138
Mean 55.04
Std Dev 9.417
Turn on : 51.3030
Width : 4.387
Height : 10.439
Entry
ampl
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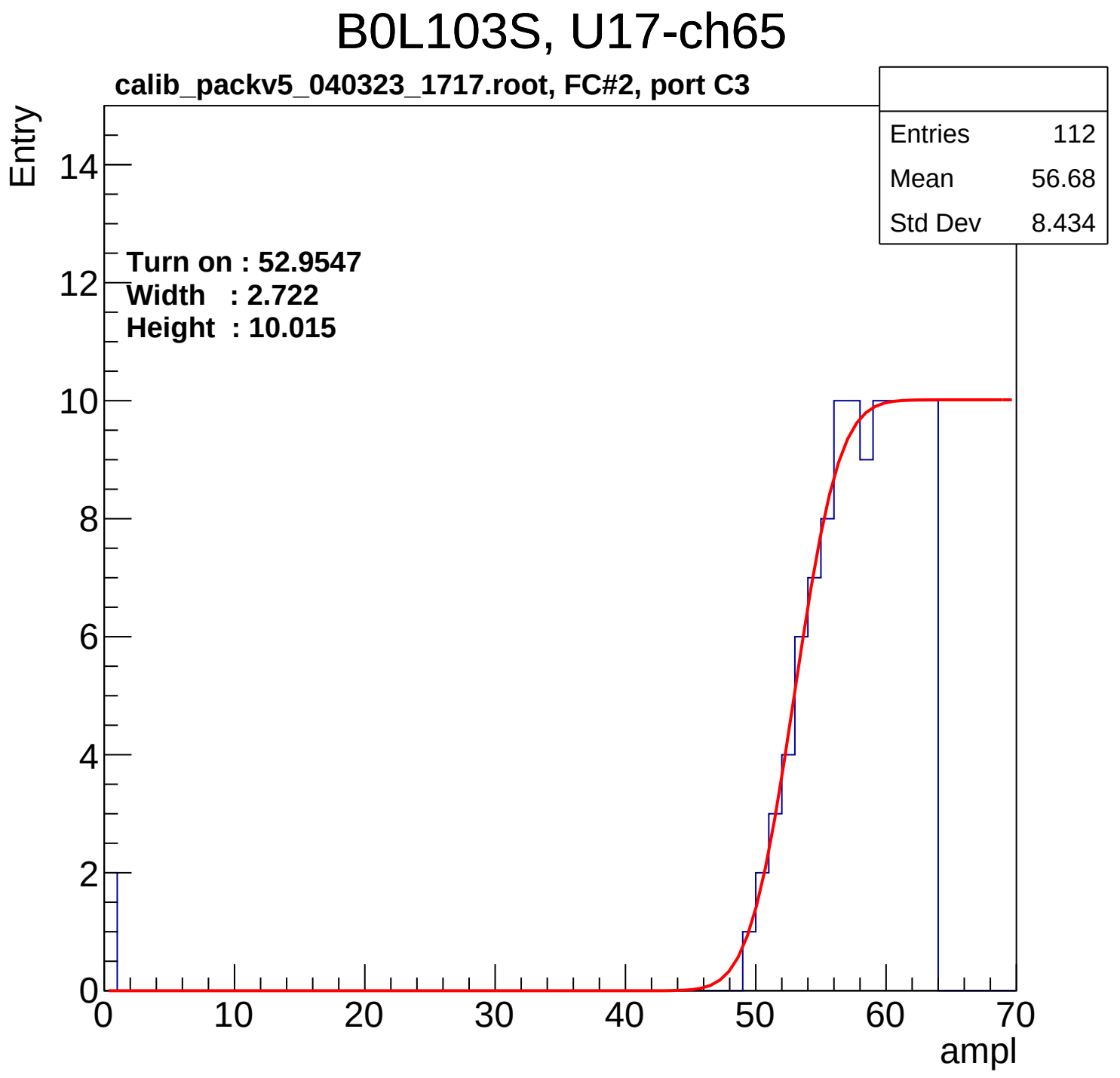
B0L103S, U17-ch65
calib_packv5_040323_1717.root, FC#2, port C3
Entries 112
Mean 56.68
Std Dev 8.434
Turn on : 52.9547
Width : 2.722
Height : 10.015
Entry
ampl
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2
4
6
8
10
12
14
0
10
20
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60
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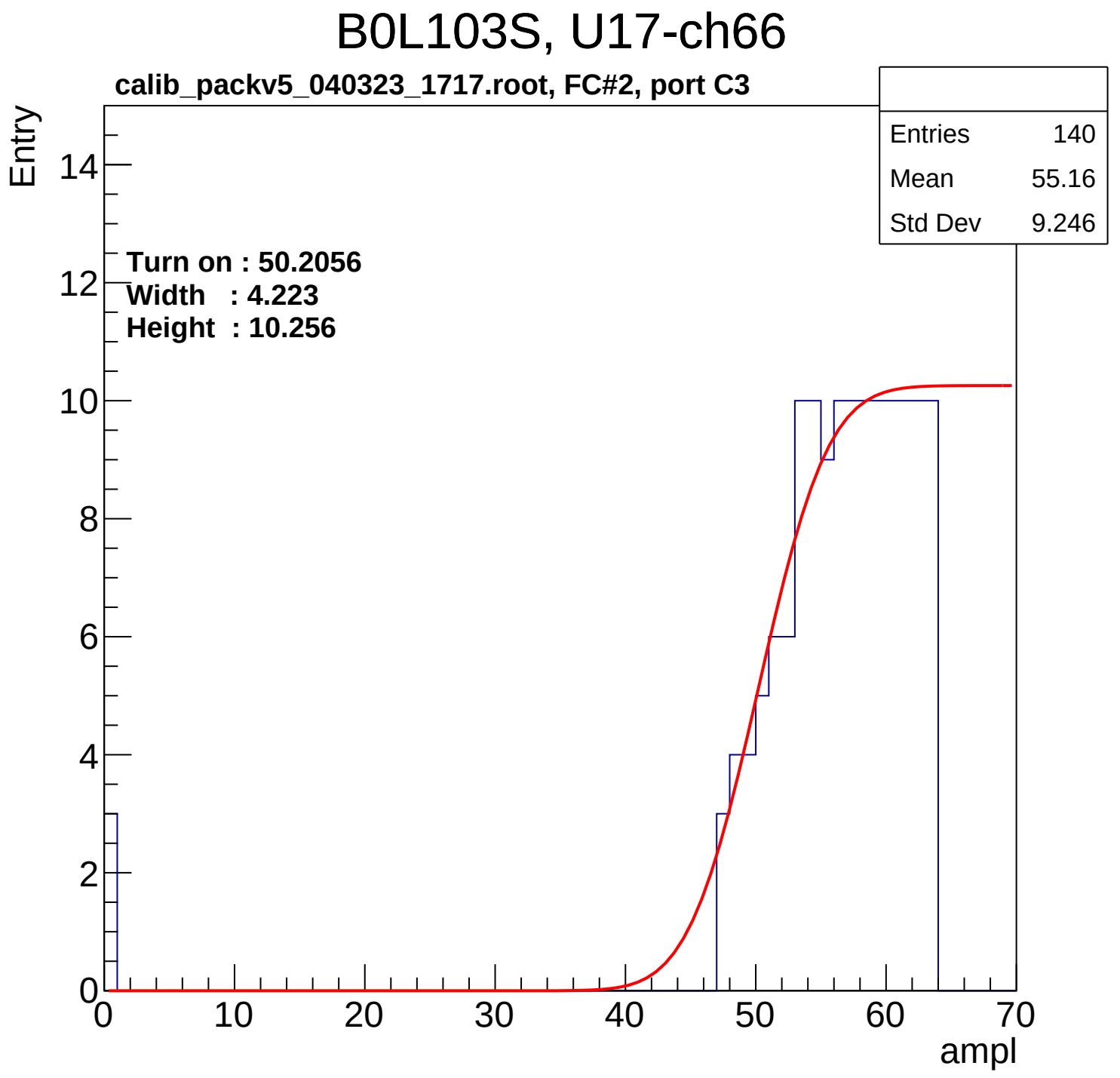
B0L103S, U17-ch66
calib_packv5_040323_1717.root, FC#2, port C3
Entries 140
Mean 55.16
Std Dev 9.246
Turn on : 50.2056
Width : 4.223
Height : 10.256
Entry
ampl
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8
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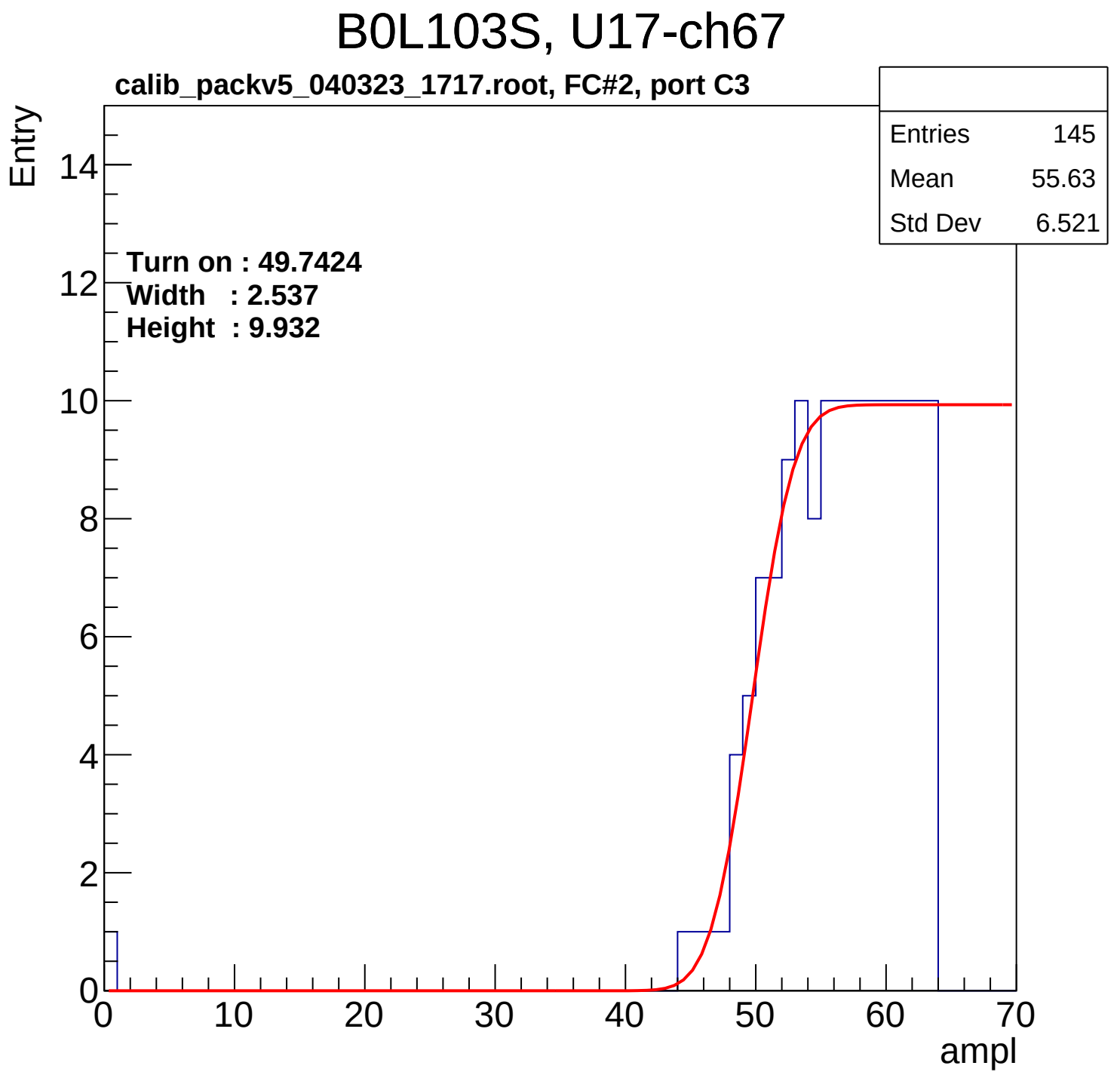
B0L103S, U17-ch67
calib_packv5_040323_1717.root, FC#2, port C3
Entries 145
Mean 55.63
Std Dev 6.521
Turn on : 49.7424
Width : 2.537
Height : 9.932
Entry
ampl
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6
8
10
12
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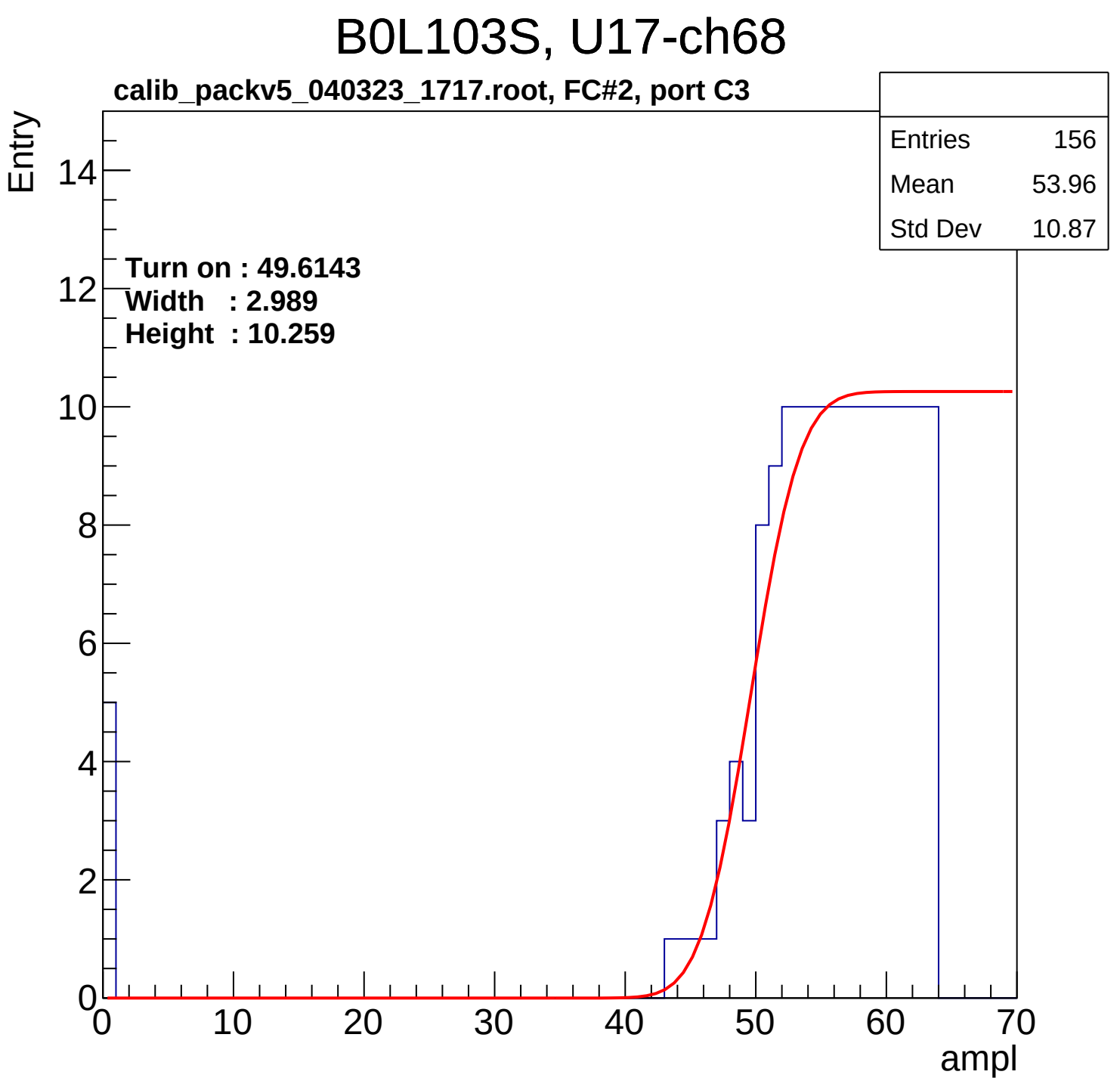
B0L103S, U17-ch68
calib_packv5_040323_1717.root, FC#2, port C3
Entries 156
Mean 53.96
Std Dev 10.87
Turn on : 49.6143
Width : 2.989
Height : 10.259
Entry
ampl
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6
8
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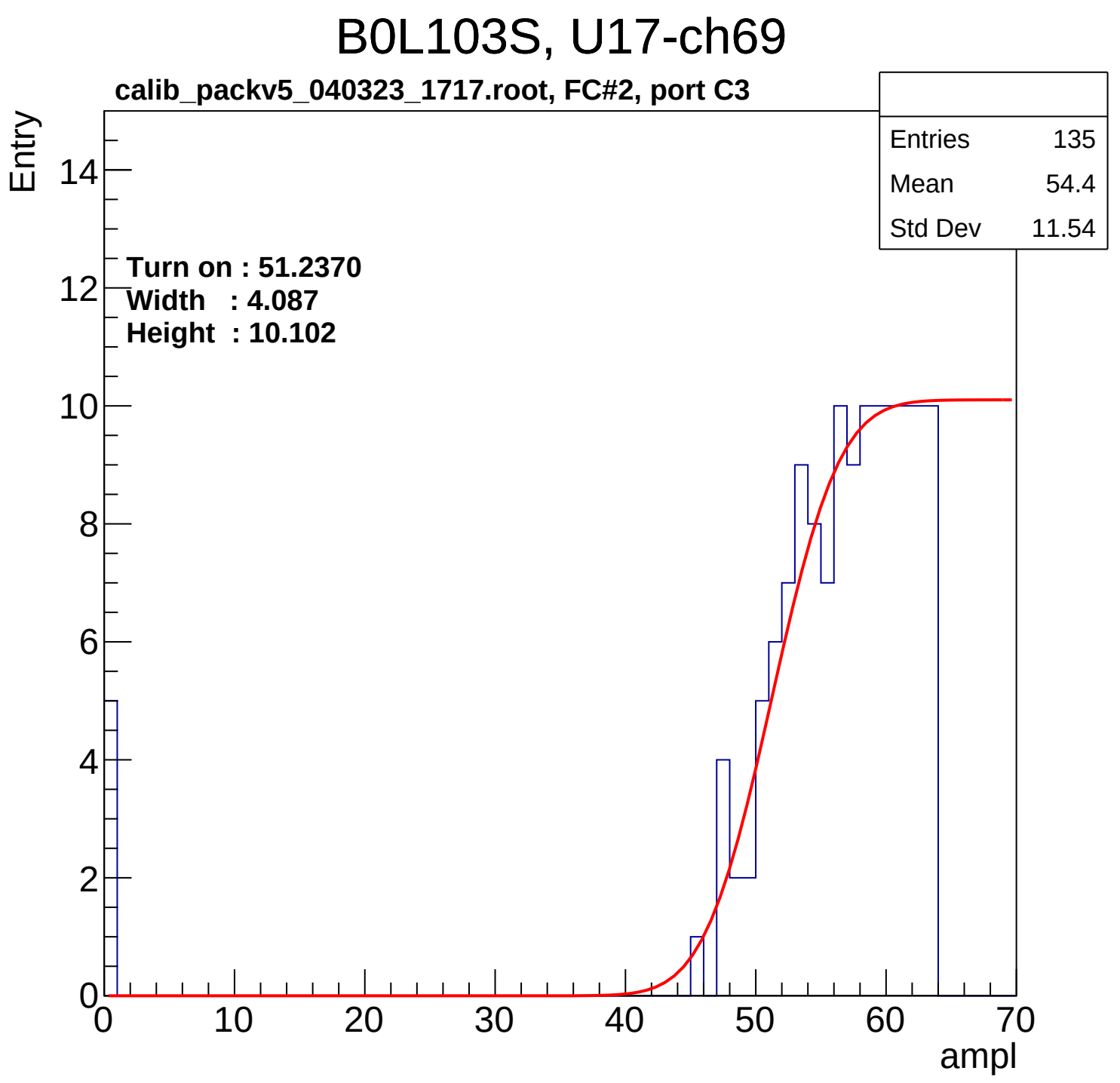
B0L103S, U17-ch69
calib_packv5_040323_1717.root, FC#2, port C3
Entries 135
Mean 54.4
Std Dev 11.54
Turn on : 51.2370
Width : 4.087
Height : 10.102
Entry
ampl
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6
8
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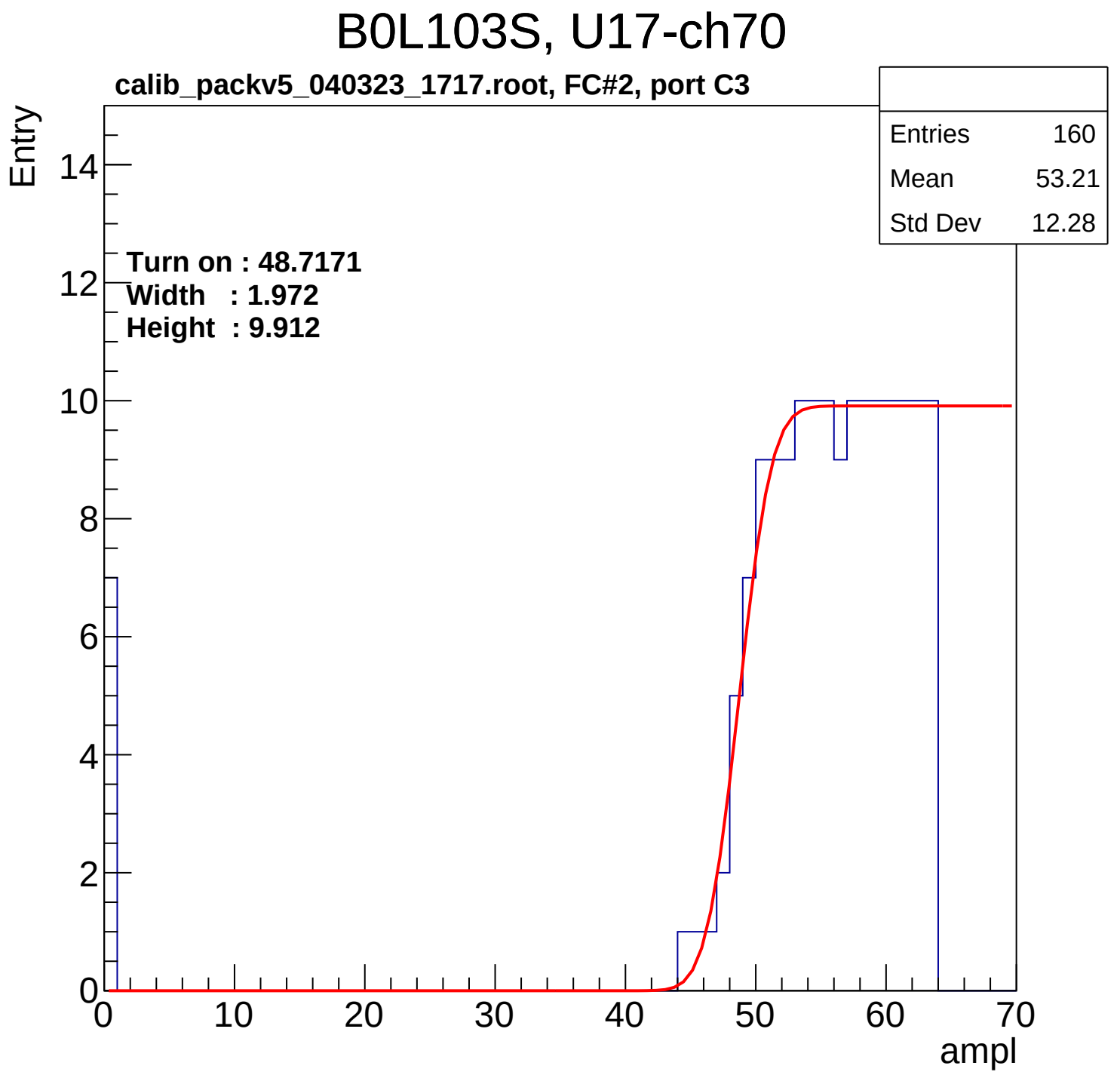
B0L103S, U17-ch70
calib_packv5_040323_1717.root, FC#2, port C3
Entries 160
Mean 53.21
Std Dev 12.28
Turn on : 48.7171
Width : 1.972
Height : 9.912
Entry
ampl
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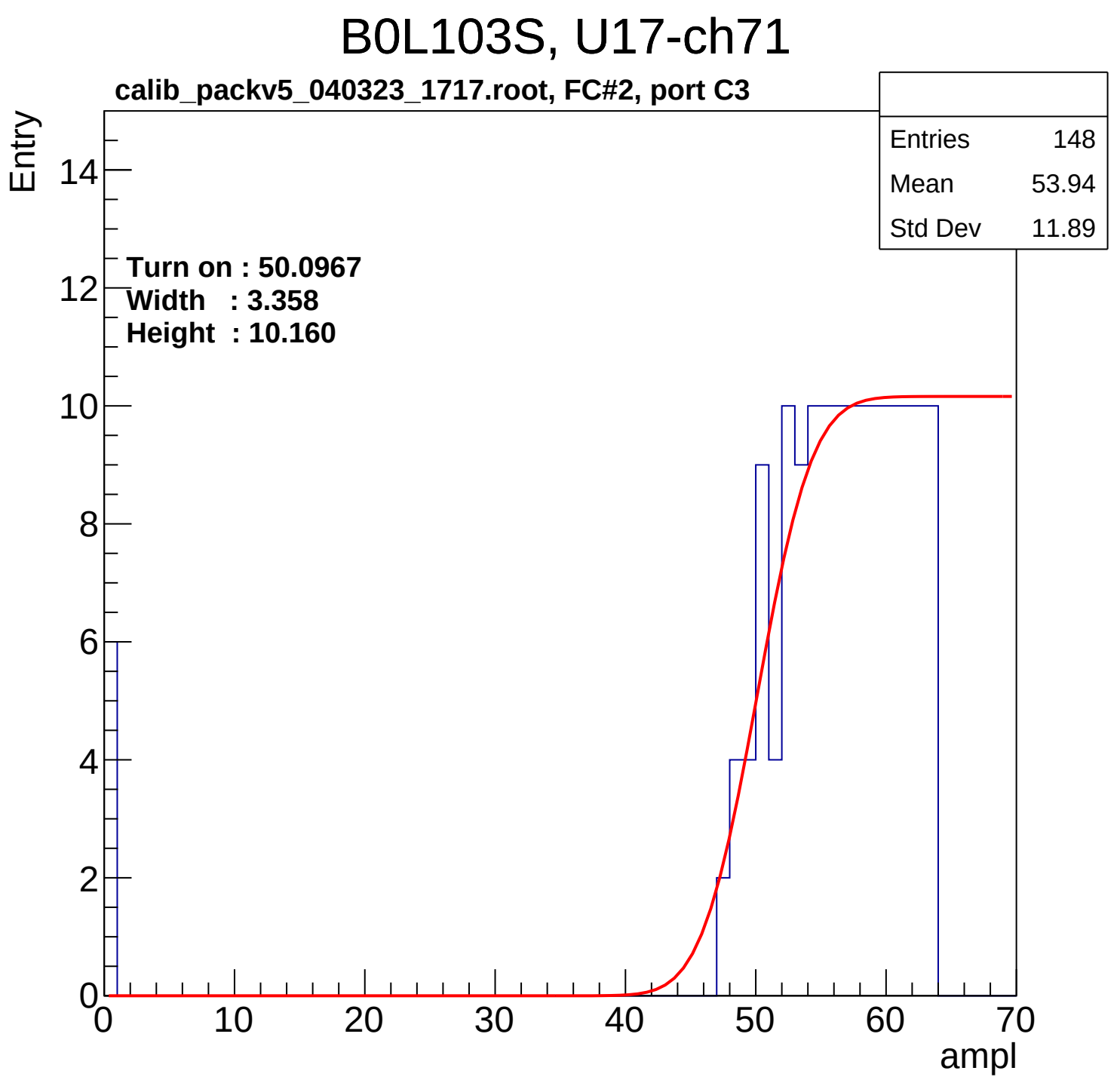
B0L103S, U17-ch71
calib_packv5_040323_1717.root, FC#2, port C3
Entries 148
Mean 53.94
Std Dev 11.89
Turn on : 50.0967
Width : 3.358
Height : 10.160
Entry
ampl
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8
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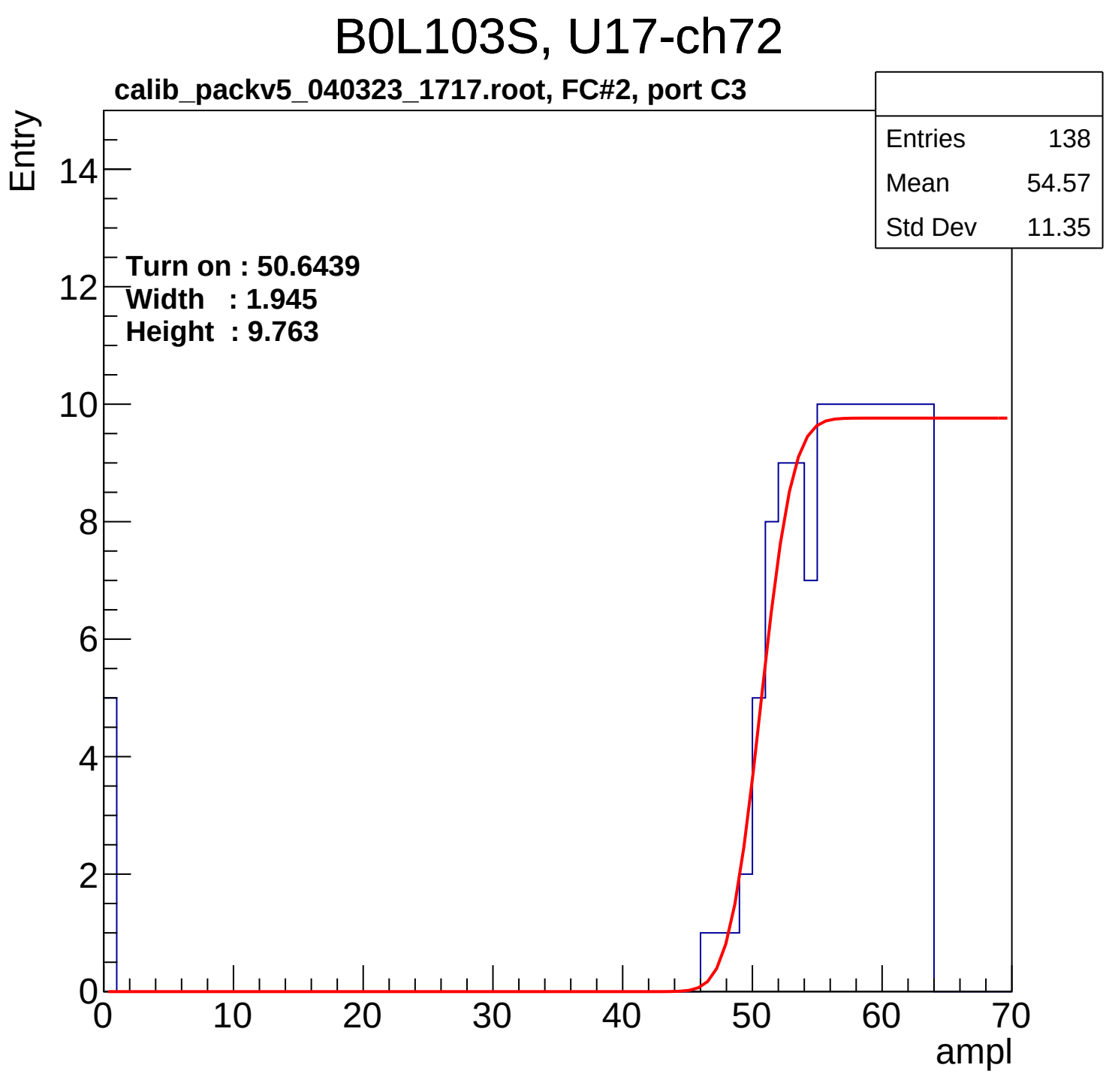
B0L103S, U17-ch72
calib_packv5_040323_1717.root, FC#2, port C3
Entries 138
Mean 54.57
Std Dev 11.35
Turn on : 50.6439
Width : 1.945
Height : 9.763
Entry
ampl
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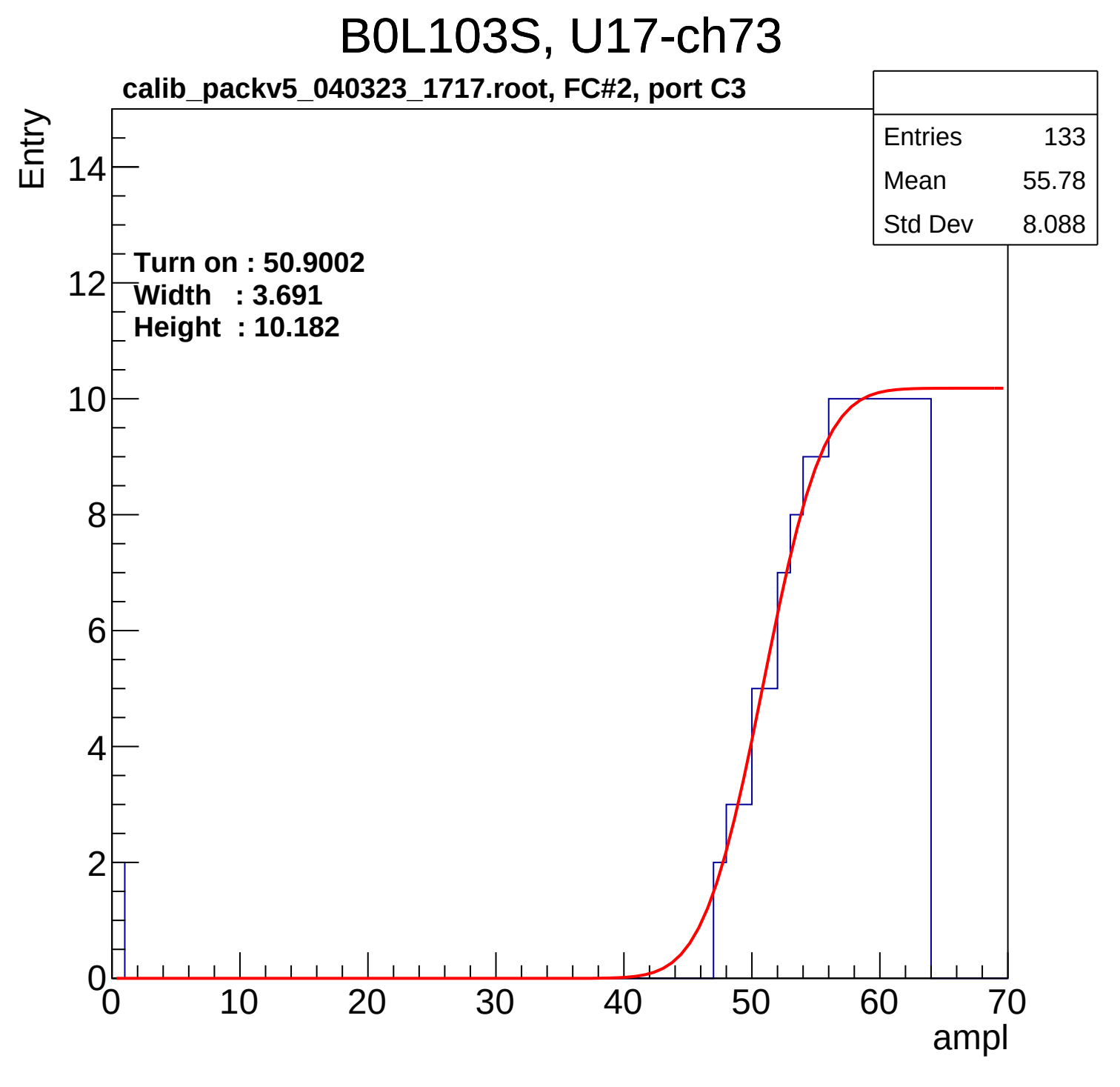
B0L103S, U17-ch73
calib_packv5_040323_1717.root, FC#2, port C3
Entries 133
Mean 55.78
Std Dev 8.088
Turn on : 50.9002
Width : 3.691
Height : 10.182
Entry
ampl
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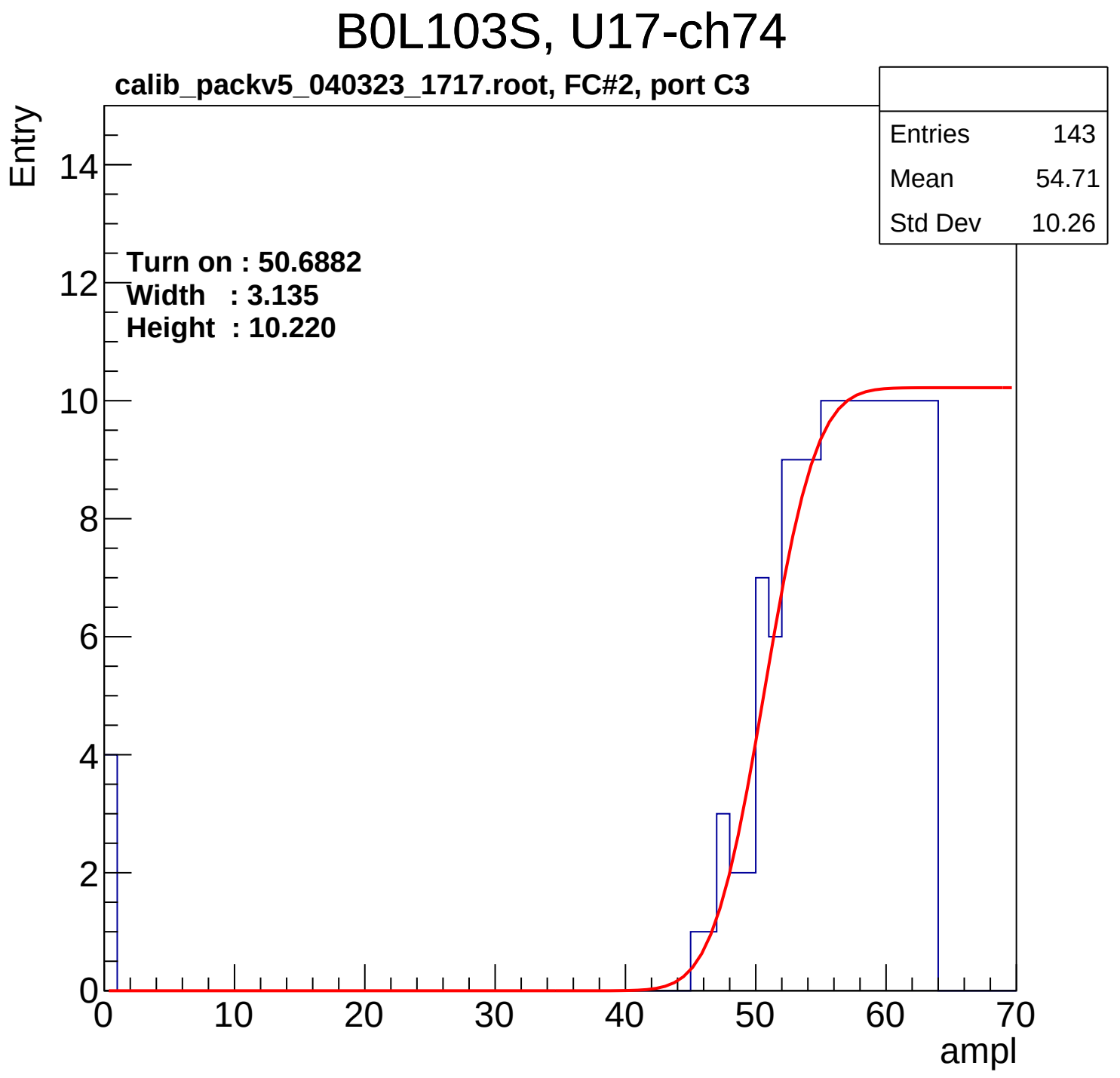
B0L103S, U17-ch74
calib_packv5_040323_1717.root, FC#2, port C3
Entries 143
Mean 54.71
Std Dev 10.26
Turn on : 50.6882
Width : 3.135
Height : 10.220
Entry
ampl
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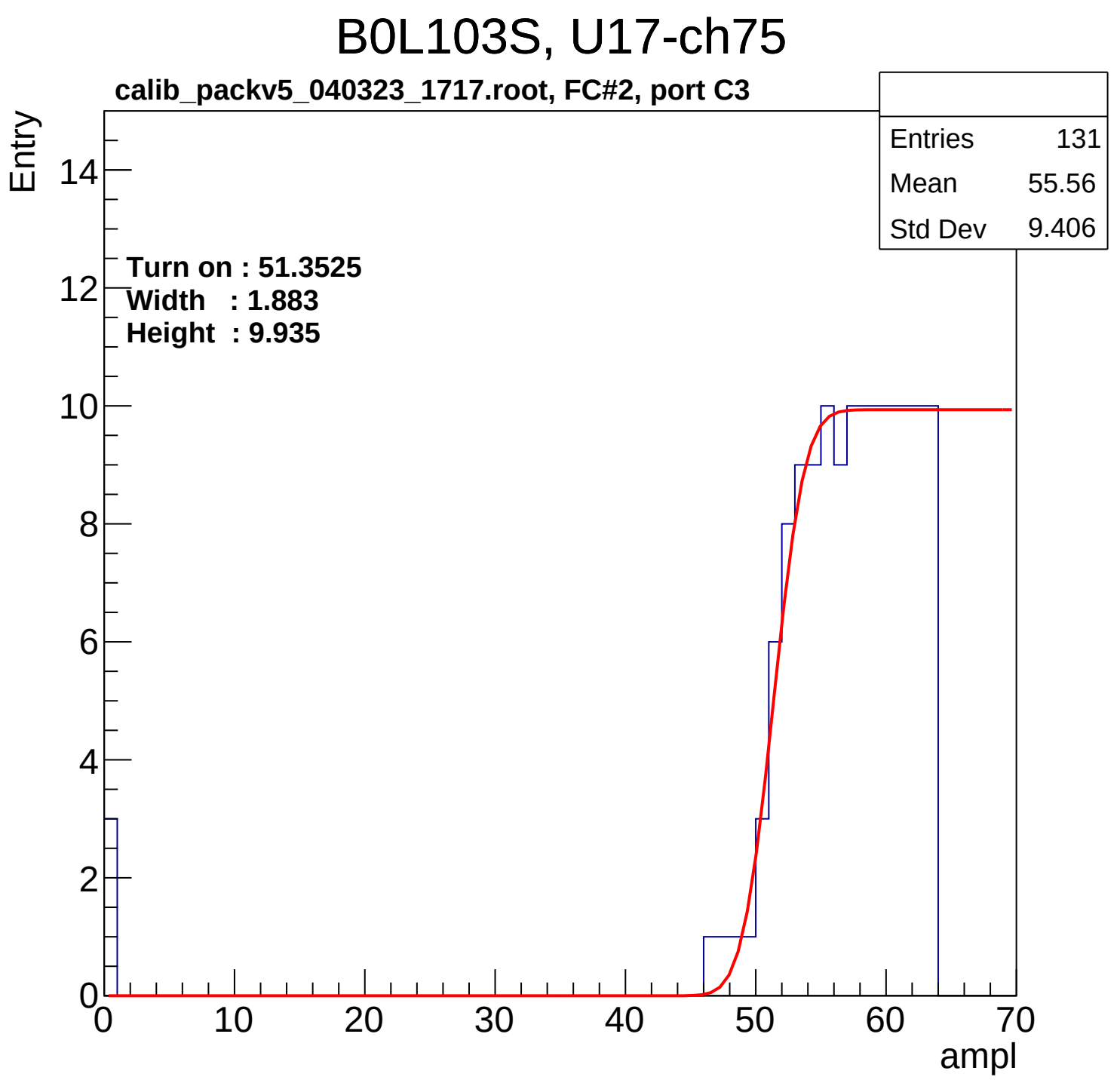
B0L103S, U17-ch75
calib_packv5_040323_1717.root, FC#2, port C3
Entries 131
Mean 55.56
Std Dev 9.406
Turn on : 51.3525
Width : 1.883
Height : 9.935
Entry
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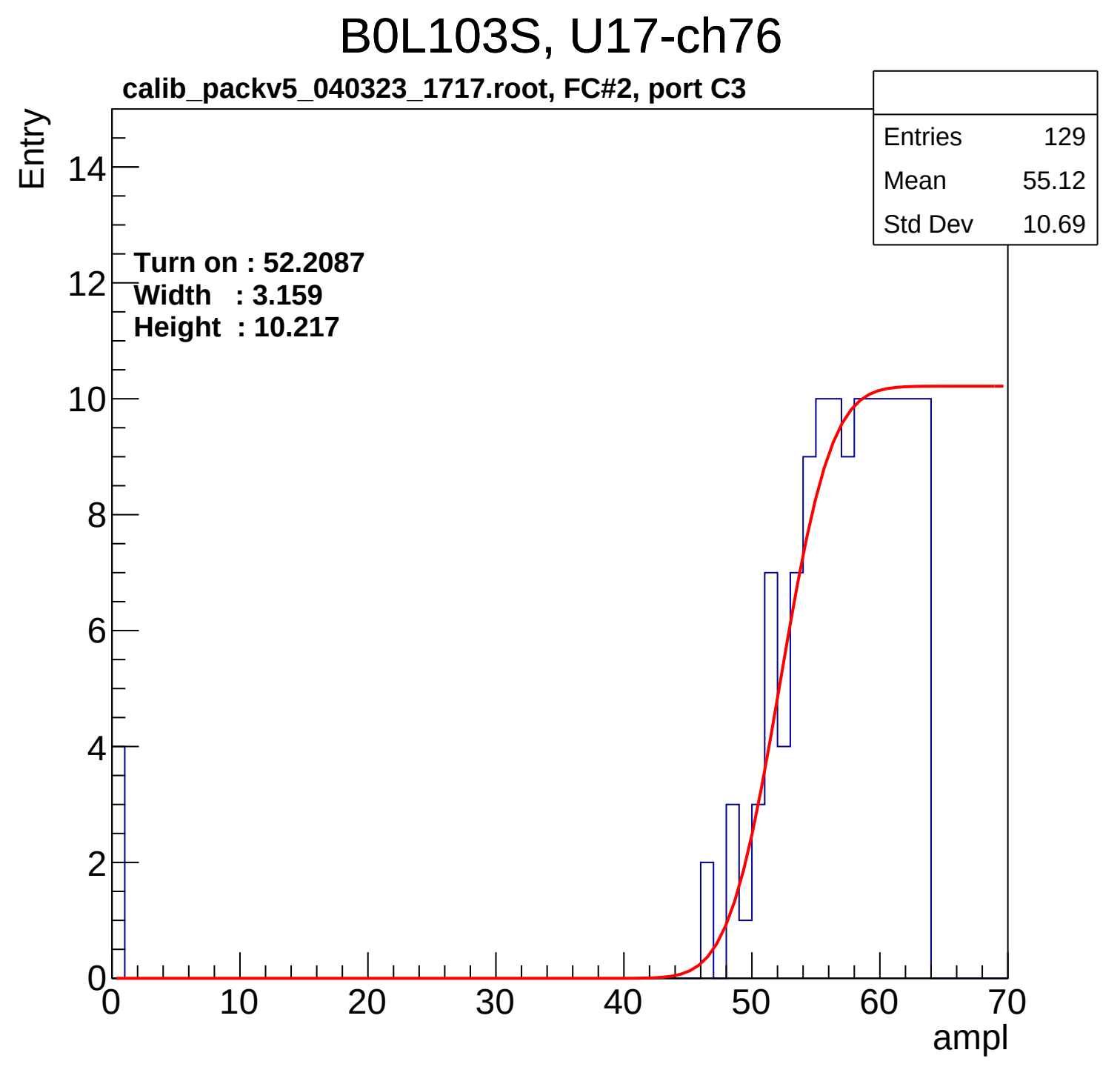
B0L103S, U17-ch76
calib_packv5_040323_1717.root, FC#2, port C3
Entries 129
Mean 55.12
Std Dev 10.69
Turn on : 52.2087
Width : 3.159
Height : 10.217
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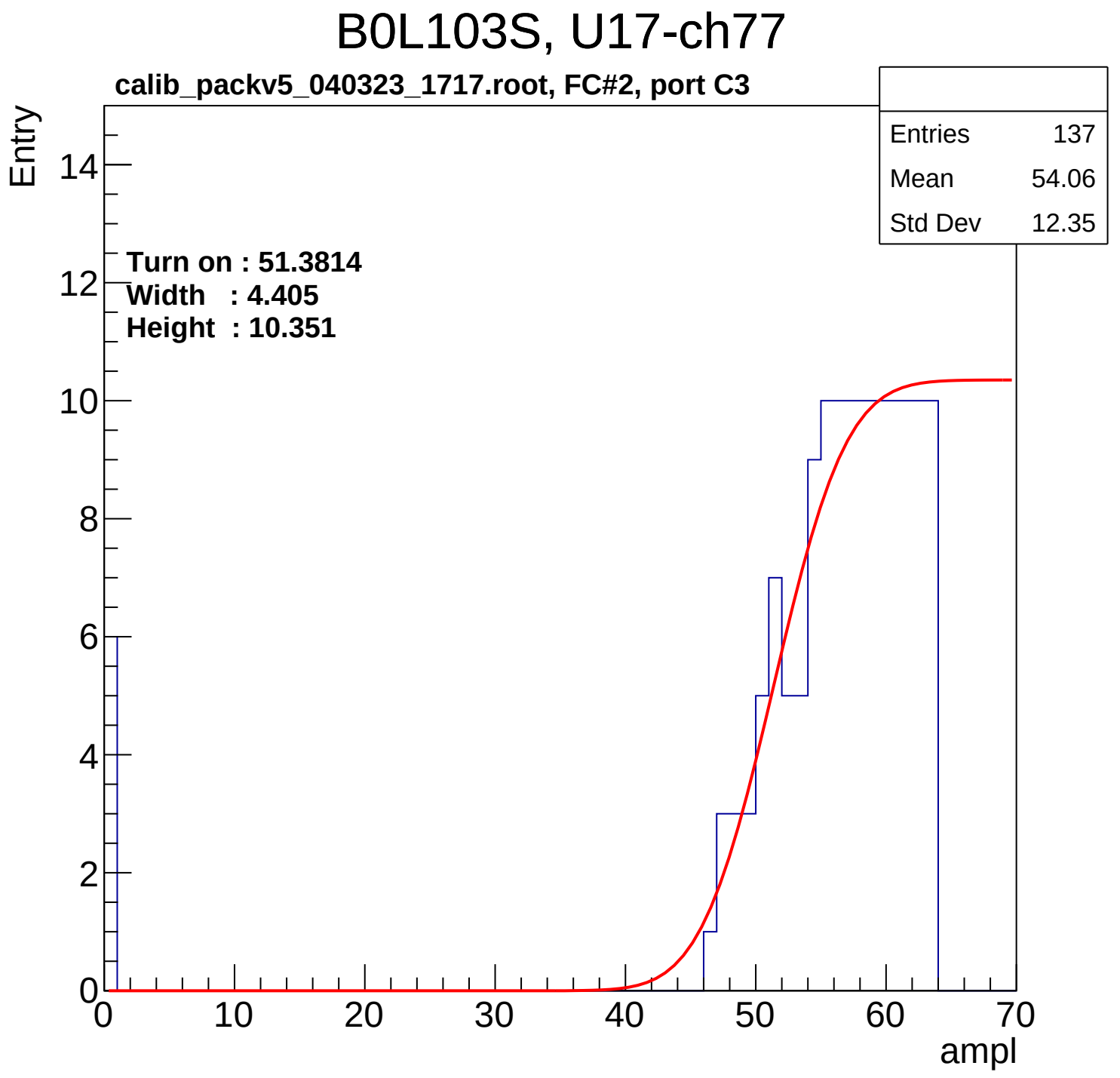
B0L103S, U17-ch77
calib_packv5_040323_1717.root, FC#2, port C3
Entries 137
Mean 54.06
Std Dev 12.35
Turn on : 51.3814
Width : 4.405
Height : 10.351
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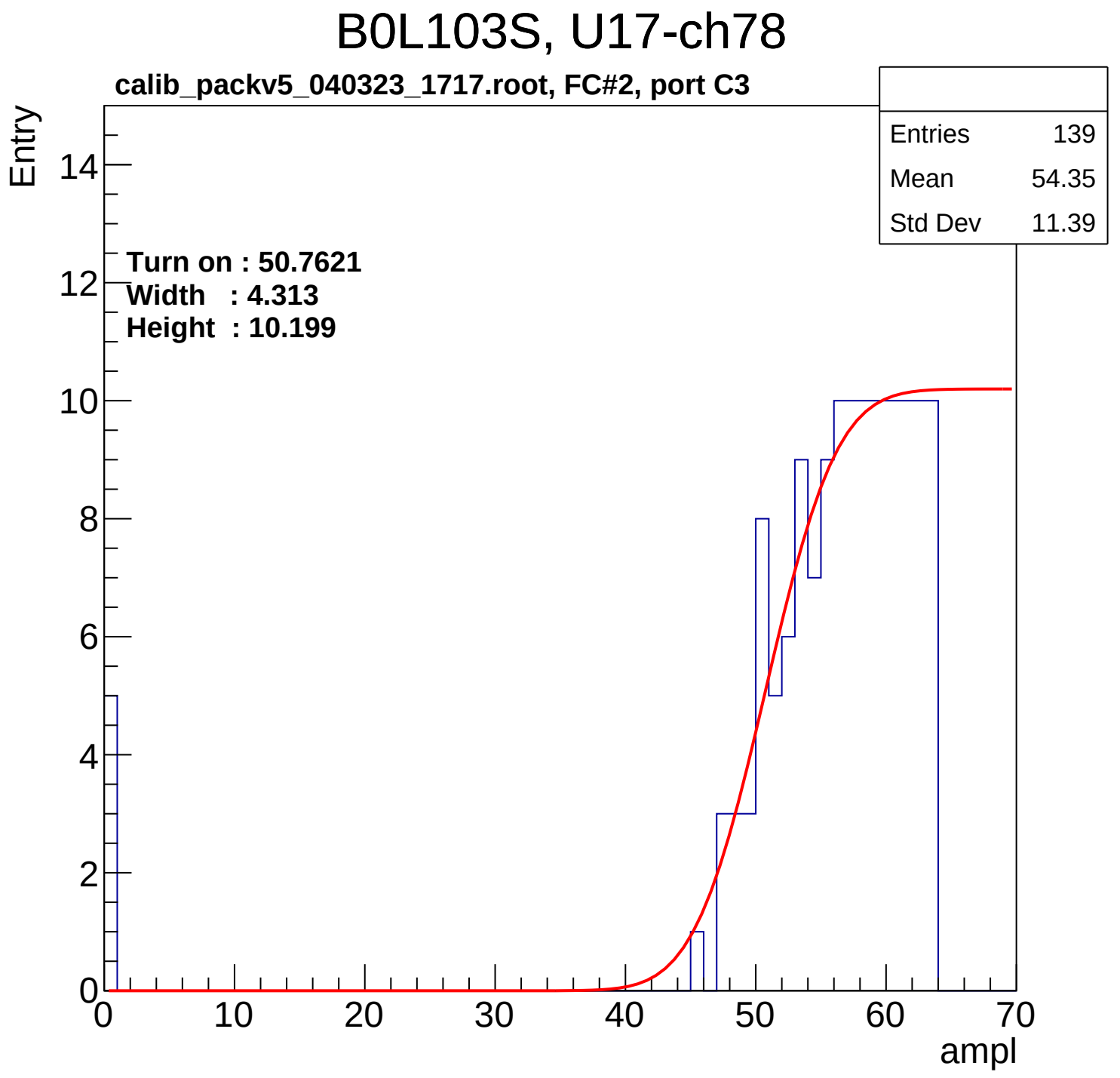
B0L103S, U17-ch78
calib_packv5_040323_1717.root, FC#2, port C3
Entries 139
Mean 54.35
Std Dev 11.39
Turn on : 50.7621
Width : 4.313
Height : 10.199
Entry
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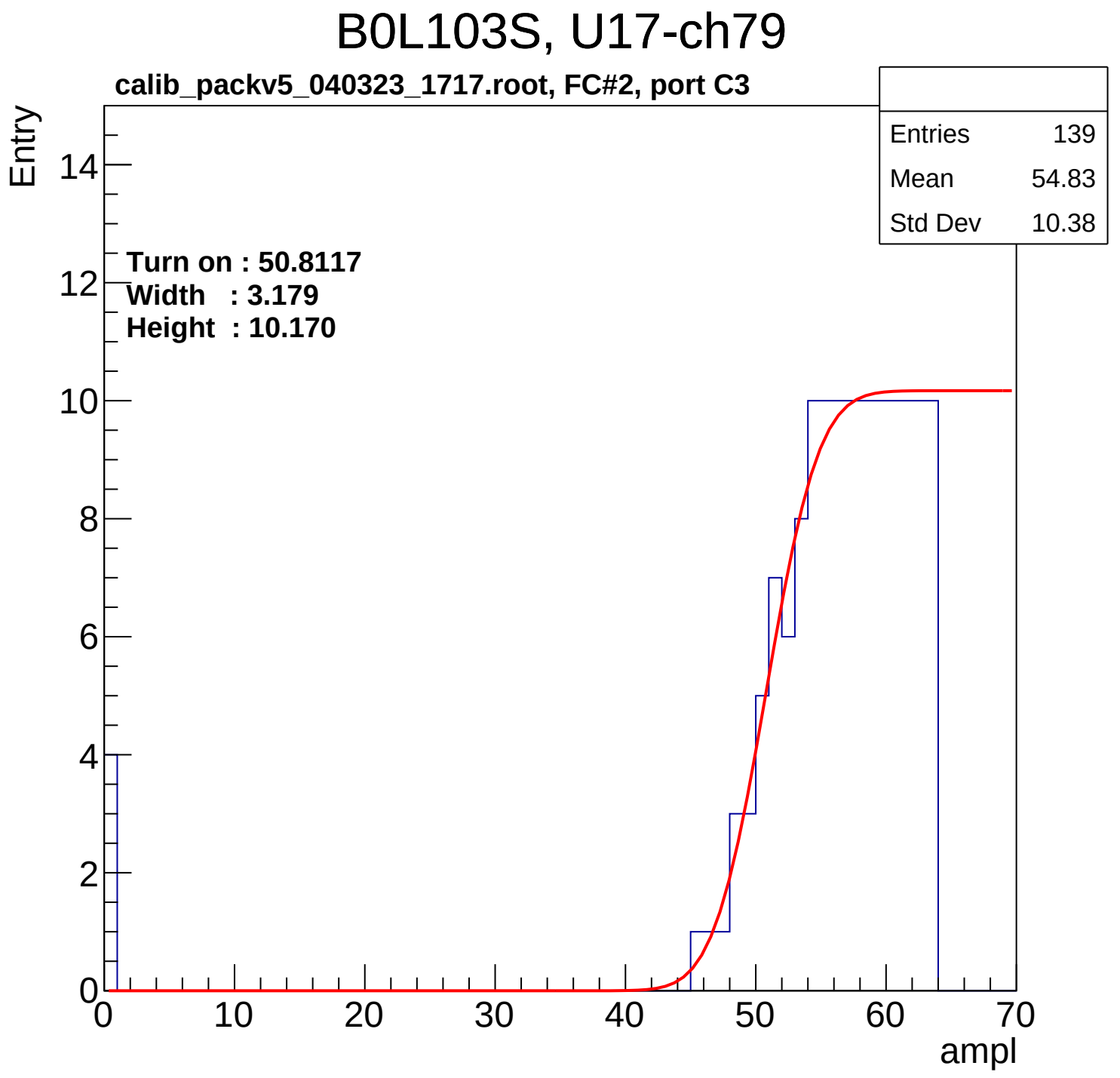
B0L103S, U17-ch79
calib_packv5_040323_1717.root, FC#2, port C3
Entries 139
Mean 54.83
Std Dev 10.38
Turn on : 50.8117
Width : 3.179
Height : 10.170
Entry
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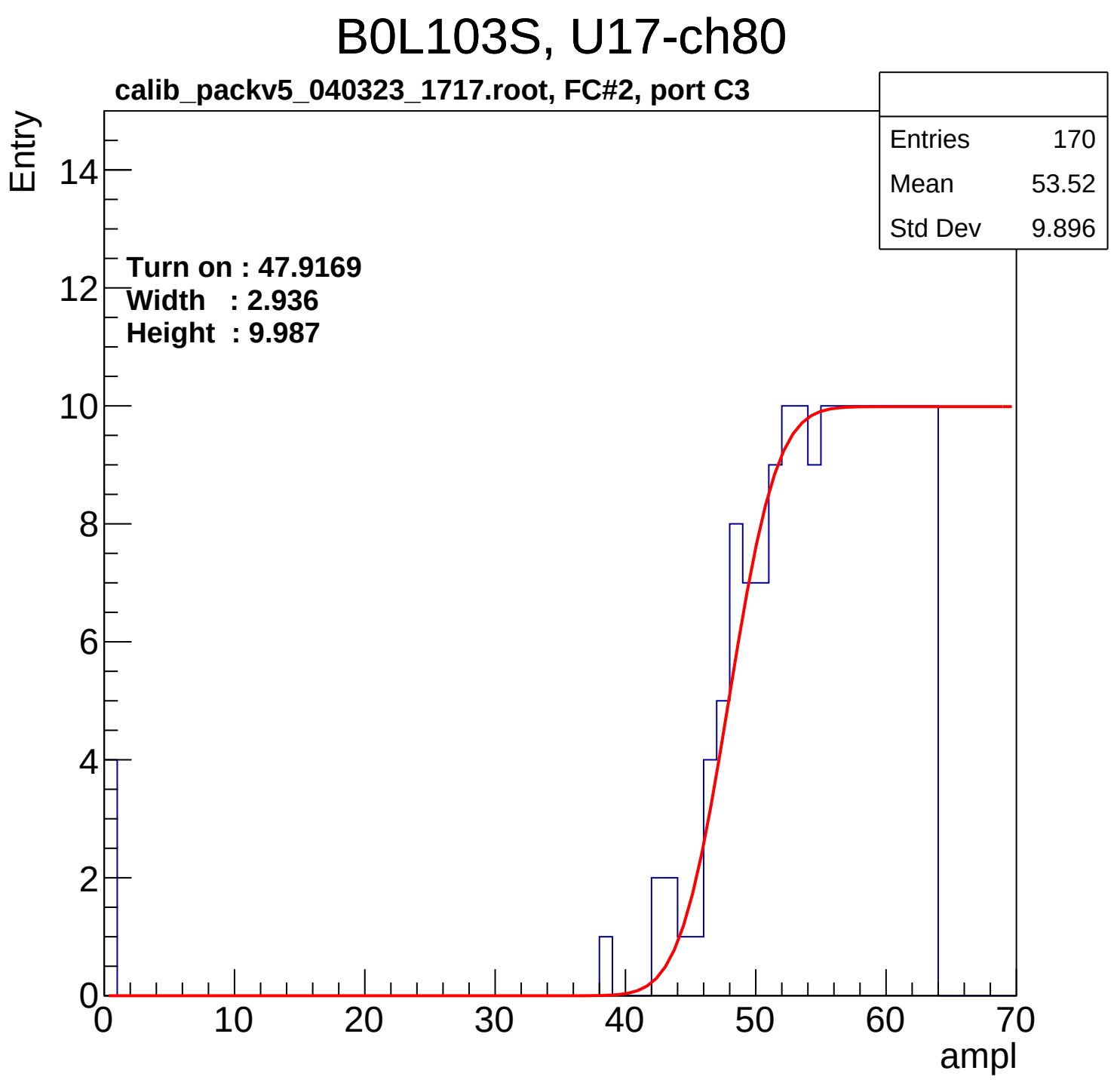
B0L103S, U17-ch80
calib_packv5_040323_1717.root, FC#2, port C3
Entries 170
Mean 53.52
Std Dev 9.896
Turn on : 47.9169
Width : 2.936
Height : 9.987
Entry
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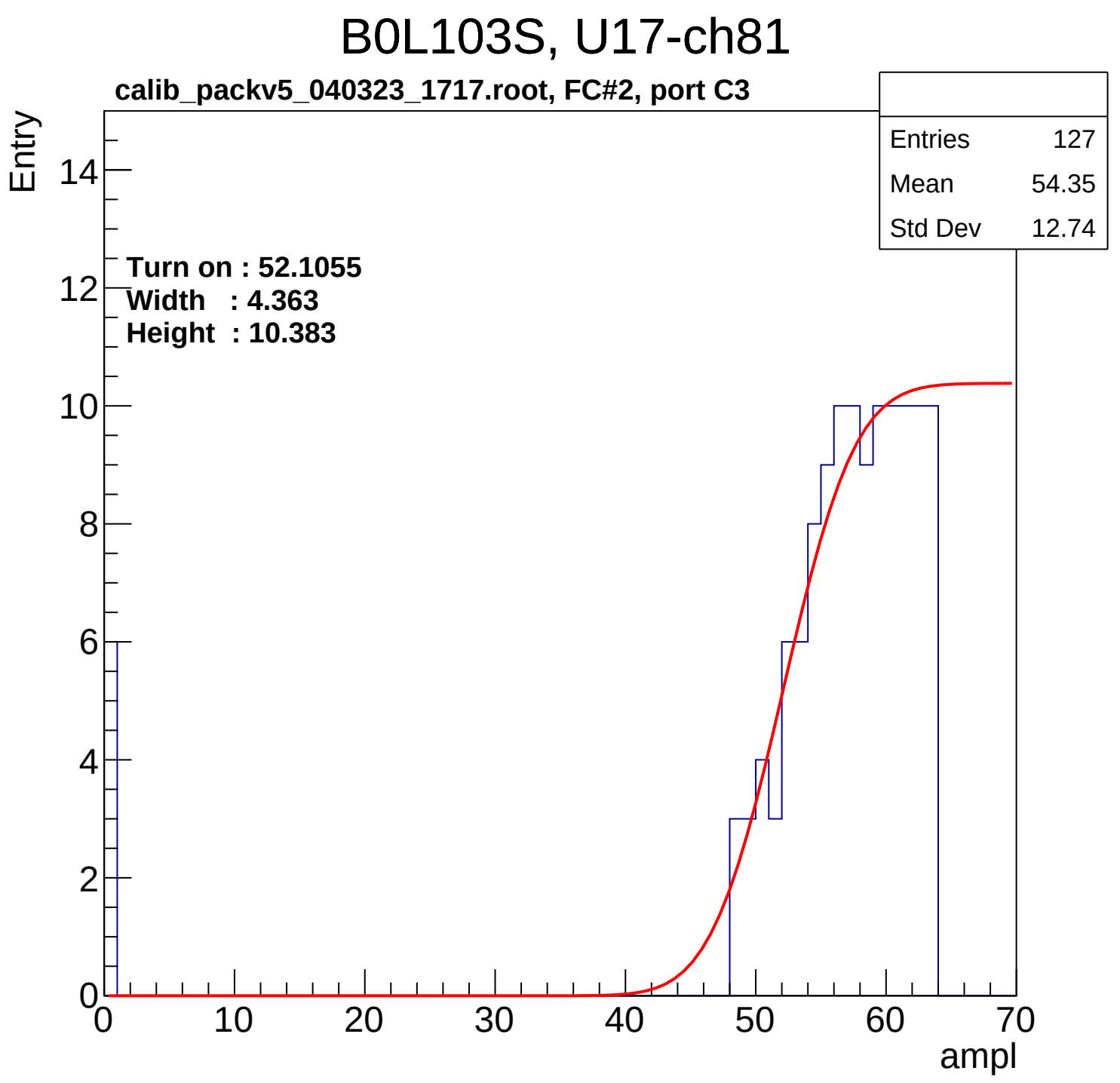
B0L103S, U17-ch81
calib_packv5_040323_1717.root, FC#2, port C3
Entries 127
Mean 54.35
Std Dev 12.74
Turn on : 52.1055
Width : 4.363
Height : 10.383
Entry
ampl
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6
8
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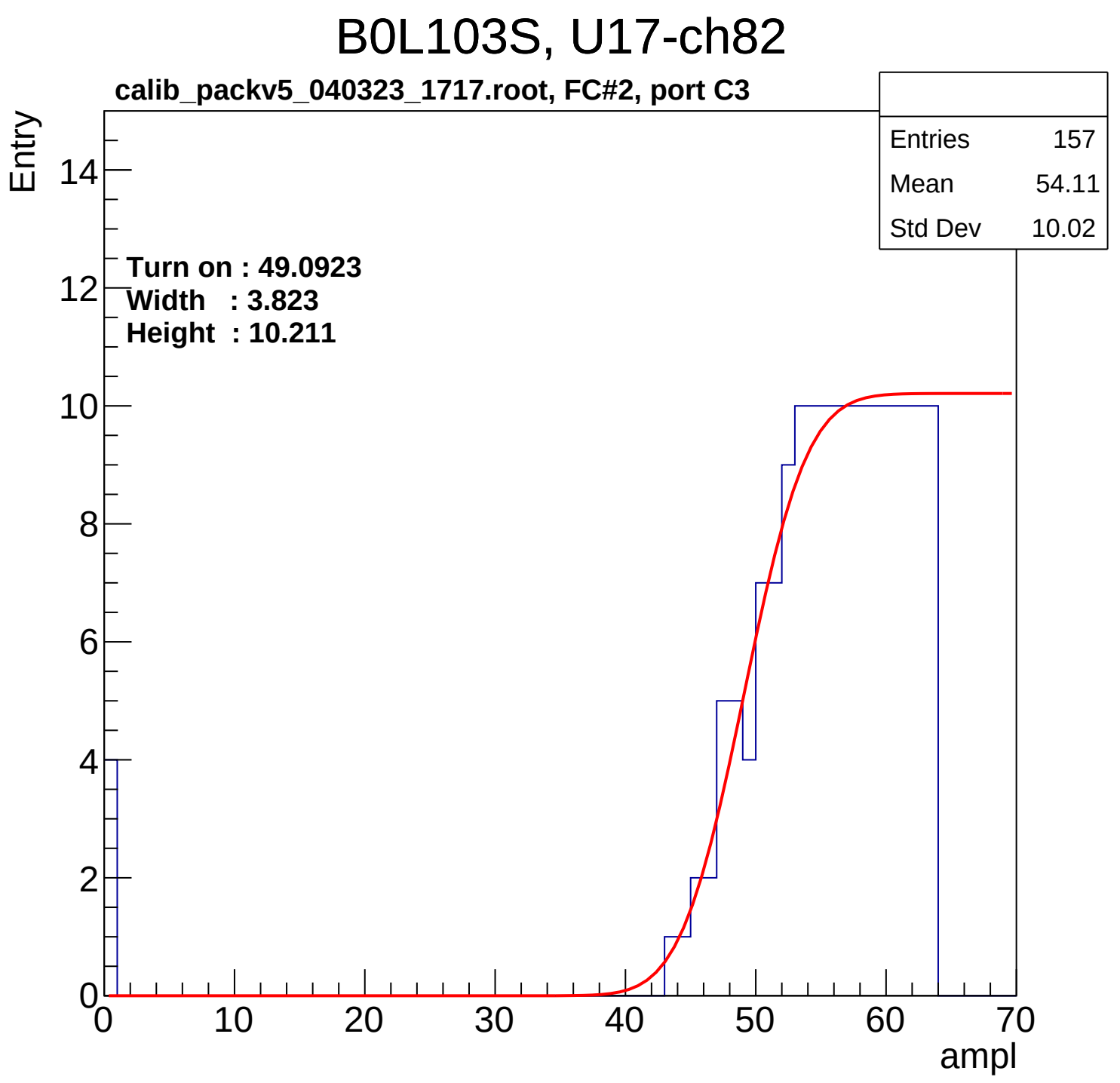
B0L103S, U17-ch82
calib_packv5_040323_1717.root, FC#2, port C3
Entries 157
Mean 54.11
Std Dev 10.02
Turn on : 49.0923
Width : 3.823
Height : 10.211
Entry
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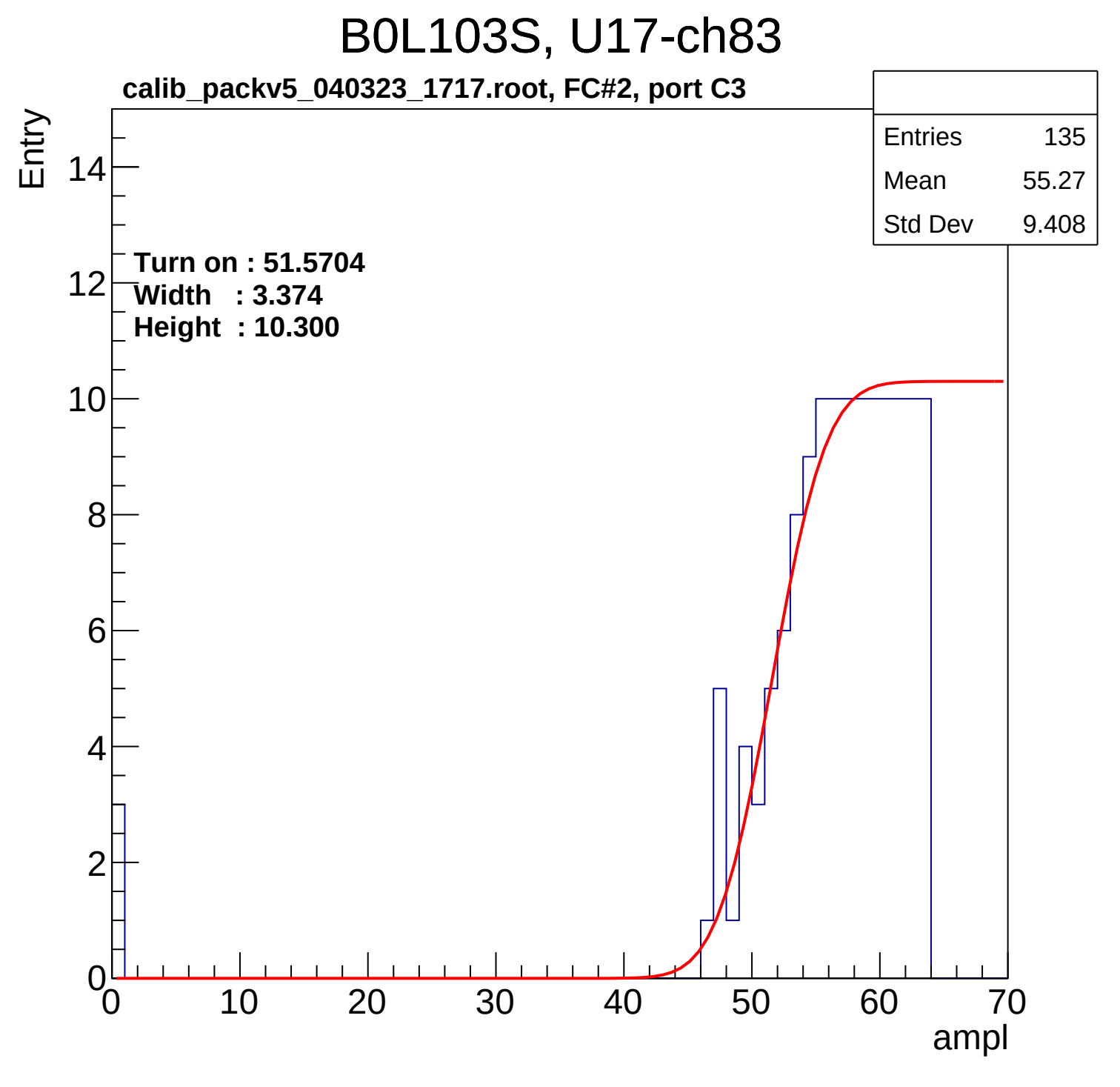
B0L103S, U17-ch83
calib_packv5_040323_1717.root, FC#2, port C3
Entries 135
Mean 55.27
Std Dev 9.408
Turn on : 51.5704
Width : 3.374
Height : 10.300
Entry
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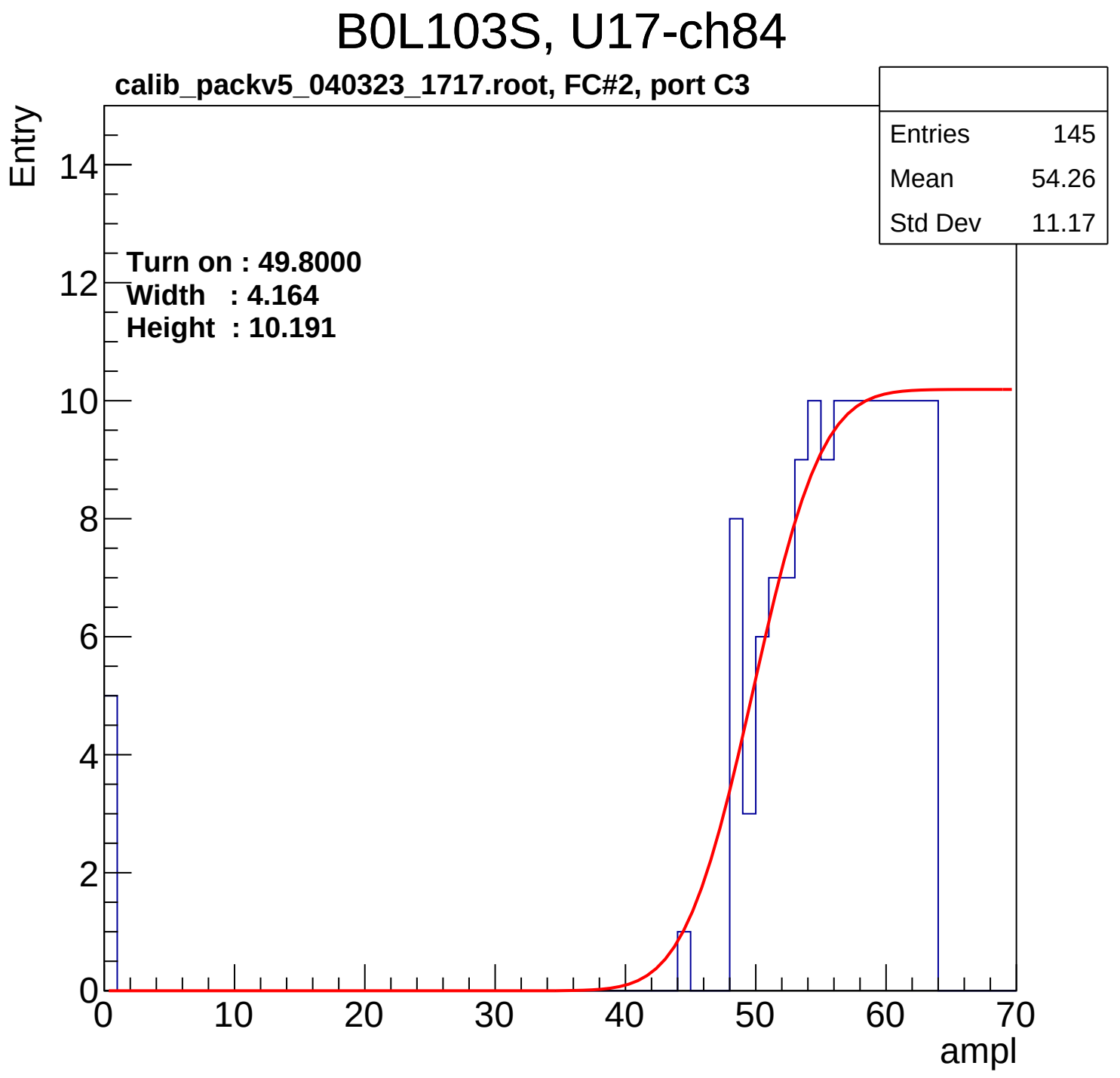
B0L103S, U17-ch84
calib_packv5_040323_1717.root, FC#2, port C3
Entries 145
Mean 54.26
Std Dev 11.17
Turn on : 49.8000
Width : 4.164
Height : 10.191
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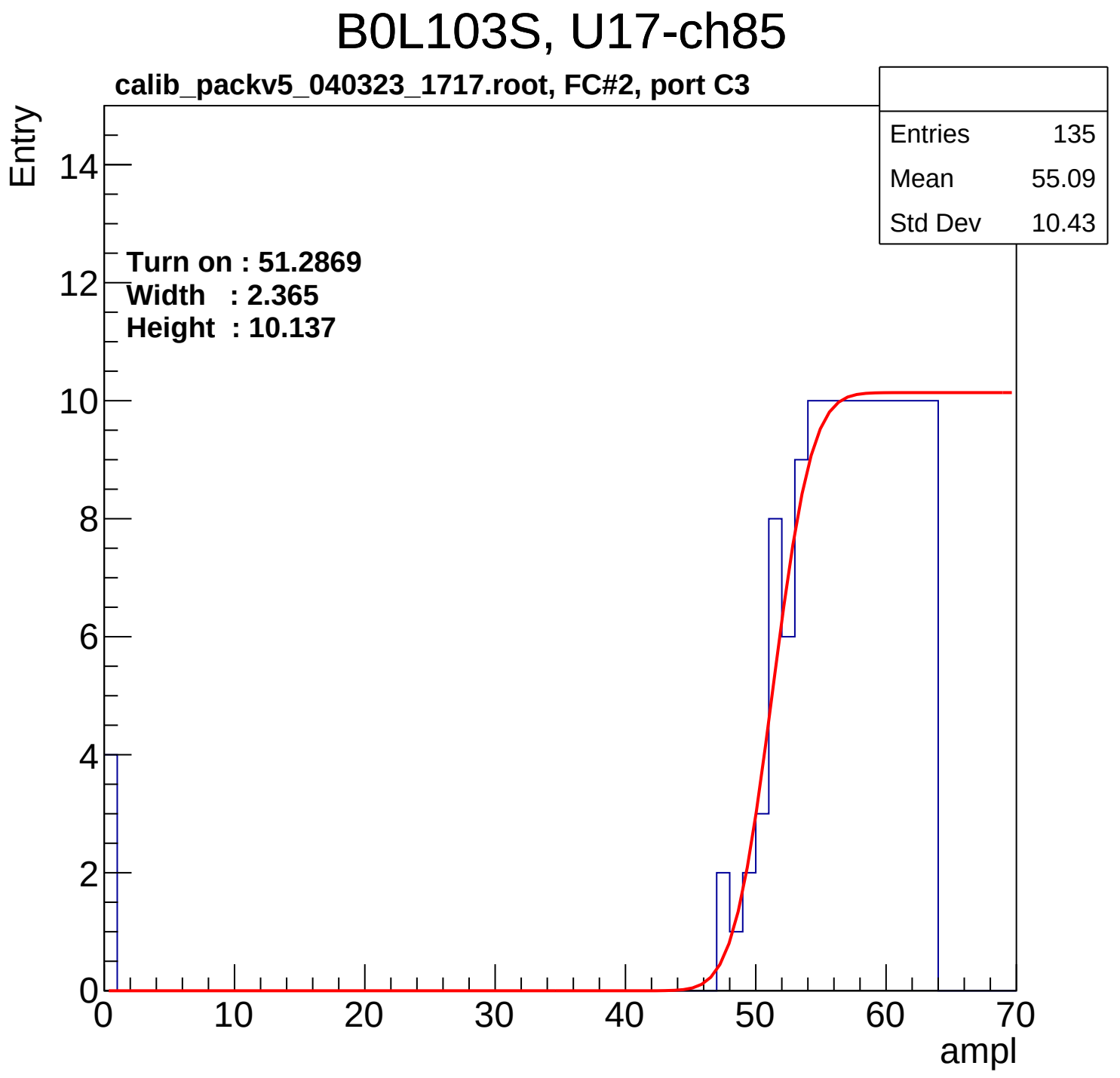
B0L103S, U17-ch85
calib_packv5_040323_1717.root, FC#2, port C3
Entries 135
Mean 55.09
Std Dev 10.43
Turn on : 51.2869
Width : 2.365
Height : 10.137
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ampl
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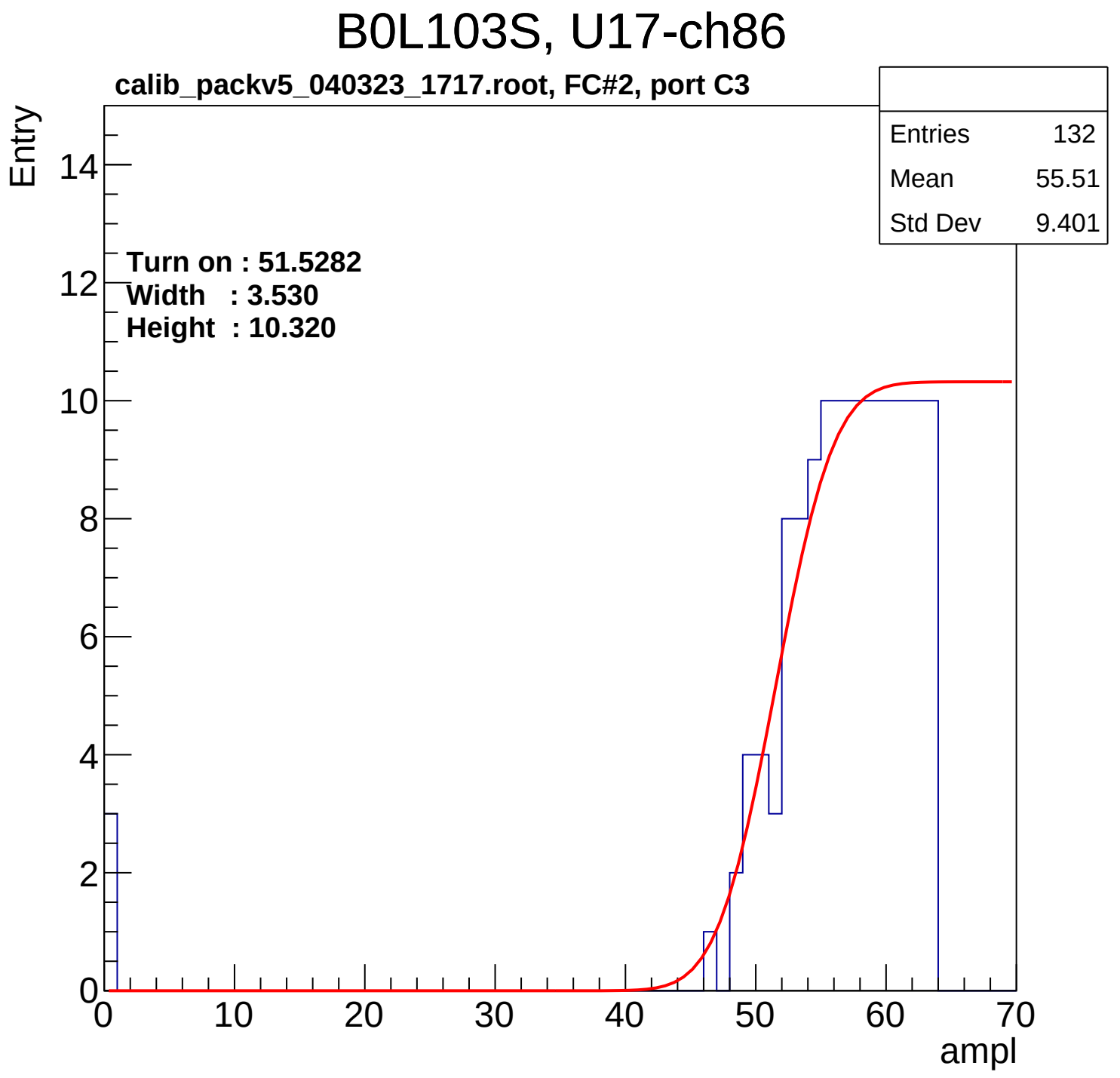
B0L103S, U17-ch86
calib_packv5_040323_1717.root, FC#2, port C3
Entries 132
Mean 55.51
Std Dev 9.401
Turn on : 51.5282
Width : 3.530
Height : 10.320
Entry
ampl
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2
4
6
8
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12
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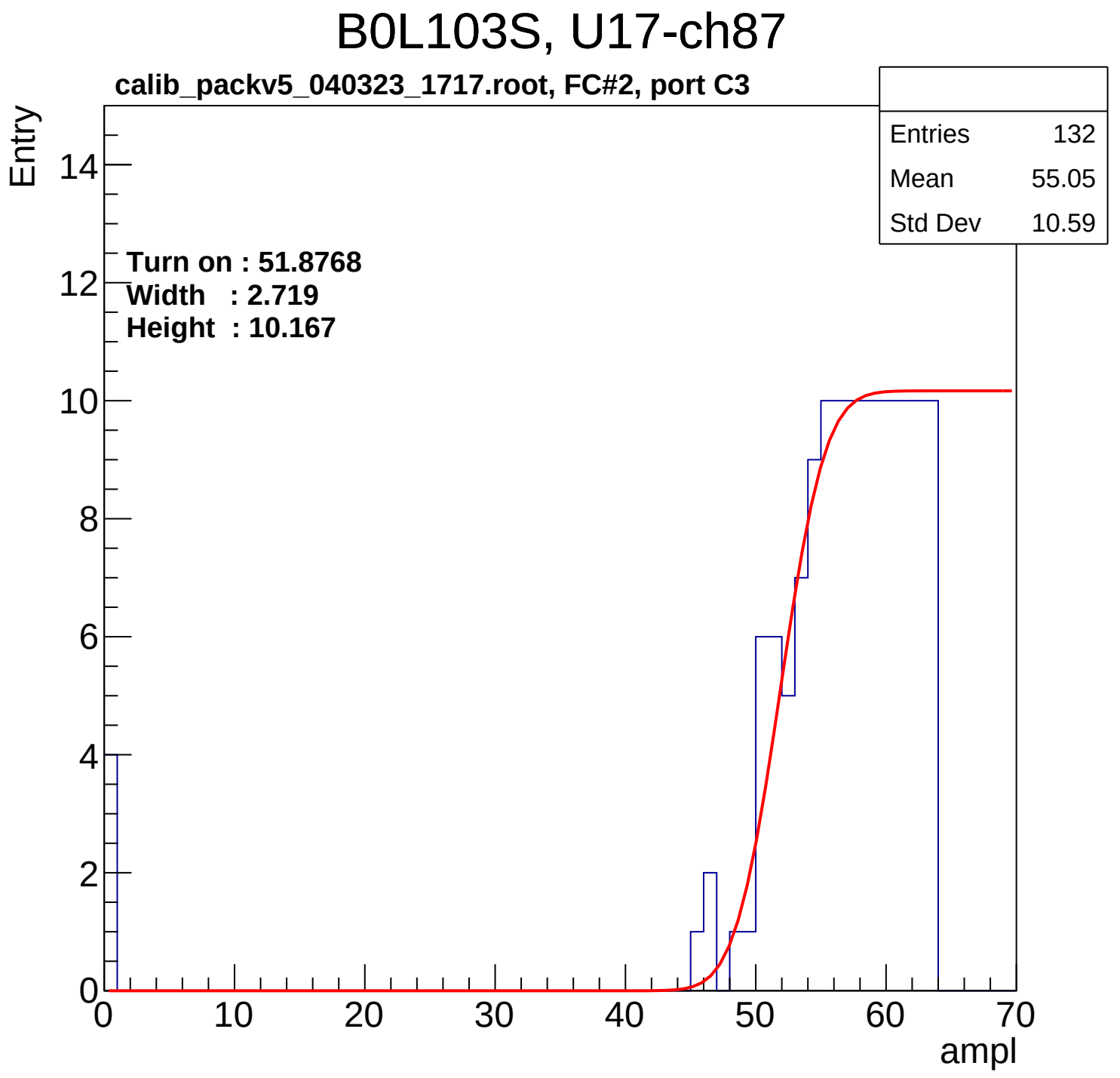
B0L103S, U17-ch87
calib_packv5_040323_1717.root, FC#2, port C3
Entries 132
Mean 55.05
Std Dev 10.59
Turn on : 51.8768
Width : 2.719
Height : 10.167
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ampl
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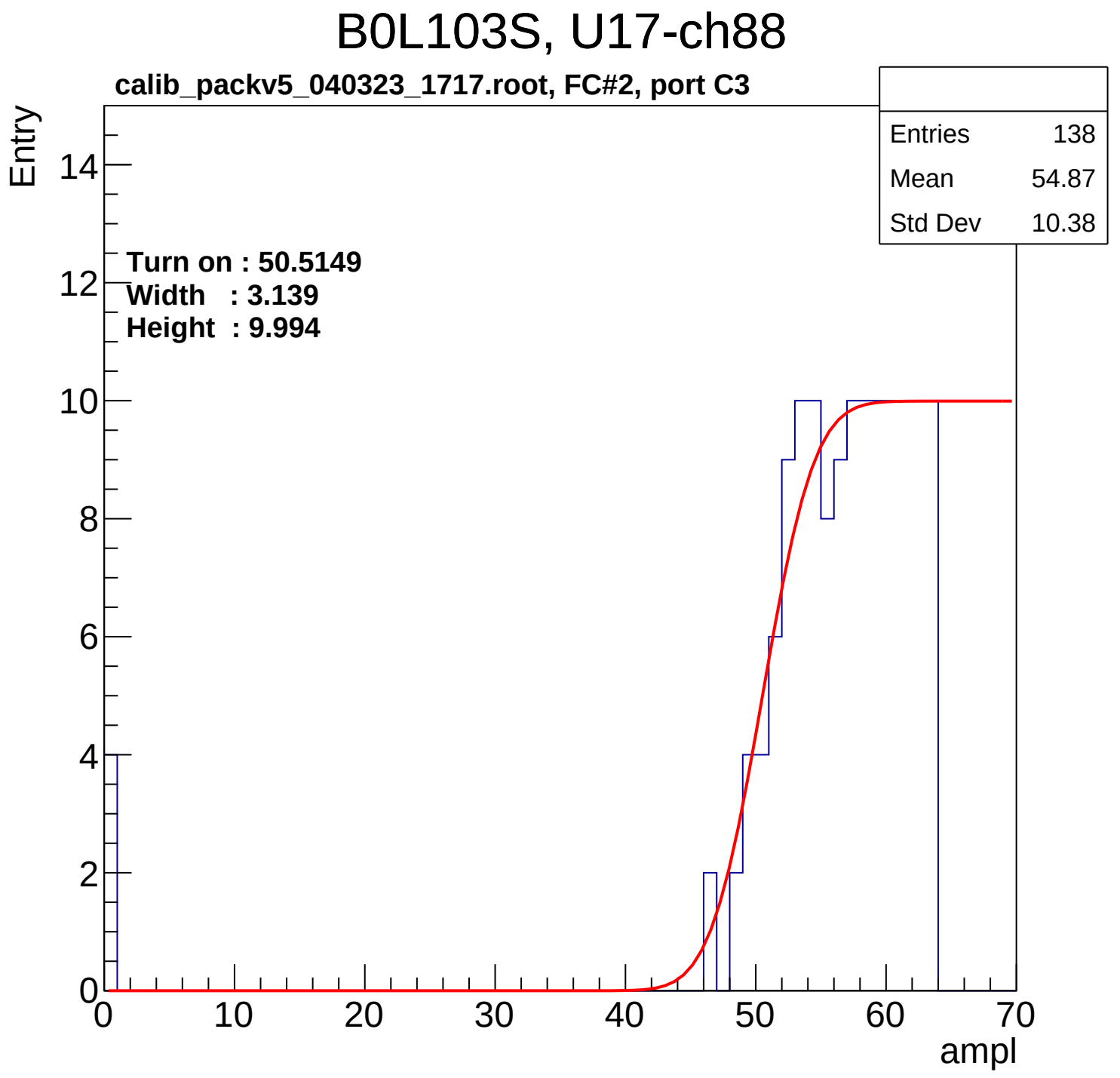
B0L103S, U17-ch88
calib_packv5_040323_1717.root, FC#2, port C3
Entries 138
Mean 54.87
Std Dev 10.38
Turn on : 50.5149
Width : 3.139
Height : 9.994
Entry
ampl
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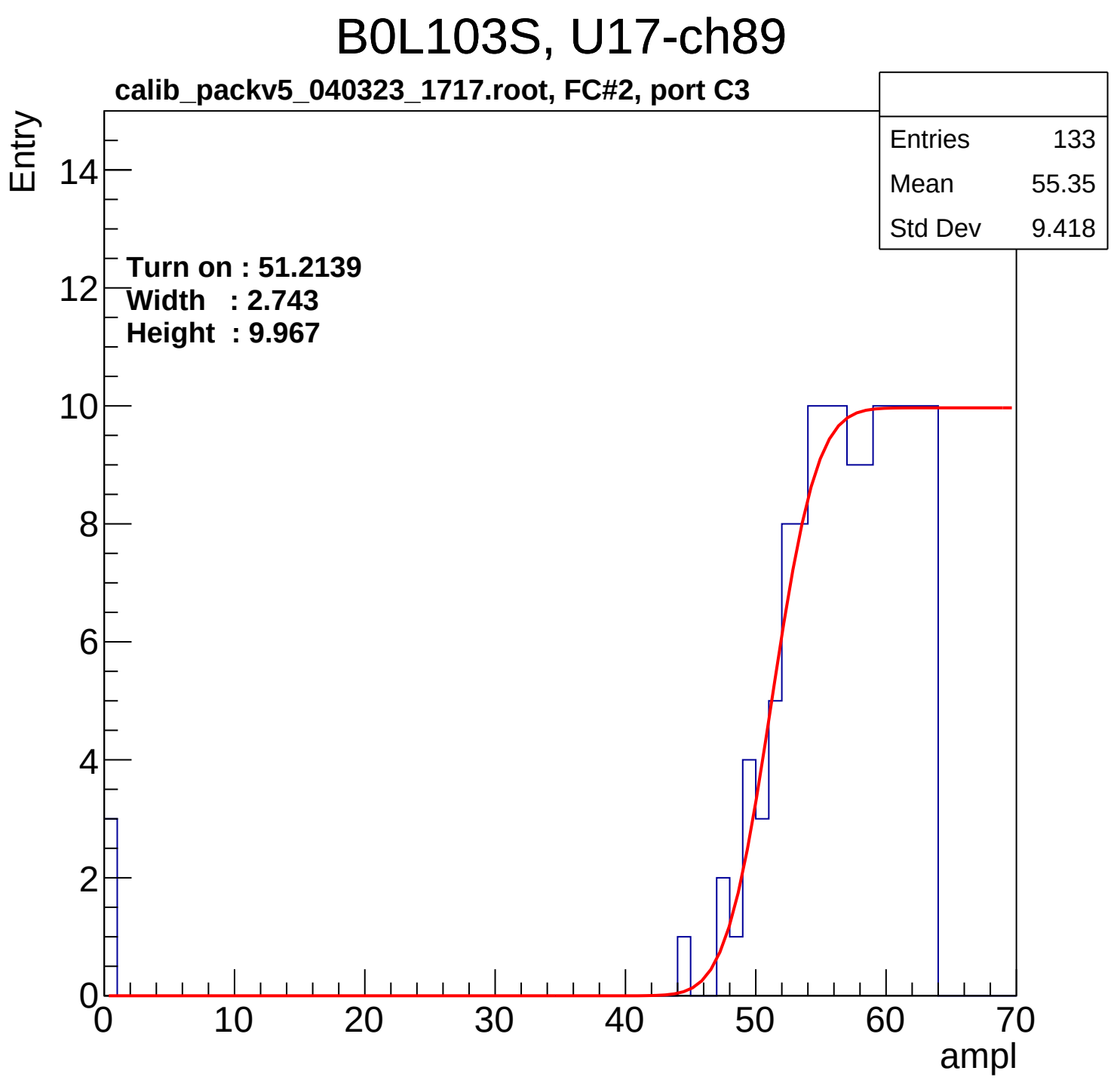
B0L103S, U17-ch89
calib_packv5_040323_1717.root, FC#2, port C3
Entries 133
Mean 55.35
Std Dev 9.418
Turn on : 51.2139
Width : 2.743
Height : 9.967
Entry
ampl
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2
4
6
8
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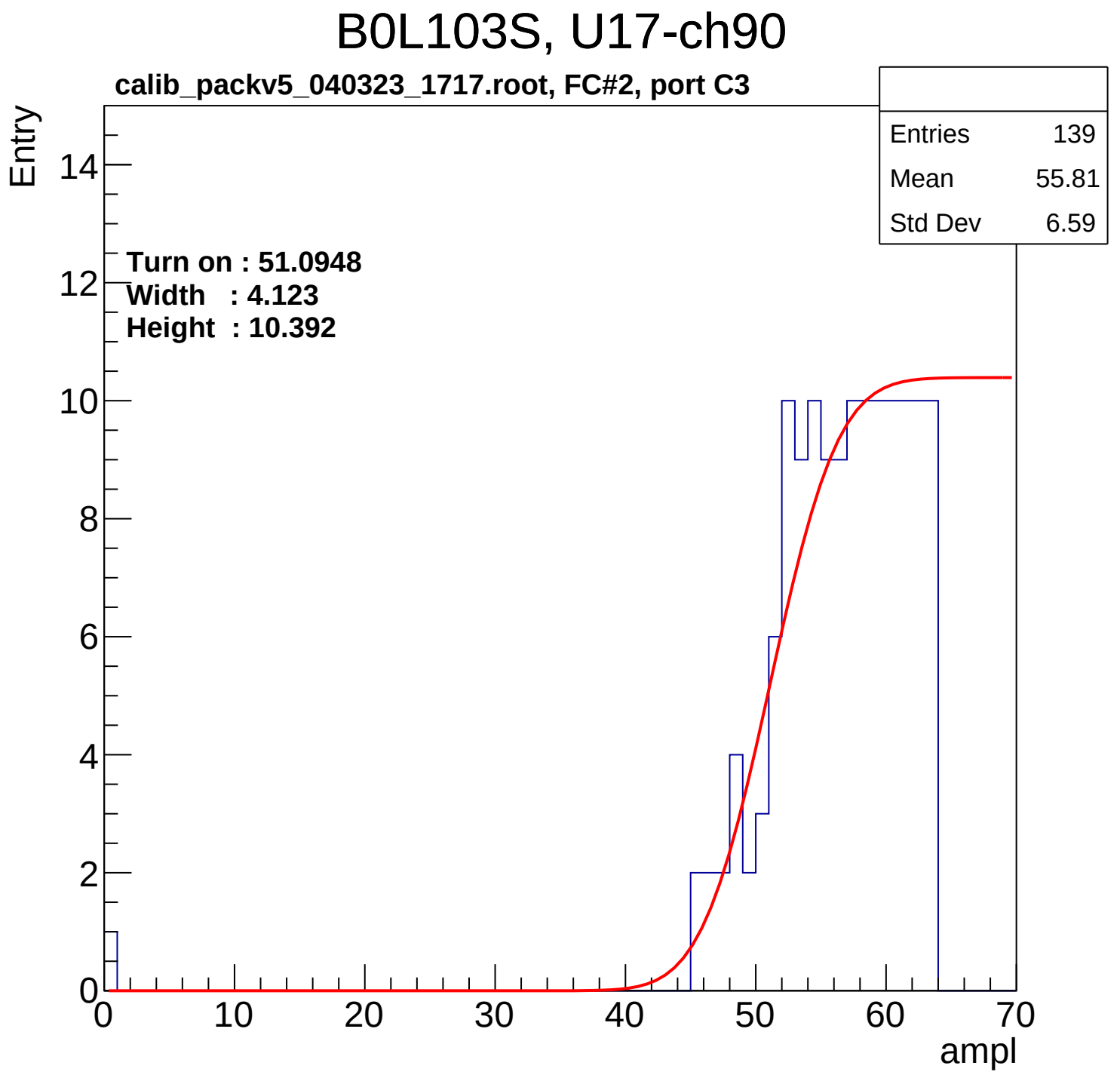
B0L103S, U17-ch90
calib_packv5_040323_1717.root, FC#2, port C3
Entries 139
Mean 55.81
Std Dev 6.59
Turn on : 51.0948
Width : 4.123
Height : 10.392
Entry
ampl
0
2
4
6
8
10
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0
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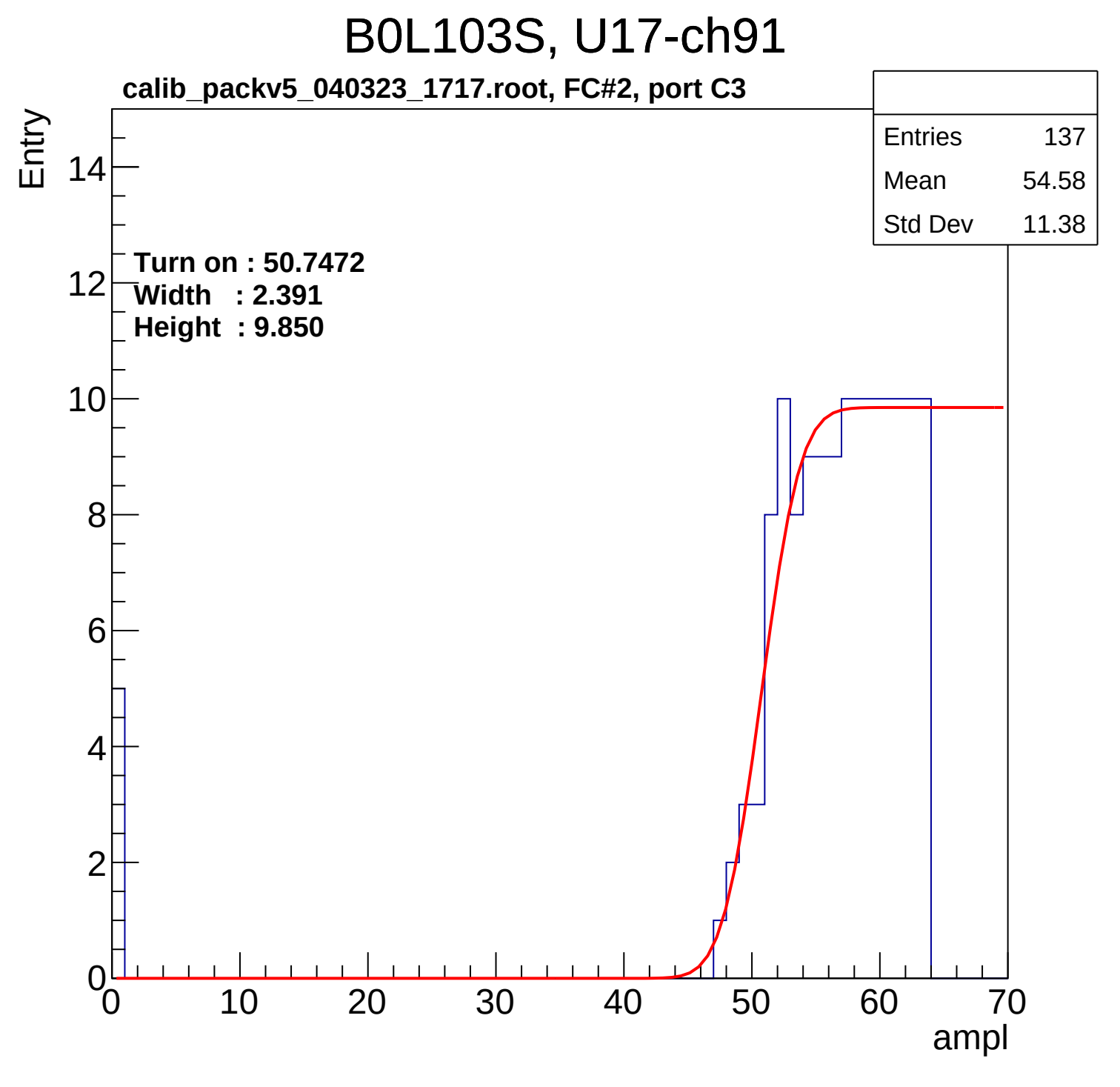
B0L103S, U17-ch91
calib_packv5_040323_1717.root, FC#2, port C3
Entries 137
Mean 54.58
Std Dev 11.38
Turn on : 50.7472
Width : 2.391
Height : 9.850
Entry
ampl
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6
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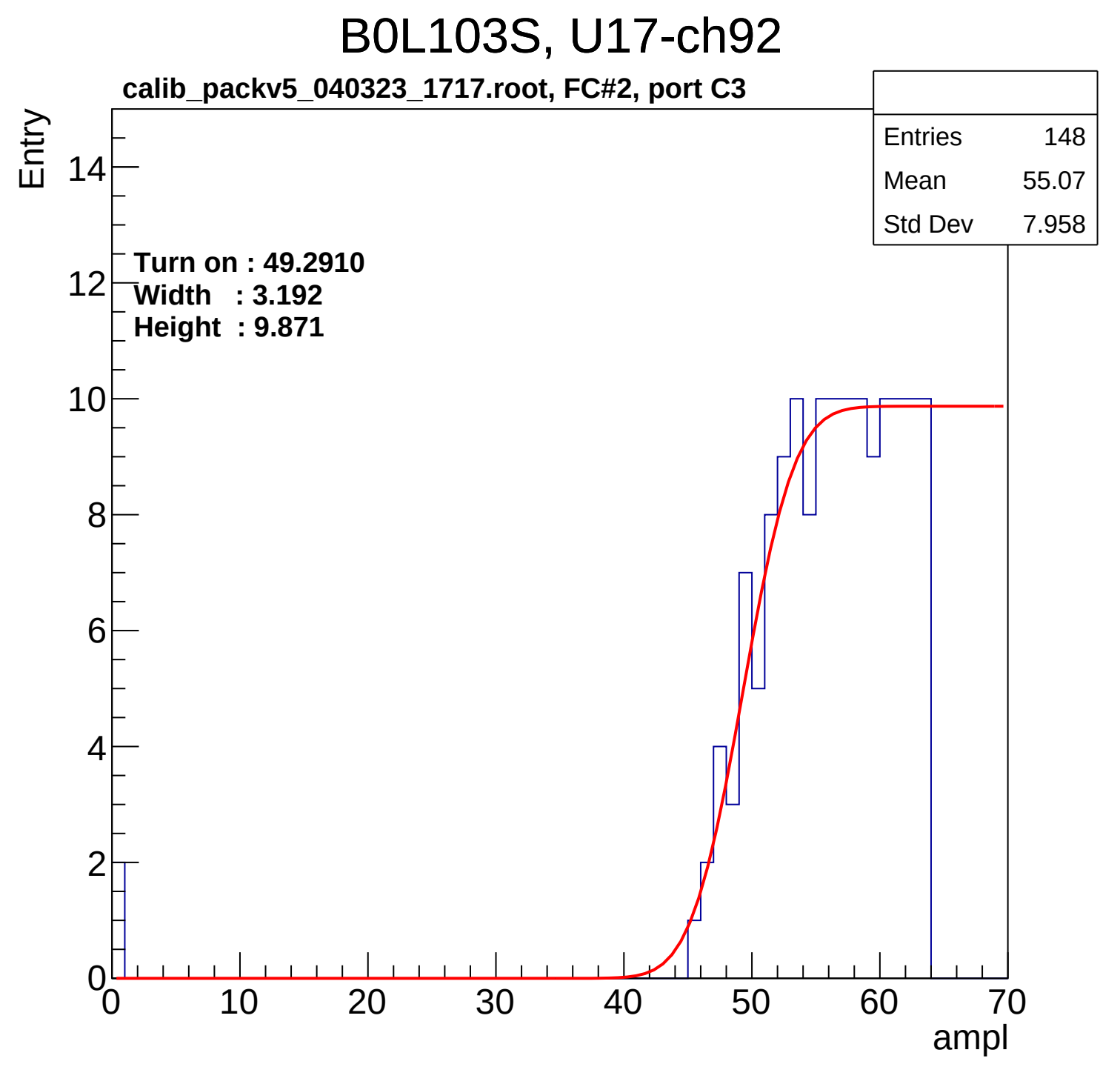
B0L103S, U17-ch92
calib_packv5_040323_1717.root, FC#2, port C3
Entries 148
Mean 55.07
Std Dev 7.958
Turn on : 49.2910
Width : 3.192
Height : 9.871
Entry
ampl
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2
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6
8
10
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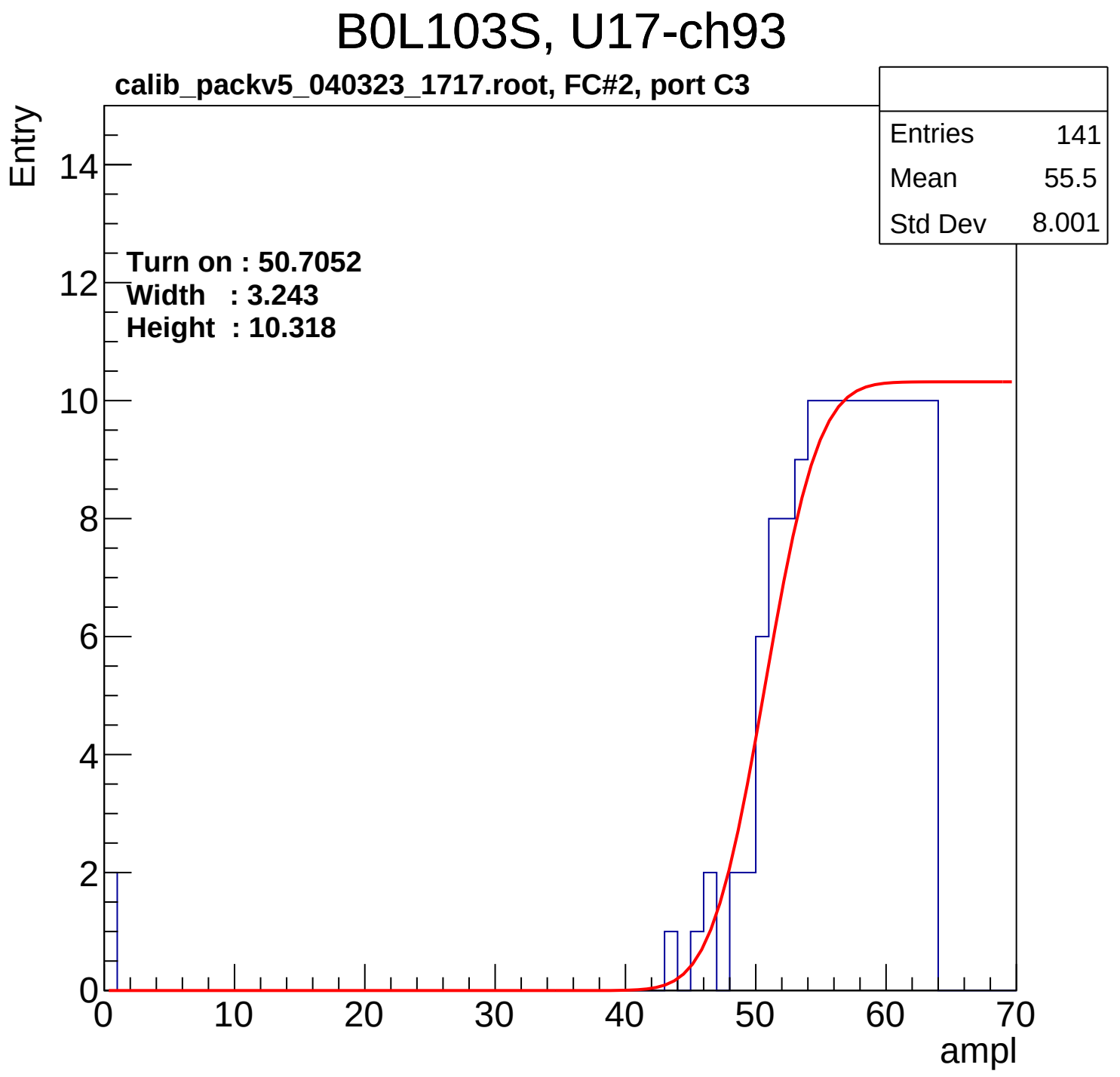
B0L103S, U17-ch93
calib_packv5_040323_1717.root, FC#2, port C3
Entries 141
Mean 55.5
Std Dev 8.001
Turn on : 50.7052
Width : 3.243
Height : 10.318
Entry
ampl
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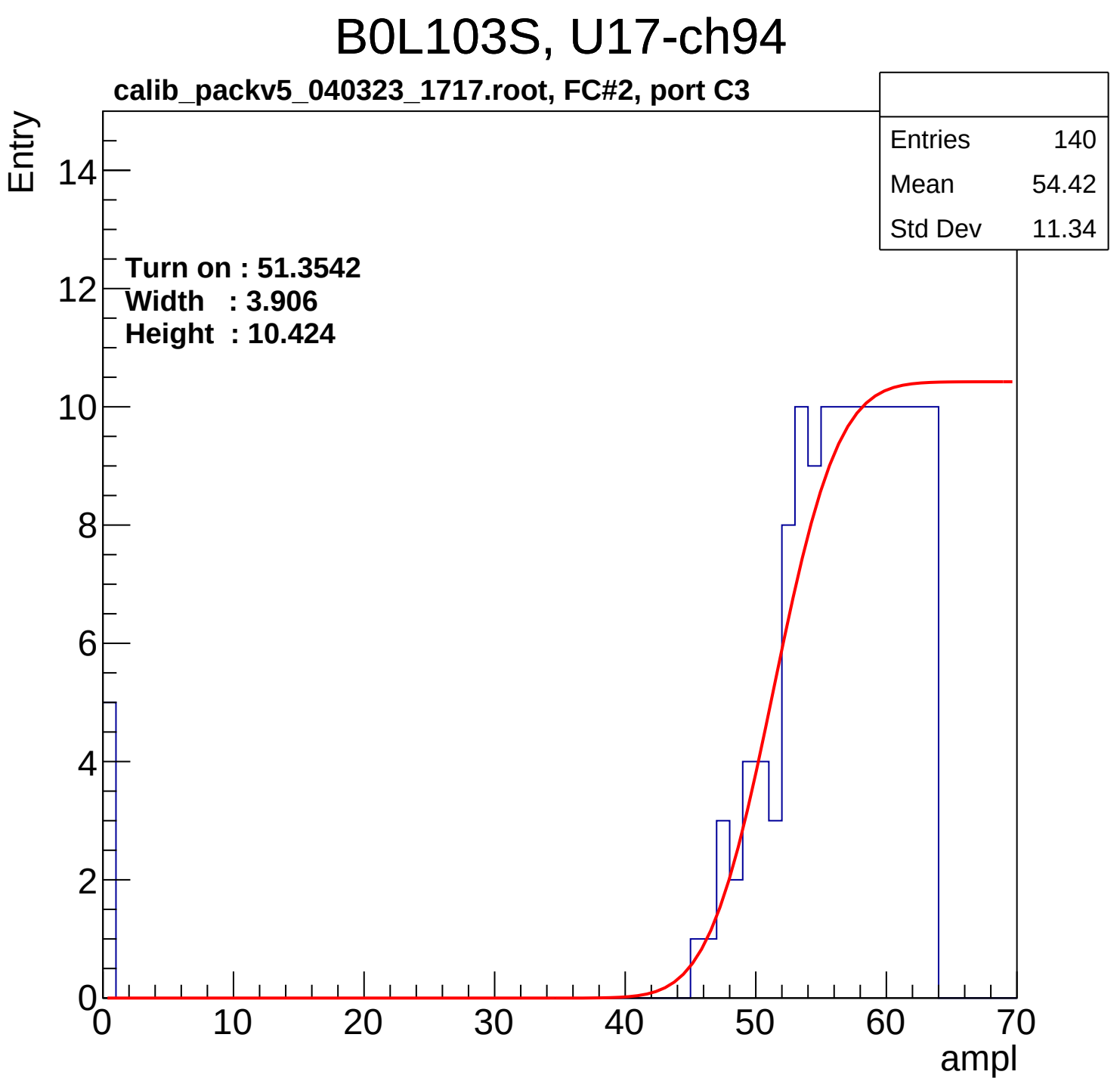
B0L103S, U17-ch94
calib_packv5_040323_1717.root, FC#2, port C3
Entries 140
Mean 54.42
Std Dev 11.34
Turn on : 51.3542
Width : 3.906
Height : 10.424
Entry
ampl
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2
4
6
8
10
12
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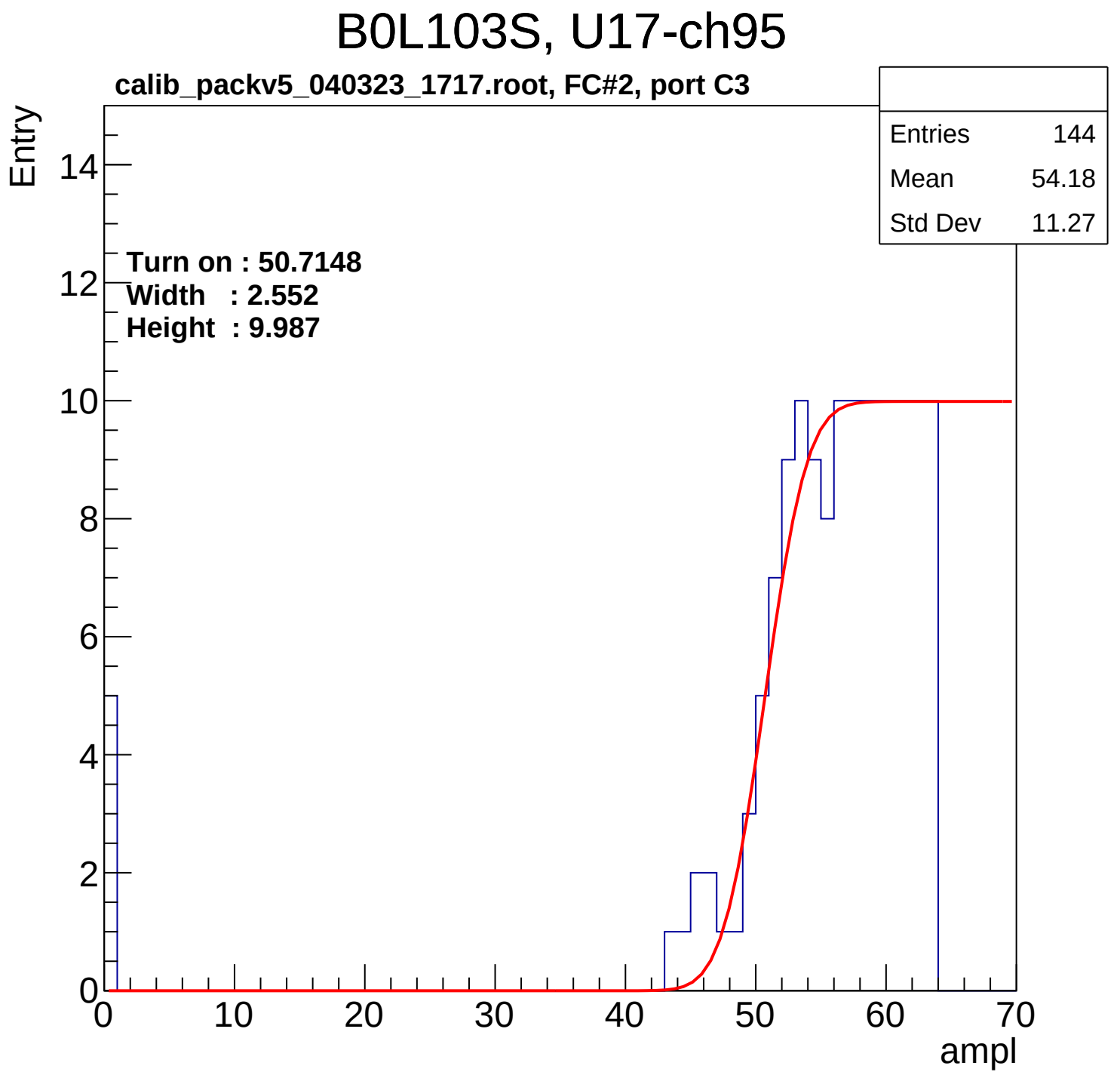
B0L103S, U17-ch95
calib_packv5_040323_1717.root, FC#2, port C3
Entries 144
Mean 54.18
Std Dev 11.27
Turn on : 50.7148
Width : 2.552
Height : 9.987
Entry
ampl
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4
6
8
10
12
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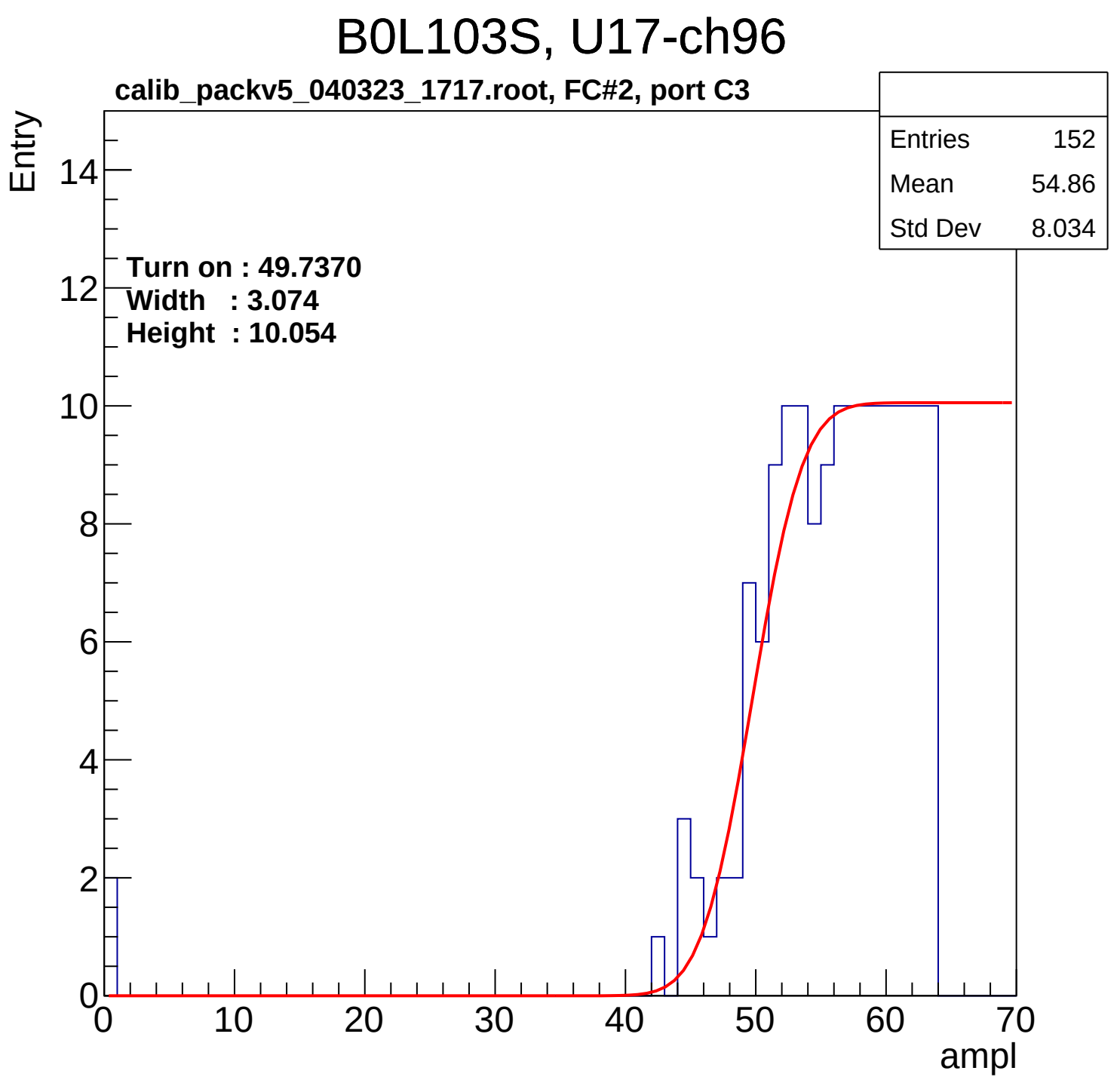
B0L103S, U17-ch96
calib_packv5_040323_1717.root, FC#2, port C3
Entries 152
Mean 54.86
Std Dev 8.034
Turn on : 49.7370
Width : 3.074
Height : 10.054
Entry
ampl
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6
8
10
12
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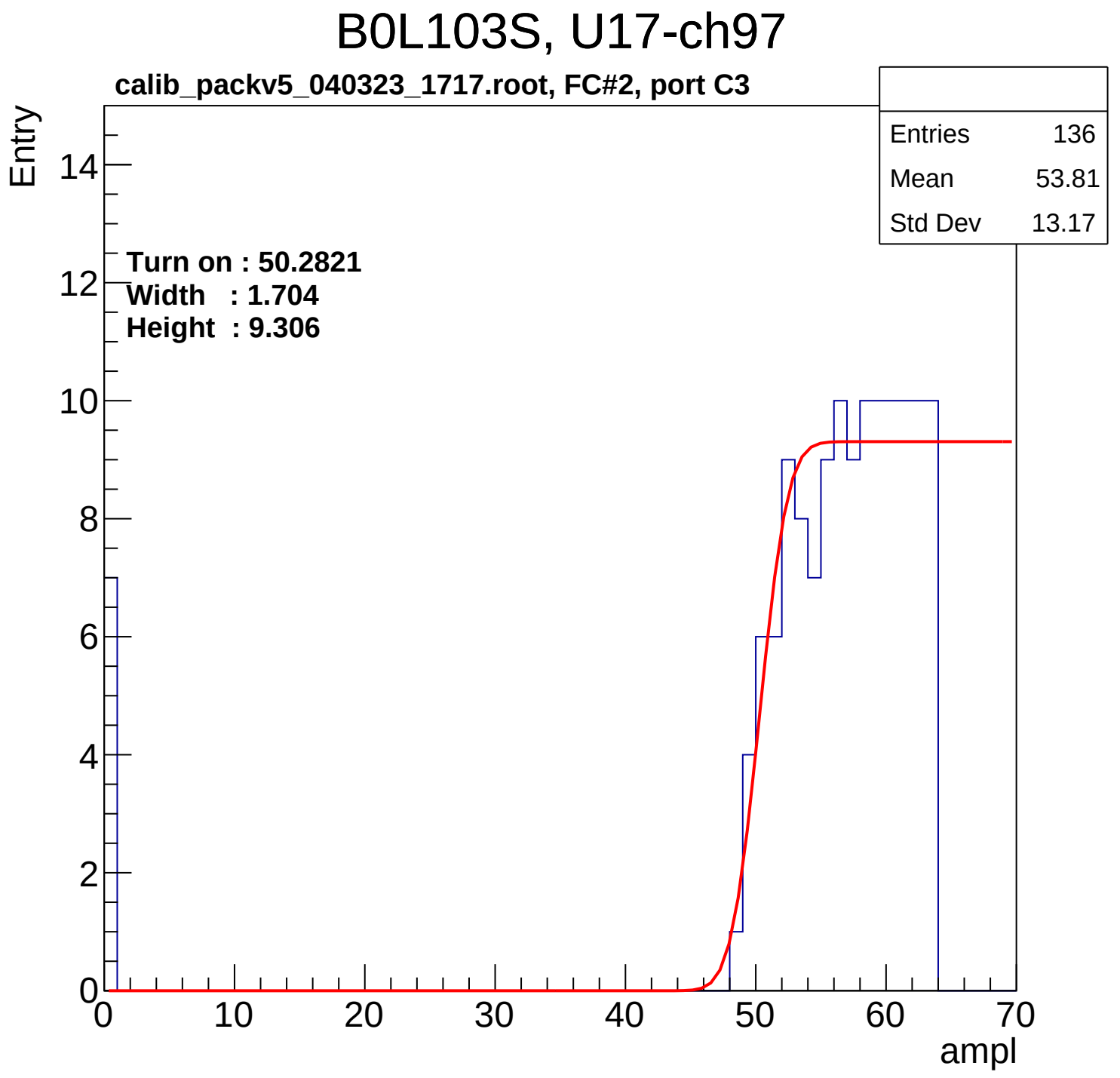
B0L103S, U17-ch97
calib_packv5_040323_1717.root, FC#2, port C3
Entries 136
Mean 53.81
Std Dev 13.17
Turn on : 50.2821
Width : 1.704
Height : 9.306
Entry
ampl
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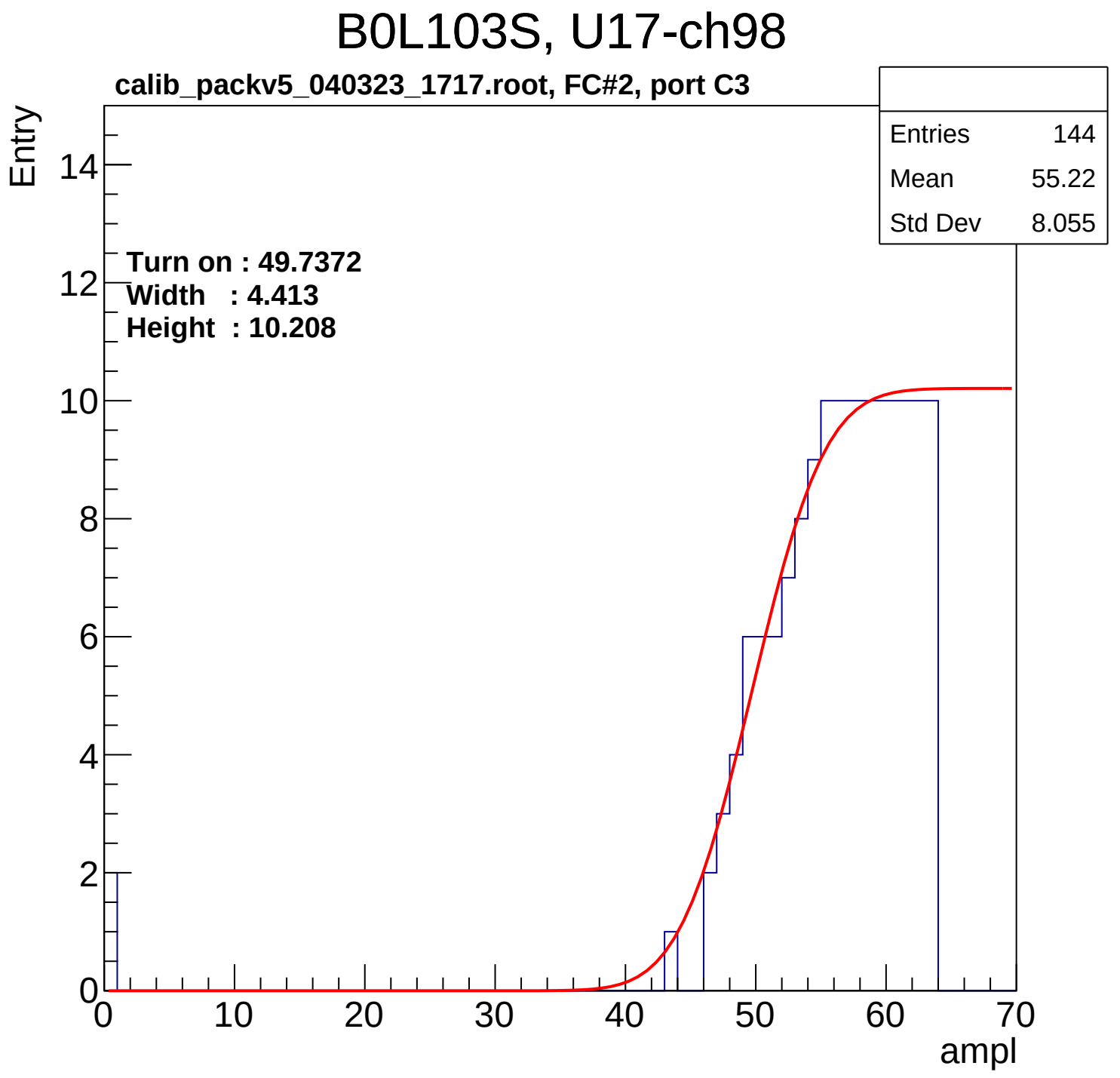
B0L103S, U17-ch98
calib_packv5_040323_1717.root, FC#2, port C3
Entries 144
Mean 55.22
Std Dev 8.055
Turn on : 49.7372
Width : 4.413
Height : 10.208
Entry
ampl
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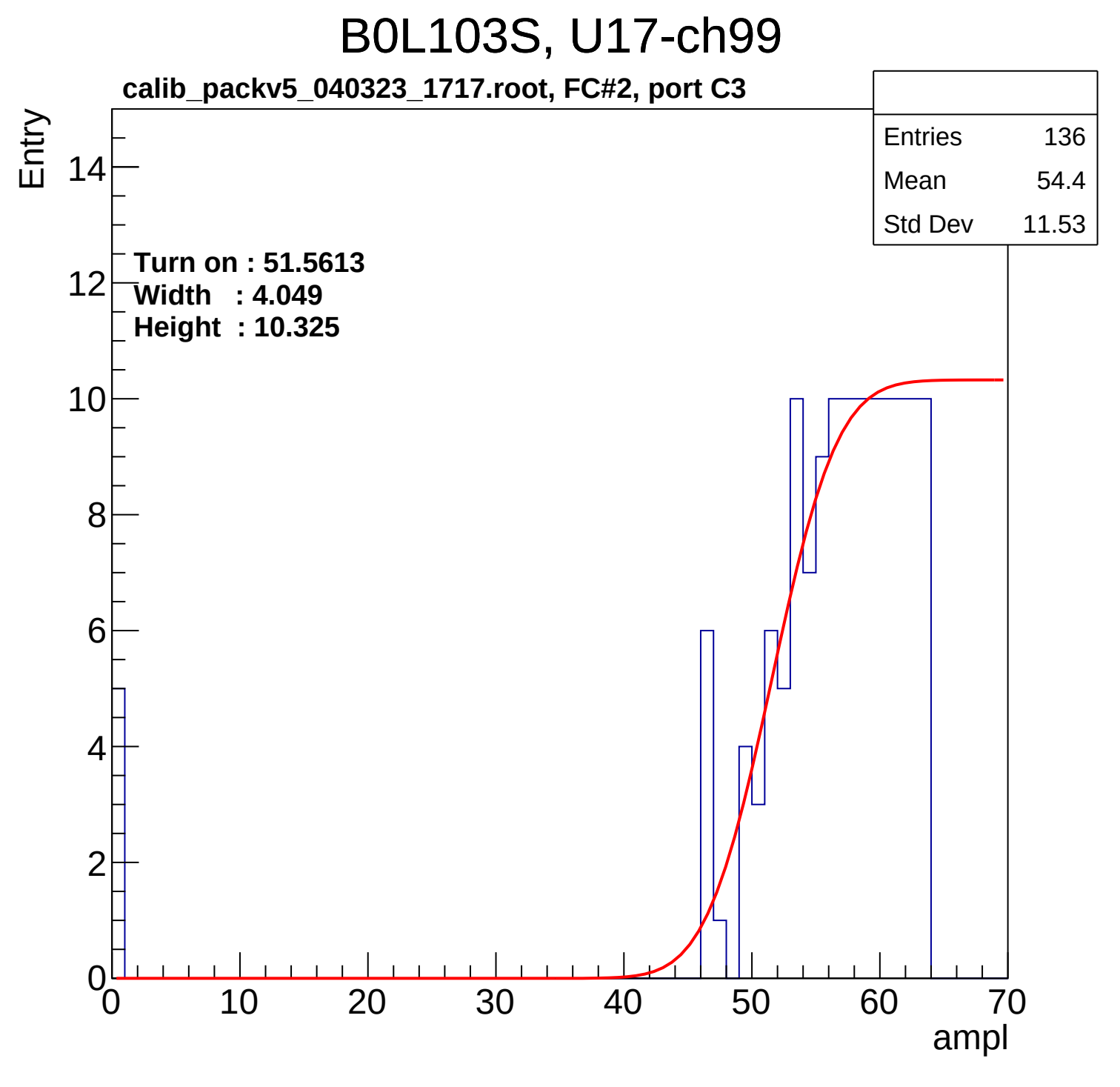
B0L103S, U17-ch99
calib_packv5_040323_1717.root, FC#2, port C3
Entries 136
Mean 54.4
Std Dev 11.53
Turn on : 51.5613
Width : 4.049
Height : 10.325
Entry
ampl
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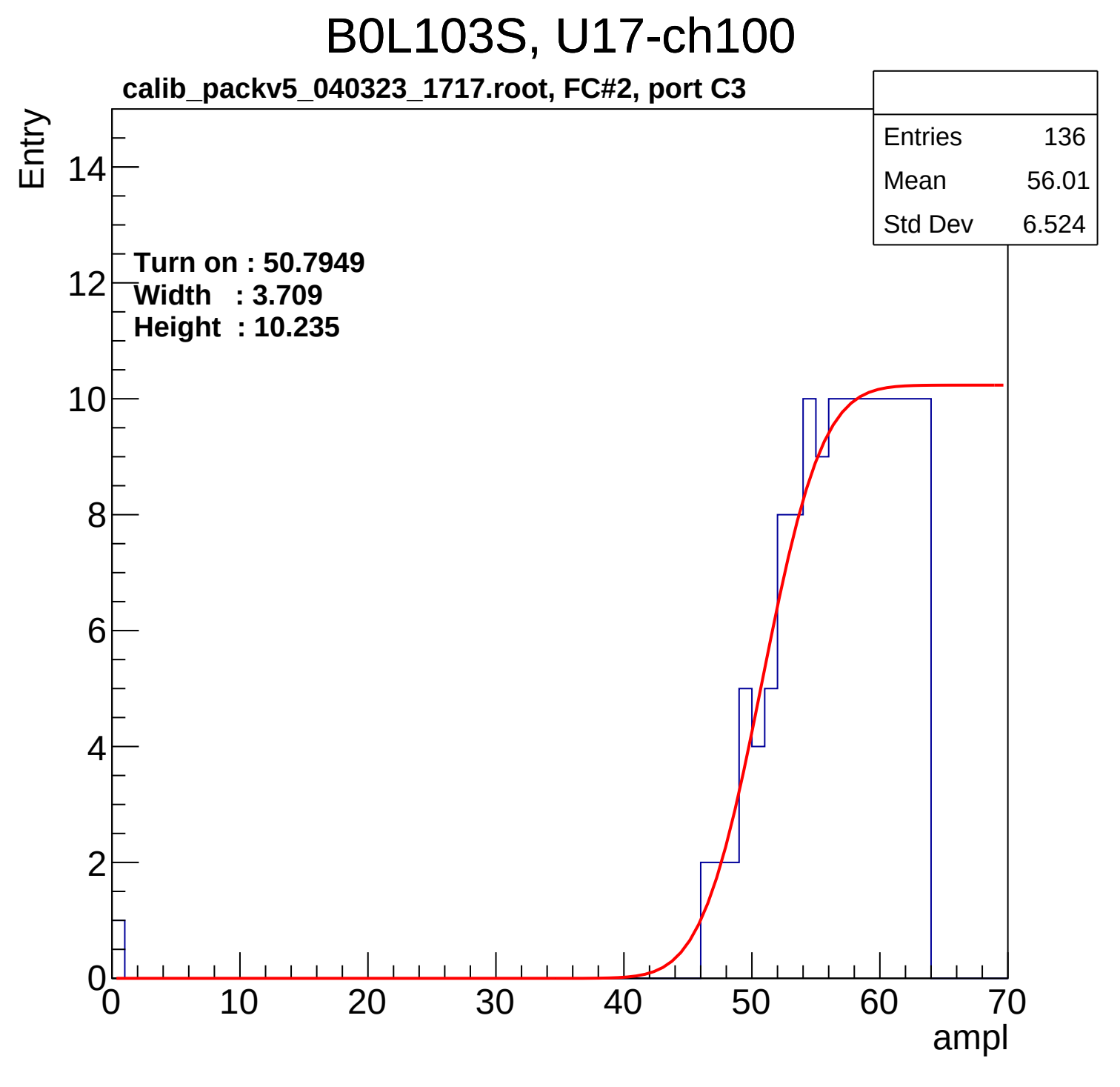
B0L103S, U17-ch100
calib_packv5_040323_1717.root, FC#2, port C3
Entries 136
Mean 56.01
Std Dev 6.524
Turn on : 50.7949
Width : 3.709
Height : 10.235
Entry
ampl
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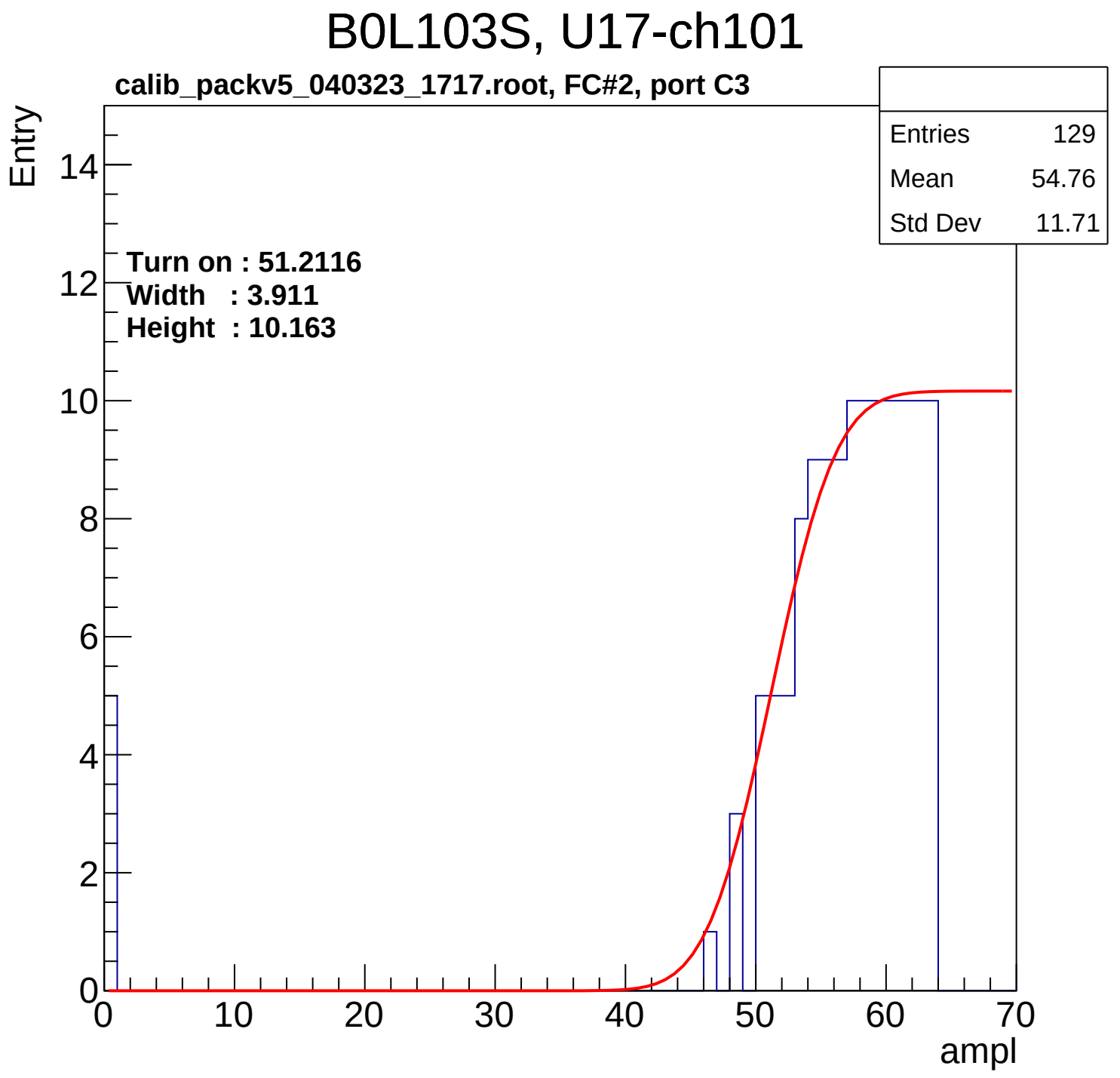
B0L103S, U17-ch101
calib_packv5_040323_1717.root, FC#2, port C3
Entries 129
Mean 54.76
Std Dev 11.71
Turn on : 51.2116
Width : 3.911
Height : 10.163
Entry
ampl
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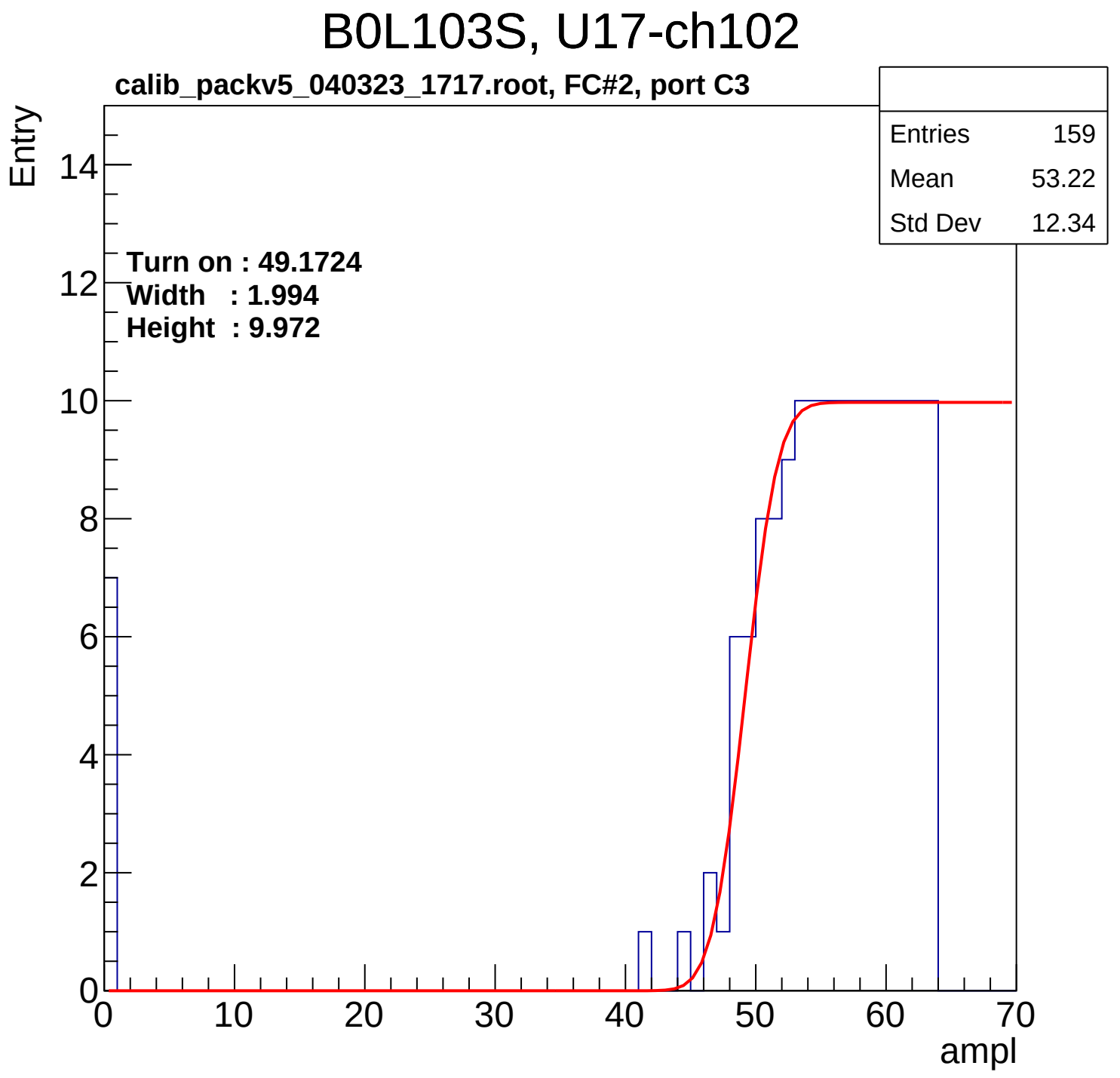
B0L103S, U17-ch102
calib_packv5_040323_1717.root, FC#2, port C3
Entries 159
Mean 53.22
Std Dev 12.34
Turn on : 49.1724
Width : 1.994
Height : 9.972
Entry
ampl
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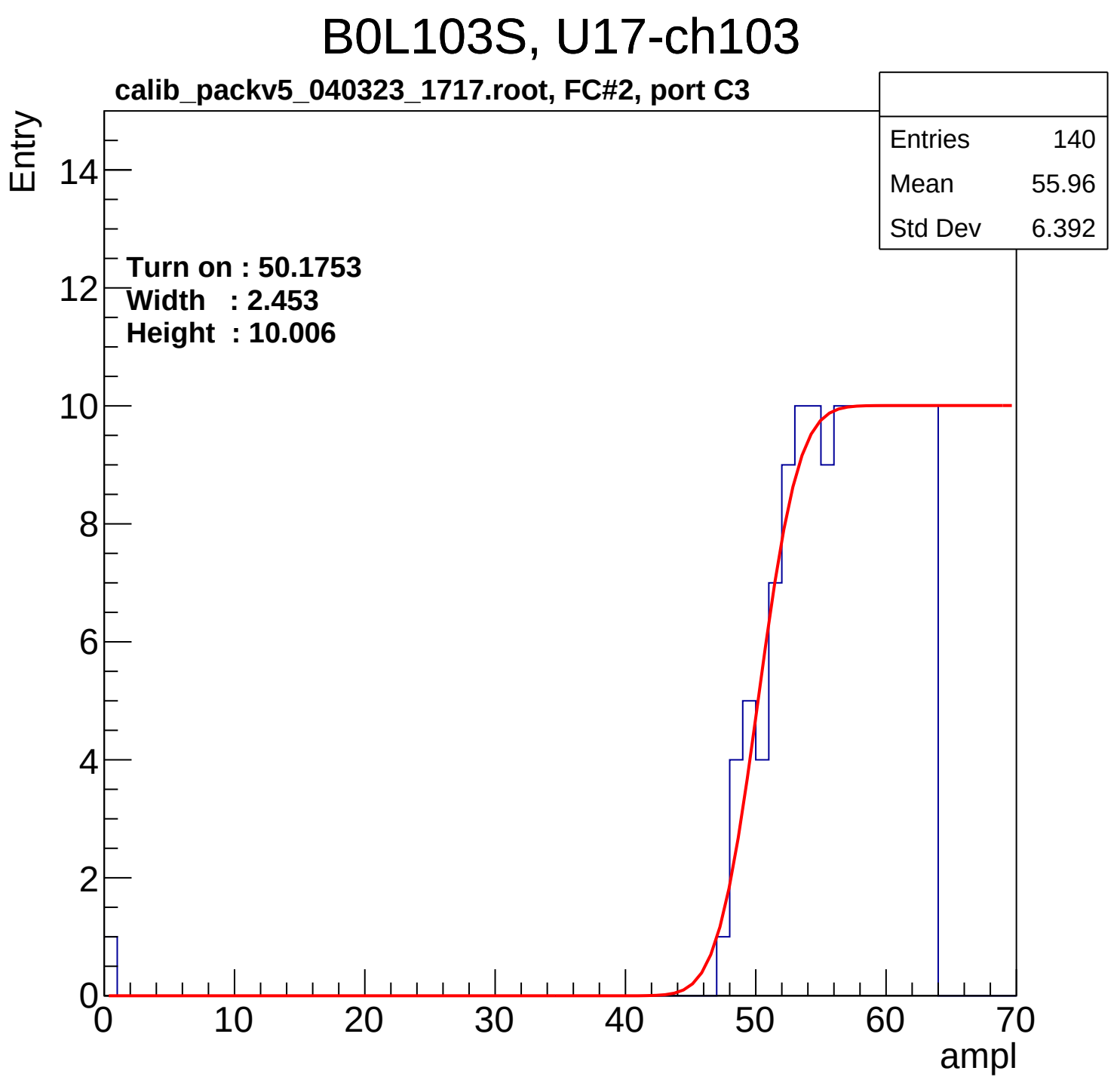
B0L103S, U17-ch103
calib_packv5_040323_1717.root, FC#2, port C3
Entries 140
Mean 55.96
Std Dev 6.392
Turn on : 50.1753
Width : 2.453
Height : 10.006
Entry
ampl
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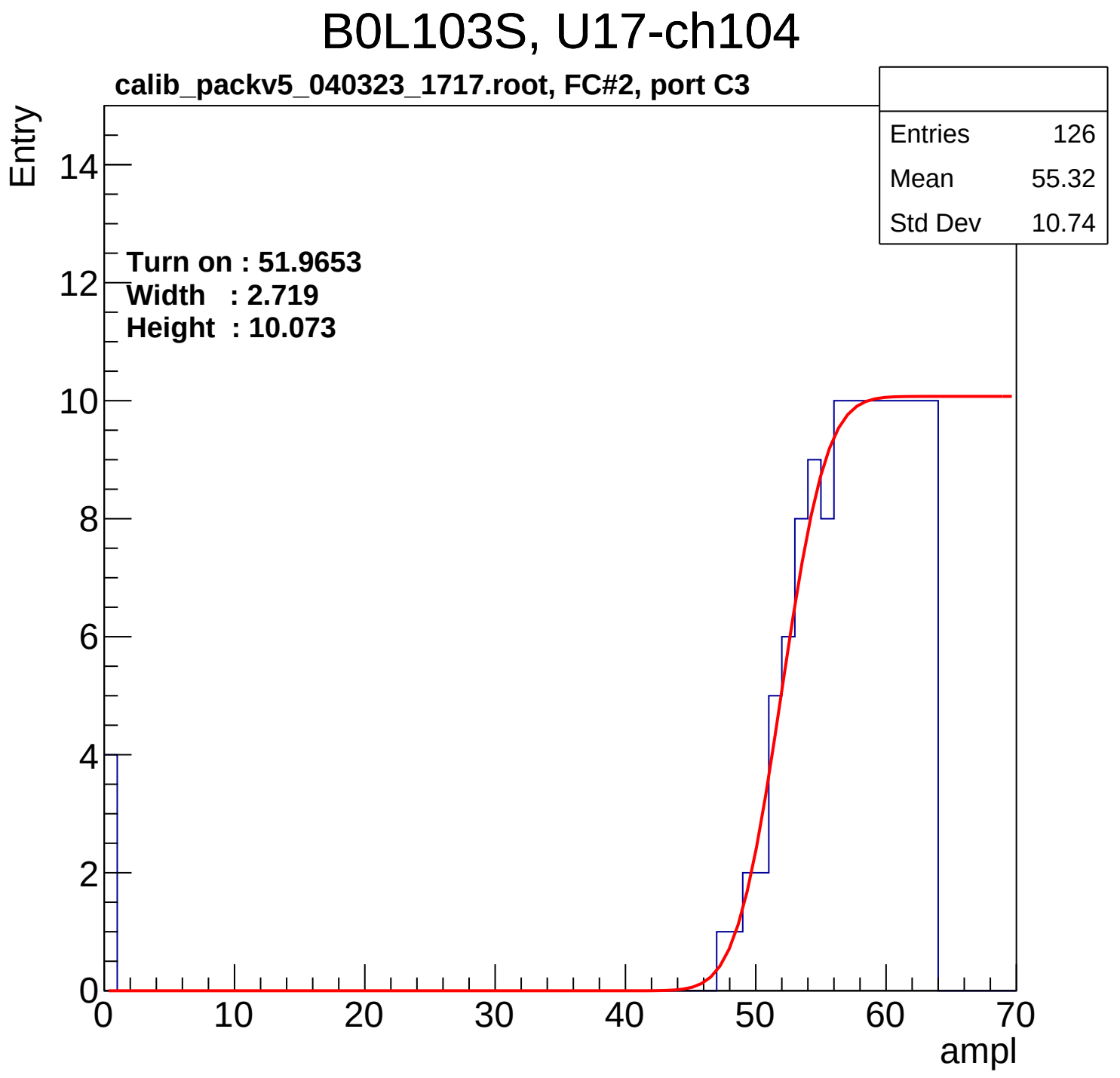
B0L103S, U17-ch104
calib_packv5_040323_1717.root, FC#2, port C3
Entries 126
Mean 55.32
Std Dev 10.74
Turn on : 51.9653
Width : 2.719
Height : 10.073
Entry
ampl
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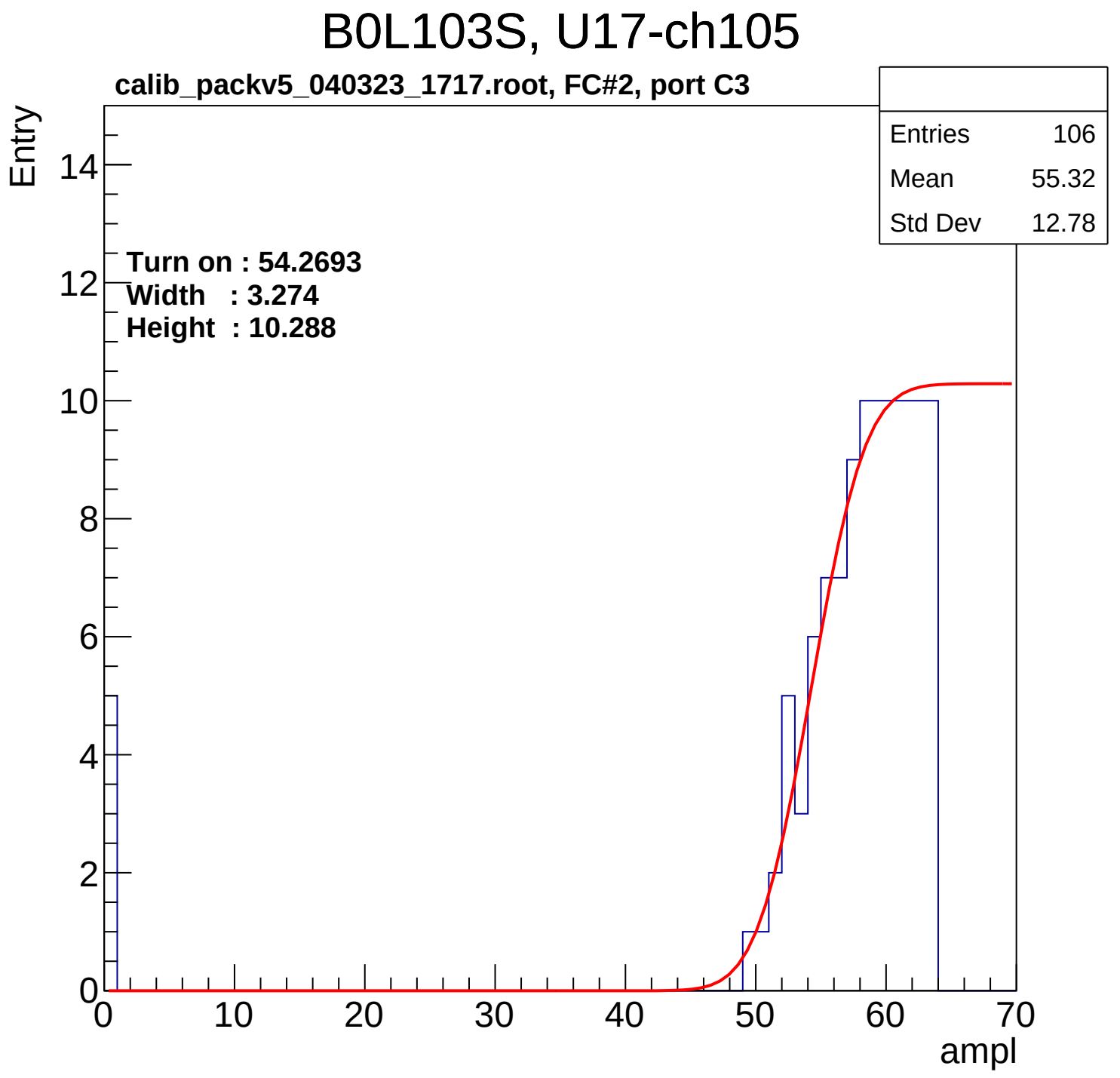
B0L103S, U17-ch105
calib_packv5_040323_1717.root, FC#2, port C3
Entries 106
Mean 55.32
Std Dev 12.78
Turn on : 54.2693
Width : 3.274
Height : 10.288
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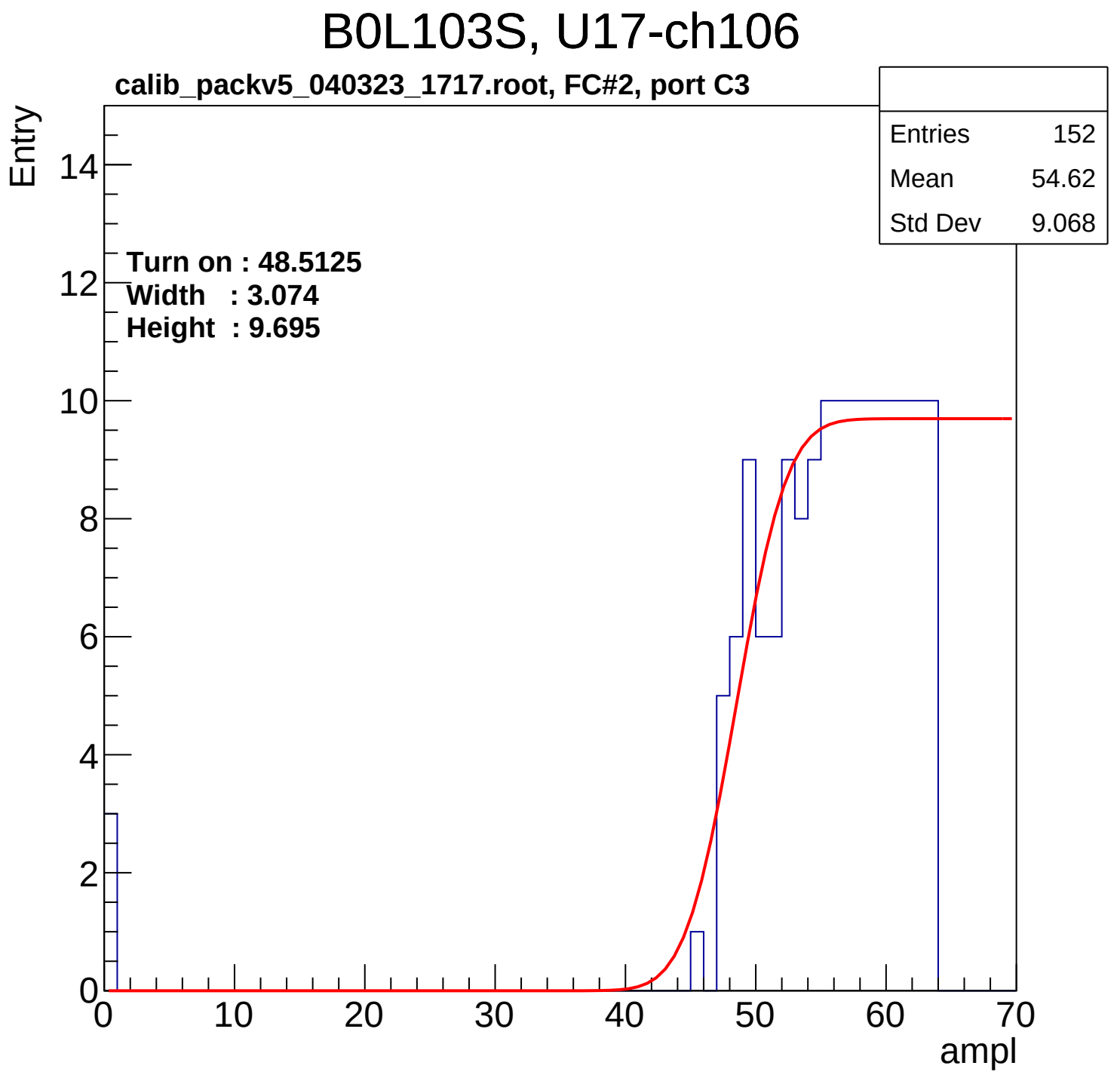
B0L103S, U17-ch106
calib_packv5_040323_1717.root, FC#2, port C3
Entries 152
Mean 54.62
Std Dev 9.068
Turn on : 48.5125
Width : 3.074
Height : 9.695
Entry
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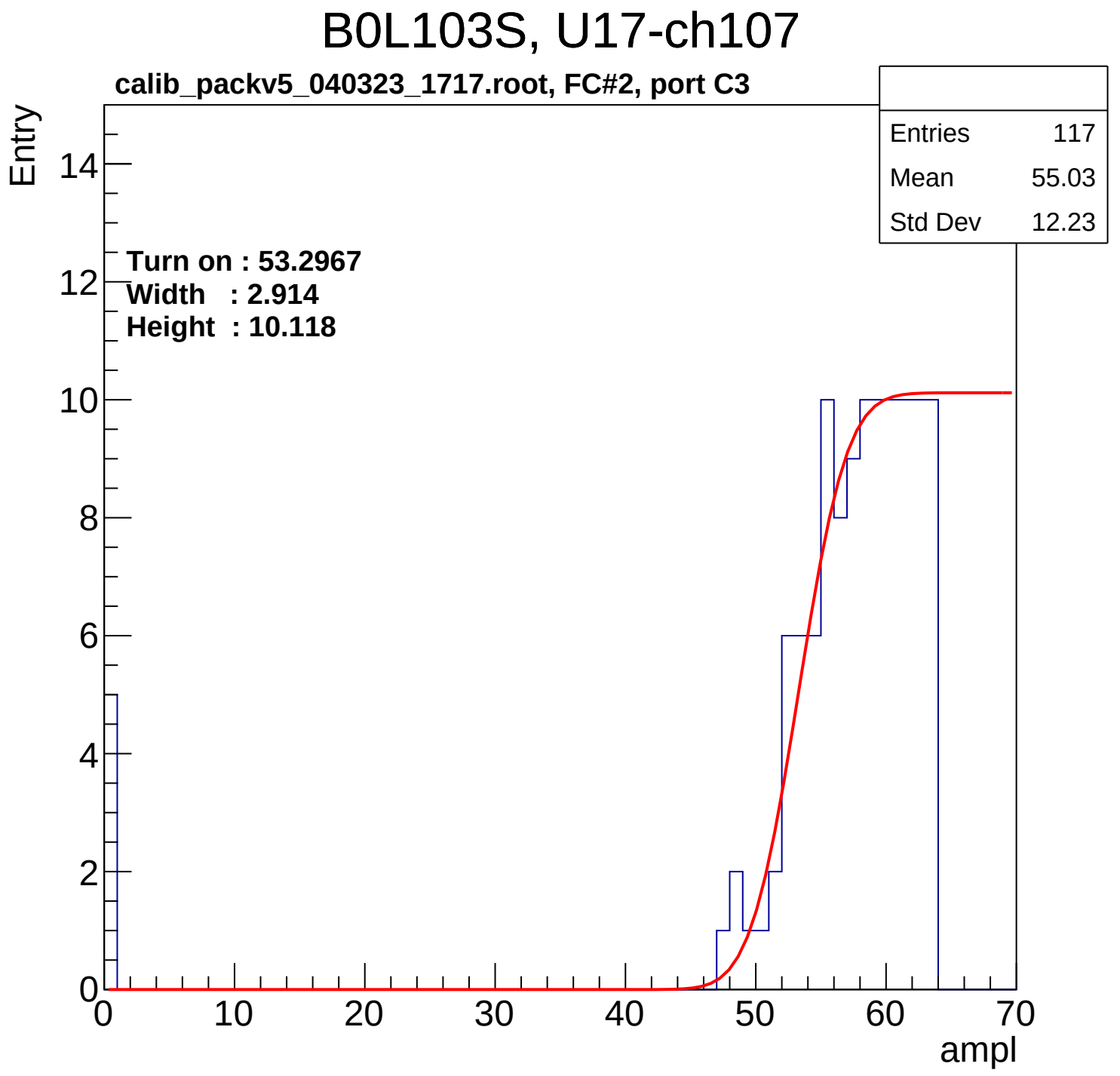
B0L103S, U17-ch107
calib_packv5_040323_1717.root, FC#2, port C3
Entries 117
Mean 55.03
Std Dev 12.23
Turn on : 53.2967
Width : 2.914
Height : 10.118
Entry
ampl
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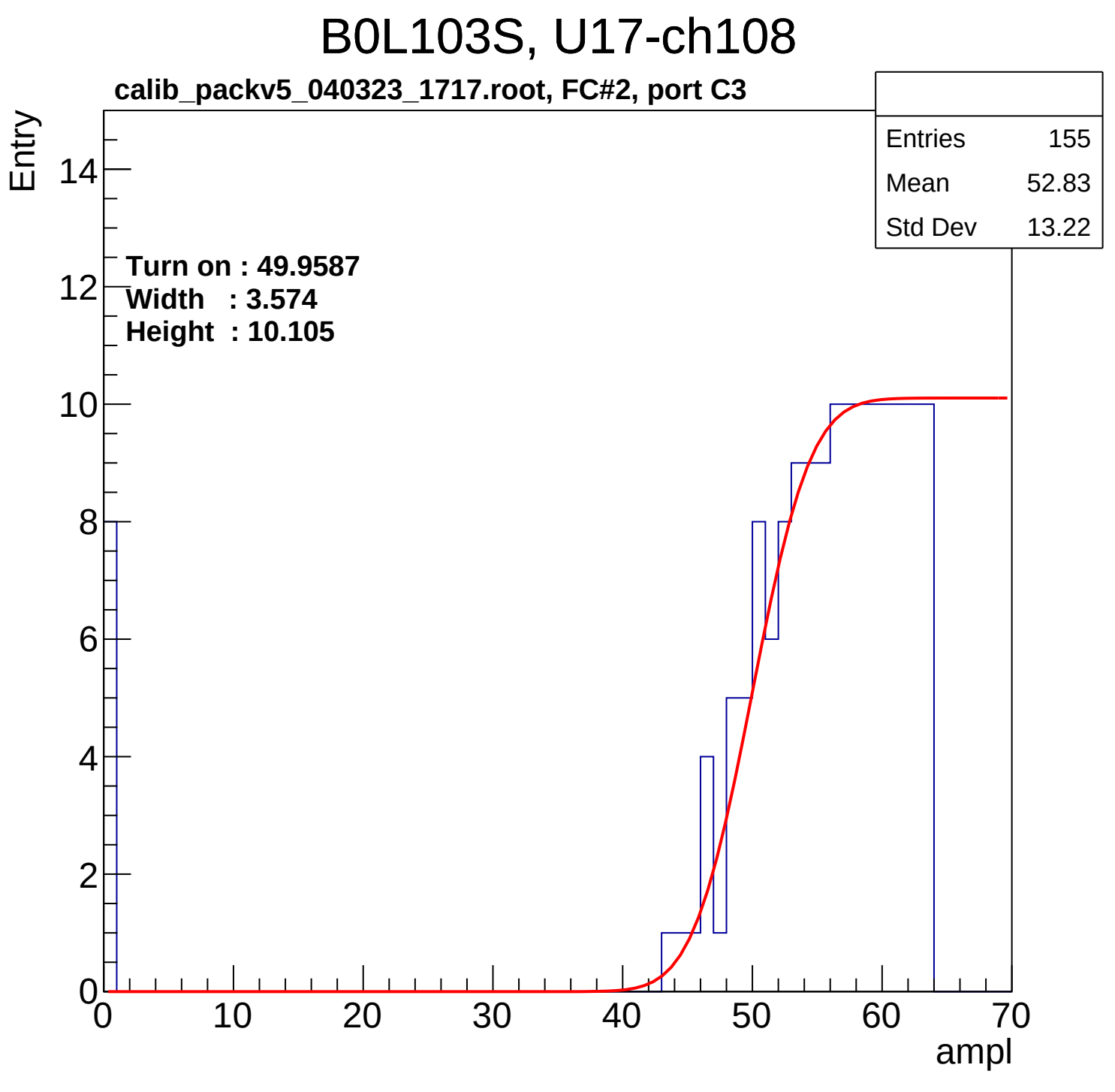
B0L103S, U17-ch108
calib_packv5_040323_1717.root, FC#2, port C3
Entries 155
Mean 52.83
Std Dev 13.22
Turn on : 49.9587
Width : 3.574
Height : 10.105
Entry
ampl
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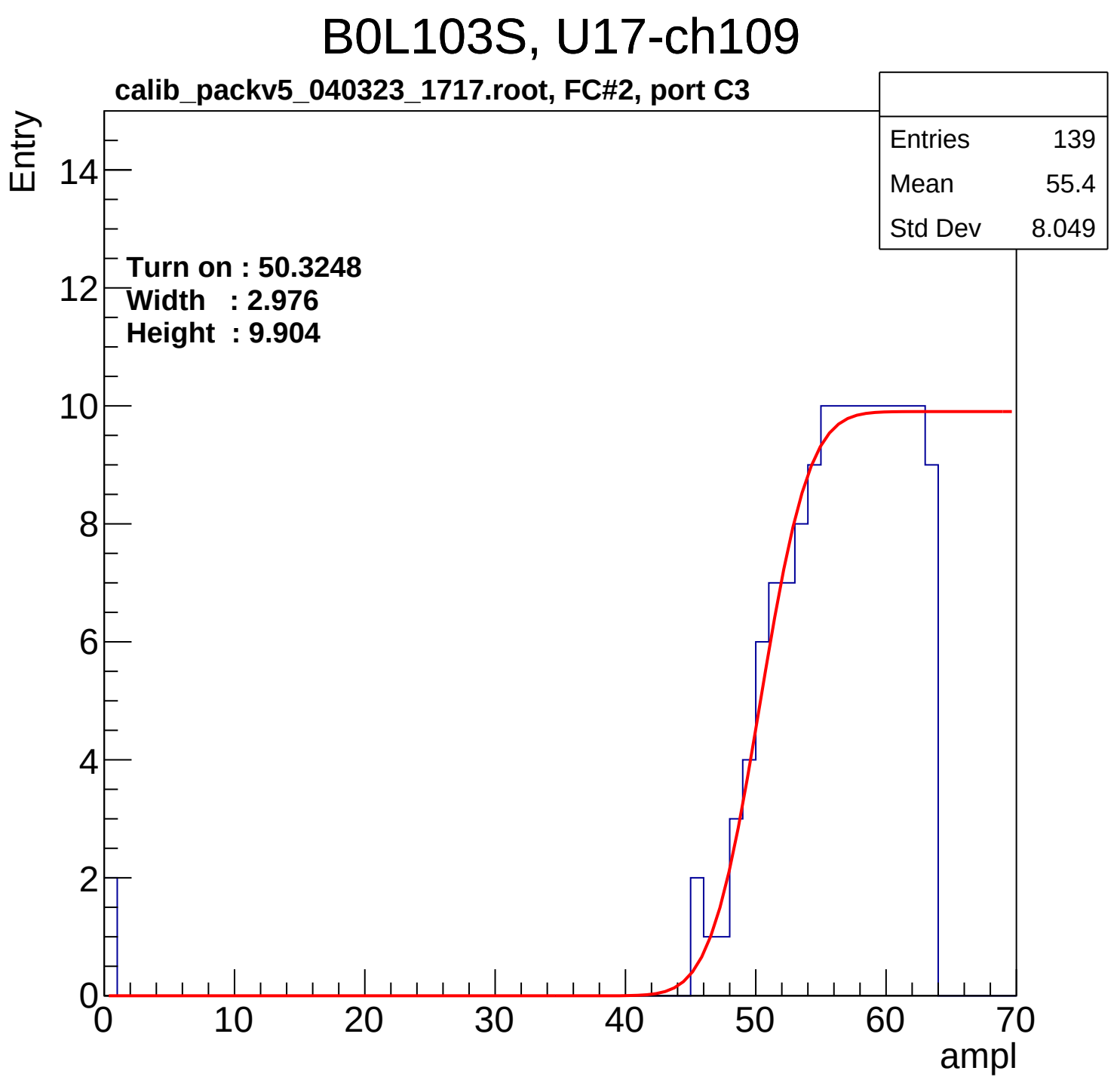
B0L103S, U17-ch109
calib_packv5_040323_1717.root, FC#2, port C3
Entries 139
Mean 55.4
Std Dev 8.049
Turn on : 50.3248
Width : 2.976
Height : 9.904
Entry
ampl
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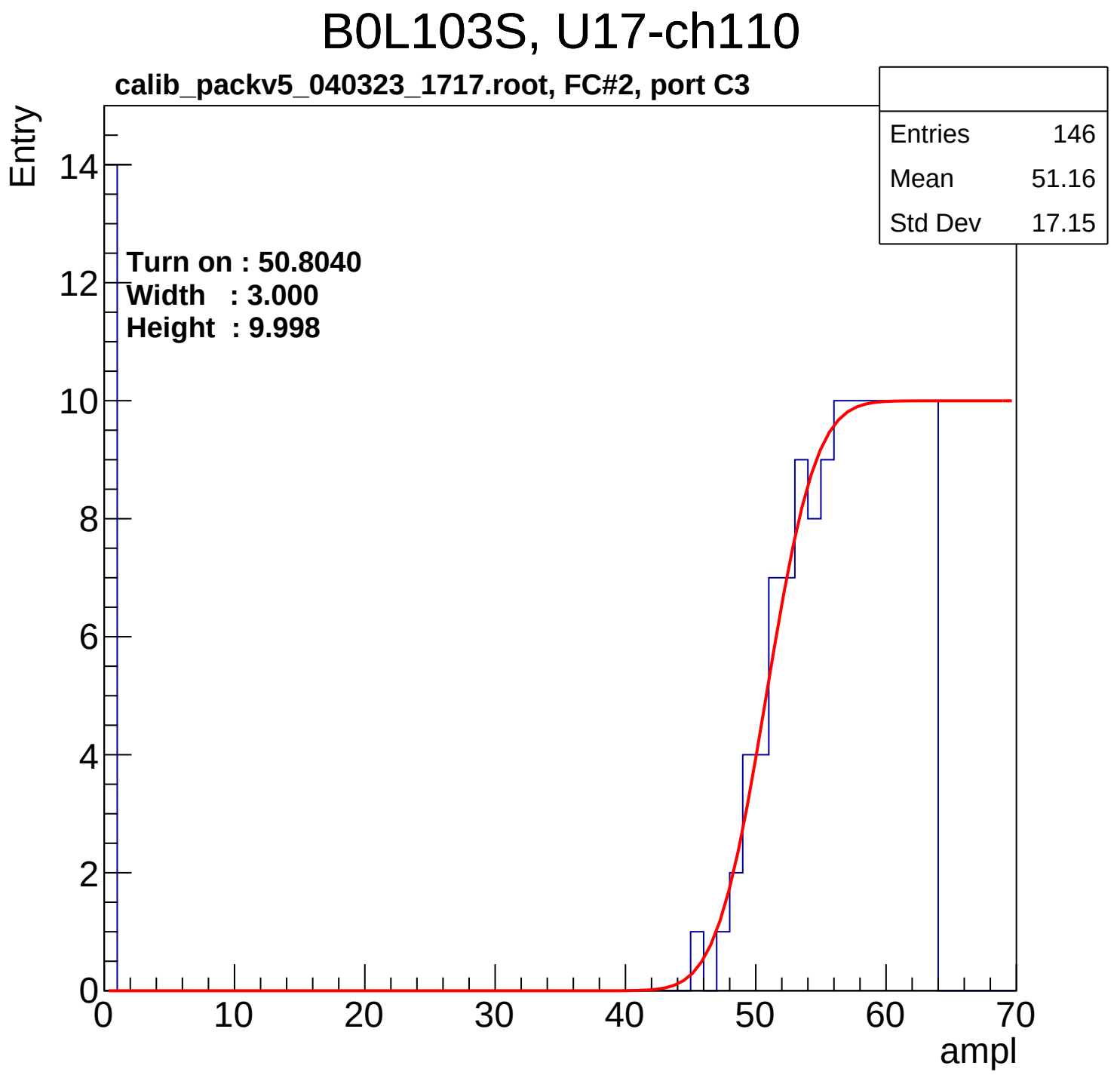
B0L103S, U17-ch110
calib_packv5_040323_1717.root, FC#2, port C3
Entries 146
Mean 51.16
Std Dev 17.15
Turn on : 50.8040
Width : 3.000
Height : 9.998
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ampl
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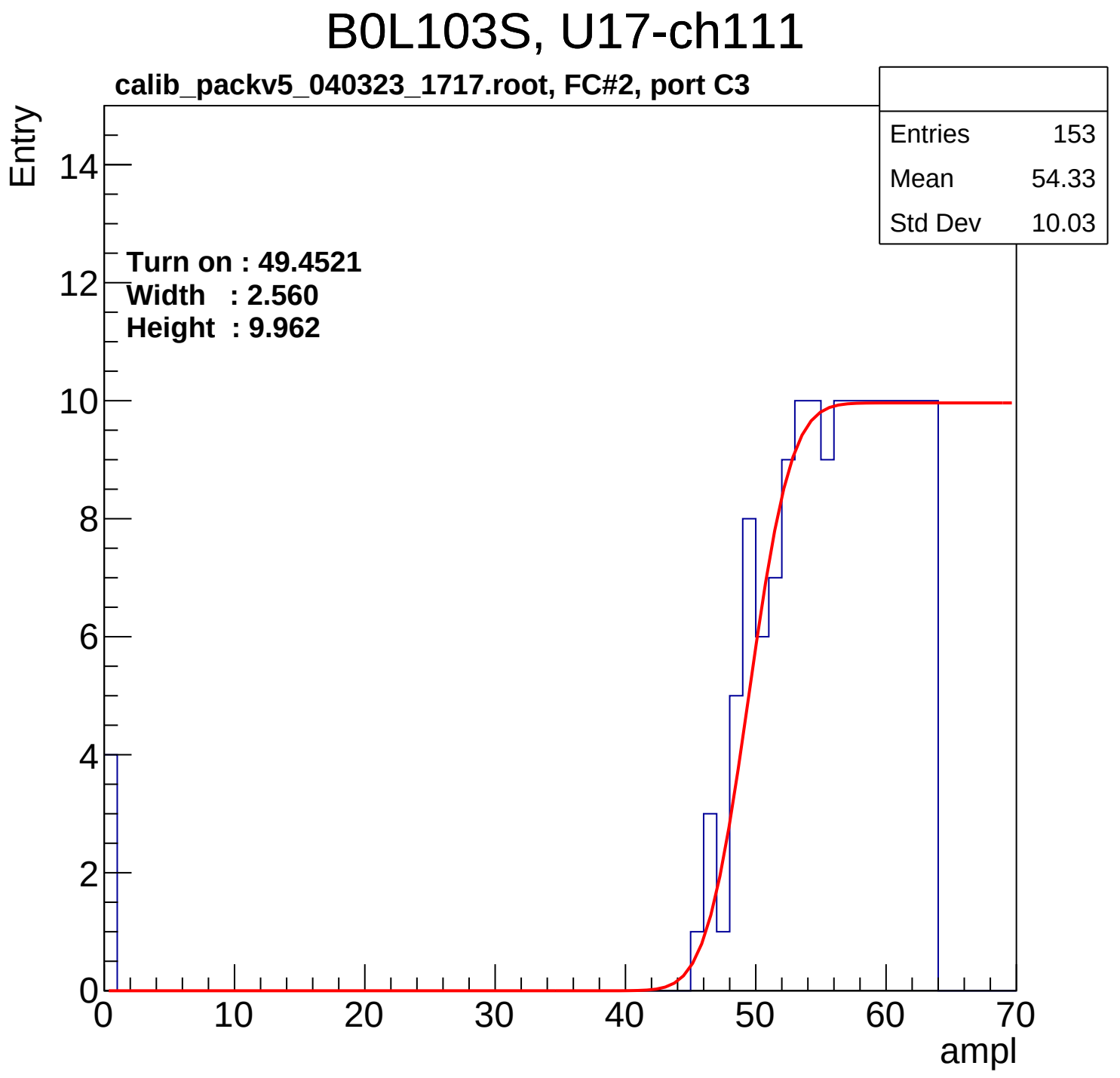
B0L103S, U17-ch111
calib_packv5_040323_1717.root, FC#2, port C3
Entries 153
Mean 54.33
Std Dev 10.03
Turn on : 49.4521
Width : 2.560
Height : 9.962
Entry
ampl
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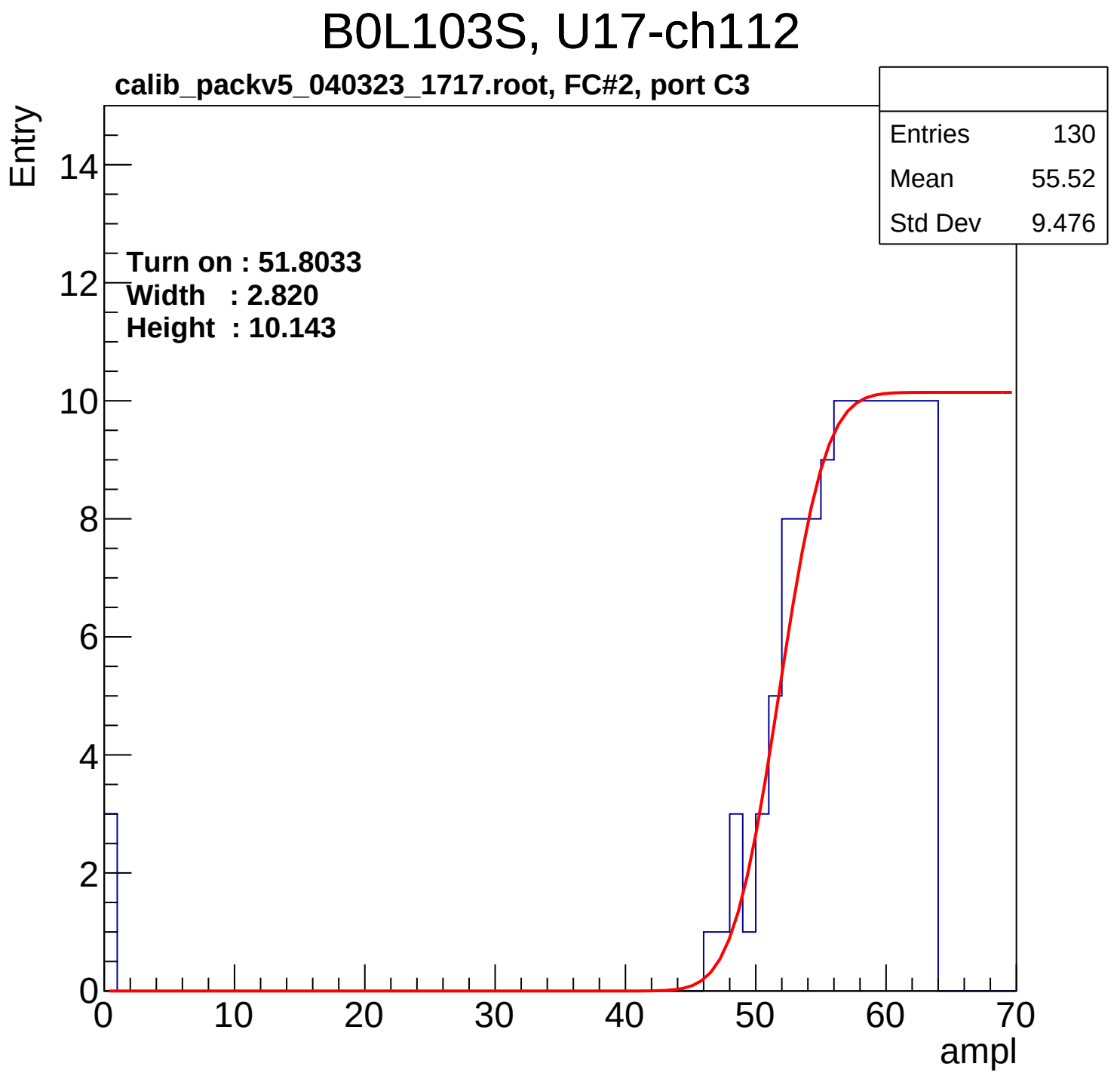
B0L103S, U17-ch112
calib_packv5_040323_1717.root, FC#2, port C3
Entries 130
Mean 55.52
Std Dev 9.476
Turn on : 51.8033
Width : 2.820
Height : 10.143
Entry
ampl
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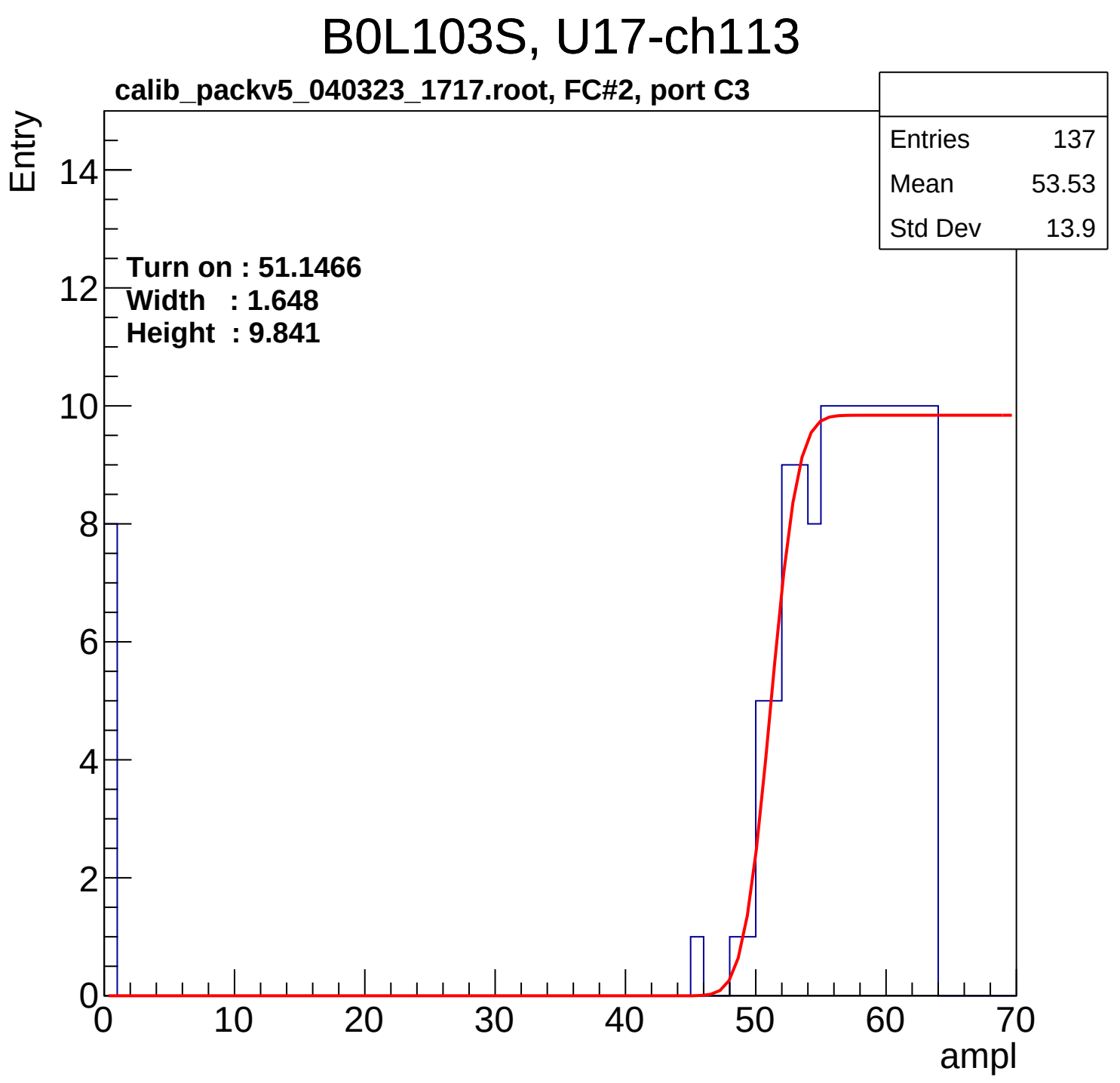
B0L103S, U17-ch113
calib_packv5_040323_1717.root, FC#2, port C3
Entries 137
Mean 53.53
Std Dev 13.9
Turn on : 51.1466
Width : 1.648
Height : 9.841
Entry
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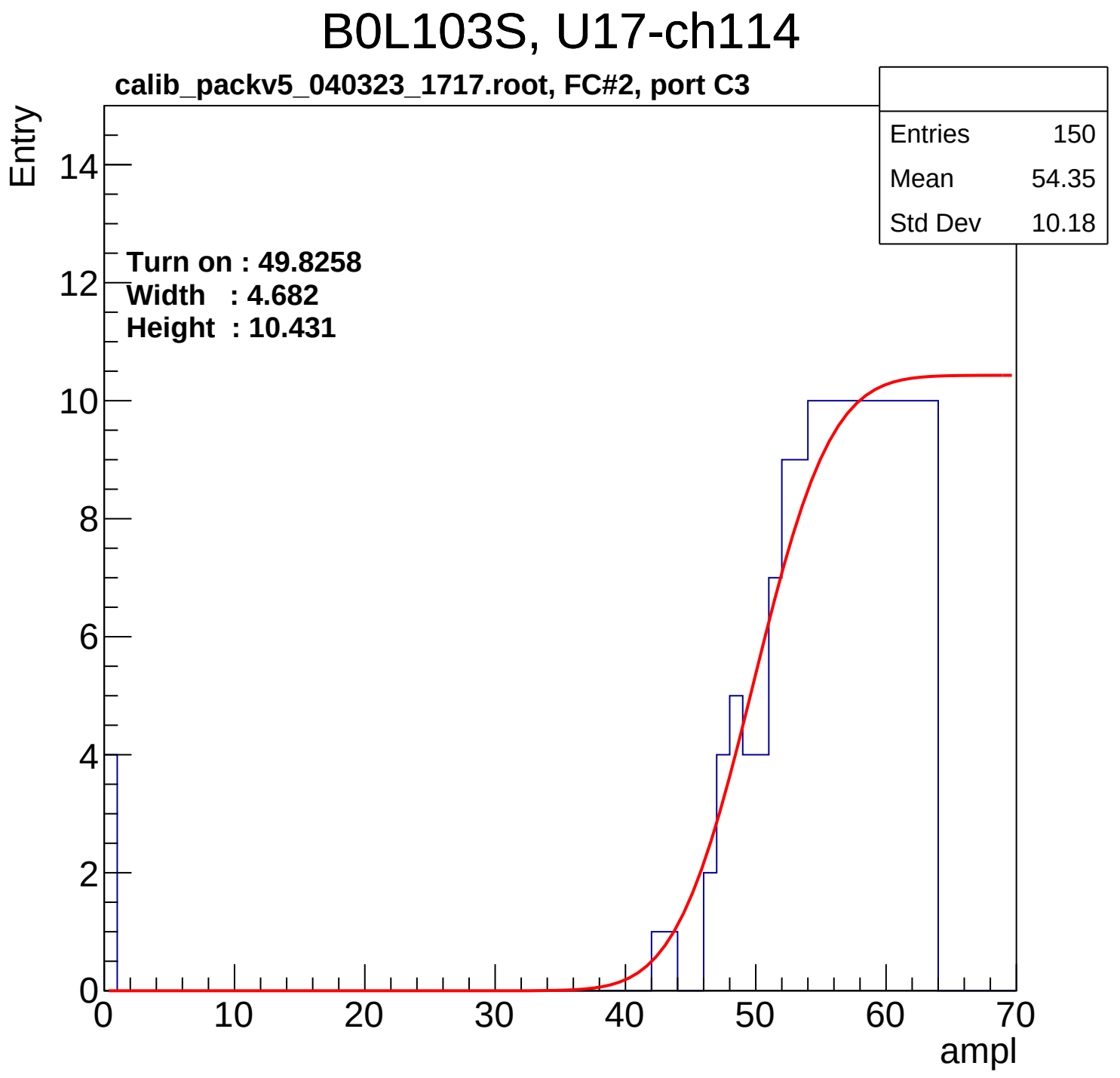
B0L103S, U17-ch114
calib_packv5_040323_1717.root, FC#2, port C3
Entries 150
Mean 54.35
Std Dev 10.18
Turn on : 49.8258
Width : 4.682
Height : 10.431
Entry
ampl
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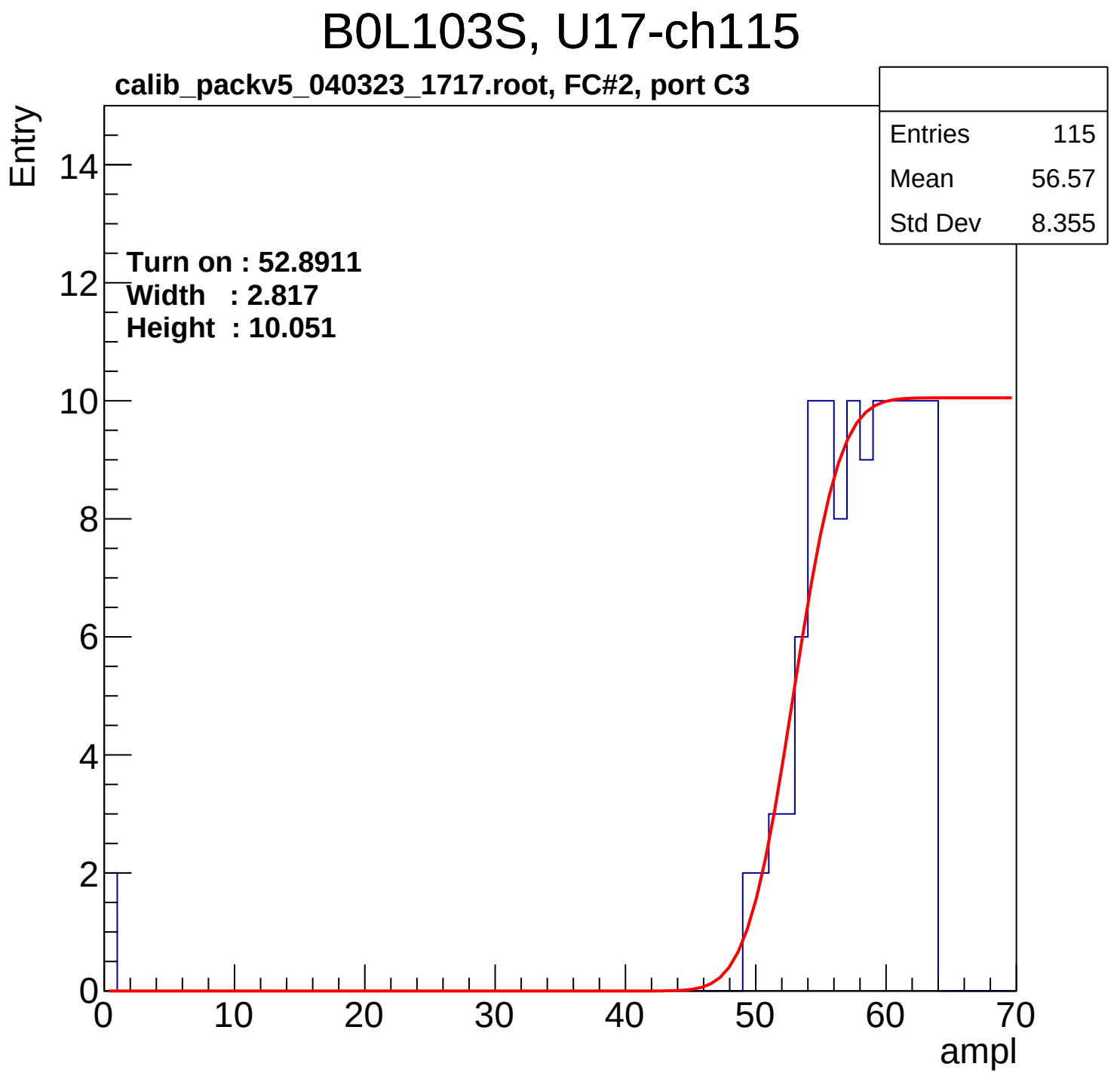
B0L103S, U17-ch115
calib_packv5_040323_1717.root, FC#2, port C3
Entries 115
Mean 56.57
Std Dev 8.355
Turn on : 52.8911
Width : 2.817
Height : 10.051
Entry
ampl
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2
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6
8
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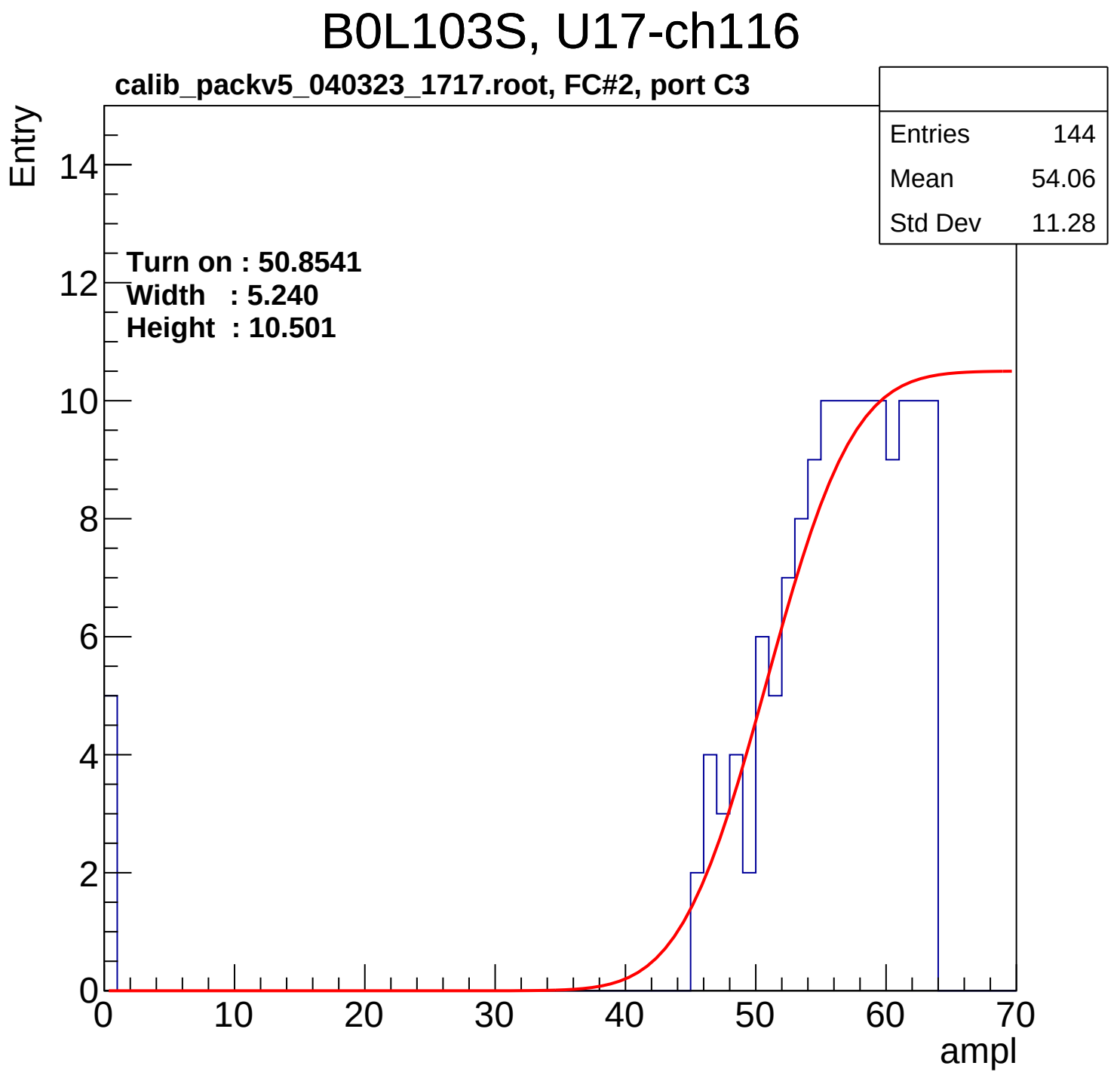
B0L103S, U17-ch116
calib_packv5_040323_1717.root, FC#2, port C3
Entries 144
Mean 54.06
Std Dev 11.28
Turn on : 50.8541
Width : 5.240
Height : 10.501
Entry
ampl
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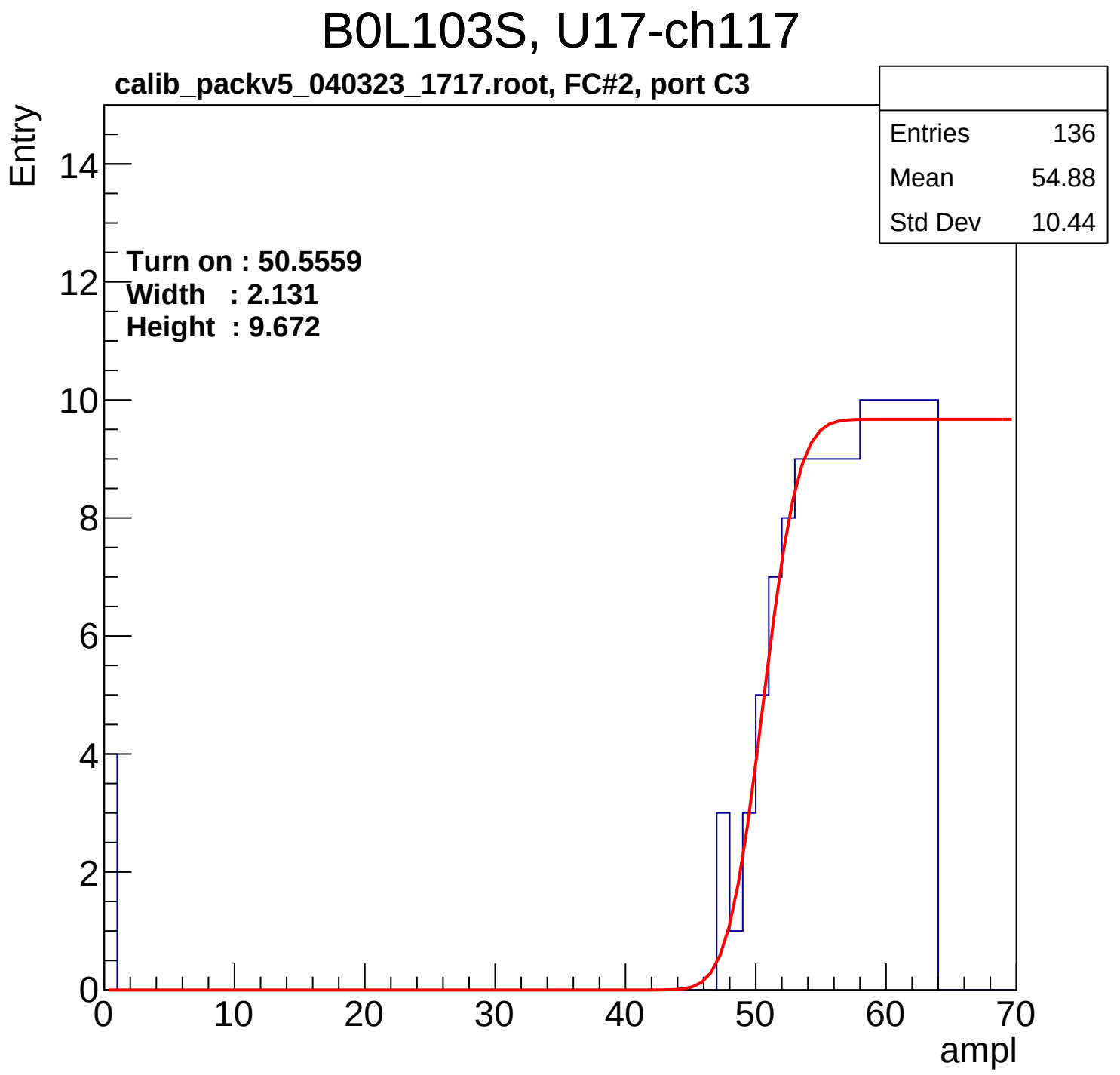
B0L103S, U17-ch117
calib_packv5_040323_1717.root, FC#2, port C3
Entries 136
Mean 54.88
Std Dev 10.44
Turn on : 50.5559
Width : 2.131
Height : 9.672
Entry
ampl
0
2
4
6
8
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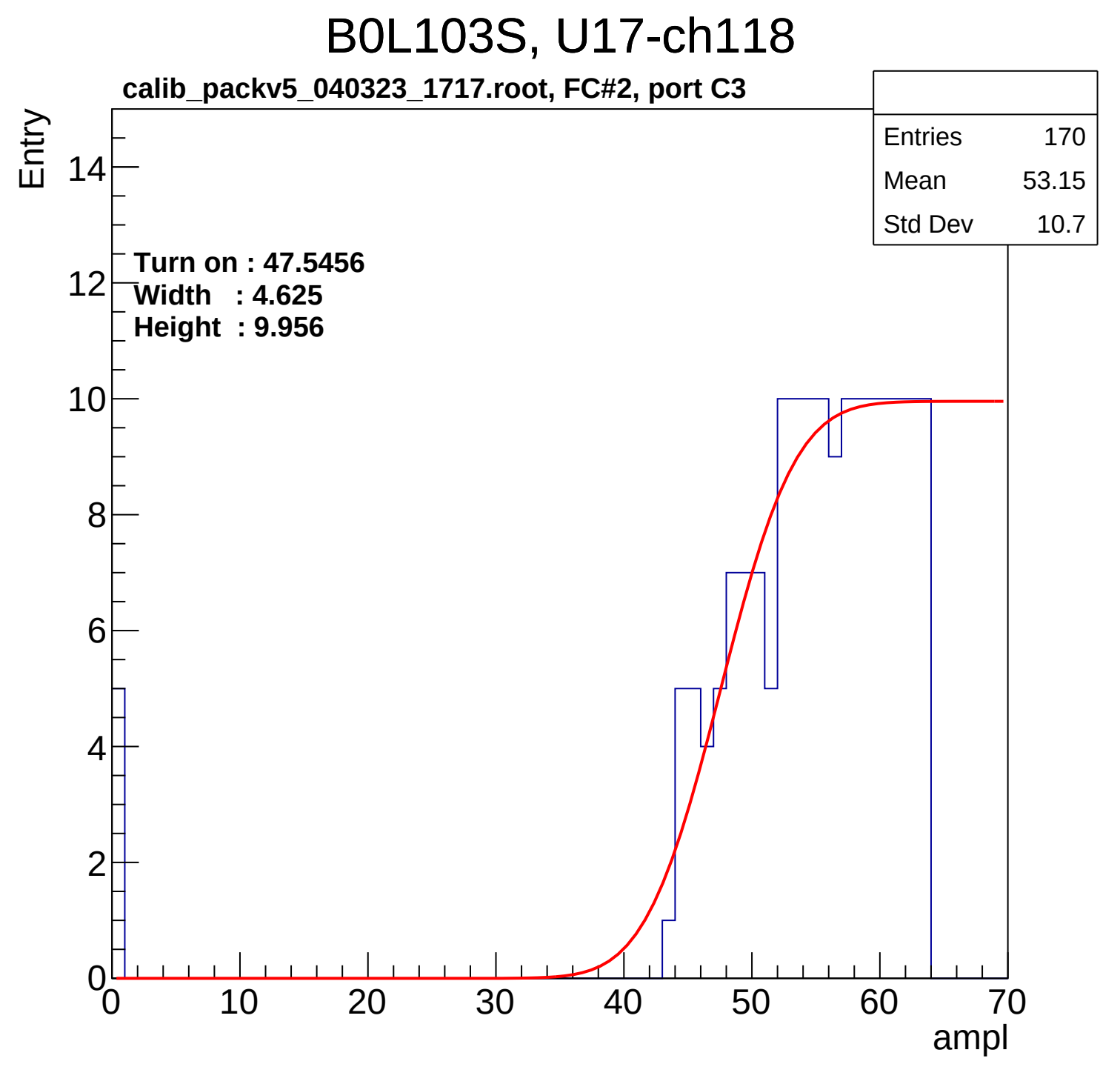
B0L103S, U17-ch118
calib_packv5_040323_1717.root, FC#2, port C3
Entries 170
Mean 53.15
Std Dev 10.7
Turn on : 47.5456
Width : 4.625
Height : 9.956
Entry
ampl
0
2
4
6
8
10
12
14
0
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40
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60
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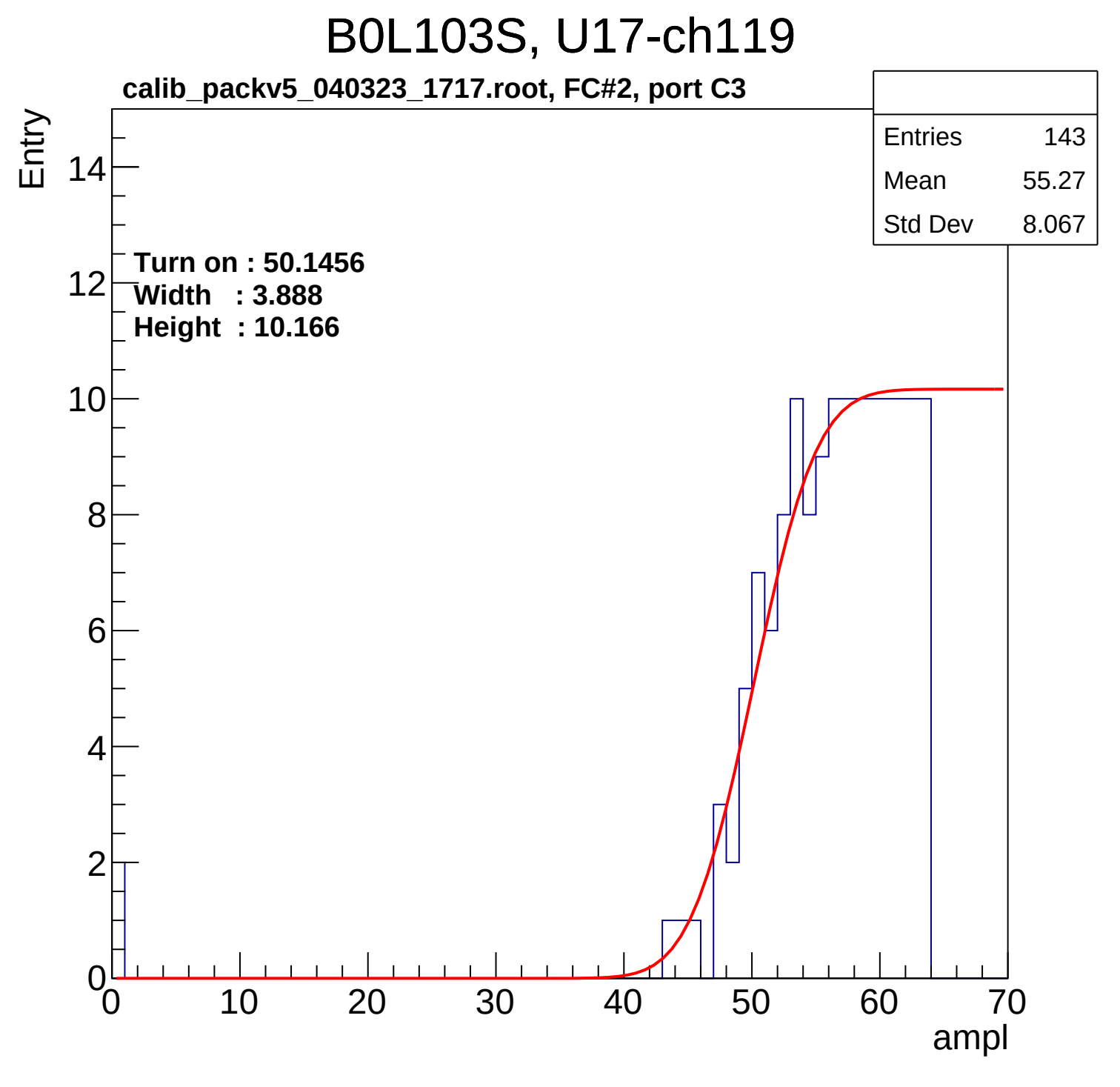
B0L103S, U17-ch119
calib_packv5_040323_1717.root, FC#2, port C3
Entries 143
Mean 55.27
Std Dev 8.067
Turn on : 50.1456
Width : 3.888
Height : 10.166
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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40
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60
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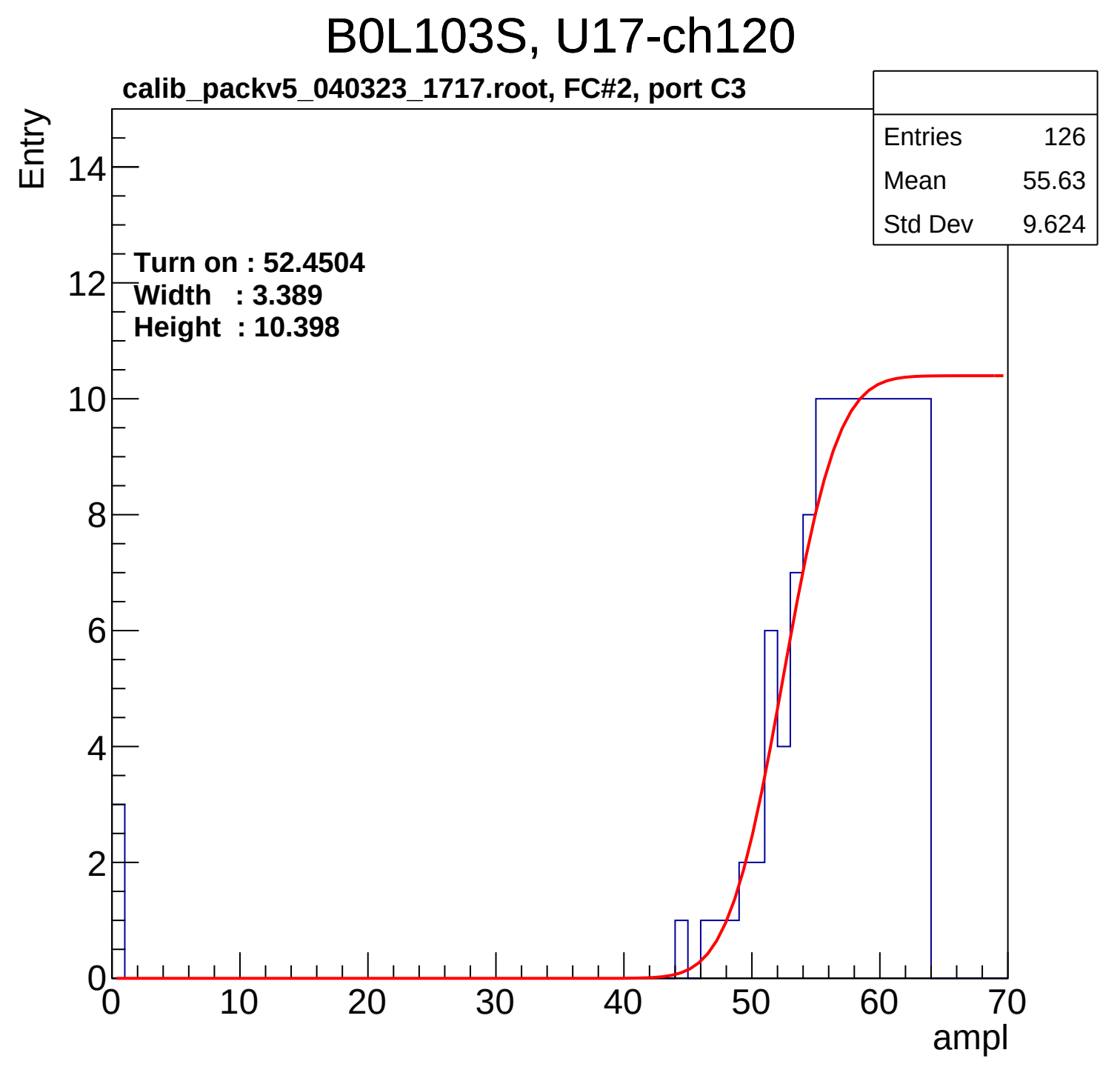
B0L103S, U17-ch120
calib_packv5_040323_1717.root, FC#2, port C3
Entries 126
Mean 55.63
Std Dev 9.624
Turn on : 52.4504
Width : 3.389
Height : 10.398
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
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60
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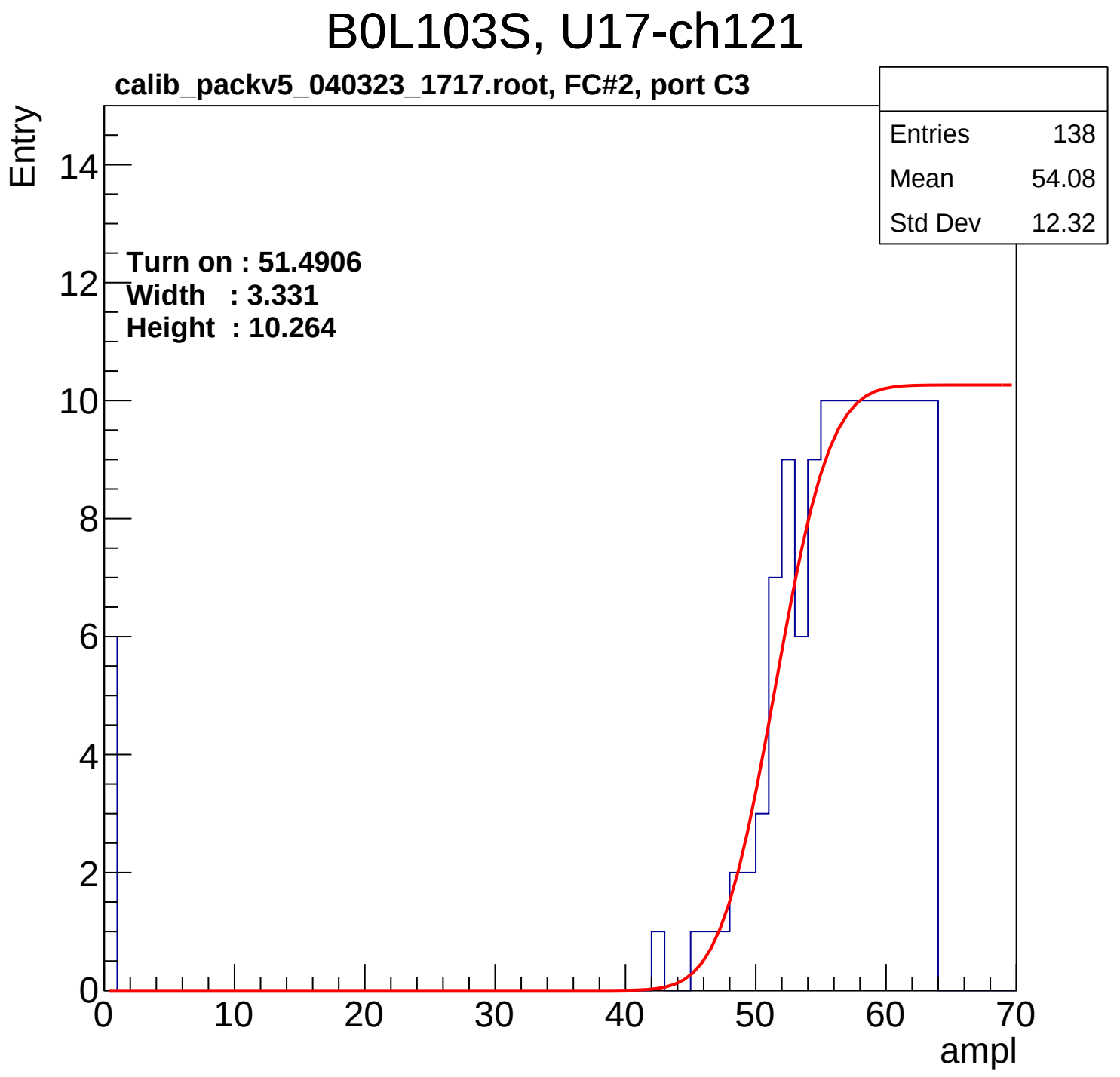
B0L103S, U17-ch121
calib_packv5_040323_1717.root, FC#2, port C3
Entries 138
Mean 54.08
Std Dev 12.32
Turn on : 51.4906
Width : 3.331
Height : 10.264
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
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60
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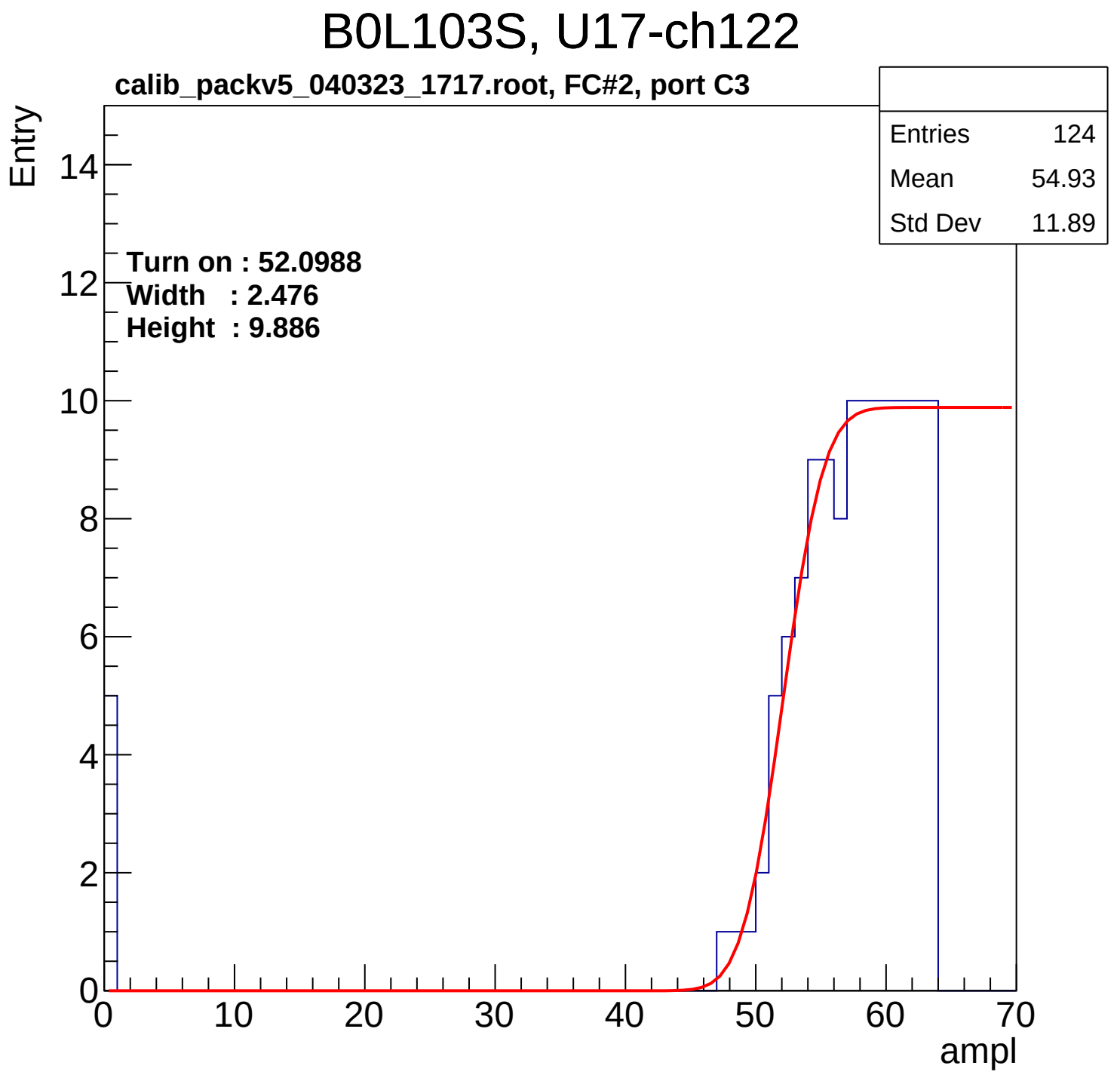
B0L103S, U17-ch122
calib_packv5_040323_1717.root, FC#2, port C3
Entries 124
Mean 54.93
Std Dev 11.89
Turn on : 52.0988
Width : 2.476
Height : 9.886
Entry
ampl
0
2
4
6
8
10
12
14
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10
20
30
40
50
60
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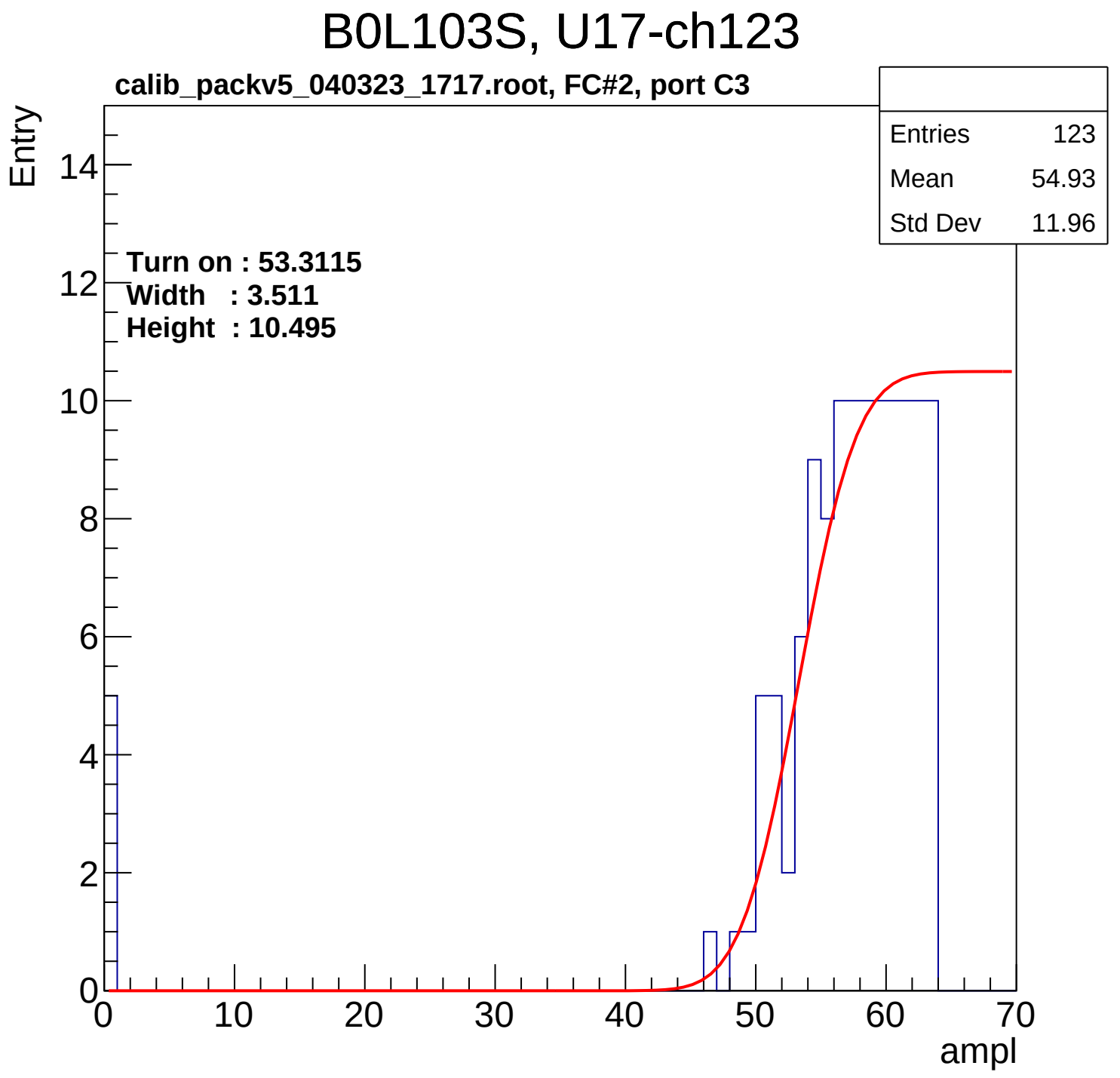
B0L103S, U17-ch123
calib_packv5_040323_1717.root, FC#2, port C3
Entries 123
Mean 54.93
Std Dev 11.96
Turn on : 53.3115
Width : 3.511
Height : 10.495
Entry
ampl
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2
4
6
8
10
12
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20
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40
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60
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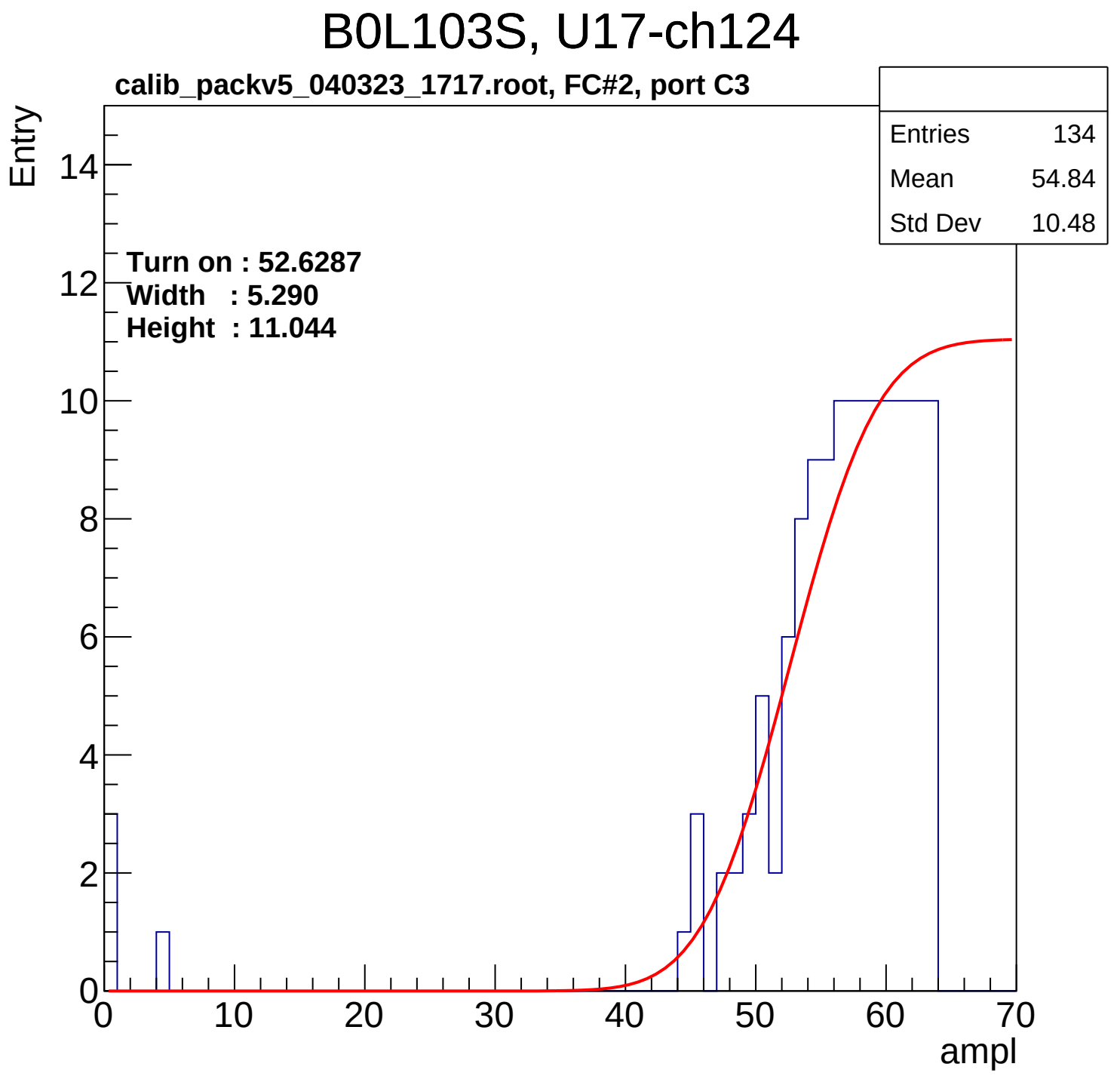
B0L103S, U17-ch124
calib_packv5_040323_1717.root, FC#2, port C3
Entries 134
Mean 54.84
Std Dev 10.48
Turn on : 52.6287
Width : 5.290
Height : 11.044
Entry
ampl
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2
4
6
8
10
12
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0
10
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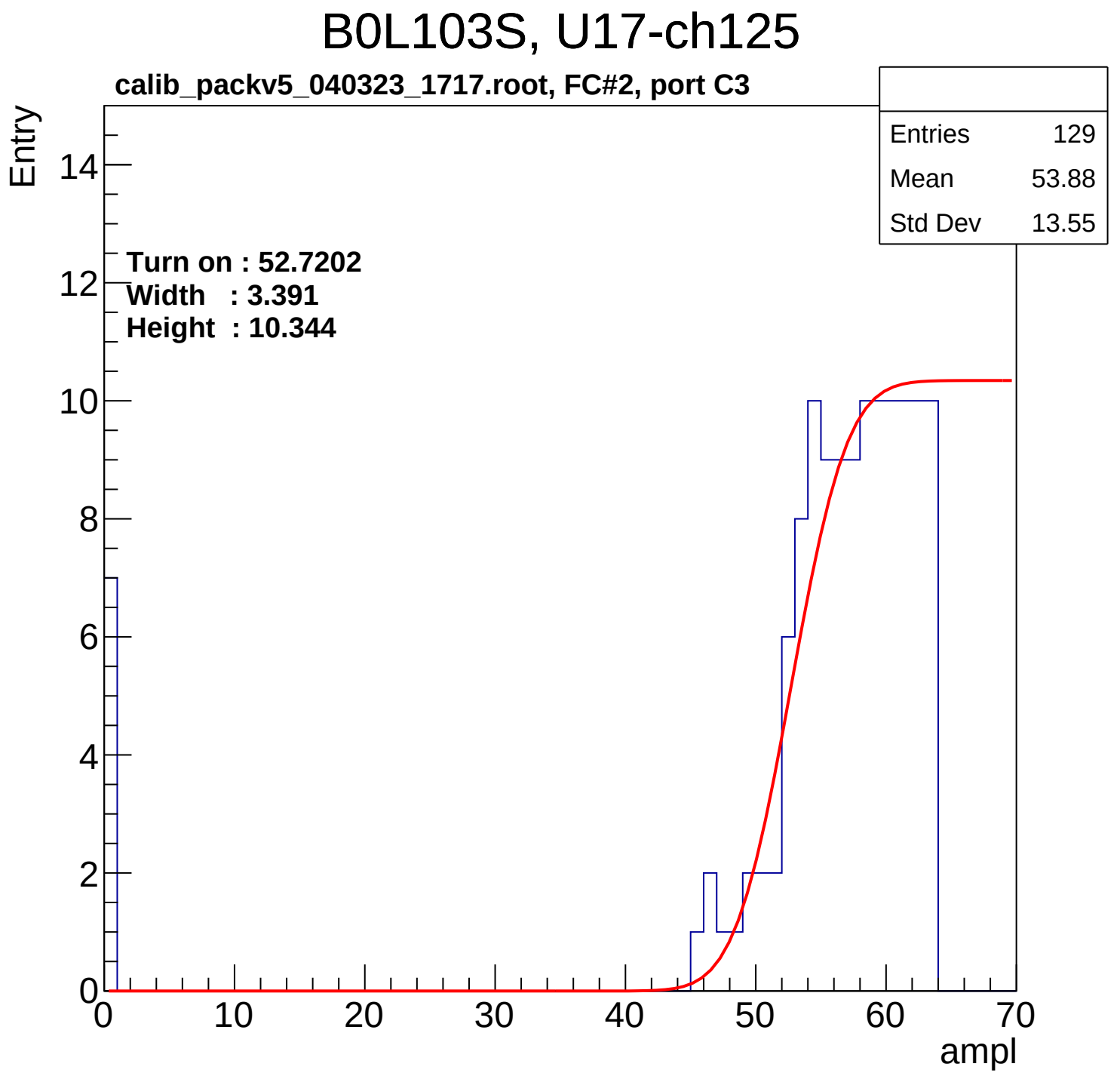
B0L103S, U17-ch125
calib_packv5_040323_1717.root, FC#2, port C3
Entries 129
Mean 53.88
Std Dev 13.55
Turn on : 52.7202
Width : 3.391
Height : 10.344
Entry
ampl
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2
4
6
8
10
12
14
0
10
20
30
40
50
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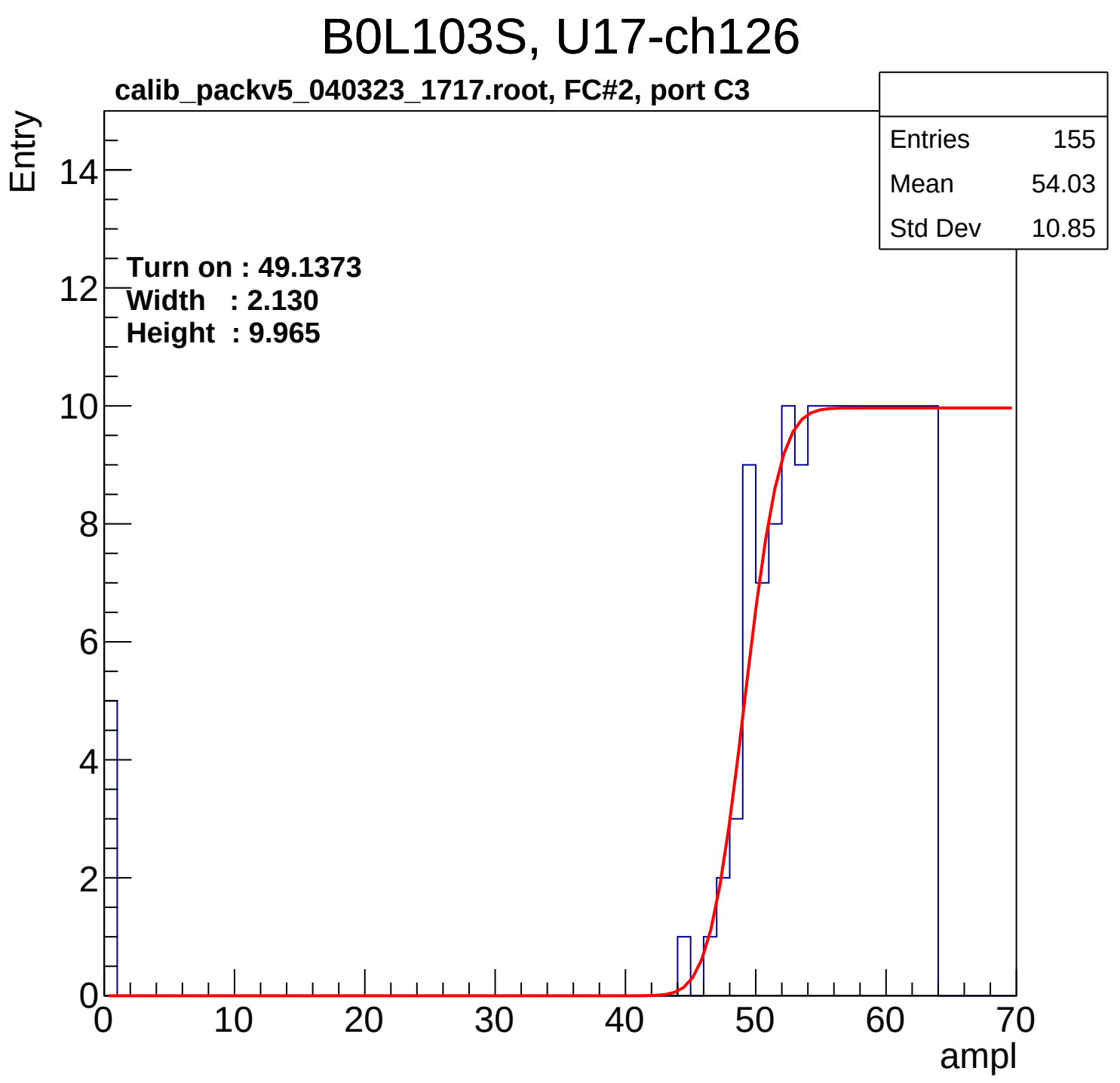
B0L103S, U17-ch126
calib_packv5_040323_1717.root, FC#2, port C3
Entries 155
Mean 54.03
Std Dev 10.85
Turn on : 49.1373
Width : 2.130
Height : 9.965
Entry
ampl
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2
4
6
8
10
12
14
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10
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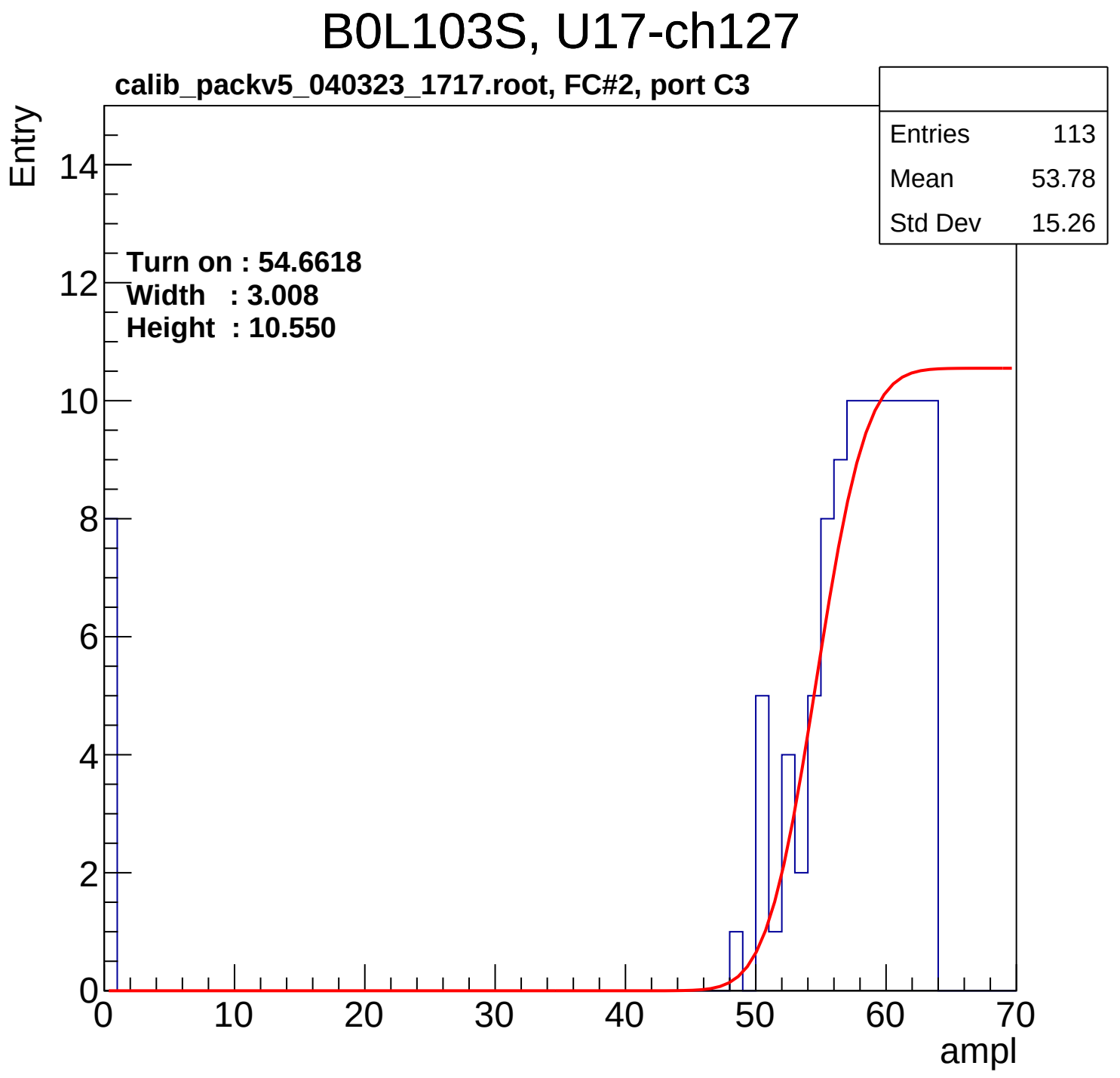
B0L103S, U17-ch127
calib_packv5_040323_1717.root, FC#2, port C3
Entries 113
Mean 53.78
Std Dev 15.26
Turn on : 54.6618
Width : 3.008
Height : 10.550
Entry
ampl
0
2
4
6
8
10
12
14
0
10
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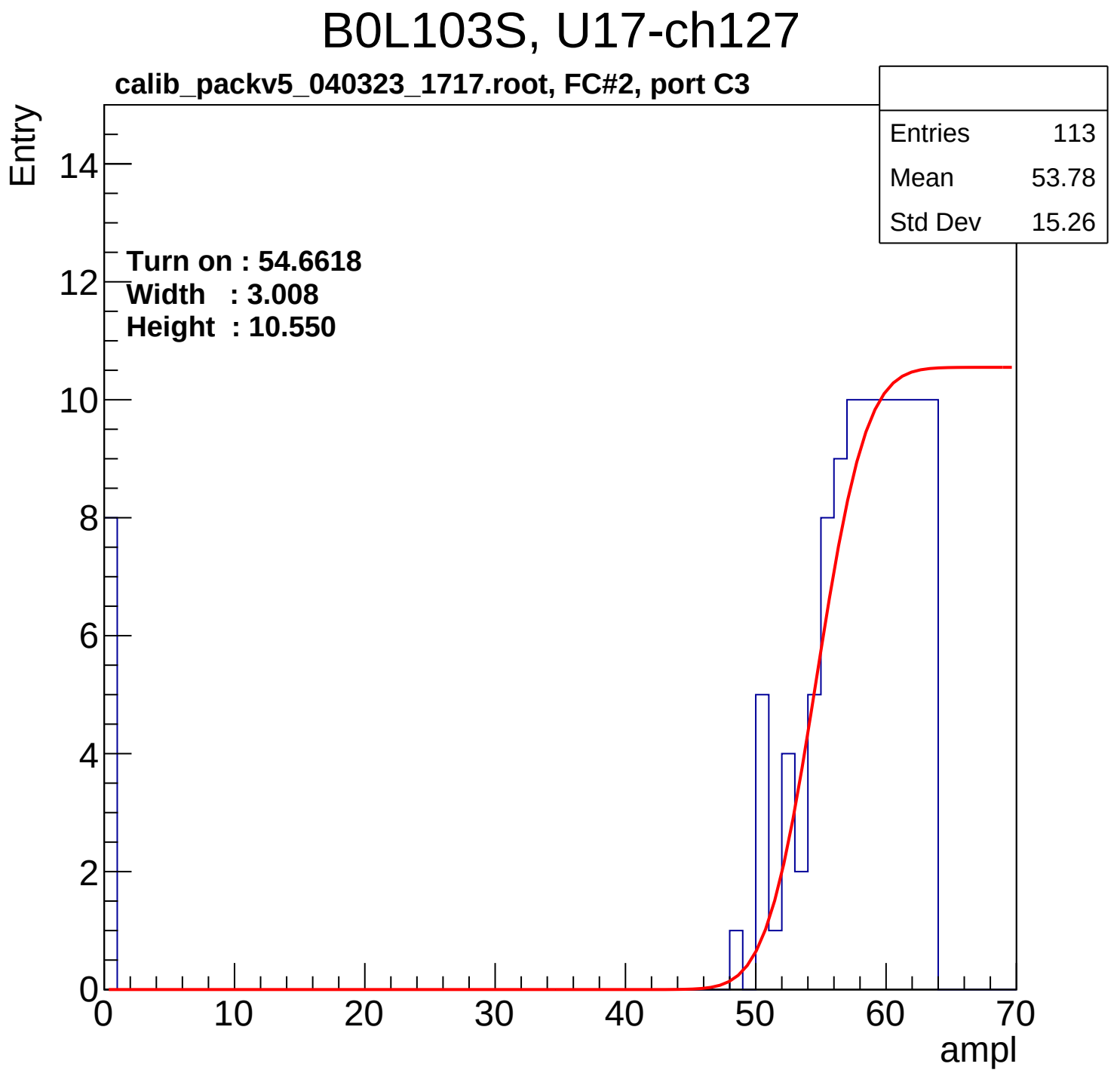
B0L103S, U17-ch127
calib_packv5_040323_1717.root, FC#2, port C3
Entries 113
Mean 53.78
Std Dev 15.26
Turn on : 54.6618
Width : 3.008
Height : 10.550
Entry
ampl
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12
14
0
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20
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