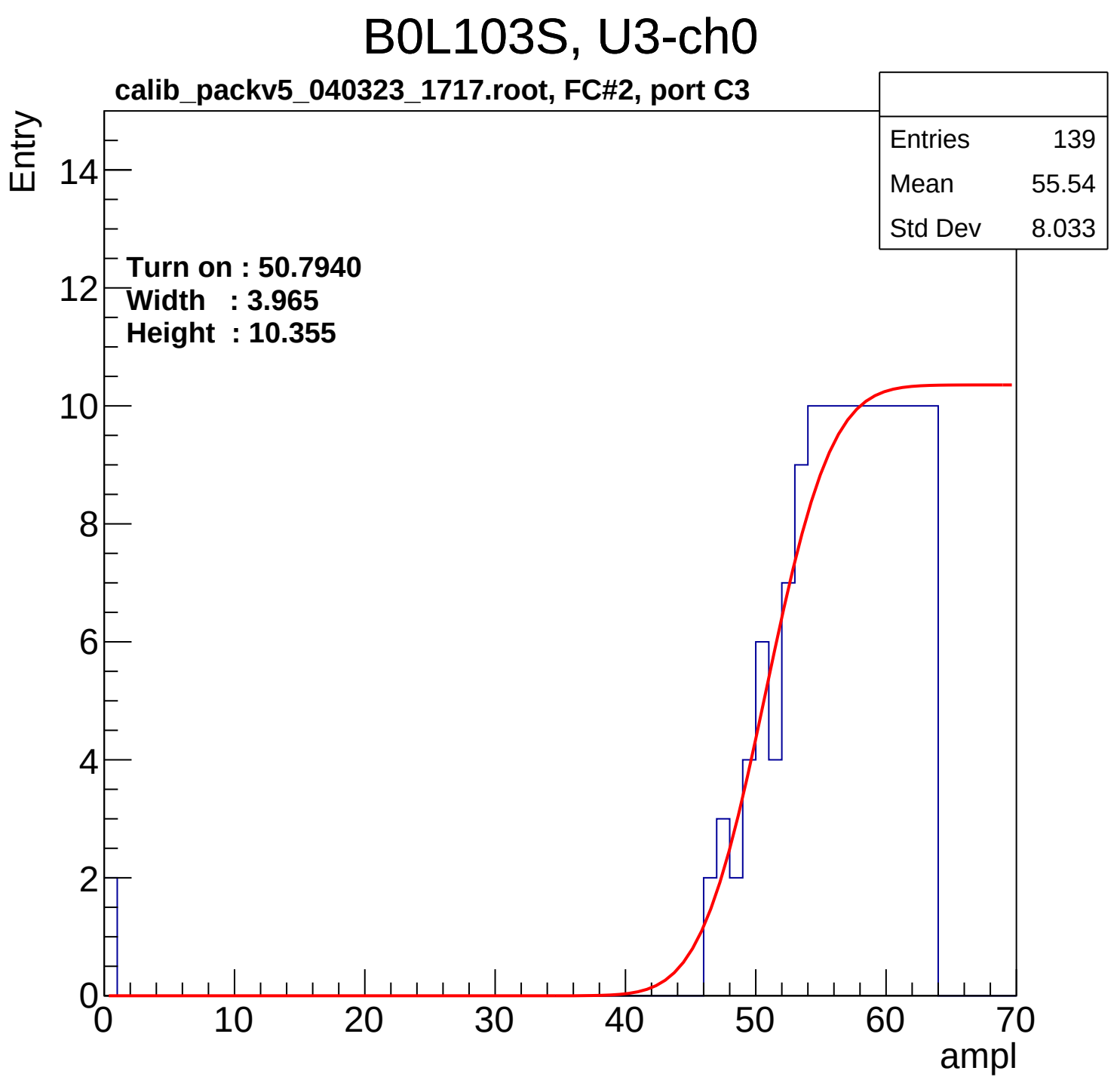
B0L103S, U3-ch0
calib_packv5_040323_1717.root, FC#2, port C3
Entries 139
Mean 55.54
Std Dev 8.033
Turn on : 50.7940
Width : 3.965
Height : 10.355
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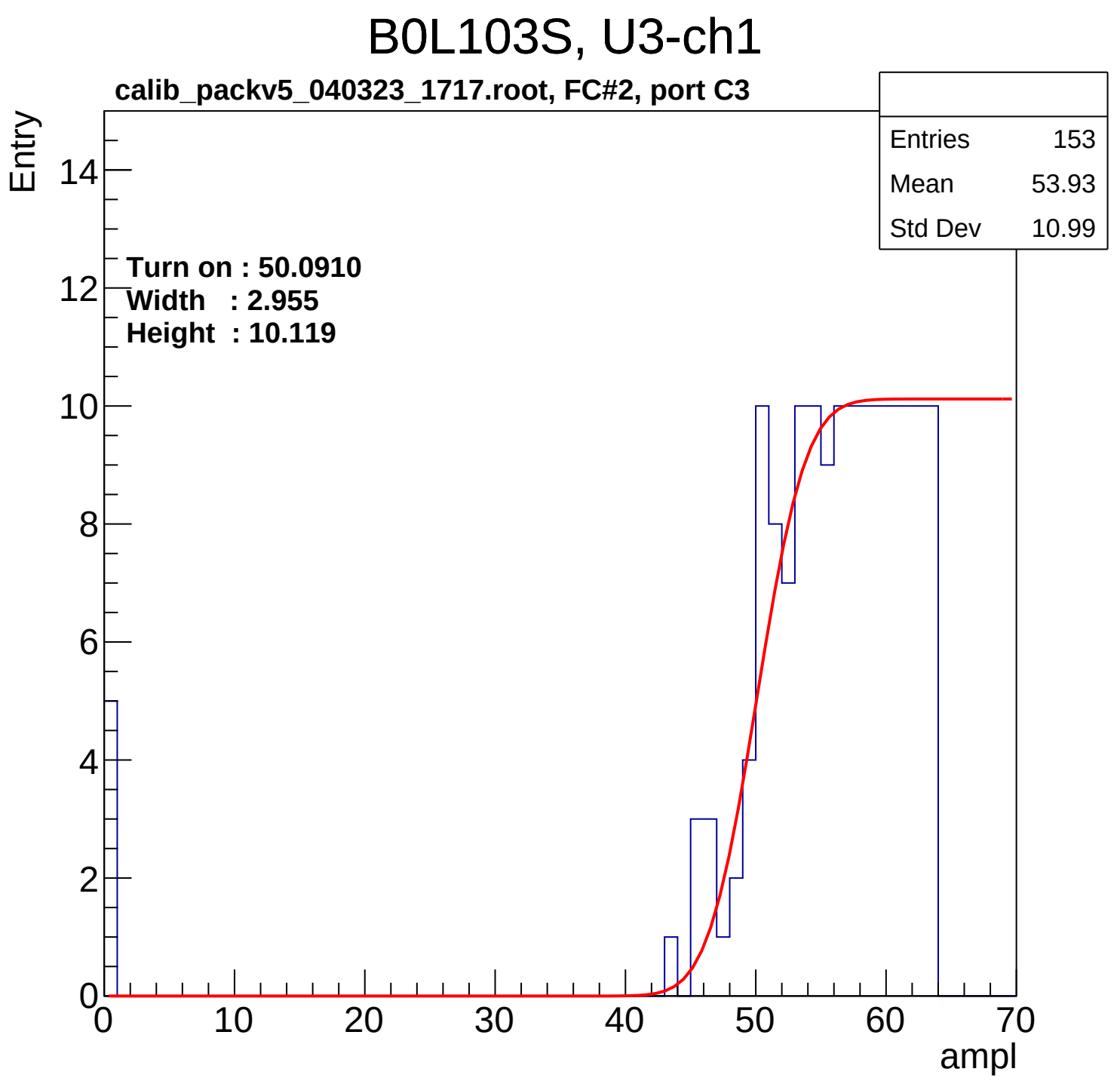
B0L103S, U3-ch1
calib_packv5_040323_1717.root, FC#2, port C3
Entries 153
Mean 53.93
Std Dev 10.99
Turn on : 50.0910
Width : 2.955
Height : 10.119
Entry
ampl
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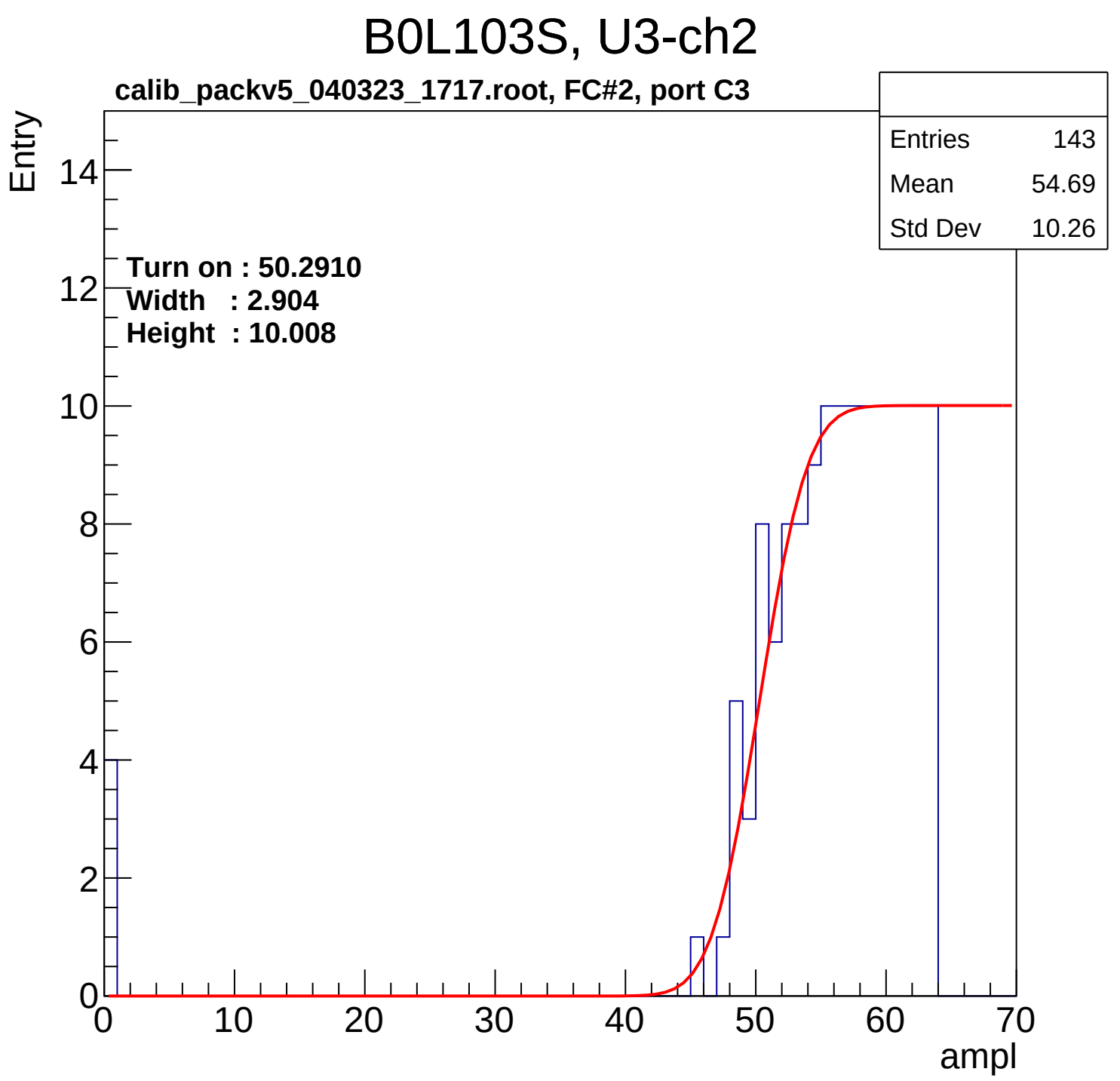
B0L103S, U3-ch2
calib_packv5_040323_1717.root, FC#2, port C3
Entries 143
Mean 54.69
Std Dev 10.26
Turn on : 50.2910
Width : 2.904
Height : 10.008
Entry
ampl
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4
6
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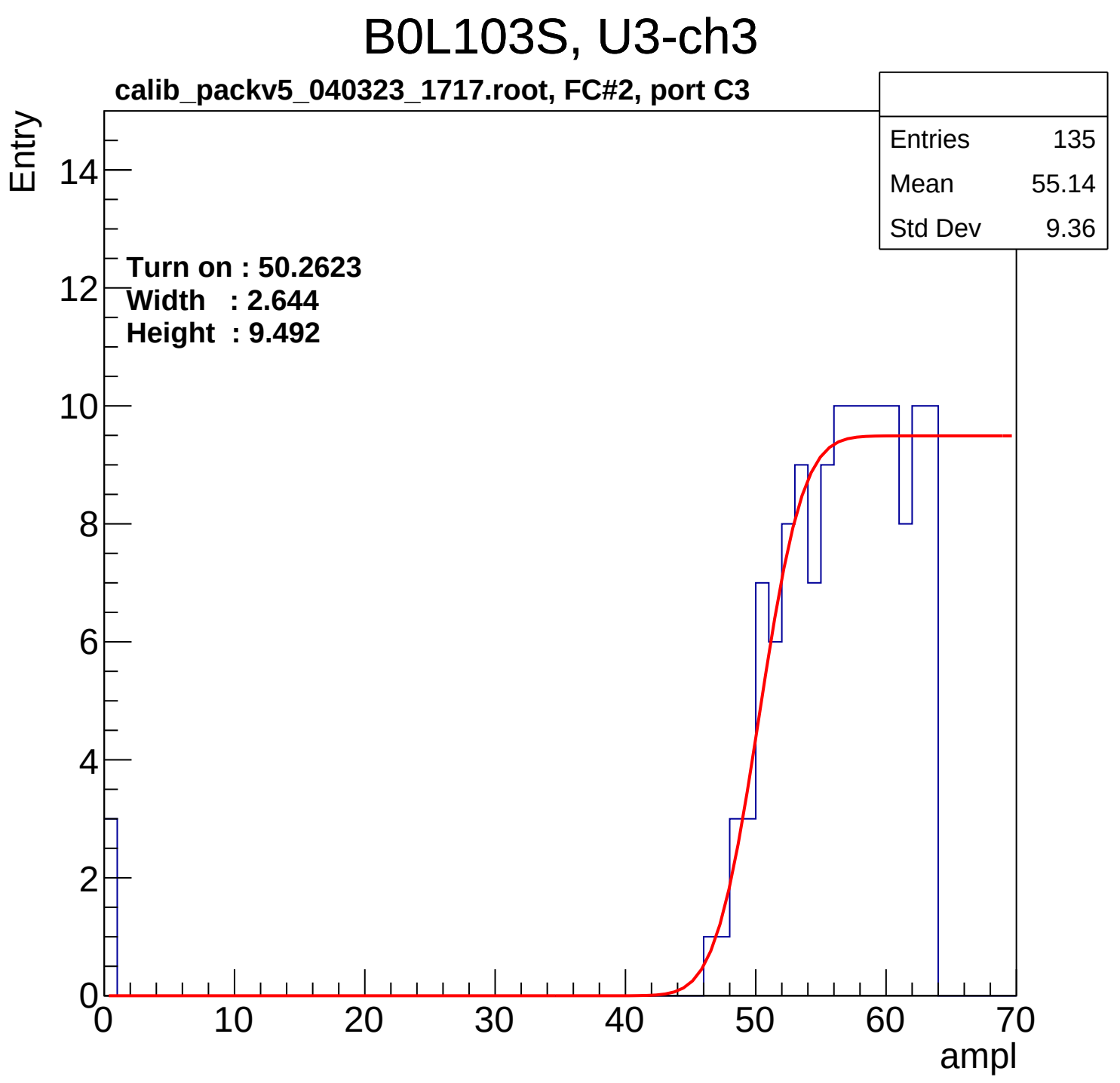
B0L103S, U3-ch3
calib_packv5_040323_1717.root, FC#2, port C3
Entries 135
Mean 55.14
Std Dev 9.36
Turn on : 50.2623
Width : 2.644
Height : 9.492
Entry
ampl
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6
8
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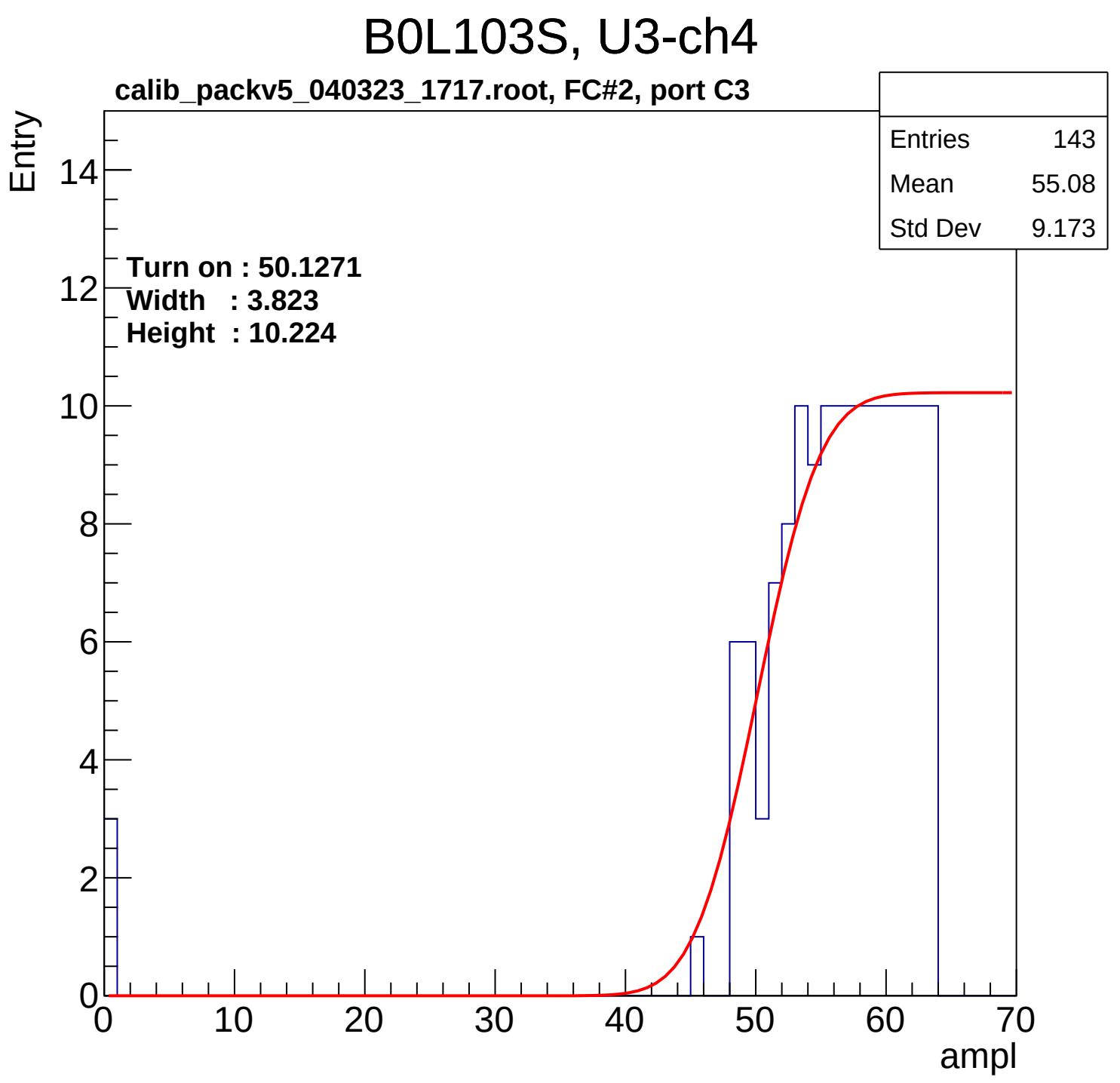
B0L103S, U3-ch4
calib_packv5_040323_1717.root, FC#2, port C3
Entries 143
Mean 55.08
Std Dev 9.173
Turn on : 50.1271
Width : 3.823
Height : 10.224
Entry
ampl
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2
4
6
8
10
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0
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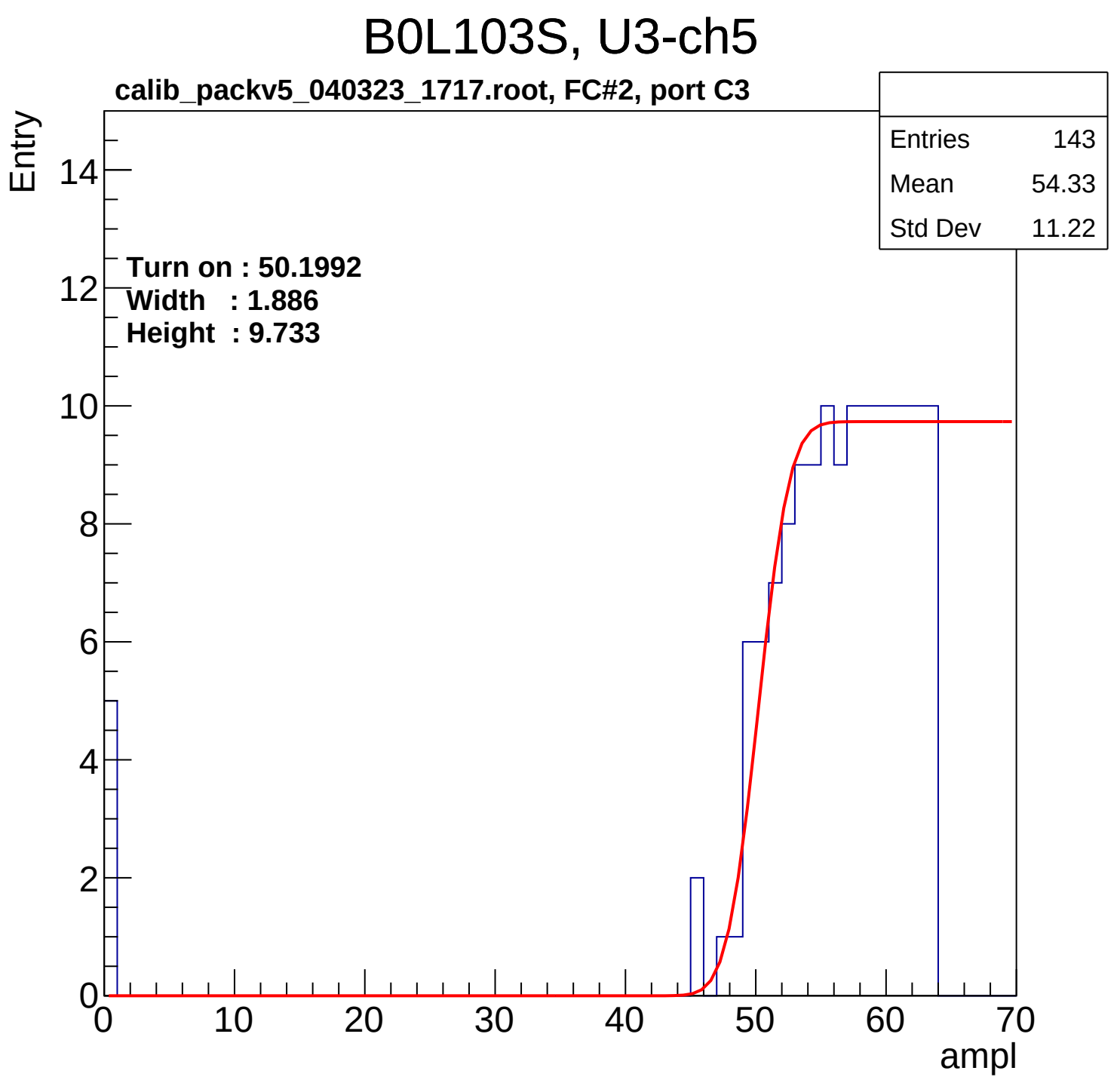
B0L103S, U3-ch5
calib_packv5_040323_1717.root, FC#2, port C3
Entries 143
Mean 54.33
Std Dev 11.22
Turn on : 50.1992
Width : 1.886
Height : 9.733
Entry
ampl
0
2
4
6
8
10
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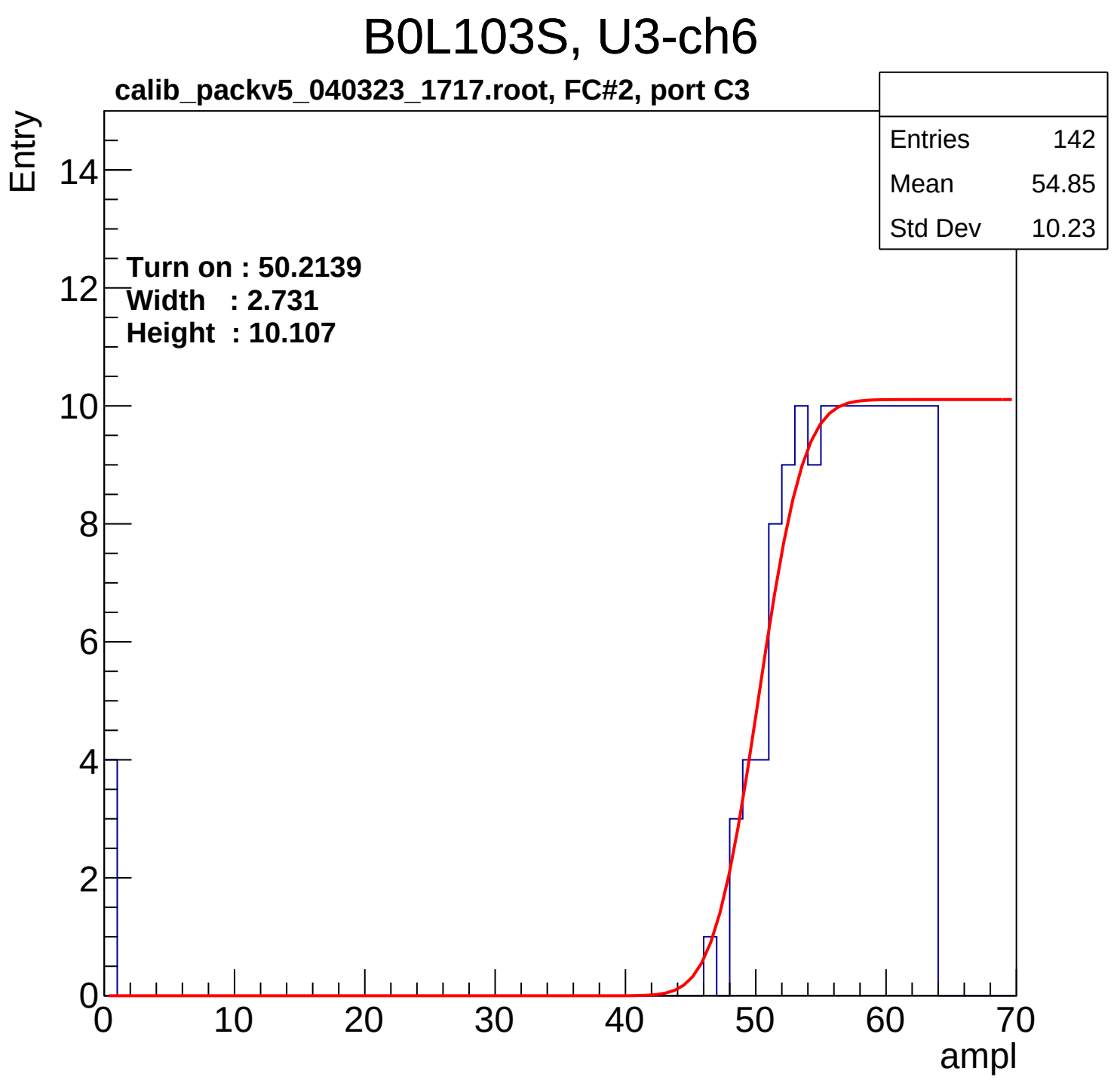
B0L103S, U3-ch6
calib_packv5_040323_1717.root, FC#2, port C3
Entries 142
Mean 54.85
Std Dev 10.23
Turn on : 50.2139
Width : 2.731
Height : 10.107
Entry
ampl
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2
4
6
8
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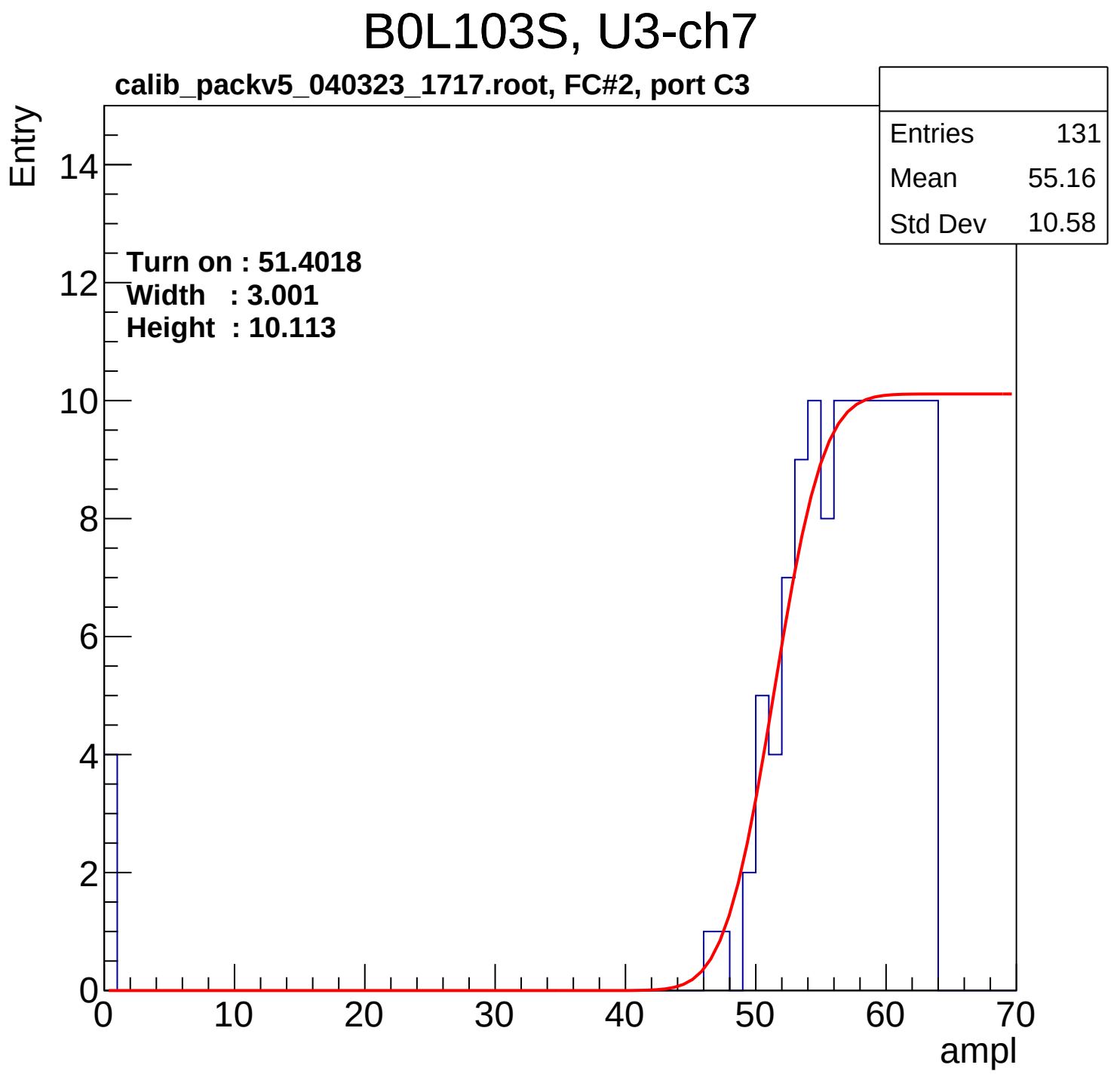
B0L103S, U3-ch7
calib_packv5_040323_1717.root, FC#2, port C3
Entries 131
Mean 55.16
Std Dev 10.58
Turn on : 51.4018
Width : 3.001
Height : 10.113
Entry
ampl
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2
4
6
8
10
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60
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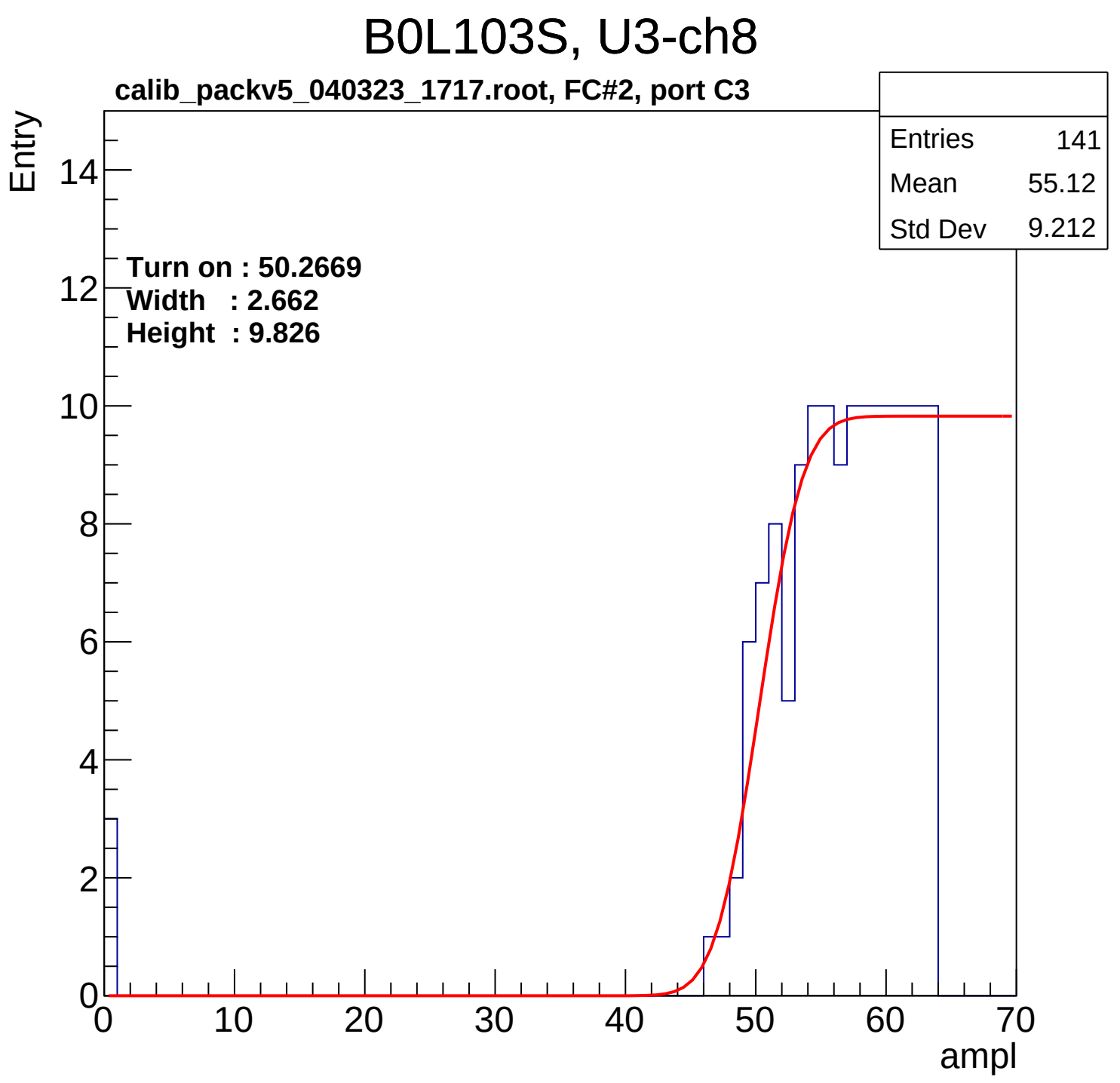
B0L103S, U3-ch8
calib_packv5_040323_1717.root, FC#2, port C3
Entries 141
Mean 55.12
Std Dev 9.212
Turn on : 50.2669
Width : 2.662
Height : 9.826
Entry
ampl
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8
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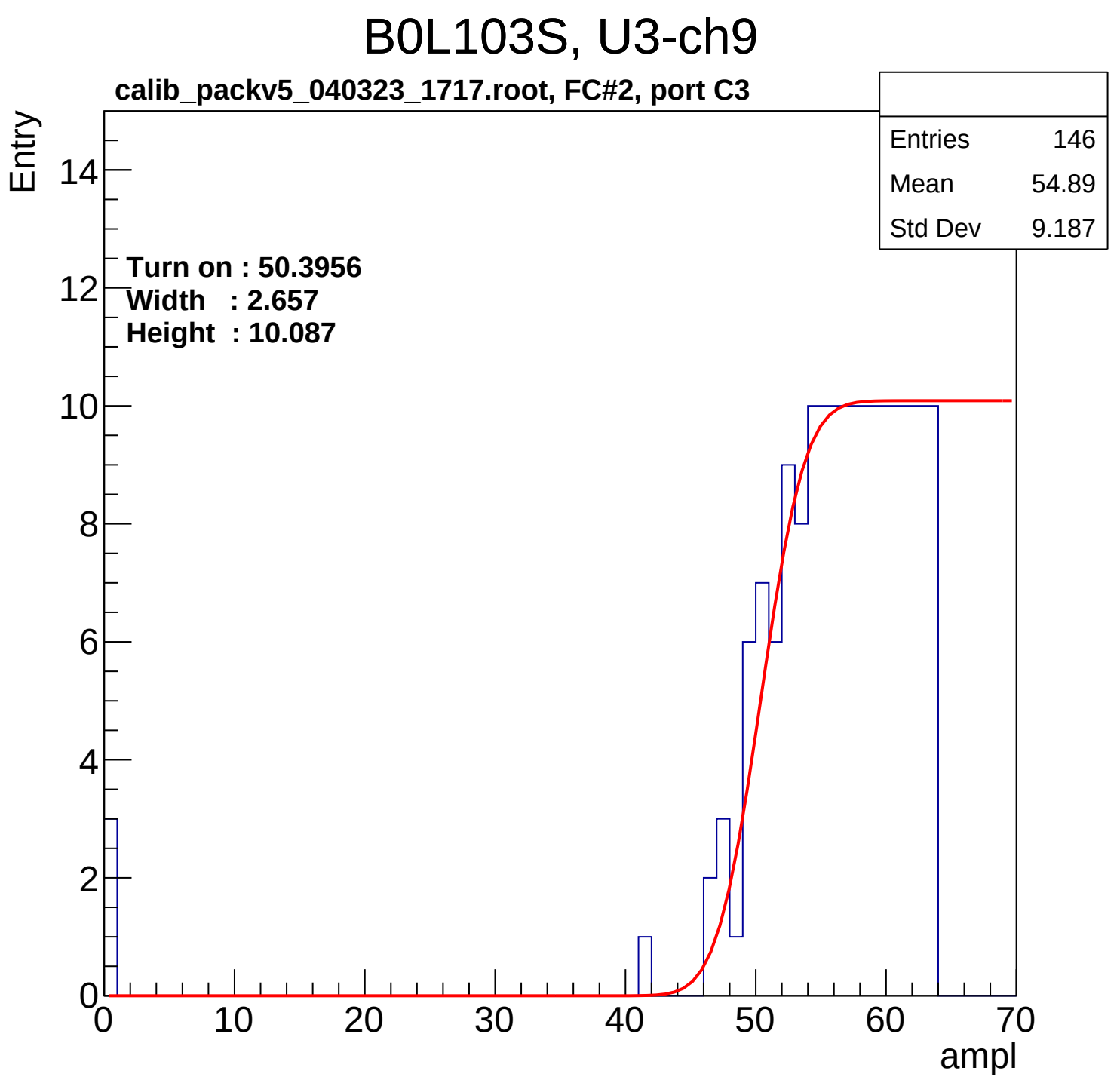
B0L103S, U3-ch9
calib_packv5_040323_1717.root, FC#2, port C3
Entries 146
Mean 54.89
Std Dev 9.187
Turn on : 50.3956
Width : 2.657
Height : 10.087
Entry
ampl
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2
4
6
8
10
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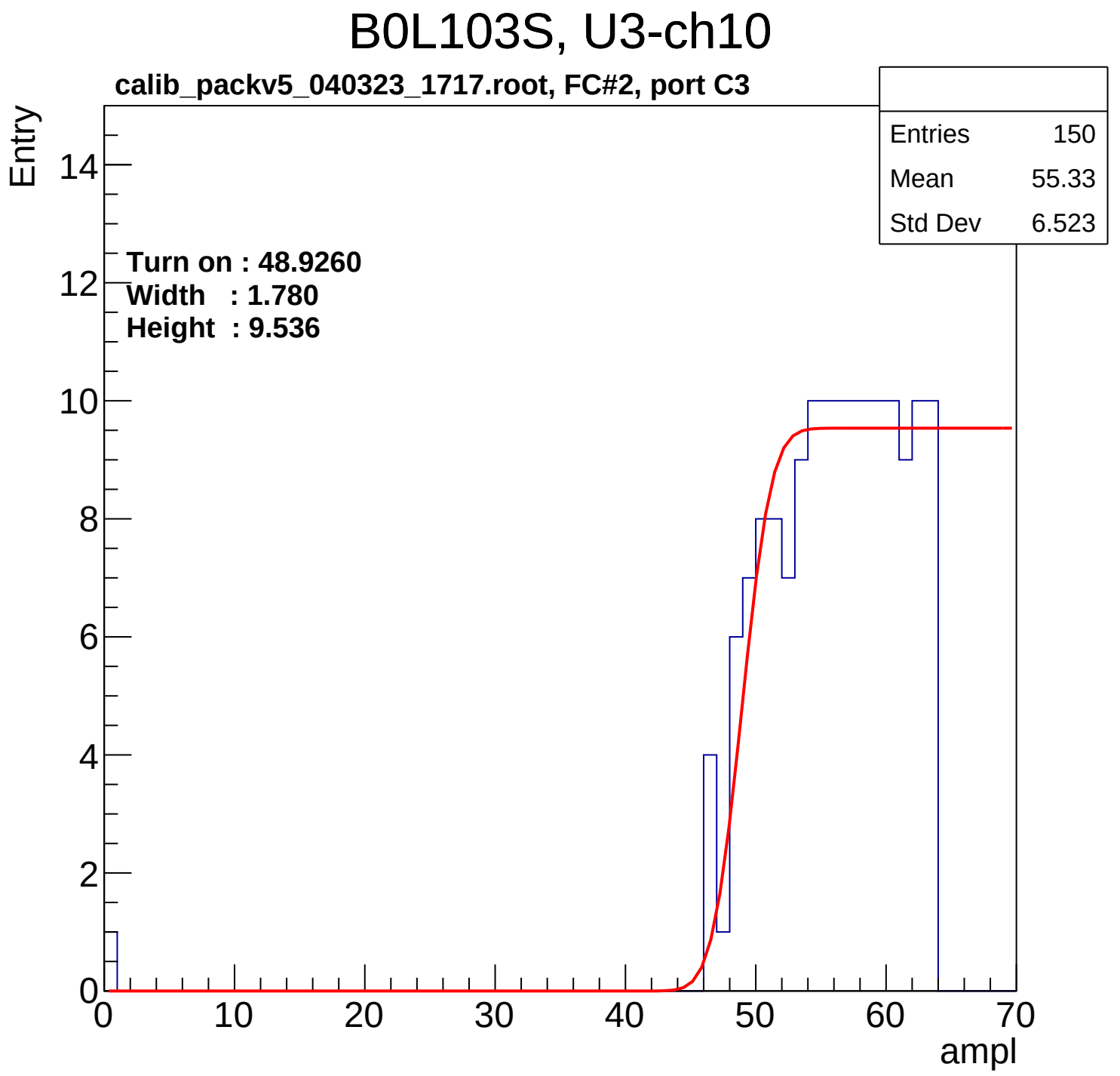
B0L103S, U3-ch10
calib_packv5_040323_1717.root, FC#2, port C3
Entries 150
Mean 55.33
Std Dev 6.523
Turn on : 48.9260
Width : 1.780
Height : 9.536
Entry
ampl
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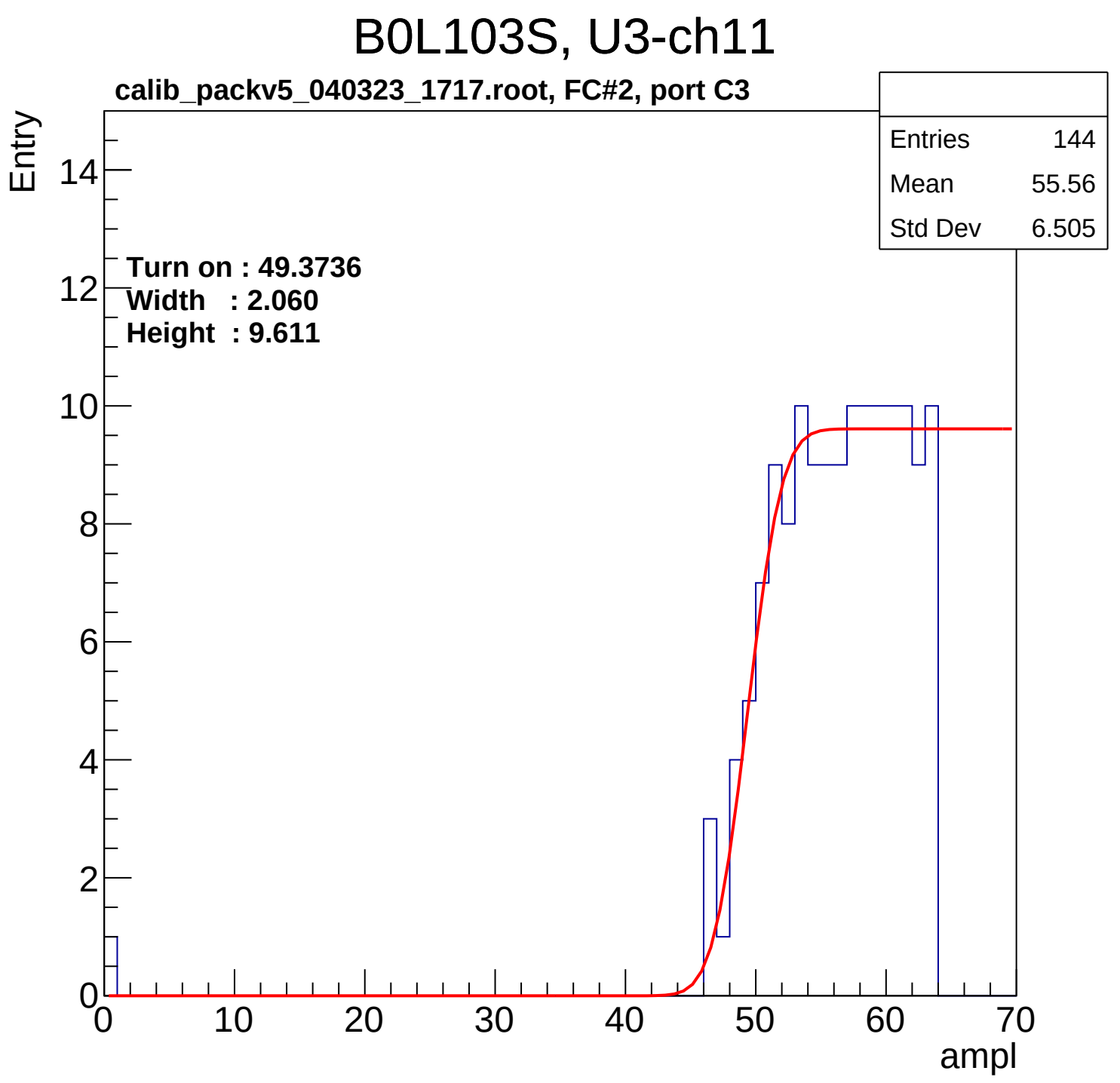
B0L103S, U3-ch11
calib_packv5_040323_1717.root, FC#2, port C3
Entries 144
Mean 55.56
Std Dev 6.505
Turn on : 49.3736
Width : 2.060
Height : 9.611
Entry
ampl
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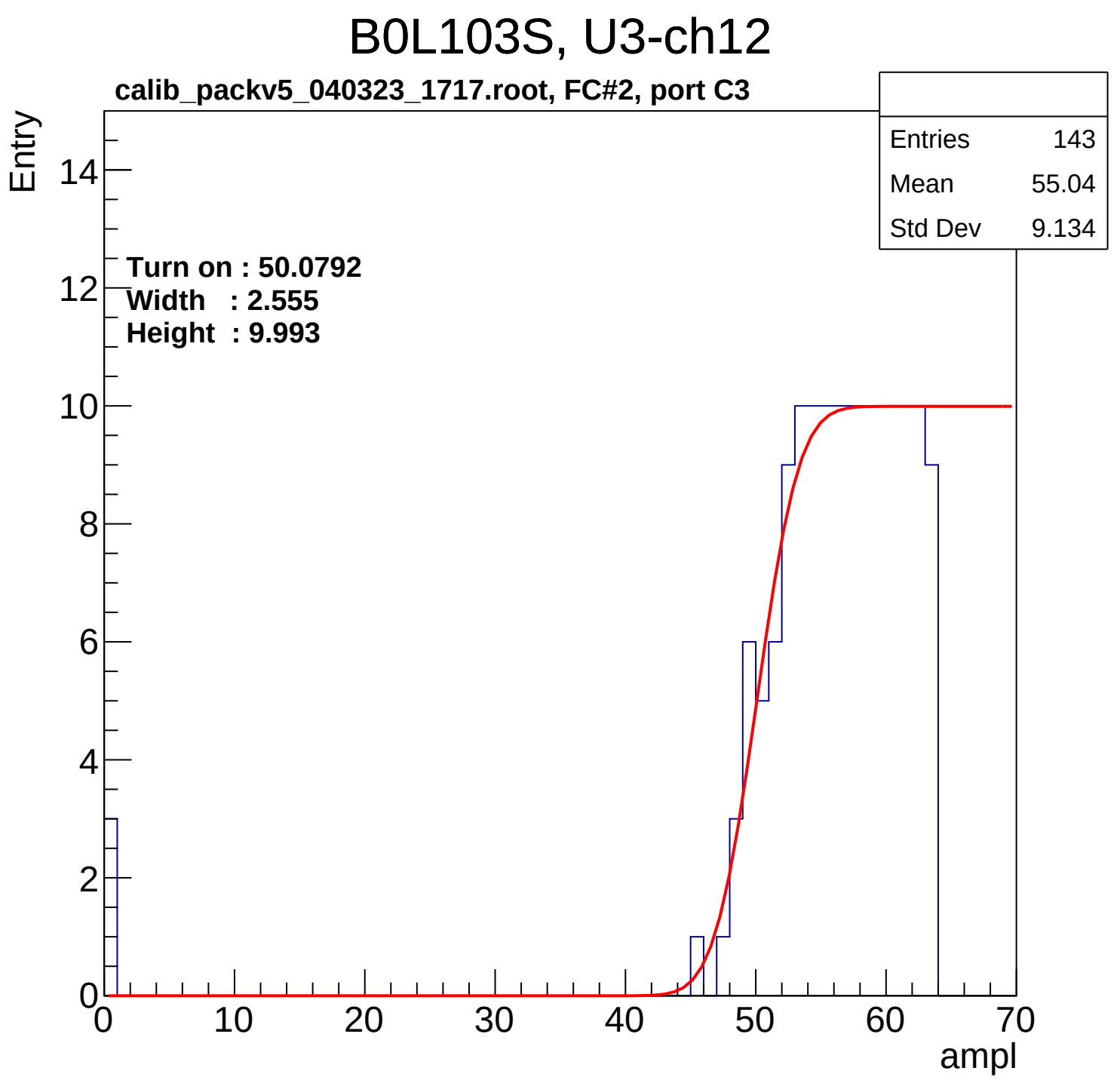
B0L103S, U3-ch12
calib_packv5_040323_1717.root, FC#2, port C3
Entries 143
Mean 55.04
Std Dev 9.134
Turn on : 50.0792
Width : 2.555
Height : 9.993
Entry
ampl
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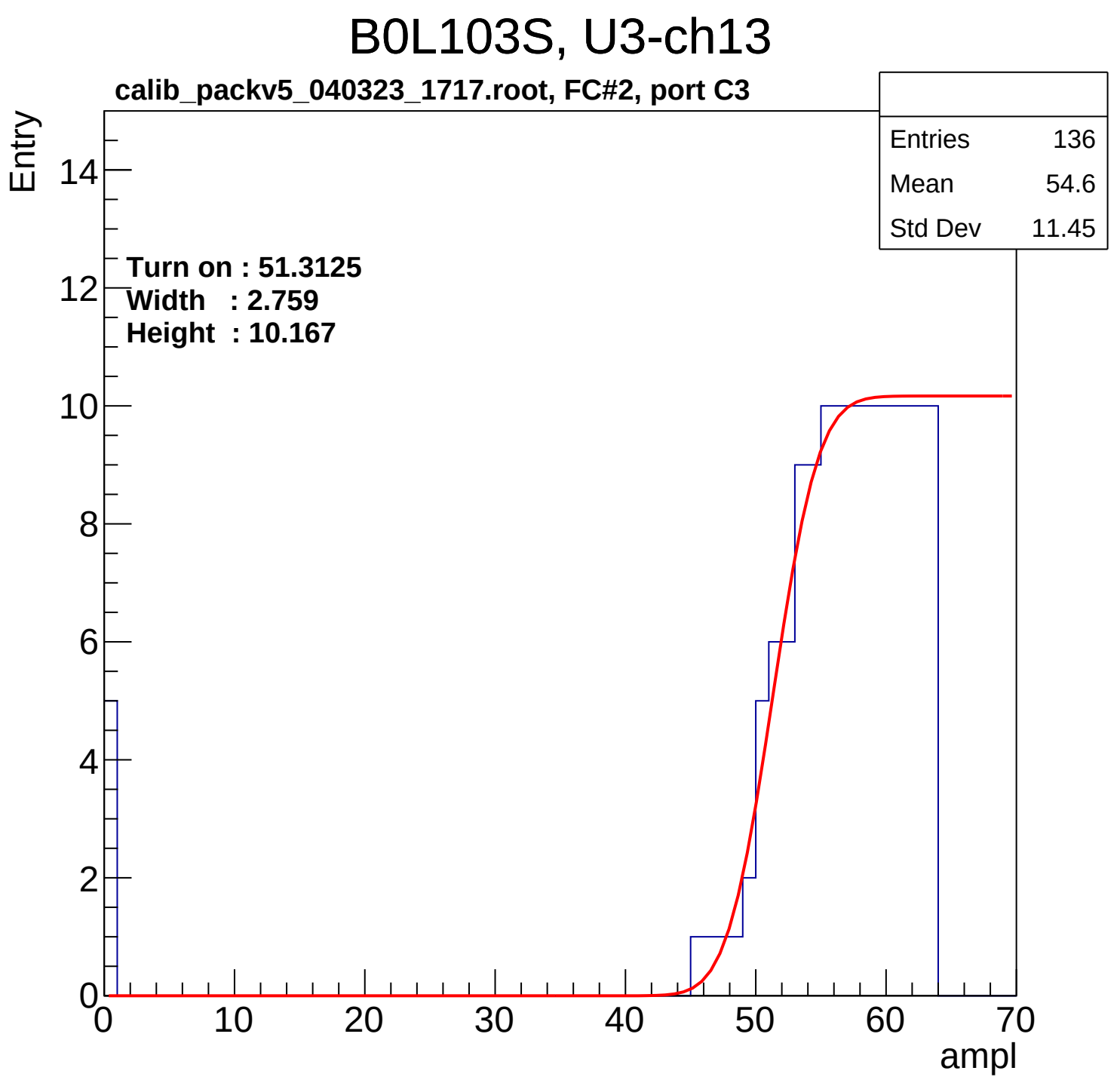
B0L103S, U3-ch13
calib_packv5_040323_1717.root, FC#2, port C3
Entries 136
Mean 54.6
Std Dev 11.45
Turn on : 51.3125
Width : 2.759
Height : 10.167
Entry
ampl
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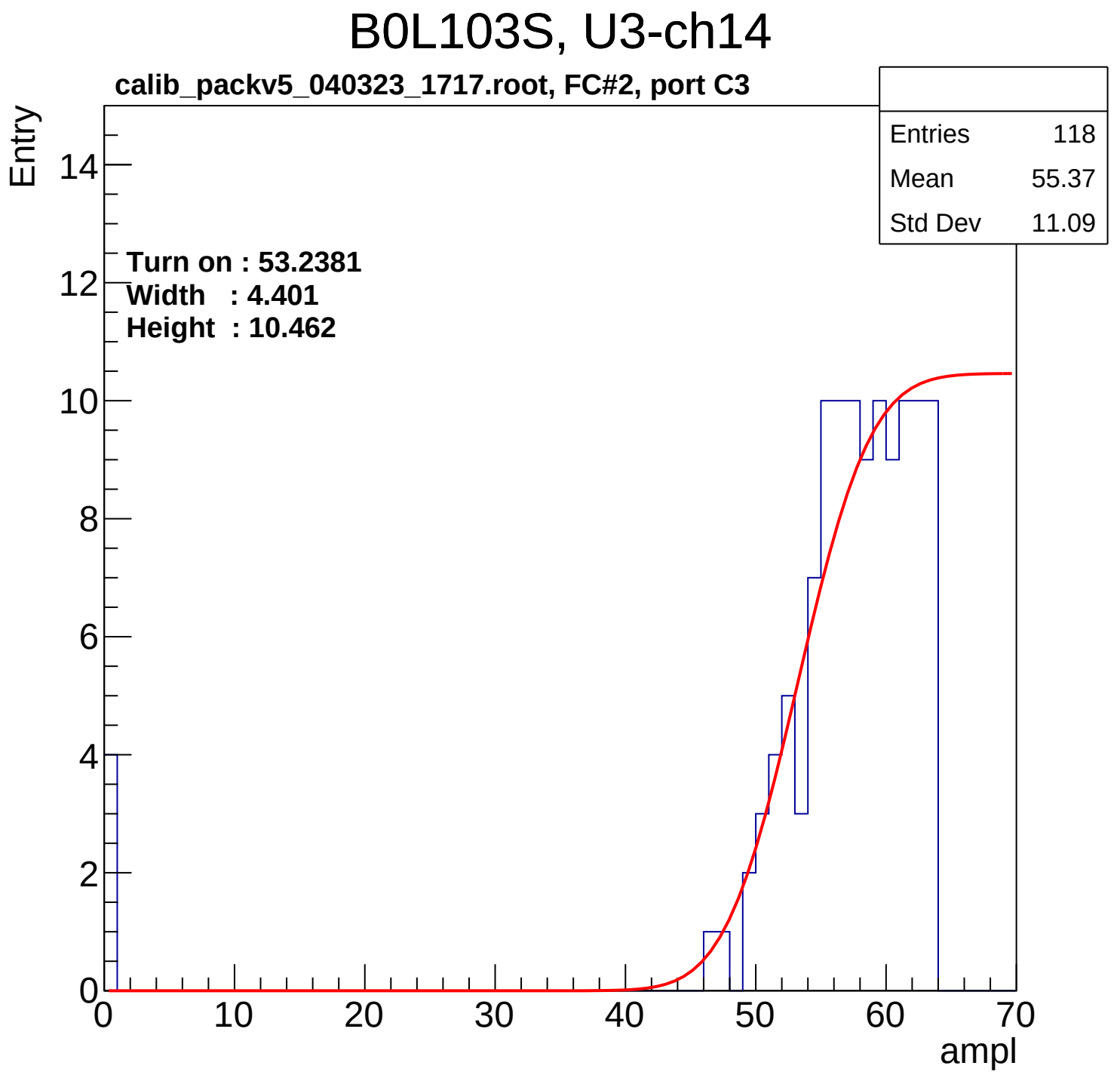
B0L103S, U3-ch14
calib_packv5_040323_1717.root, FC#2, port C3
Entries 118
Mean 55.37
Std Dev 11.09
Turn on : 53.2381
Width : 4.401
Height : 10.462
Entry
ampl
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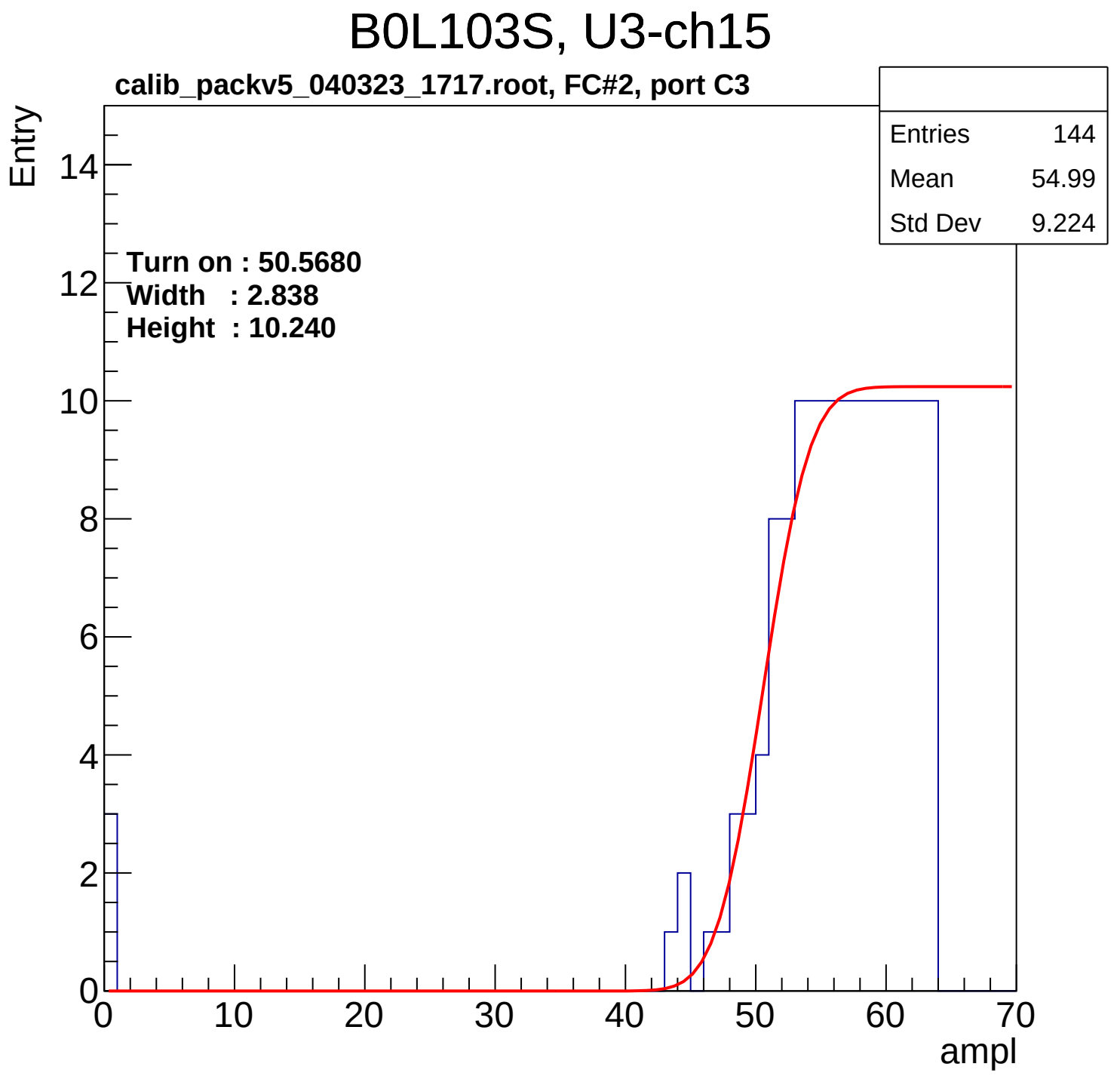
B0L103S, U3-ch15
calib_packv5_040323_1717.root, FC#2, port C3
Entries 144
Mean 54.99
Std Dev 9.224
Turn on : 50.5680
Width : 2.838
Height : 10.240
Entry
ampl
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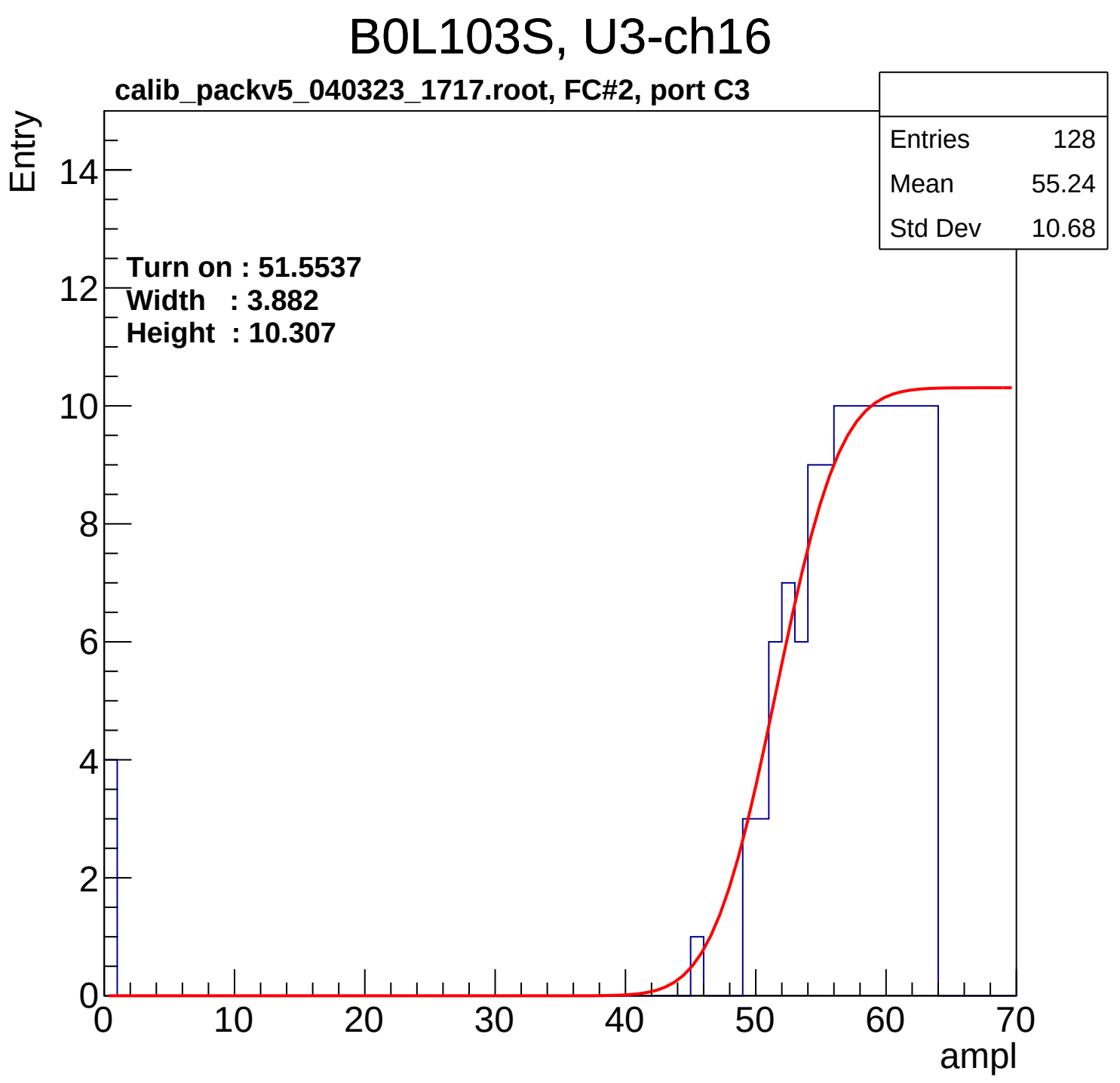
B0L103S, U3-ch16
calib_packv5_040323_1717.root, FC#2, port C3
Entries 128
Mean 55.24
Std Dev 10.68
Turn on : 51.5537
Width : 3.882
Height : 10.307
Entry
ampl
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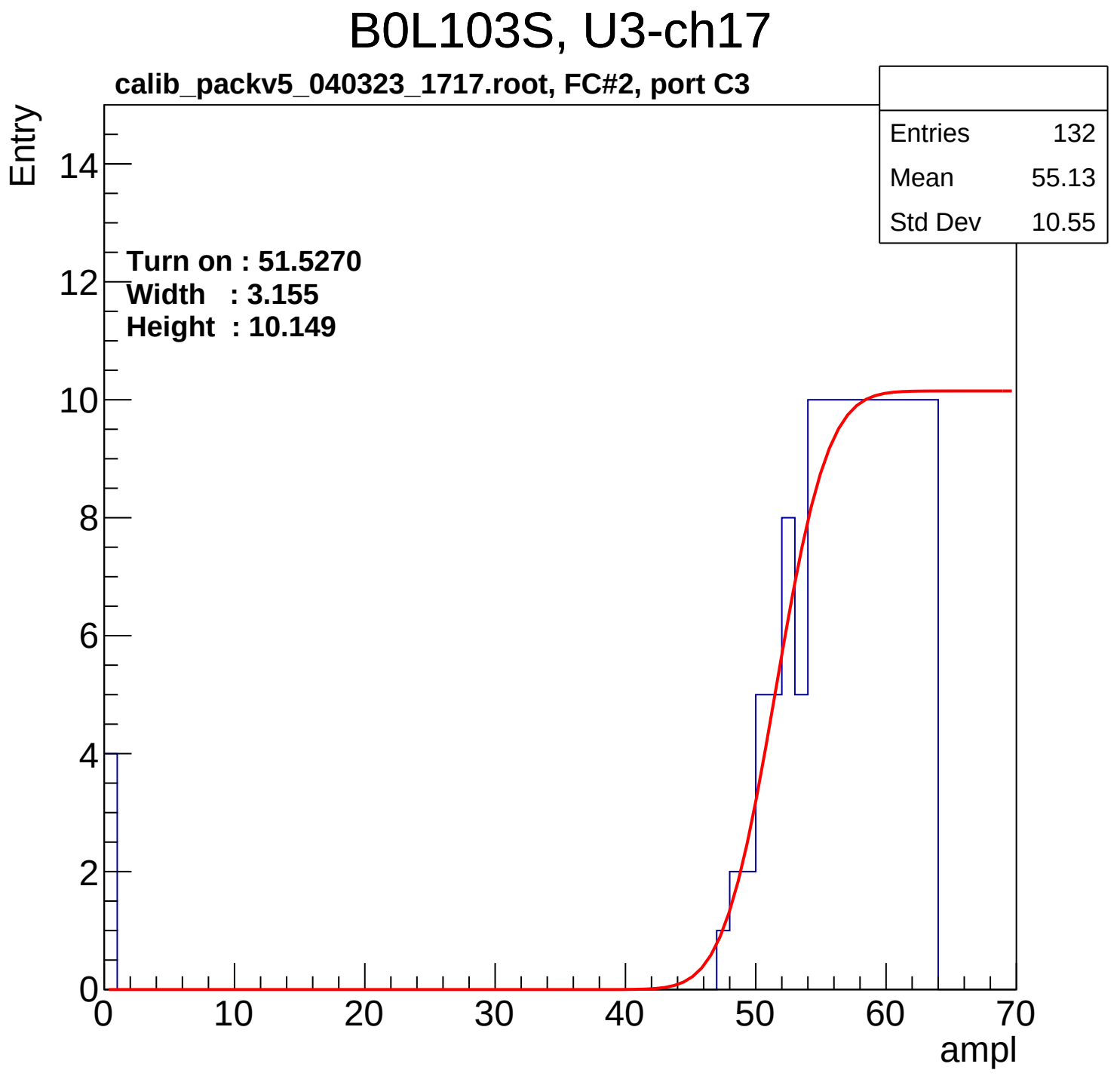
B0L103S, U3-ch17
calib_packv5_040323_1717.root, FC#2, port C3
Entries 132
Mean 55.13
Std Dev 10.55
Turn on : 51.5270
Width : 3.155
Height : 10.149
Entry
ampl
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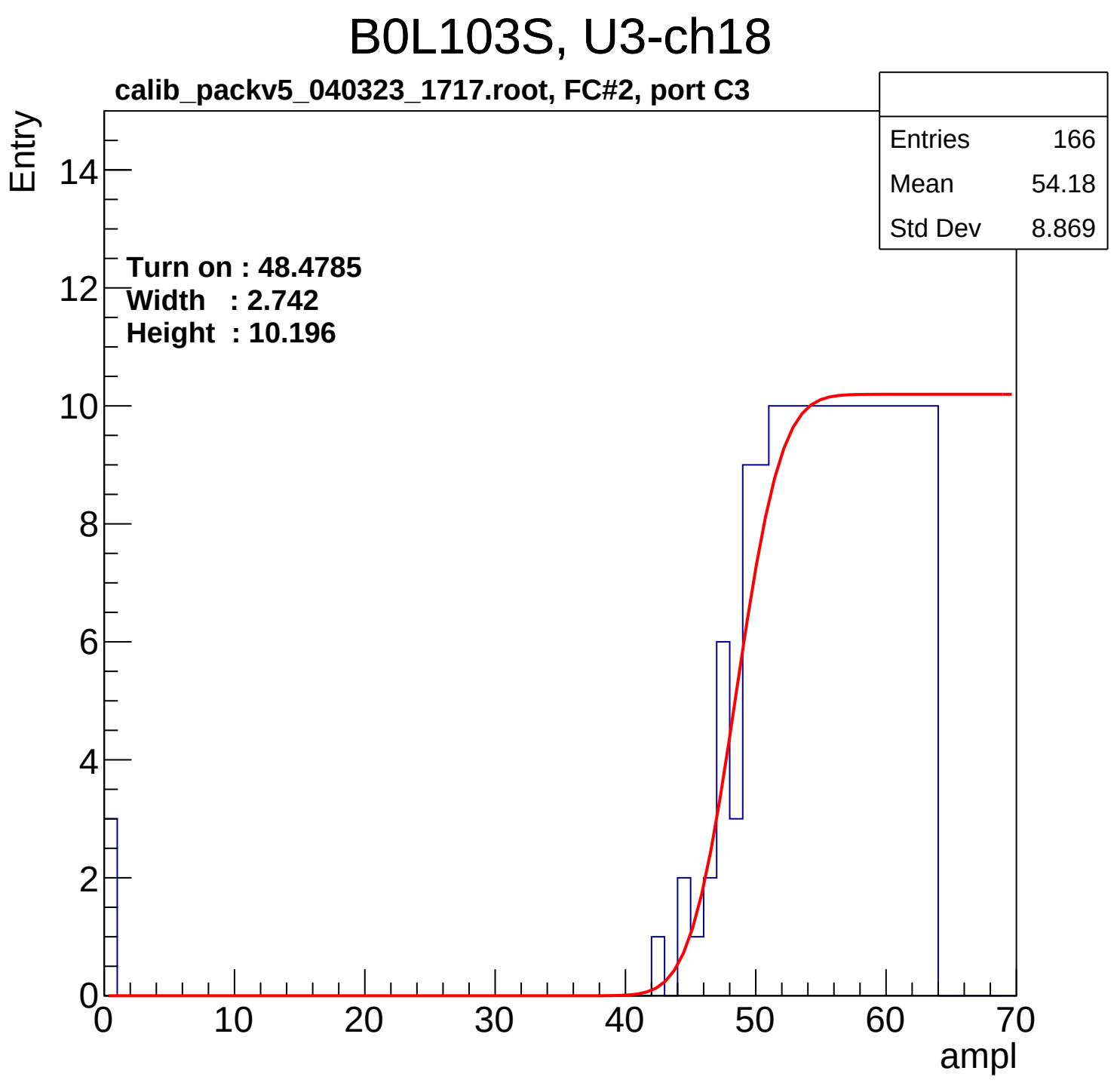
B0L103S, U3-ch18
calib_packv5_040323_1717.root, FC#2, port C3
Entries 166
Mean 54.18
Std Dev 8.869
Turn on : 48.4785
Width : 2.742
Height : 10.196
Entry
ampl
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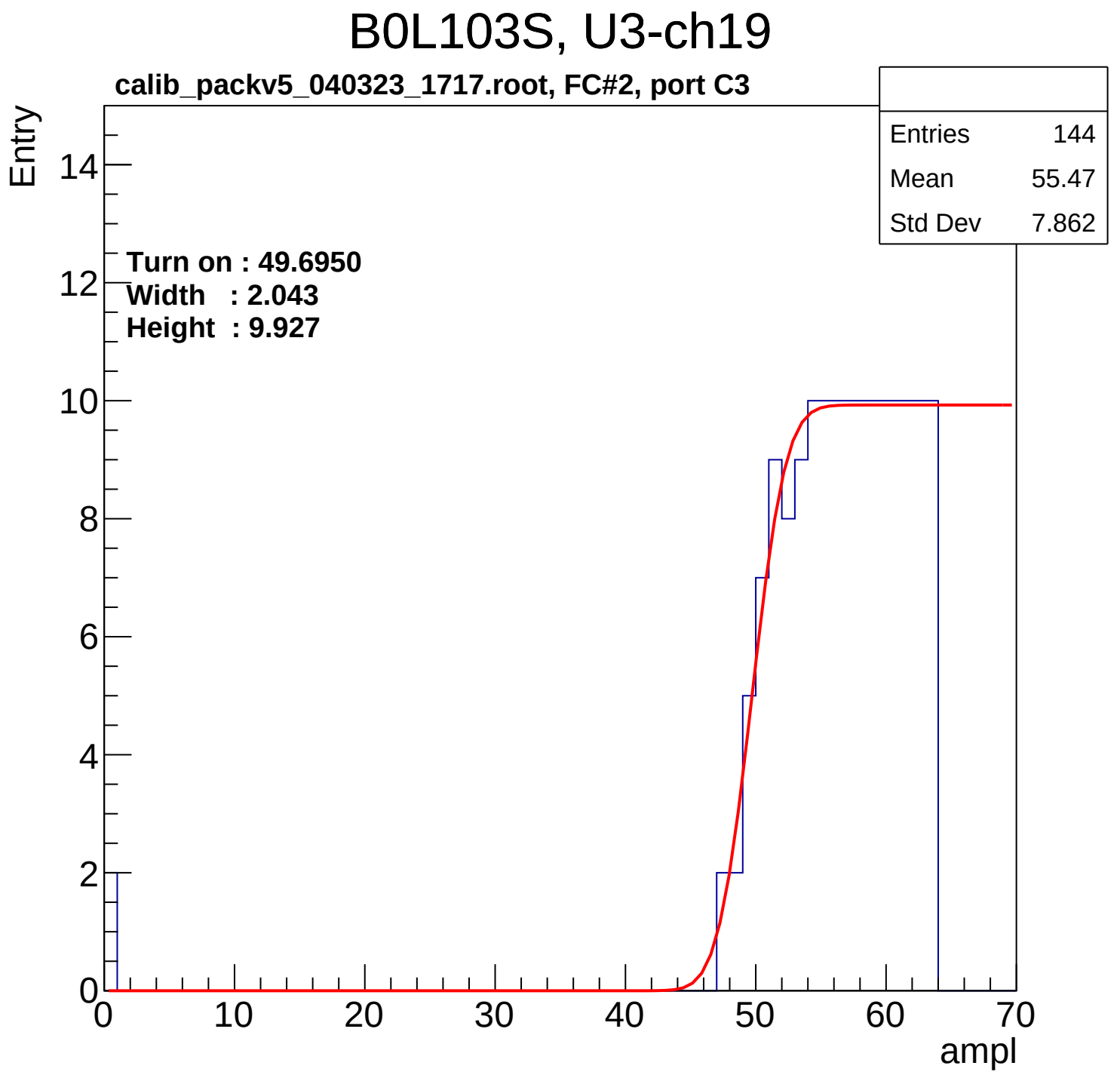
B0L103S, U3-ch19
calib_packv5_040323_1717.root, FC#2, port C3
Entries 144
Mean 55.47
Std Dev 7.862
Turn on : 49.6950
Width : 2.043
Height : 9.927
Entry
ampl
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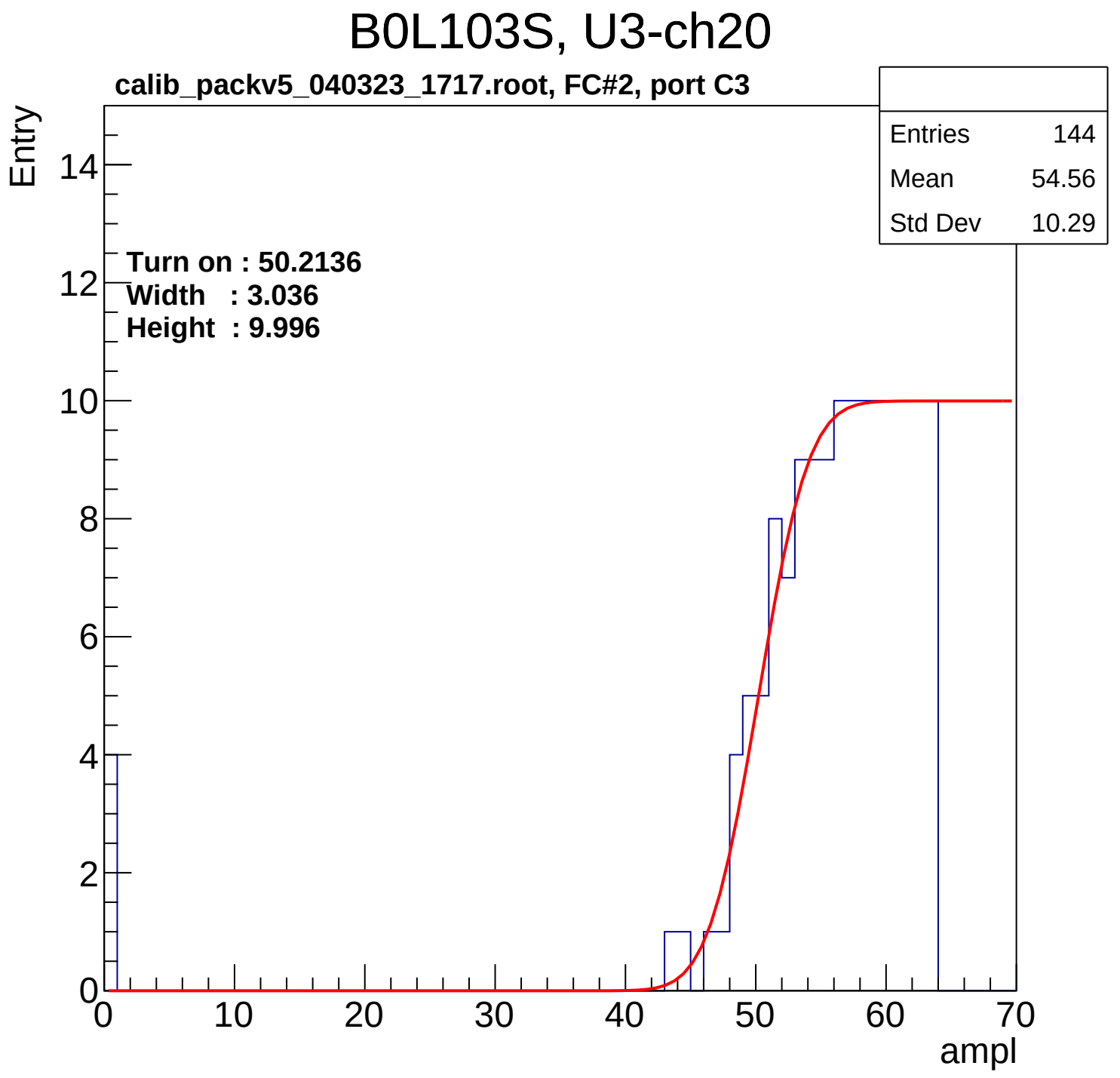
B0L103S, U3-ch20
calib_packv5_040323_1717.root, FC#2, port C3
Entries 144
Mean 54.56
Std Dev 10.29
Turn on : 50.2136
Width : 3.036
Height : 9.996
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ampl
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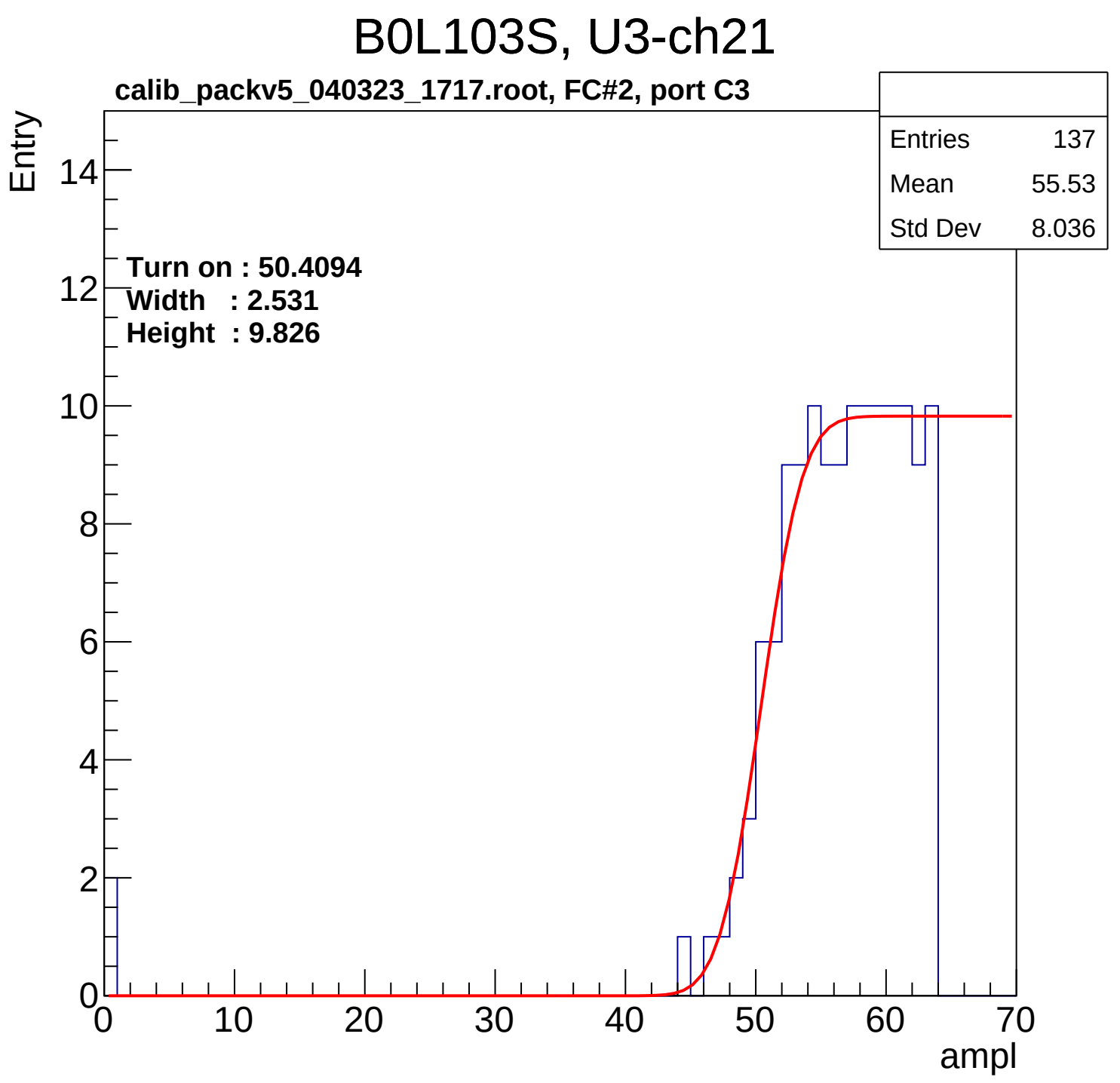
B0L103S, U3-ch21
calib_packv5_040323_1717.root, FC#2, port C3
Entries 137
Mean 55.53
Std Dev 8.036
Turn on : 50.4094
Width : 2.531
Height : 9.826
Entry
ampl
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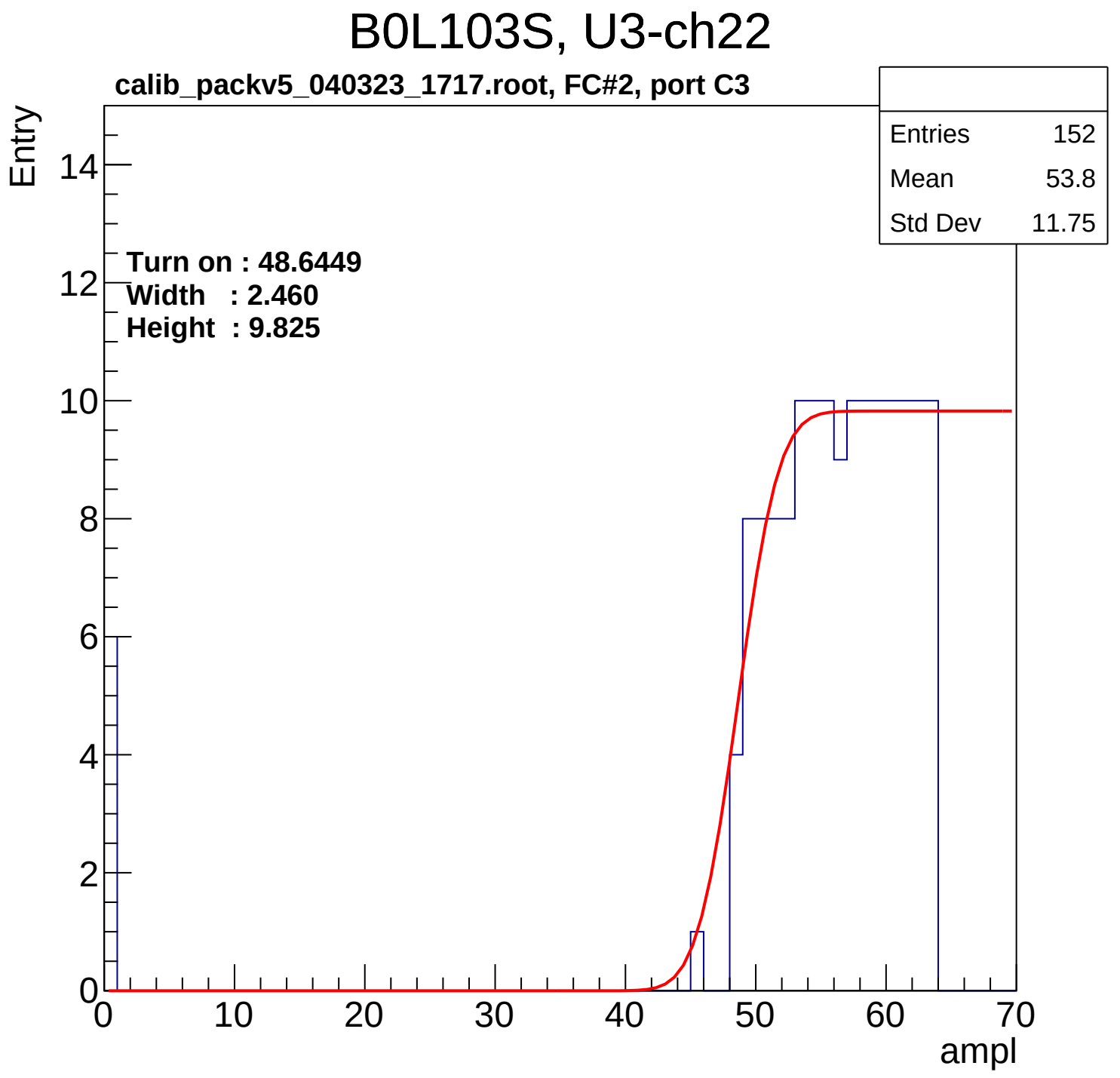
B0L103S, U3-ch22
calib_packv5_040323_1717.root, FC#2, port C3
Entries 152
Mean 53.8
Std Dev 11.75
Turn on : 48.6449
Width : 2.460
Height : 9.825
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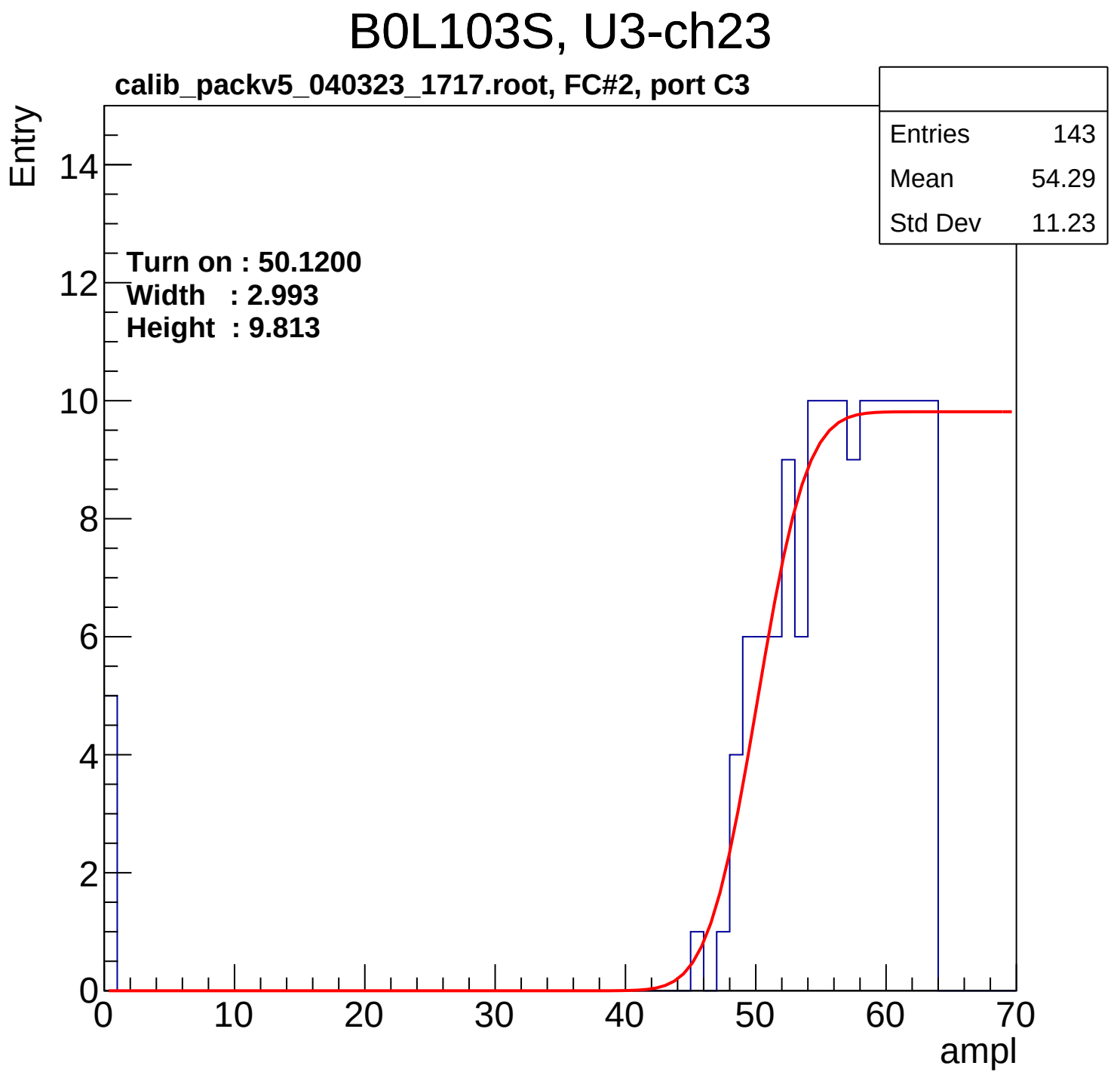
B0L103S, U3-ch23
calib_packv5_040323_1717.root, FC#2, port C3
Entries 143
Mean 54.29
Std Dev 11.23
Turn on : 50.1200
Width : 2.993
Height : 9.813
Entry
ampl
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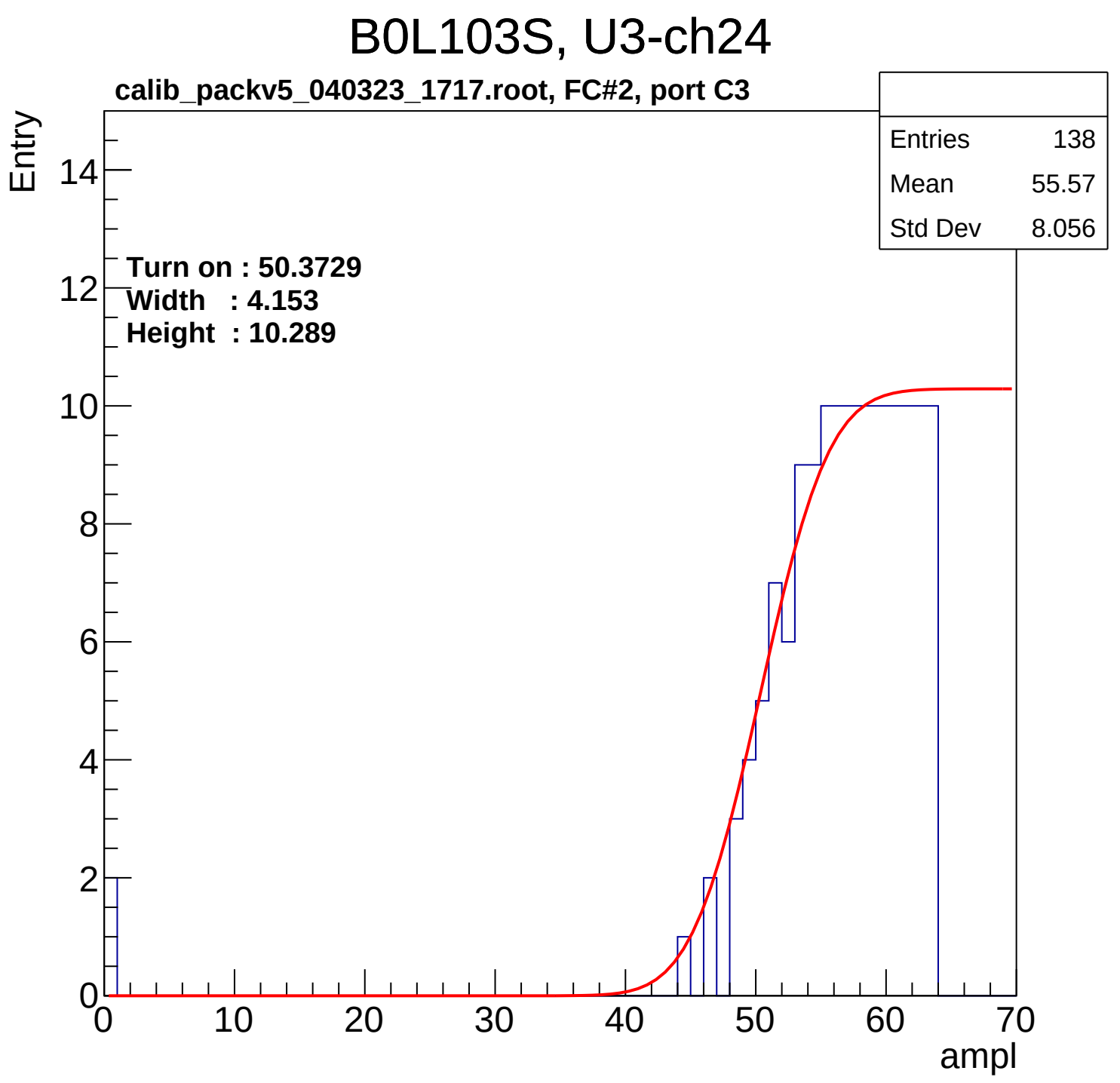
B0L103S, U3-ch24
calib_packv5_040323_1717.root, FC#2, port C3
Entries 138
Mean 55.57
Std Dev 8.056
Turn on : 50.3729
Width : 4.153
Height : 10.289
Entry
ampl
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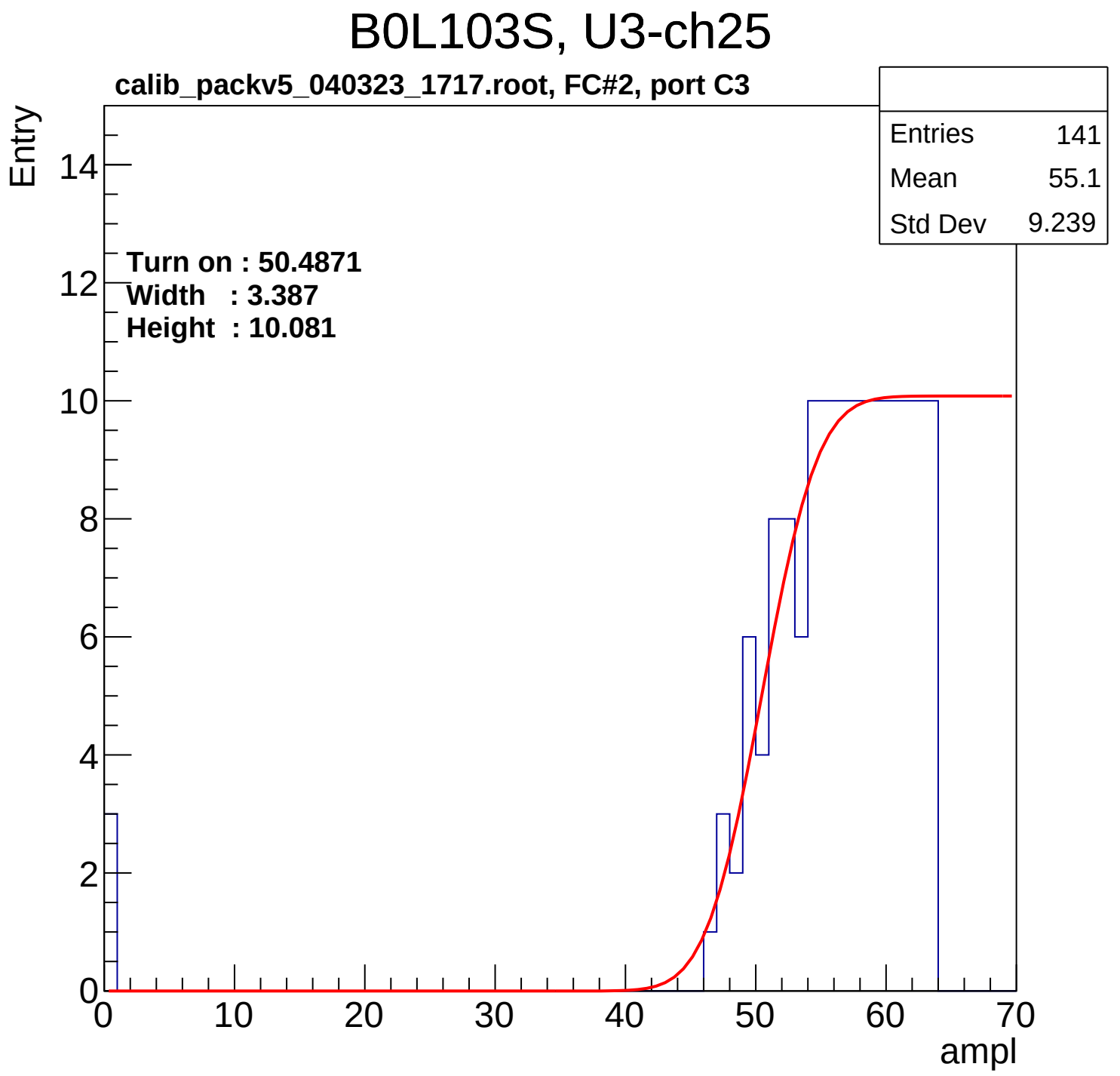
B0L103S, U3-ch25
calib_packv5_040323_1717.root, FC#2, port C3
Entries 141
Mean 55.1
Std Dev 9.239
Turn on : 50.4871
Width : 3.387
Height : 10.081
Entry
ampl
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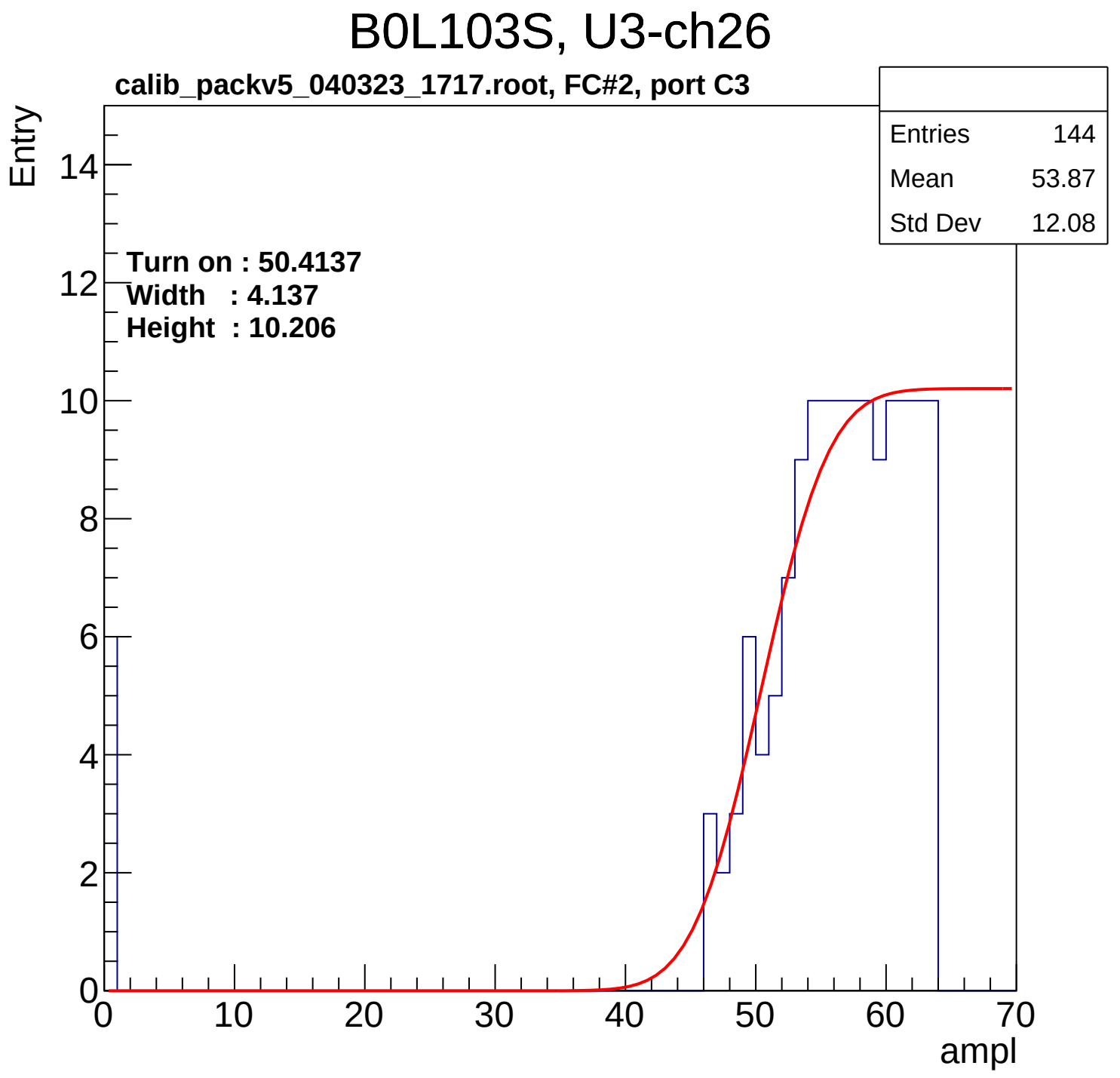
B0L103S, U3-ch26
calib_packv5_040323_1717.root, FC#2, port C3
Entries 144
Mean 53.87
Std Dev 12.08
Turn on : 50.4137
Width : 4.137
Height : 10.206
Entry
ampl
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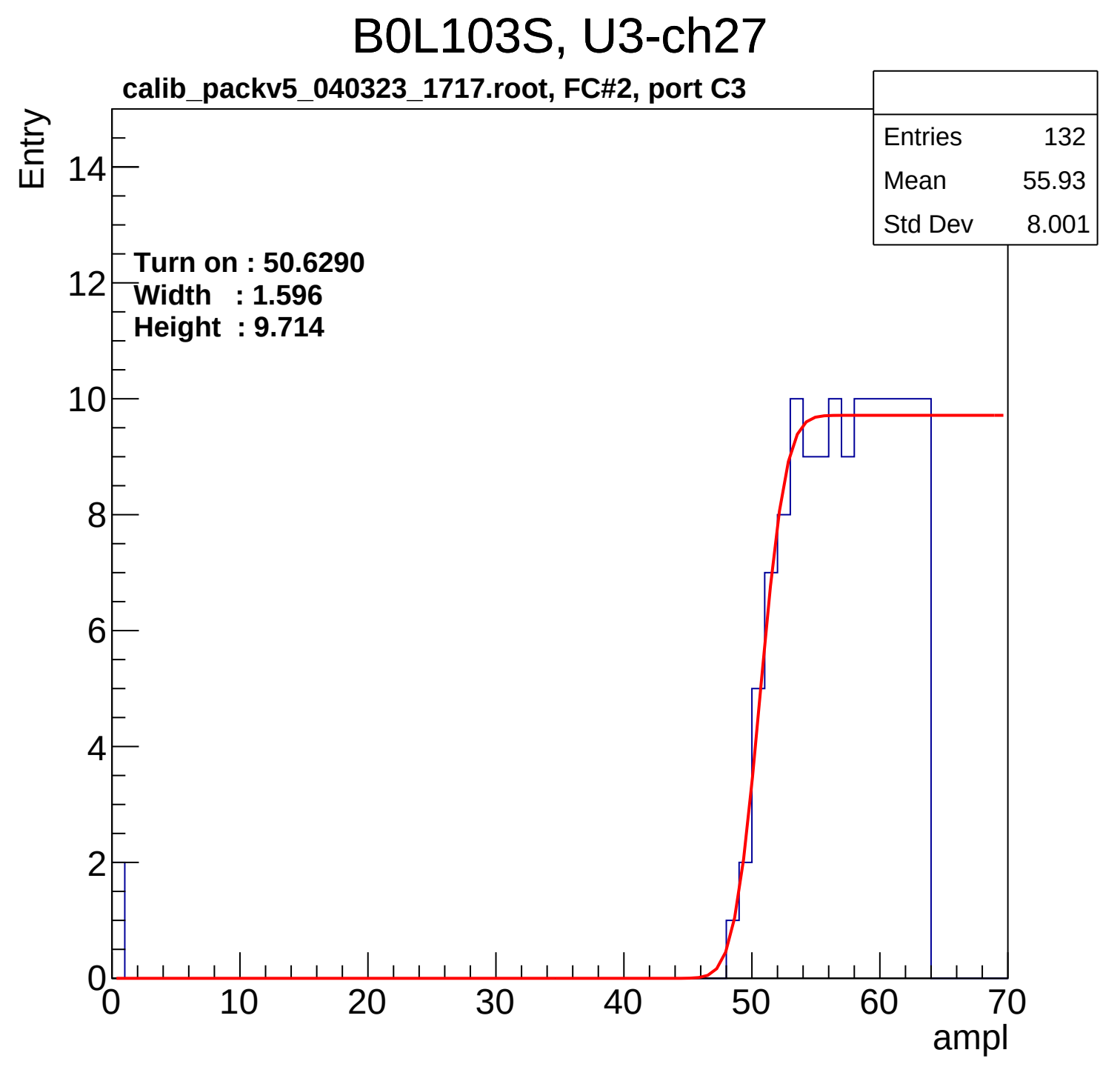
B0L103S, U3-ch27
calib_packv5_040323_1717.root, FC#2, port C3
Entries 132
Mean 55.93
Std Dev 8.001
Turn on : 50.6290
Width : 1.596
Height : 9.714
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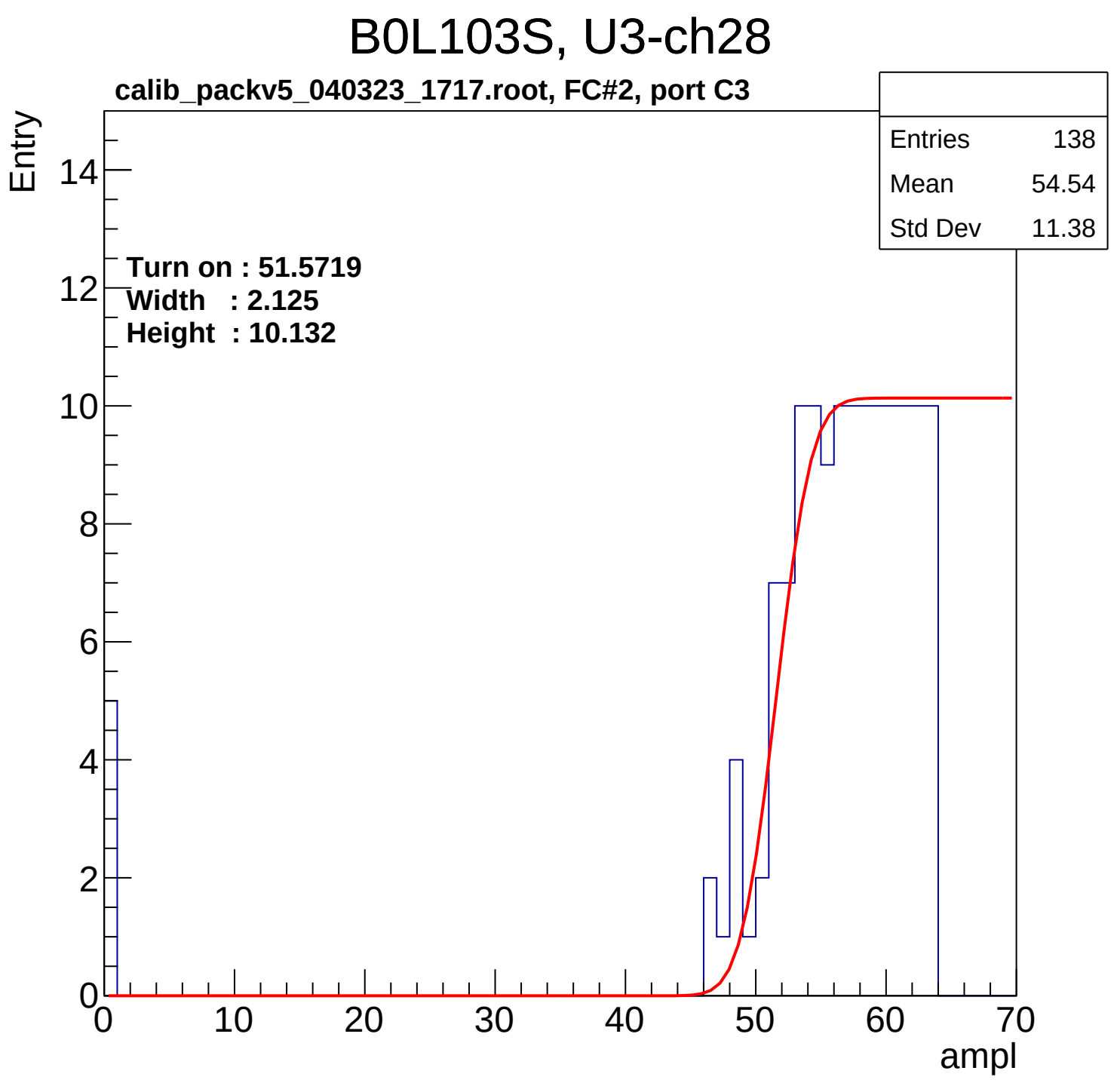
B0L103S, U3-ch28
calib_packv5_040323_1717.root, FC#2, port C3
Entries 138
Mean 54.54
Std Dev 11.38
Turn on : 51.5719
Width : 2.125
Height : 10.132
Entry
ampl
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4
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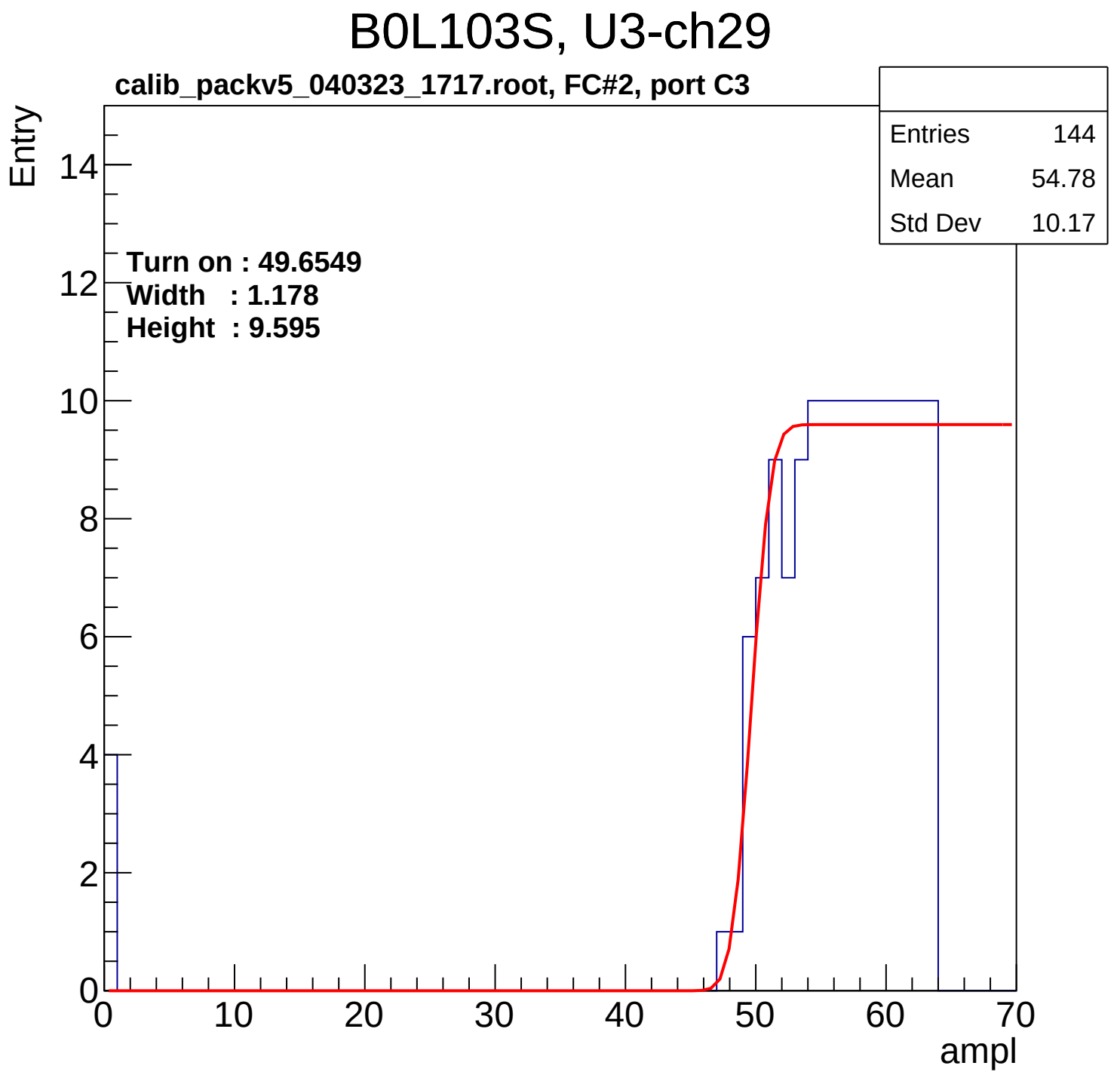
B0L103S, U3-ch29
calib_packv5_040323_1717.root, FC#2, port C3
Entries 144
Mean 54.78
Std Dev 10.17
Turn on : 49.6549
Width : 1.178
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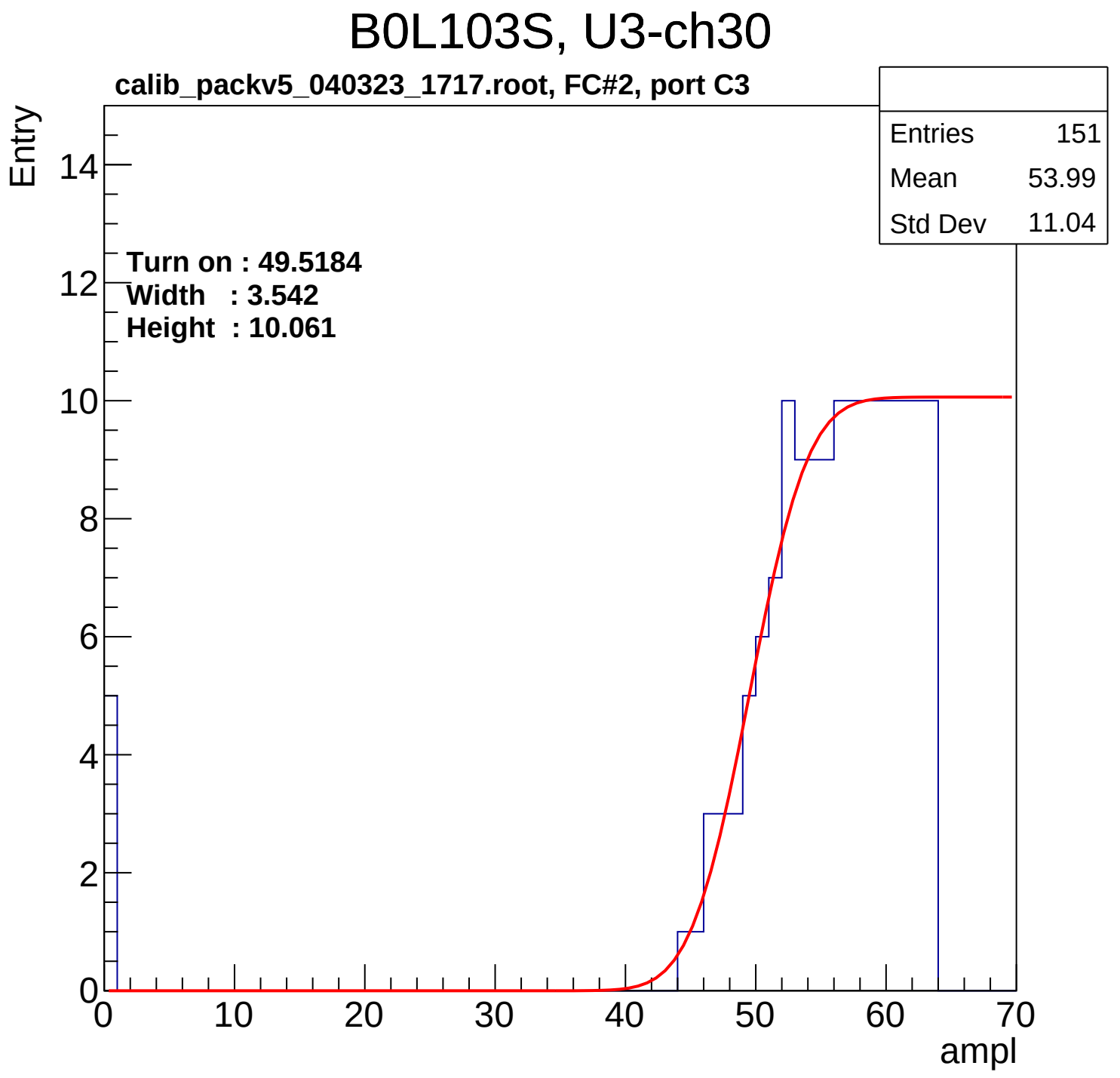
B0L103S, U3-ch30
calib_packv5_040323_1717.root, FC#2, port C3
Entries 151
Mean 53.99
Std Dev 11.04
Turn on : 49.5184
Width : 3.542
Height : 10.061
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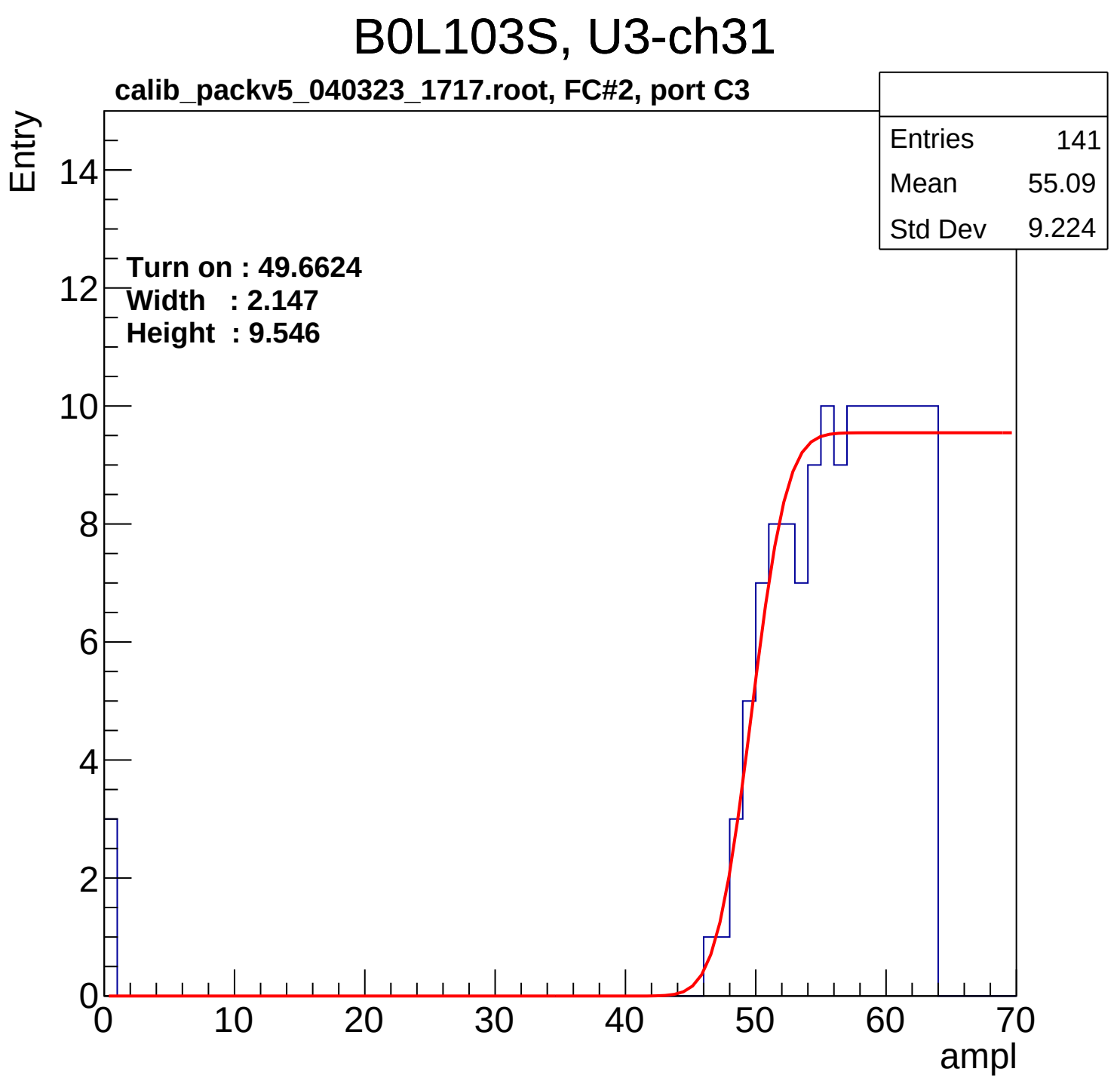
B0L103S, U3-ch31
calib_packv5_040323_1717.root, FC#2, port C3
Entries 141
Mean 55.09
Std Dev 9.224
Turn on : 49.6624
Width : 2.147
Height : 9.546
Entry
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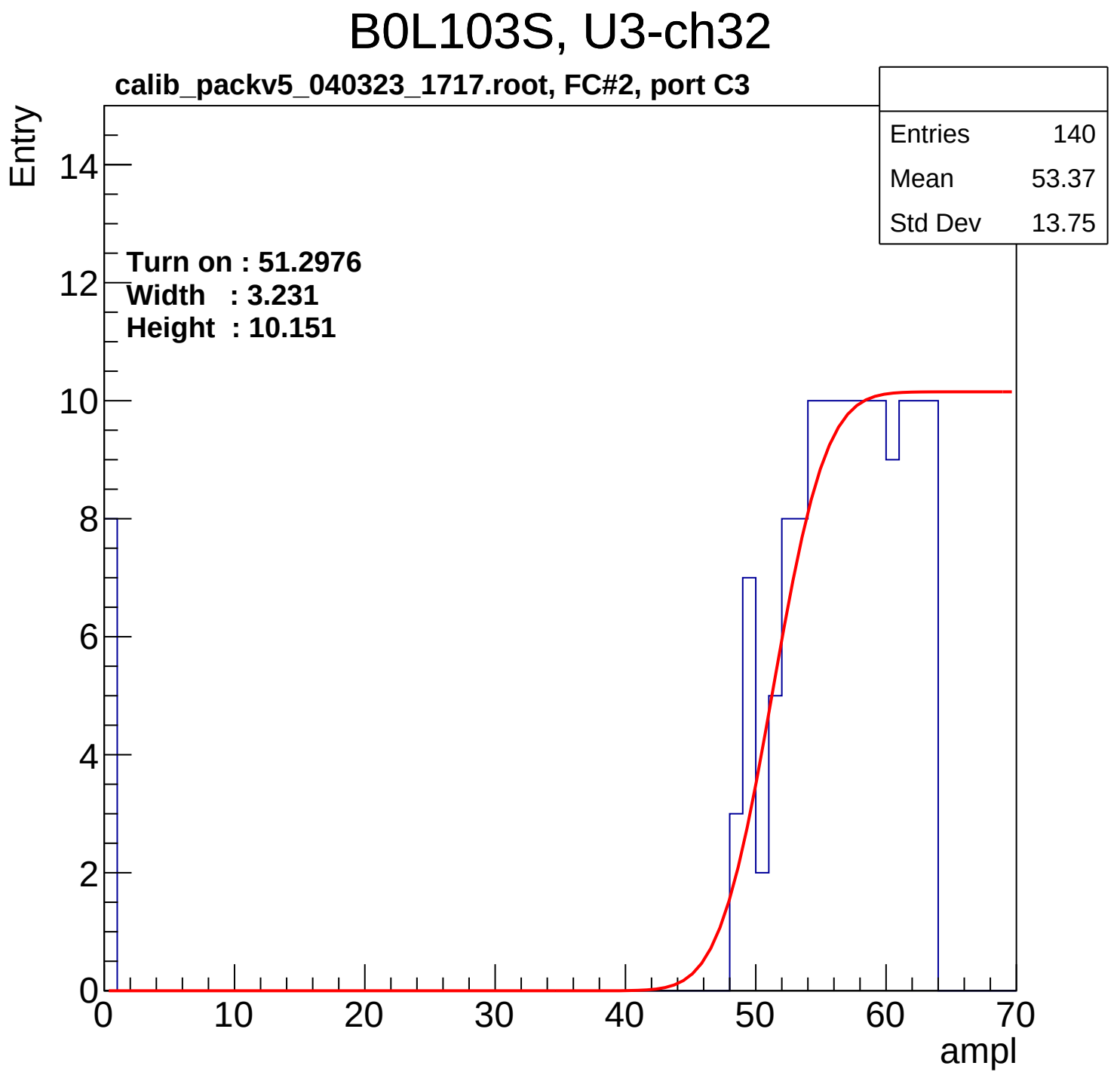
B0L103S, U3-ch32
calib_packv5_040323_1717.root, FC#2, port C3
Entries 140
Mean 53.37
Std Dev 13.75
Turn on : 51.2976
Width : 3.231
Height : 10.151
Entry
ampl
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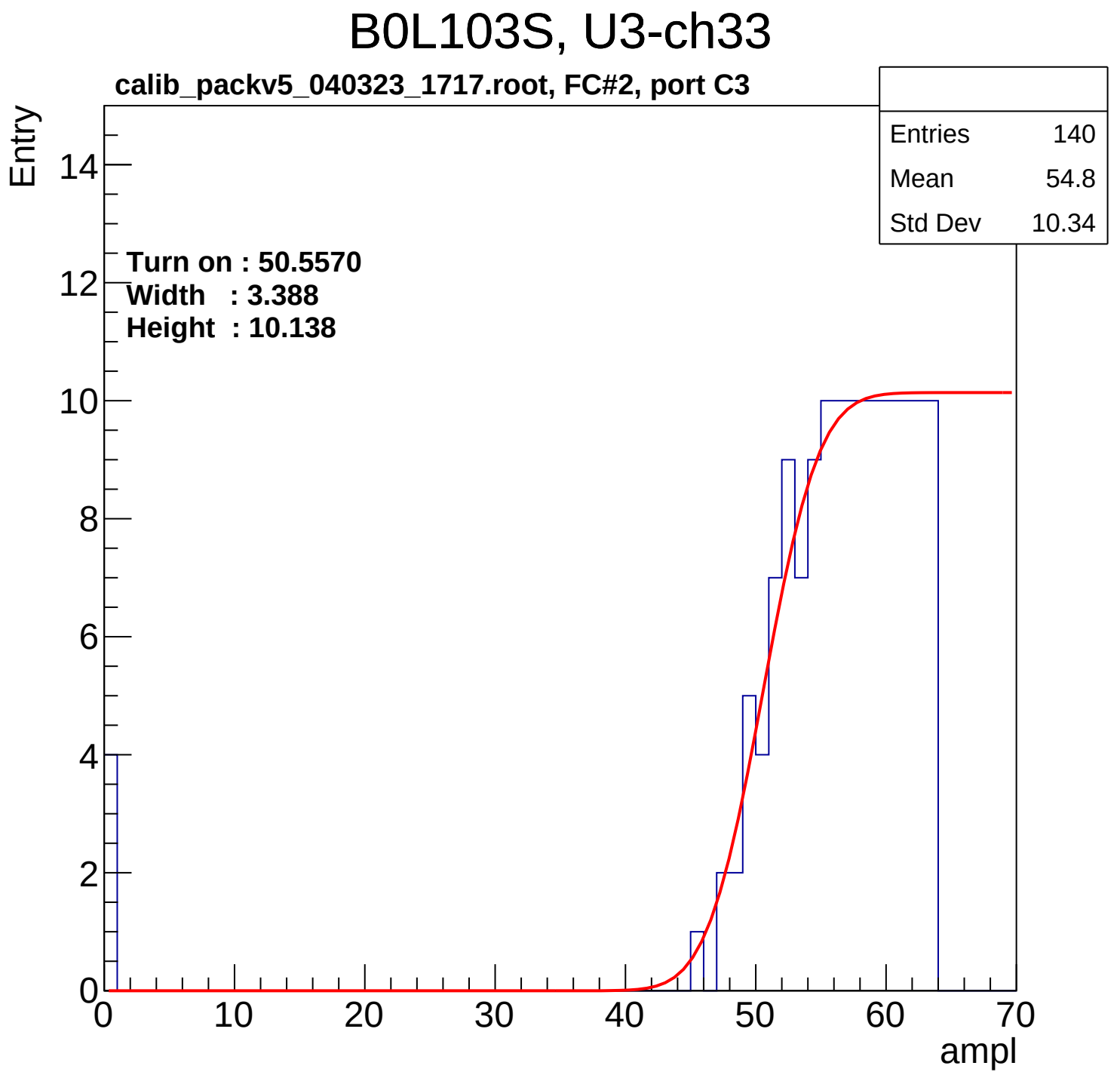
B0L103S, U3-ch33
calib_packv5_040323_1717.root, FC#2, port C3
Entries 140
Mean 54.8
Std Dev 10.34
Turn on : 50.5570
Width : 3.388
Height : 10.138
Entry
ampl
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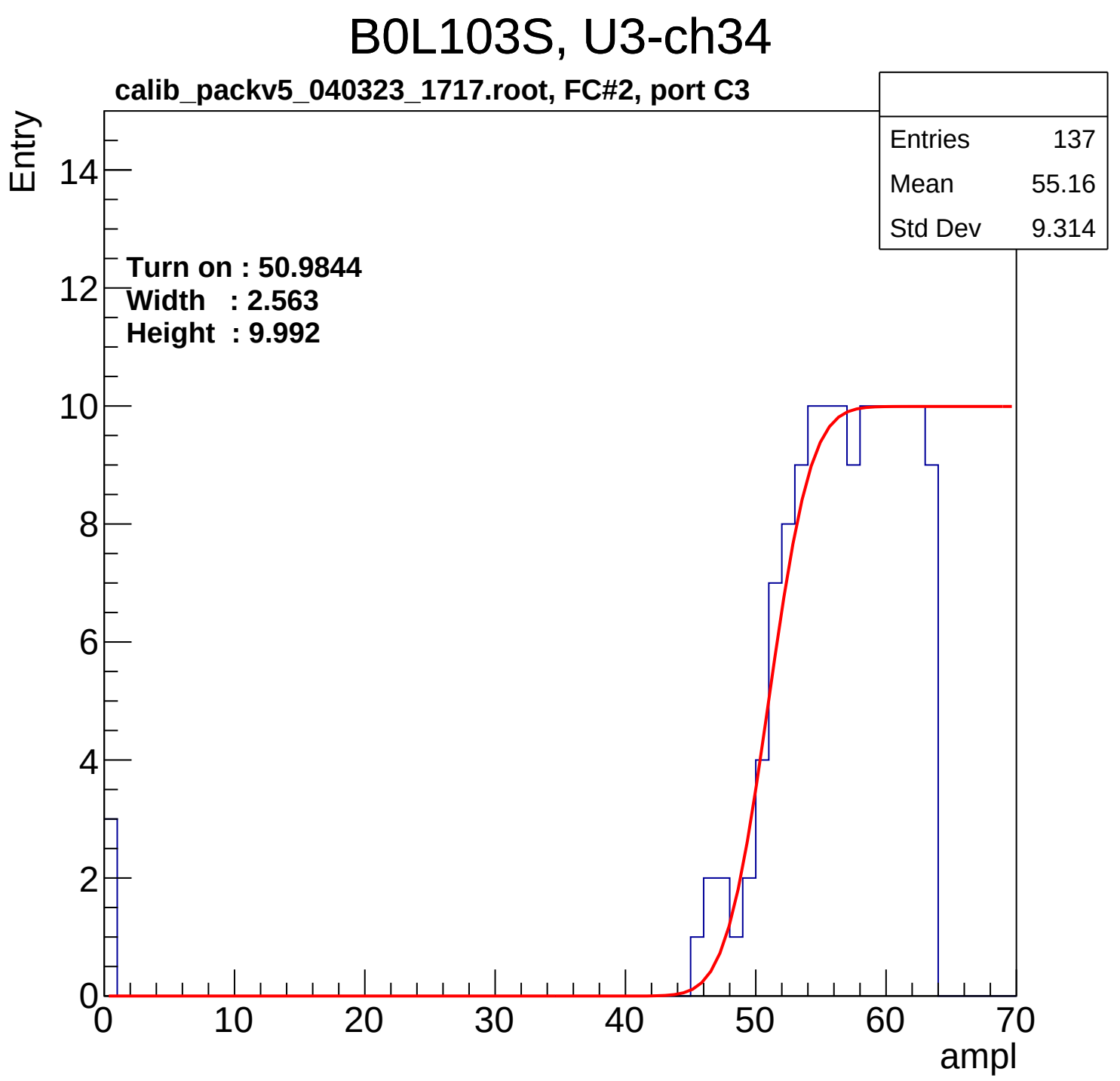
B0L103S, U3-ch34
calib_packv5_040323_1717.root, FC#2, port C3
Entries 137
Mean 55.16
Std Dev 9.314
Turn on : 50.9844
Width : 2.563
Height : 9.992
Entry
ampl
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2
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6
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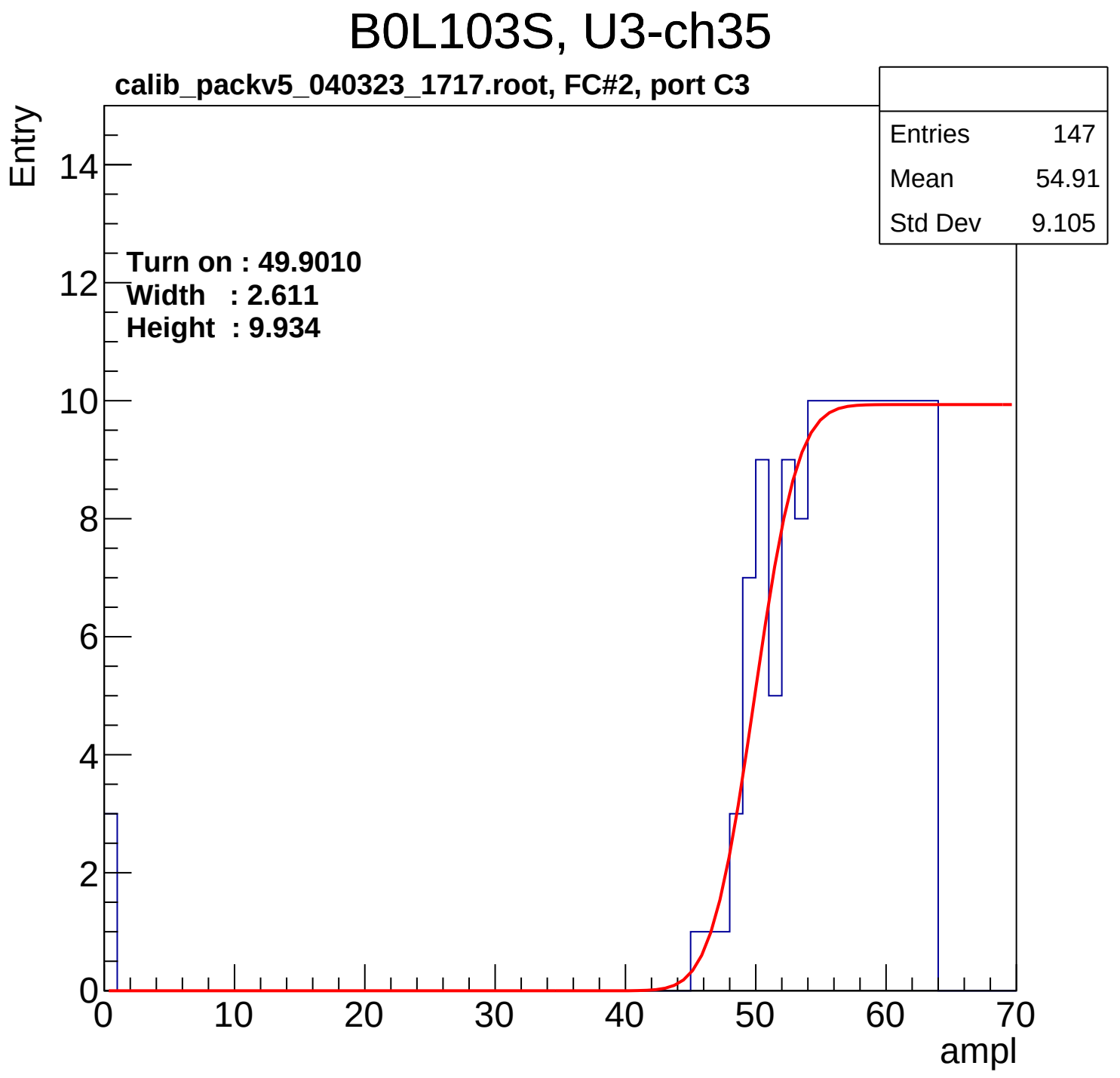
B0L103S, U3-ch35
calib_packv5_040323_1717.root, FC#2, port C3
Entries 147
Mean 54.91
Std Dev 9.105
Turn on : 49.9010
Width : 2.611
Height : 9.934
Entry
ampl
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6
8
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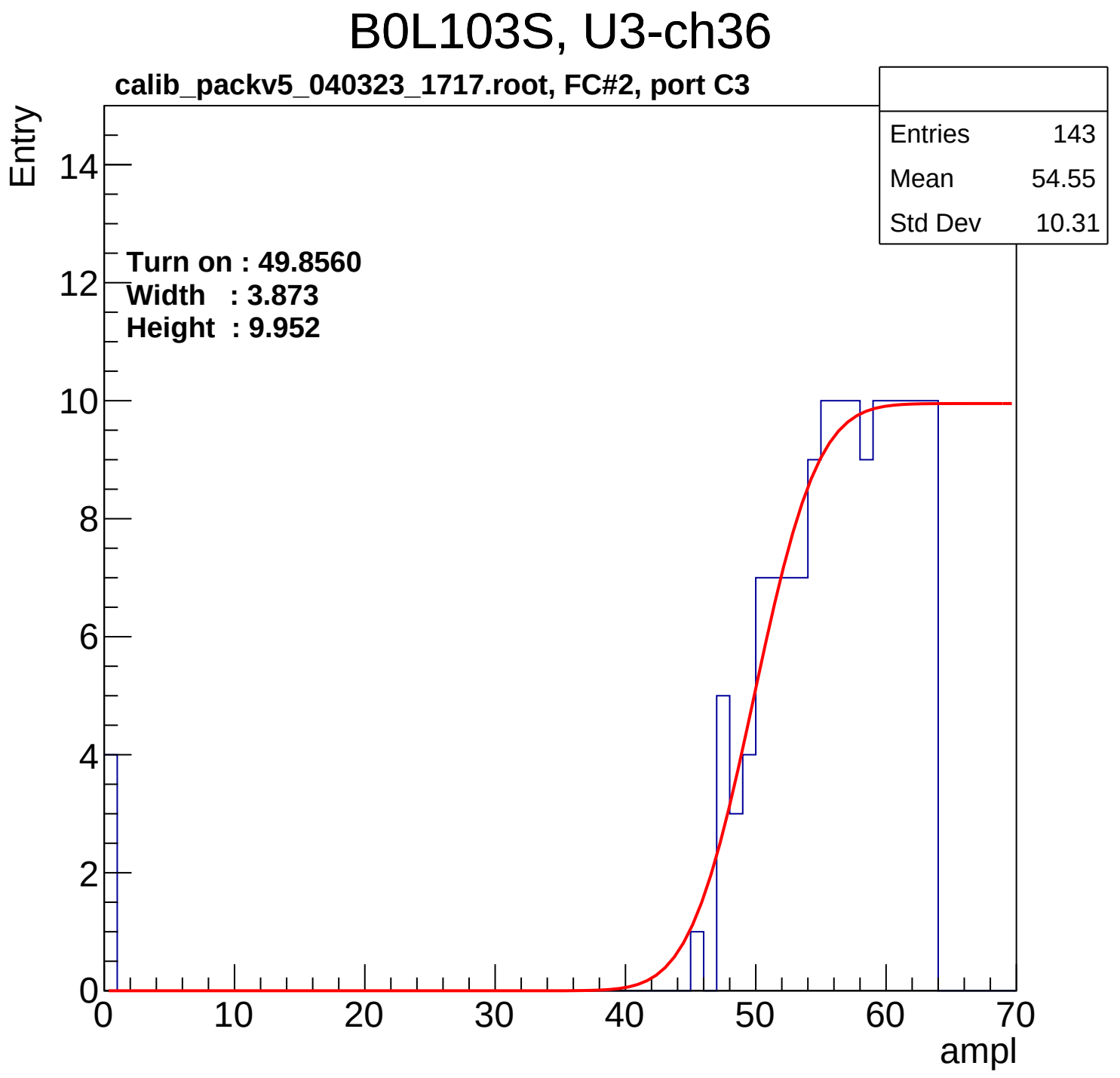
B0L103S, U3-ch36
calib_packv5_040323_1717.root, FC#2, port C3
Entries 143
Mean 54.55
Std Dev 10.31
Turn on : 49.8560
Width : 3.873
Height : 9.952
Entry
ampl
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4
6
8
10
12
14
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10
20
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40
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60
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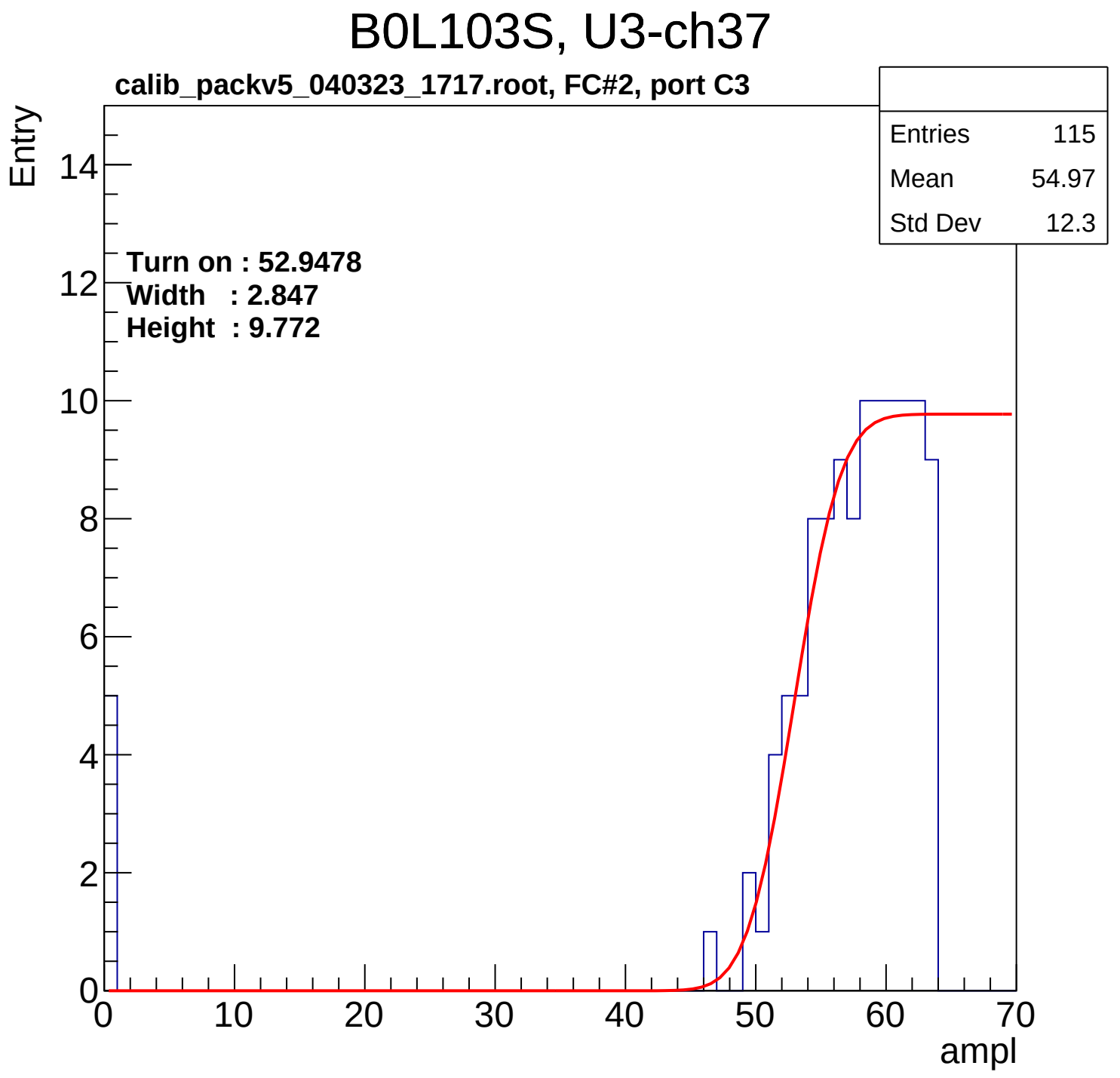
B0L103S, U3-ch37
calib_packv5_040323_1717.root, FC#2, port C3
Entries 115
Mean 54.97
Std Dev 12.3
Turn on : 52.9478
Width : 2.847
Height : 9.772
Entry
ampl
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6
8
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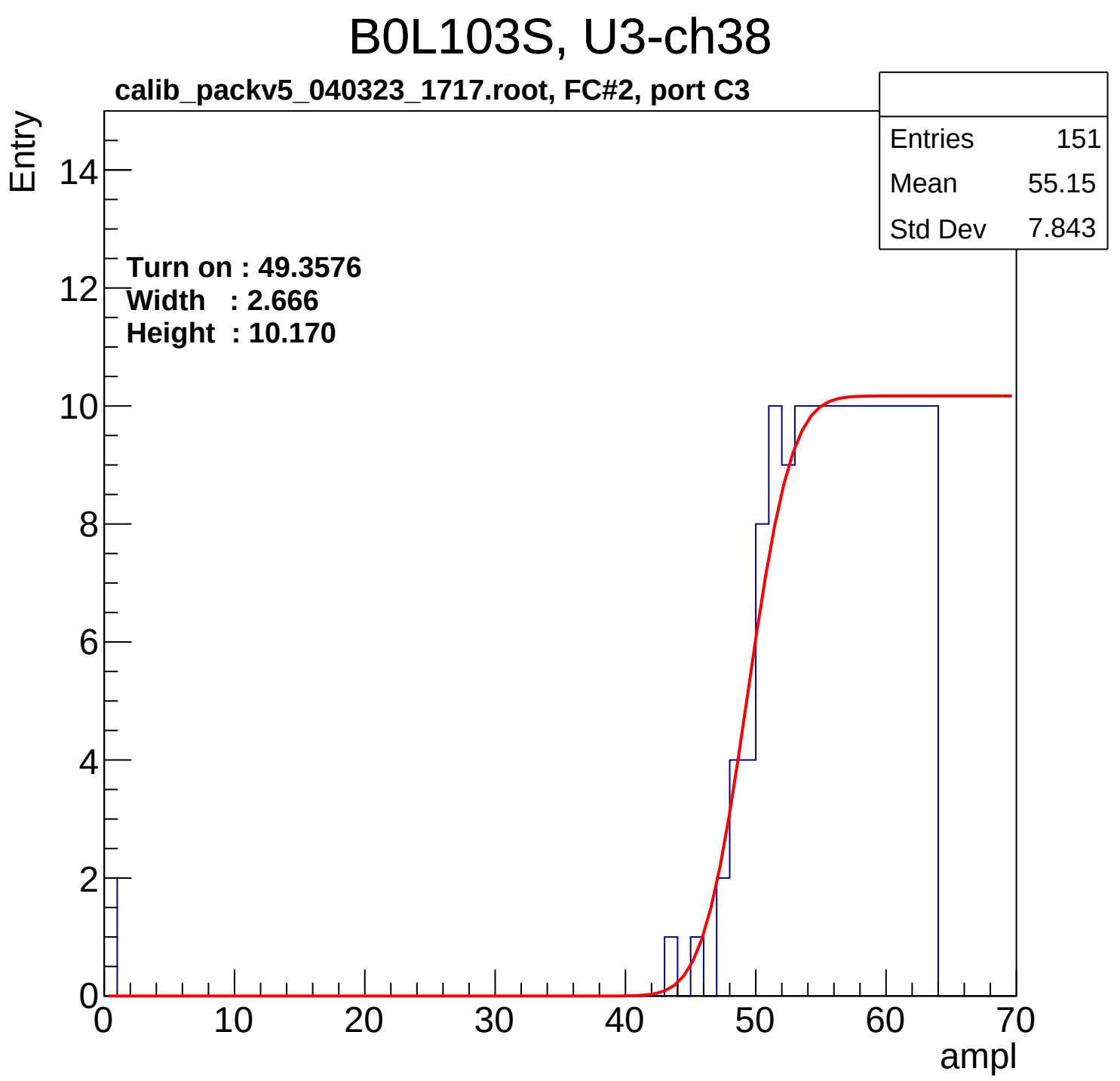
B0L103S, U3-ch38
calib_packv5_040323_1717.root, FC#2, port C3
Entries 151
Mean 55.15
Std Dev 7.843
Turn on : 49.3576
Width : 2.666
Height : 10.170
Entry
ampl
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6
8
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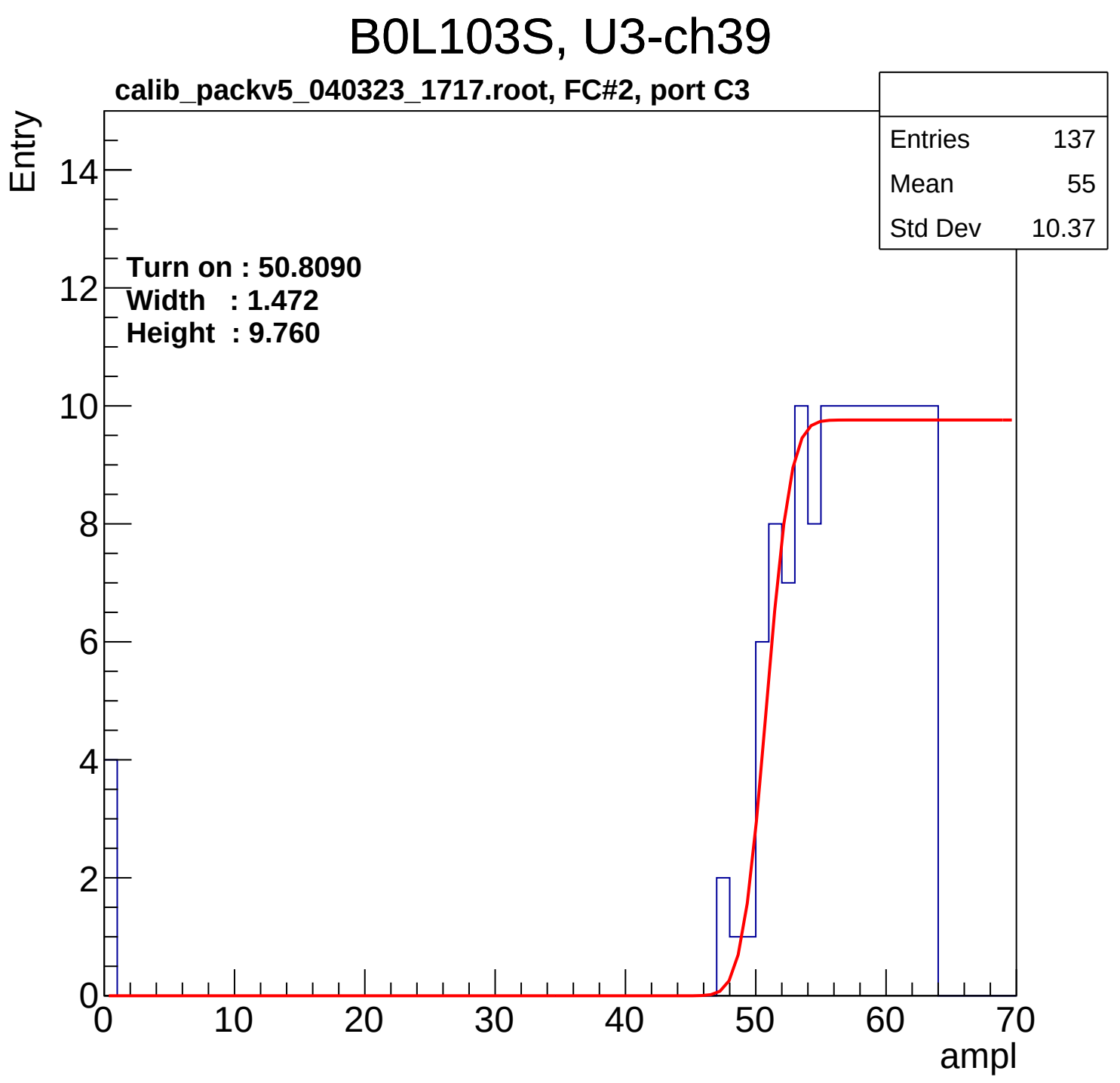
B0L103S, U3-ch39
calib_packv5_040323_1717.root, FC#2, port C3
Entries 137
Mean 55
Std Dev 10.37
Turn on : 50.8090
Width : 1.472
Height : 9.760
Entry
ampl
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6
8
10
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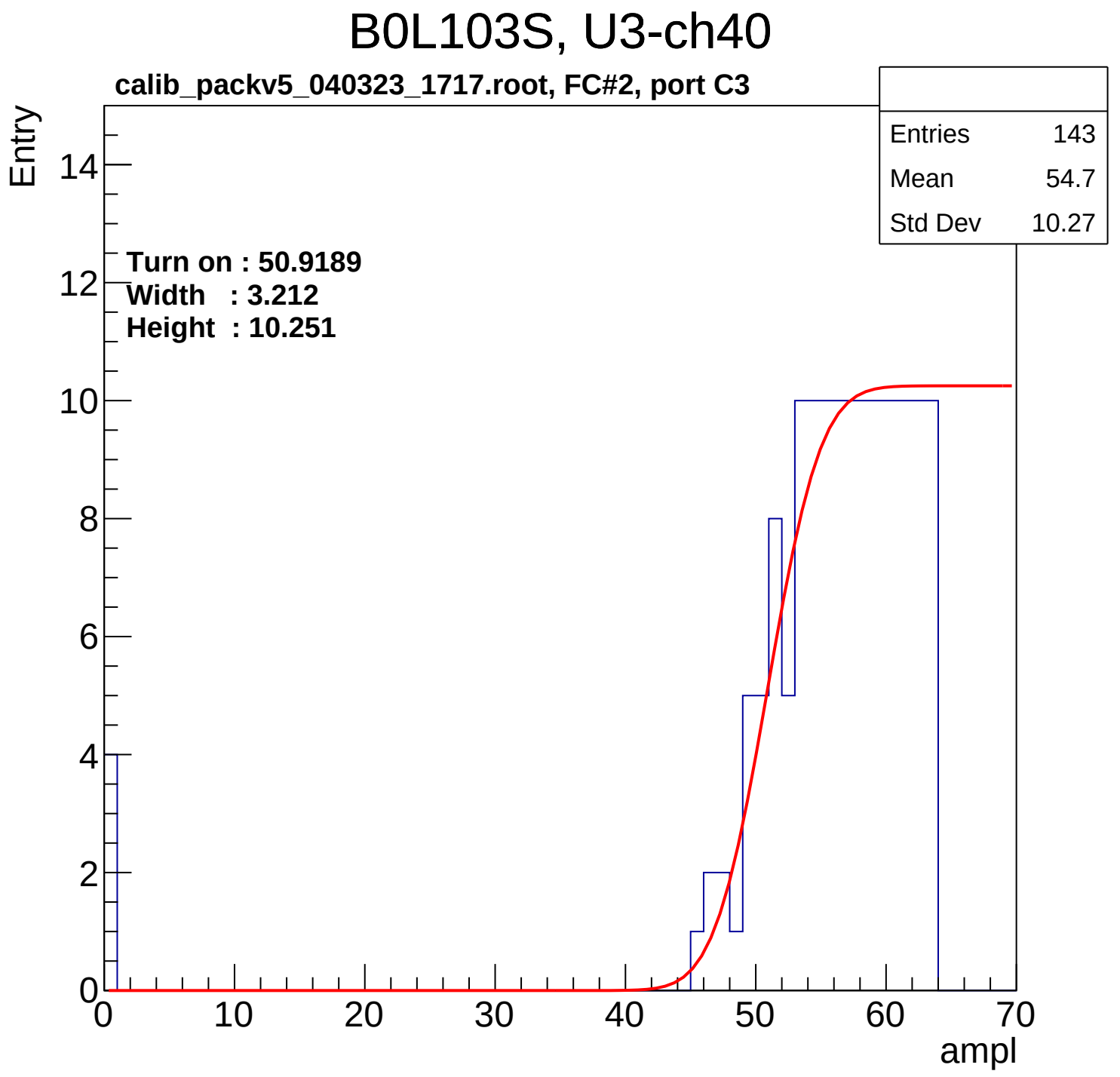
B0L103S, U3-ch40
calib_packv5_040323_1717.root, FC#2, port C3
Entries 143
Mean 54.7
Std Dev 10.27
Turn on : 50.9189
Width : 3.212
Height : 10.251
Entry
ampl
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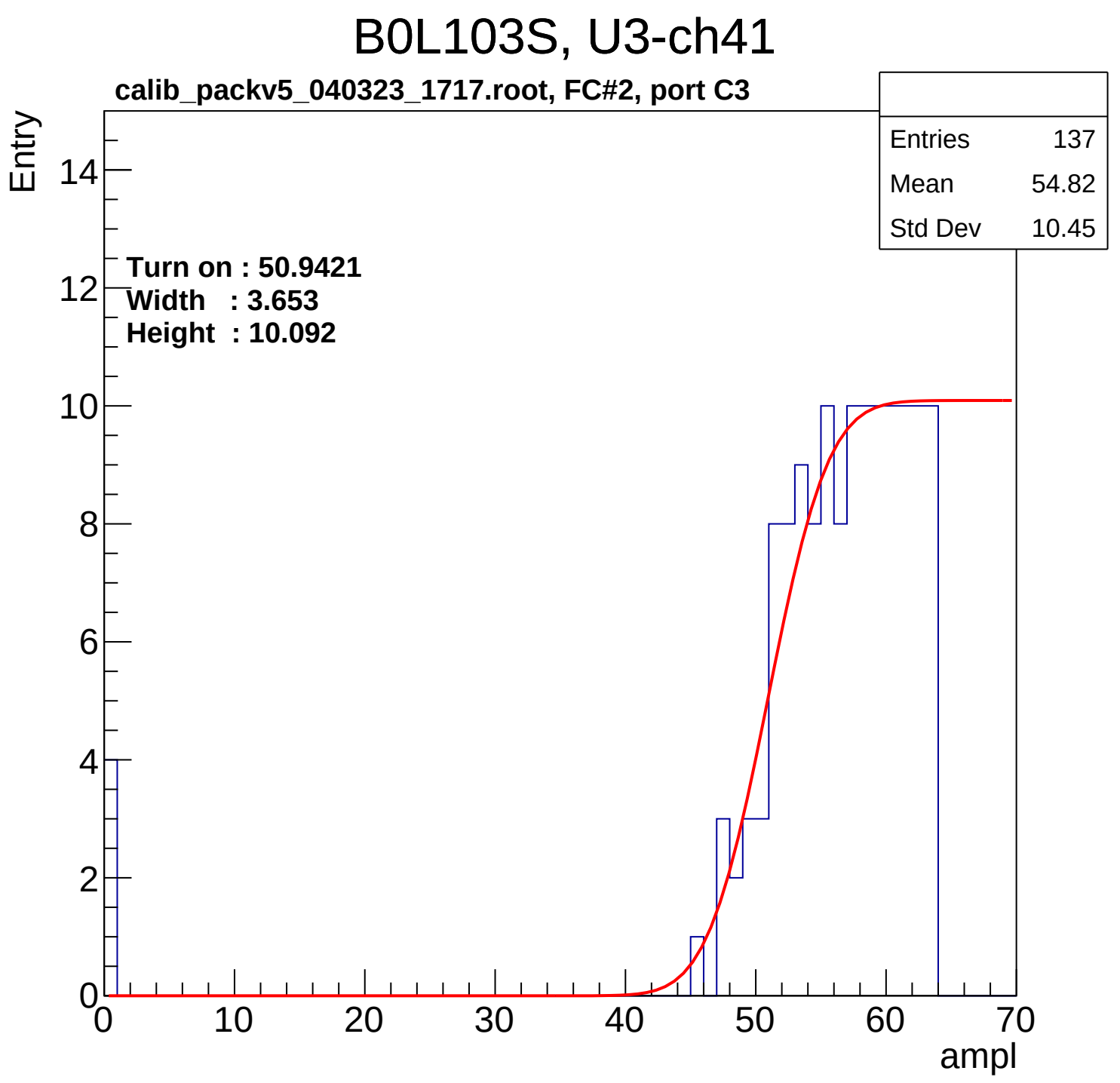
B0L103S, U3-ch41
calib_packv5_040323_1717.root, FC#2, port C3
Entries 137
Mean 54.82
Std Dev 10.45
Turn on : 50.9421
Width : 3.653
Height : 10.092
Entry
ampl
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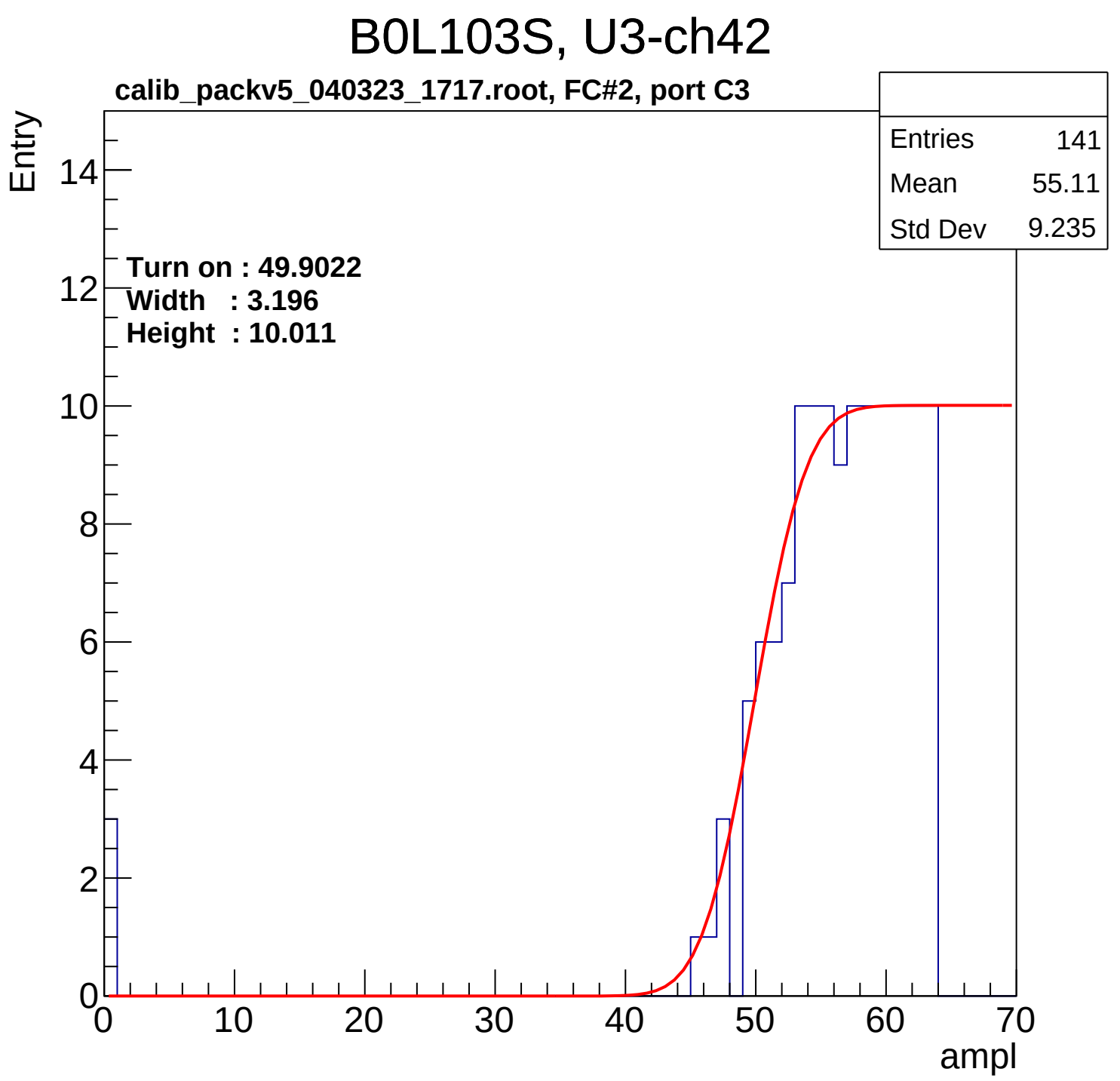
B0L103S, U3-ch42
calib_packv5_040323_1717.root, FC#2, port C3
Entries 141
Mean 55.11
Std Dev 9.235
Turn on : 49.9022
Width : 3.196
Height : 10.011
Entry
ampl
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6
8
10
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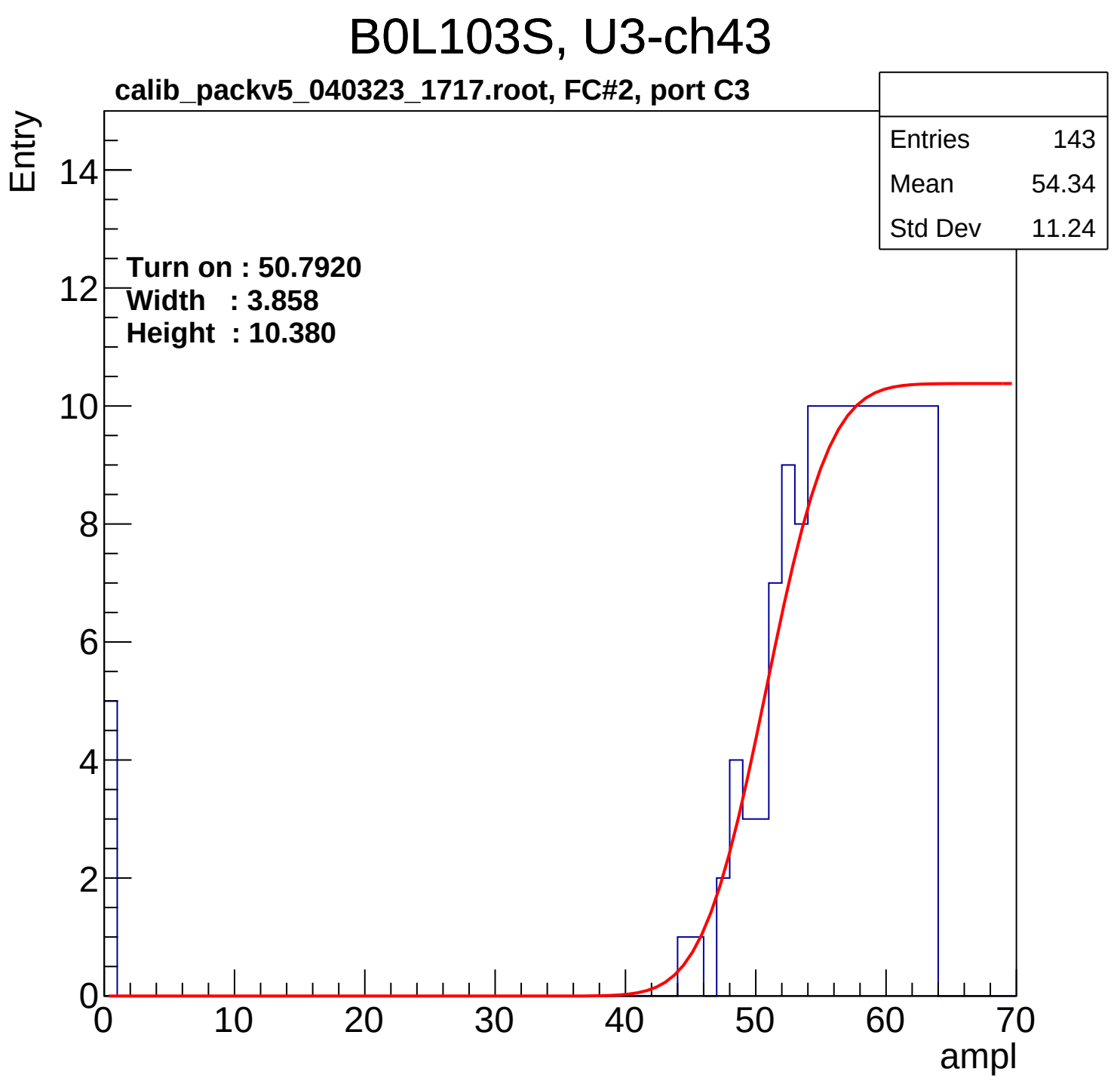
B0L103S, U3-ch43
calib_packv5_040323_1717.root, FC#2, port C3
Entries 143
Mean 54.34
Std Dev 11.24
Turn on : 50.7920
Width : 3.858
Height : 10.380
Entry
ampl
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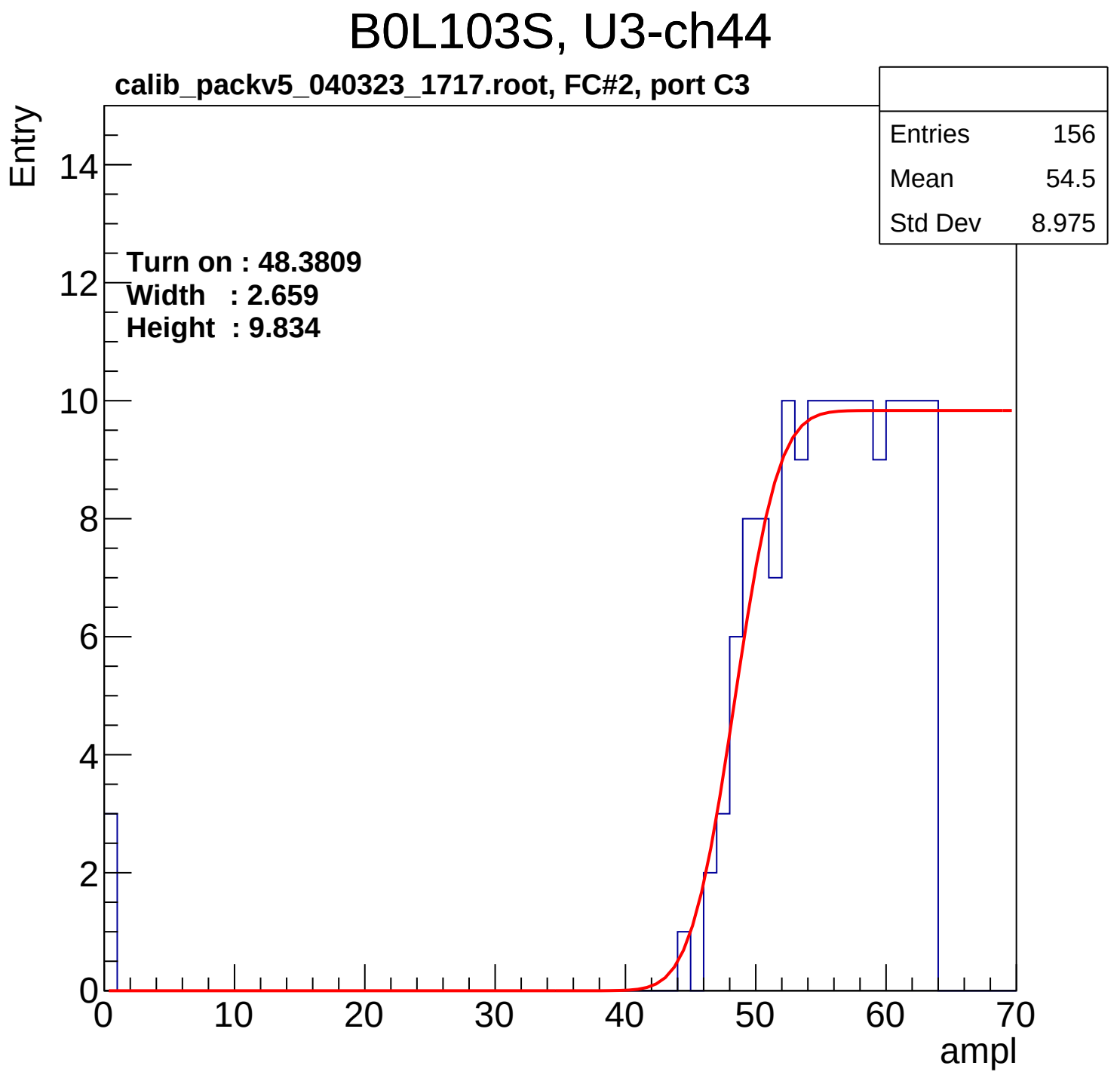
B0L103S, U3-ch44
calib_packv5_040323_1717.root, FC#2, port C3
Entries 156
Mean 54.5
Std Dev 8.975
Turn on : 48.3809
Width : 2.659
Height : 9.834
Entry
ampl
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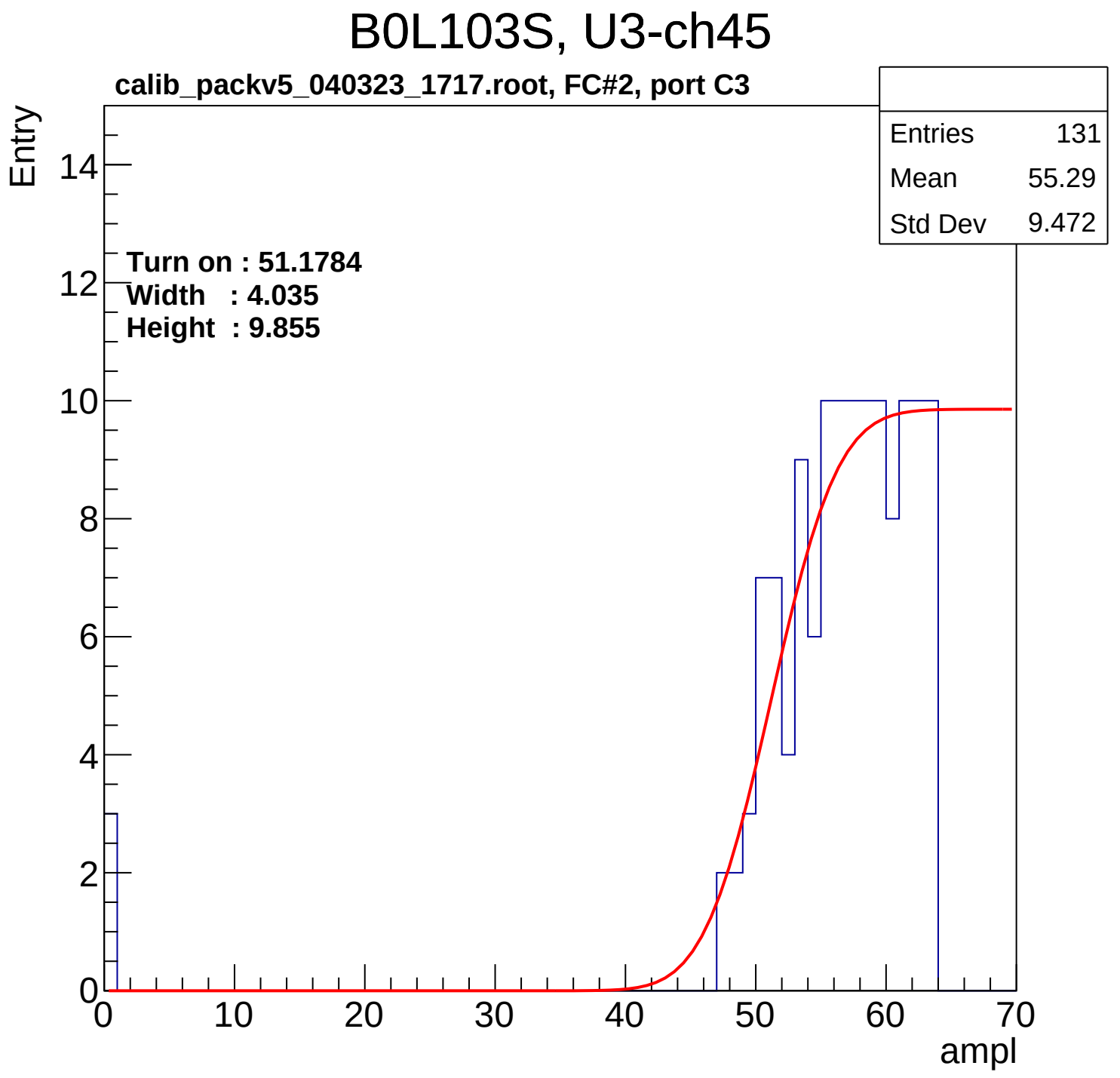
B0L103S, U3-ch45
calib_packv5_040323_1717.root, FC#2, port C3
Entries 131
Mean 55.29
Std Dev 9.472
Turn on : 51.1784
Width : 4.035
Height : 9.855
Entry
ampl
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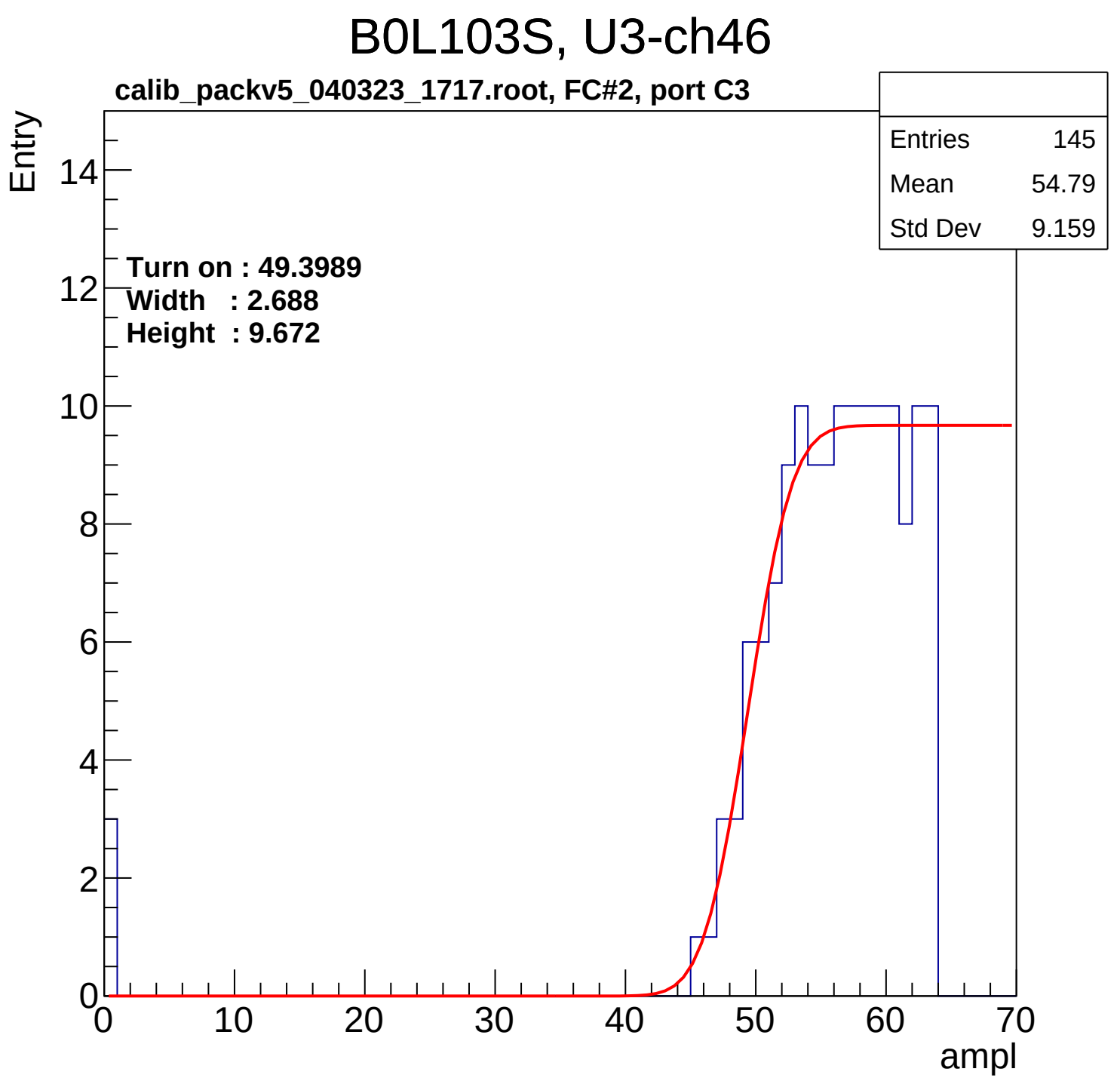
B0L103S, U3-ch46
calib_packv5_040323_1717.root, FC#2, port C3
Entries 145
Mean 54.79
Std Dev 9.159
Turn on : 49.3989
Width : 2.688
Height : 9.672
Entry
ampl
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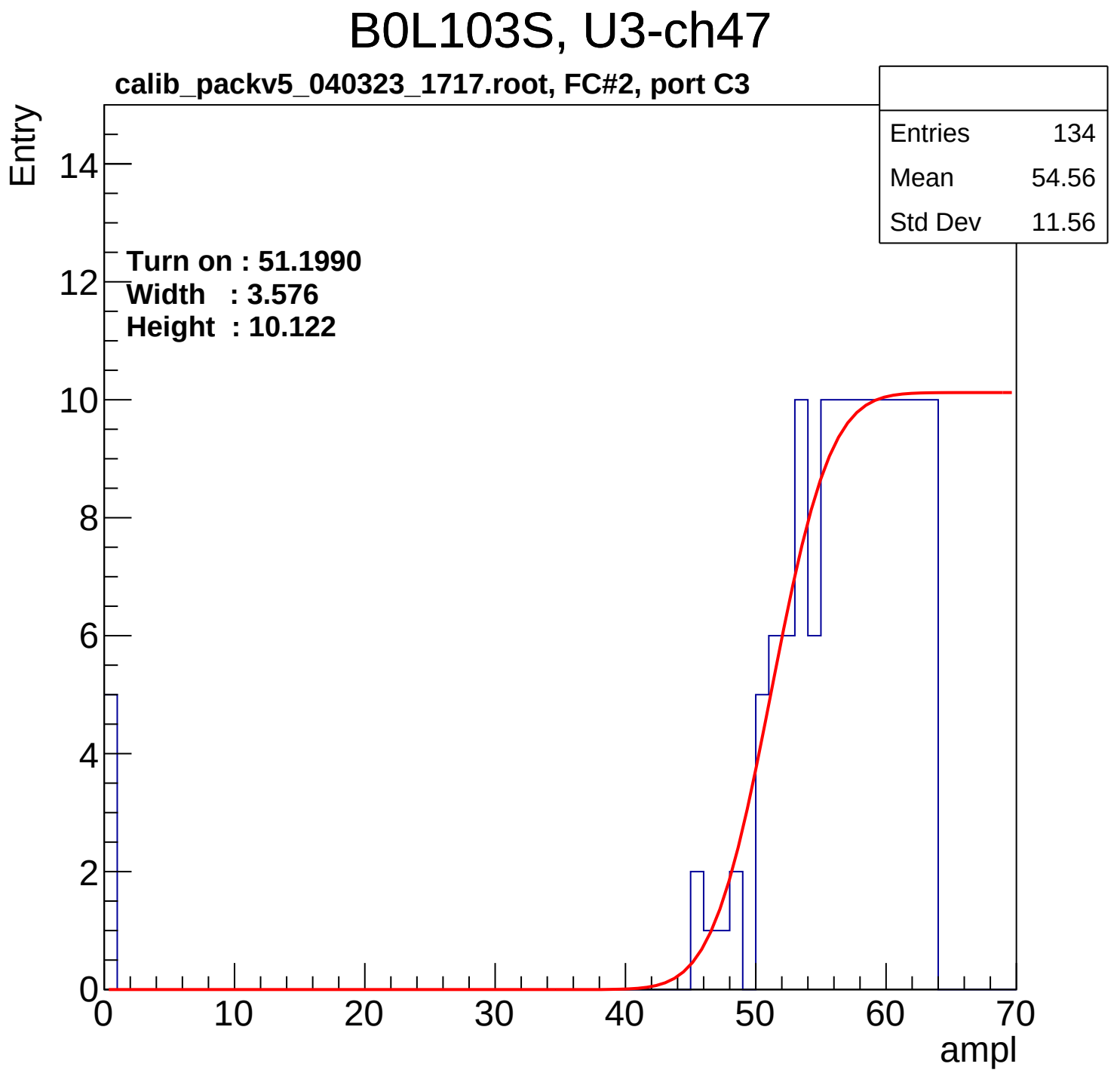
B0L103S, U3-ch47
calib_packv5_040323_1717.root, FC#2, port C3
Entries 134
Mean 54.56
Std Dev 11.56
Turn on : 51.1990
Width : 3.576
Height : 10.122
Entry
ampl
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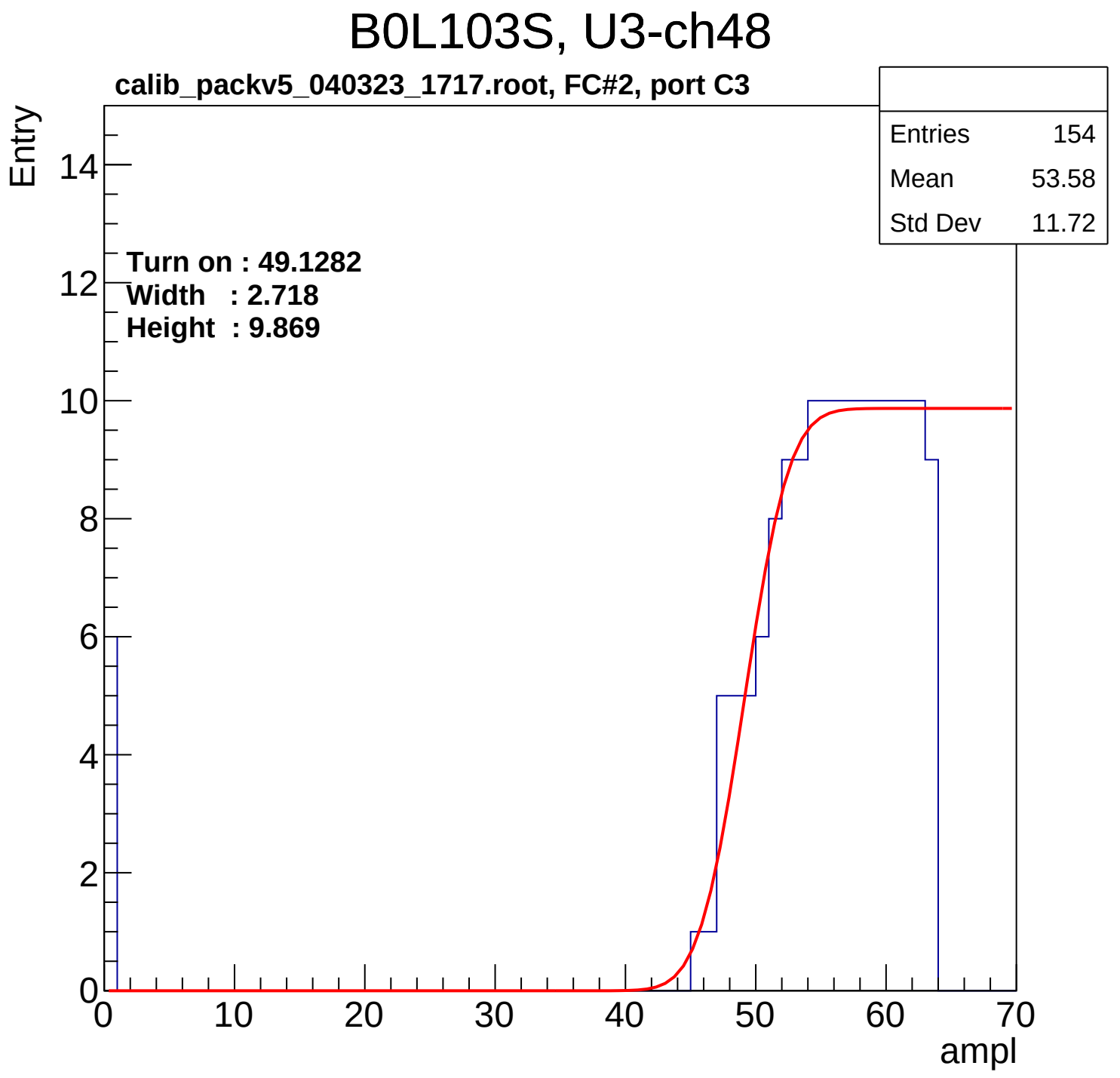
B0L103S, U3-ch48
calib_packv5_040323_1717.root, FC#2, port C3
Entries 154
Mean 53.58
Std Dev 11.72
Turn on : 49.1282
Width : 2.718
Height : 9.869
Entry
ampl
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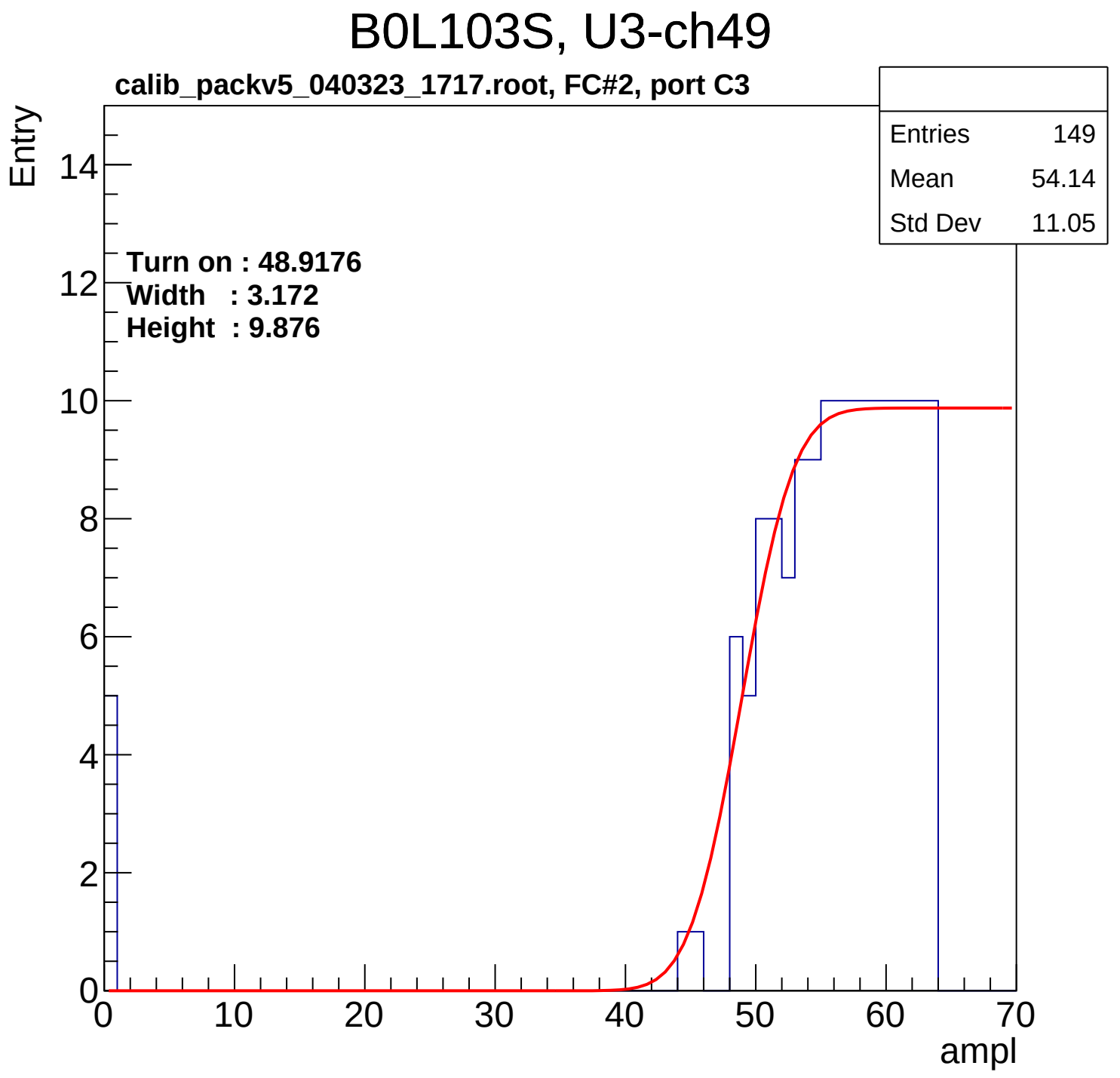
B0L103S, U3-ch49
calib_packv5_040323_1717.root, FC#2, port C3
Entries 149
Mean 54.14
Std Dev 11.05
Turn on : 48.9176
Width : 3.172
Height : 9.876
Entry
ampl
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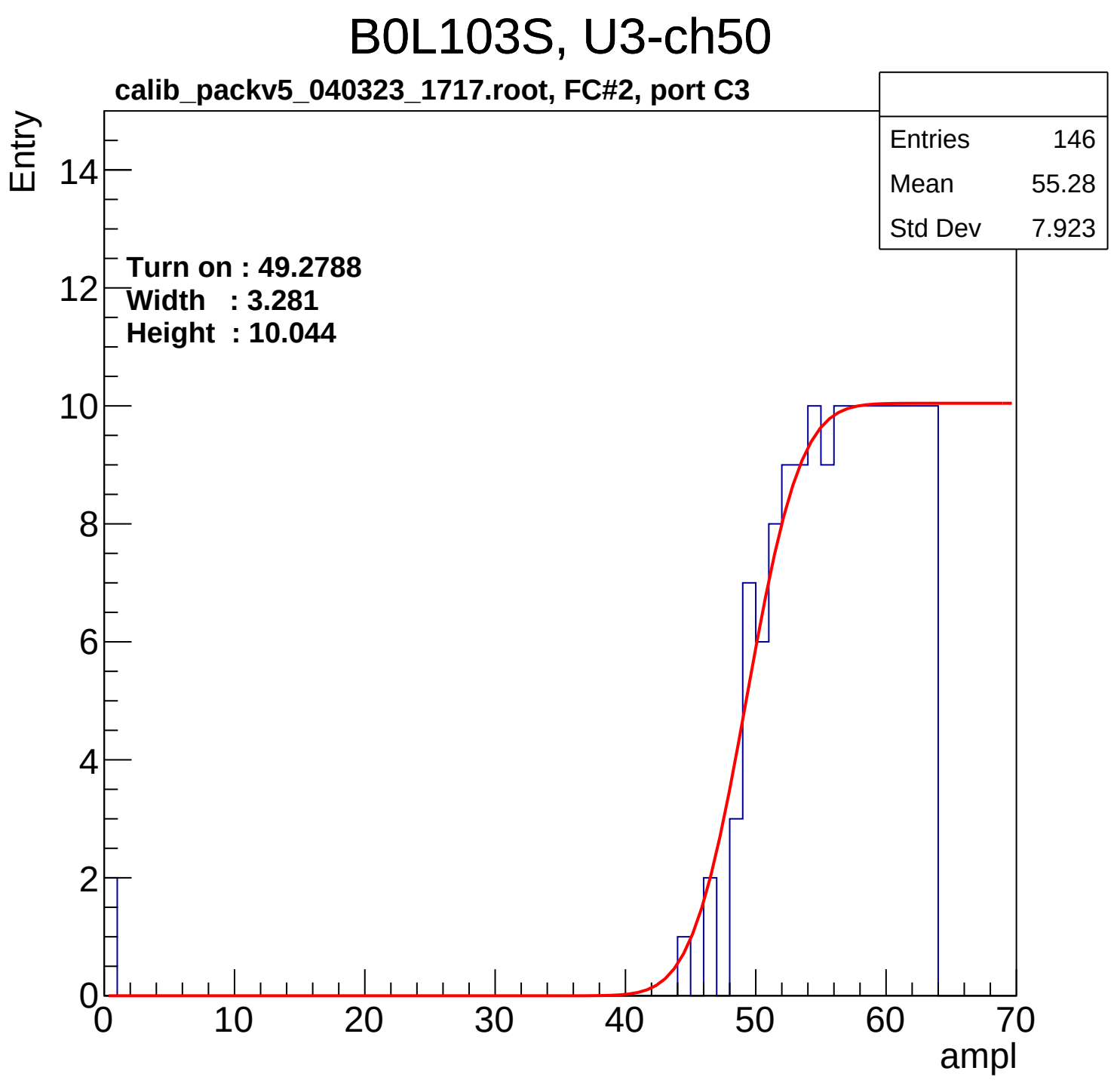
B0L103S, U3-ch50
calib_packv5_040323_1717.root, FC#2, port C3
Entries 146
Mean 55.28
Std Dev 7.923
Turn on : 49.2788
Width : 3.281
Height : 10.044
Entry
ampl
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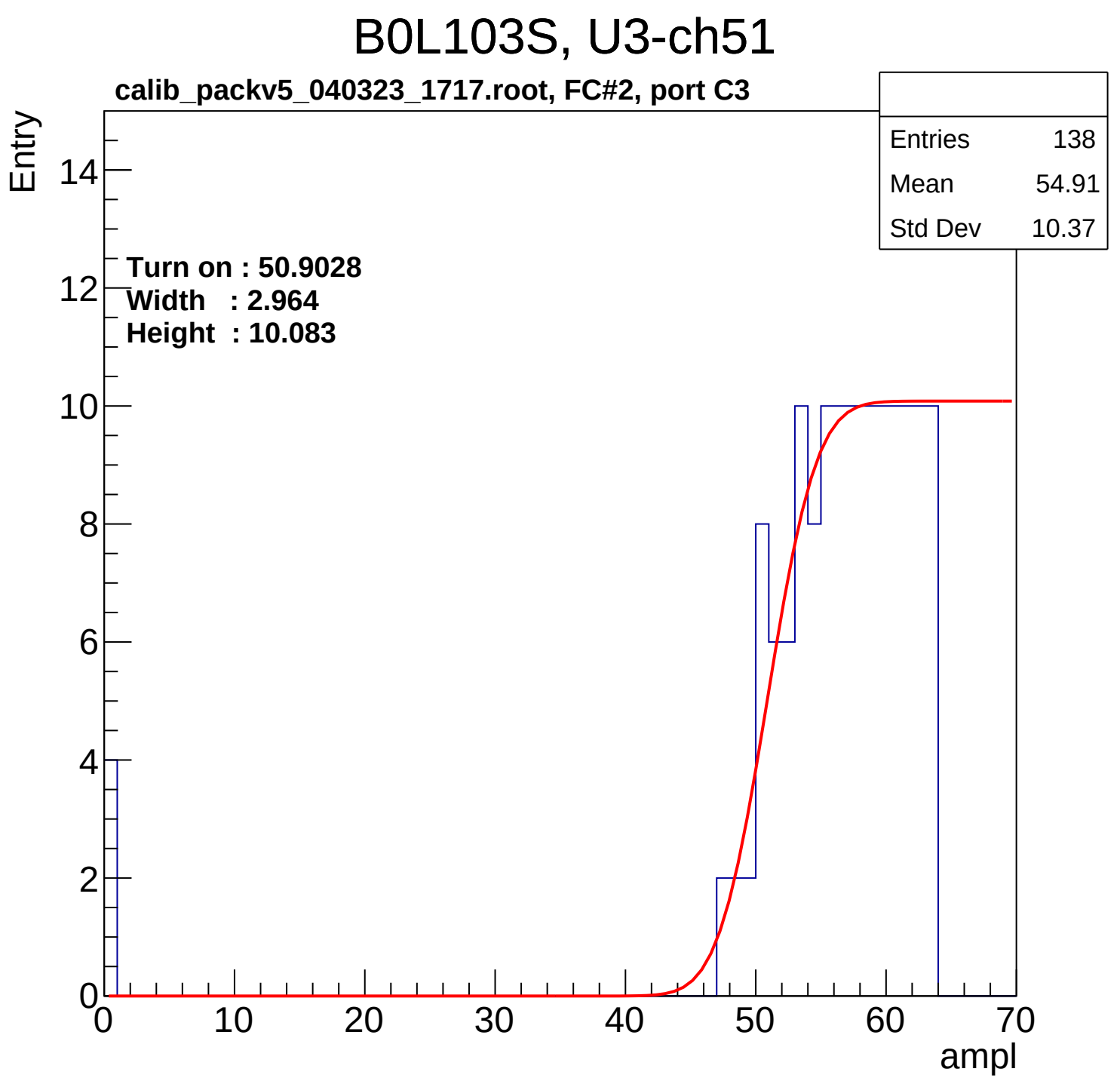
B0L103S, U3-ch51
calib_packv5_040323_1717.root, FC#2, port C3
Entries 138
Mean 54.91
Std Dev 10.37
Turn on : 50.9028
Width : 2.964
Height : 10.083
Entry
ampl
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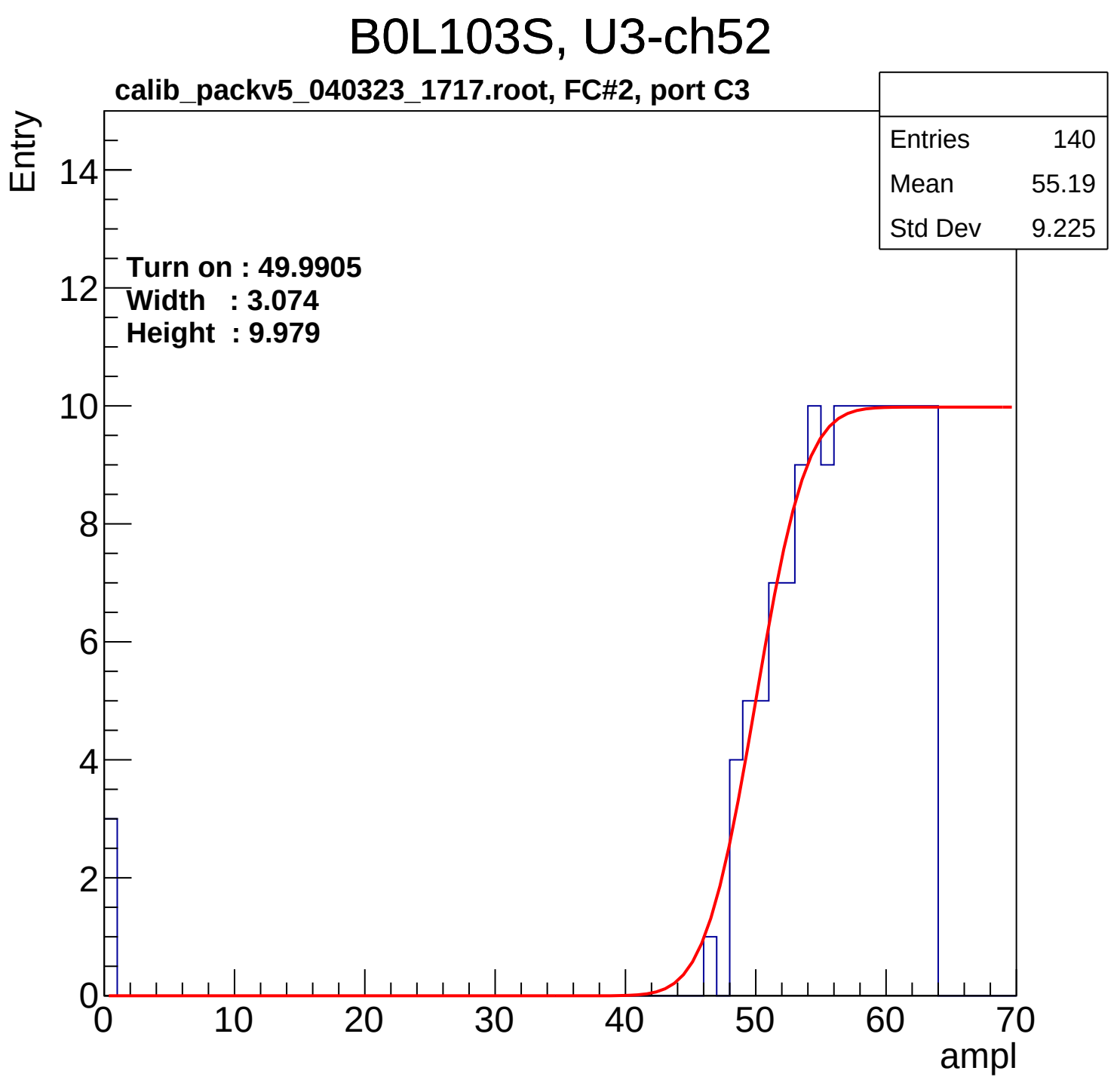
B0L103S, U3-ch52
calib_packv5_040323_1717.root, FC#2, port C3
Entries 140
Mean 55.19
Std Dev 9.225
Turn on : 49.9905
Width : 3.074
Height : 9.979
Entry
ampl
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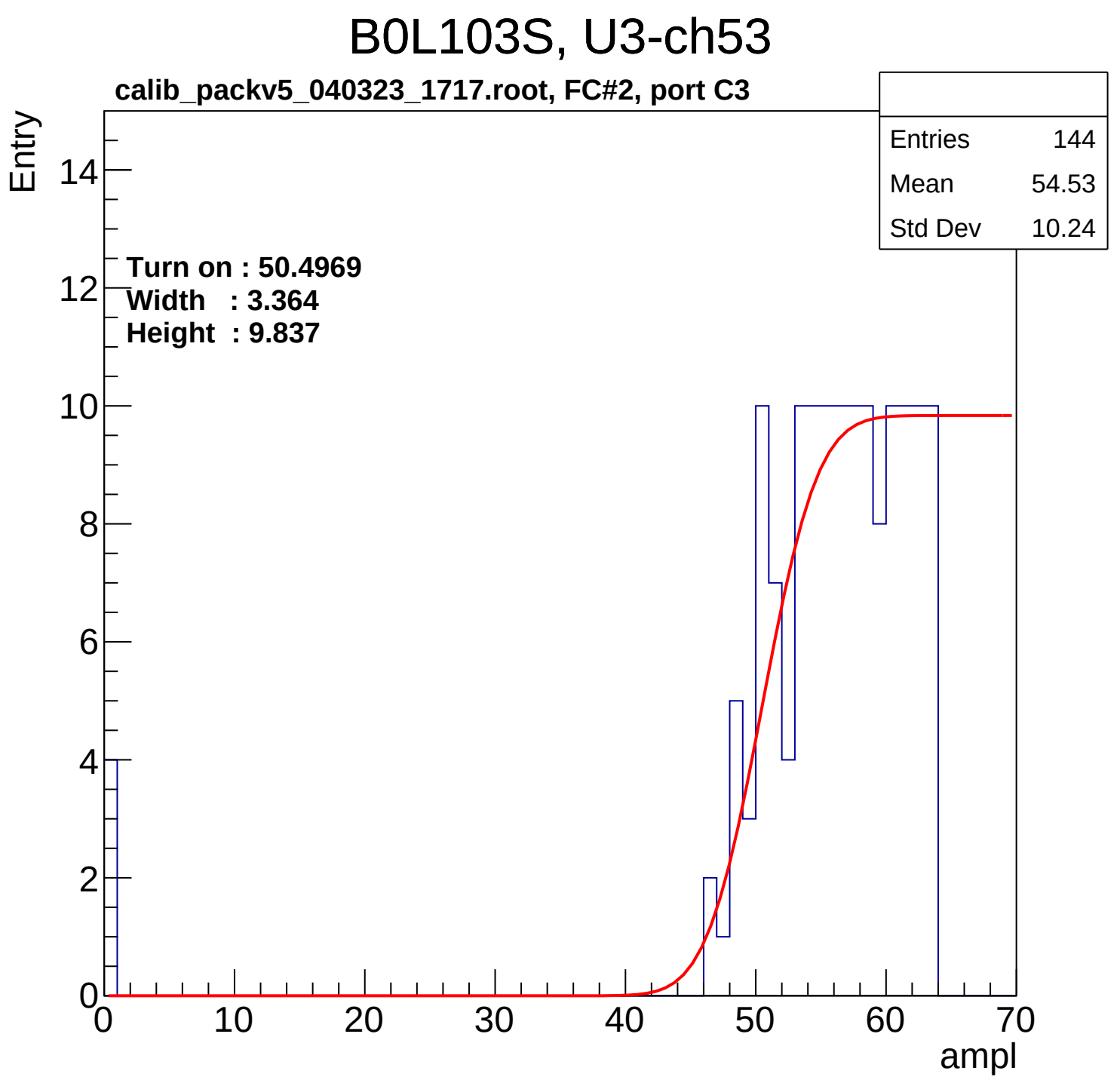
B0L103S, U3-ch53
calib_packv5_040323_1717.root, FC#2, port C3
Entries 144
Mean 54.53
Std Dev 10.24
Turn on : 50.4969
Width : 3.364
Height : 9.837
Entry
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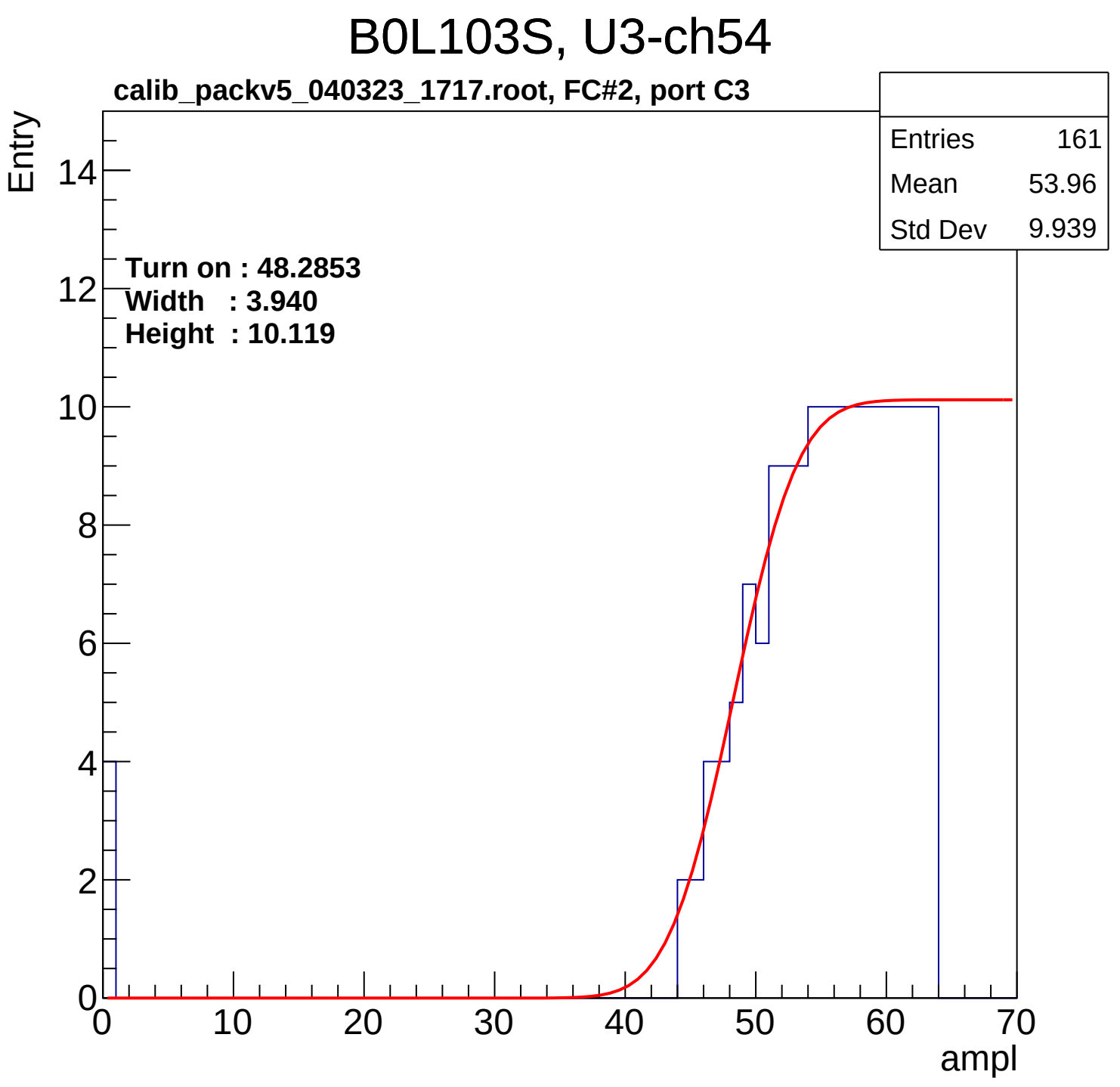
B0L103S, U3-ch54
calib_packv5_040323_1717.root, FC#2, port C3
Entries 161
Mean 53.96
Std Dev 9.939
Turn on : 48.2853
Width : 3.940
Height : 10.119
Entry
ampl
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8
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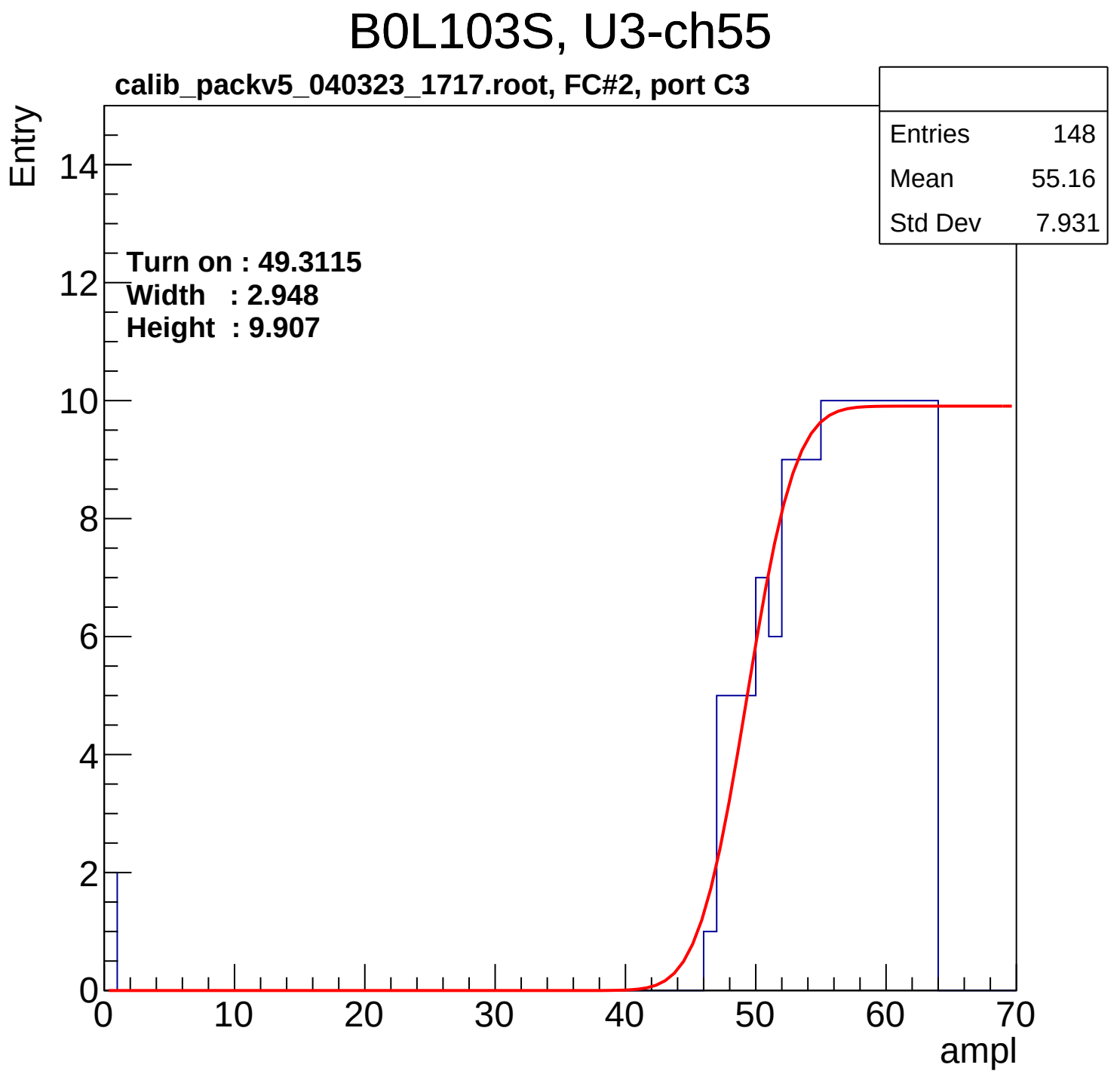
B0L103S, U3-ch55
calib_packv5_040323_1717.root, FC#2, port C3
Entries 148
Mean 55.16
Std Dev 7.931
Turn on : 49.3115
Width : 2.948
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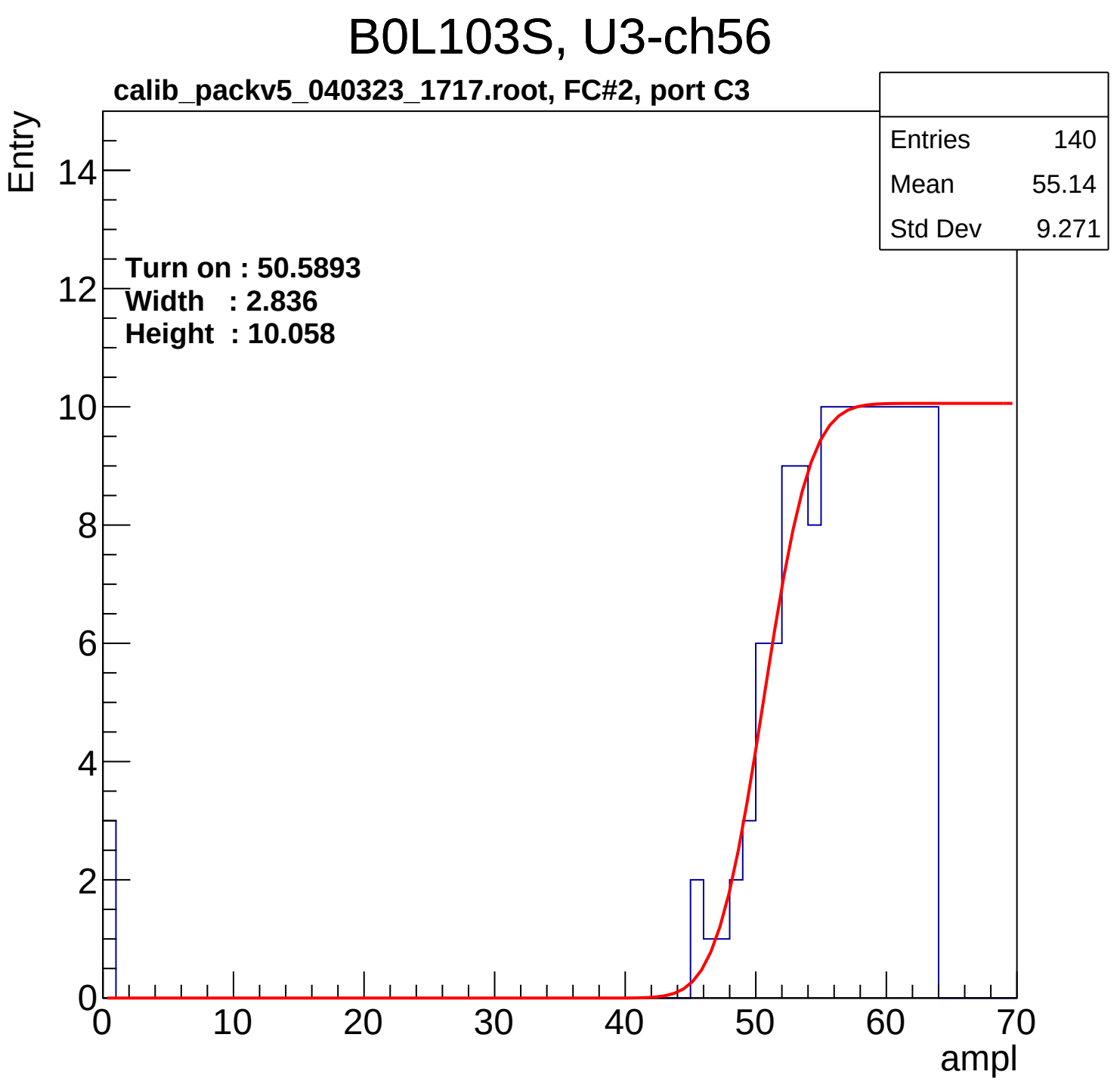
B0L103S, U3-ch56
calib_packv5_040323_1717.root, FC#2, port C3
Entries 140
Mean 55.14
Std Dev 9.271
Turn on : 50.5893
Width : 2.836
Height : 10.058
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ampl
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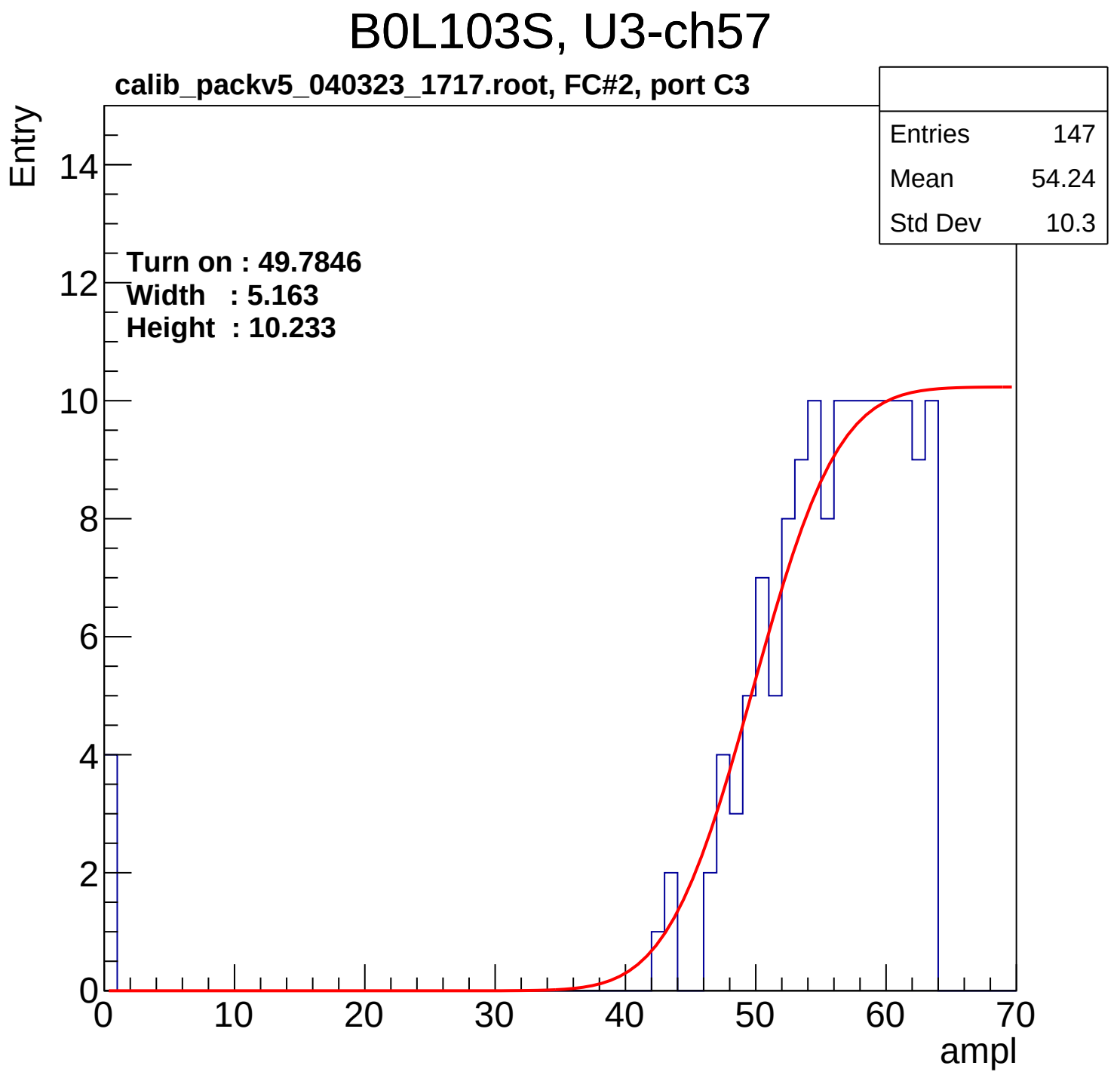
B0L103S, U3-ch57
calib_packv5_040323_1717.root, FC#2, port C3
Entries 147
Mean 54.24
Std Dev 10.3
Turn on : 49.7846
Width : 5.163
Height : 10.233
Entry
ampl
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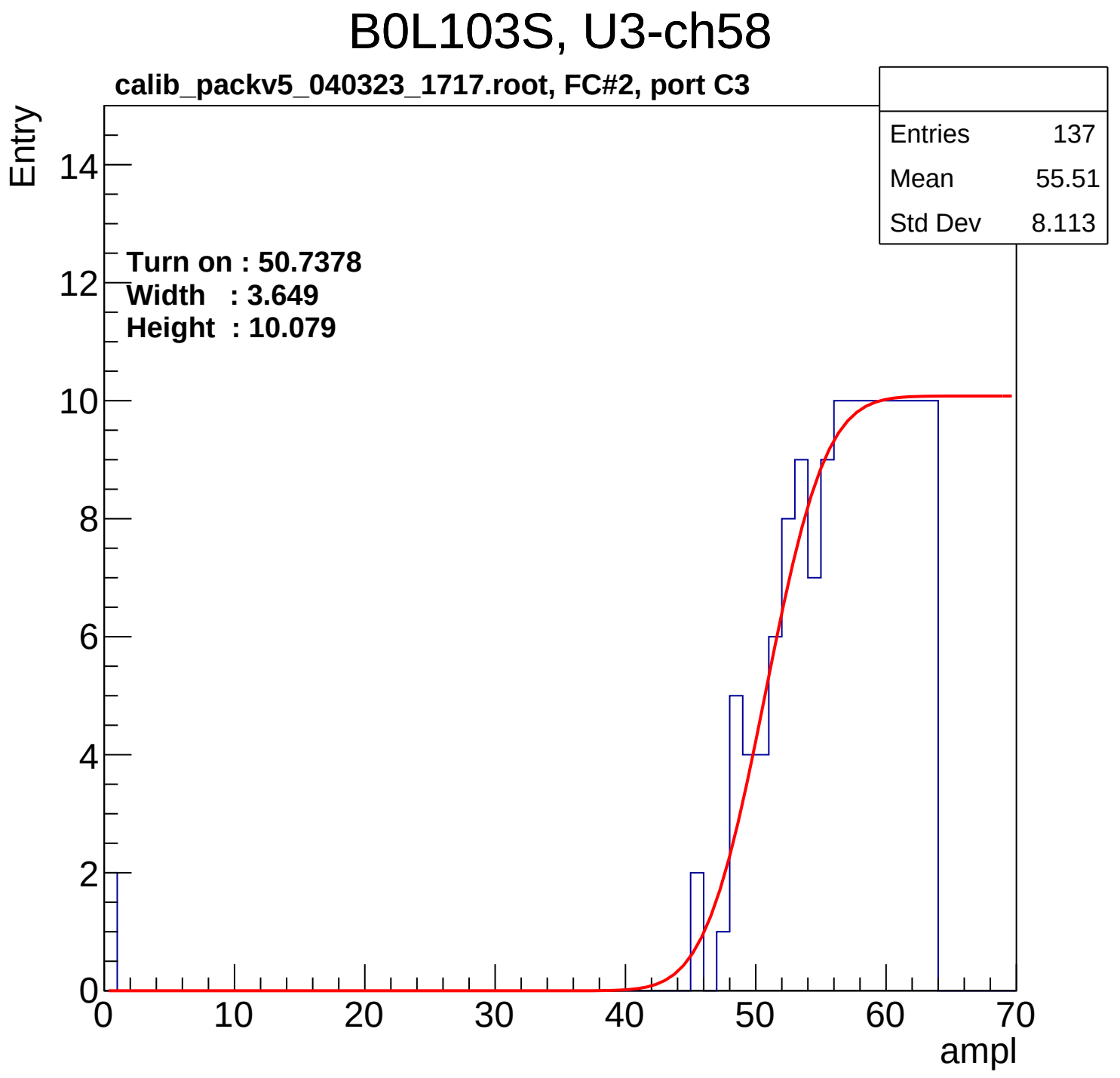
B0L103S, U3-ch58
calib_packv5_040323_1717.root, FC#2, port C3
Entries 137
Mean 55.51
Std Dev 8.113
Turn on : 50.7378
Width : 3.649
Height : 10.079
Entry
ampl
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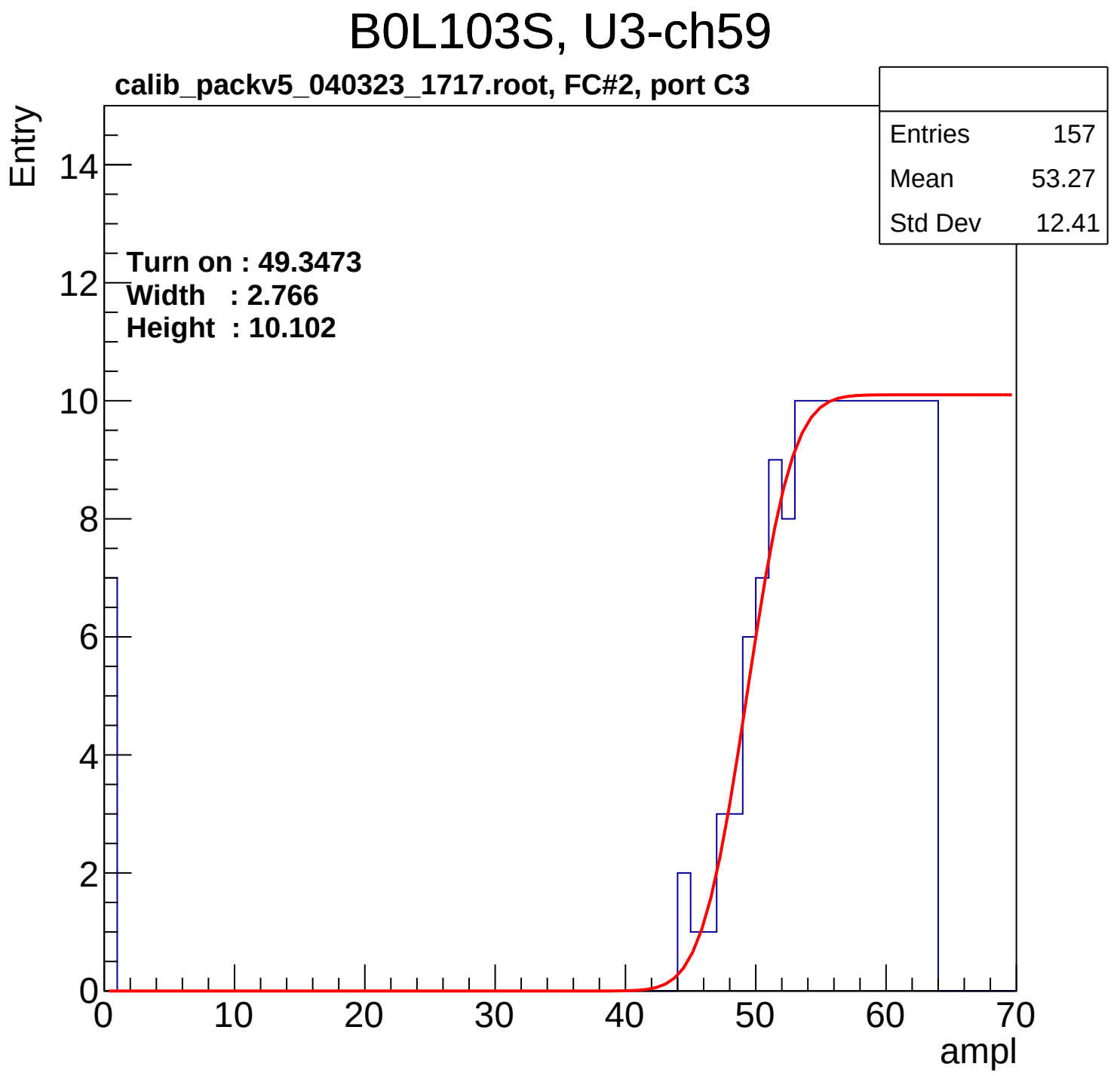
B0L103S, U3-ch59
calib_packv5_040323_1717.root, FC#2, port C3
Entries 157
Mean 53.27
Std Dev 12.41
Turn on : 49.3473
Width : 2.766
Height : 10.102
Entry
ampl
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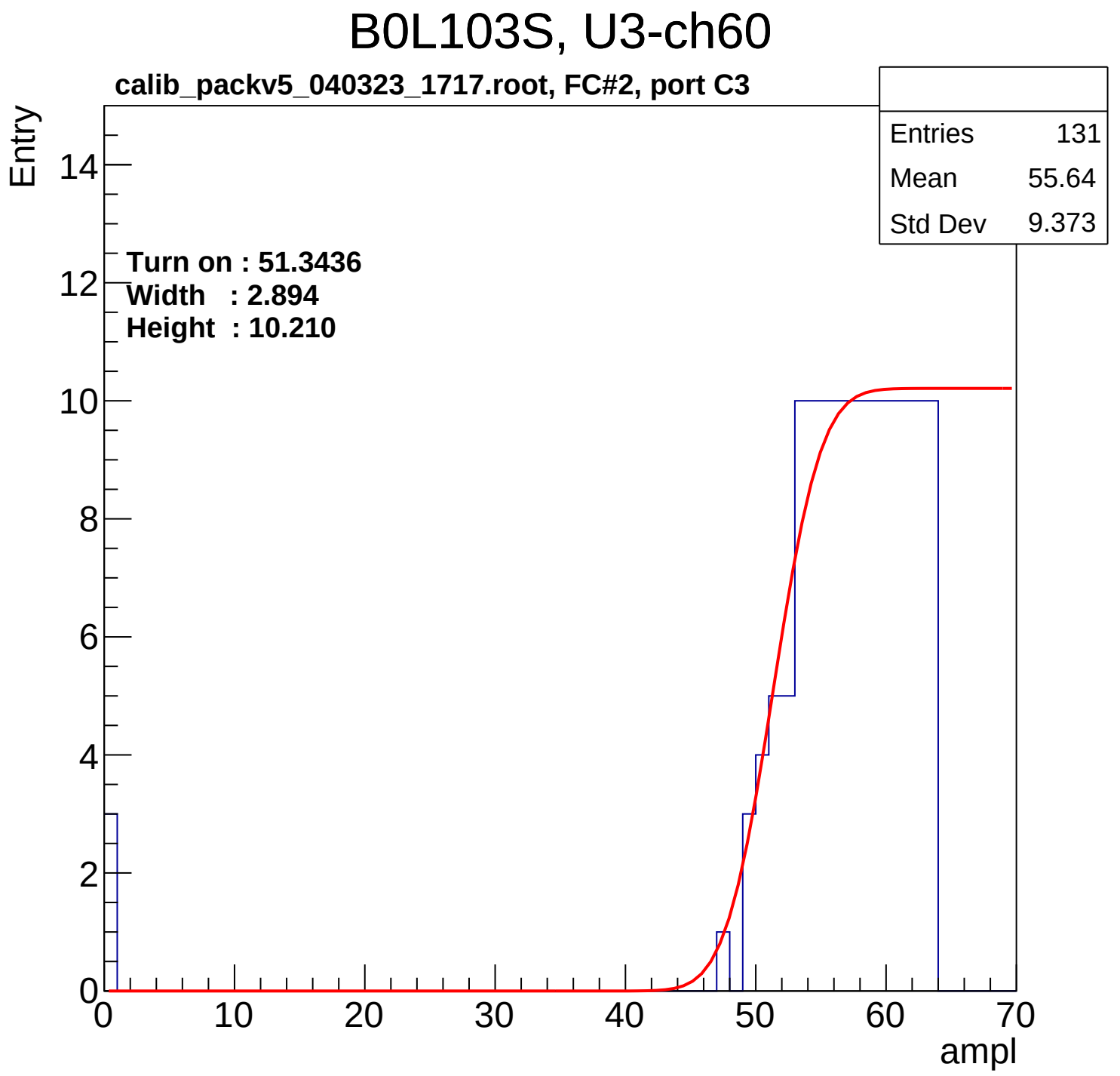
B0L103S, U3-ch60
calib_packv5_040323_1717.root, FC#2, port C3
Entries 131
Mean 55.64
Std Dev 9.373
Turn on : 51.3436
Width : 2.894
Height : 10.210
Entry
ampl
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2
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6
8
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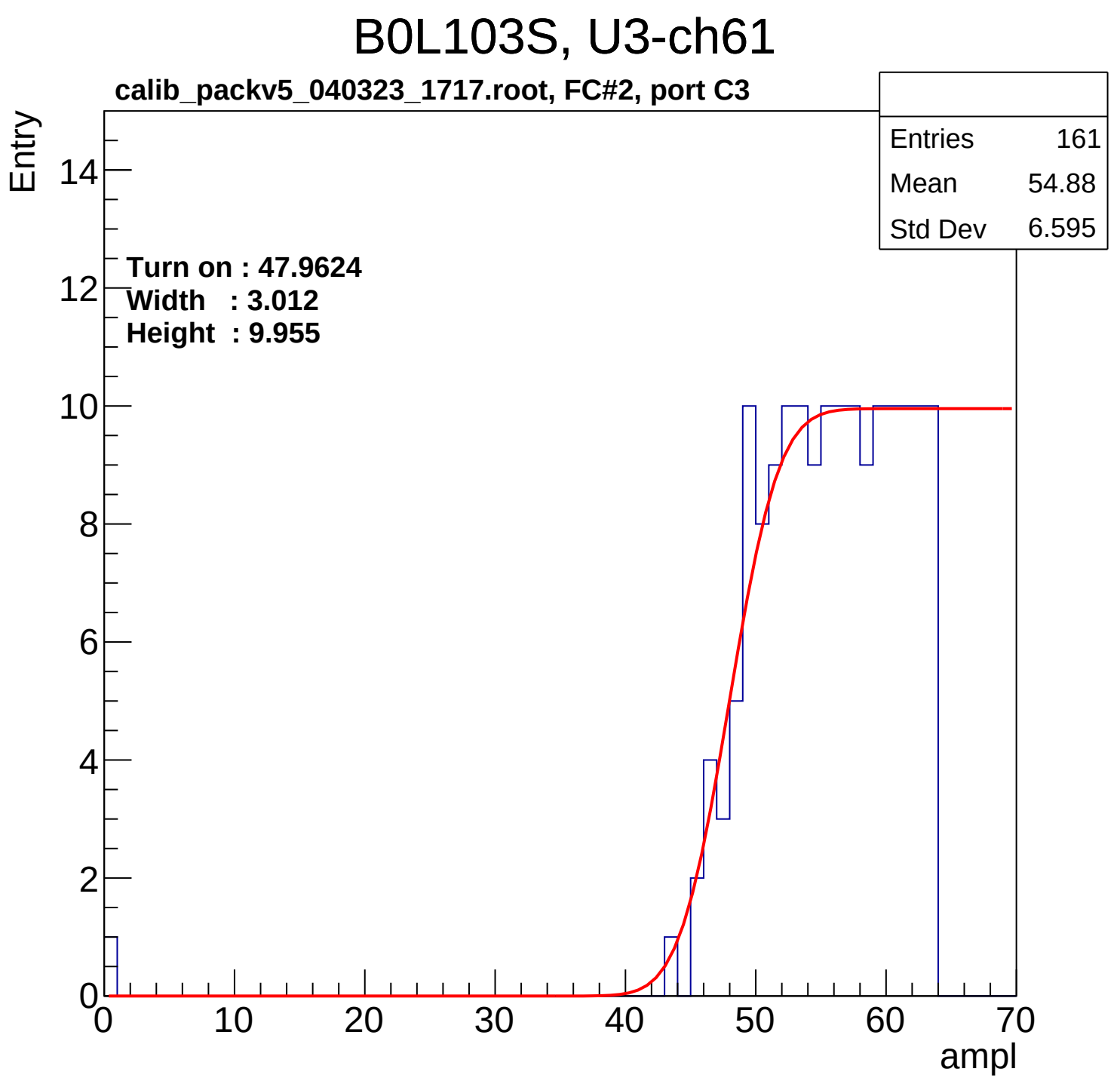
B0L103S, U3-ch61
calib_packv5_040323_1717.root, FC#2, port C3
Entries 161
Mean 54.88
Std Dev 6.595
Turn on : 47.9624
Width : 3.012
Height : 9.955
Entry
ampl
0
2
4
6
8
10
12
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0
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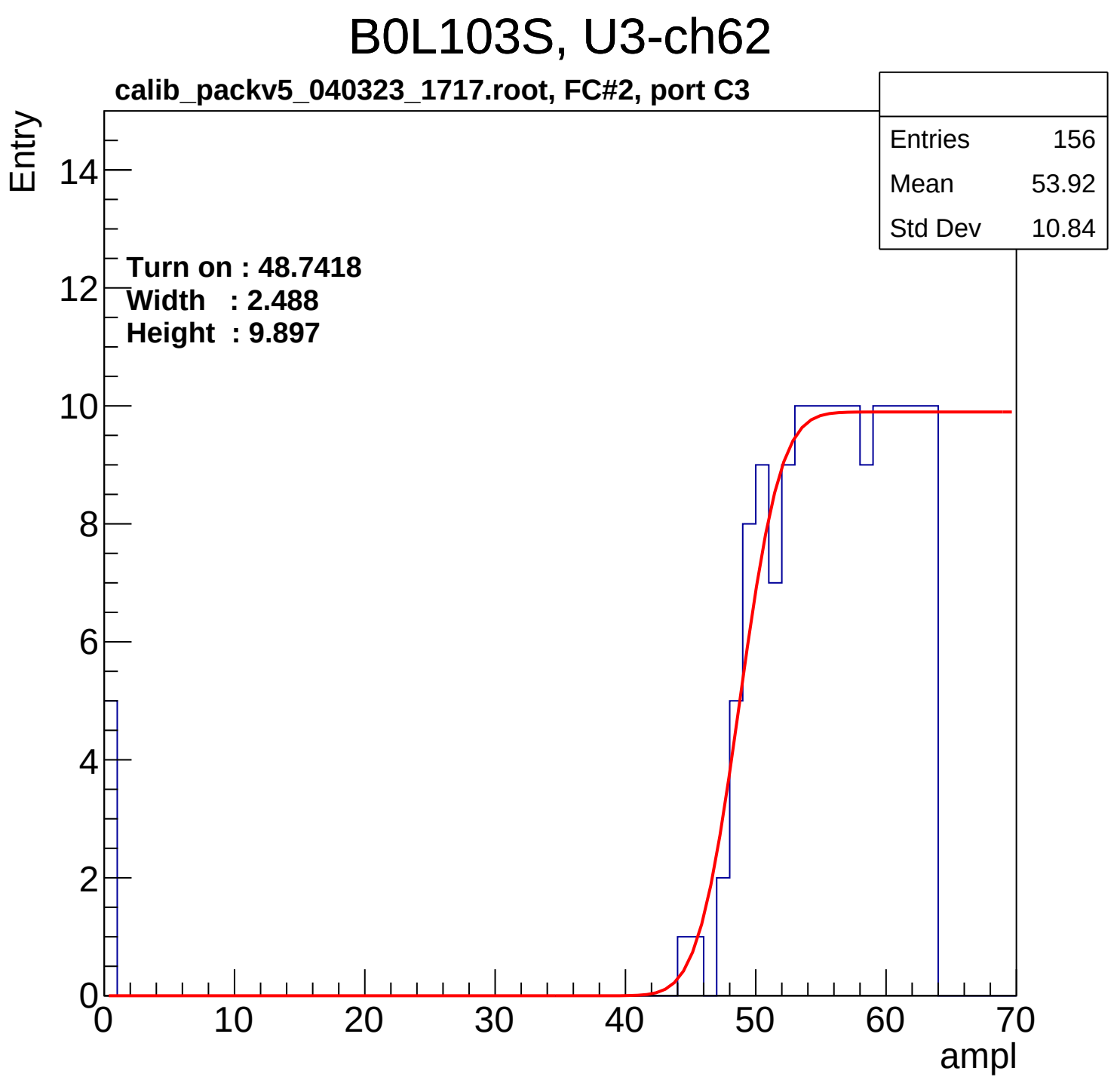
B0L103S, U3-ch62
calib_packv5_040323_1717.root, FC#2, port C3
Entries 156
Mean 53.92
Std Dev 10.84
Turn on : 48.7418
Width : 2.488
Height : 9.897
Entry
ampl
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2
4
6
8
10
12
14
0
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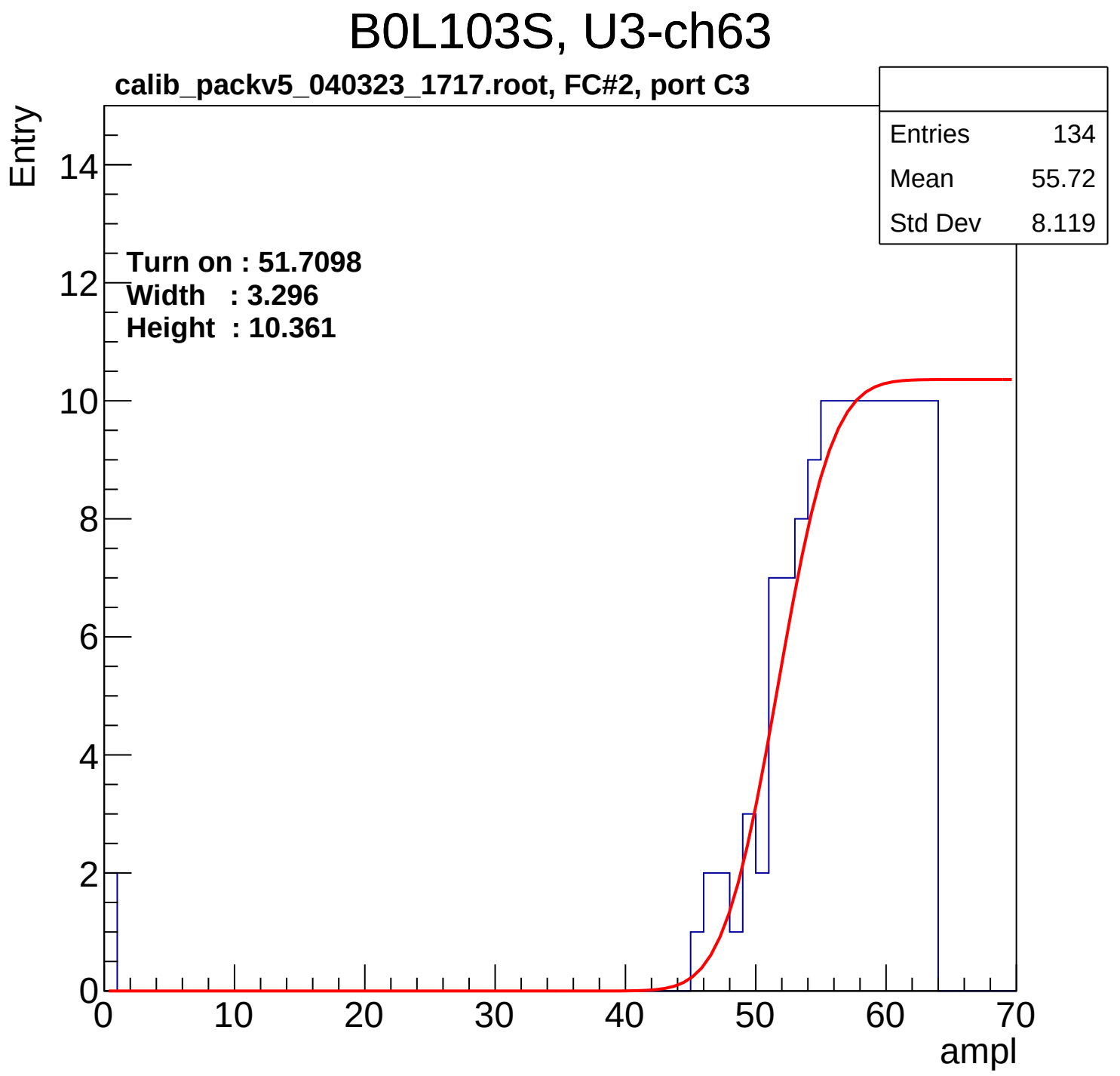
B0L103S, U3-ch63
calib_packv5_040323_1717.root, FC#2, port C3
Entries 134
Mean 55.72
Std Dev 8.119
Turn on : 51.7098
Width : 3.296
Height : 10.361
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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40
50
60
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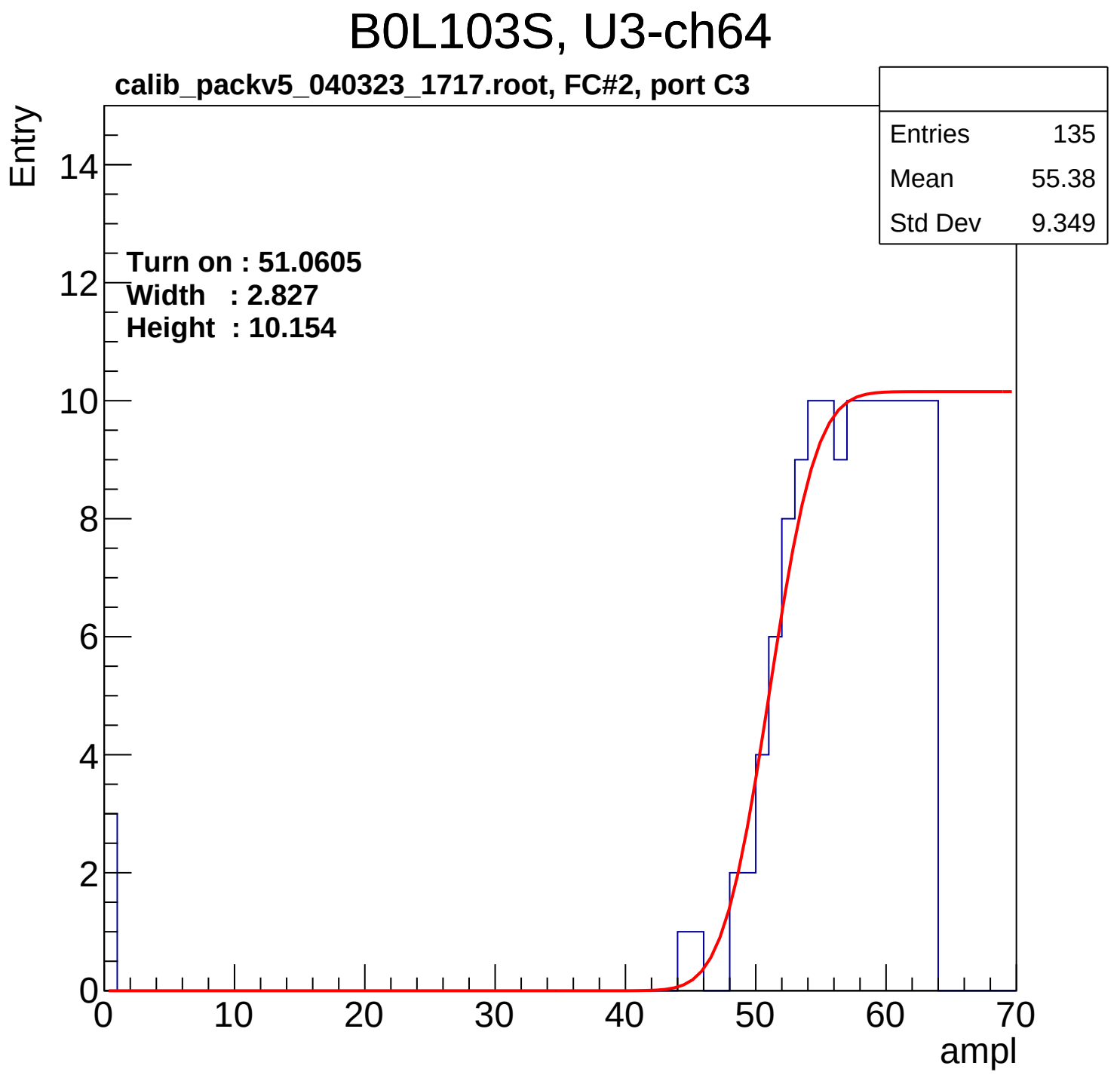
B0L103S, U3-ch64
calib_packv5_040323_1717.root, FC#2, port C3
Entries 135
Mean 55.38
Std Dev 9.349
Turn on : 51.0605
Width : 2.827
Height : 10.154
Entry
ampl
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2
4
6
8
10
12
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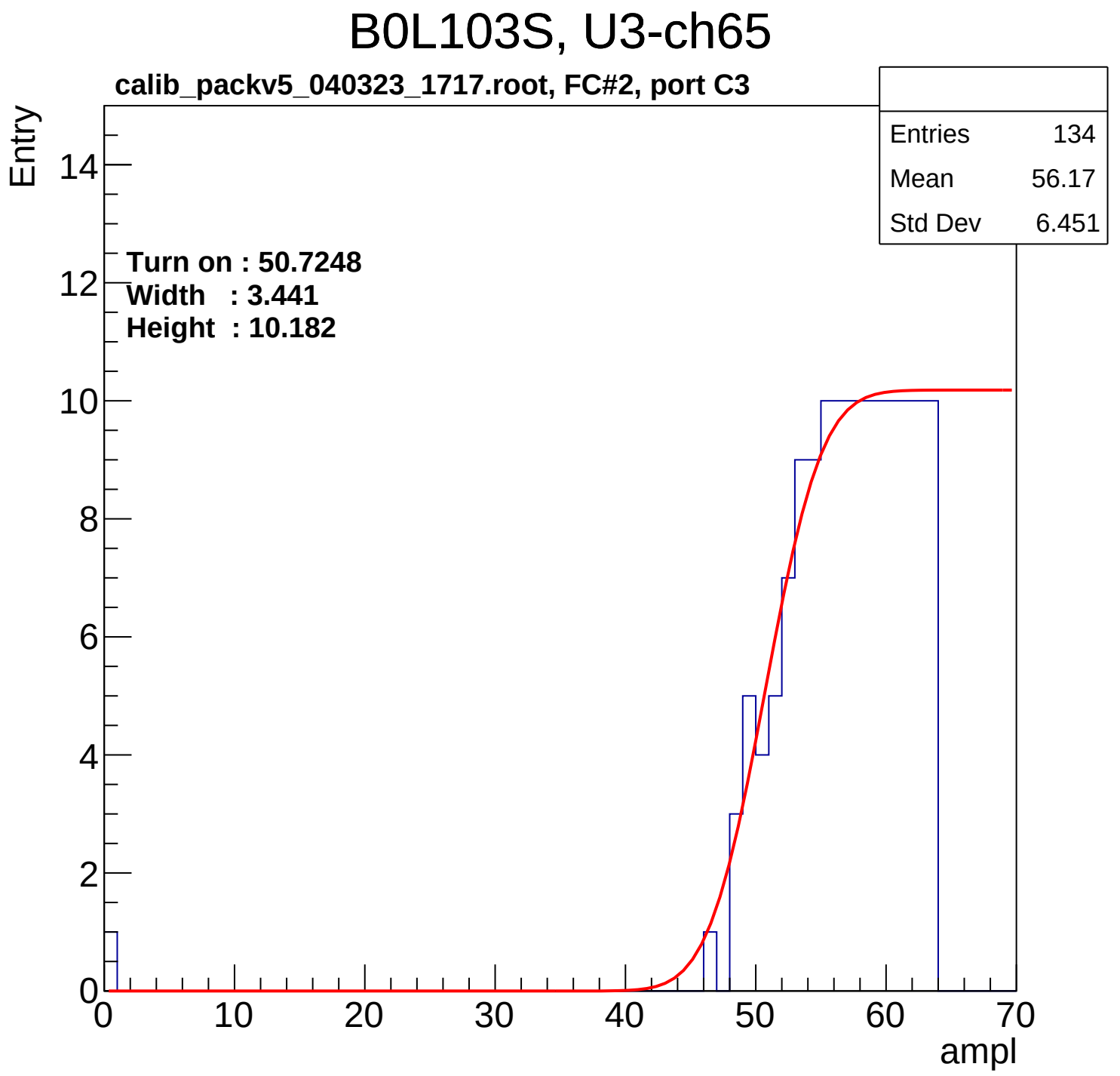
B0L103S, U3-ch65
calib_packv5_040323_1717.root, FC#2, port C3
Entries 134
Mean 56.17
Std Dev 6.451
Turn on : 50.7248
Width : 3.441
Height : 10.182
Entry
ampl
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2
4
6
8
10
12
14
0
10
20
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40
50
60
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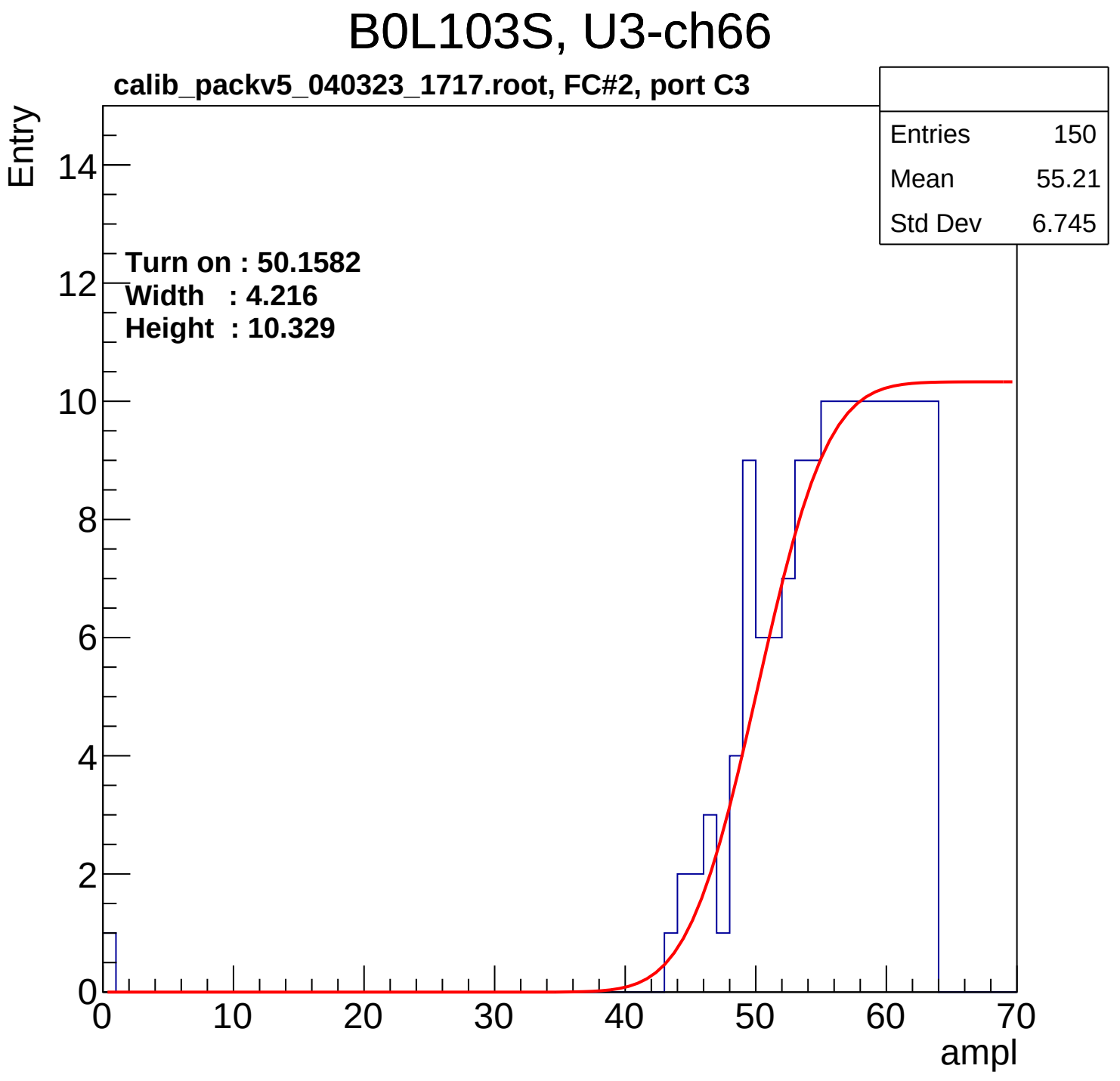
B0L103S, U3-ch66
calib_packv5_040323_1717.root, FC#2, port C3
Entries 150
Mean 55.21
Std Dev 6.745
Turn on : 50.1582
Width : 4.216
Height : 10.329
Entry
ampl
0
2
4
6
8
10
12
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0
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20
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40
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60
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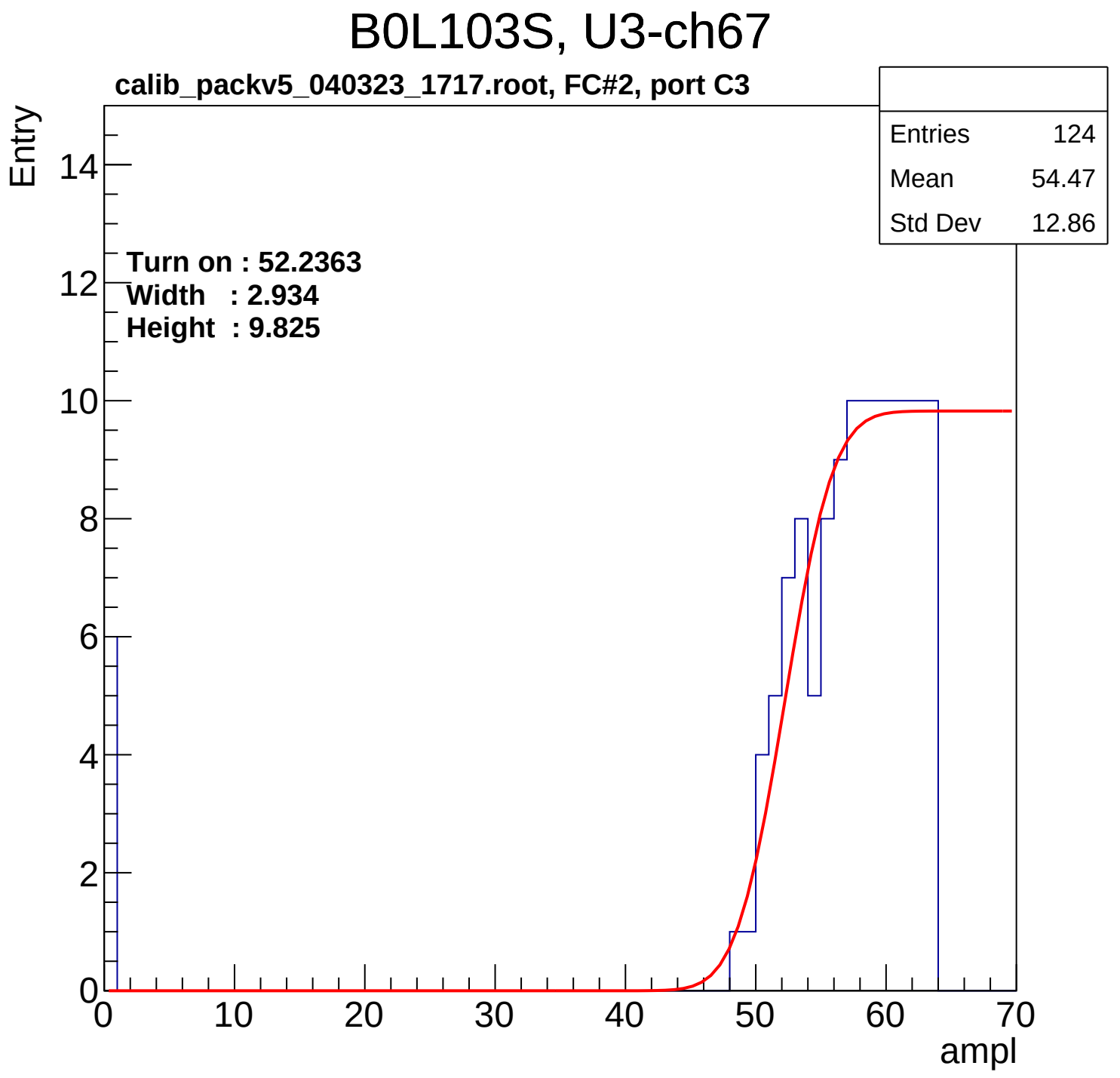
B0L103S, U3-ch67
calib_packv5_040323_1717.root, FC#2, port C3
Entries 124
Mean 54.47
Std Dev 12.86
Turn on : 52.2363
Width : 2.934
Height : 9.825
Entry
ampl
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2
4
6
8
10
12
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0
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20
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40
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60
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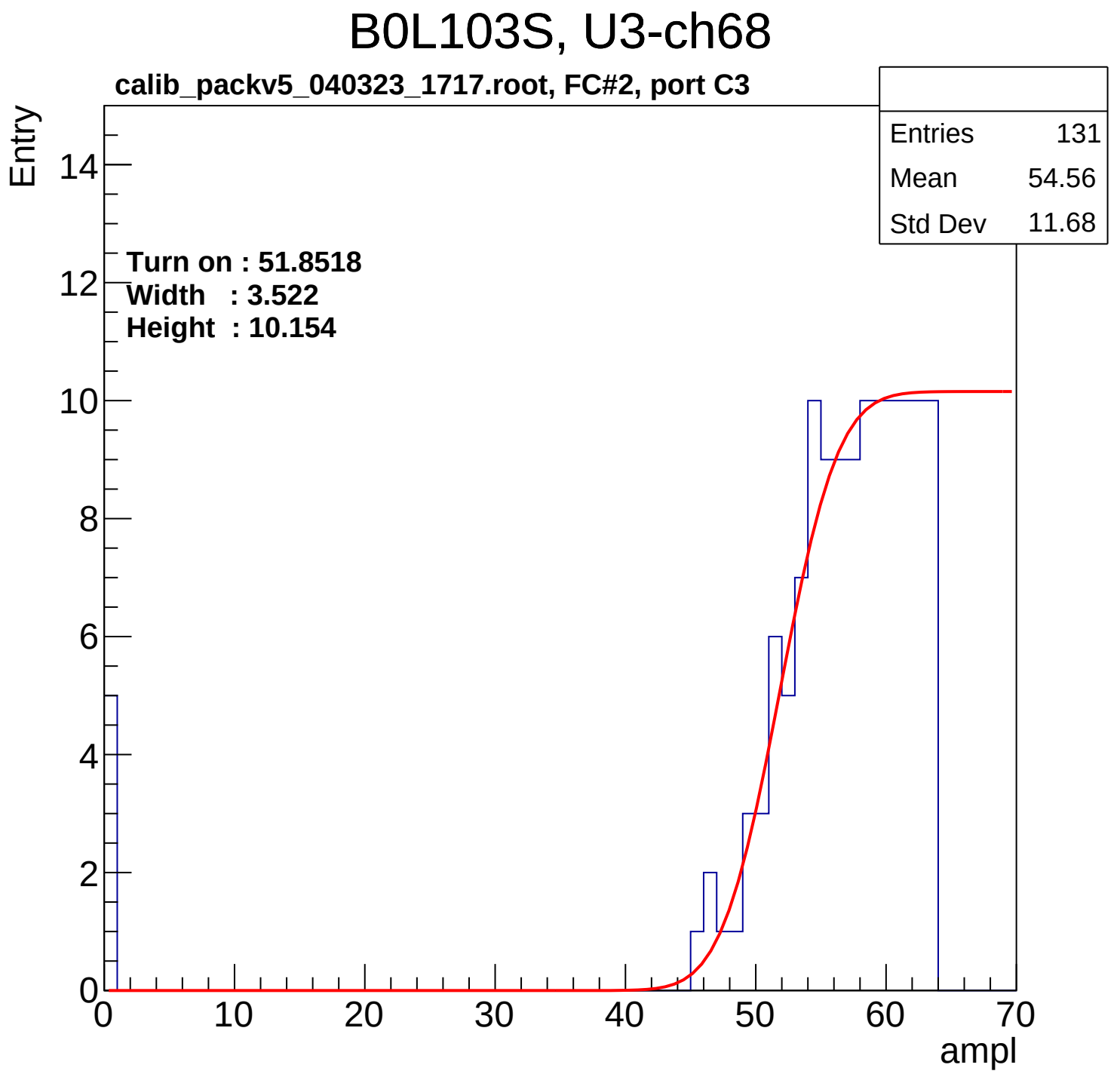
B0L103S, U3-ch68
calib_packv5_040323_1717.root, FC#2, port C3
Entries 131
Mean 54.56
Std Dev 11.68
Turn on : 51.8518
Width : 3.522
Height : 10.154
Entry
ampl
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4
6
8
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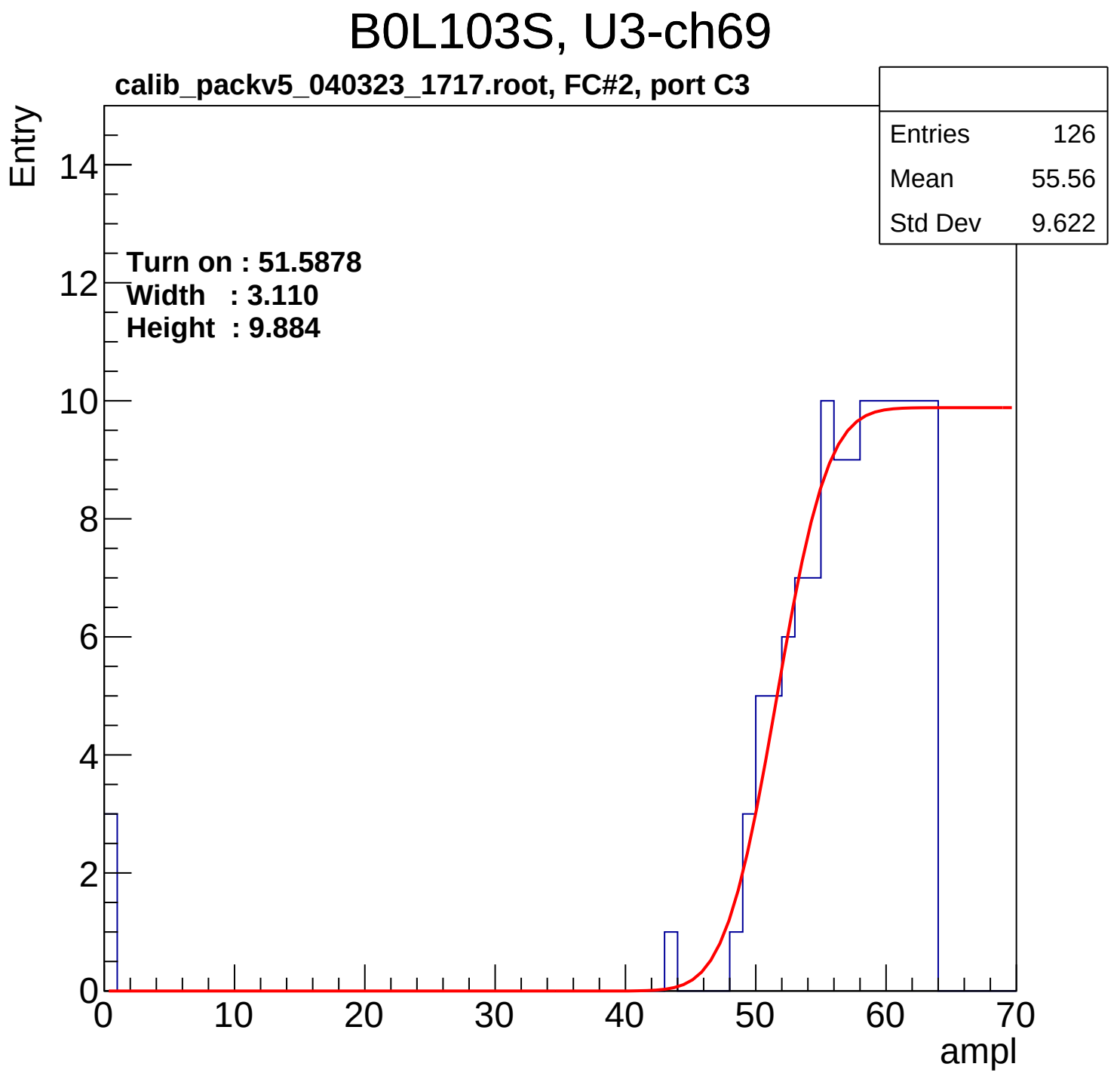
B0L103S, U3-ch69
calib_packv5_040323_1717.root, FC#2, port C3
Entries 126
Mean 55.56
Std Dev 9.622
Turn on : 51.5878
Width : 3.110
Height : 9.884
Entry
ampl
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6
8
10
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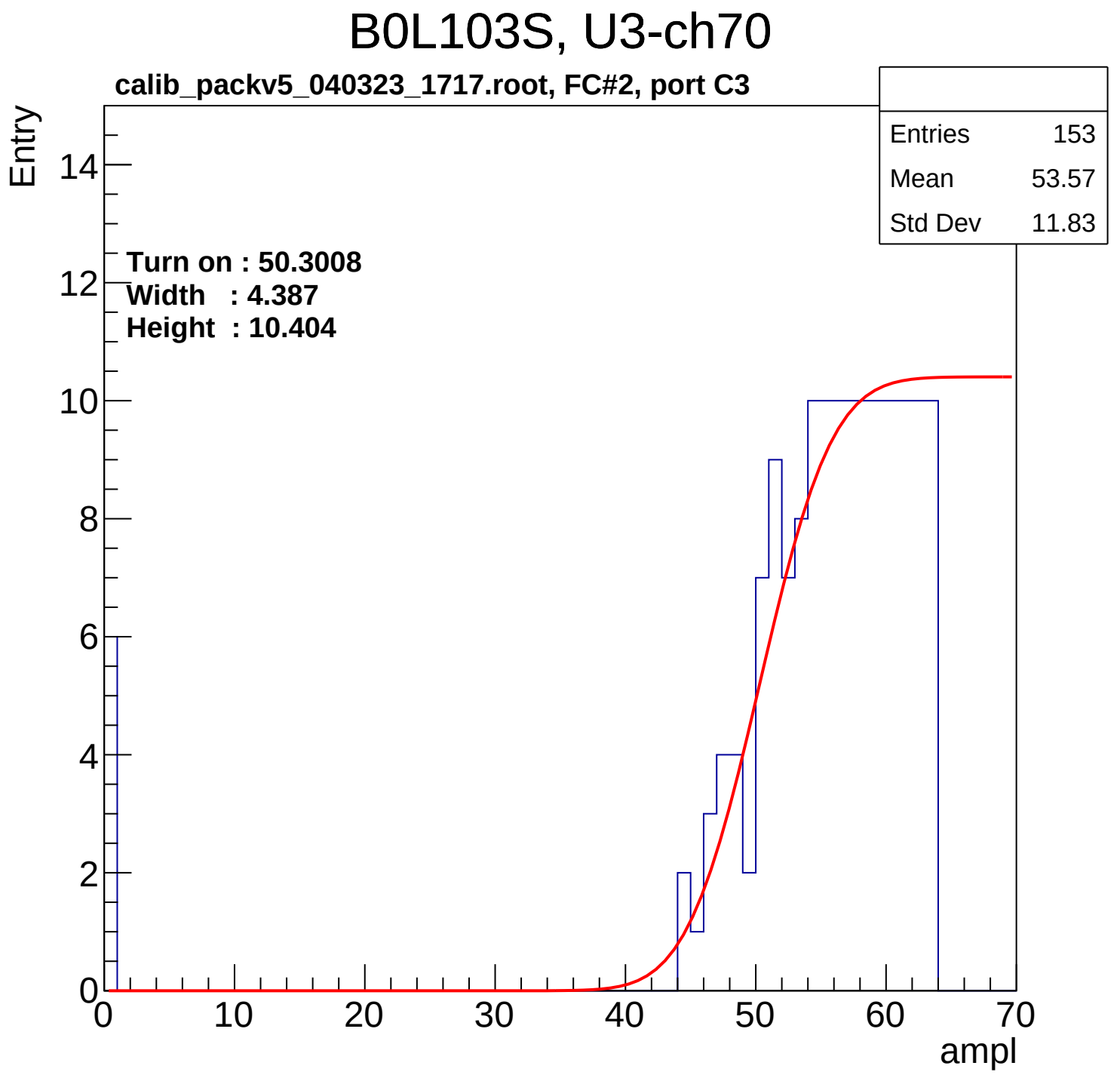
B0L103S, U3-ch70
calib_packv5_040323_1717.root, FC#2, port C3
Entries 153
Mean 53.57
Std Dev 11.83
Turn on : 50.3008
Width : 4.387
Height : 10.404
Entry
ampl
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8
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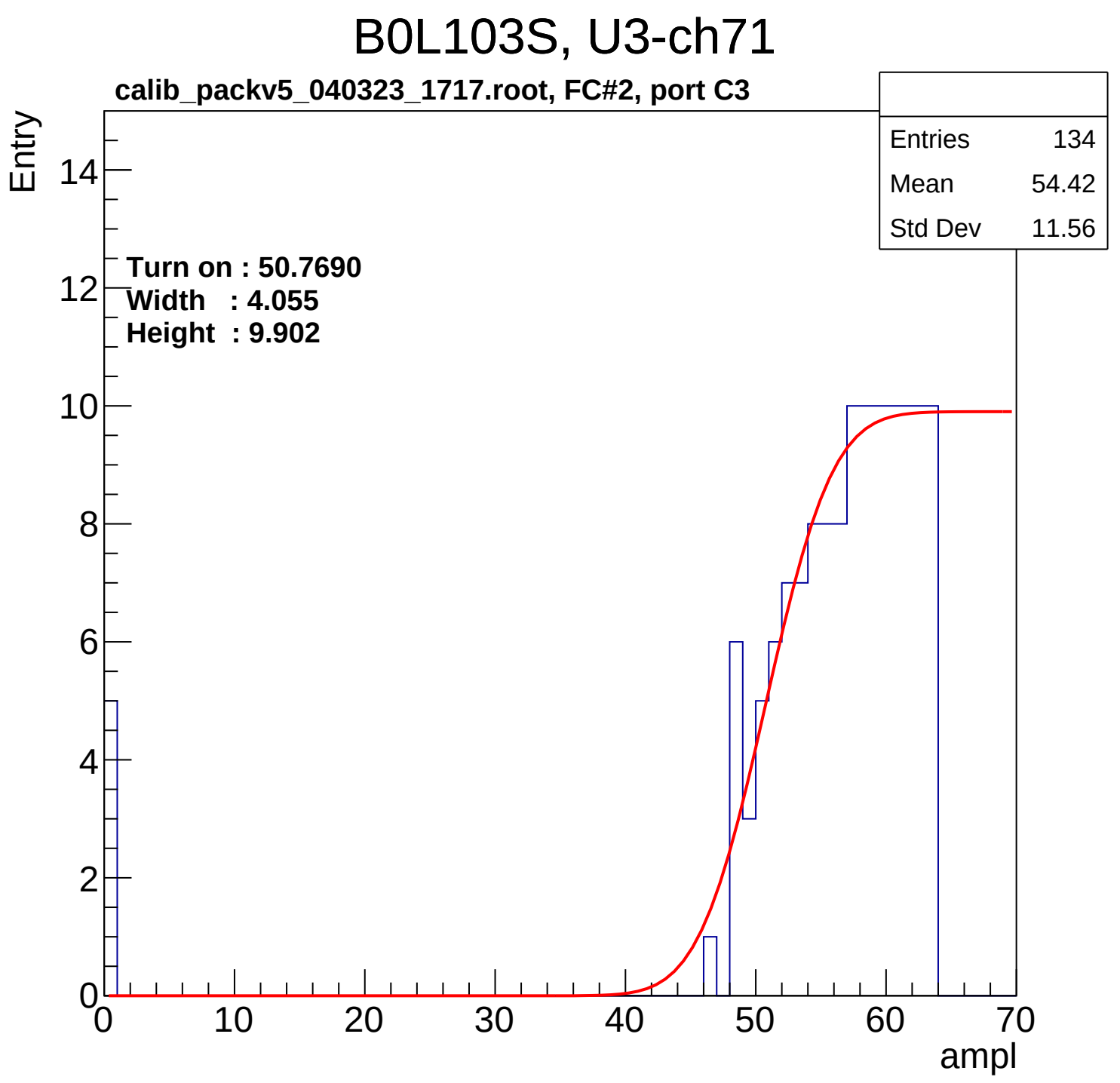
B0L103S, U3-ch71
calib_packv5_040323_1717.root, FC#2, port C3
Entries 134
Mean 54.42
Std Dev 11.56
Turn on : 50.7690
Width : 4.055
Height : 9.902
Entry
ampl
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4
6
8
10
12
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20
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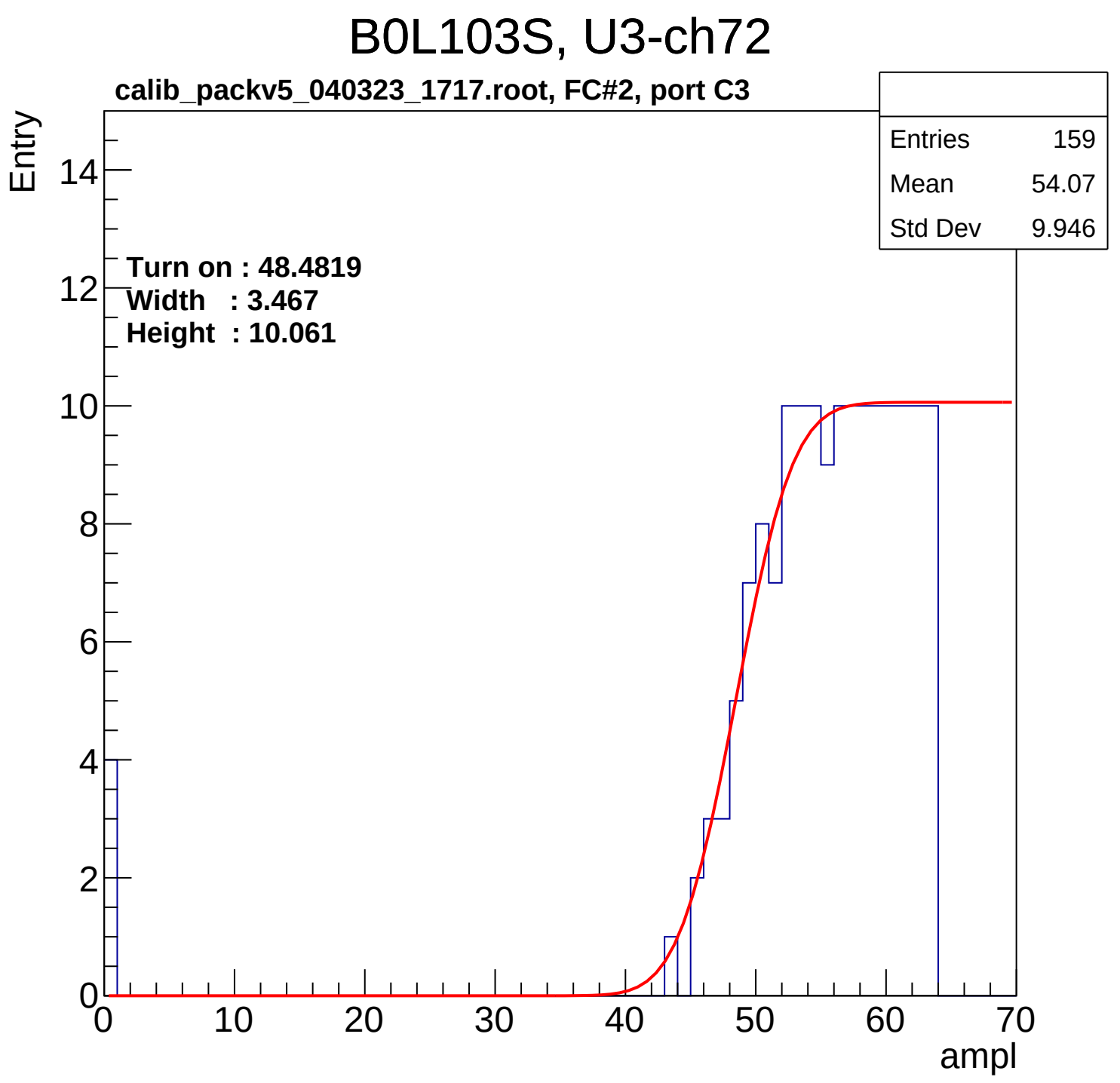
B0L103S, U3-ch72
calib_packv5_040323_1717.root, FC#2, port C3
Entries 159
Mean 54.07
Std Dev 9.946
Turn on : 48.4819
Width : 3.467
Height : 10.061
Entry
ampl
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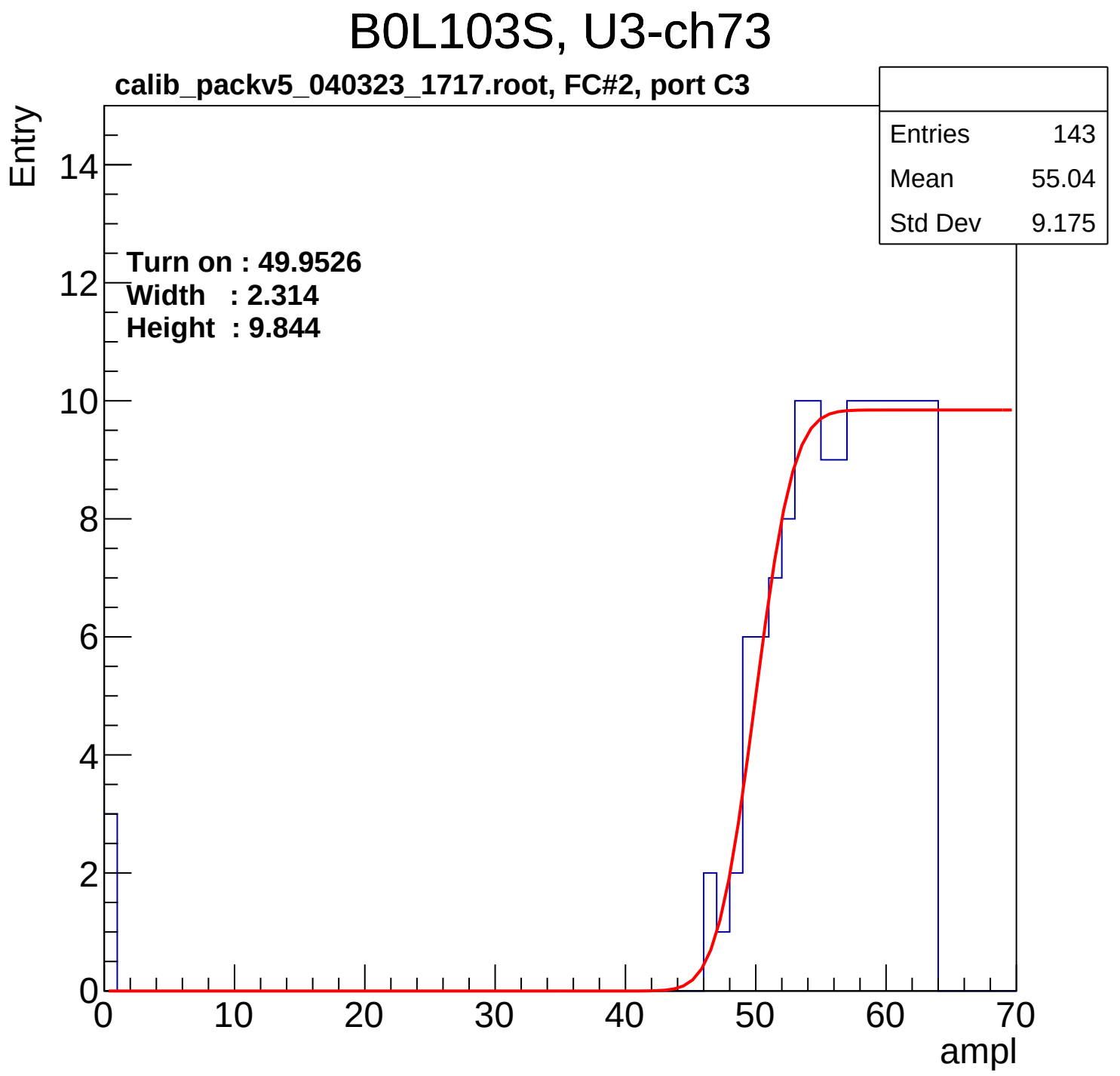
B0L103S, U3-ch73
calib_packv5_040323_1717.root, FC#2, port C3
Entries 143
Mean 55.04
Std Dev 9.175
Turn on : 49.9526
Width : 2.314
Height : 9.844
Entry
ampl
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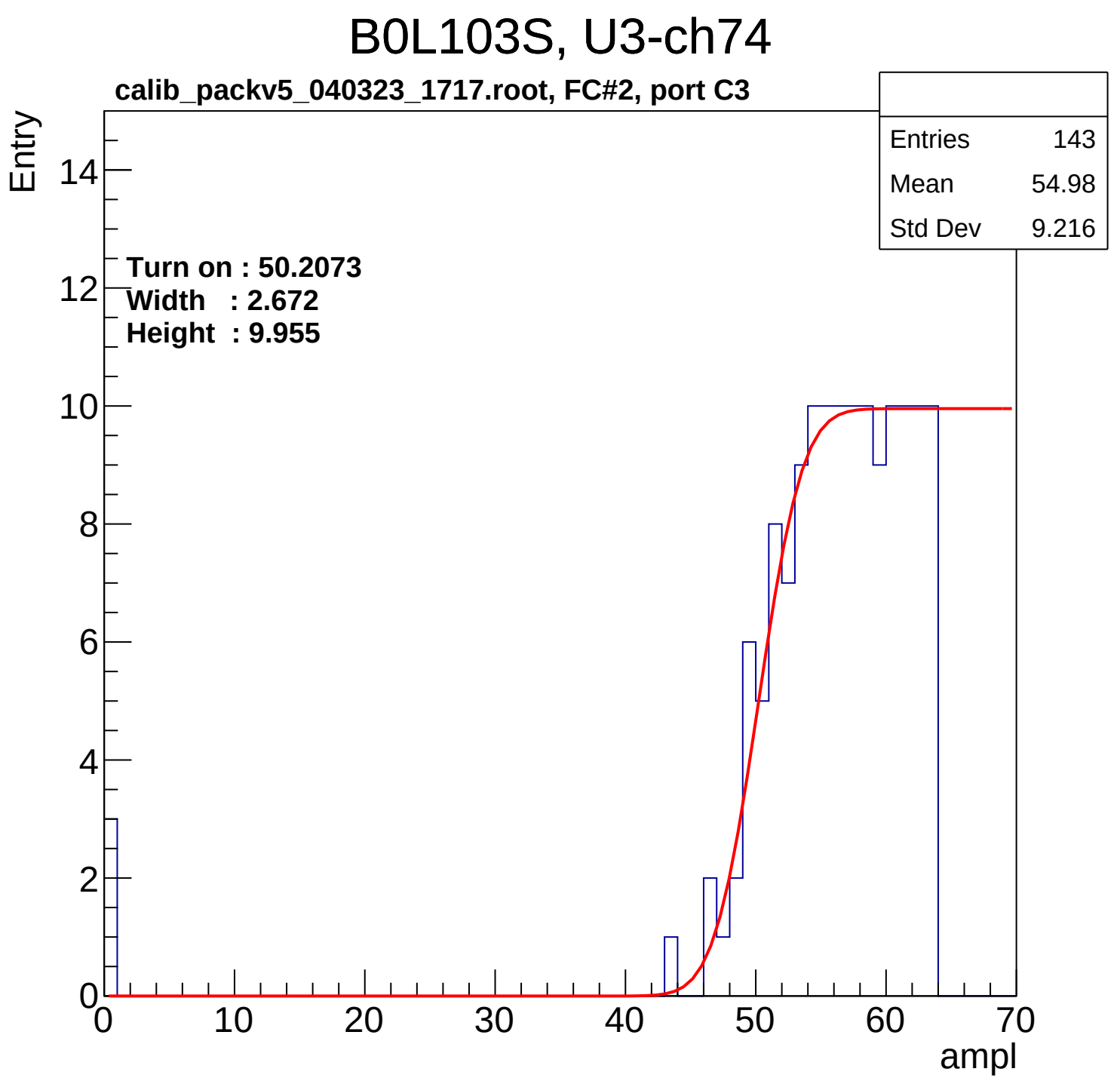
B0L103S, U3-ch74
calib_packv5_040323_1717.root, FC#2, port C3
Entries 143
Mean 54.98
Std Dev 9.216
Turn on : 50.2073
Width : 2.672
Height : 9.955
Entry
ampl
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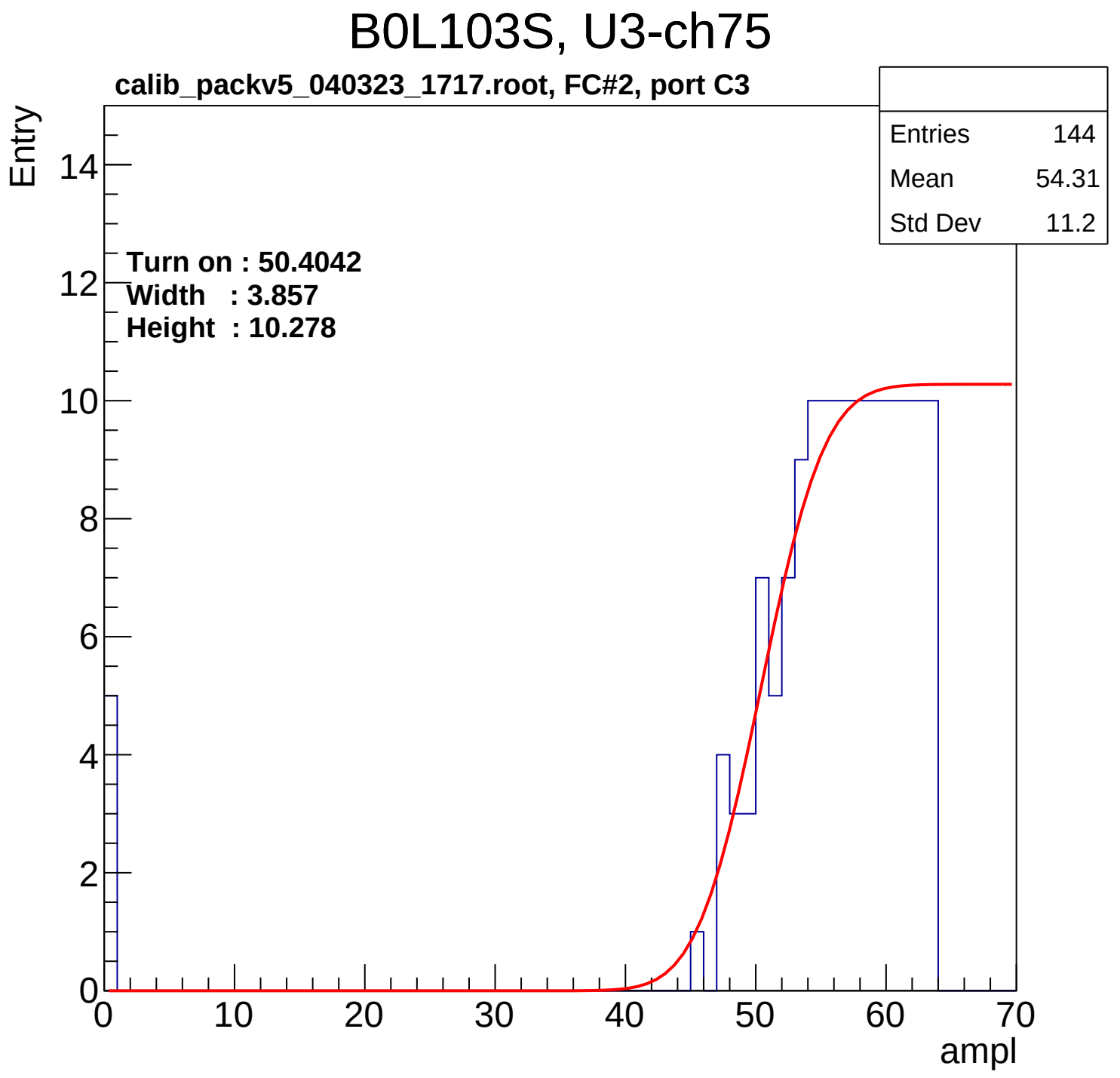
B0L103S, U3-ch75
calib_packv5_040323_1717.root, FC#2, port C3
Entries 144
Mean 54.31
Std Dev 11.2
Turn on : 50.4042
Width : 3.857
Height : 10.278
Entry
ampl
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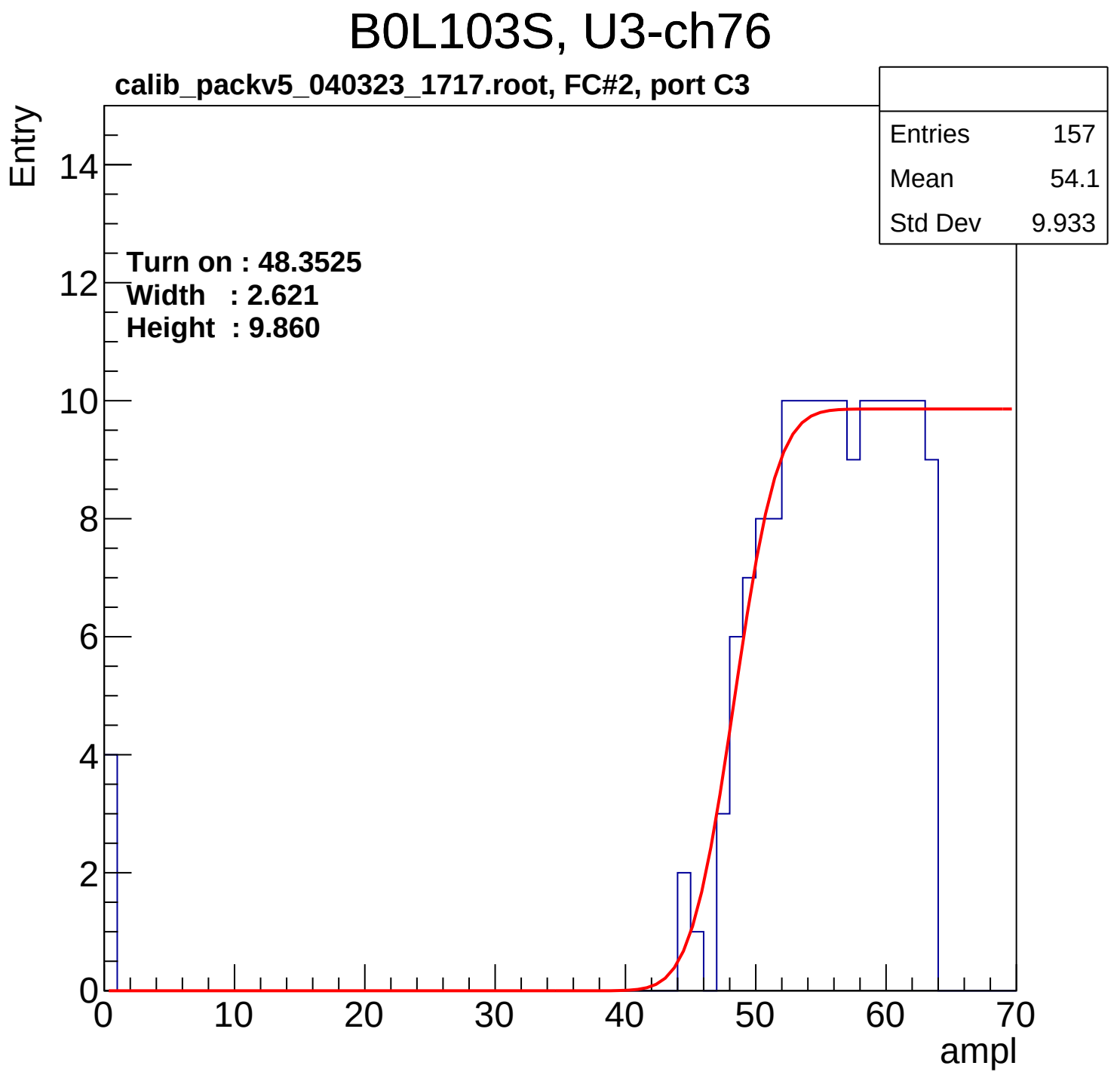
B0L103S, U3-ch76
calib_packv5_040323_1717.root, FC#2, port C3
Entries 157
Mean 54.1
Std Dev 9.933
Turn on : 48.3525
Width : 2.621
Height : 9.860
Entry
ampl
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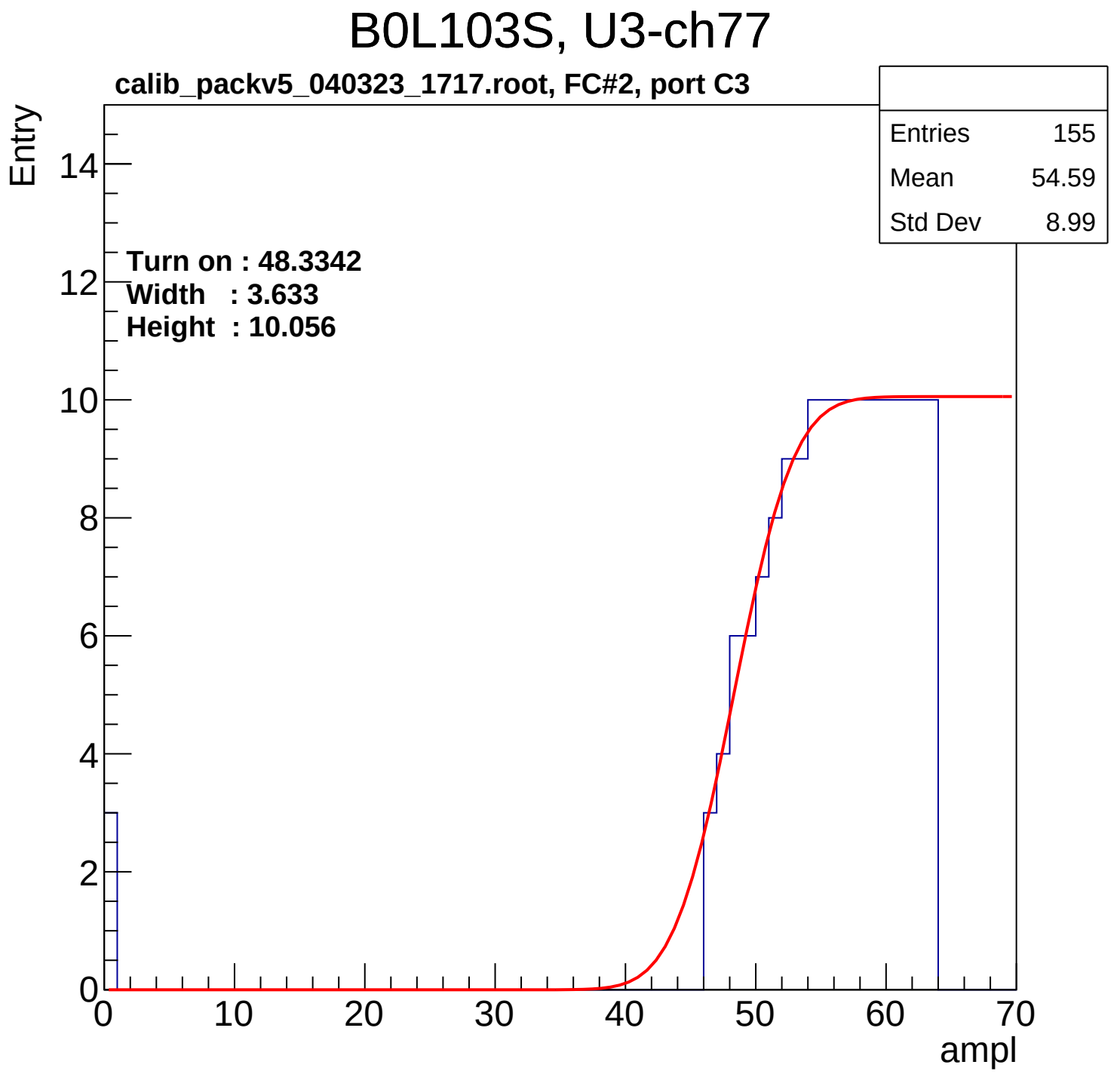
B0L103S, U3-ch77
calib_packv5_040323_1717.root, FC#2, port C3
Entries 155
Mean 54.59
Std Dev 8.99
Turn on : 48.3342
Width : 3.633
Height : 10.056
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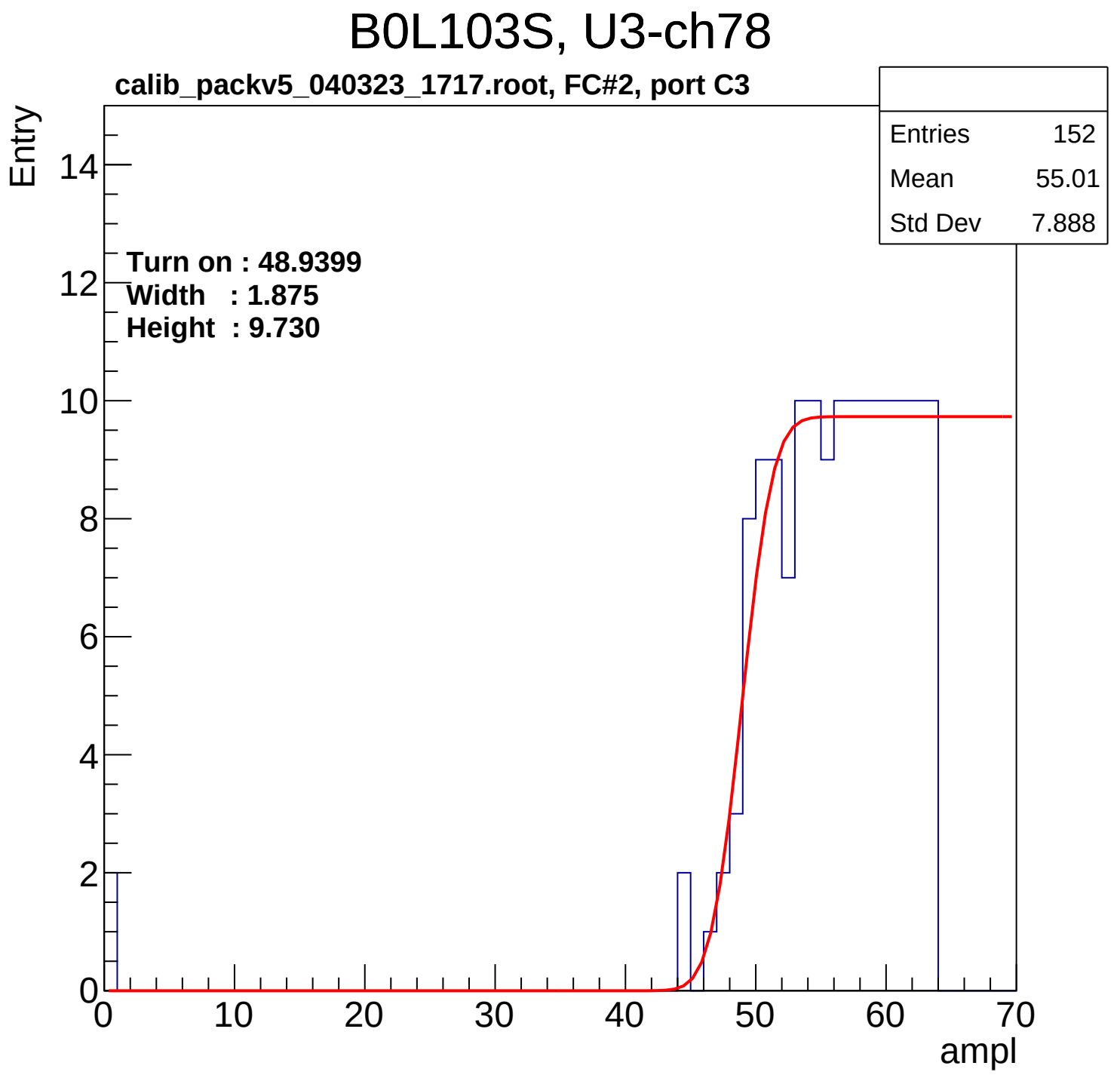
B0L103S, U3-ch78
calib_packv5_040323_1717.root, FC#2, port C3
Entries 152
Mean 55.01
Std Dev 7.888
Turn on : 48.9399
Width : 1.875
Height : 9.730
Entry
ampl
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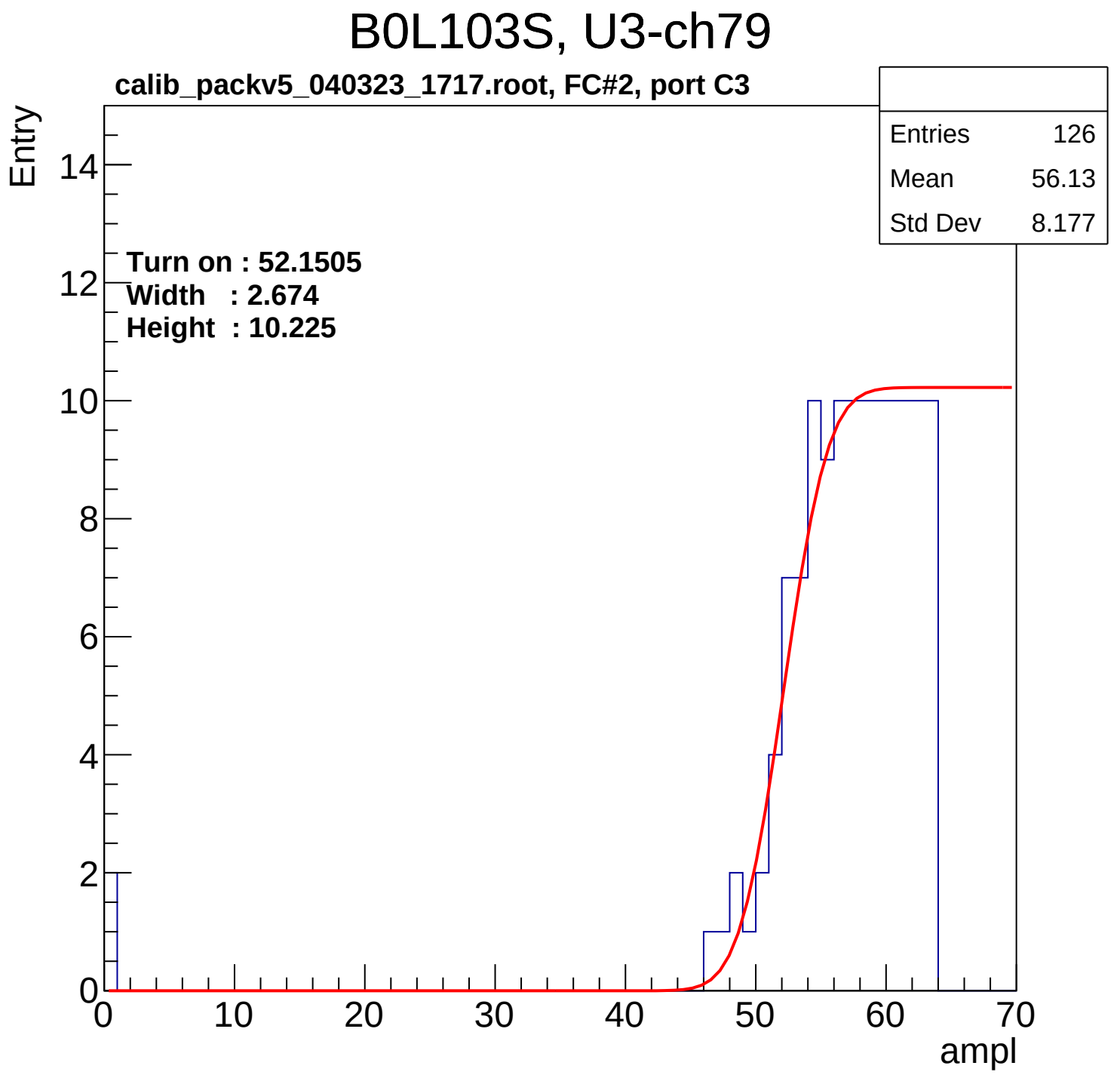
B0L103S, U3-ch79
calib_packv5_040323_1717.root, FC#2, port C3
Entries 126
Mean 56.13
Std Dev 8.177
Turn on : 52.1505
Width : 2.674
Height : 10.225
Entry
ampl
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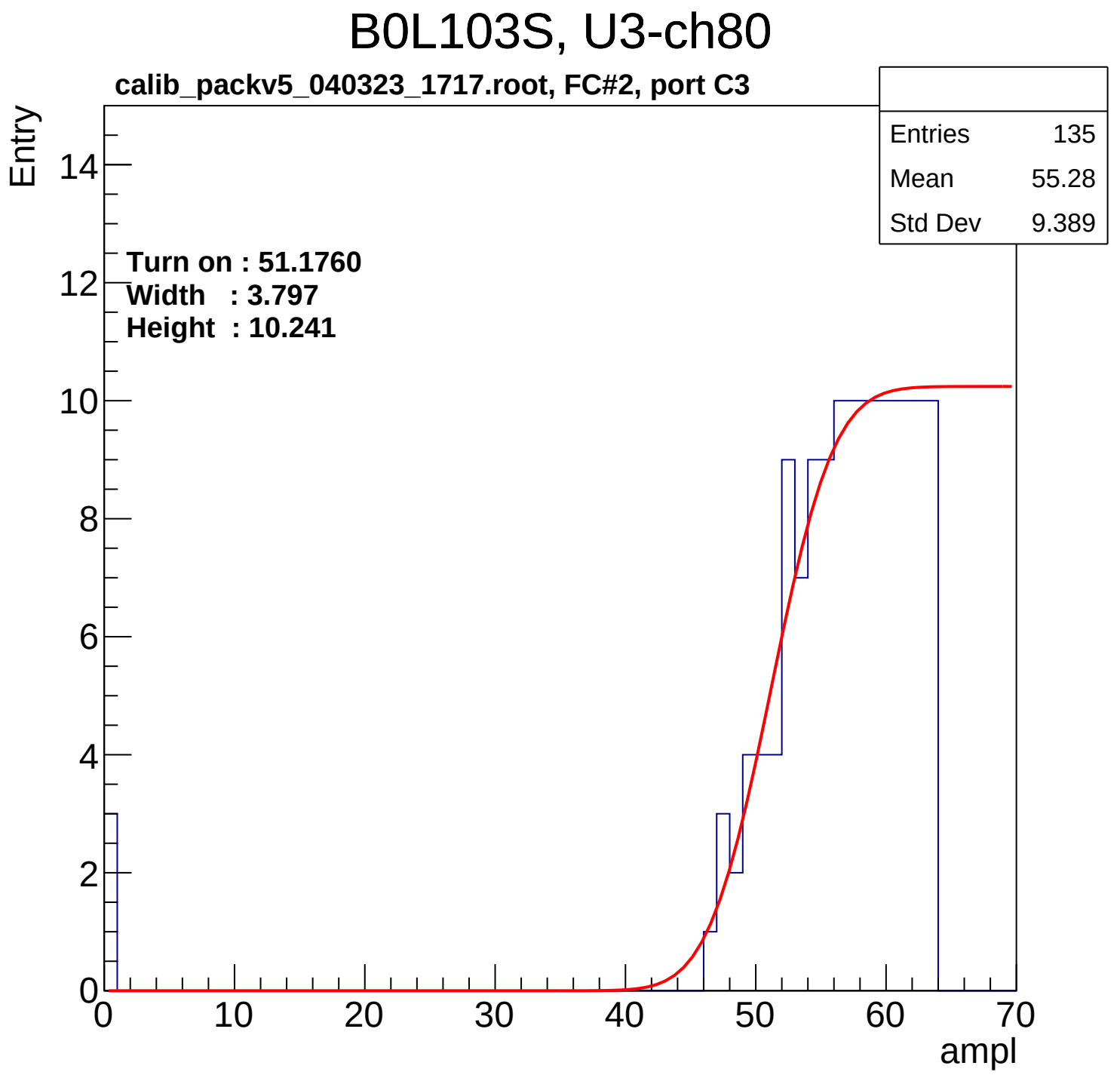
B0L103S, U3-ch80
calib_packv5_040323_1717.root, FC#2, port C3
Entries 135
Mean 55.28
Std Dev 9.389
Turn on : 51.1760
Width : 3.797
Height : 10.241
Entry
ampl
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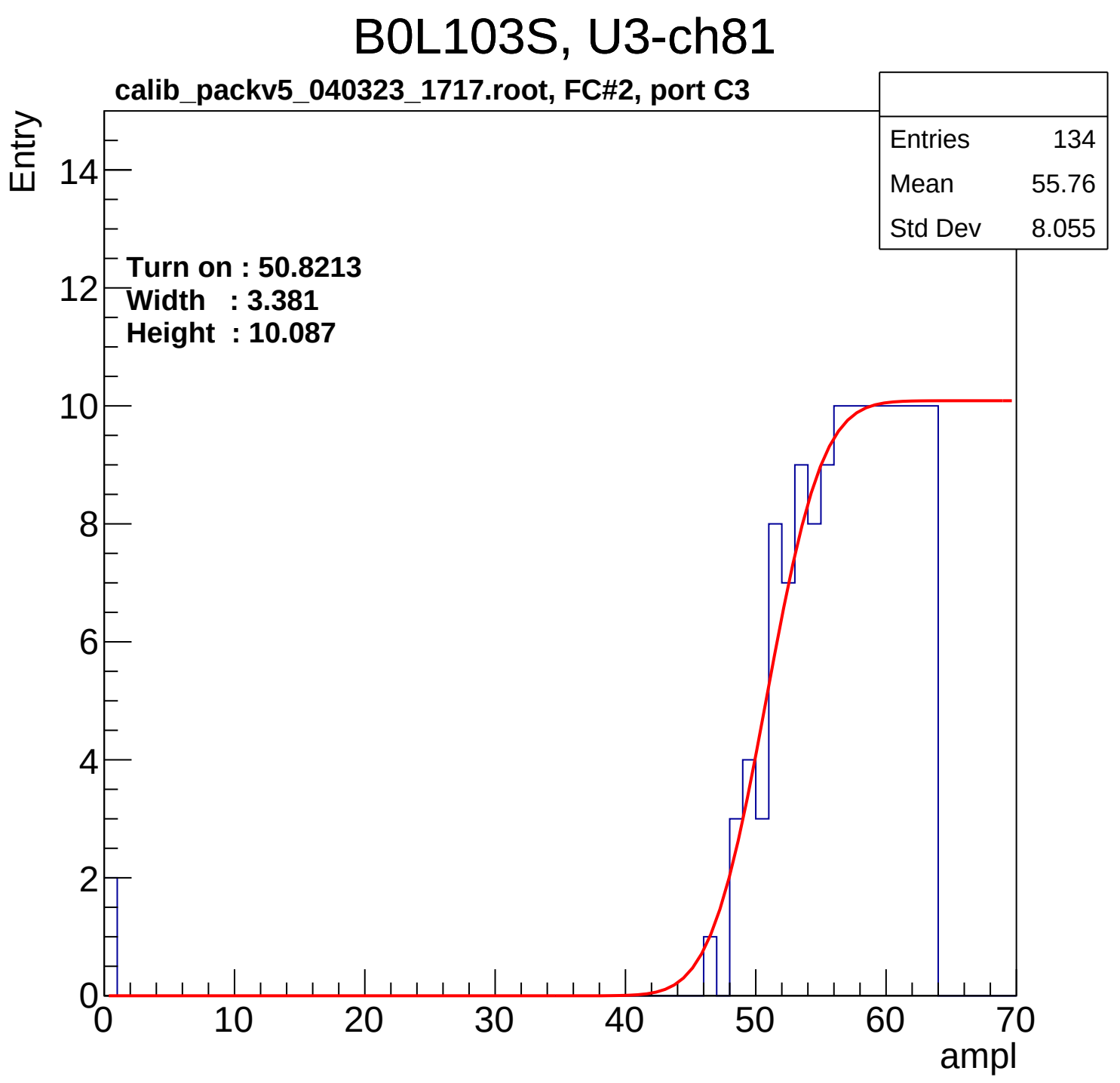
B0L103S, U3-ch81
calib_packv5_040323_1717.root, FC#2, port C3
Entries 134
Mean 55.76
Std Dev 8.055
Turn on : 50.8213
Width : 3.381
Height : 10.087
Entry
ampl
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4
6
8
10
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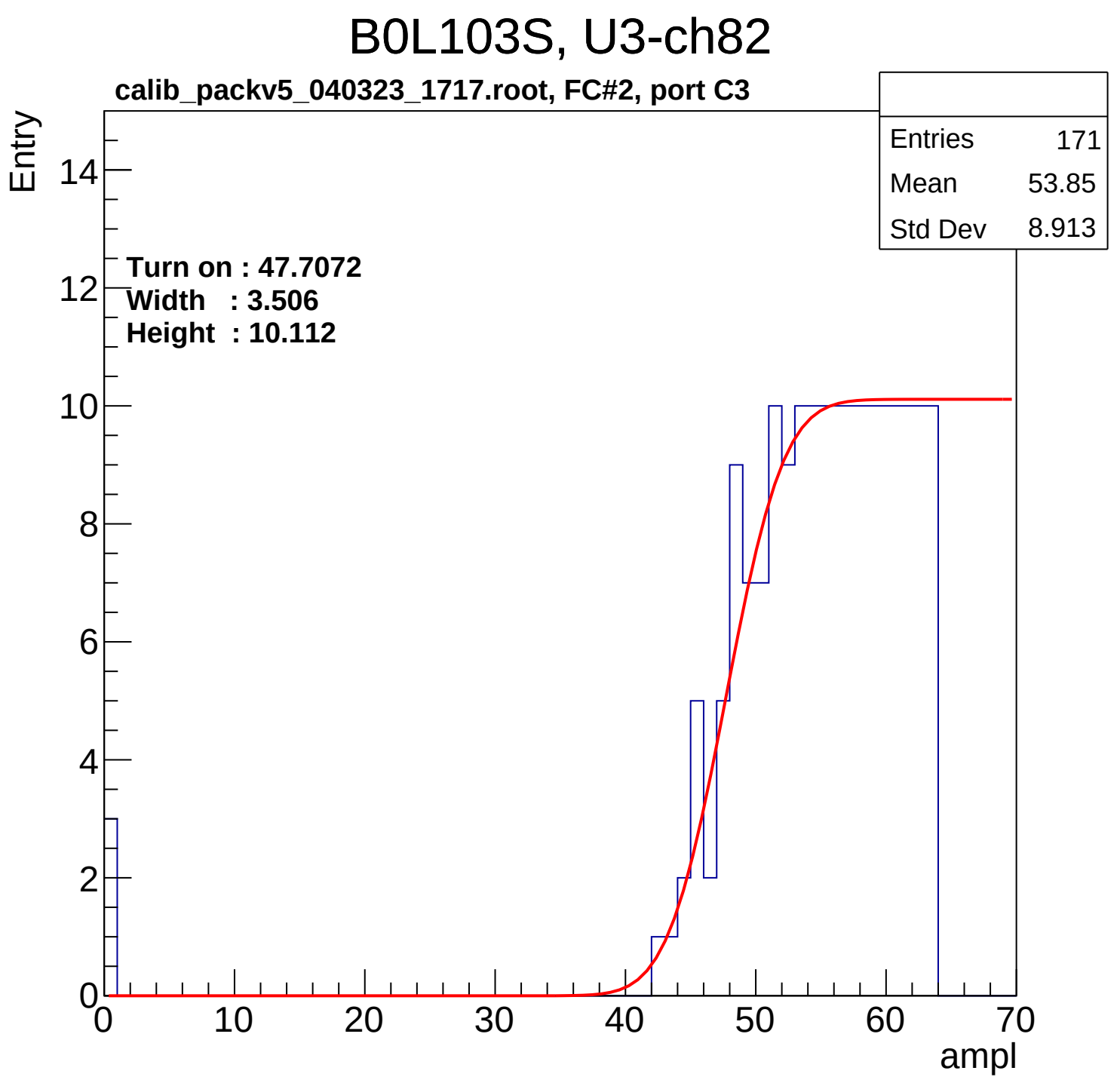
B0L103S, U3-ch82
calib_packv5_040323_1717.root, FC#2, port C3
Entries 171
Mean 53.85
Std Dev 8.913
Turn on : 47.7072
Width : 3.506
Height : 10.112
Entry
ampl
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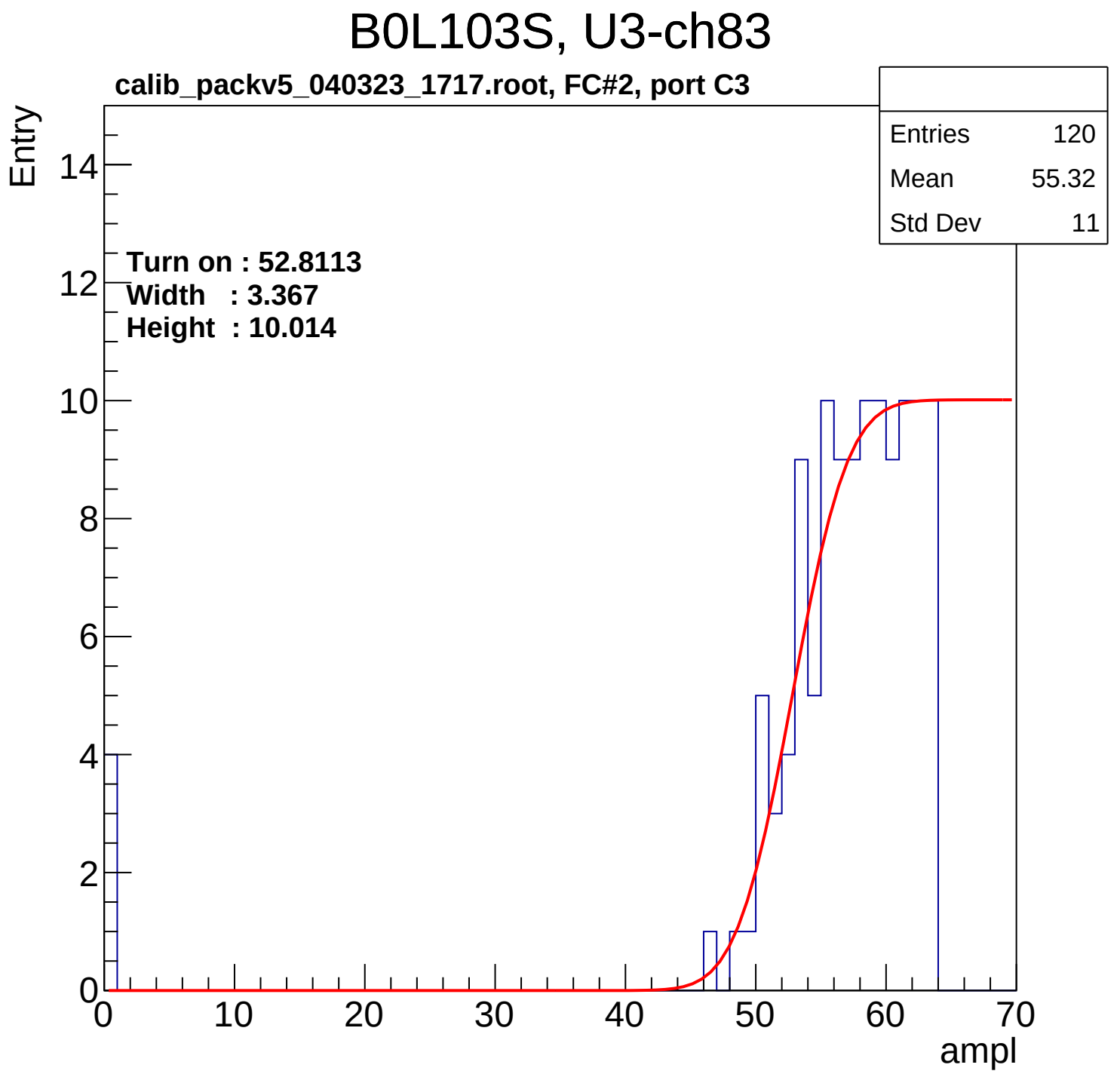
B0L103S, U3-ch83
calib_packv5_040323_1717.root, FC#2, port C3
Entries 120
Mean 55.32
Std Dev 11
Turn on : 52.8113
Width : 3.367
Height : 10.014
Entry
ampl
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6
8
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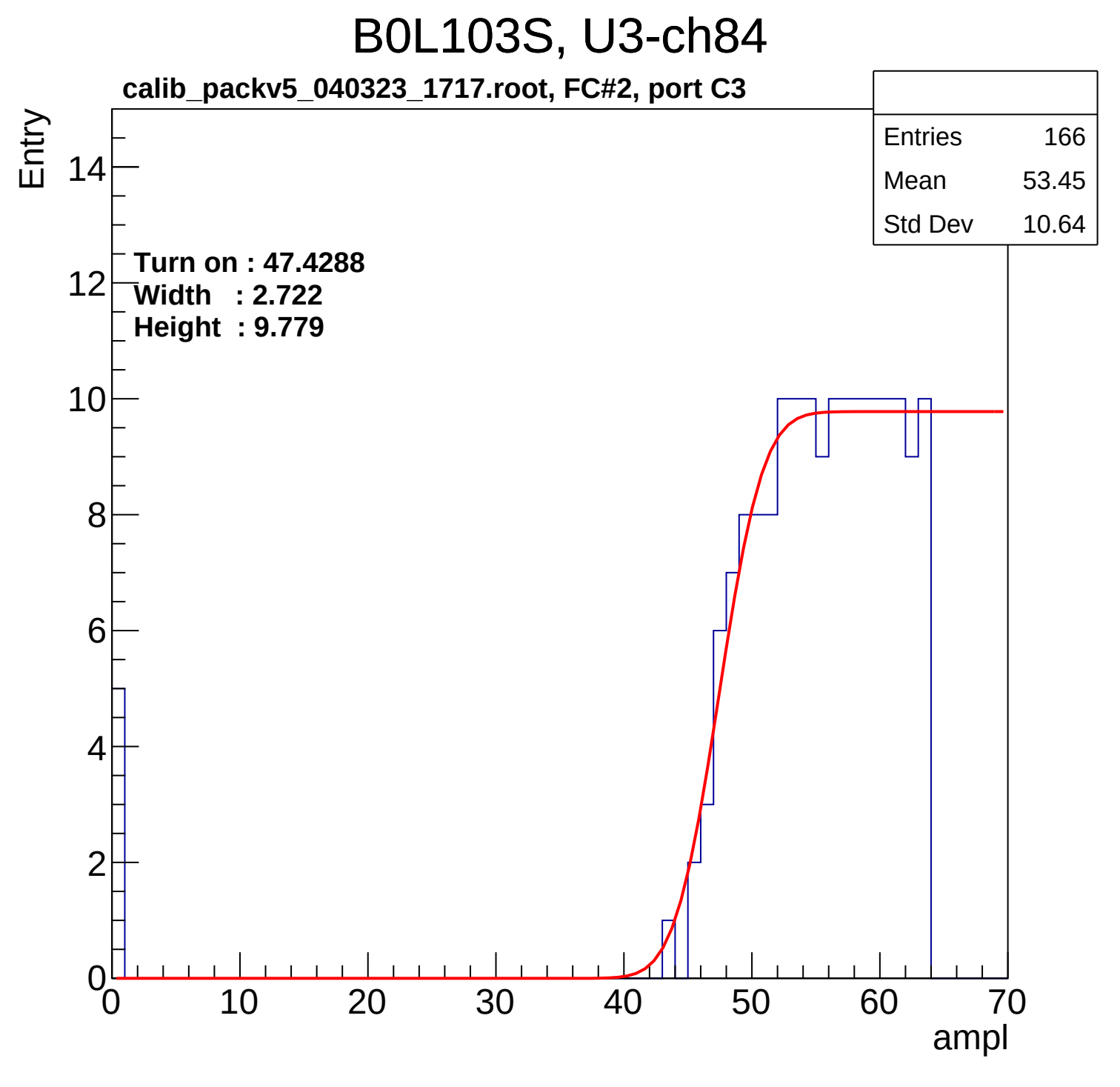
B0L103S, U3-ch84
calib_packv5_040323_1717.root, FC#2, port C3
Entries 166
Mean 53.45
Std Dev 10.64
Turn on : 47.4288
Width : 2.722
Height : 9.779
Entry
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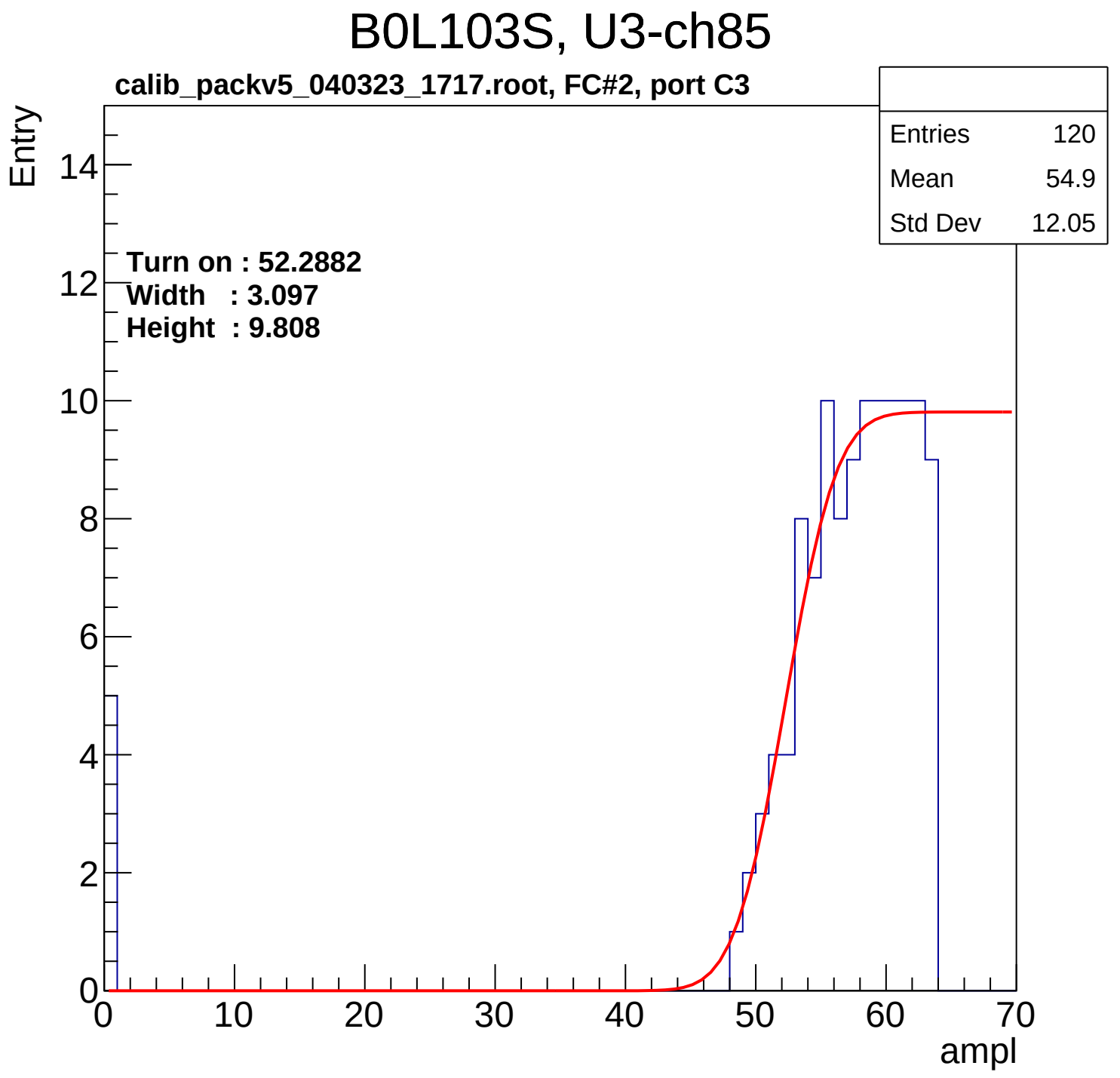
B0L103S, U3-ch85
calib_packv5_040323_1717.root, FC#2, port C3
Entries 120
Mean 54.9
Std Dev 12.05
Turn on : 52.2882
Width : 3.097
Height : 9.808
Entry
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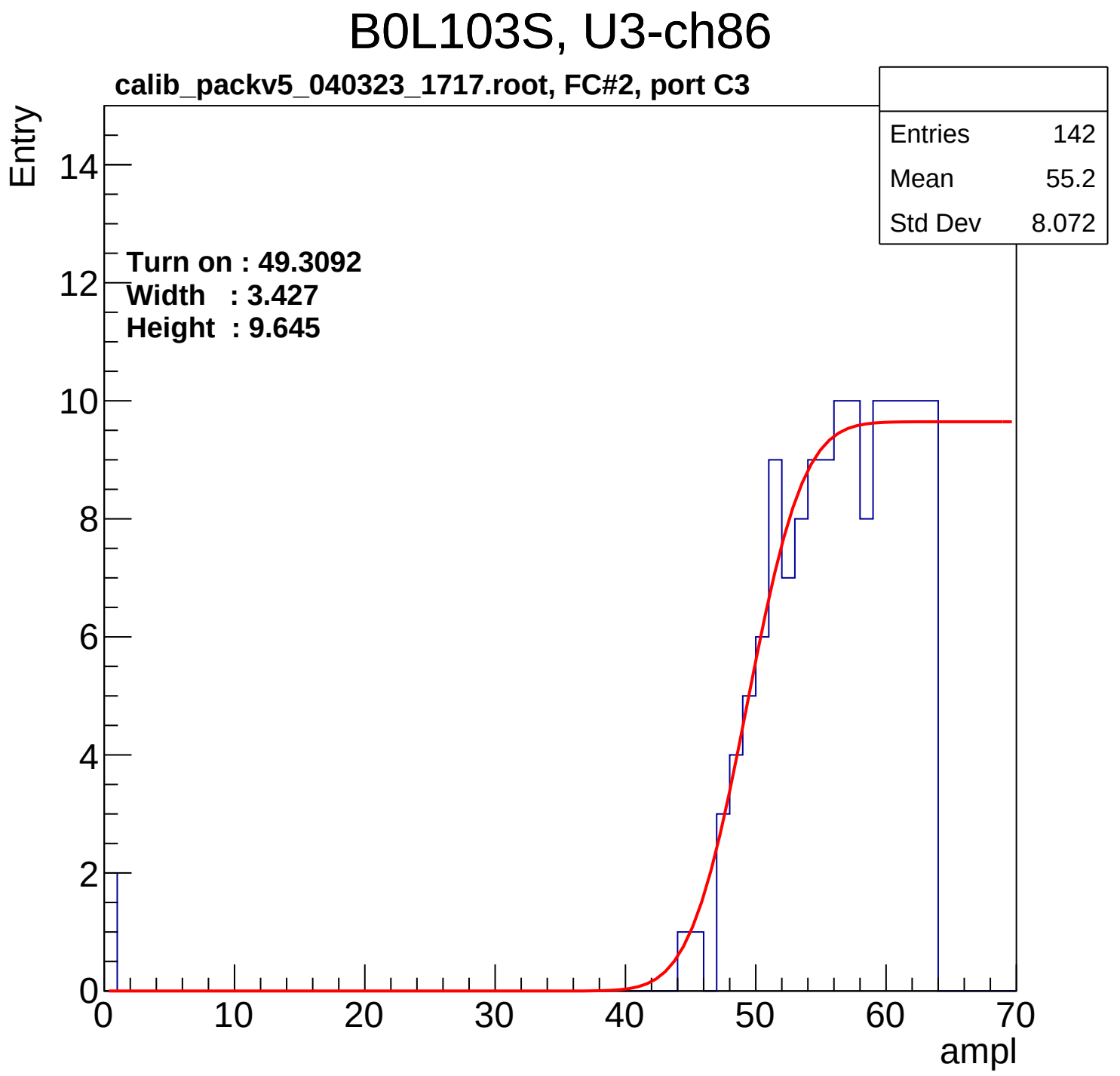
B0L103S, U3-ch86
calib_packv5_040323_1717.root, FC#2, port C3
Entries 142
Mean 55.2
Std Dev 8.072
Turn on : 49.3092
Width : 3.427
Height : 9.645
Entry
ampl
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2
4
6
8
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12
14
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10
20
30
40
50
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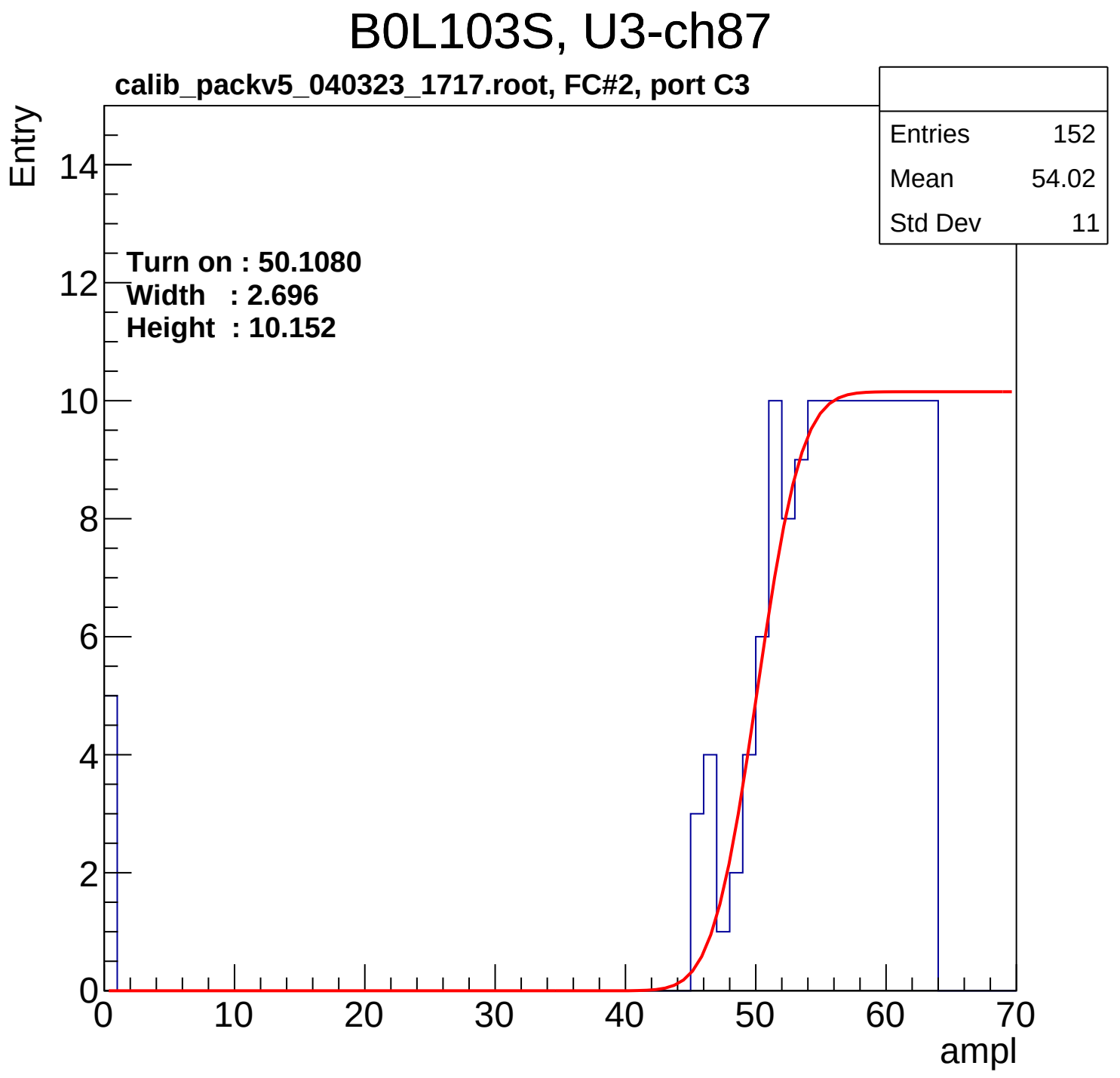
B0L103S, U3-ch87
calib_packv5_040323_1717.root, FC#2, port C3
Entries 152
Mean 54.02
Std Dev 11
Turn on : 50.1080
Width : 2.696
Height : 10.152
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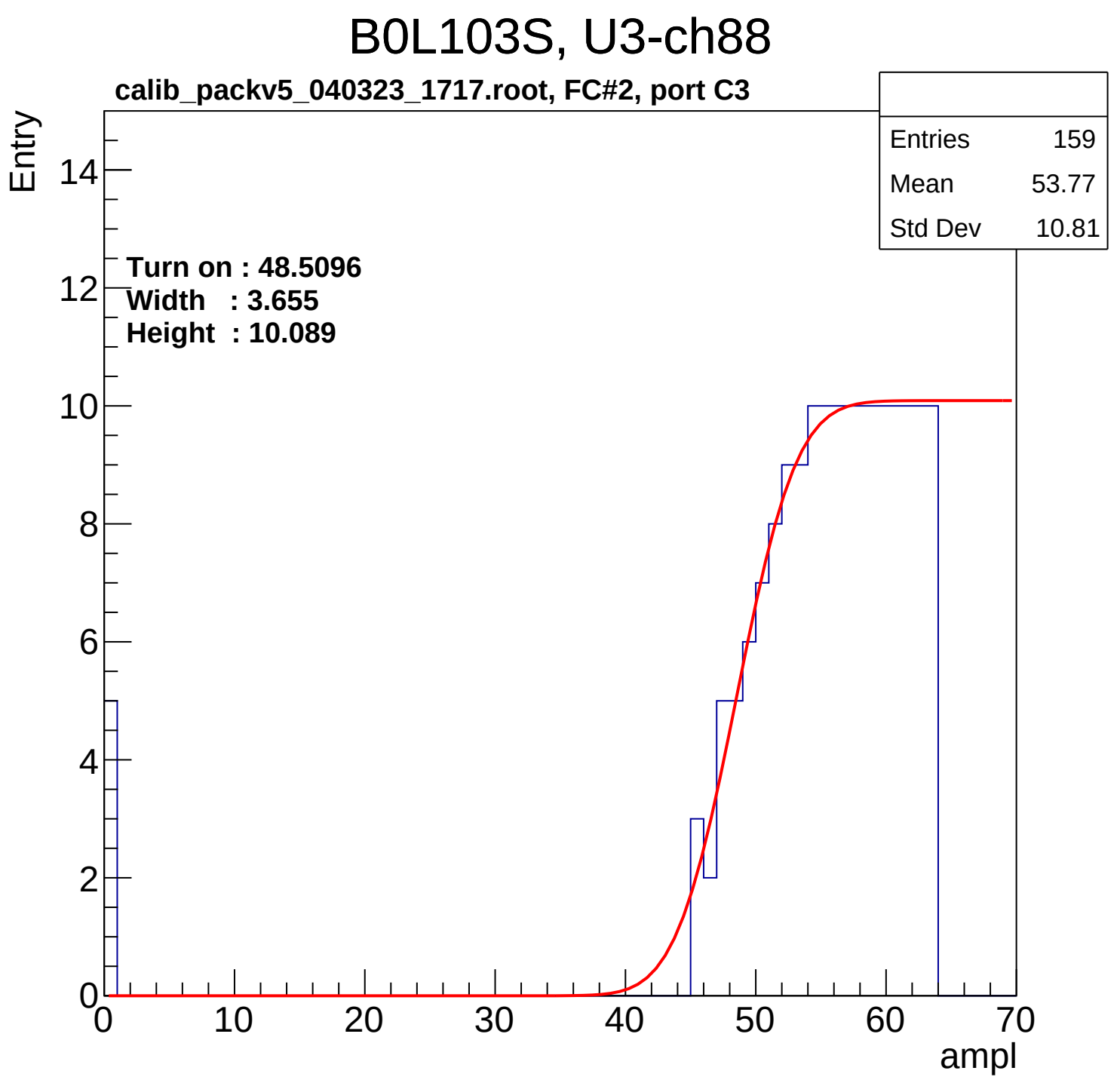
B0L103S, U3-ch88
calib_packv5_040323_1717.root, FC#2, port C3
Entries 159
Mean 53.77
Std Dev 10.81
Turn on : 48.5096
Width : 3.655
Height : 10.089
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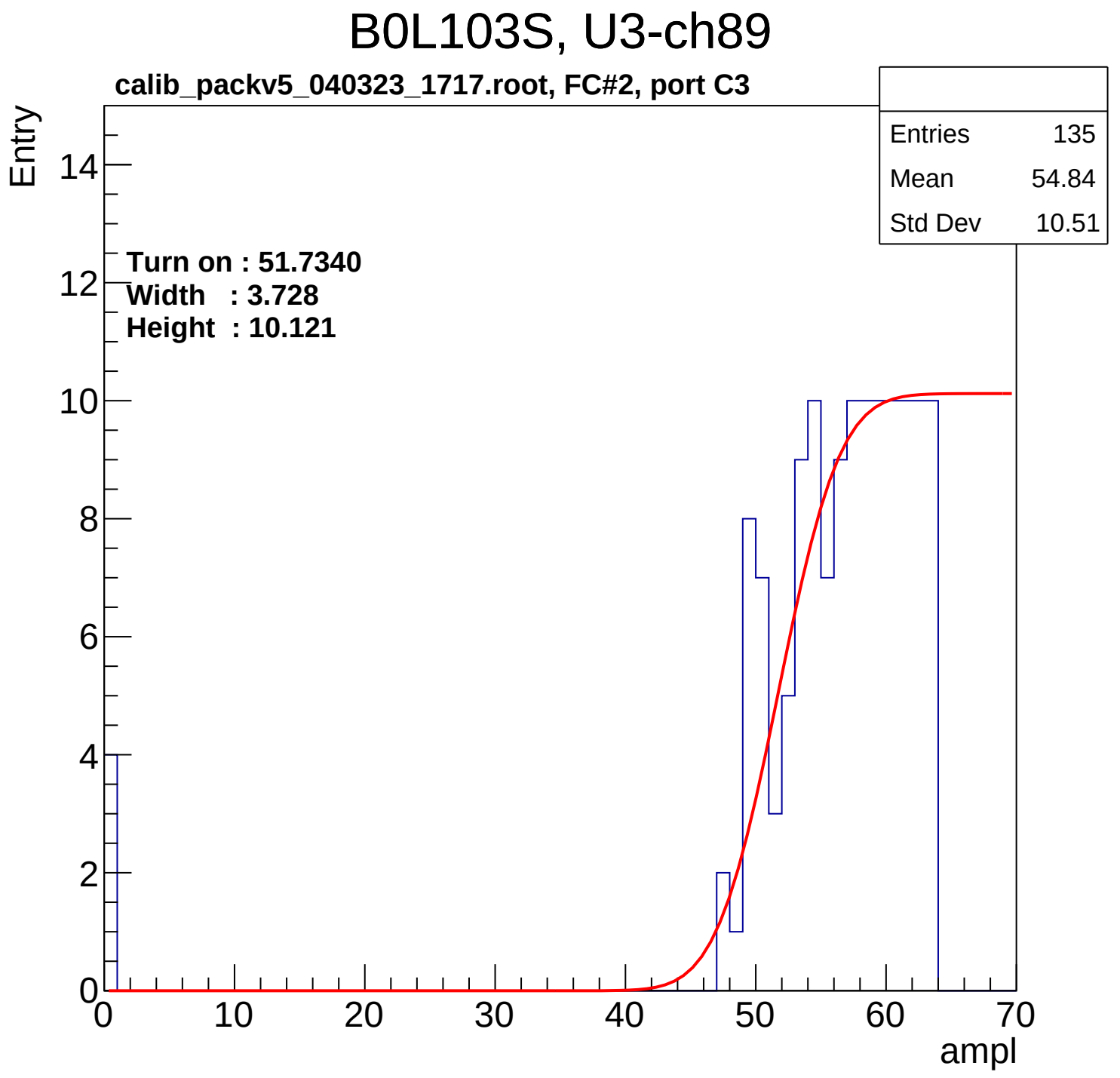
B0L103S, U3-ch89
calib_packv5_040323_1717.root, FC#2, port C3
Entries 135
Mean 54.84
Std Dev 10.51
Turn on : 51.7340
Width : 3.728
Height : 10.121
Entry
ampl
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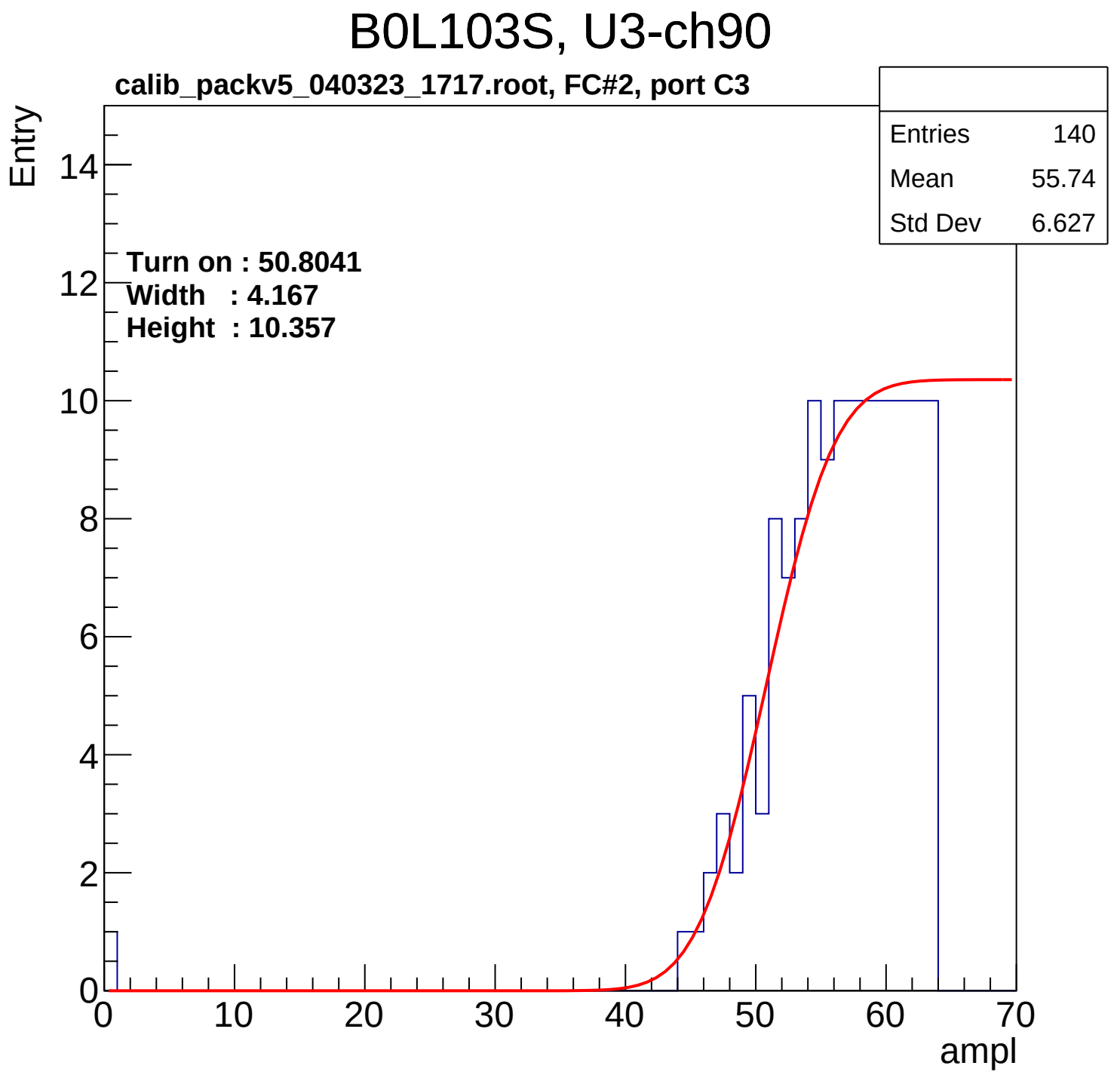
B0L103S, U3-ch90
calib_packv5_040323_1717.root, FC#2, port C3
Entries 140
Mean 55.74
Std Dev 6.627
Turn on : 50.8041
Width : 4.167
Height : 10.357
Entry
ampl
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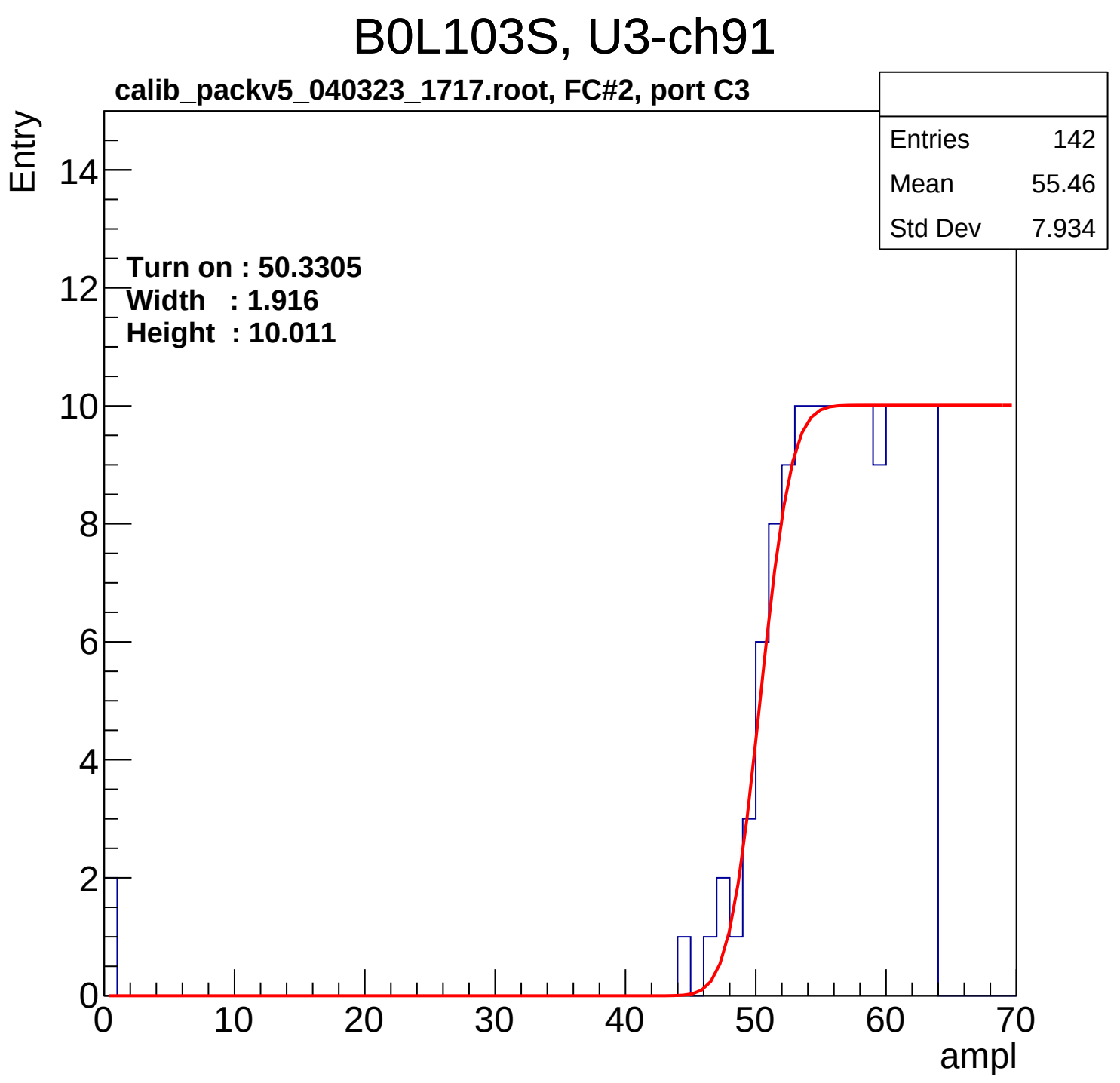
B0L103S, U3-ch91
calib_packv5_040323_1717.root, FC#2, port C3
Entries 142
Mean 55.46
Std Dev 7.934
Turn on : 50.3305
Width : 1.916
Height : 10.011
Entry
ampl
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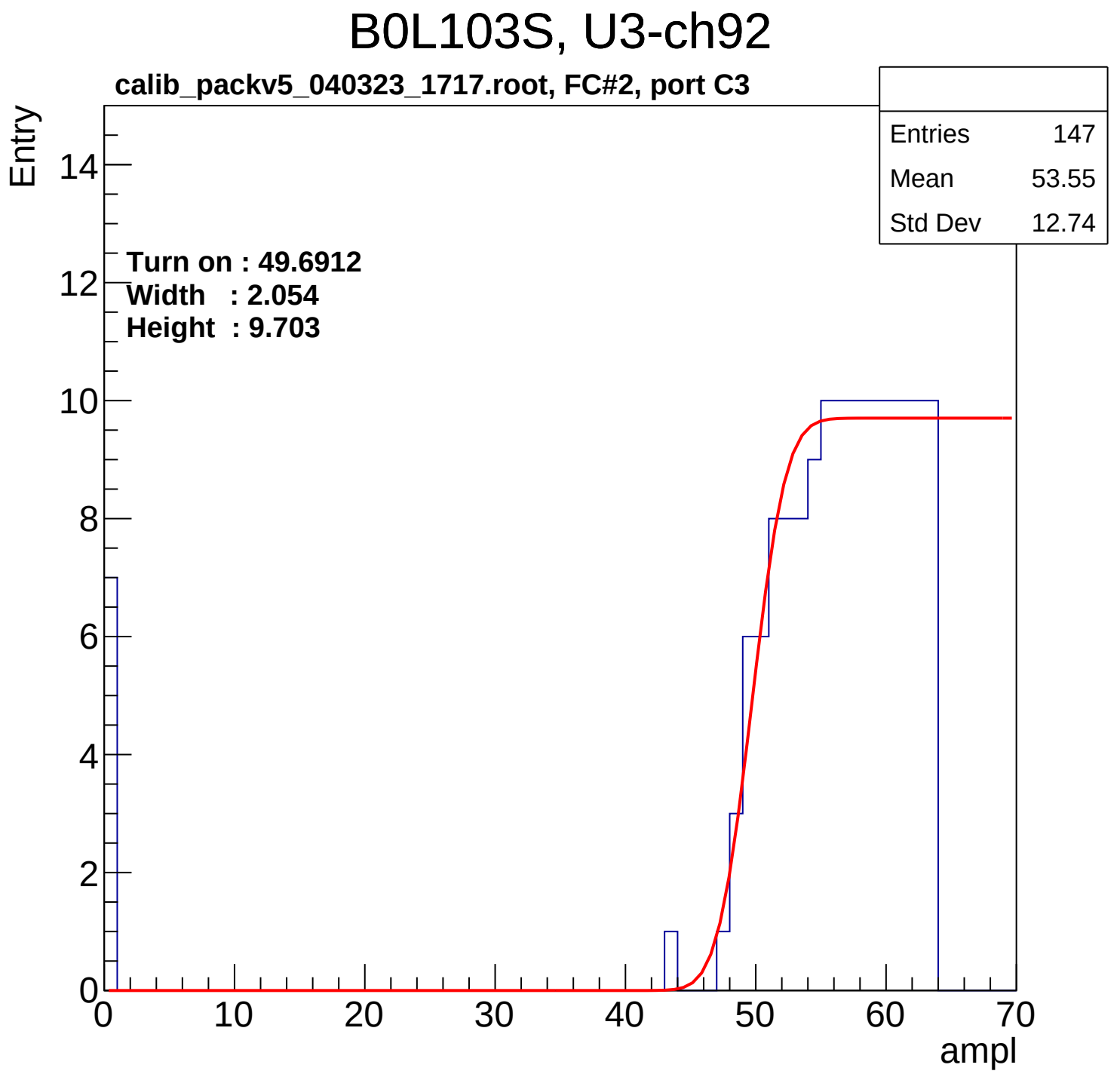
B0L103S, U3-ch92
calib_packv5_040323_1717.root, FC#2, port C3
Entries 147
Mean 53.55
Std Dev 12.74
Turn on : 49.6912
Width : 2.054
Height : 9.703
Entry
ampl
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8
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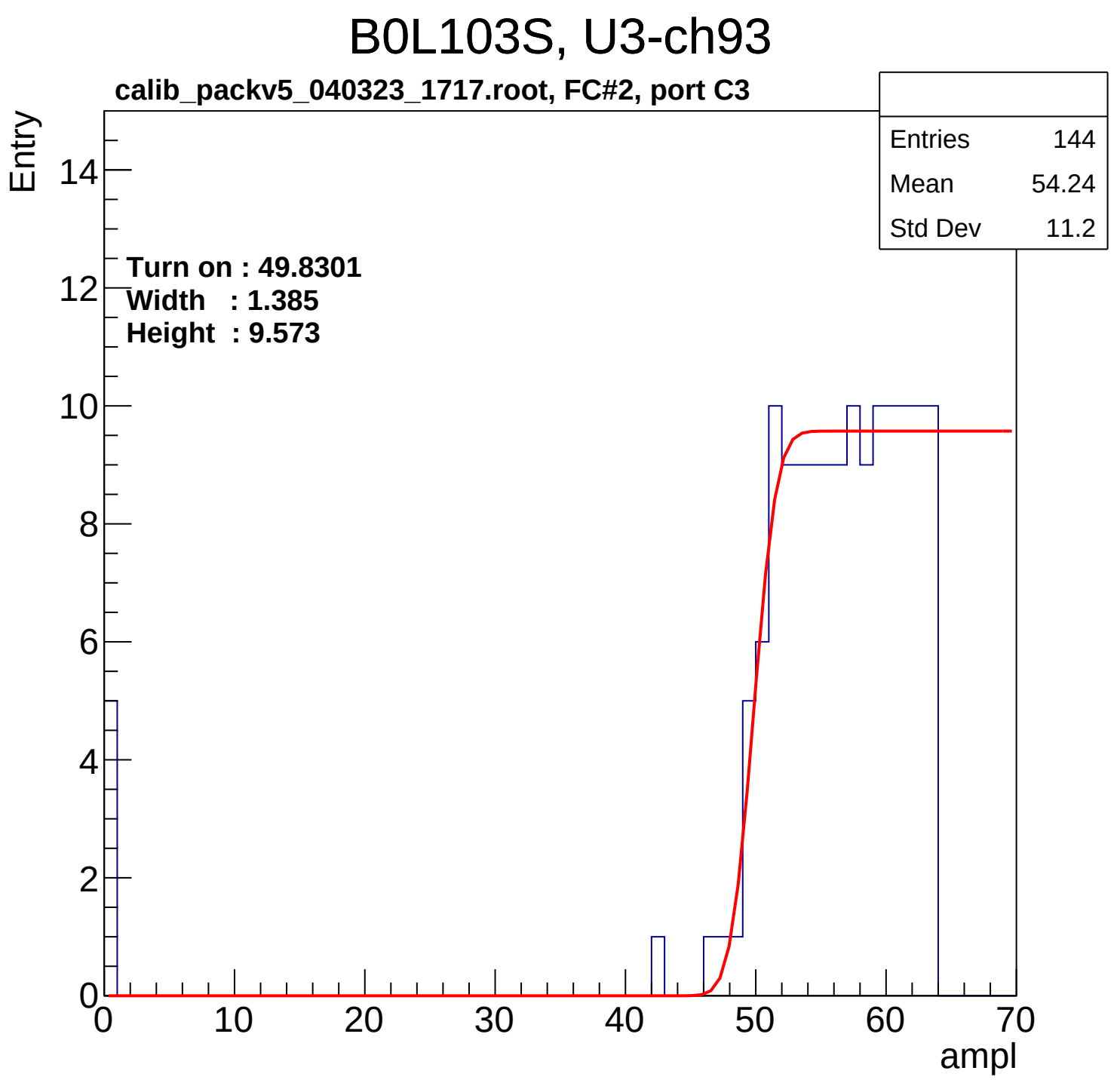
B0L103S, U3-ch93
calib_packv5_040323_1717.root, FC#2, port C3
Entries 144
Mean 54.24
Std Dev 11.2
Turn on : 49.8301
Width : 1.385
Height : 9.573
Entry
ampl
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6
8
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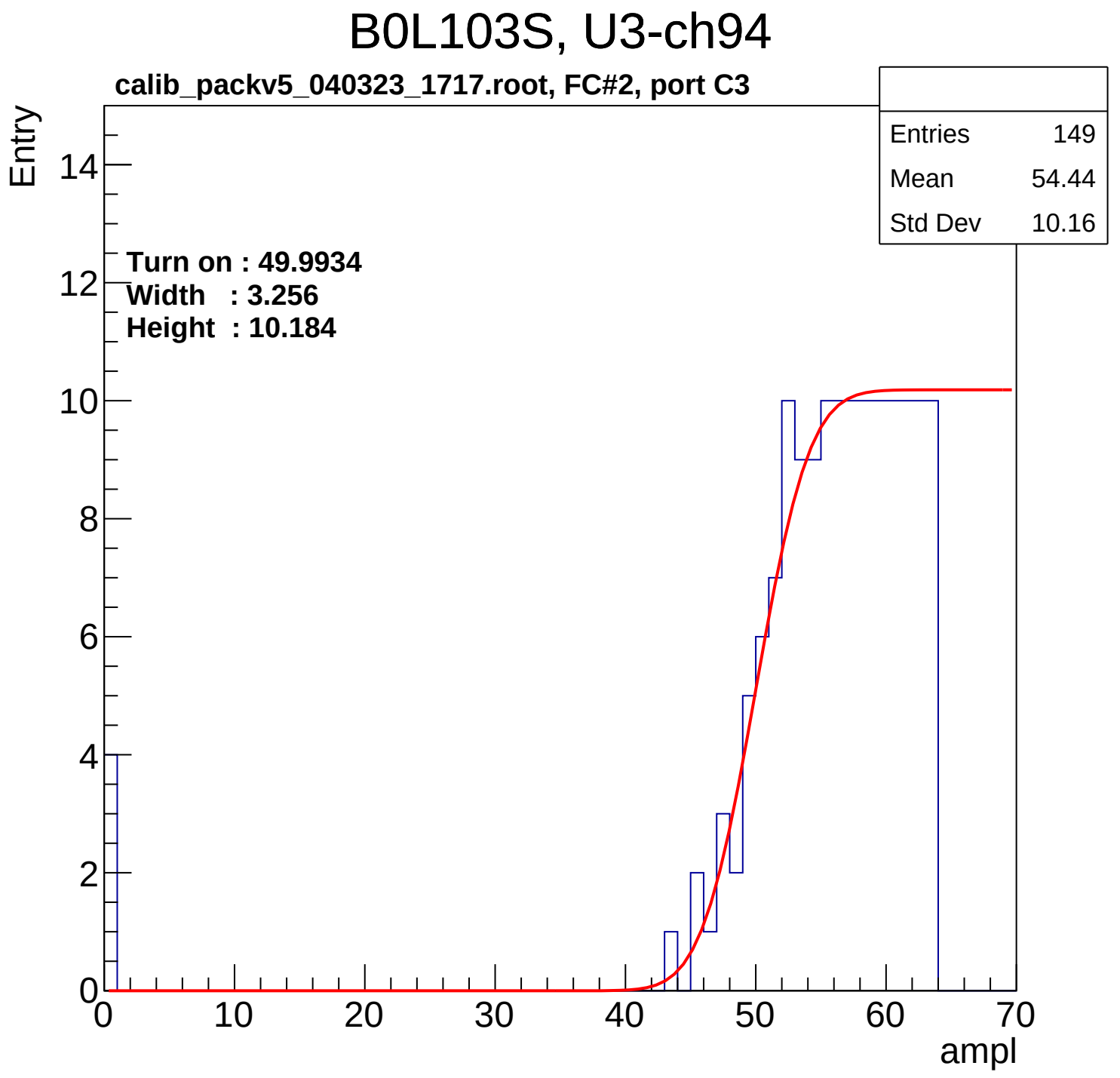
B0L103S, U3-ch94
calib_packv5_040323_1717.root, FC#2, port C3
Entries 149
Mean 54.44
Std Dev 10.16
Turn on : 49.9934
Width : 3.256
Height : 10.184
Entry
ampl
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6
8
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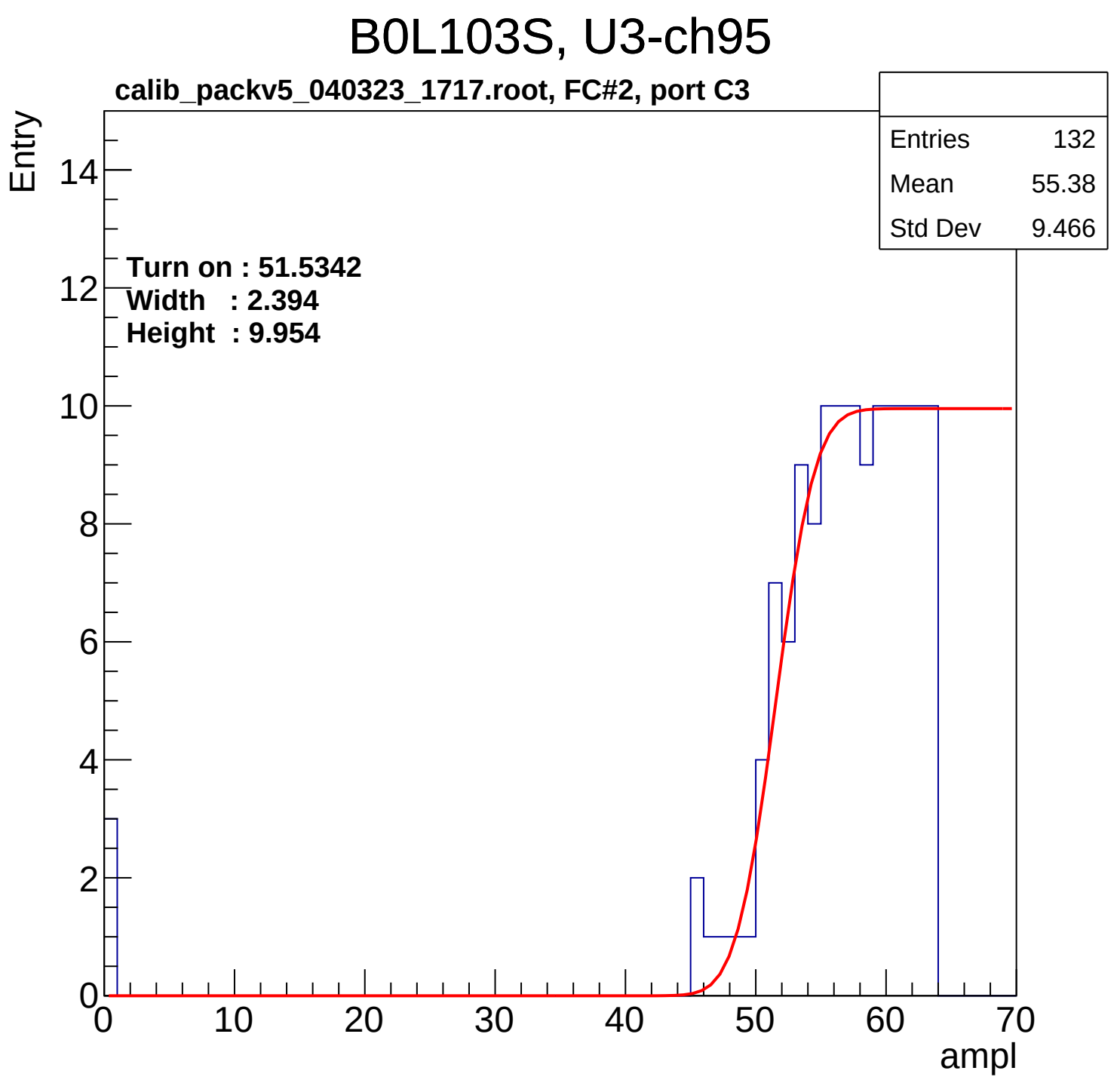
B0L103S, U3-ch95
calib_packv5_040323_1717.root, FC#2, port C3
Entries 132
Mean 55.38
Std Dev 9.466
Turn on : 51.5342
Width : 2.394
Height : 9.954
Entry
ampl
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6
8
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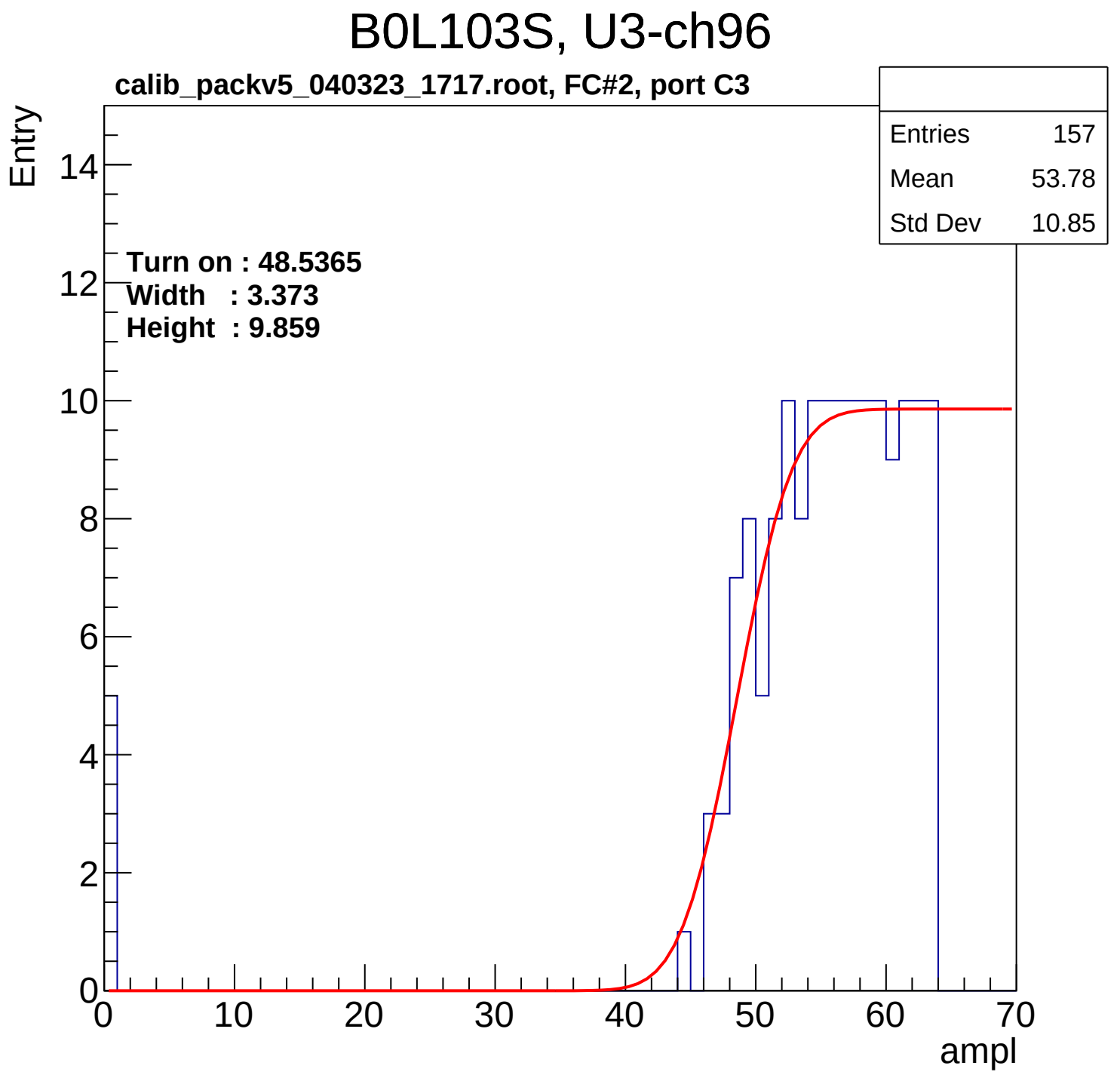
B0L103S, U3-ch96
calib_packv5_040323_1717.root, FC#2, port C3
Entries 157
Mean 53.78
Std Dev 10.85
Turn on : 48.5365
Width : 3.373
Height : 9.859
Entry
ampl
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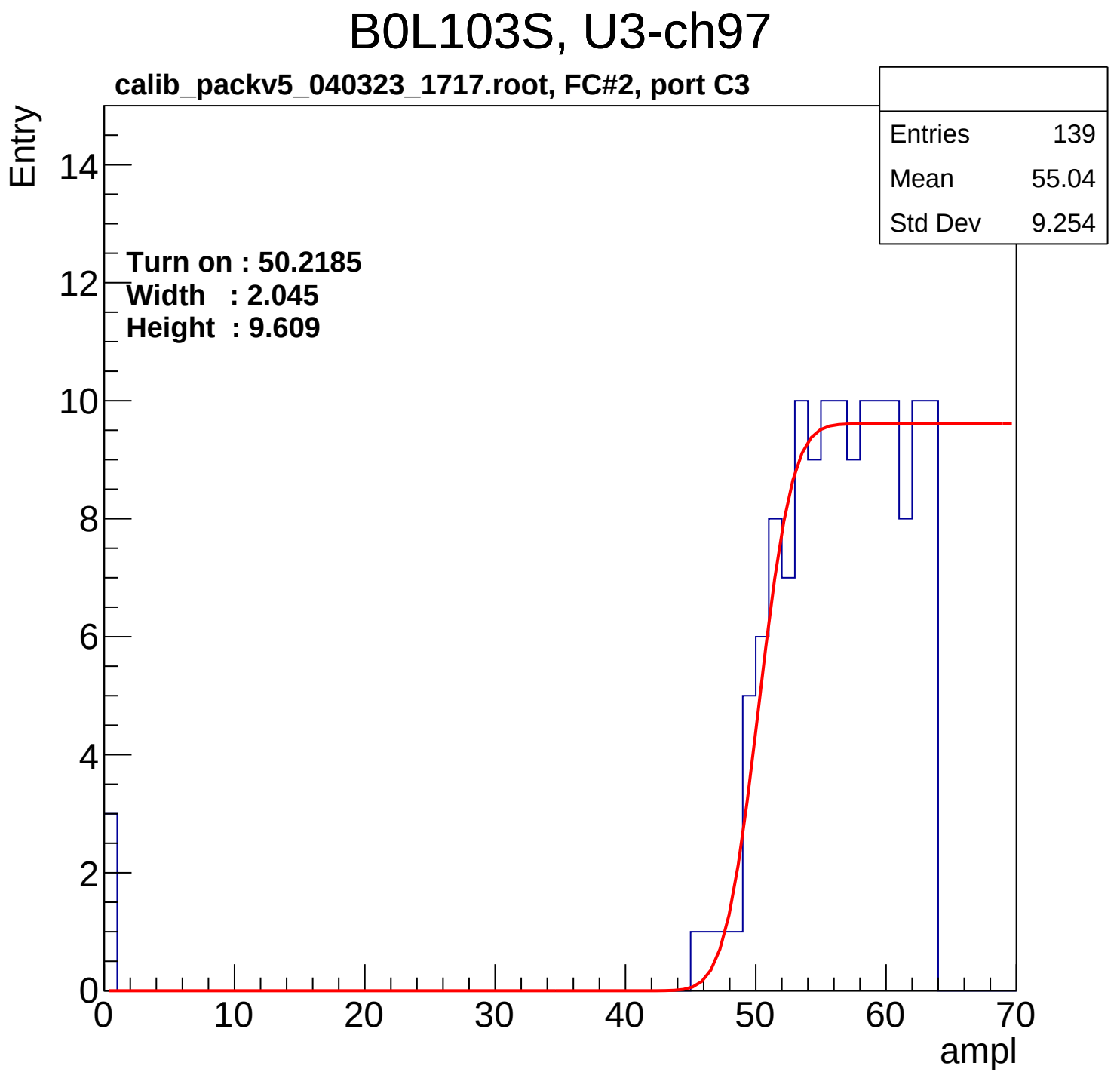
B0L103S, U3-ch97
calib_packv5_040323_1717.root, FC#2, port C3
Entries 139
Mean 55.04
Std Dev 9.254
Turn on : 50.2185
Width : 2.045
Height : 9.609
Entry
ampl
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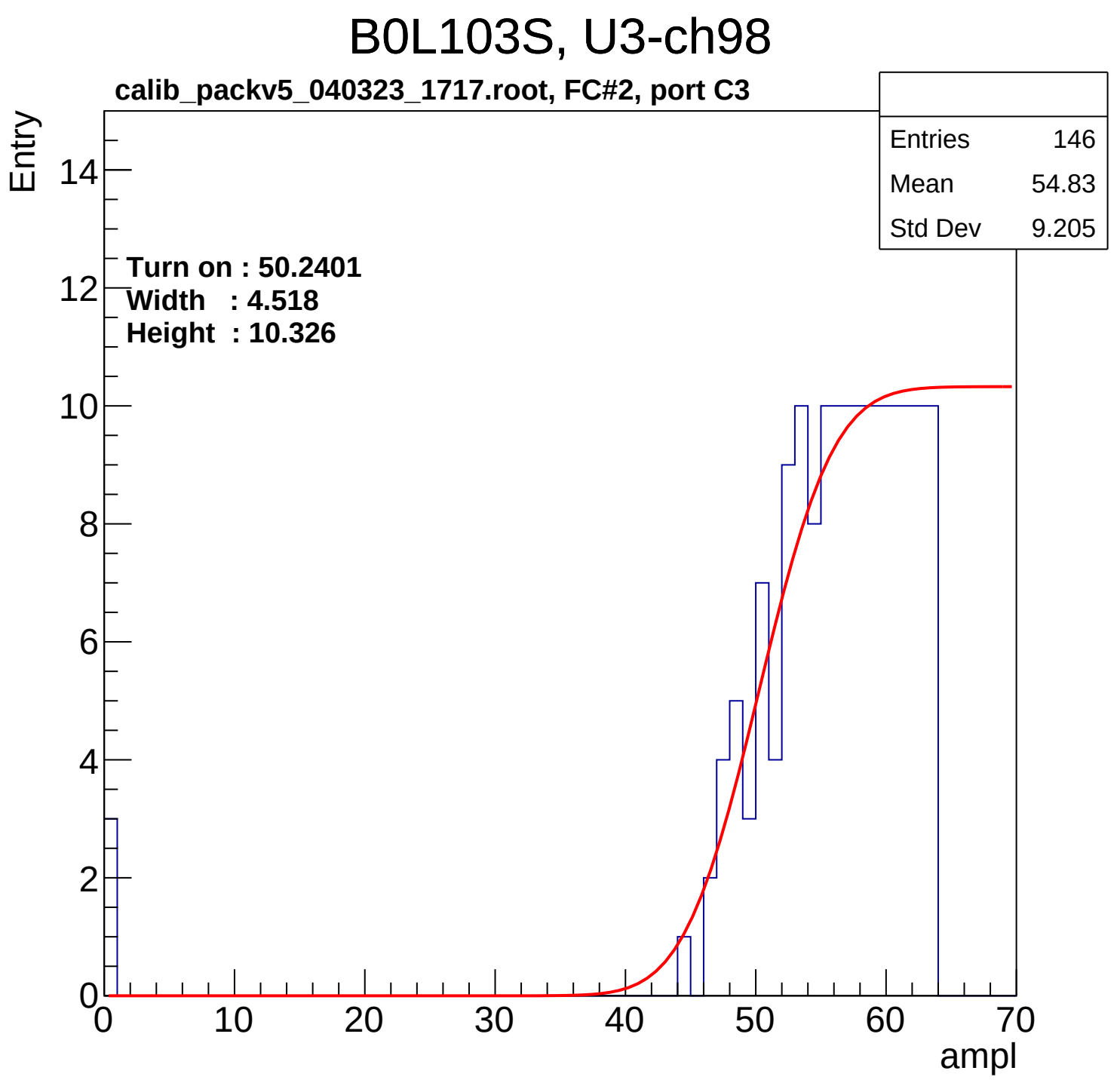
B0L103S, U3-ch98
calib_packv5_040323_1717.root, FC#2, port C3
Entries 146
Mean 54.83
Std Dev 9.205
Turn on : 50.2401
Width : 4.518
Height : 10.326
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ampl
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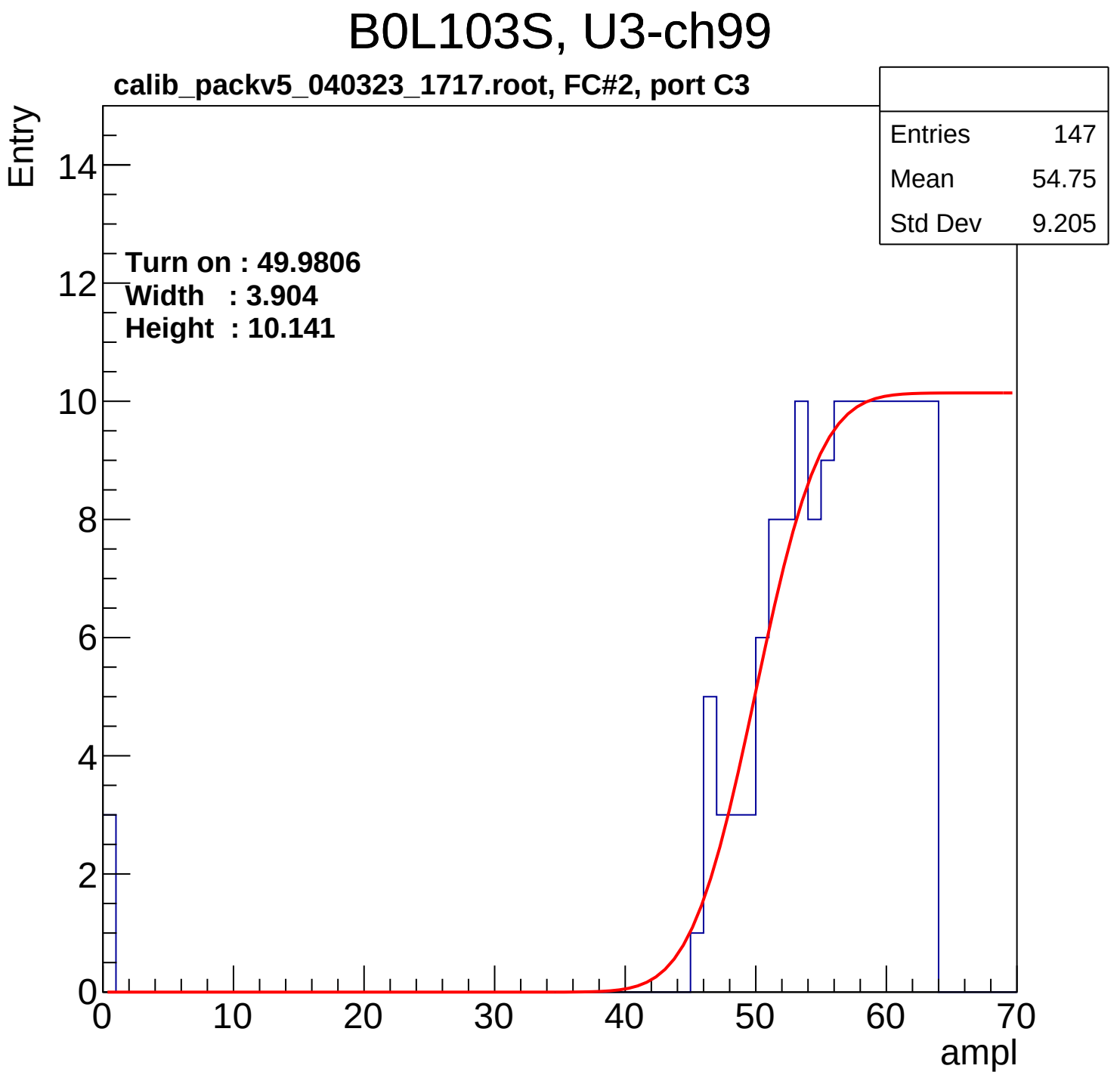
B0L103S, U3-ch99
calib_packv5_040323_1717.root, FC#2, port C3
Entries 147
Mean 54.75
Std Dev 9.205
Turn on : 49.9806
Width : 3.904
Height : 10.141
Entry
ampl
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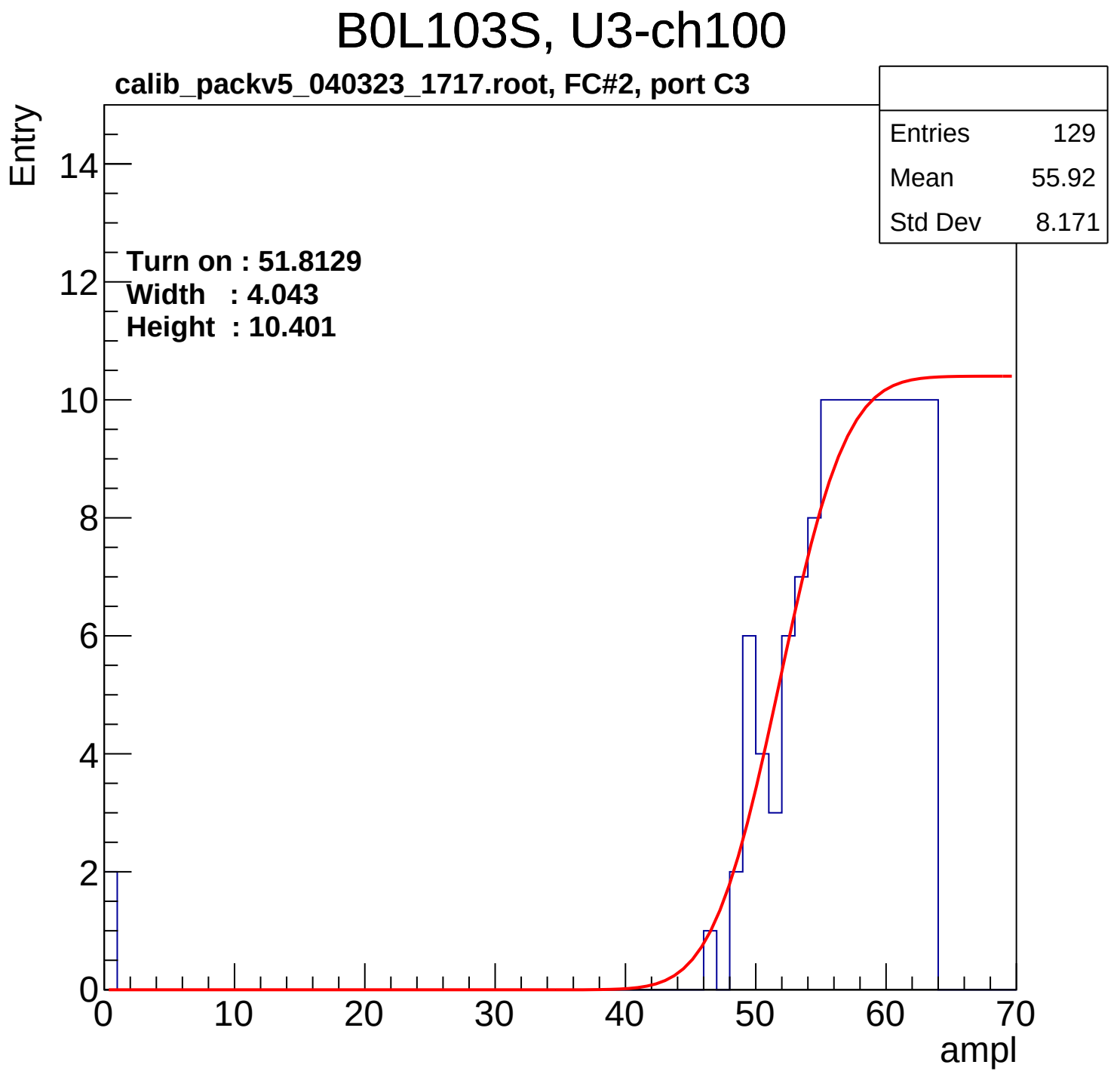
B0L103S, U3-ch100
calib_packv5_040323_1717.root, FC#2, port C3
Entries 129
Mean 55.92
Std Dev 8.171
Turn on : 51.8129
Width : 4.043
Height : 10.401
Entry
ampl
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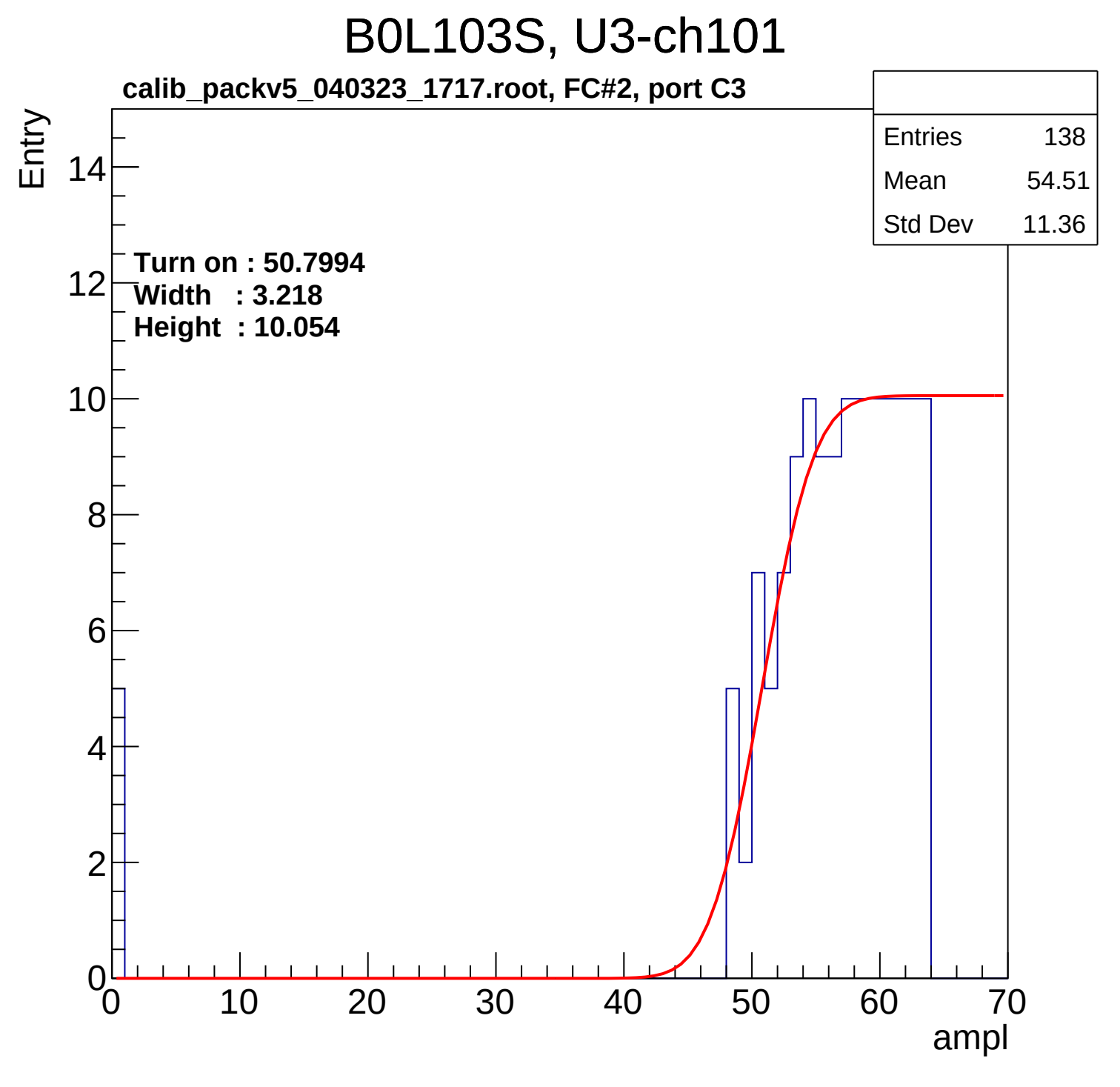
B0L103S, U3-ch101
calib_packv5_040323_1717.root, FC#2, port C3
Entries 138
Mean 54.51
Std Dev 11.36
Turn on : 50.7994
Width : 3.218
Height : 10.054
Entry
ampl
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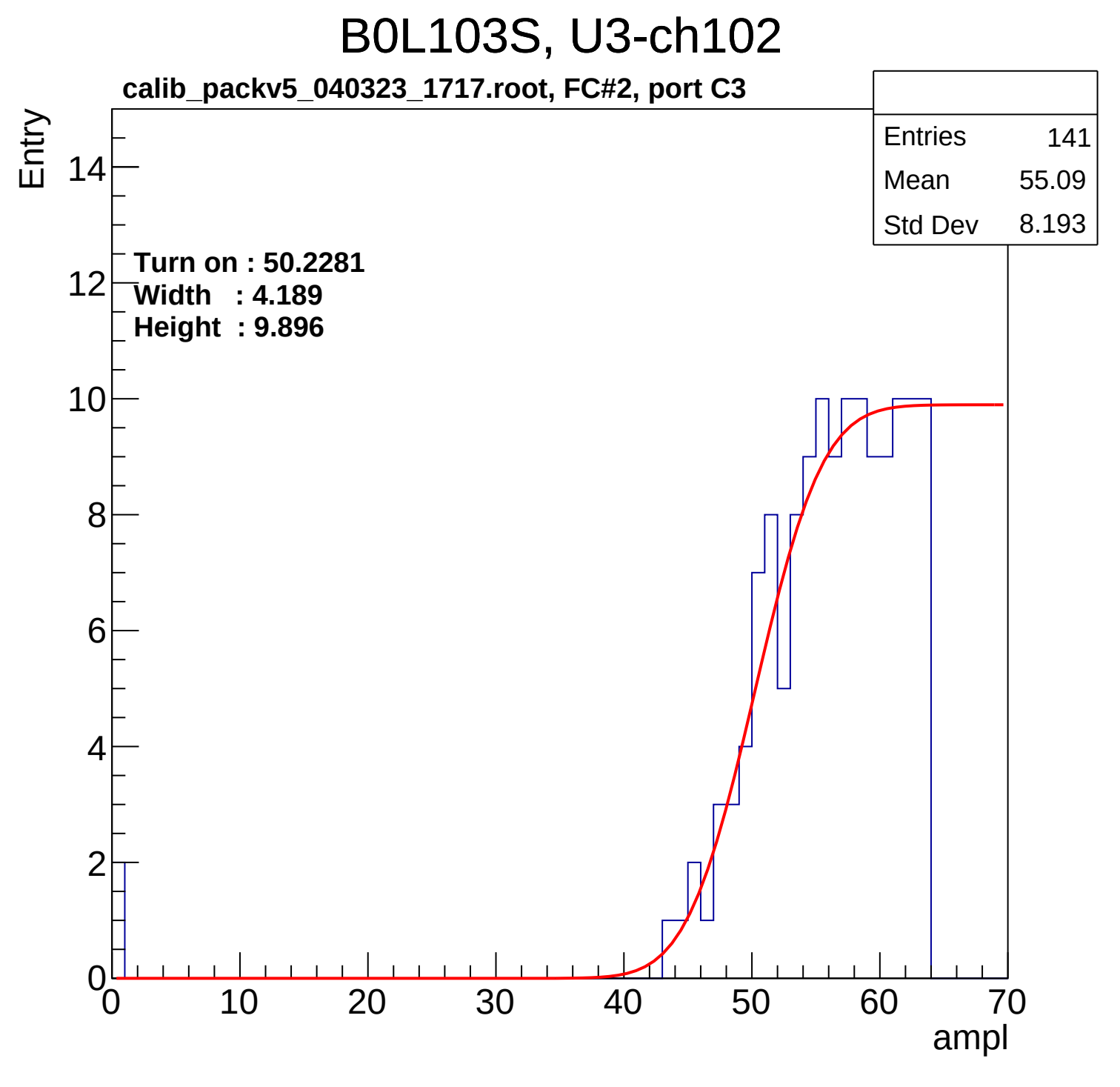
B0L103S, U3-ch102
calib_packv5_040323_1717.root, FC#2, port C3
Entries 141
Mean 55.09
Std Dev 8.193
Turn on : 50.2281
Width : 4.189
Height : 9.896
Entry
ampl
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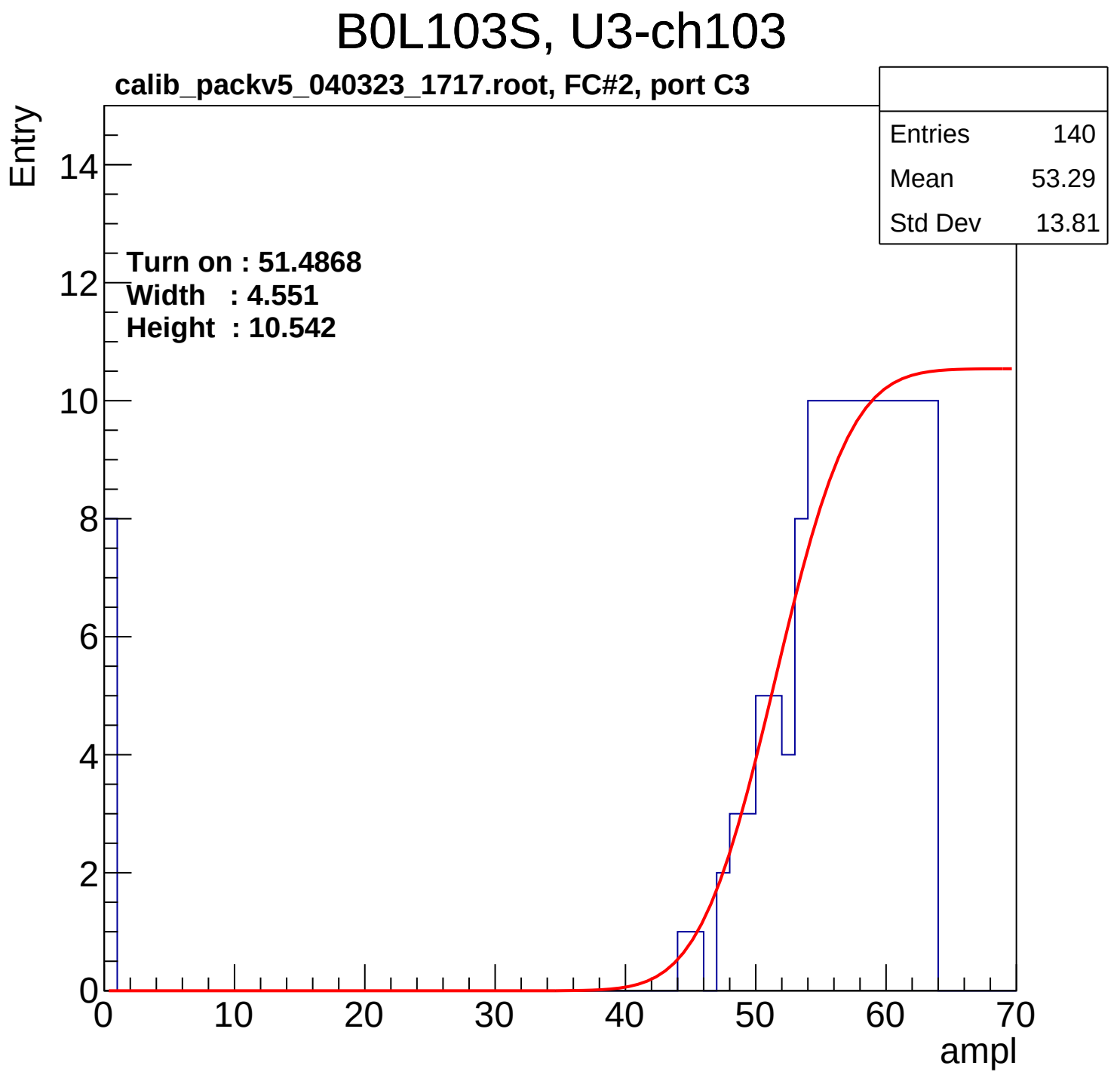
B0L103S, U3-ch103
calib_packv5_040323_1717.root, FC#2, port C3
Entries 140
Mean 53.29
Std Dev 13.81
Turn on : 51.4868
Width : 4.551
Height : 10.542
Entry
ampl
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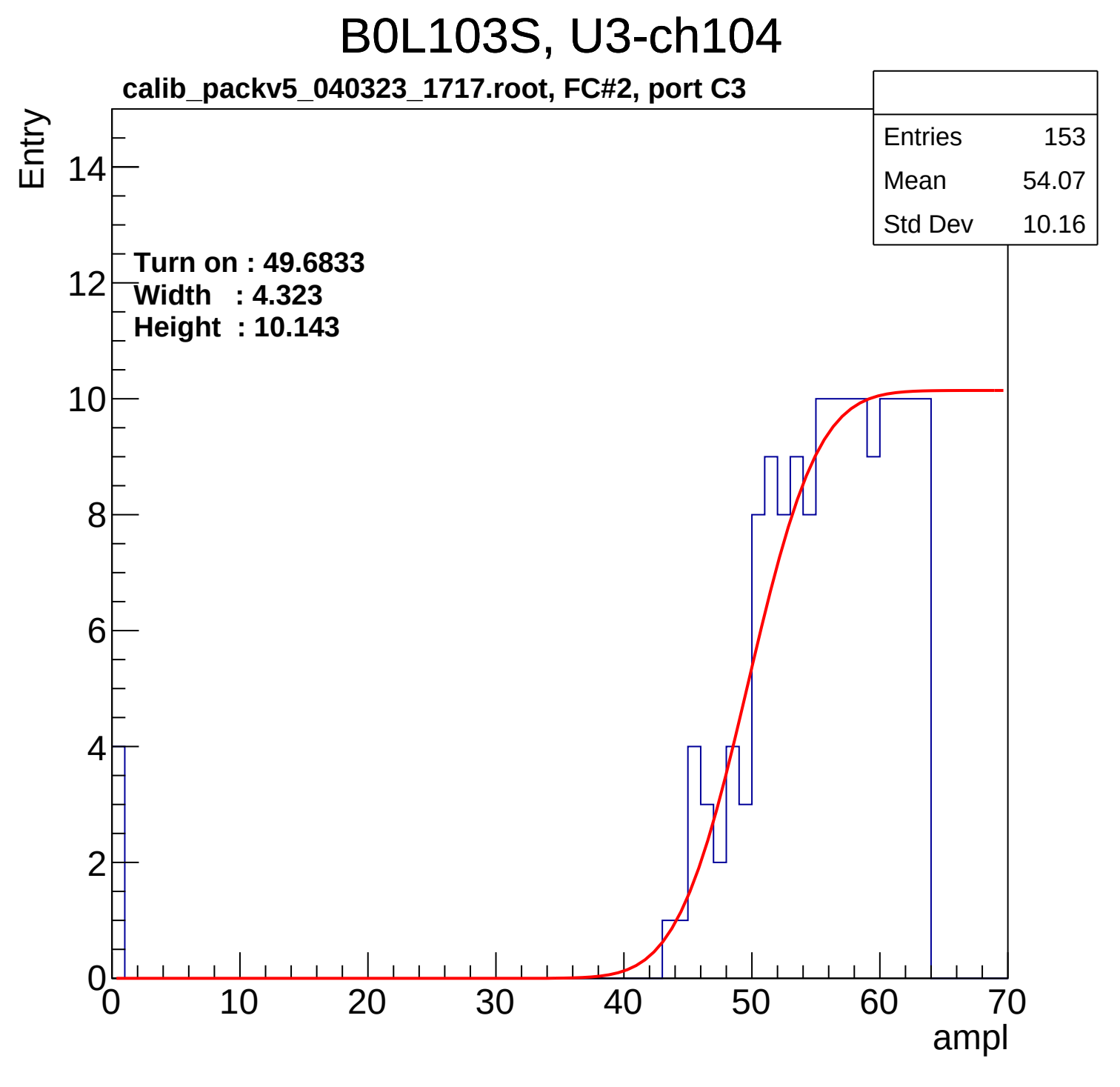
B0L103S, U3-ch104
calib_packv5_040323_1717.root, FC#2, port C3
Entries 153
Mean 54.07
Std Dev 10.16
Turn on : 49.6833
Width : 4.323
Height : 10.143
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ampl
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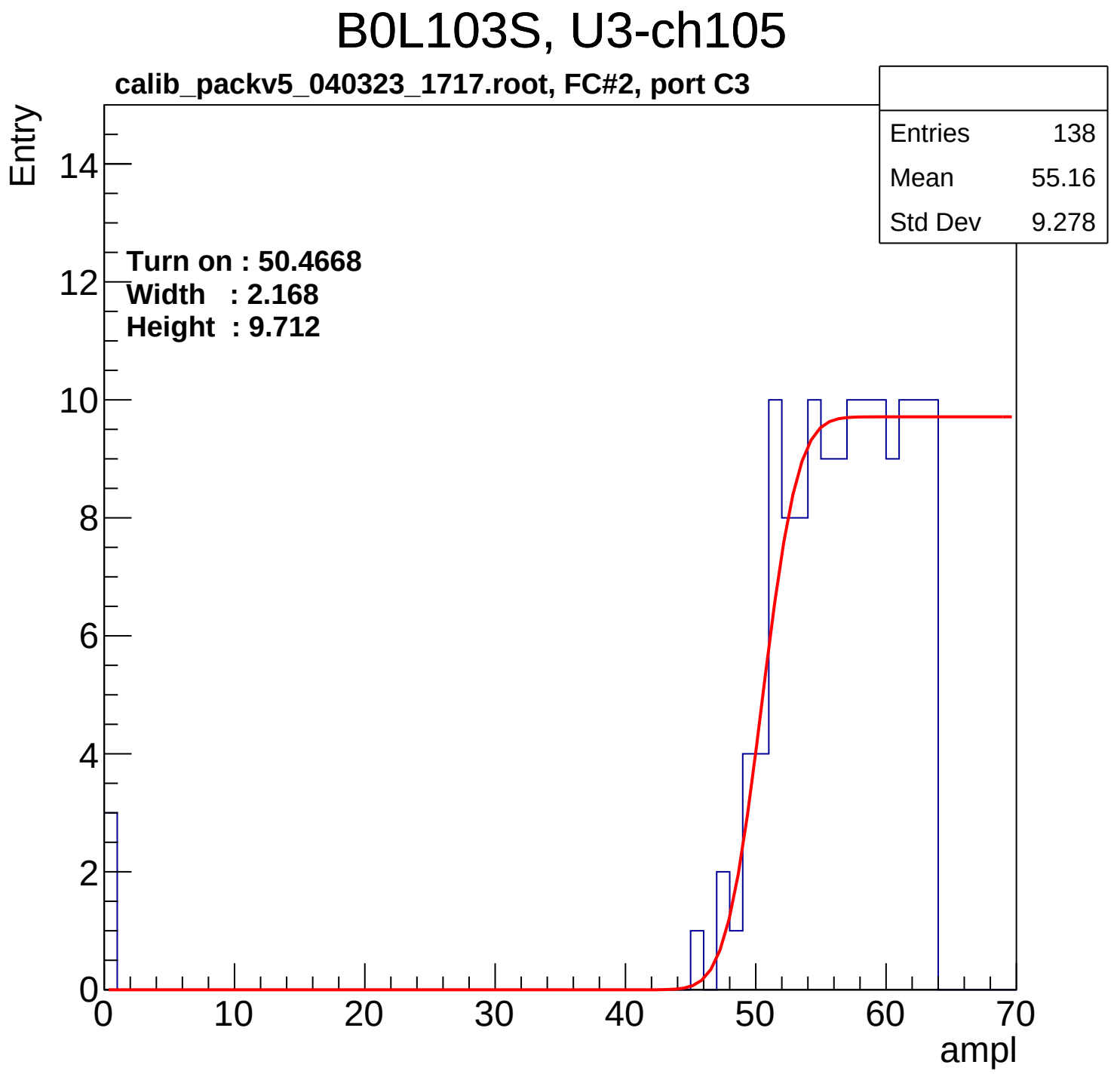
B0L103S, U3-ch105
calib_packv5_040323_1717.root, FC#2, port C3
Entries 138
Mean 55.16
Std Dev 9.278
Turn on : 50.4668
Width : 2.168
Height : 9.712
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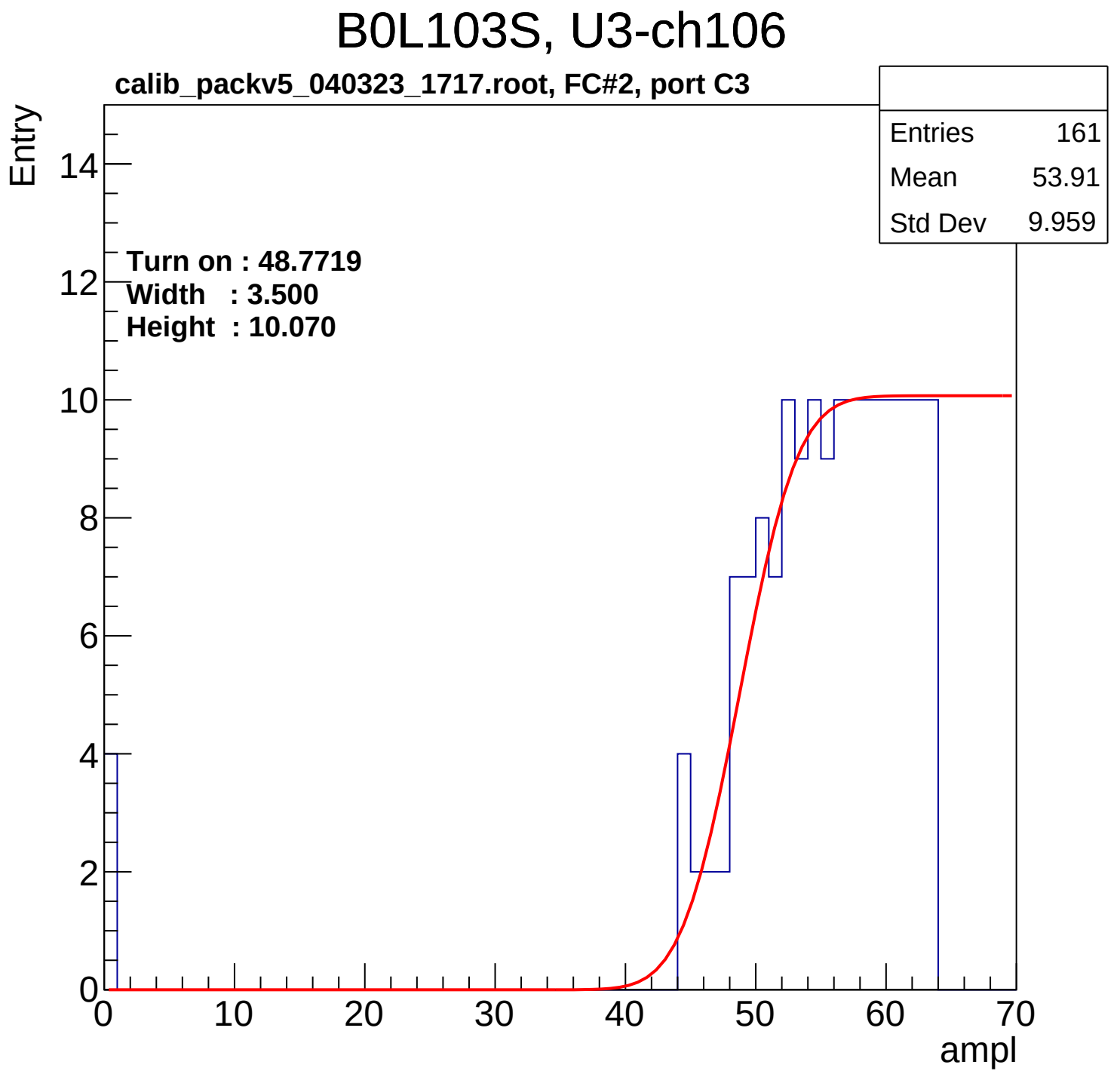
B0L103S, U3-ch106
calib_packv5_040323_1717.root, FC#2, port C3
Entries 161
Mean 53.91
Std Dev 9.959
Turn on : 48.7719
Width : 3.500
Height : 10.070
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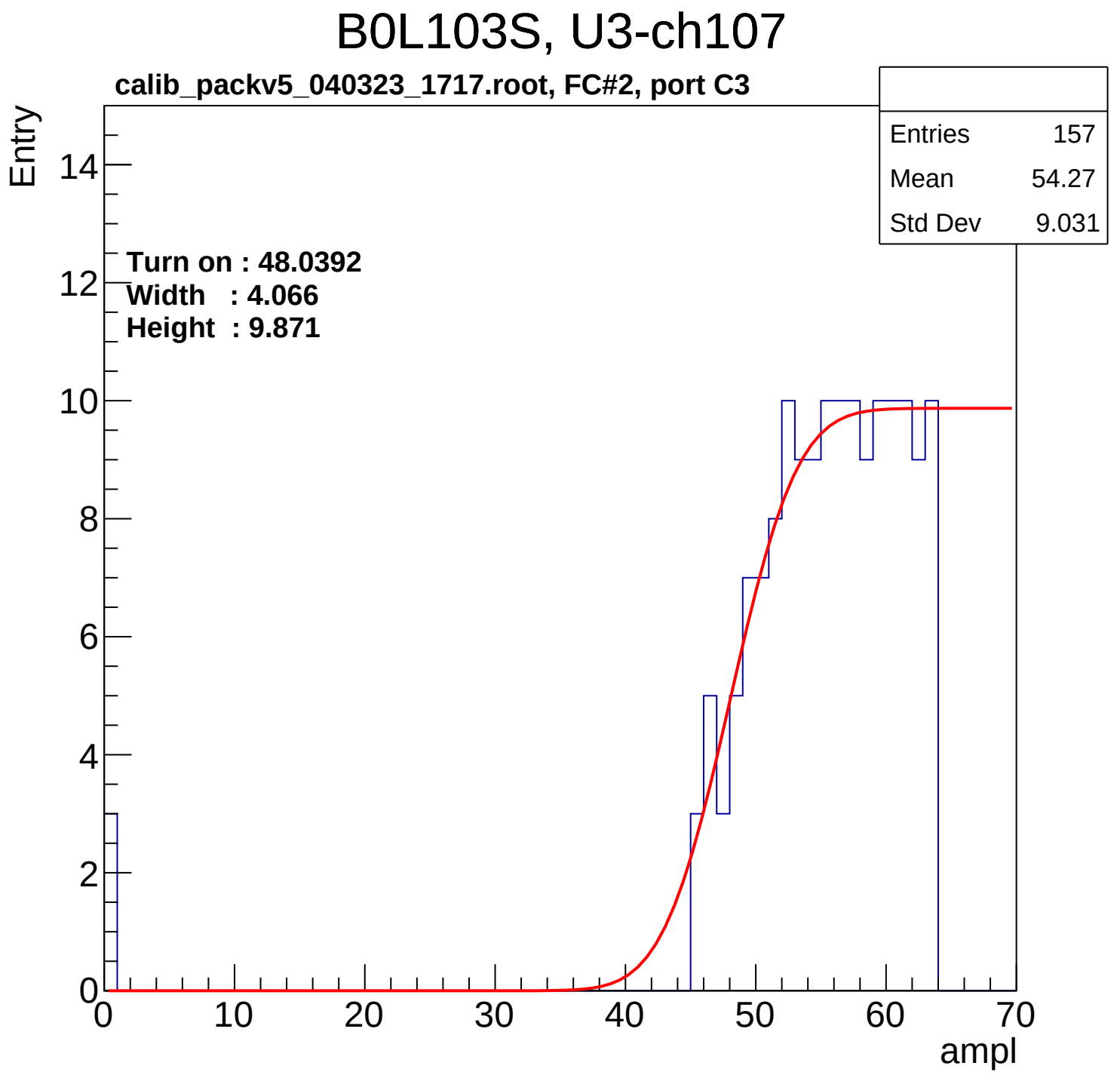
B0L103S, U3-ch107
calib_packv5_040323_1717.root, FC#2, port C3
Entries 157
Mean 54.27
Std Dev 9.031
Turn on : 48.0392
Width : 4.066
Height : 9.871
Entry
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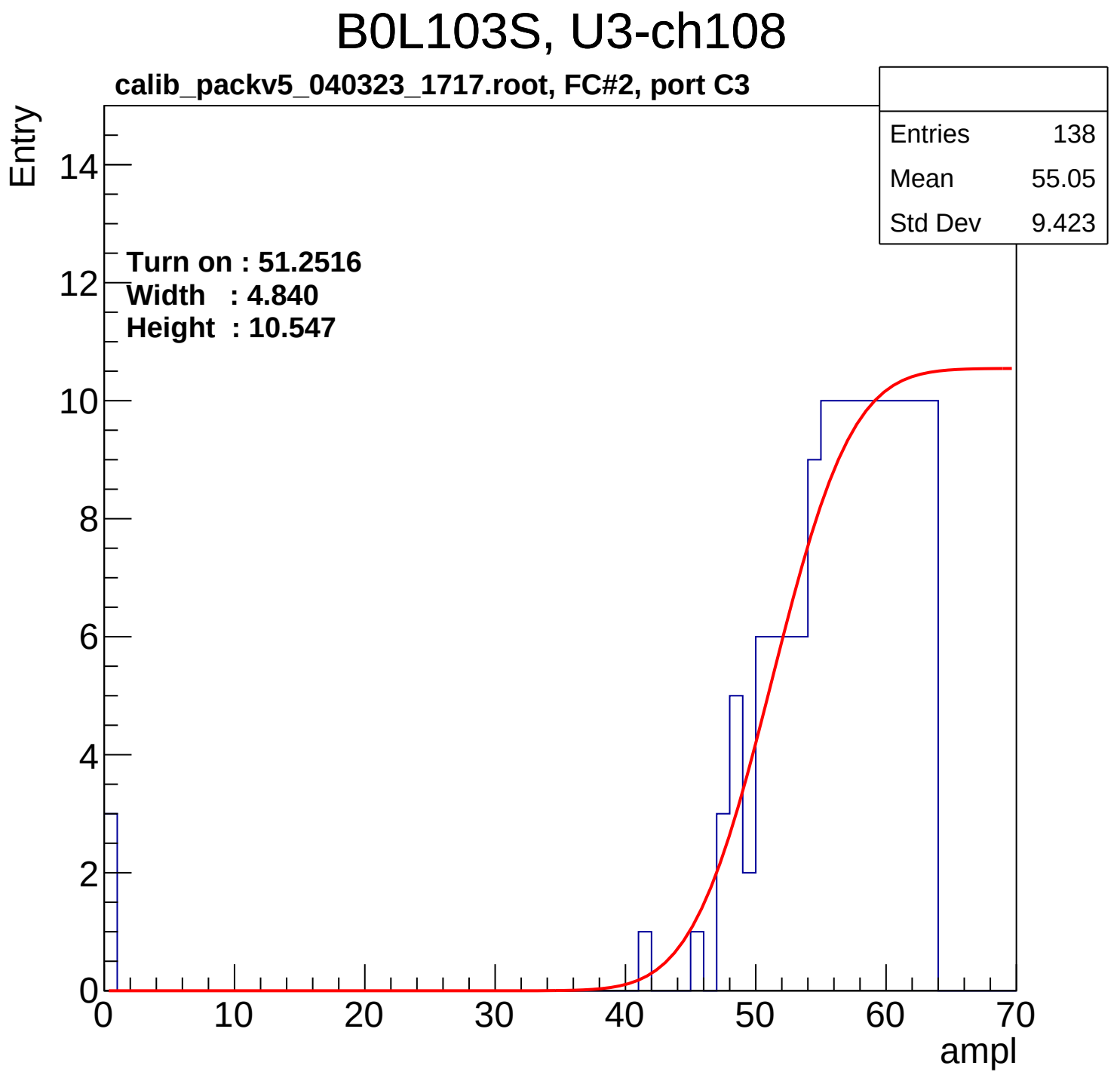
B0L103S, U3-ch108
calib_packv5_040323_1717.root, FC#2, port C3
Entries 138
Mean 55.05
Std Dev 9.423
Turn on : 51.2516
Width : 4.840
Height : 10.547
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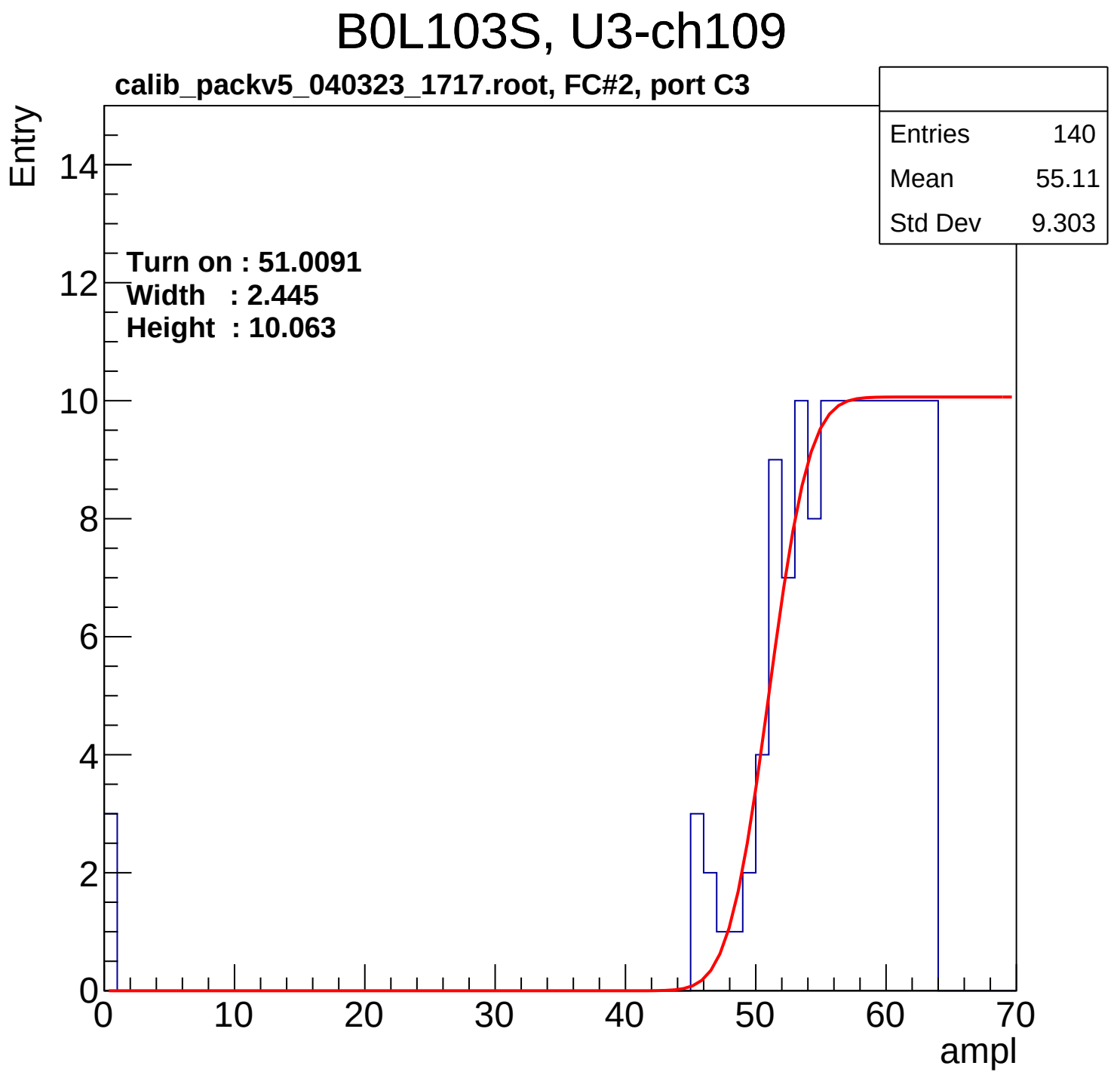
B0L103S, U3-ch109
calib_packv5_040323_1717.root, FC#2, port C3
Entries 140
Mean 55.11
Std Dev 9.303
Turn on : 51.0091
Width : 2.445
Height : 10.063
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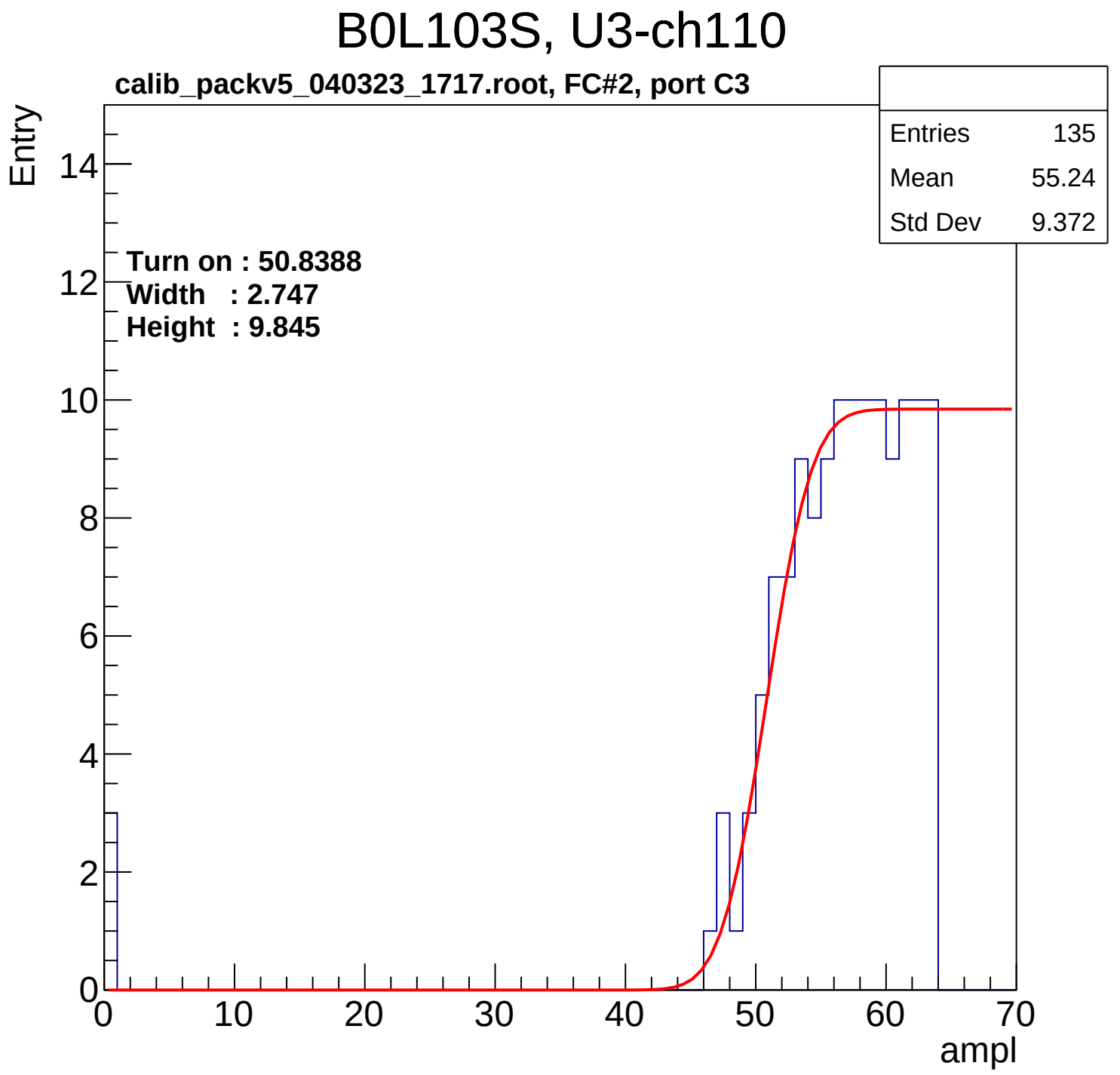
B0L103S, U3-ch110
calib_packv5_040323_1717.root, FC#2, port C3
Entries 135
Mean 55.24
Std Dev 9.372
Turn on : 50.8388
Width : 2.747
Height : 9.845
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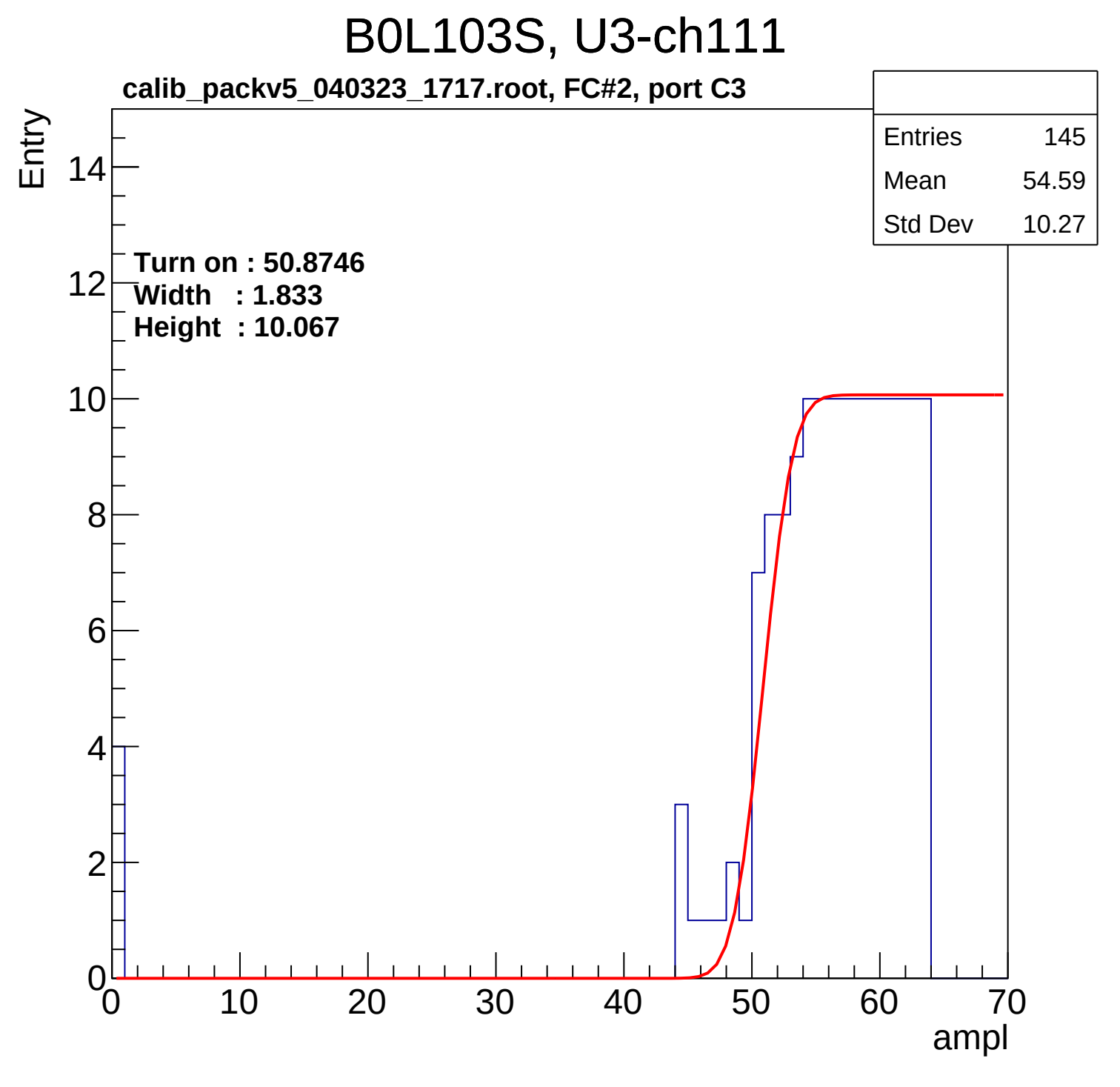
B0L103S, U3-ch111
calib_packv5_040323_1717.root, FC#2, port C3
Entries 145
Mean 54.59
Std Dev 10.27
Turn on : 50.8746
Width : 1.833
Height : 10.067
Entry
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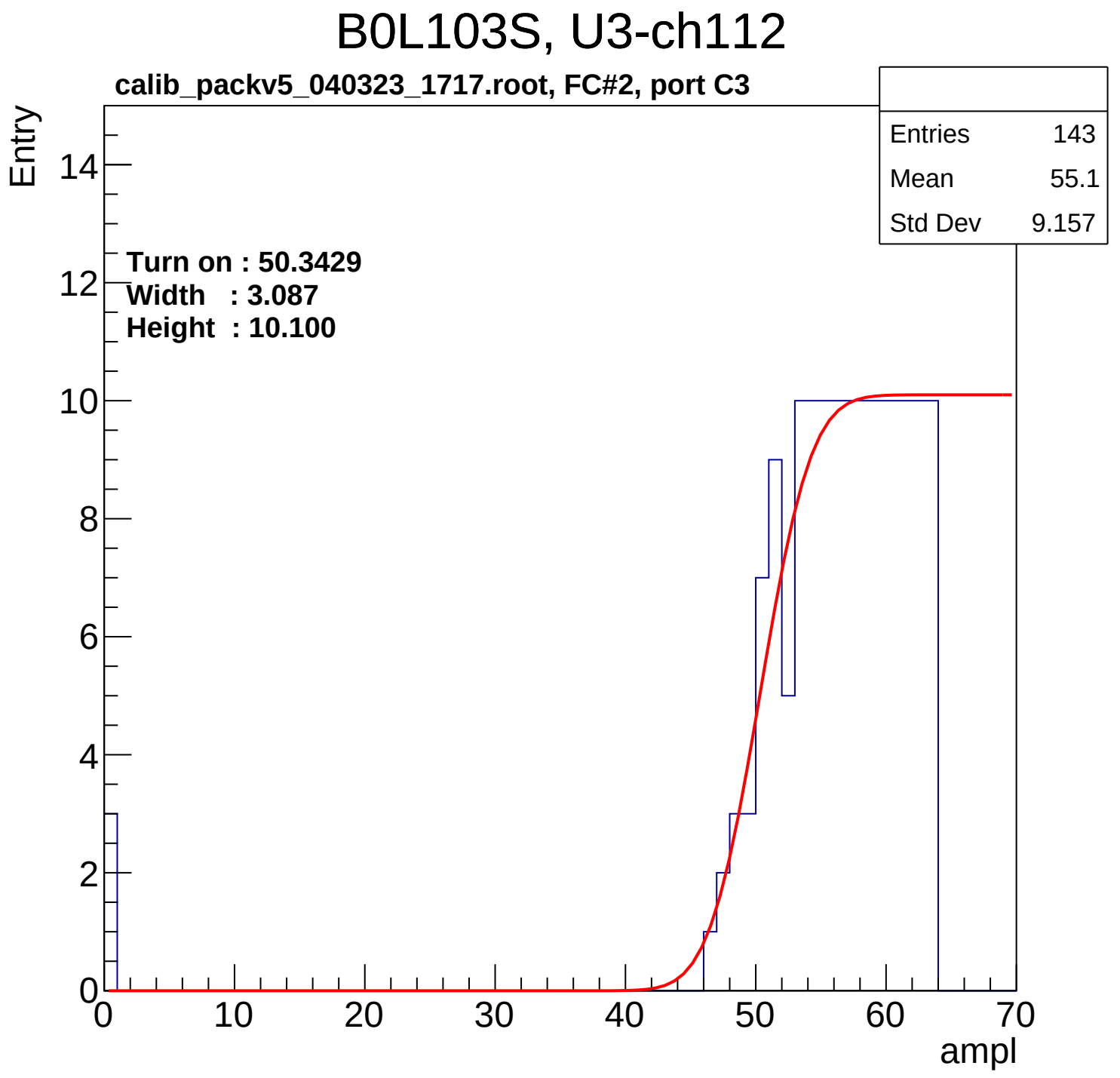
B0L103S, U3-ch112
calib_packv5_040323_1717.root, FC#2, port C3
Entries 143
Mean 55.1
Std Dev 9.157
Turn on : 50.3429
Width : 3.087
Height : 10.100
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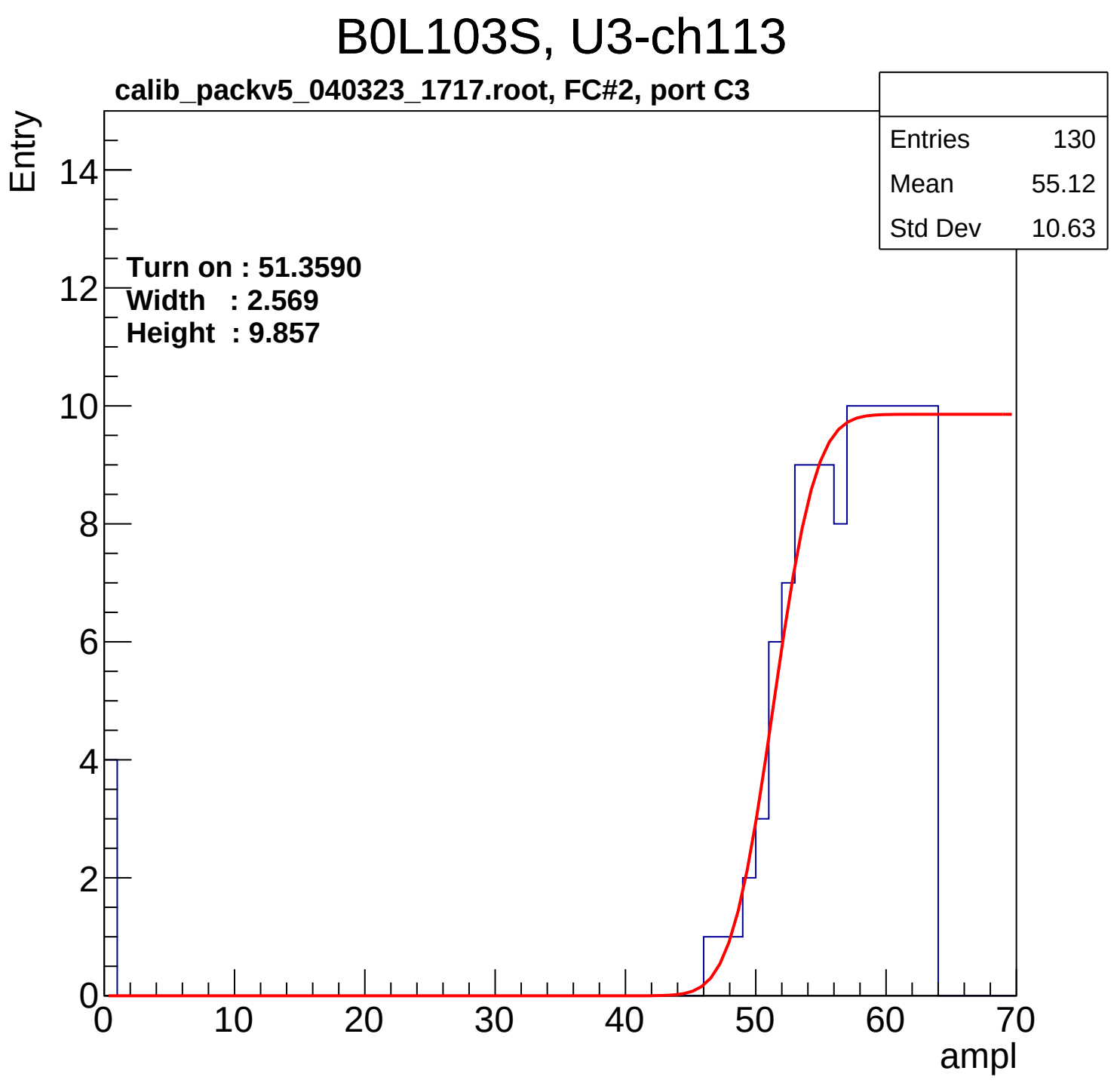
B0L103S, U3-ch113
calib_packv5_040323_1717.root, FC#2, port C3
Entries 130
Mean 55.12
Std Dev 10.63
Turn on : 51.3590
Width : 2.569
Height : 9.857
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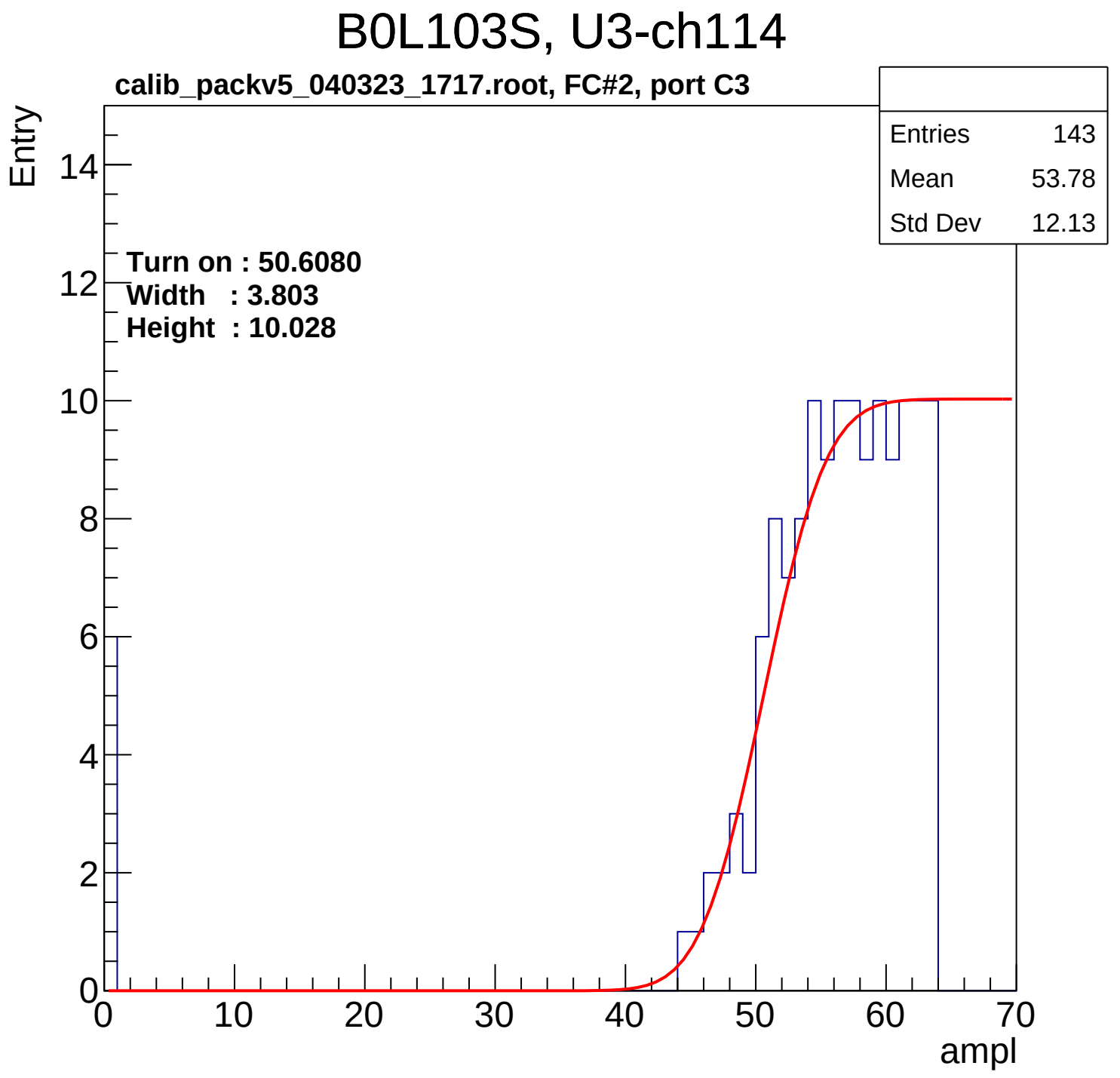
B0L103S, U3-ch114
calib_packv5_040323_1717.root, FC#2, port C3
Entries 143
Mean 53.78
Std Dev 12.13
Turn on : 50.6080
Width : 3.803
Height : 10.028
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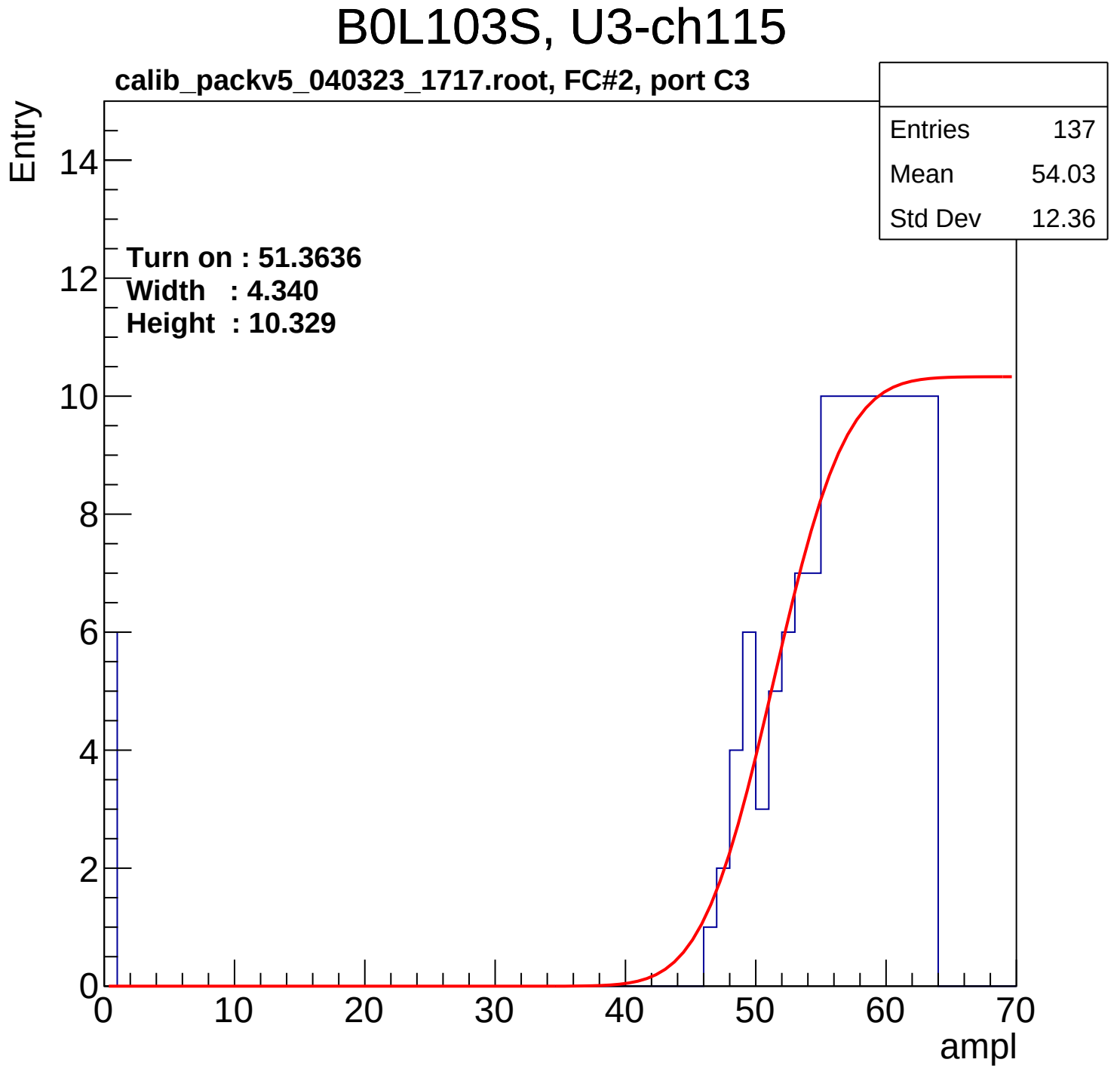
B0L103S, U3-ch115
calib_packv5_040323_1717.root, FC#2, port C3
Entries 137
Mean 54.03
Std Dev 12.36
Turn on : 51.3636
Width : 4.340
Height : 10.329
Entry
ampl
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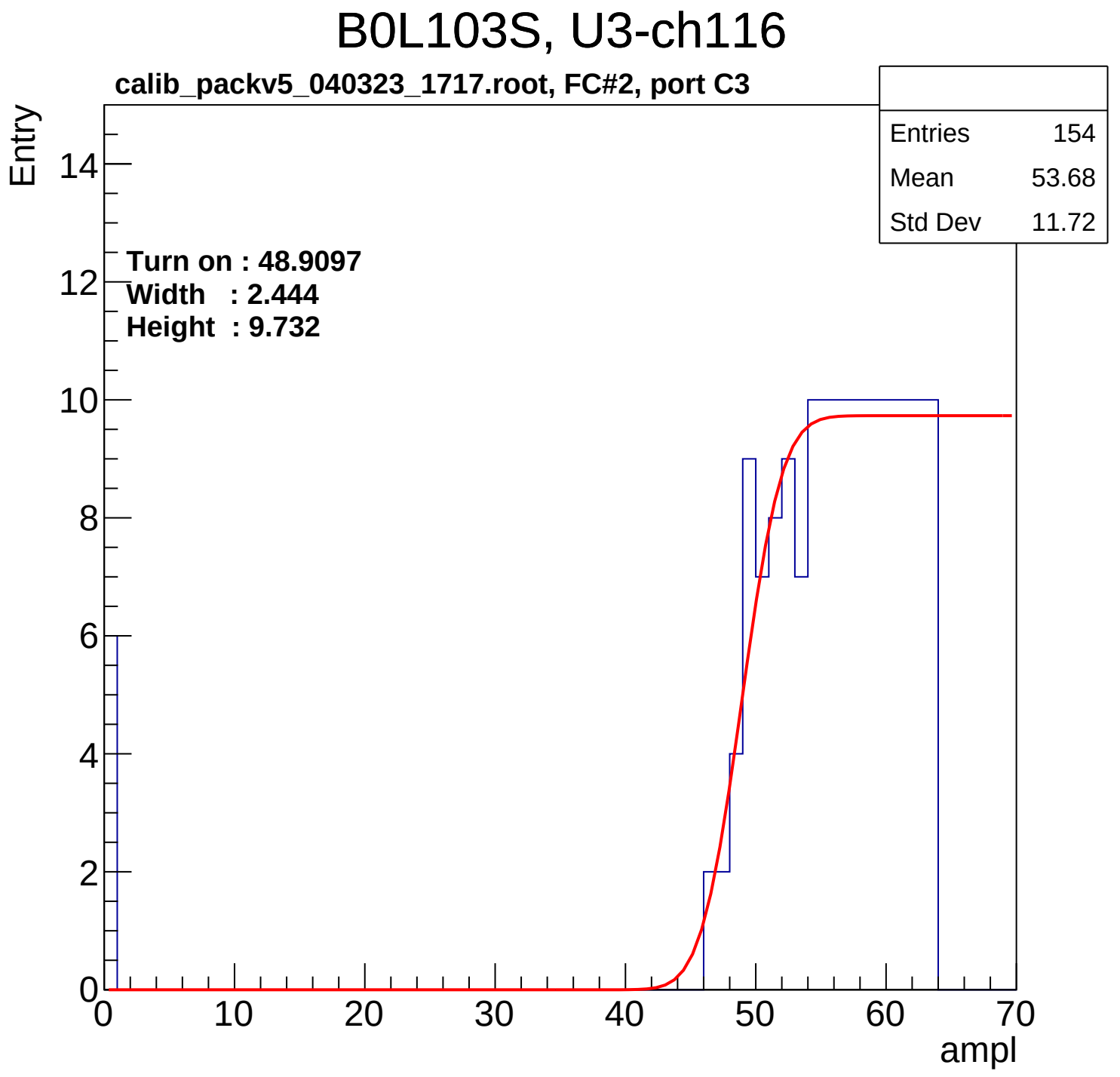
B0L103S, U3-ch116
calib_packv5_040323_1717.root, FC#2, port C3
Entries 154
Mean 53.68
Std Dev 11.72
Turn on : 48.9097
Width : 2.444
Height : 9.732
Entry
ampl
0
2
4
6
8
10
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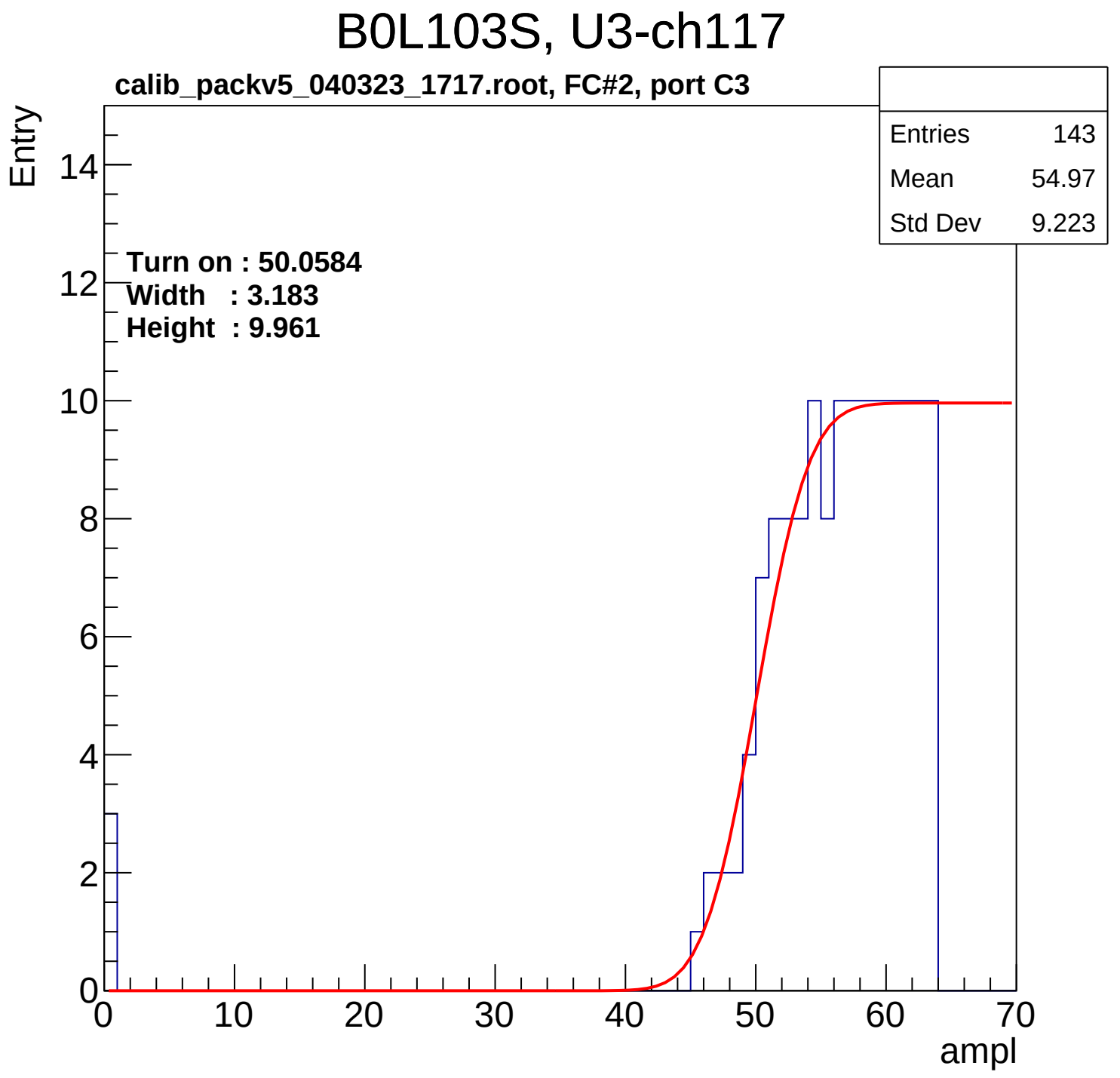
B0L103S, U3-ch117
calib_packv5_040323_1717.root, FC#2, port C3
Entries 143
Mean 54.97
Std Dev 9.223
Turn on : 50.0584
Width : 3.183
Height : 9.961
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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40
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60
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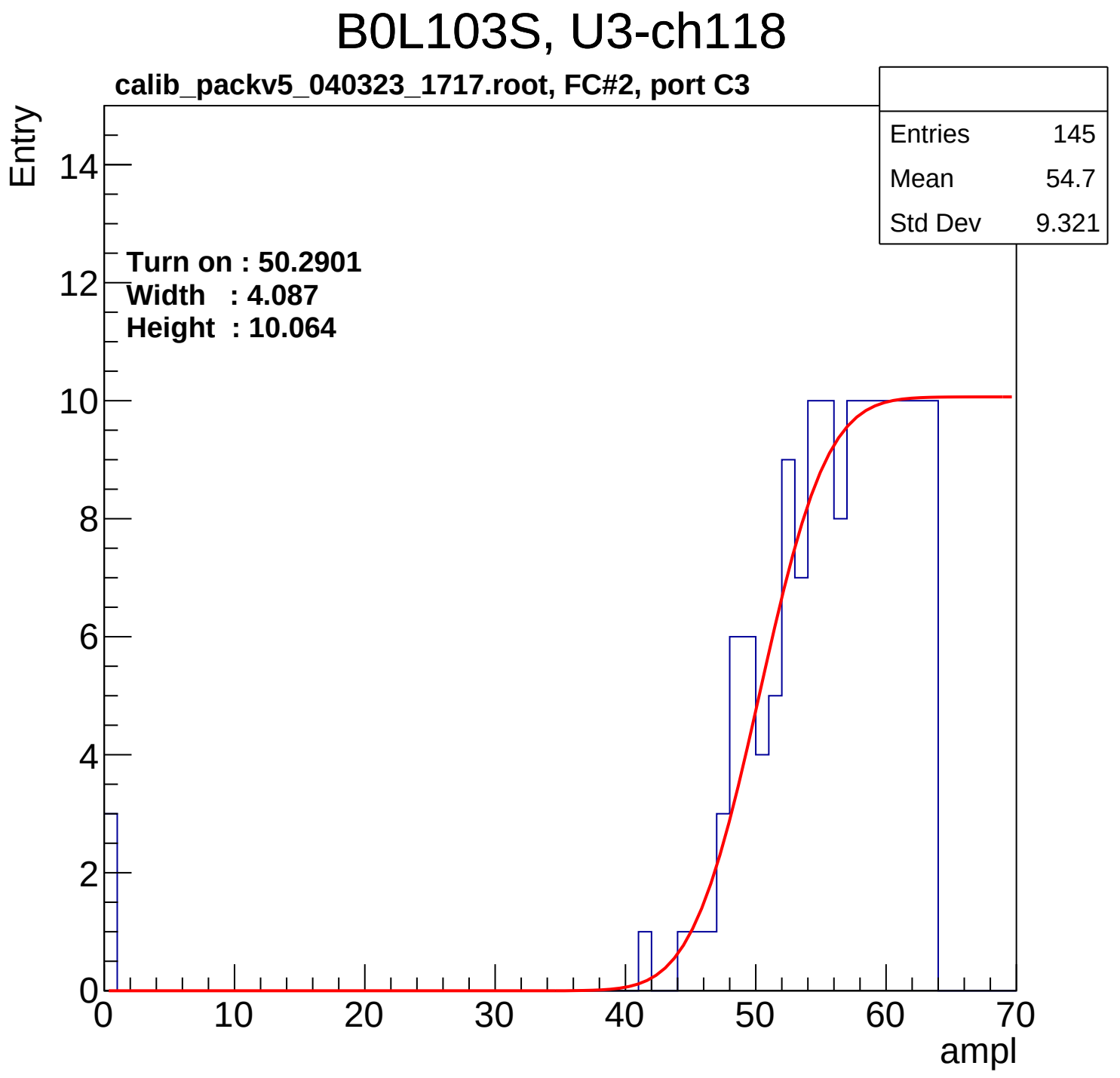
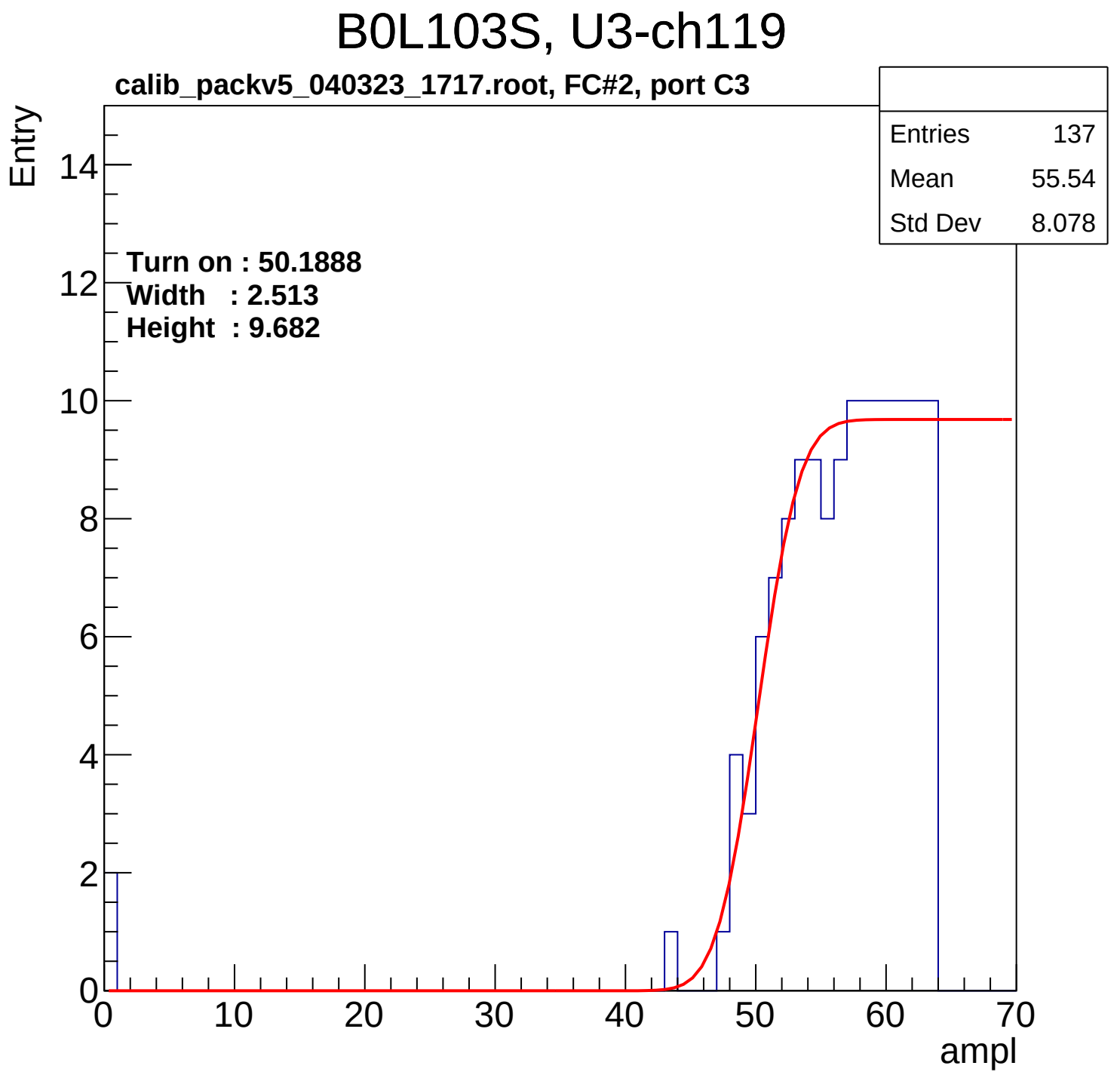
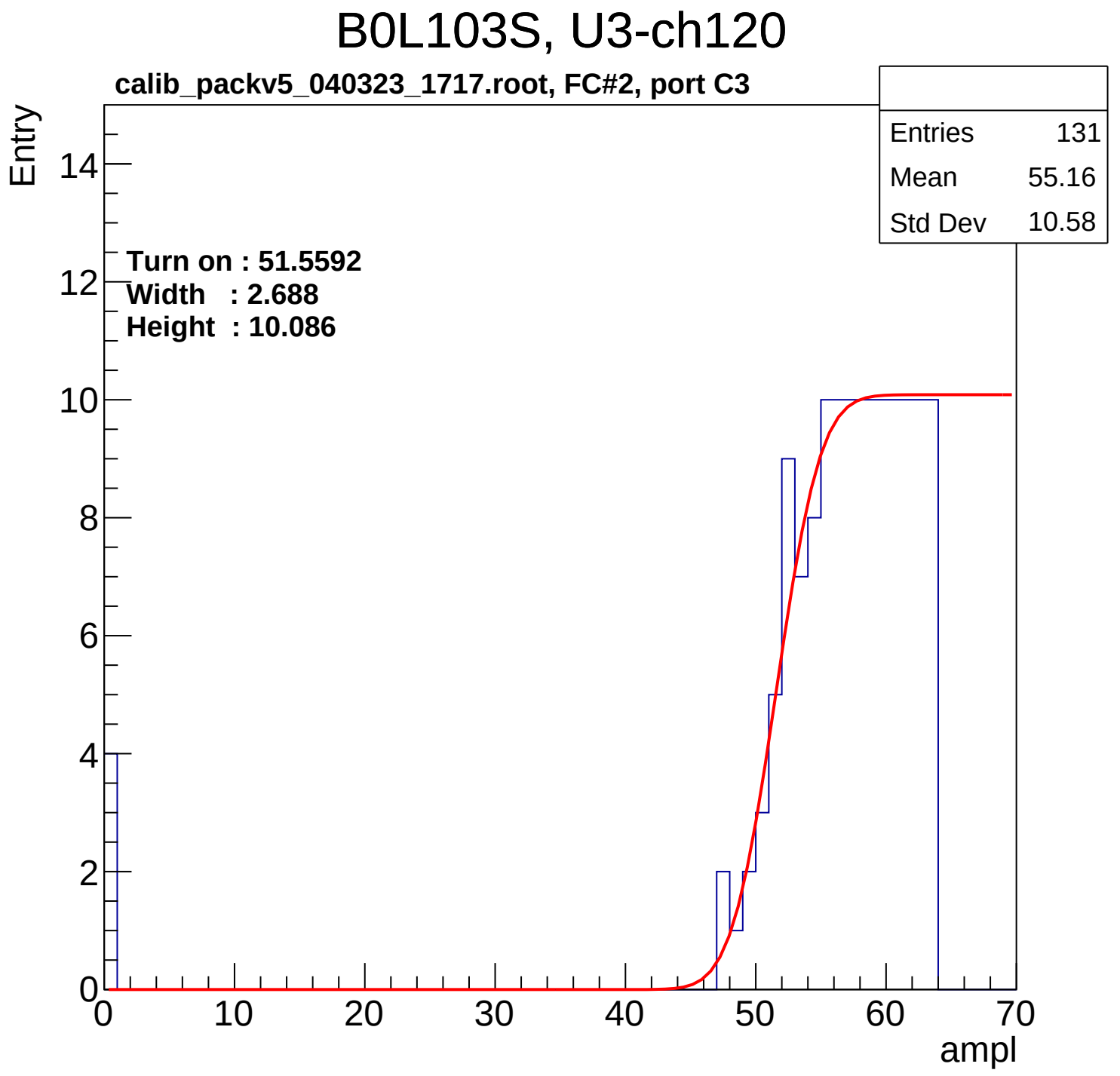
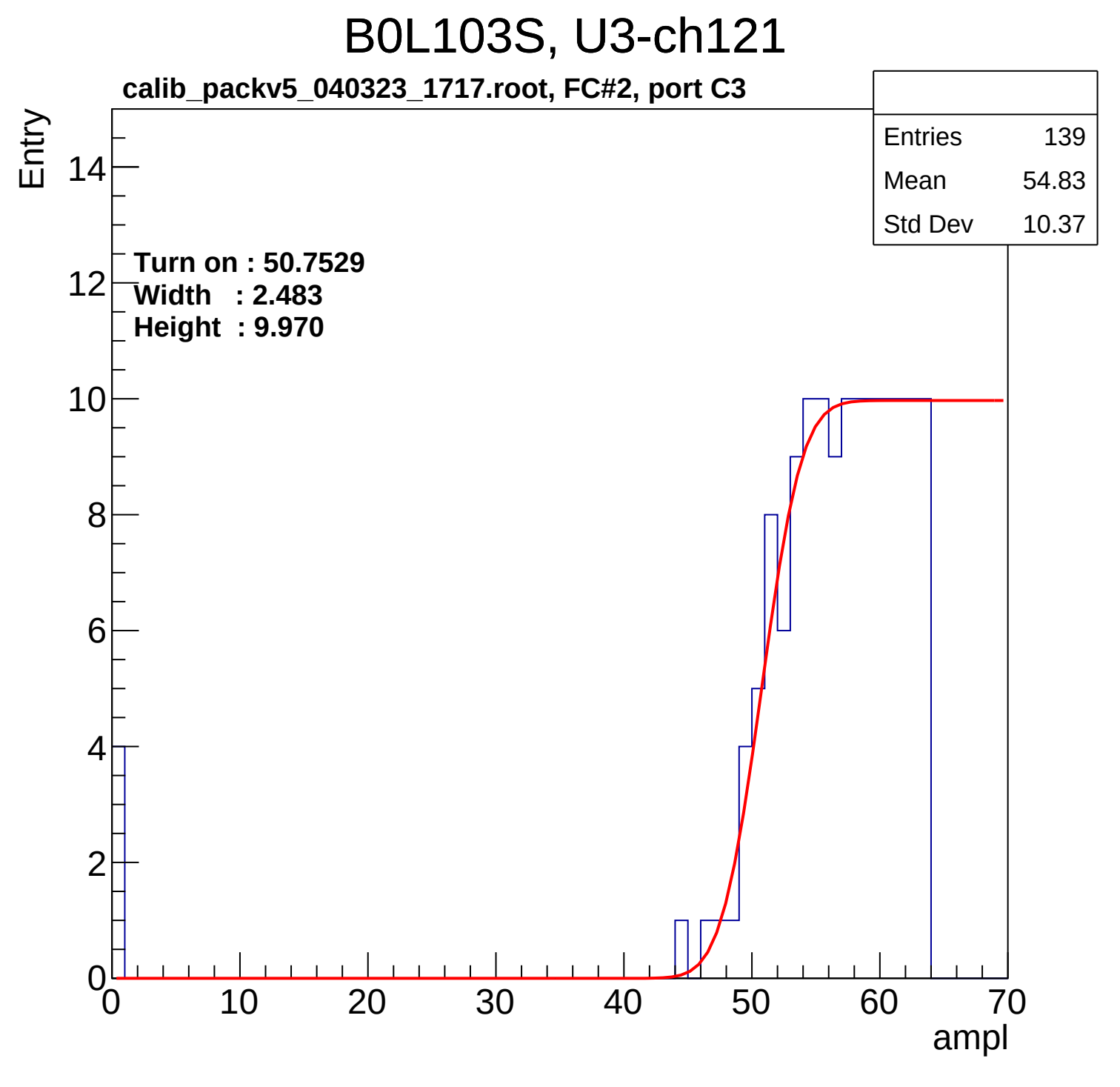
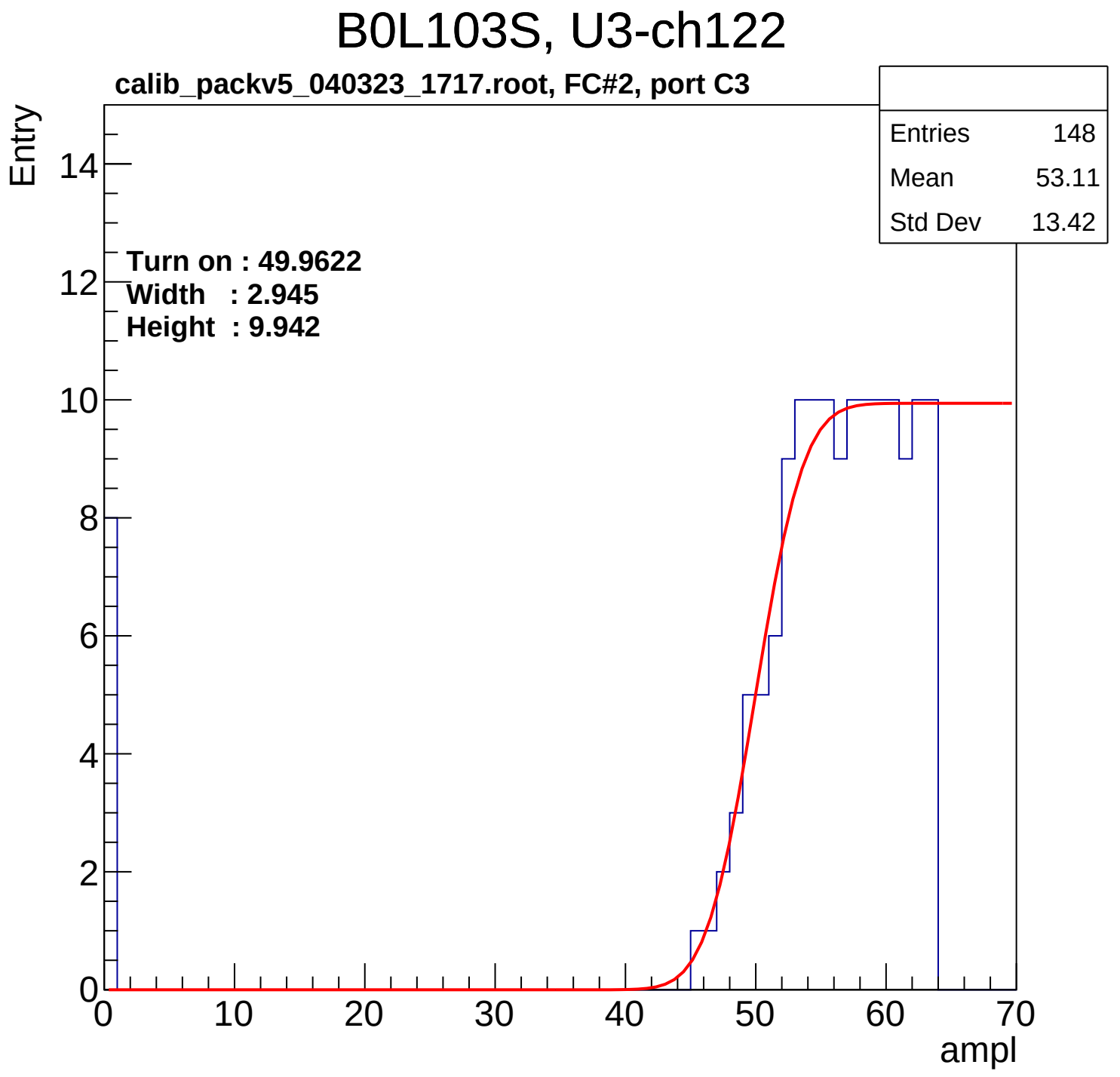
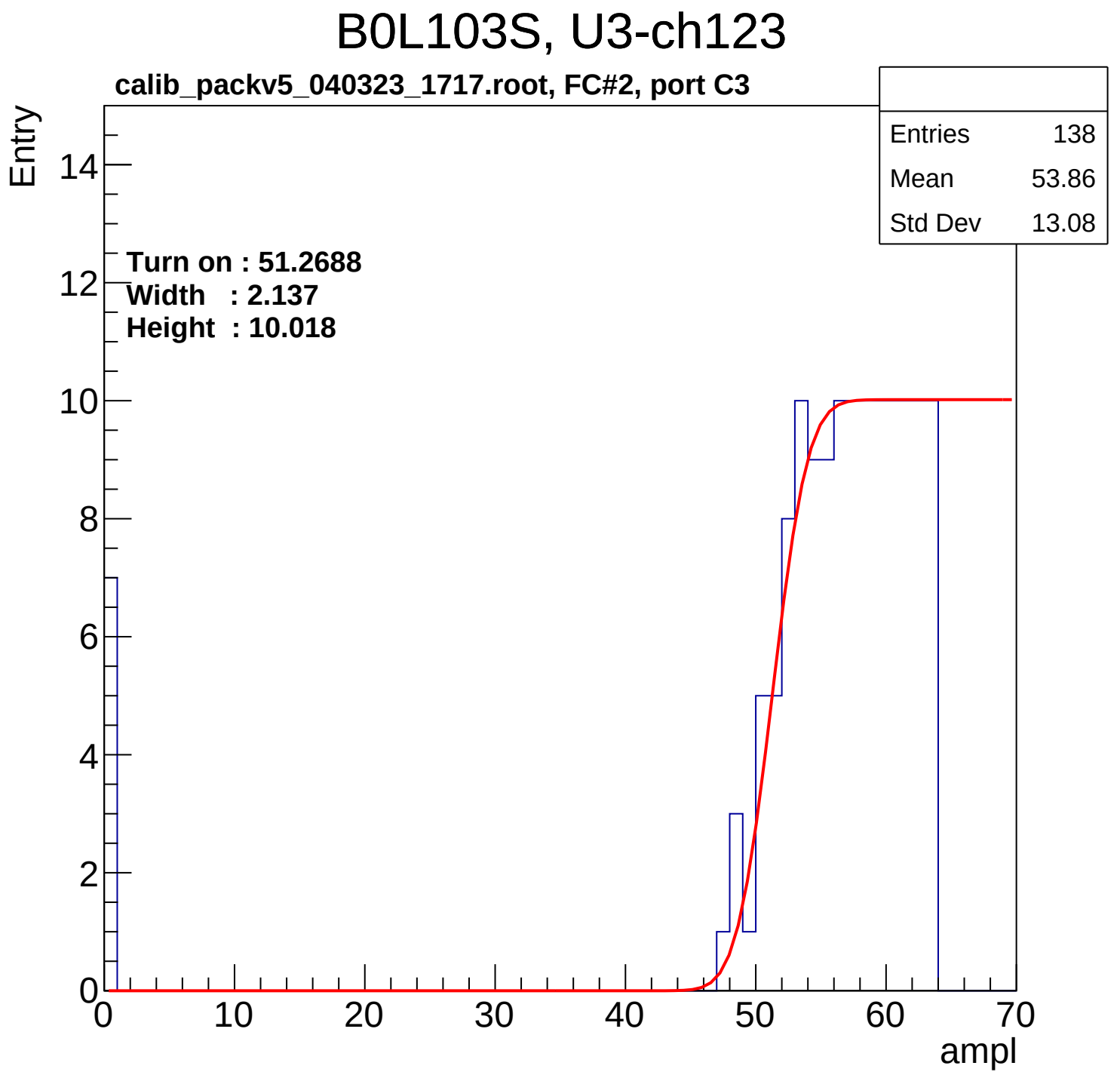

B0L103S, U3-ch118
calib_packv5_040323_1717.root, FC#2, port C3
Entries 145
Mean 54.7
Std Dev 9.321
Turn on : 50.2901
Width : 4.087
Height : 10.064
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L103S, U3-ch119
calib_packv5_040323_1717.root, FC#2, port C3
Entries 137
Mean 55.54
Std Dev 8.078
Turn on : 50.1888
Width : 2.513
Height : 9.682
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L103S, U3-ch120
calib_packv5_040323_1717.root, FC#2, port C3
Entries 131
Mean 55.16
Std Dev 10.58
Turn on : 51.5592
Width : 2.688
Height : 10.086
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L103S, U3-ch121
calib_packv5_040323_1717.root, FC#2, port C3
Entries 139
Mean 54.83
Std Dev 10.37
Turn on : 50.7529
Width : 2.483
Height : 9.970
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L103S, U3-ch122
calib_packv5_040323_1717.root, FC#2, port C3
Entries 148
Mean 53.11
Std Dev 13.42
Turn on : 49.9622
Width : 2.945
Height : 9.942
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L103S, U3-ch123
calib_packv5_040323_1717.root, FC#2, port C3
Entries 138
Mean 53.86
Std Dev 13.08
Turn on : 51.2688
Width : 2.137
Height : 10.018
Entry
ampl
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2
4
6
8
10
12
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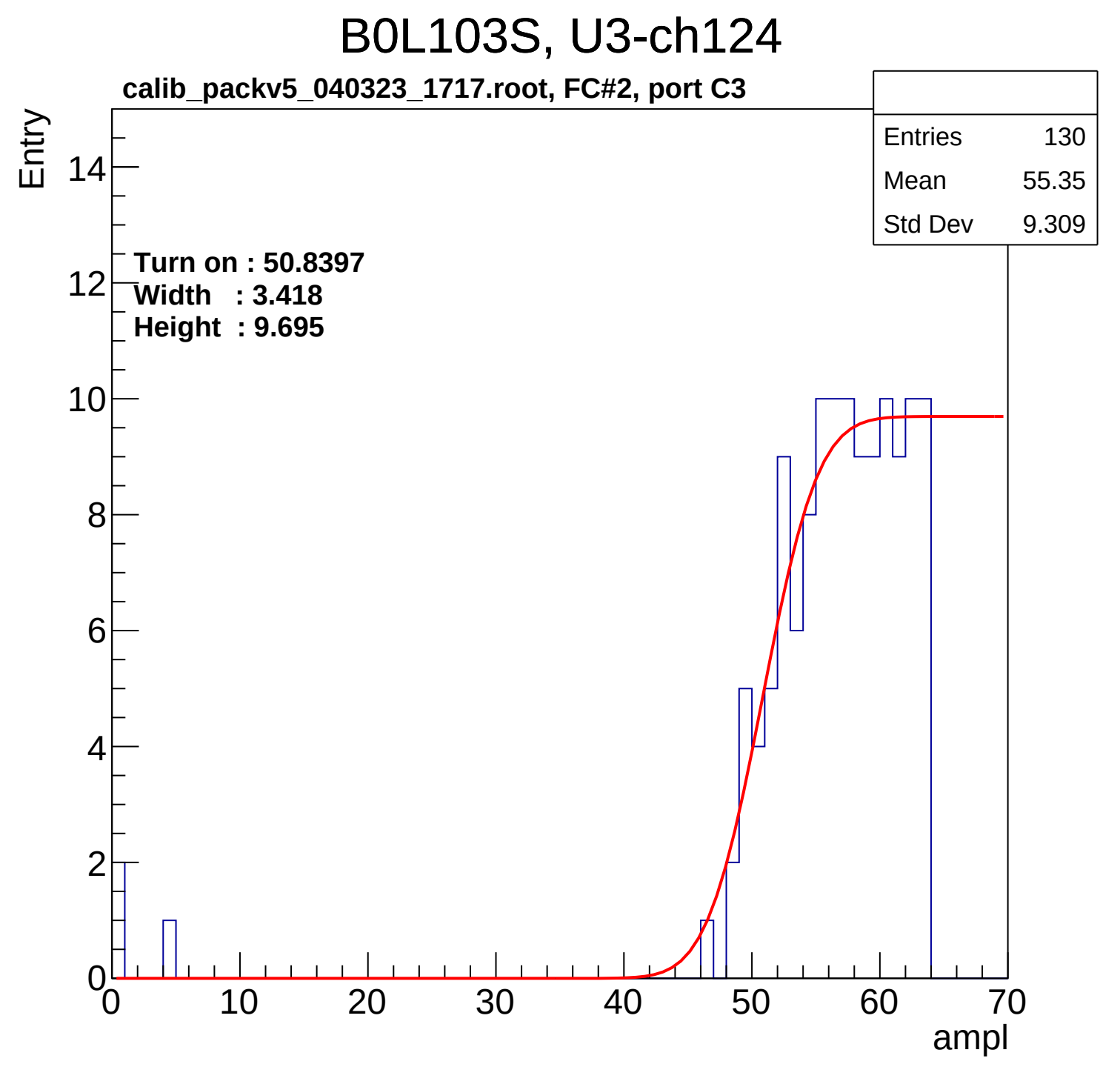
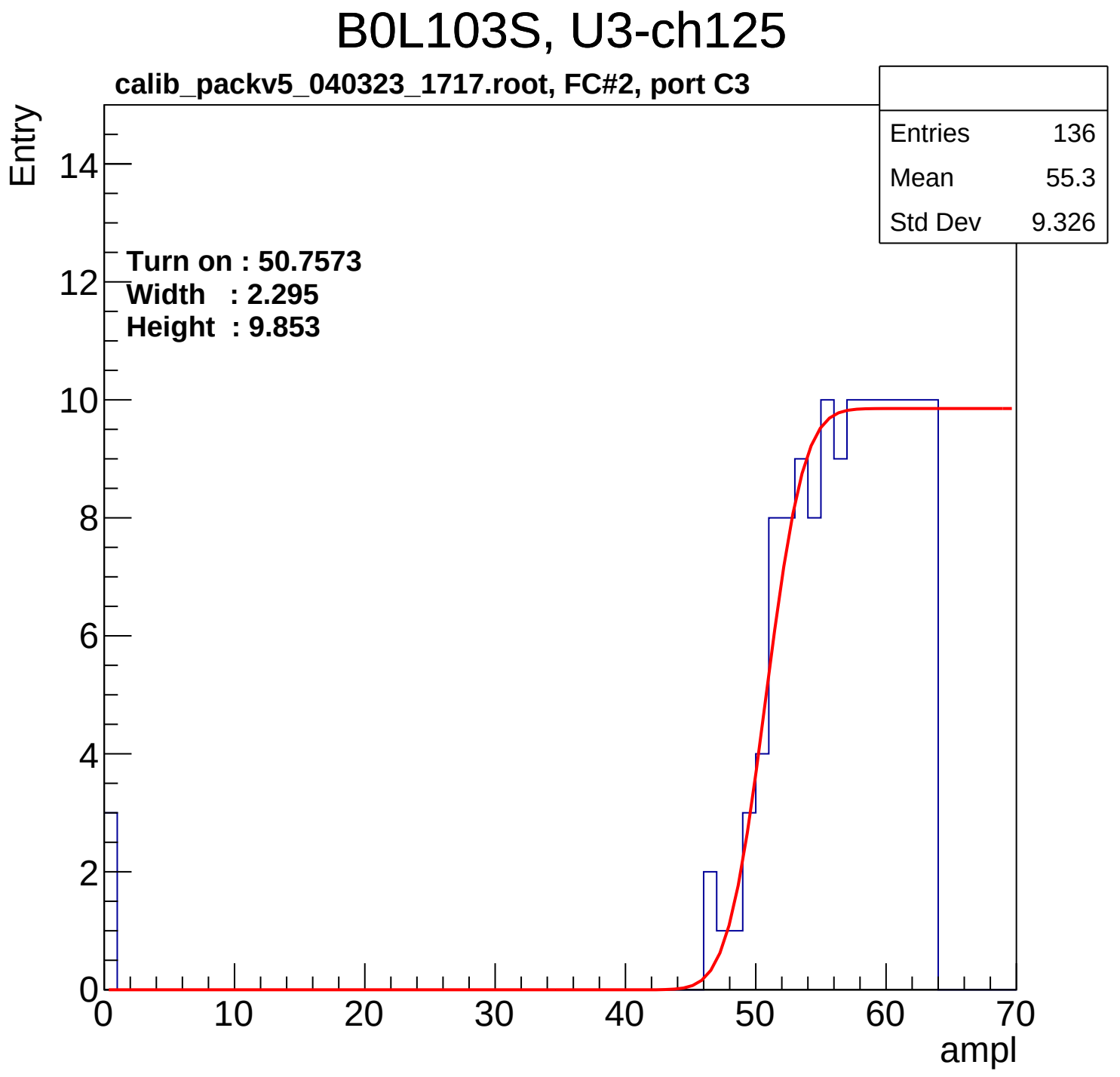
0
10
20
30
40
50
60
70


B0L103S, U3-ch124
calib_packv5_040323_1717.root, FC#2, port C3
Entries 130
Mean 55.35
Std Dev 9.309
Turn on : 50.8397
Width : 3.418
Height : 9.695
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L103S, U3-ch125
calib_packv5_040323_1717.root, FC#2, port C3
Entries 136
Mean 55.3
Std Dev 9.326
Turn on : 50.7573
Width : 2.295
Height : 9.853
Entry
ampl
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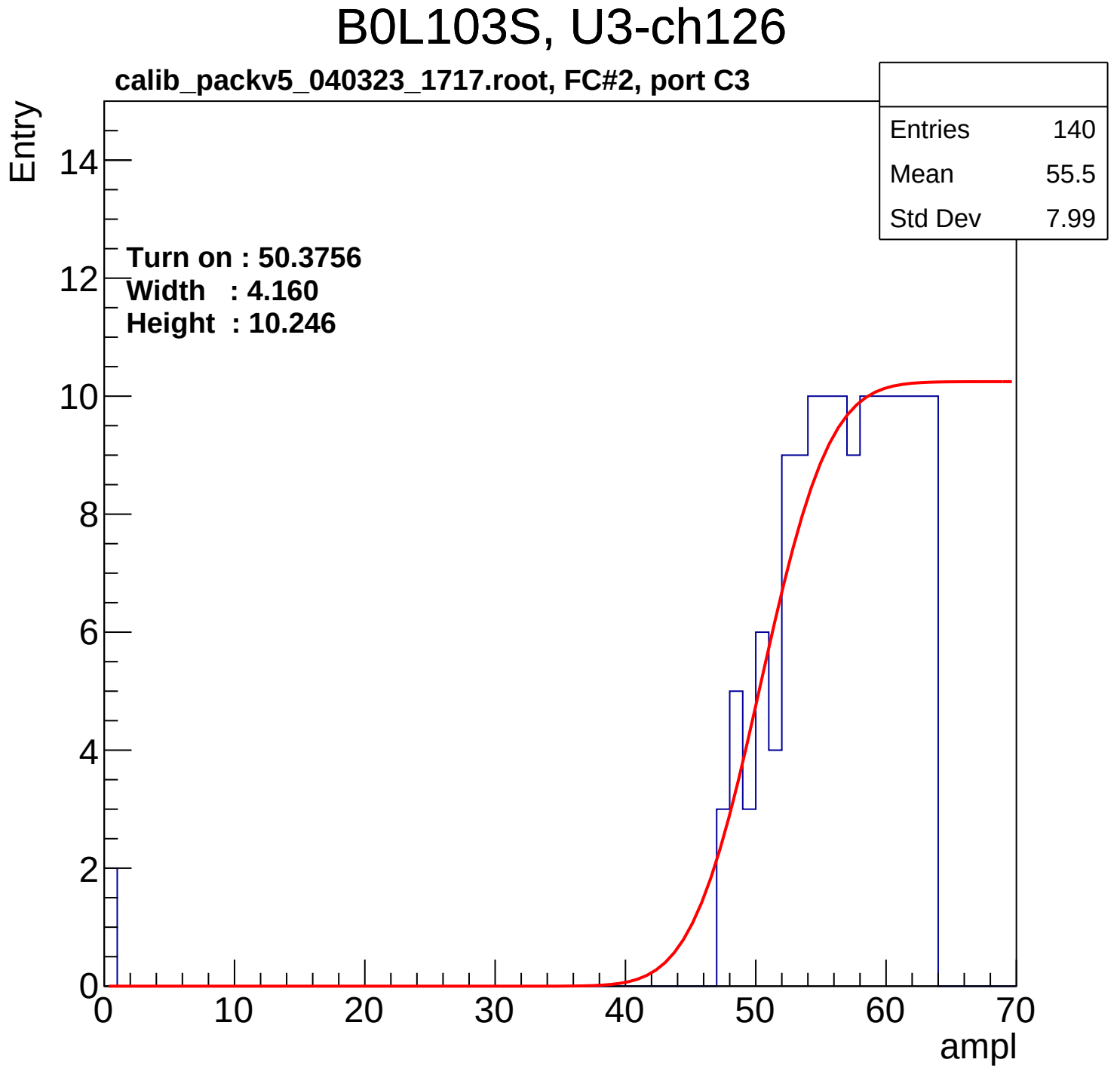
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L103S, U3-ch126
calib_packv5_040323_1717.root, FC#2, port C3
Entries 140
Mean 55.5
Std Dev 7.99
Turn on : 50.3756
Width : 4.160
Height : 10.246
Entry
ampl
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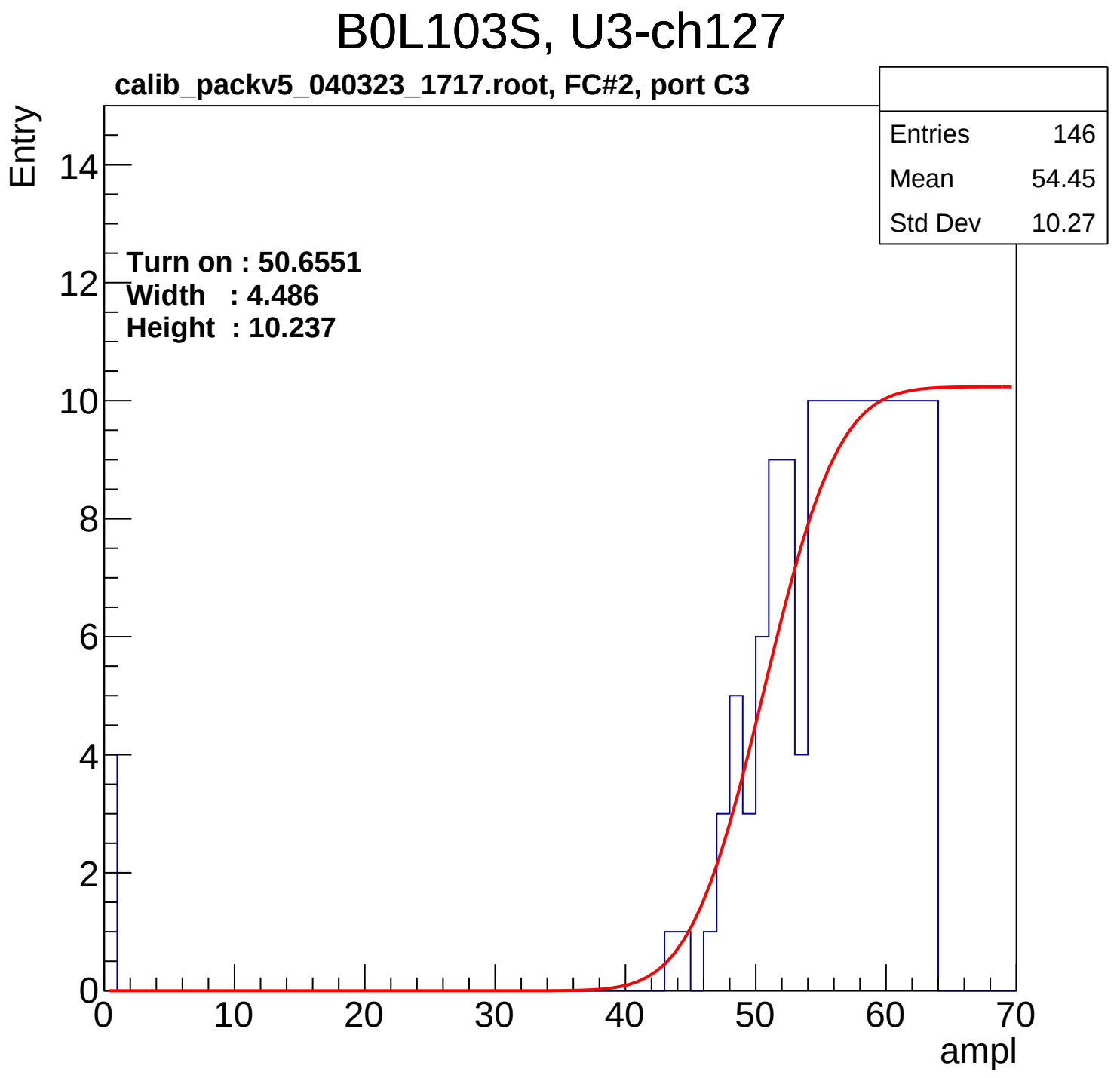
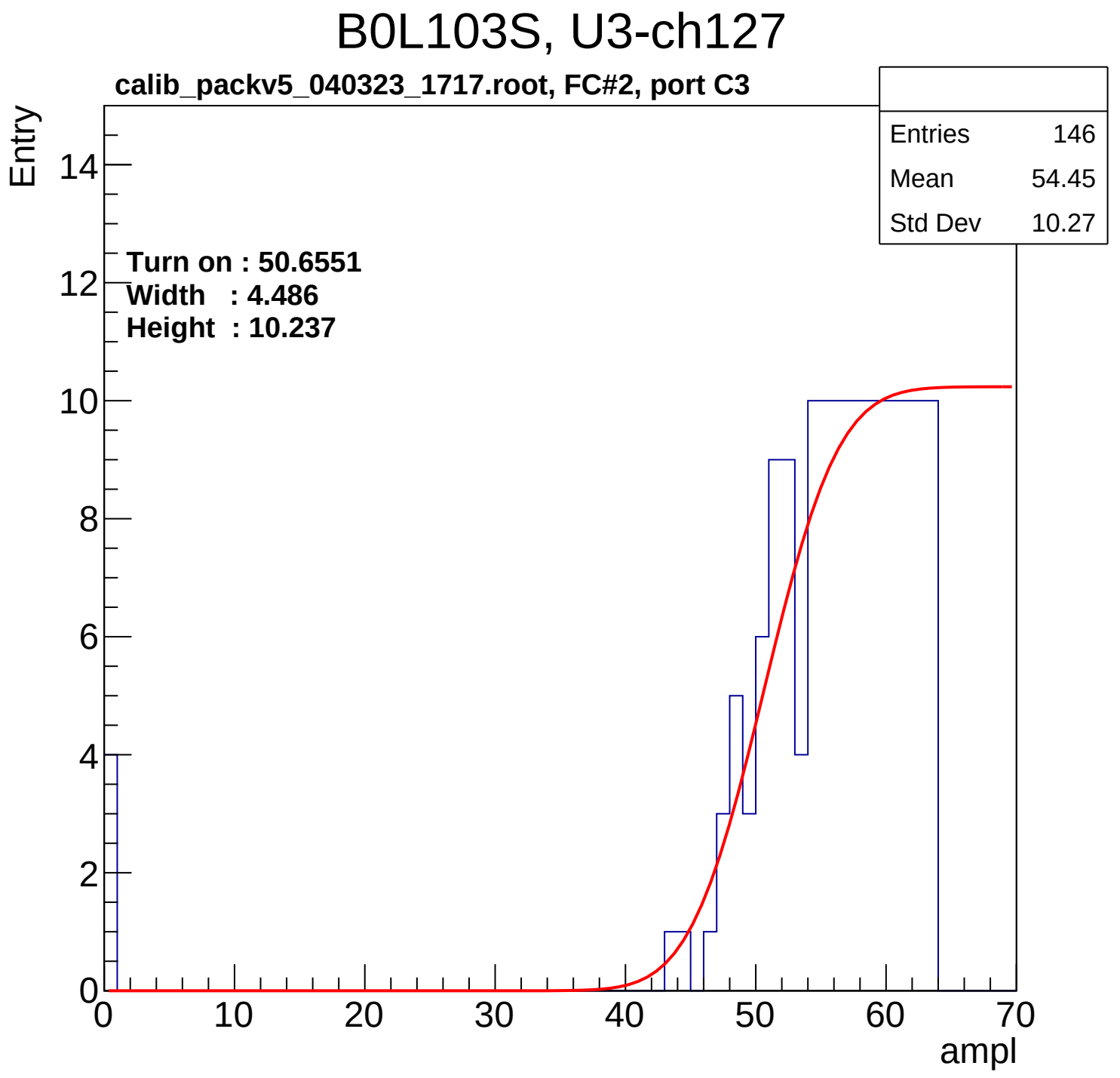
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L103S, U3-ch127
calib_packv5_040323_1717.root, FC#2, port C3
Entries 146
Mean 54.45
Std Dev 10.27
Turn on : 50.6551
Width : 4.486
Height : 10.237
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L103S, U3-ch127
calib_packv5_040323_1717.root, FC#2, port C3
Entries 146
Mean 54.45
Std Dev 10.27
Turn on : 50.6551
Width : 4.486
Height : 10.237
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70