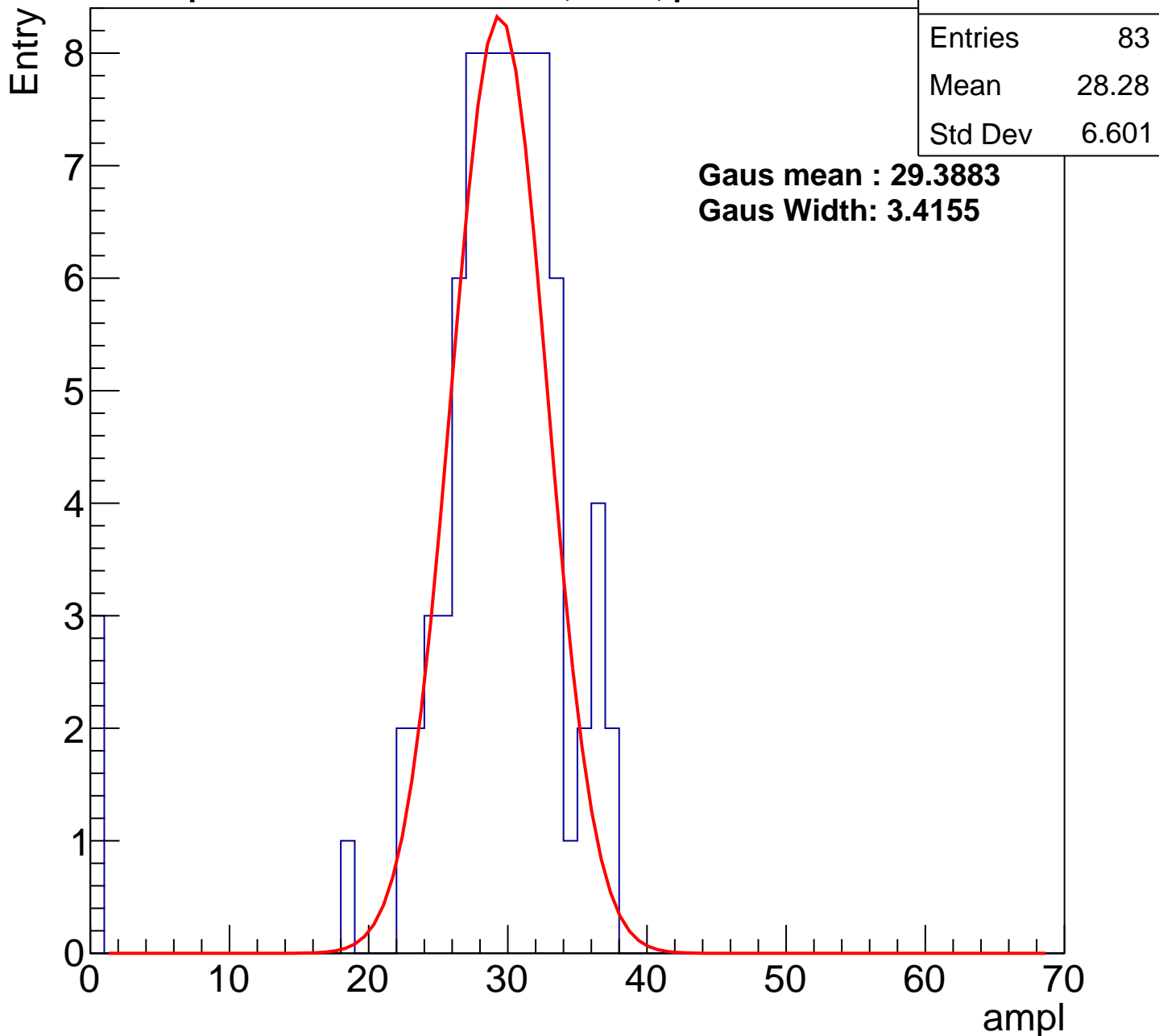




# B1L101S, U20-ch0, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U20-ch0, adc1

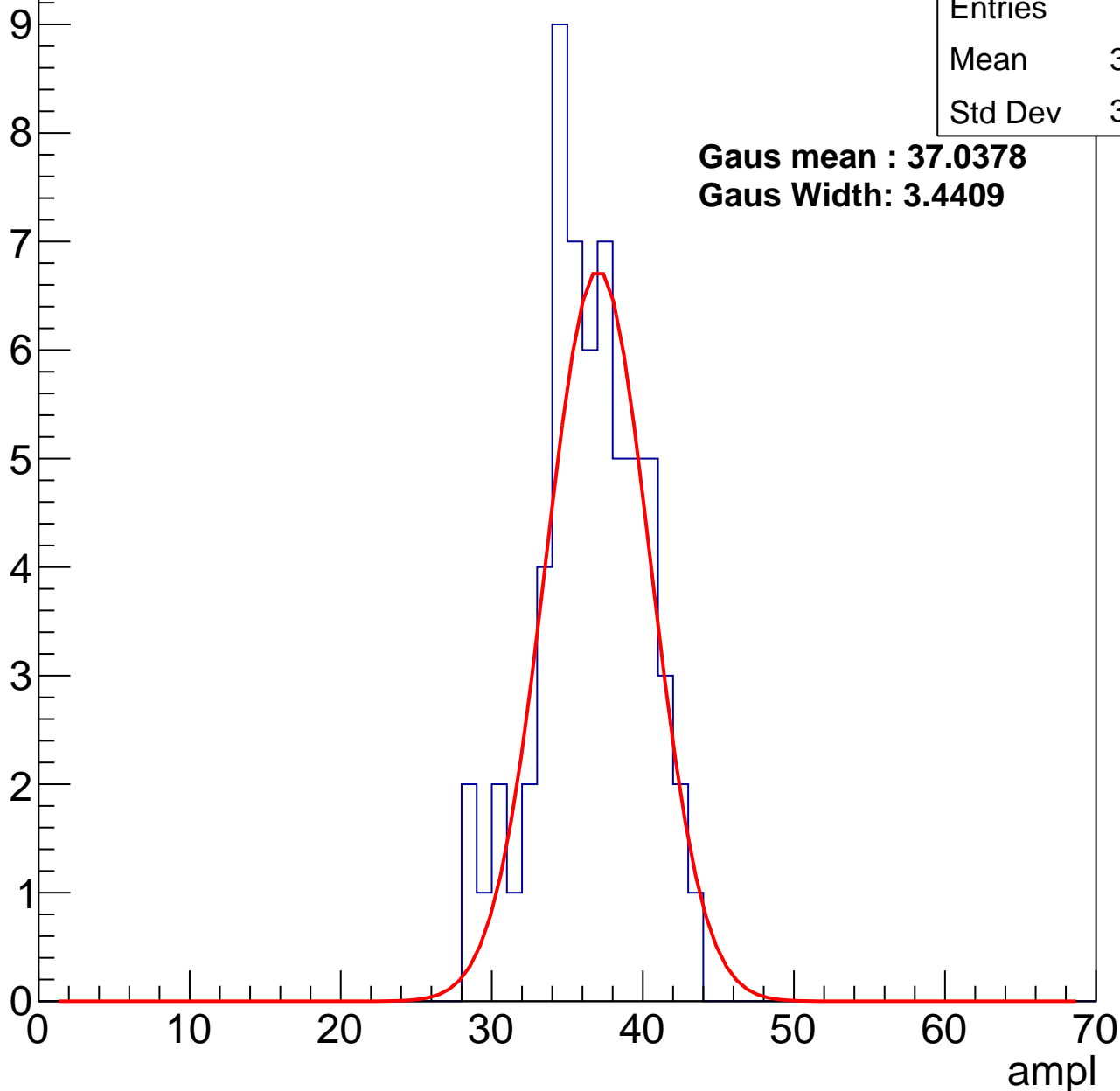
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	36.02
Std Dev	3.438

**Gaus mean : 37.0378**

**Gaus Width: 3.4409**



# B1L101S, U20-ch0, adc2

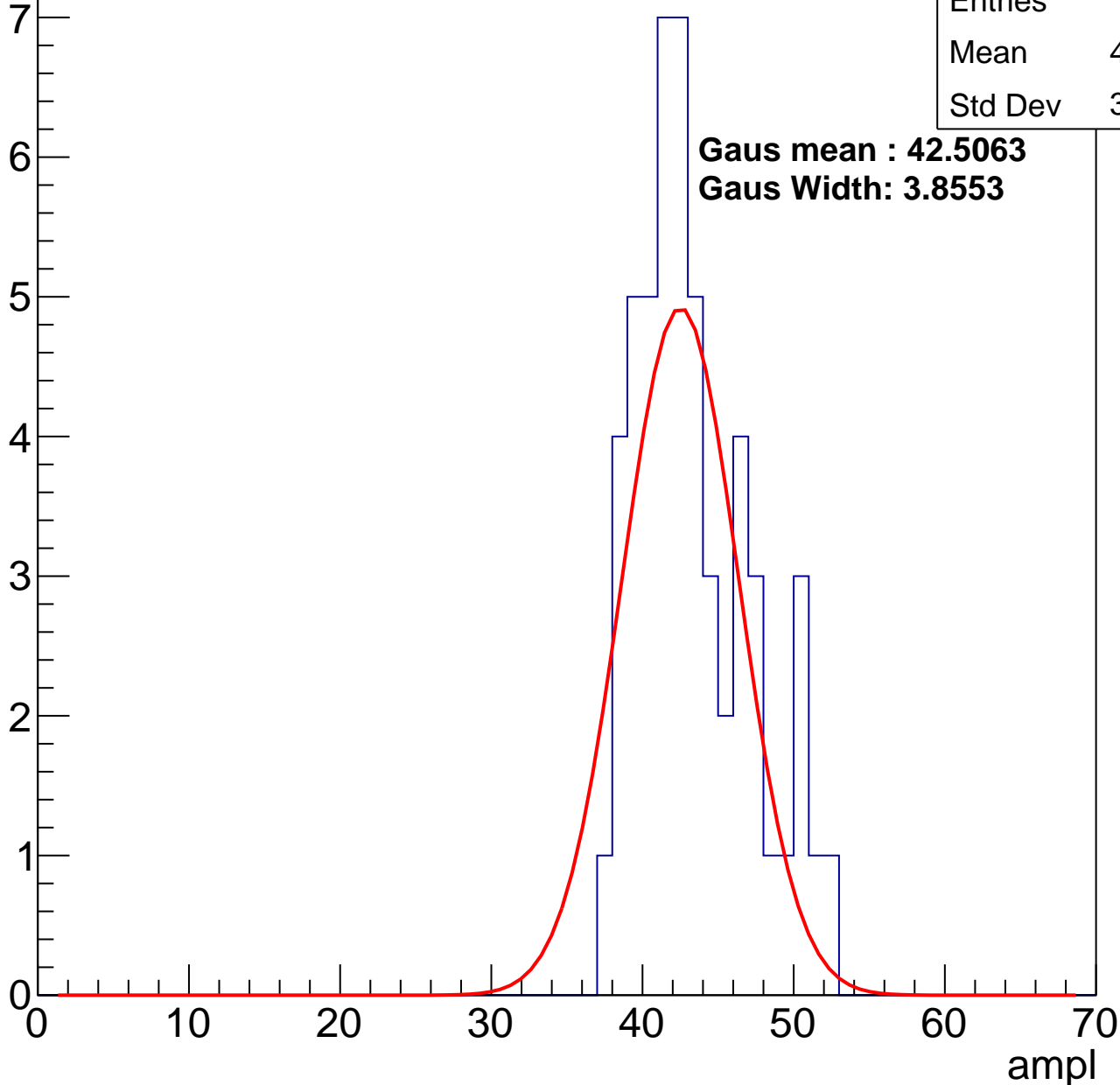
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	53
Mean	42.96
Std Dev	3.747

**Gaus mean : 42.5063**

**Gaus Width: 3.8553**

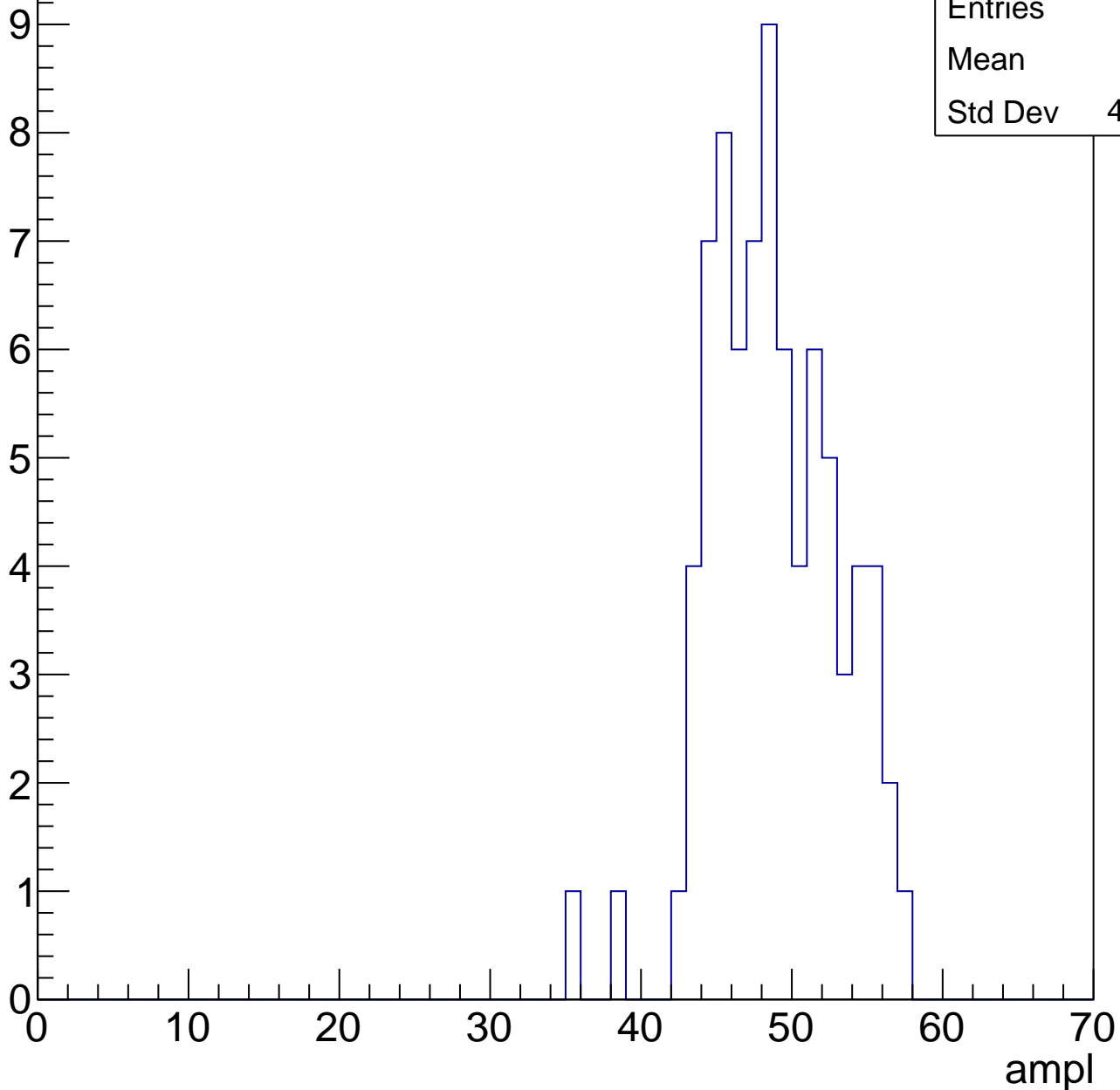


# B1L101S, U20-ch0, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	79
Mean	48.3
Std Dev	4.199

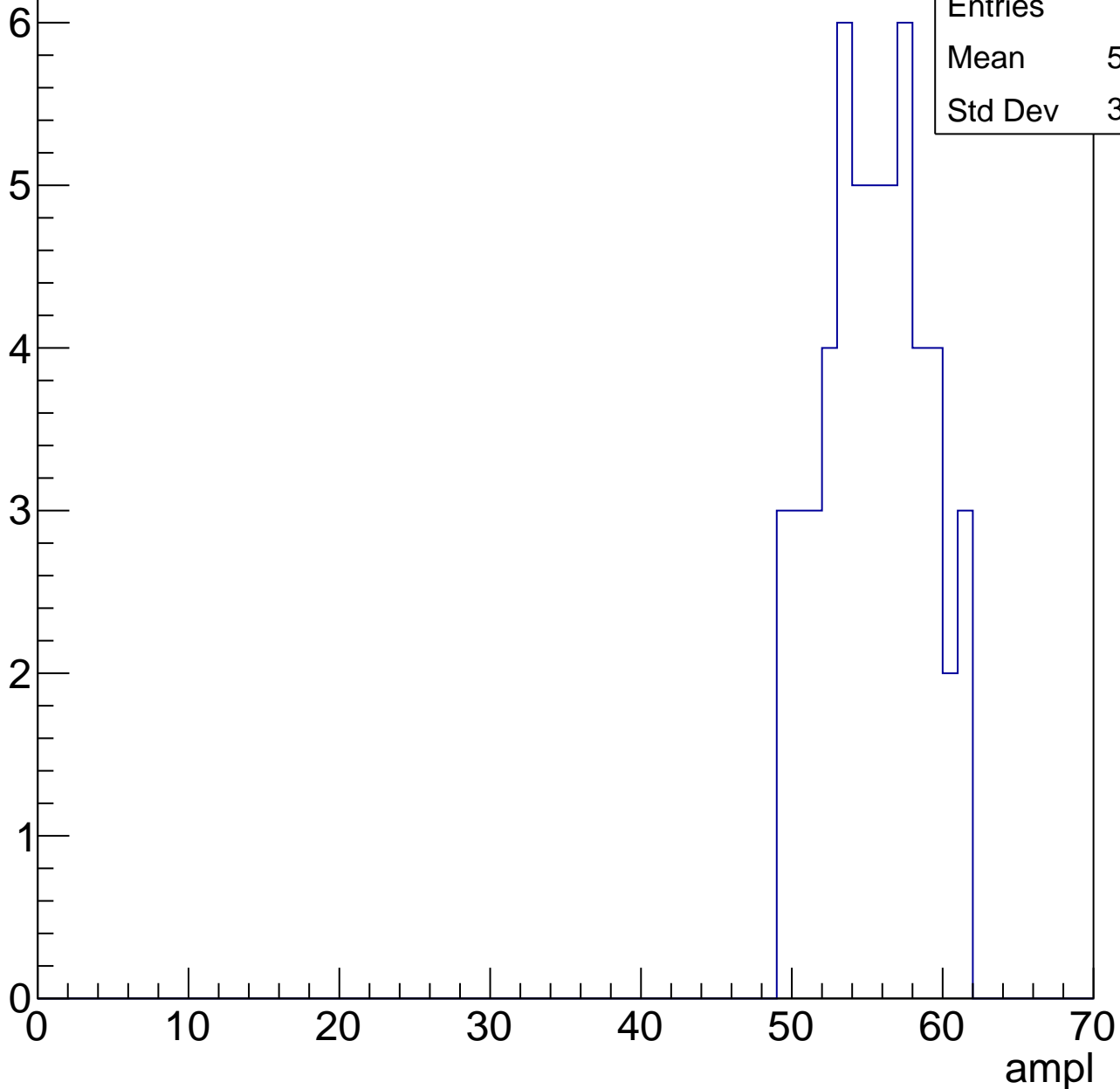


# B1L101S, U20-ch0, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	53
Mean	54.98
Std Dev	3.317

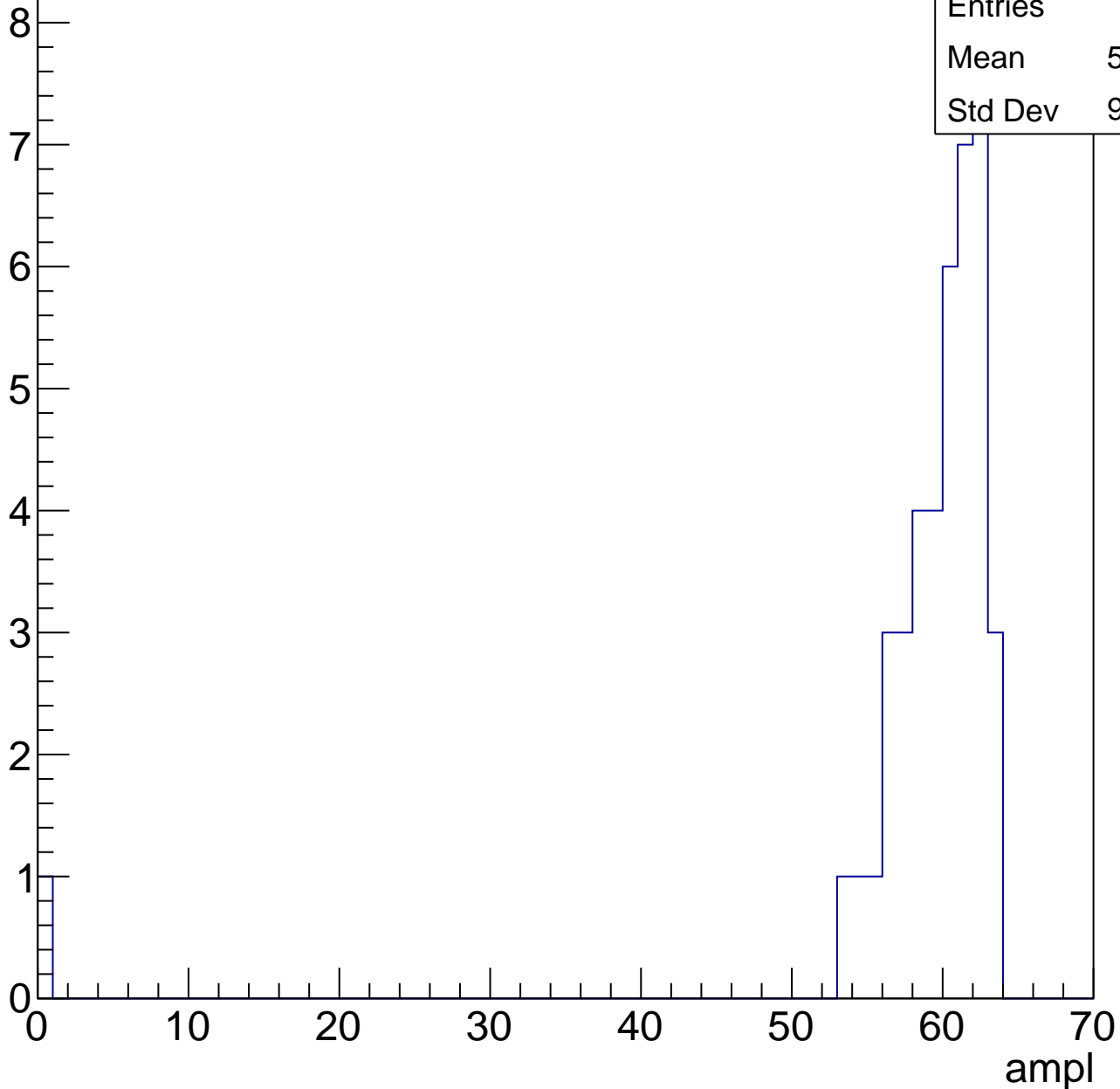


# B1L101S, U20-ch0, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	42
Mean	58.12
Std Dev	9.414

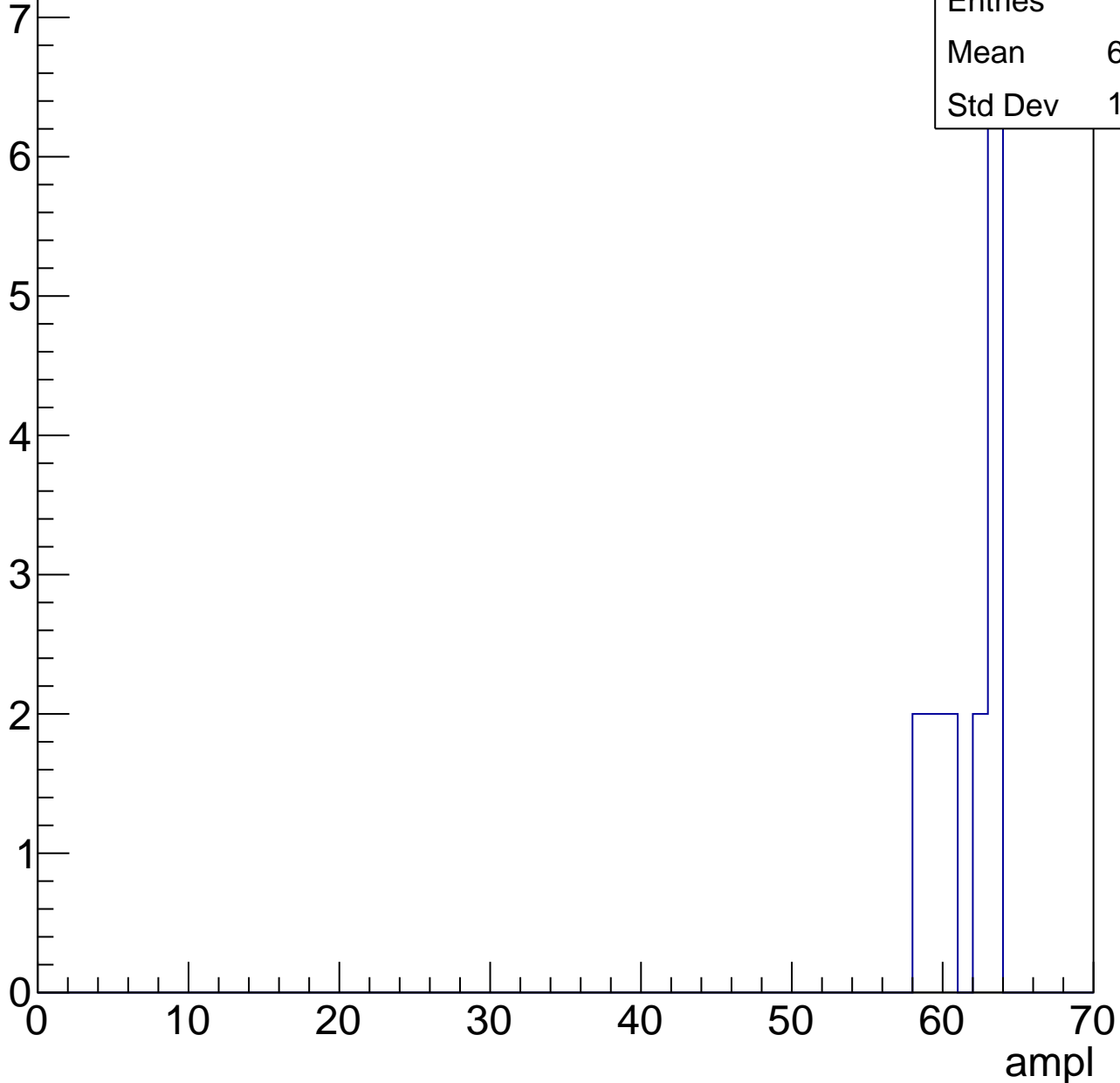


# B1L101S, U20-ch0, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	15
Mean	61.27
Std Dev	1.948





# B1L101S, U20-ch0, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U20-ch1, adc0

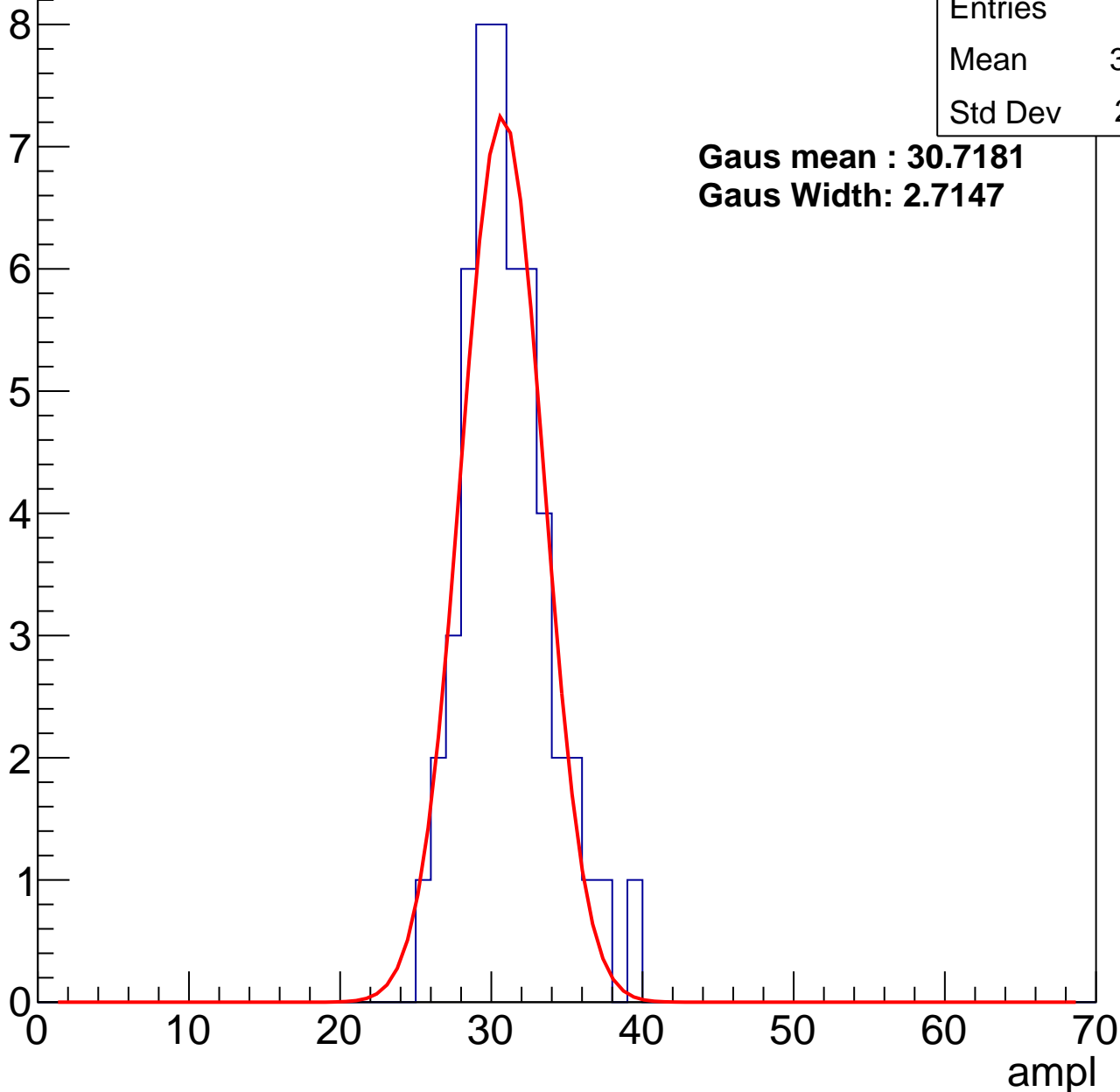
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	51
Mean	30.55
Std Dev	2.851

**Gaus mean : 30.7181**

**Gaus Width: 2.7147**



# B1L101S, U20-ch1, adc1

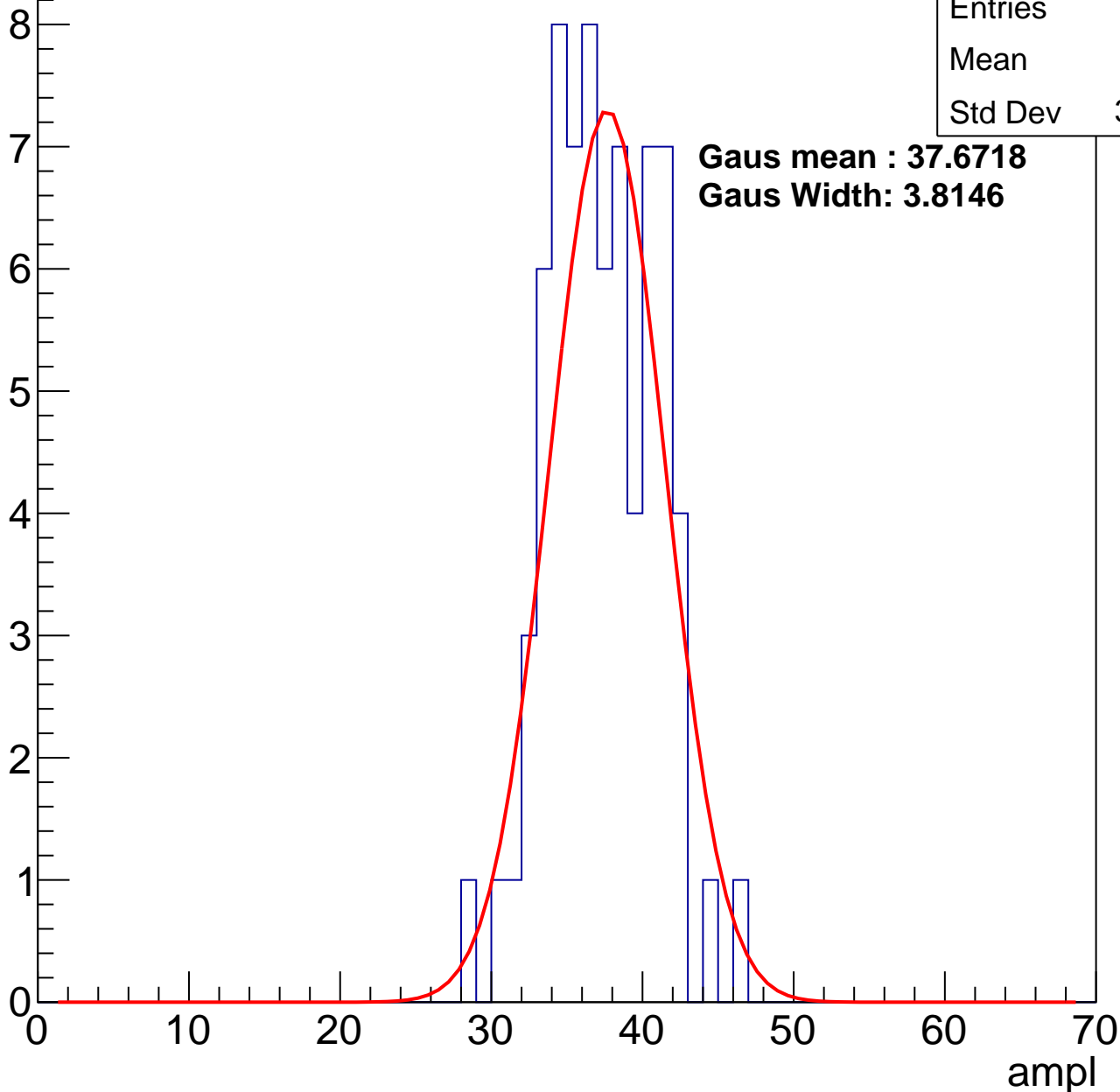
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	72
Mean	36.9
Std Dev	3.481

**Gaus mean : 37.6718**

**Gaus Width: 3.8146**



# B1L101S, U20-ch1, adc2

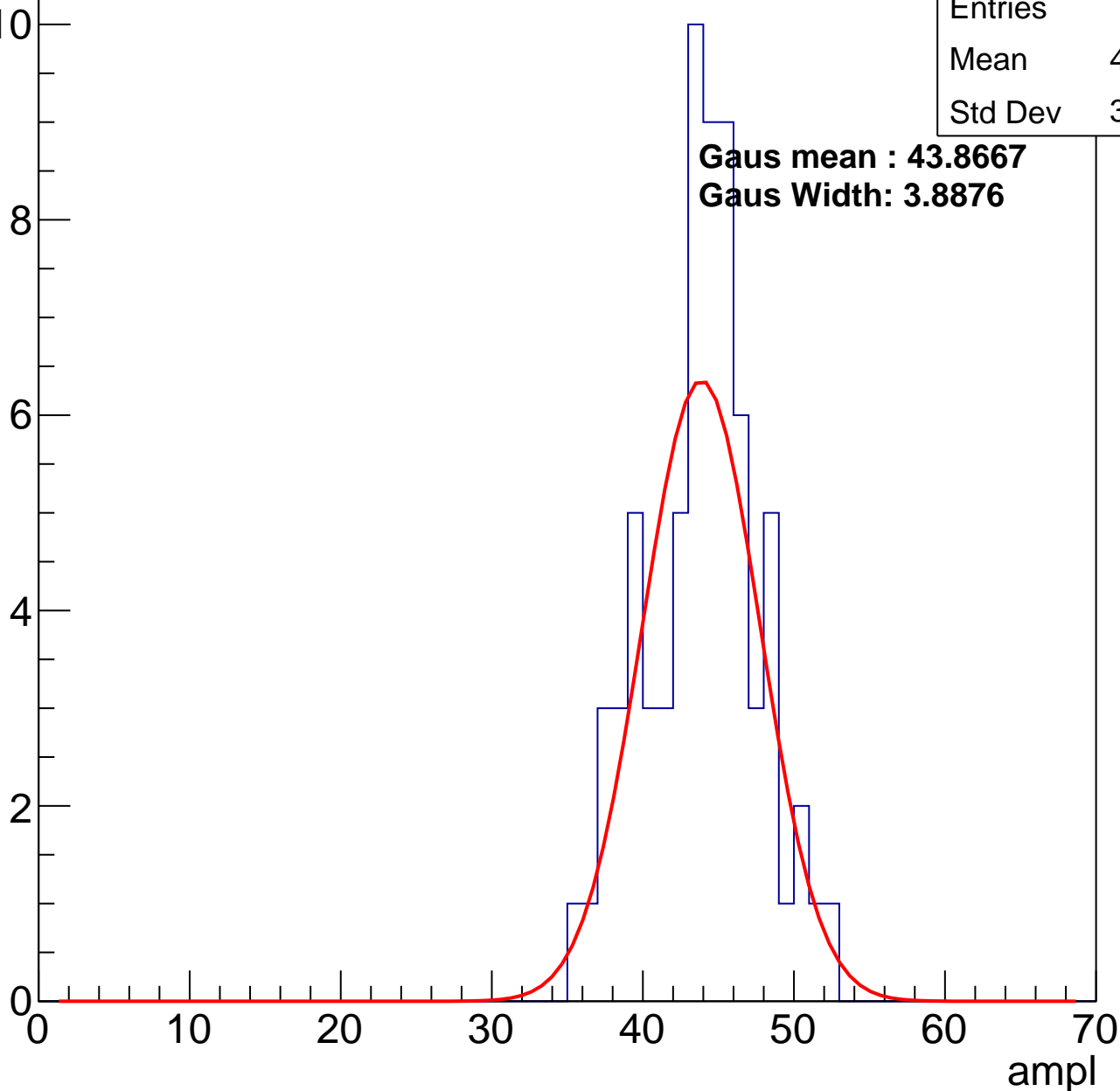
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	71
Mean	43.44
Std Dev	3.672

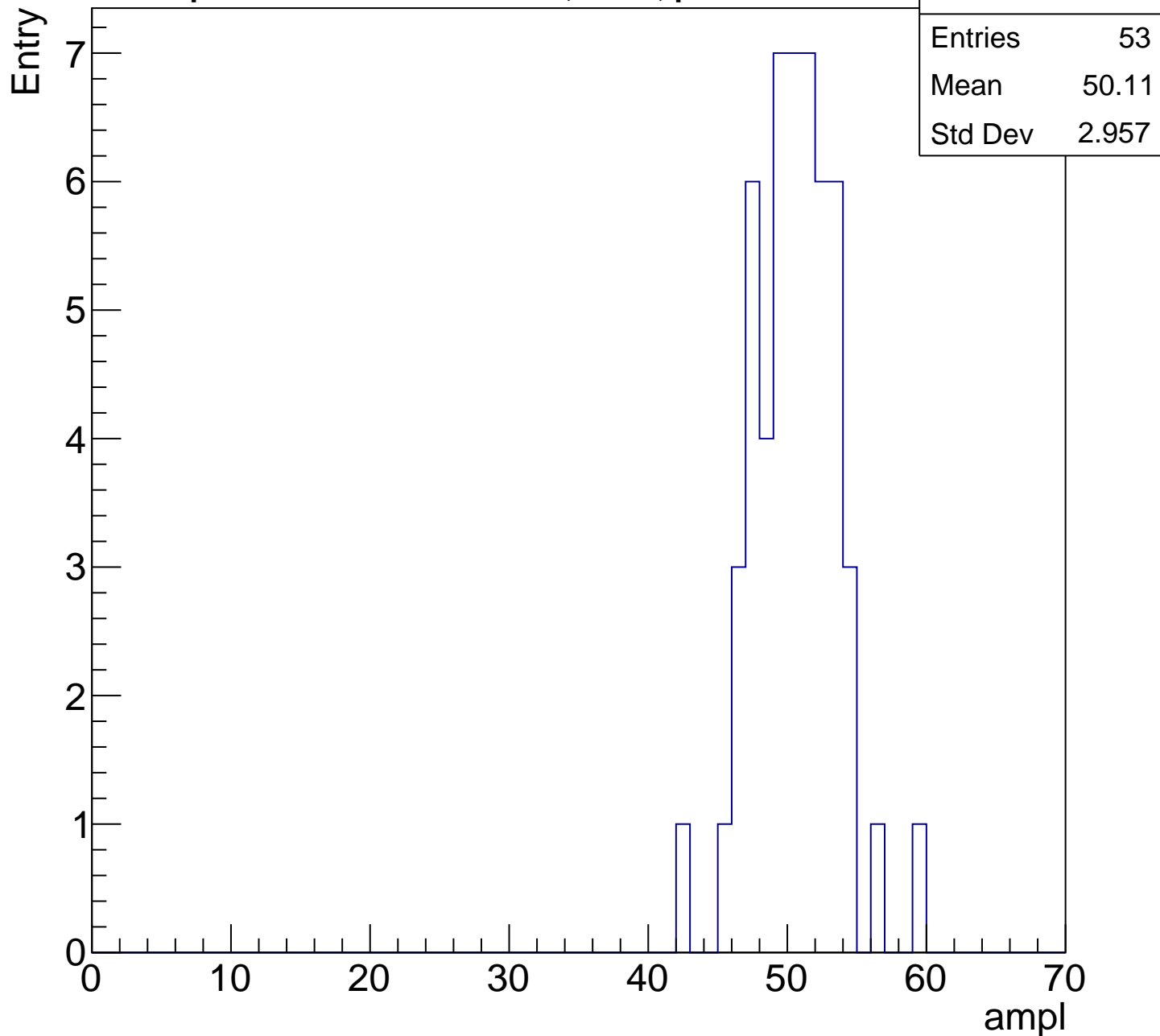
**Gaus mean : 43.8667**

**Gaus Width: 3.8876**



# B1L101S, U20-ch1, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U20-ch1, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	65
Mean	55.83
Std Dev	3.358

Entry

10

8

6

4

2

0

0

10

20

30

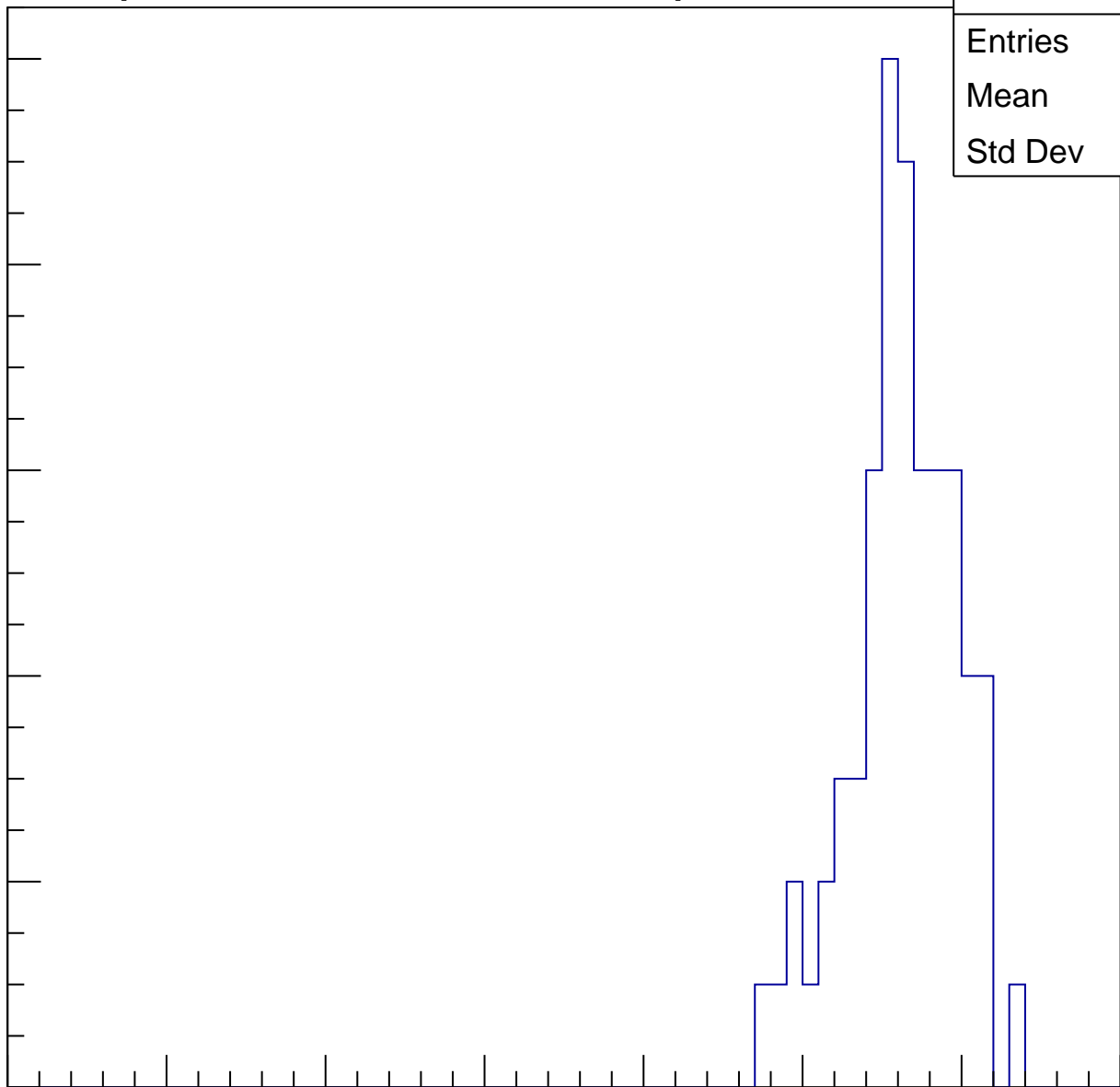
40

50

60

70

ampl

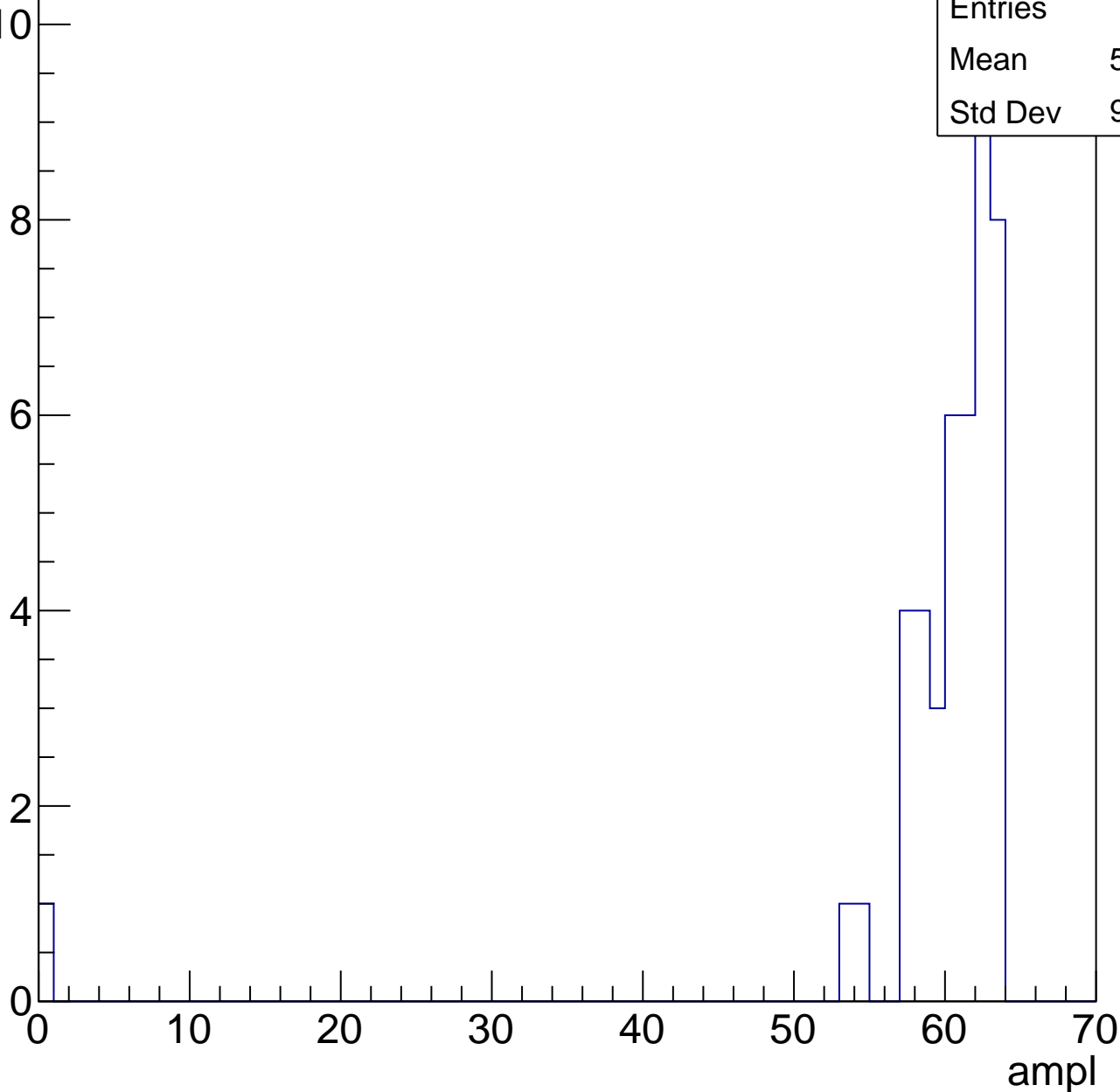


# B1L101S, U20-ch1, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	44
Mean	58.95
Std Dev	9.305



# B1L101S, U20-ch1, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U20-ch1, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U20-ch2, adc0

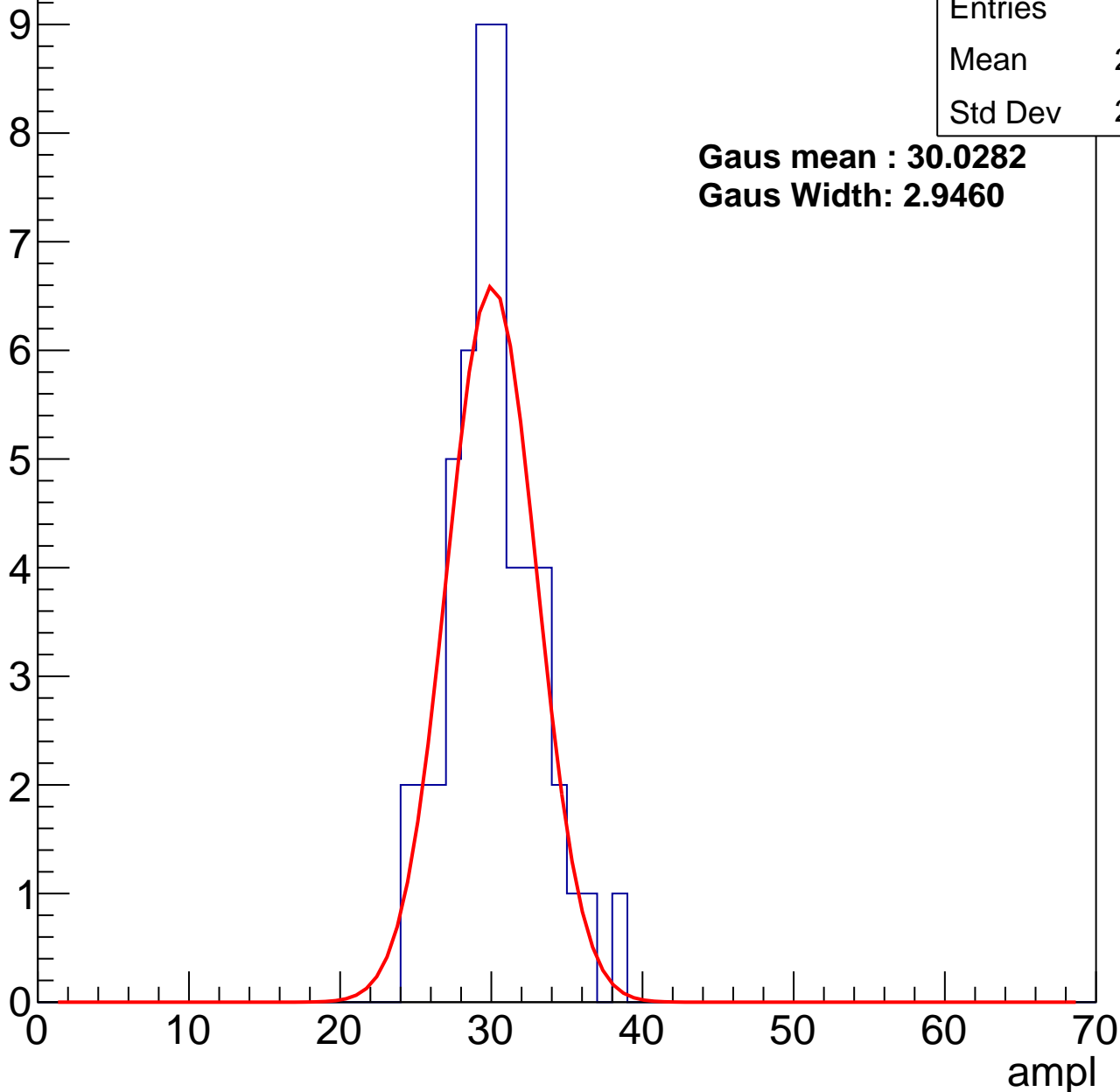
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	52
Mean	29.71
Std Dev	2.911

**Gaus mean : 30.0282**

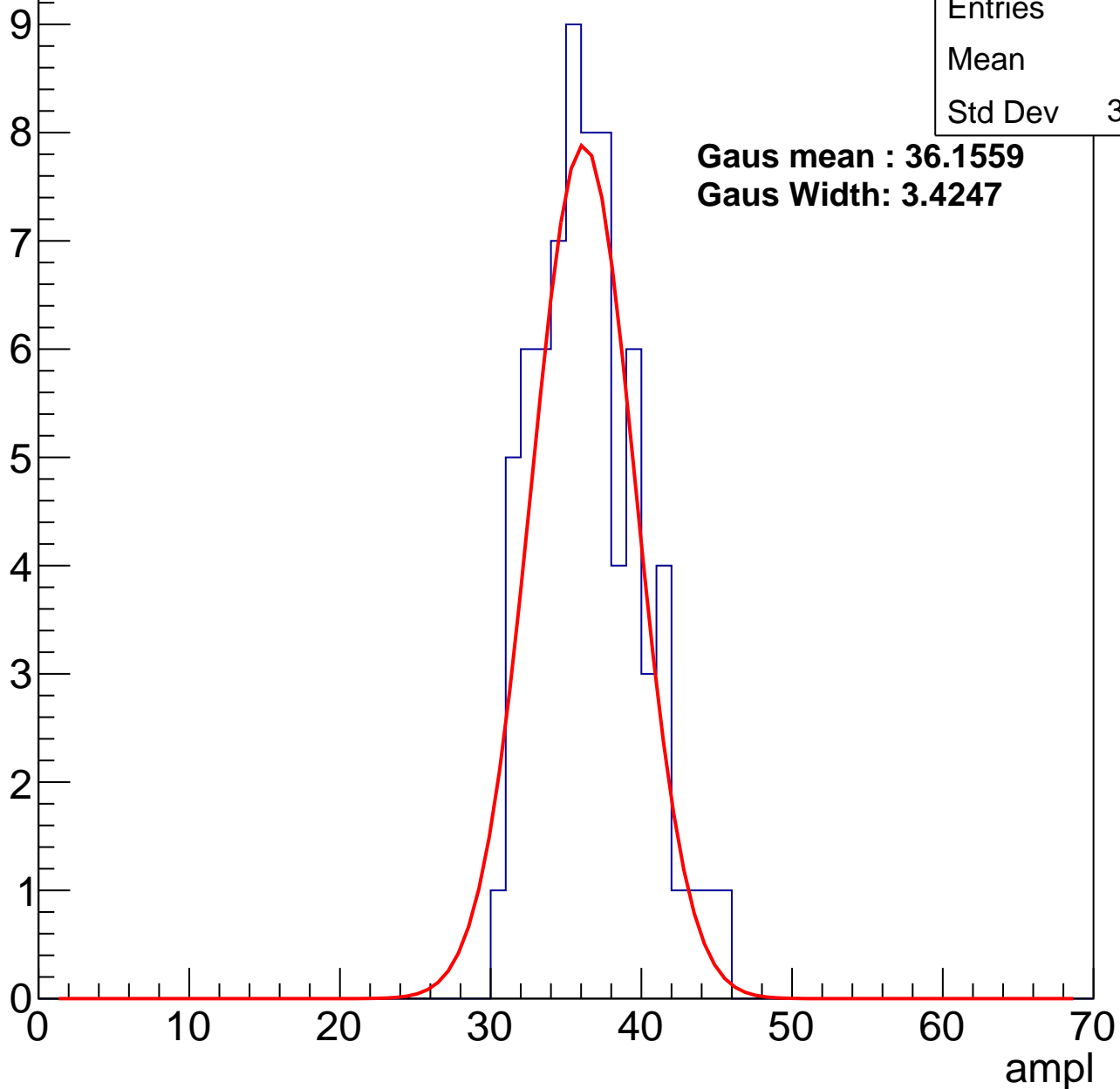
**Gaus Width: 2.9460**



# B1L101S, U20-ch2, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	71
Mean	36
Std Dev	3.365

# B1L101S, U20-ch2, adc2

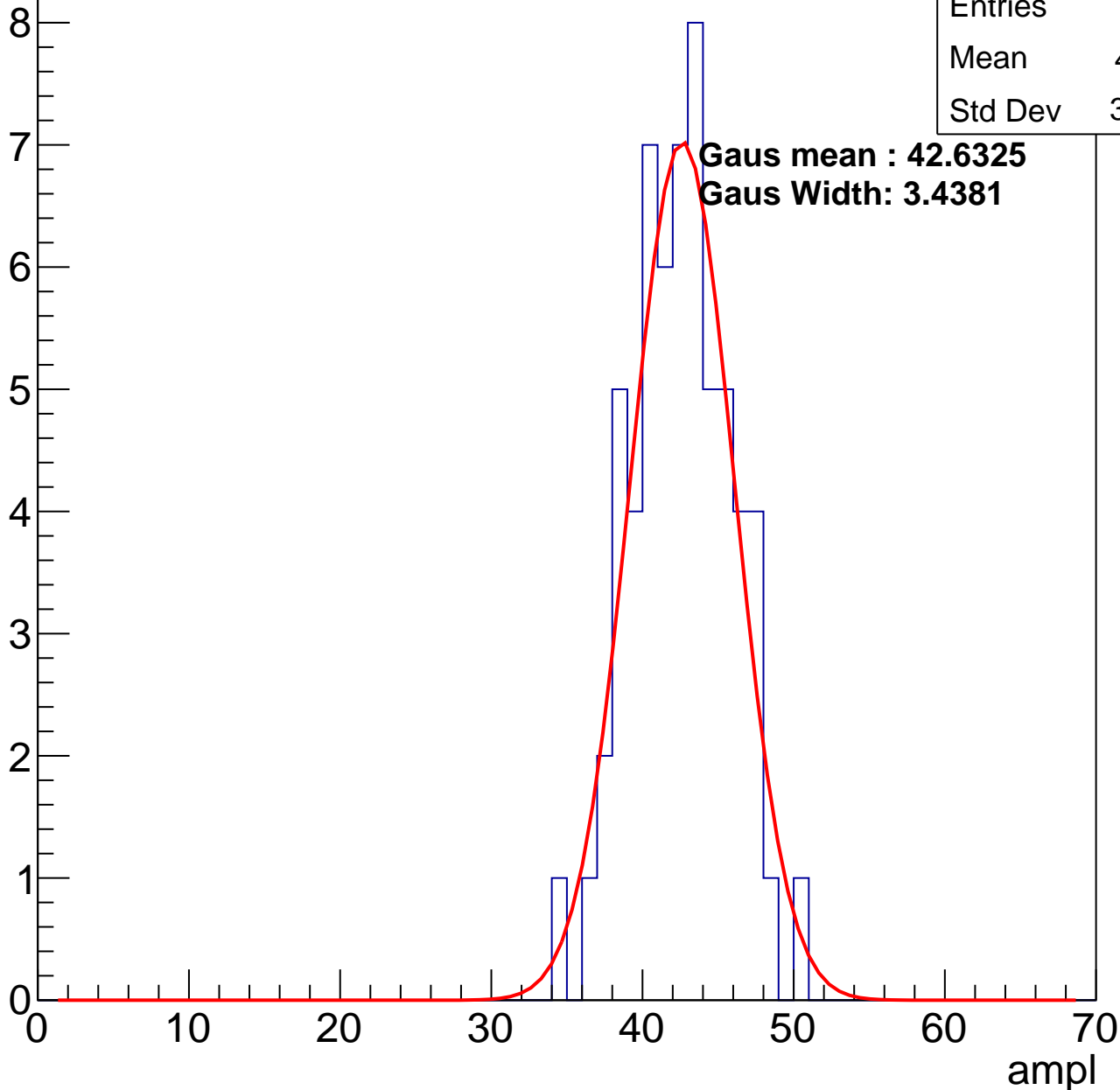
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	42.11
Std Dev	3.229

**Gaus mean : 42.6325**

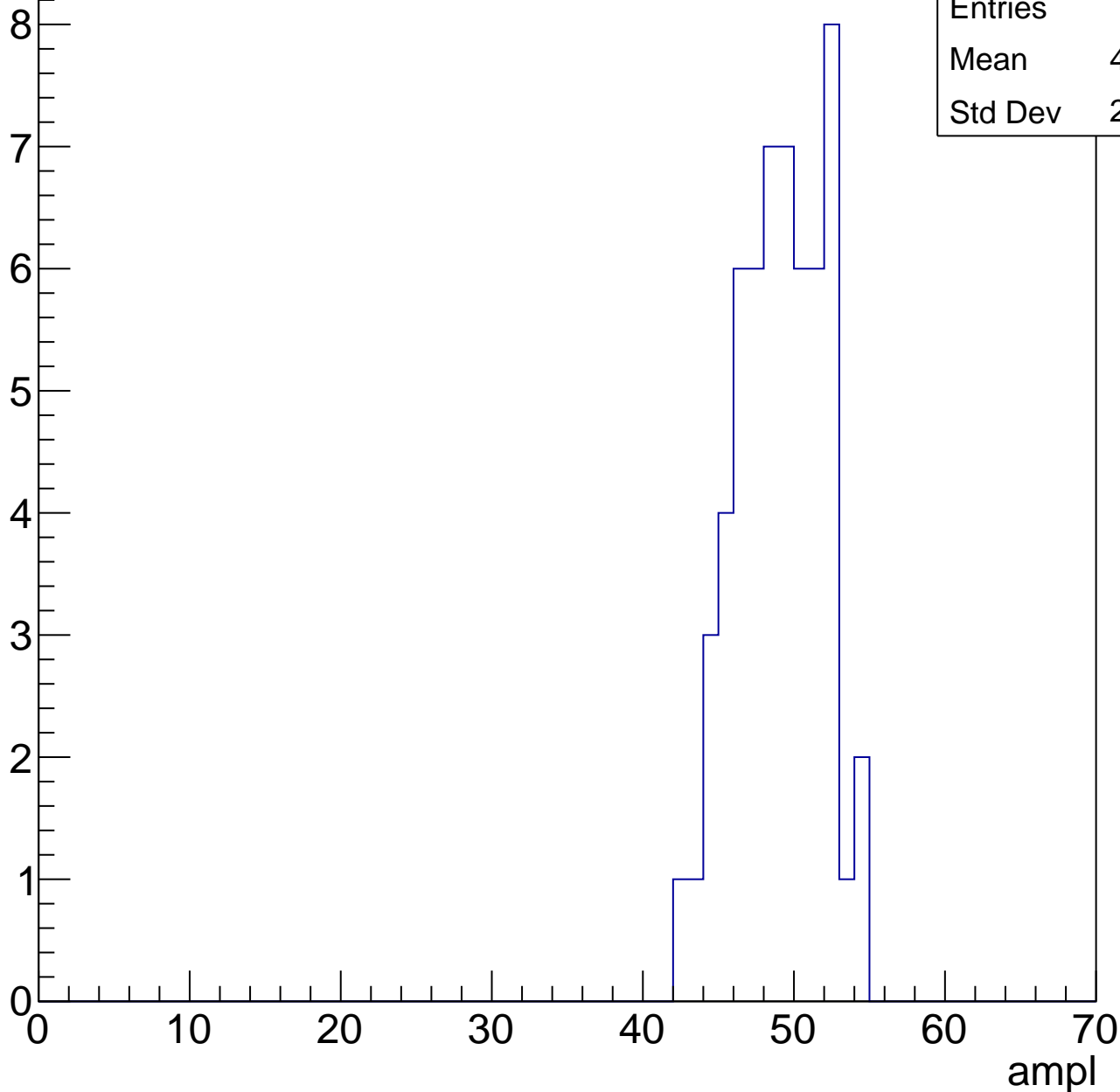
**Gaus Width: 3.4381**



# B1L101S, U20-ch2, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

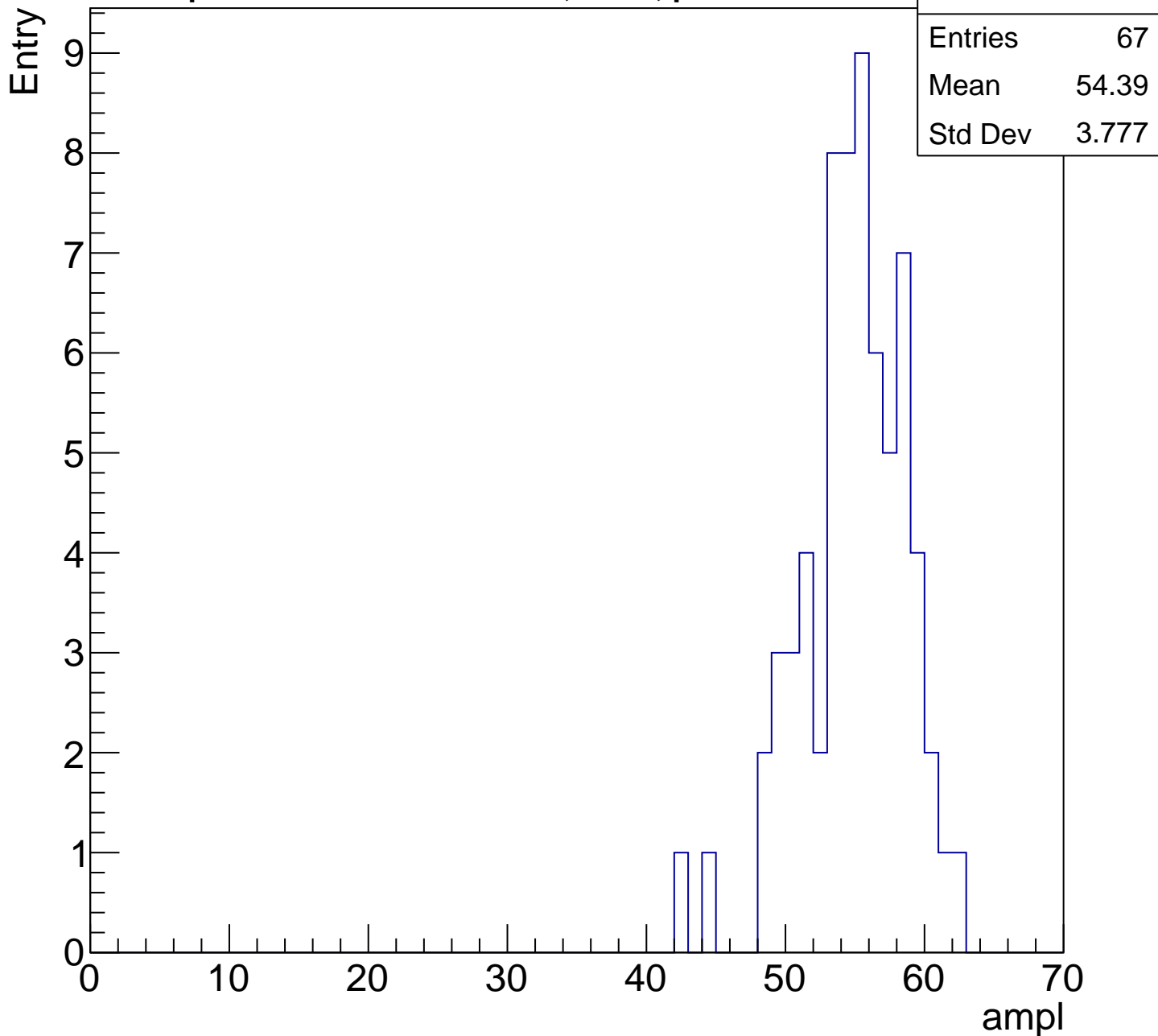
Entry



Entries	58
Mean	48.57
Std Dev	2.835

# B1L101S, U20-ch2, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U20-ch2, adc5

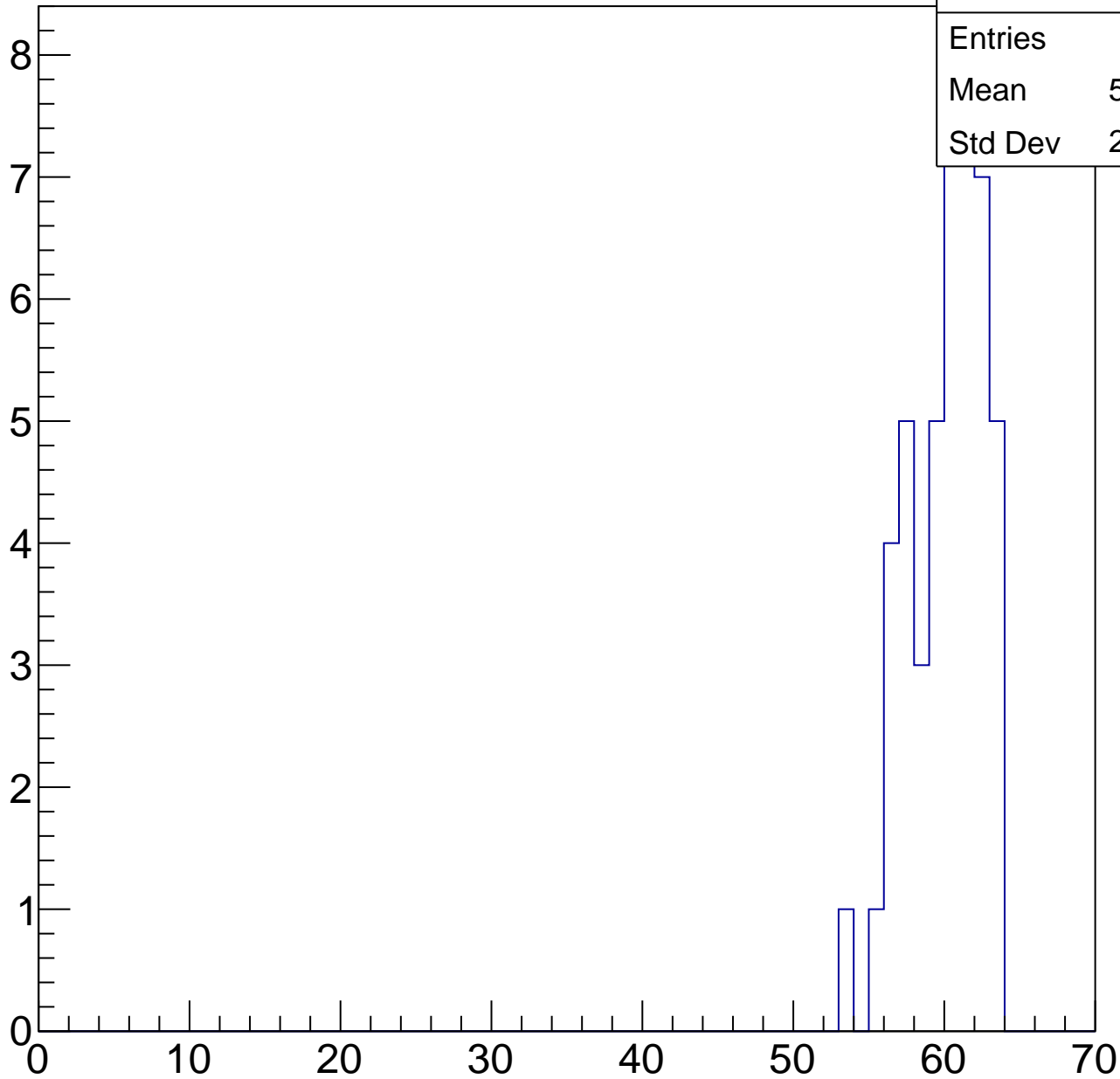
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	47
Mean	59.64
Std Dev	2.418

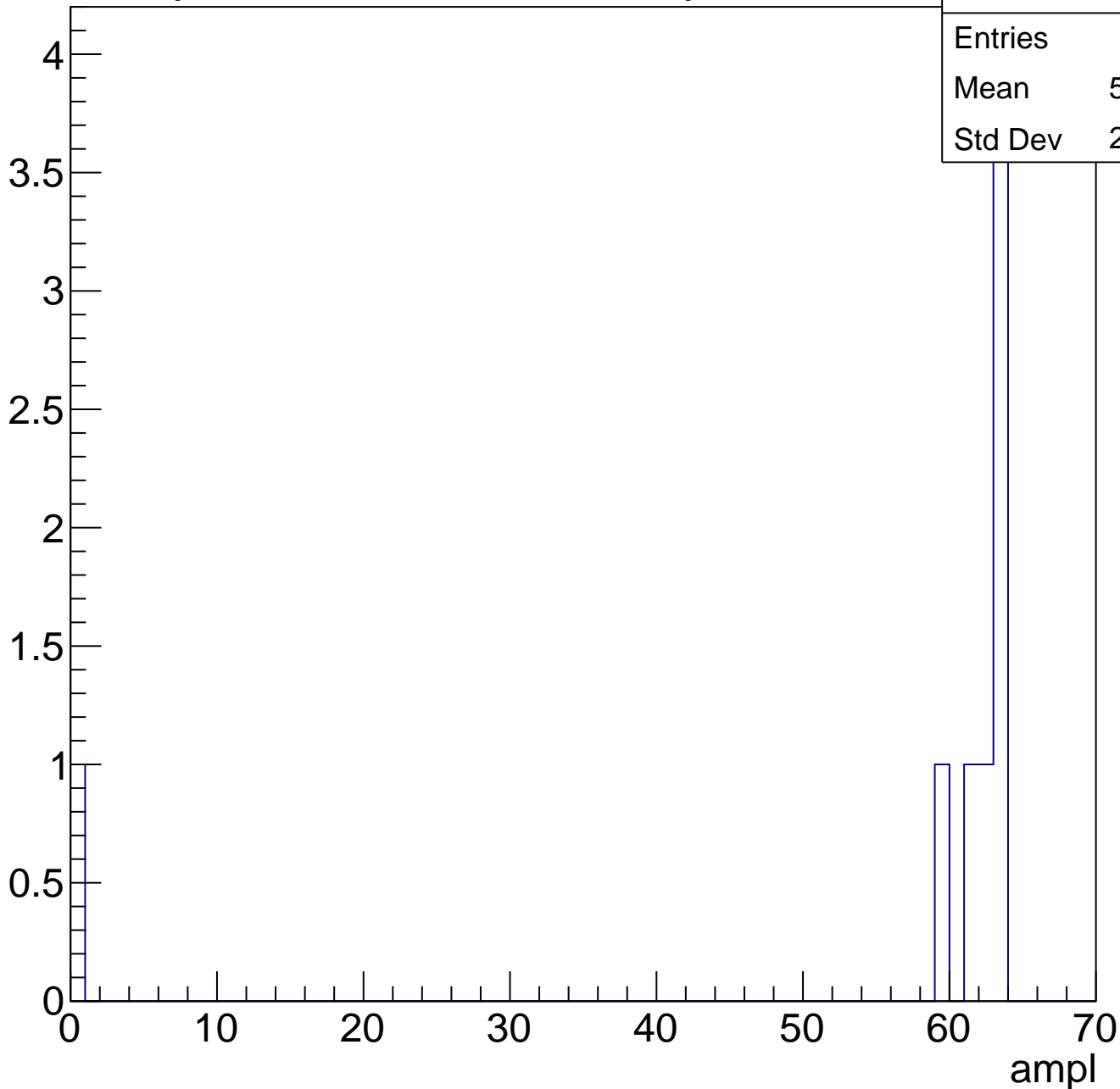
ampl



# B1L101S, U20-ch2, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U20-ch2, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

1  
0.8  
0.6  
0.4  
0.2  
0

Entries	3
Mean	49
Std Dev	19.1

ampl

# B1L101S, U20-ch3, adc0

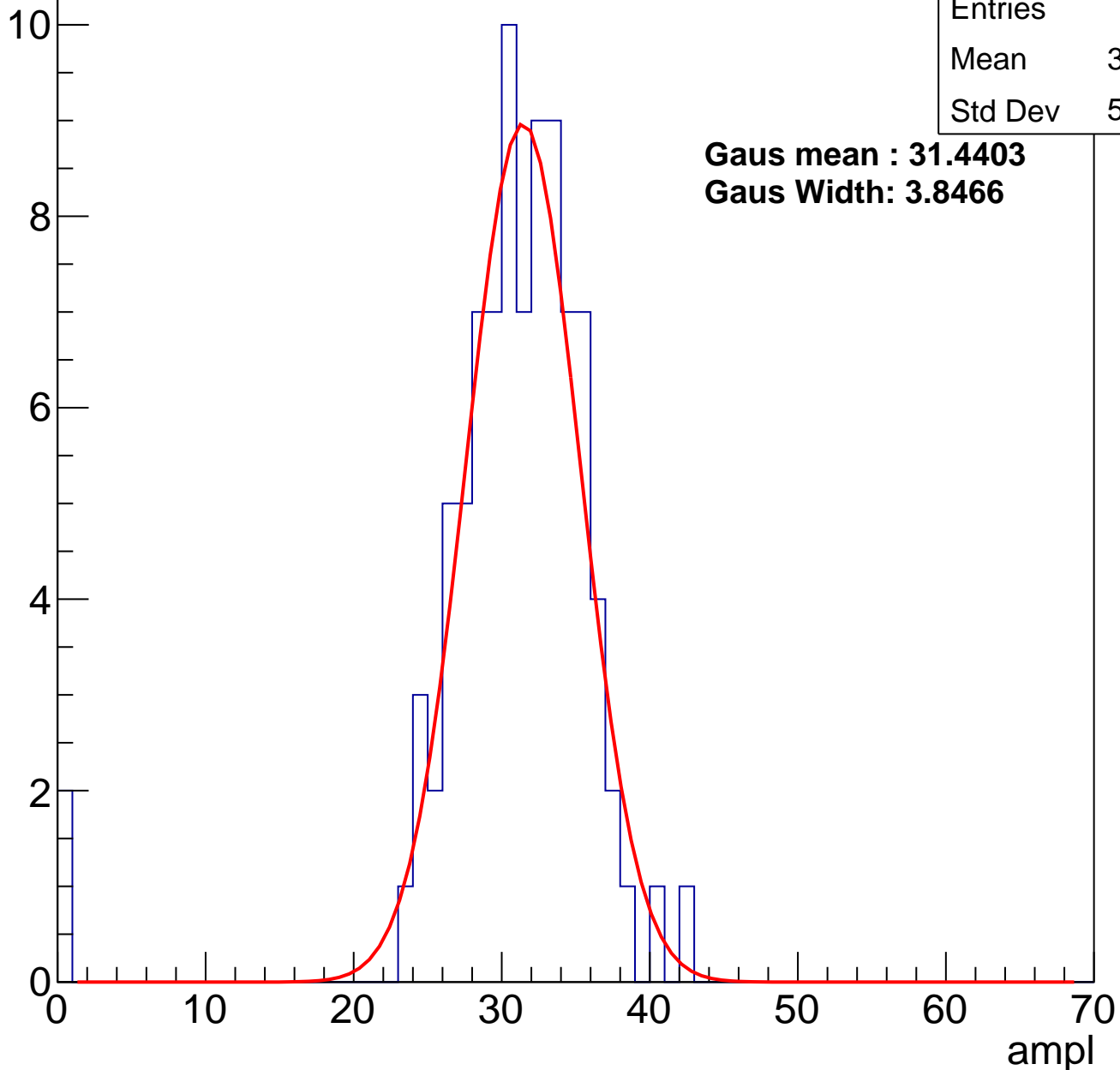
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	90
Mean	30.36
Std Dev	5.885

**Gaus mean : 31.4403**

**Gaus Width: 3.8466**

Entry



# B1L101S, U20-ch3, adc1

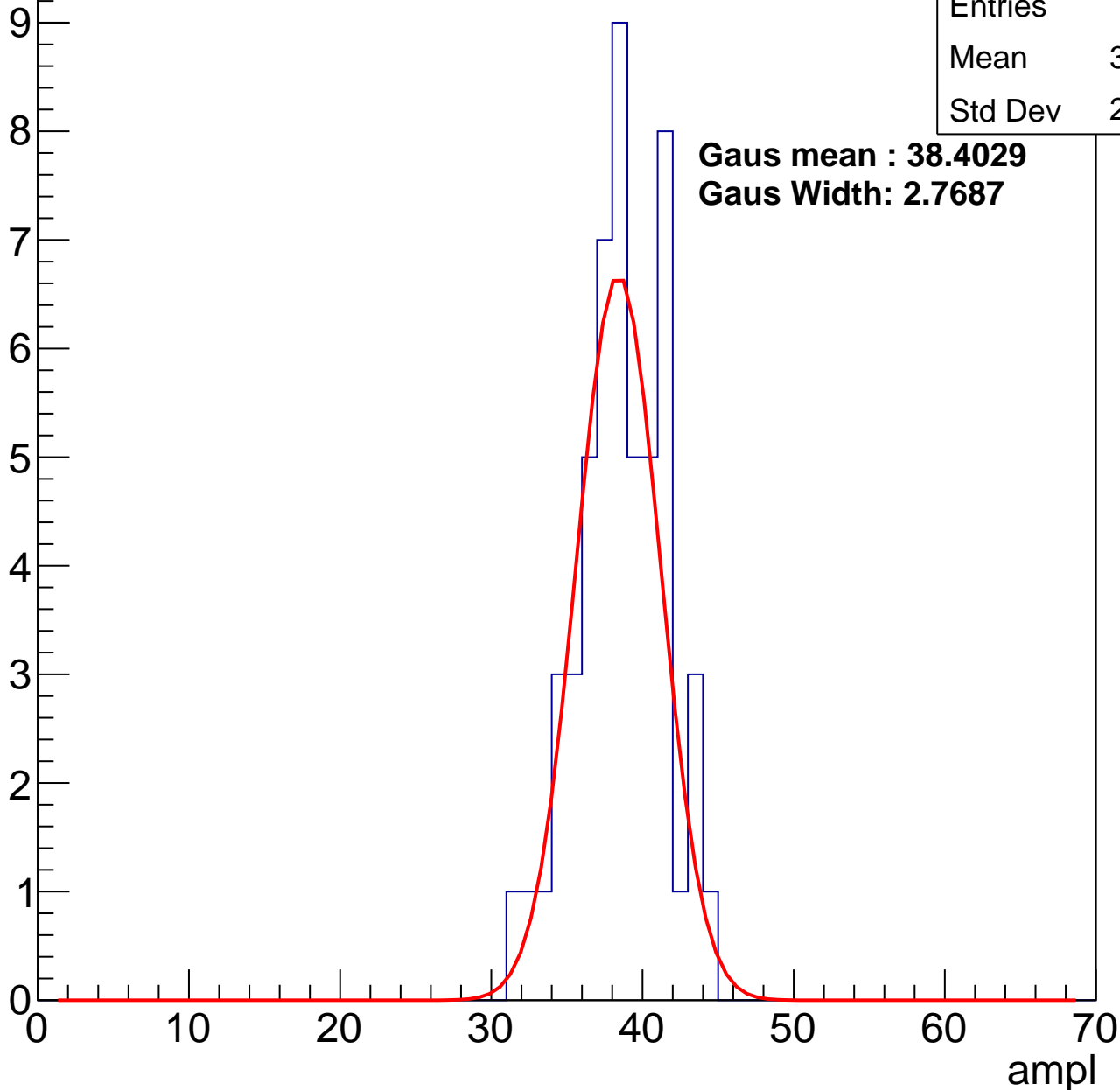
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	53
Mean	38.15
Std Dev	2.864

**Gaus mean : 38.4029**

**Gaus Width: 2.7687**



# B1L101S, U20-ch3, adc2

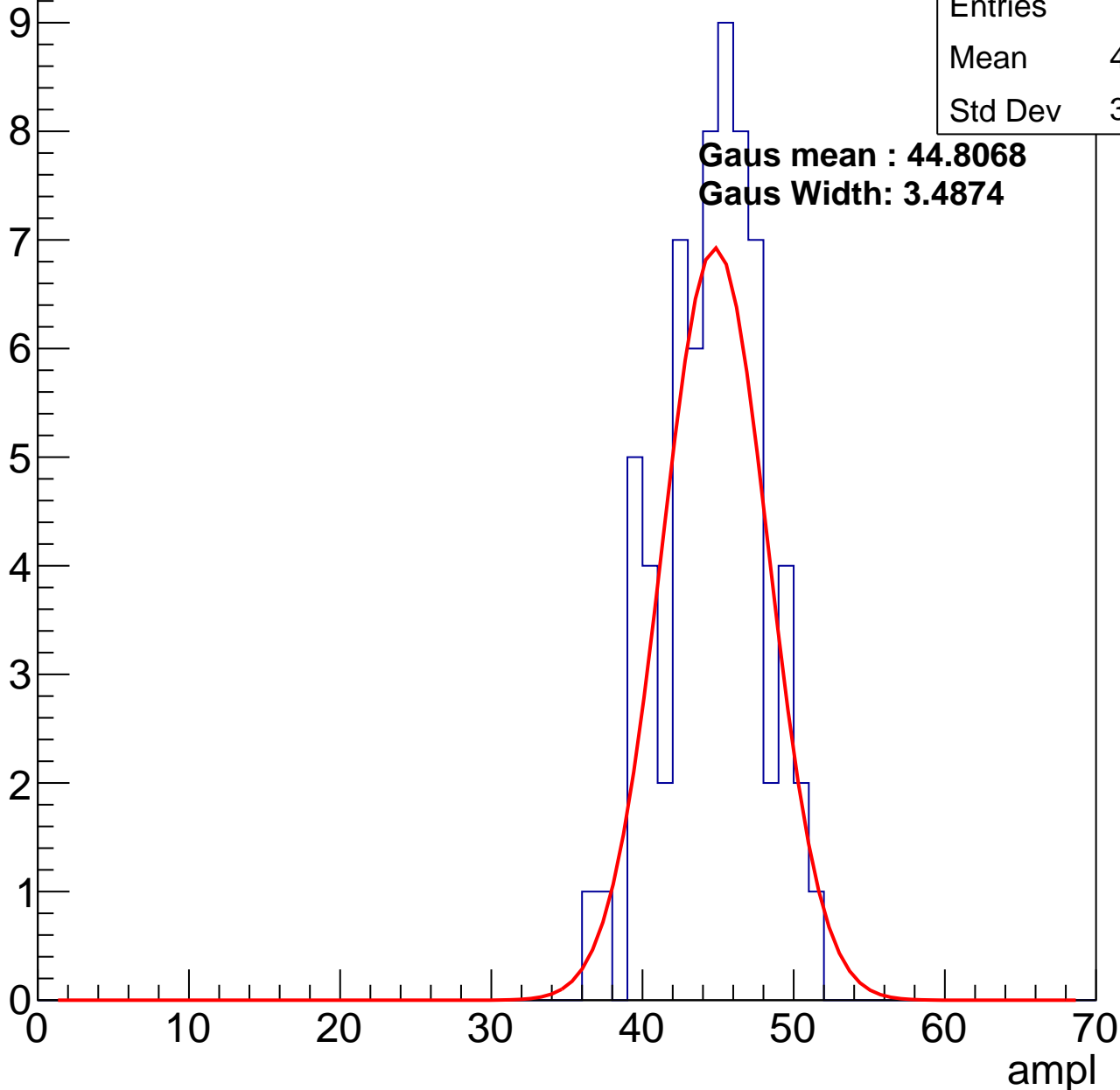
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	67
Mean	44.16
Std Dev	3.253

**Gaus mean : 44.8068**

**Gaus Width: 3.4874**

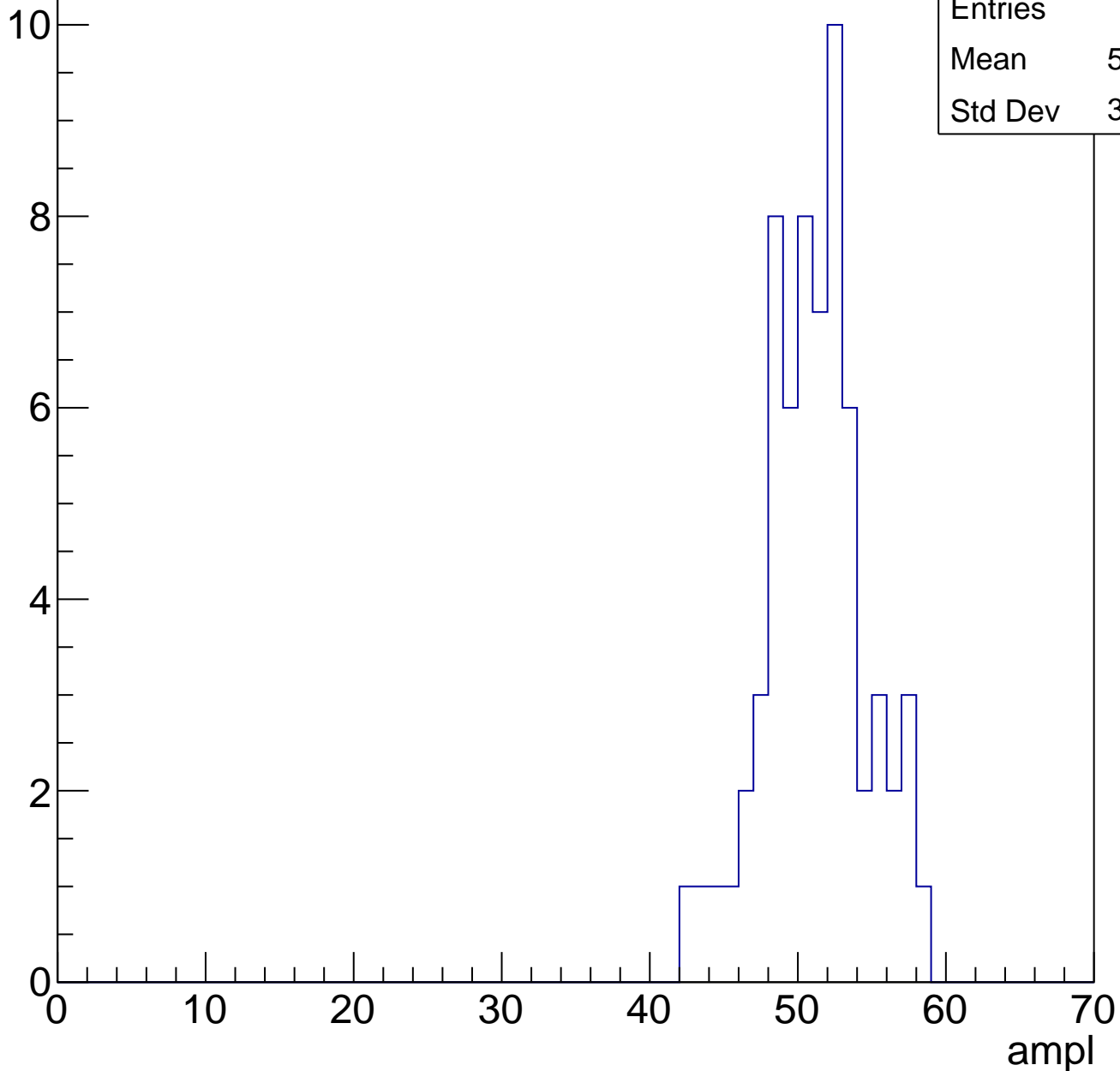


# B1L101S, U20-ch3, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	65
Mean	50.68
Std Dev	3.356

Entry

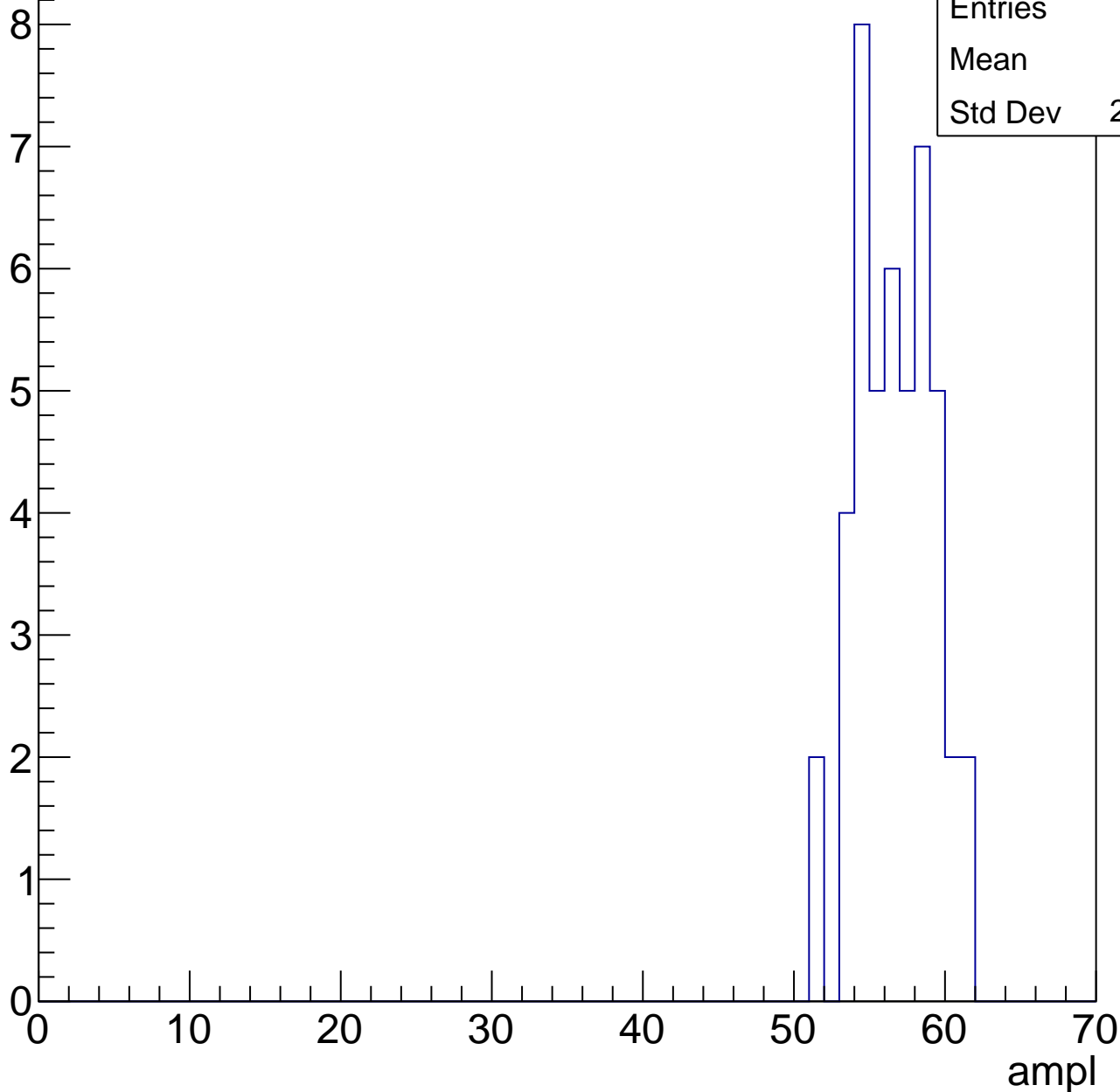


# B1L101S, U20-ch3, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	46
Mean	56.2
Std Dev	2.473

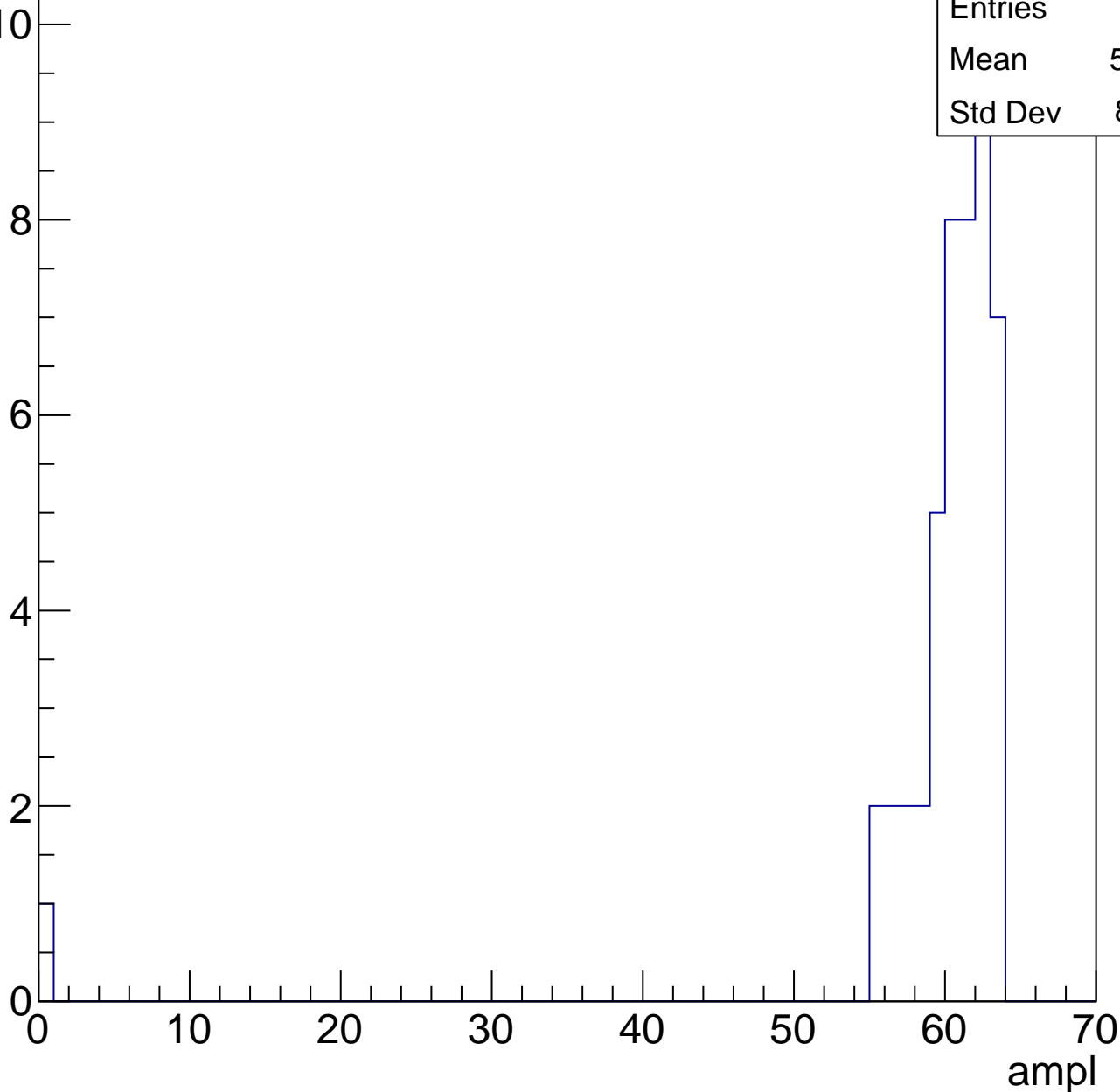


# B1L101S, U20-ch3, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	47
Mean	59.06
Std Dev	8.971



# B1L101S, U20-ch3, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U20-ch3, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L101S, U20-ch4, adc0

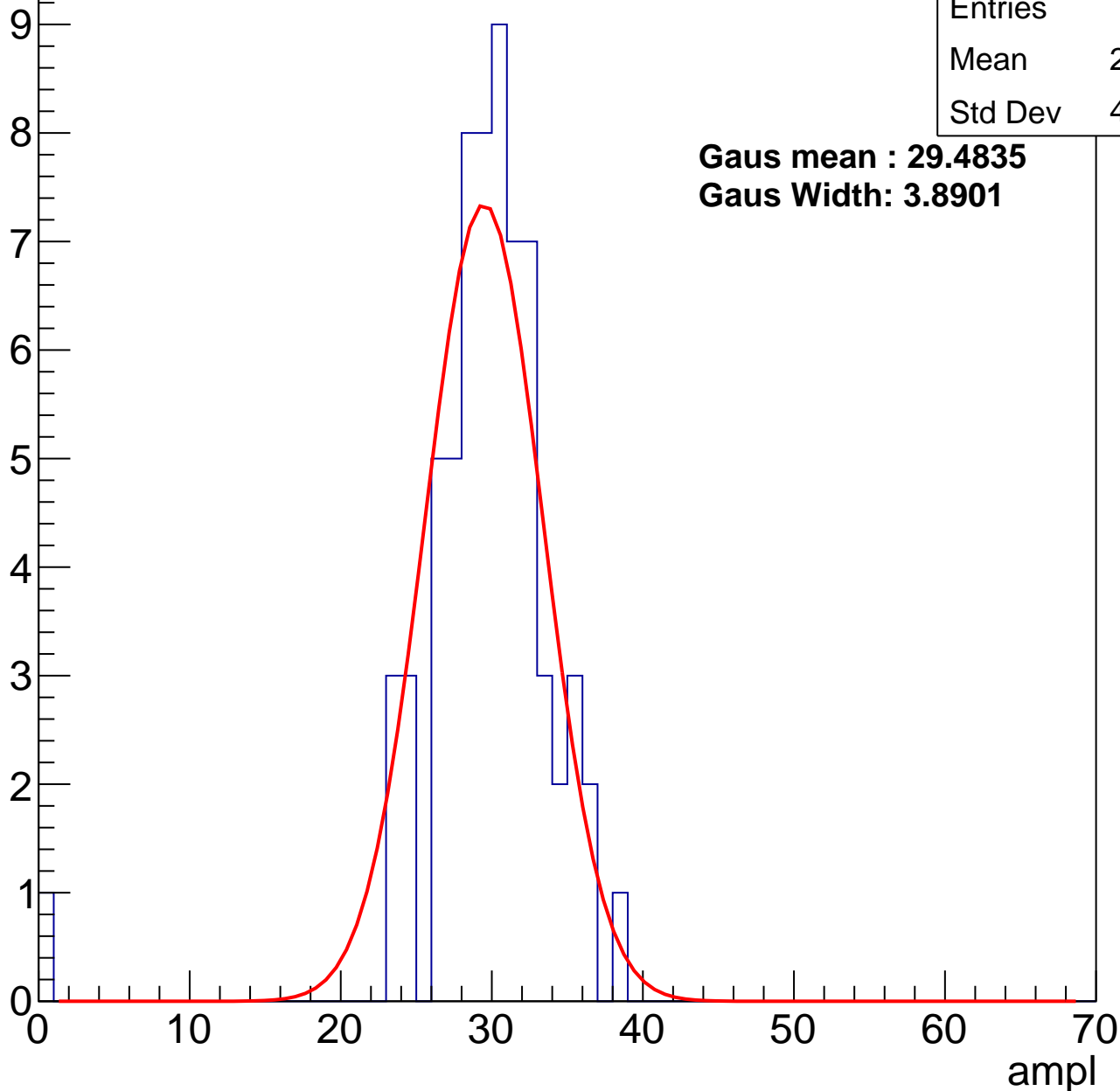
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	67
Mean	29.18
Std Dev	4.856

**Gaus mean : 29.4835**

**Gaus Width: 3.8901**



# B1L101S, U20-ch4, adc1

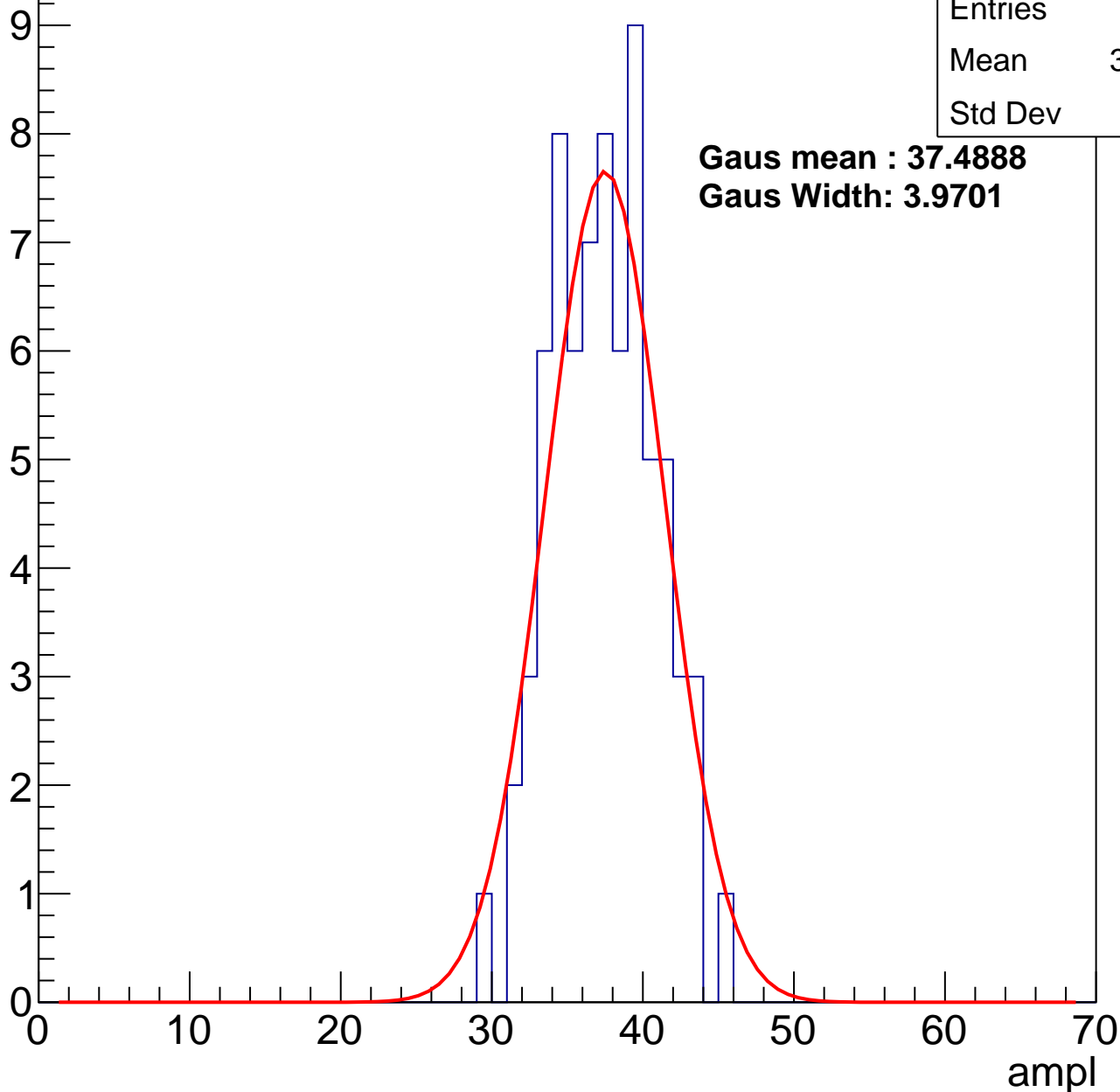
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	73
Mean	36.97
Std Dev	3.36

**Gaus mean : 37.4888**

**Gaus Width: 3.9701**



# B1L101S, U20-ch4, adc2

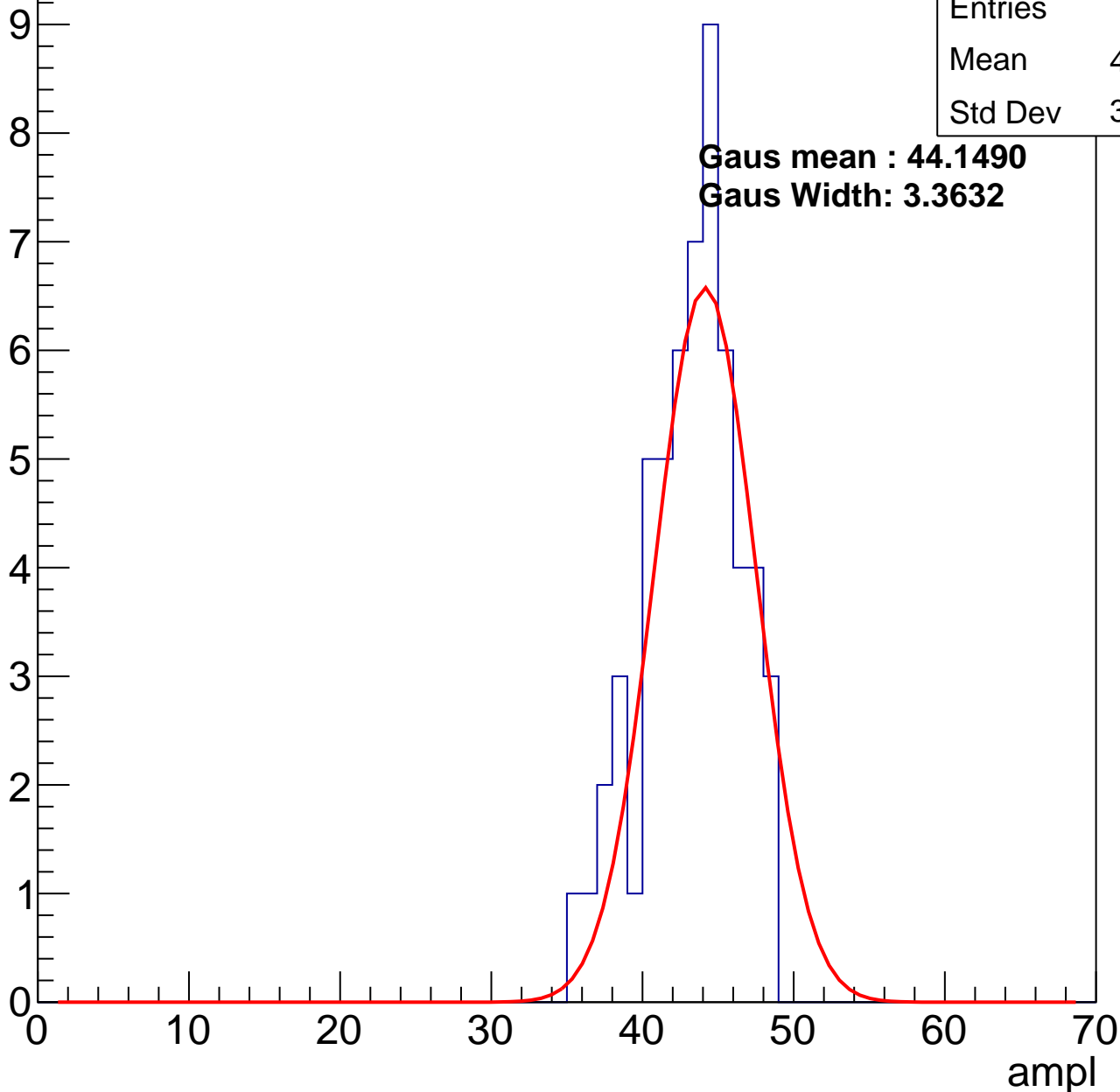
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	57
Mean	42.77
Std Dev	3.112

**Gaus mean : 44.1490**

**Gaus Width: 3.3632**

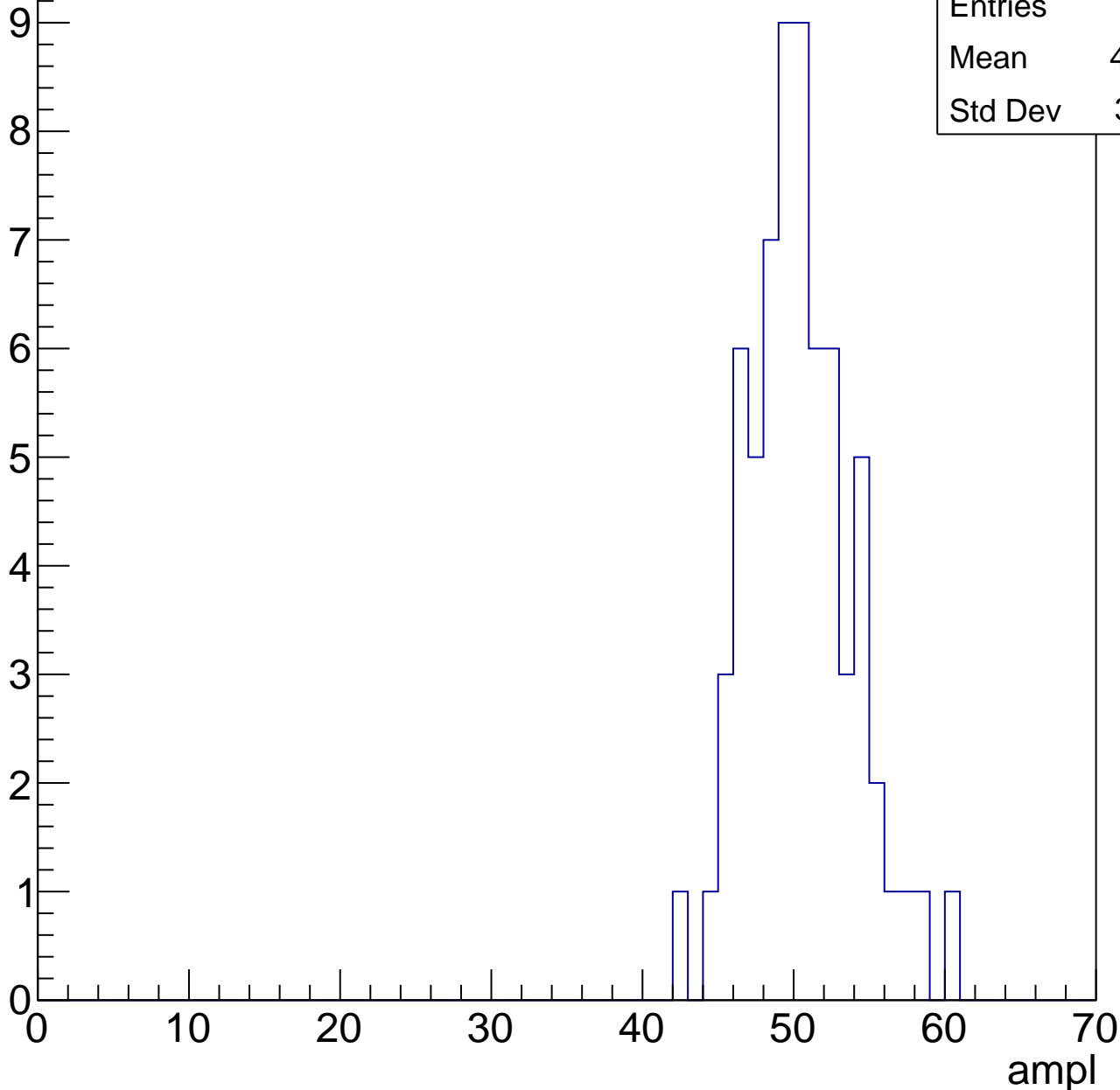


# B1L101S, U20-ch4, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	67
Mean	49.96
Std Dev	3.431

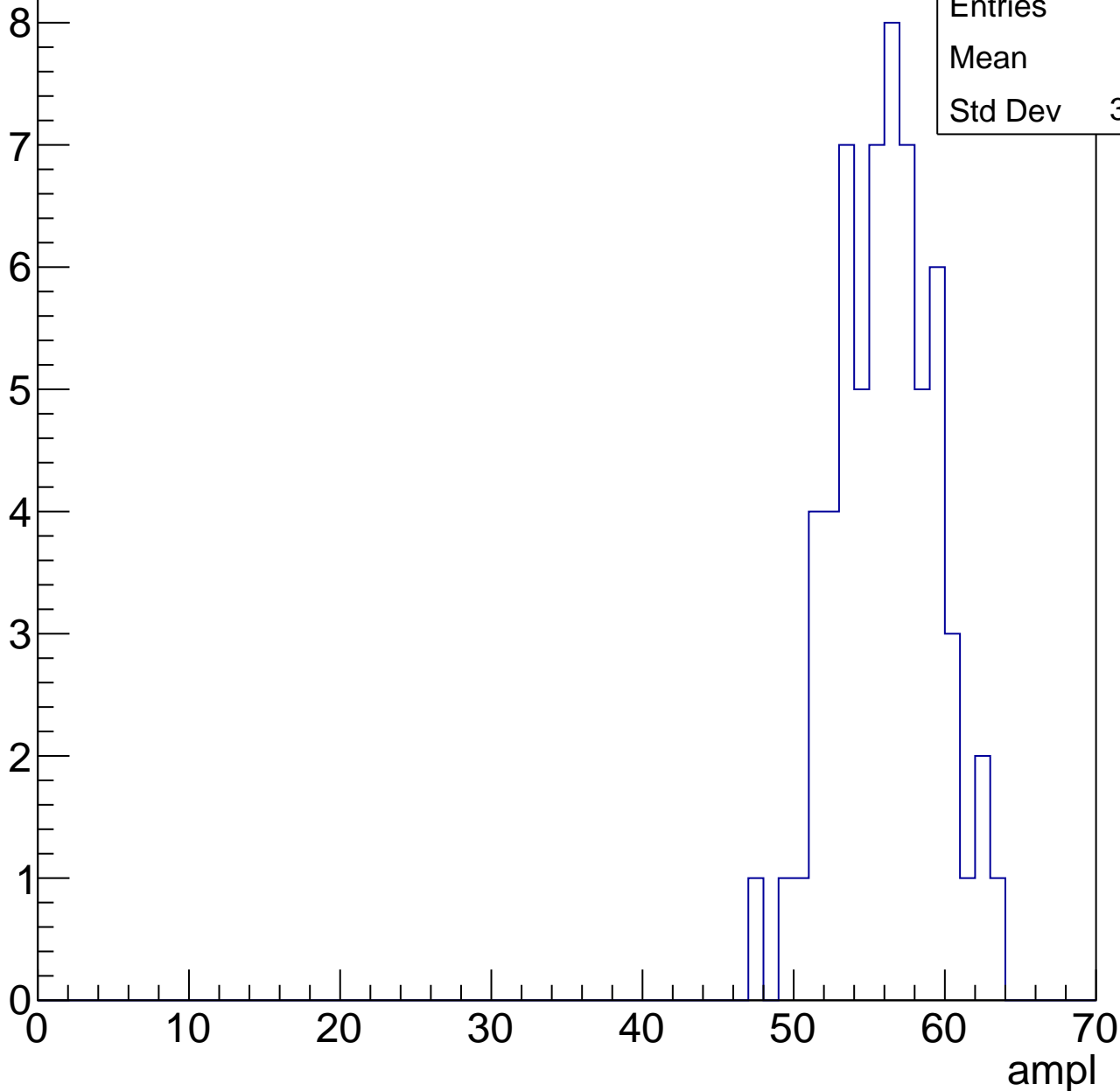


# B1L101S, U20-ch4, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	55.6
Std Dev	3.298

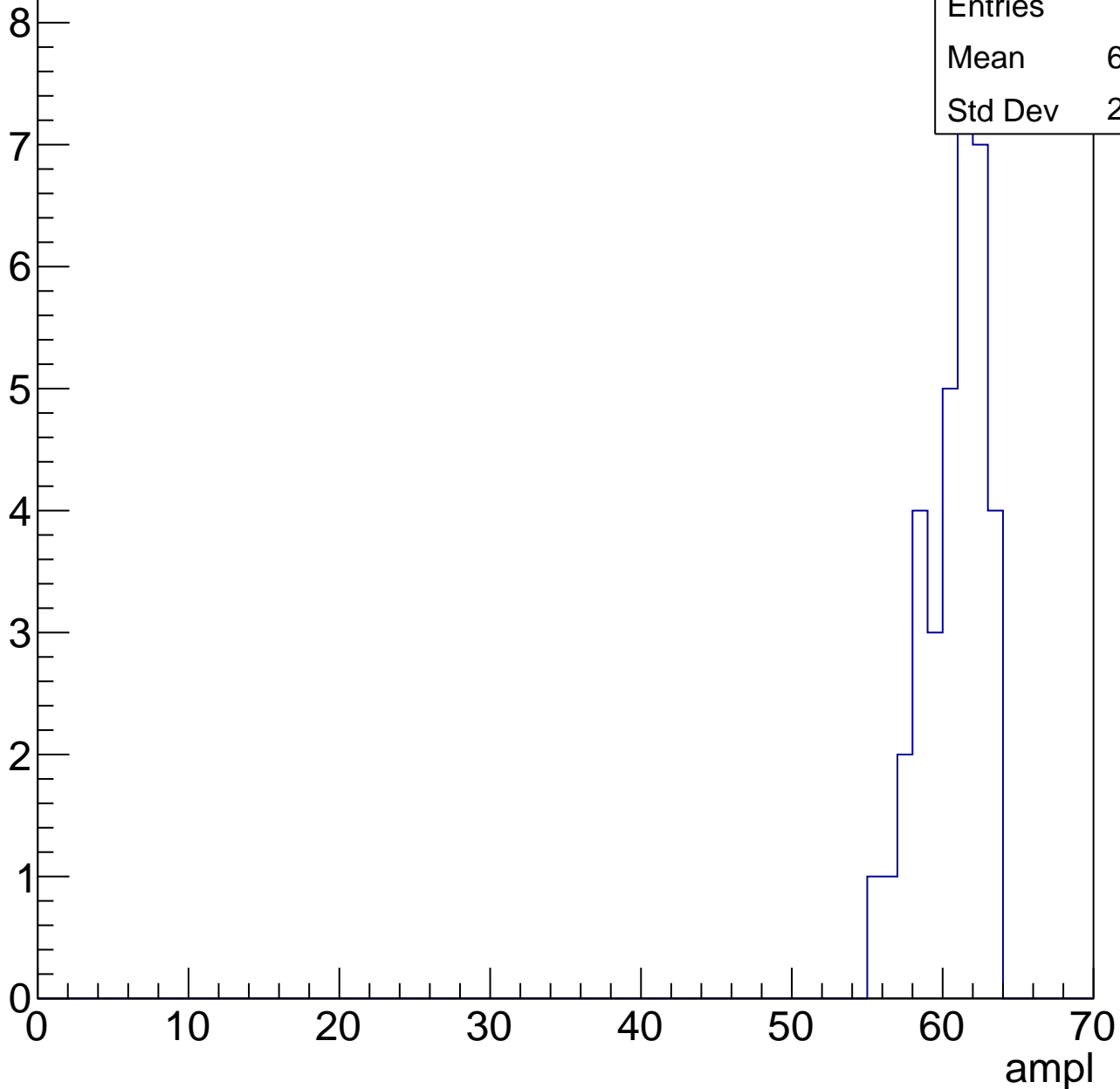


# B1L101S, U20-ch4, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	35
Mean	60.23
Std Dev	2.058

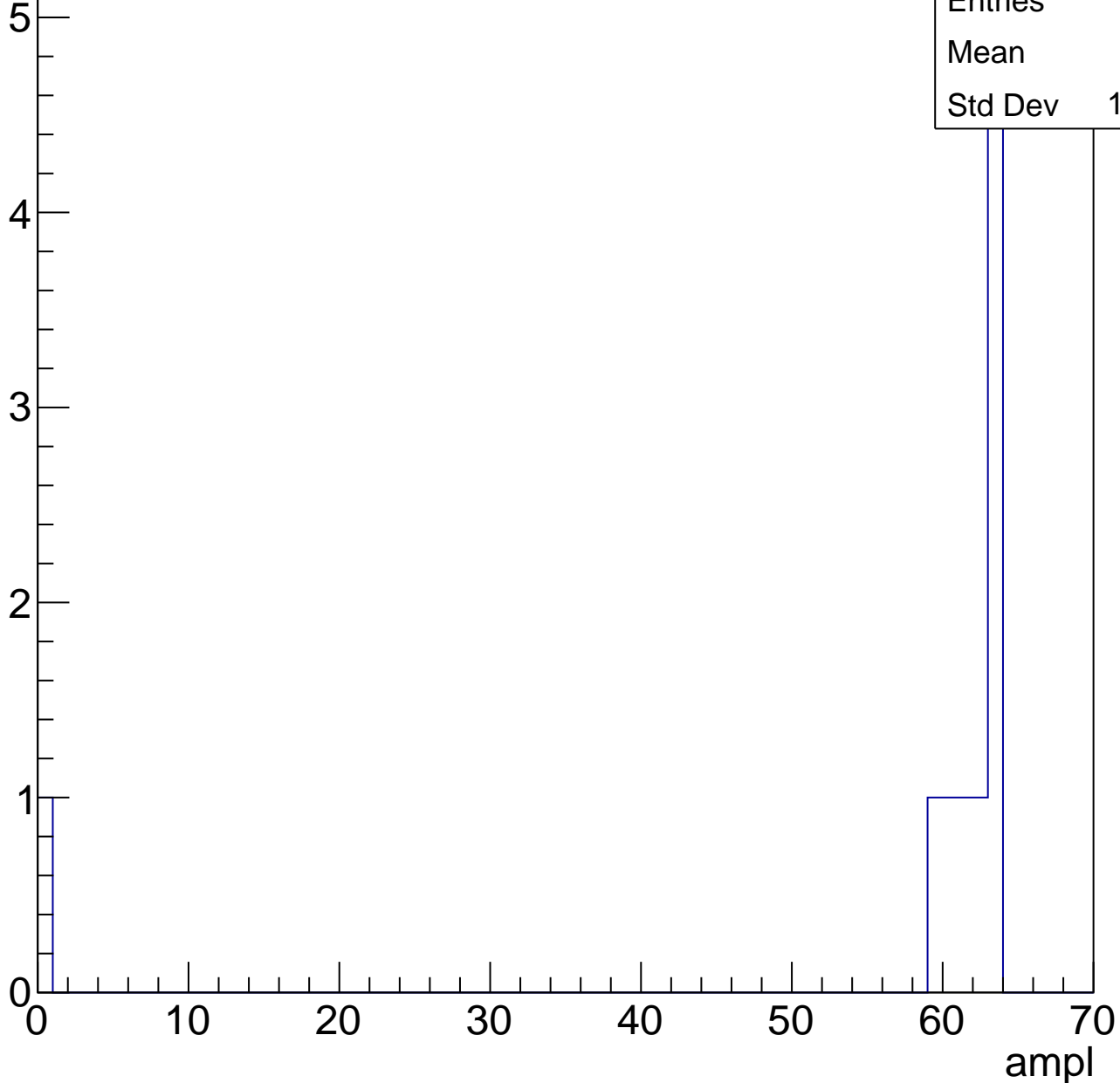


# B1L101S, U20-ch4, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	10
Mean	55.7
Std Dev	18.62





# B1L101S, U20-ch4, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U20-ch5, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	77
Mean	31.43
Std Dev	4.847

**Gaus mean : 31.8218**

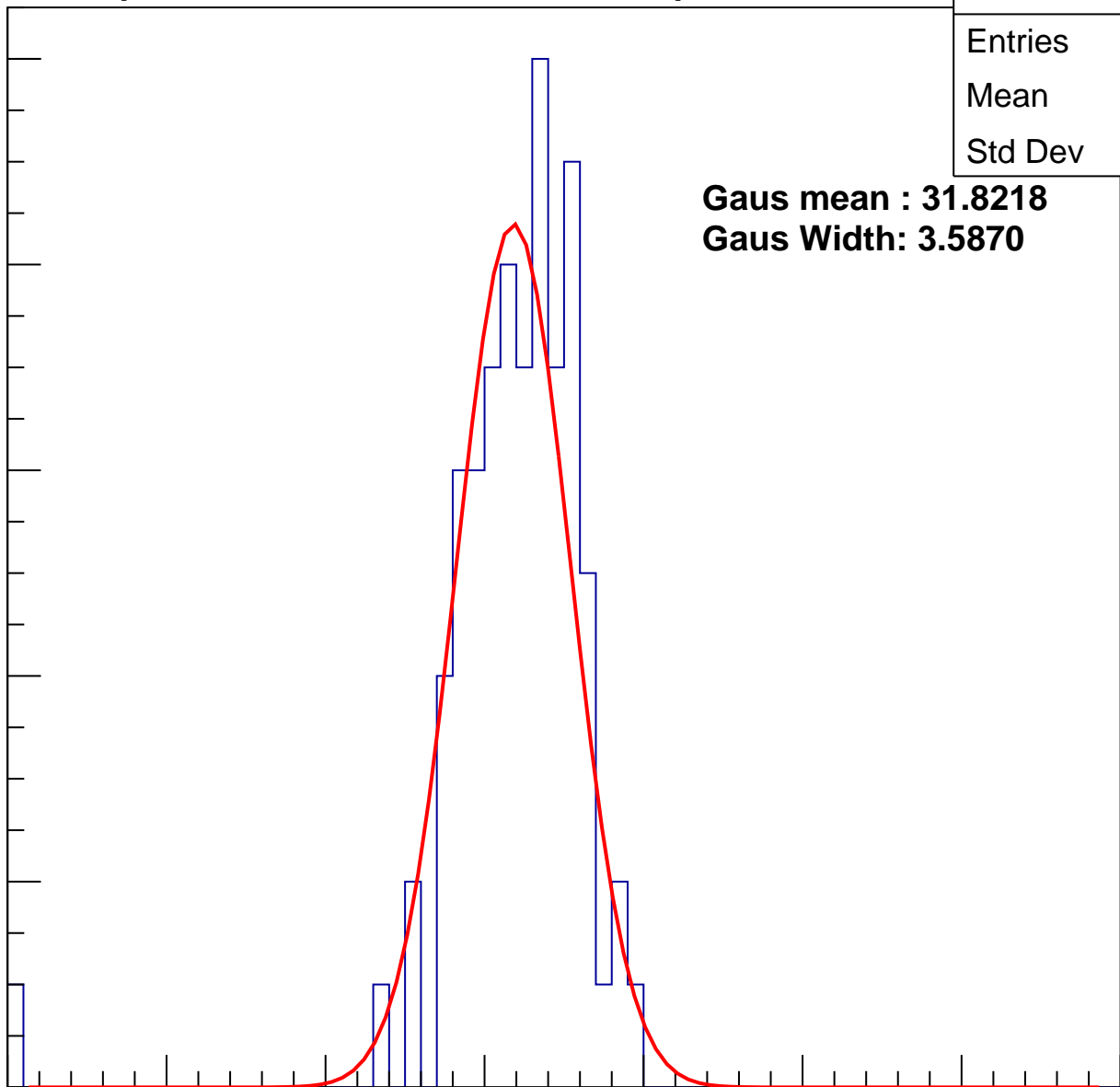
**Gaus Width: 3.5870**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U20-ch5, adc1

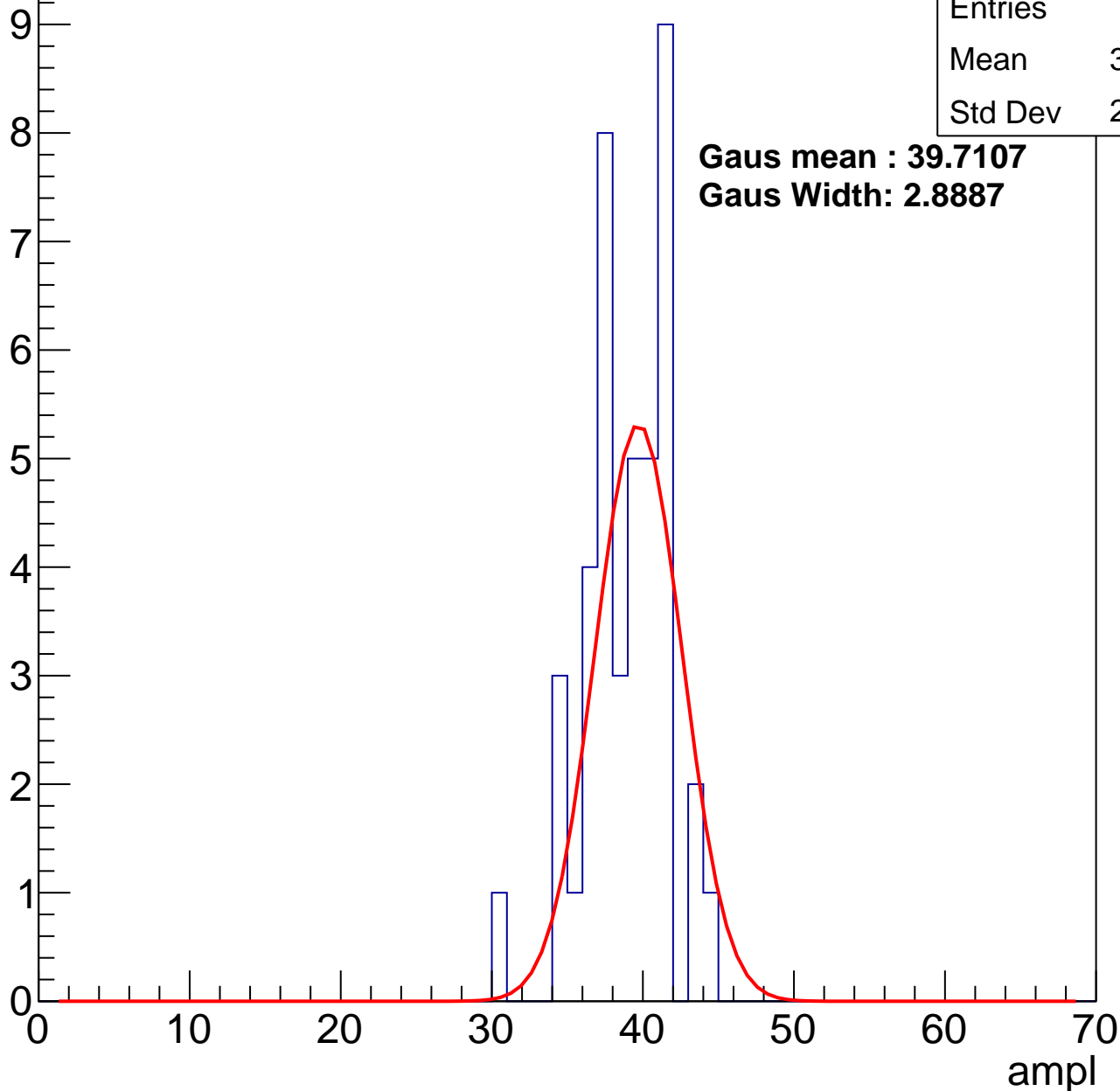
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	42
Mean	38.45
Std Dev	2.796

**Gaus mean : 39.7107**

**Gaus Width: 2.8887**



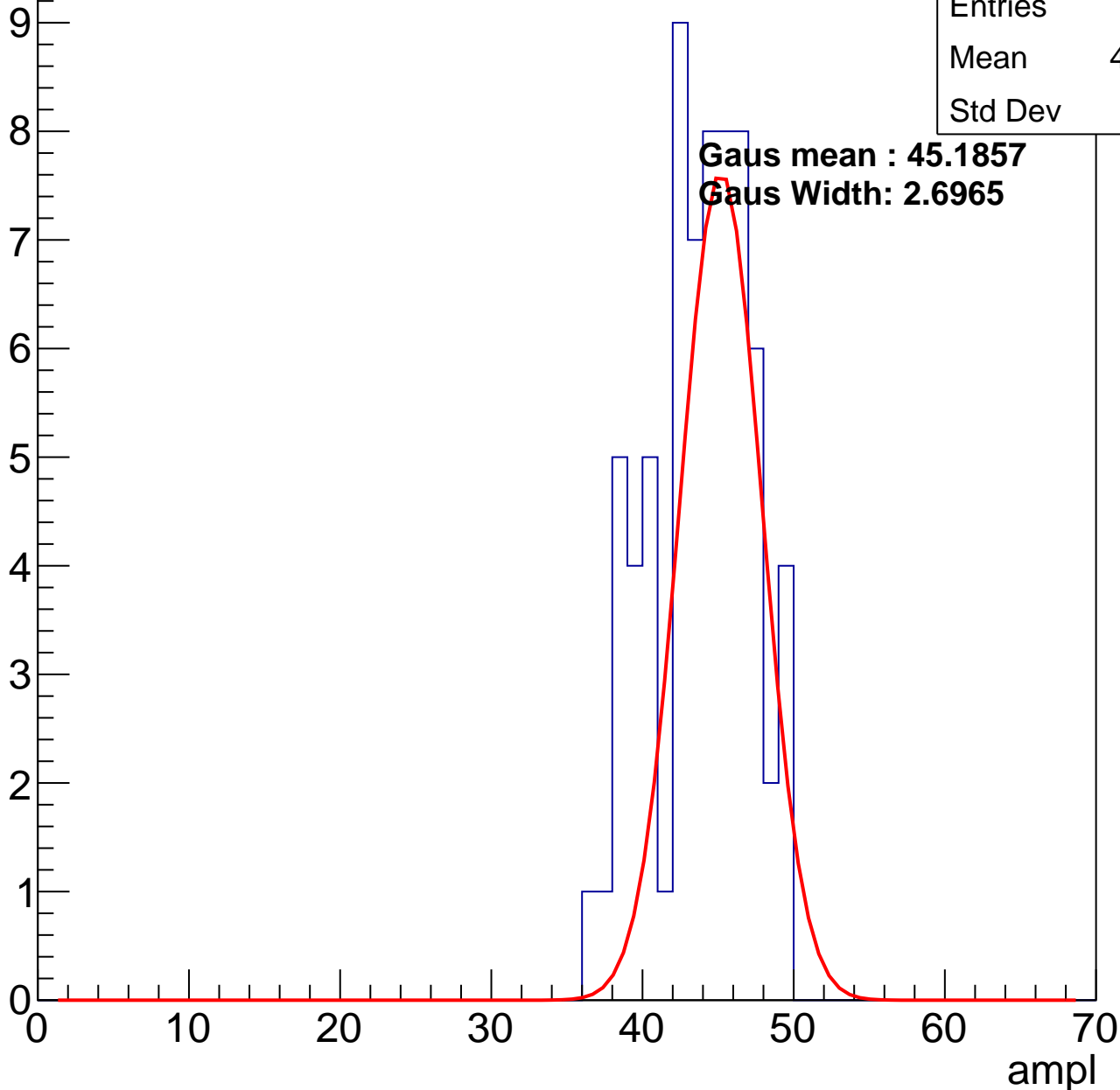
# B1L101S, U20-ch5, adc2

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

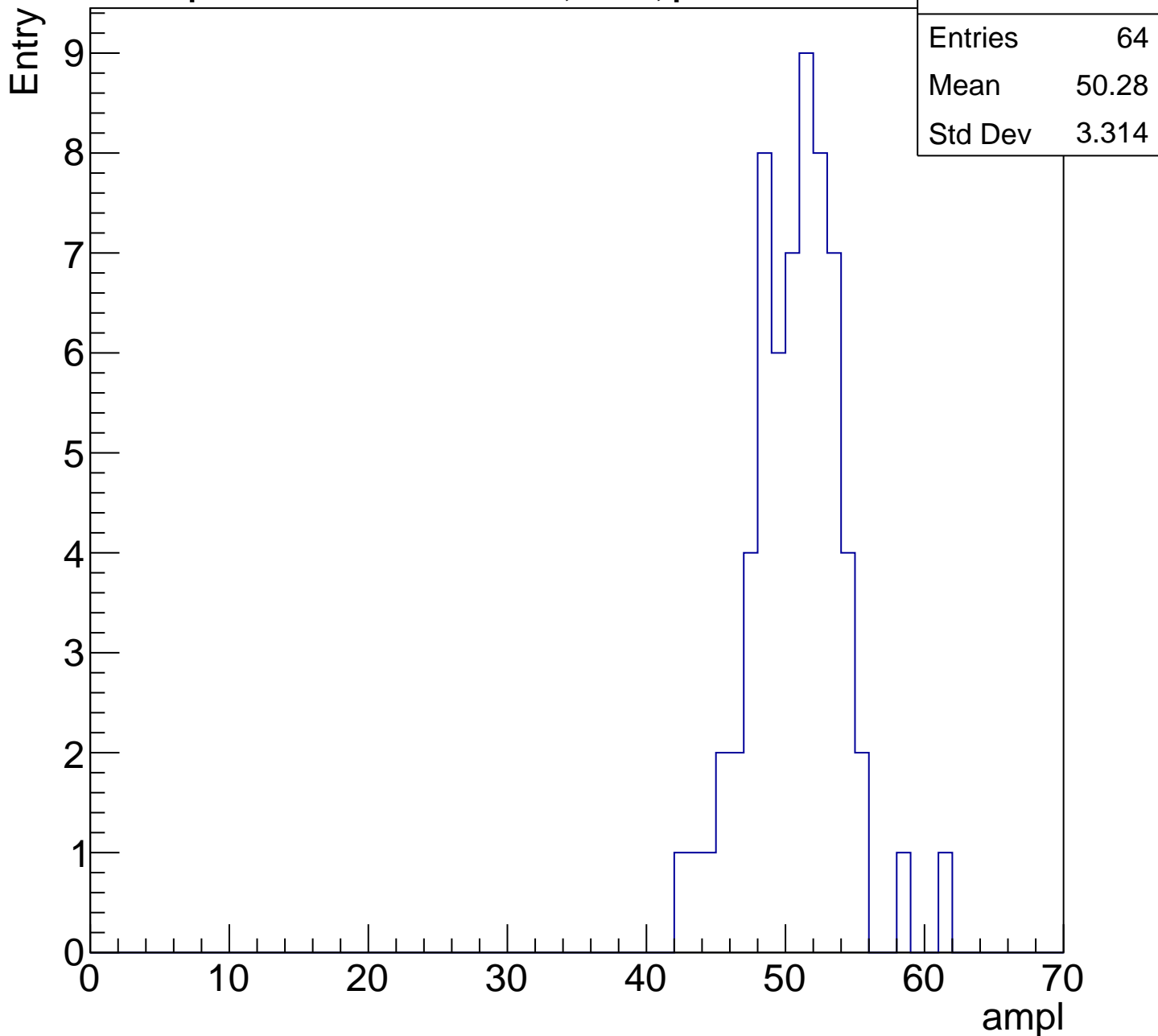
Entries	69
Mean	43.38
Std Dev	3.24

**Gaus mean : 45.1857**  
**Gaus Width: 2.6965**



# B1L101S, U20-ch5, adc3

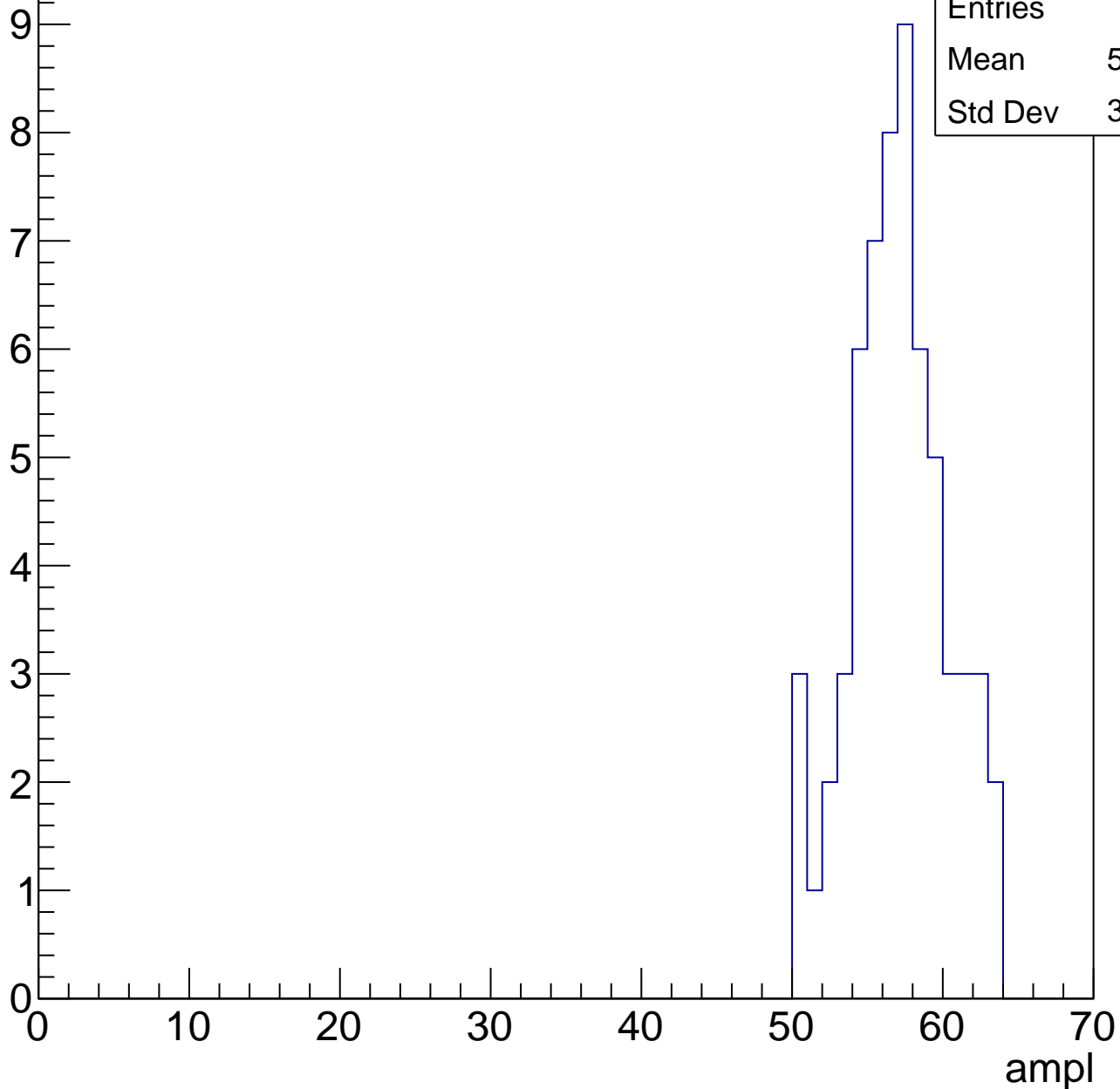
calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U20-ch5, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U20-ch5, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

7

6

5

4

3

2

1

0

0

10

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30

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50

60

70

ampl

Entries

36

Mean

58.47

Std Dev

10.1

0

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3

# B1L101S, U20-ch5, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U20-ch5, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L101S, U20-ch6, adc0

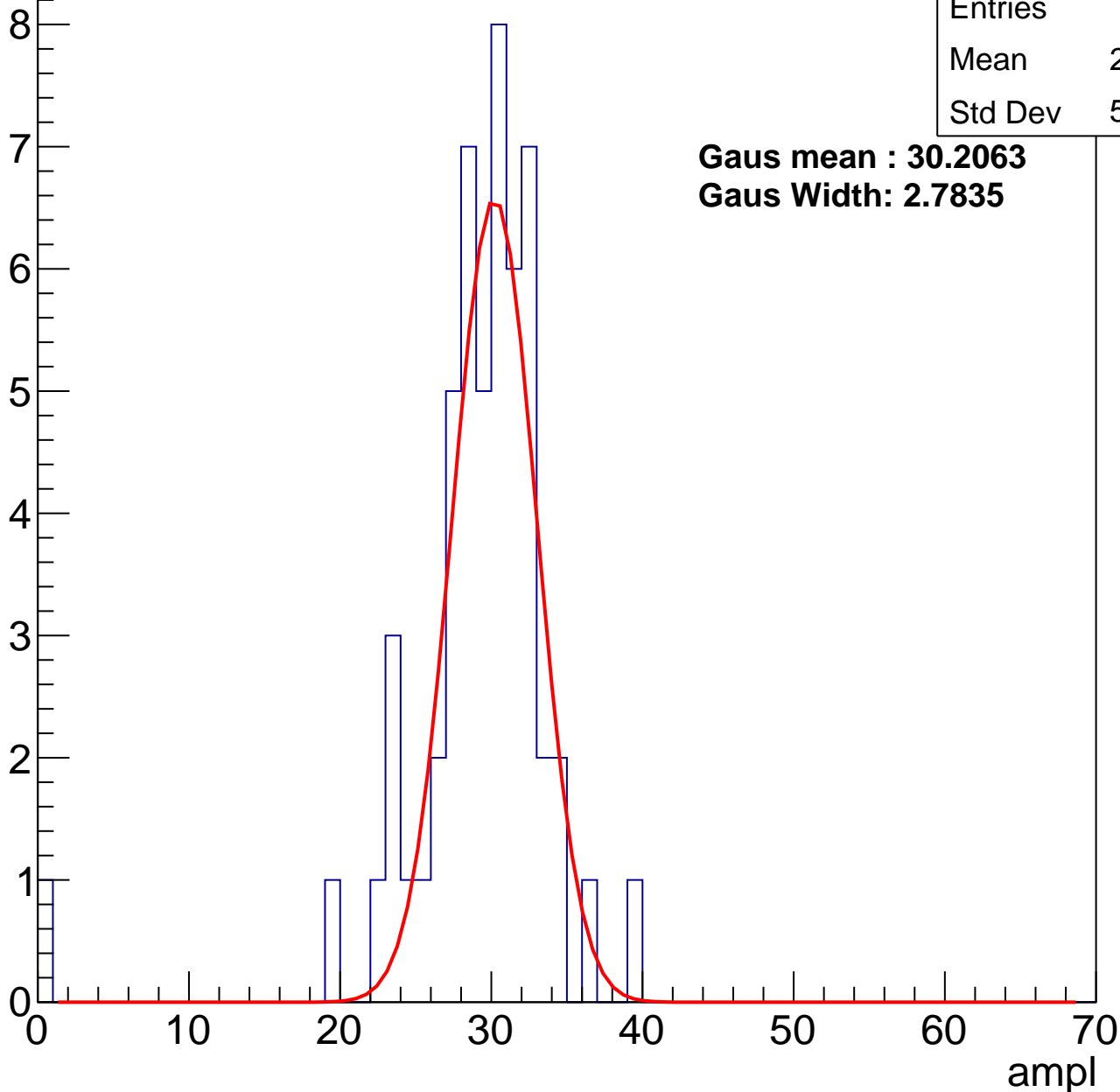
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	54
Mean	28.63
Std Dev	5.275

**Gaus mean : 30.2063**

**Gaus Width: 2.7835**



# B1L101S, U20-ch6, adc1

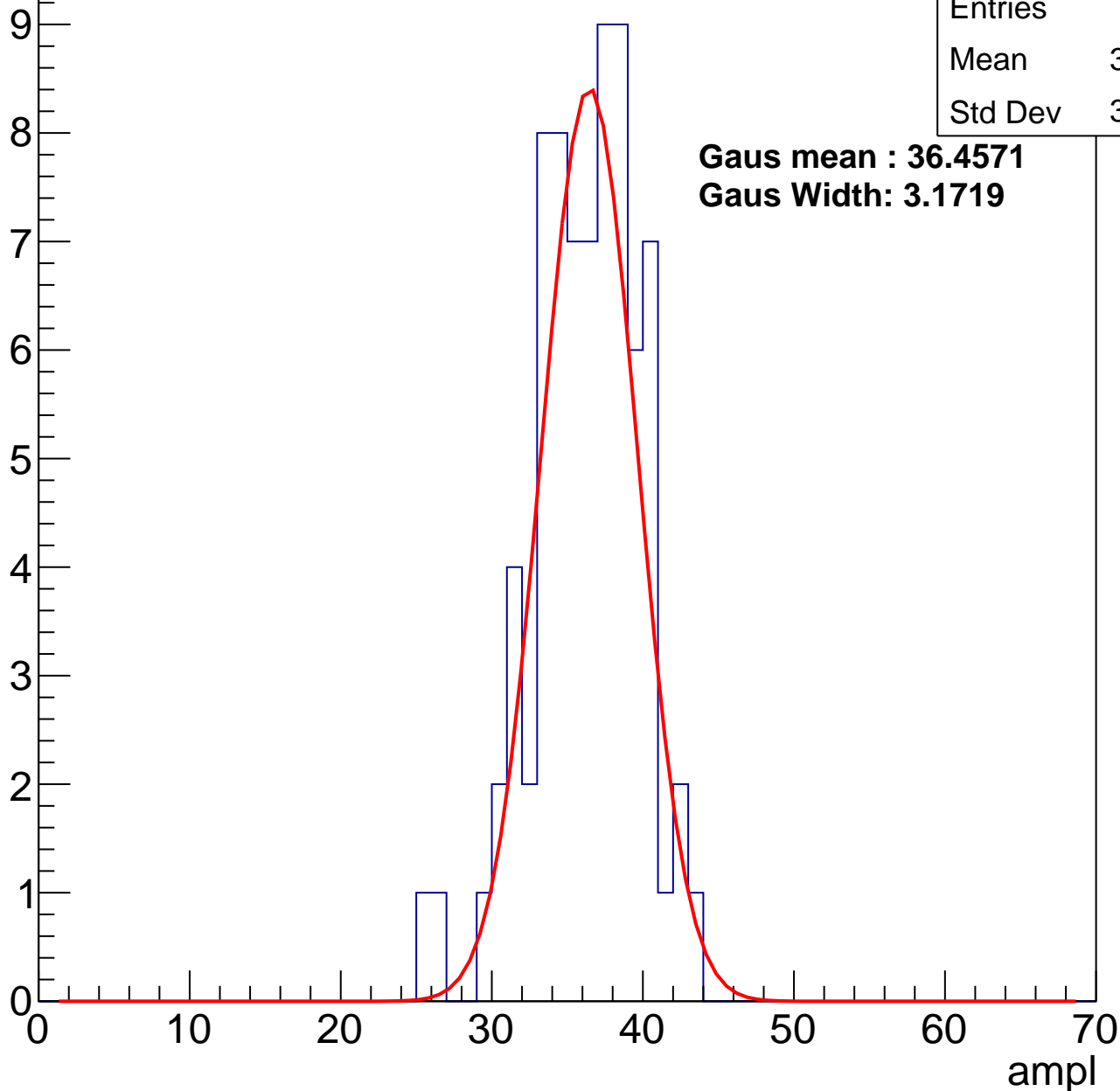
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	76
Mean	35.76
Std Dev	3.513

**Gaus mean : 36.4571**

**Gaus Width: 3.1719**



# B1L101S, U20-ch6, adc2

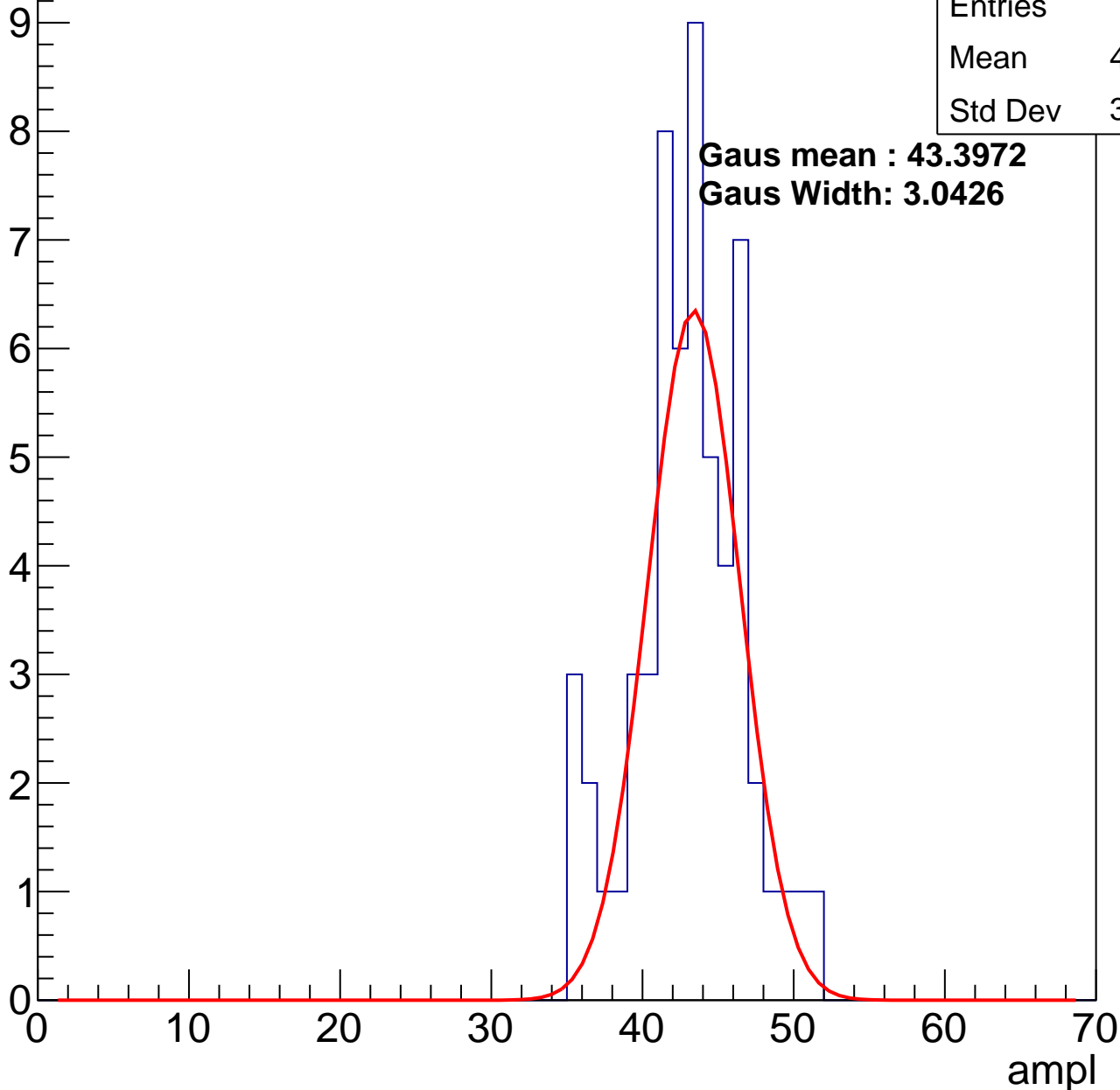
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	58
Mean	42.59
Std Dev	3.582

**Gaus mean : 43.3972**

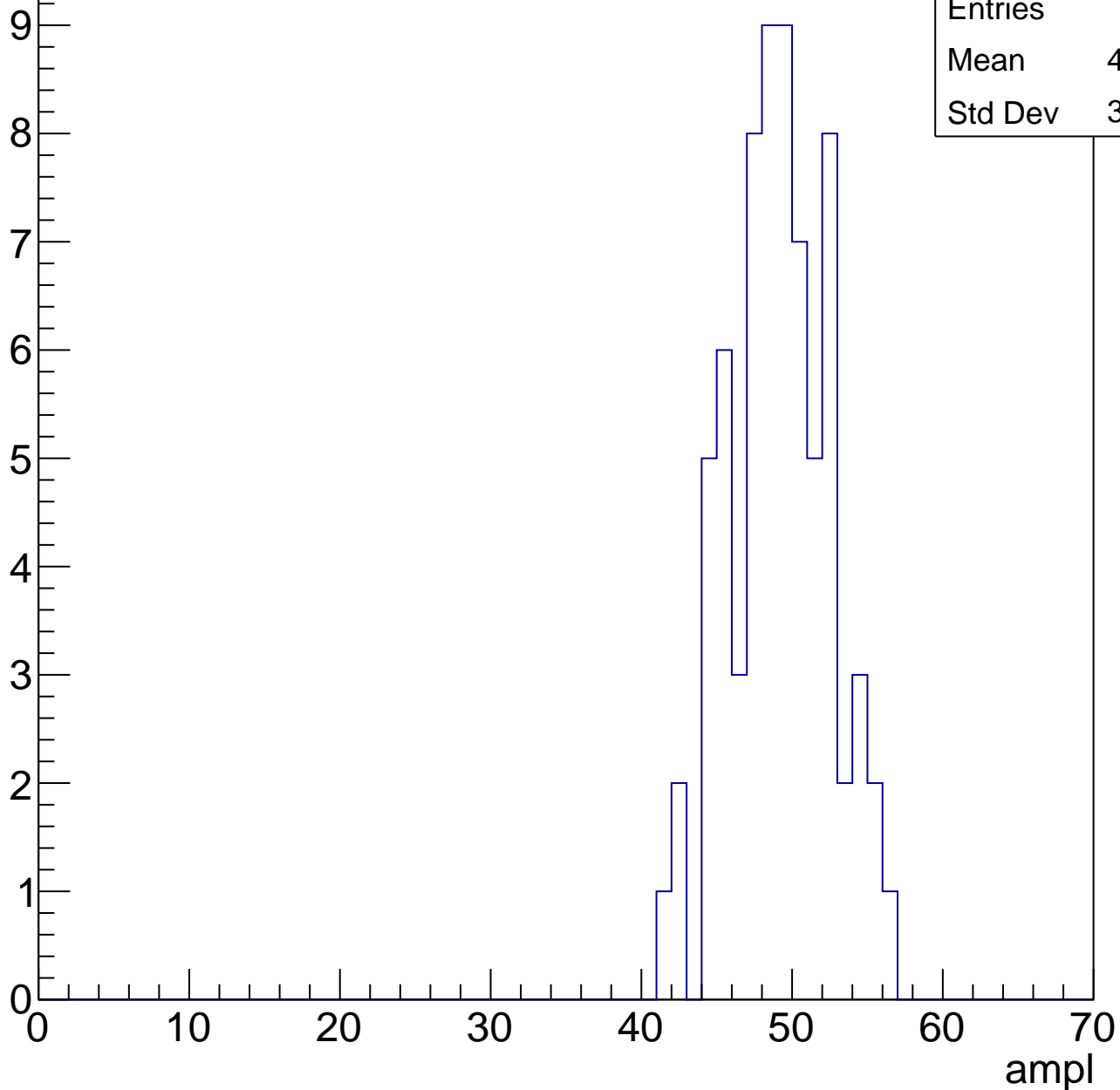
**Gaus Width: 3.0426**



# B1L101S, U20-ch6, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

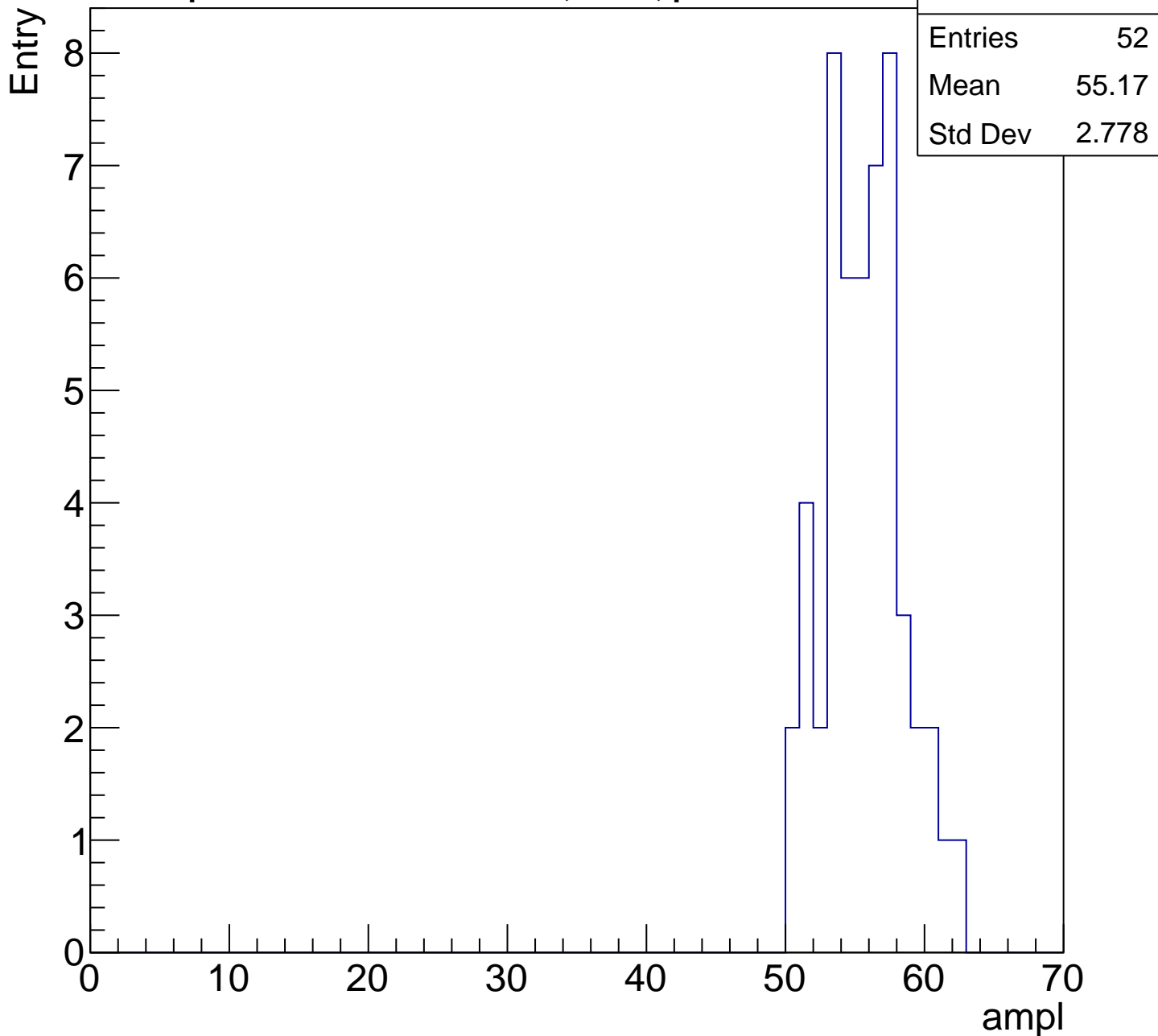
Entry



Entries	71
Mean	48.69
Std Dev	3.296

# B1L101S, U20-ch6, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U20-ch6, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	52
Mean	58.77
Std Dev	8.545

ampl

0 10 20 30 40 50 60 70

0

1

2

3

4

5

6

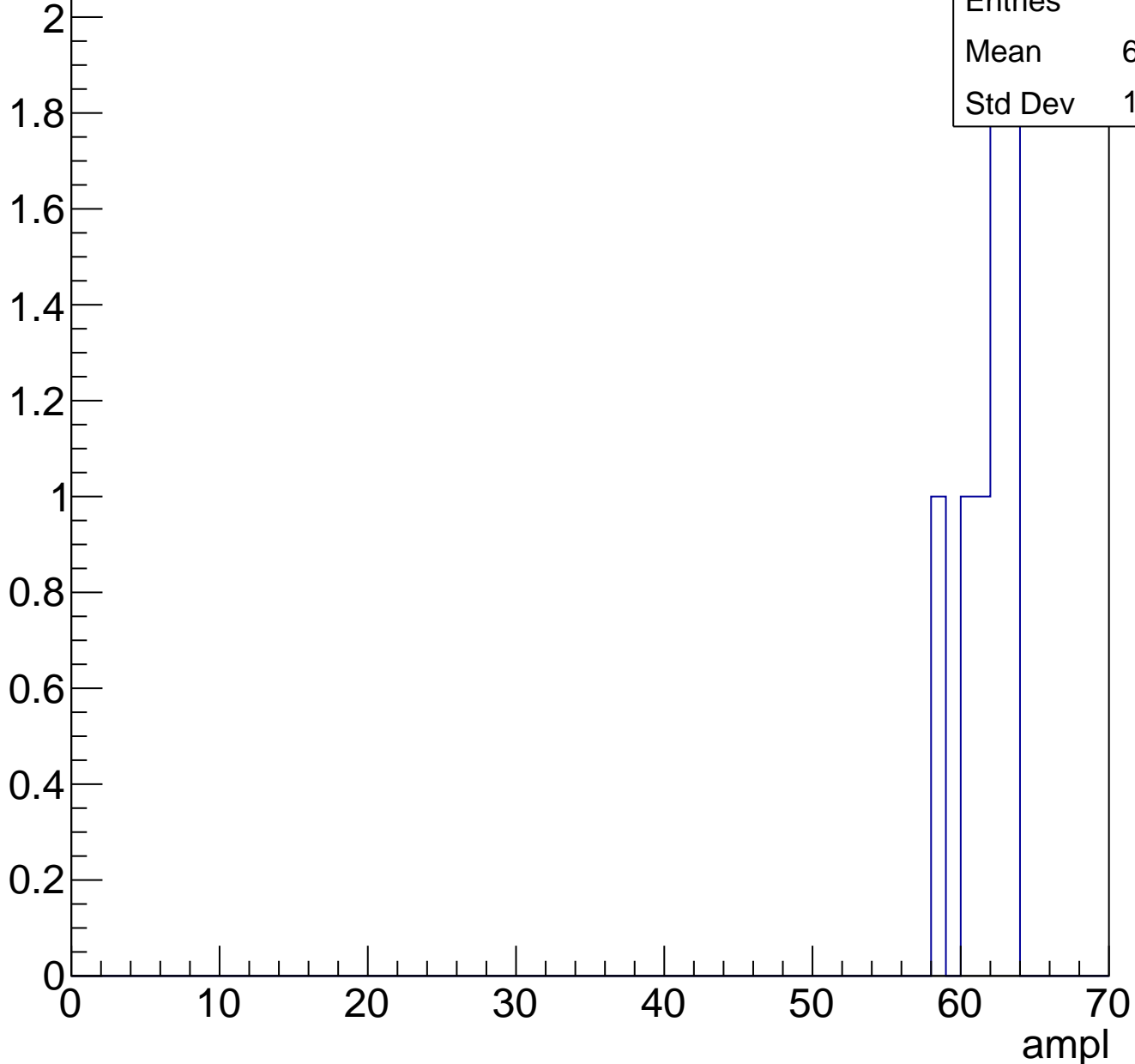
7

8

# B1L101S, U20-ch6, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U20-ch6, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U20-ch7, adc0

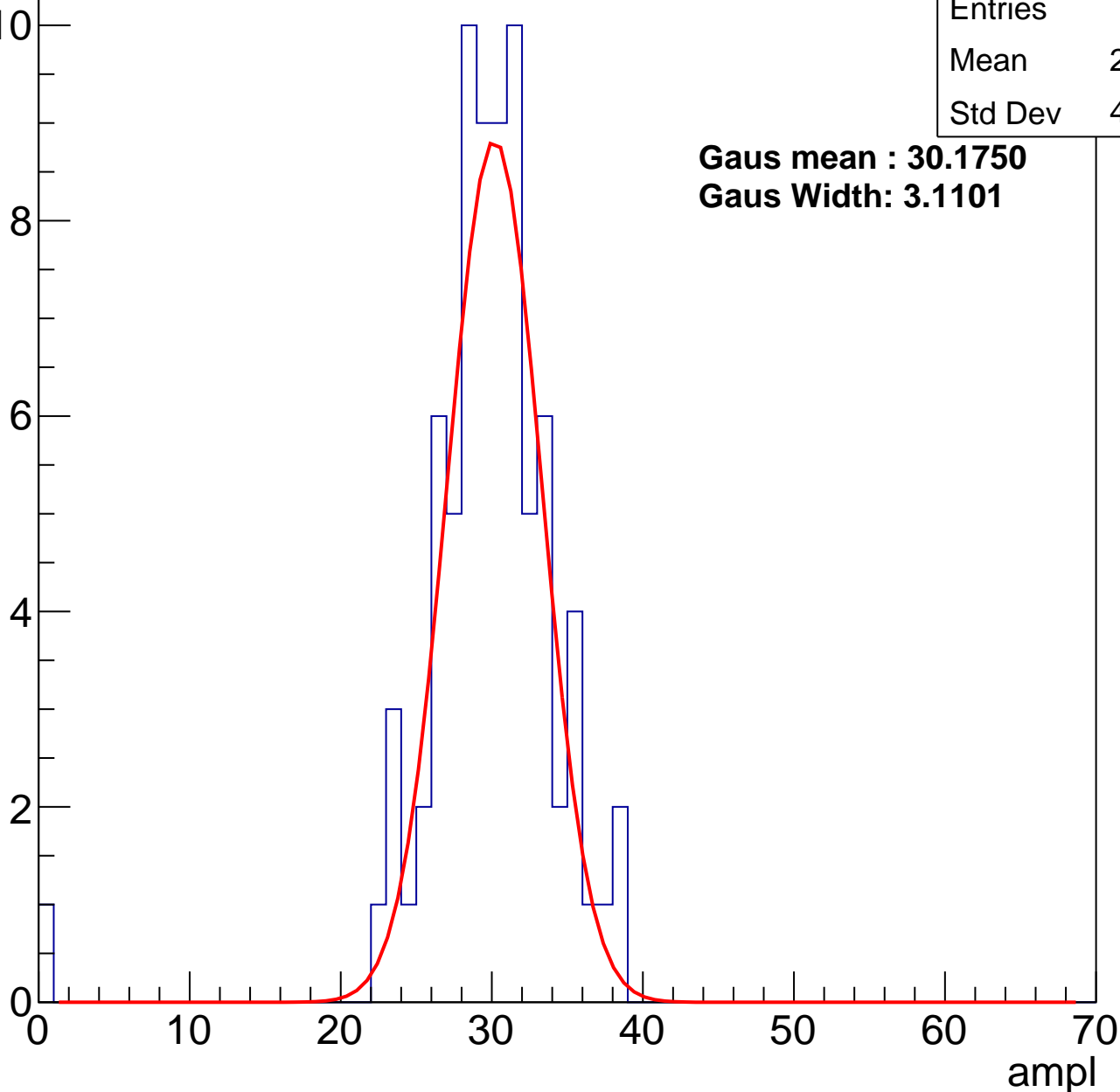
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	78
Mean	29.38
Std Dev	4.786

**Gaus mean : 30.1750**

**Gaus Width: 3.1101**



# B1L101S, U20-ch7, adc1

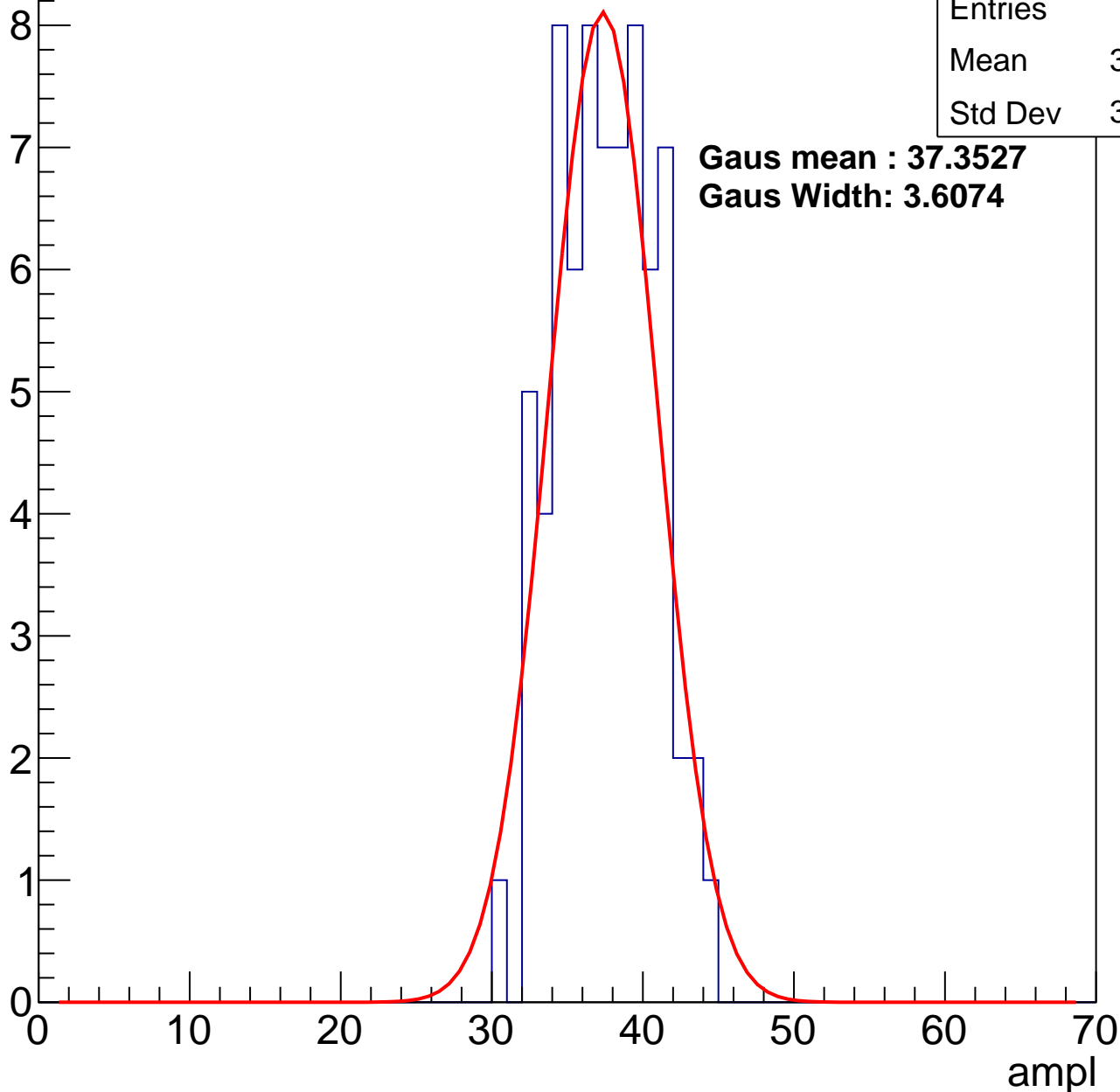
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	72
Mean	37.08
Std Dev	3.157

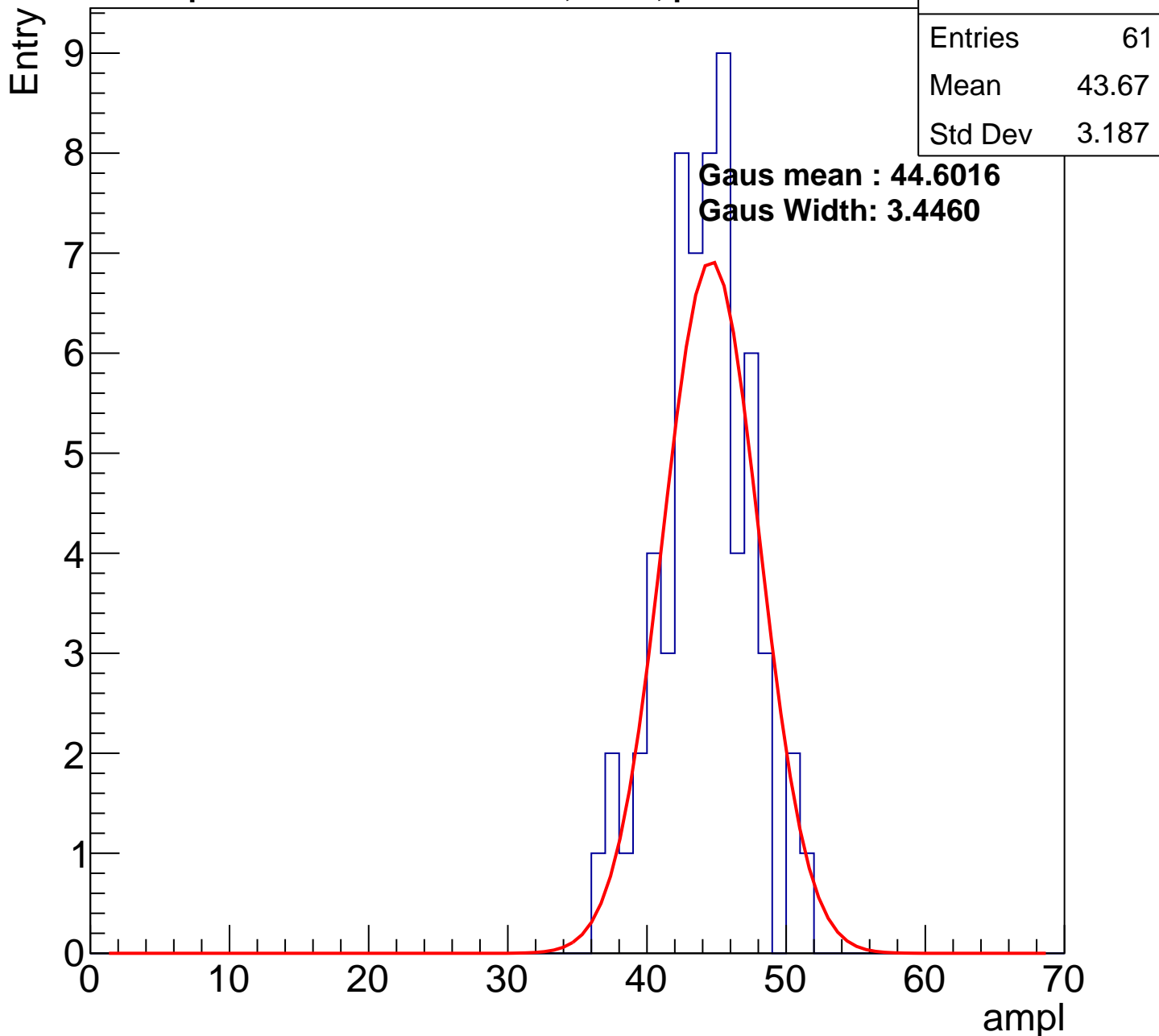
**Gaus mean : 37.3527**

**Gaus Width: 3.6074**



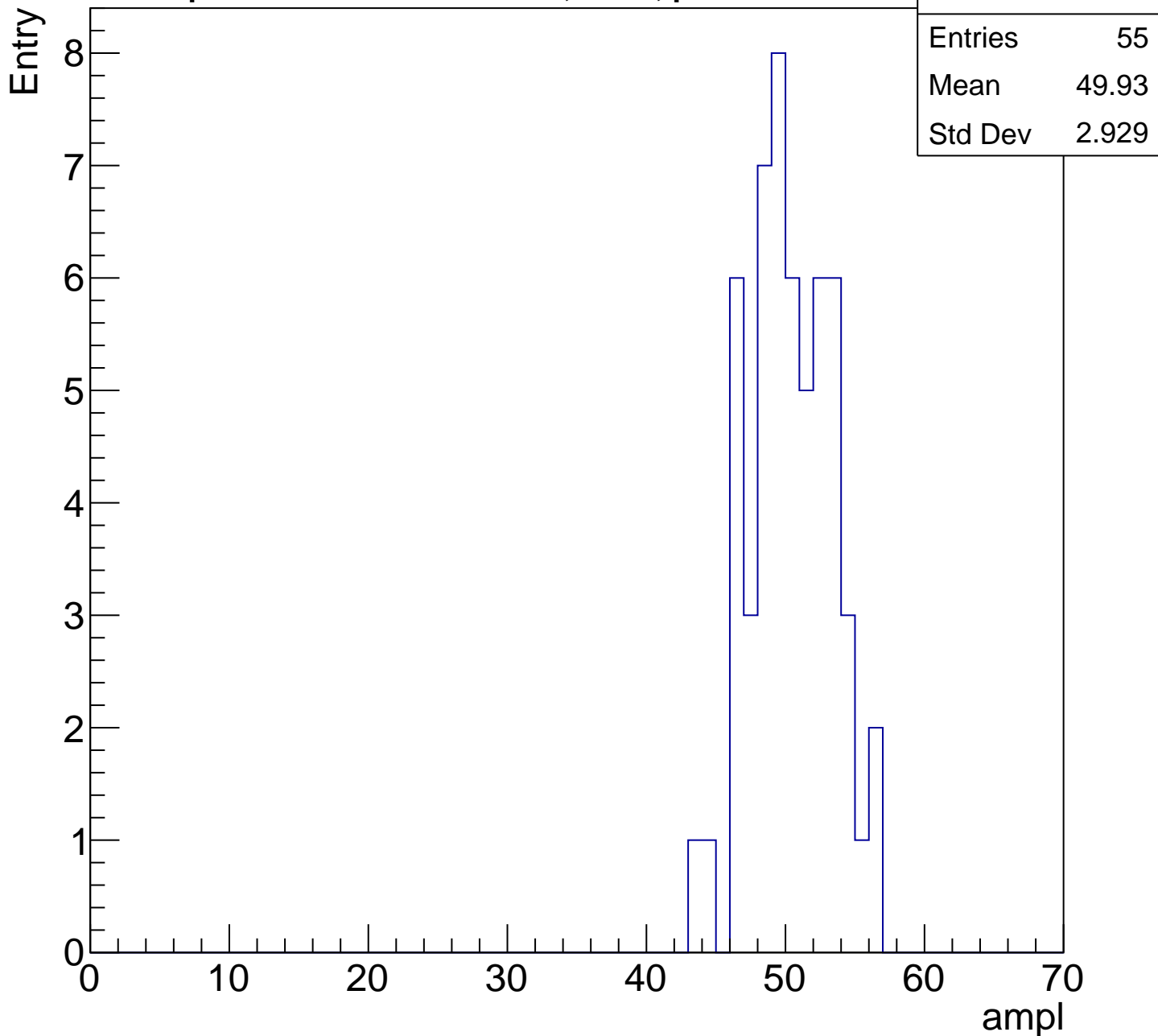
# B1L101S, U20-ch7, adc2

calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U20-ch7, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U20-ch7, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

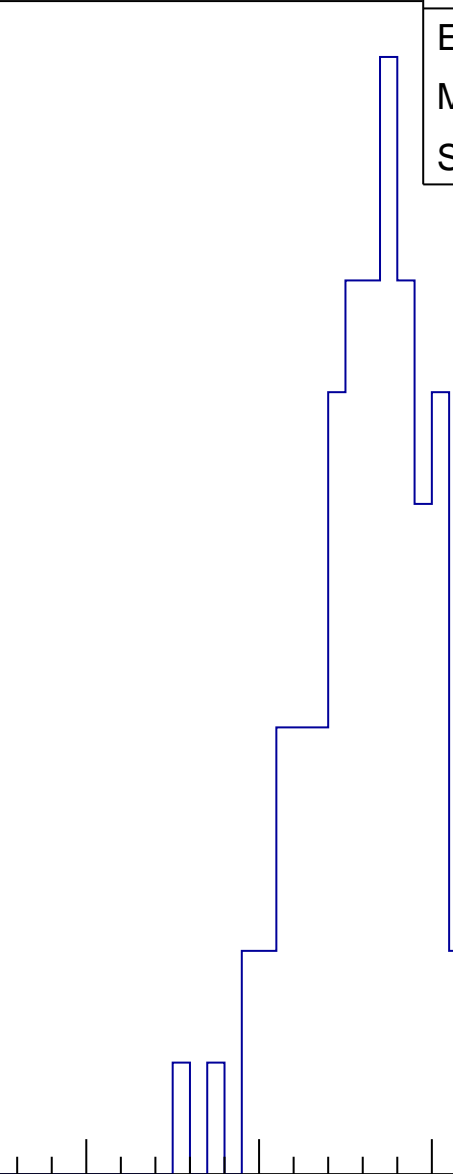
Entries	75
Mean	55.64
Std Dev	3.474

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

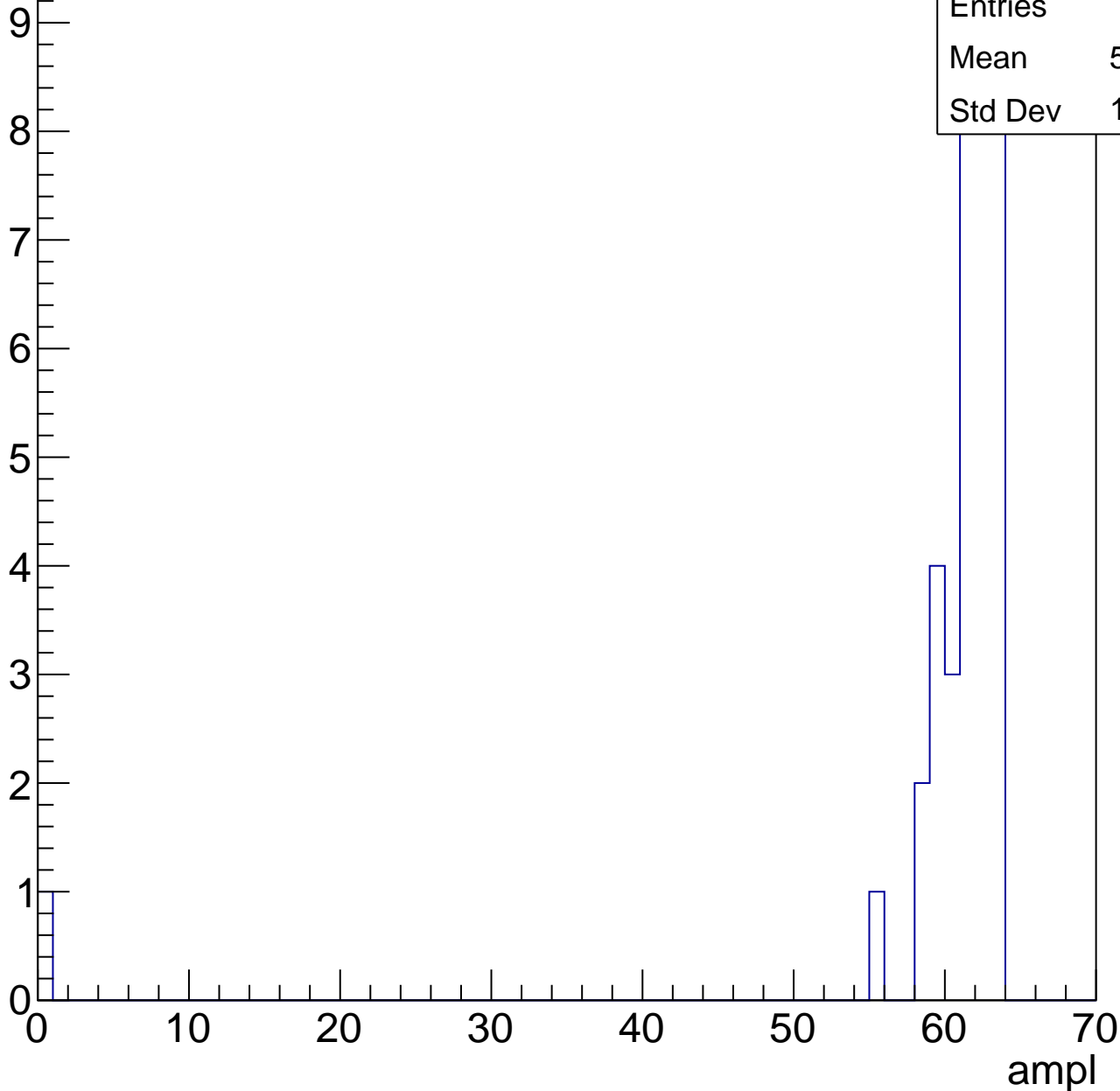


# B1L101S, U20-ch7, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	36
Mean	59.36
Std Dev	10.19



# B1L101S, U20-ch7, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U20-ch7, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	3
Mean	7.333
Std Dev	10.37

# B1L101S, U20-ch8, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	81
Mean	29.23
Std Dev	4.897

**Gaus mean : 30.3964**

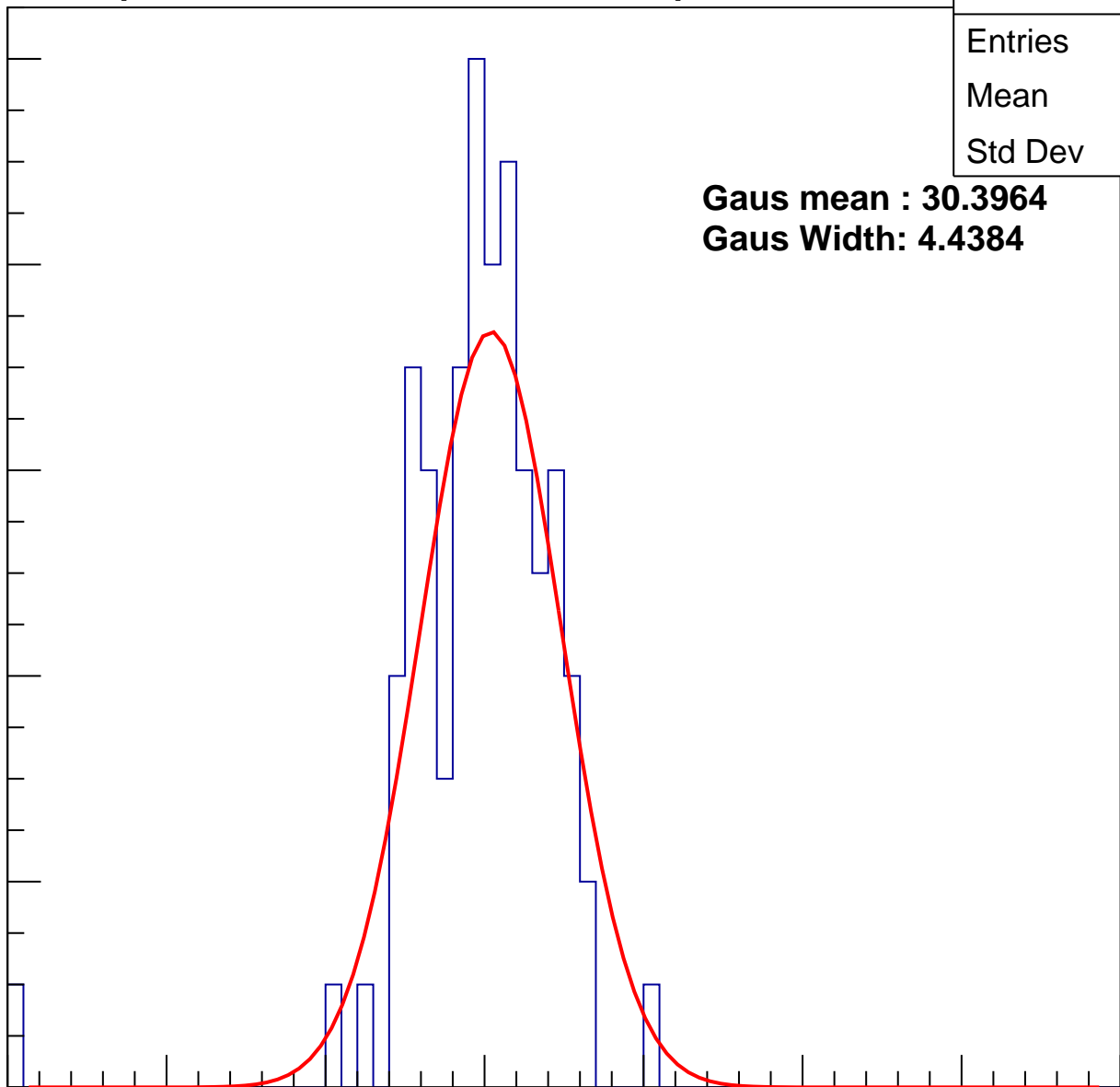
**Gaus Width: 4.4384**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U20-ch8, adc1

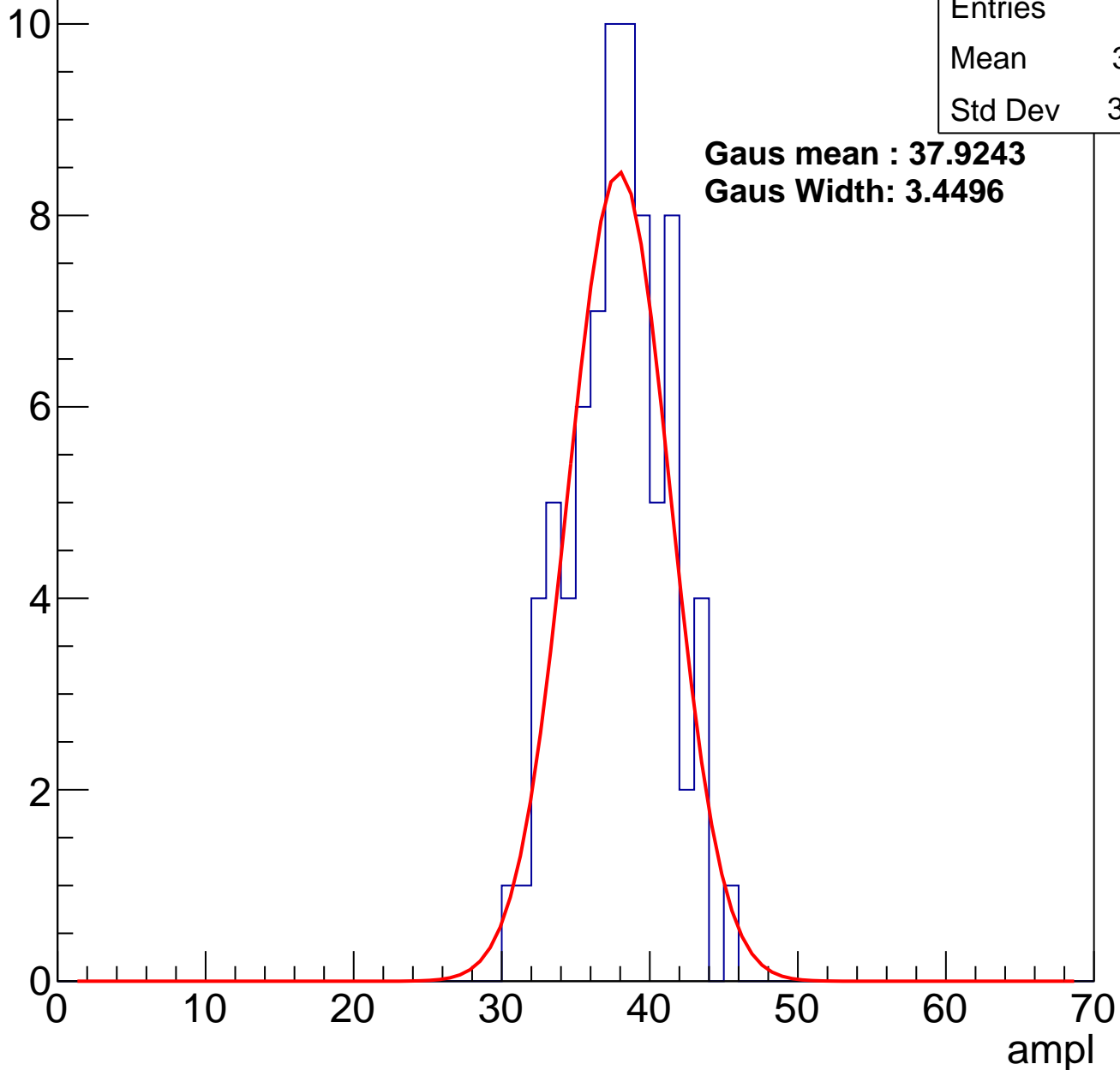
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	76
Mean	37.41
Std Dev	3.229

**Gaus mean : 37.9243**

**Gaus Width: 3.4496**

Entry



# B1L101S, U20-ch8, adc2

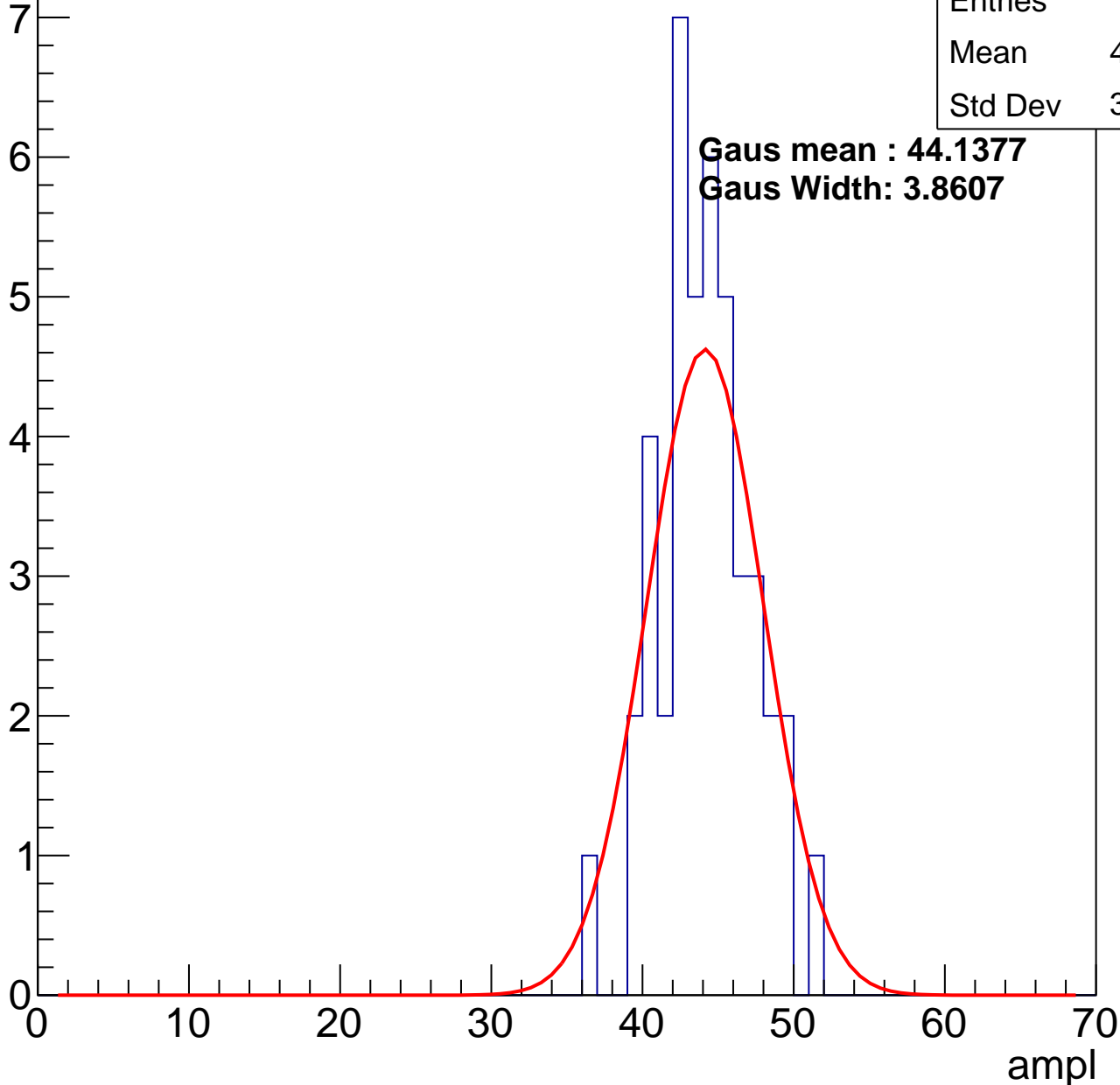
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	43
Mean	43.67
Std Dev	3.048

**Gaus mean : 44.1377**

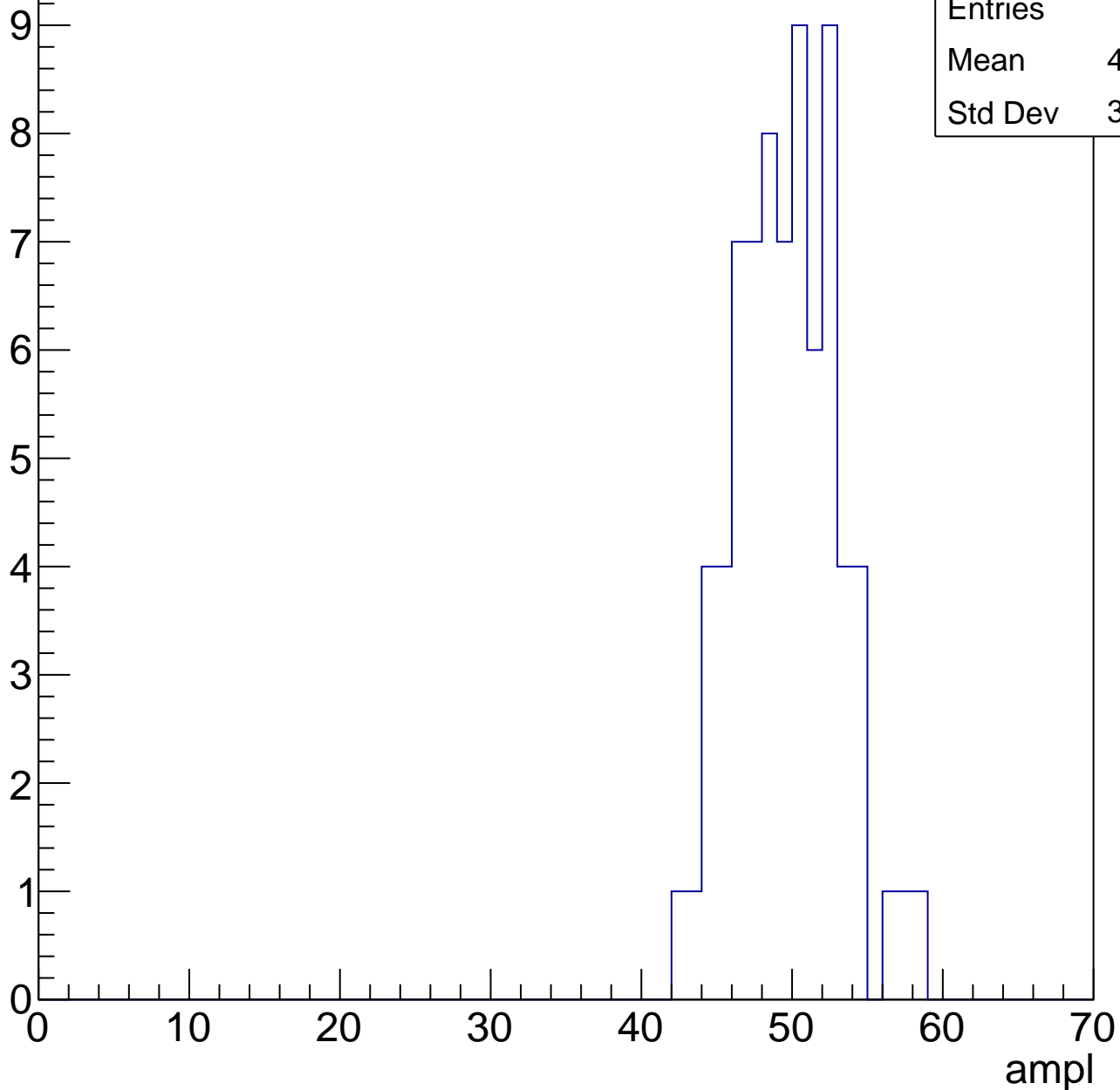
**Gaus Width: 3.8607**



# B1L101S, U20-ch8, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



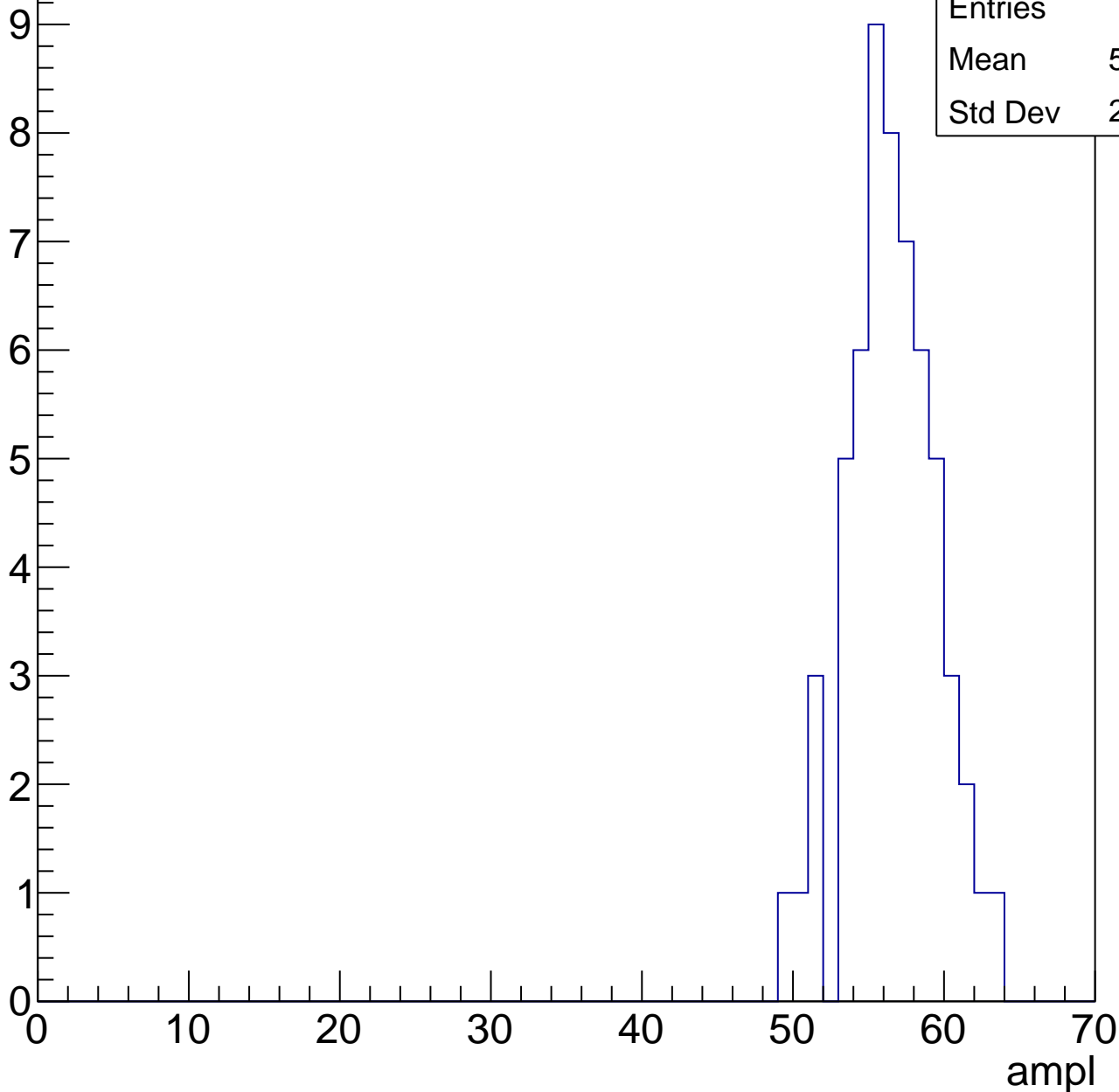
Entries	74
Mean	49.22
Std Dev	3.322

# B1L101S, U20-ch8, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	58
Mean	56.09
Std Dev	2.926

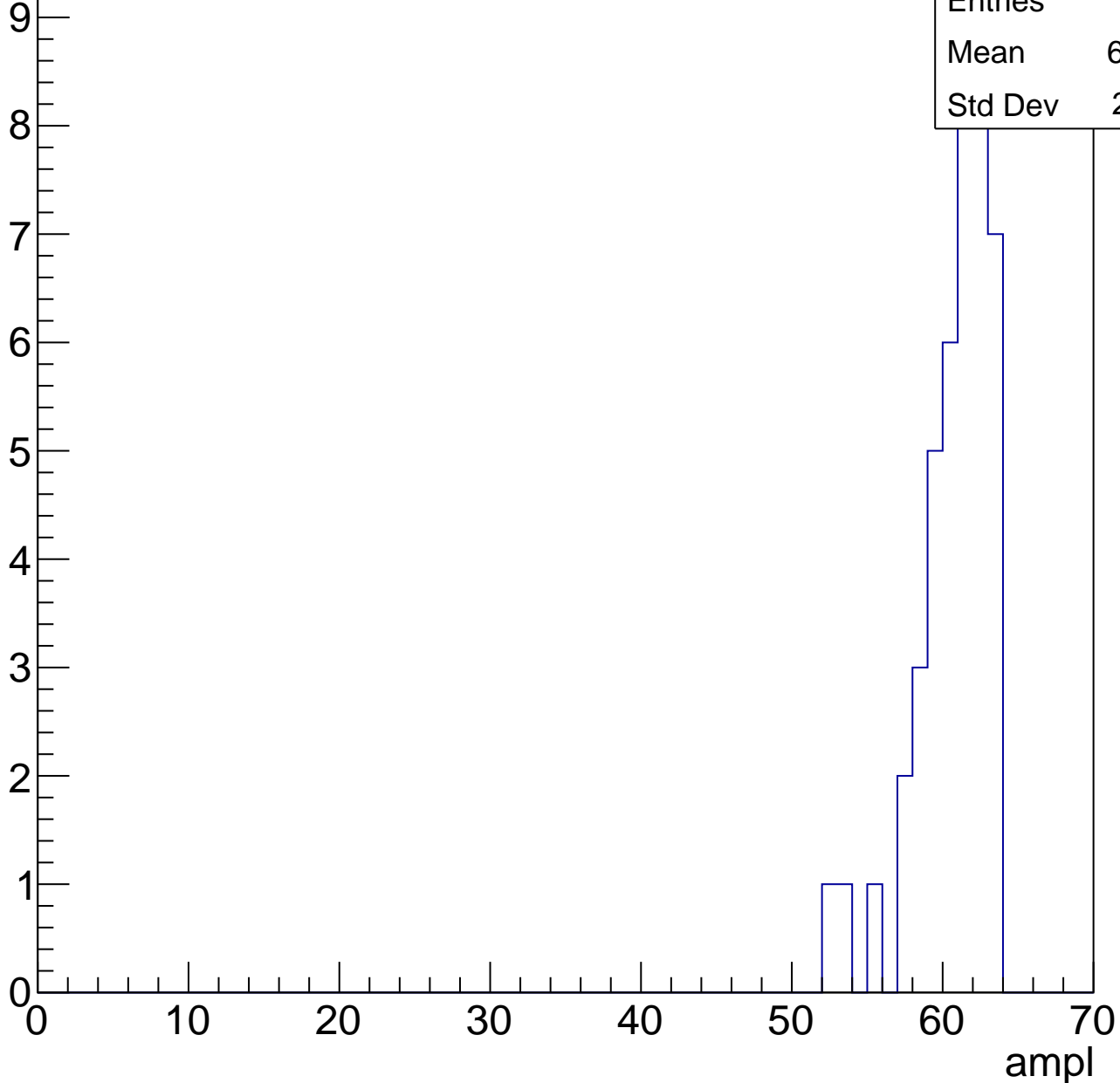


# B1L101S, U20-ch8, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

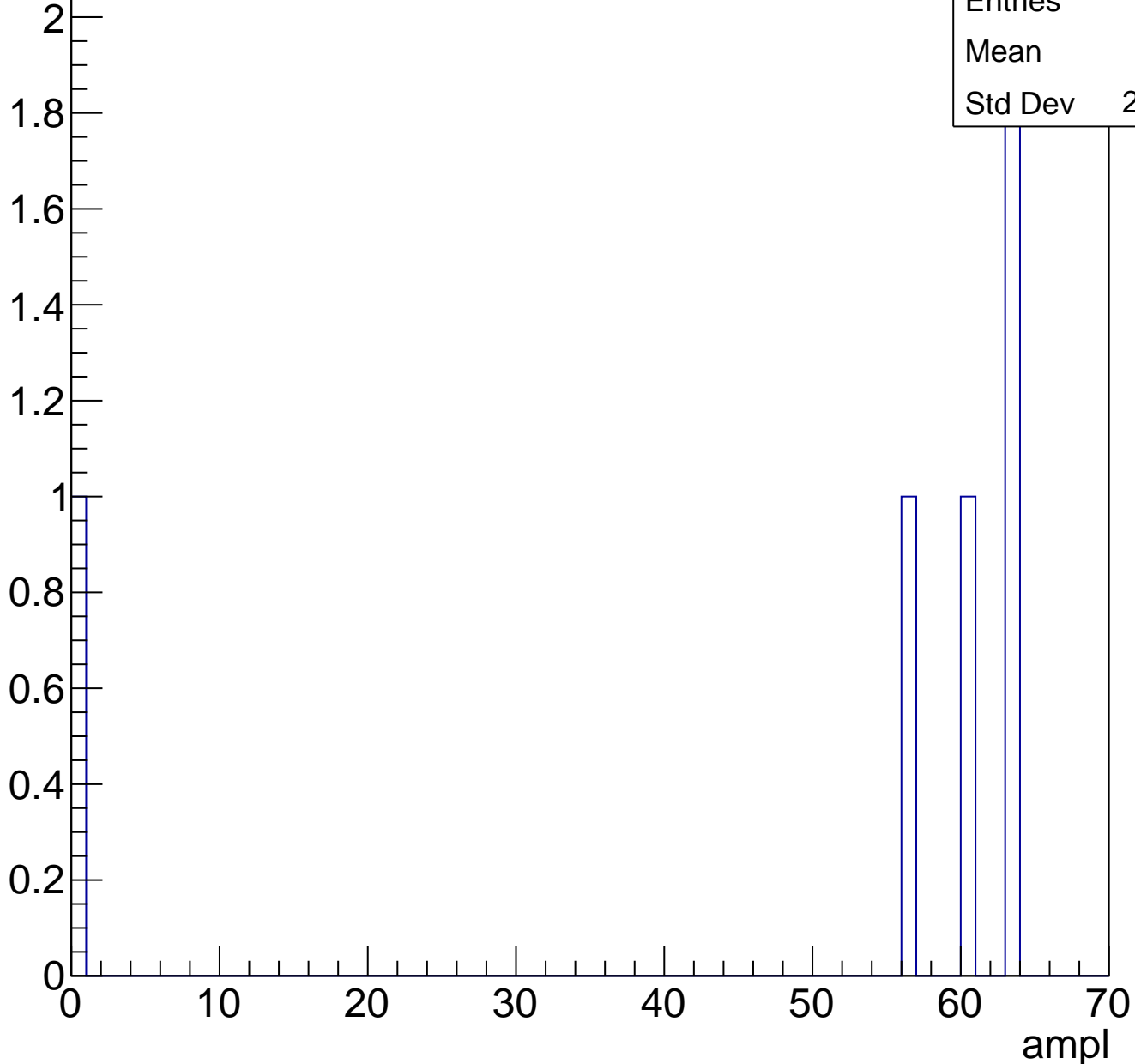
Entries	43
Mean	60.23
Std Dev	2.541



# B1L101S, U20-ch8, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	5
Mean	48.4
Std Dev	24.34



# B1L101S, U20-ch8, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U20-ch9, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	79
Mean	29.99
Std Dev	3.29

**Gaus mean : 30.5571**

**Gaus Width: 3.5067**

10

8

6

4

2

0

0

10

20

30

40

50

60

70

ampl

0

2

4

6

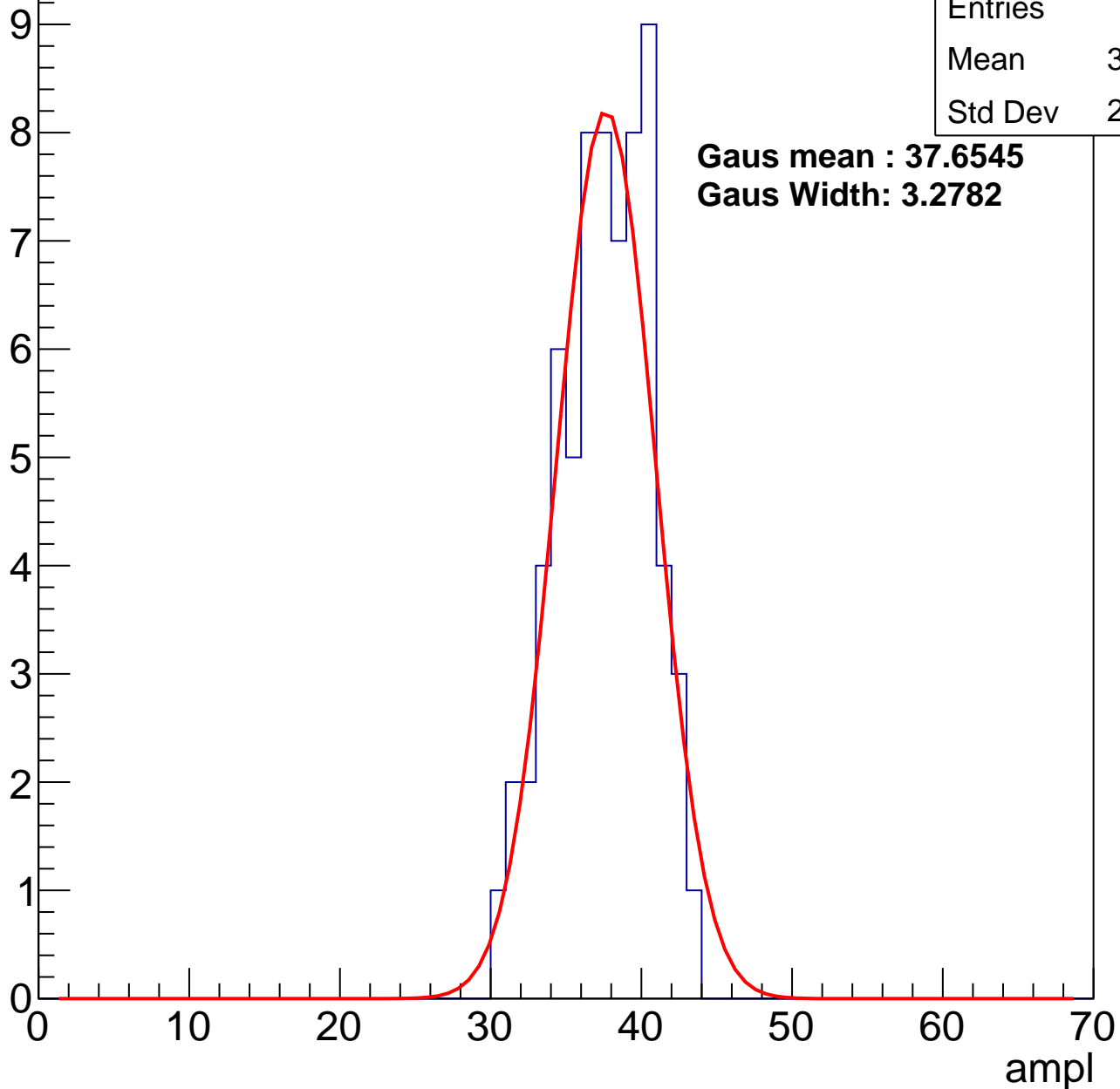
8

10

# B1L101S, U20-ch9, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U20-ch9, adc2

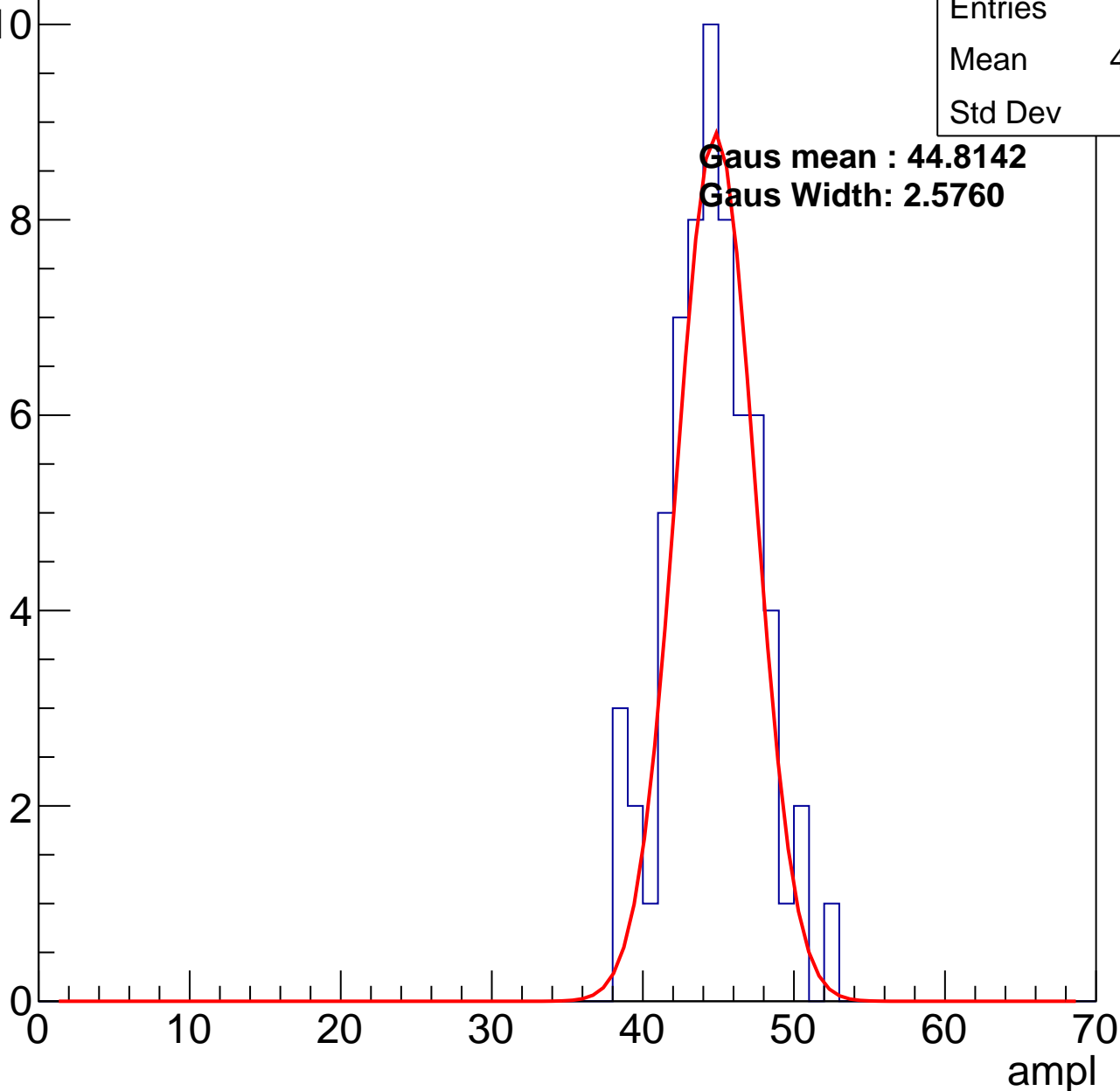
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	44.16
Std Dev	2.97

**Gaus mean : 44.8142**

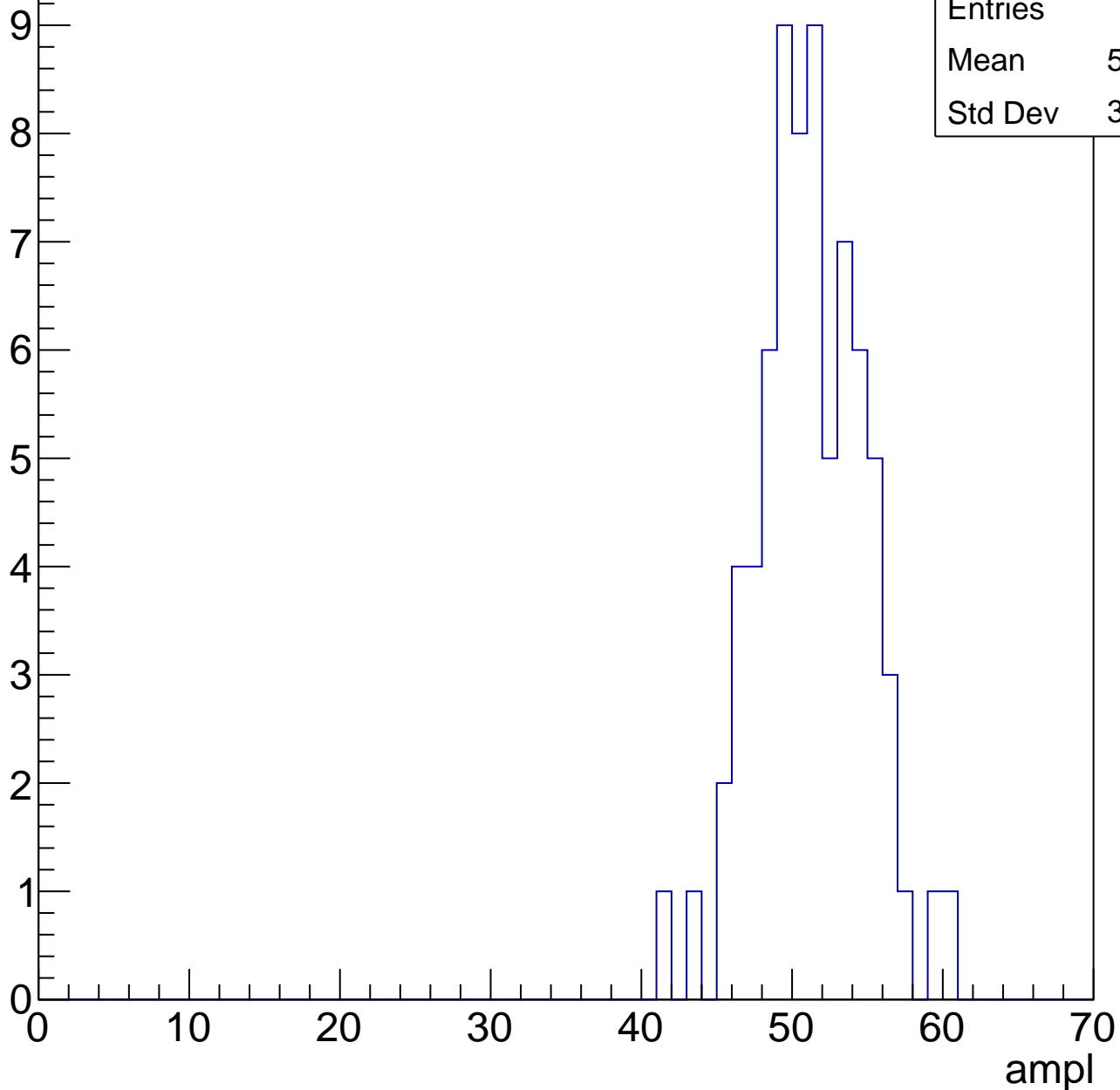
**Gaus Width: 2.5760**



# B1L101S, U20-ch9, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

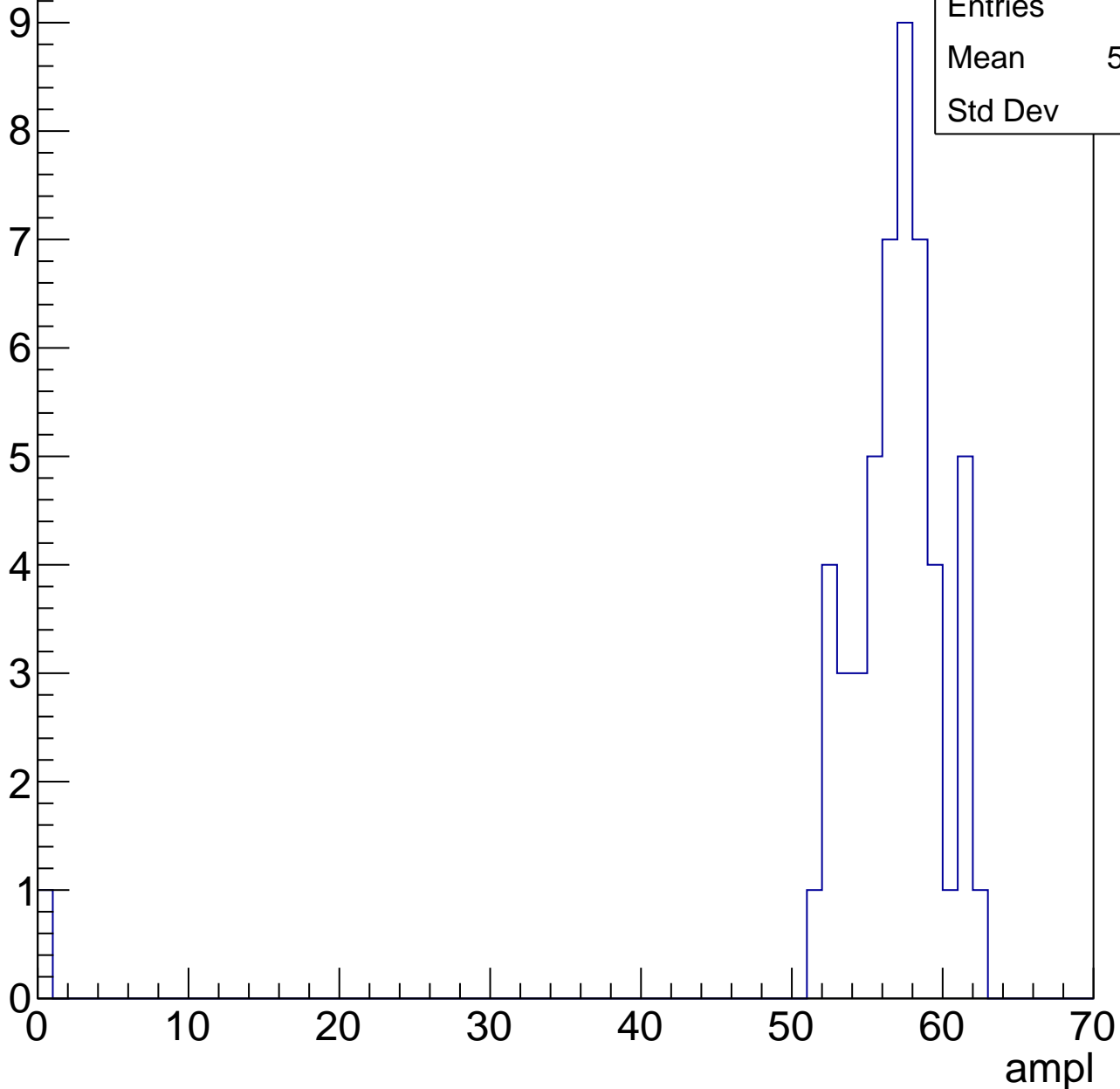


# B1L101S, U20-ch9, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

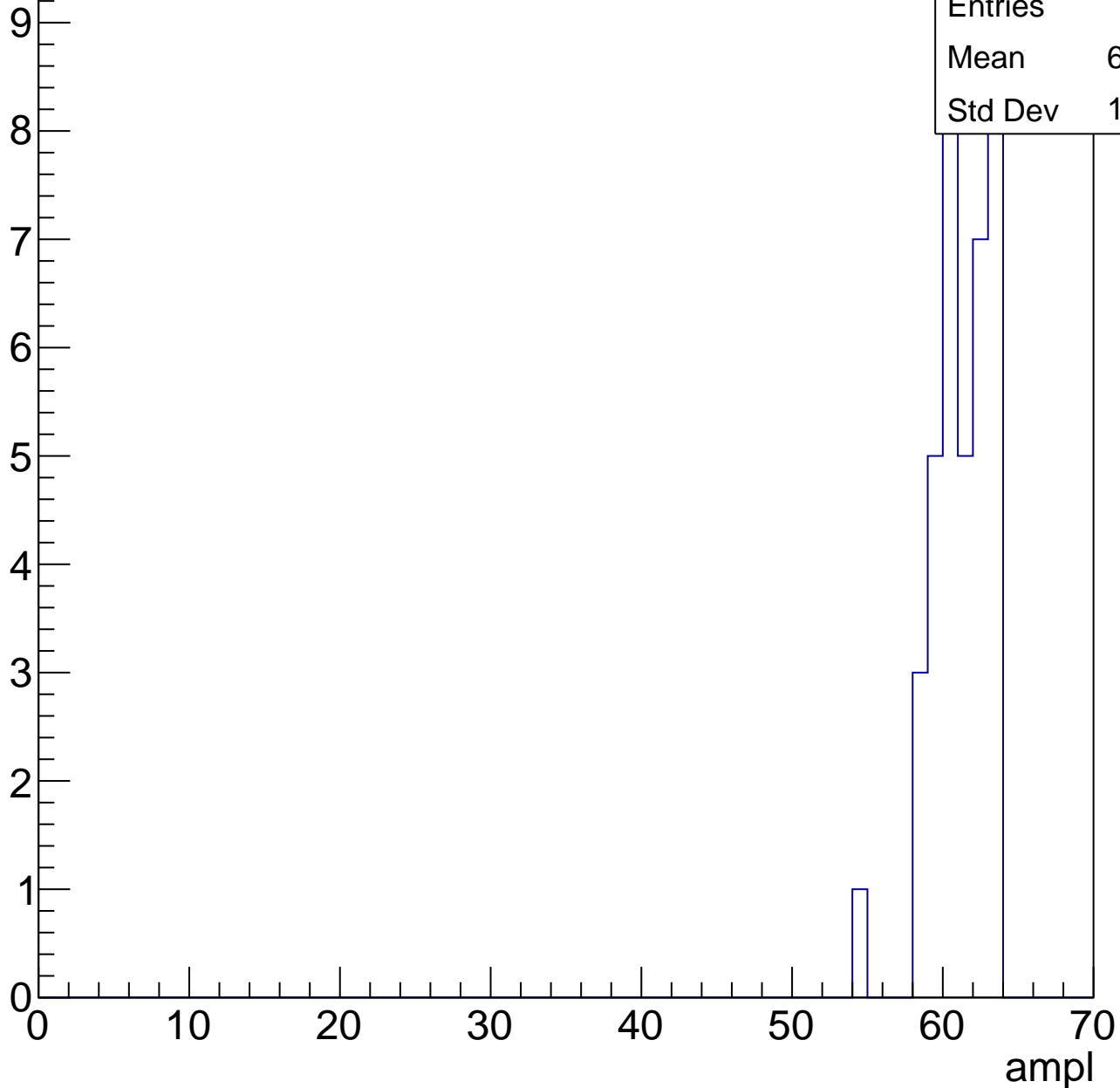
Entries	51
Mean	55.47
Std Dev	8.29



# B1L101S, U20-ch9, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U20-ch9, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

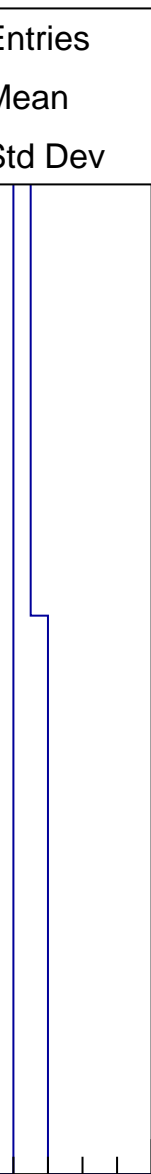
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	3
Mean	62.33
Std Dev	0.4714

0 10 20 30 40 50 60 70

ampl





# B1L101S, U20-ch9, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U20-ch10, adc0

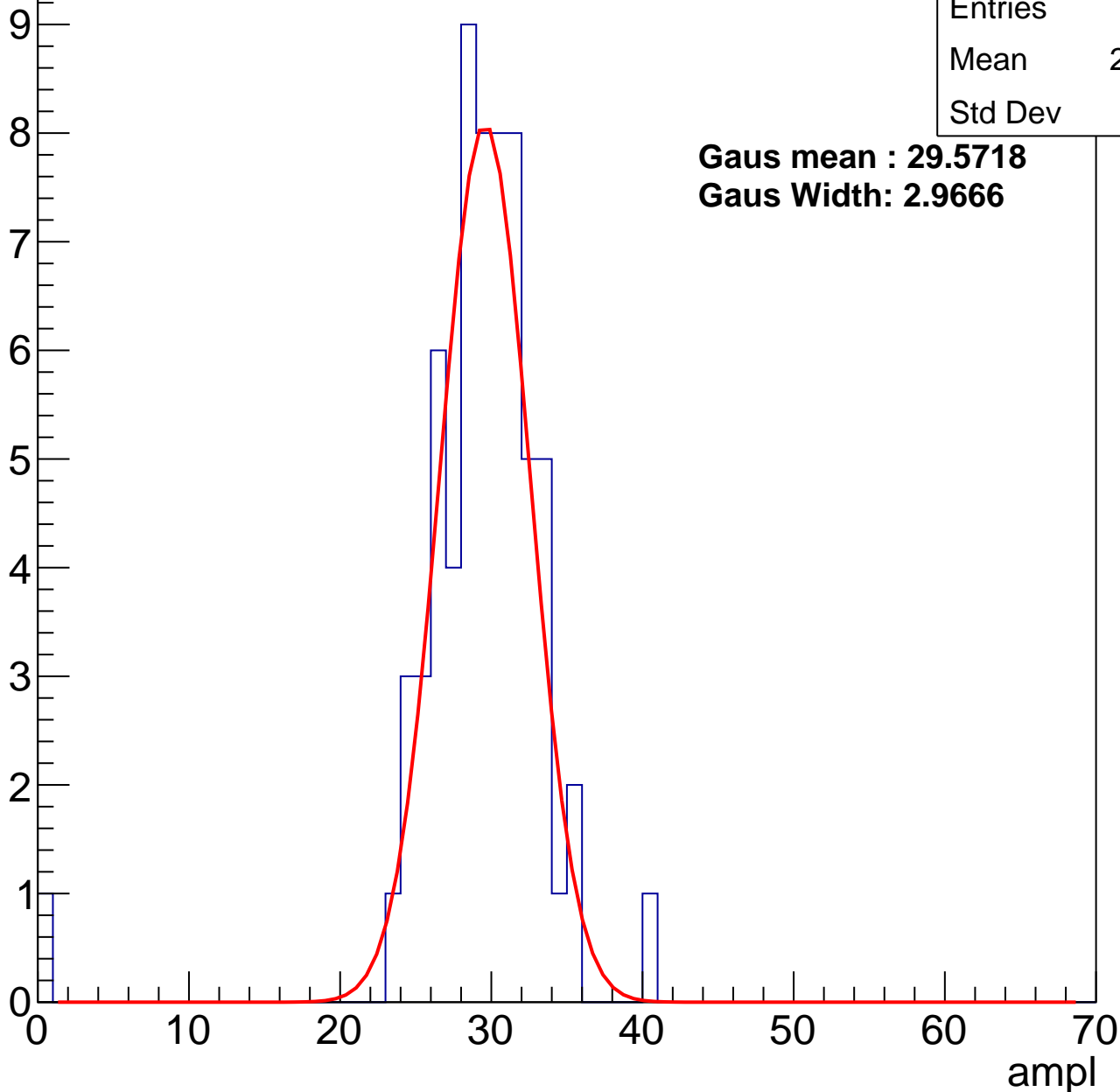
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	28.85
Std Dev	4.74

**Gaus mean : 29.5718**

**Gaus Width: 2.9666**



# B1L101S, U20-ch10, adc1

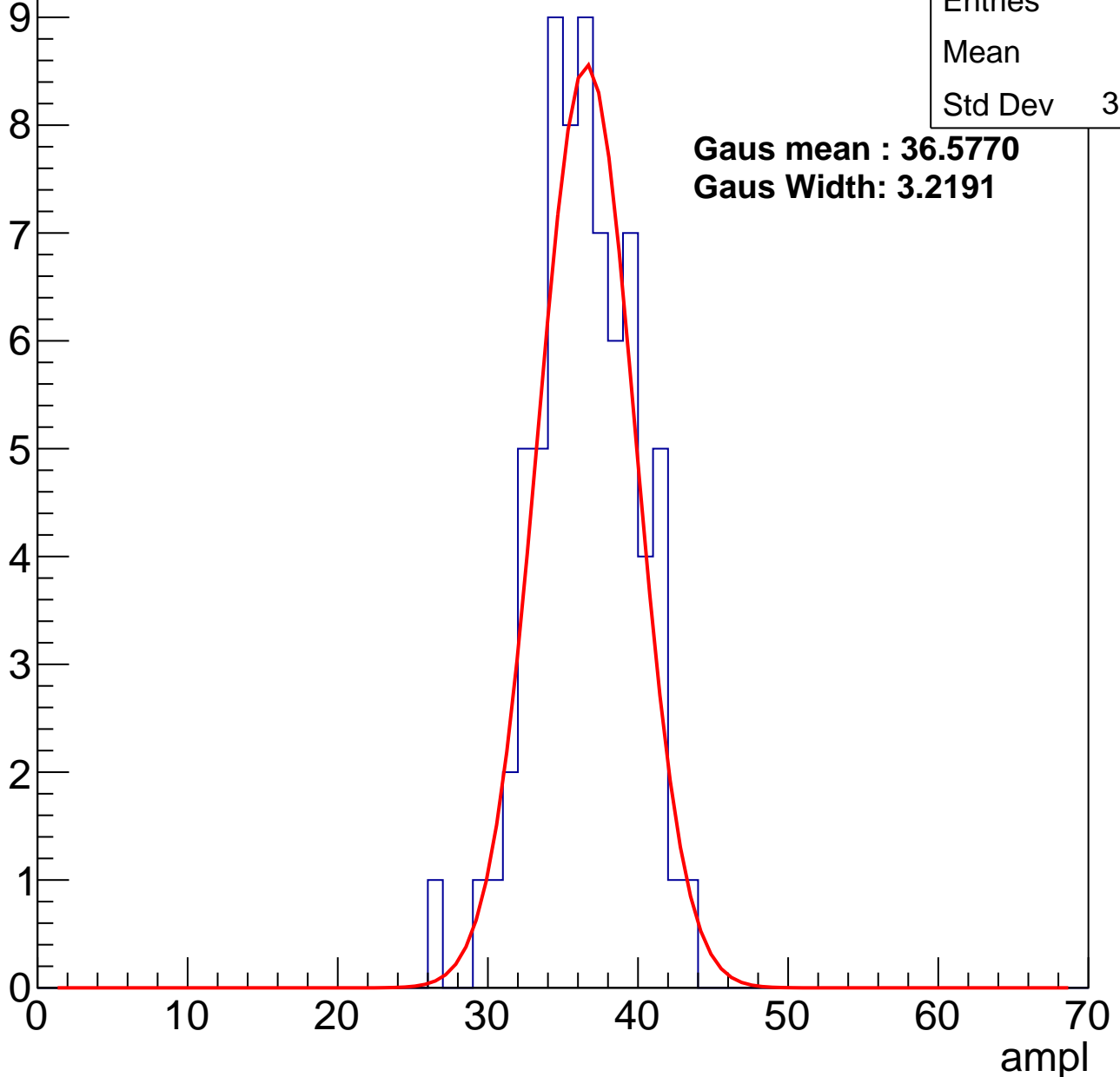
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	72
Mean	36
Std Dev	3.274

**Gaus mean : 36.5770**

**Gaus Width: 3.2191**



# B1L101S, U20-ch10, adc2

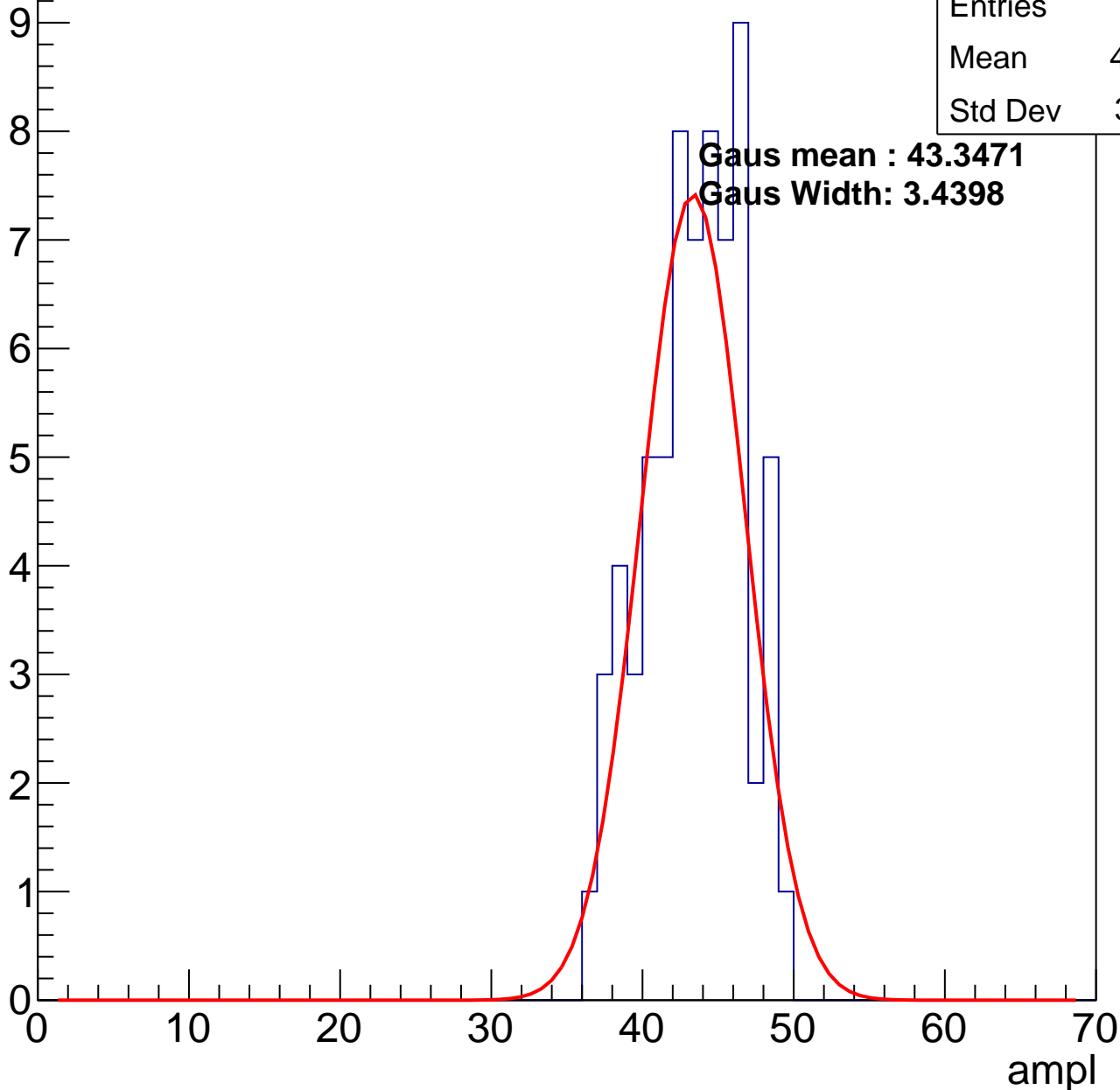
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	42.97
Std Dev	3.181

**Gaus mean : 43.3471**

**Gaus Width: 3.4398**

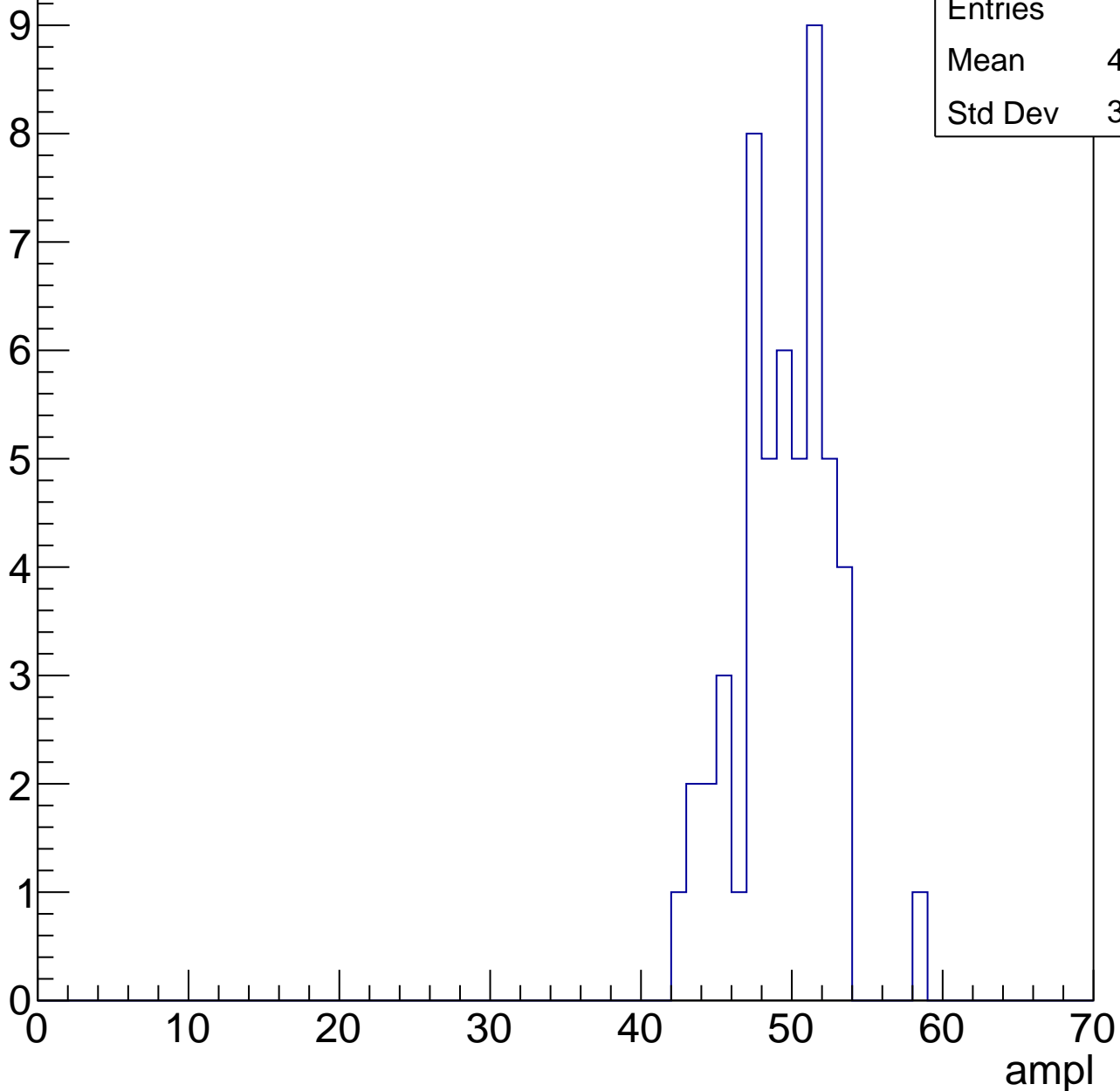


# B1L101S, U20-ch10, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	52
Mean	48.96
Std Dev	3.088

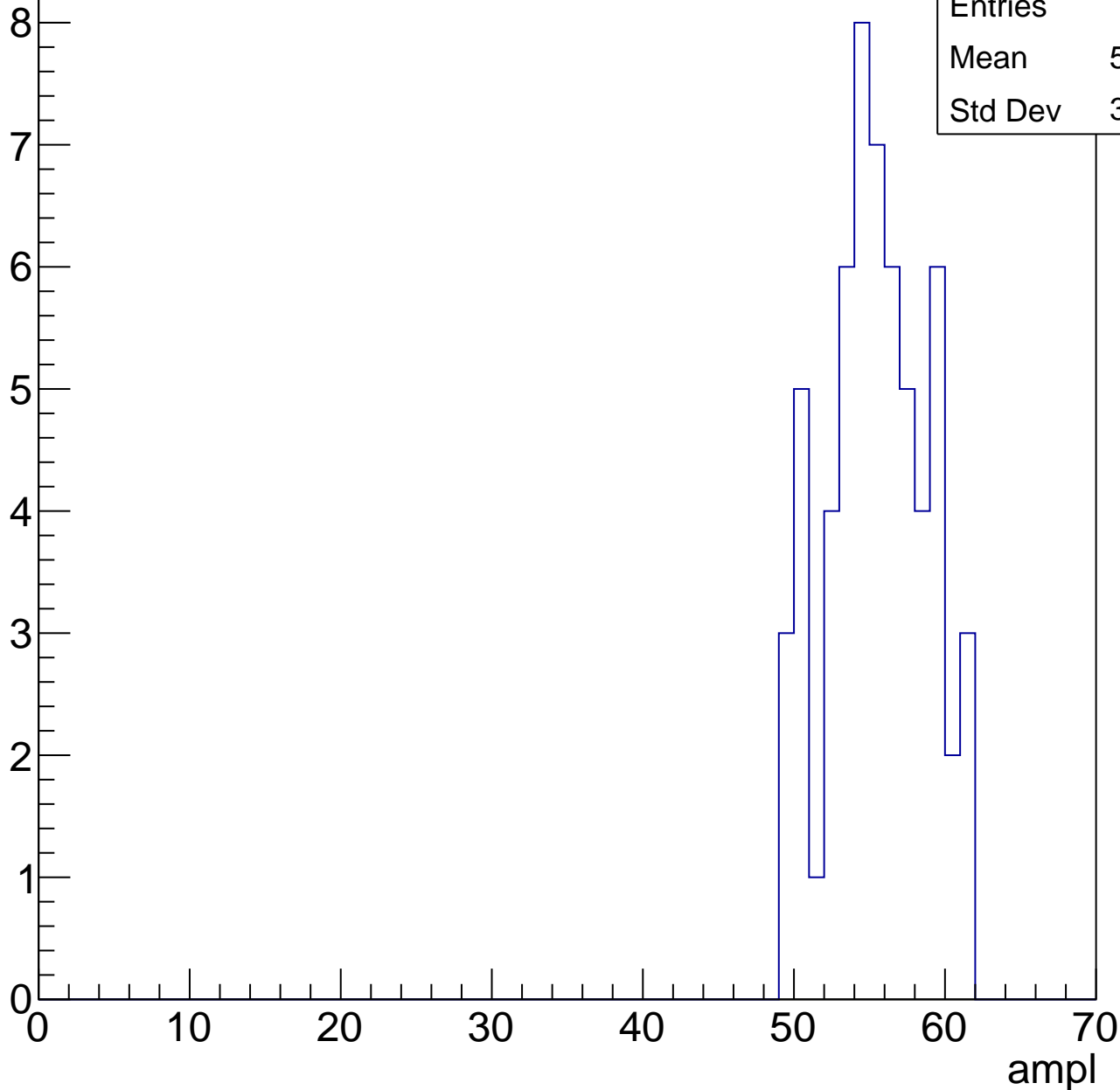


# B1L101S, U20-ch10, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	60
Mean	55.02
Std Dev	3.248

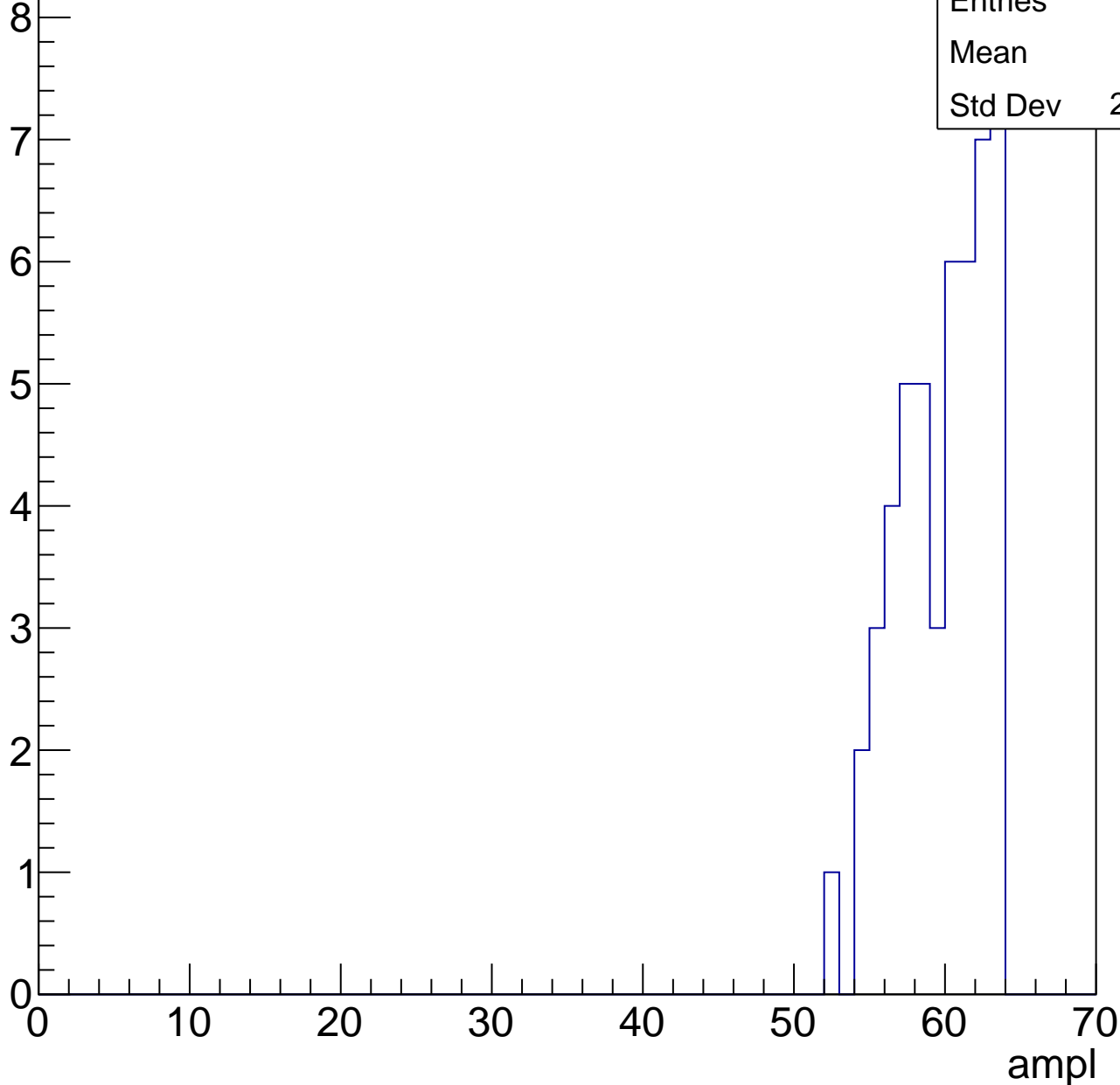


# B1L101S, U20-ch10, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	50
Mean	59.3
Std Dev	2.914



# B1L101S, U20-ch10, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

3

2.5

2

1.5

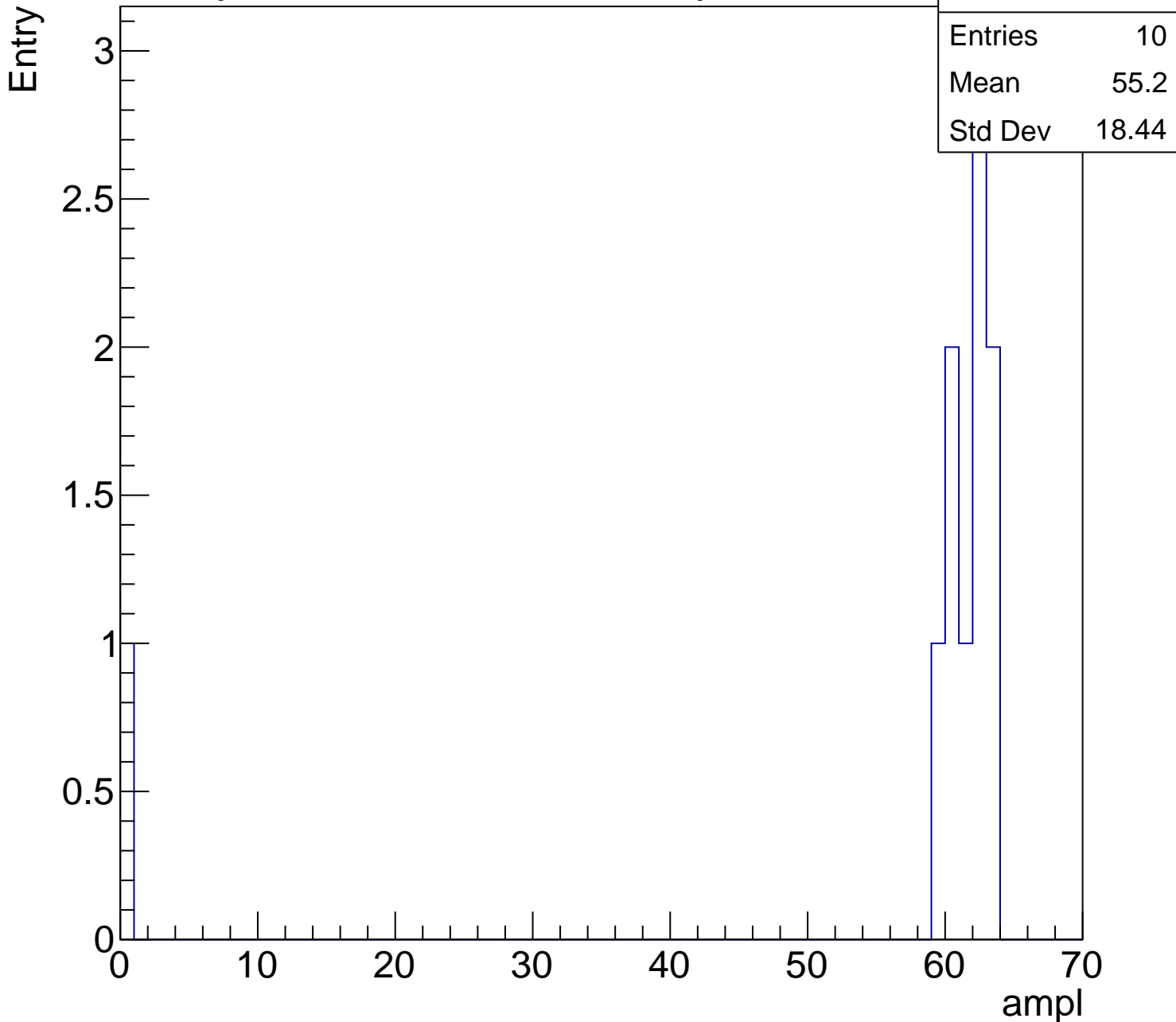
1

0.5

0

Entries	10
Mean	55.2
Std Dev	18.44

ampl





# B1L101S, U20-ch10, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U20-ch11, adc0

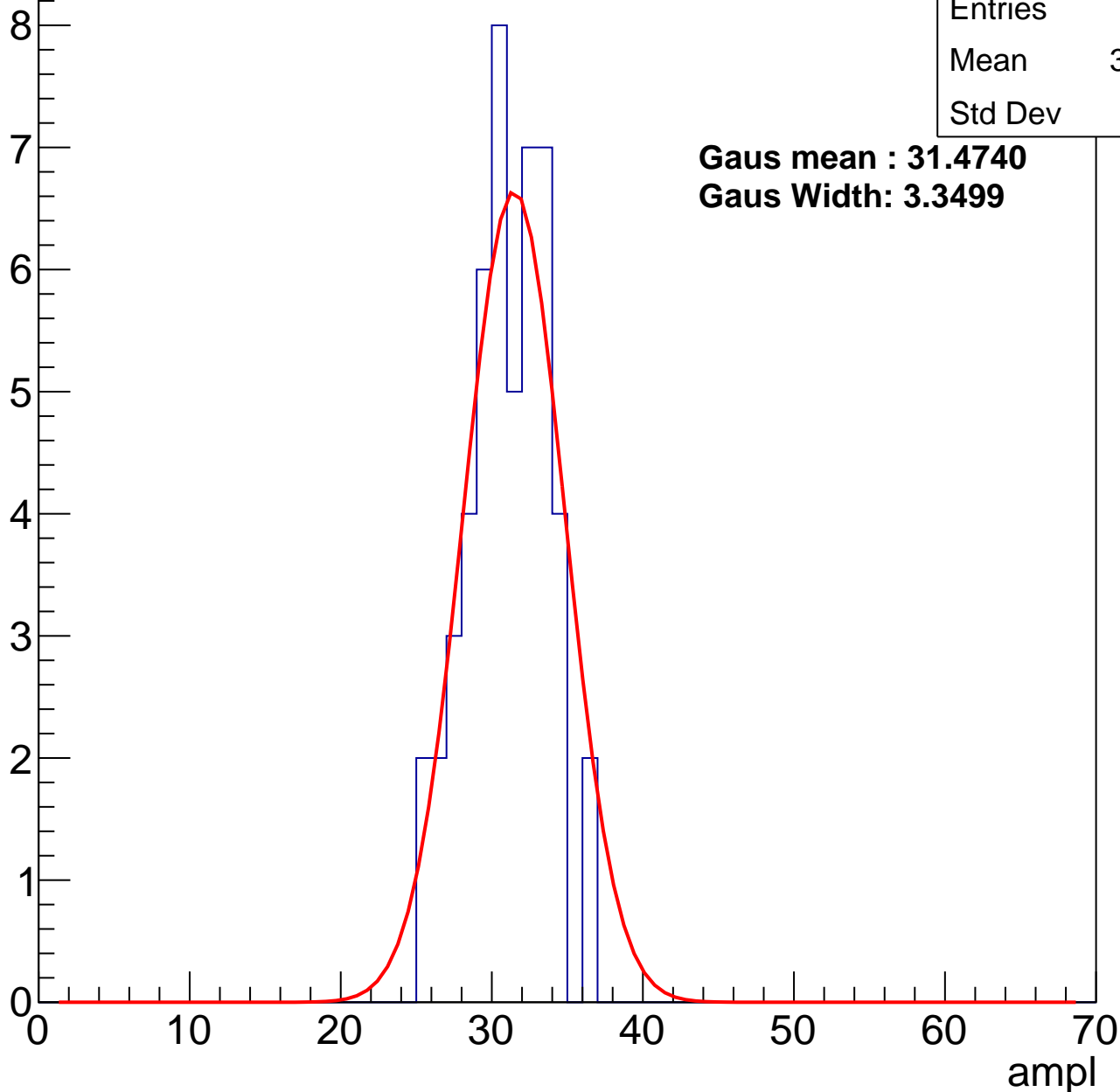
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	50
Mean	30.54
Std Dev	2.64

**Gaus mean : 31.4740**

**Gaus Width: 3.3499**



# B1L101S, U20-ch11, adc1

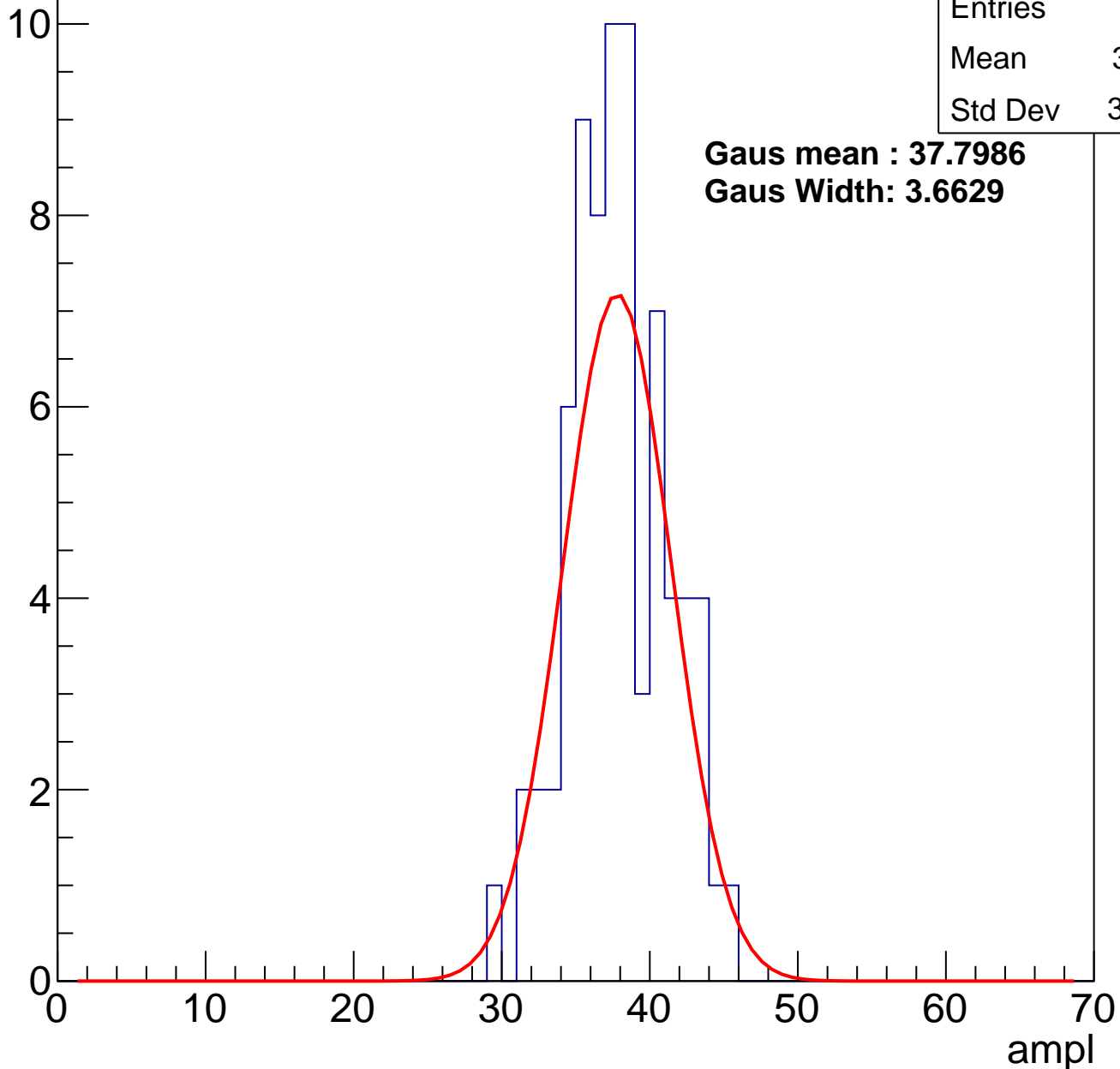
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	74
Mean	37.41
Std Dev	3.308

**Gaus mean : 37.7986**

**Gaus Width: 3.6629**

Entry



# B1L101S, U20-ch11, adc2

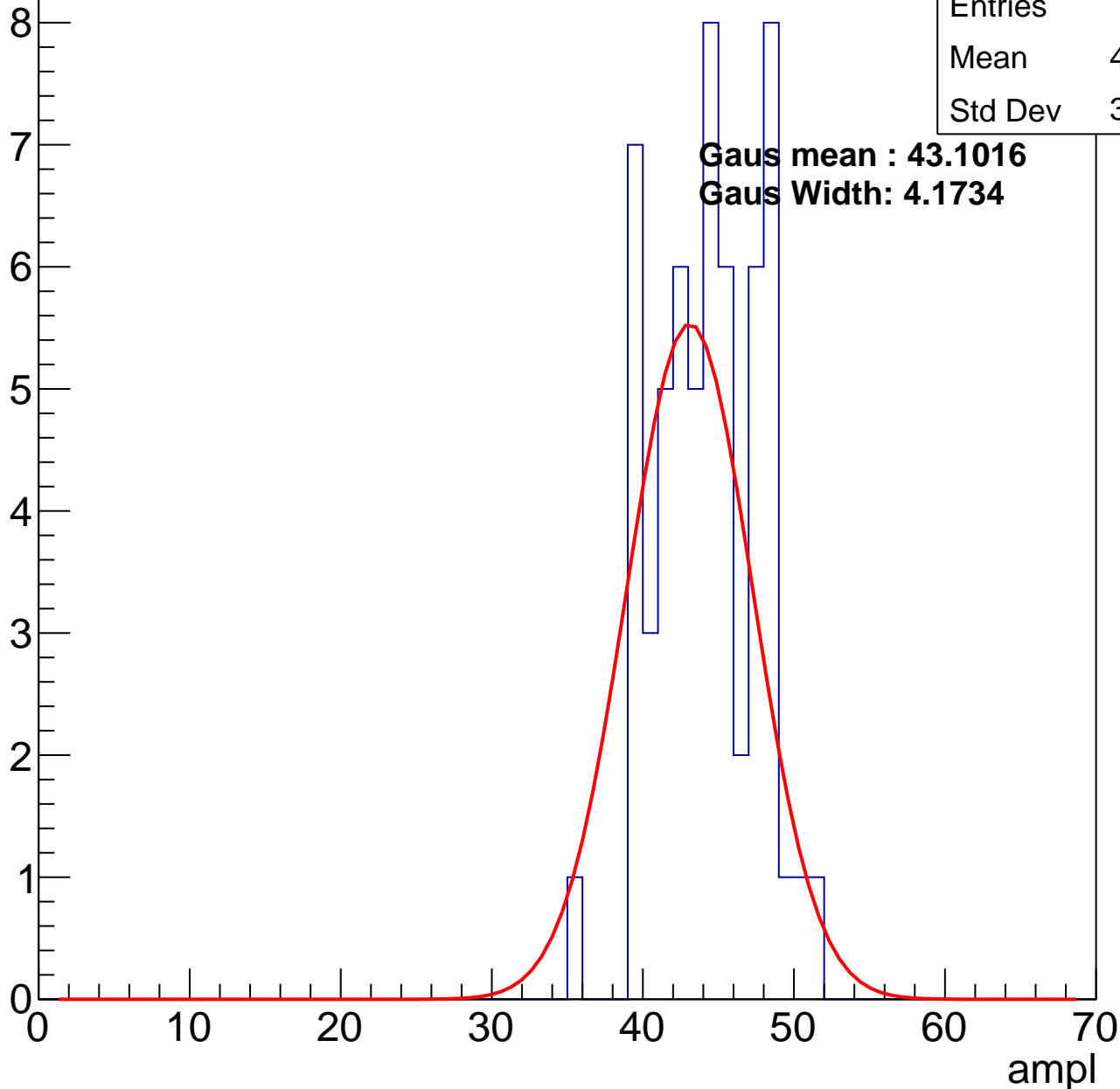
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	60
Mean	43.83
Std Dev	3.372

**Gaus mean : 43.1016**

**Gaus Width: 4.1734**

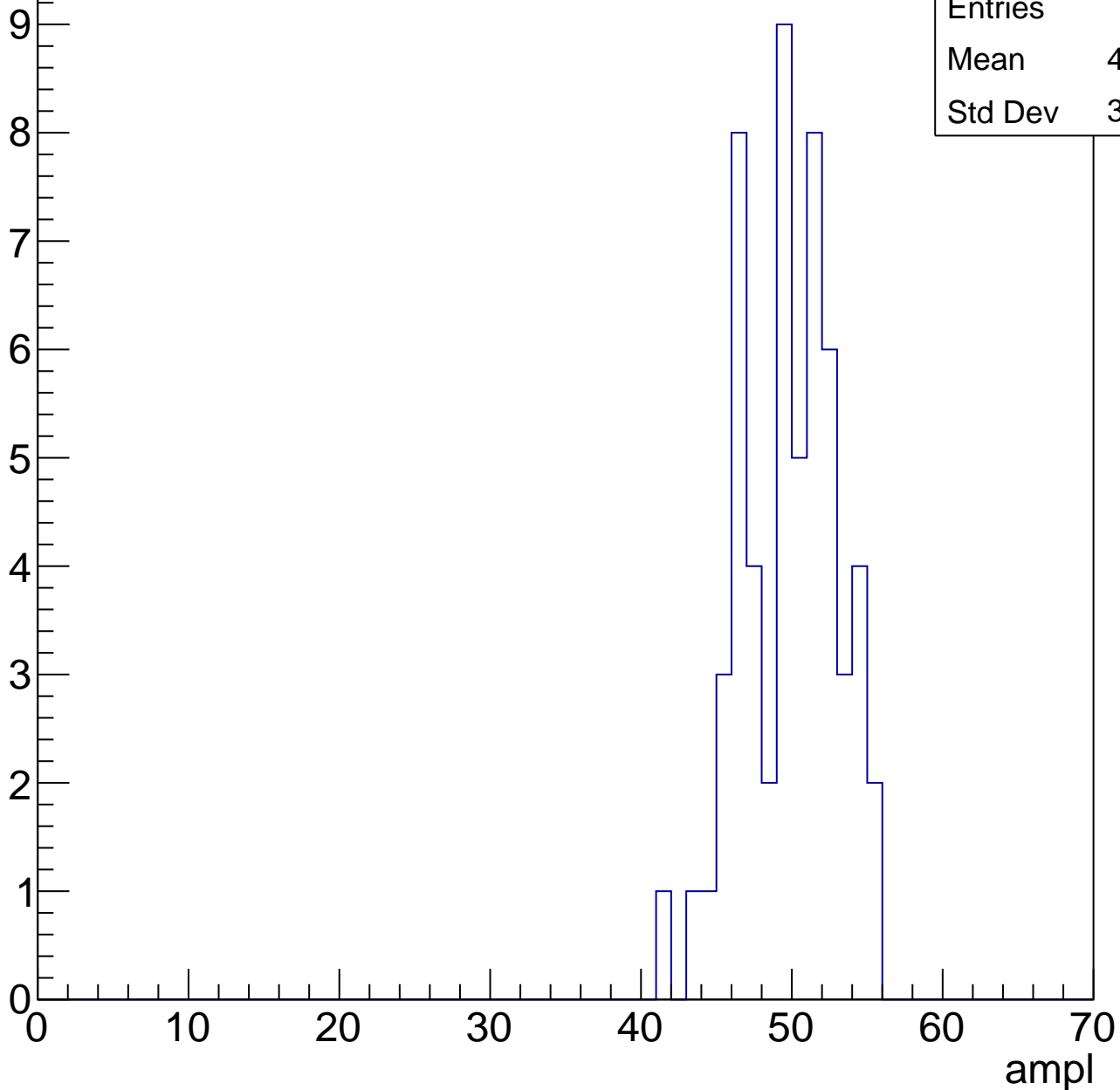


# B1L101S, U20-ch11, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	57
Mean	49.32
Std Dev	3.158



# B1L101S, U20-ch11, adc4

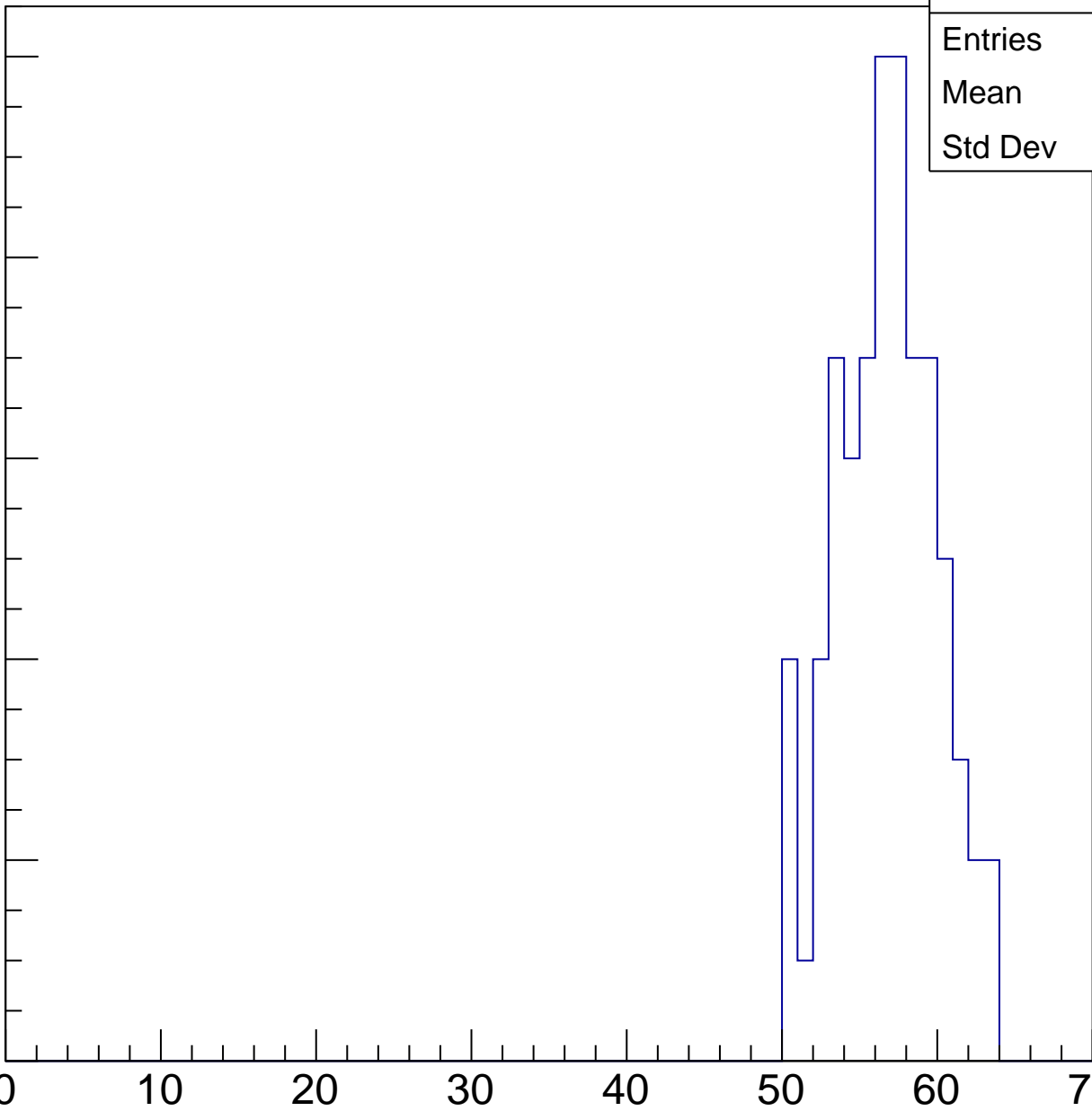
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	75
Mean	56.28
Std Dev	3.156

Entry

10  
8  
6  
4  
2  
0

ampl

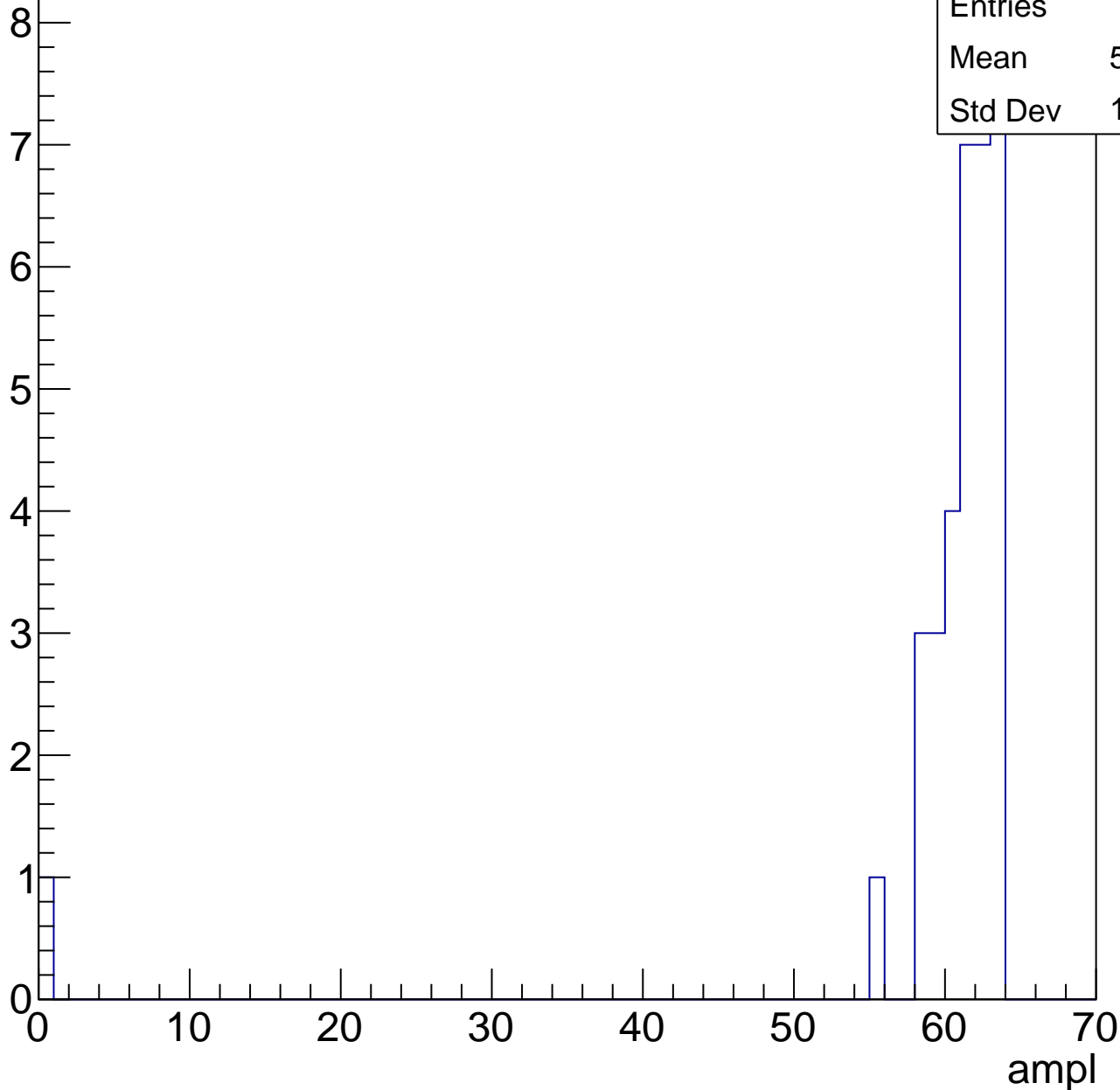


# B1L101S, U20-ch11, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	34
Mean	59.15
Std Dev	10.46



# B1L101S, U20-ch11, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

1

0.8

0.6

0.4

0.2

0

0

10

20

30

40

50

60

70

ampl

Entries

2

Mean

61

Std Dev

1



# B1L101S, U20-ch11, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	3
Mean	8.333
Std Dev	11.79

# B1L101S, U20-ch12, adc0

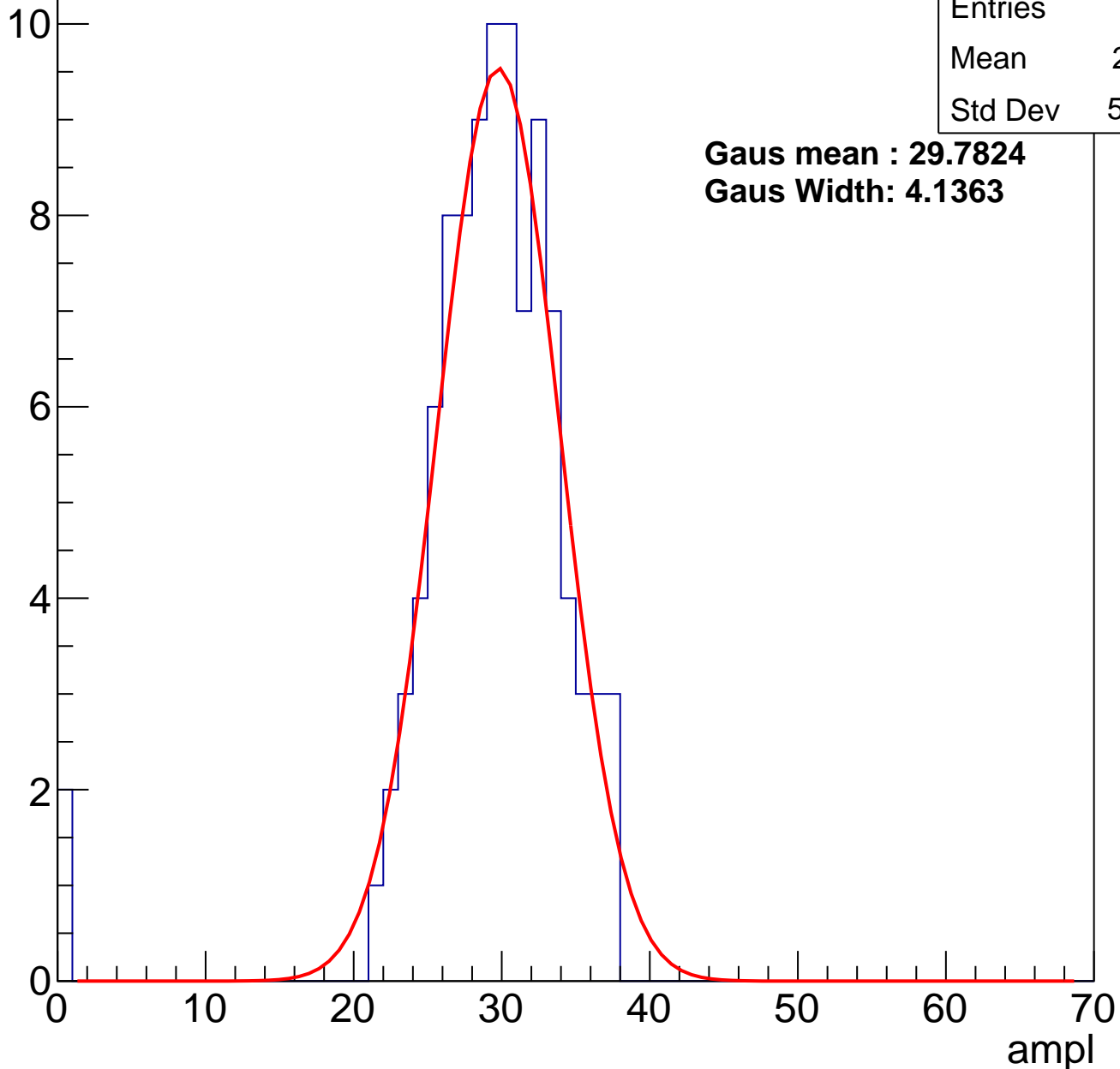
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	99
Mean	28.71
Std Dev	5.533

**Gaus mean : 29.7824**

**Gaus Width: 4.1363**

Entry



# B1L101S, U20-ch12, adc1

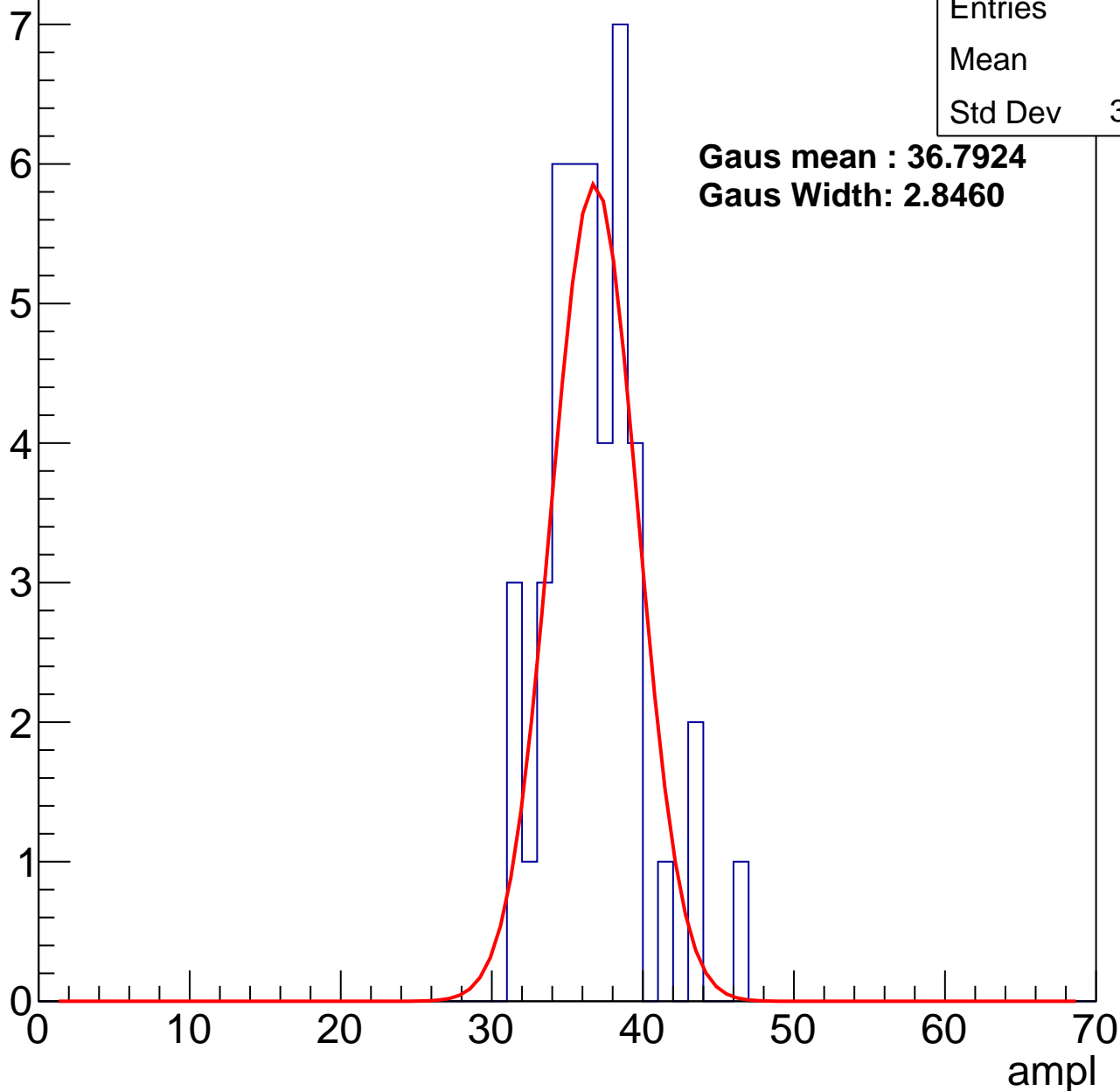
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	44
Mean	36.3
Std Dev	3.145

**Gaus mean : 36.7924**

**Gaus Width: 2.8460**



# B1L101S, U20-ch12, adc2

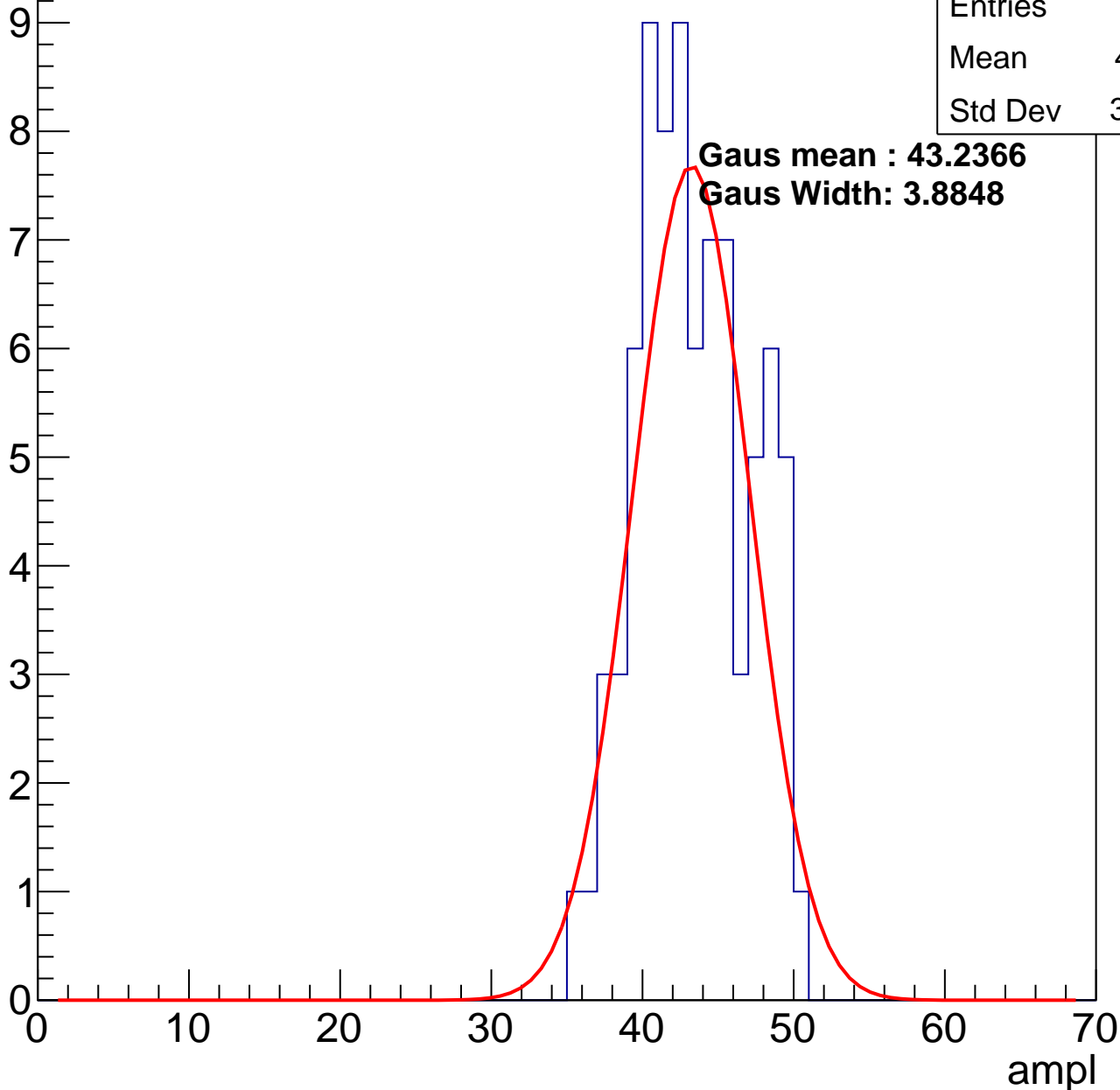
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	80
Mean	42.91
Std Dev	3.596

**Gaus mean : 43.2366**

**Gaus Width: 3.8848**

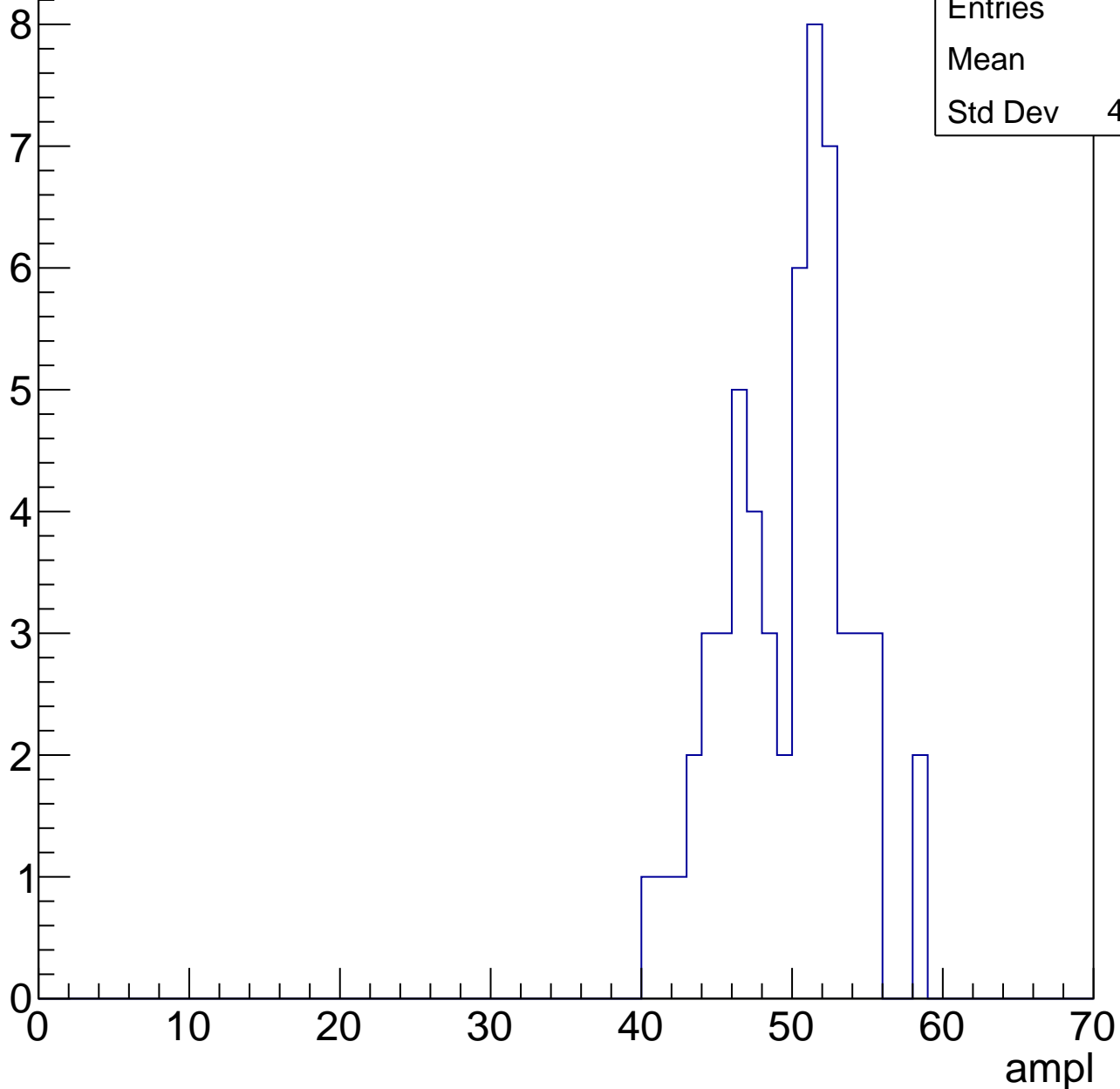


# B1L101S, U20-ch12, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	57
Mean	49.3
Std Dev	4.065

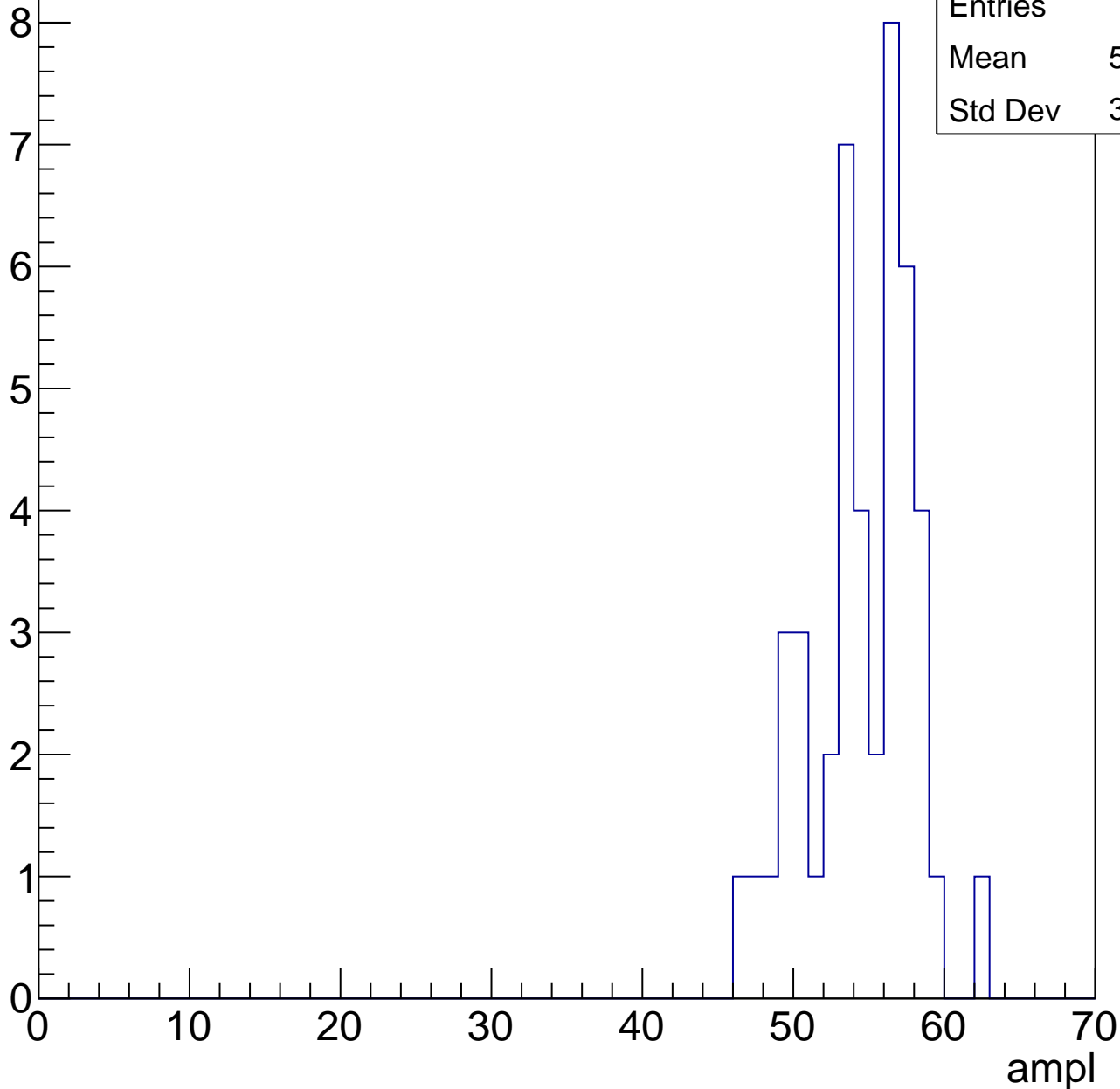


# B1L101S, U20-ch12, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	45
Mean	54.07
Std Dev	3.454

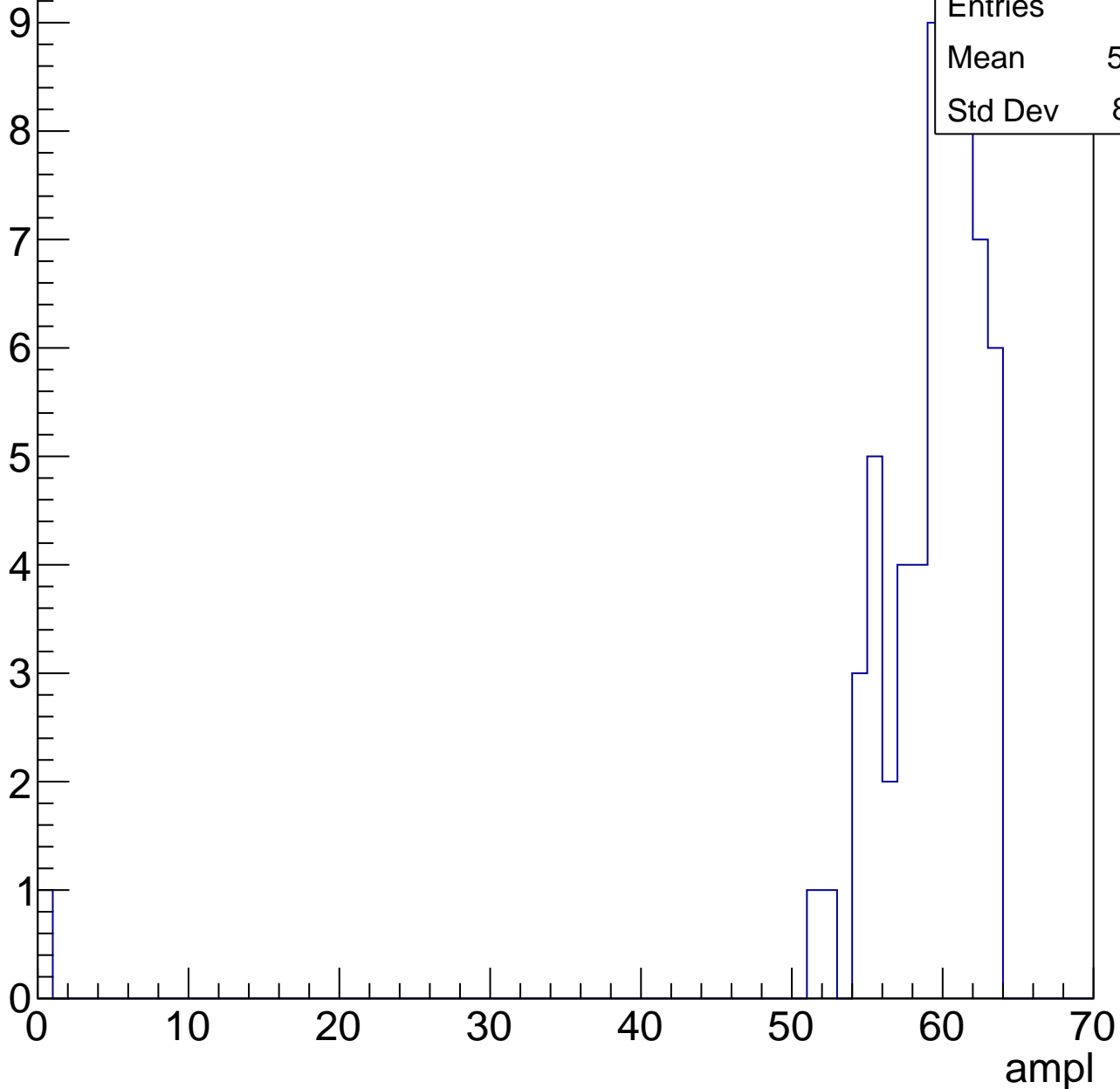


# B1L101S, U20-ch12, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

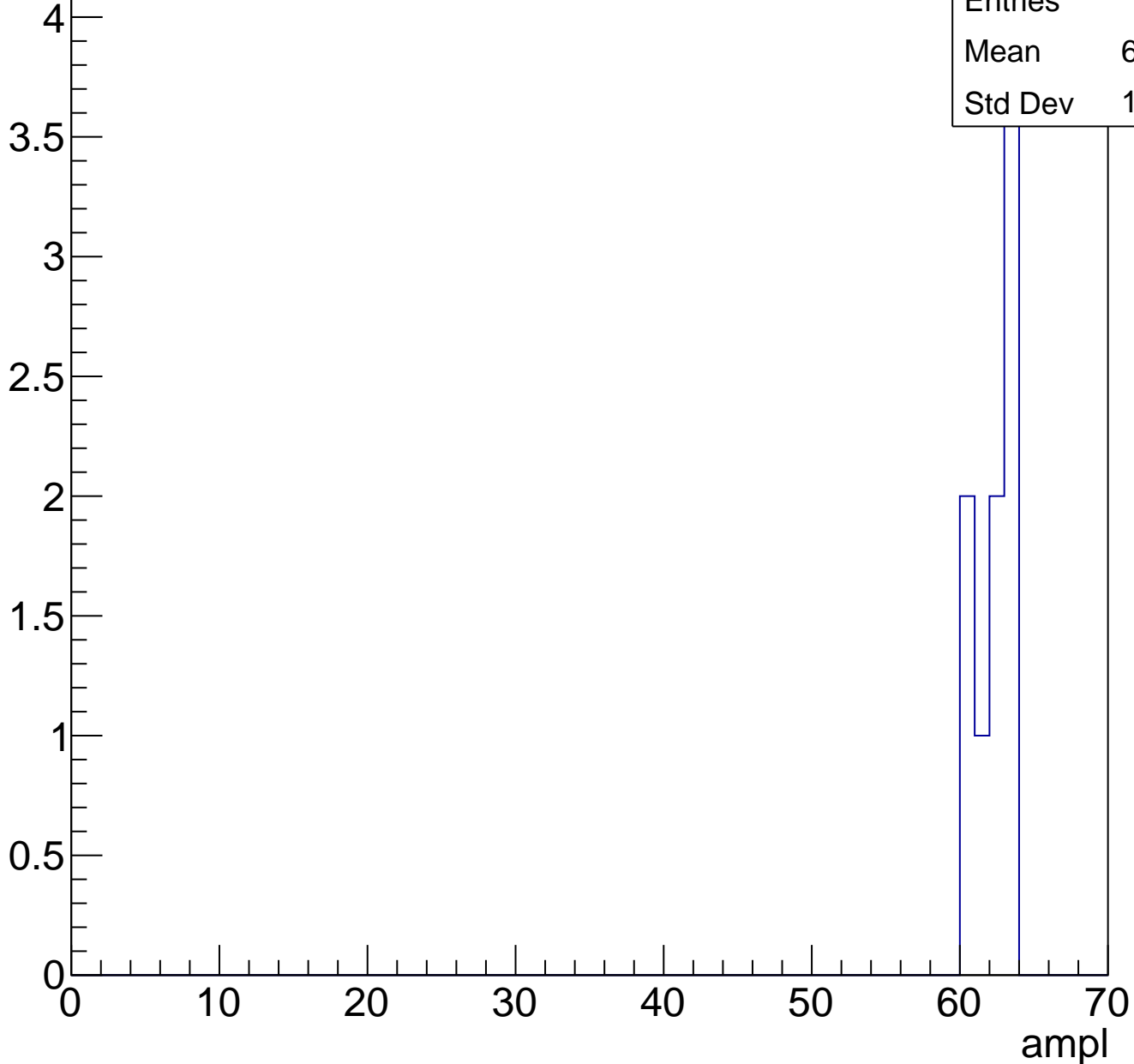
Entries	60
Mean	58.07
Std Dev	8.101



# B1L101S, U20-ch12, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U20-ch12, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L101S, U20-ch13, adc0

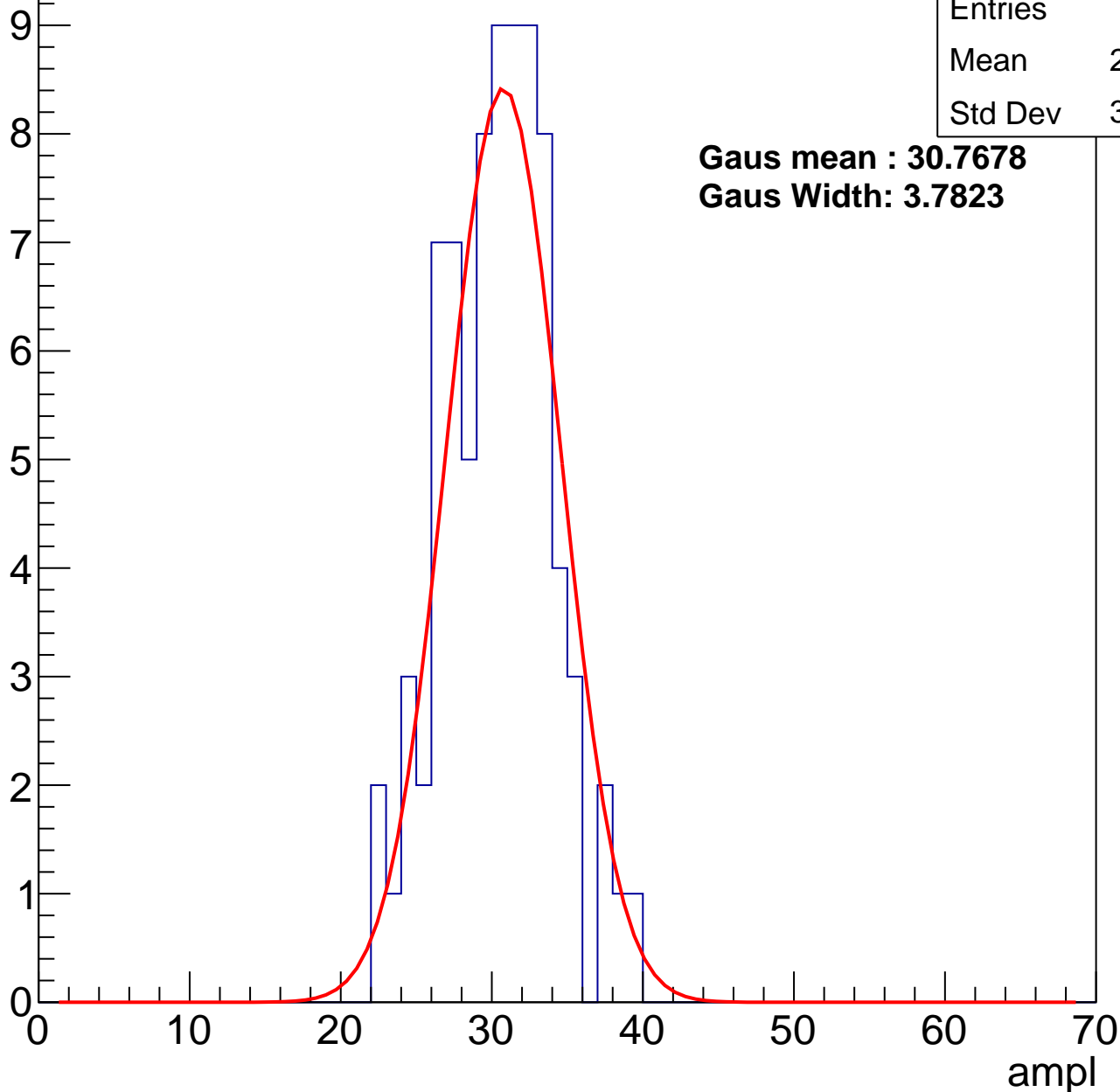
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	81
Mean	29.94
Std Dev	3.578

**Gaus mean : 30.7678**

**Gaus Width: 3.7823**



# B1L101S, U20-ch13, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	67
Mean	37.91
Std Dev	3.231

**Gaus mean : 38.0875**

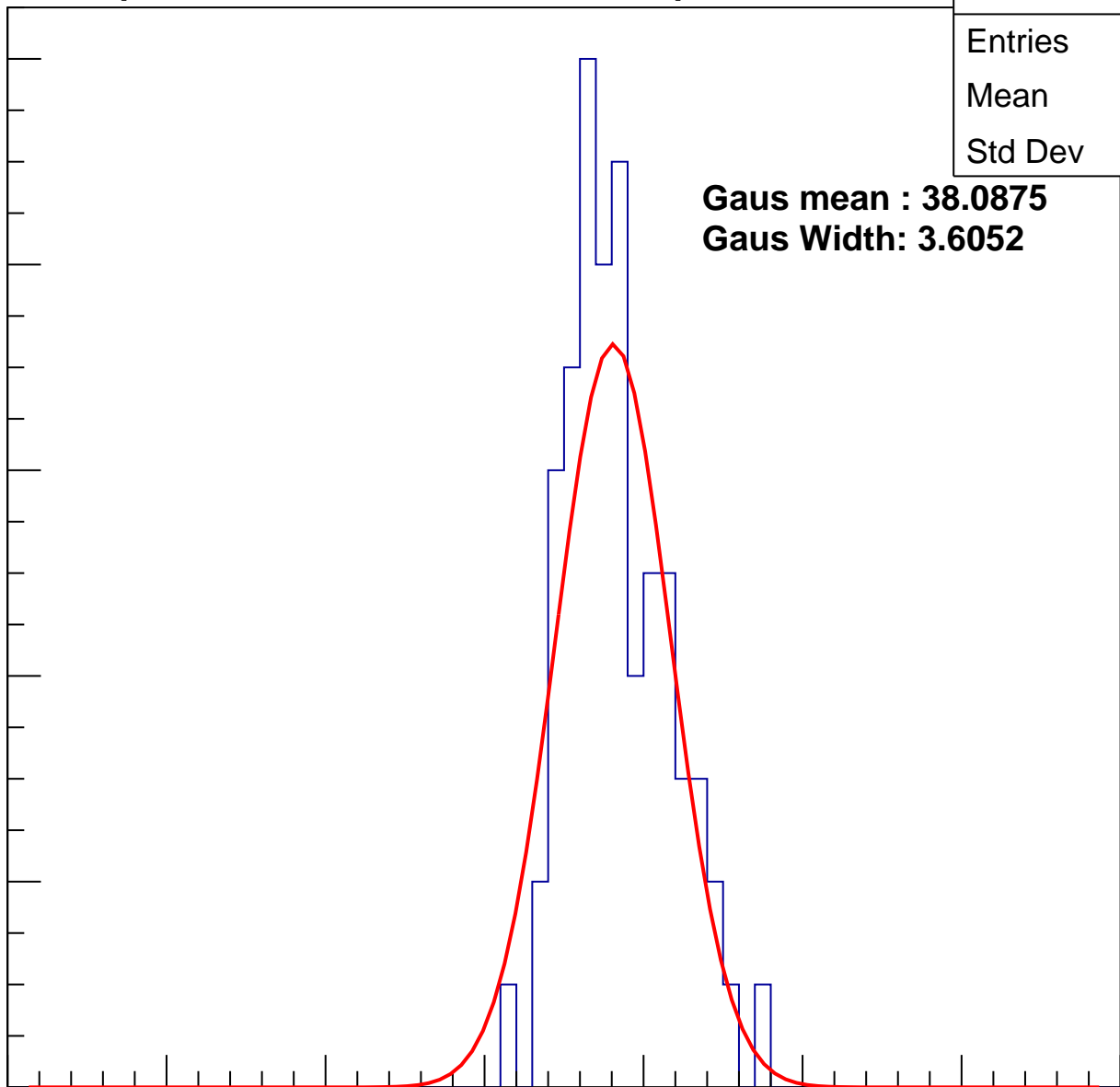
**Gaus Width: 3.6052**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U20-ch13, adc2

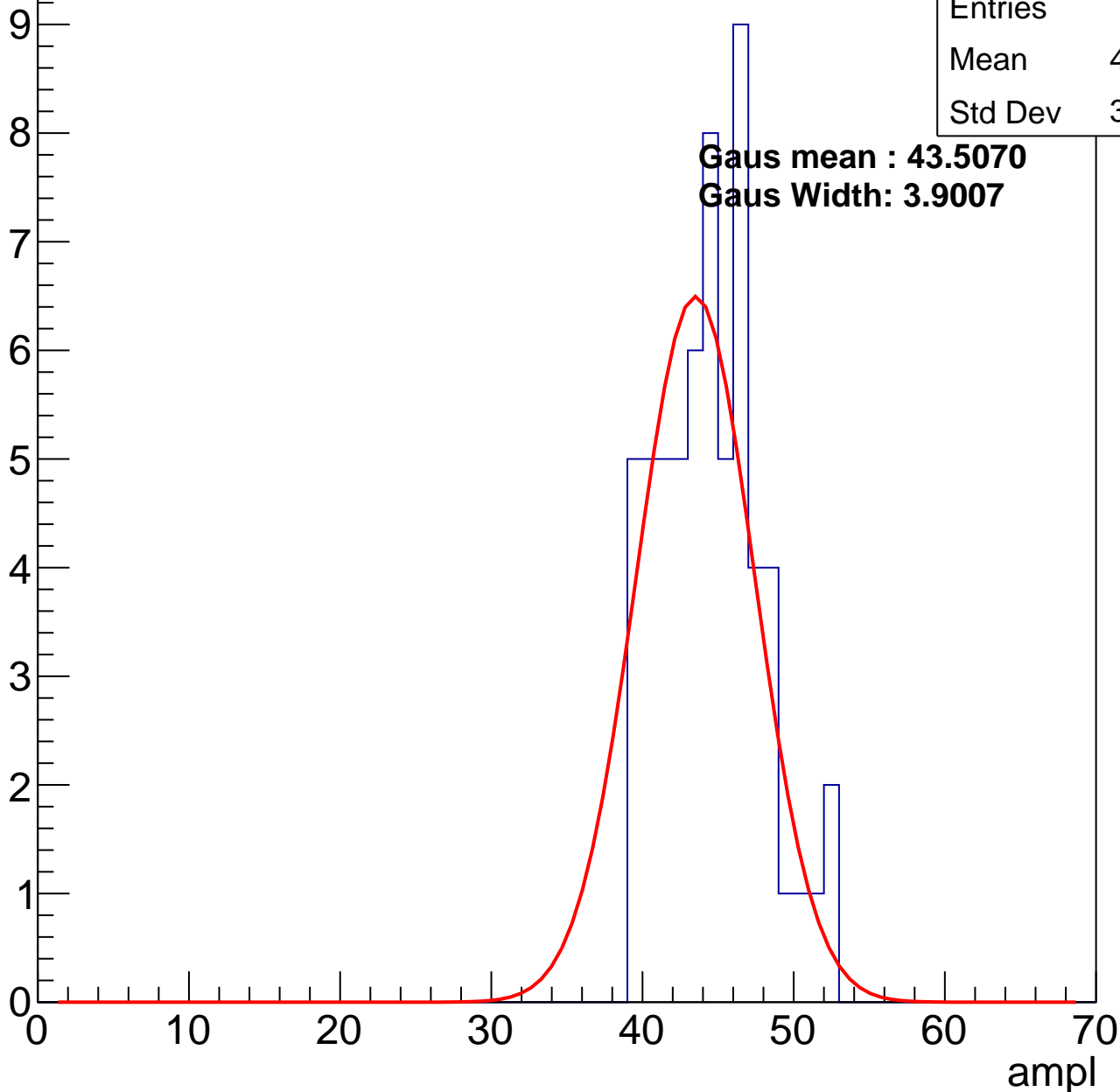
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	44.15
Std Dev	3.274

**Gaus mean : 43.5070**

**Gaus Width: 3.9007**

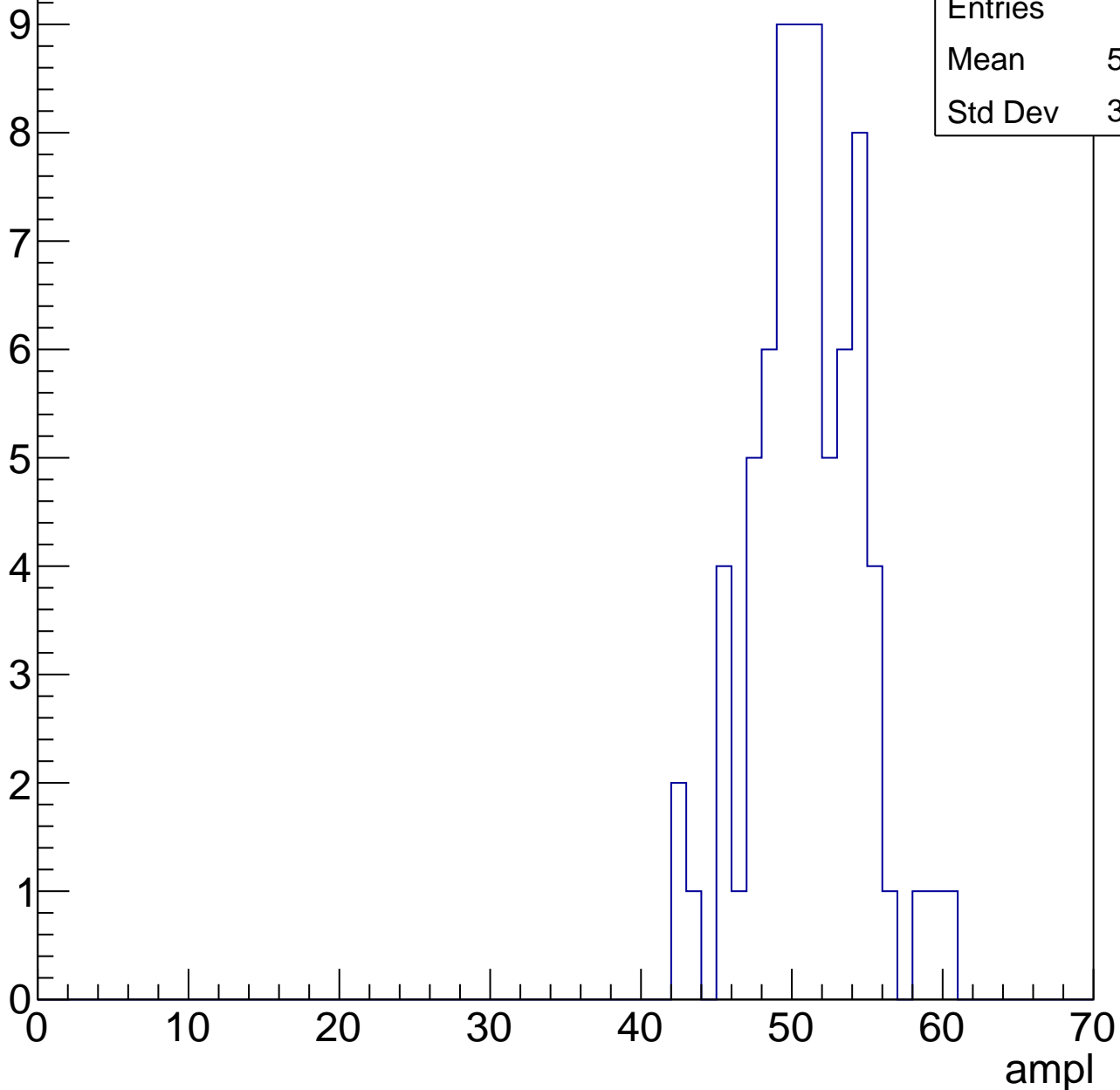


# B1L101S, U20-ch13, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	73
Mean	50.53
Std Dev	3.593

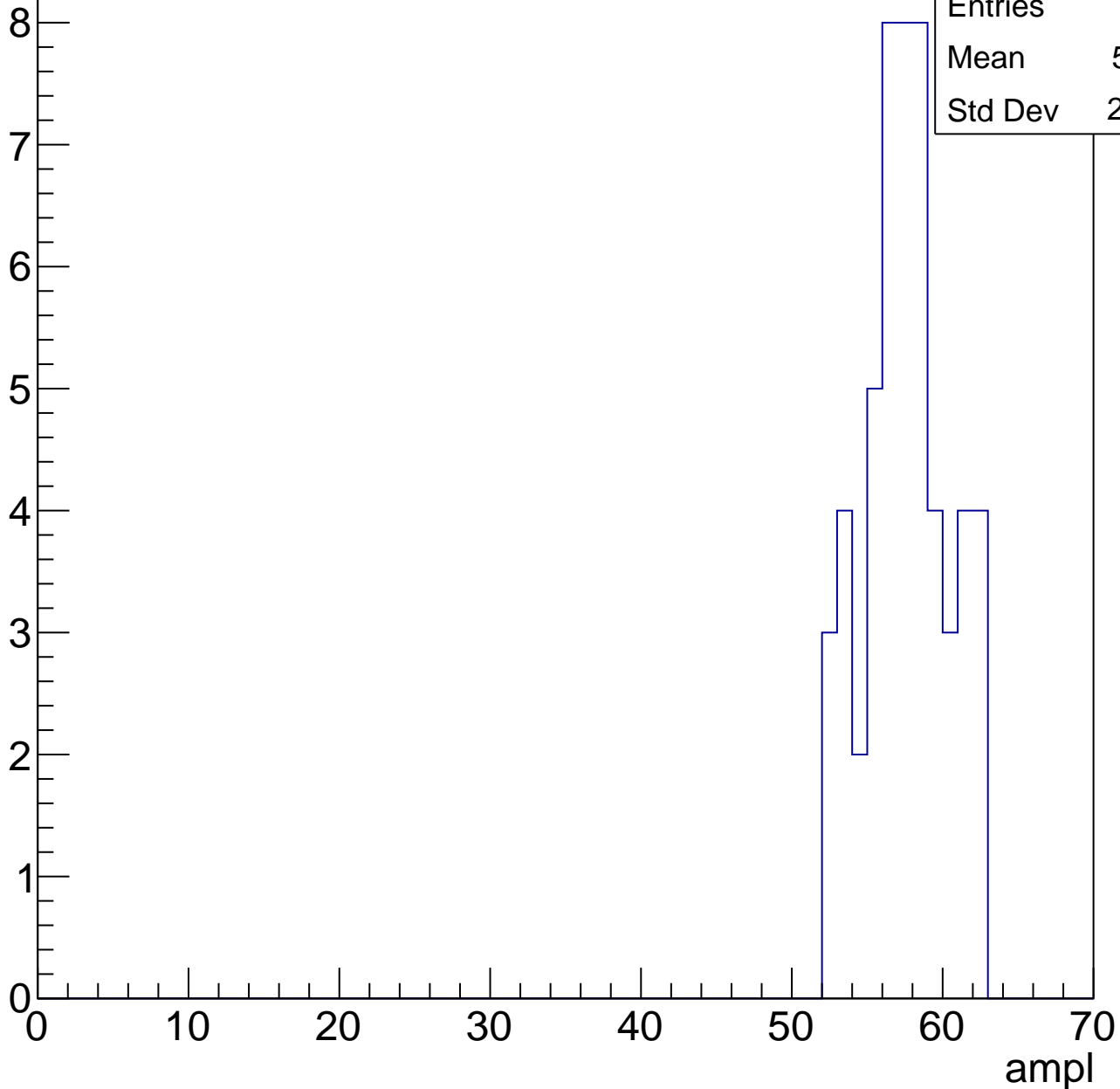


# B1L101S, U20-ch13, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

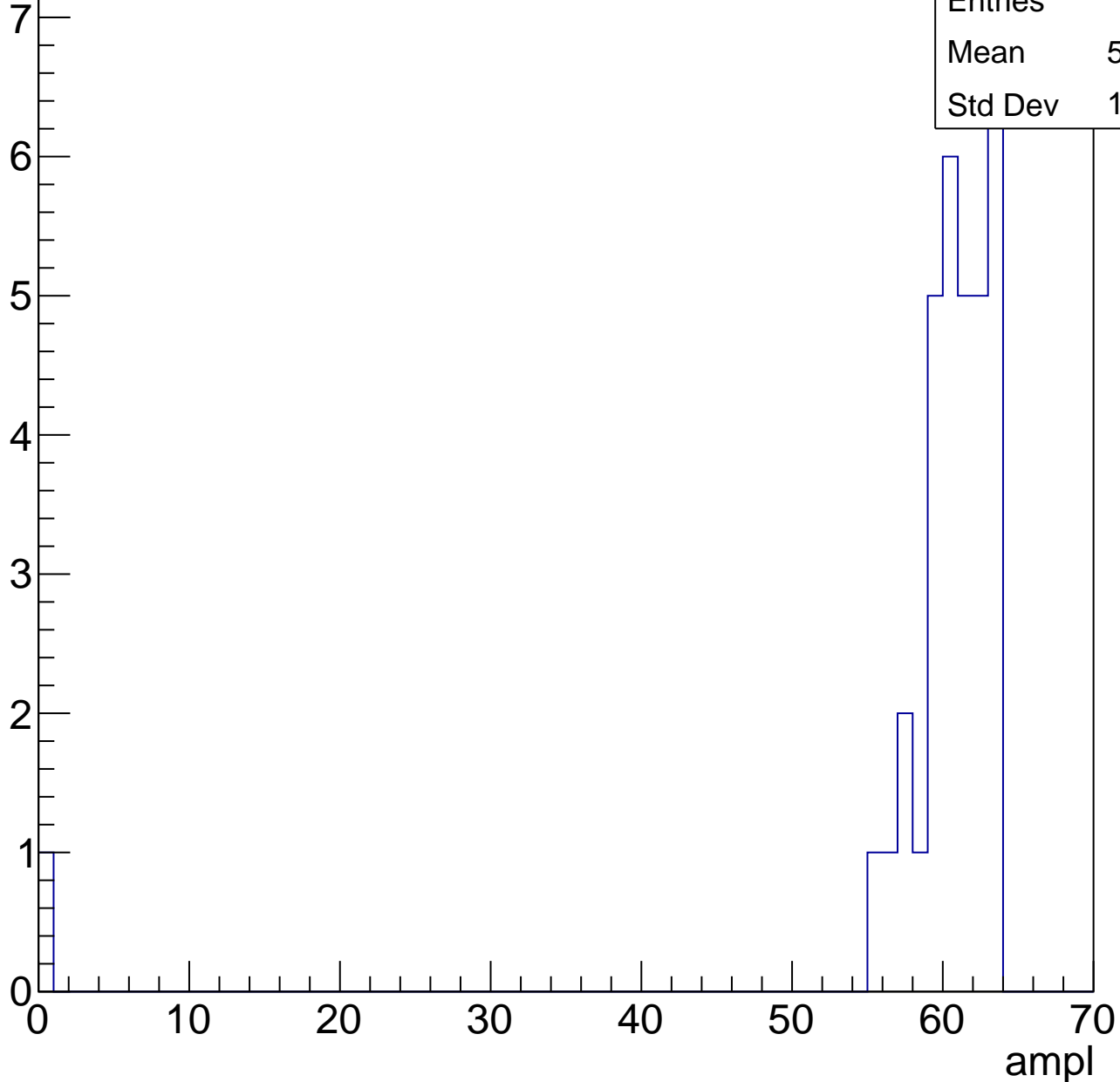
Entries	53
Mean	57.11
Std Dev	2.745



# B1L101S, U20-ch13, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U20-ch13, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U20-ch13, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	2
Mean	10.5
Std Dev	10.5

# B1L101S, U20-ch14, adc0

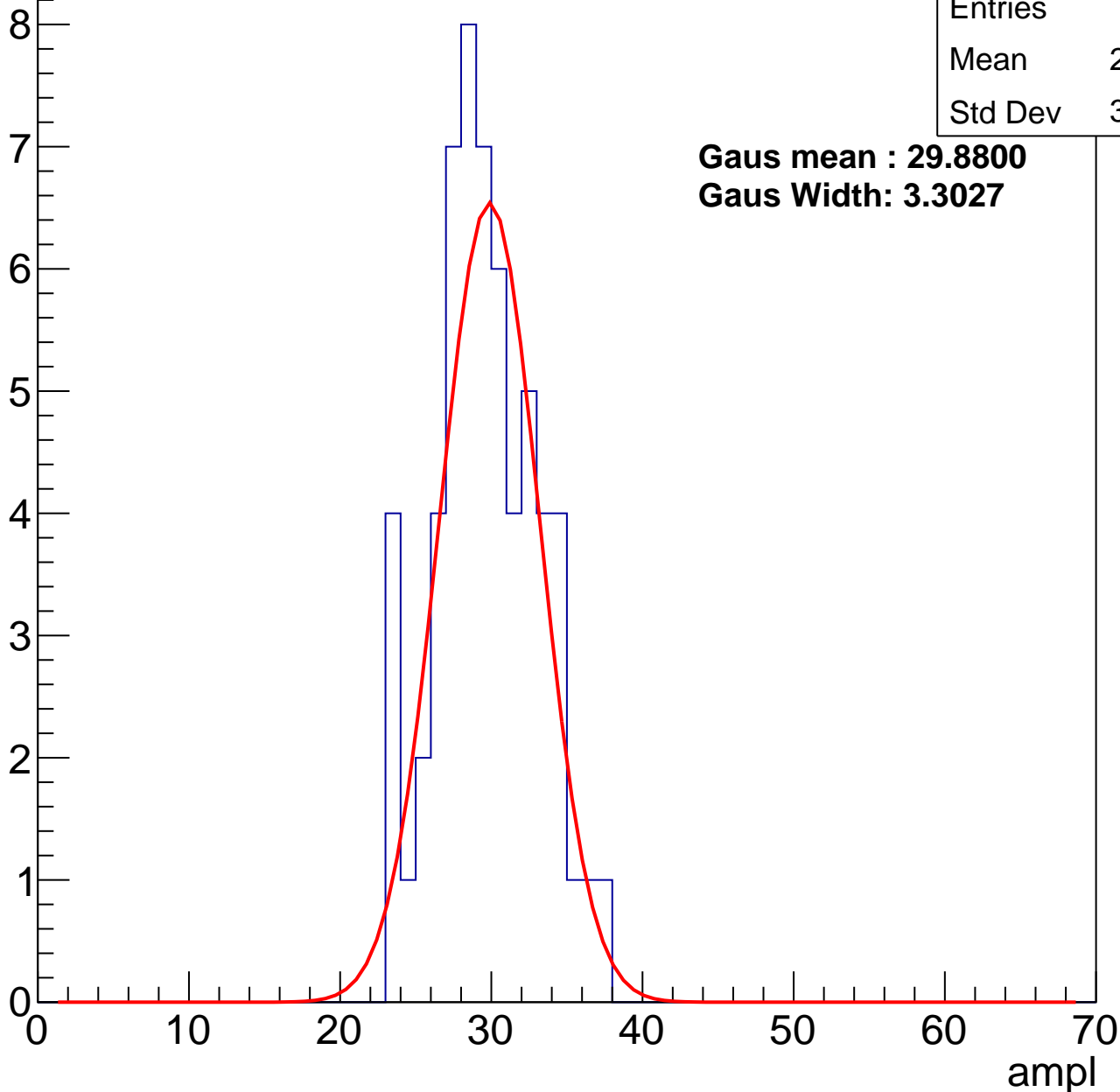
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	59
Mean	29.25
Std Dev	3.317

**Gaus mean : 29.8800**

**Gaus Width: 3.3027**



# B1L101S, U20-ch14, adc1

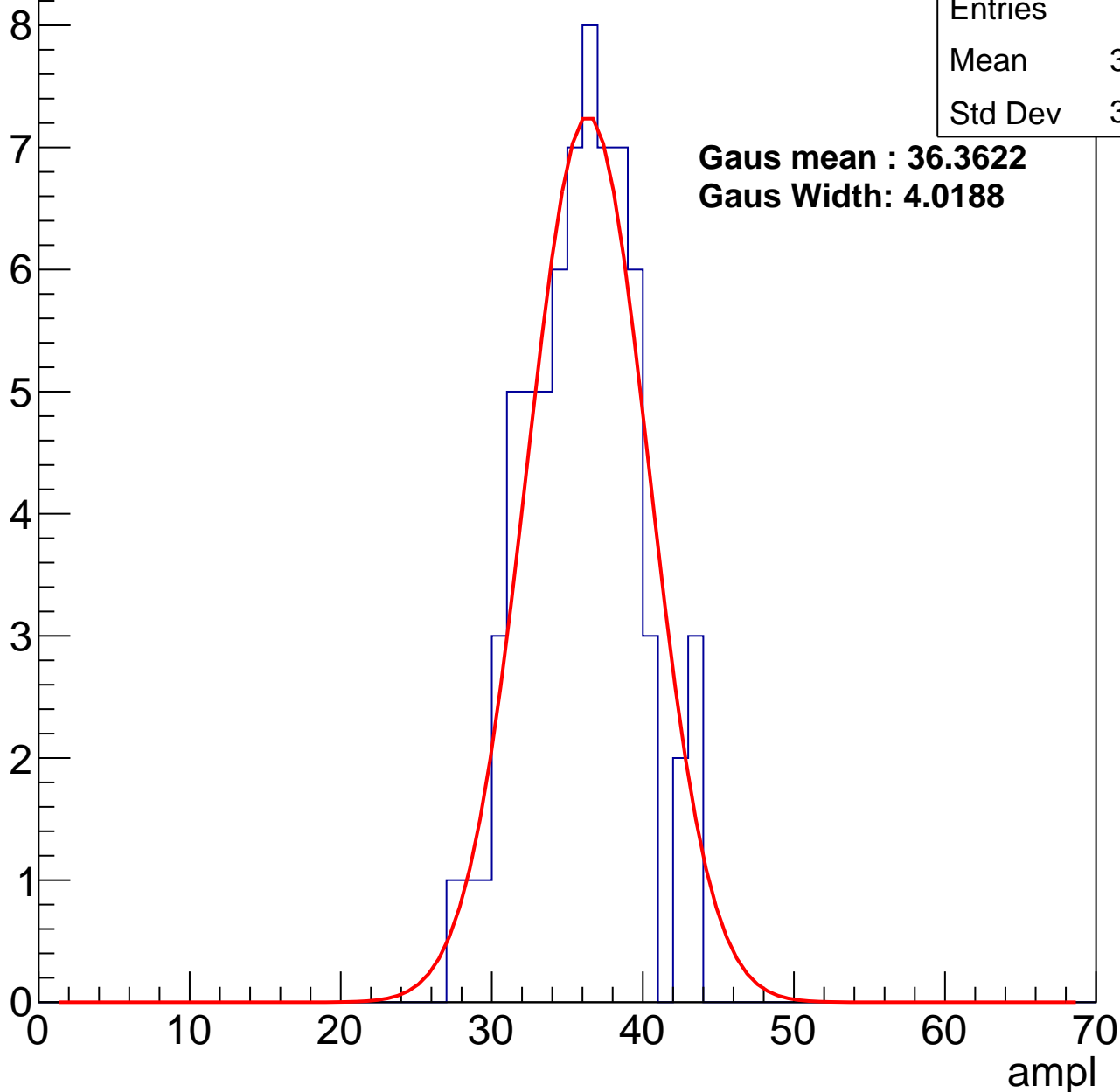
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	35.47
Std Dev	3.624

**Gaus mean : 36.3622**

**Gaus Width: 4.0188**



# B1L101S, U20-ch14, adc2

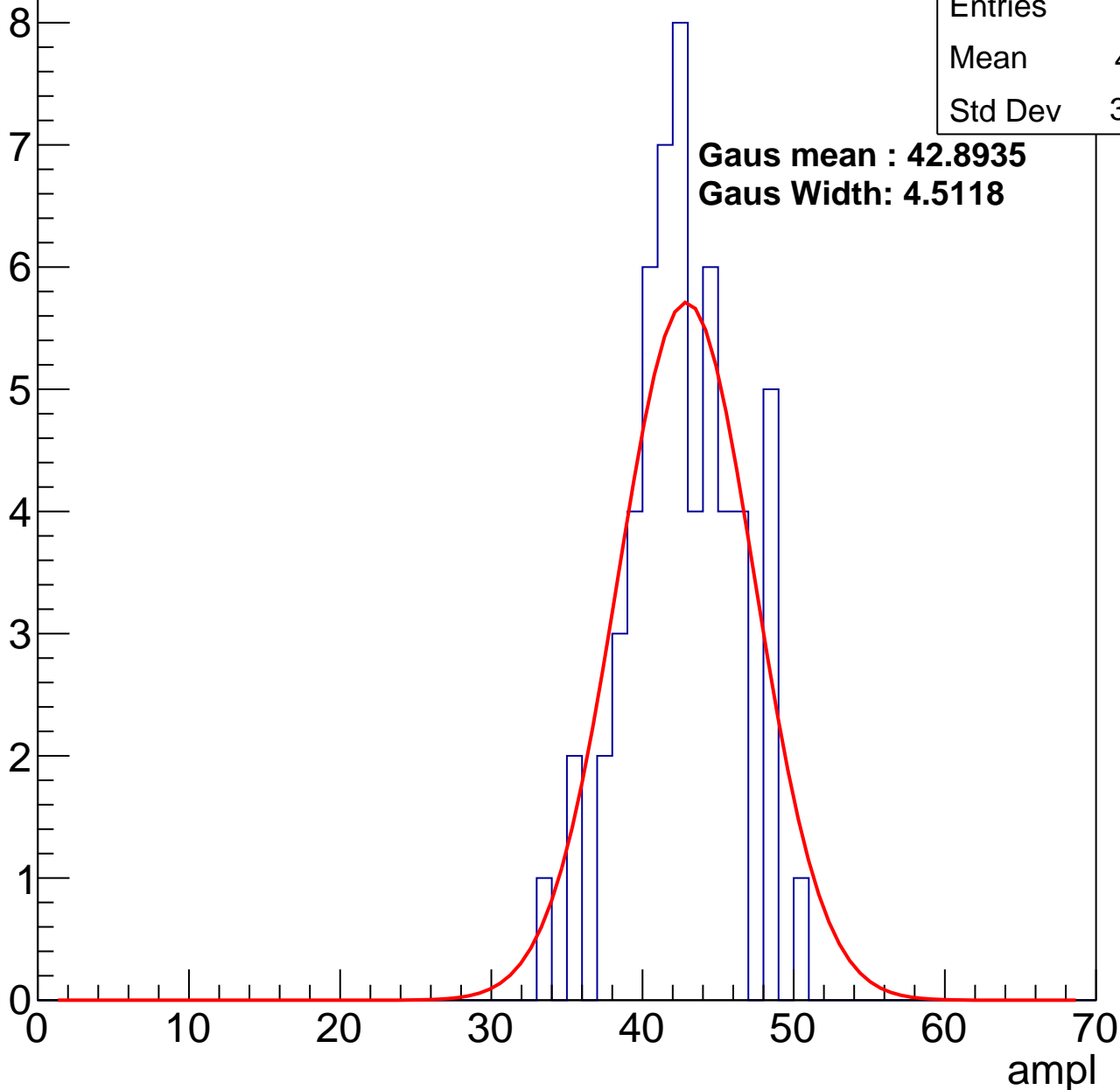
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	57
Mean	42.11
Std Dev	3.543

**Gaus mean : 42.8935**

**Gaus Width: 4.5118**

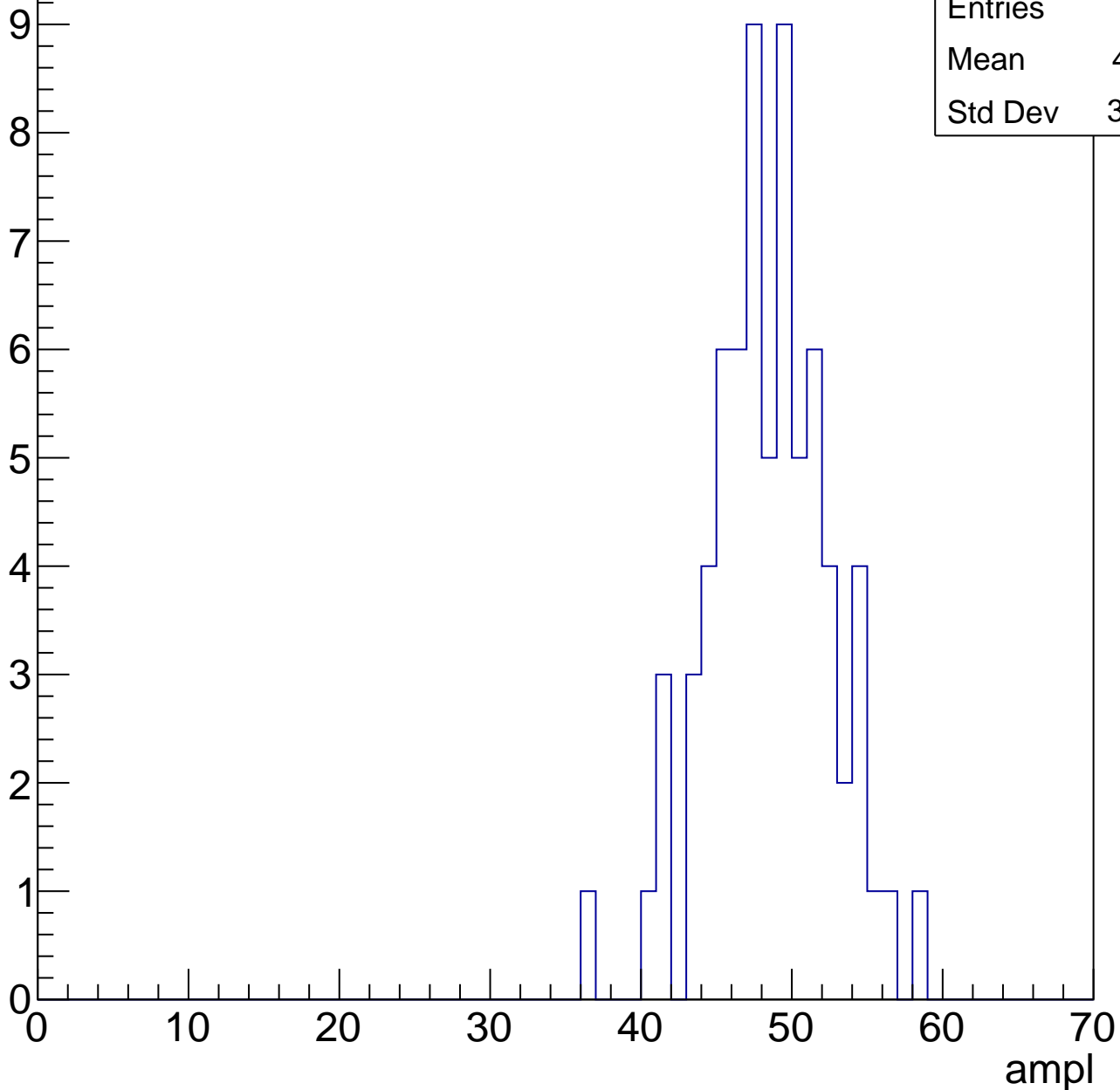


# B1L101S, U20-ch14, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

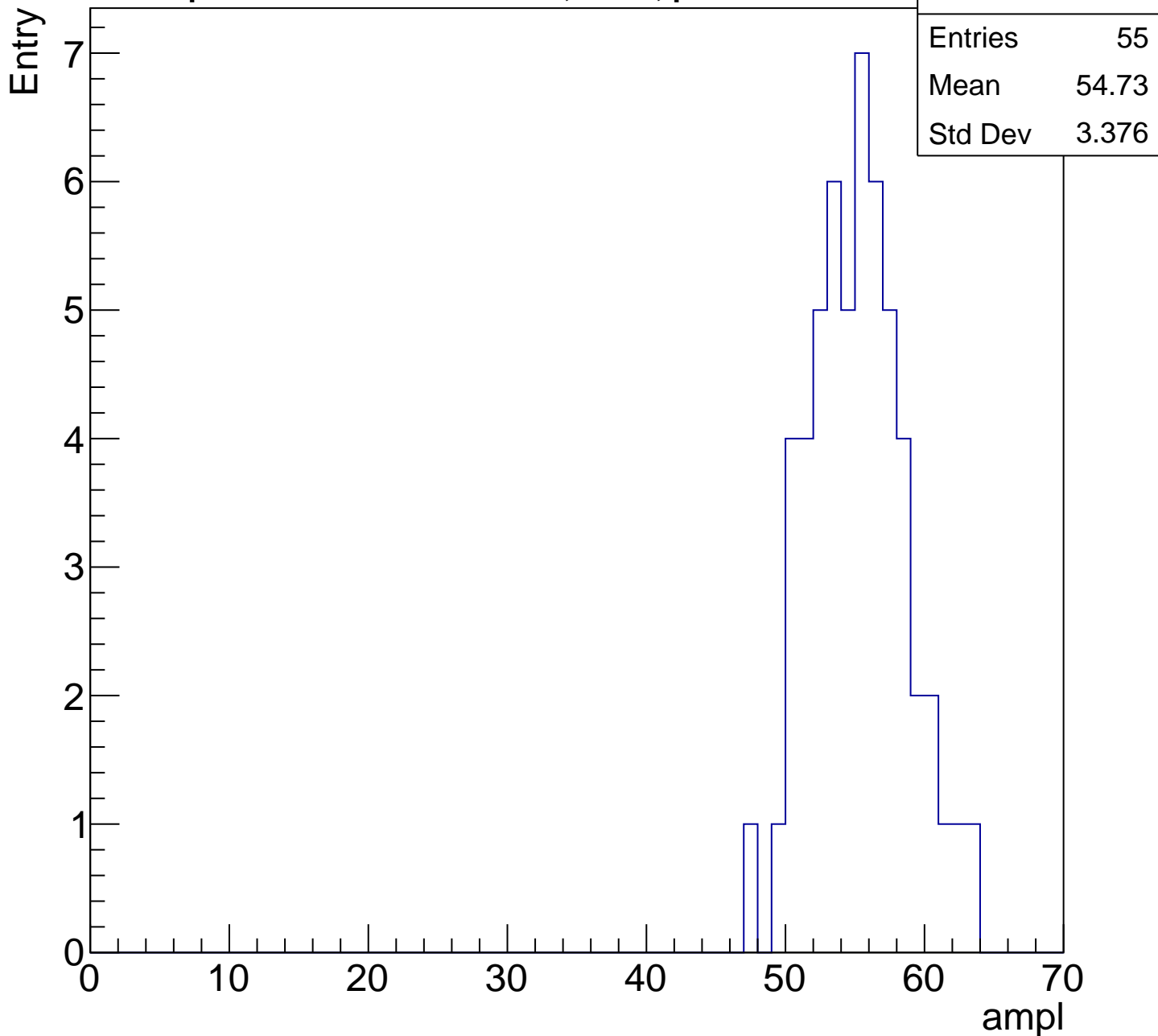
Entry

Entries	71
Mean	48.01
Std Dev	3.998



# B1L101S, U20-ch14, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U20-ch14, adc5

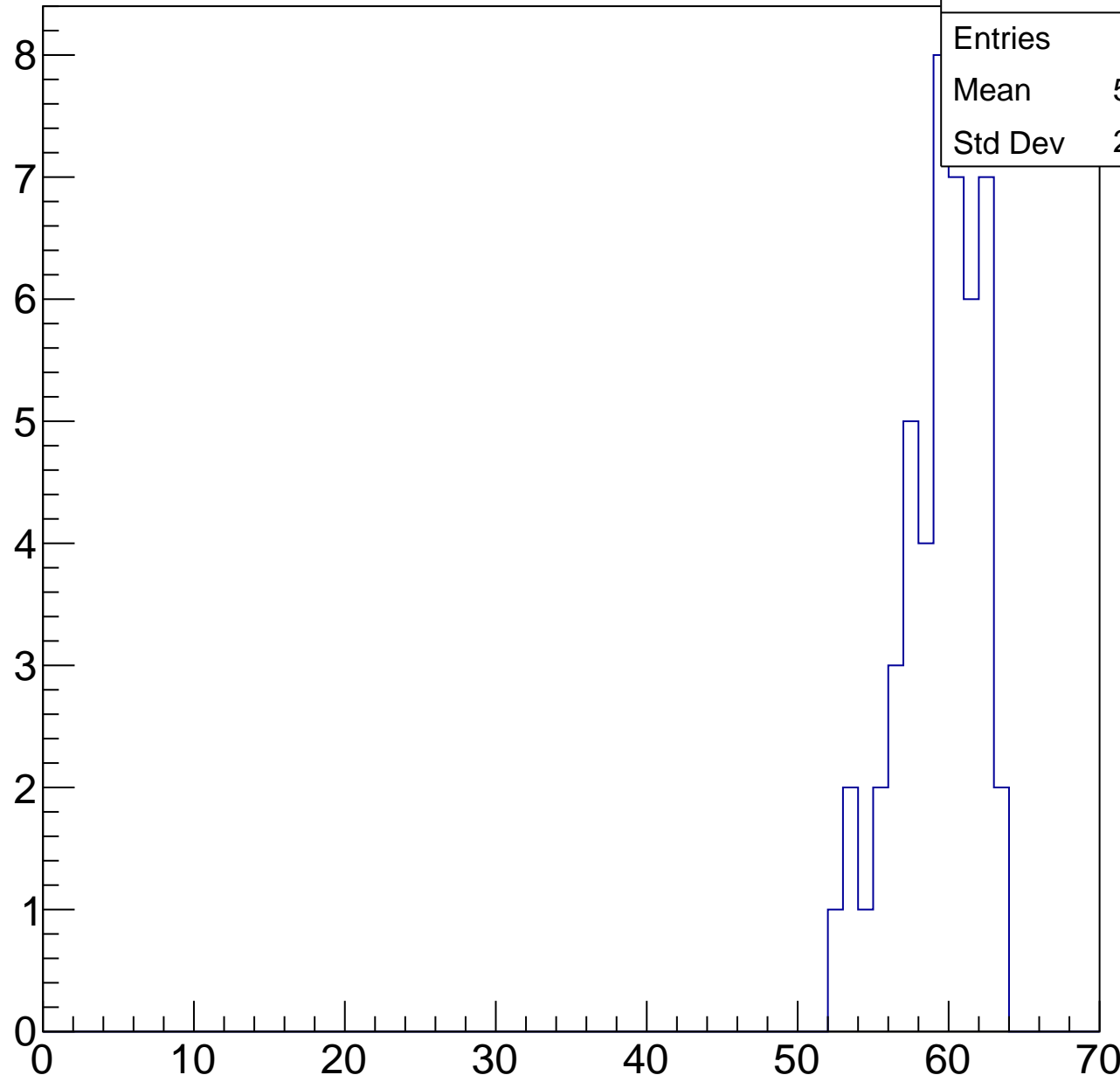
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	48
Mean	58.85
Std Dev	2.716

ampl

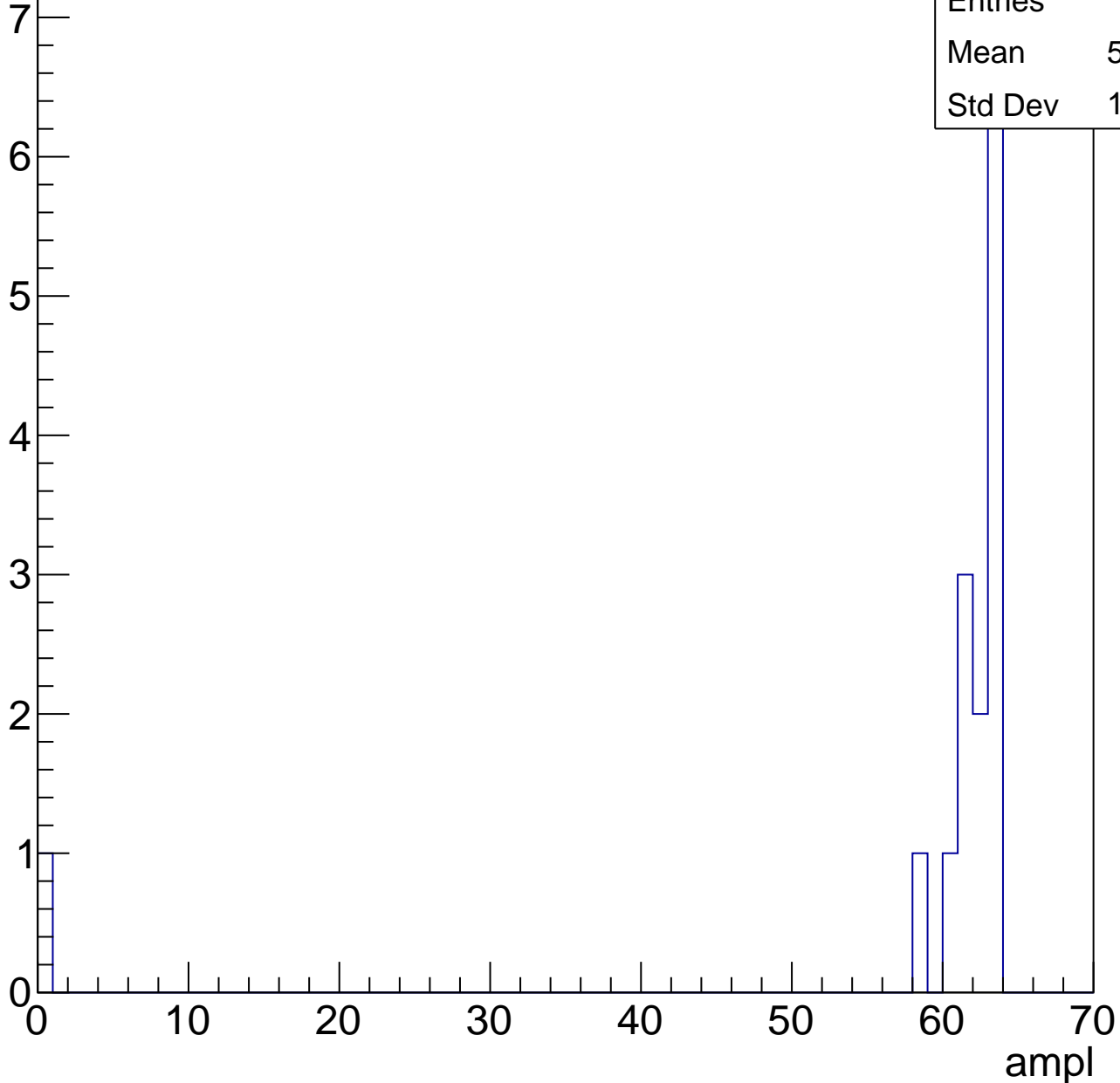


# B1L101S, U20-ch14, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	15
Mean	57.73
Std Dev	15.49





# B1L101S, U20-ch14, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	2
Mean	11
Std Dev	11

# B1L101S, U20-ch15, adc0

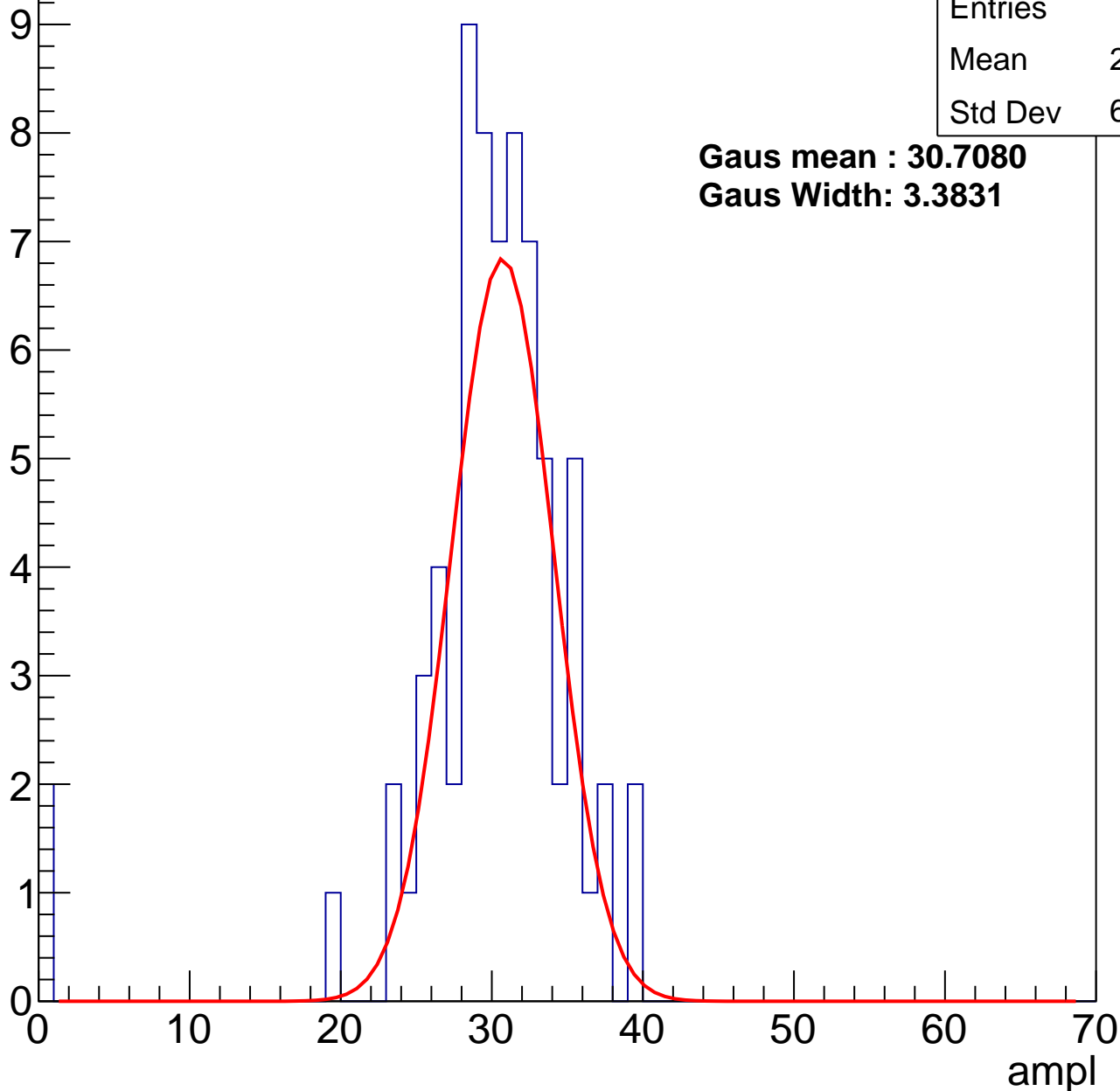
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	71
Mean	29.35
Std Dev	6.235

**Gaus mean : 30.7080**

**Gaus Width: 3.3831**



# B1L101S, U20-ch15, adc1

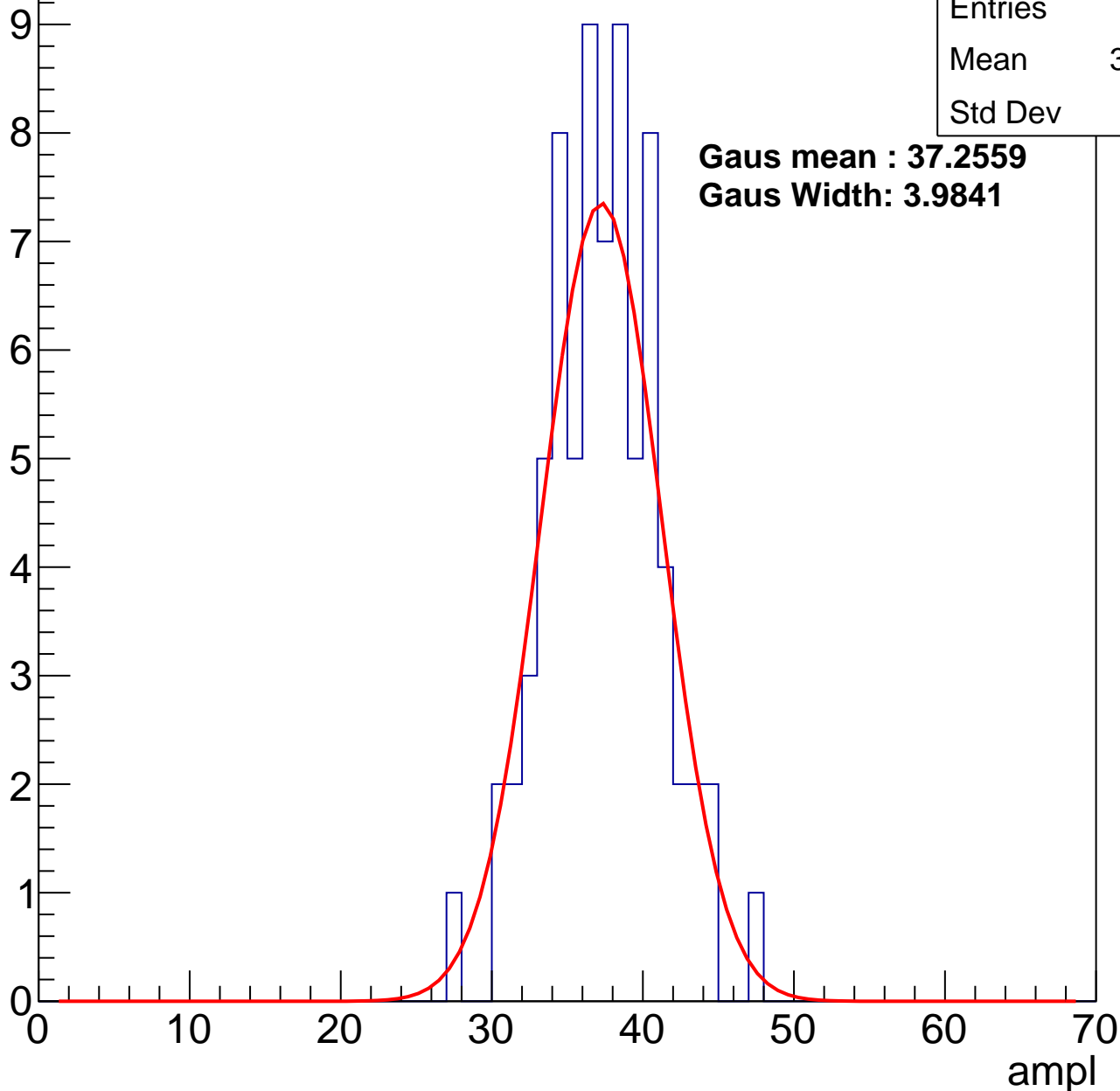
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	75
Mean	36.88
Std Dev	3.67

**Gaus mean : 37.2559**

**Gaus Width: 3.9841**



# B1L101S, U20-ch15, adc2

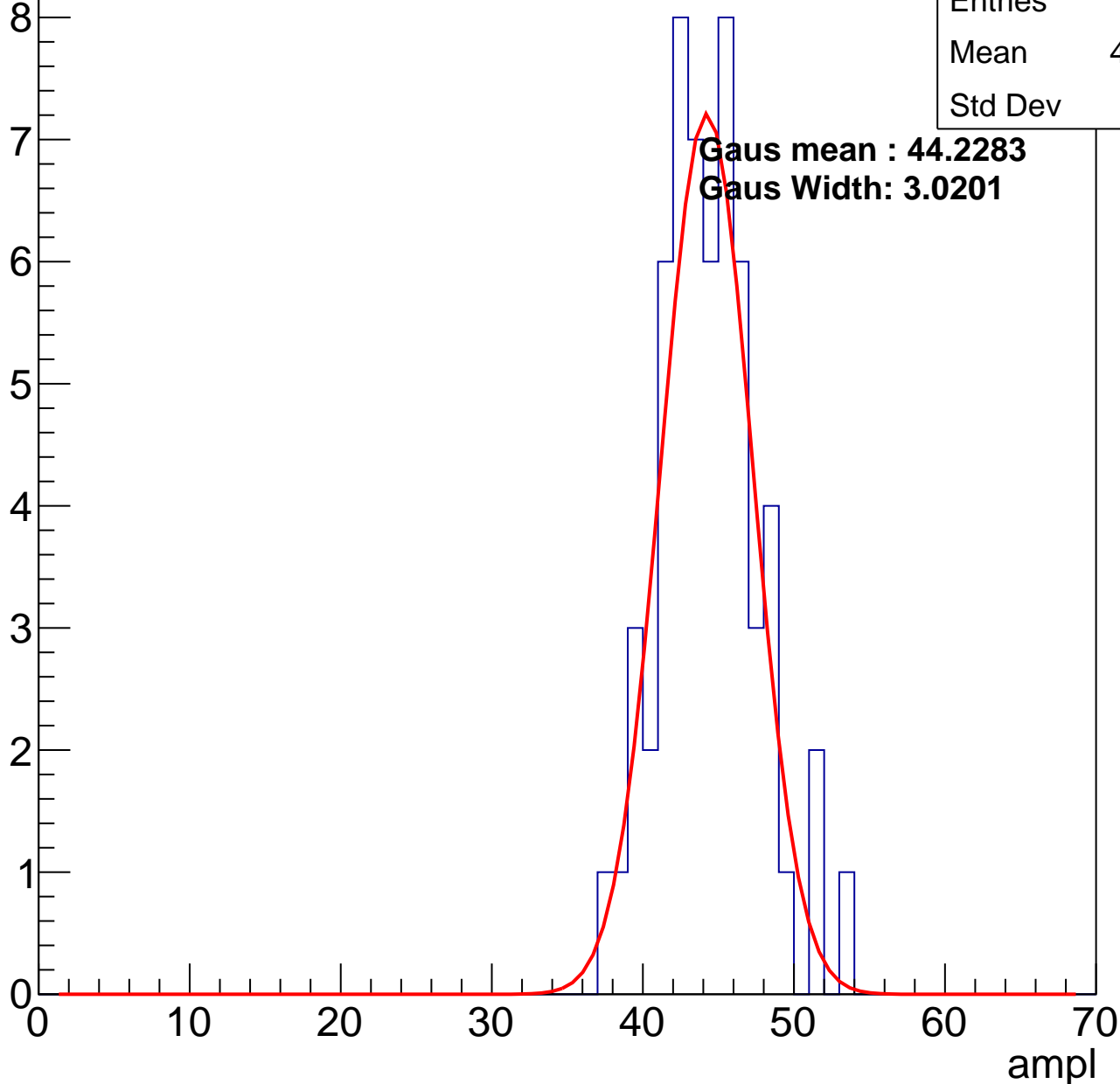
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	59
Mean	43.93
Std Dev	3.22

**Gaus mean : 44.2283**

**Gaus Width: 3.0201**

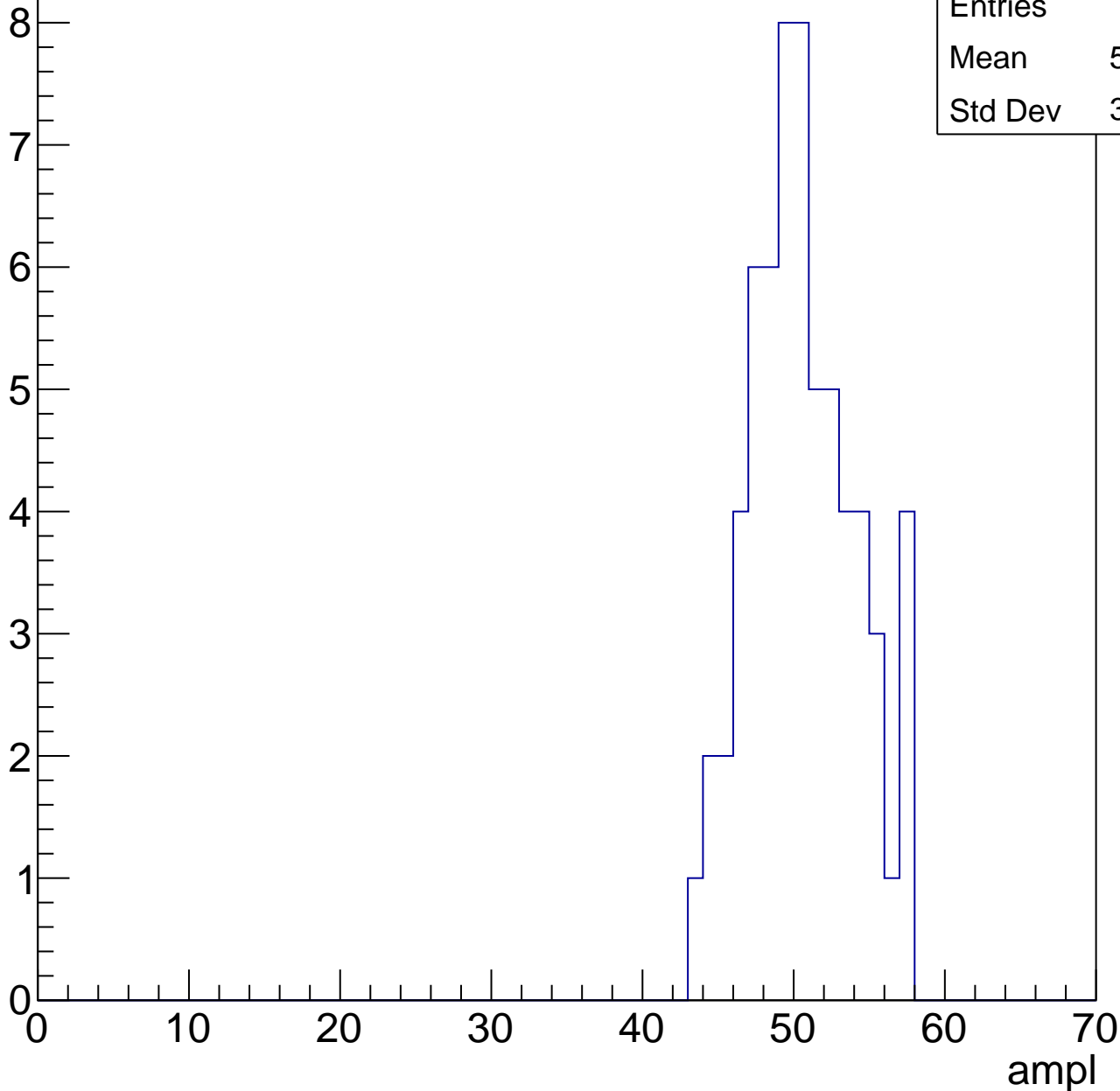


# B1L101S, U20-ch15, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

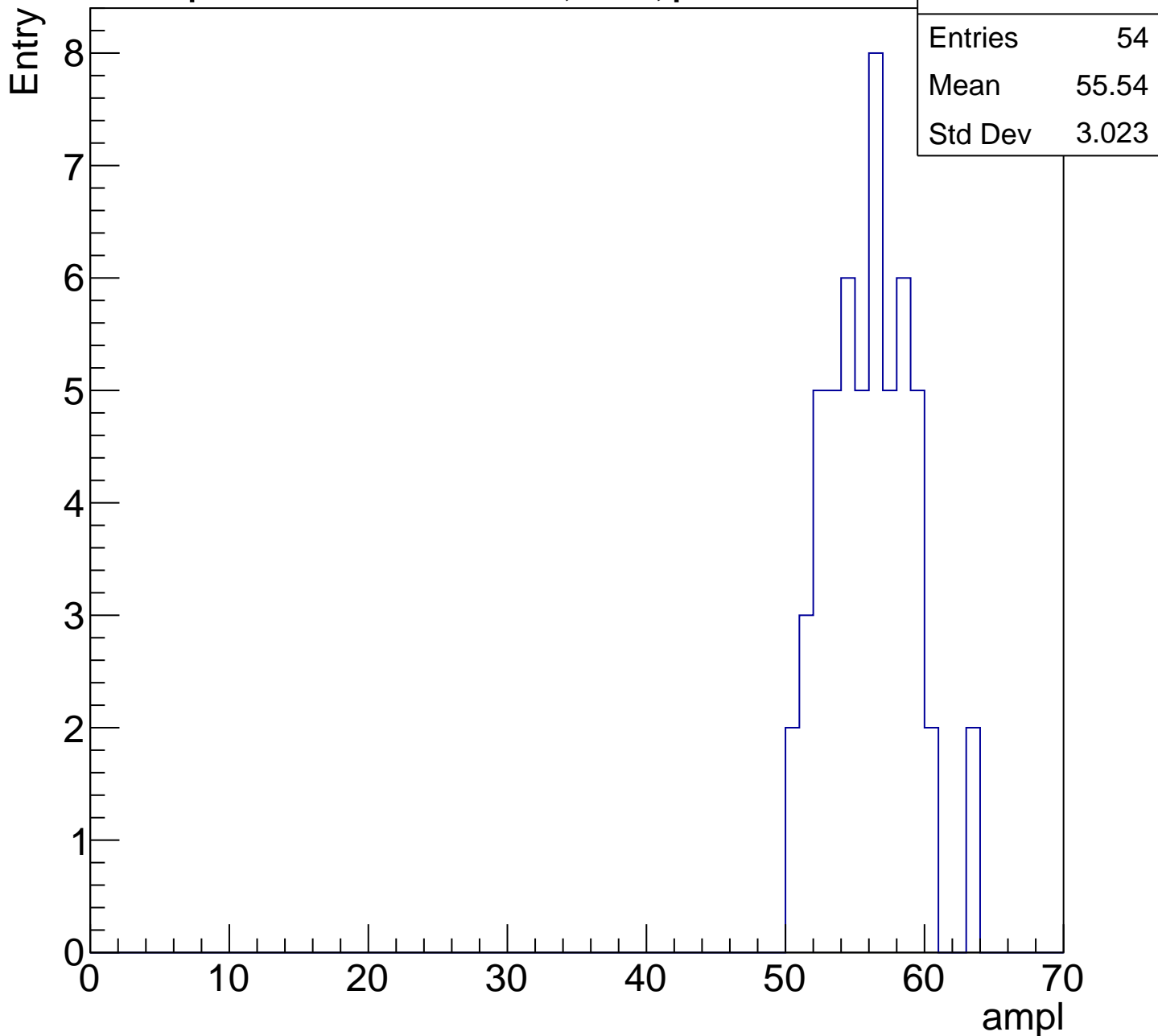
Entry

Entries	63
Mean	50.14
Std Dev	3.454



# B1L101S, U20-ch15, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U20-ch15, adc5

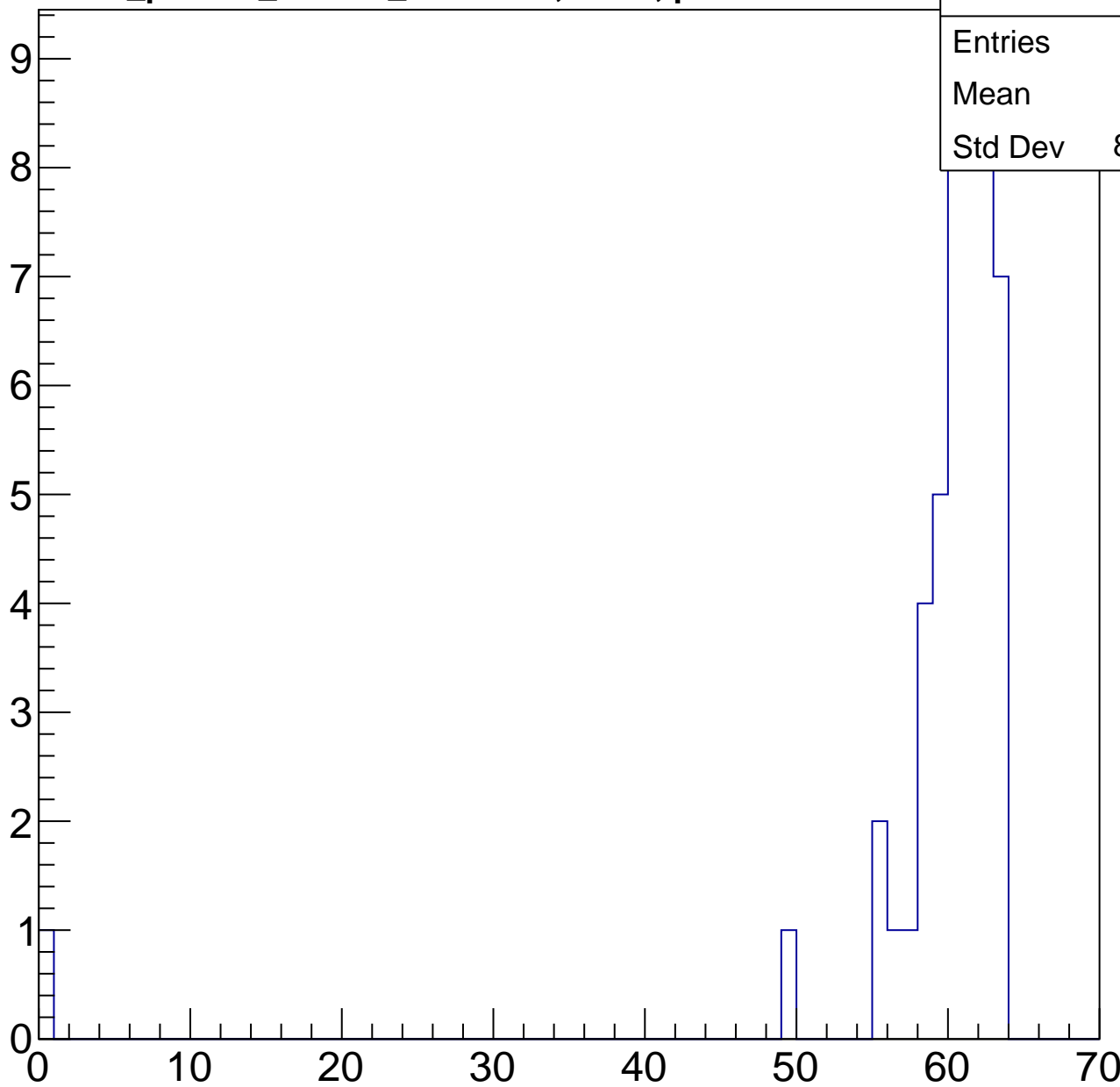
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	48
Mean	58.9
Std Dev	8.975

ampl



# B1L101S, U20-ch15, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U20-ch15, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U20-ch16, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	66
Mean	29.14
Std Dev	4.933

**Gaus mean : 30.2202**

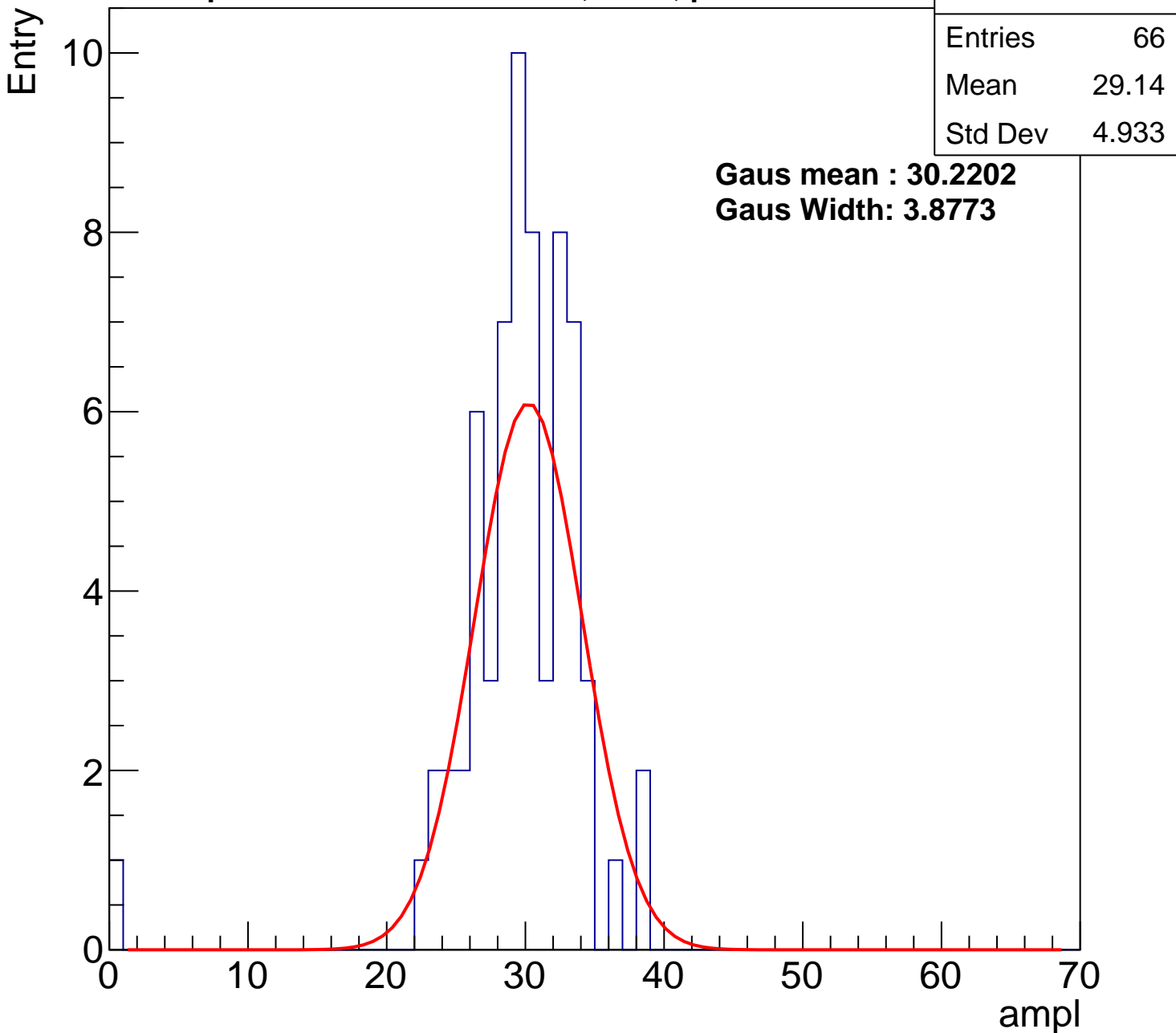
**Gaus Width: 3.8773**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U20-ch16, adc1

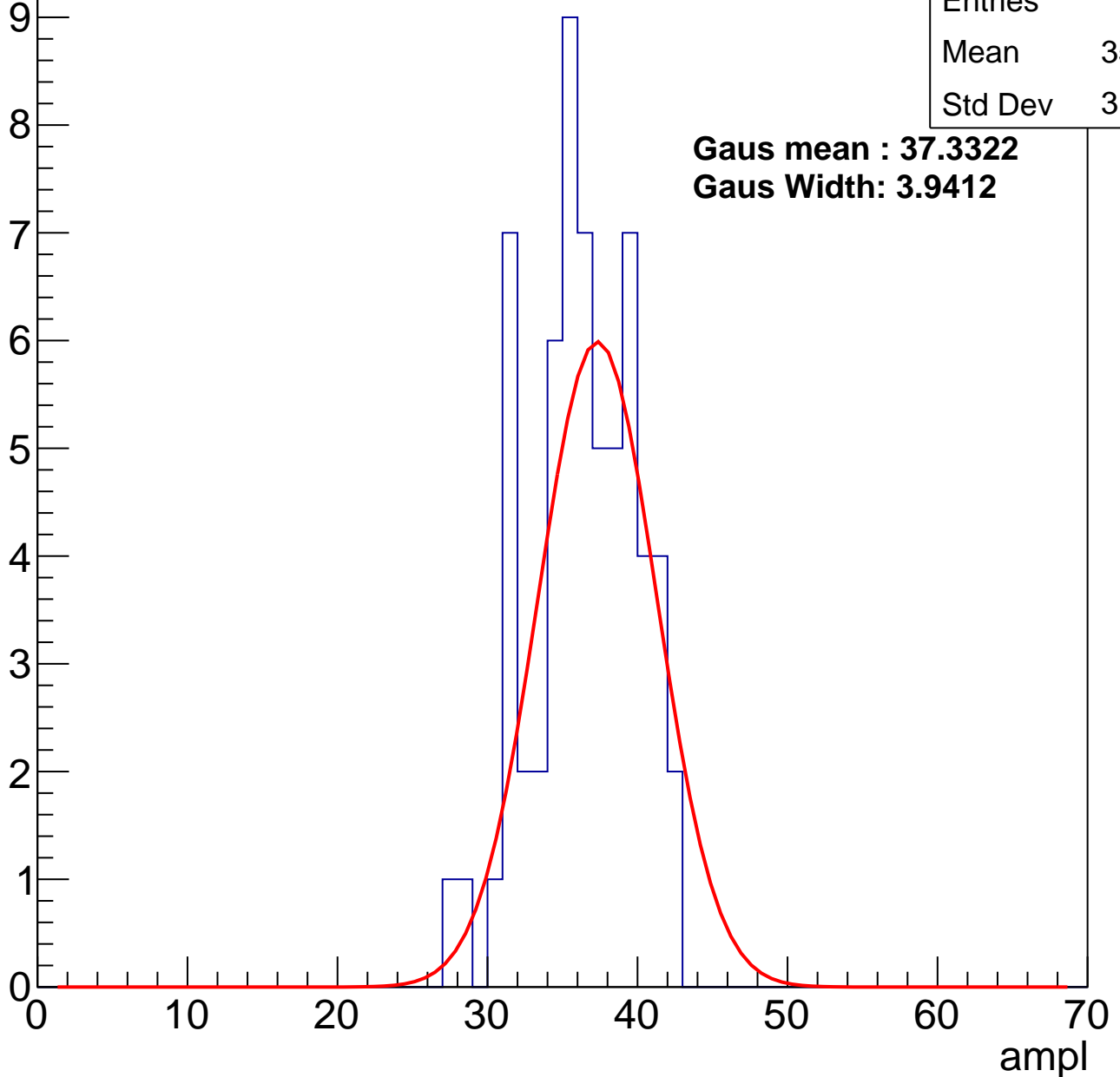
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	35.86
Std Dev	3.477

**Gaus mean : 37.3322**

**Gaus Width: 3.9412**

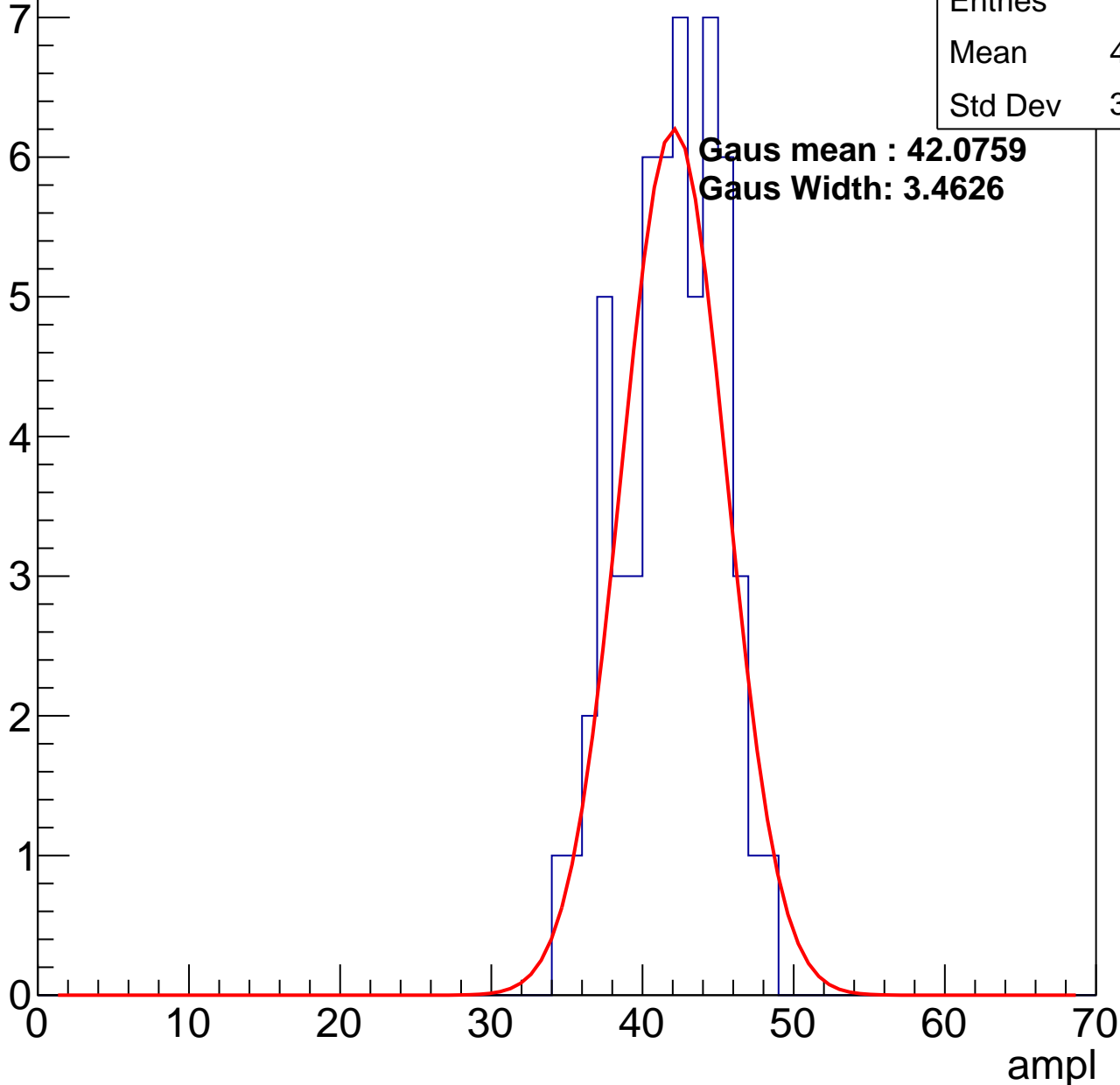


# B1L101S, U20-ch16, adc2

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	57
Mean	41.46
Std Dev	3.229

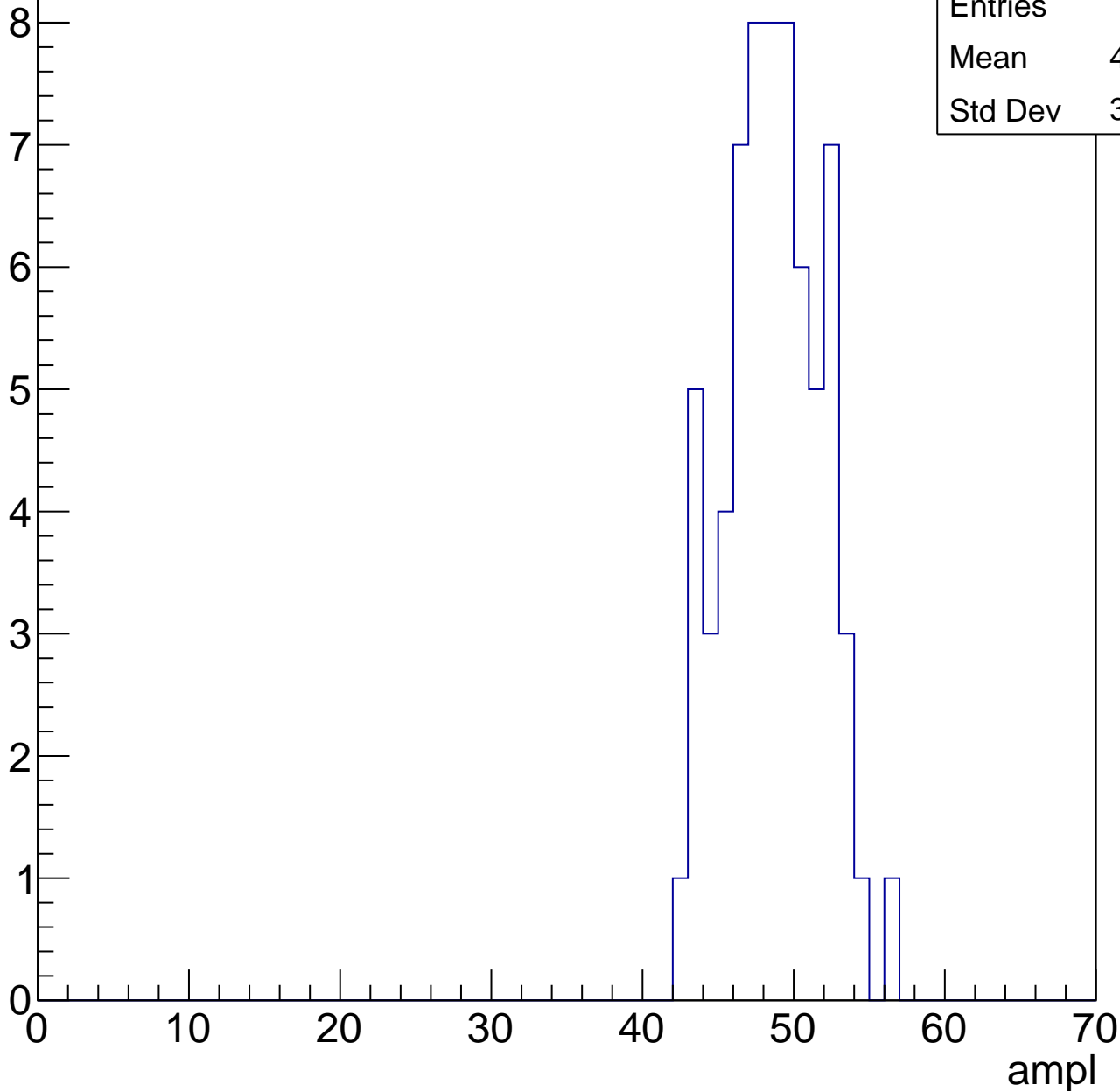


# B1L101S, U20-ch16, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	67
Mean	48.22
Std Dev	3.095

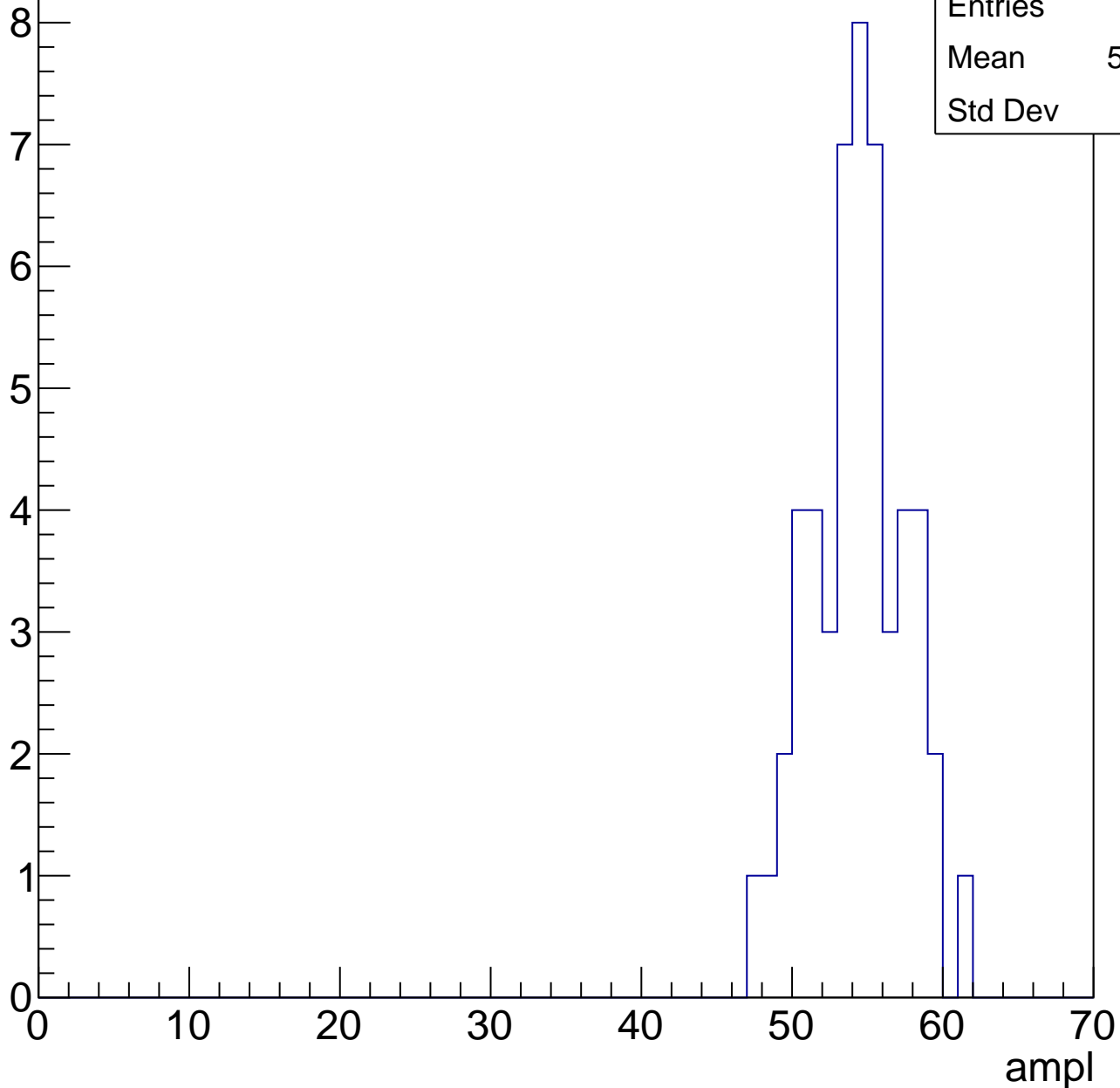


# B1L101S, U20-ch16, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	51
Mean	53.88
Std Dev	3.04



# B1L101S, U20-ch16, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

10

Entries 64

Mean 59.3

Std Dev 2.638

8

6

4

2

0

0

10

20

30

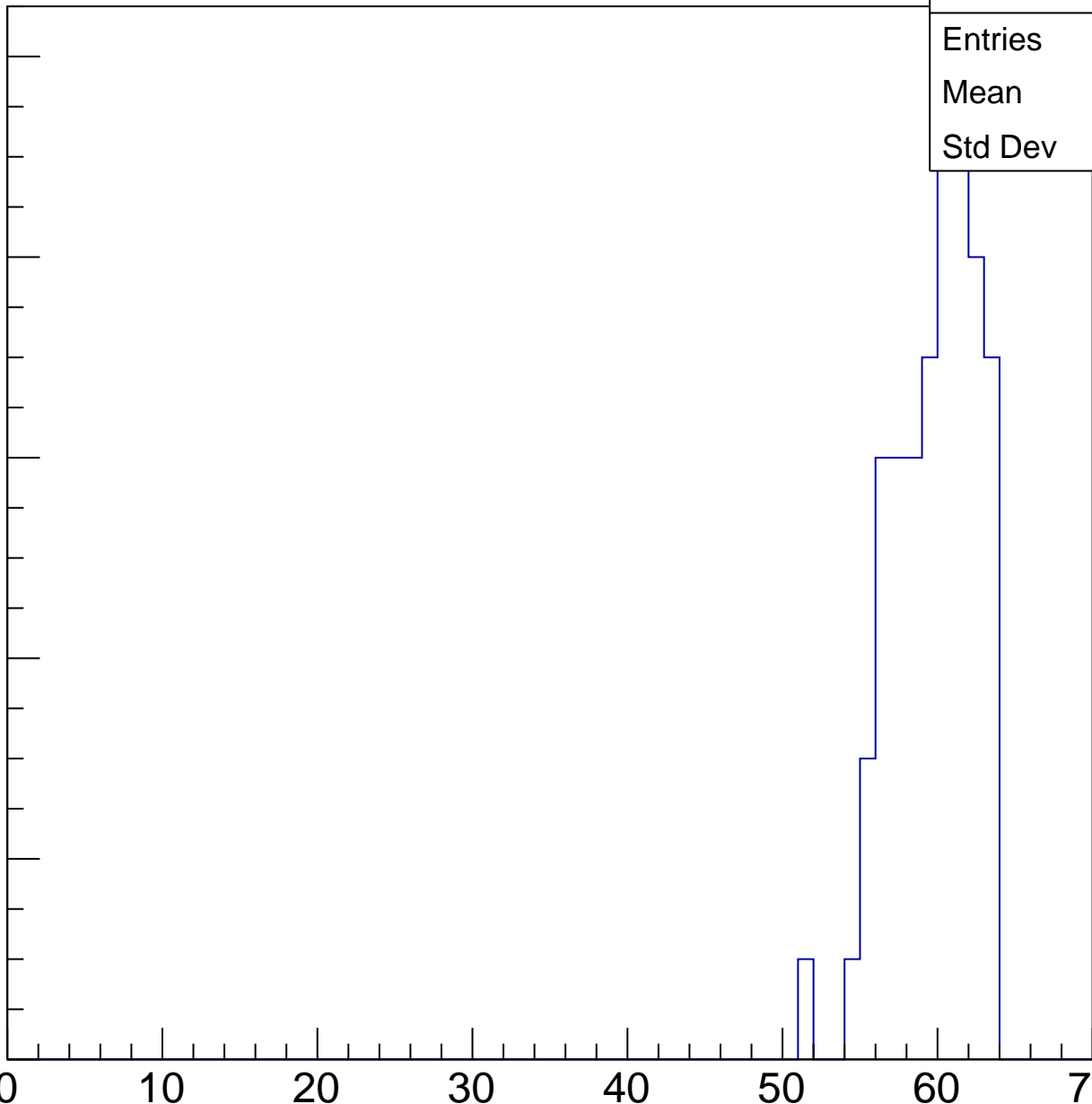
40

50

60

70

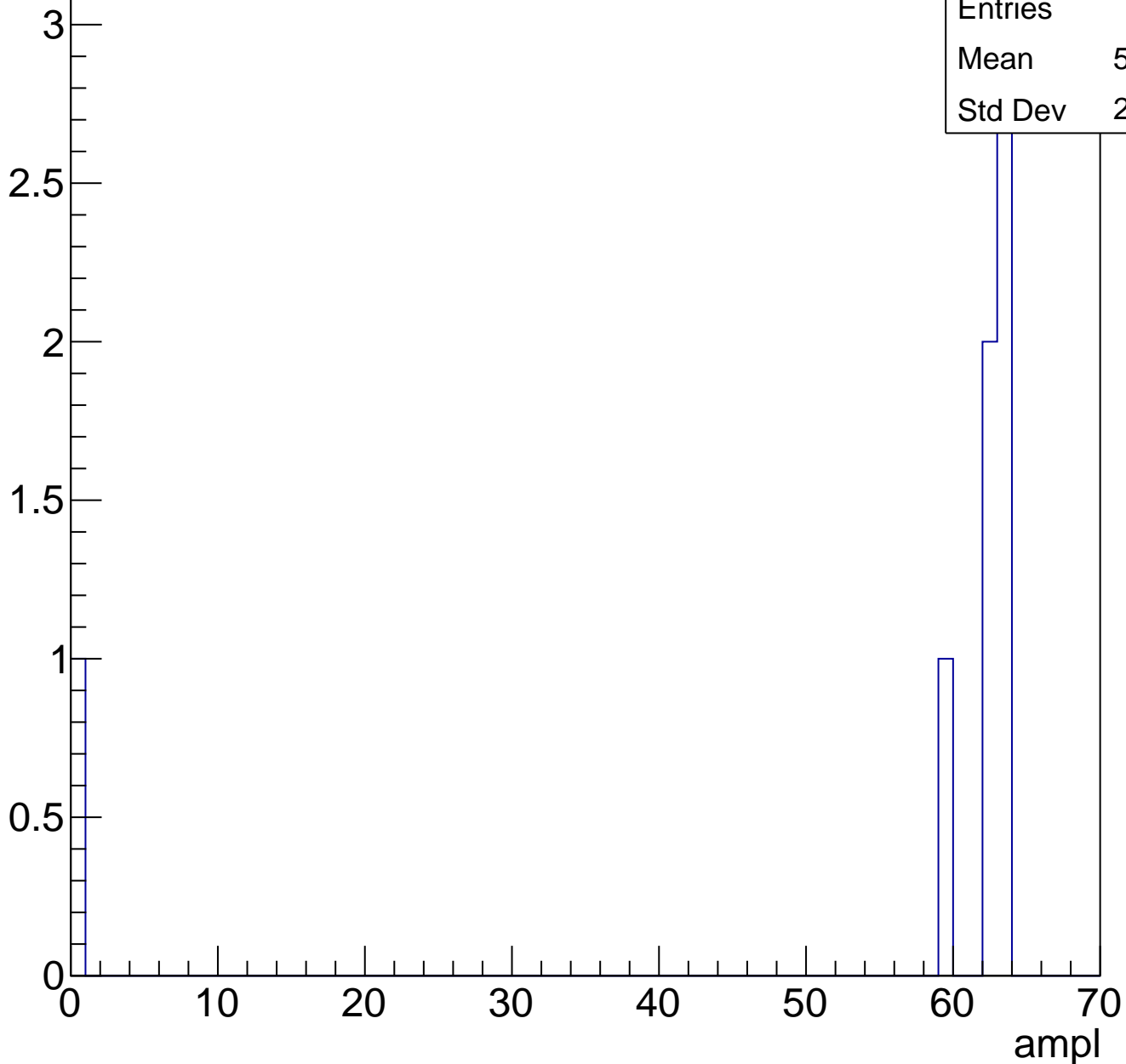
ampl



# B1L101S, U20-ch16, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U20-ch16, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U20-ch17, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	77
Mean	29.22
Std Dev	6.585

**Gaus mean : 30.6799**

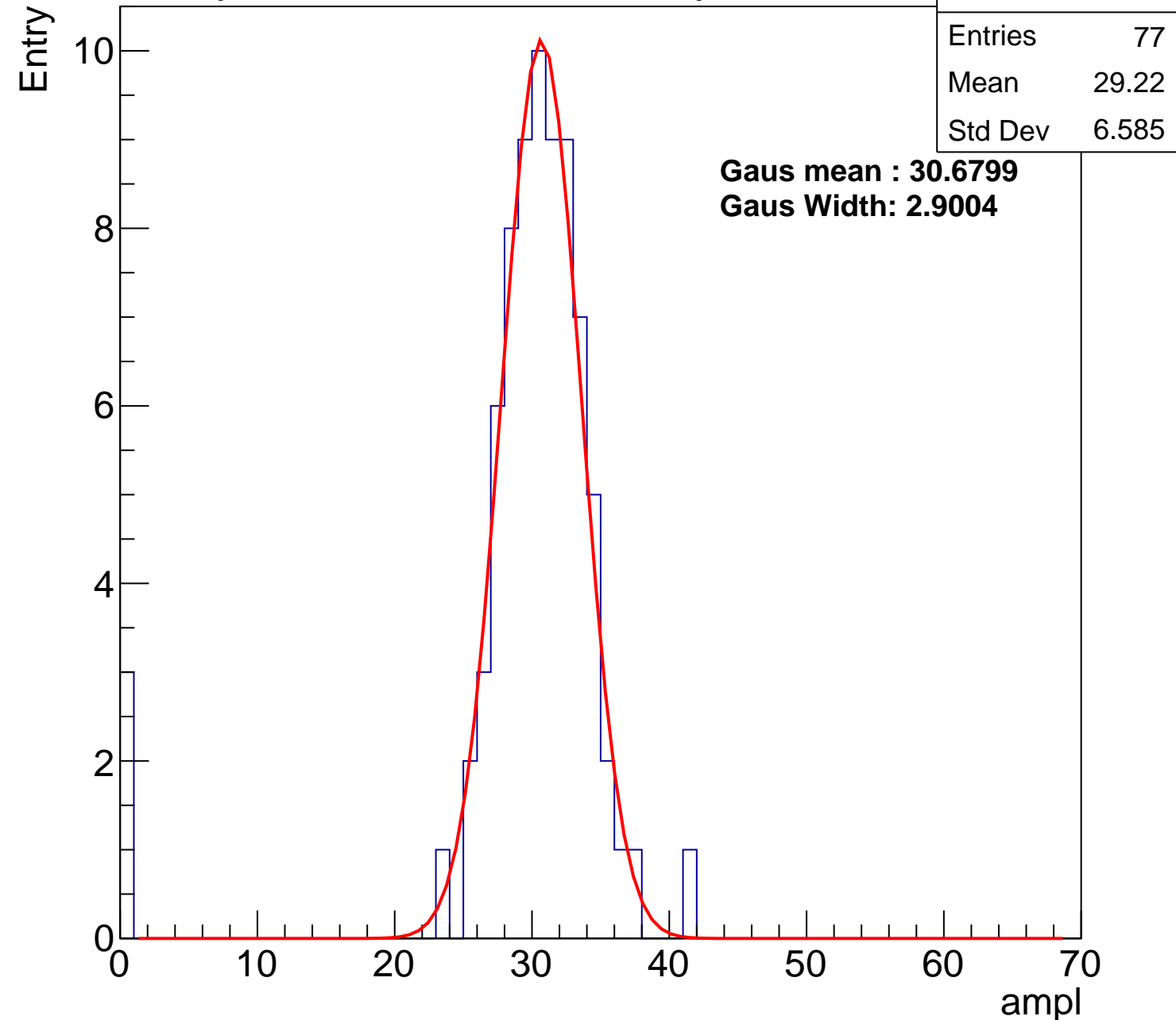
**Gaus Width: 2.9004**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U20-ch17, adc1

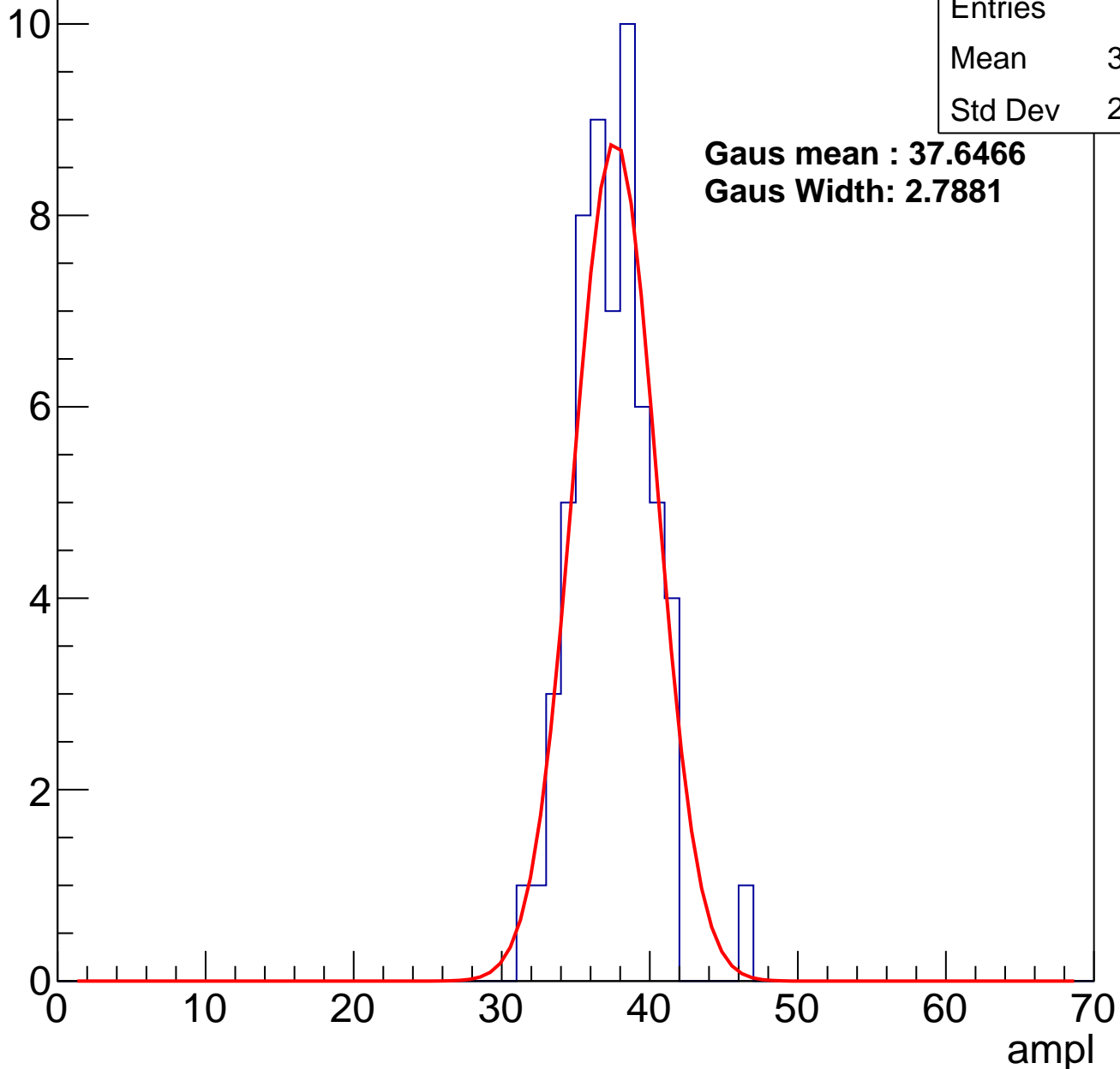
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	60
Mean	36.98
Std Dev	2.643

**Gaus mean : 37.6466**

**Gaus Width: 2.7881**

Entry



# B1L101S, U20-ch17, adc2

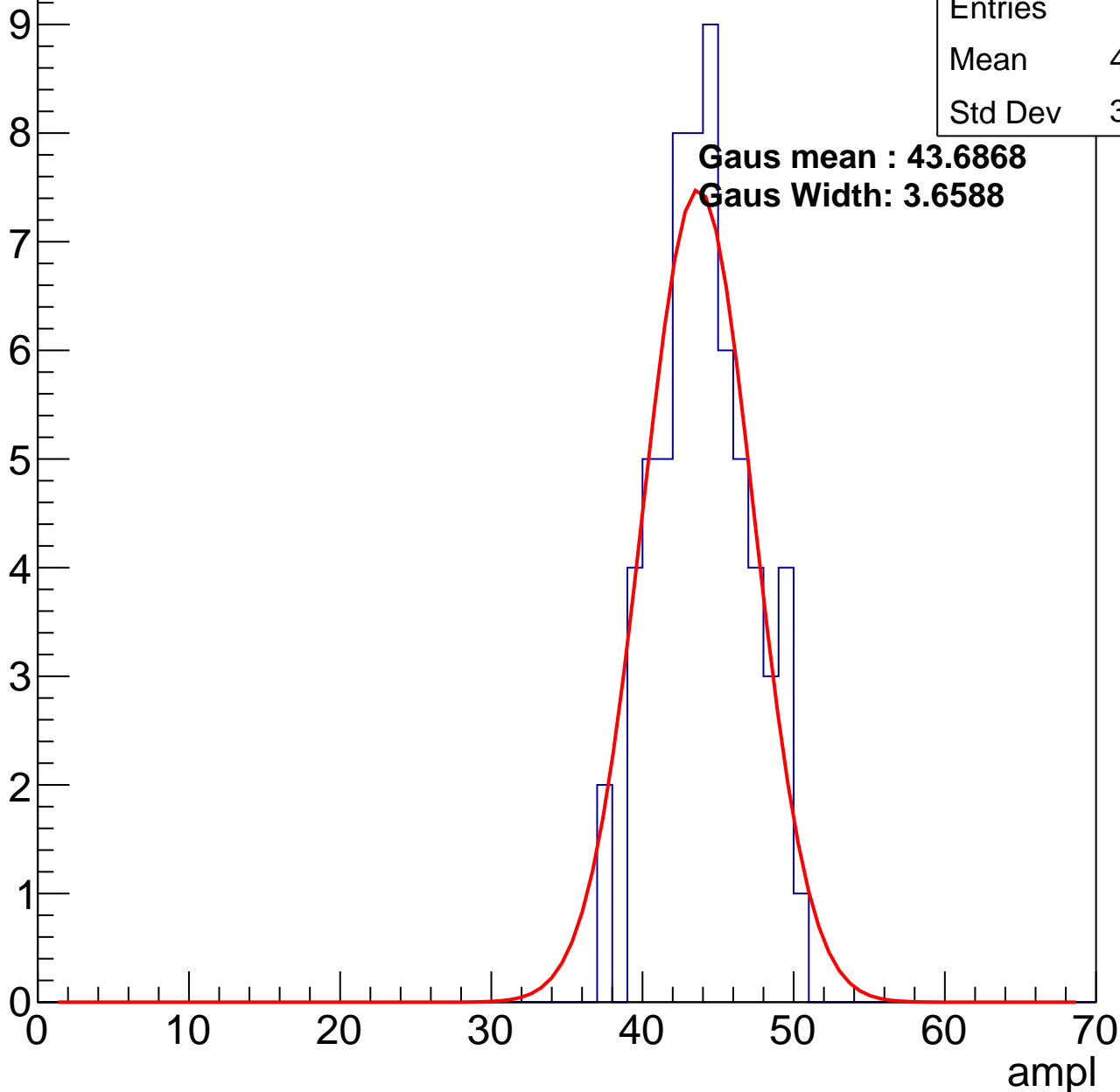
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	43.58
Std Dev	3.056

**Gaus mean : 43.6868**

**Gaus Width: 3.6588**

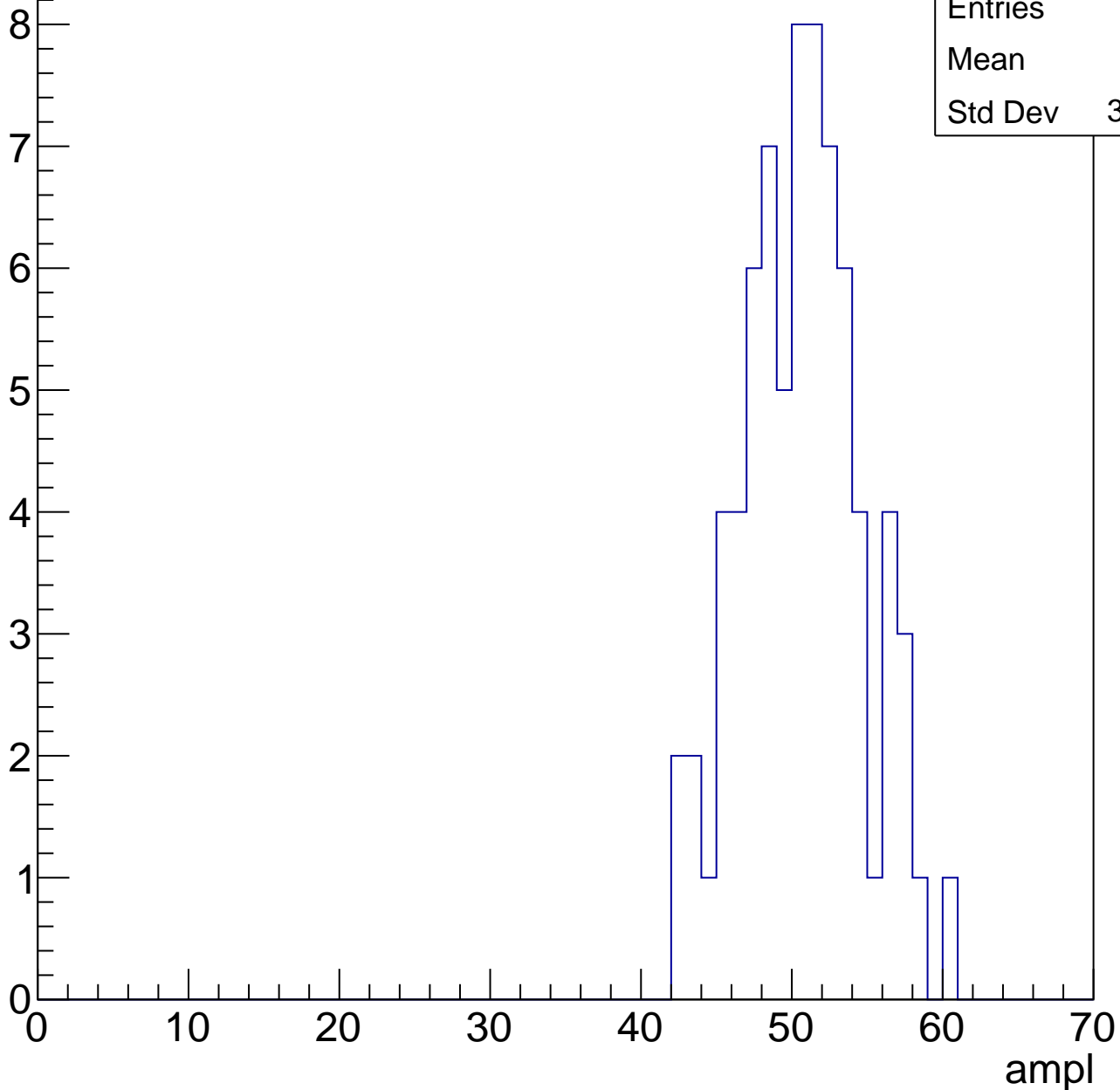


# B1L101S, U20-ch17, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	74
Mean	50.2
Std Dev	3.932

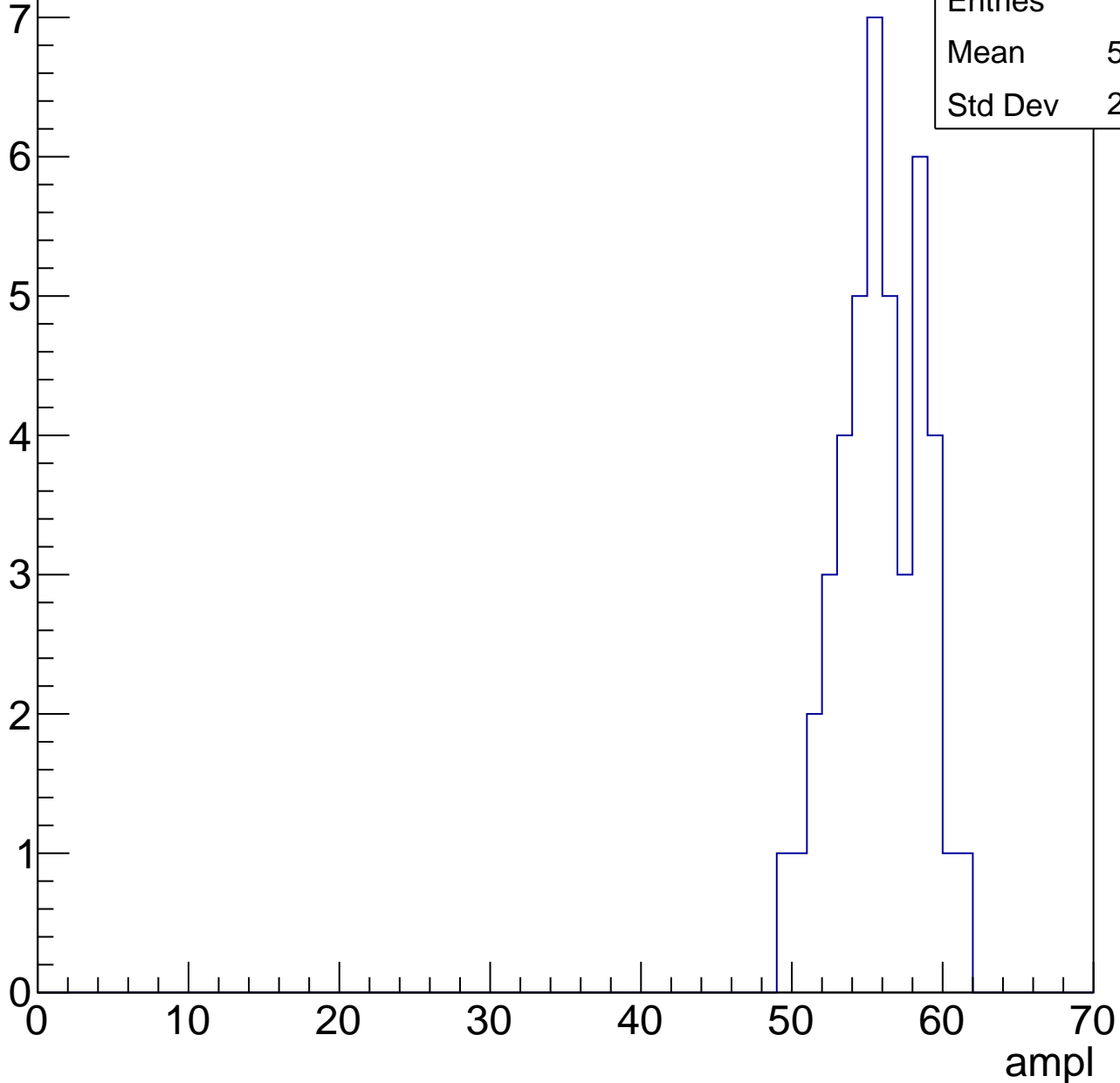


# B1L101S, U20-ch17, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	43
Mean	55.35
Std Dev	2.778

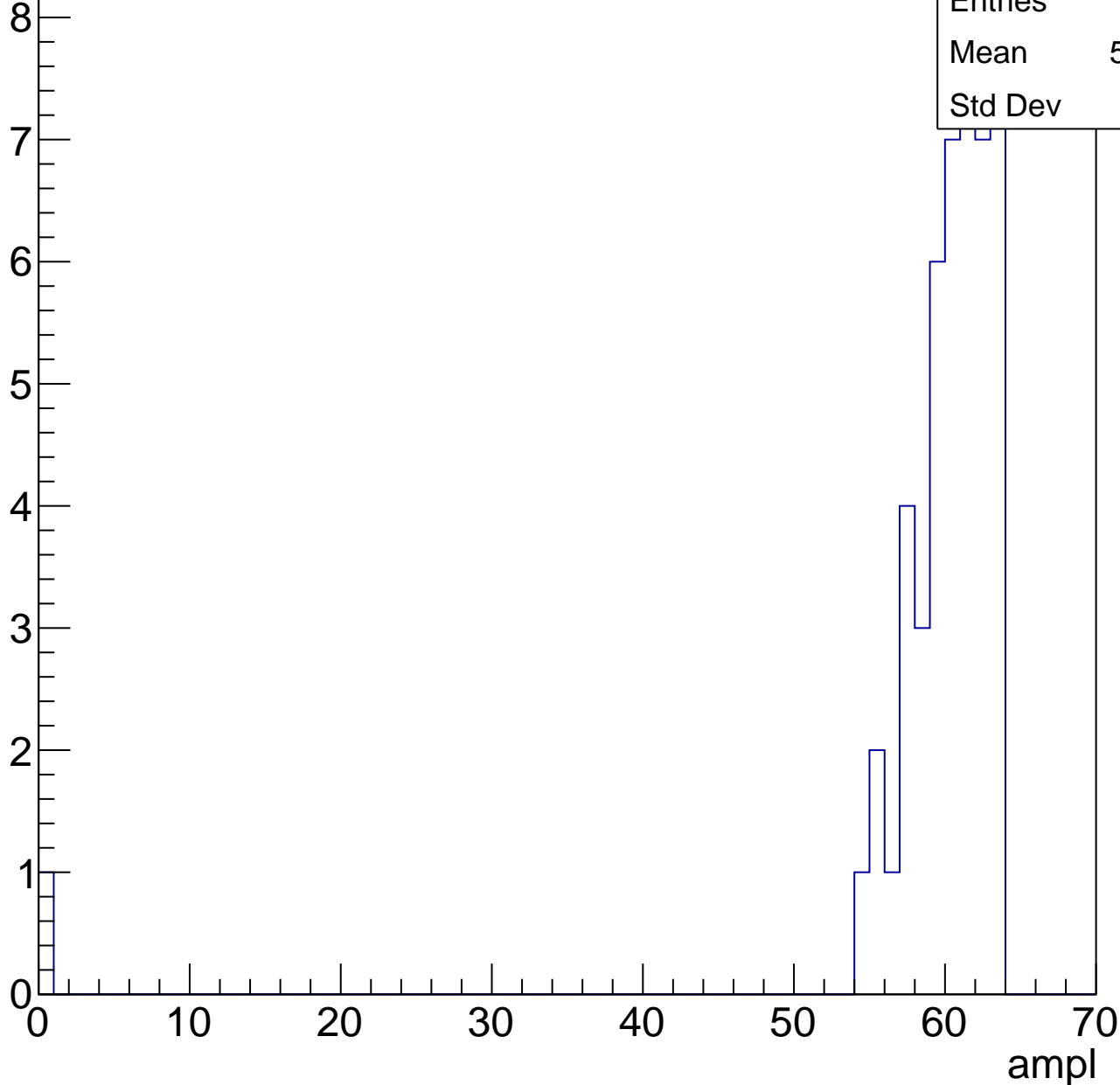


# B1L101S, U20-ch17, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	48
Mean	58.79
Std Dev	8.89



# B1L101S, U20-ch17, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

3

2.5

2

1.5

1

0.5

0

0

10

20

30

40

50

60

70

ampl

Entries

7

Mean

61.86

Std Dev

0.9897



# B1L101S, U20-ch17, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U20-ch18, adc0

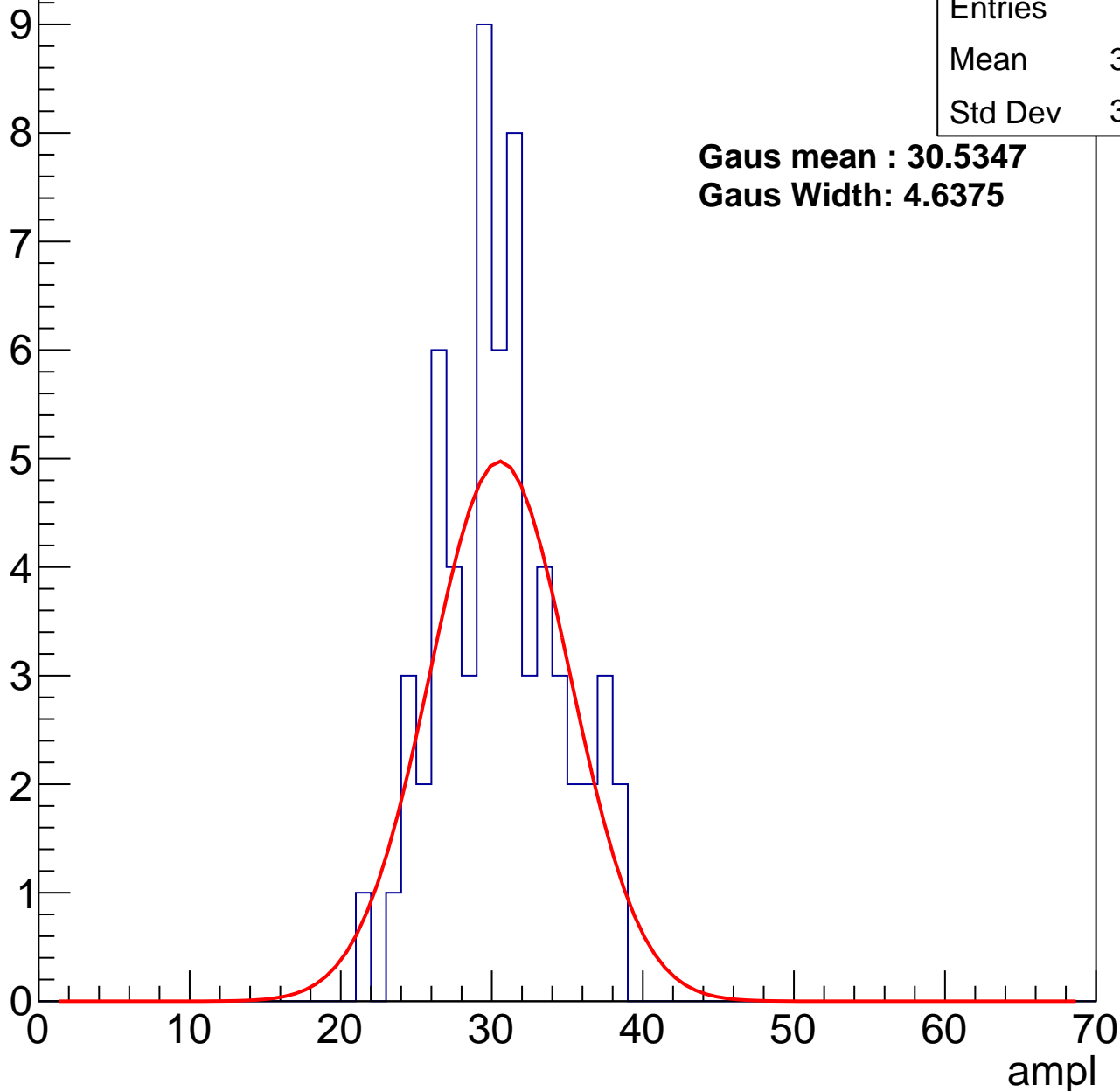
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	30.03
Std Dev	3.898

**Gaus mean : 30.5347**

**Gaus Width: 4.6375**



# B1L101S, U20-ch18, adc1

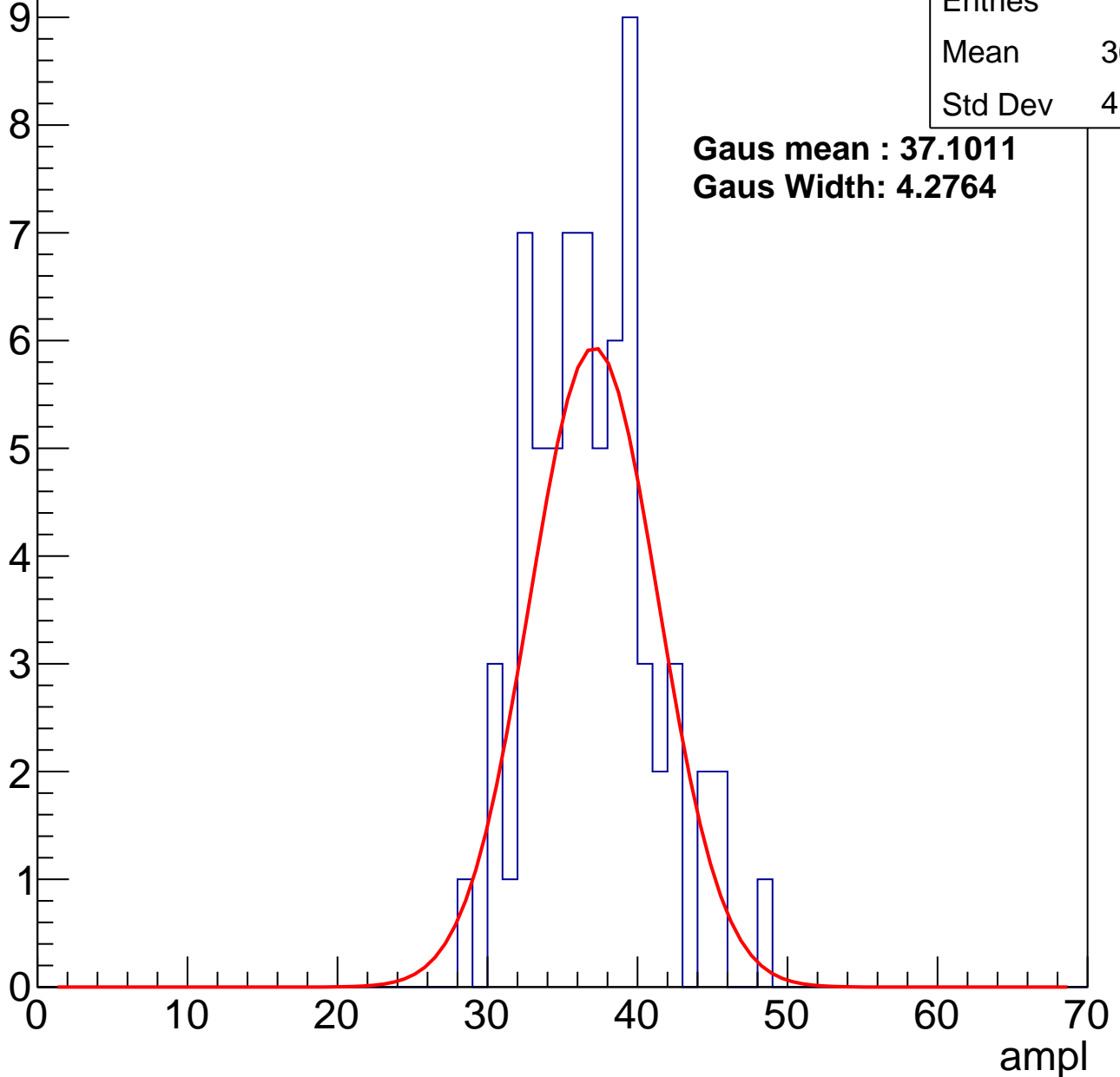
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	36.57
Std Dev	4.009

**Gaus mean : 37.1011**

**Gaus Width: 4.2764**



# B1L101S, U20-ch18, adc2

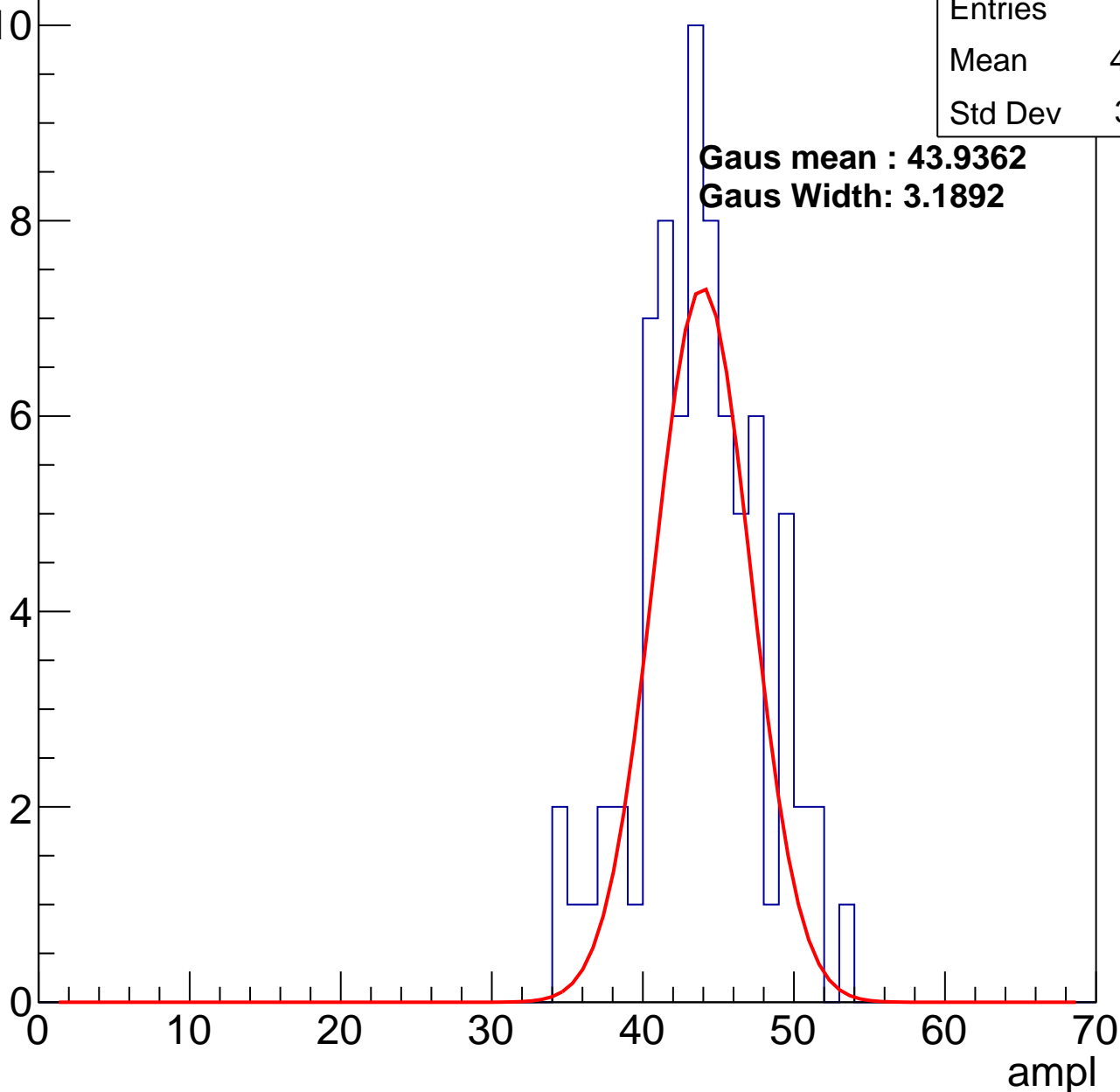
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	76
Mean	43.42
Std Dev	3.981

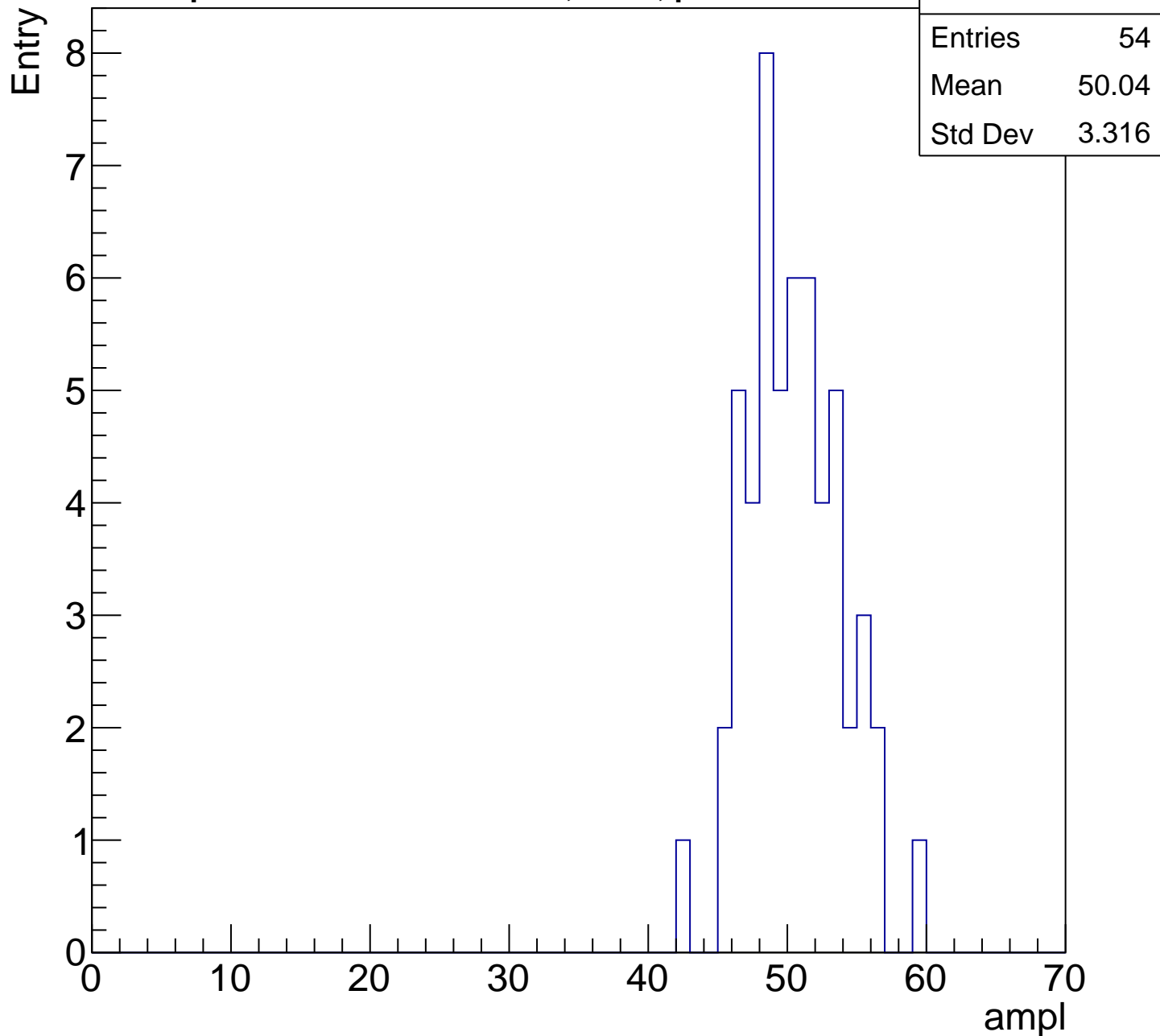
**Gaus mean : 43.9362**

**Gaus Width: 3.1892**



# B1L101S, U20-ch18, adc3

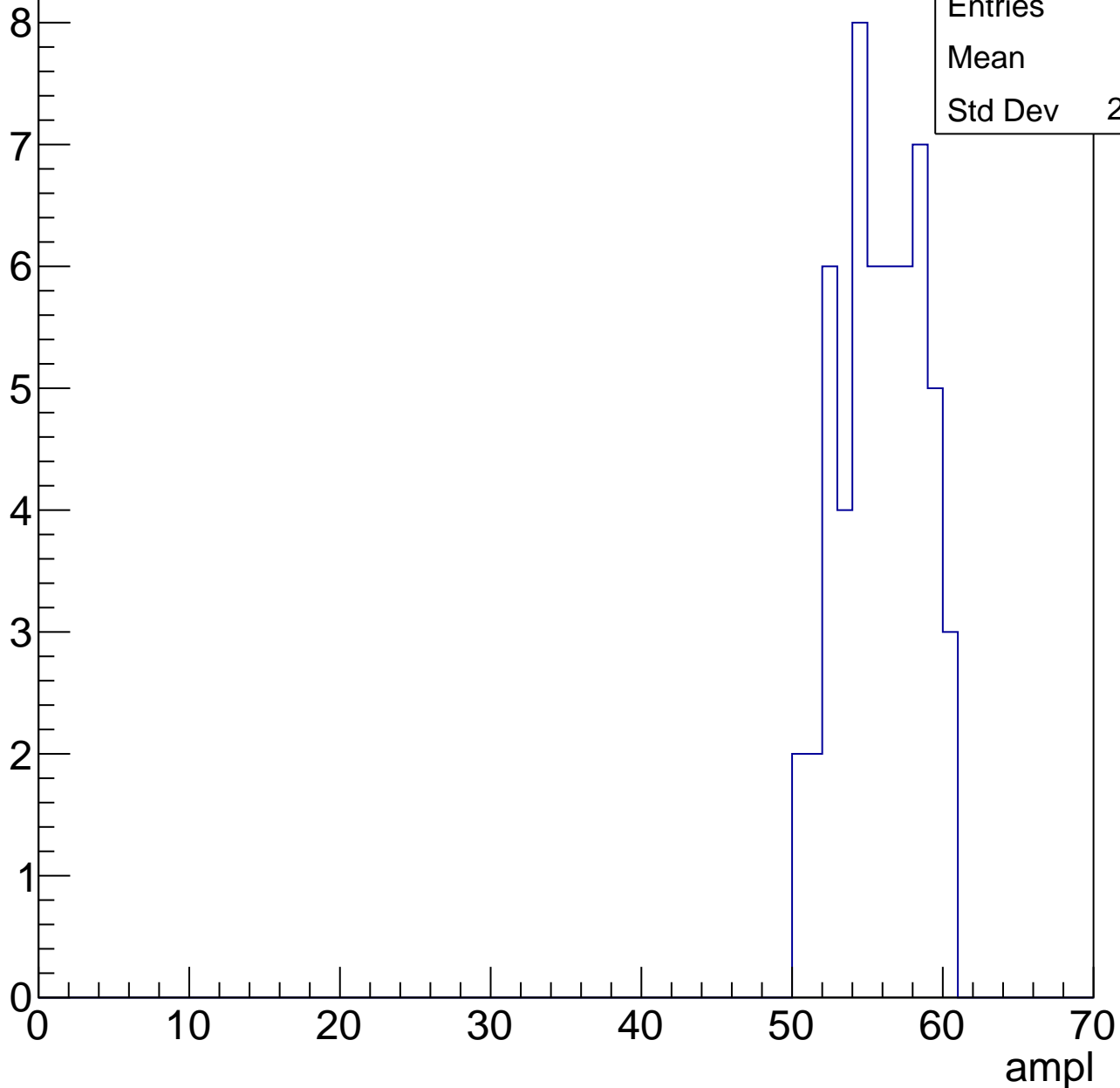
calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U20-ch18, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



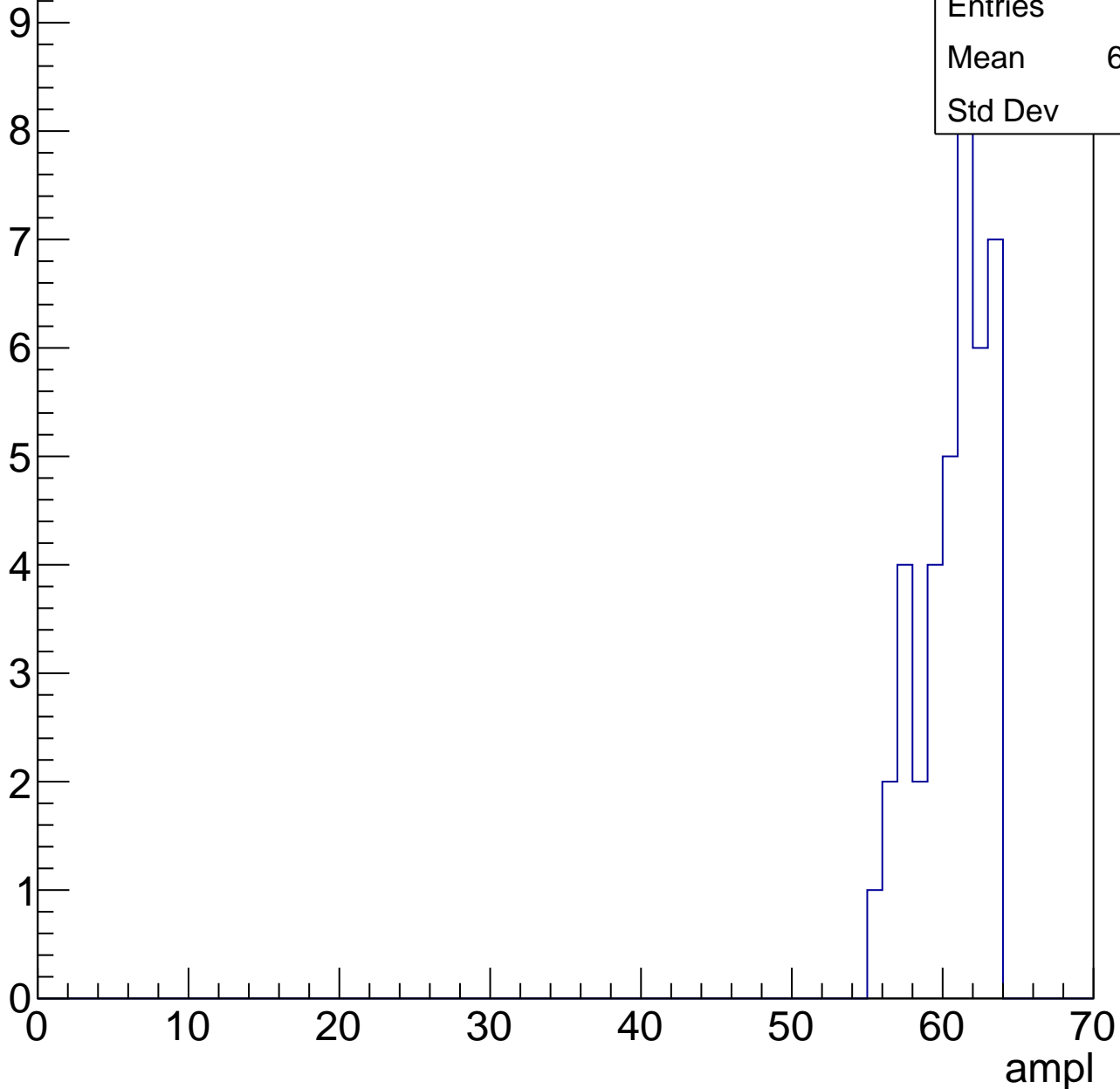
Entries	55
Mean	55.4
Std Dev	2.694

# B1L101S, U20-ch18, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

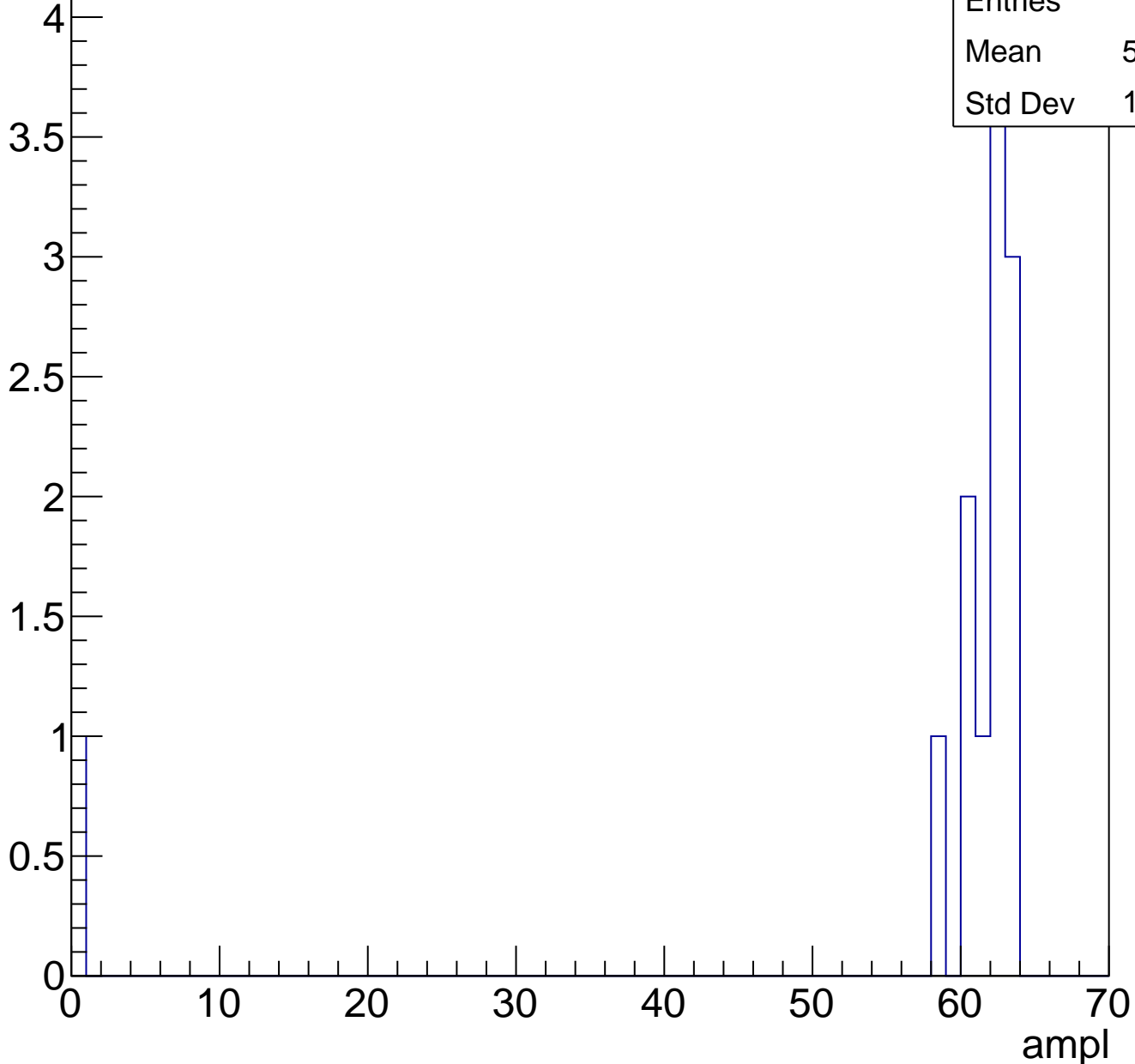
Entries	40
Mean	60.23
Std Dev	2.23



# B1L101S, U20-ch18, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U20-ch18, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L101S, U20-ch19, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	75
Mean	30.01
Std Dev	4.583

**Gaus mean : 30.8193**

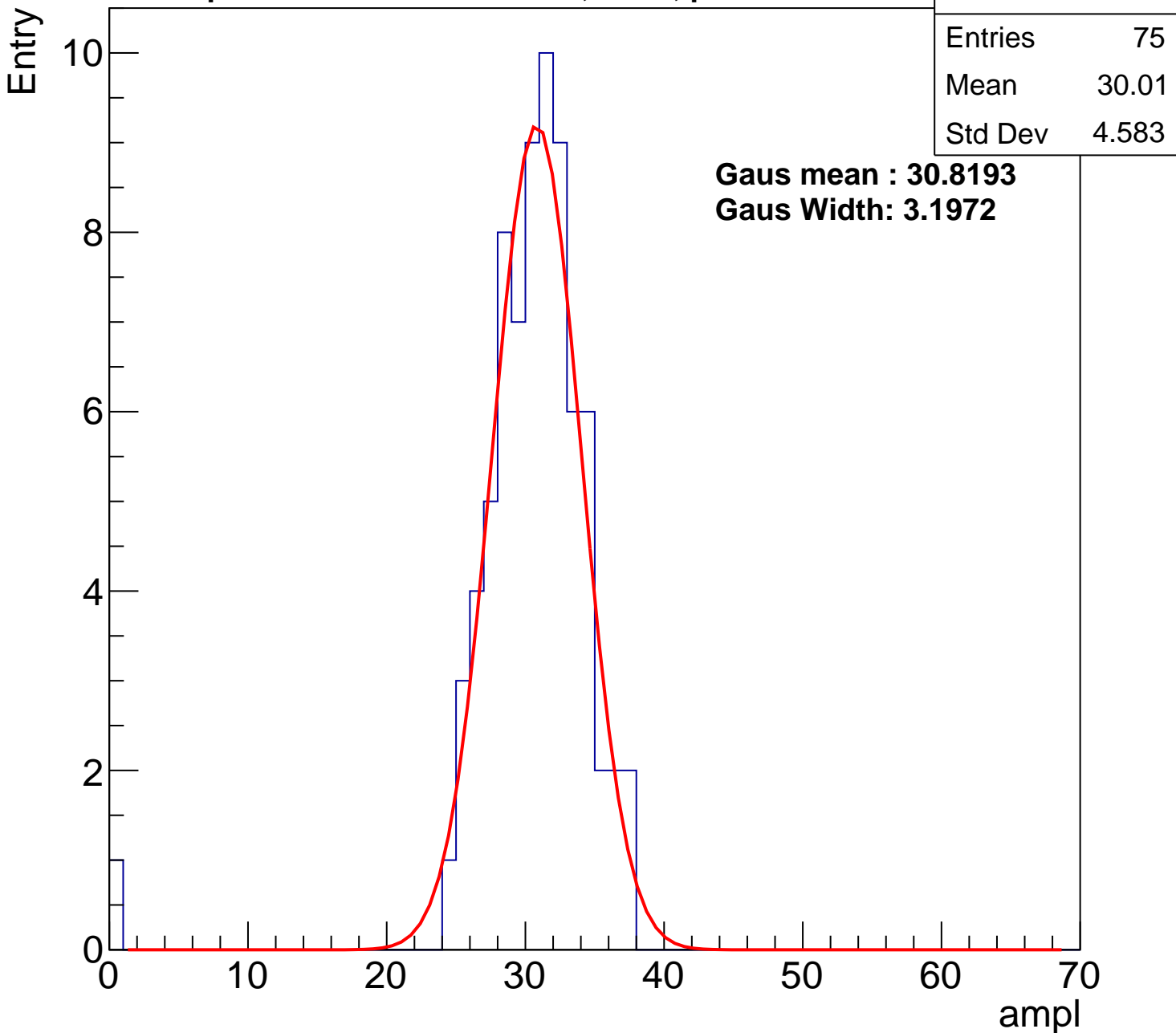
**Gaus Width: 3.1972**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U20-ch19, adc1

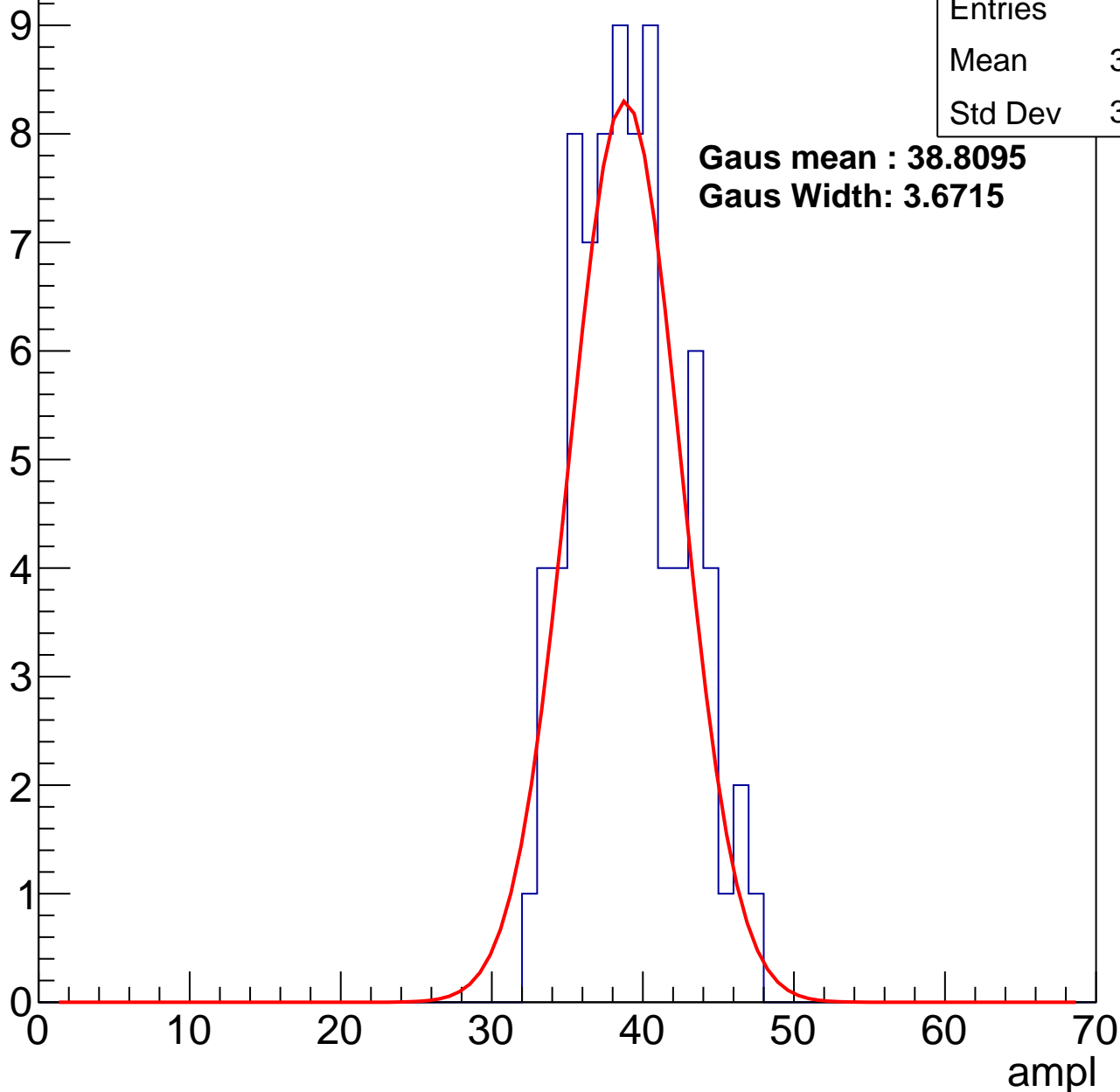
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	80
Mean	38.65
Std Dev	3.482

**Gaus mean : 38.8095**

**Gaus Width: 3.6715**



# B1L101S, U20-ch19, adc2

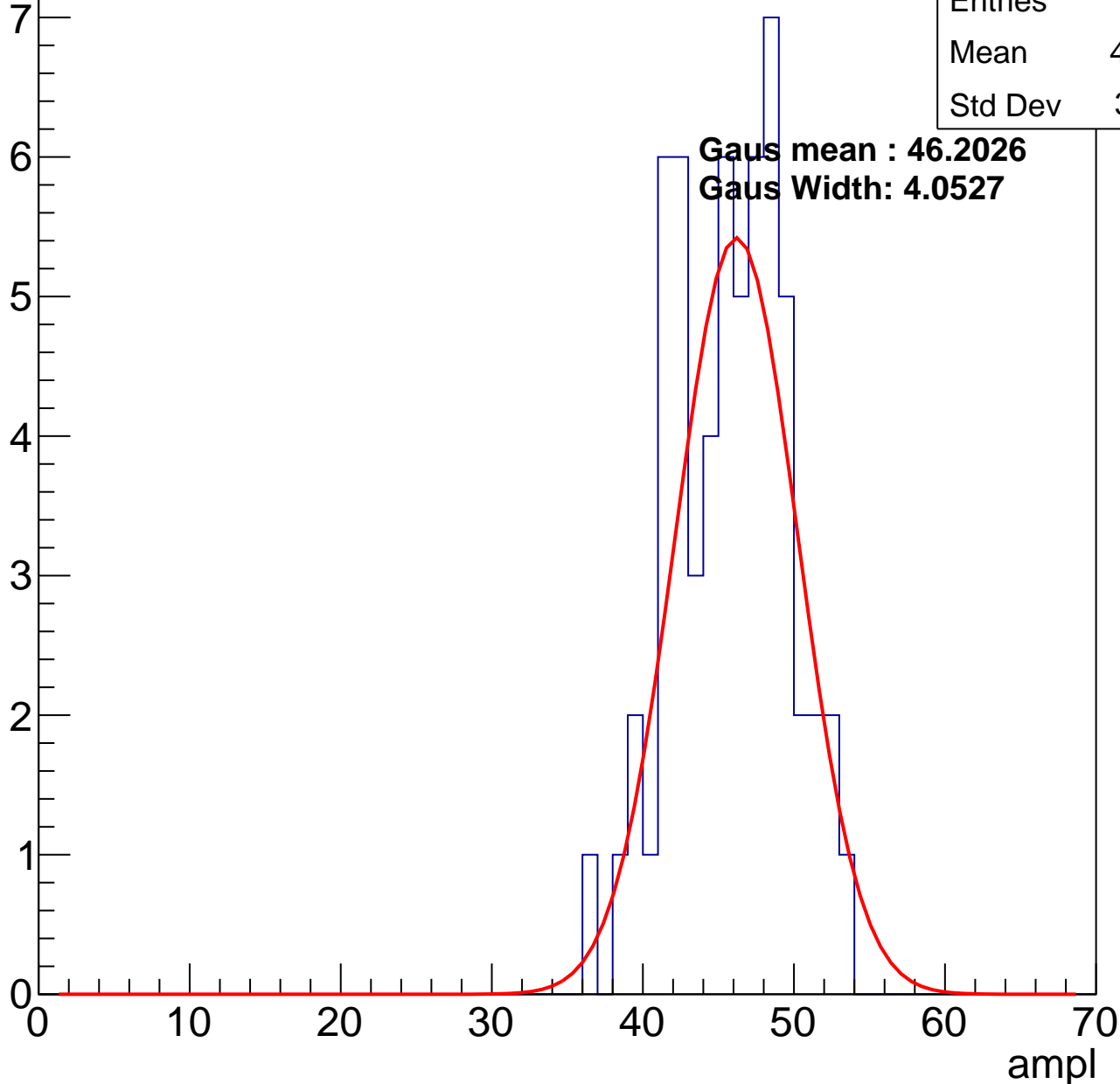
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	60
Mean	45.28
Std Dev	3.751

**Gaus mean : 46.2026**

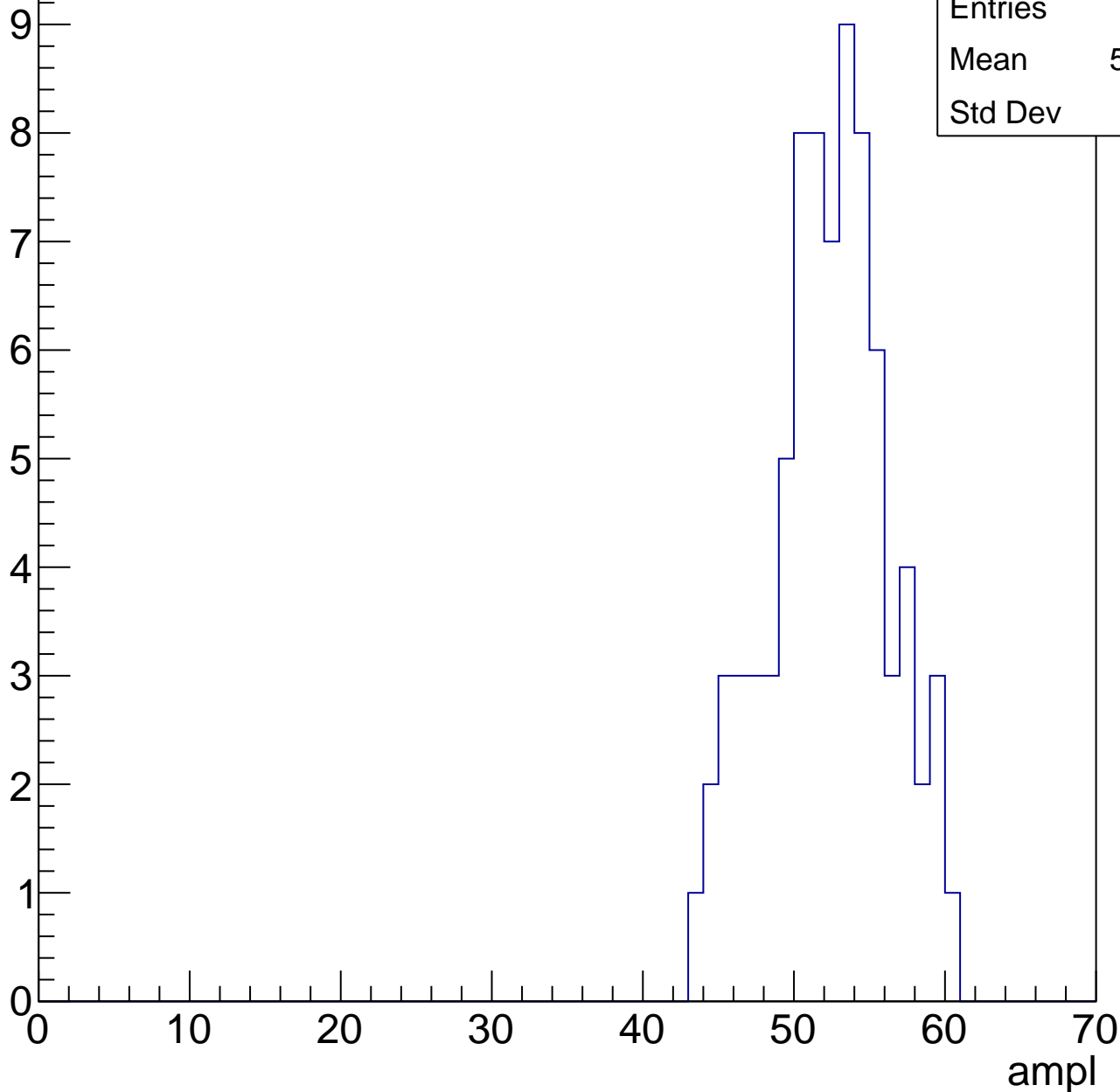
**Gaus Width: 4.0527**



# B1L101S, U20-ch19, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

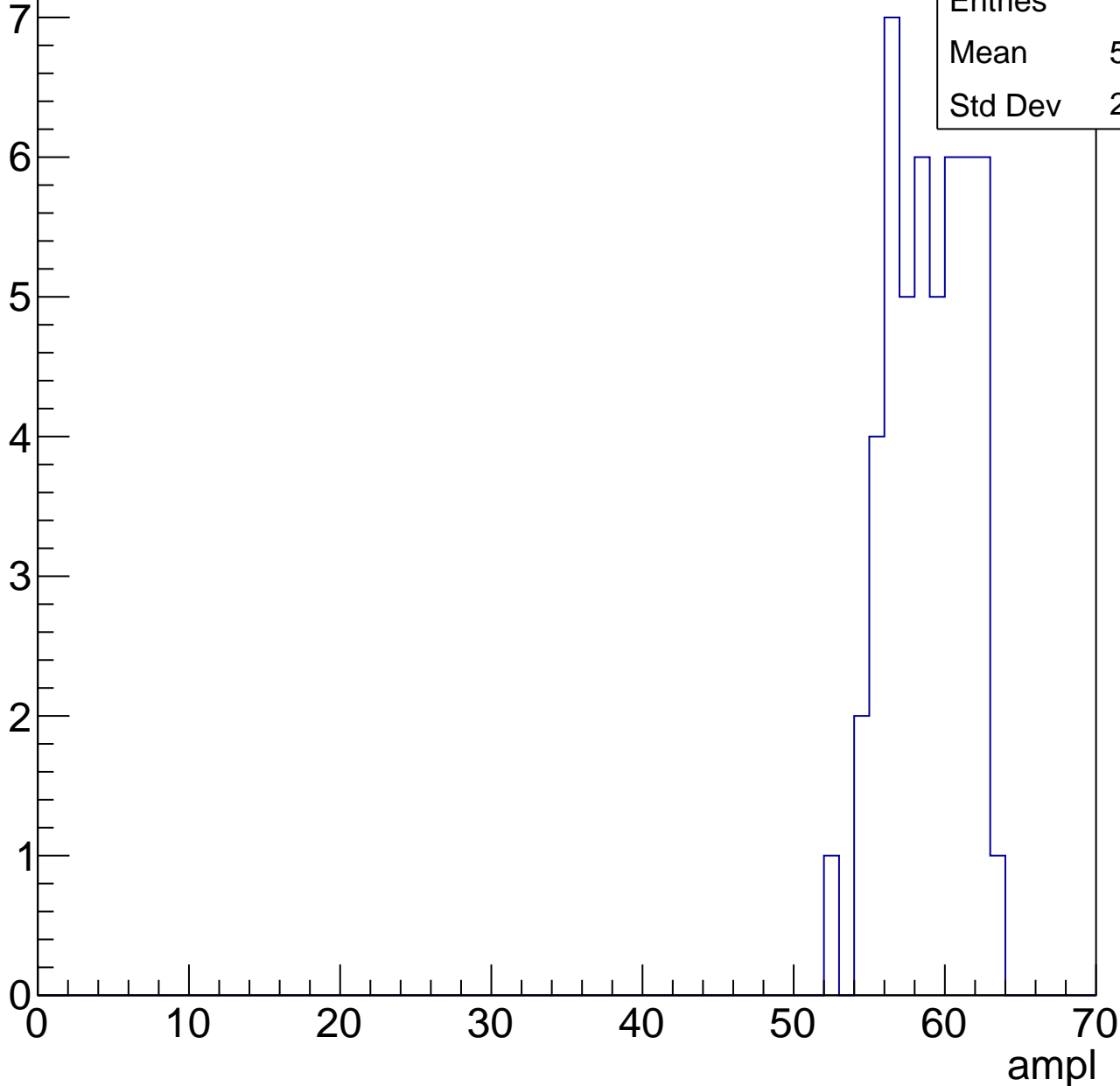


# B1L101S, U20-ch19, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	49
Mean	58.39
Std Dev	2.609

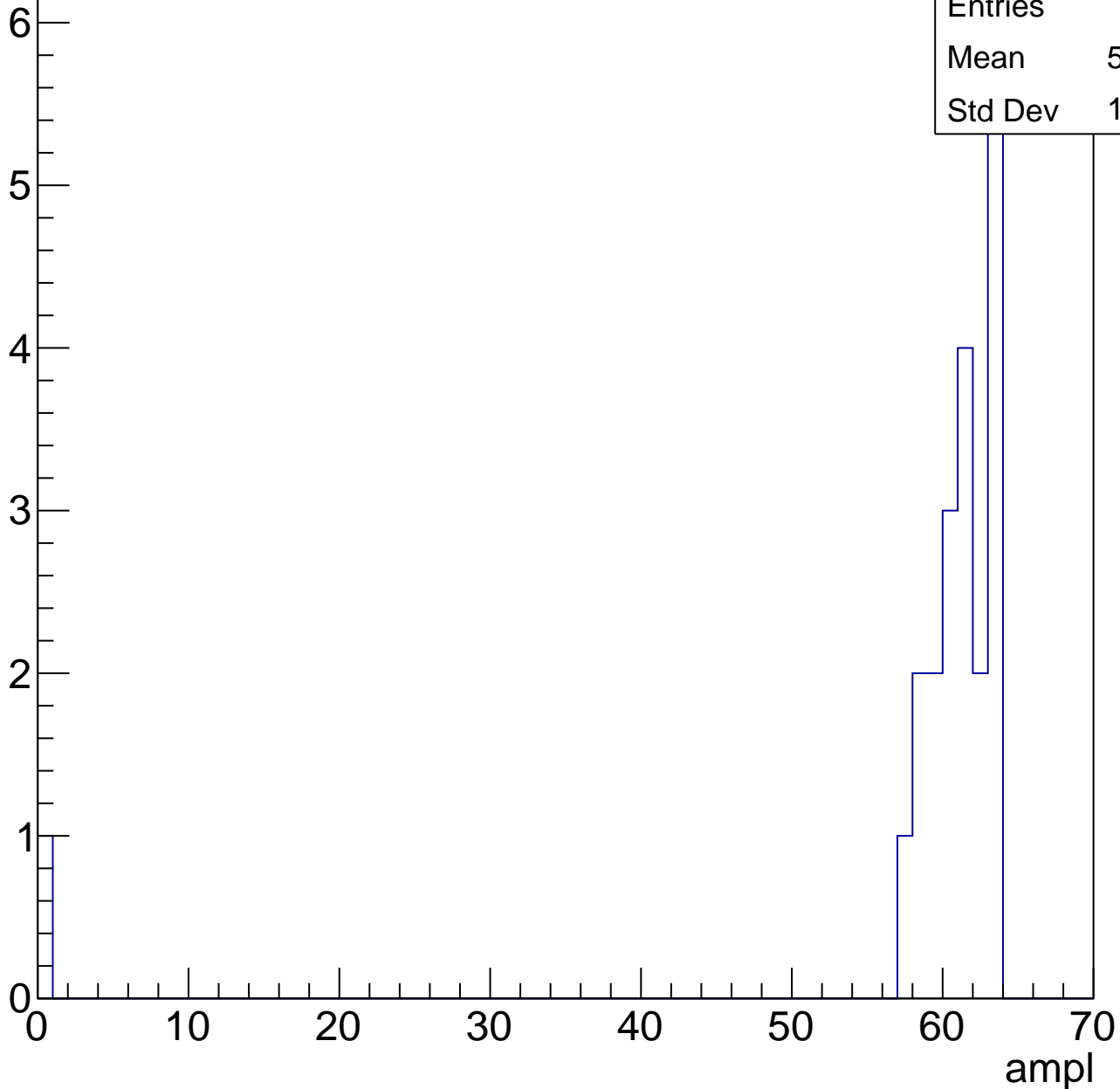


# B1L101S, U20-ch19, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	21
Mean	57.95
Std Dev	13.09



# B1L101S, U20-ch19, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

3  
2.5  
2  
1.5  
1  
0.5  
0

Entries	5
Mean	62.6
Std Dev	0.4899

ampl

0 10 20 30 40 50 60 70



# B1L101S, U20-ch19, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U20-ch20, adc0

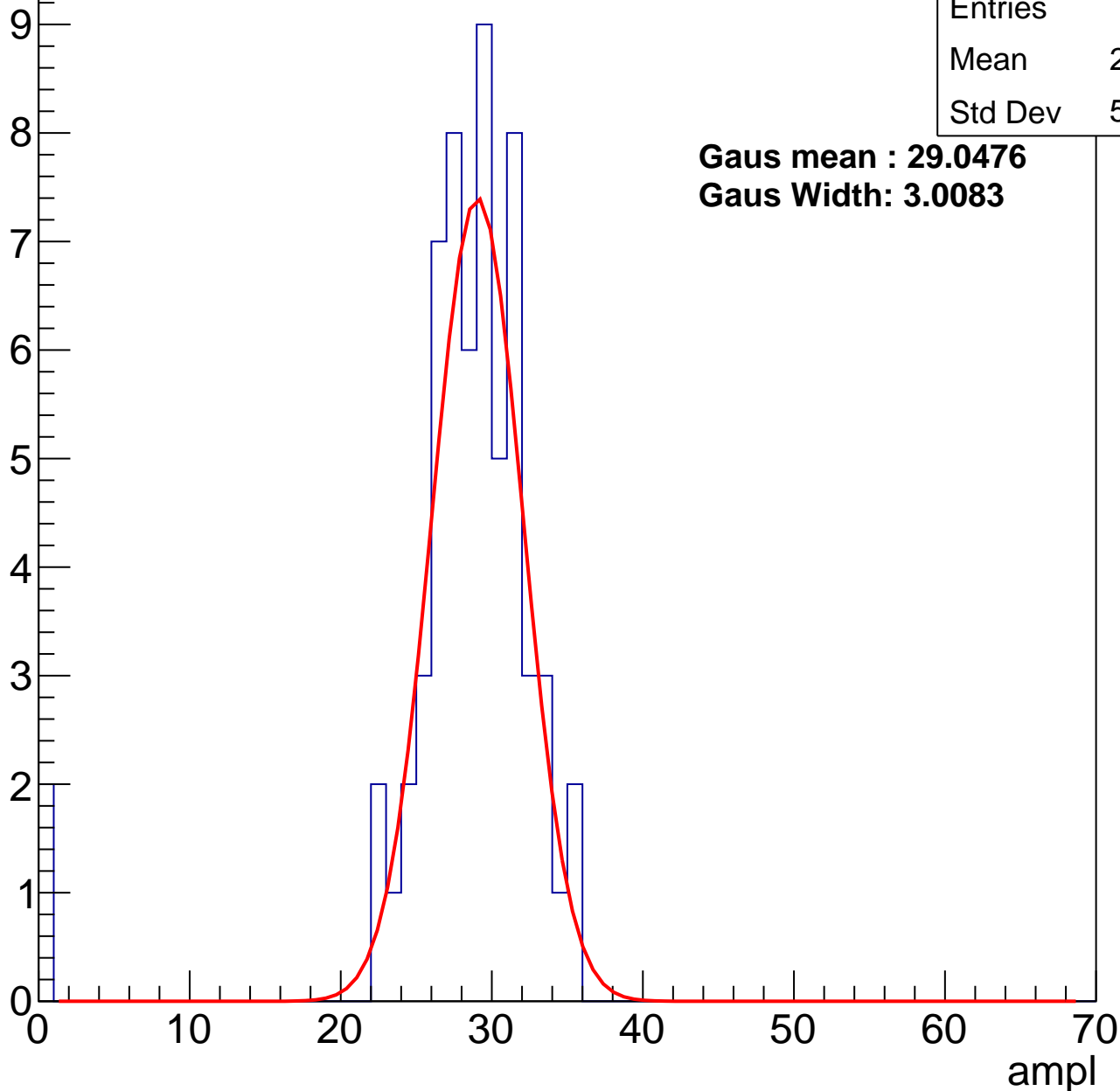
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	27.65
Std Dev	5.834

**Gaus mean : 29.0476**

**Gaus Width: 3.0083**



# B1L101S, U20-ch20, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	89
Mean	36.34
Std Dev	3.92

**Gaus mean : 36.5868**

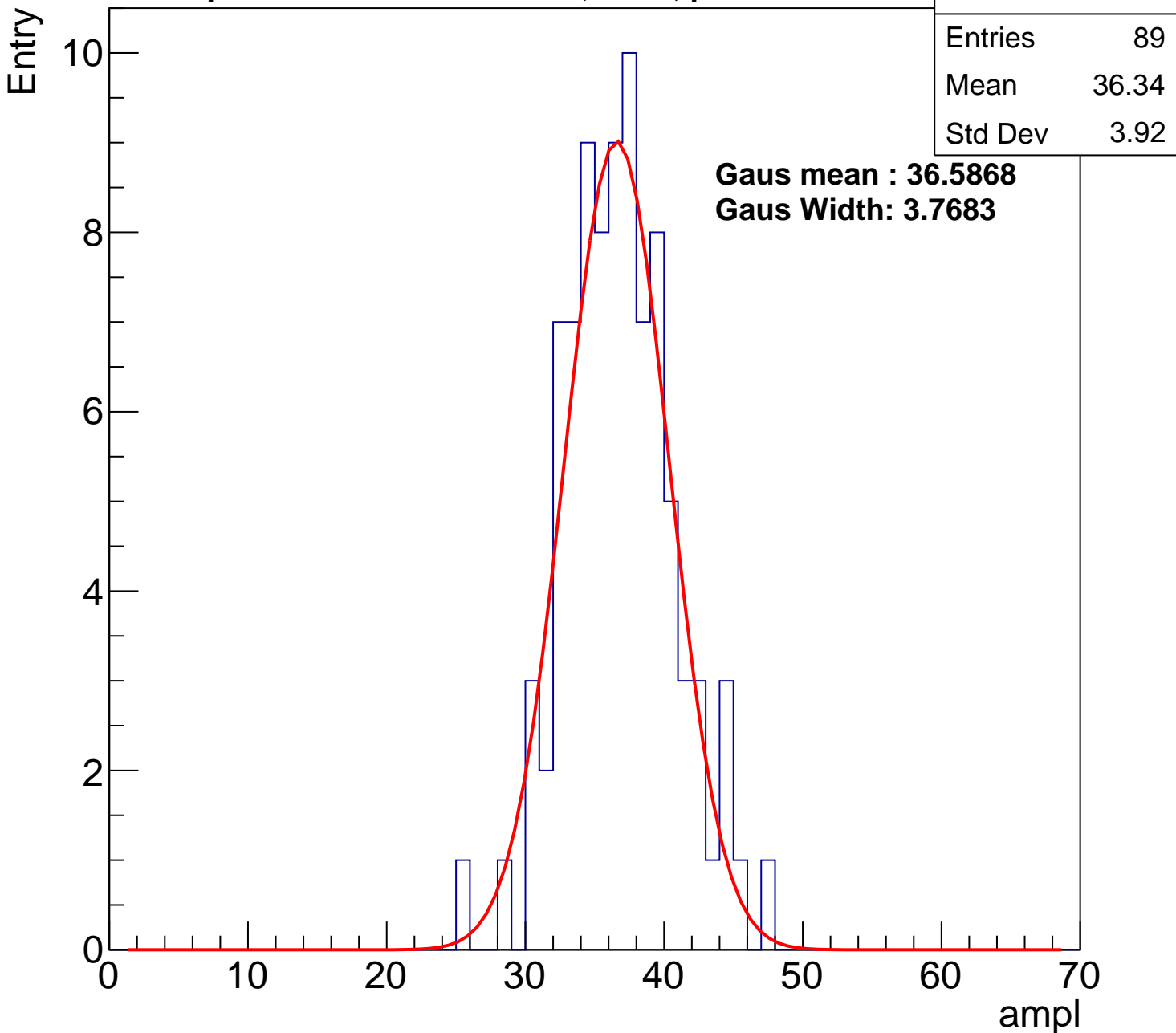
**Gaus Width: 3.7683**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U20-ch20, adc2

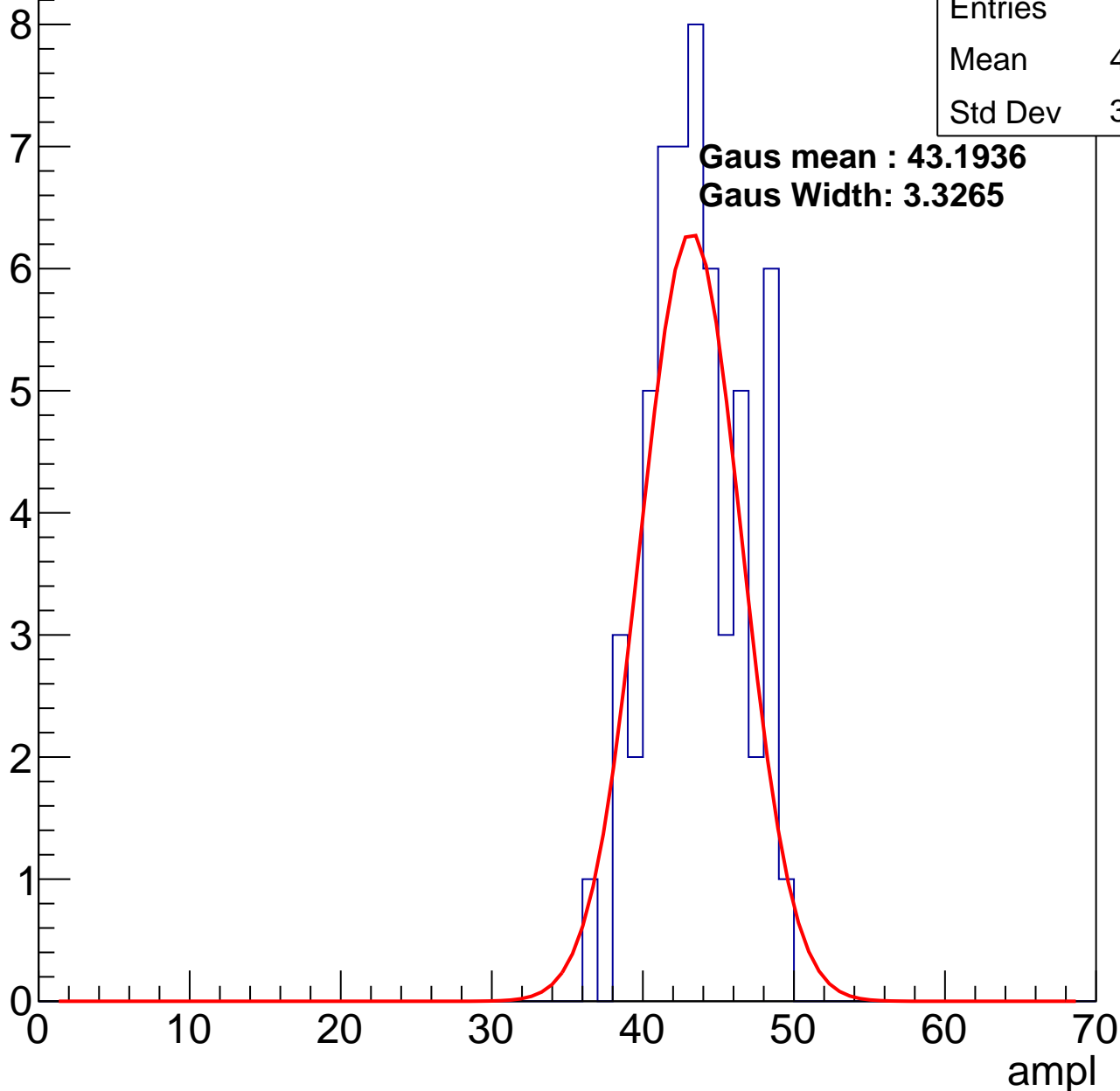
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	56
Mean	43.09
Std Dev	3.037

**Gaus mean : 43.1936**

**Gaus Width: 3.3265**



# B1L101S, U20-ch20, adc3

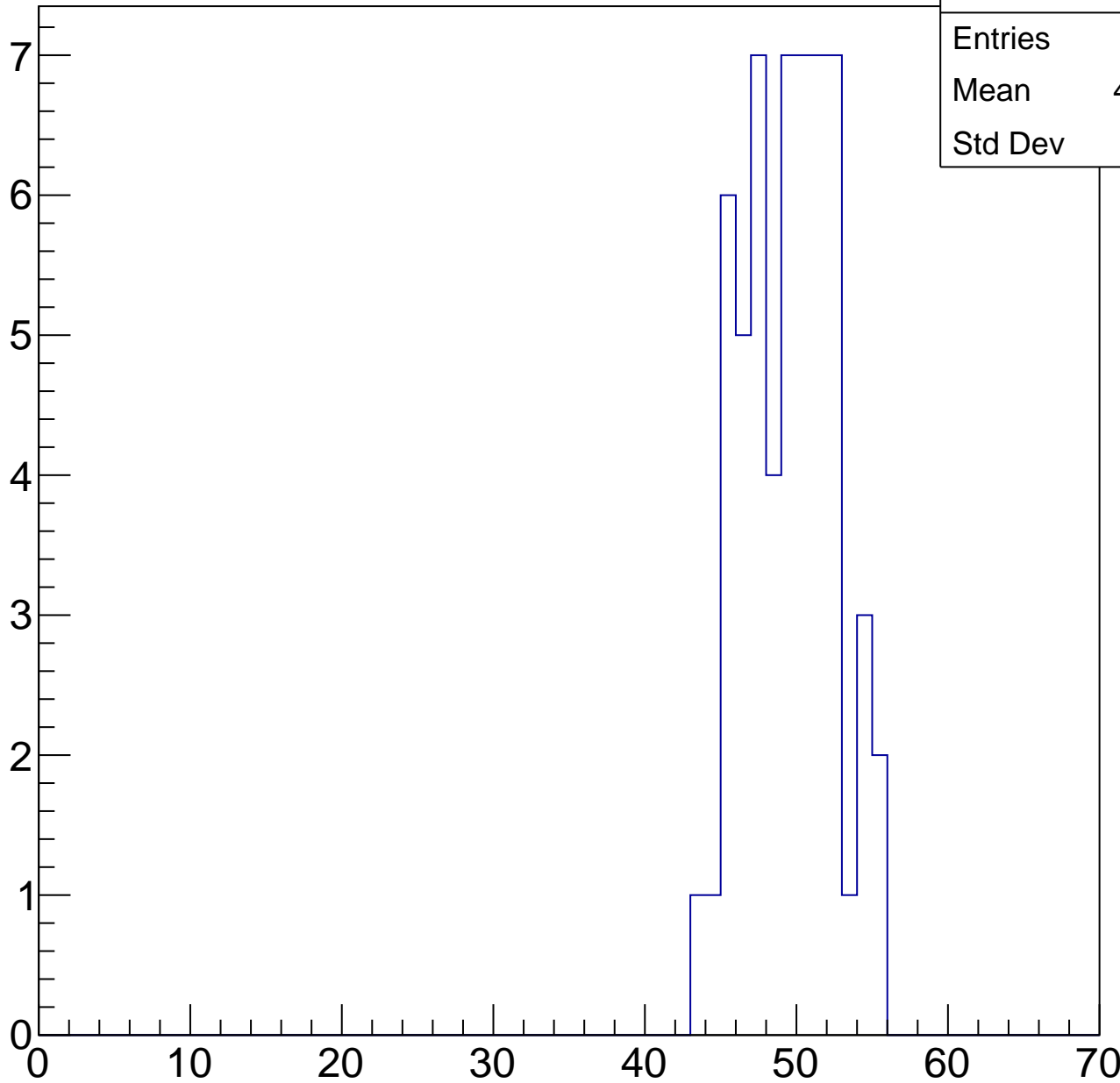
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

7  
6  
5  
4  
3  
2  
1  
0

Entries	58
Mean	49.09
Std Dev	2.92

ampl

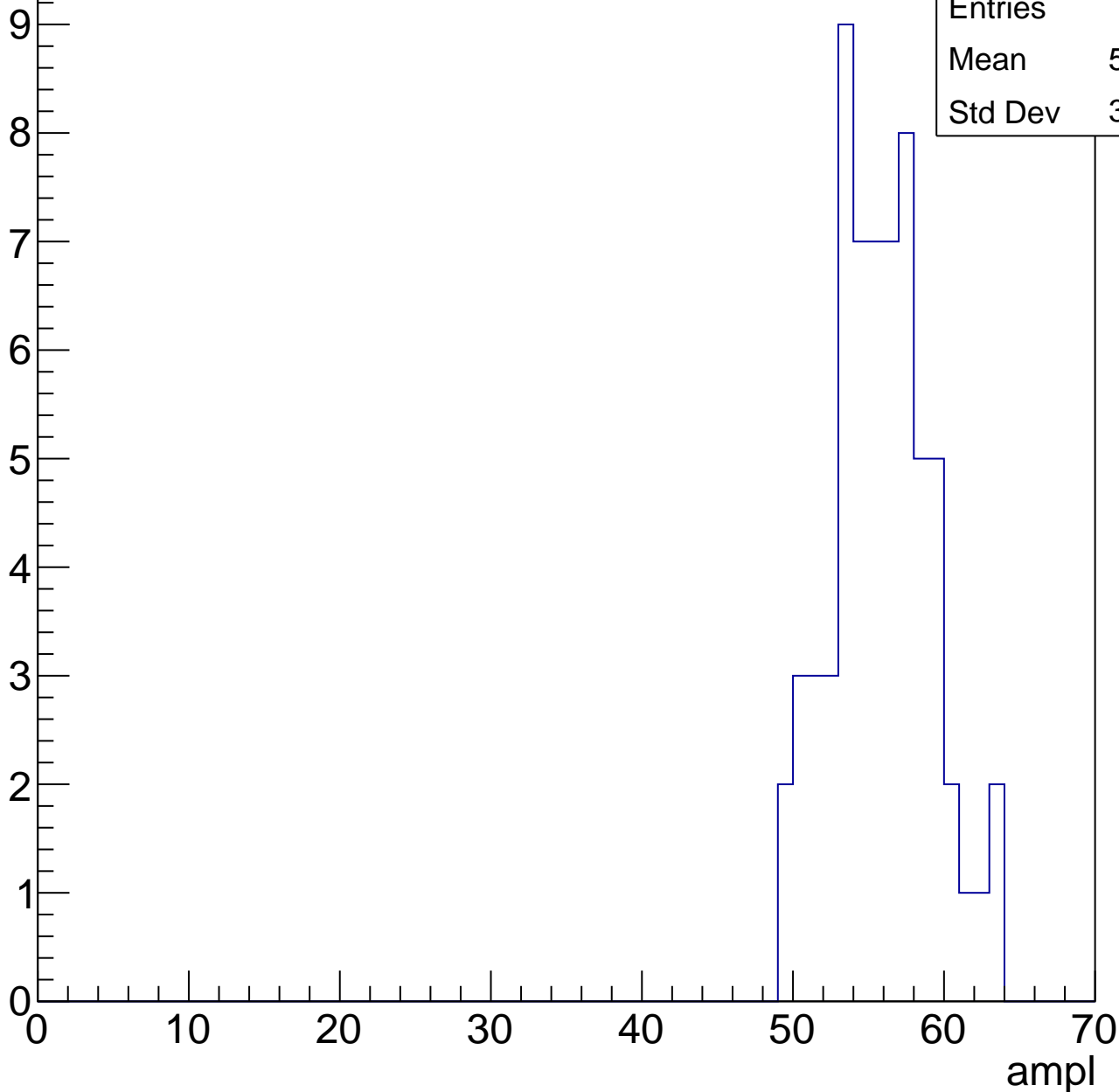


# B1L101S, U20-ch20, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	55.37
Std Dev	3.242

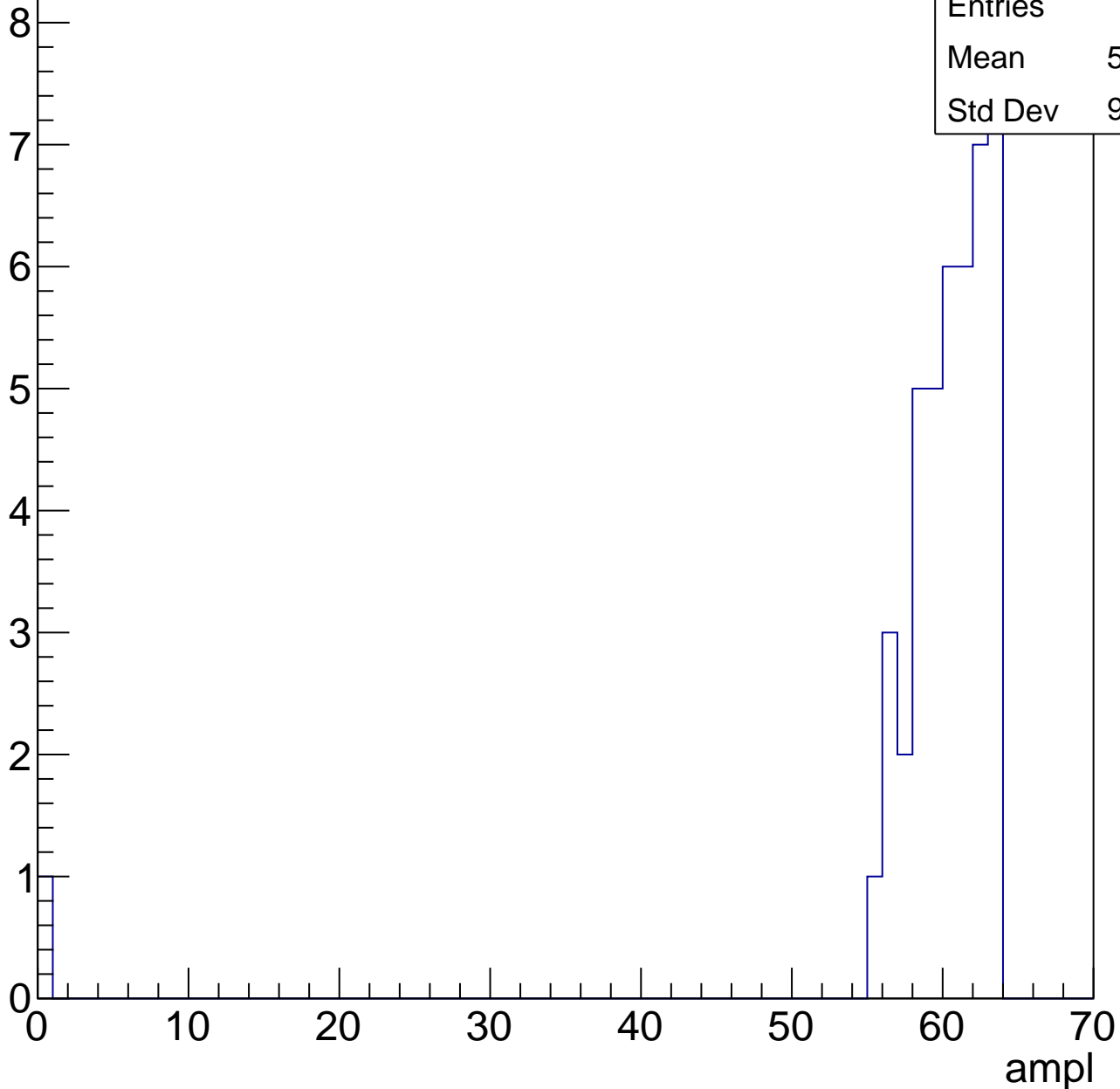


# B1L101S, U20-ch20, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

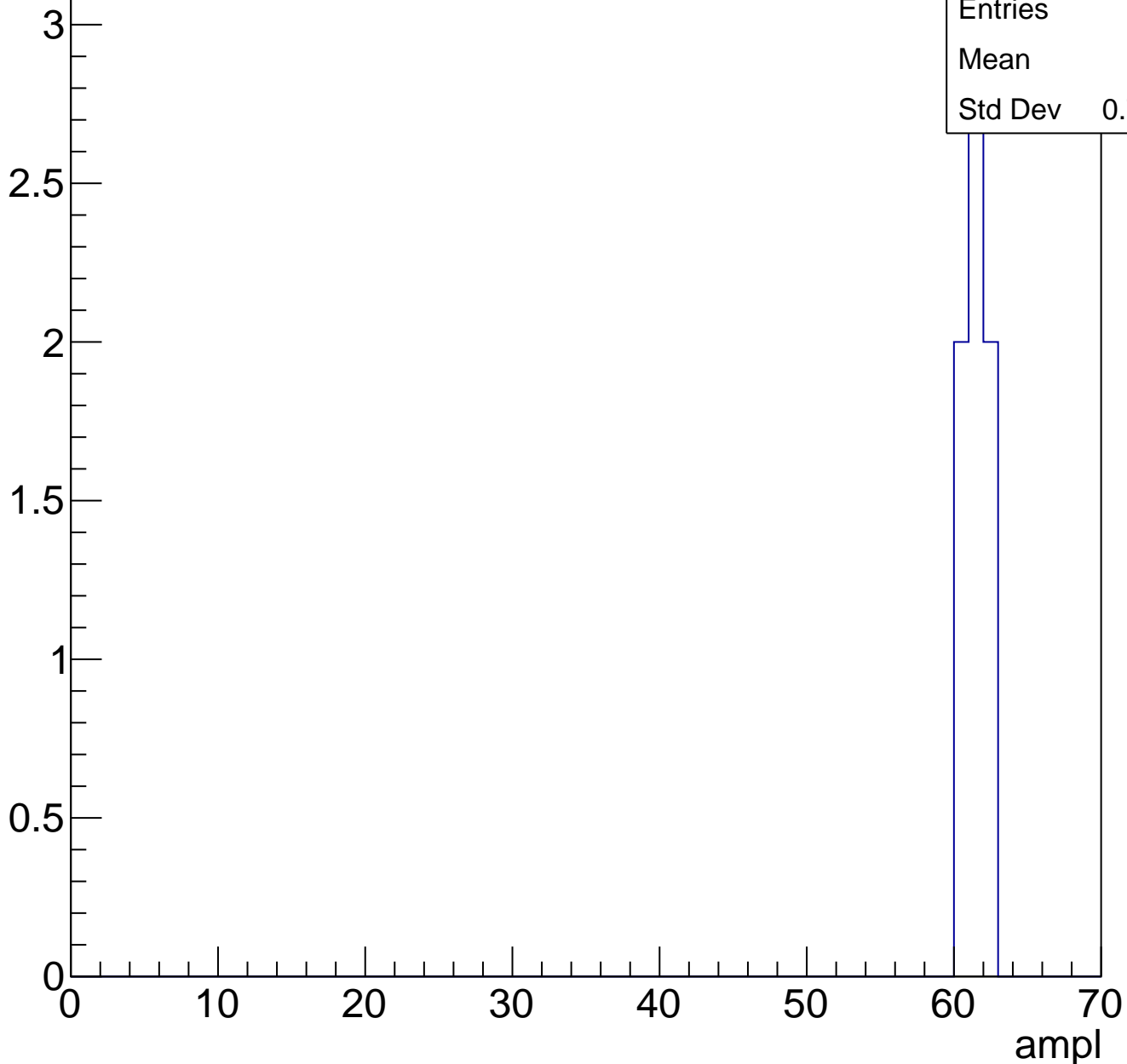
Entries	44
Mean	58.77
Std Dev	9.239



# B1L101S, U20-ch20, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U20-ch20, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

1

0.8

0.6

0.4

0.2

0

0

10

20

30

40

50

60

70

ampl

Entries

0

Mean

0

Std Dev

0

# B1L101S, U20-ch21, adc0

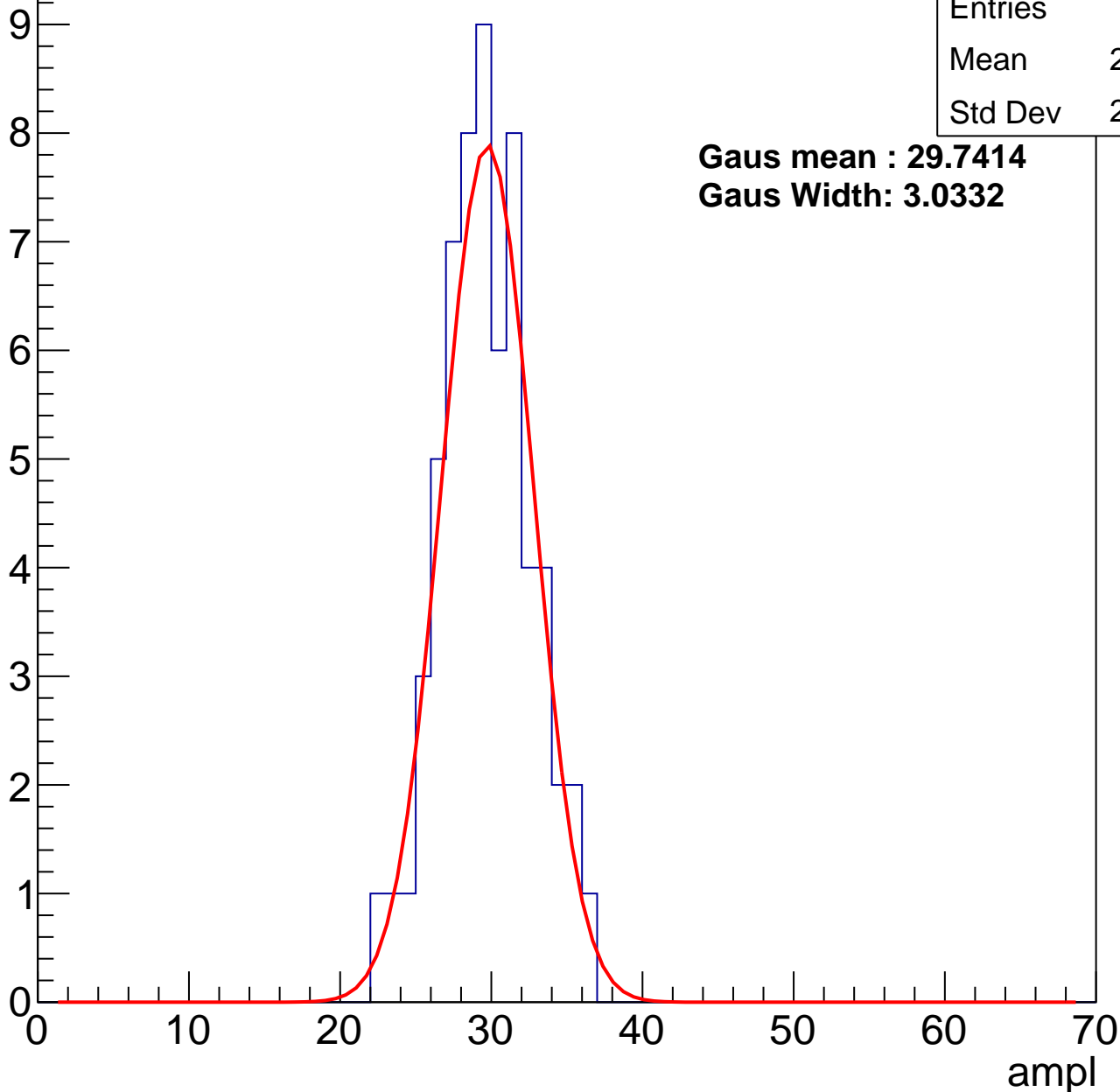
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	29.19
Std Dev	2.967

**Gaus mean : 29.7414**

**Gaus Width: 3.0332**



# B1L101S, U20-ch21, adc1

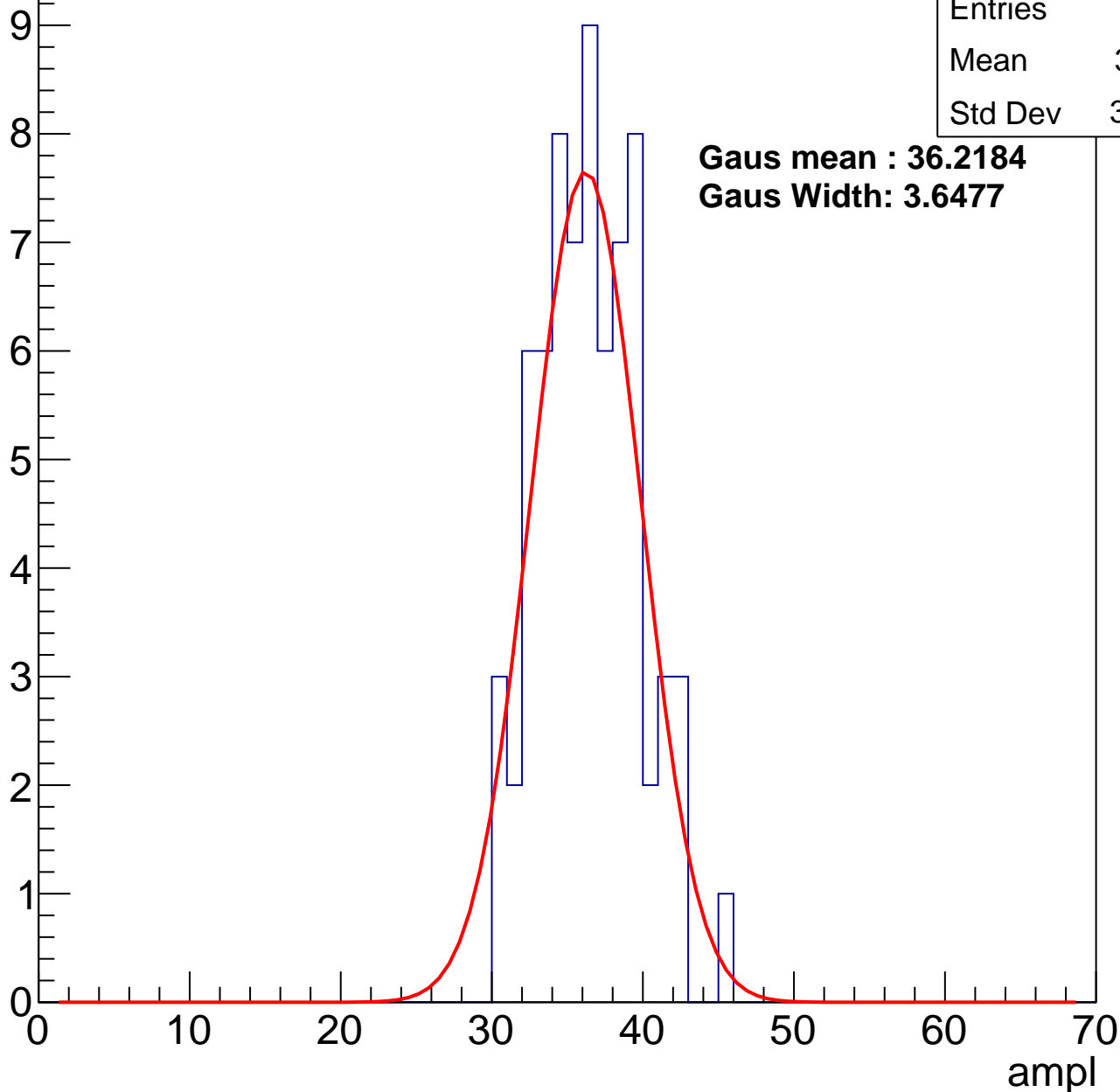
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	71
Mean	36.01
Std Dev	3.248

**Gaus mean : 36.2184**

**Gaus Width: 3.6477**



# B1L101S, U20-ch21, adc2

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	79
Mean	43.19
Std Dev	3.357

**Gaus mean : 43.9061**

**Gaus Width: 3.5637**

10

8

6

4

2

0

0

10

20

30

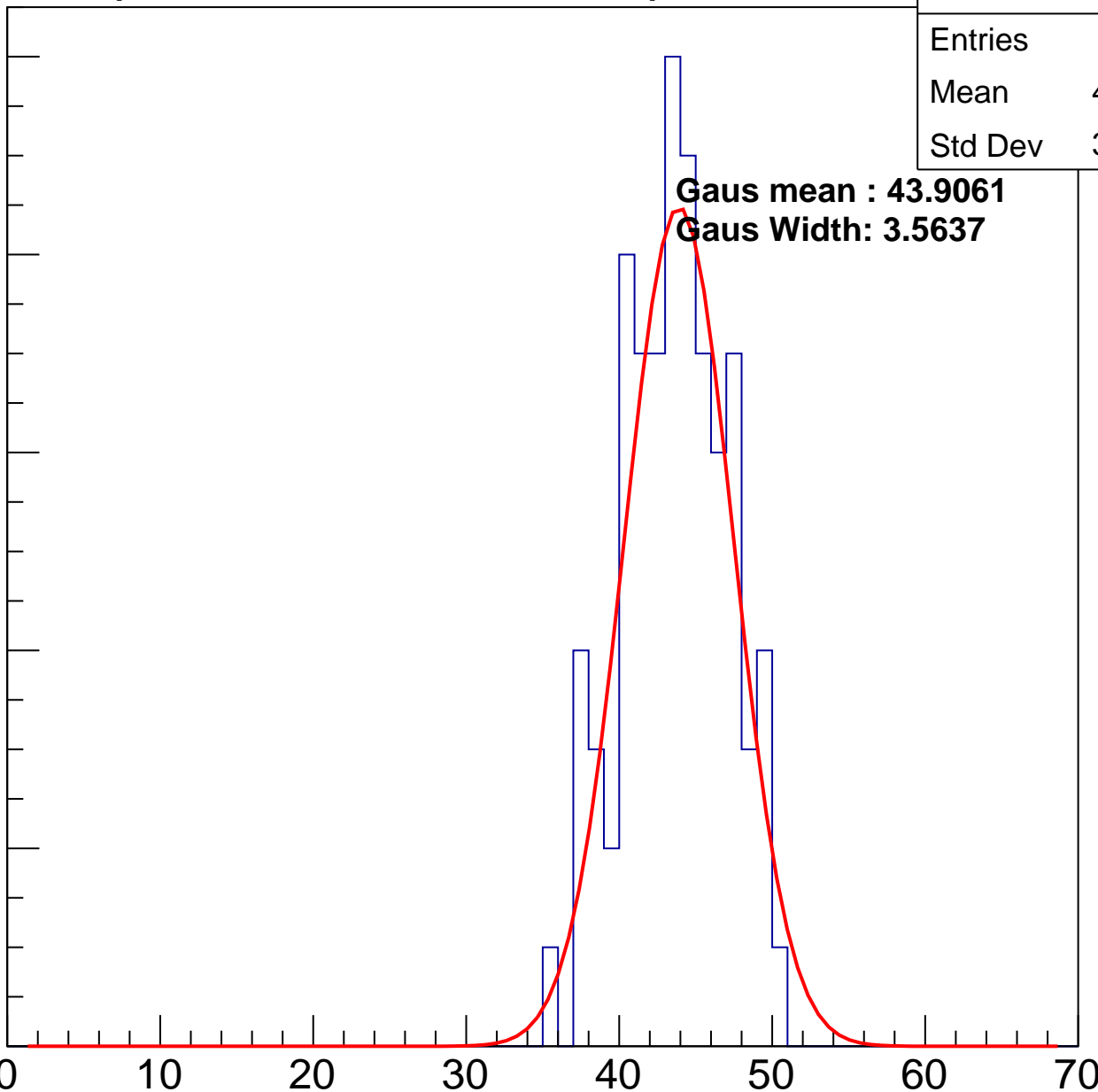
40

50

60

70

ampl

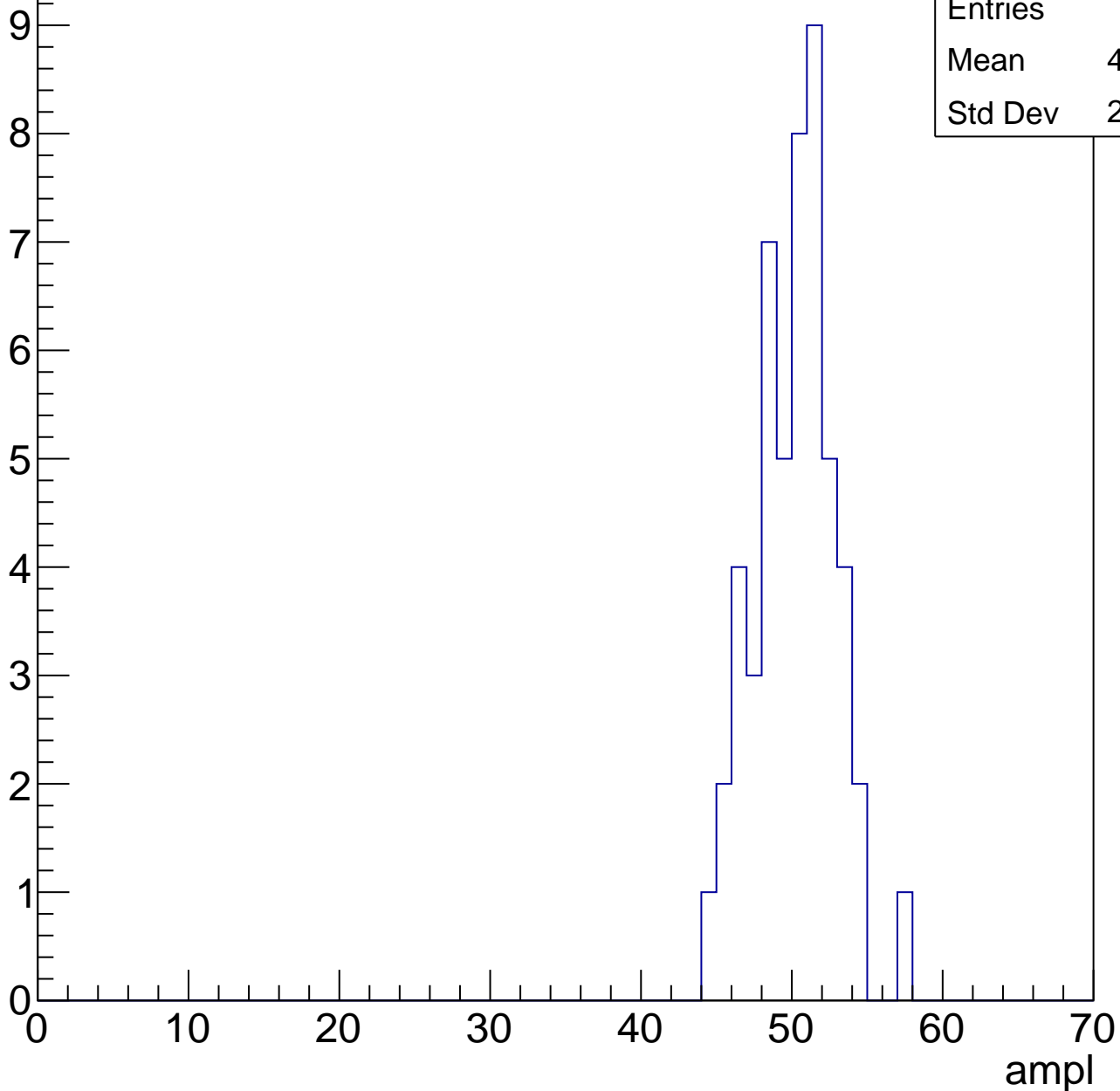


# B1L101S, U20-ch21, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

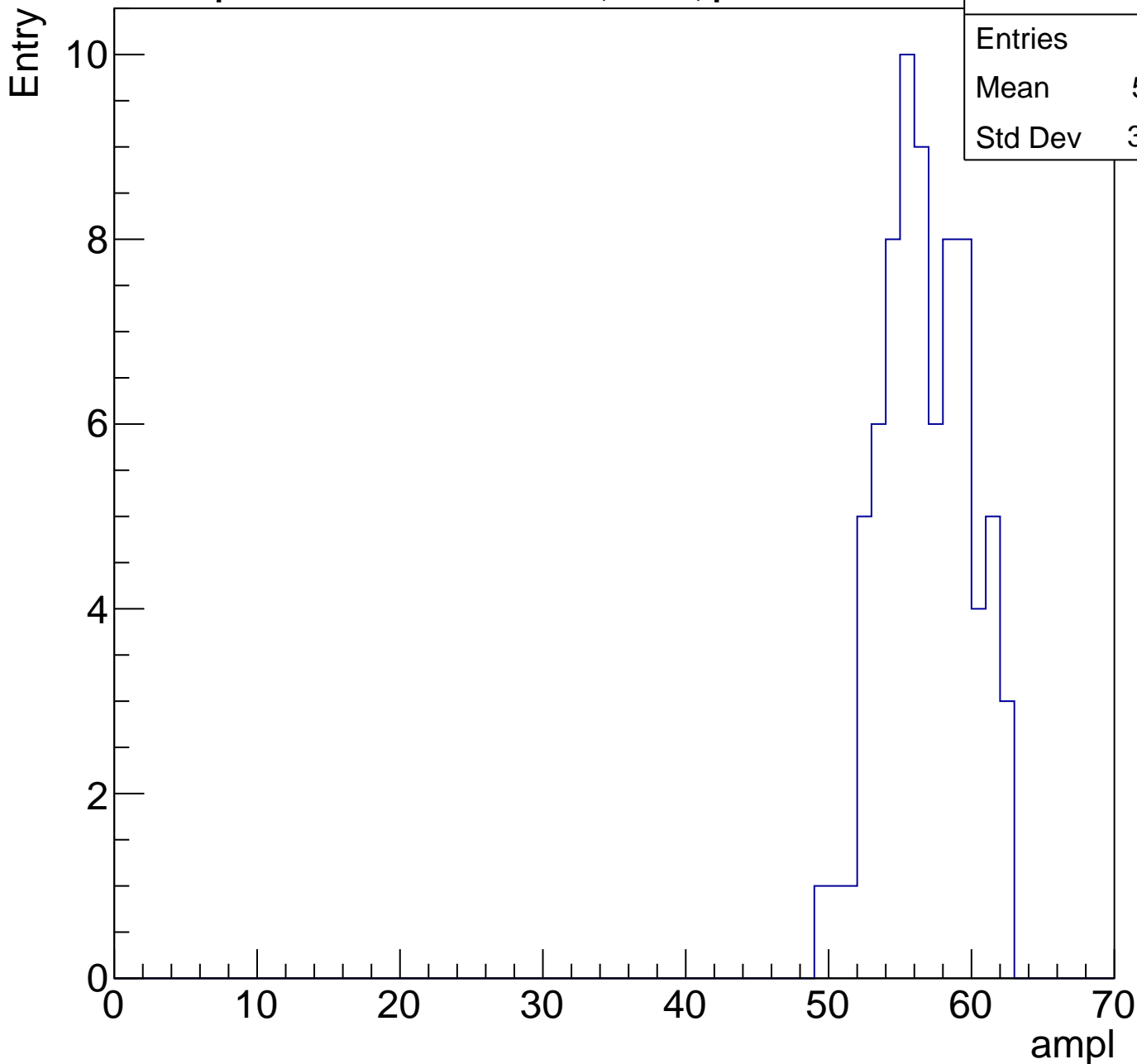
Entries	51
Mean	49.73
Std Dev	2.628



# B1L101S, U20-ch21, adc4

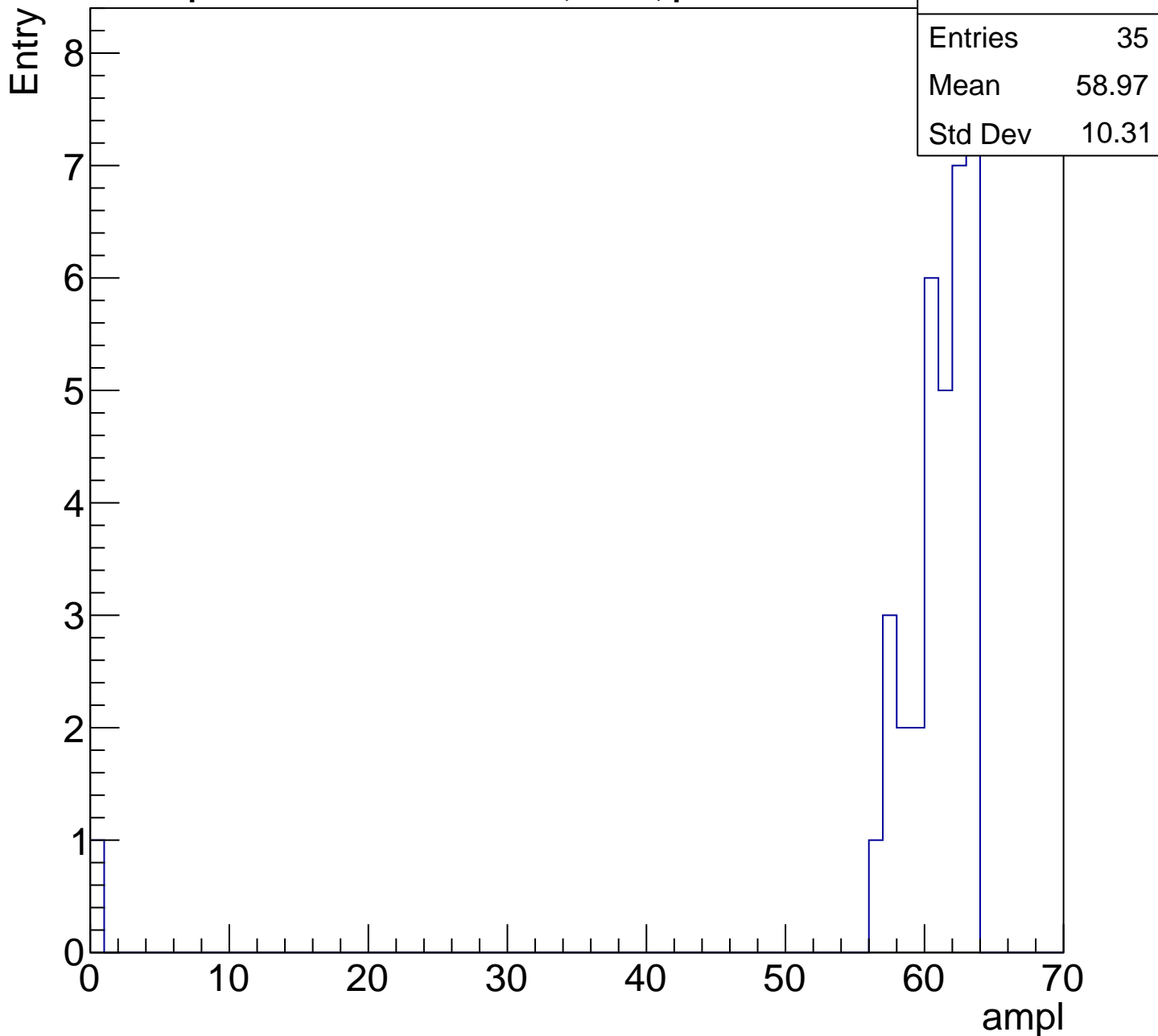
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	75
Mean	56.31
Std Dev	3.024



# B1L101S, U20-ch21, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U20-ch21, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	2
Mean	63
Std Dev	0

0 10 20 30 40 50 60 70

ampl



# B1L101S, U20-ch21, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U20-ch22, adc0

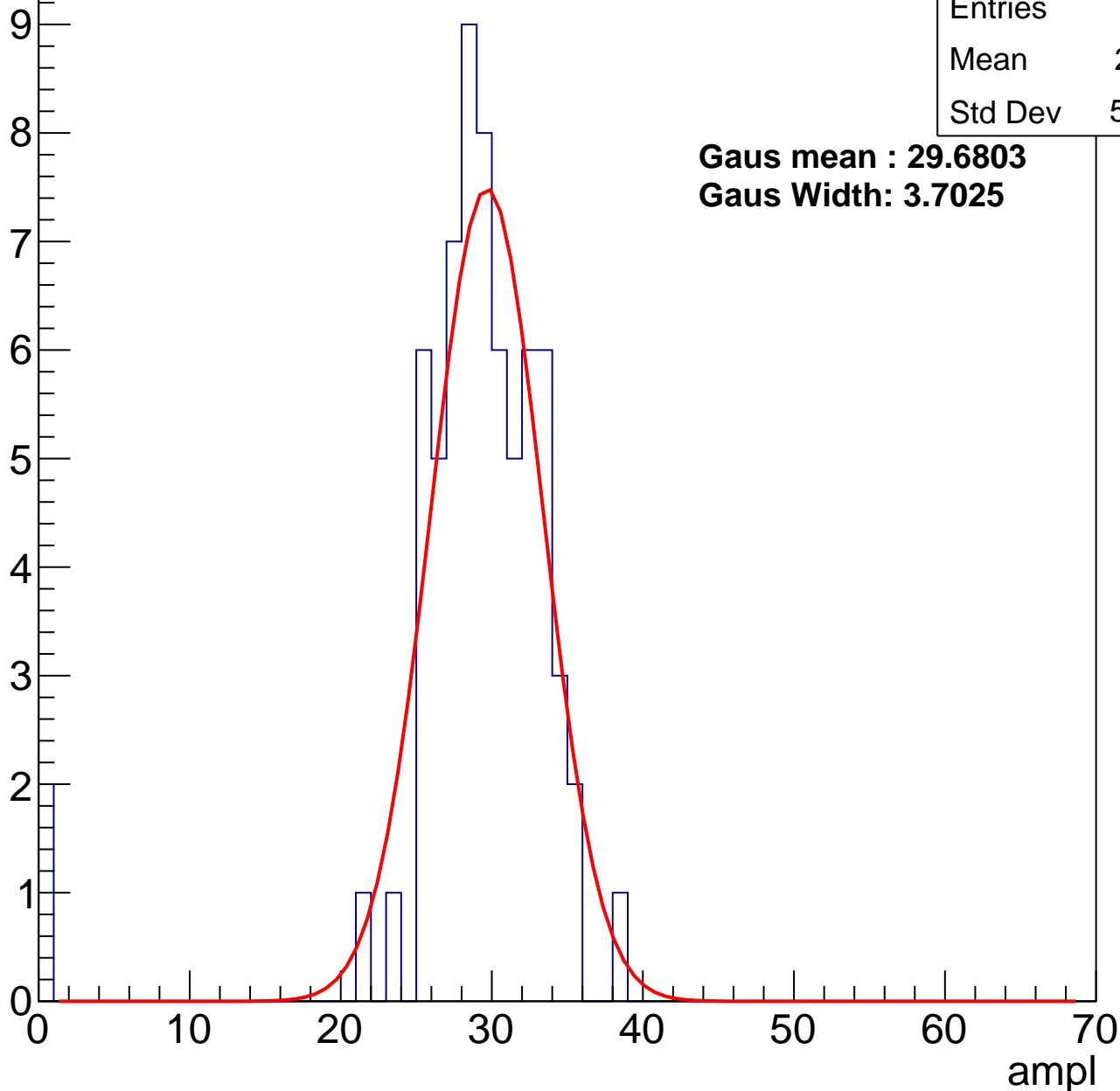
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	28.41
Std Dev	5.867

**Gaus mean : 29.6803**

**Gaus Width: 3.7025**



# B1L101S, U20-ch22, adc1

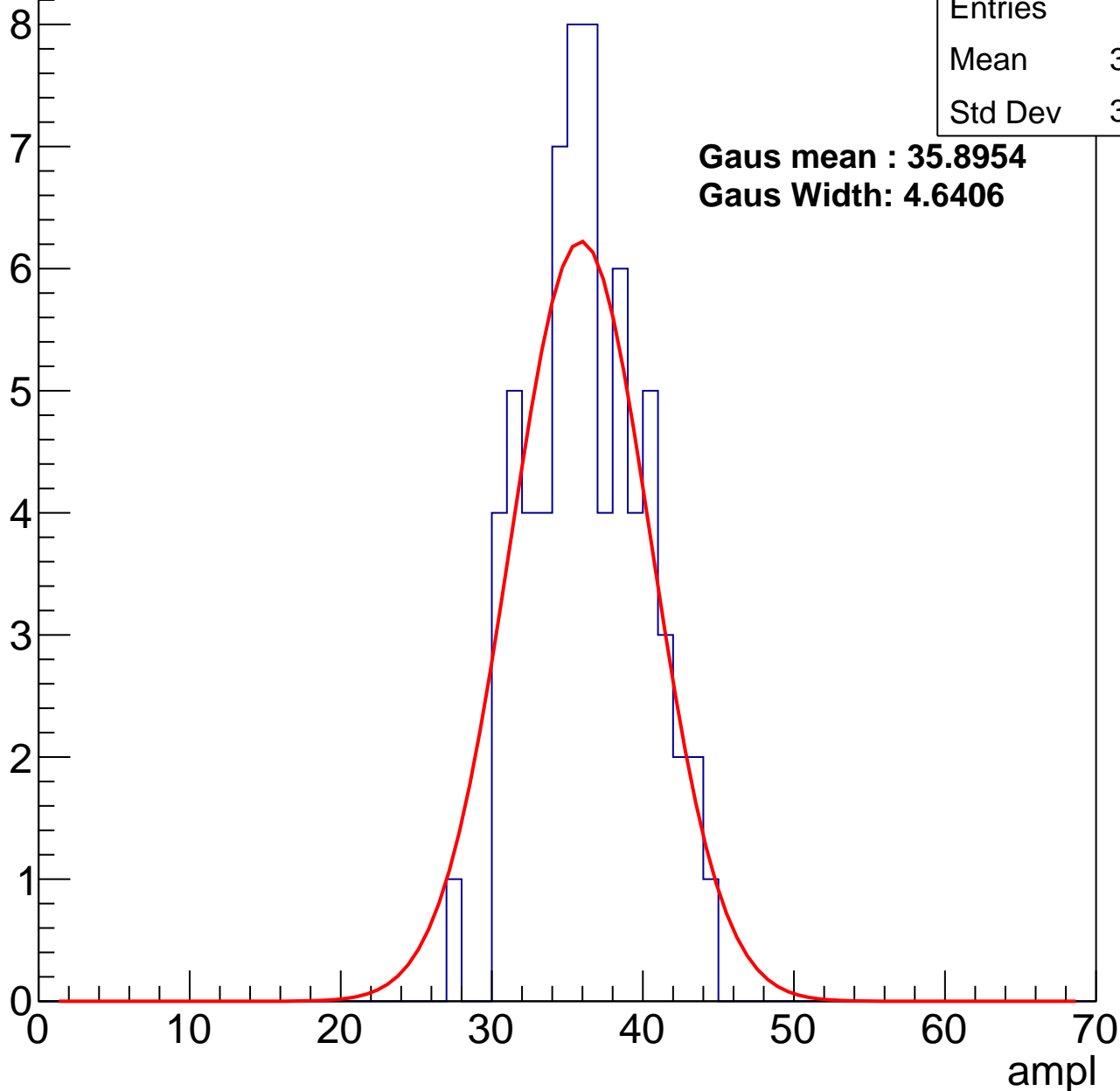
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	35.84
Std Dev	3.712

**Gaus mean : 35.8954**

**Gaus Width: 4.6406**



# B1L101S, U20-ch22, adc2

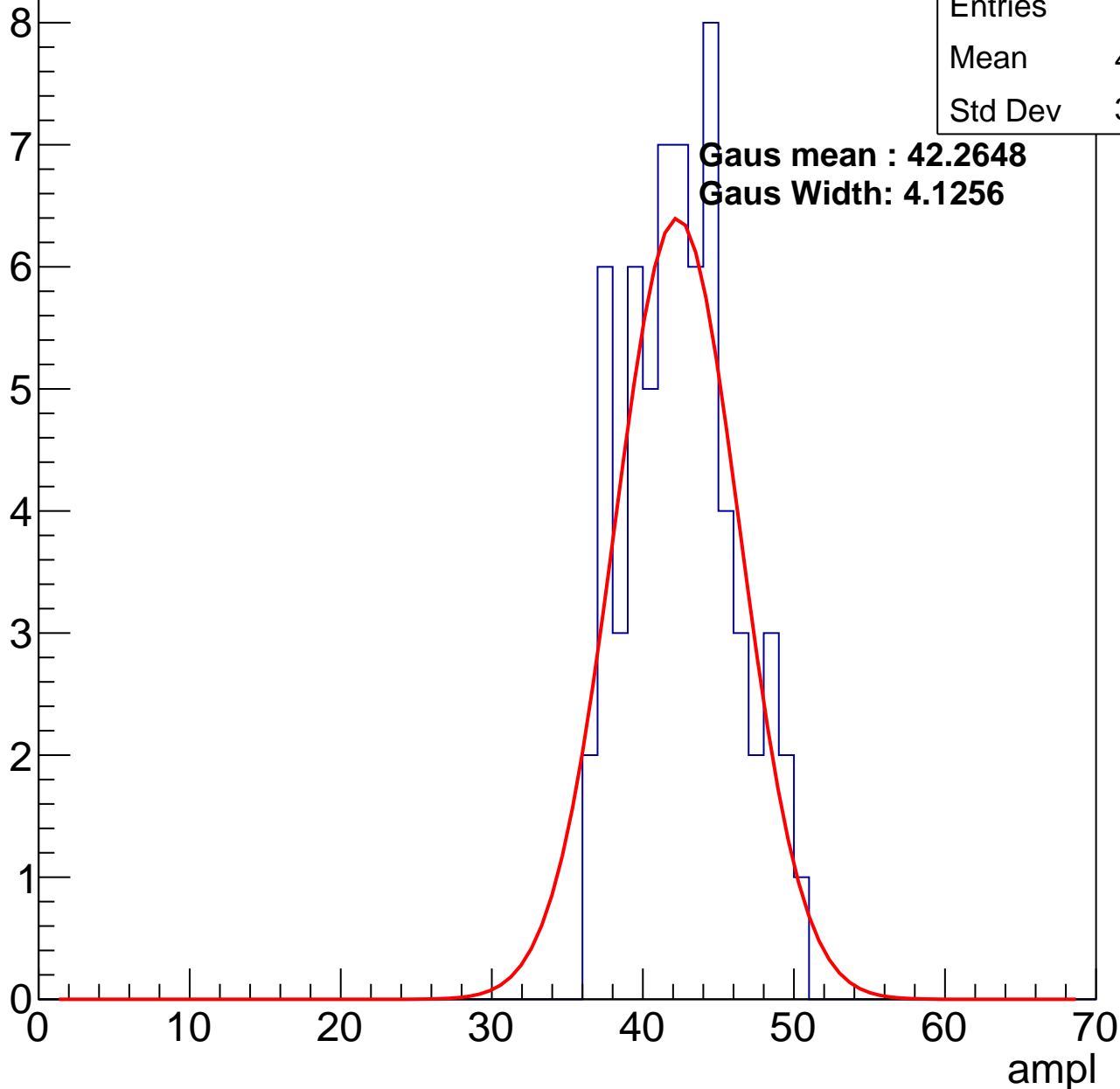
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	42.11
Std Dev	3.491

**Gaus mean : 42.2648**

**Gaus Width: 4.1256**

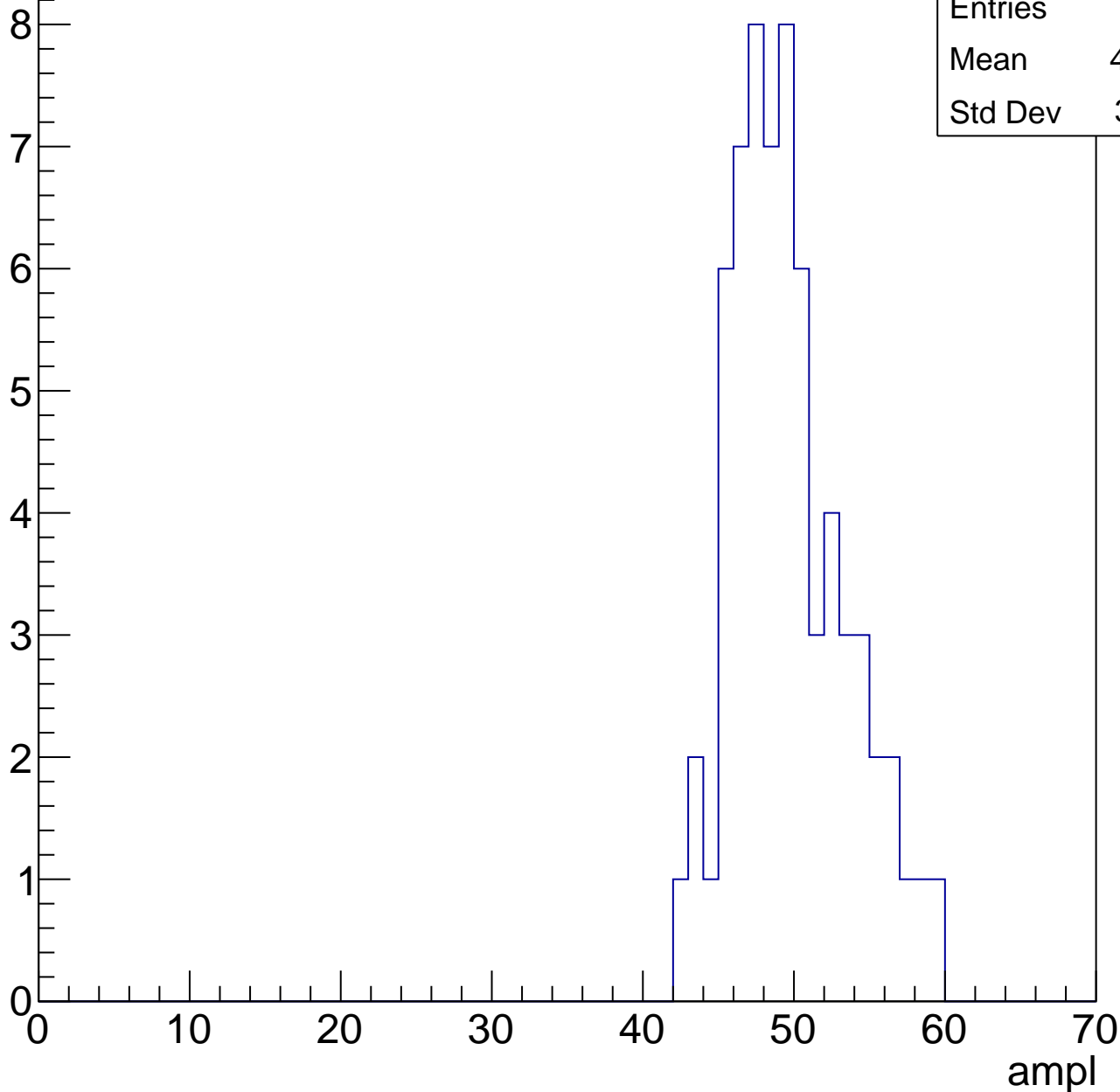


# B1L101S, U20-ch22, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	66
Mean	49.18
Std Dev	3.761

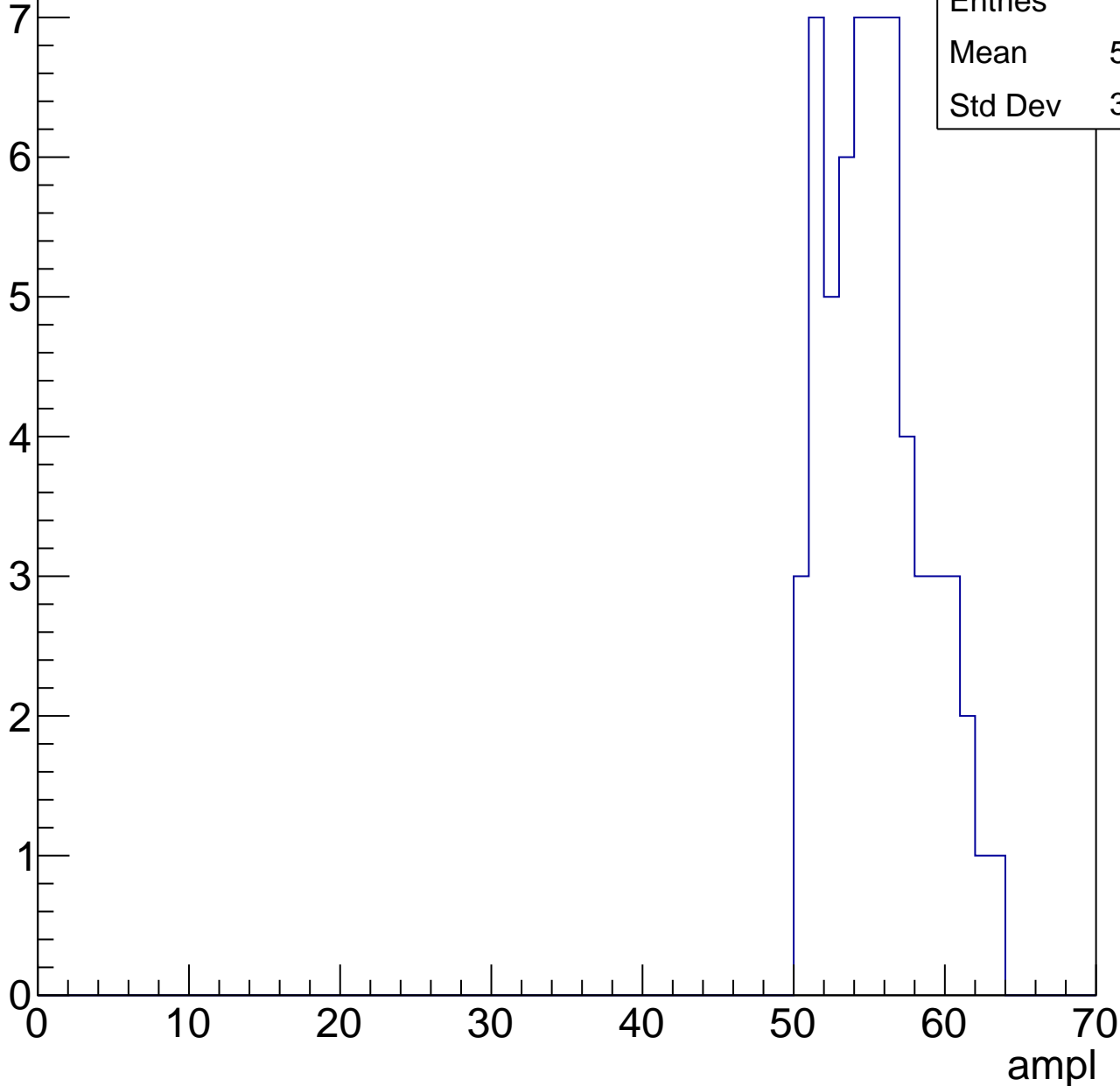


# B1L101S, U20-ch22, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	59
Mean	55.02
Std Dev	3.244

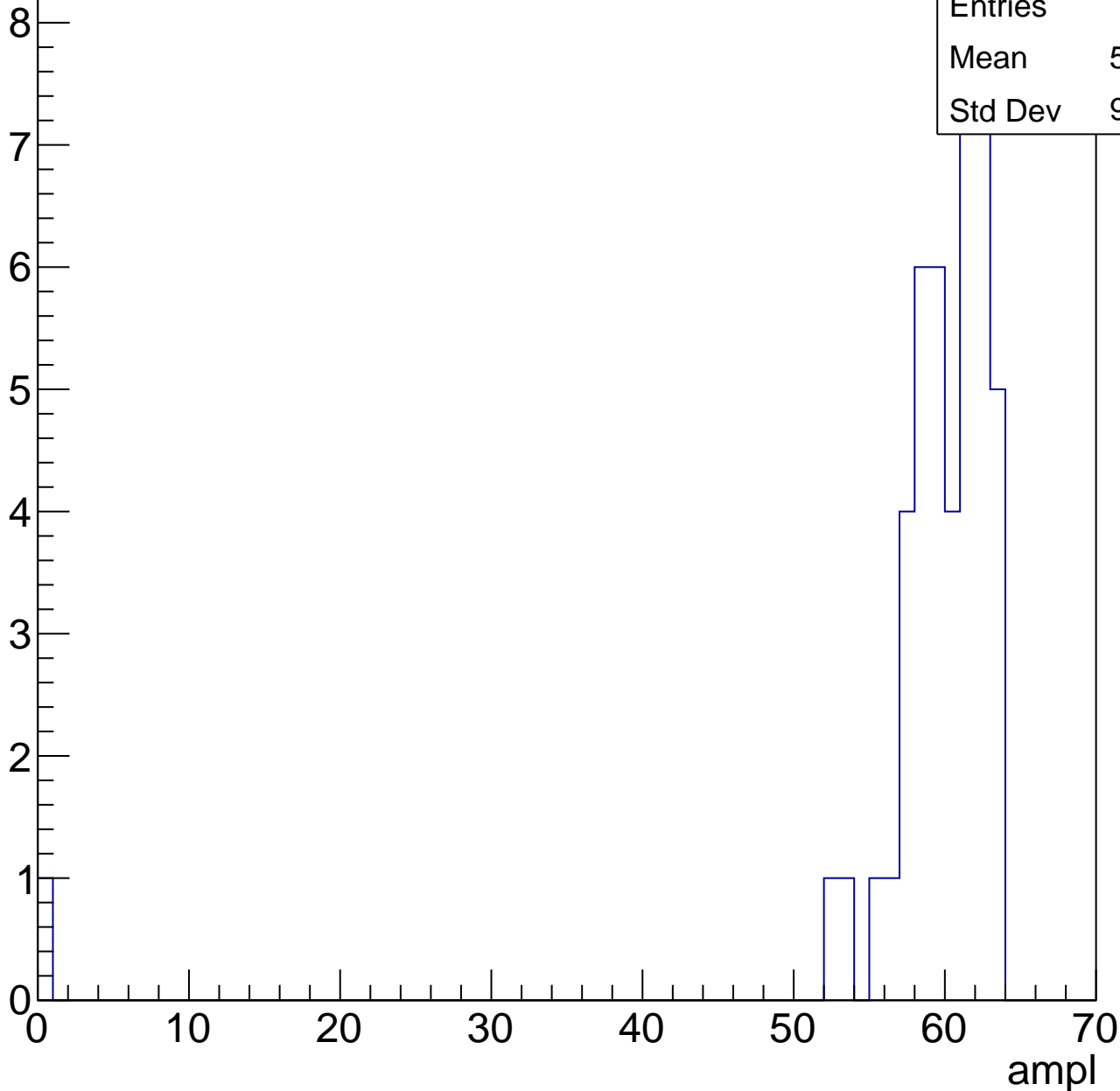


# B1L101S, U20-ch22, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

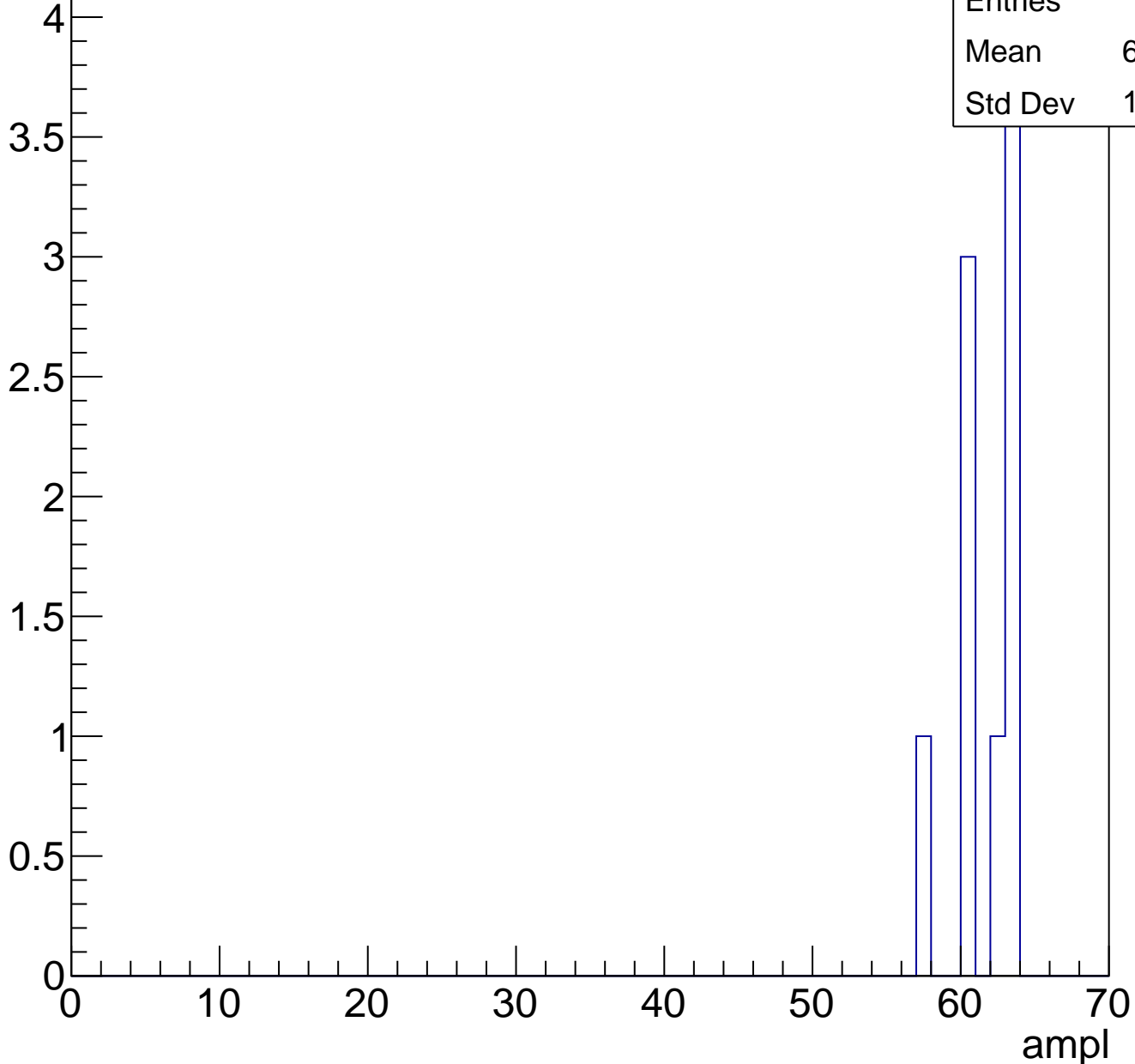
Entries	46
Mean	58.37
Std Dev	9.068



# B1L101S, U20-ch22, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	9
Mean	61.22
Std Dev	1.988



# B1L101S, U20-ch22, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U20-ch23, adc0

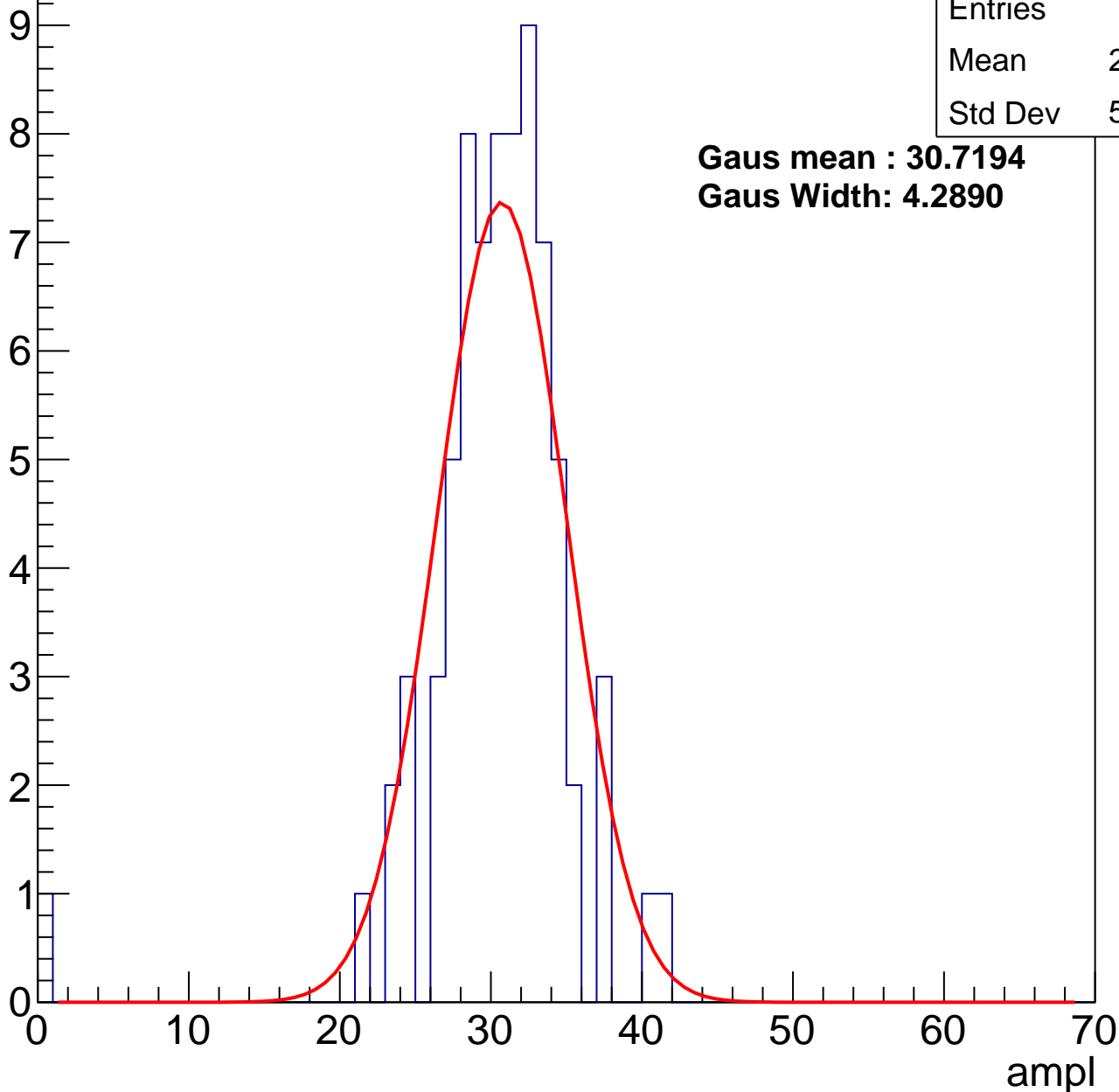
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	74
Mean	29.97
Std Dev	5.099

**Gaus mean : 30.7194**

**Gaus Width: 4.2890**



# B1L101S, U20-ch23, adc1

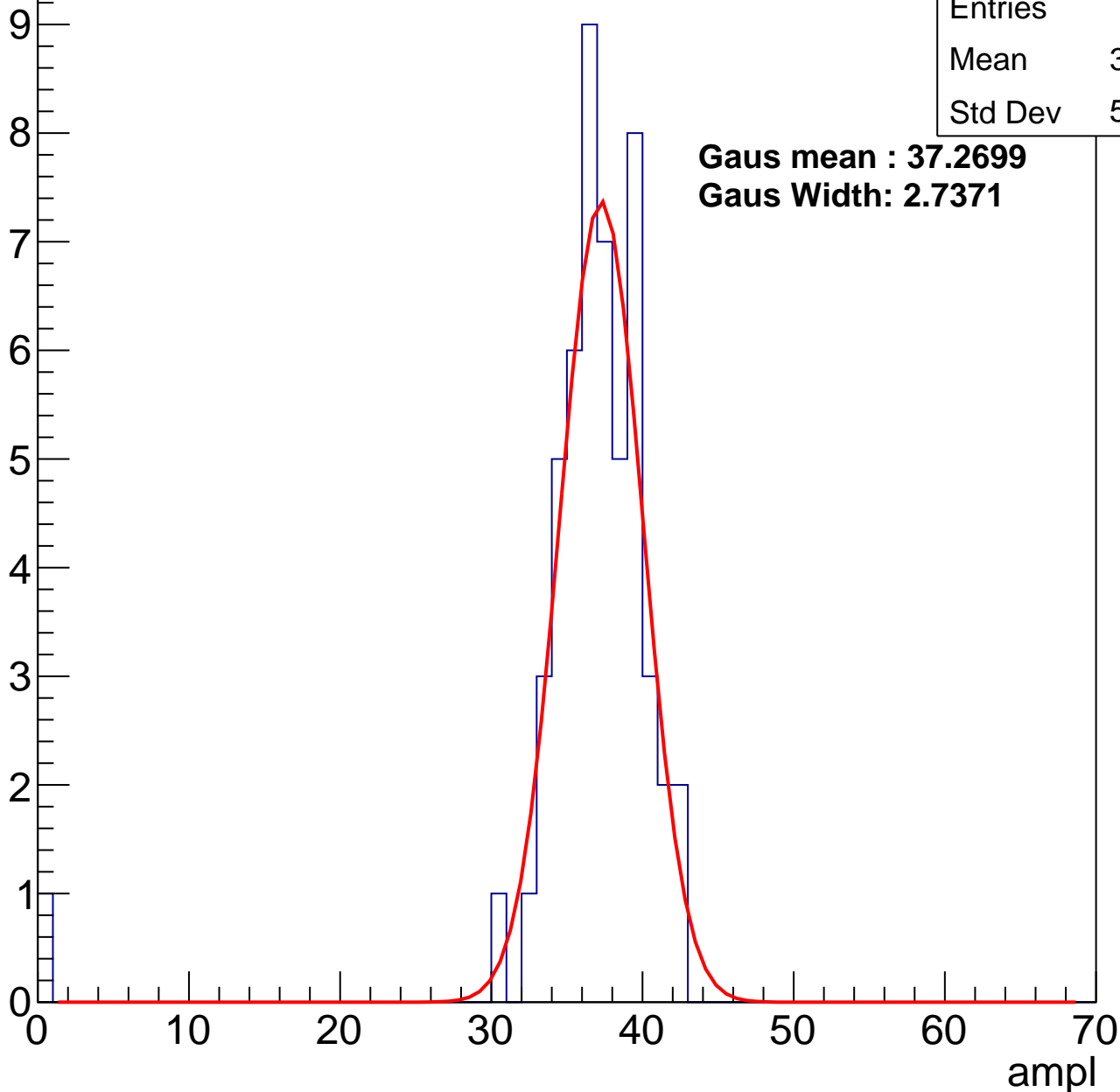
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	53
Mean	36.08
Std Dev	5.613

**Gaus mean : 37.2699**

**Gaus Width: 2.7371**



# B1L101S, U20-ch23, adc2

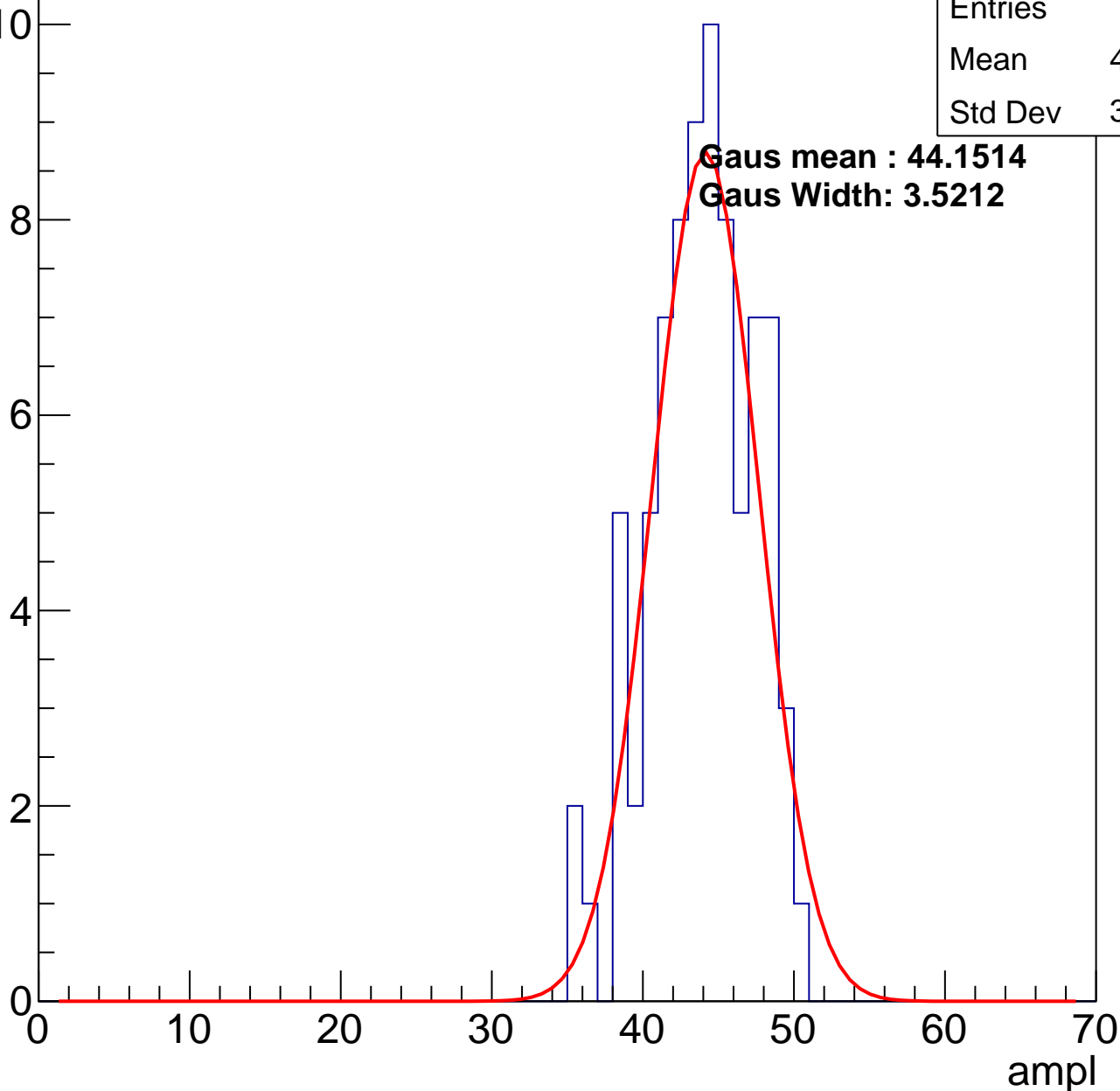
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	80
Mean	43.45
Std Dev	3.409

**Gaus mean : 44.1514**

**Gaus Width: 3.5212**



# B1L101S, U20-ch23, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	71
Mean	50.77
Std Dev	3.303

Entry

10

8

6

4

2

0

0

10

20

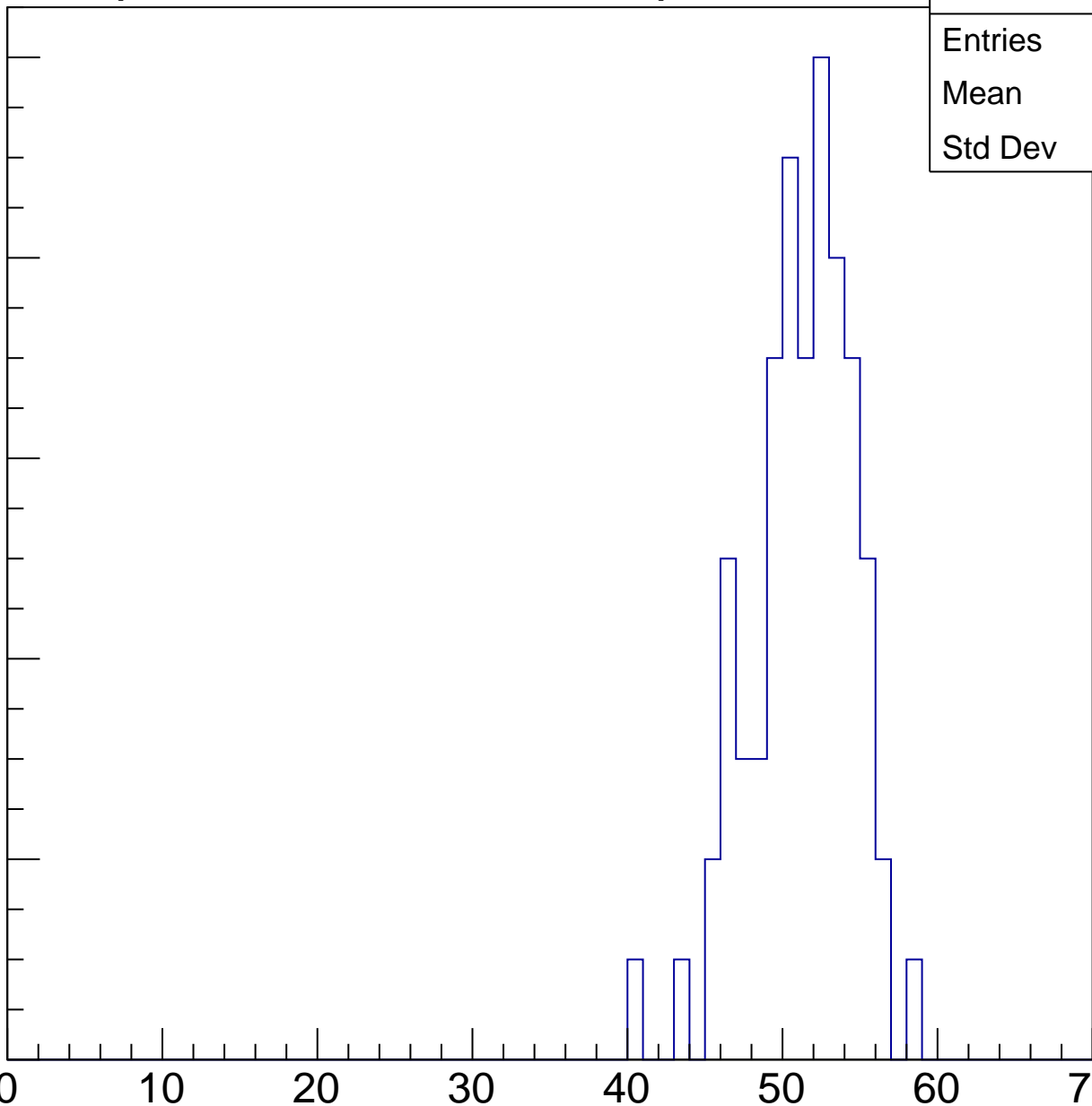
30

40

50

60

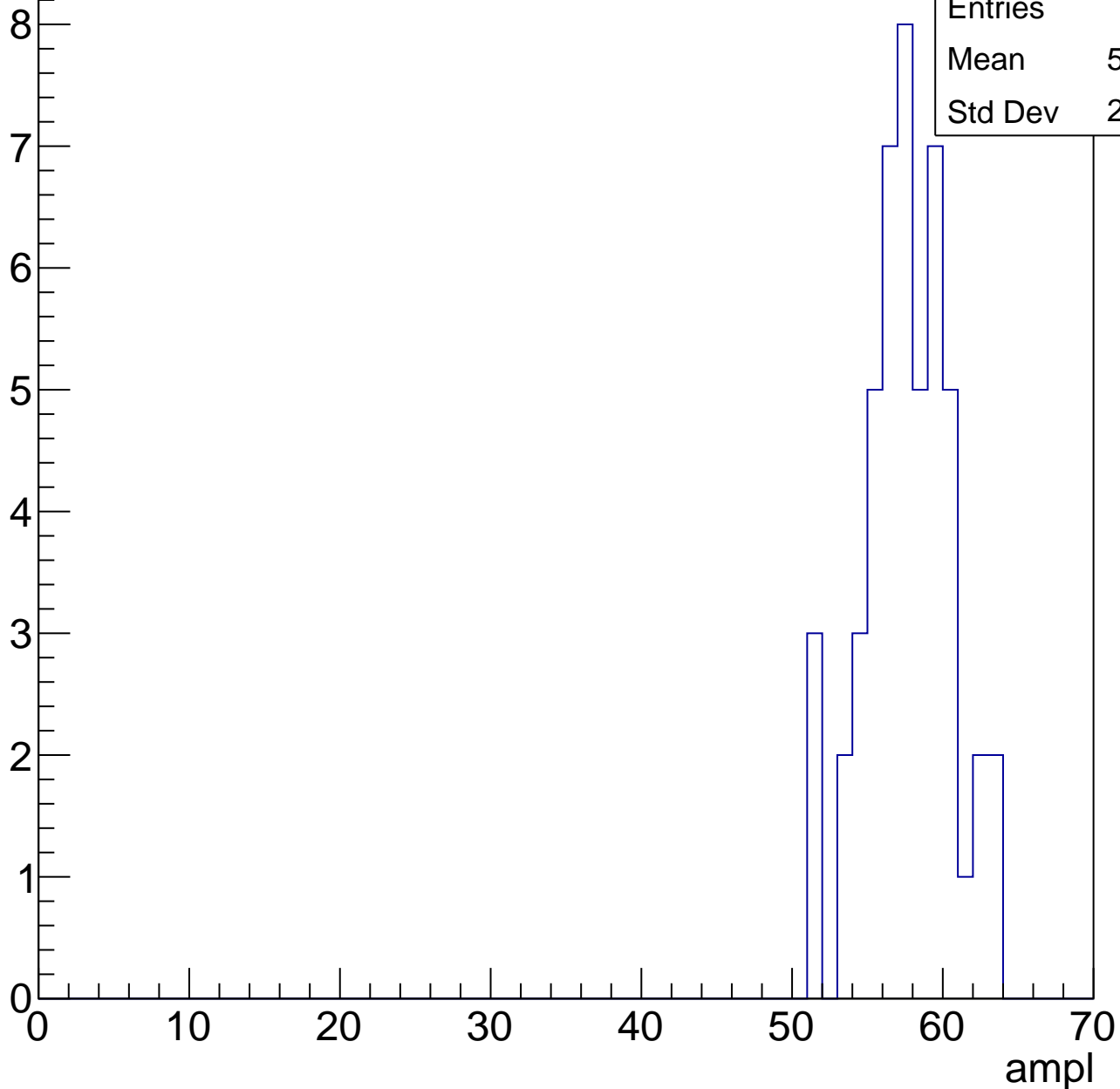
ampl



# B1L101S, U20-ch23, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

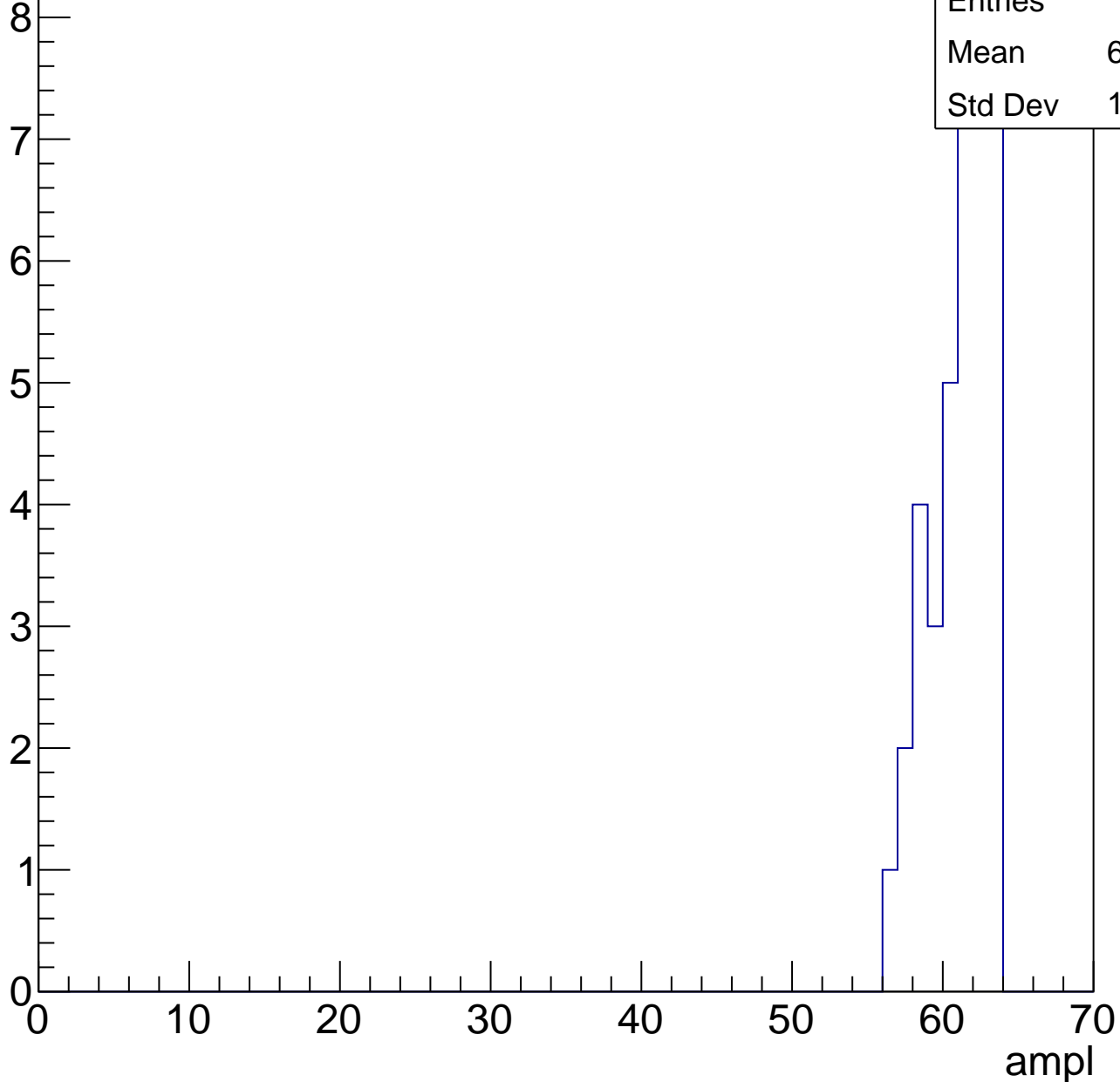
Entry



# B1L101S, U20-ch23, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U20-ch23, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U20-ch23, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L101S, U20-ch24, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	66
Mean	29.03
Std Dev	4.899

**Gaus mean : 29.8197**

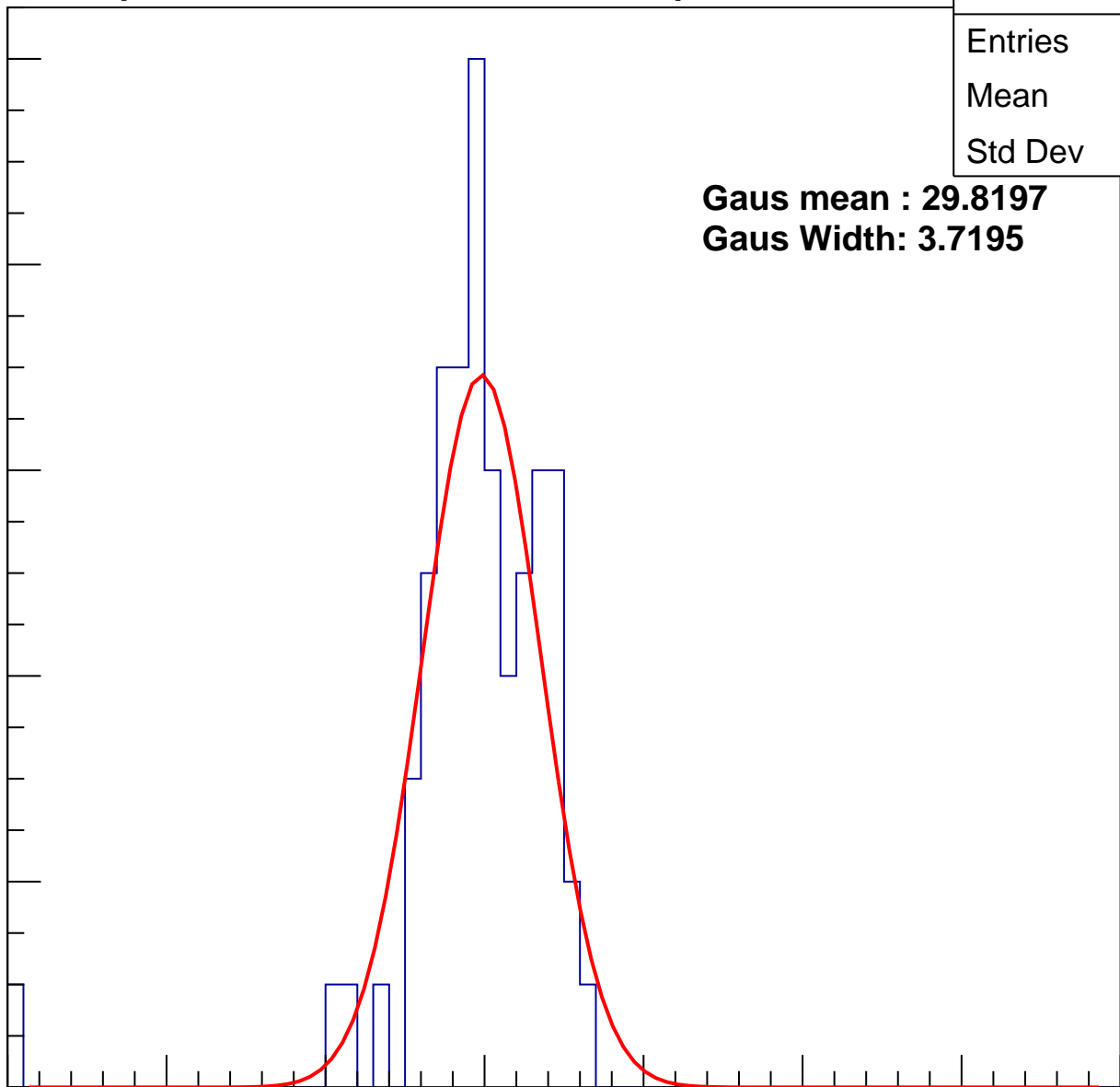
**Gaus Width: 3.7195**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U20-ch24, adc1

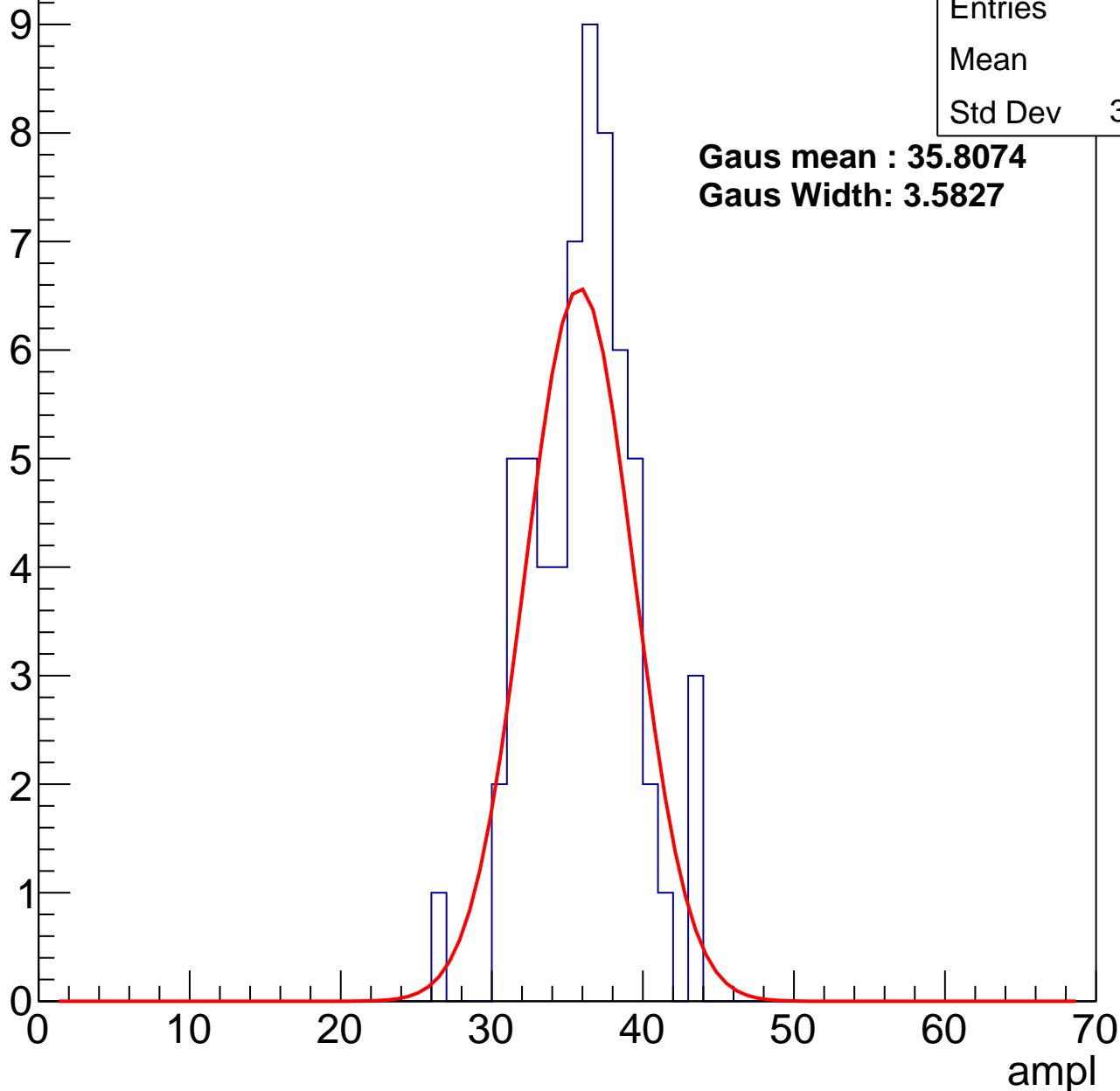
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	35.6
Std Dev	3.377

**Gaus mean : 35.8074**

**Gaus Width: 3.5827**



# B1L101S, U20-ch24, adc2

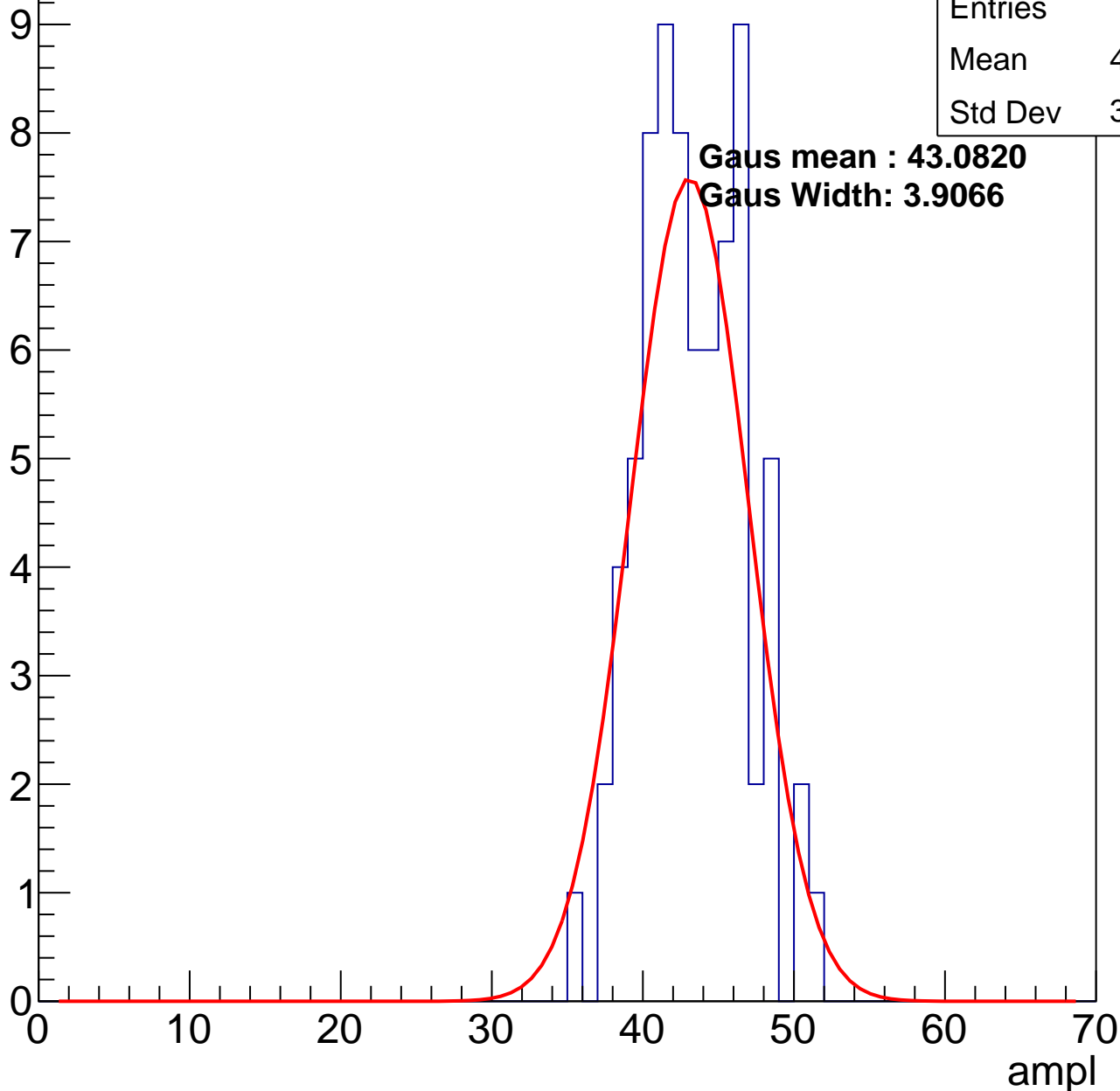
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	75
Mean	42.89
Std Dev	3.396

**Gaus mean : 43.0820**

**Gaus Width: 3.9066**



# B1L101S, U20-ch24, adc3

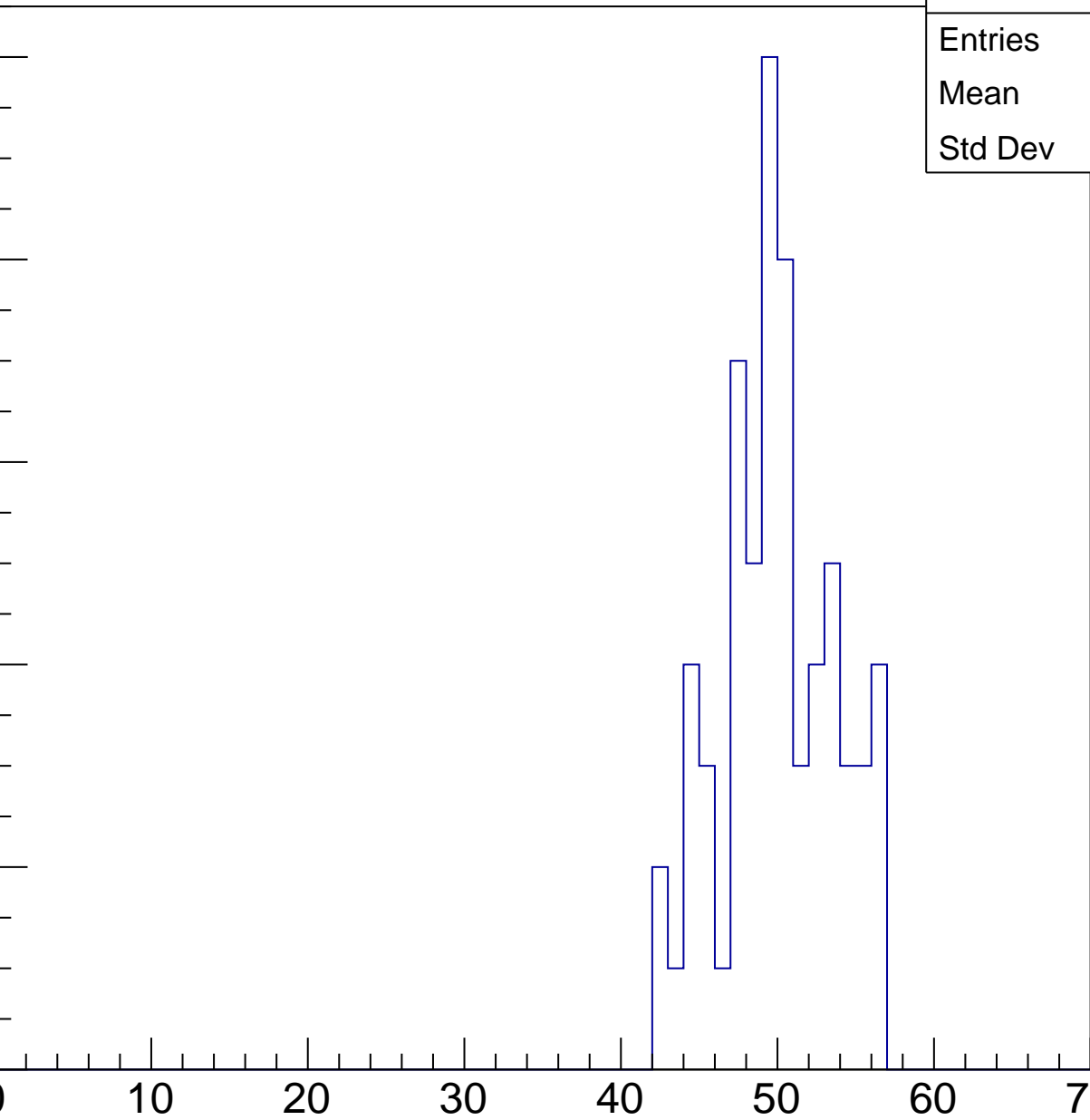
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	63
Mean	49.52
Std Dev	3.612

Entry

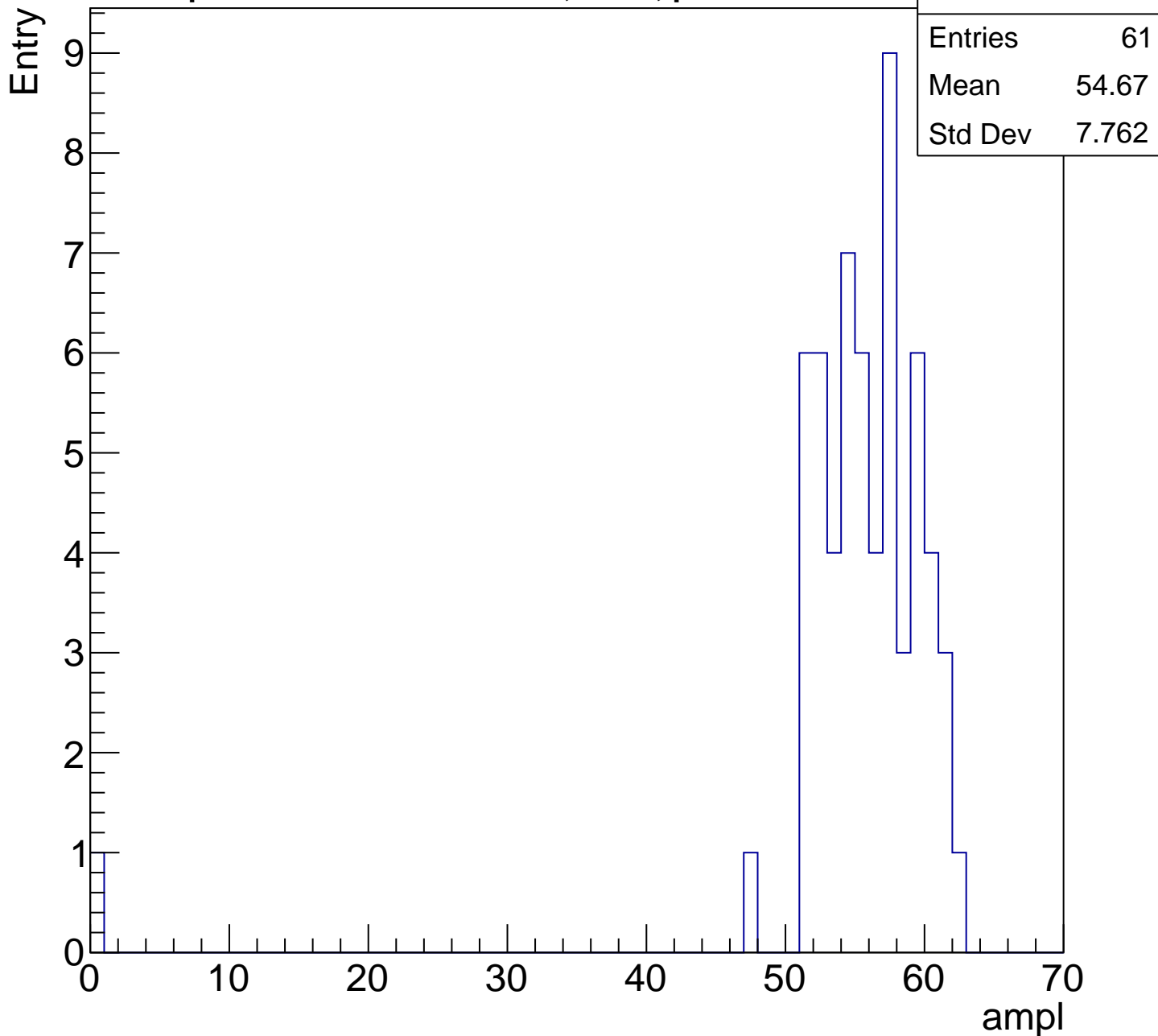
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U20-ch24, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

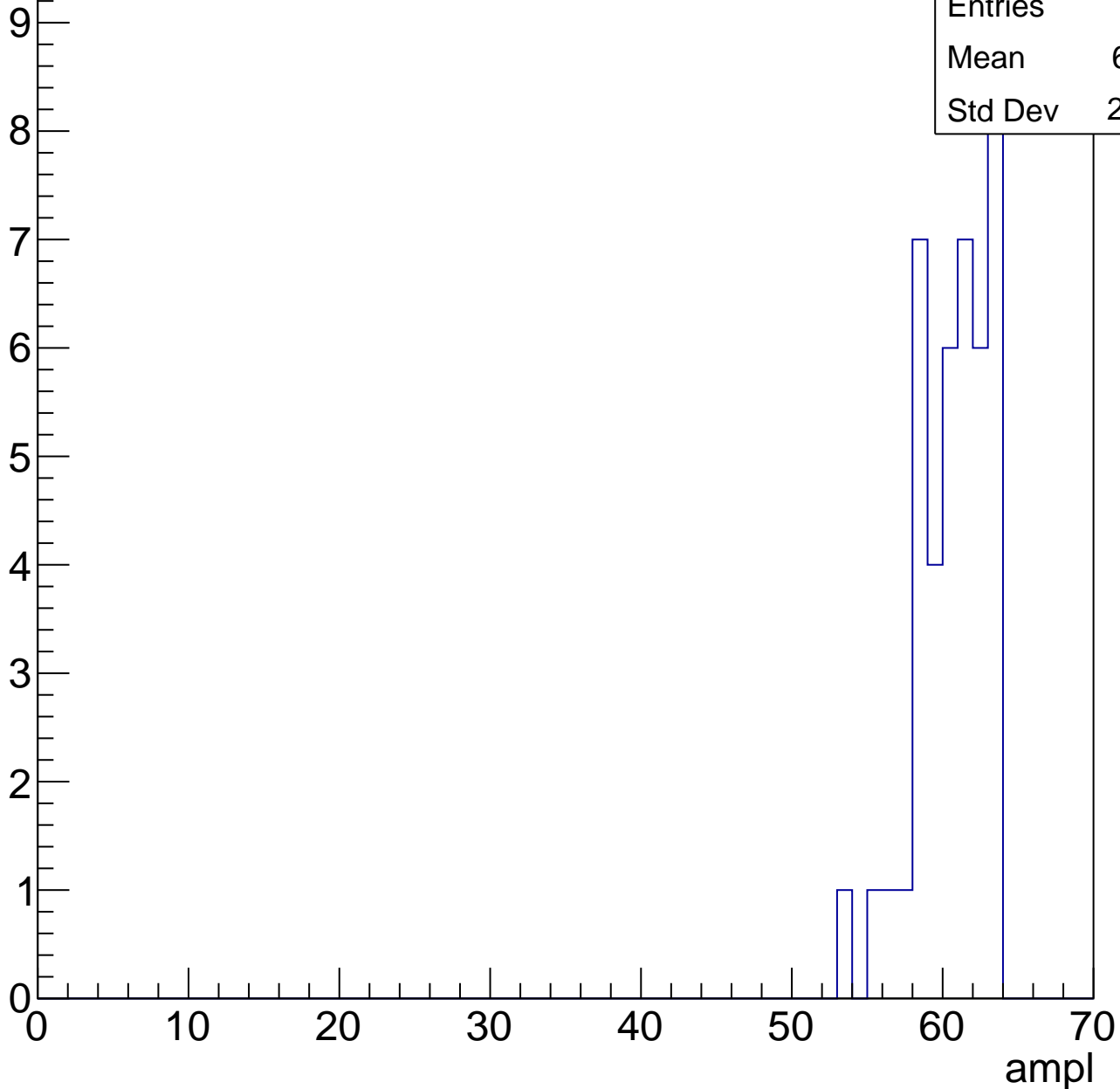


# B1L101S, U20-ch24, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

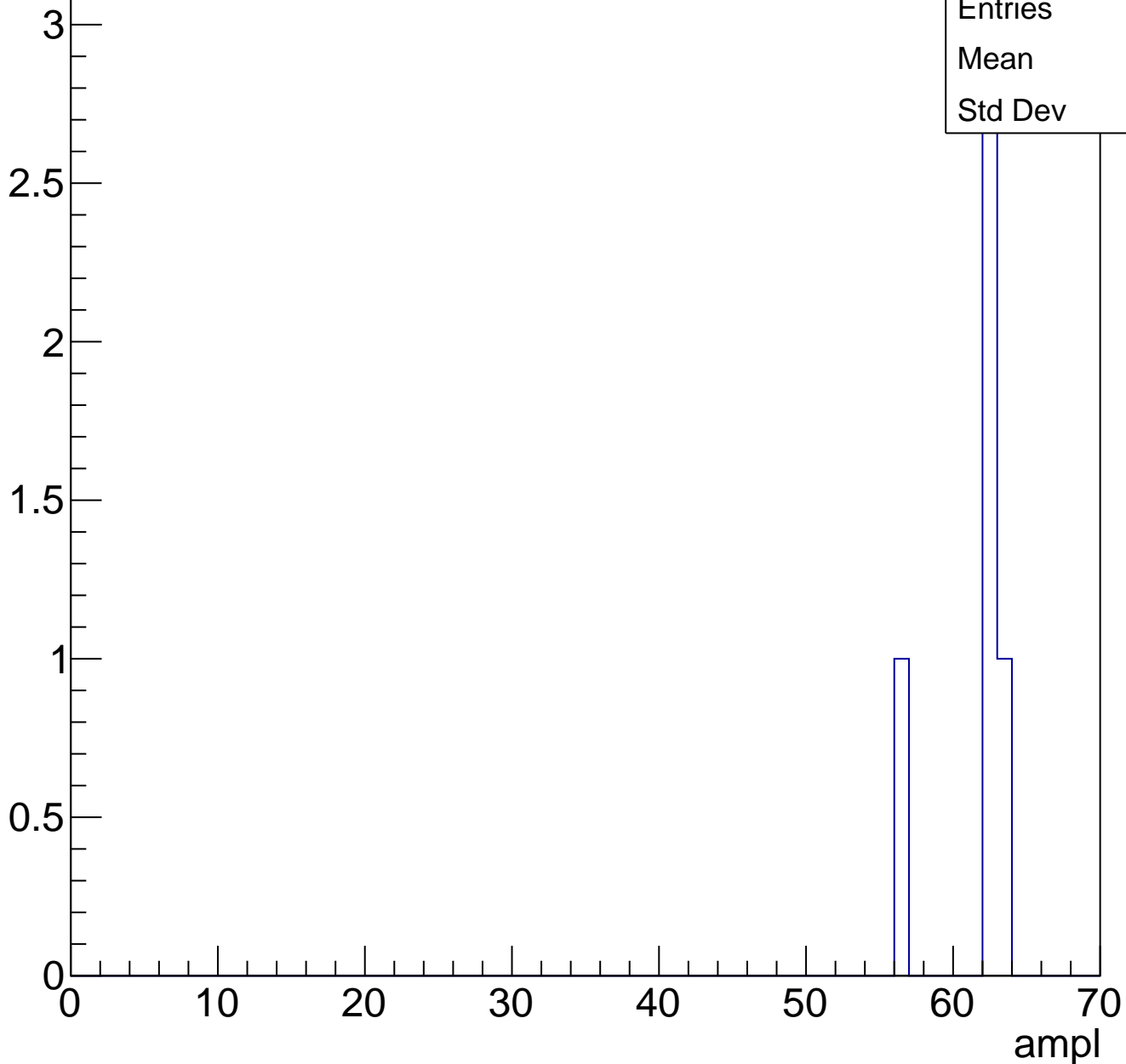
Entries	43
Mean	60.21
Std Dev	2.368



# B1L101S, U20-ch24, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U20-ch24, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U20-ch25, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	87
Mean	28.62
Std Dev	5.575

**Gaus mean : 29.6781**

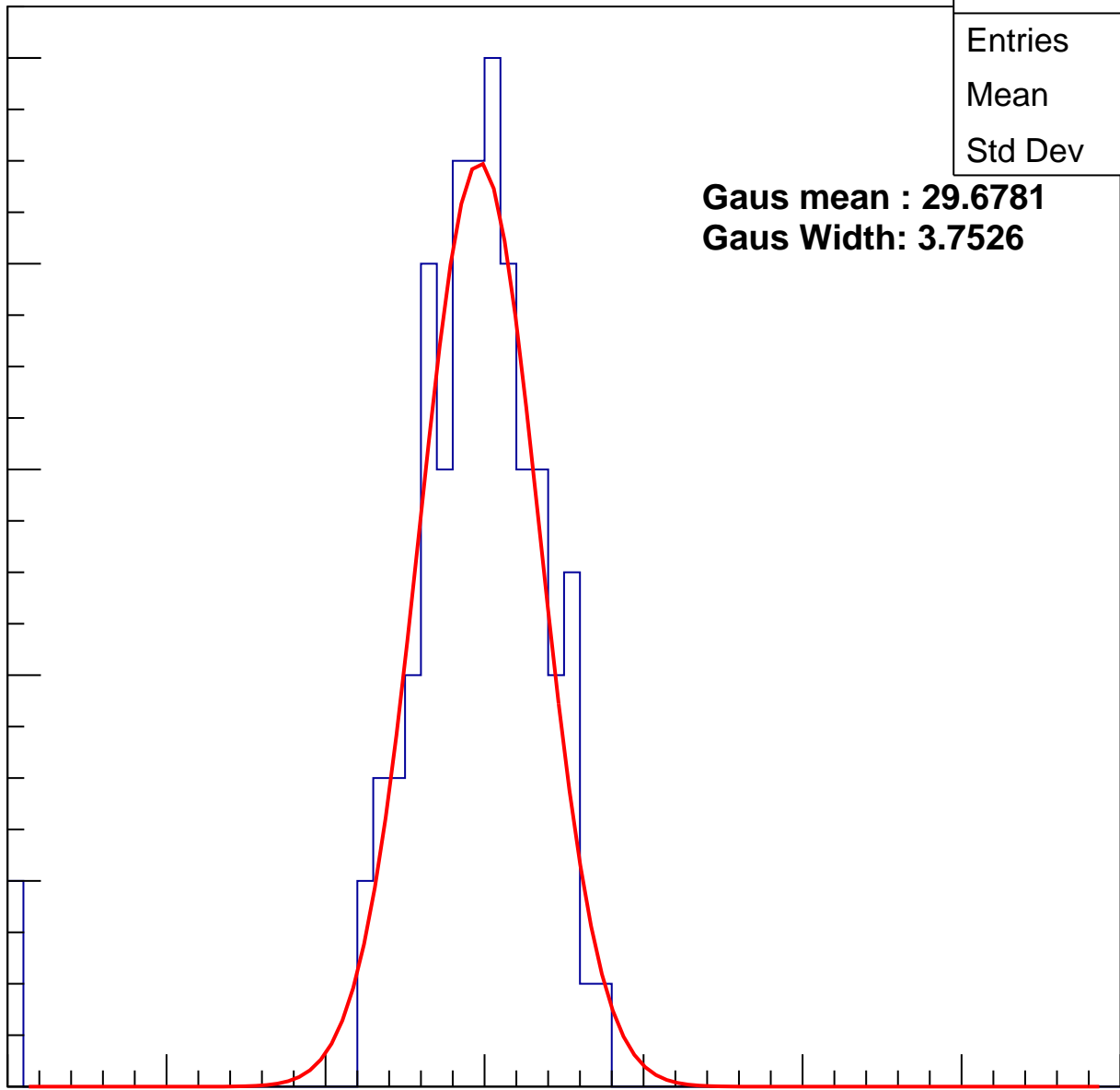
**Gaus Width: 3.7526**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U20-ch25, adc1

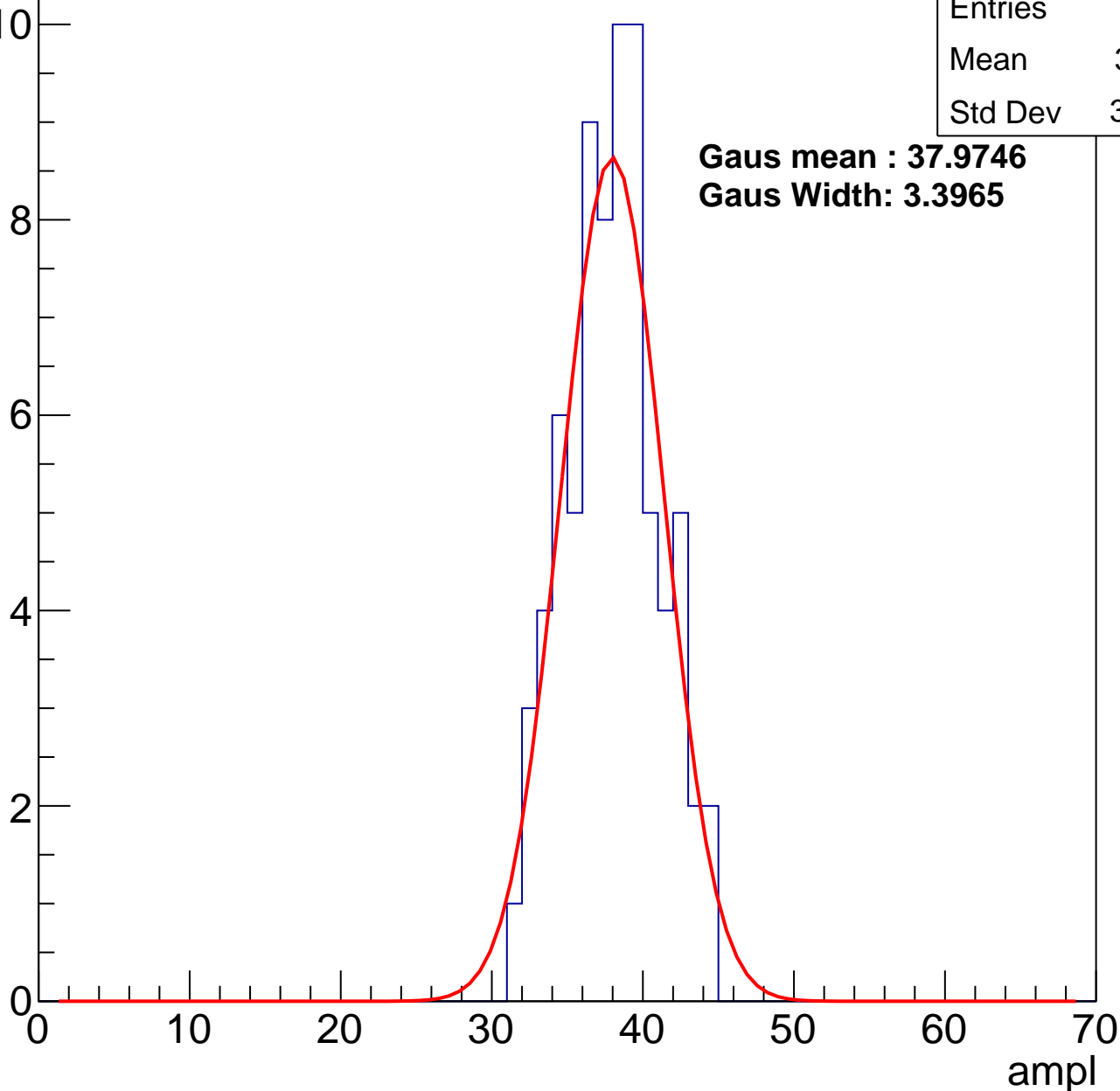
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	74
Mean	37.51
Std Dev	3.059

**Gaus mean : 37.9746**

**Gaus Width: 3.3965**



# B1L101S, U20-ch25, adc2

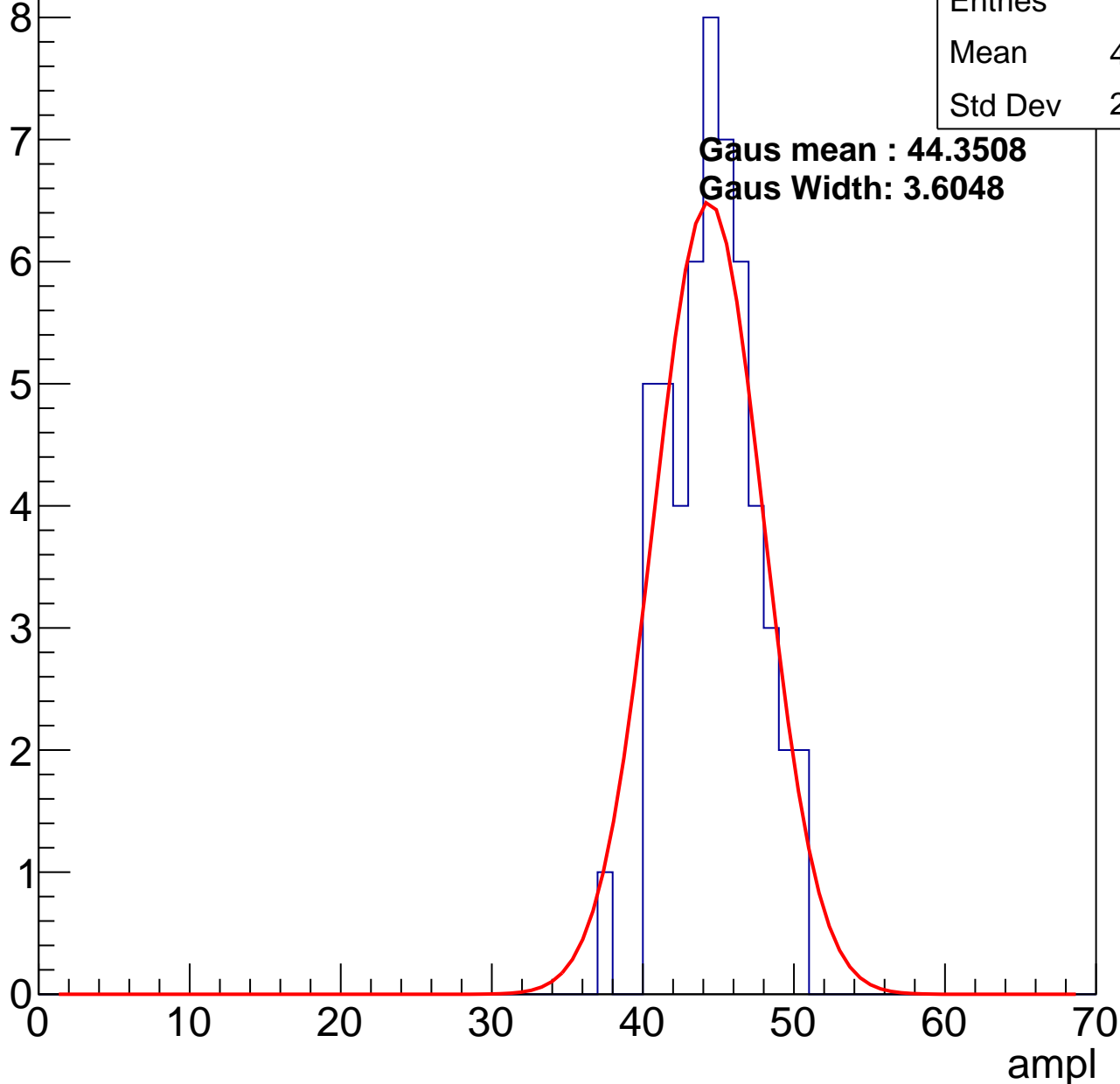
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	53
Mean	44.17
Std Dev	2.853

**Gaus mean : 44.3508**

**Gaus Width: 3.6048**

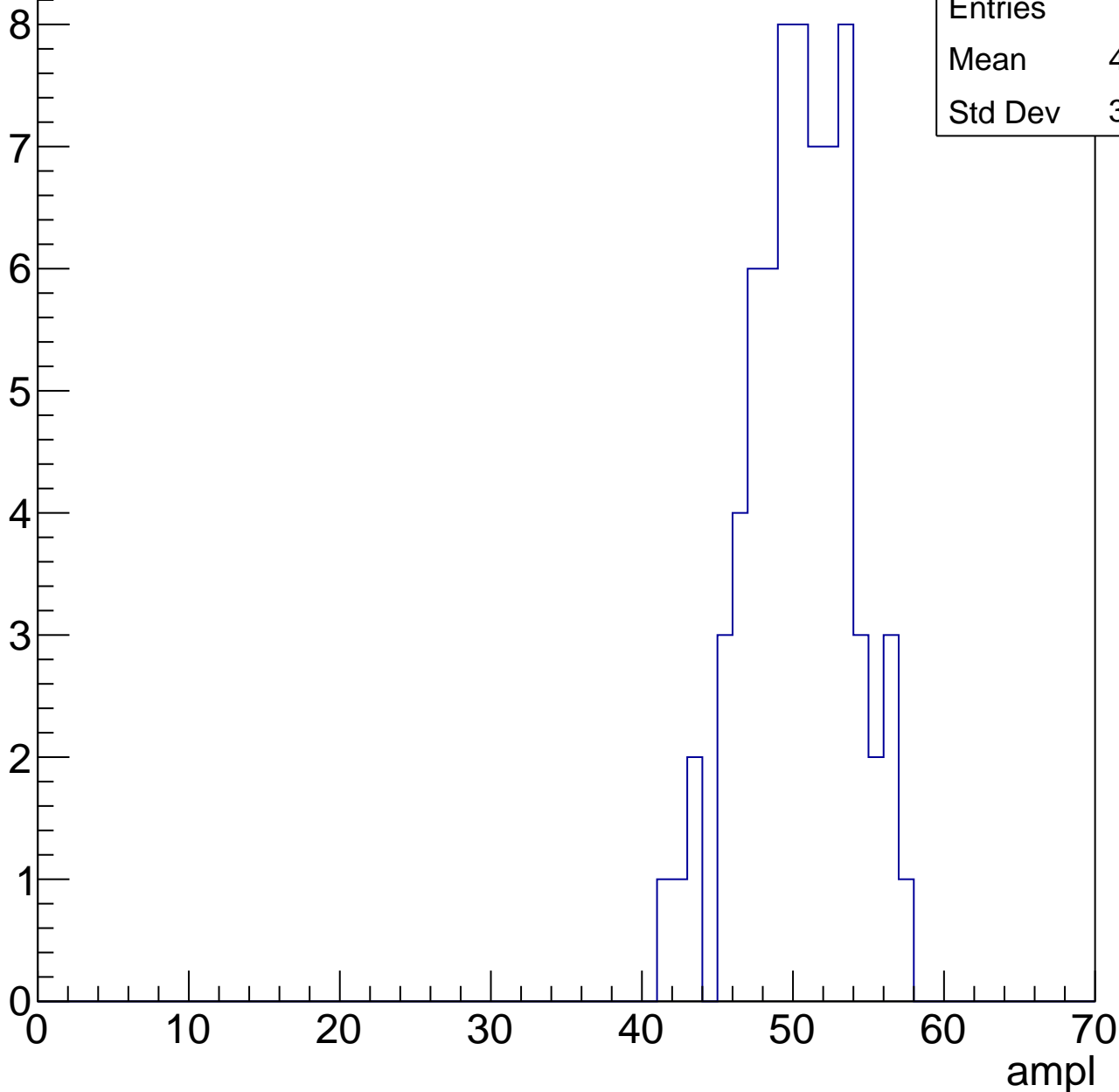


# B1L101S, U20-ch25, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	49.89
Std Dev	3.442

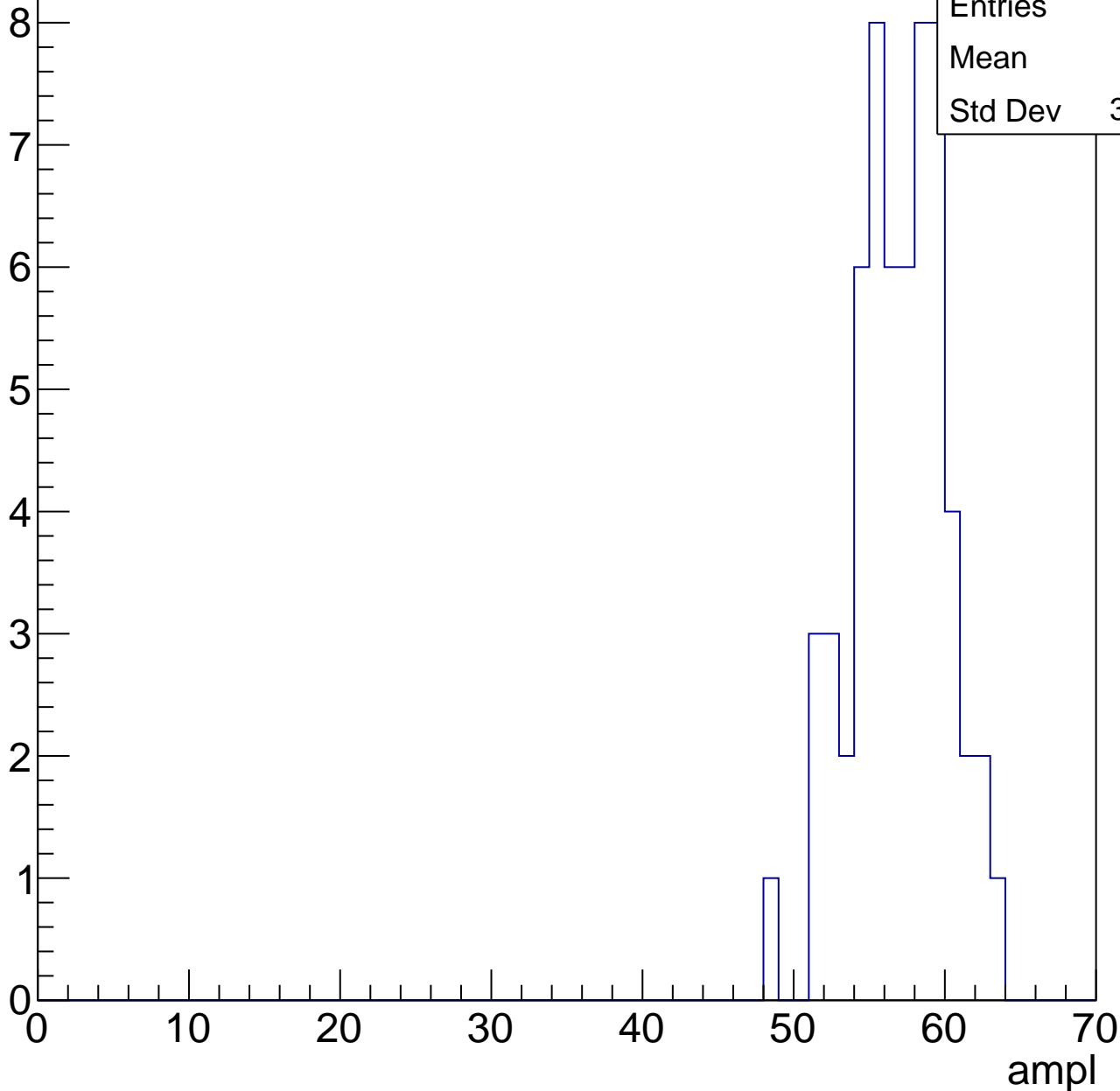


# B1L101S, U20-ch25, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

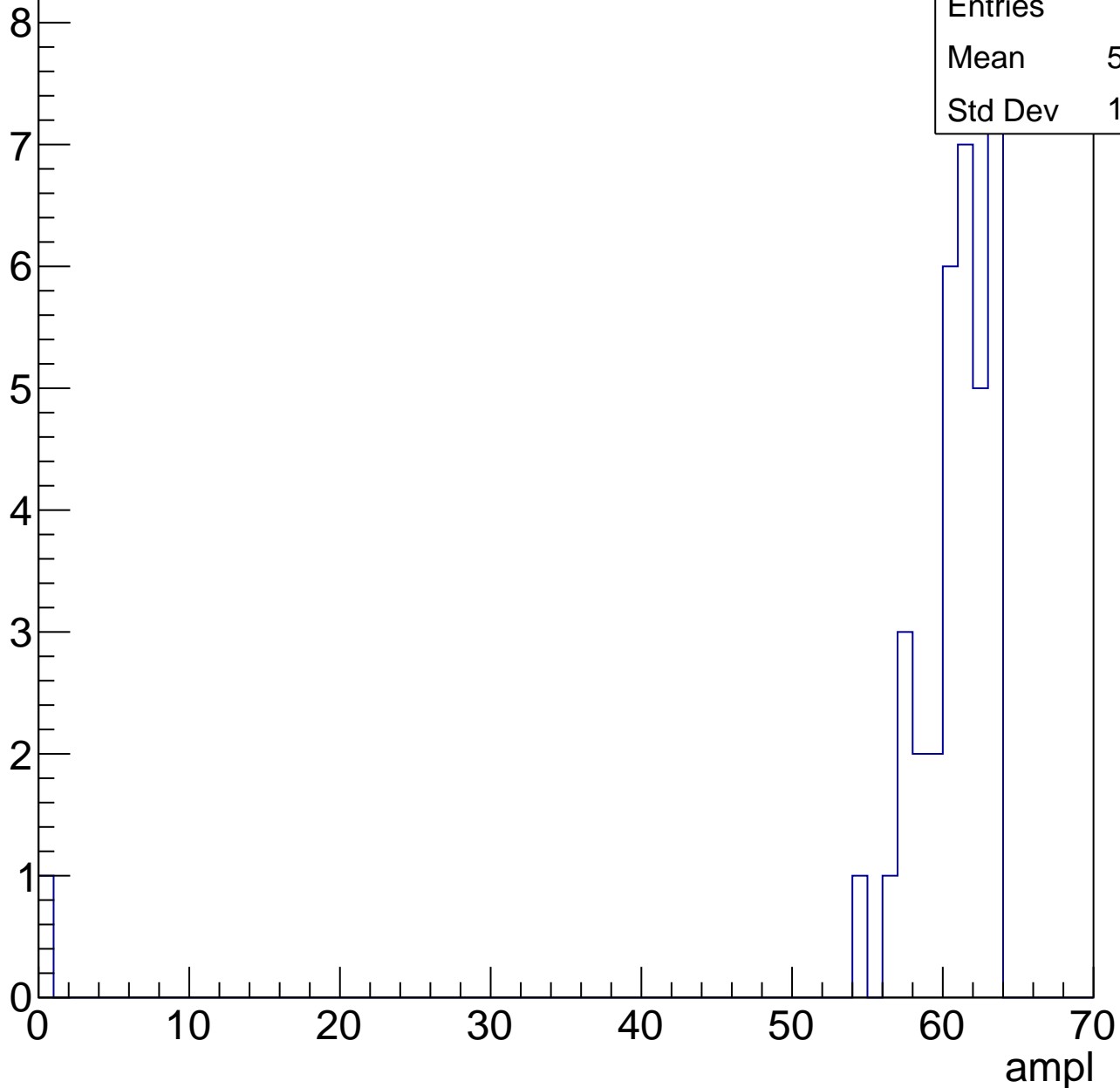
Entries	60
Mean	56.5
Std Dev	3.074



# B1L101S, U20-ch25, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U20-ch25, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	5
Mean	62
Std Dev	0.6325



# B1L101S, U20-ch25, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U20-ch26, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	72
Mean	28.01
Std Dev	3.534

**Gaus mean : 28.5708**

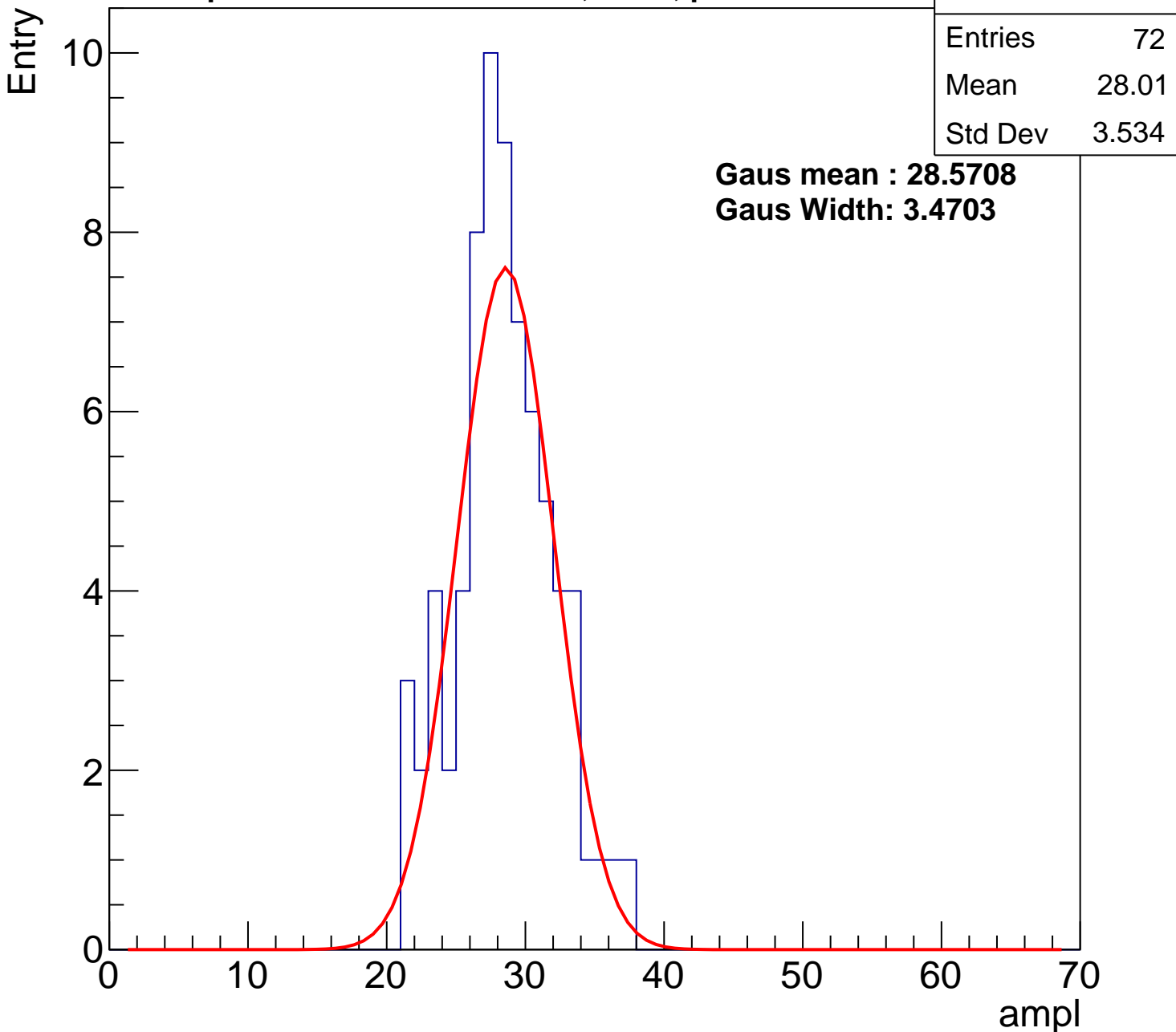
**Gaus Width: 3.4703**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



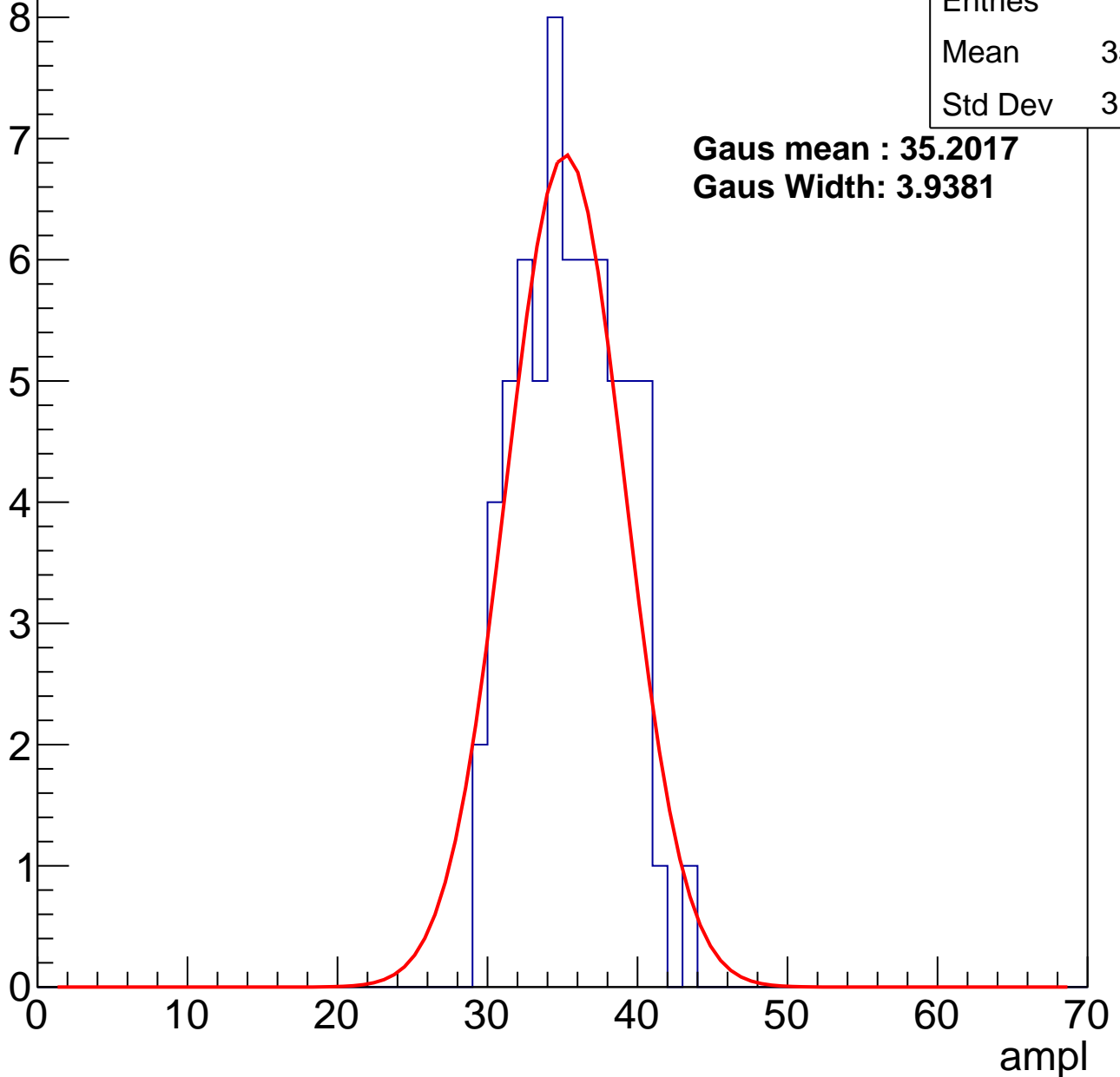
# B1L101S, U20-ch26, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	35.06
Std Dev	3.314

**Gaus mean : 35.2017**  
**Gaus Width: 3.9381**



# B1L101S, U20-ch26, adc2

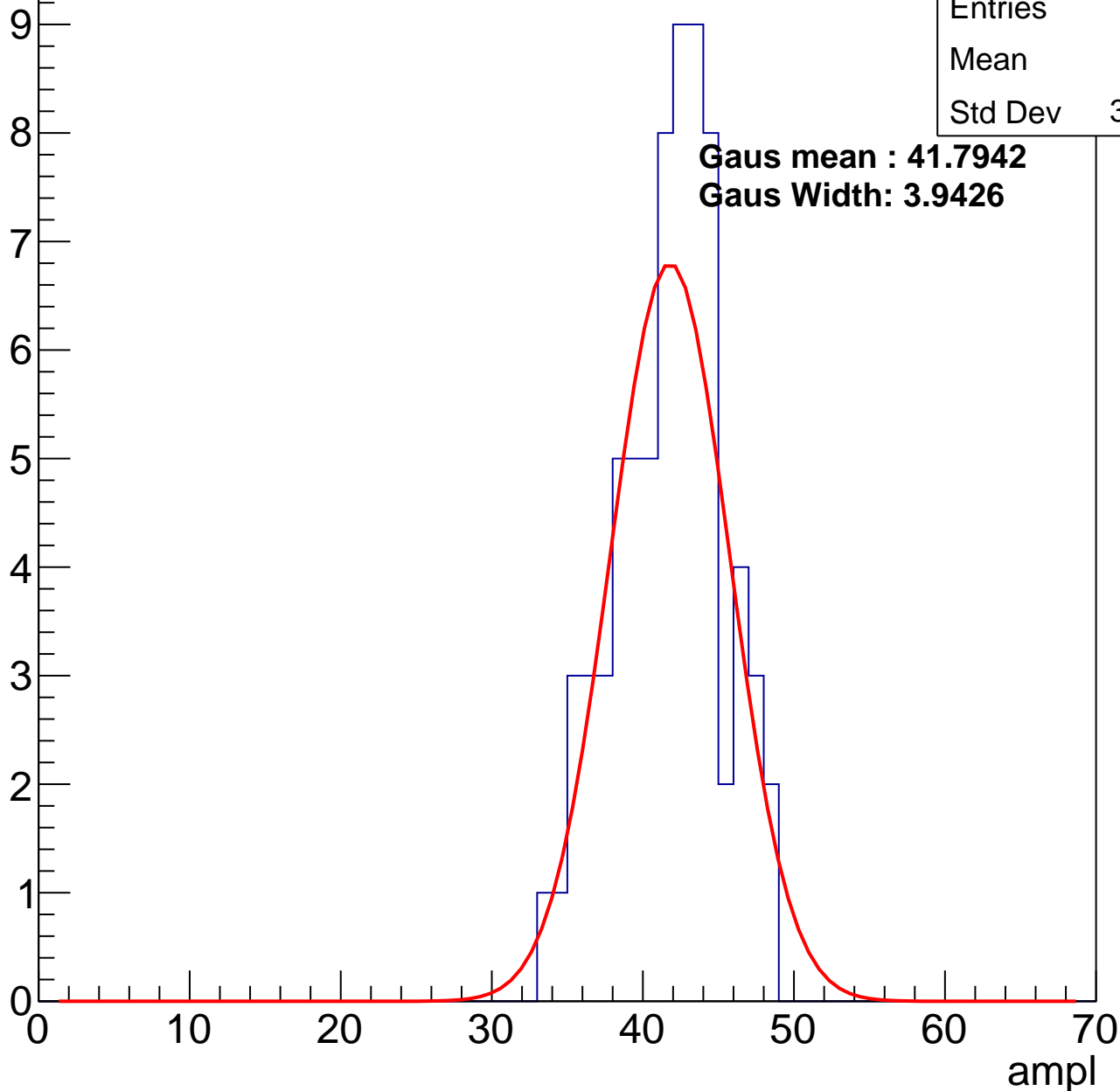
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	71
Mean	41.3
Std Dev	3.486

**Gaus mean : 41.7942**

**Gaus Width: 3.9426**

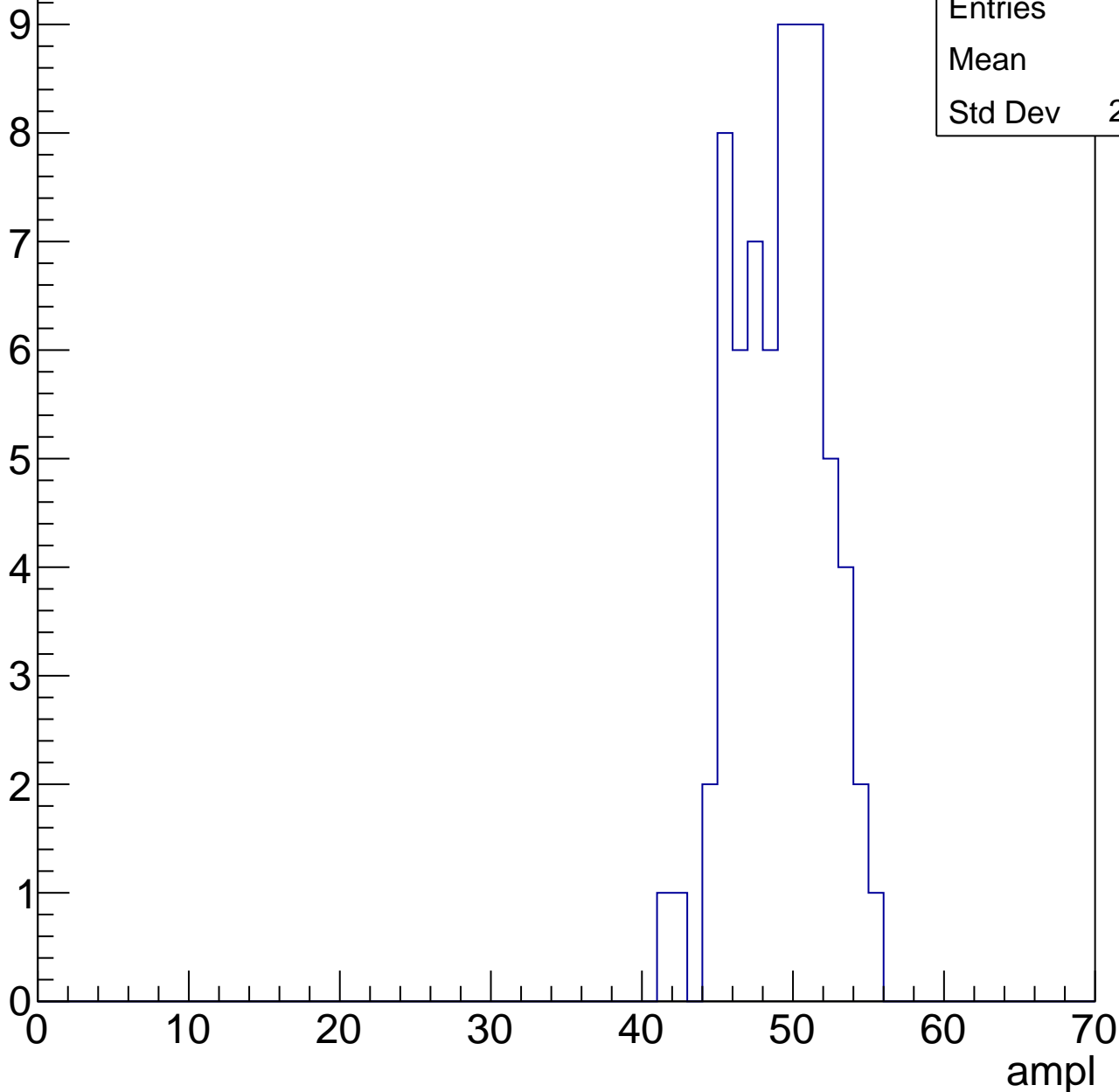


# B1L101S, U20-ch26, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	48.7
Std Dev	2.959

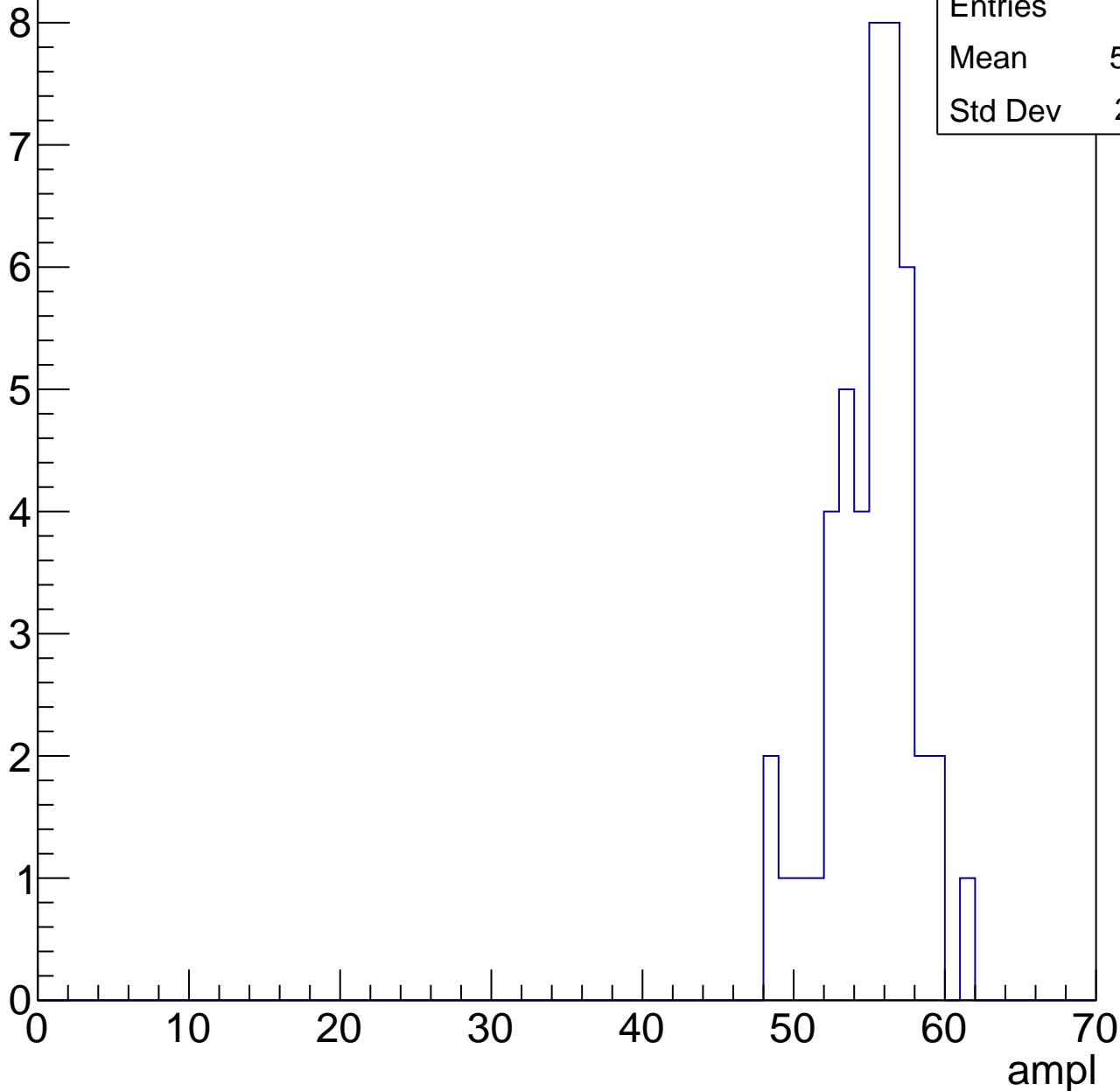


# B1L101S, U20-ch26, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	45
Mean	54.67
Std Dev	2.781



# B1L101S, U20-ch26, adc5

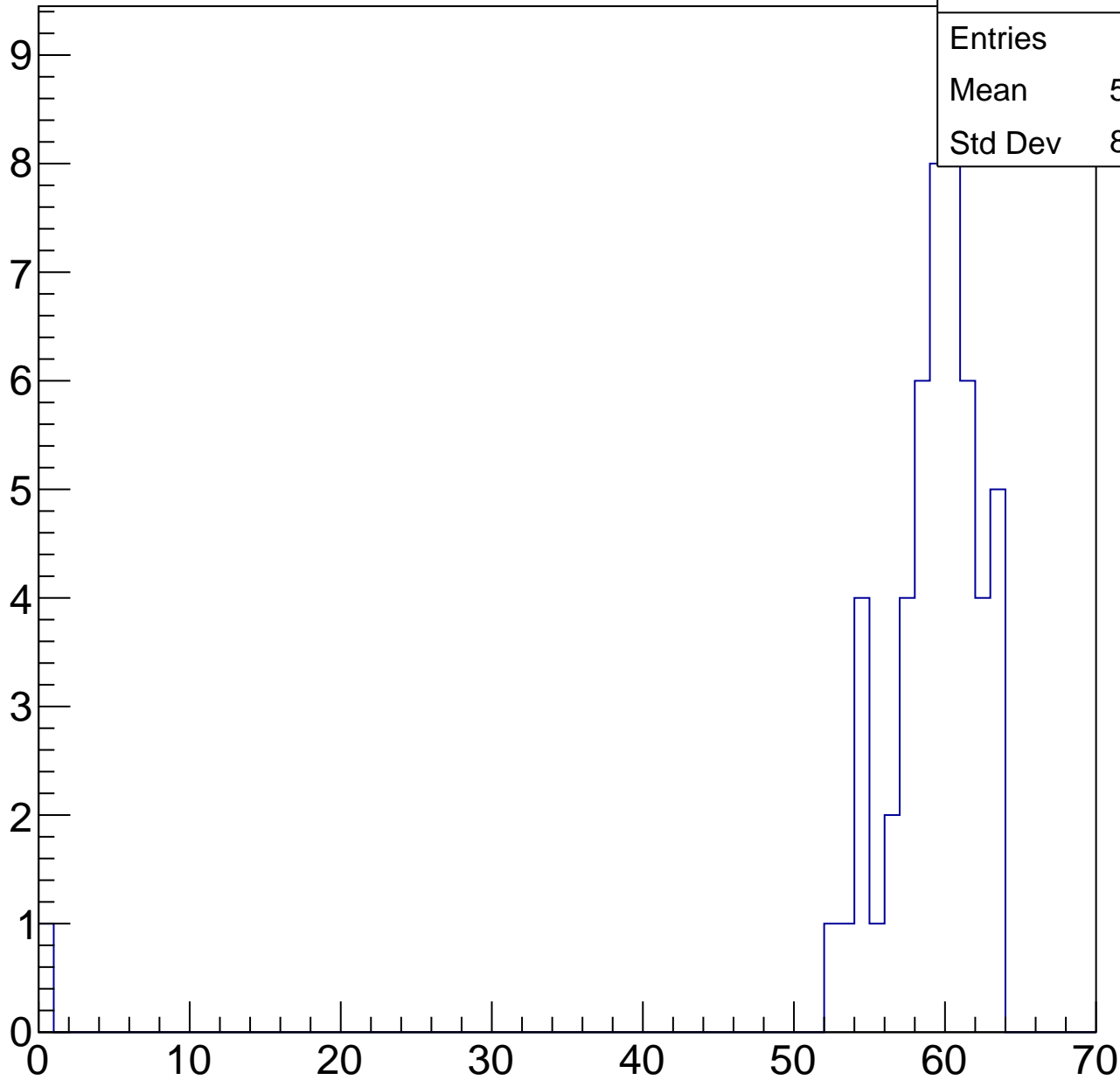
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	52
Mean	57.79
Std Dev	8.543

ampl

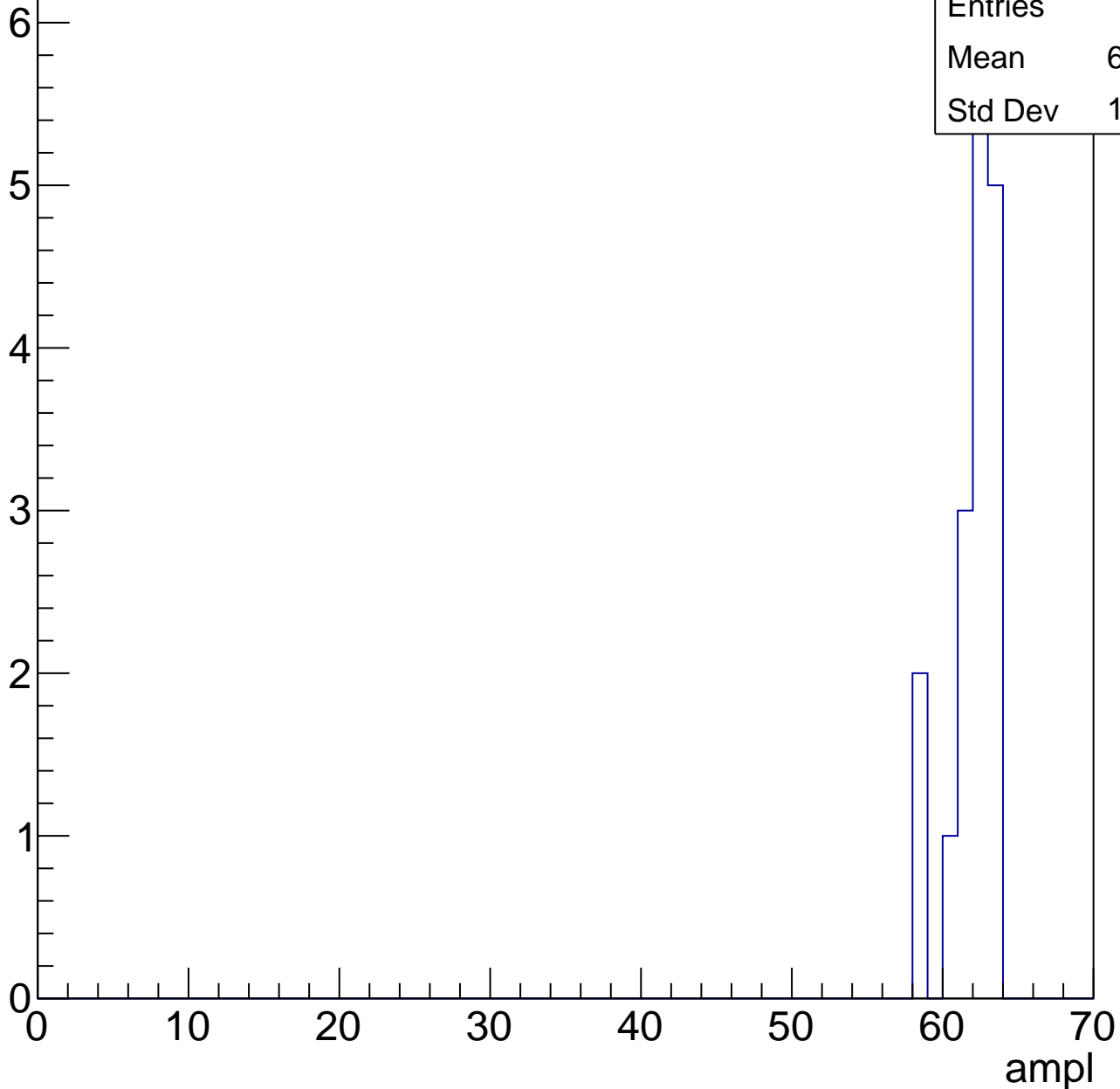


# B1L101S, U20-ch26, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	17
Mean	61.53
Std Dev	1.538





# B1L101S, U20-ch26, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L101S, U20-ch27, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	71
Mean	27.93
Std Dev	4.607

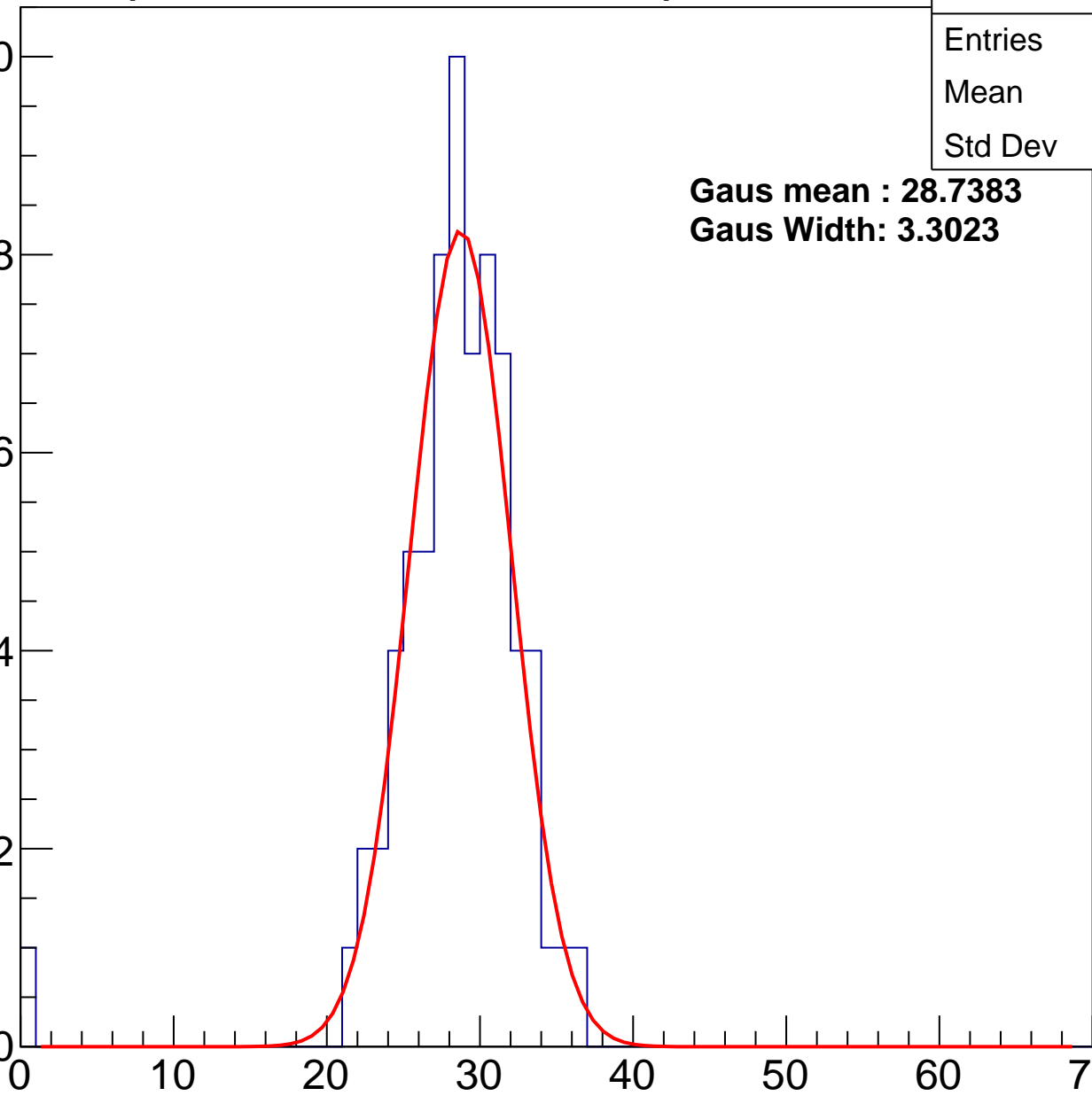
**Gaus mean : 28.7383**

**Gaus Width: 3.3023**

Entry

10  
8  
6  
4  
2  
0

ampl



# B1L101S, U20-ch27, adc1

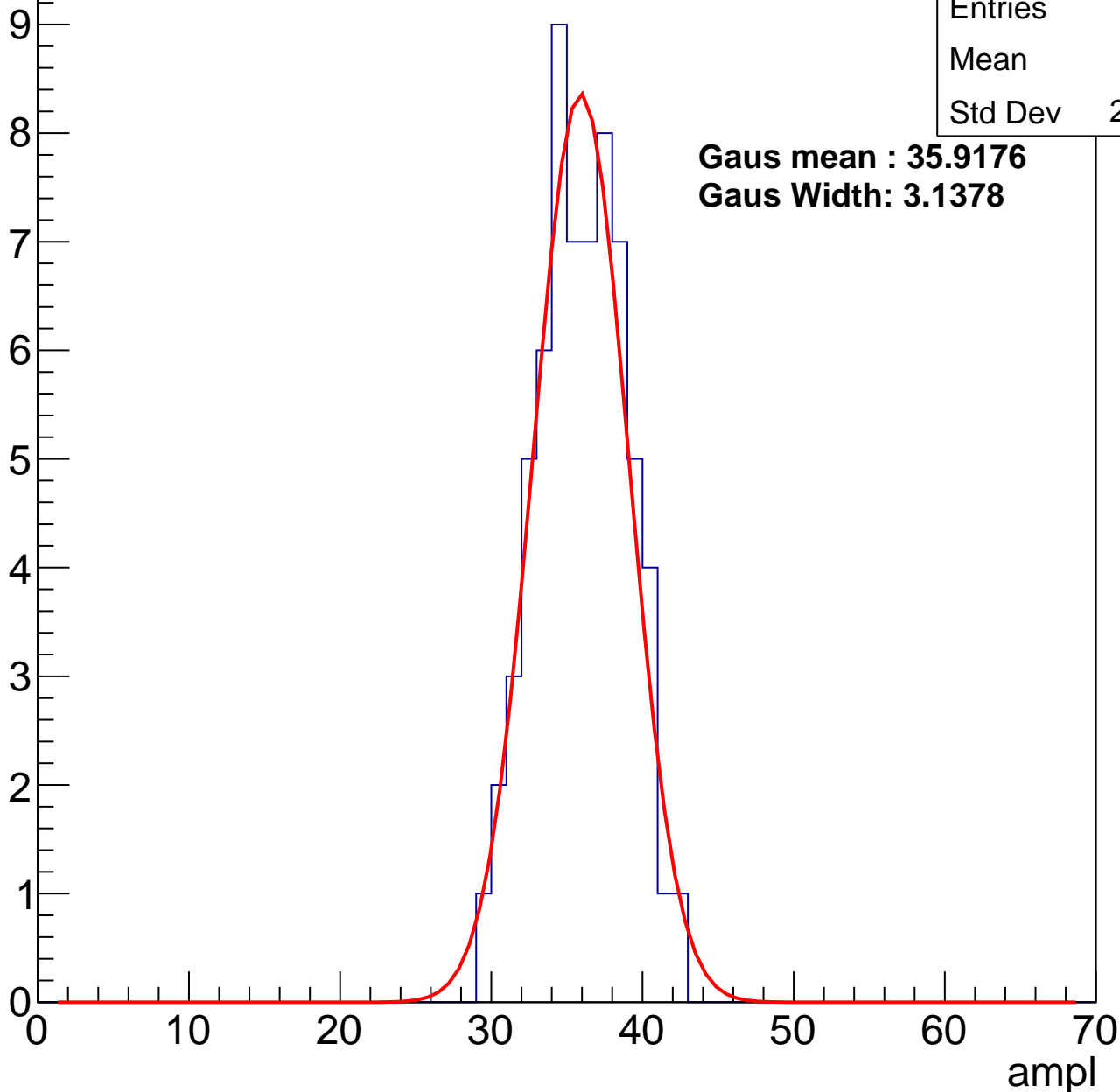
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	66
Mean	35.5
Std Dev	2.919

**Gaus mean : 35.9176**

**Gaus Width: 3.1378**



# B1L101S, U20-ch27, adc2

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

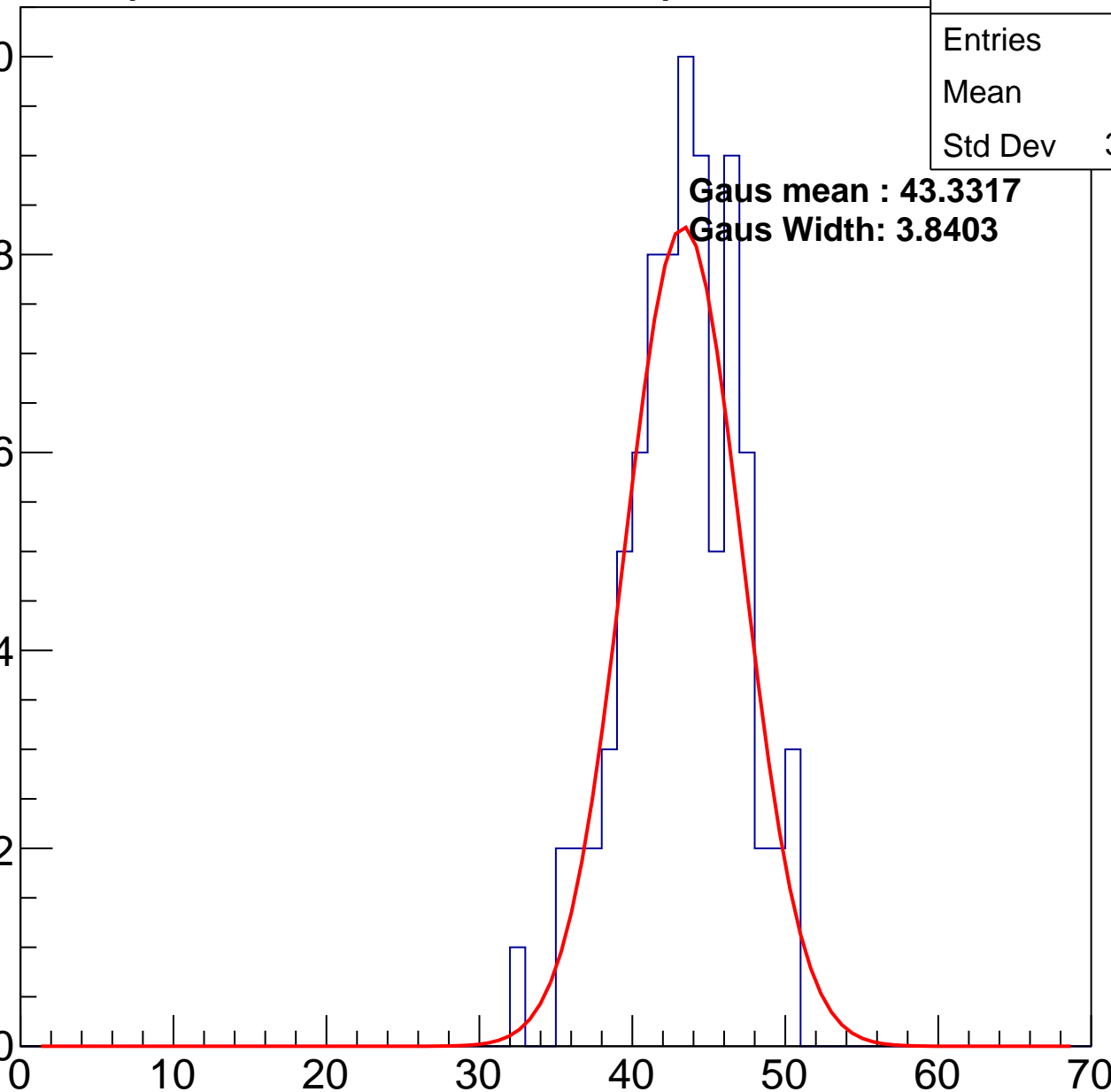
Entries	83
Mean	42.8
Std Dev	3.705

**Gaus mean : 43.3317**

**Gaus Width: 3.8403**

10  
8  
6  
4  
2  
0

ampl

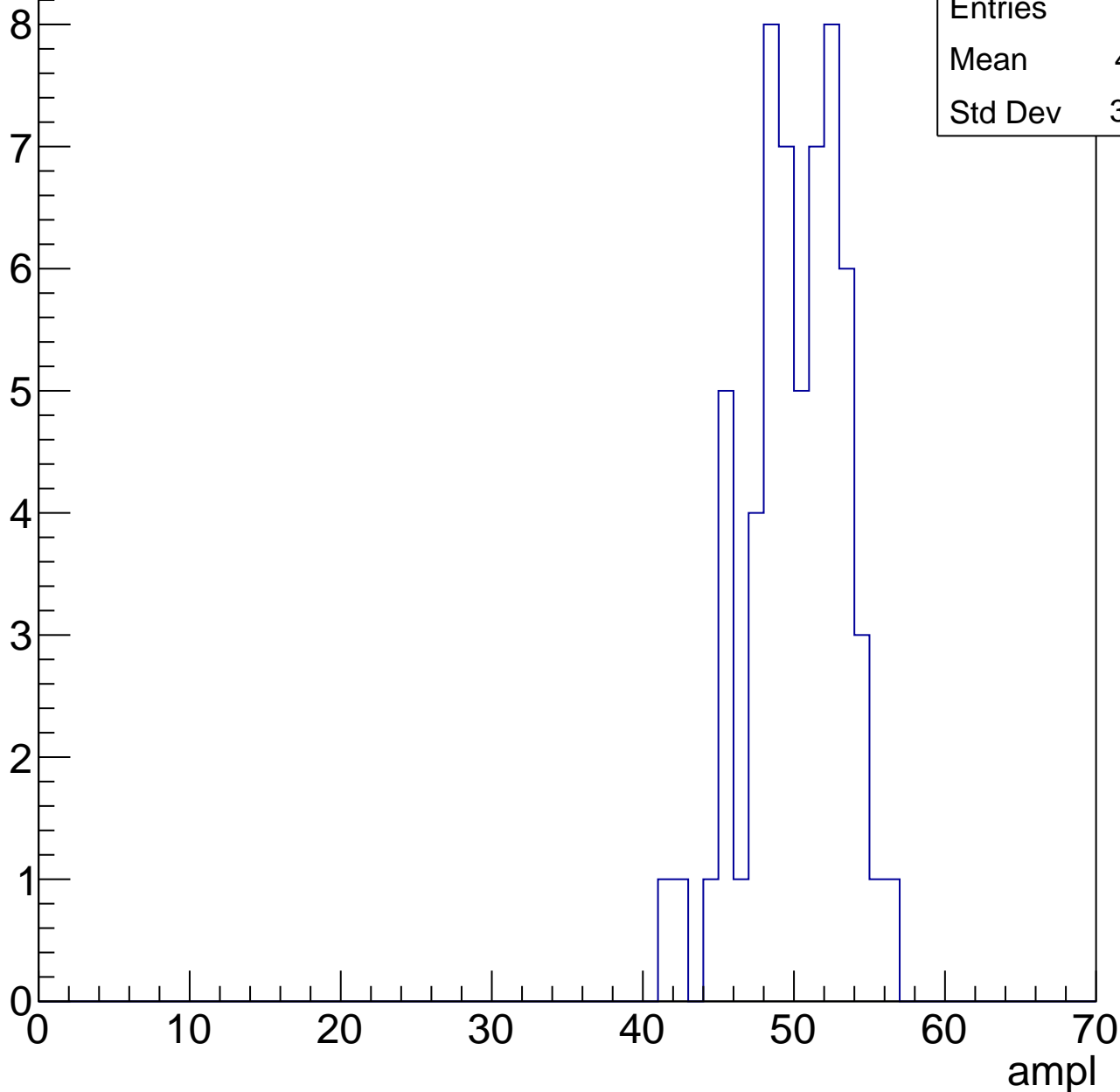


# B1L101S, U20-ch27, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

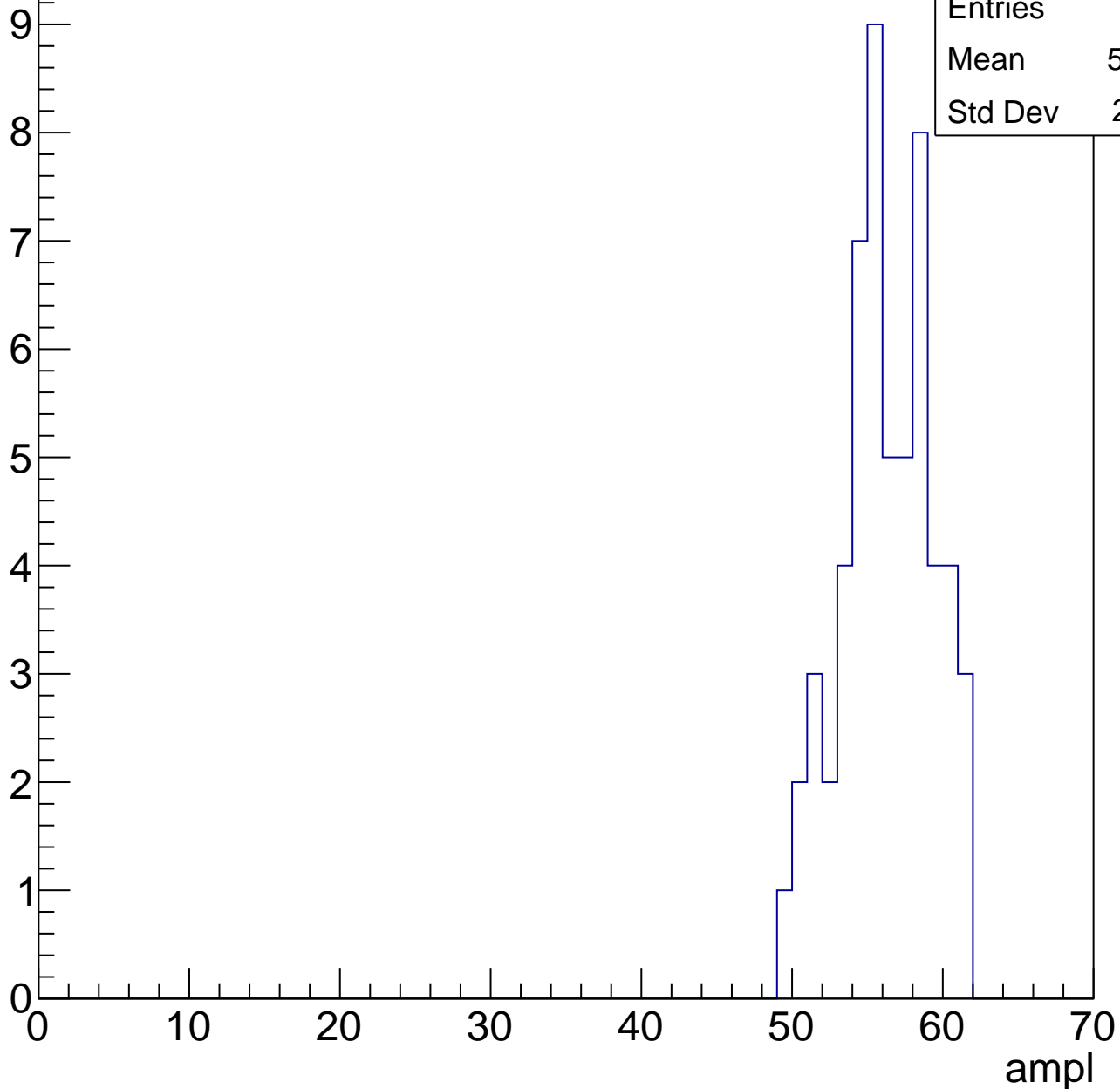
Entries	59
Mean	49.61
Std Dev	3.162



# B1L101S, U20-ch27, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

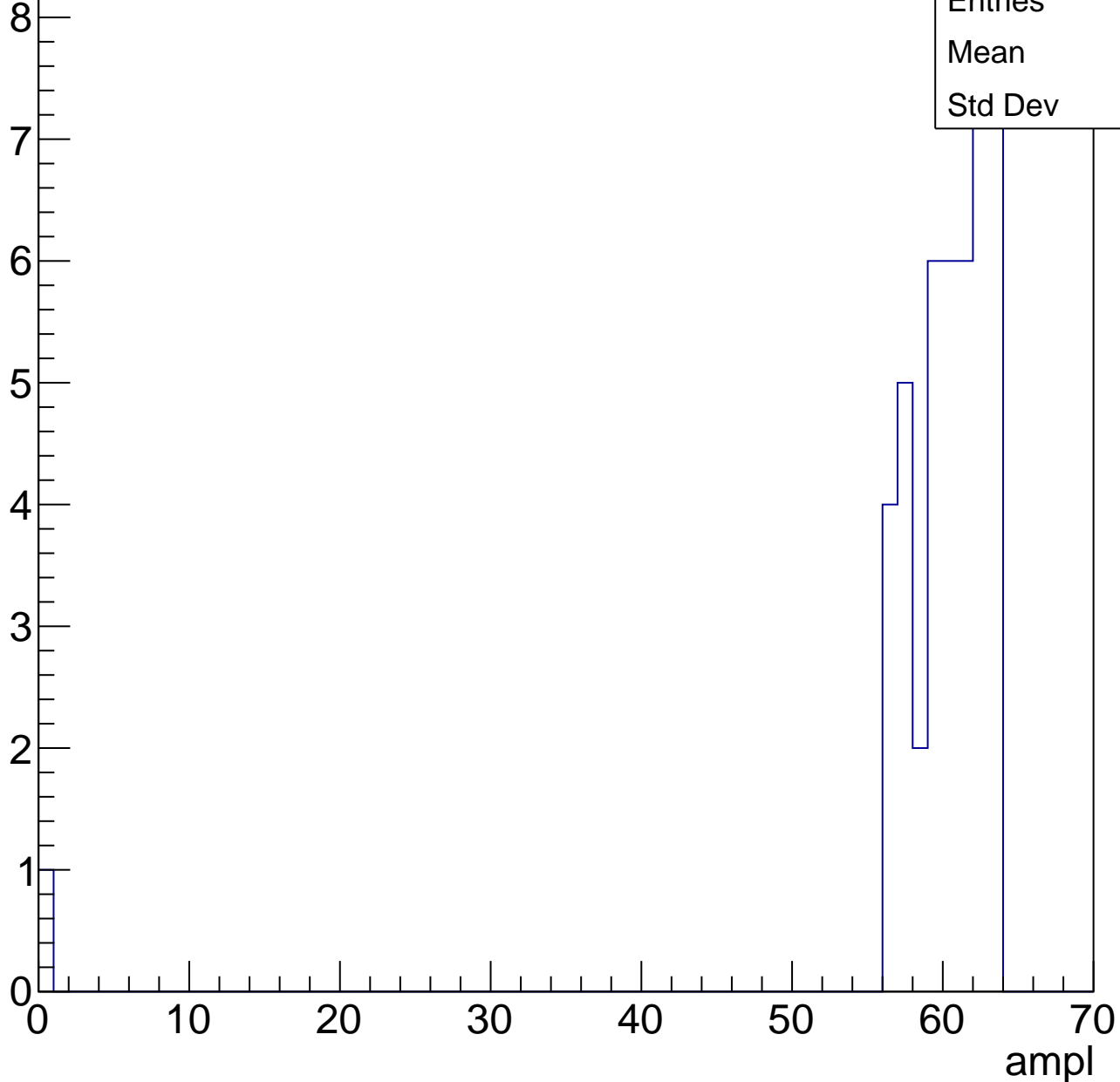


Entries	57
Mean	55.77
Std Dev	2.991

# B1L101S, U20-ch27, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U20-ch27, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	5
Mean	62.2
Std Dev	0.7483

ampl

0 10 20 30 40 50 60 70



# B1L101S, U20-ch27, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U20-ch28, adc0

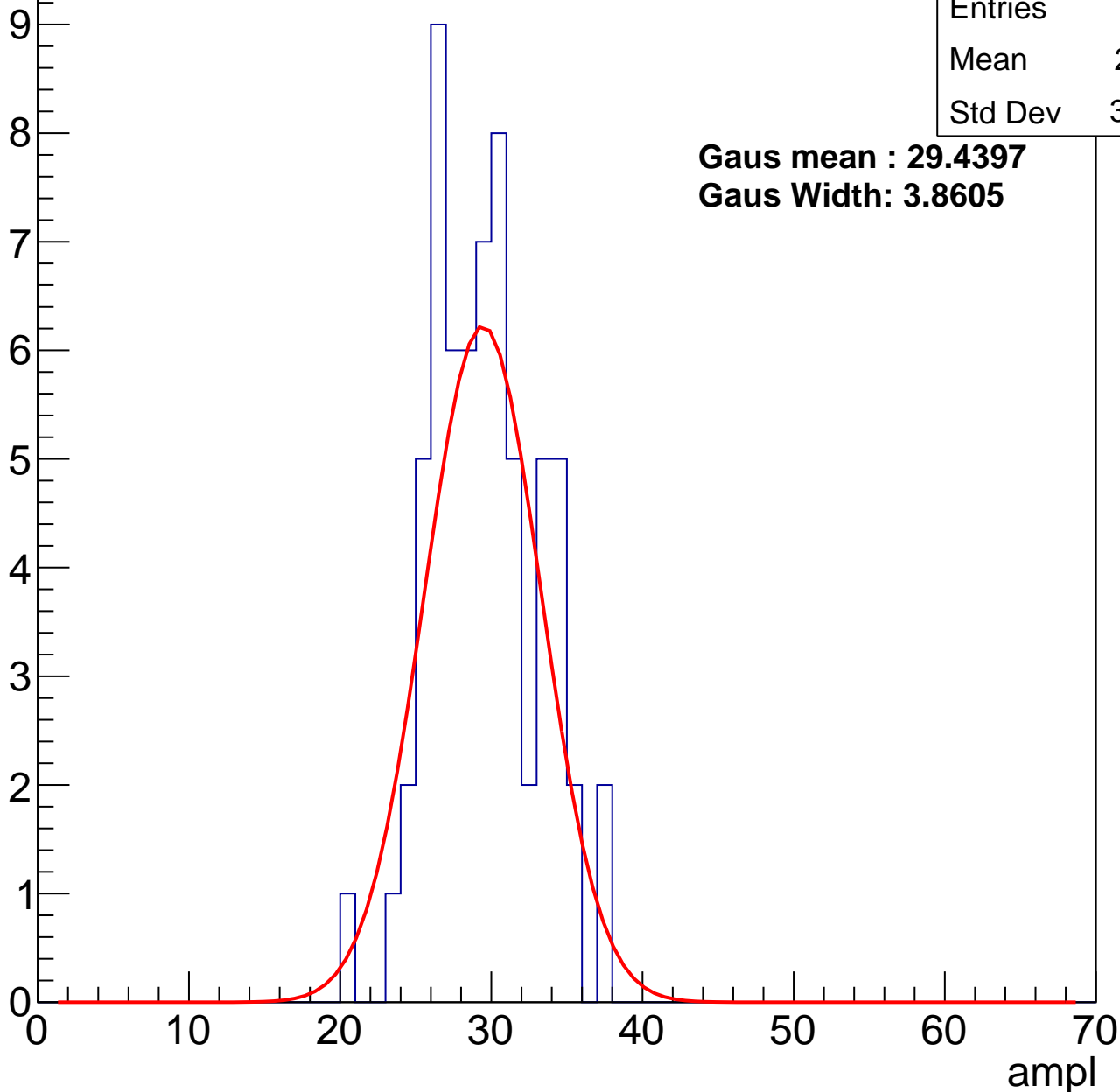
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	66
Mean	29.11
Std Dev	3.499

**Gaus mean : 29.4397**

**Gaus Width: 3.8605**



# B1L101S, U20-ch28, adc1

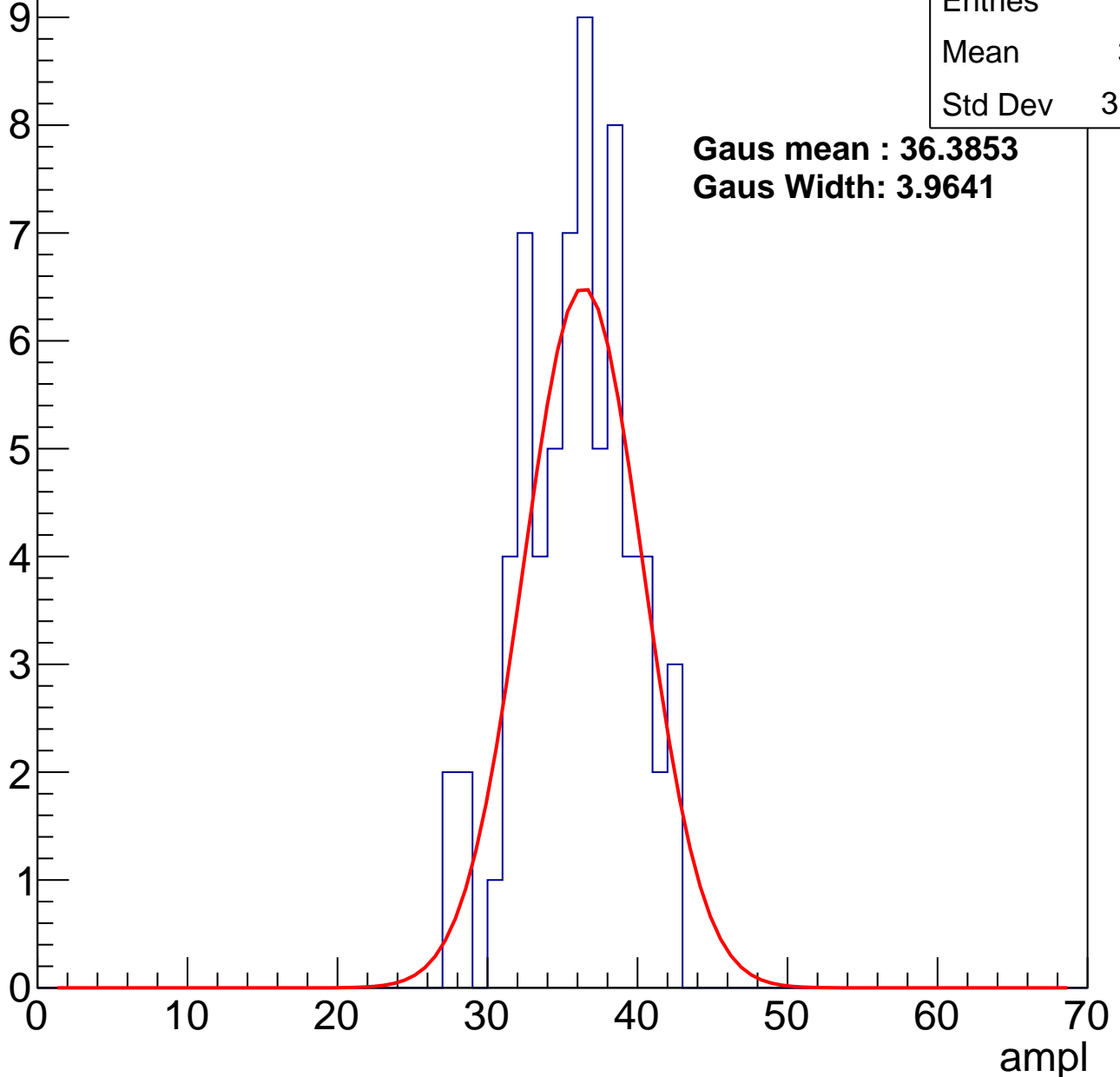
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	67
Mean	35.4
Std Dev	3.608

**Gaus mean : 36.3853**

**Gaus Width: 3.9641**



# B1L101S, U20-ch28, adc2

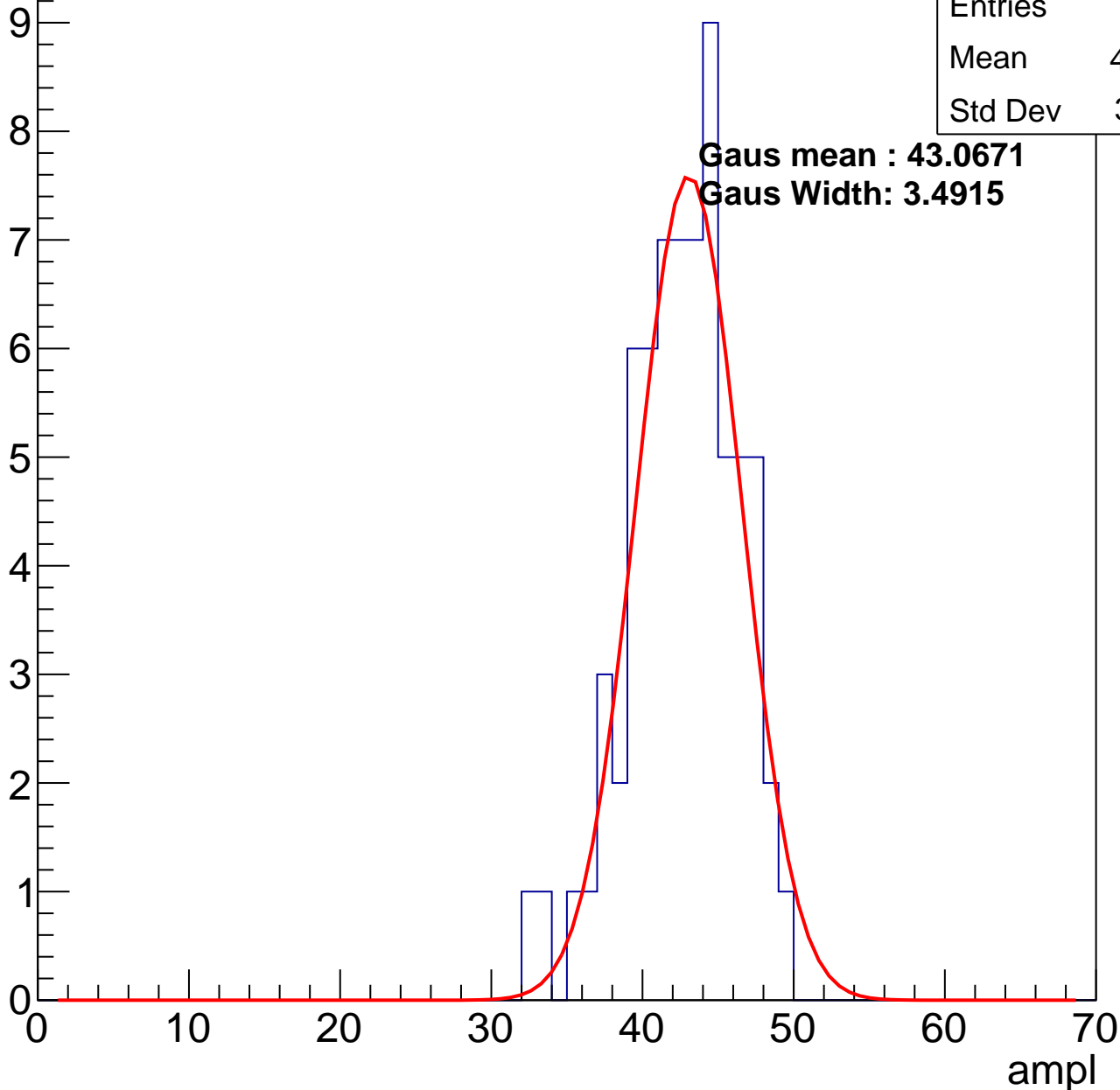
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	42.17
Std Dev	3.551

**Gaus mean : 43.0671**

**Gaus Width: 3.4915**

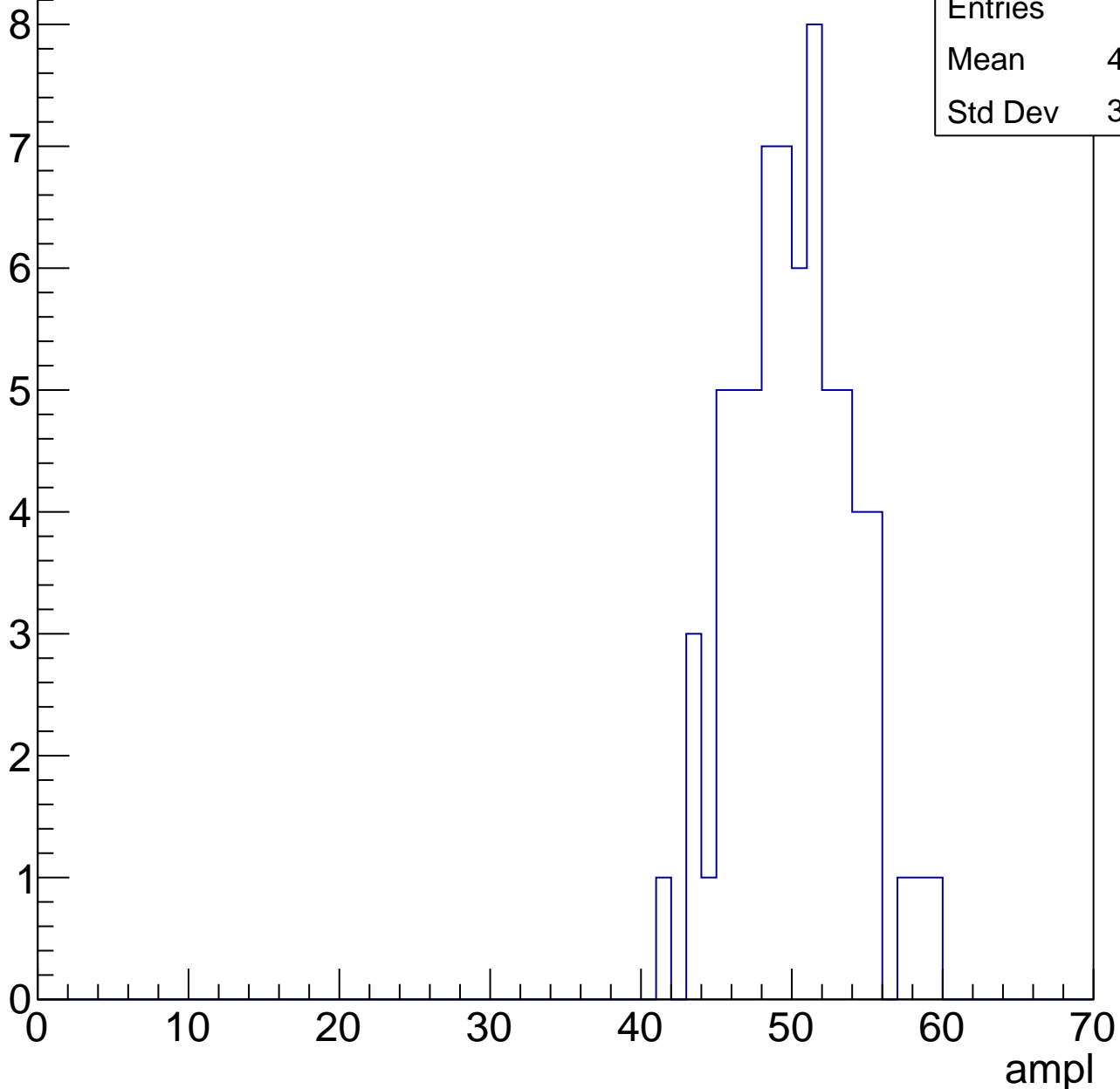


# B1L101S, U20-ch28, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	49.65
Std Dev	3.753

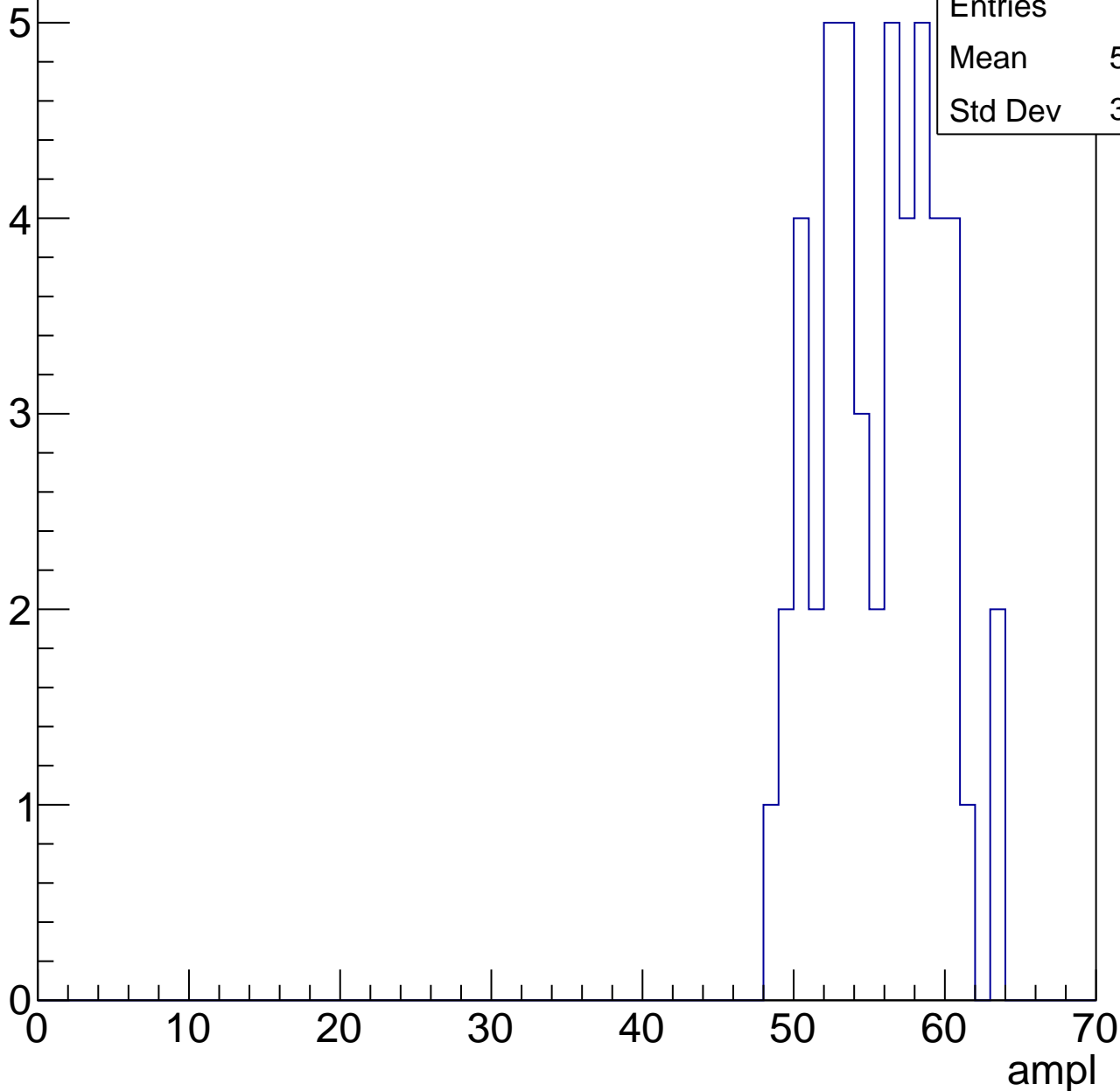


# B1L101S, U20-ch28, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

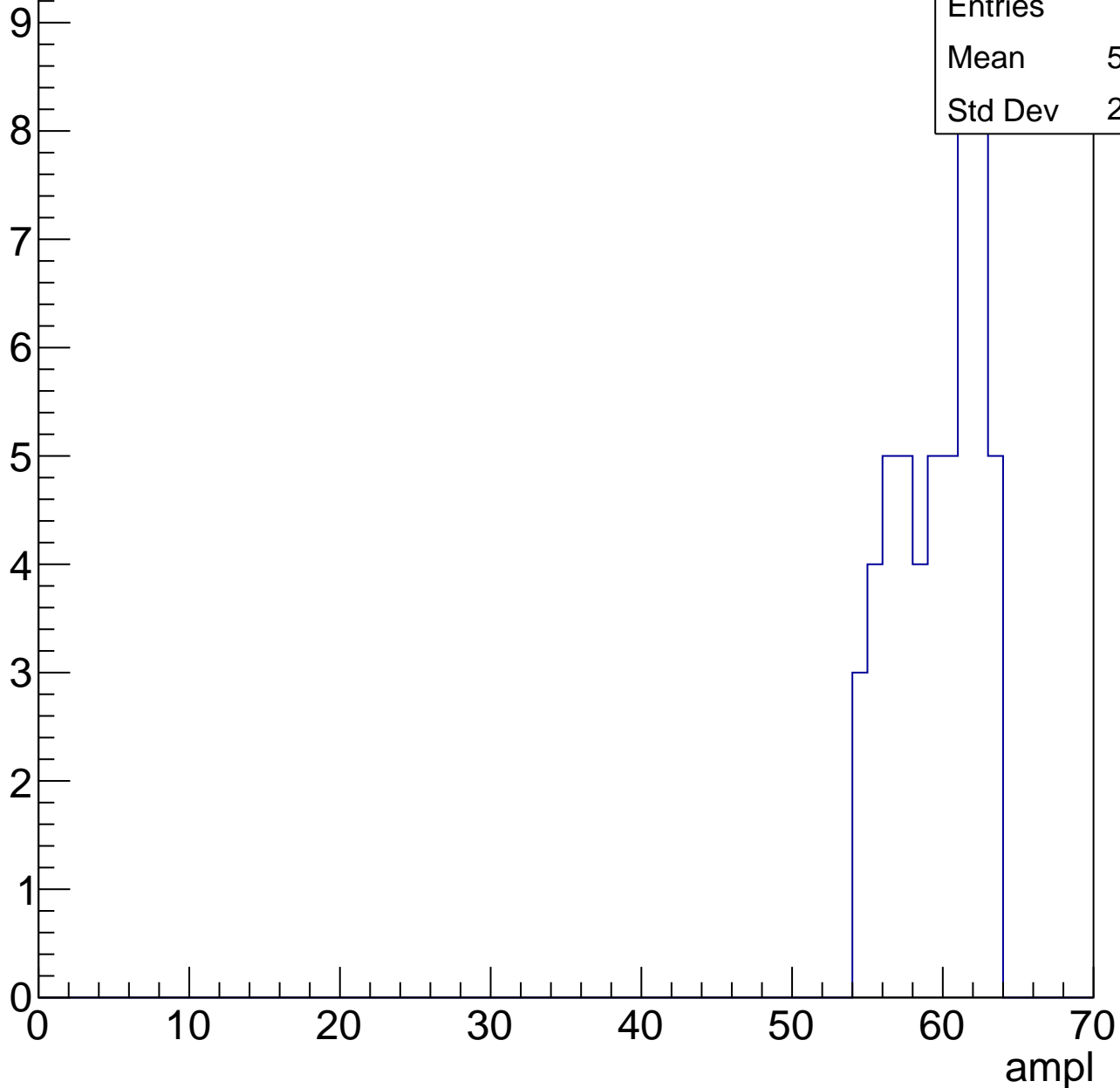
Entries	49
Mean	55.22
Std Dev	3.813



# B1L101S, U20-ch28, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

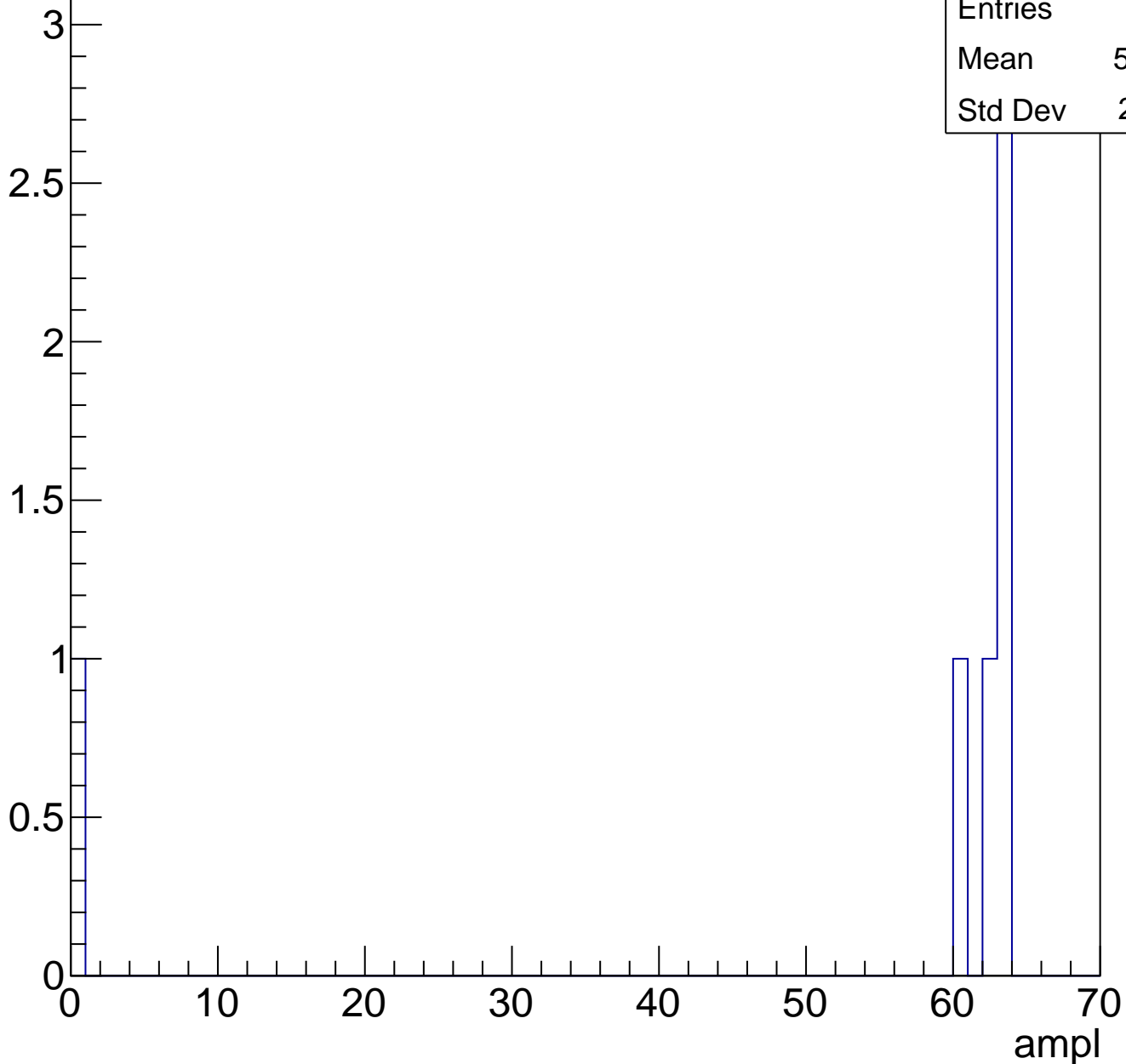
Entry



# B1L101S, U20-ch28, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U20-ch28, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L101S, U20-ch29, adc0

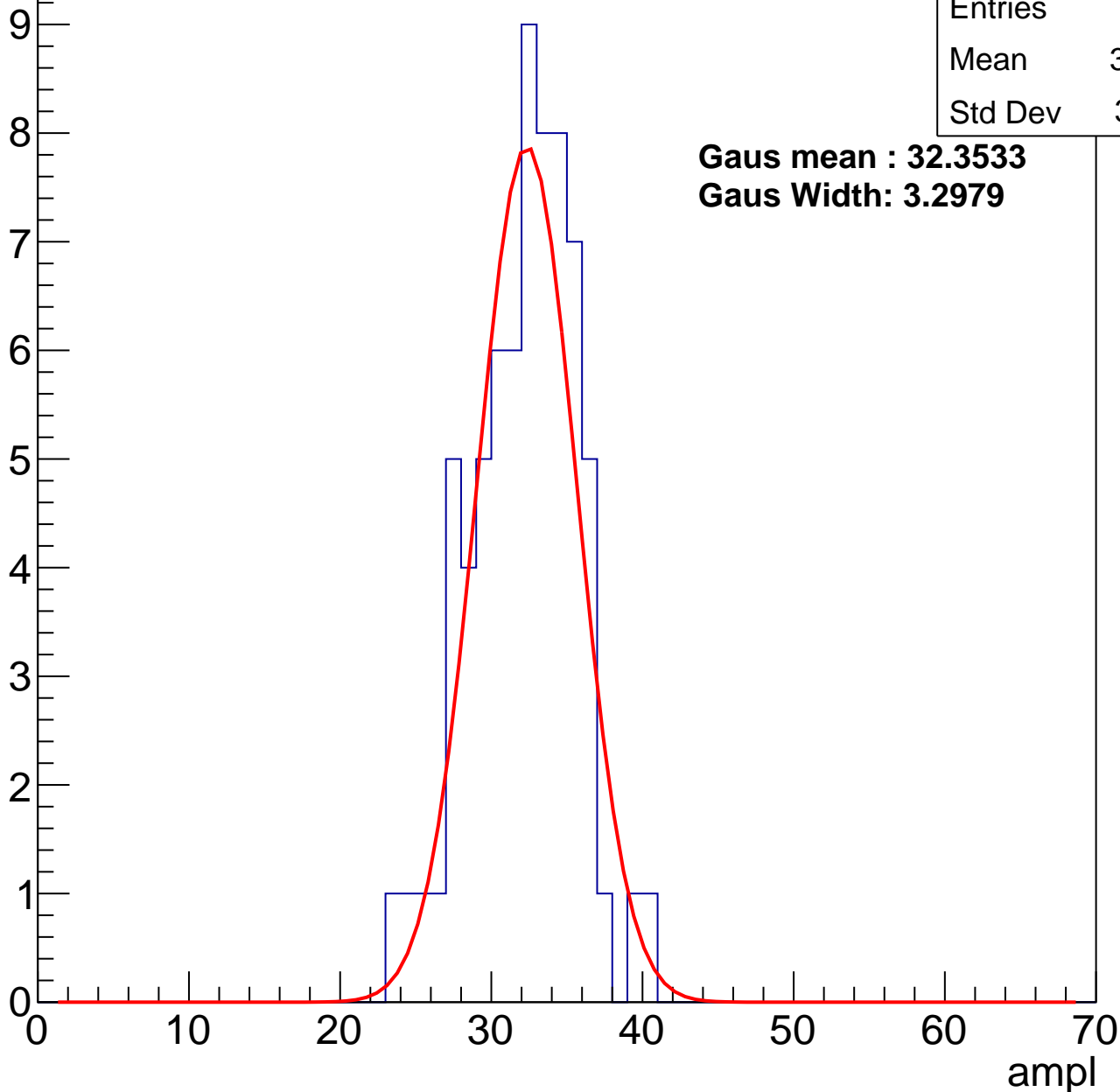
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	31.73
Std Dev	3.401

**Gaus mean : 32.3533**

**Gaus Width: 3.2979**



# B1L101S, U20-ch29, adc1

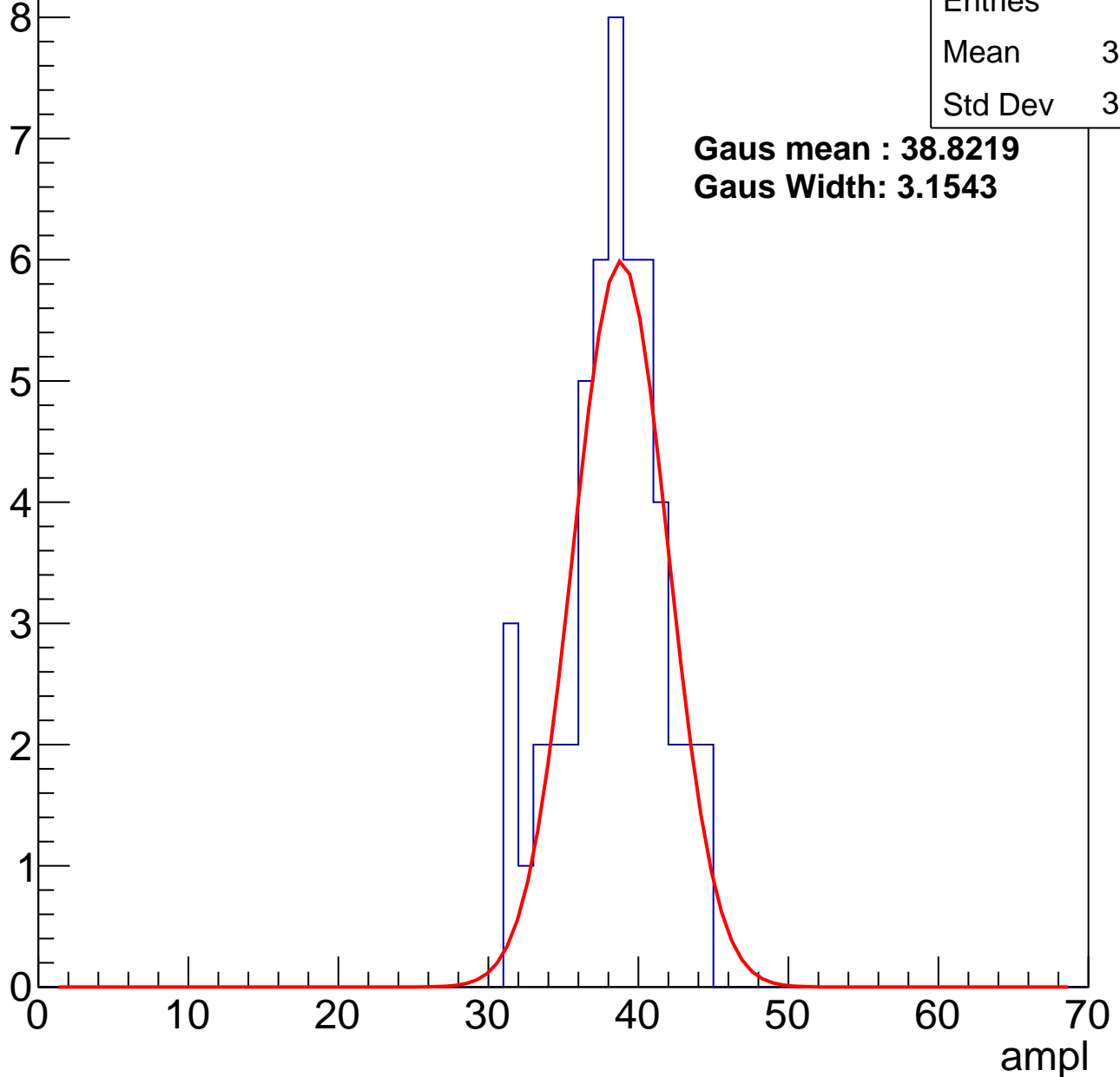
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	51
Mean	37.86
Std Dev	3.218

**Gaus mean : 38.8219**

**Gaus Width: 3.1543**



# B1L101S, U20-ch29, adc2

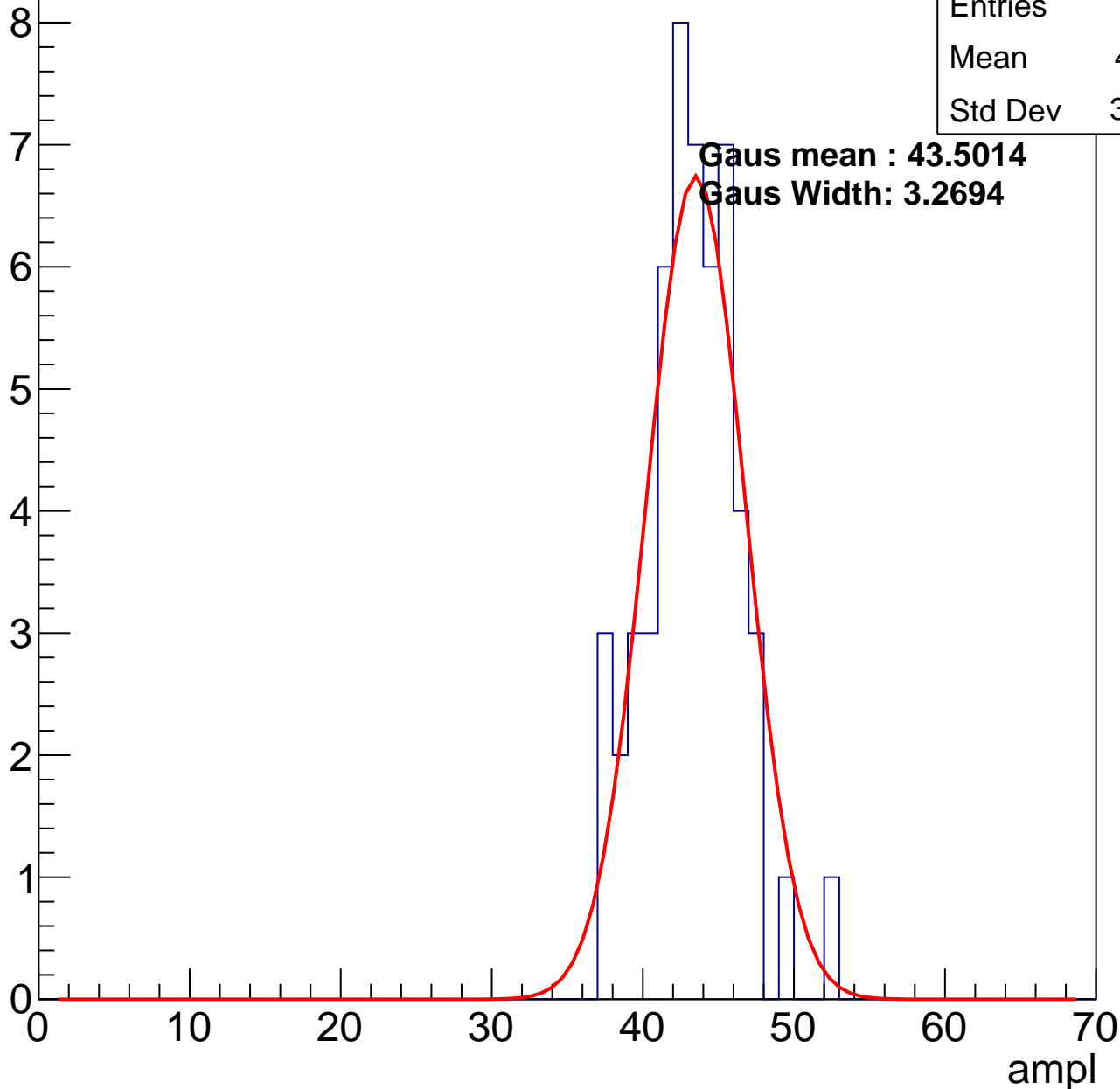
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	54
Mean	42.81
Std Dev	3.037

**Gaus mean : 43.5014**

**Gaus Width: 3.2694**



# B1L101S, U20-ch29, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	70
Mean	49.53
Std Dev	3.106

Entry

10

8

6

4

2

0

0

10

20

30

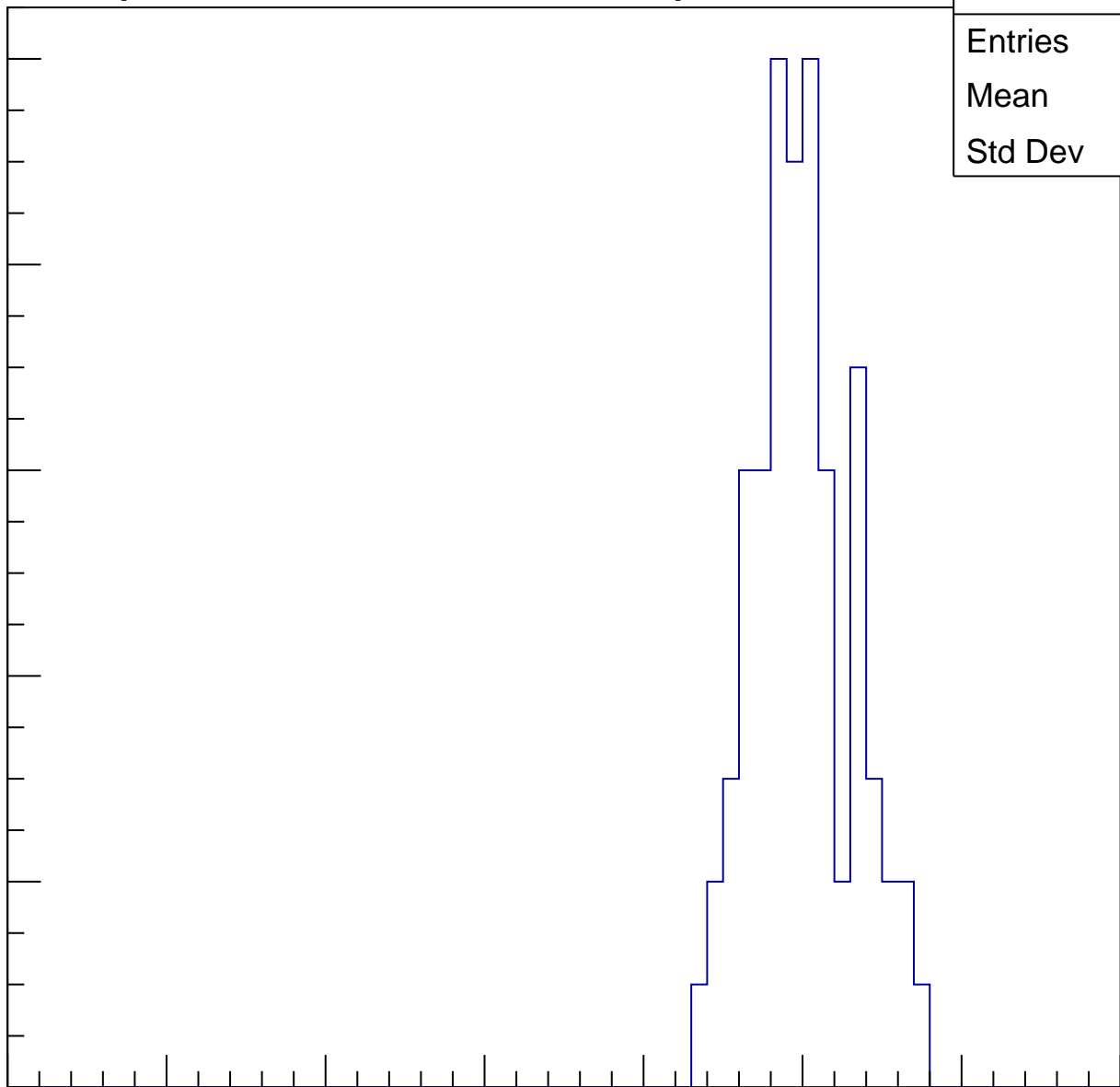
40

50

60

70

ampl

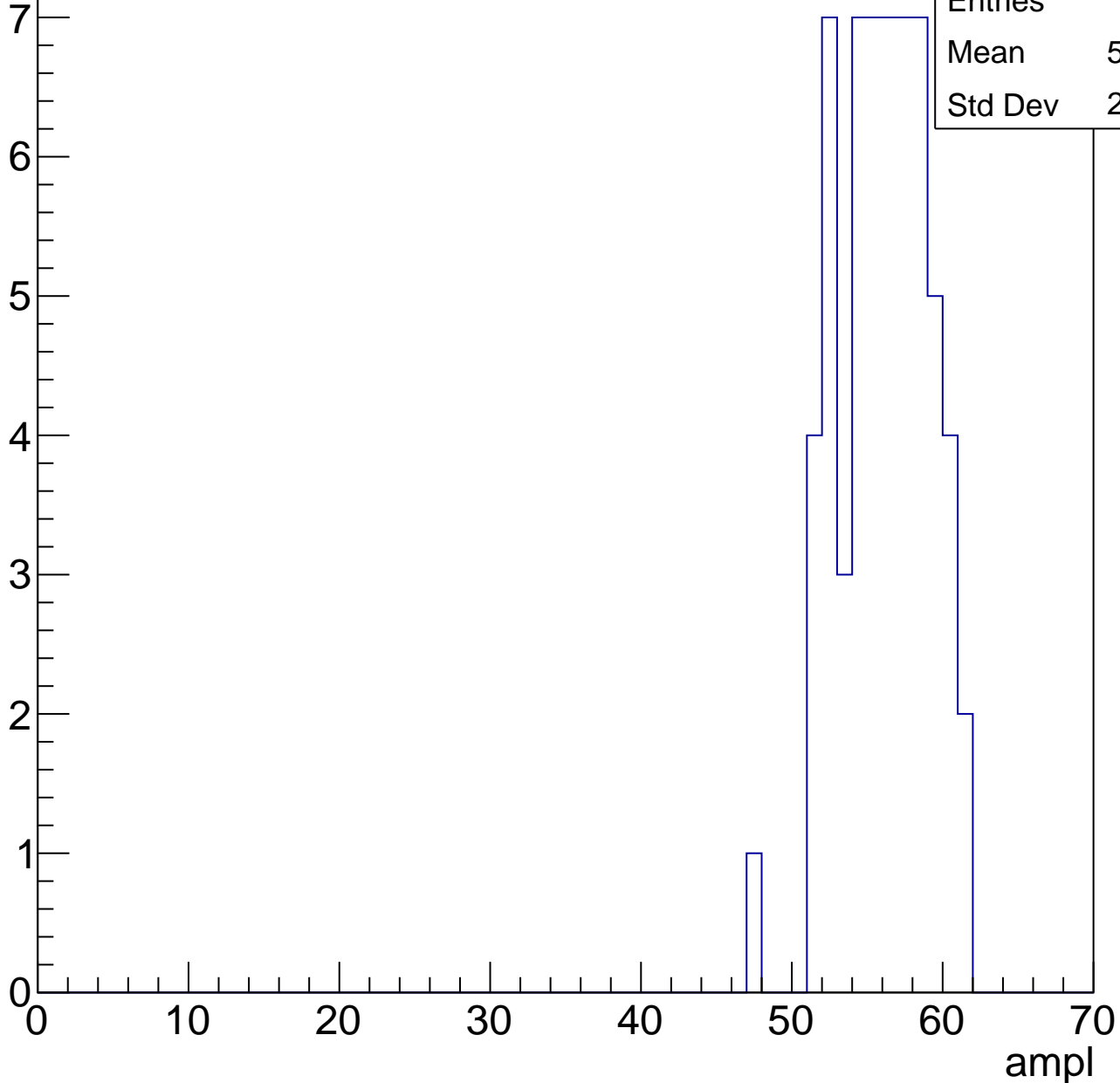


# B1L101S, U20-ch29, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	55.59
Std Dev	2.972



# B1L101S, U20-ch29, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	43
Mean	59.14
Std Dev	9.35

ampl

0

10

20

30

40

50

60

70

# B1L101S, U20-ch29, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U20-ch29, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U20-ch30, adc0

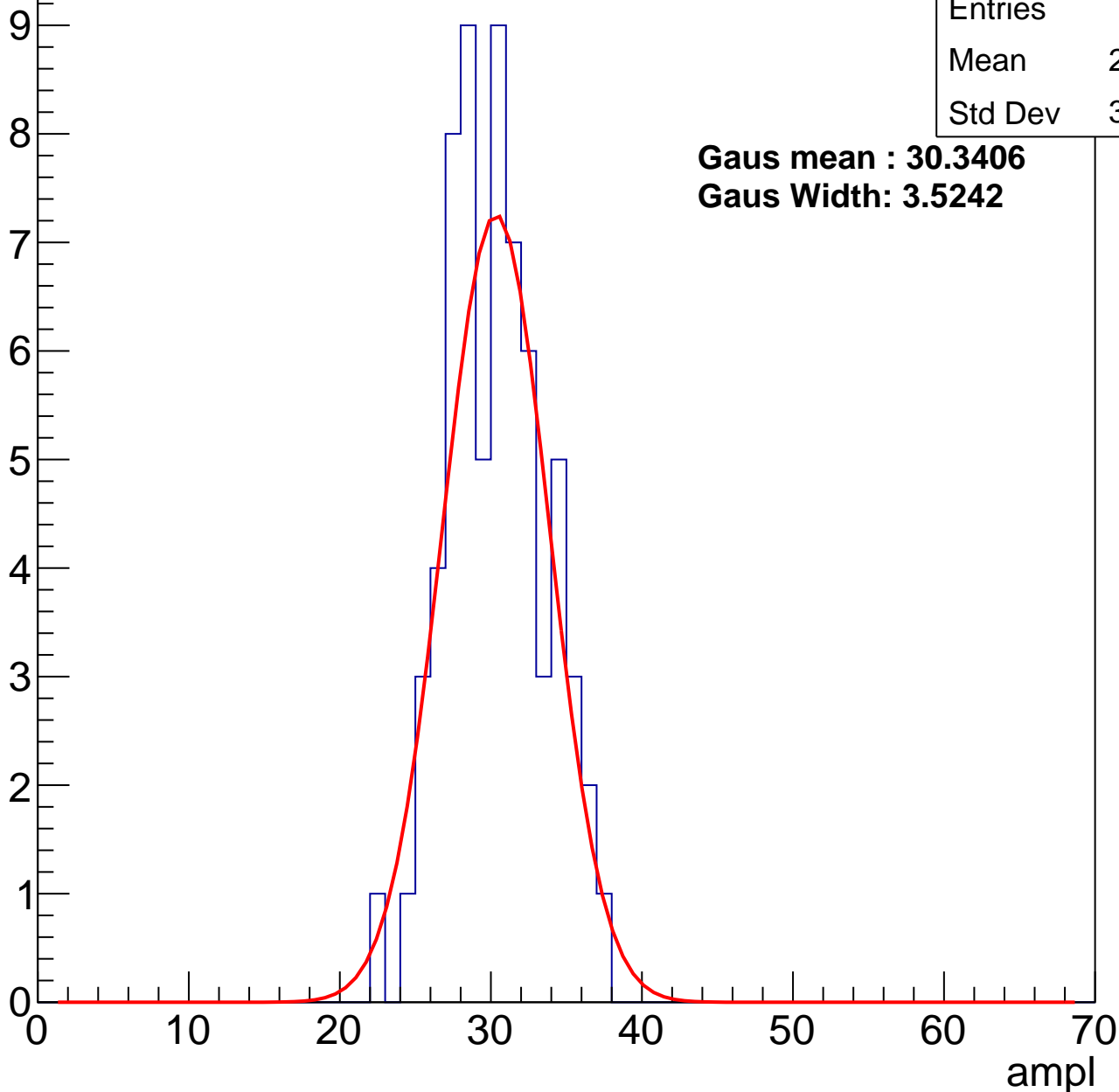
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	67
Mean	29.85
Std Dev	3.196

**Gaus mean : 30.3406**

**Gaus Width: 3.5242**



# B1L101S, U20-ch30, adc1

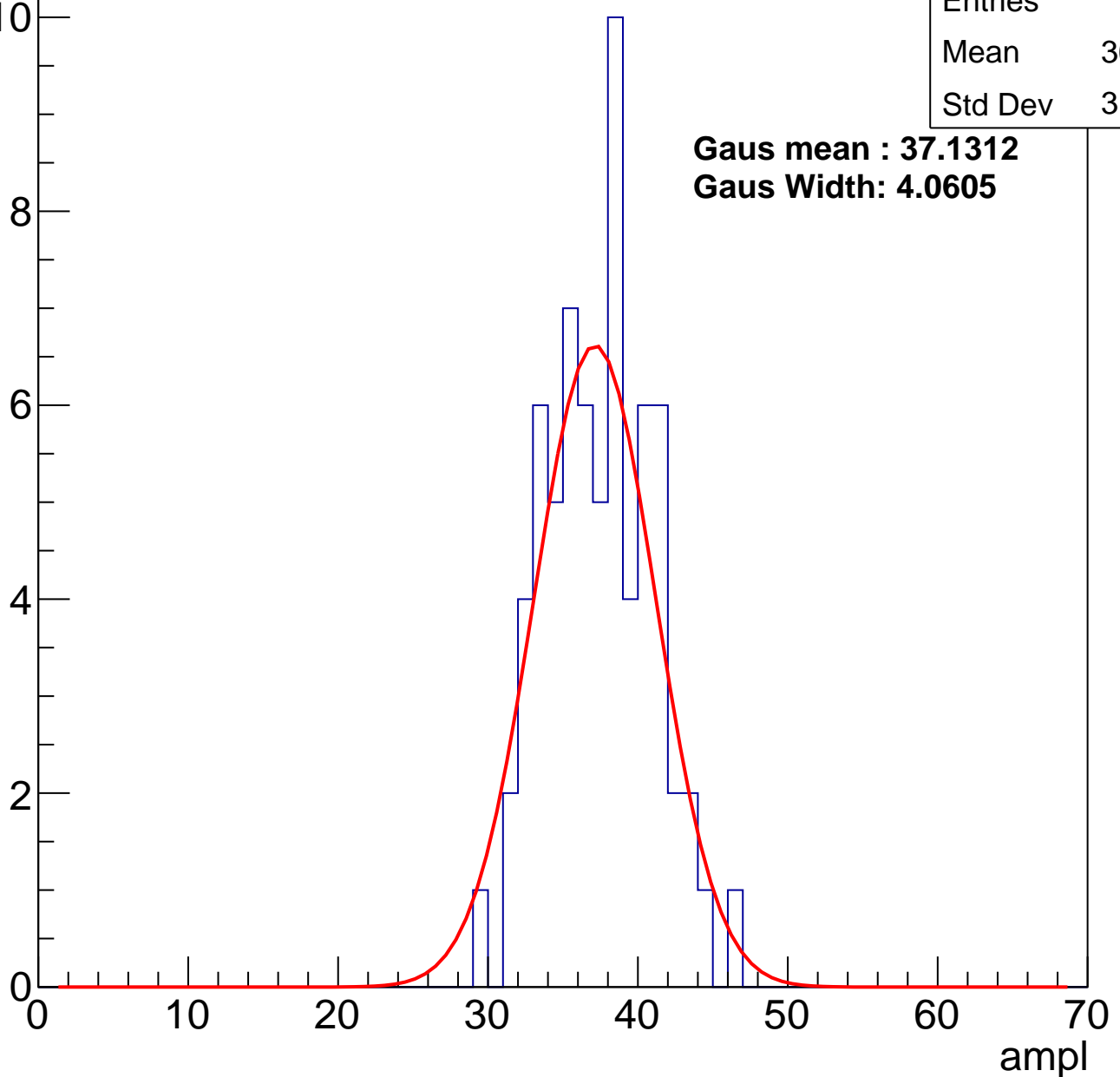
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	36.99
Std Dev	3.513

**Gaus mean : 37.1312**

**Gaus Width: 4.0605**



# B1L101S, U20-ch30, adc2

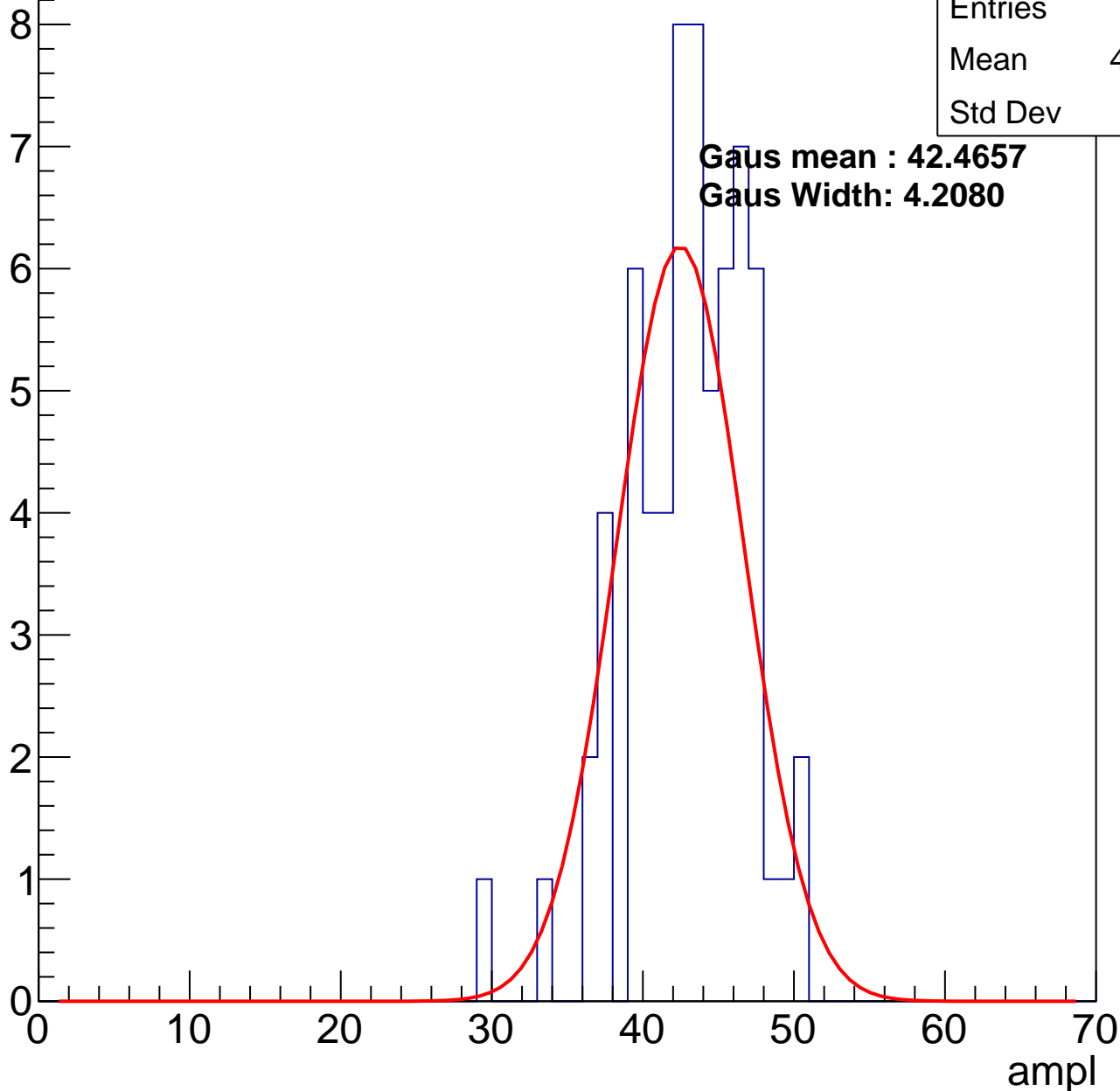
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	66
Mean	42.59
Std Dev	3.95

**Gaus mean : 42.4657**

**Gaus Width: 4.2080**

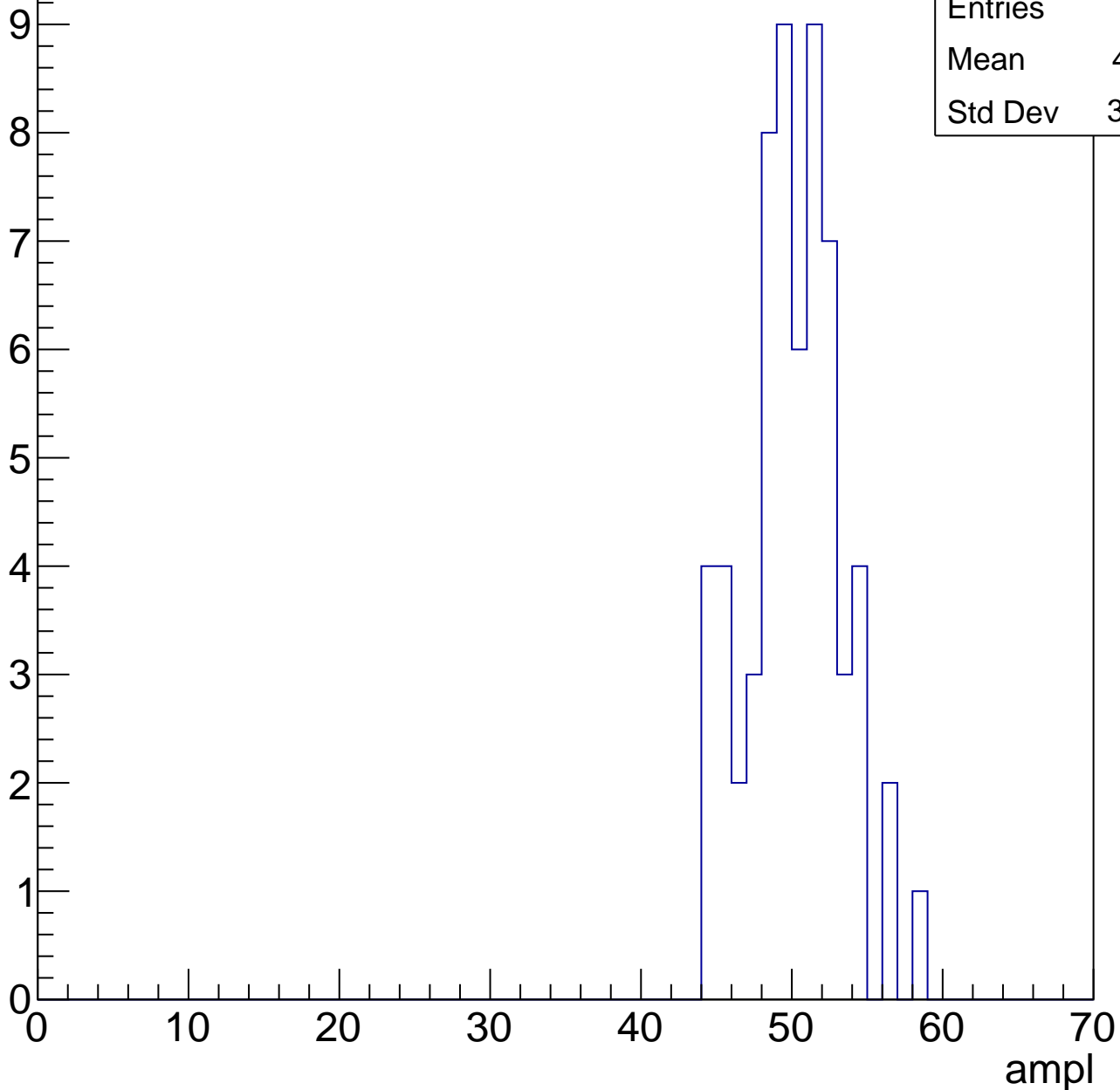


# B1L101S, U20-ch30, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	49.71
Std Dev	3.118

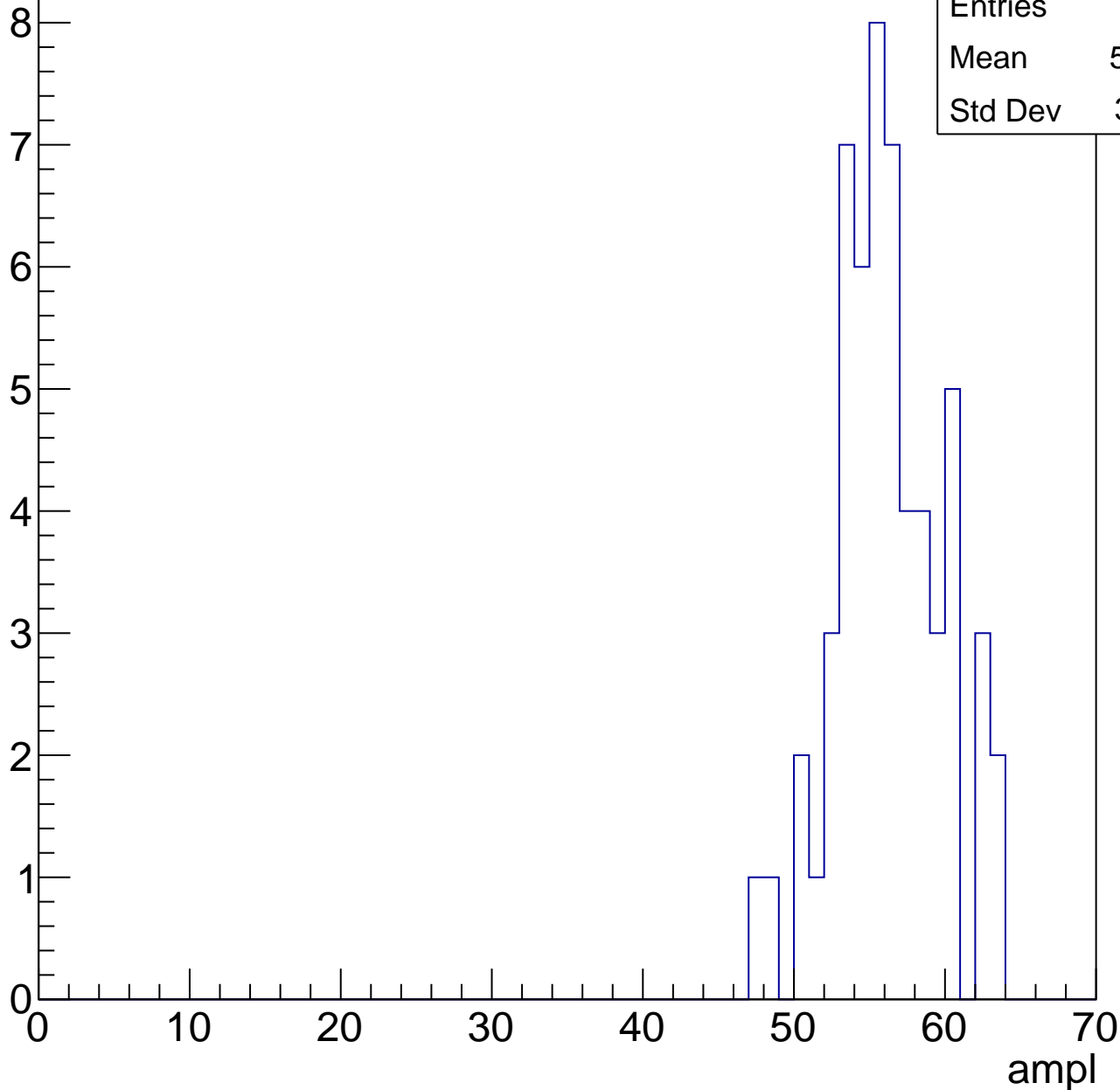


# B1L101S, U20-ch30, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	57
Mean	55.75
Std Dev	3.541

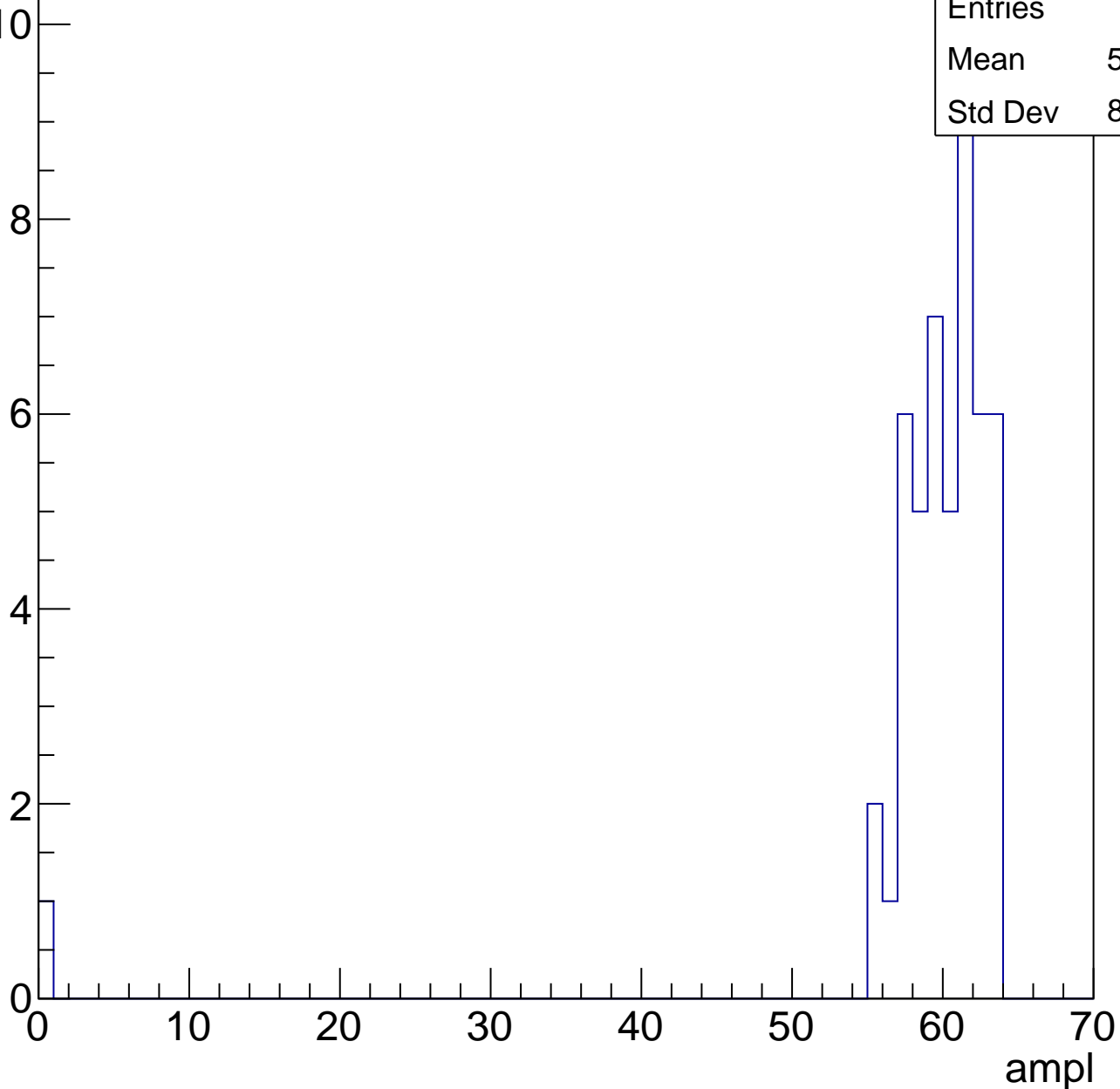


# B1L101S, U20-ch30, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	49
Mean	58.59
Std Dev	8.734



# B1L101S, U20-ch30, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	3
Mean	62.67
Std Dev	0.4714

ampl

0 10 20 30 40 50 60 70



# B1L101S, U20-ch30, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	3
Mean	0
Std Dev	0

# B1L101S, U20-ch31, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	78
Mean	30.81
Std Dev	4.669

**Gaus mean : 31.6518**

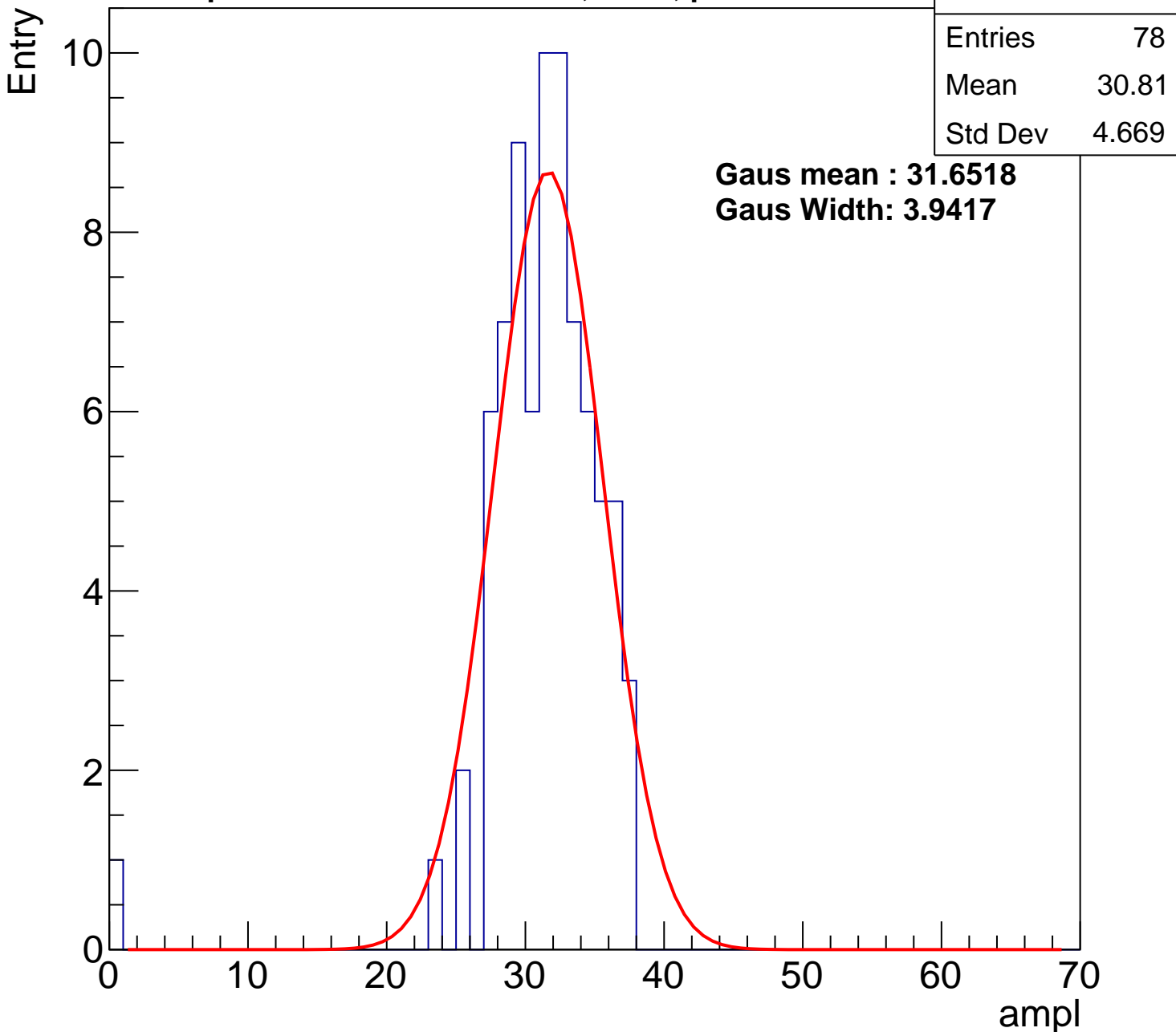
**Gaus Width: 3.9417**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U20-ch31, adc1

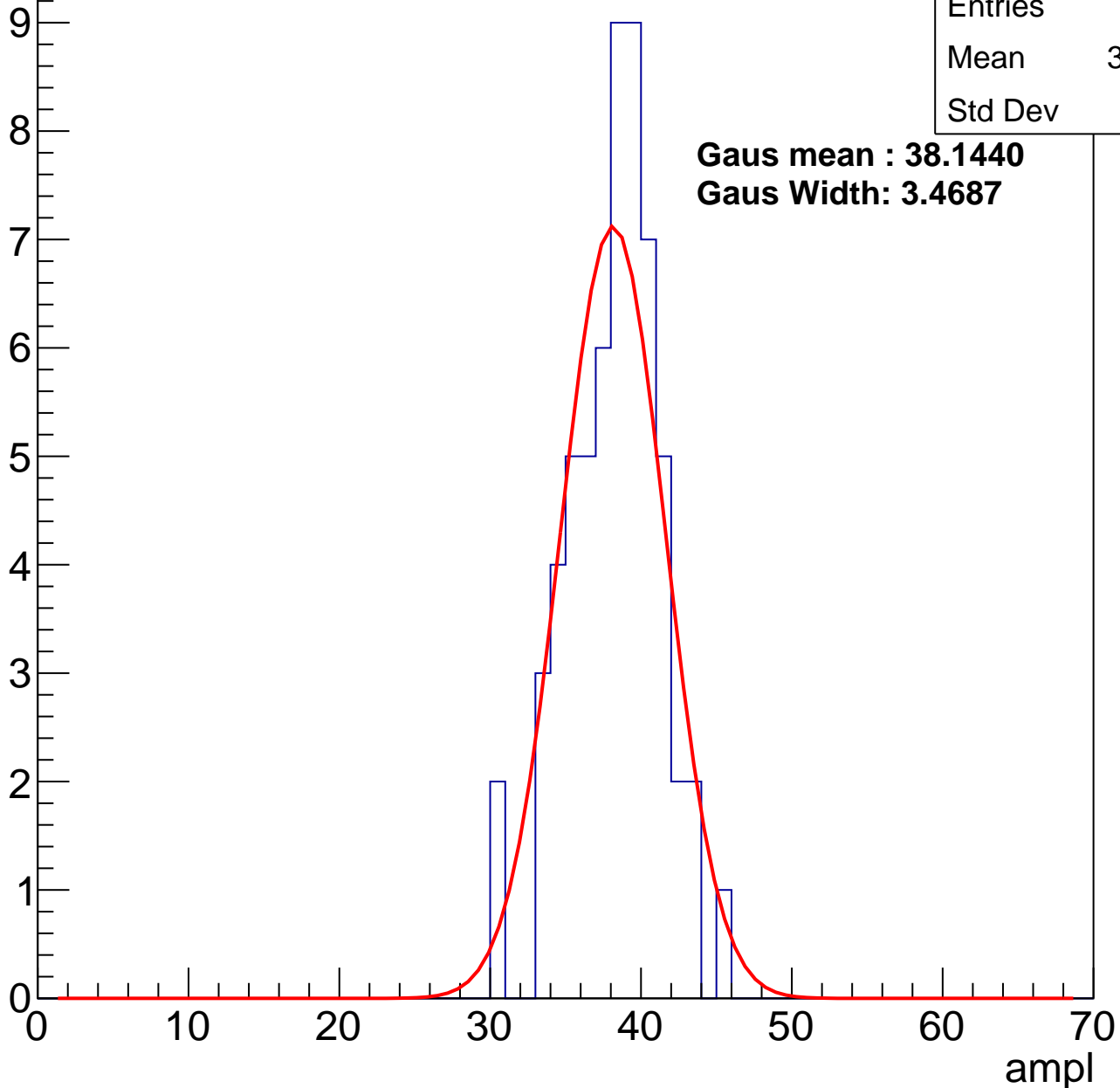
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	60
Mean	37.75
Std Dev	3.02

**Gaus mean : 38.1440**

**Gaus Width: 3.4687**



# B1L101S, U20-ch31, adc2

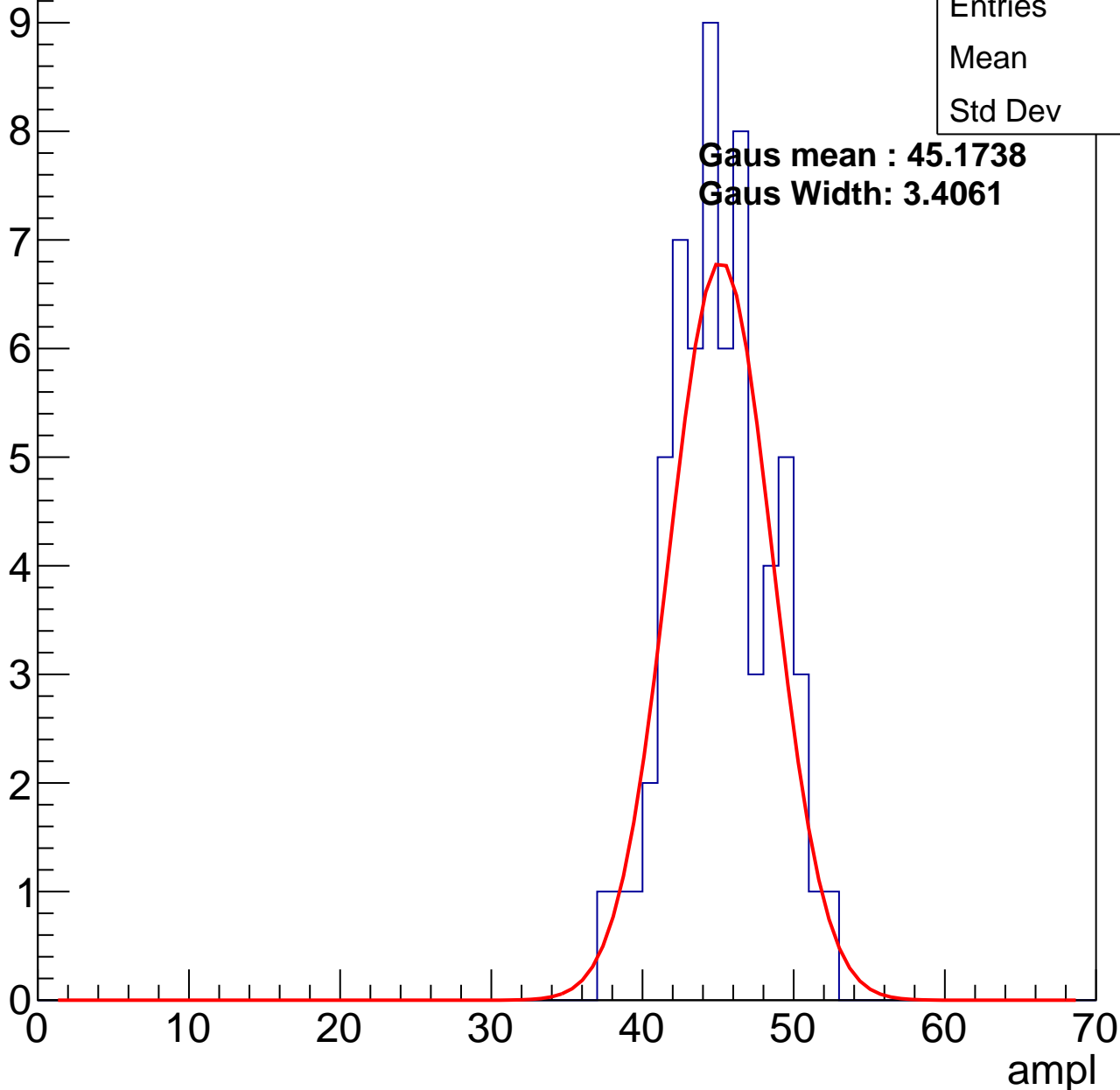
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	44.7
Std Dev	3.25

**Gaus mean : 45.1738**

**Gaus Width: 3.4061**

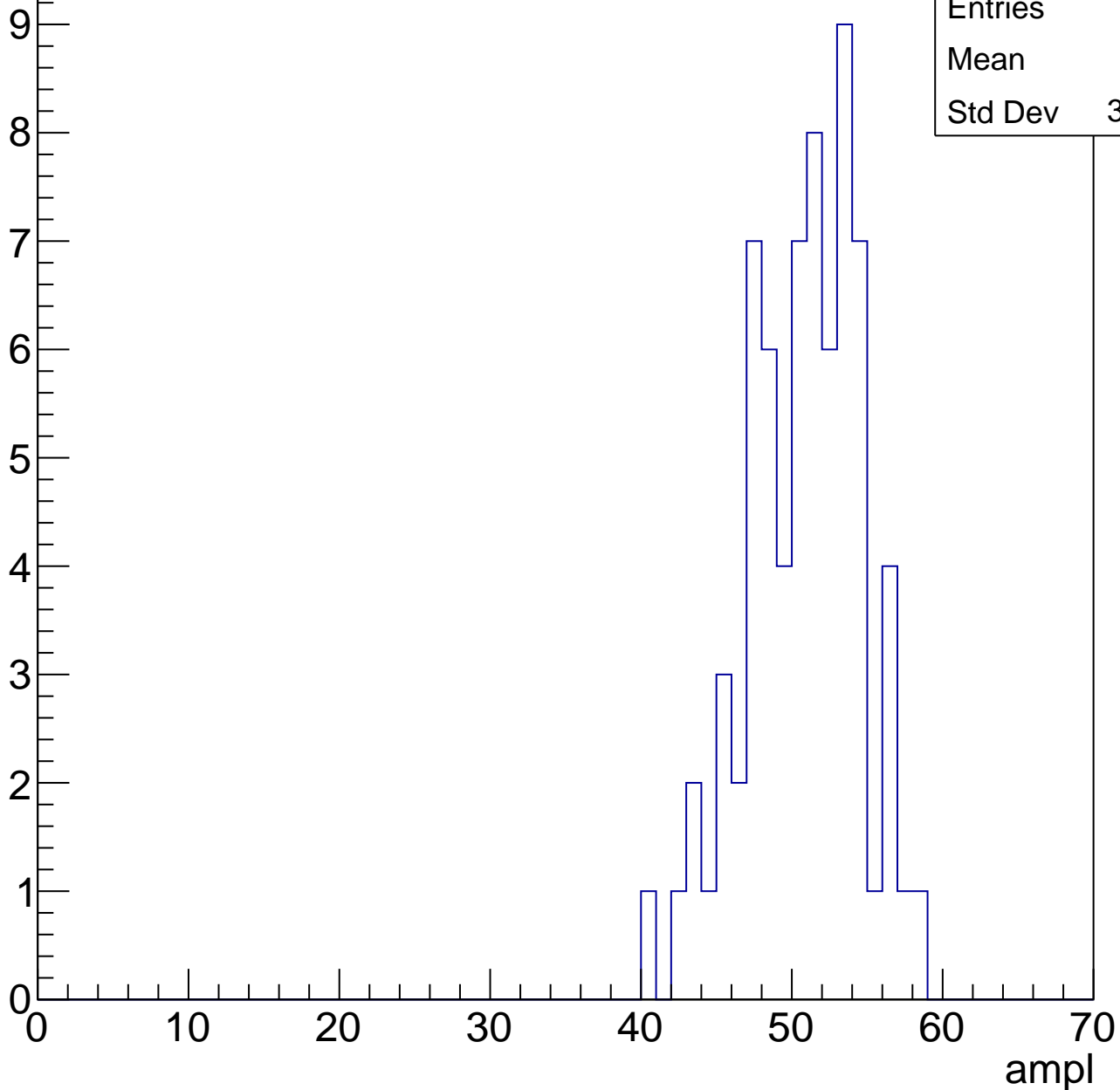


# B1L101S, U20-ch31, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

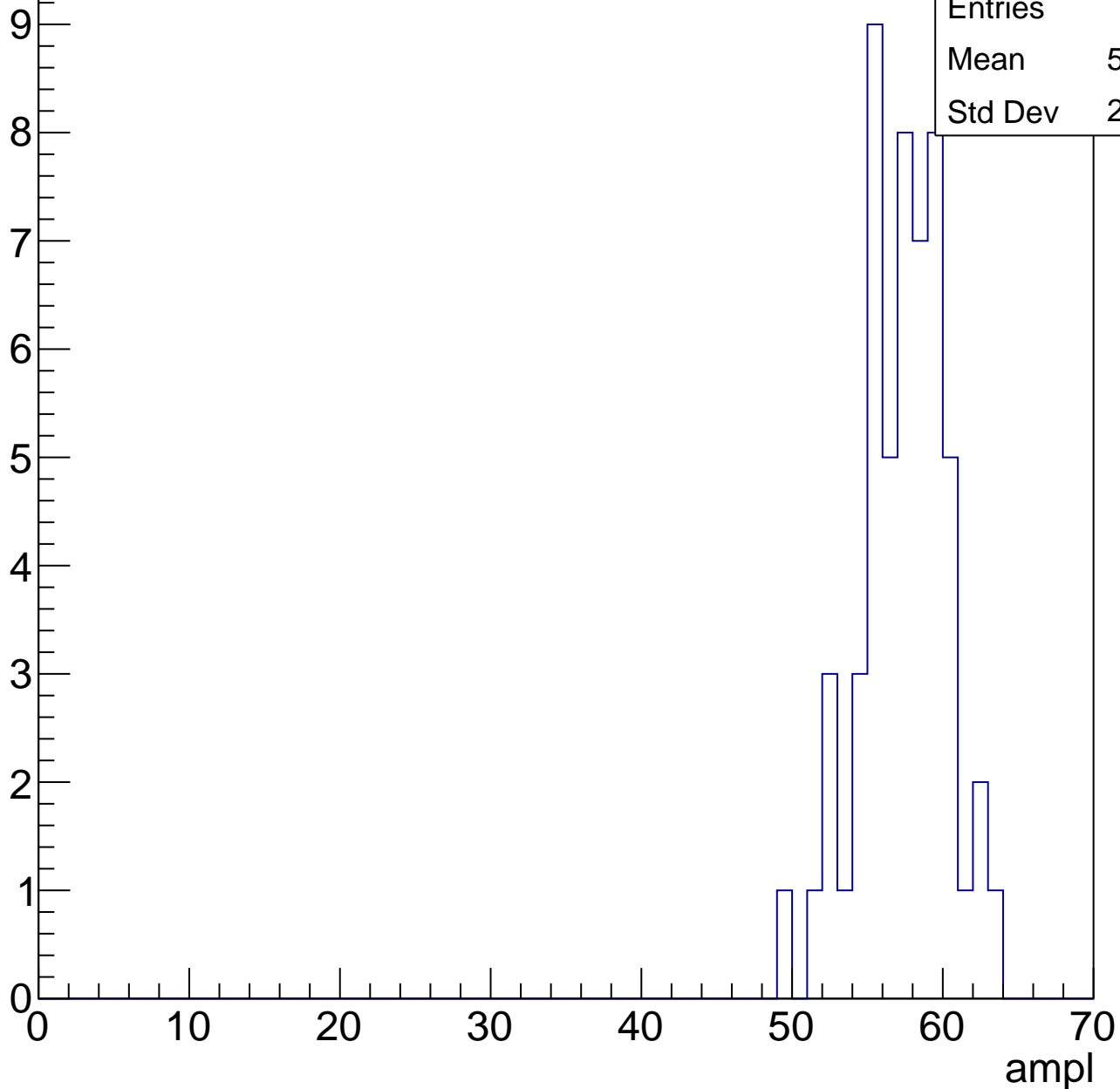
Entries	71
Mean	50.3
Std Dev	3.747



# B1L101S, U20-ch31, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U20-ch31, adc5

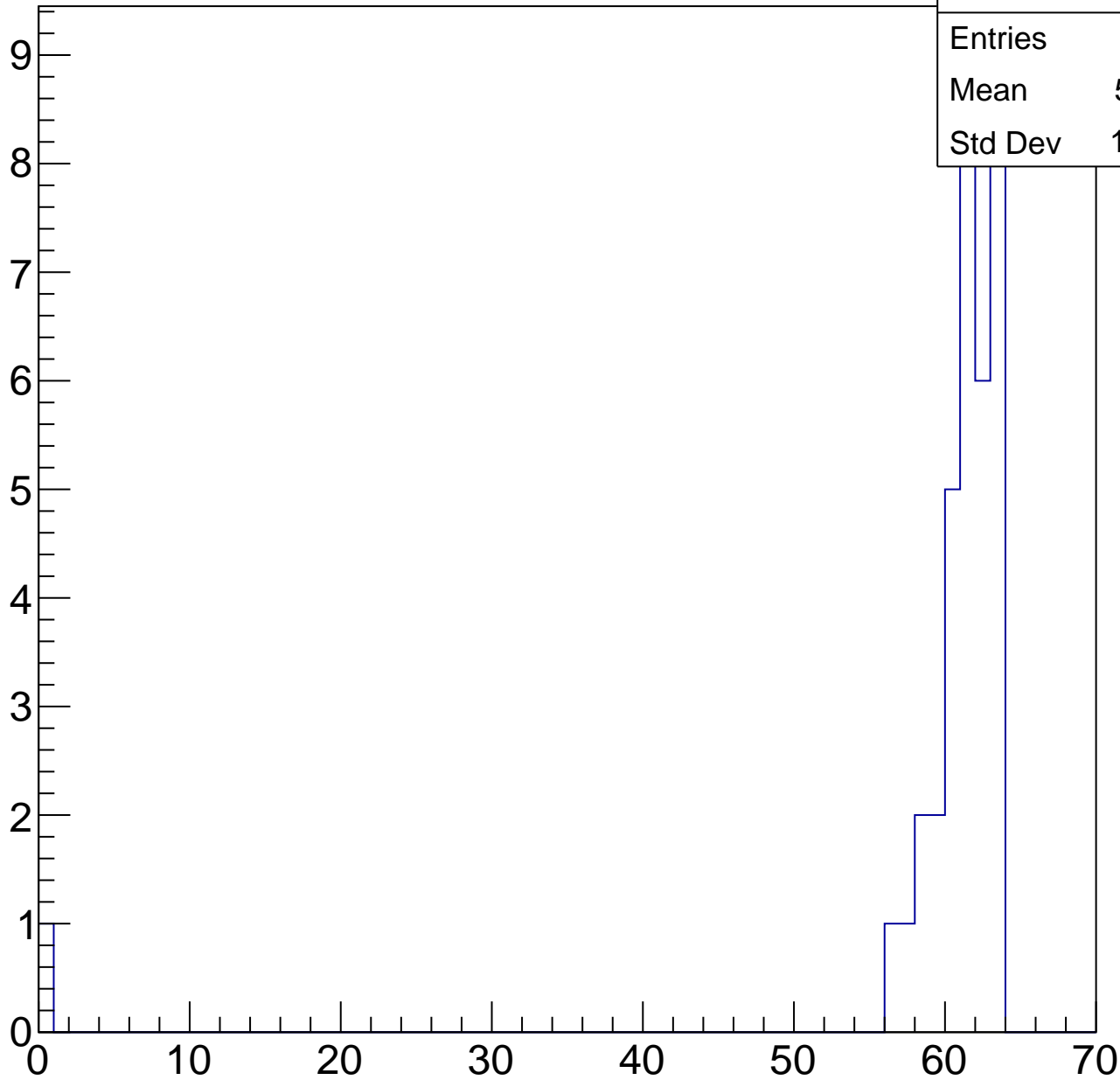
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	36
Mean	59.31
Std Dev	10.18

ampl



# B1L101S, U20-ch31, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U20-ch31, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U20-ch32, adc0

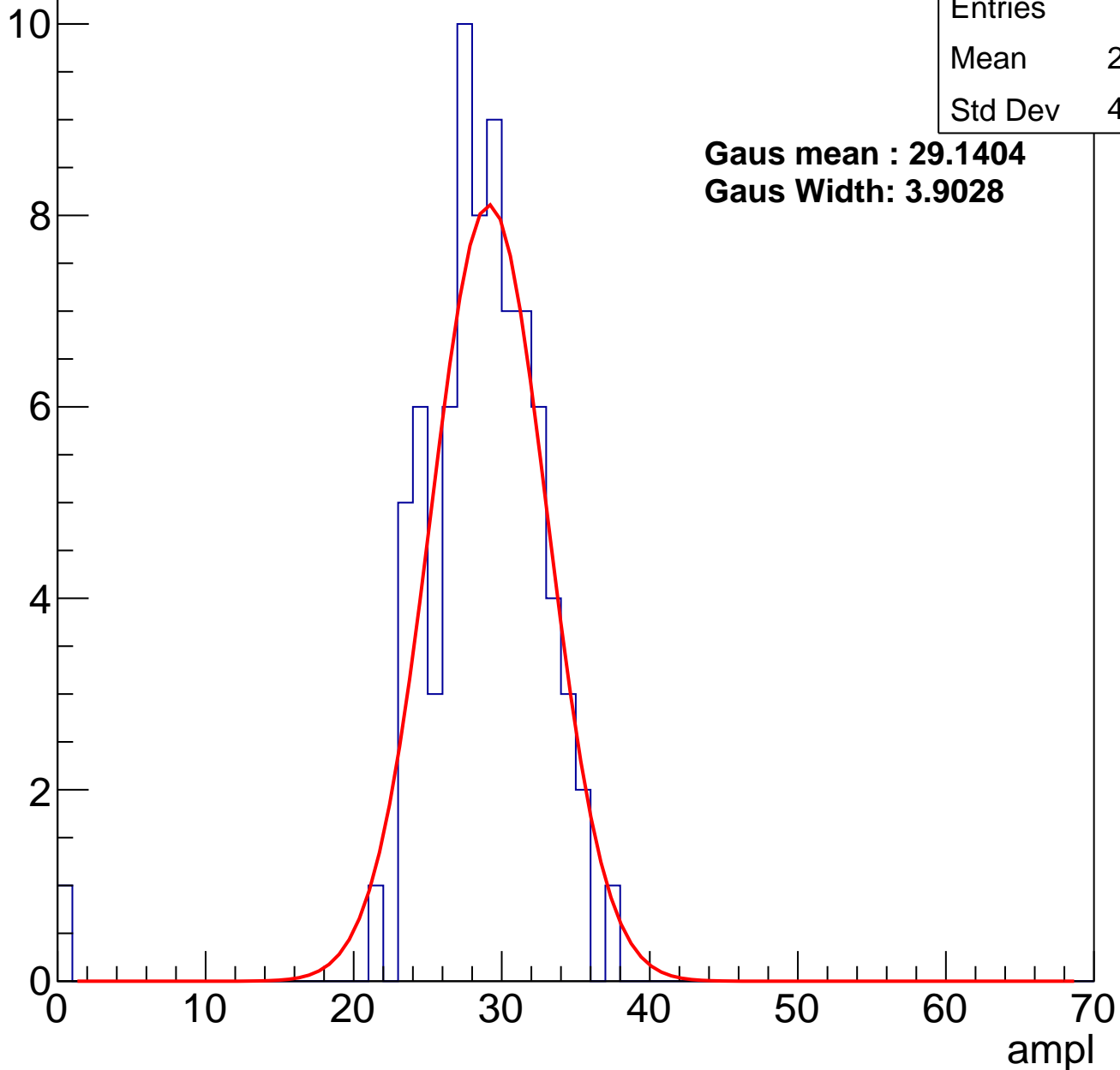
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	79
Mean	28.18
Std Dev	4.633

**Gaus mean : 29.1404**

**Gaus Width: 3.9028**

Entry



# B1L101S, U20-ch32, adc1

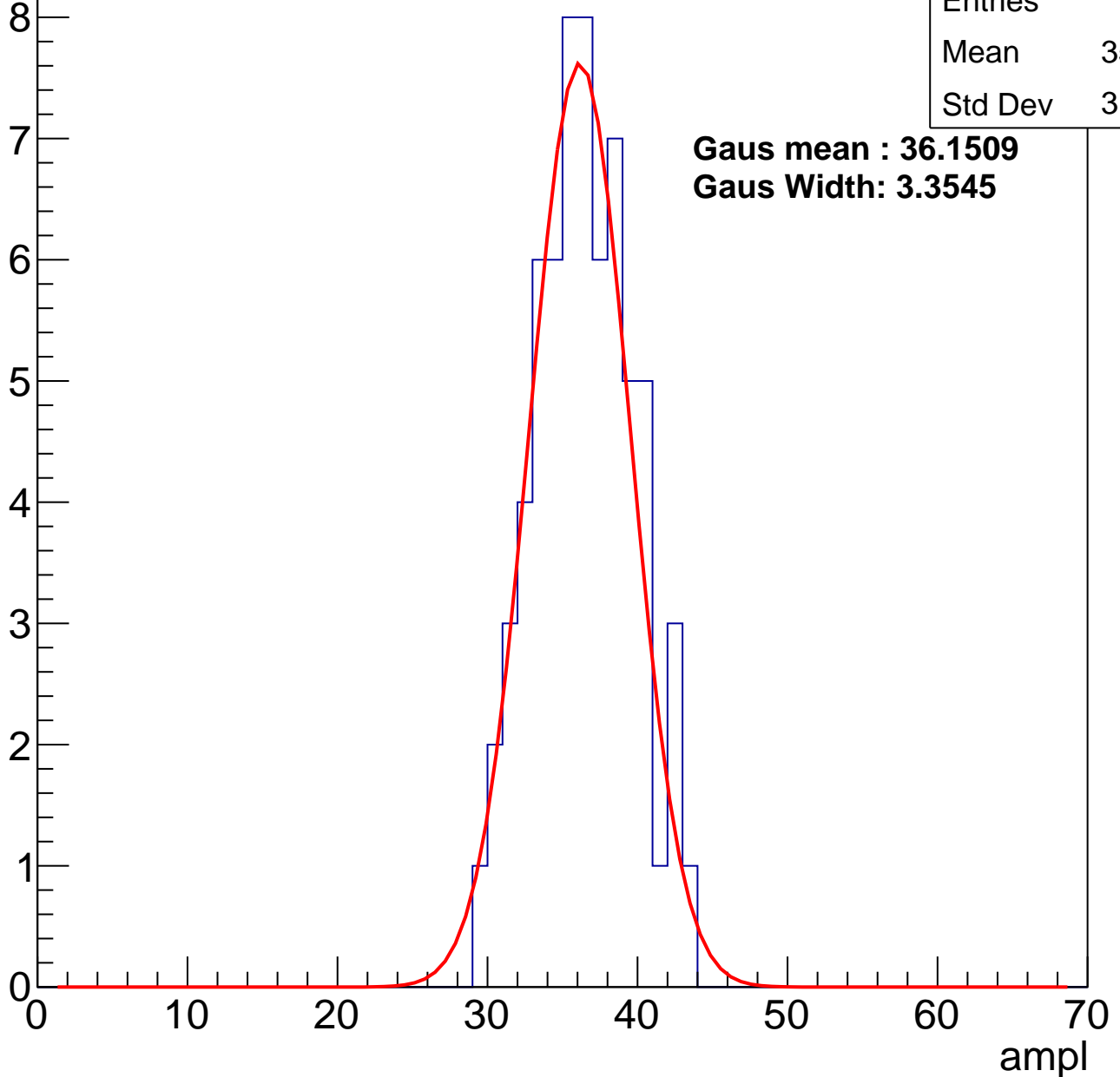
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	66
Mean	35.95
Std Dev	3.226

**Gaus mean : 36.1509**

**Gaus Width: 3.3545**



# B1L101S, U20-ch32, adc2

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	66
Mean	42.36
Std Dev	3.278

**Gaus mean : 42.8072**

**Gaus Width: 3.7428**

10

8

6

4

2

0

ampl

0

10

20

30

40

50

60

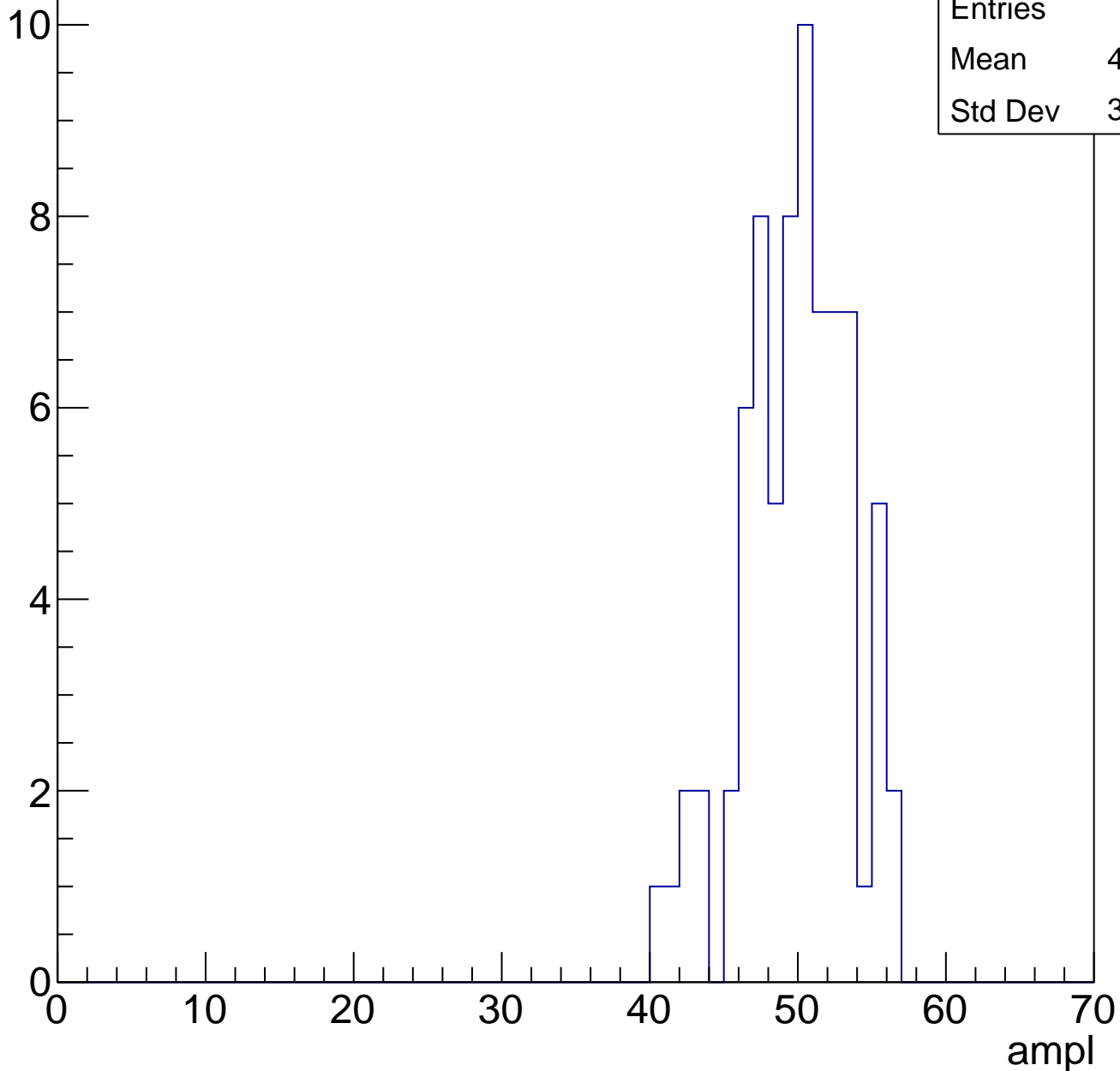
70

# B1L101S, U20-ch32, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	74
Mean	49.43
Std Dev	3.564

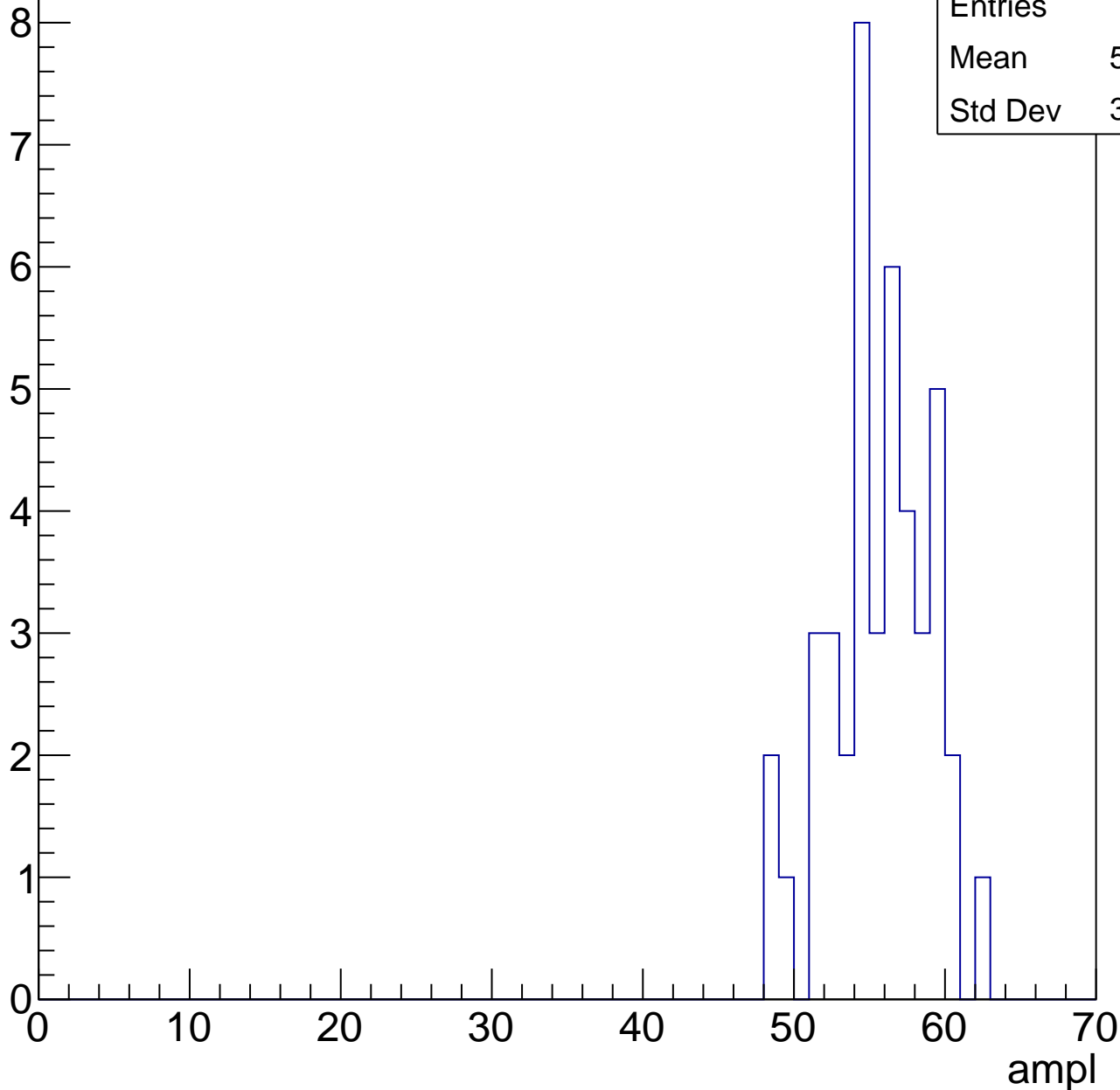


# B1L101S, U20-ch32, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

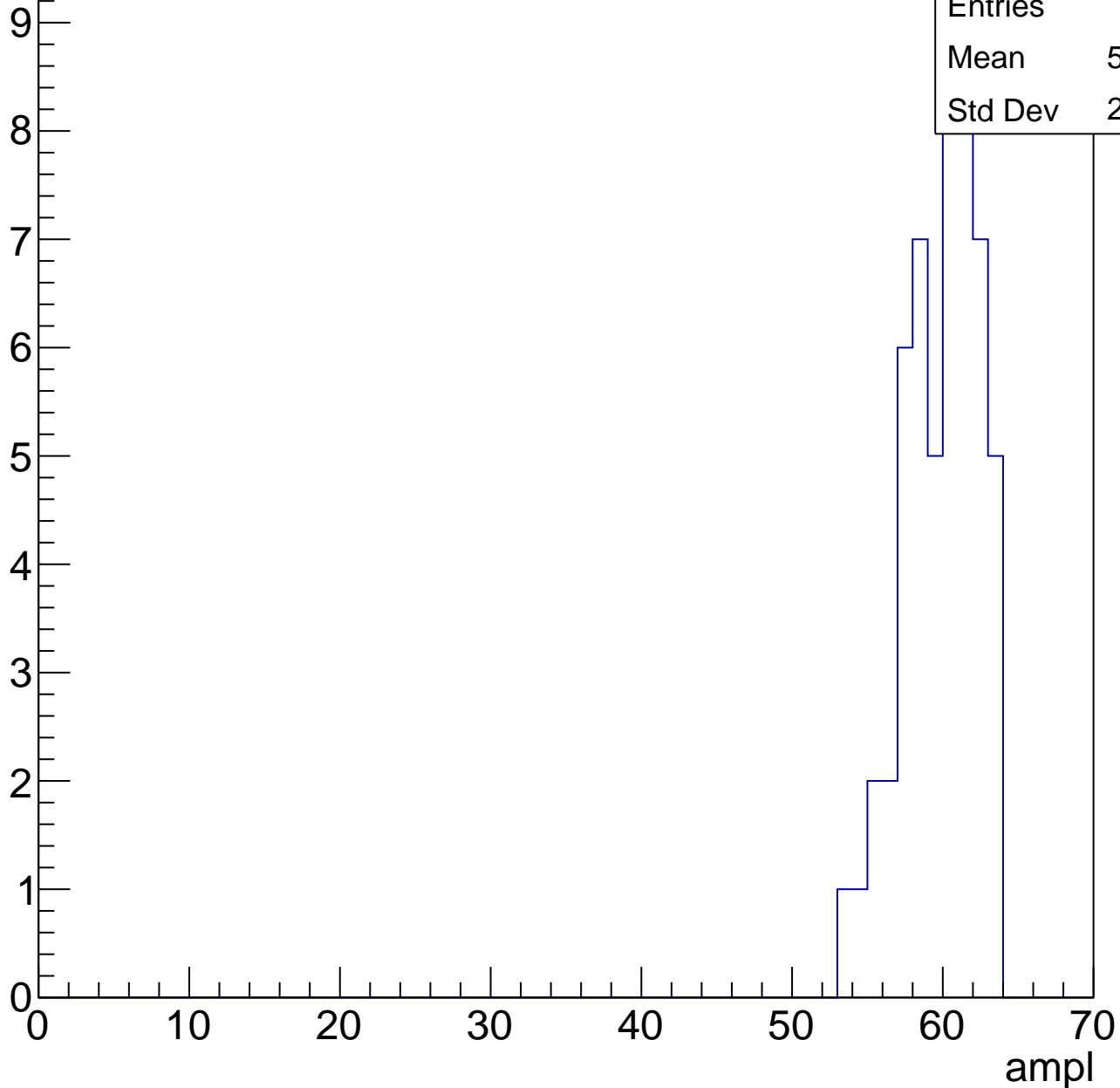
Entries	43
Mean	55.16
Std Dev	3.242



# B1L101S, U20-ch32, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U20-ch32, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U20-ch32, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	3
Mean	21
Std Dev	29.7

# B1L101S, U20-ch33, adc0

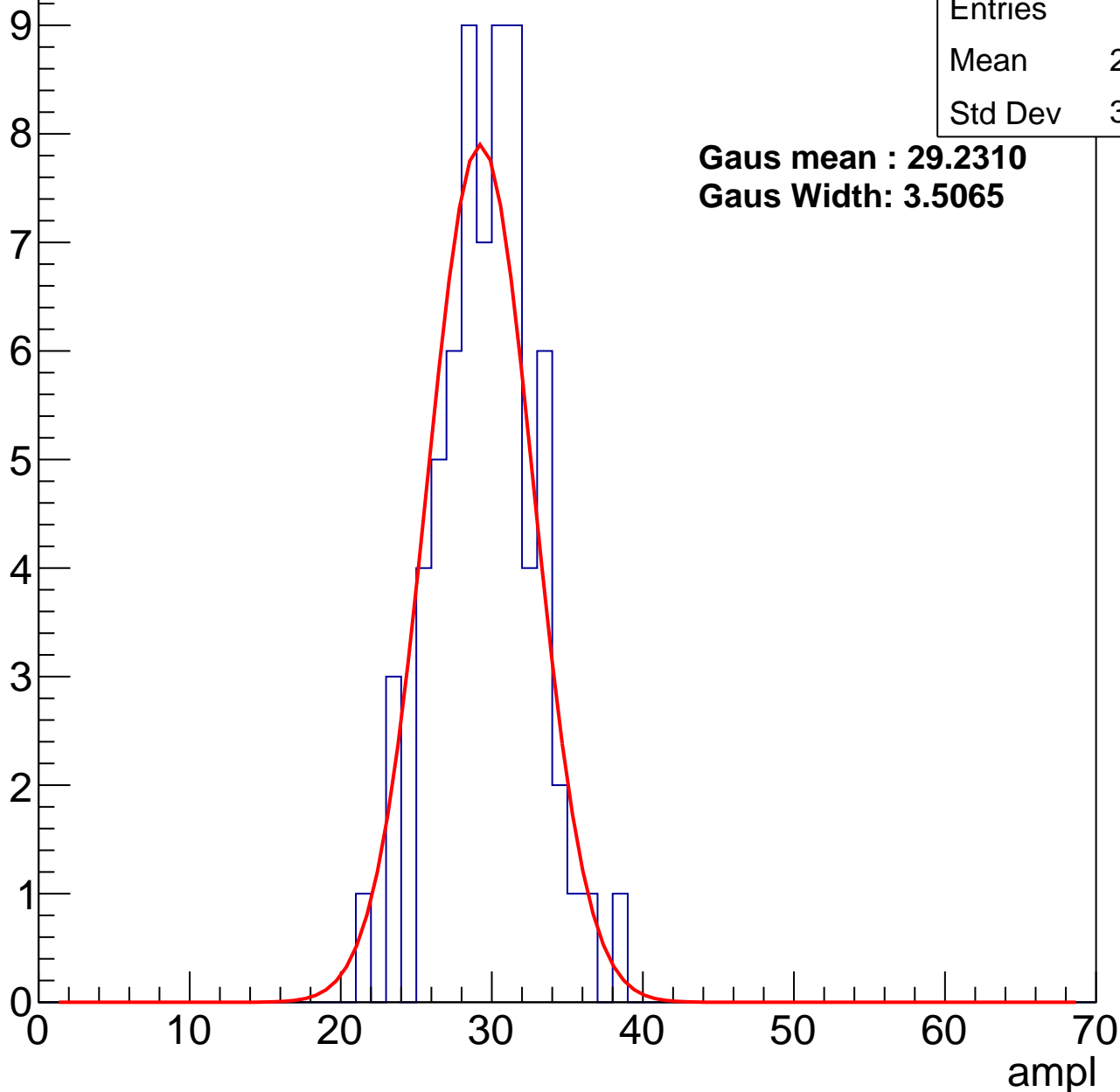
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	29.25
Std Dev	3.215

**Gaus mean : 29.2310**

**Gaus Width: 3.5065**



# B1L101S, U20-ch33, adc1

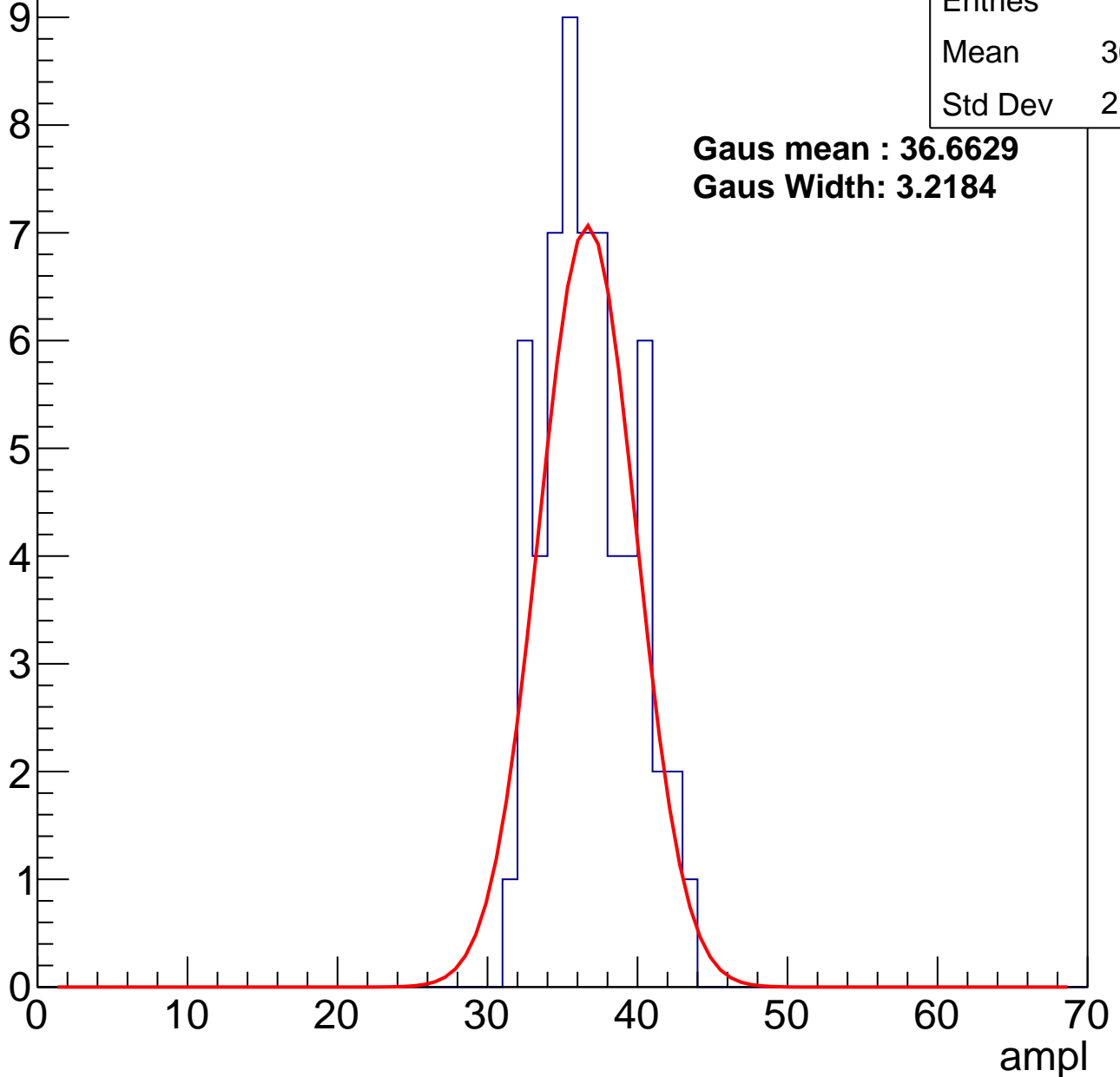
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	60
Mean	36.27
Std Dev	2.932

**Gaus mean : 36.6629**

**Gaus Width: 3.2184**



# B1L101S, U20-ch33, adc2

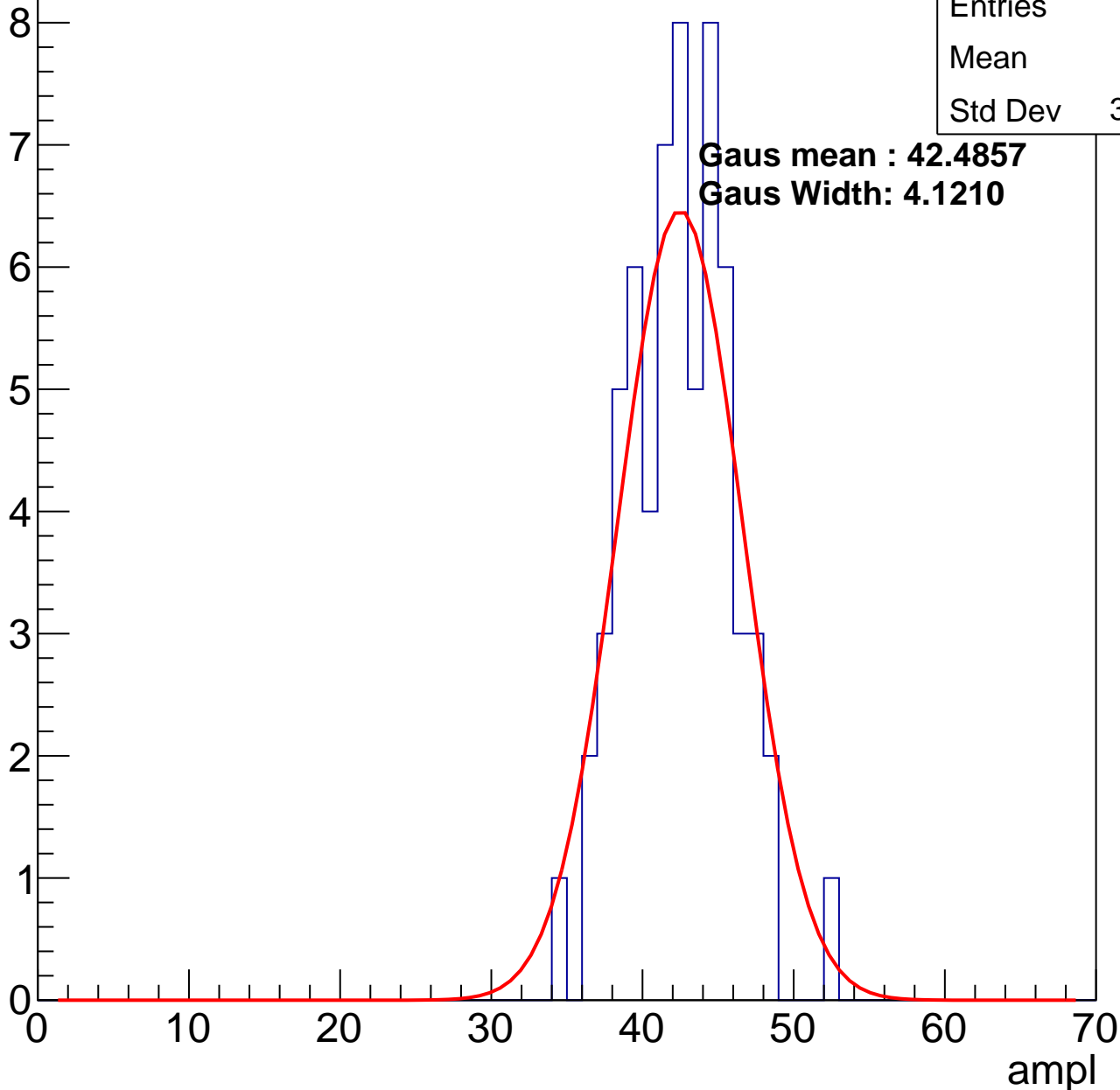
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	42
Std Dev	3.432

**Gaus mean : 42.4857**

**Gaus Width: 4.1210**

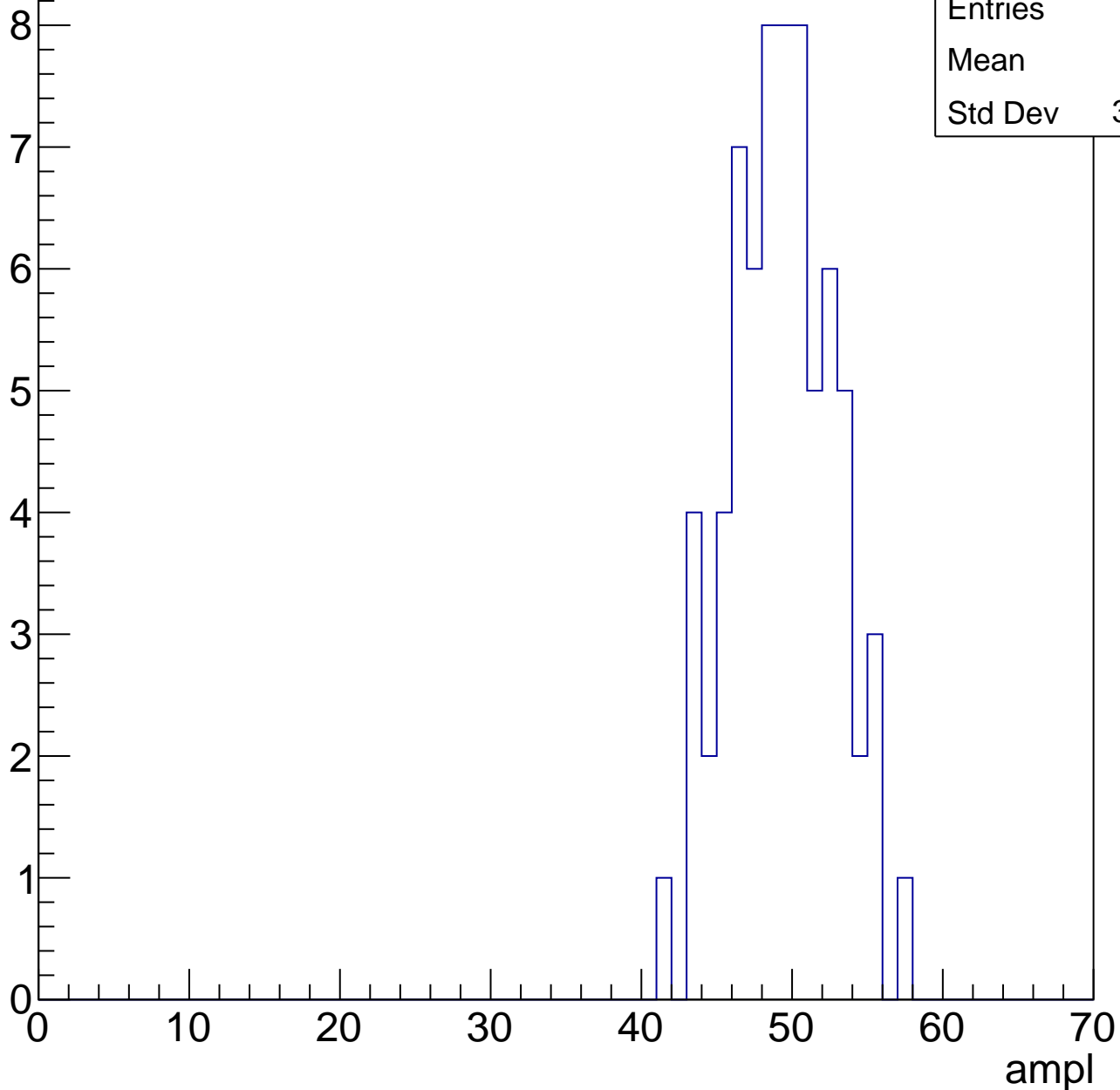


# B1L101S, U20-ch33, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

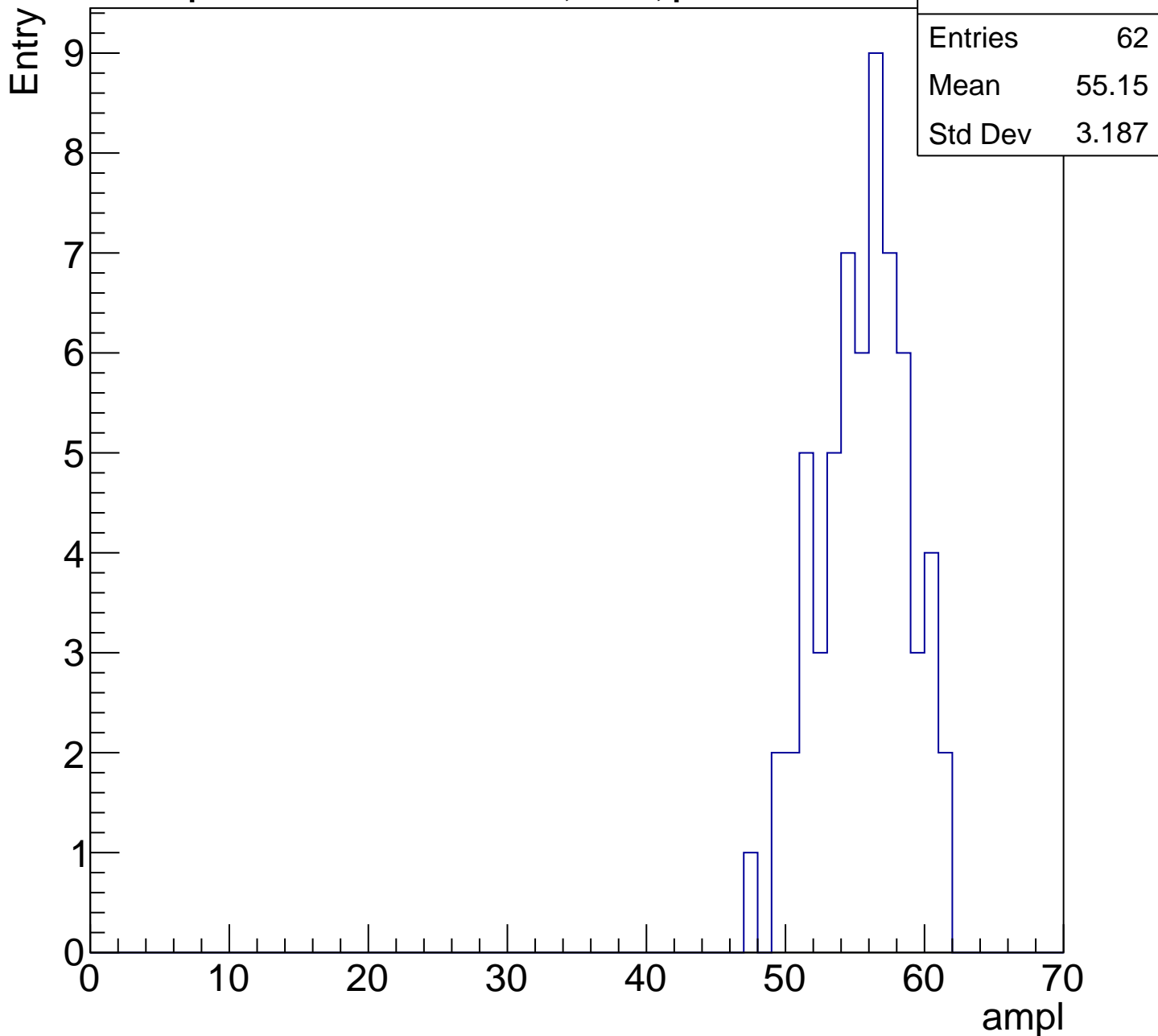
Entry

Entries	70
Mean	48.9
Std Dev	3.381



# B1L101S, U20-ch33, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

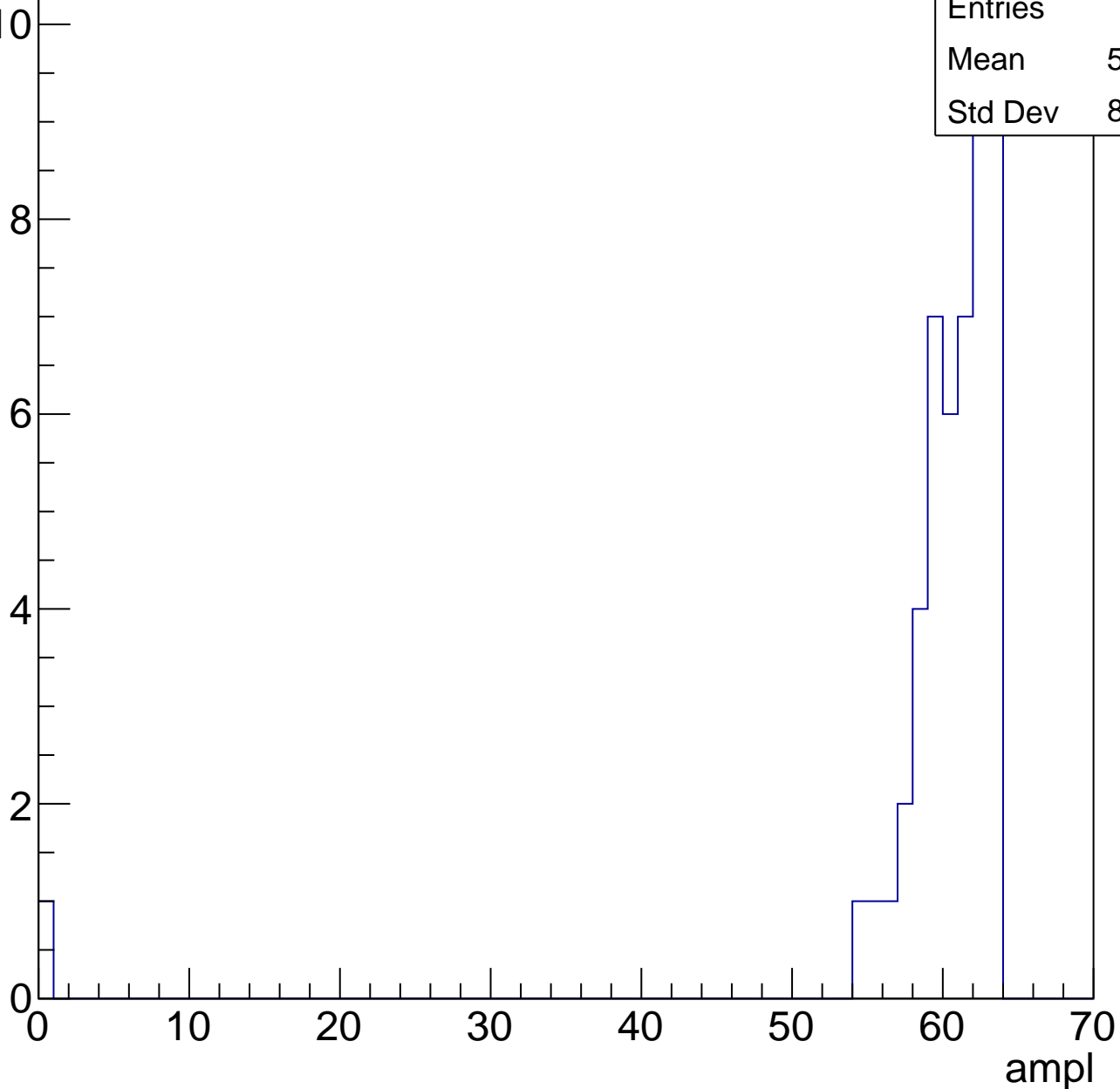


# B1L101S, U20-ch33, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	49
Mean	59.14
Std Dev	8.818



# B1L101S, U20-ch33, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U20-ch33, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U20-ch34, adc0

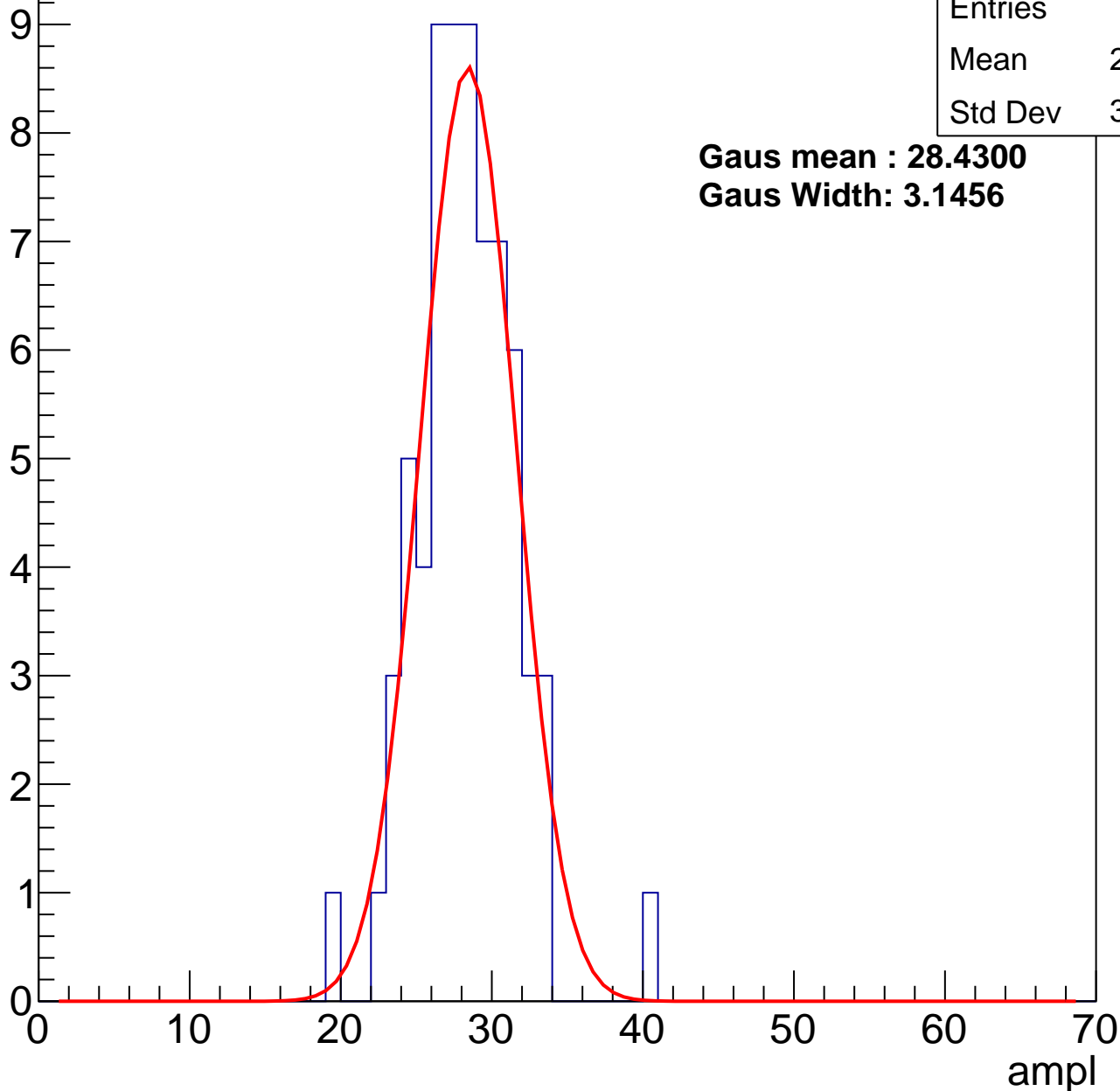
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	27.84
Std Dev	3.225

**Gaus mean : 28.4300**

**Gaus Width: 3.1456**



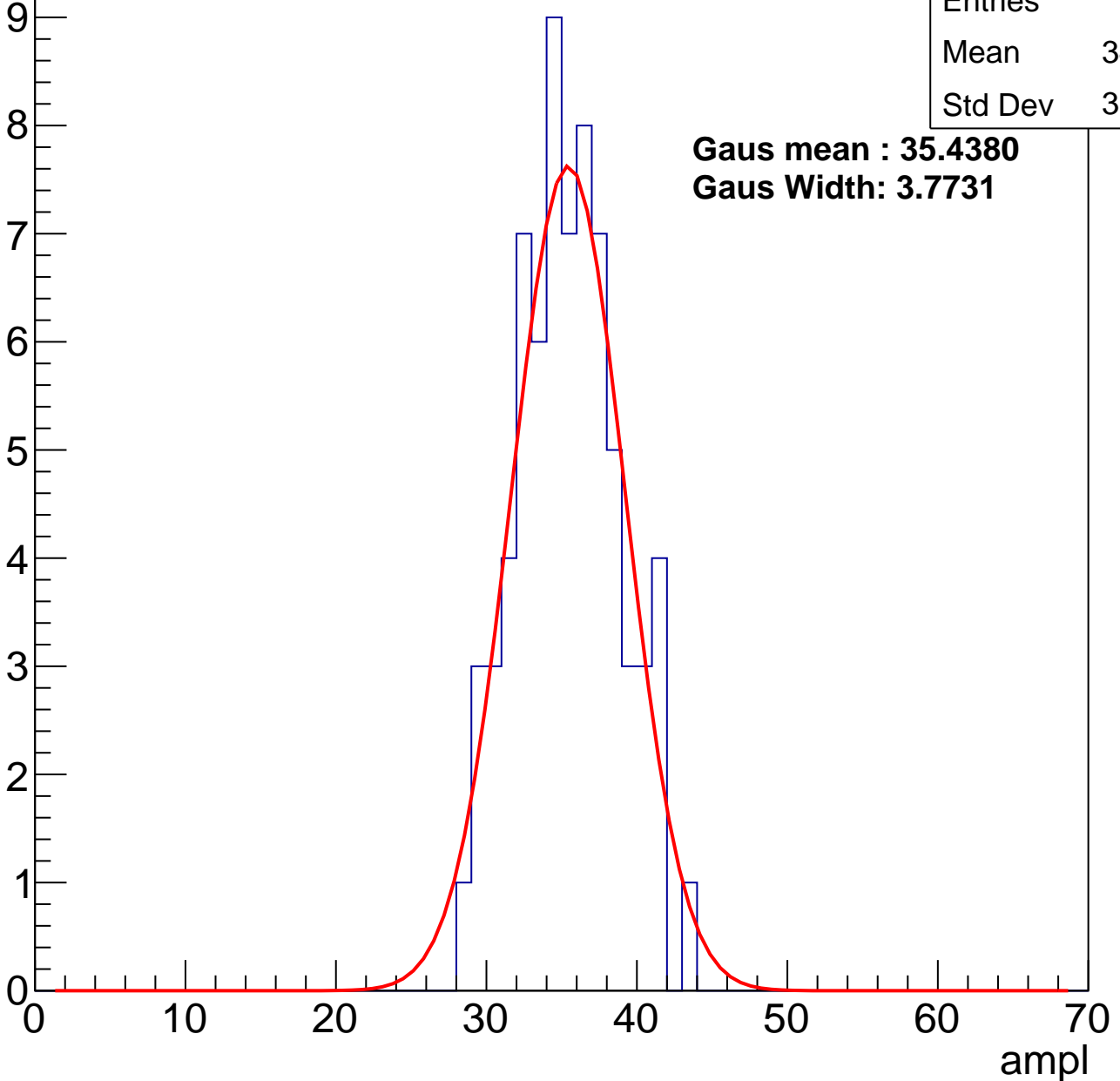
# B1L101S, U20-ch34, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	71
Mean	34.97
Std Dev	3.365

**Gaus mean : 35.4380**  
**Gaus Width: 3.7731**



# B1L101S, U20-ch34, adc2

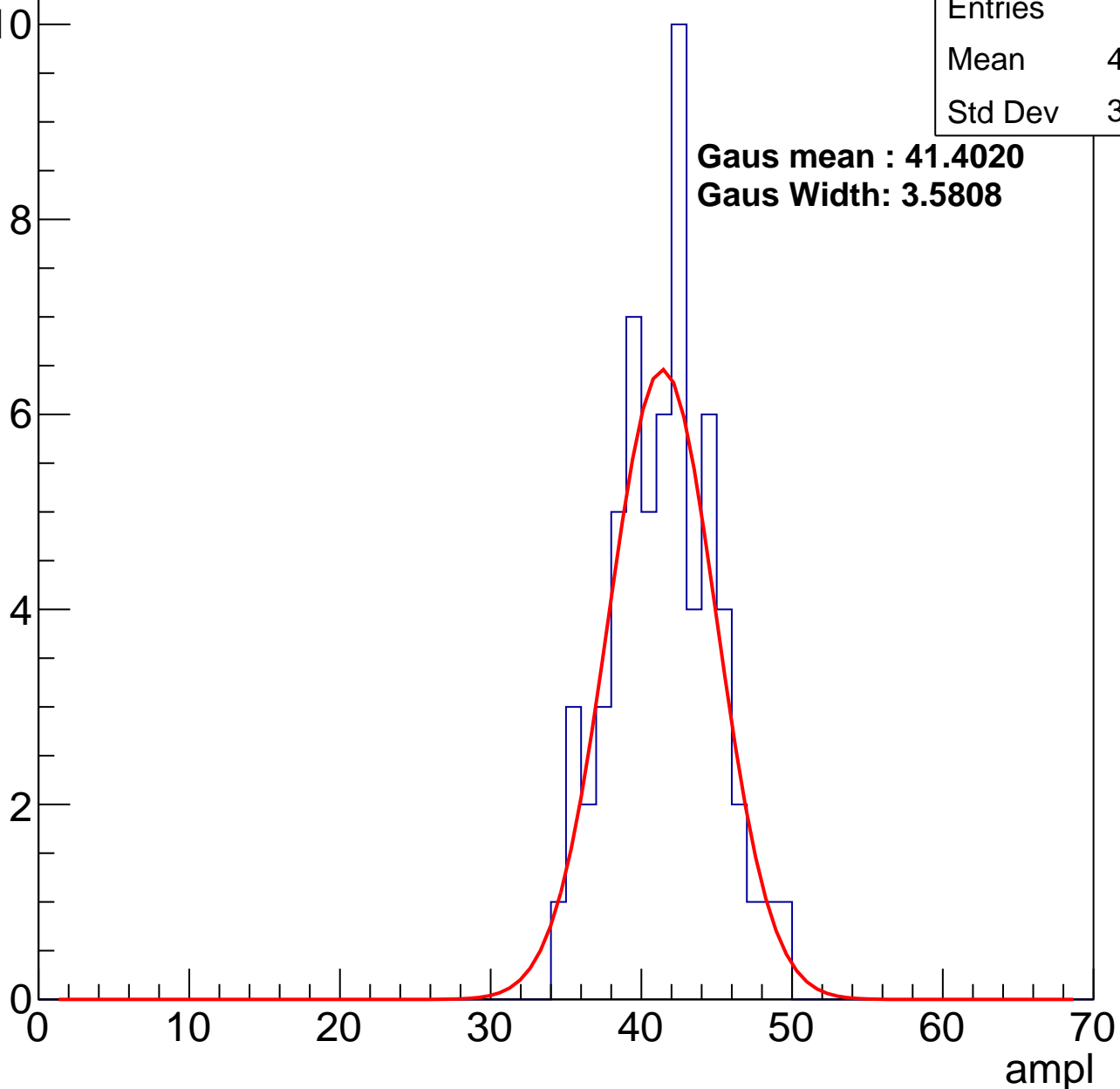
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	41.03
Std Dev	3.329

**Gaus mean : 41.4020**

**Gaus Width: 3.5808**

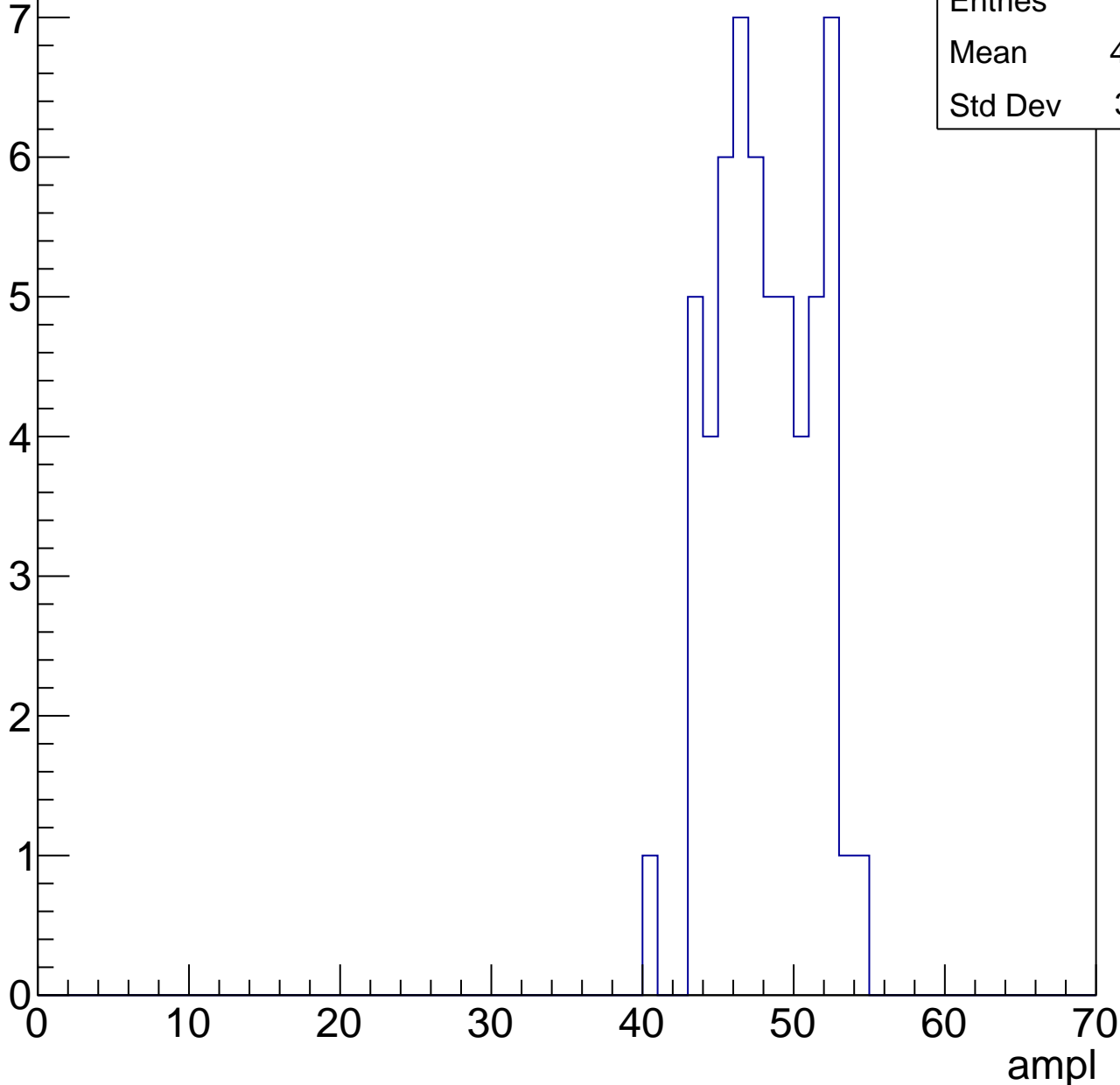


# B1L101S, U20-ch34, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	57
Mean	47.65
Std Dev	3.171

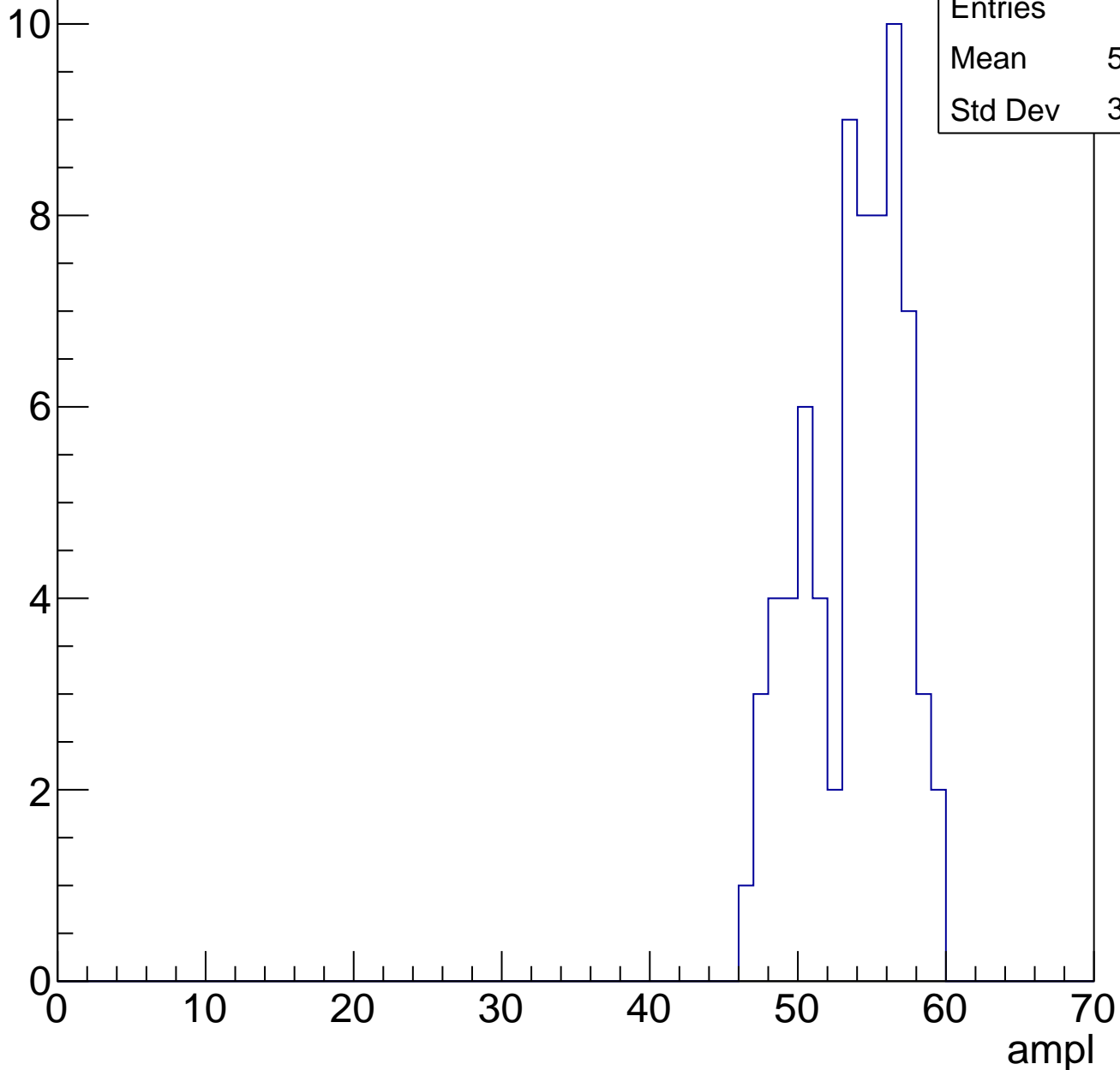


# B1L101S, U20-ch34, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	71
Mean	53.28
Std Dev	3.307

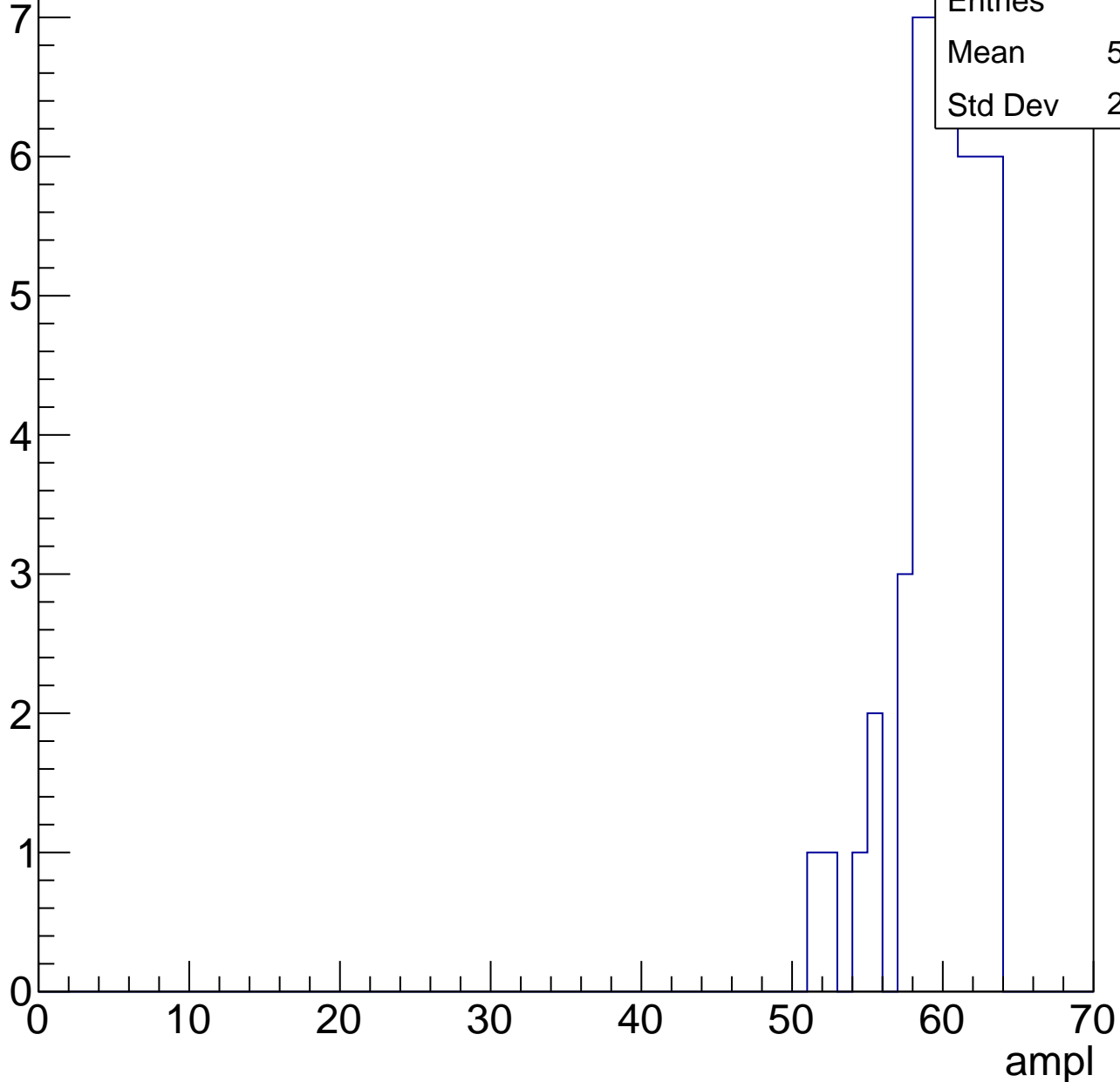
Entry



# B1L101S, U20-ch34, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

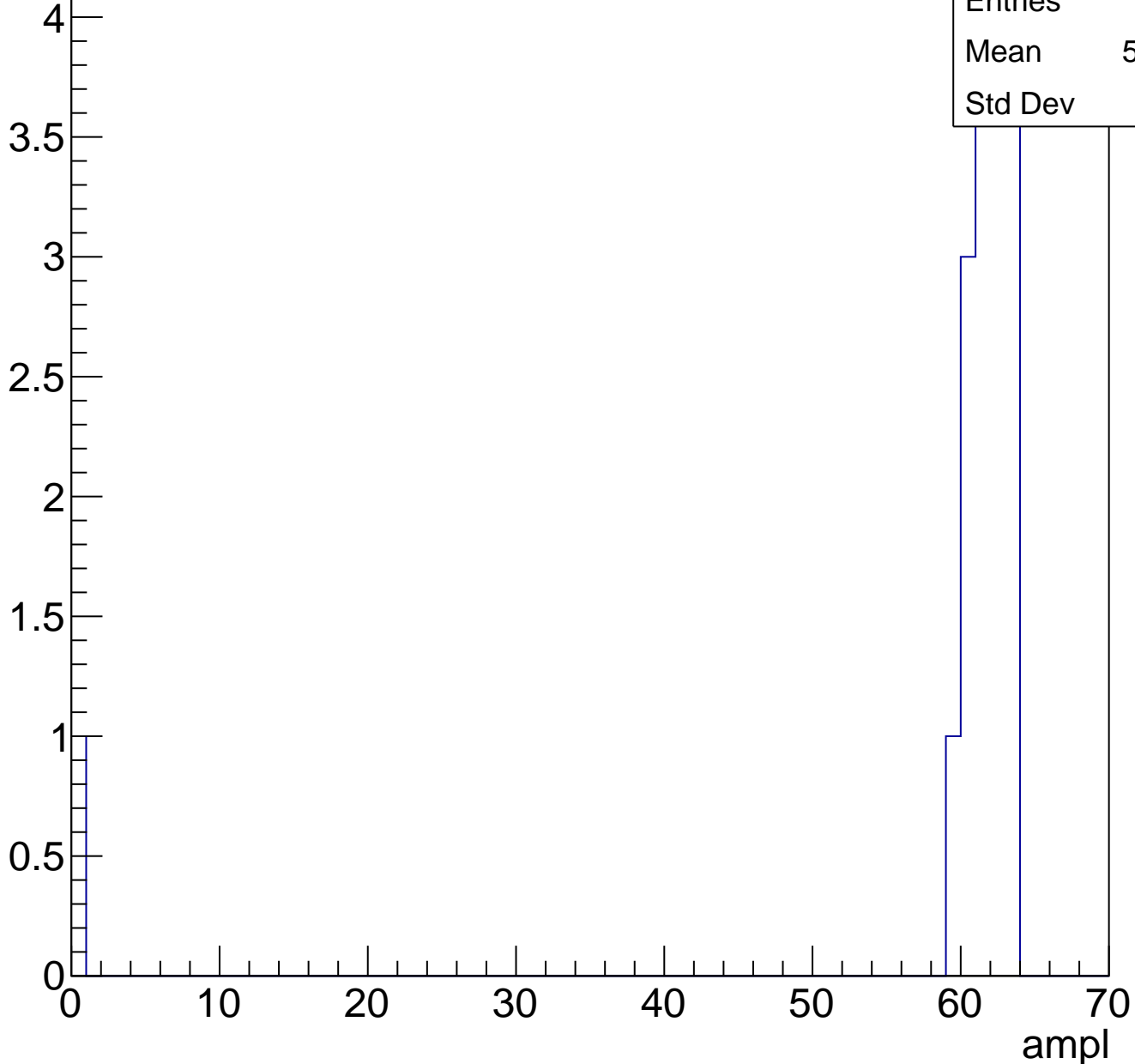


Entries	47
Mean	59.43
Std Dev	2.773

# B1L101S, U20-ch34, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	17
Mean	57.82
Std Dev	14.5



# B1L101S, U20-ch34, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	2
Mean	8.5
Std Dev	8.5

# B1L101S, U20-ch35, adc0

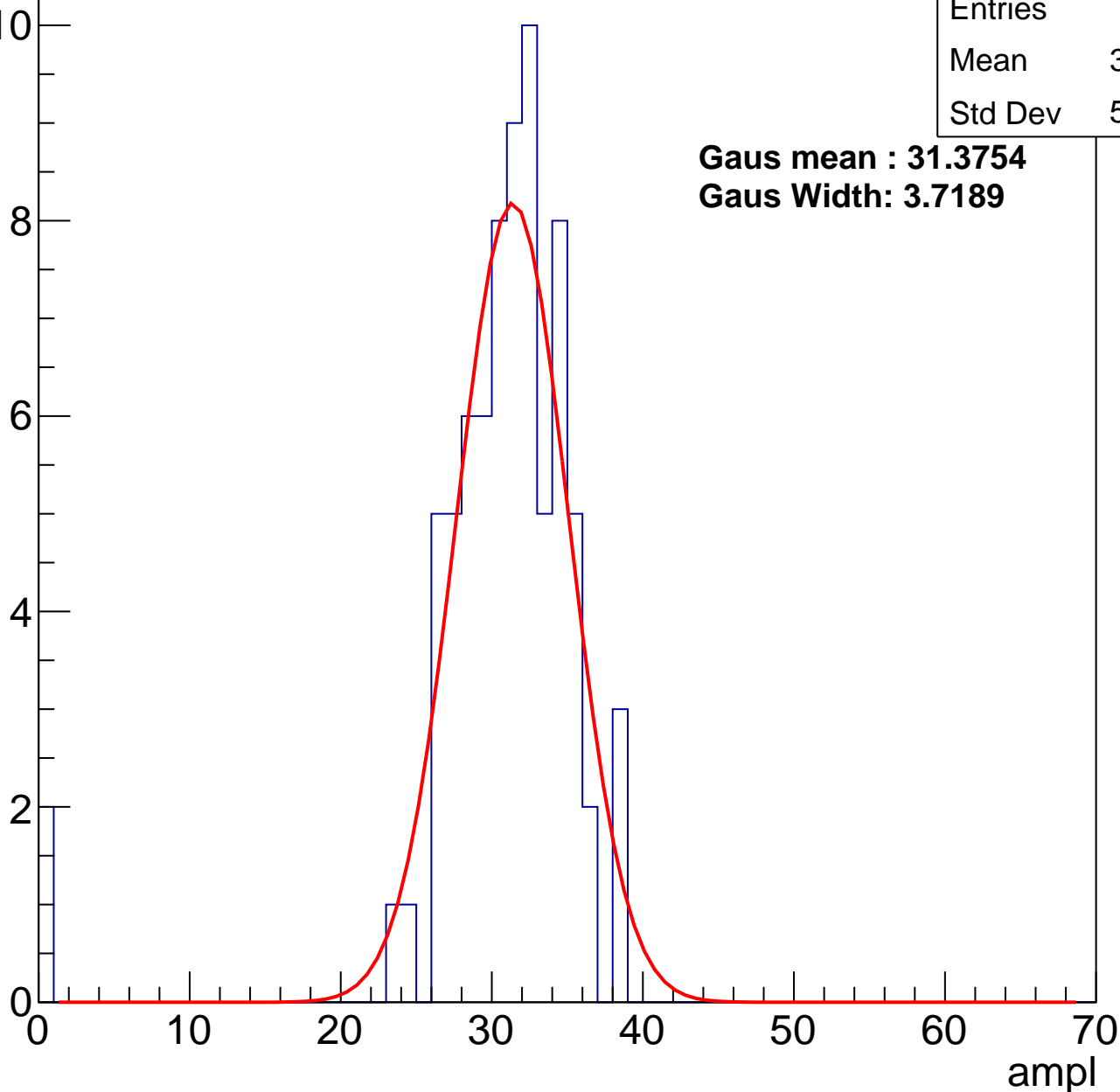
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	76
Mean	30.14
Std Dev	5.904

**Gaus mean : 31.3754**

**Gaus Width: 3.7189**



# B1L101S, U20-ch35, adc1

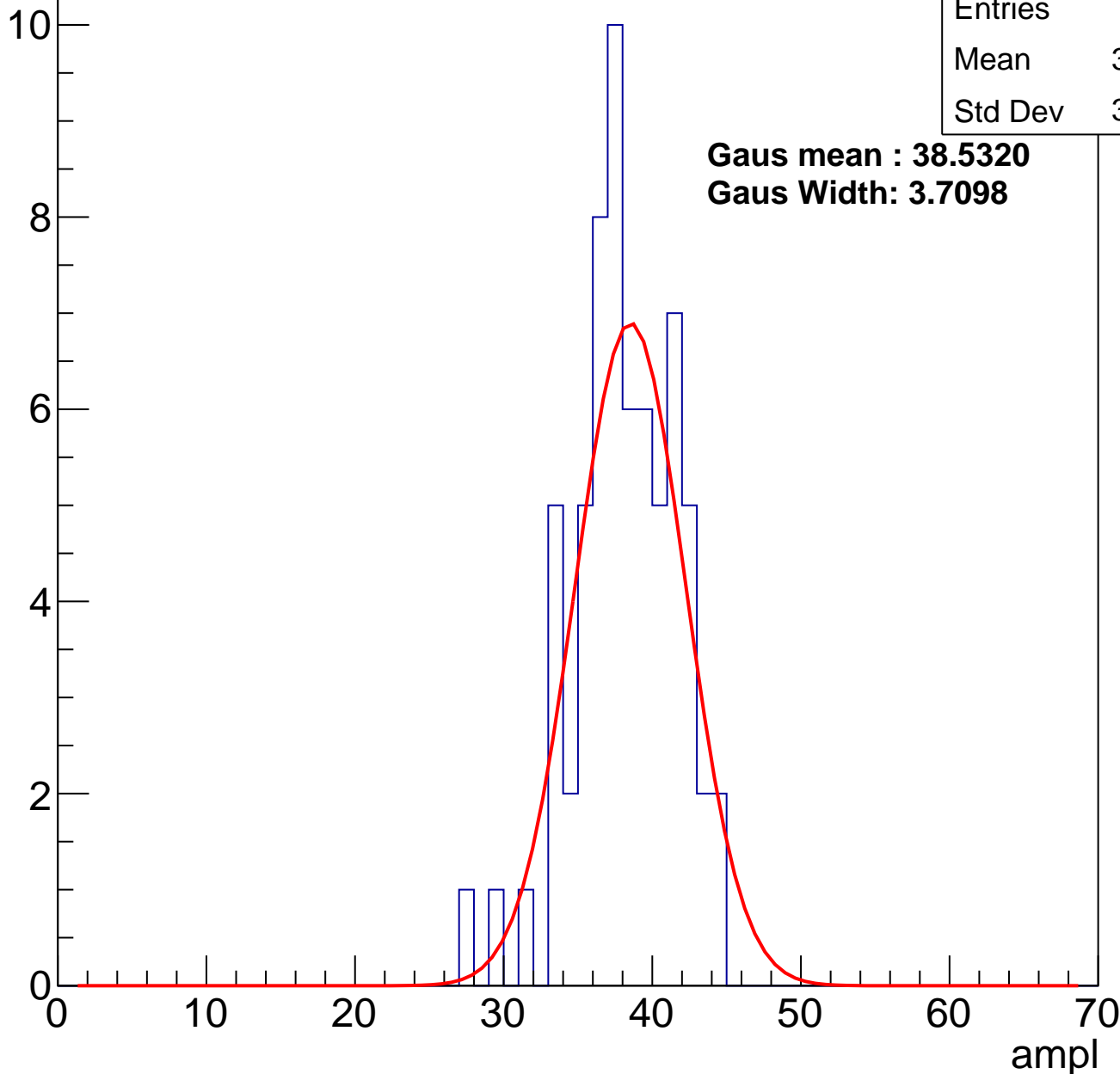
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	66
Mean	37.67
Std Dev	3.435

**Gaus mean : 38.5320**

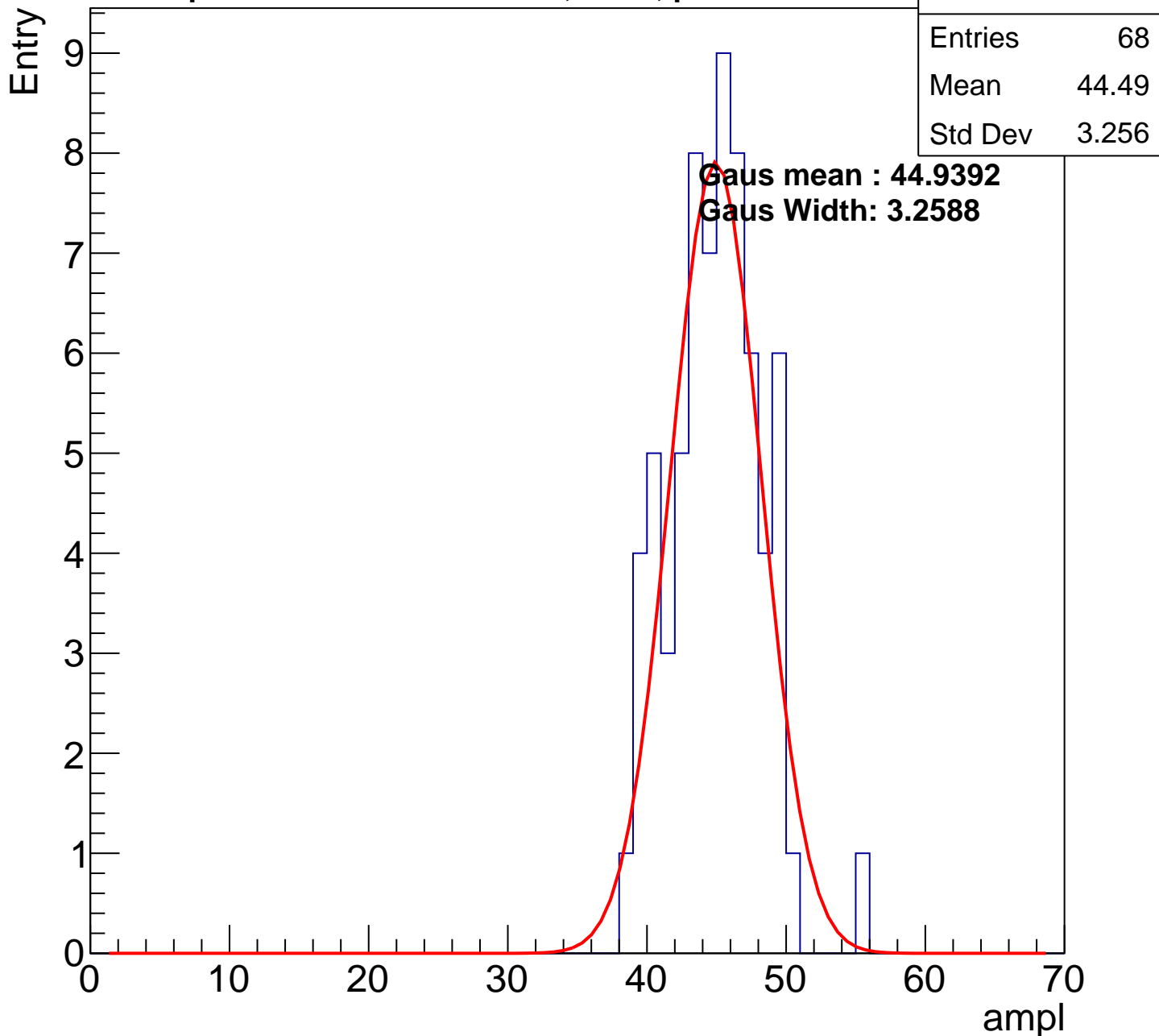
**Gaus Width: 3.7098**

Entry



# B1L101S, U20-ch35, adc2

calib\_packv5\_042523\_0143.root, FC#0, port D2

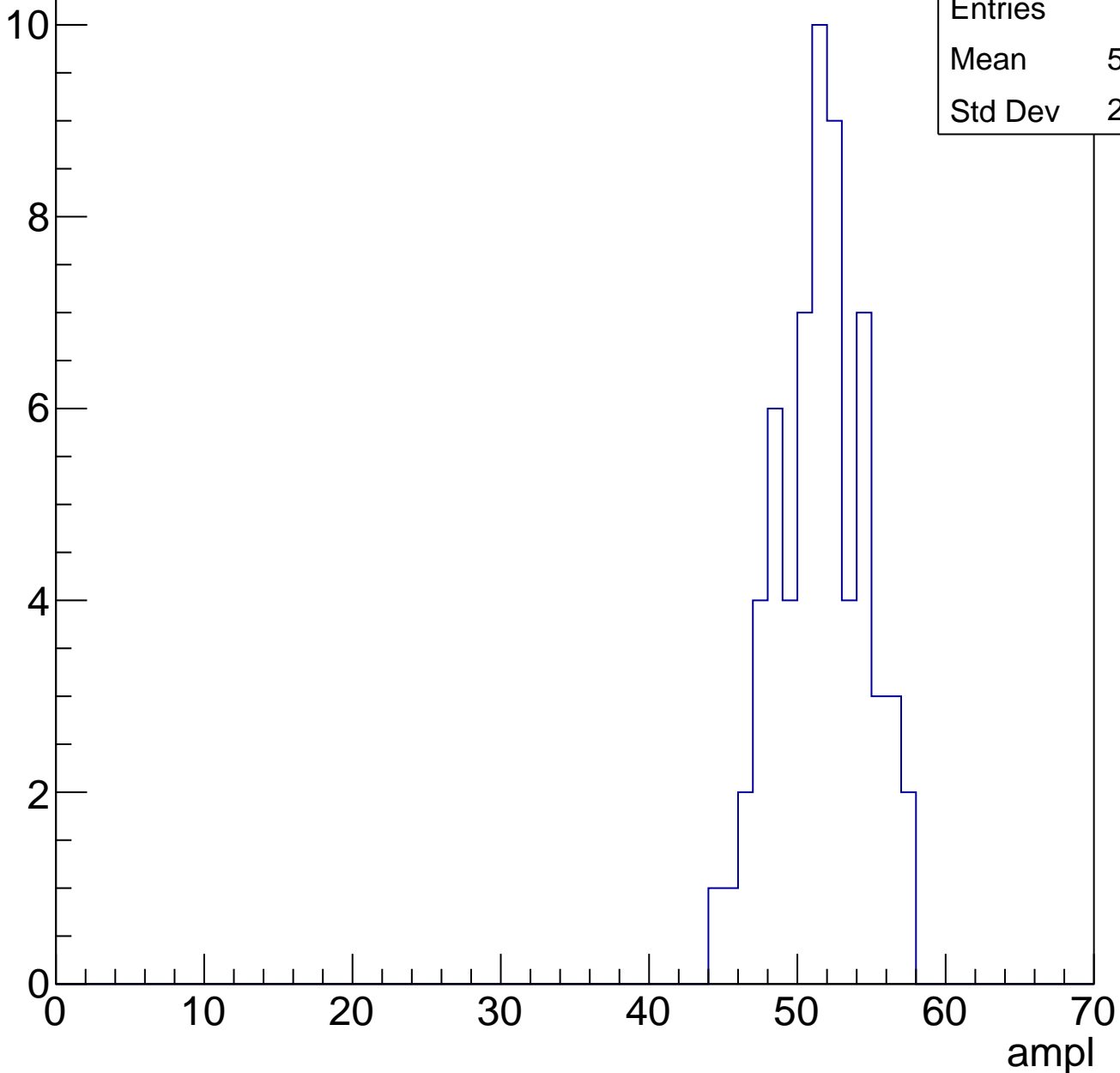


# B1L101S, U20-ch35, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	51.08
Std Dev	2.978

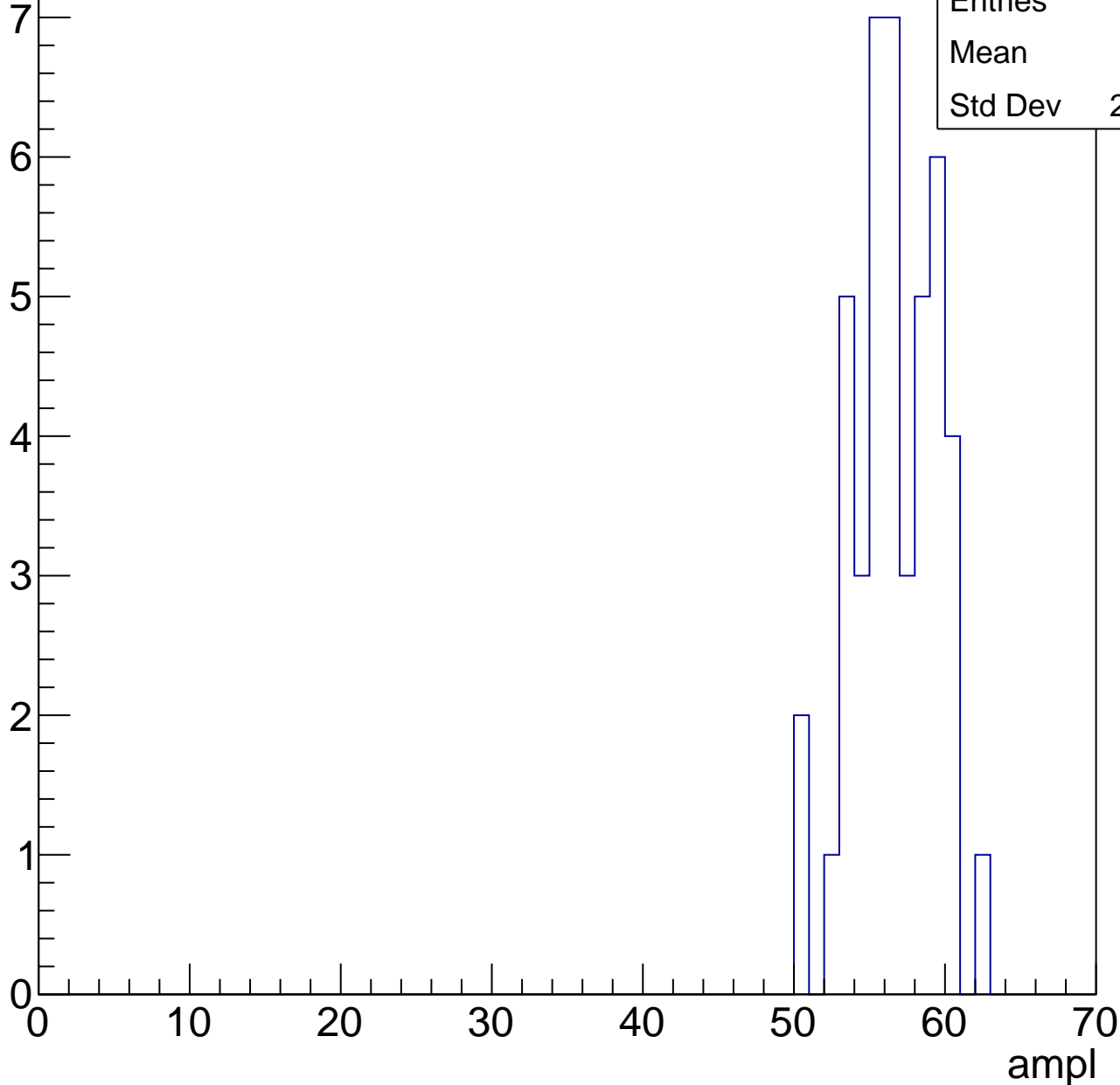


# B1L101S, U20-ch35, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	44
Mean	56.2
Std Dev	2.727

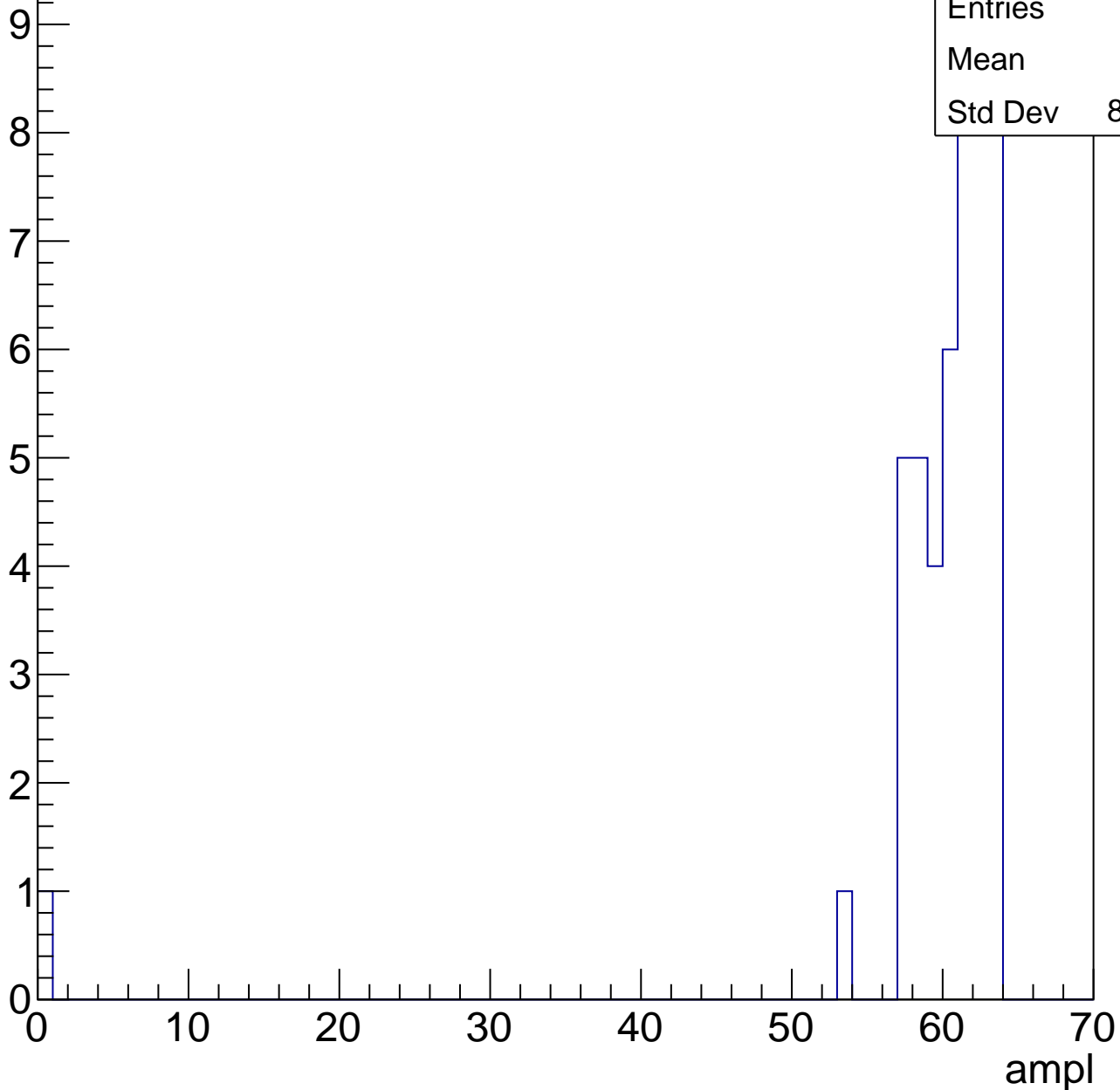


# B1L101S, U20-ch35, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	47
Mean	59
Std Dev	8.973



# B1L101S, U20-ch35, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U20-ch35, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U20-ch36, adc0

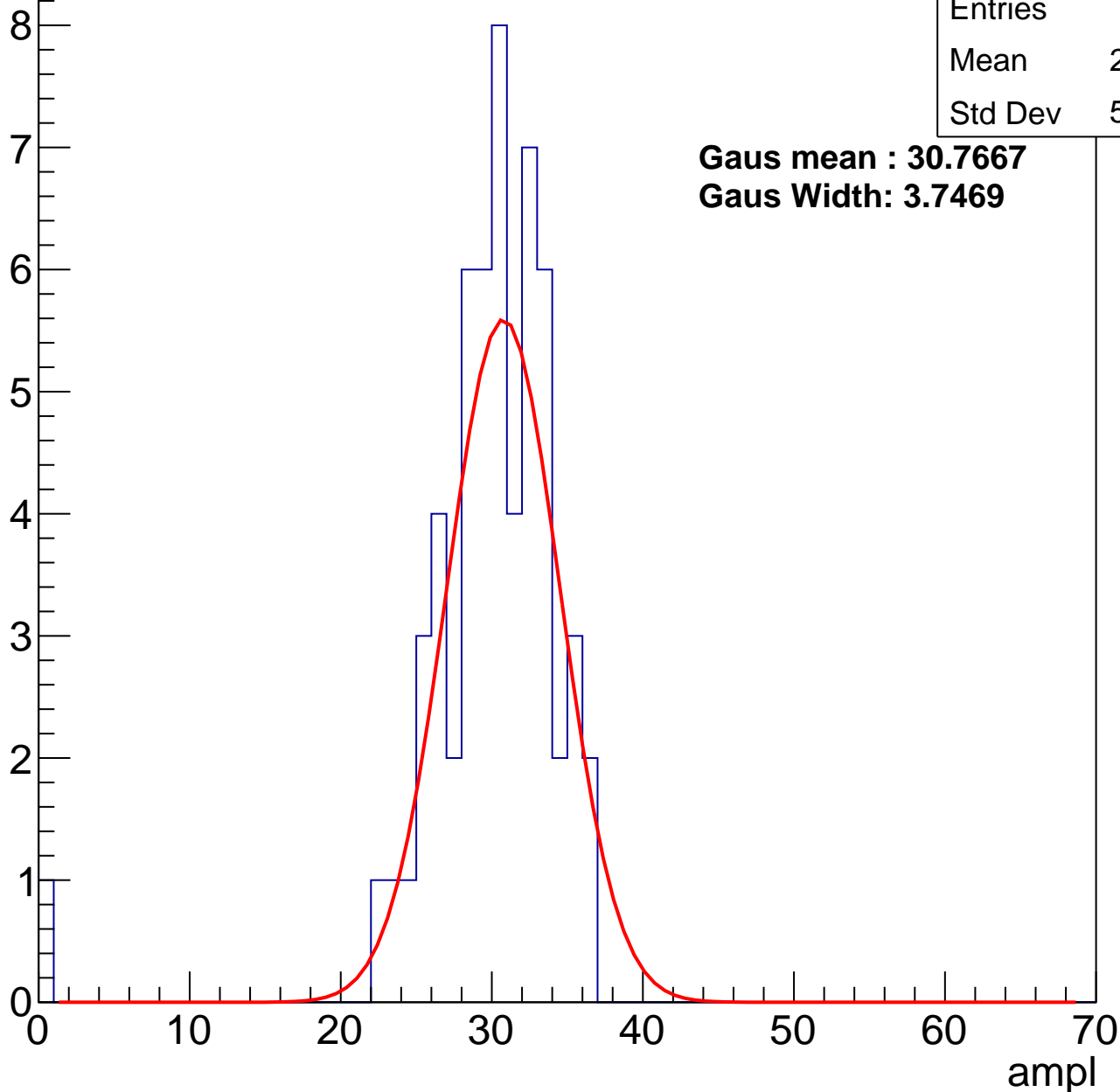
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	57
Mean	29.39
Std Dev	5.095

**Gaus mean : 30.7667**

**Gaus Width: 3.7469**



# B1L101S, U20-ch36, adc1

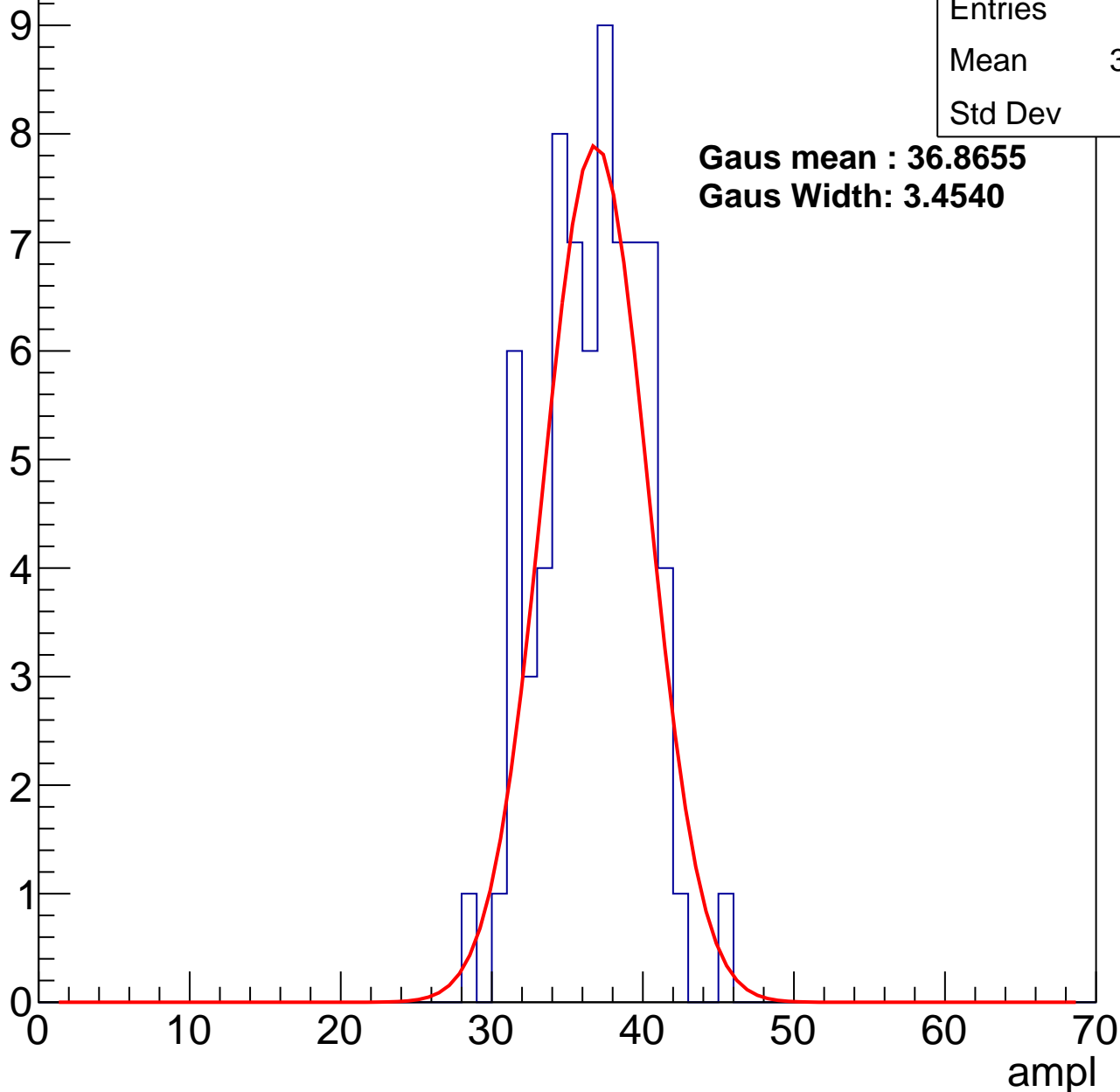
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	72
Mean	36.22
Std Dev	3.33

**Gaus mean : 36.8655**

**Gaus Width: 3.4540**



# B1L101S, U20-ch36, adc2

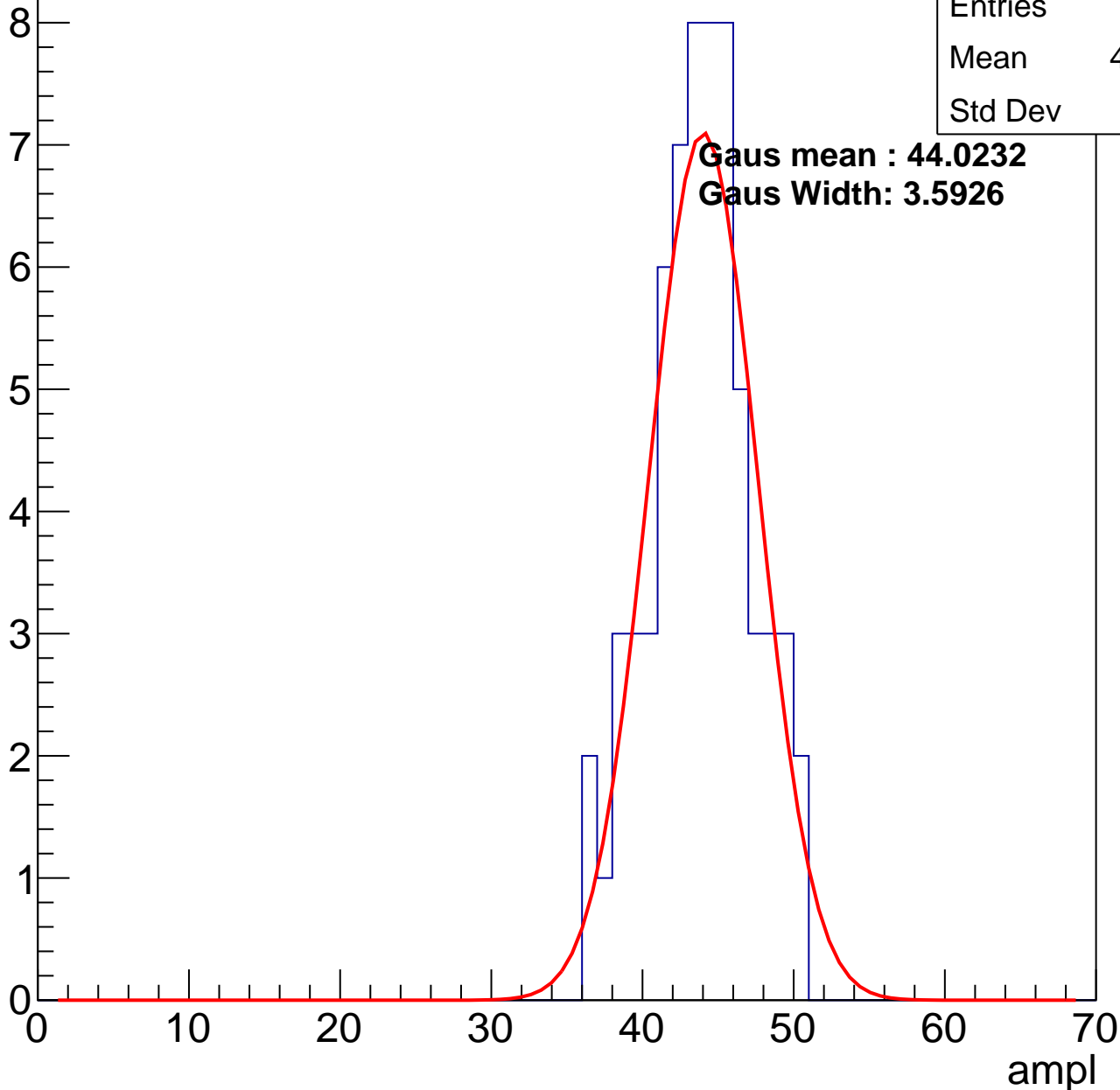
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	43.35
Std Dev	3.33

**Gaus mean : 44.0232**

**Gaus Width: 3.5926**

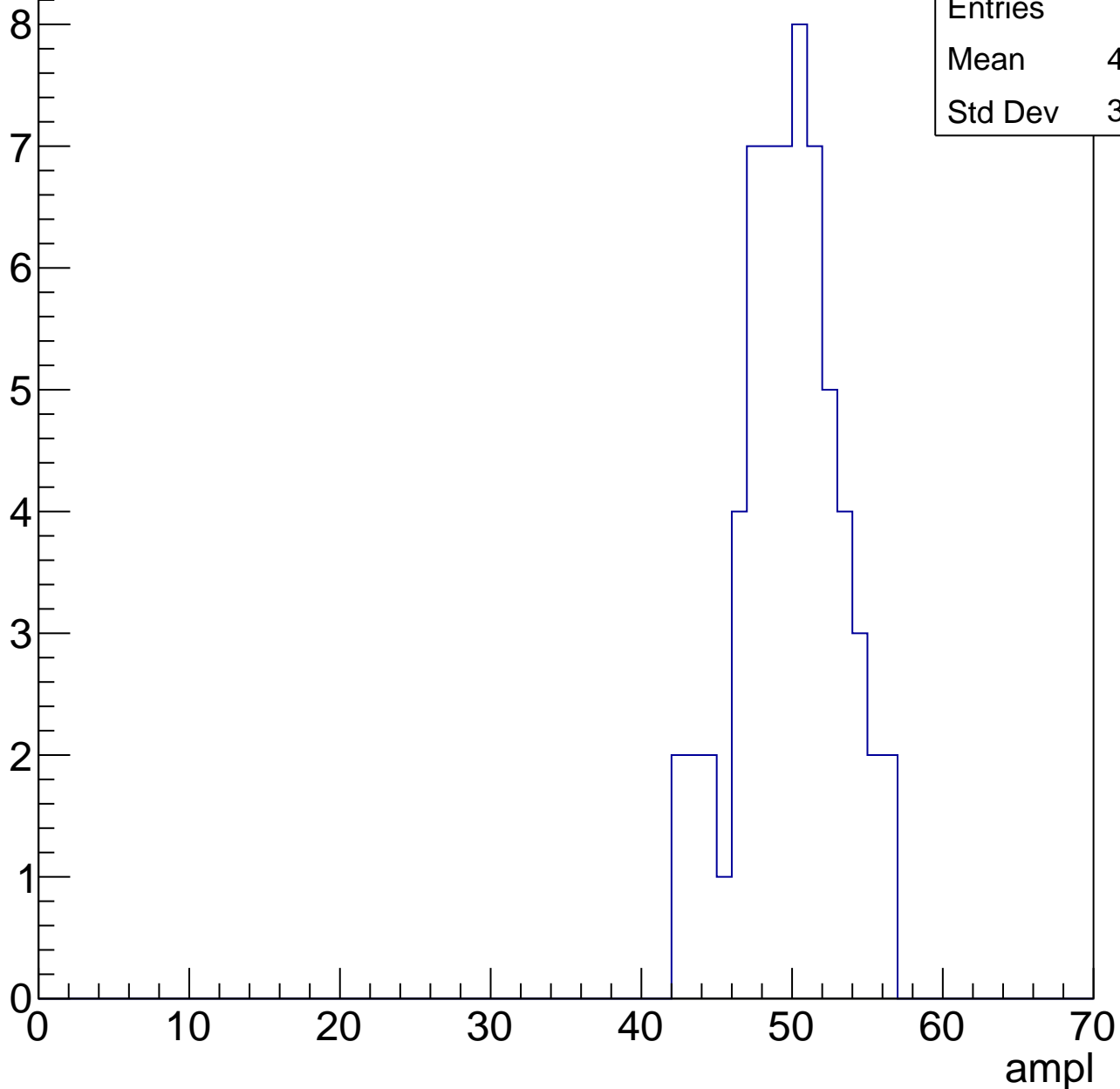


# B1L101S, U20-ch36, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	49.33
Std Dev	3.309

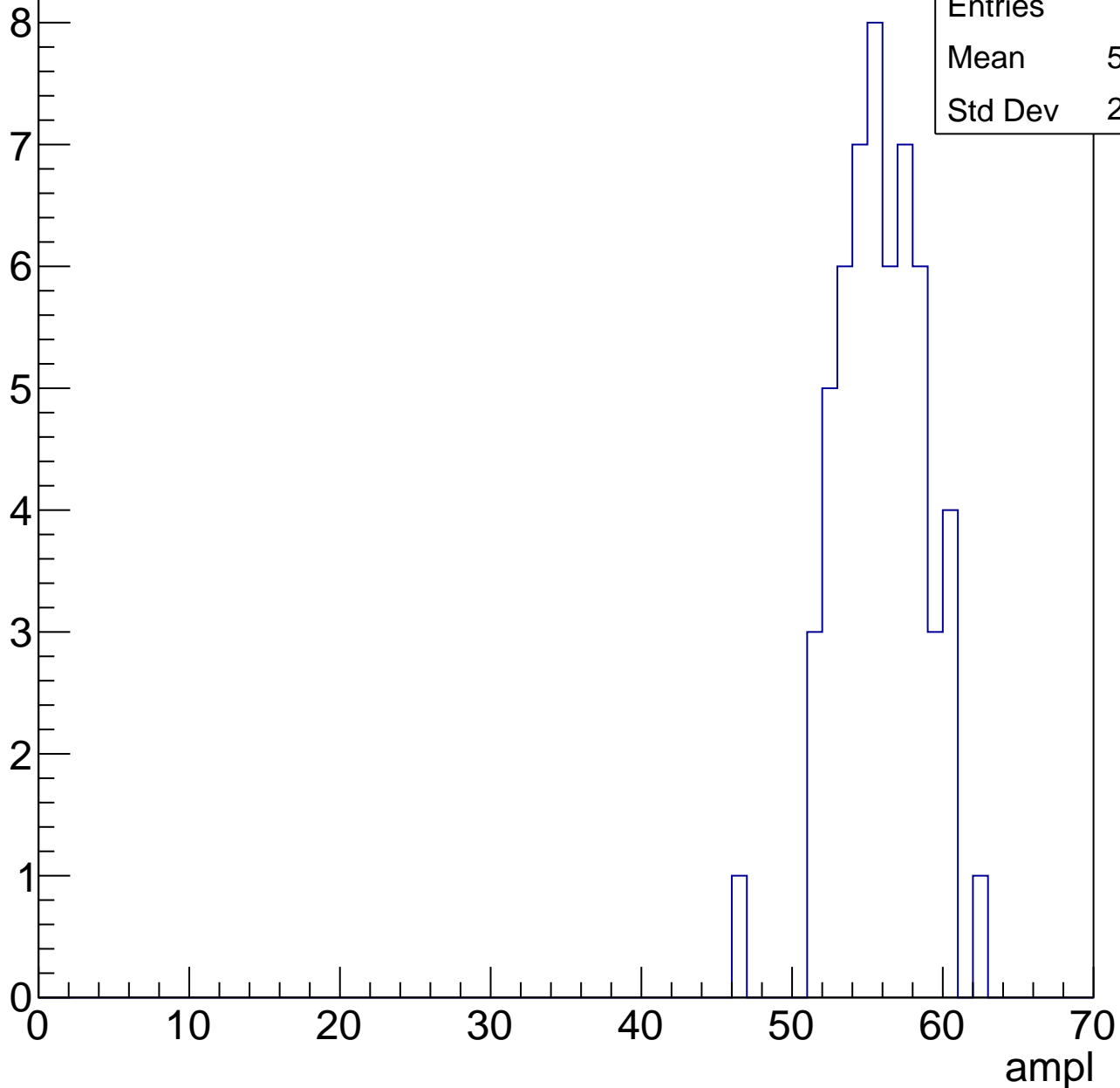


# B1L101S, U20-ch36, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	57
Mean	55.39
Std Dev	2.906

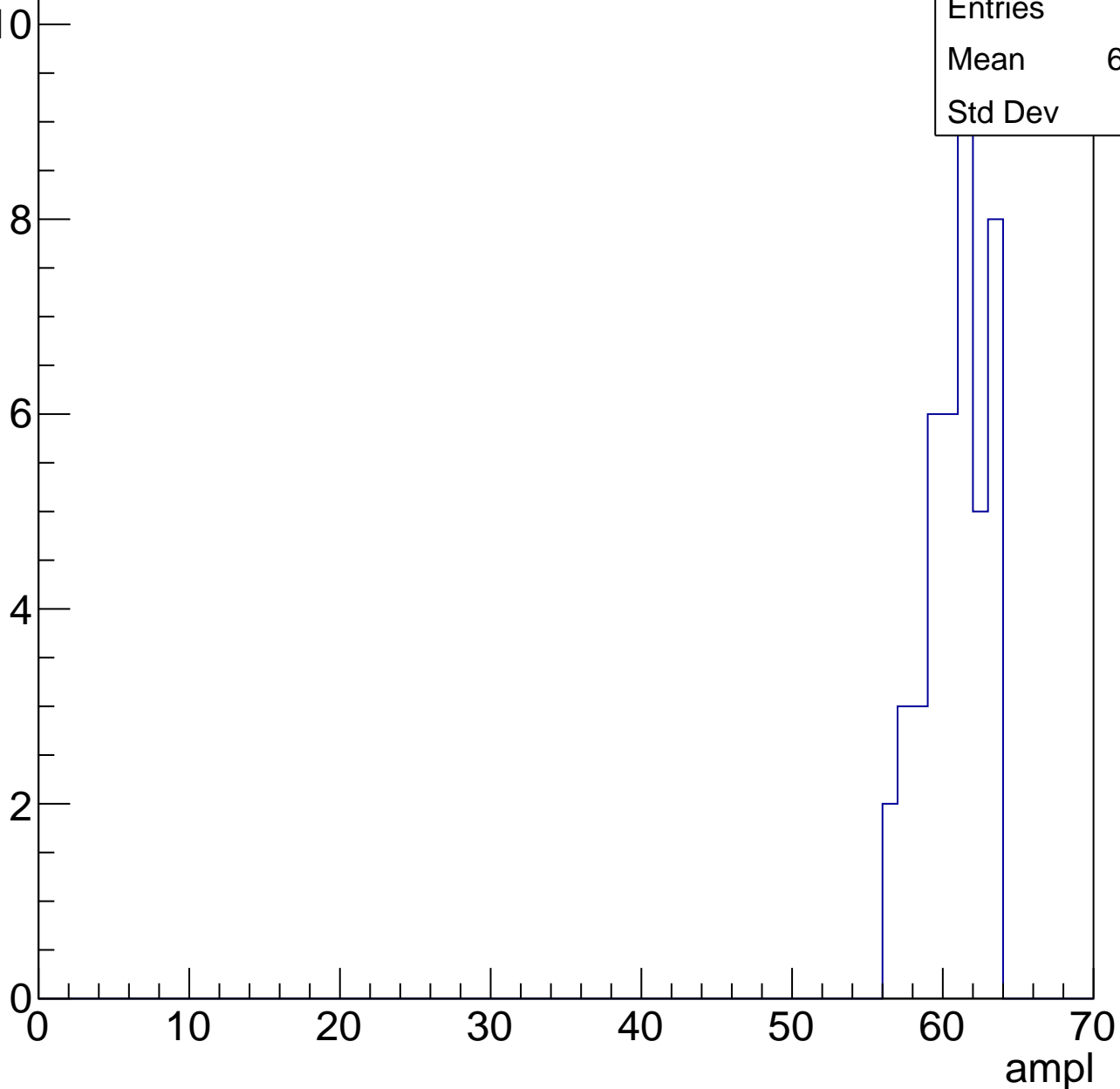


# B1L101S, U20-ch36, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

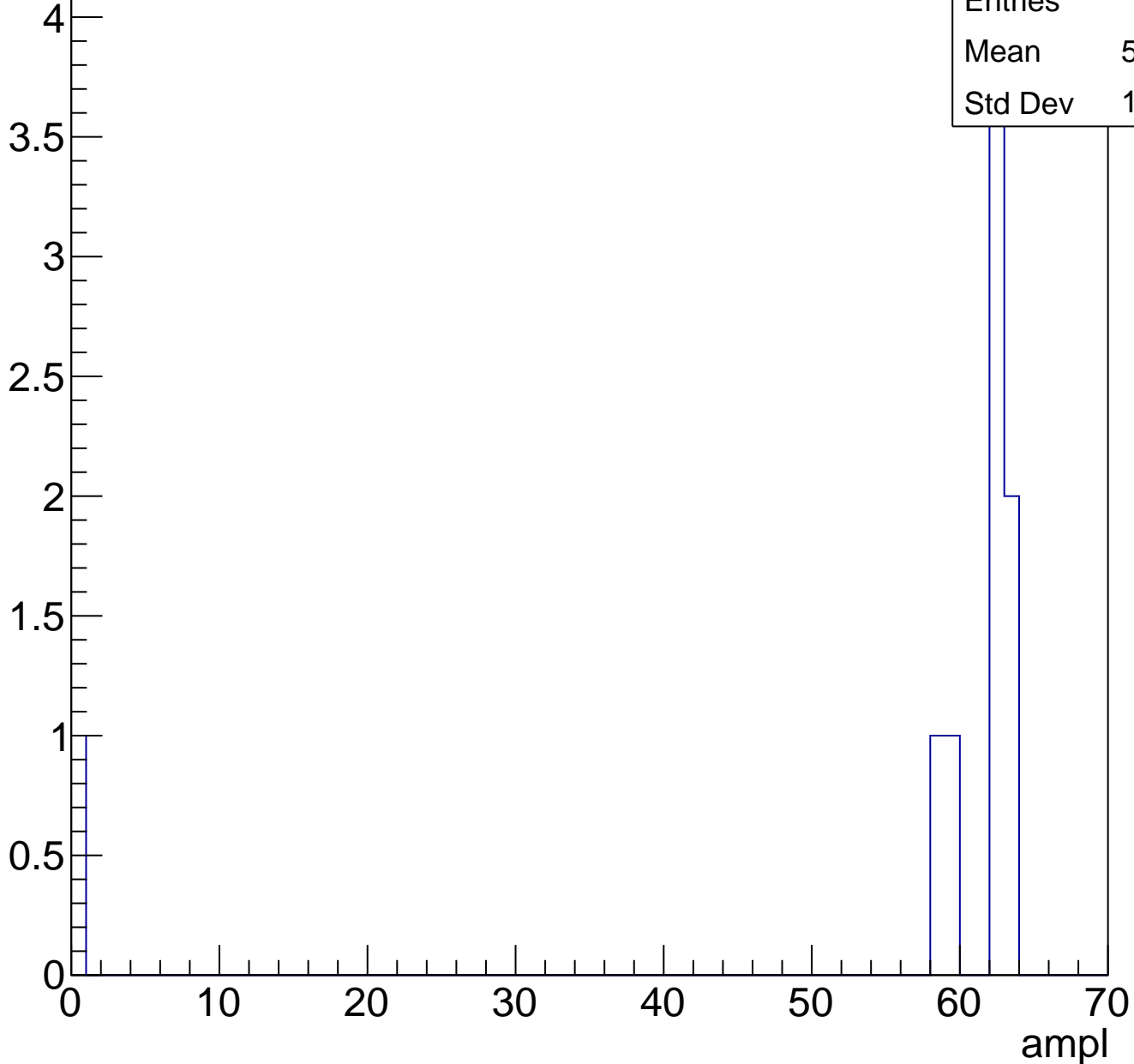
Entries	43
Mean	60.35
Std Dev	2.01



# B1L101S, U20-ch36, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U20-ch36, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L101S, U20-ch37, adc0

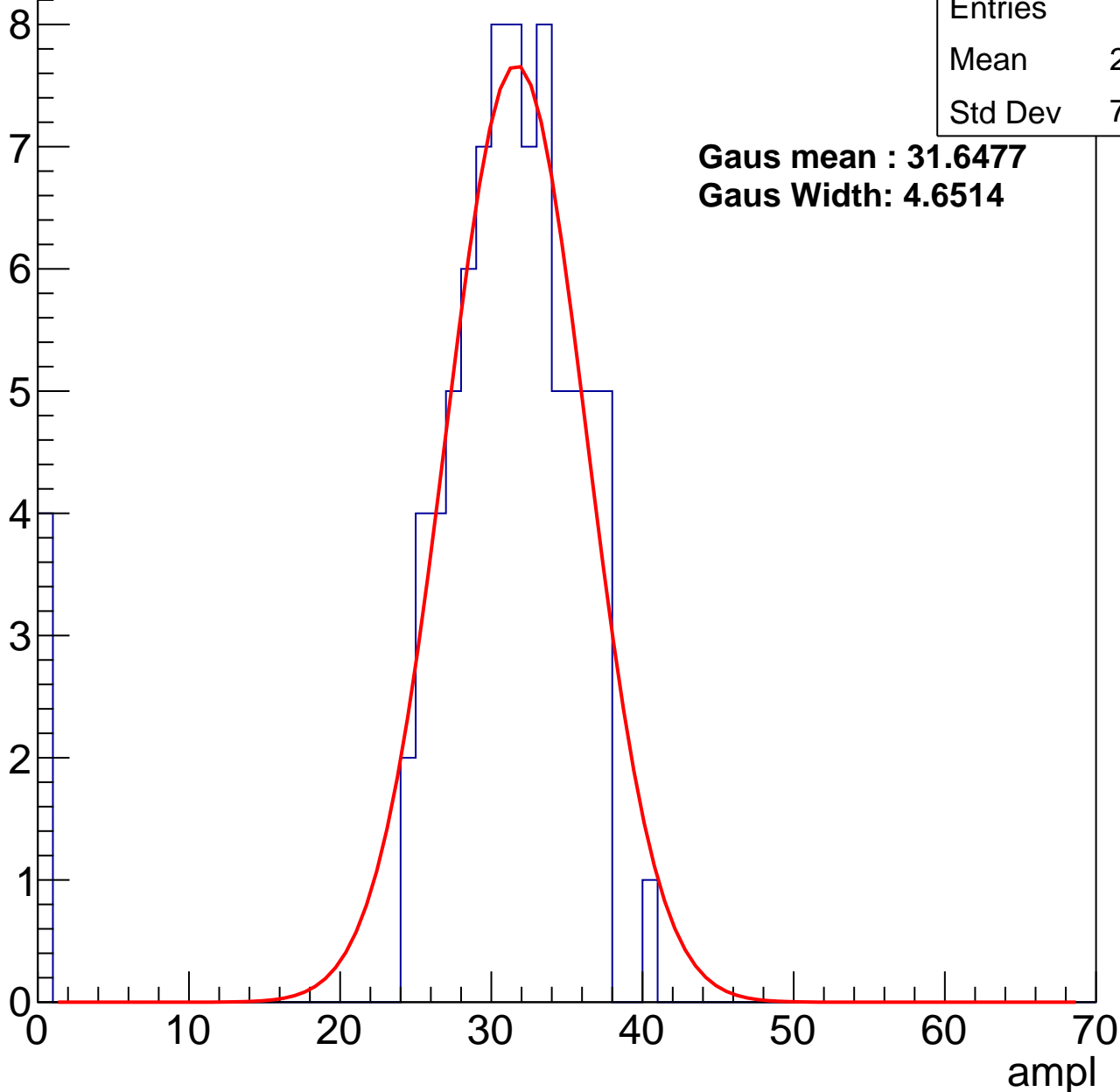
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	84
Mean	29.57
Std Dev	7.508

**Gaus mean : 31.6477**

**Gaus Width: 4.6514**

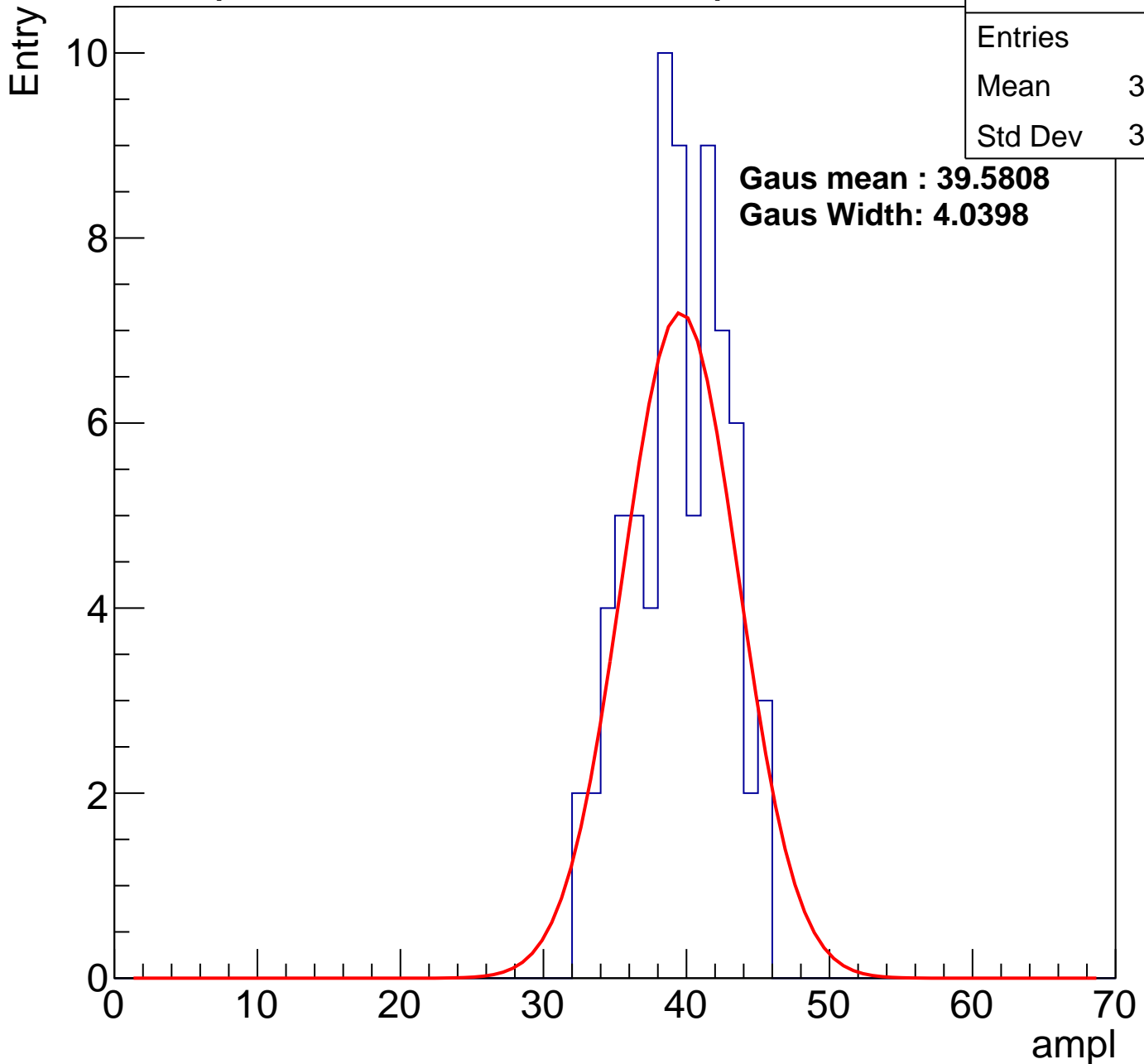


# B1L101S, U20-ch37, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

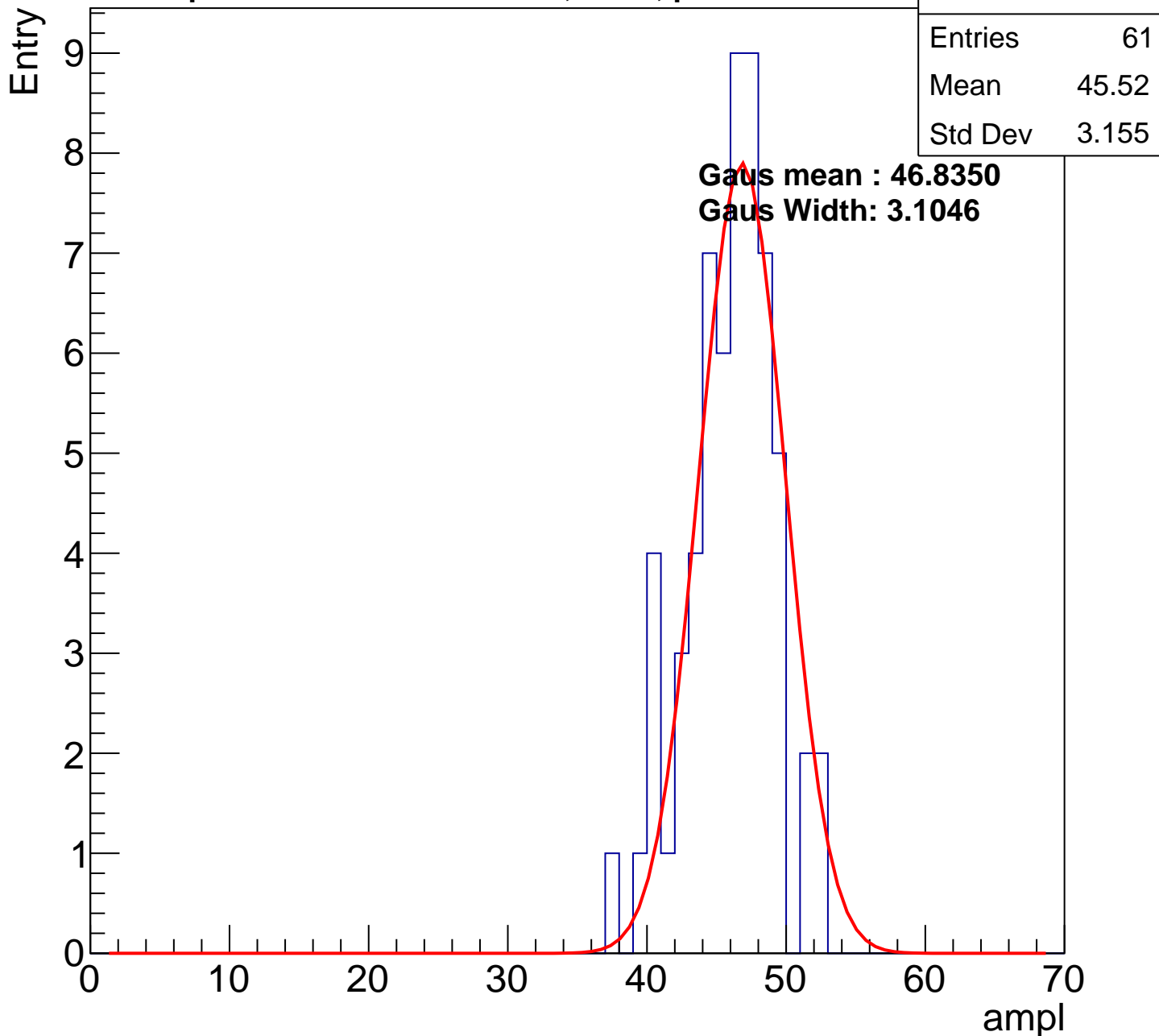
Entries	73
Mean	38.96
Std Dev	3.266

**Gaus mean : 39.5808**  
**Gaus Width: 4.0398**



# B1L101S, U20-ch37, adc2

calib\_packv5\_042523\_0143.root, FC#0, port D2

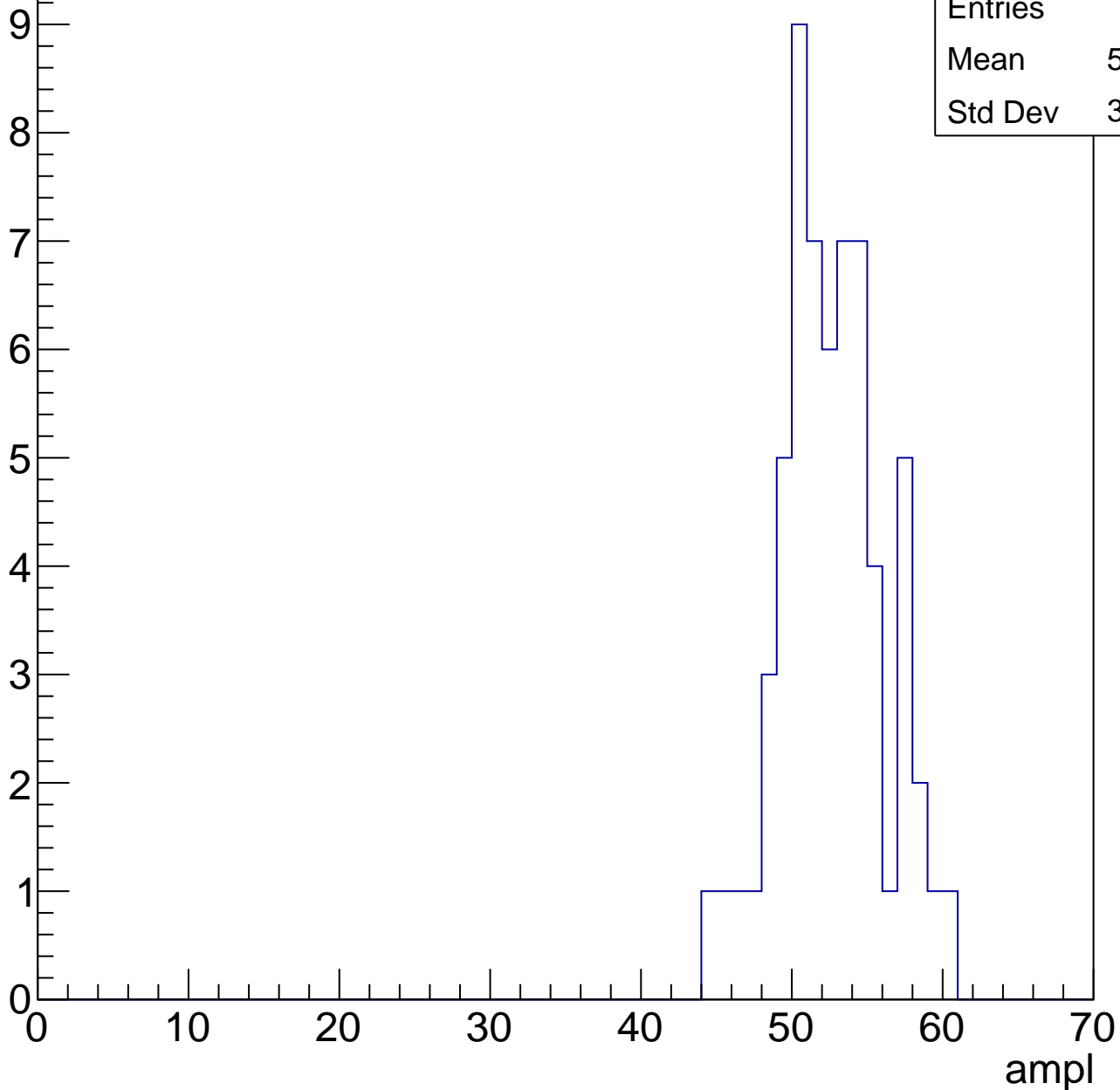


# B1L101S, U20-ch37, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	52.18
Std Dev	3.372

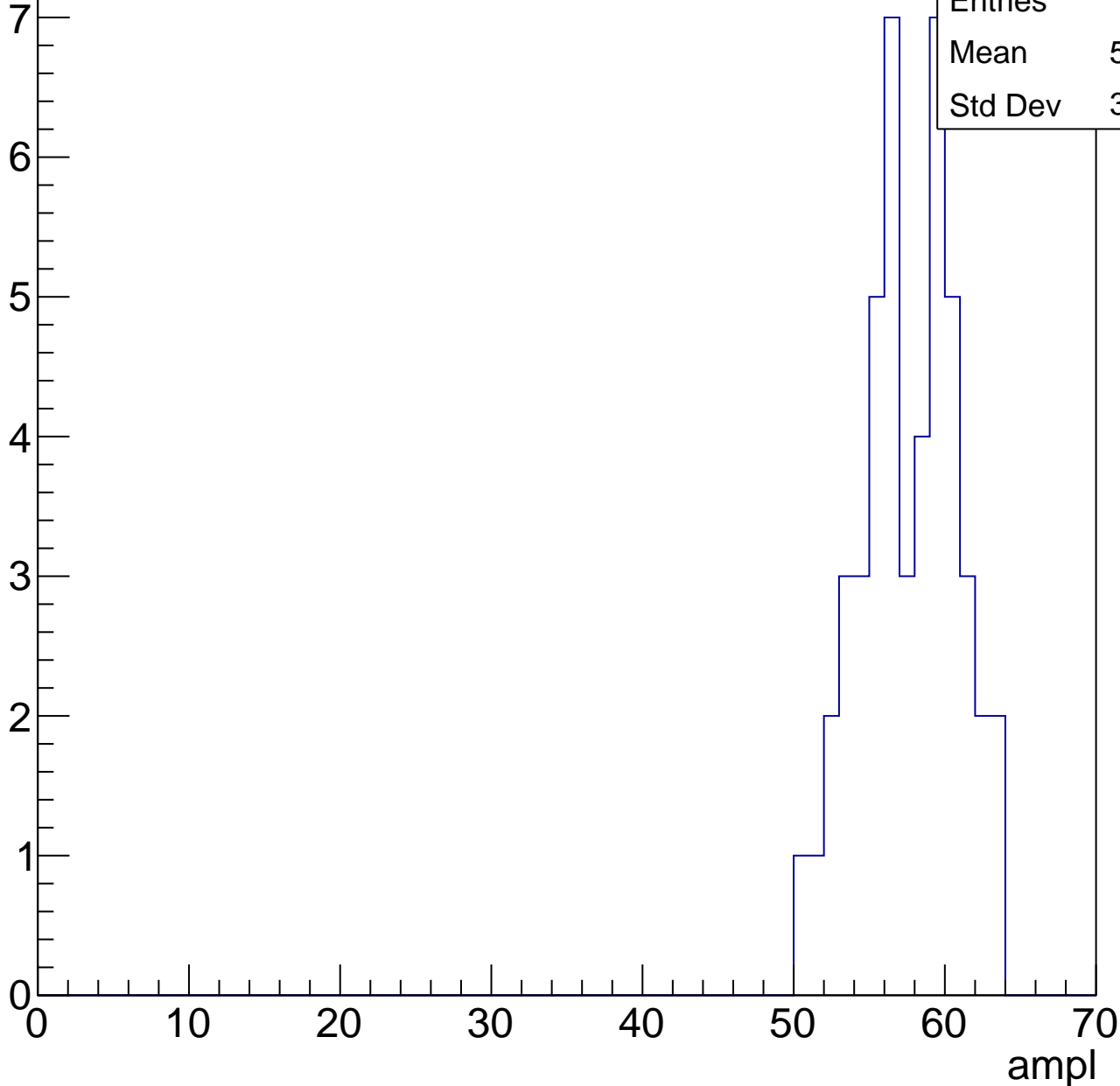


# B1L101S, U20-ch37, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	48
Mean	57.12
Std Dev	3.173

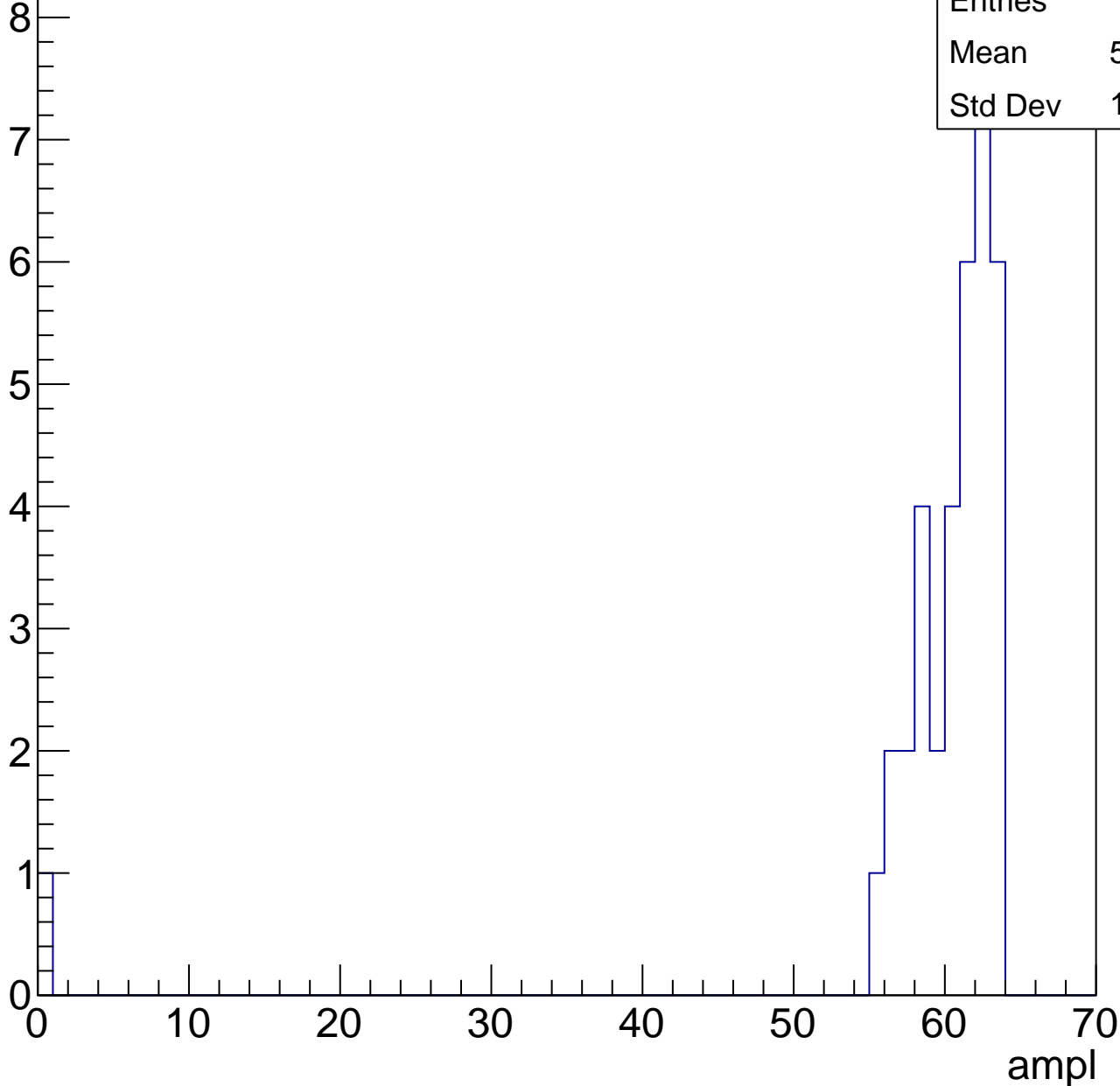


# B1L101S, U20-ch37, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	36
Mean	58.64
Std Dev	10.16



# B1L101S, U20-ch37, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	3
Mean	62.33
Std Dev	0.9428

0 10 20 30 40 50 60 70

ampl





# B1L101S, U20-ch37, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U20-ch38, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	79
Mean	28.66
Std Dev	4.799

**Gaus mean : 29.8400**

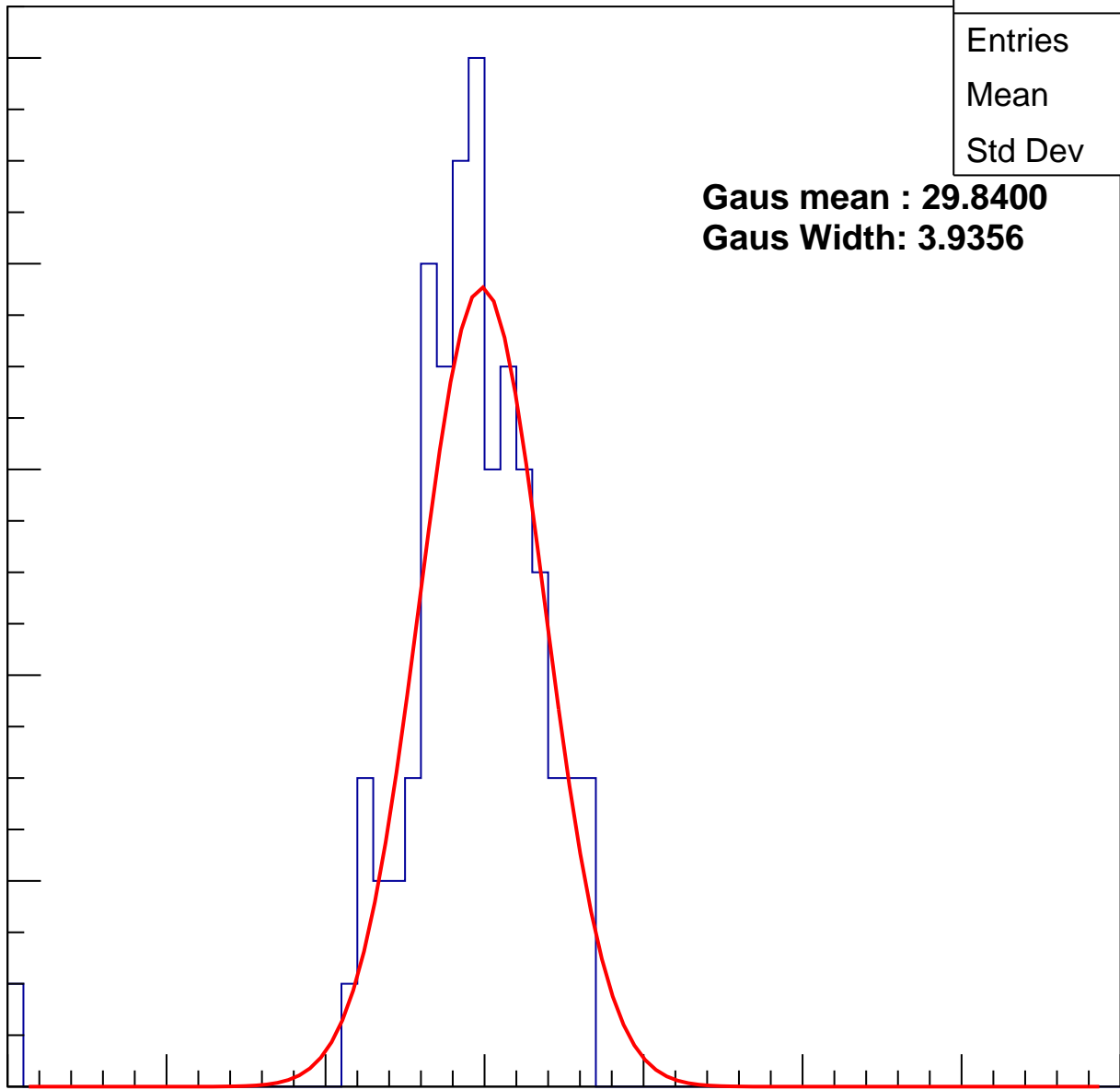
**Gaus Width: 3.9356**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U20-ch38, adc1

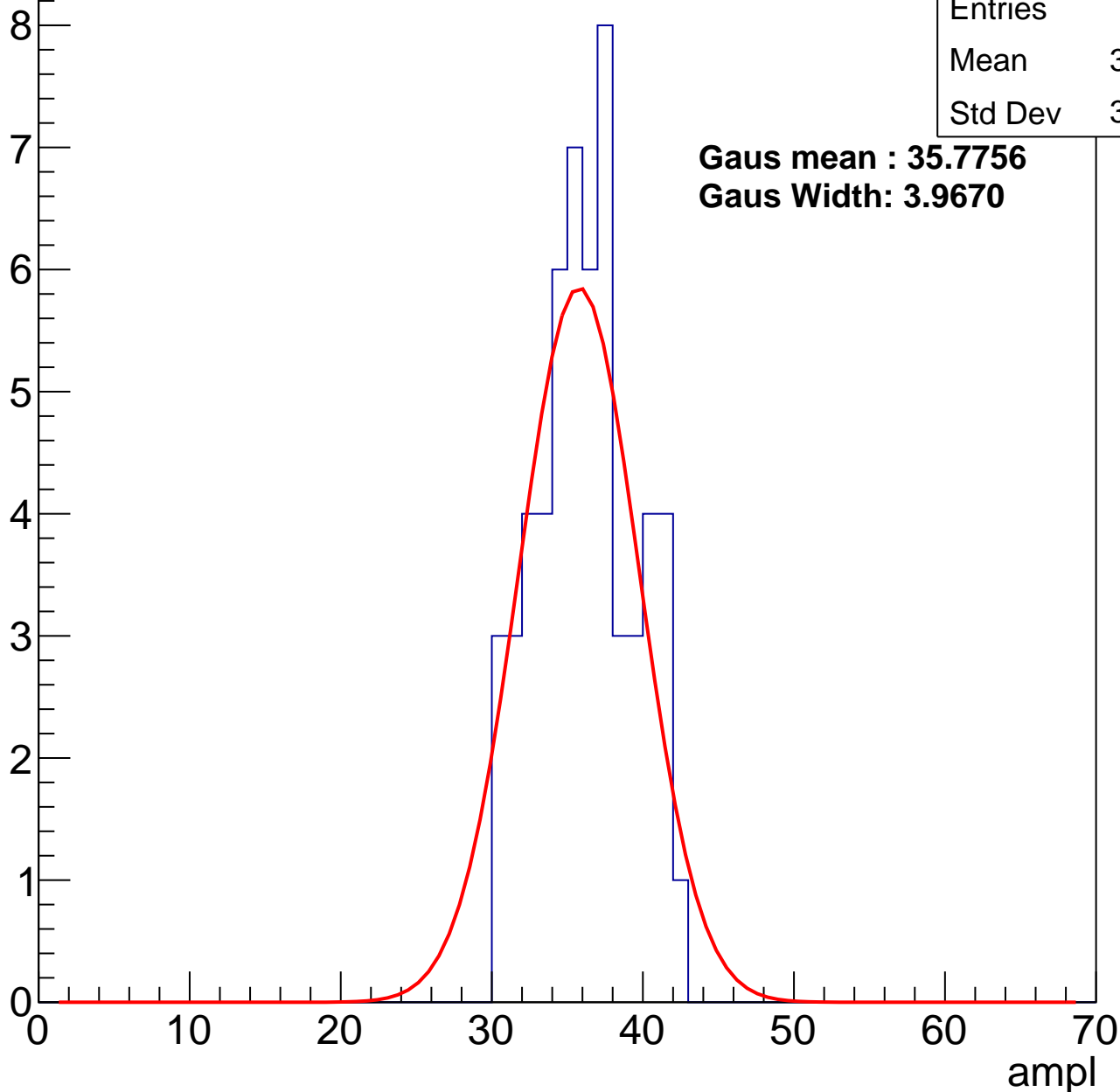
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	56
Mean	35.73
Std Dev	3.154

**Gaus mean : 35.7756**

**Gaus Width: 3.9670**



# B1L101S, U20-ch38, adc2

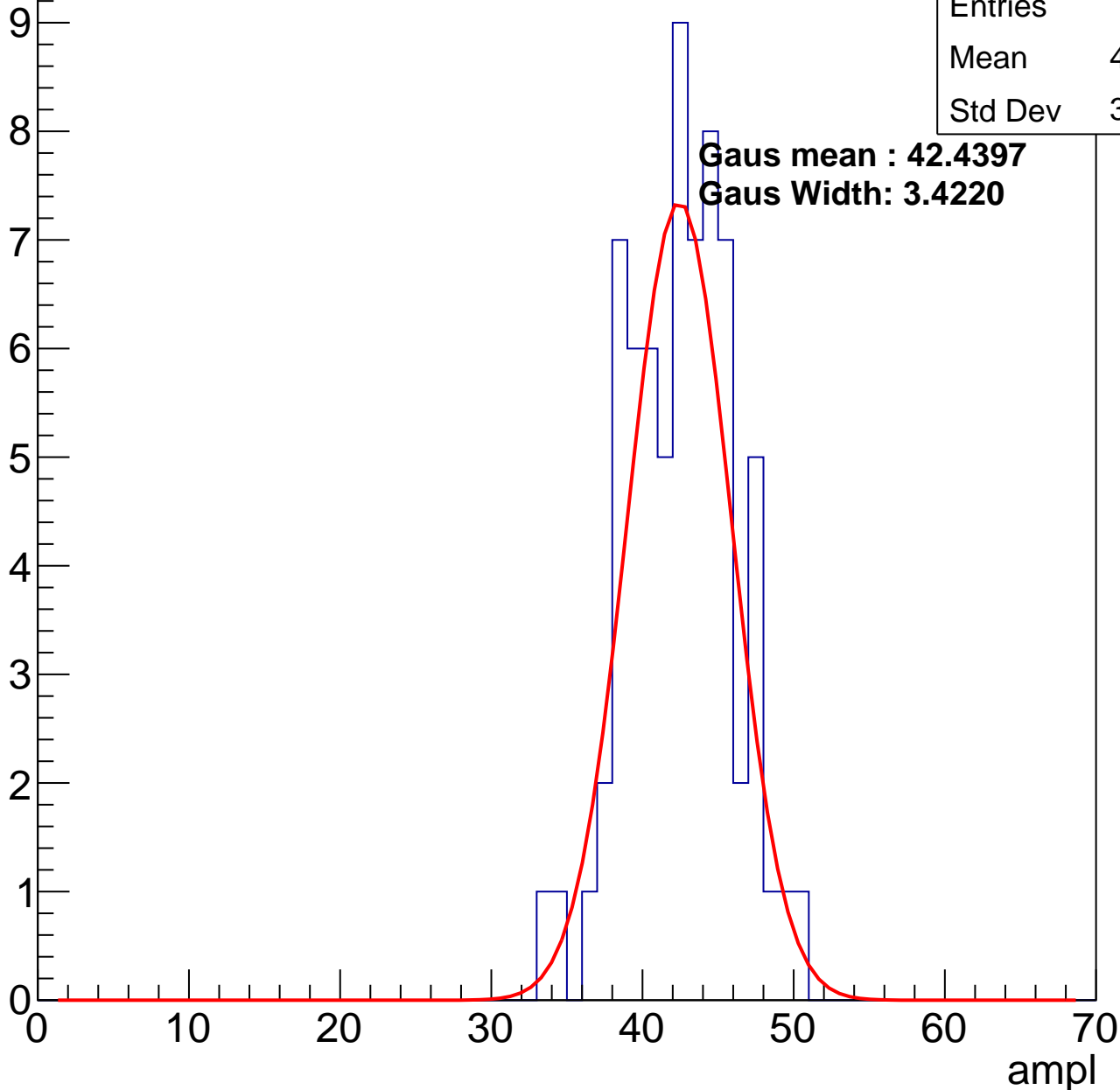
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	42.03
Std Dev	3.452

**Gaus mean : 42.4397**

**Gaus Width: 3.4220**

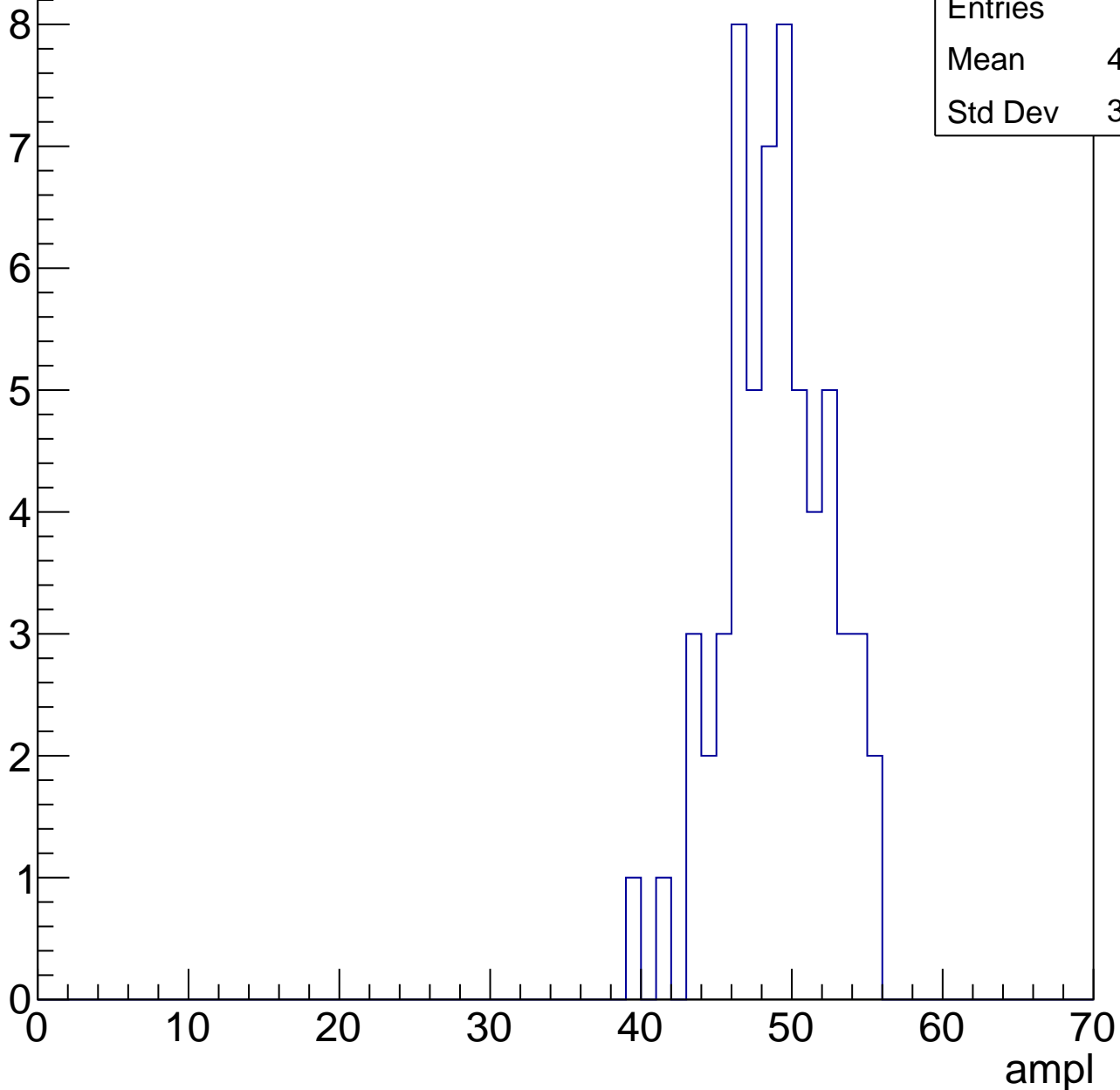


# B1L101S, U20-ch38, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	60
Mean	48.47
Std Dev	3.447

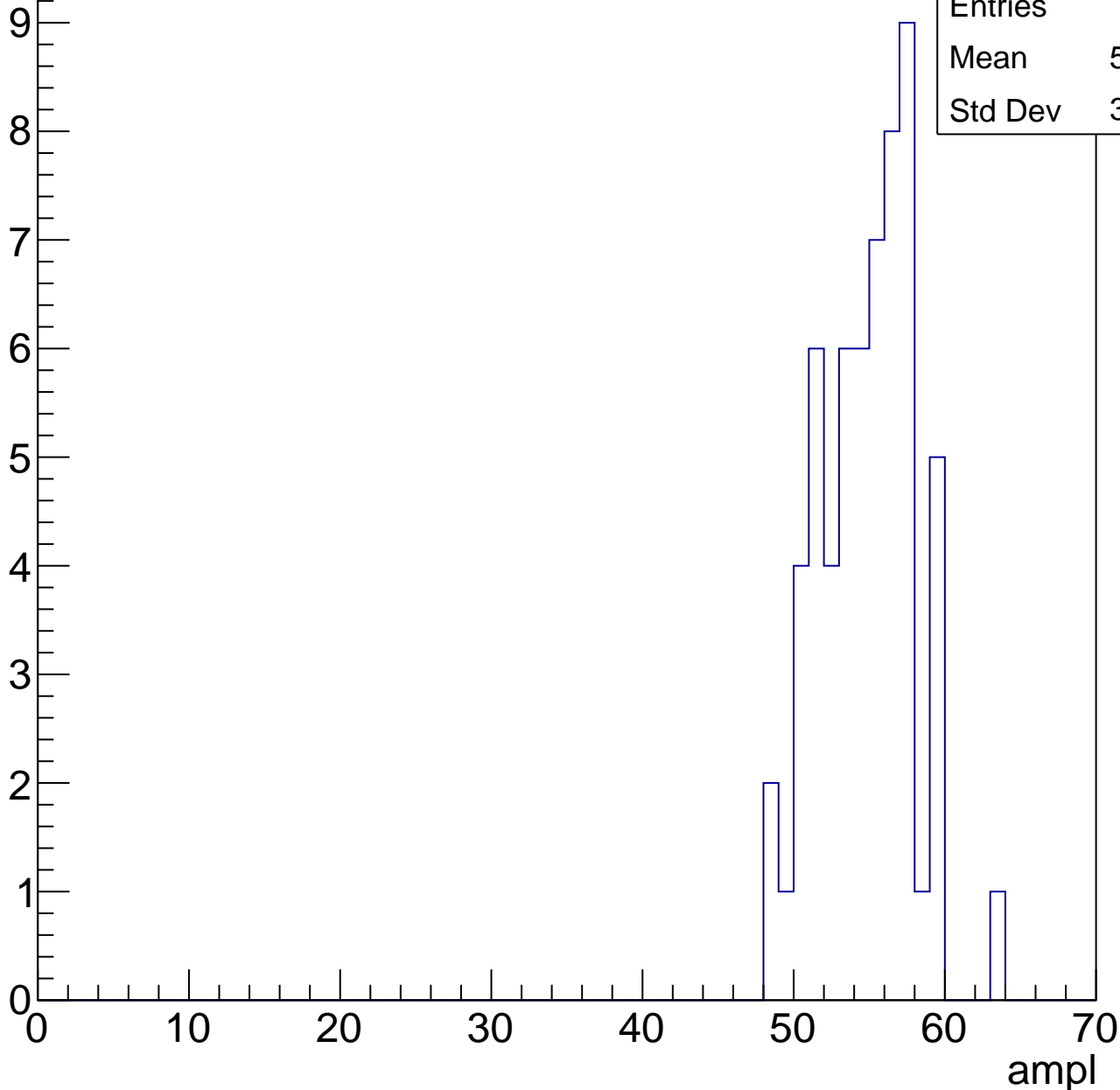


# B1L101S, U20-ch38, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

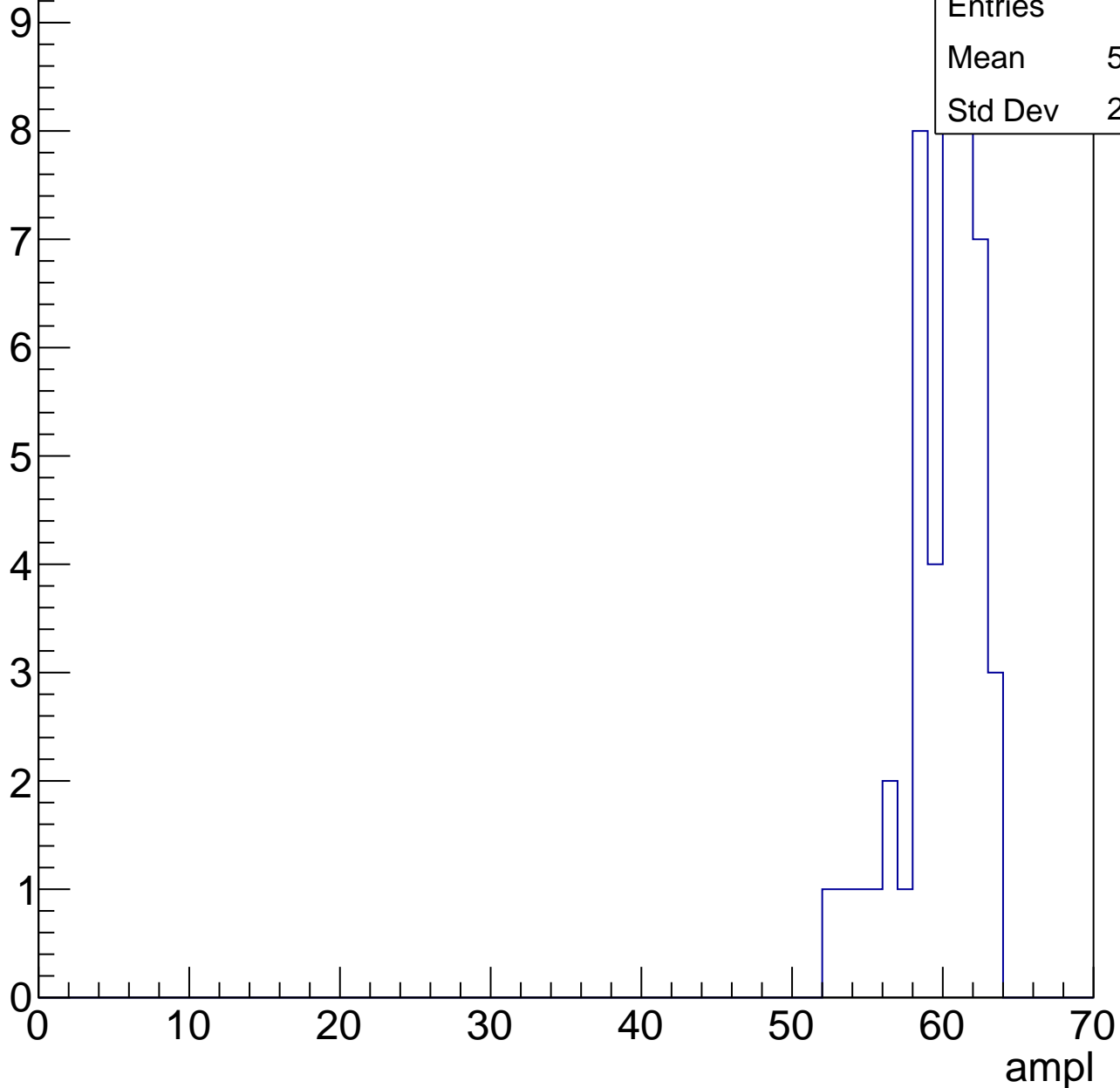
Entries	60
Mean	54.38
Std Dev	3.083



# B1L101S, U20-ch38, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

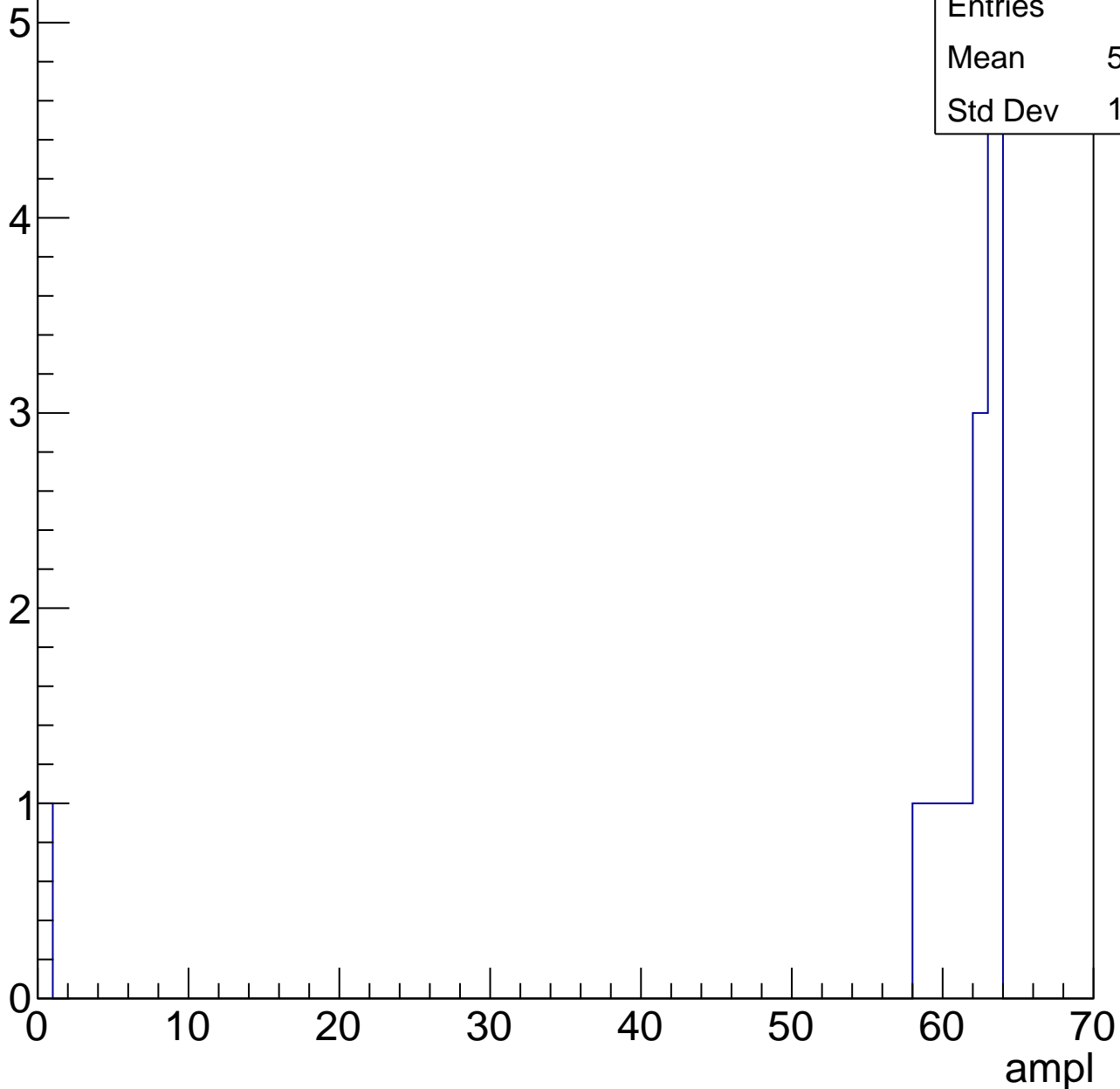


# B1L101S, U20-ch38, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	13
Mean	56.85
Std Dev	16.49





# B1L101S, U20-ch38, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U20-ch39, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	77
Mean	29.34
Std Dev	5.872

**Gaus mean : 30.9825**

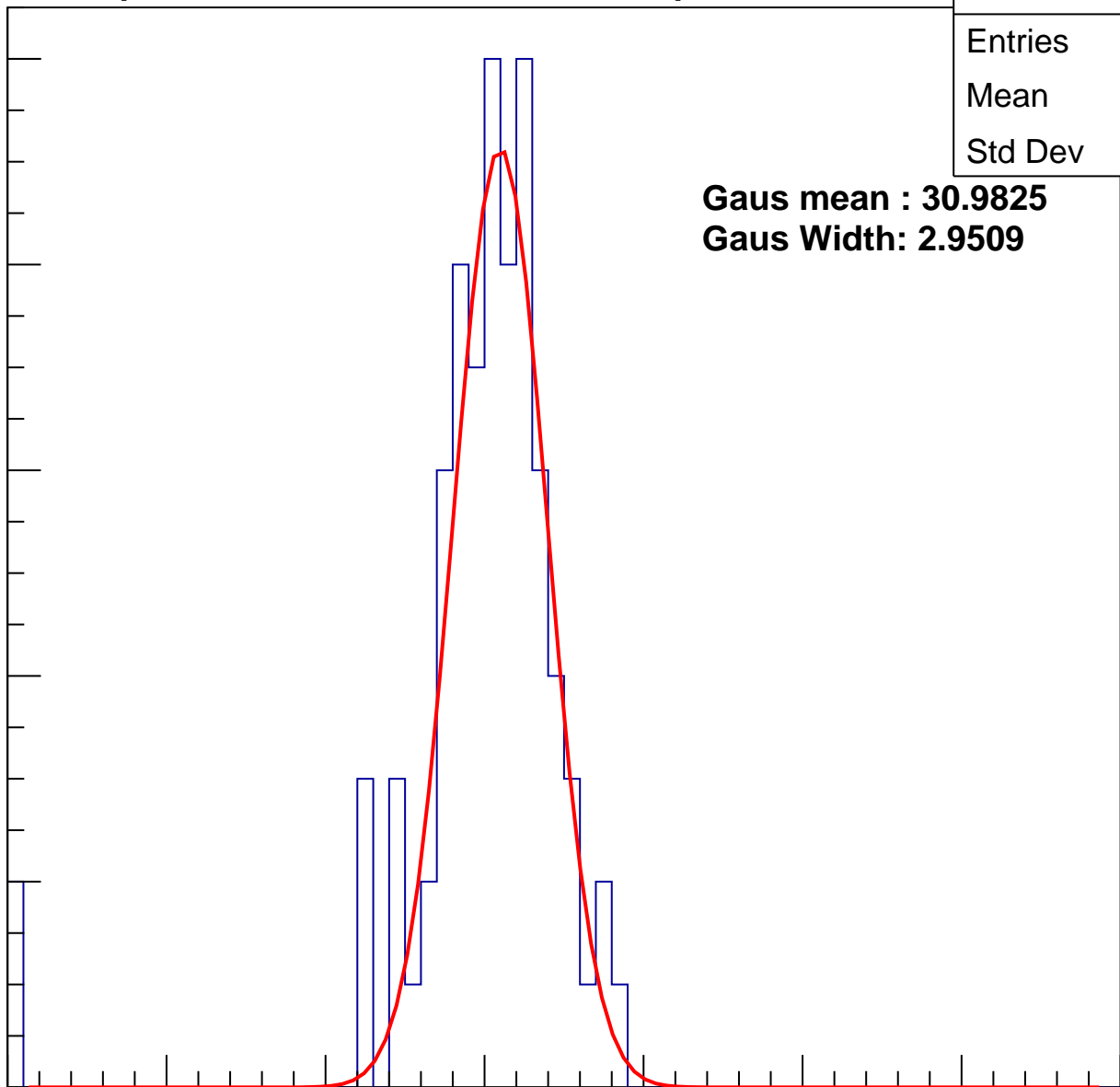
**Gaus Width: 2.9509**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U20-ch39, adc1

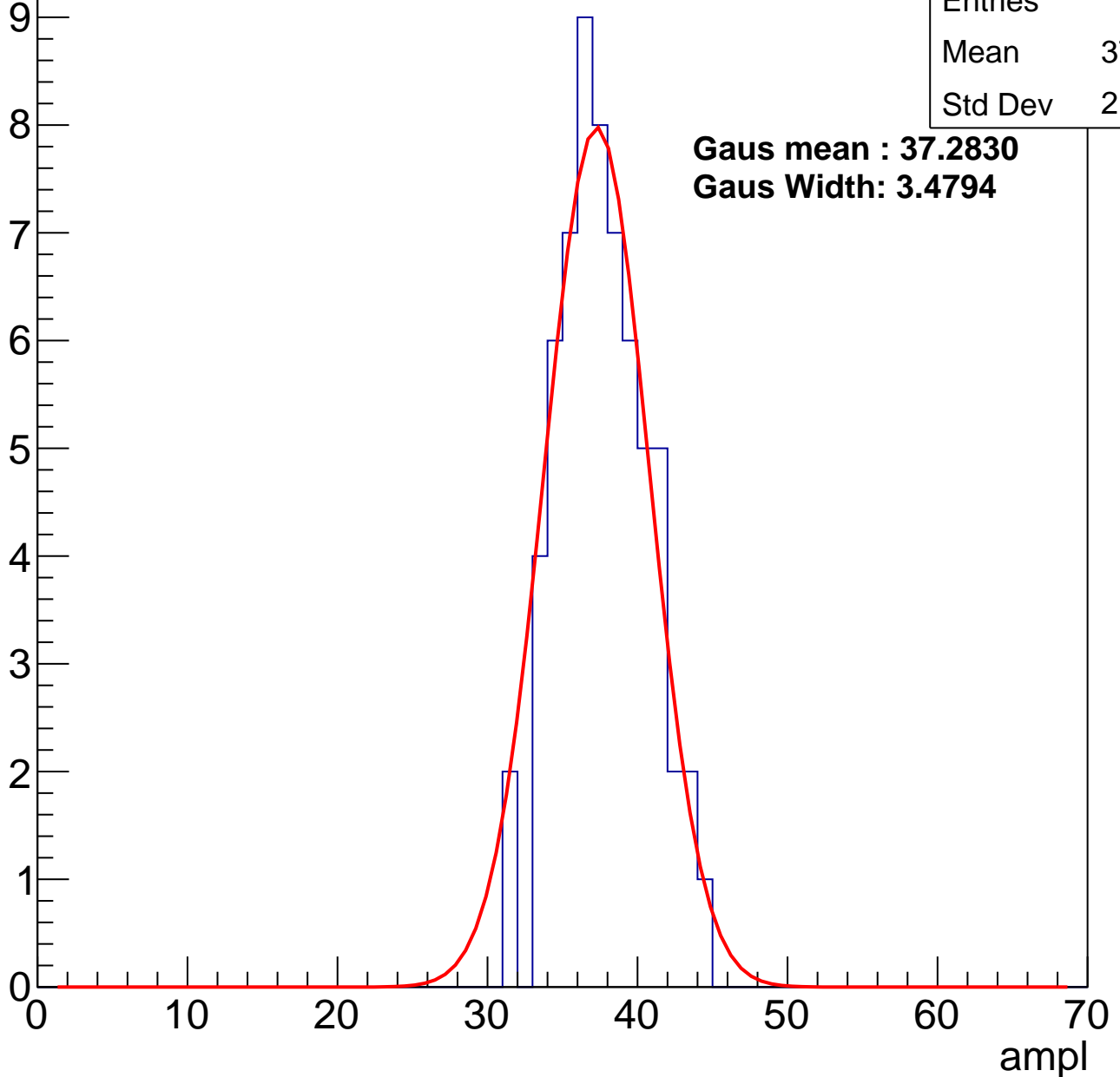
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	37.22
Std Dev	2.934

**Gaus mean : 37.2830**

**Gaus Width: 3.4794**



# B1L101S, U20-ch39, adc2

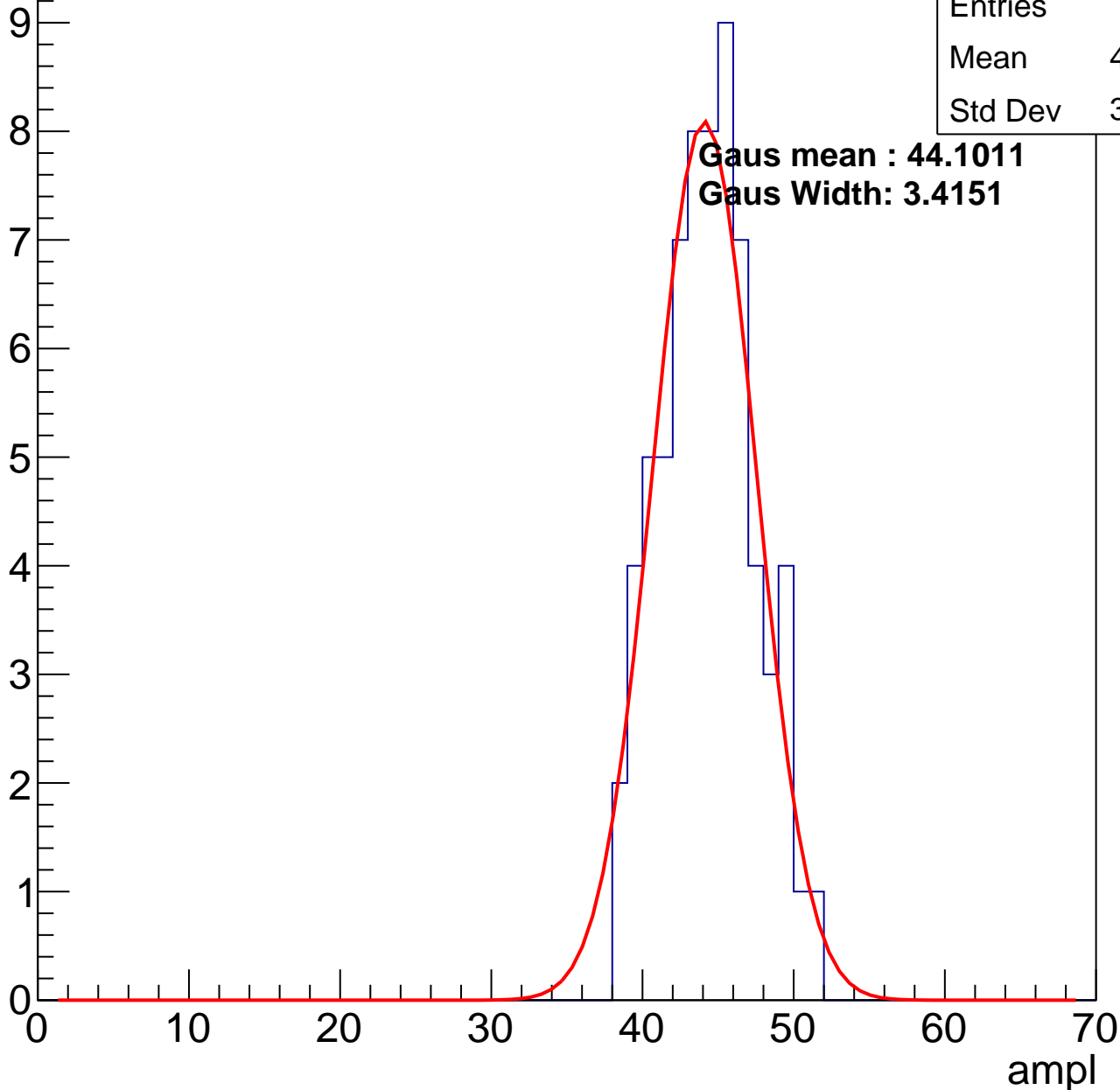
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	43.87
Std Dev	3.063

**Gaus mean : 44.1011**

**Gaus Width: 3.4151**

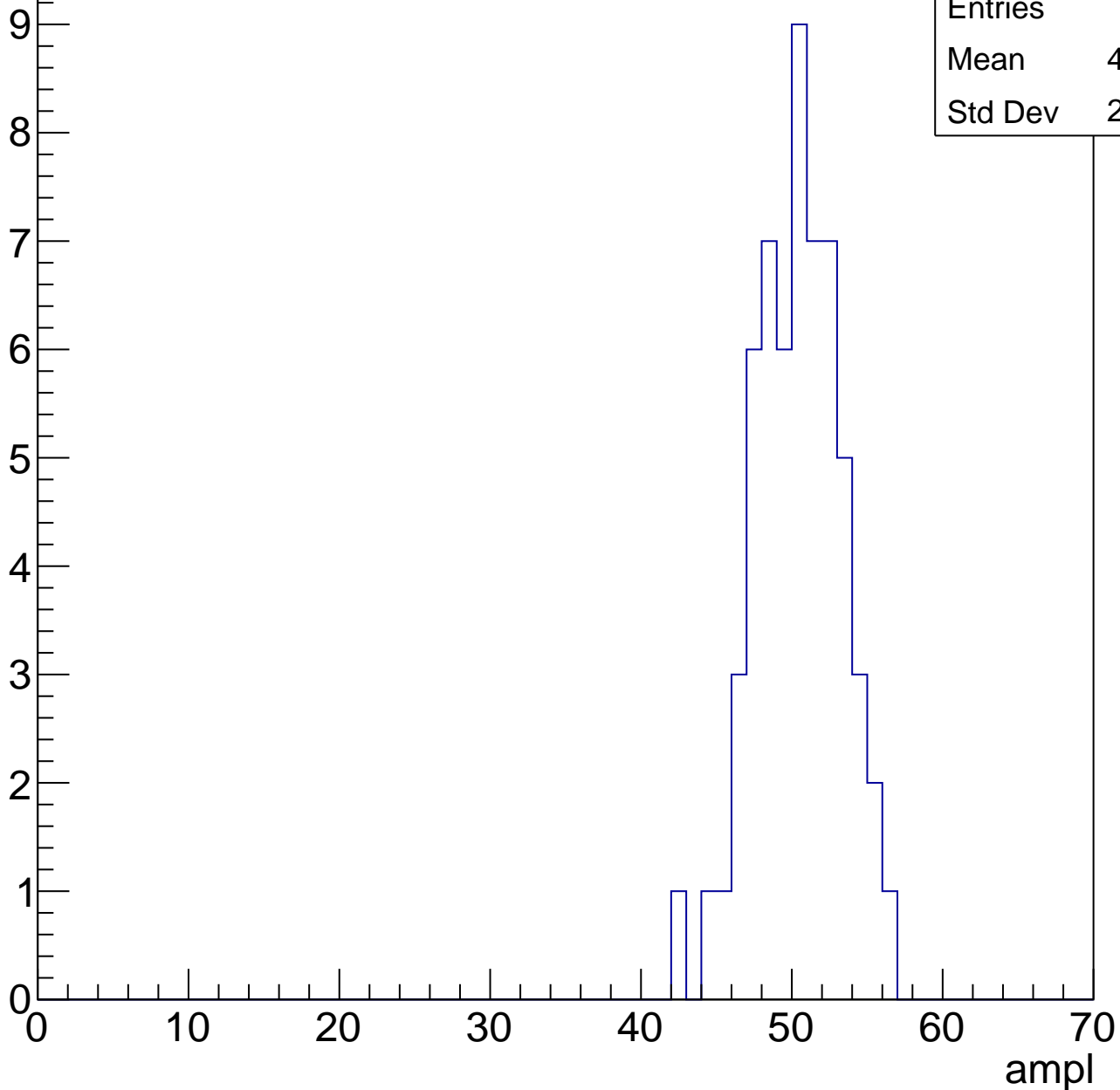


# B1L101S, U20-ch39, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	59
Mean	49.92
Std Dev	2.836

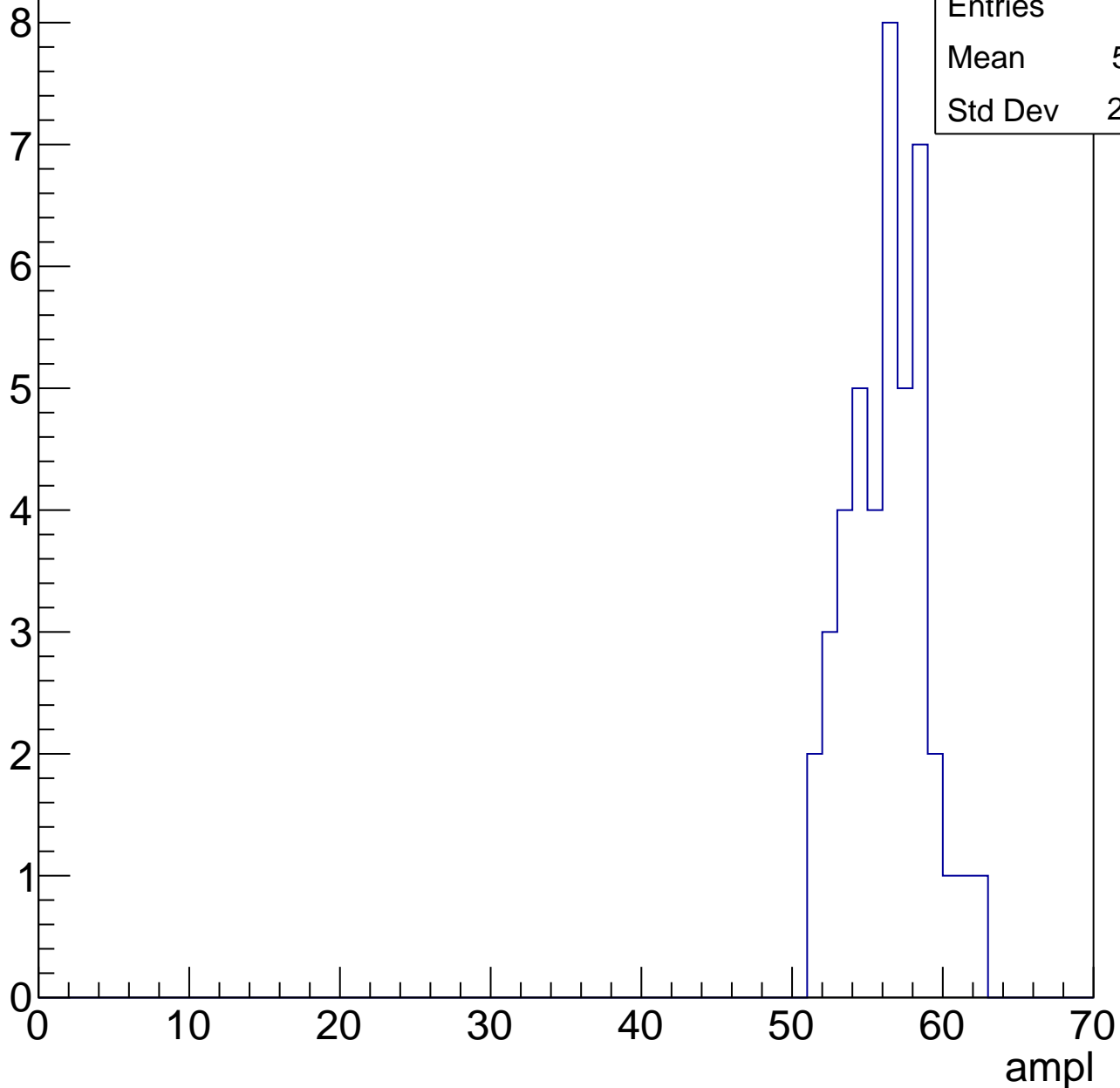


# B1L101S, U20-ch39, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

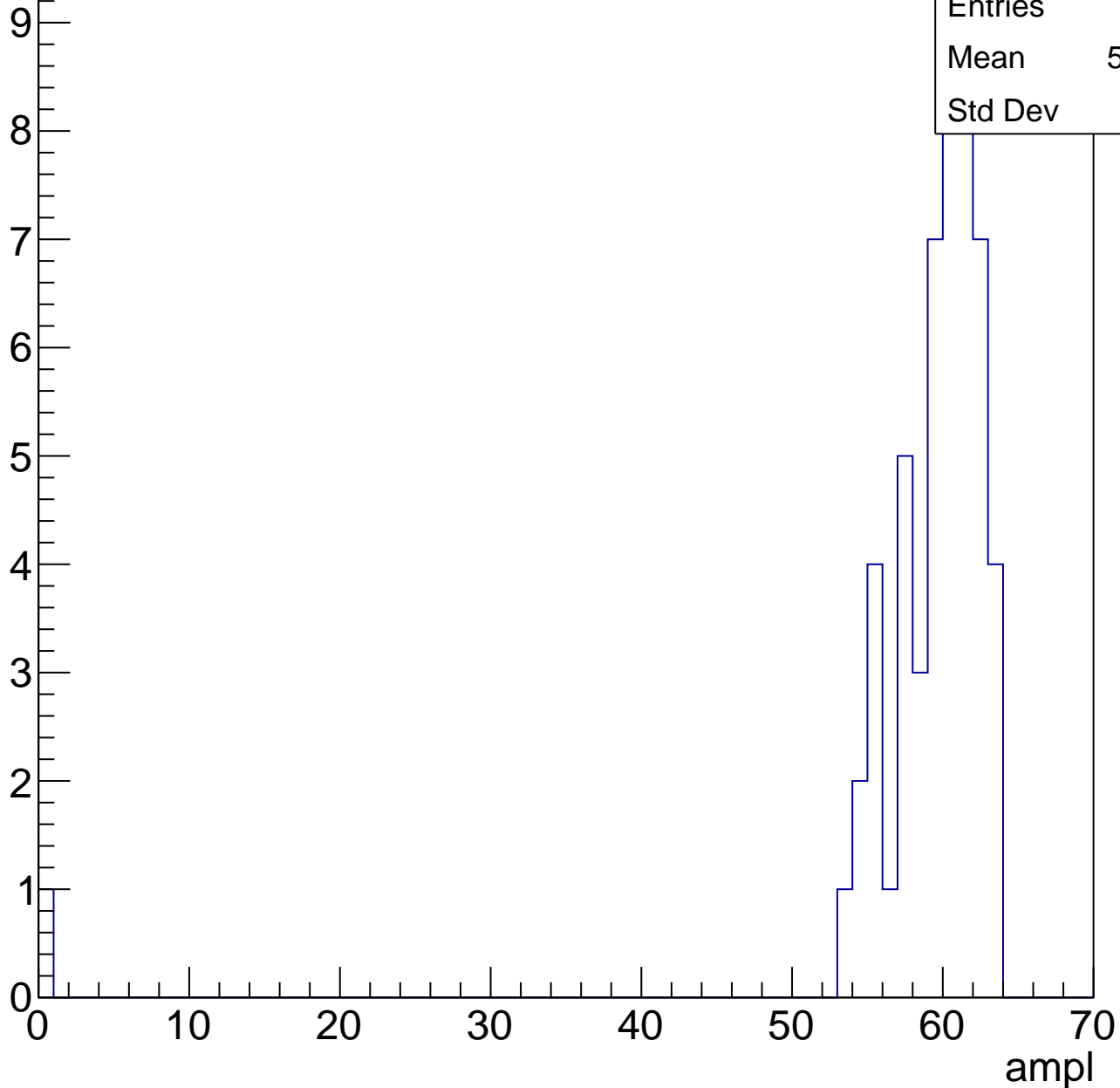
Entries	43
Mean	55.81
Std Dev	2.572



# B1L101S, U20-ch39, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

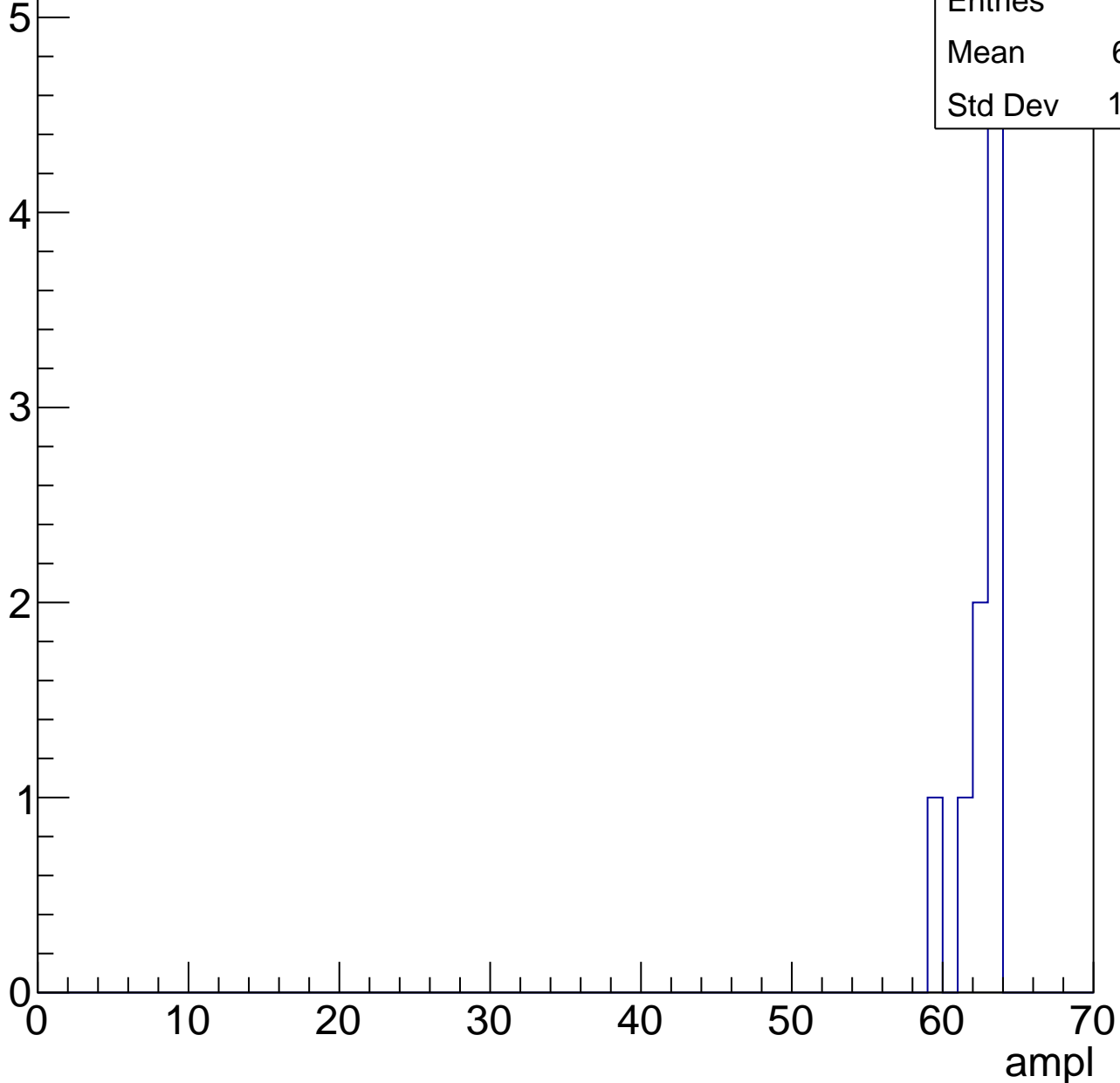


# B1L101S, U20-ch39, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	9
Mean	62.11
Std Dev	1.286





# B1L101S, U20-ch39, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U20-ch40, adc0

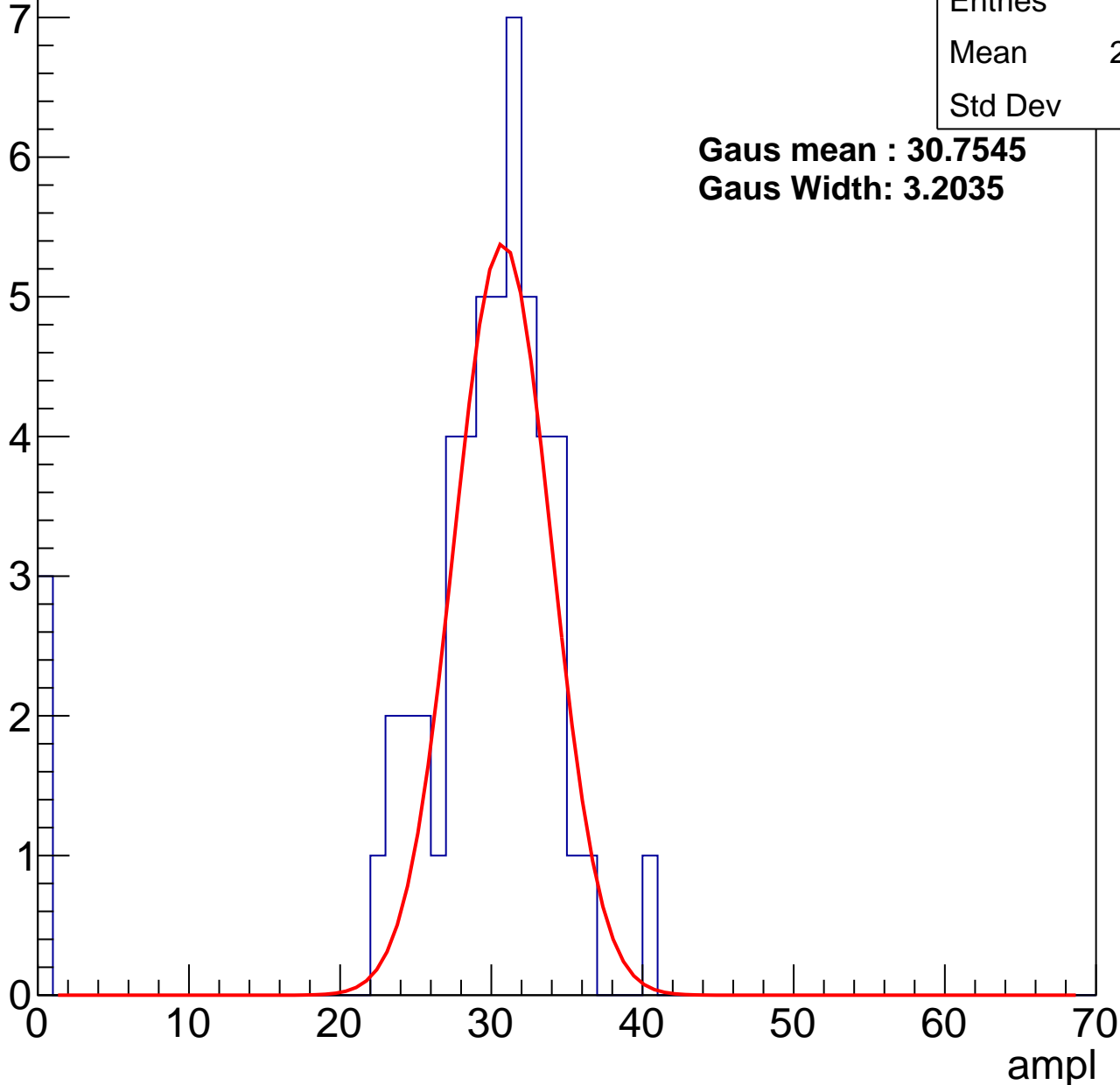
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	52
Mean	28.13
Std Dev	7.8

**Gaus mean : 30.7545**

**Gaus Width: 3.2035**



# B1L101S, U20-ch40, adc1

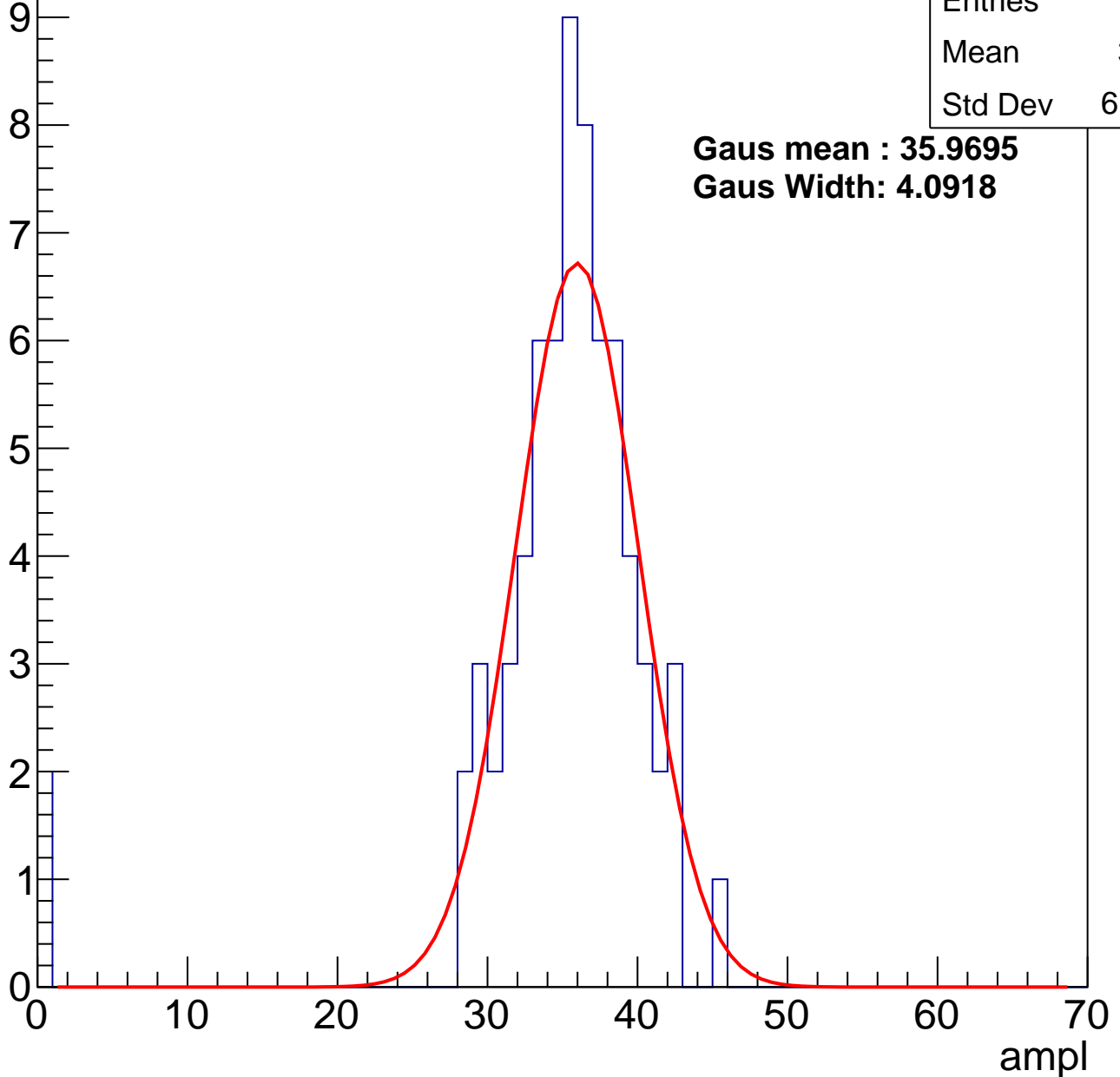
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	34.4
Std Dev	6.906

**Gaus mean : 35.9695**

**Gaus Width: 4.0918**



# B1L101S, U20-ch40, adc2

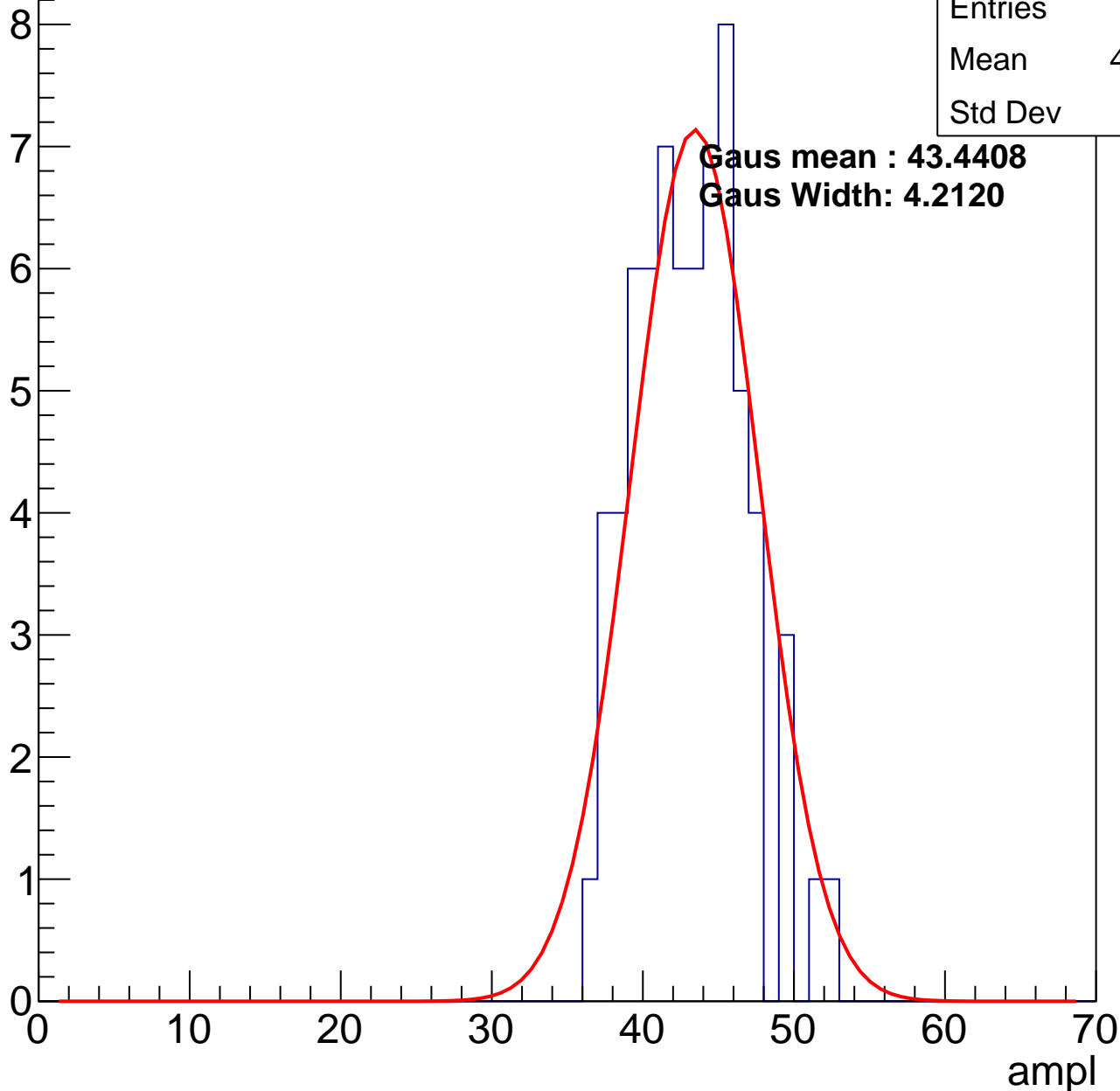
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	42.65
Std Dev	3.55

**Gaus mean : 43.4408**

**Gaus Width: 4.2120**

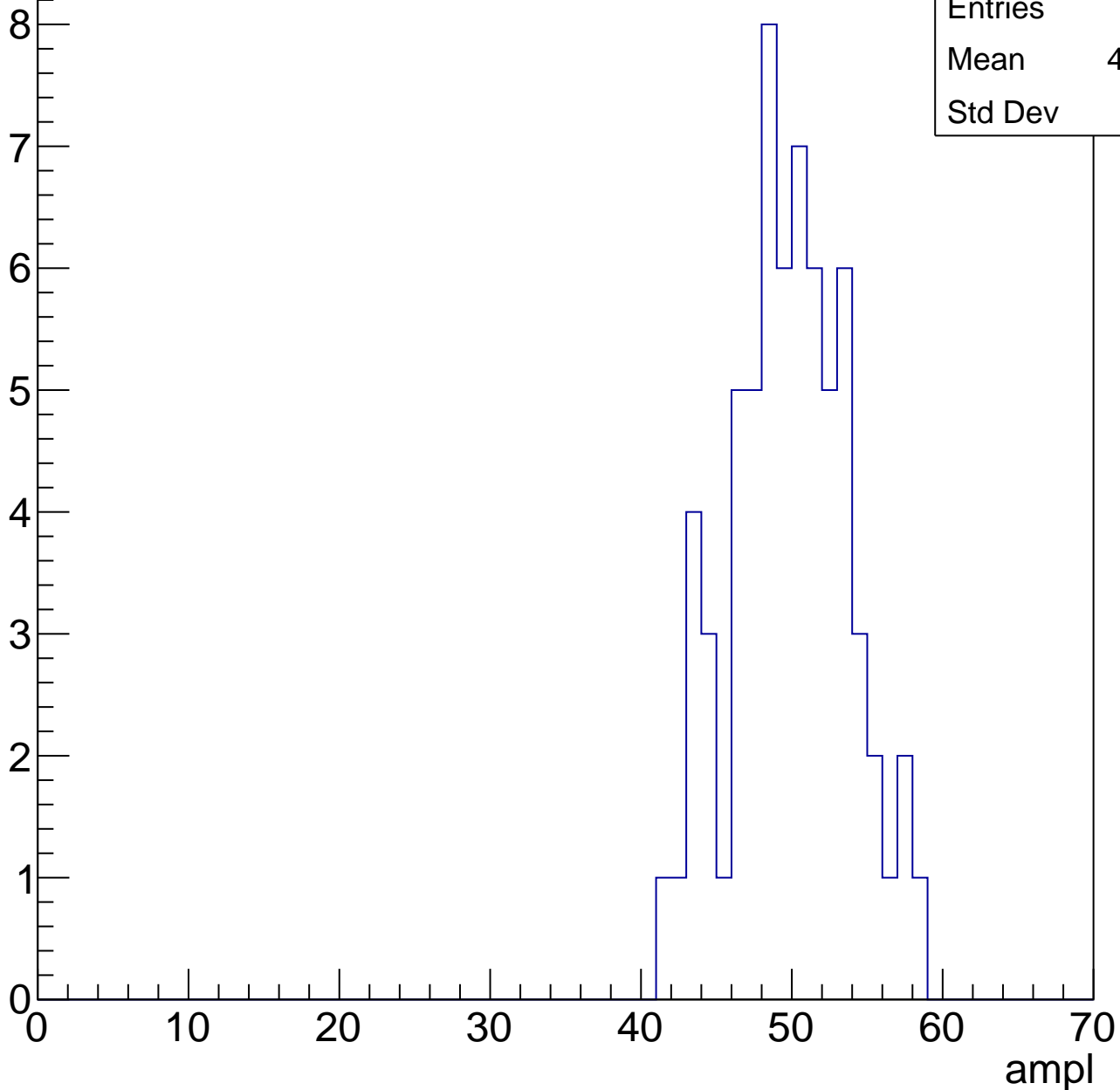


# B1L101S, U20-ch40, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	67
Mean	49.39
Std Dev	3.84

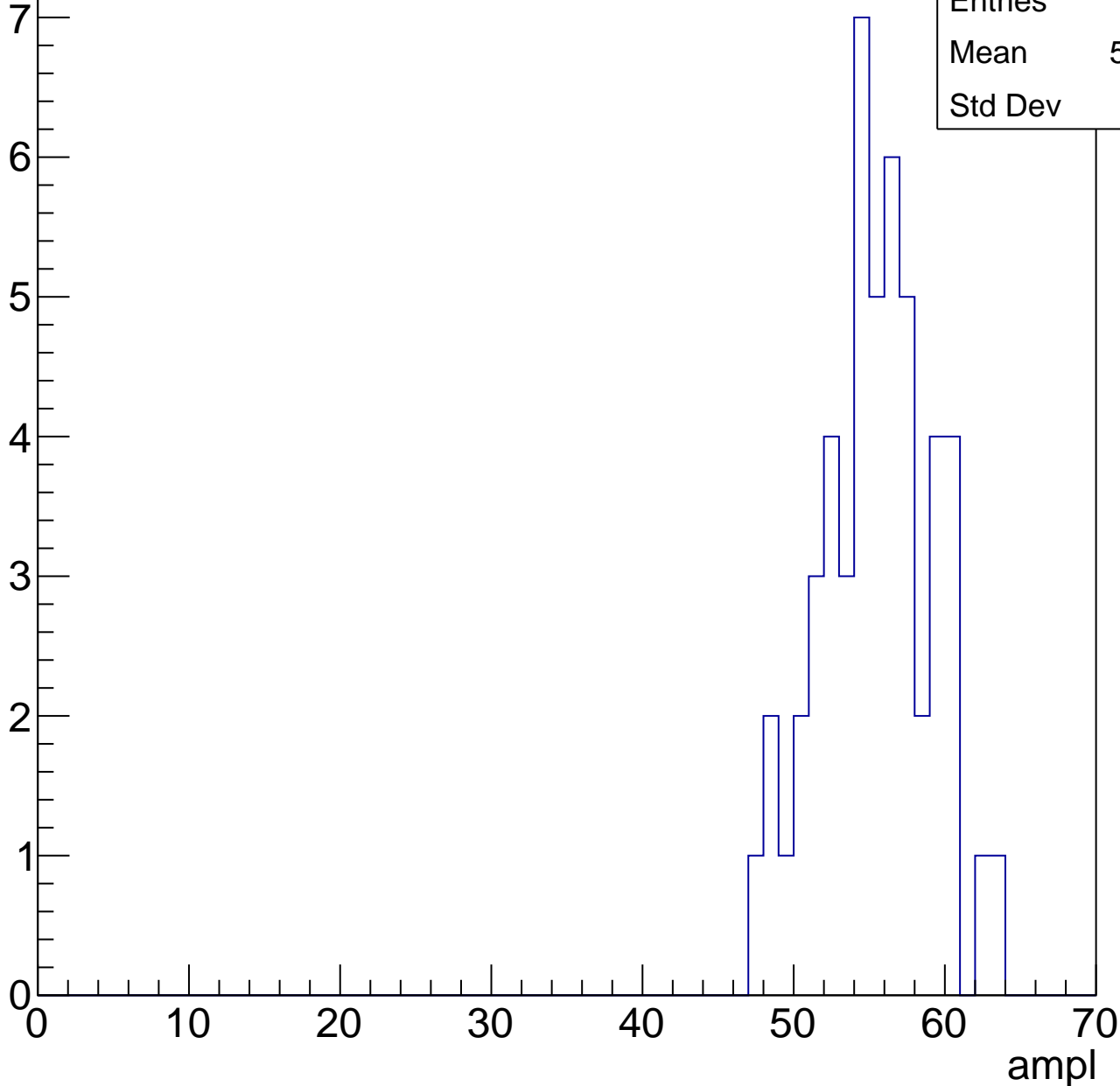


# B1L101S, U20-ch40, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	51
Mean	54.96
Std Dev	3.63

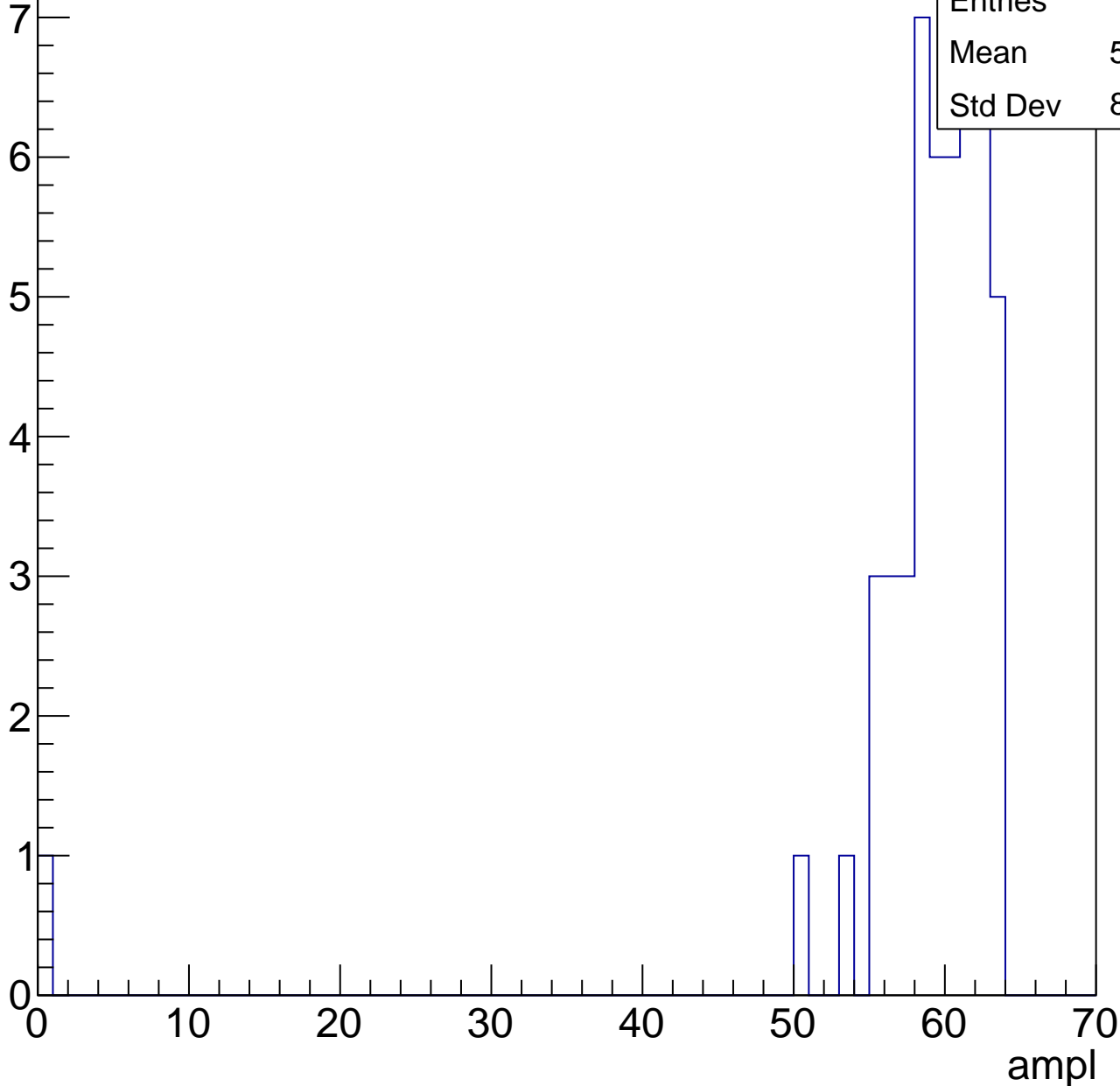


# B1L101S, U20-ch40, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

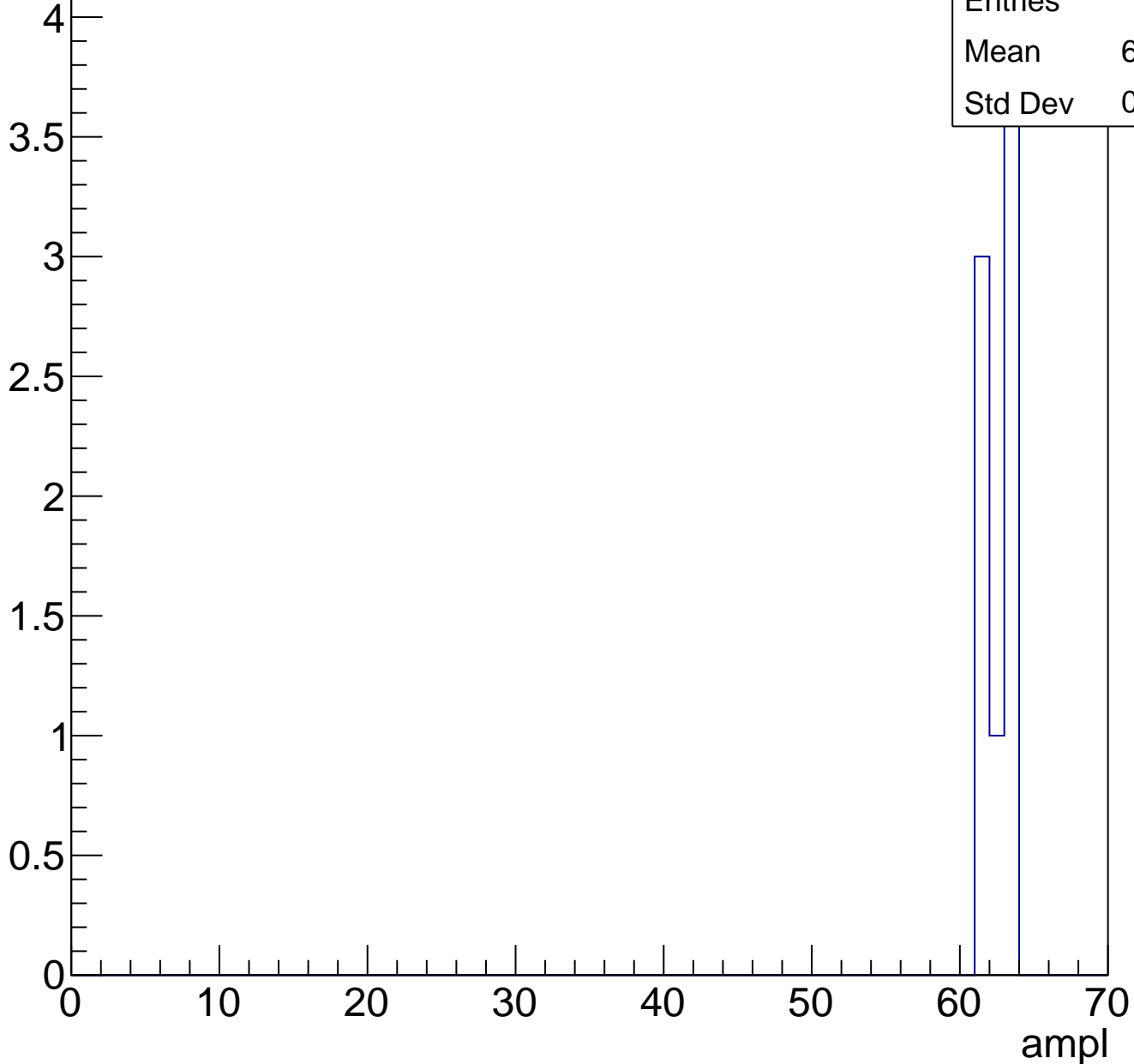
Entries	50
Mean	58.06
Std Dev	8.746



# B1L101S, U20-ch40, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U20-ch40, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U20-ch41, adc0

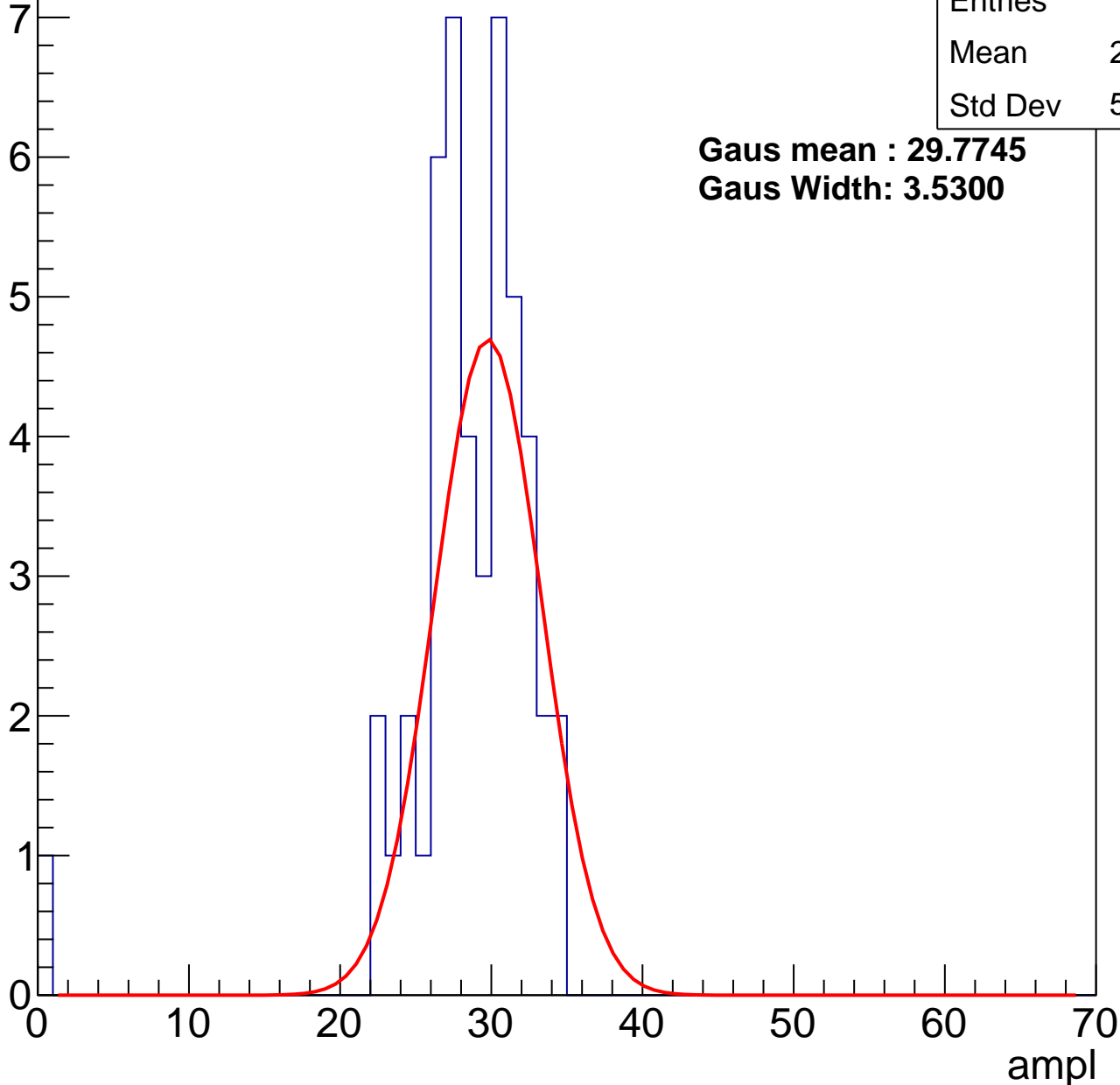
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	47
Mean	27.89
Std Dev	5.083

**Gaus mean : 29.7745**

**Gaus Width: 3.5300**



# B1L101S, U20-ch41, adc1

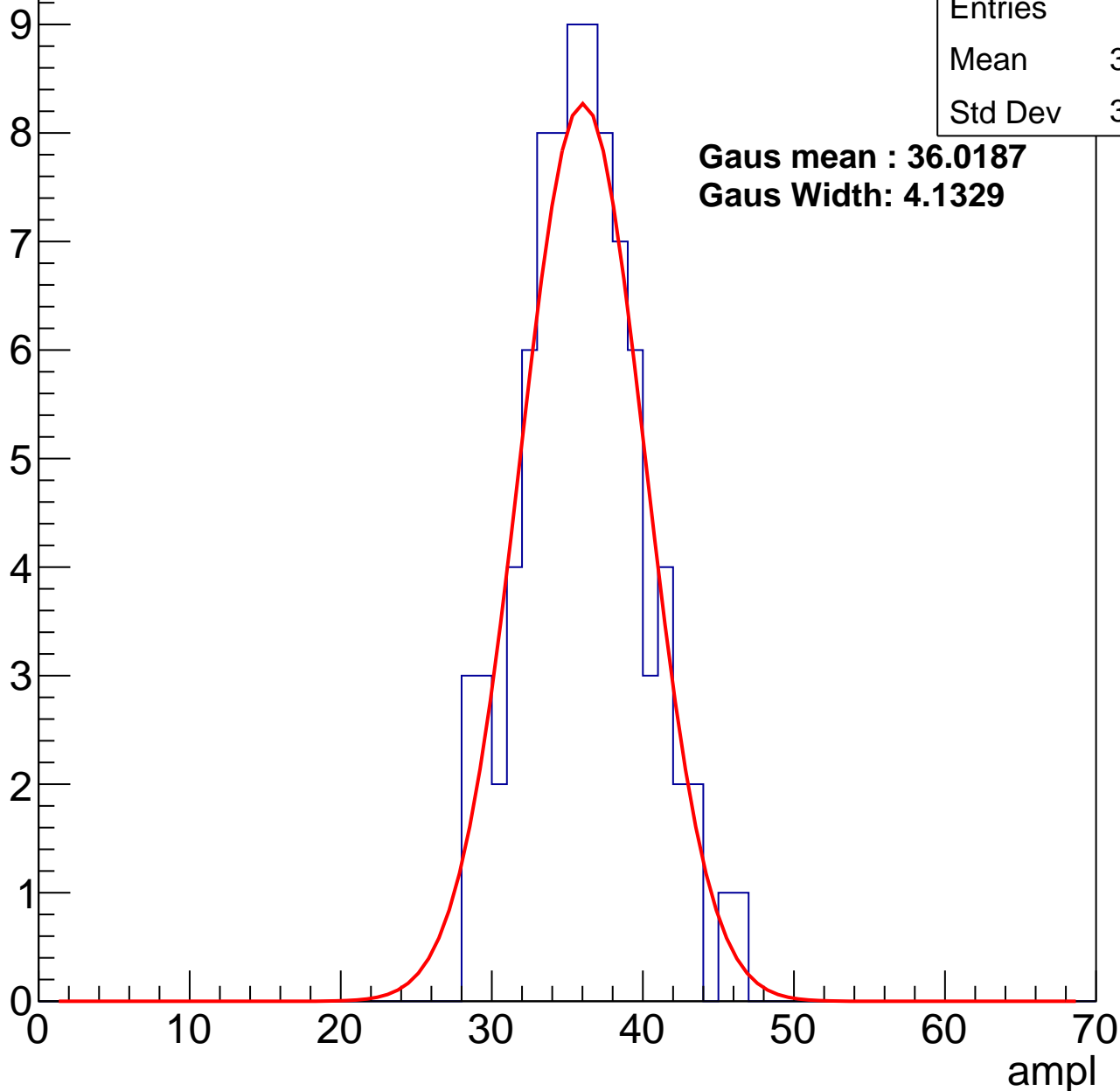
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	86
Mean	35.62
Std Dev	3.882

**Gaus mean : 36.0187**

**Gaus Width: 4.1329**



# B1L101S, U20-ch41, adc2

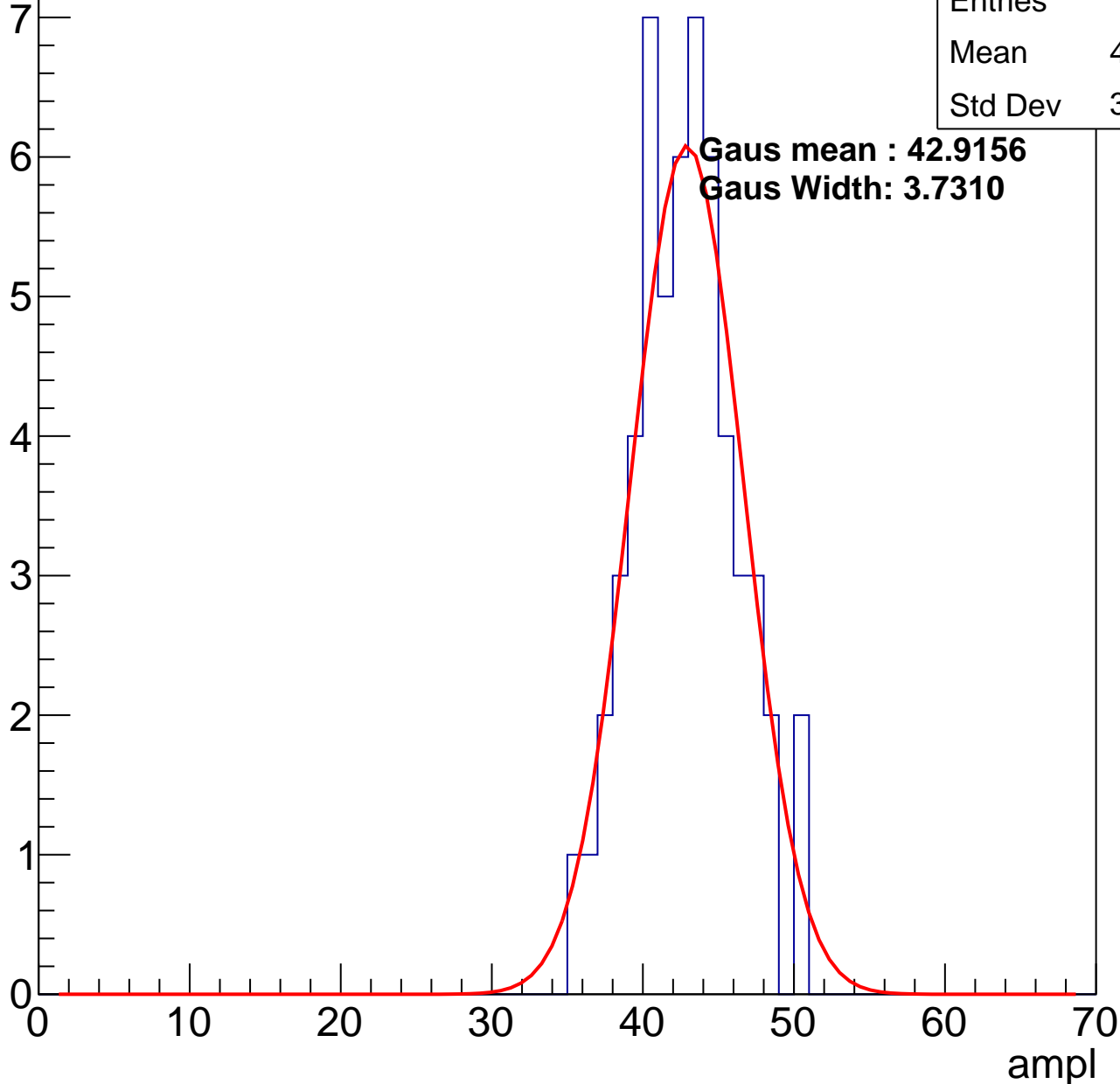
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	56
Mean	42.36
Std Dev	3.367

**Gaus mean : 42.9156**

**Gaus Width: 3.7310**



# B1L101S, U20-ch41, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	79
Mean	49.24
Std Dev	3.708

Entry

10

8

6

4

2

0

0

10

20

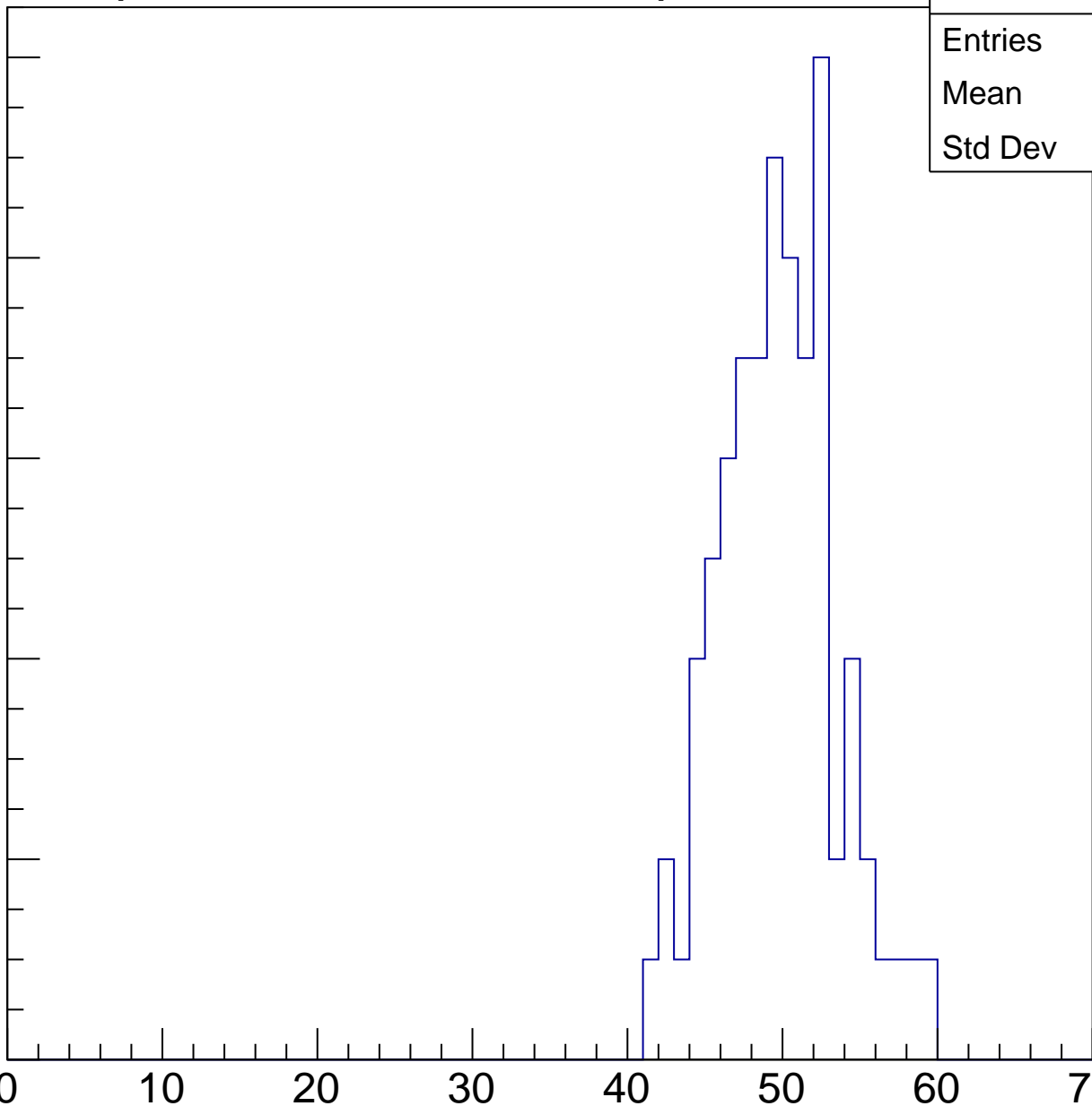
30

40

50

60

ampl

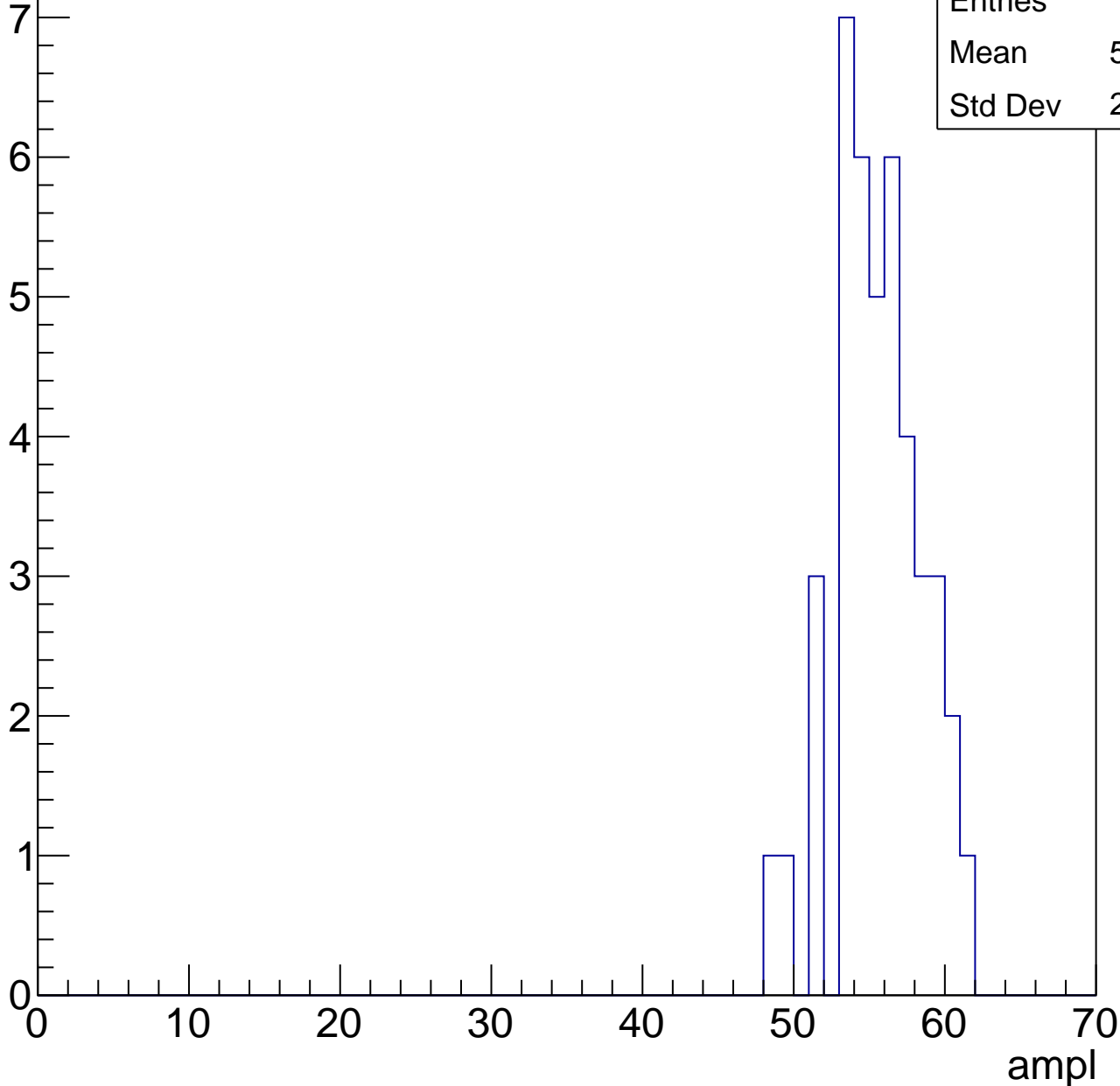


# B1L101S, U20-ch41, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

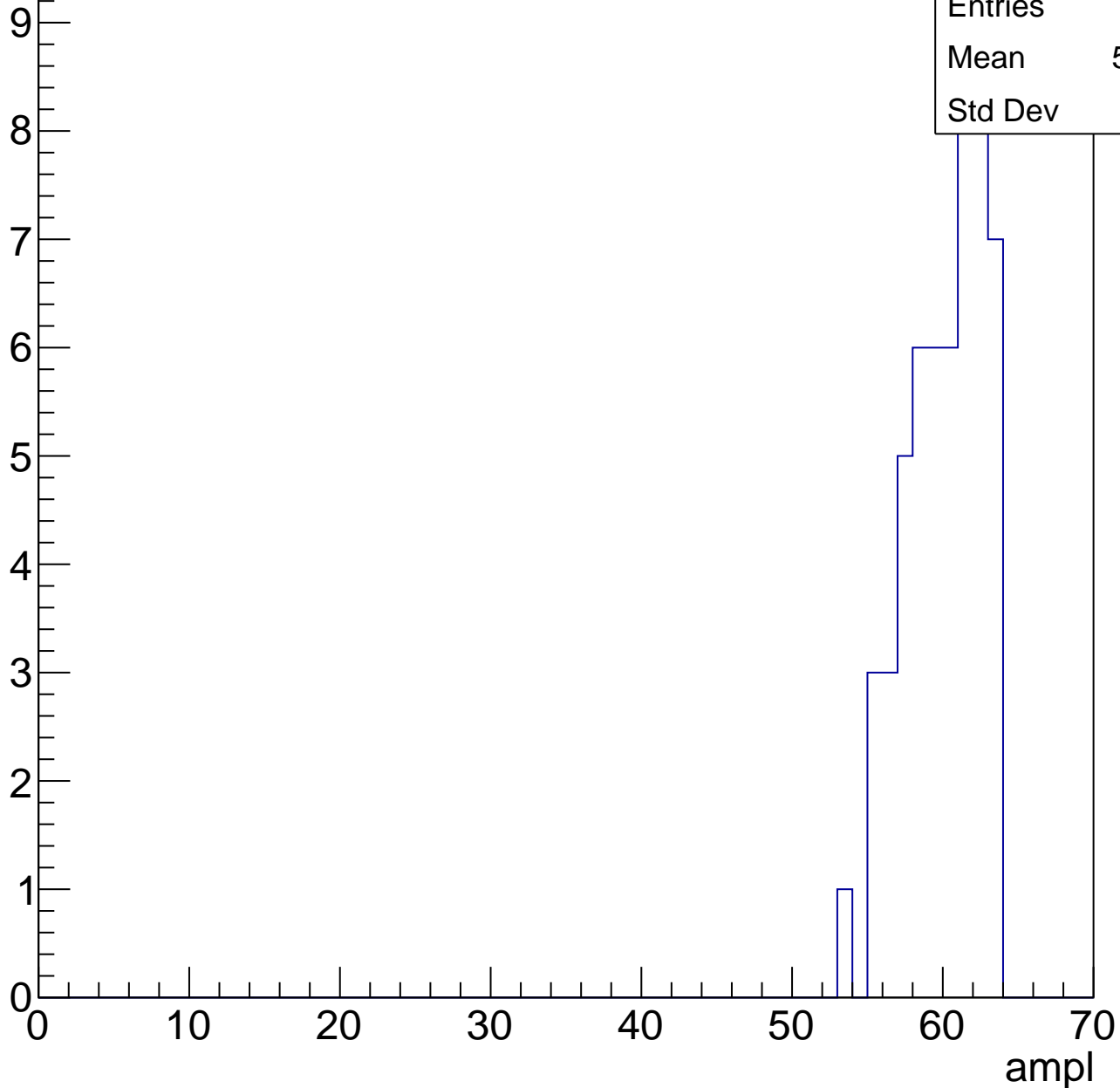
Entries	42
Mean	55.14
Std Dev	2.883



# B1L101S, U20-ch41, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

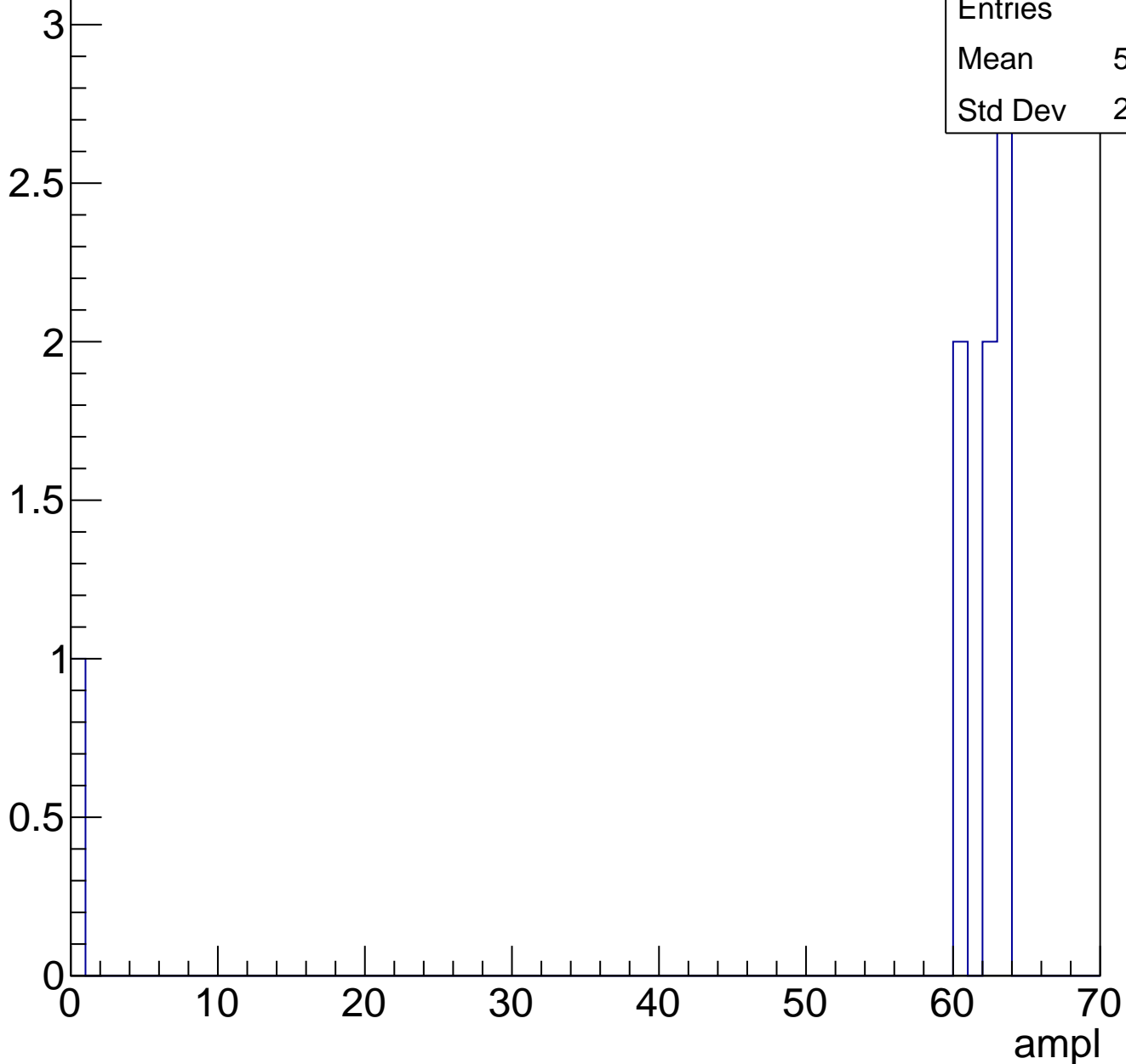
Entry



# B1L101S, U20-ch41, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	8
Mean	54.12
Std Dev	20.49



# B1L101S, U20-ch41, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L101S, U20-ch42, adc0

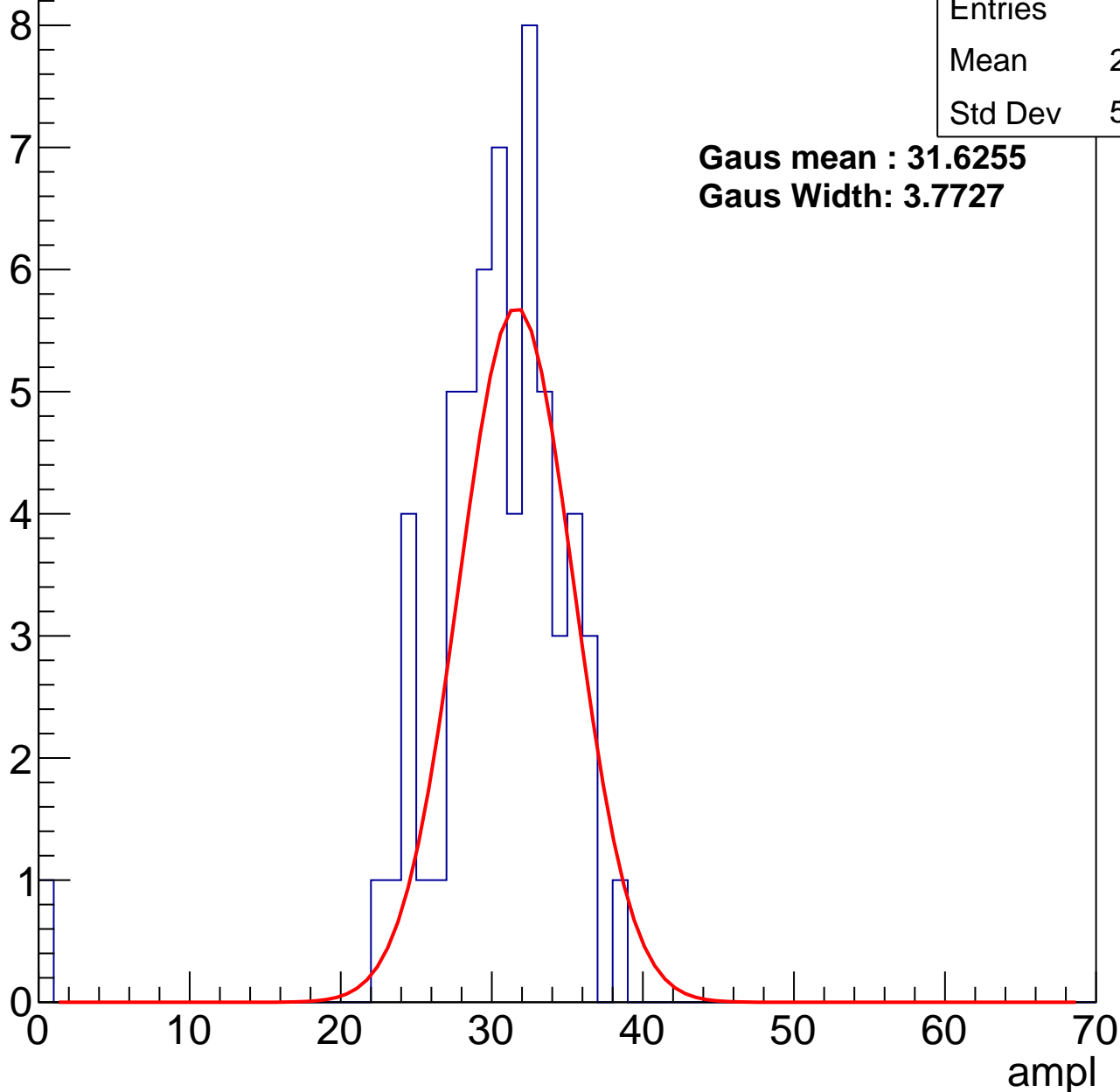
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	60
Mean	29.73
Std Dev	5.269

**Gaus mean : 31.6255**

**Gaus Width: 3.7727**



# B1L101S, U20-ch42, adc1

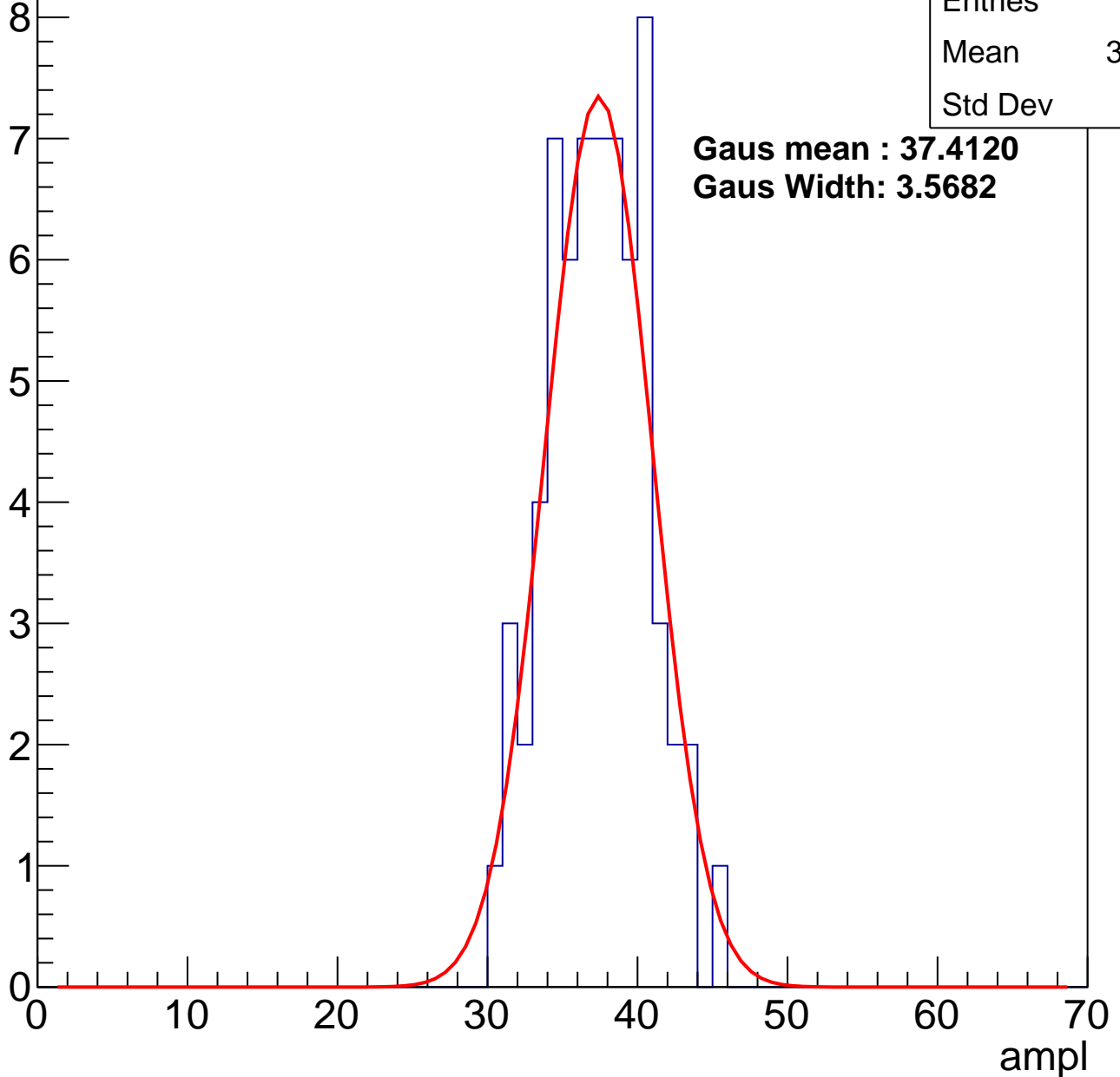
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	66
Mean	36.91
Std Dev	3.26

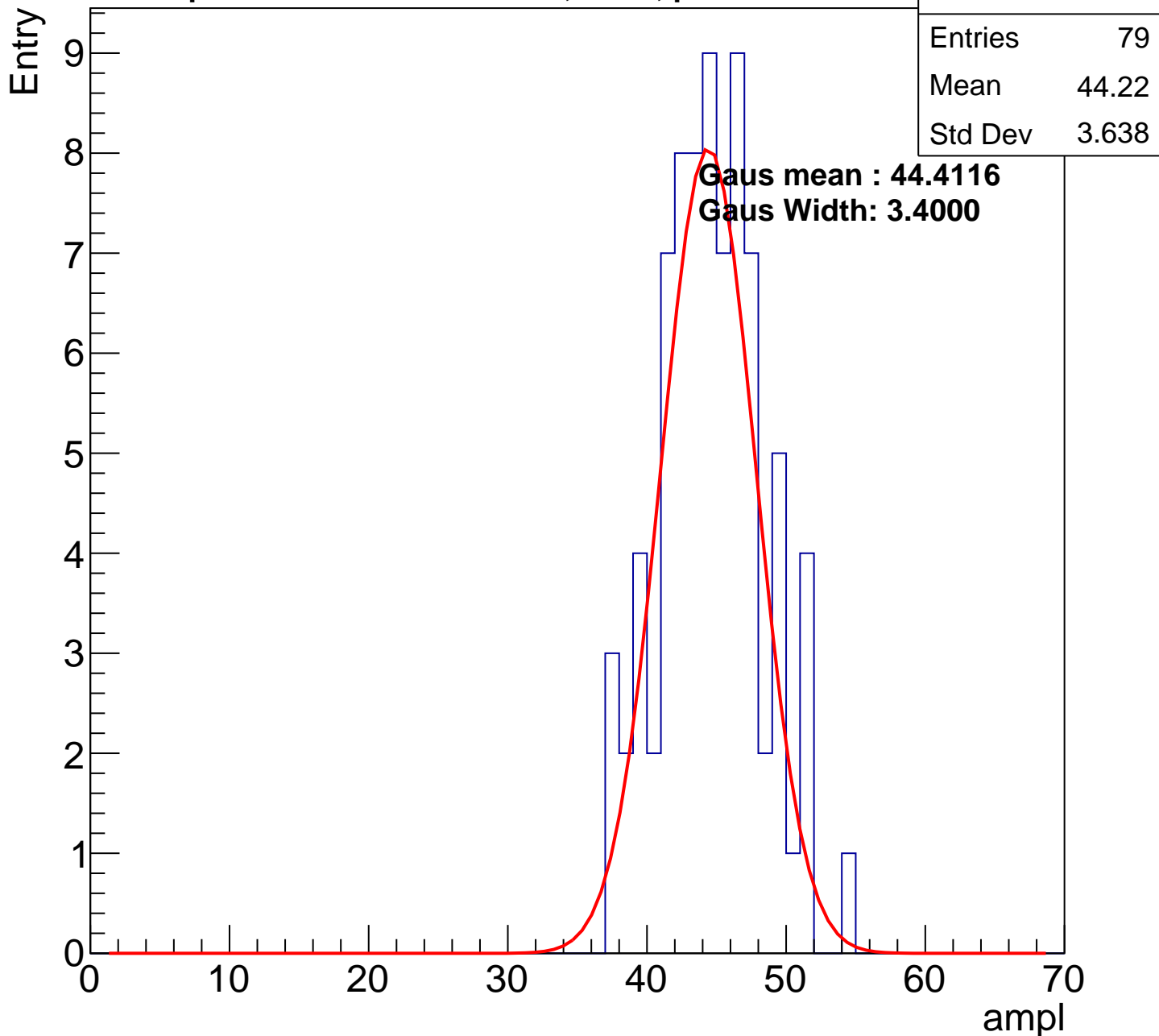
**Gaus mean : 37.4120**

**Gaus Width: 3.5682**



# B1L101S, U20-ch42, adc2

calib\_packv5\_042523\_0143.root, FC#0, port D2

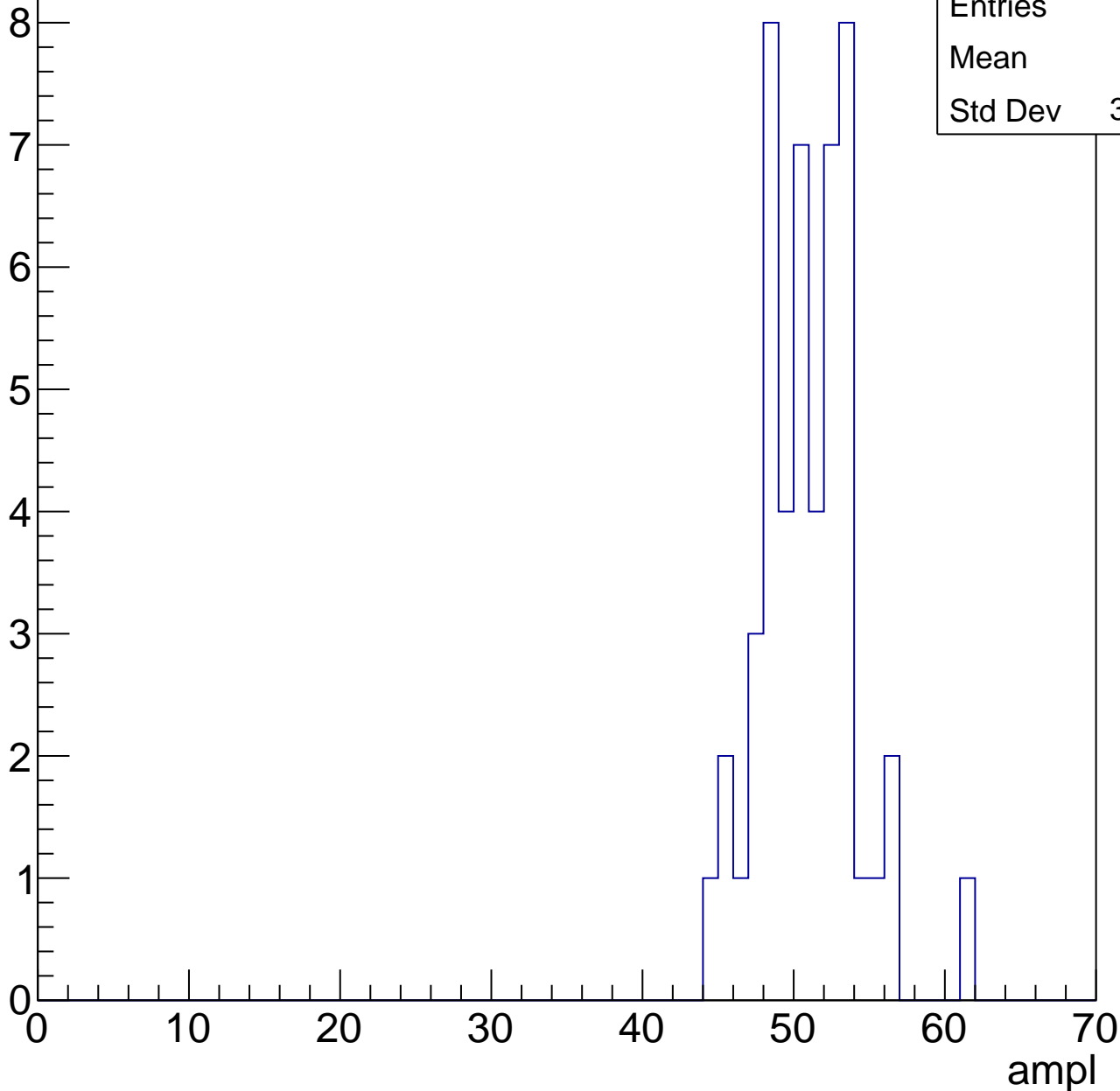


# B1L101S, U20-ch42, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	50
Mean	50.5
Std Dev	3.132

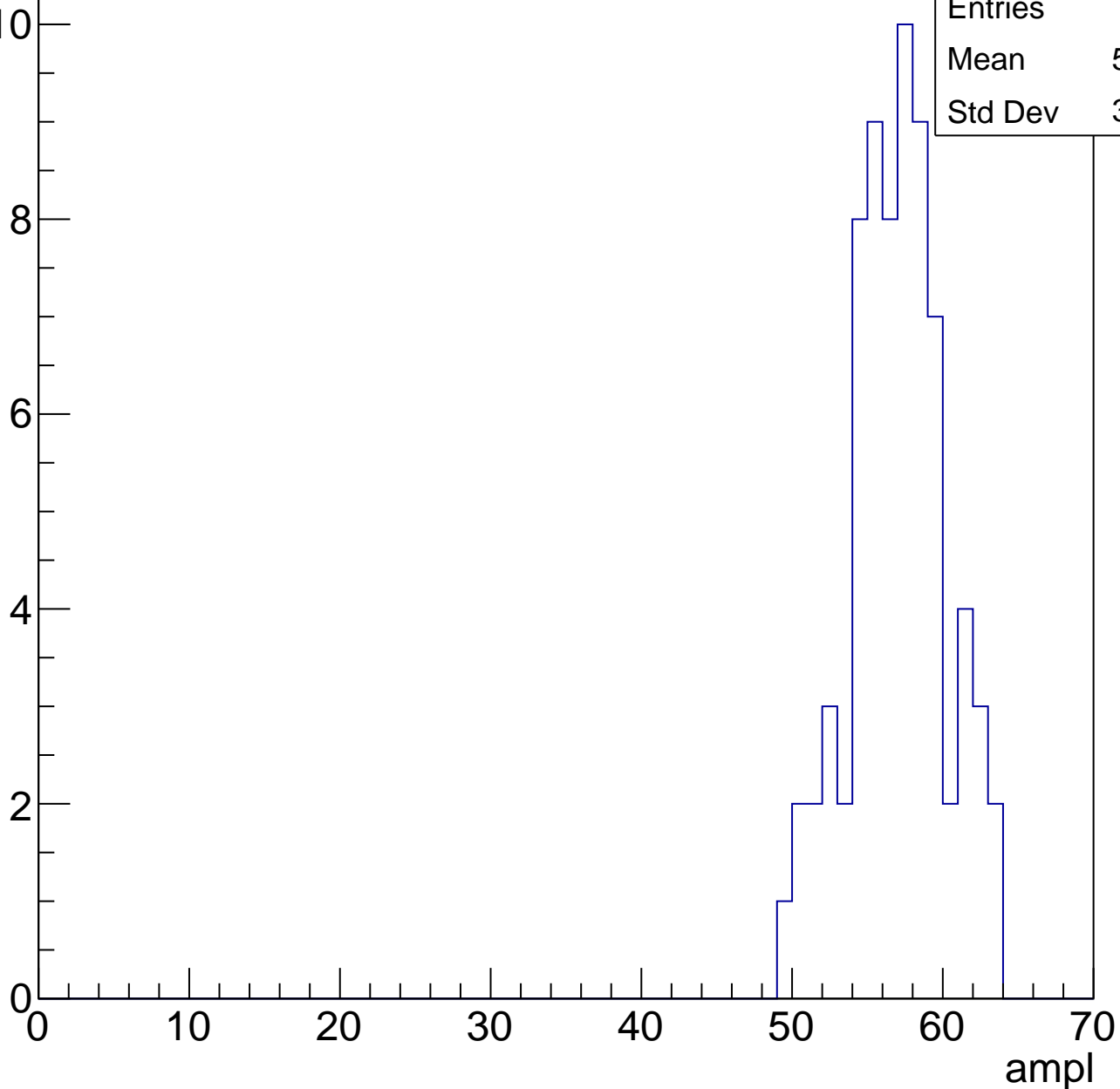


# B1L101S, U20-ch42, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

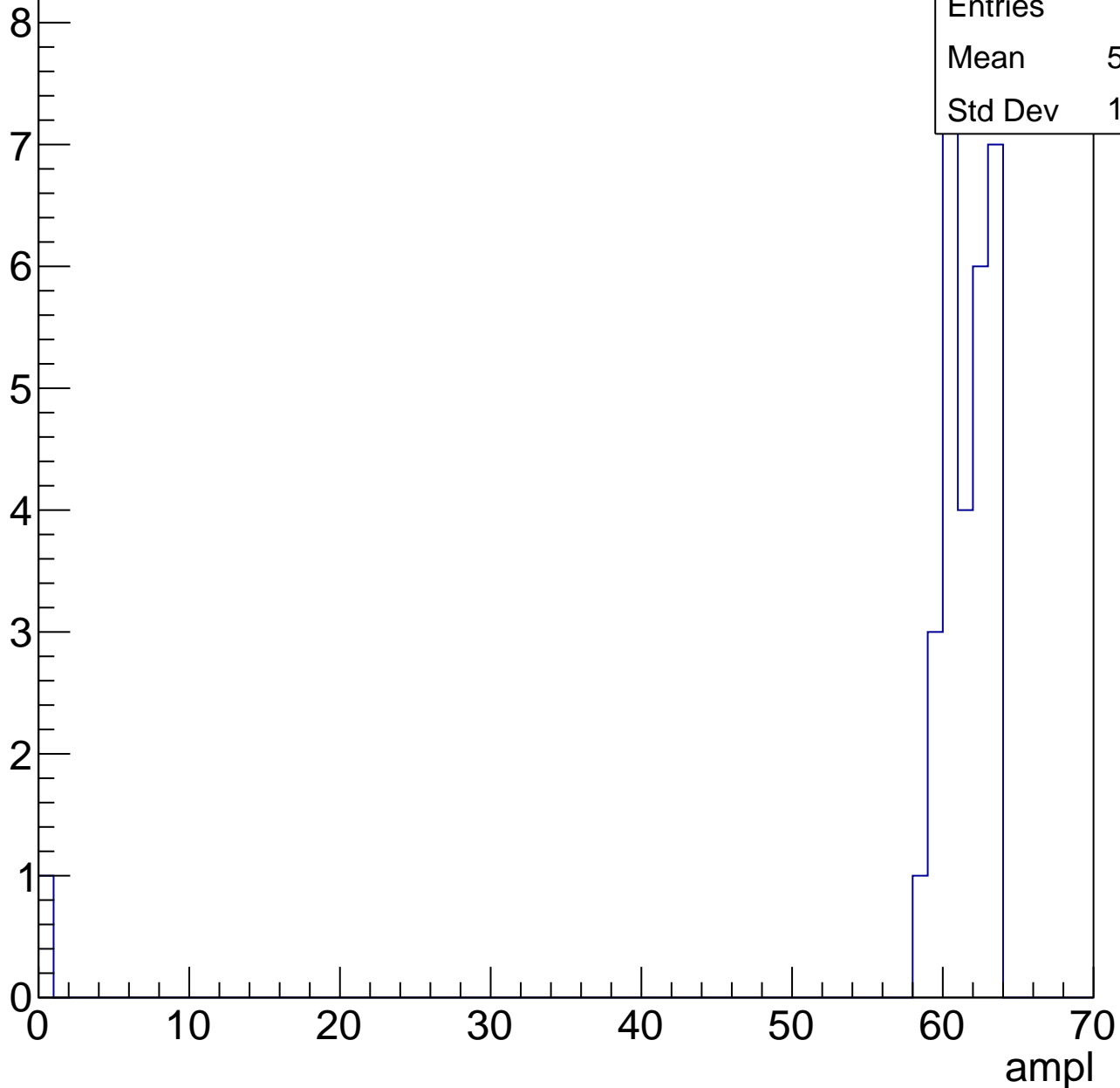
Entries	72
Mean	56.51
Std Dev	3.131



# B1L101S, U20-ch42, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U20-ch42, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U20-ch42, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U20-ch43, adc0

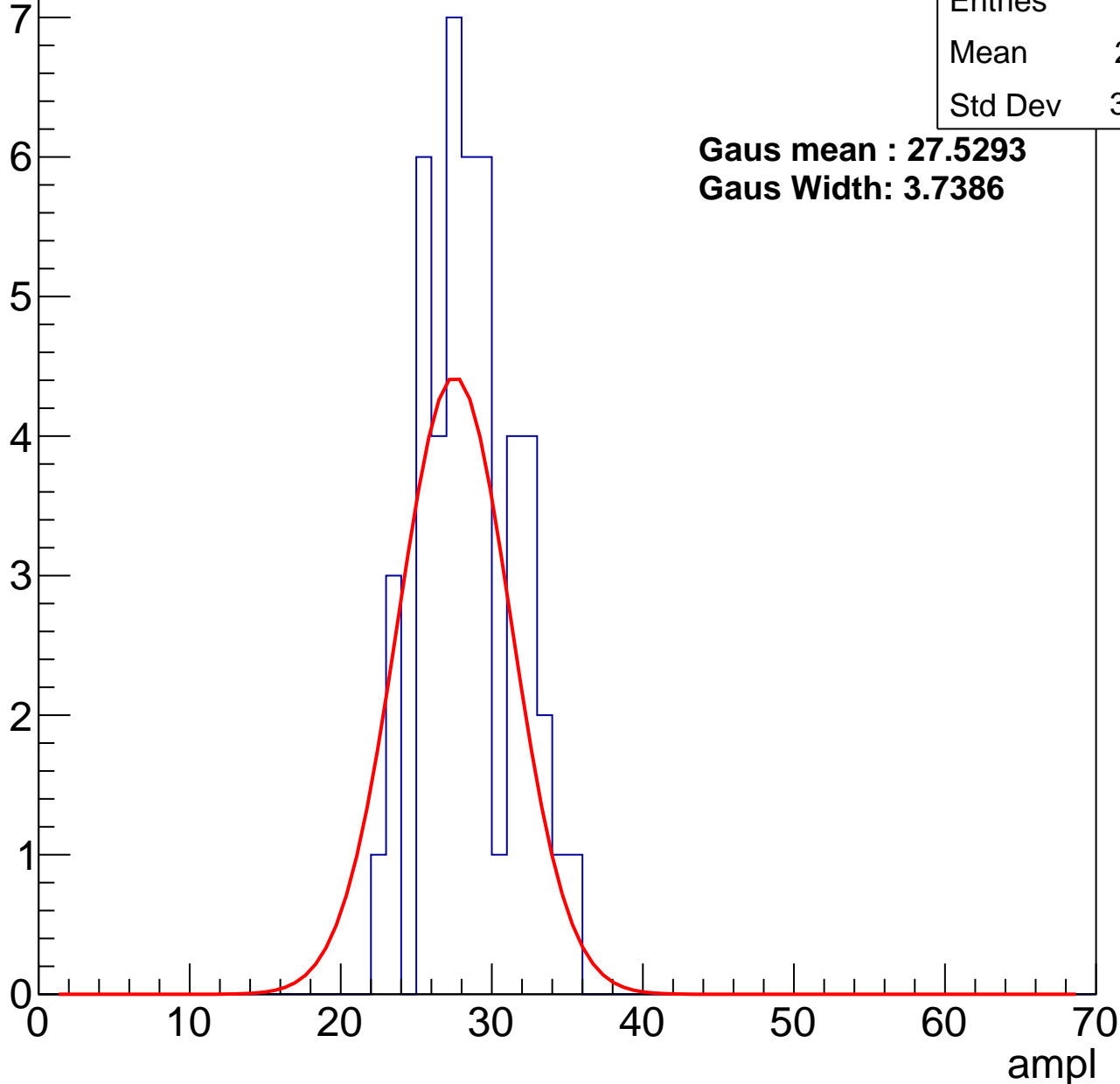
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	46
Mean	28.11
Std Dev	3.066

**Gaus mean : 27.5293**

**Gaus Width: 3.7386**



# B1L101S, U20-ch43, adc1

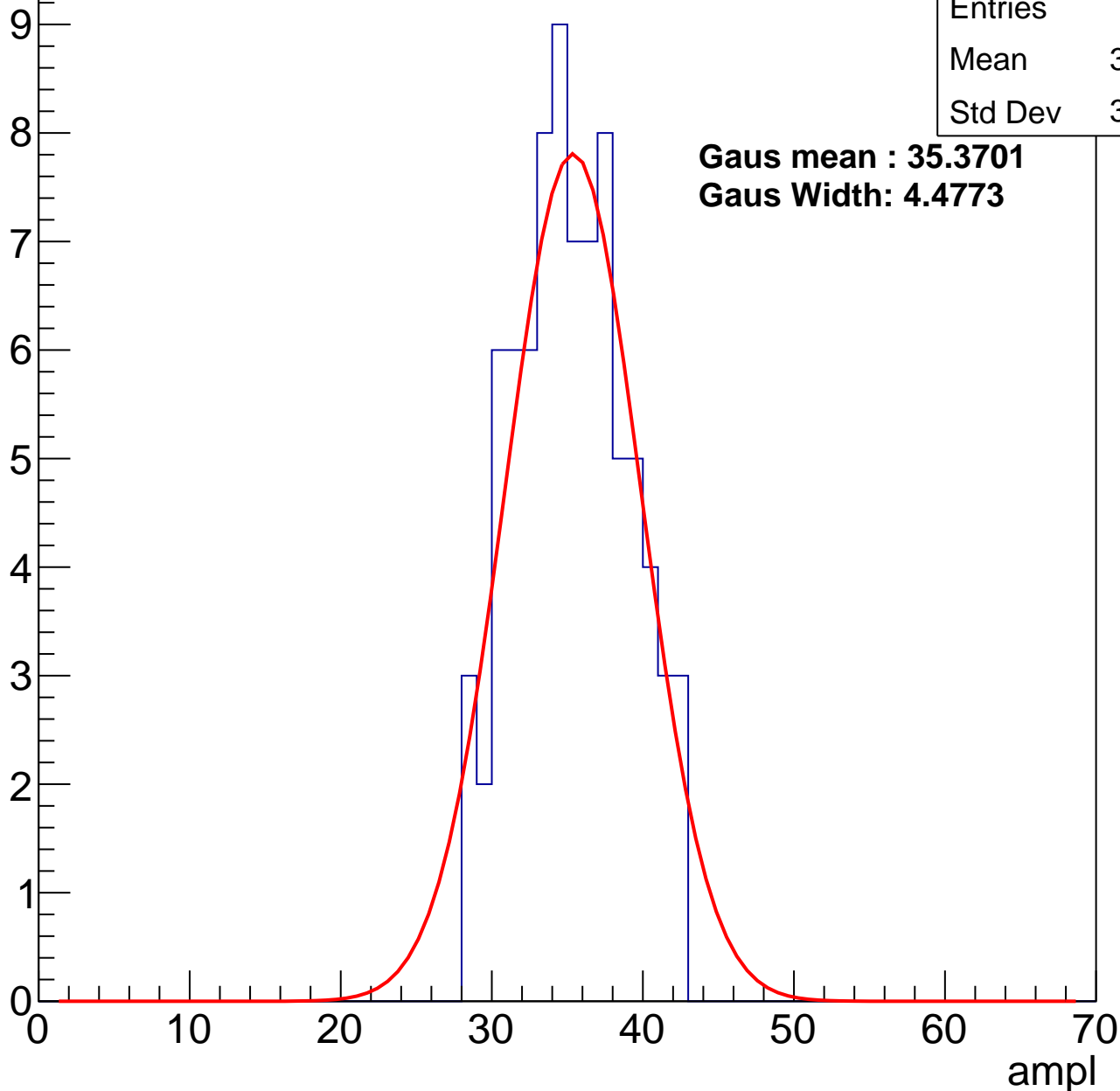
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	82
Mean	34.84
Std Dev	3.624

**Gaus mean : 35.3701**

**Gaus Width: 4.4773**



# B1L101S, U20-ch43, adc2

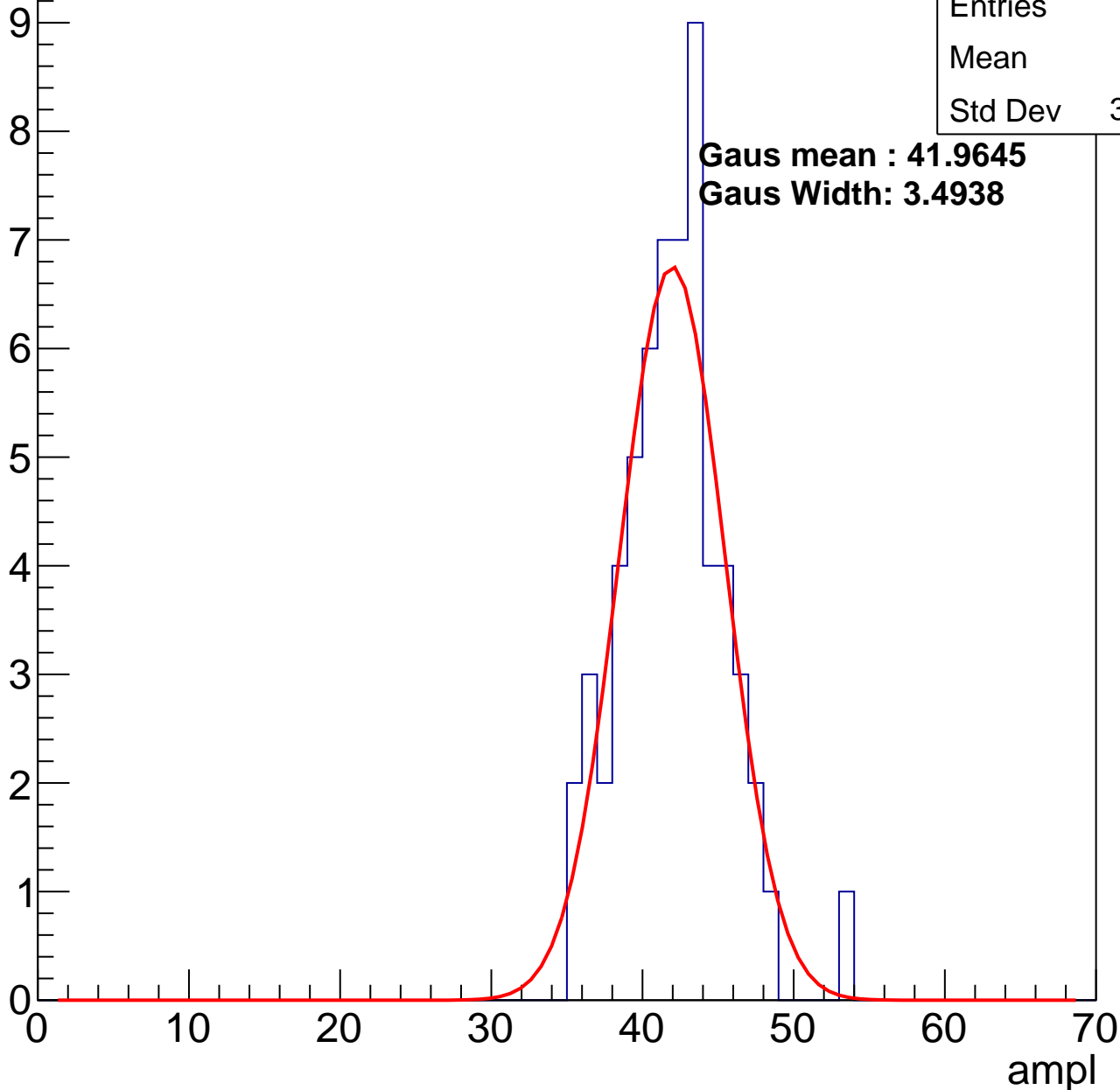
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	60
Mean	41.6
Std Dev	3.422

**Gaus mean : 41.9645**

**Gaus Width: 3.4938**

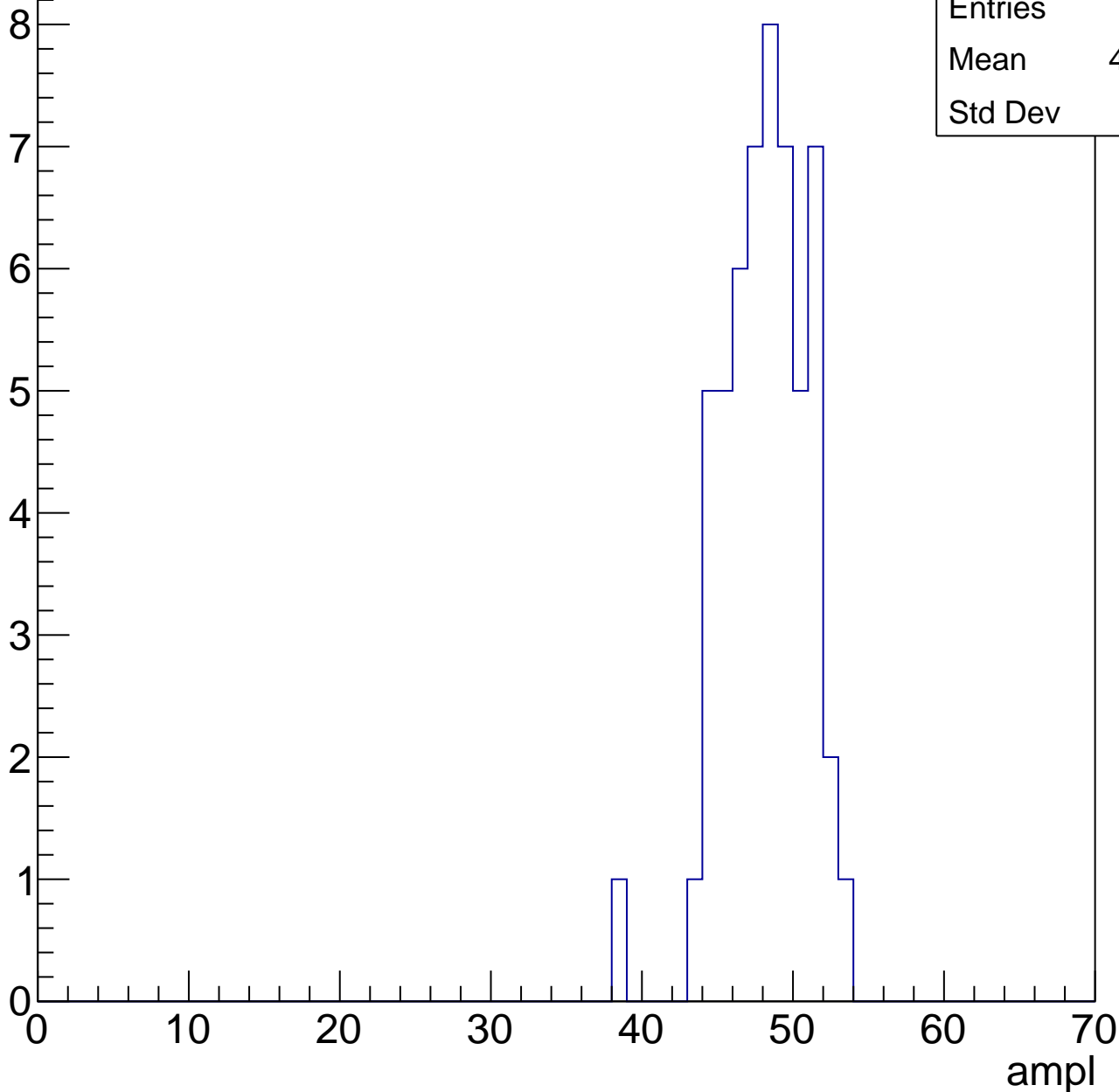


# B1L101S, U20-ch43, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

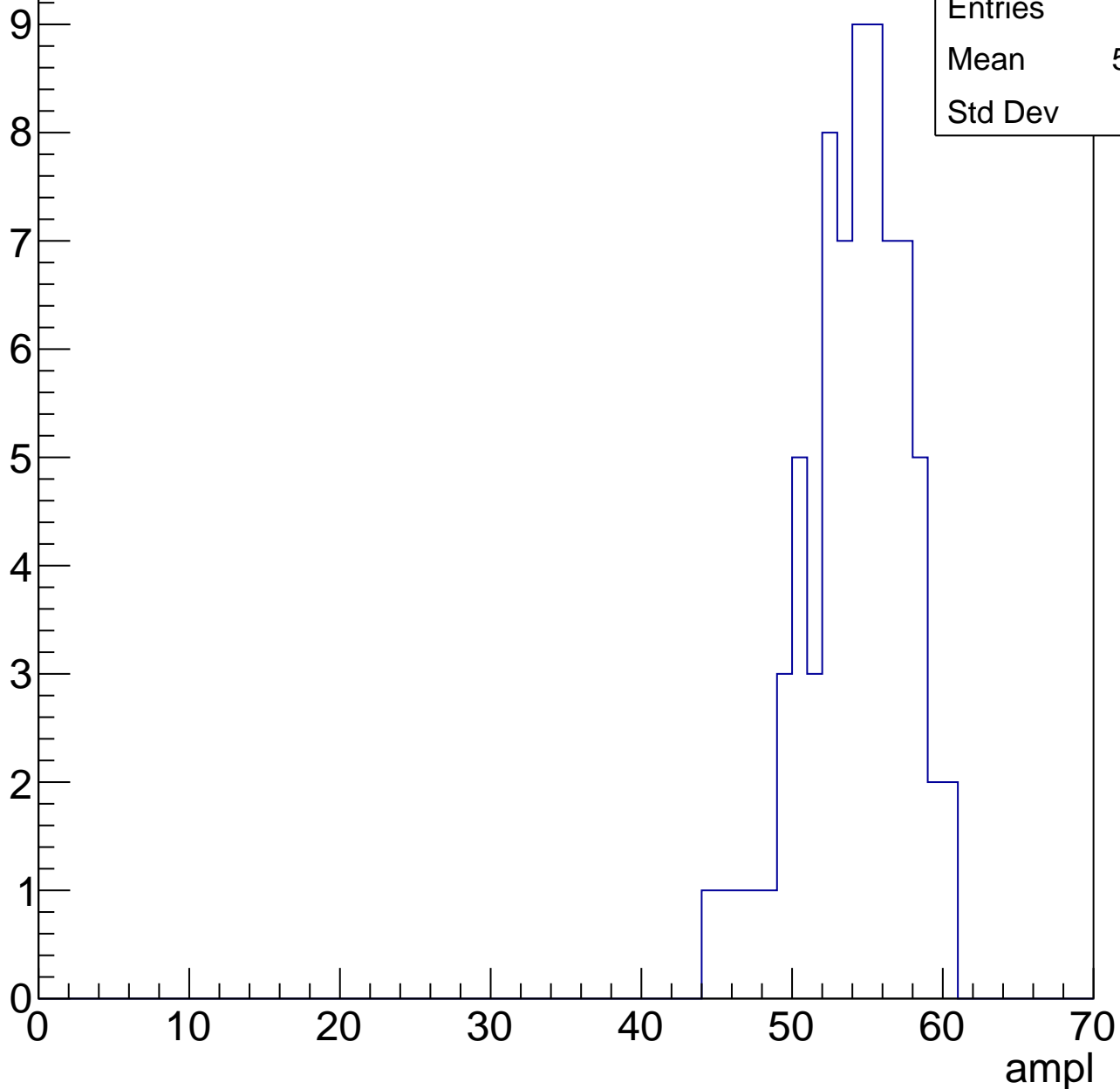
Entries	55
Mean	47.67
Std Dev	2.77



# B1L101S, U20-ch43, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

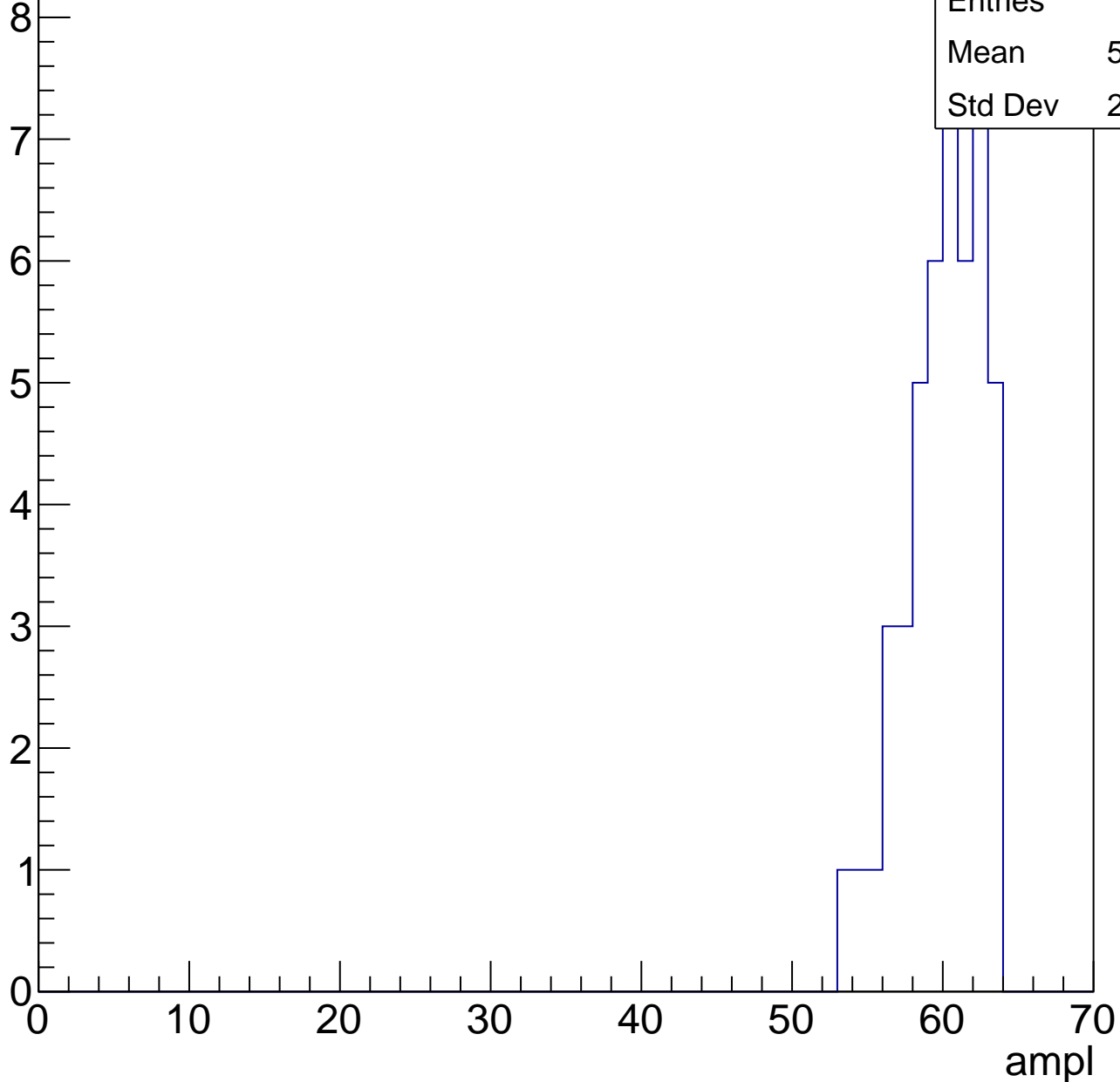


Entries	72
Mean	53.71
Std Dev	3.43

# B1L101S, U20-ch43, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

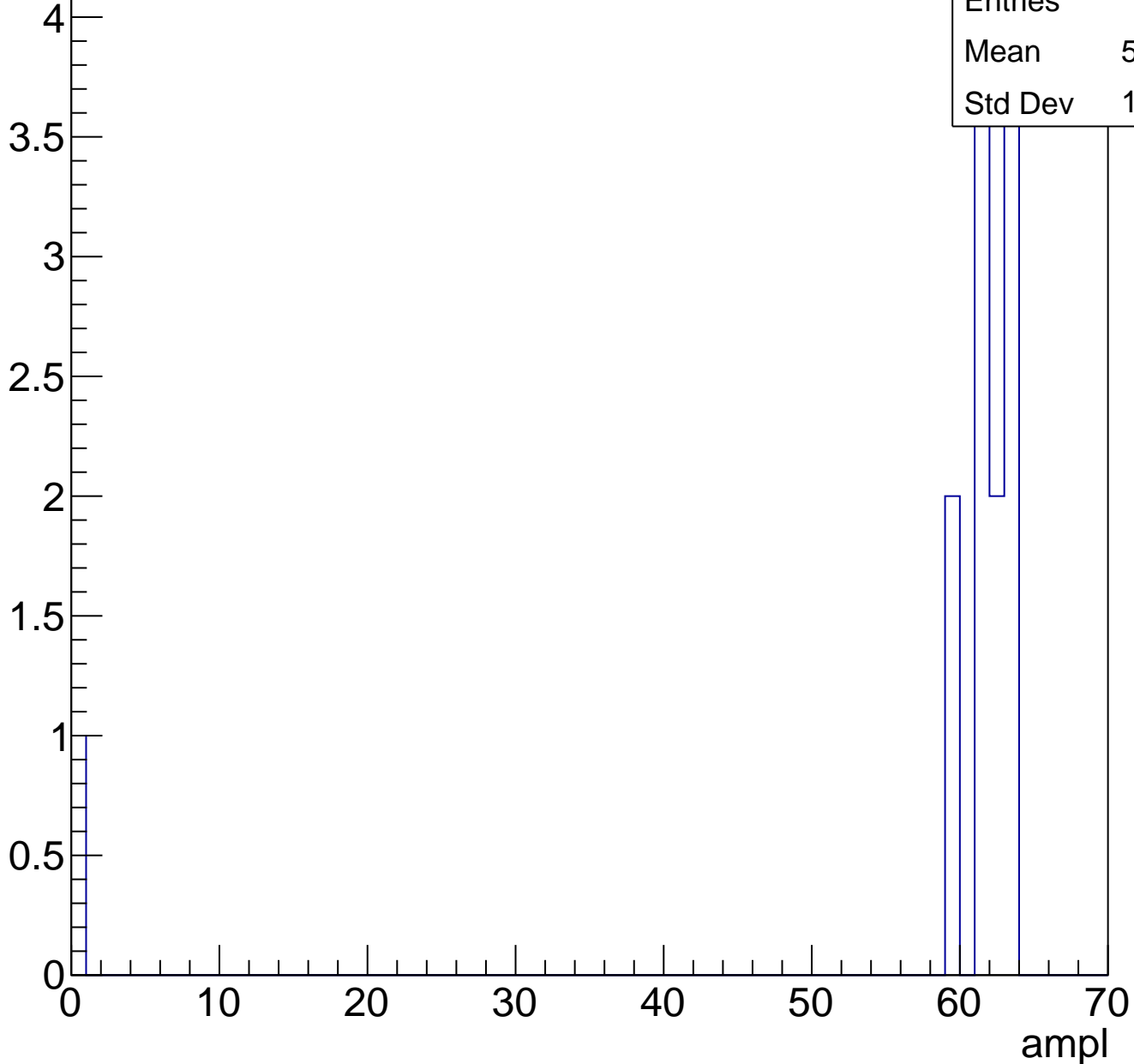
Entry



# B1L101S, U20-ch43, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U20-ch43, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U20-ch44, adc0

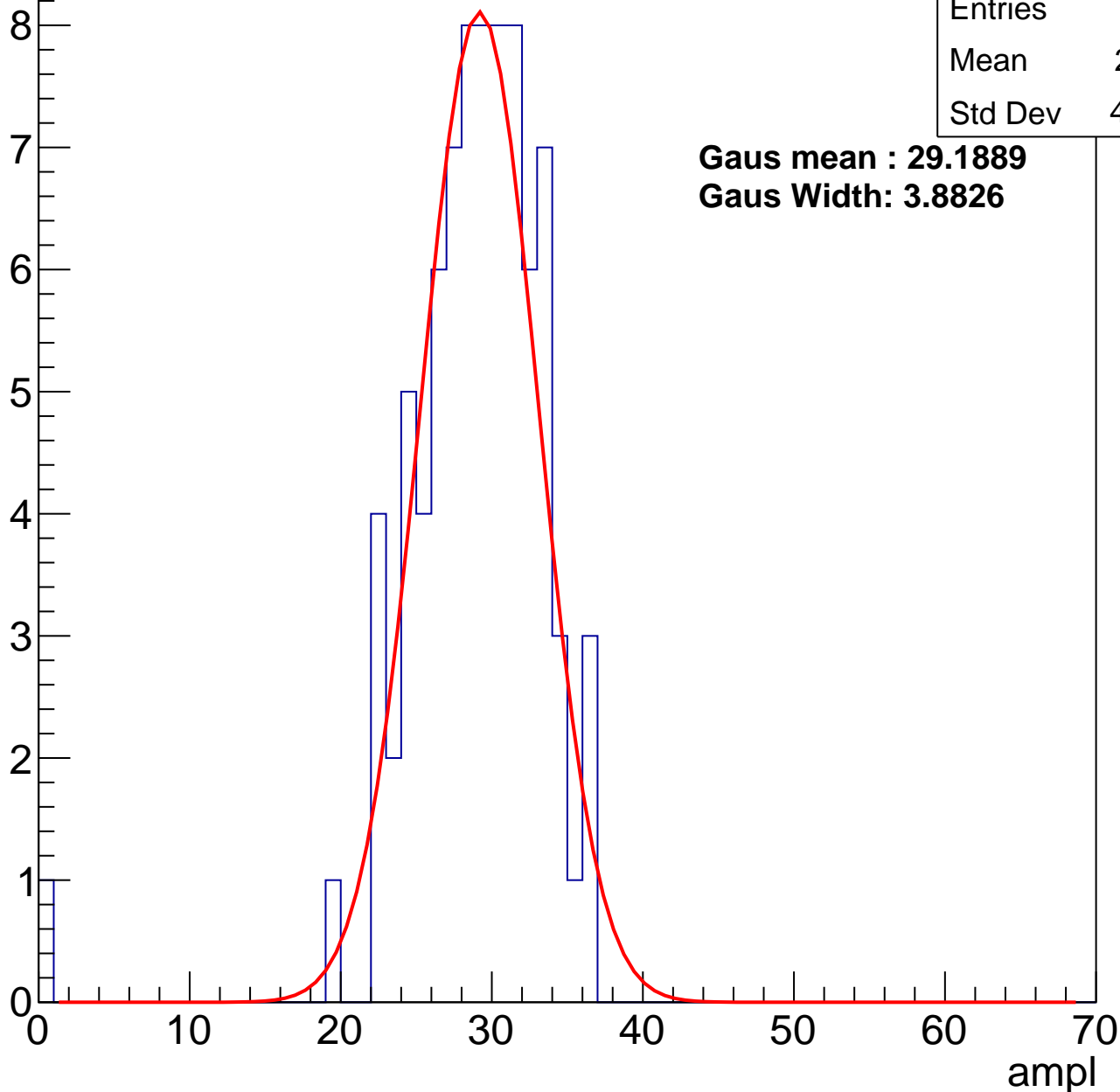
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	82
Mean	28.41
Std Dev	4.844

**Gaus mean : 29.1889**

**Gaus Width: 3.8826**



# B1L101S, U20-ch44, adc1

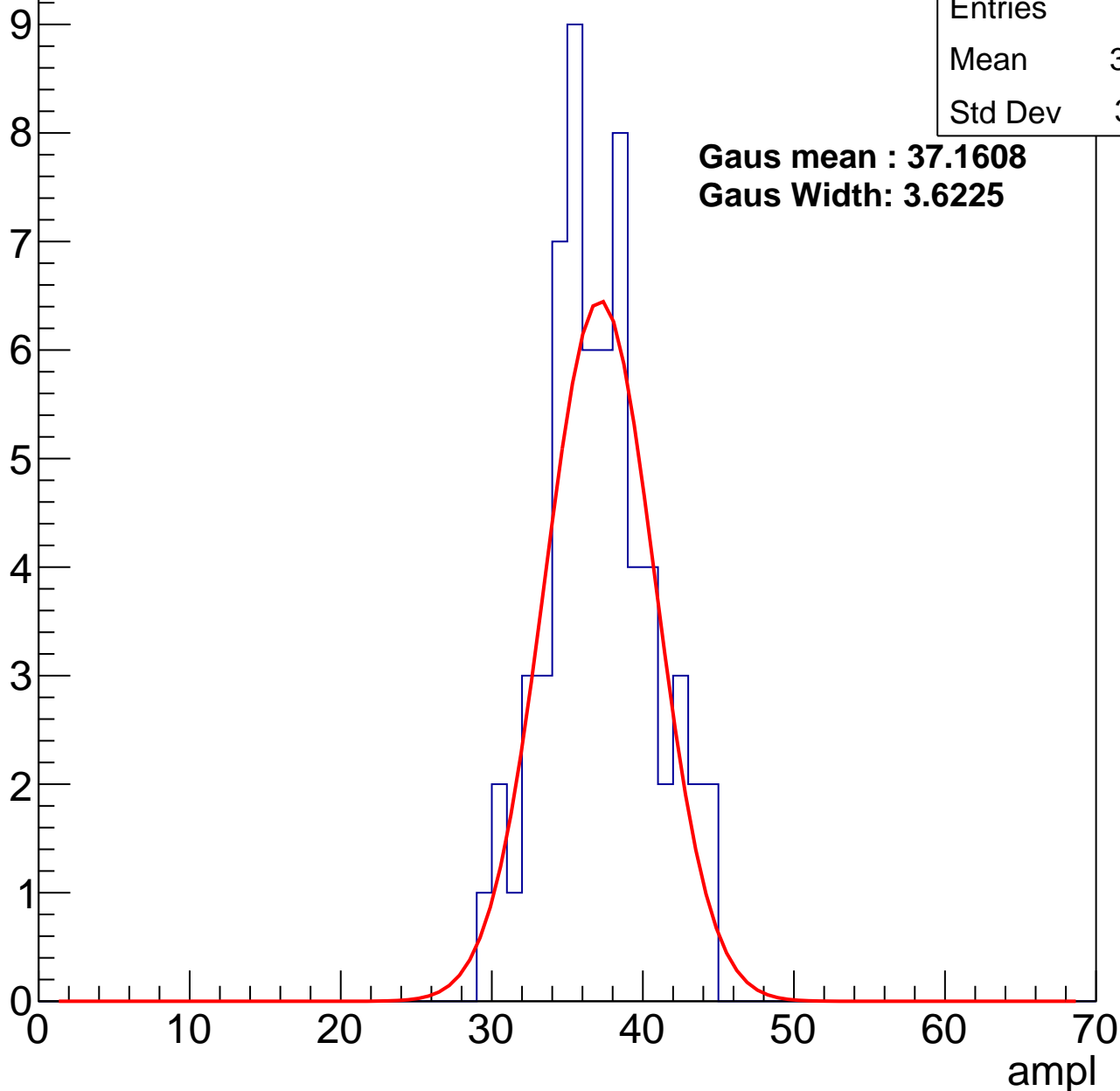
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	36.63
Std Dev	3.461

**Gaus mean : 37.1608**

**Gaus Width: 3.6225**



# B1L101S, U20-ch44, adc2

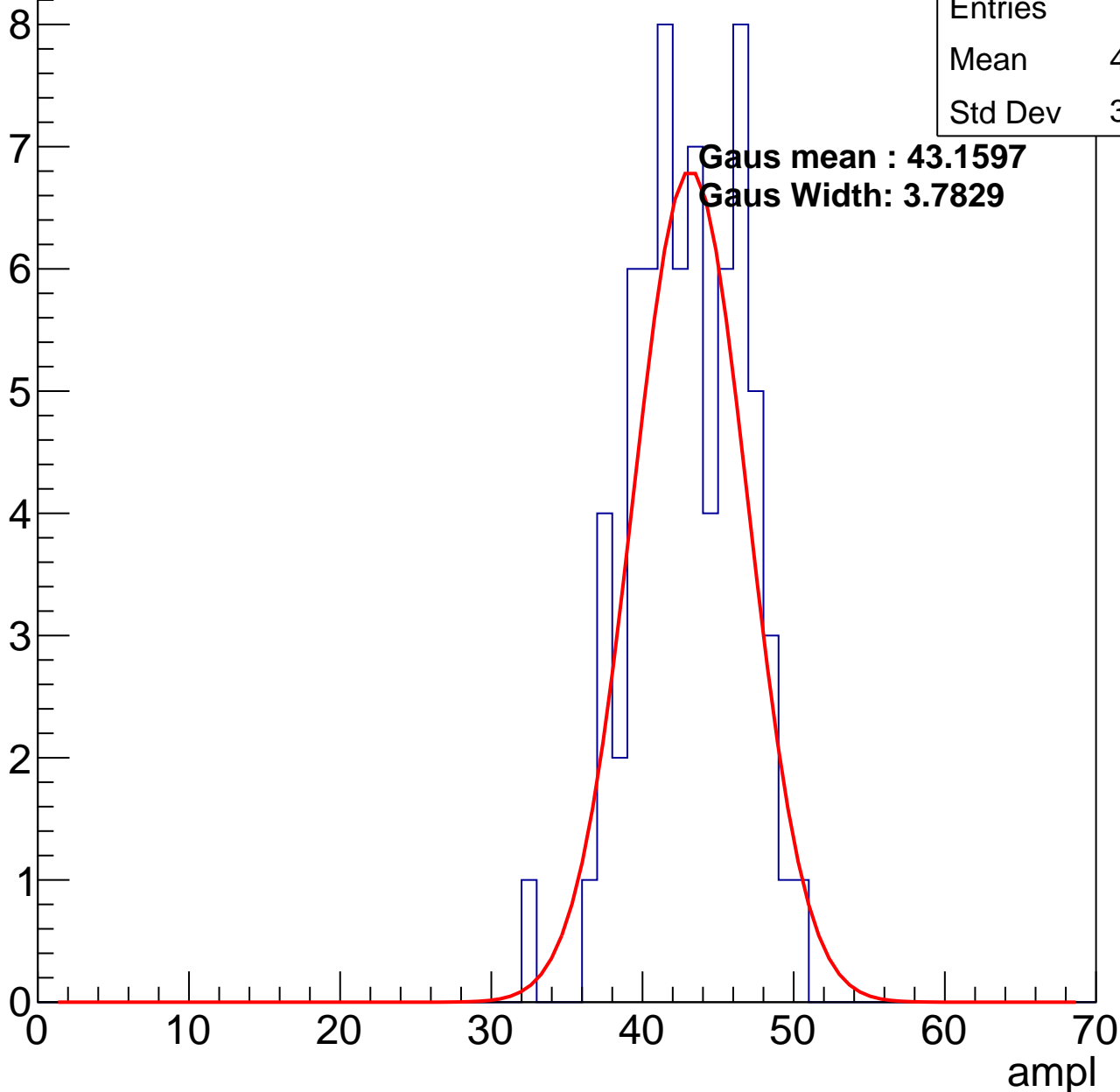
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	42.59
Std Dev	3.573

**Gaus mean : 43.1597**

**Gaus Width: 3.7829**

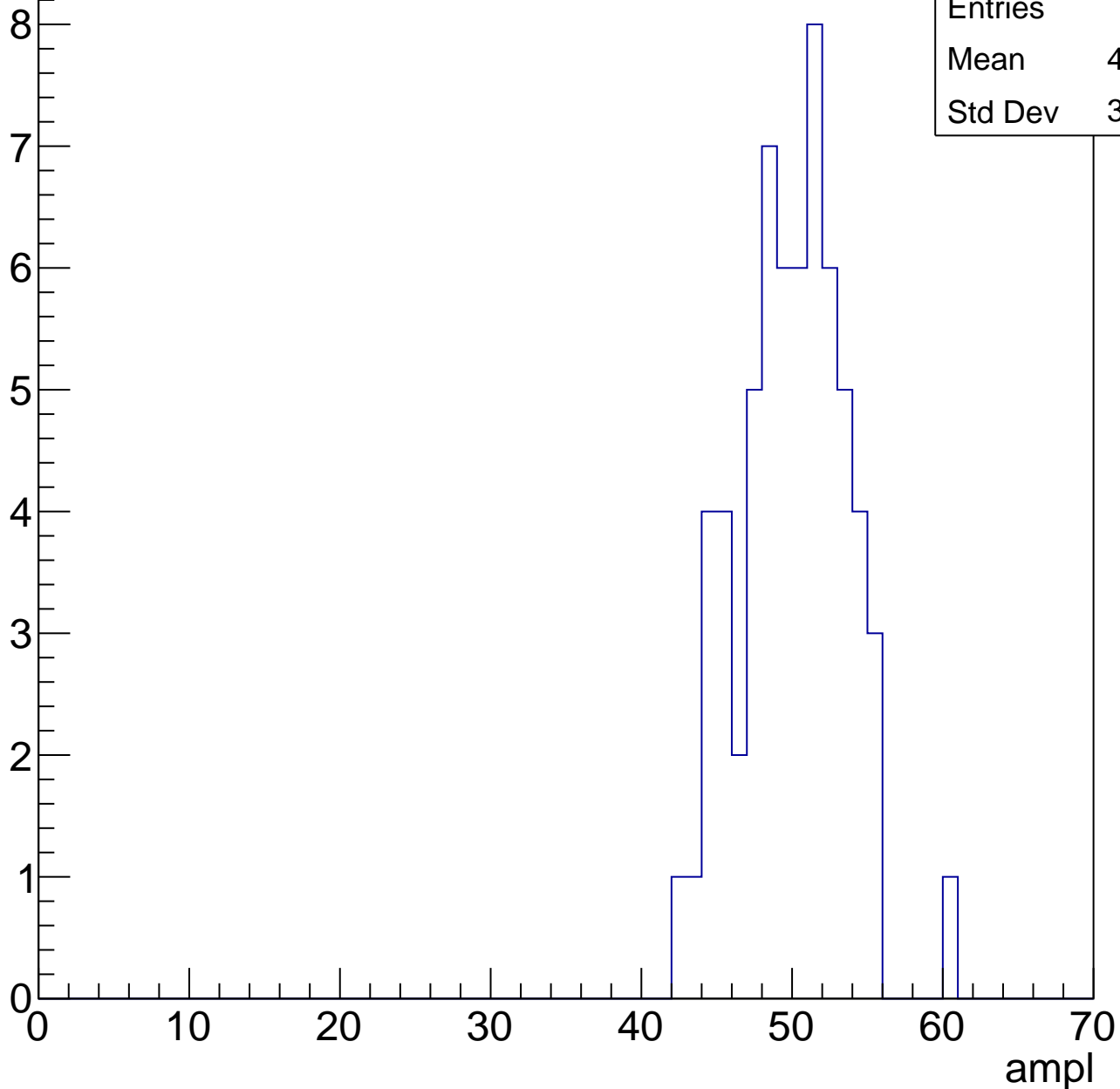


# B1L101S, U20-ch44, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	49.59
Std Dev	3.503

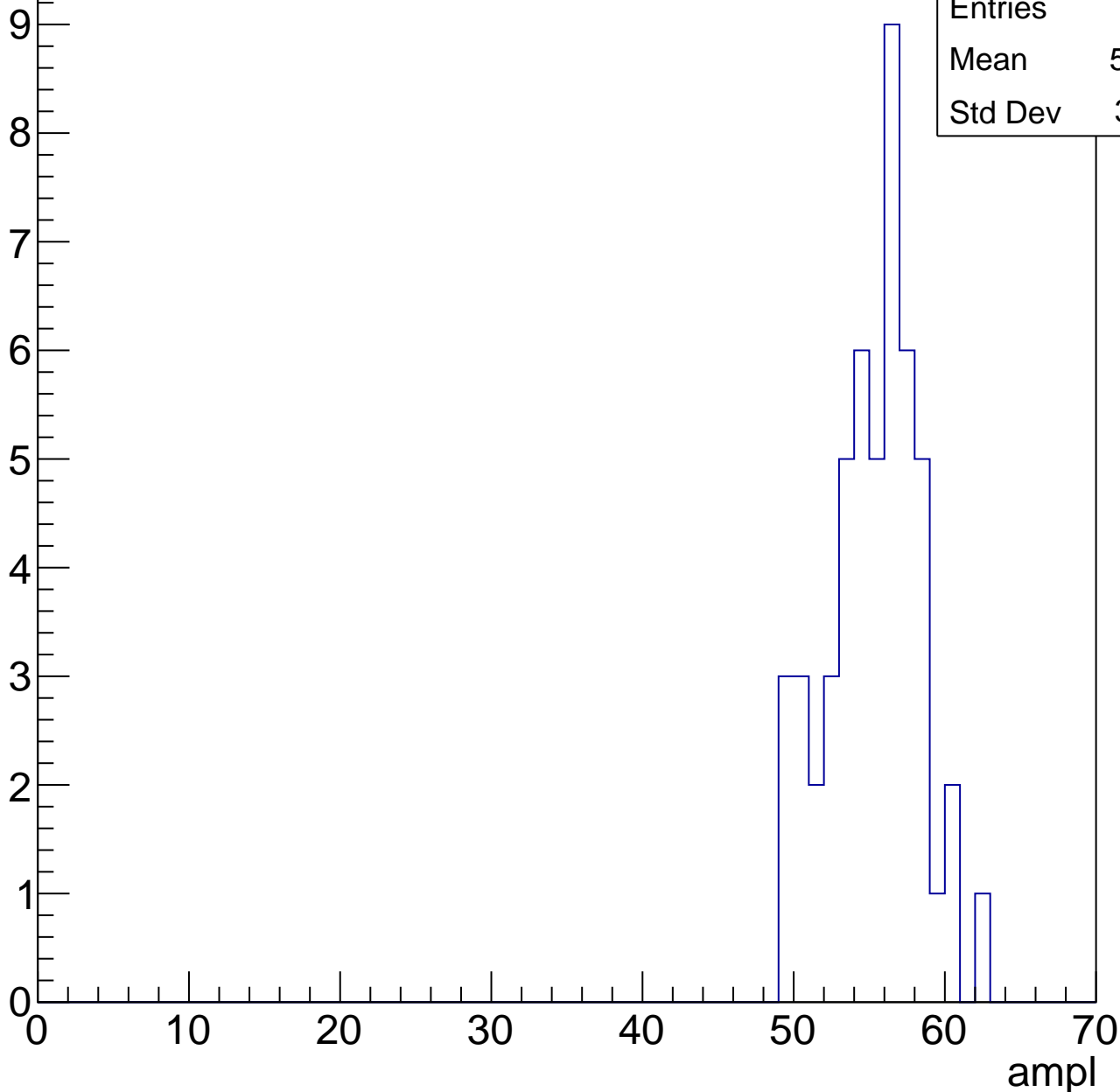


# B1L101S, U20-ch44, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

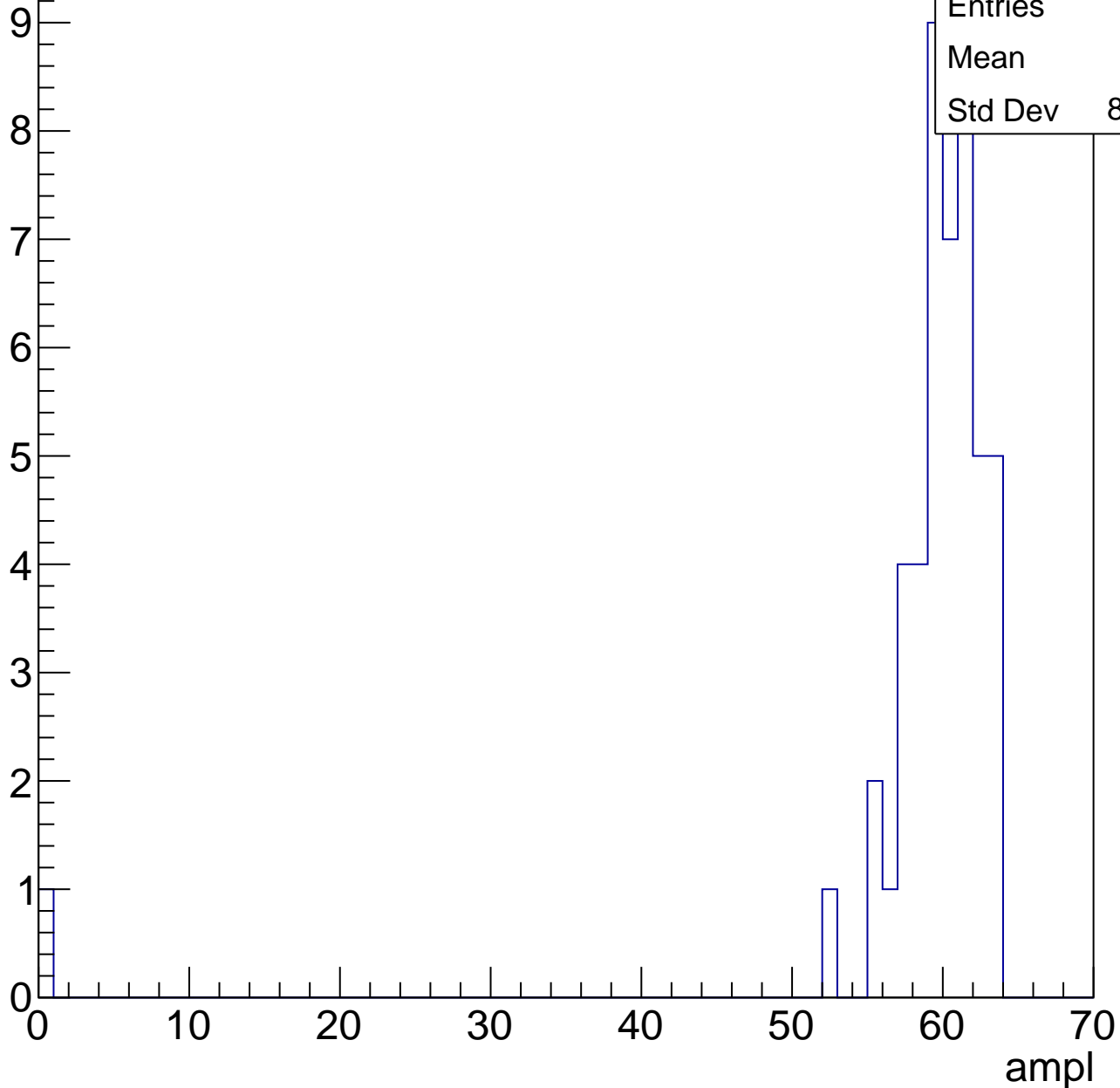
Entries	51
Mean	54.82
Std Dev	3.001



# B1L101S, U20-ch44, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

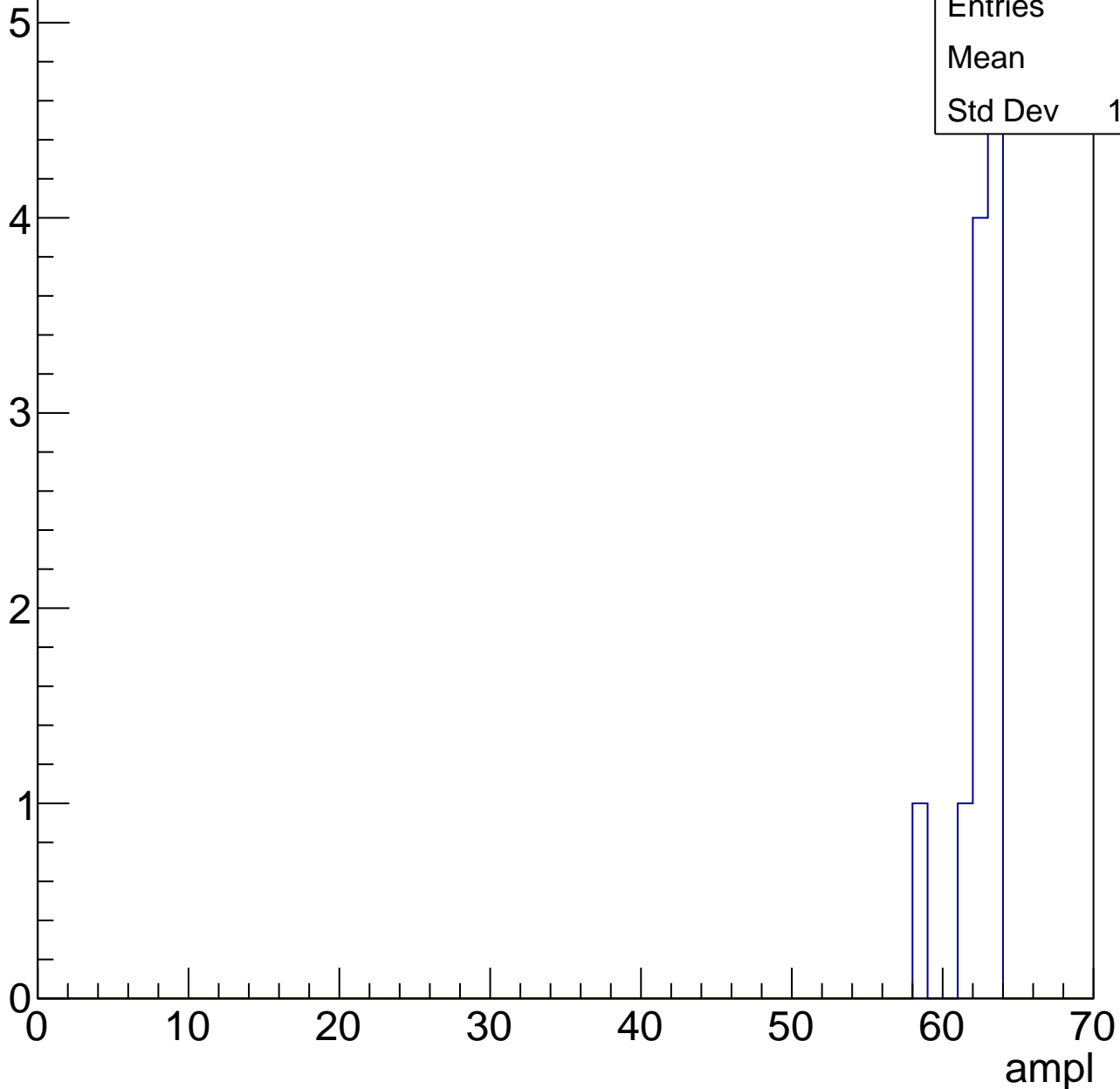


# B1L101S, U20-ch44, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	11
Mean	62
Std Dev	1.414





# B1L101S, U20-ch44, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U20-ch45, adc0

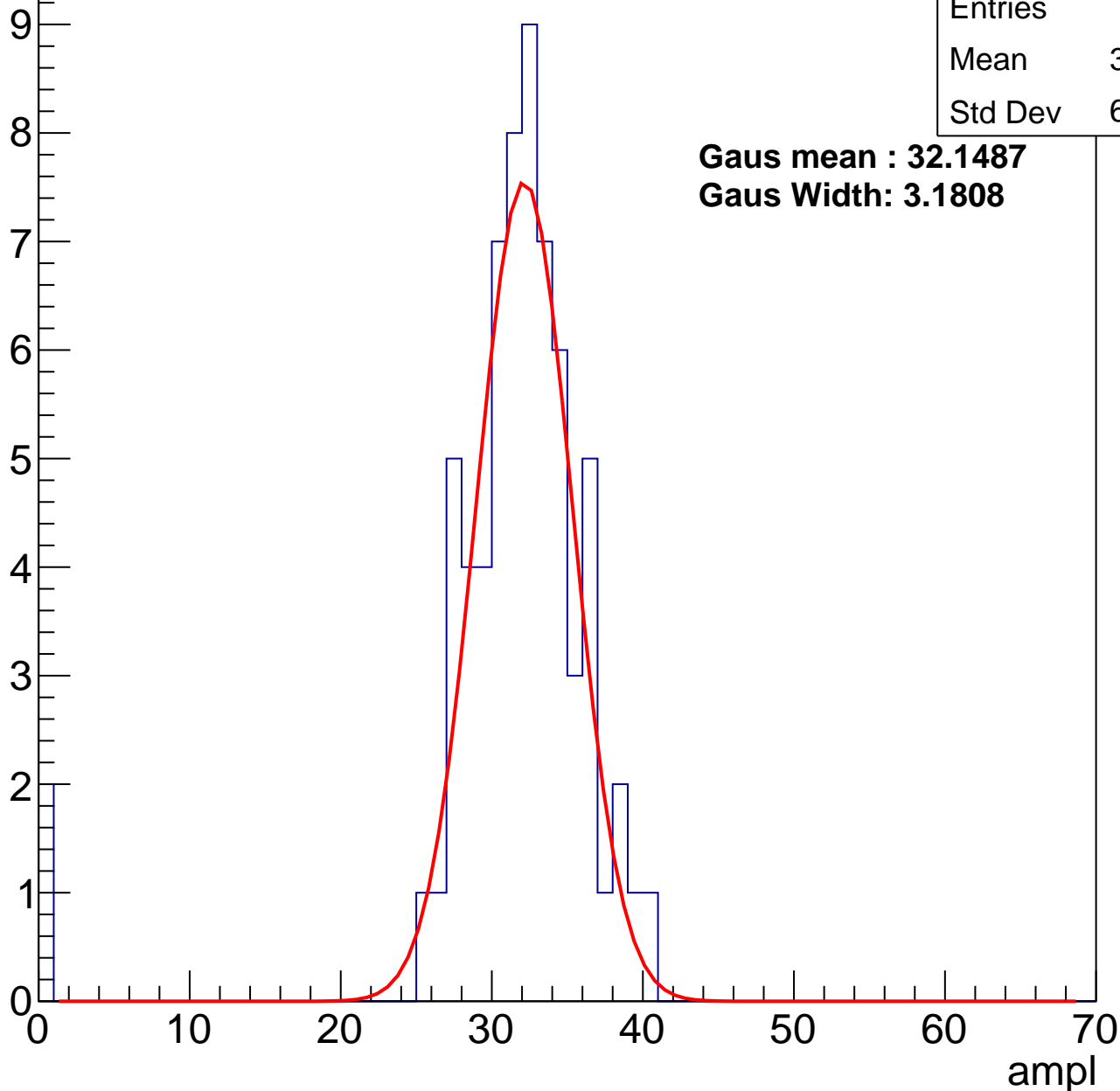
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	67
Mean	30.93
Std Dev	6.306

**Gaus mean : 32.1487**

**Gaus Width: 3.1808**



# B1L101S, U20-ch45, adc1

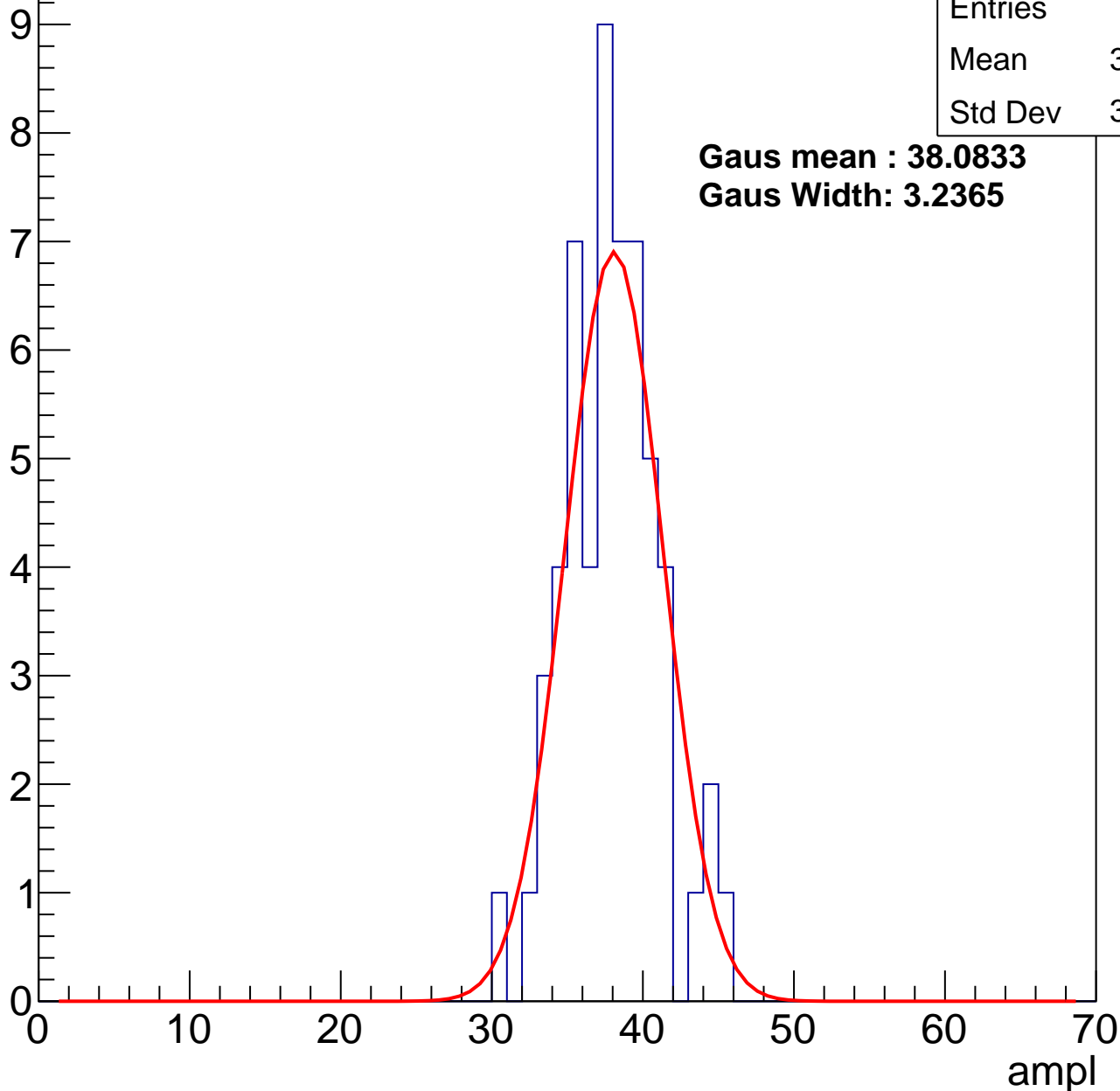
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	56
Mean	37.46
Std Dev	3.047

**Gaus mean : 38.0833**

**Gaus Width: 3.2365**



# B1L101S, U20-ch45, adc2

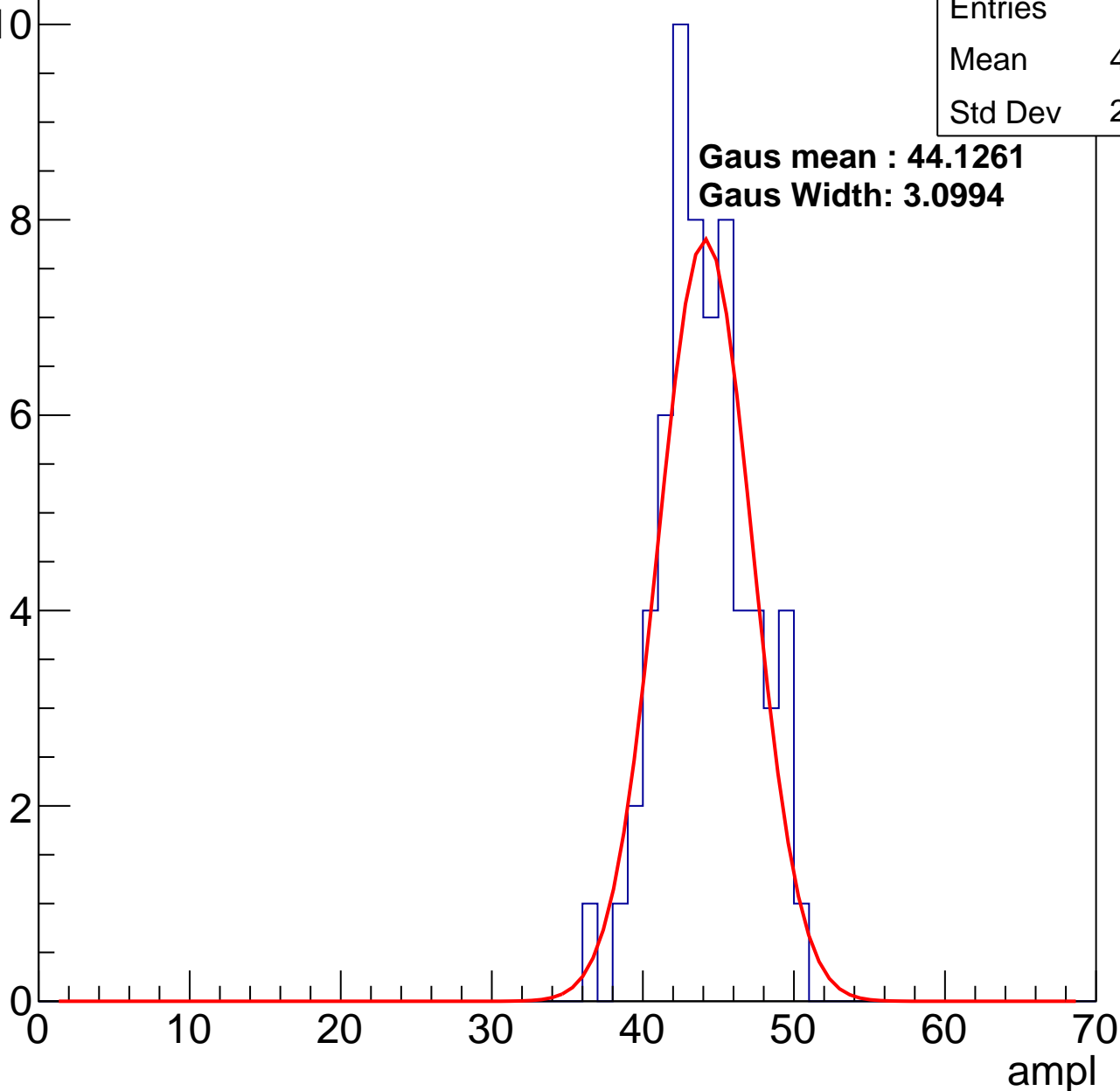
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	43.68
Std Dev	2.964

**Gaus mean : 44.1261**

**Gaus Width: 3.0994**

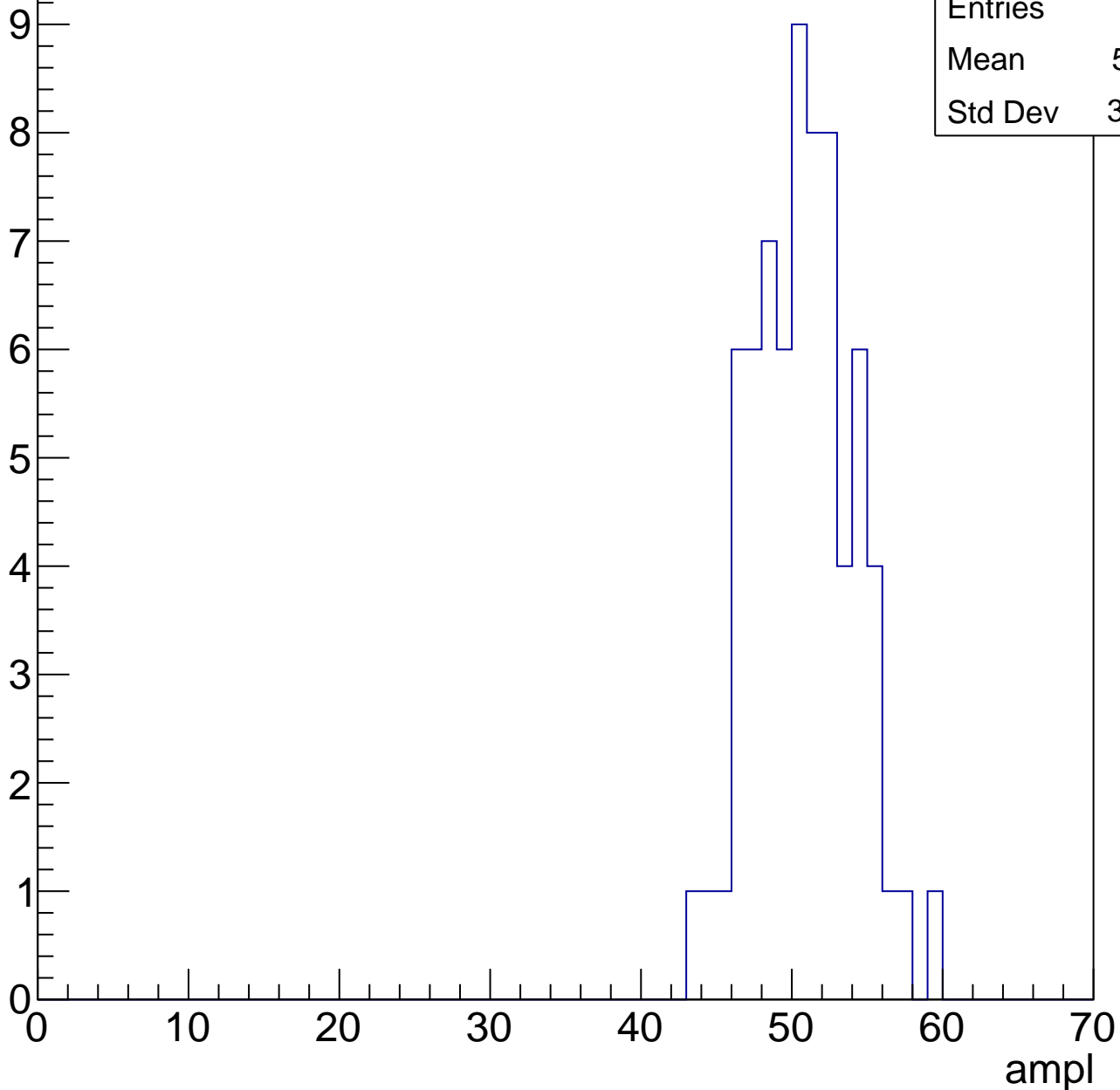


# B1L101S, U20-ch45, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

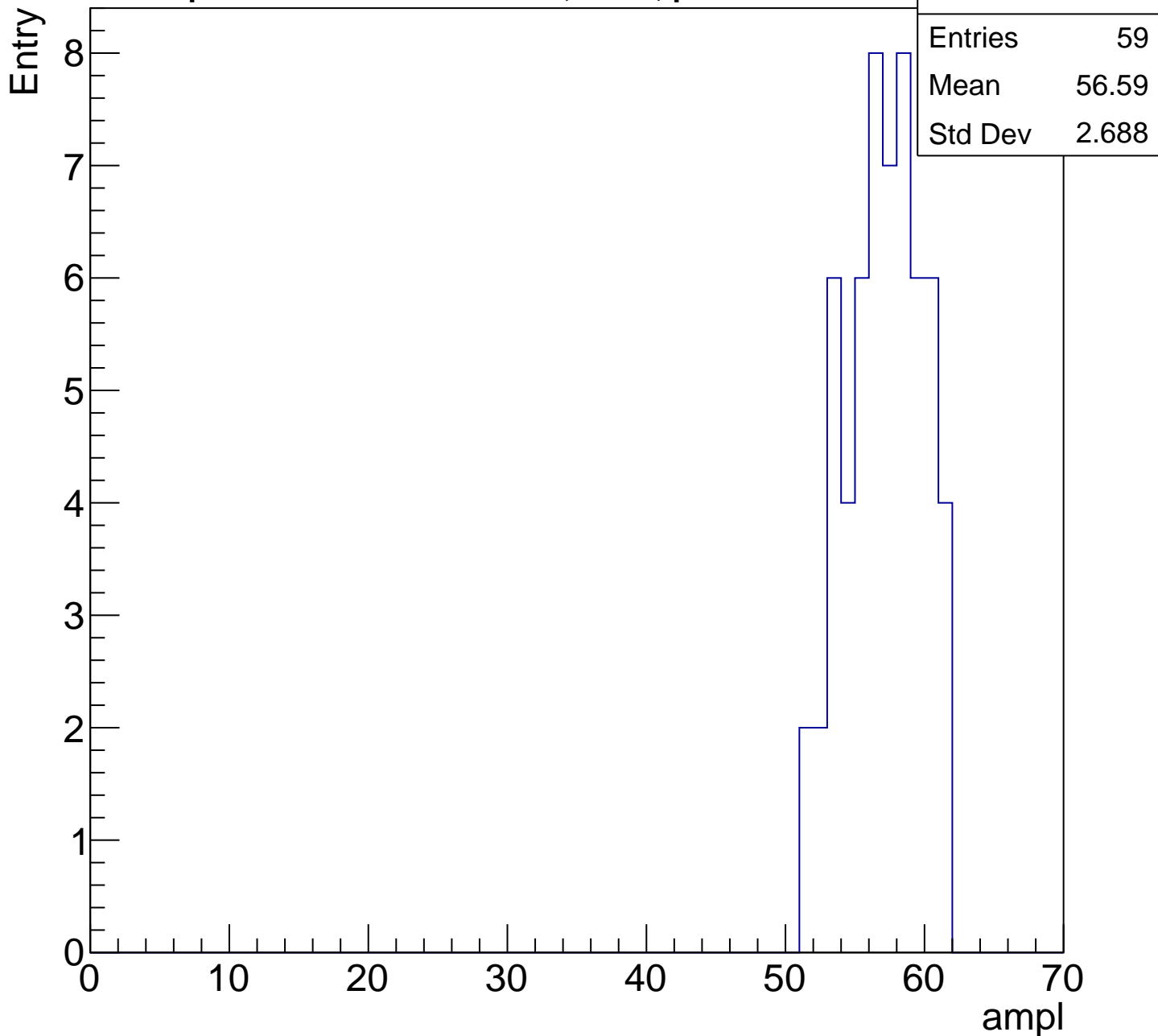
Entry

Entries	70
Mean	50.31
Std Dev	3.218



# B1L101S, U20-ch45, adc4

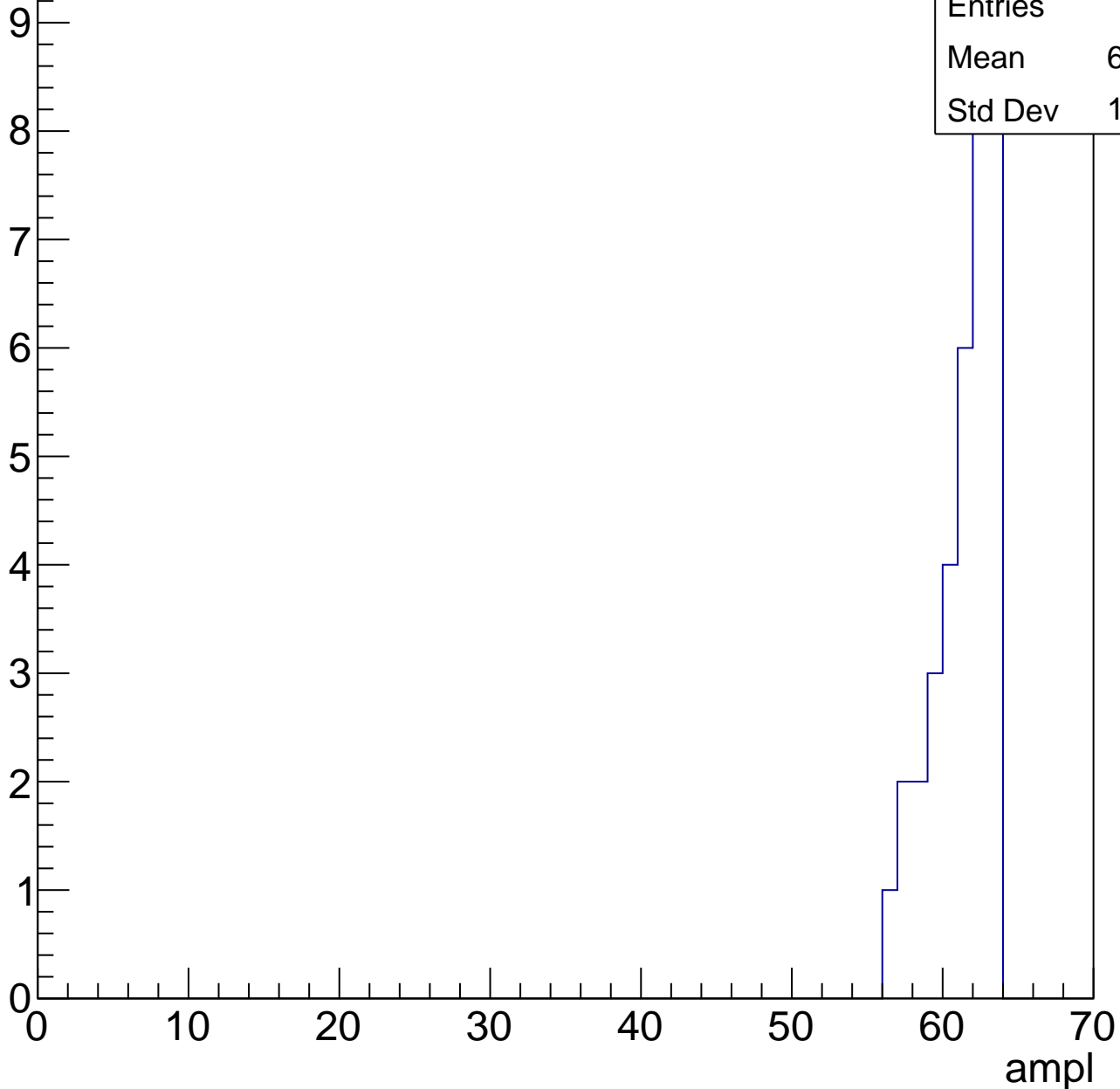
calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U20-ch45, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U20-ch45, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U20-ch45, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U20-ch46, adc0

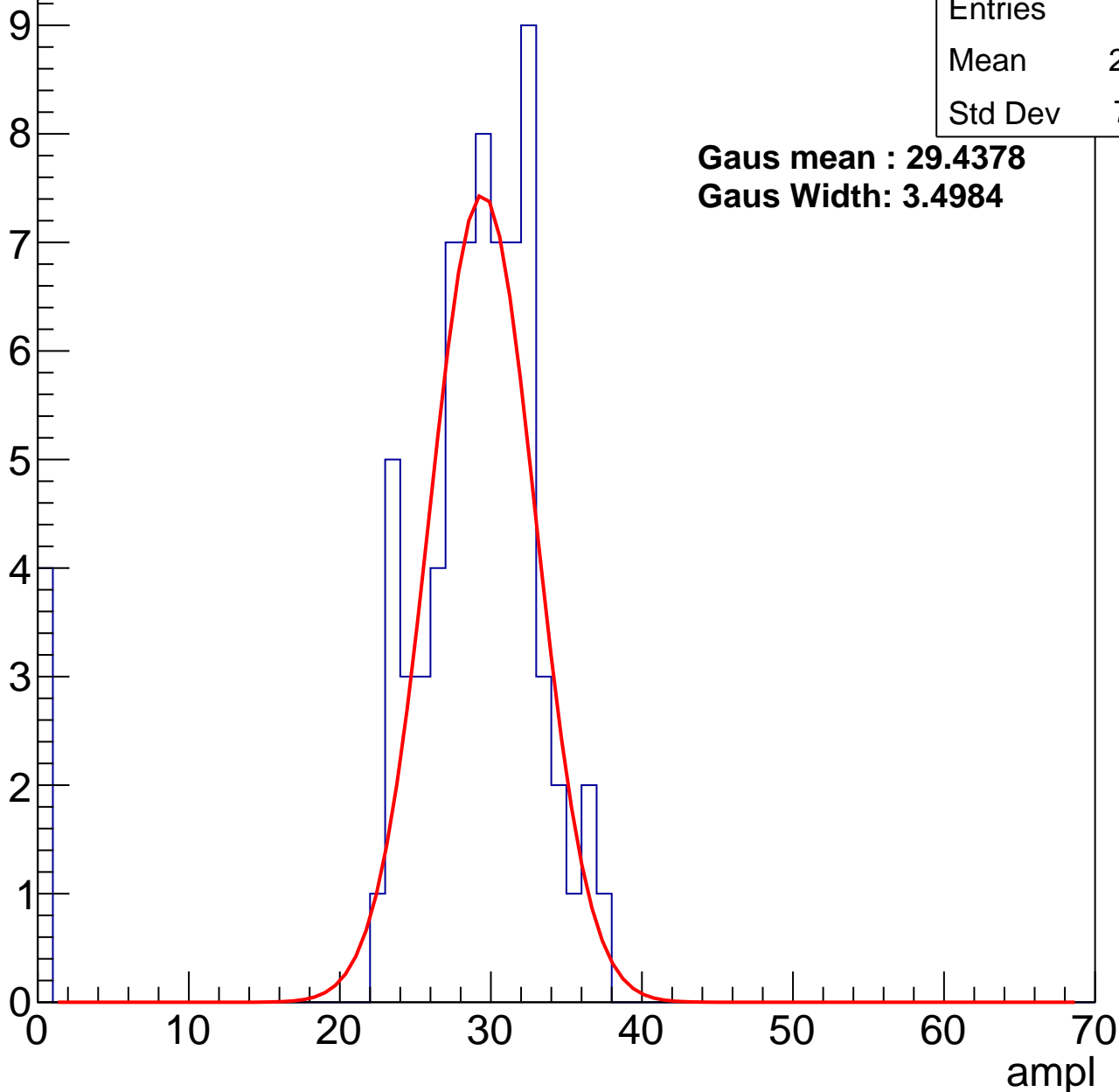
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	74
Mean	27.45
Std Dev	7.371

**Gaus mean : 29.4378**

**Gaus Width: 3.4984**



# B1L101S, U20-ch46, adc1

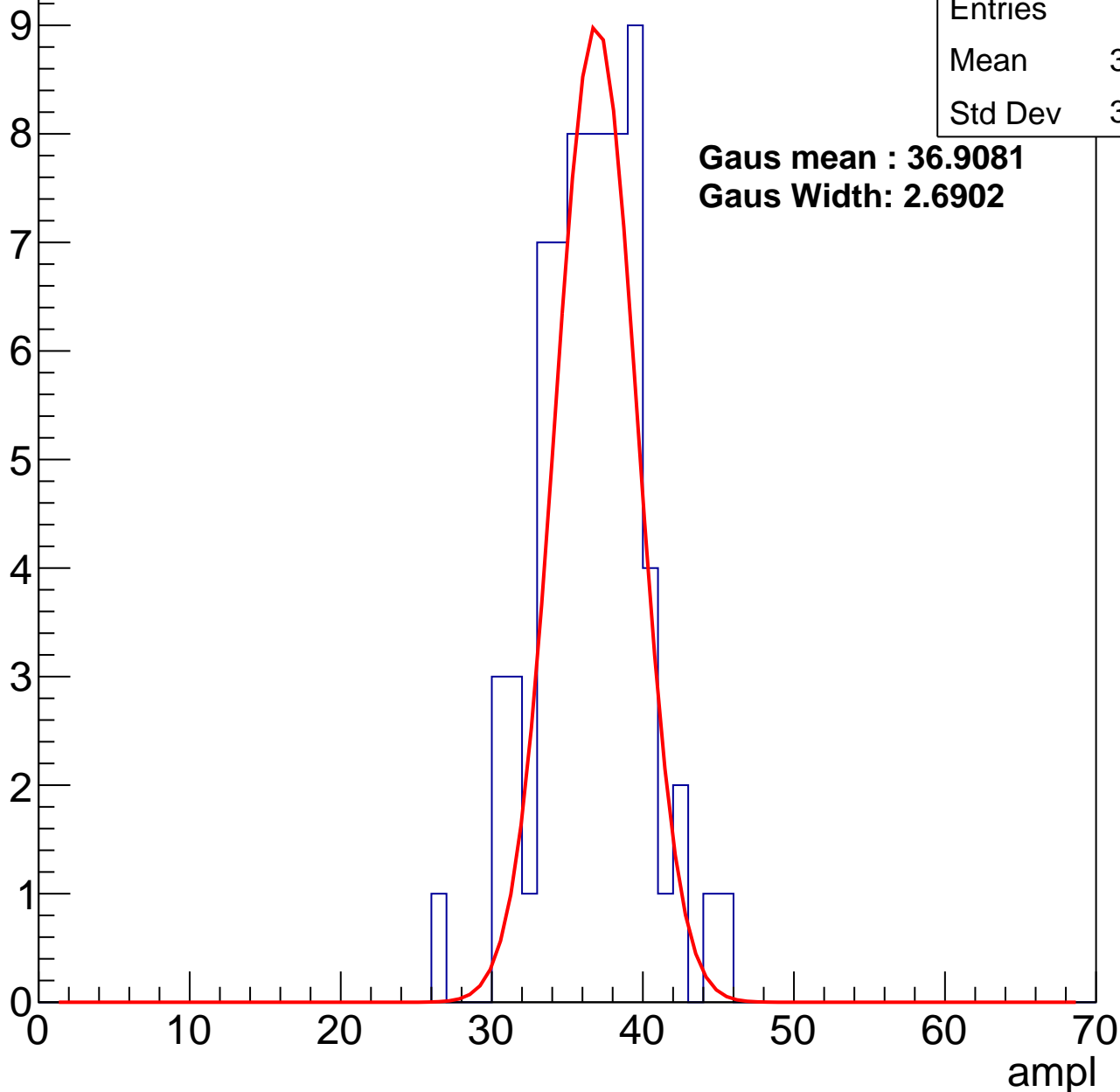
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	72
Mean	36.15
Std Dev	3.382

**Gaus mean : 36.9081**

**Gaus Width: 2.6902**



# B1L101S, U20-ch46, adc2

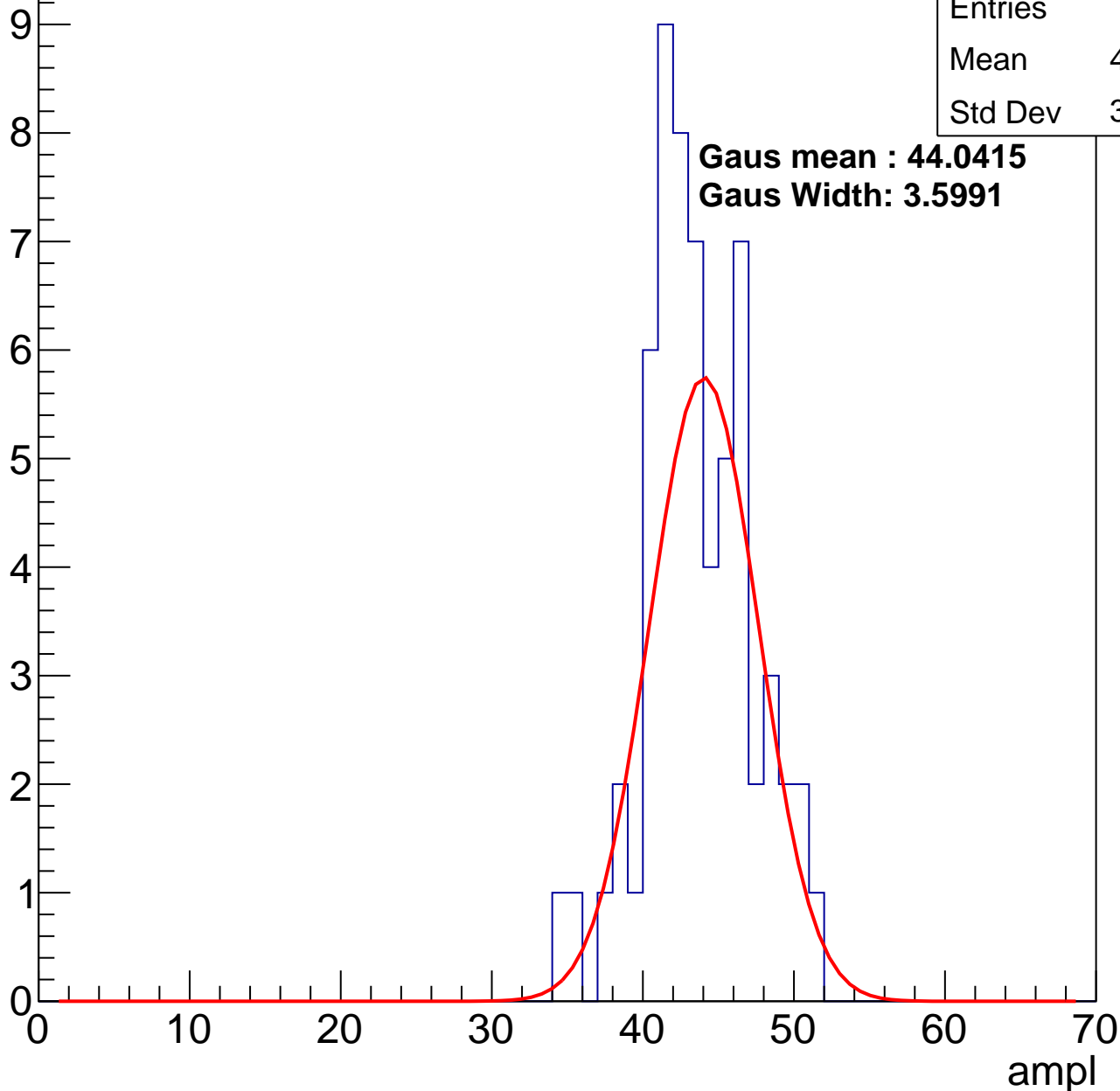
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	43.18
Std Dev	3.527

**Gaus mean : 44.0415**

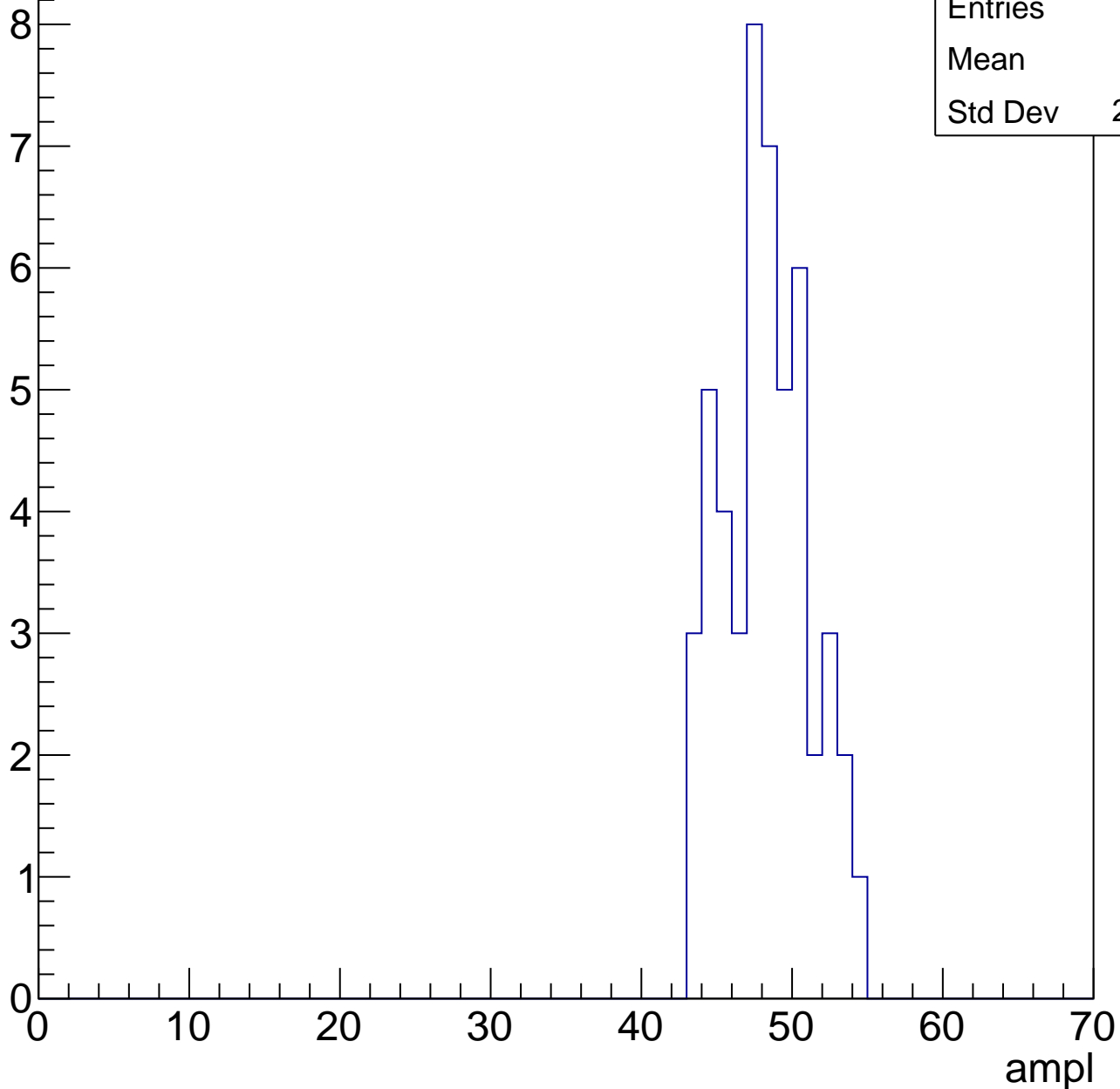
**Gaus Width: 3.5991**



# B1L101S, U20-ch46, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



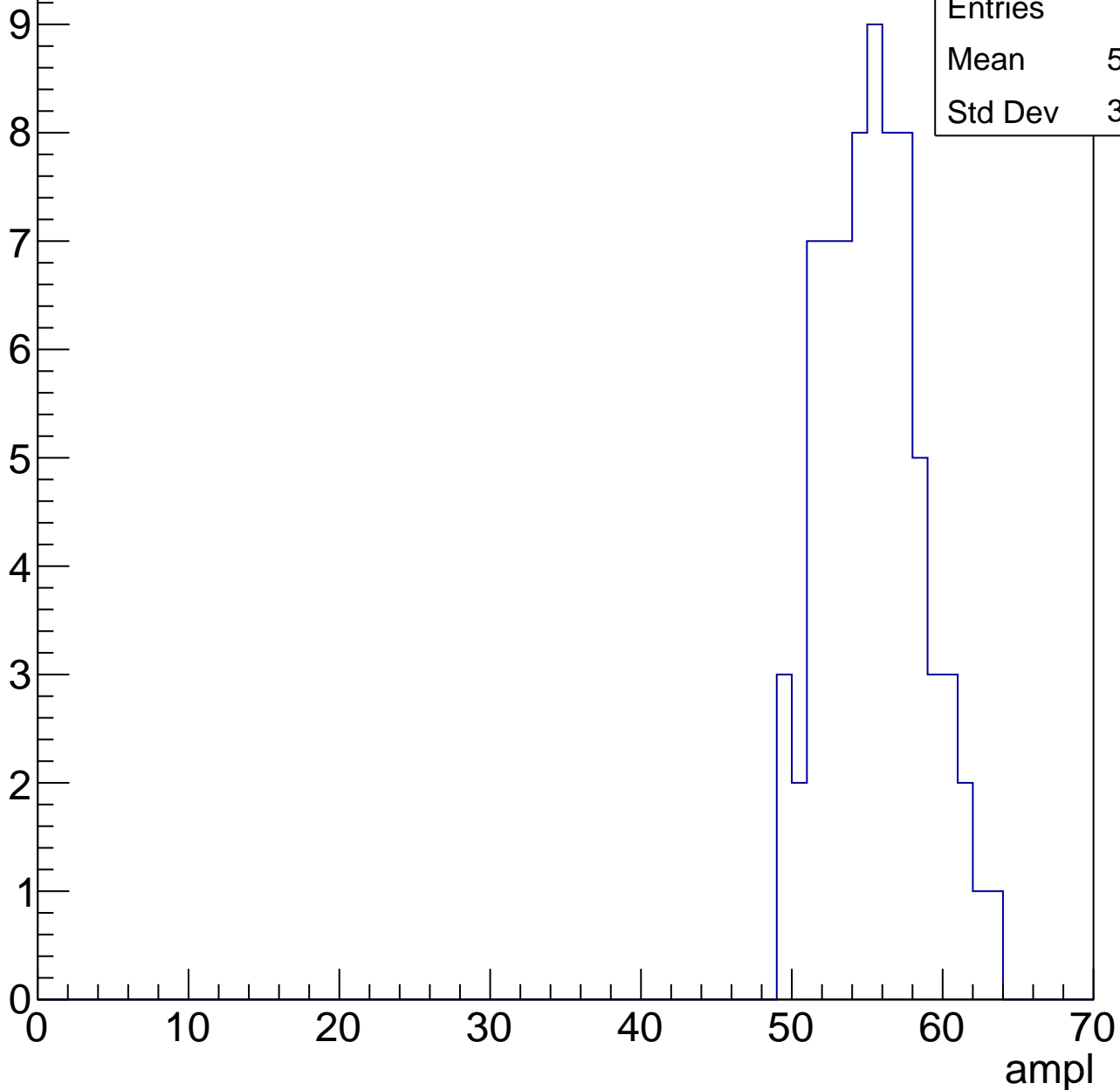
Entries	49
Mean	47.8
Std Dev	2.821

# B1L101S, U20-ch46, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

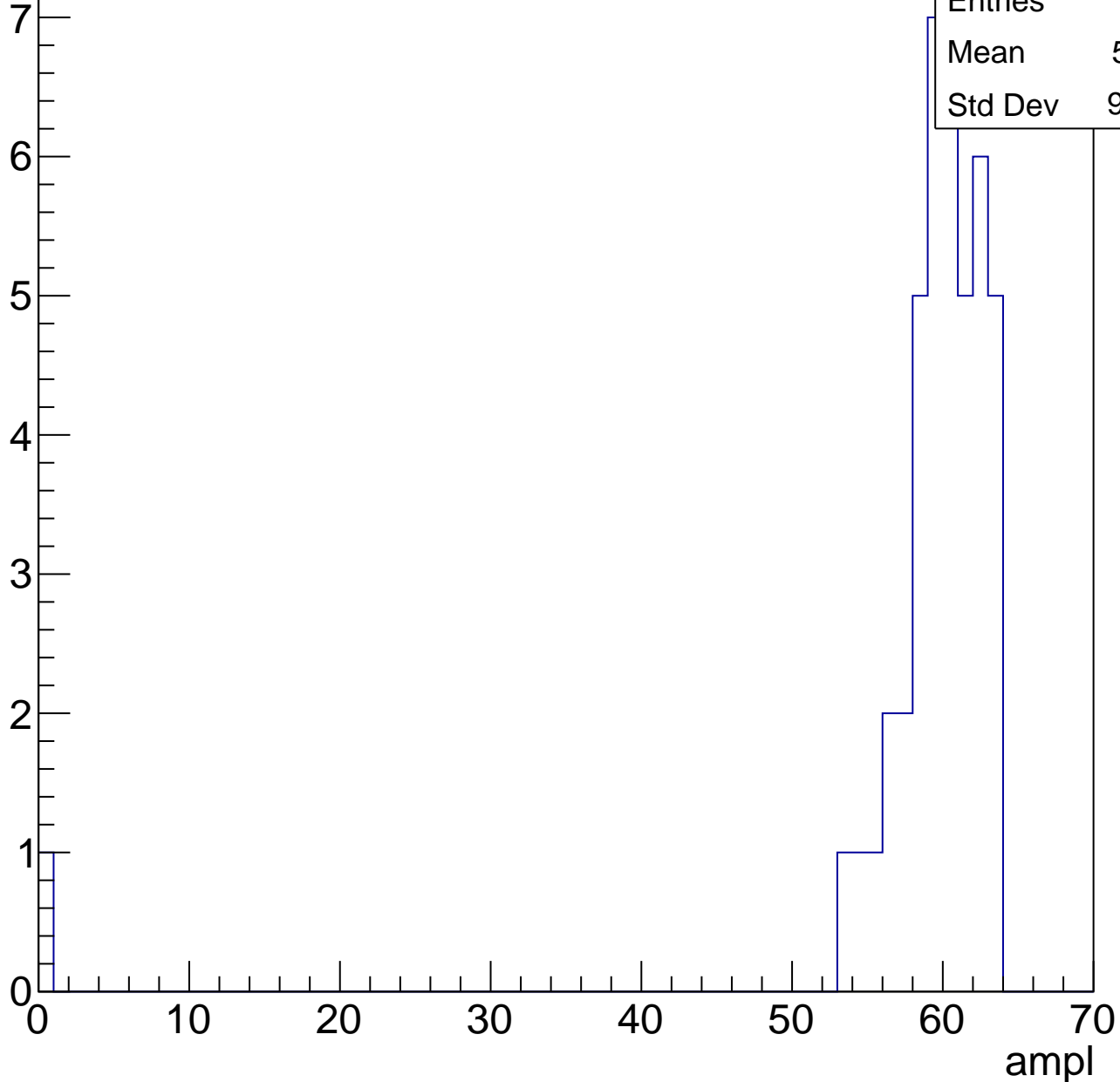
Entries	74
Mean	54.92
Std Dev	3.208



# B1L101S, U20-ch46, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U20-ch46, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

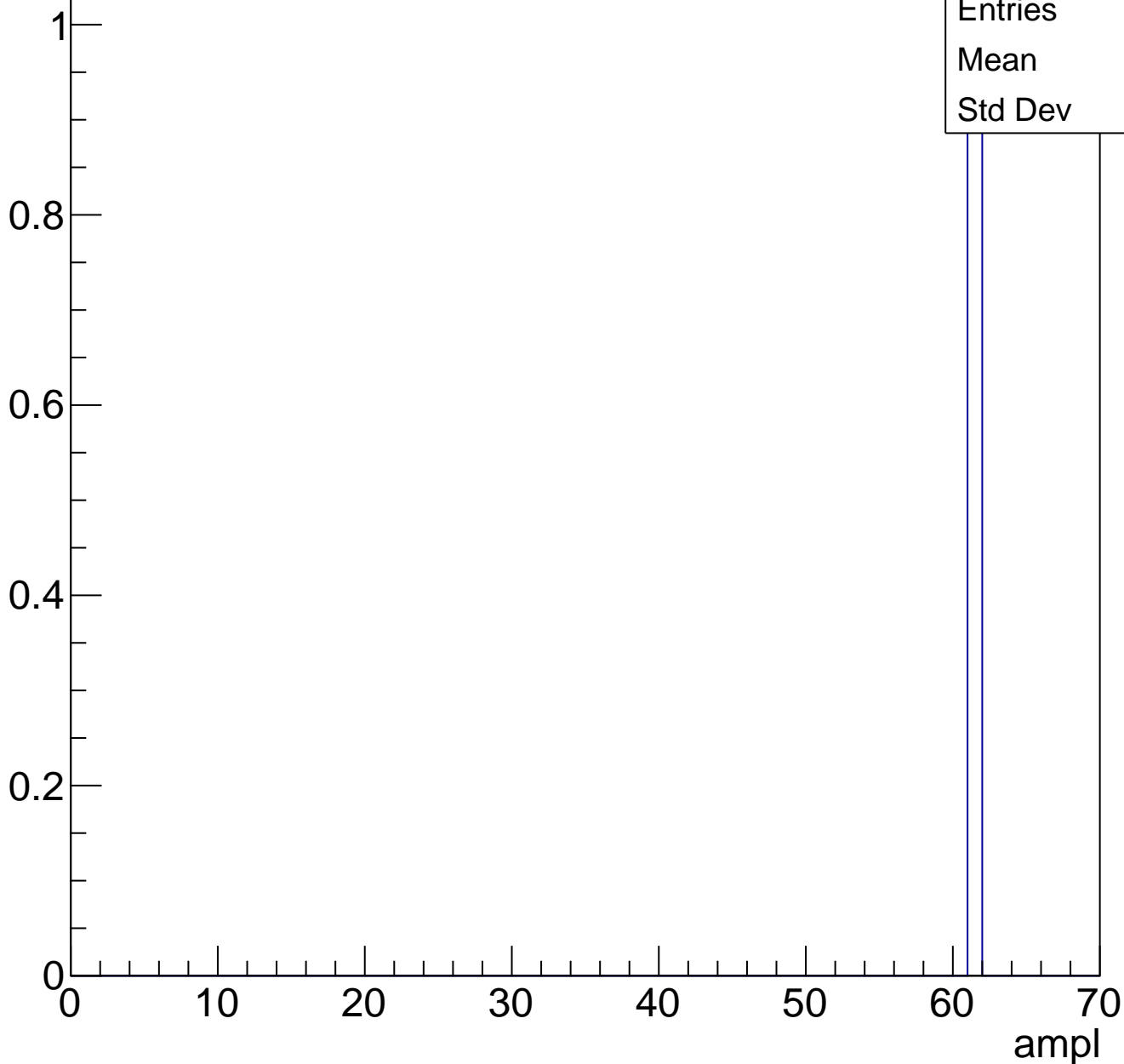




# B1L101S, U20-ch46, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U20-ch47, adc0

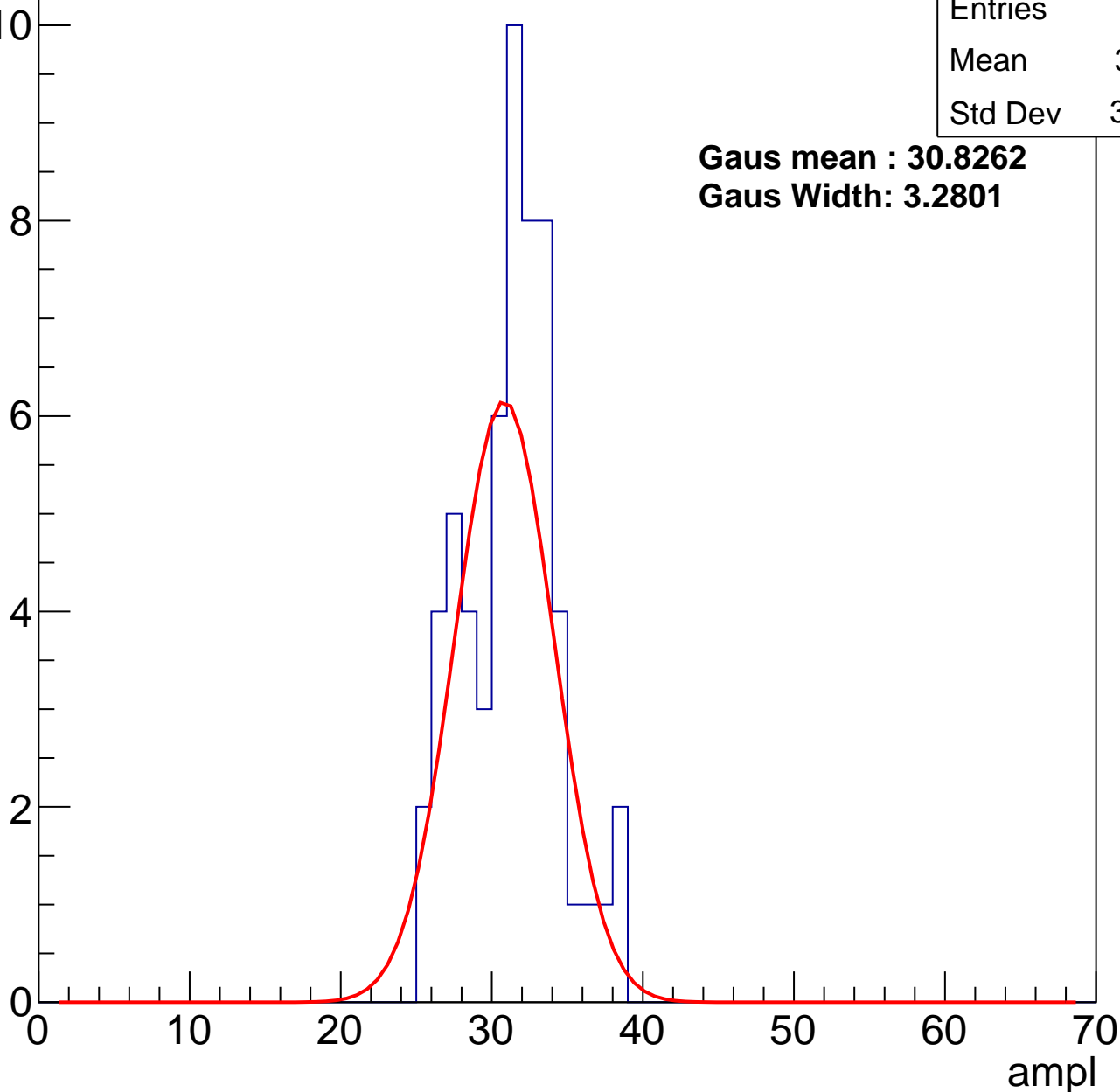
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	59
Mean	30.81
Std Dev	3.067

**Gaus mean : 30.8262**

**Gaus Width: 3.2801**



# B1L101S, U20-ch47, adc1

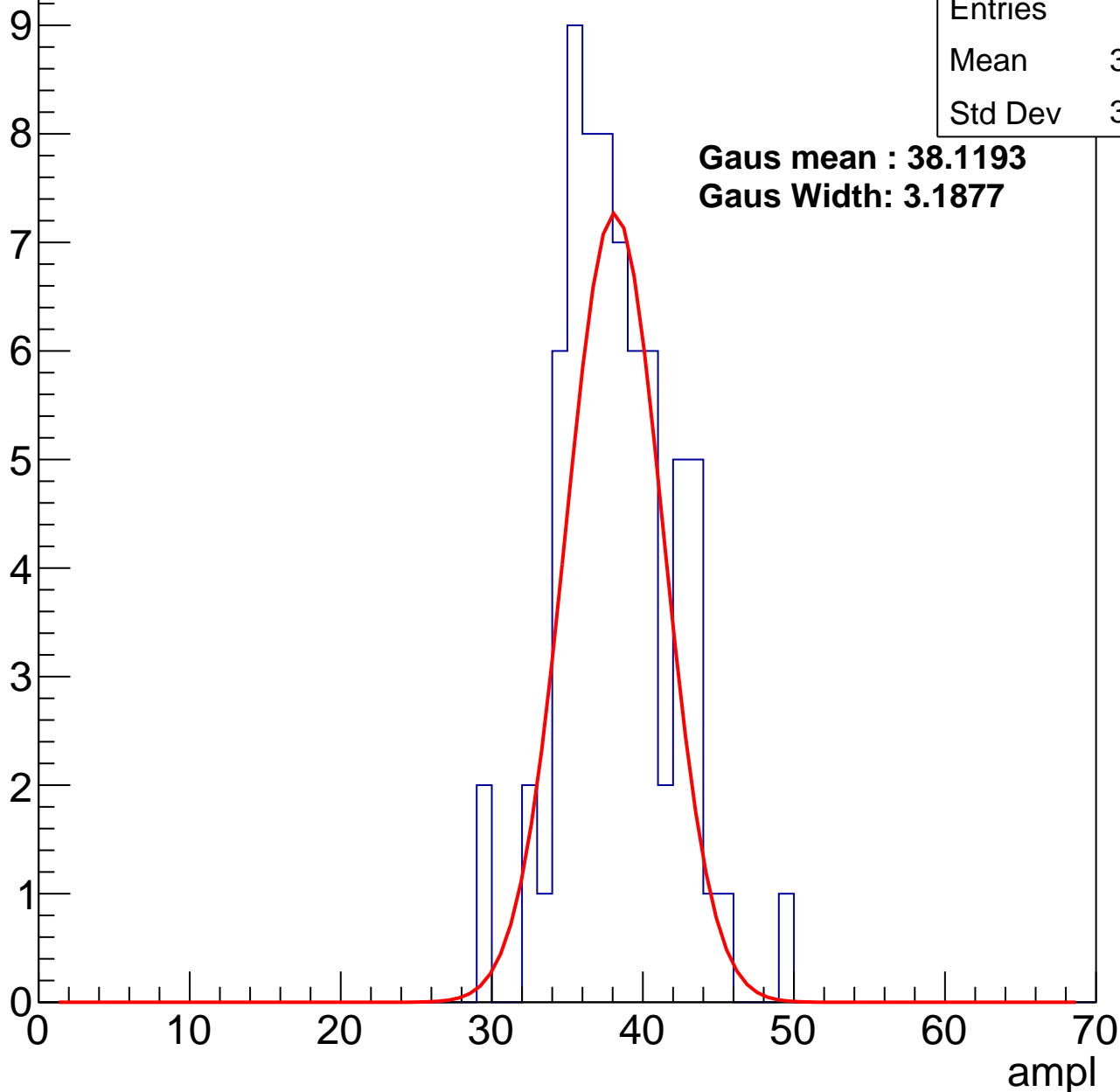
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	37.76
Std Dev	3.647

**Gaus mean : 38.1193**

**Gaus Width: 3.1877**



# B1L101S, U20-ch47, adc2

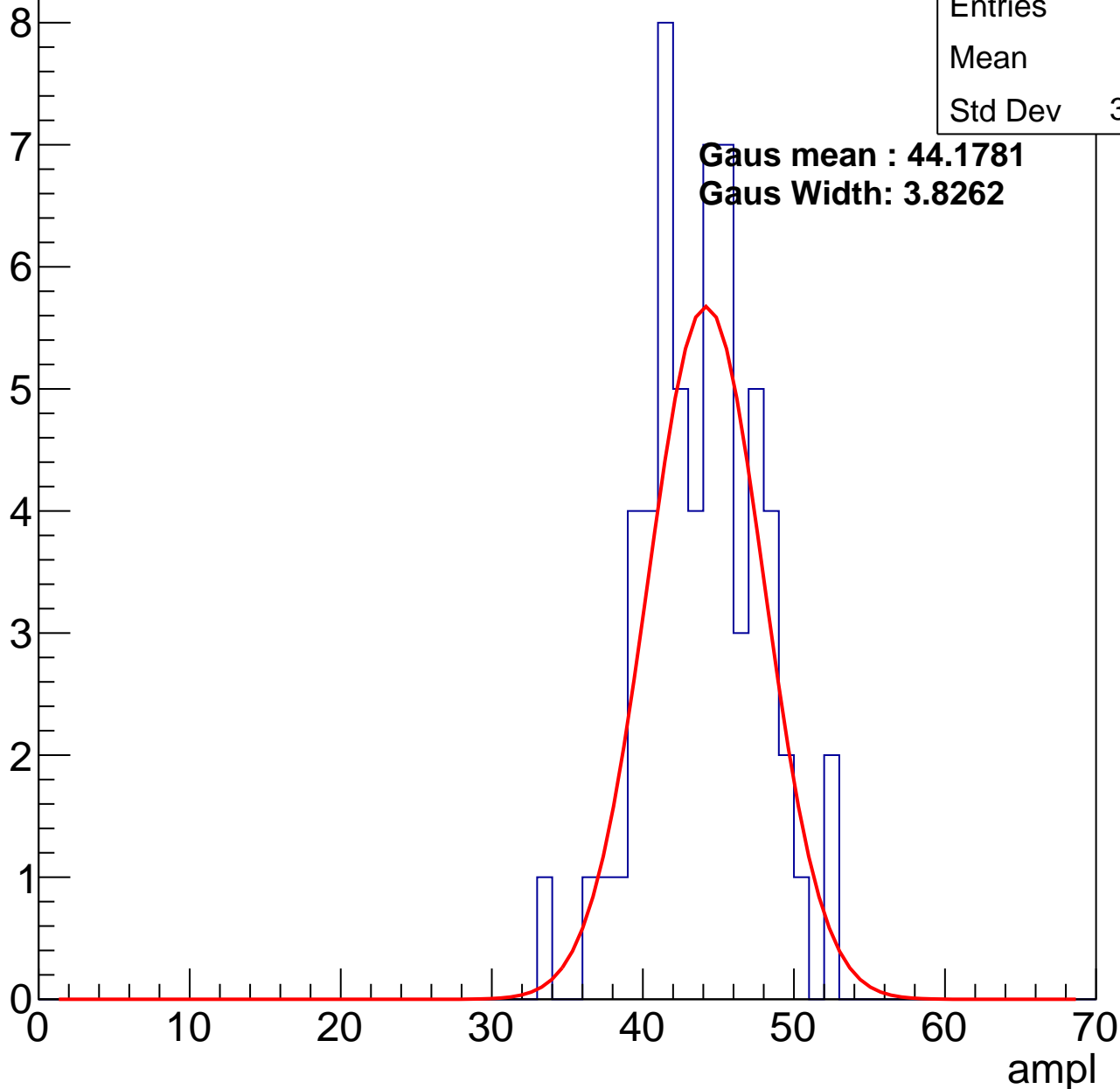
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	60
Mean	43.5
Std Dev	3.779

**Gaus mean : 44.1781**

**Gaus Width: 3.8262**

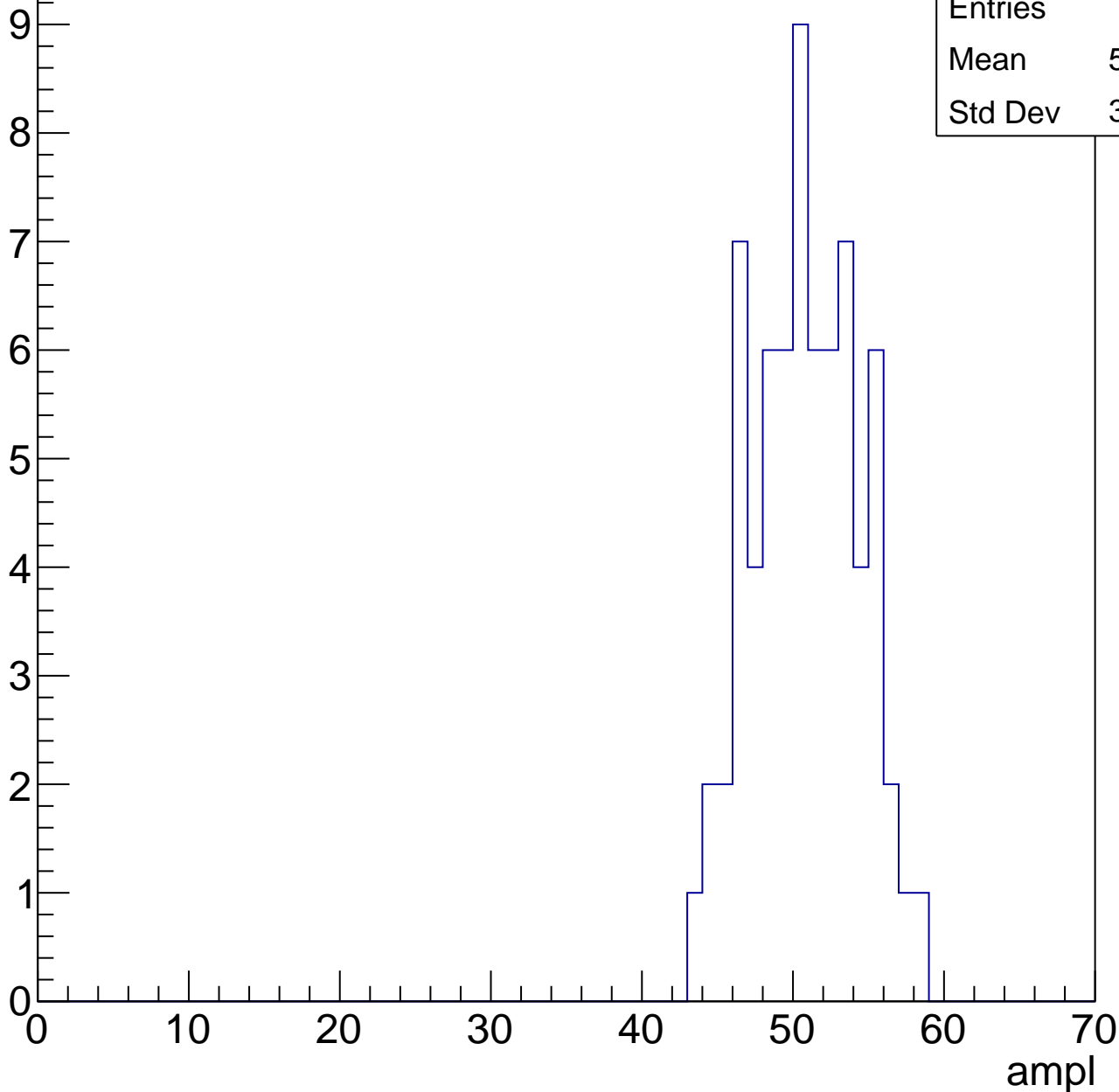


# B1L101S, U20-ch47, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	50.36
Std Dev	3.448

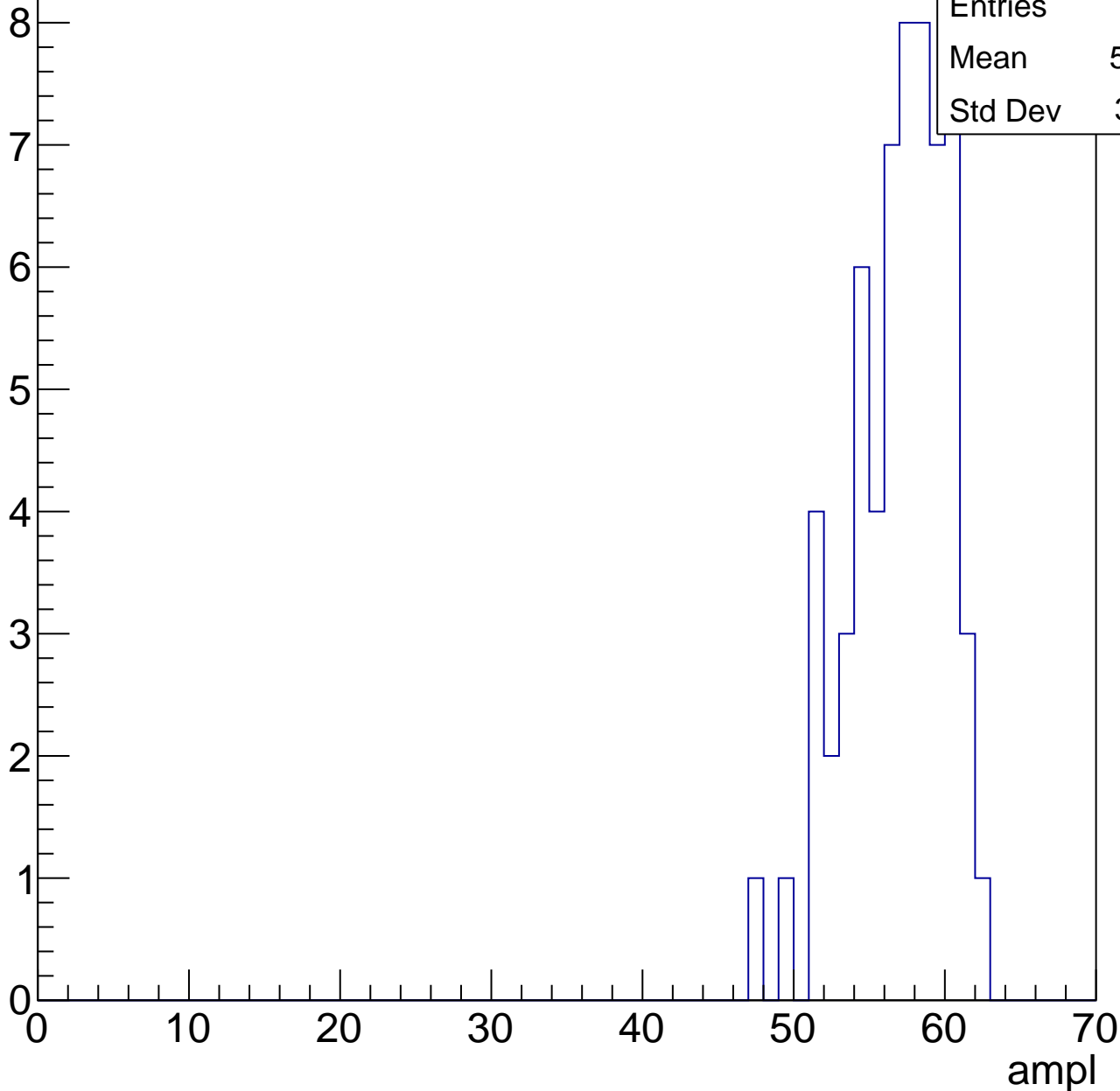


# B1L101S, U20-ch47, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	56.46
Std Dev	3.201

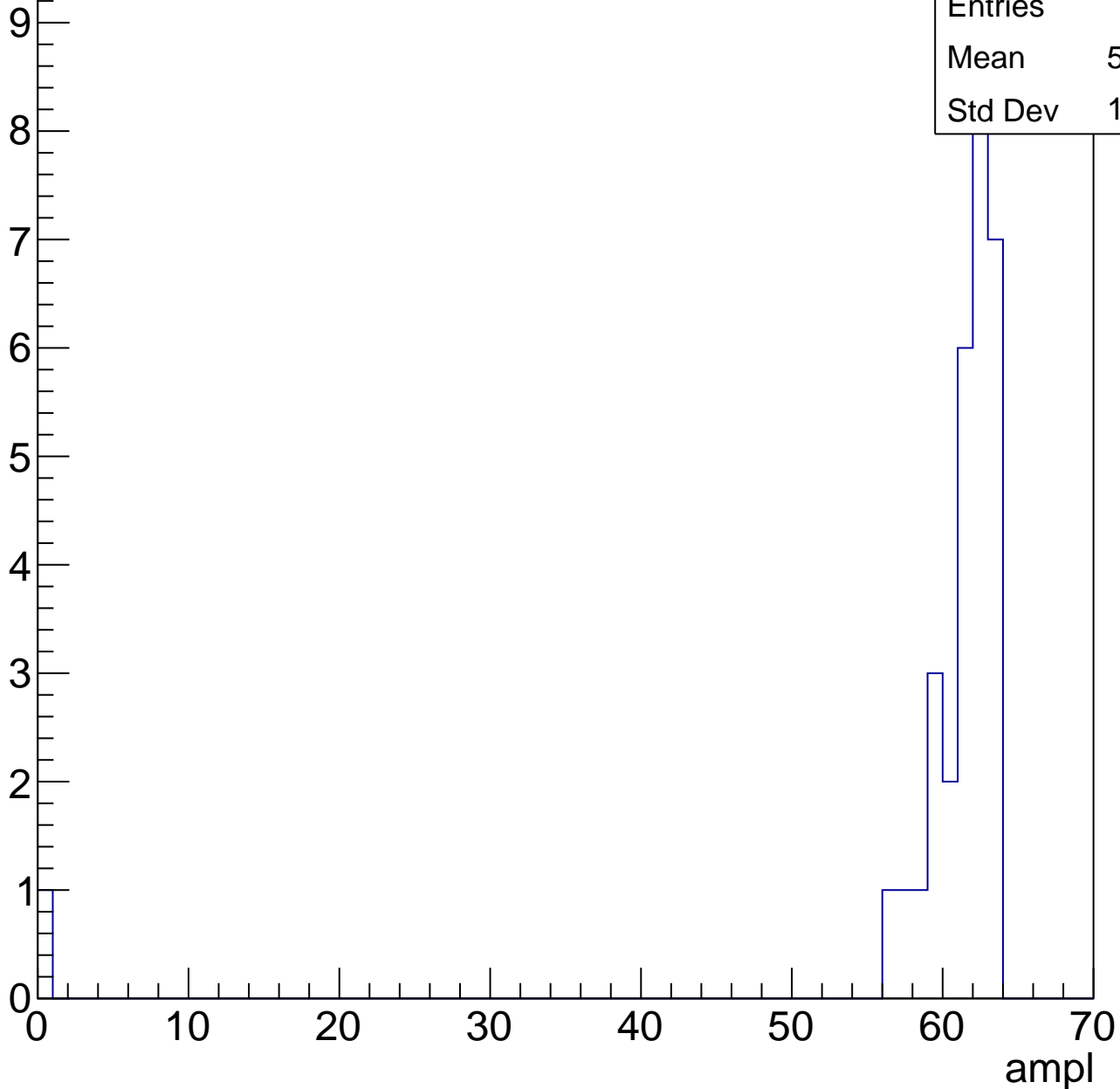


# B1L101S, U20-ch47, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	31
Mean	59.13
Std Dev	10.94



# B1L101S, U20-ch47, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U20-ch47, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L101S, U20-ch48, adc0

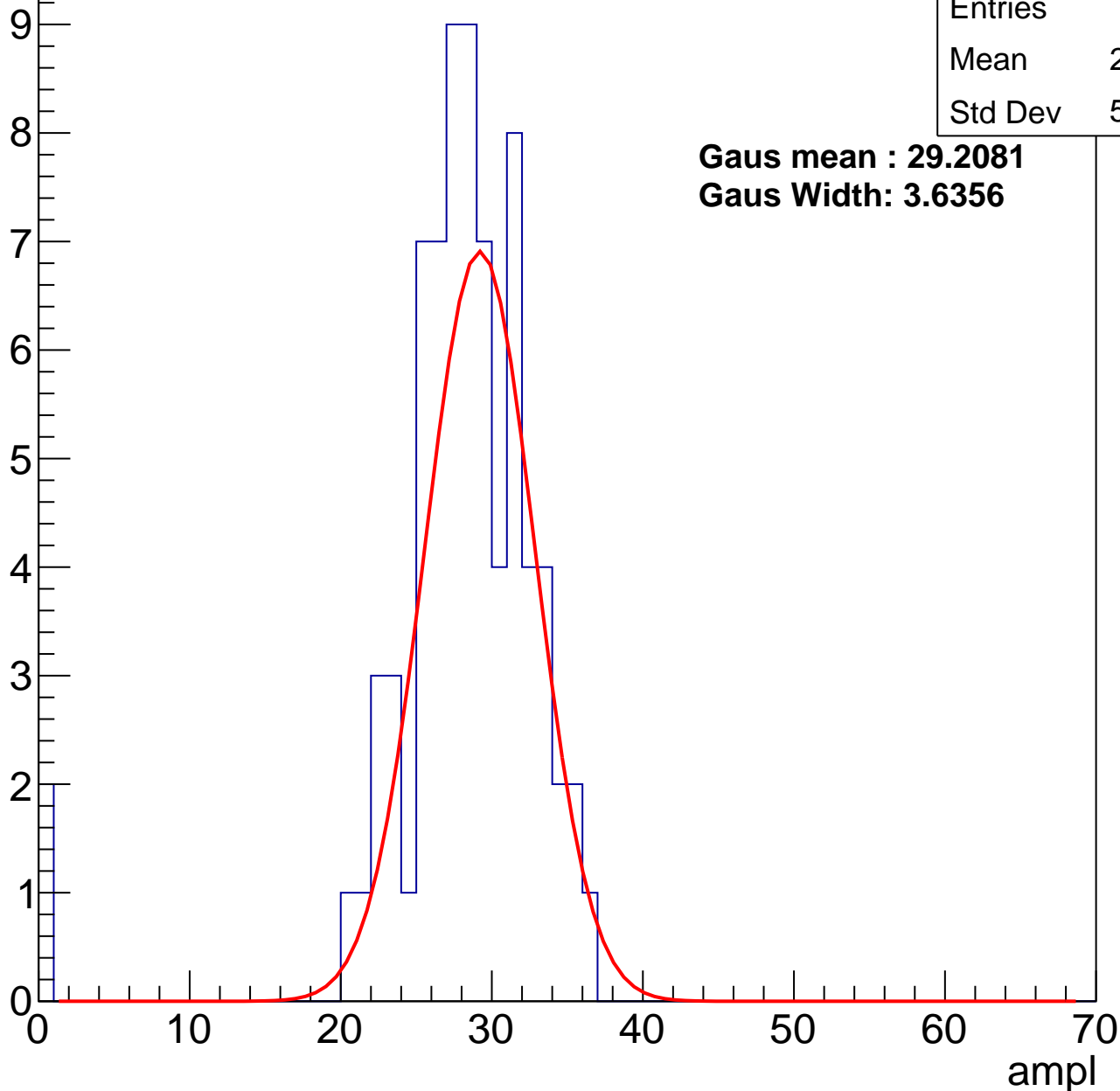
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	75
Mean	27.43
Std Dev	5.714

**Gaus mean : 29.2081**

**Gaus Width: 3.6356**



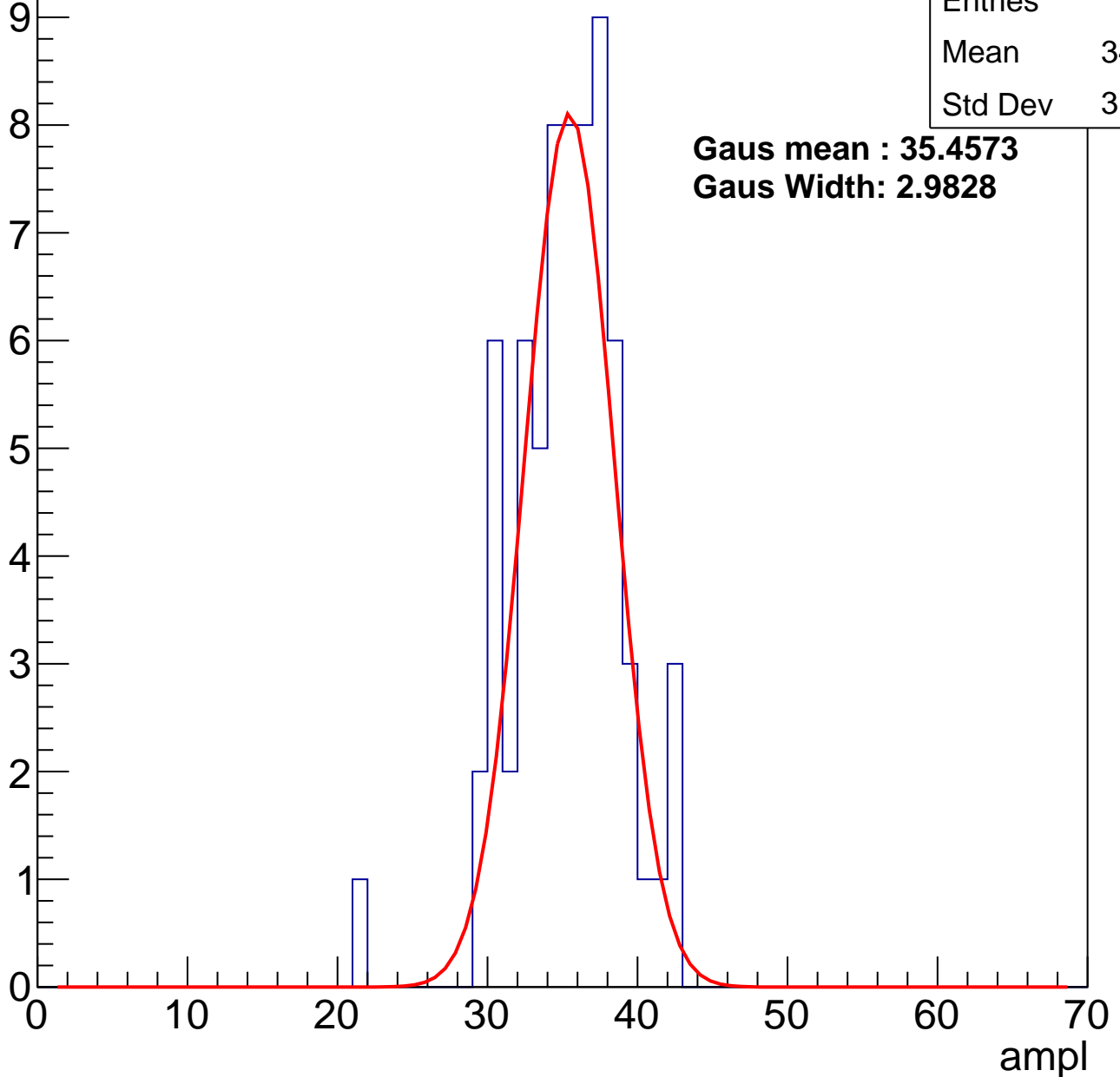
# B1L101S, U20-ch48, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	34.83
Std Dev	3.579

**Gaus mean : 35.4573**  
**Gaus Width: 2.9828**



# B1L101S, U20-ch48, adc2

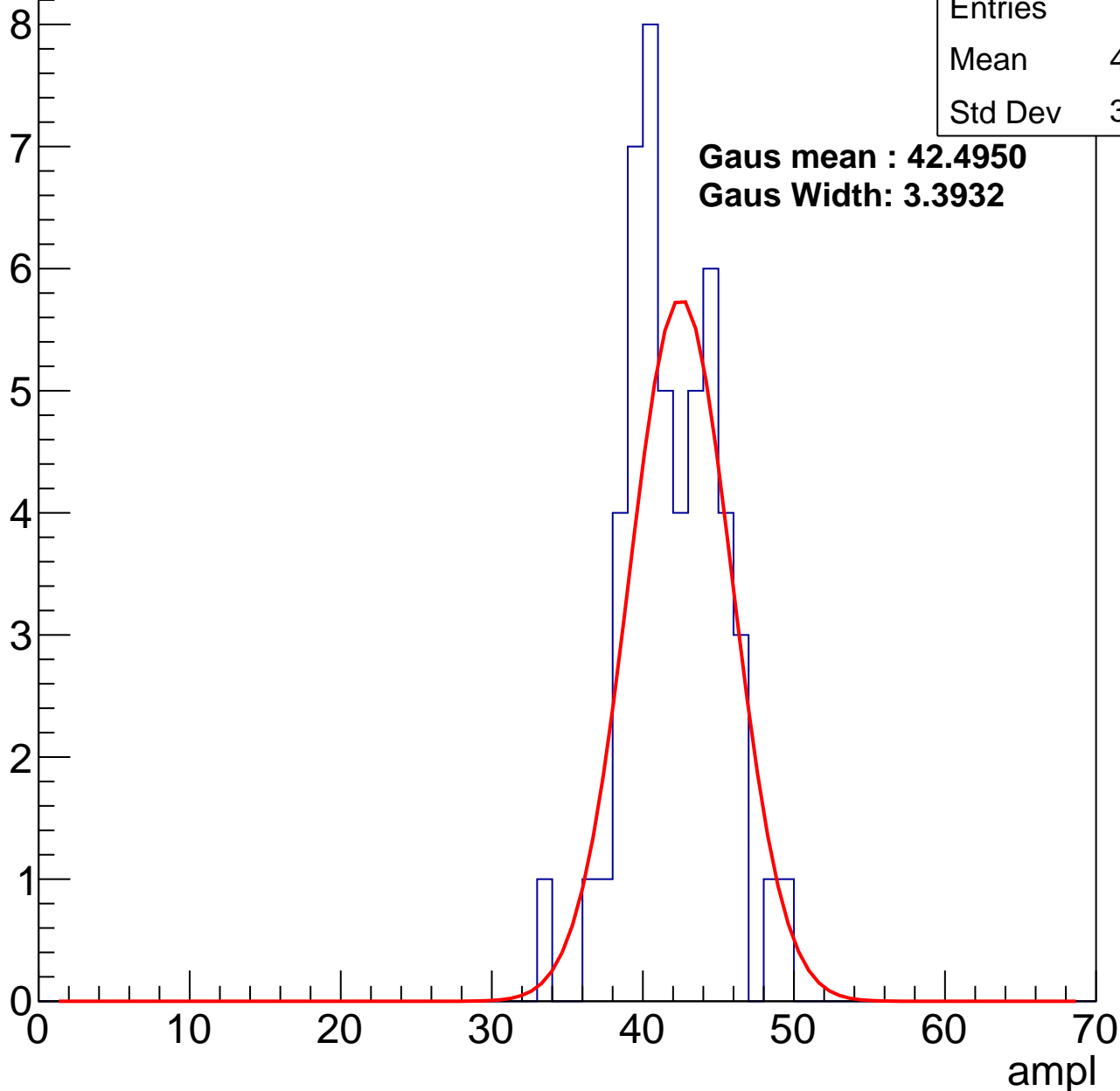
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	51
Mean	41.53
Std Dev	3.108

**Gaus mean : 42.4950**

**Gaus Width: 3.3932**

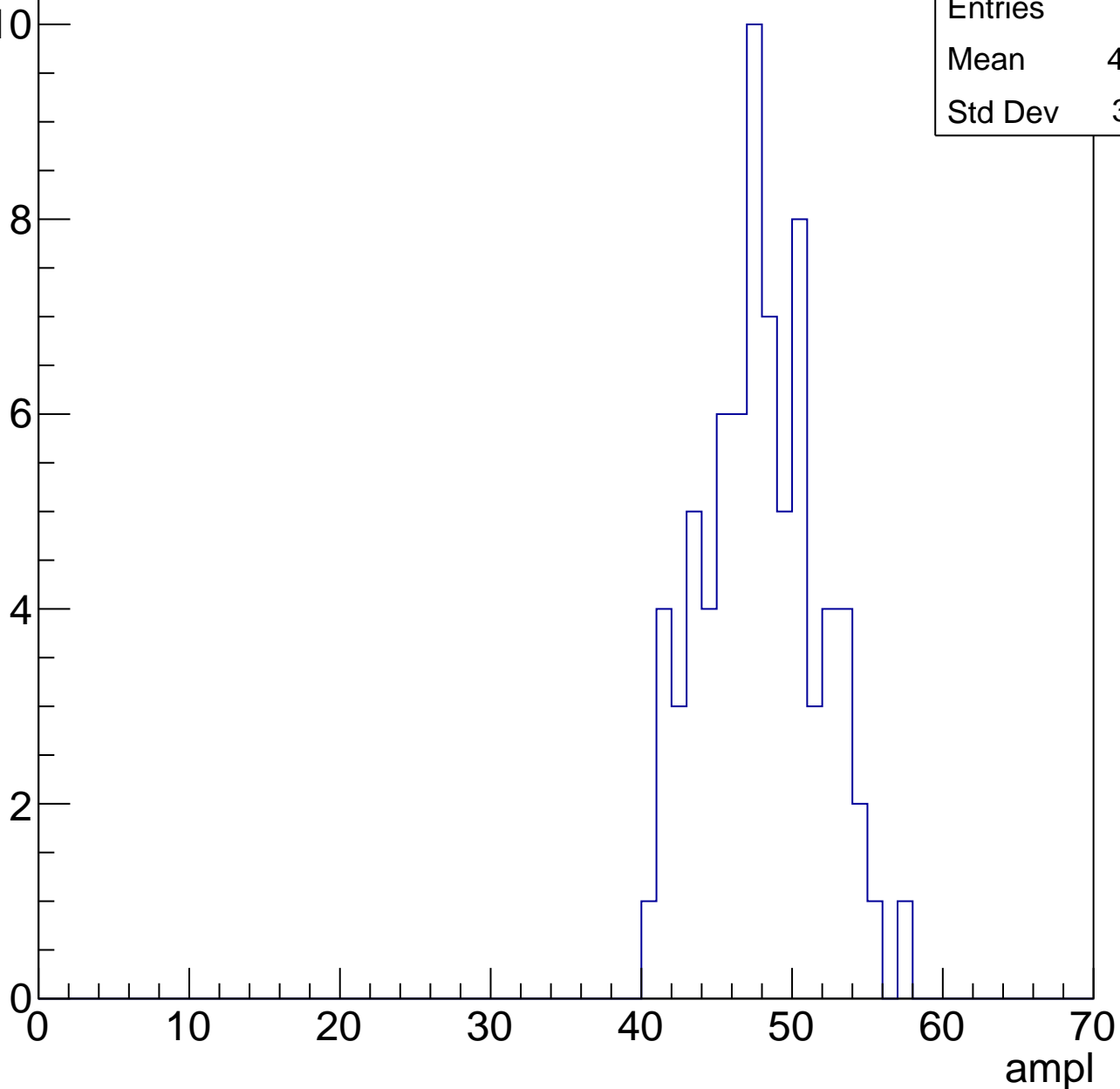


# B1L101S, U20-ch48, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	74
Mean	47.45
Std Dev	3.771

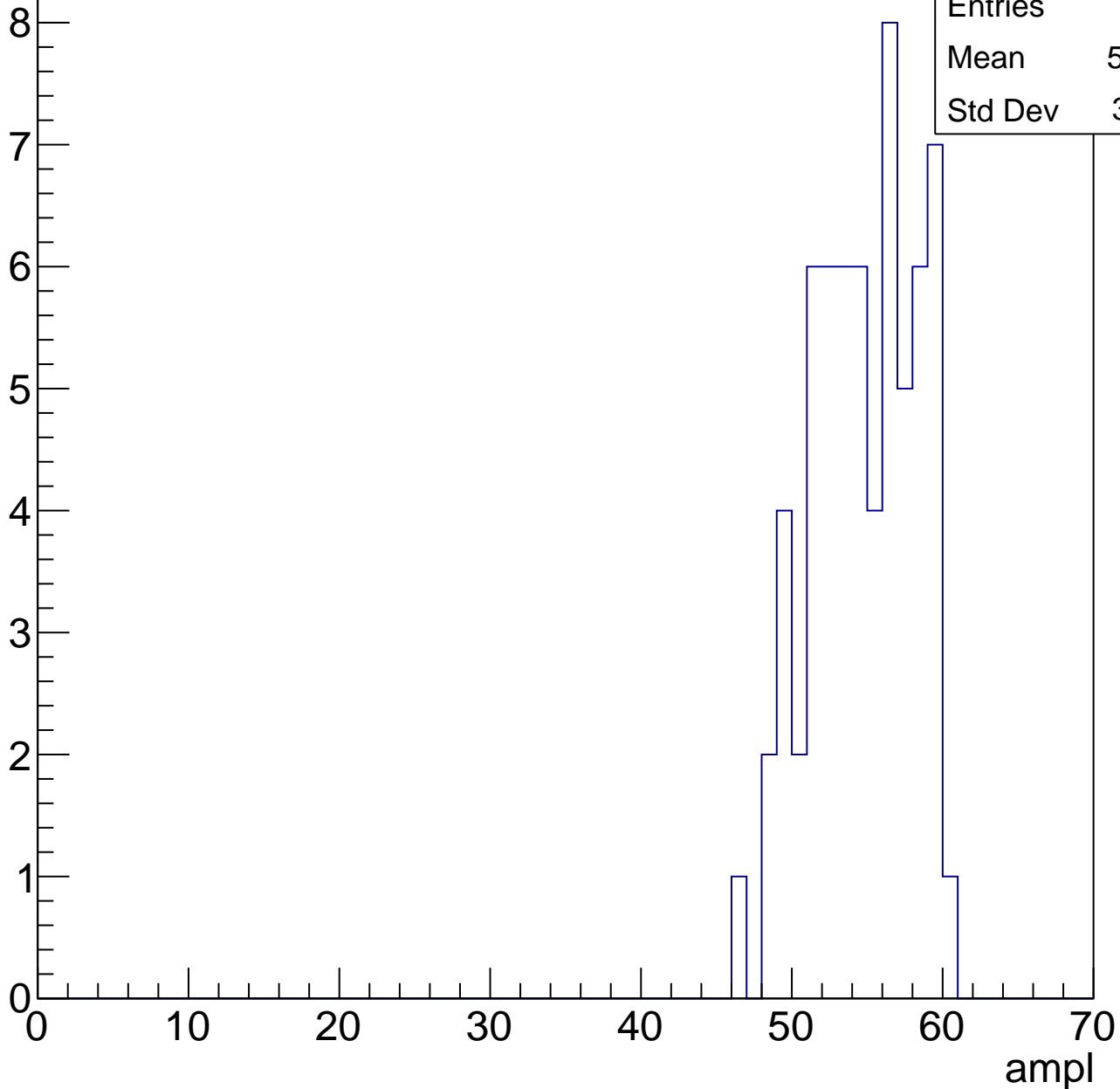


# B1L101S, U20-ch48, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	54.25
Std Dev	3.391

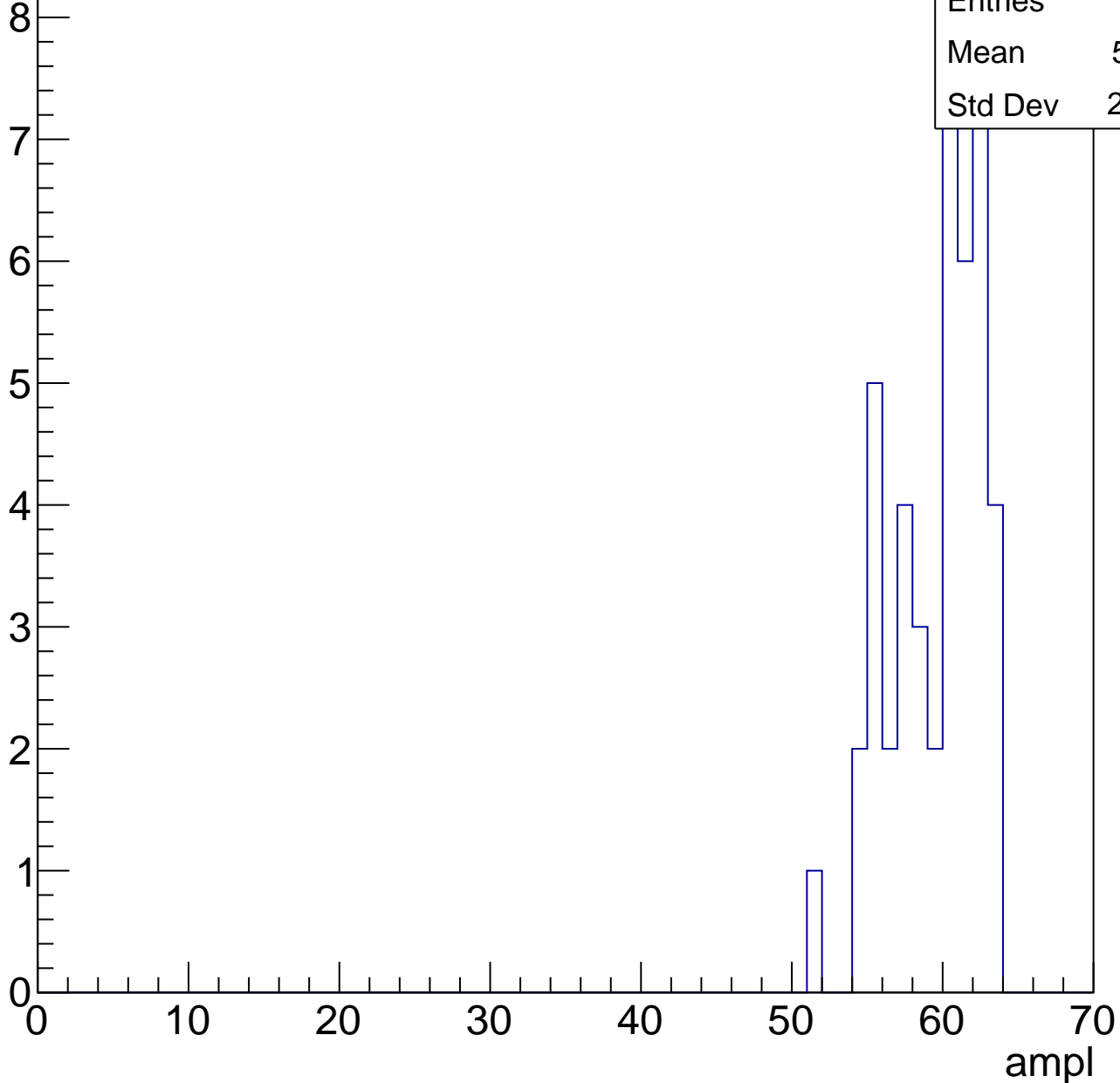


# B1L101S, U20-ch48, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	45
Mean	59.11
Std Dev	2.976

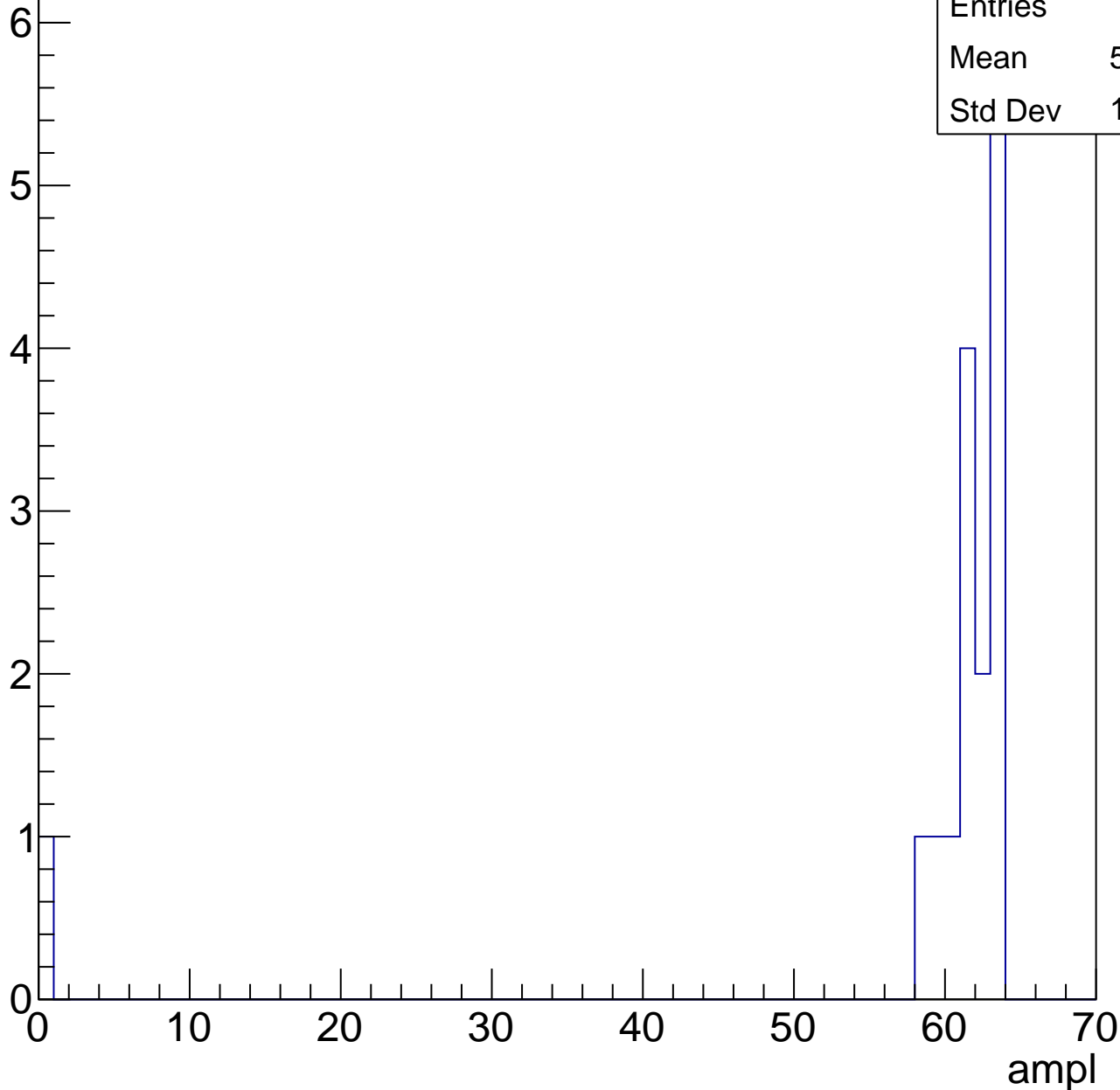


# B1L101S, U20-ch48, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	16
Mean	57.69
Std Dev	14.97





# B1L101S, U20-ch48, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L101S, U20-ch49, adc0

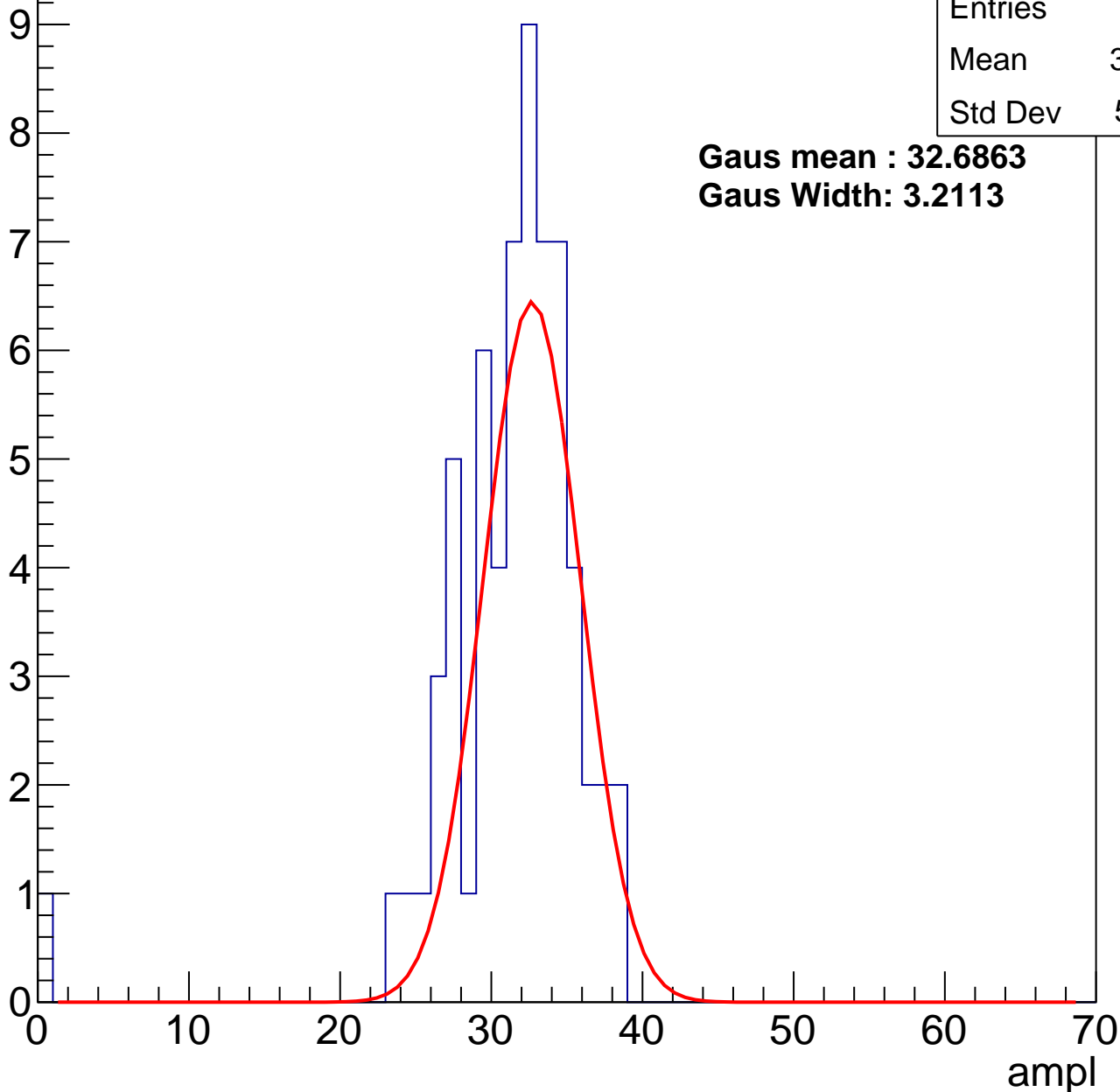
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	30.84
Std Dev	5.171

**Gaus mean : 32.6863**

**Gaus Width: 3.2113**



# B1L101S, U20-ch49, adc1

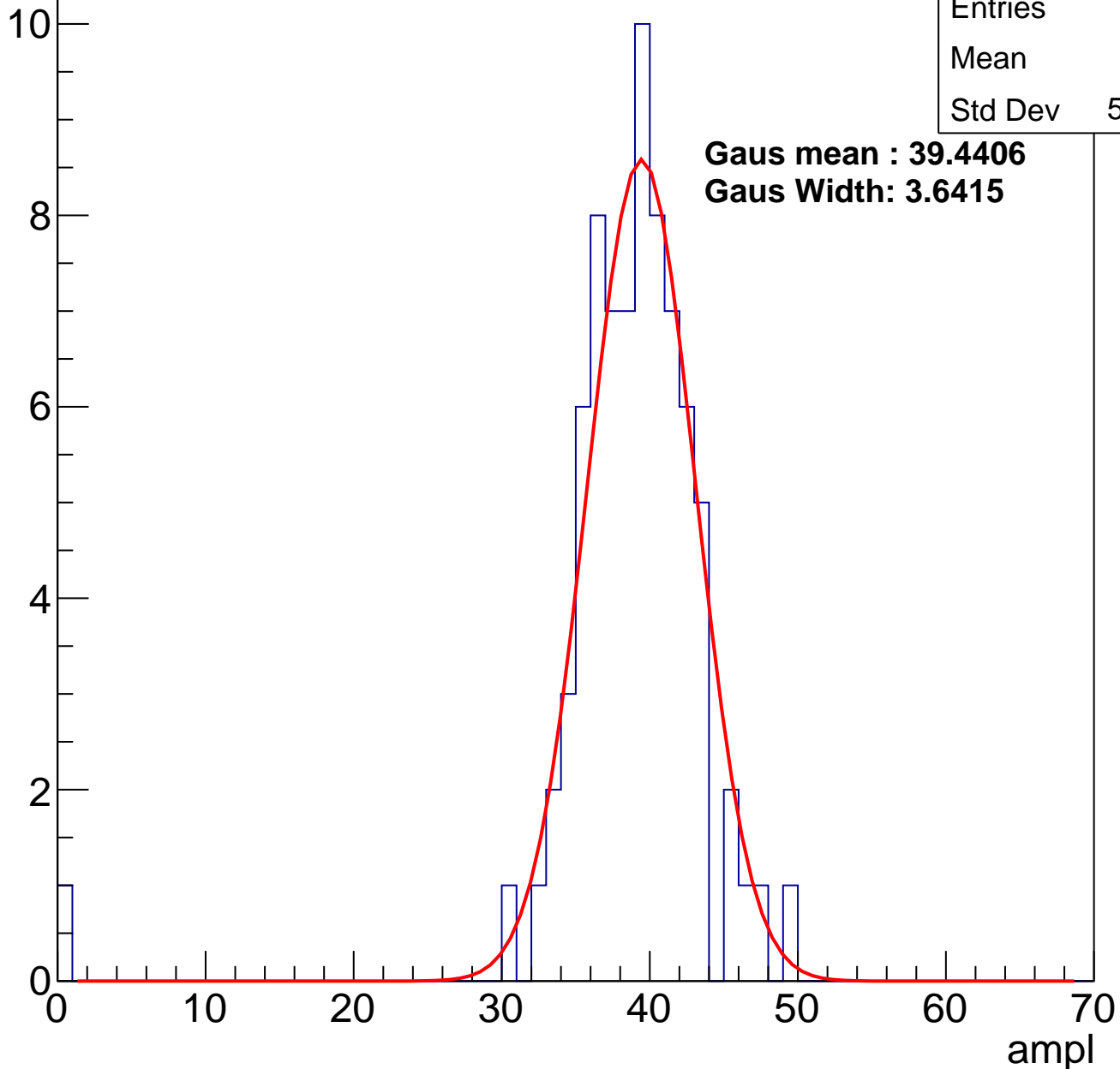
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	77
Mean	38.3
Std Dev	5.604

**Gaus mean : 39.4406**

**Gaus Width: 3.6415**

Entry



# B1L101S, U20-ch49, adc2

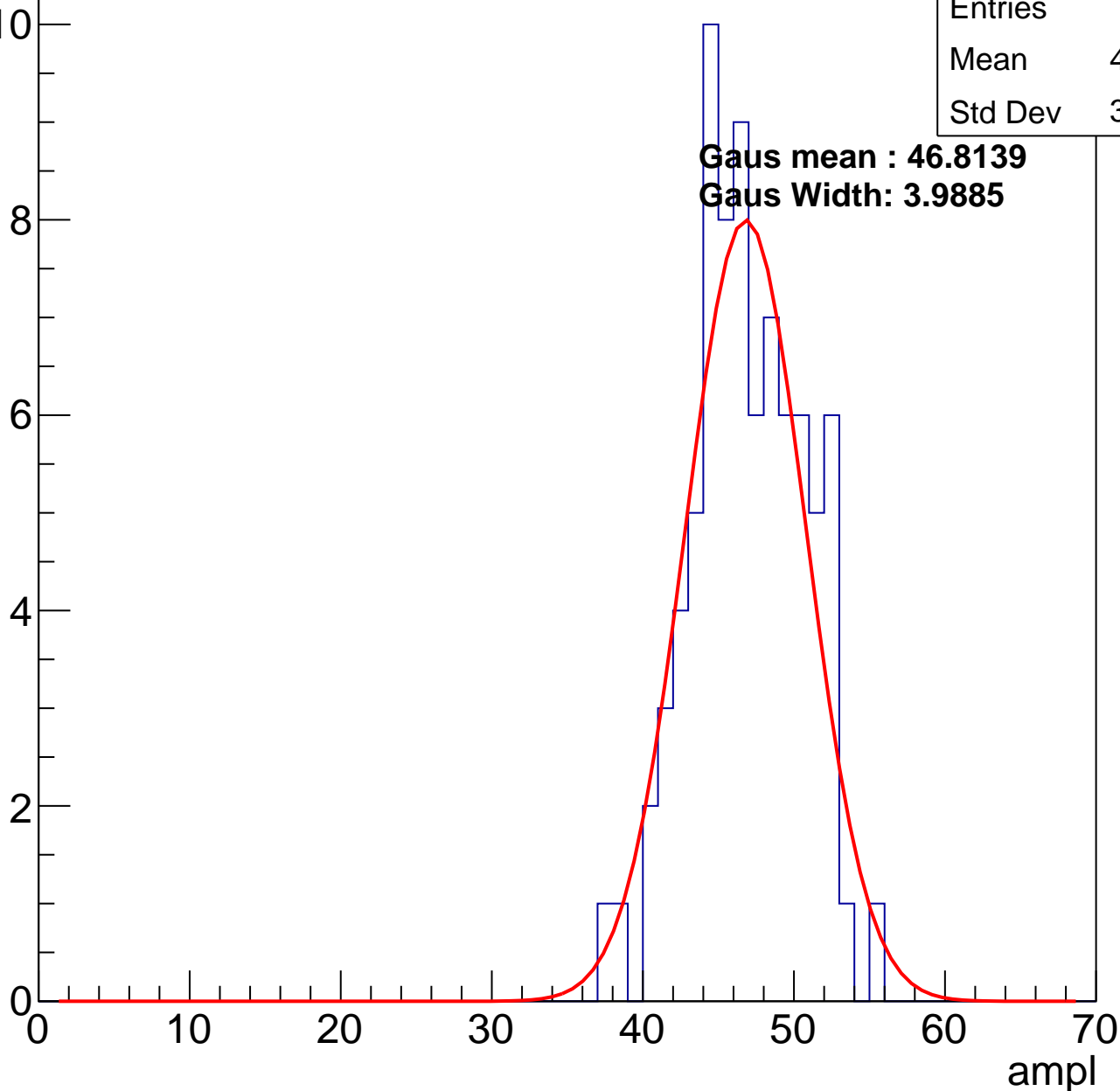
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	81
Mean	46.44
Std Dev	3.665

**Gaus mean : 46.8139**

**Gaus Width: 3.9885**



# B1L101S, U20-ch49, adc3

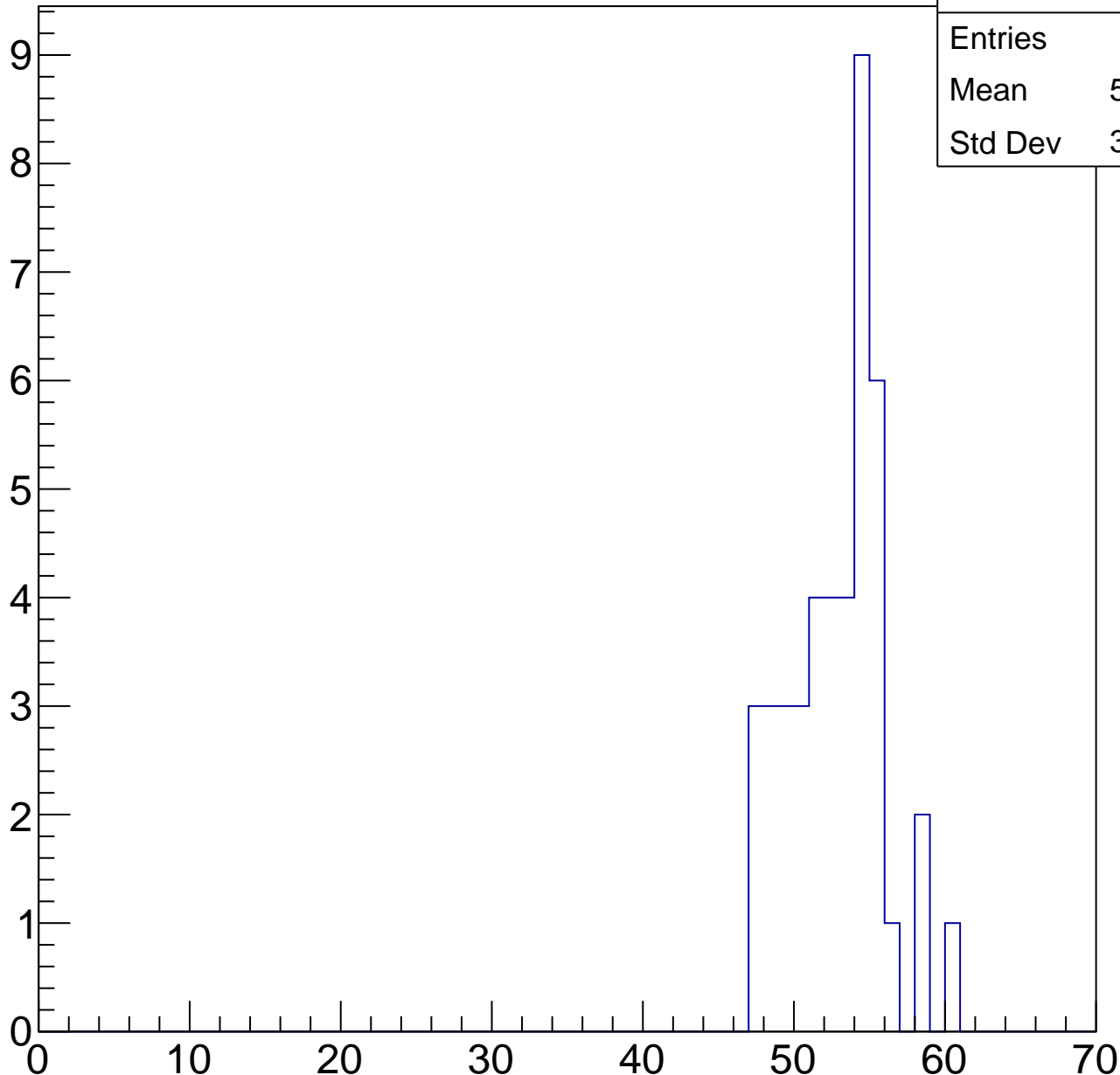
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	43
Mean	52.42
Std Dev	3.067

ampl



# B1L101S, U20-ch49, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

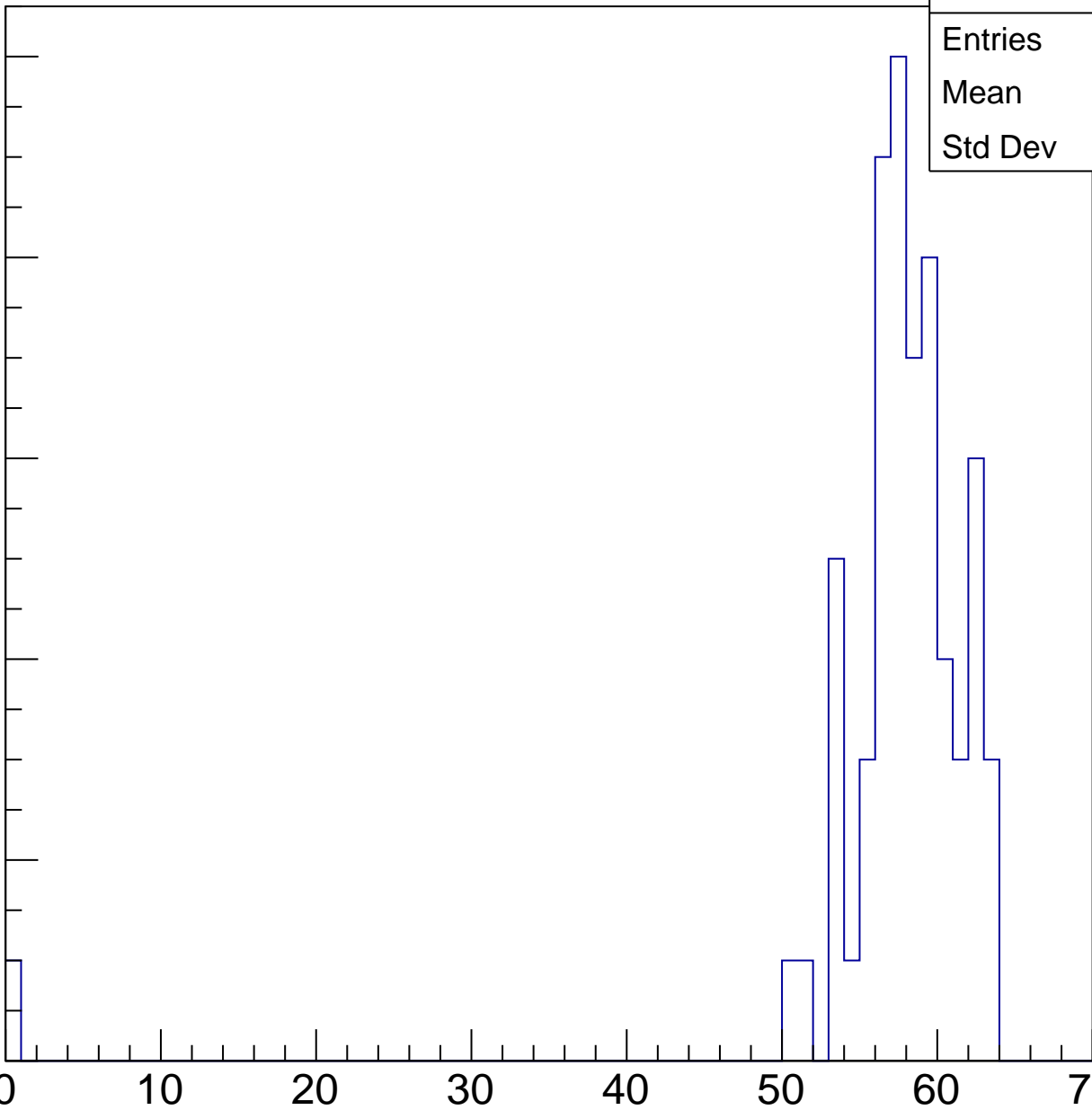
Entries	62
Mean	56.79
Std Dev	7.852

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

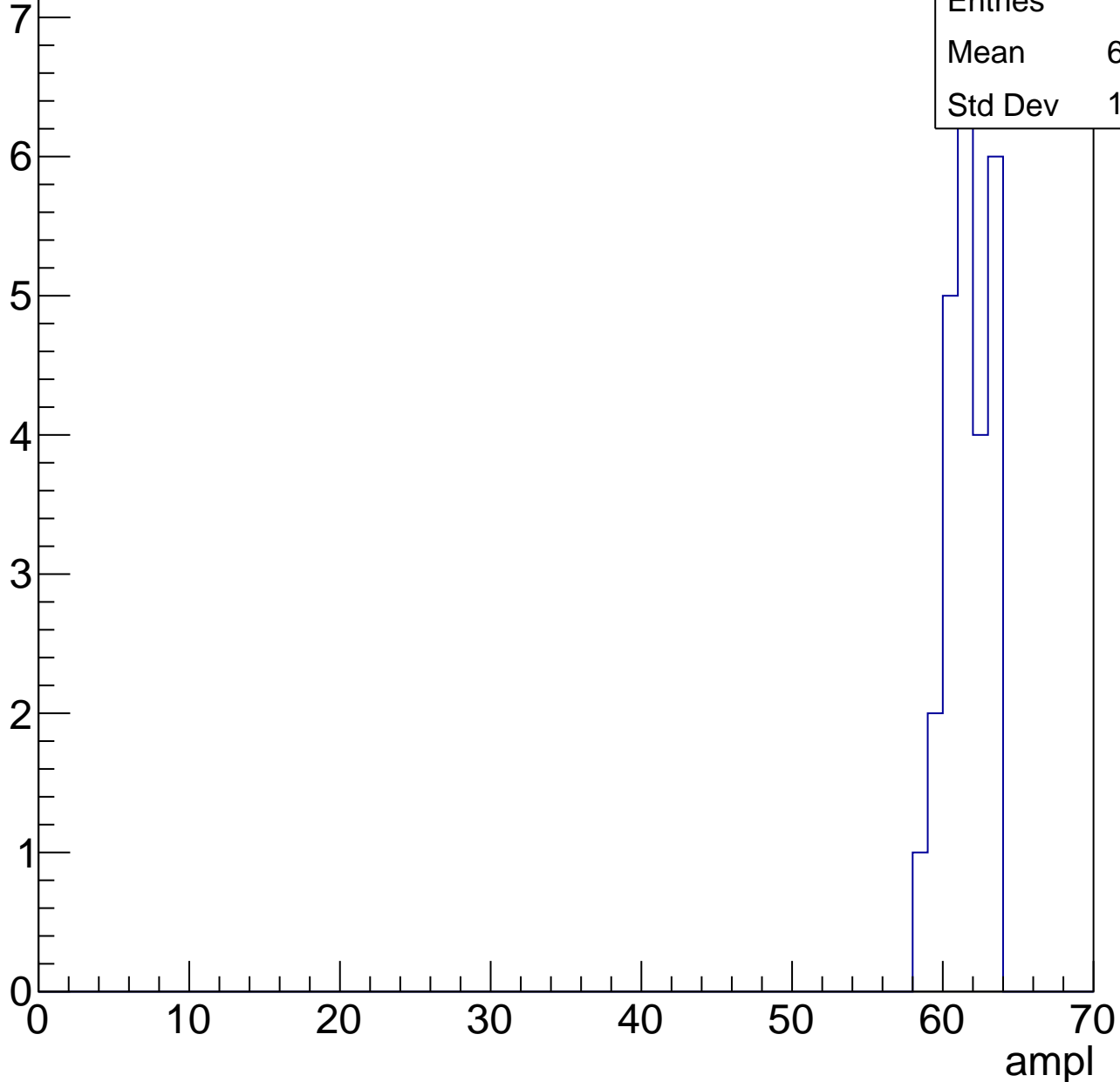
ampl



# B1L101S, U20-ch49, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U20-ch49, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U20-ch49, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U20-ch50, adc0

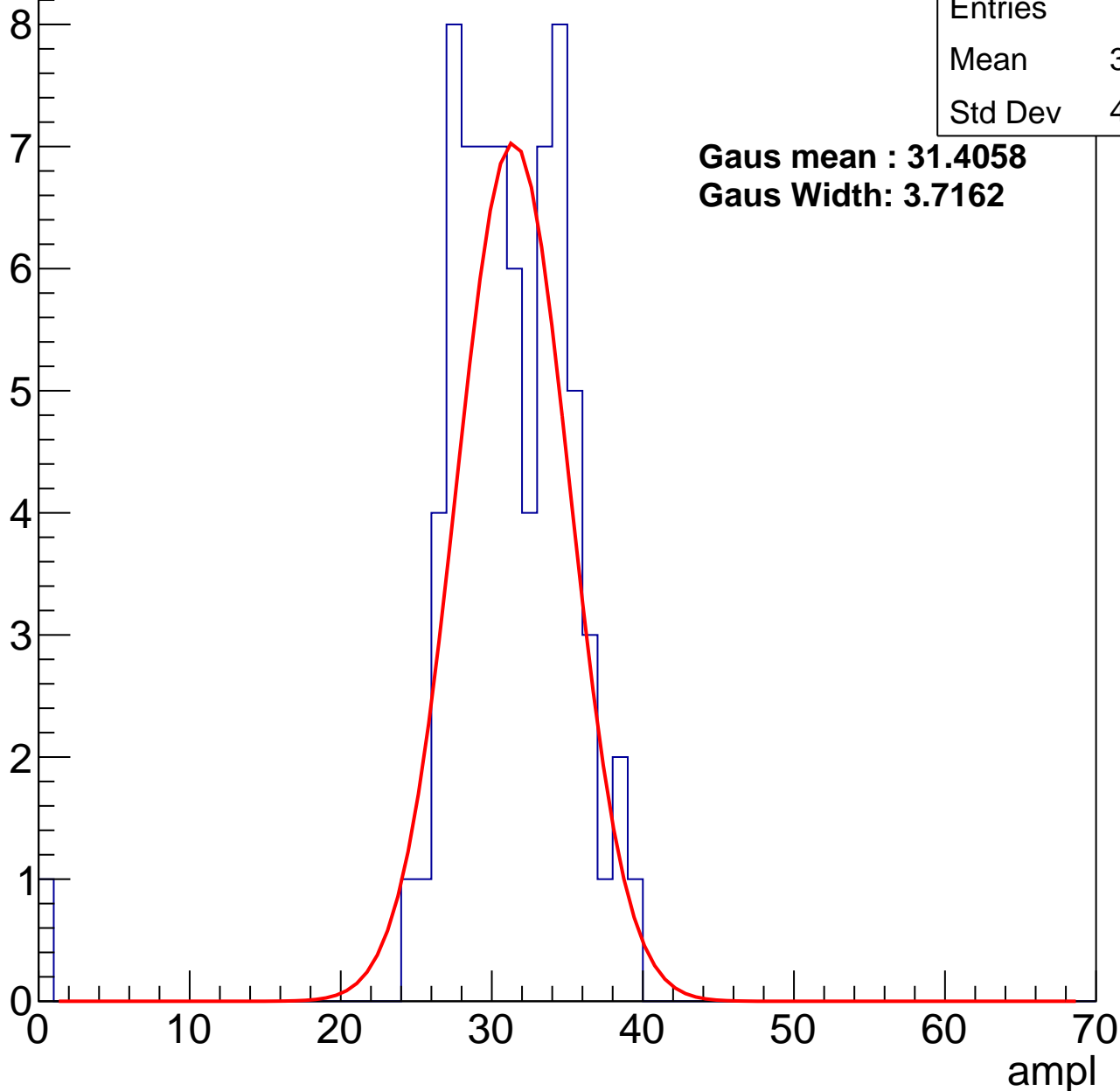
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	73
Mean	30.55
Std Dev	4.985

**Gaus mean : 31.4058**

**Gaus Width: 3.7162**



# B1L101S, U20-ch50, adc1

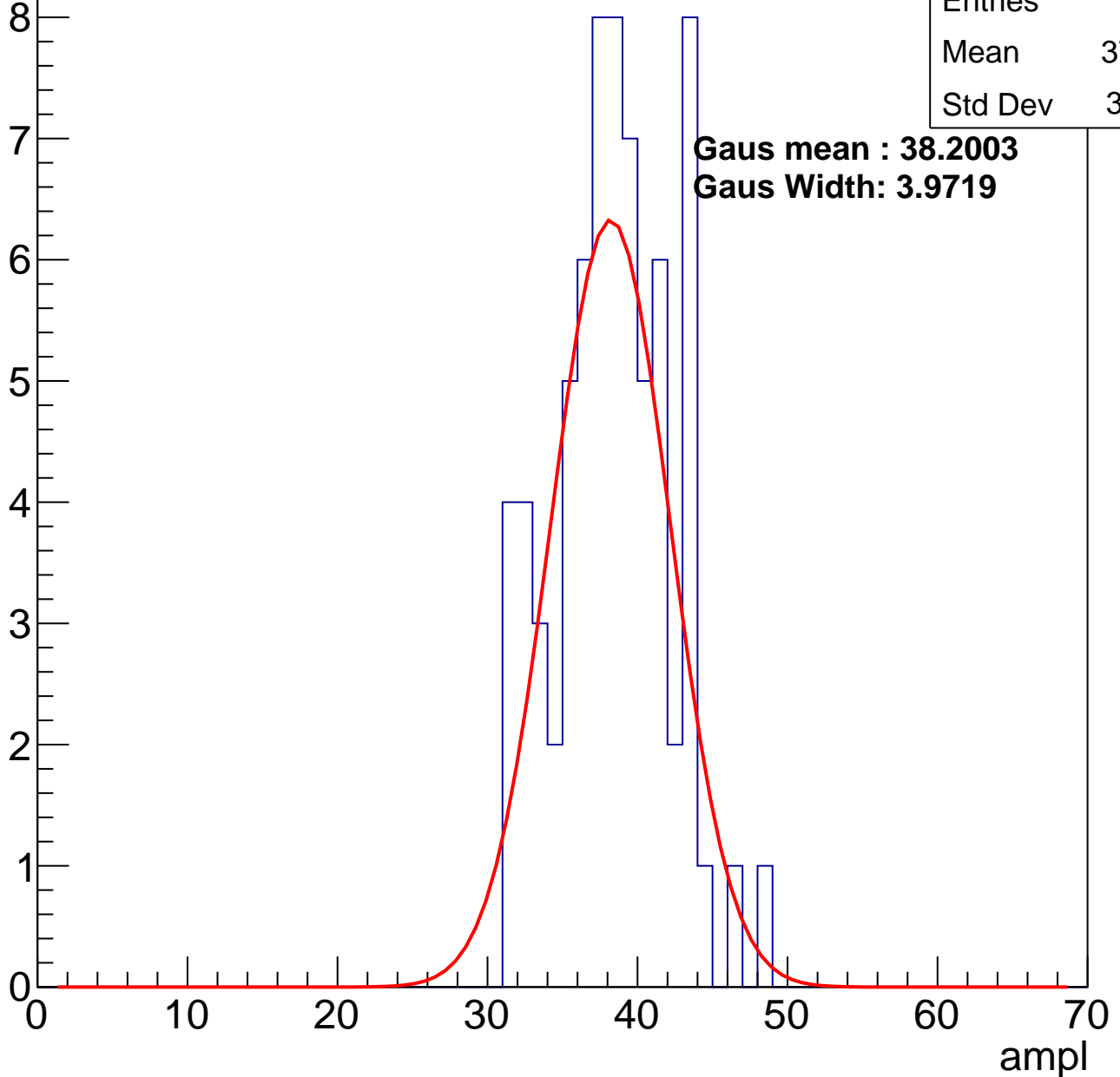
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	71
Mean	37.96
Std Dev	3.821

**Gaus mean : 38.2003**

**Gaus Width: 3.9719**



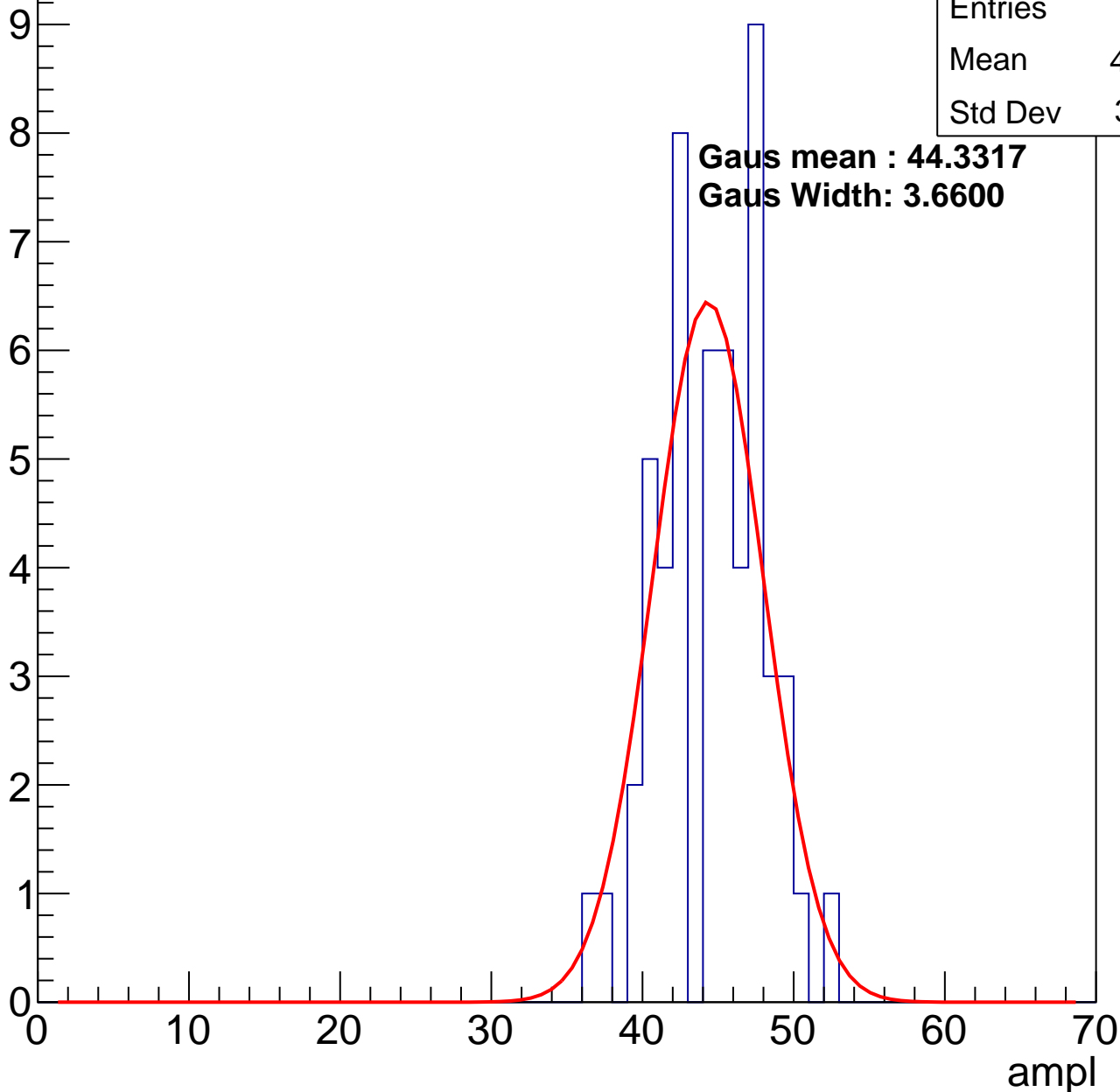
# B1L101S, U20-ch50, adc2

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	54
Mean	44.17
Std Dev	3.431

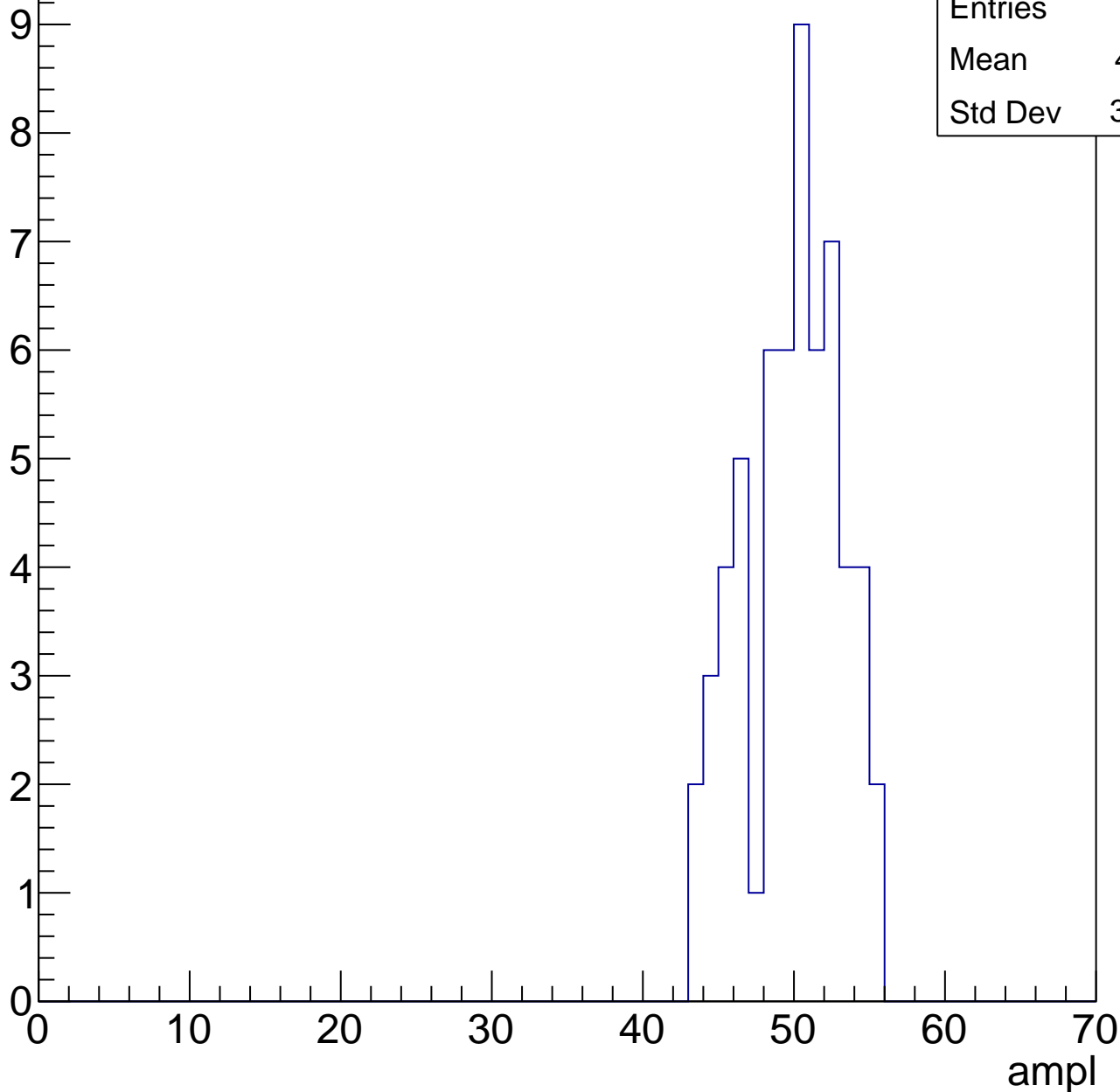
**Gaus mean : 44.3317**  
**Gaus Width: 3.6600**



# B1L101S, U20-ch50, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

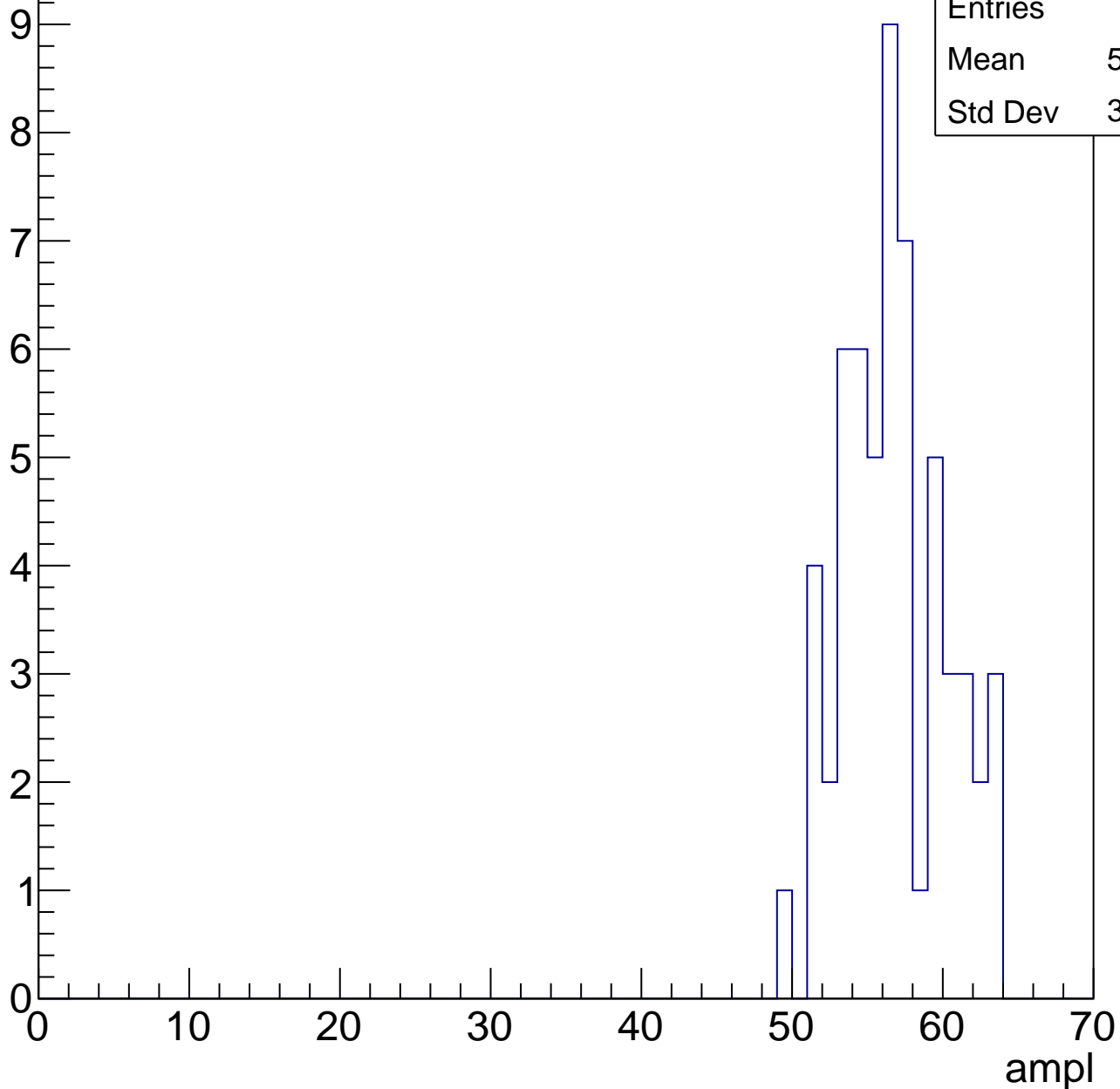
Entry



# B1L101S, U20-ch50, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



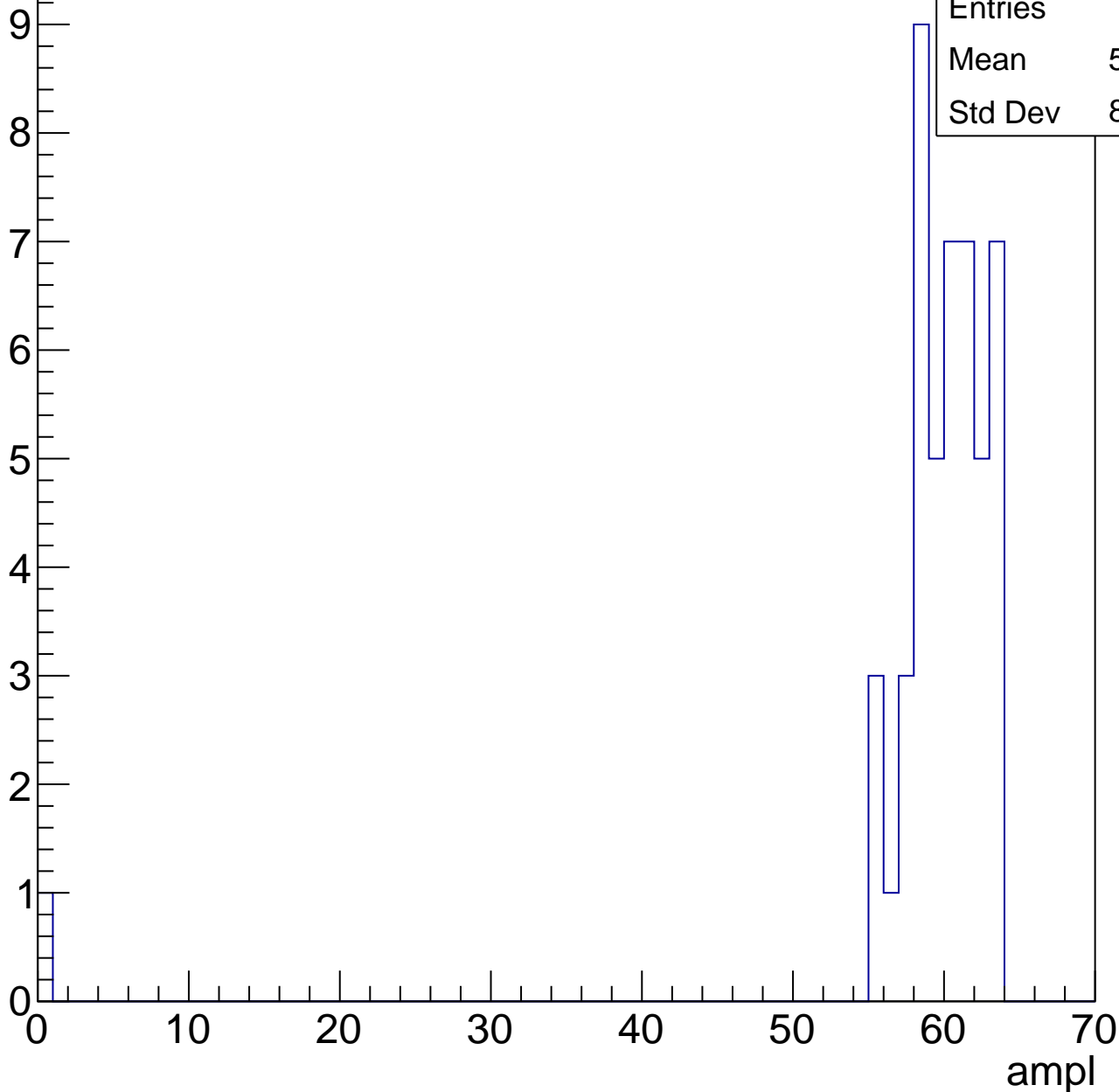
Entries	57
Mean	56.25
Std Dev	3.399

# B1L101S, U20-ch50, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	48
Mean	58.48
Std Dev	8.825



# B1L101S, U20-ch50, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U20-ch50, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U20-ch51, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	60
Mean	30.18
Std Dev	2.79

**Gaus mean : 30.7904**

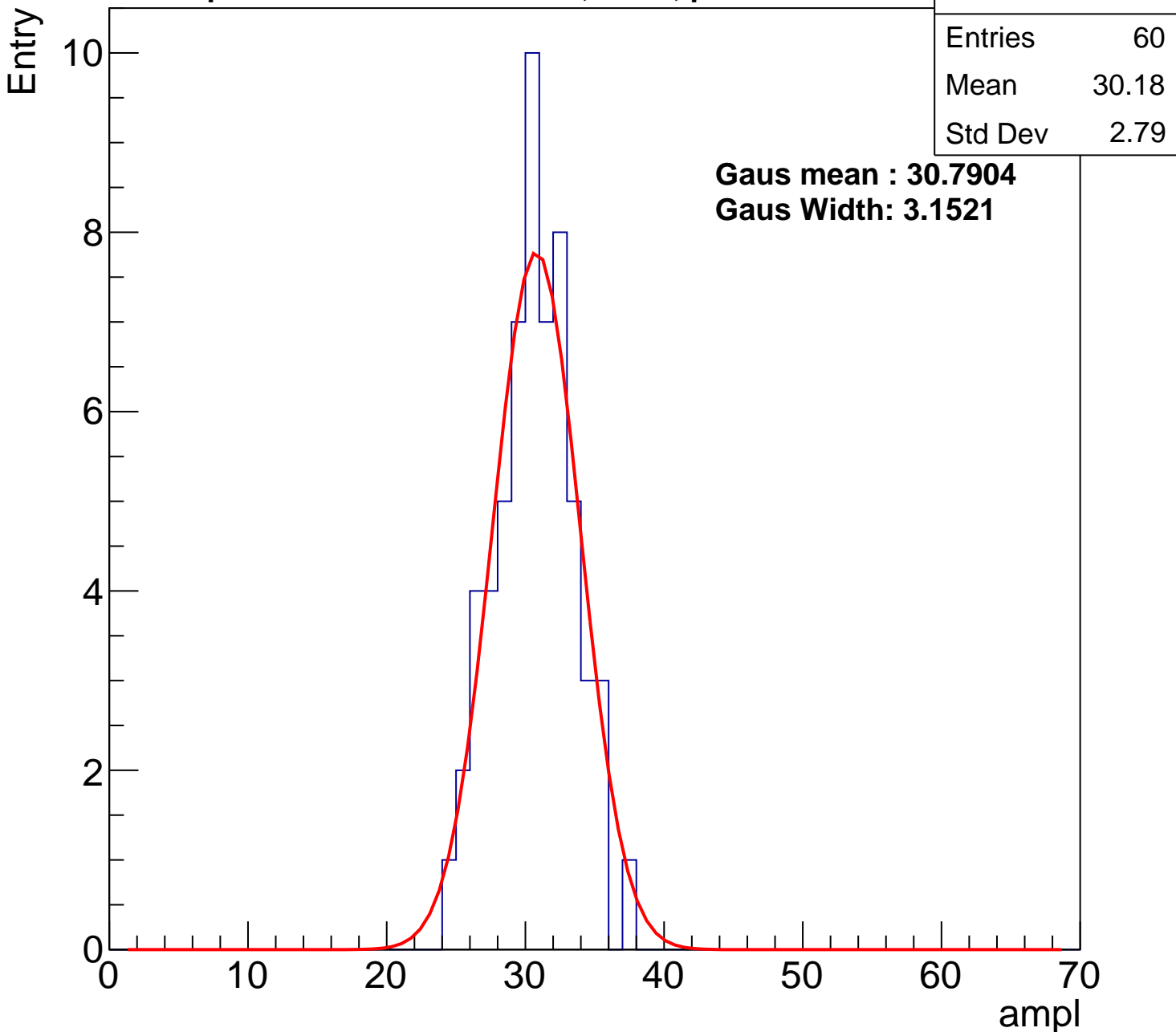
**Gaus Width: 3.1521**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



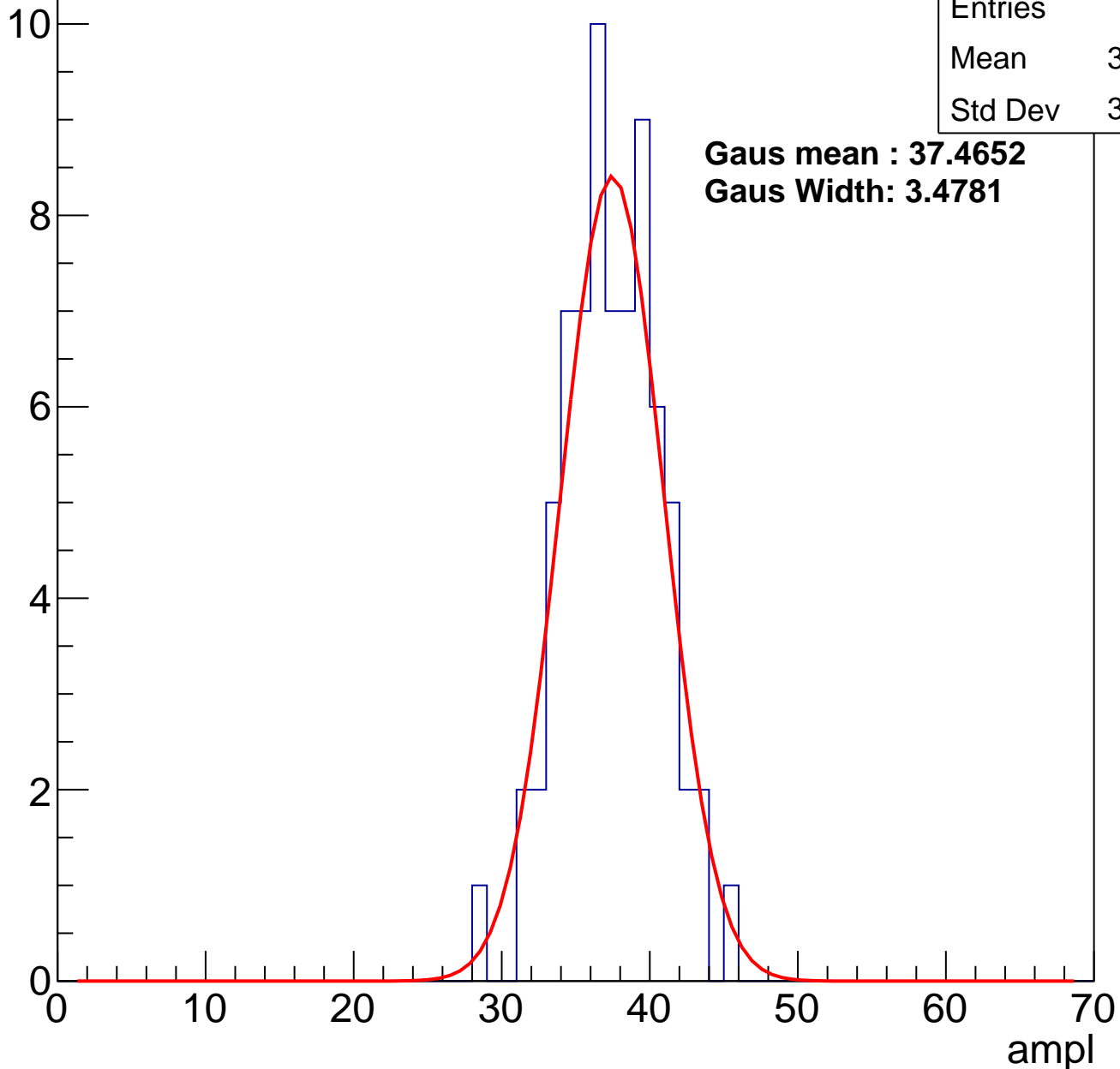
# B1L101S, U20-ch51, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	73
Mean	36.96
Std Dev	3.199

**Gaus mean : 37.4652**  
**Gaus Width: 3.4781**

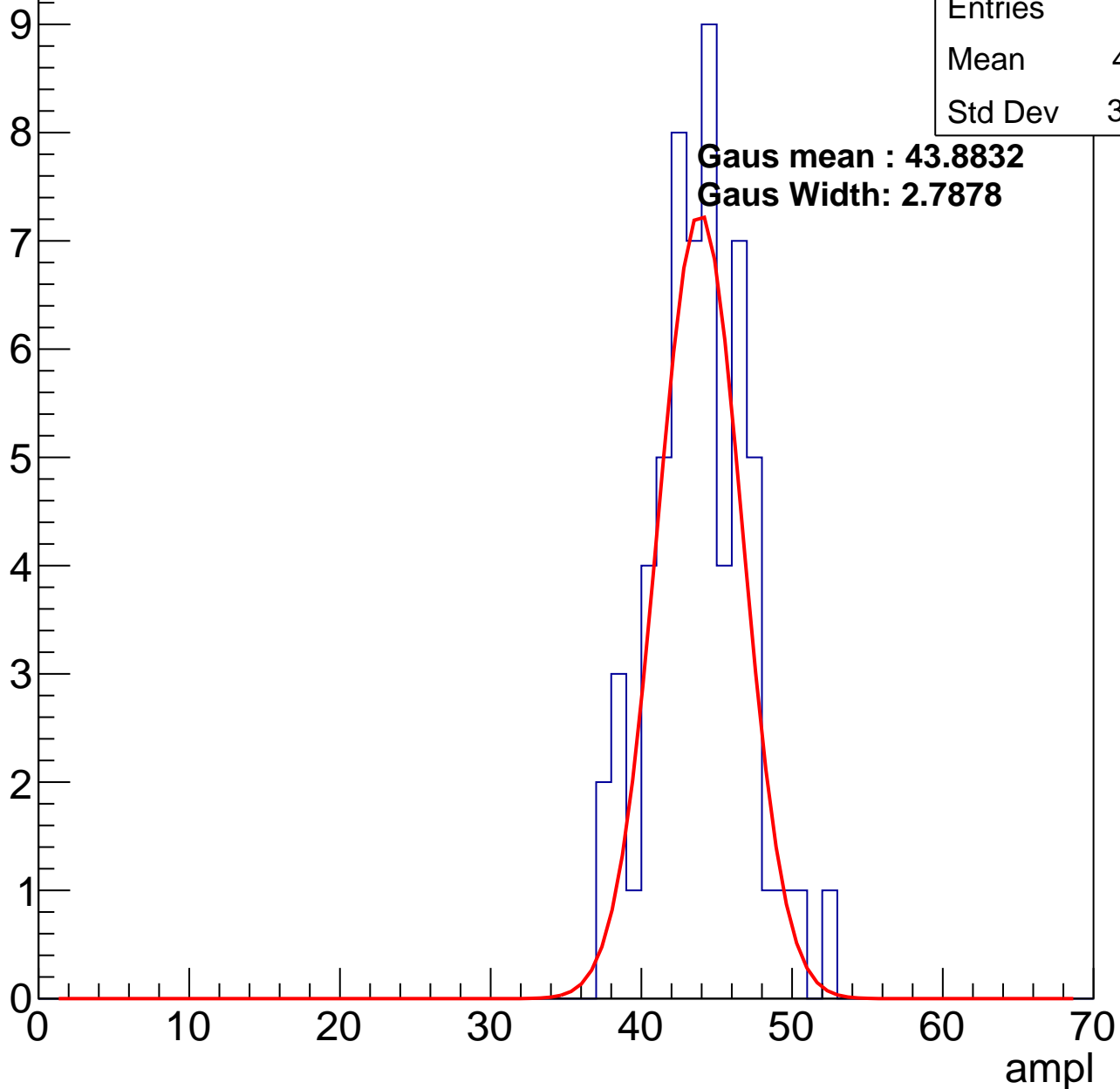
Entry



# B1L101S, U20-ch51, adc2

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

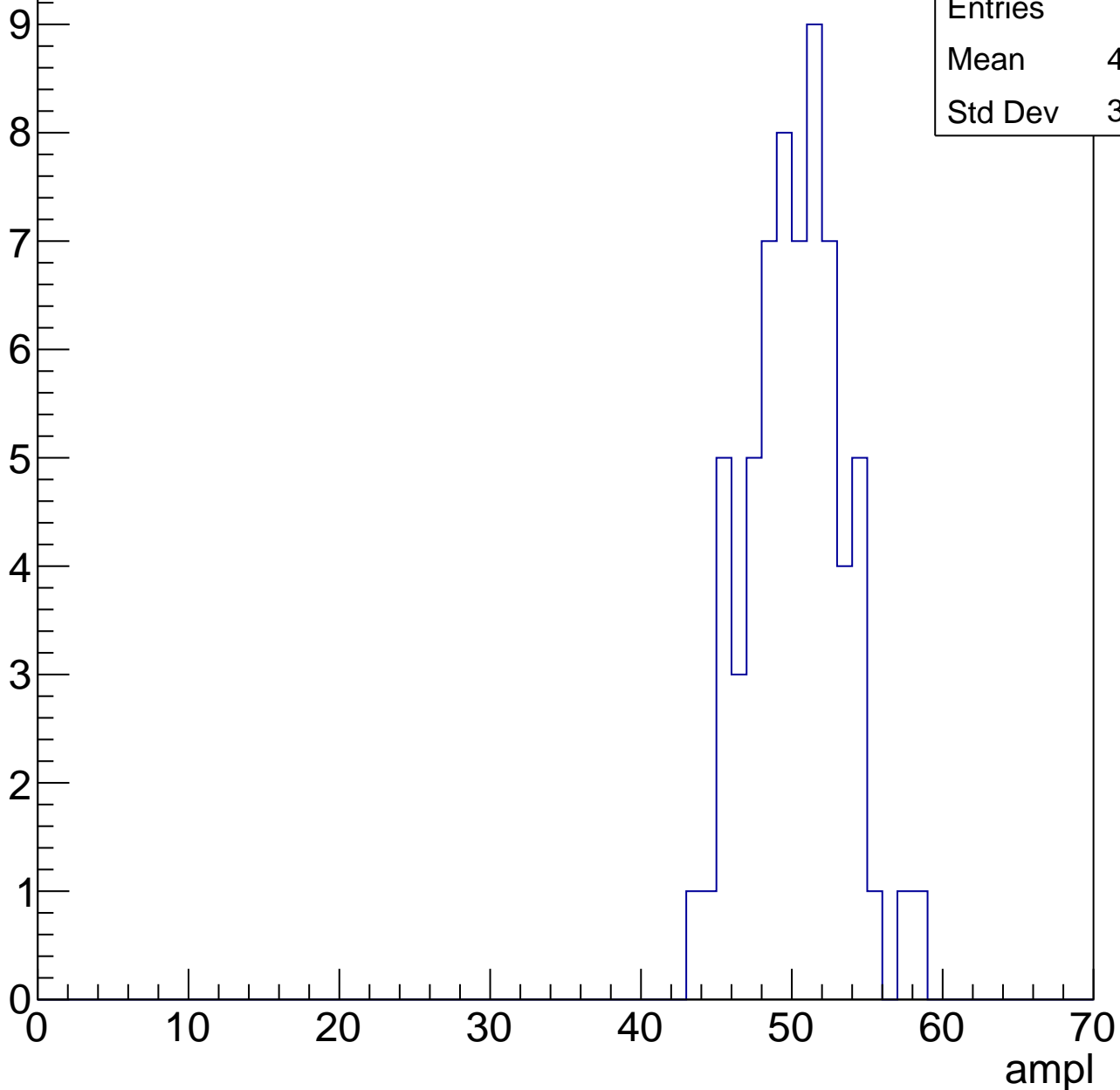


# B1L101S, U20-ch51, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

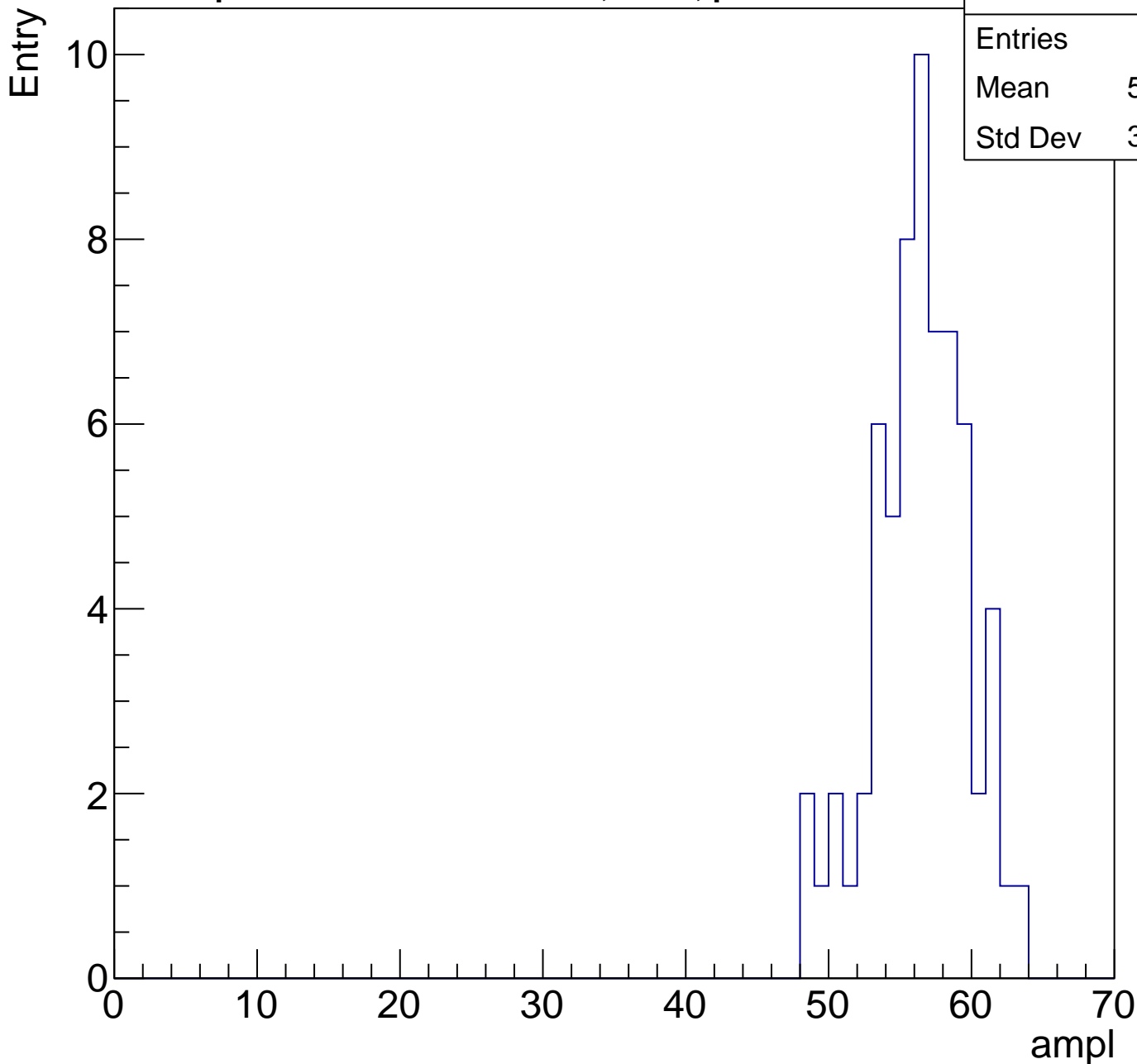
Entries	65
Mean	49.82
Std Dev	3.108



# B1L101S, U20-ch51, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	65
Mean	55.94
Std Dev	3.267

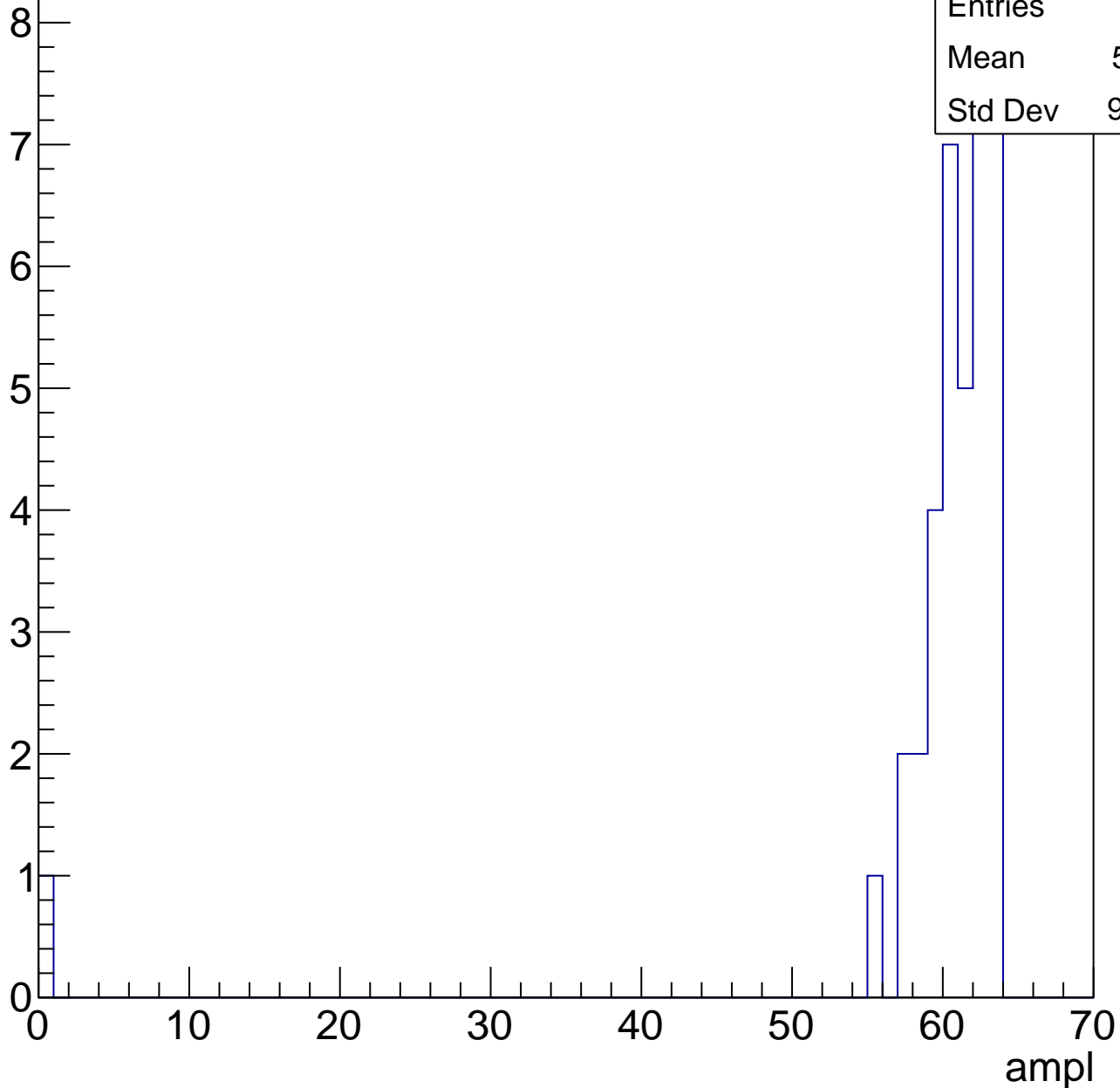


# B1L101S, U20-ch51, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	38
Mean	59.11
Std Dev	9.912



# B1L101S, U20-ch51, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U20-ch51, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	3
Mean	8
Std Dev	11.31

# B1L101S, U20-ch52, adc0

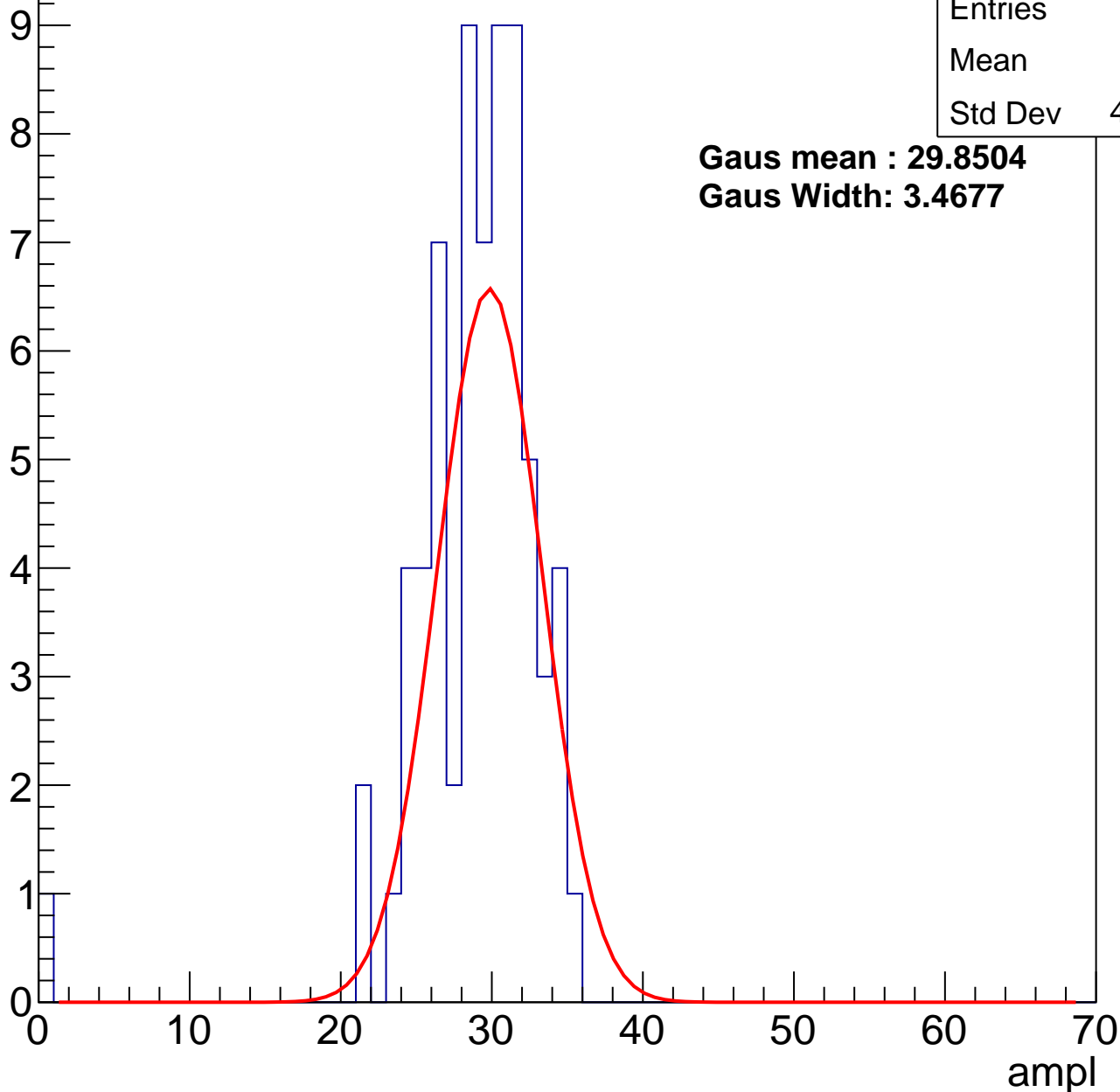
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	28.4
Std Dev	4.694

**Gaus mean : 29.8504**

**Gaus Width: 3.4677**



# B1L101S, U20-ch52, adc1

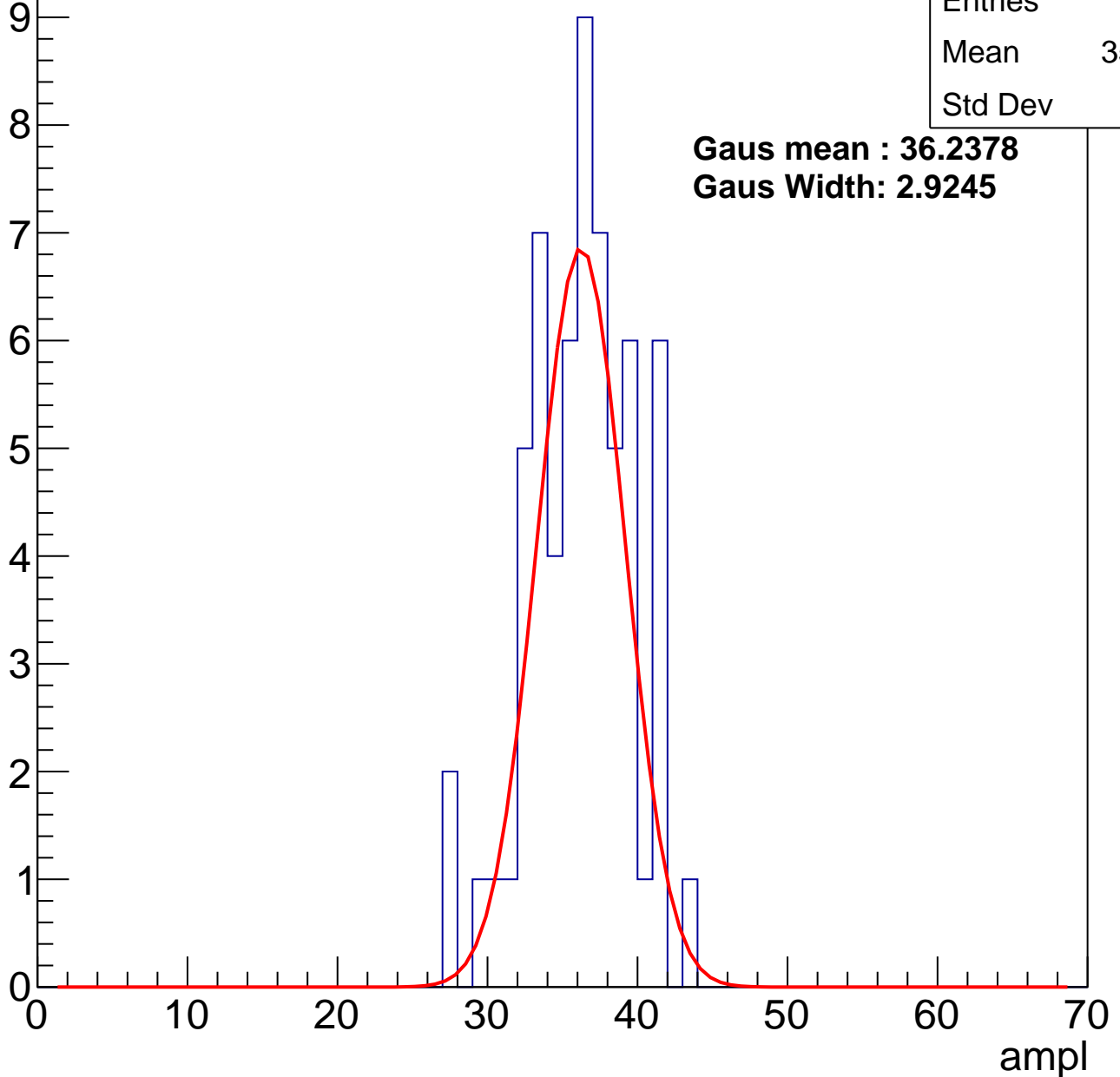
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	35.76
Std Dev	3.43

**Gaus mean : 36.2378**

**Gaus Width: 2.9245**



# B1L101S, U20-ch52, adc2

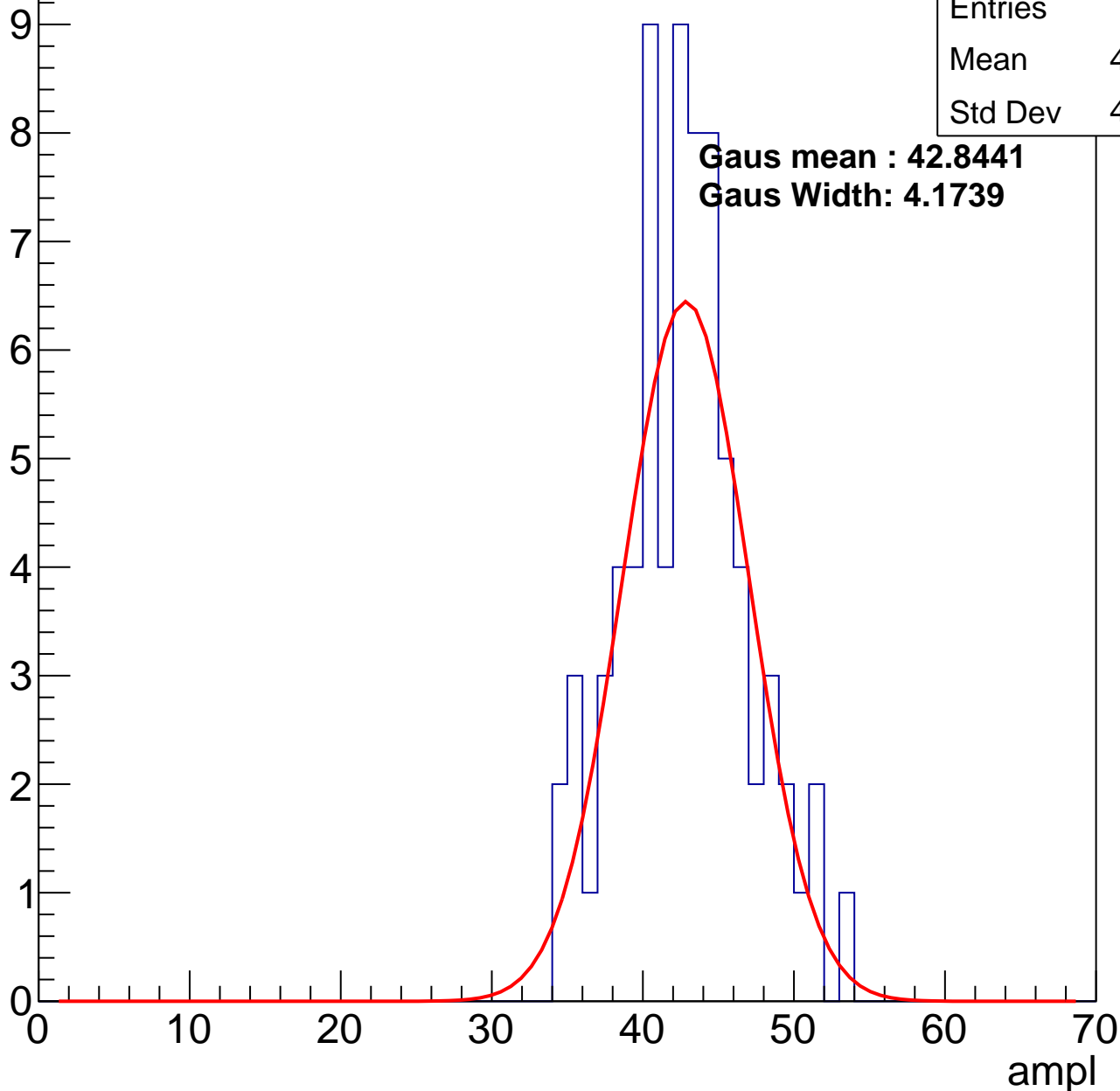
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	75
Mean	42.35
Std Dev	4.113

**Gaus mean : 42.8441**

**Gaus Width: 4.1739**

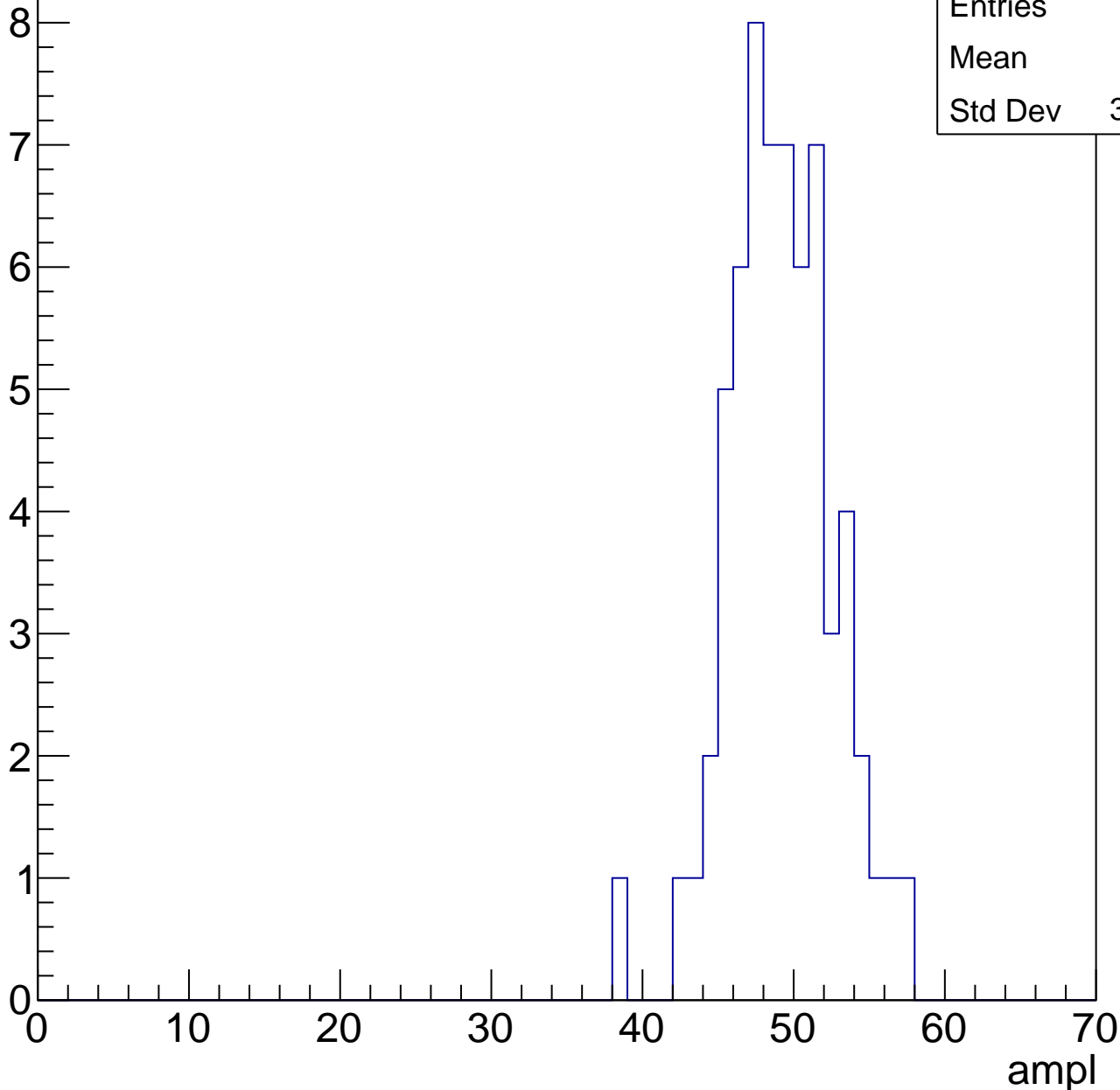


# B1L101S, U20-ch52, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	48.7
Std Dev	3.444

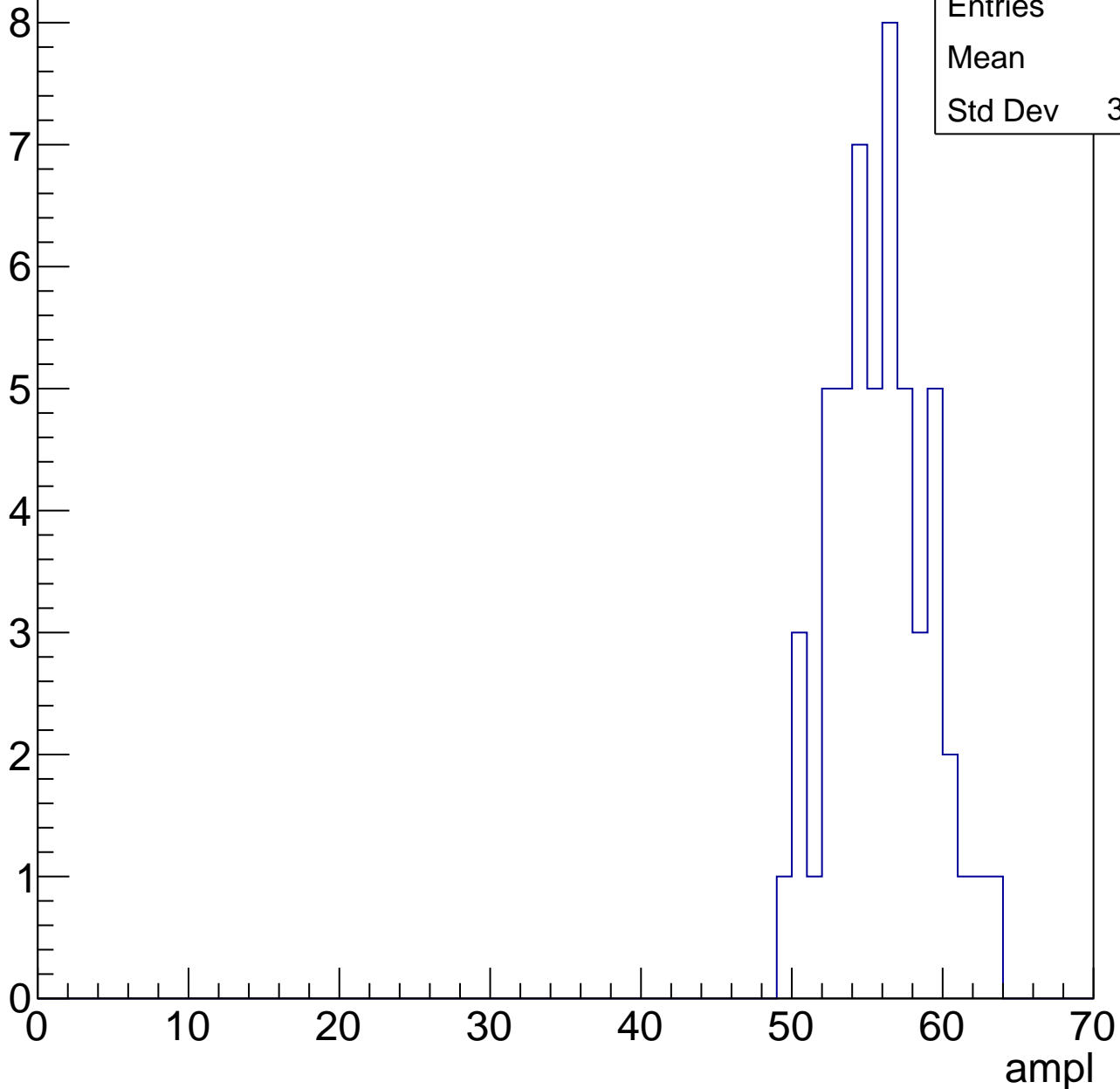


# B1L101S, U20-ch52, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

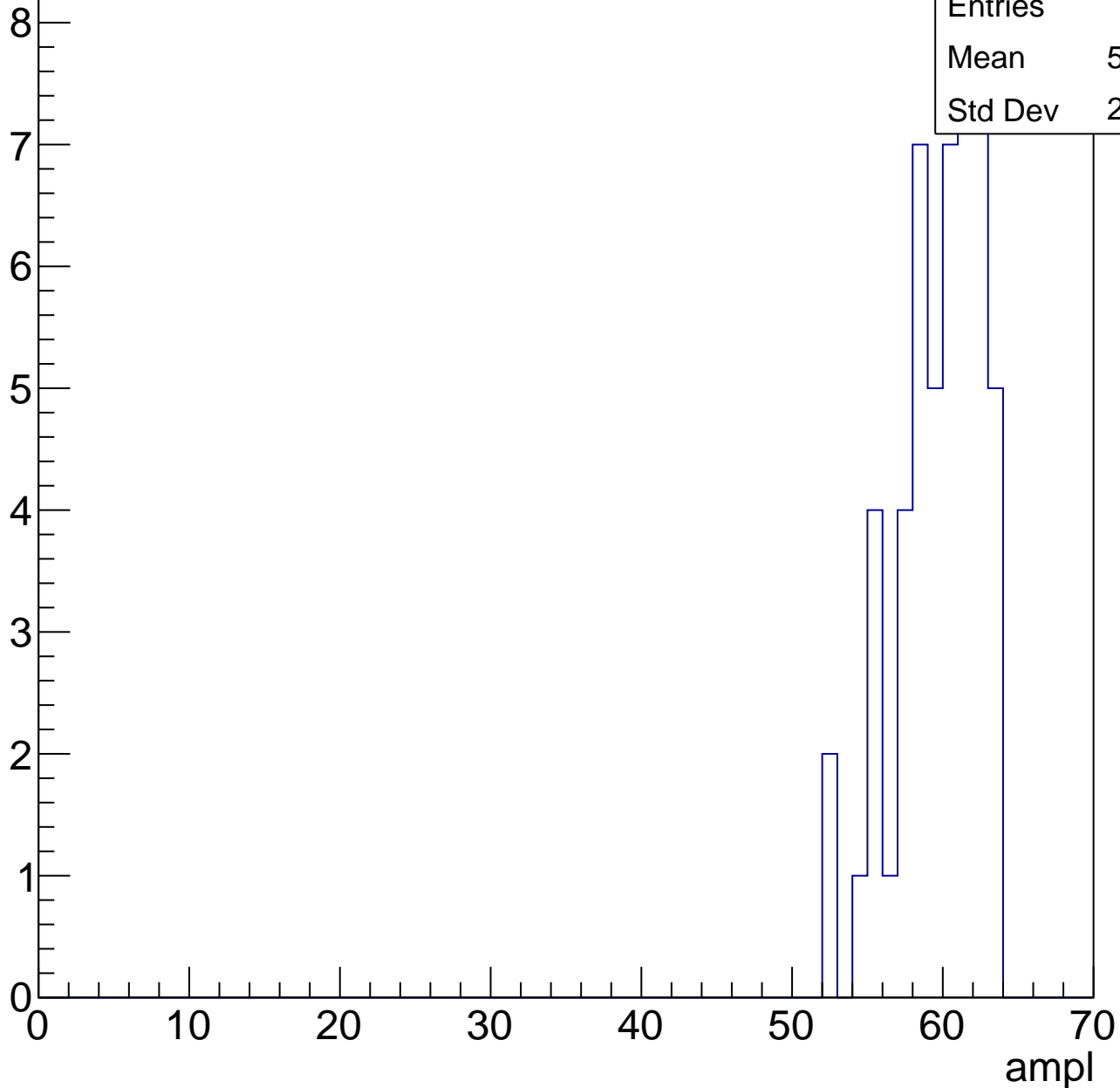
Entries	53
Mean	55.4
Std Dev	3.146



# B1L101S, U20-ch52, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

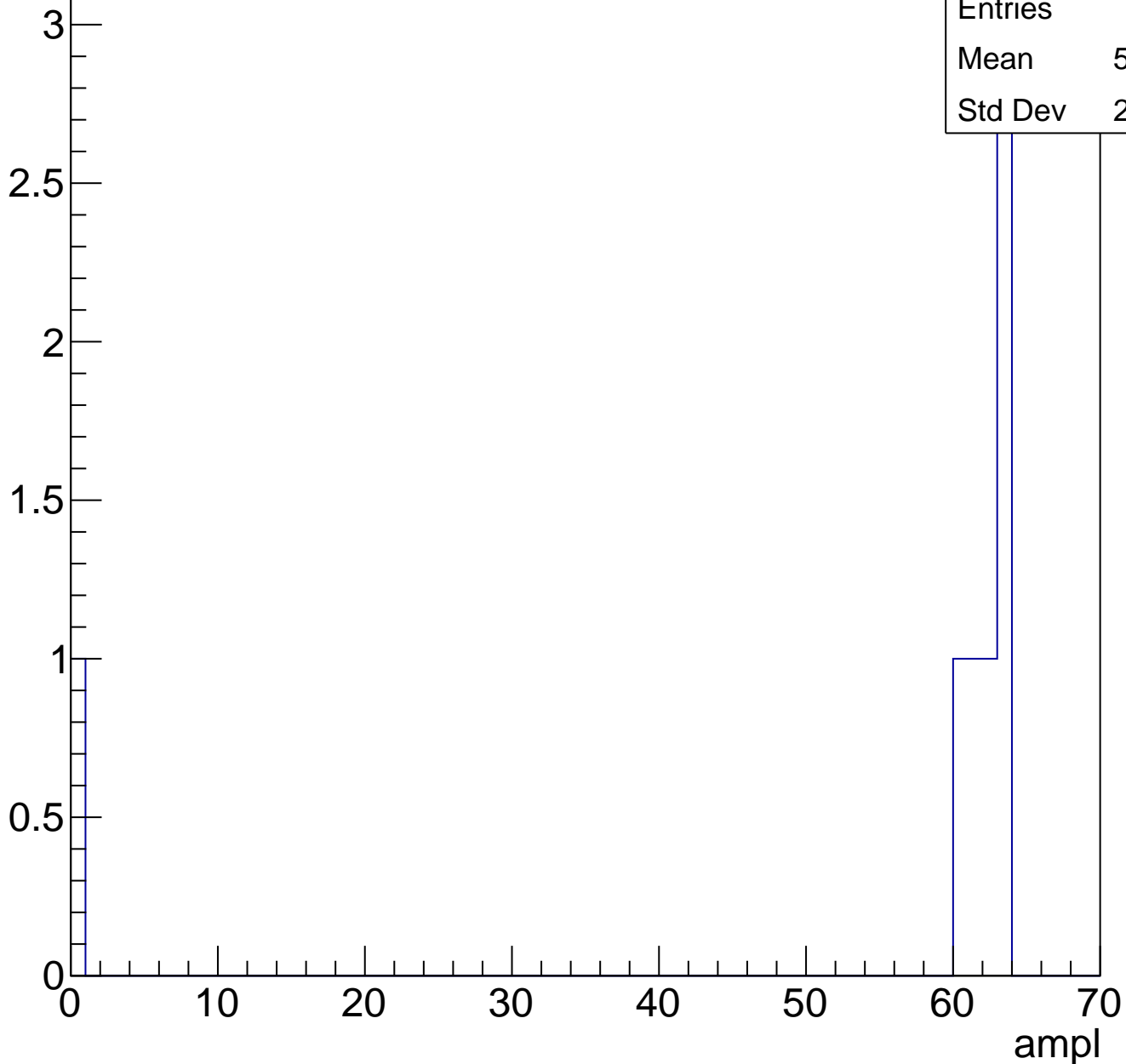
Entry



# B1L101S, U20-ch52, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U20-ch52, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U20-ch53, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

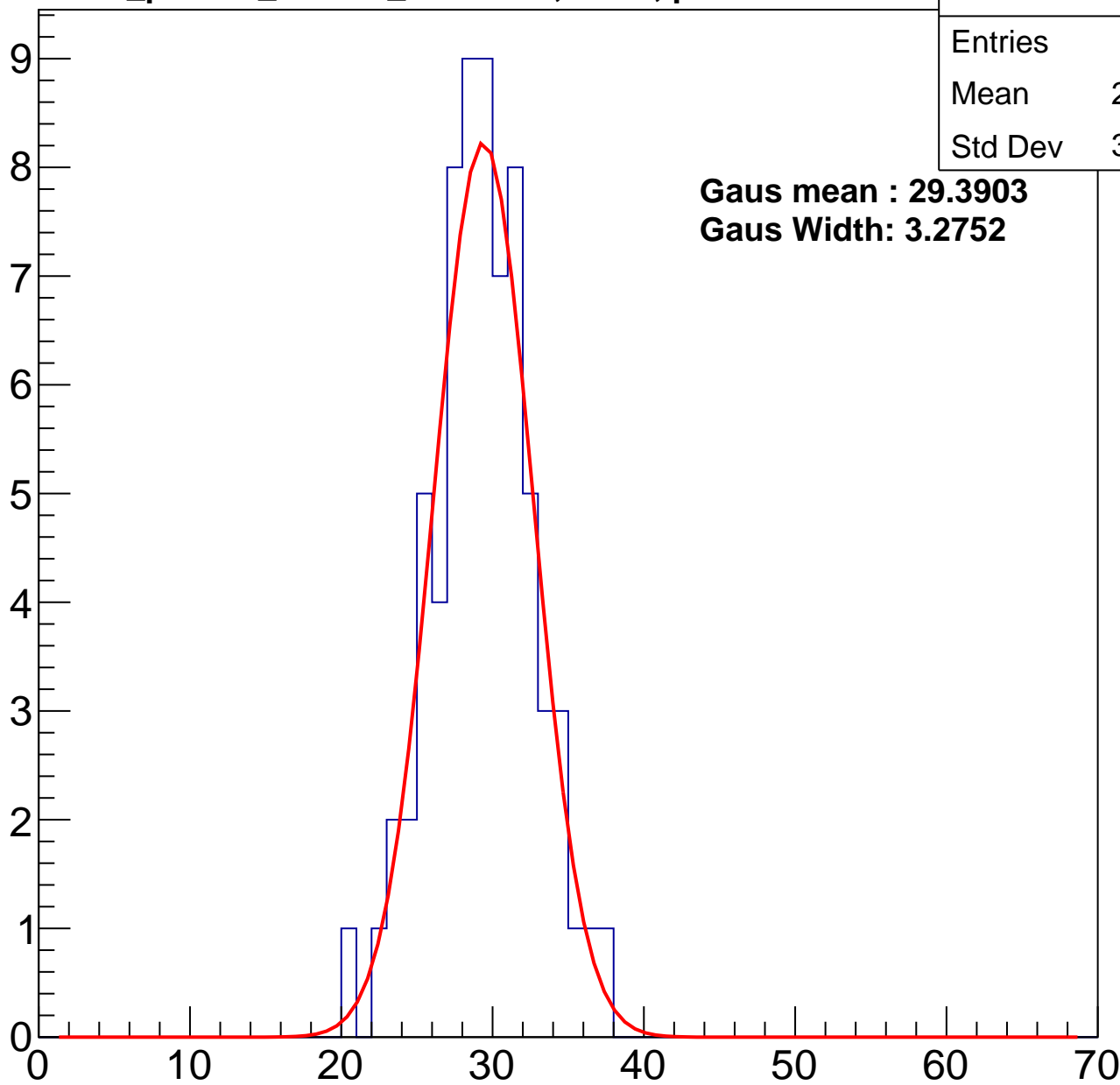
9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	70
Mean	28.87
Std Dev	3.303

**Gaus mean : 29.3903**

**Gaus Width: 3.2752**

ampl



# B1L101S, U20-ch53, adc1

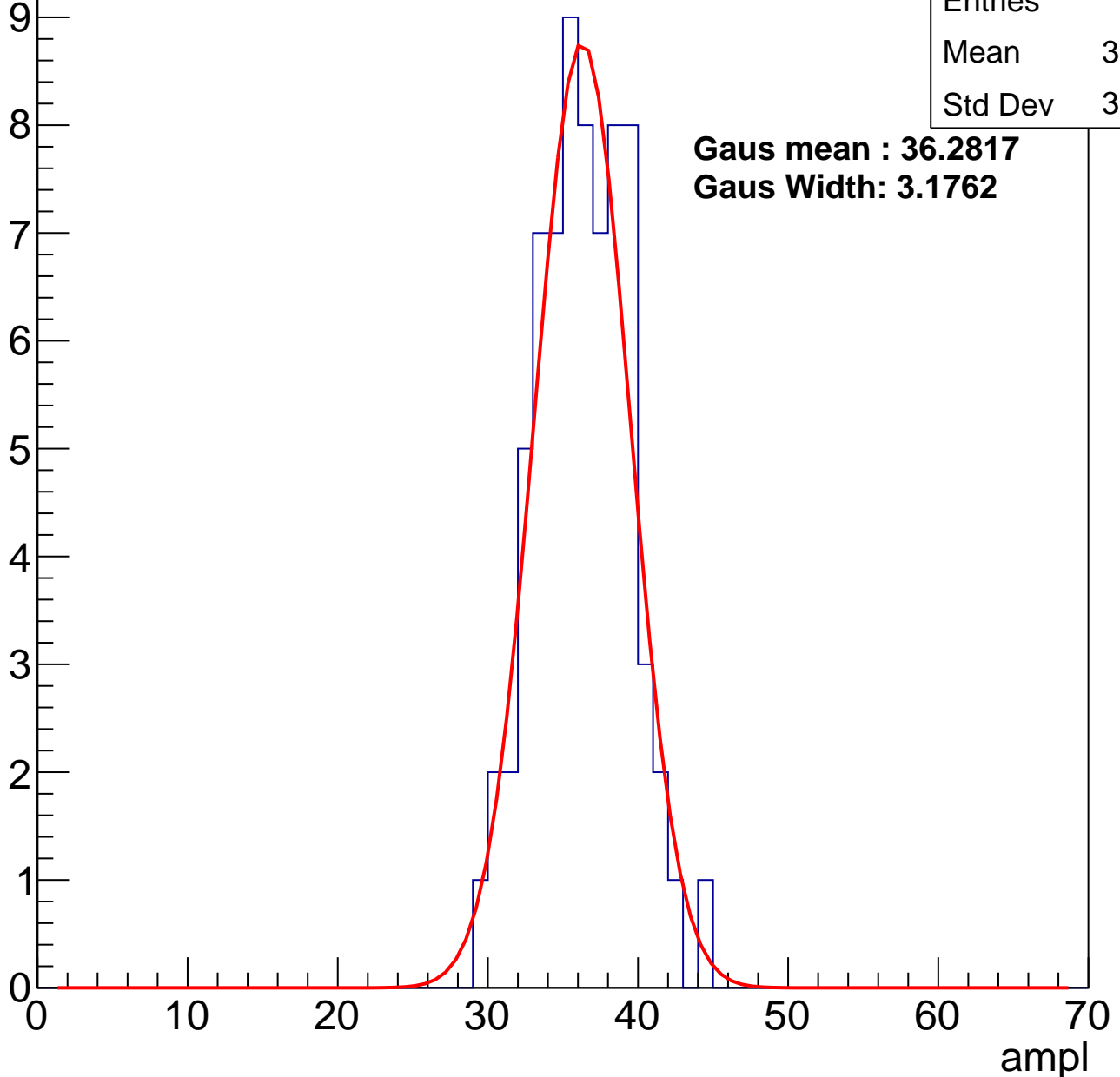
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	71
Mean	35.86
Std Dev	3.046

**Gaus mean : 36.2817**

**Gaus Width: 3.1762**



# B1L101S, U20-ch53, adc2

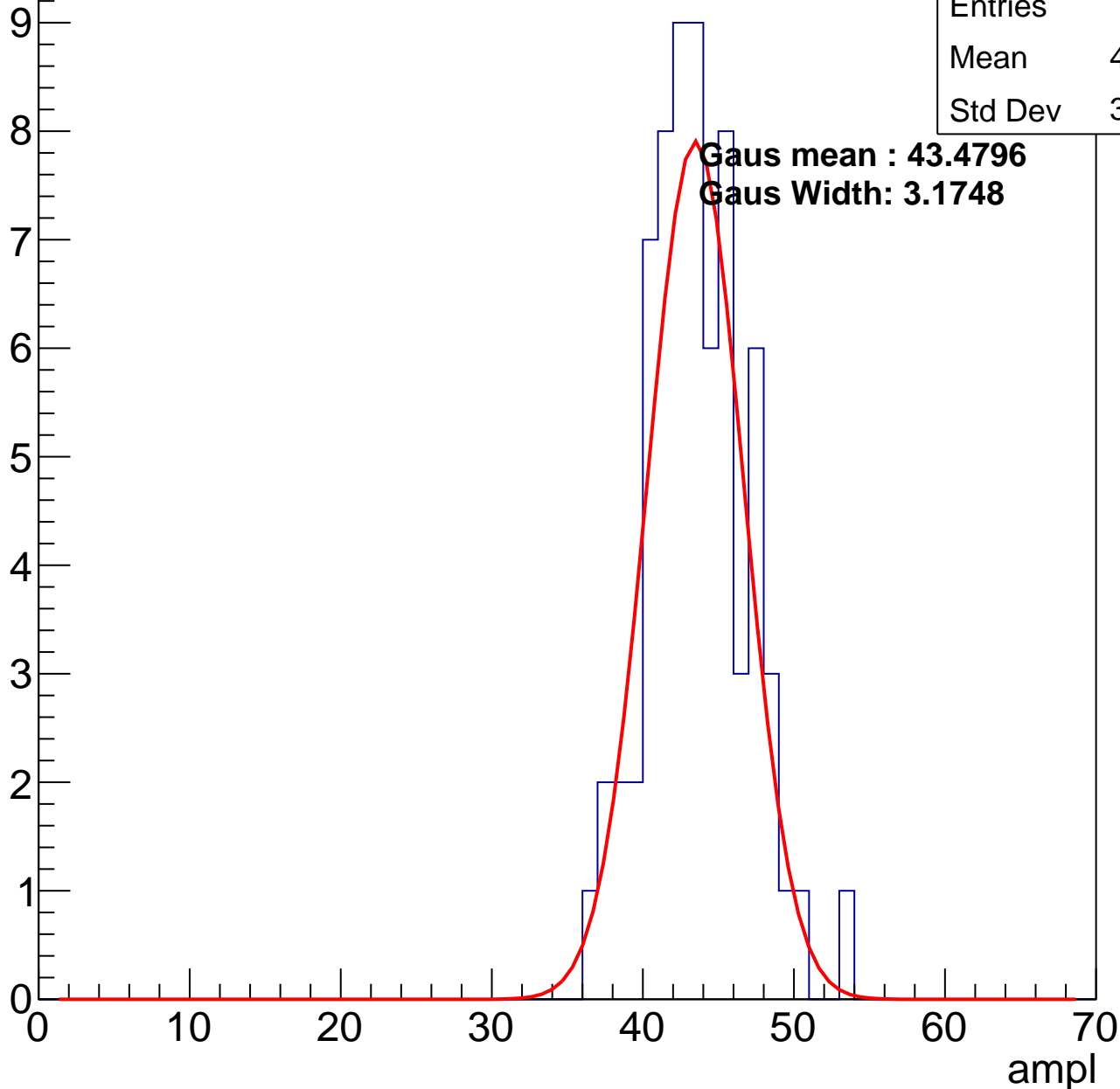
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	43.14
Std Dev	3.245

**Gaus mean : 43.4796**

**Gaus Width: 3.1748**

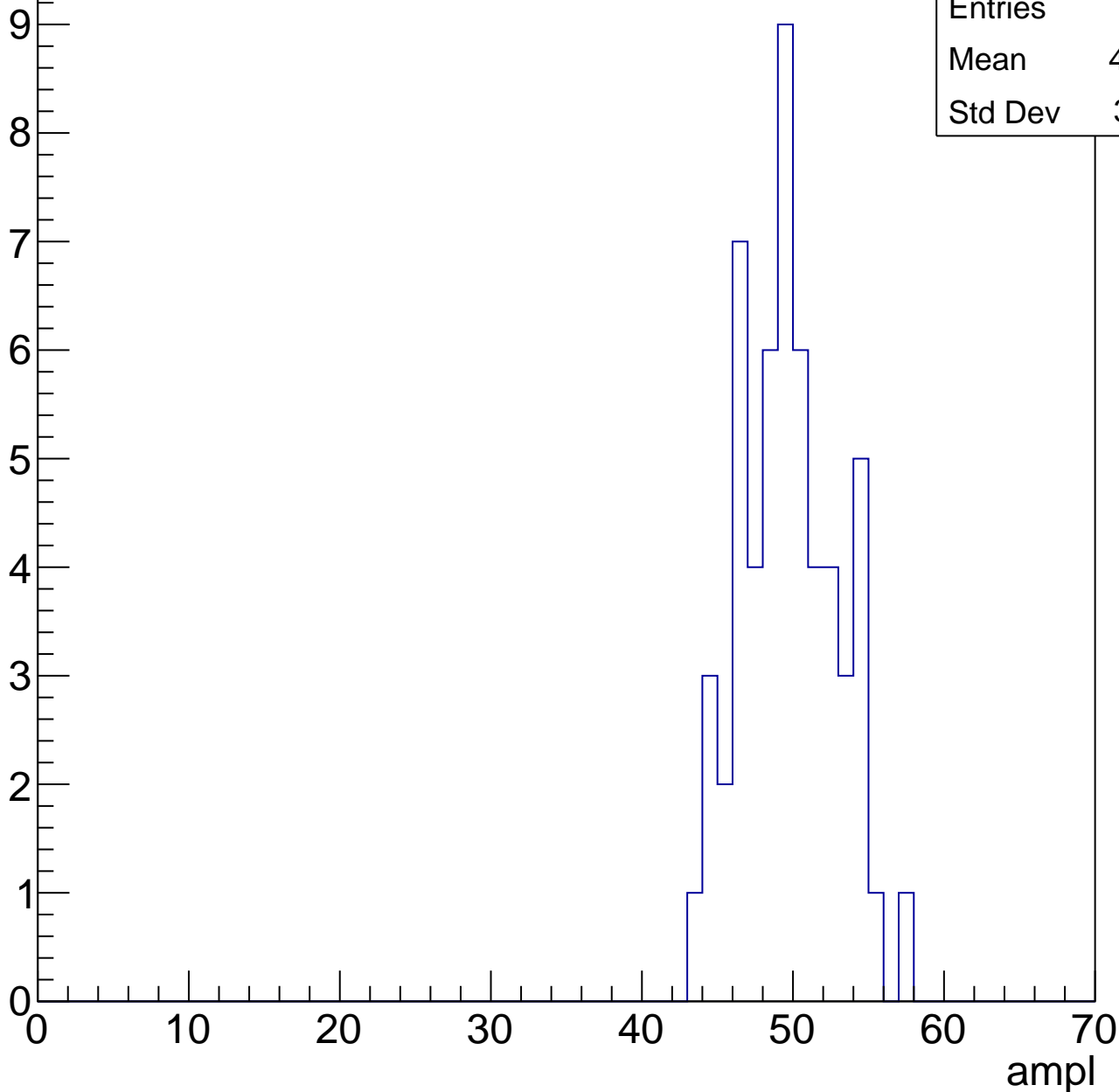


# B1L101S, U20-ch53, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	56
Mean	49.23
Std Dev	3.151

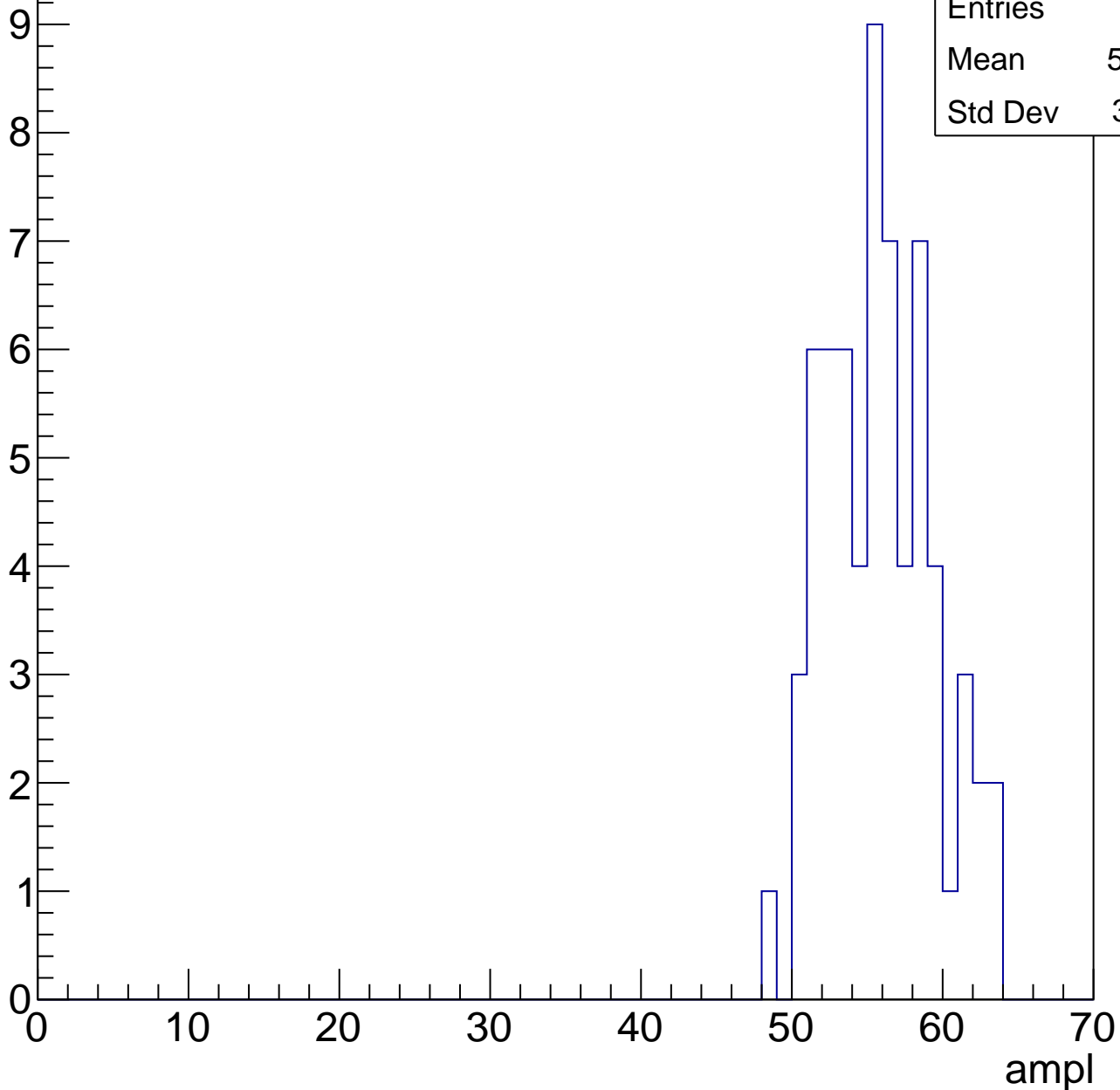


# B1L101S, U20-ch53, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	55.38
Std Dev	3.511

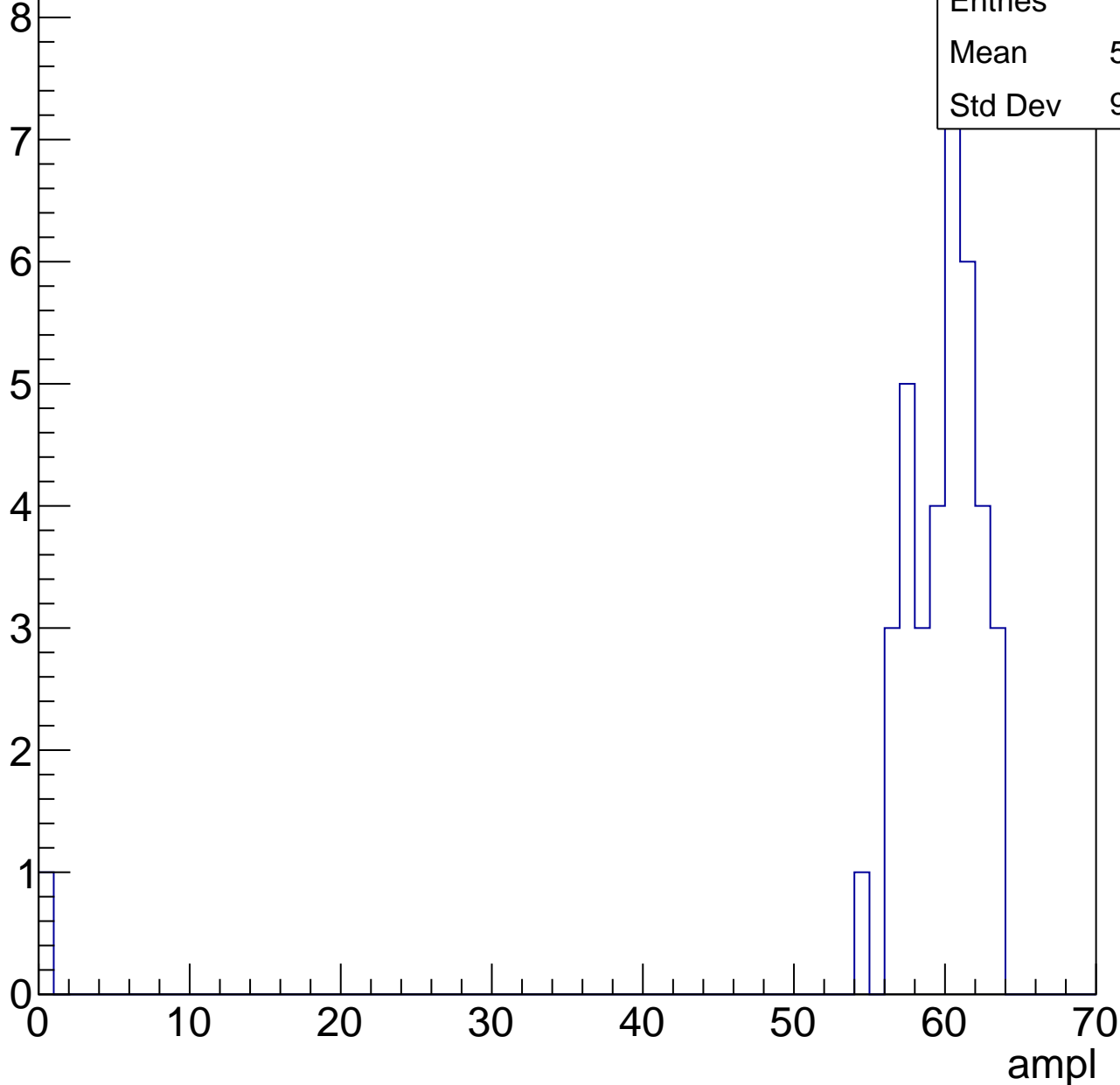


# B1L101S, U20-ch53, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	38
Mean	57.89
Std Dev	9.768

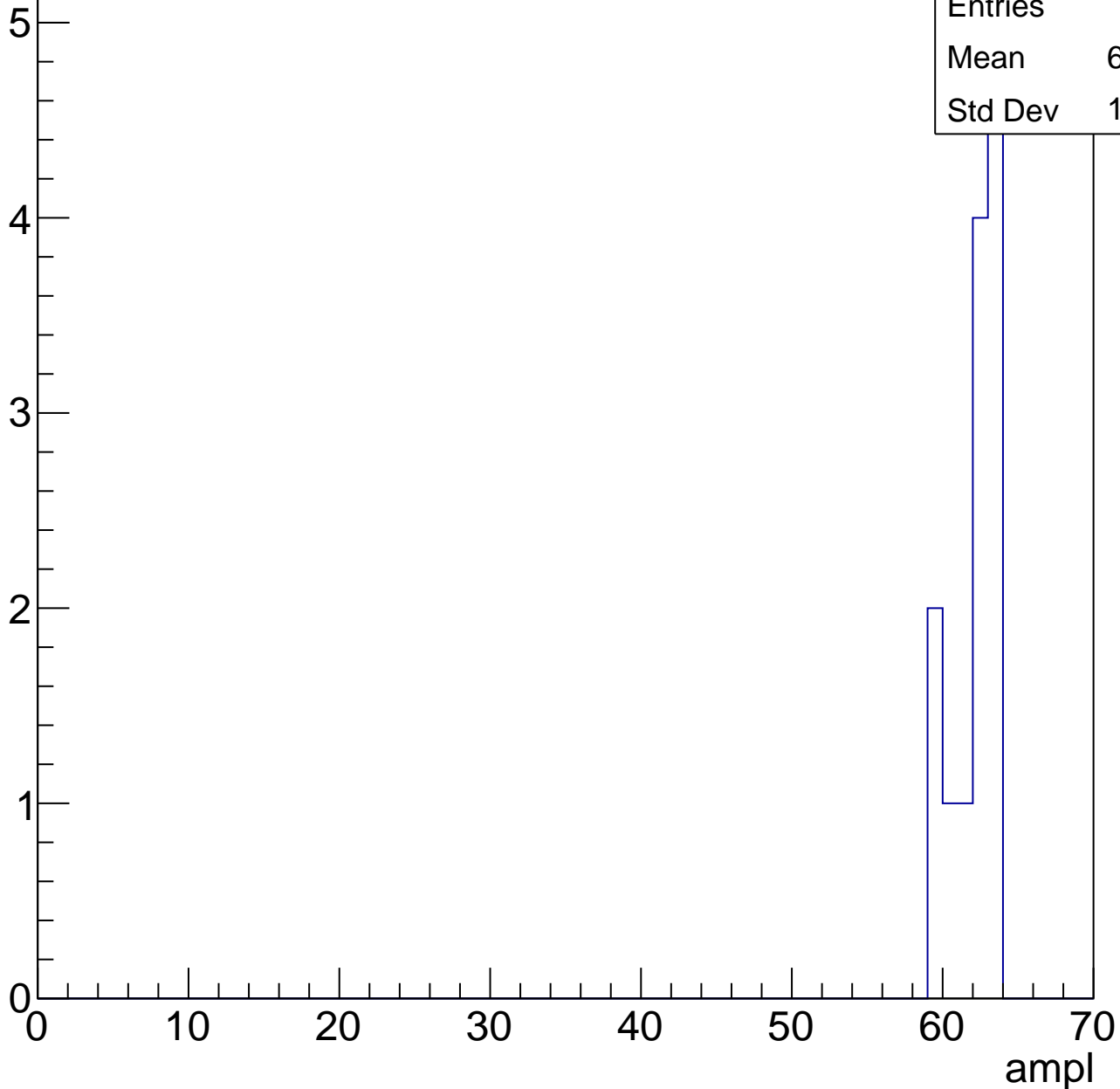


# B1L101S, U20-ch53, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	13
Mean	61.69
Std Dev	1.435





# B1L101S, U20-ch53, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U20-ch54, adc0

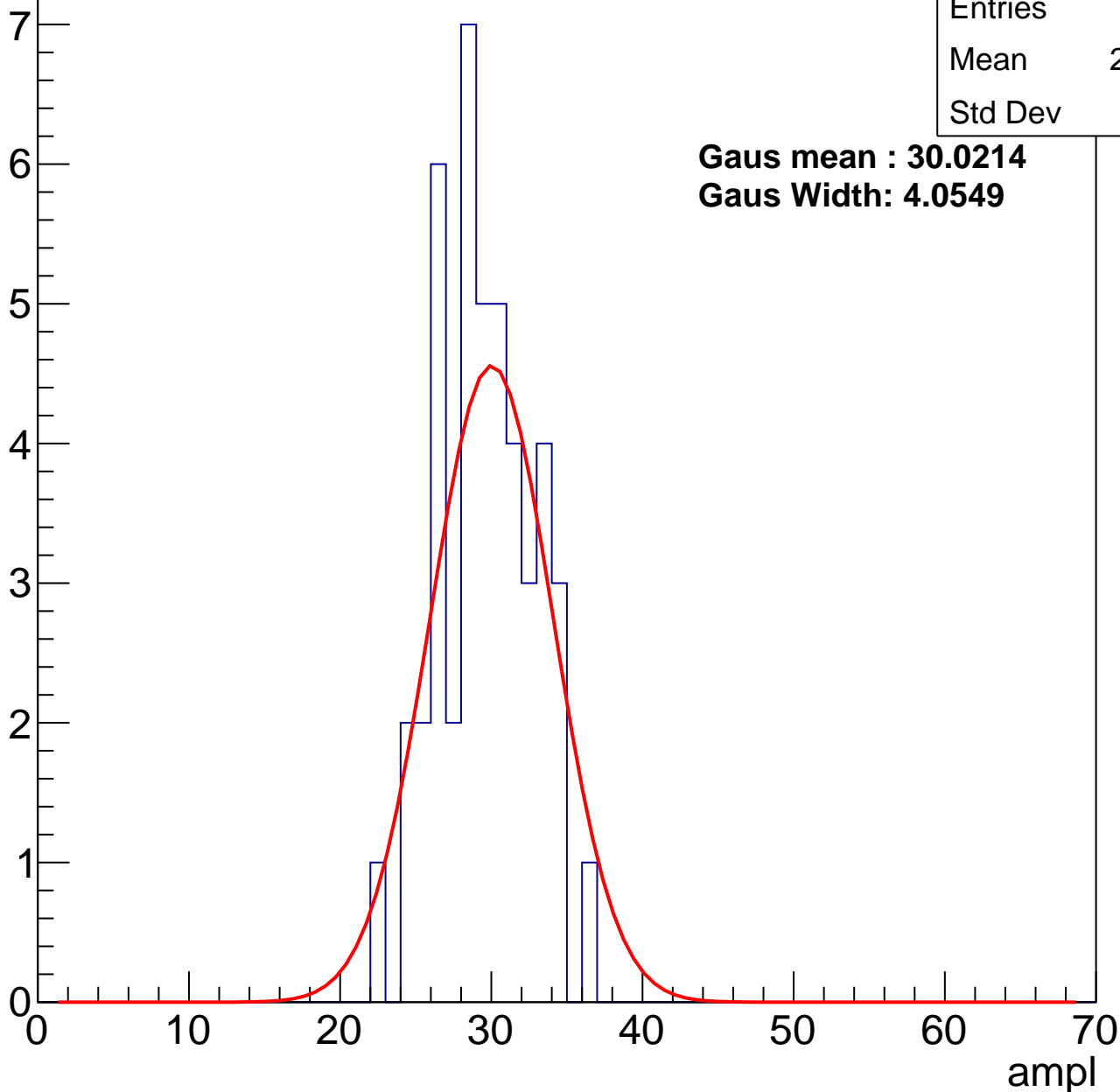
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	45
Mean	29.13
Std Dev	3.11

**Gaus mean : 30.0214**

**Gaus Width: 4.0549**



# B1L101S, U20-ch54, adc1

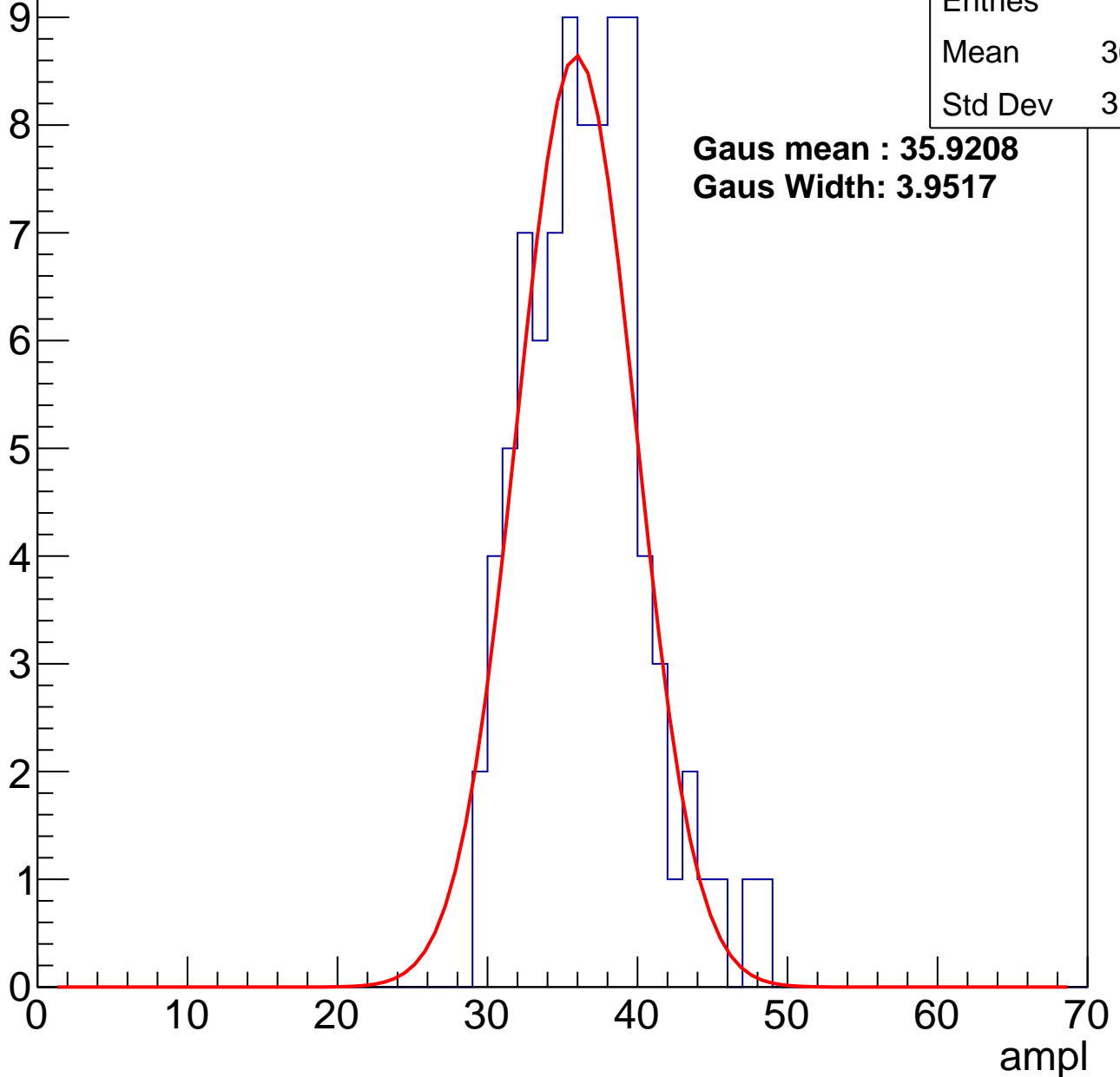
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	88
Mean	36.14
Std Dev	3.955

**Gaus mean : 35.9208**

**Gaus Width: 3.9517**



# B1L101S, U20-ch54, adc2

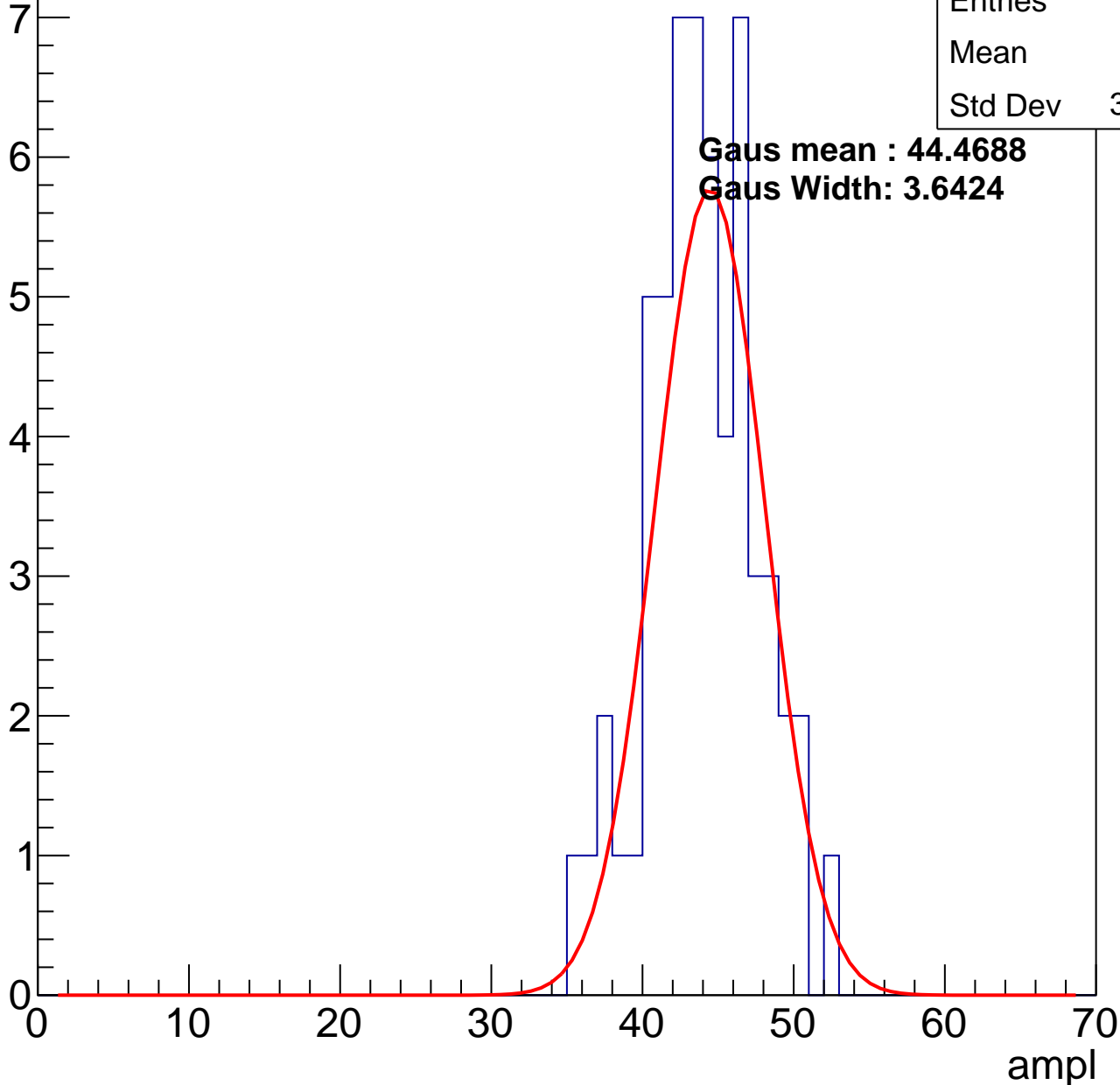
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	58
Mean	43.5
Std Dev	3.578

**Gaus mean : 44.4688**

**Gaus Width: 3.6424**

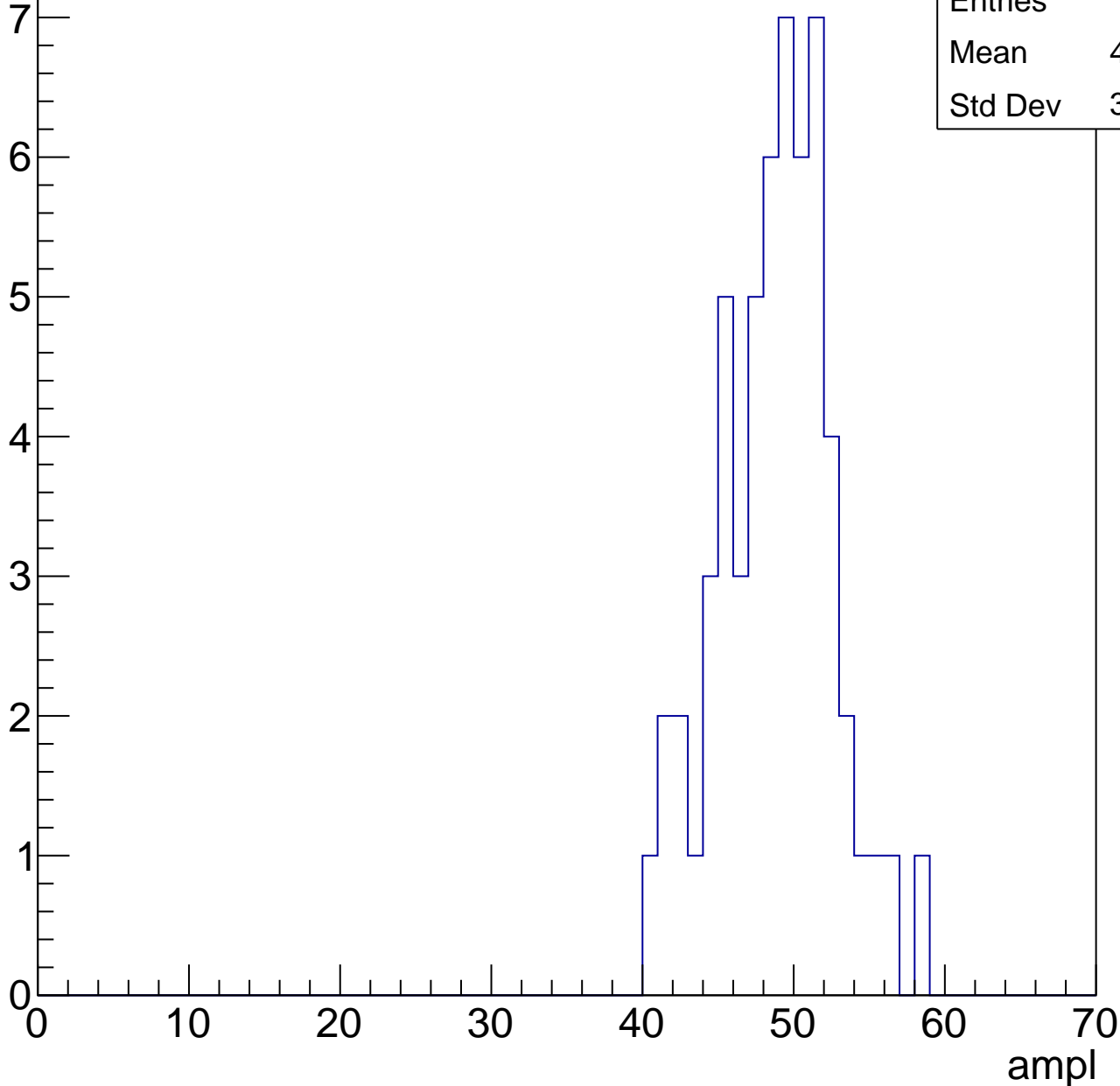


# B1L101S, U20-ch54, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	58
Mean	48.34
Std Dev	3.758

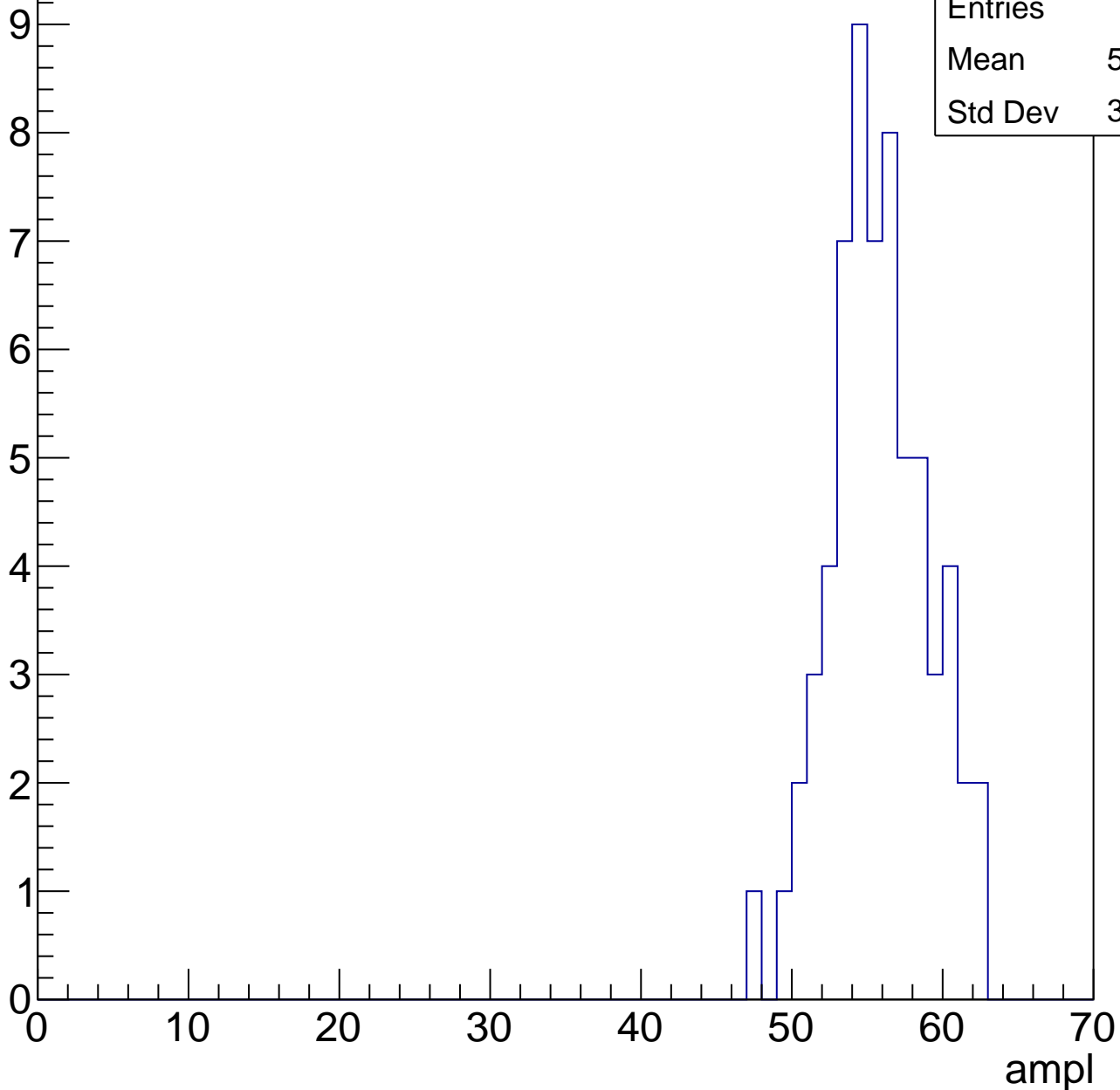


# B1L101S, U20-ch54, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	55.32
Std Dev	3.226

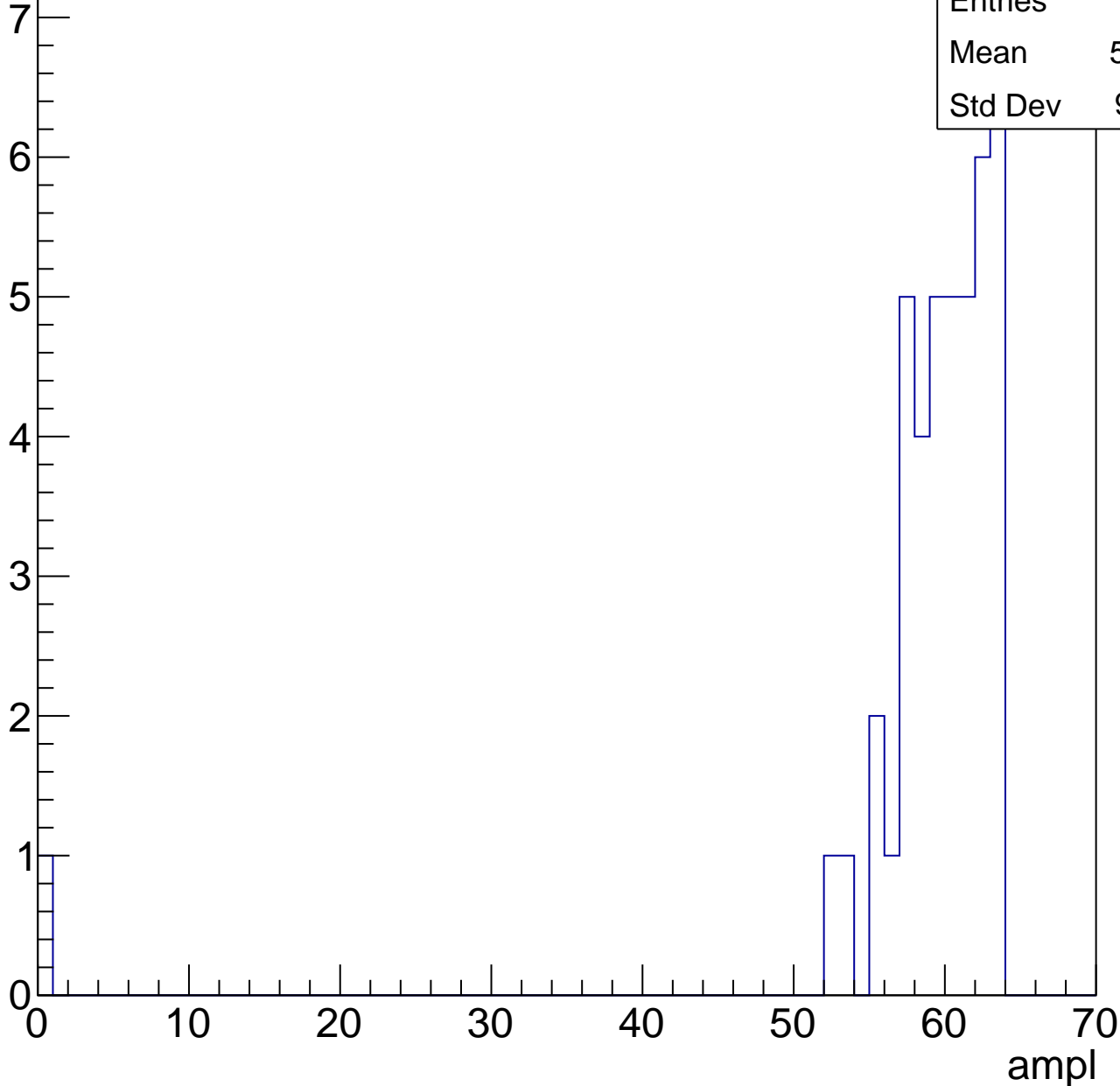


# B1L101S, U20-ch54, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	43
Mean	58.16
Std Dev	9.391



# B1L101S, U20-ch54, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

3

2.5

2

1.5

1

0.5

0

Entries

11

Mean

61.27

Std Dev

1.42

ampl

0 10 20 30 40 50 60 70



# B1L101S, U20-ch54, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U20-ch55, adc0

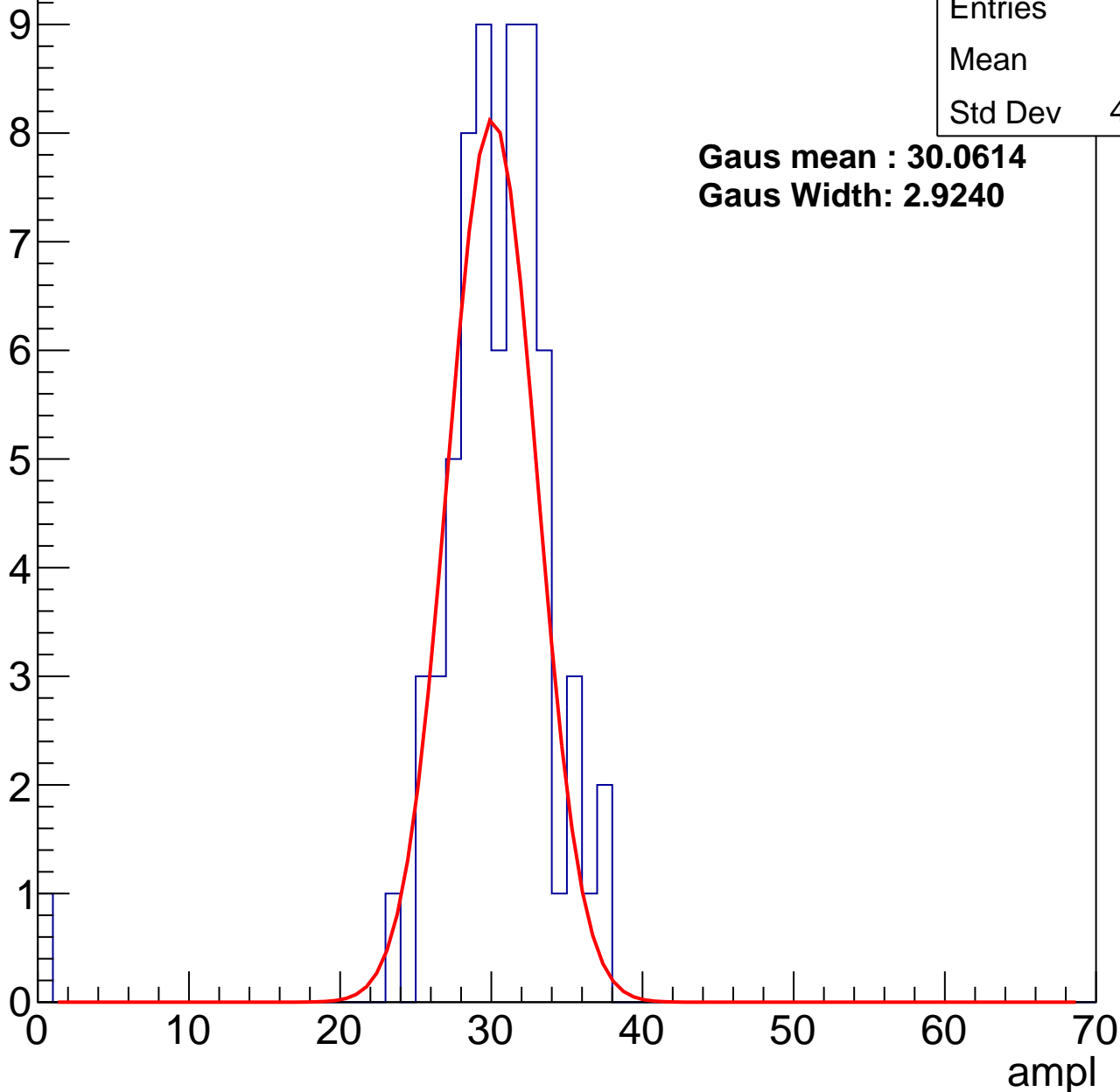
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	67
Mean	29.7
Std Dev	4.694

**Gaus mean : 30.0614**

**Gaus Width: 2.9240**



# B1L101S, U20-ch55, adc1

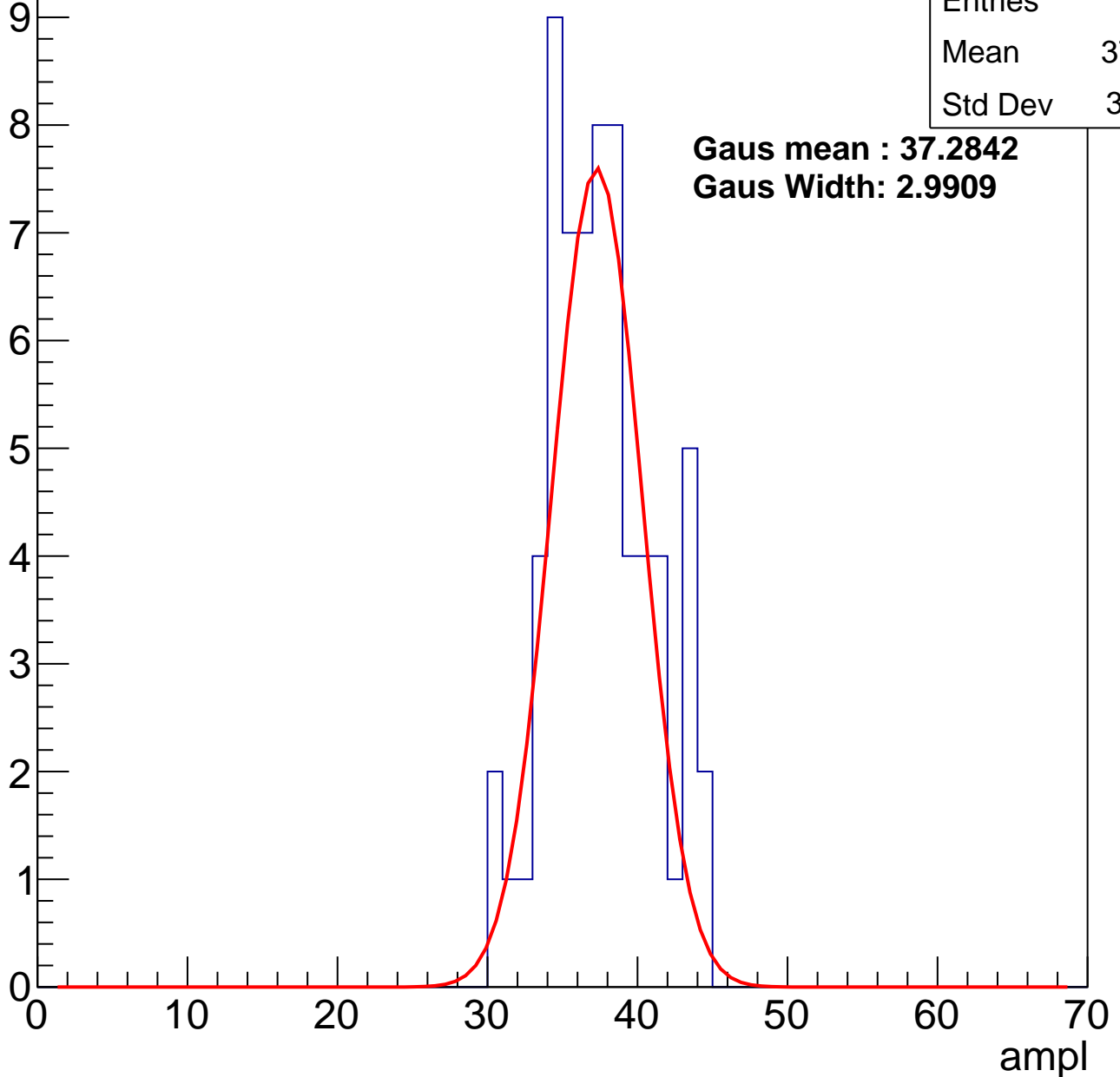
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	67
Mean	37.06
Std Dev	3.381

**Gaus mean : 37.2842**

**Gaus Width: 2.9909**



# B1L101S, U20-ch55, adc2

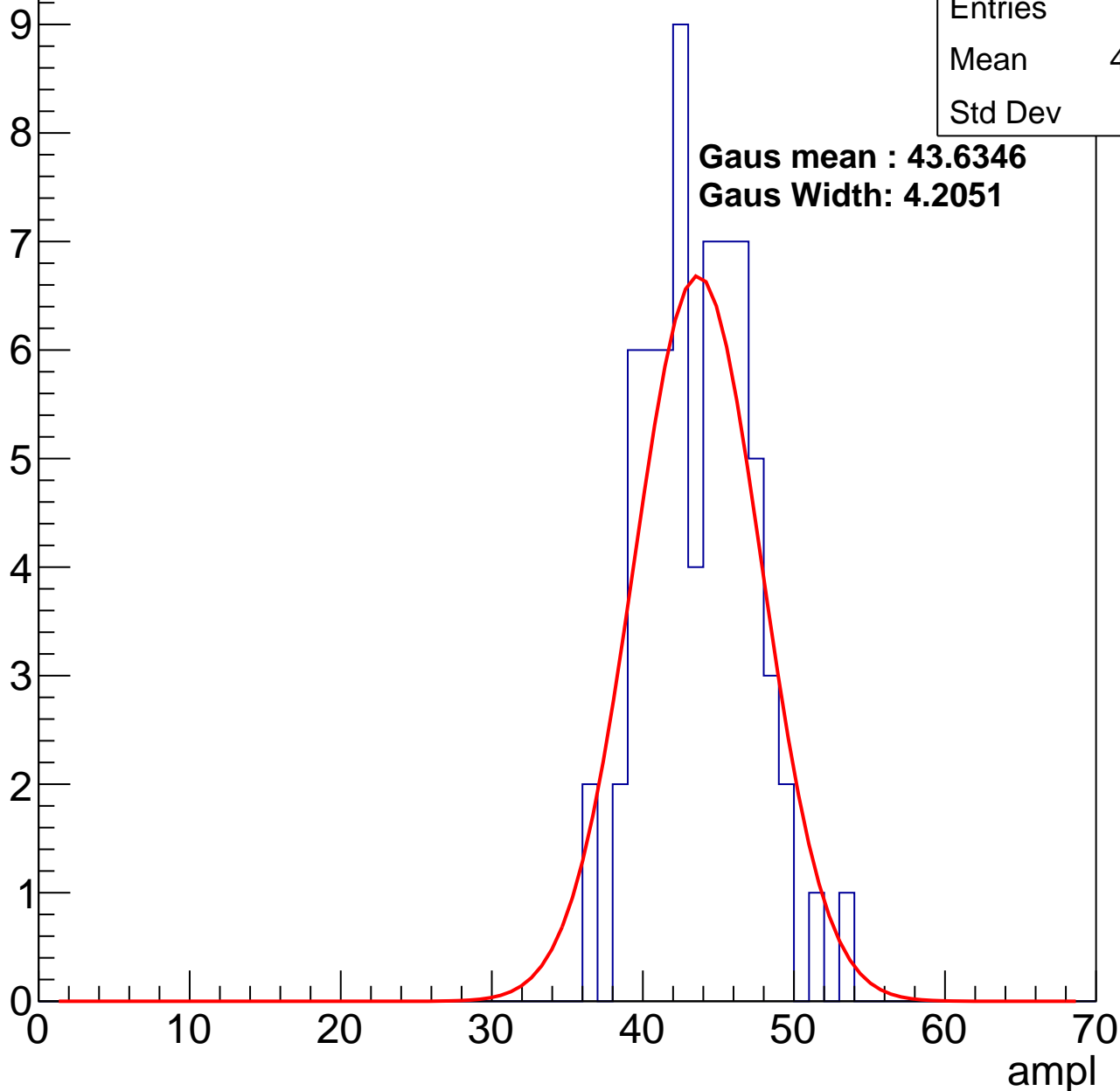
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	43.29
Std Dev	3.46

**Gaus mean : 43.6346**

**Gaus Width: 4.2051**

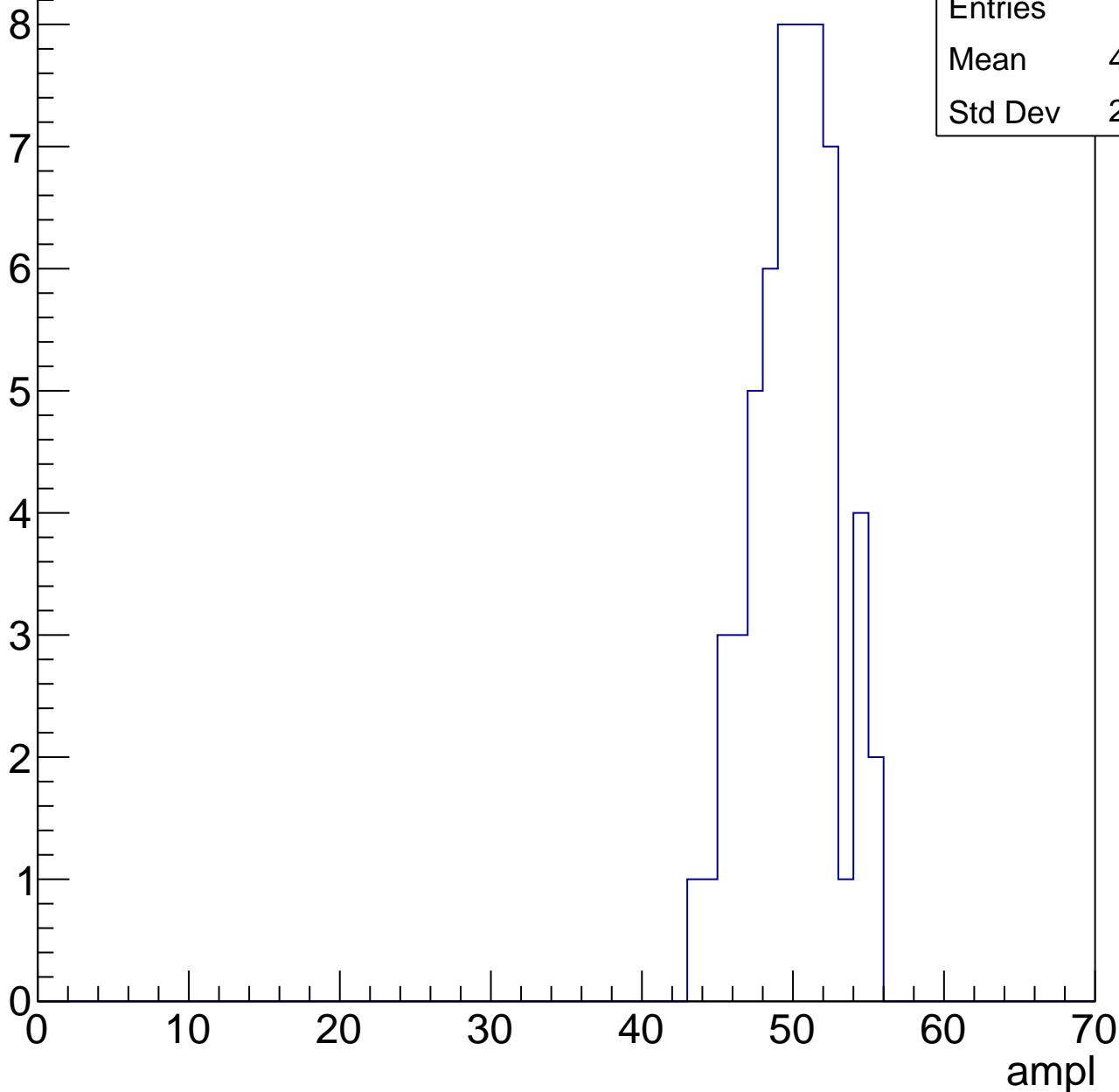


# B1L101S, U20-ch55, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	57
Mean	49.58
Std Dev	2.759

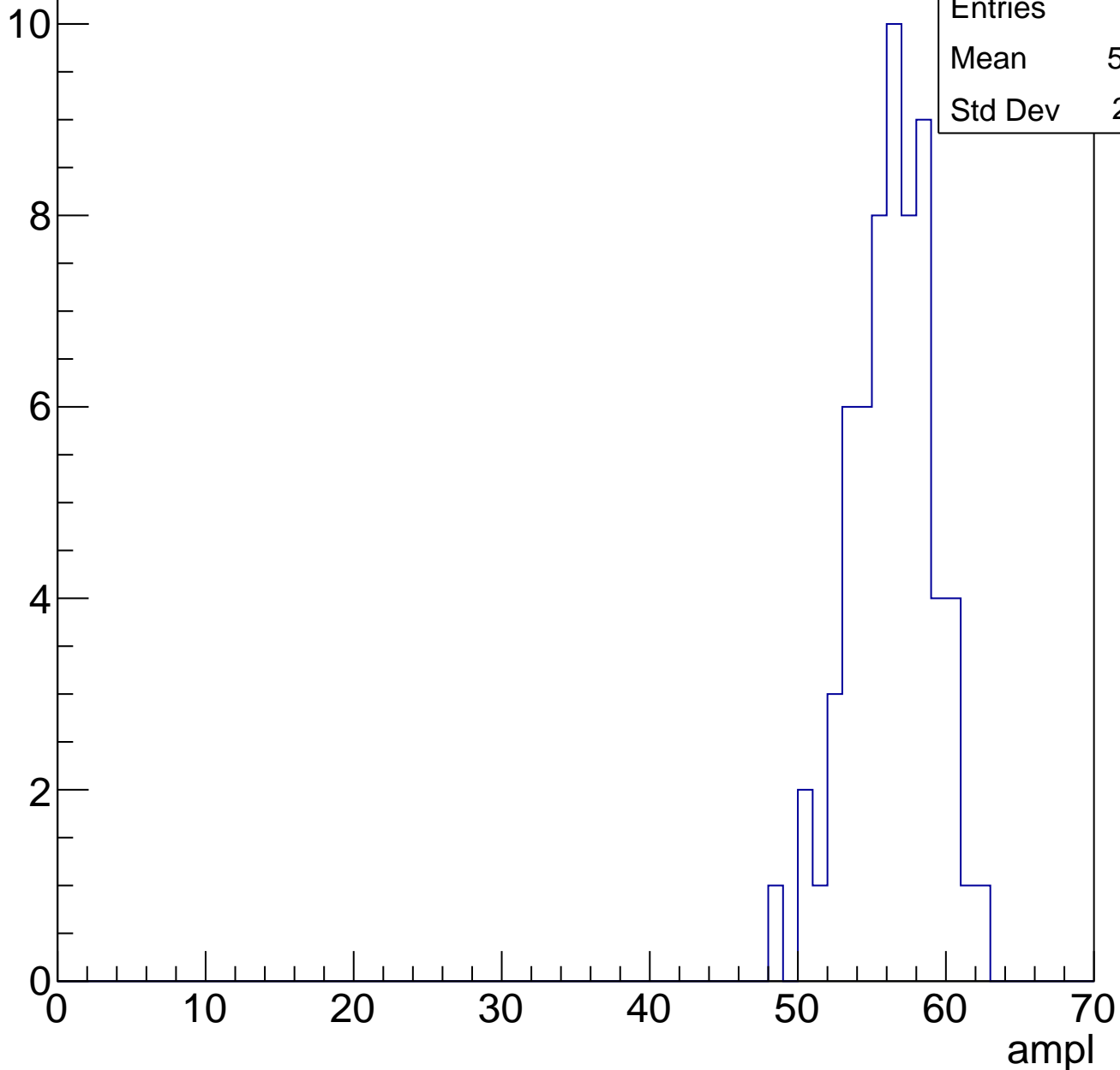


# B1L101S, U20-ch55, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	64
Mean	55.84
Std Dev	2.791

Entry



# B1L101S, U20-ch55, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

10

8

6

4

2

0

0

10

20

30

40

50

60

ampl

Entries	44
Mean	59.27
Std Dev	9.338

8

6

4

2

0

0

10

20

30

40

50

60

70

# B1L101S, U20-ch55, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U20-ch55, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L101S, U20-ch56, adc0

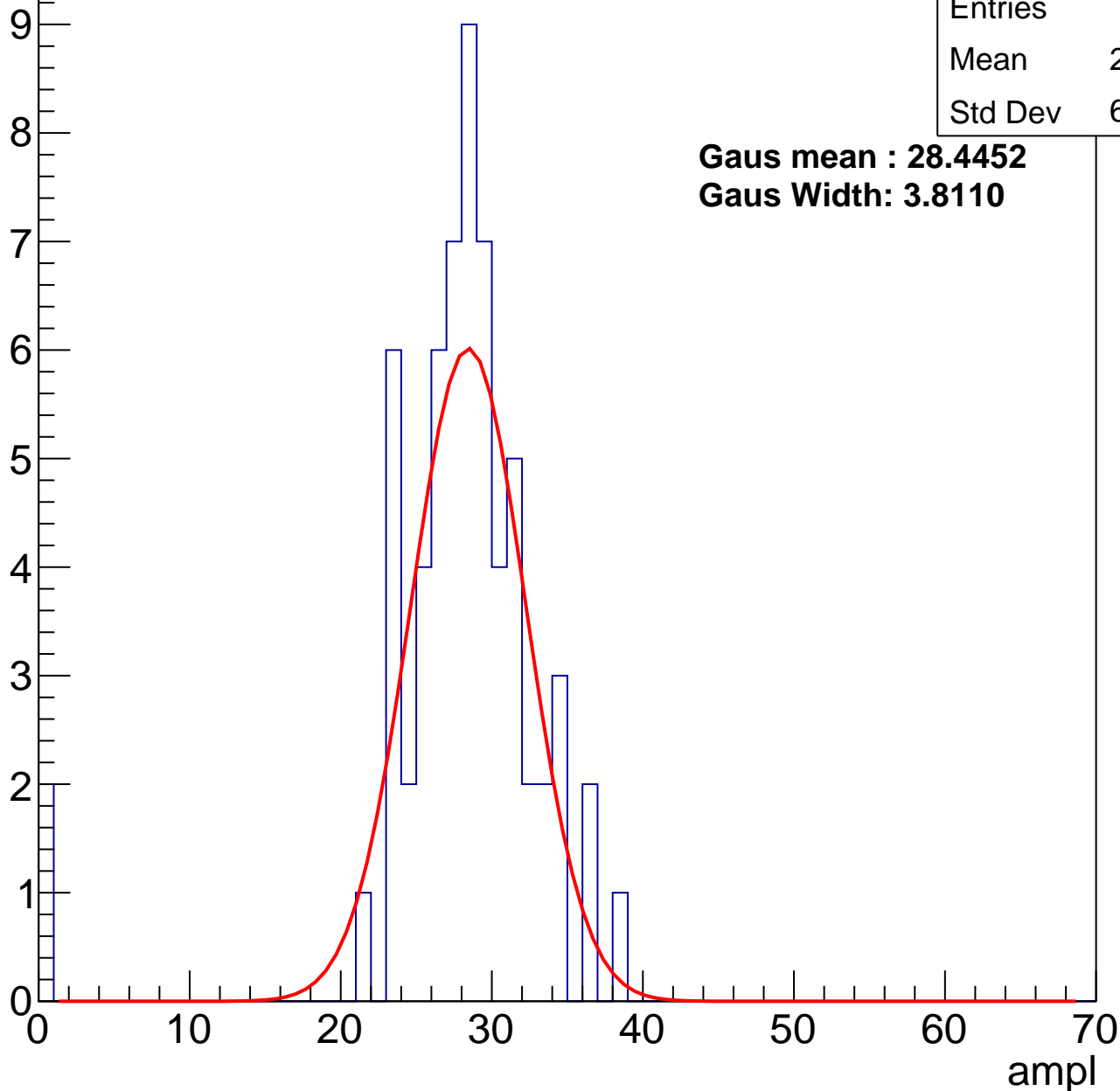
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	27.37
Std Dev	6.077

**Gaus mean : 28.4452**

**Gaus Width: 3.8110**



# B1L101S, U20-ch56, adc1

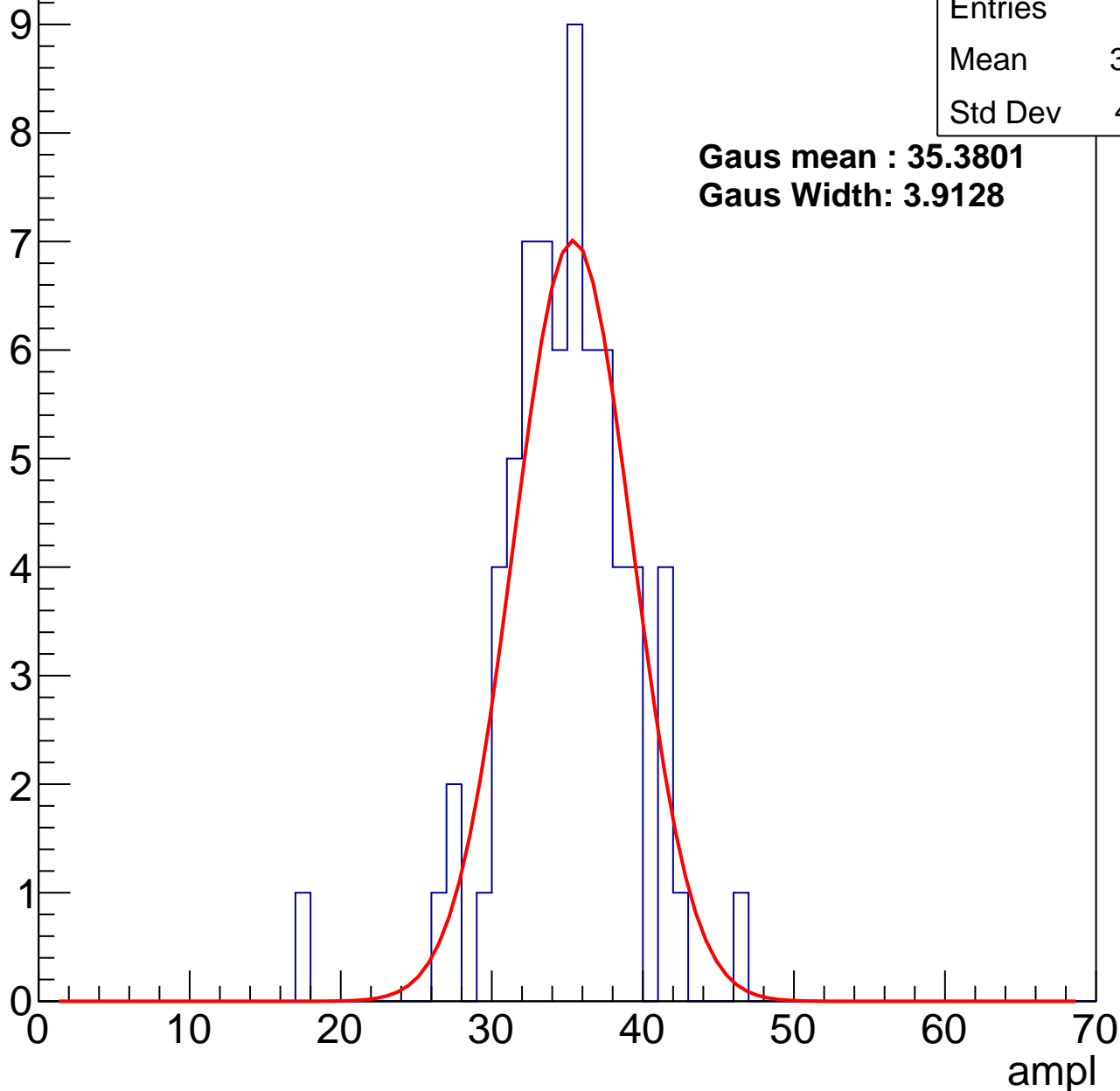
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	34.39
Std Dev	4.281

**Gaus mean : 35.3801**

**Gaus Width: 3.9128**



# B1L101S, U20-ch56, adc2

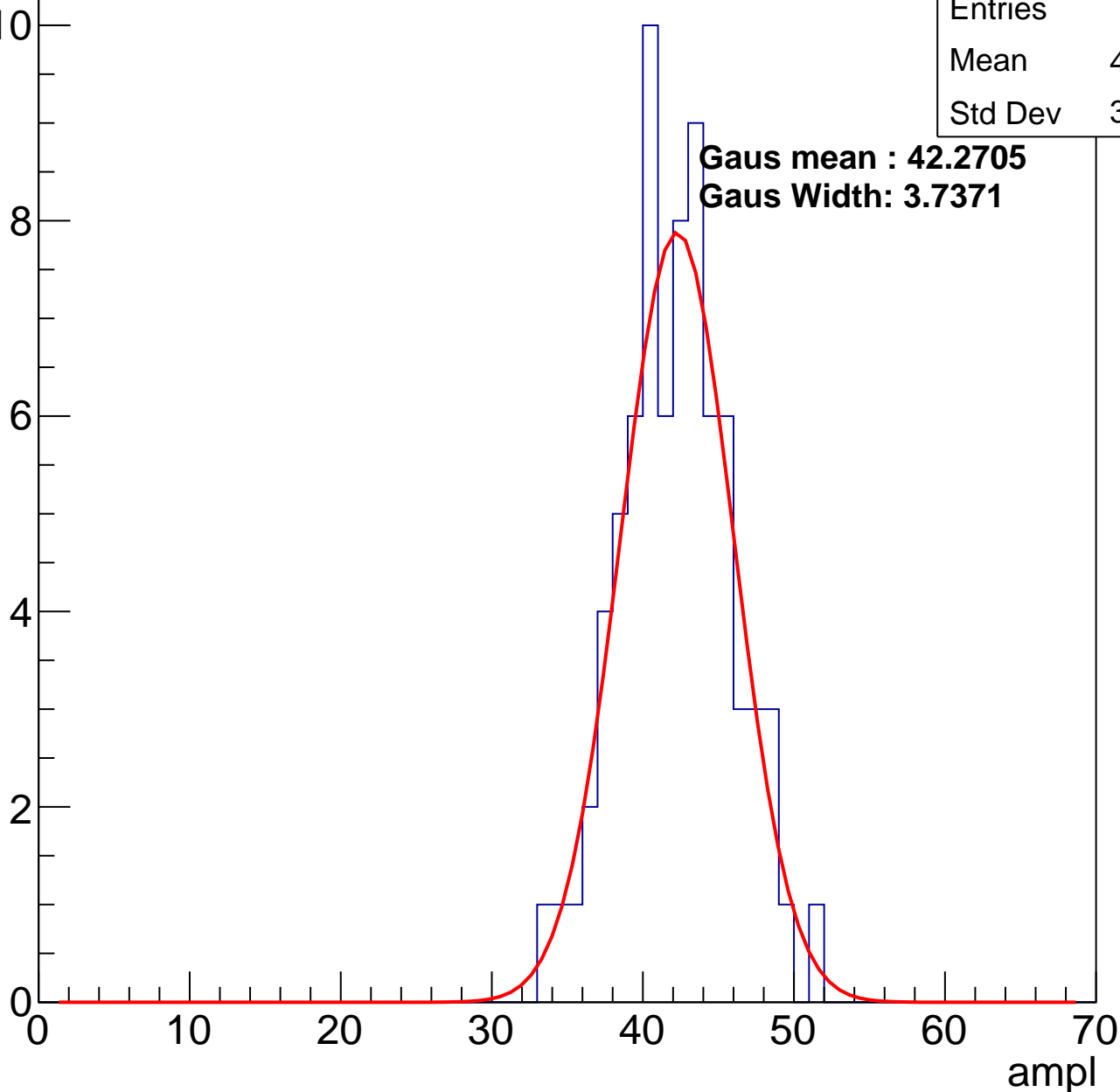
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	76
Mean	41.74
Std Dev	3.607

**Gaus mean : 42.2705**

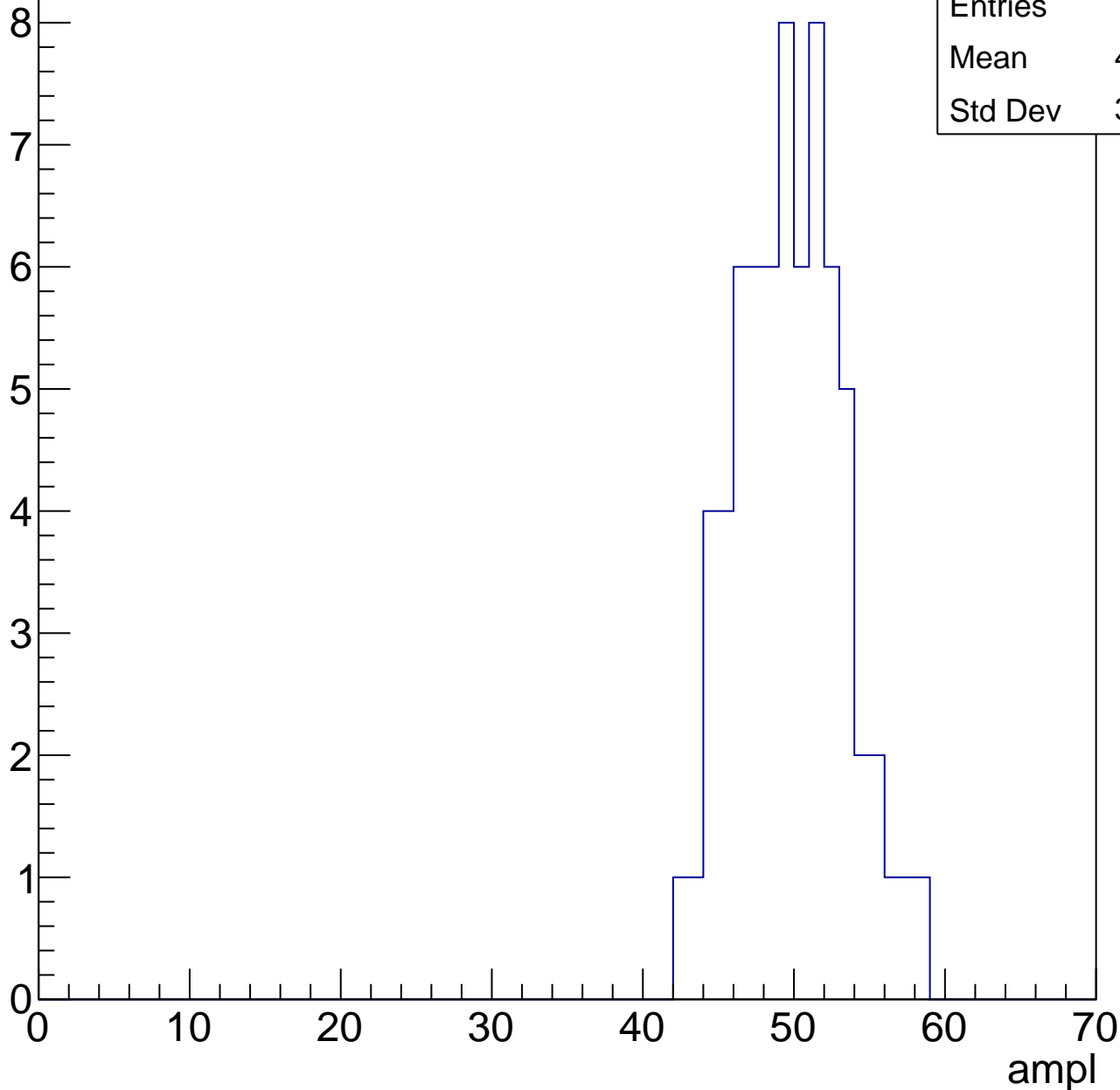
**Gaus Width: 3.7371**



# B1L101S, U20-ch56, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



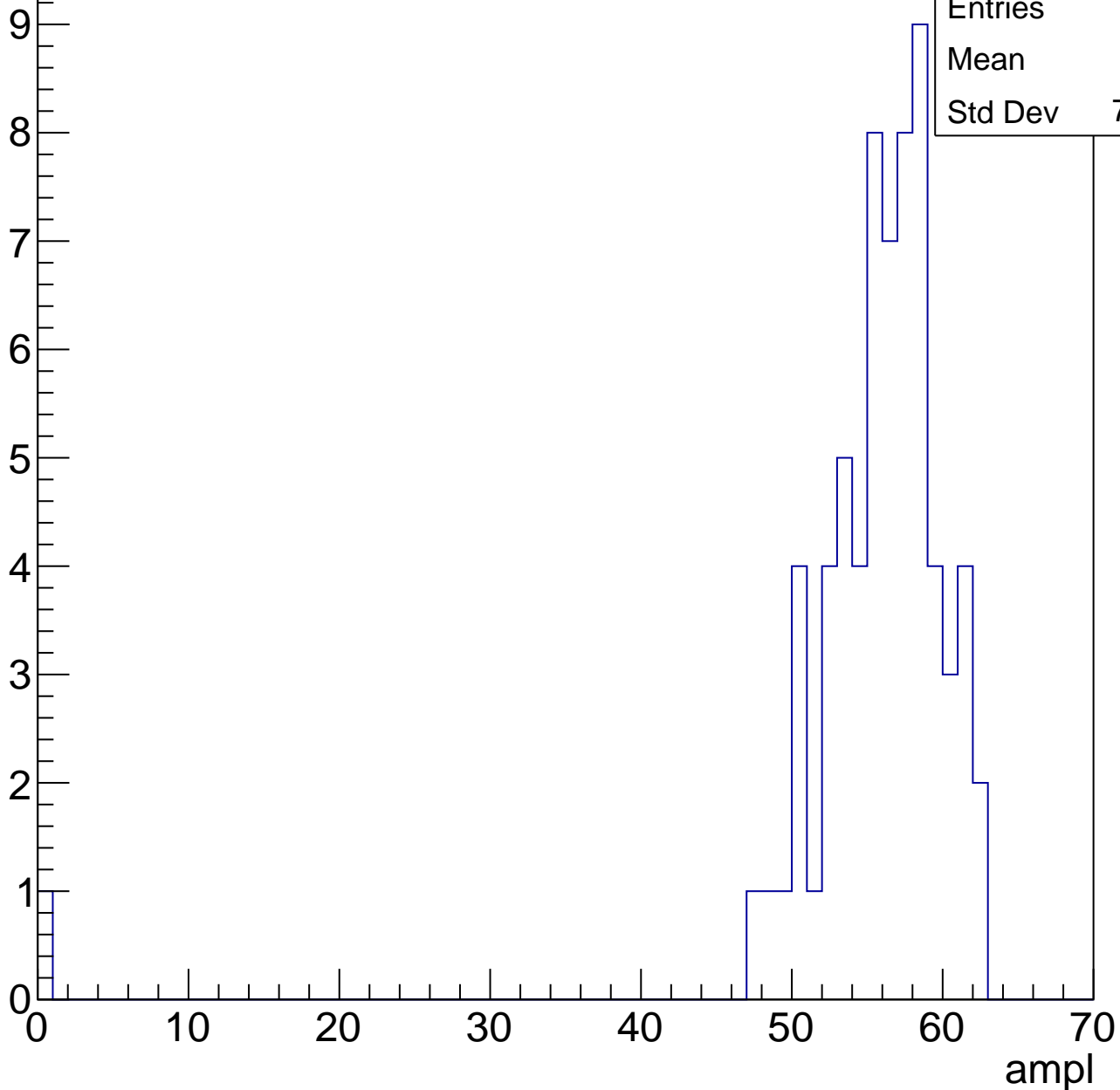
Entries	68
Mean	49.31
Std Dev	3.461

# B1L101S, U20-ch56, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	67
Mean	54.9
Std Dev	7.581

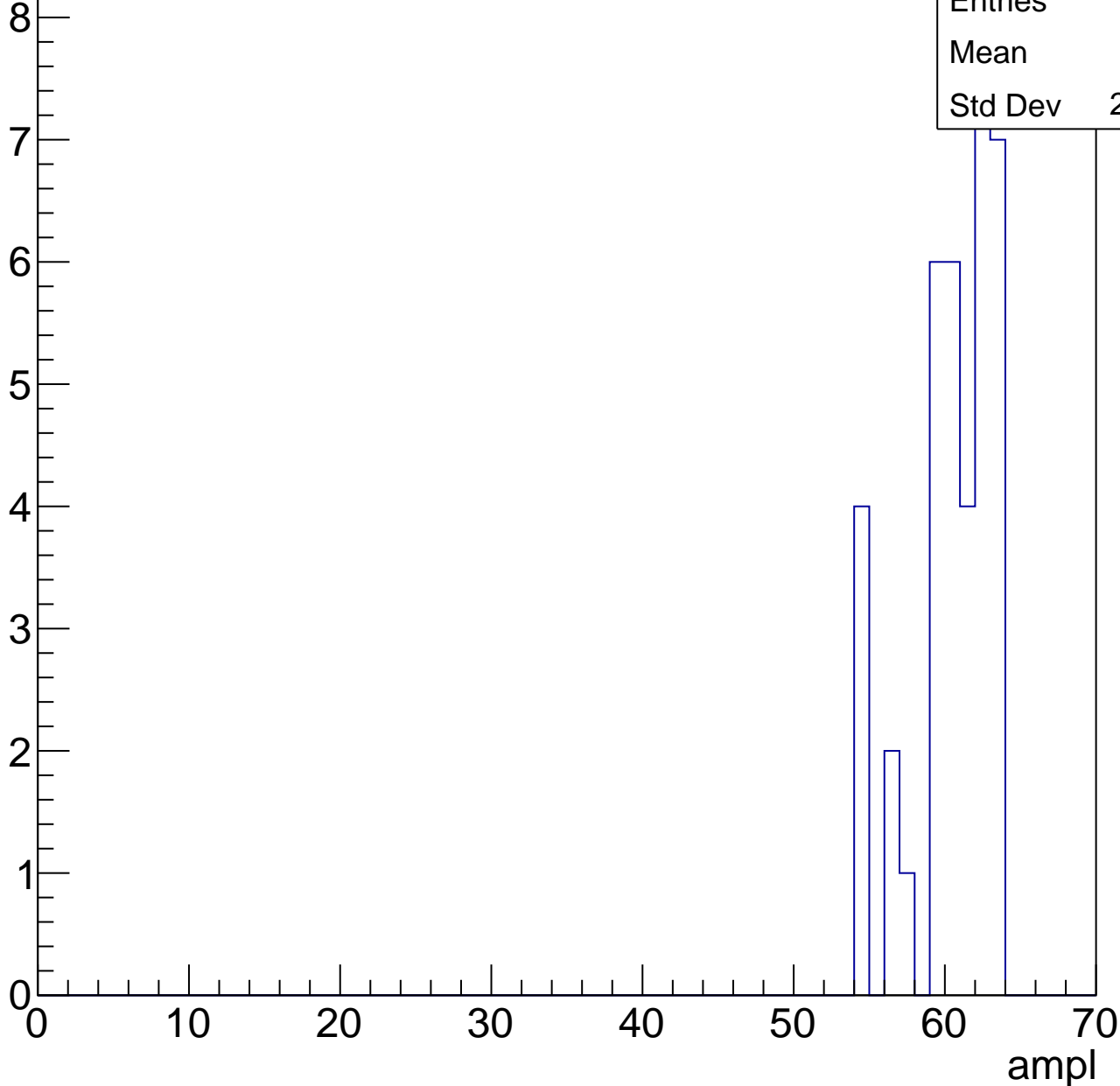


# B1L101S, U20-ch56, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

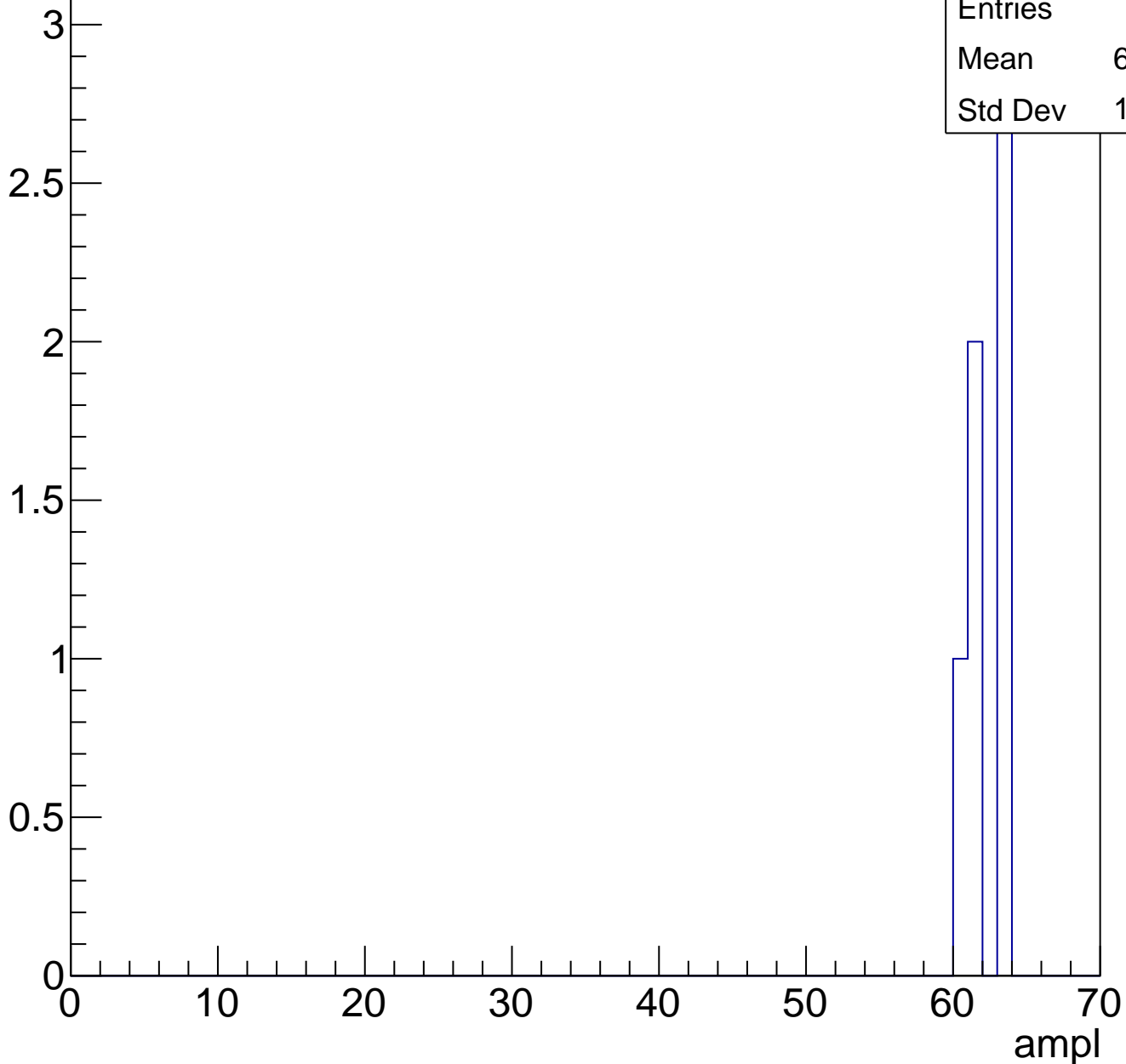
Entries	38
Mean	60
Std Dev	2.763



# B1L101S, U20-ch56, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

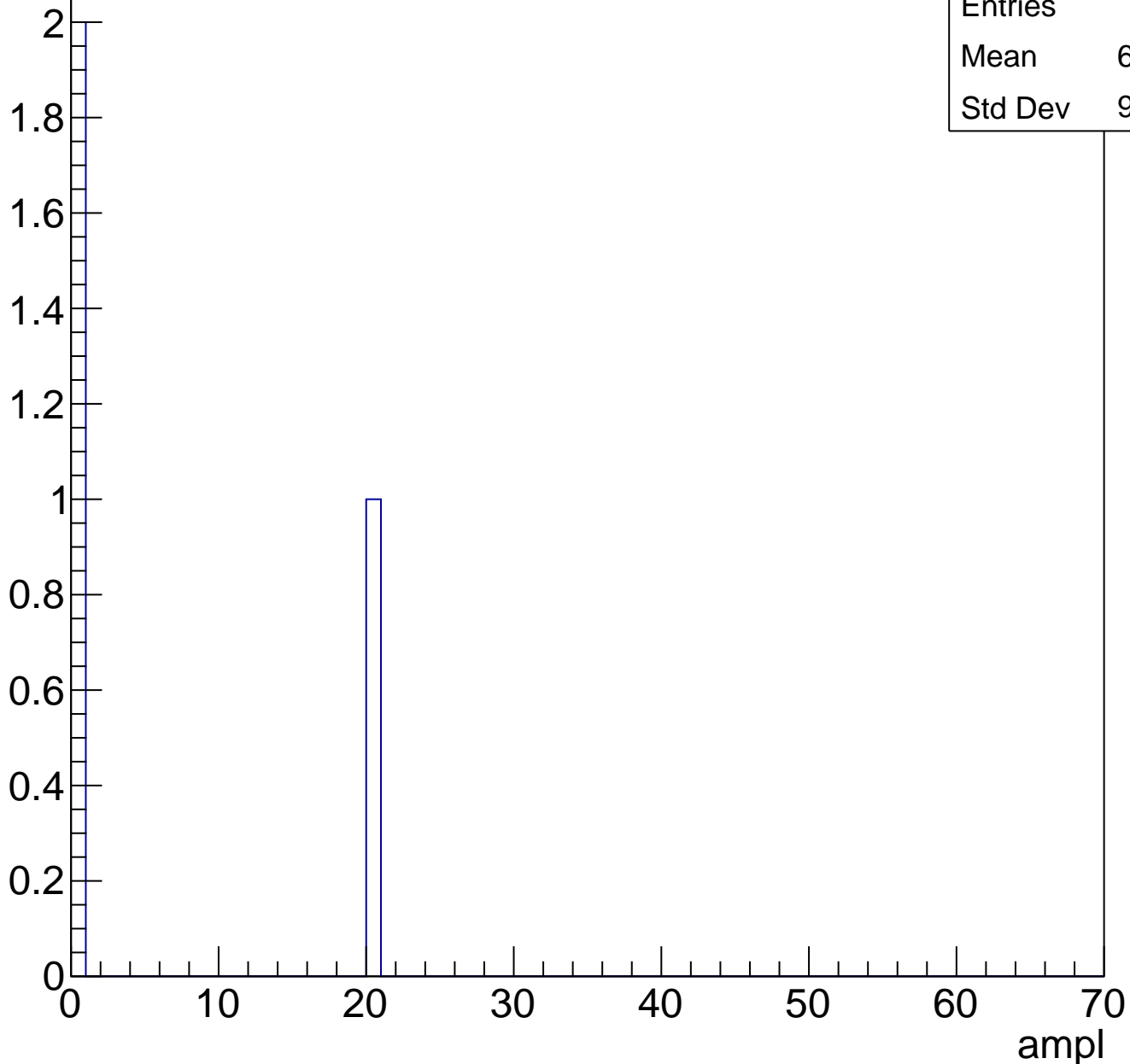




# B1L101S, U20-ch56, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	3
Mean	6.667
Std Dev	9.428

# B1L101S, U20-ch57, adc0

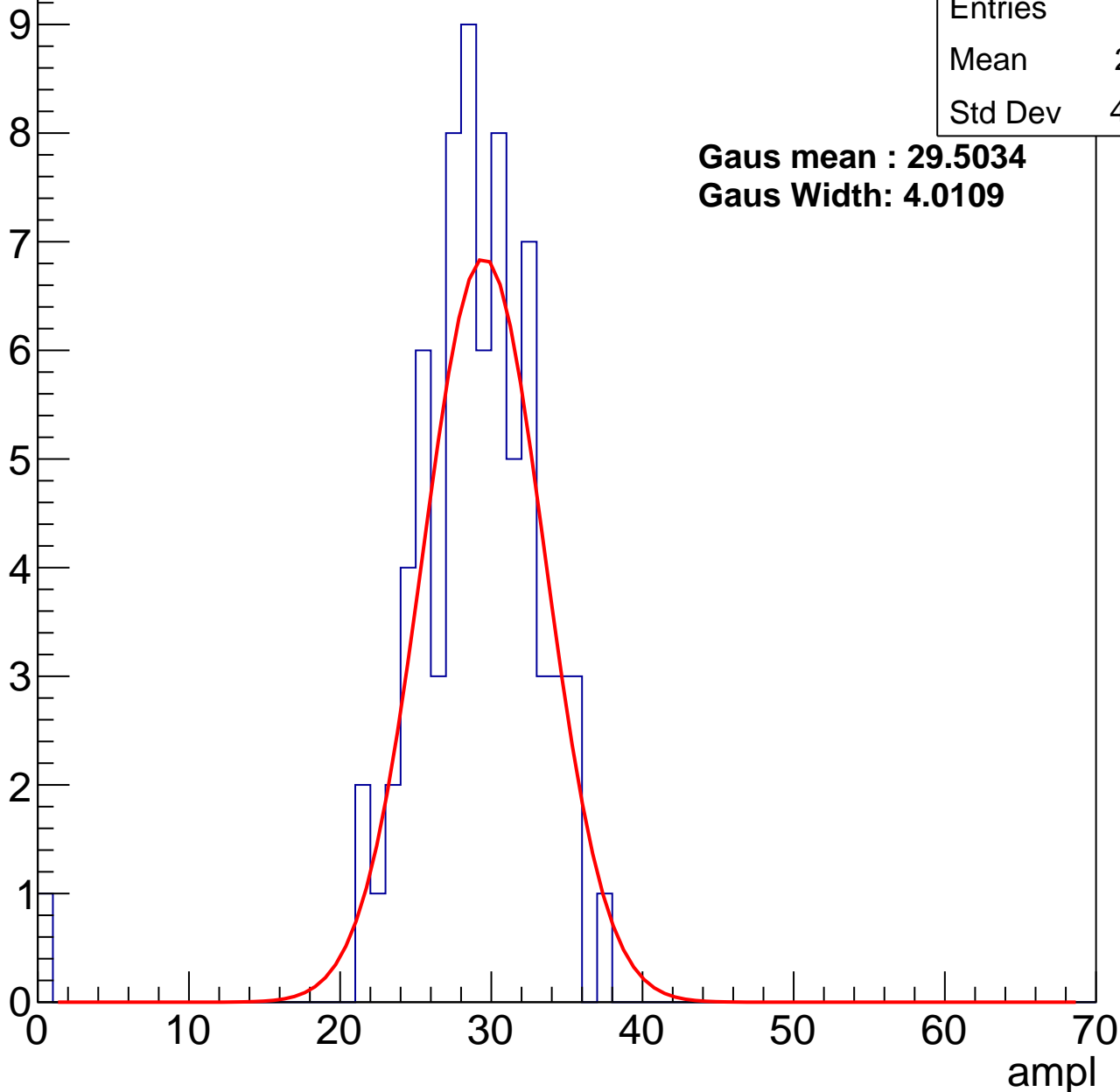
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	72
Mean	28.31
Std Dev	4.867

**Gaus mean : 29.5034**

**Gaus Width: 4.0109**



# B1L101S, U20-ch57, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	82
Mean	36.1
Std Dev	3.701

**Gaus mean : 36.4761**

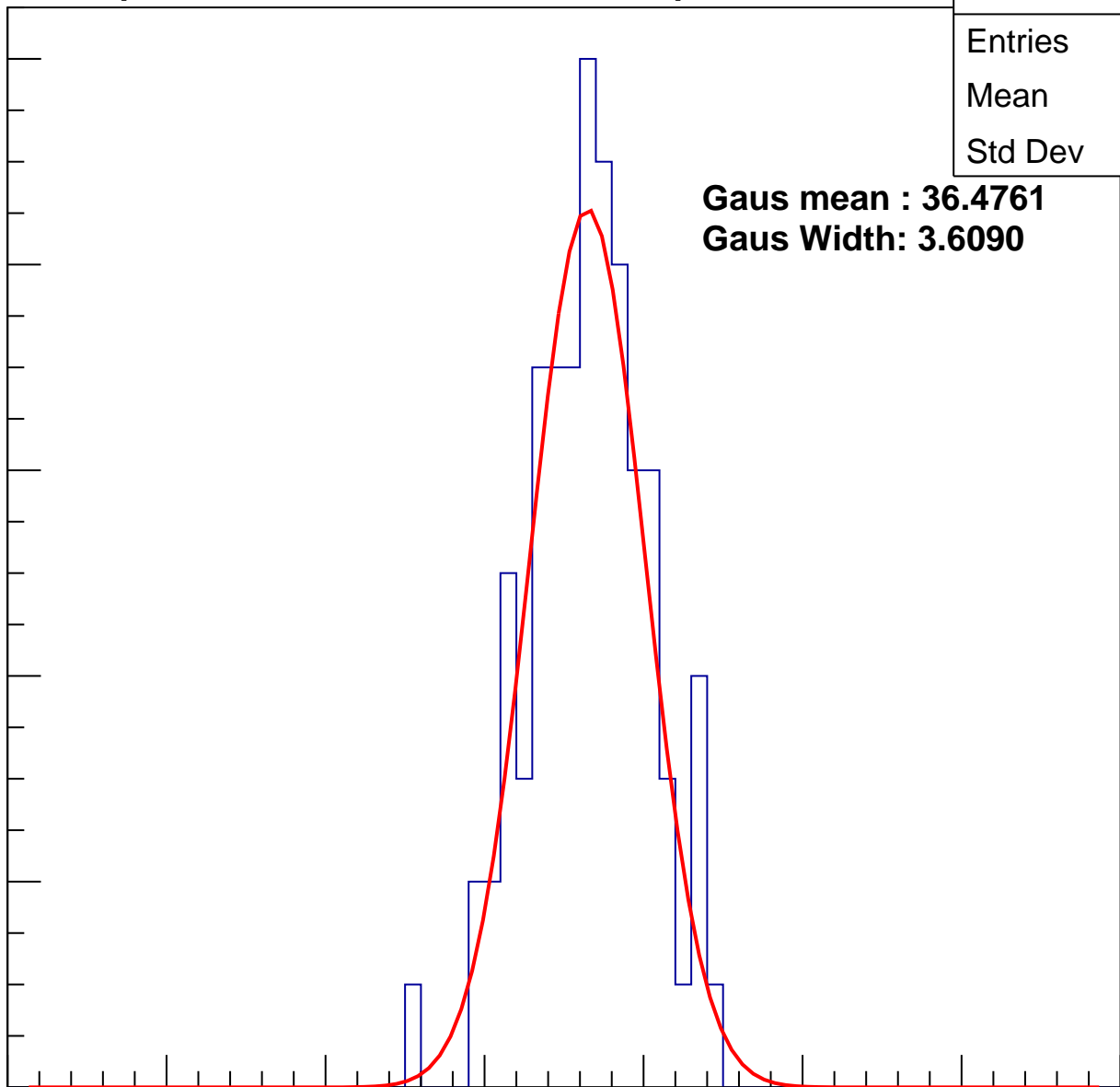
**Gaus Width: 3.6090**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U20-ch57, adc2

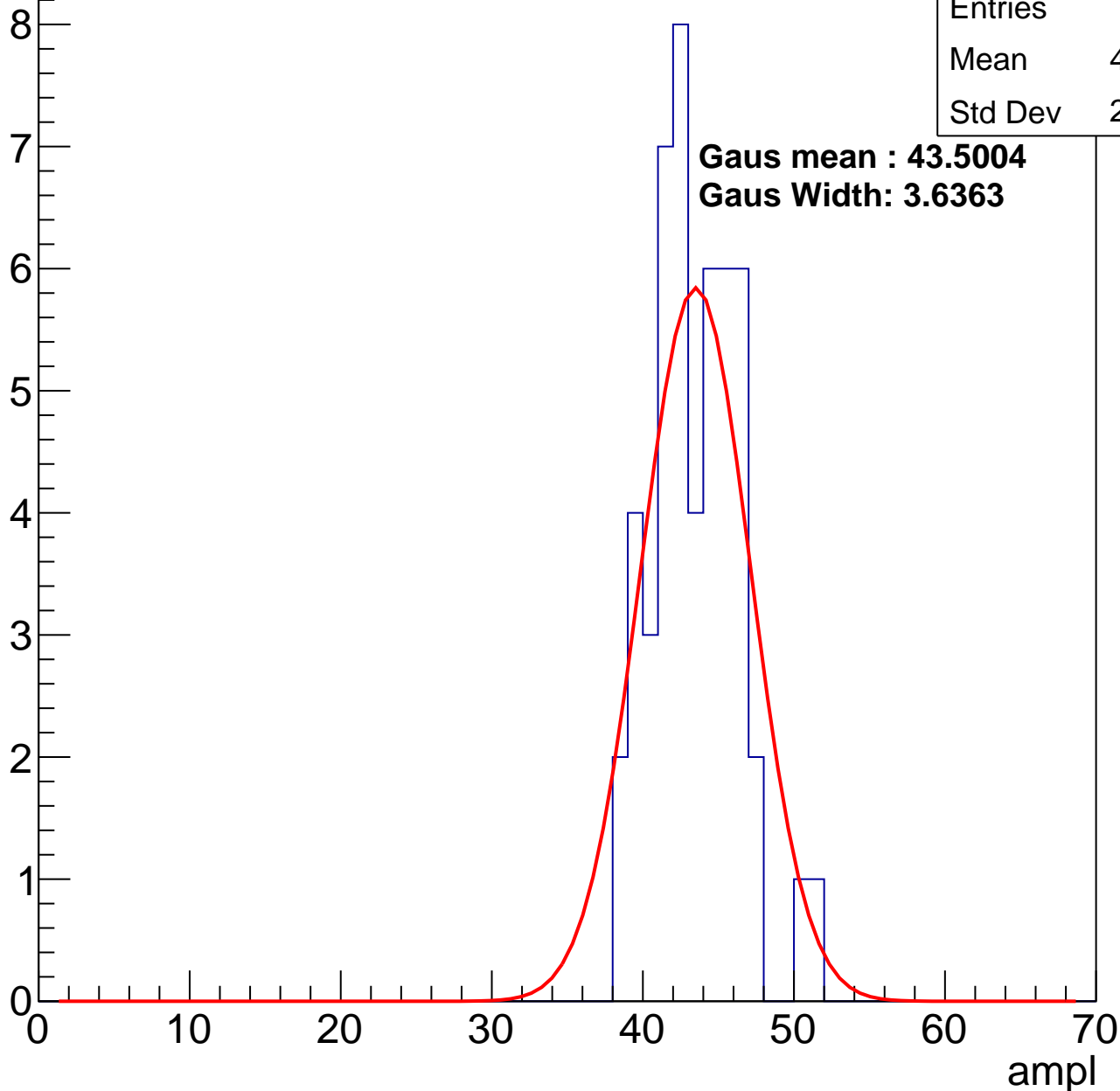
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	50
Mean	43.04
Std Dev	2.849

**Gaus mean : 43.5004**

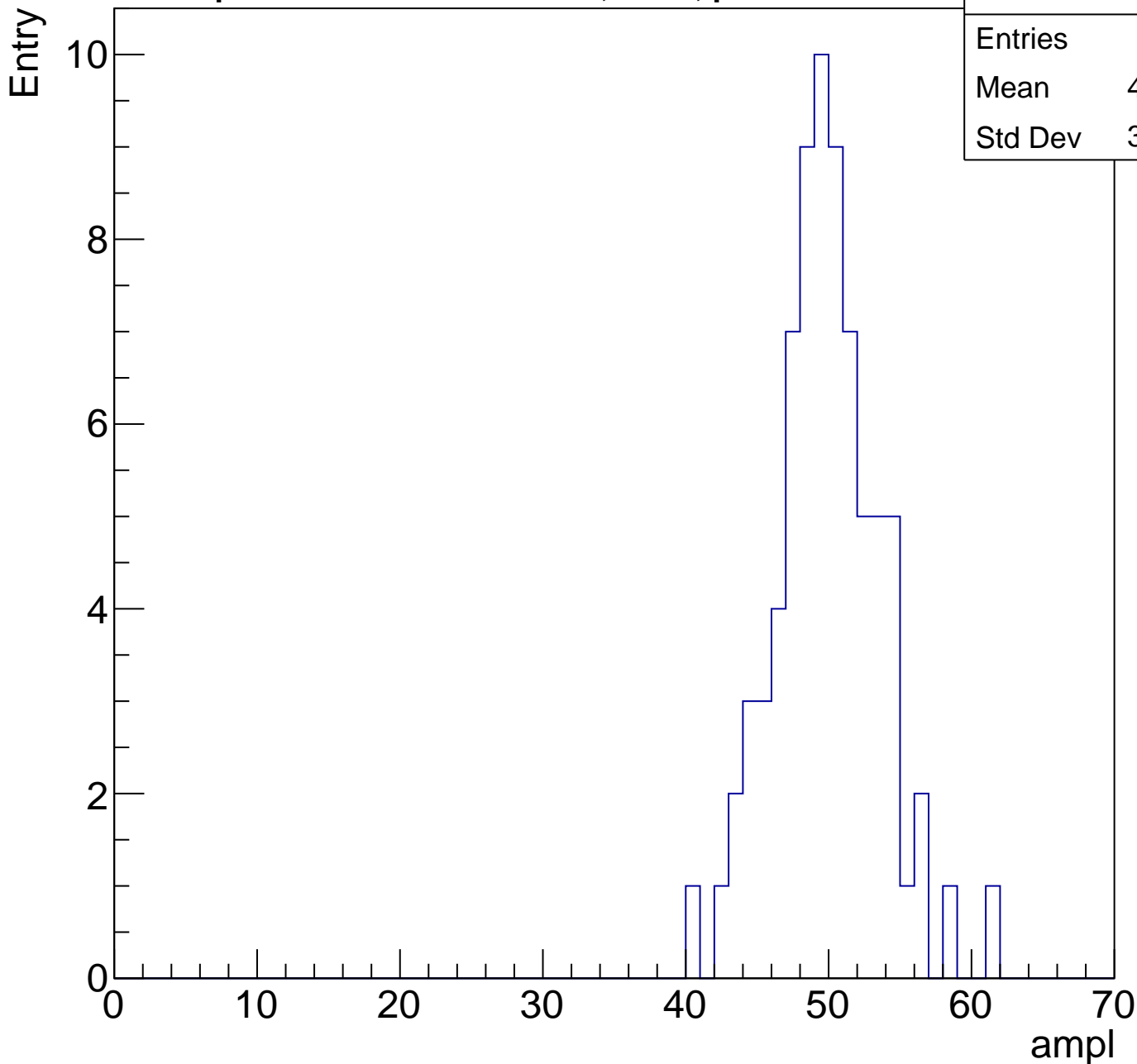
**Gaus Width: 3.6363**



# B1L101S, U20-ch57, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

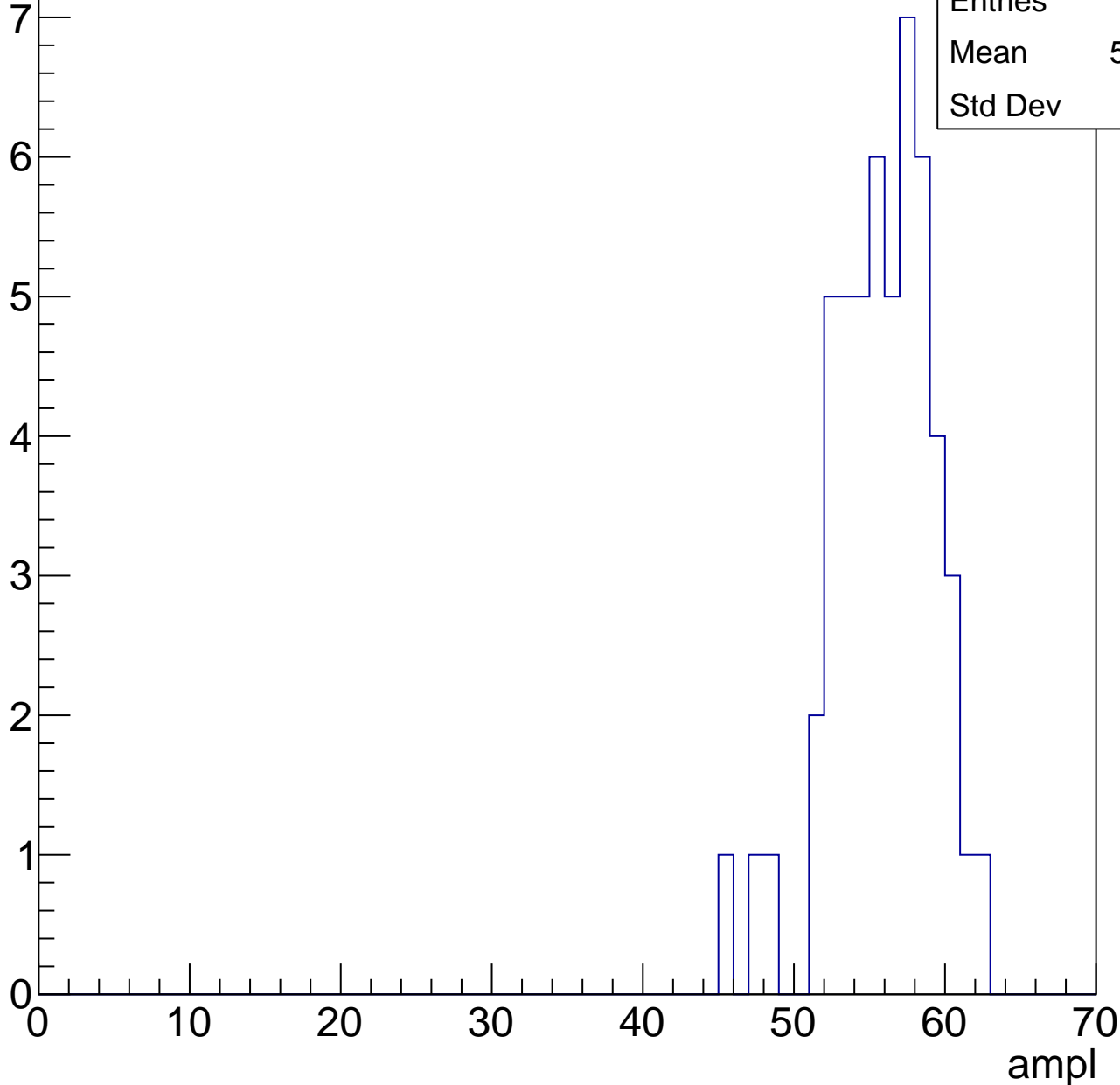
Entries	76
Mean	49.45
Std Dev	3.679



# B1L101S, U20-ch57, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

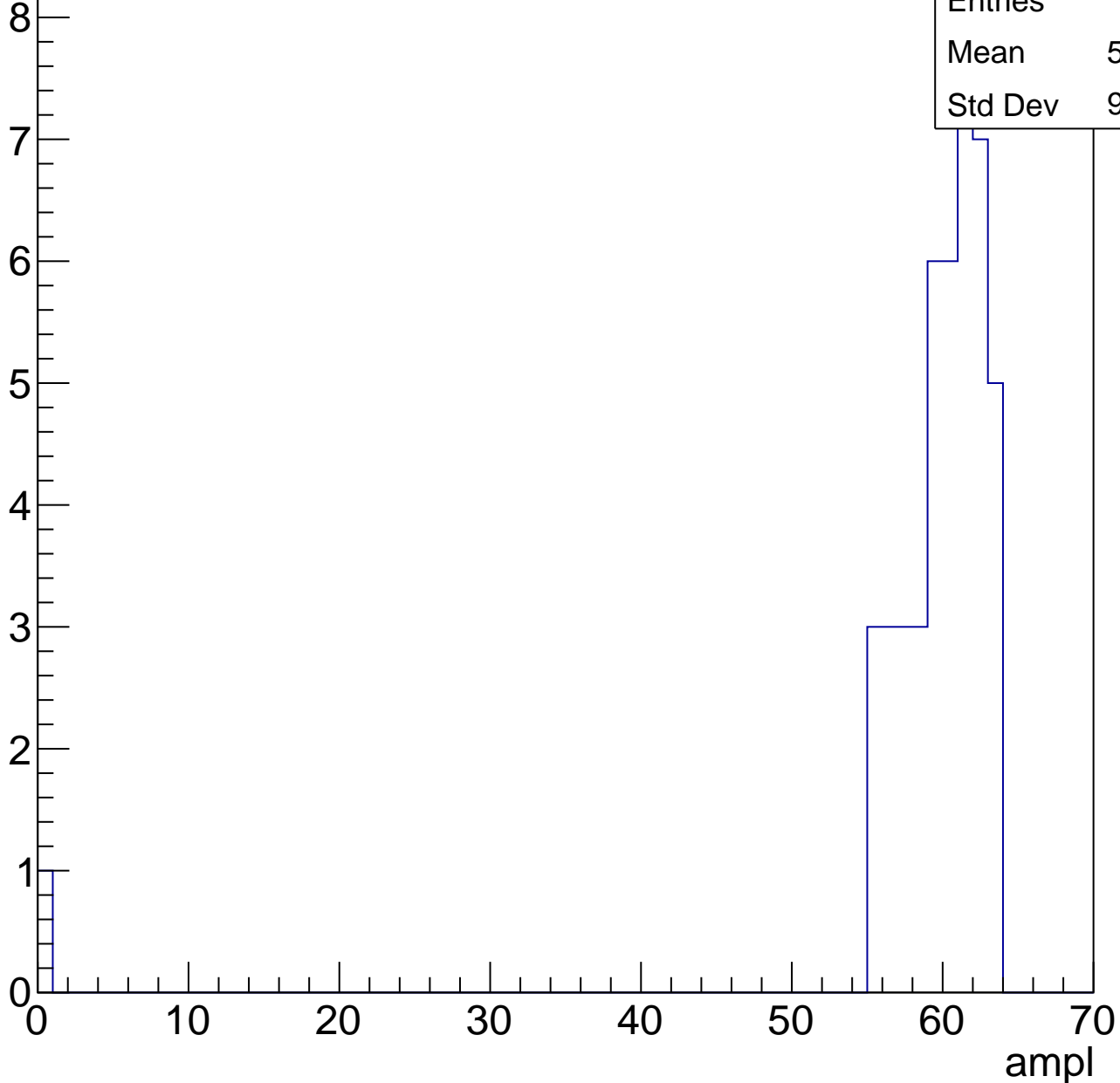


# B1L101S, U20-ch57, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	45
Mean	58.42
Std Dev	9.113

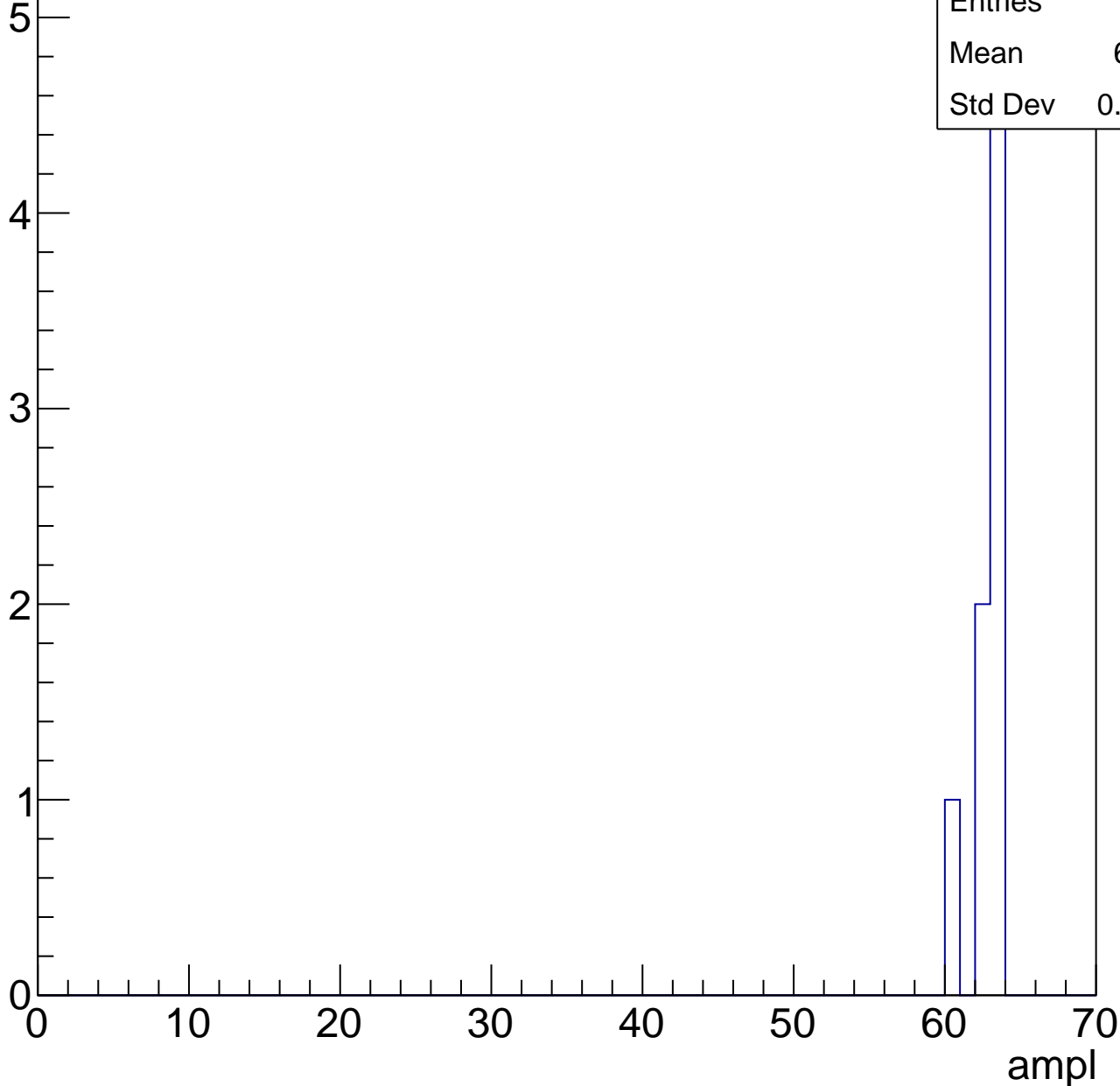


# B1L101S, U20-ch57, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	8
Mean	62.38
Std Dev	0.9922





# B1L101S, U20-ch57, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U20-ch58, adc0

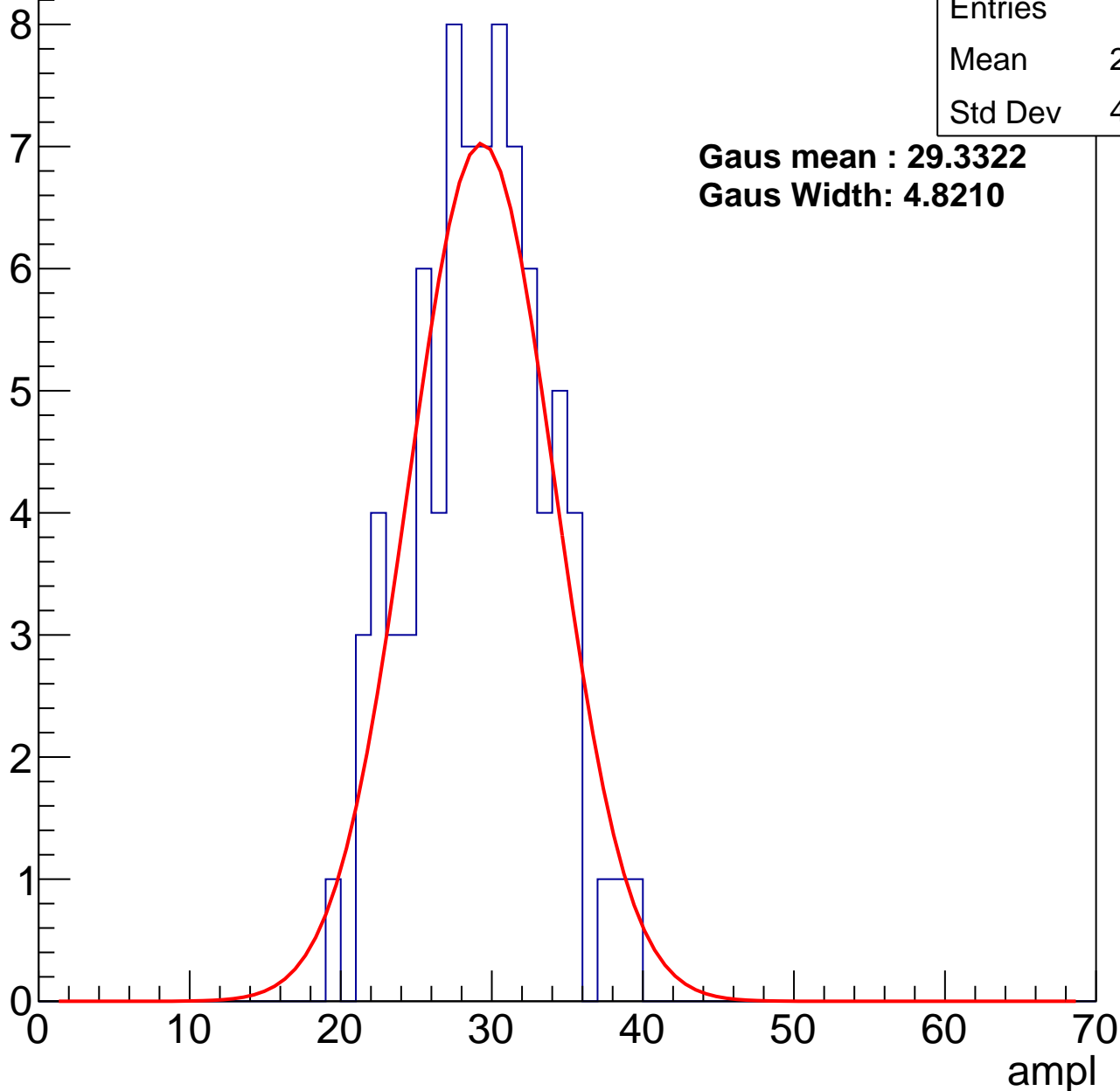
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	83
Mean	28.73
Std Dev	4.257

**Gaus mean : 29.3322**

**Gaus Width: 4.8210**



# B1L101S, U20-ch58, adc1

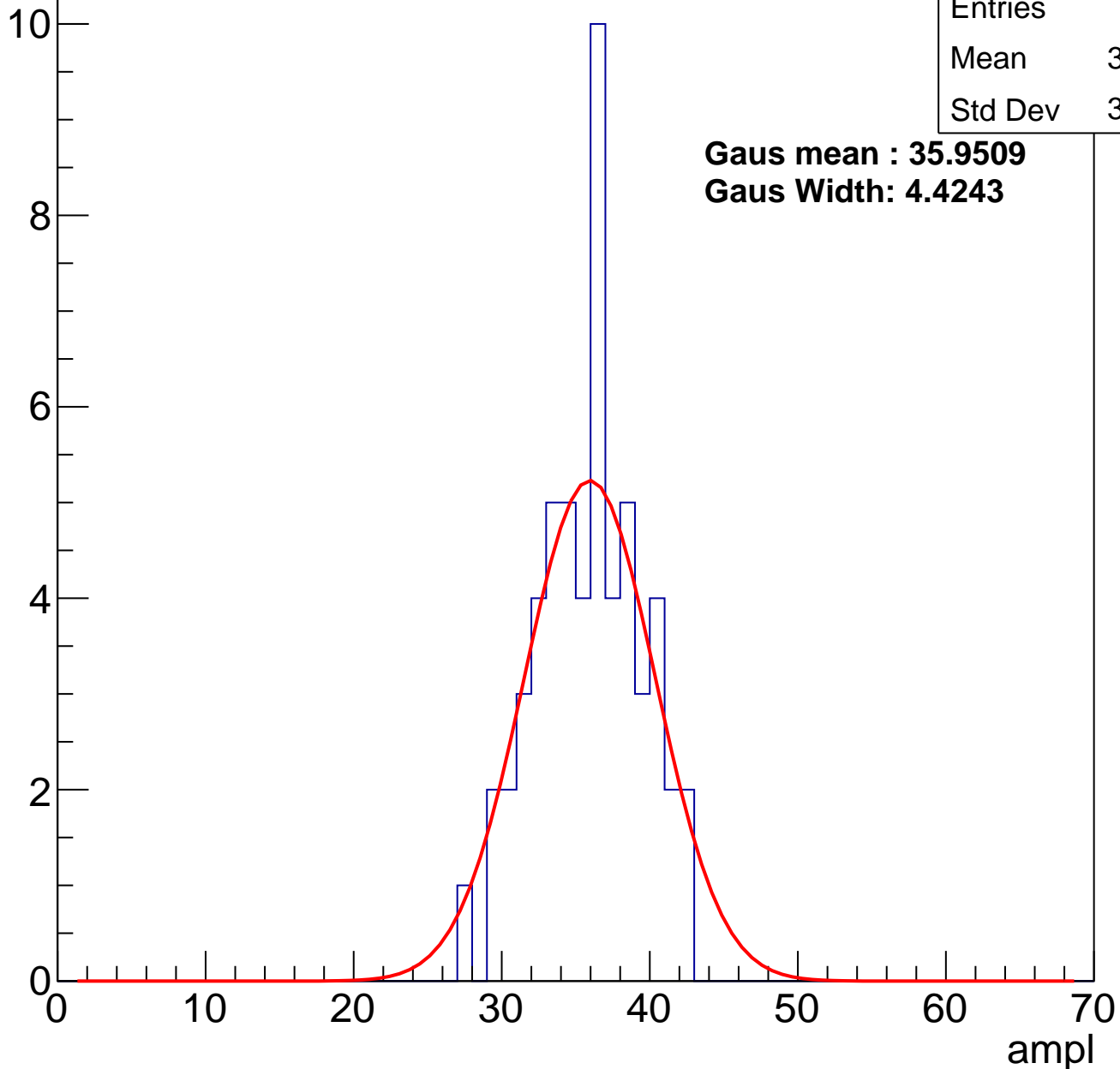
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	56
Mean	35.39
Std Dev	3.473

**Gaus mean : 35.9509**

**Gaus Width: 4.4243**

Entry



# B1L101S, U20-ch58, adc2

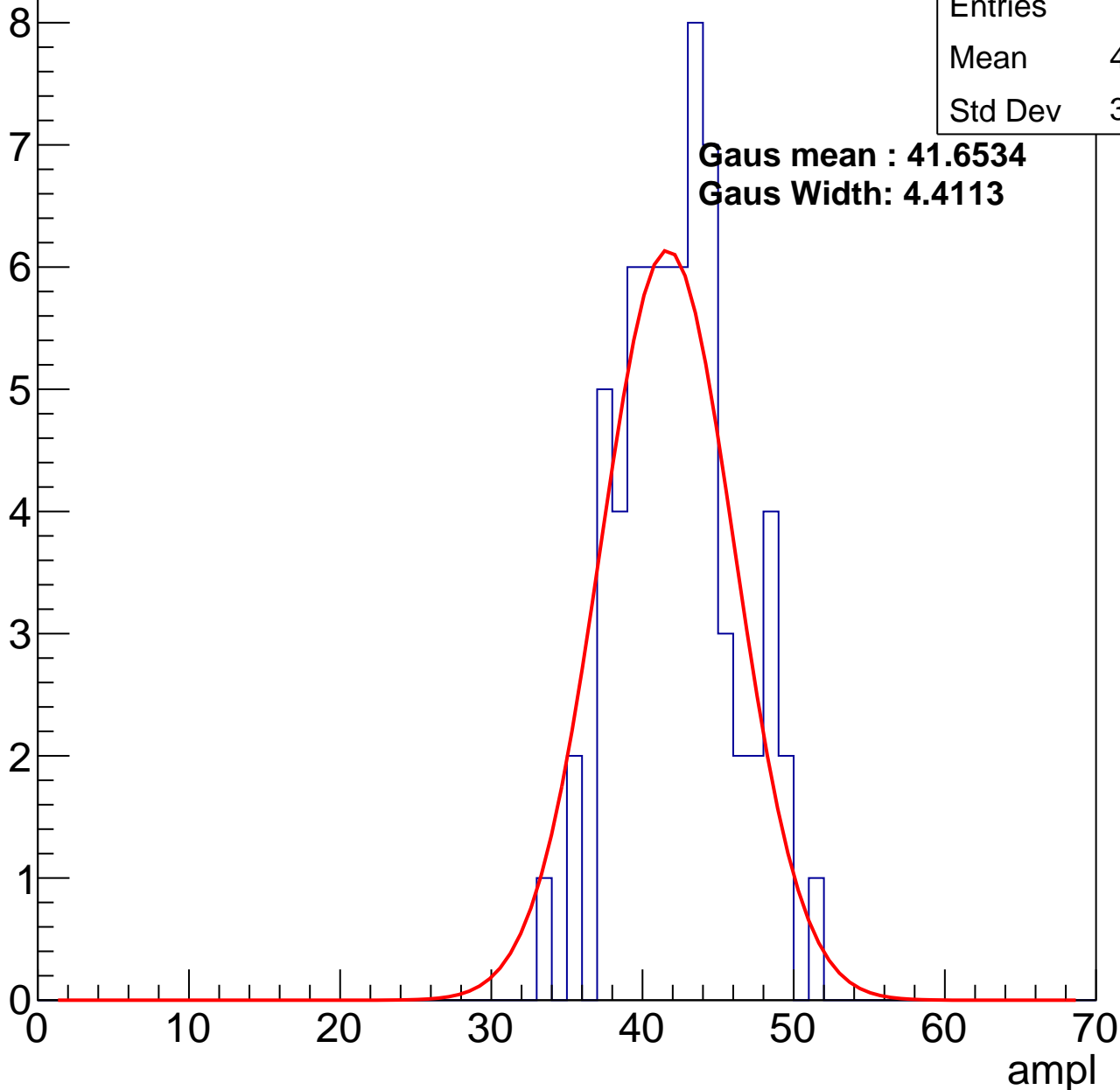
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	41.94
Std Dev	3.762

**Gaus mean : 41.6534**

**Gaus Width: 4.4113**

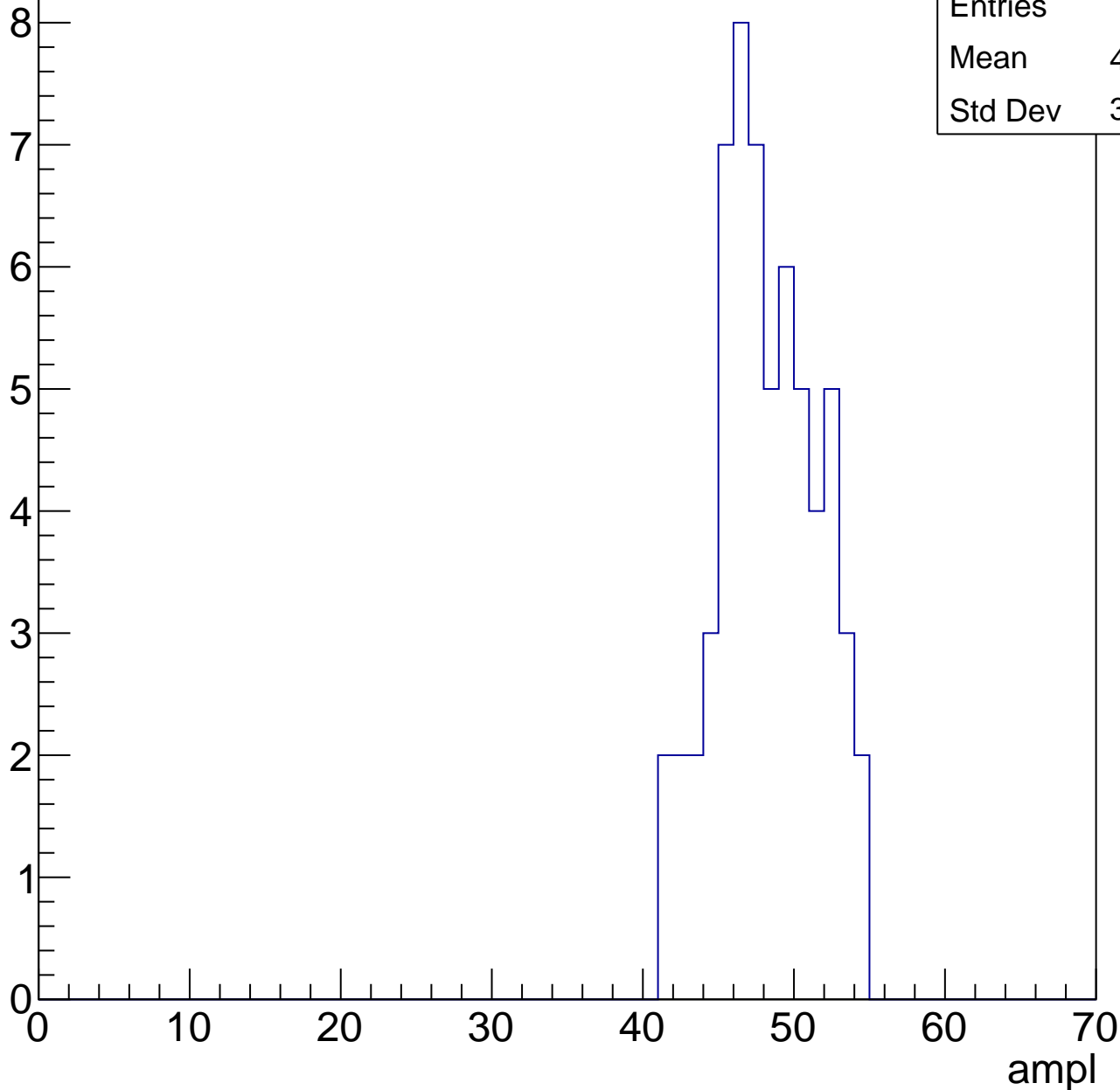


# B1L101S, U20-ch58, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

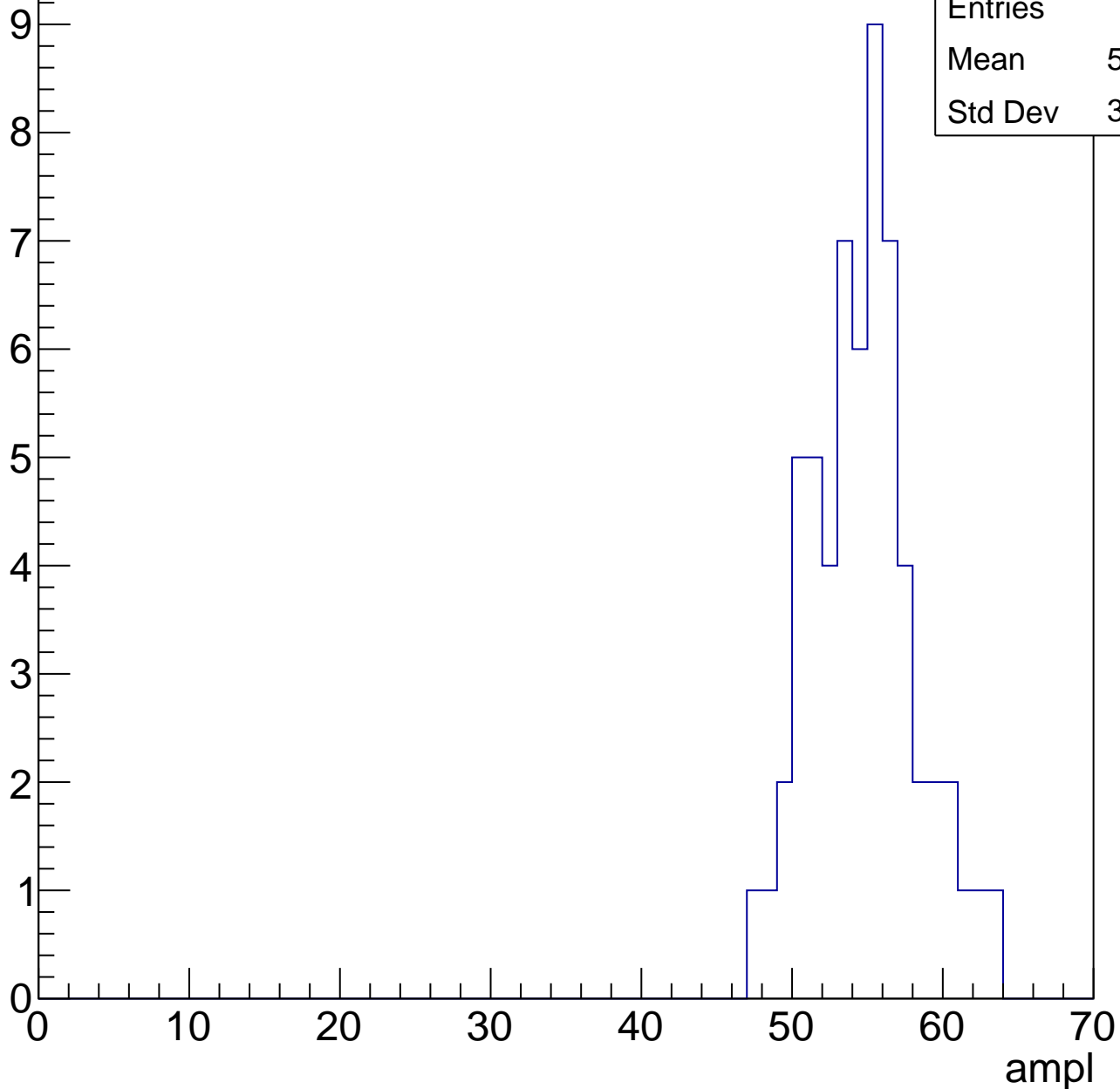
Entries	61
Mean	47.72
Std Dev	3.275



# B1L101S, U20-ch58, adc4

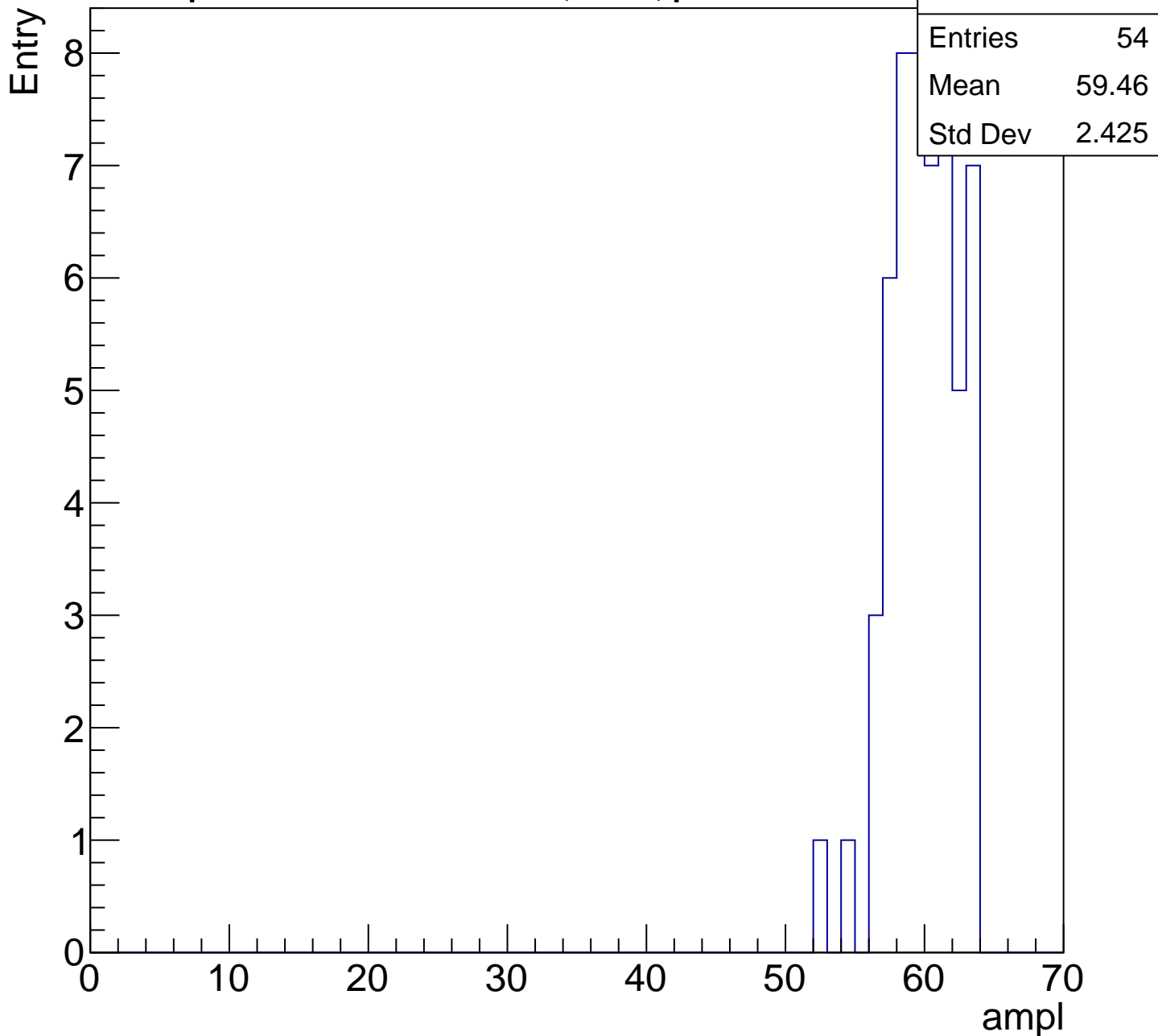
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U20-ch58, adc5

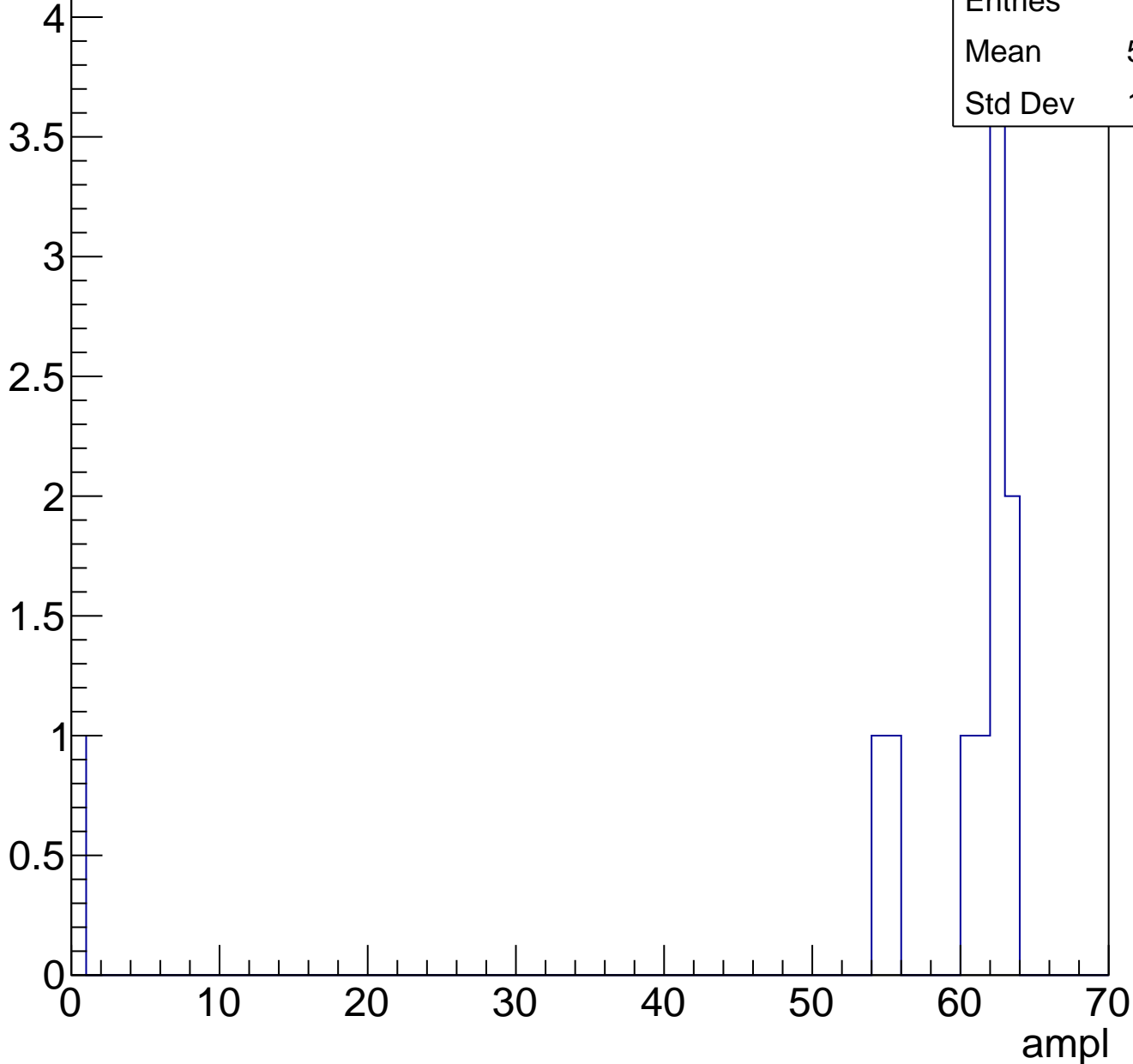
calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U20-ch58, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U20-ch58, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U20-ch59, adc0

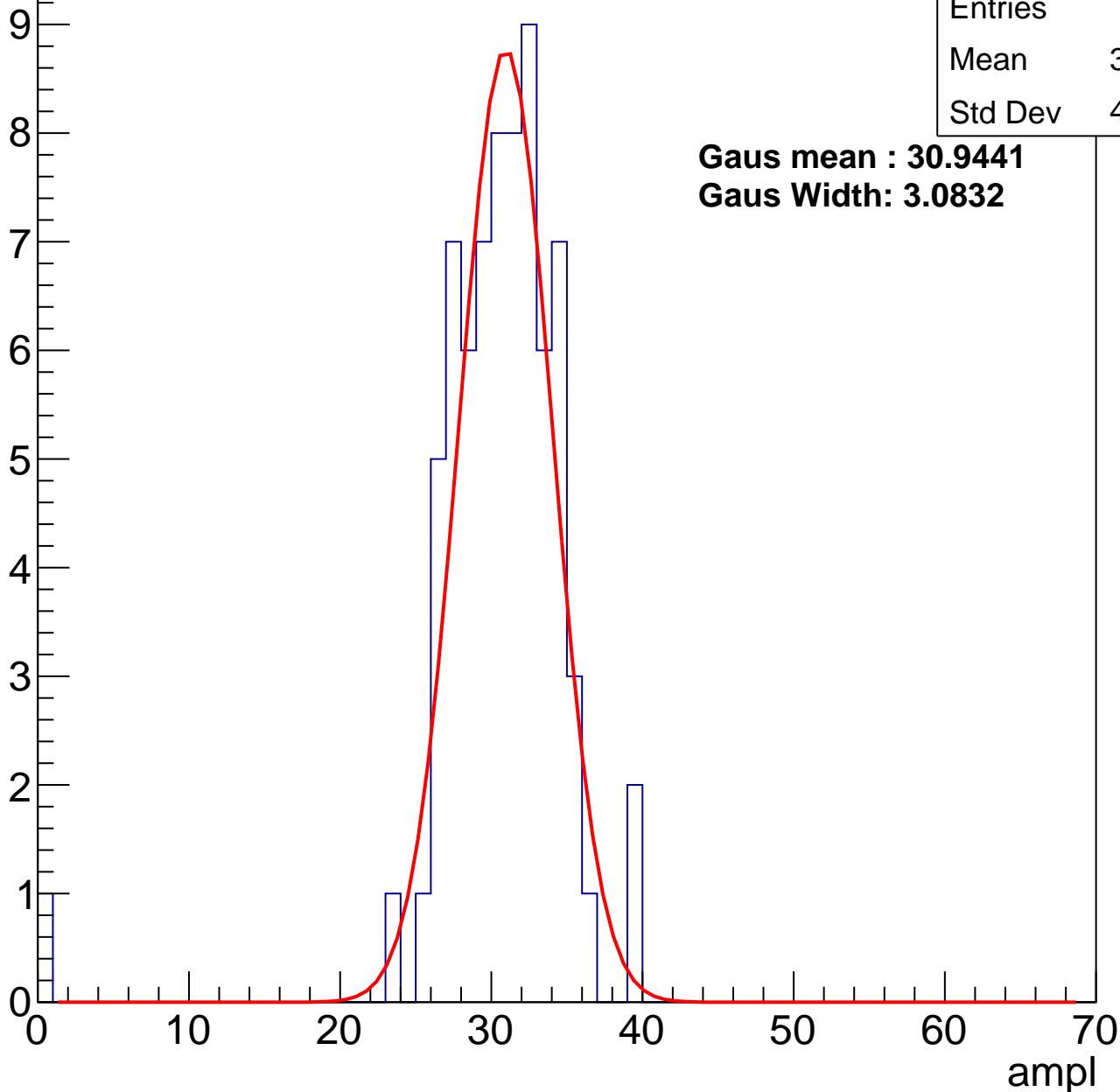
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	72
Mean	30.12
Std Dev	4.758

**Gaus mean : 30.9441**

**Gaus Width: 3.0832**



# B1L101S, U20-ch59, adc1

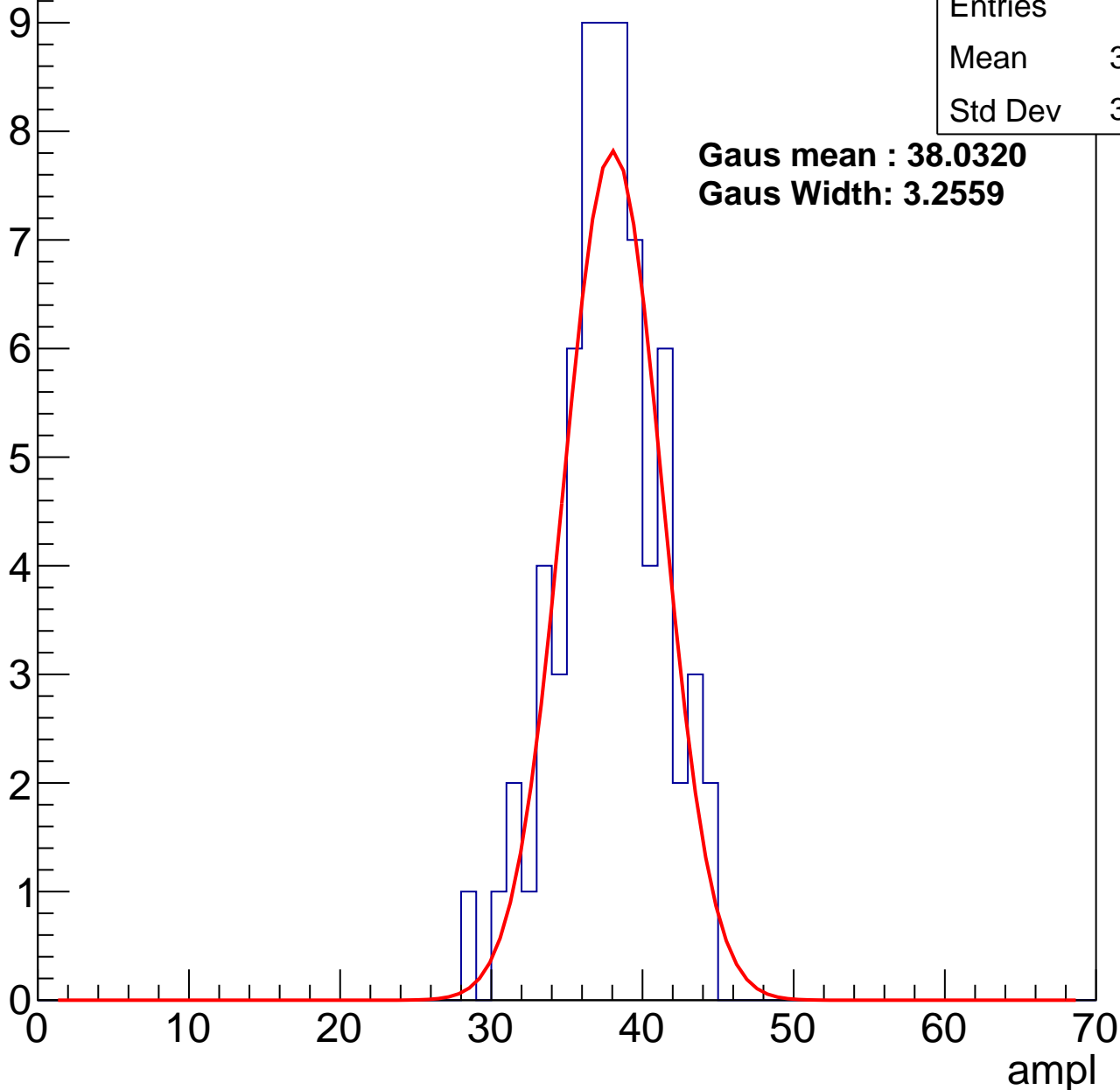
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	37.32
Std Dev	3.338

**Gaus mean : 38.0320**

**Gaus Width: 3.2559**



# B1L101S, U20-ch59, adc2

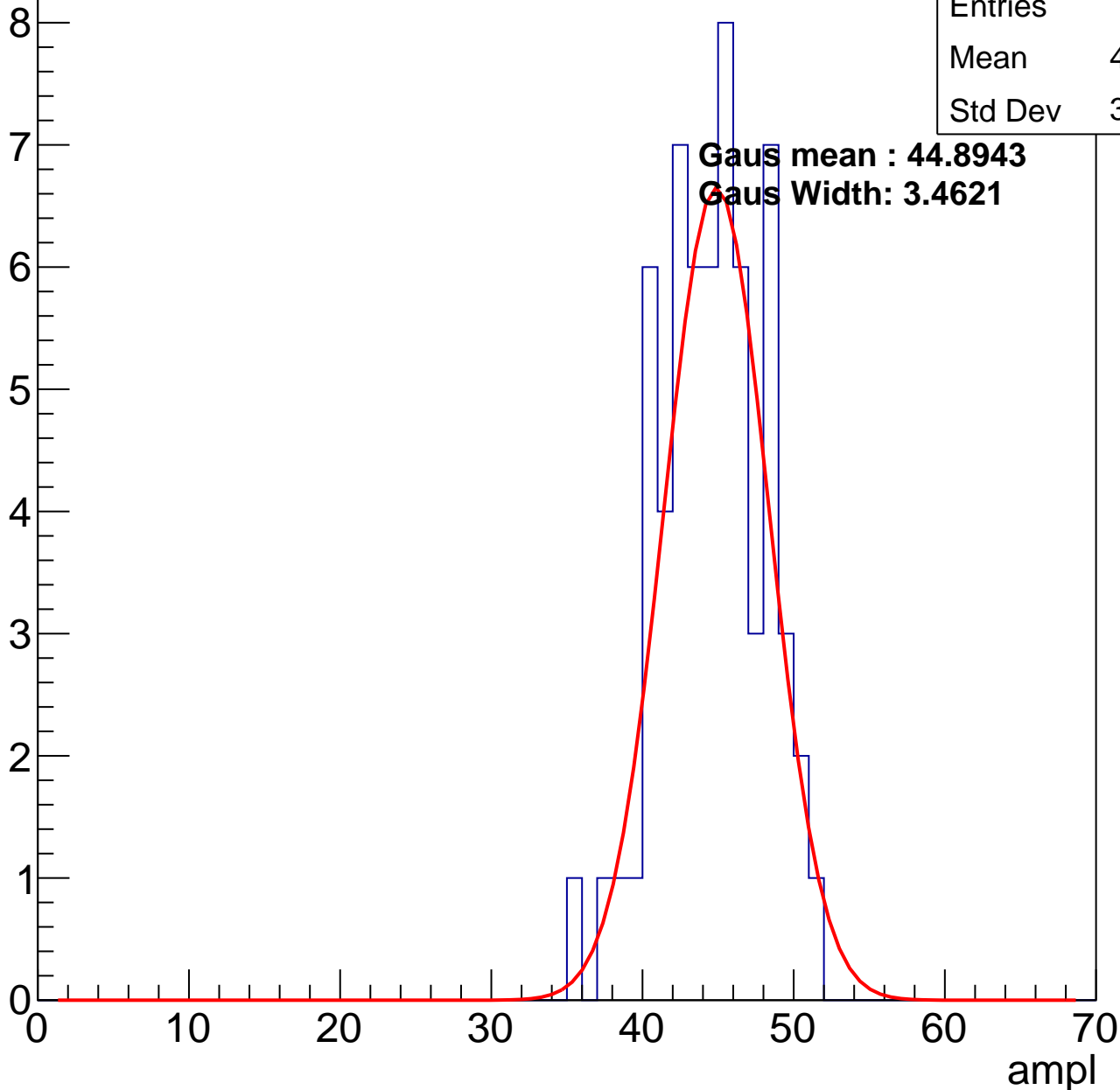
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	44.13
Std Dev	3.388

Gaus mean : 44.8943

Gaus Width: 3.4621

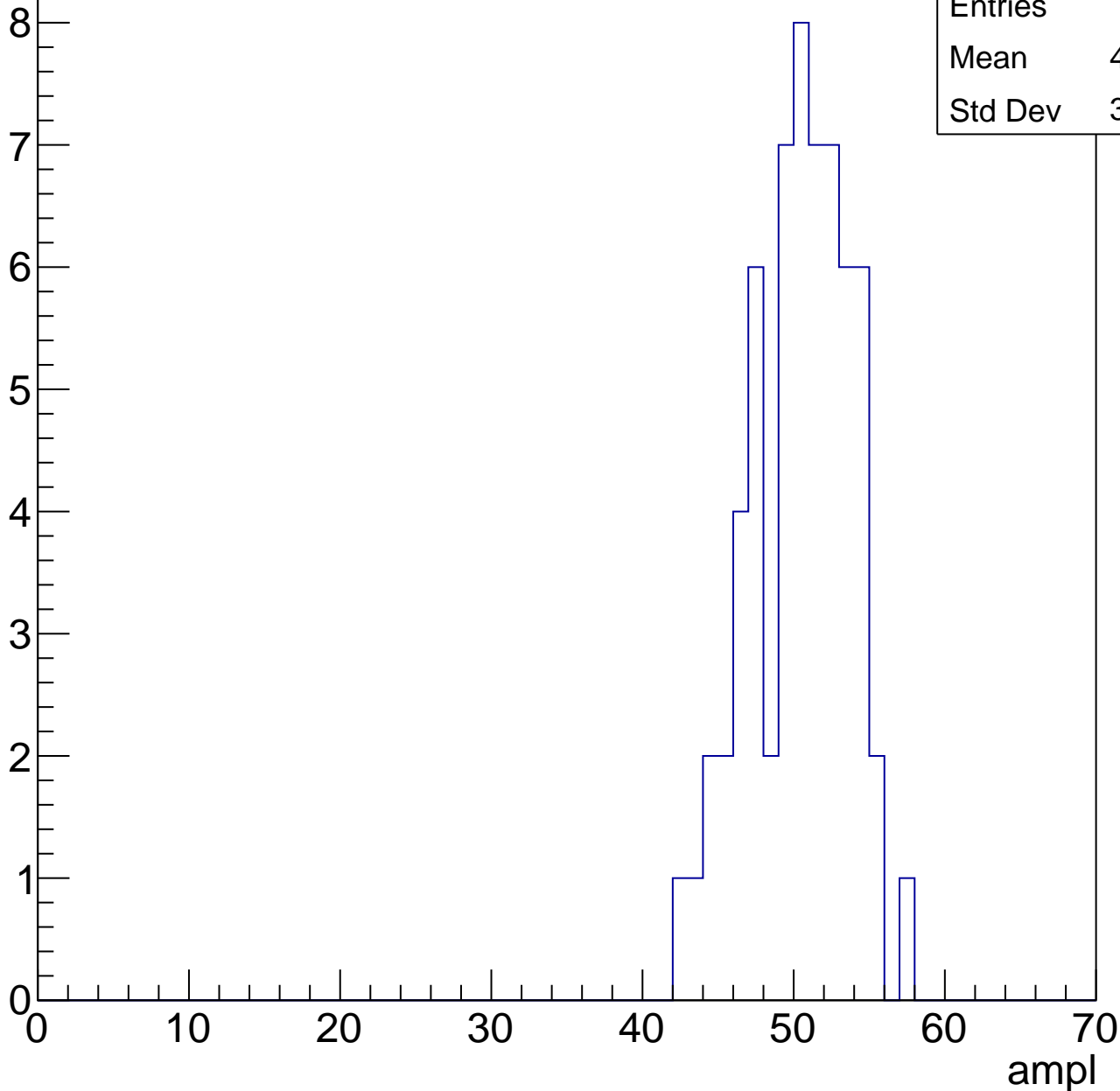


# B1L101S, U20-ch59, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	49.97
Std Dev	3.243



# B1L101S, U20-ch59, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	60
Mean	56.6
Std Dev	3.382

Entry

10

8

6

4

2

0

0

10

20

30

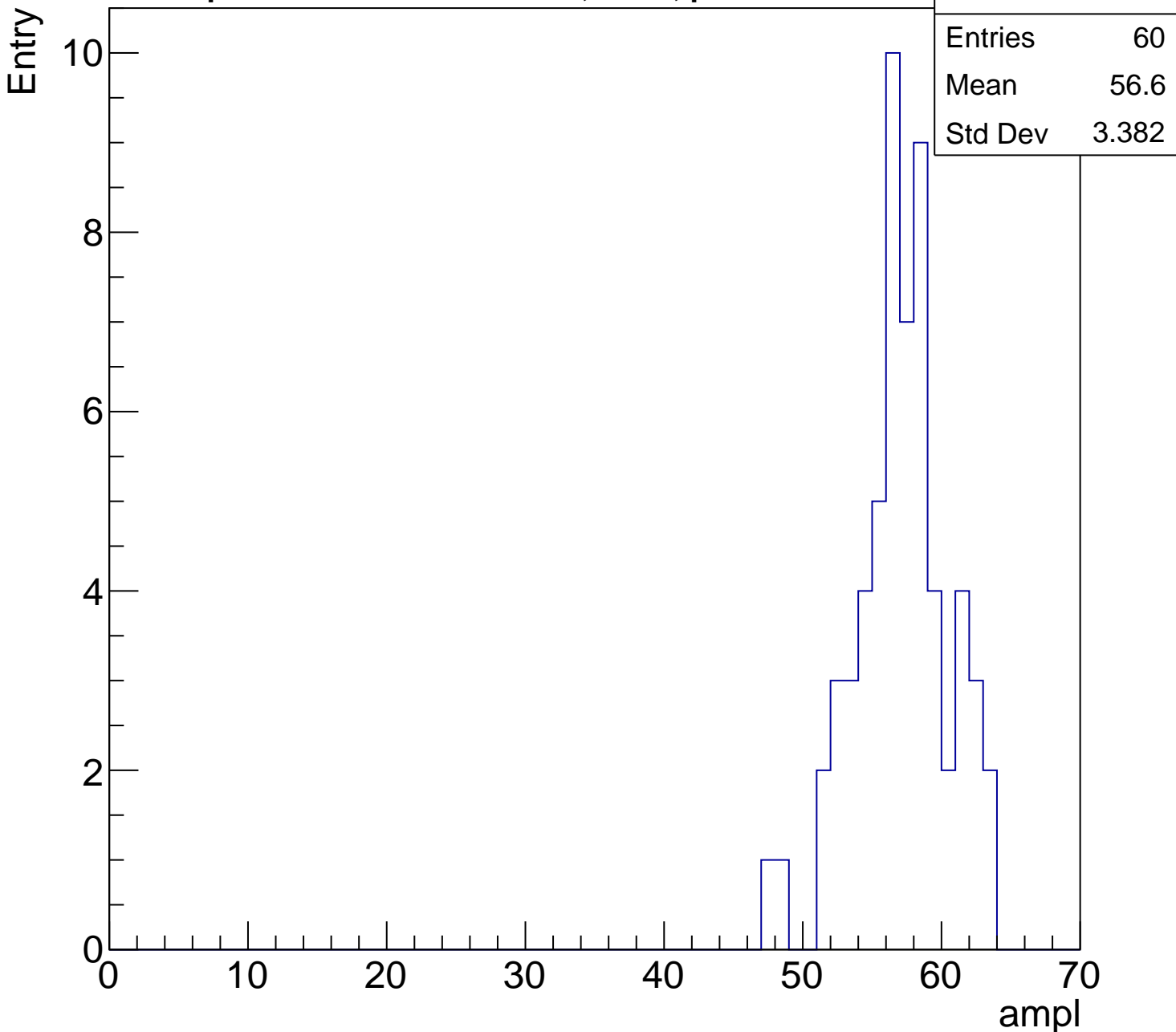
40

50

60

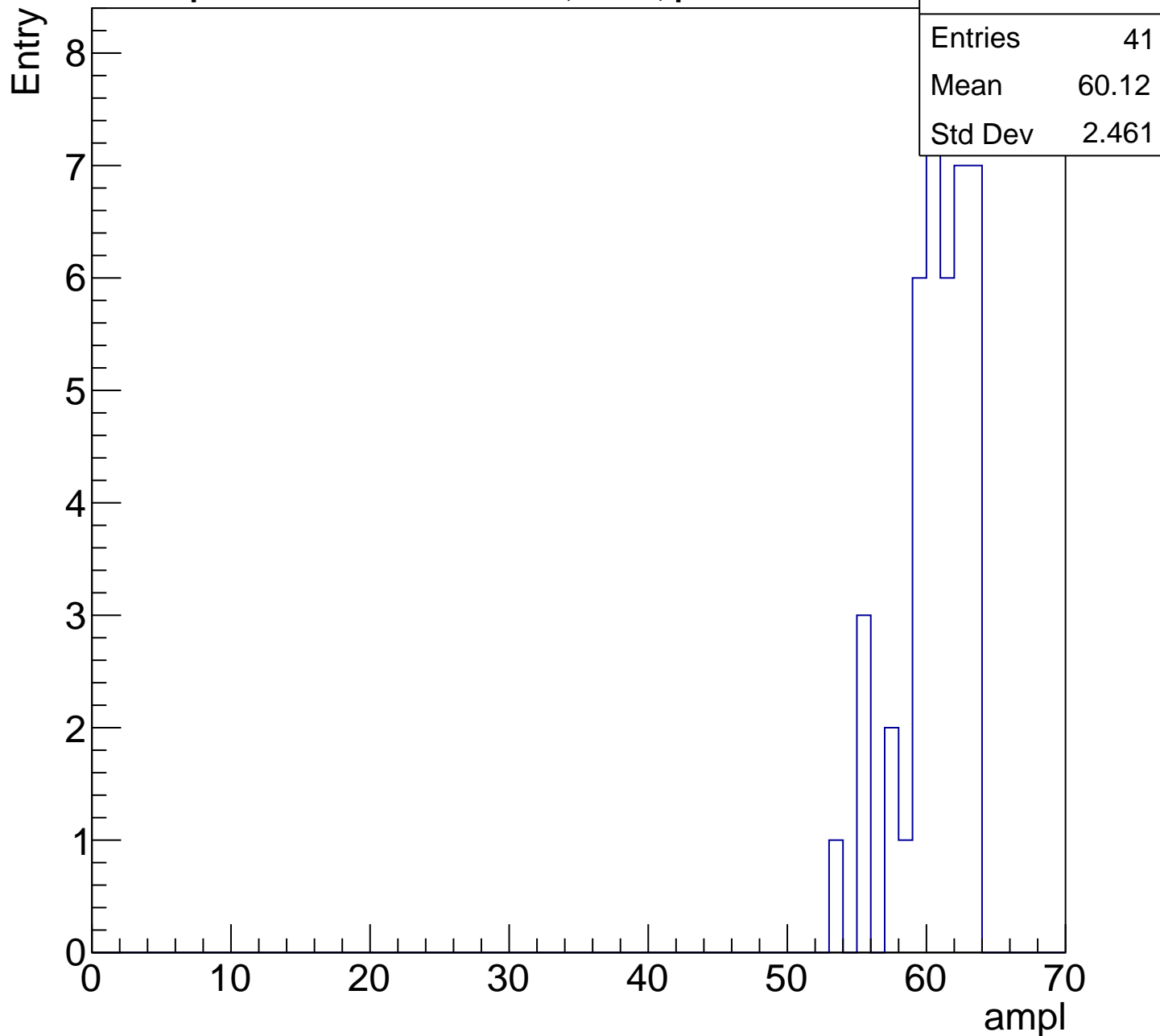
ampl

70



# B1L101S, U20-ch59, adc5

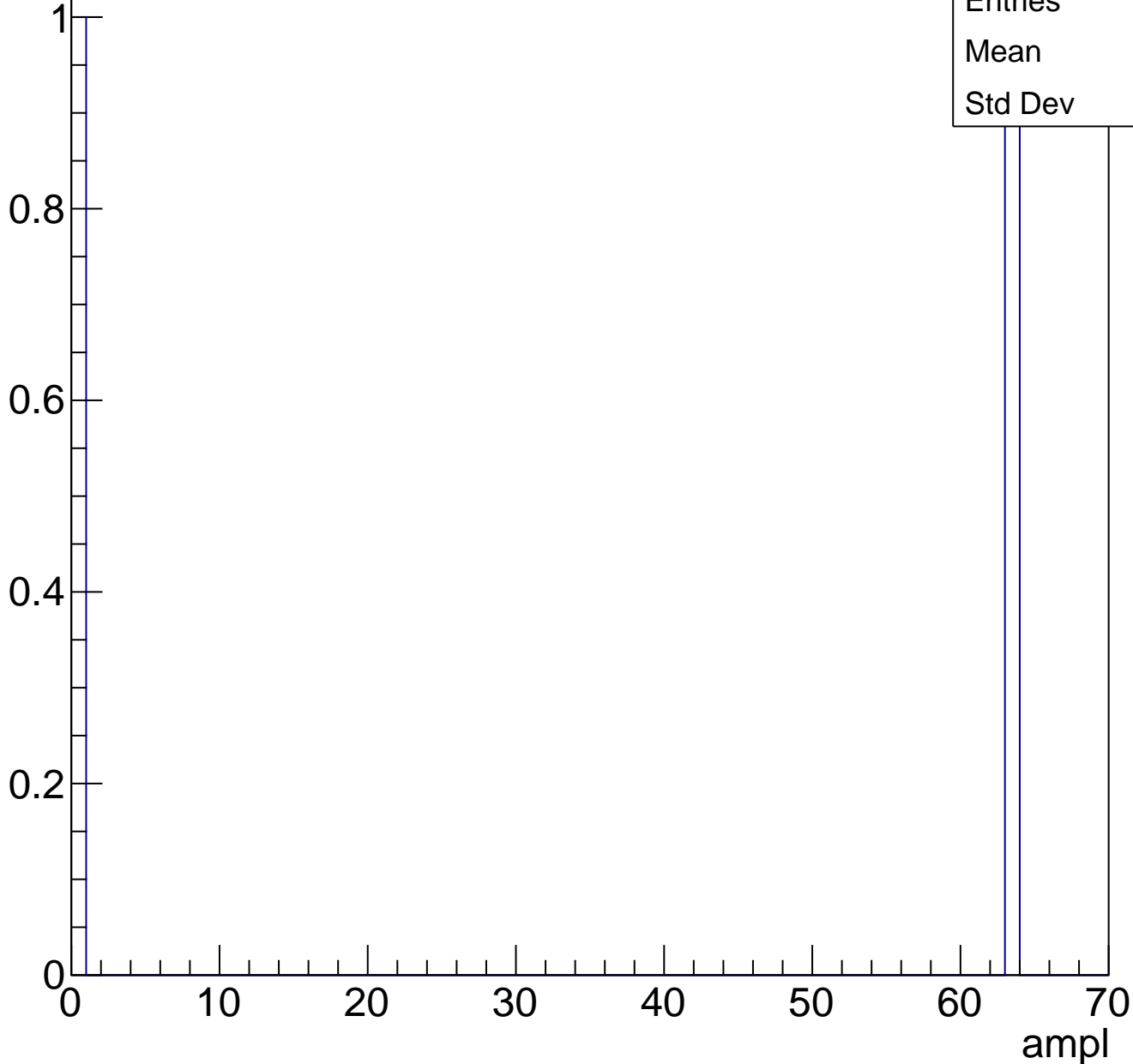
calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U20-ch59, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U20-ch59, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U20-ch60, adc0

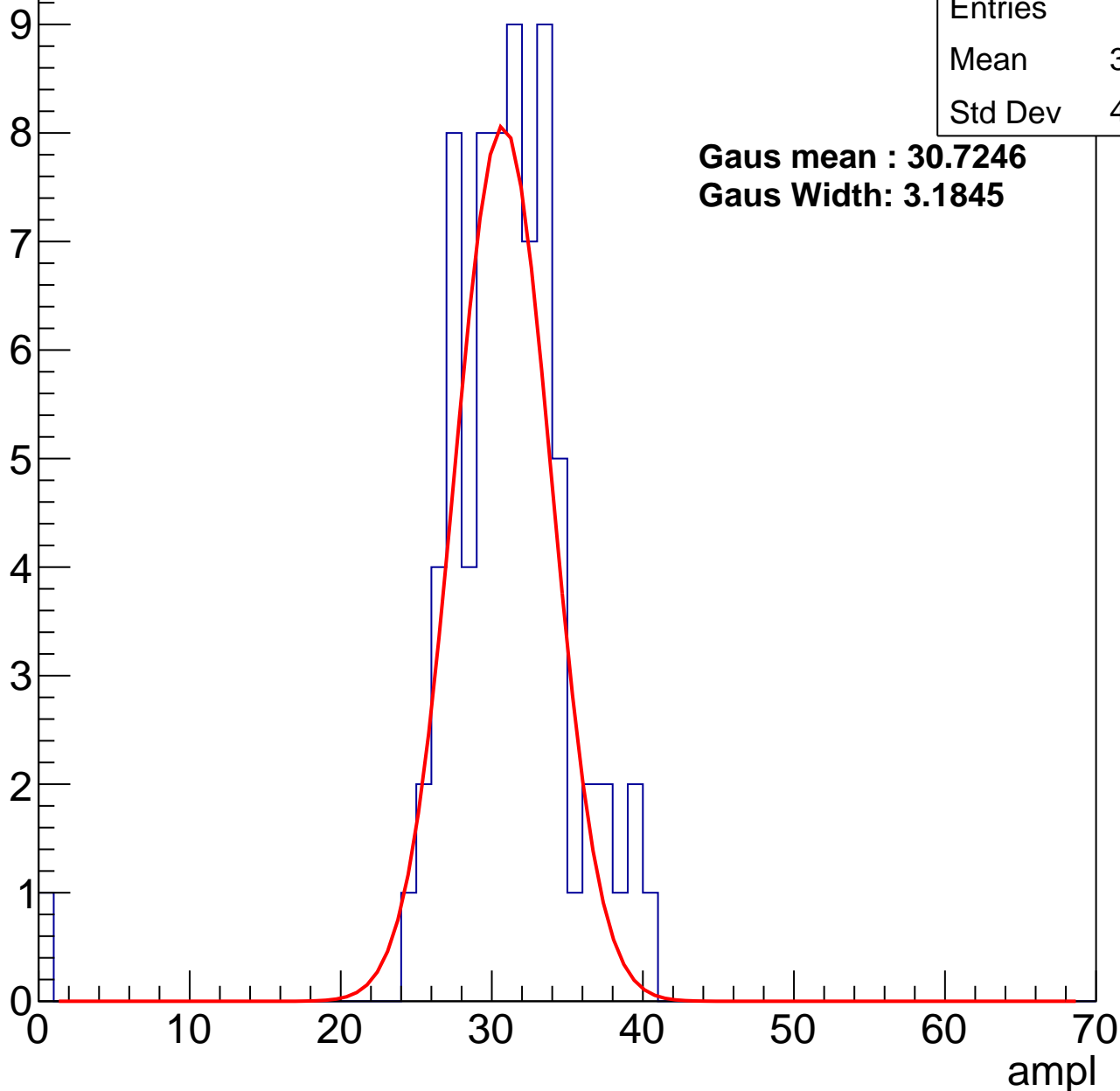
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	75
Mean	30.47
Std Dev	4.965

**Gaus mean : 30.7246**

**Gaus Width: 3.1845**



# B1L101S, U20-ch60, adc1

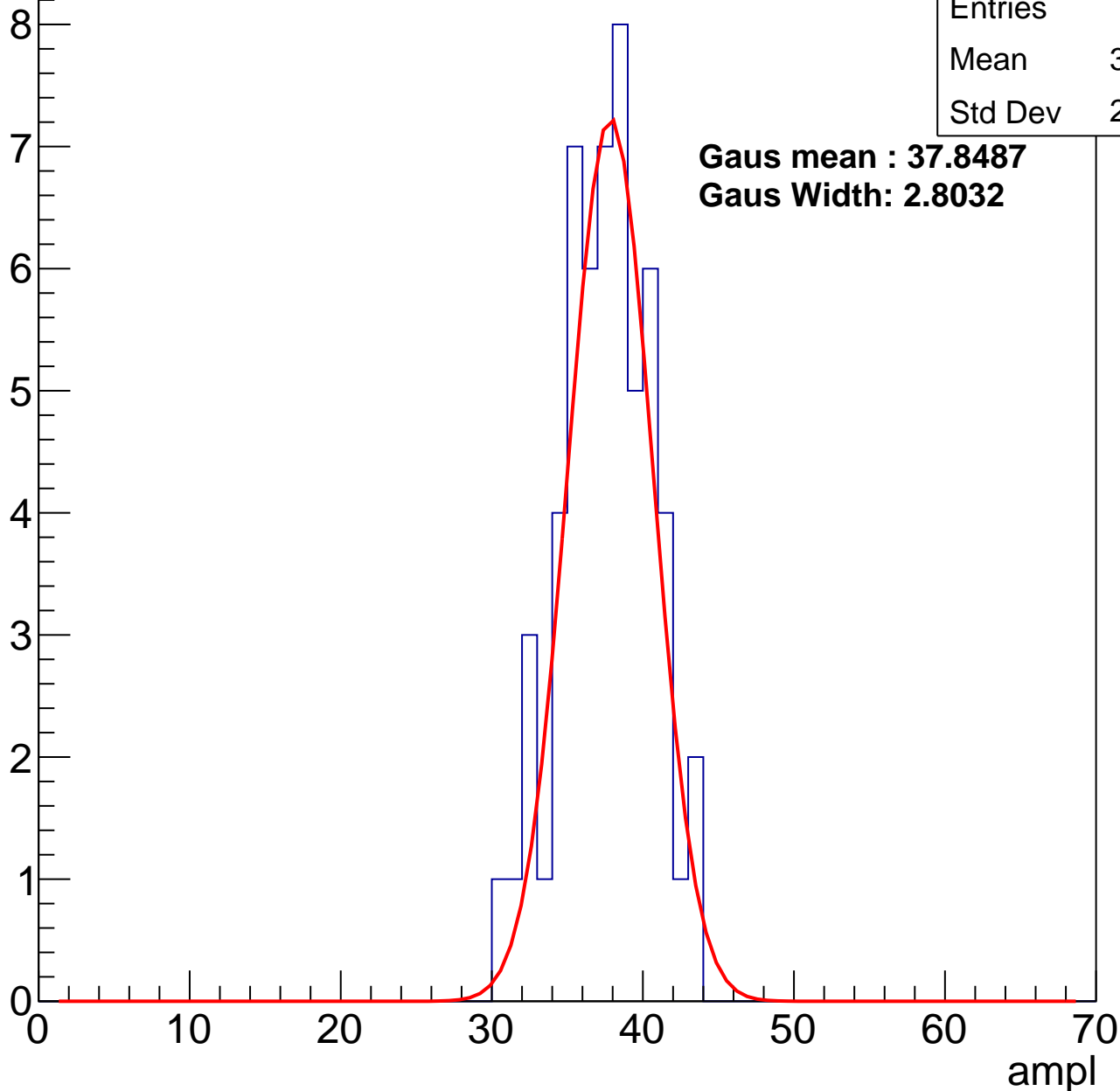
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	56
Mean	37.09
Std Dev	2.954

**Gaus mean : 37.8487**

**Gaus Width: 2.8032**



# B1L101S, U20-ch60, adc2

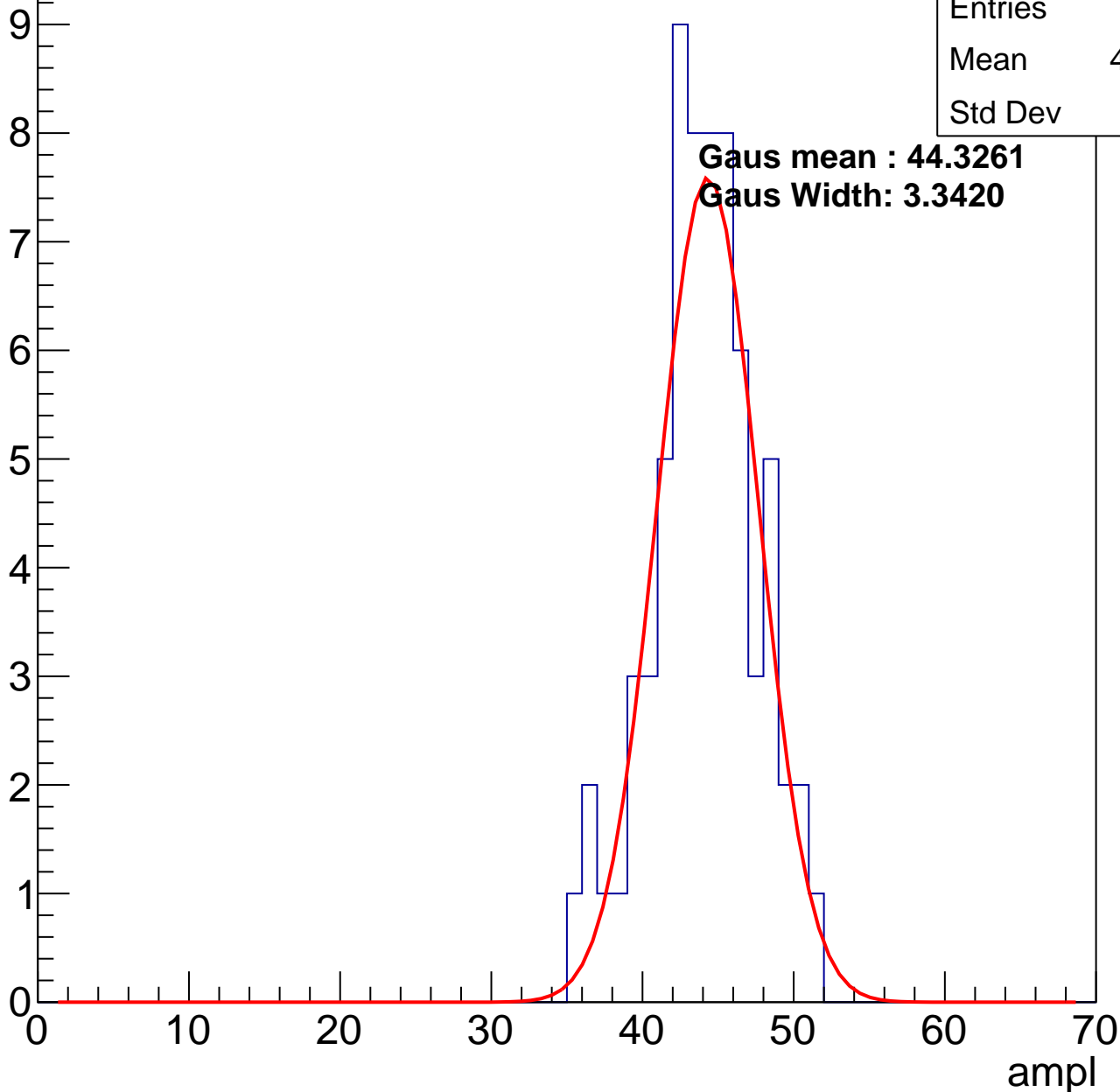
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	43.59
Std Dev	3.44

**Gaus mean : 44.3261**

**Gaus Width: 3.3420**

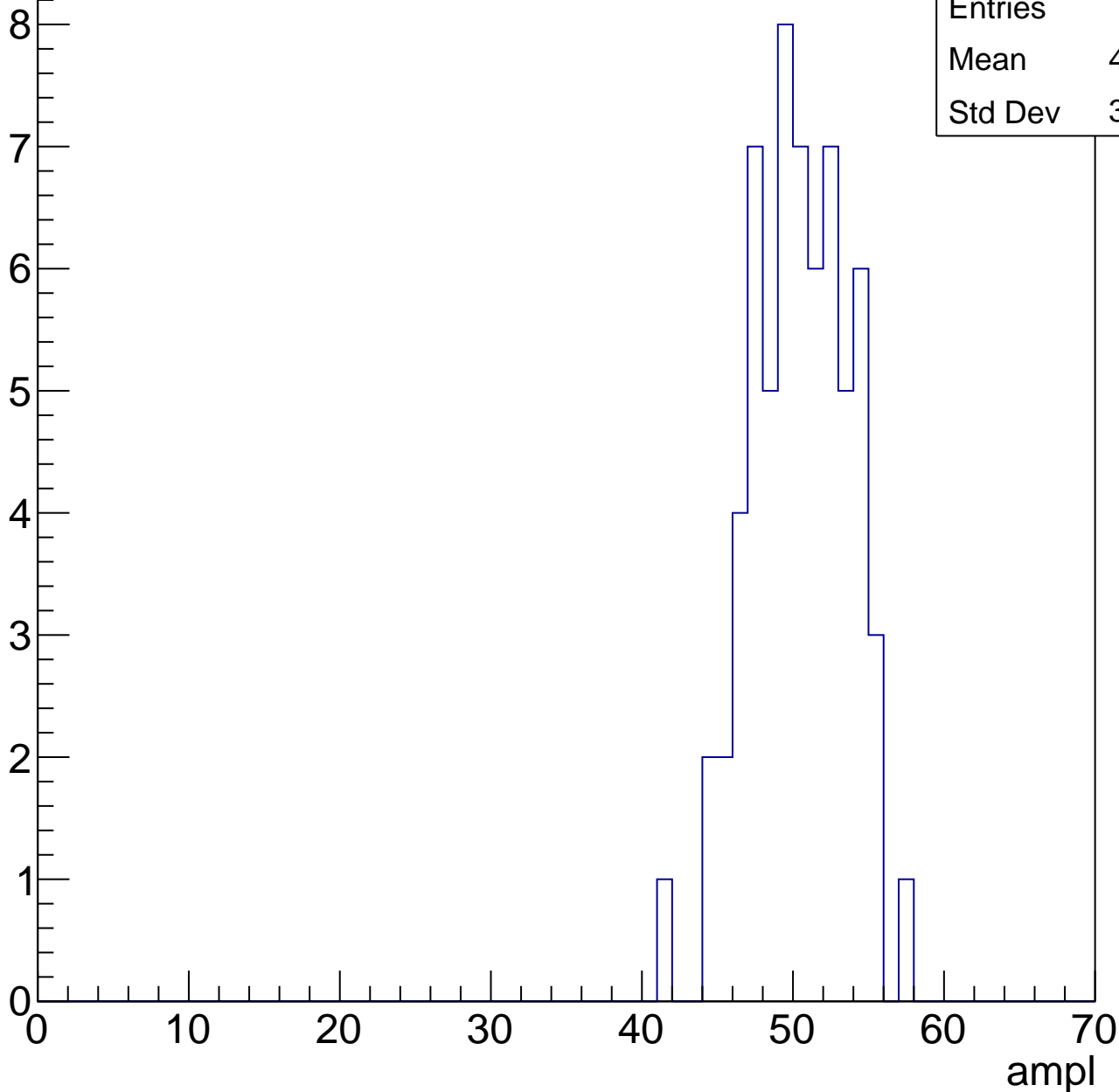


# B1L101S, U20-ch60, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	49.92
Std Dev	3.203

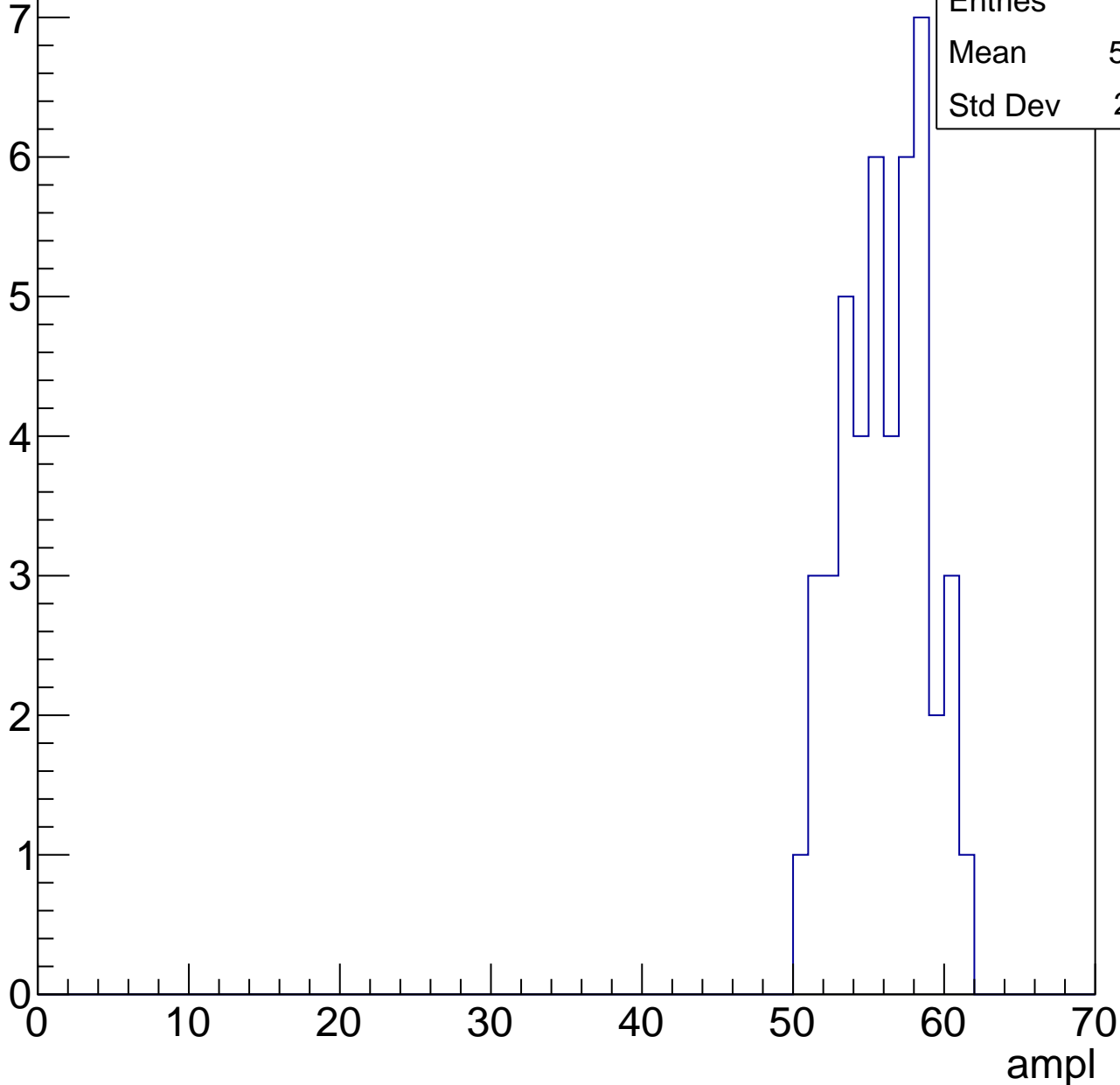


# B1L101S, U20-ch60, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

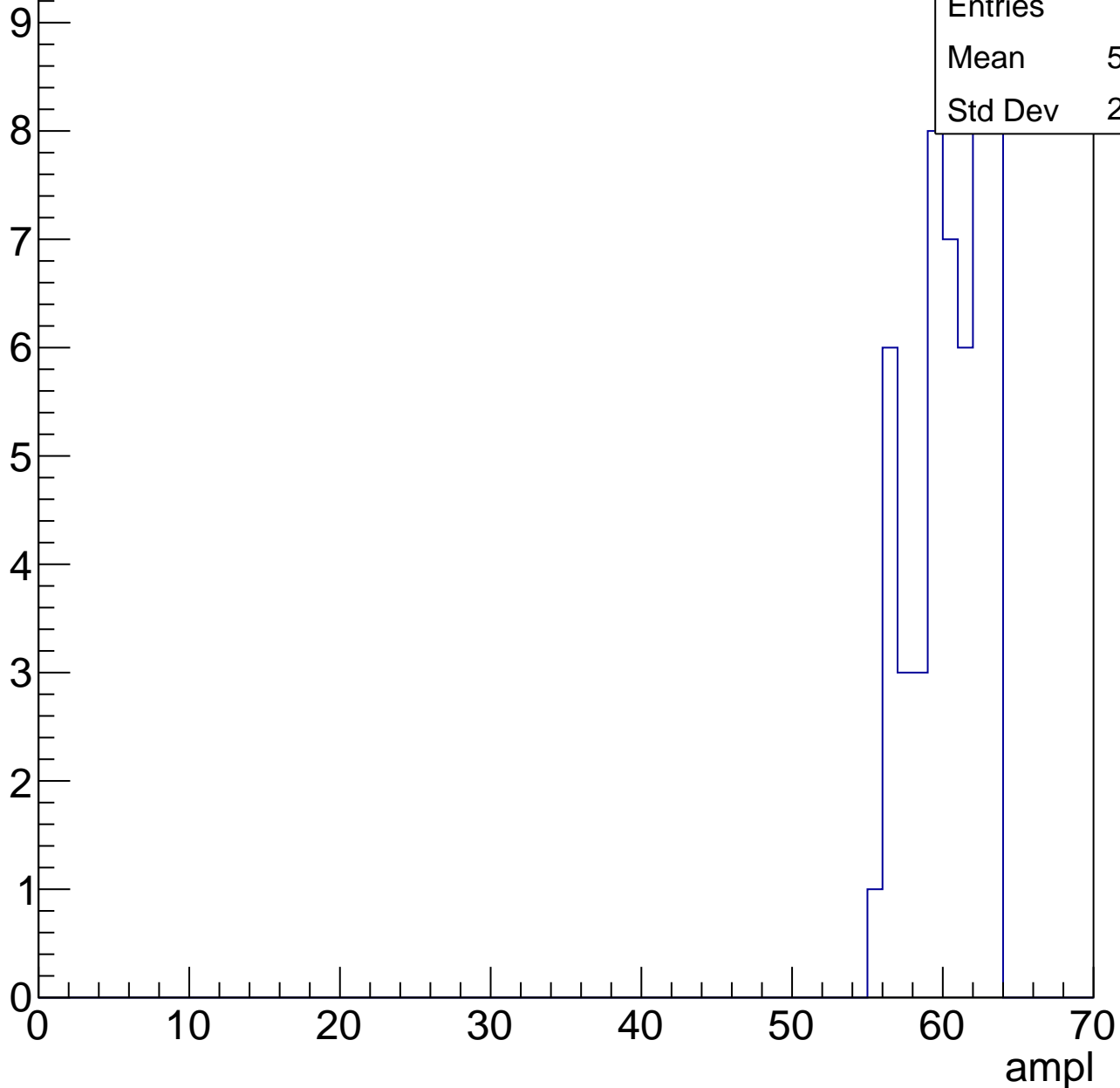
Entries	45
Mean	55.58
Std Dev	2.761



# B1L101S, U20-ch60, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

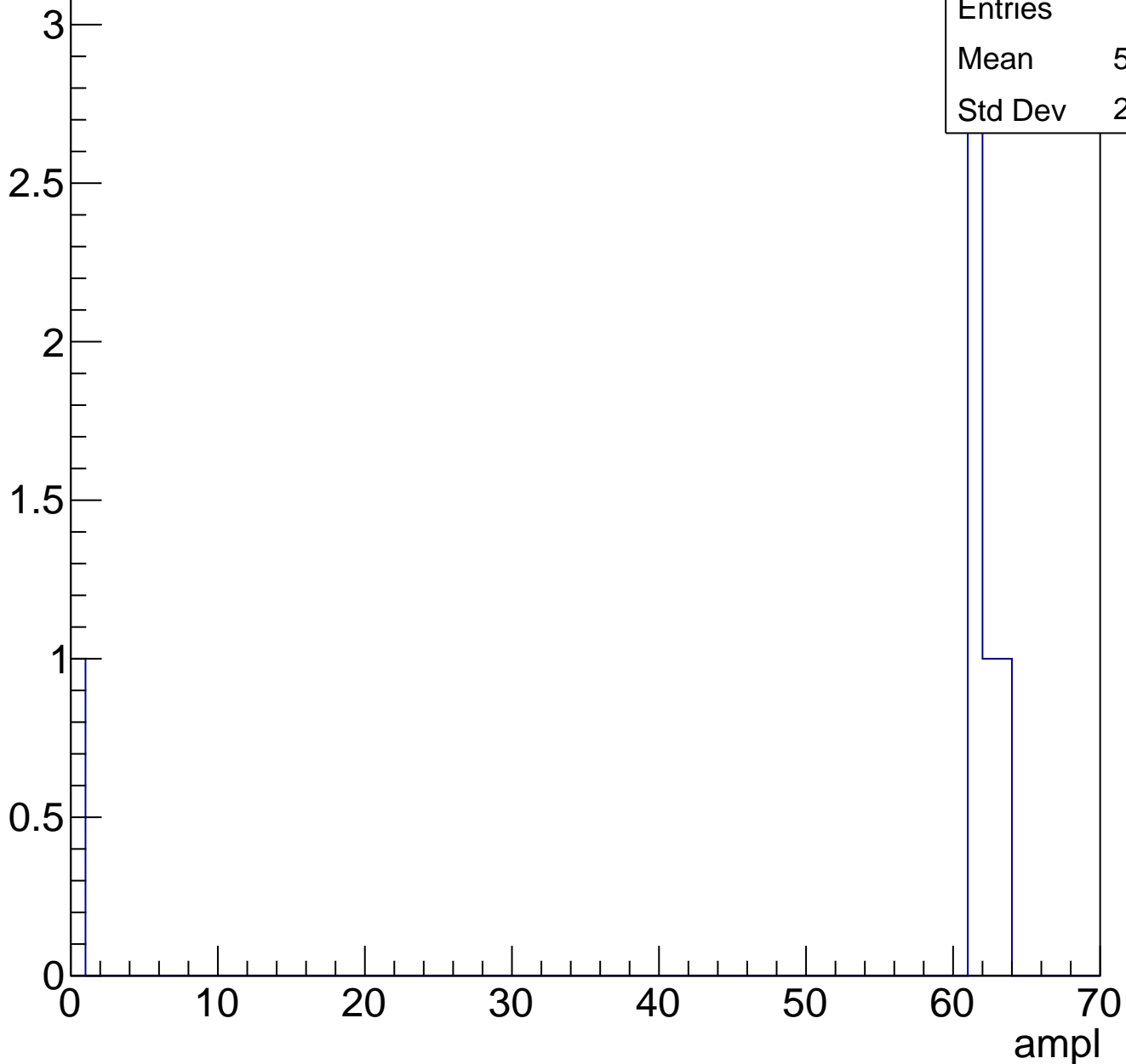


Entries	52
Mean	59.98
Std Dev	2.366

# B1L101S, U20-ch60, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U20-ch60, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	2
Mean	11
Std Dev	11

# B1L101S, U20-ch61, adc0

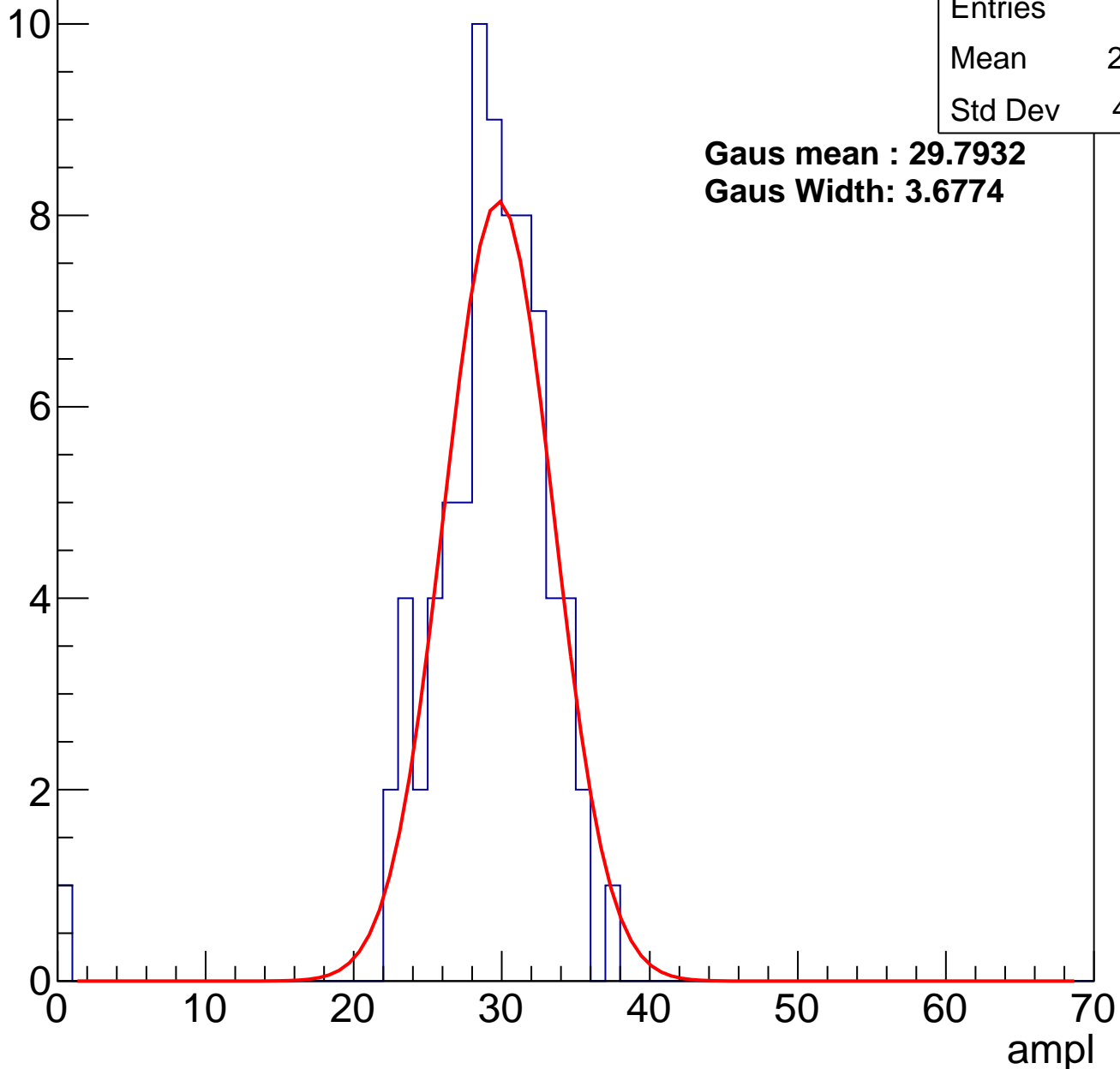
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	76
Mean	28.64
Std Dev	4.681

**Gaus mean : 29.7932**

**Gaus Width: 3.6774**

Entry



# B1L101S, U20-ch61, adc1

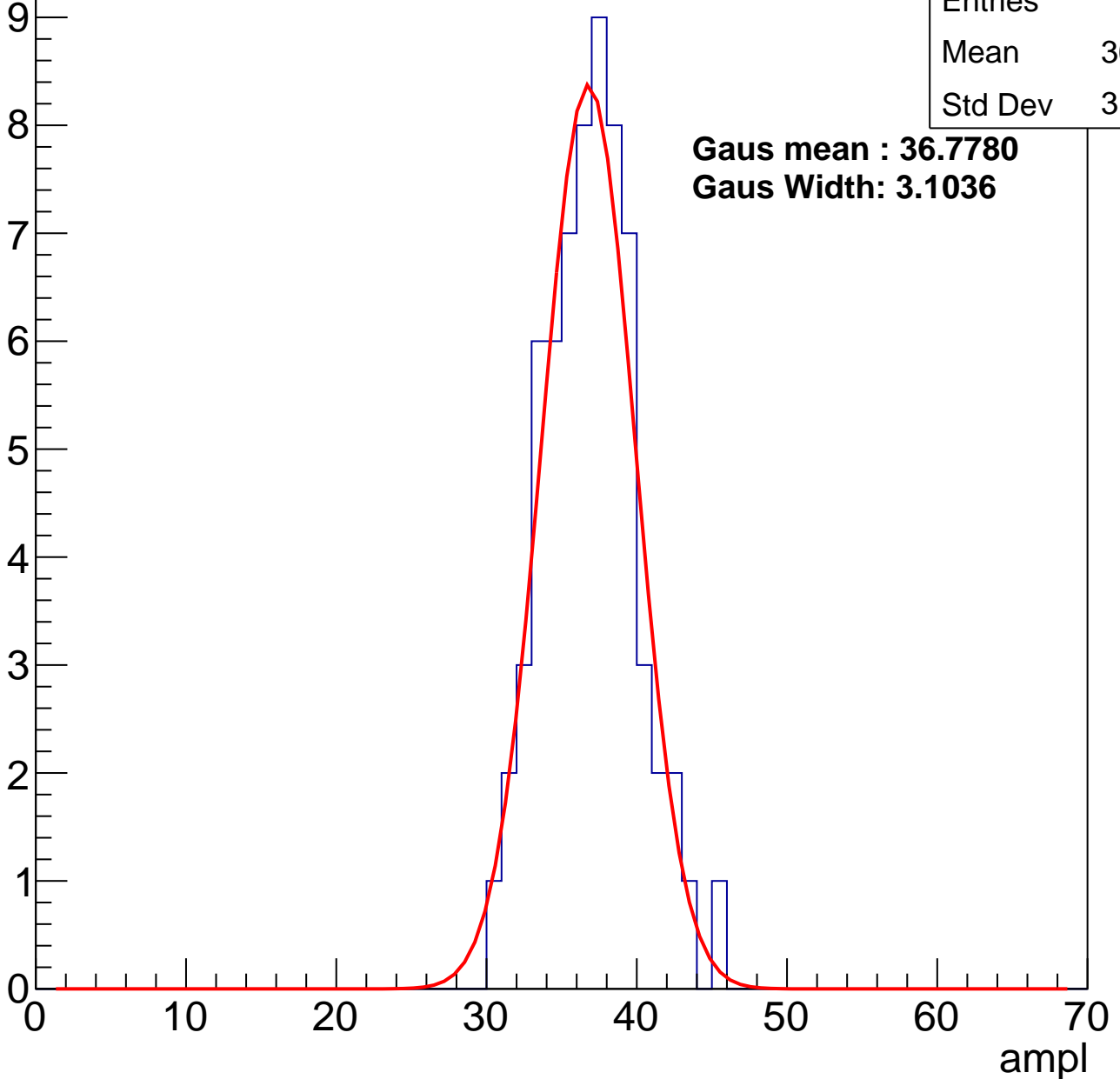
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	66
Mean	36.47
Std Dev	3.036

**Gaus mean : 36.7780**

**Gaus Width: 3.1036**



# B1L101S, U20-ch61, adc2

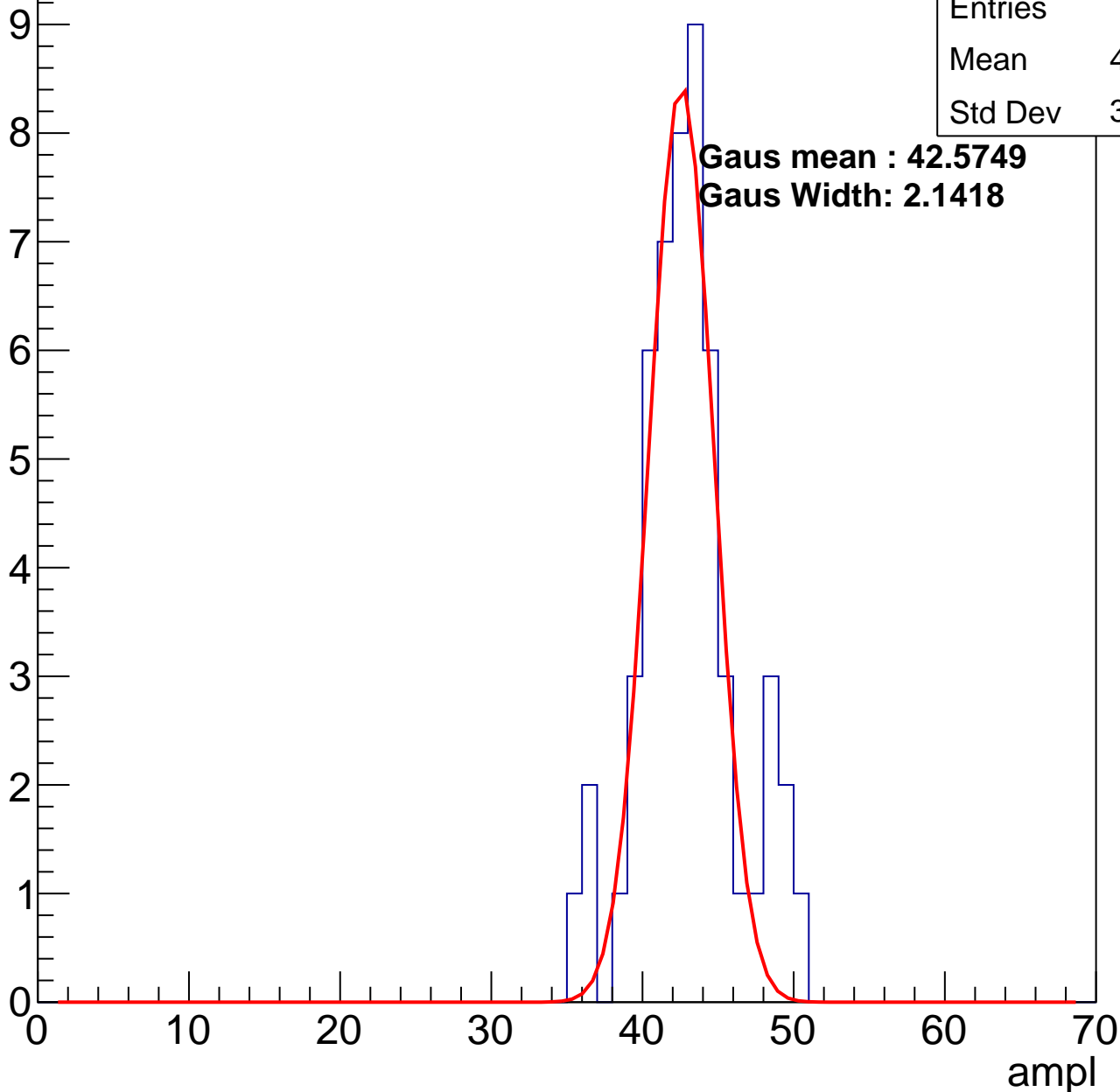
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	54
Mean	42.52
Std Dev	3.196

**Gaus mean : 42.5749**

**Gaus Width: 2.1418**

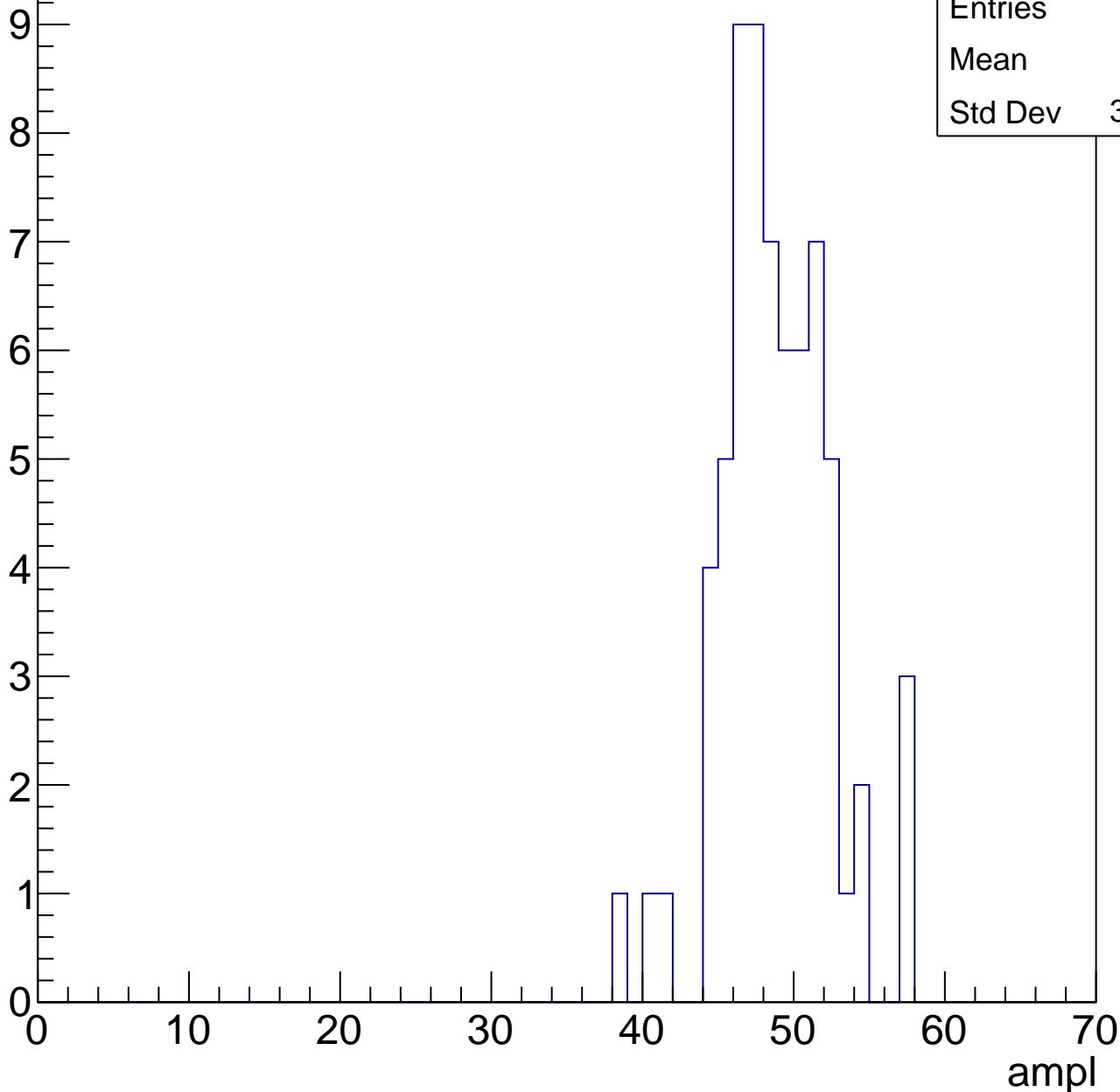


# B1L101S, U20-ch61, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	67
Mean	48.3
Std Dev	3.612



# B1L101S, U20-ch61, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	57
Mean	54.39
Std Dev	3.21

Entry

10

8

6

4

2

0

0

10

20

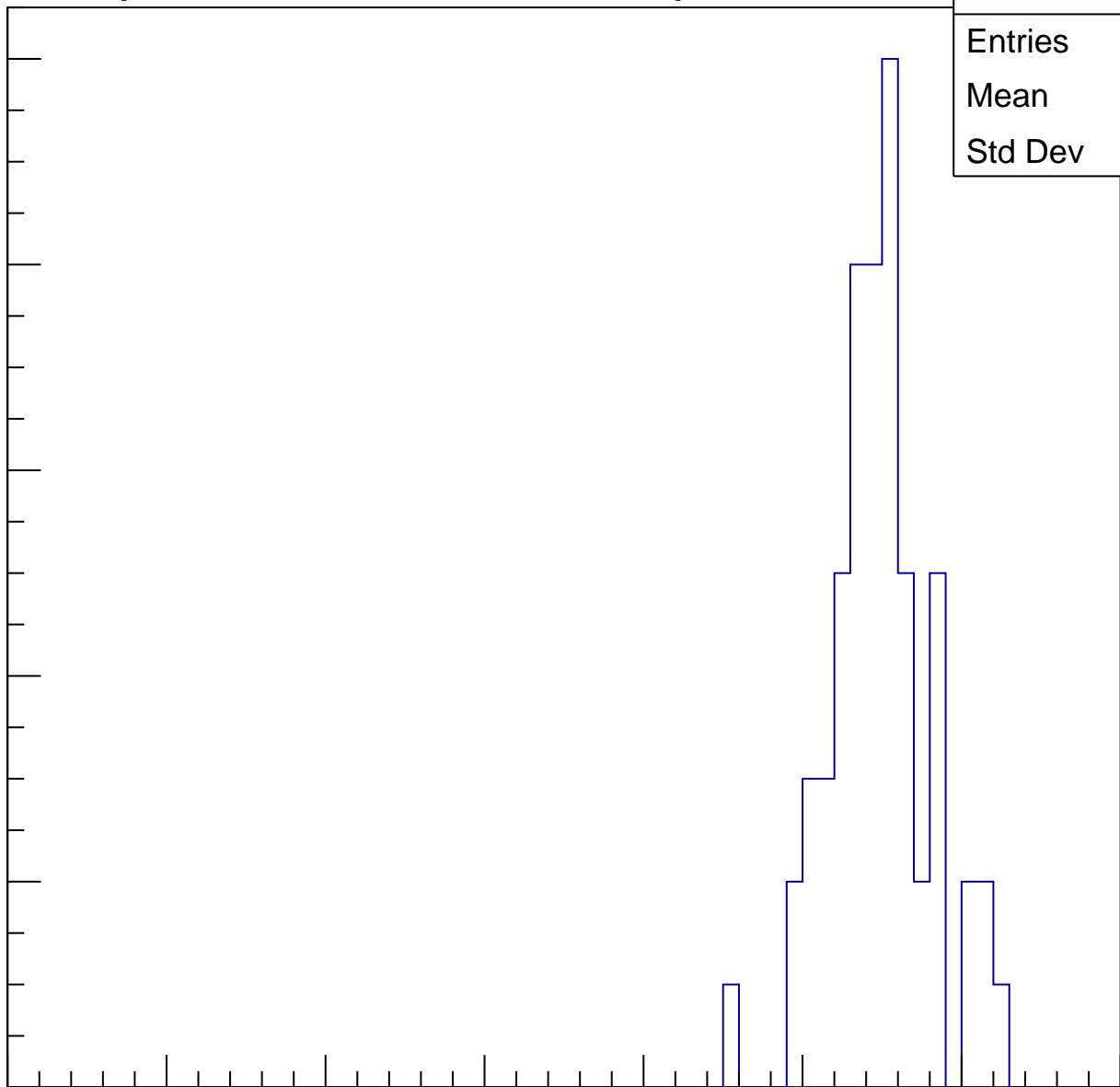
30

40

50

60

ampl

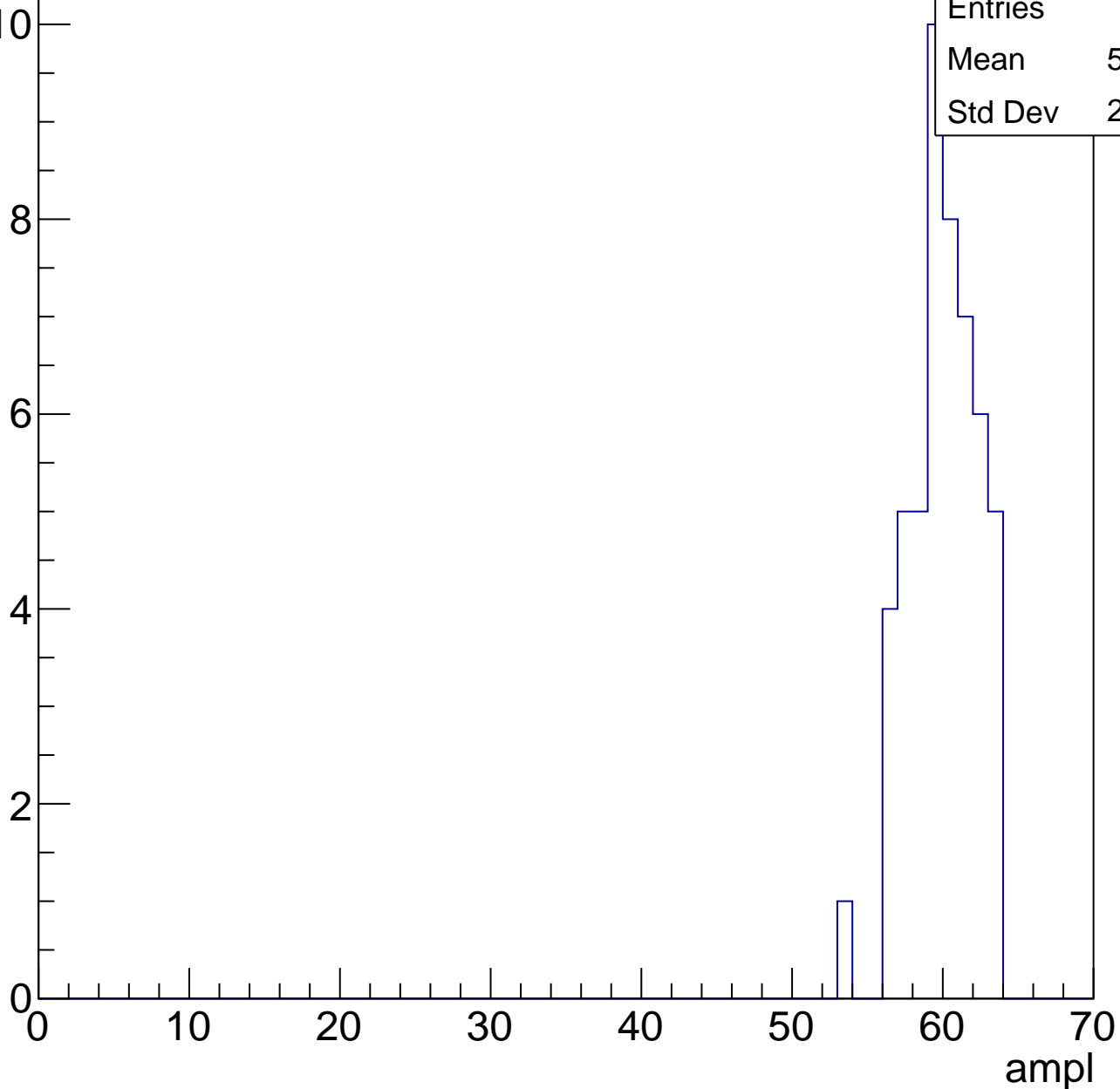


# B1L101S, U20-ch61, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	51
Mean	59.53
Std Dev	2.226

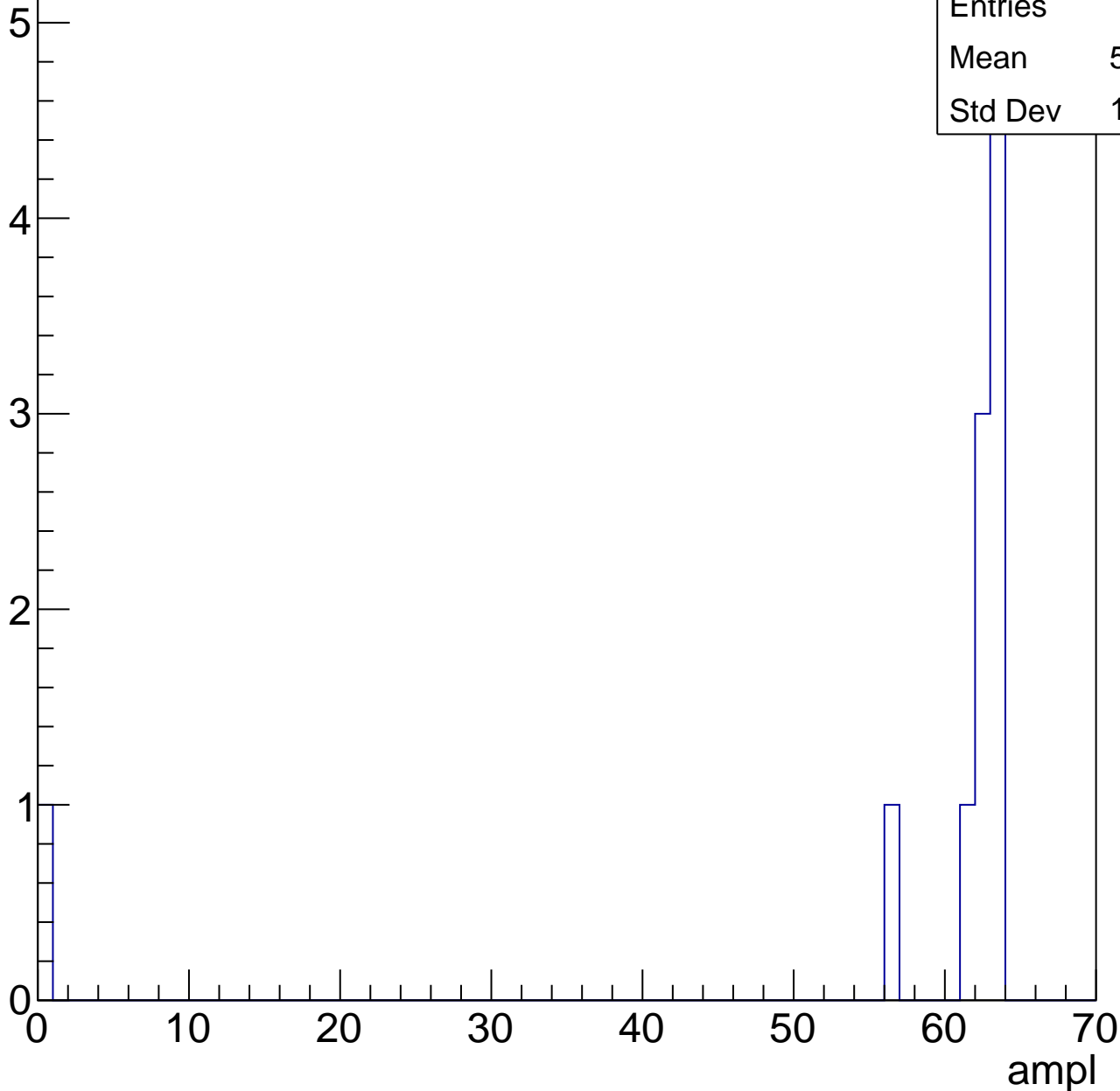


# B1L101S, U20-ch61, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	11
Mean	56.18
Std Dev	17.87





# B1L101S, U20-ch61, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U20-ch62, adc0

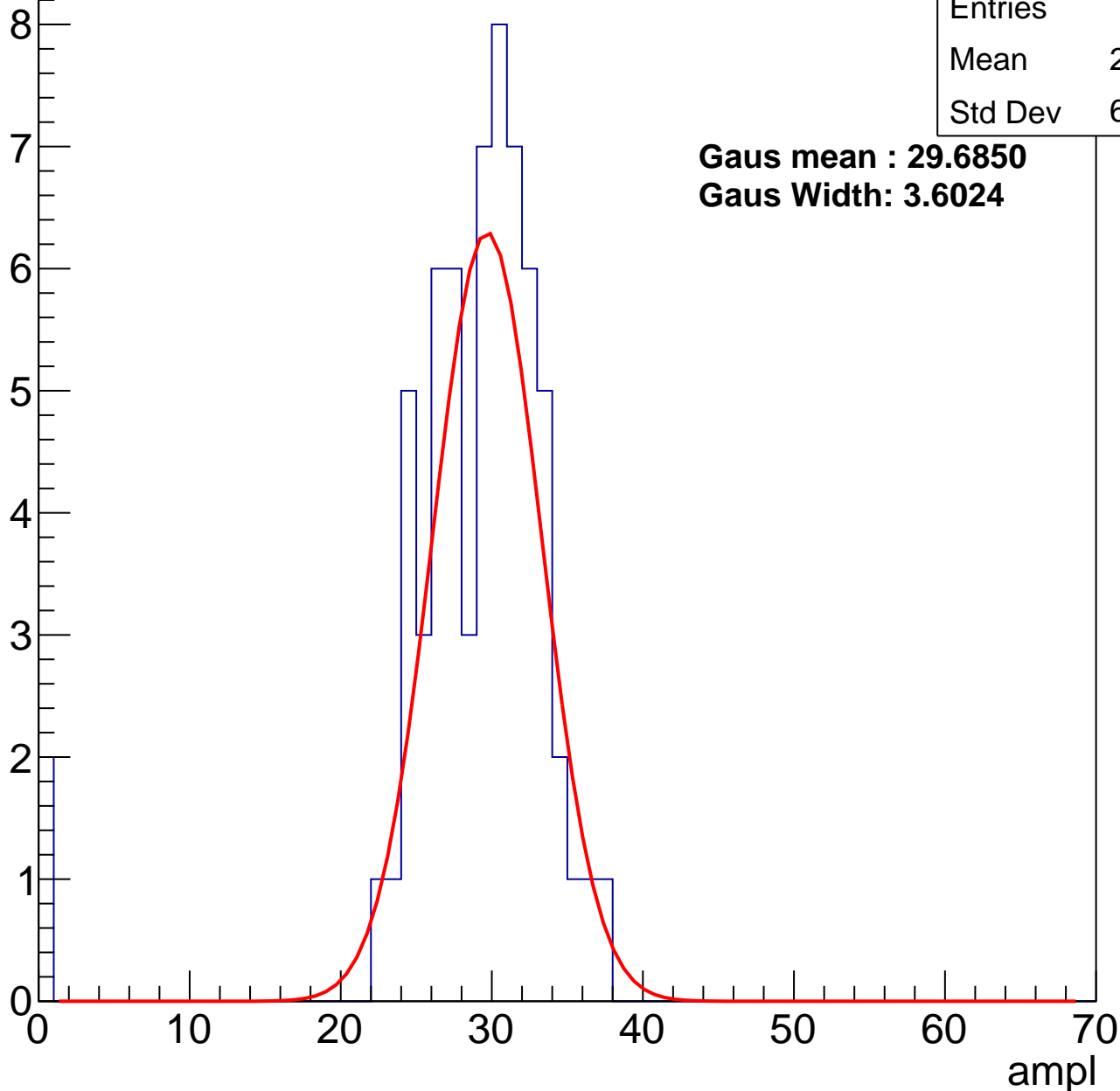
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	28.23
Std Dev	6.015

**Gaus mean : 29.6850**

**Gaus Width: 3.6024**



# B1L101S, U20-ch62, adc1

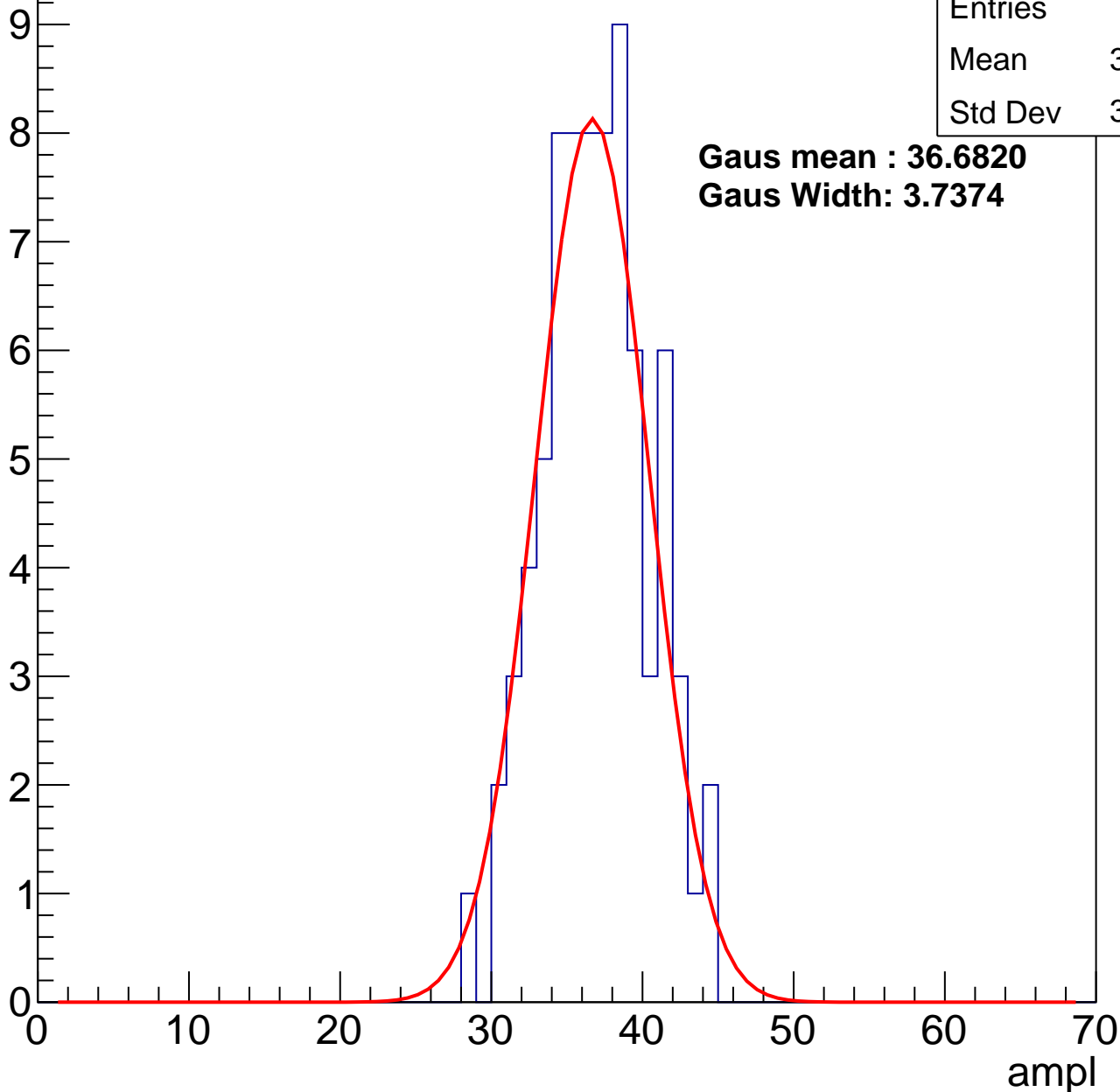
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	77
Mean	36.48
Std Dev	3.463

**Gaus mean : 36.6820**

**Gaus Width: 3.7374**



# B1L101S, U20-ch62, adc2

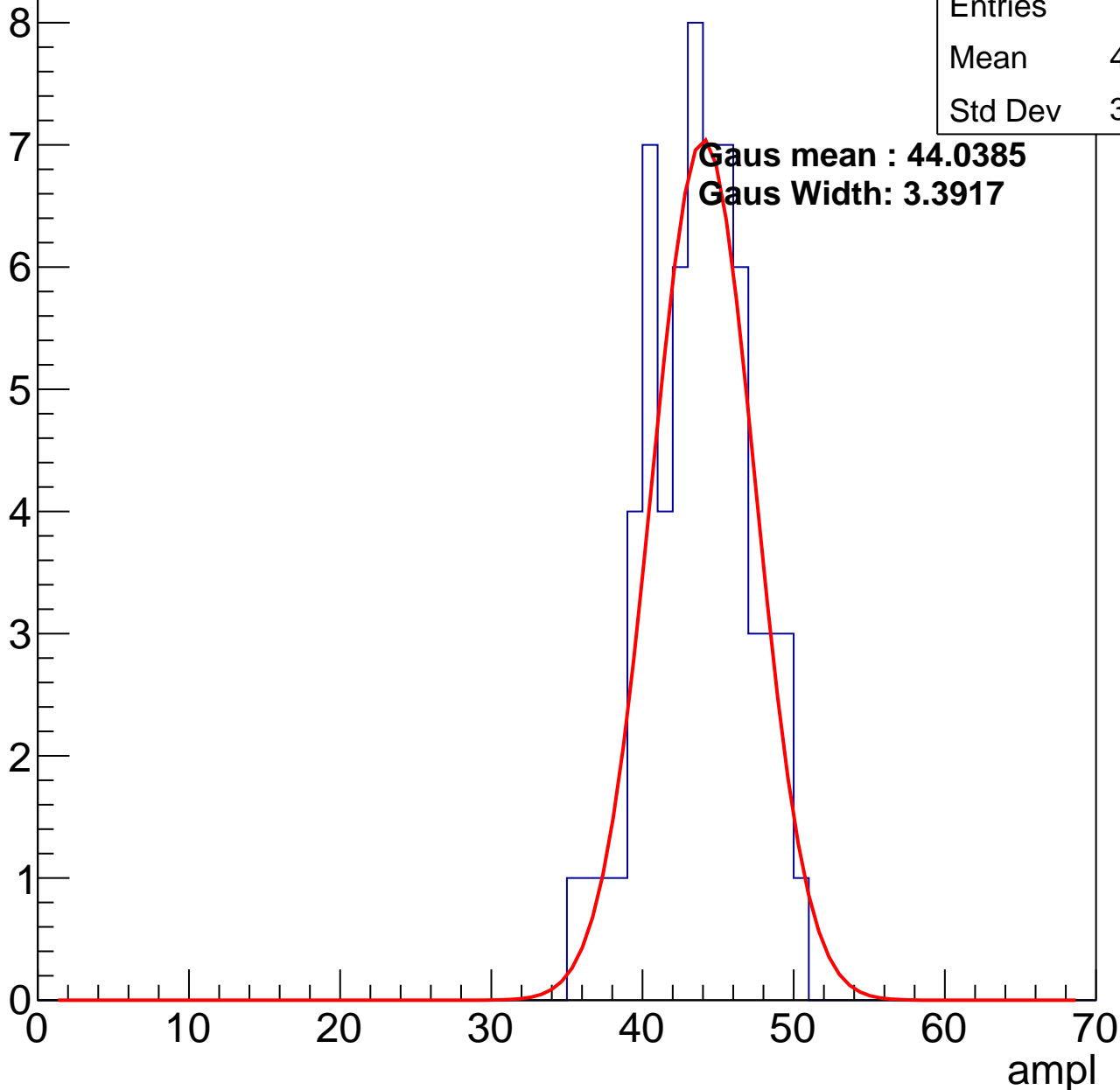
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	43.22
Std Dev	3.307

**Gaus mean : 44.0385**

**Gaus Width: 3.3917**

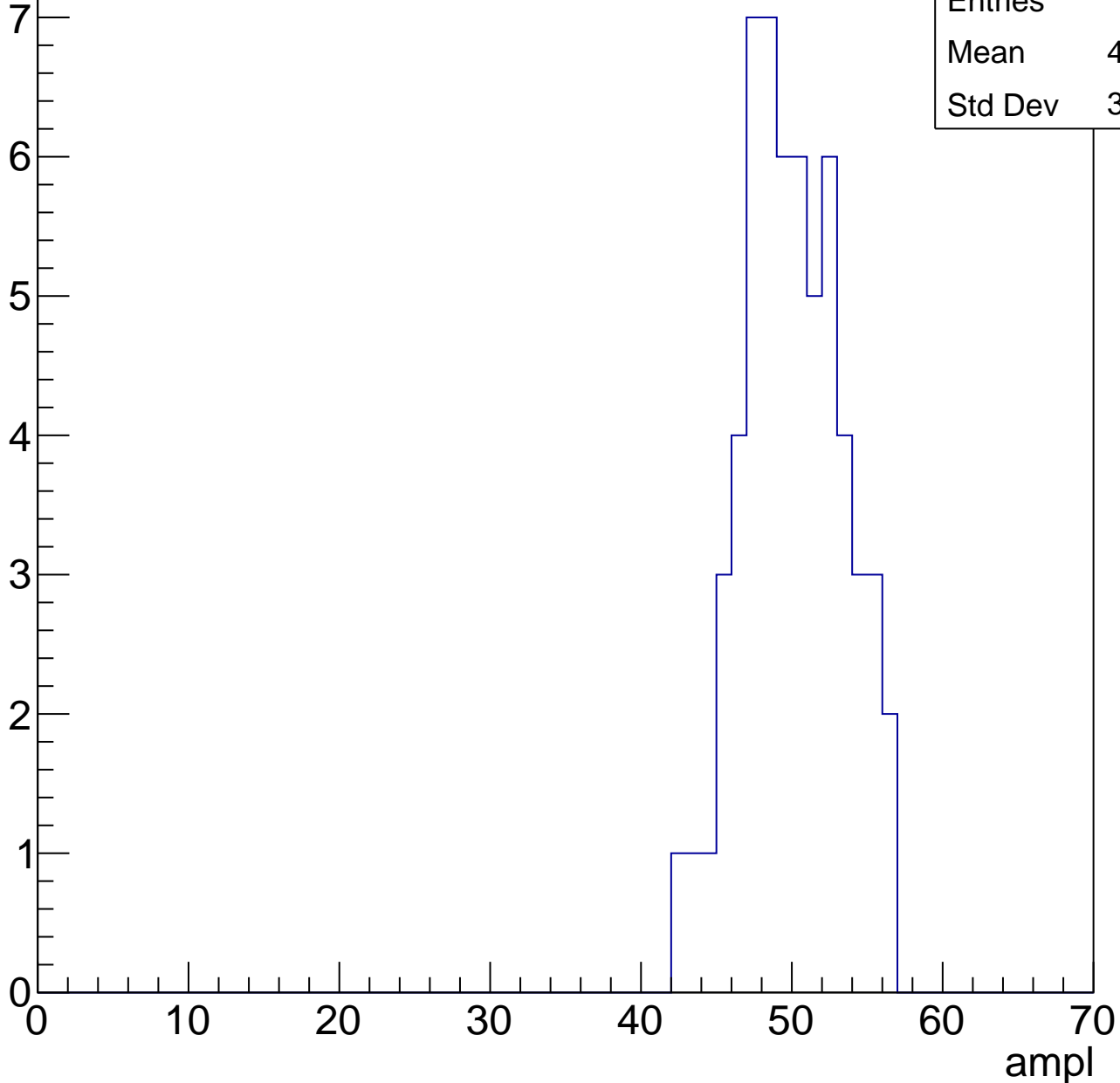


# B1L101S, U20-ch62, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	59
Mean	49.58
Std Dev	3.279

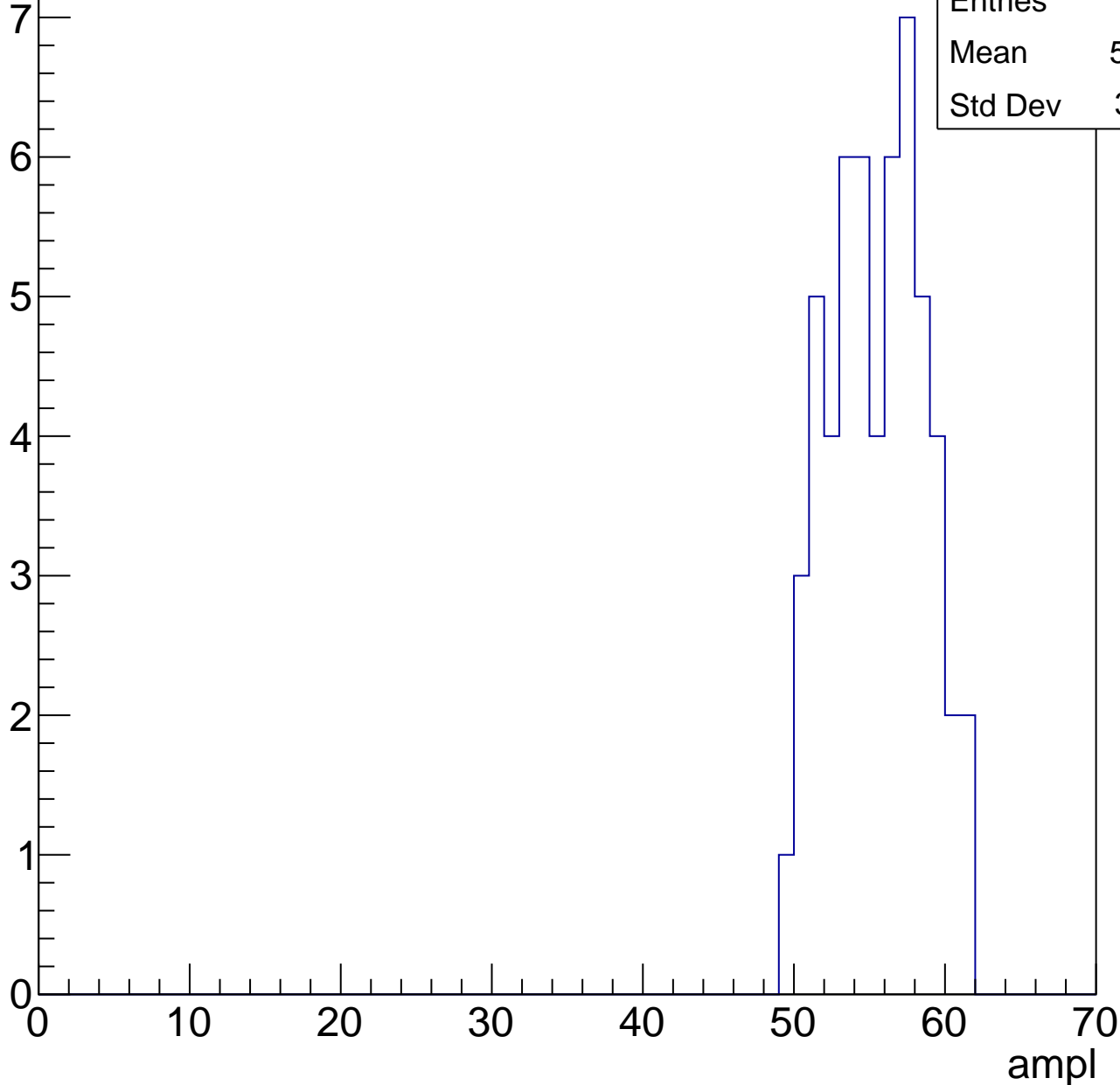


# B1L101S, U20-ch62, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

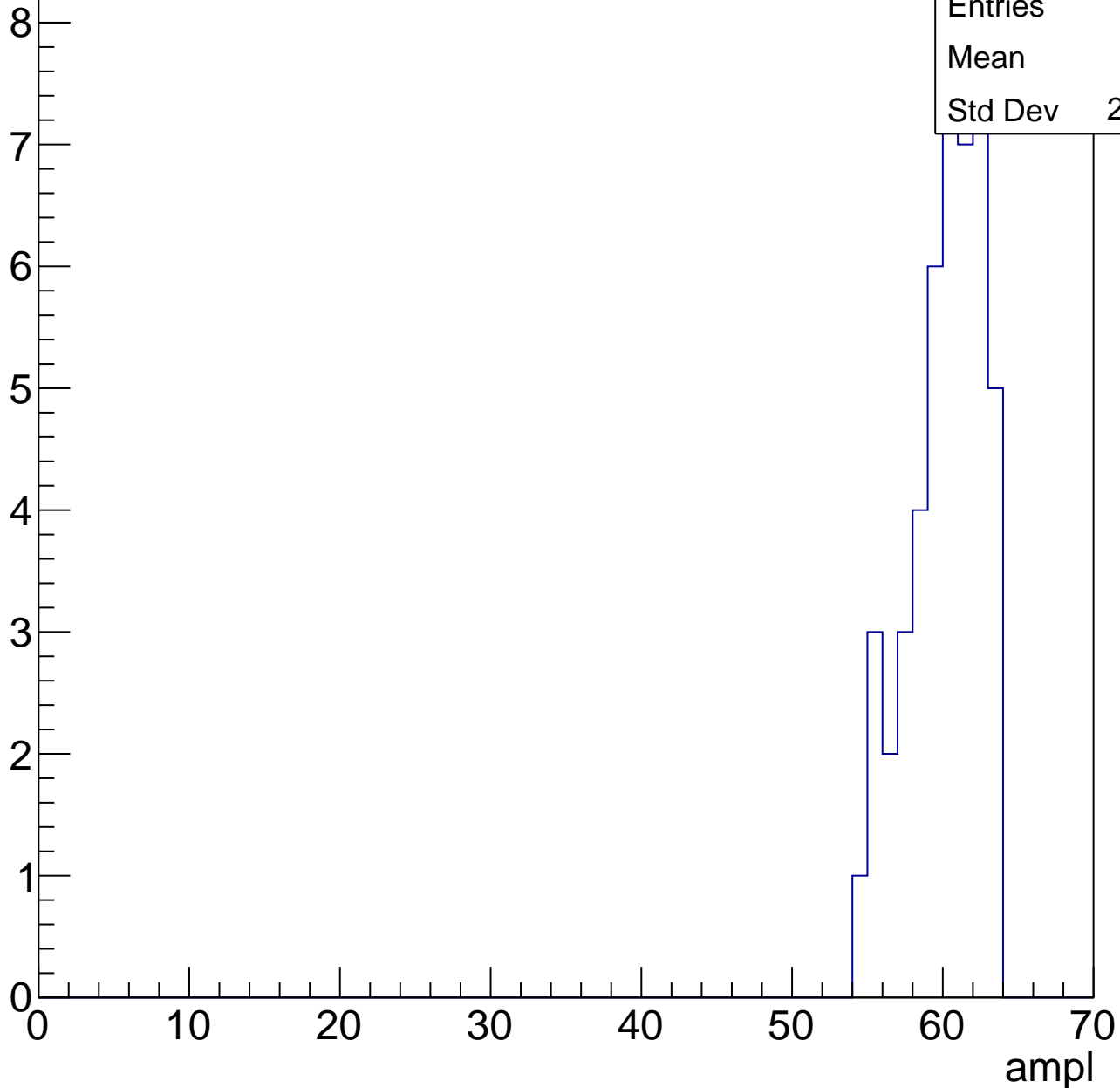
Entries	55
Mean	55.04
Std Dev	3.081



# B1L101S, U20-ch62, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



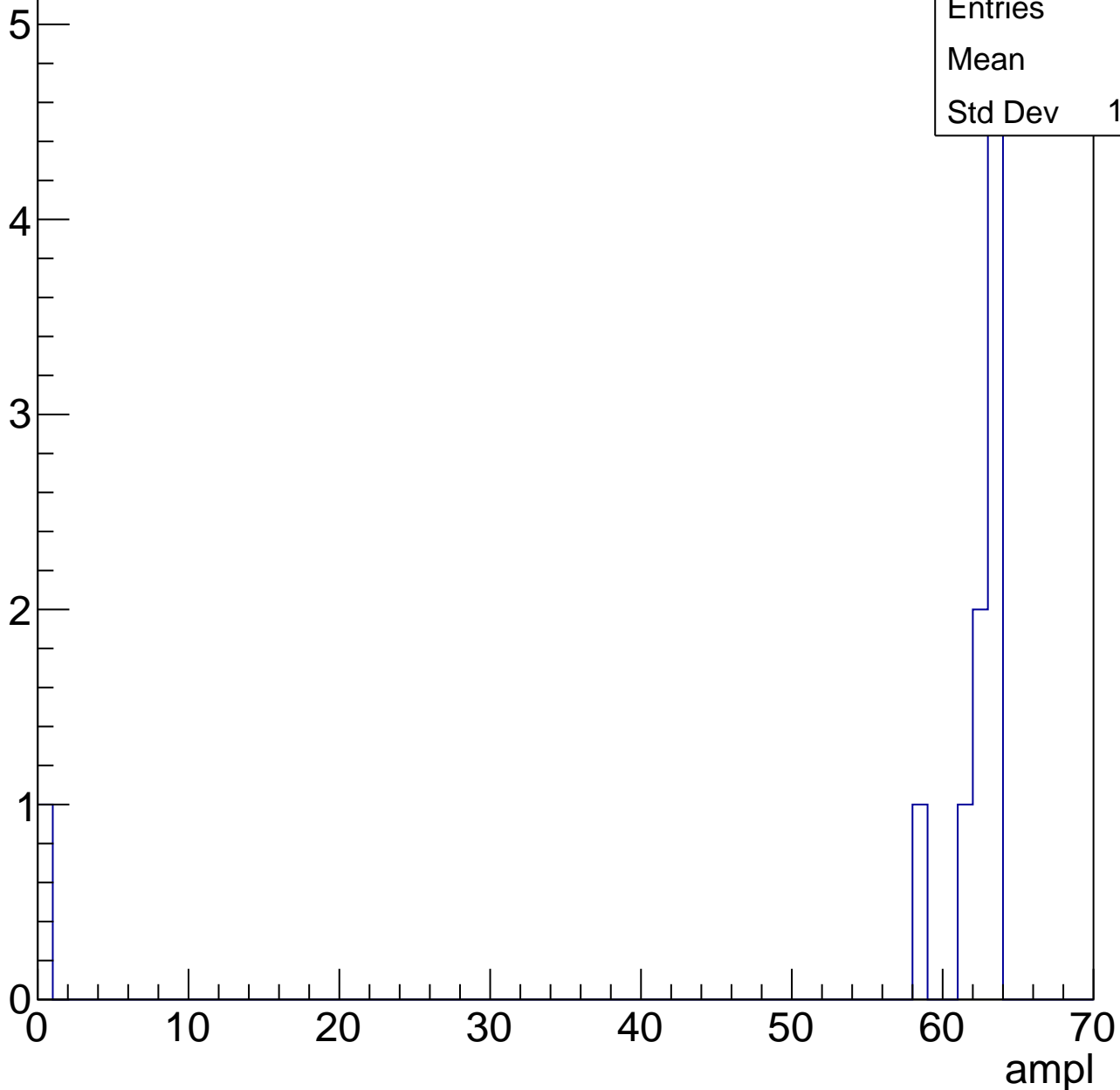
Entries	47
Mean	59.7
Std Dev	2.405

# B1L101S, U20-ch62, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	10
Mean	55.8
Std Dev	18.66





# B1L101S, U20-ch62, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U20-ch63, adc0

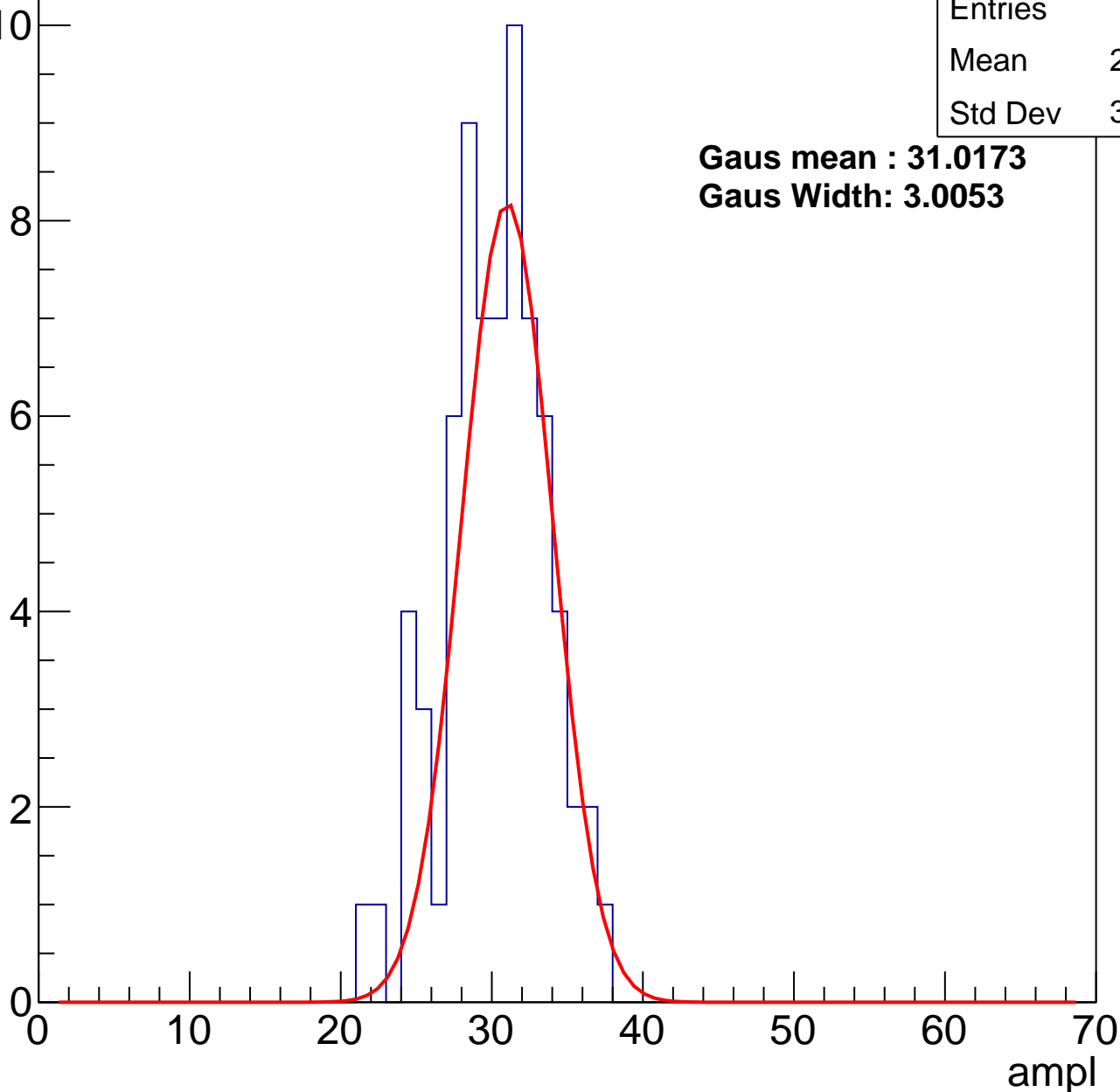
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	71
Mean	29.77
Std Dev	3.358

**Gaus mean : 31.0173**

**Gaus Width: 3.0053**



# B1L101S, U20-ch63, adc1

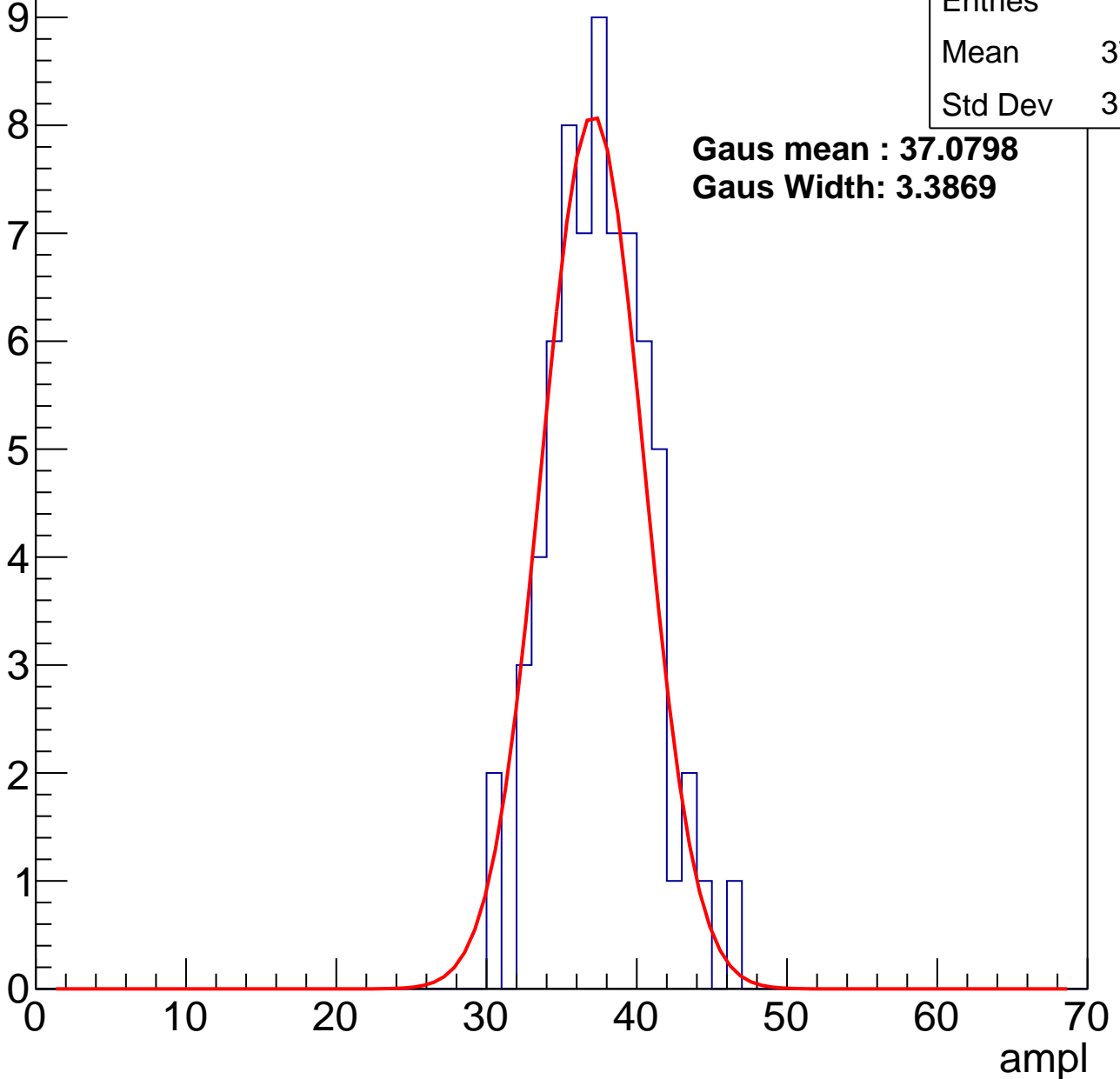
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	37.09
Std Dev	3.243

**Gaus mean : 37.0798**

**Gaus Width: 3.3869**



# B1L101S, U20-ch63, adc2

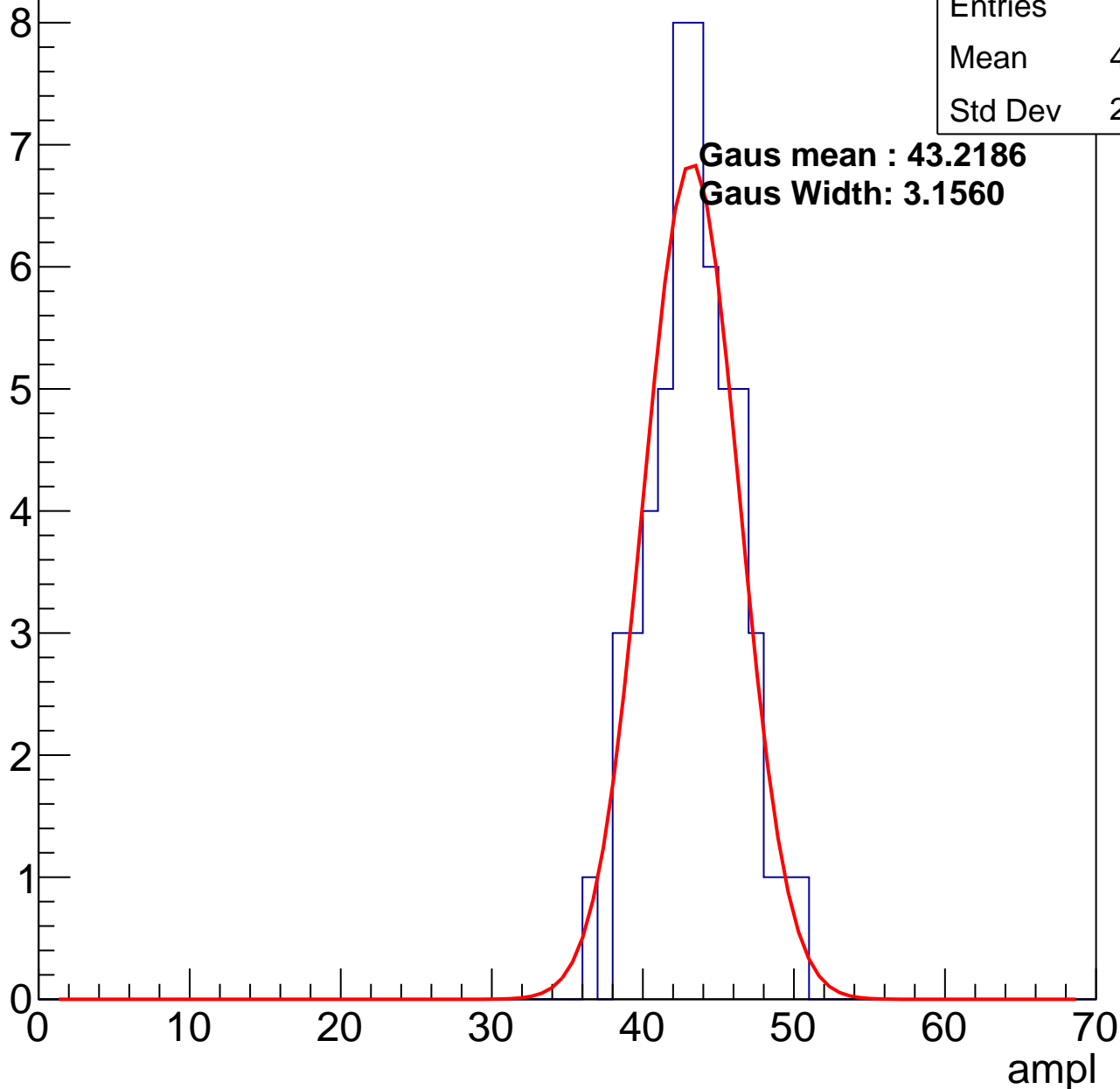
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	54
Mean	42.94
Std Dev	2.934

**Gaus mean : 43.2186**

**Gaus Width: 3.1560**

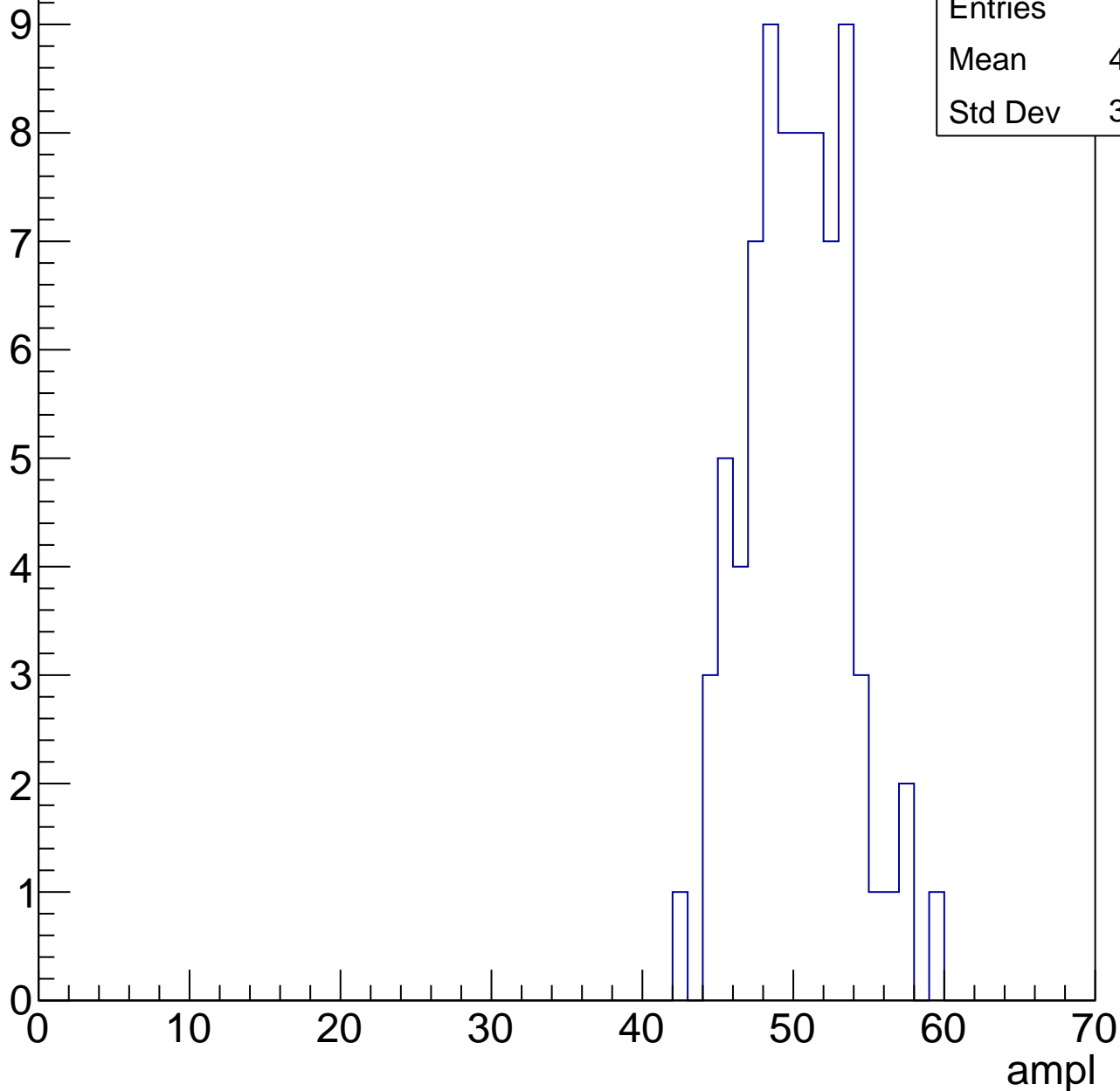


# B1L101S, U20-ch63, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	77
Mean	49.75
Std Dev	3.358

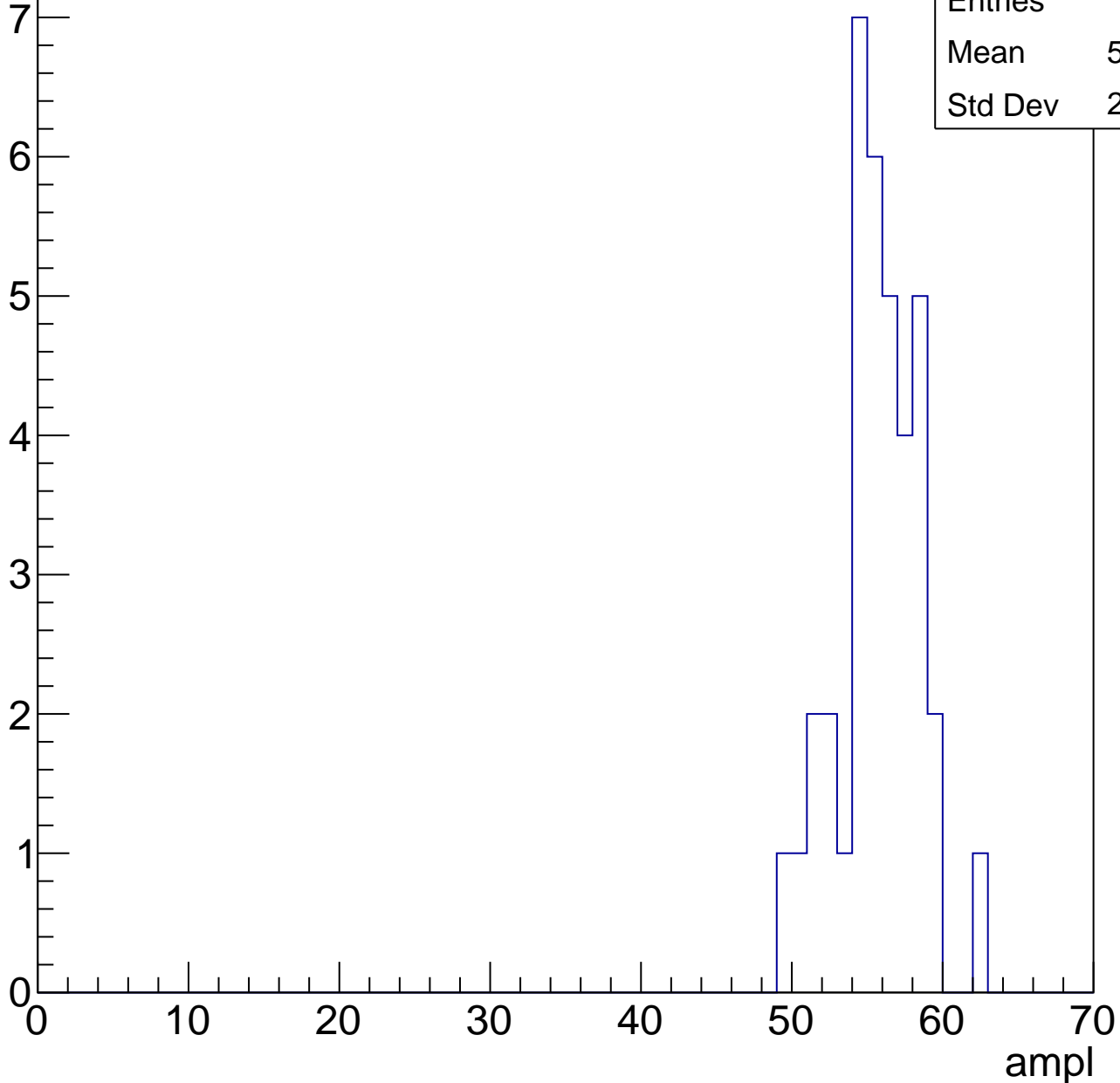


# B1L101S, U20-ch63, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	37
Mean	55.24
Std Dev	2.685

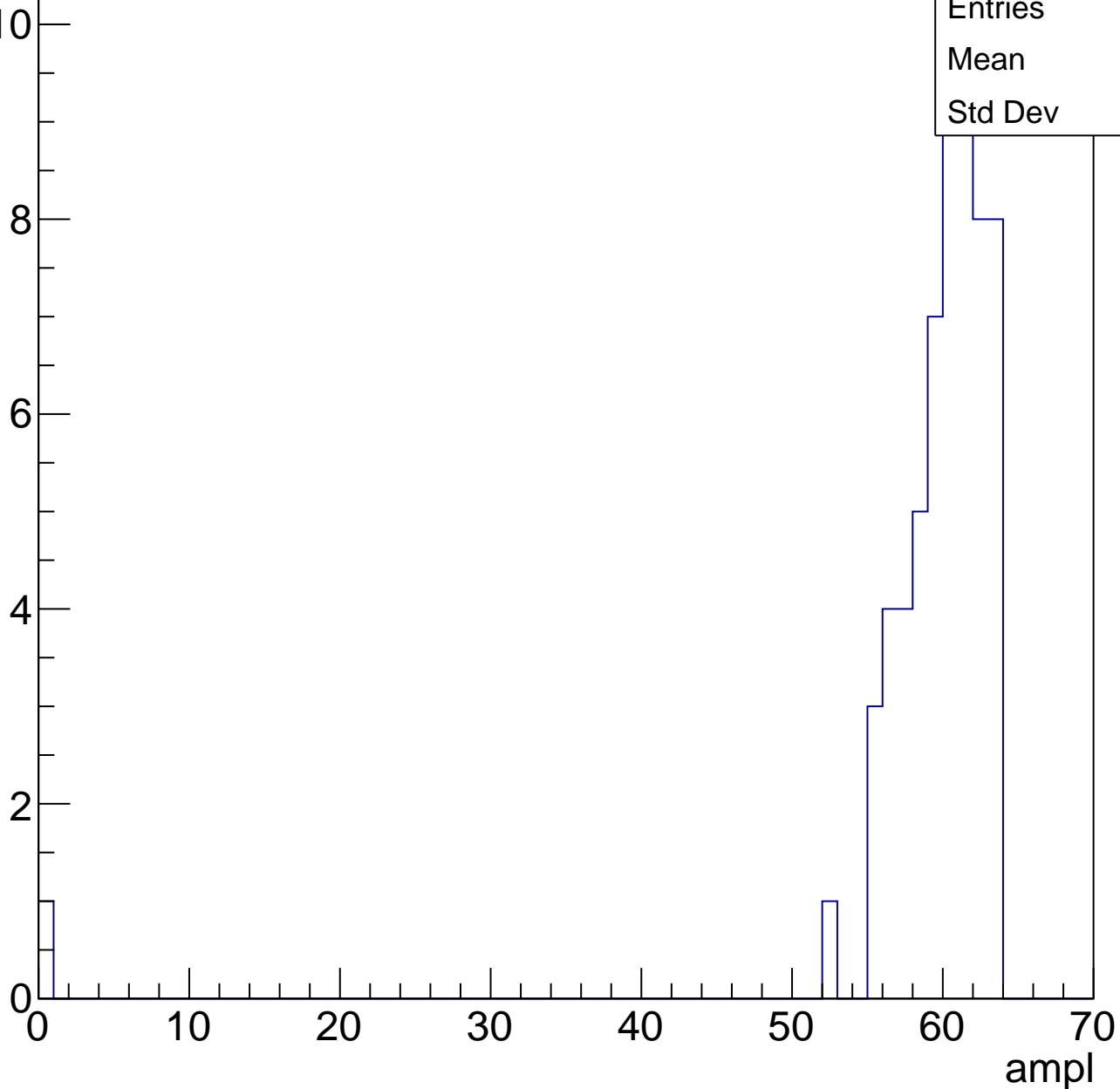


# B1L101S, U20-ch63, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	60
Mean	58.7
Std Dev	8.04



# B1L101S, U20-ch63, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U20-ch63, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L101S, U20-ch64, adc0

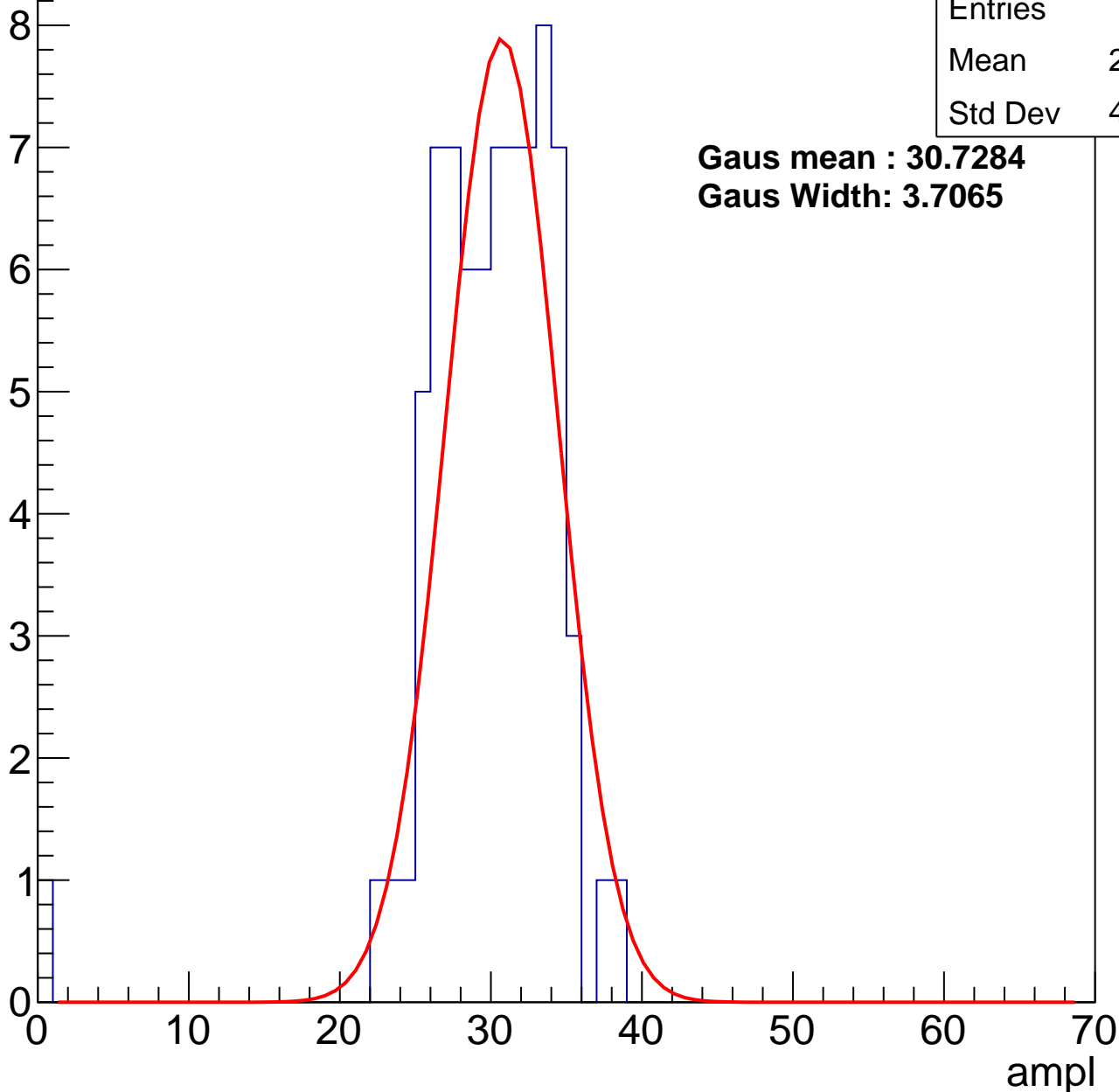
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	76
Mean	29.47
Std Dev	4.819

**Gaus mean : 30.7284**

**Gaus Width: 3.7065**



# B1L101S, U20-ch64, adc1

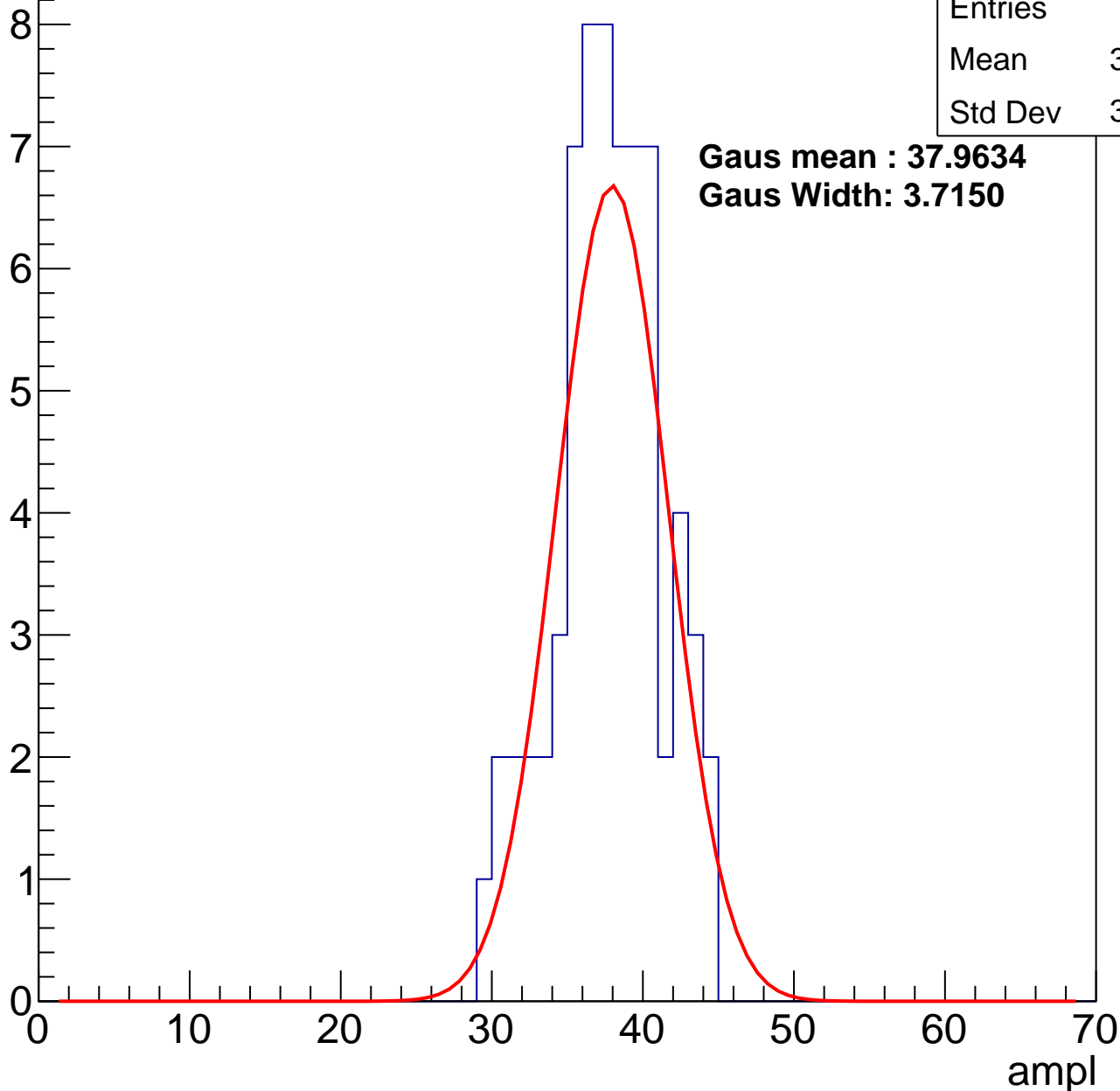
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	67
Mean	37.28
Std Dev	3.476

**Gaus mean : 37.9634**

**Gaus Width: 3.7150**



# B1L101S, U20-ch64, adc2

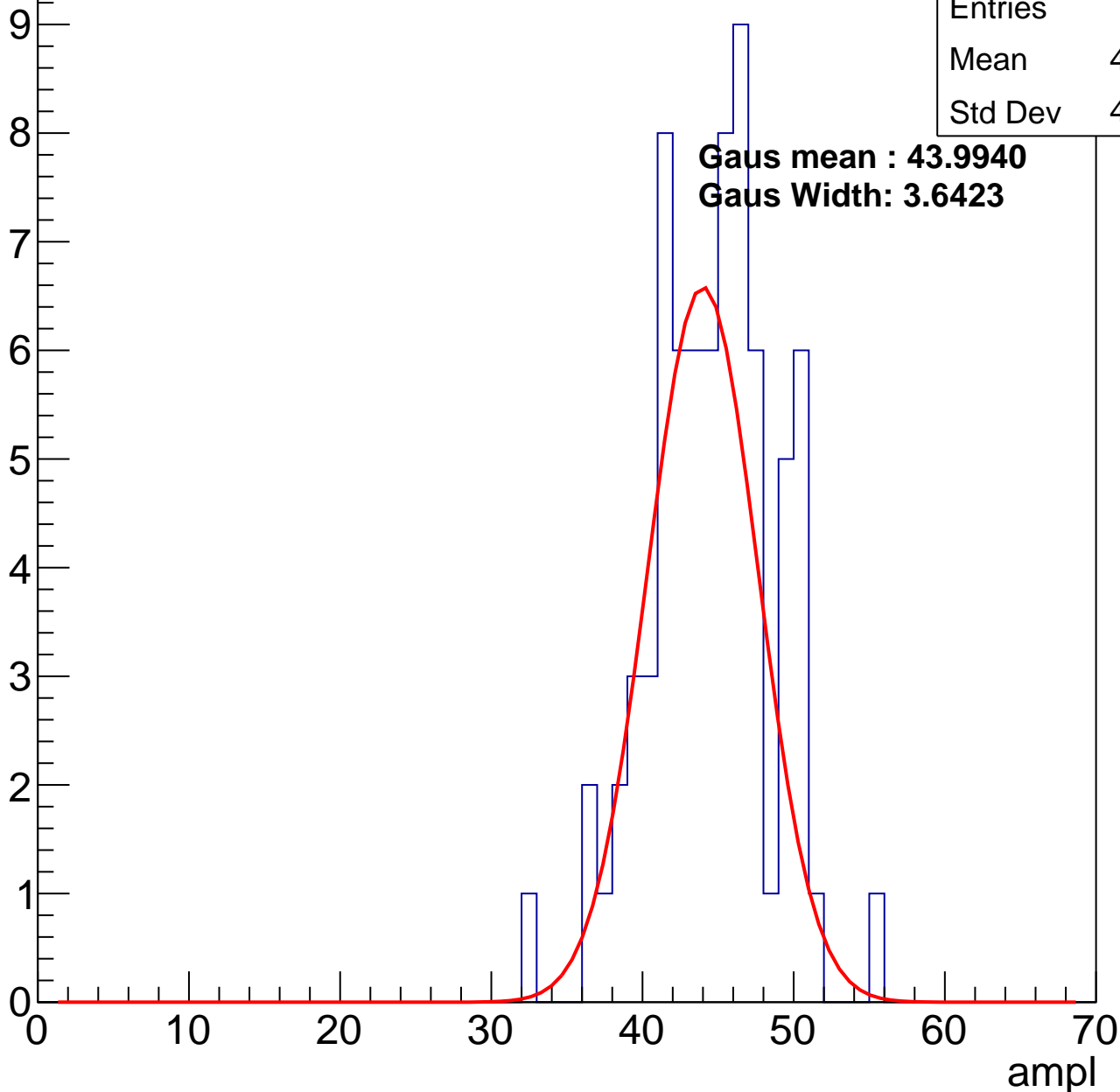
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	75
Mean	44.15
Std Dev	4.068

**Gaus mean : 43.9940**

**Gaus Width: 3.6423**

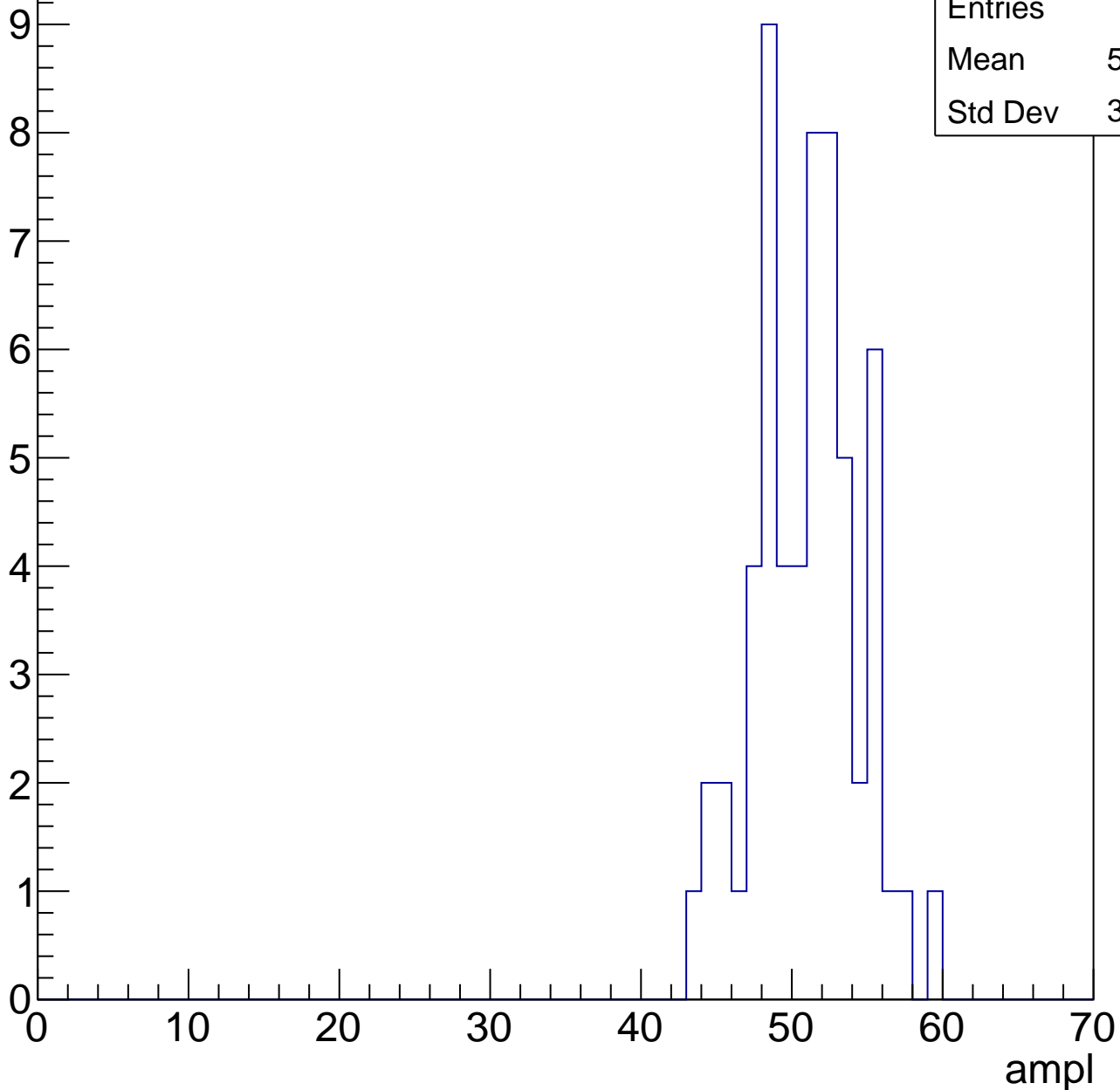


# B1L101S, U20-ch64, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	59
Mean	50.54
Std Dev	3.392

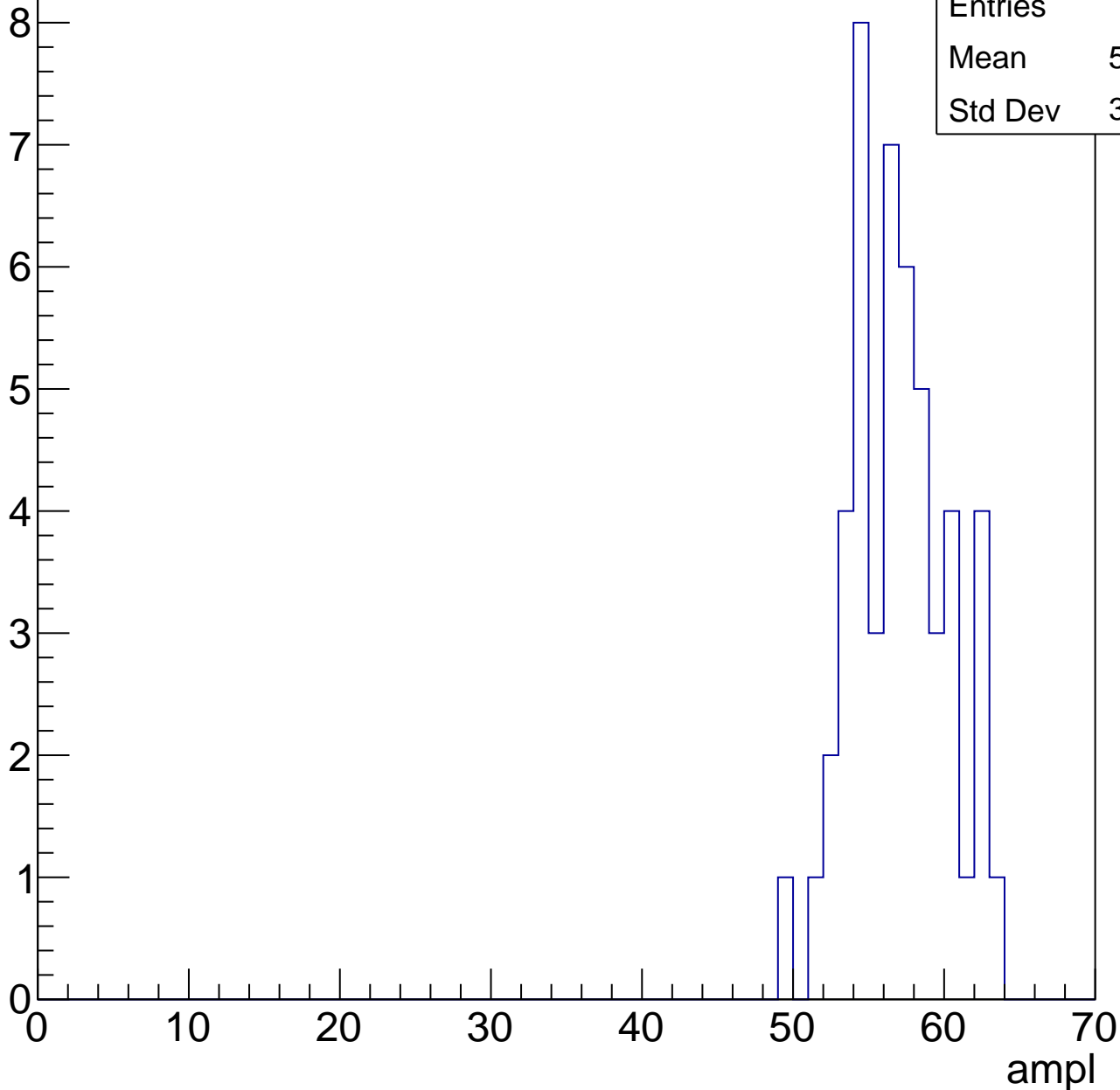


# B1L101S, U20-ch64, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	50
Mean	56.52
Std Dev	3.157

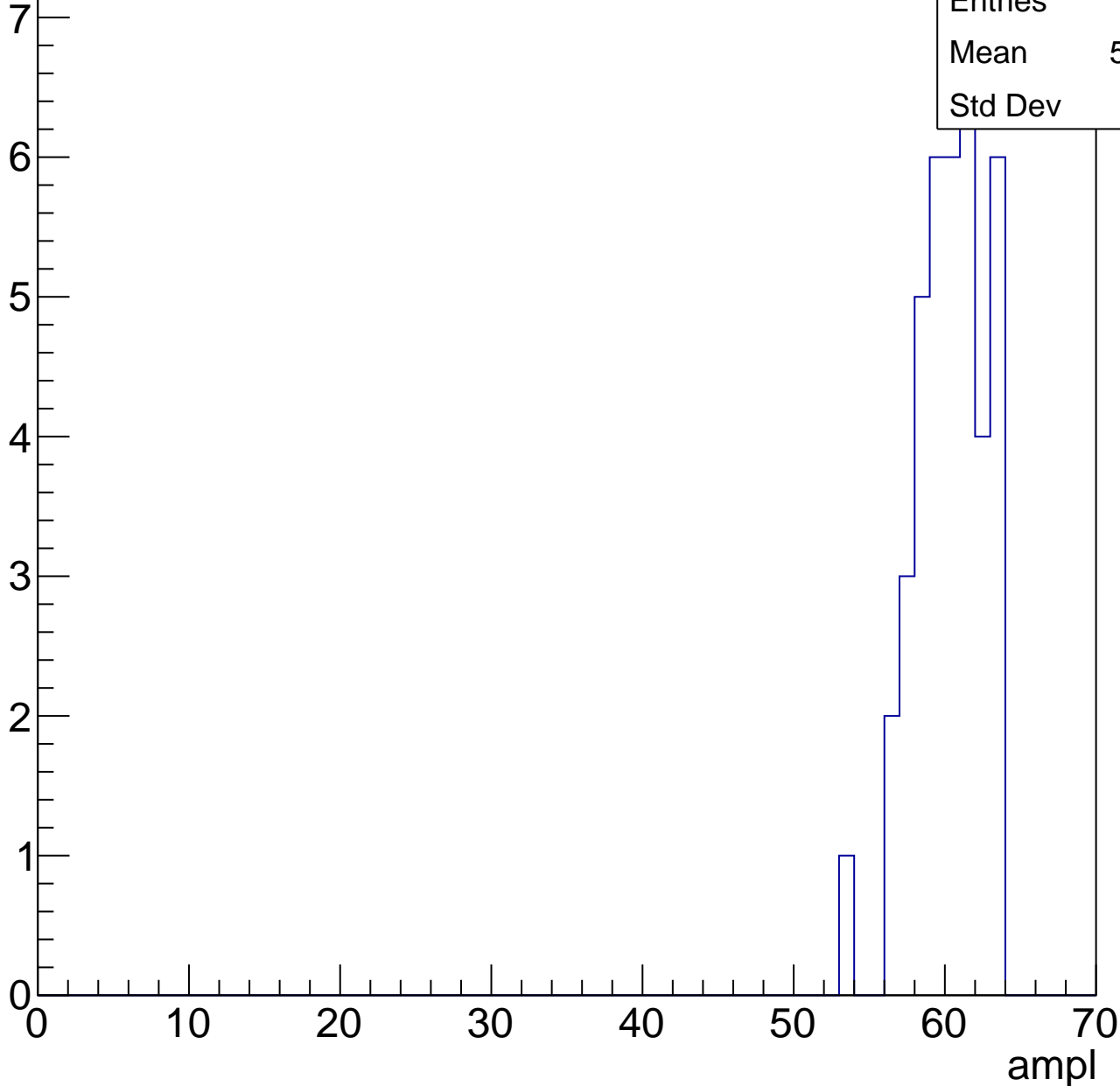


# B1L101S, U20-ch64, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

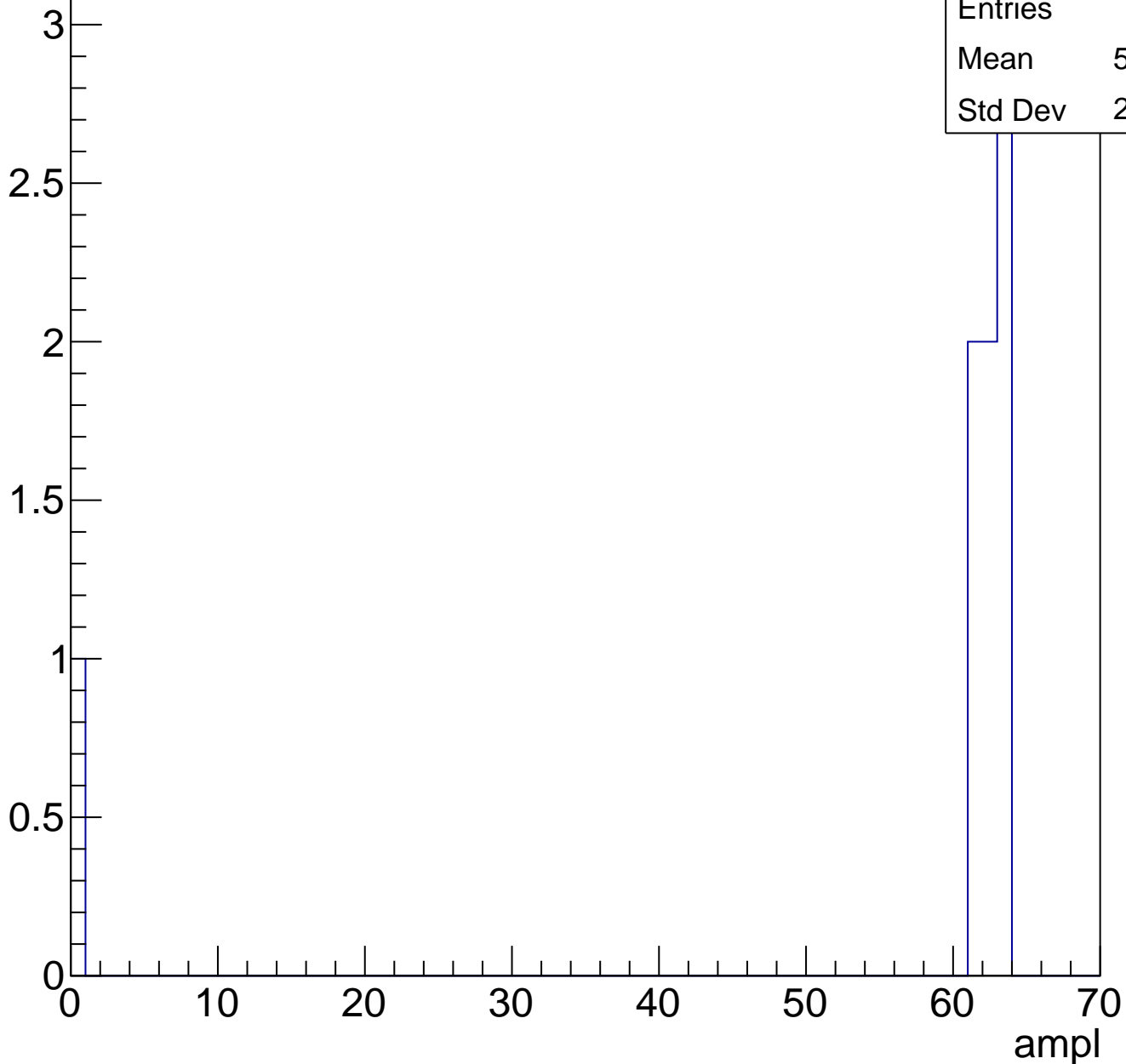
Entries	40
Mean	59.83
Std Dev	2.29



# B1L101S, U20-ch64, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U20-ch64, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U20-ch65, adc0

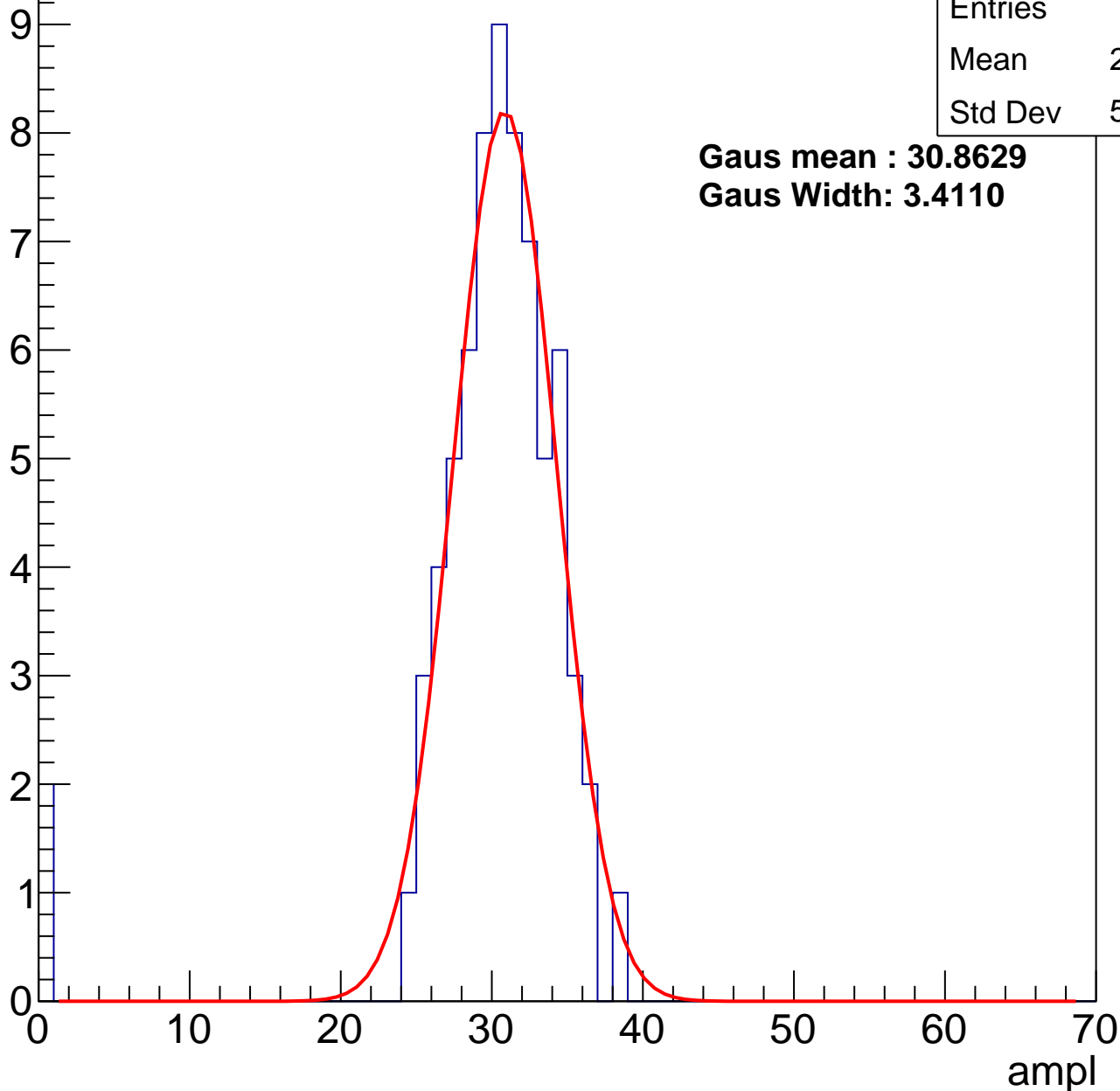
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	29.49
Std Dev	5.882

**Gaus mean : 30.8629**

**Gaus Width: 3.4110**



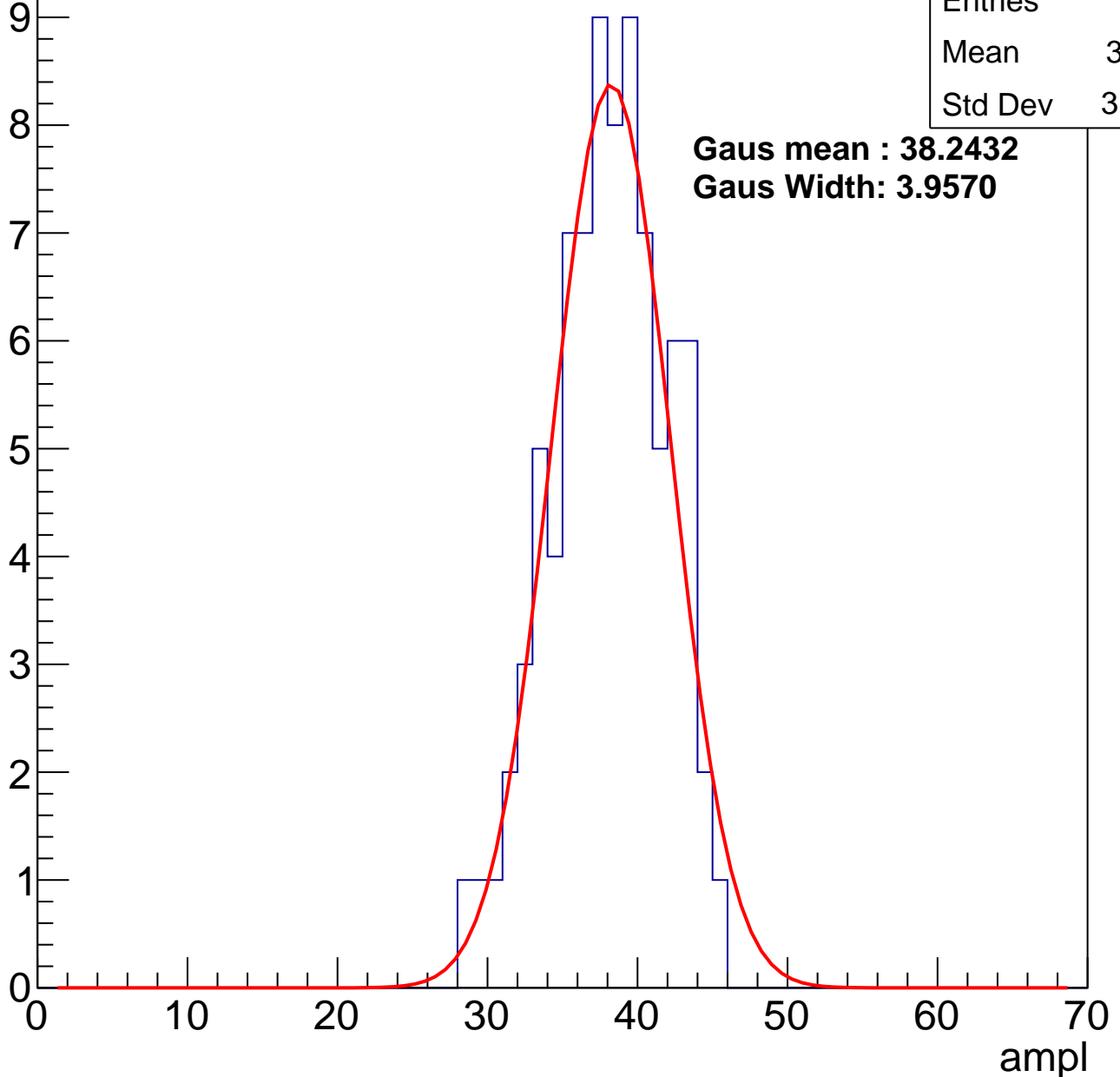
# B1L101S, U20-ch65, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	84
Mean	37.61
Std Dev	3.742

**Gaus mean : 38.2432**  
**Gaus Width: 3.9570**



# B1L101S, U20-ch65, adc2

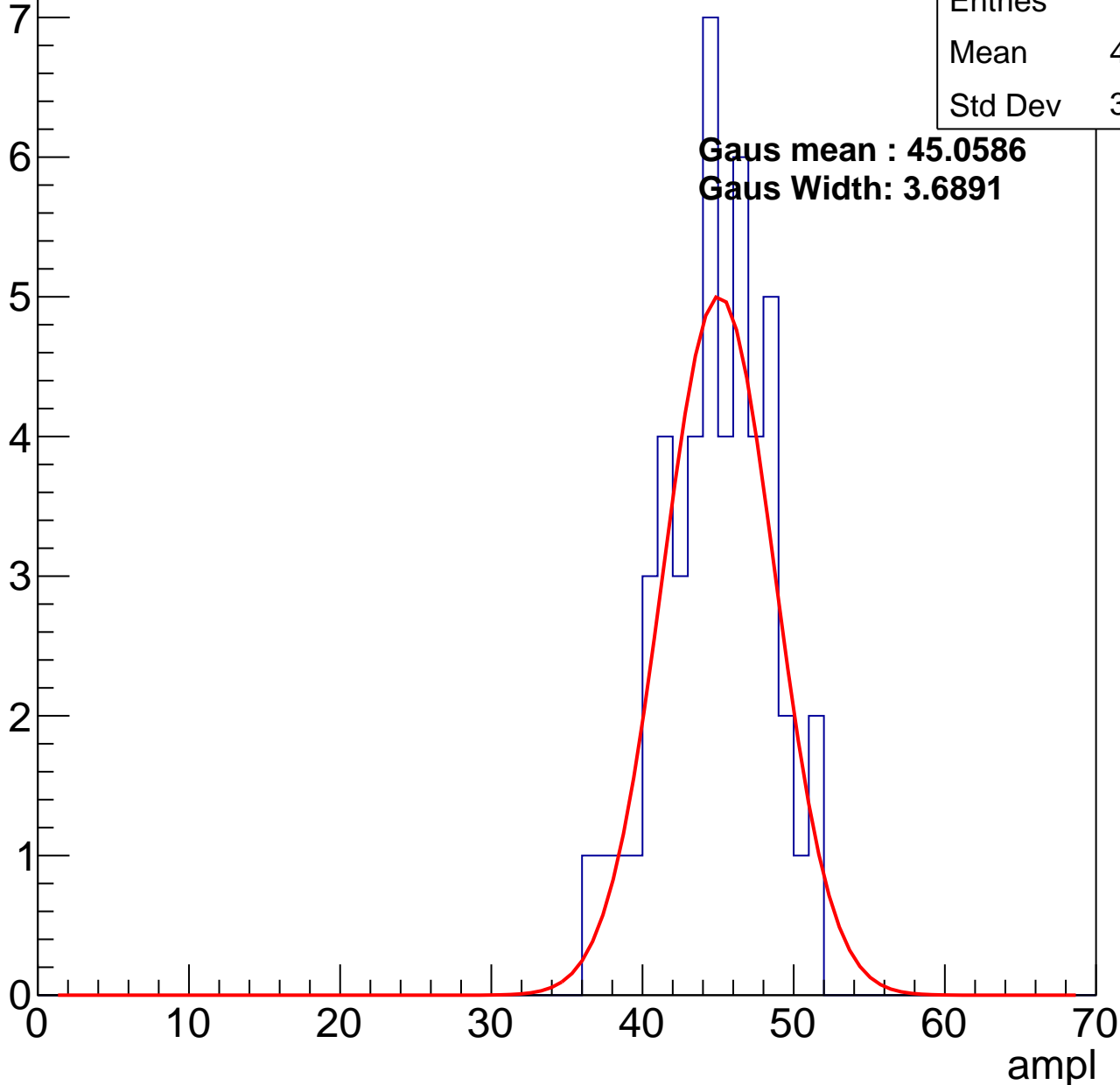
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	49
Mean	44.37
Std Dev	3.486

**Gaus mean : 45.0586**

**Gaus Width: 3.6891**

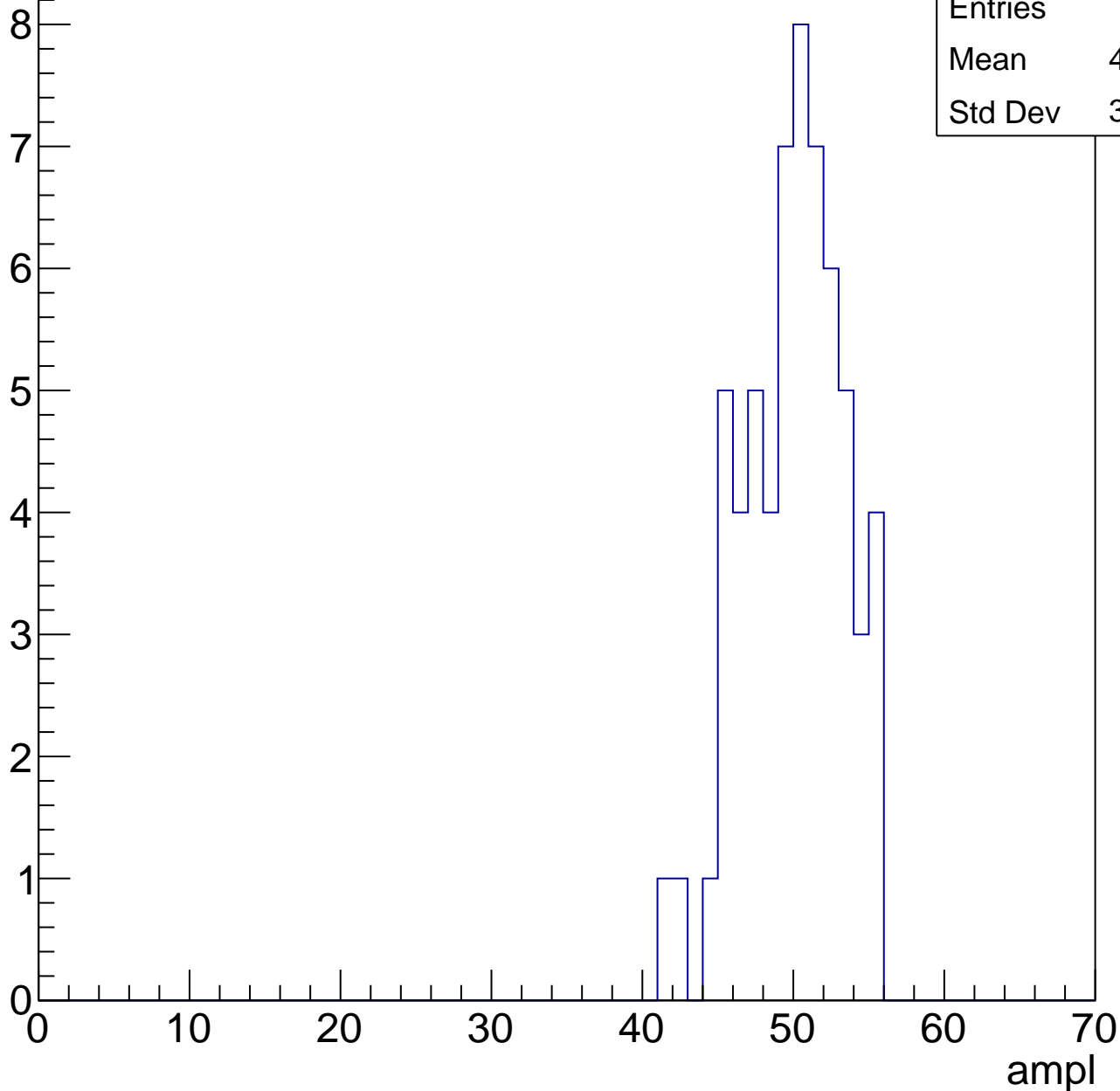


# B1L101S, U20-ch65, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	49.54
Std Dev	3.262



# B1L101S, U20-ch65, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	68
Mean	56.06
Std Dev	3.356

Entry

10

8

6

4

2

0

0

10

20

30

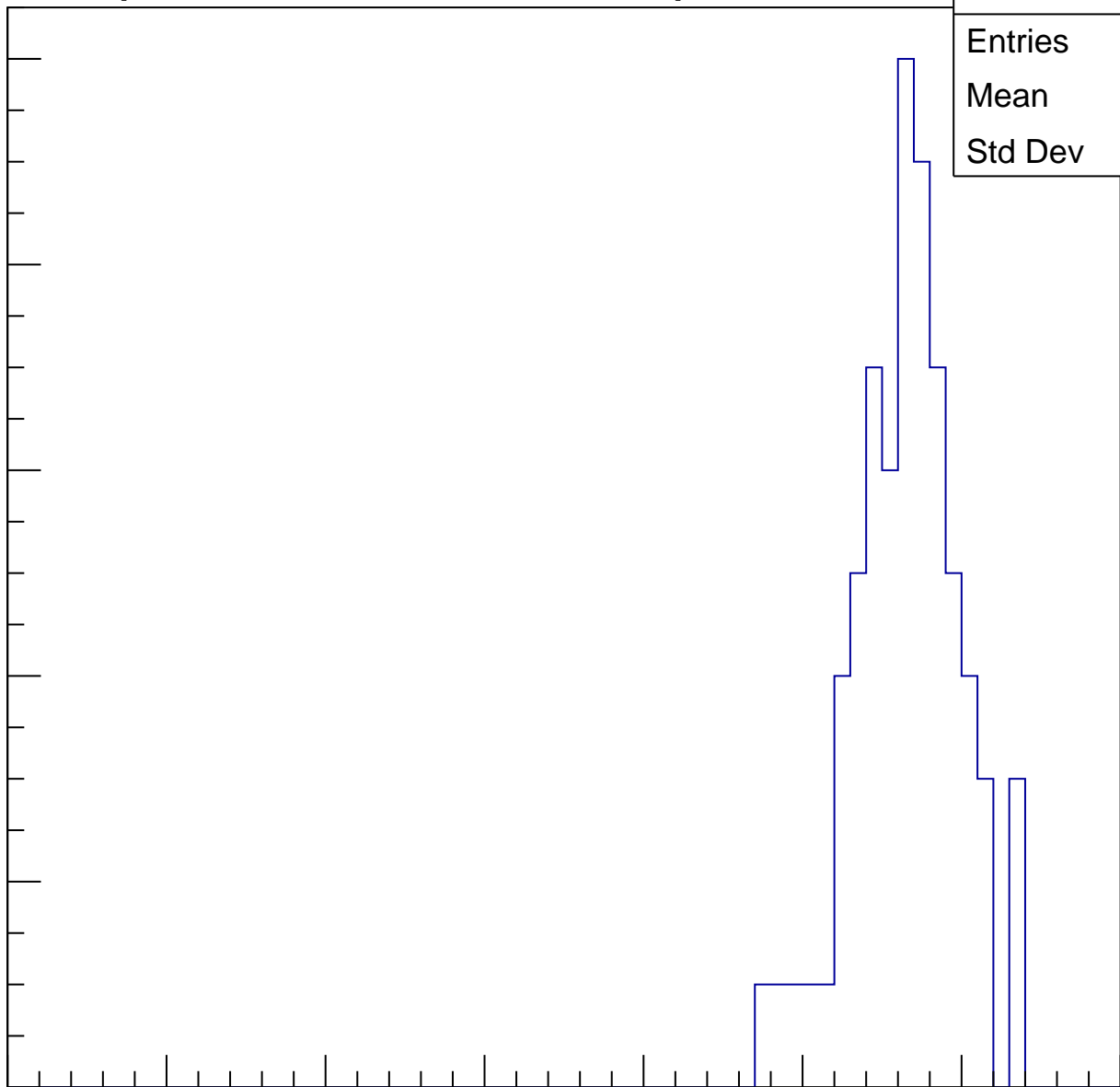
40

50

60

70

ampl

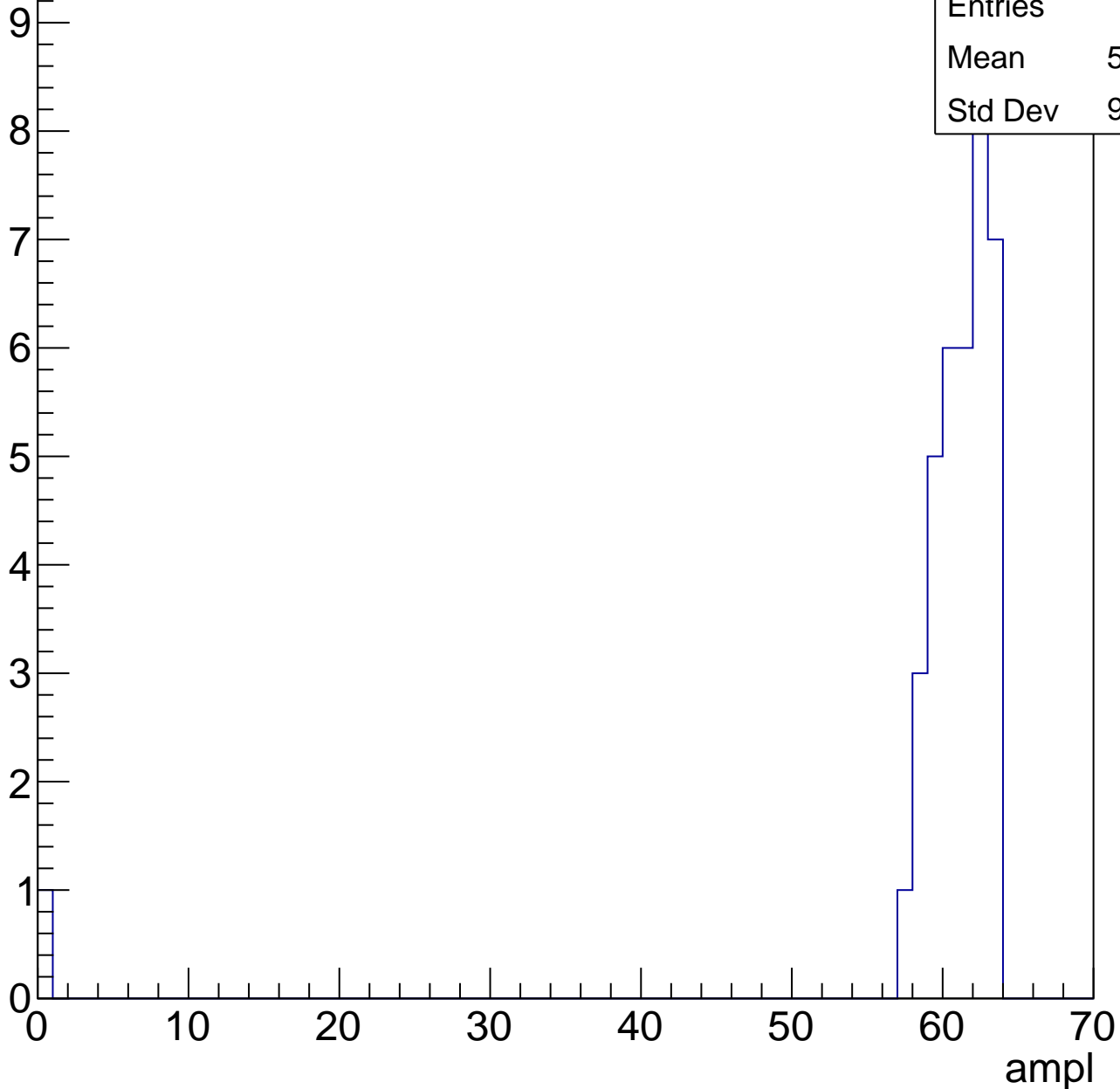


# B1L101S, U20-ch65, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	38
Mean	59.24
Std Dev	9.879



# B1L101S, U20-ch65, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U20-ch65, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U20-ch66, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	62
Mean	28.63
Std Dev	5.262

**Gaus mean : 28.8210**

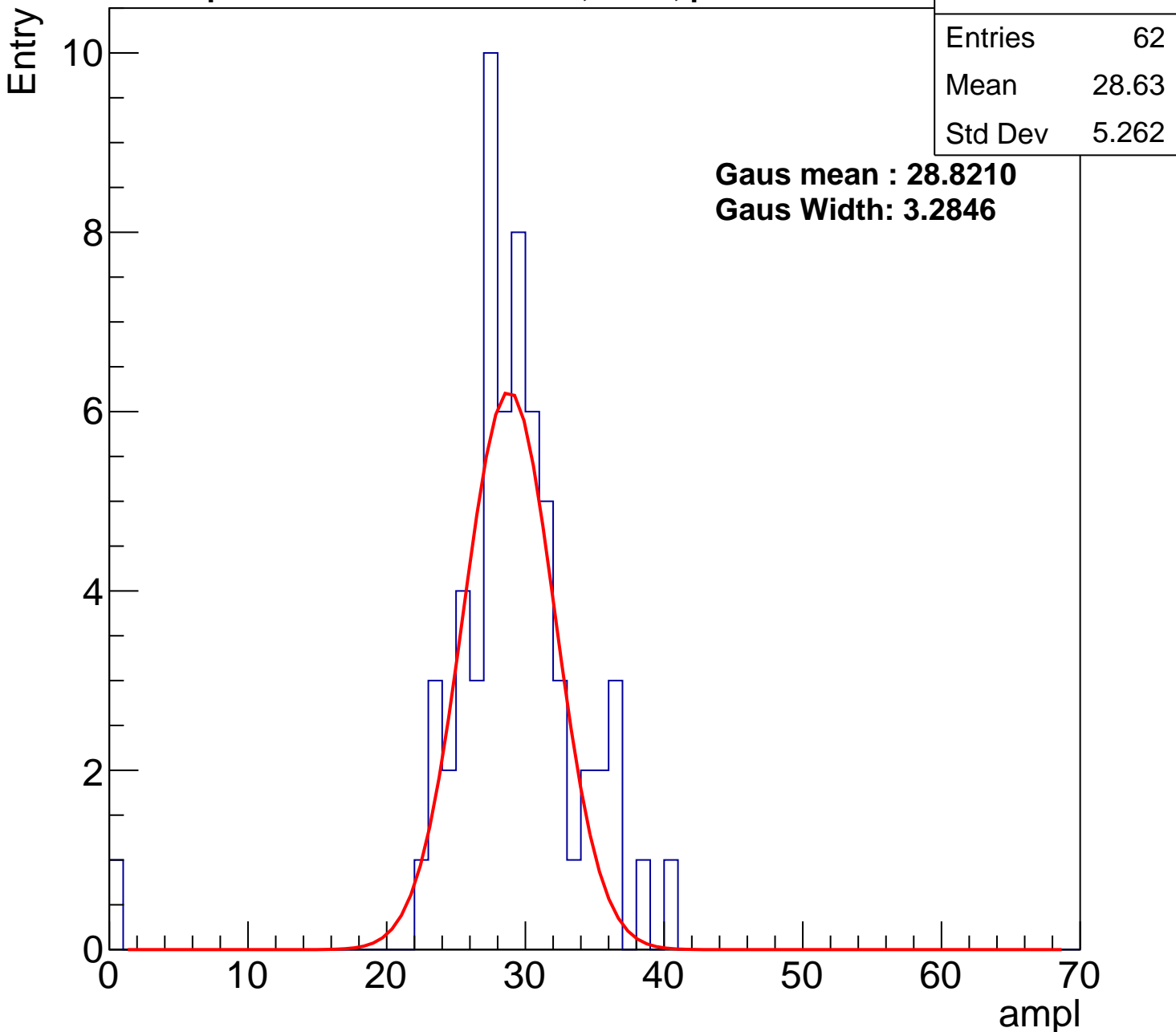
**Gaus Width: 3.2846**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U20-ch66, adc1

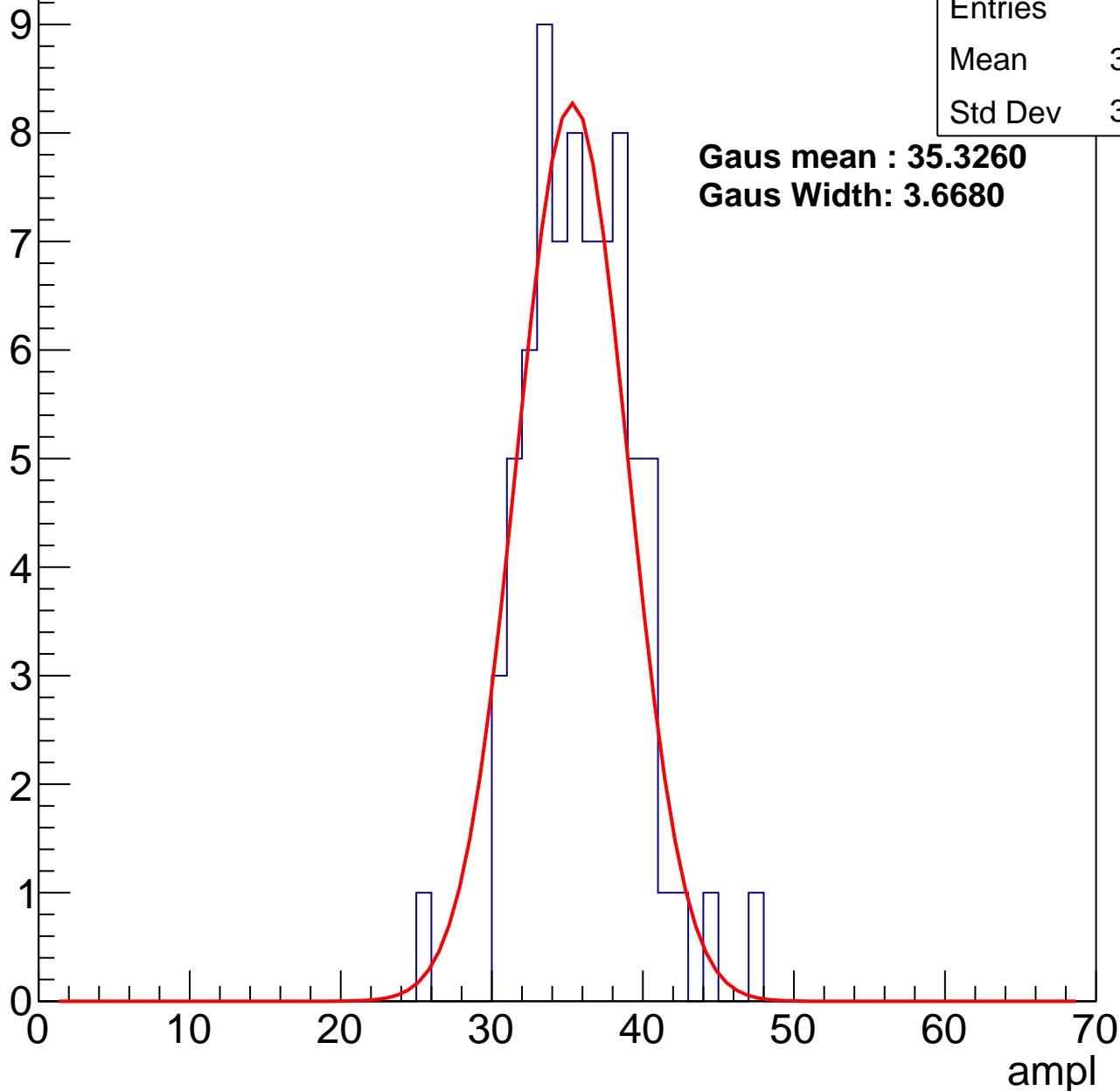
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	75
Mean	35.48
Std Dev	3.572

**Gaus mean : 35.3260**

**Gaus Width: 3.6680**



# B1L101S, U20-ch66, adc2

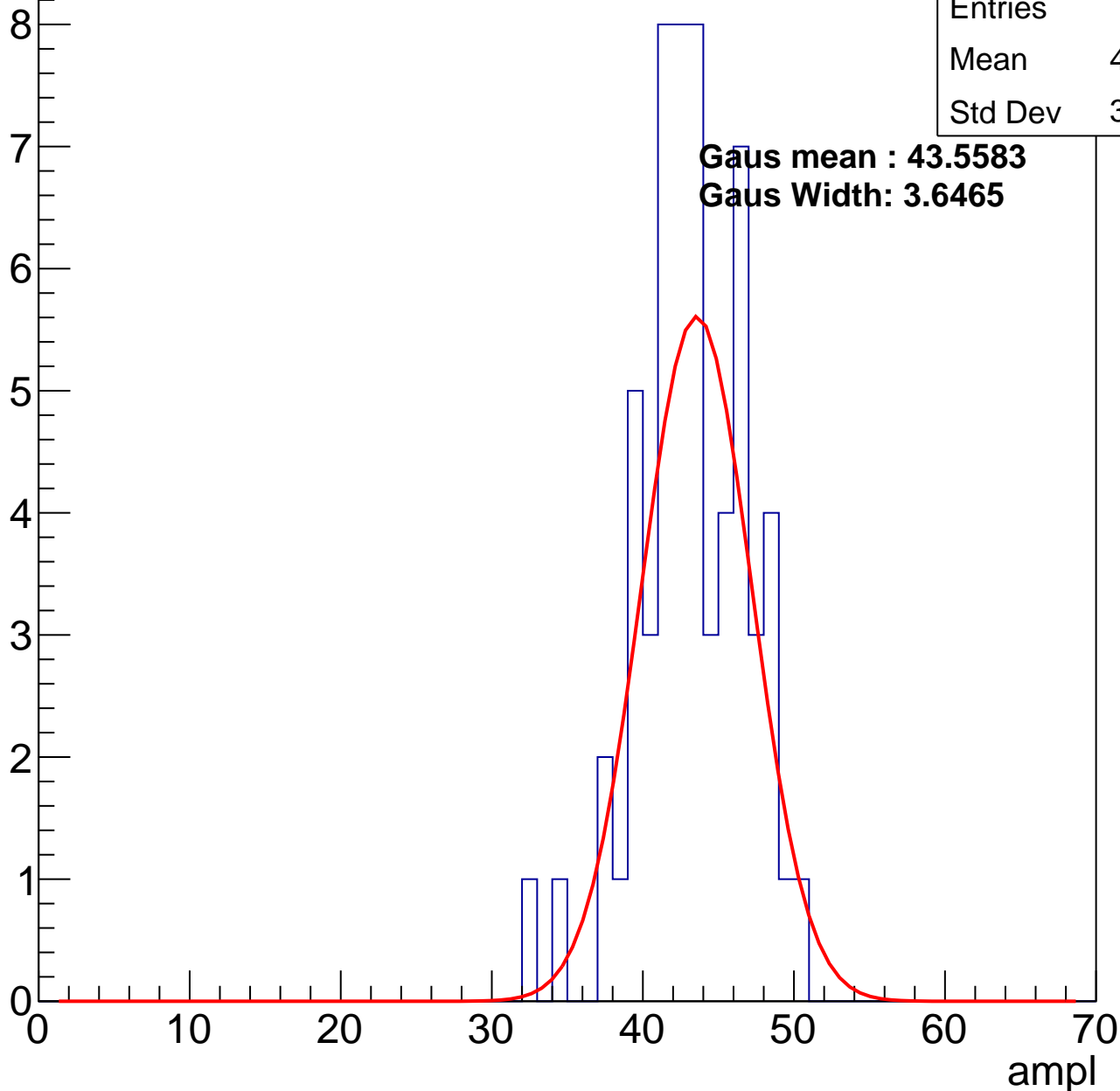
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	60
Mean	42.78
Std Dev	3.555

**Gaus mean : 43.5583**

**Gaus Width: 3.6465**

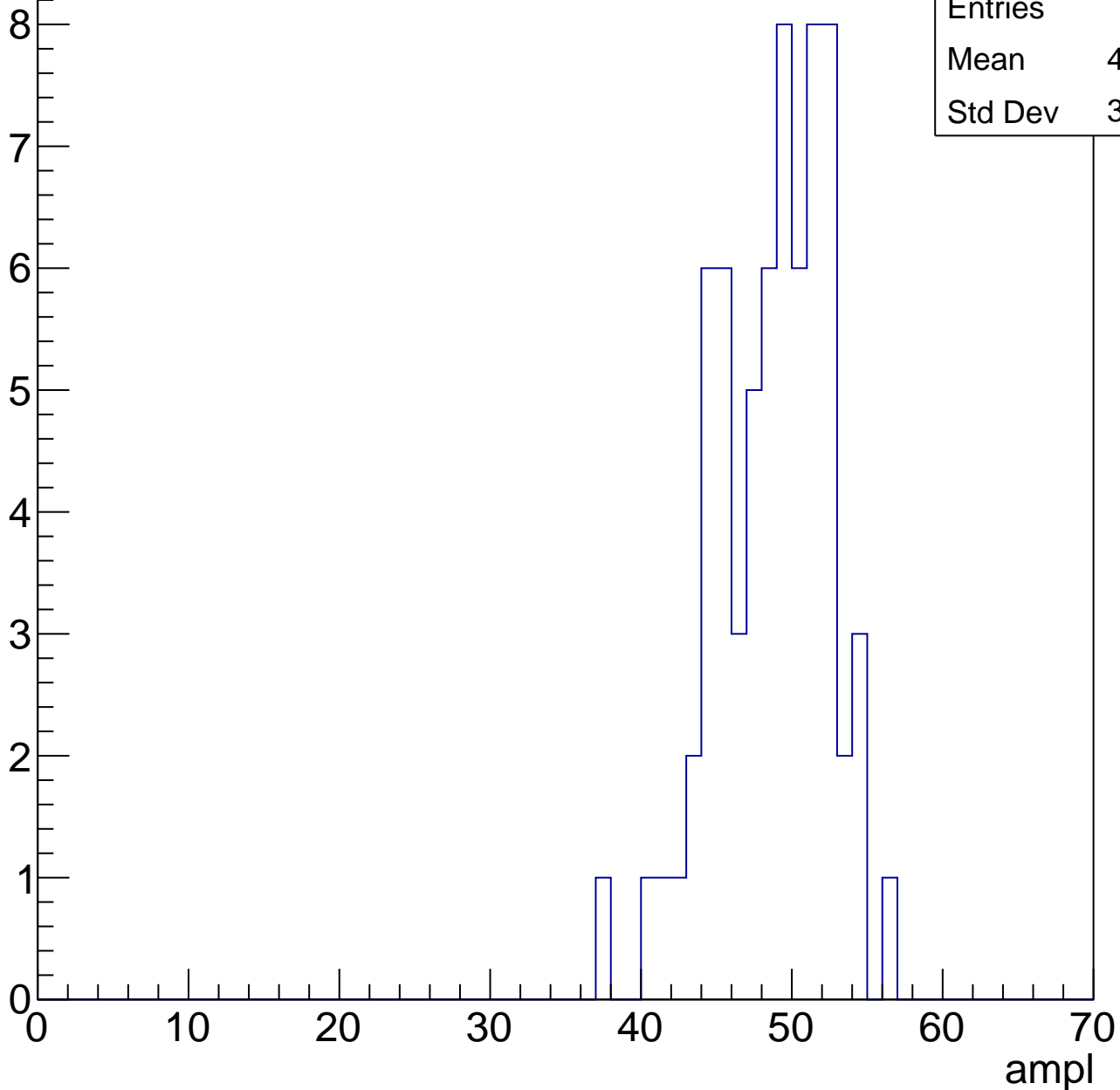


# B1L101S, U20-ch66, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	48.25
Std Dev	3.712

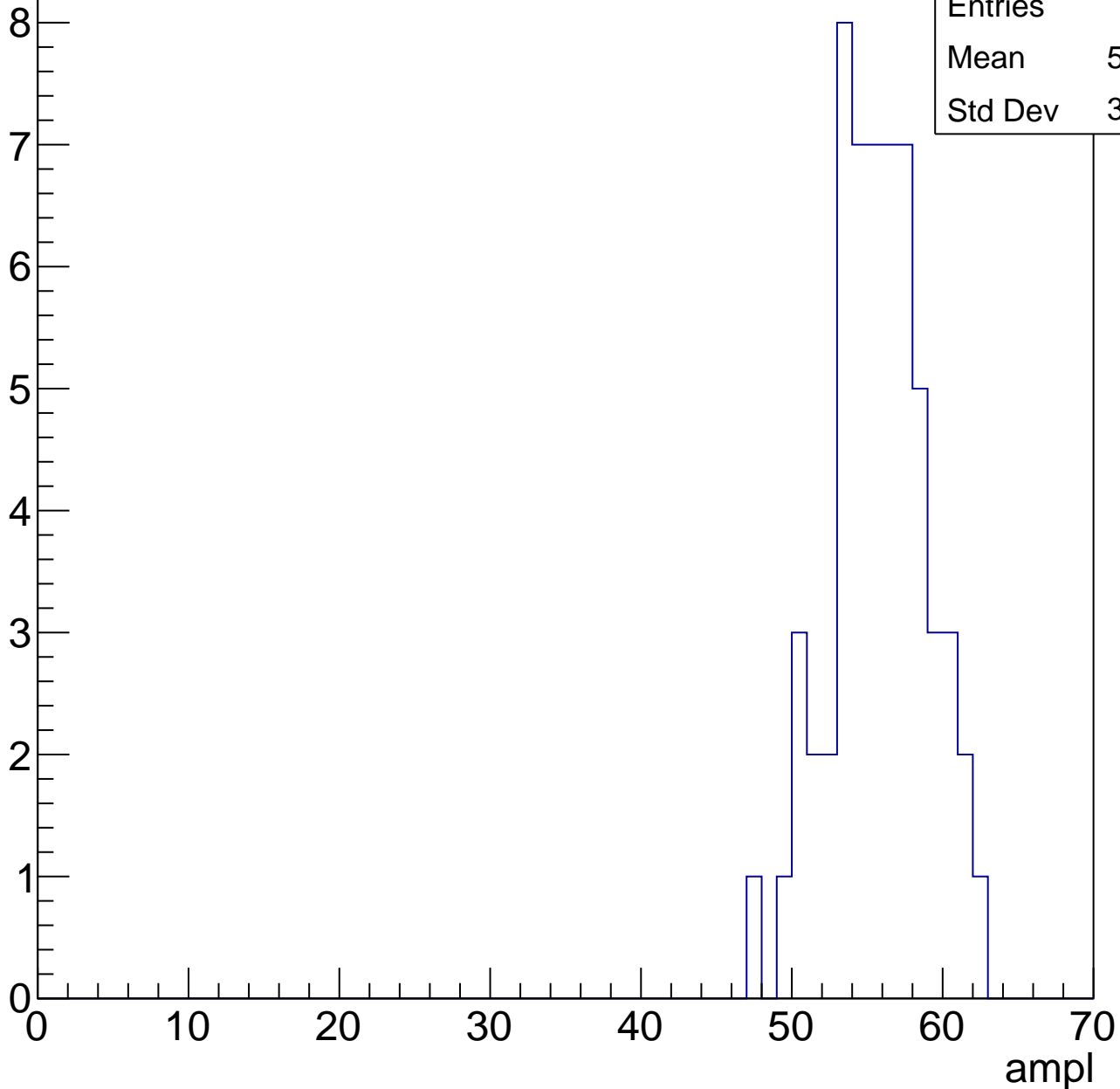


# B1L101S, U20-ch66, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	59
Mean	55.27
Std Dev	3.145



# B1L101S, U20-ch66, adc5

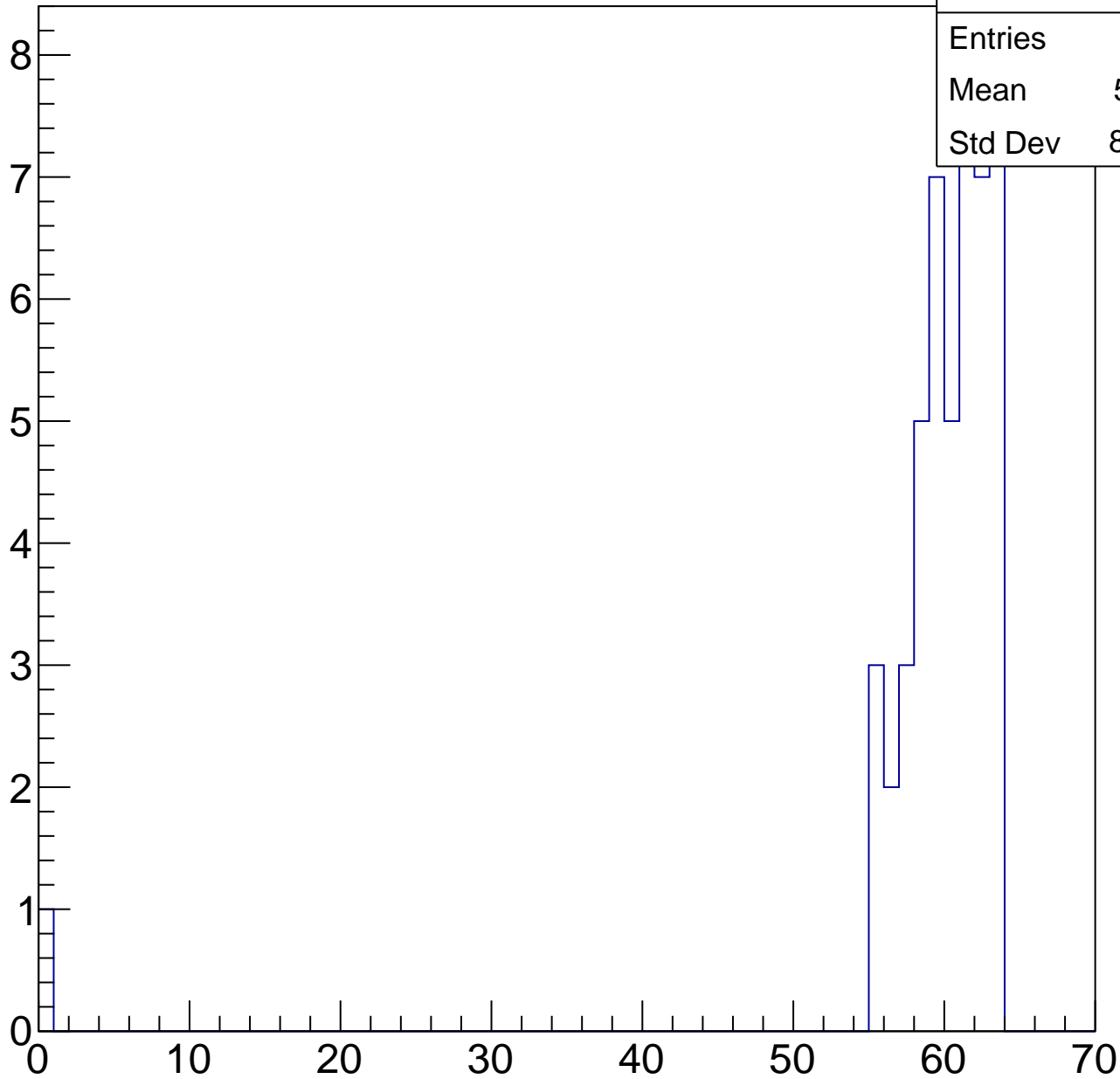
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	49
Mean	58.71
Std Dev	8.792

ampl



# B1L101S, U20-ch66, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

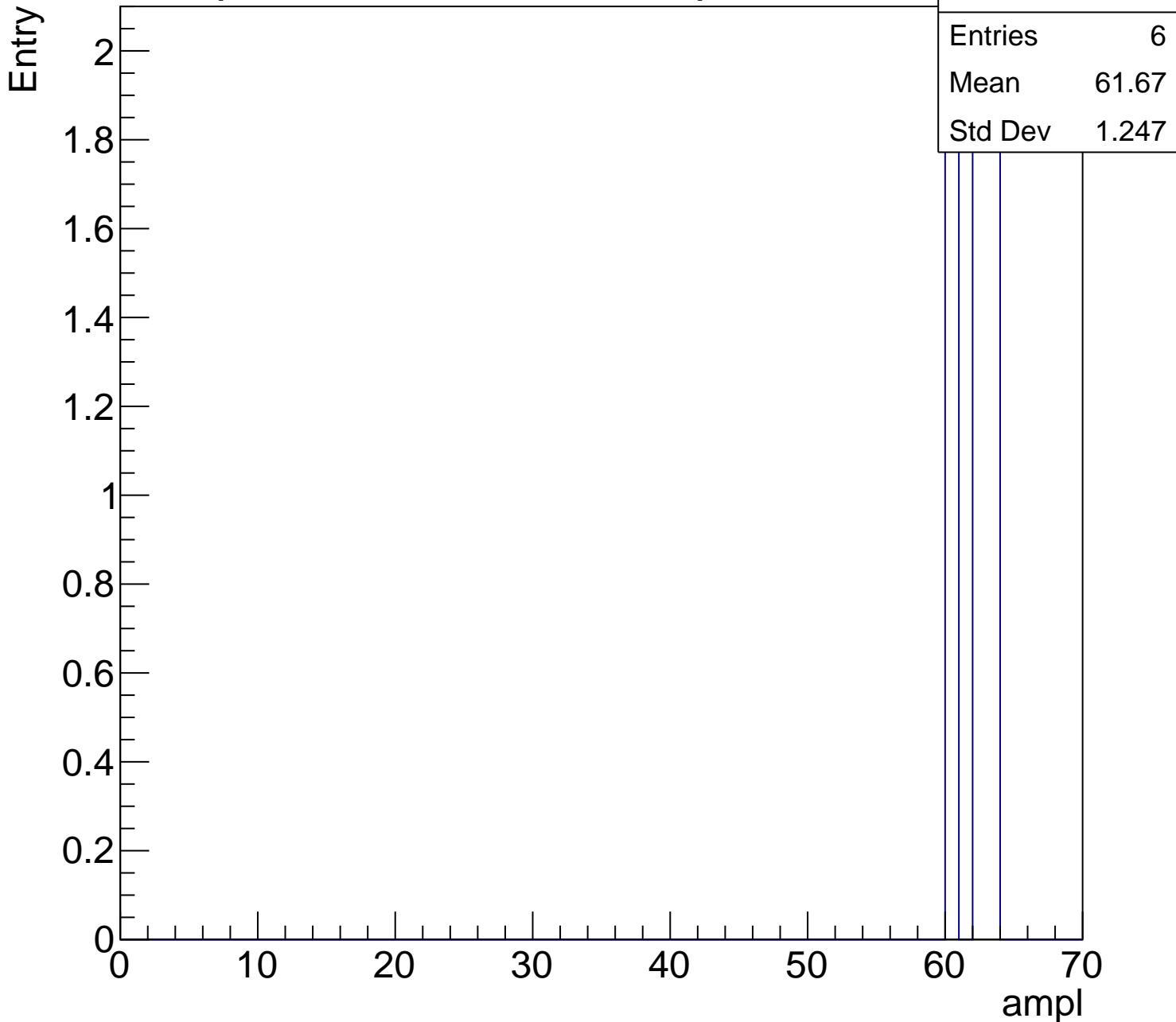
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	6
Mean	61.67
Std Dev	1.247

0 10 20 30 40 50 60 70

ampl





# B1L101S, U20-ch66, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U20-ch67, adc0

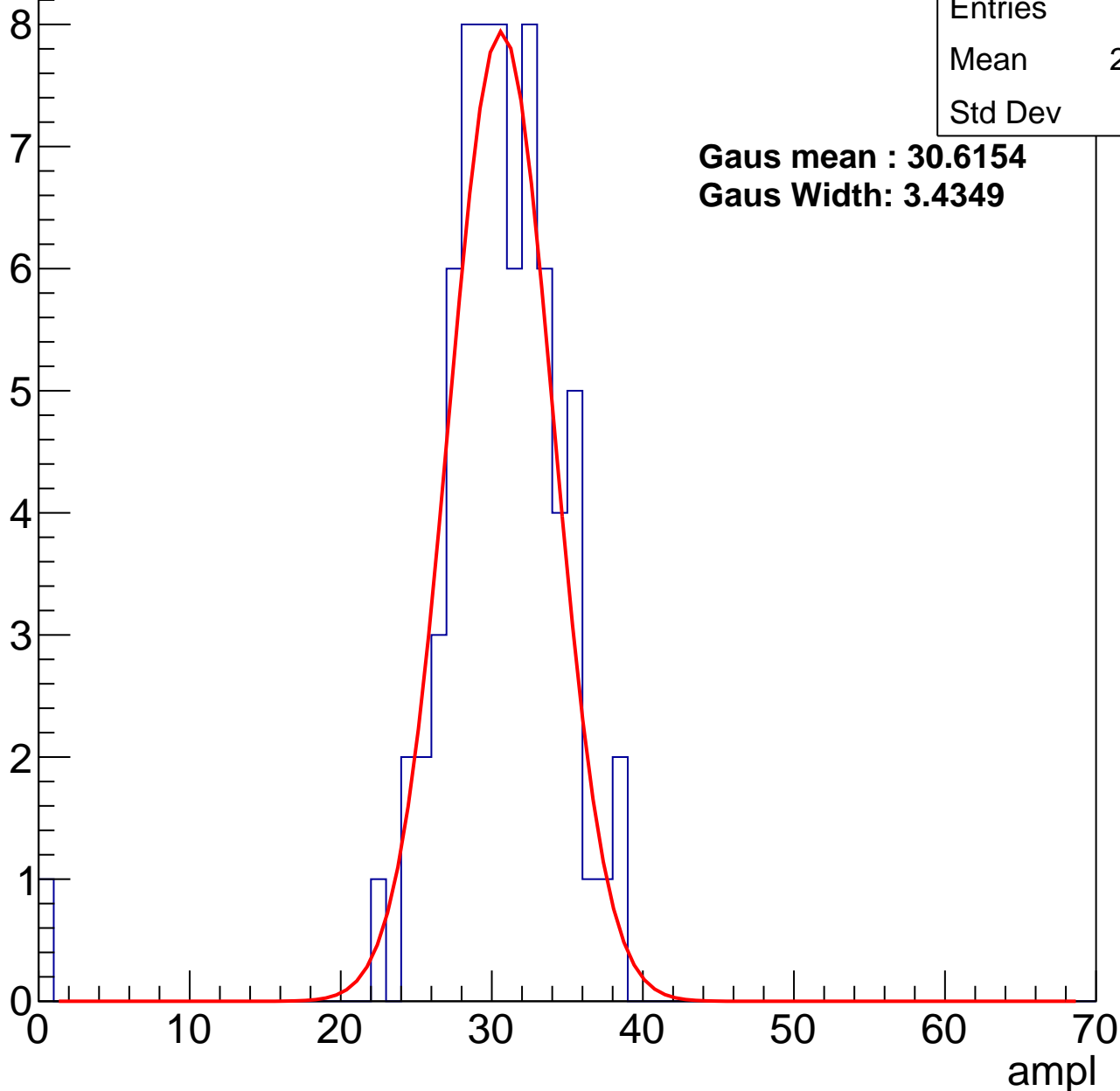
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	72
Mean	29.94
Std Dev	4.89

**Gaus mean : 30.6154**

**Gaus Width: 3.4349**



# B1L101S, U20-ch67, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	68
Mean	36.94
Std Dev	3.176

**Gaus mean : 37.4515**

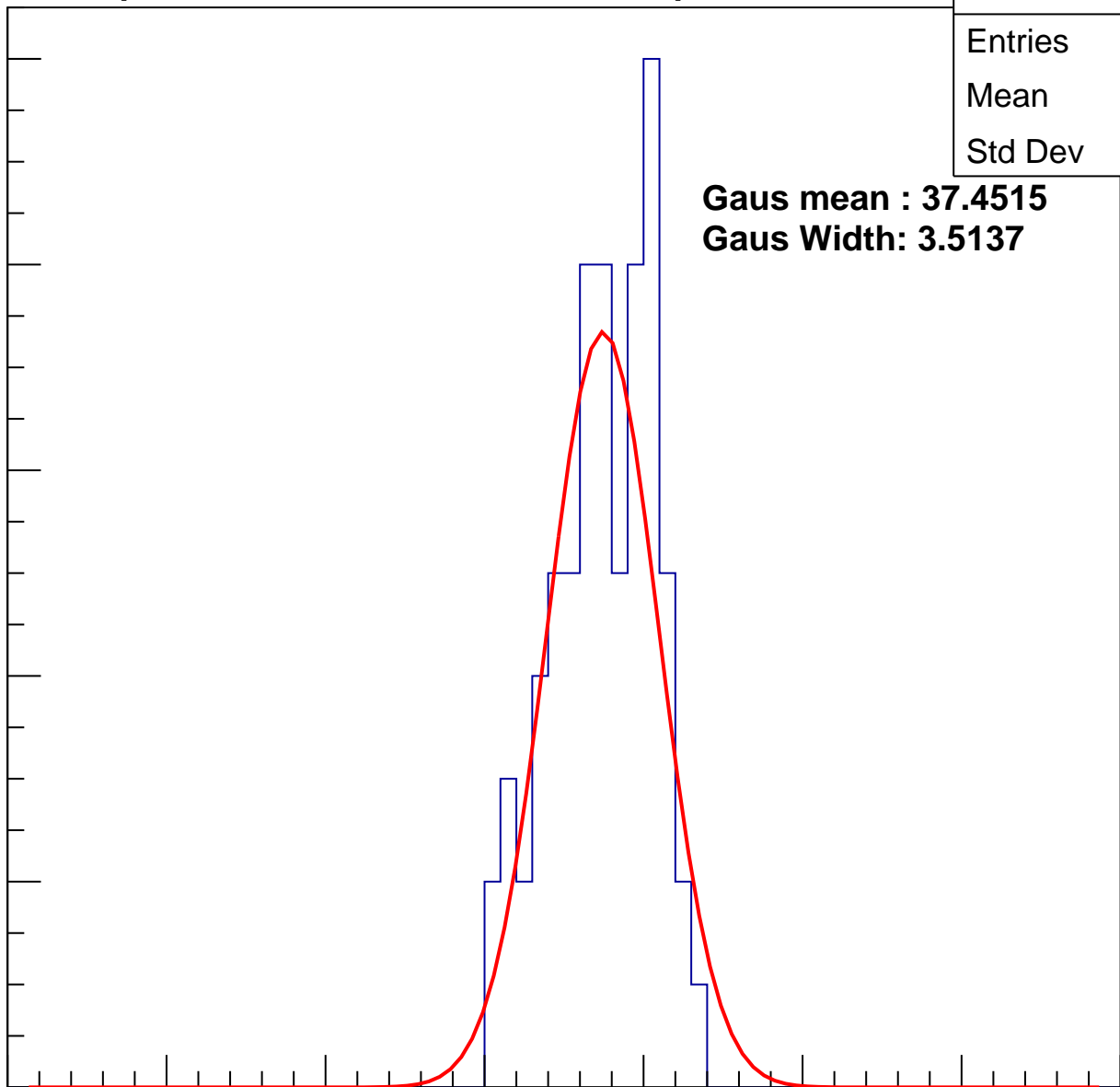
**Gaus Width: 3.5137**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B1L101S, U20-ch67, adc2

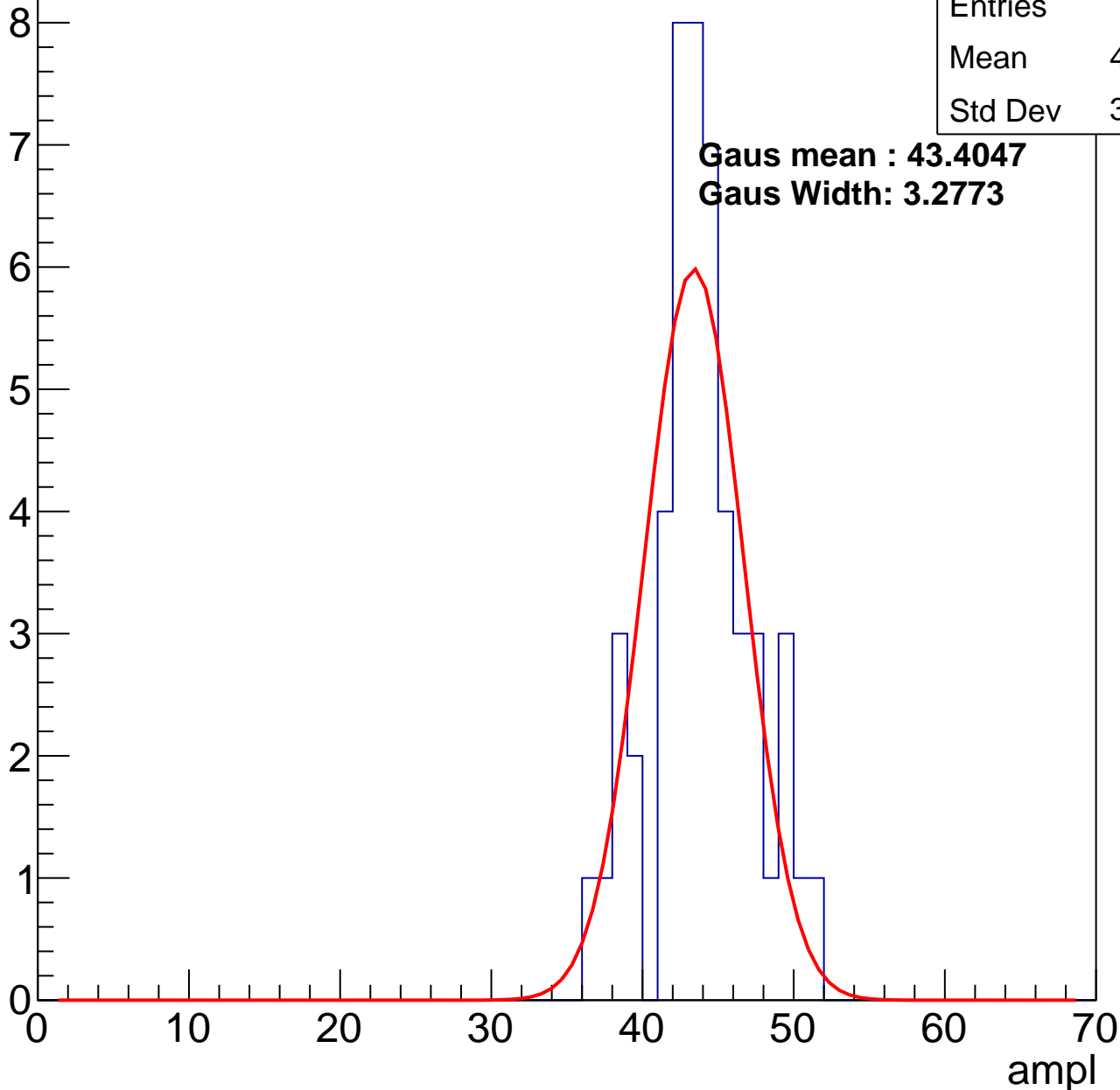
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	50
Mean	43.44
Std Dev	3.318

**Gaus mean : 43.4047**

**Gaus Width: 3.2773**

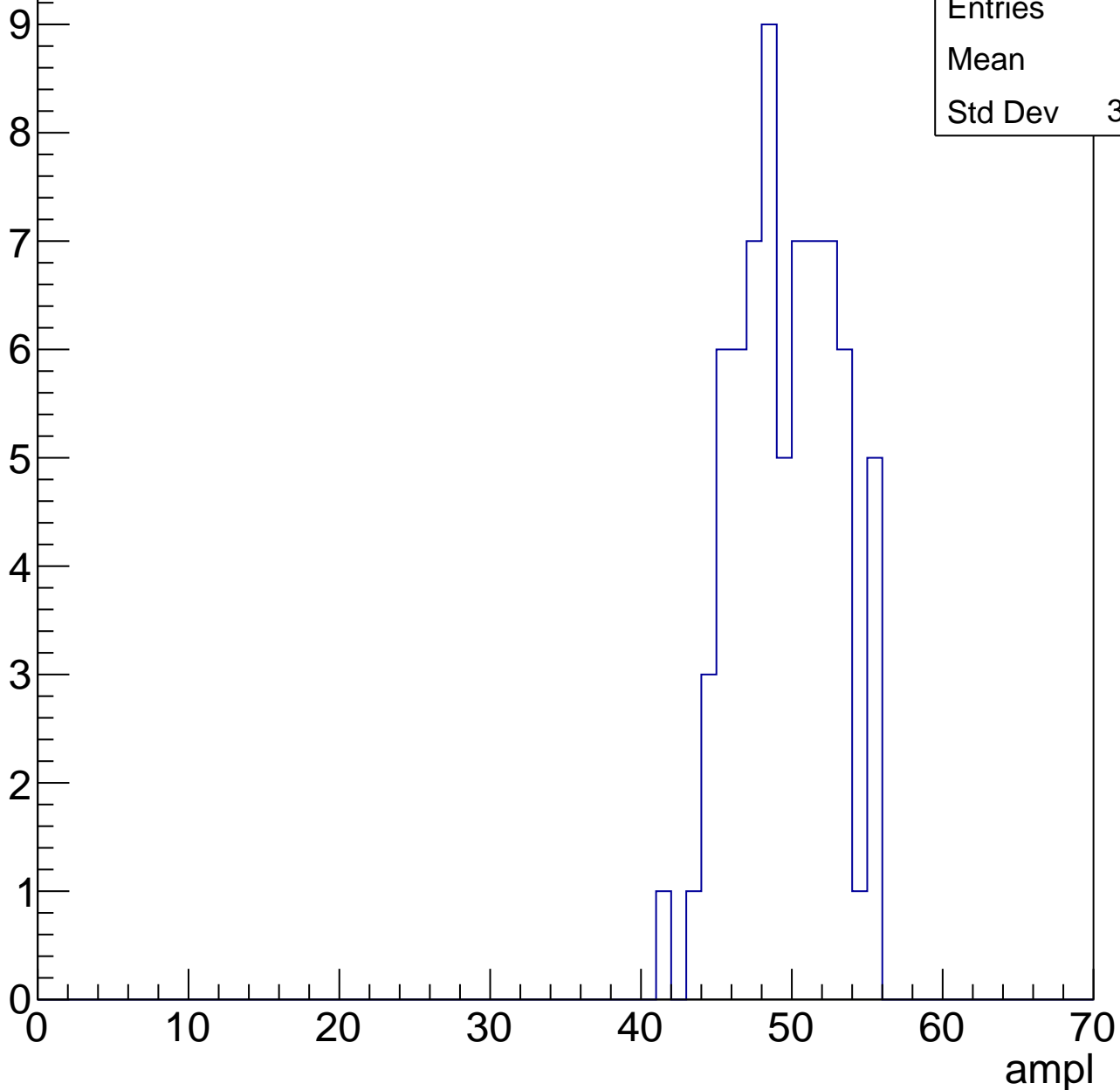


# B1L101S, U20-ch67, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

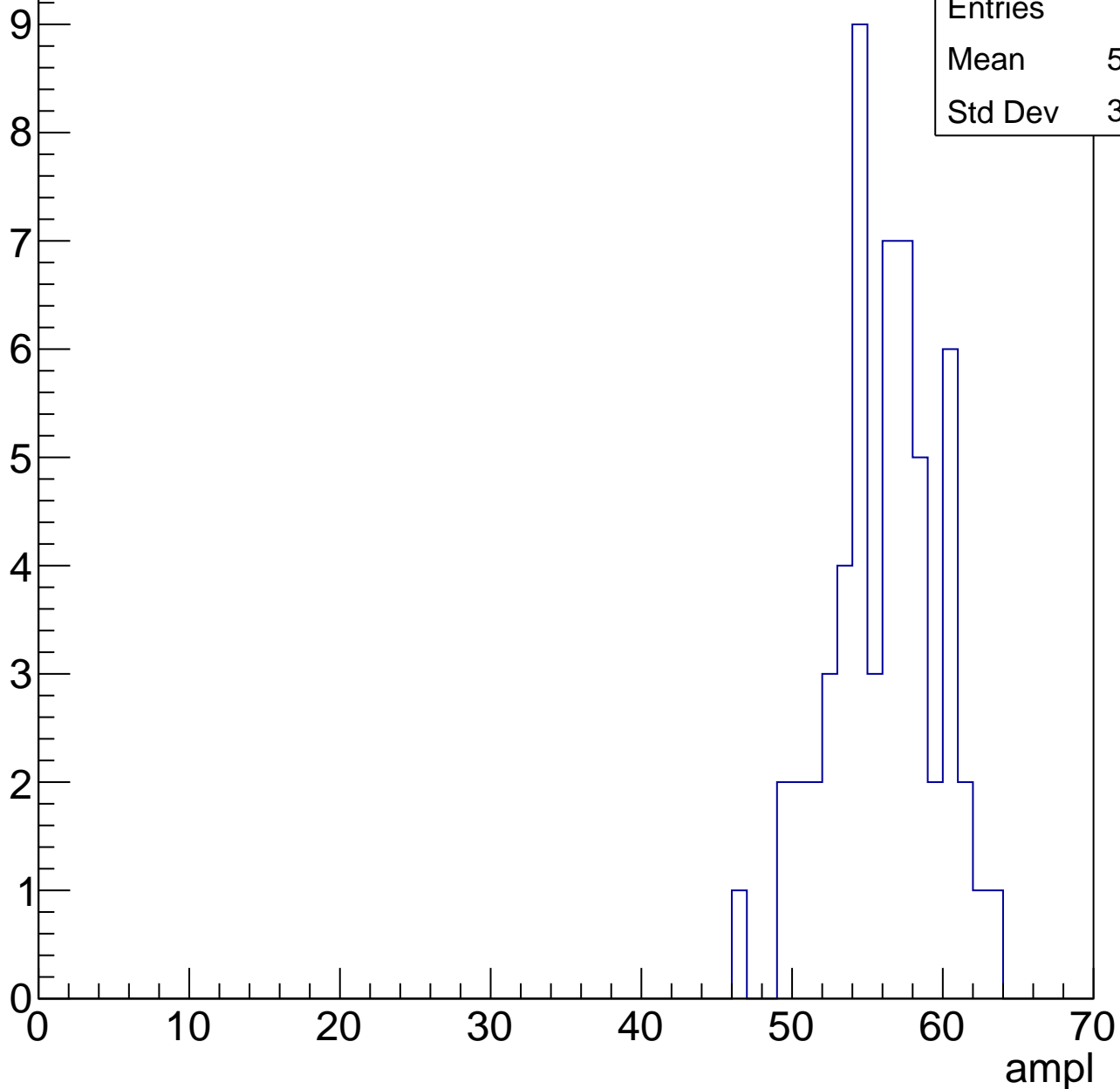
Entries	71
Mean	49.1
Std Dev	3.272



# B1L101S, U20-ch67, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	57
Mean	55.63
Std Dev	3.532

# B1L101S, U20-ch67, adc5

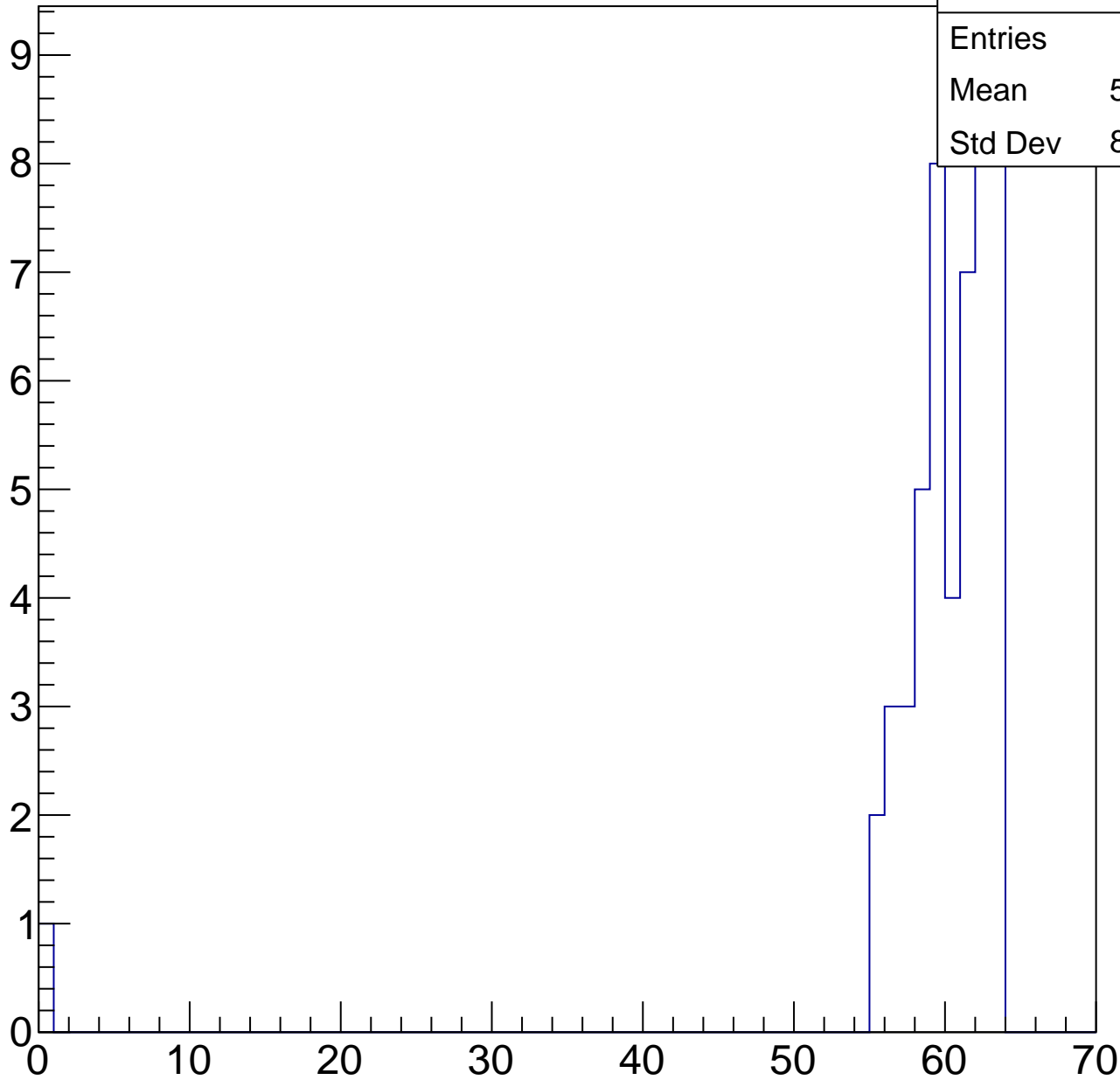
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	50
Mean	58.82
Std Dev	8.722

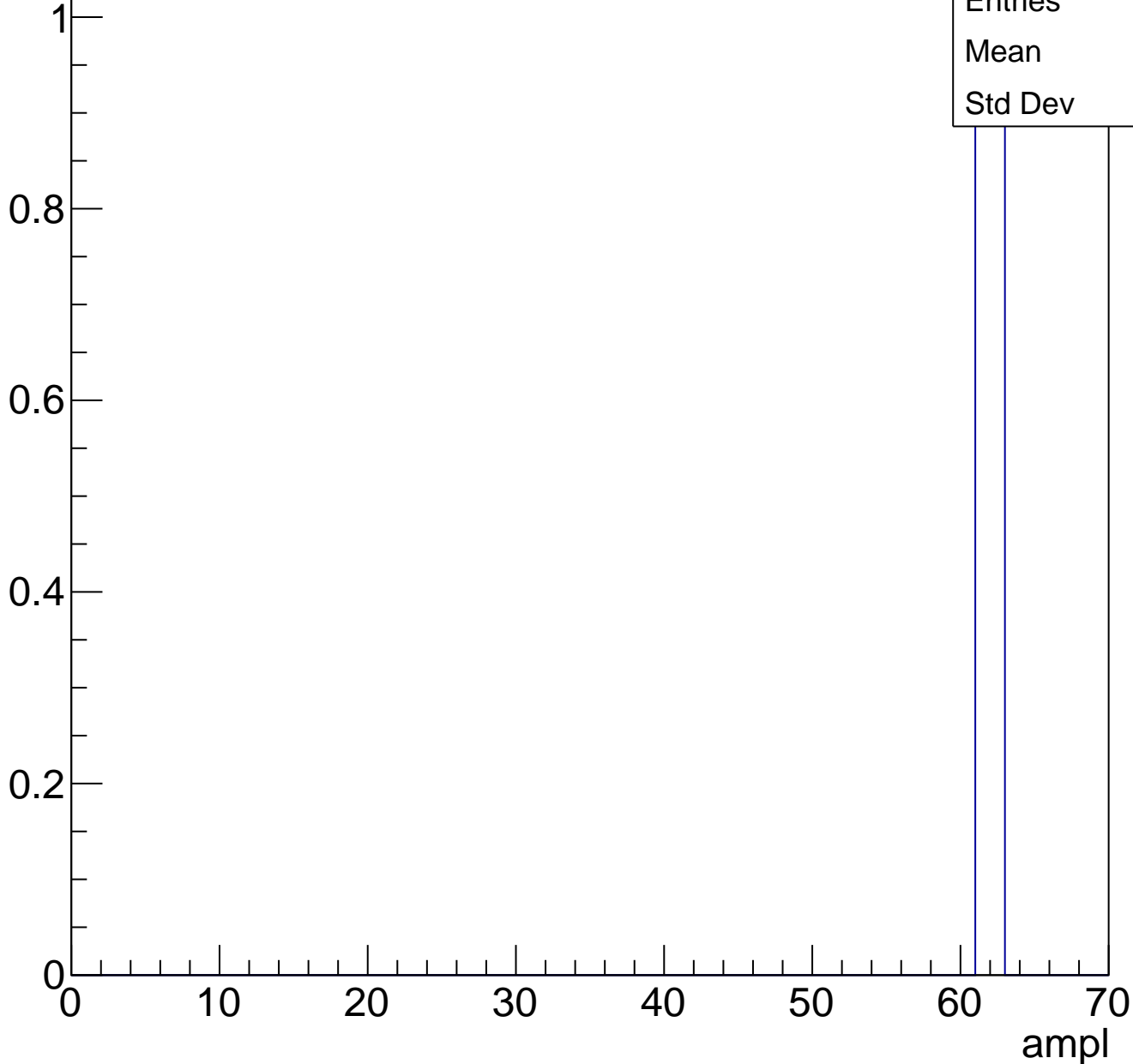
ampl



# B1L101S, U20-ch67, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U20-ch67, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L101S, U20-ch68, adc0

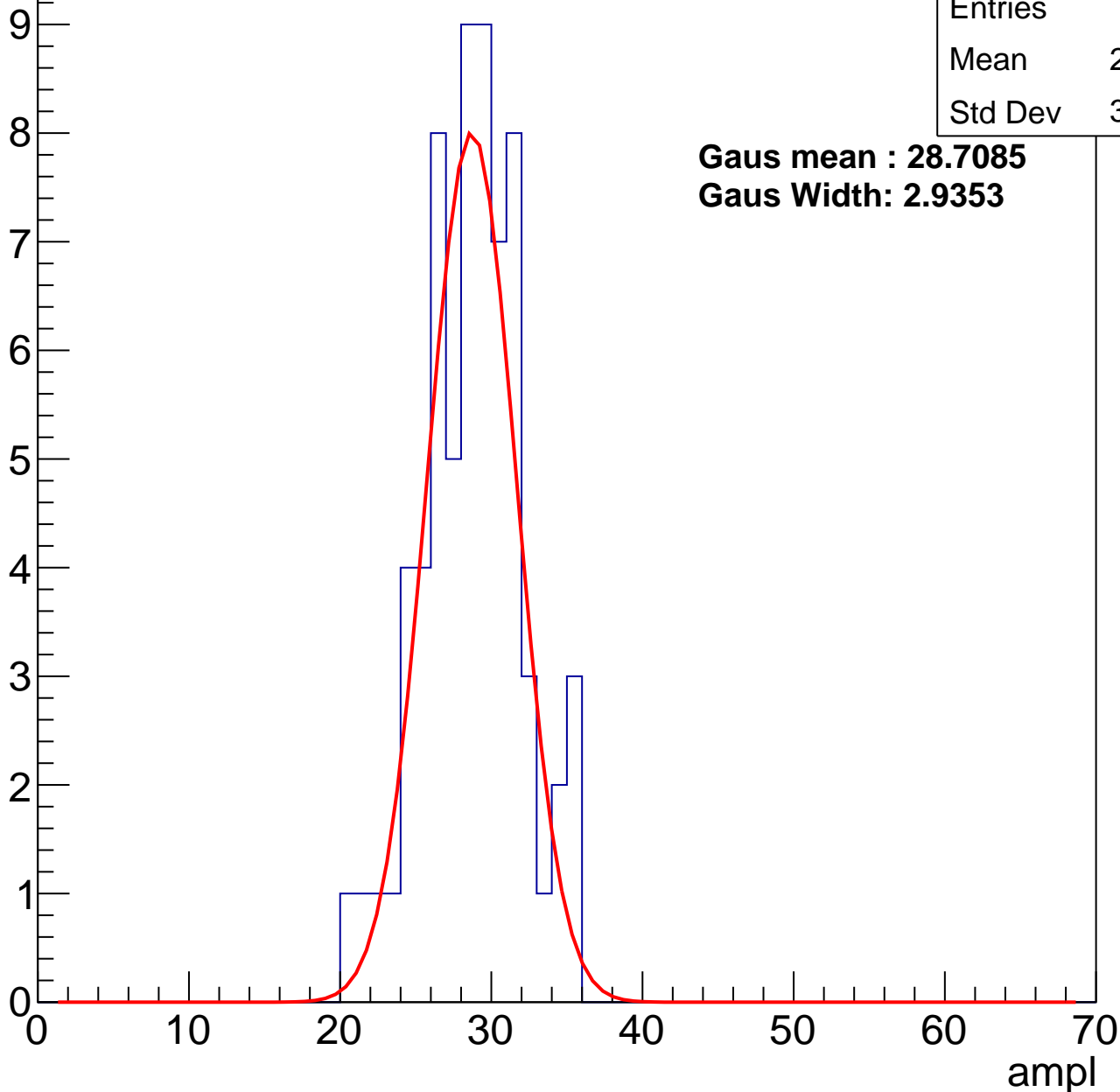
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	67
Mean	28.33
Std Dev	3.243

**Gaus mean : 28.7085**

**Gaus Width: 2.9353**



# B1L101S, U20-ch68, adc1

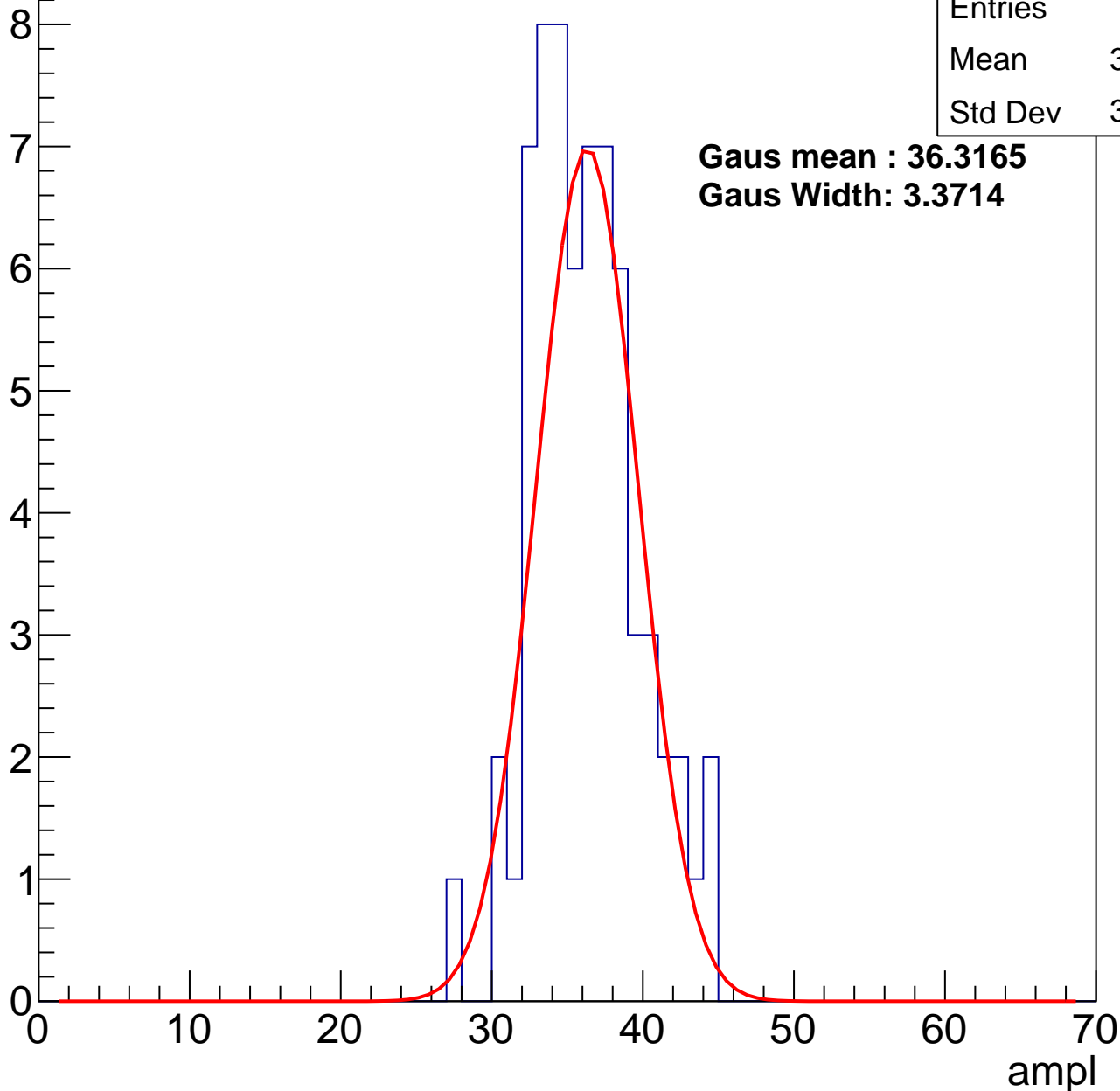
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	66
Mean	35.77
Std Dev	3.485

**Gaus mean : 36.3165**

**Gaus Width: 3.3714**



# B1L101S, U20-ch68, adc2

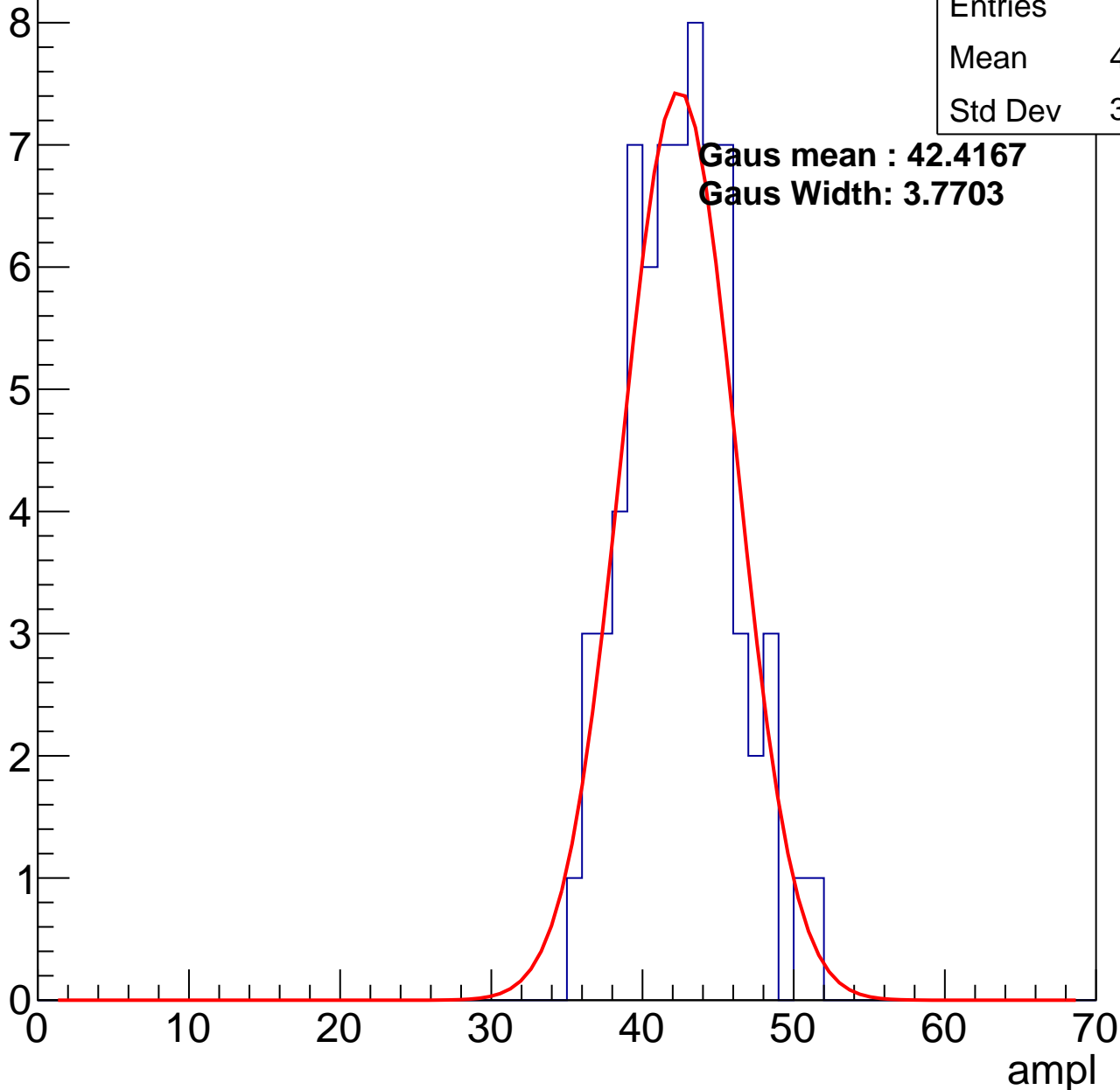
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	42.06
Std Dev	3.464

**Gaus mean : 42.4167**

**Gaus Width: 3.7703**



# B1L101S, U20-ch68, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	84
Mean	49.82
Std Dev	3.684

Entry

10

8

6

4

2

0

0

10

20

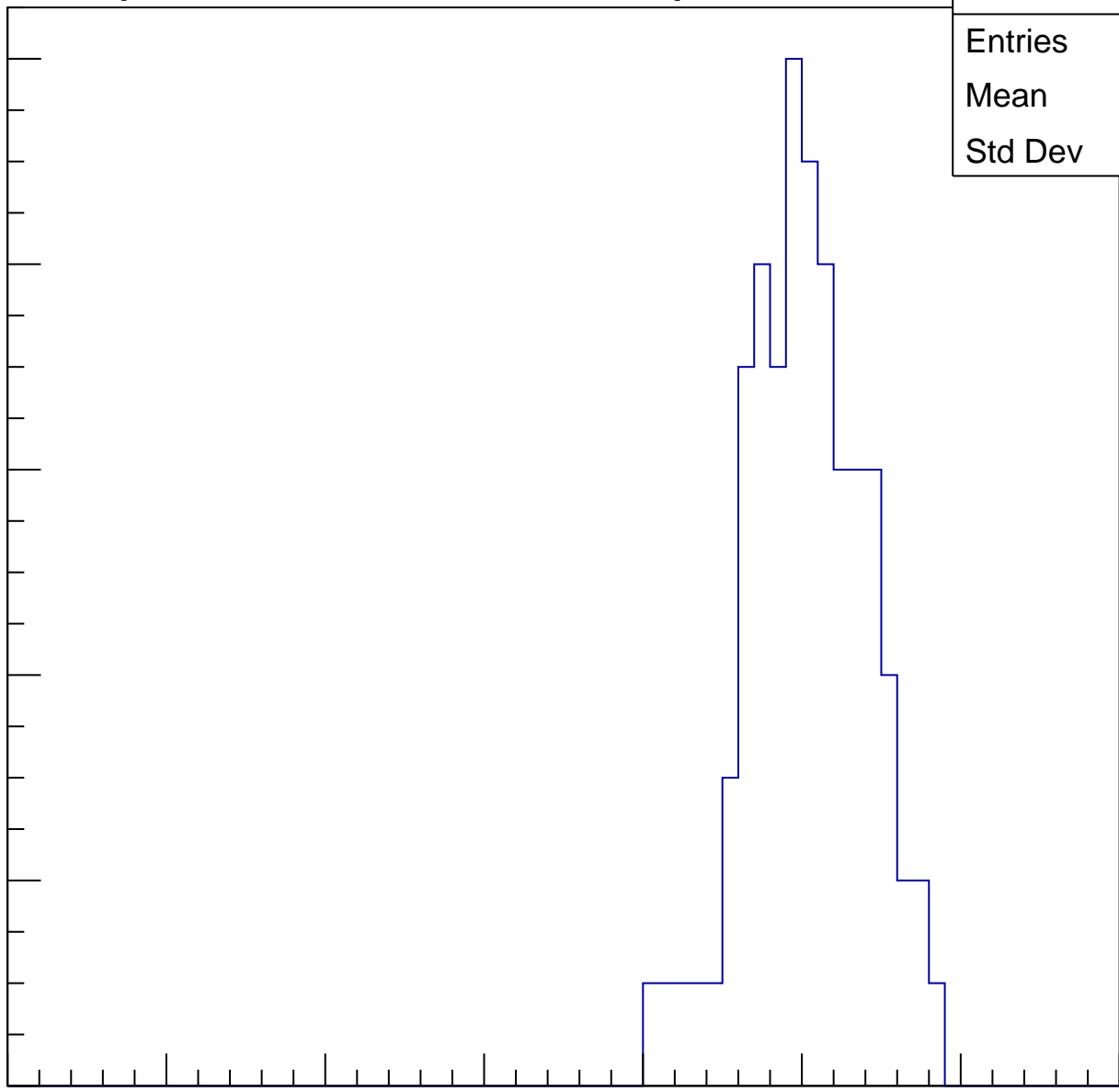
30

40

50

60

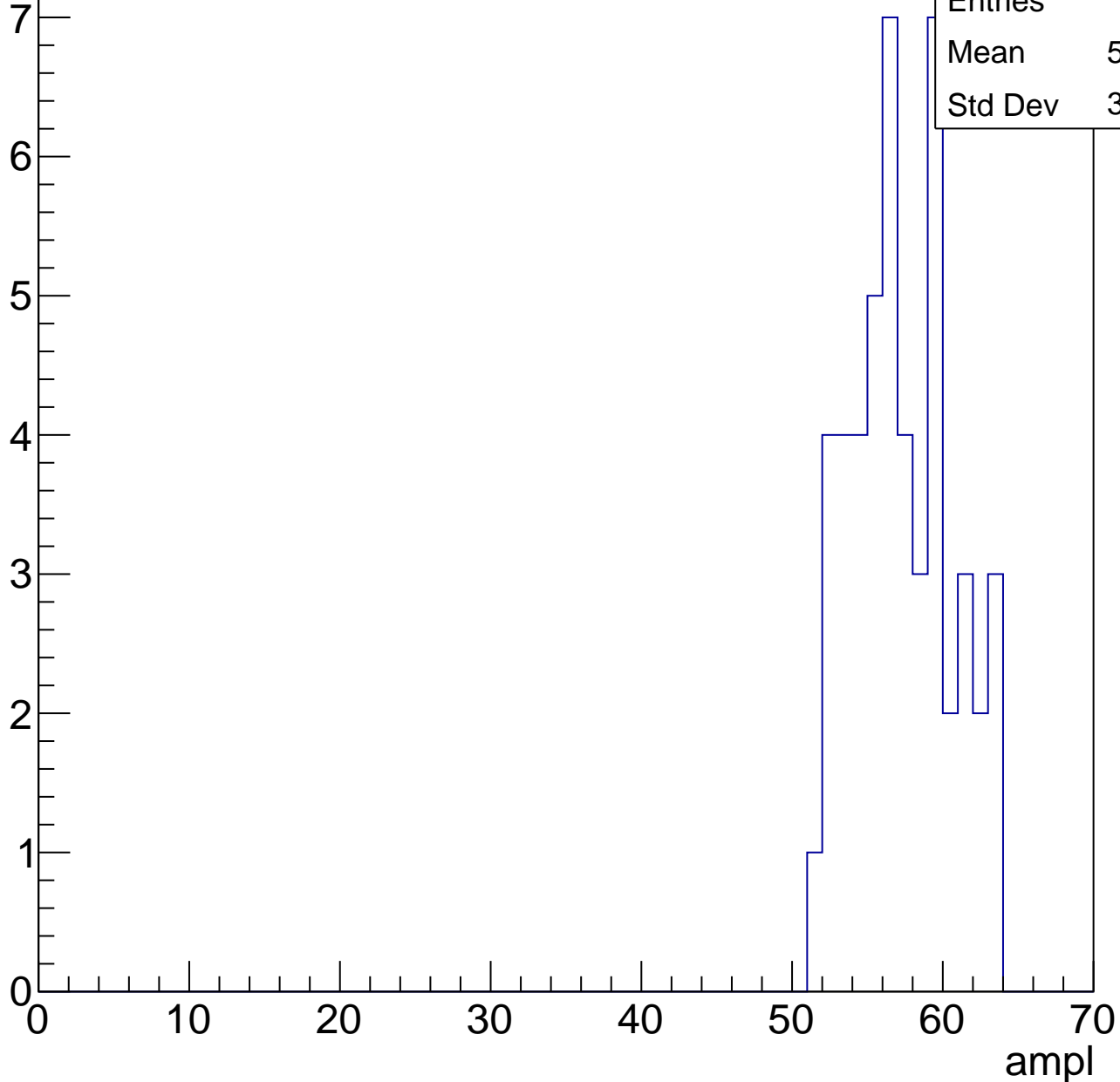
ampl



# B1L101S, U20-ch68, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

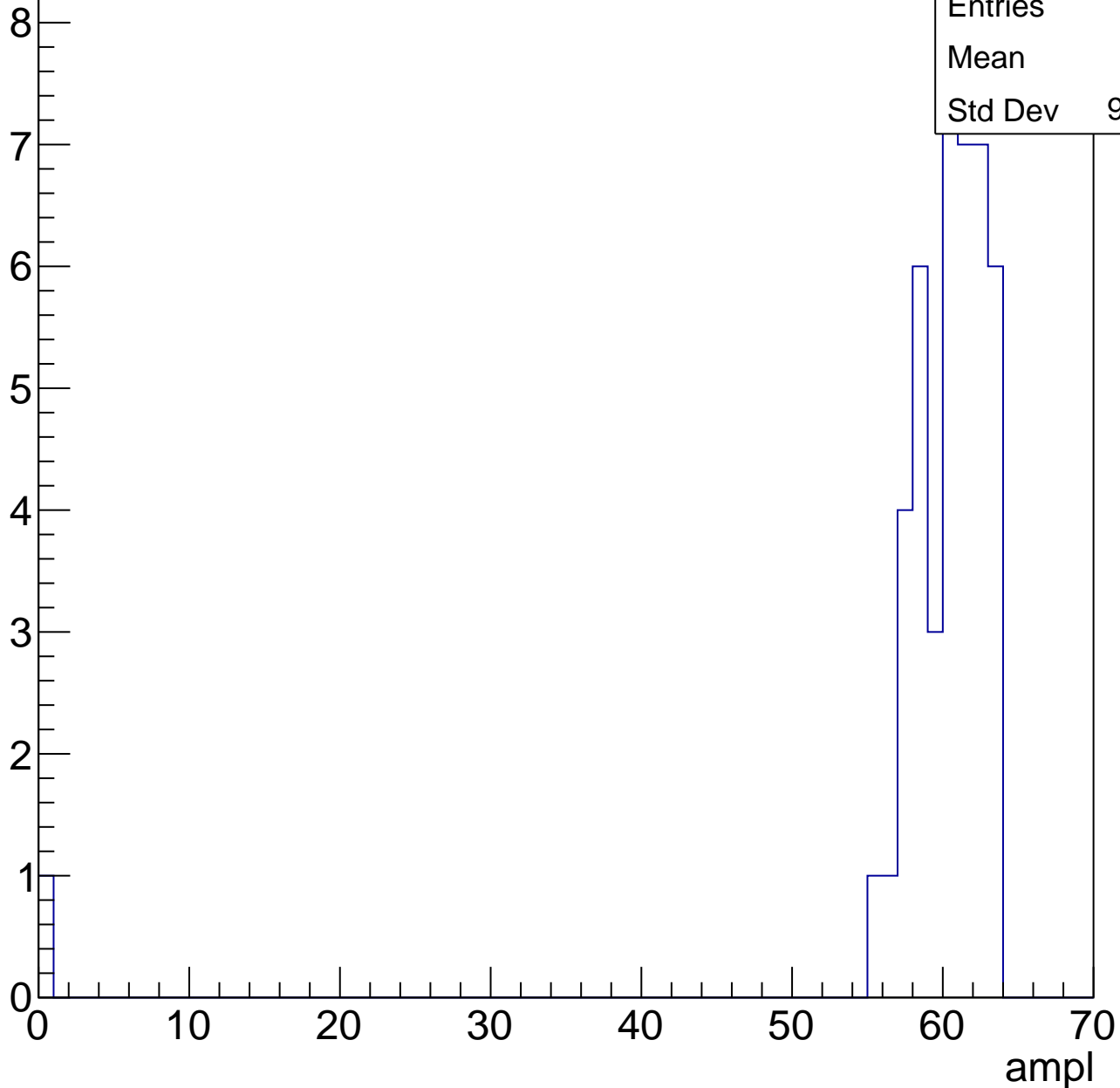
Entry



# B1L101S, U20-ch68, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U20-ch68, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U20-ch68, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U20-ch69, adc0

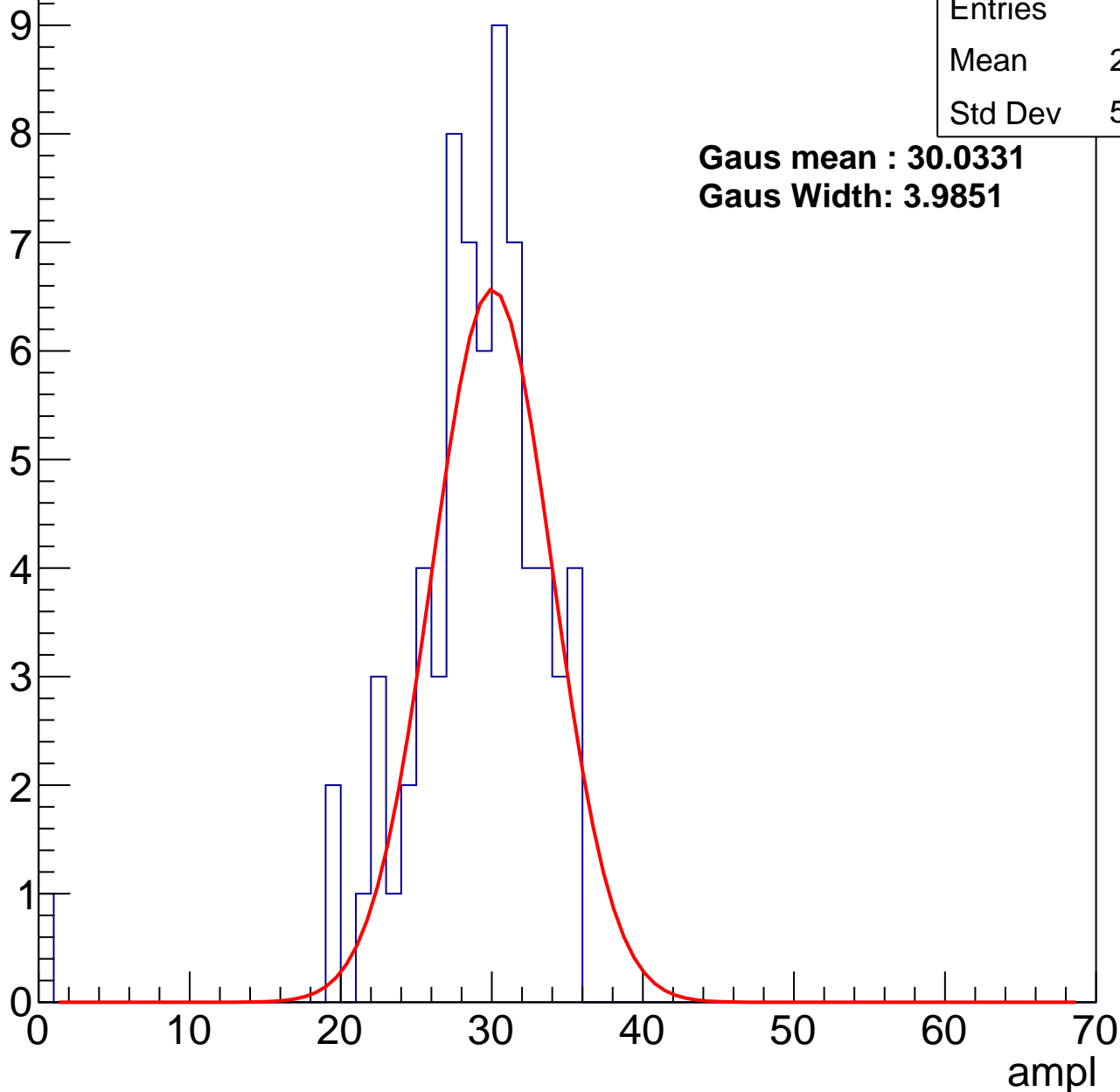
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	28.25
Std Dev	5.086

**Gaus mean : 30.0331**

**Gaus Width: 3.9851**



# B1L101S, U20-ch69, adc1

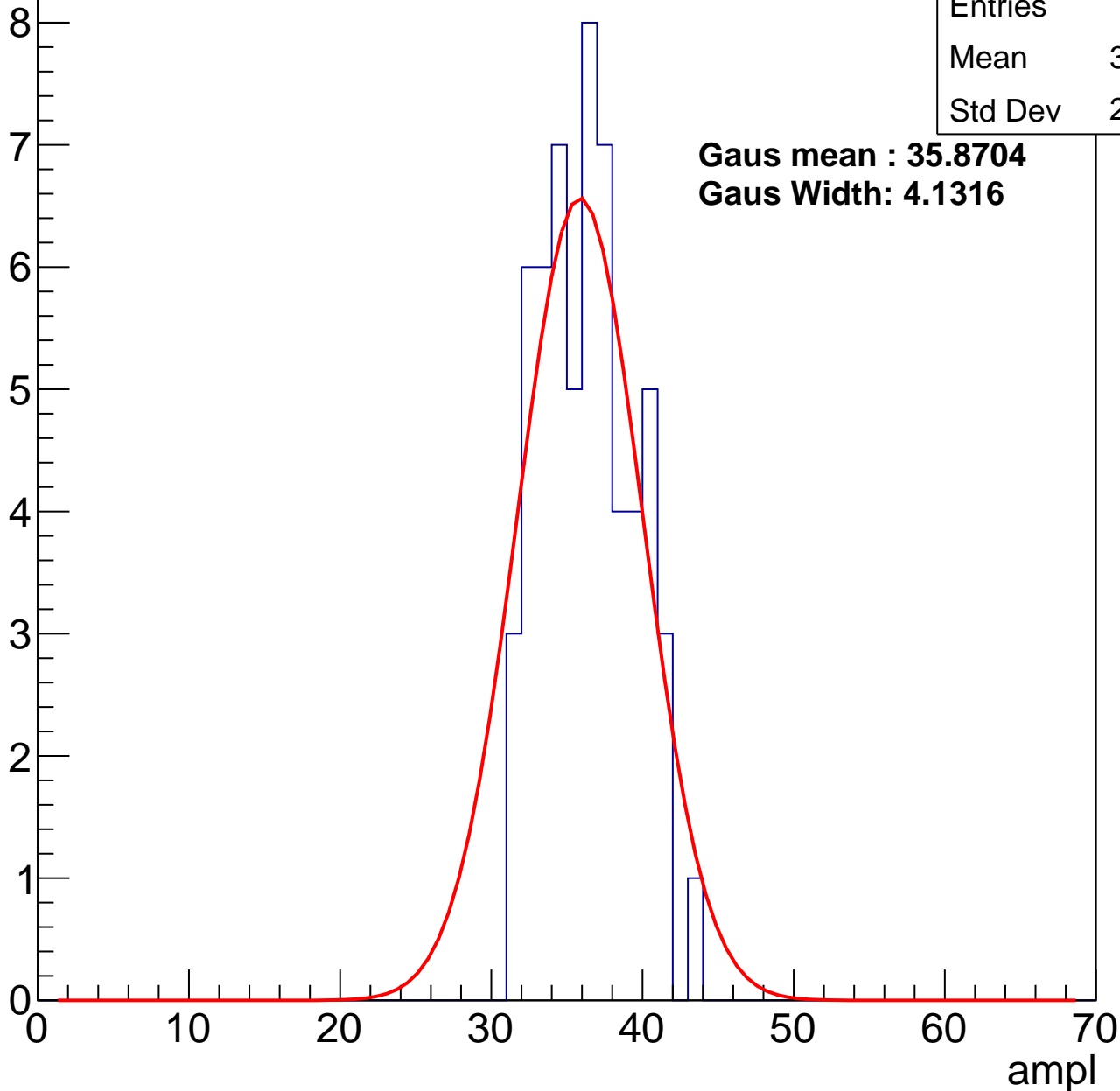
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	59
Mean	35.88
Std Dev	2.969

**Gaus mean : 35.8704**

**Gaus Width: 4.1316**



# B1L101S, U20-ch69, adc2

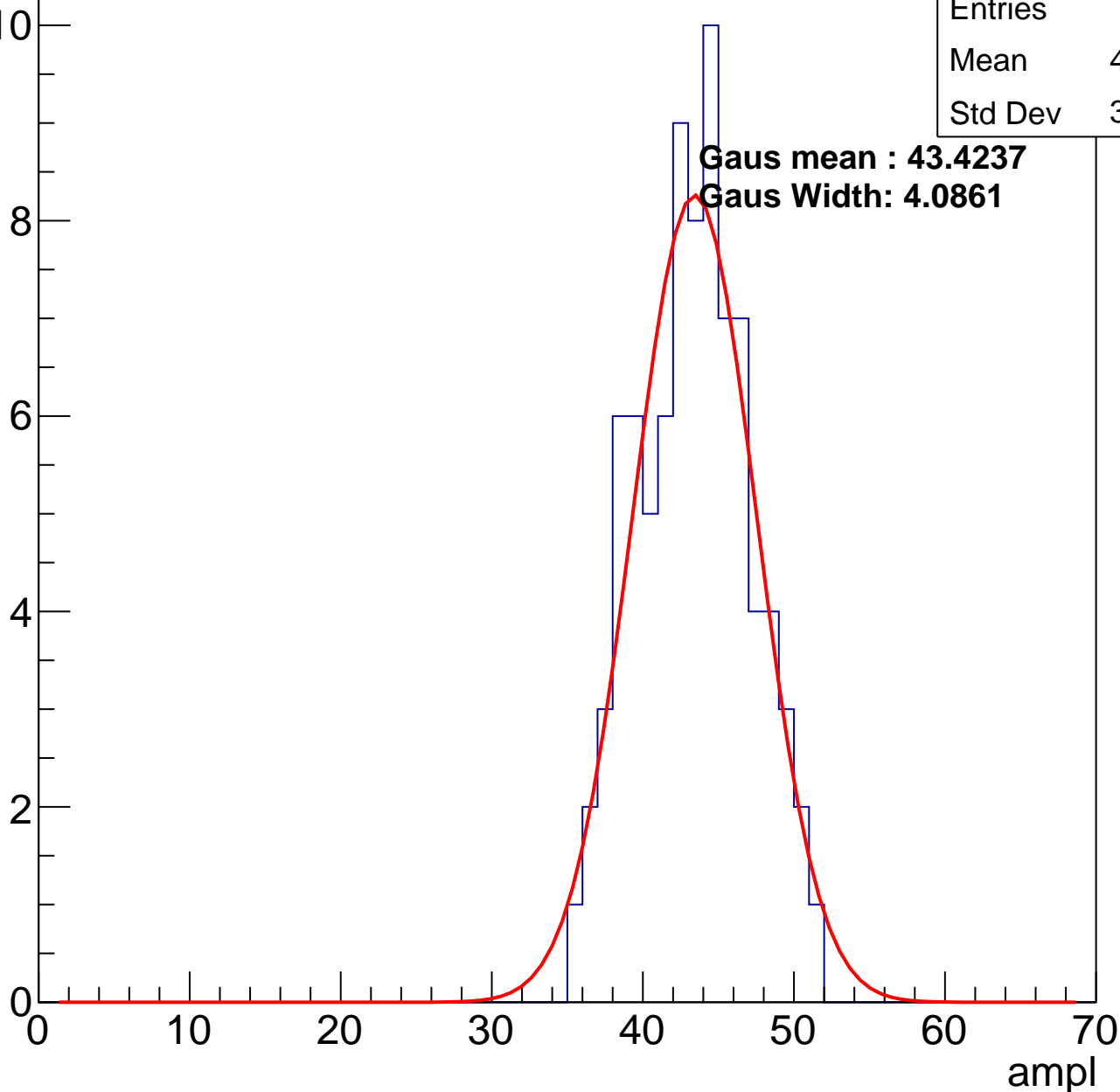
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	84
Mean	42.89
Std Dev	3.665

**Gaus mean : 43.4237**

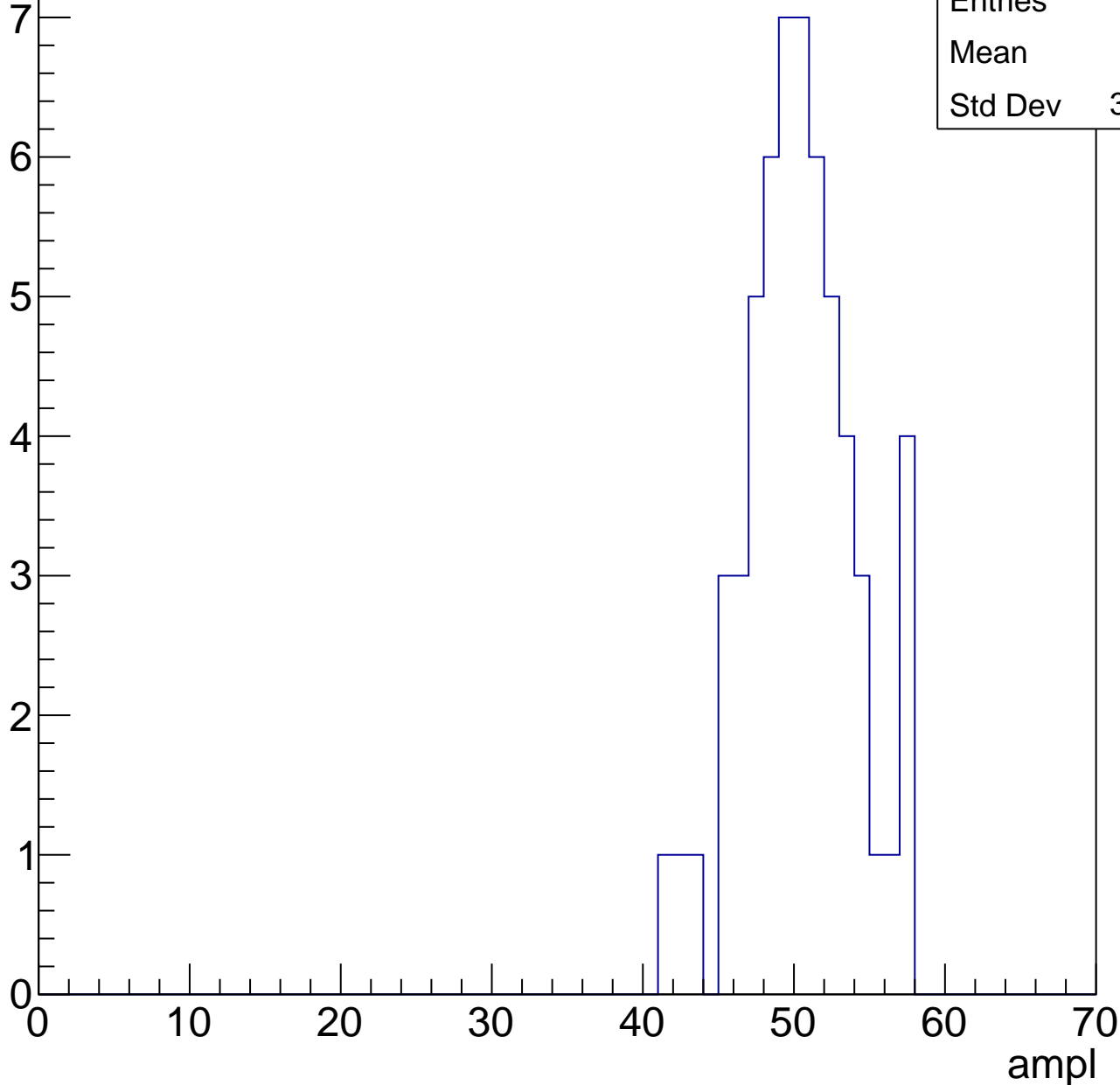
**Gaus Width: 4.0861**



# B1L101S, U20-ch69, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

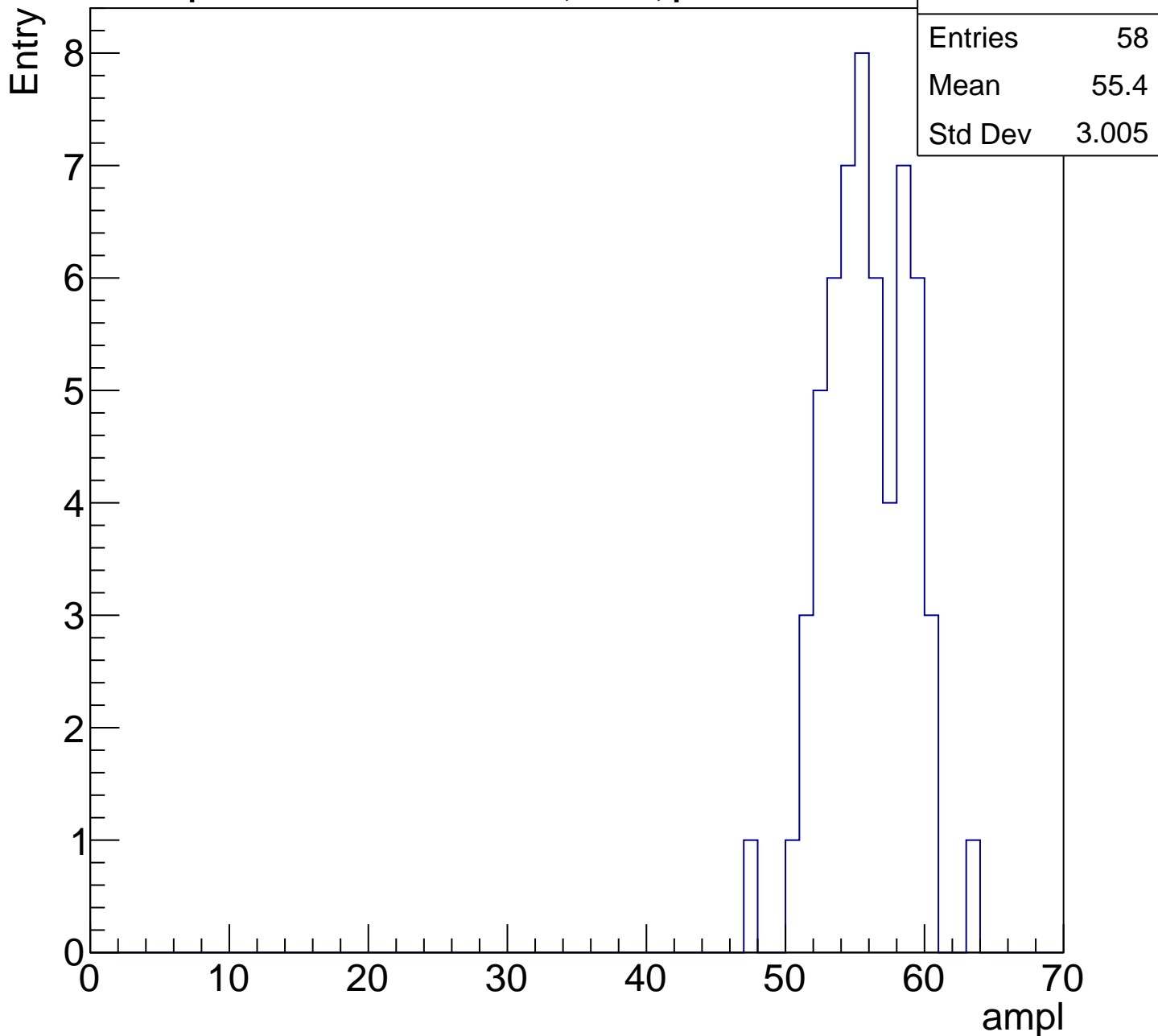
Entry



Entries	58
Mean	49.9
Std Dev	3.618

# B1L101S, U20-ch69, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

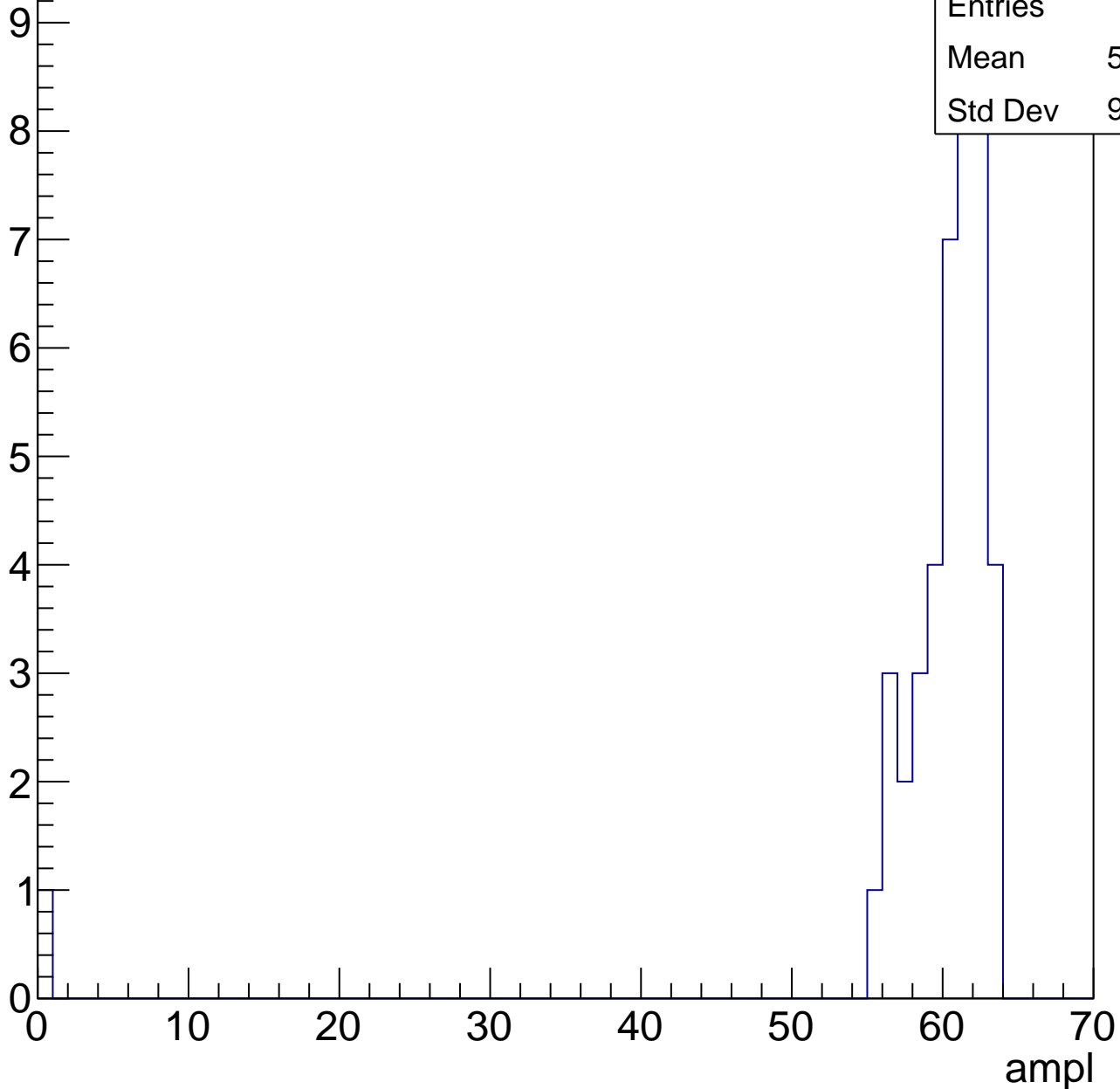


# B1L101S, U20-ch69, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	42
Mean	58.69
Std Dev	9.405



# B1L101S, U20-ch69, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

5

4

3

2

1

0

Entries	8
Mean	62.38
Std Dev	0.857

ampl

0

10

20

30

40

50

60

70



# B1L101S, U20-ch69, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L101S, U20-ch70, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	60
Mean	28.52
Std Dev	3.165

**Gaus mean : 29.5233**

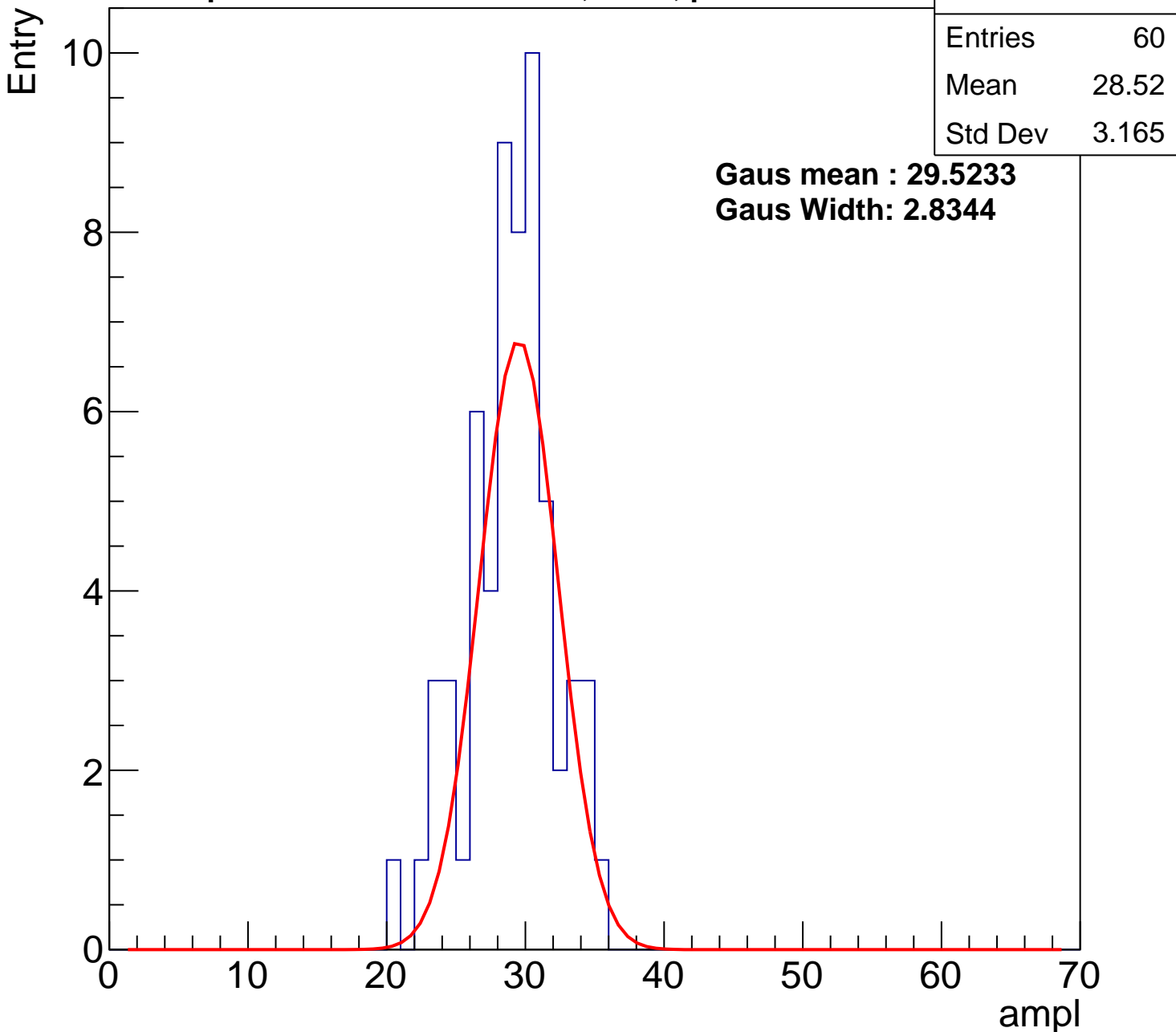
**Gaus Width: 2.8344**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U20-ch70, adc1

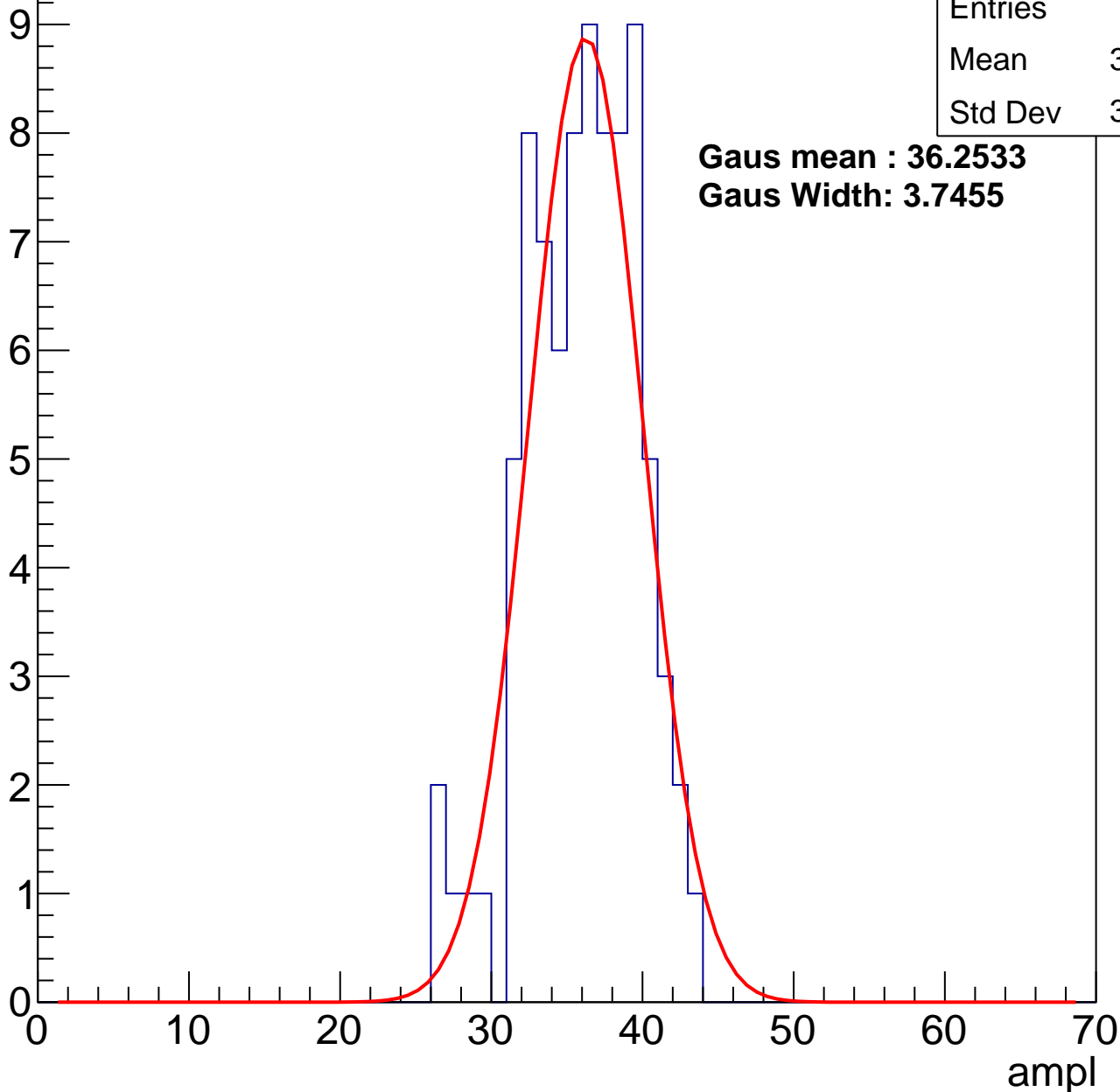
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	84
Mean	35.56
Std Dev	3.656

**Gaus mean : 36.2533**

**Gaus Width: 3.7455**



# B1L101S, U20-ch70, adc2

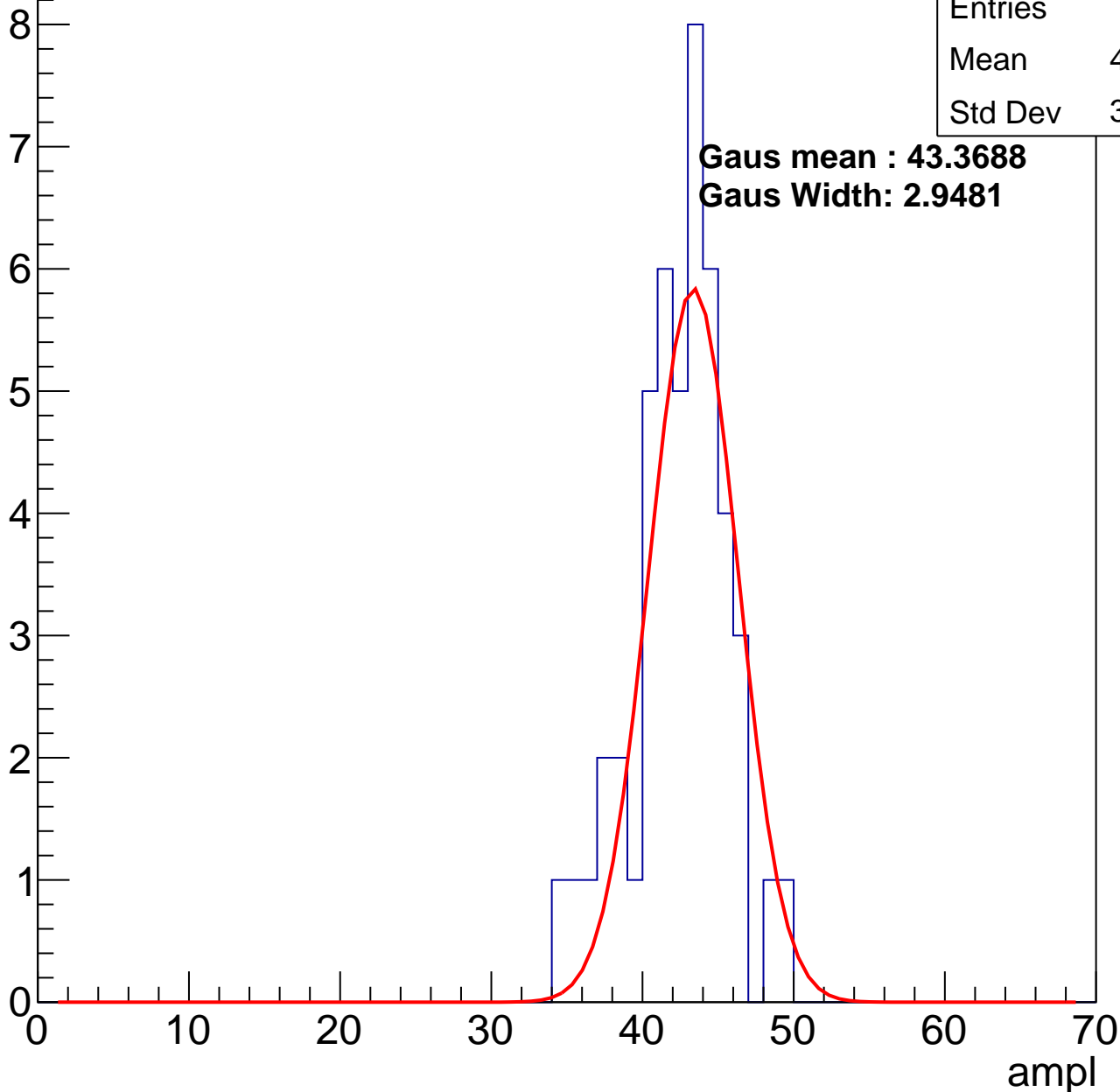
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	47
Mean	41.98
Std Dev	3.152

**Gaus mean : 43.3688**

**Gaus Width: 2.9481**



# B1L101S, U20-ch70, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

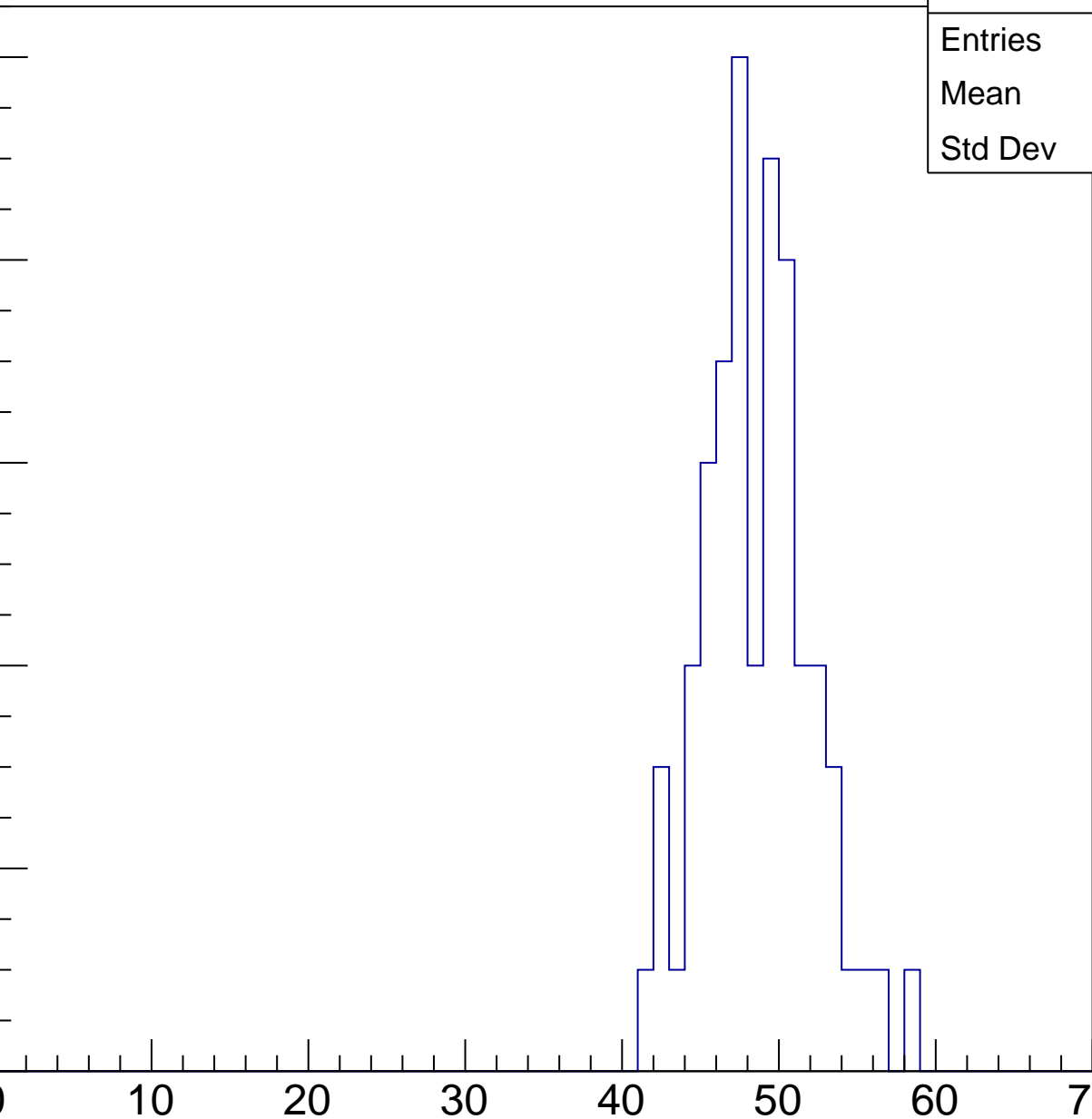
Entries	68
Mean	48.16
Std Dev	3.433

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

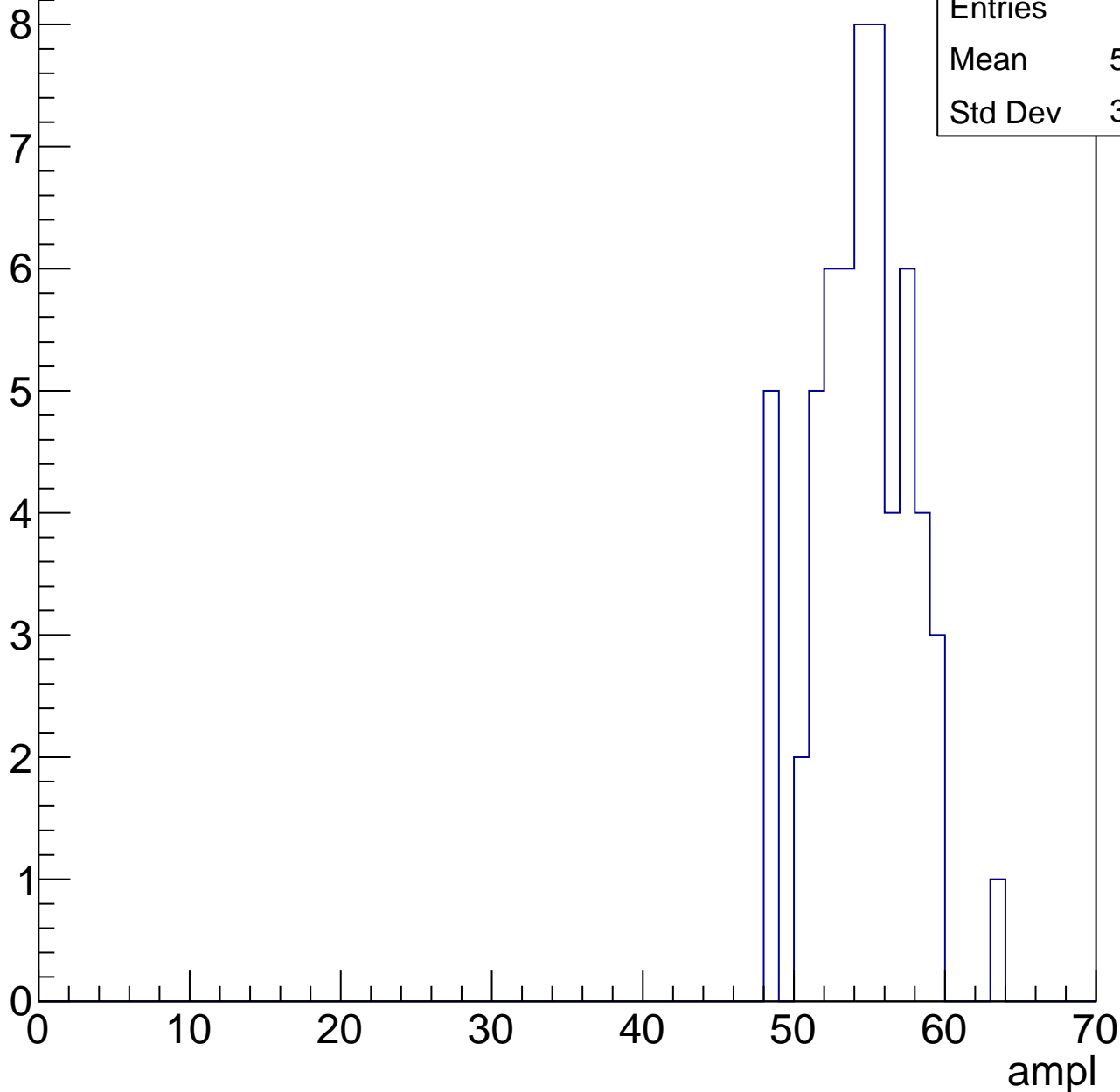


# B1L101S, U20-ch70, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	58
Mean	54.05
Std Dev	3.175

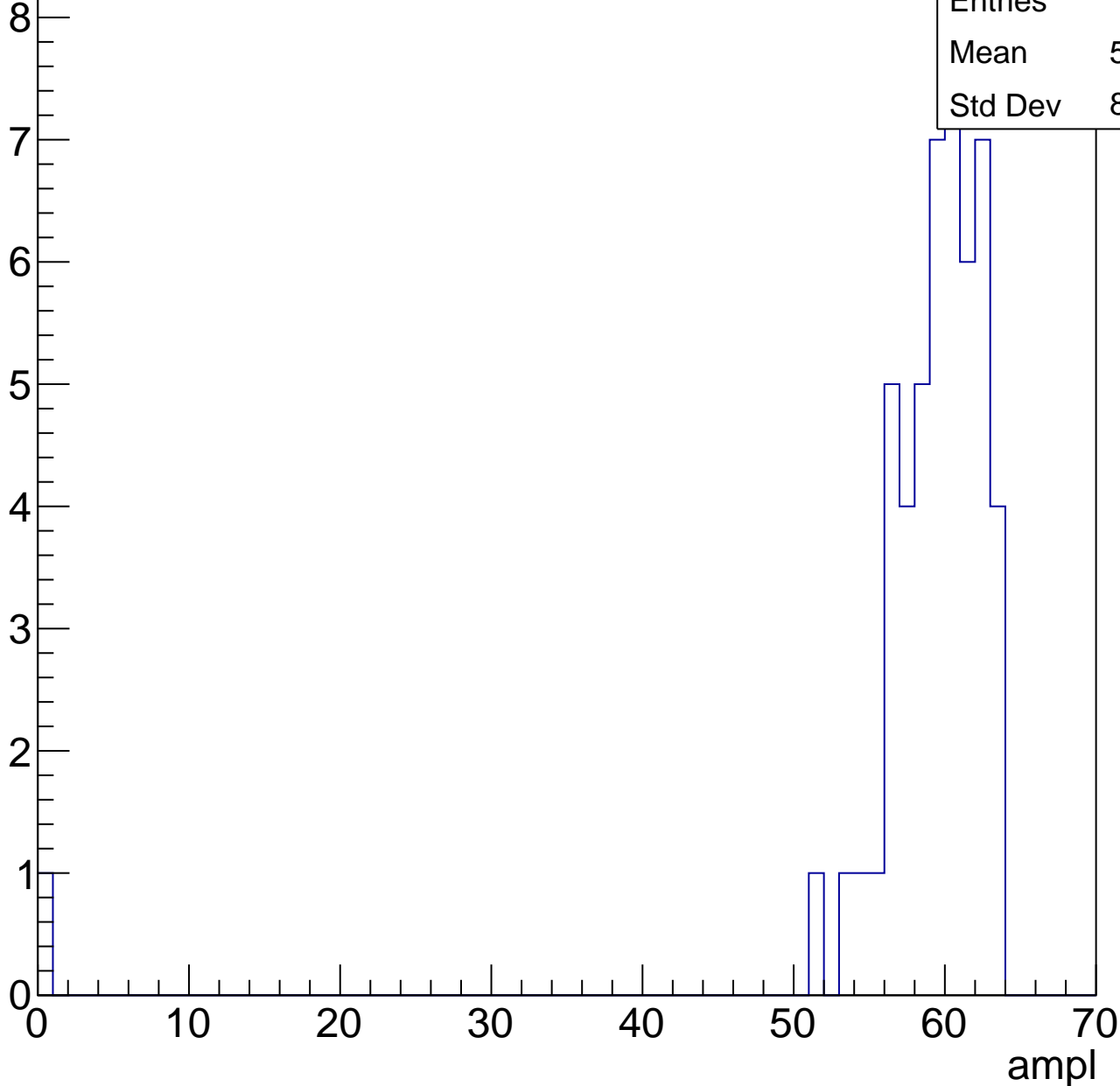


# B1L101S, U20-ch70, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	51
Mean	57.96
Std Dev	8.623

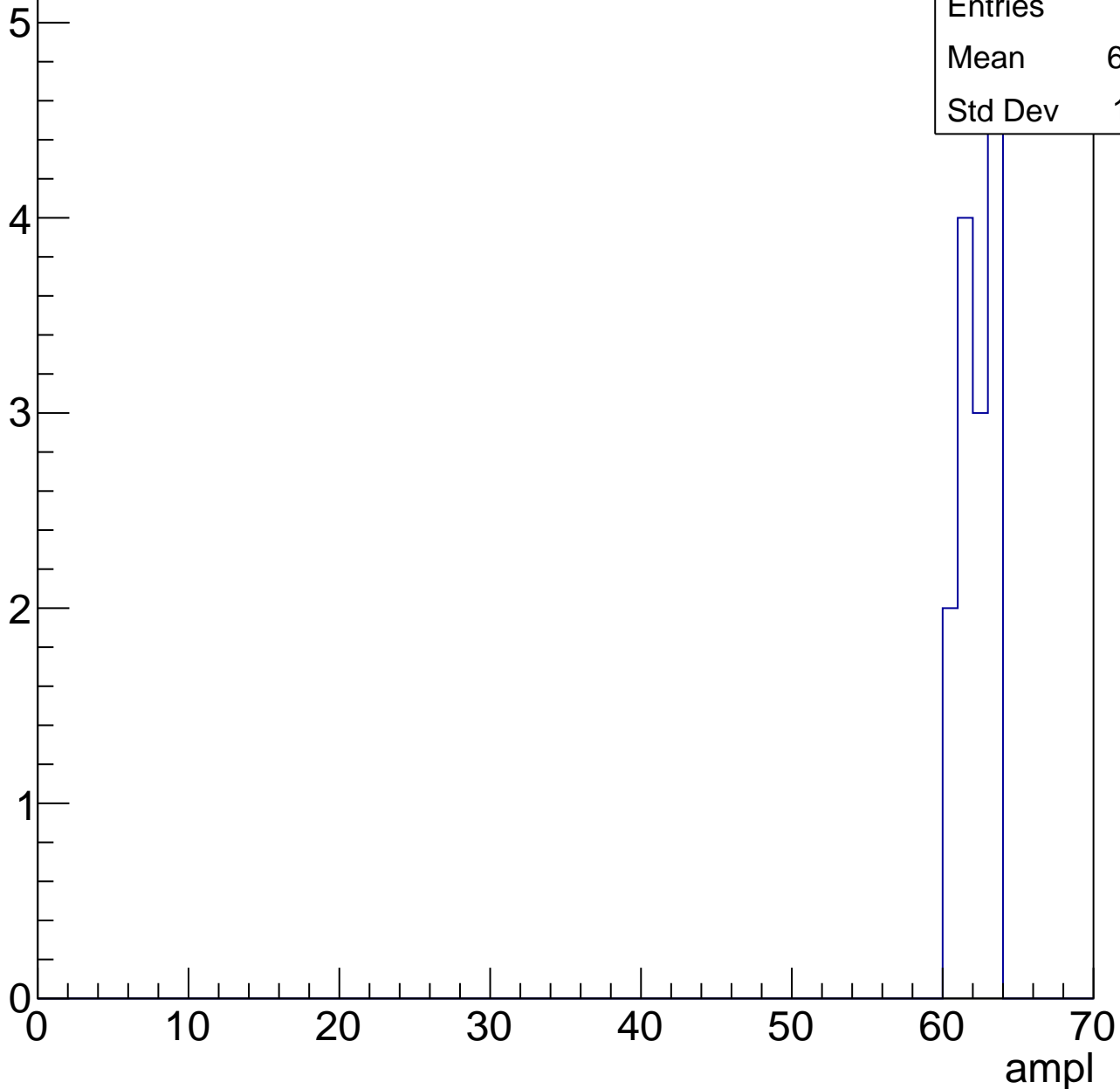


# B1L101S, U20-ch70, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	14
Mean	61.79
Std Dev	1.081





# B1L101S, U20-ch70, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	2
Mean	9.5
Std Dev	9.5

# B1L101S, U20-ch71, adc0

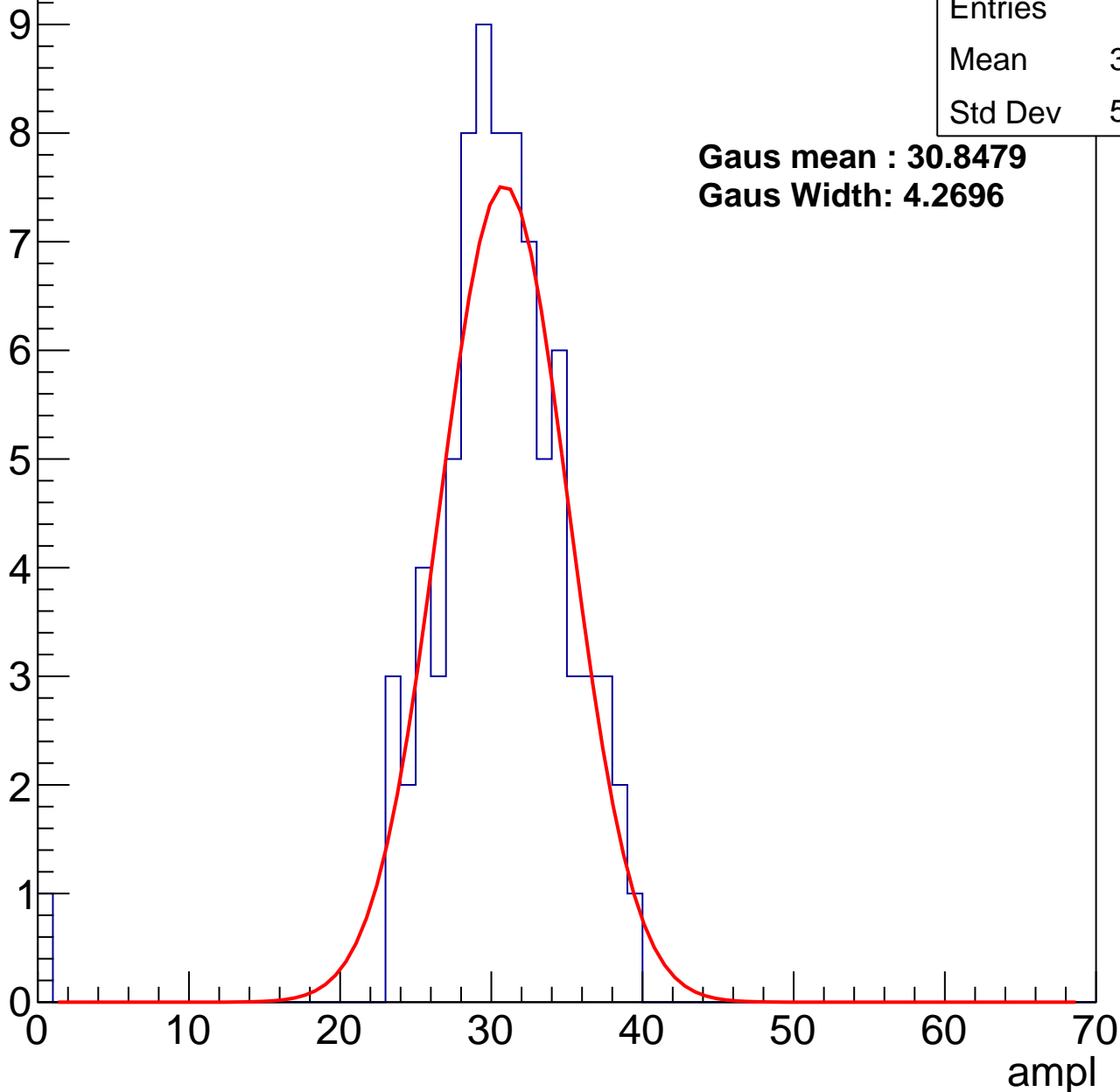
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	81
Mean	30.06
Std Dev	5.054

**Gaus mean : 30.8479**

**Gaus Width: 4.2696**



# B1L101S, U20-ch71, adc1

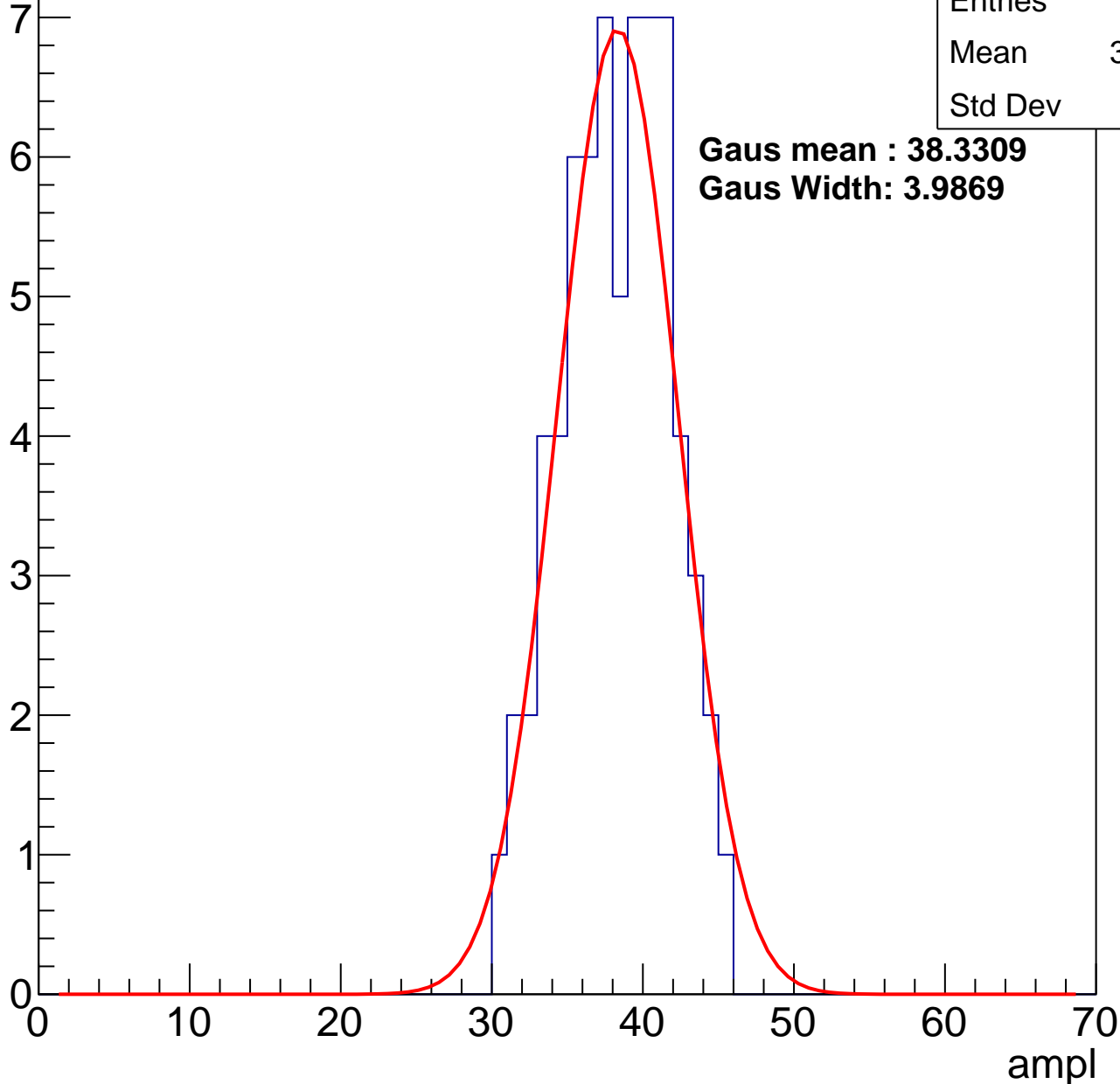
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	37.78
Std Dev	3.51

**Gaus mean : 38.3309**

**Gaus Width: 3.9869**



# B1L101S, U20-ch71, adc2

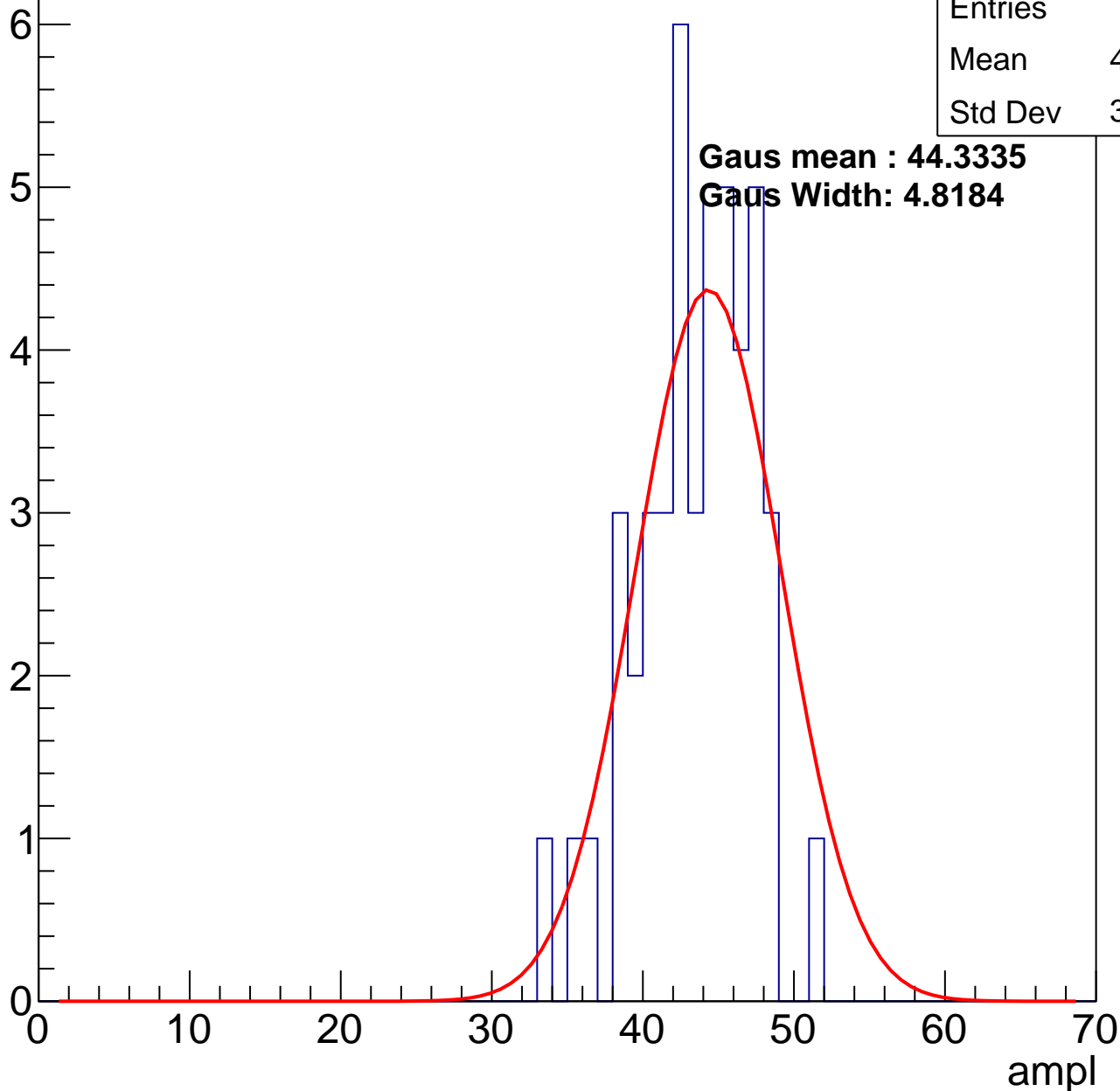
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	46
Mean	43.02
Std Dev	3.744

**Gaus mean : 44.3335**

**Gaus Width: 4.8184**

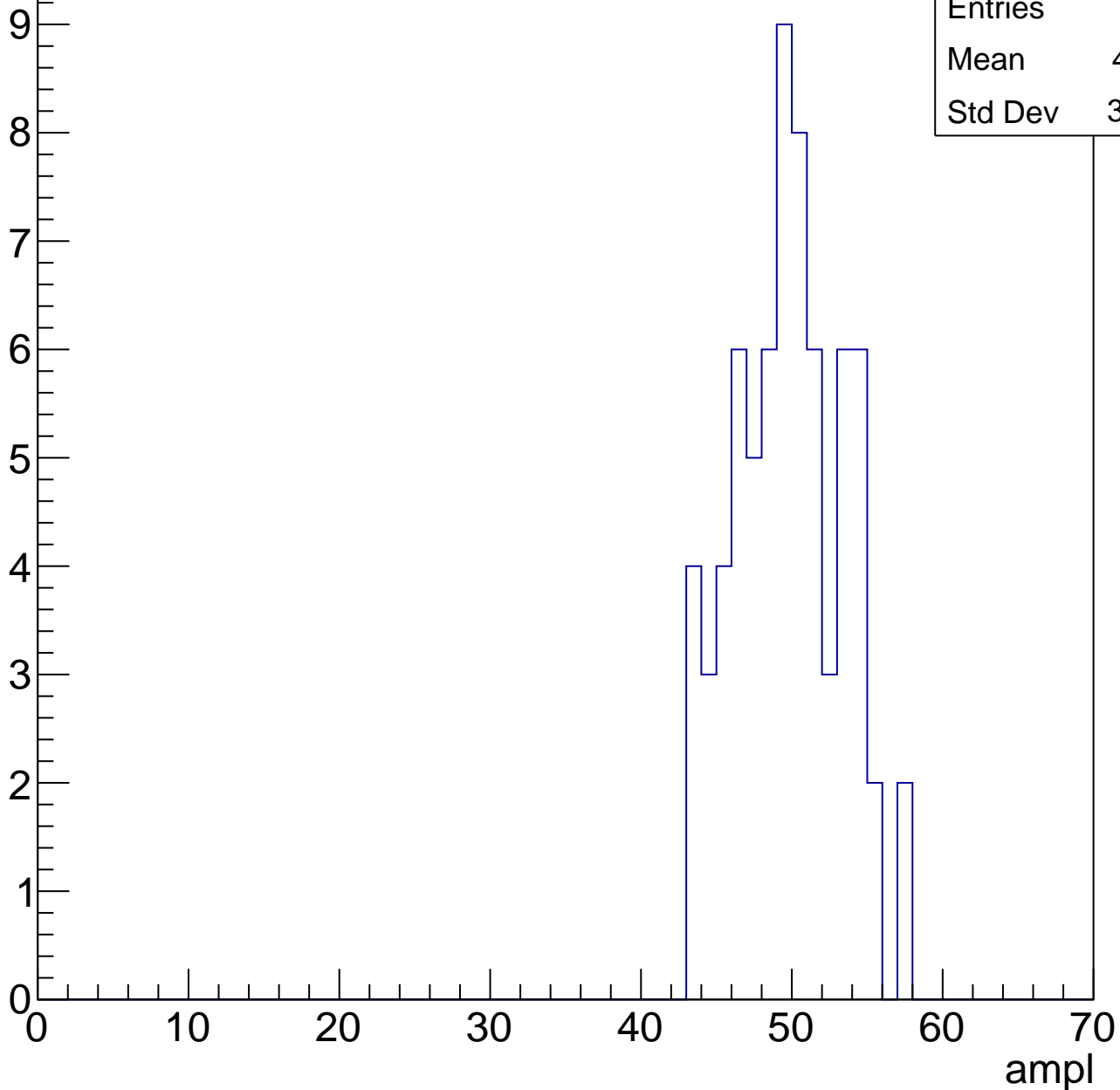


# B1L101S, U20-ch71, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	49.31
Std Dev	3.507

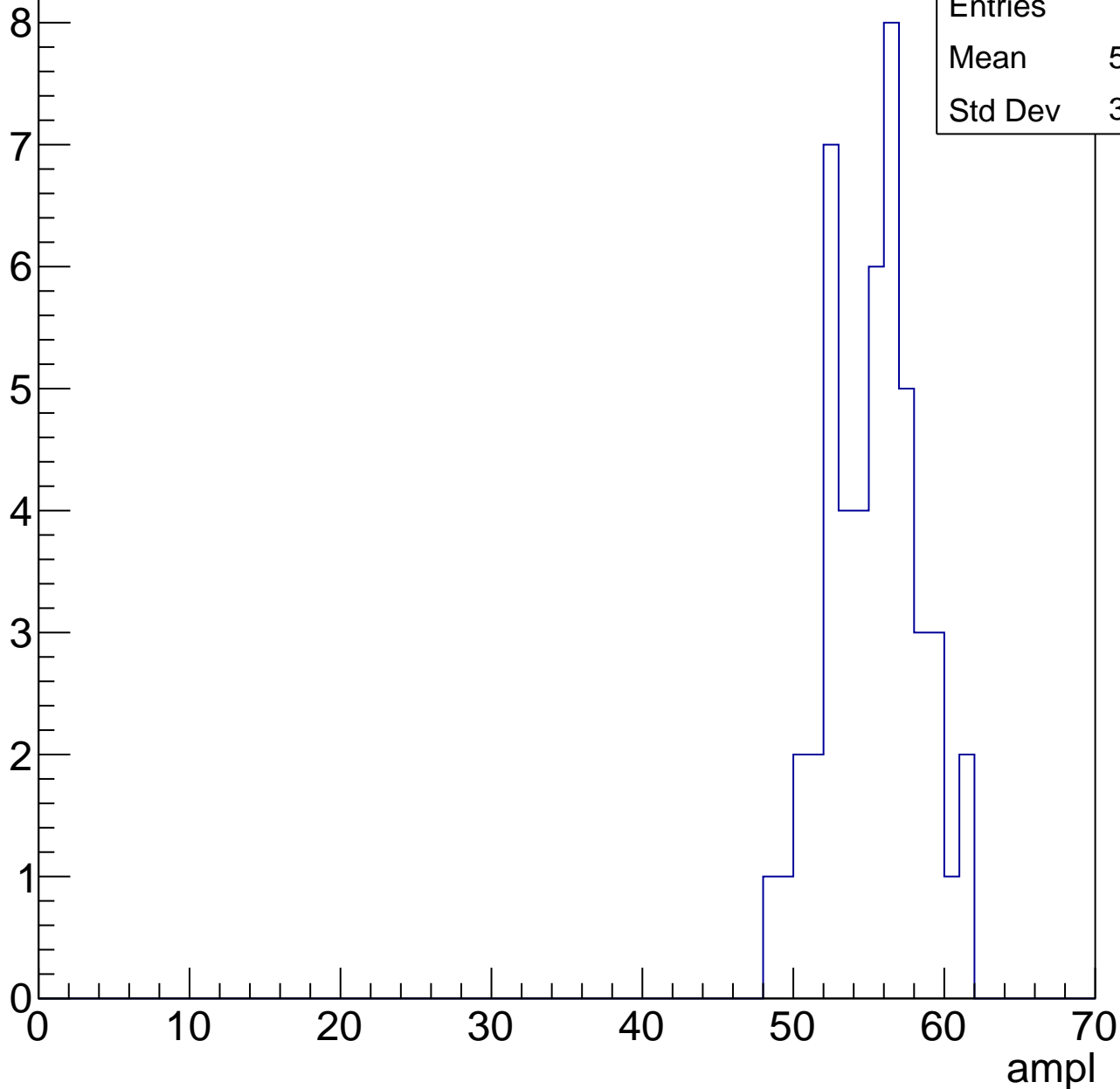


# B1L101S, U20-ch71, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

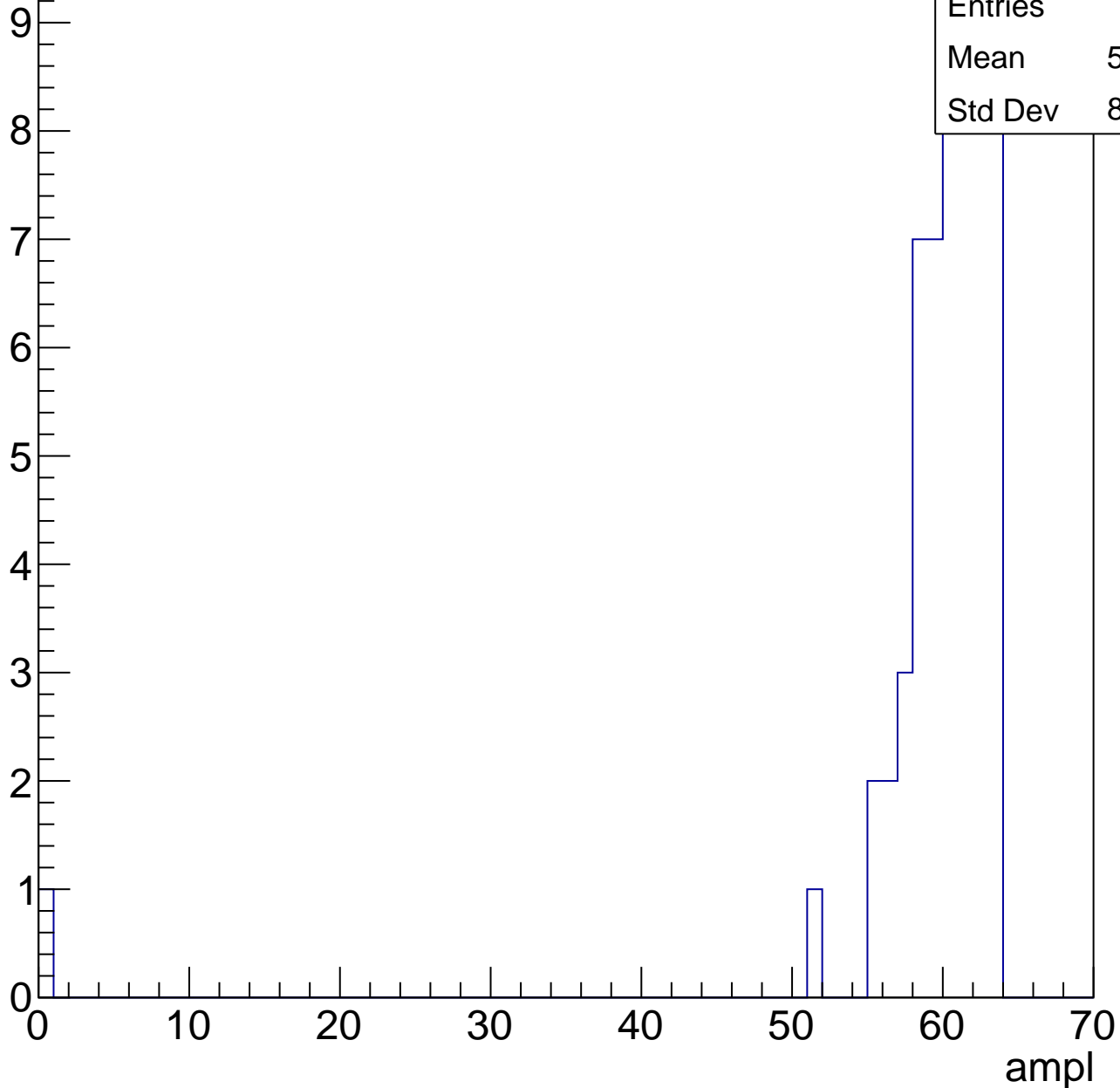
Entries	49
Mean	54.84
Std Dev	3.026



# B1L101S, U20-ch71, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U20-ch71, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	3
Mean	62.67
Std Dev	0.4714

ampl

0 10 20 30 40 50 60 70



# B1L101S, U20-ch71, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	3
Mean	0
Std Dev	0

# B1L101S, U20-ch72, adc0

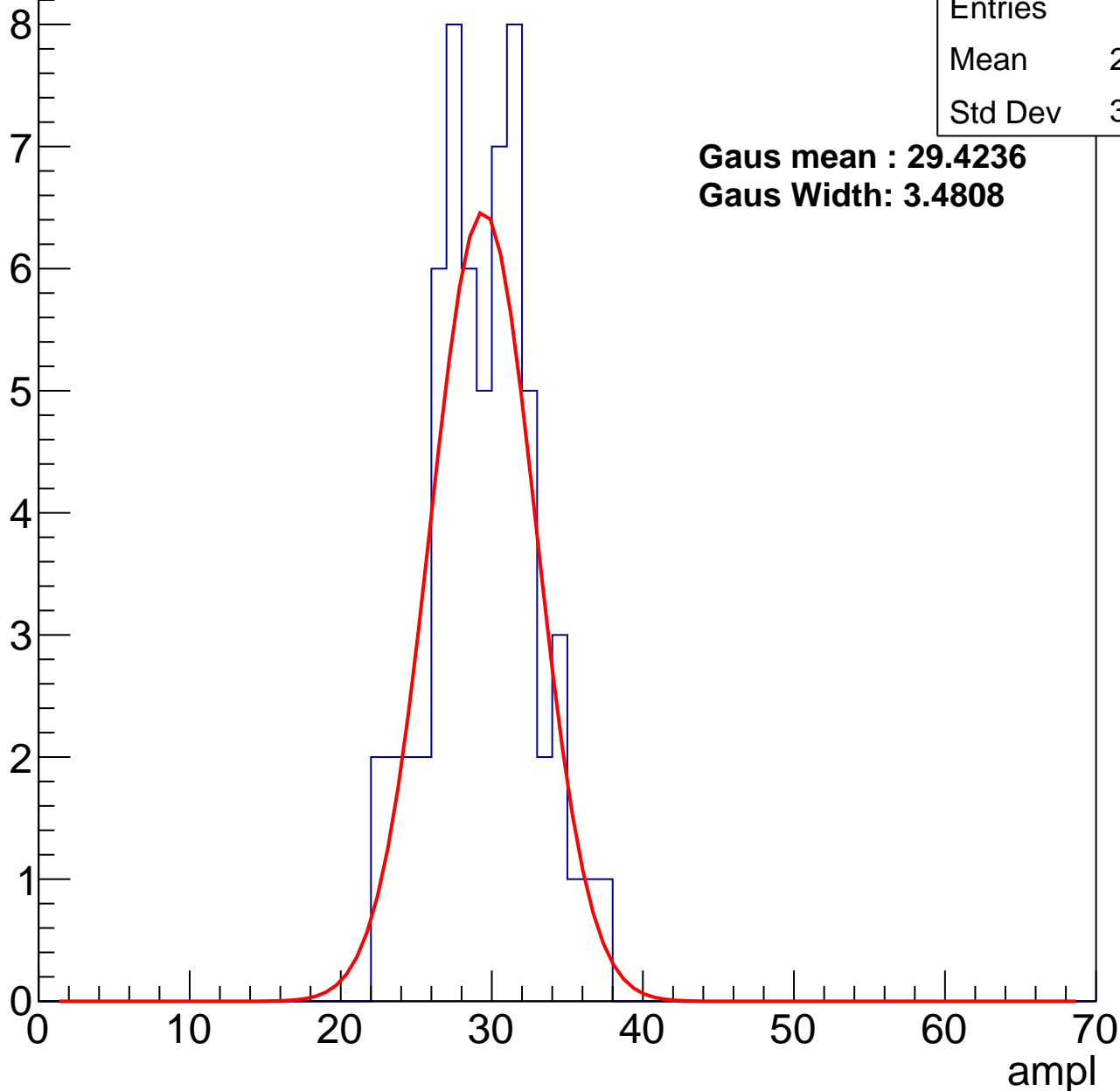
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	28.97
Std Dev	3.348

**Gaus mean : 29.4236**

**Gaus Width: 3.4808**



# B1L101S, U20-ch72, adc1

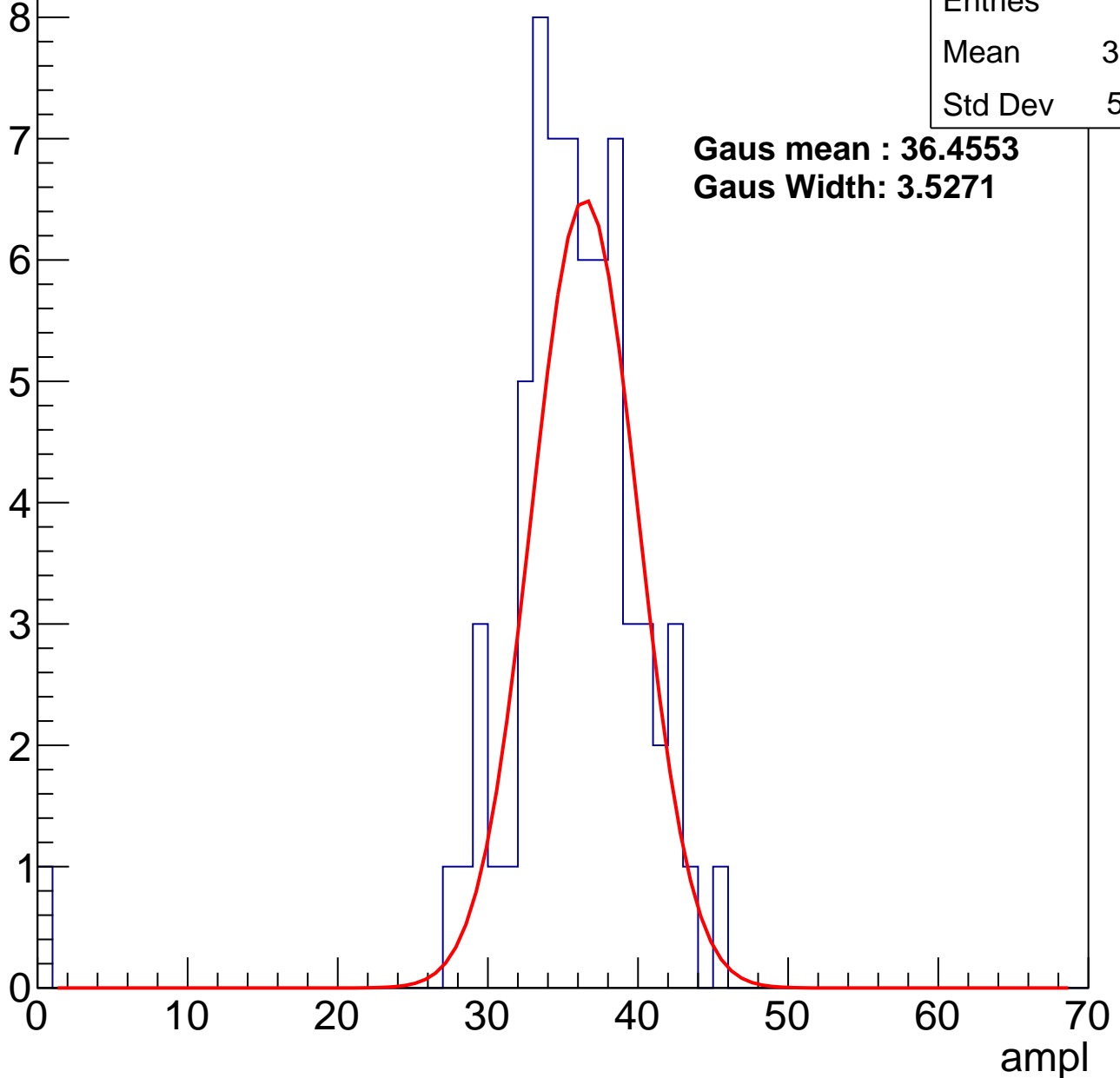
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	67
Mean	35.03
Std Dev	5.691

**Gaus mean : 36.4553**

**Gaus Width: 3.5271**



# B1L101S, U20-ch72, adc2

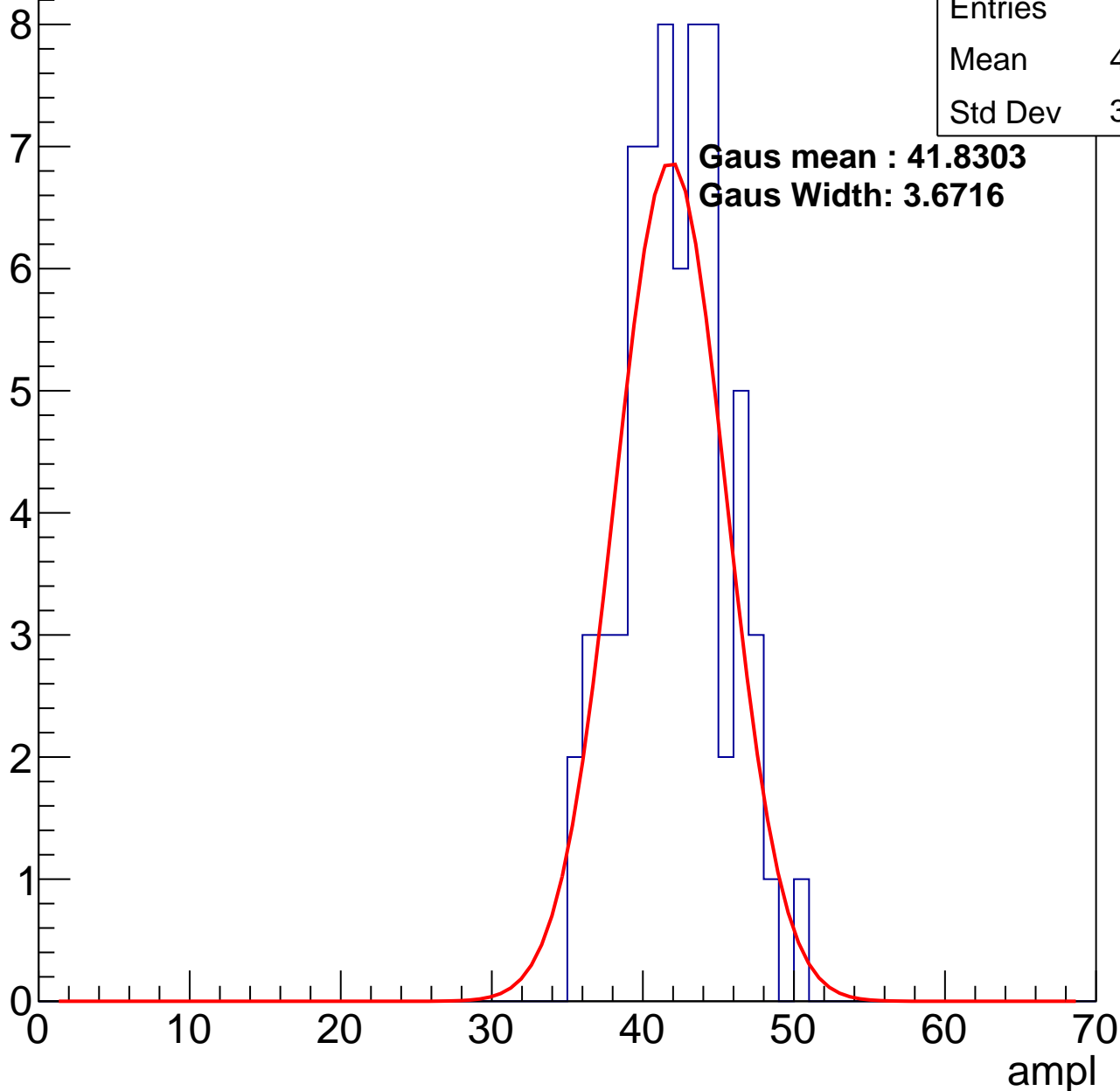
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	67
Mean	41.66
Std Dev	3.308

**Gaus mean : 41.8303**

**Gaus Width: 3.6716**

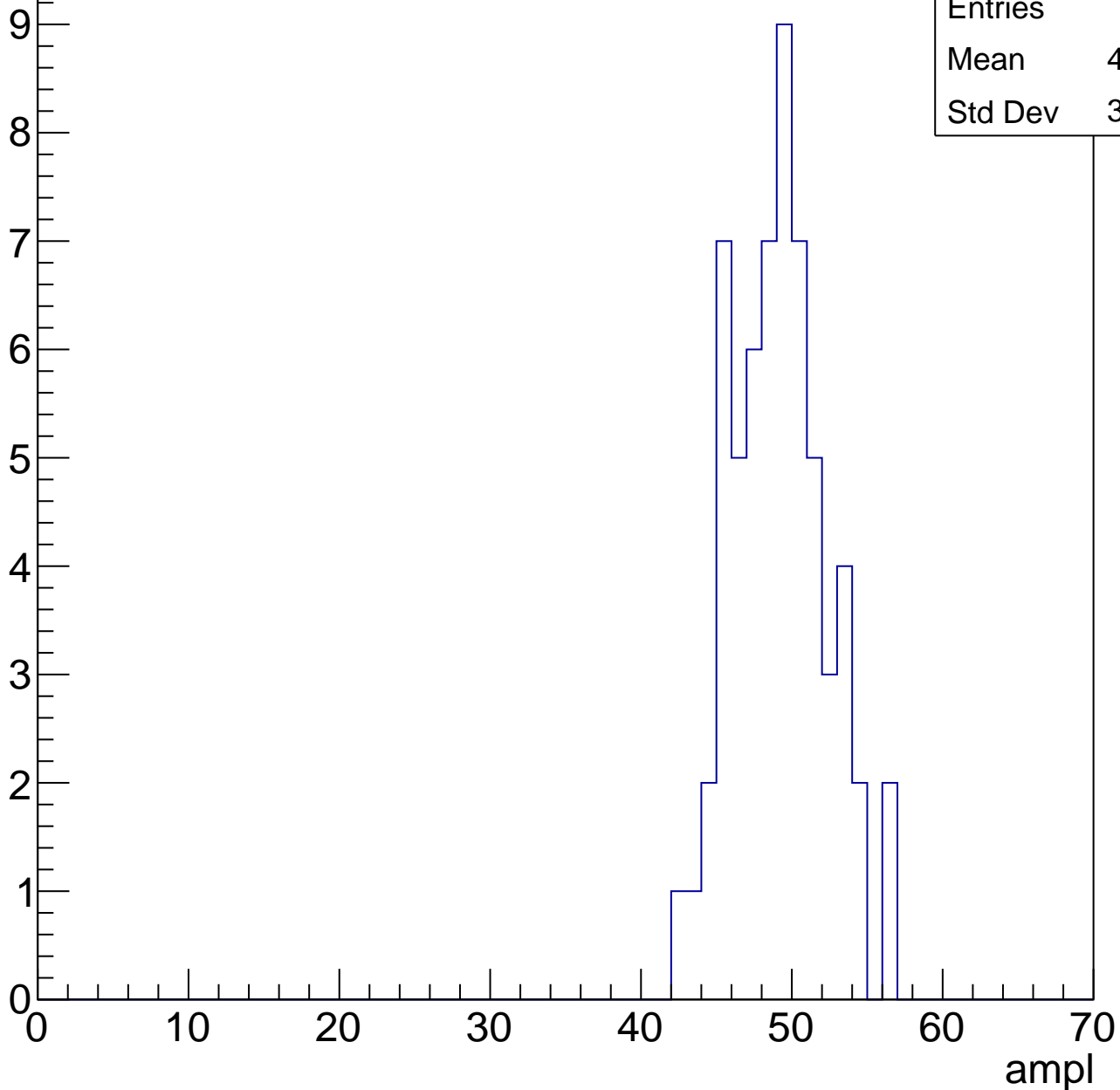


# B1L101S, U20-ch72, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	48.69
Std Dev	3.092

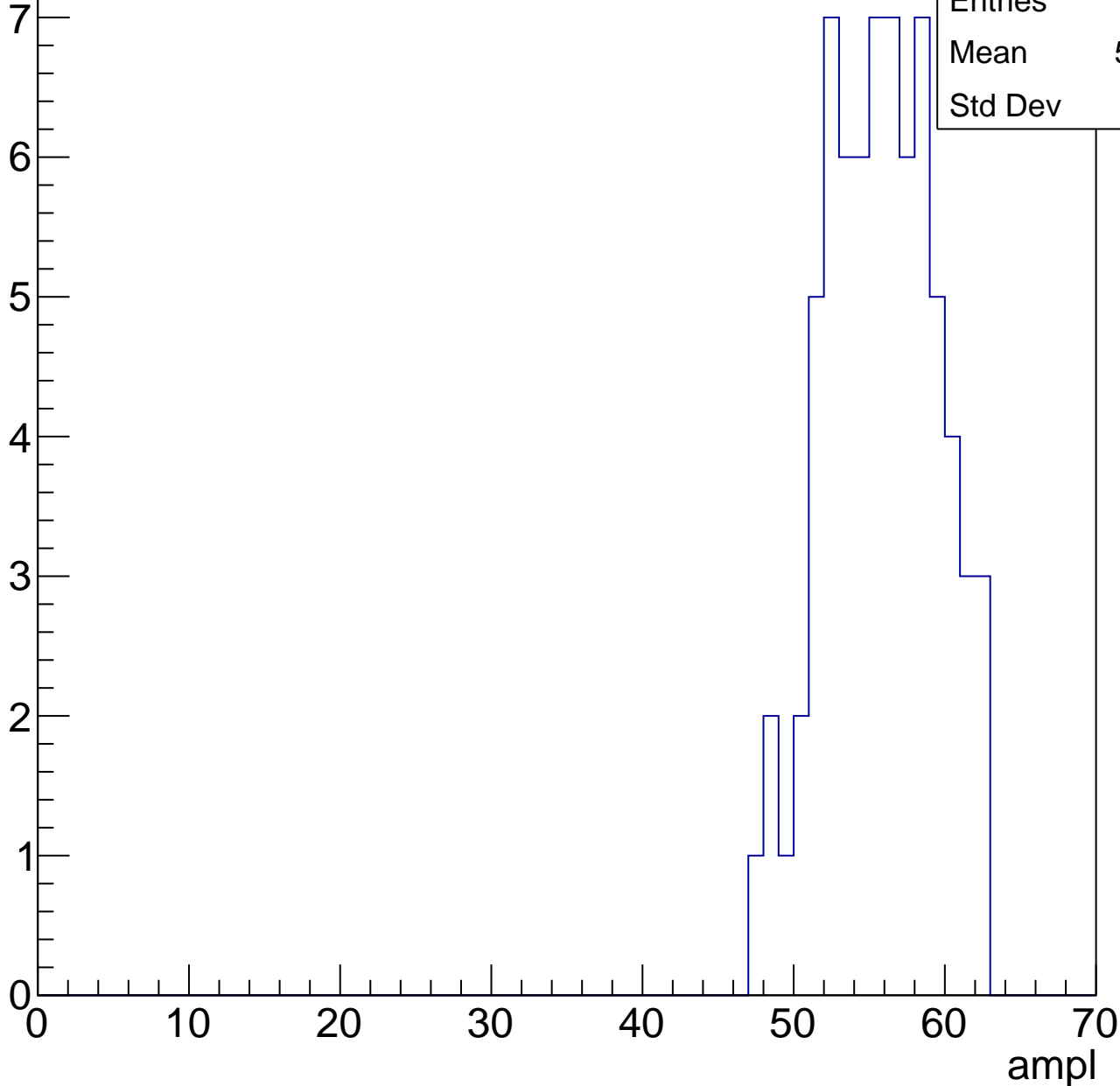


# B1L101S, U20-ch72, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

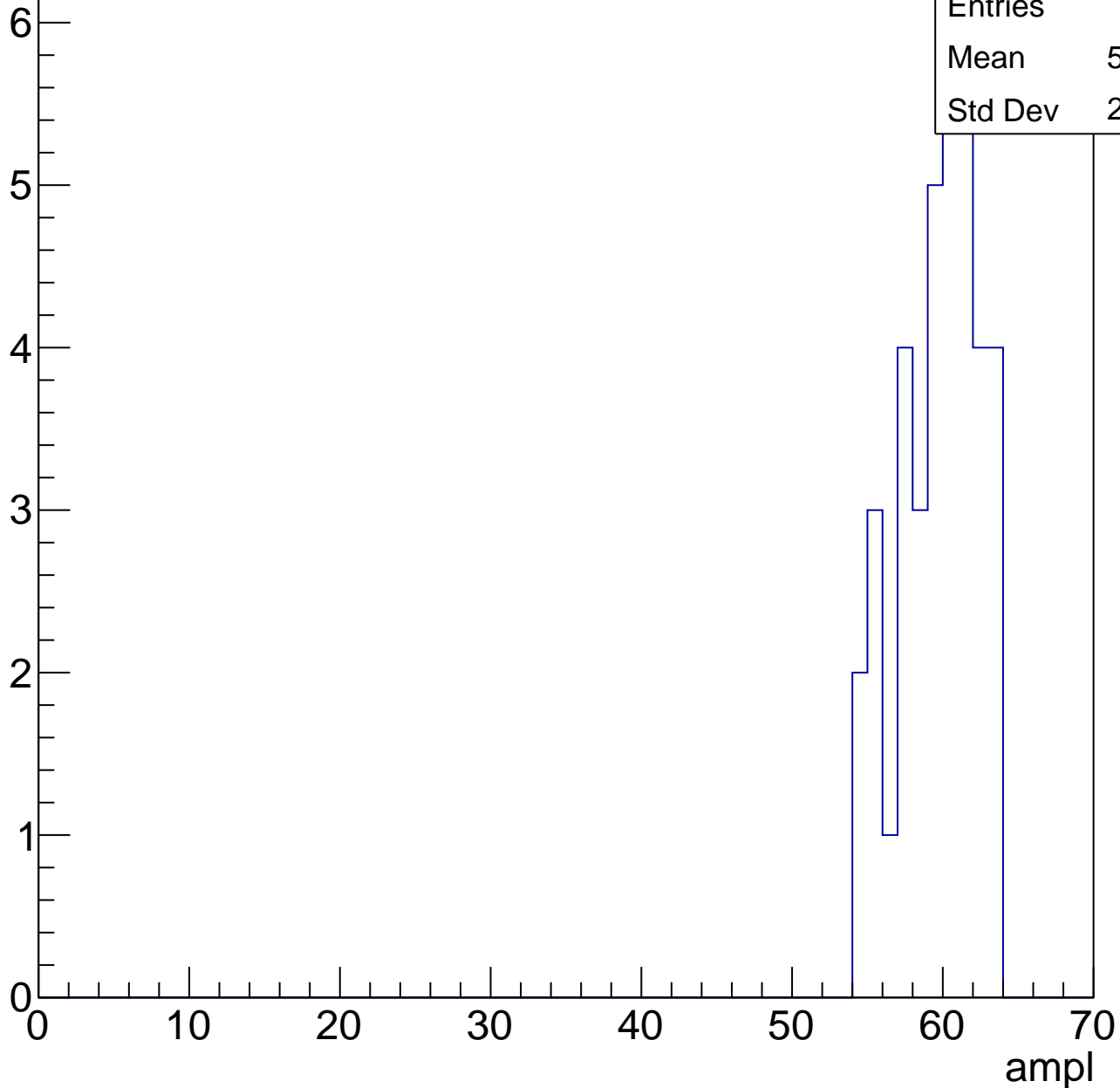
Entries	72
Mean	55.31
Std Dev	3.62



# B1L101S, U20-ch72, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



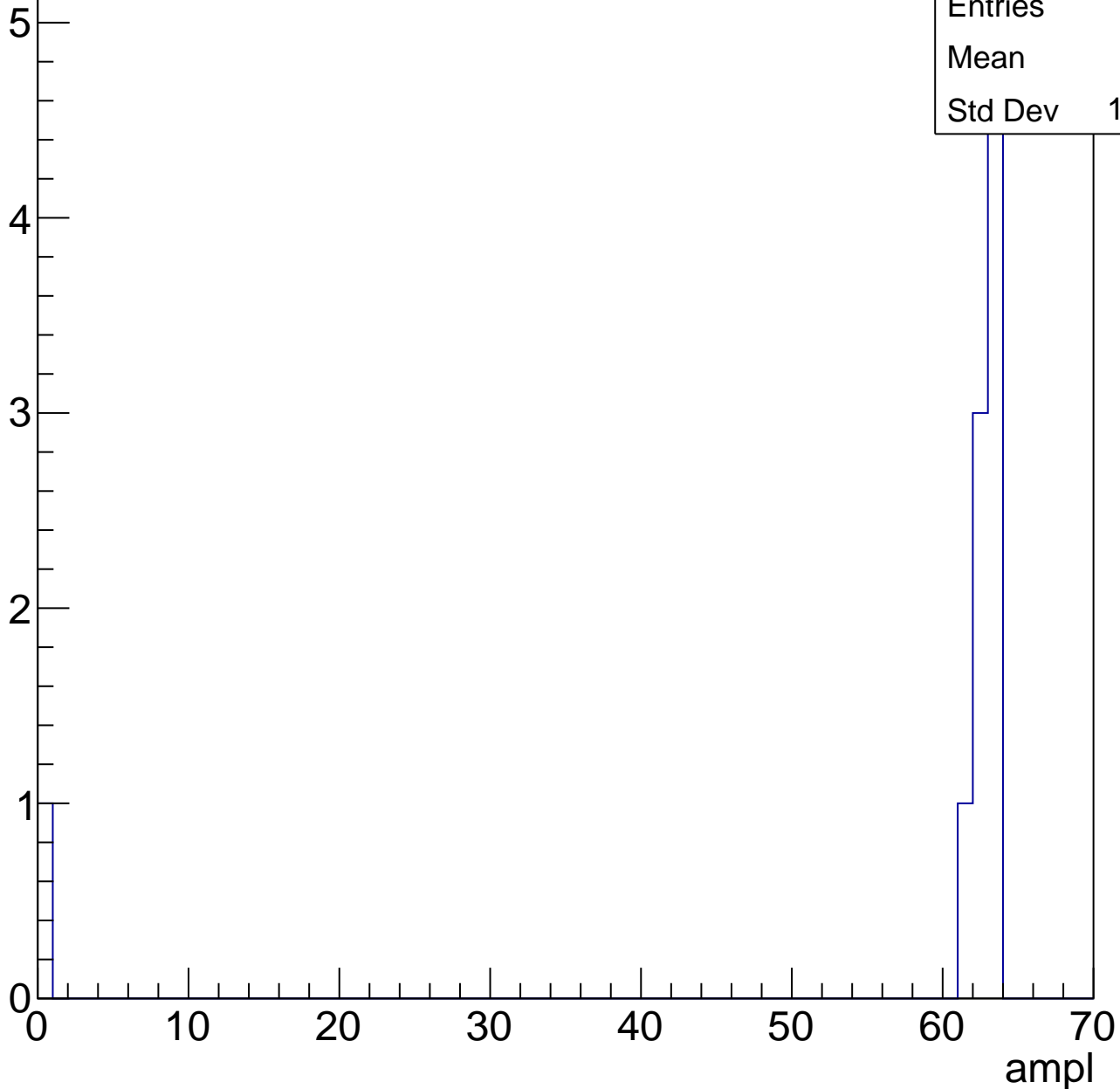
Entries	38
Mean	59.26
Std Dev	2.582

# B1L101S, U20-ch72, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	10
Mean	56.2
Std Dev	18.74





# B1L101S, U20-ch72, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U20-ch73, adc0

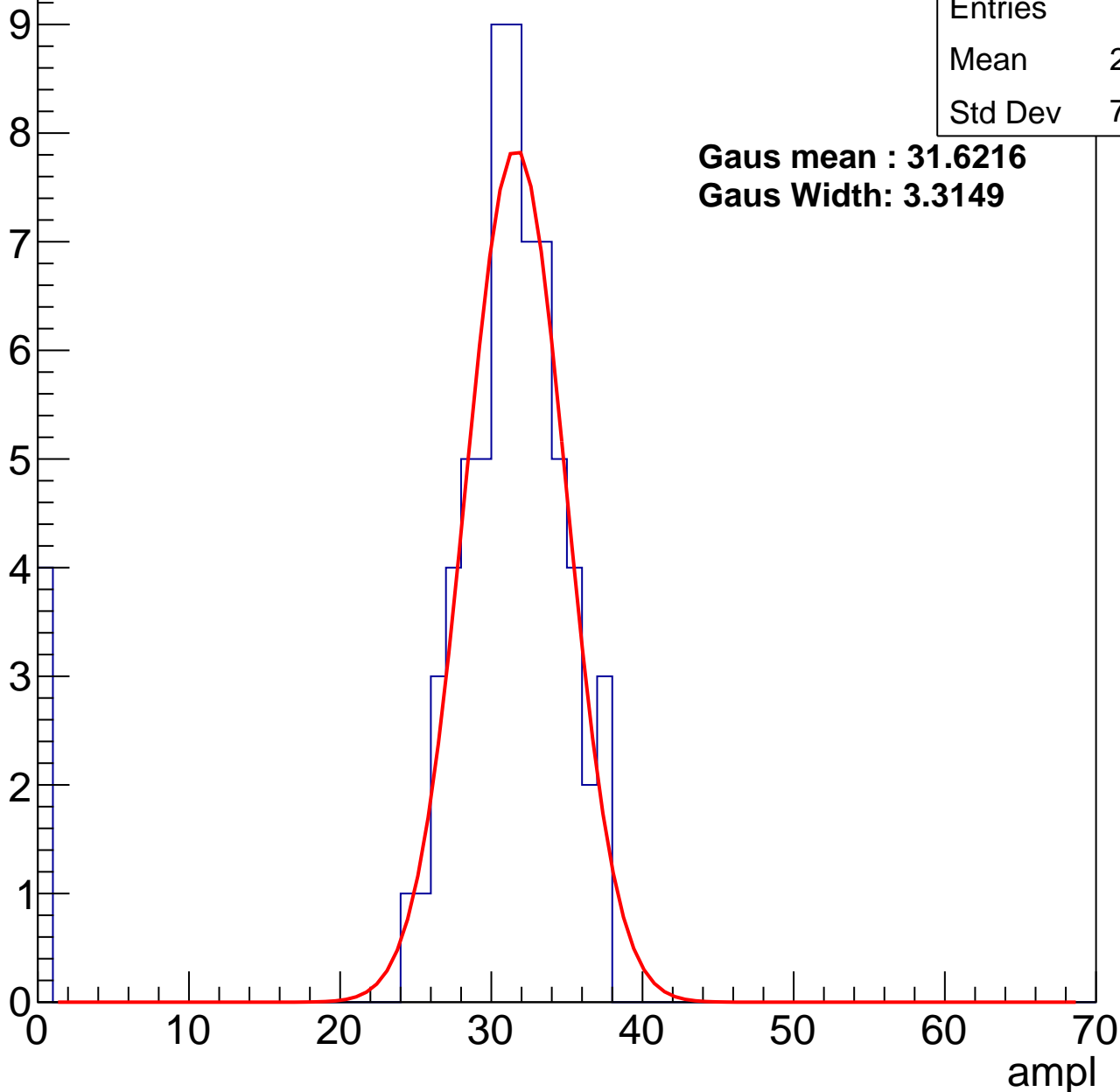
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	29.23
Std Dev	7.828

**Gaus mean : 31.6216**

**Gaus Width: 3.3149**



# B1L101S, U20-ch73, adc1

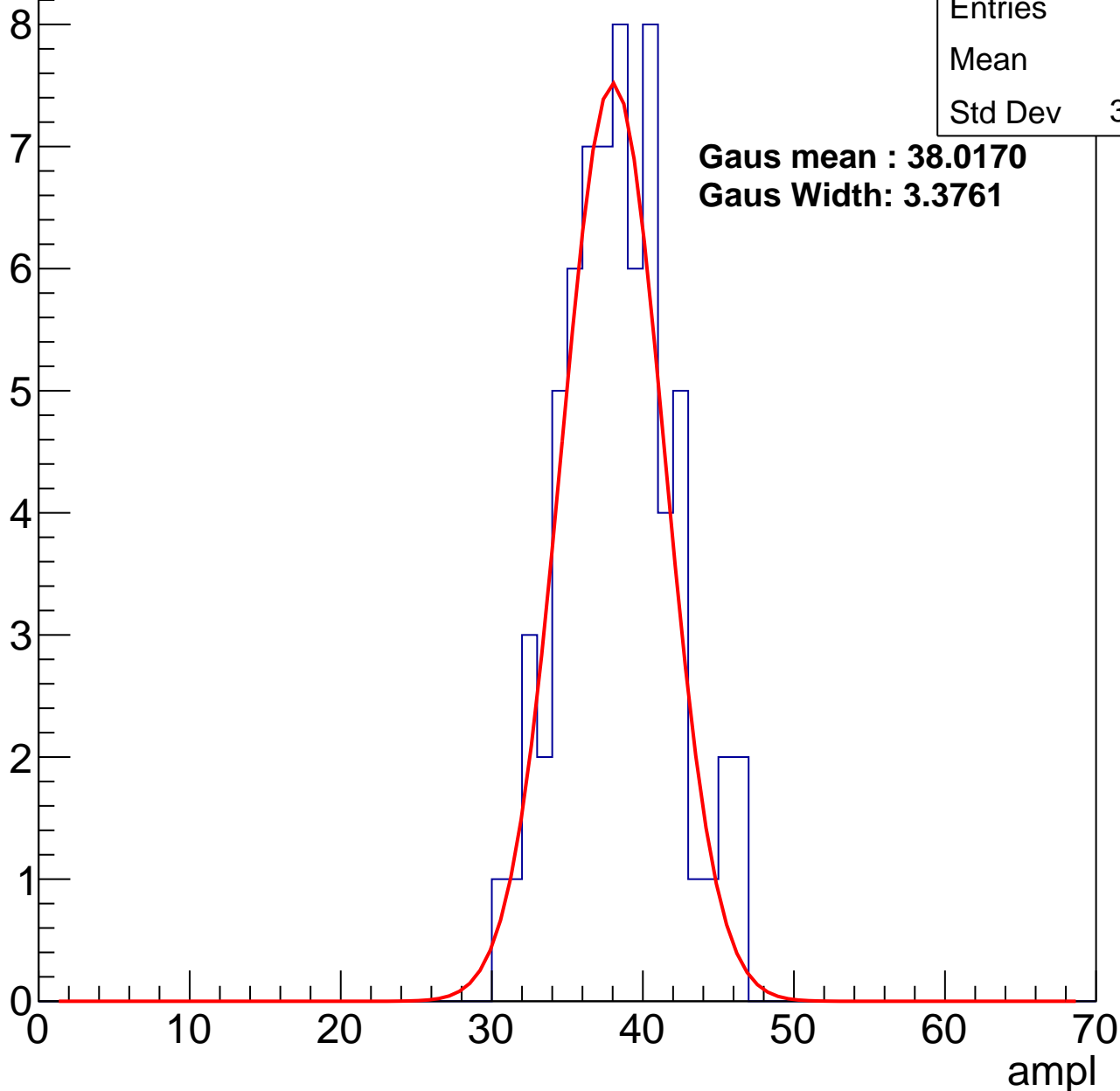
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	37.9
Std Dev	3.572

**Gaus mean : 38.0170**

**Gaus Width: 3.3761**



# B1L101S, U20-ch73, adc2

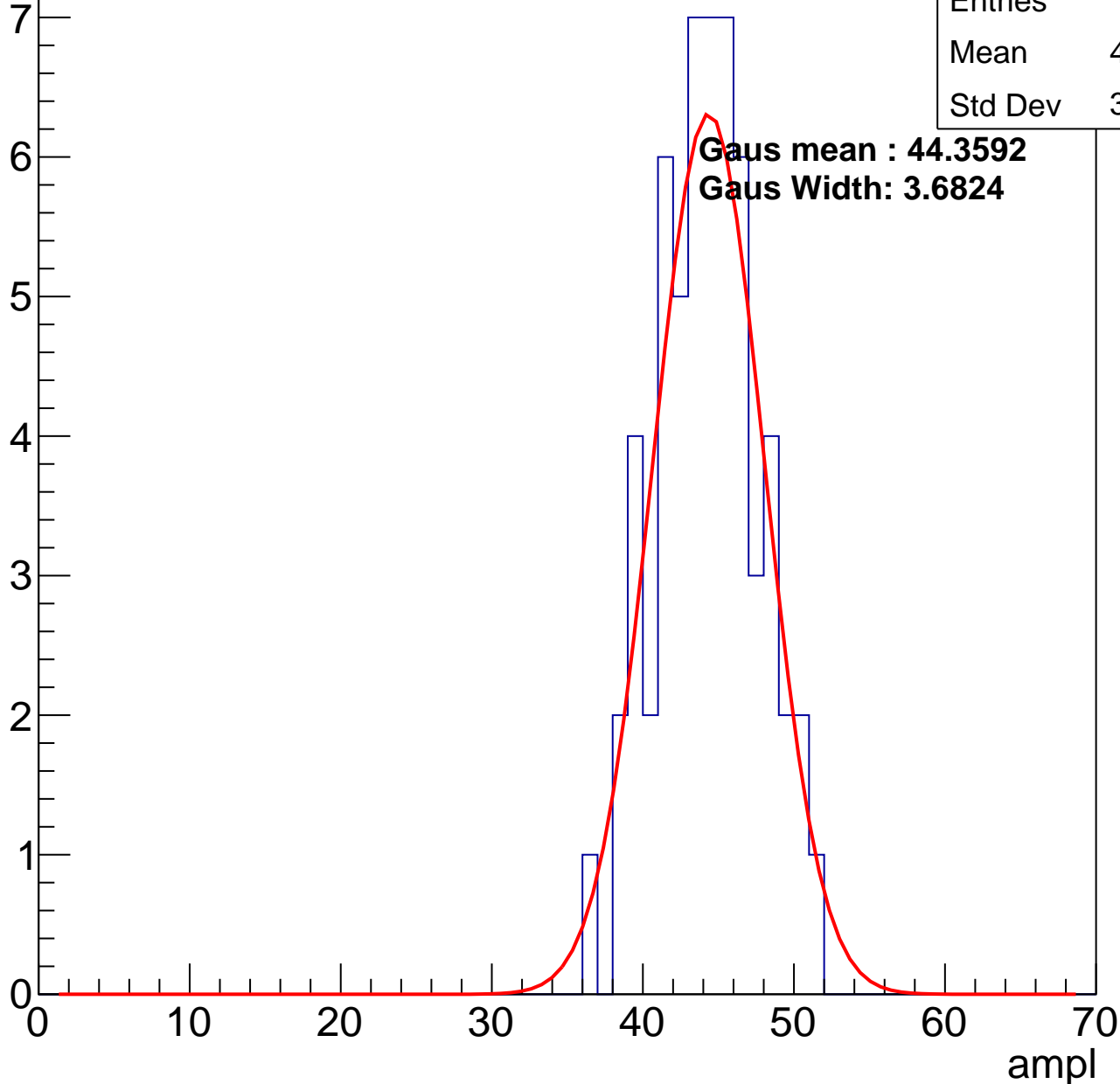
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	59
Mean	43.83
Std Dev	3.294

**Gaus mean : 44.3592**

**Gaus Width: 3.6824**

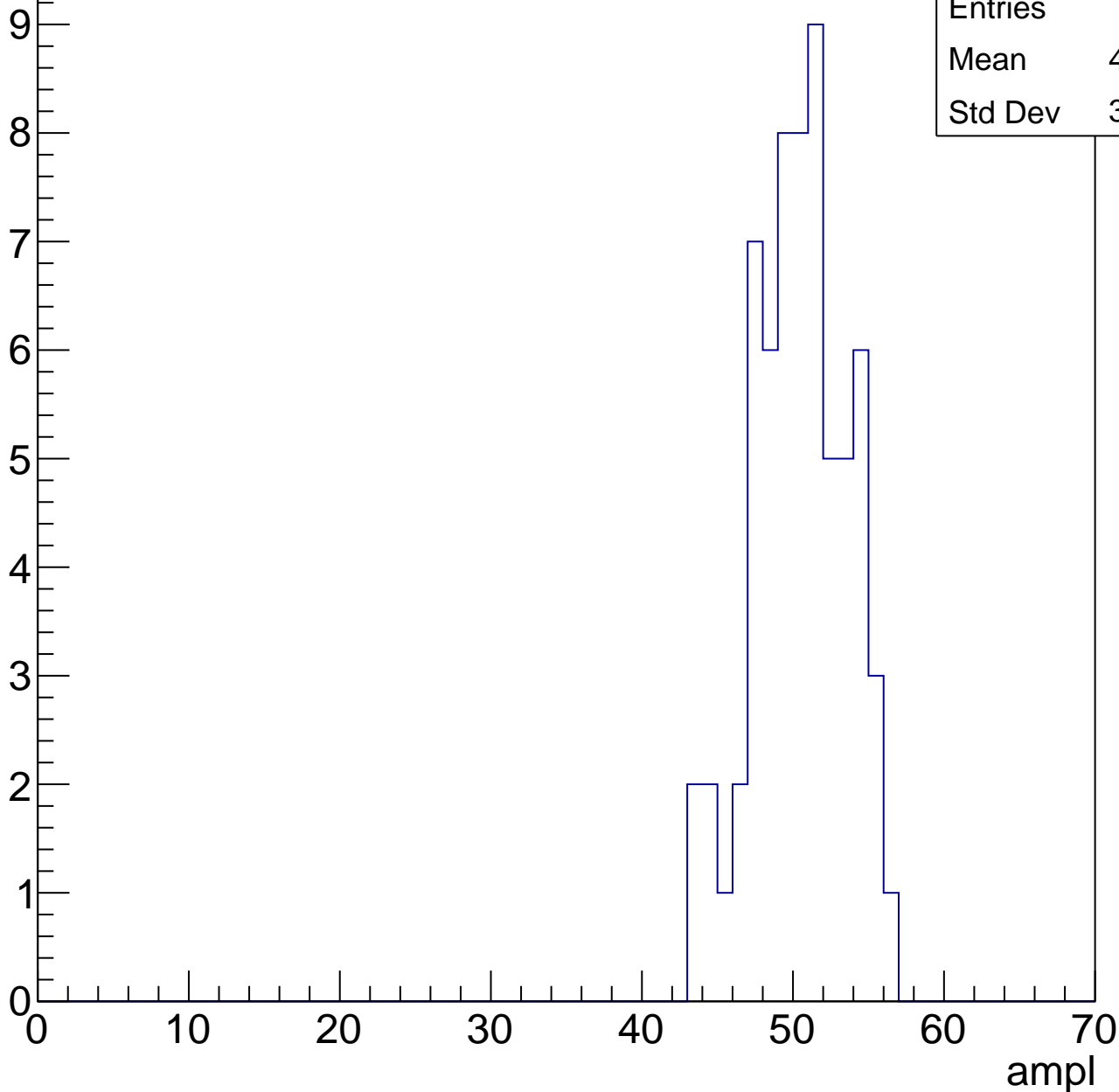


# B1L101S, U20-ch73, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

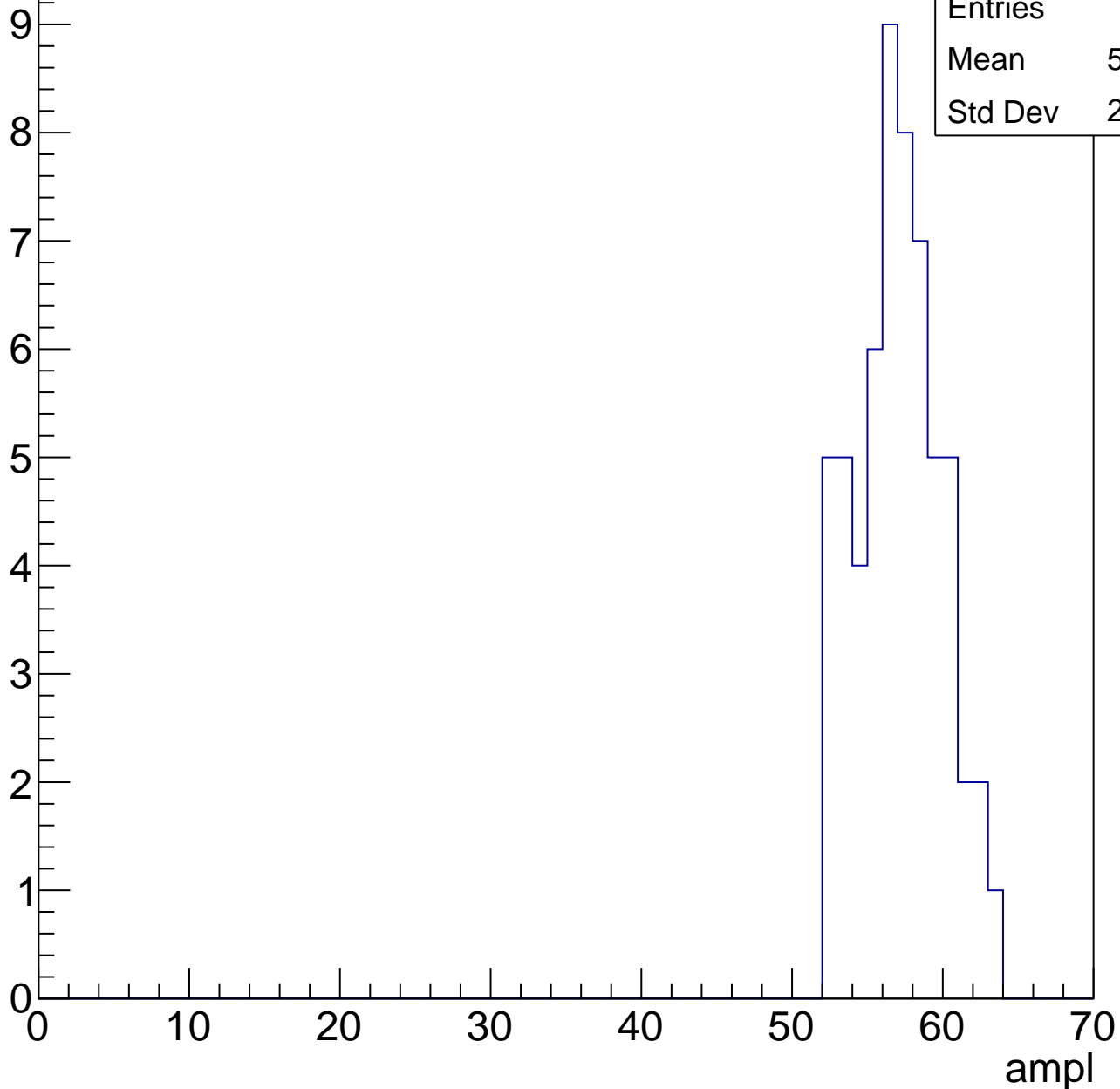
Entries	65
Mean	49.98
Std Dev	3.046



# B1L101S, U20-ch73, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

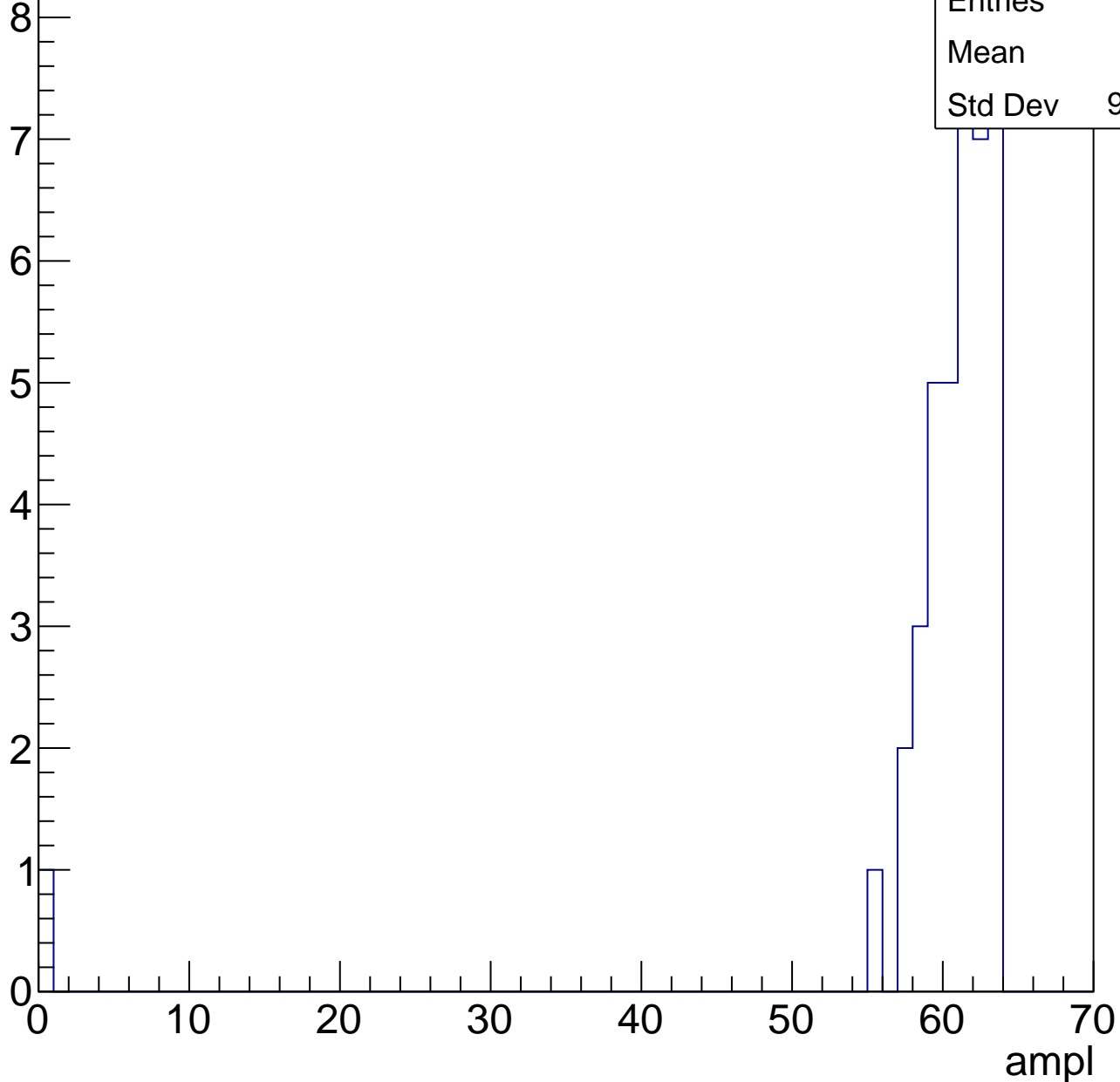


# B1L101S, U20-ch73, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	40
Mean	59.1
Std Dev	9.664



# B1L101S, U20-ch73, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U20-ch73, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U20-ch74, adc0

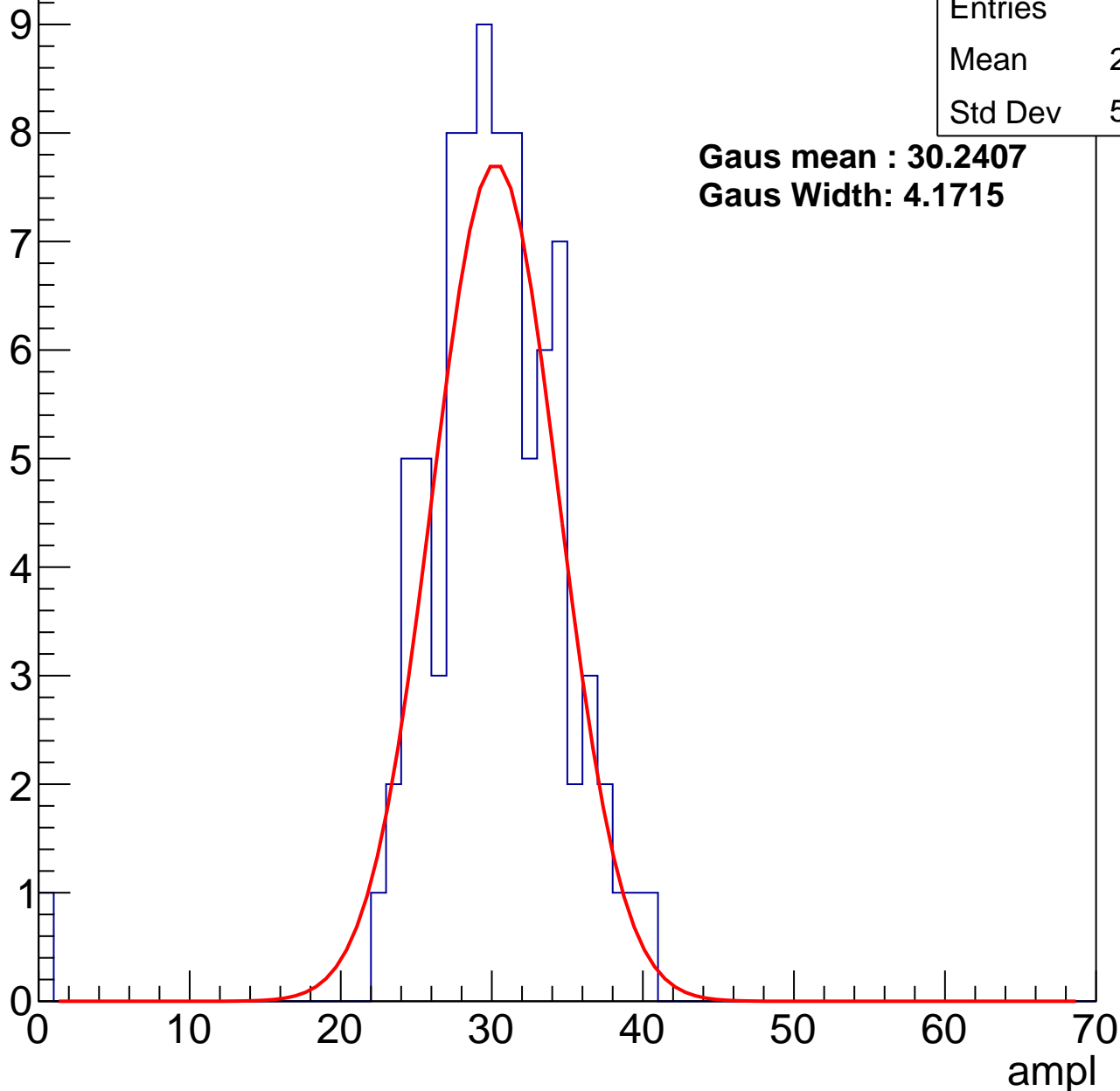
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	86
Mean	29.59
Std Dev	5.068

**Gaus mean : 30.2407**

**Gaus Width: 4.1715**



# B1L101S, U20-ch74, adc1

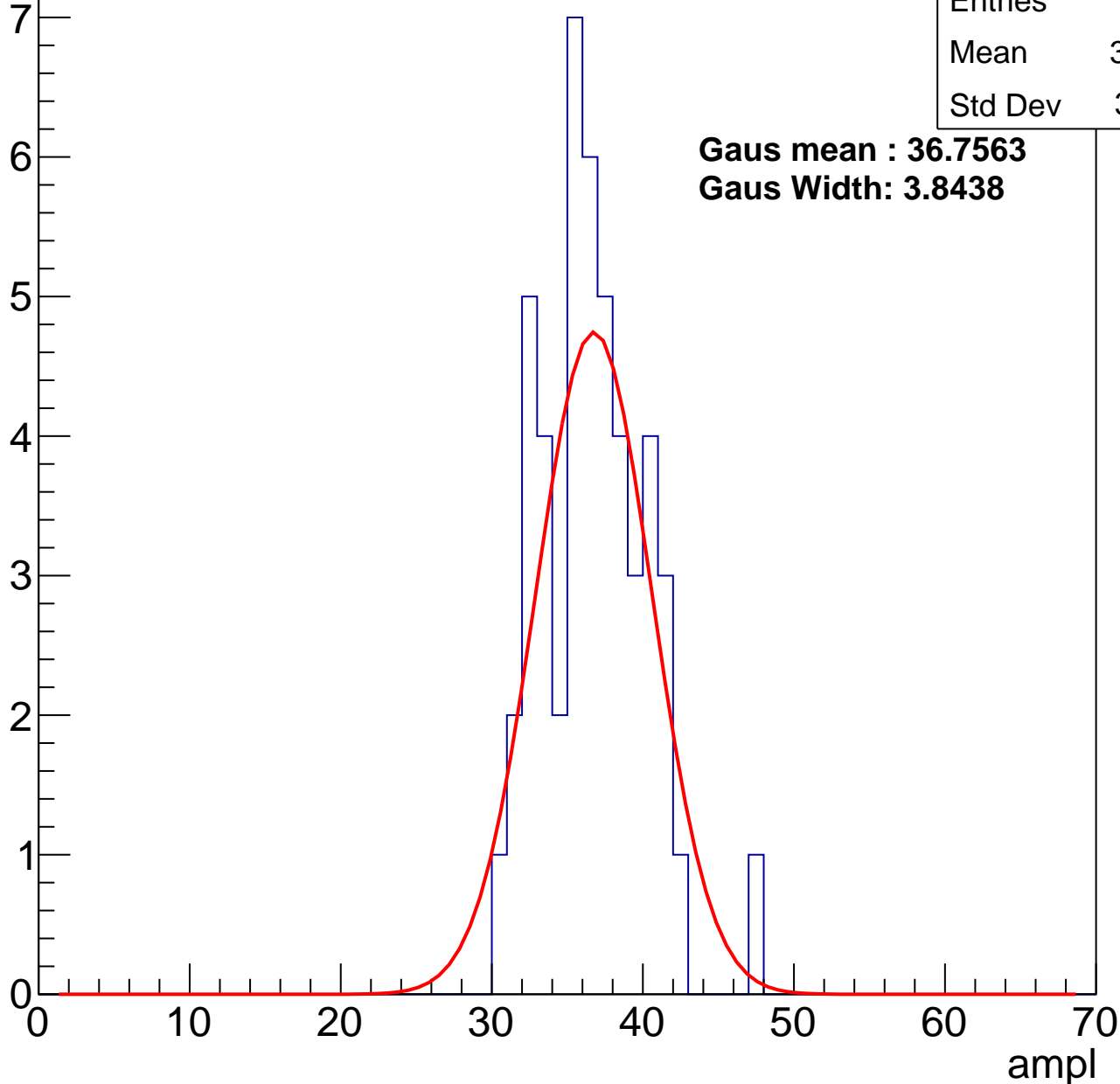
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	48
Mean	36.23
Std Dev	3.411

**Gaus mean : 36.7563**

**Gaus Width: 3.8438**



# B1L101S, U20-ch74, adc2

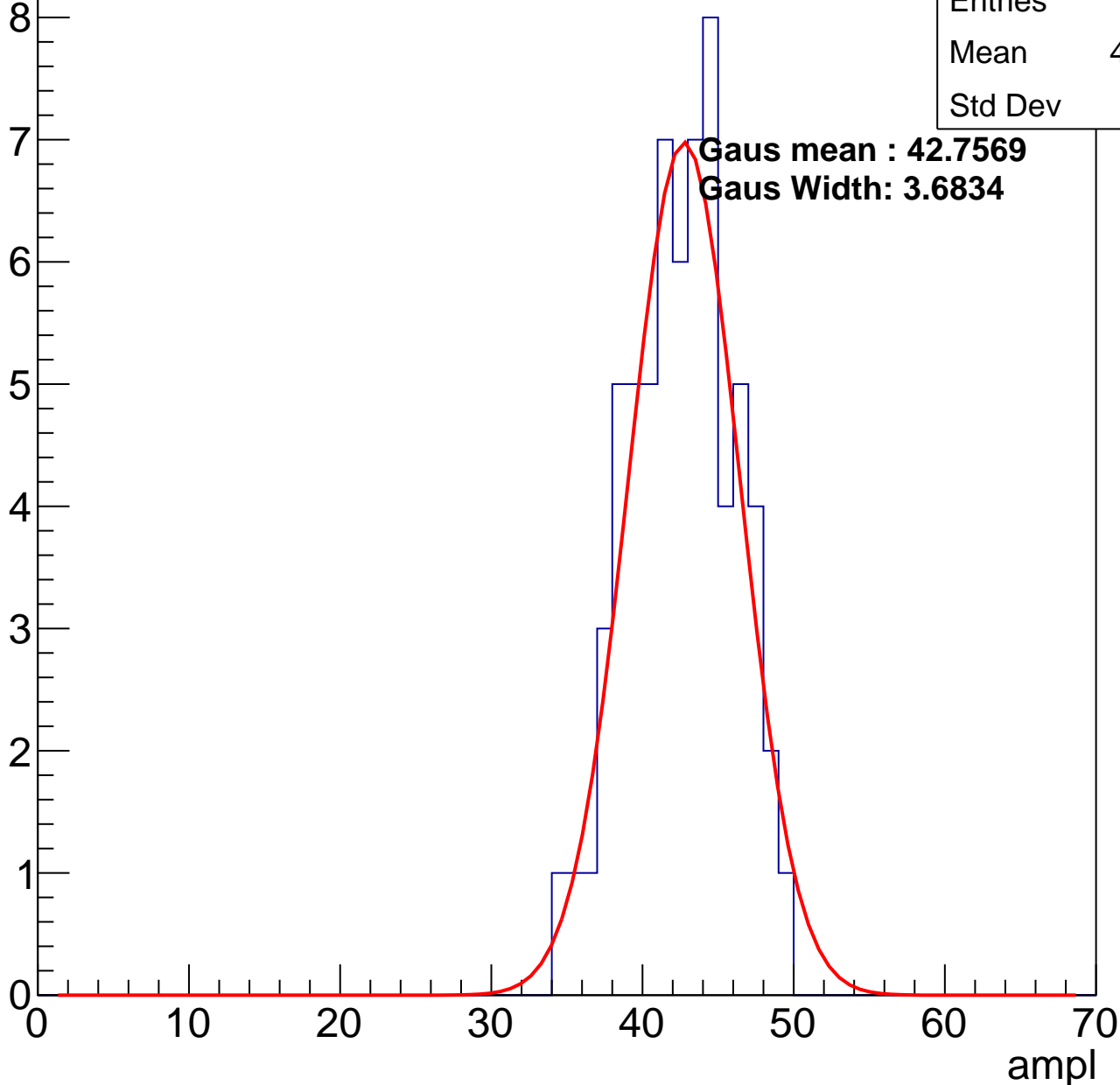
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	42.09
Std Dev	3.4

**Gaus mean : 42.7569**

**Gaus Width: 3.6834**

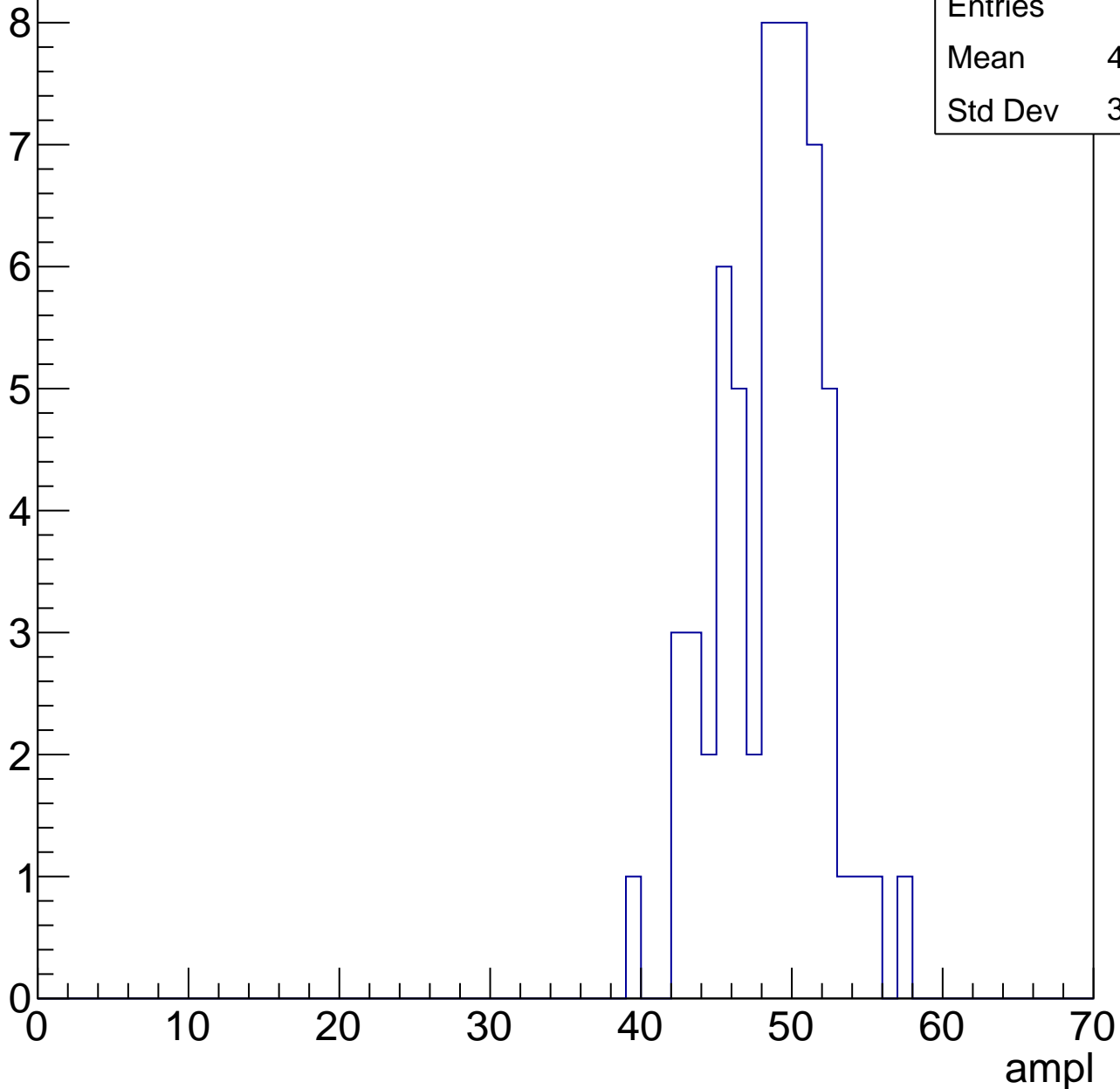


# B1L101S, U20-ch74, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	48.19
Std Dev	3.463

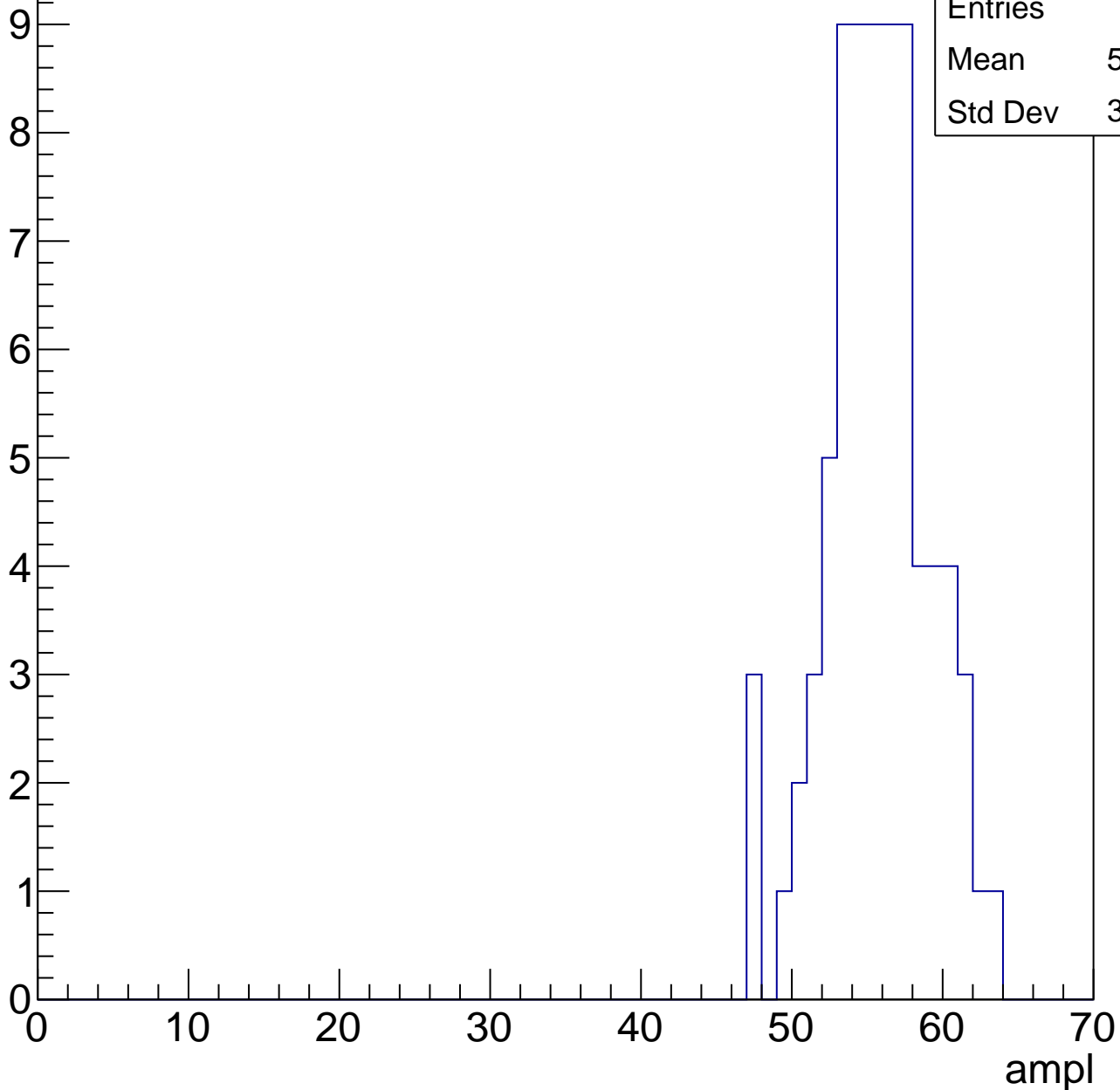


# B1L101S, U20-ch74, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	76
Mean	55.18
Std Dev	3.402

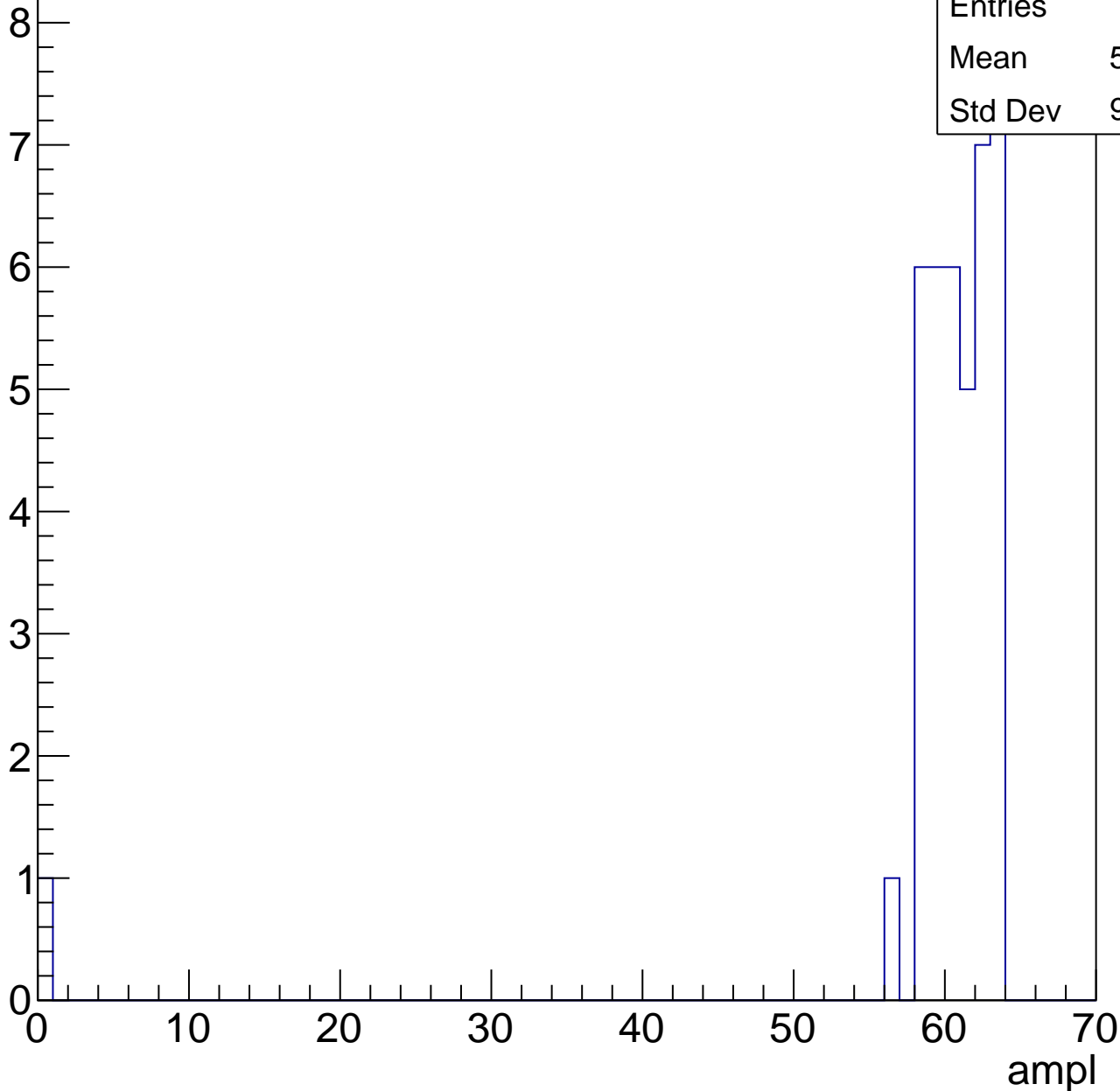


# B1L101S, U20-ch74, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	40
Mean	59.02
Std Dev	9.635



# B1L101S, U20-ch74, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

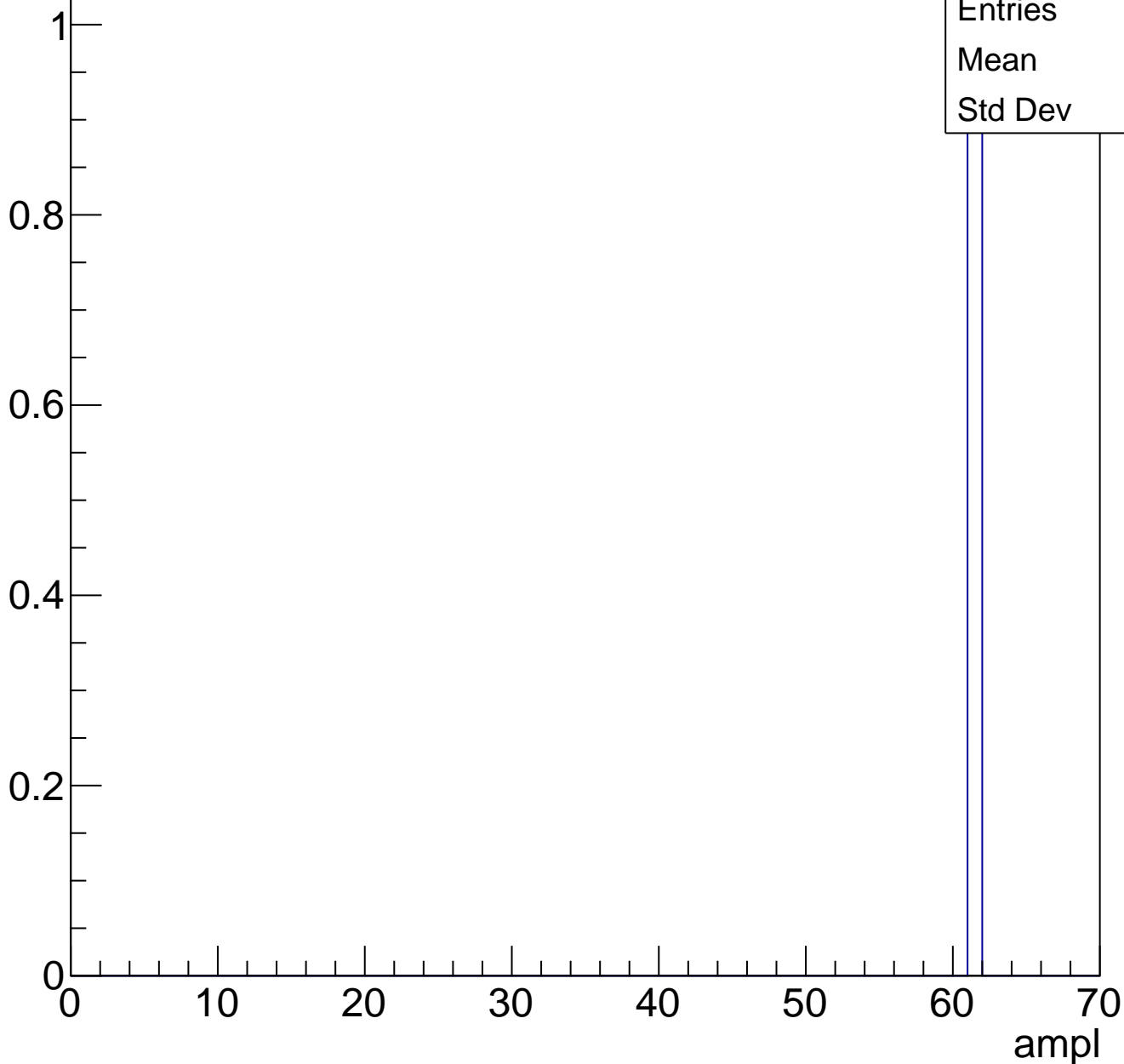




# B1L101S, U20-ch74, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U20-ch75, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	79
Mean	31.53
Std Dev	3.617

**Gaus mean : 32.4423**

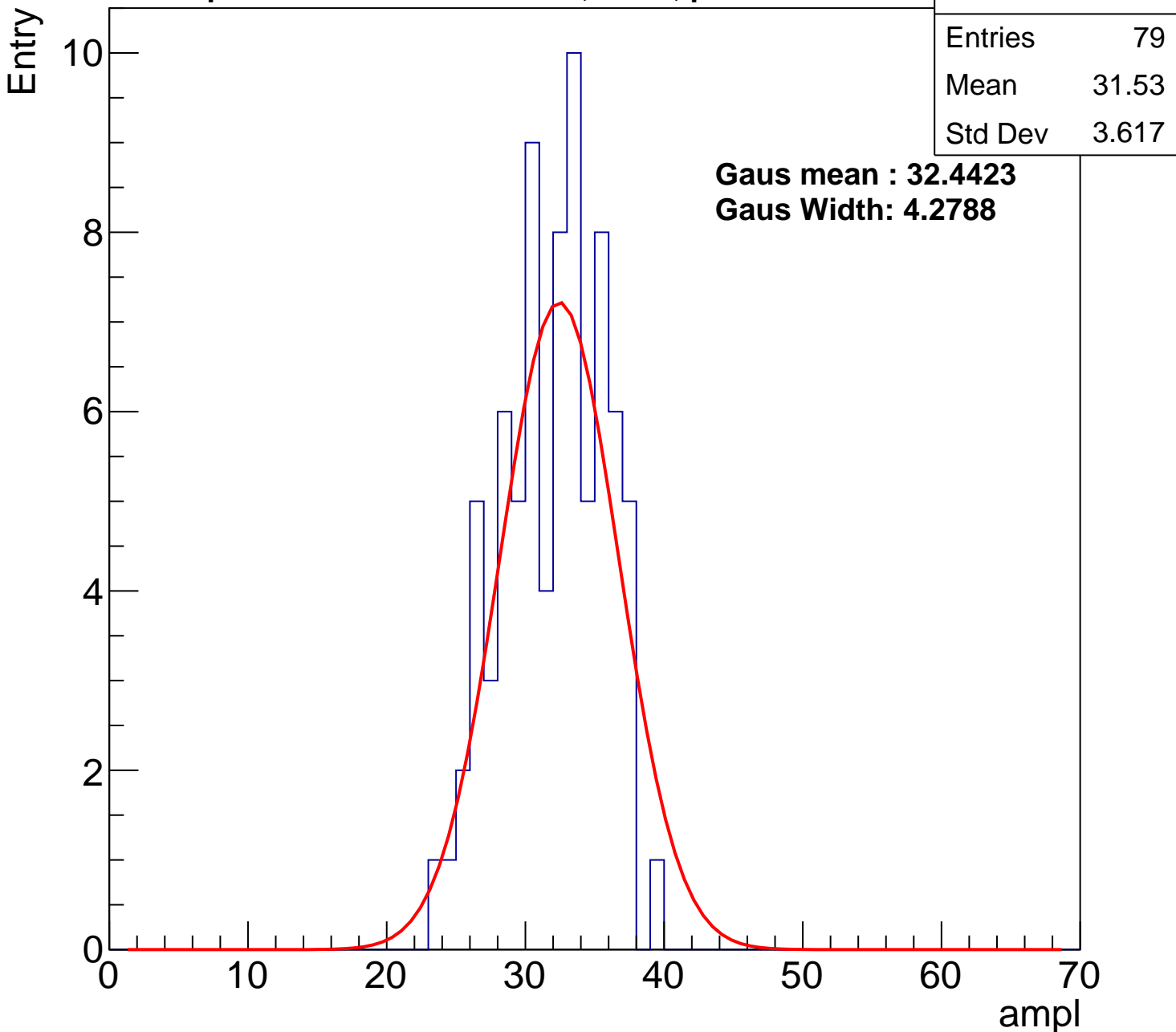
**Gaus Width: 4.2788**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U20-ch75, adc1

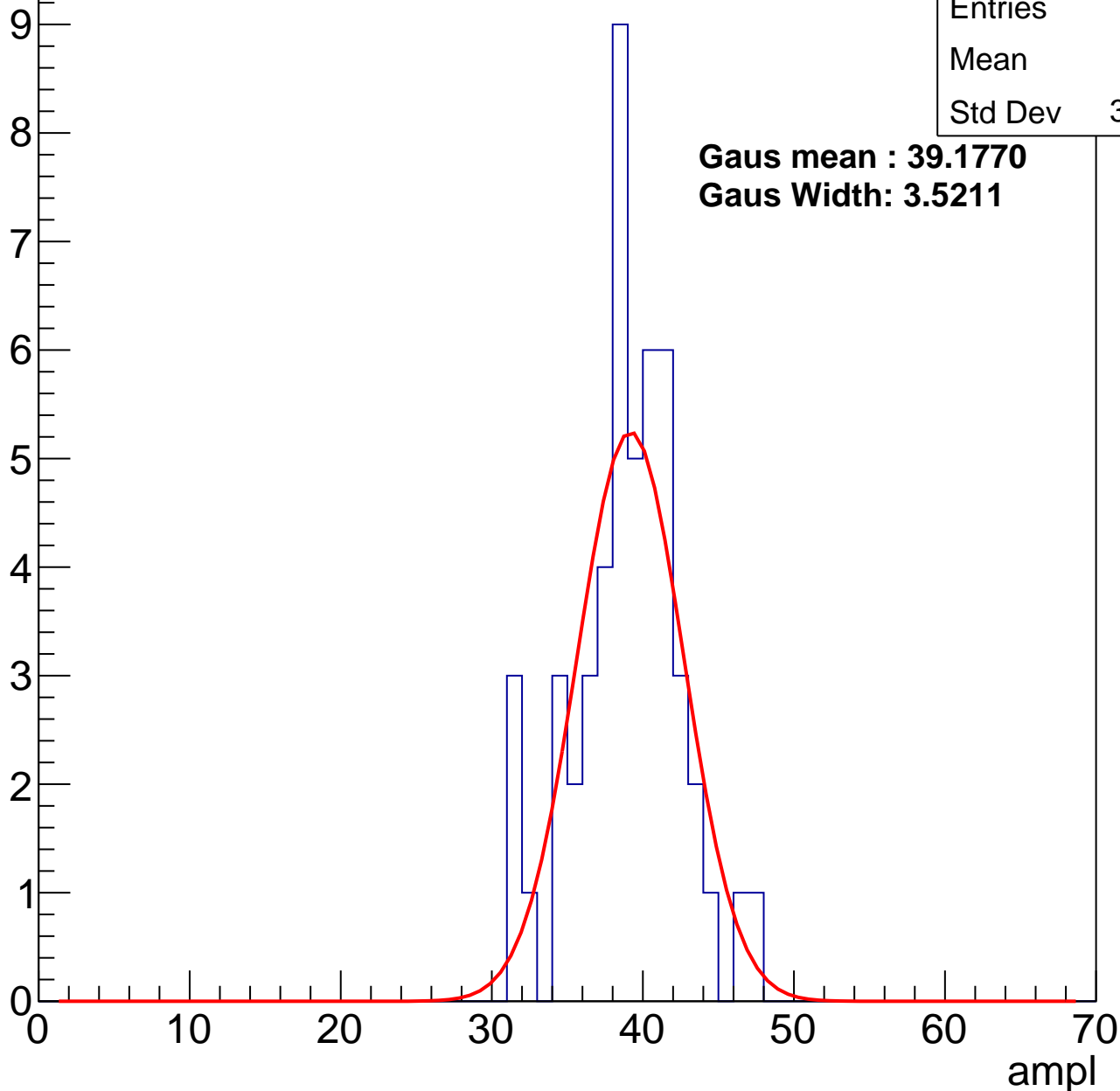
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	50
Mean	38.5
Std Dev	3.506

**Gaus mean : 39.1770**

**Gaus Width: 3.5211**

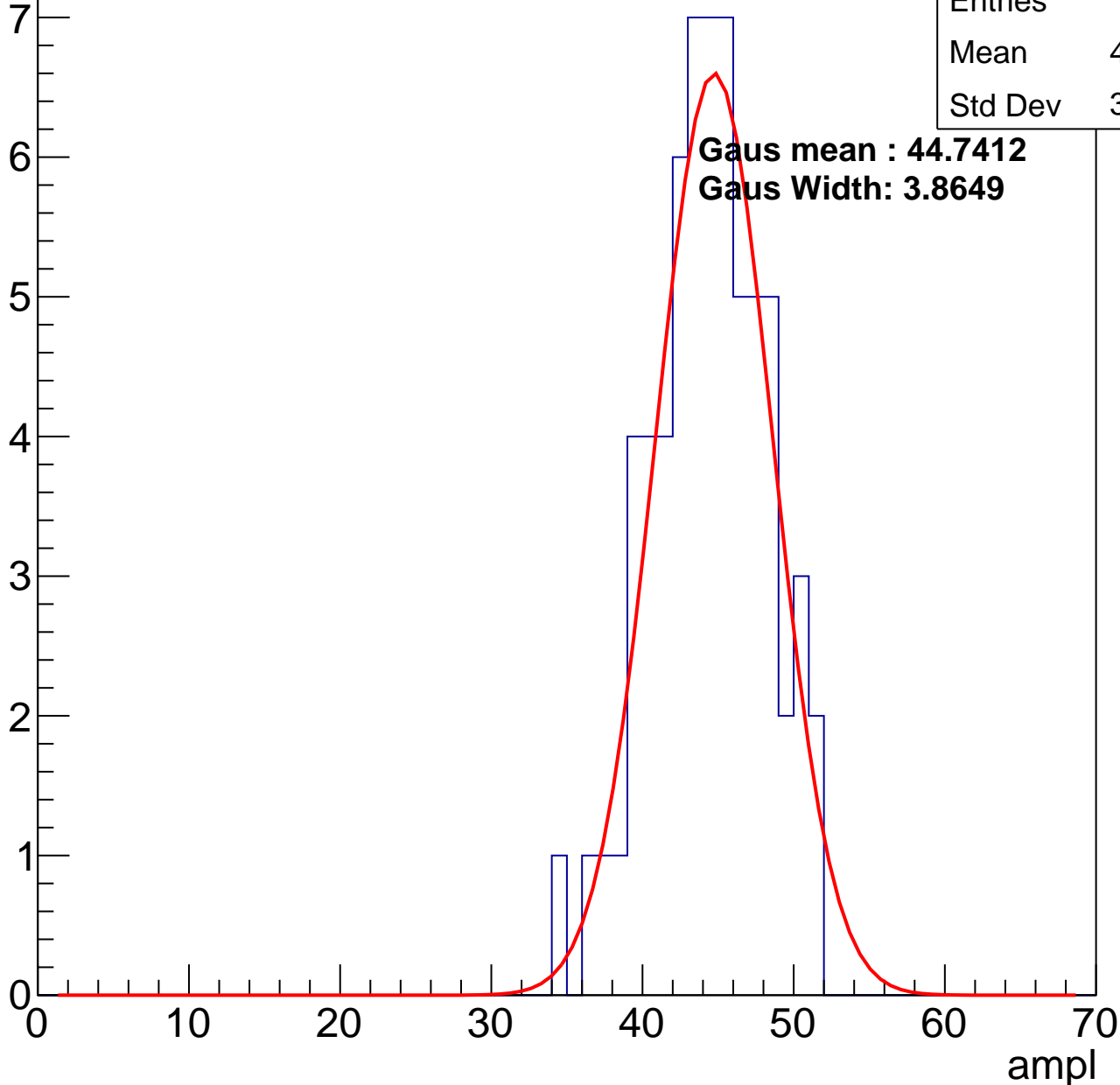


# B1L101S, U20-ch75, adc2

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	43.94
Std Dev	3.696

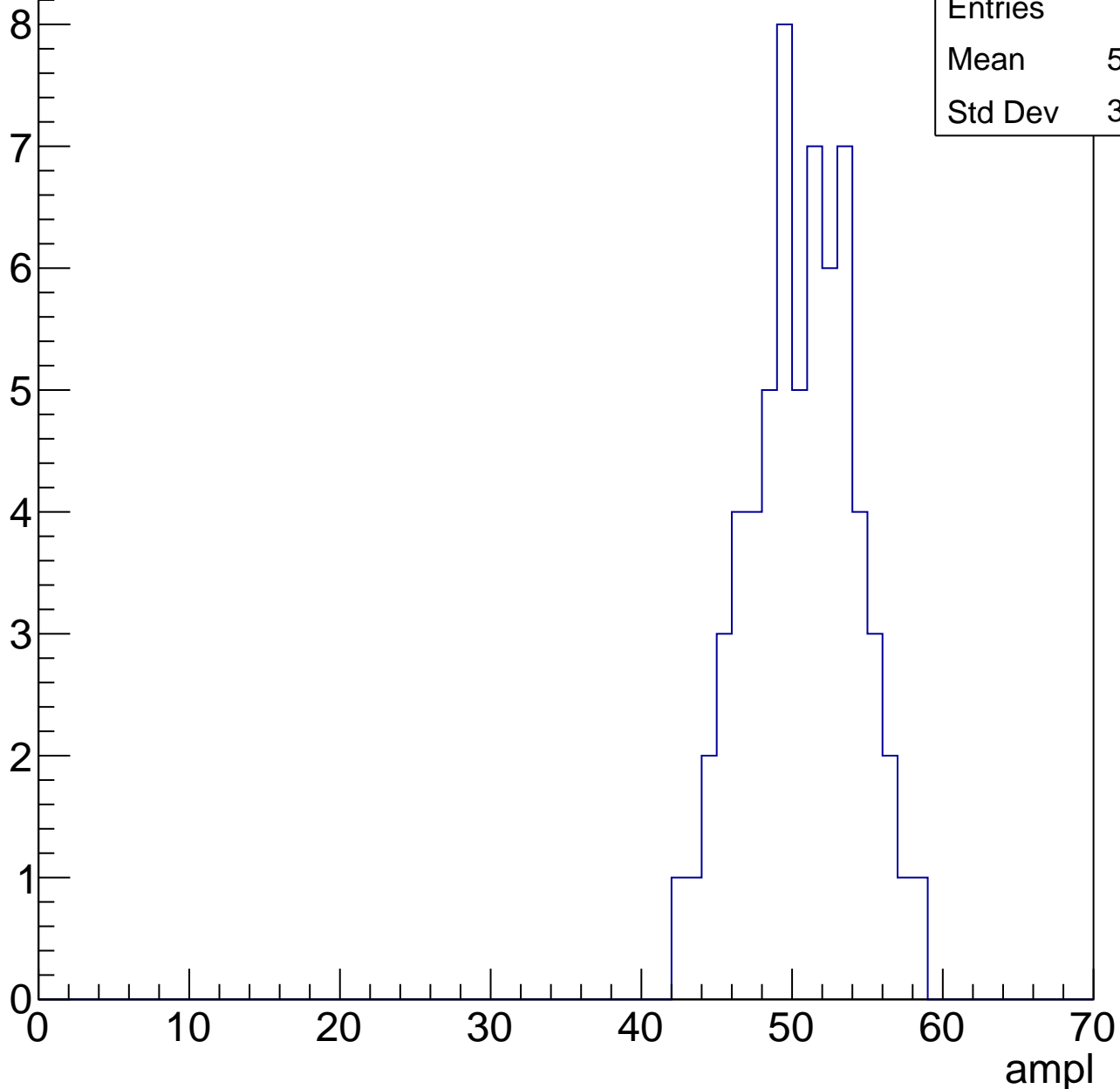


# B1L101S, U20-ch75, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	50.16
Std Dev	3.545

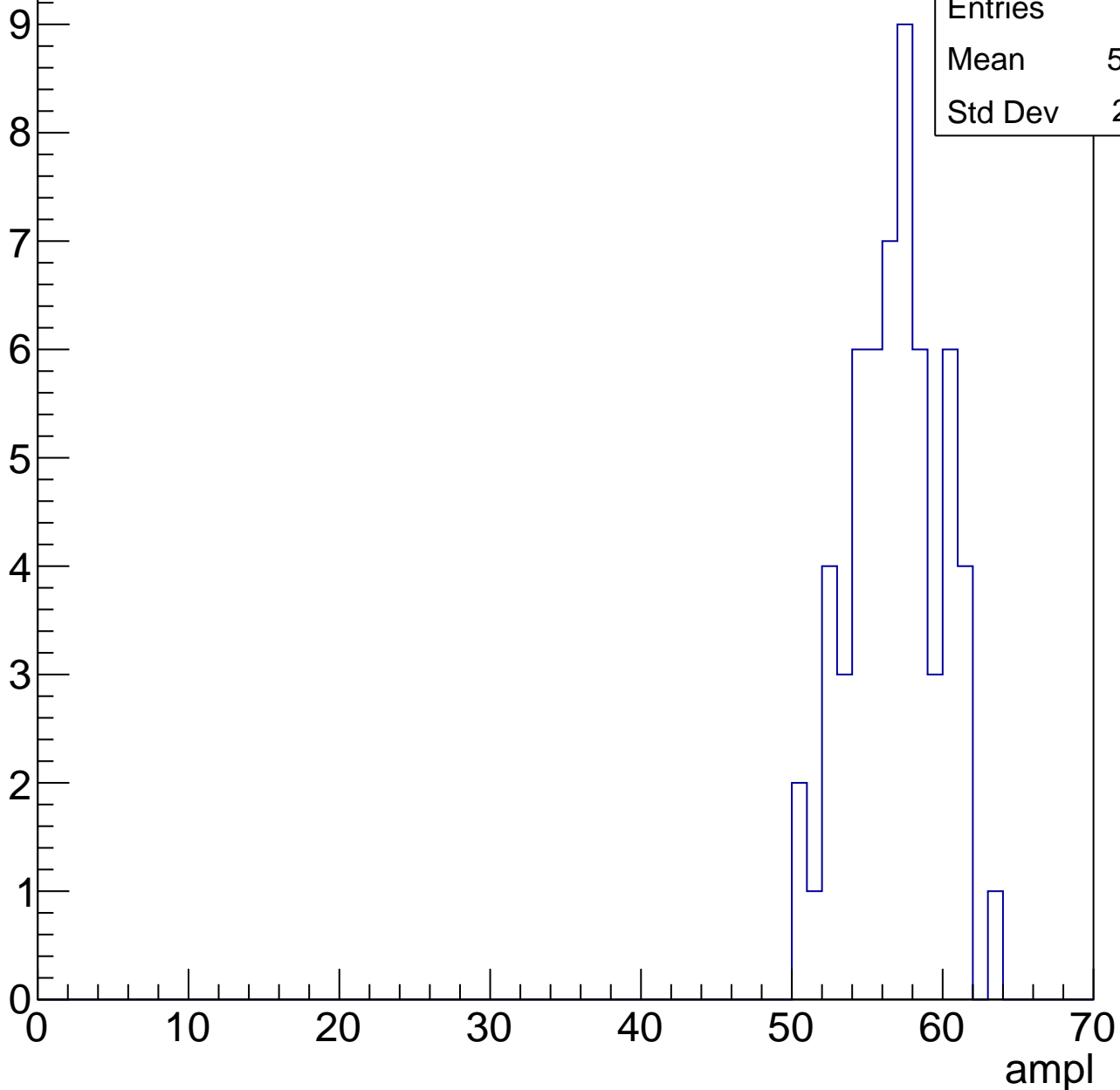


# B1L101S, U20-ch75, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	58
Mean	56.36
Std Dev	2.981

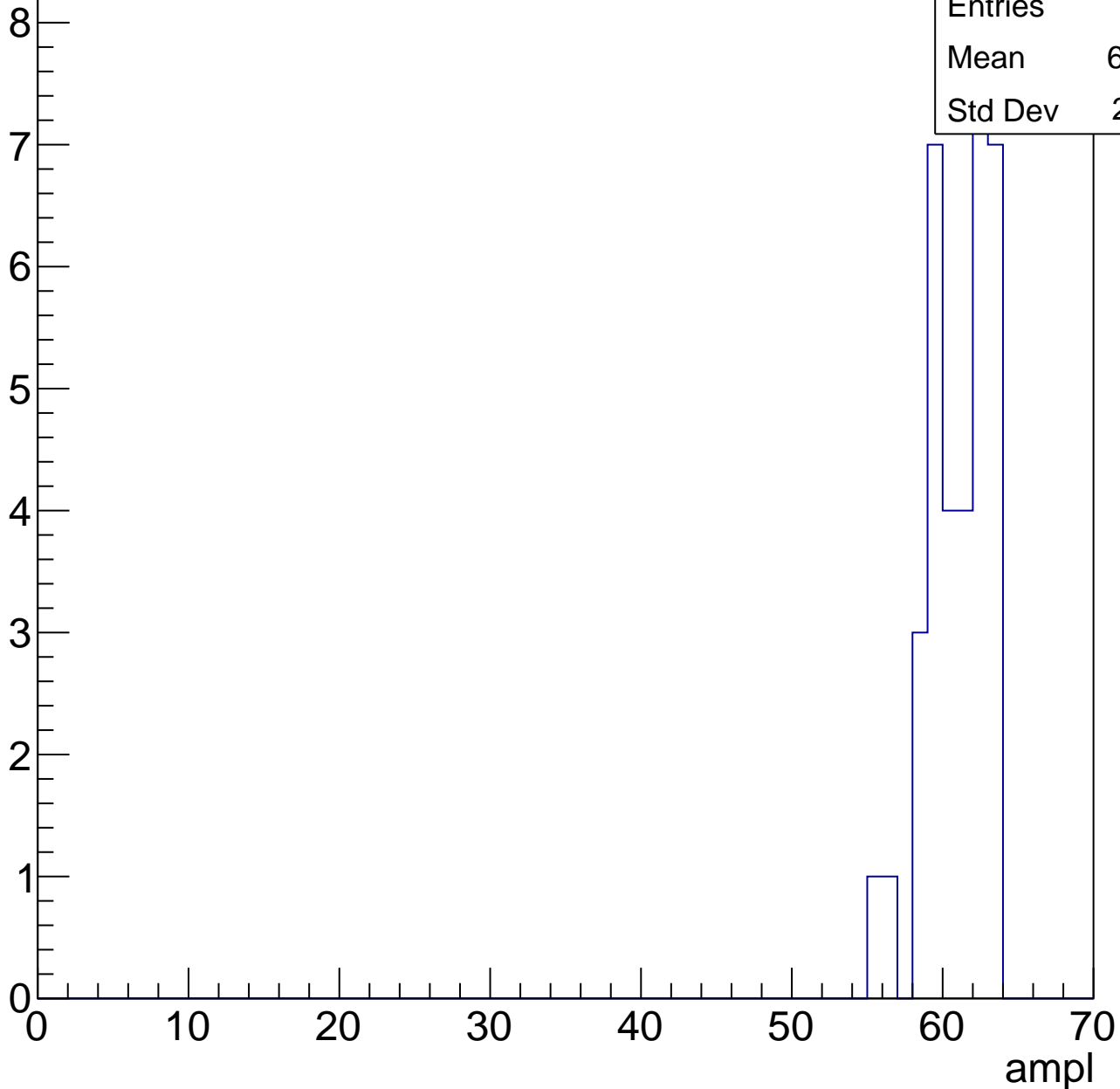


# B1L101S, U20-ch75, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

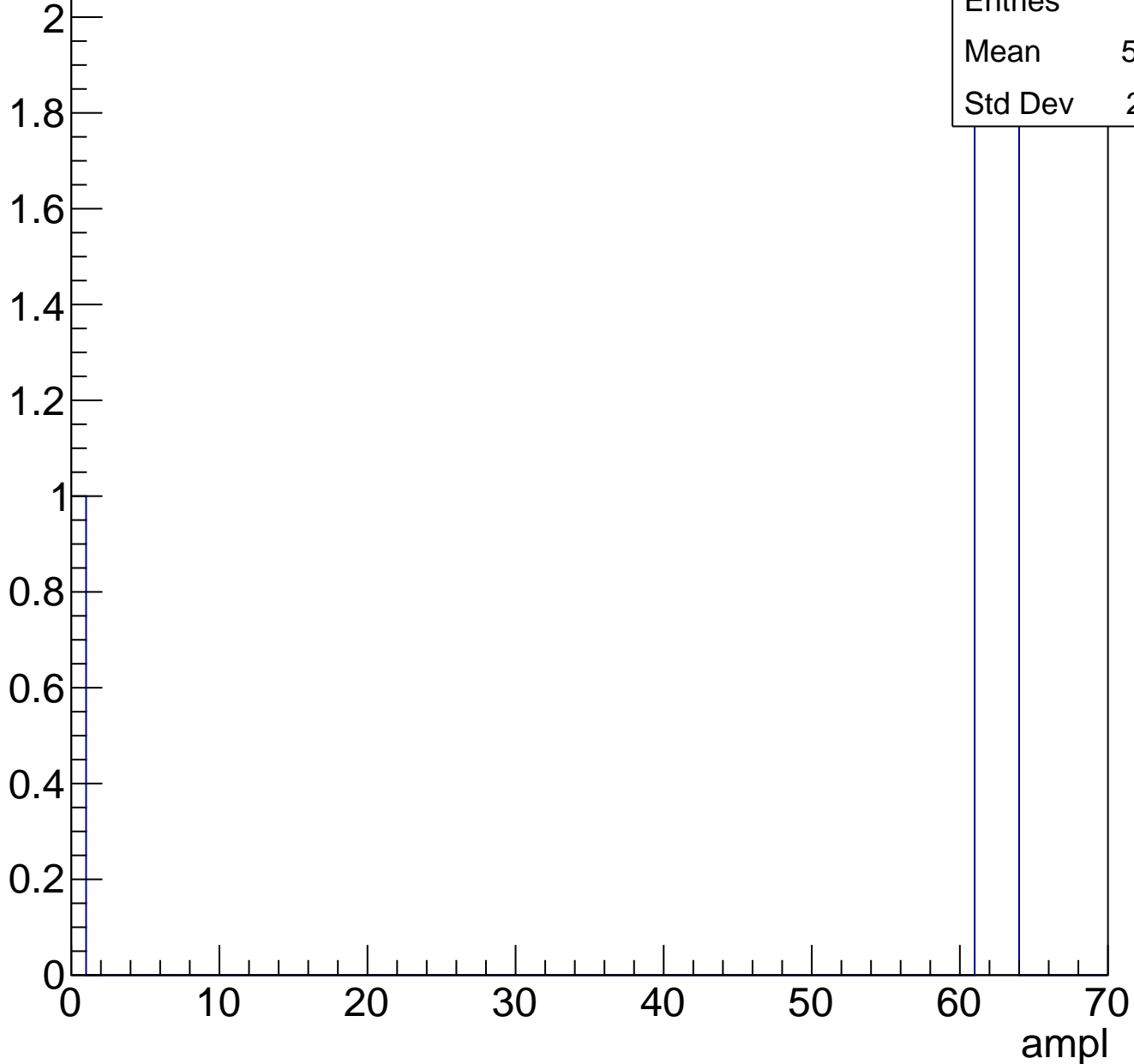
Entries	35
Mean	60.54
Std Dev	2.061



# B1L101S, U20-ch75, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U20-ch75, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U20-ch76, adc0

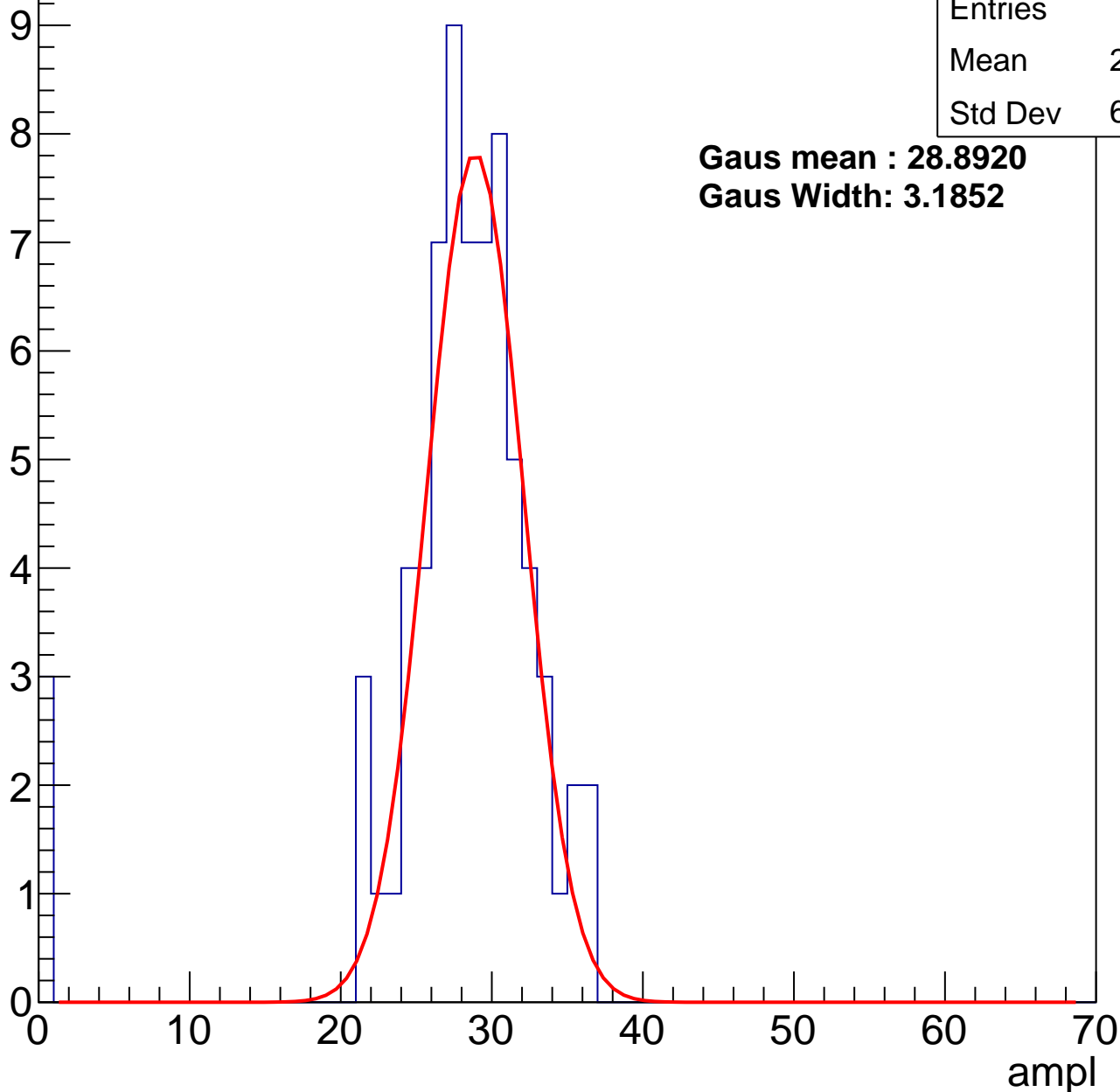
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	71
Mean	27.13
Std Dev	6.637

**Gaus mean : 28.8920**

**Gaus Width: 3.1852**



# B1L101S, U20-ch76, adc1

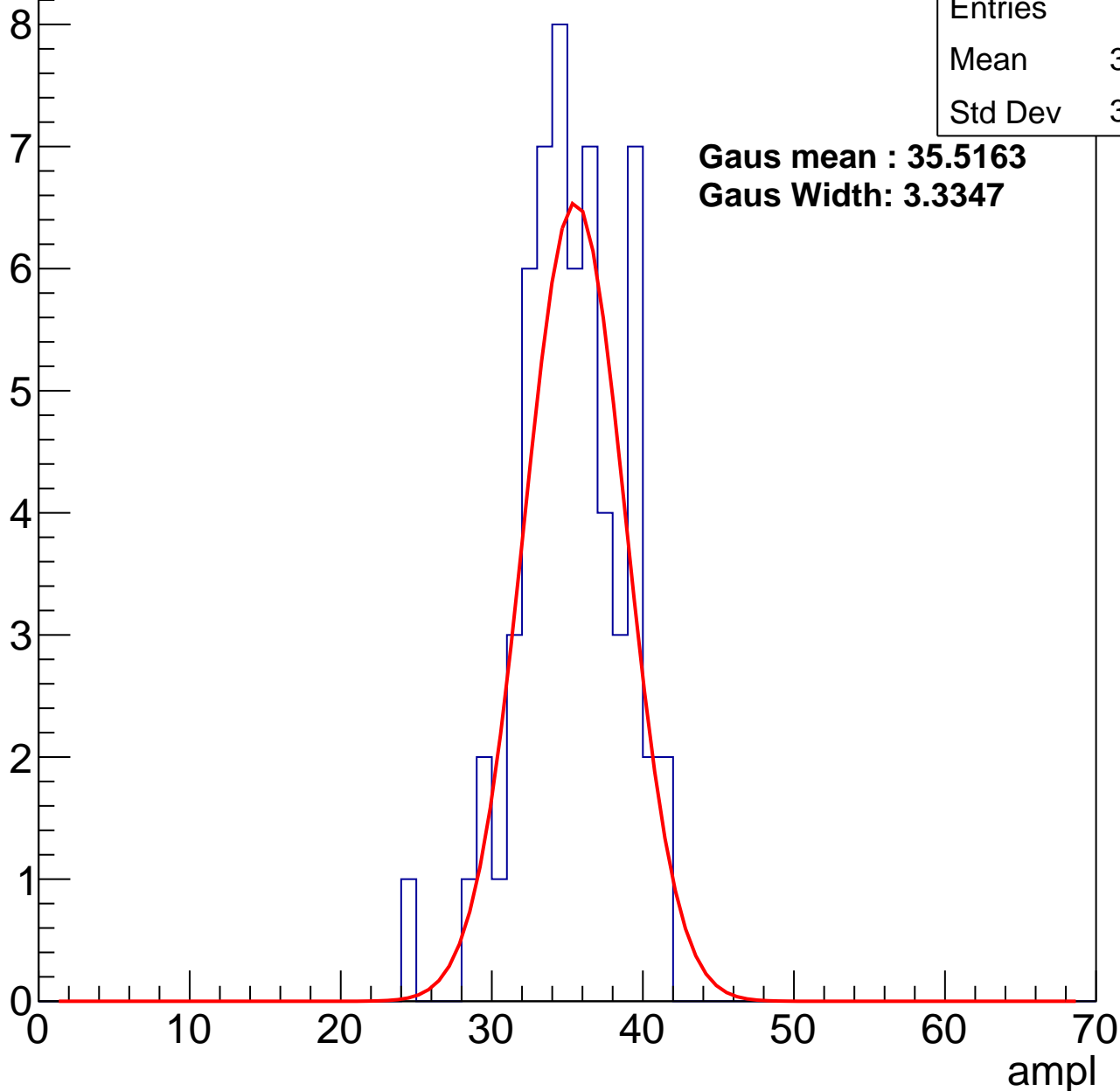
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	60
Mean	34.78
Std Dev	3.382

**Gaus mean : 35.5163**

**Gaus Width: 3.3347**

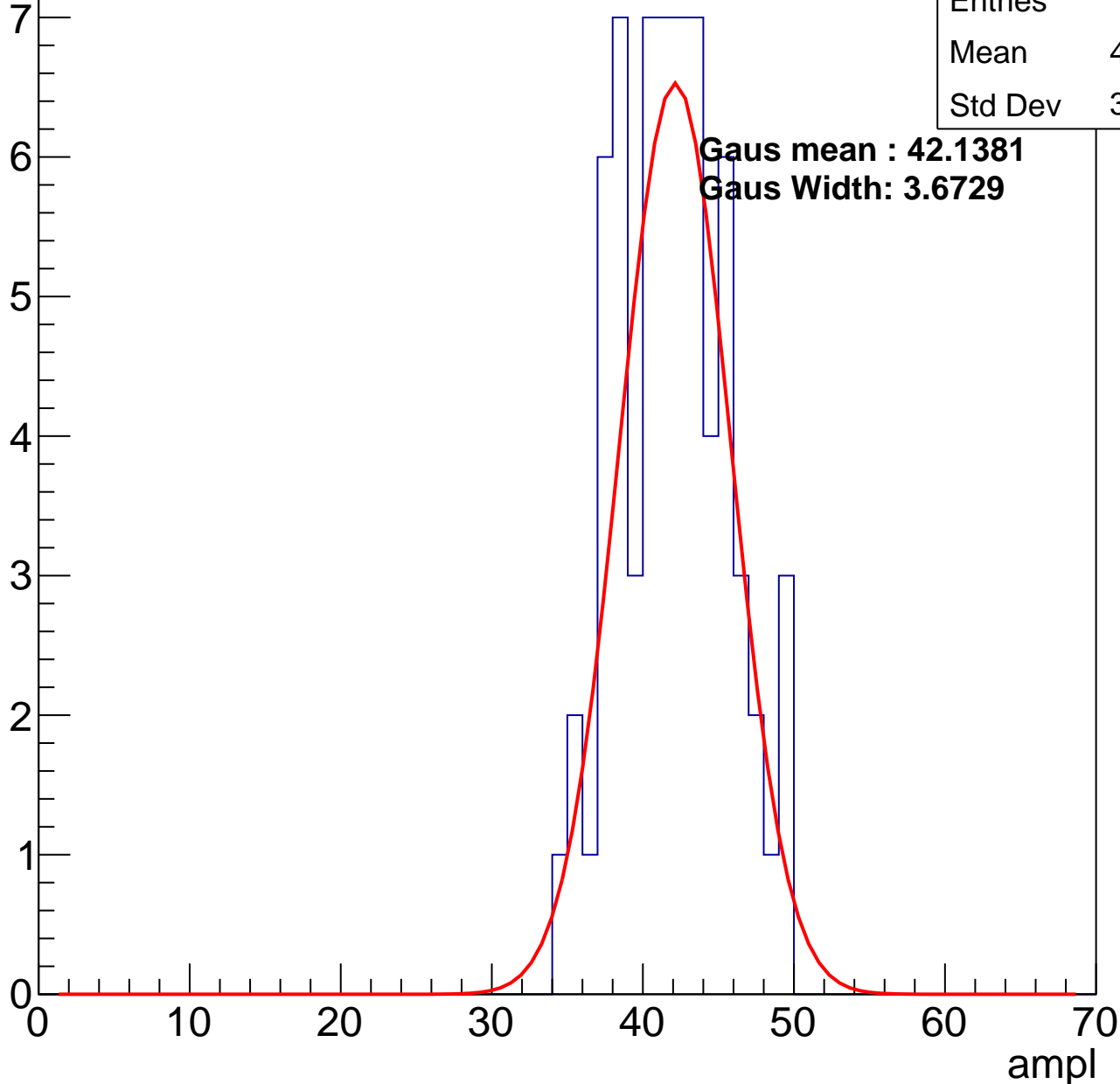


# B1L101S, U20-ch76, adc2

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	67
Mean	41.49
Std Dev	3.588

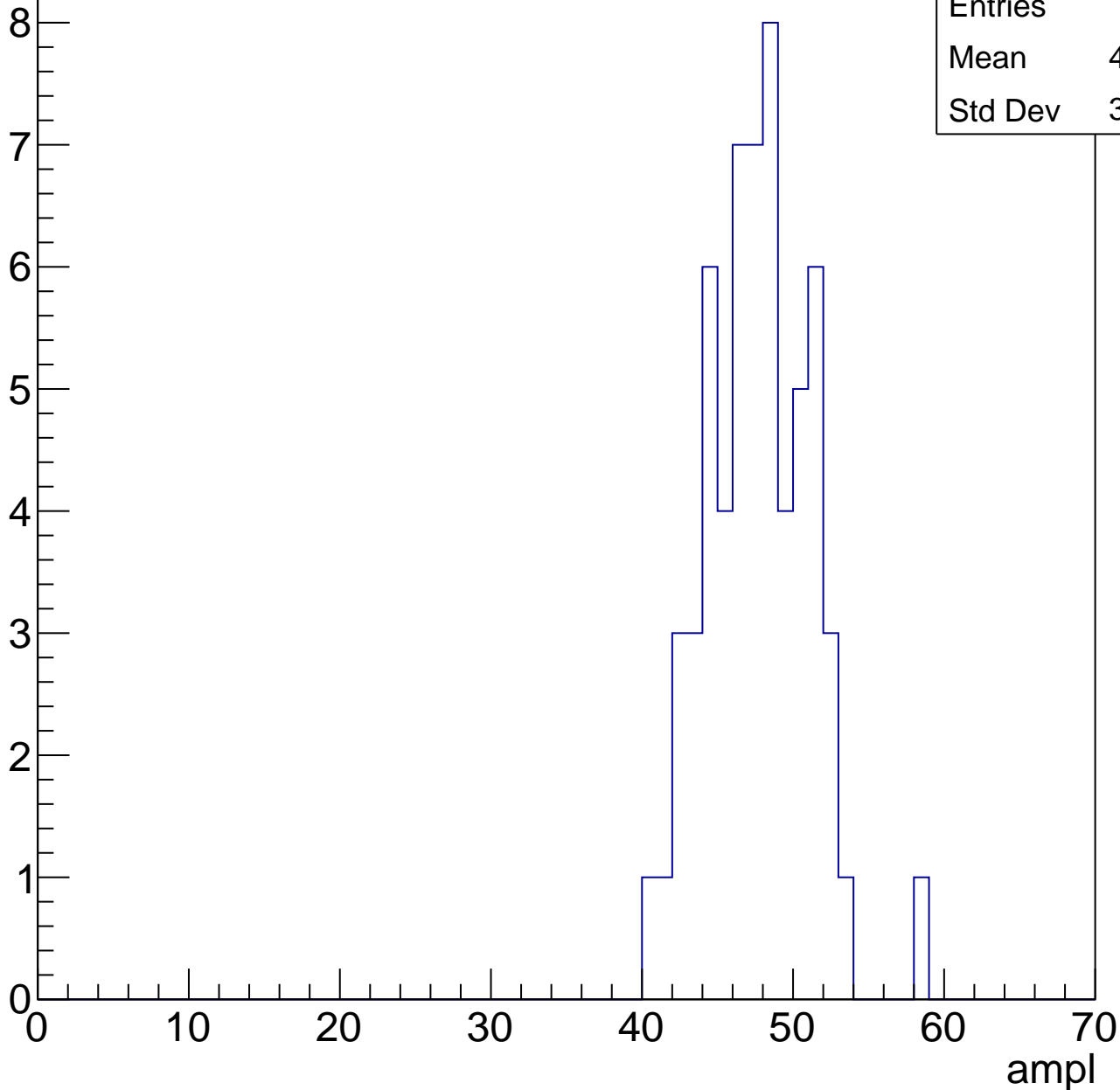


# B1L101S, U20-ch76, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

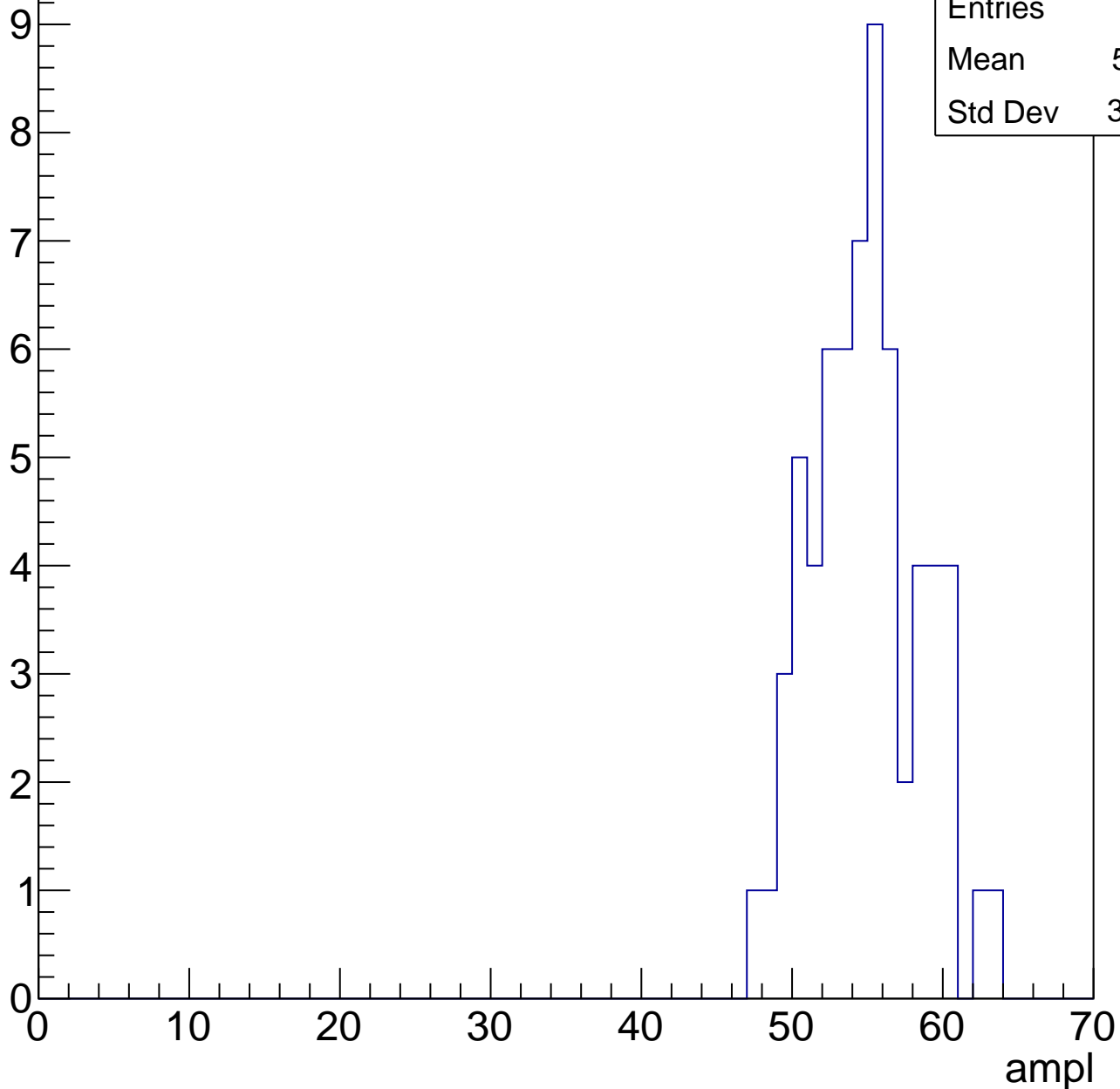
Entries	60
Mean	47.23
Std Dev	3.363



# B1L101S, U20-ch76, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

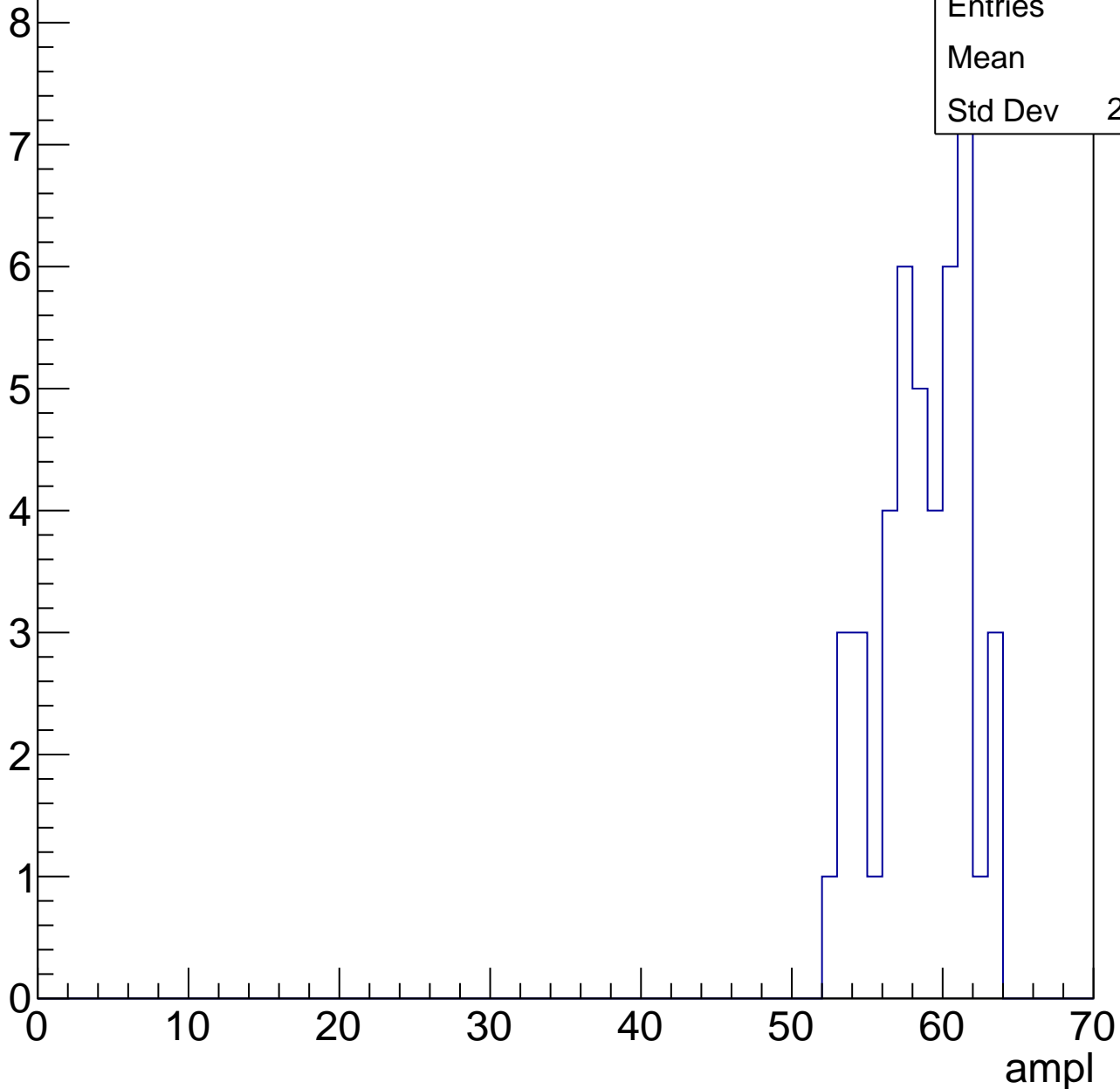


# B1L101S, U20-ch76, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	45
Mean	58.2
Std Dev	2.903

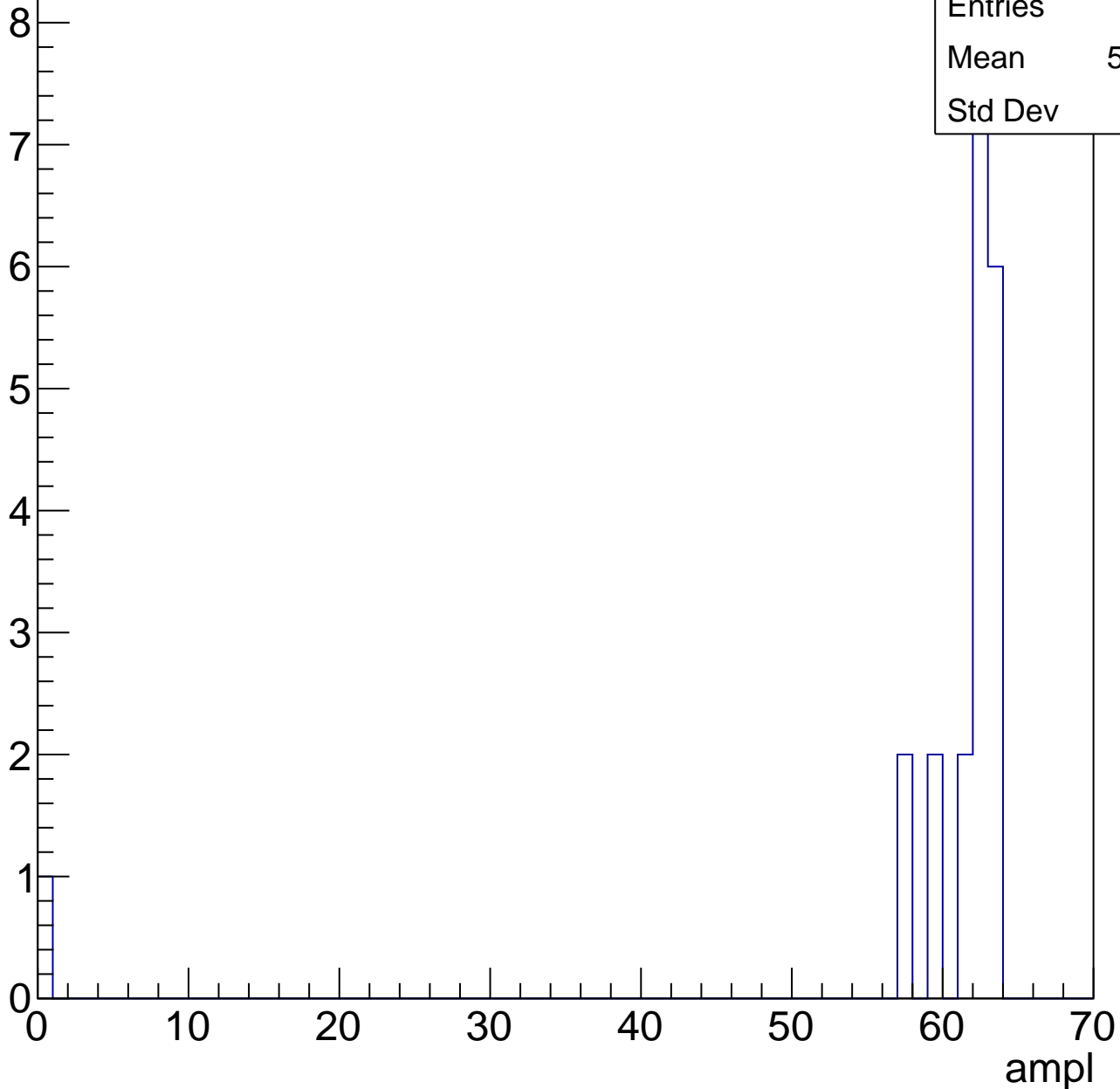


# B1L101S, U20-ch76, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	21
Mean	58.48
Std Dev	13.2





# B1L101S, U20-ch76, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L101S, U20-ch77, adc0

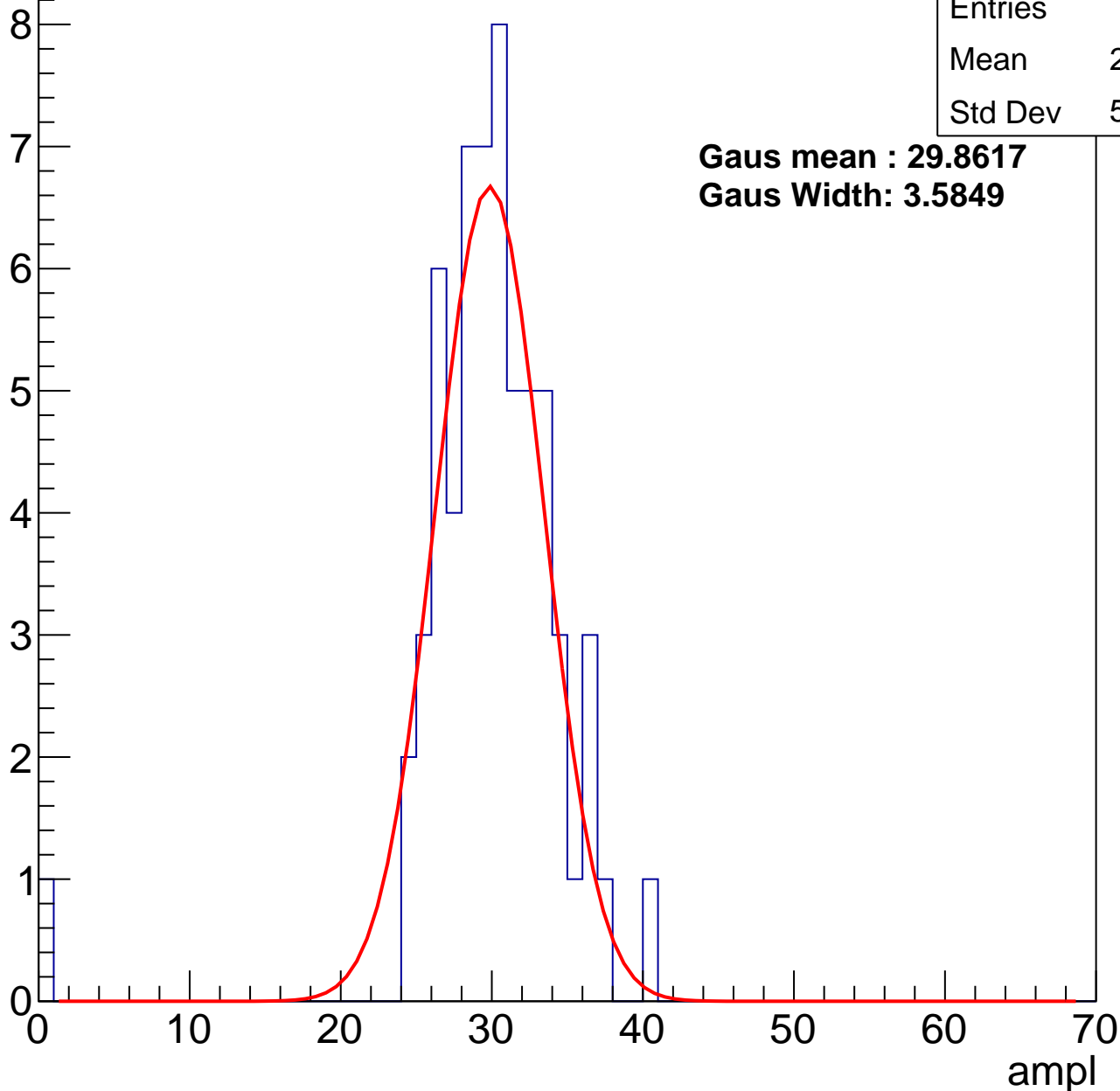
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	29.48
Std Dev	5.076

**Gaus mean : 29.8617**

**Gaus Width: 3.5849**



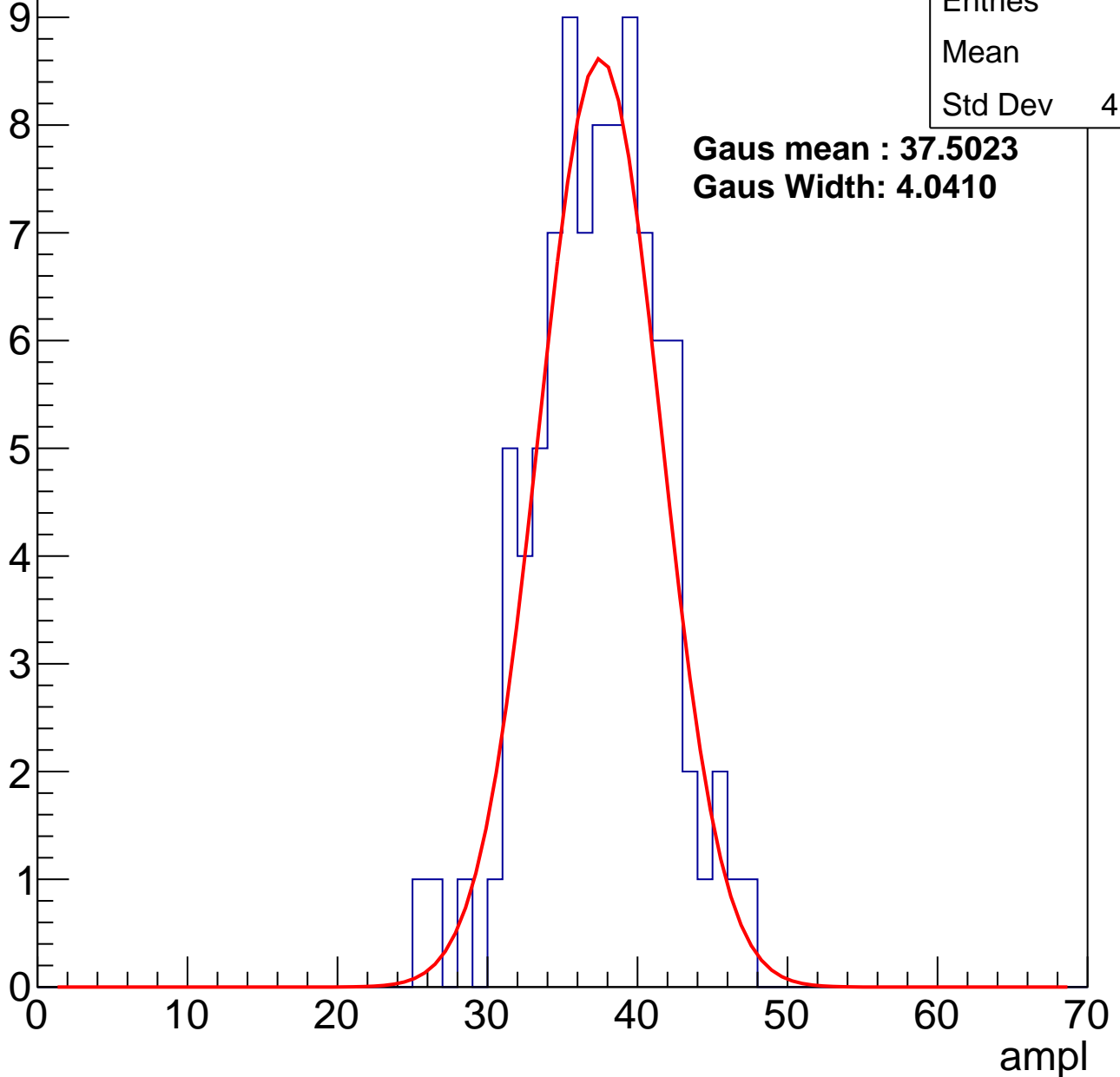
# B1L101S, U20-ch77, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	92
Mean	37
Std Dev	4.227

**Gaus mean : 37.5023**  
**Gaus Width: 4.0410**



# B1L101S, U20-ch77, adc2

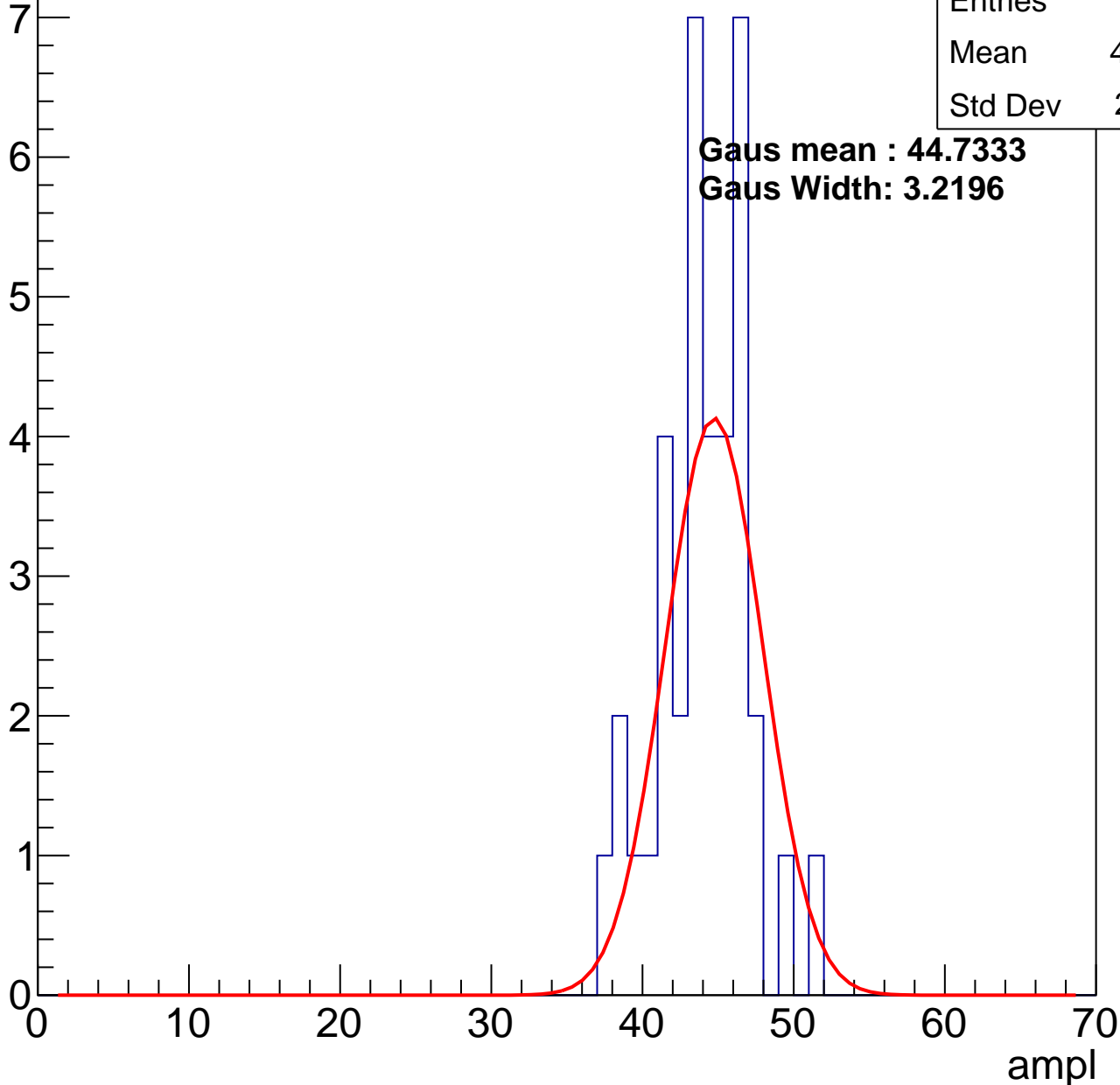
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	37
Mean	43.59
Std Dev	2.991

**Gaus mean : 44.7333**

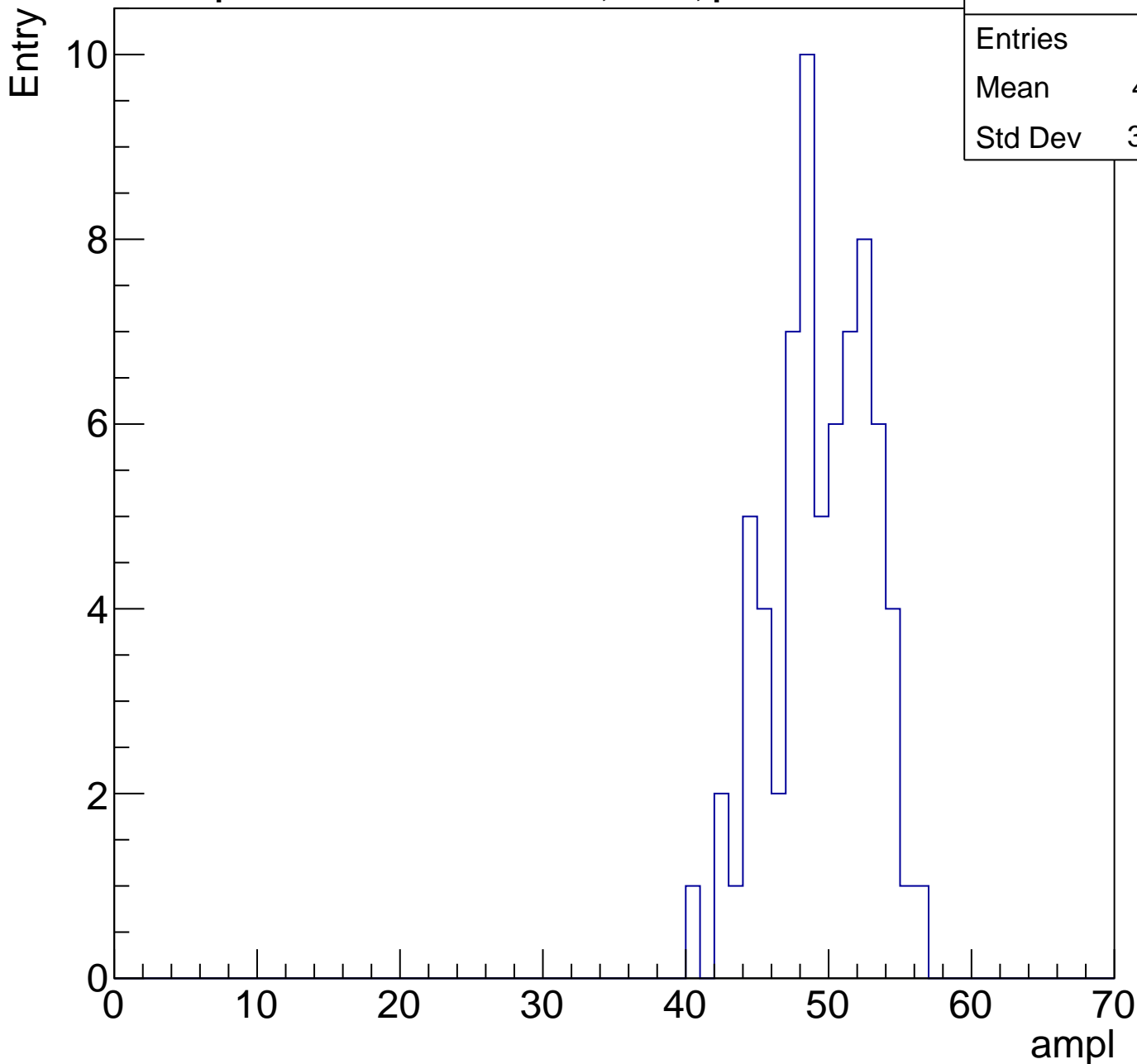
**Gaus Width: 3.2196**



# B1L101S, U20-ch77, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	70
Mean	49.01
Std Dev	3.478

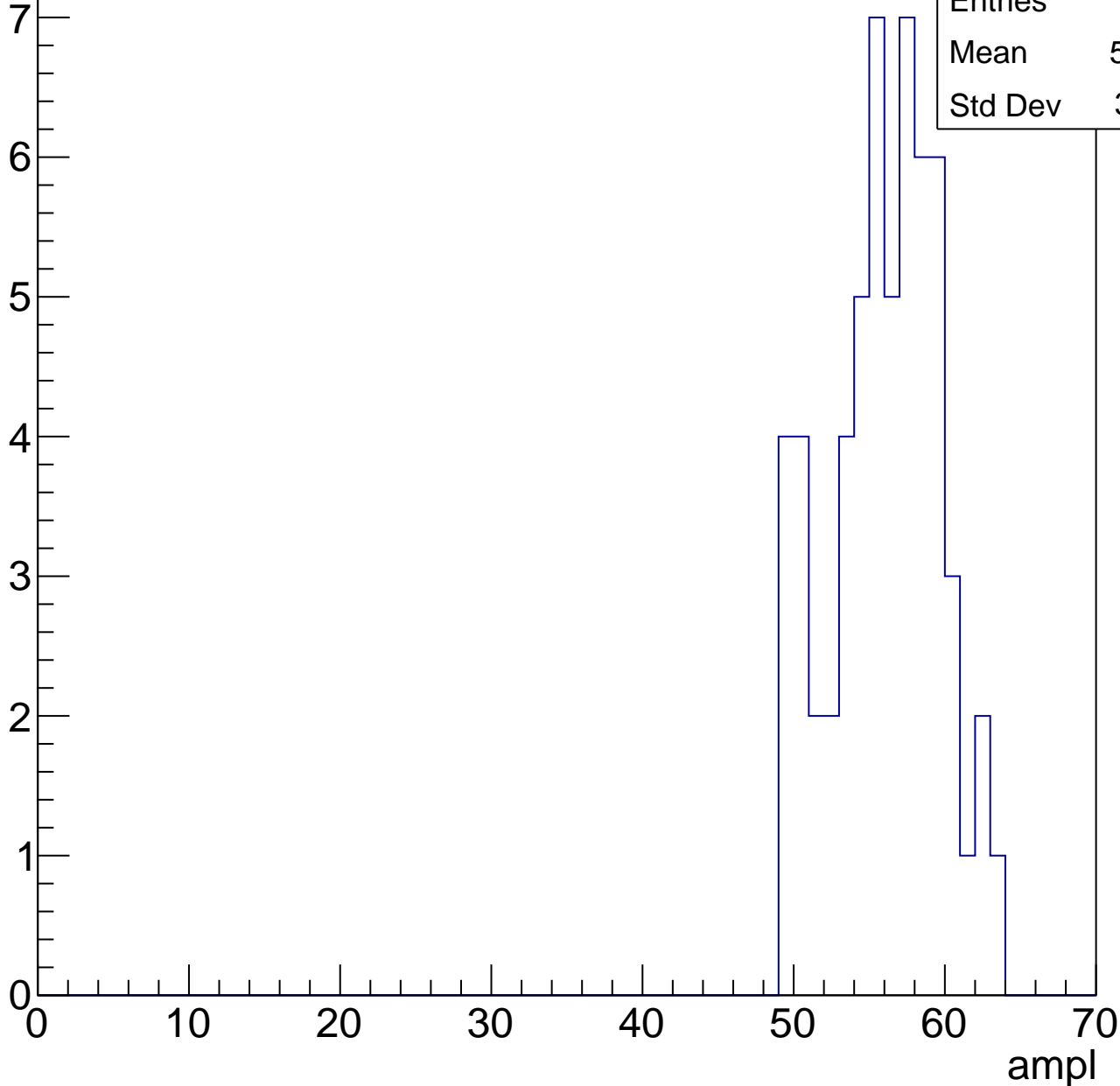


# B1L101S, U20-ch77, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	59
Mean	55.56
Std Dev	3.571

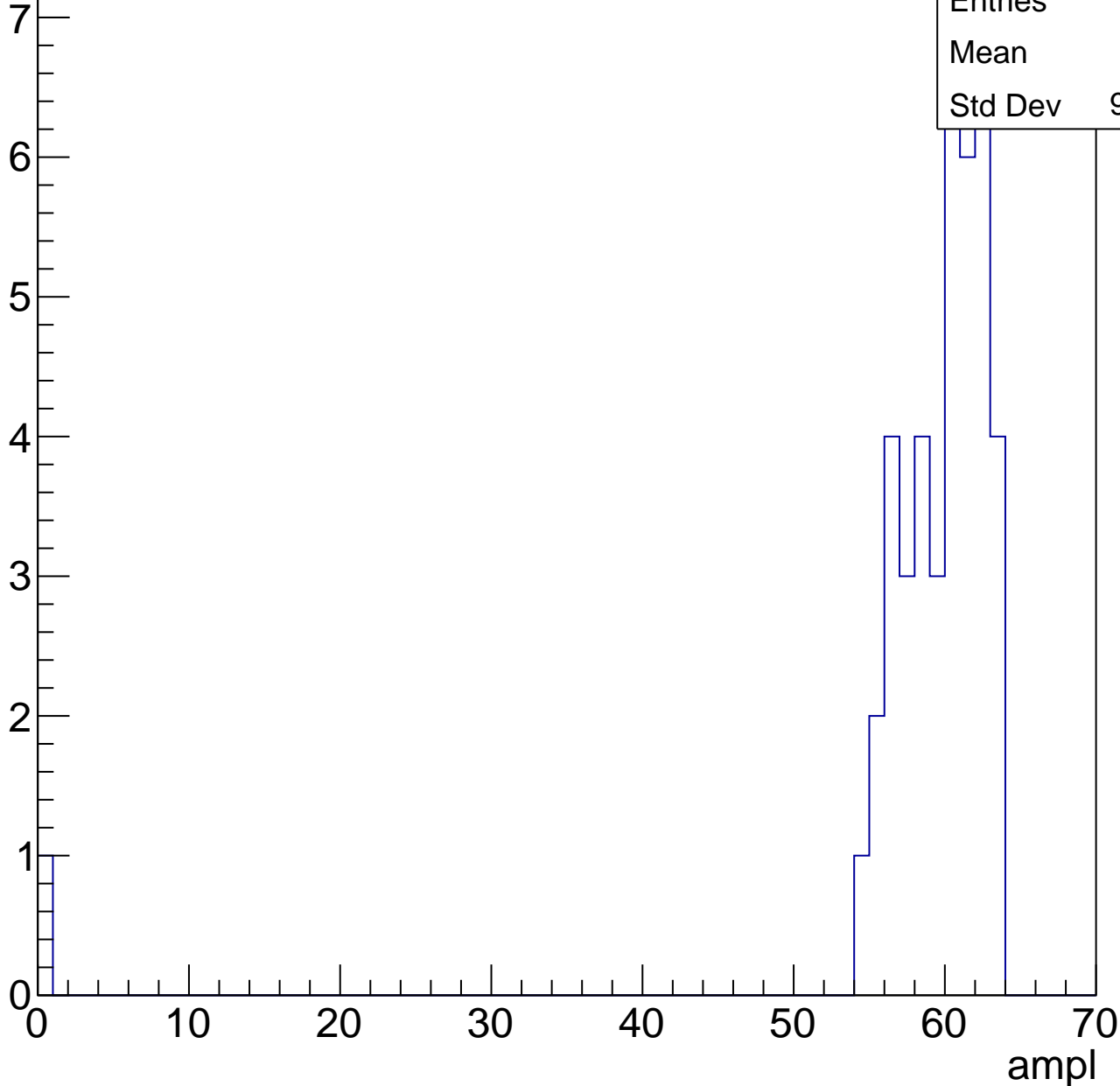


# B1L101S, U20-ch77, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	42
Mean	58.1
Std Dev	9.403

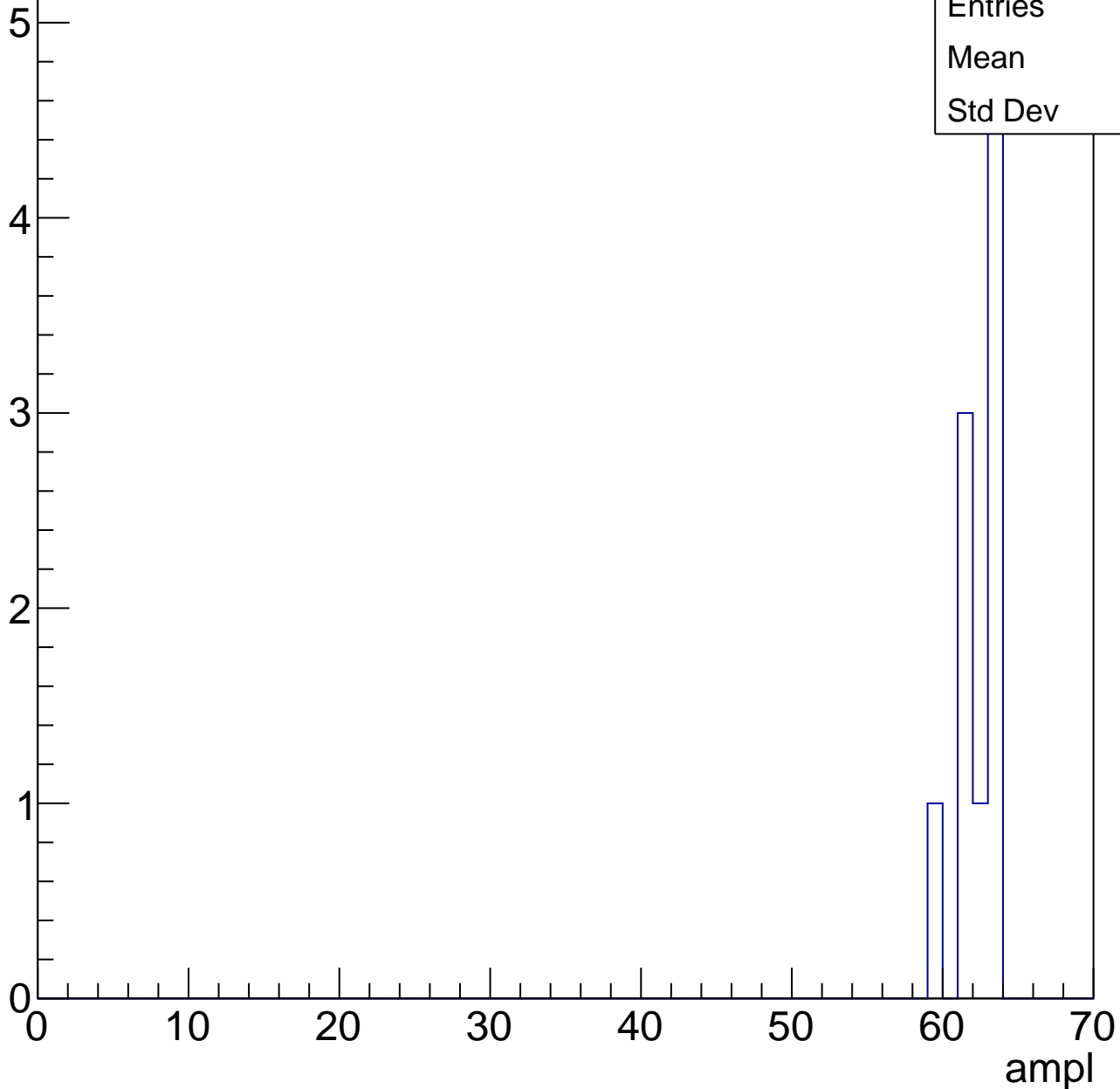


# B1L101S, U20-ch77, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	10
Mean	61.9
Std Dev	1.3





# B1L101S, U20-ch77, adc7

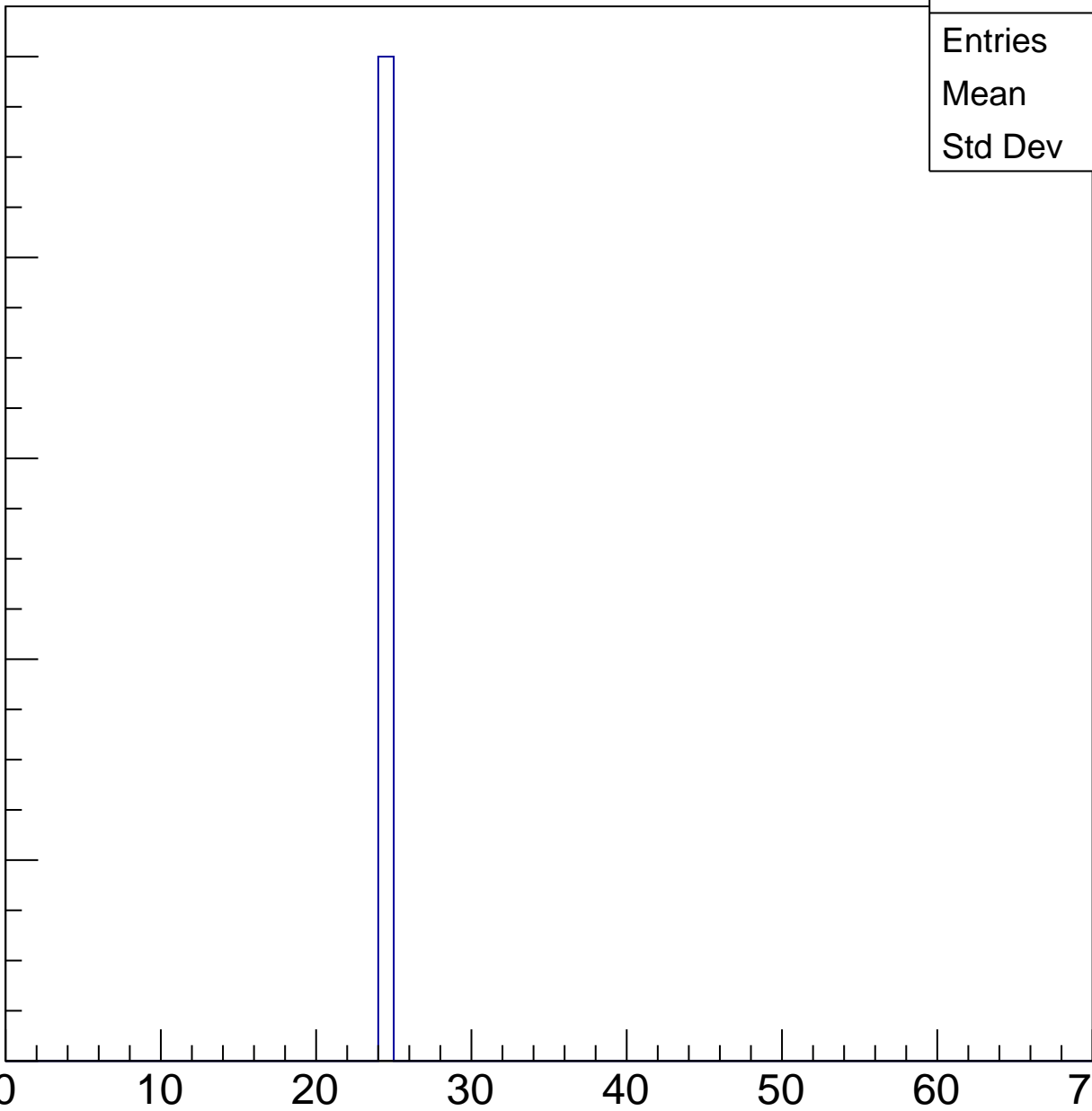
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

1  
0.8  
0.6  
0.4  
0.2  
0

Entries	1
Mean	24
Std Dev	0

ampl



# B1L101S, U20-ch78, adc0

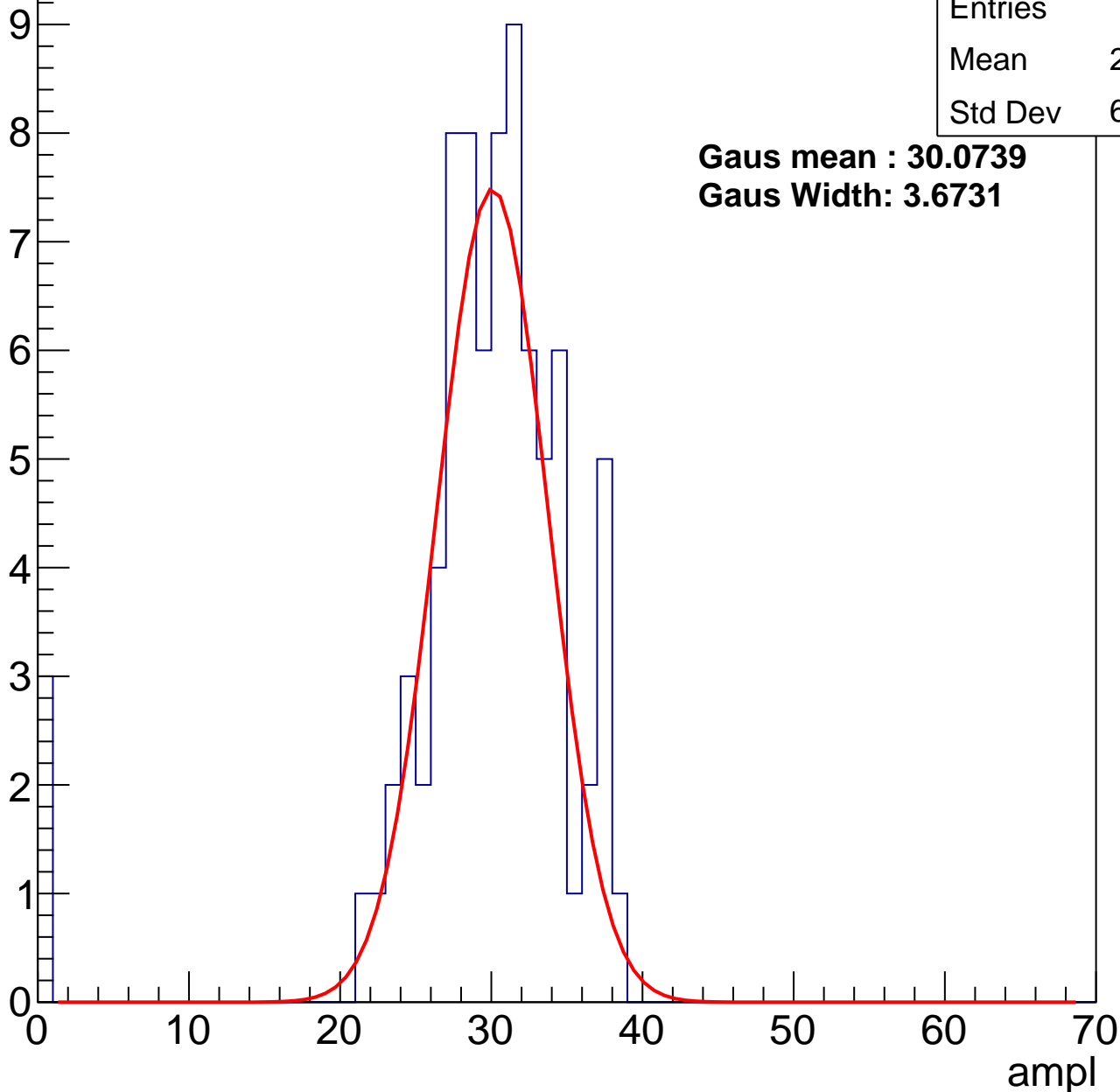
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	81
Mean	28.88
Std Dev	6.807

**Gaus mean : 30.0739**

**Gaus Width: 3.6731**



# B1L101S, U20-ch78, adc1

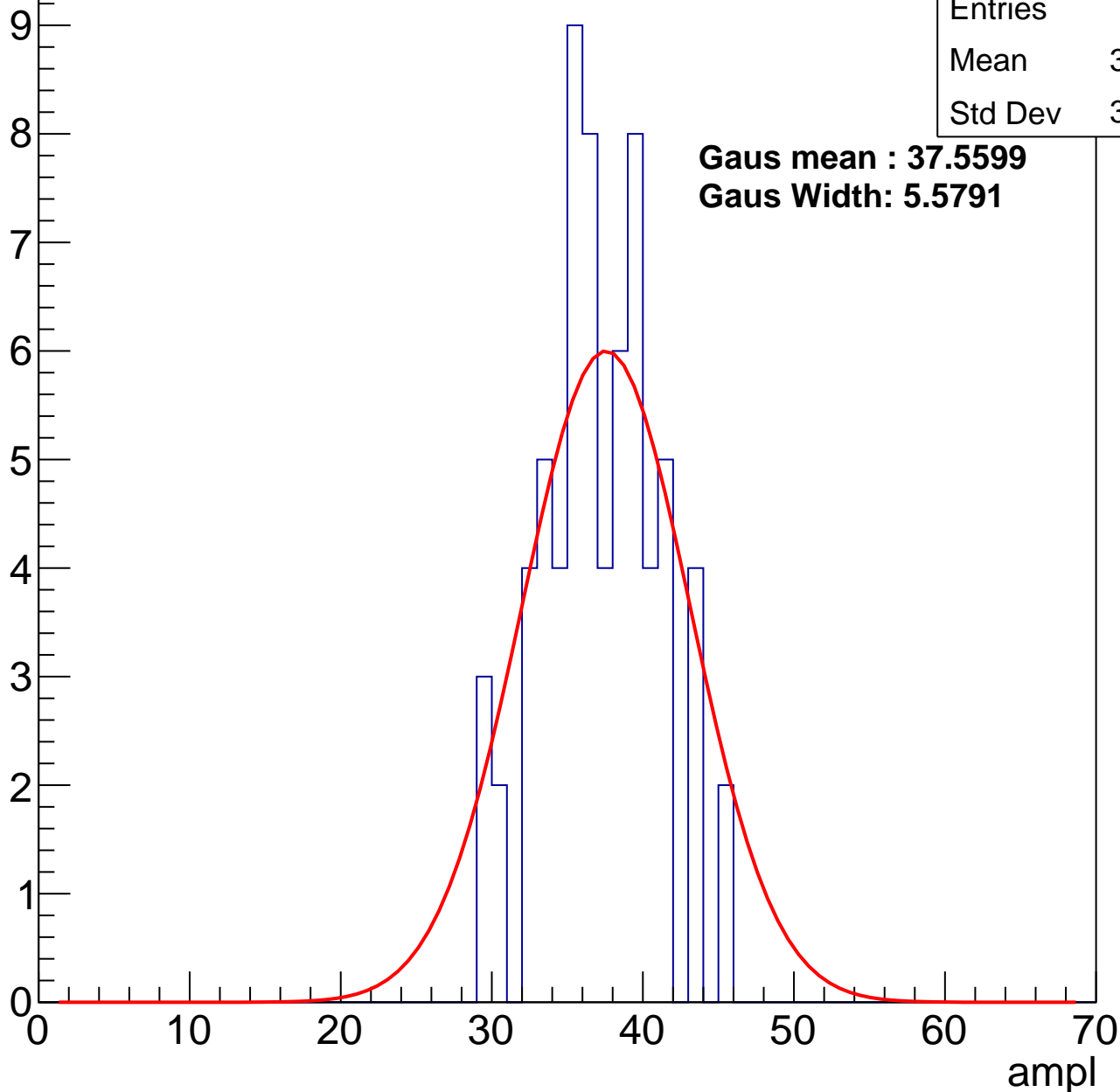
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	36.68
Std Dev	3.775

**Gaus mean : 37.5599**

**Gaus Width: 5.5791**



# B1L101S, U20-ch78, adc2

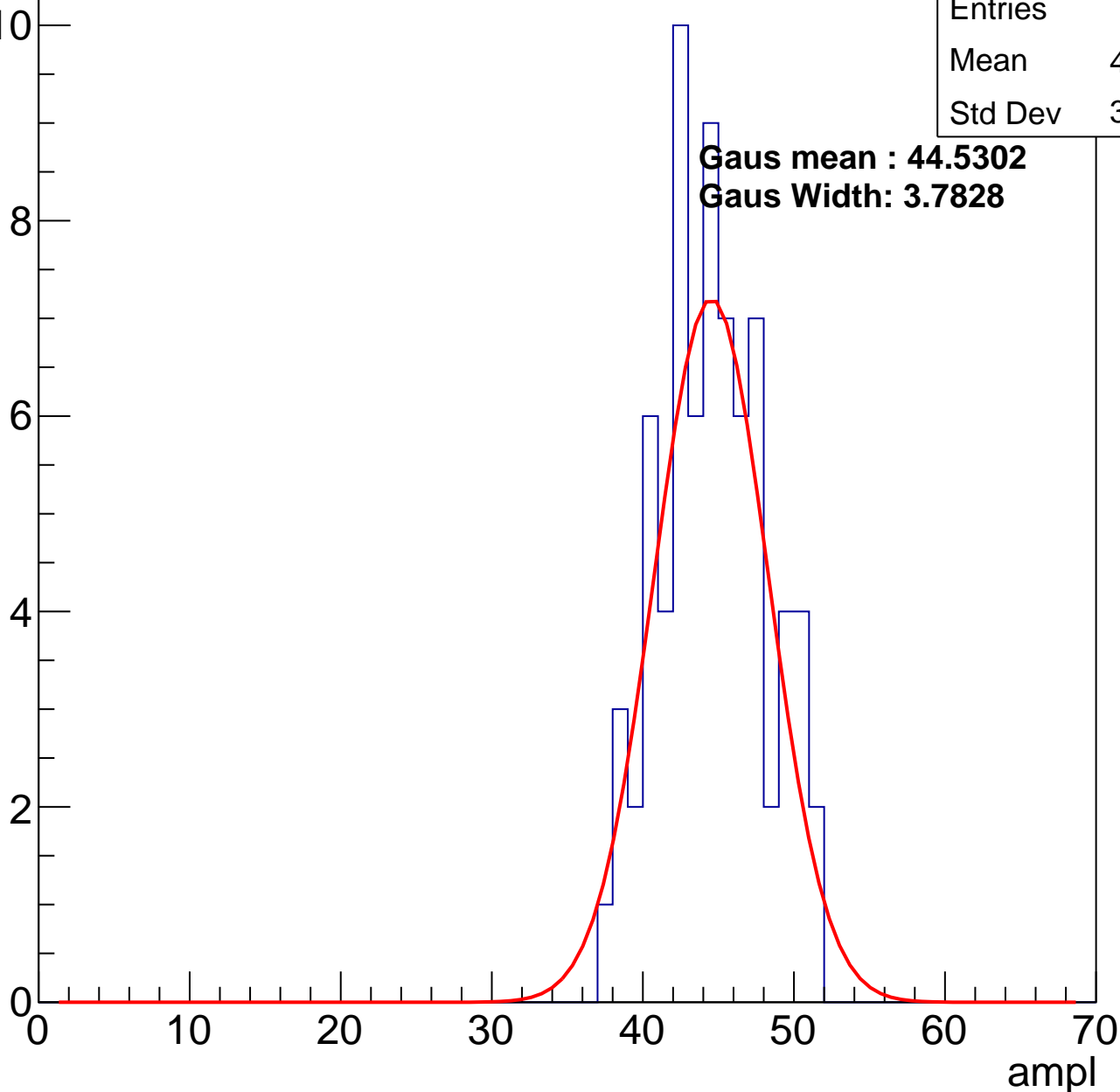
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	73
Mean	44.12
Std Dev	3.416

**Gaus mean : 44.5302**

**Gaus Width: 3.7828**

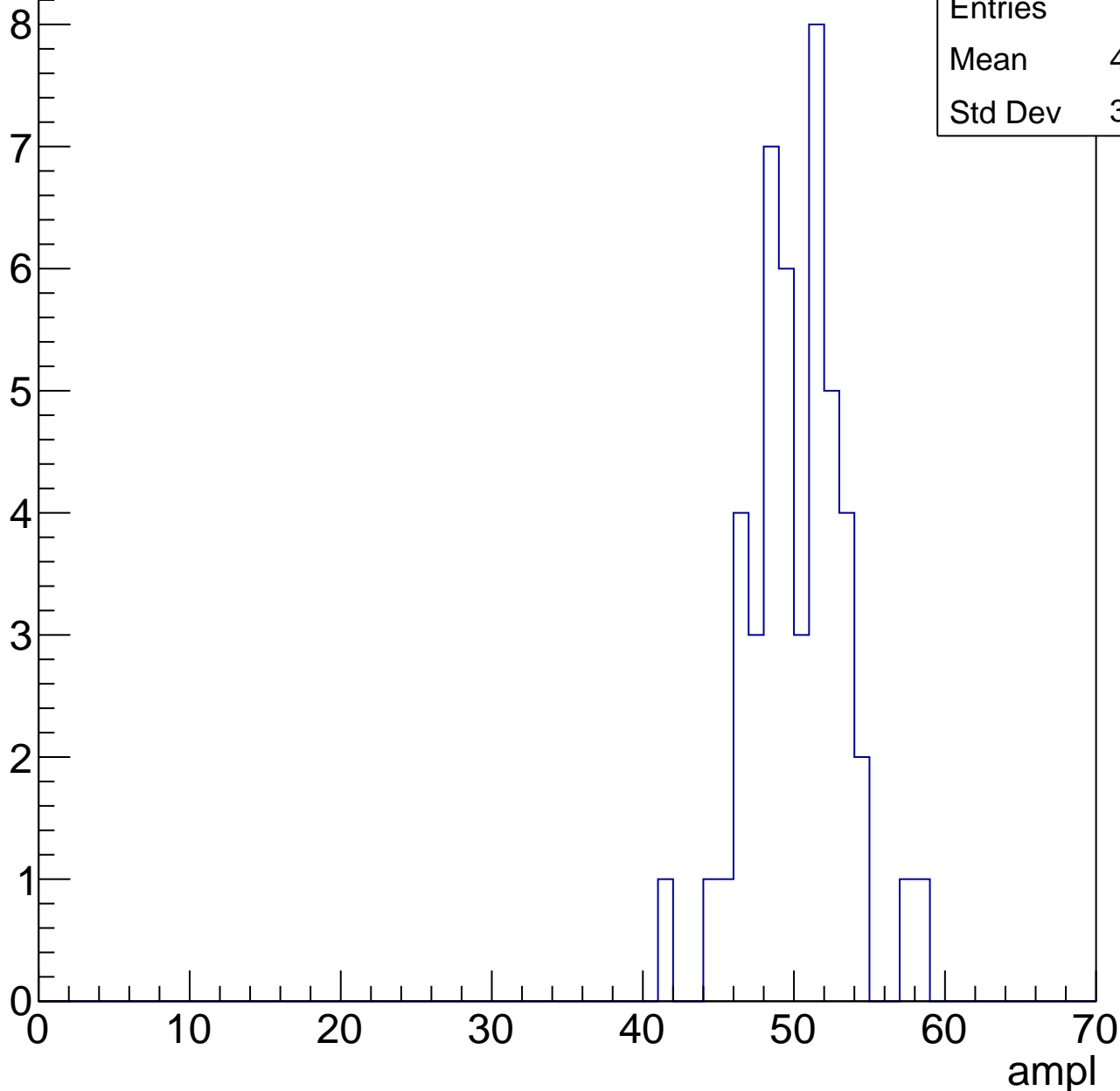


# B1L101S, U20-ch78, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	47
Mean	49.74
Std Dev	3.172

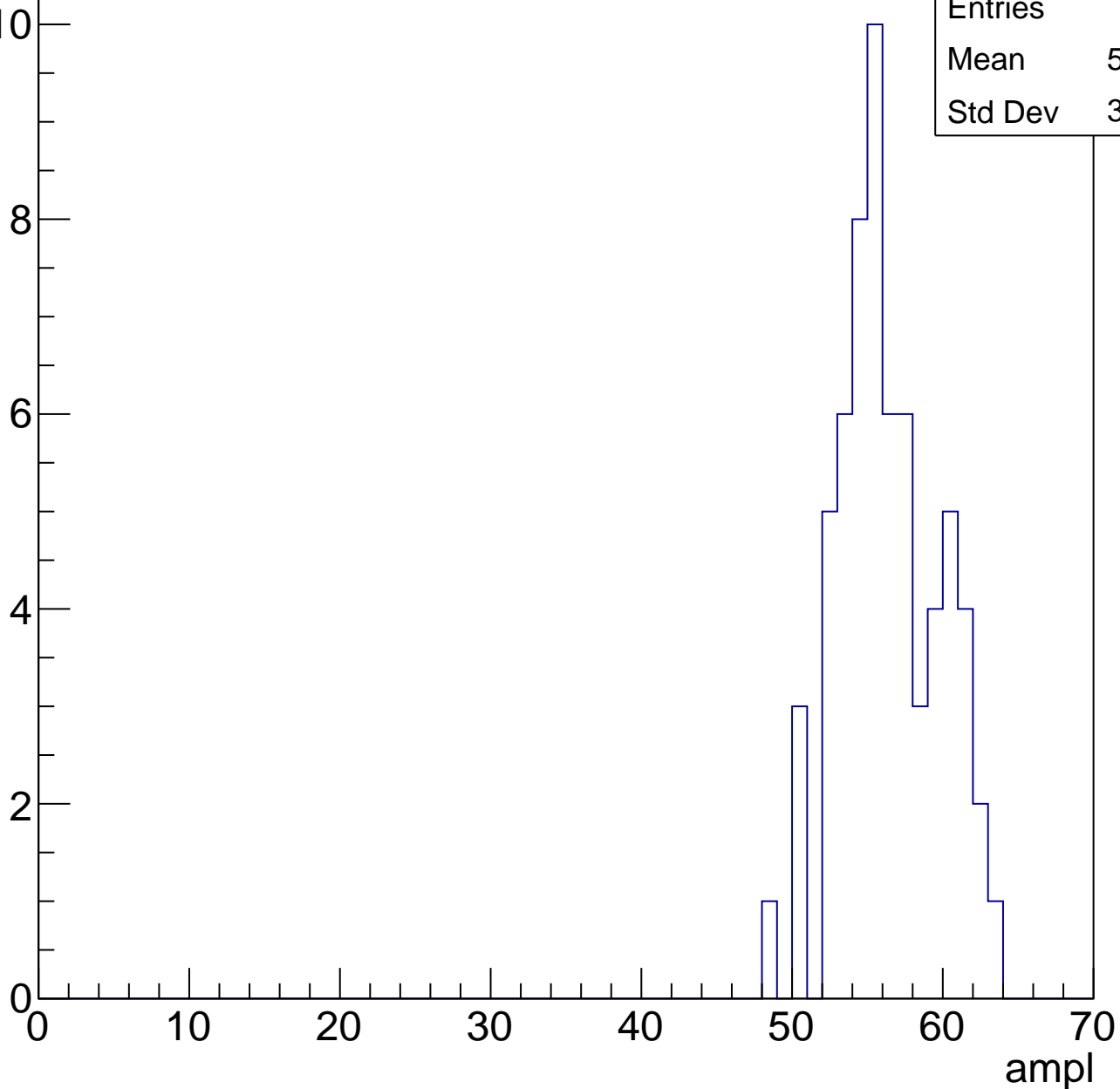


# B1L101S, U20-ch78, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	55.89
Std Dev	3.312

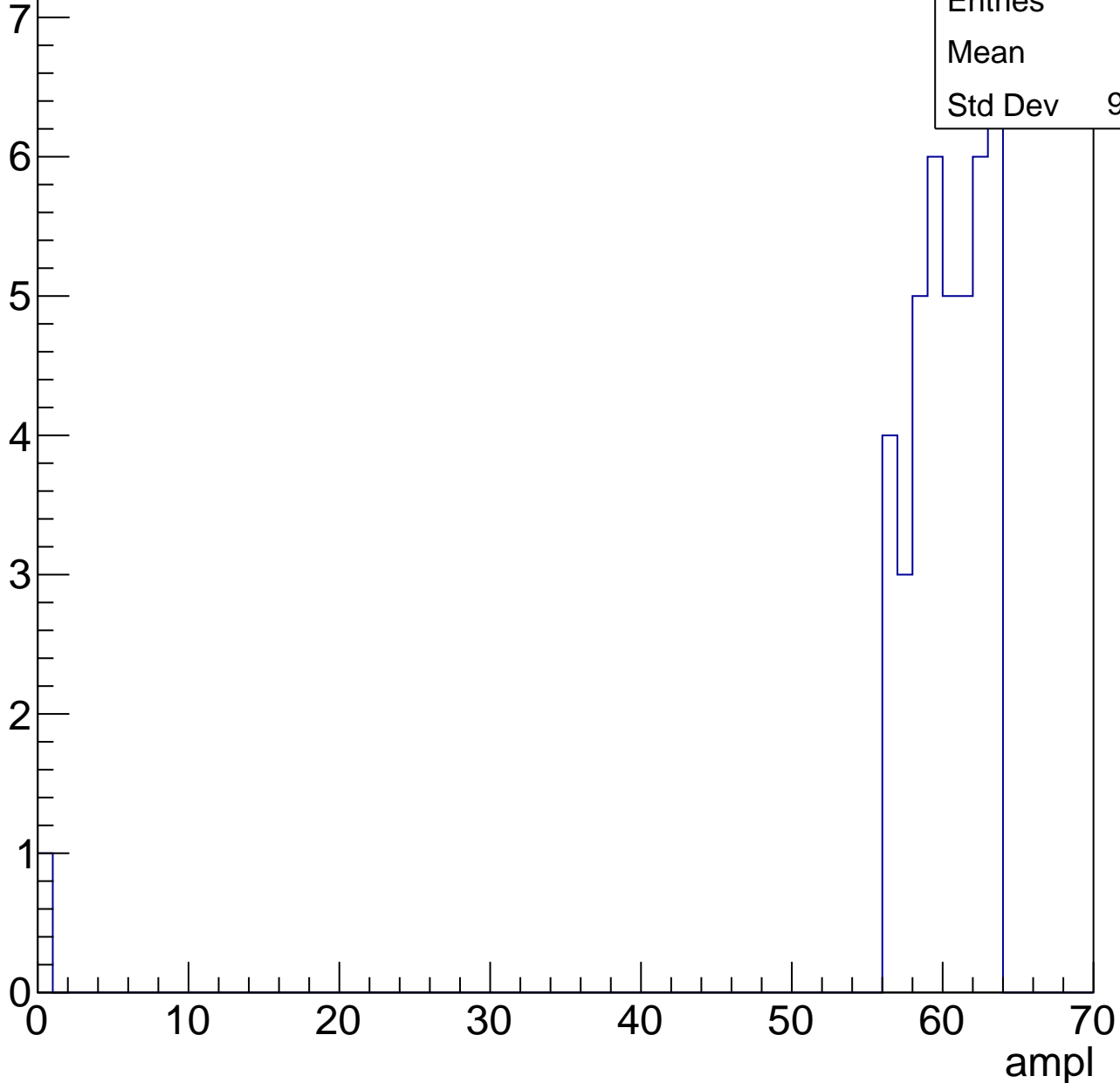


# B1L101S, U20-ch78, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

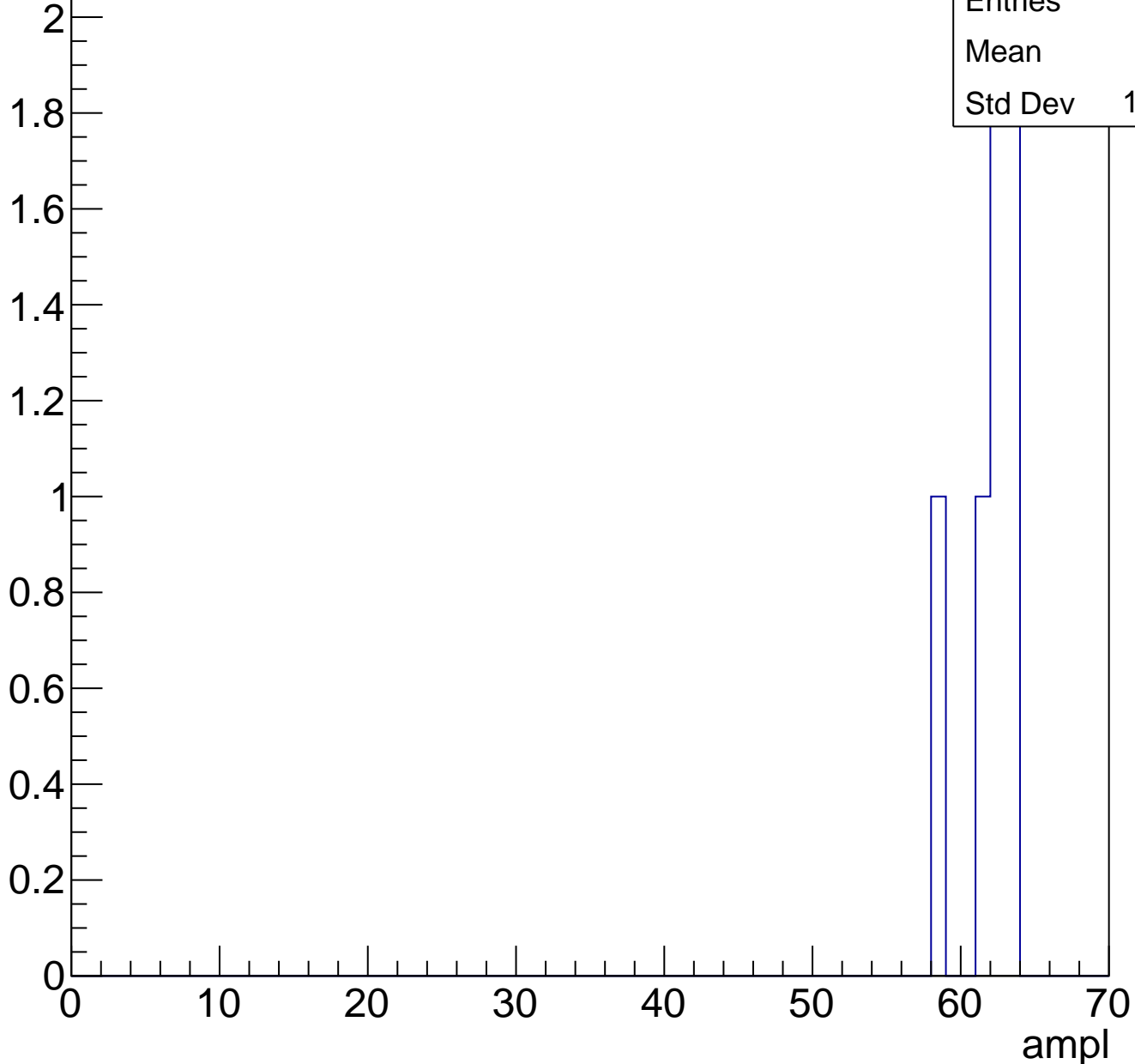
Entries	42
Mean	58.5
Std Dev	9.404



# B1L101S, U20-ch78, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U20-ch78, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	3
Mean	0
Std Dev	0

# B1L101S, U20-ch79, adc0

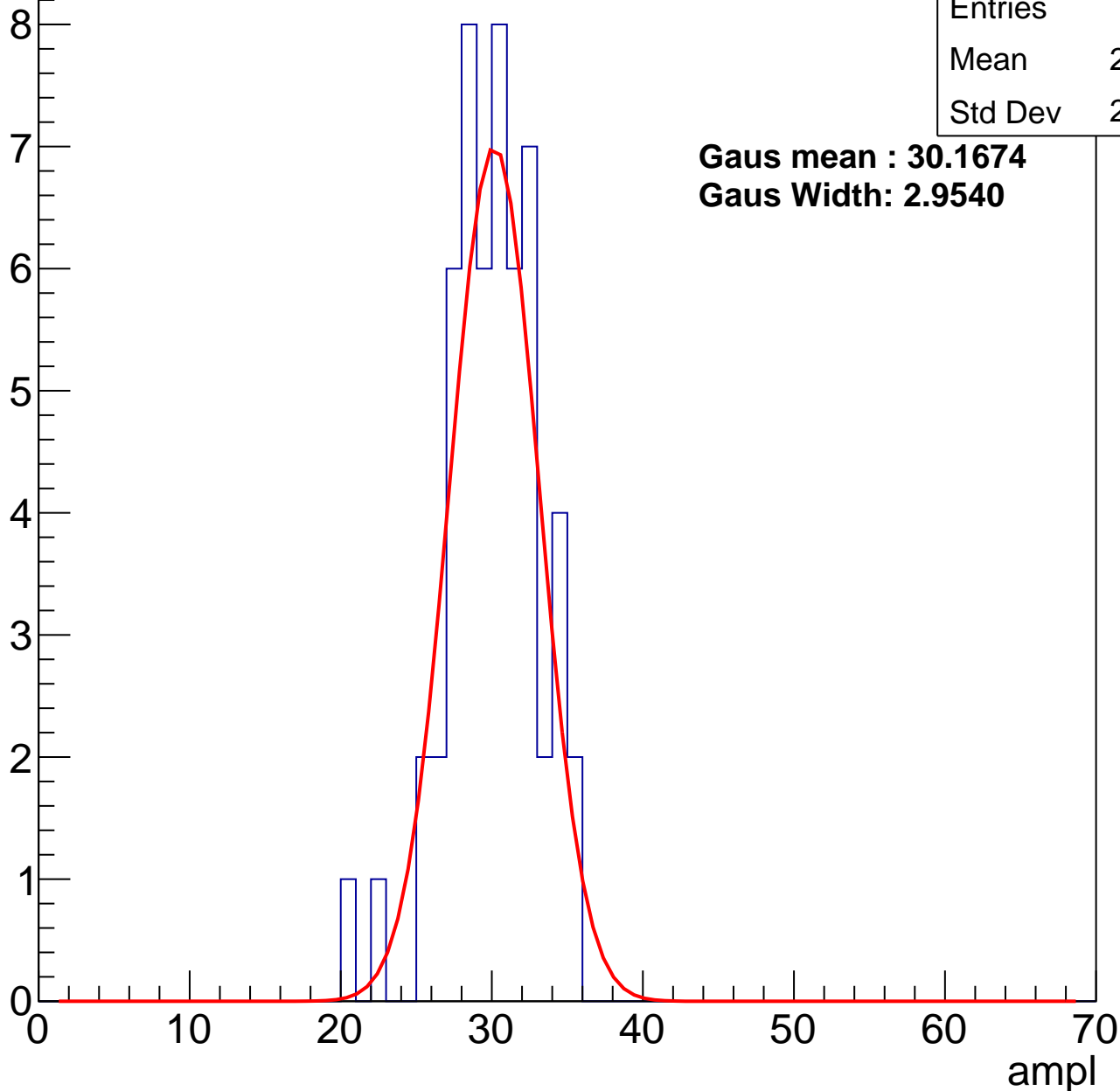
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	55
Mean	29.56
Std Dev	2.996

**Gaus mean : 30.1674**

**Gaus Width: 2.9540**



# B1L101S, U20-ch79, adc1

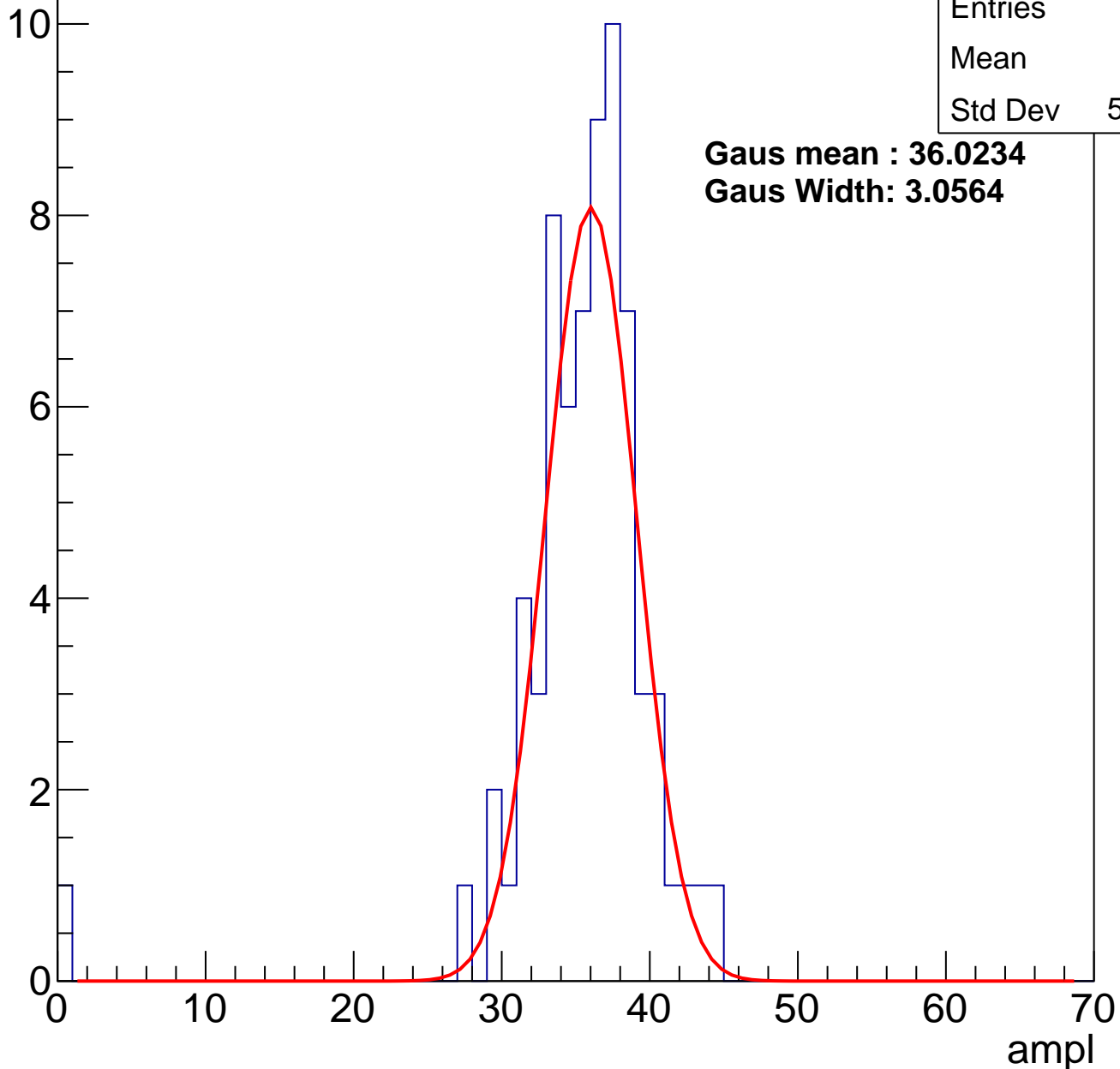
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	69
Mean	35
Std Dev	5.357

**Gaus mean : 36.0234**

**Gaus Width: 3.0564**

Entry



# B1L101S, U20-ch79, adc2

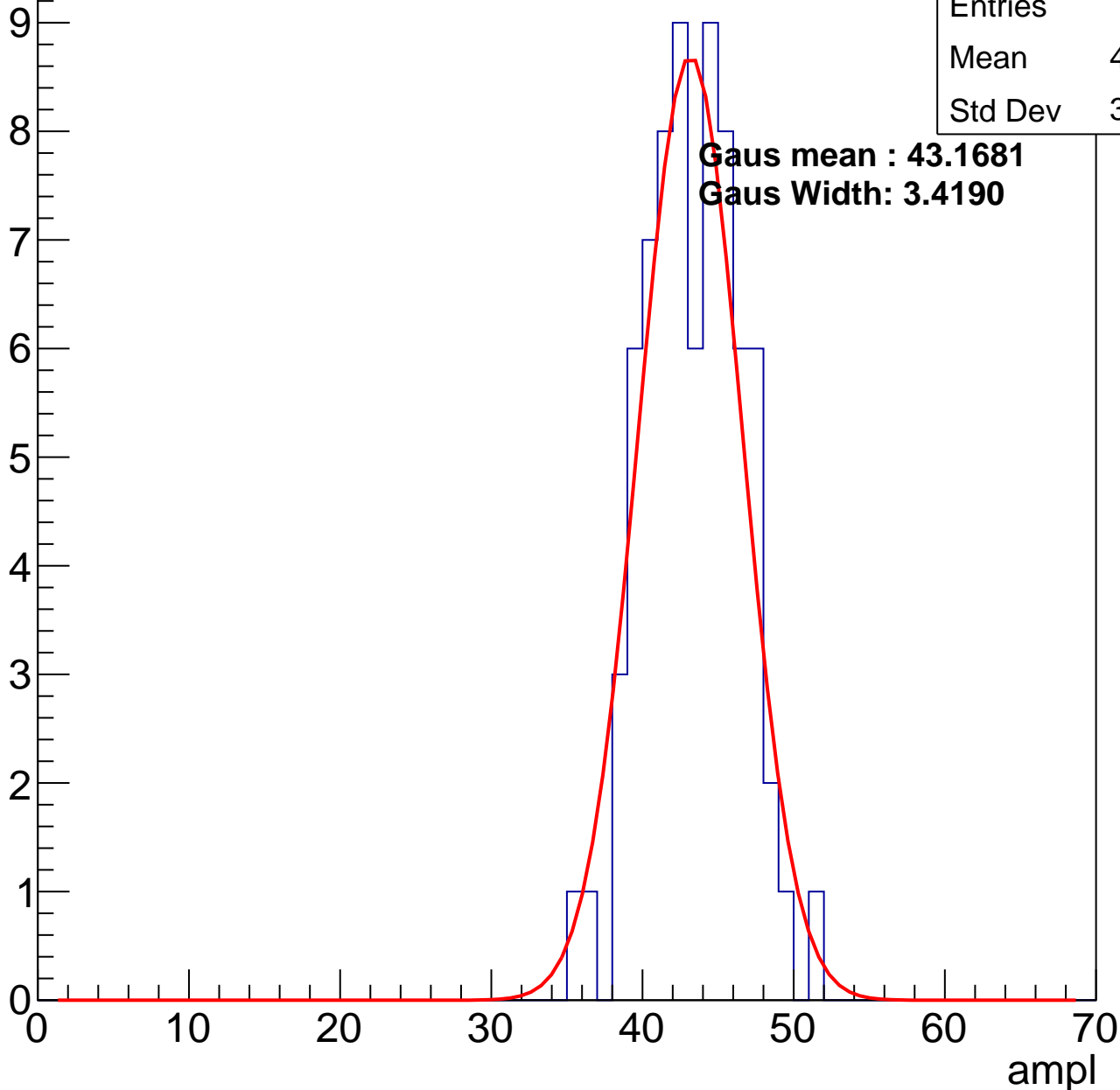
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	74
Mean	42.88
Std Dev	3.136

**Gaus mean : 43.1681**

**Gaus Width: 3.4190**

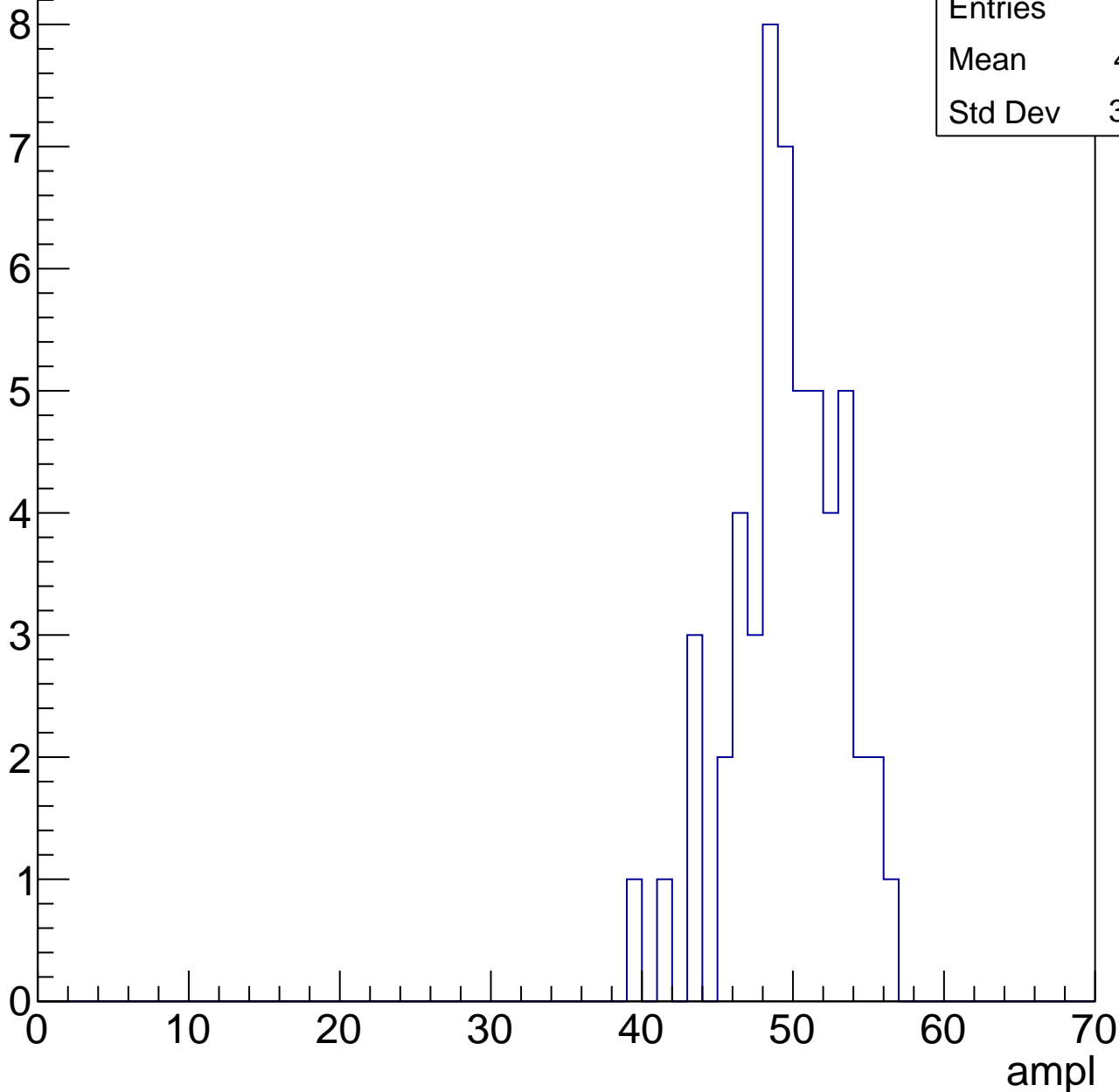


# B1L101S, U20-ch79, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	53
Mean	49.11
Std Dev	3.559

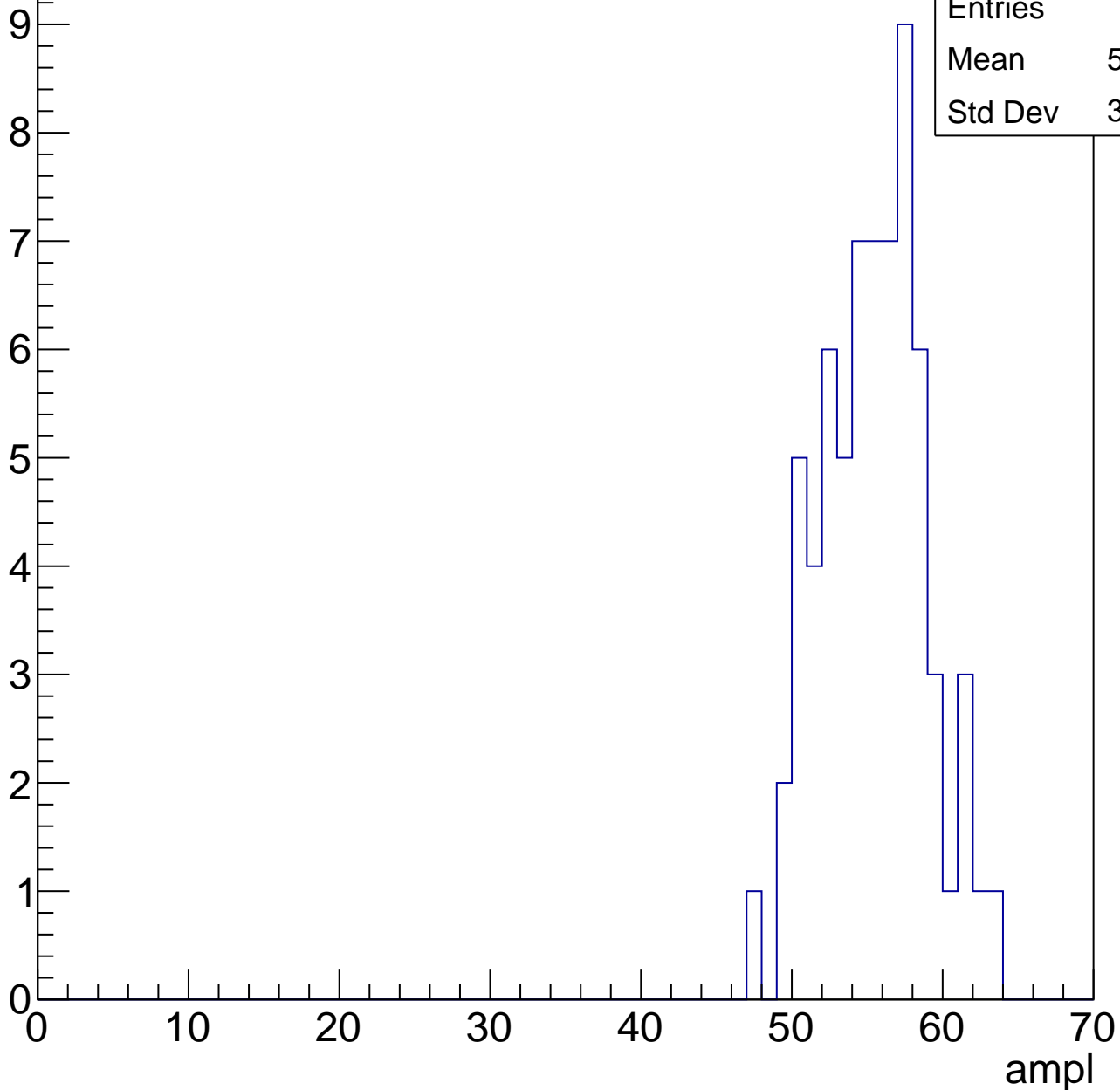


# B1L101S, U20-ch79, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	54.96
Std Dev	3.423



# B1L101S, U20-ch79, adc5

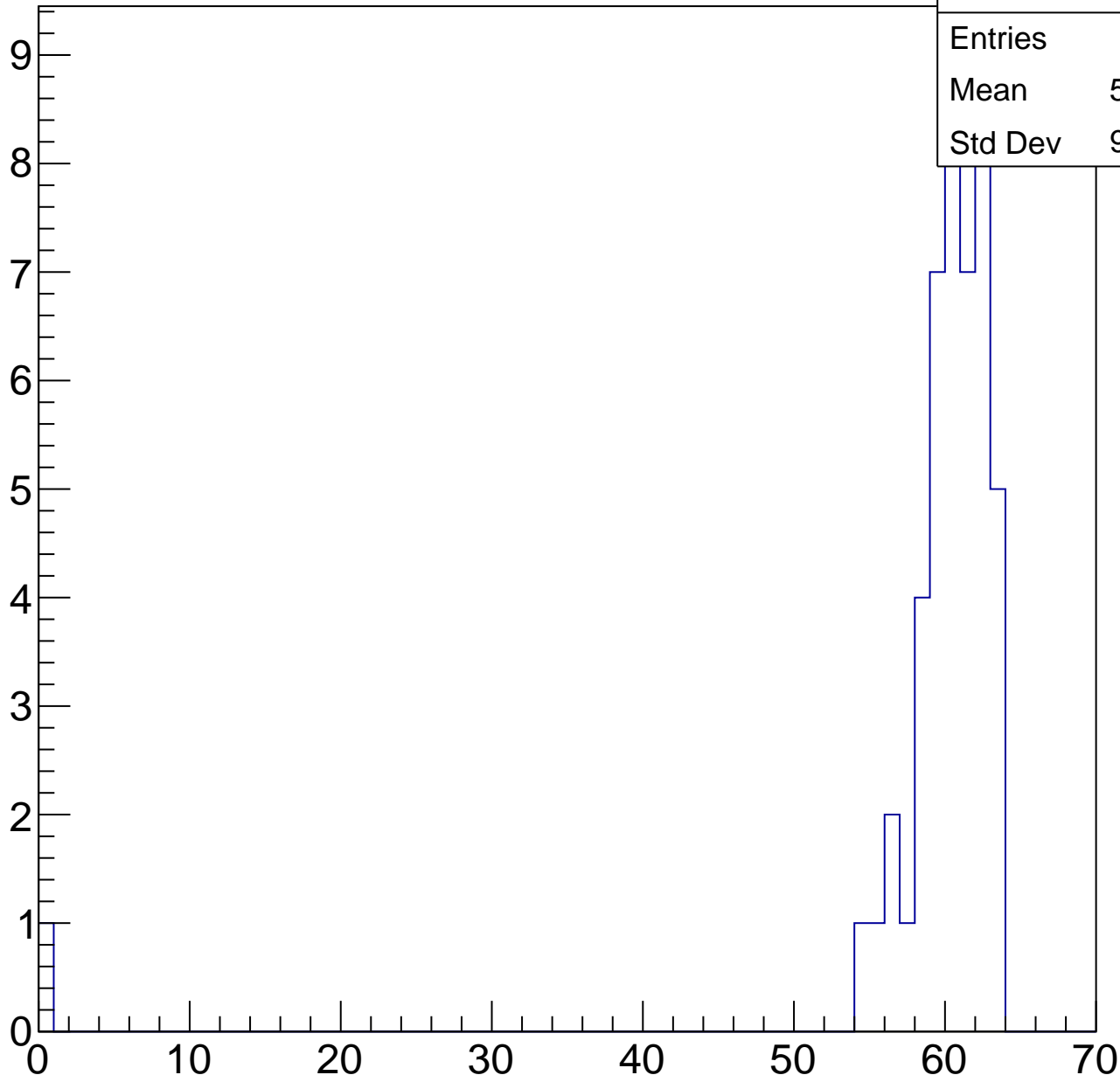
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	46
Mean	58.72
Std Dev	9.009

ampl



# B1L101S, U20-ch79, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U20-ch79, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U20-ch80, adc0

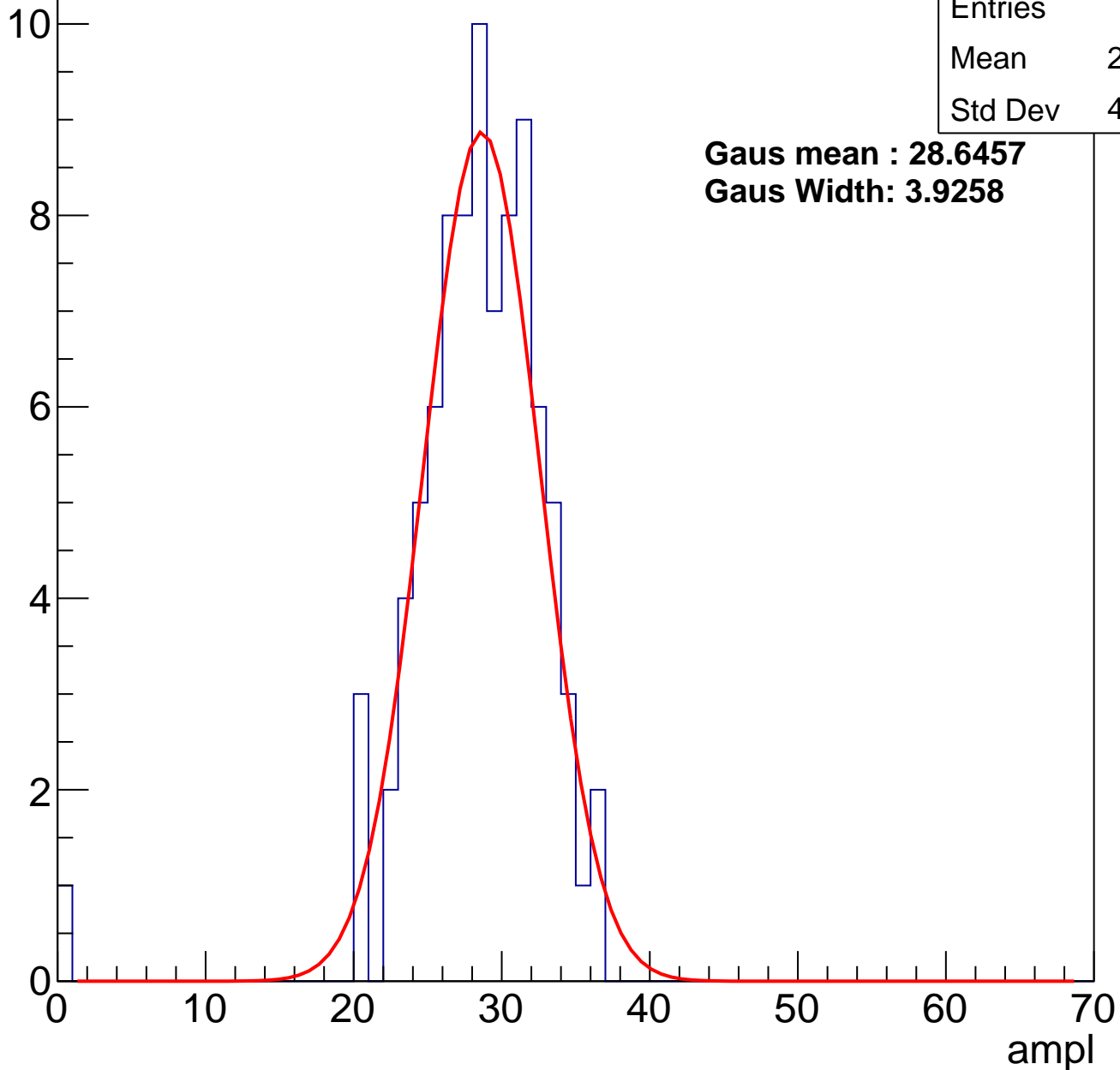
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	88
Mean	27.93
Std Dev	4.704

**Gaus mean : 28.6457**

**Gaus Width: 3.9258**

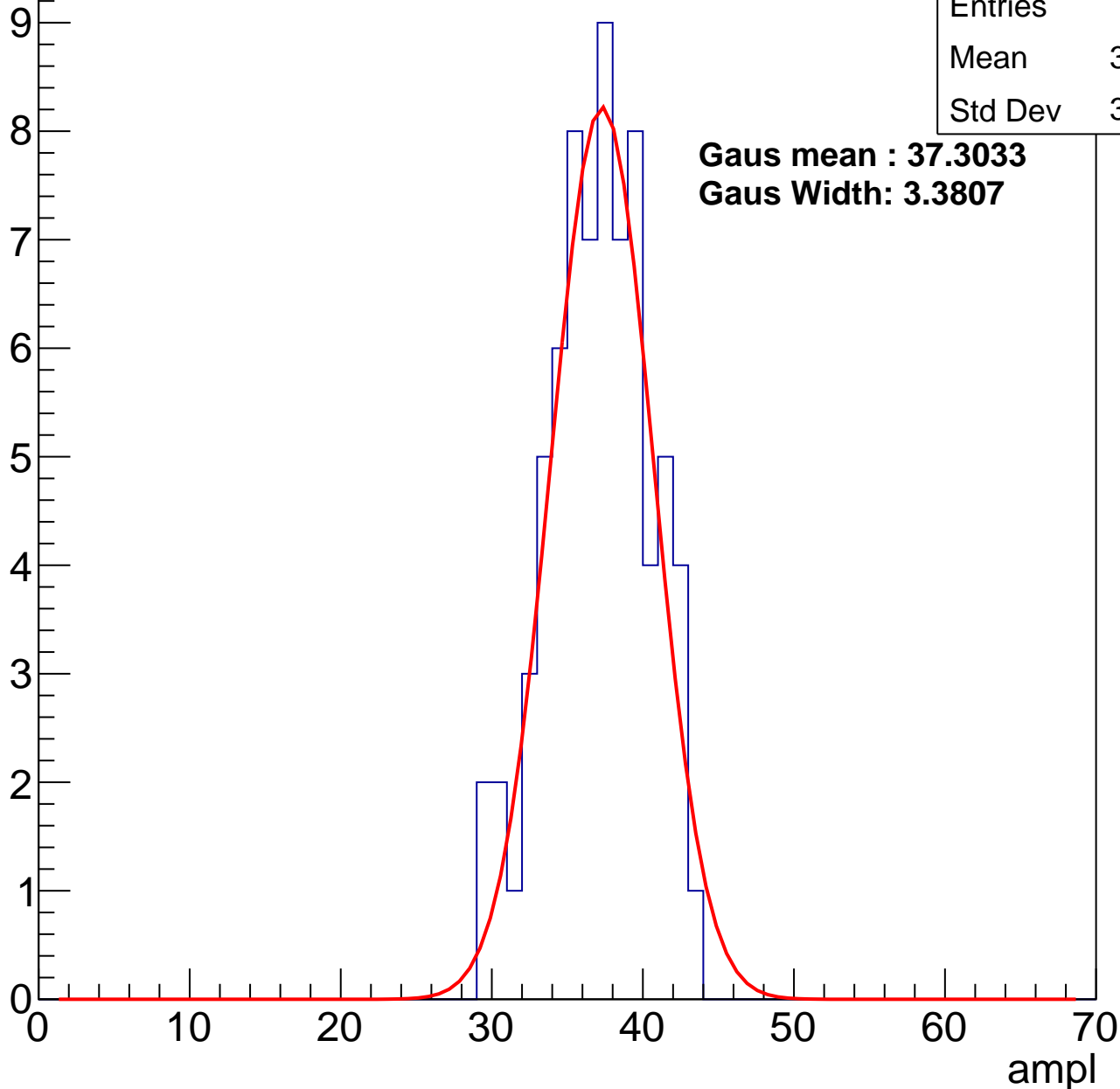
Entry



# B1L101S, U20-ch80, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U20-ch80, adc2

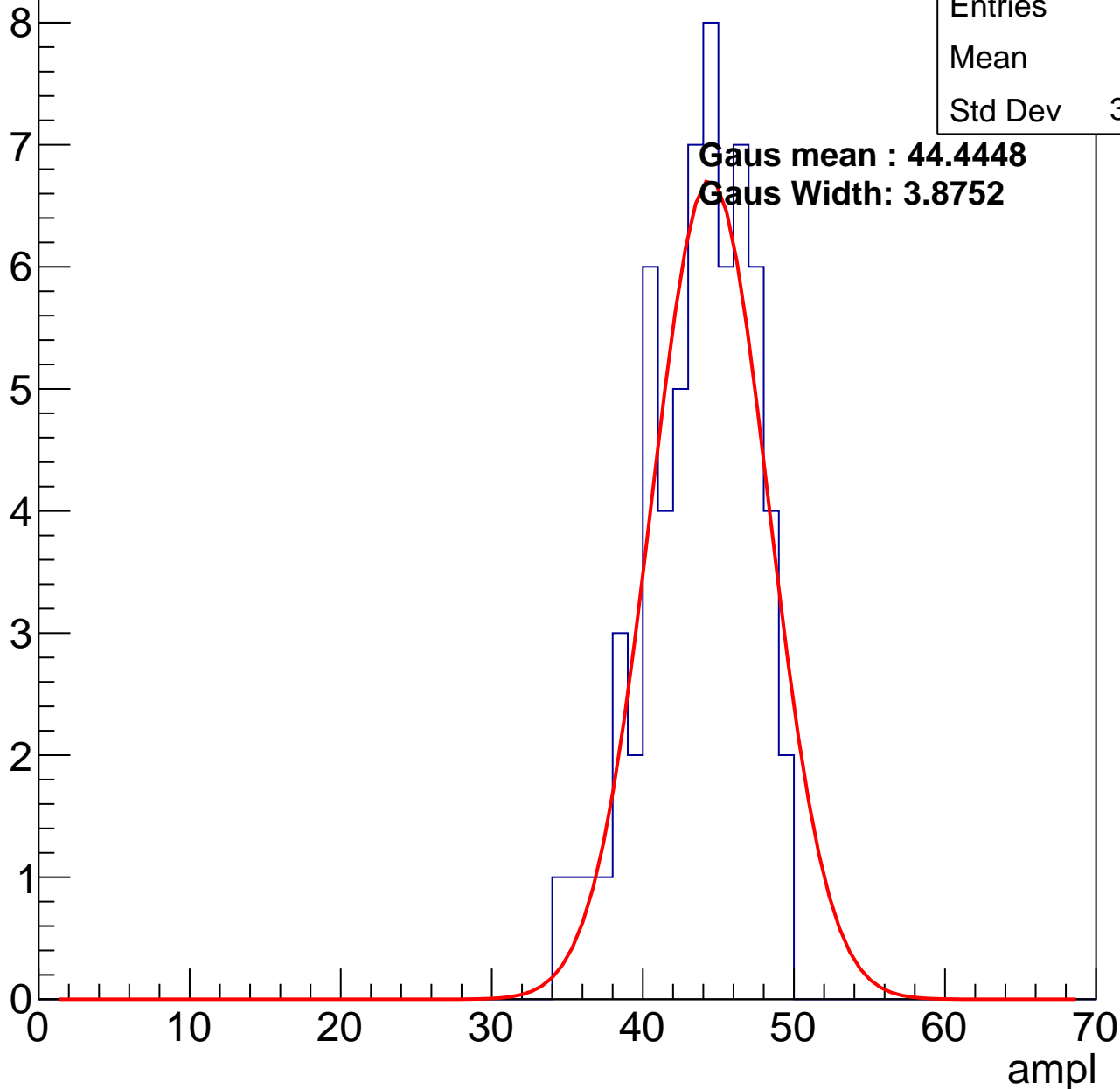
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	43.2
Std Dev	3.474

**Gaus mean : 44.4448**

**Gaus Width: 3.8752**

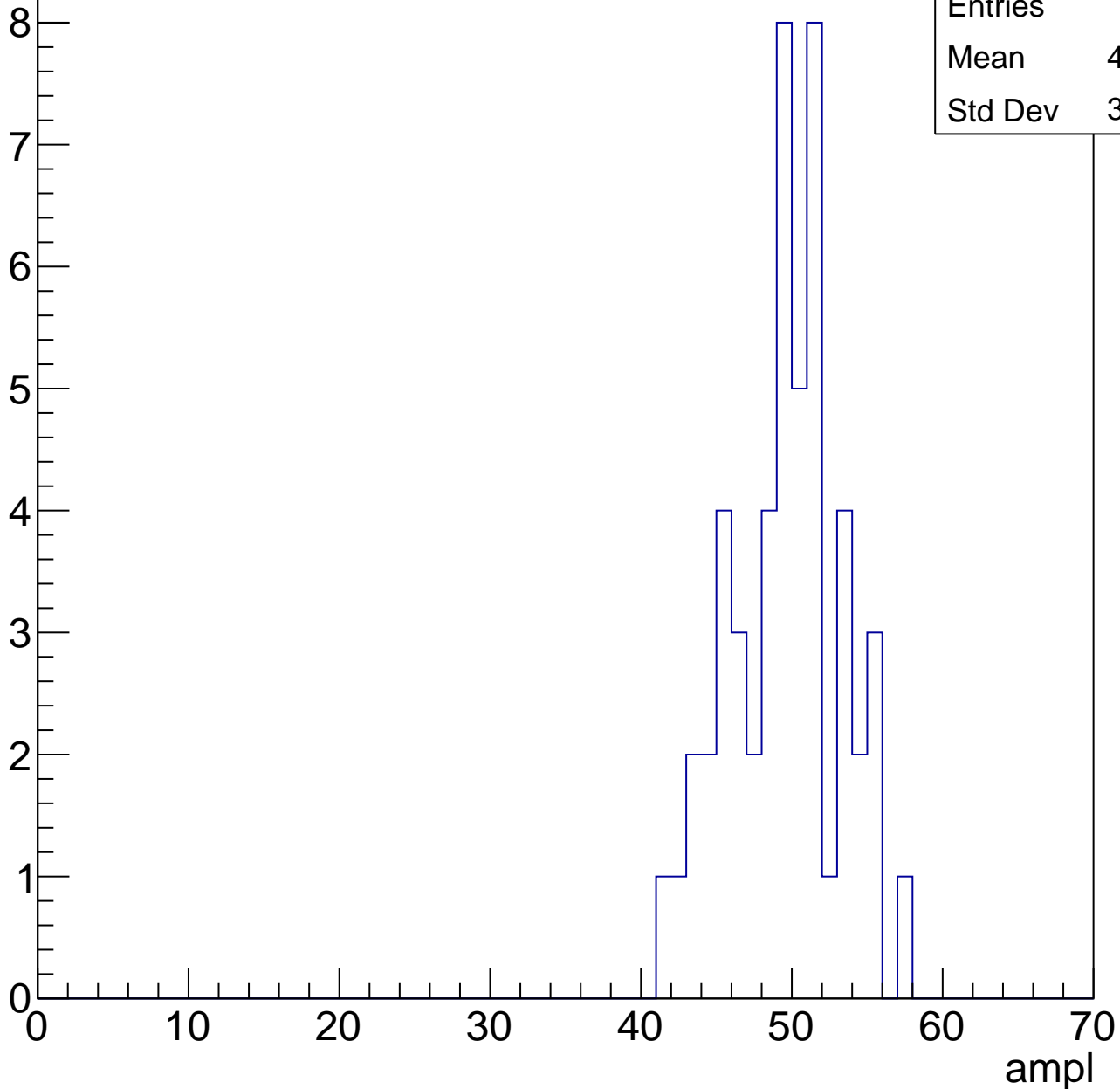


# B1L101S, U20-ch80, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	51
Mean	49.12
Std Dev	3.623

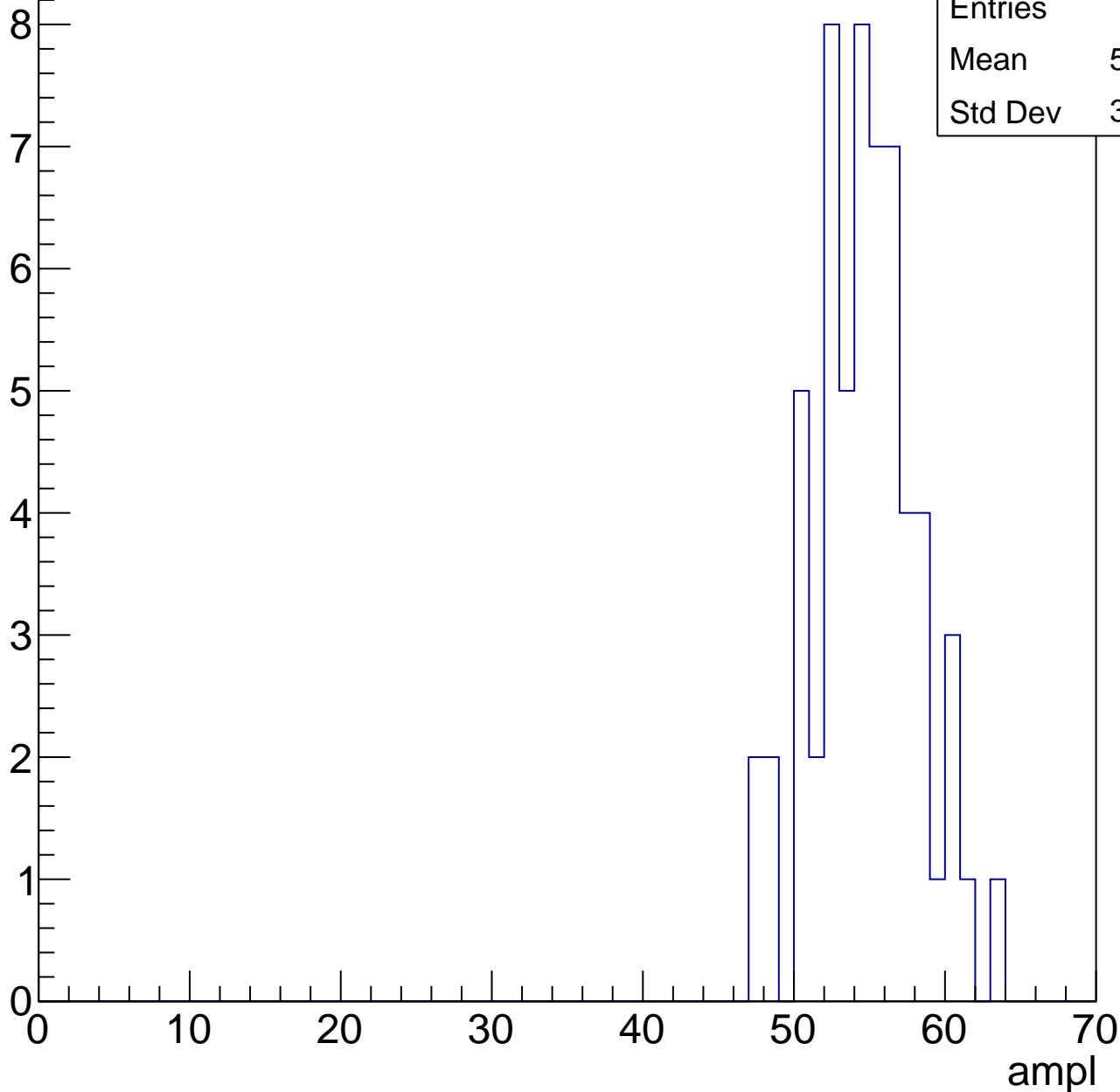


# B1L101S, U20-ch80, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

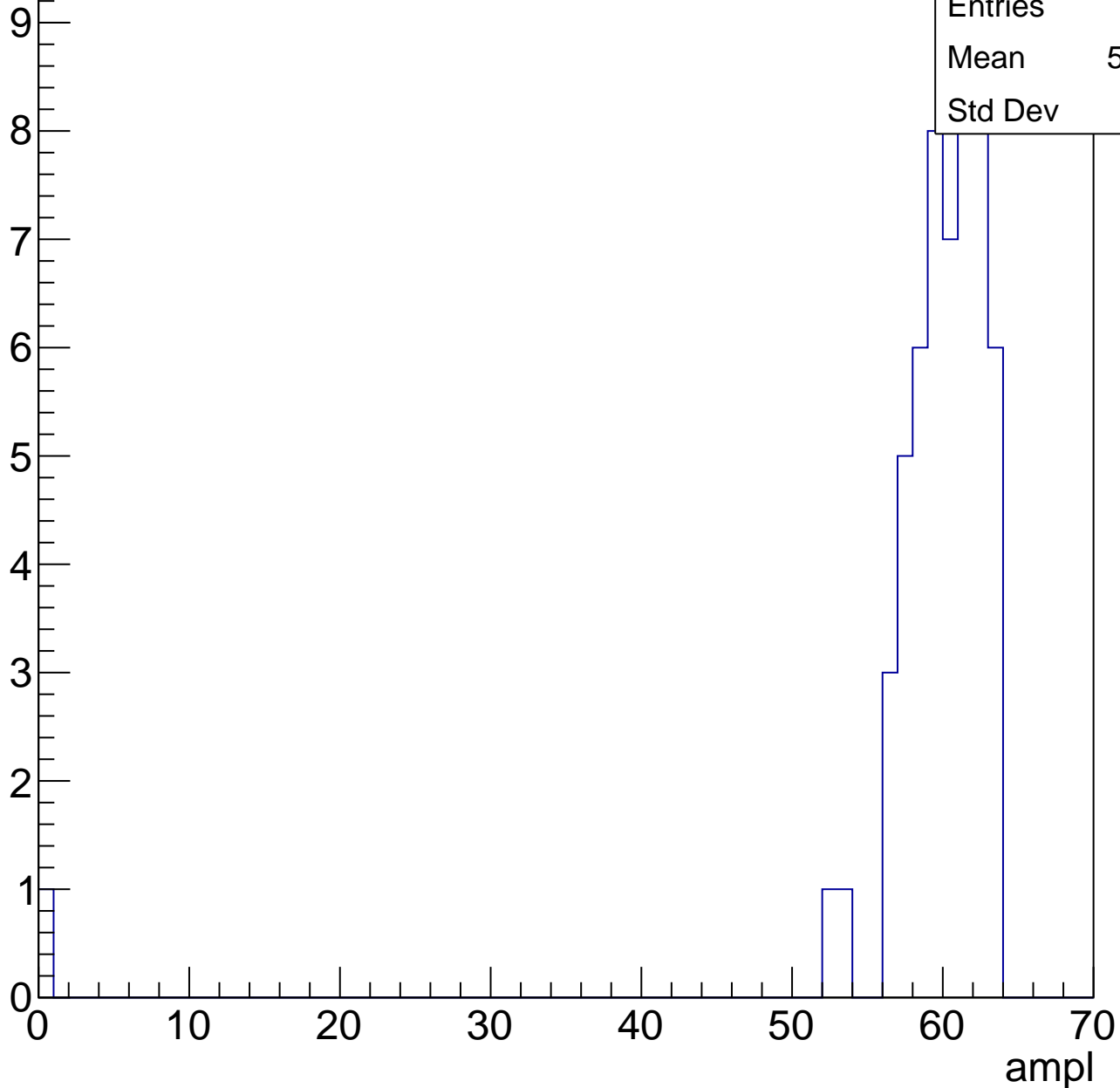
Entries	60
Mean	54.25
Std Dev	3.414



# B1L101S, U20-ch80, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U20-ch80, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U20-ch80, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U20-ch81, adc0

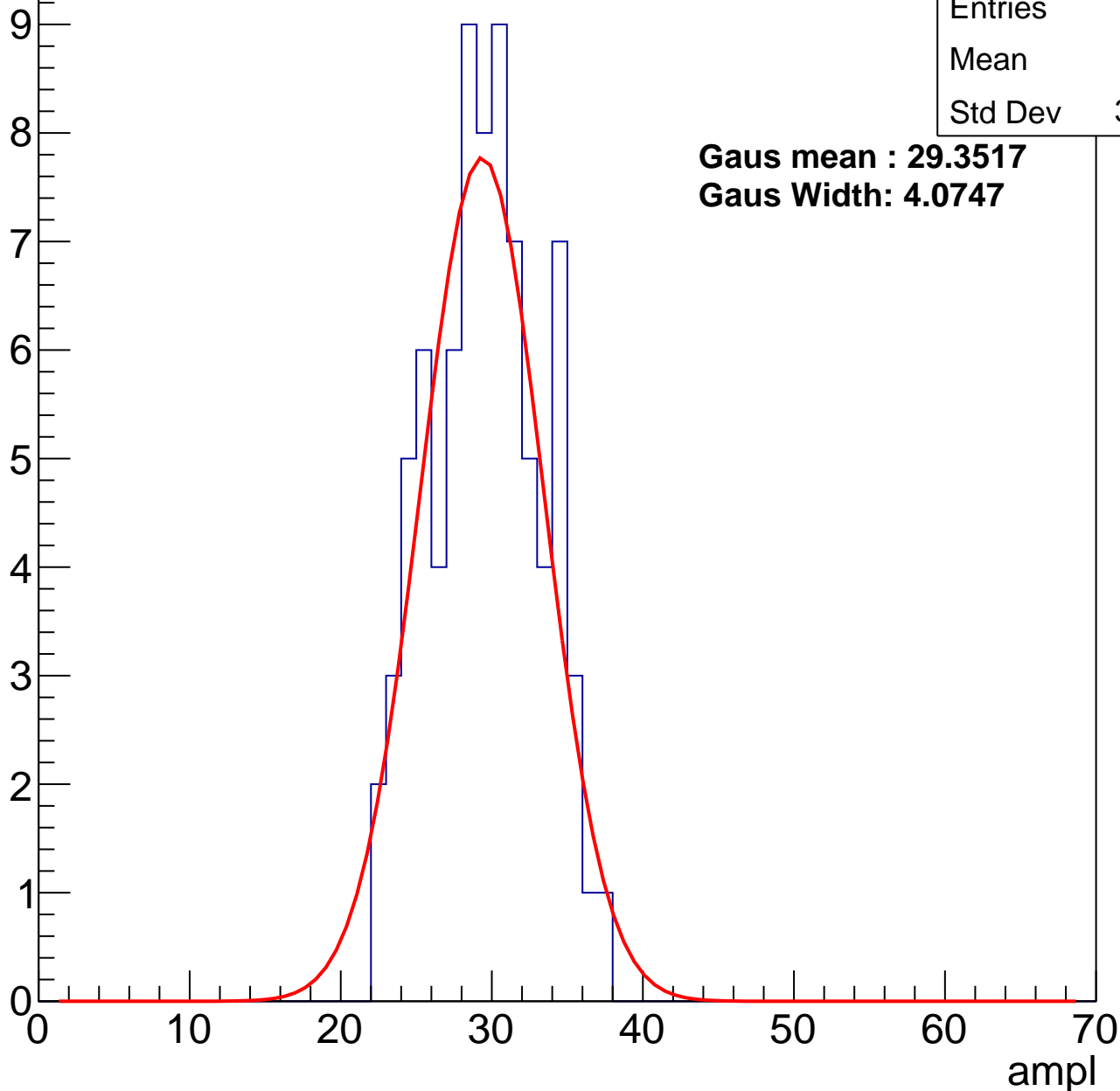
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	80
Mean	29.1
Std Dev	3.601

**Gaus mean : 29.3517**

**Gaus Width: 4.0747**



# B1L101S, U20-ch81, adc1

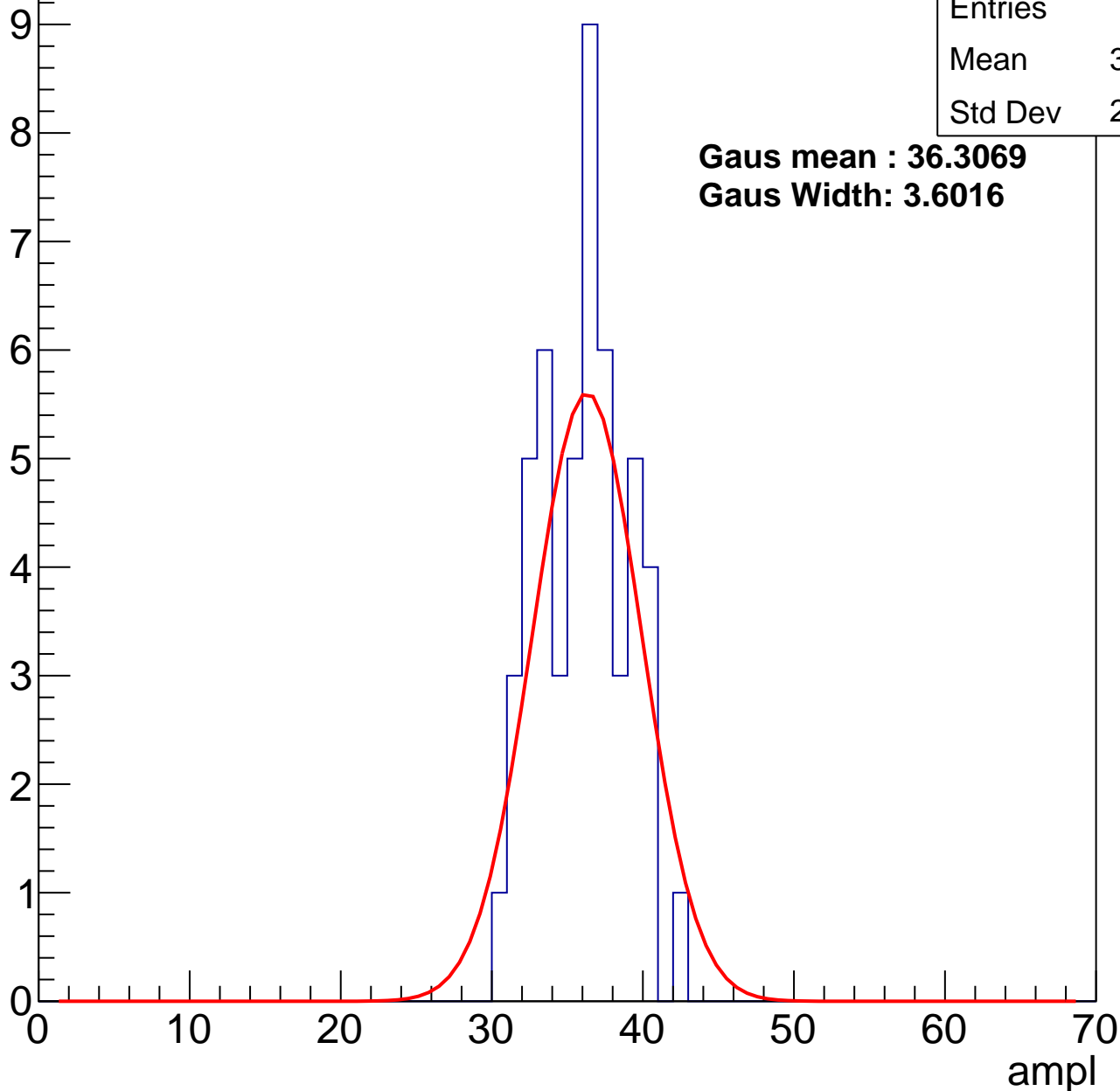
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	51
Mean	35.59
Std Dev	2.857

**Gaus mean : 36.3069**

**Gaus Width: 3.6016**



# B1L101S, U20-ch81, adc2

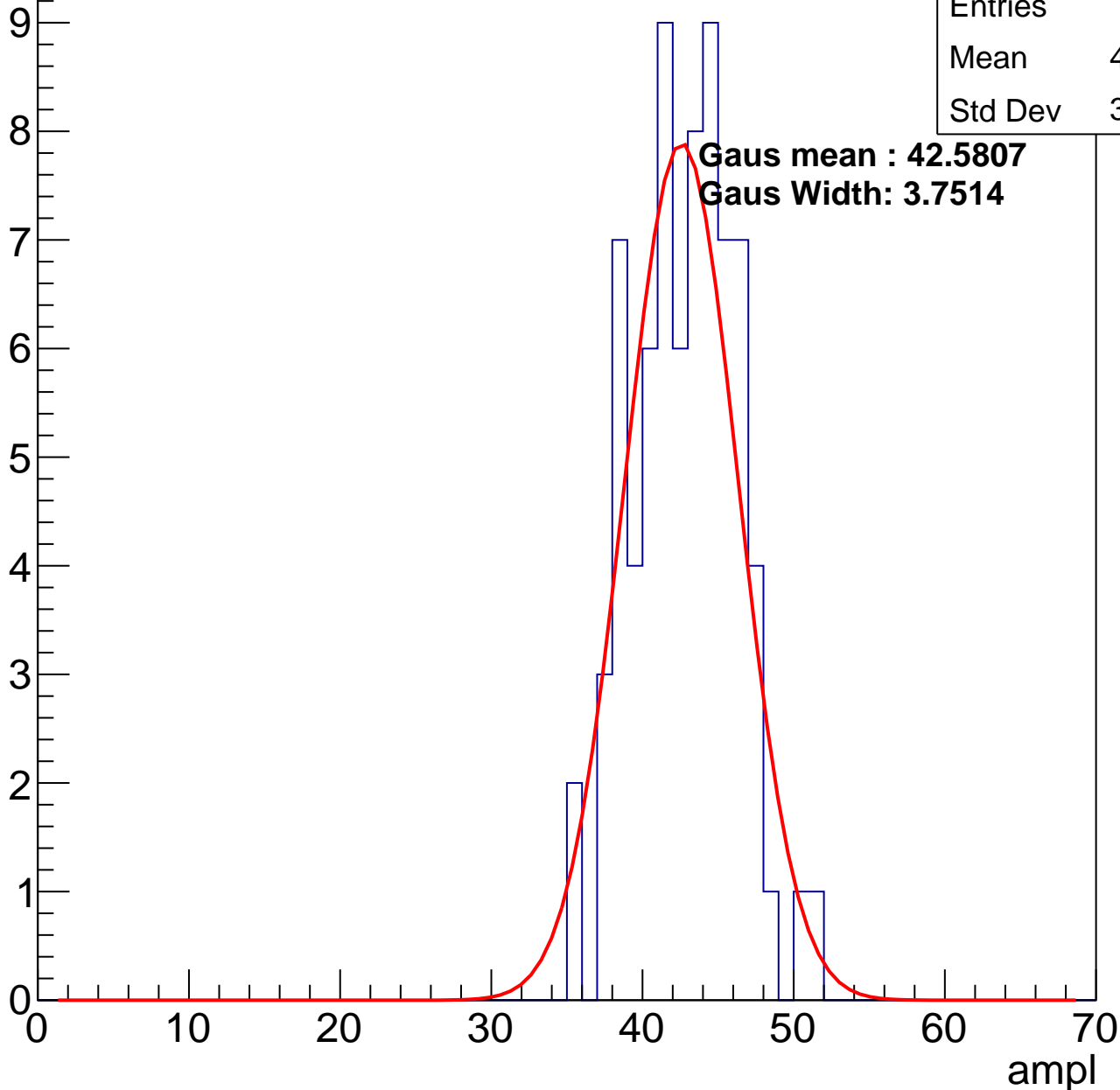
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	75
Mean	42.37
Std Dev	3.354

**Gaus mean : 42.5807**

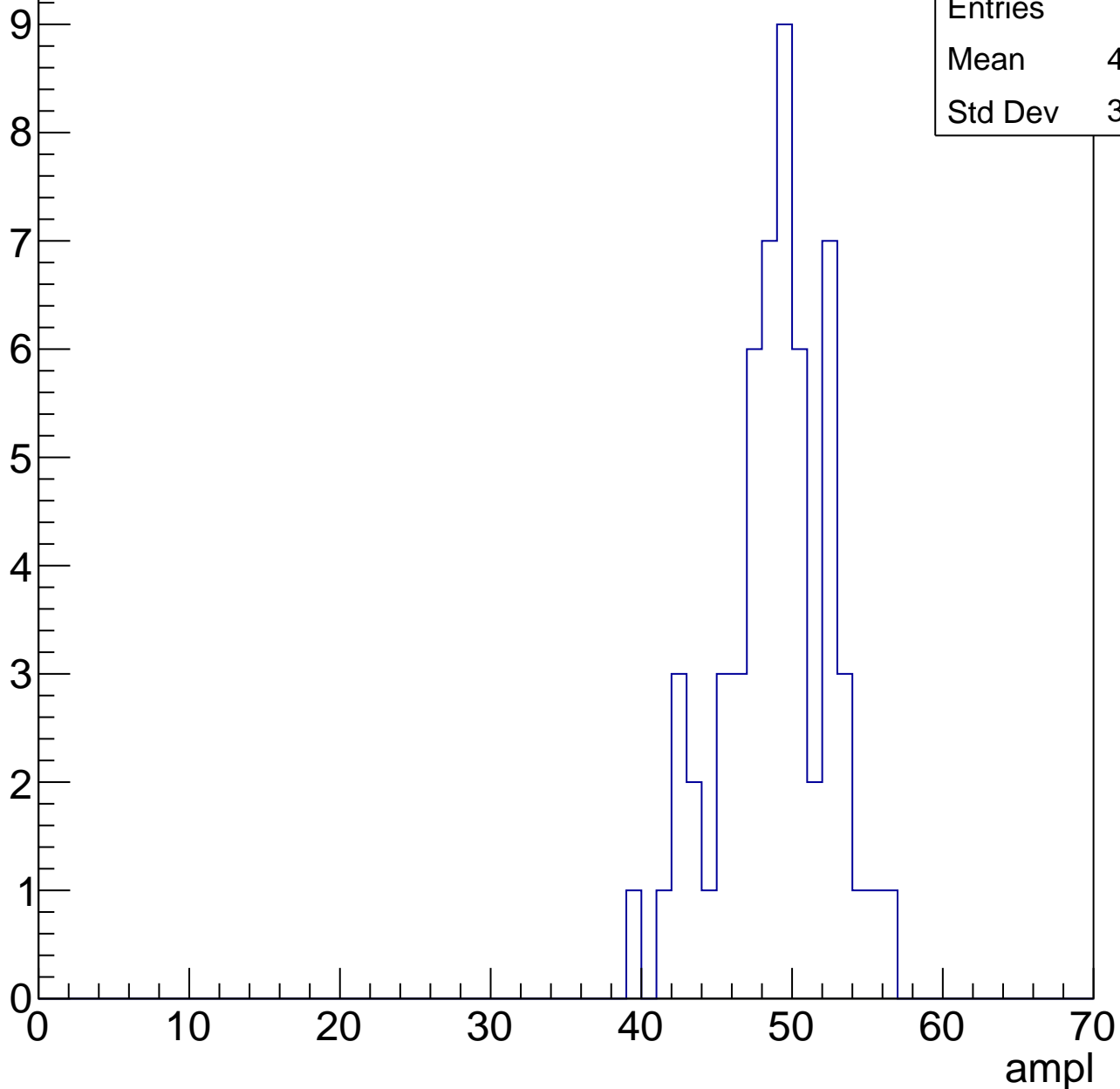
**Gaus Width: 3.7514**



# B1L101S, U20-ch81, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

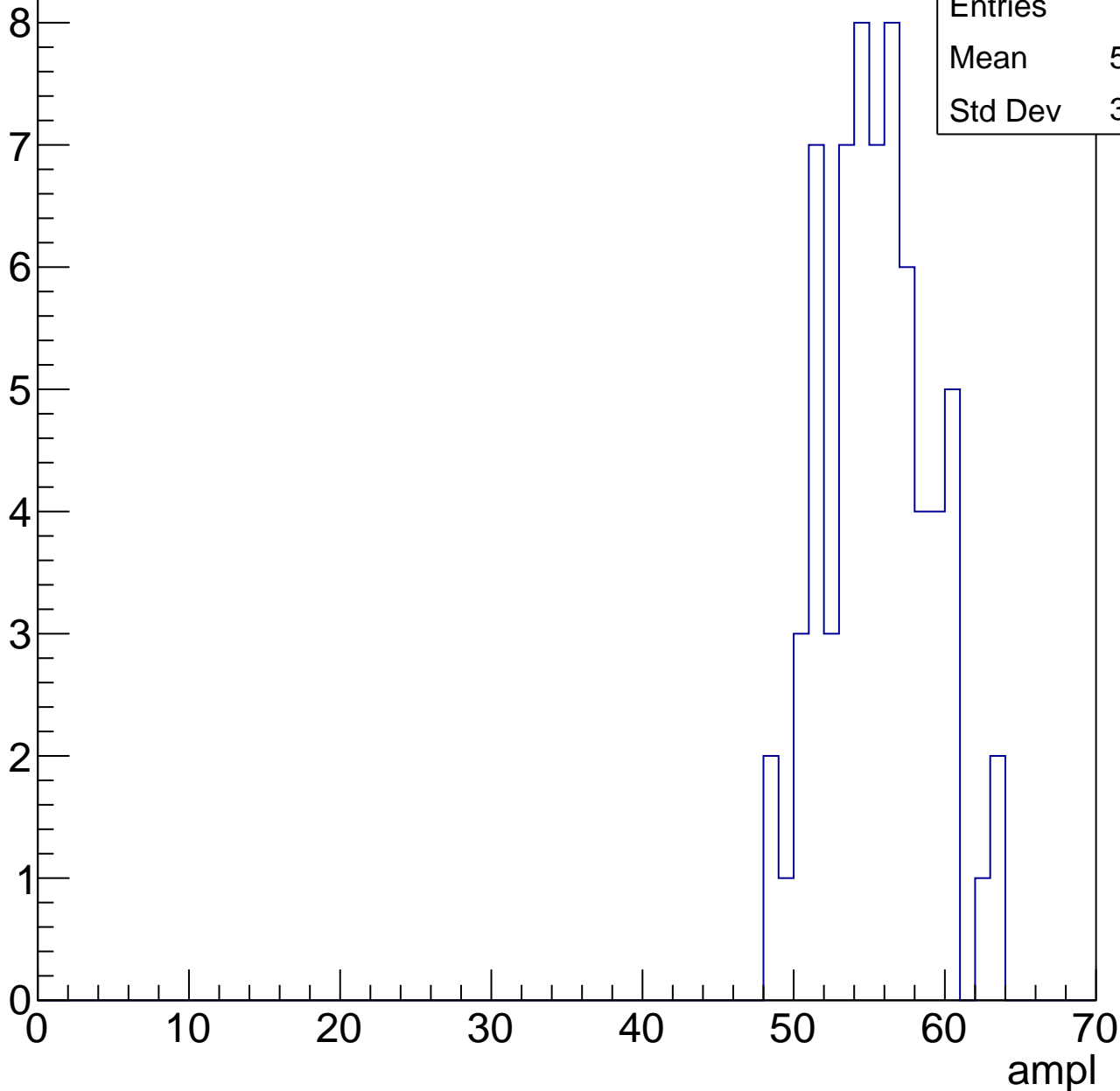


# B1L101S, U20-ch81, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	55.03
Std Dev	3.468

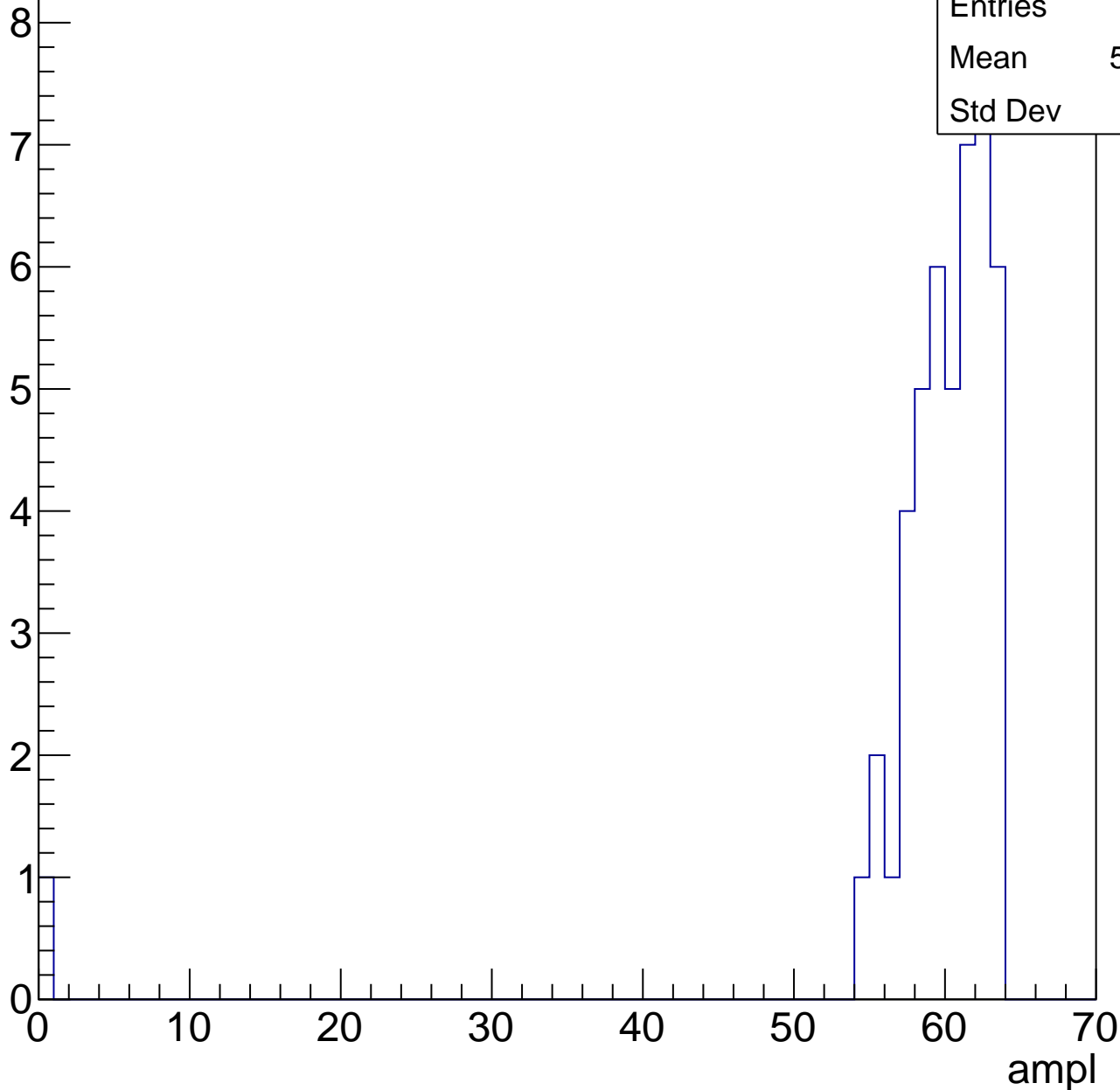


# B1L101S, U20-ch81, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

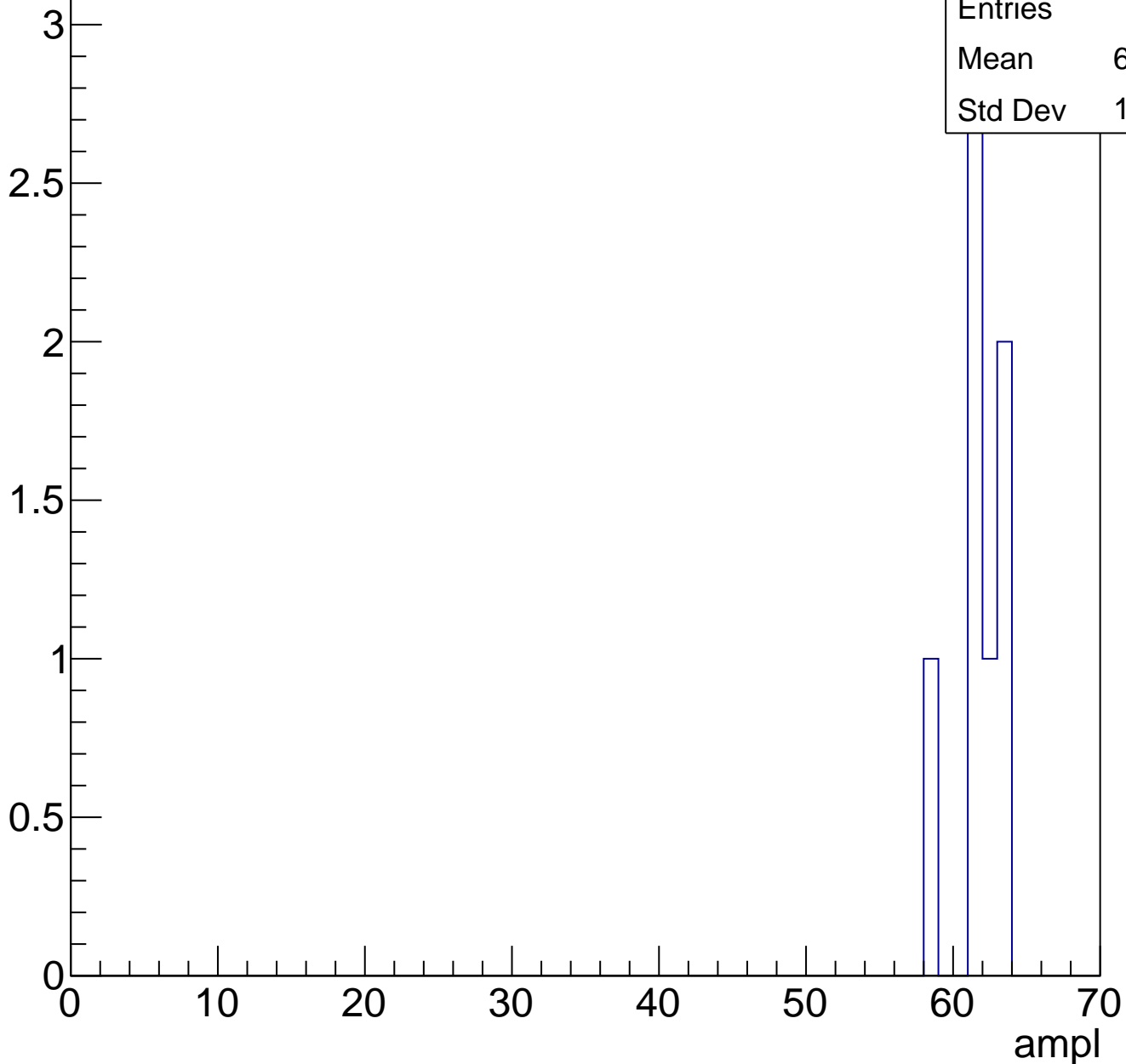
Entries	46
Mean	58.54
Std Dev	9.04



# B1L101S, U20-ch81, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U20-ch81, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U20-ch82, adc0

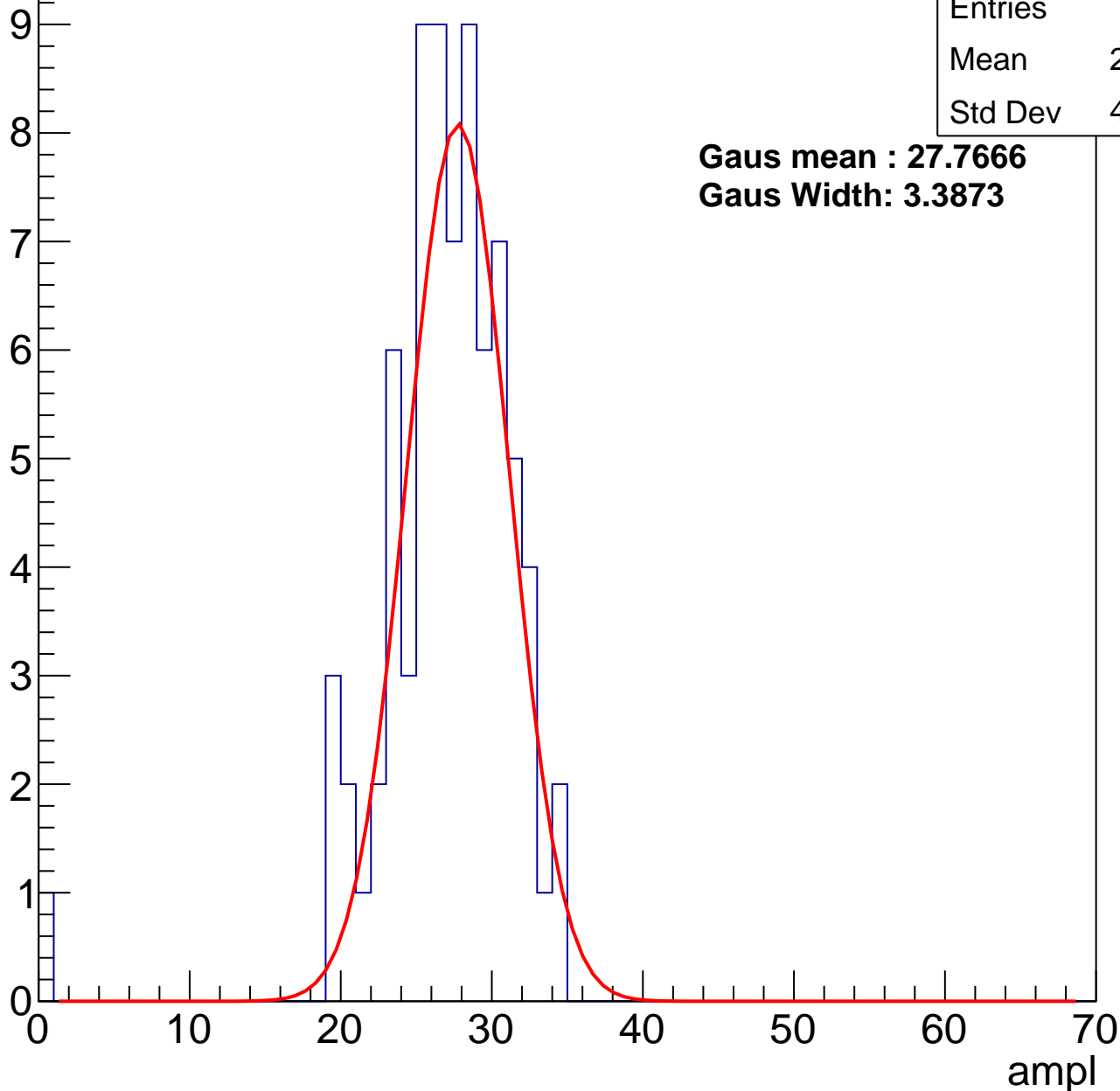
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	77
Mean	26.49
Std Dev	4.648

**Gaus mean : 27.7666**

**Gaus Width: 3.3873**



# B1L101S, U20-ch82, adc1

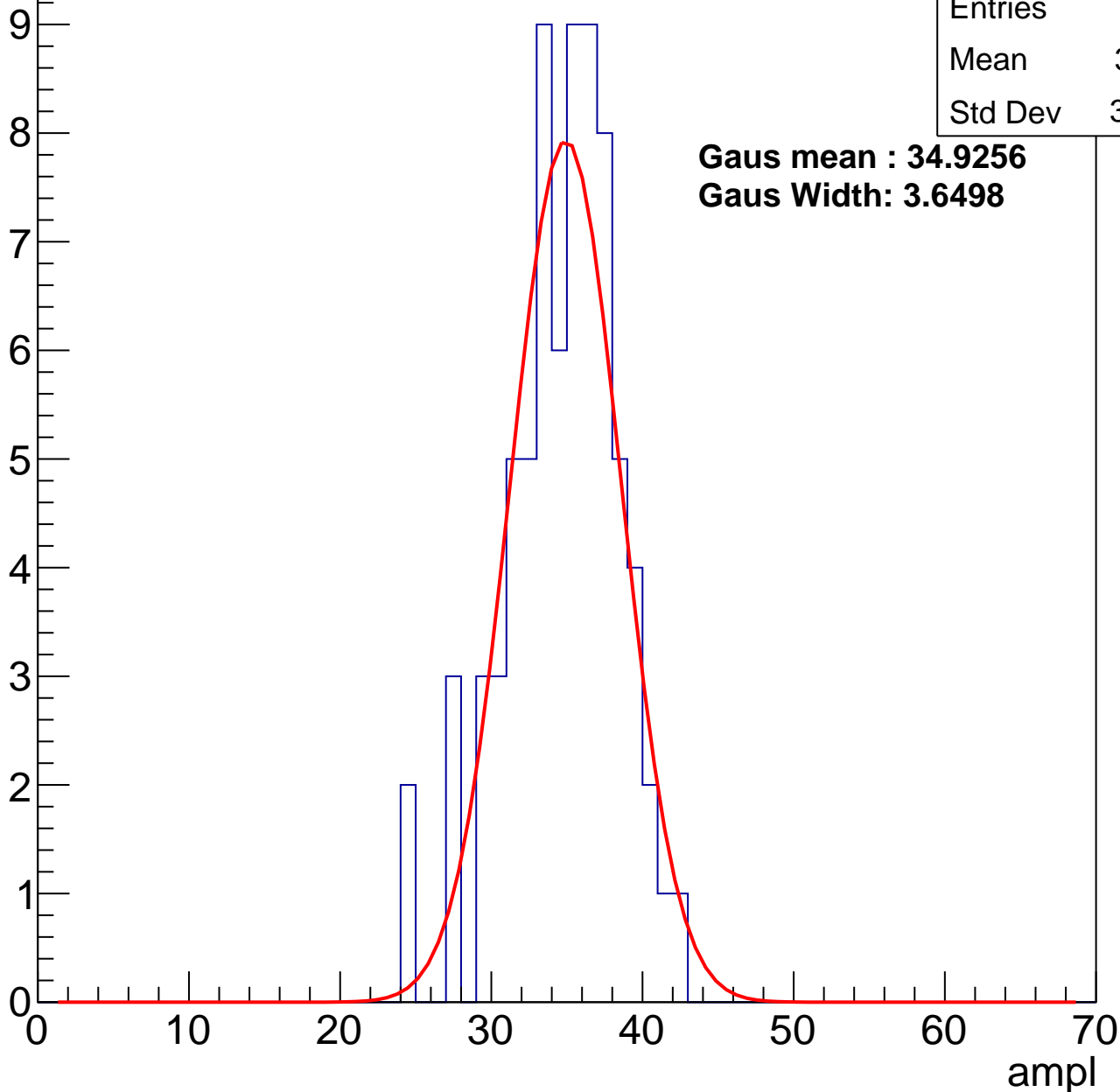
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	75
Mean	34.21
Std Dev	3.692

**Gaus mean : 34.9256**

**Gaus Width: 3.6498**



# B1L101S, U20-ch82, adc2

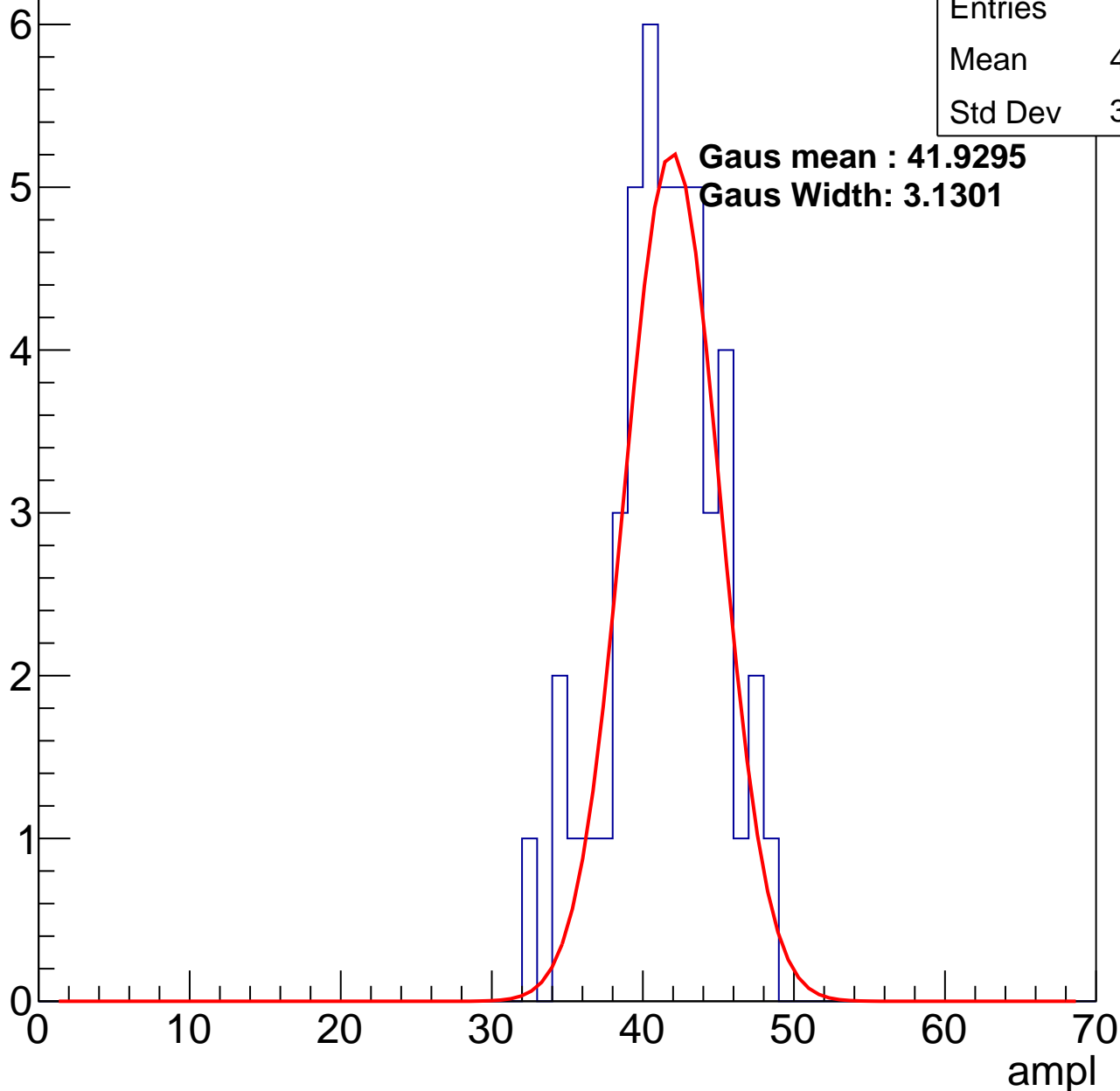
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	46
Mean	41.02
Std Dev	3.523

**Gaus mean : 41.9295**

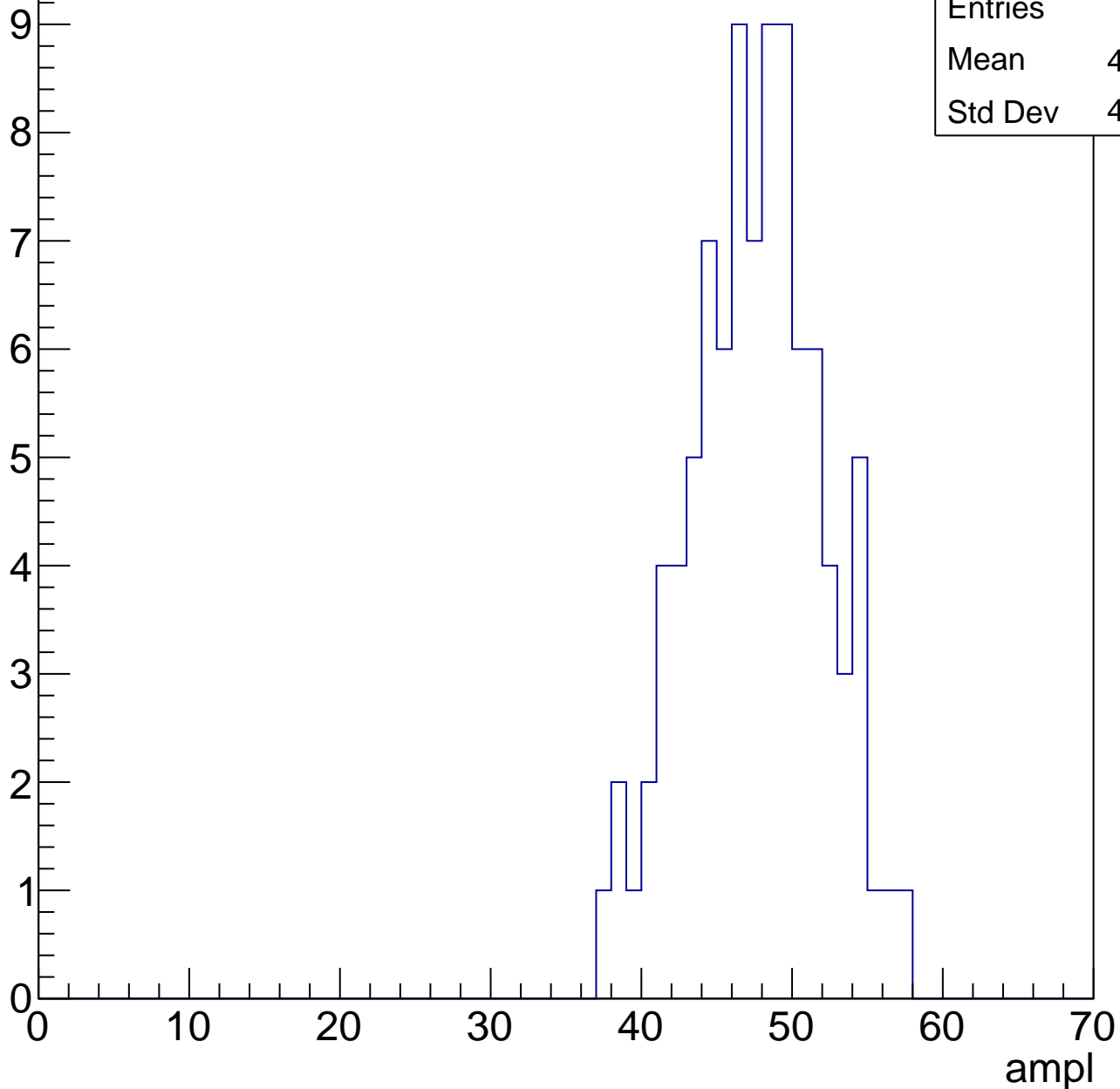
**Gaus Width: 3.1301**



# B1L101S, U20-ch82, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



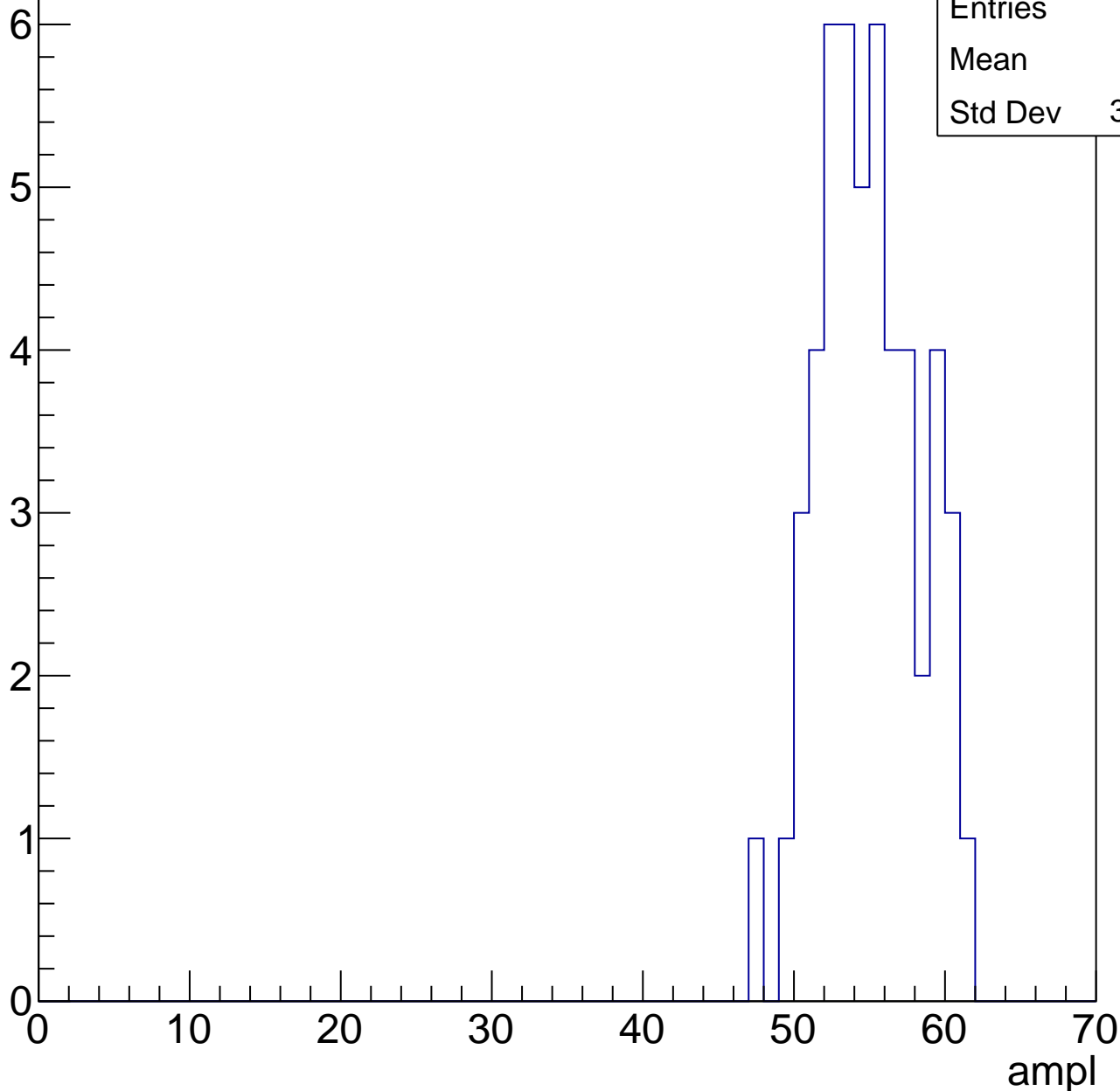
Entries	93
Mean	47.14
Std Dev	4.319

# B1L101S, U20-ch82, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	50
Mean	54.5
Std Dev	3.233



# B1L101S, U20-ch82, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

7

6

5

4

3

2

1

0

Entries 46

Mean 57.48

Std Dev 9.009

0

10

20

30

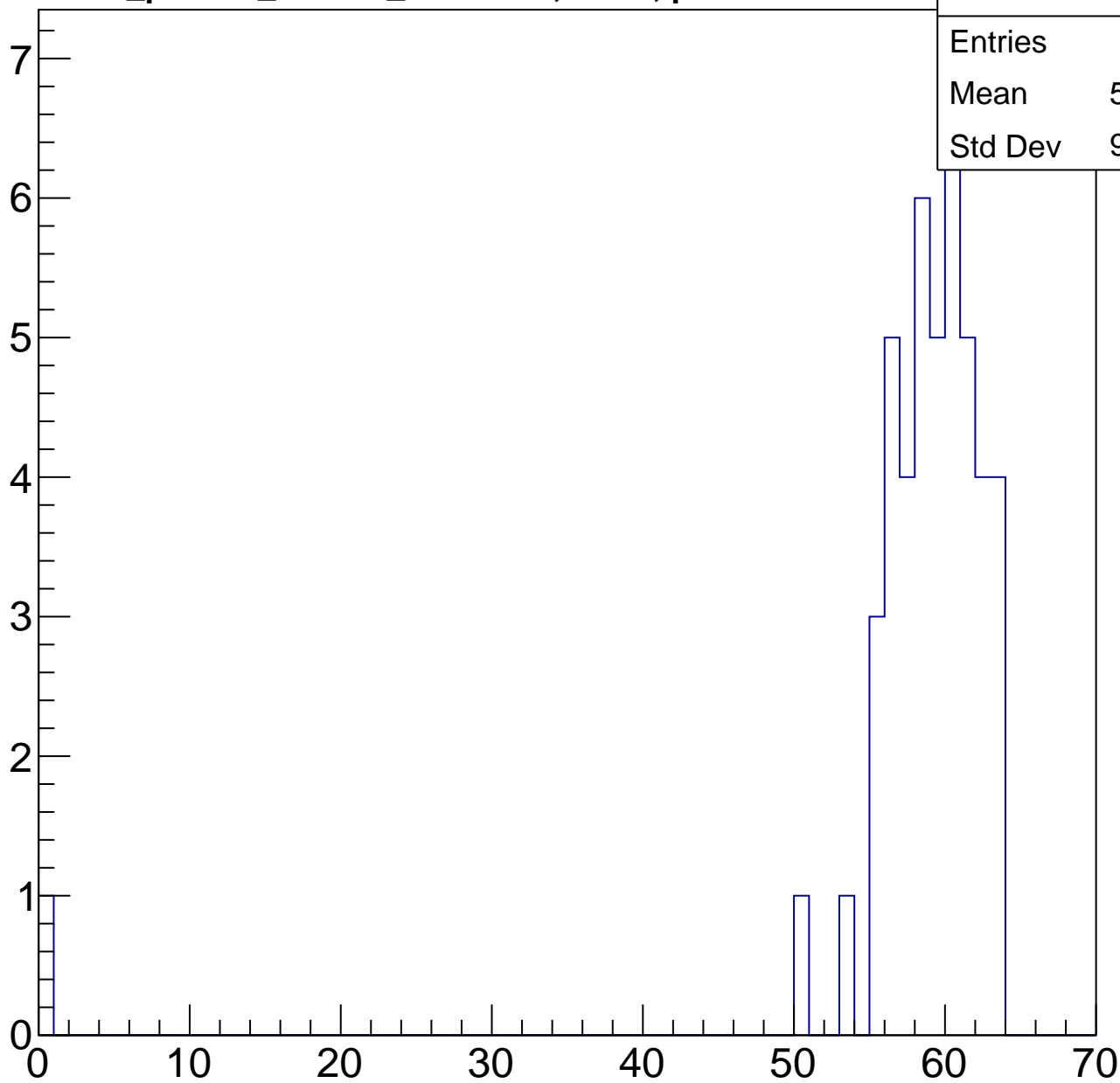
40

50

60

70

ampl

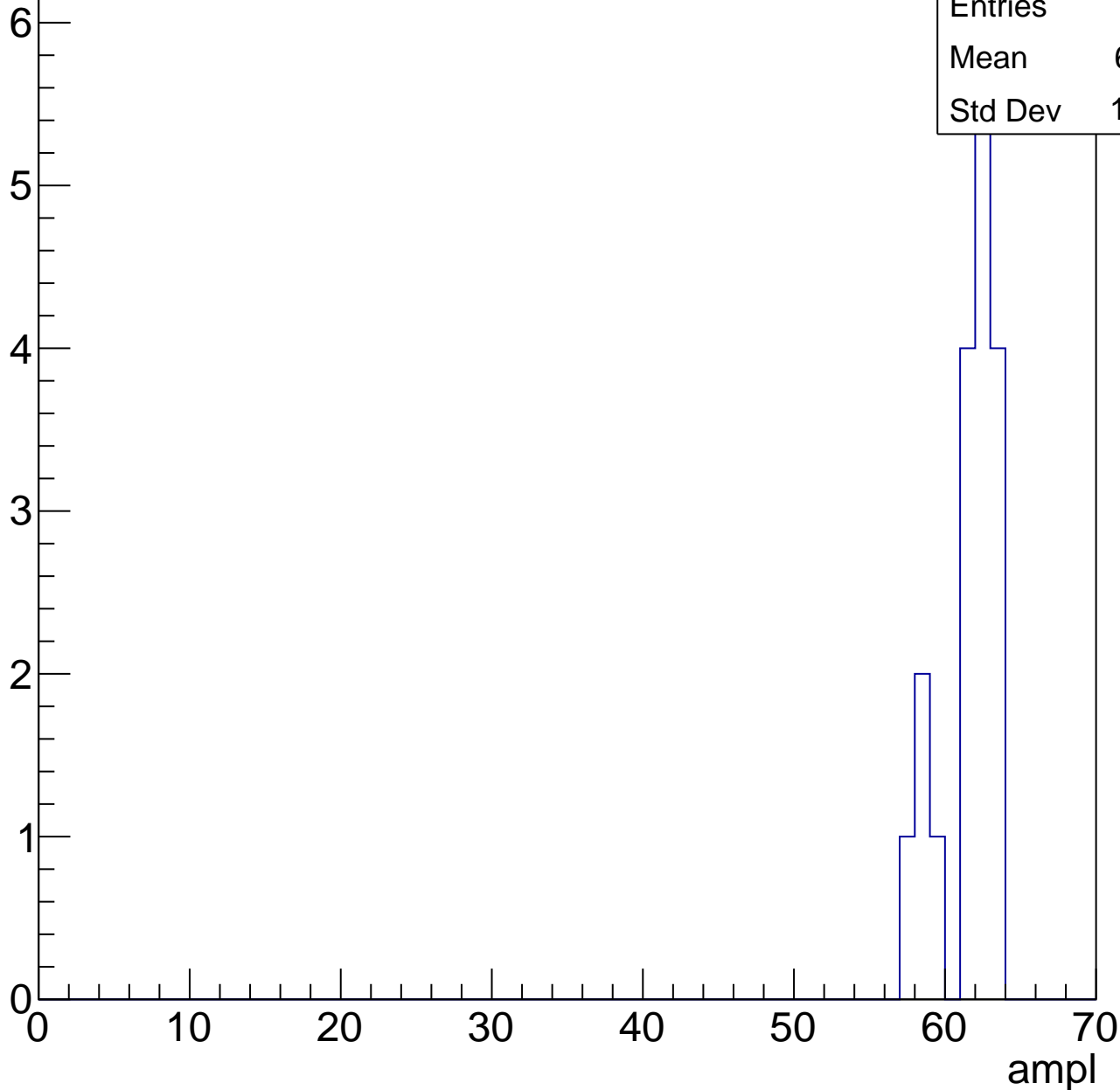


# B1L101S, U20-ch82, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	18
Mean	61.11
Std Dev	1.822

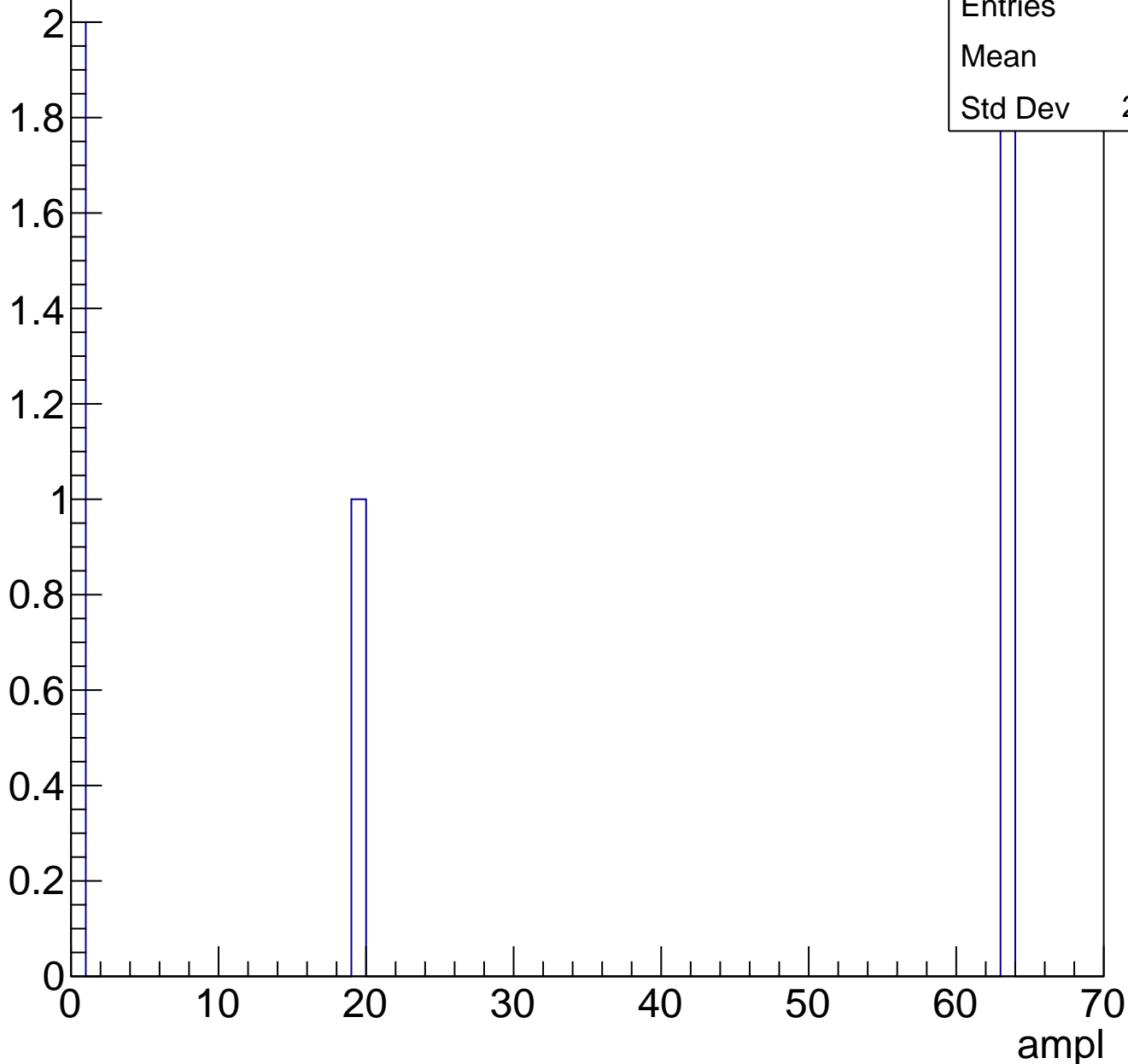




# B1L101S, U20-ch82, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U20-ch83, adc0

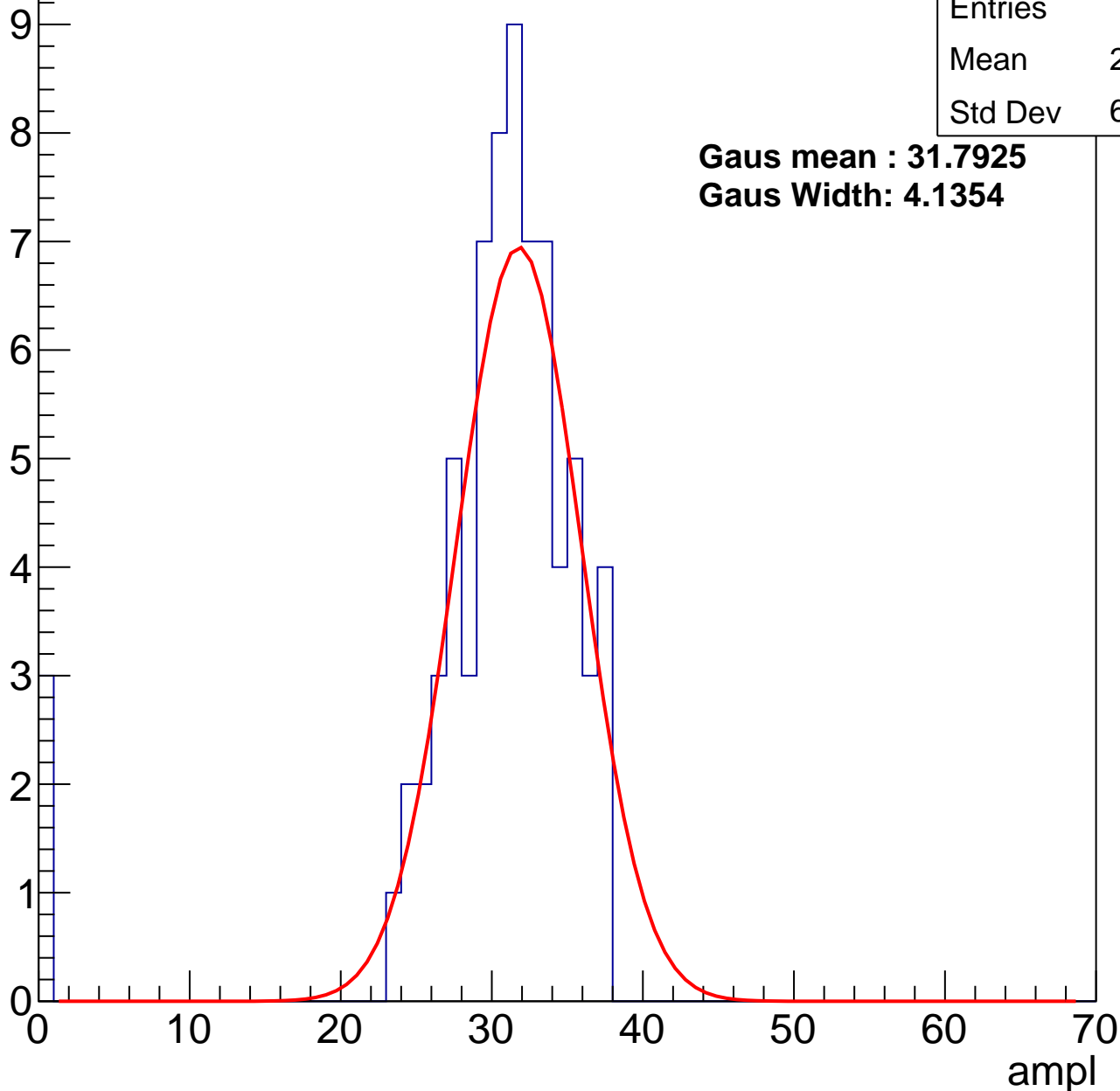
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	73
Mean	29.62
Std Dev	6.989

**Gaus mean : 31.7925**

**Gaus Width: 4.1354**



# B1L101S, U20-ch83, adc1

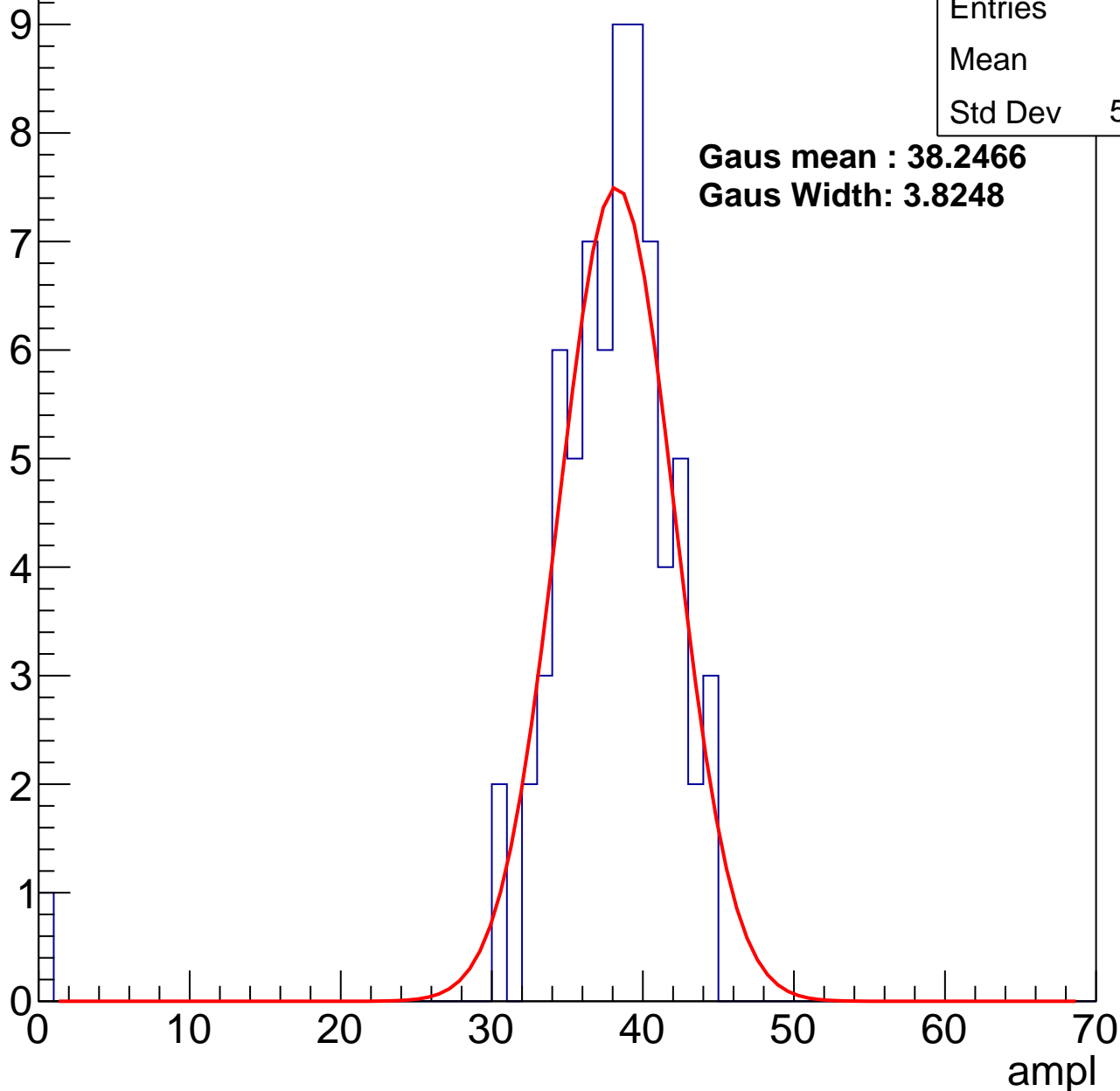
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	71
Mean	37.2
Std Dev	5.515

**Gaus mean : 38.2466**

**Gaus Width: 3.8248**



# B1L101S, U20-ch83, adc2

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	69
Mean	44.96
Std Dev	3.192

**Gaus mean : 45.2706**

**Gaus Width: 3.2384**

Entry

10

8

6

4

2

0

0

10

20

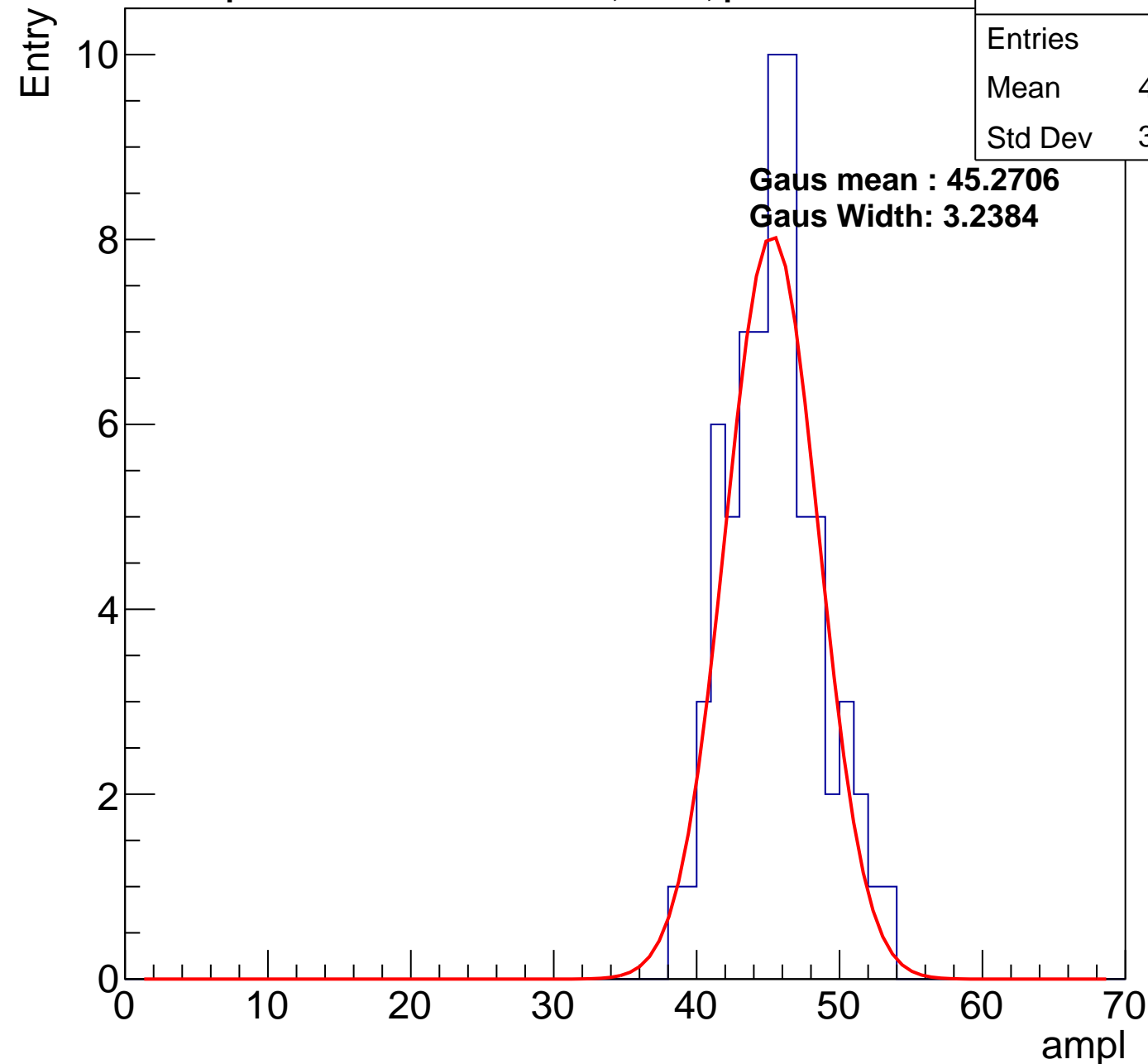
30

40

50

60

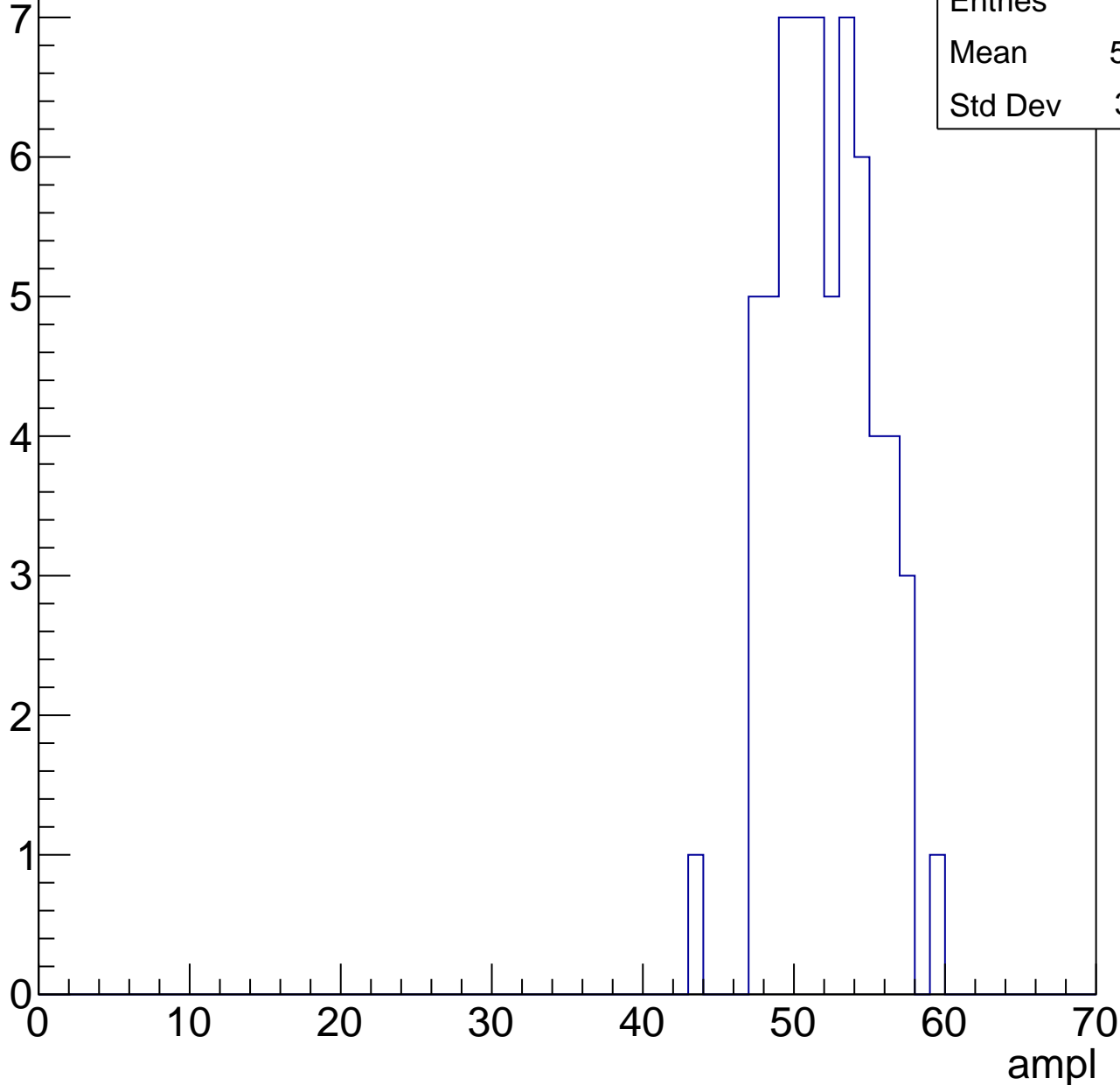
ampl



# B1L101S, U20-ch83, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

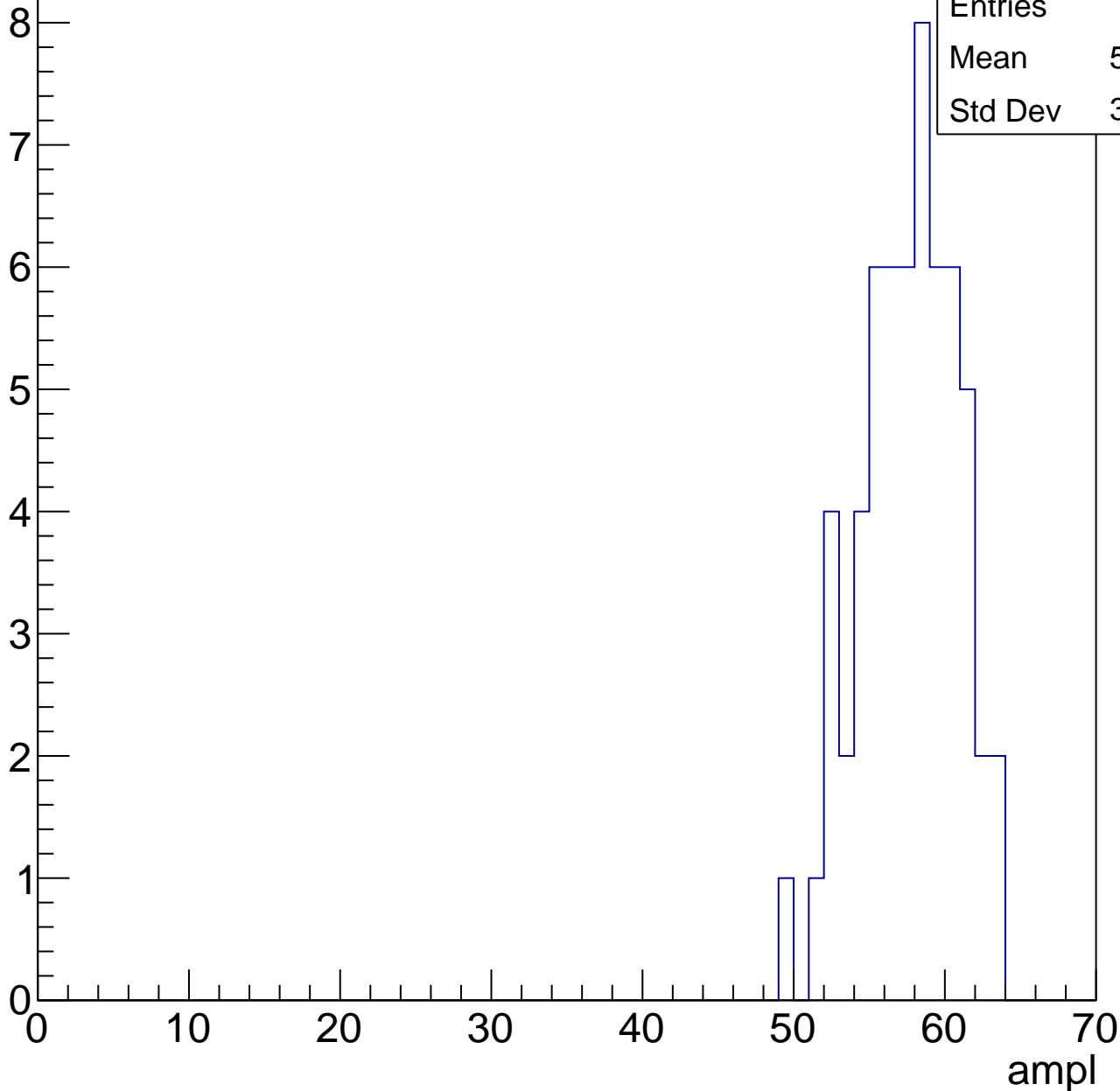


# B1L101S, U20-ch83, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	59
Mean	57.14
Std Dev	3.149

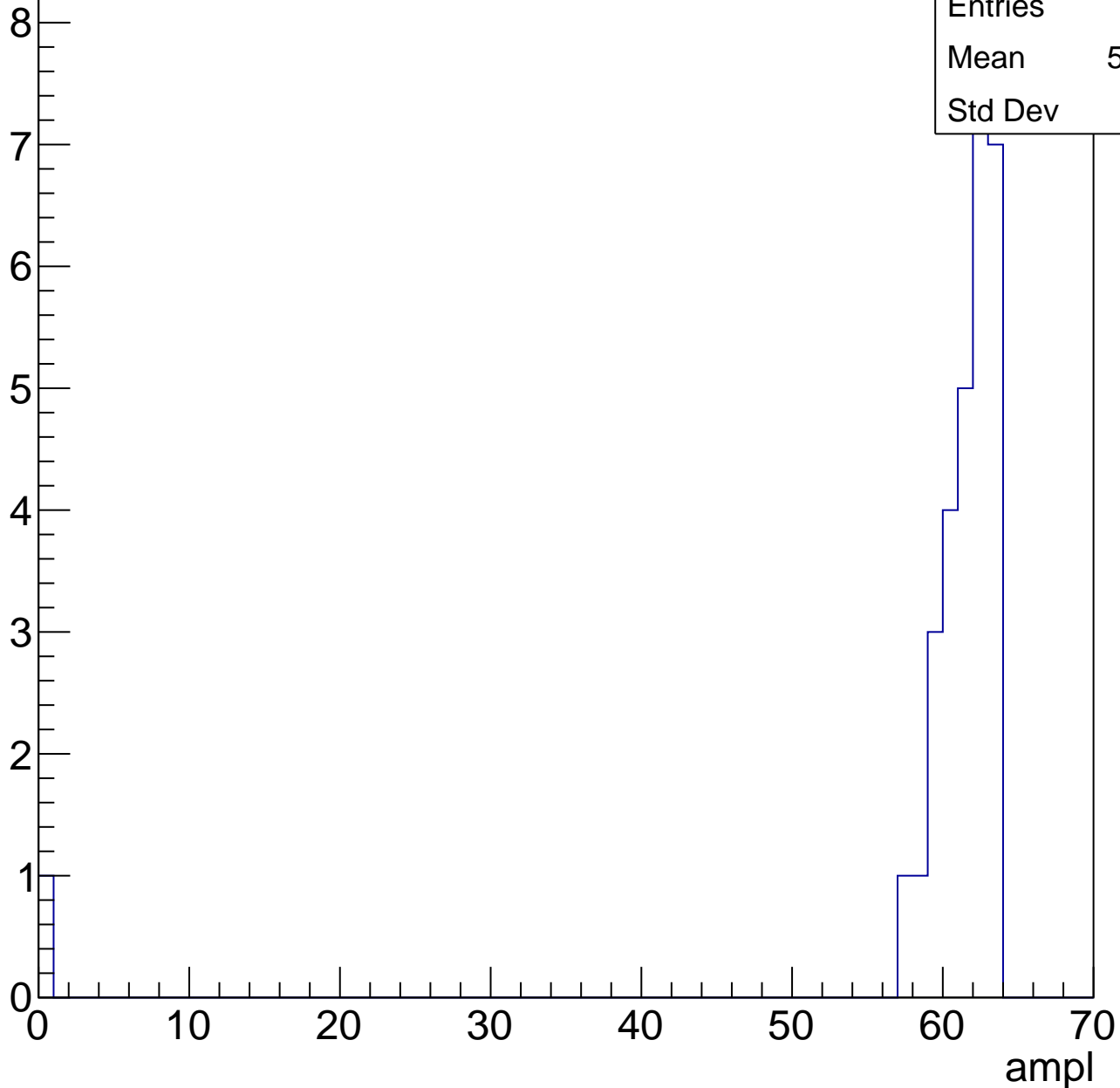


# B1L101S, U20-ch83, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

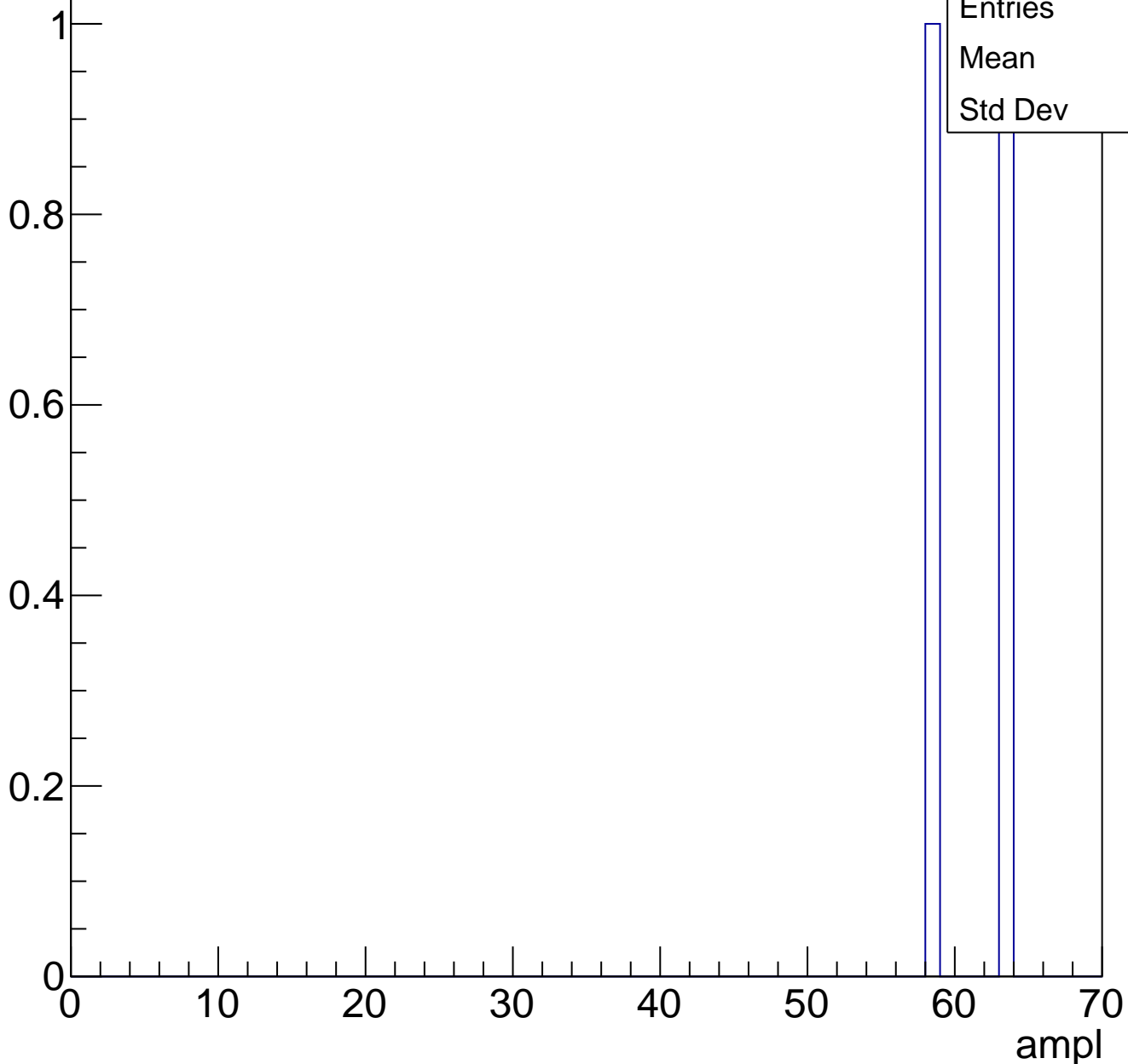
Entries	30
Mean	59.13
Std Dev	11.1



# B1L101S, U20-ch83, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U20-ch83, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U20-ch84, adc0

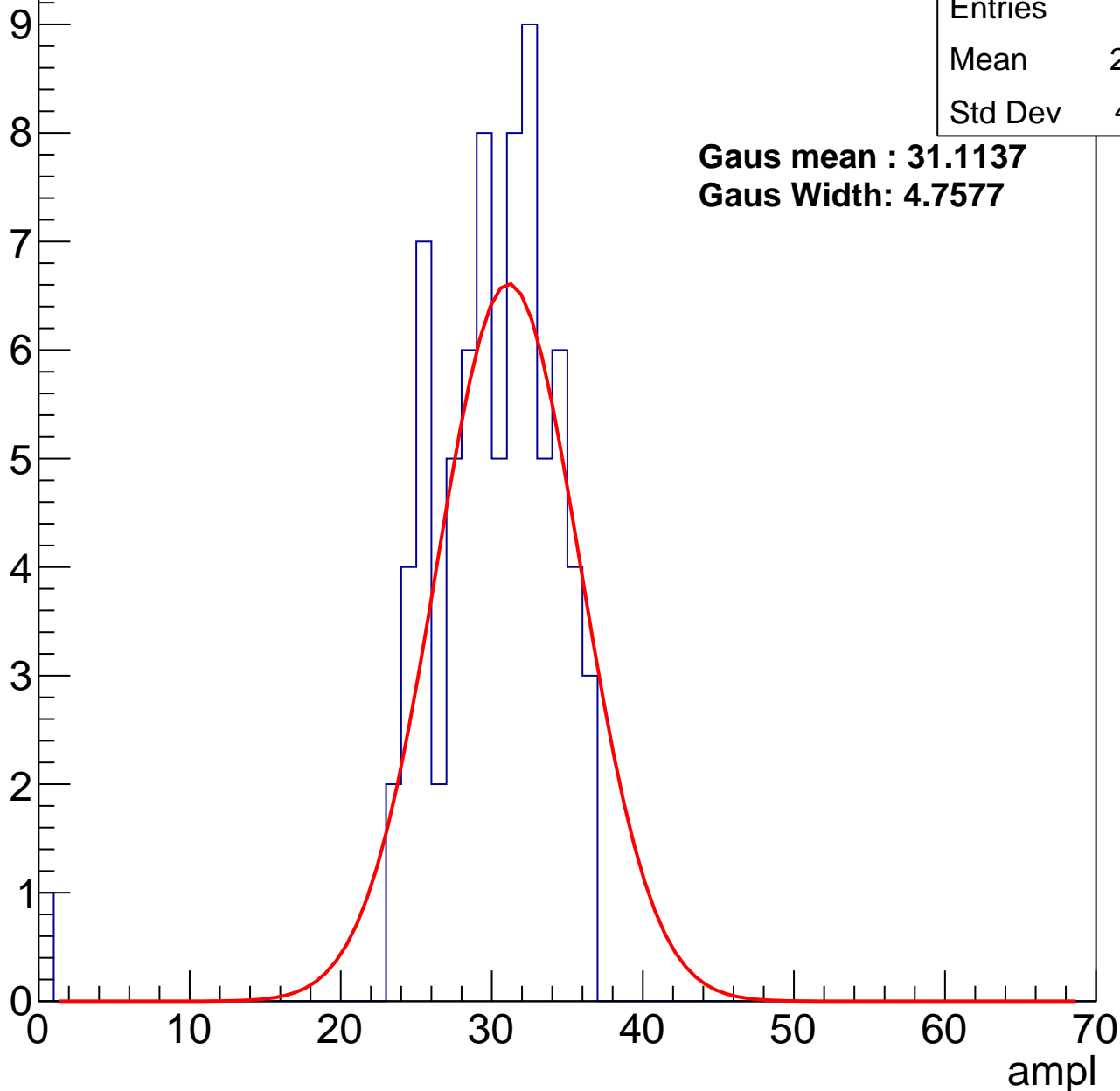
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	75
Mean	29.43
Std Dev	4.891

**Gaus mean : 31.1137**

**Gaus Width: 4.7577**



# B1L101S, U20-ch84, adc1

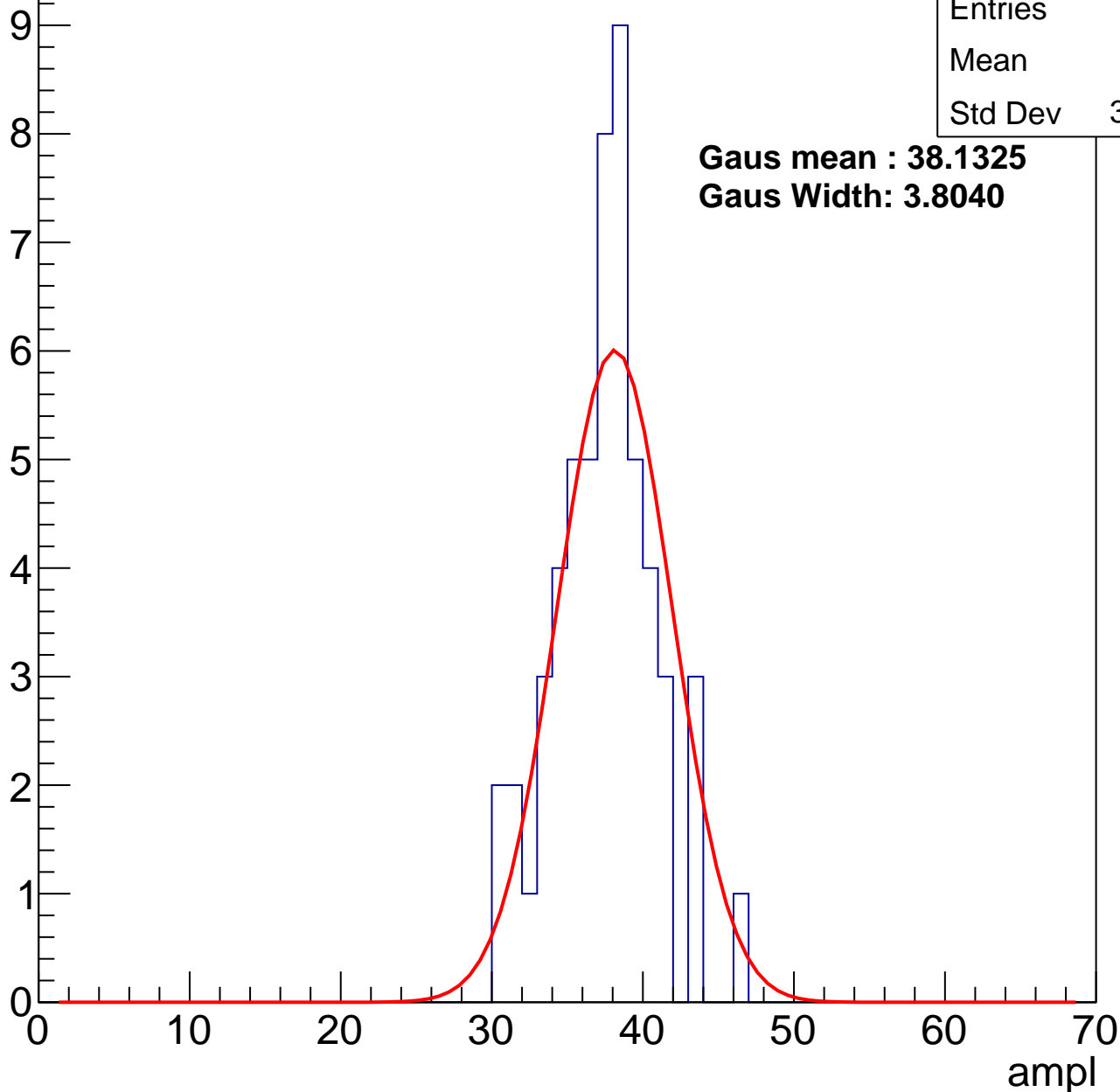
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	55
Mean	37
Std Dev	3.319

**Gaus mean : 38.1325**

**Gaus Width: 3.8040**



# B1L101S, U20-ch84, adc2

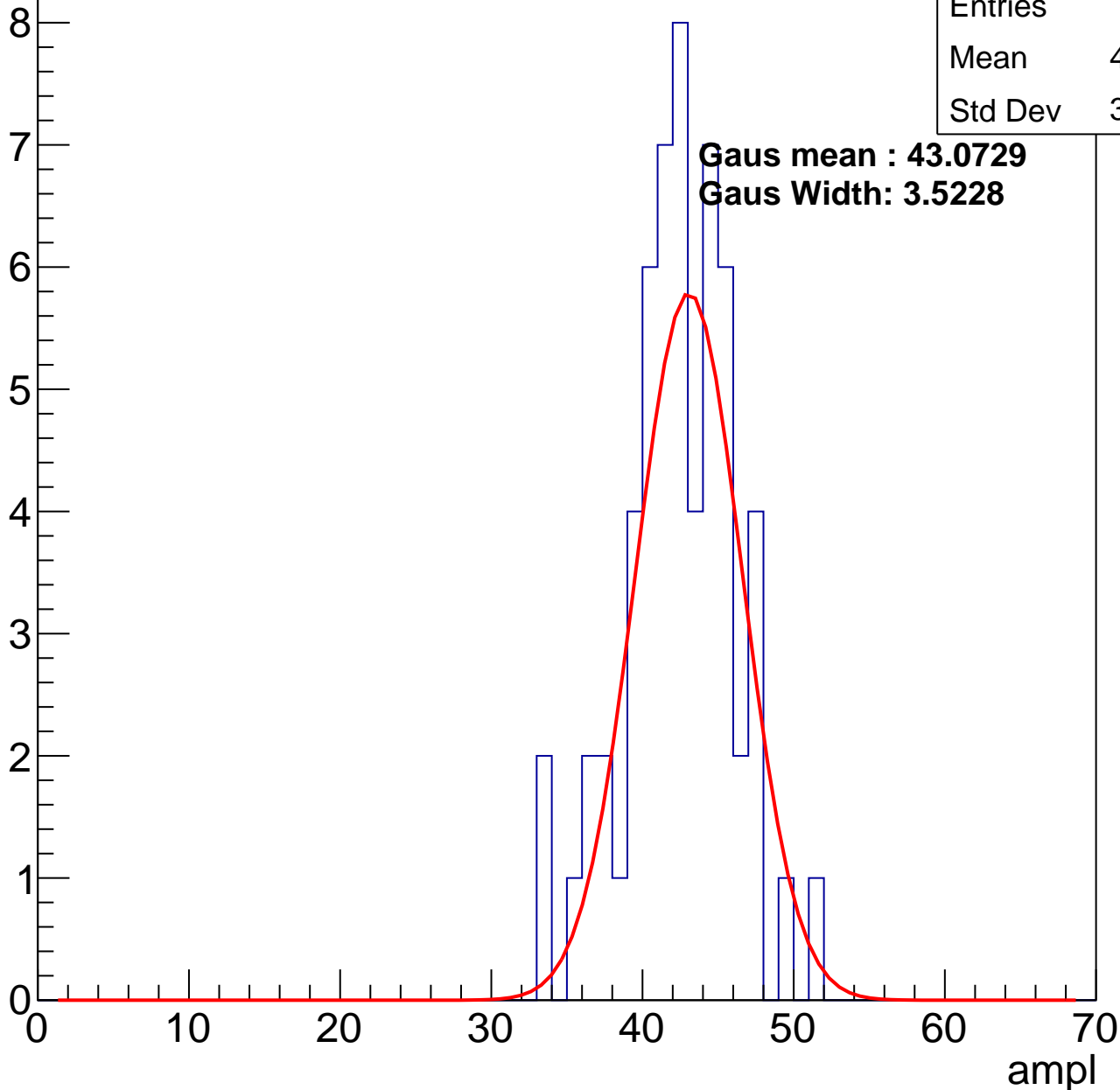
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	58
Mean	41.97
Std Dev	3.629

**Gaus mean : 43.0729**

**Gaus Width: 3.5228**



# B1L101S, U20-ch84, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

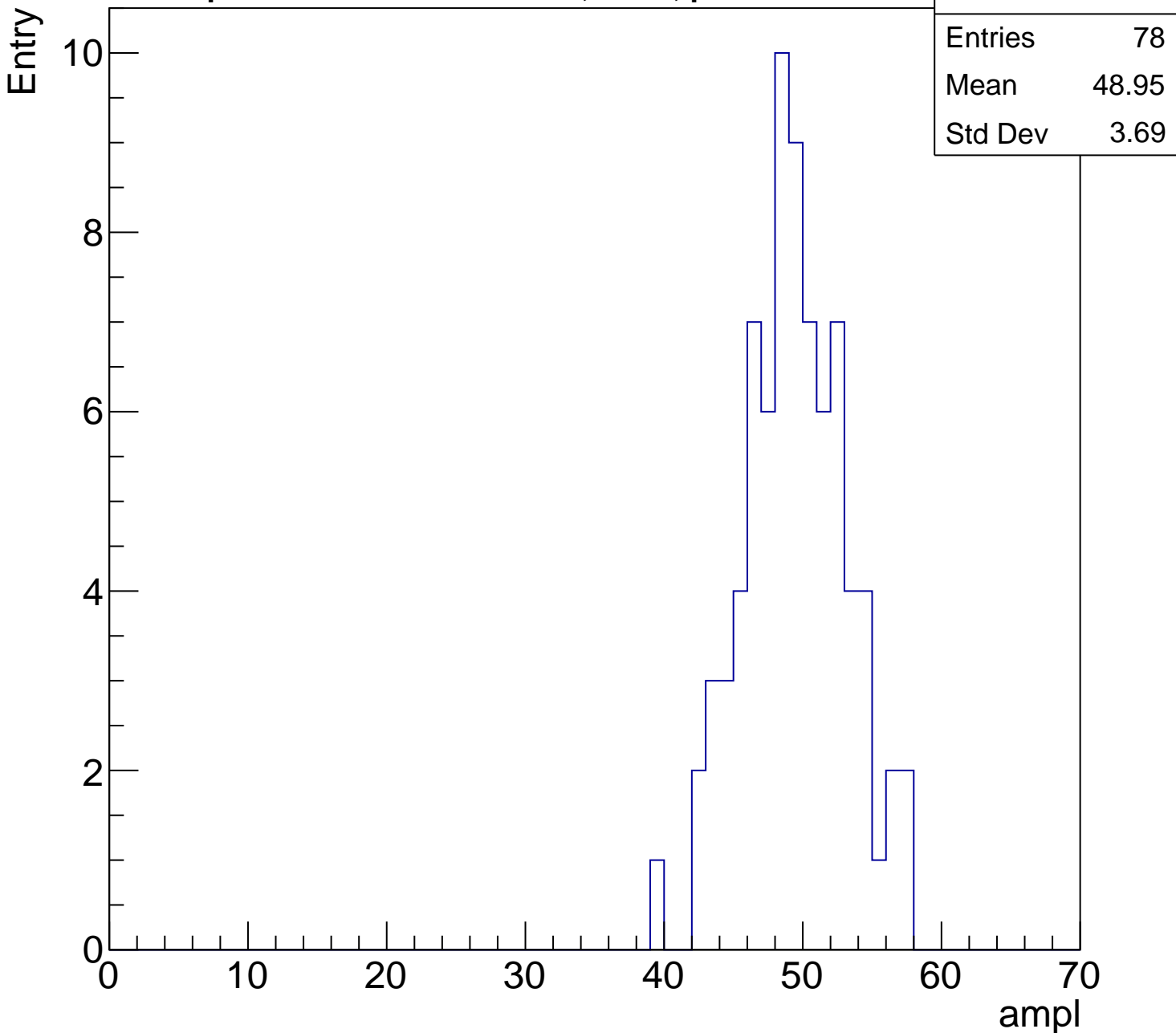
Entries	78
Mean	48.95
Std Dev	3.69

Entry

10  
8  
6  
4  
2  
0

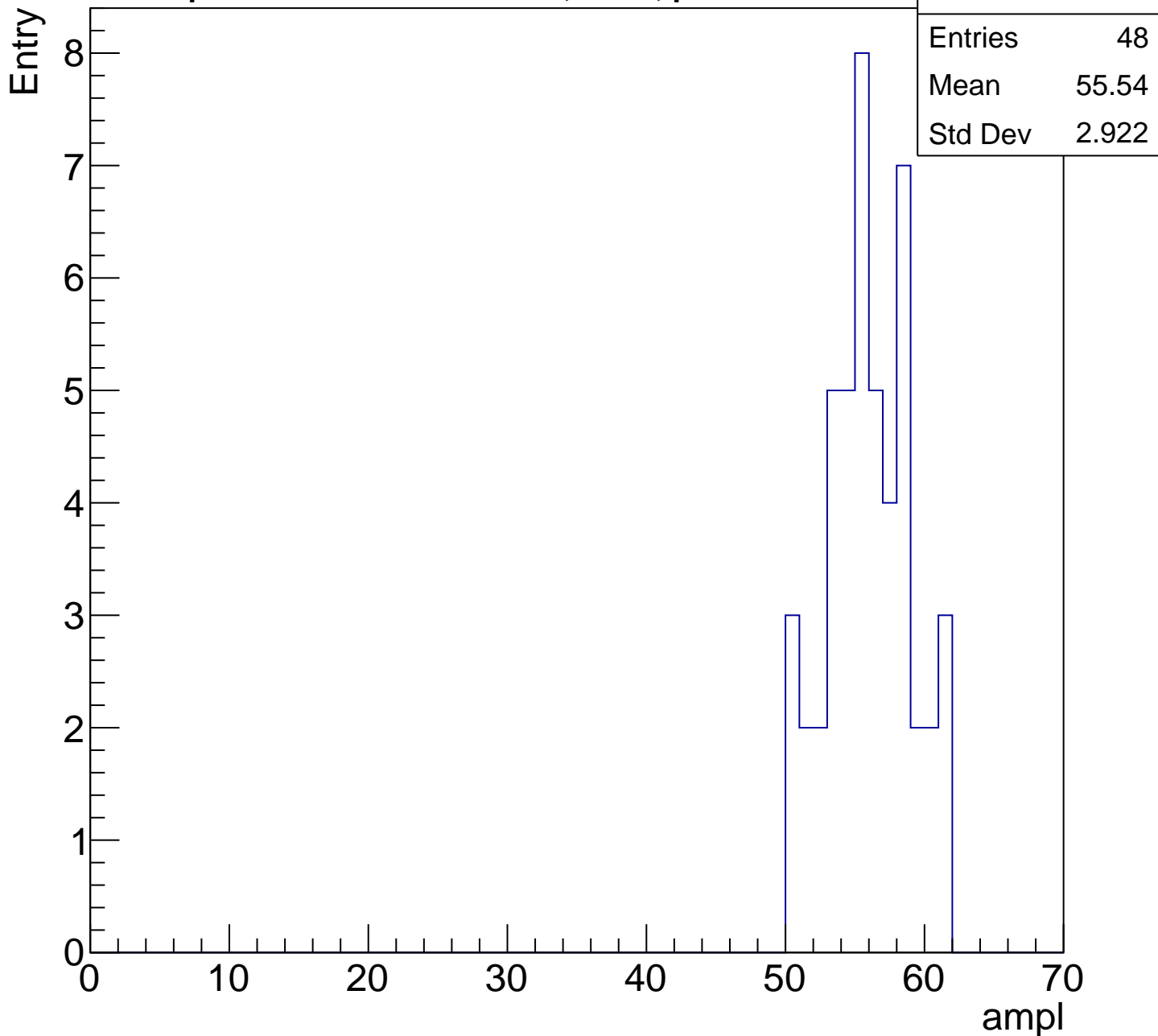
0 10 20 30 40 50 60 70

ampl



# B1L101S, U20-ch84, adc4

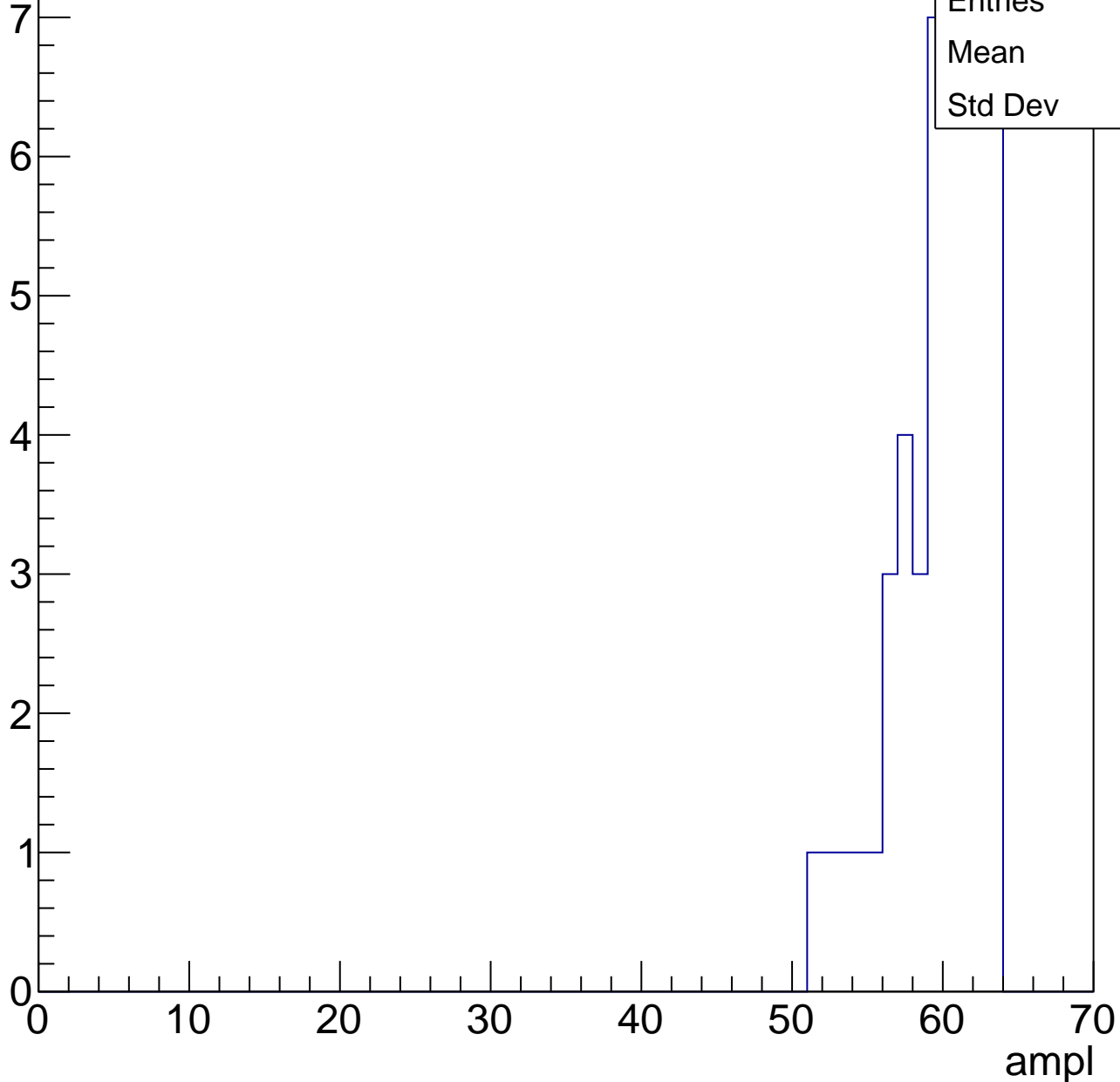
calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U20-ch84, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U20-ch84, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

3

2.5

2

1.5

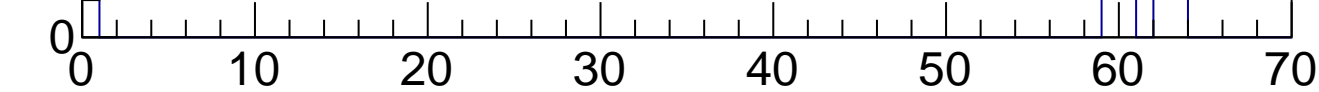
1

0.5

0

ampl

Entries	9
Mean	54.89
Std Dev	19.45





# B1L101S, U20-ch84, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U20-ch85, adc0

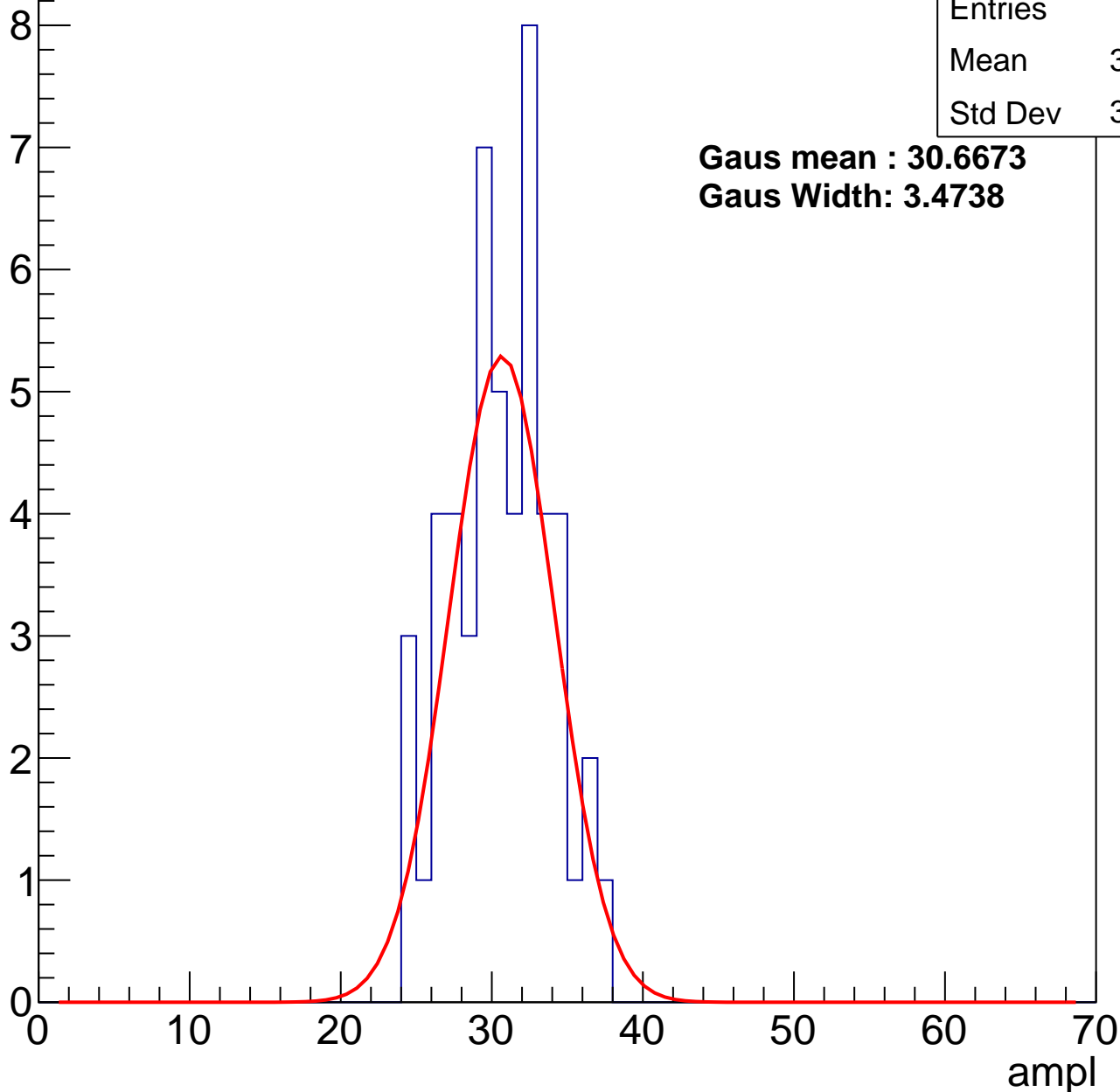
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	51
Mean	30.16
Std Dev	3.232

**Gaus mean : 30.6673**

**Gaus Width: 3.4738**



# B1L101S, U20-ch85, adc1

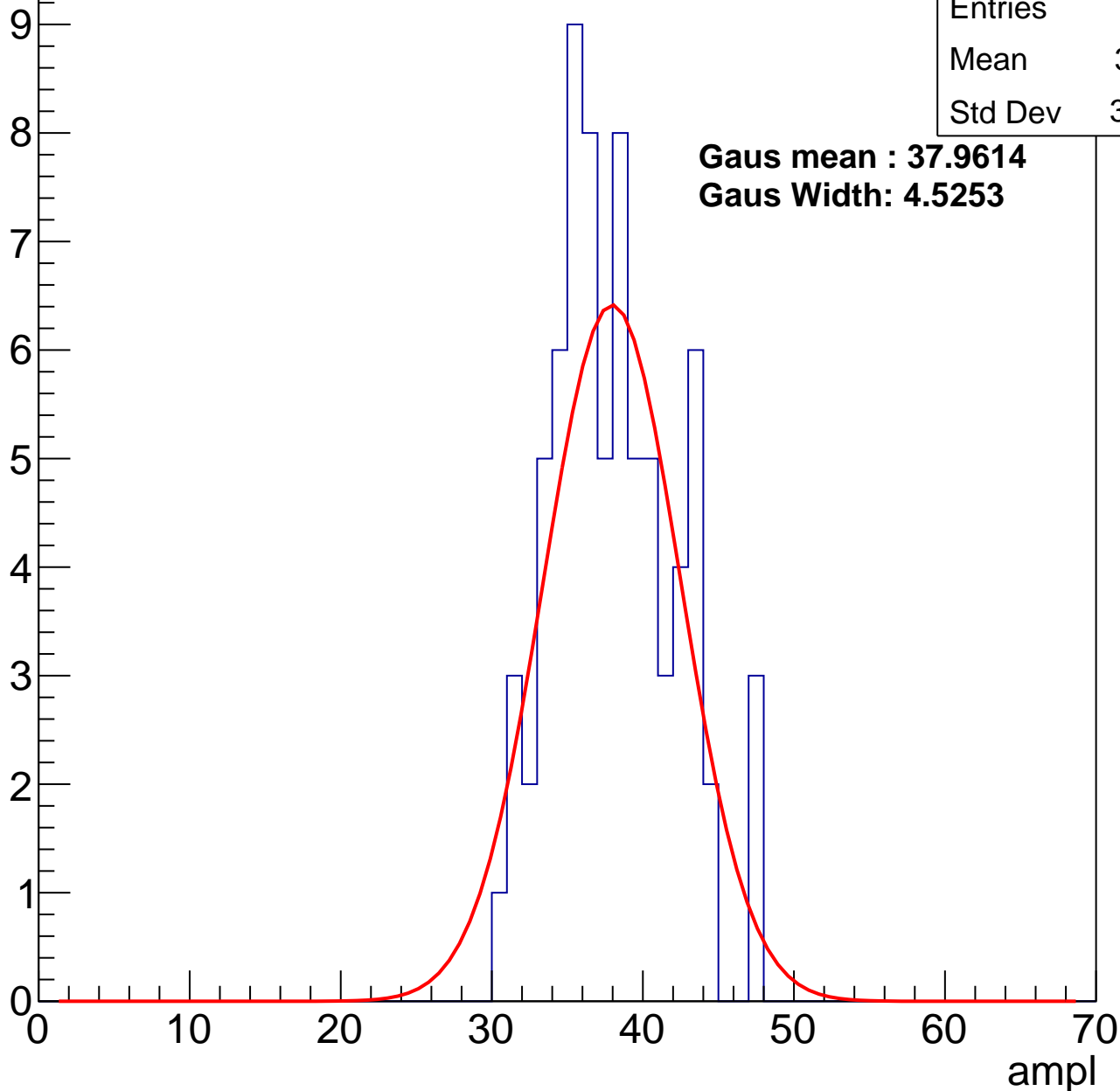
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	75
Mean	37.61
Std Dev	3.986

**Gaus mean : 37.9614**

**Gaus Width: 4.5253**



# B1L101S, U20-ch85, adc2

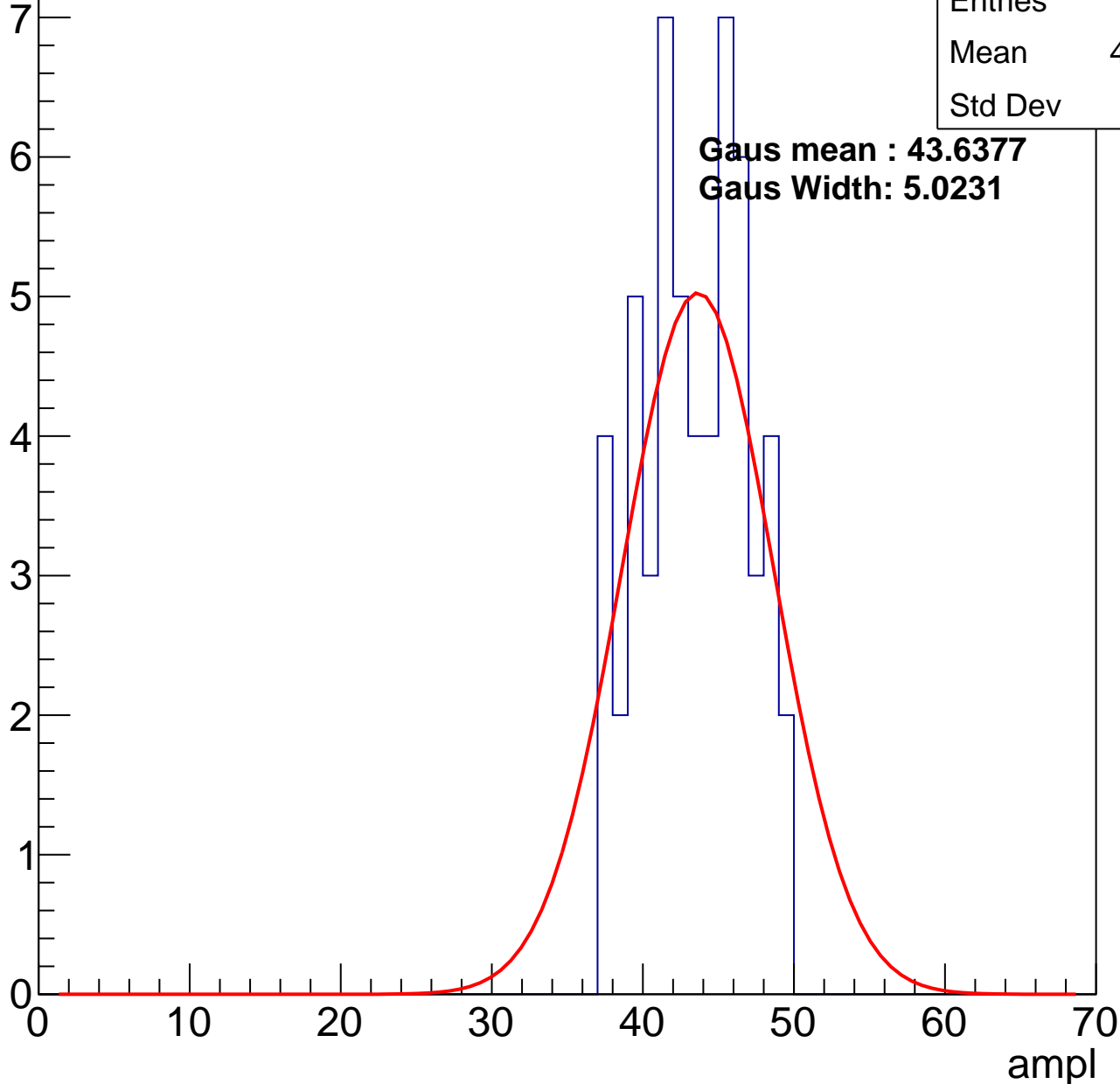
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	56
Mean	42.96
Std Dev	3.38

**Gaus mean : 43.6377**

**Gaus Width: 5.0231**



# B1L101S, U20-ch85, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	80
Mean	50.2
Std Dev	3.881

Entry

10

8

6

4

2

0

0

10

20

30

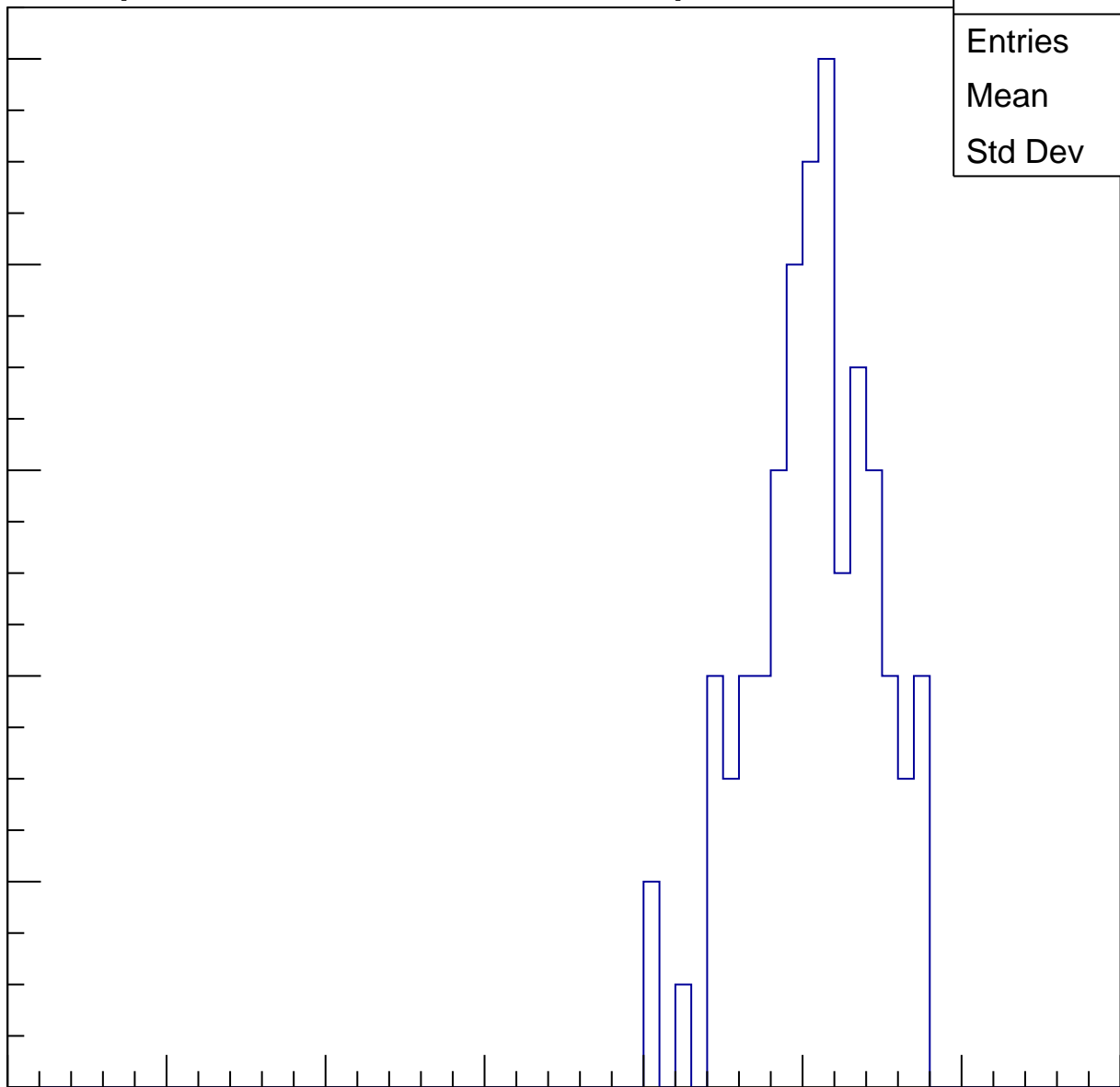
40

50

60

70

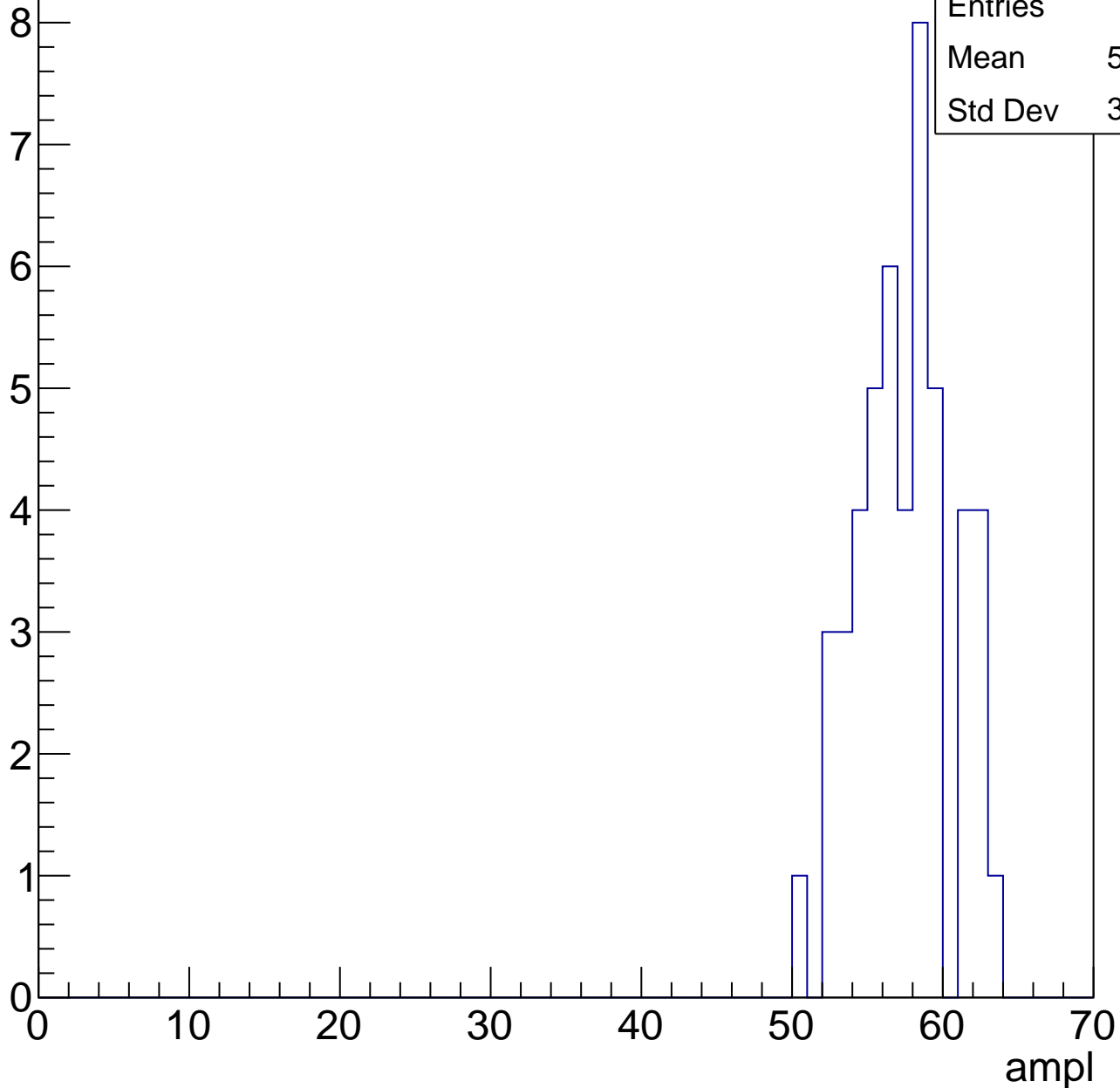
ampl



# B1L101S, U20-ch85, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

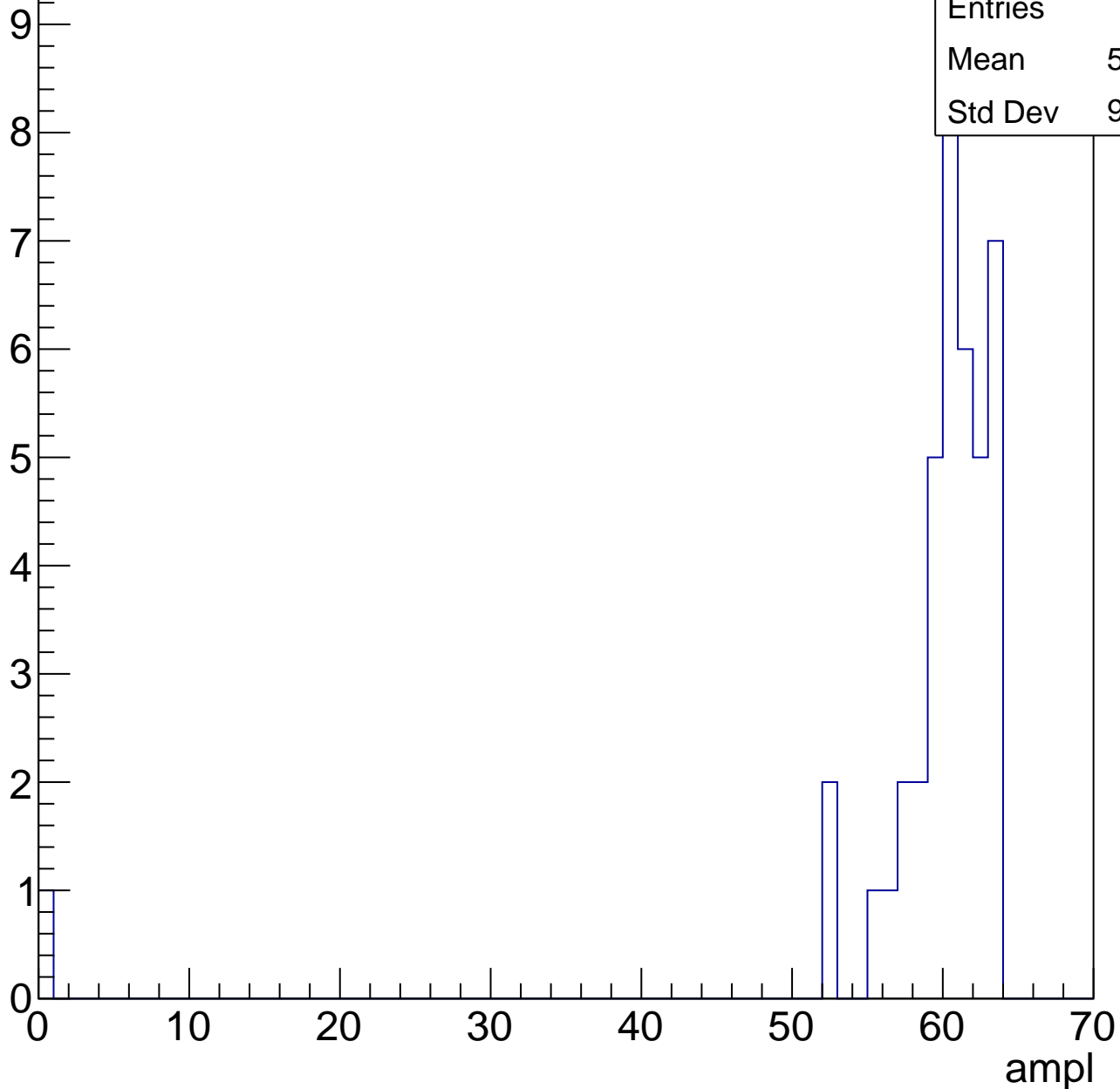


Entries	48
Mean	56.96
Std Dev	3.102

# B1L101S, U20-ch85, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U20-ch85, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U20-ch85, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U20-ch86, adc0

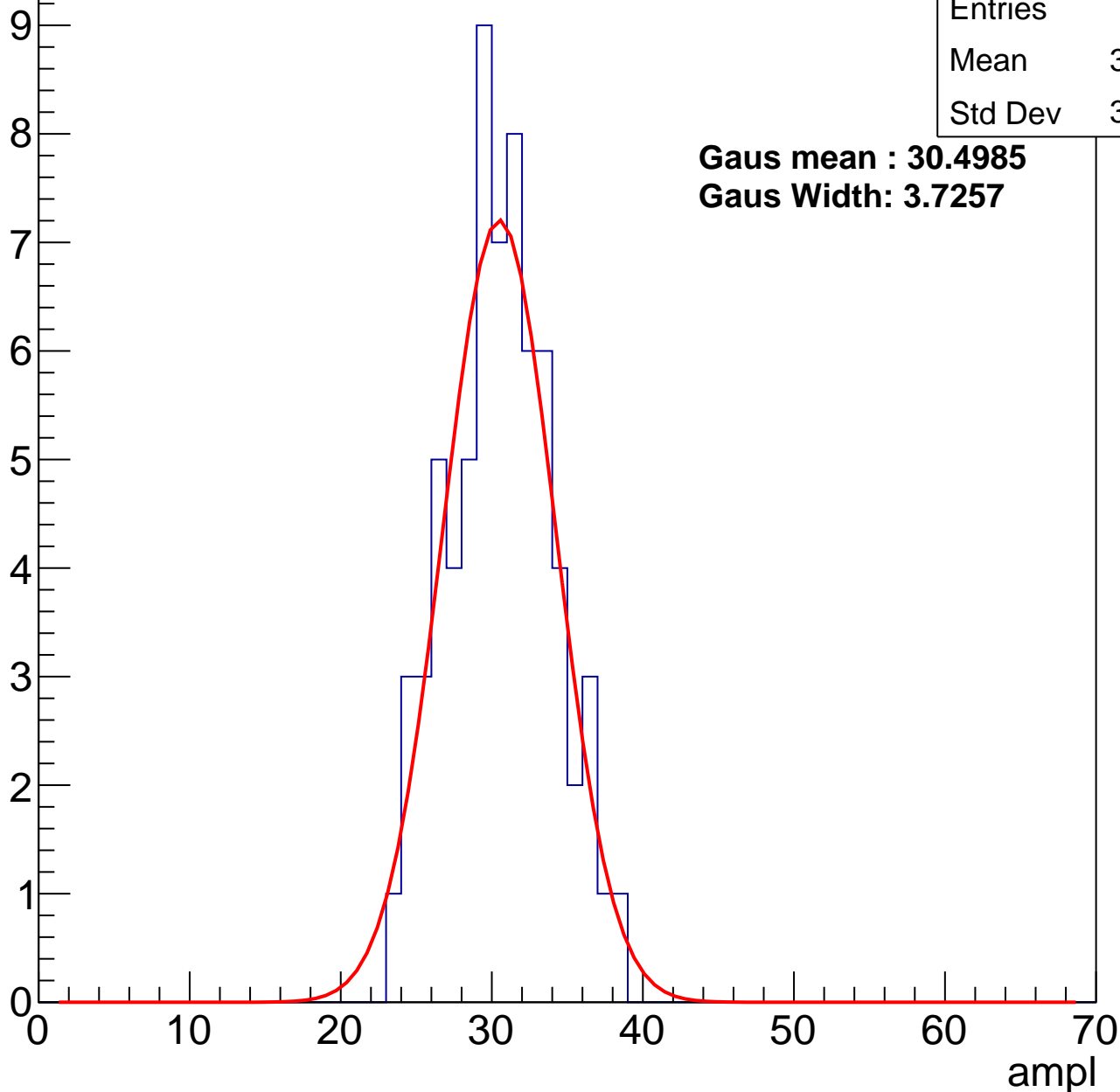
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	30.09
Std Dev	3.425

**Gaus mean : 30.4985**

**Gaus Width: 3.7257**



# B1L101S, U20-ch86, adc1

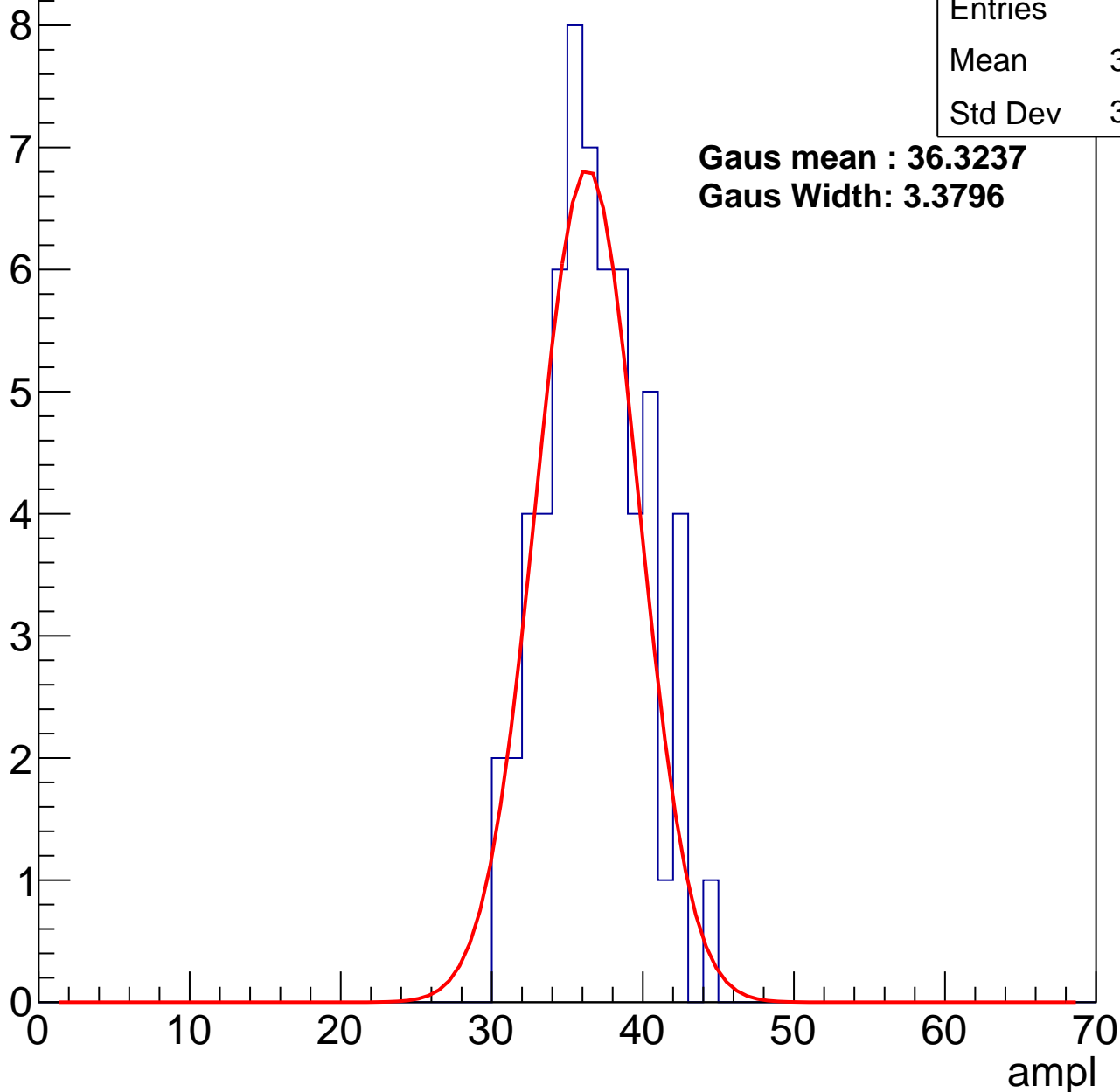
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	60
Mean	36.28
Std Dev	3.236

**Gaus mean : 36.3237**

**Gaus Width: 3.3796**



# B1L101S, U20-ch86, adc2

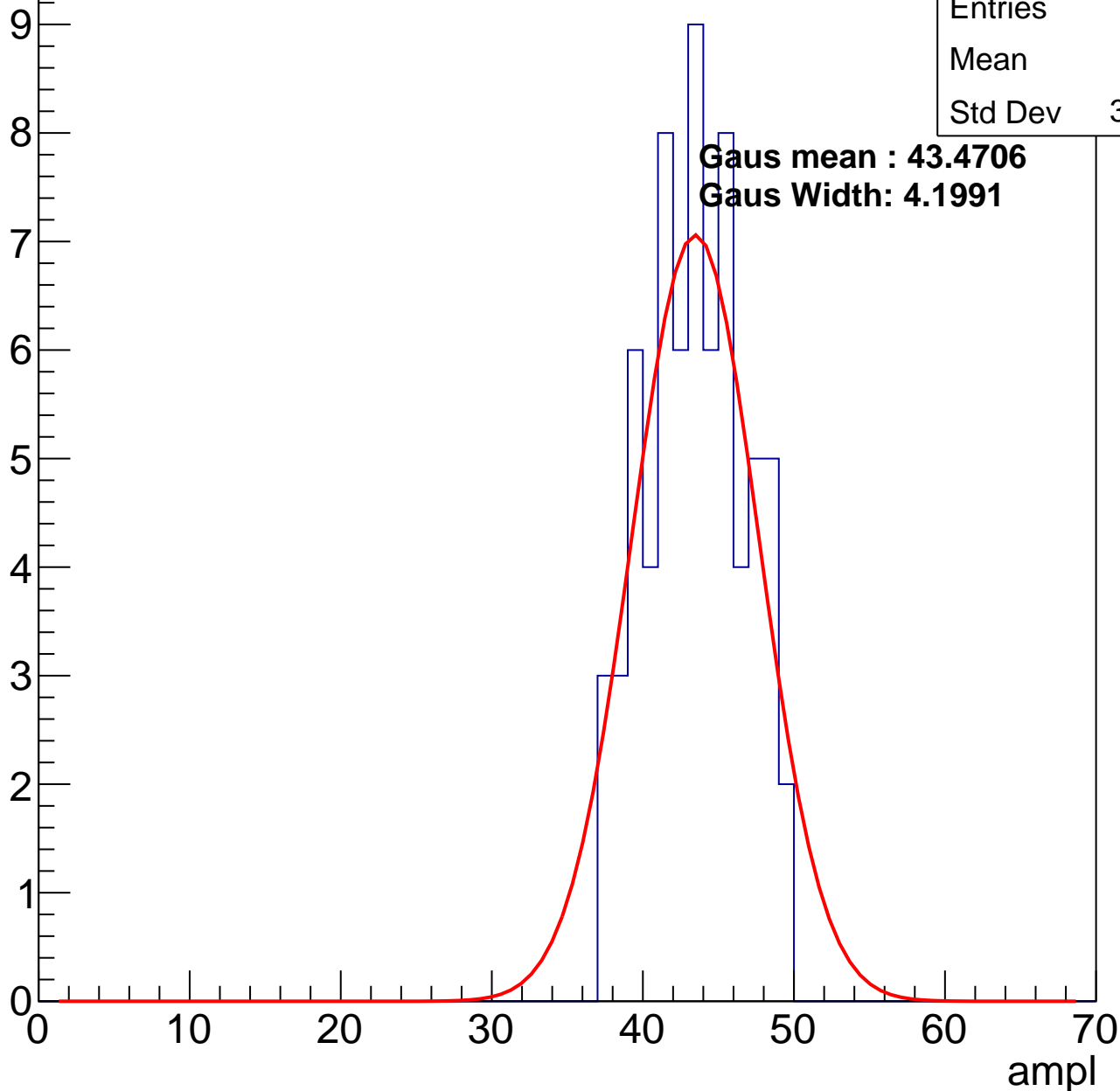
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	43
Std Dev	3.194

**Gaus mean : 43.4706**

**Gaus Width: 4.1991**

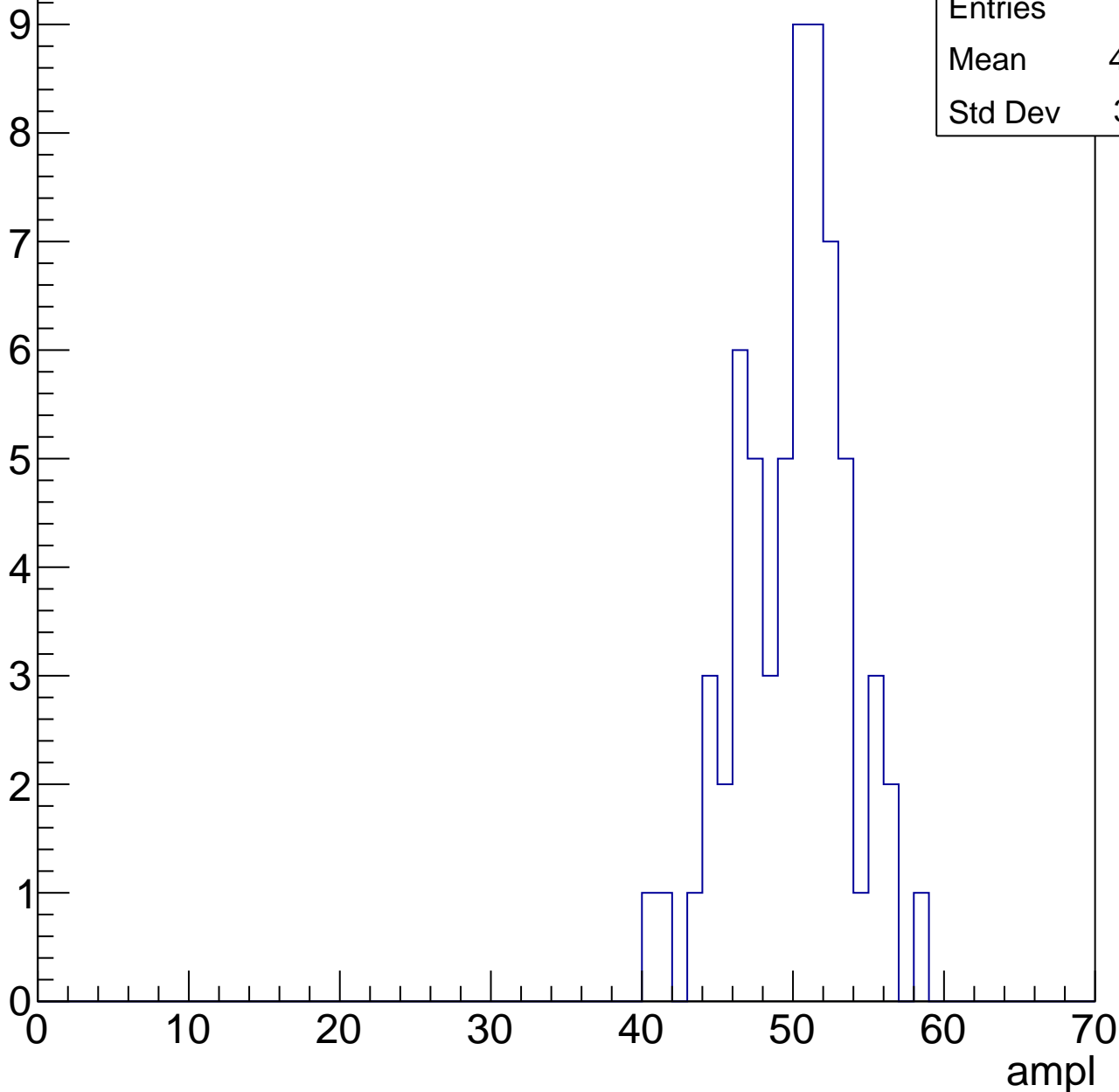


# B1L101S, U20-ch86, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	49.58
Std Dev	3.631

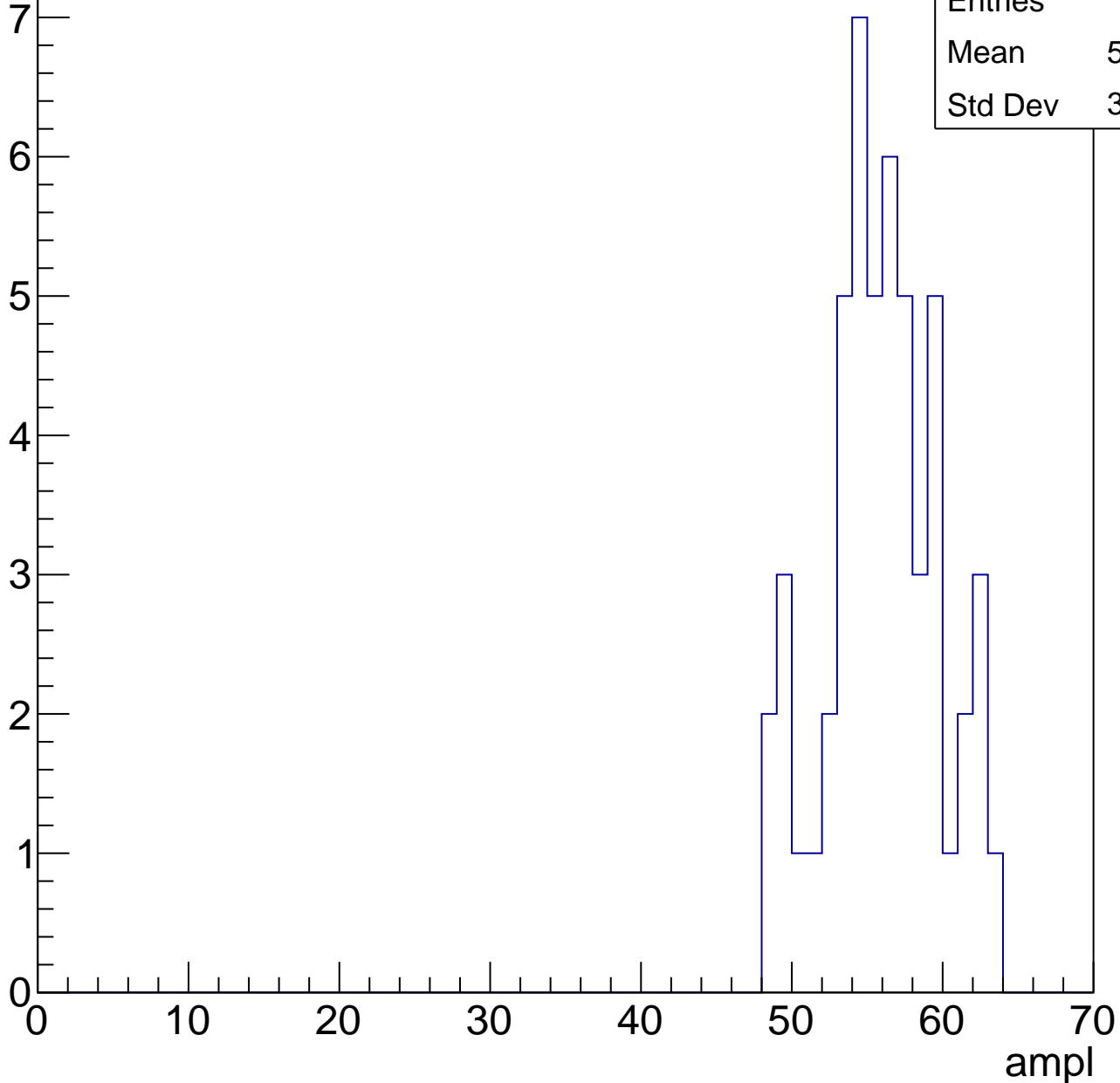


# B1L101S, U20-ch86, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	52
Mean	55.52
Std Dev	3.718



# B1L101S, U20-ch86, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	53
Mean	58.38
Std Dev	8.524

ampl

0 10 20 30 40 50 60 70

1

2

3

4

5

6

7

8

# B1L101S, U20-ch86, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U20-ch86, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U20-ch87, adc0

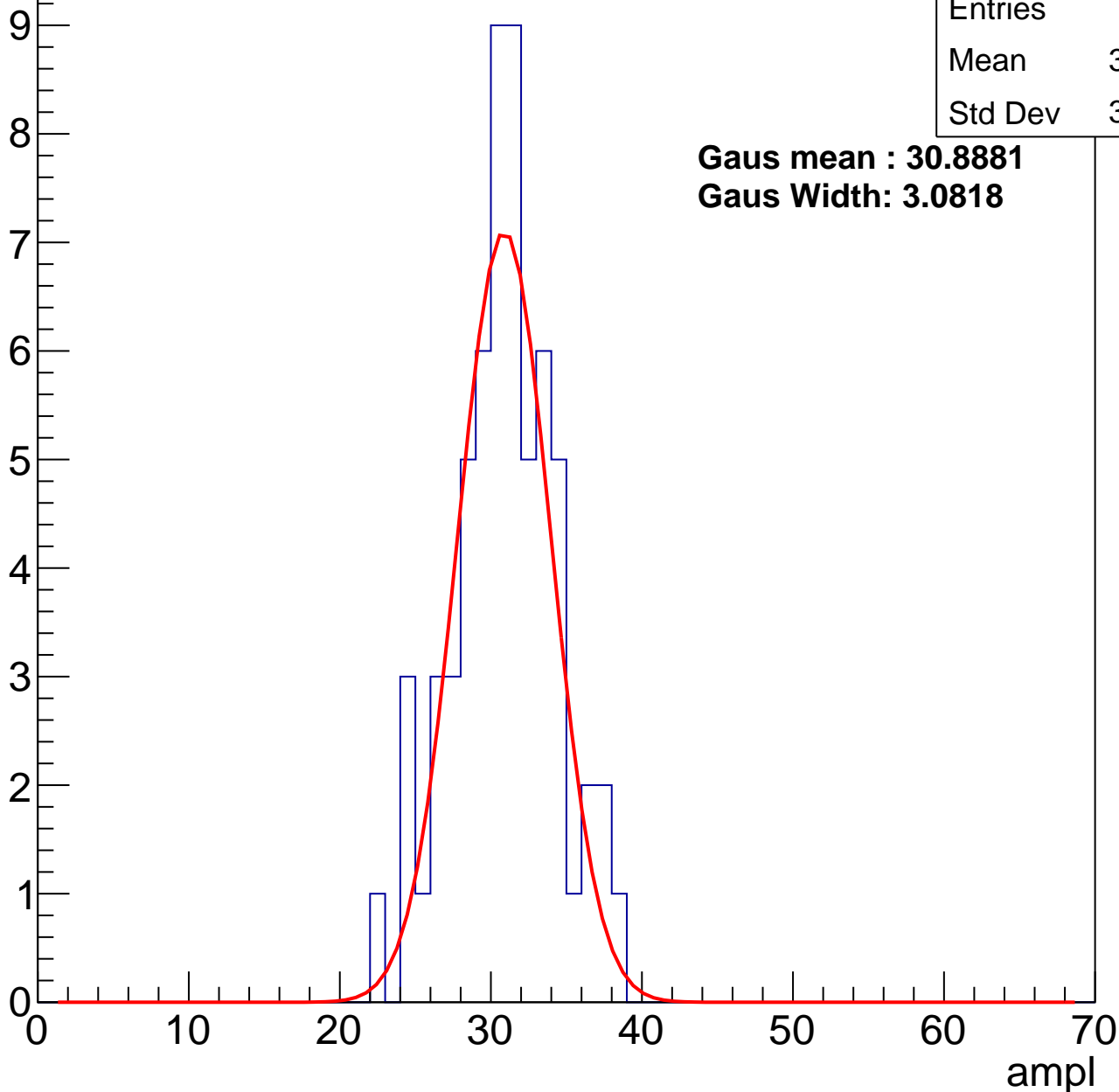
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	30.45
Std Dev	3.378

**Gaus mean : 30.8881**

**Gaus Width: 3.0818**



# B1L101S, U20-ch87, adc1

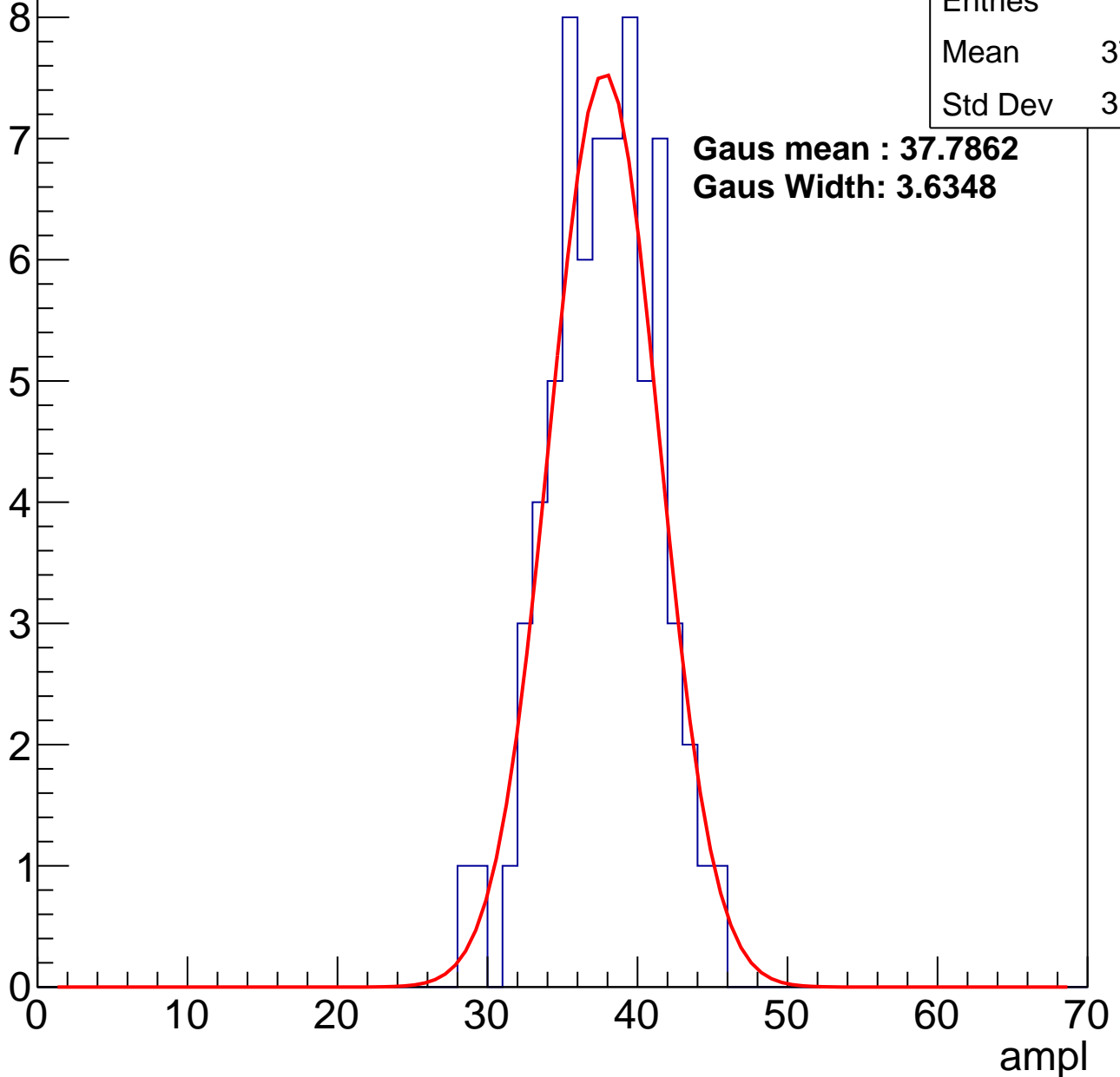
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	37.24
Std Dev	3.495

**Gaus mean : 37.7862**

**Gaus Width: 3.6348**



# B1L101S, U20-ch87, adc2

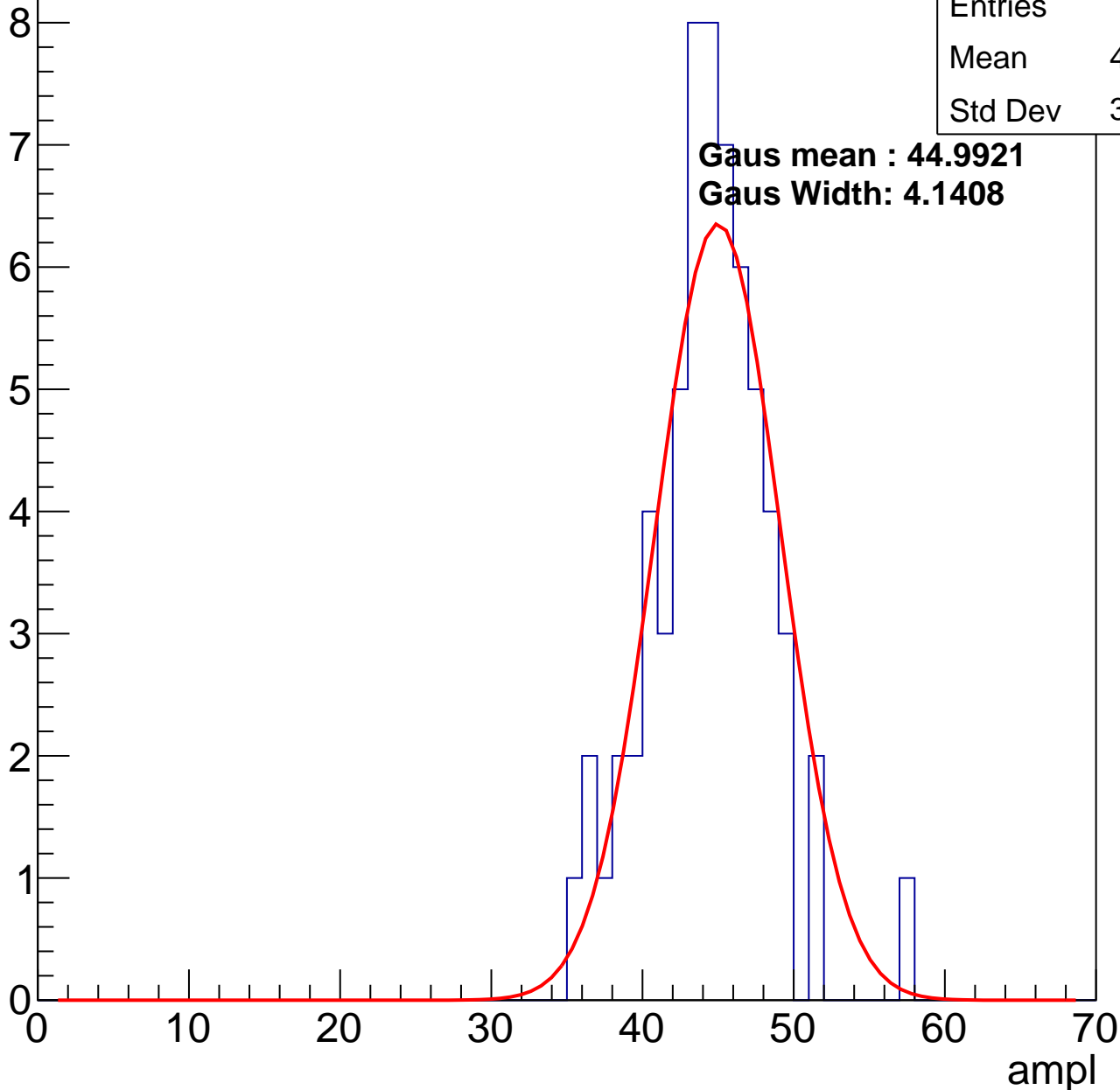
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	43.92
Std Dev	3.914

**Gaus mean : 44.9921**

**Gaus Width: 4.1408**

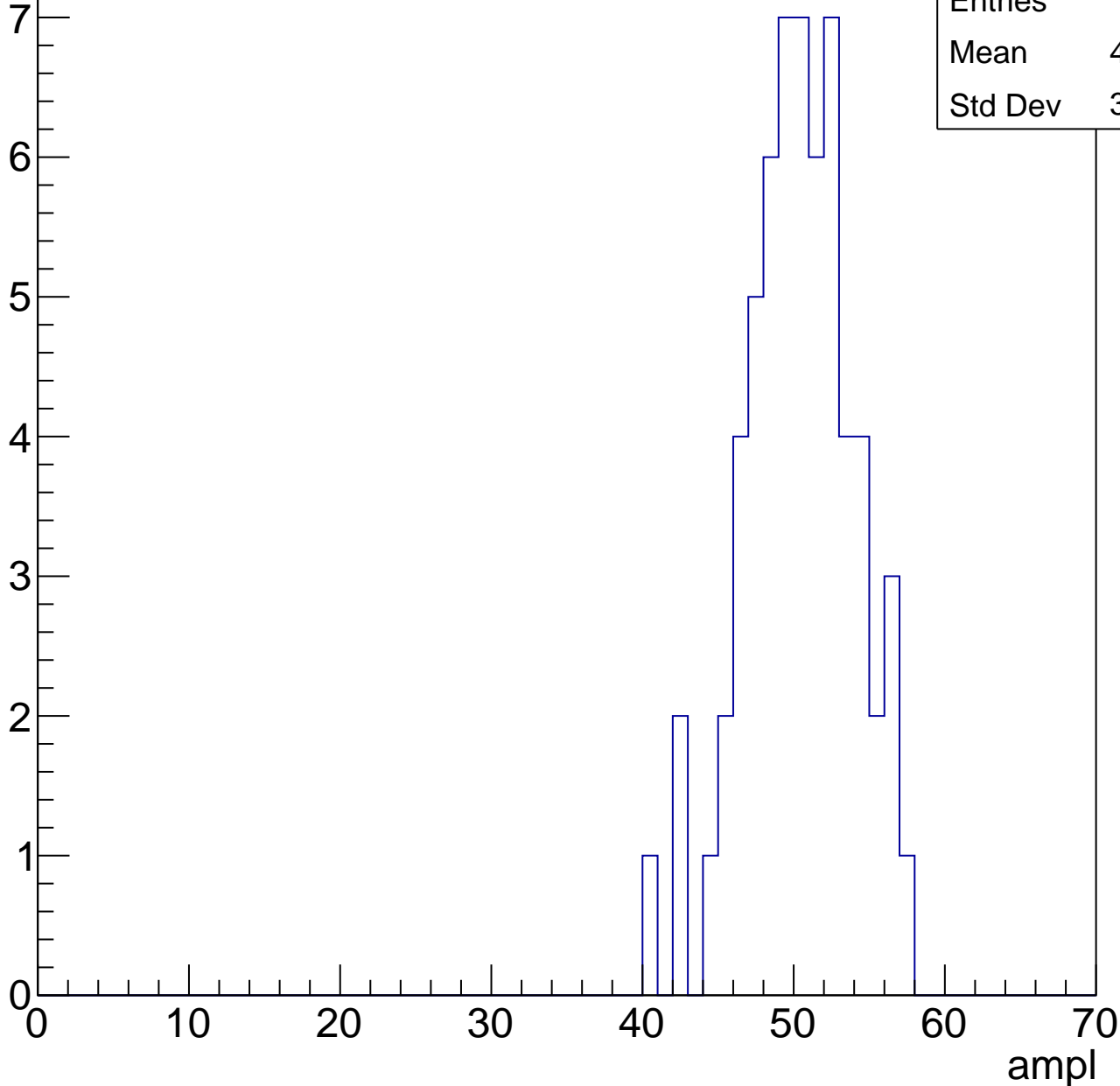


# B1L101S, U20-ch87, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	49.85
Std Dev	3.578

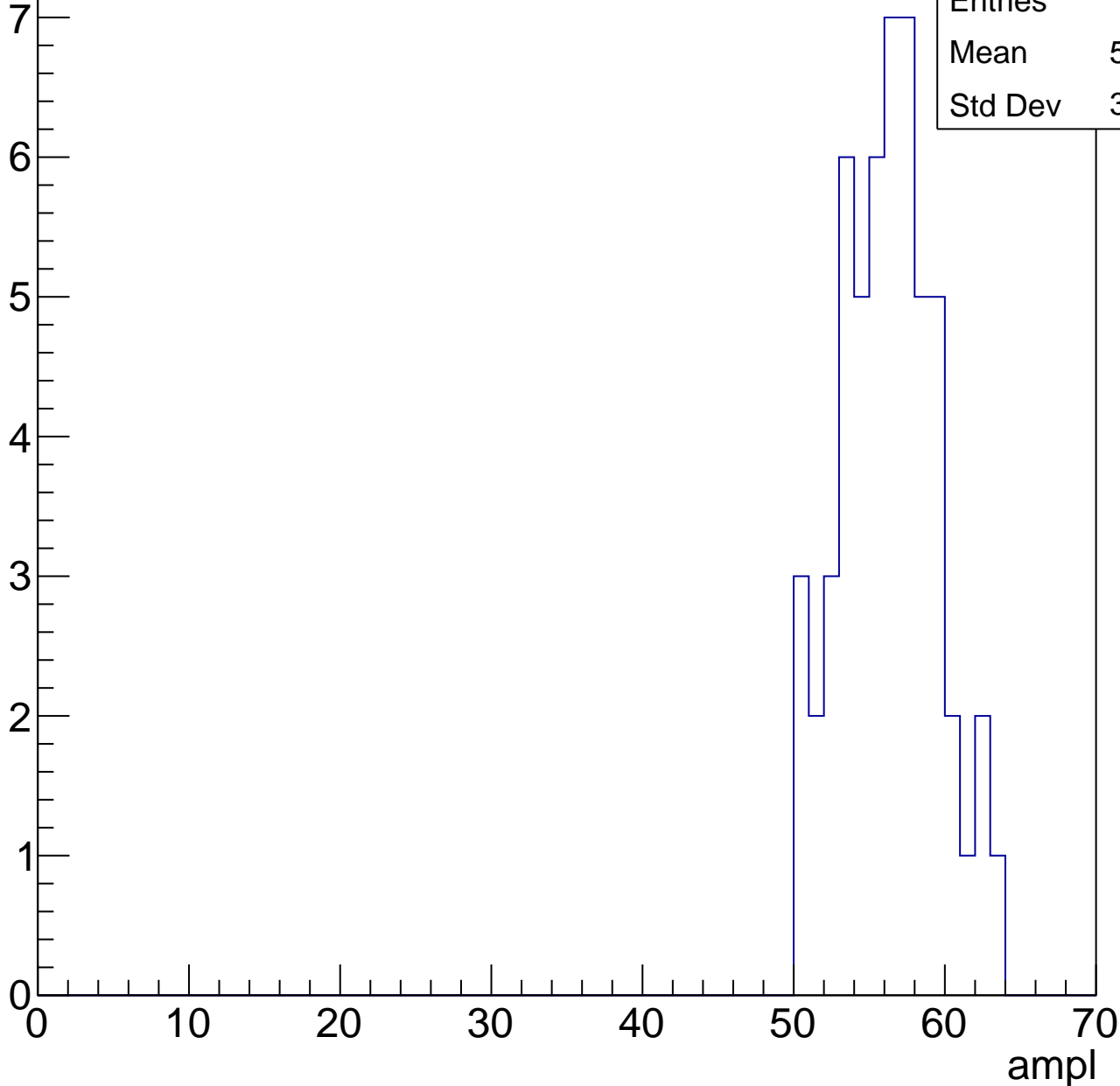


# B1L101S, U20-ch87, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

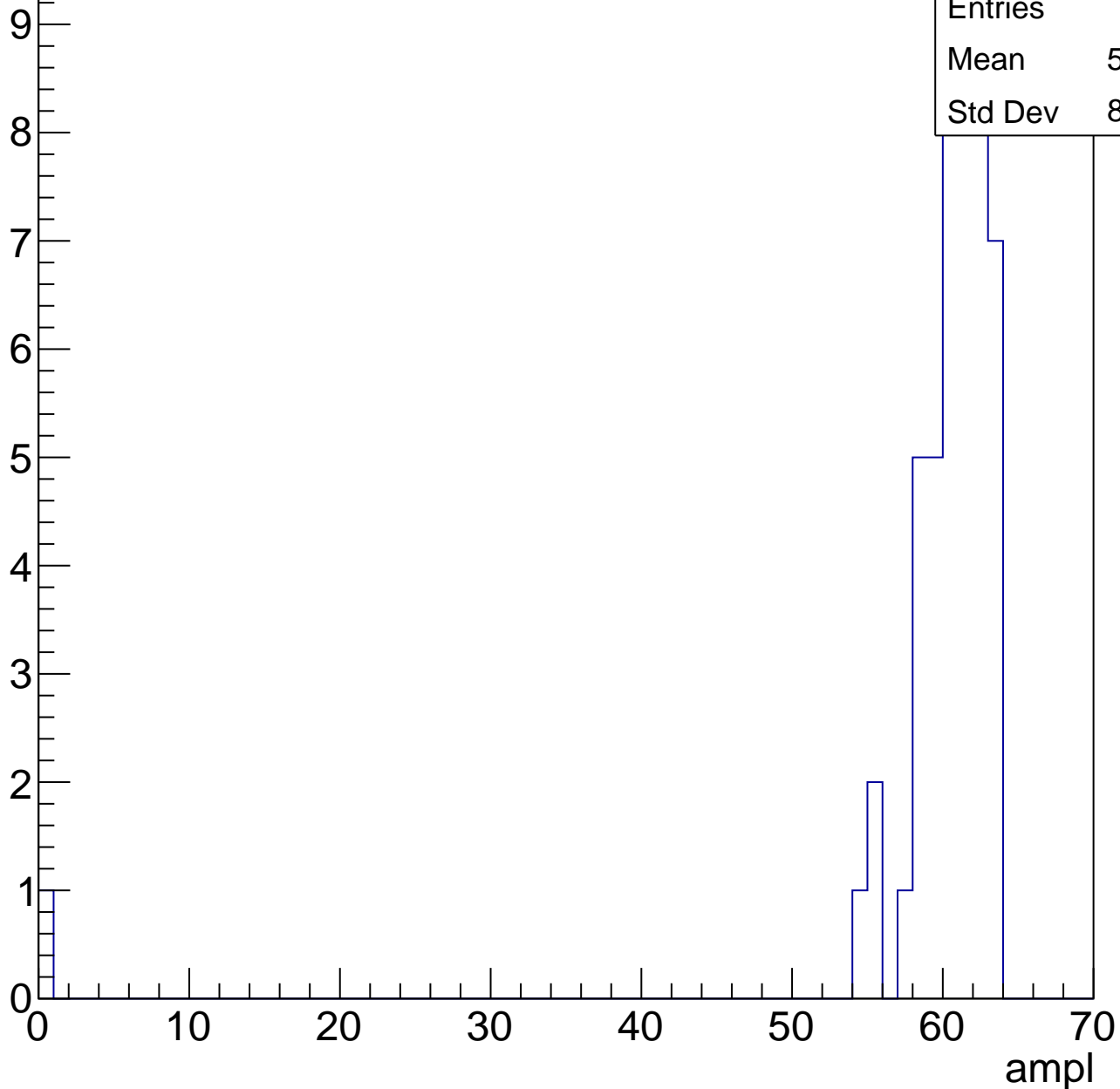
Entries	55
Mean	55.82
Std Dev	3.116



# B1L101S, U20-ch87, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U20-ch87, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U20-ch87, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L101S, U20-ch88, adc0

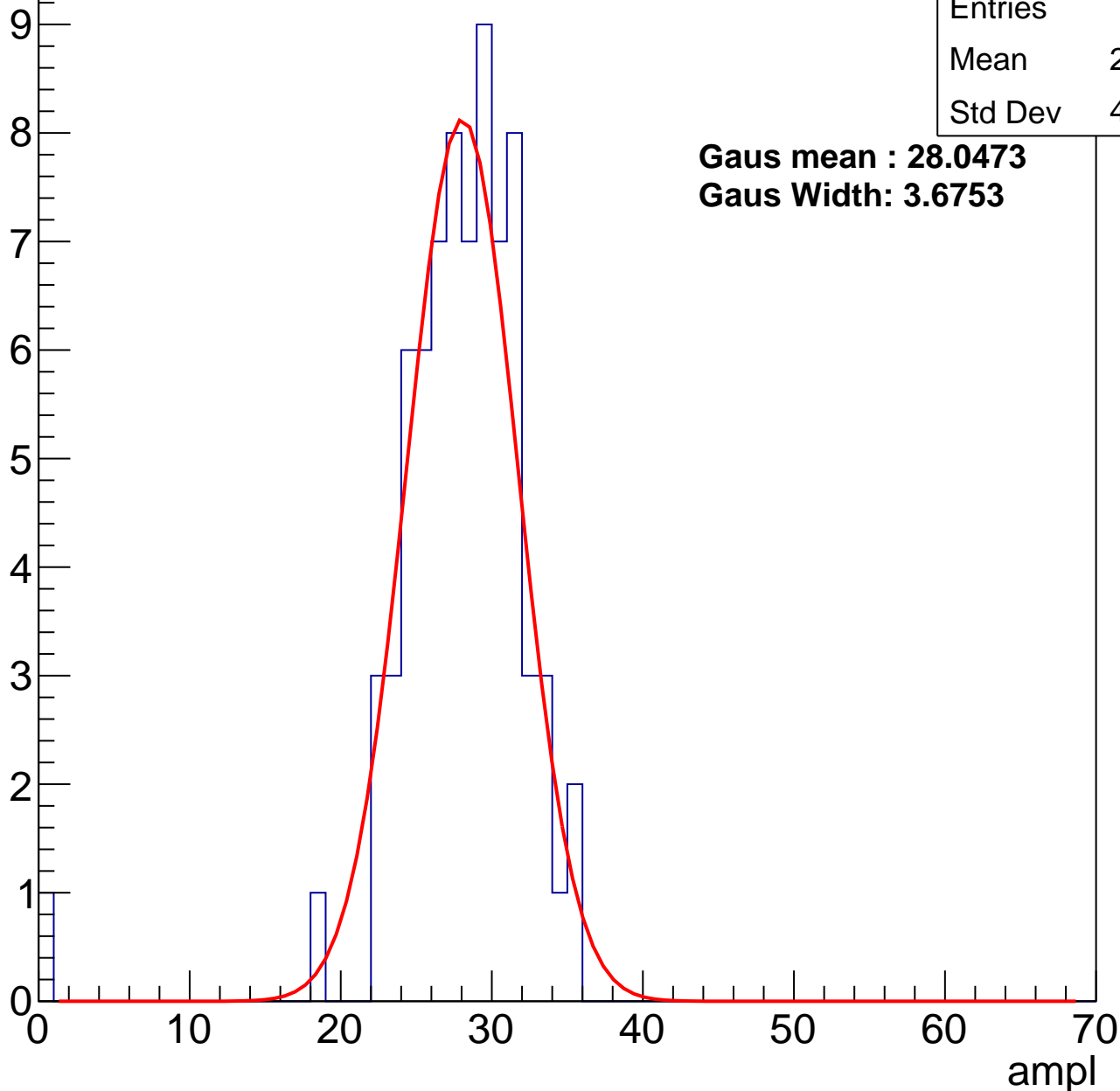
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	75
Mean	27.45
Std Dev	4.614

**Gaus mean : 28.0473**

**Gaus Width: 3.6753**



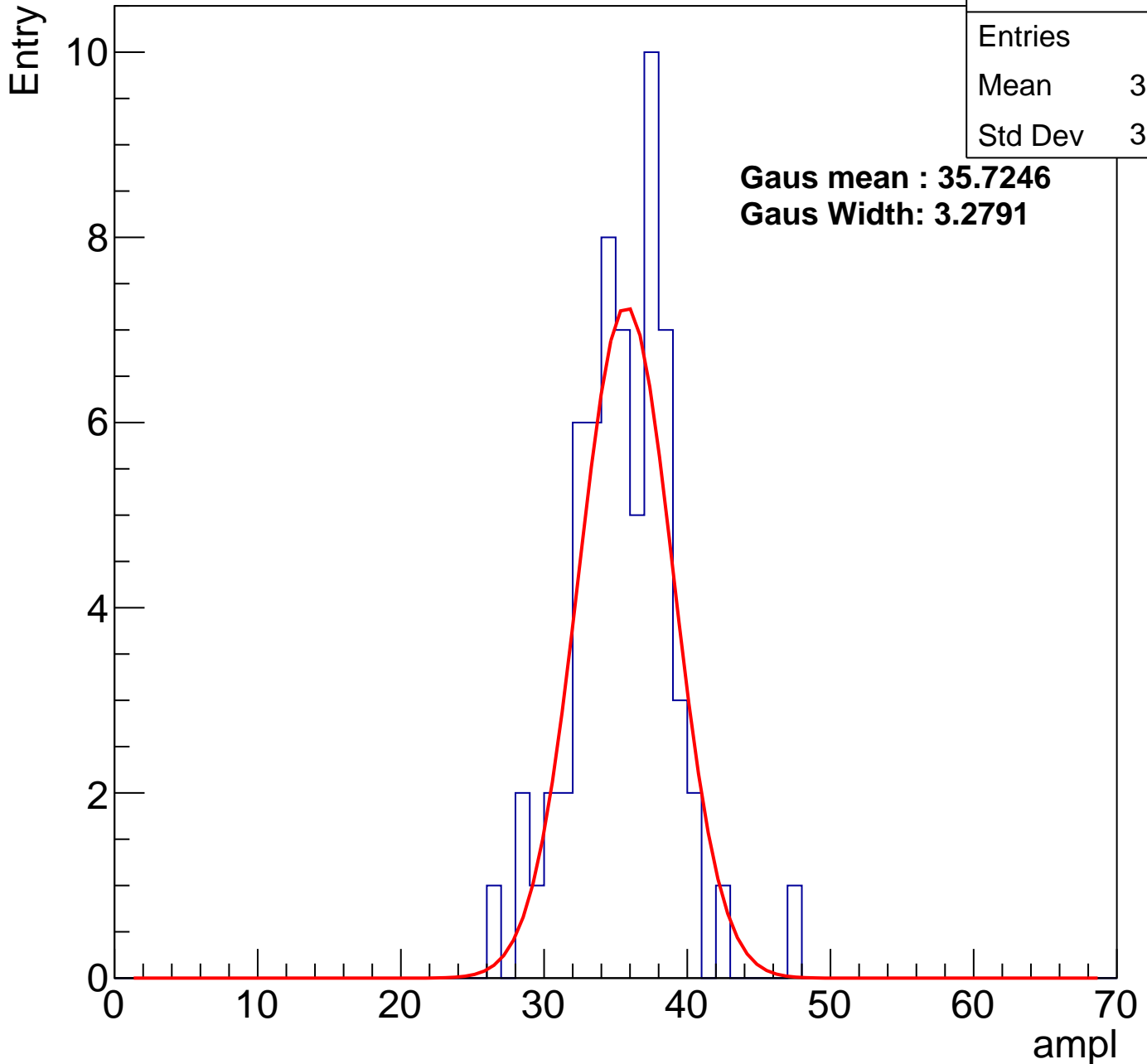
# B1L101S, U20-ch88, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	64
Mean	35.03
Std Dev	3.495

**Gaus mean : 35.7246**

**Gaus Width: 3.2791**



# B1L101S, U20-ch88, adc2

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	58
Mean	40.76
Std Dev	3.098

**Gaus mean : 41.0954**

**Gaus Width: 3.1201**

10

8

6

4

2

0

0

10

20

30

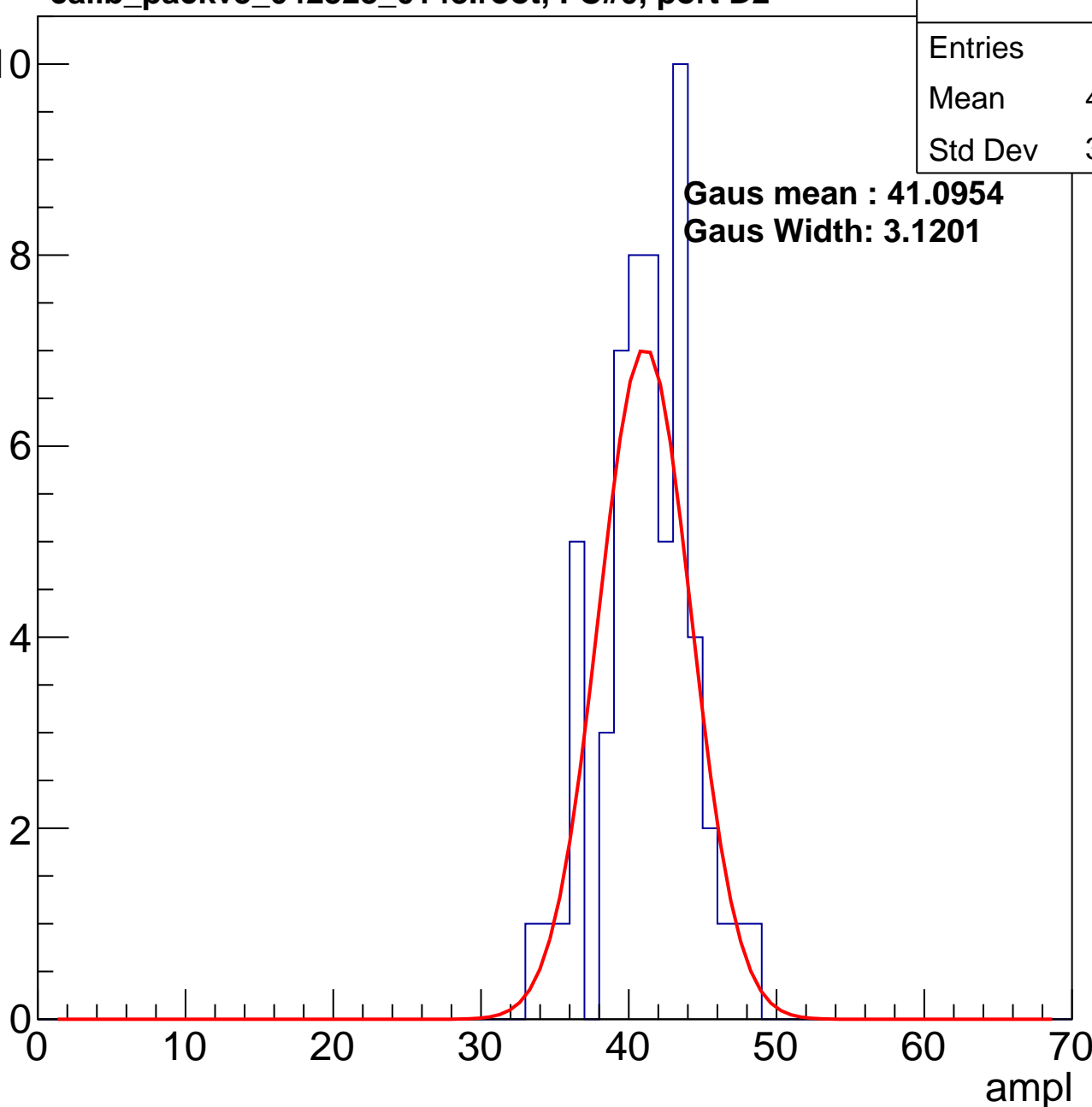
40

50

60

70

ampl

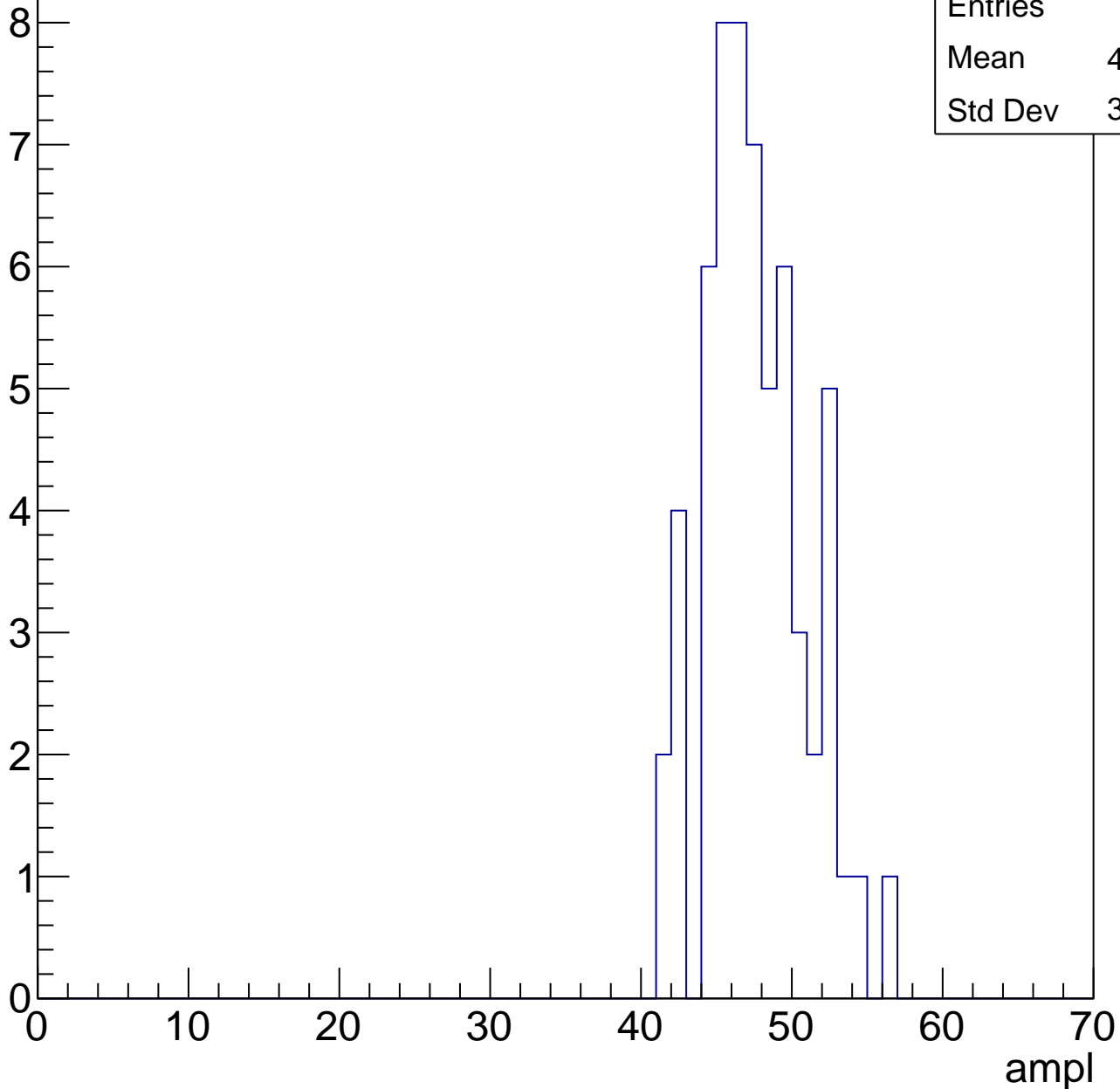


# B1L101S, U20-ch88, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	59
Mean	47.12
Std Dev	3.304

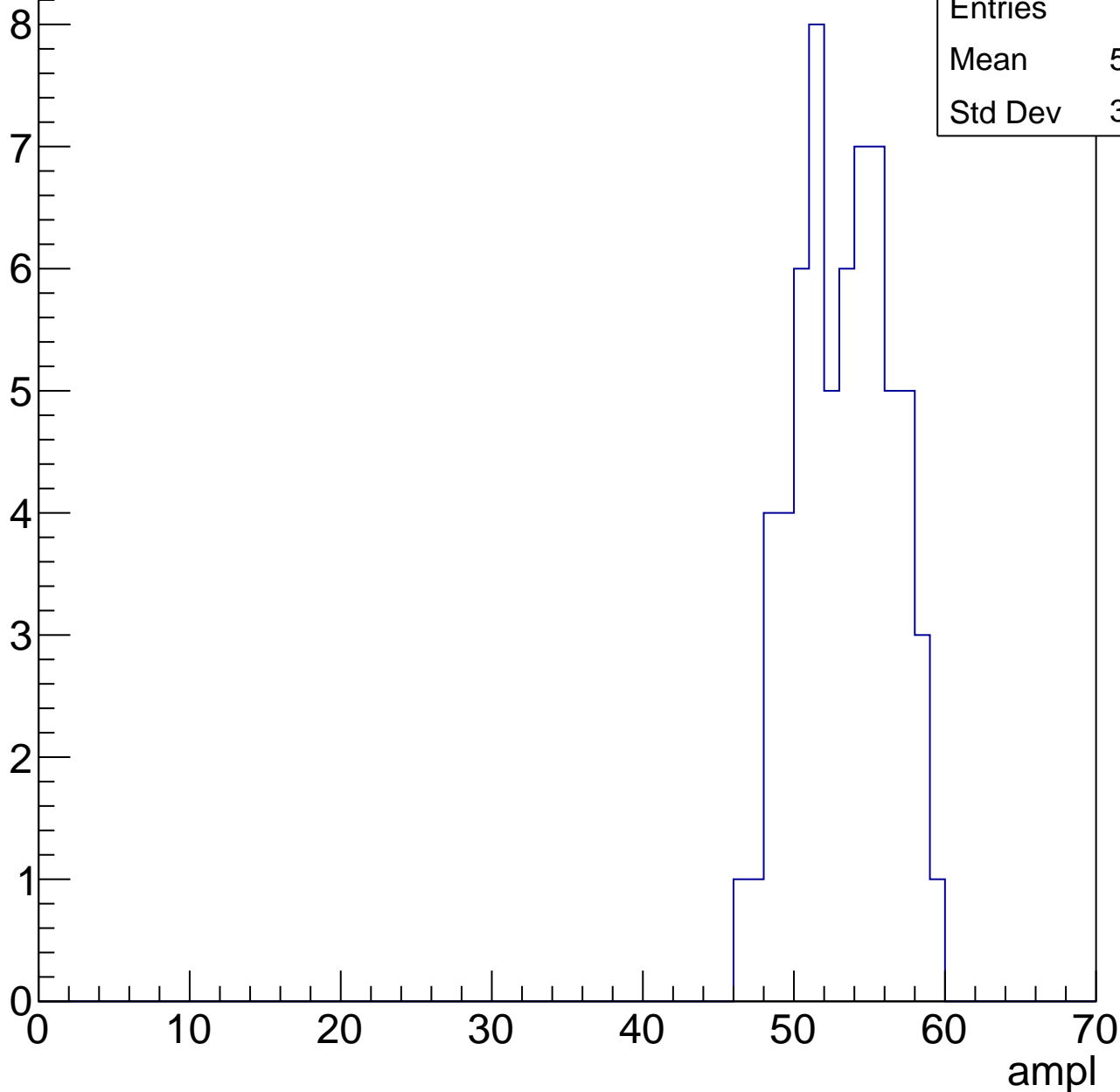


# B1L101S, U20-ch88, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	52.83
Std Dev	3.109



# B1L101S, U20-ch88, adc5

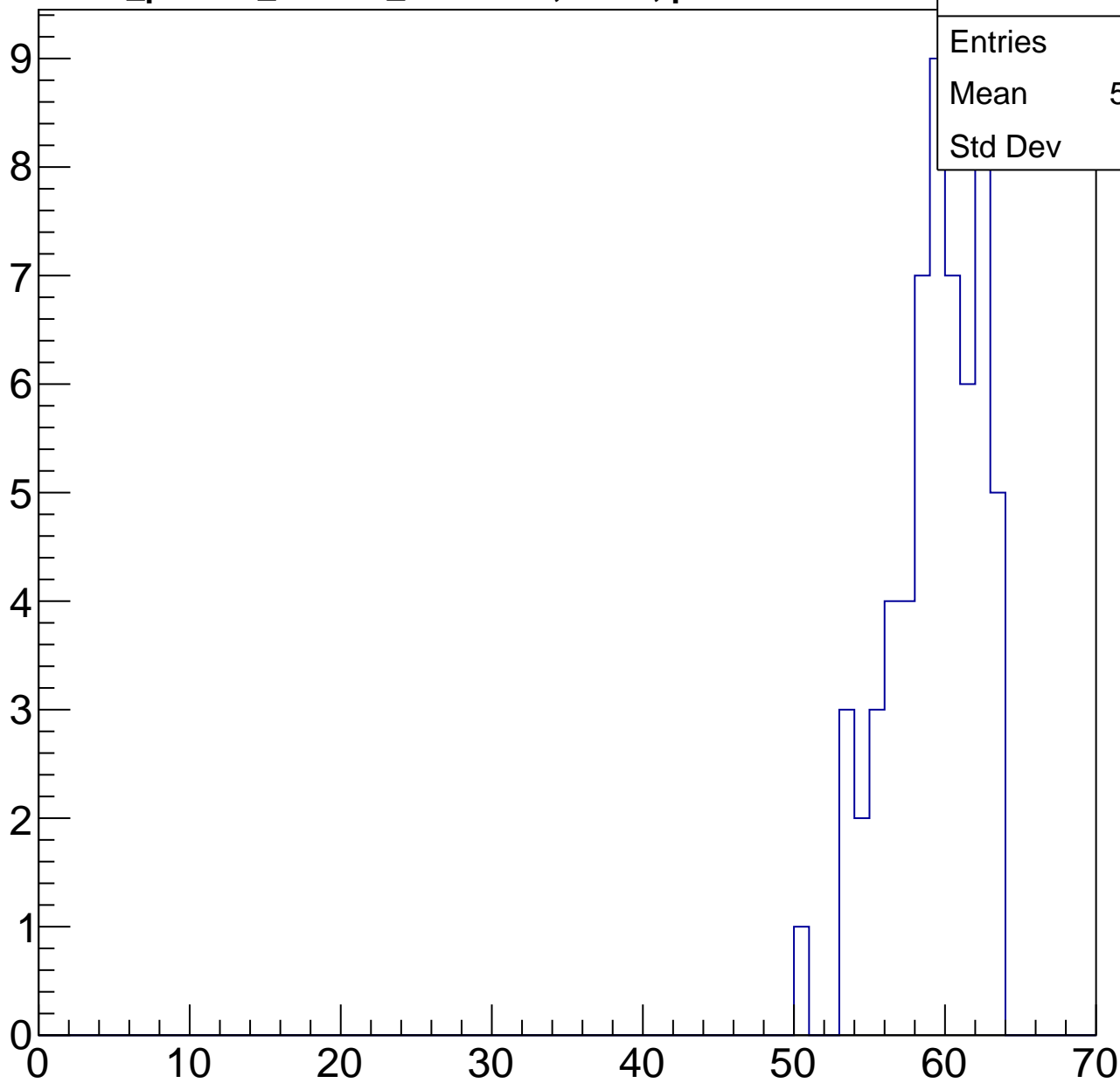
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	60
Mean	58.83
Std Dev	2.99

ampl

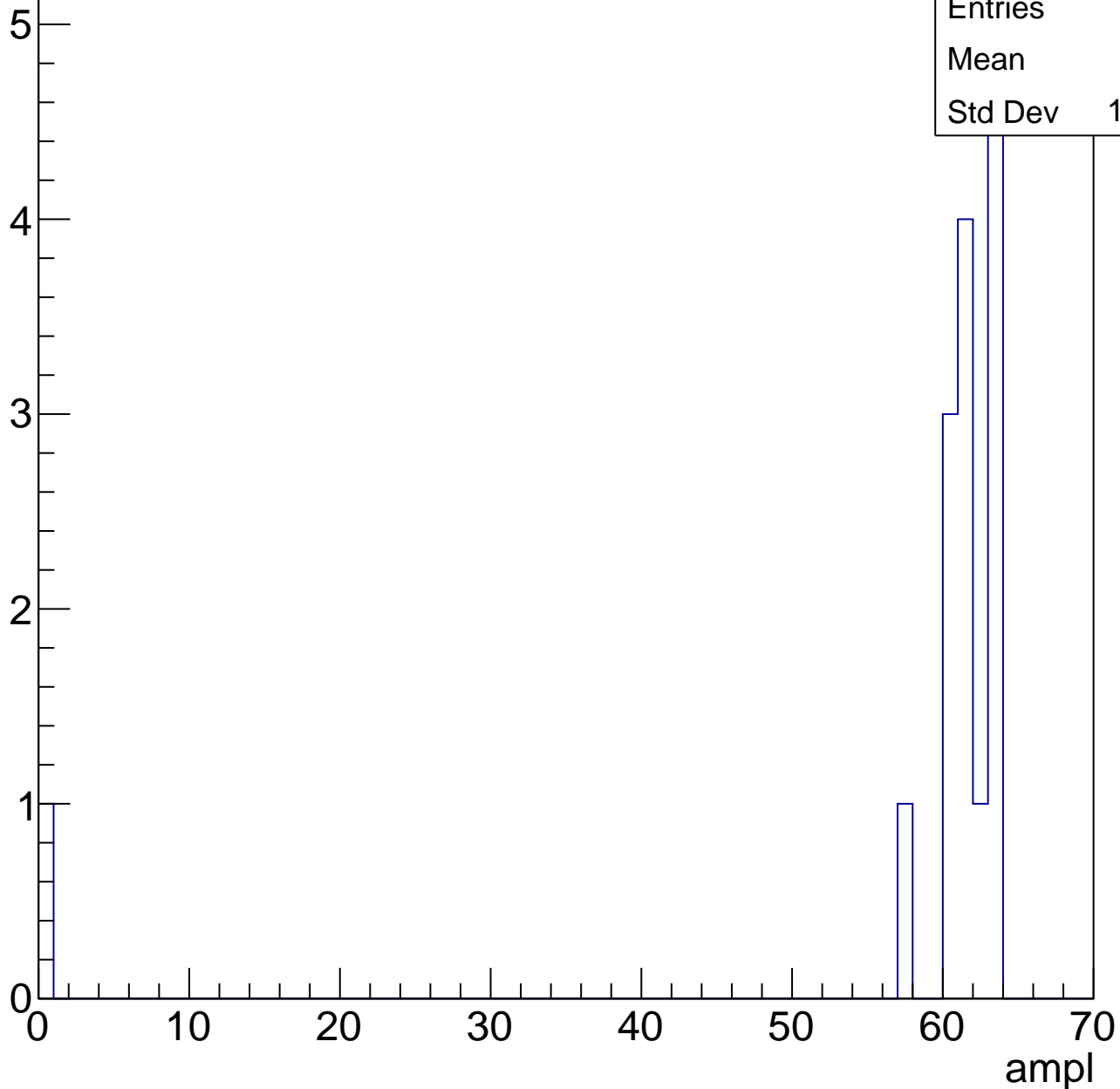


# B1L101S, U20-ch88, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	15
Mean	57.2
Std Dev	15.37





# B1L101S, U20-ch88, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U20-ch89, adc0

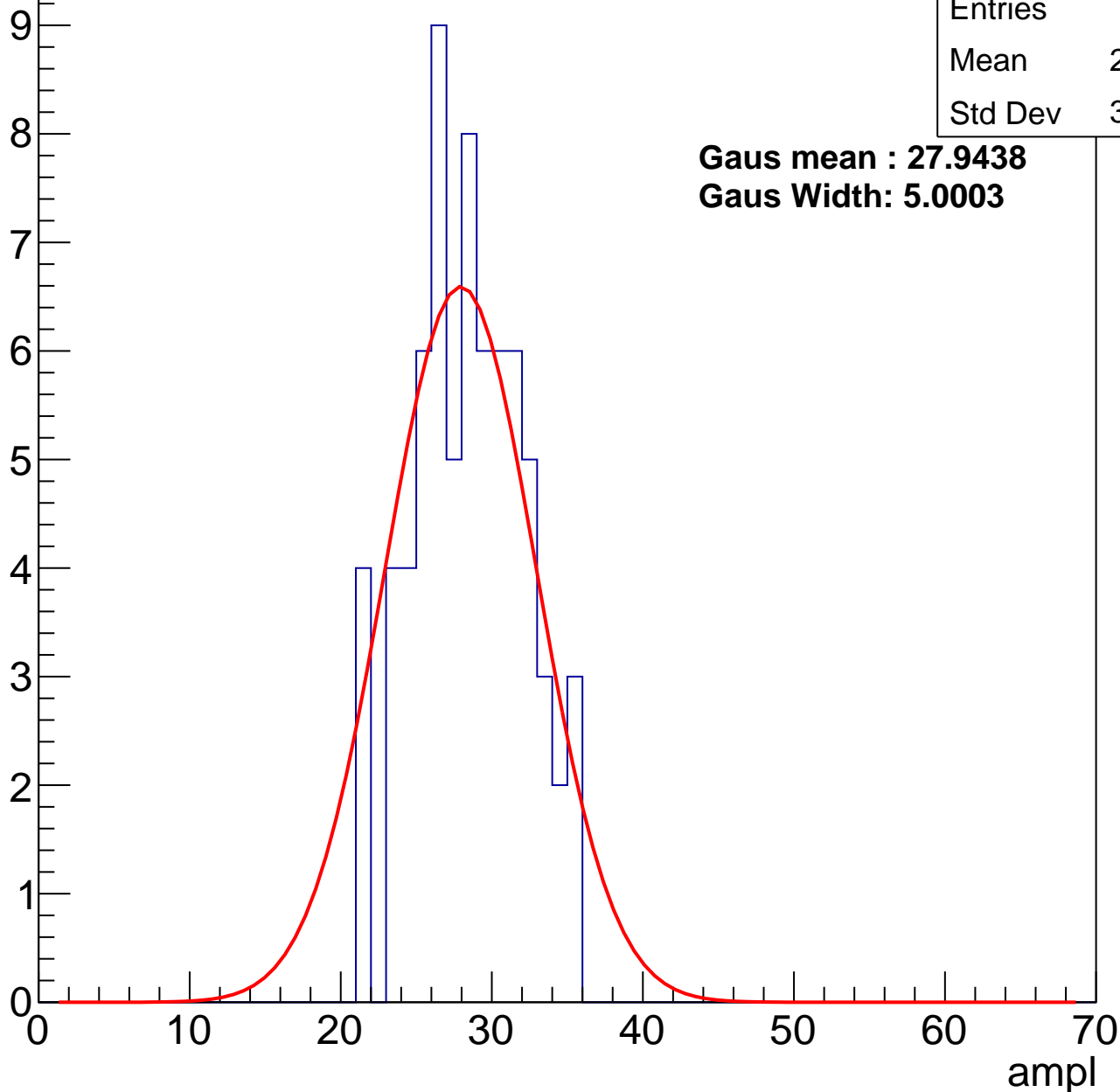
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	71
Mean	27.99
Std Dev	3.586

**Gaus mean : 27.9438**

**Gaus Width: 5.0003**



# B1L101S, U20-ch89, adc1

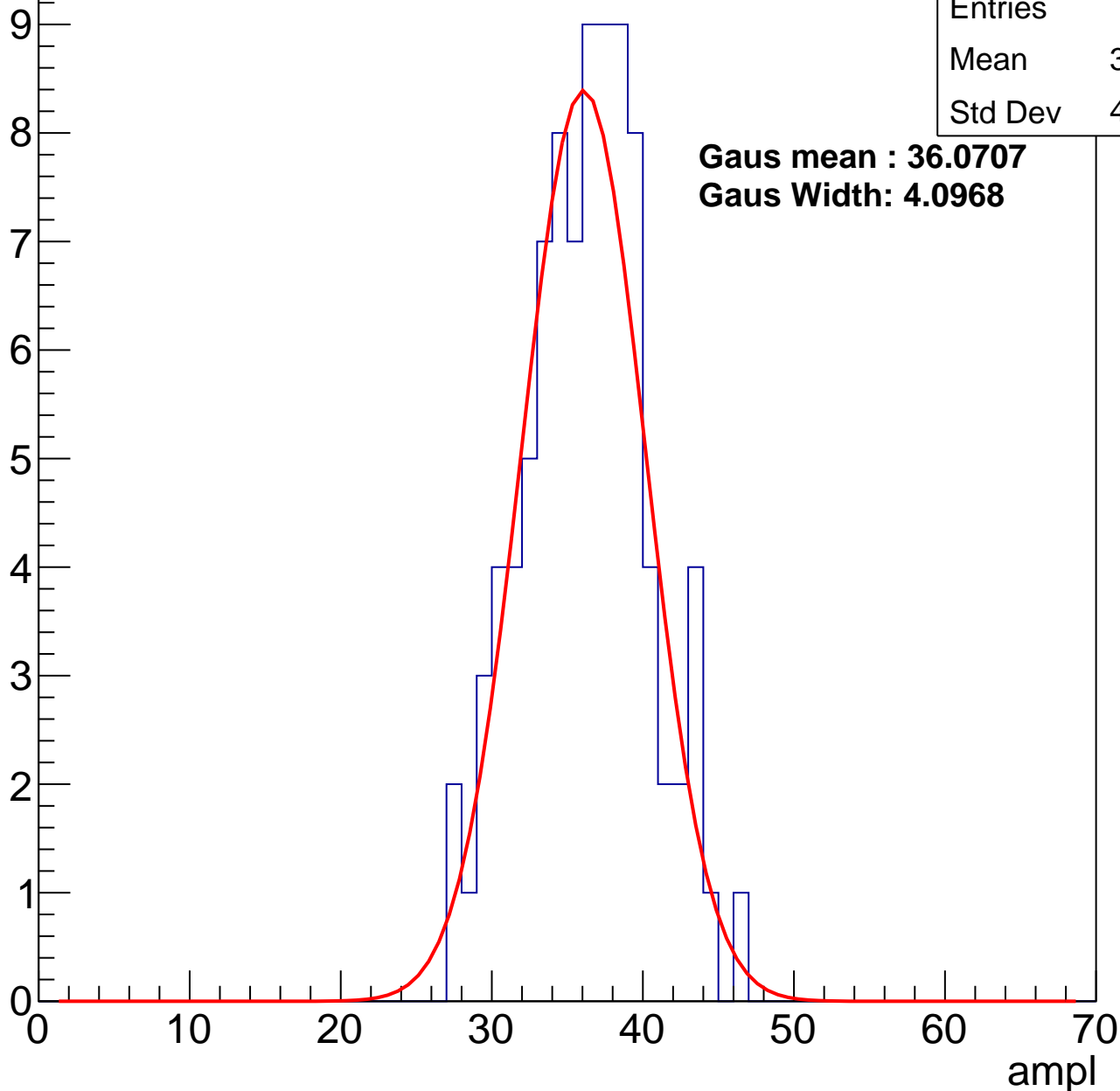
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	90
Mean	35.78
Std Dev	4.024

**Gaus mean : 36.0707**

**Gaus Width: 4.0968**



# B1L101S, U20-ch89, adc2

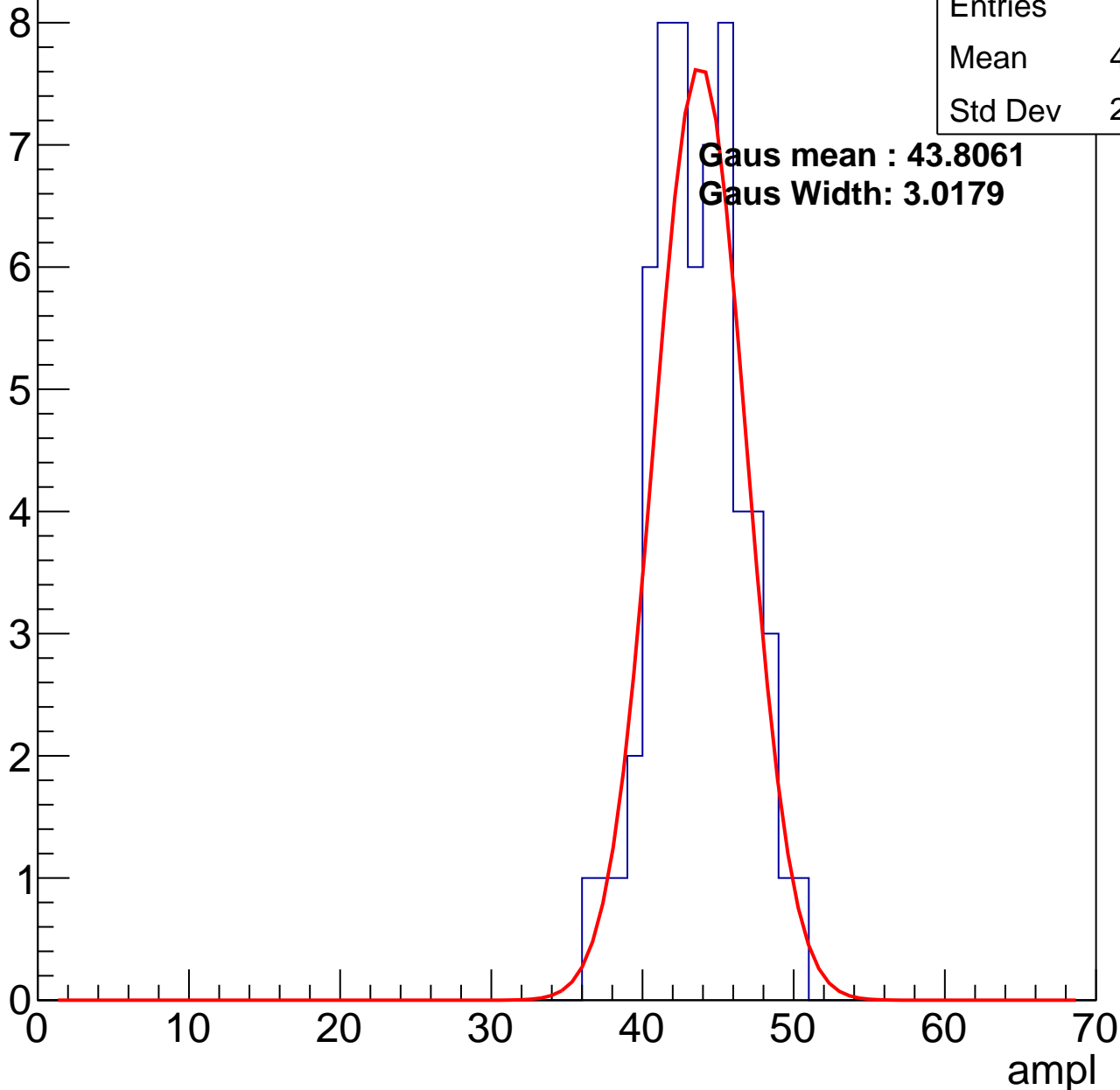
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	43.18
Std Dev	2.956

**Gaus mean : 43.8061**

**Gaus Width: 3.0179**

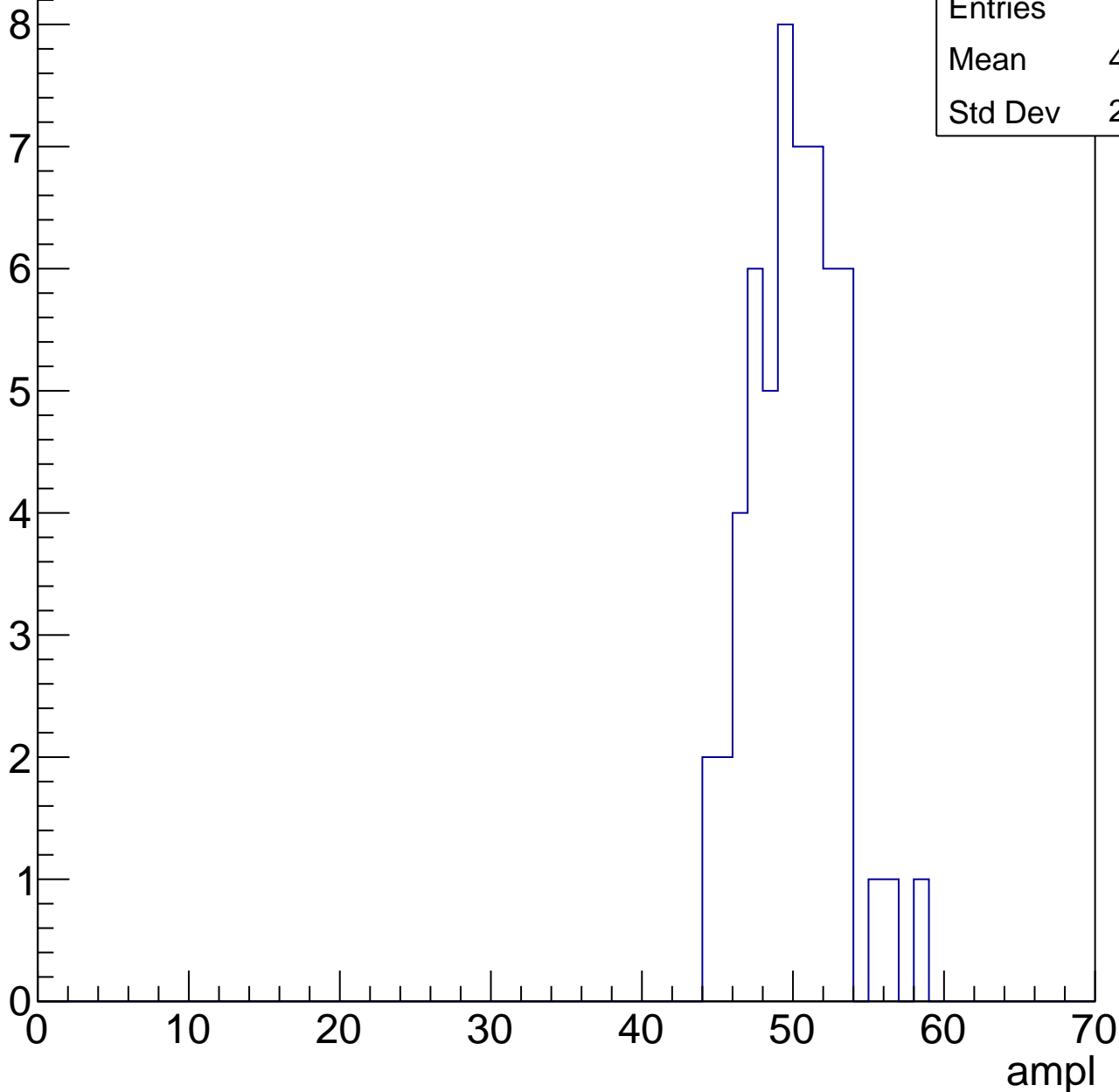


# B1L101S, U20-ch89, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	56
Mean	49.68
Std Dev	2.904

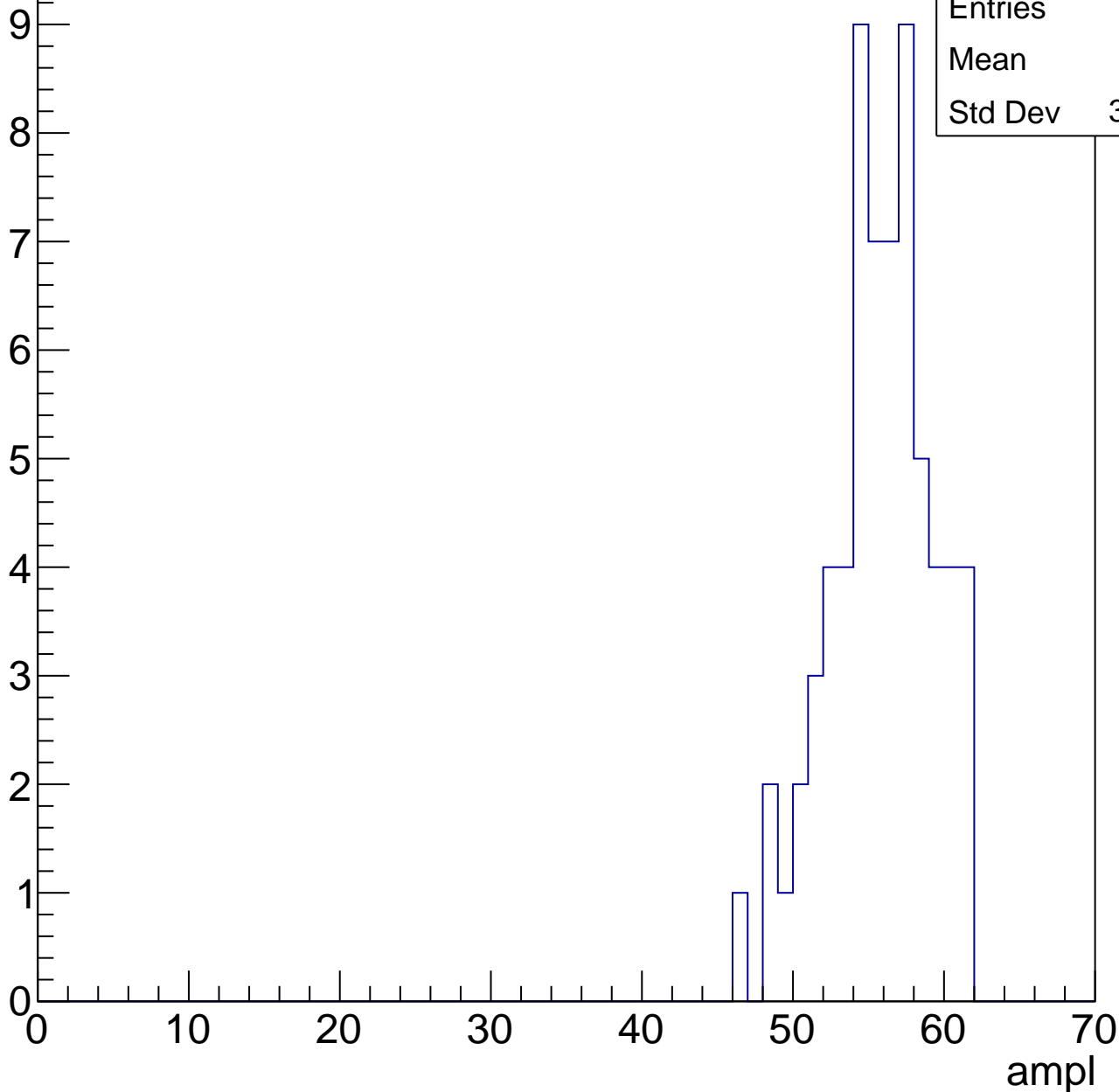


# B1L101S, U20-ch89, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	66
Mean	55.3
Std Dev	3.402



# B1L101S, U20-ch89, adc5

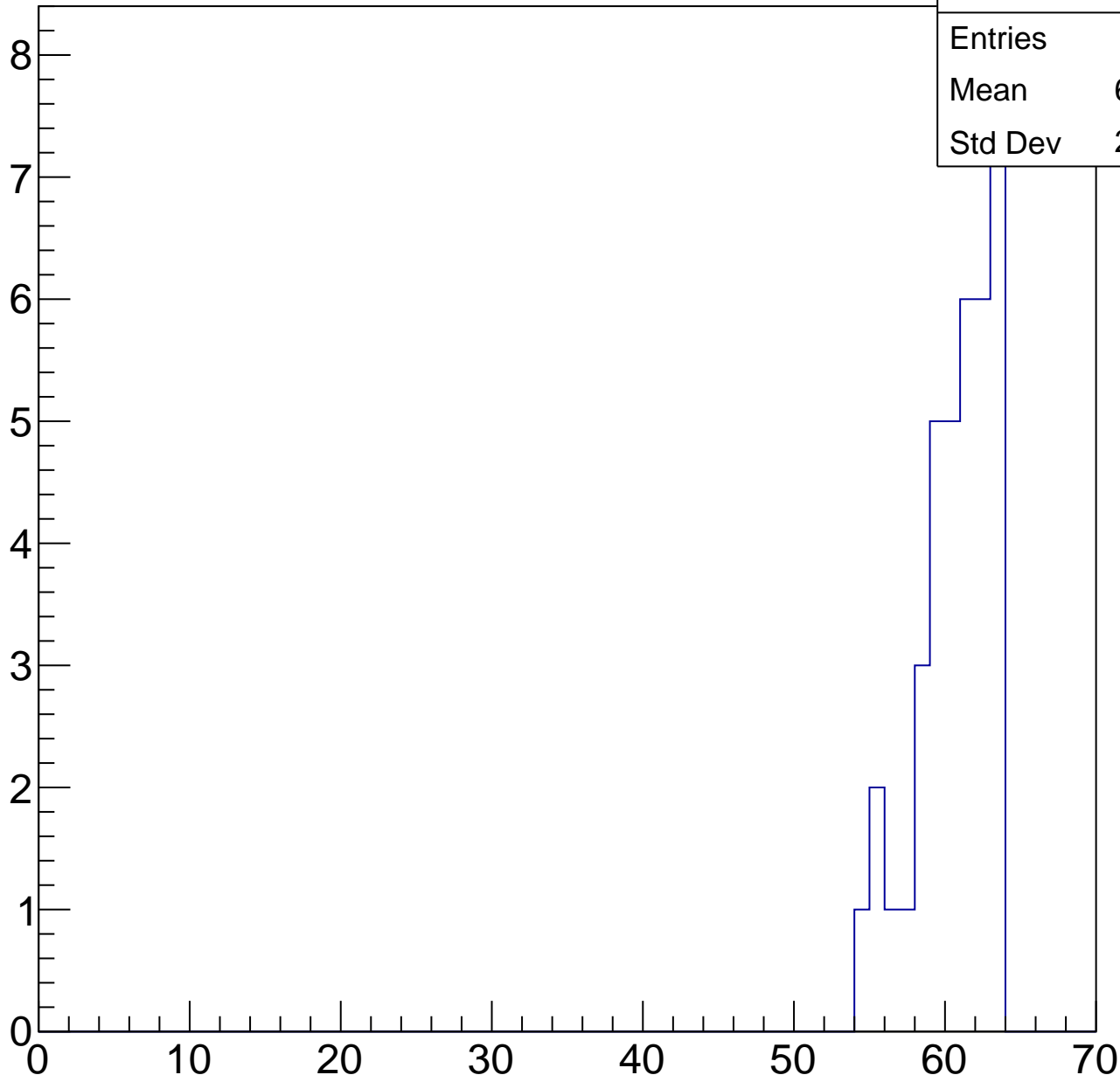
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	38
Mean	60.21
Std Dev	2.451

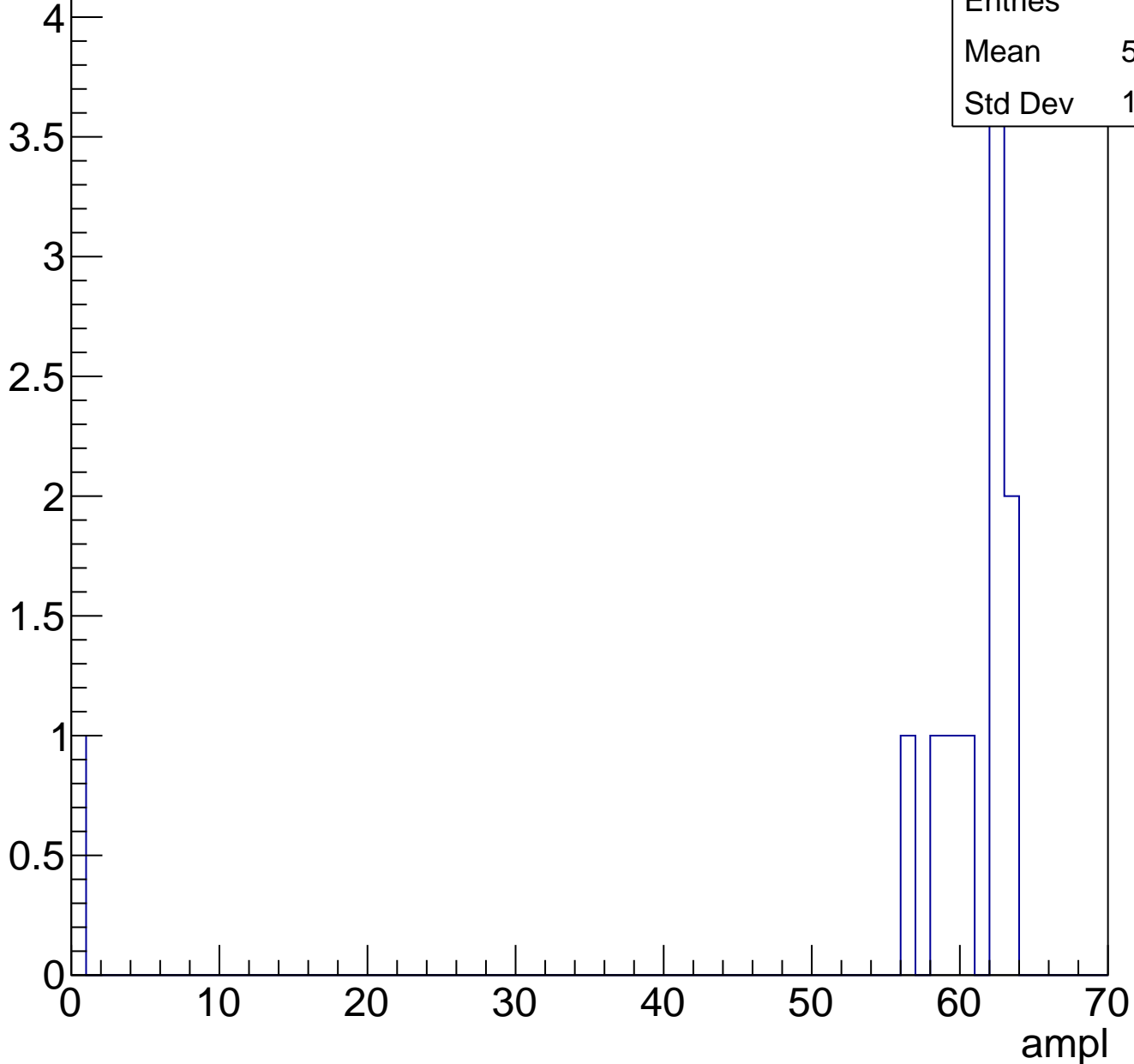
ampl



# B1L101S, U20-ch89, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U20-ch89, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U20-ch90, adc0

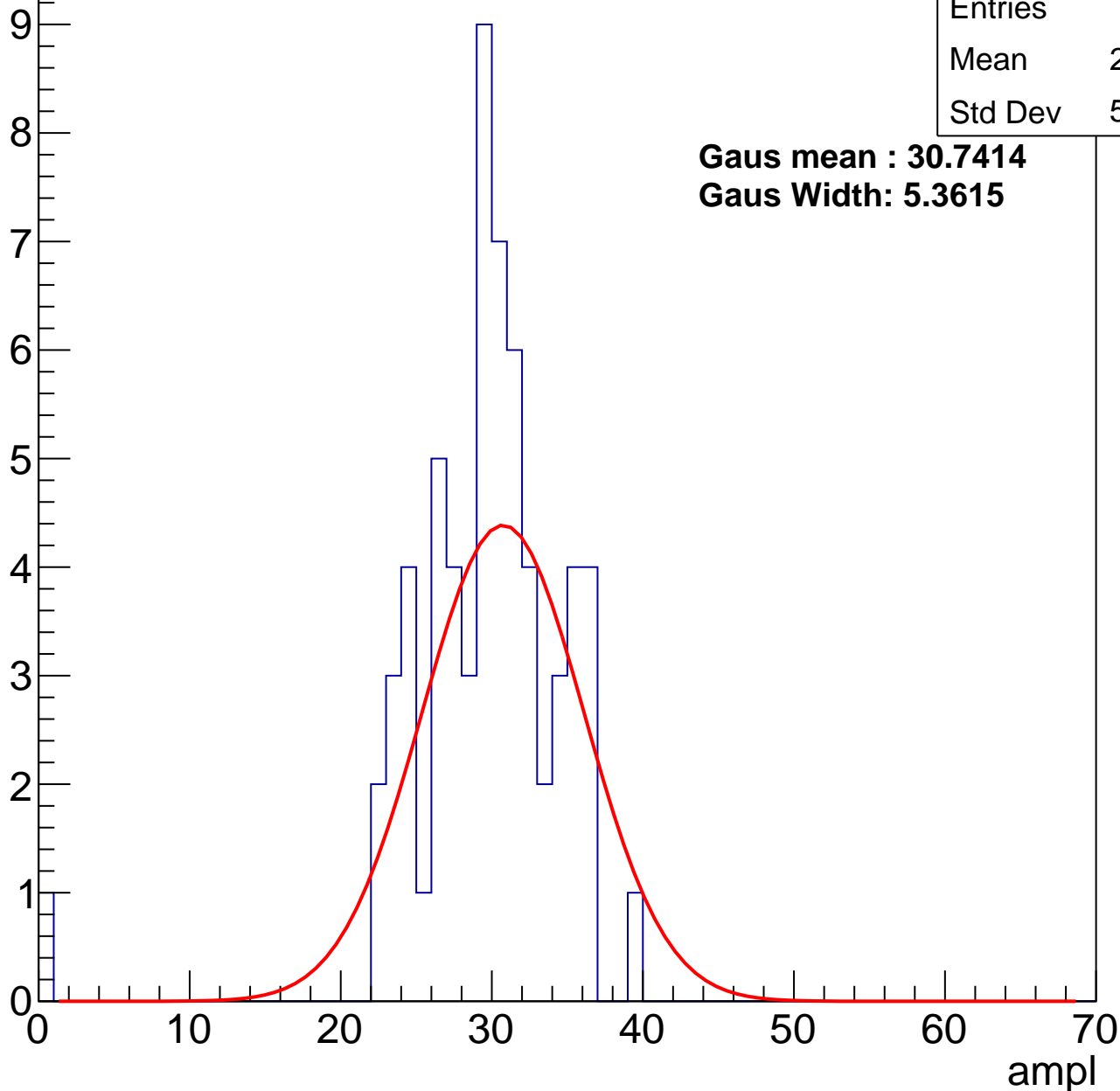
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	29.08
Std Dev	5.405

**Gaus mean : 30.7414**

**Gaus Width: 5.3615**



# B1L101S, U20-ch90, adc1

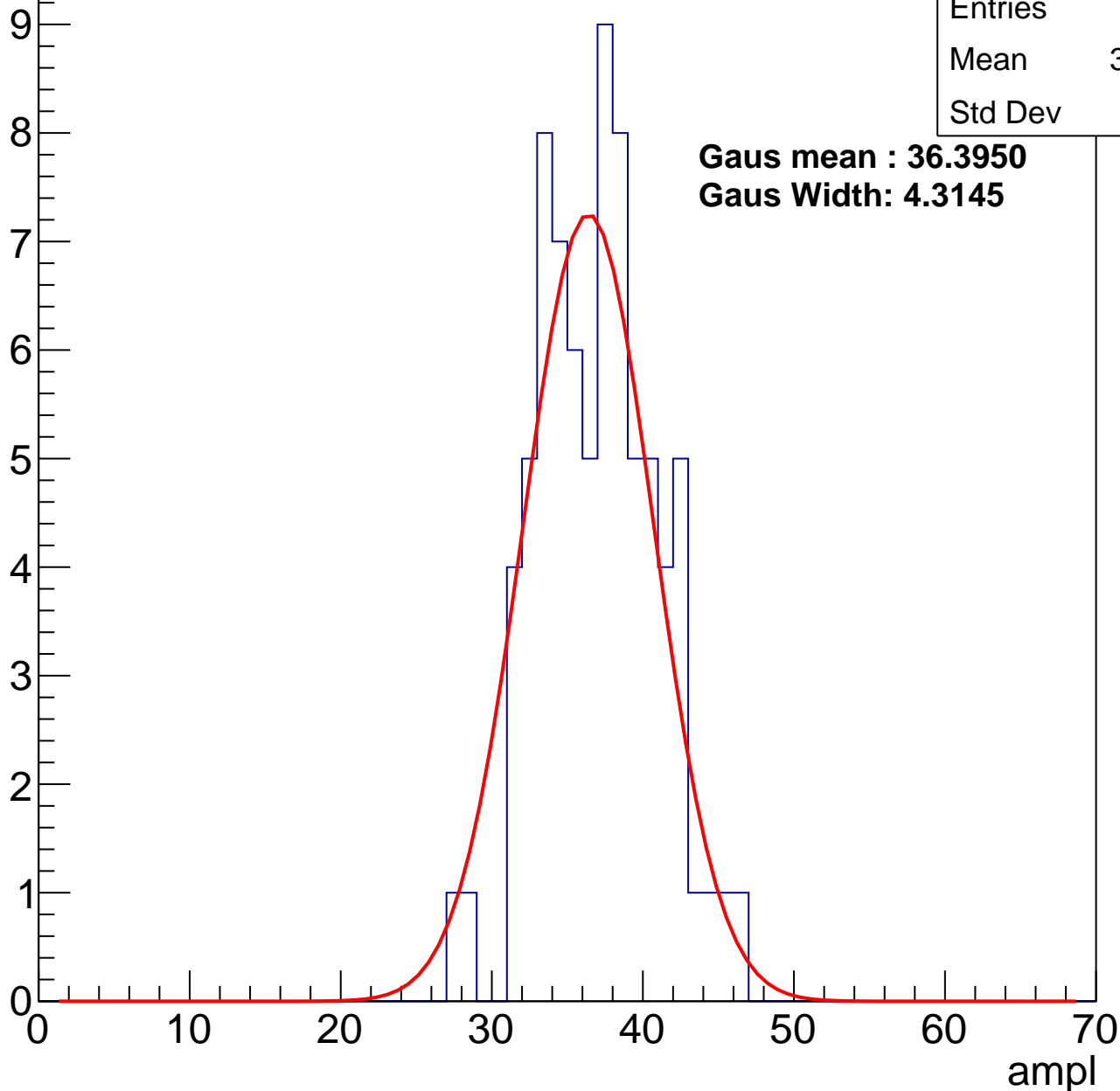
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	77
Mean	36.56
Std Dev	3.86

**Gaus mean : 36.3950**

**Gaus Width: 4.3145**



# B1L101S, U20-ch90, adc2

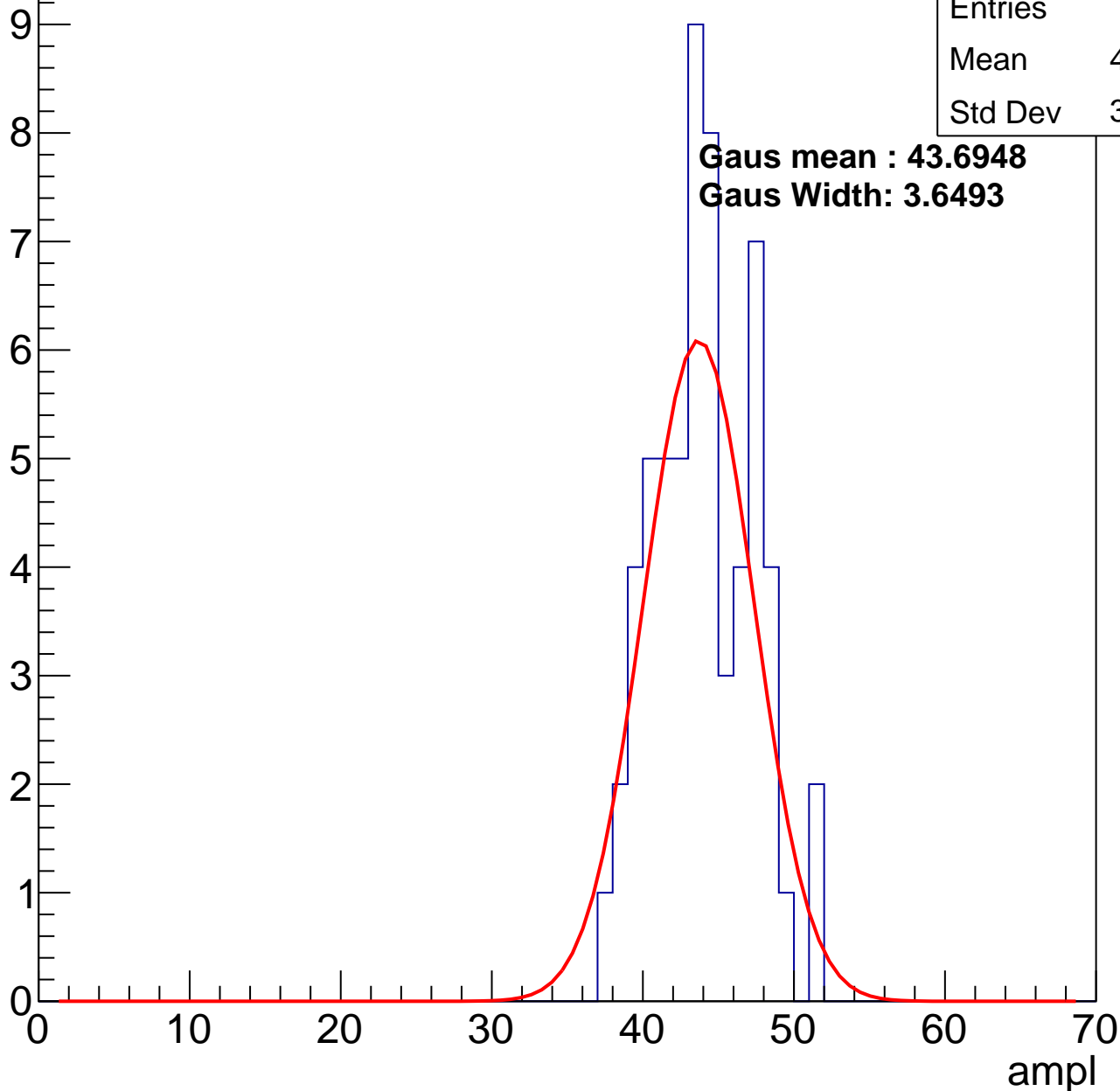
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	60
Mean	43.57
Std Dev	3.247

**Gaus mean : 43.6948**

**Gaus Width: 3.6493**

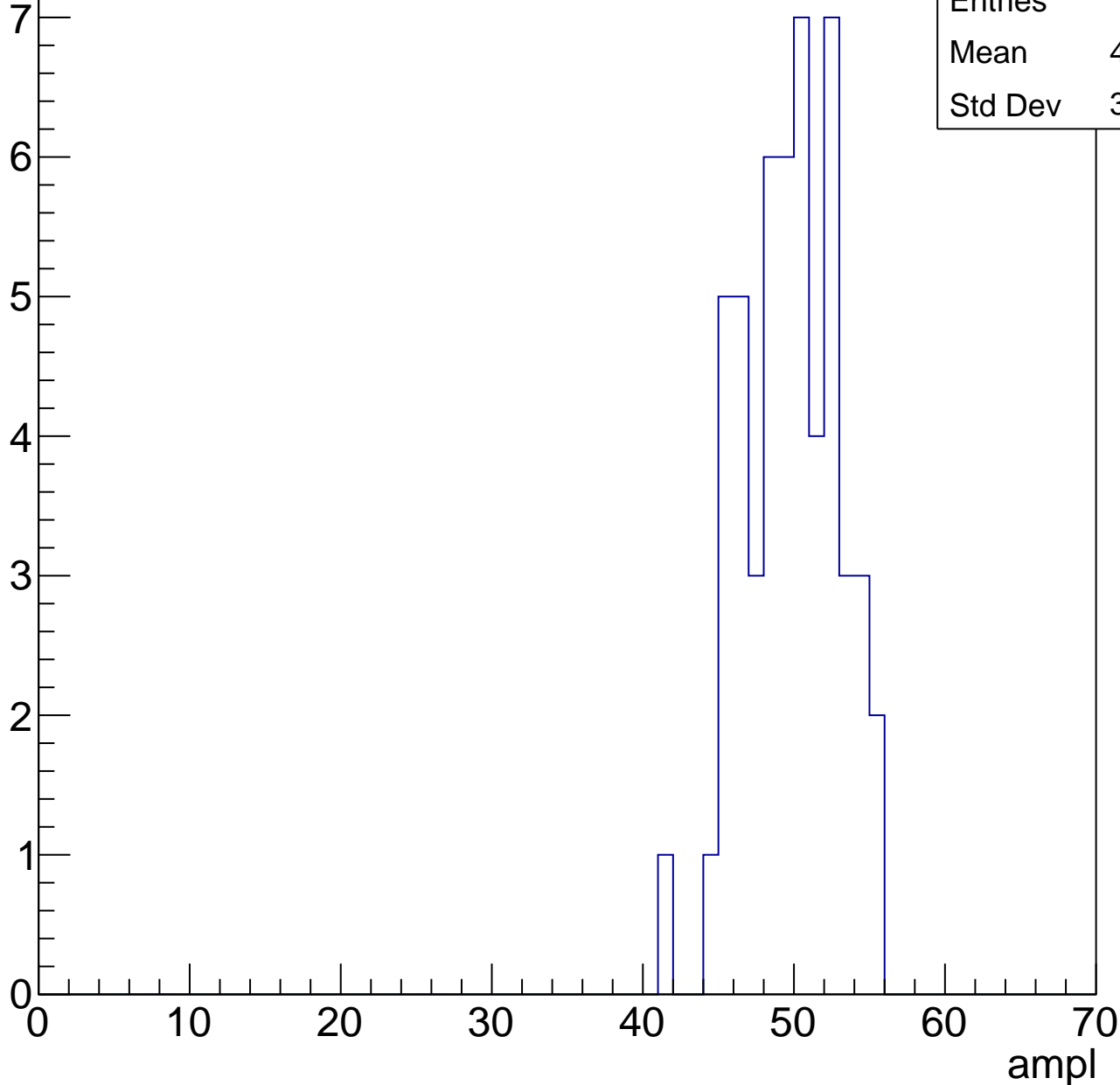


# B1L101S, U20-ch90, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	53
Mean	49.28
Std Dev	3.098

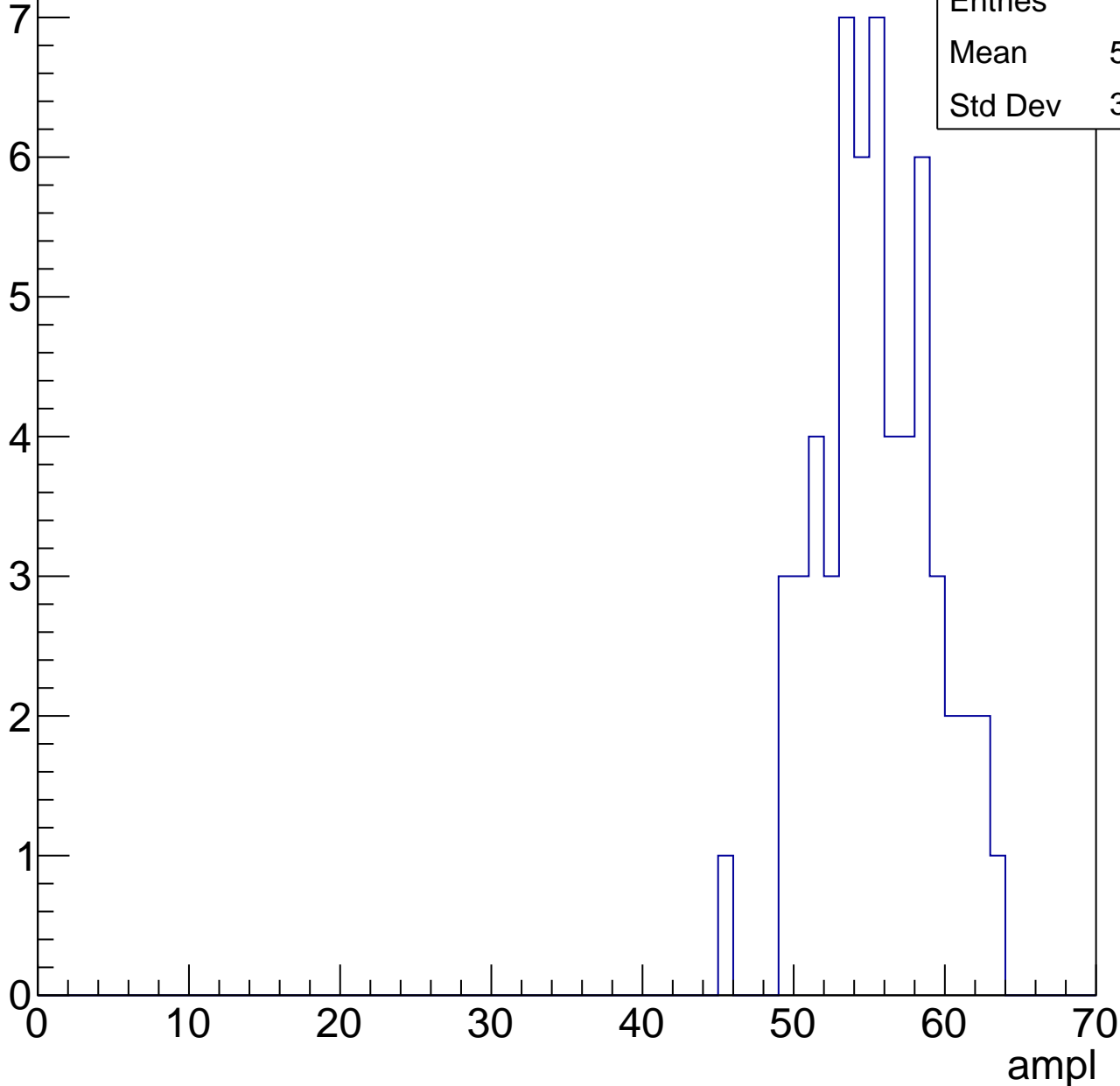


# B1L101S, U20-ch90, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

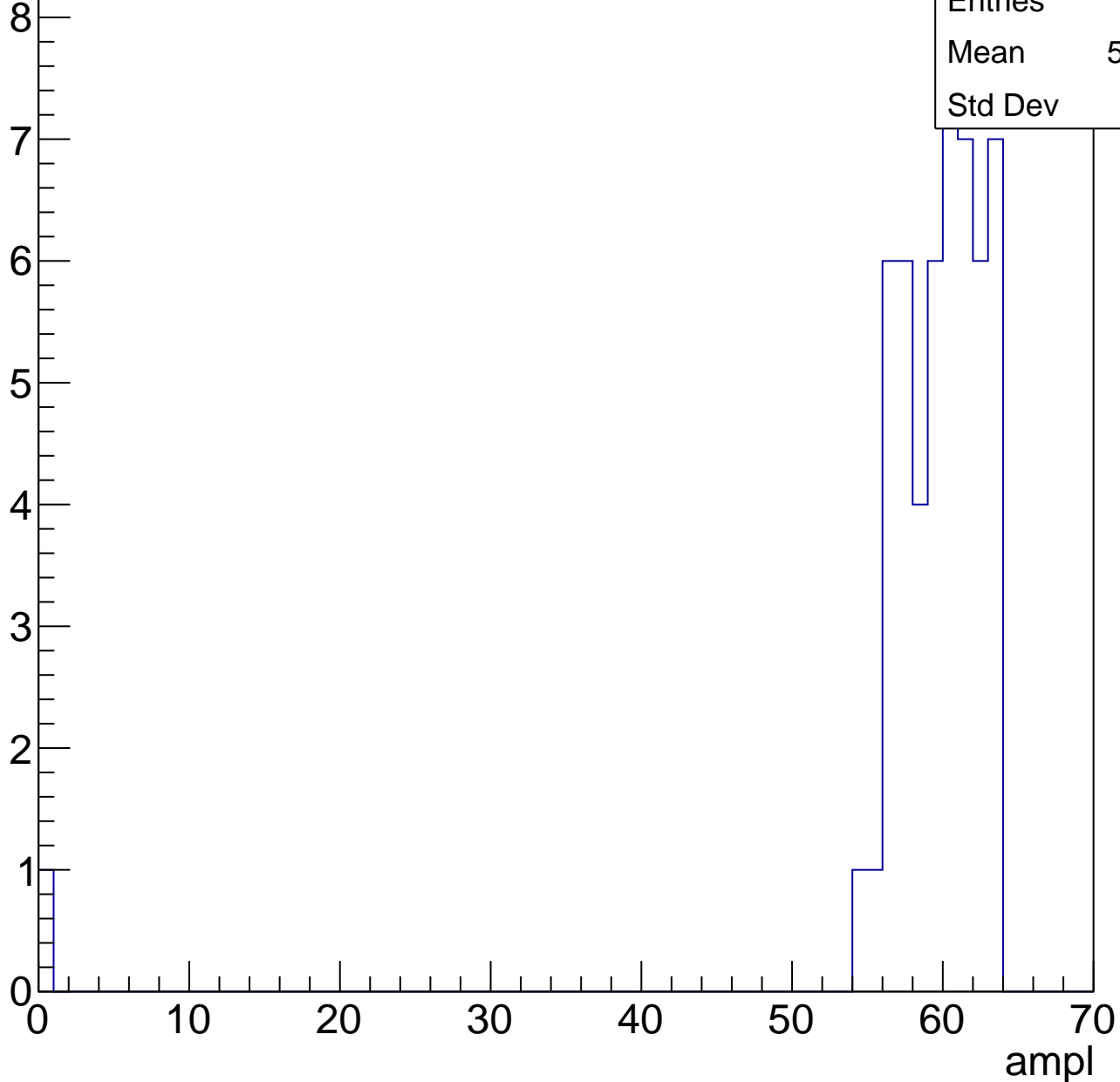
Entries	58
Mean	54.97
Std Dev	3.746



# B1L101S, U20-ch90, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

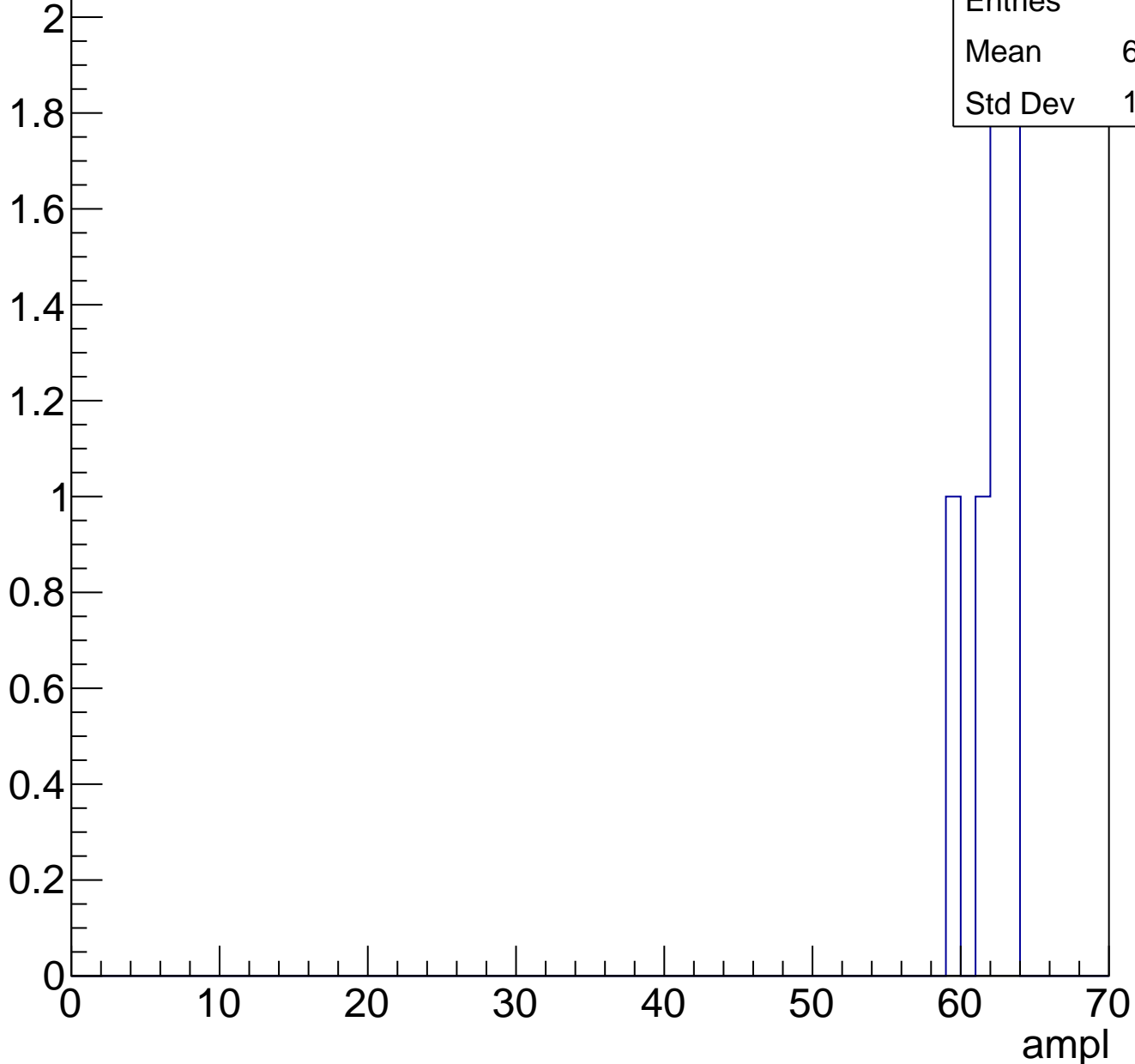
Entry



# B1L101S, U20-ch90, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U20-ch90, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U20-ch91, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	74
Mean	29.91
Std Dev	3.699

**Gaus mean : 30.2423**

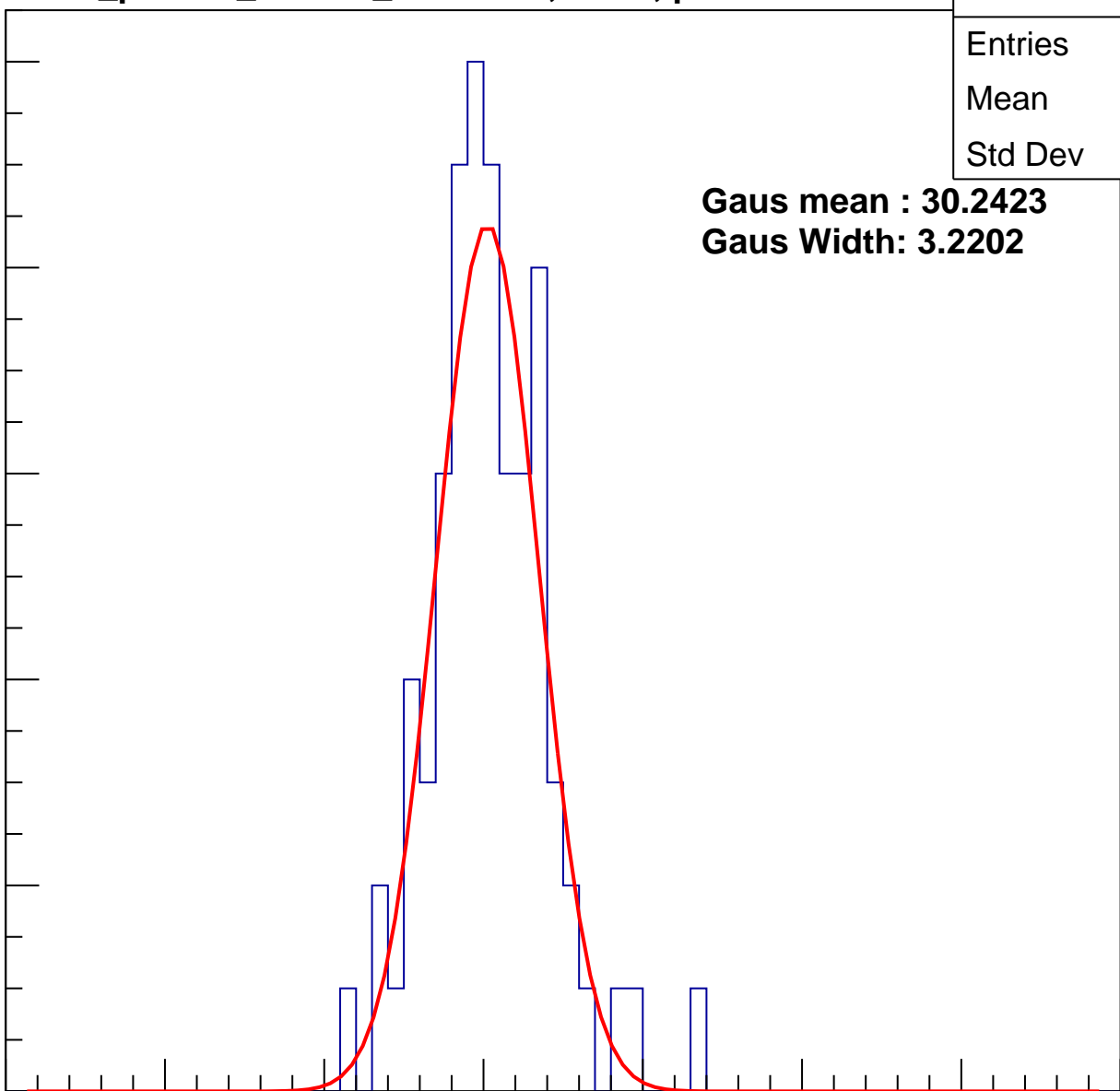
**Gaus Width: 3.2202**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U20-ch91, adc1

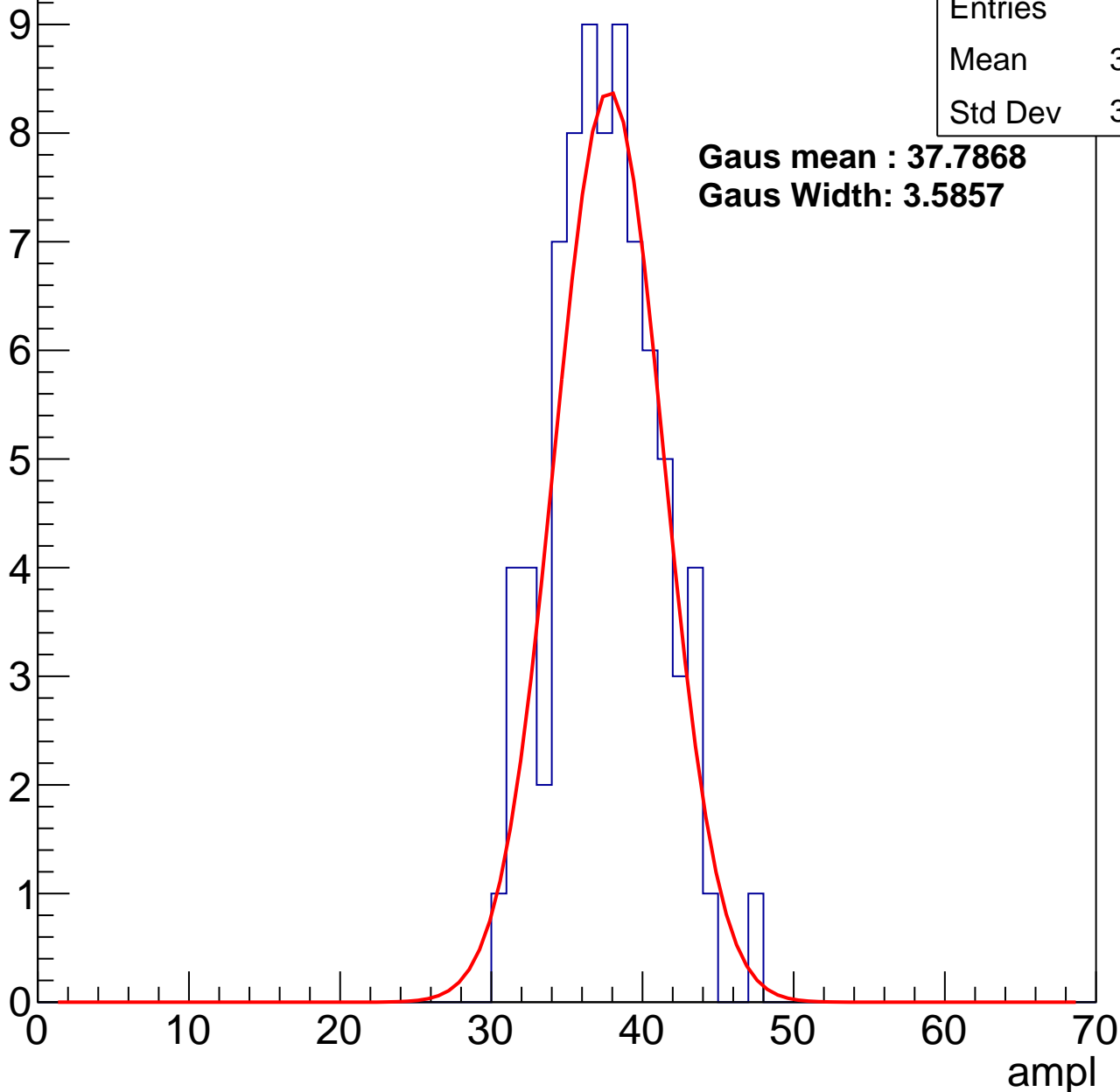
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	79
Mean	37.15
Std Dev	3.497

**Gaus mean : 37.7868**

**Gaus Width: 3.5857**



# B1L101S, U20-ch91, adc2

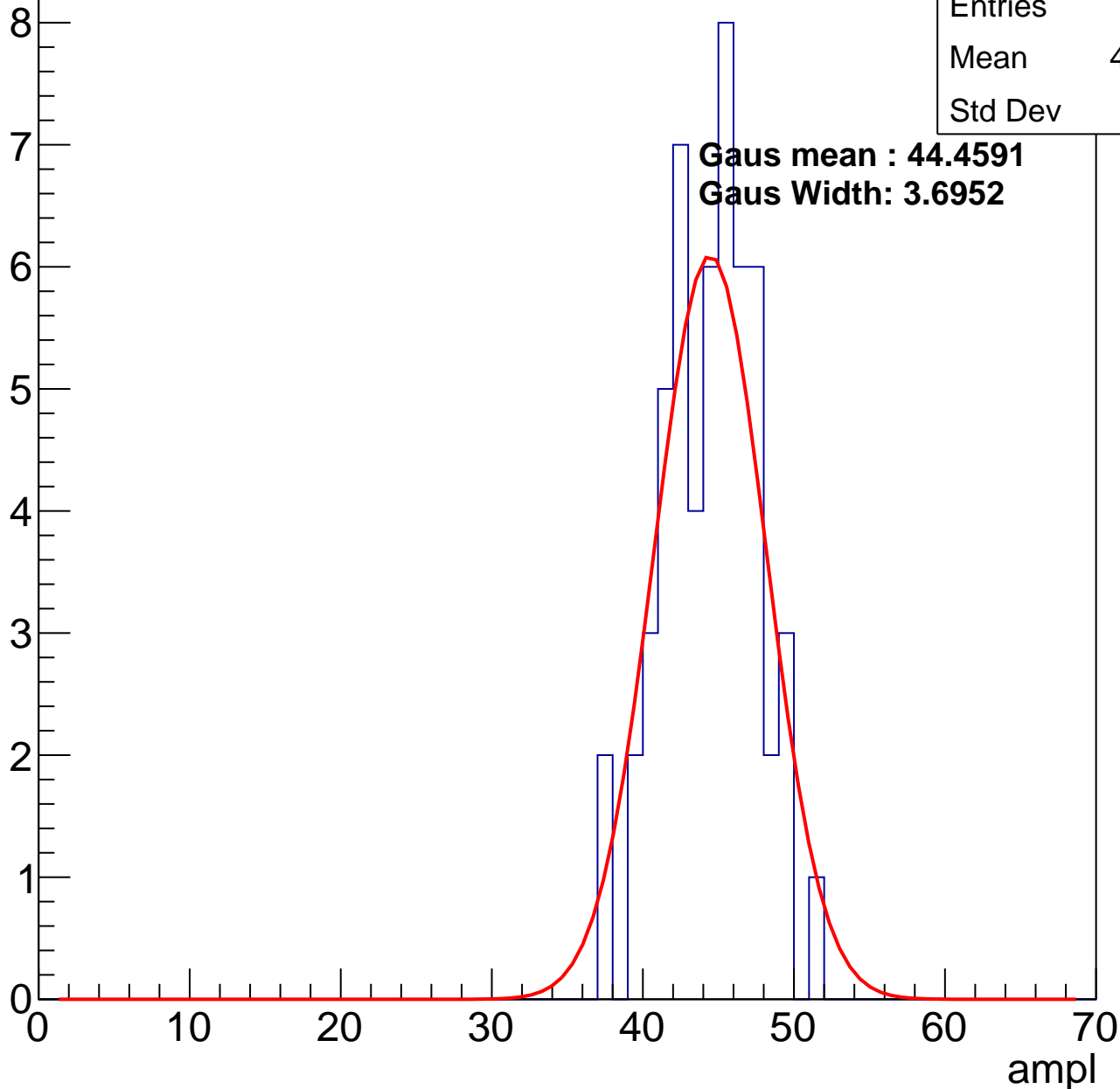
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	55
Mean	43.98
Std Dev	3.06

**Gaus mean : 44.4591**

**Gaus Width: 3.6952**

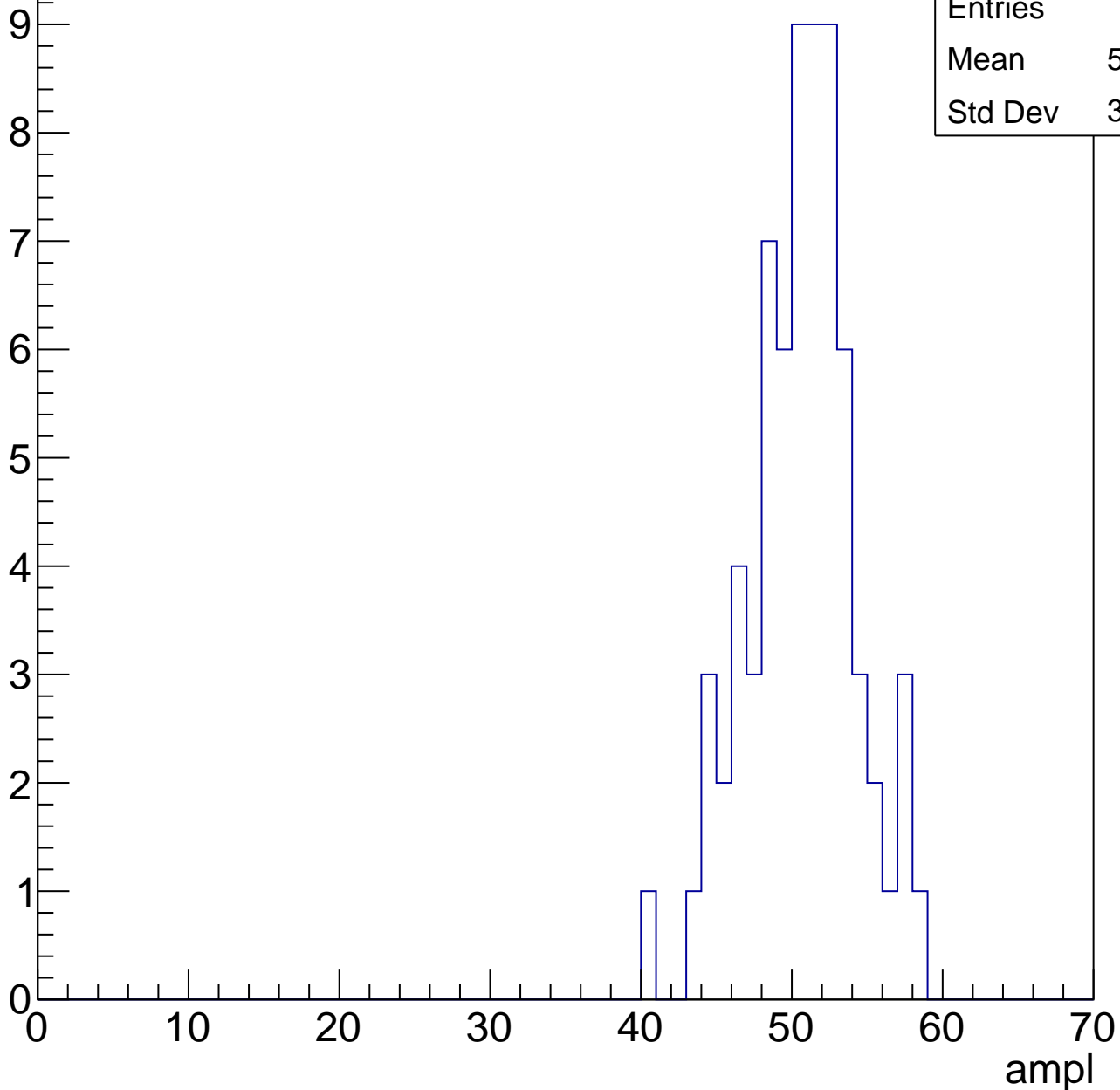


# B1L101S, U20-ch91, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	50.17
Std Dev	3.533

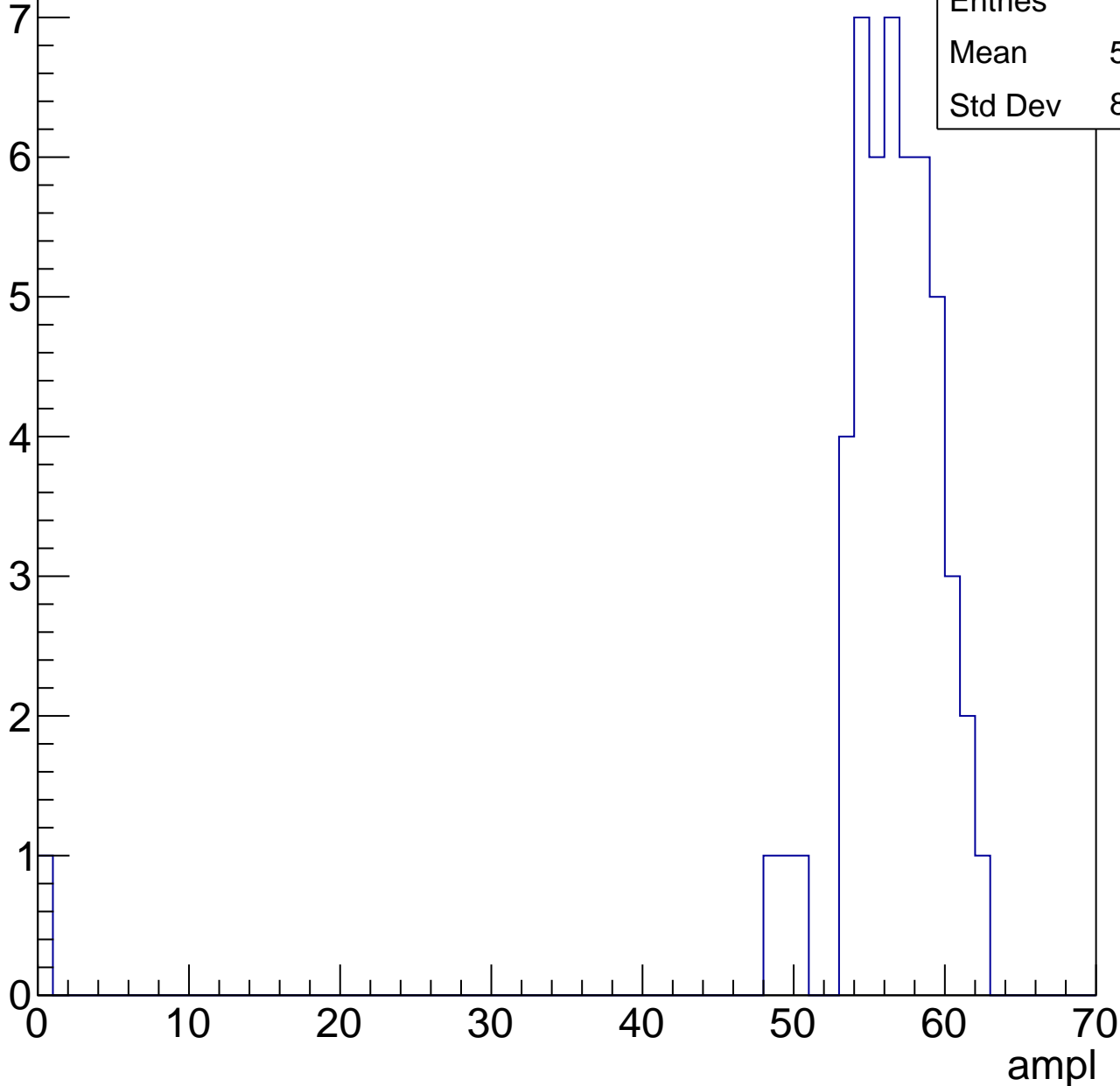


# B1L101S, U20-ch91, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

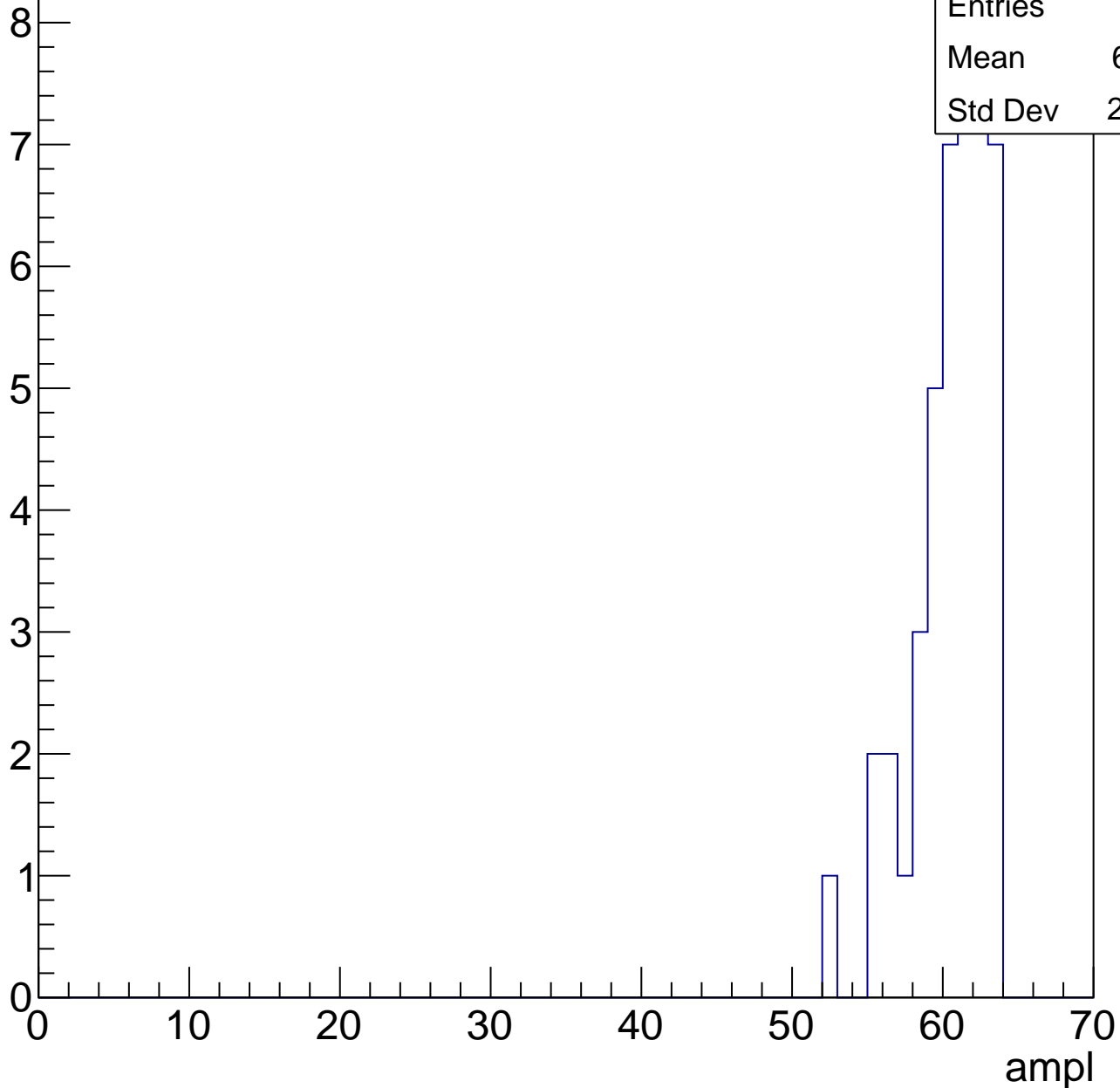
Entries	51
Mean	55.06
Std Dev	8.306



# B1L101S, U20-ch91, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U20-ch91, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U20-ch91, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L101S, U20-ch92, adc0

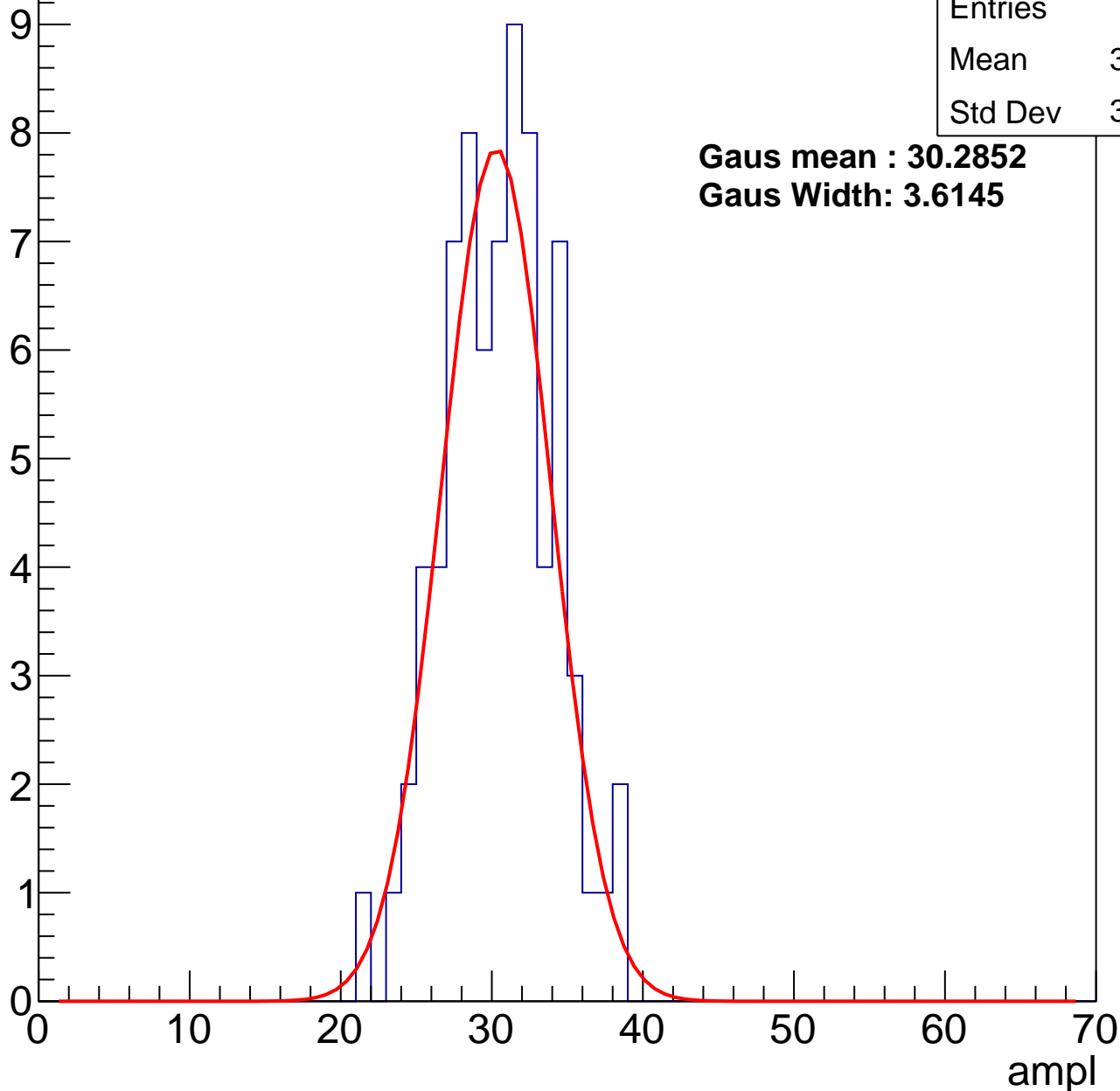
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	75
Mean	30.03
Std Dev	3.548

**Gaus mean : 30.2852**

**Gaus Width: 3.6145**



# B1L101S, U20-ch92, adc1

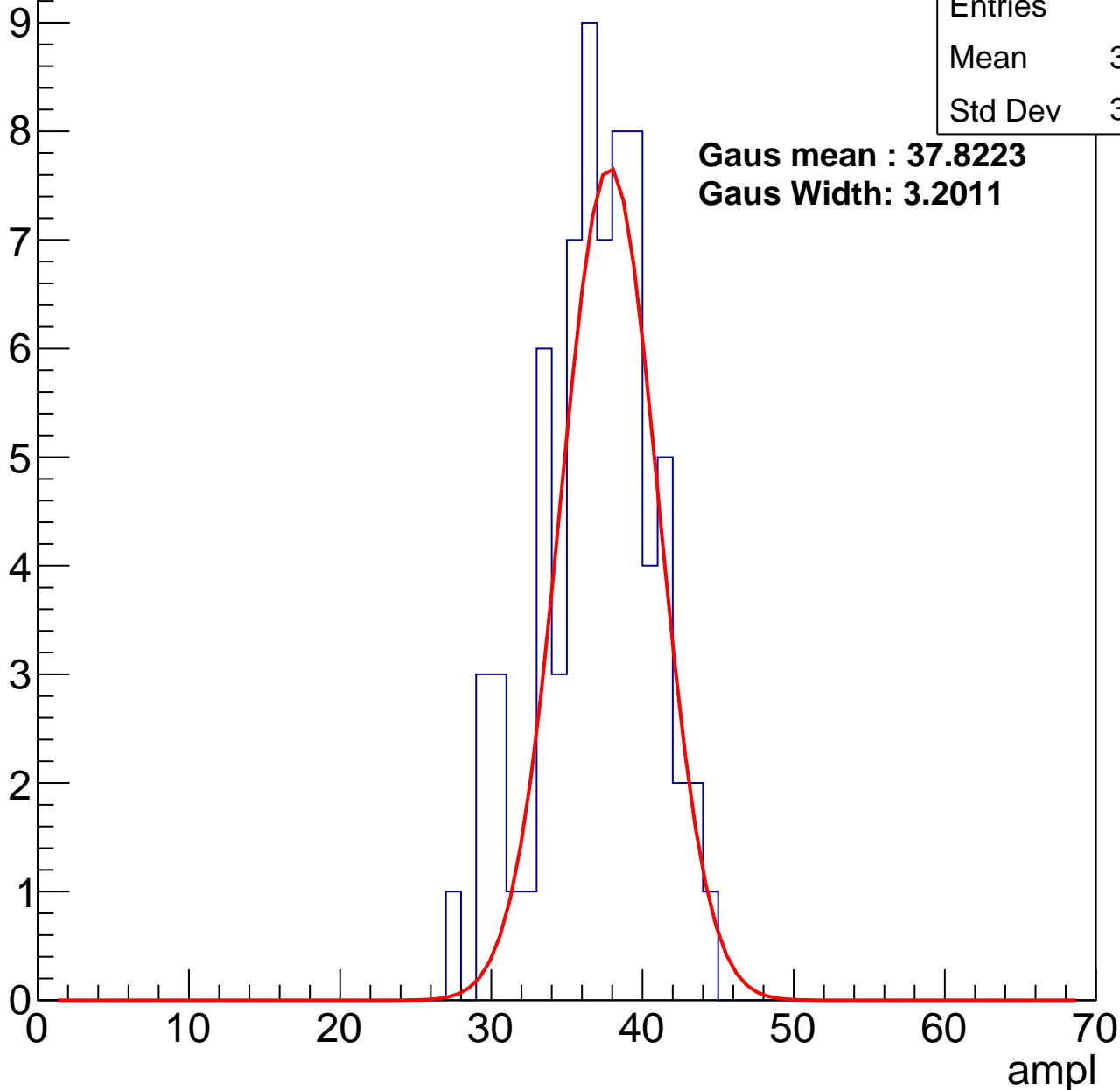
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	71
Mean	36.48
Std Dev	3.692

**Gaus mean : 37.8223**

**Gaus Width: 3.2011**



# B1L101S, U20-ch92, adc2

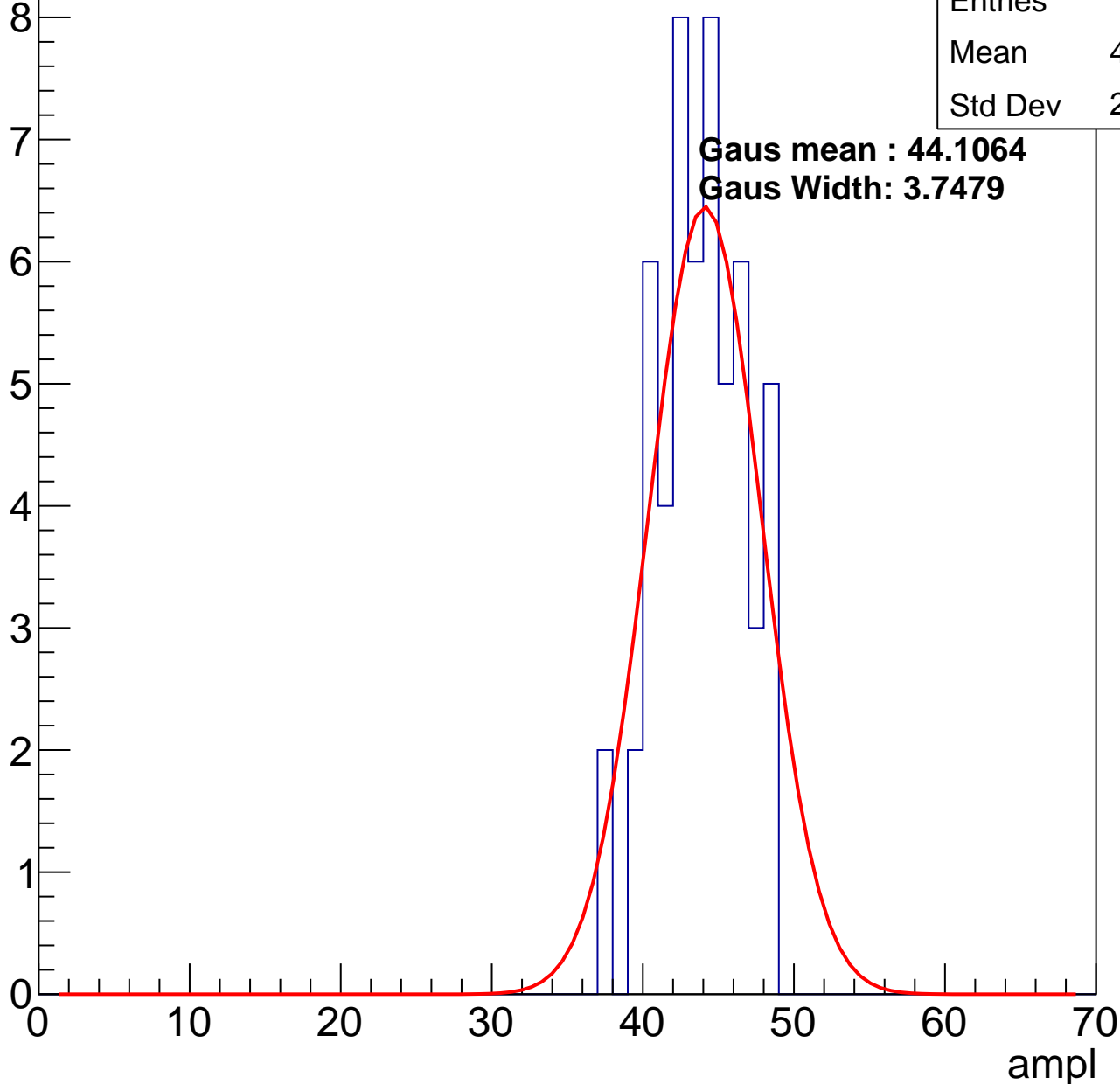
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	55
Mean	43.35
Std Dev	2.798

**Gaus mean : 44.1064**

**Gaus Width: 3.7479**



# B1L101S, U20-ch92, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	67
Mean	49.43
Std Dev	3.329

Entry

10

8

6

4

2

0

0

10

20

30

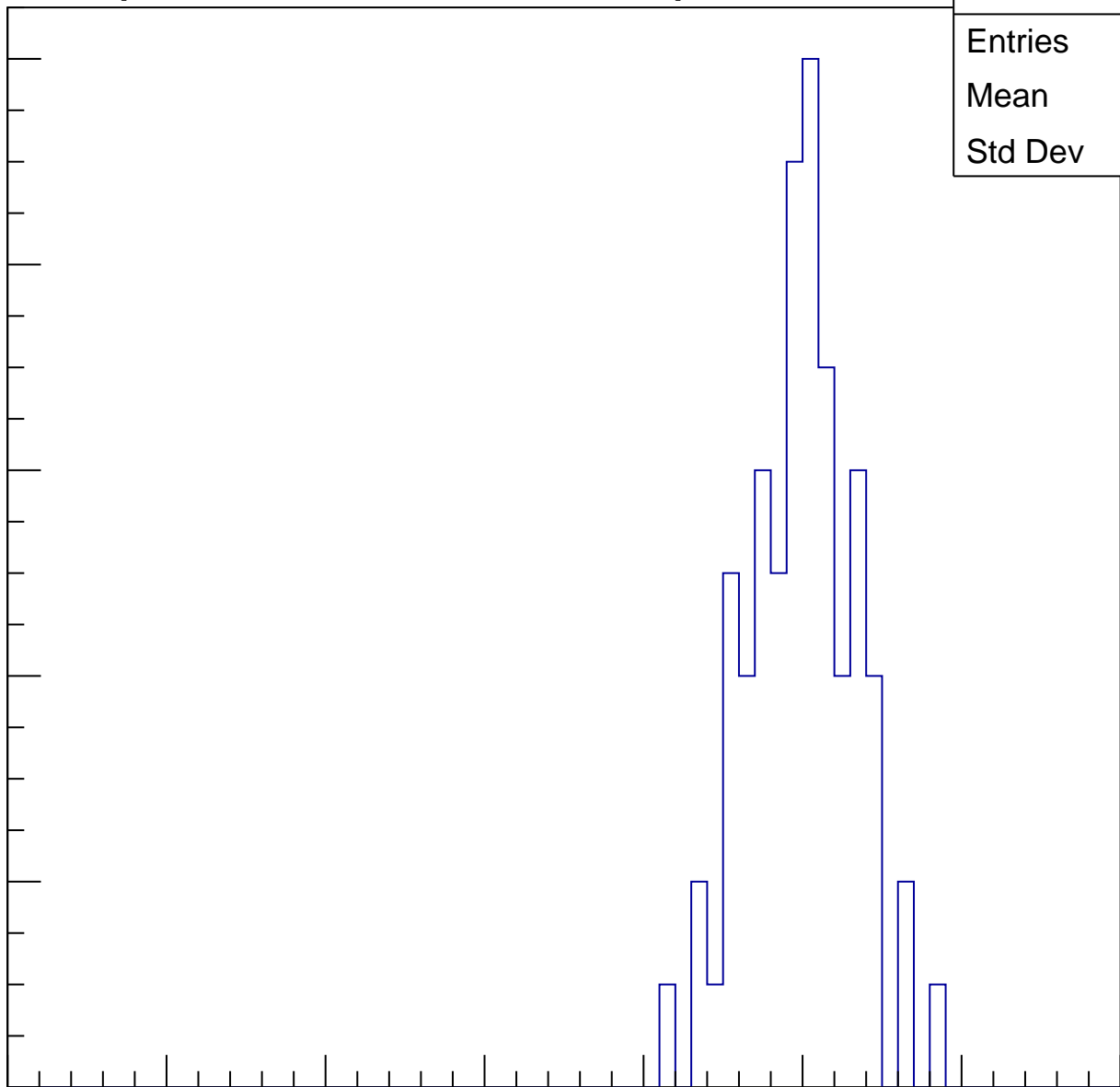
40

50

60

ampl

70

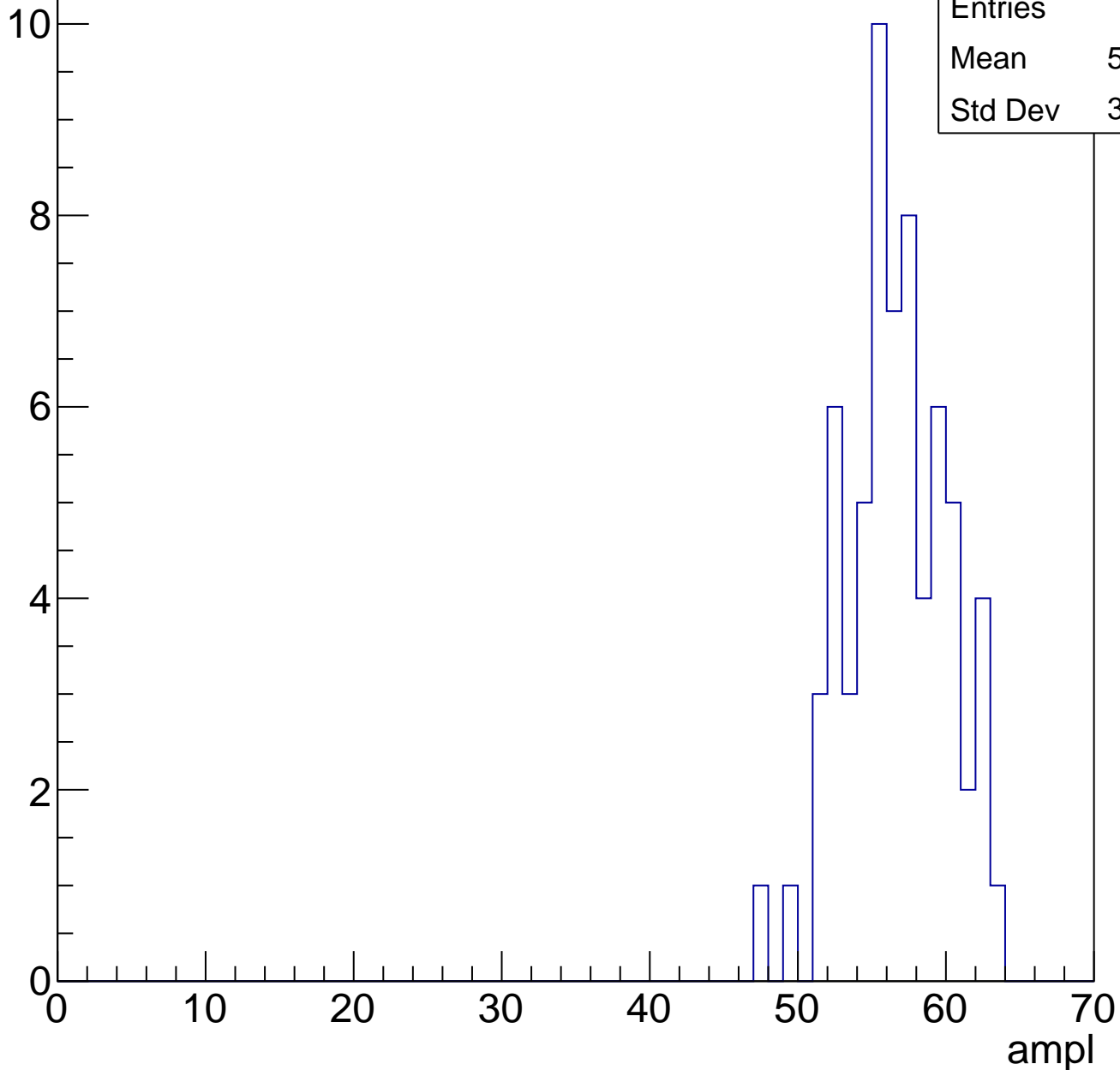


# B1L101S, U20-ch92, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	66
Mean	56.17
Std Dev	3.387

Entry

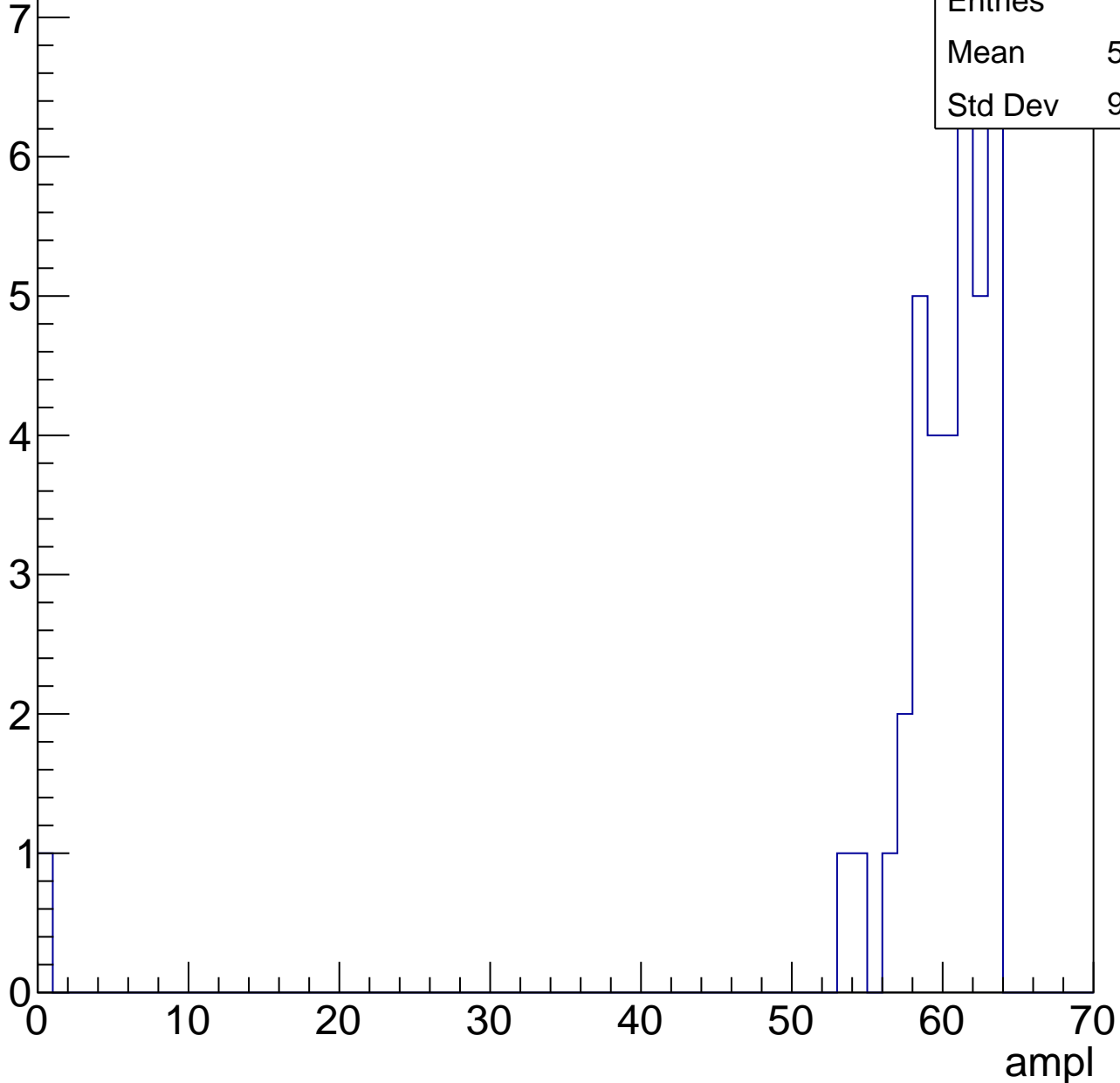


# B1L101S, U20-ch92, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	38
Mean	58.45
Std Dev	9.923



# B1L101S, U20-ch92, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

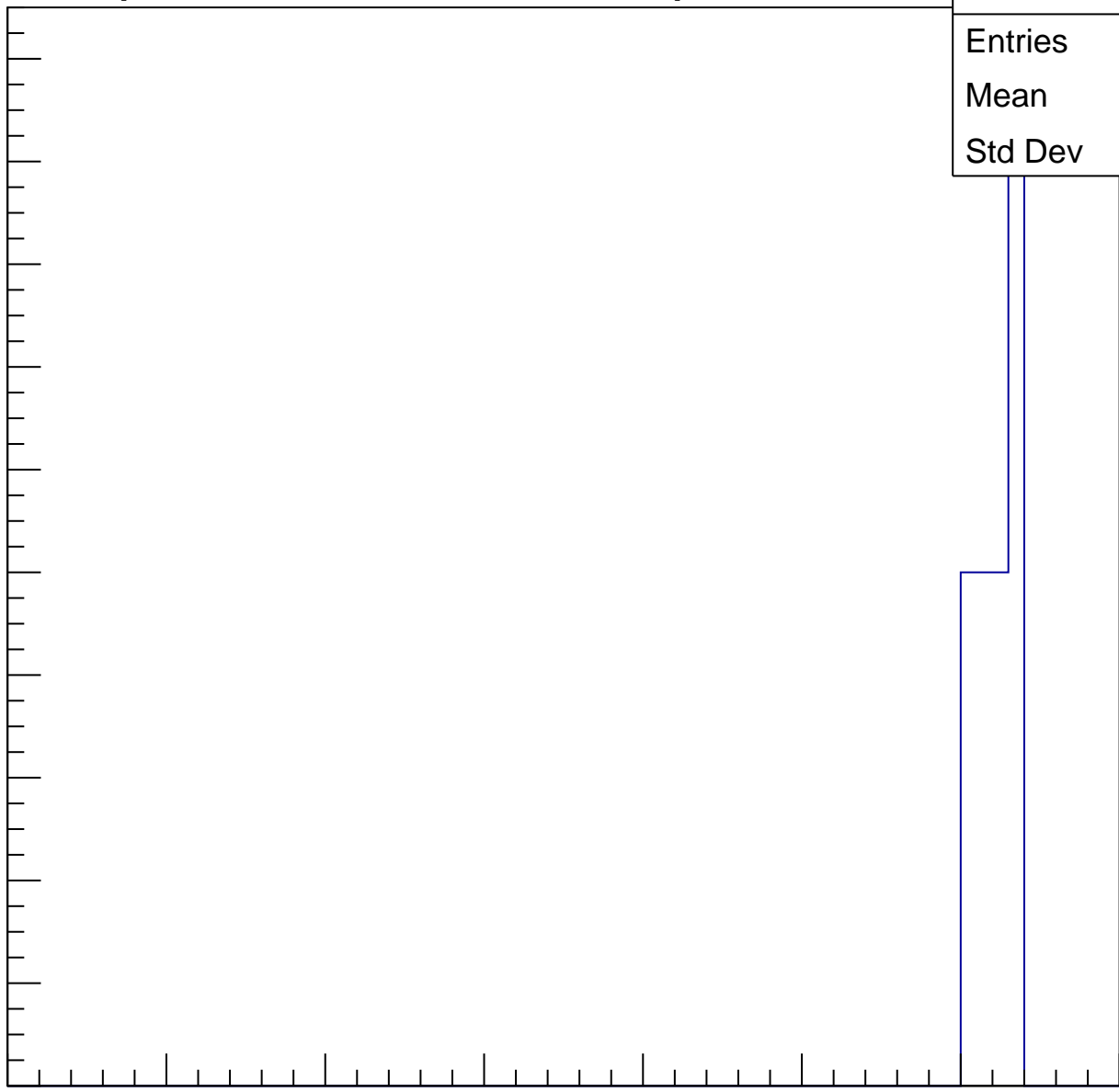
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	5
Mean	61.8
Std Dev	1.166

ampl

0 10 20 30 40 50 60 70





# B1L101S, U20-ch92, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U20-ch93, adc0

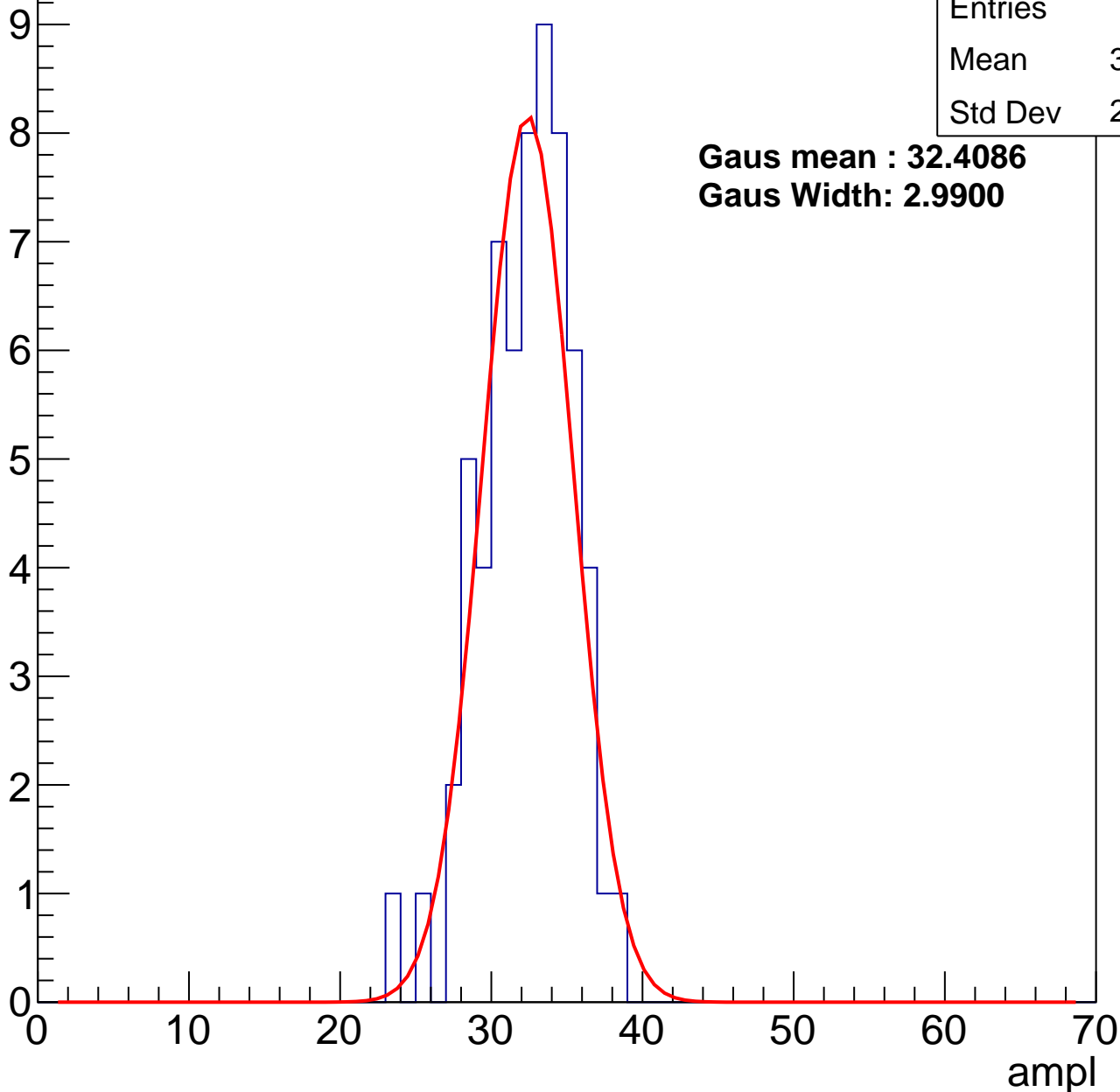
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	31.87
Std Dev	2.952

**Gaus mean : 32.4086**

**Gaus Width: 2.9900**



# B1L101S, U20-ch93, adc1

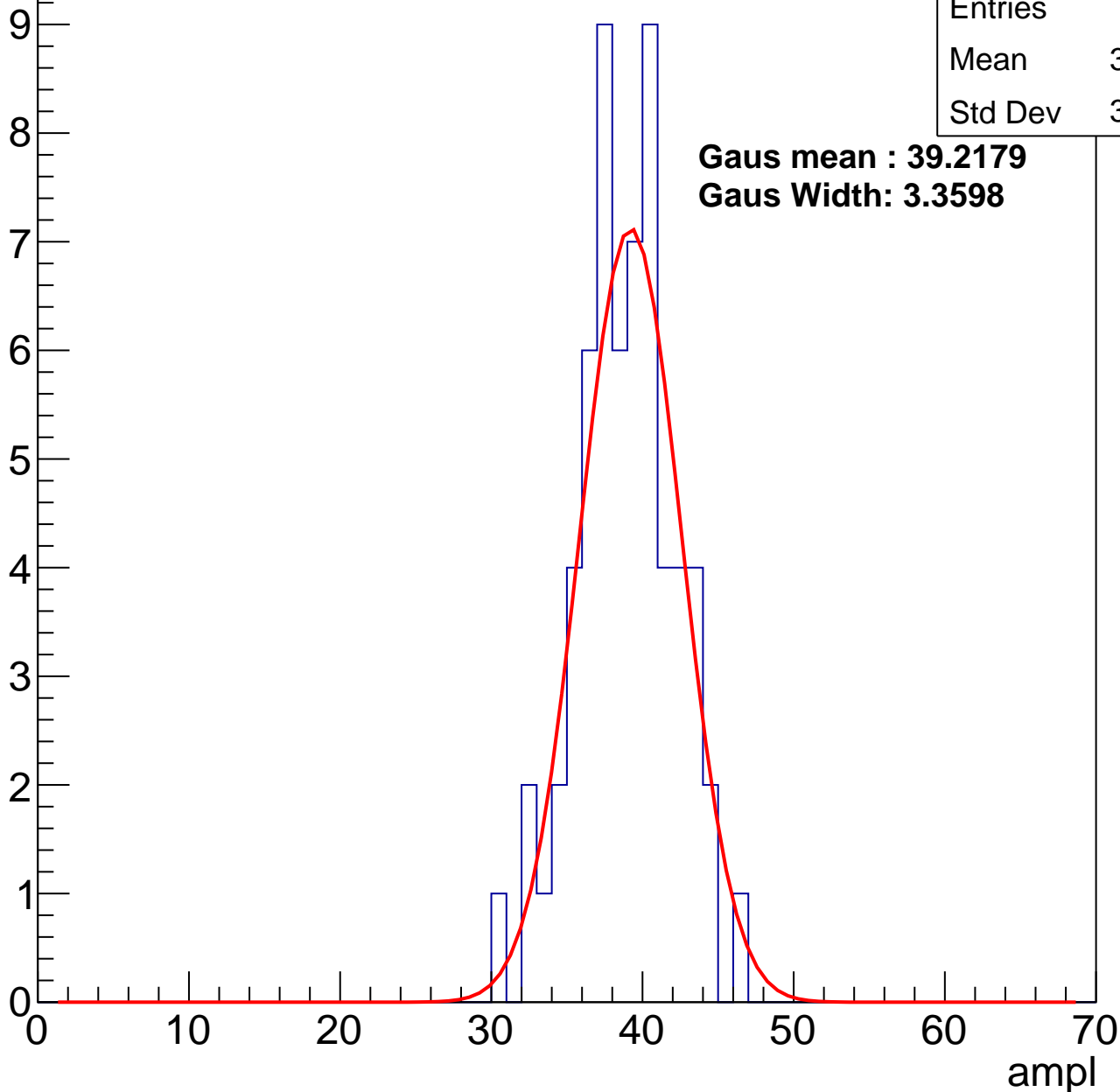
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	38.44
Std Dev	3.186

**Gaus mean : 39.2179**

**Gaus Width: 3.3598**



# B1L101S, U20-ch93, adc2

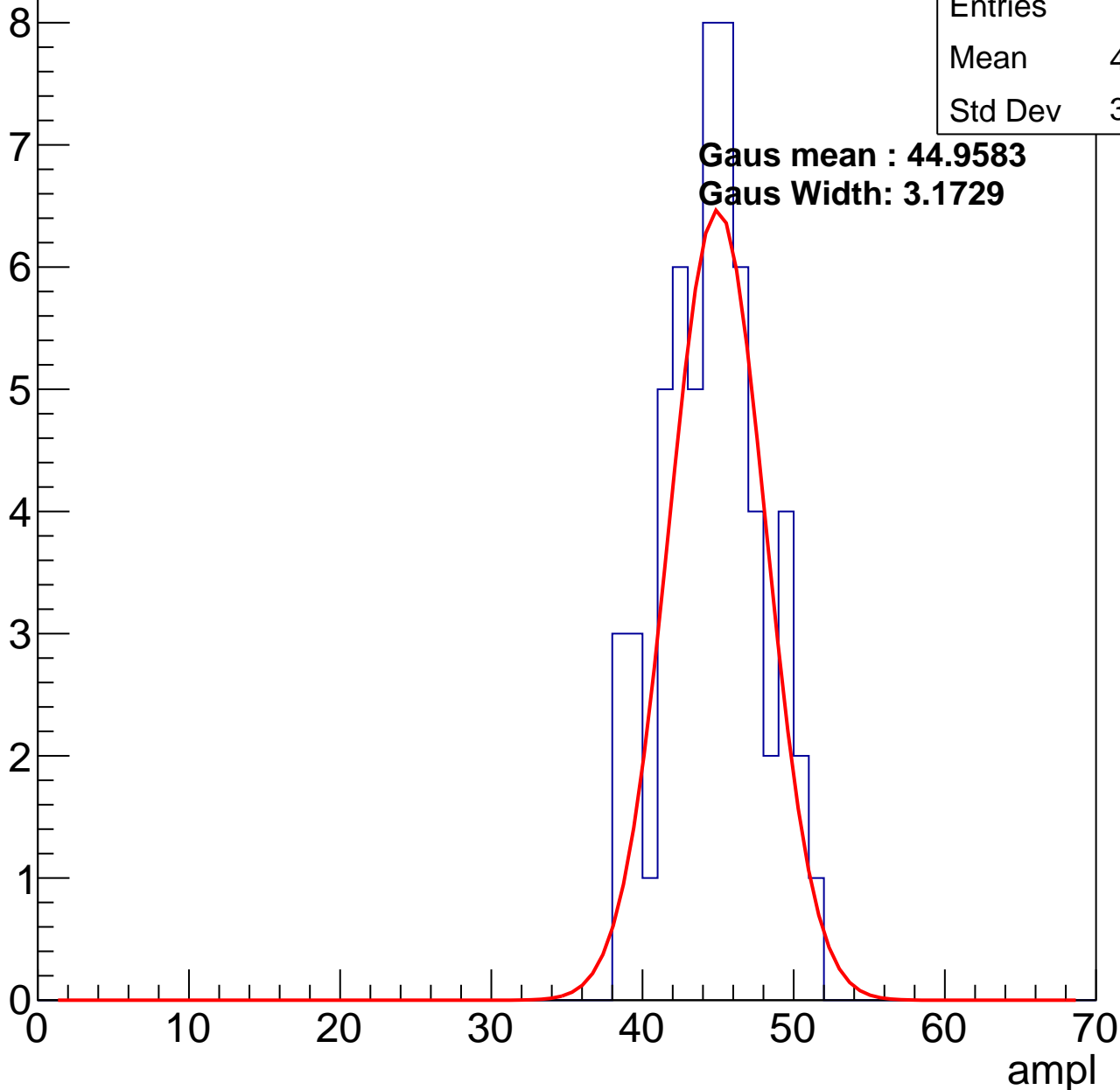
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	58
Mean	44.17
Std Dev	3.196

**Gaus mean : 44.9583**

**Gaus Width: 3.1729**

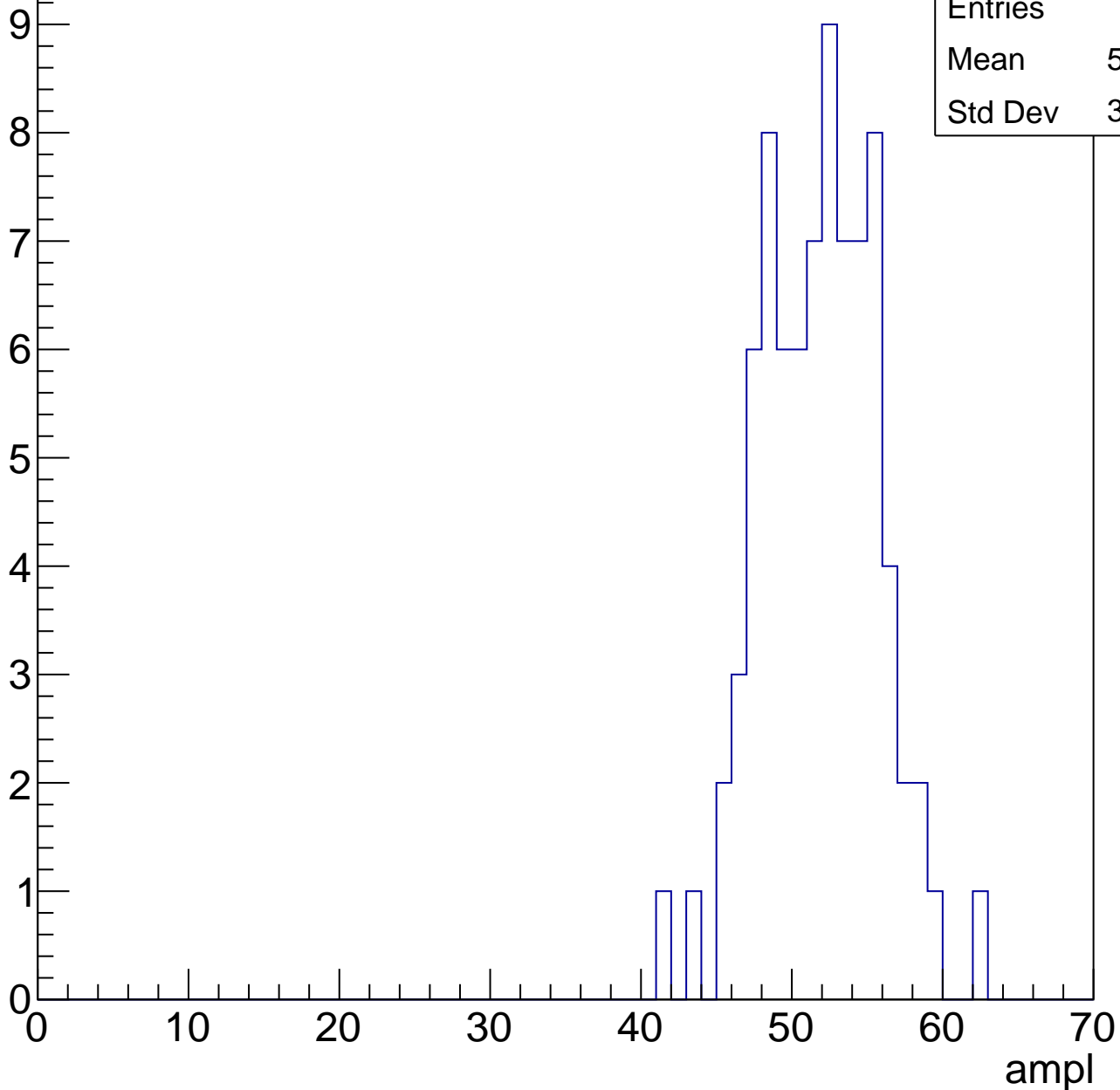


# B1L101S, U20-ch93, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

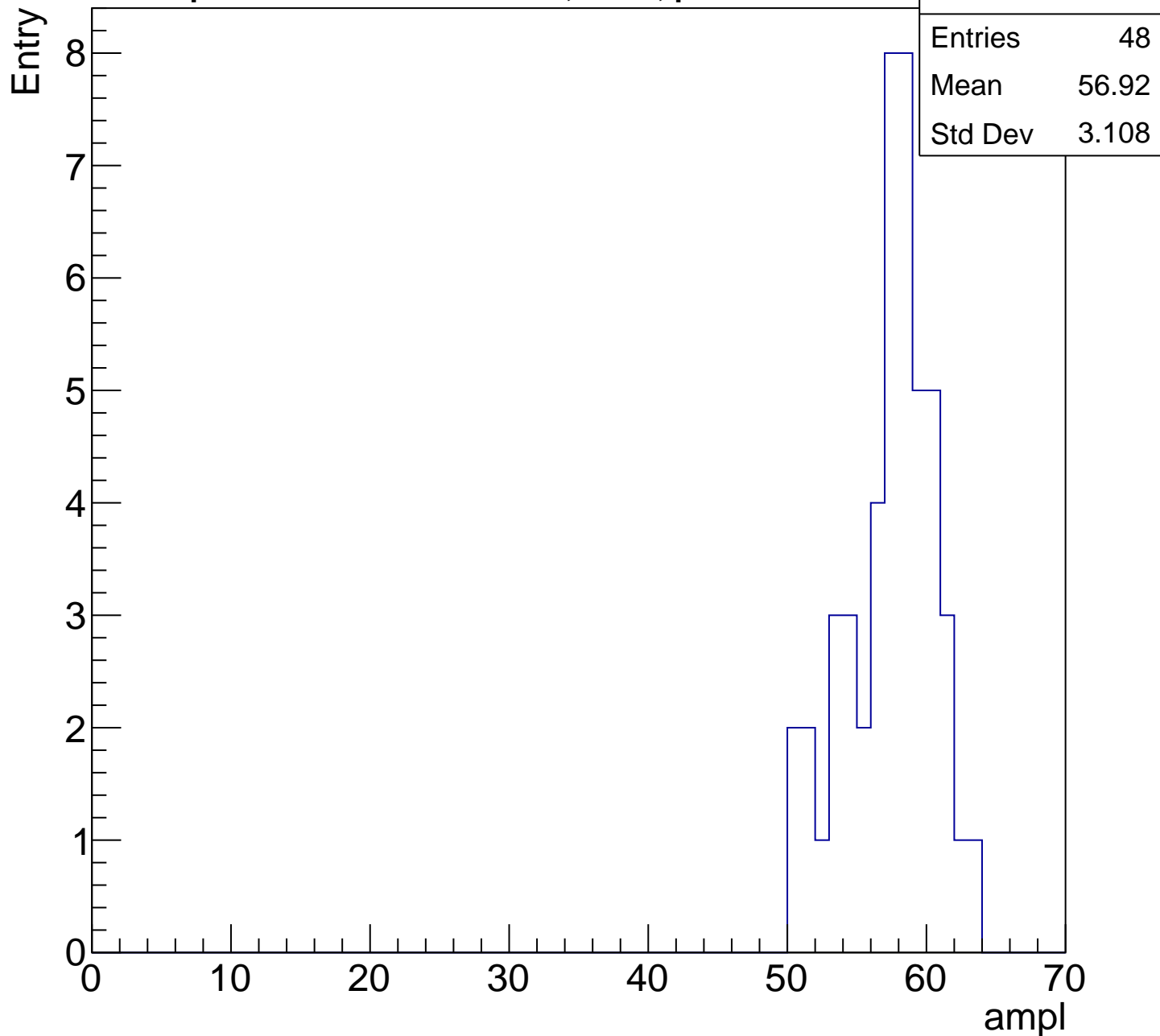
Entry

Entries	81
Mean	51.37
Std Dev	3.818



# B1L101S, U20-ch93, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

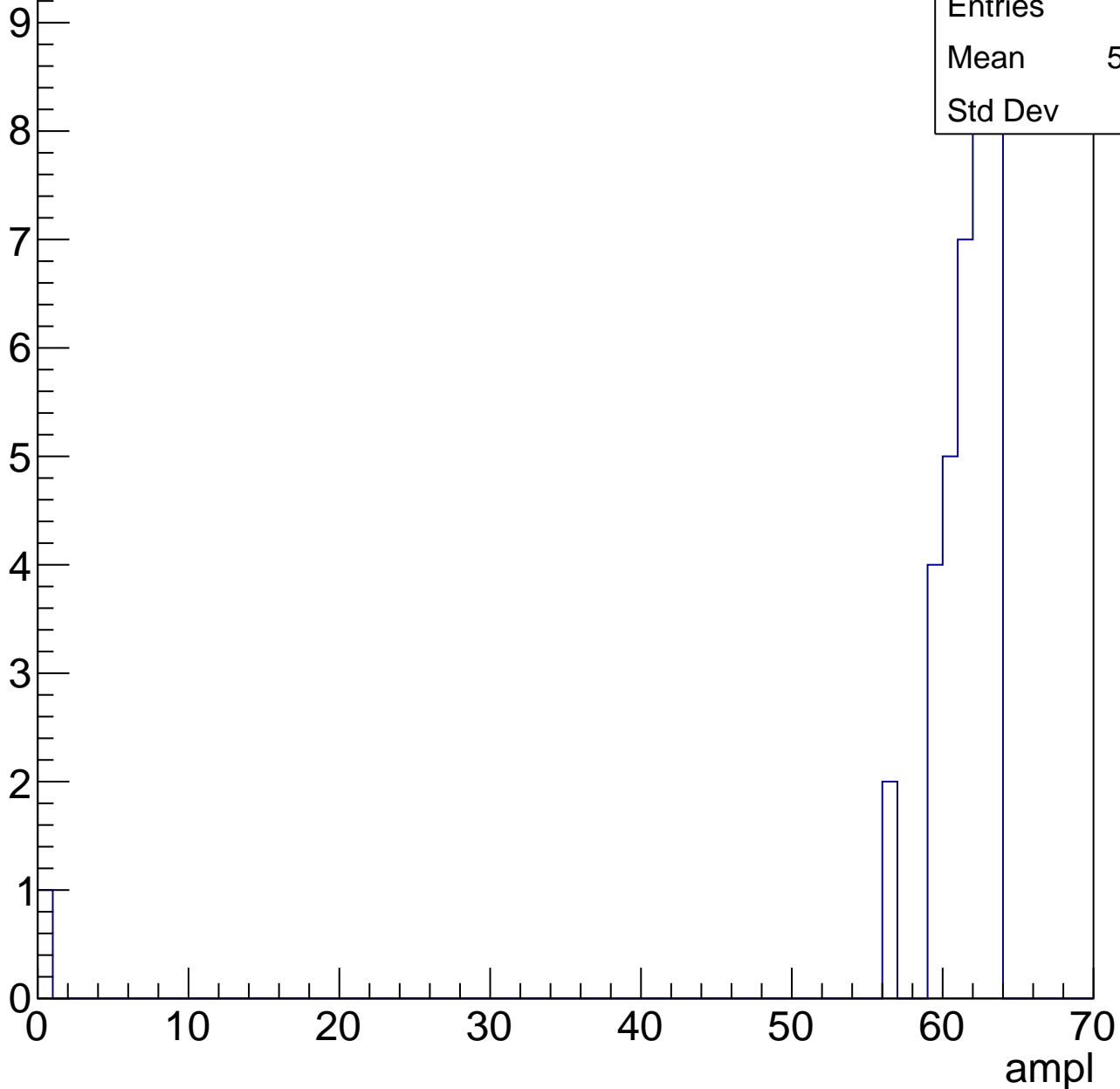


# B1L101S, U20-ch93, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	36
Mean	59.39
Std Dev	10.2



# B1L101S, U20-ch93, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0



# B1L101S, U20-ch93, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U20-ch94, adc0

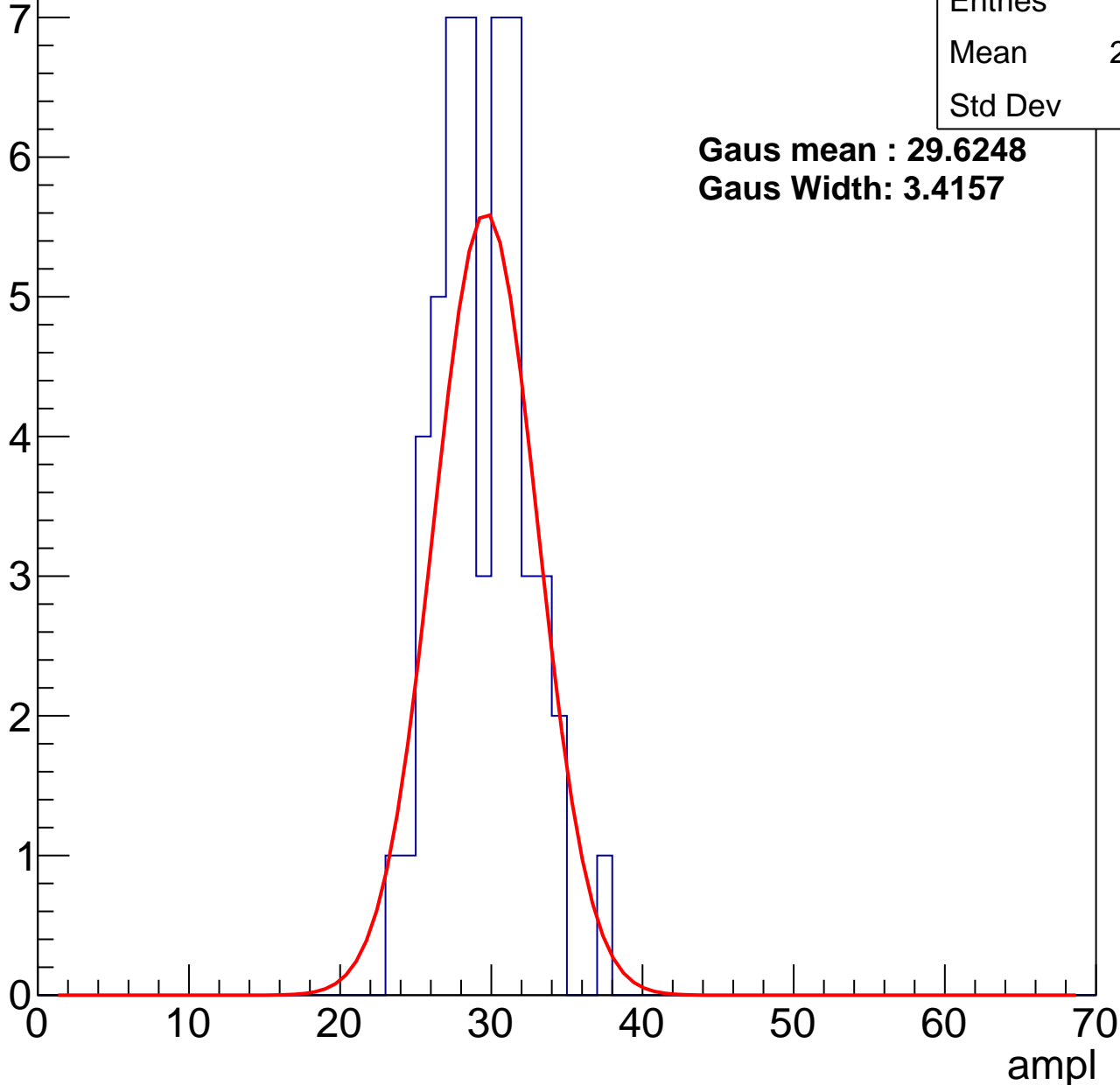
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	51
Mean	28.94
Std Dev	2.9

**Gaus mean : 29.6248**

**Gaus Width: 3.4157**



# B1L101S, U20-ch94, adc1

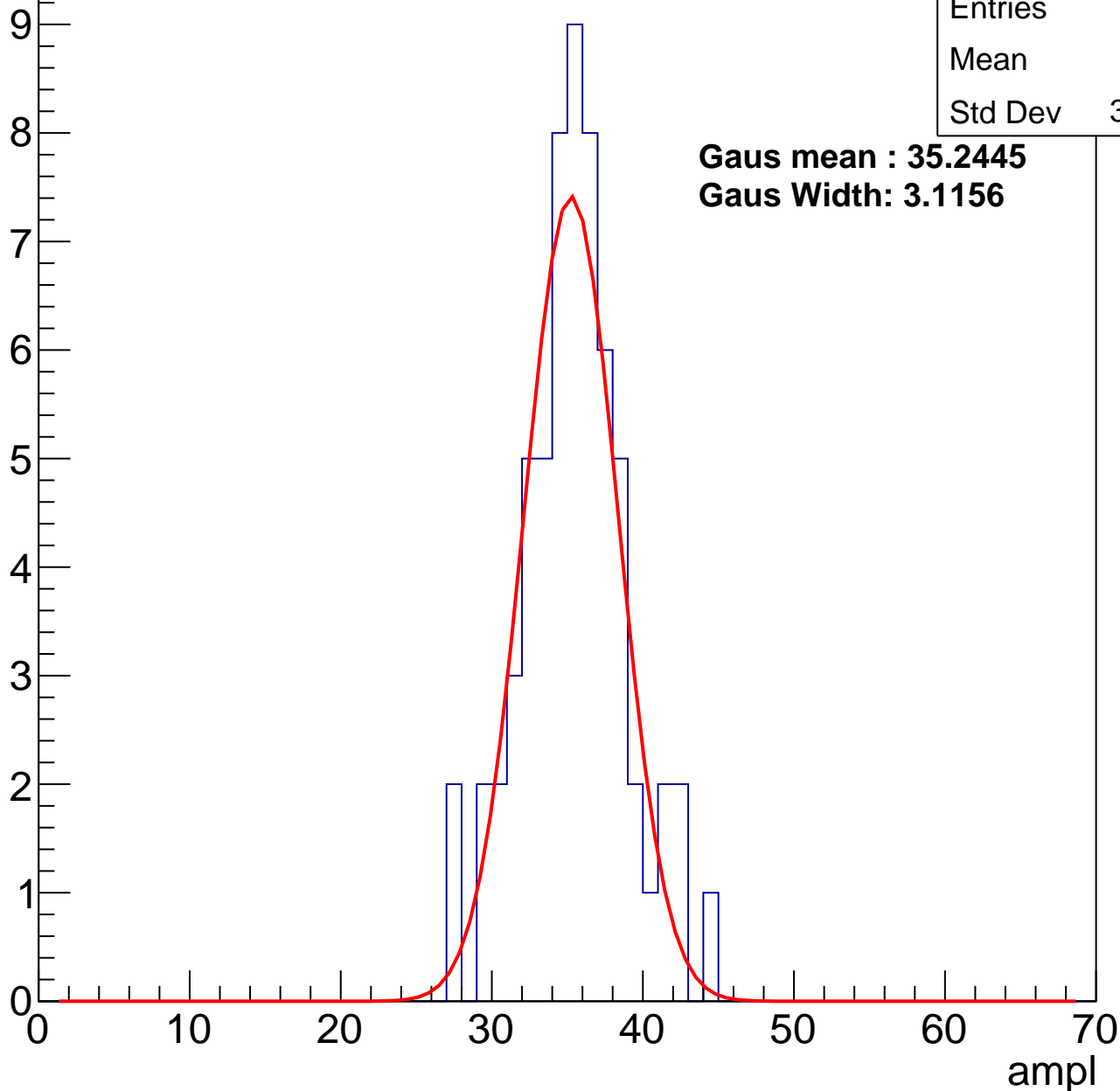
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	35
Std Dev	3.464

**Gaus mean : 35.2445**

**Gaus Width: 3.1156**



# B1L101S, U20-ch94, adc2

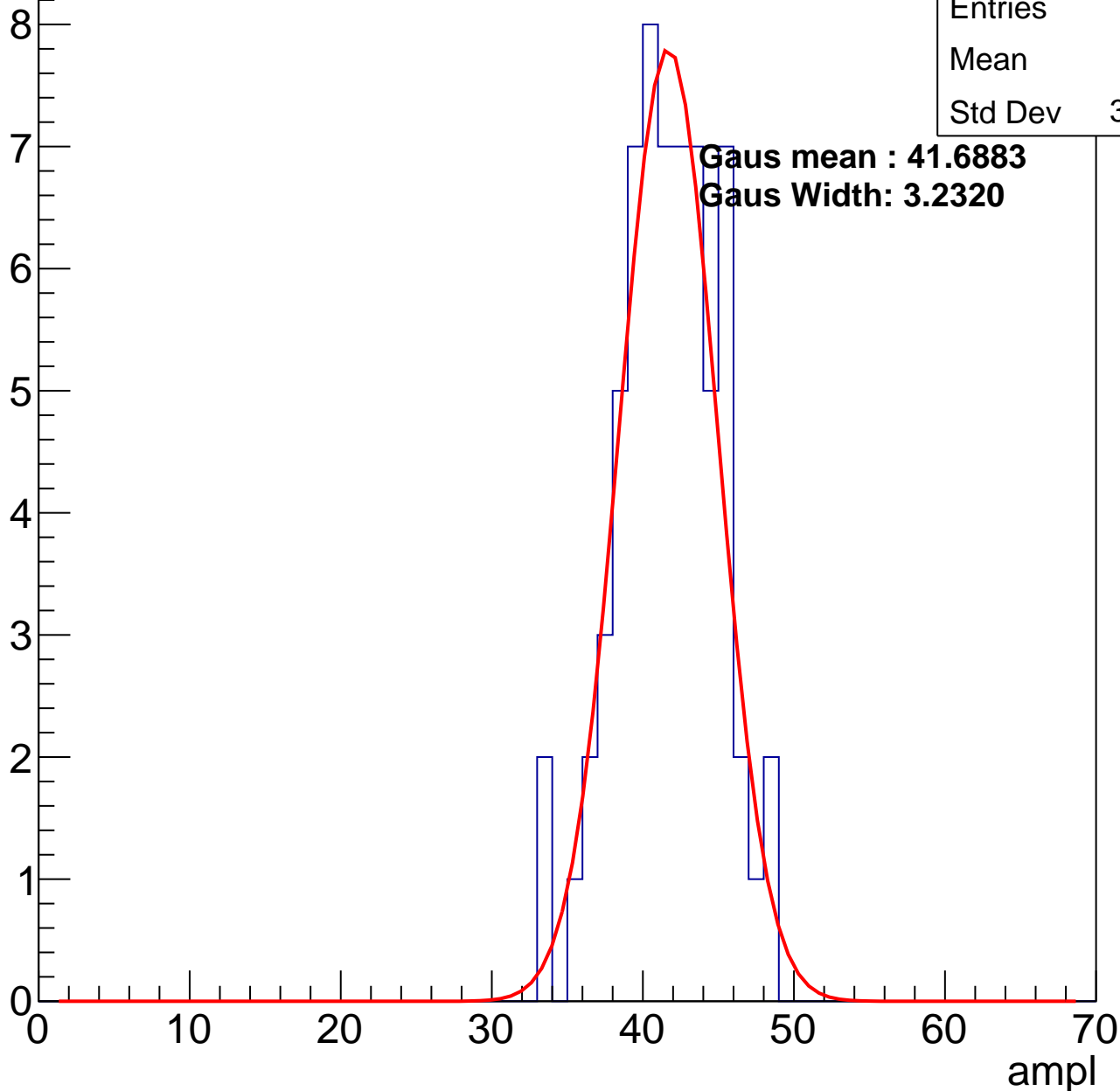
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	66
Mean	41.2
Std Dev	3.295

**Gaus mean : 41.6883**

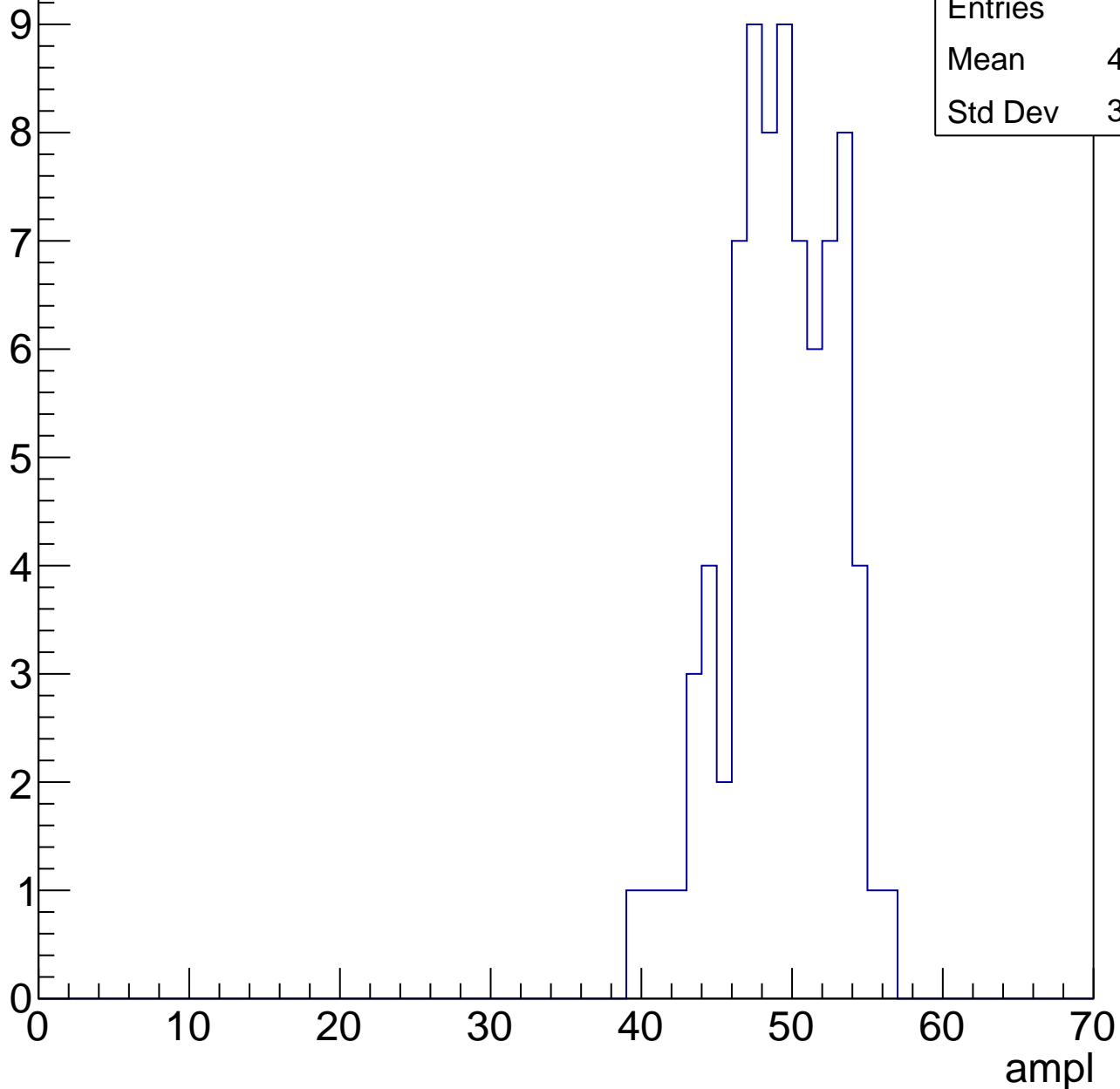
**Gaus Width: 3.2320**



# B1L101S, U20-ch94, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

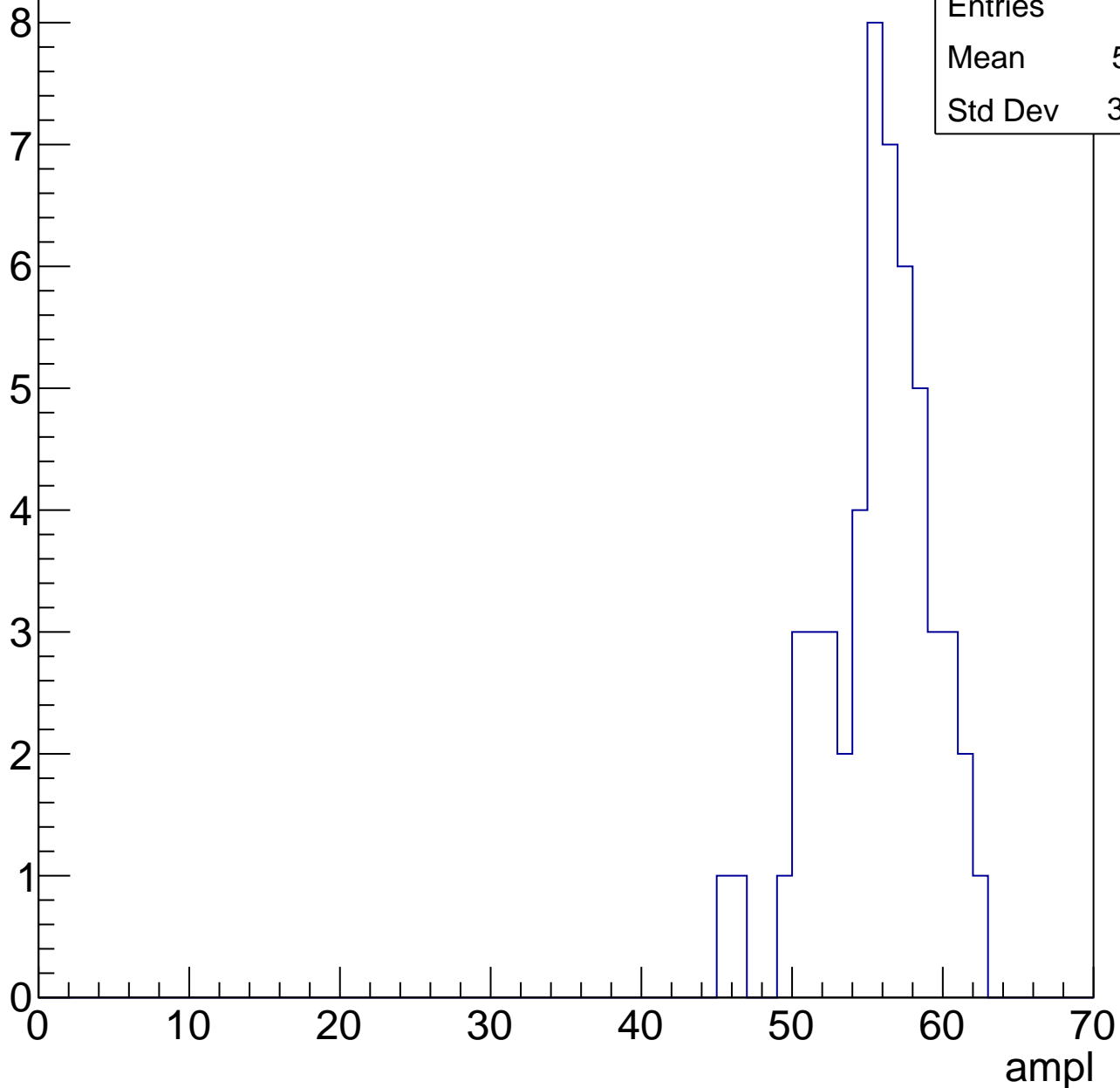
Entry



# B1L101S, U20-ch94, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



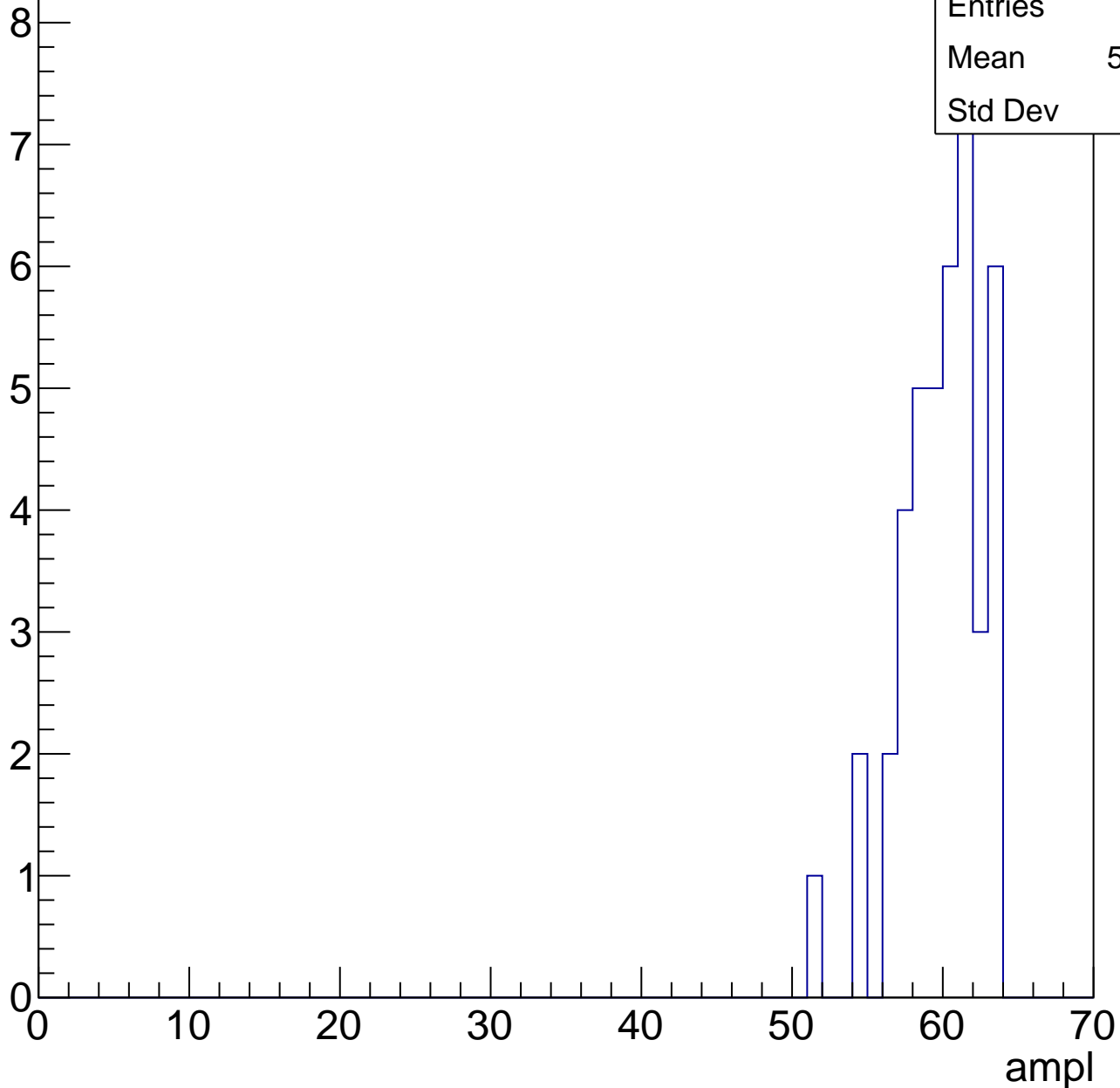
Entries	53
Mean	55.21
Std Dev	3.626

# B1L101S, U20-ch94, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	42
Mean	59.43
Std Dev	2.7

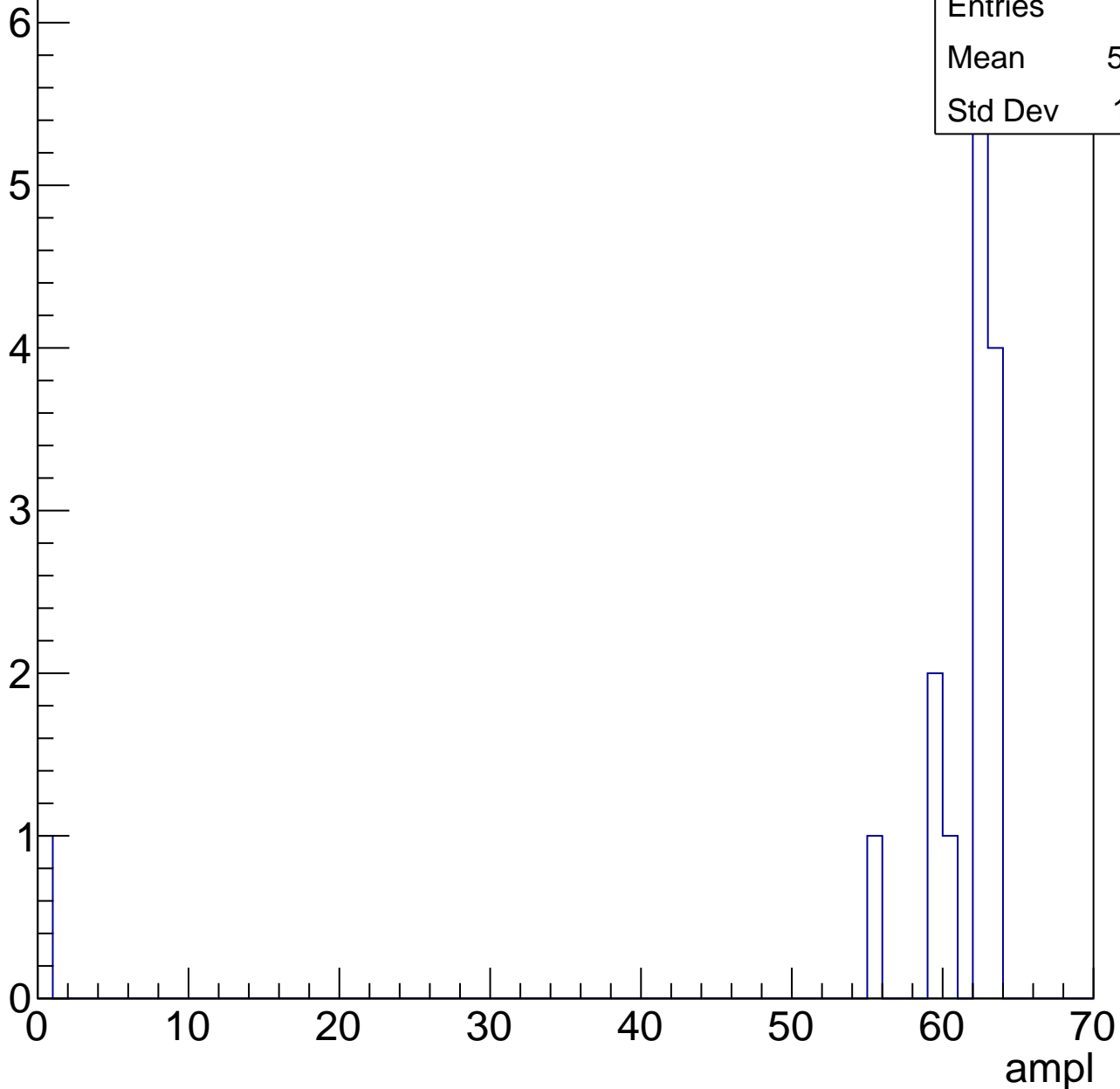


# B1L101S, U20-ch94, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	15
Mean	57.13
Std Dev	15.41

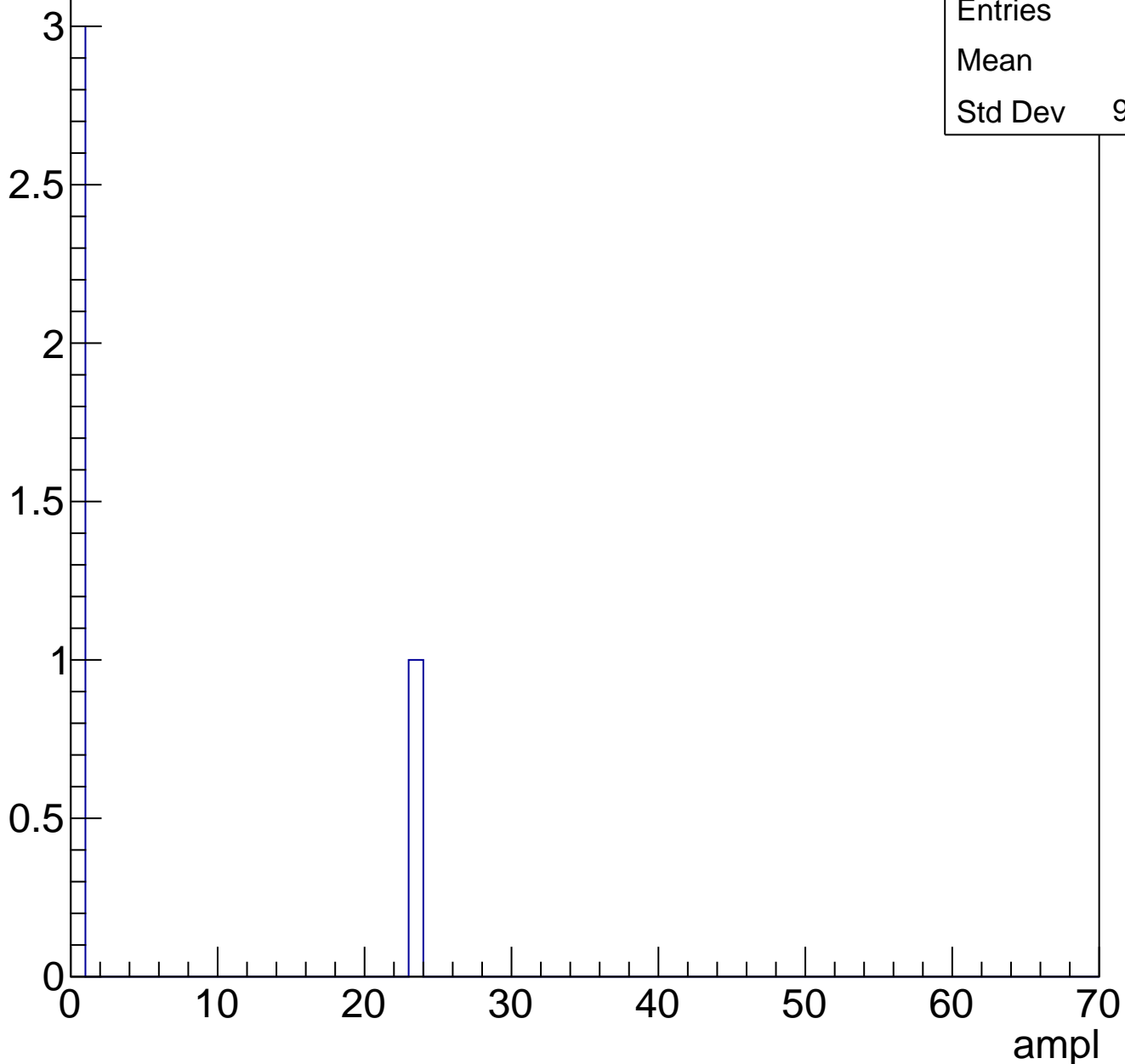




# B1L101S, U20-ch94, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U20-ch95, adc0

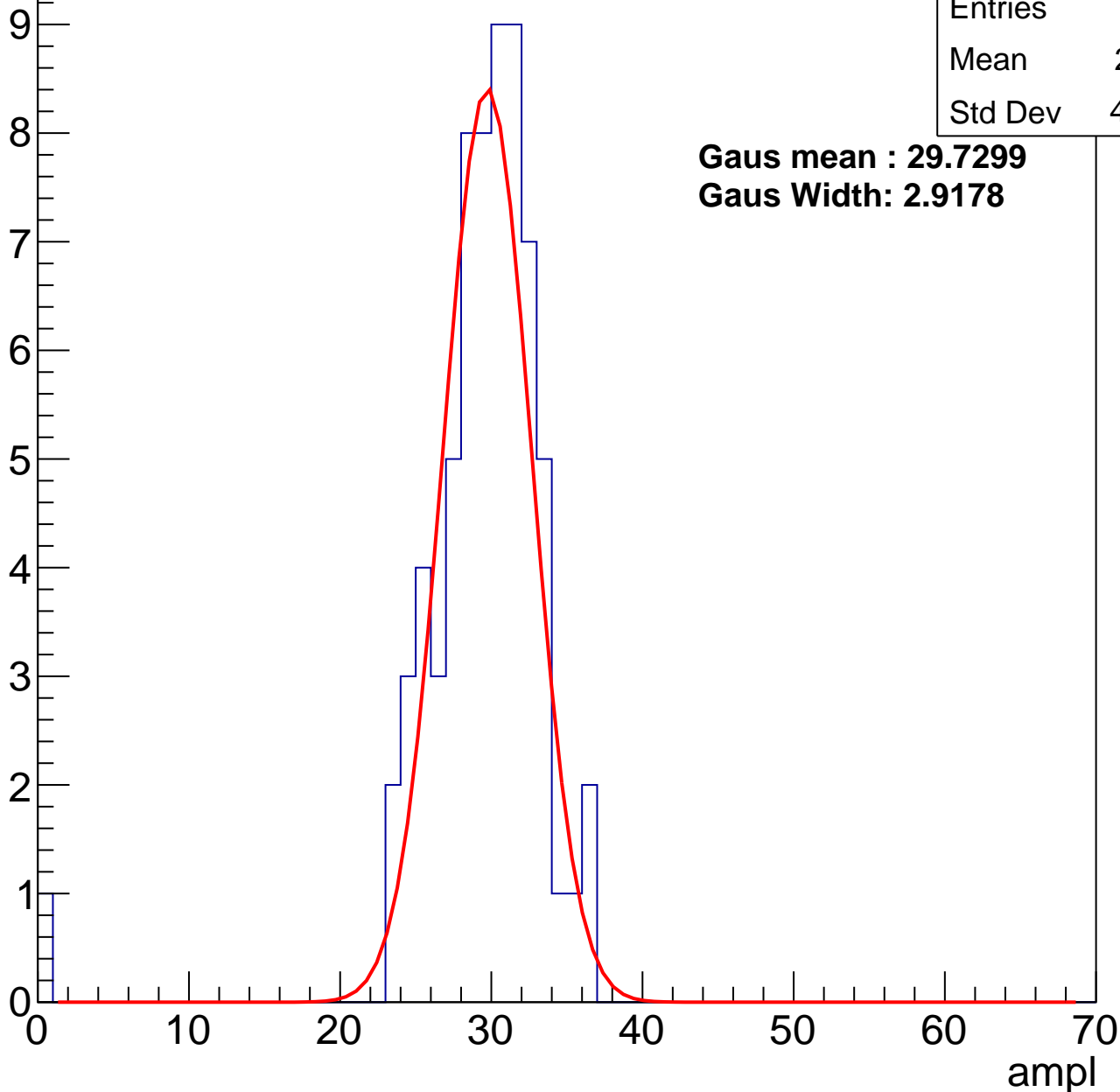
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	28.91
Std Dev	4.623

**Gaus mean : 29.7299**

**Gaus Width: 2.9178**



# B1L101S, U20-ch95, adc1

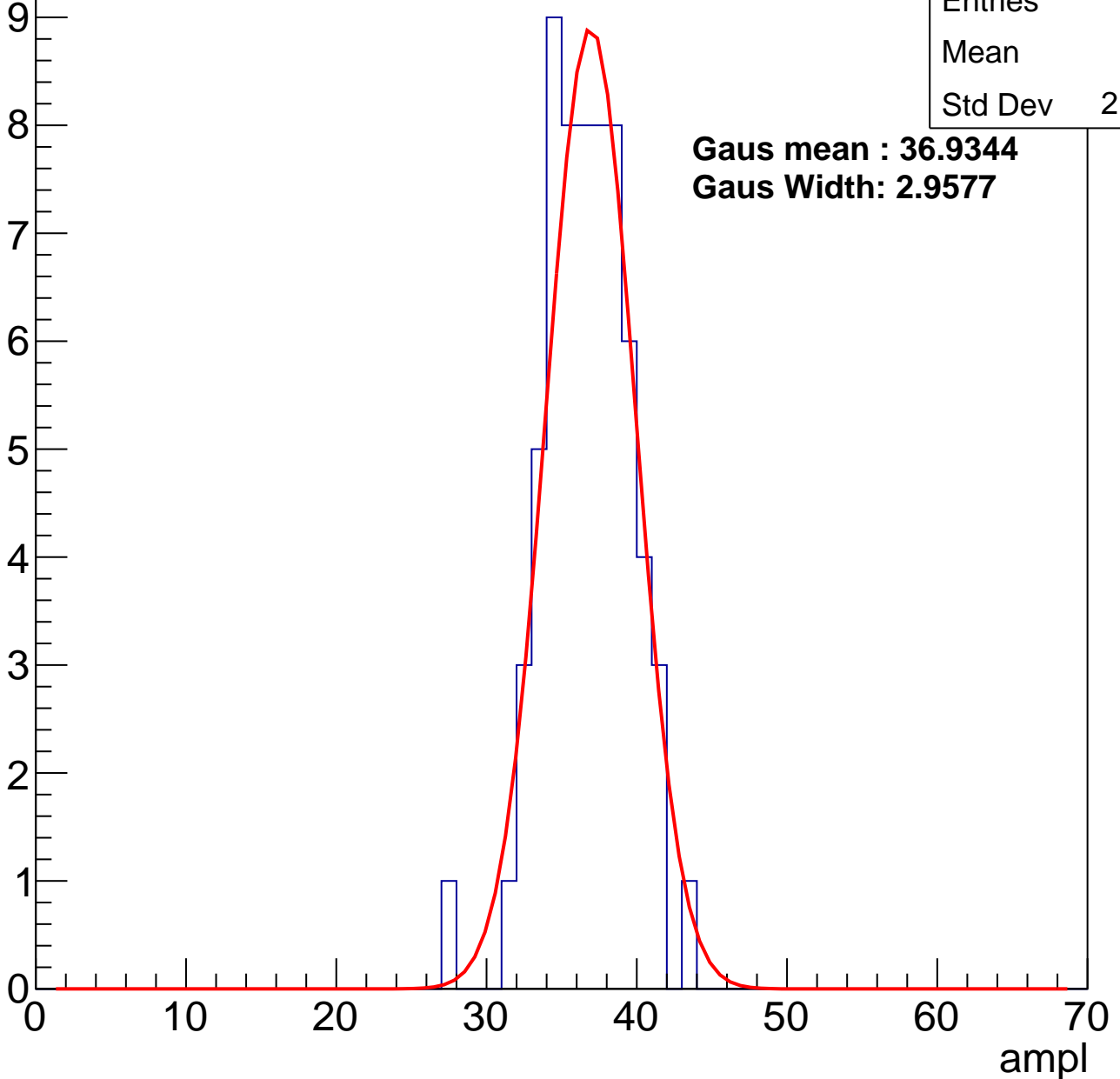
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	36.2
Std Dev	2.835

**Gaus mean : 36.9344**

**Gaus Width: 2.9577**



# B1L101S, U20-ch95, adc2

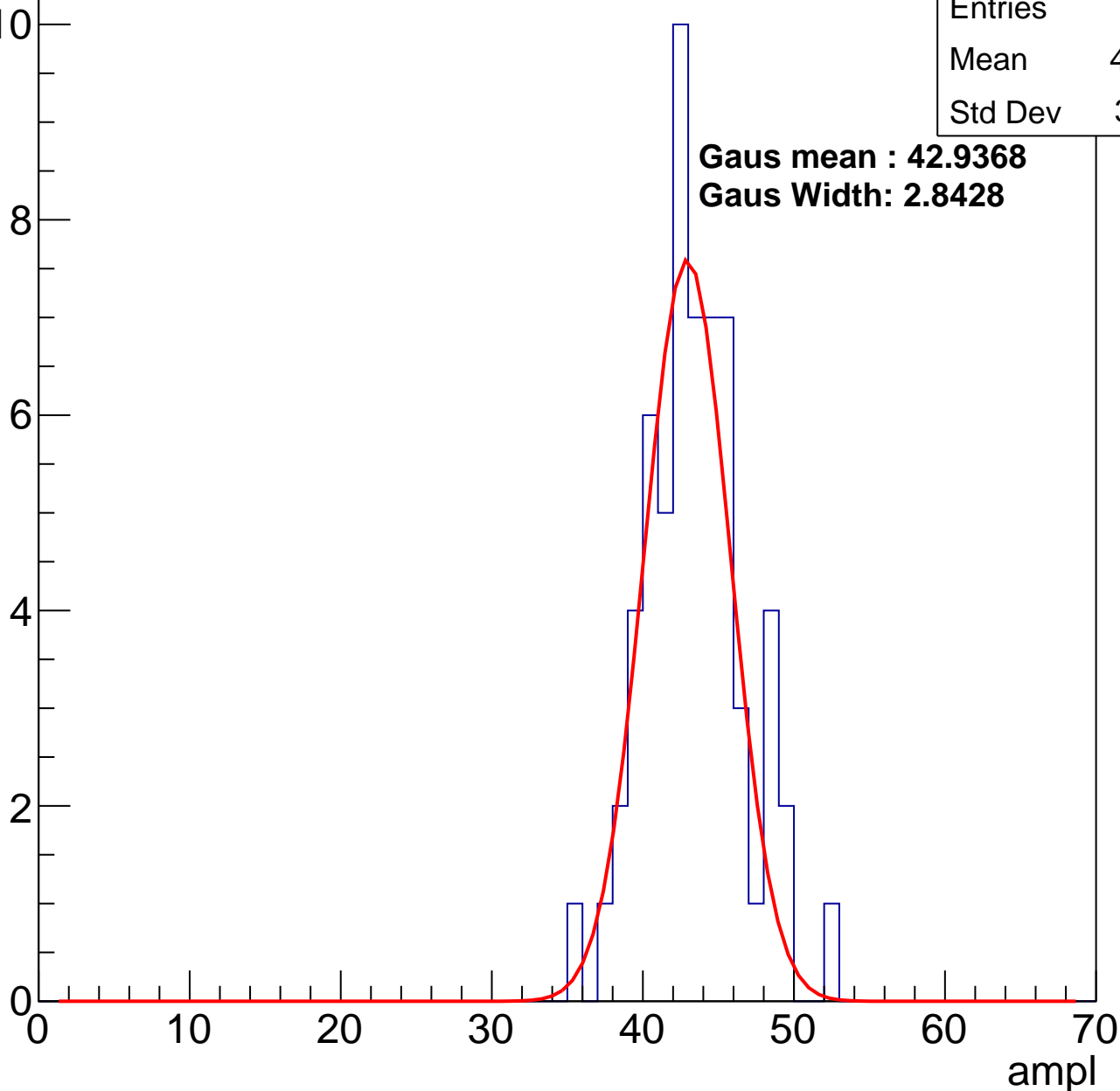
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	42.95
Std Dev	3.211

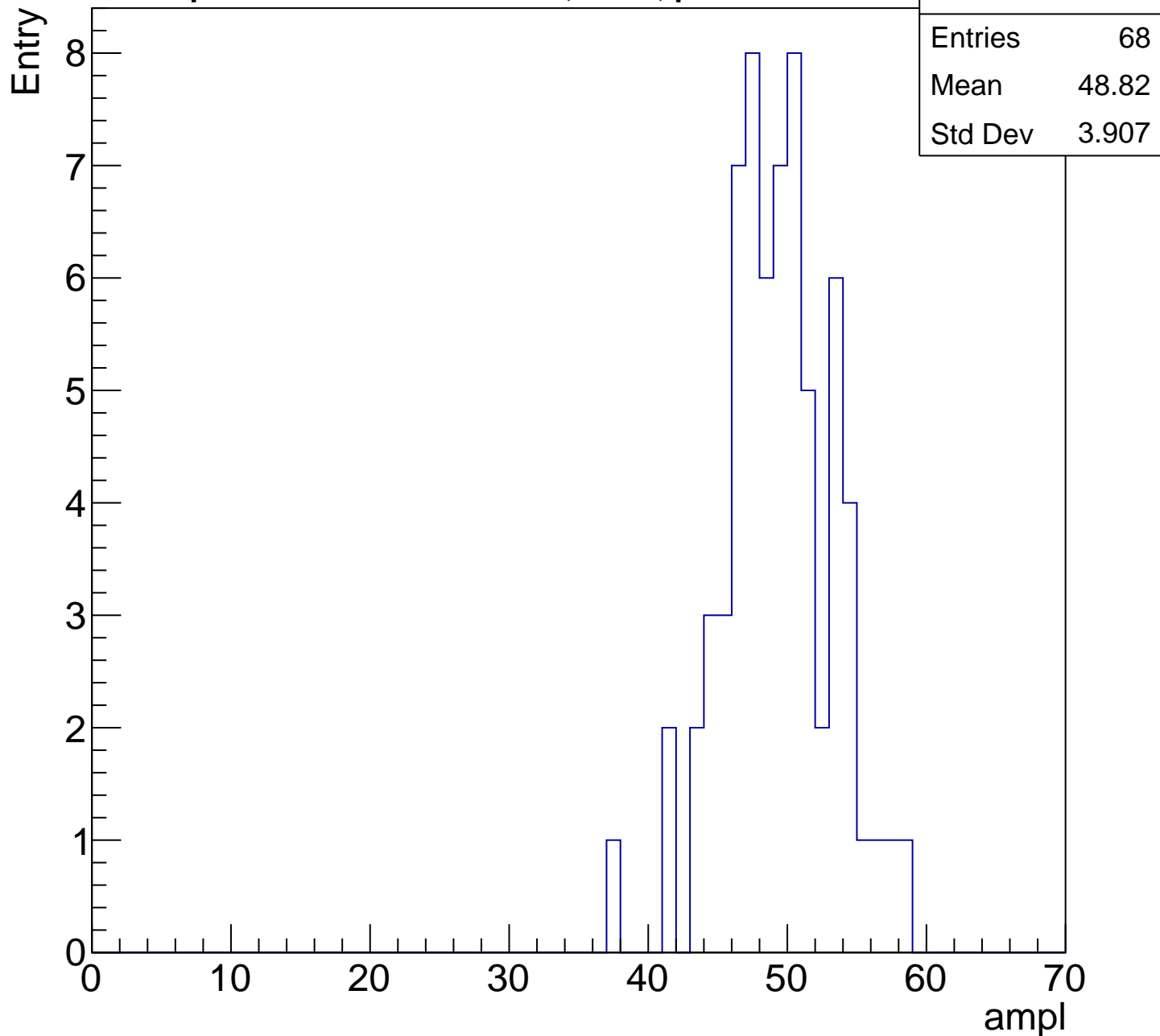
**Gaus mean : 42.9368**

**Gaus Width: 2.8428**



# B1L101S, U20-ch95, adc3

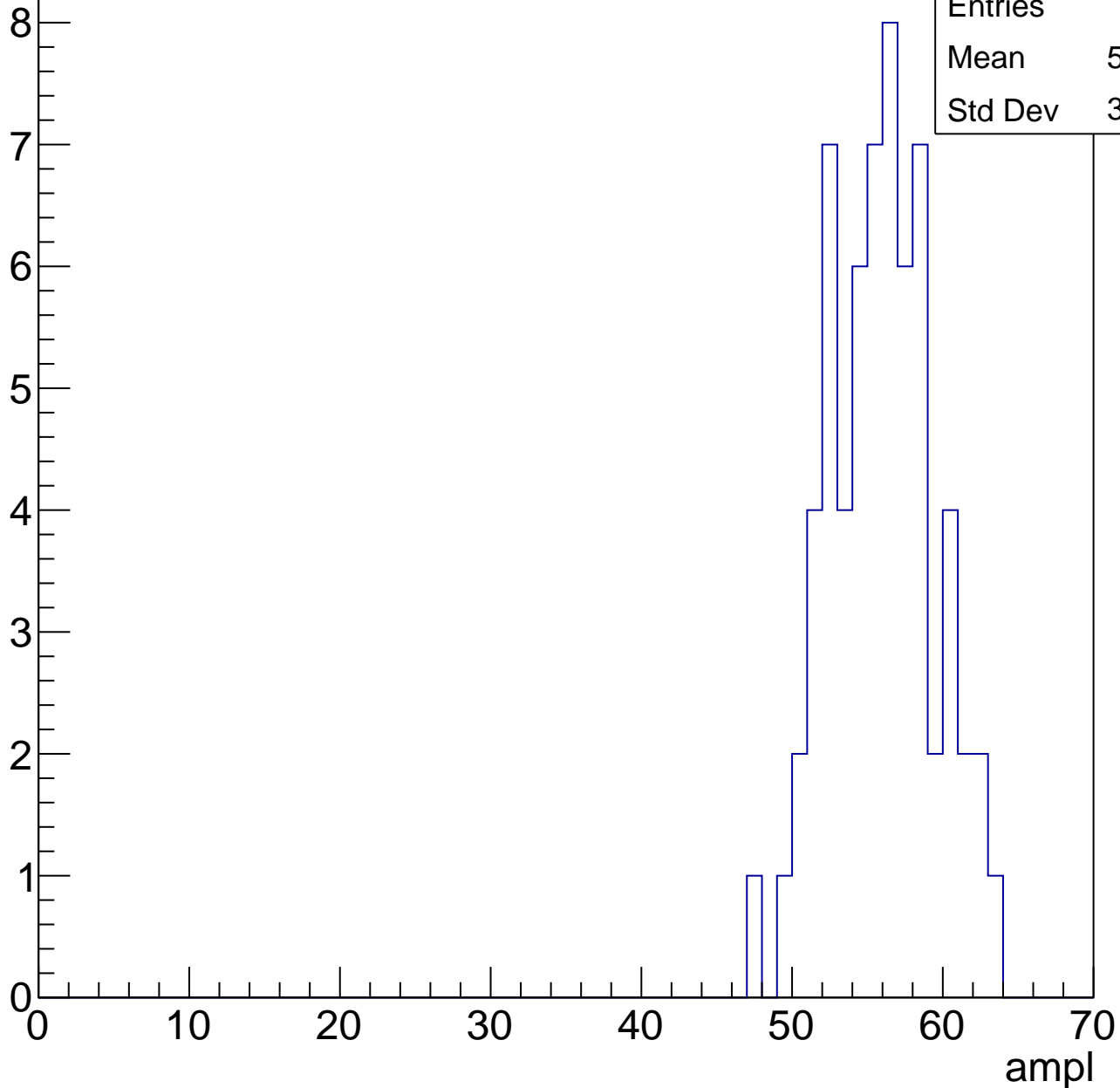
calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U20-ch95, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

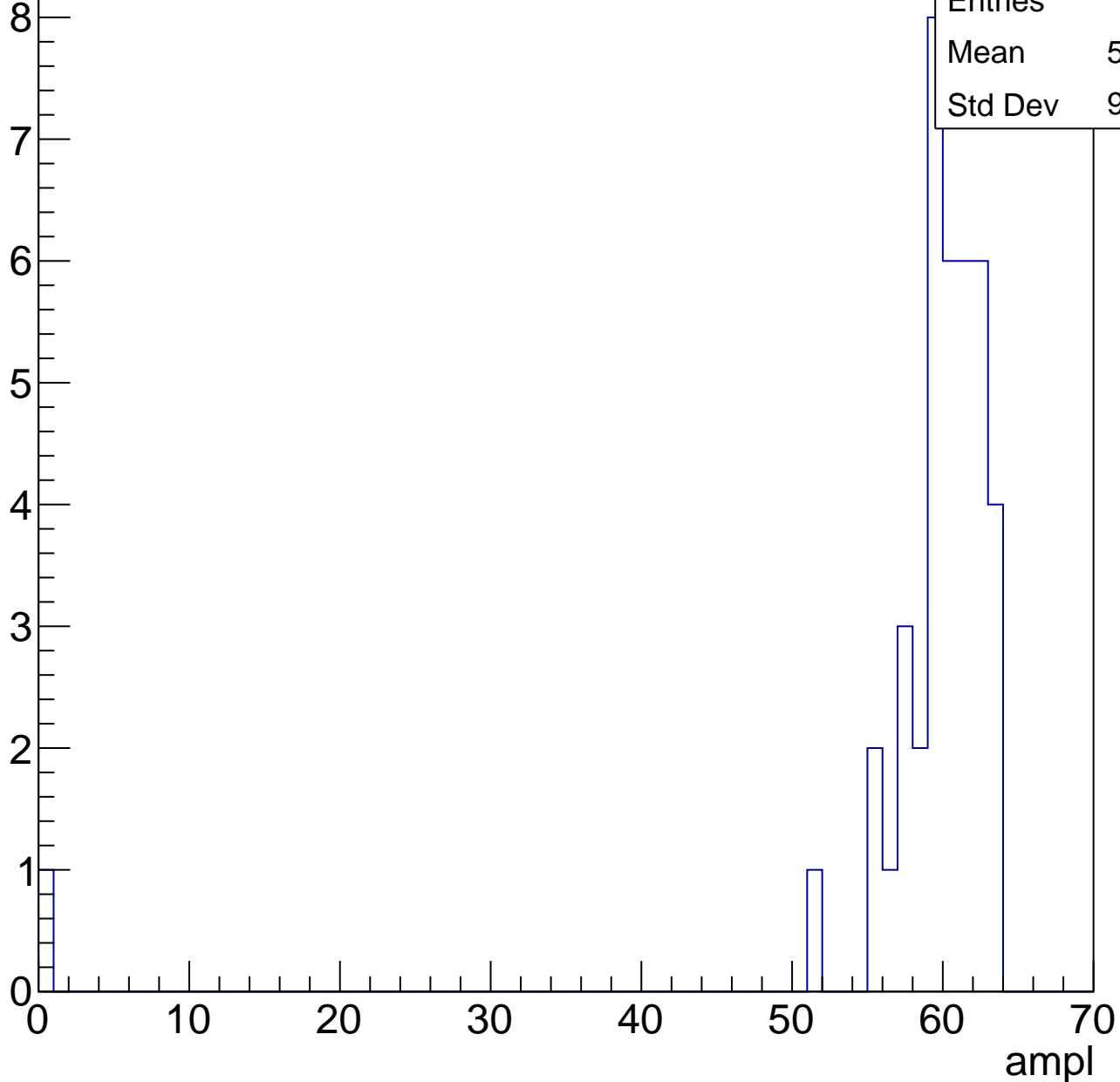


Entries	64
Mean	55.44
Std Dev	3.418

# B1L101S, U20-ch95, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

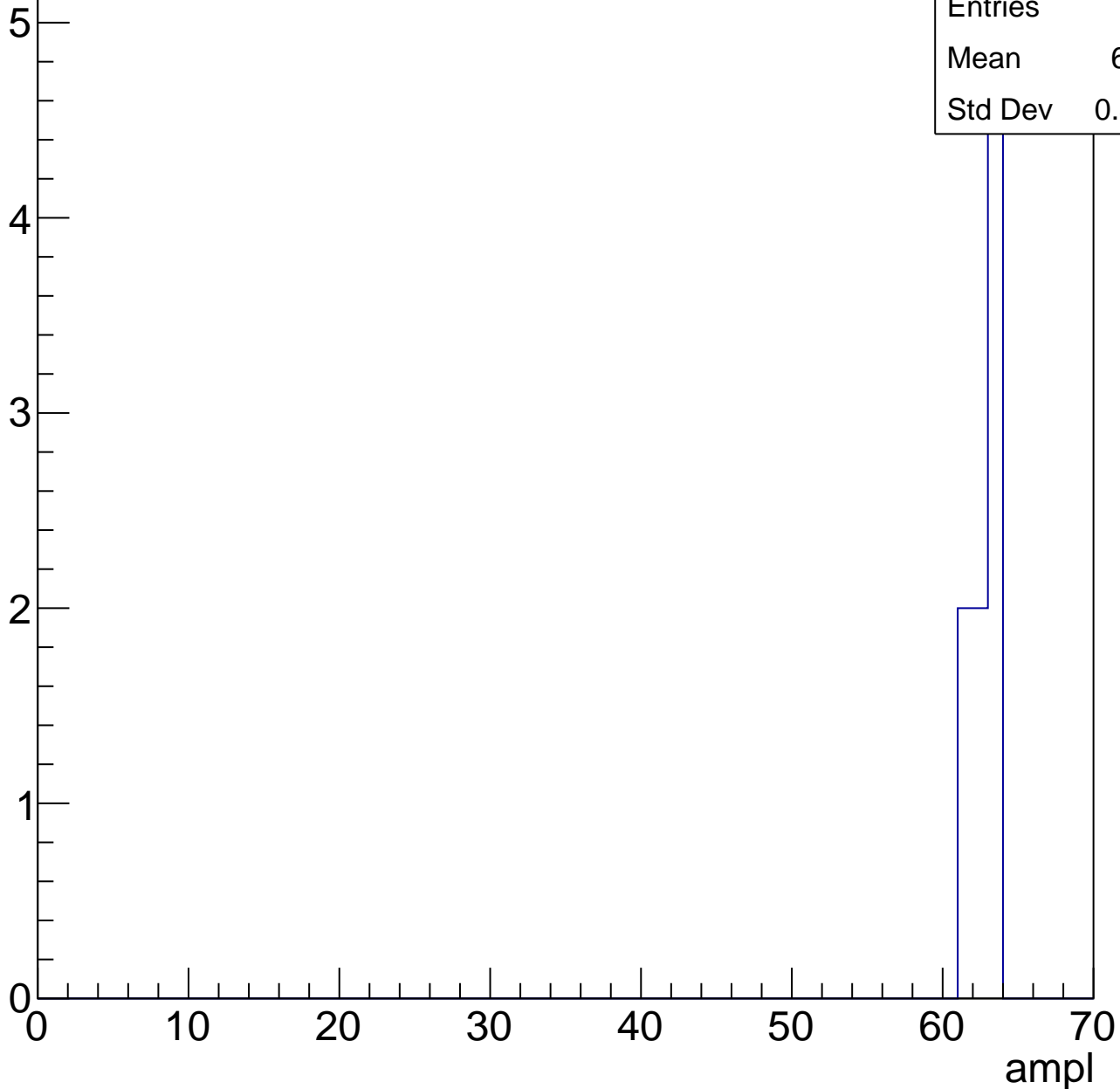


# B1L101S, U20-ch95, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	9
Mean	62.33
Std Dev	0.8165





# B1L101S, U20-ch95, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U20-ch96, adc0

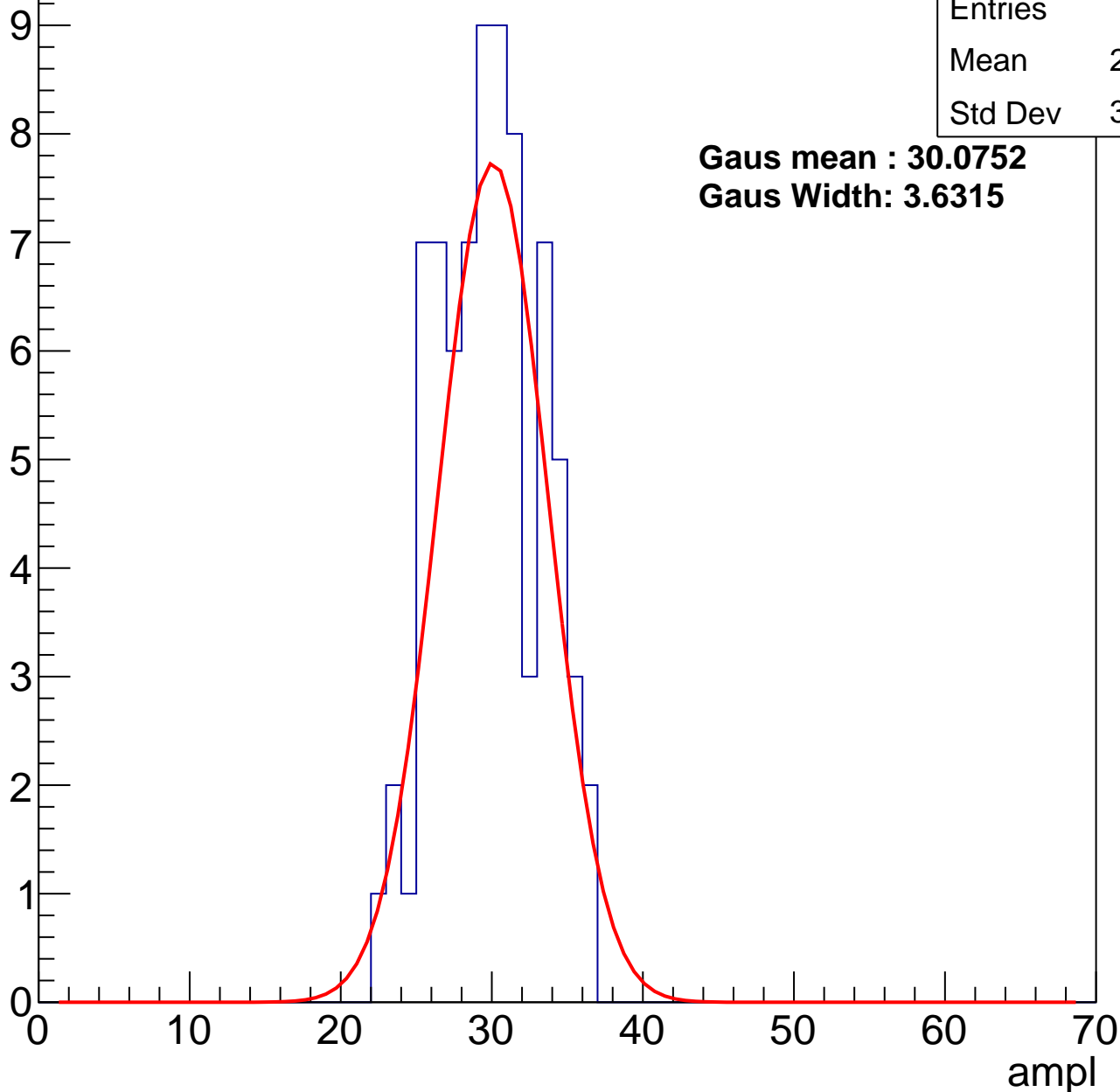
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	77
Mean	29.35
Std Dev	3.329

**Gaus mean : 30.0752**

**Gaus Width: 3.6315**



# B1L101S, U20-ch96, adc1

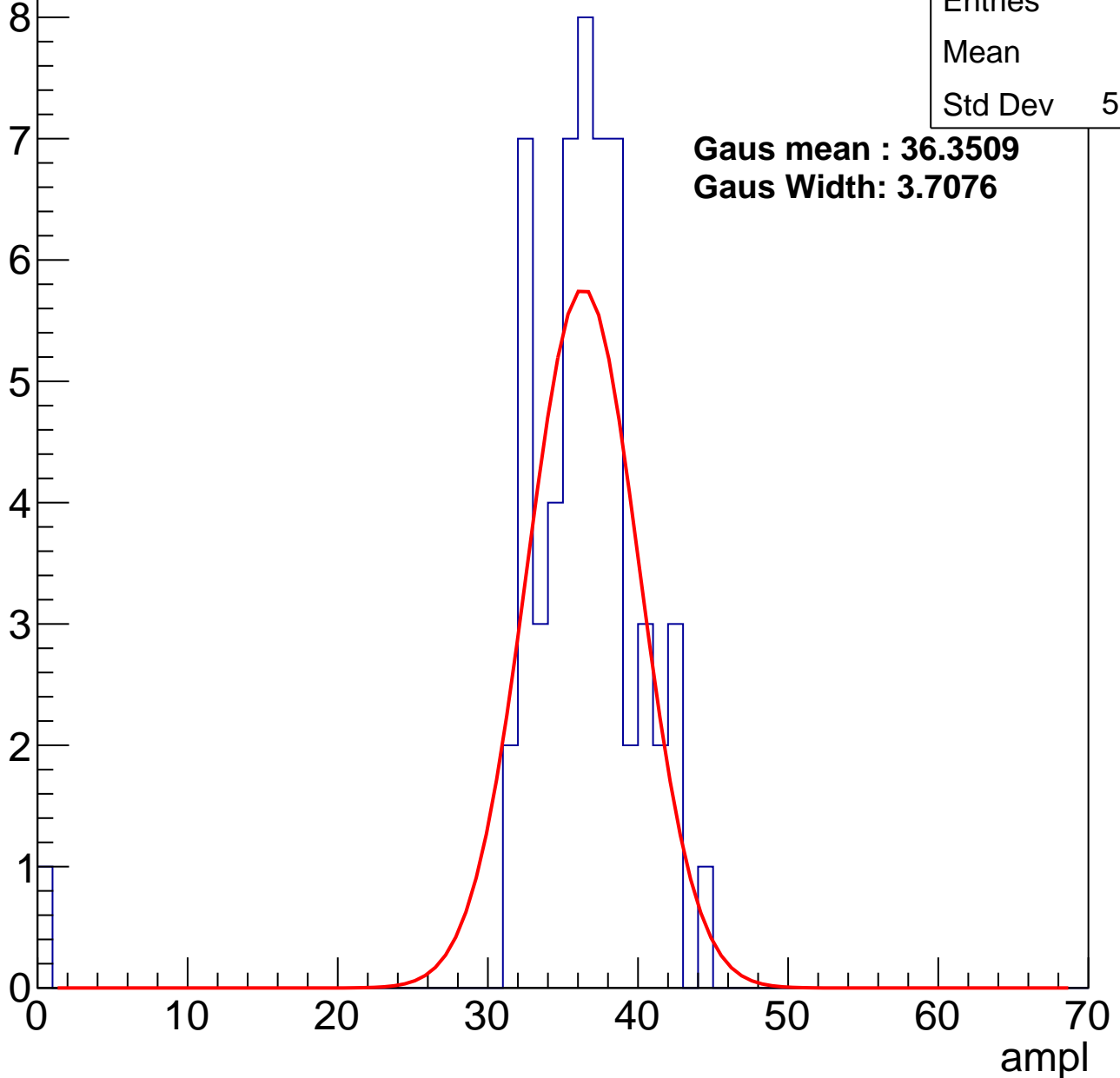
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	57
Mean	35.6
Std Dev	5.653

**Gaus mean : 36.3509**

**Gaus Width: 3.7076**



# B1L101S, U20-ch96, adc2

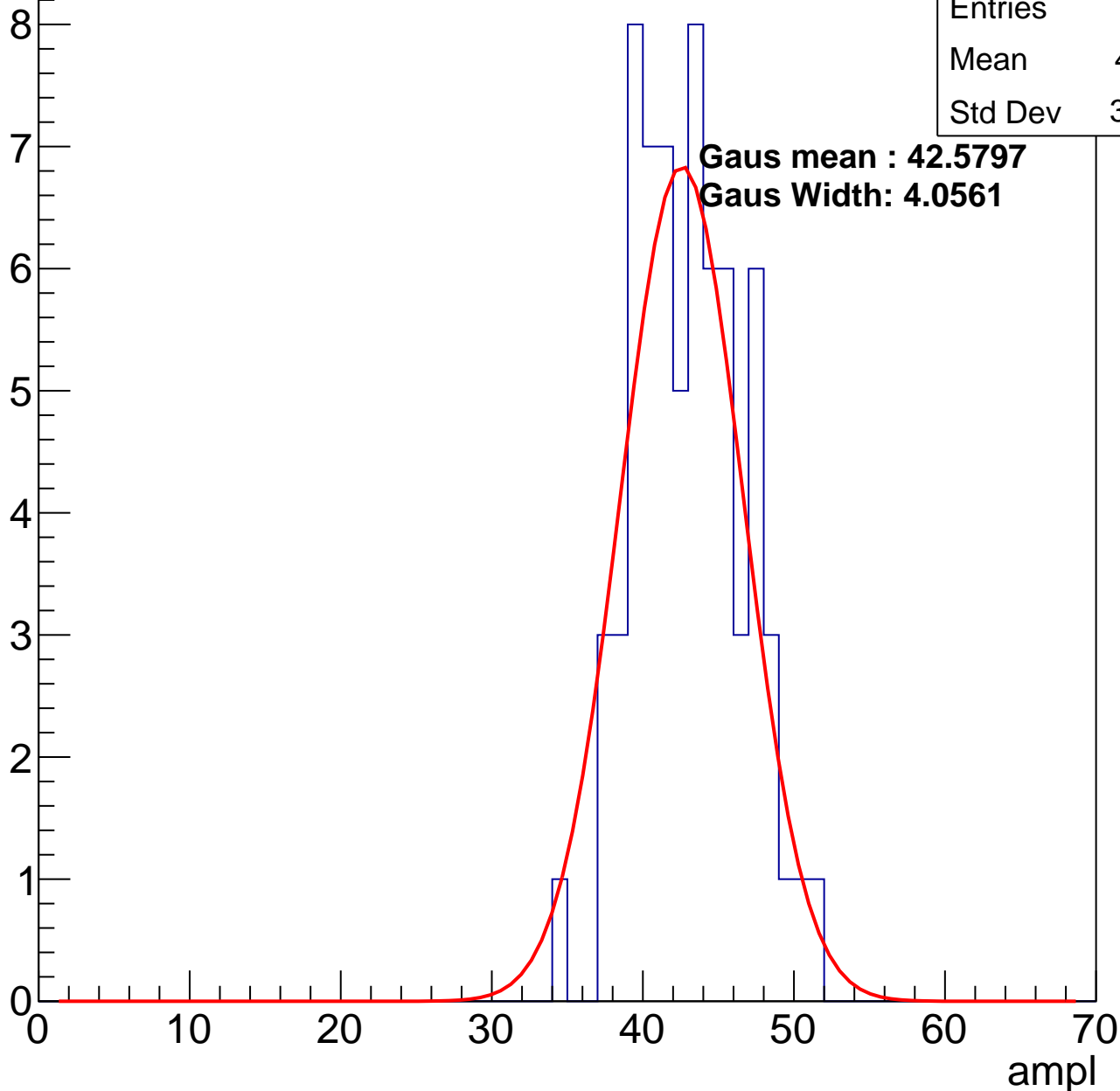
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	42.61
Std Dev	3.519

**Gaus mean : 42.5797**

**Gaus Width: 4.0561**

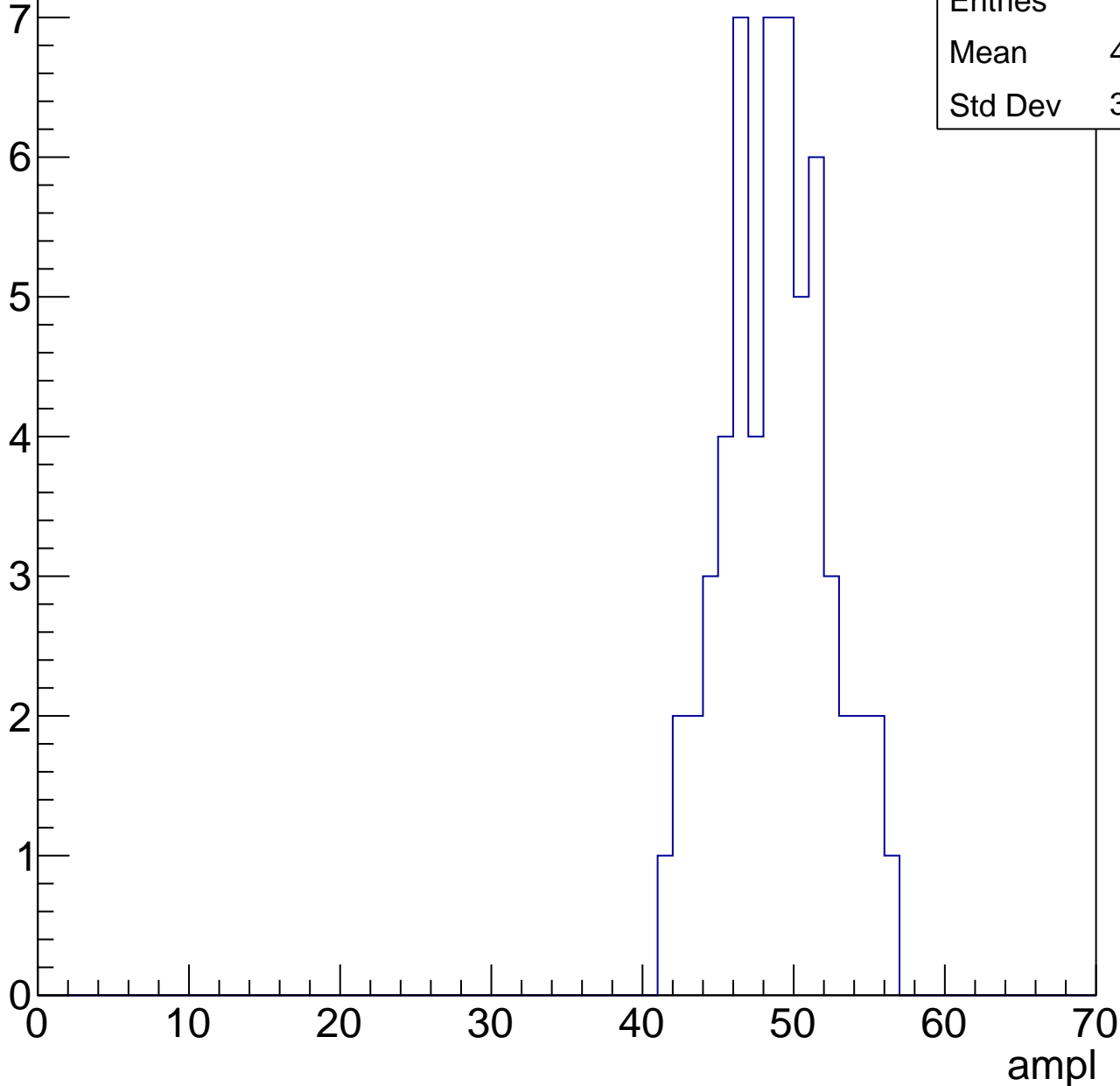


# B1L101S, U20-ch96, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	58
Mean	48.34
Std Dev	3.457

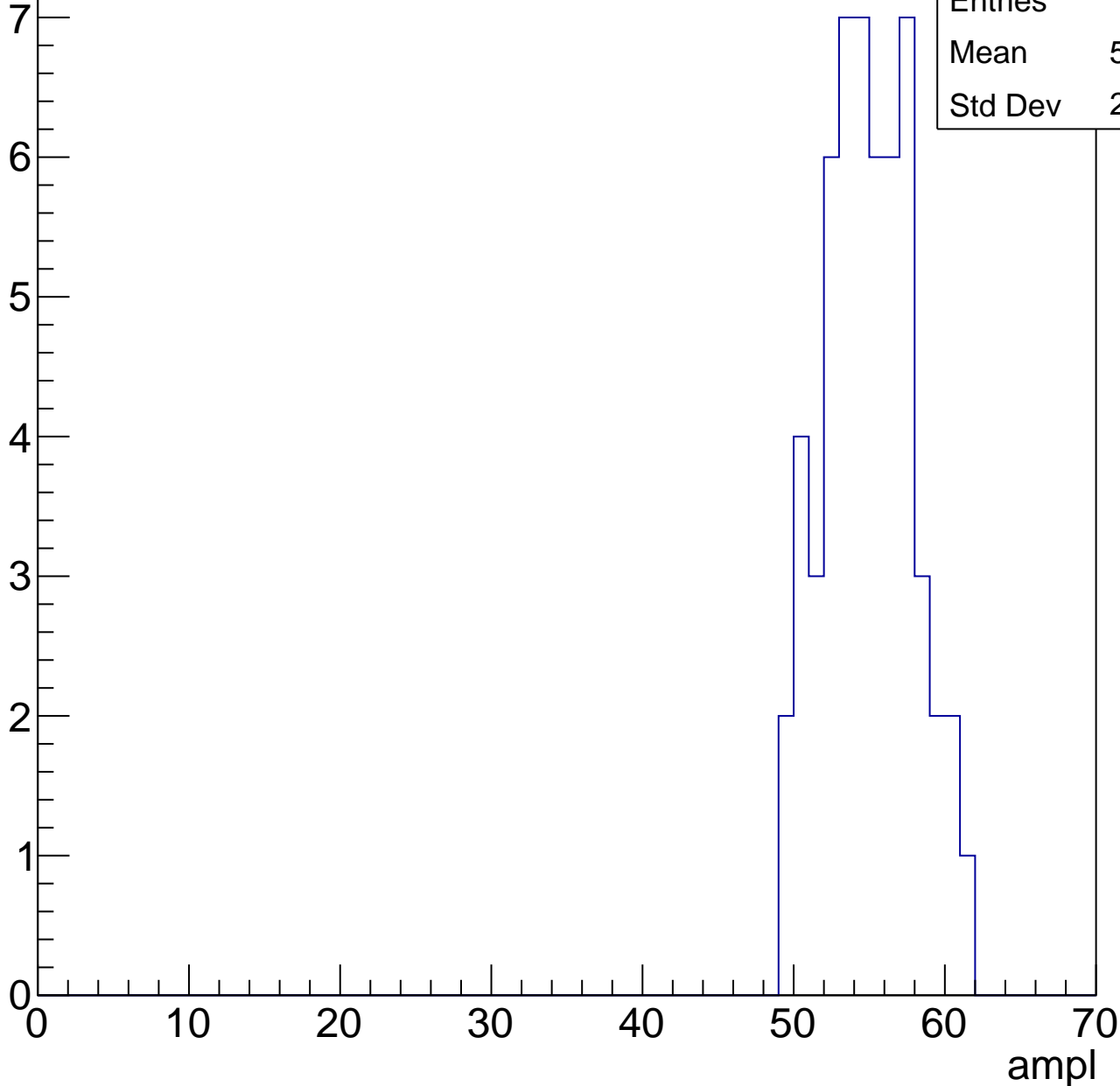


# B1L101S, U20-ch96, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	56
Mean	54.46
Std Dev	2.903



# B1L101S, U20-ch96, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

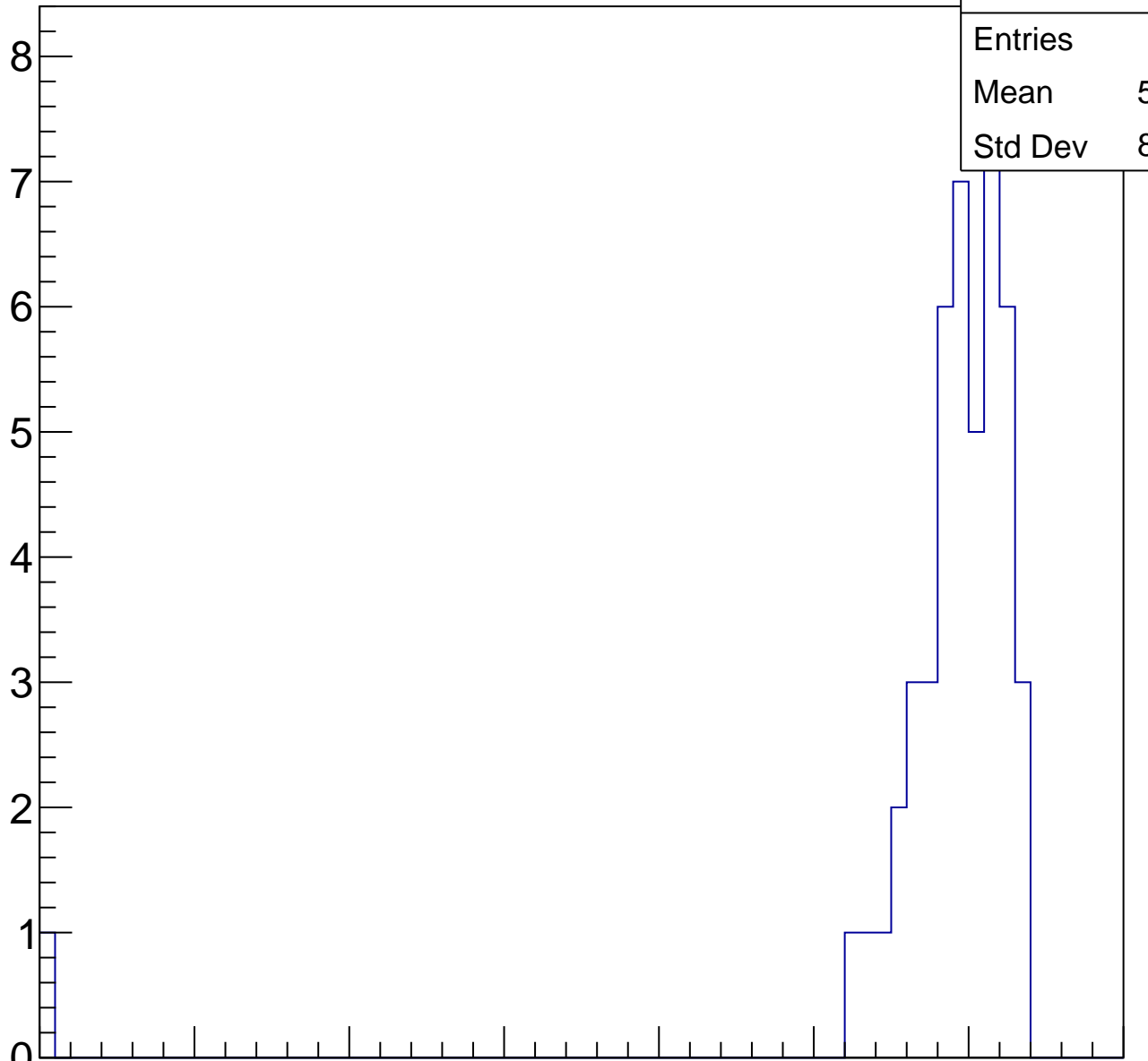
Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	47
Mean	57.83
Std Dev	8.924

ampl

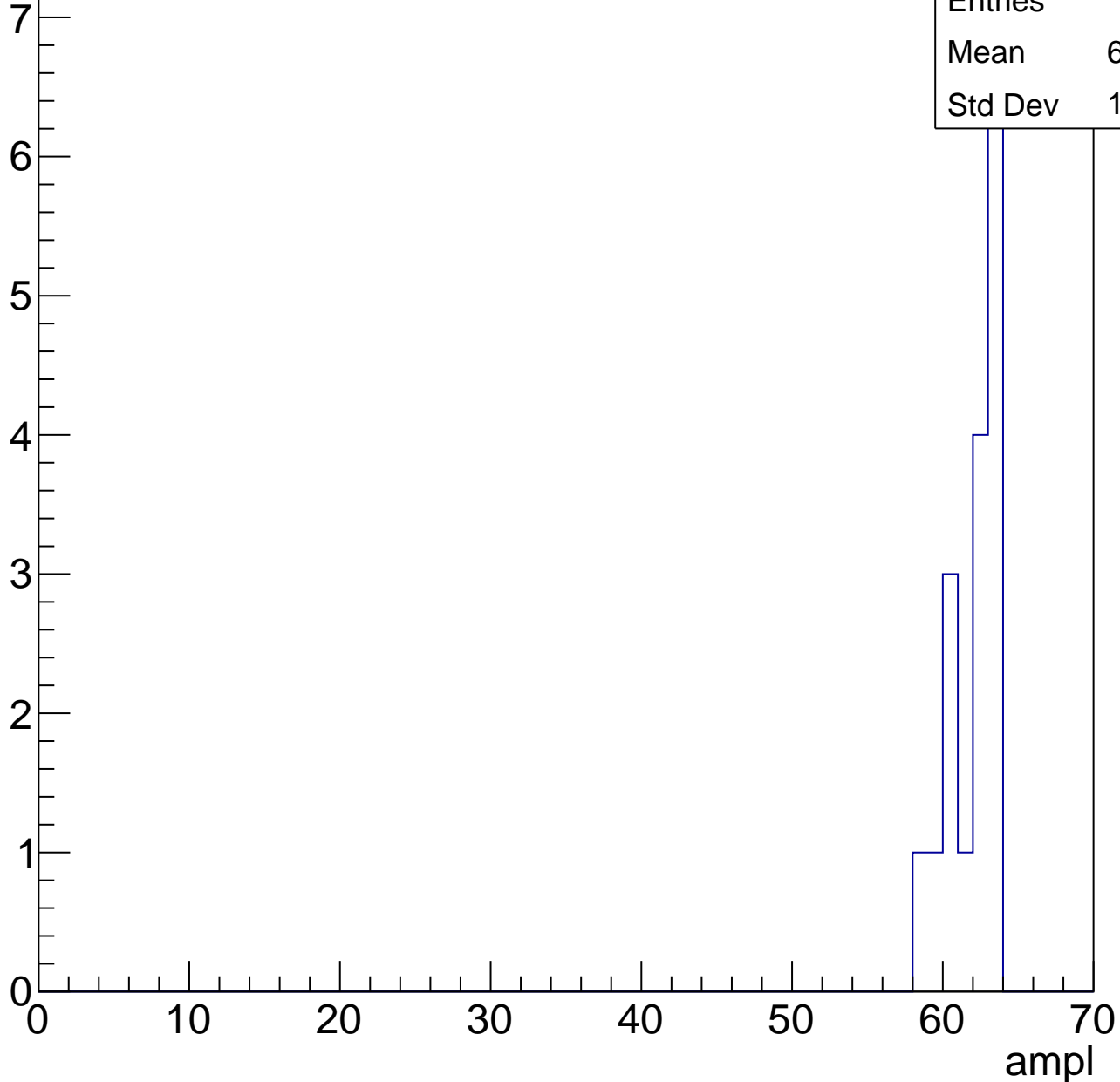
0 10 20 30 40 50 60 70



# B1L101S, U20-ch96, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U20-ch96, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L101S, U20-ch97, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	101
Mean	29.25
Std Dev	5.675

**Gaus mean : 29.7674**

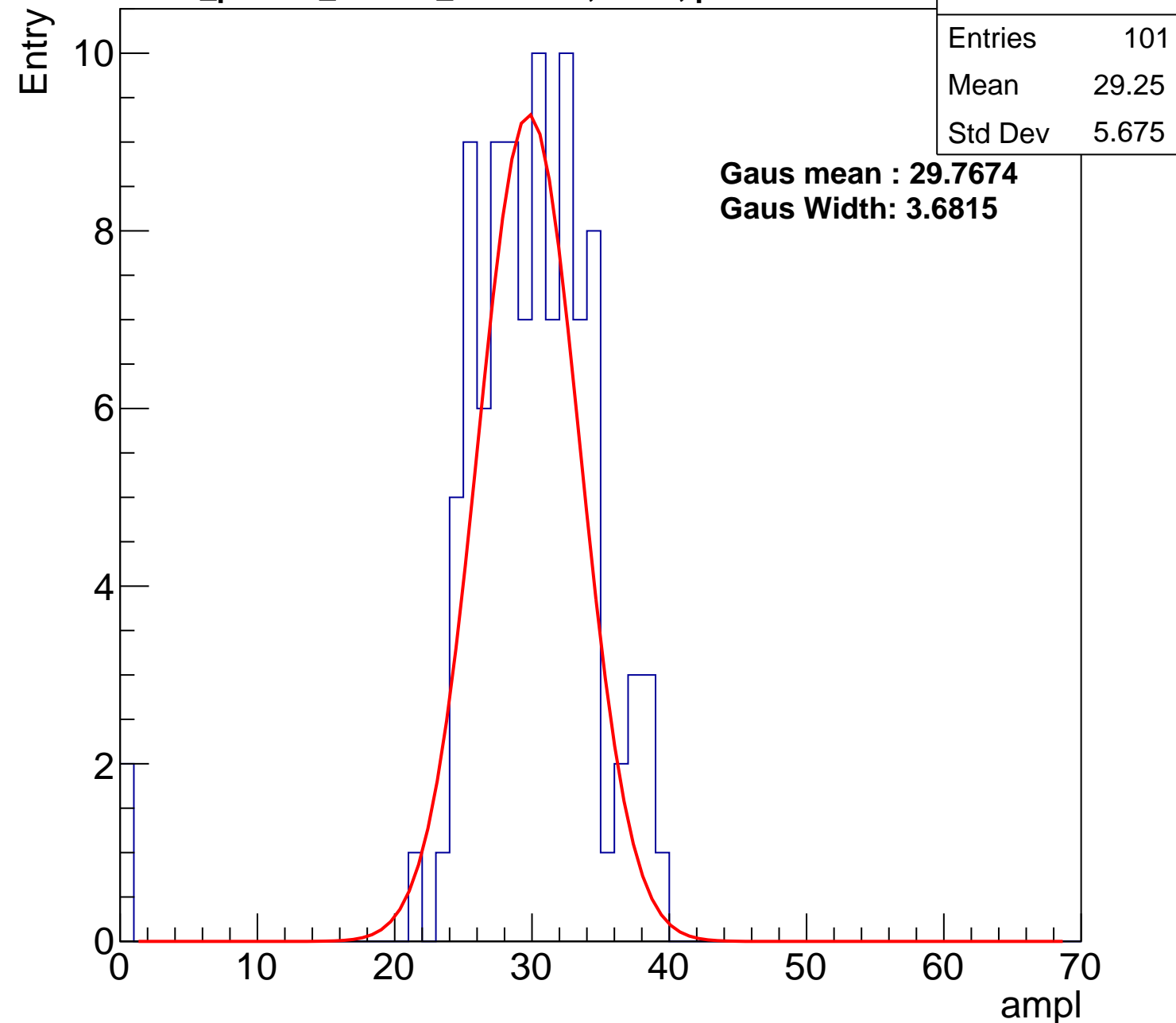
**Gaus Width: 3.6815**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U20-ch97, adc1

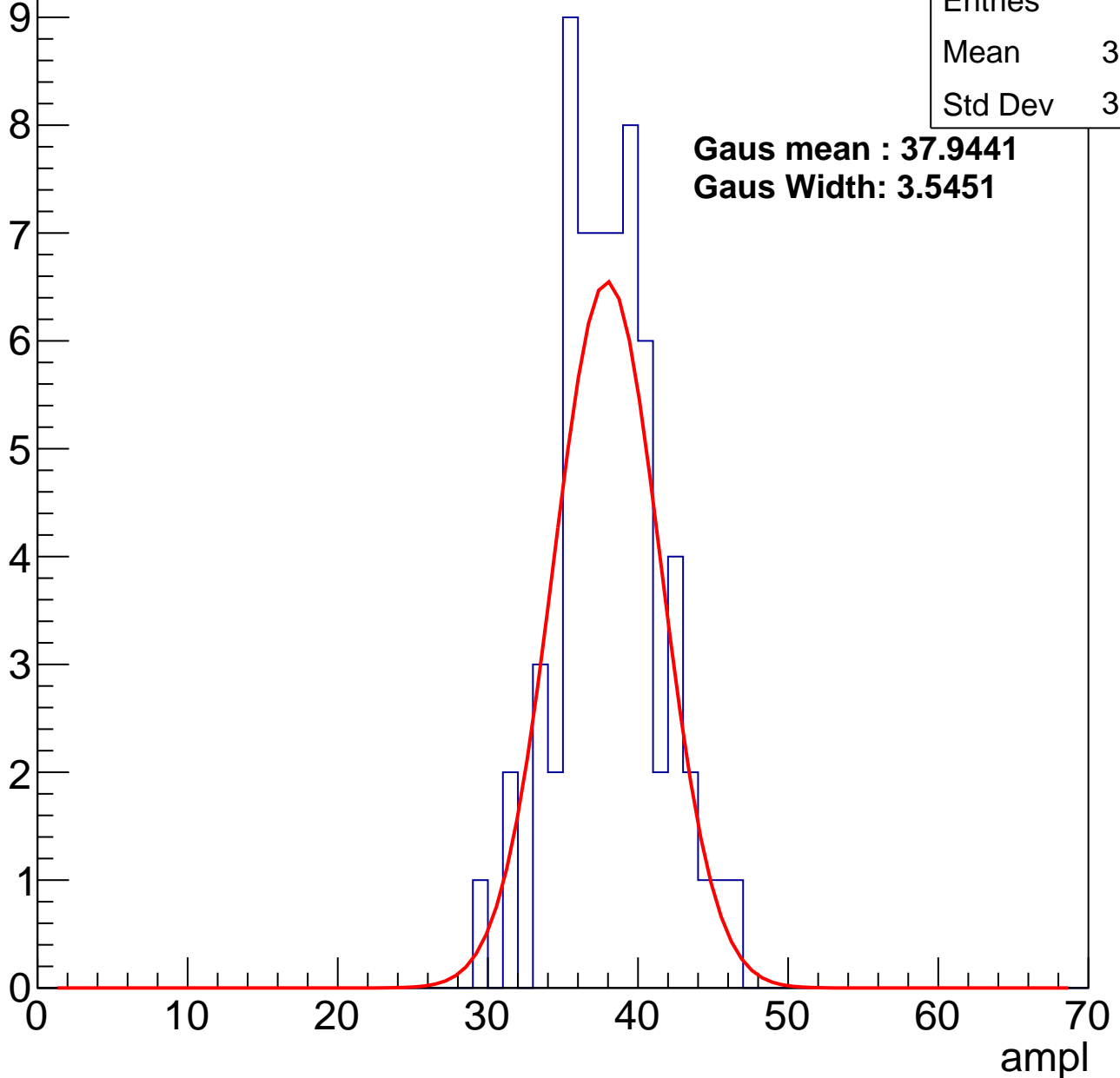
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	37.67
Std Dev	3.352

**Gaus mean : 37.9441**

**Gaus Width: 3.5451**



# B1L101S, U20-ch97, adc2

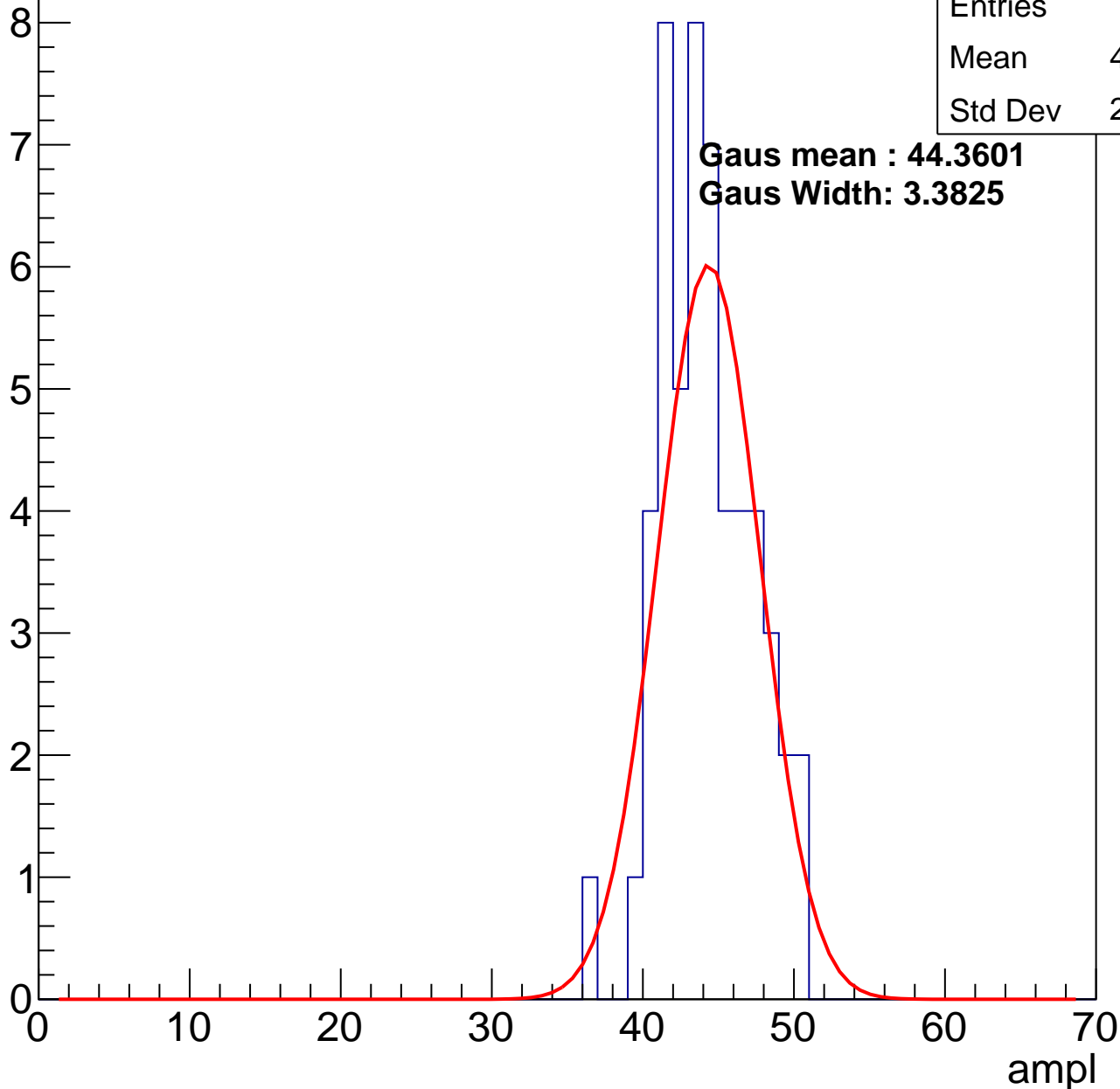
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	53
Mean	43.75
Std Dev	2.996

**Gaus mean : 44.3601**

**Gaus Width: 3.3825**

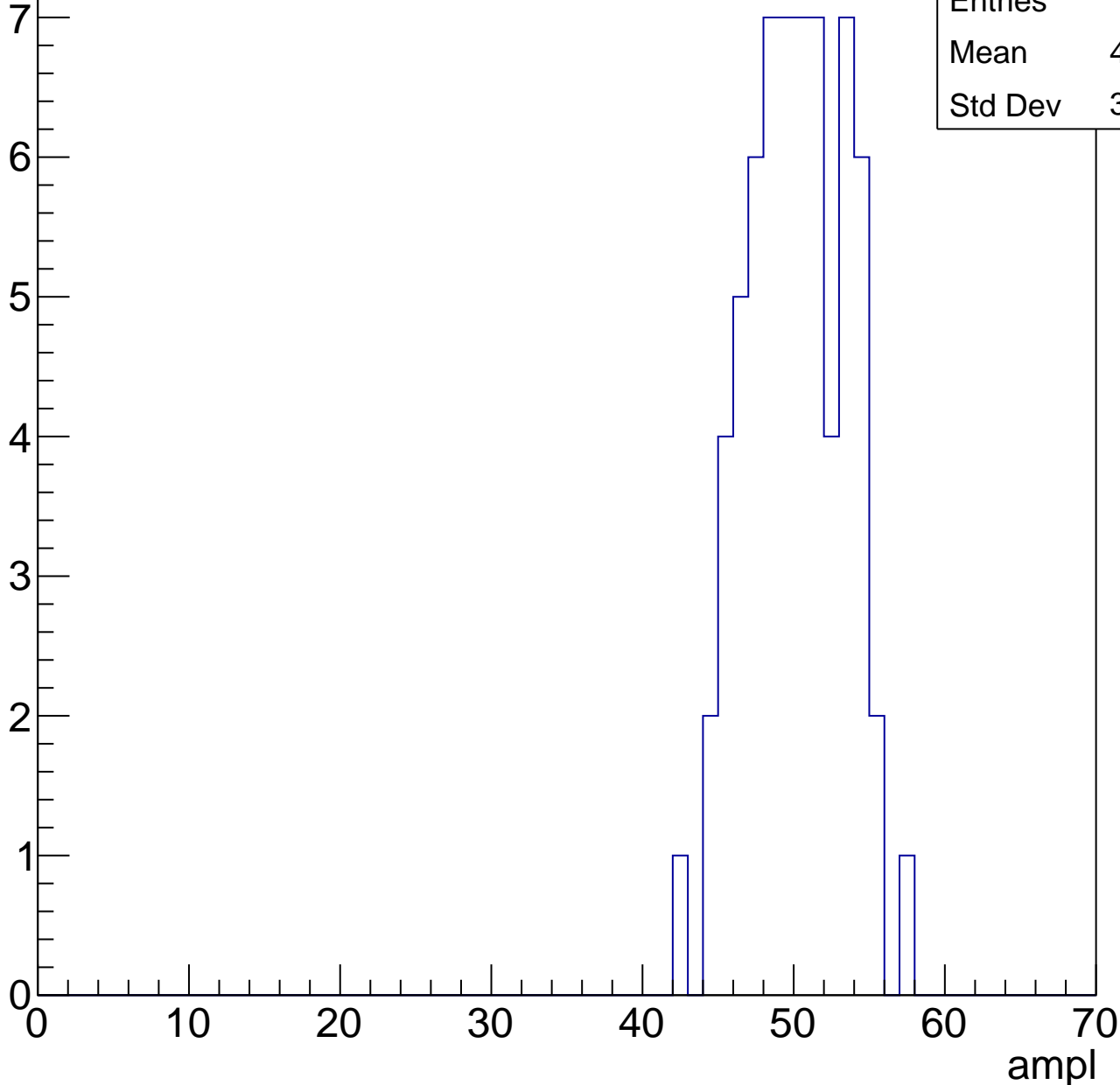


# B1L101S, U20-ch97, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	66
Mean	49.67
Std Dev	3.207

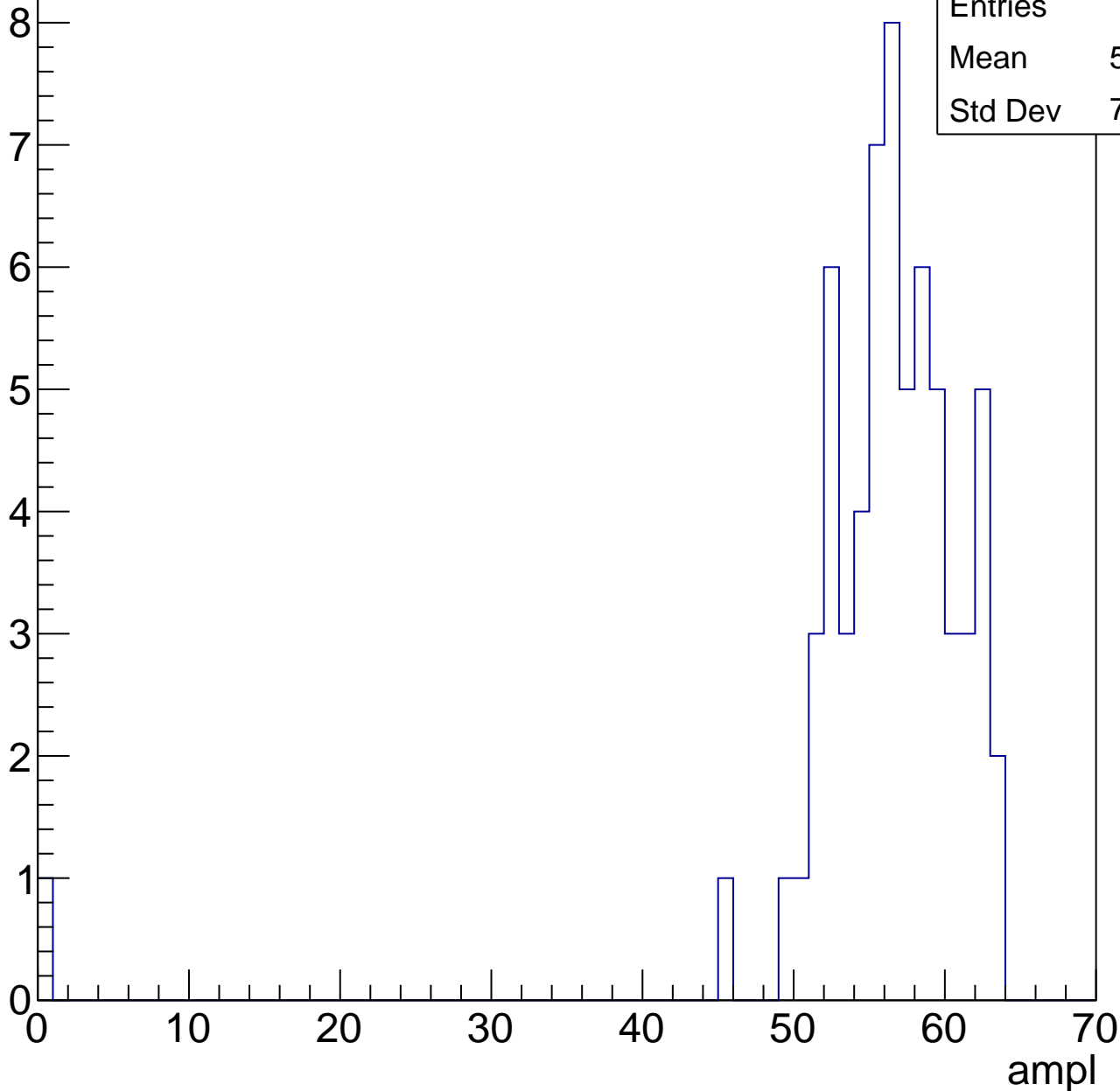


# B1L101S, U20-ch97, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	55.38
Std Dev	7.919

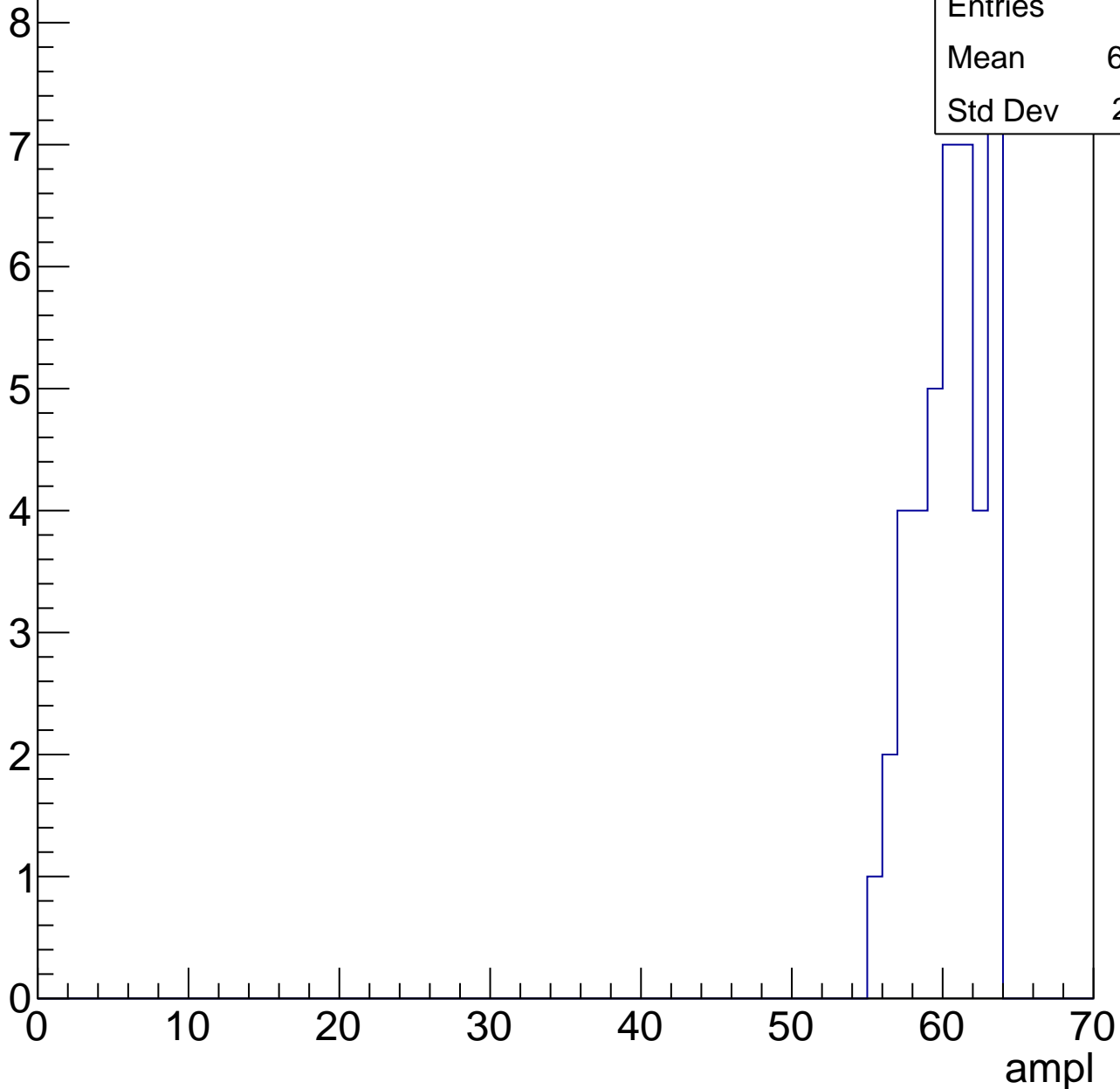


# B1L101S, U20-ch97, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	42
Mean	60.02
Std Dev	2.231



# B1L101S, U20-ch97, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U20-ch97, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	0
Std Dev	0

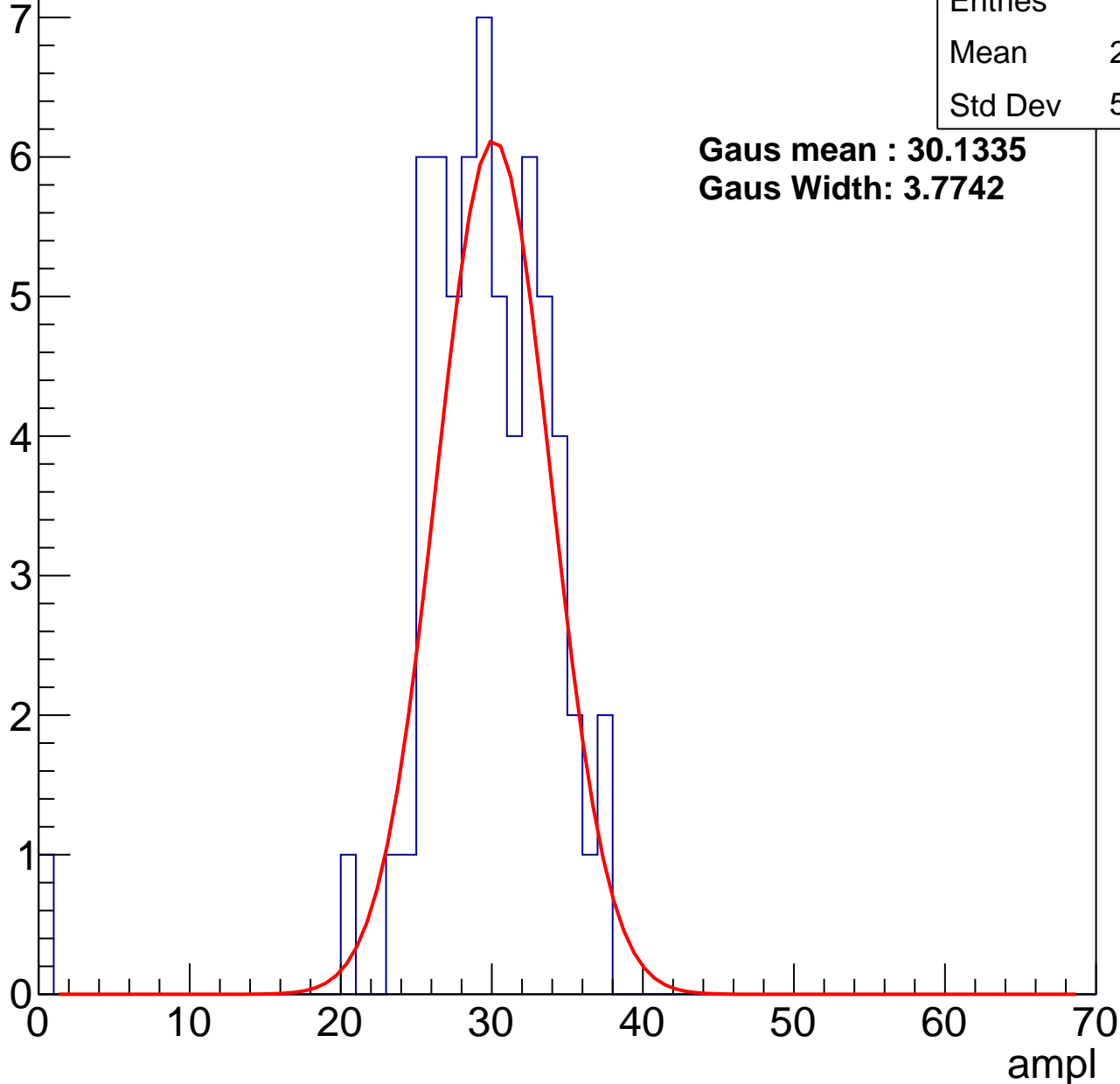
# B1L101S, U20-ch98, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	28.98
Std Dev	5.138

**Gaus mean : 30.1335**  
**Gaus Width: 3.7742**



# B1L101S, U20-ch98, adc1

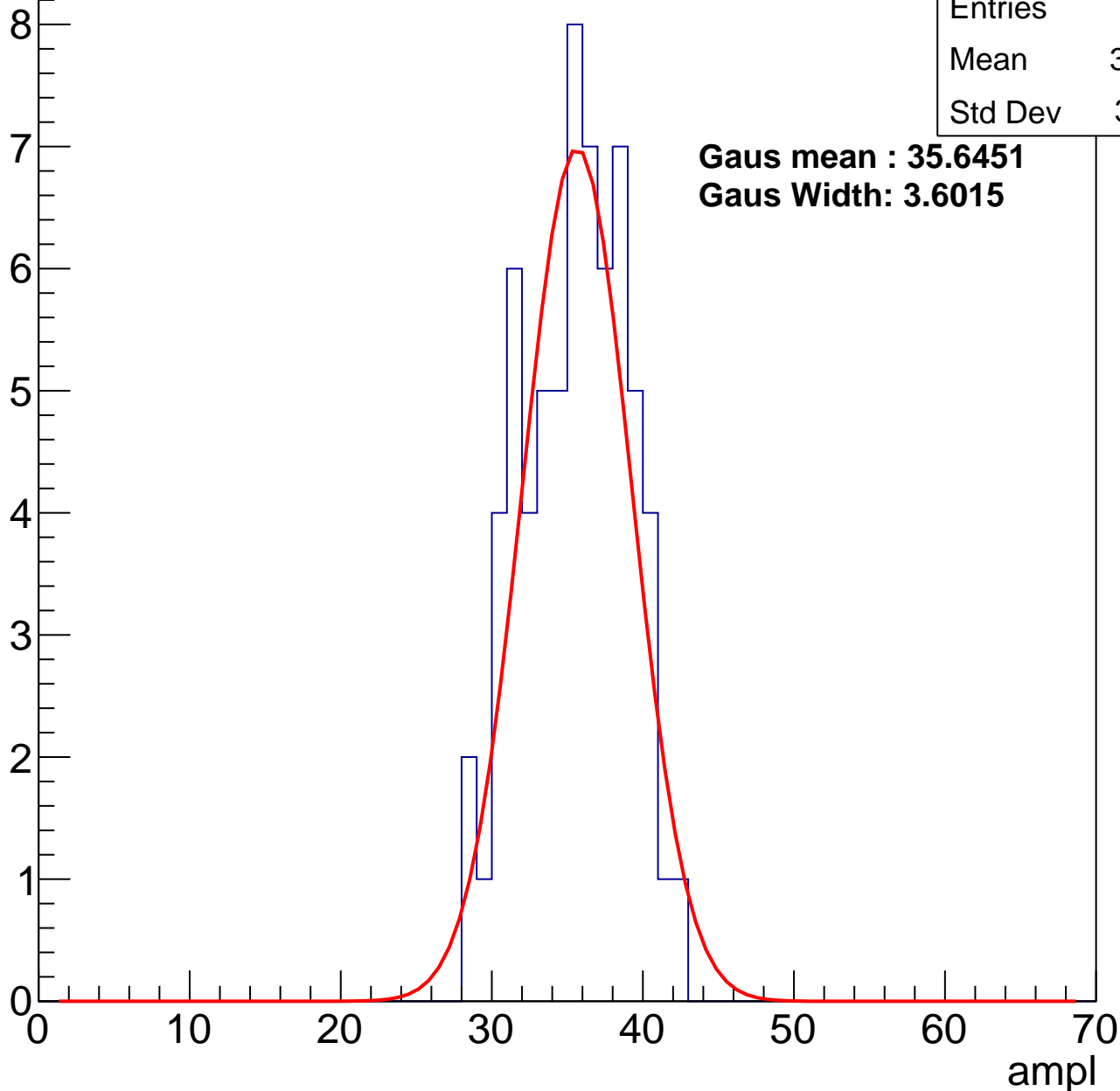
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	66
Mean	35.03
Std Dev	3.371

**Gaus mean : 35.6451**

**Gaus Width: 3.6015**



# B1L101S, U20-ch98, adc2

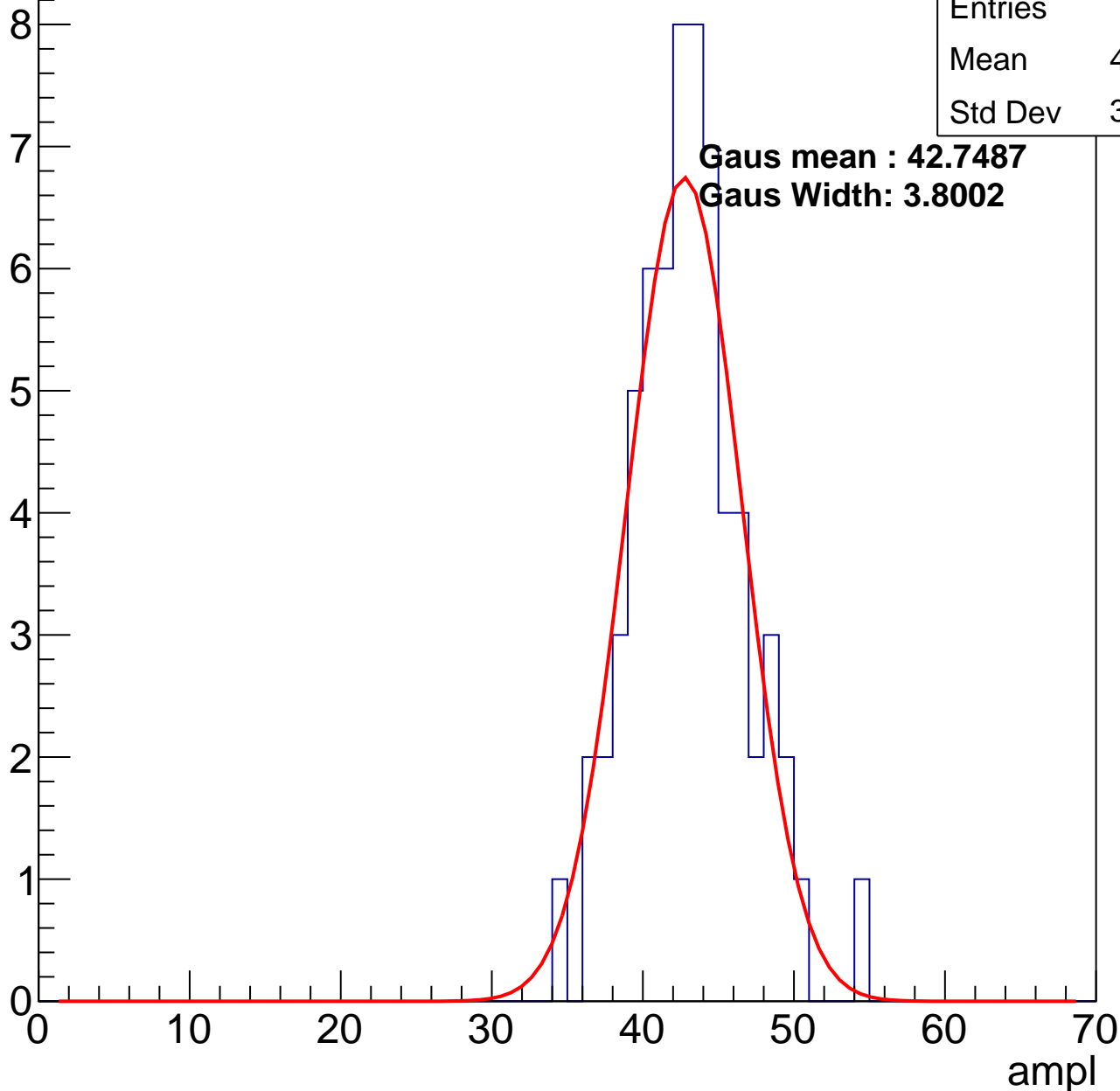
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	42.57
Std Dev	3.696

**Gaus mean : 42.7487**

**Gaus Width: 3.8002**

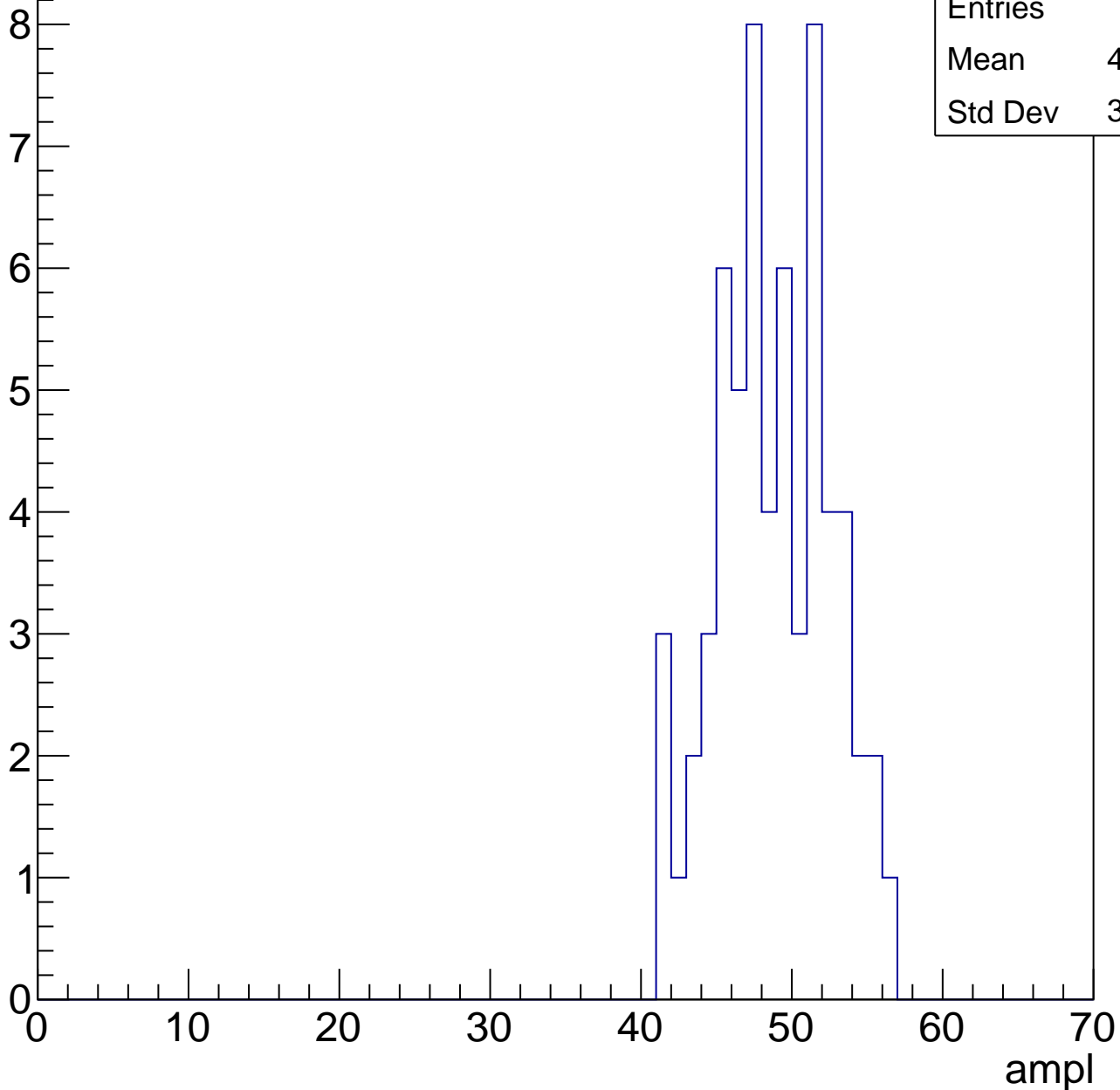


# B1L101S, U20-ch98, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	48.34
Std Dev	3.689

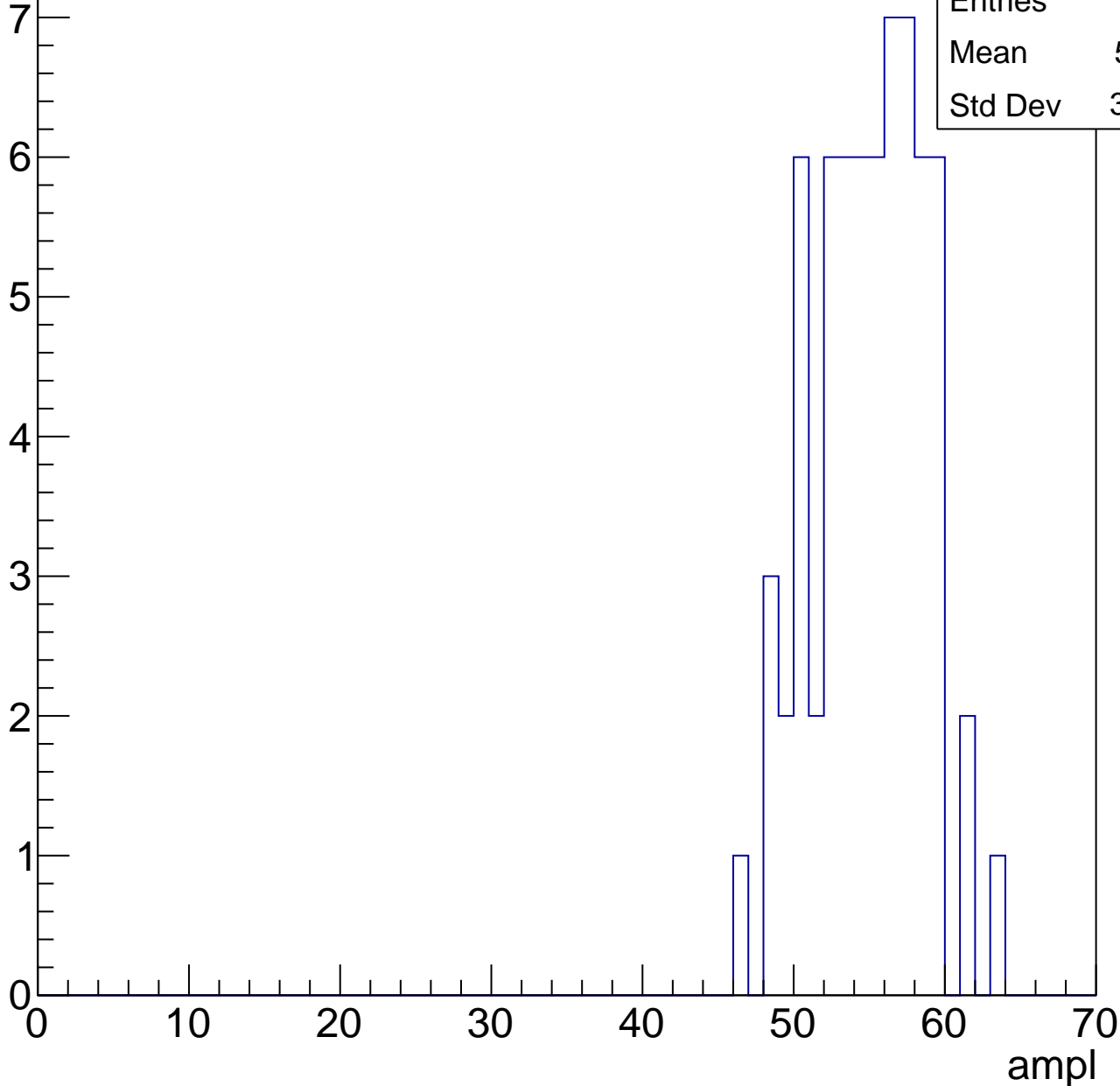


# B1L101S, U20-ch98, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	67
Mean	54.51
Std Dev	3.605

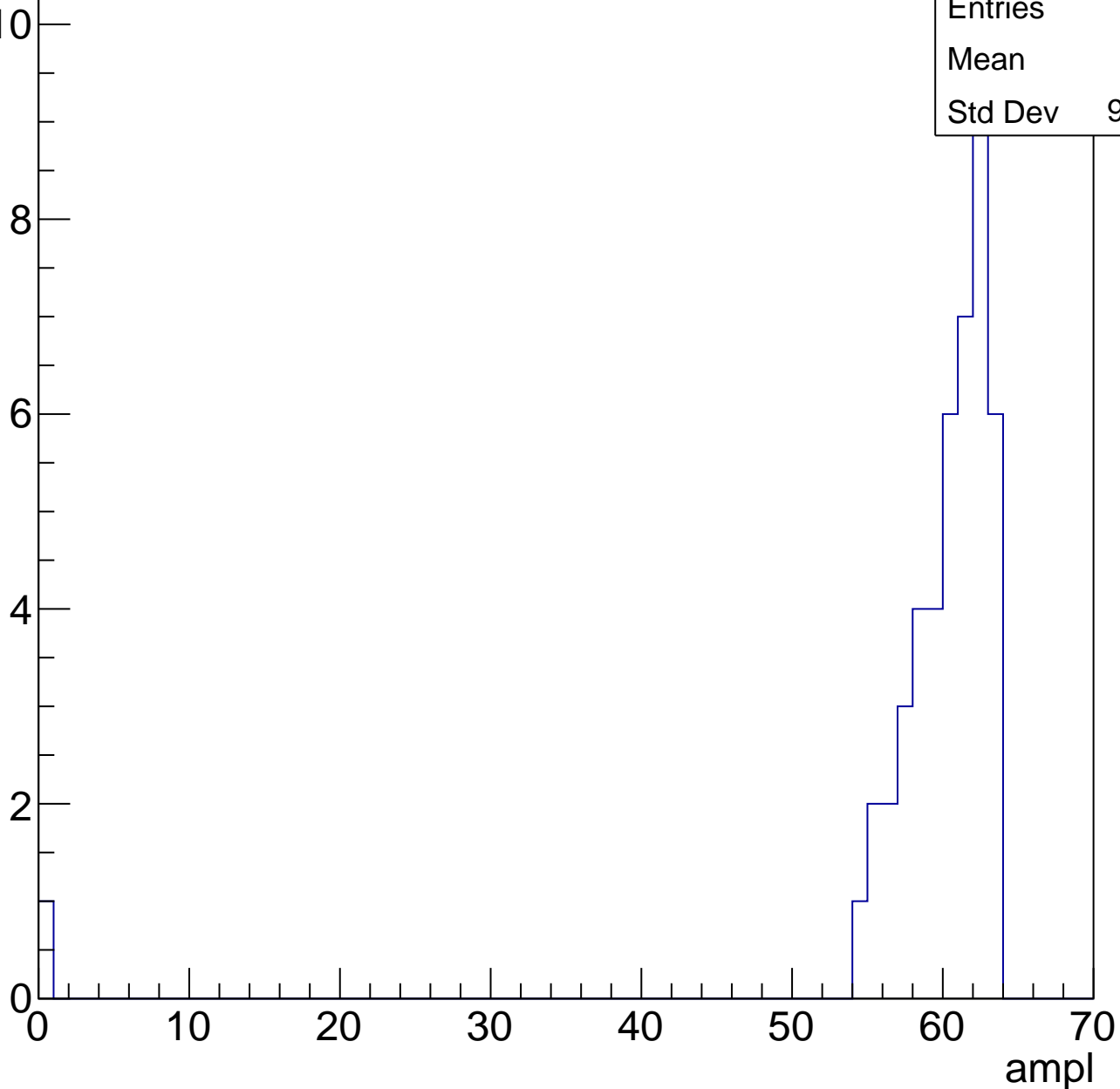


# B1L101S, U20-ch98, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

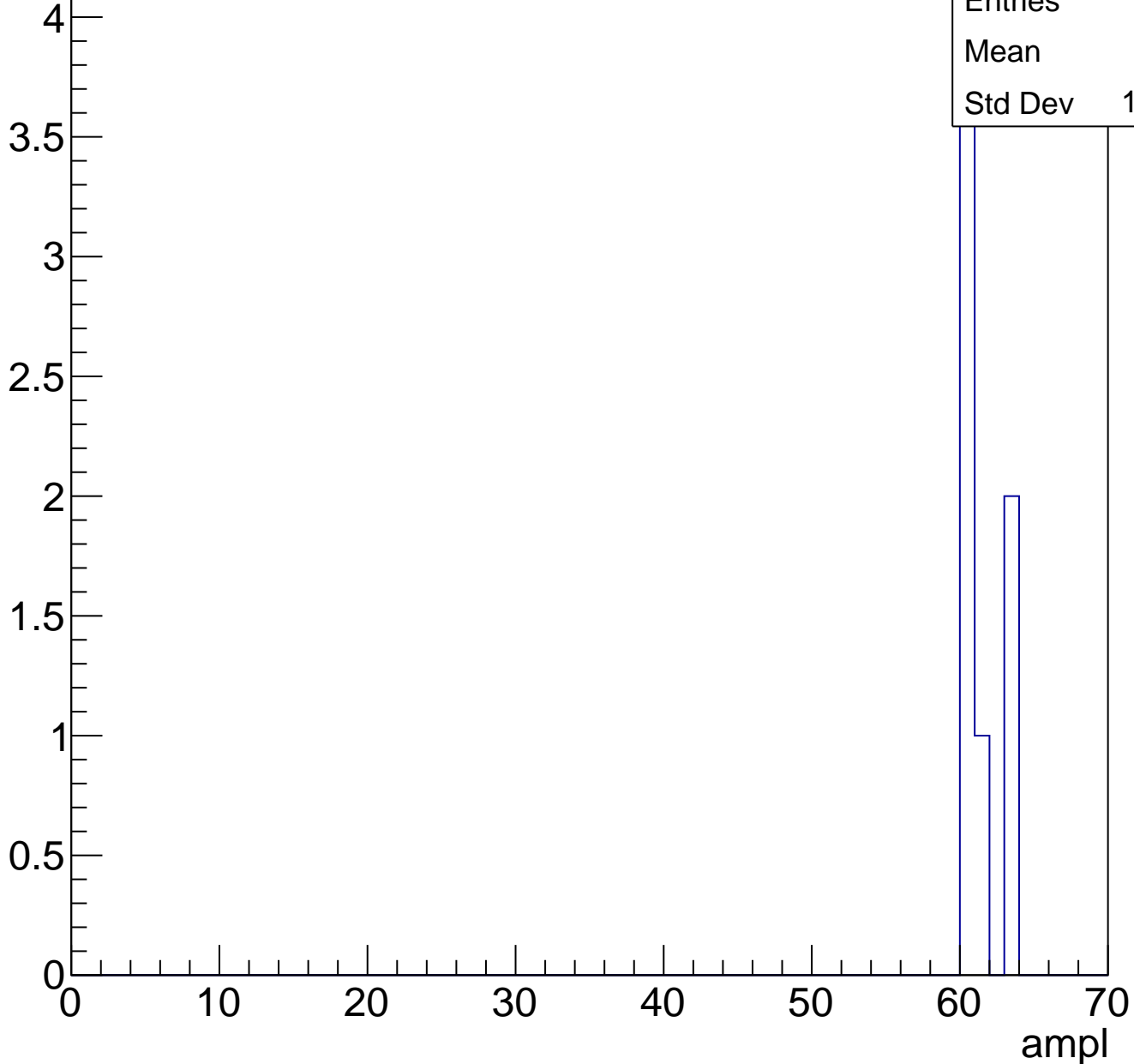
Entries	46
Mean	58.7
Std Dev	9.074



# B1L101S, U20-ch98, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U20-ch98, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U20-ch99, adc0

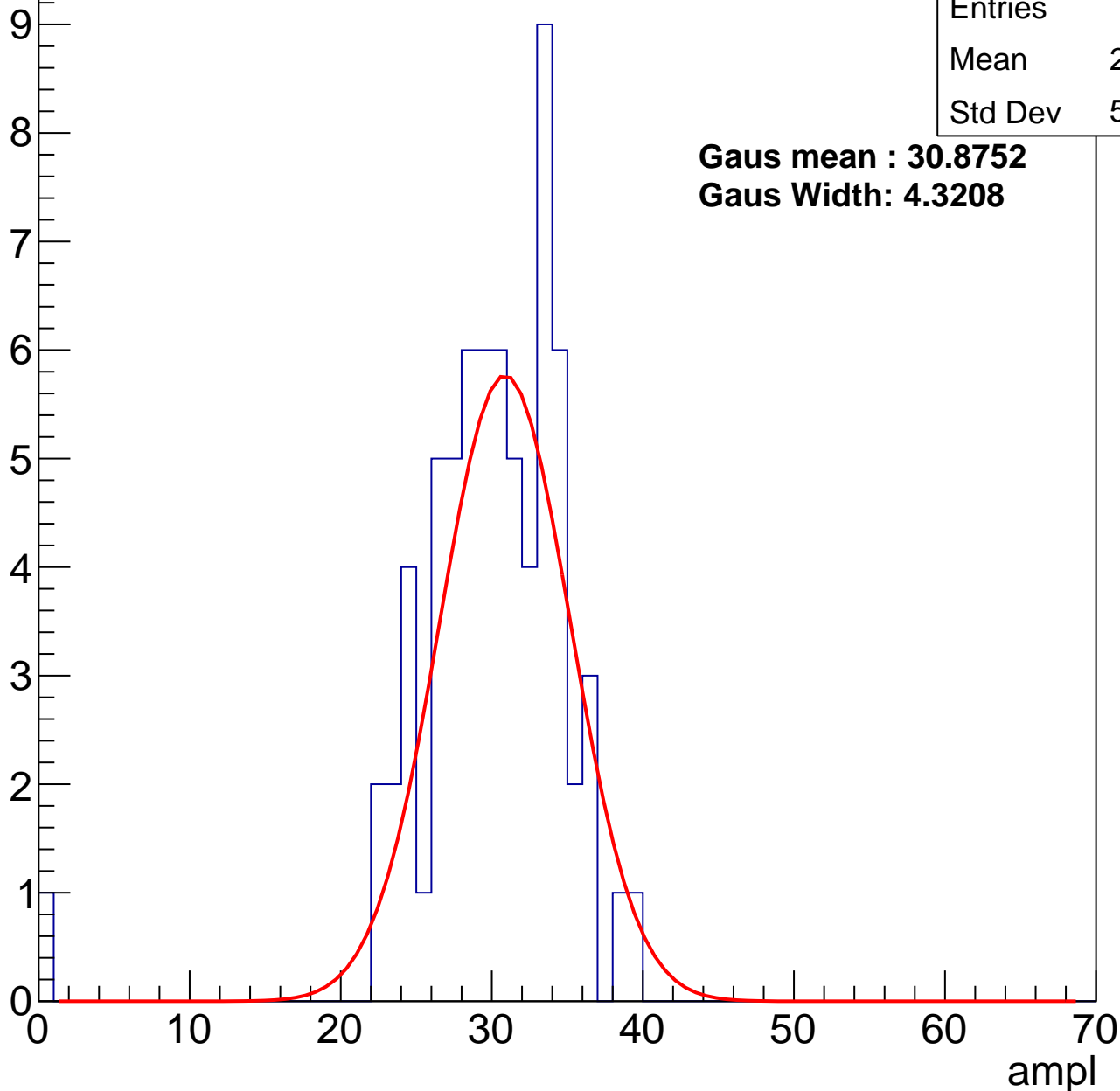
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	29.52
Std Dev	5.296

**Gaus mean : 30.8752**

**Gaus Width: 4.3208**



# B1L101S, U20-ch99, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	79
Mean	37.01
Std Dev	3.979

**Gaus mean : 38.1505**

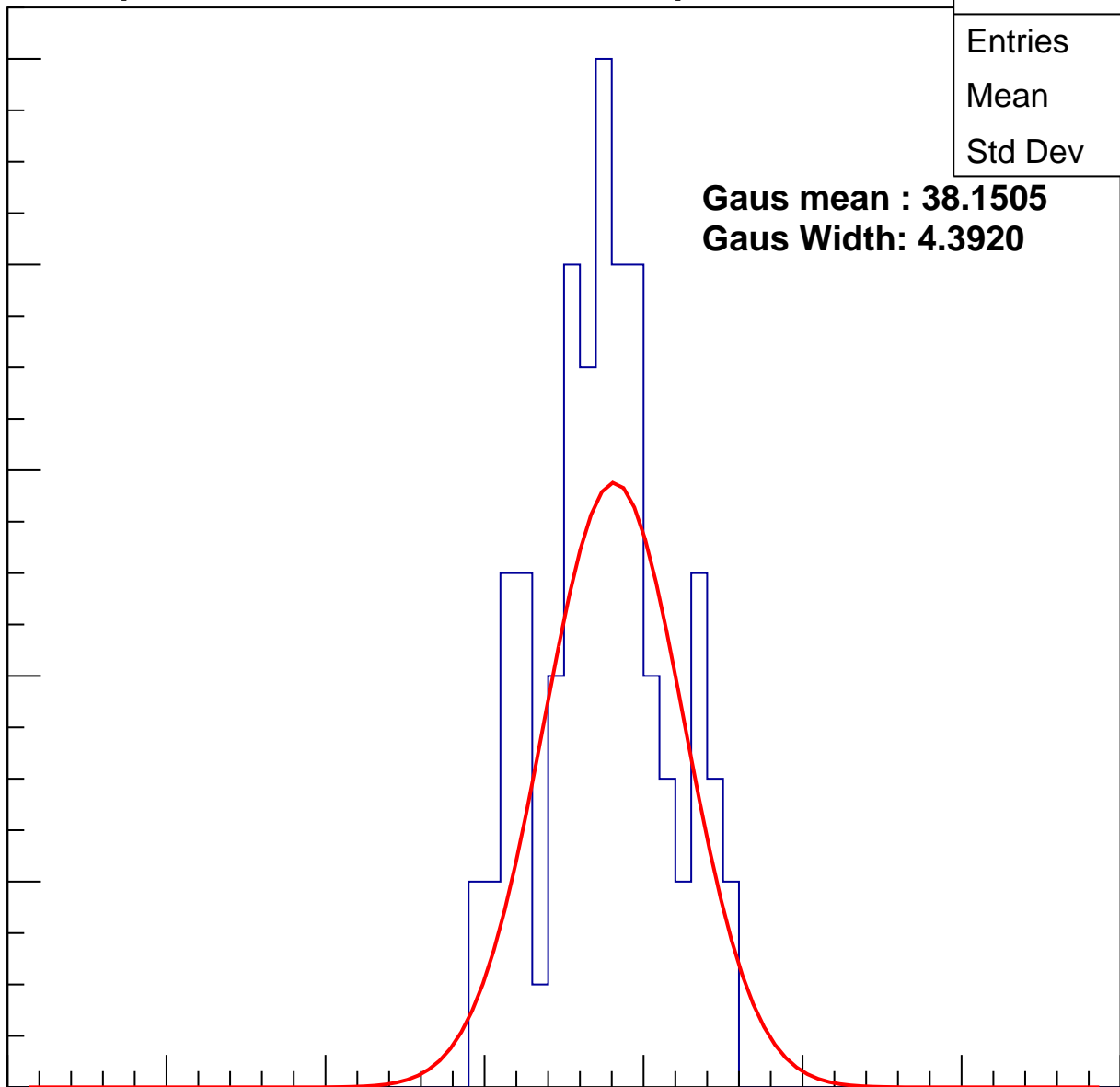
**Gaus Width: 4.3920**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U20-ch99, adc2

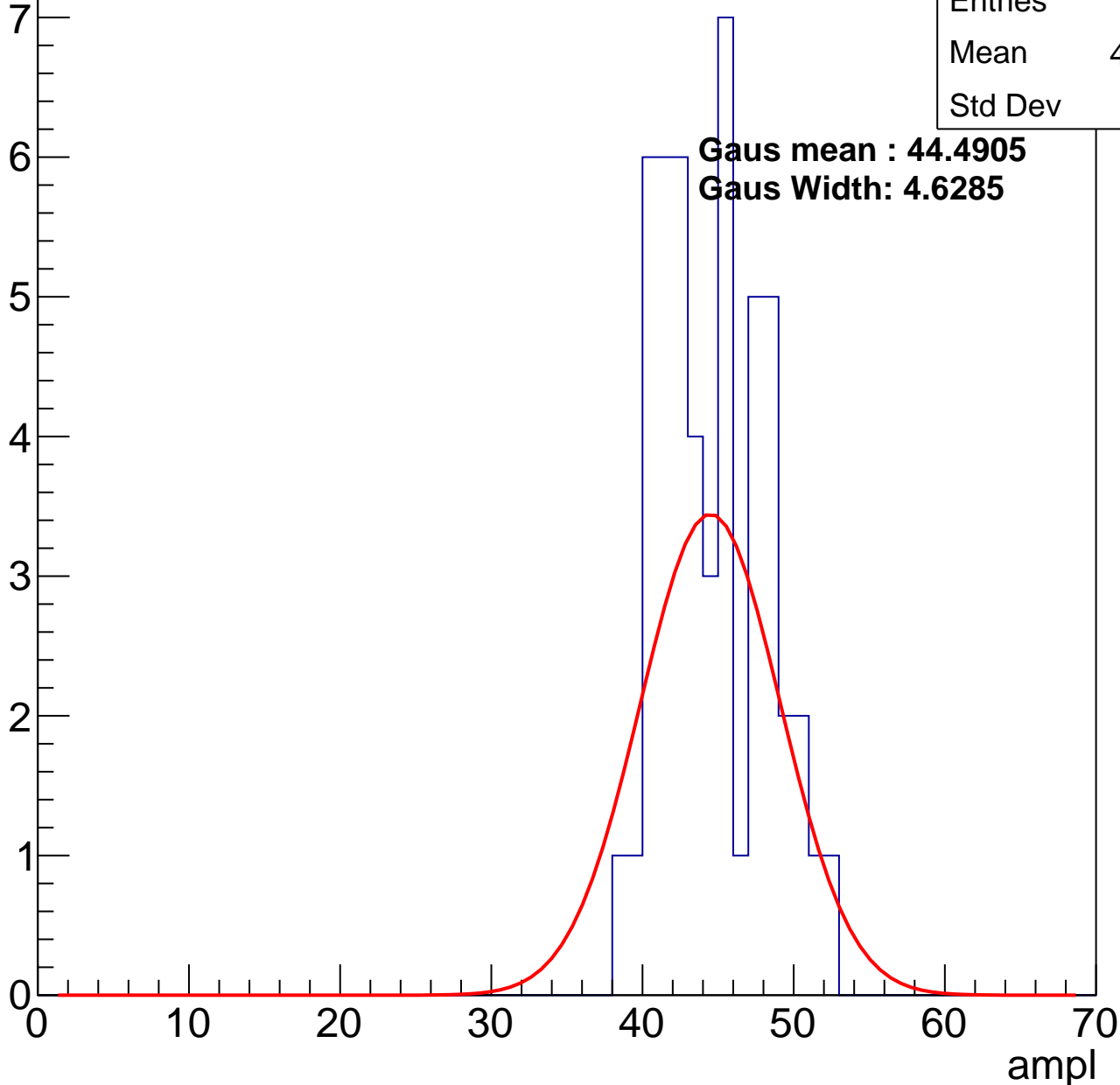
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	51
Mean	44.24
Std Dev	3.45

**Gaus mean : 44.4905**

**Gaus Width: 4.6285**

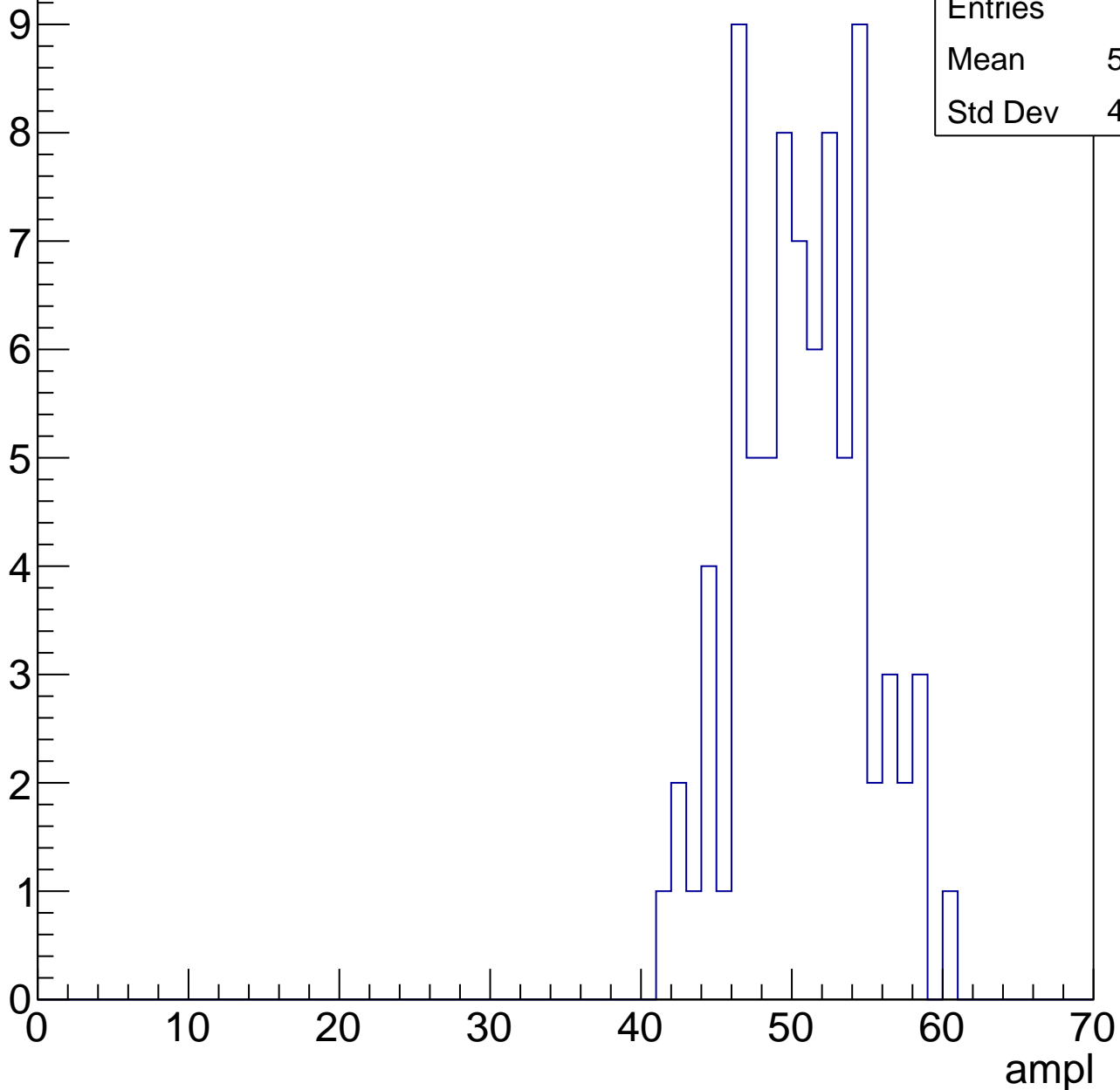


# B1L101S, U20-ch99, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

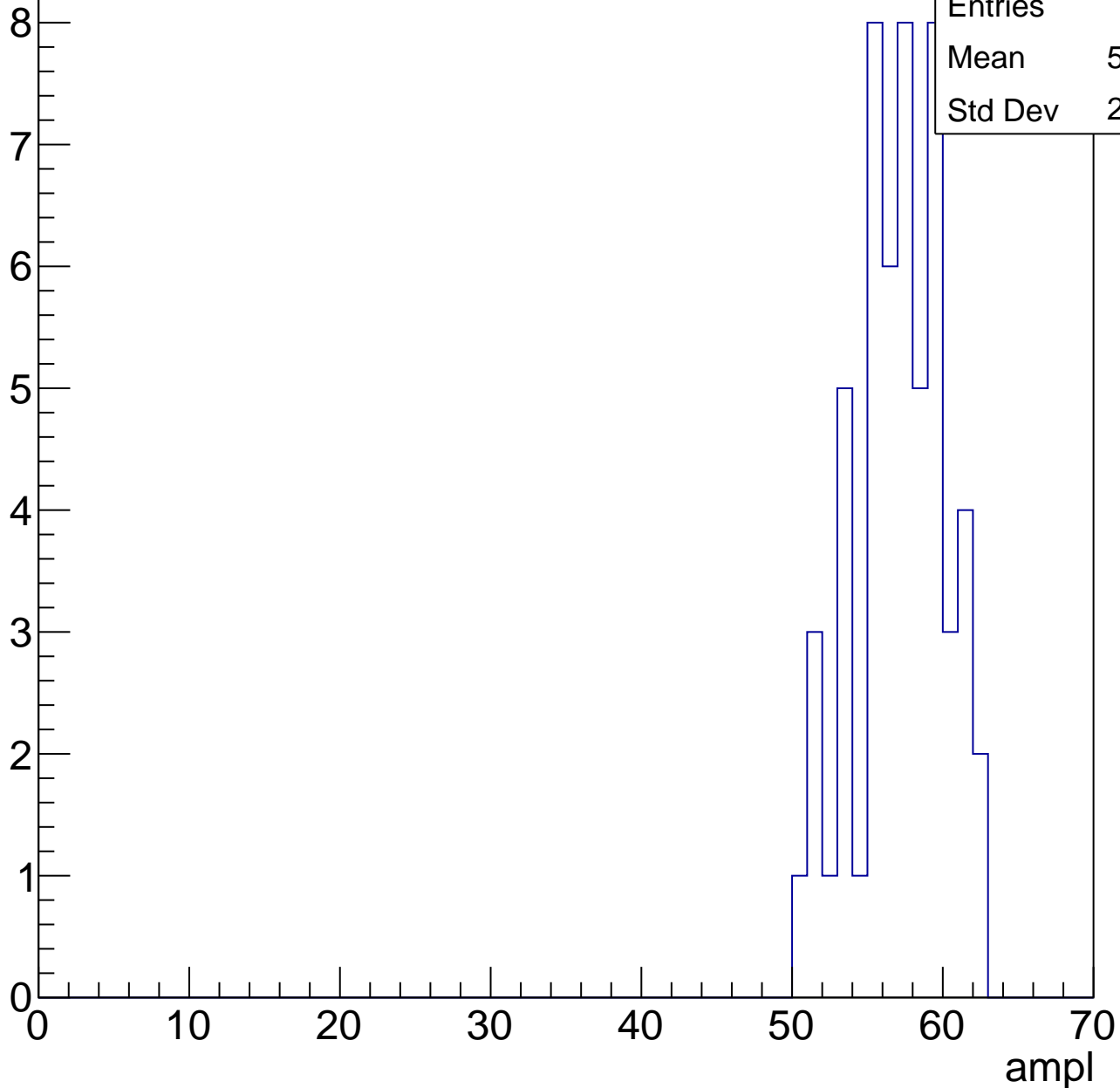
Entries	82
Mean	50.23
Std Dev	4.153



# B1L101S, U20-ch99, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



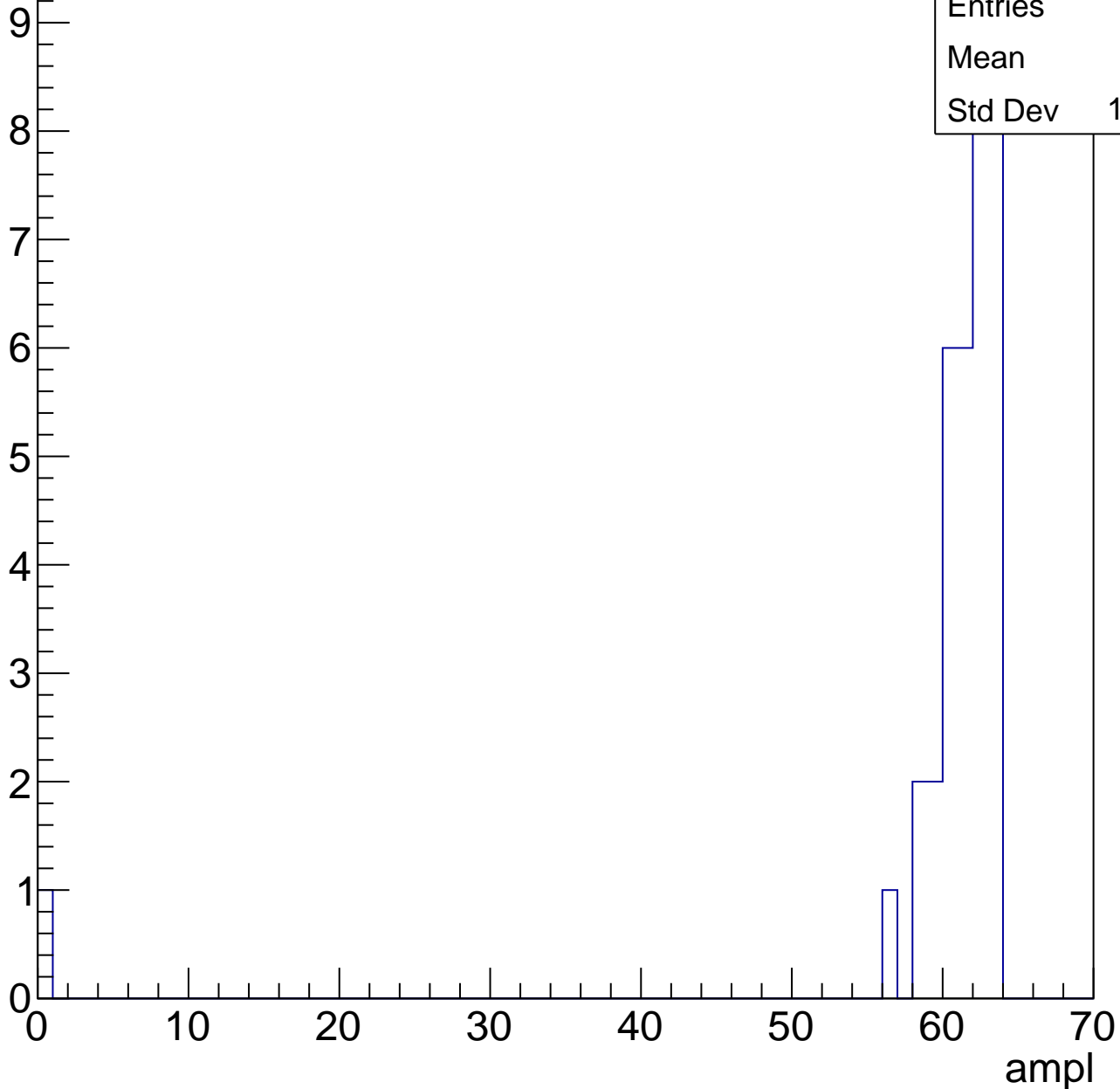
Entries	55
Mean	56.65
Std Dev	2.956

# B1L101S, U20-ch99, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	35
Mean	59.4
Std Dev	10.33



# B1L101S, U20-ch99, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U20-ch99, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	3
Mean	0
Std Dev	0

# B1L101S, U20-ch100, adc0

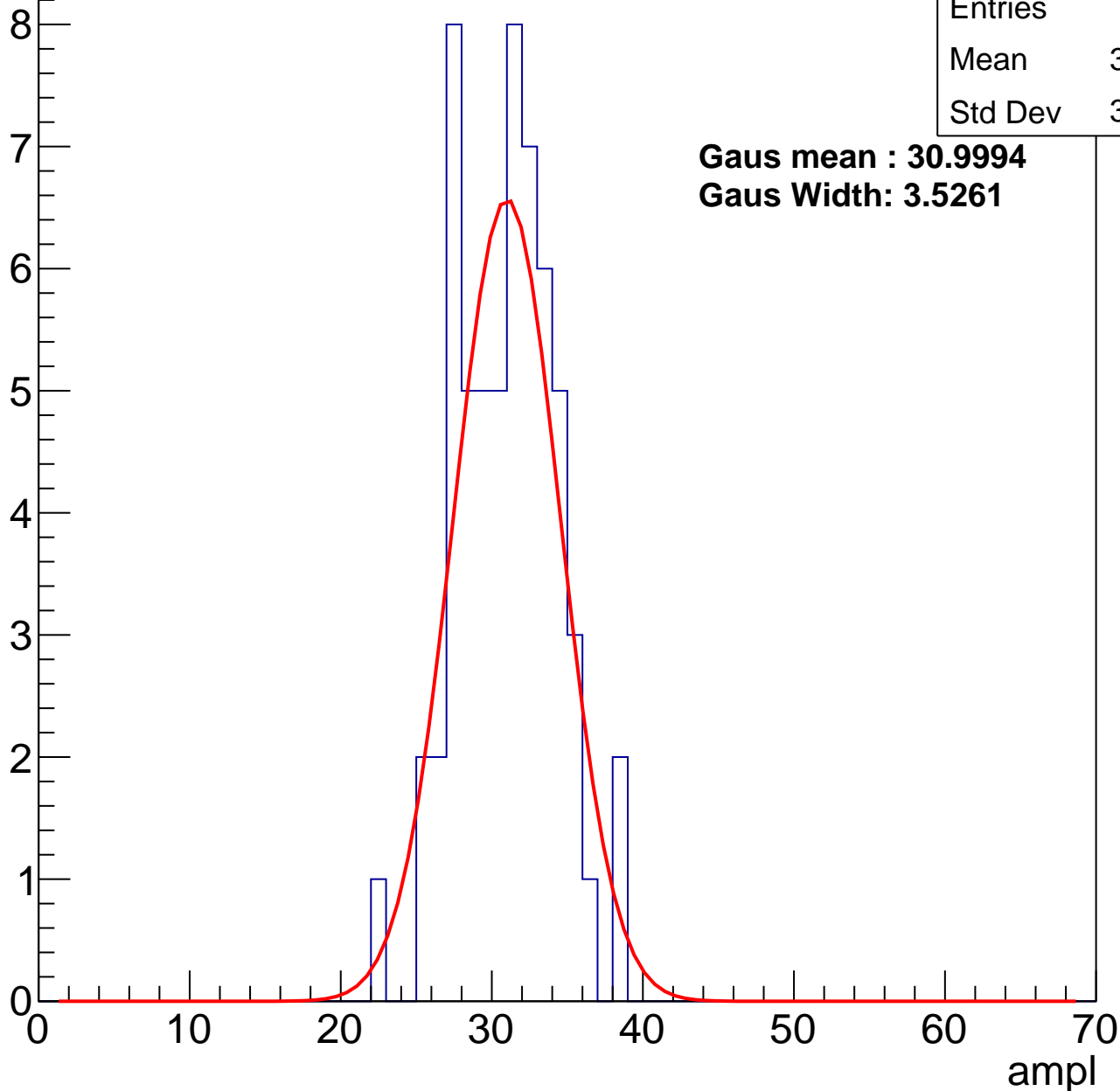
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	60
Mean	30.53
Std Dev	3.253

**Gaus mean : 30.9994**

**Gaus Width: 3.5261**



# B1L101S, U20-ch100, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	73
Mean	36.47
Std Dev	5.5

**Gaus mean : 37.6612**

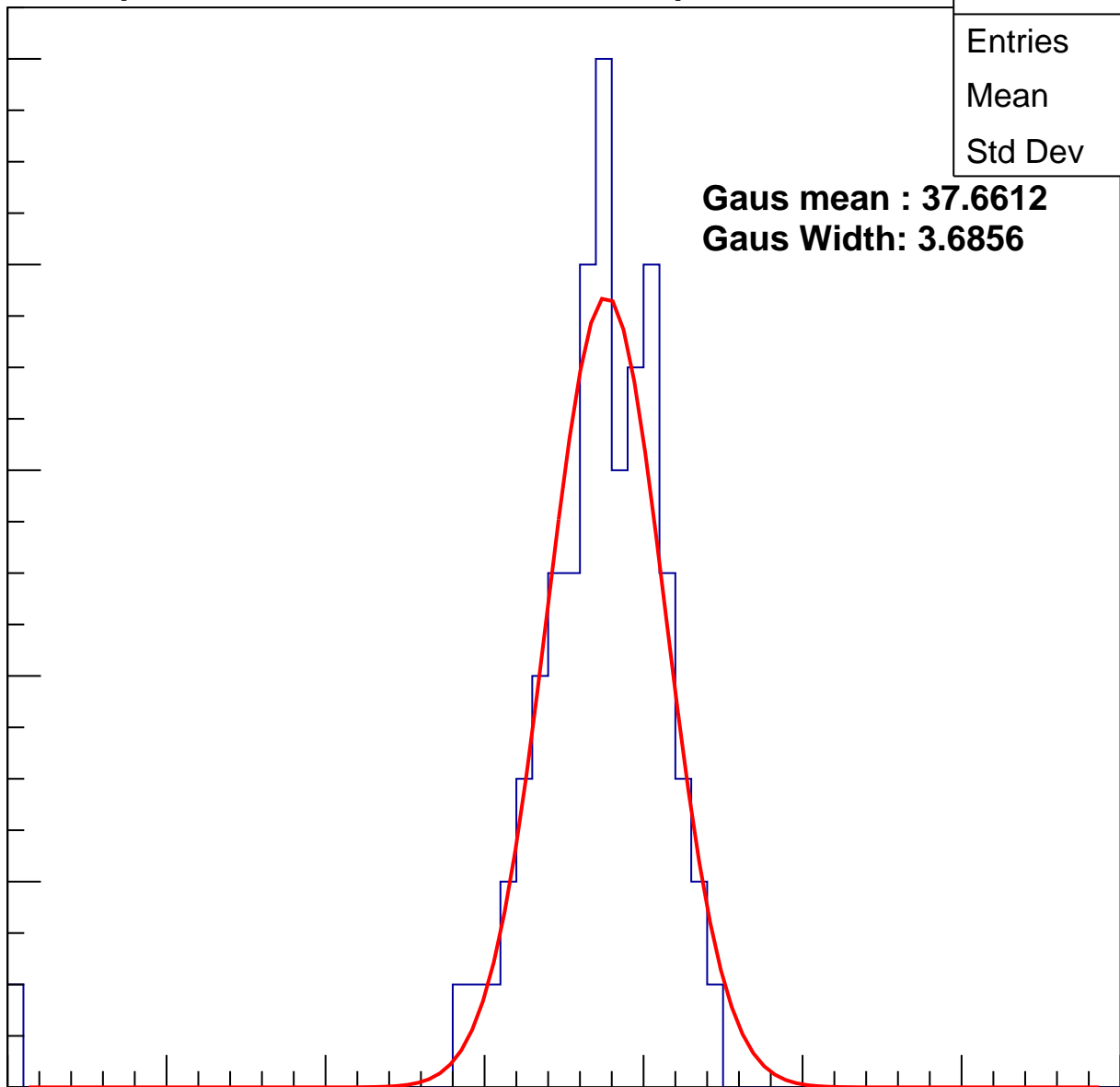
**Gaus Width: 3.6856**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U20-ch100, adc2

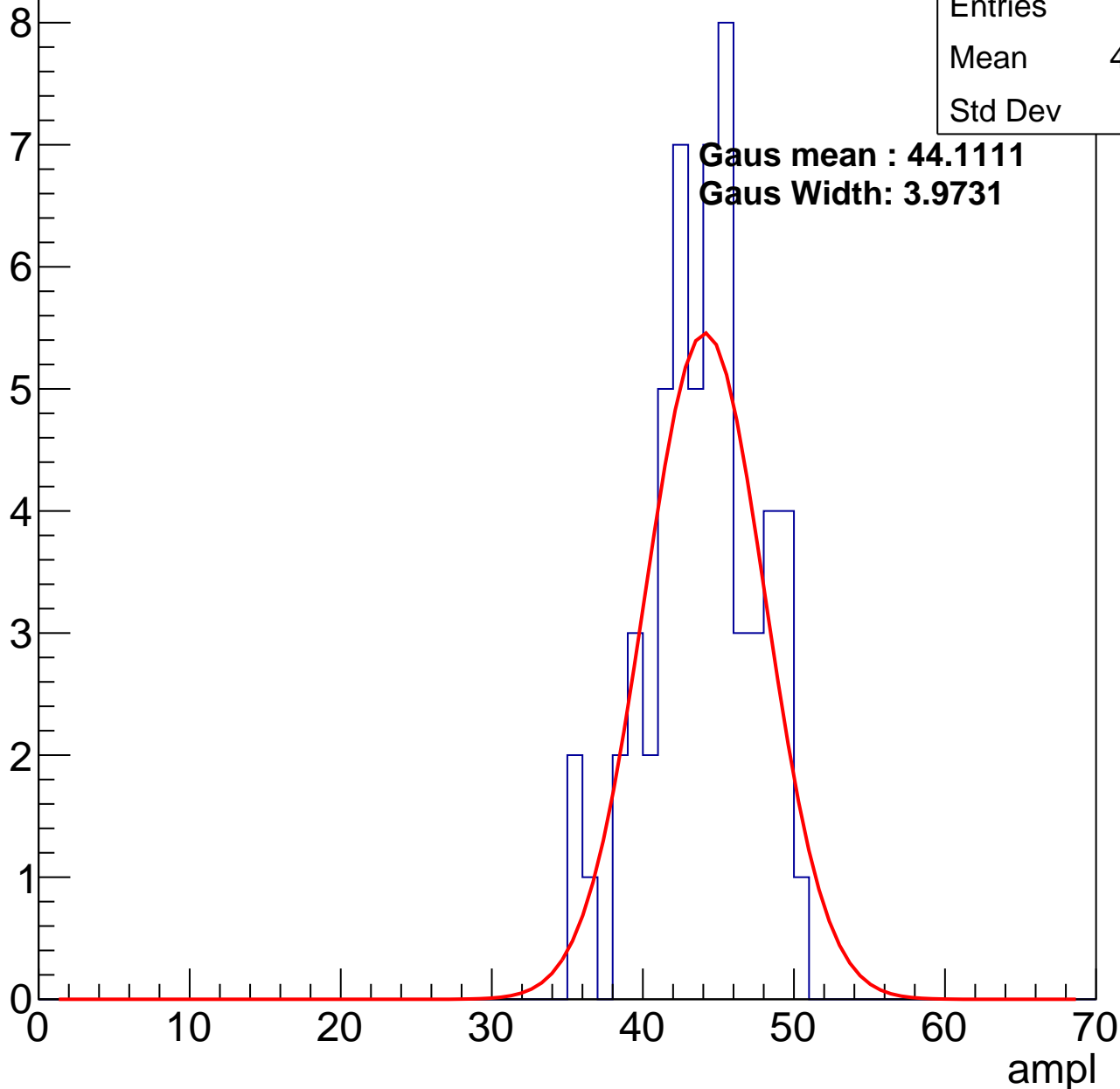
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	57
Mean	43.47
Std Dev	3.54

**Gaus mean : 44.1111**

**Gaus Width: 3.9731**

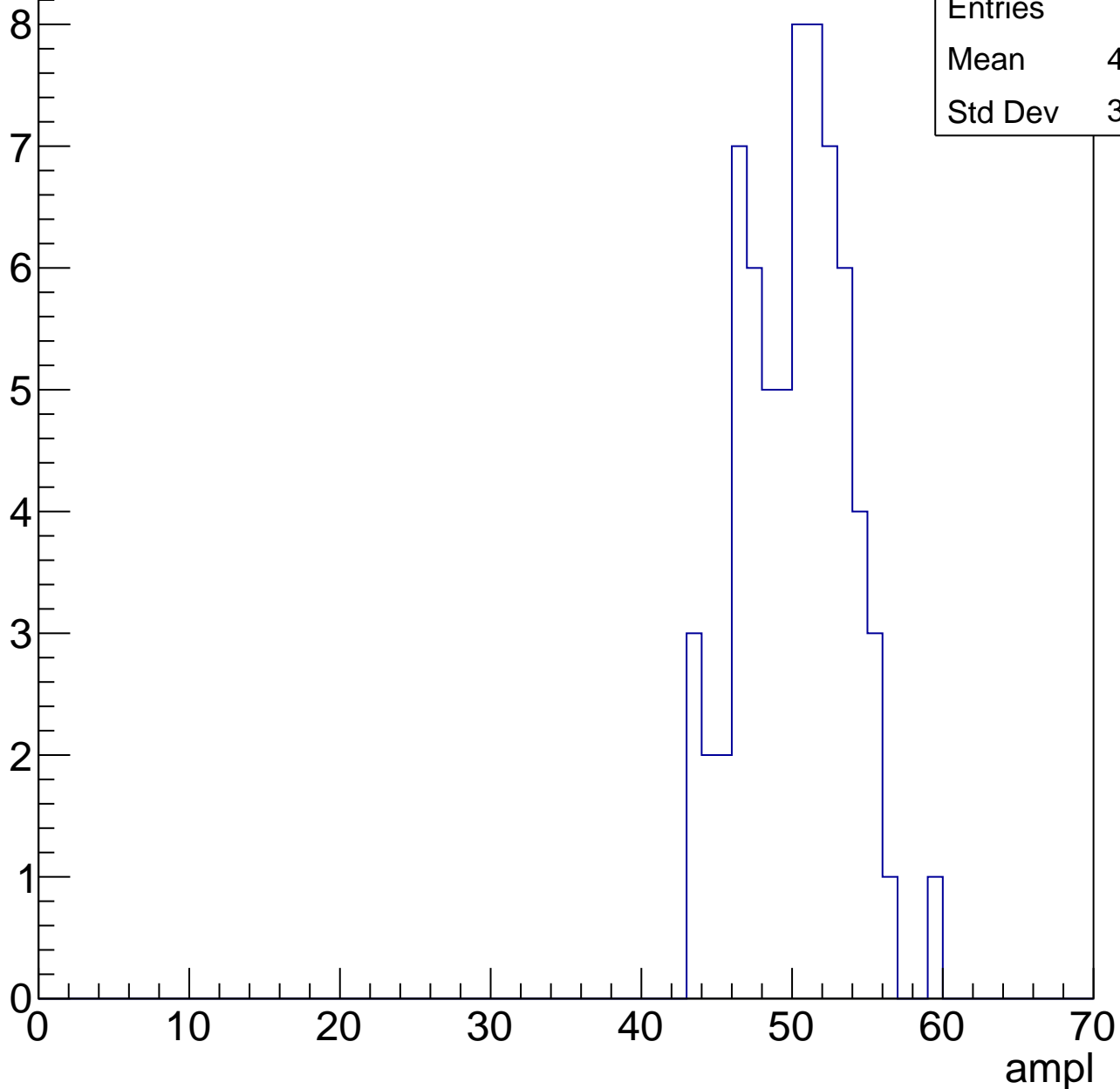


# B1L101S, U20-ch100, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	49.74
Std Dev	3.433

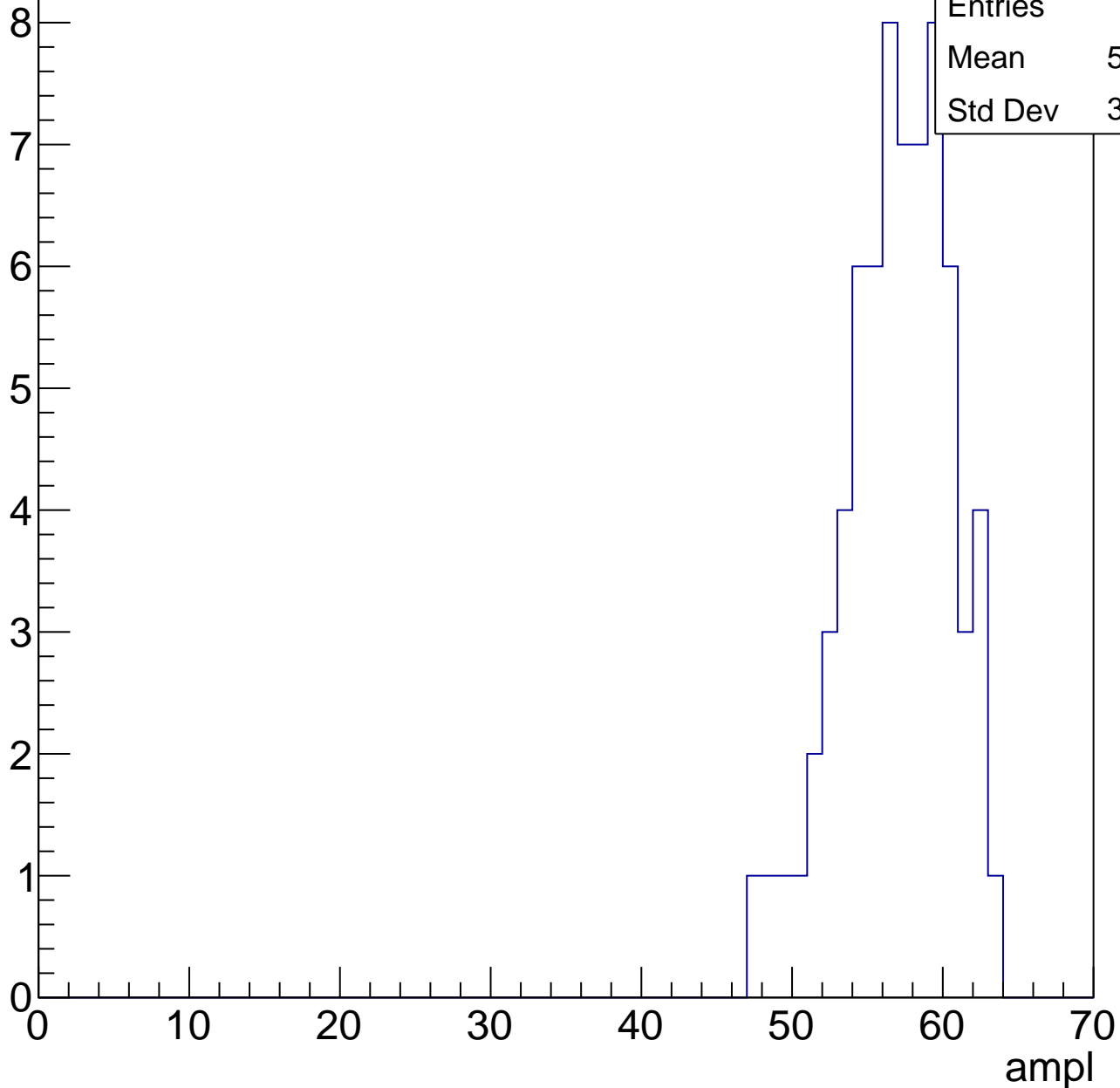


# B1L101S, U20-ch100, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	56.48
Std Dev	3.508

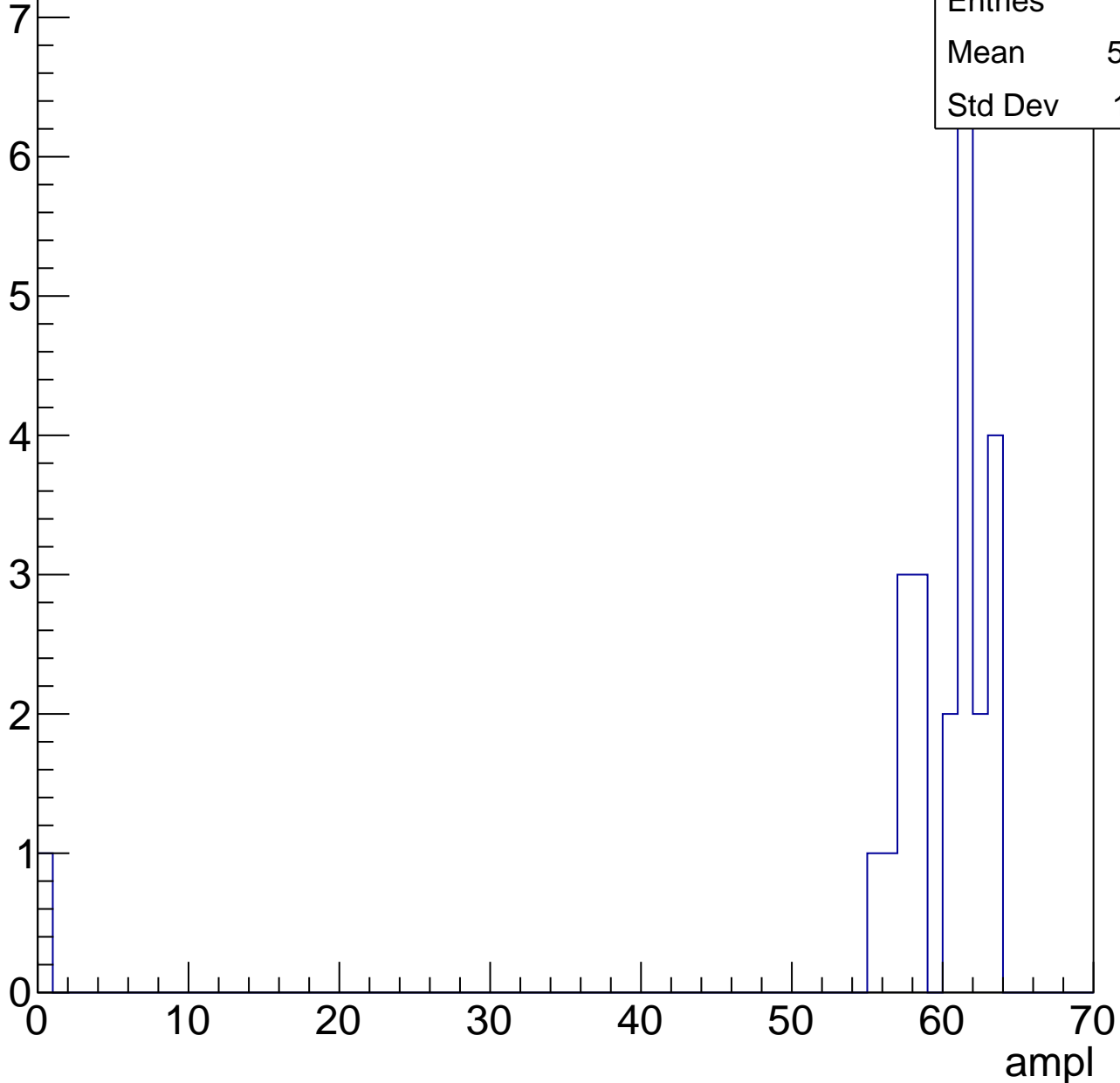


# B1L101S, U20-ch100, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	24
Mean	57.46
Std Dev	12.21

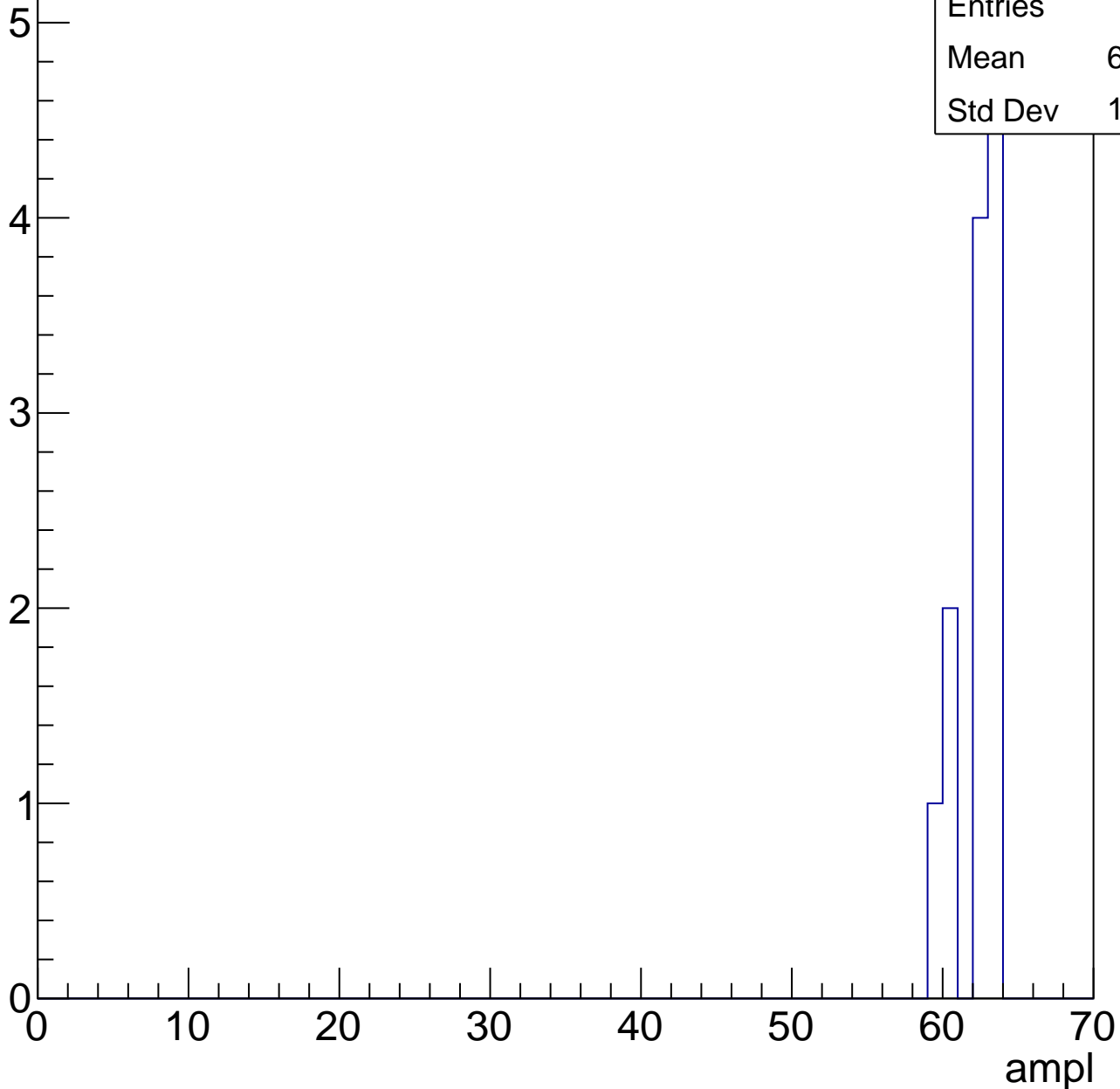


# B1L101S, U20-ch100, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	12
Mean	61.83
Std Dev	1.344





# B1L101S, U20-ch100, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U20-ch101, adc0

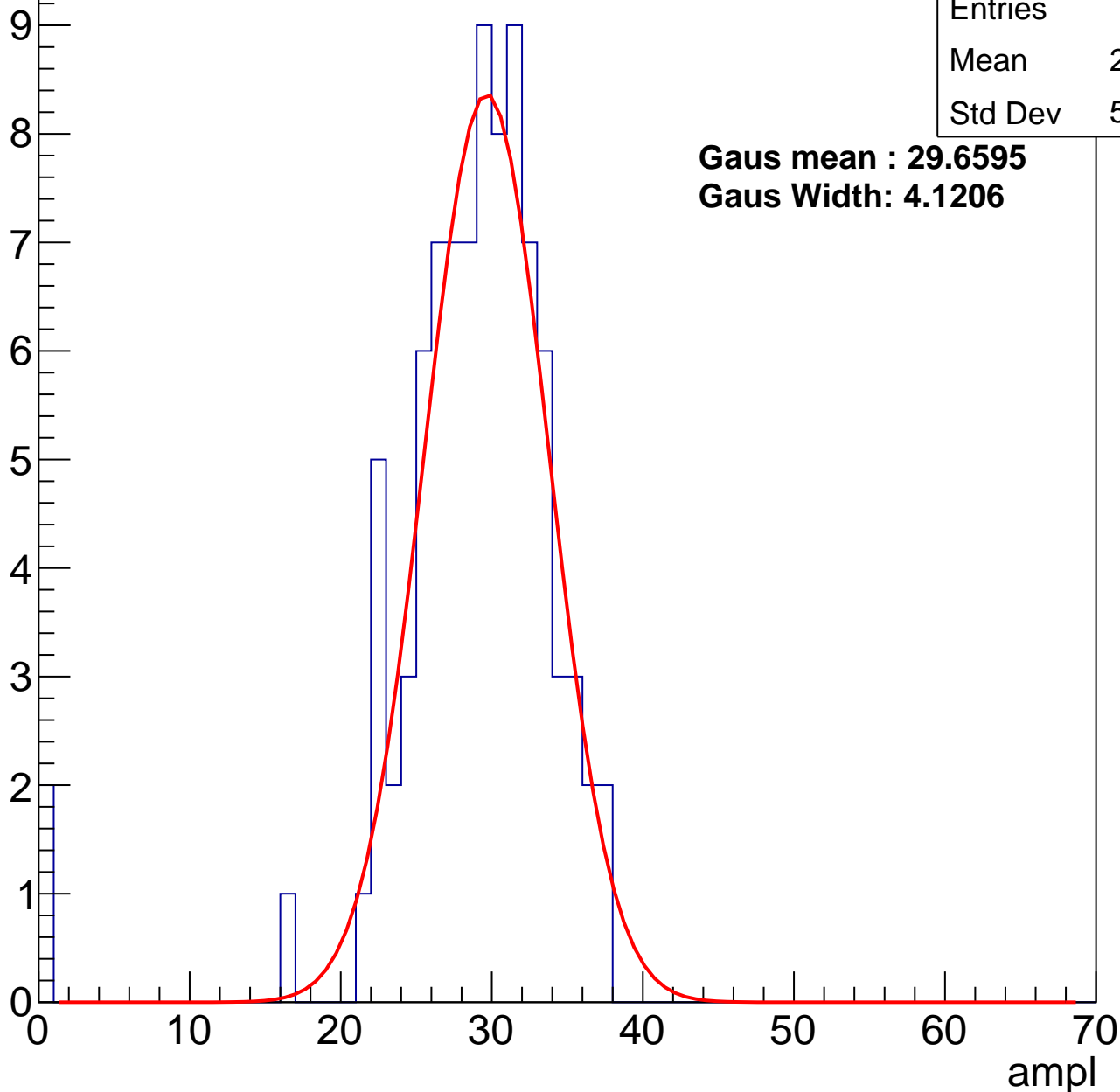
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	90
Mean	28.19
Std Dev	5.825

**Gaus mean : 29.6595**

**Gaus Width: 4.1206**



# B1L101S, U20-ch101, adc1

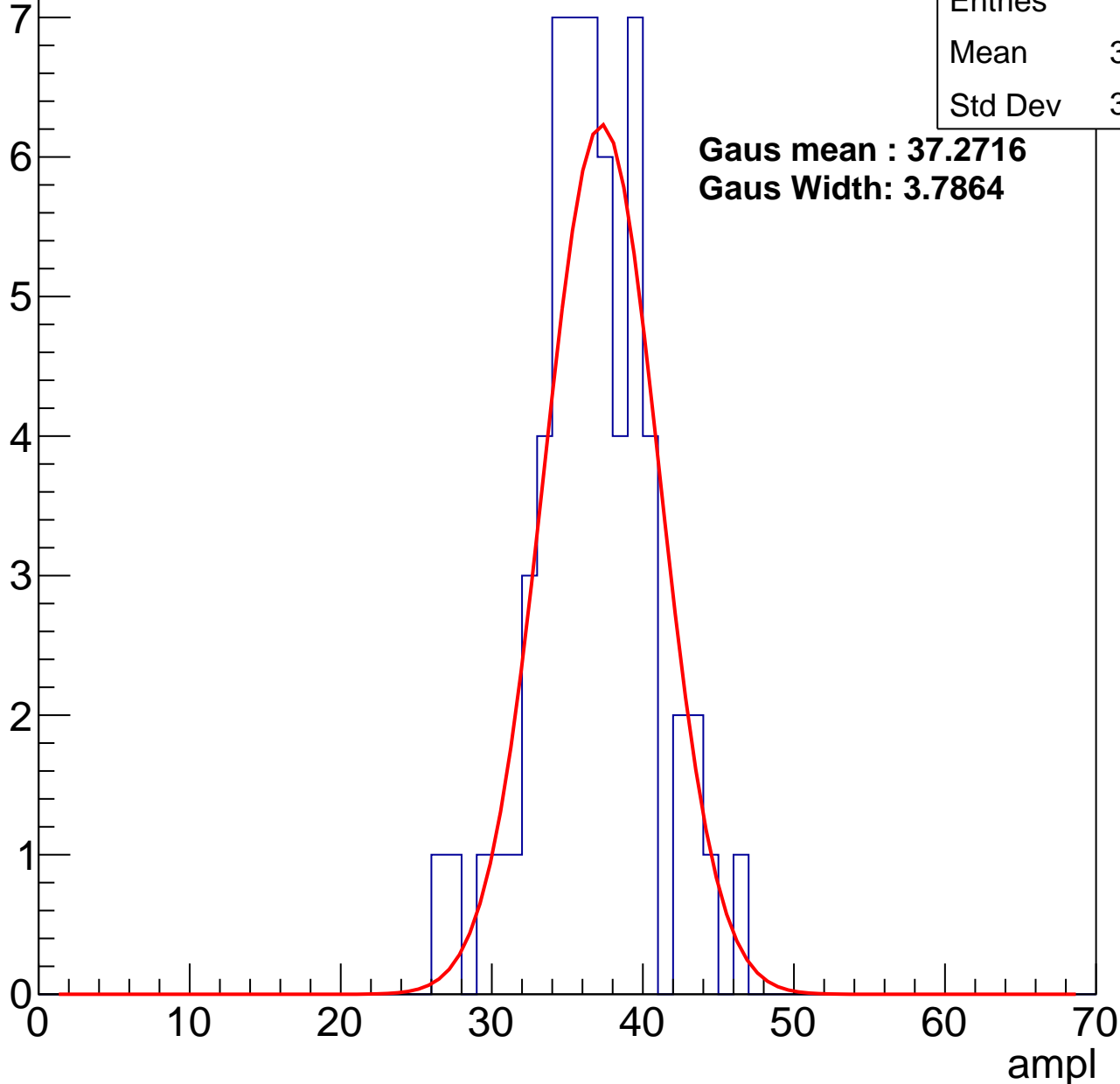
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	60
Mean	36.22
Std Dev	3.852

**Gaus mean : 37.2716**

**Gaus Width: 3.7864**



# B1L101S, U20-ch101, adc2

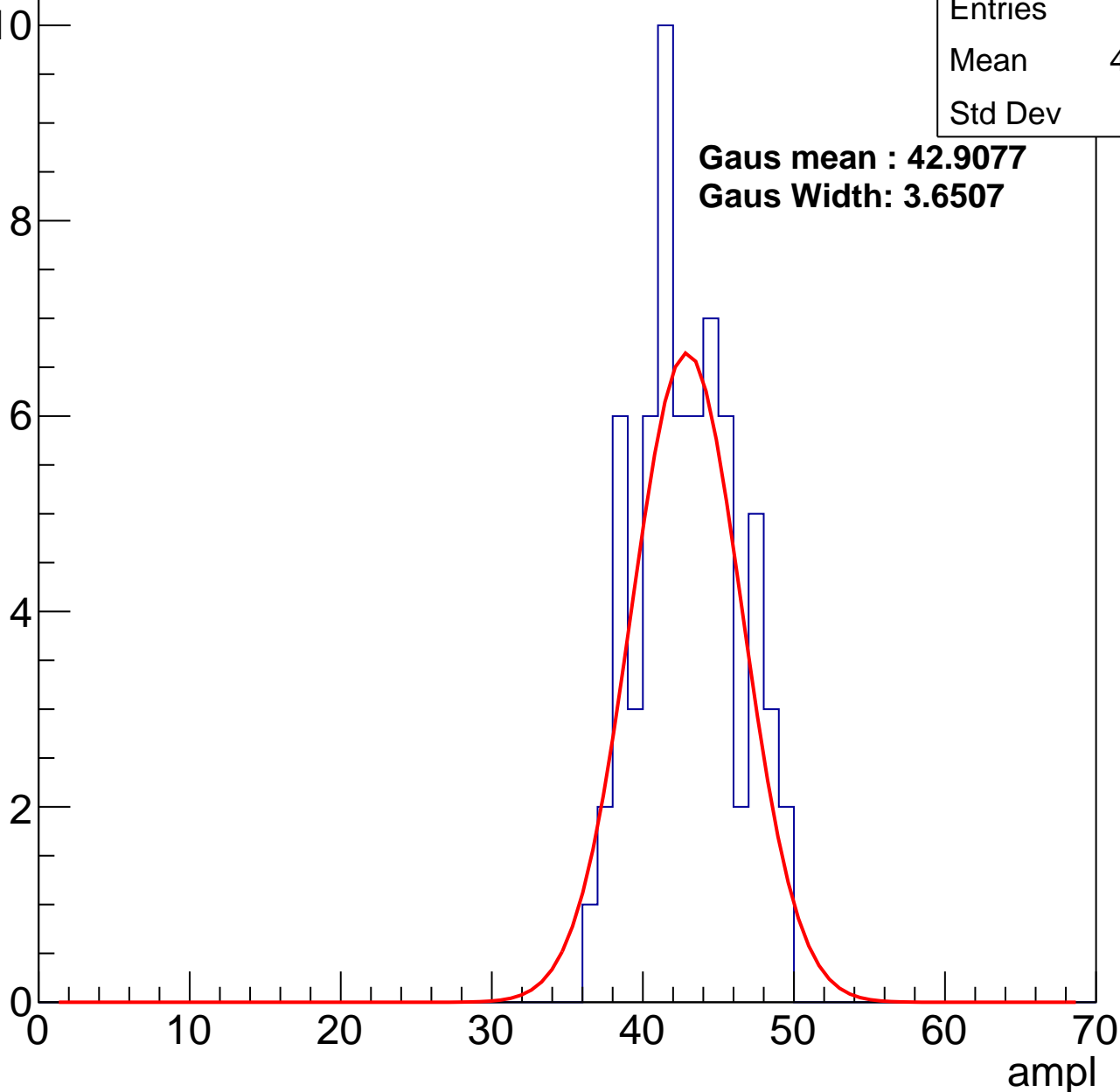
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	42.49
Std Dev	3.23

**Gaus mean : 42.9077**

**Gaus Width: 3.6507**

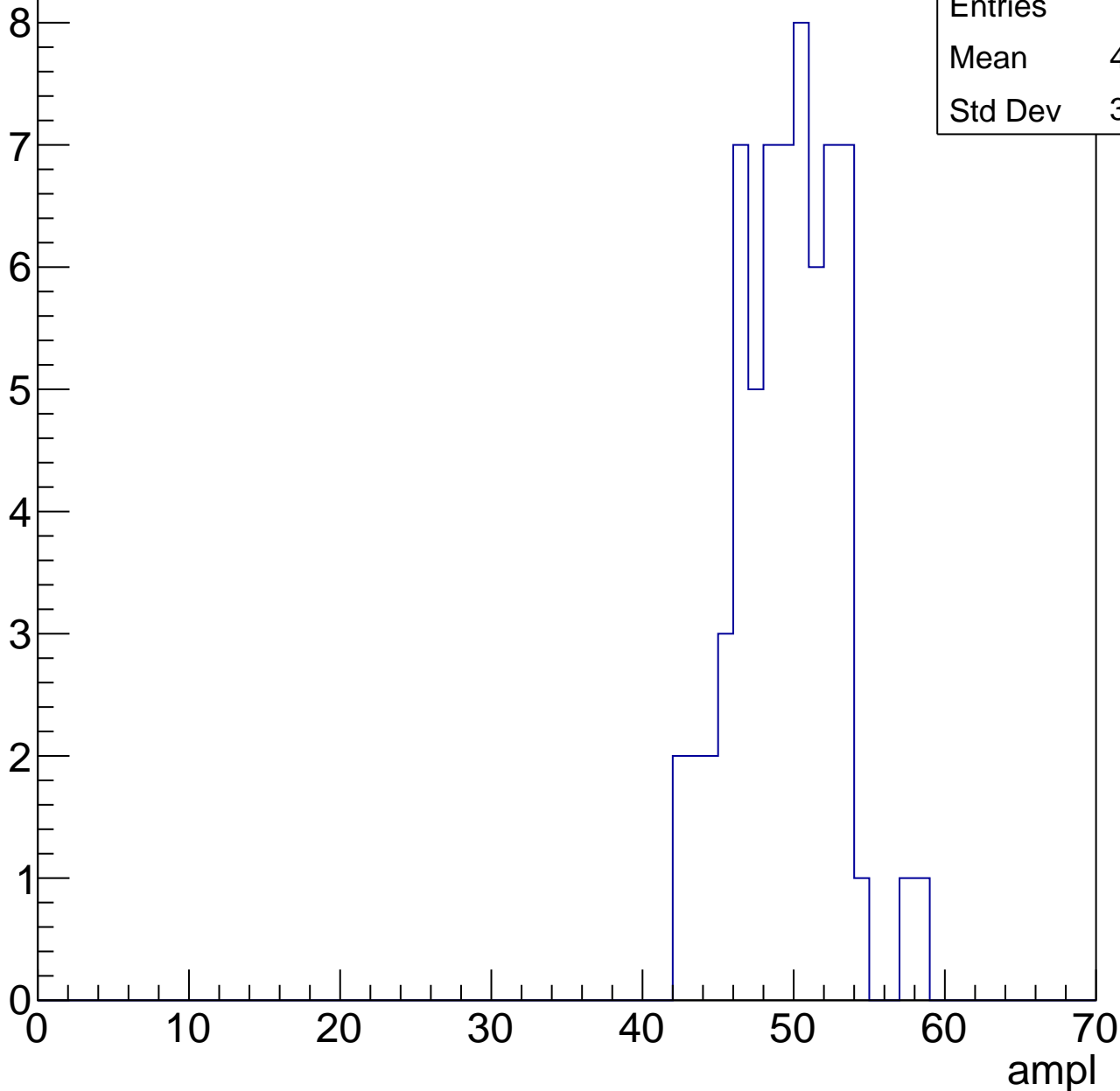


# B1L101S, U20-ch101, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	66
Mean	49.08
Std Dev	3.336

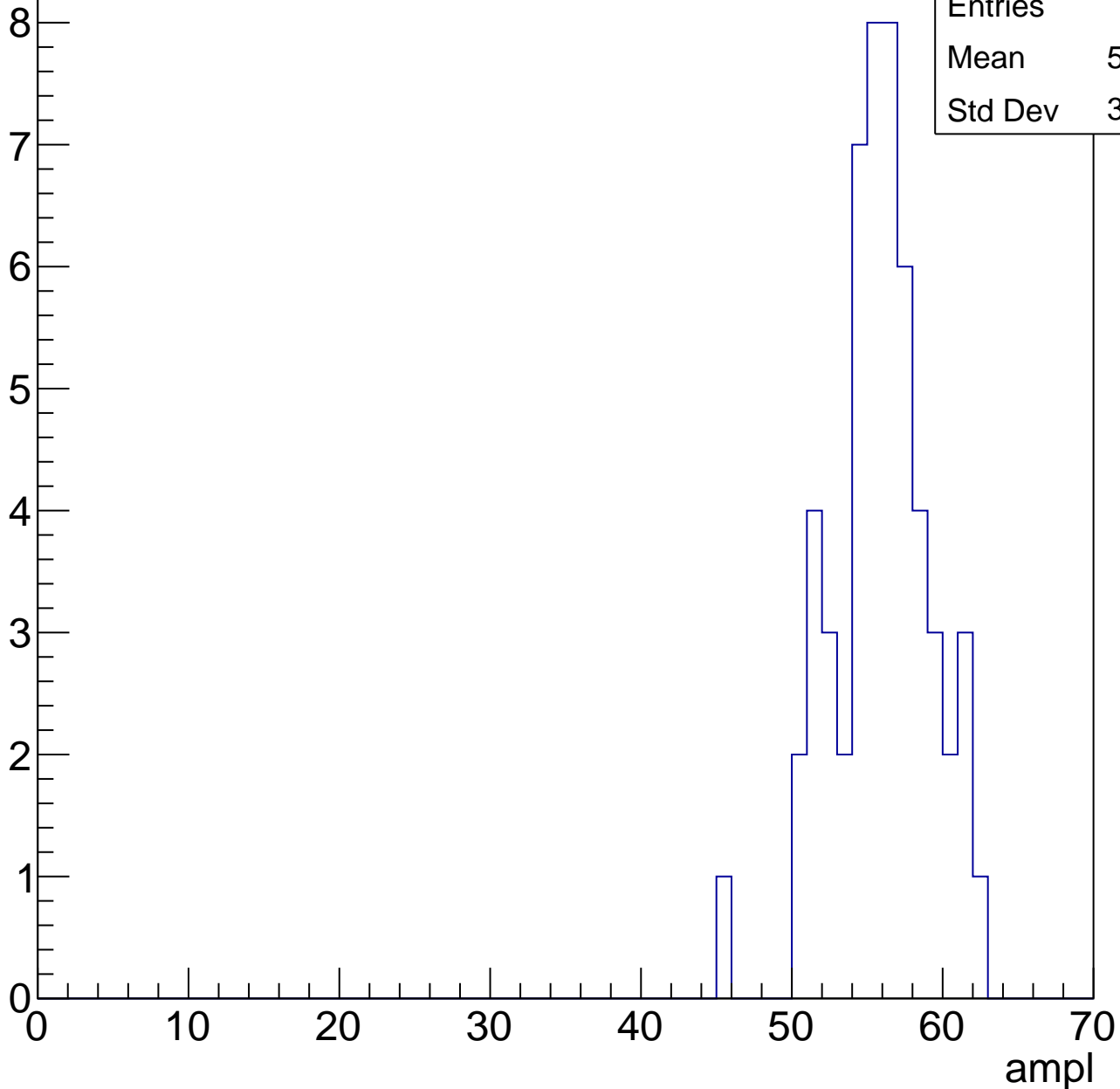


# B1L101S, U20-ch101, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	54
Mean	55.43
Std Dev	3.247

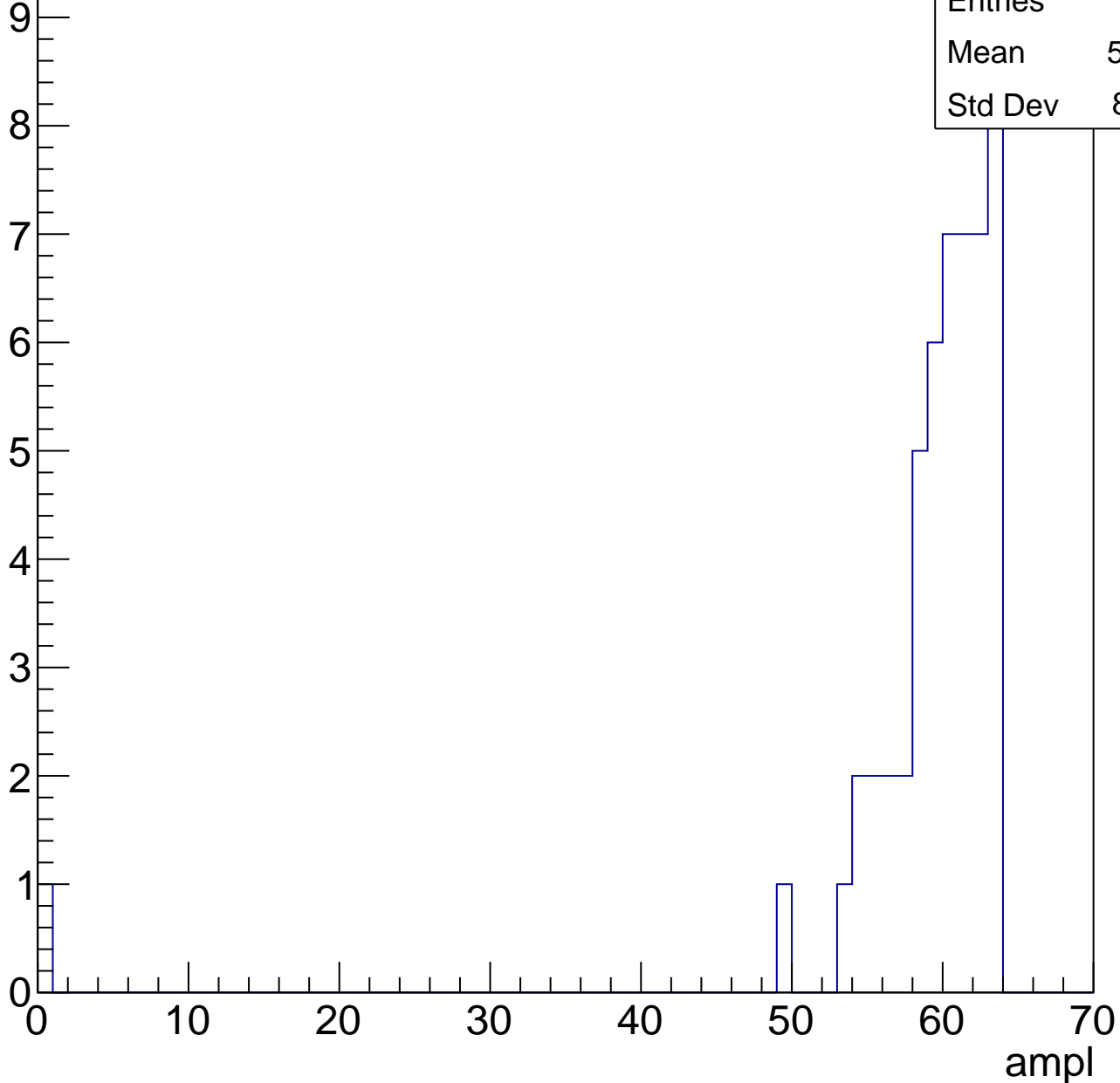


# B1L101S, U20-ch101, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	52
Mean	58.42
Std Dev	8.721



# B1L101S, U20-ch101, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

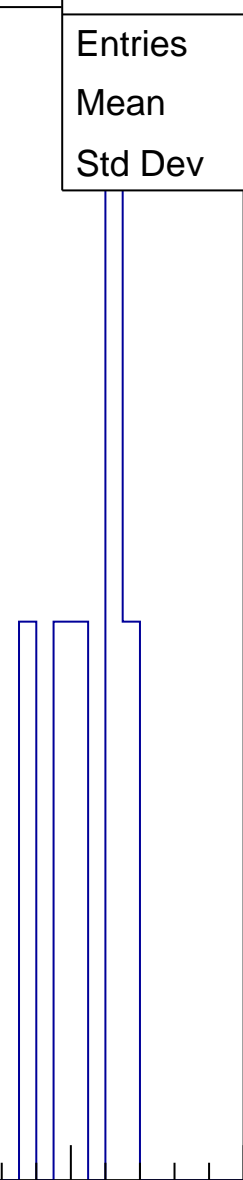
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	6
Mean	60.5
Std Dev	2.062

0 10 20 30 40 50 60 70

ampl





# B1L101S, U20-ch101, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U20-ch102, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	78
Mean	30.06
Std Dev	4.834

**Gaus mean : 31.1831**

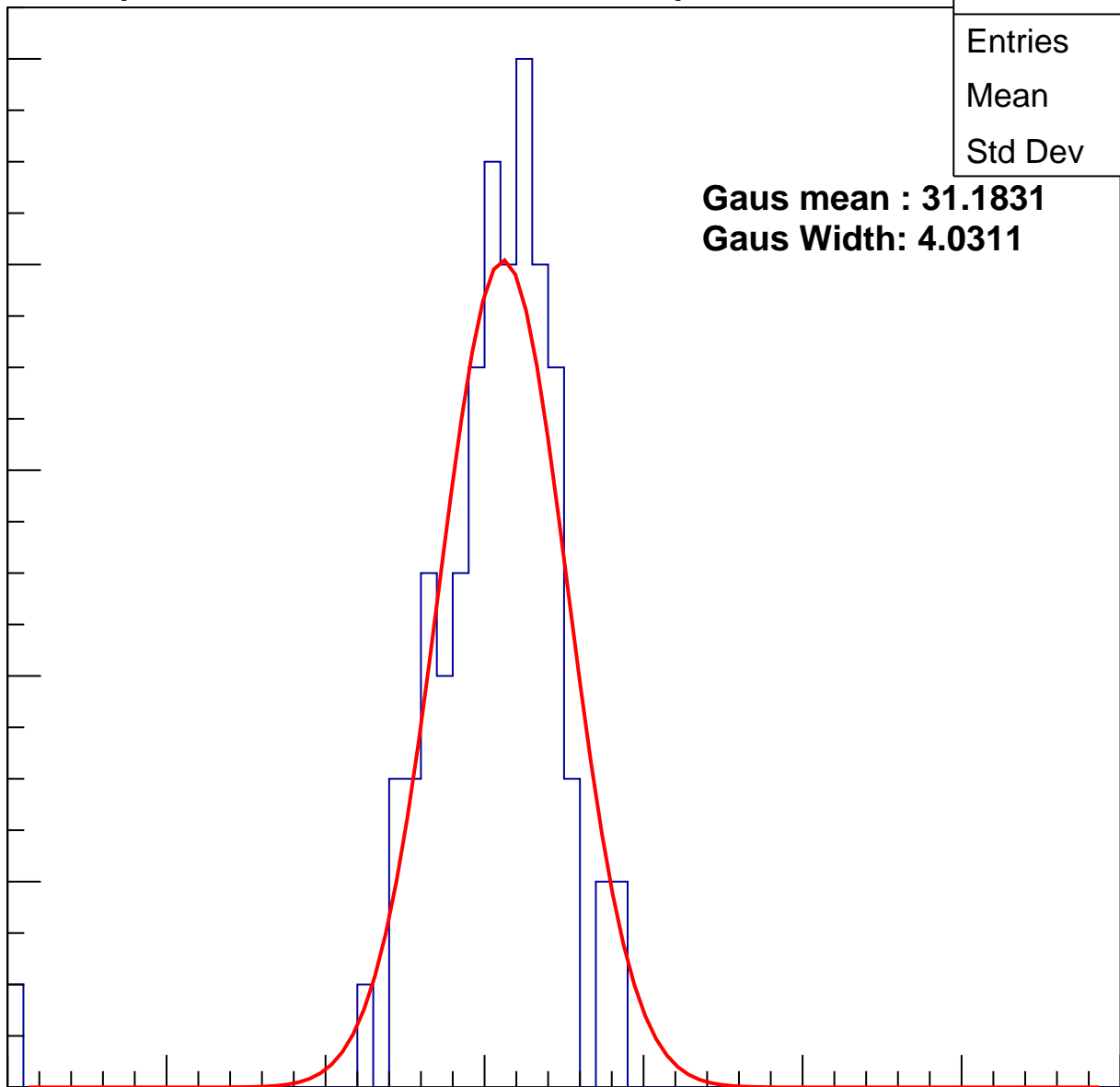
**Gaus Width: 4.0311**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U20-ch102, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	65
Mean	38.15
Std Dev	3.492

**Gaus mean : 38.7742**

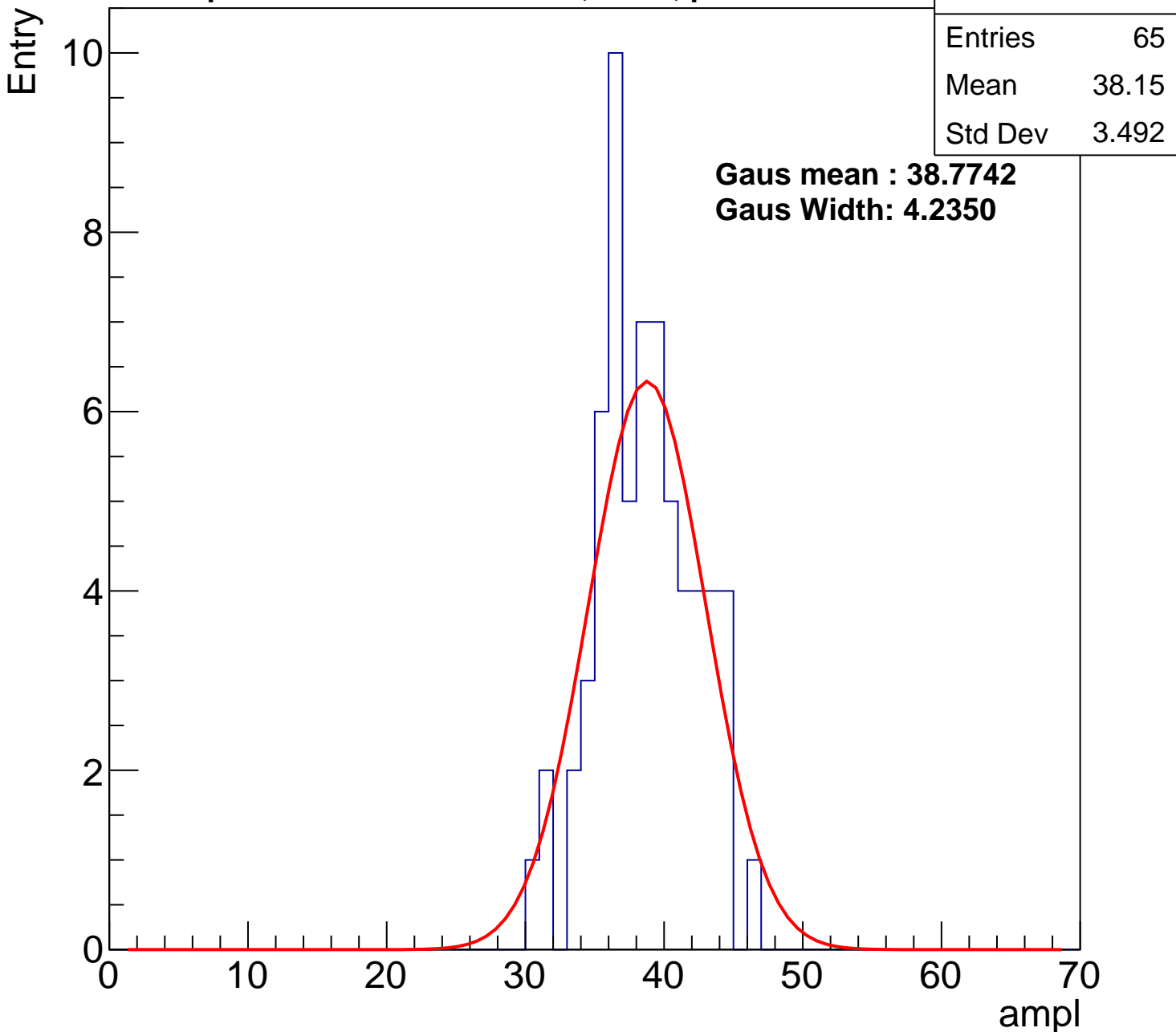
**Gaus Width: 4.2350**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B1L101S, U20-ch102, adc2

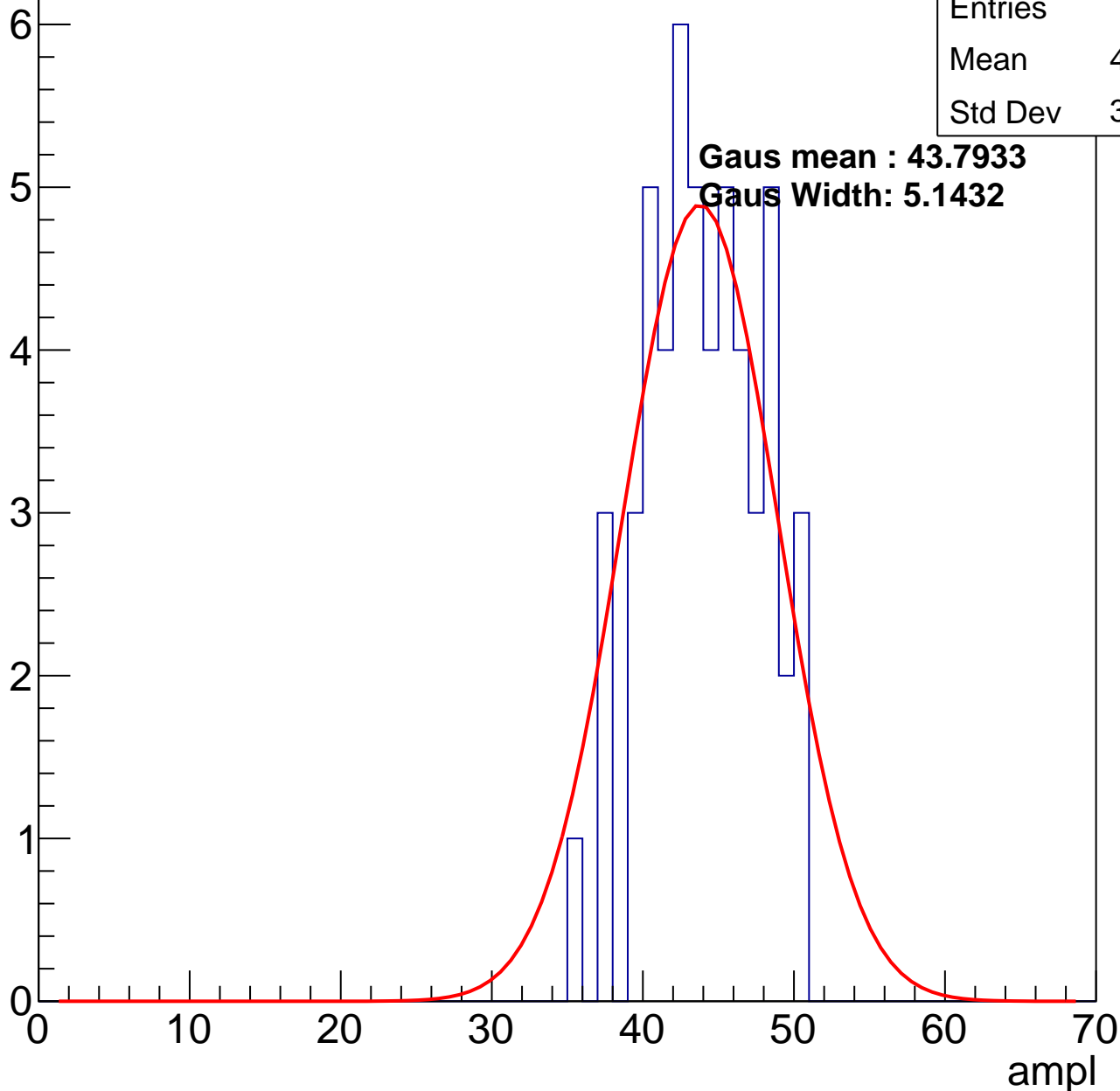
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	53
Mean	43.55
Std Dev	3.694

**Gaus mean : 43.7933**

**Gaus Width: 5.1432**



# B1L101S, U20-ch102, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

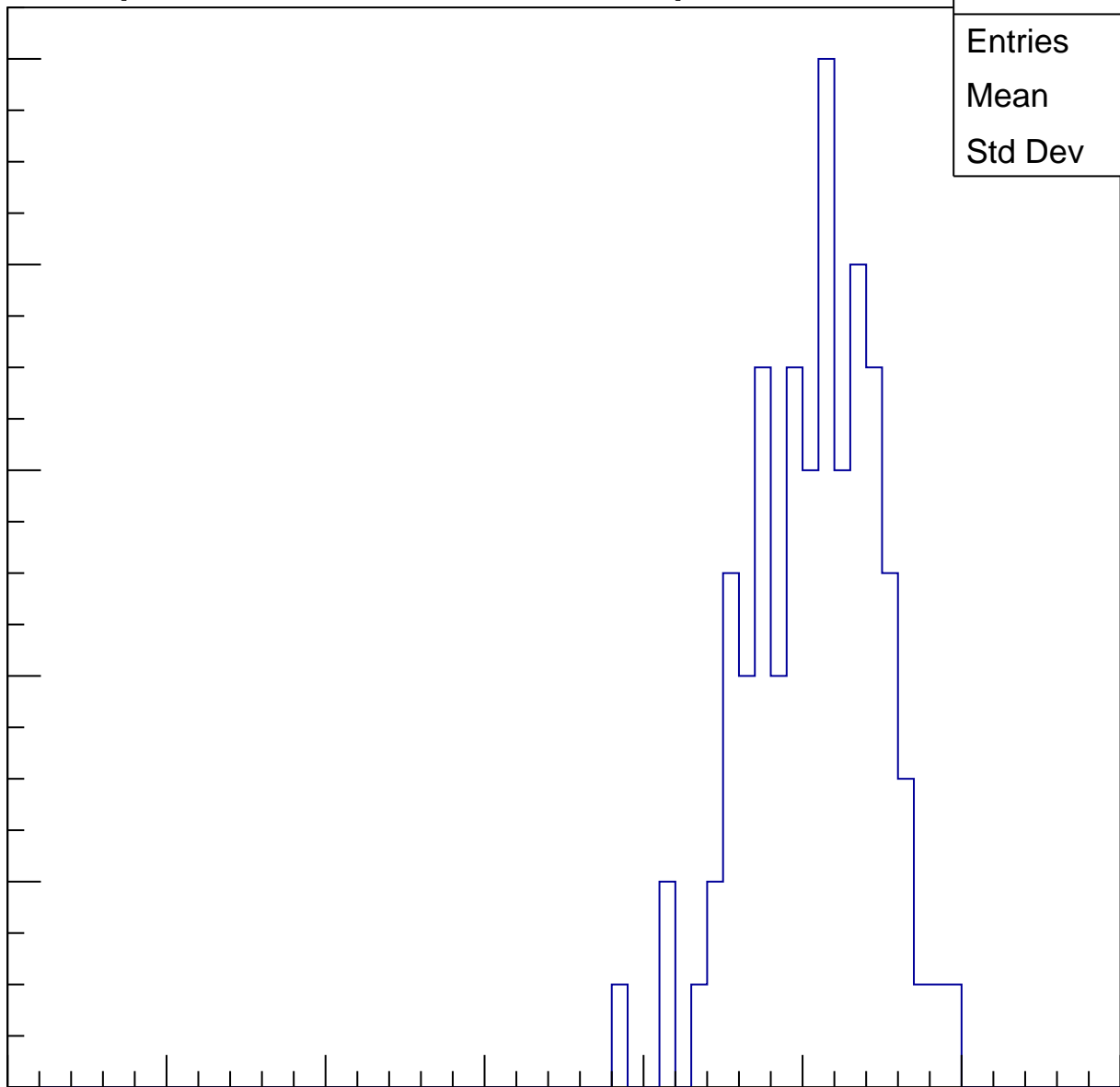
Entries	81
Mean	50.19
Std Dev	4.074

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

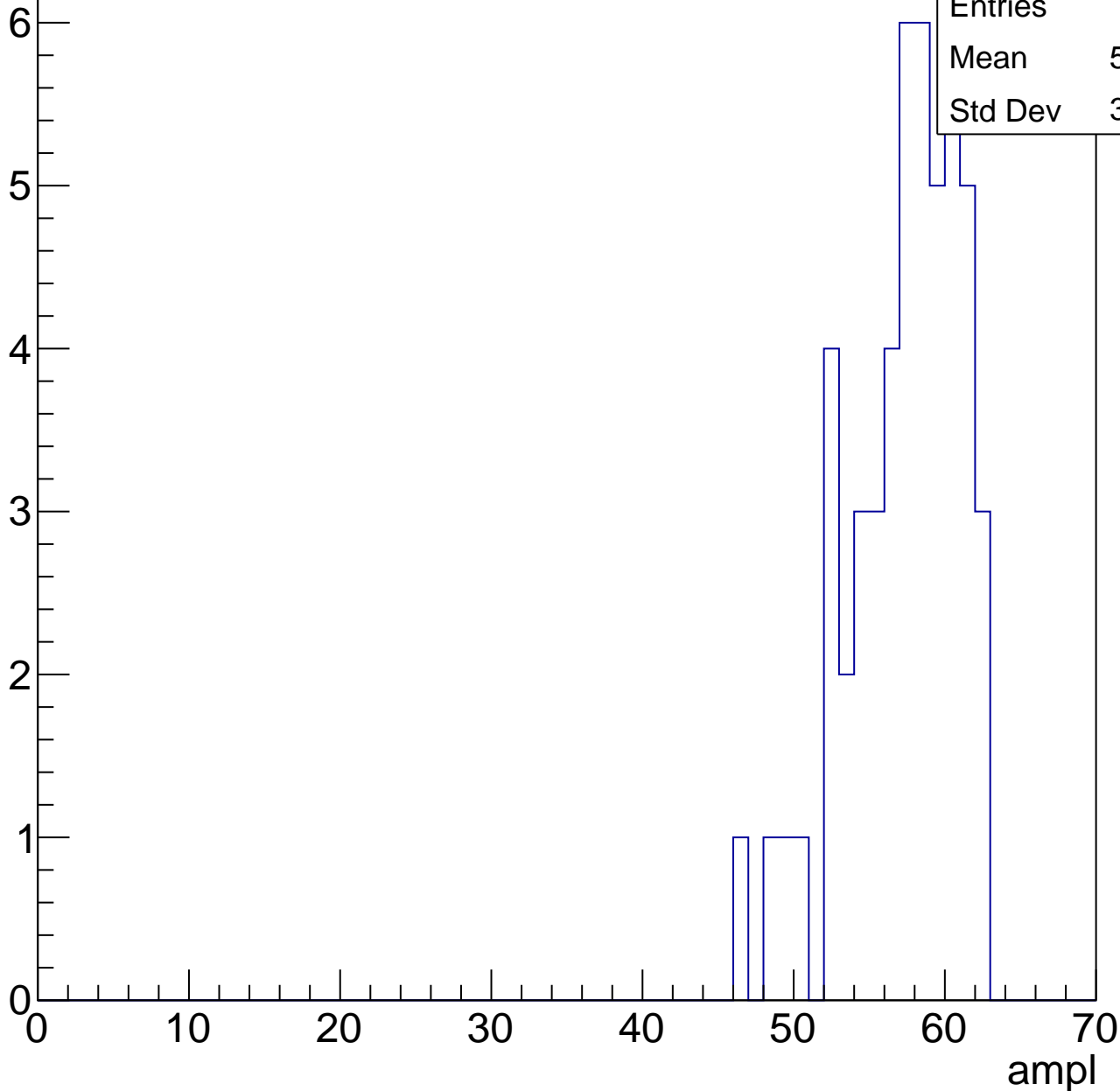


# B1L101S, U20-ch102, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	51
Mean	56.75
Std Dev	3.762

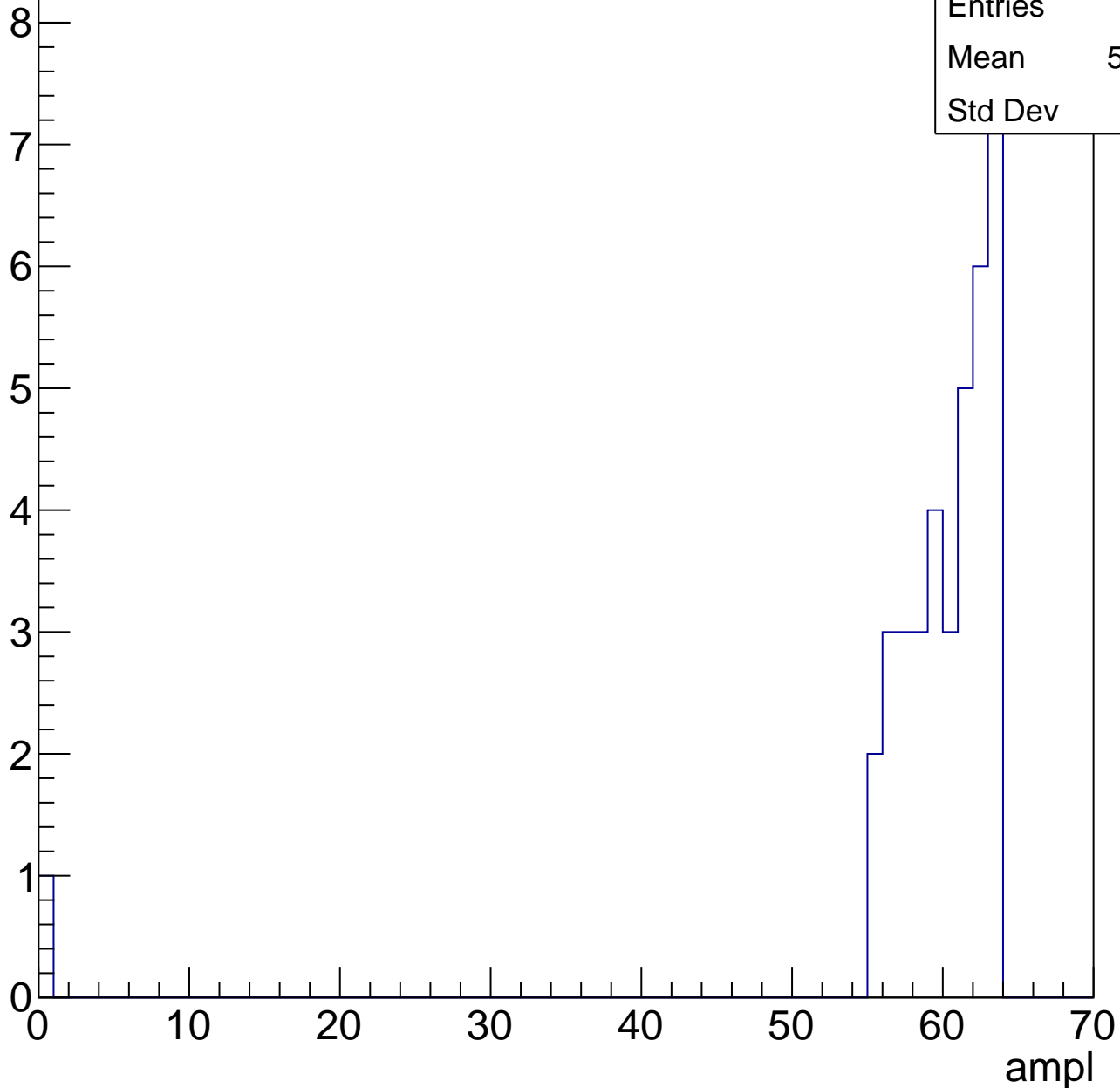


# B1L101S, U20-ch102, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	38
Mean	58.42
Std Dev	9.93



# B1L101S, U20-ch102, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

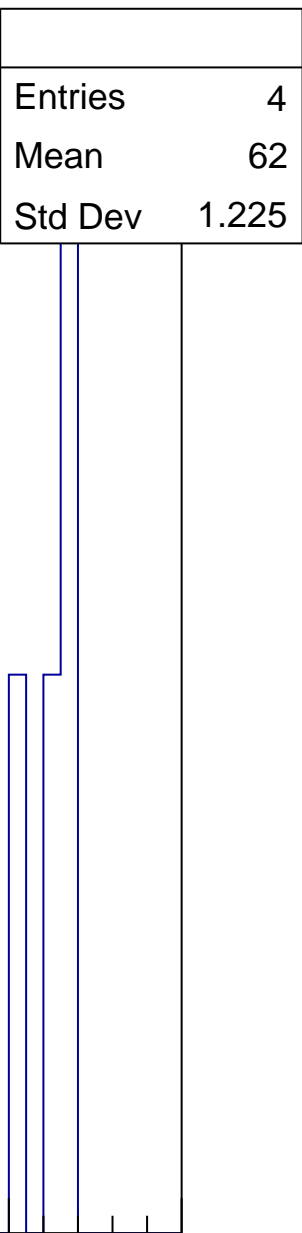
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	4
Mean	62
Std Dev	1.225

0 10 20 30 40 50 60 70

ampl





# B1L101S, U20-ch102, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U20-ch103, adc0

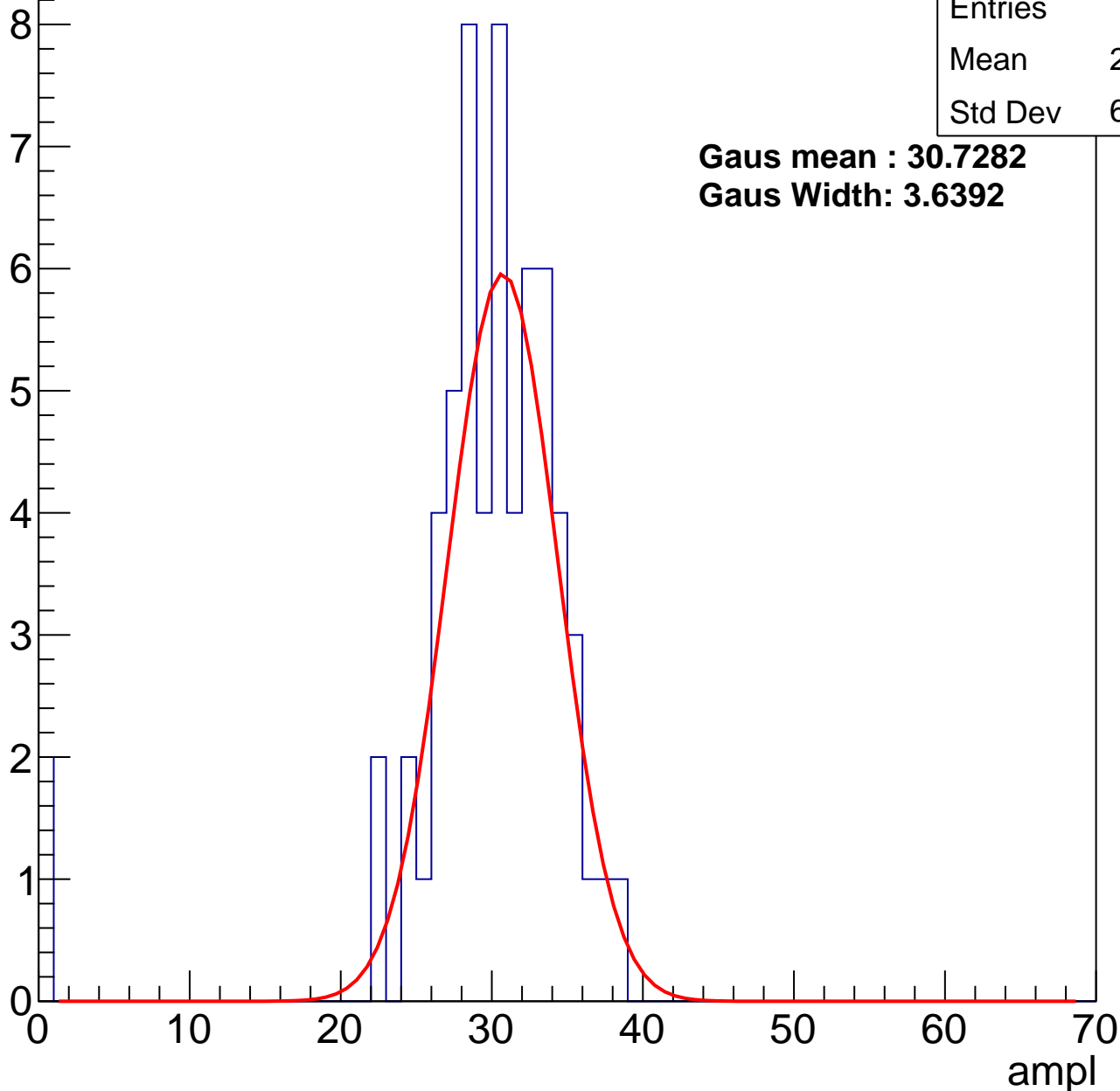
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	29.06
Std Dev	6.332

**Gaus mean : 30.7282**

**Gaus Width: 3.6392**



# B1L101S, U20-ch103, adc1

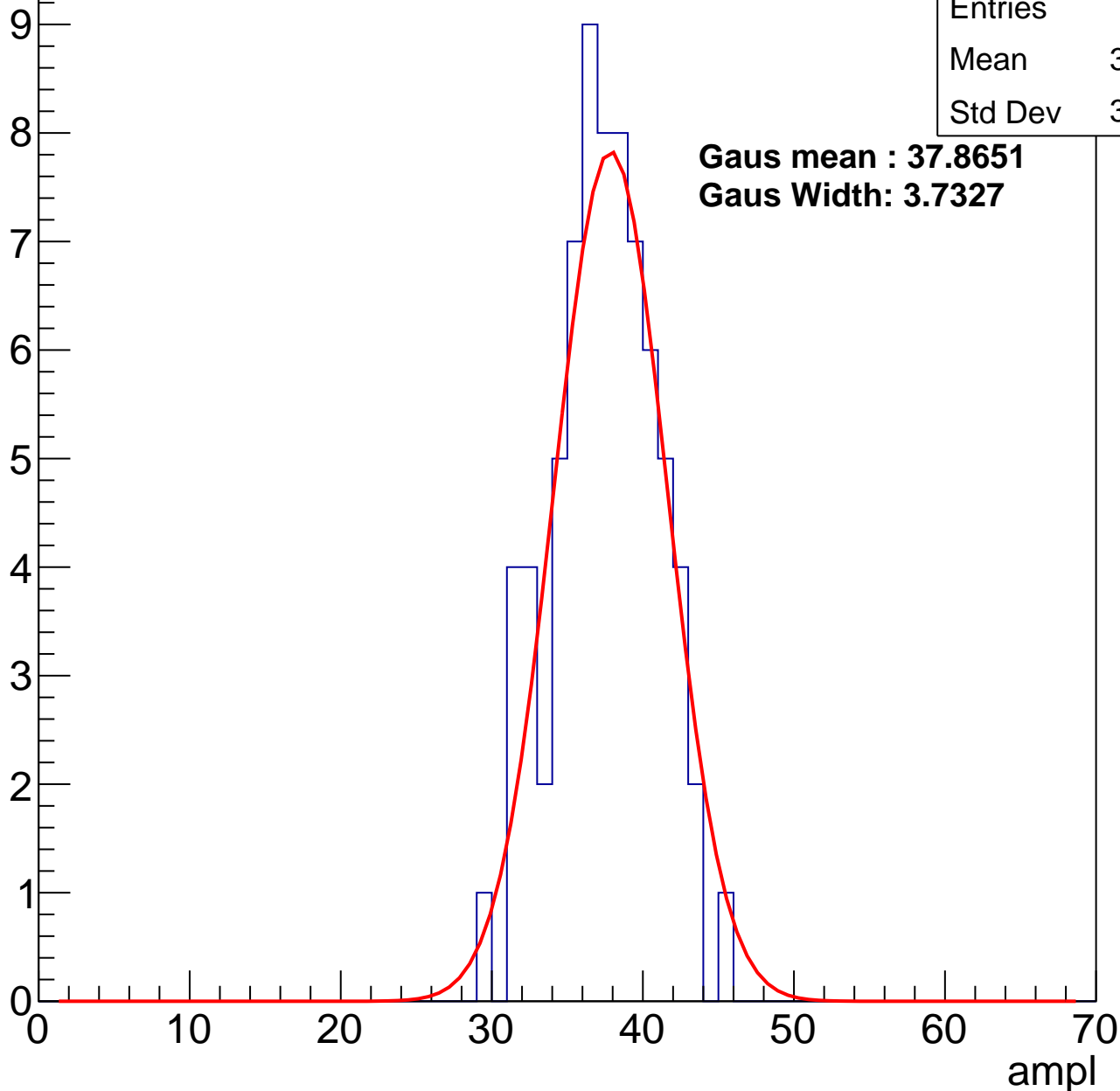
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	73
Mean	37.03
Std Dev	3.368

**Gaus mean : 37.8651**

**Gaus Width: 3.7327**



# B1L101S, U20-ch103, adc2

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	72
Mean	44.61
Std Dev	3.747

**Gaus mean : 45.1236**

**Gaus Width: 4.0100**

Entry

10

8

6

4

2

0

0

10

20

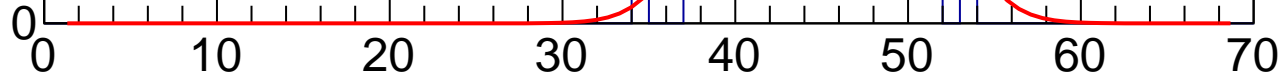
30

40

50

60

ampl



# B1L101S, U20-ch103, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

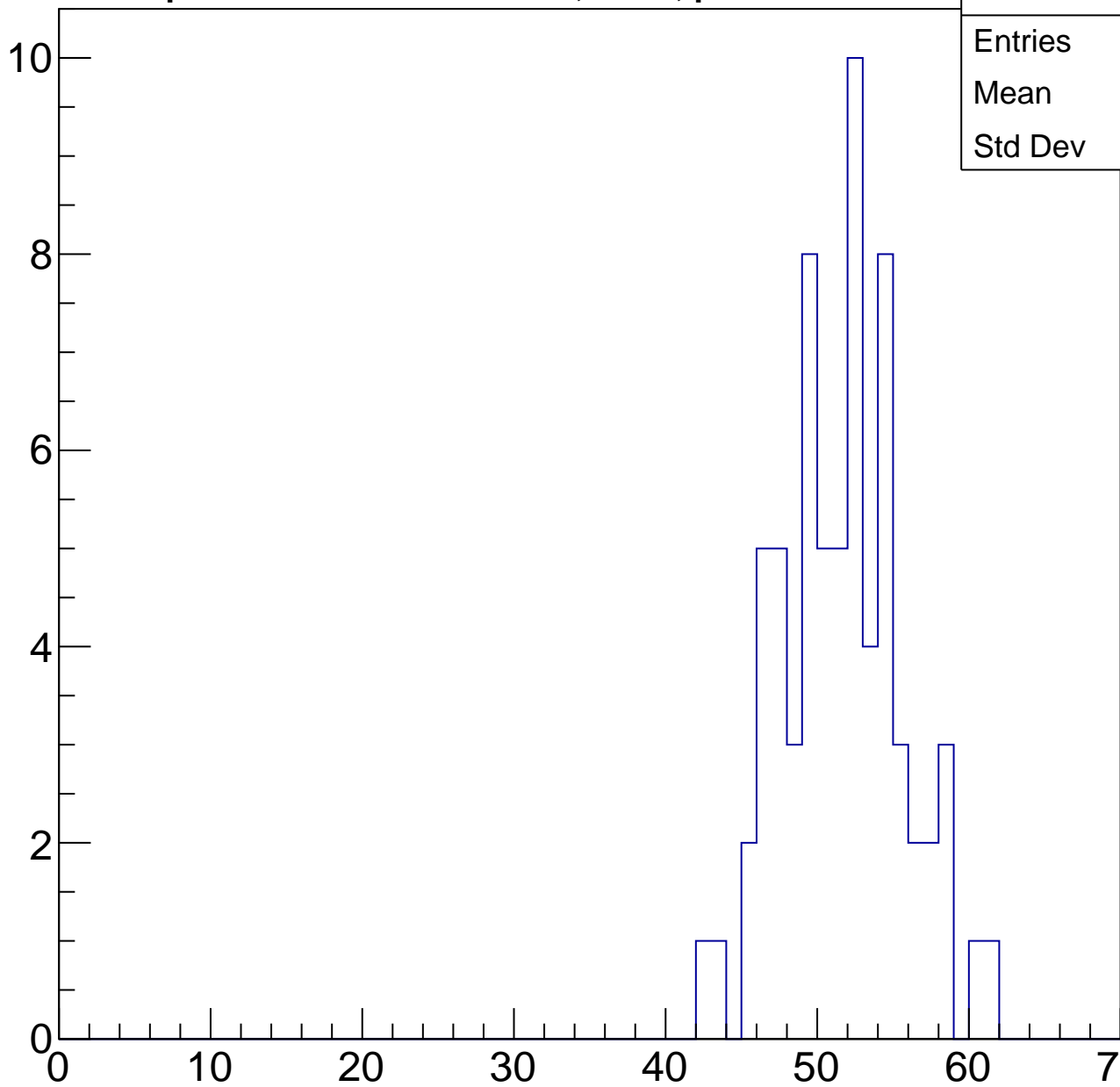
Entries	69
Mean	51.17
Std Dev	3.956

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

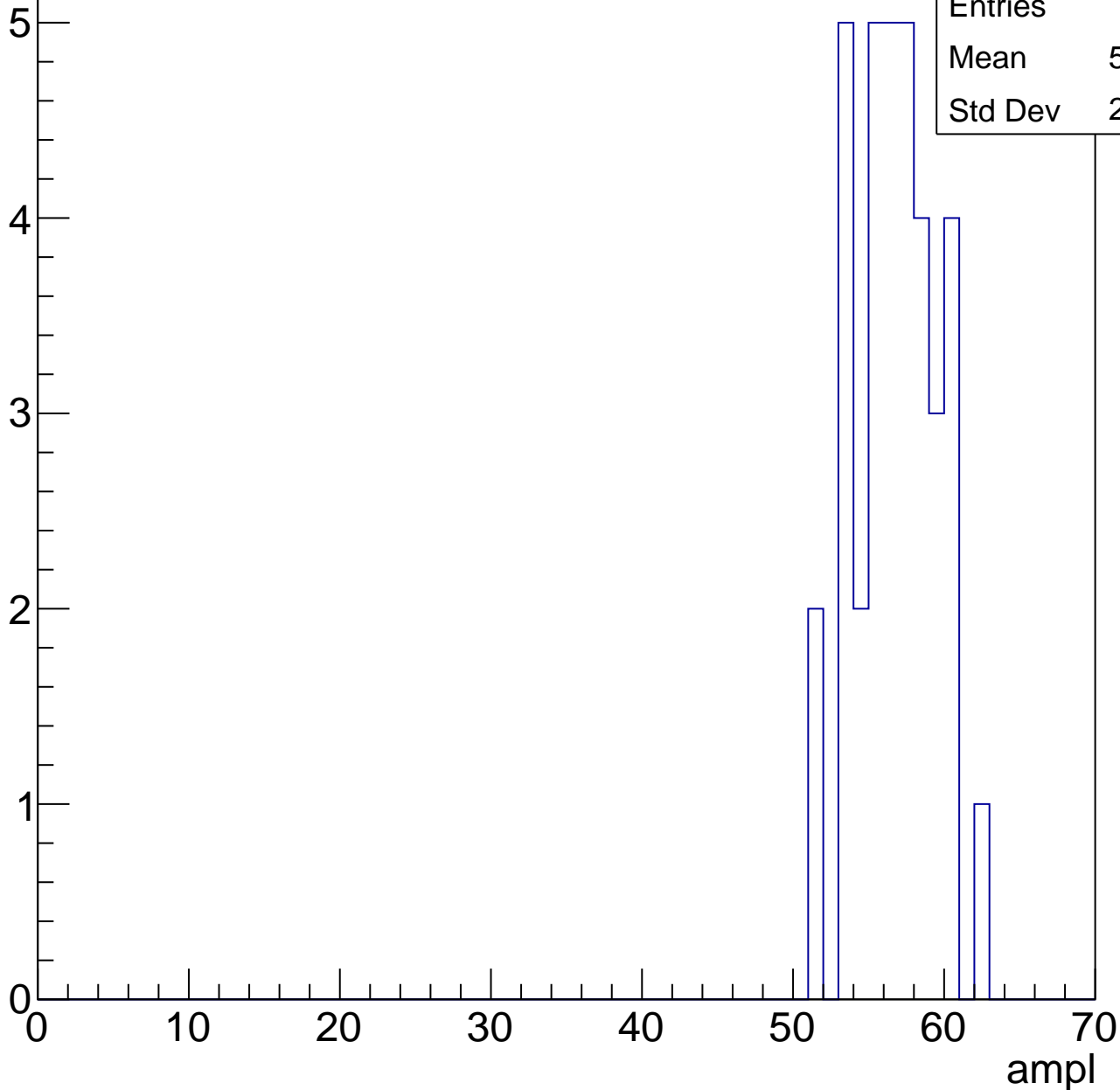


# B1L101S, U20-ch103, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	36
Mean	56.28
Std Dev	2.652

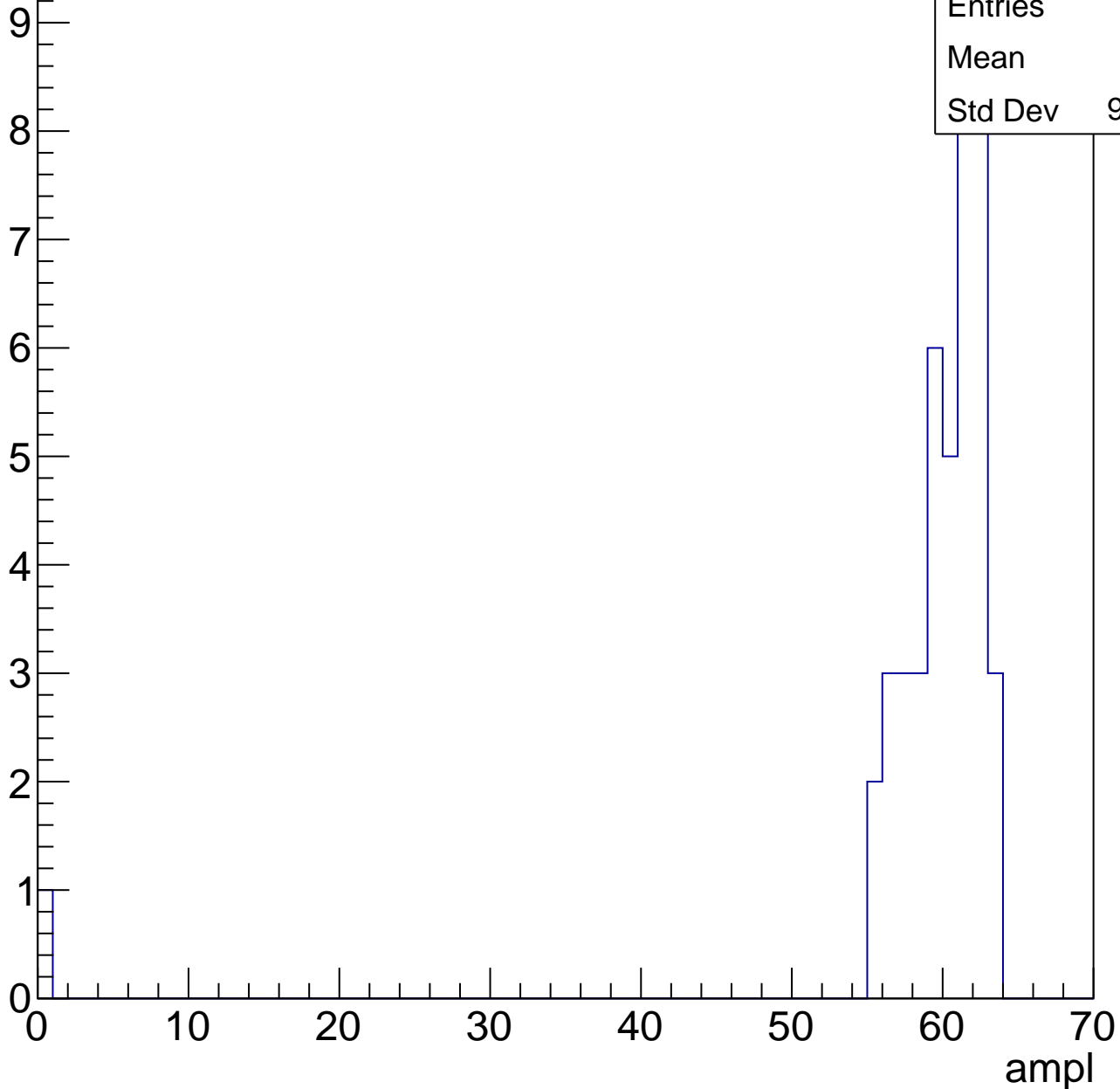


# B1L101S, U20-ch103, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	43
Mean	58.4
Std Dev	9.276

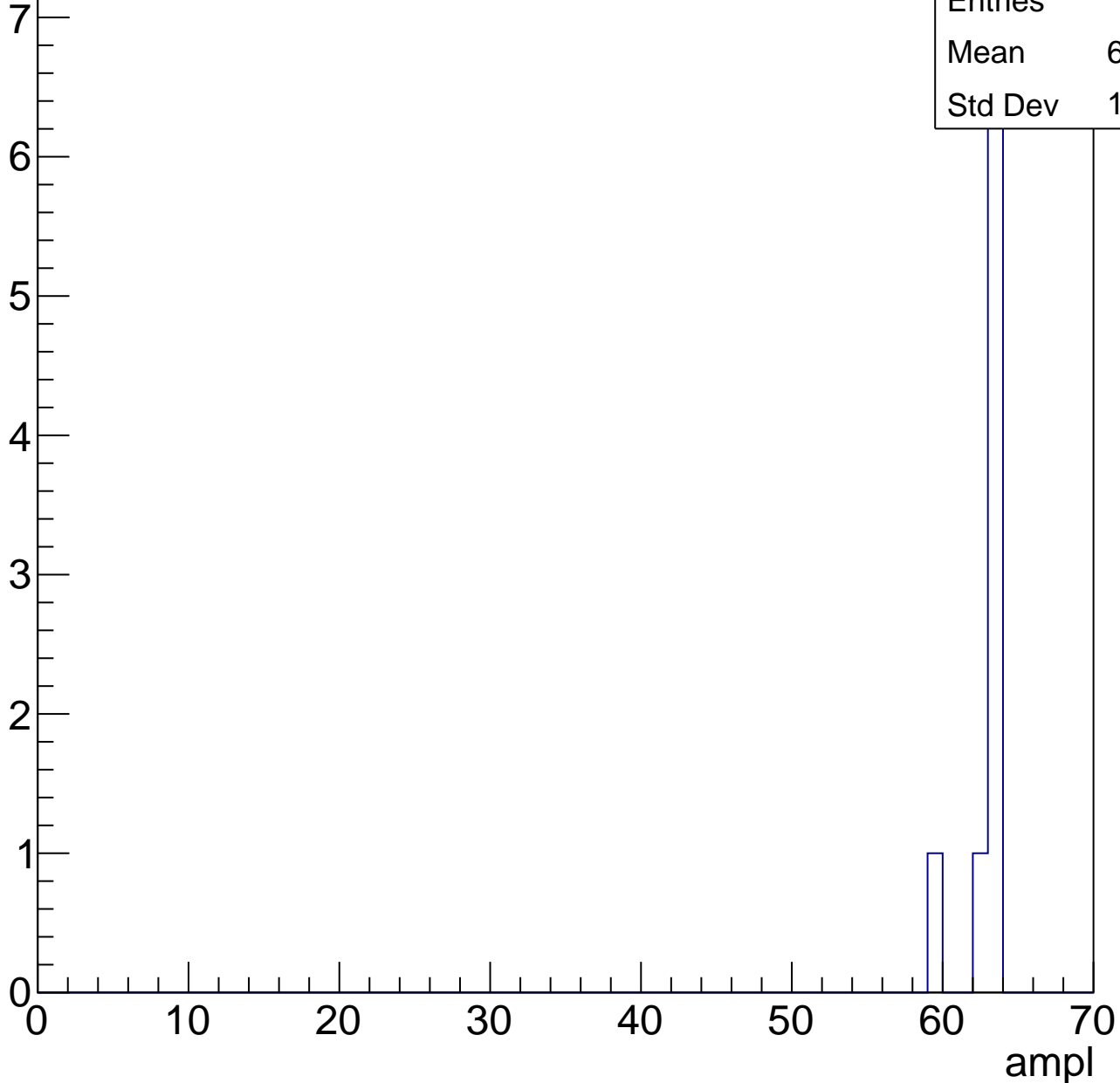


# B1L101S, U20-ch103, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	9
Mean	62.44
Std Dev	1.257





# B1L101S, U20-ch103, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L101S, U20-ch104, adc0

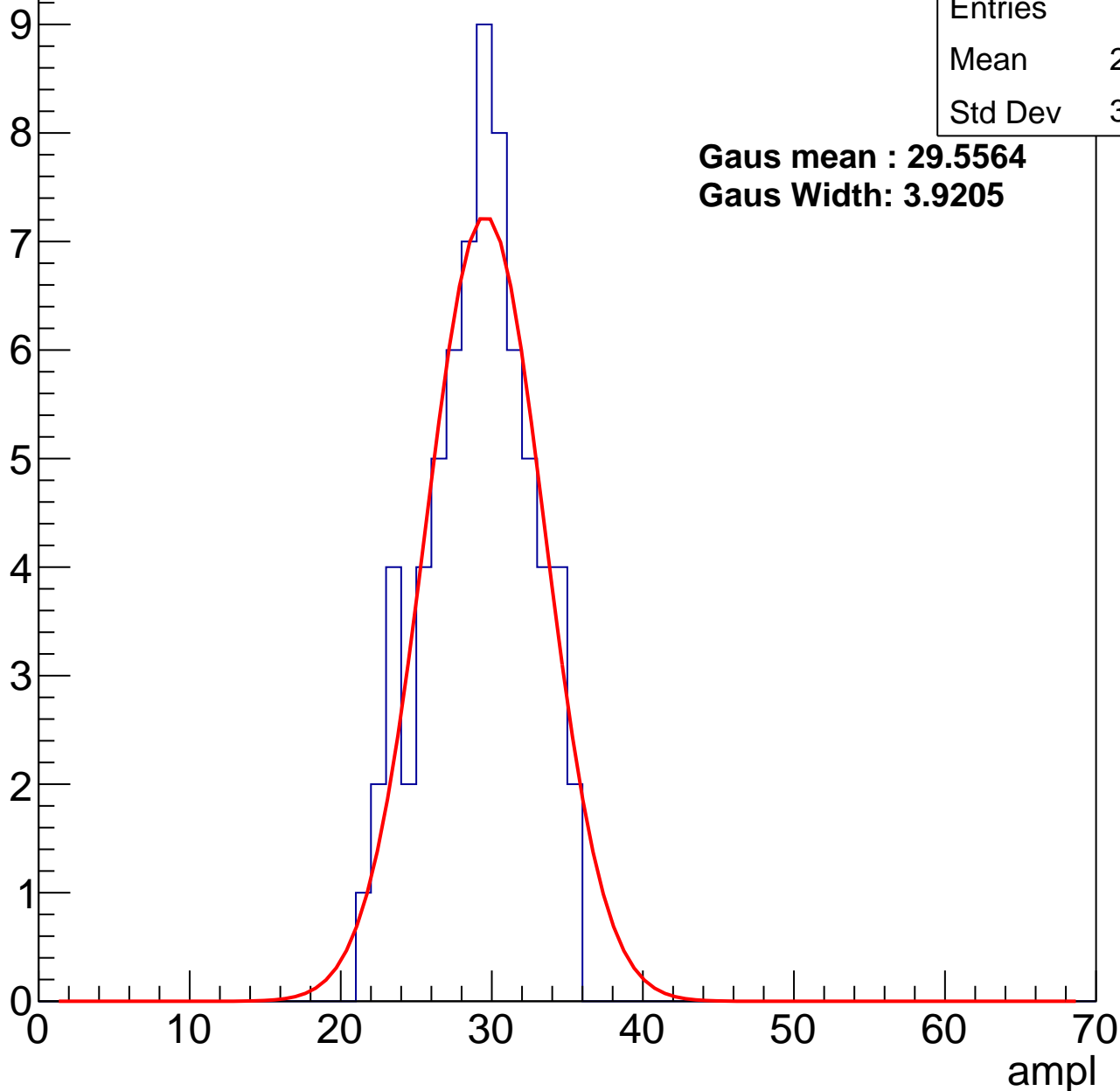
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	28.67
Std Dev	3.408

**Gaus mean : 29.5564**

**Gaus Width: 3.9205**



# B1L101S, U20-ch104, adc1

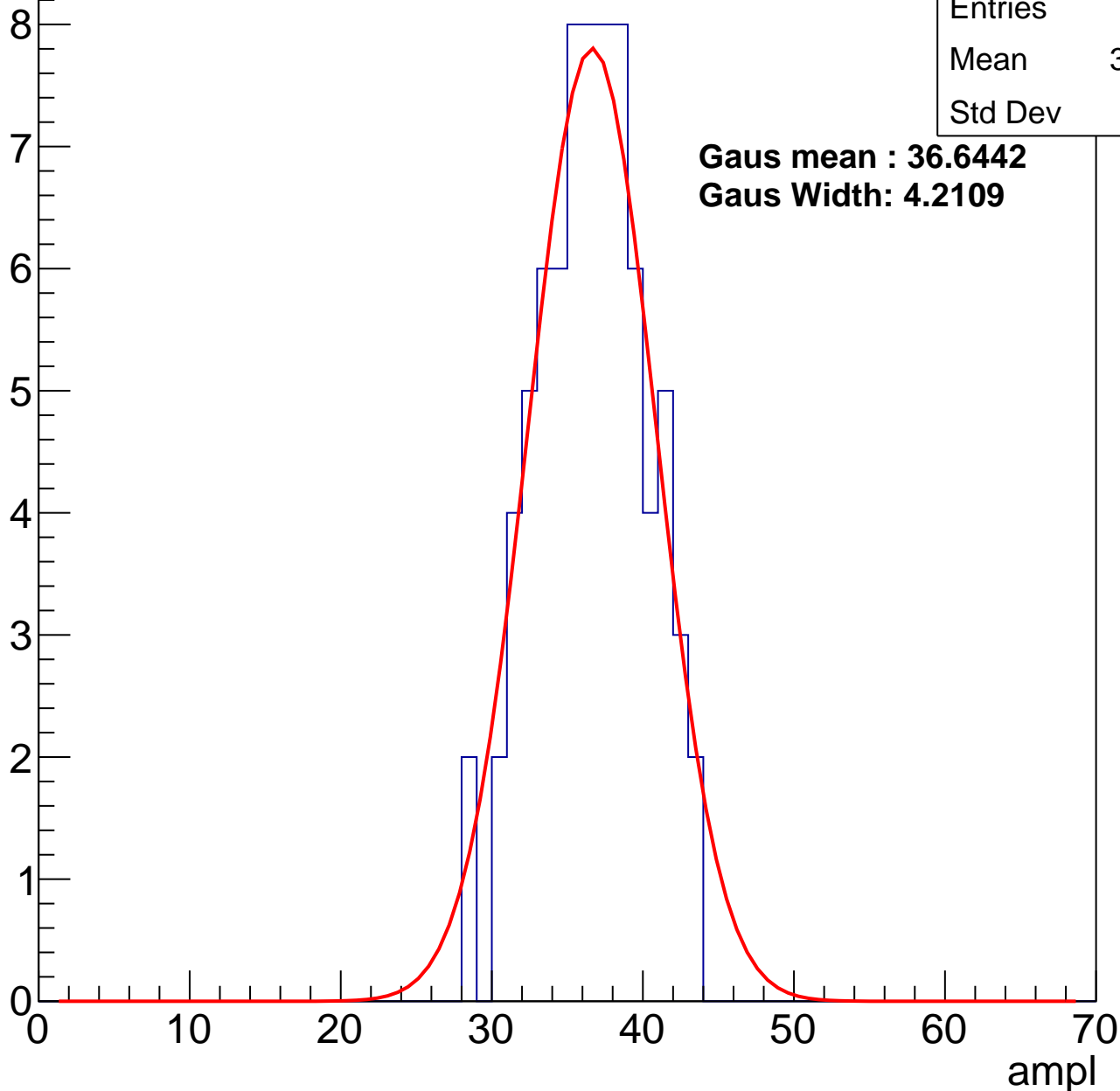
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	77
Mean	36.12
Std Dev	3.52

**Gaus mean : 36.6442**

**Gaus Width: 4.2109**



# B1L101S, U20-ch104, adc2

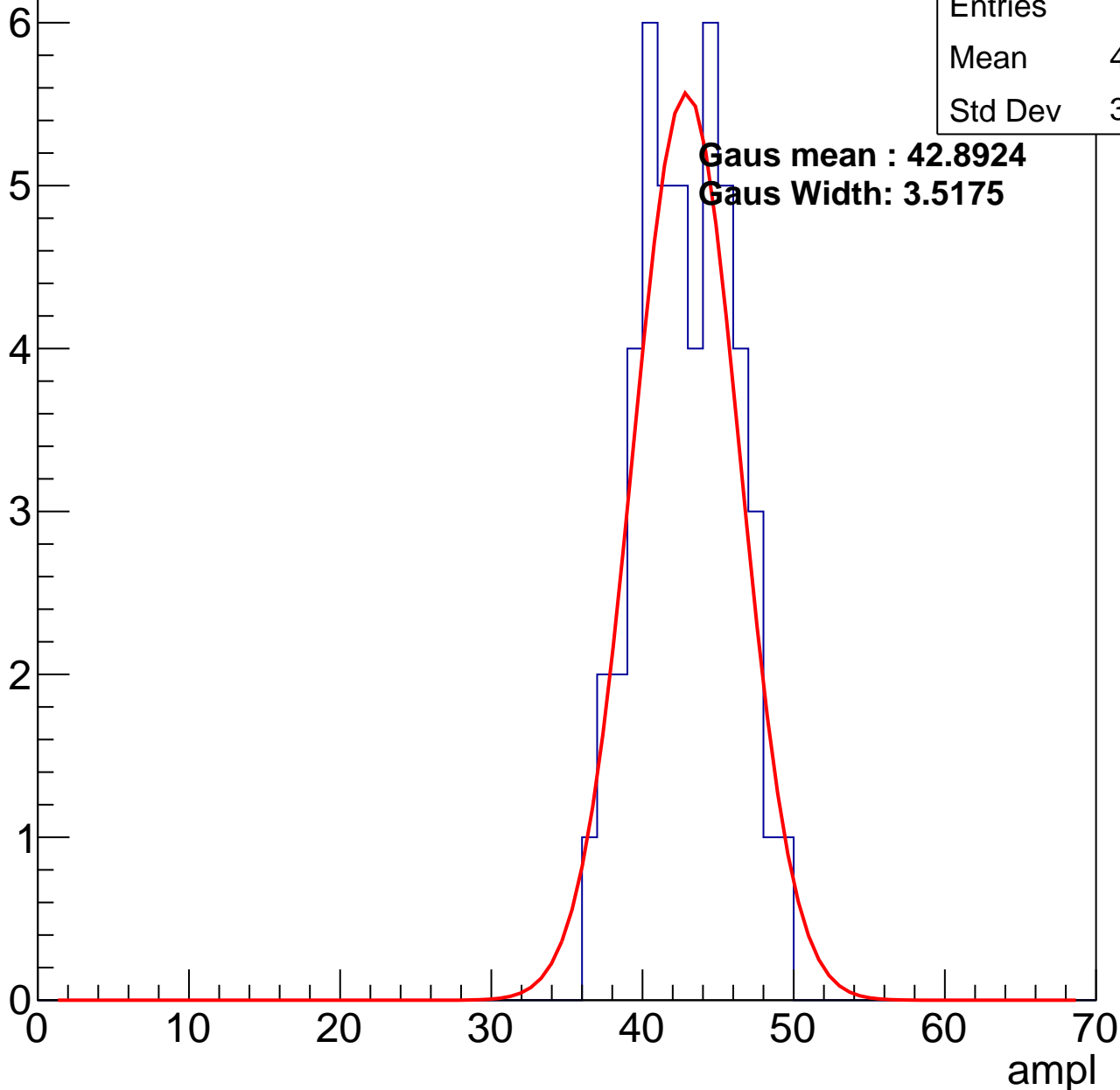
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	49
Mean	42.45
Std Dev	3.097

**Gaus mean : 42.8924**

**Gaus Width: 3.5175**

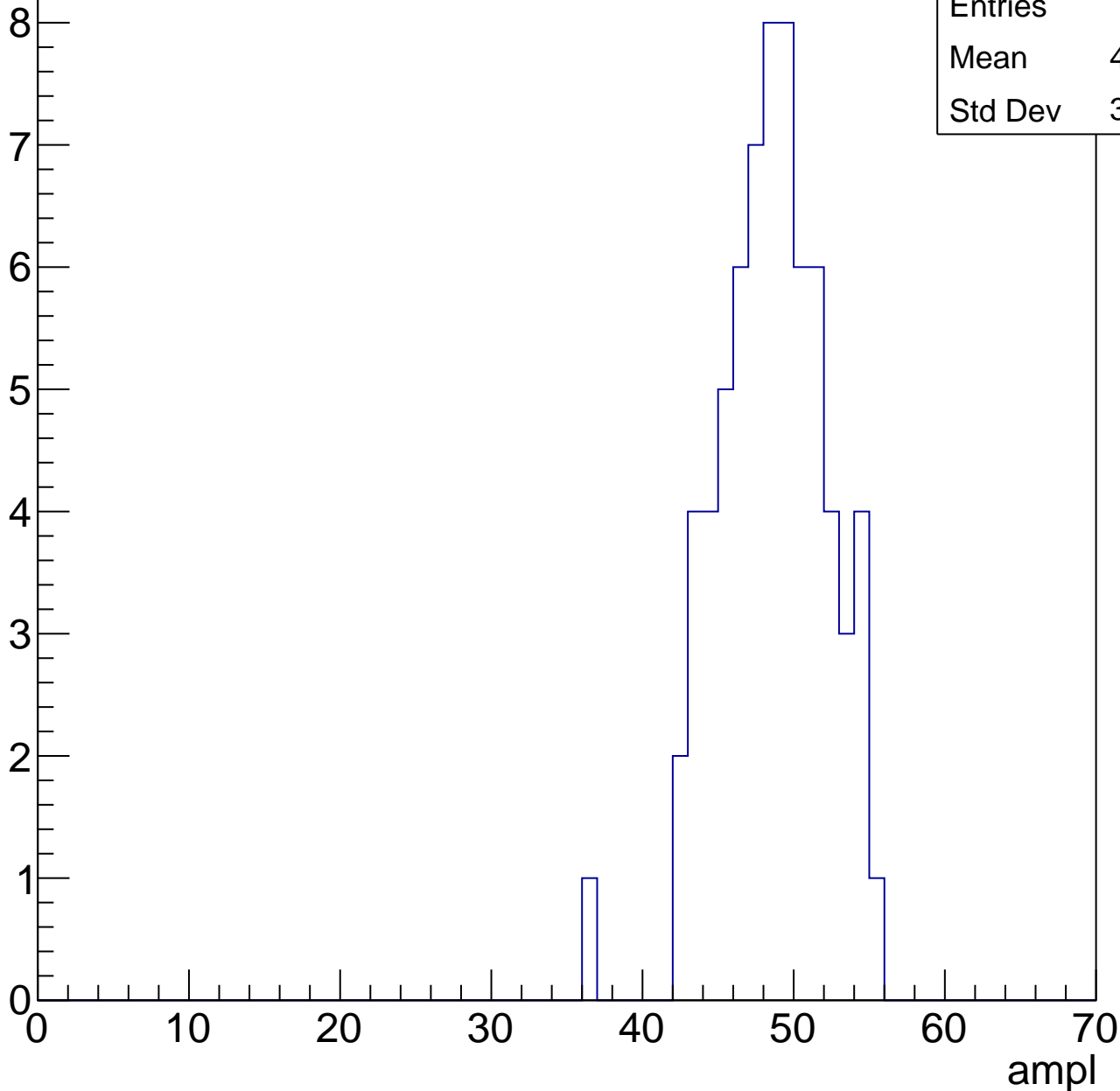


# B1L101S, U20-ch104, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	48.09
Std Dev	3.558

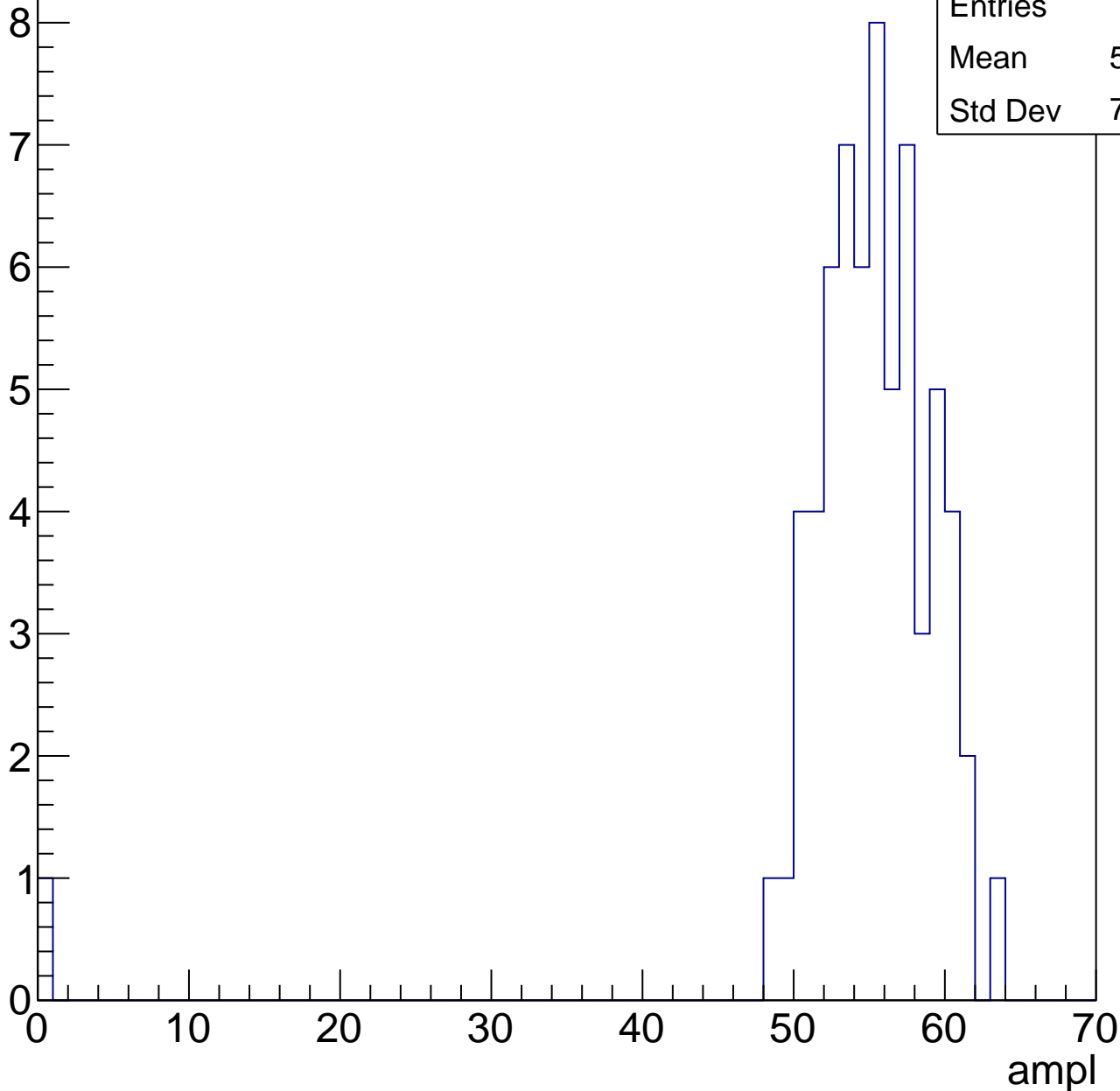


# B1L101S, U20-ch104, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	54.17
Std Dev	7.538

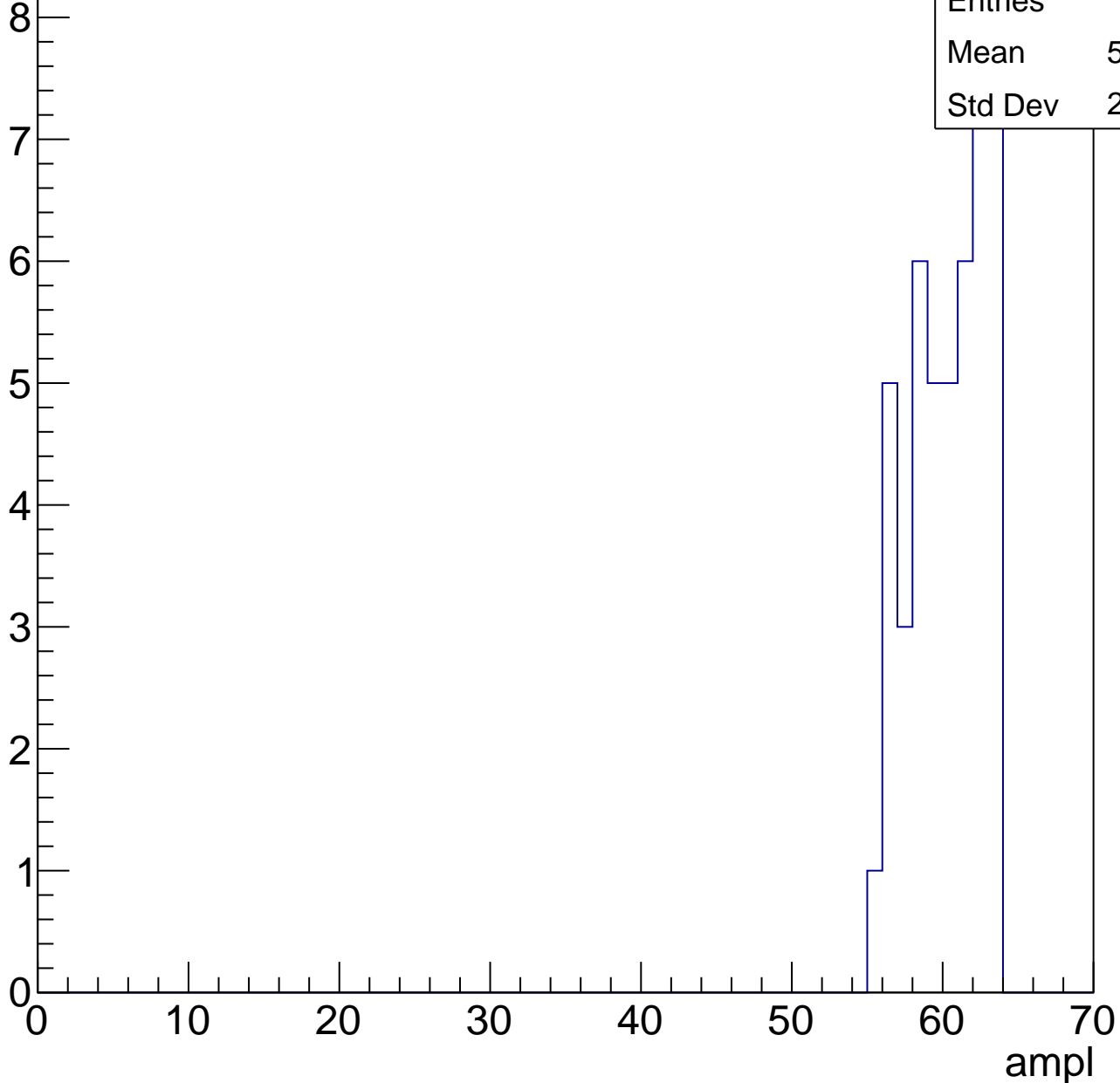


# B1L101S, U20-ch104, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	47
Mean	59.89
Std Dev	2.399



# B1L101S, U20-ch104, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

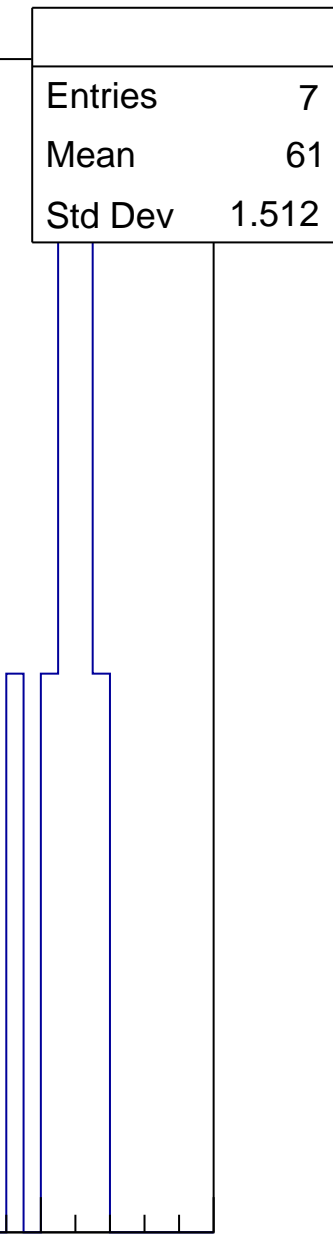
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	7
Mean	61
Std Dev	1.512

0 10 20 30 40 50 60 70

ampl





# B1L101S, U20-ch104, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	3
Mean	0
Std Dev	0

# B1L101S, U20-ch105, adc0

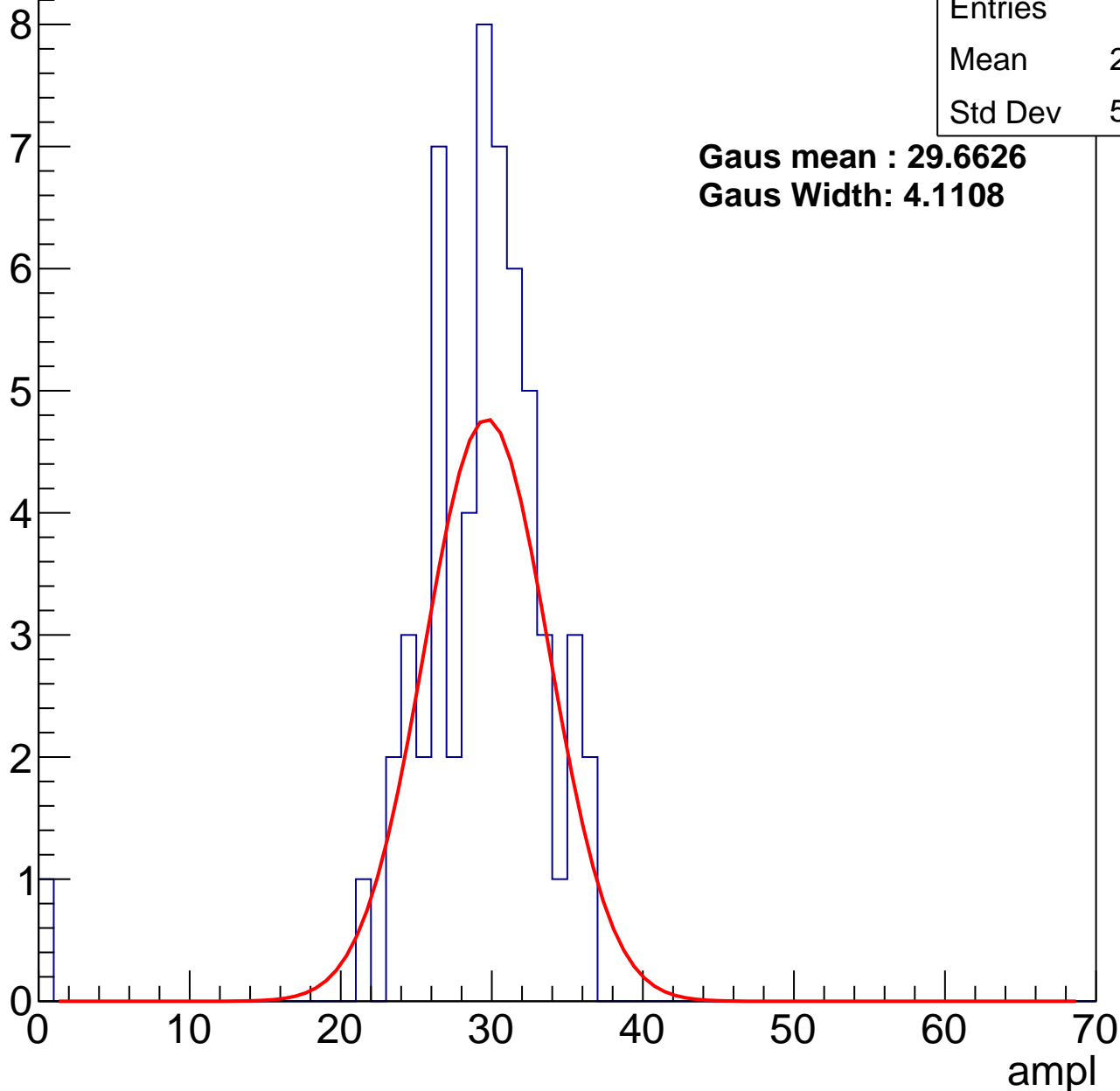
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	57
Mean	28.68
Std Dev	5.144

**Gaus mean : 29.6626**

**Gaus Width: 4.1108**



# B1L101S, U20-ch105, adc1

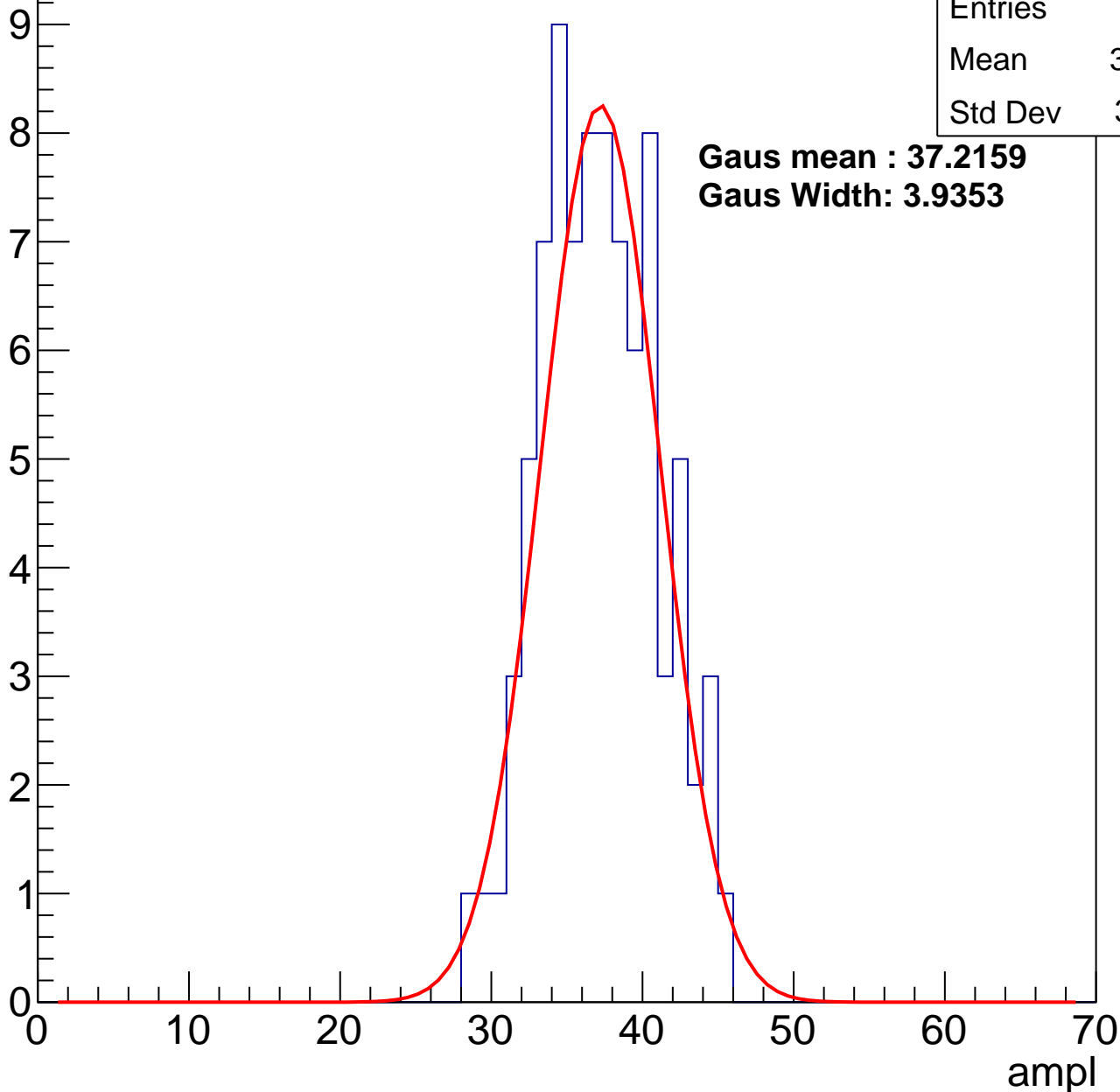
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	85
Mean	36.73
Std Dev	3.771

**Gaus mean : 37.2159**

**Gaus Width: 3.9353**



# B1L101S, U20-ch105, adc2

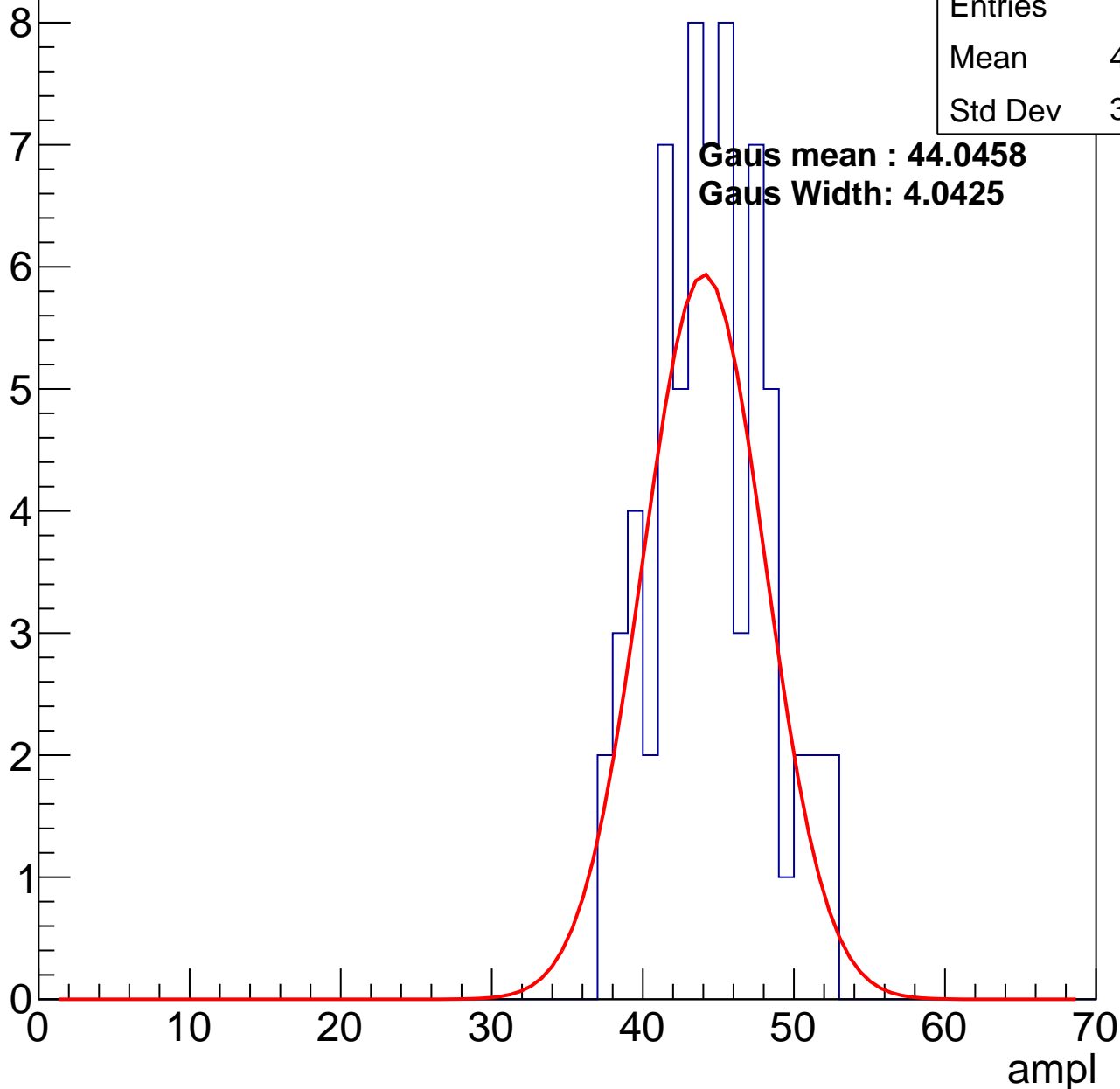
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	44.04
Std Dev	3.668

**Gaus mean : 44.0458**

**Gaus Width: 4.0425**

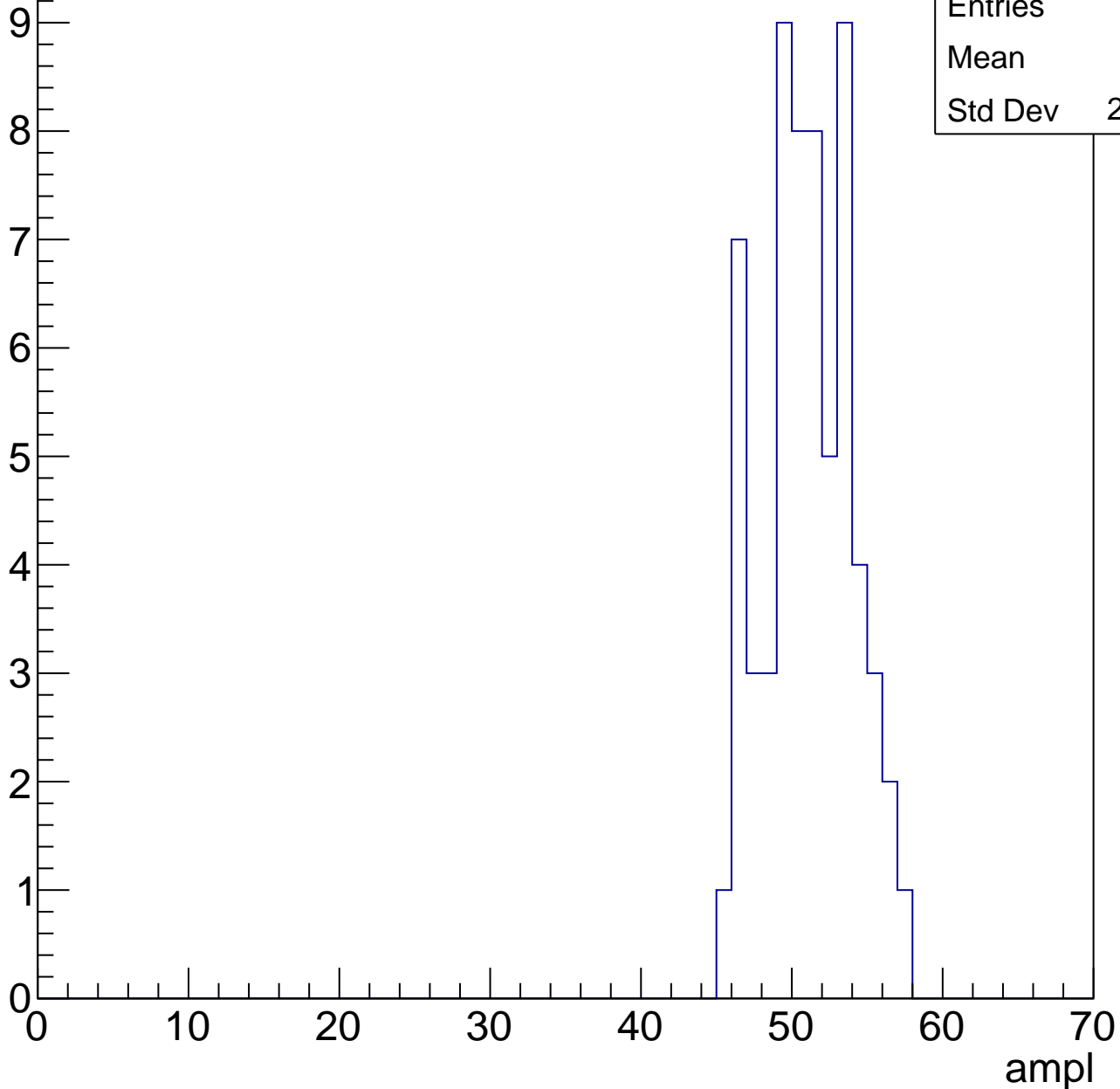


# B1L101S, U20-ch105, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	50.6
Std Dev	2.903

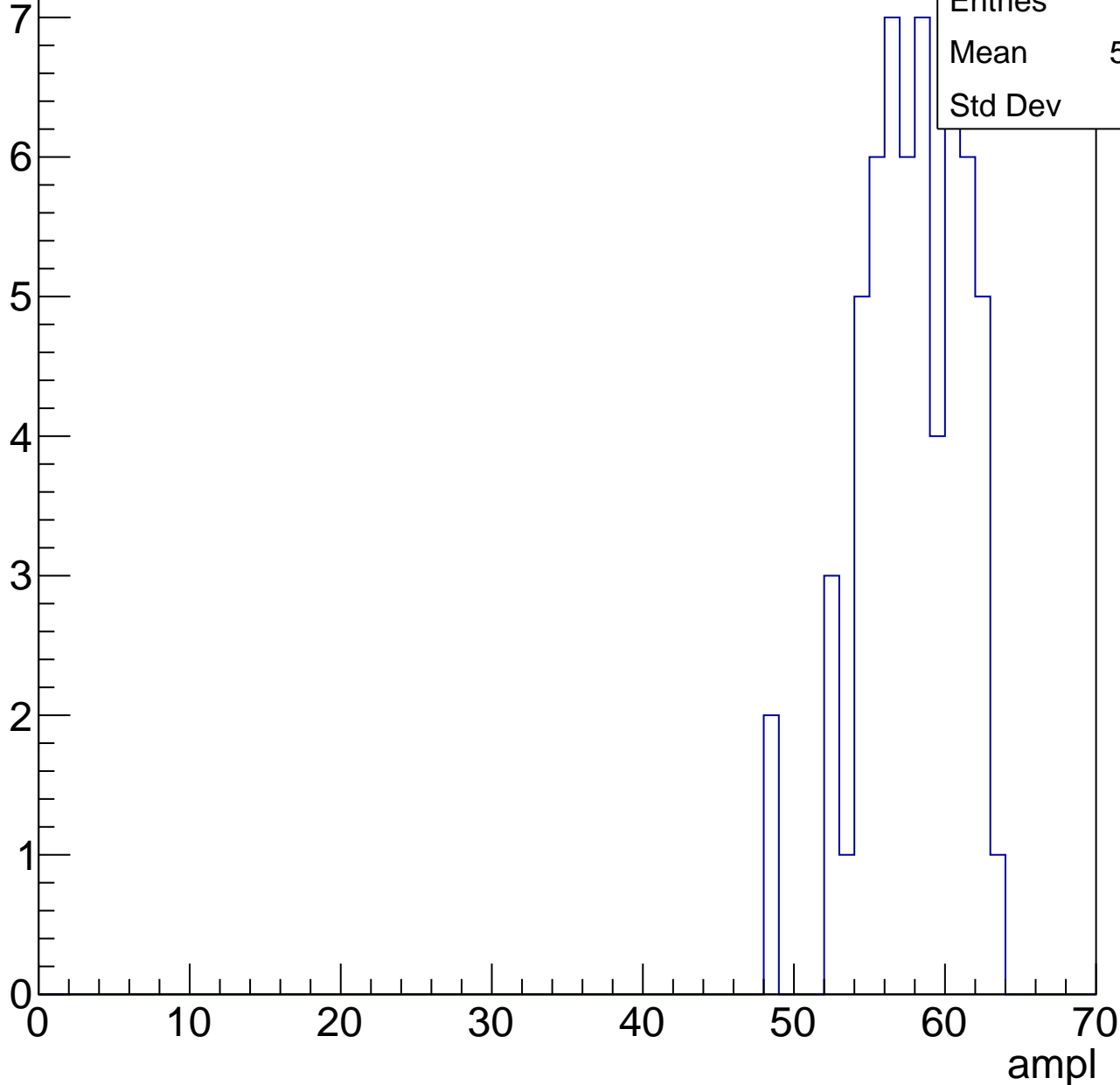


# B1L101S, U20-ch105, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	60
Mean	57.33
Std Dev	3.33

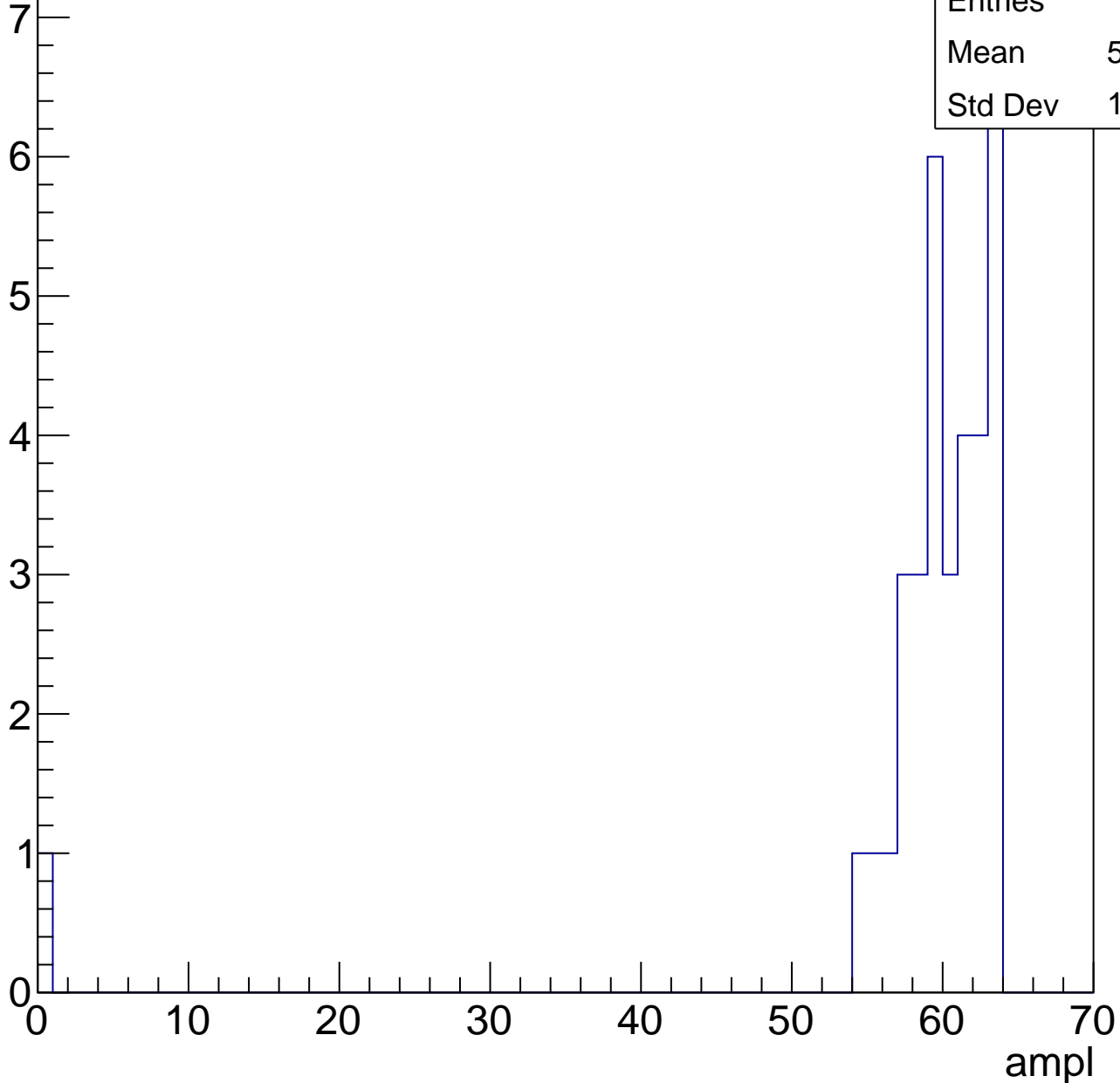


# B1L101S, U20-ch105, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	34
Mean	58.15
Std Dev	10.42



# B1L101S, U20-ch105, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	3
Mean	62.67
Std Dev	0.4714

ampl

0 10 20 30 40 50 60 70



# B1L101S, U20-ch105, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U20-ch106, adc0

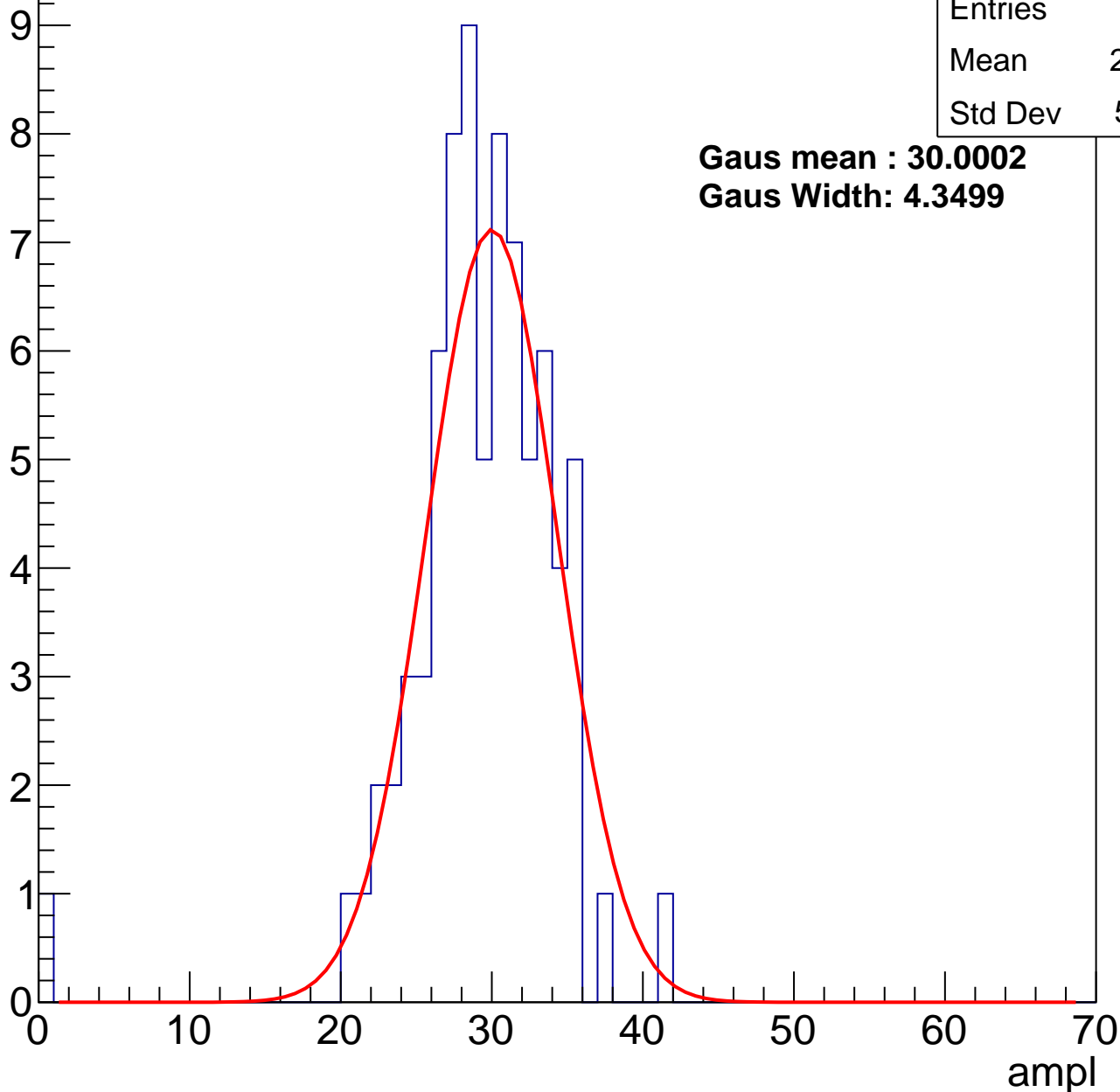
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	78
Mean	28.86
Std Dev	5.111

**Gaus mean : 30.0002**

**Gaus Width: 4.3499**



# B1L101S, U20-ch106, adc1

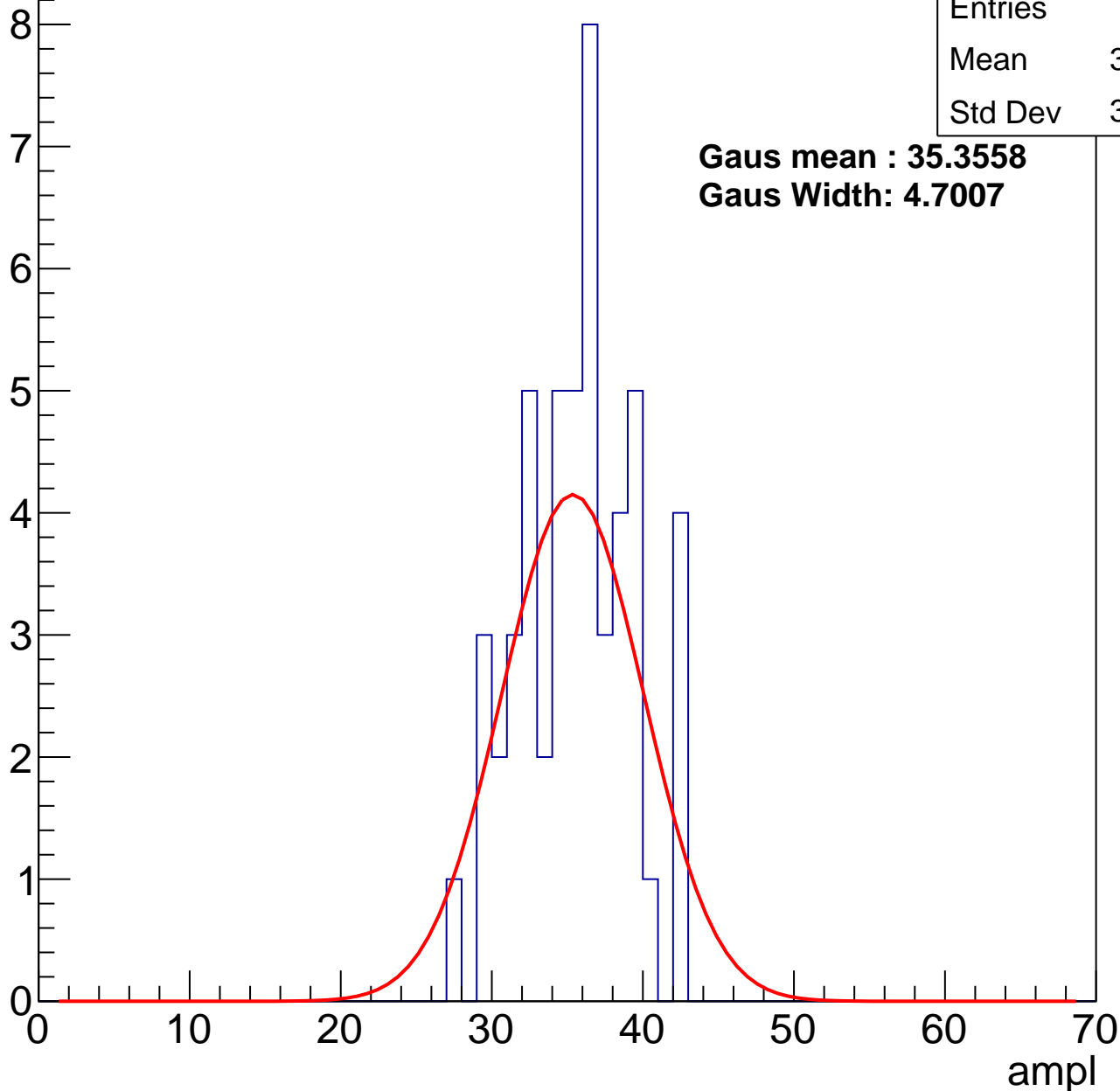
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	51
Mean	35.14
Std Dev	3.662

**Gaus mean : 35.3558**

**Gaus Width: 4.7007**



# B1L101S, U20-ch106, adc2

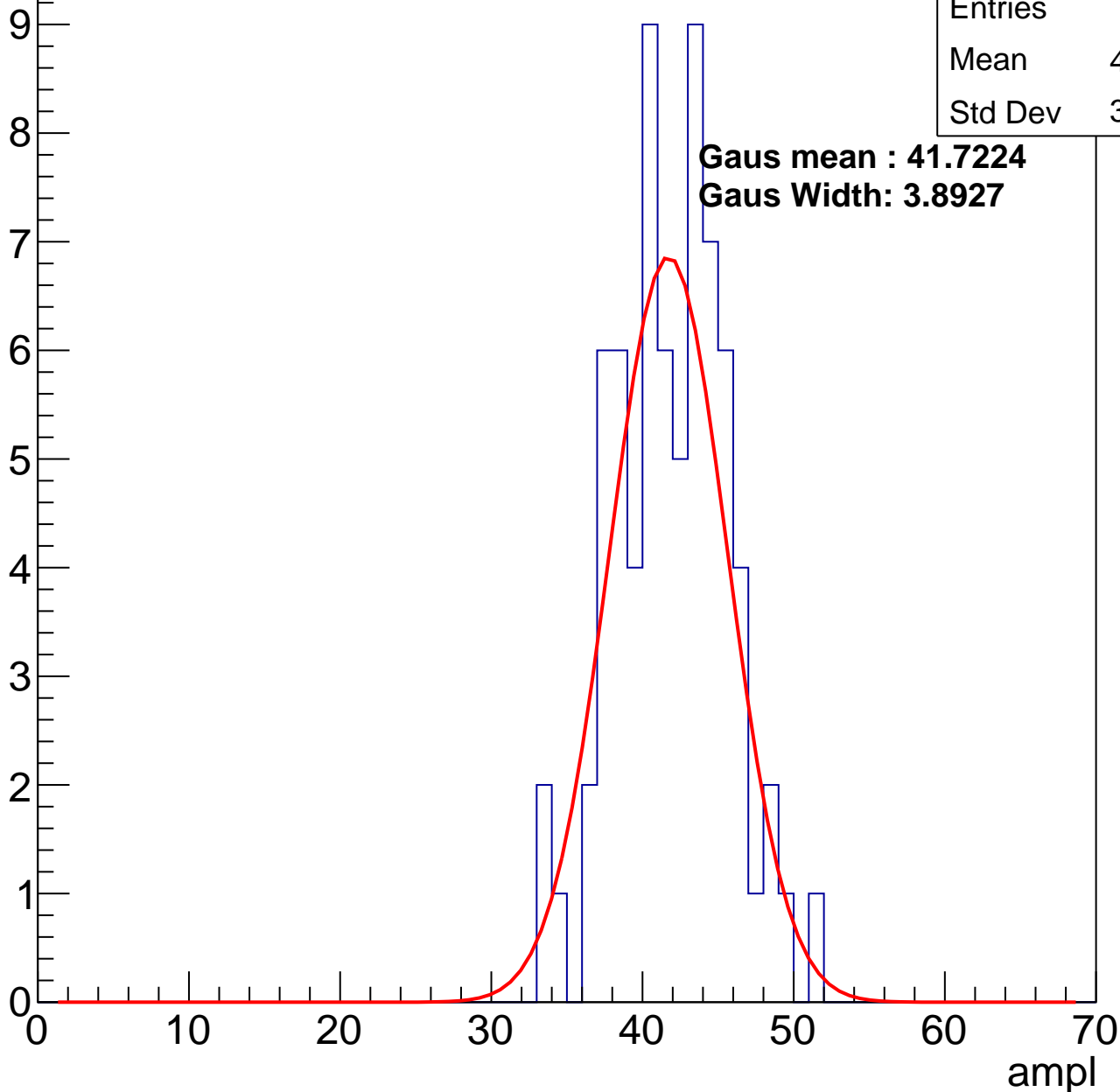
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	72
Mean	41.47
Std Dev	3.697

**Gaus mean : 41.7224**

**Gaus Width: 3.8927**

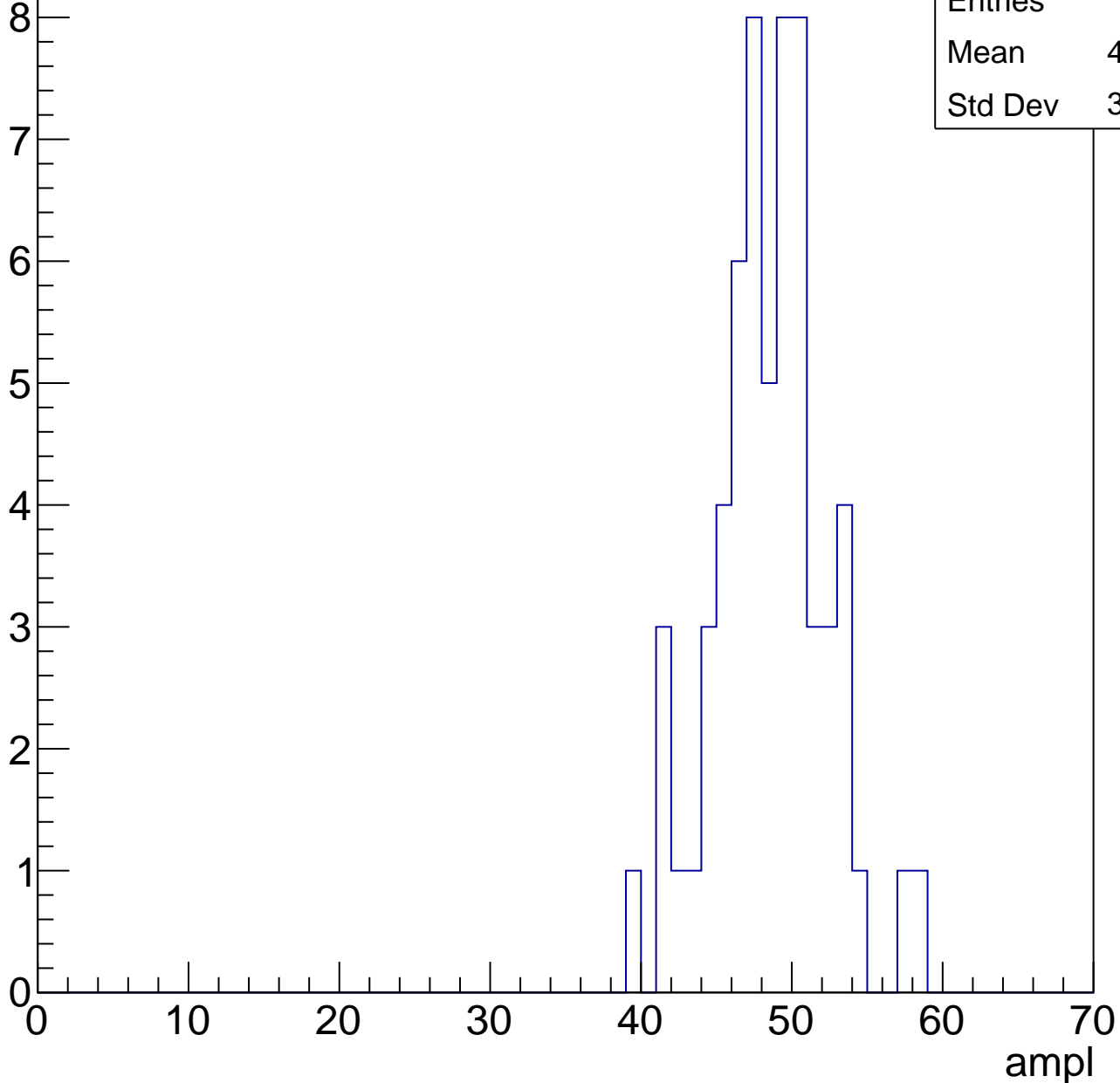


# B1L101S, U20-ch106, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	48.08
Std Dev	3.703

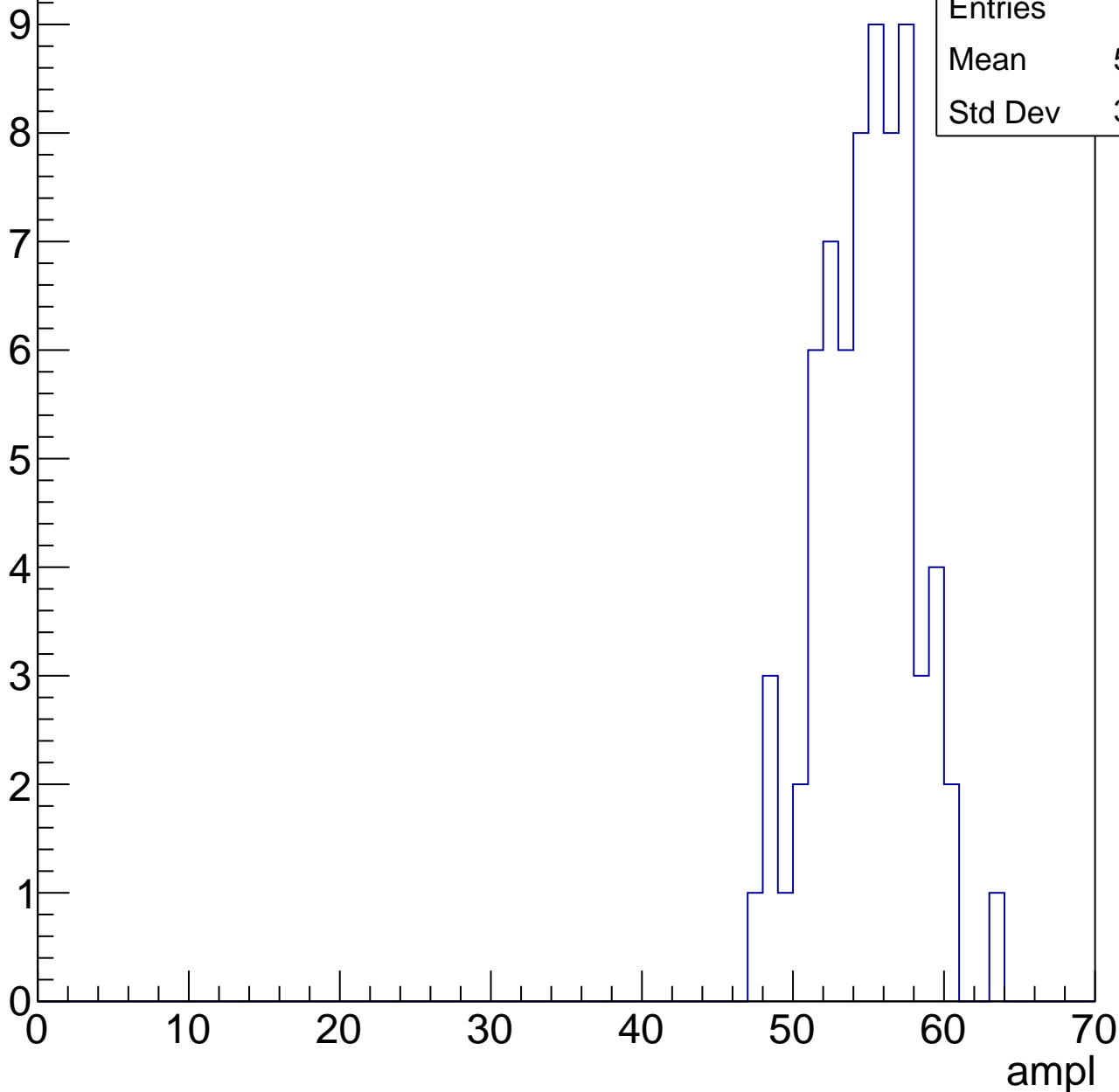


# B1L101S, U20-ch106, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	54.41
Std Dev	3.191

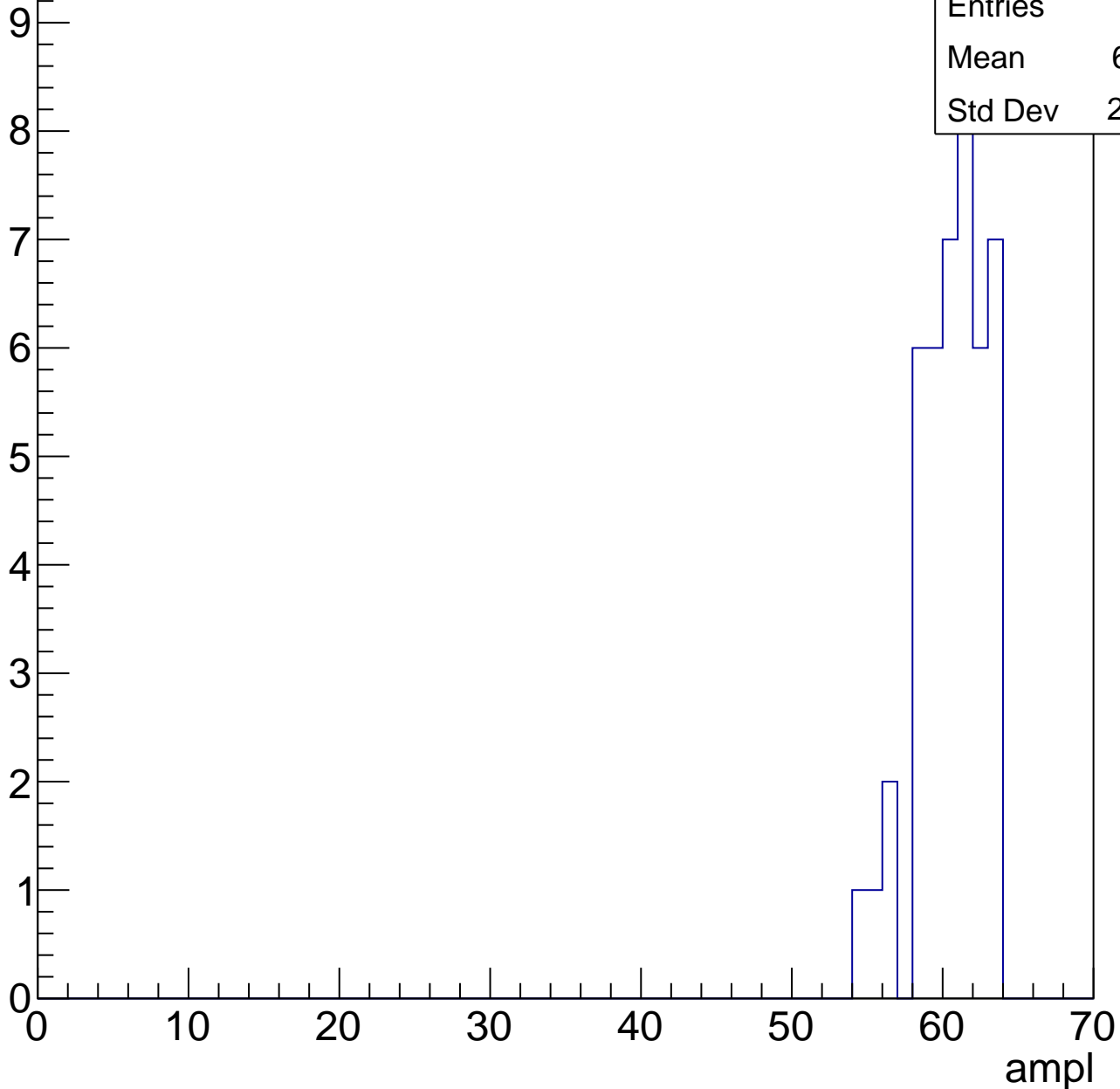


# B1L101S, U20-ch106, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

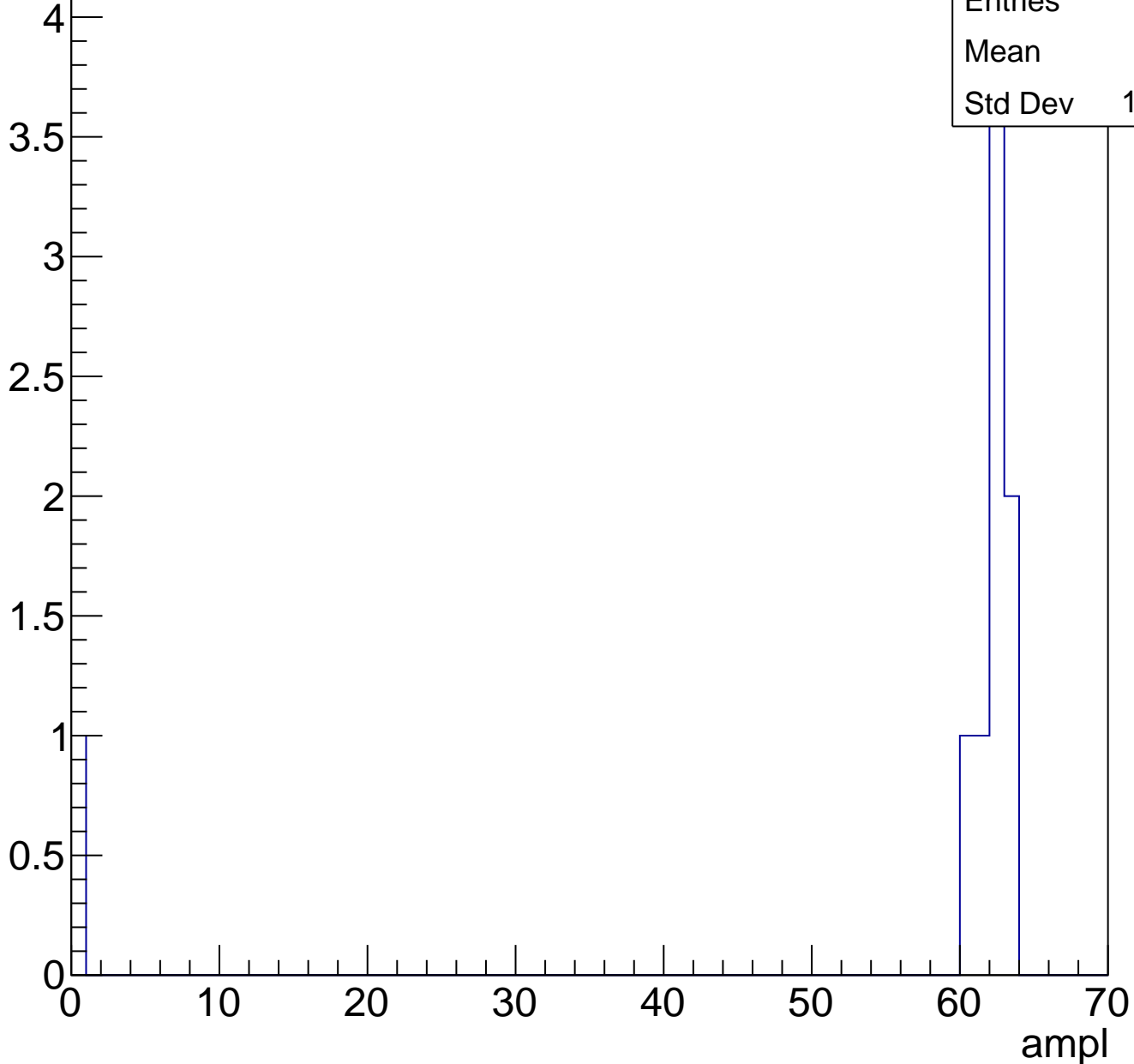
Entries	45
Mean	60.11
Std Dev	2.203



# B1L101S, U20-ch106, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U20-ch106, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U20-ch107, adc0

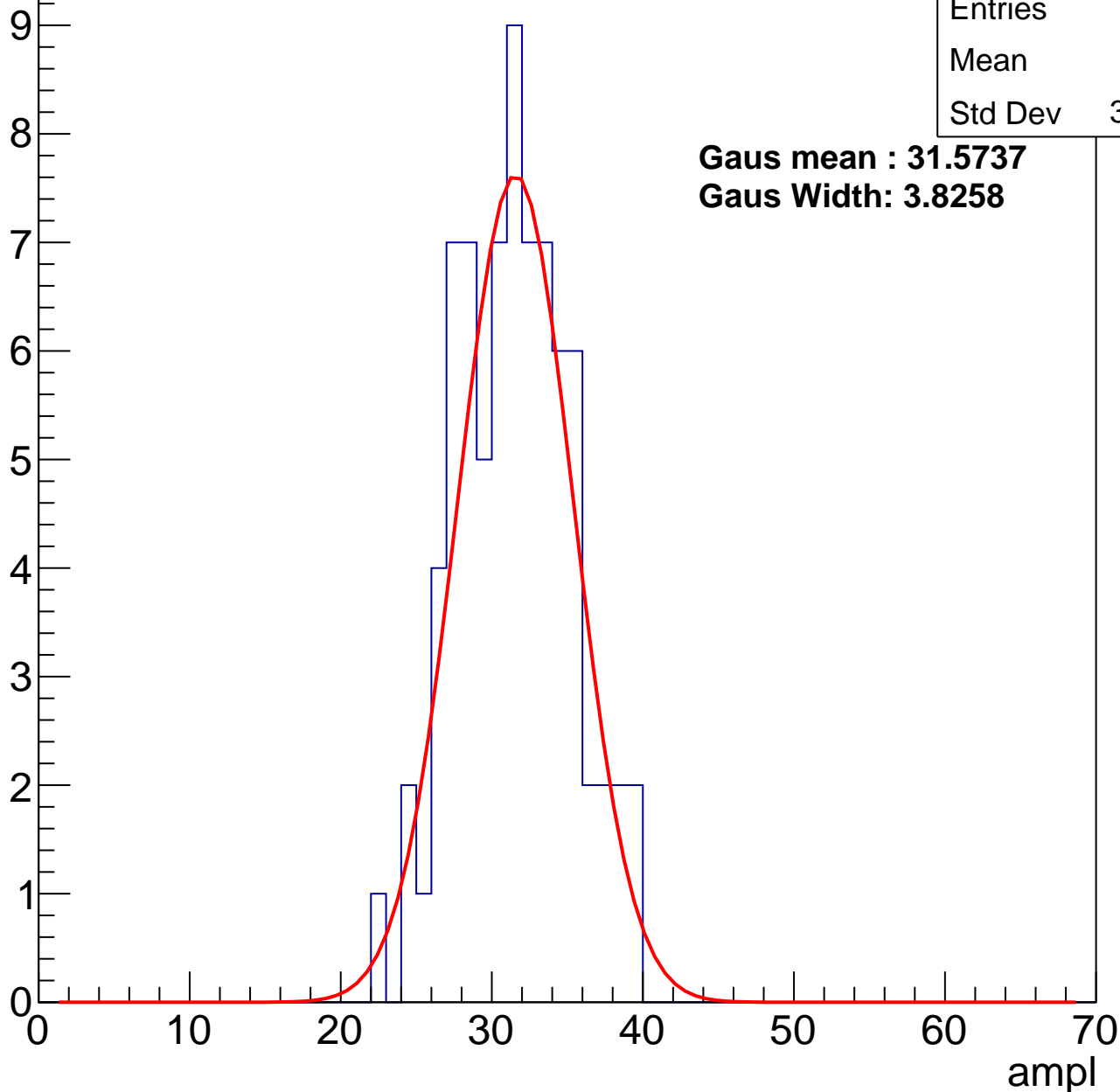
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	77
Mean	31
Std Dev	3.693

**Gaus mean : 31.5737**

**Gaus Width: 3.8258**



# B1L101S, U20-ch107, adc1

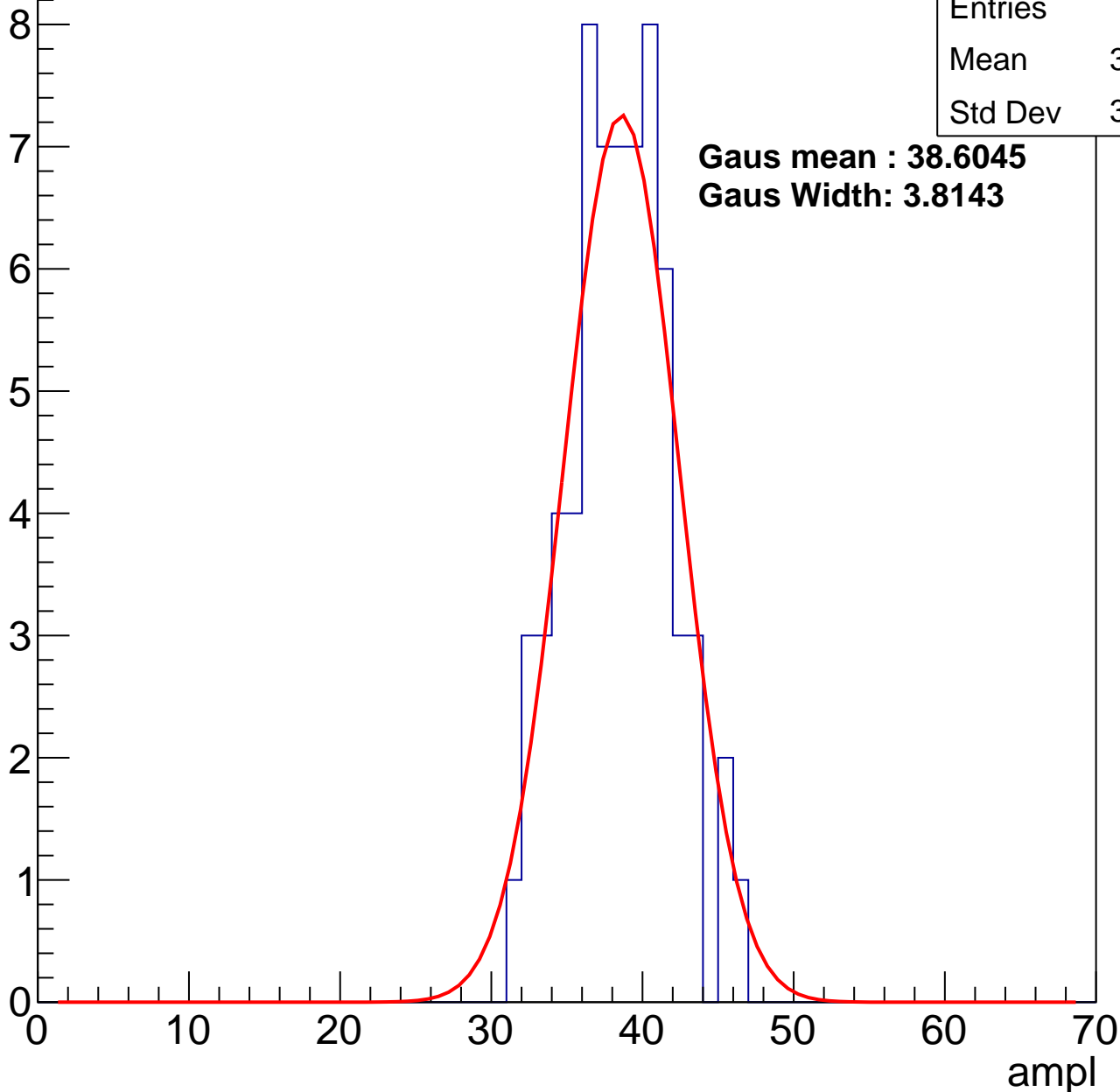
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	67
Mean	37.99
Std Dev	3.343

**Gaus mean : 38.6045**

**Gaus Width: 3.8143**



# B1L101S, U20-ch107, adc2

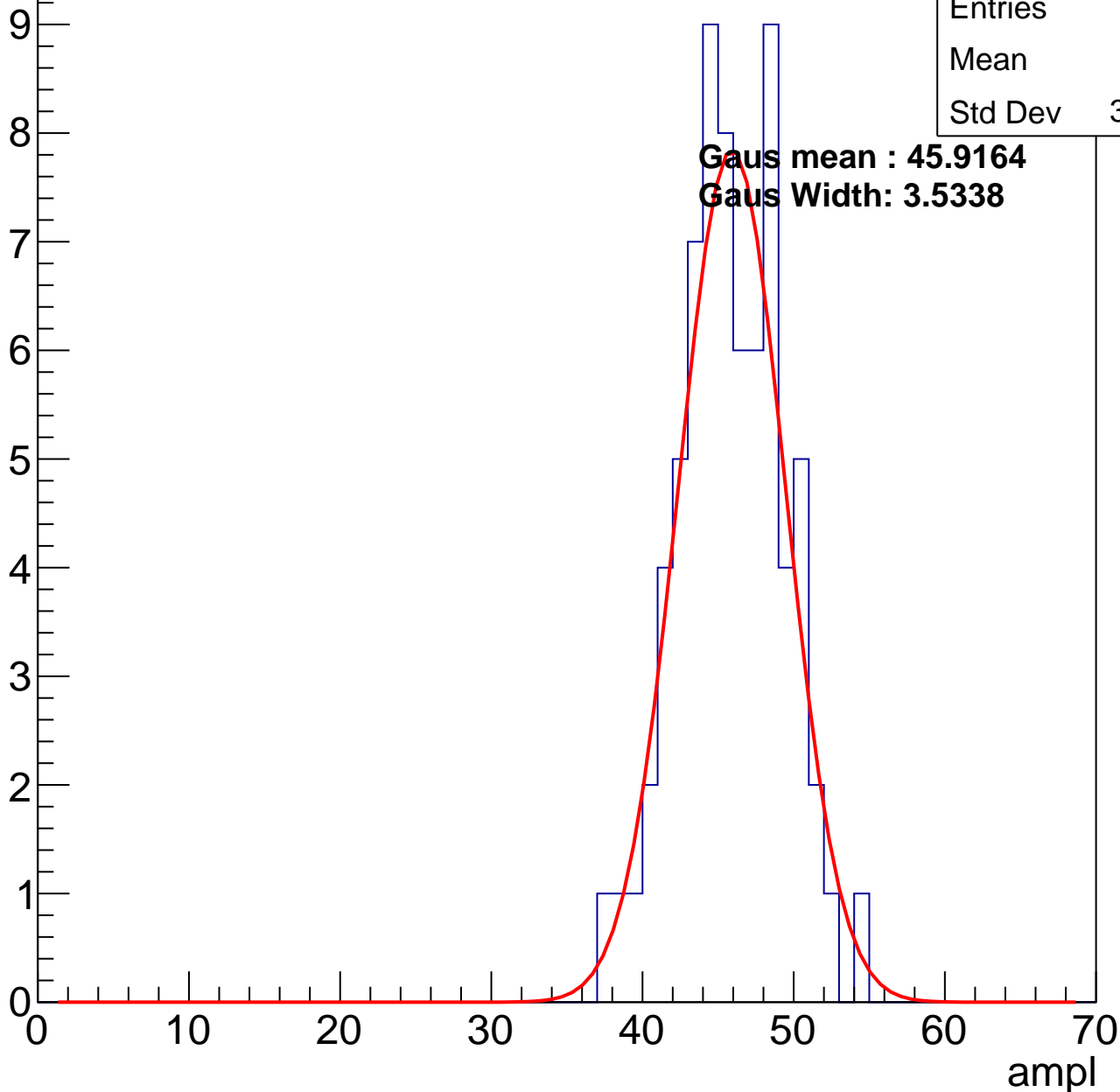
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	72
Mean	45.4
Std Dev	3.406

**Gaus mean : 45.9164**

**Gaus Width: 3.5338**

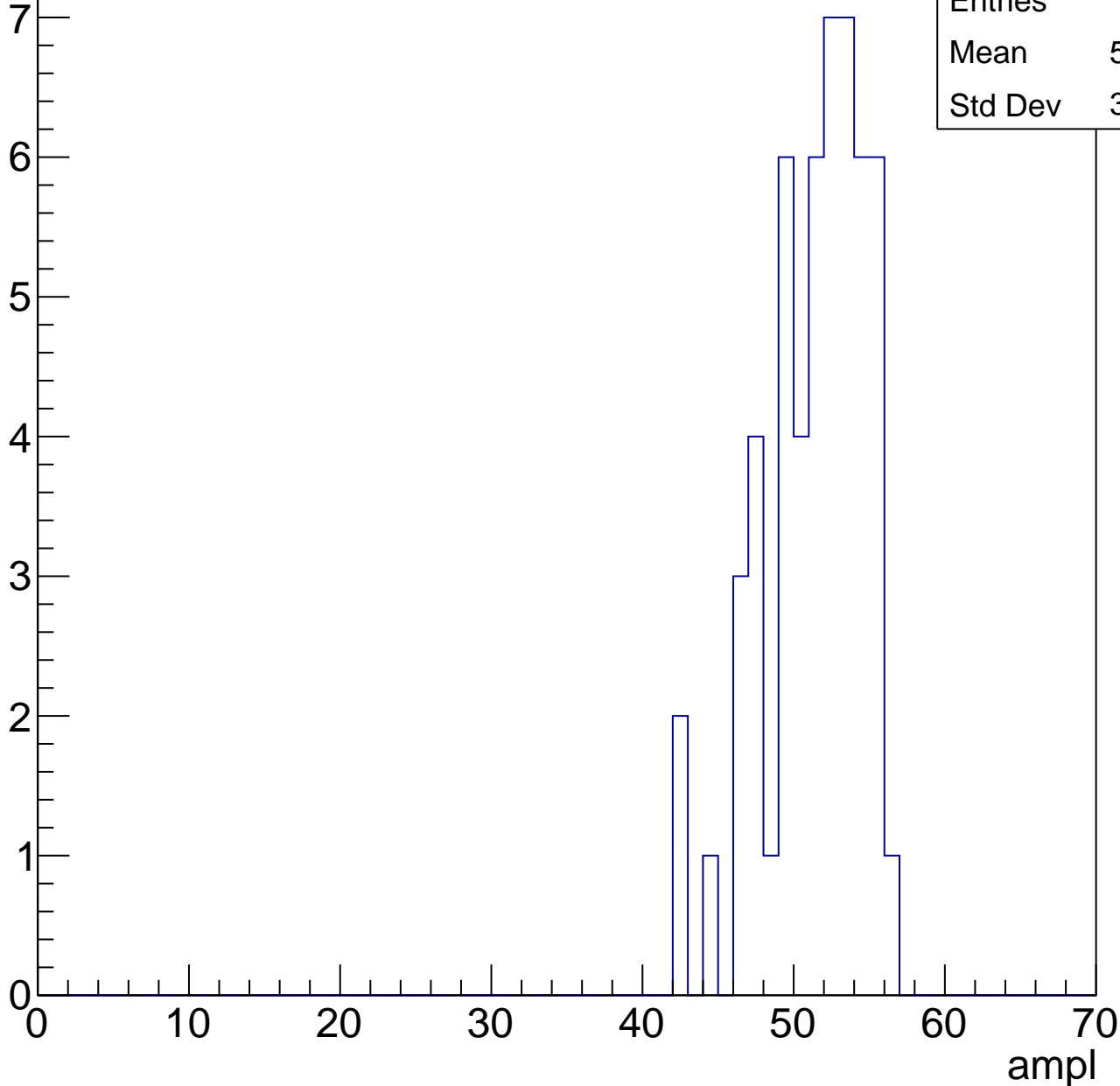


# B1L101S, U20-ch107, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

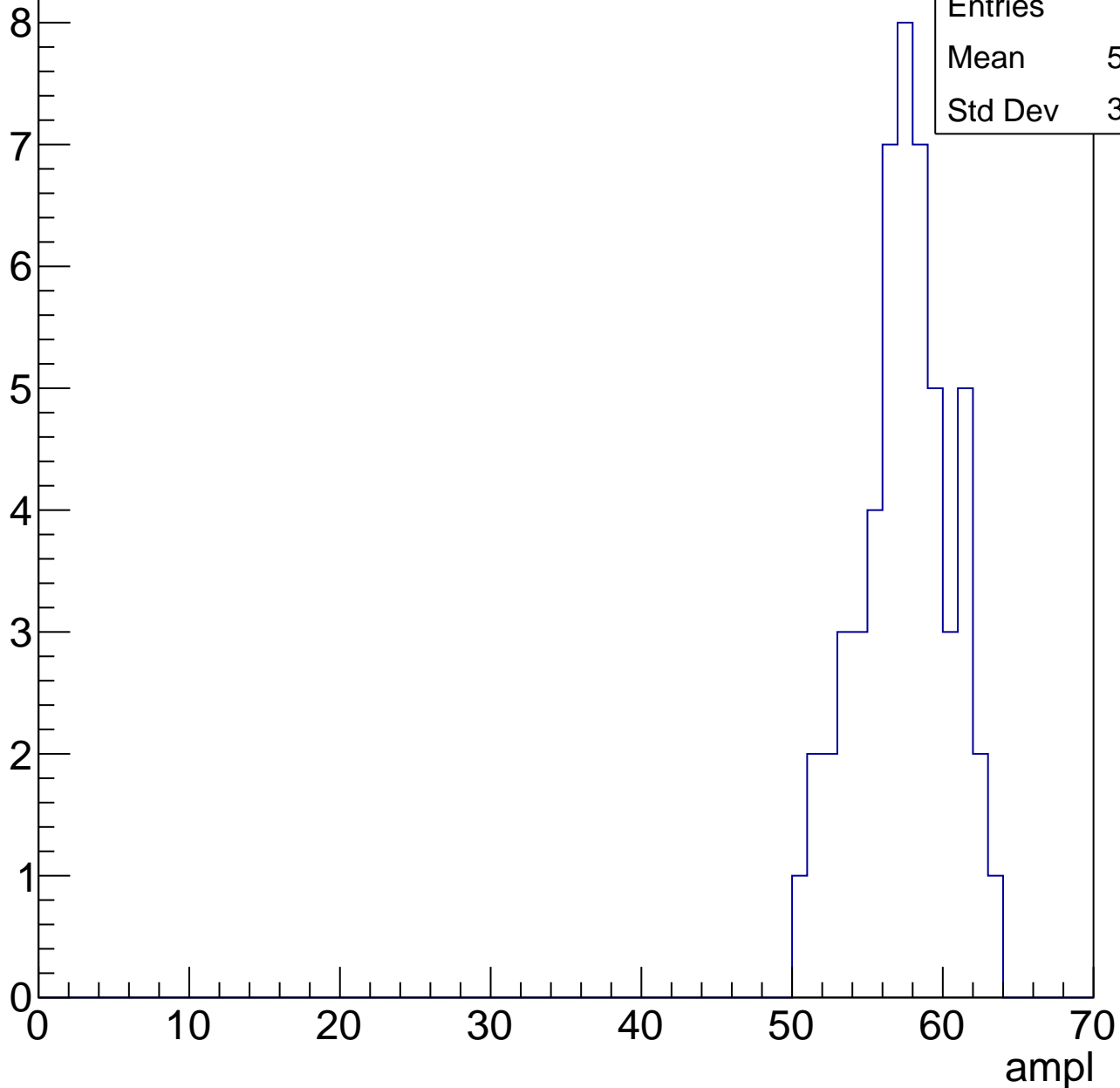
Entries	54
Mean	50.87
Std Dev	3.322



# B1L101S, U20-ch107, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

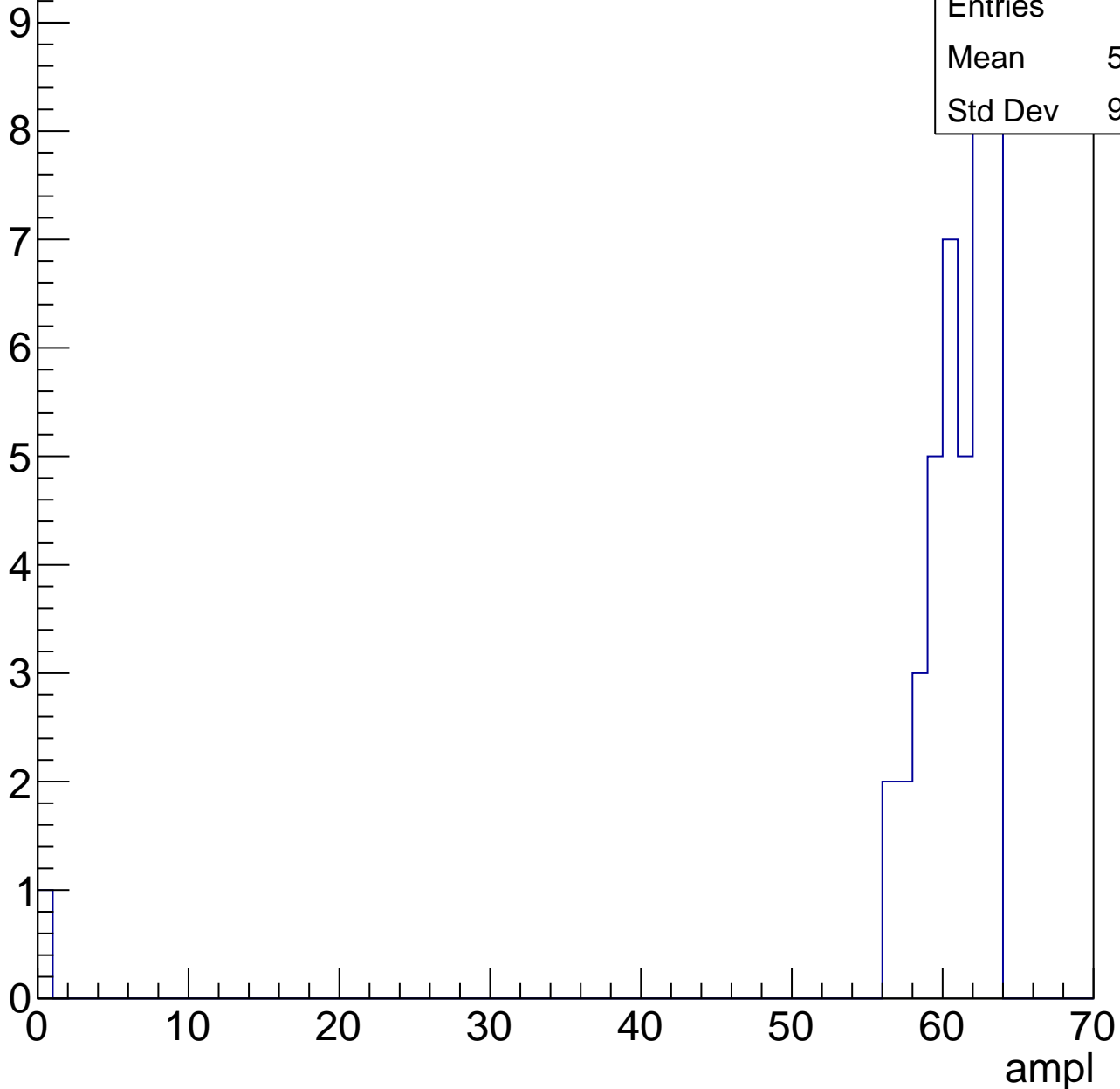


# B1L101S, U20-ch107, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	42
Mean	59.12
Std Dev	9.452



# B1L101S, U20-ch107, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0



# B1L101S, U20-ch107, adc7

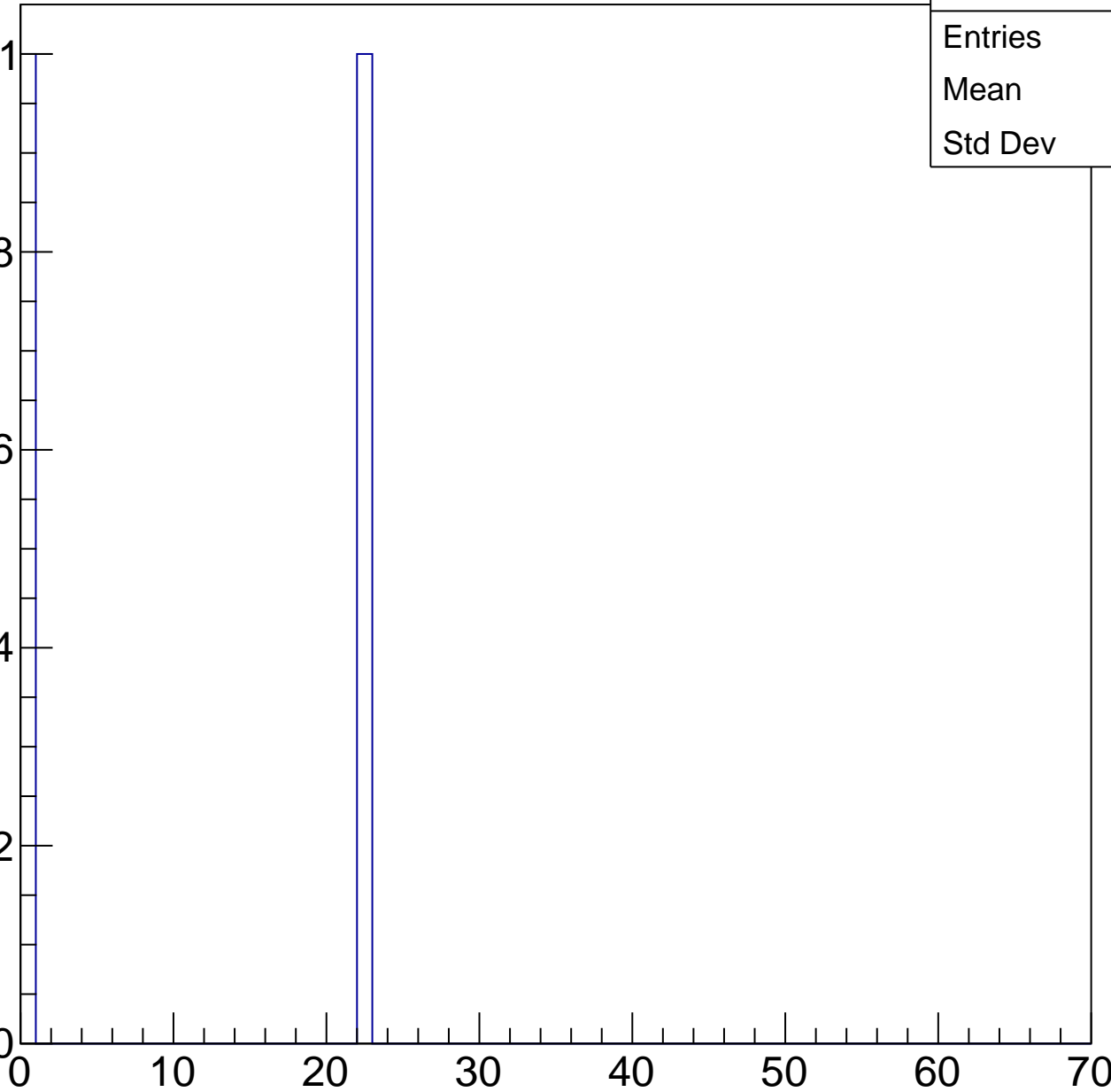
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

1  
0.8  
0.6  
0.4  
0.2  
0

Entries	2
Mean	11
Std Dev	11

ampl



# B1L101S, U20-ch108, adc0

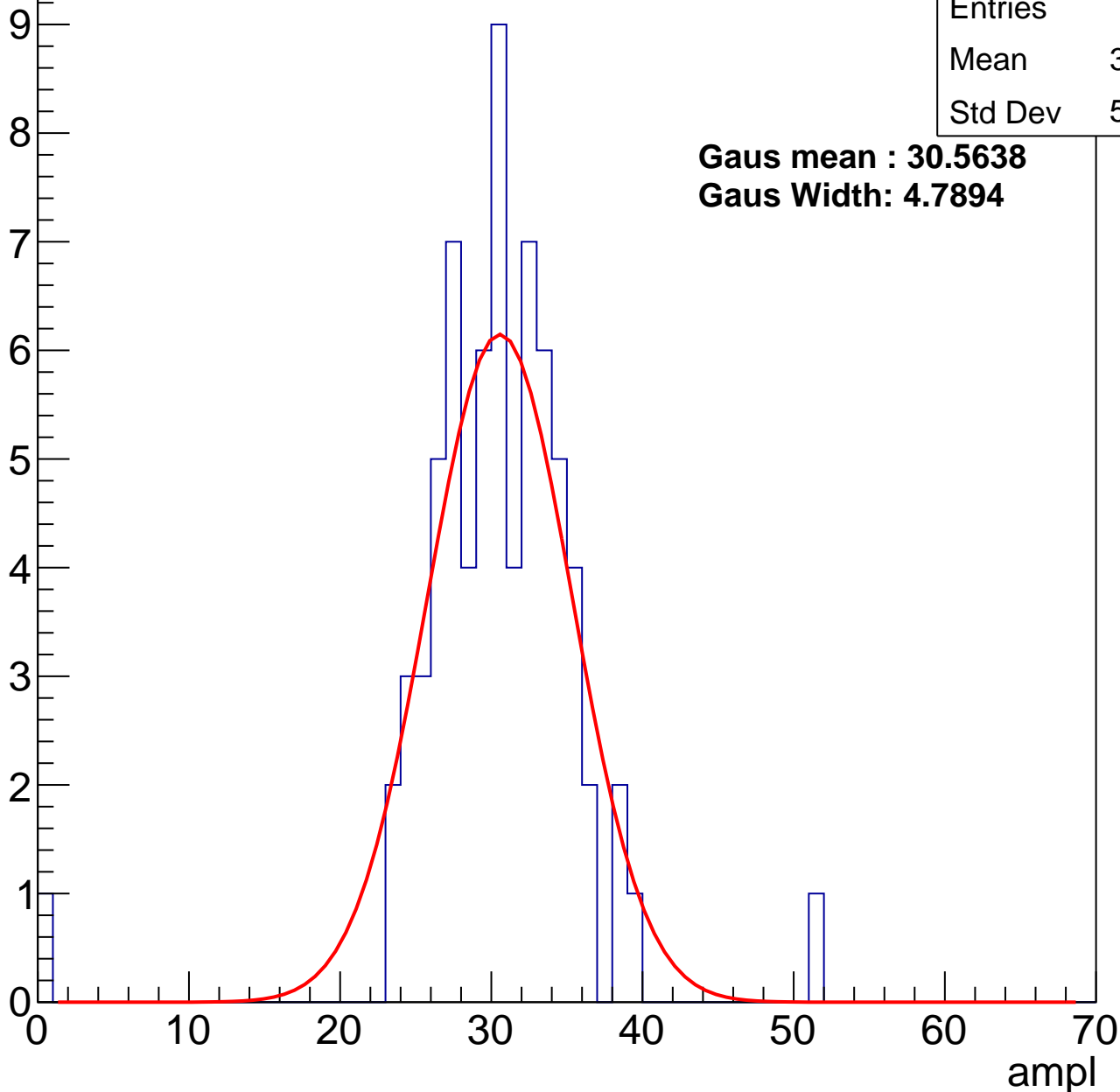
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	72
Mean	30.03
Std Dev	5.693

**Gaus mean : 30.5638**

**Gaus Width: 4.7894**



# B1L101S, U20-ch108, adc1

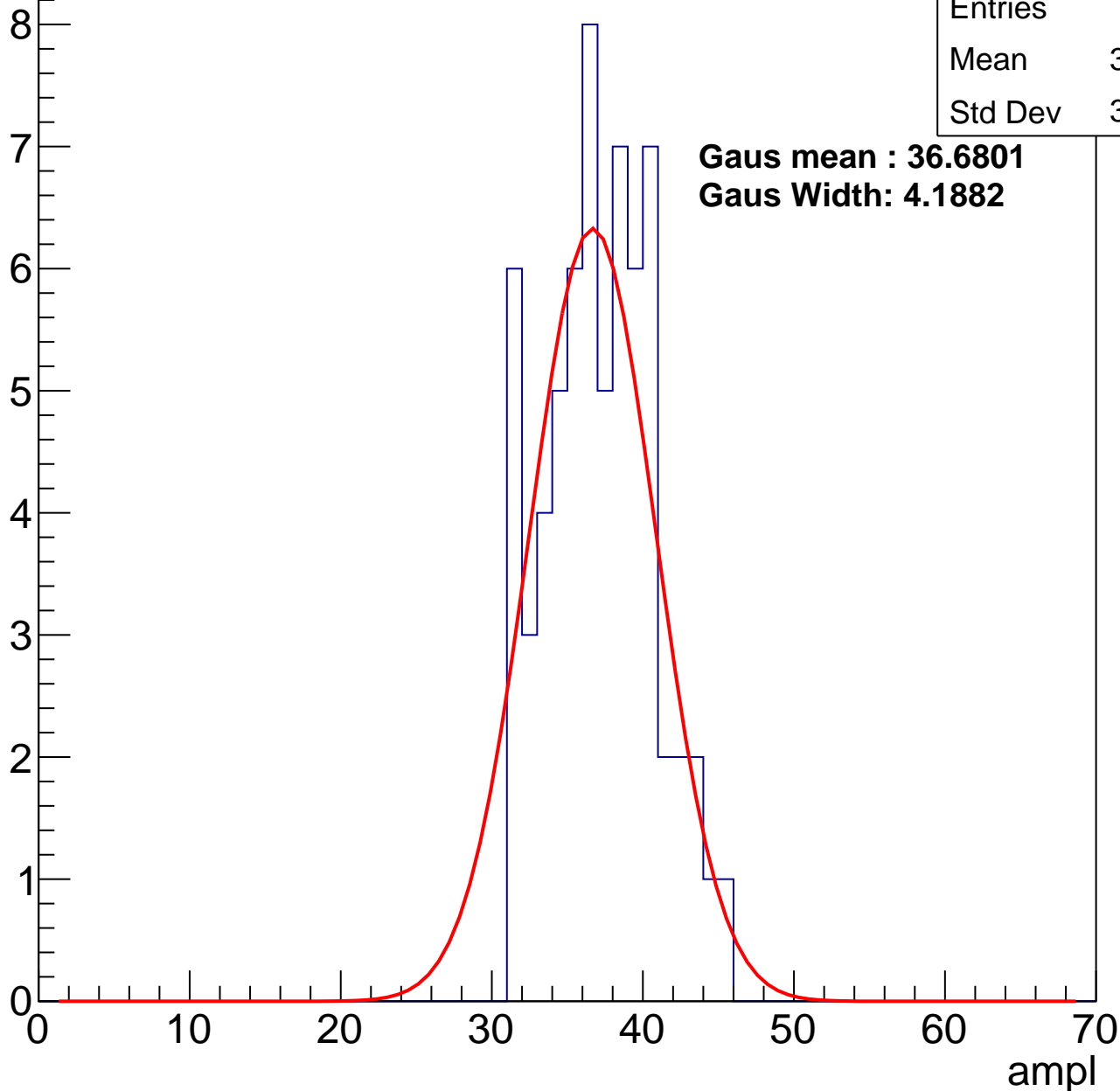
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	36.74
Std Dev	3.483

**Gaus mean : 36.6801**

**Gaus Width: 4.1882**



# B1L101S, U20-ch108, adc2

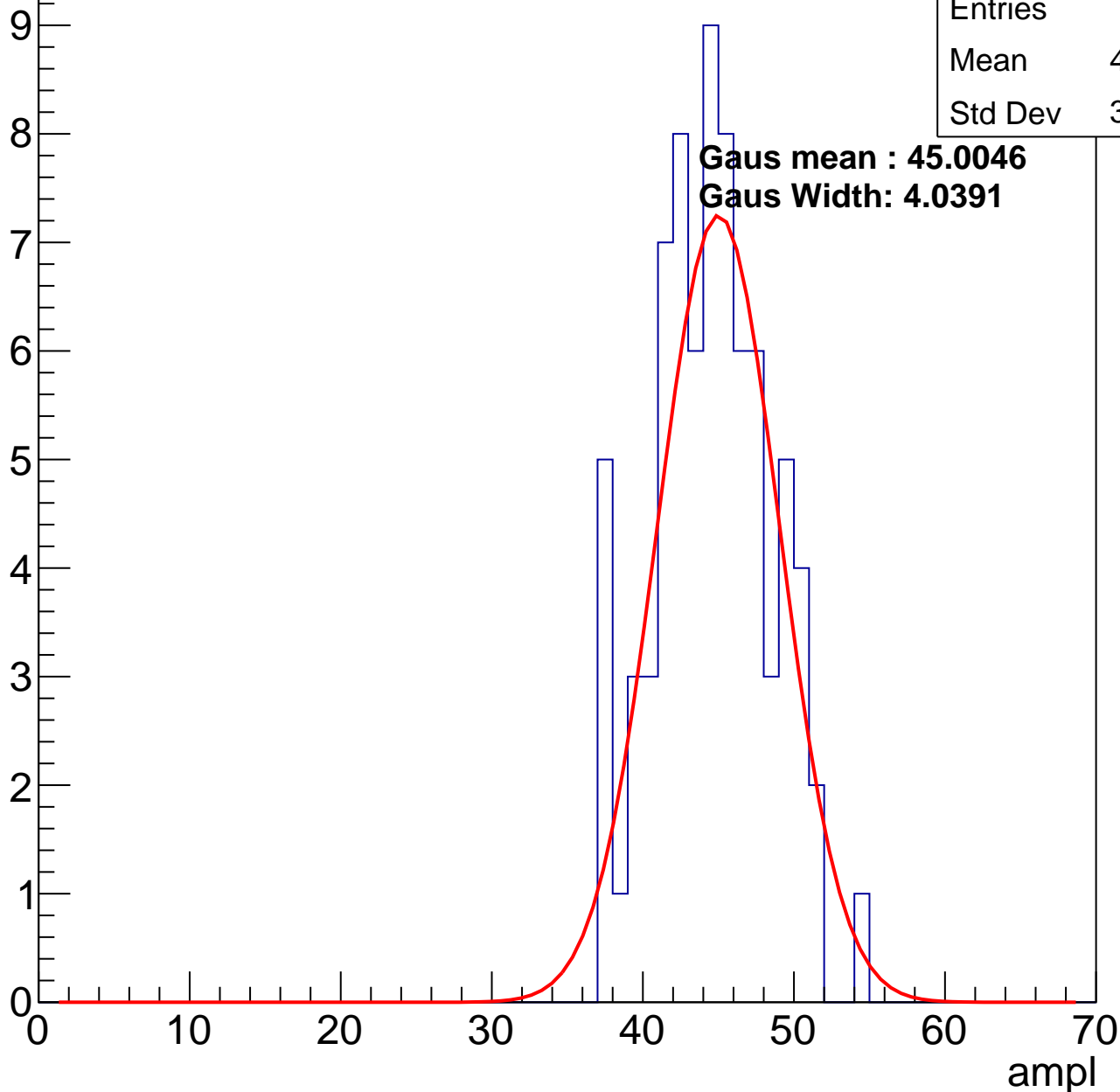
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	77
Mean	44.16
Std Dev	3.787

**Gaus mean : 45.0046**

**Gaus Width: 4.0391**

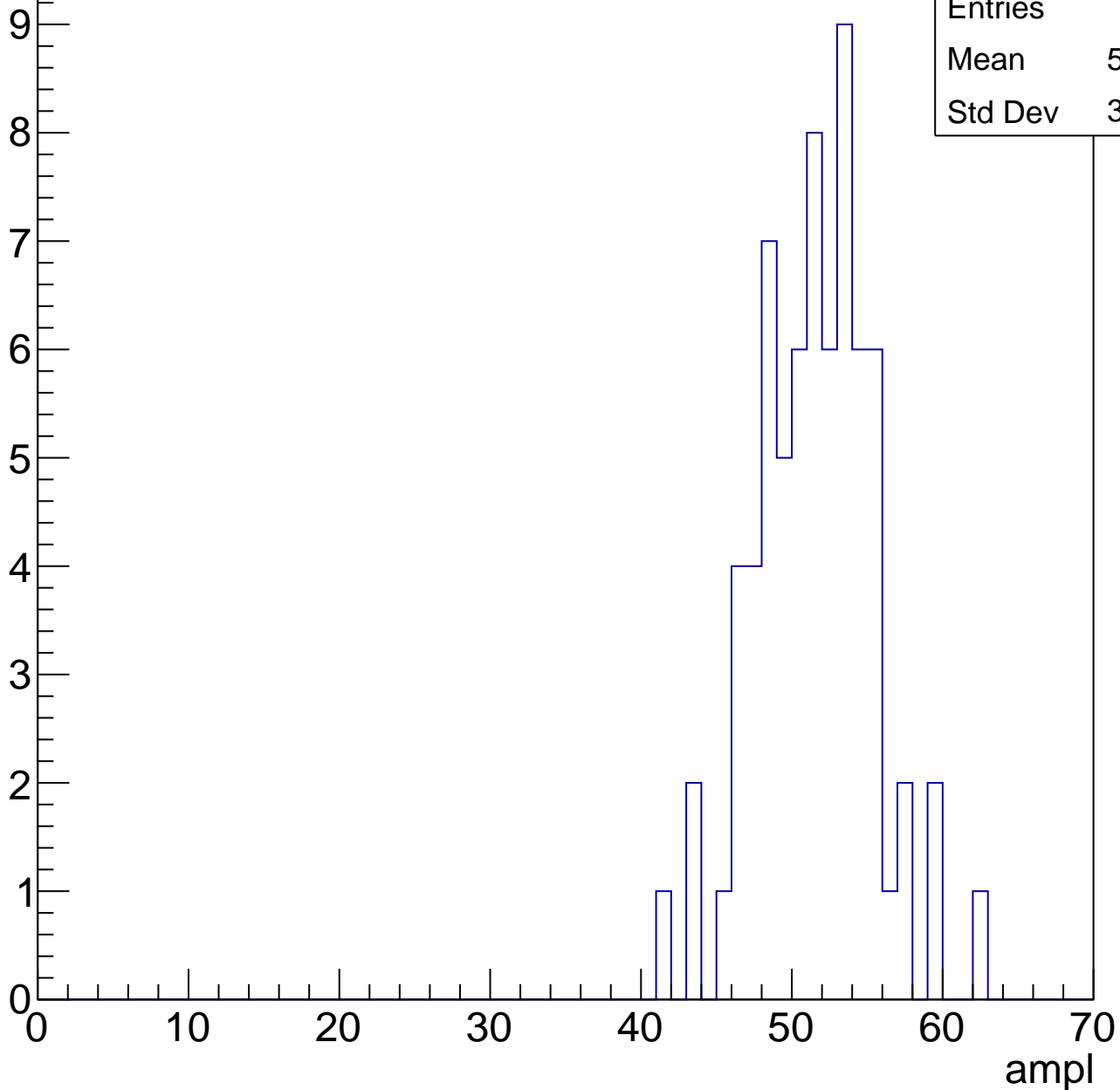


# B1L101S, U20-ch108, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	71
Mean	51.07
Std Dev	3.854

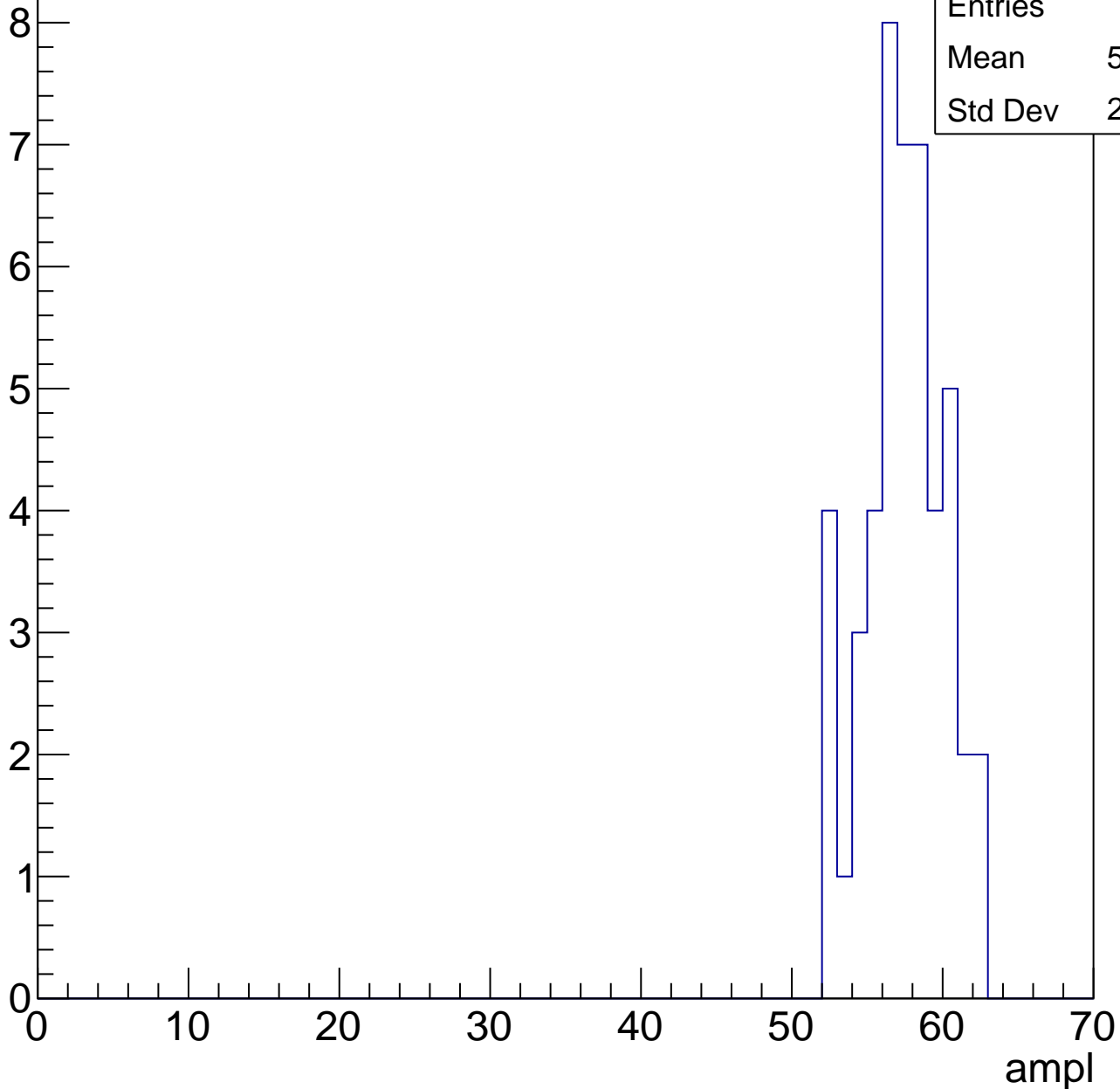


# B1L101S, U20-ch108, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

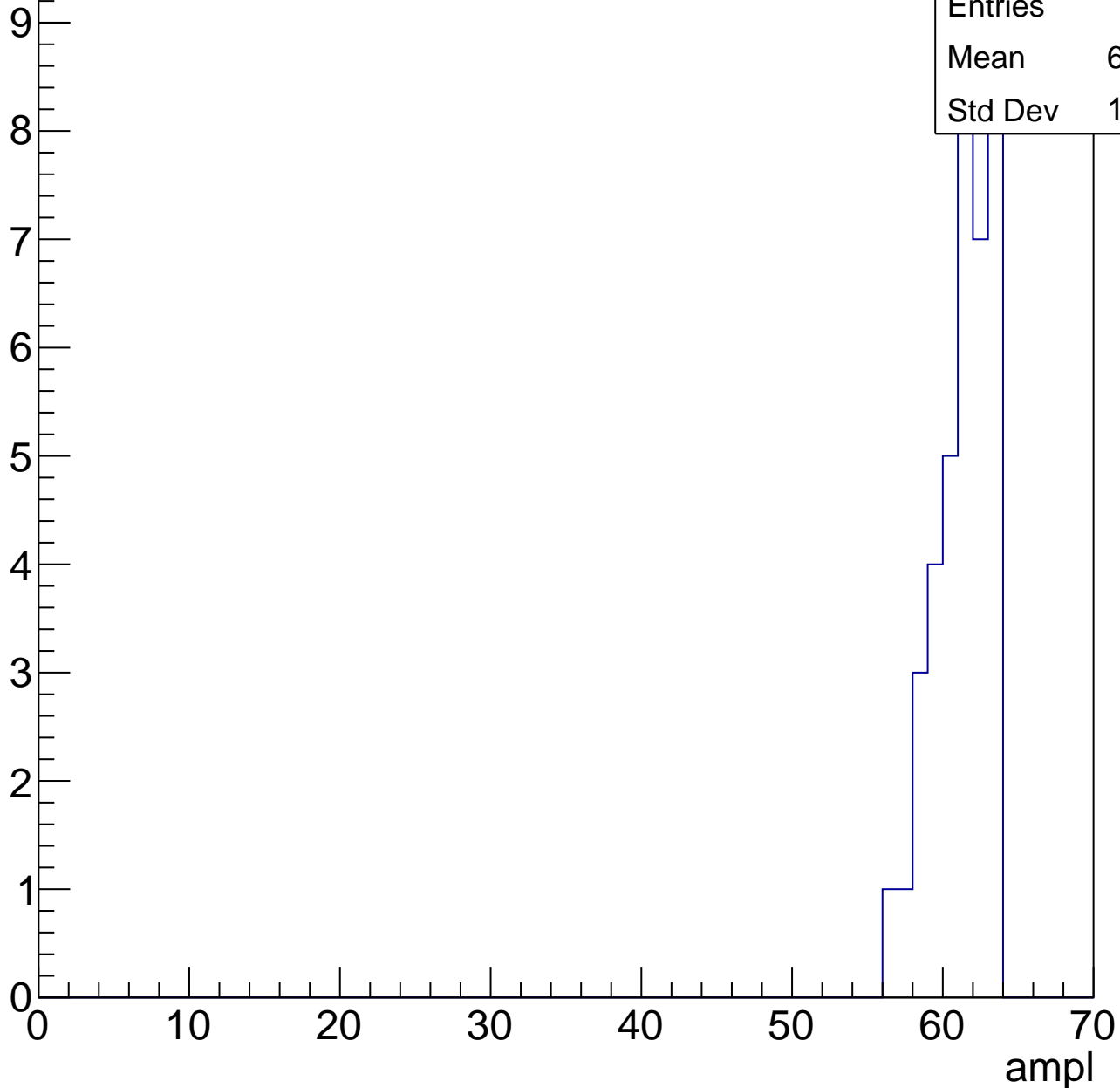
Entries	47
Mean	56.98
Std Dev	2.597



# B1L101S, U20-ch108, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U20-ch108, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U20-ch108, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U20-ch109, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	77
Mean	30.16
Std Dev	4.96

**Gaus mean : 31.0375**

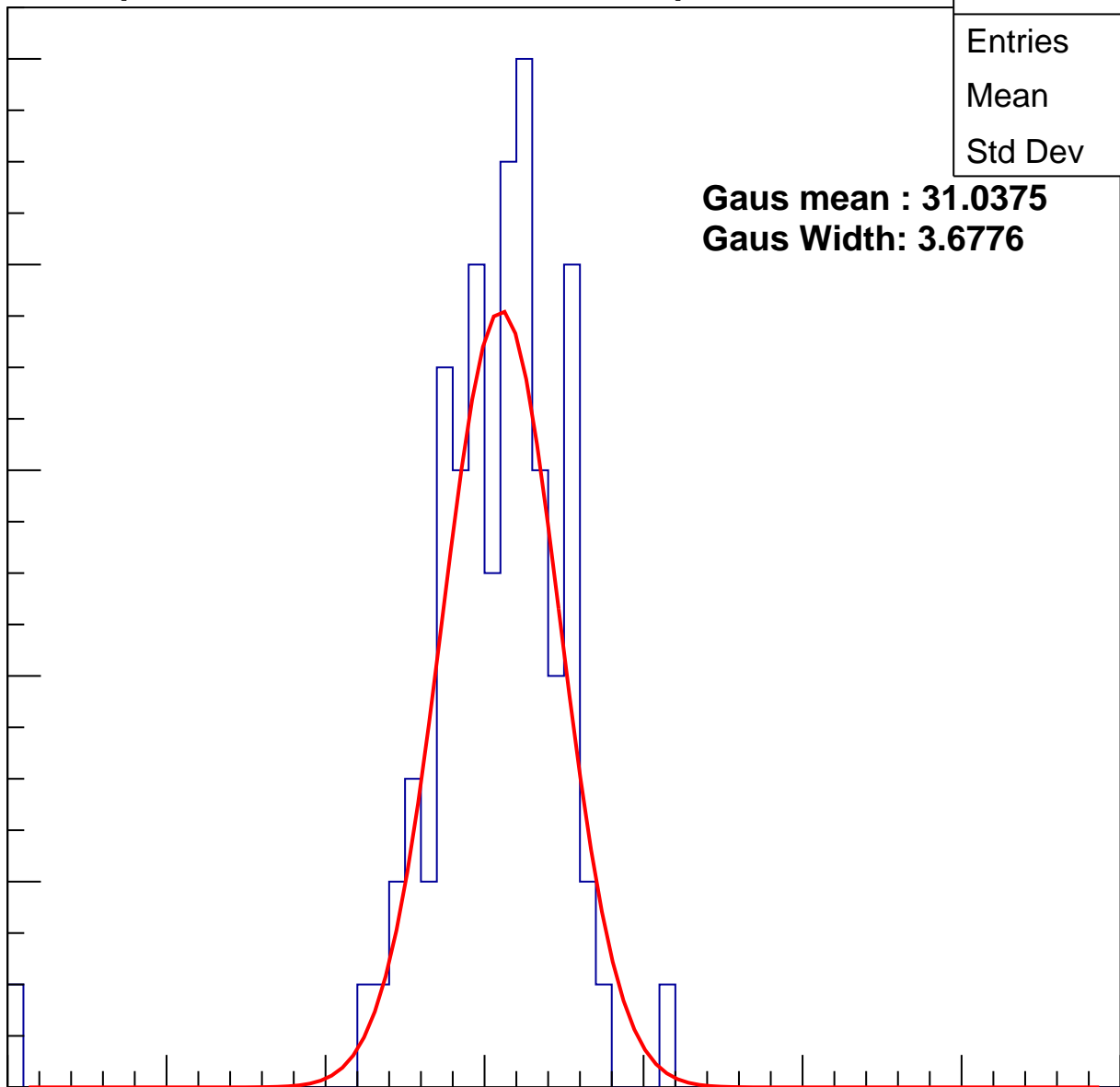
**Gaus Width: 3.6776**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U20-ch109, adc1

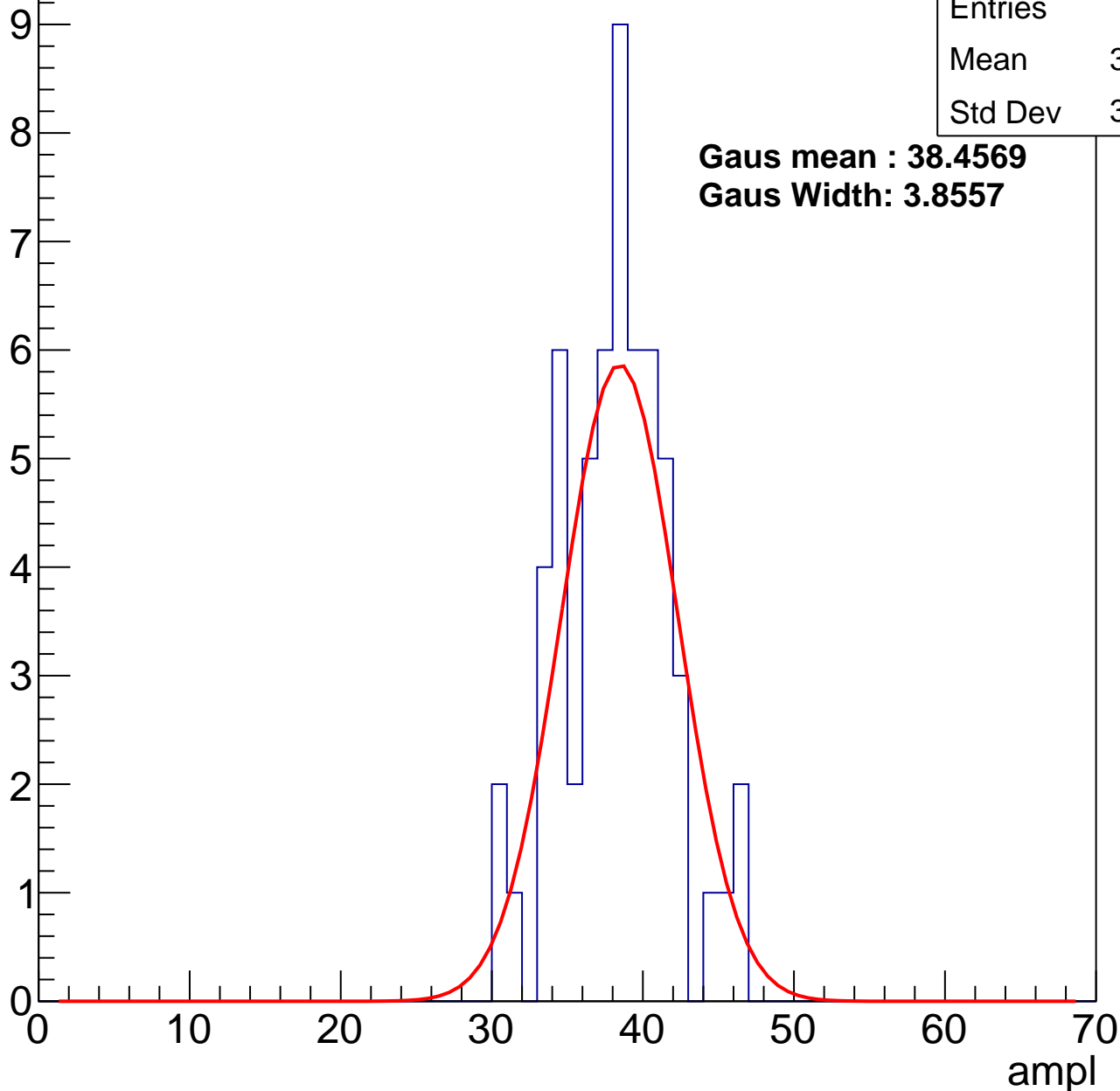
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	59
Mean	37.75
Std Dev	3.563

**Gaus mean : 38.4569**

**Gaus Width: 3.8557**



# B1L101S, U20-ch109, adc2

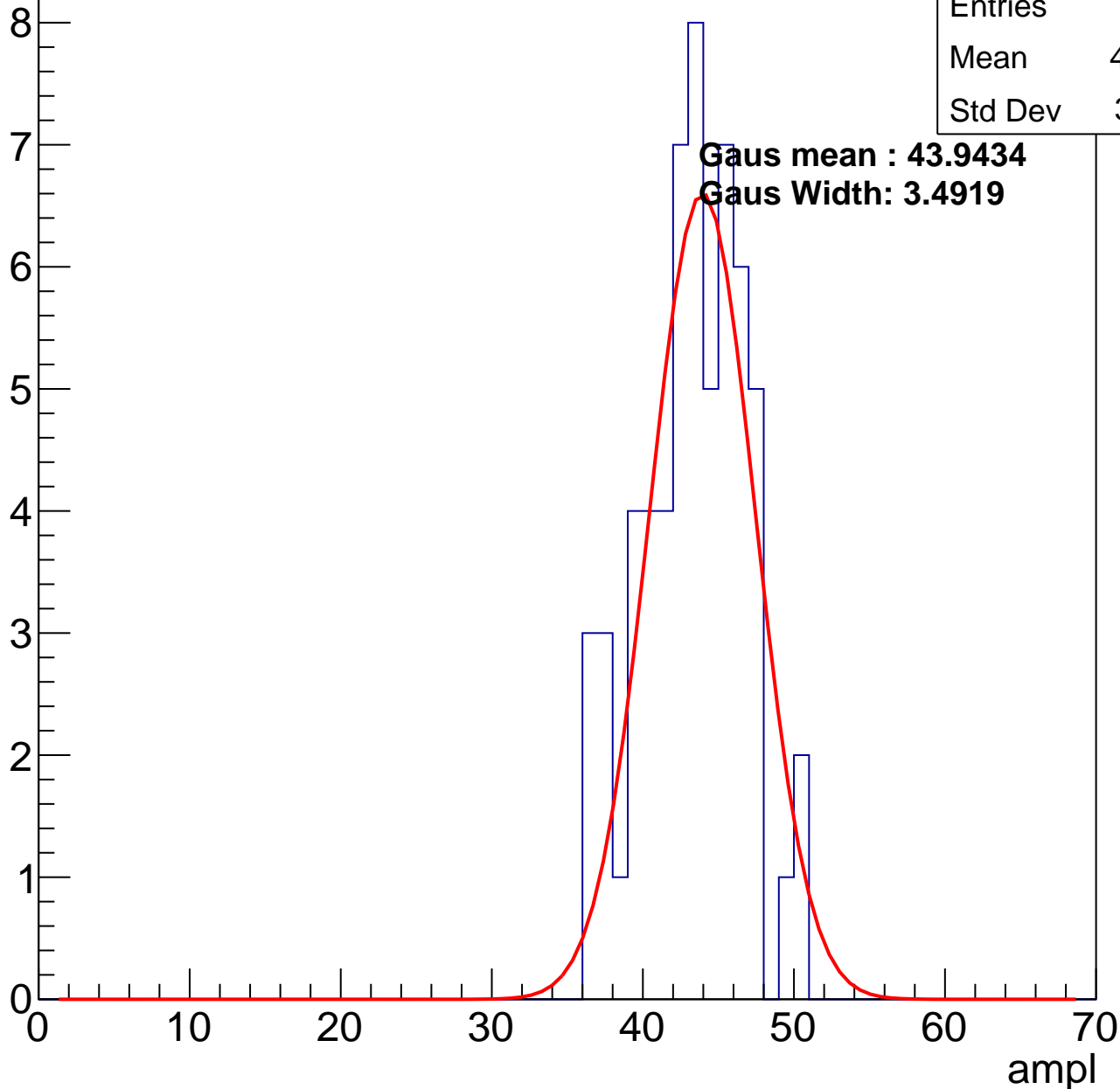
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	60
Mean	42.83
Std Dev	3.421

**Gaus mean : 43.9434**

**Gaus Width: 3.4919**

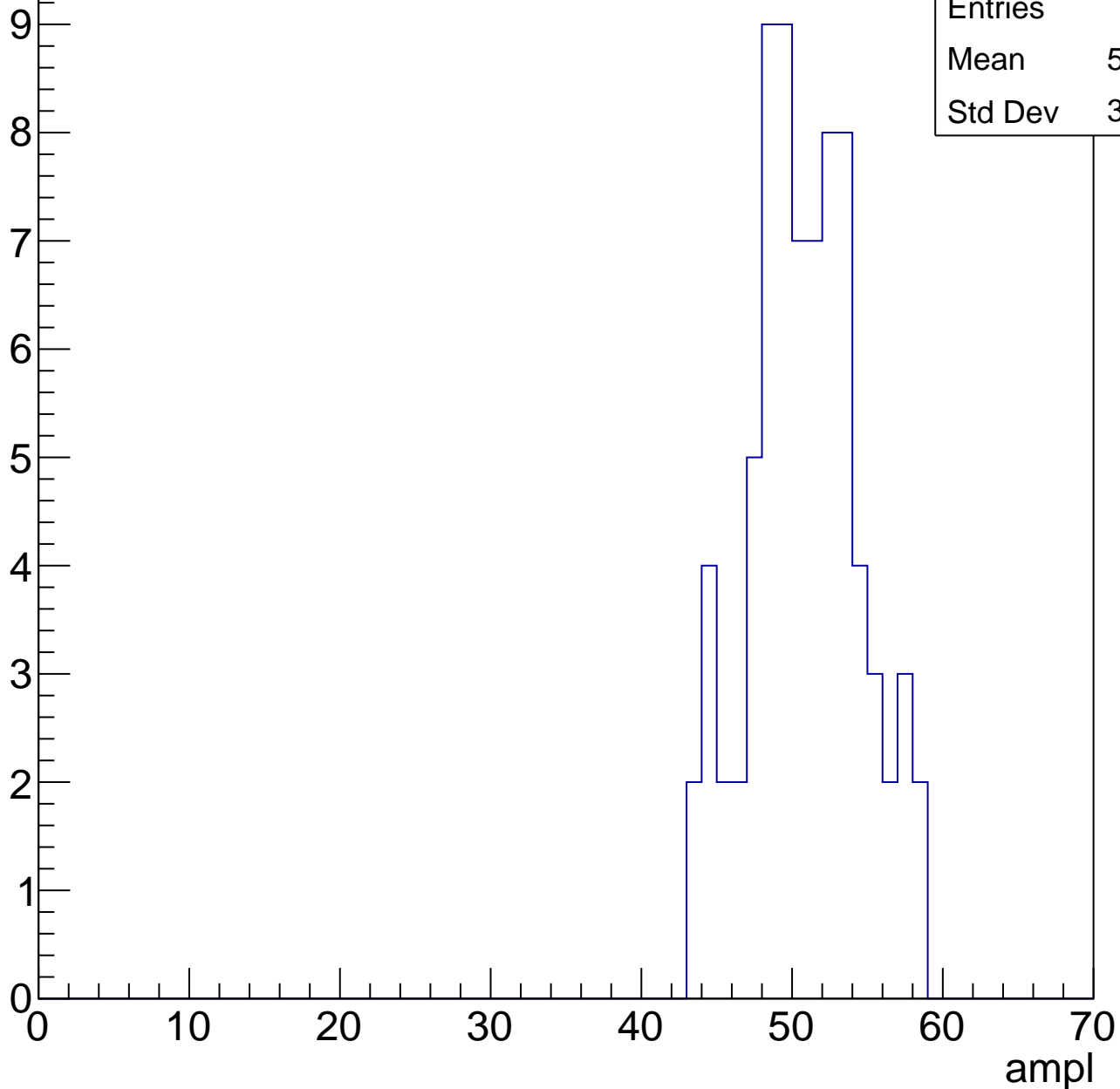


# B1L101S, U20-ch109, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	77
Mean	50.38
Std Dev	3.604

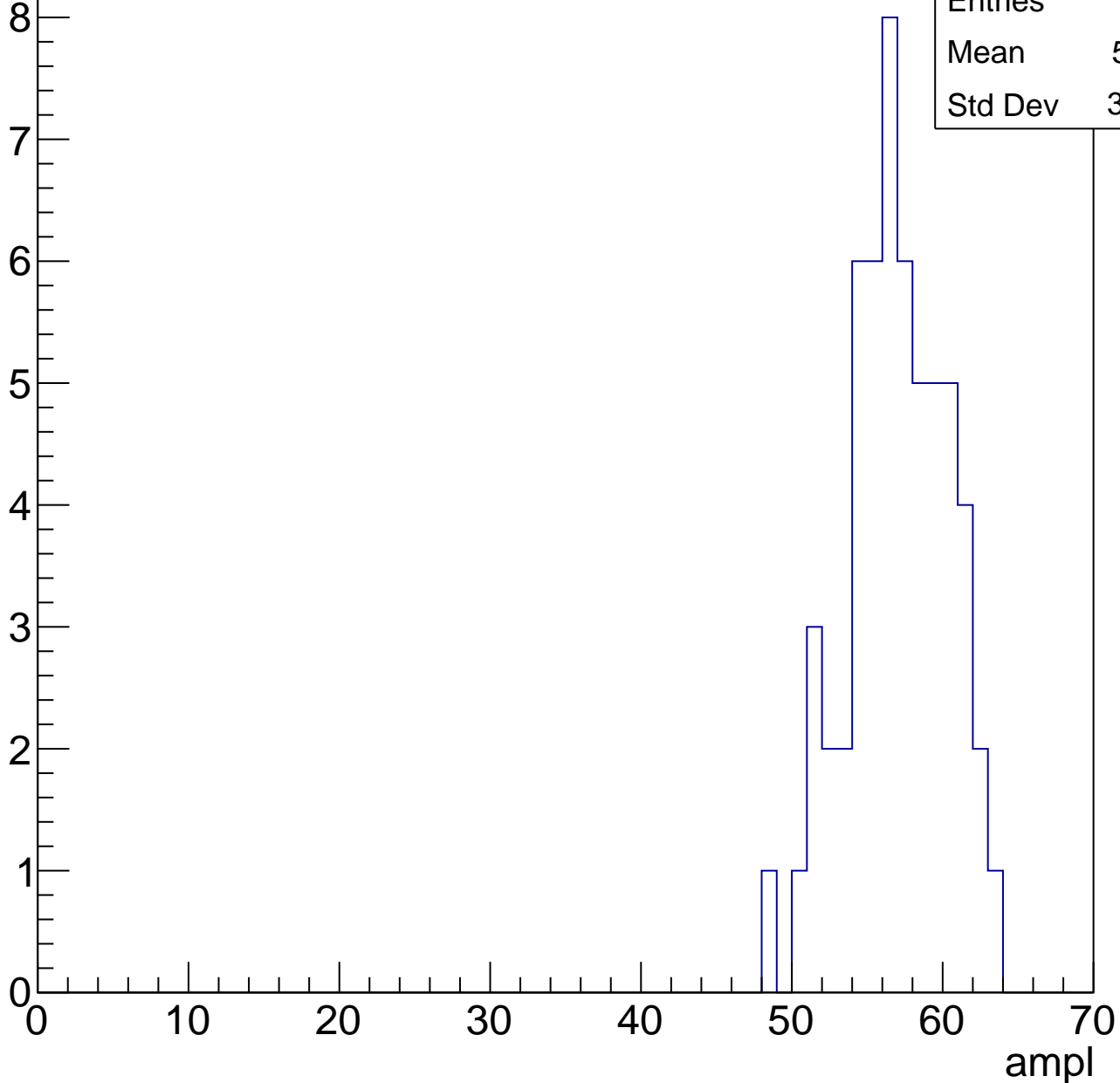


# B1L101S, U20-ch109, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	57
Mean	56.51
Std Dev	3.277

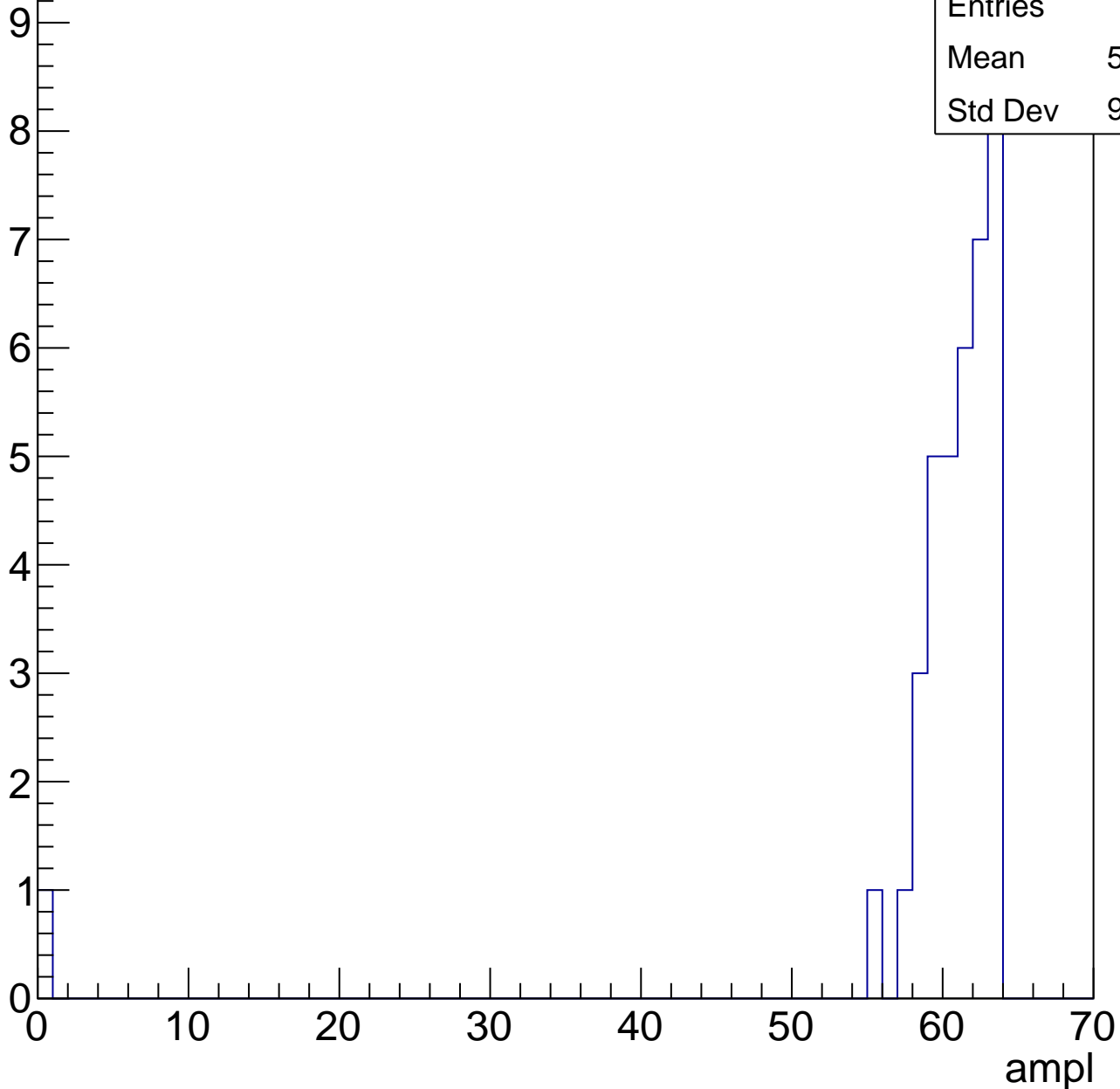


# B1L101S, U20-ch109, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	38
Mean	59.16
Std Dev	9.919



# B1L101S, U20-ch109, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U20-ch109, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L101S, U20-ch110, adc0

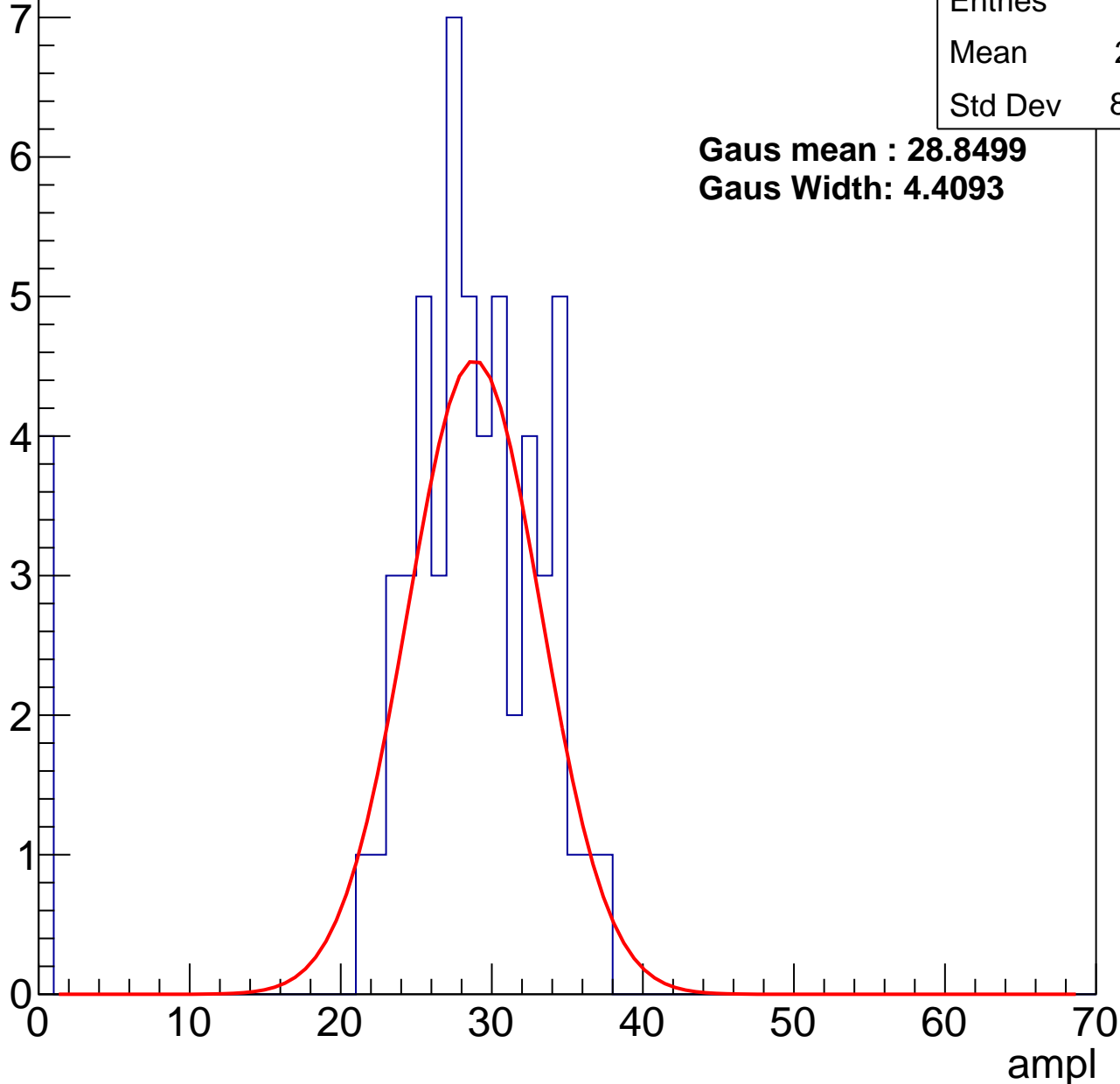
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	58
Mean	26.71
Std Dev	8.164

**Gaus mean : 28.8499**

**Gaus Width: 4.4093**



# B1L101S, U20-ch110, adc1

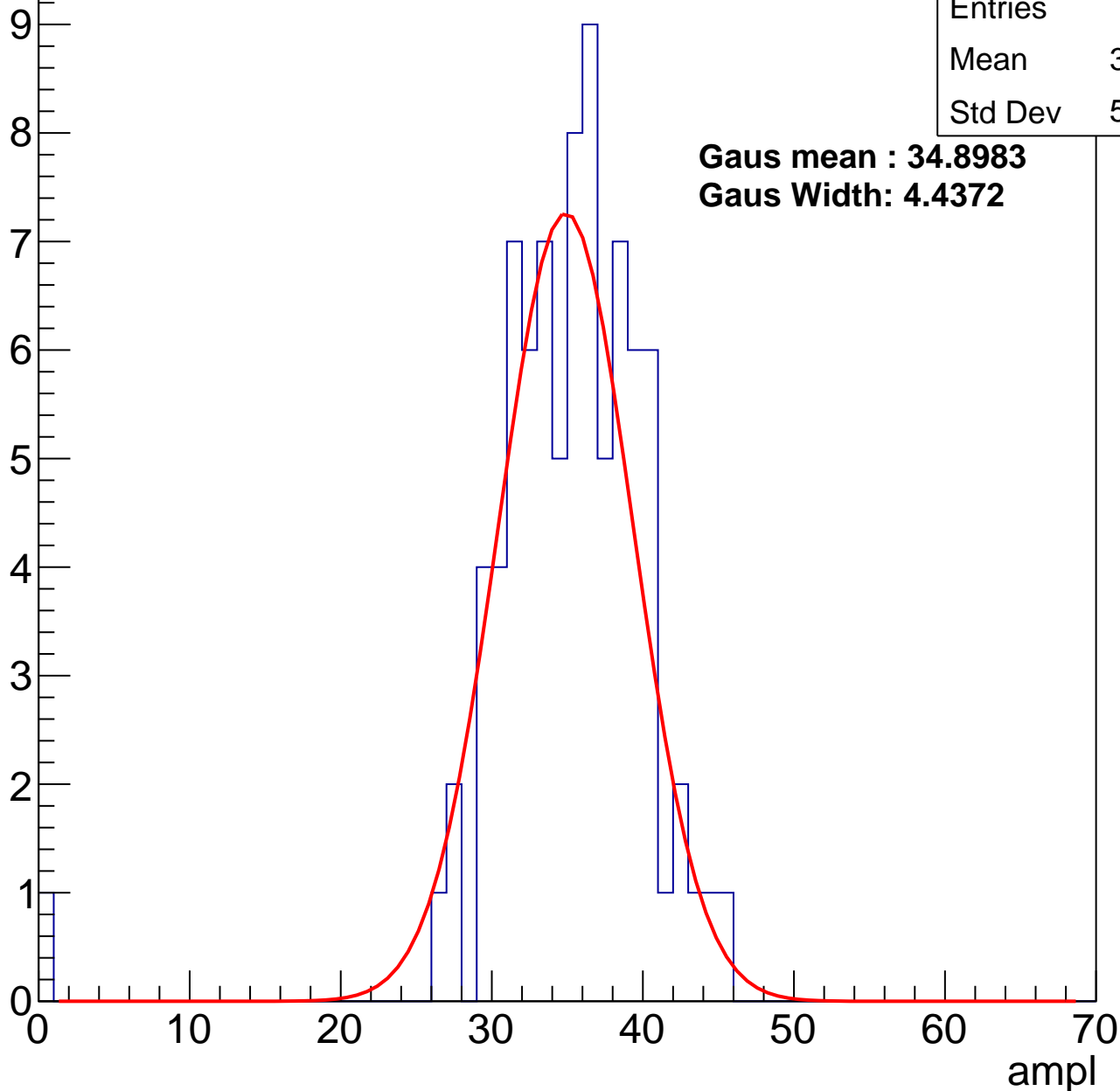
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	84
Mean	34.67
Std Dev	5.547

**Gaus mean : 34.8983**

**Gaus Width: 4.4372**



# B1L101S, U20-ch110, adc2

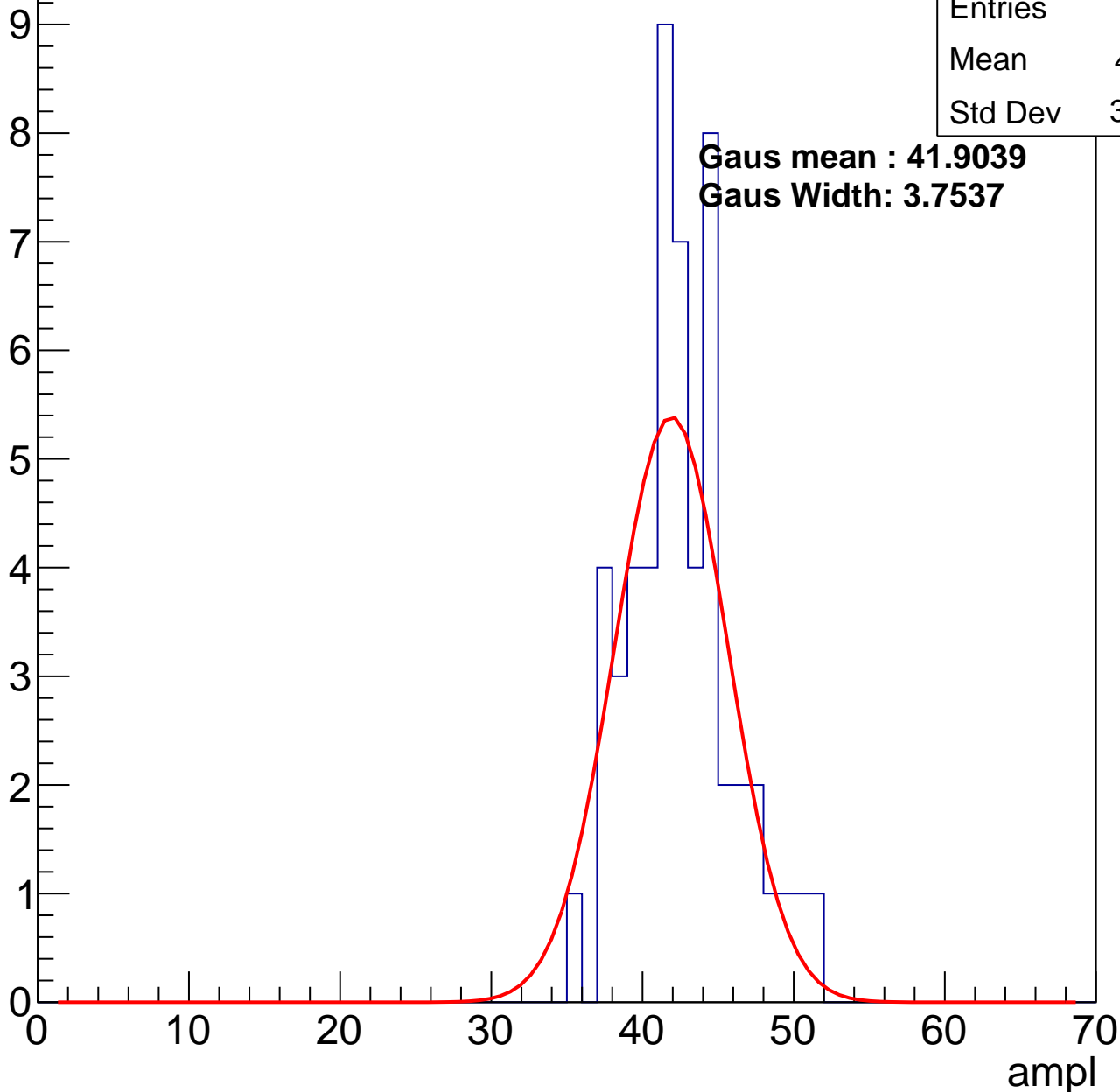
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	54
Mean	42.11
Std Dev	3.398

**Gaus mean : 41.9039**

**Gaus Width: 3.7537**

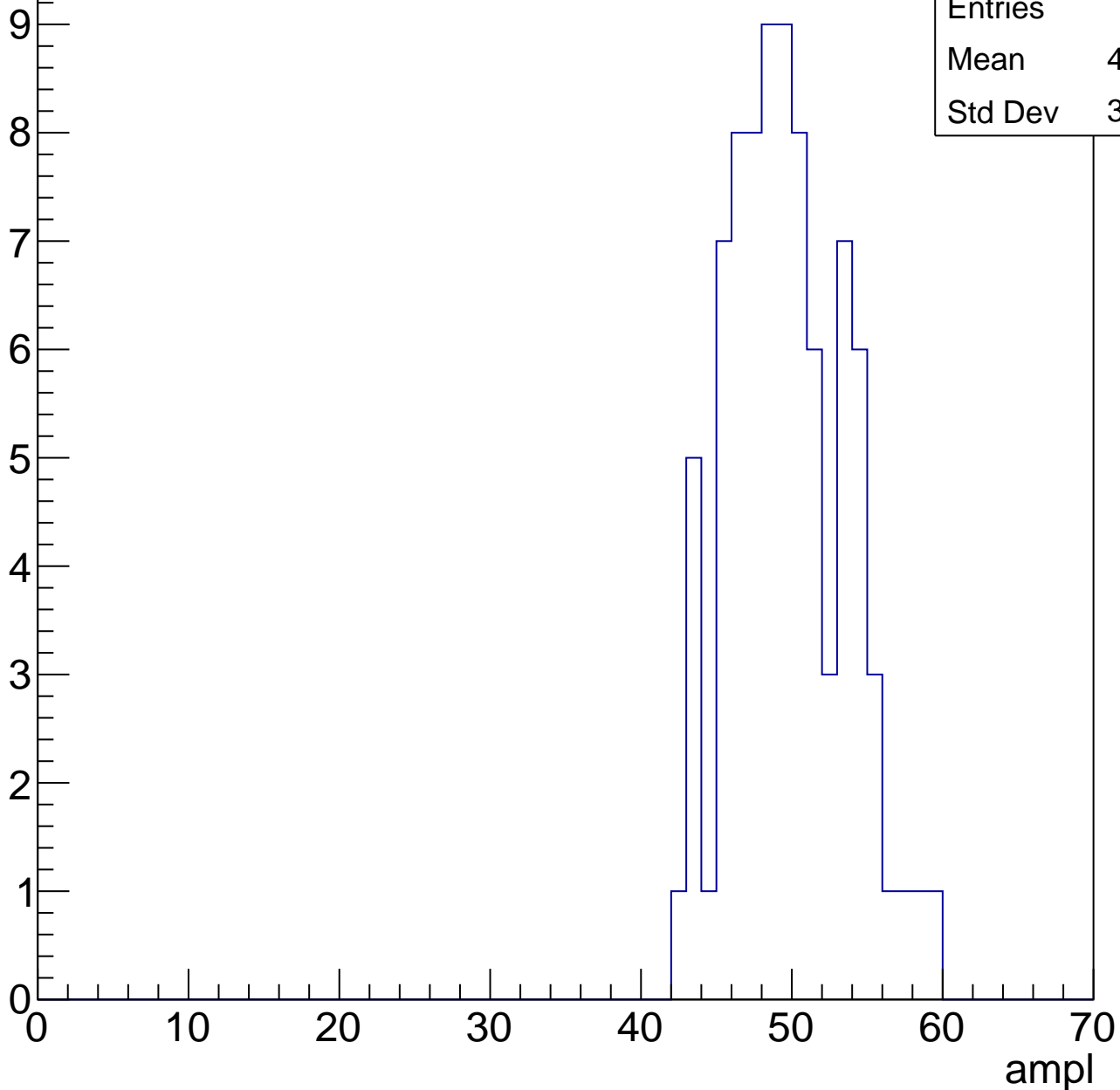


# B1L101S, U20-ch110, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	85
Mean	49.24
Std Dev	3.753



# B1L101S, U20-ch110, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

6

5

4

3

2

1

0

Entries	43
Mean	55.3
Std Dev	2.93

ampl

0

10

20

30

40

50

60

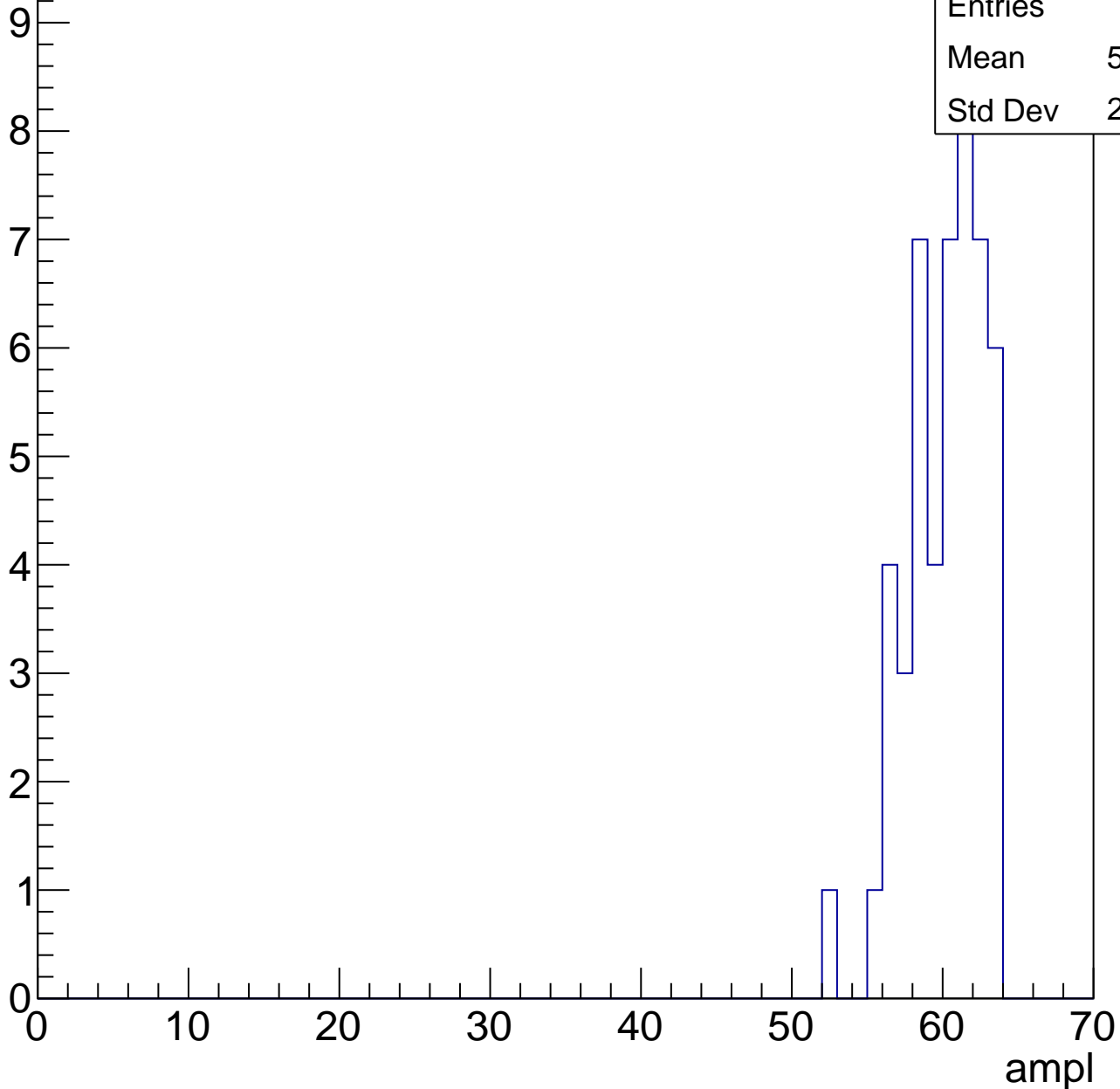
70

# B1L101S, U20-ch110, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

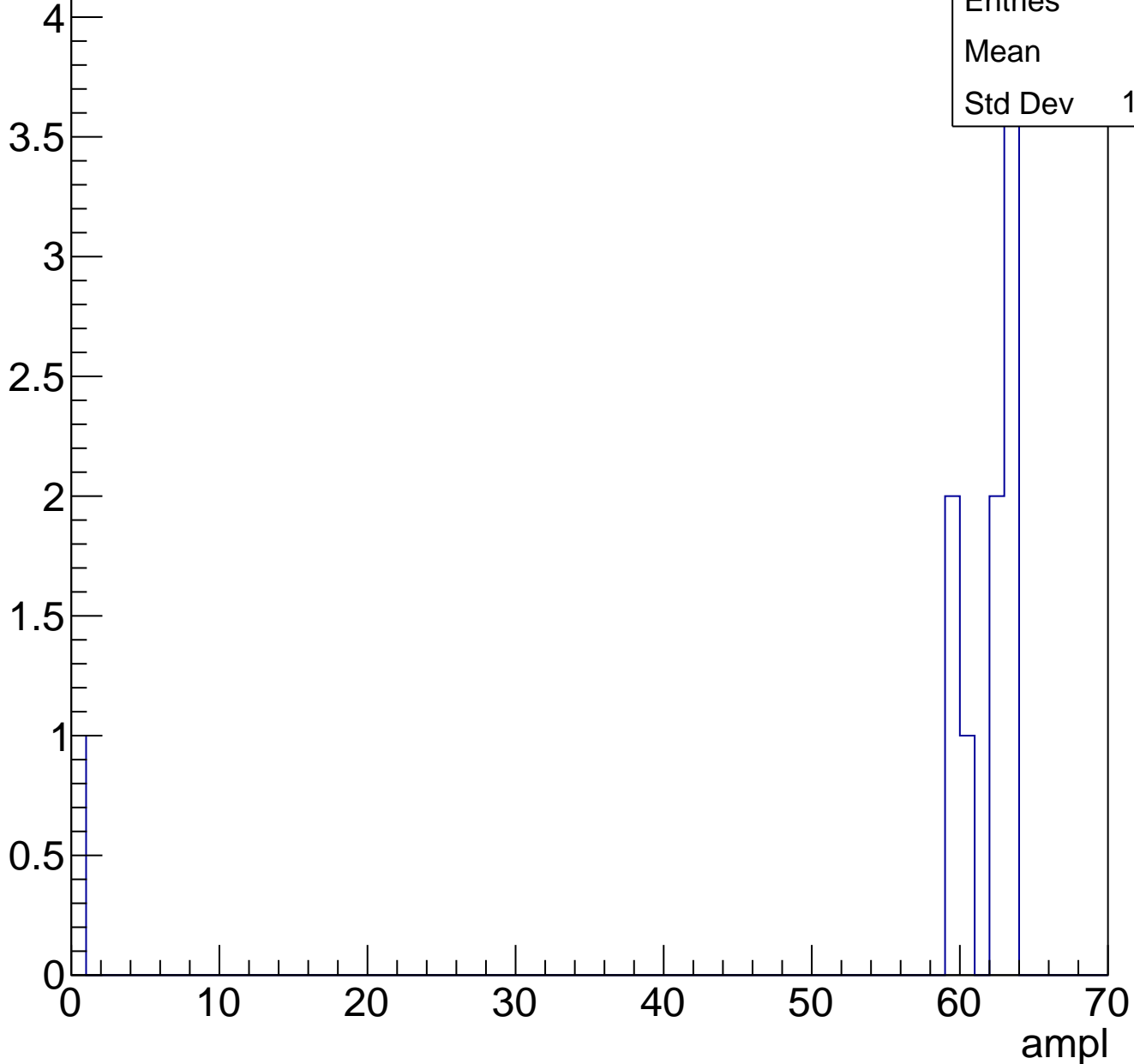
Entries	49
Mean	59.69
Std Dev	2.468



# B1L101S, U20-ch110, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U20-ch110, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U20-ch111, adc0

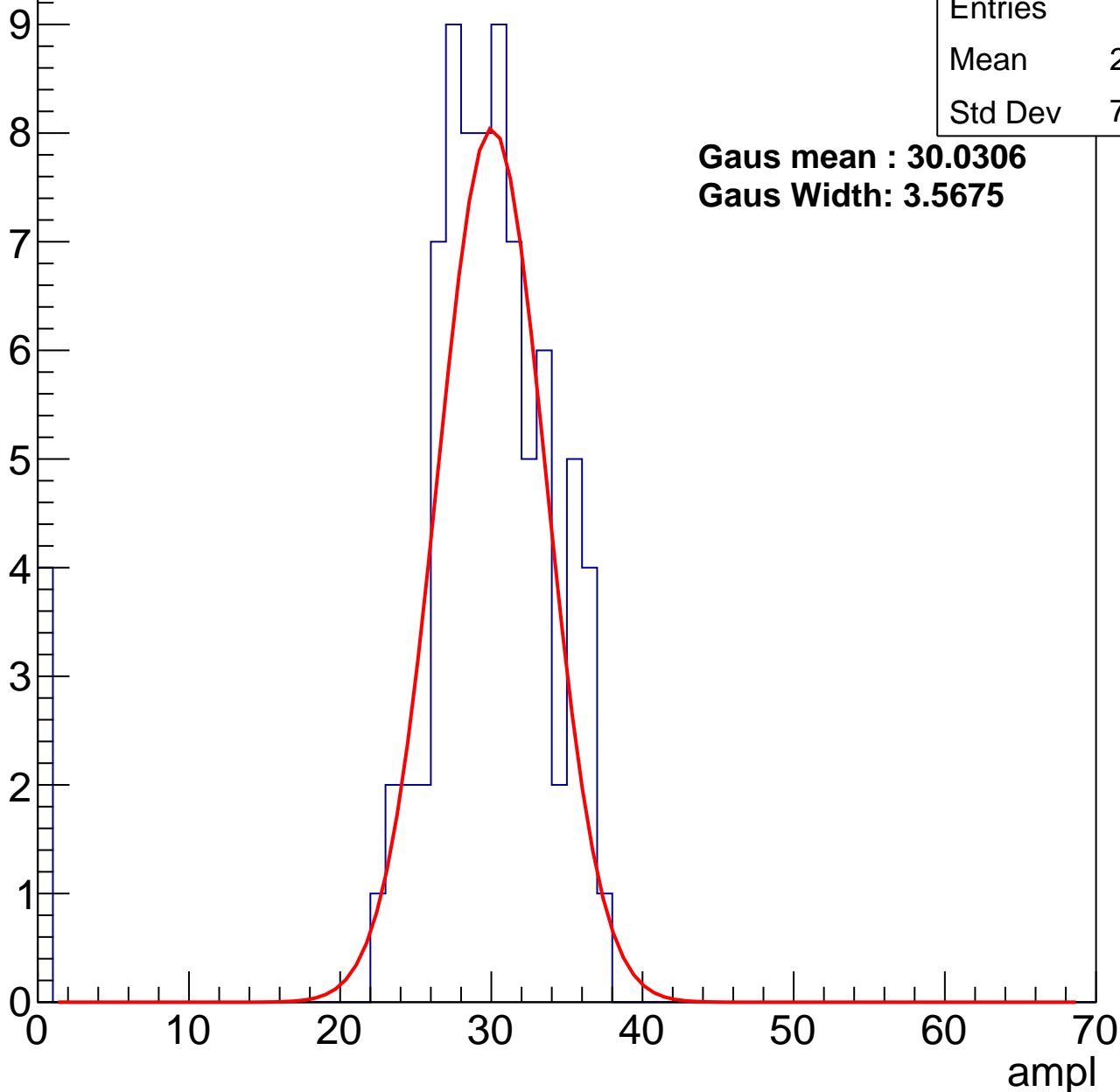
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	82
Mean	28.24
Std Dev	7.237

**Gaus mean : 30.0306**

**Gaus Width: 3.5675**



# B1L101S, U20-ch111, adc1

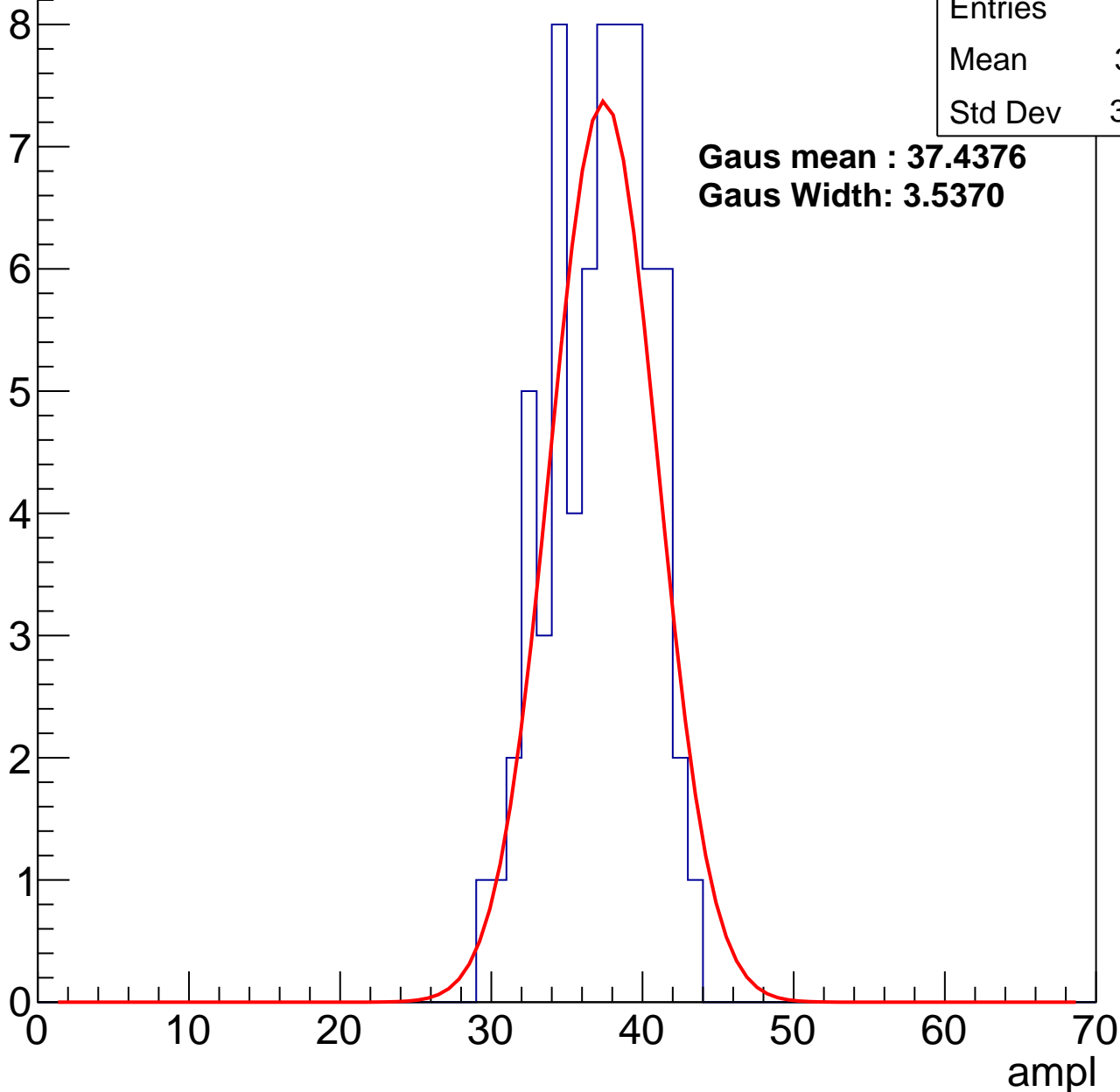
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	36.71
Std Dev	3.235

**Gaus mean : 37.4376**

**Gaus Width: 3.5370**



# B1L101S, U20-ch111, adc2

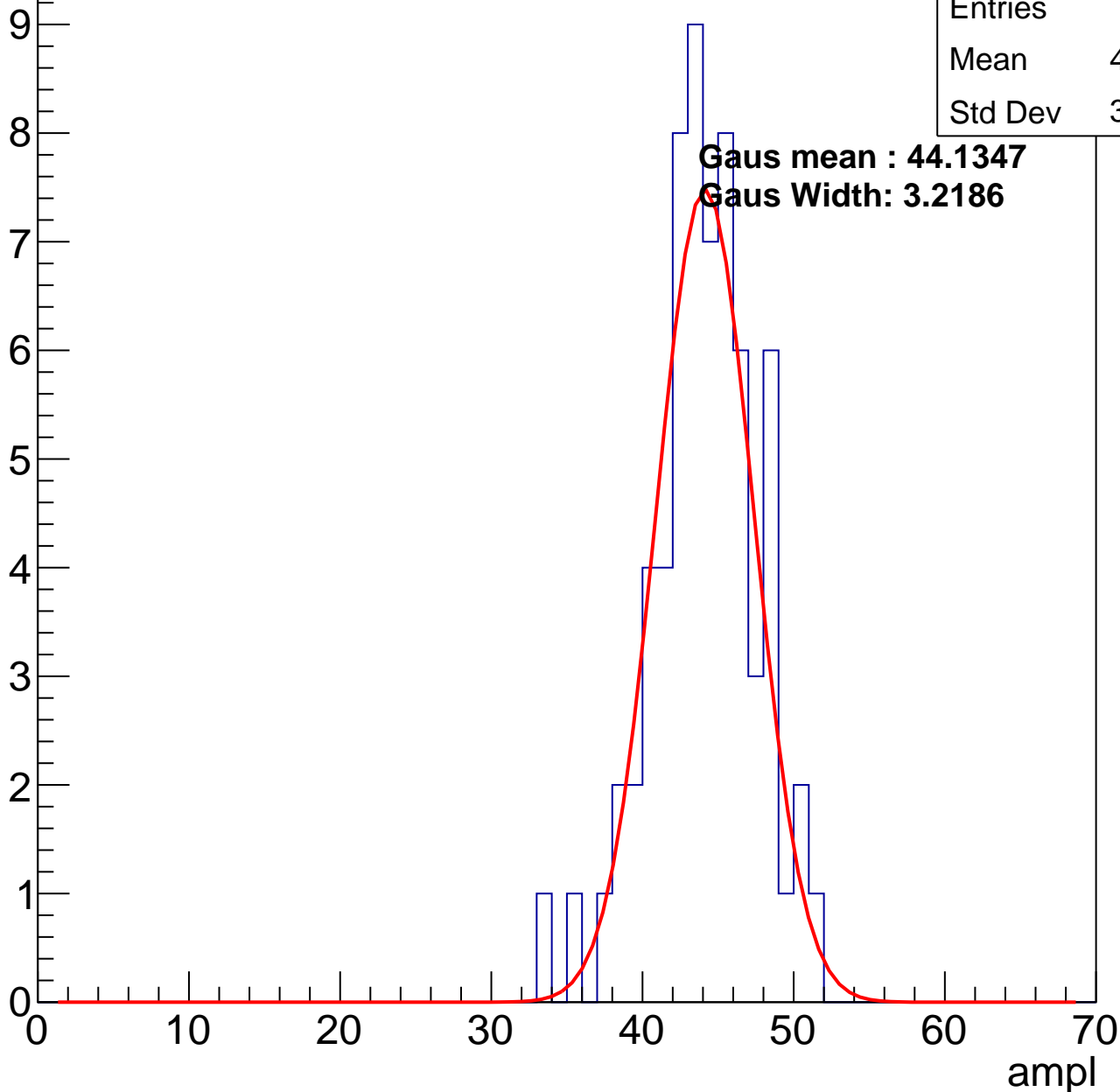
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	66
Mean	43.62
Std Dev	3.494

**Gaus mean : 44.1347**

**Gaus Width: 3.2186**

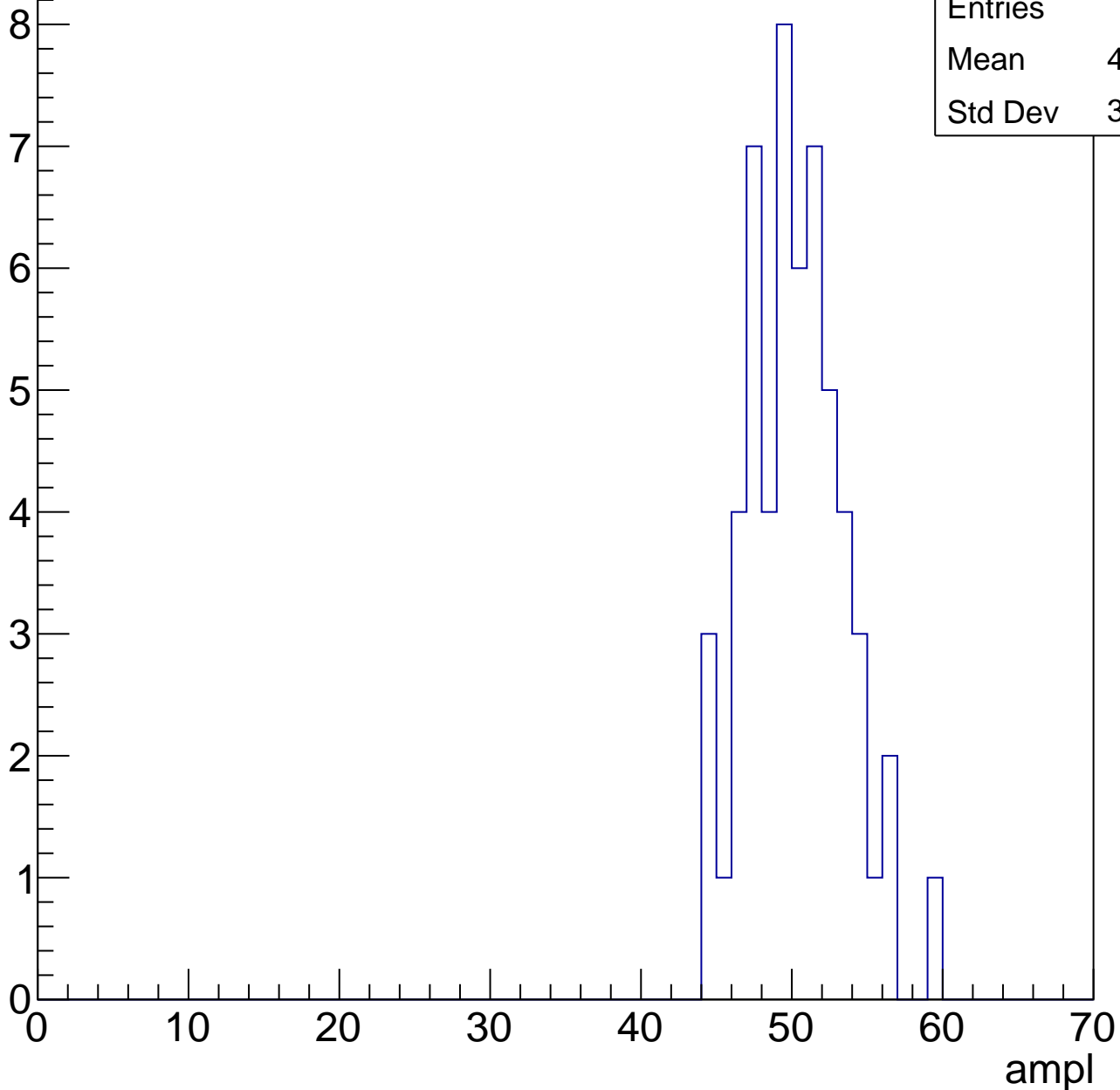


# B1L101S, U20-ch111, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	56
Mean	49.84
Std Dev	3.195

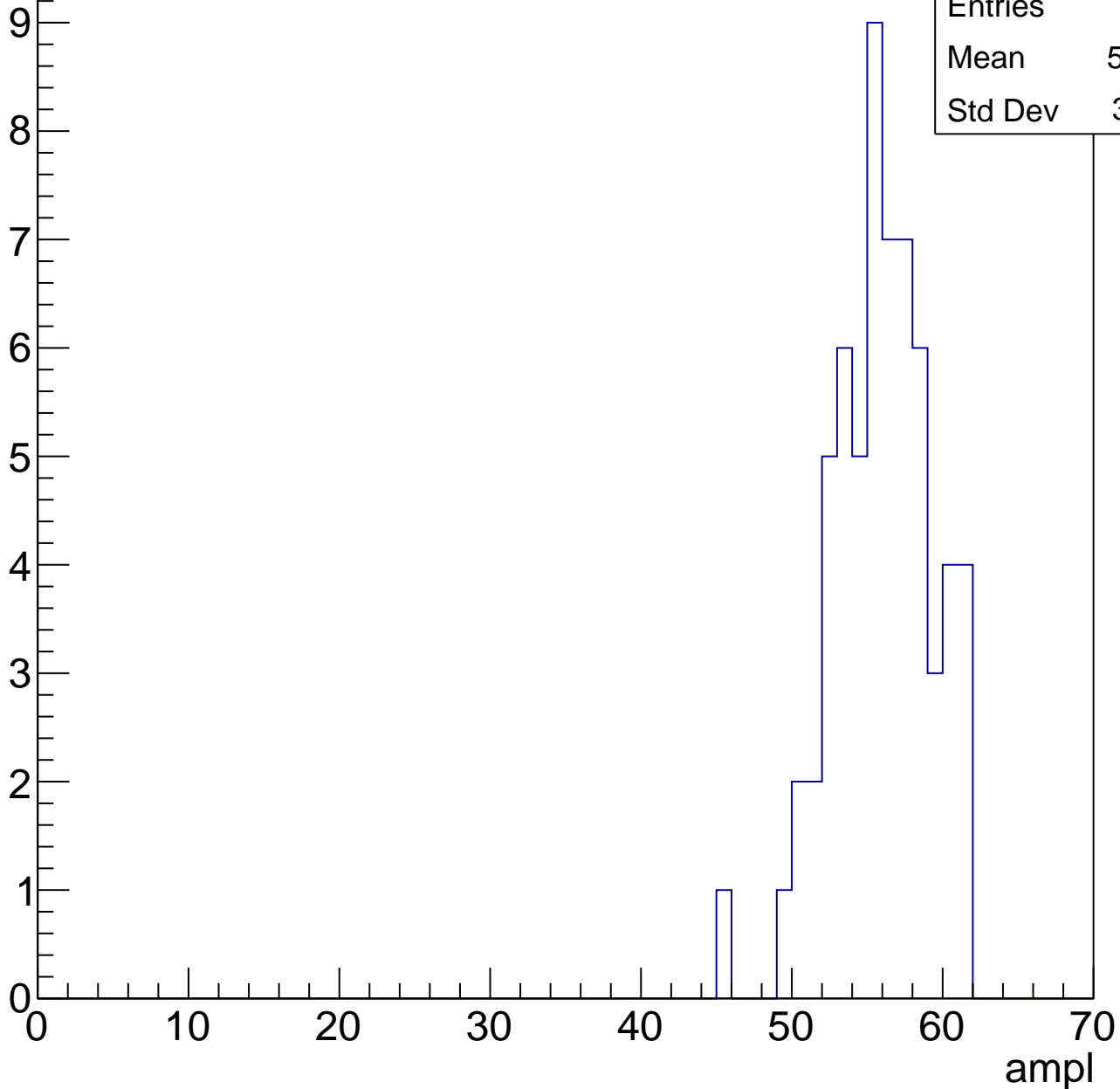


# B1L101S, U20-ch111, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	55.47
Std Dev	3.261

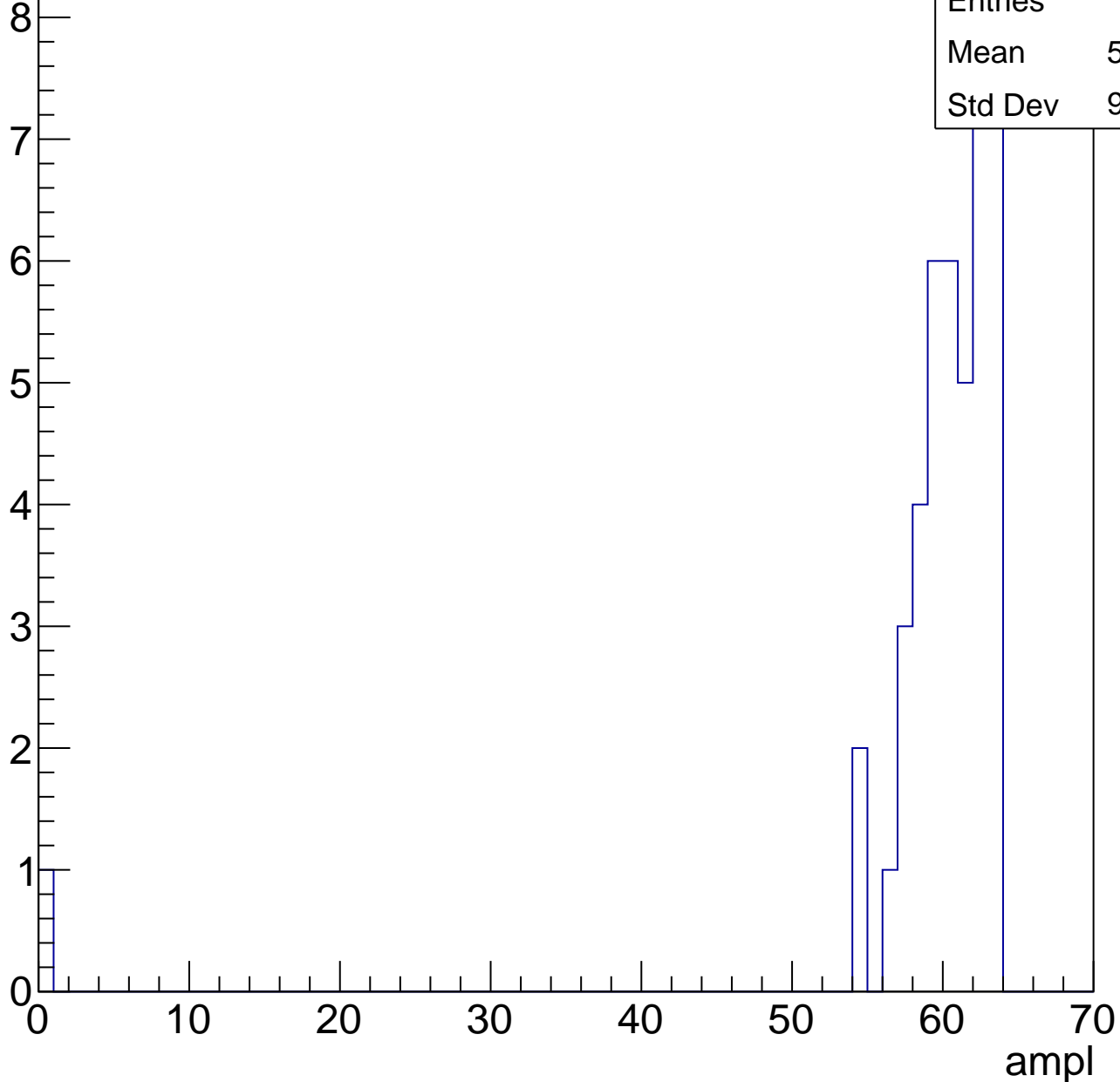


# B1L101S, U20-ch111, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	44
Mean	58.77
Std Dev	9.268



# B1L101S, U20-ch111, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	5
Mean	62.2
Std Dev	0.7483

ampl

0 10 20 30 40 50 60 70



# B1L101S, U20-ch111, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U20-ch112, adc0

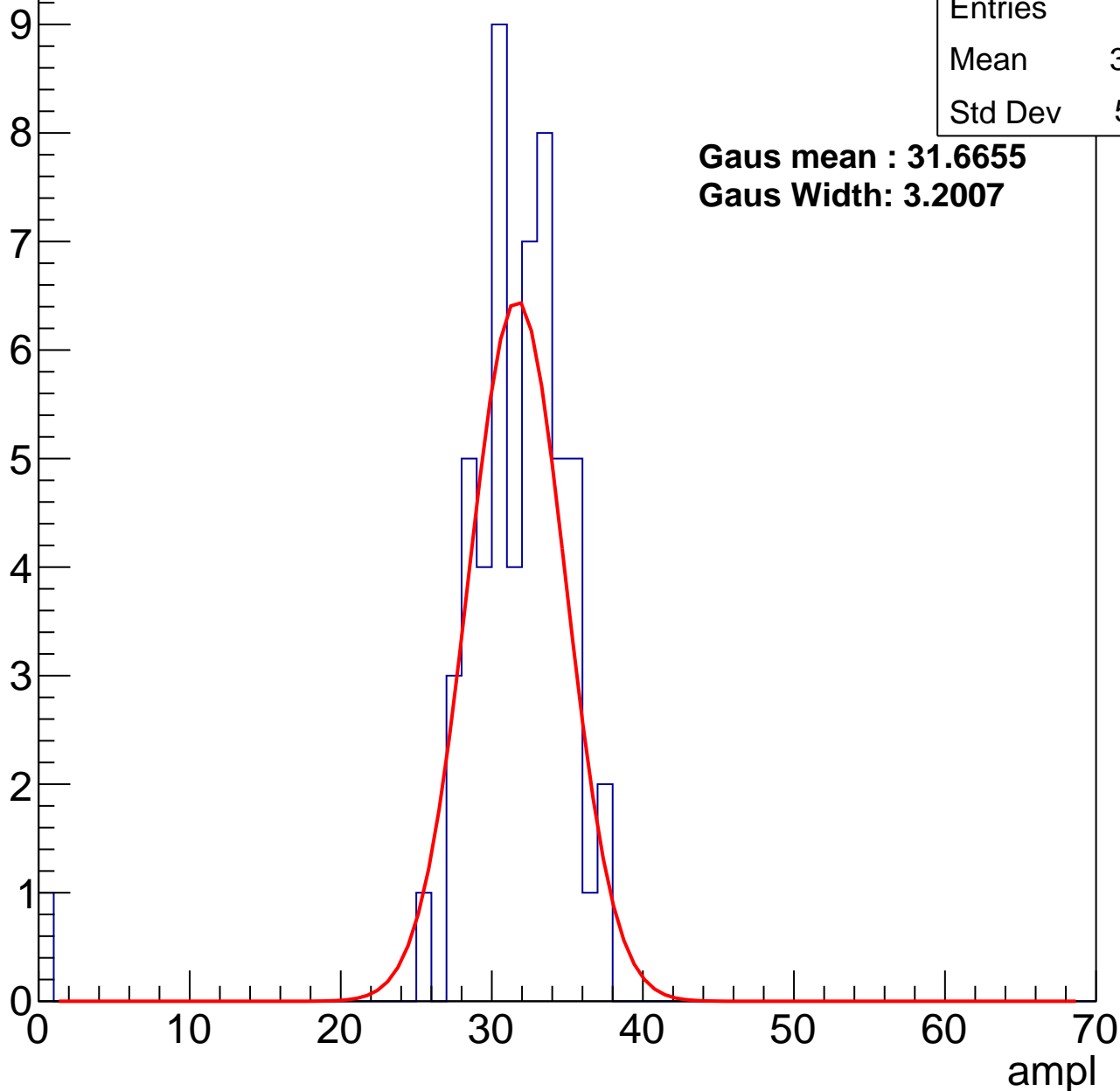
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	55
Mean	30.89
Std Dev	5.001

**Gaus mean : 31.6655**

**Gaus Width: 3.2007**



# B1L101S, U20-ch112, adc1

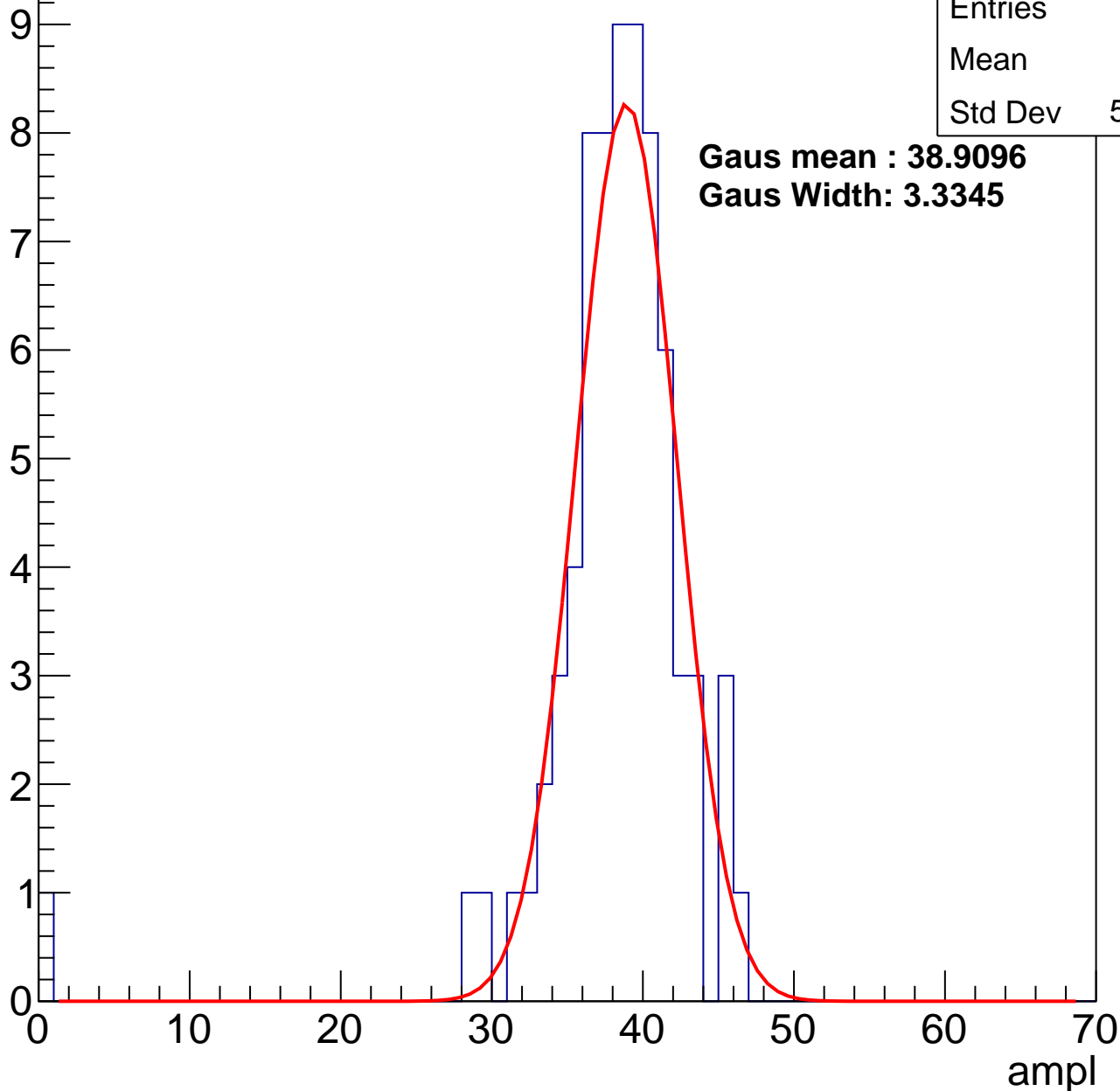
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	72
Mean	37.6
Std Dev	5.654

**Gaus mean : 38.9096**

**Gaus Width: 3.3345**



# B1L101S, U20-ch112, adc2

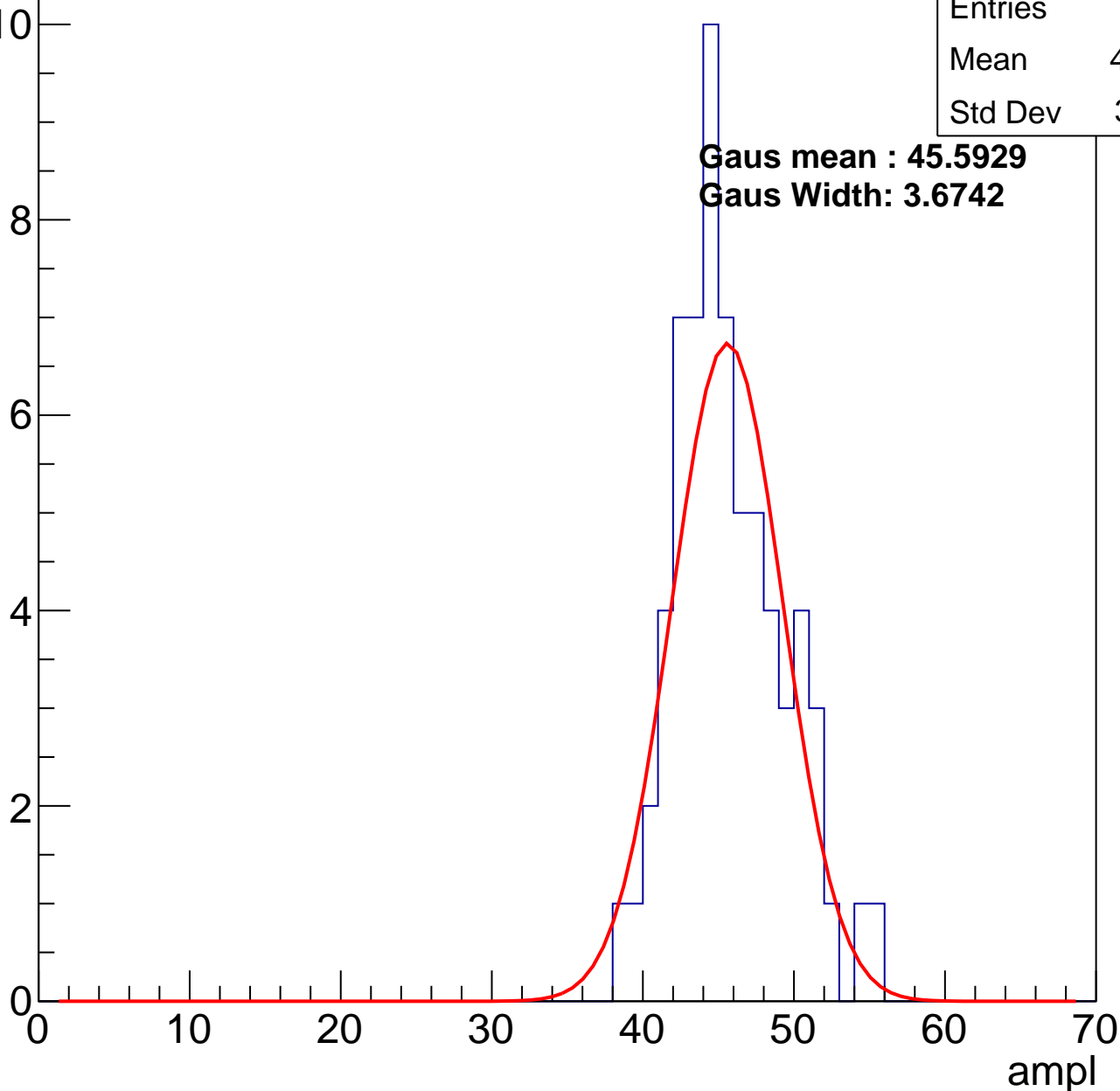
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	66
Mean	45.29
Std Dev	3.571

**Gaus mean : 45.5929**

**Gaus Width: 3.6742**

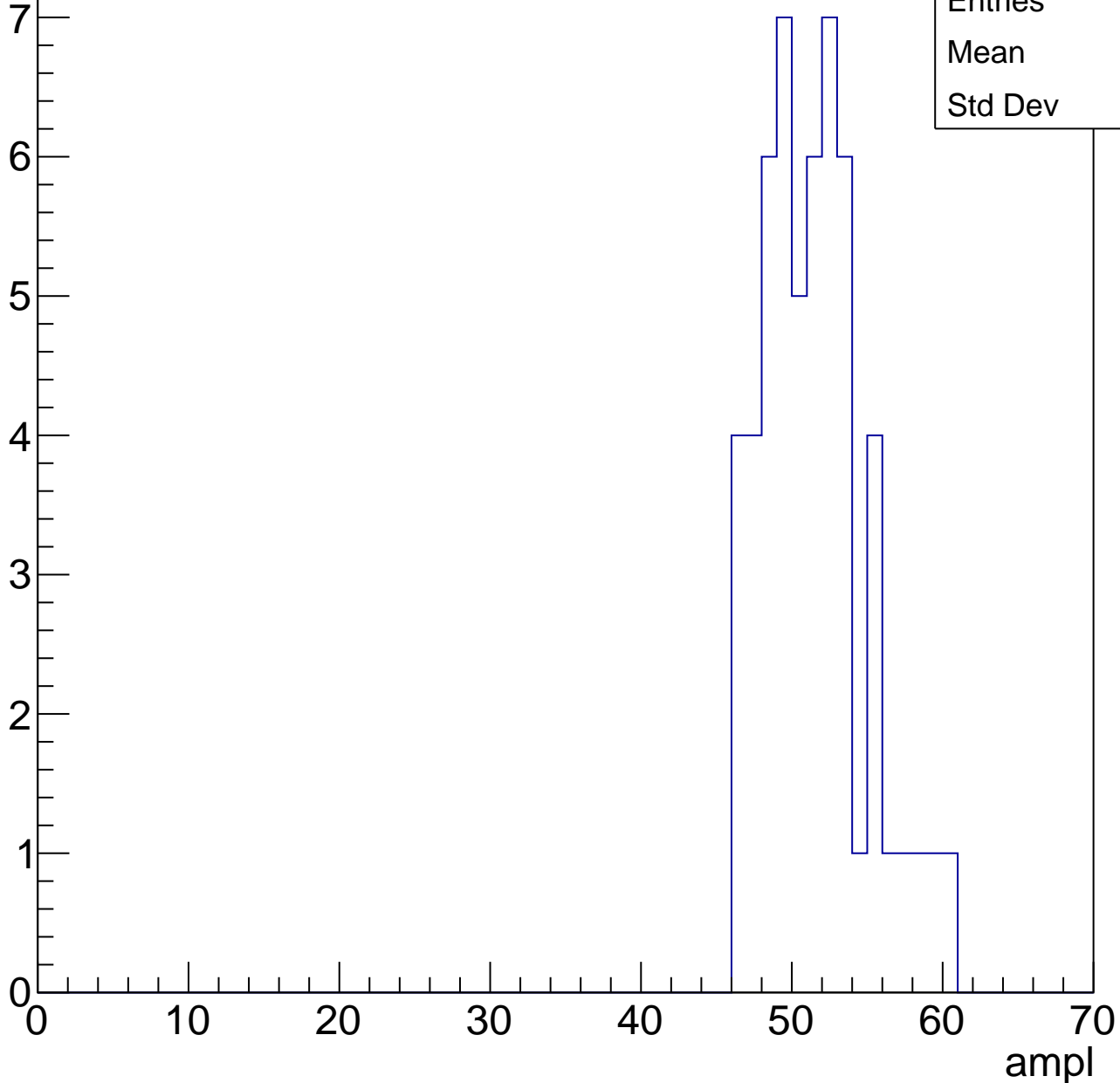


# B1L101S, U20-ch112, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	55
Mean	51
Std Dev	3.33

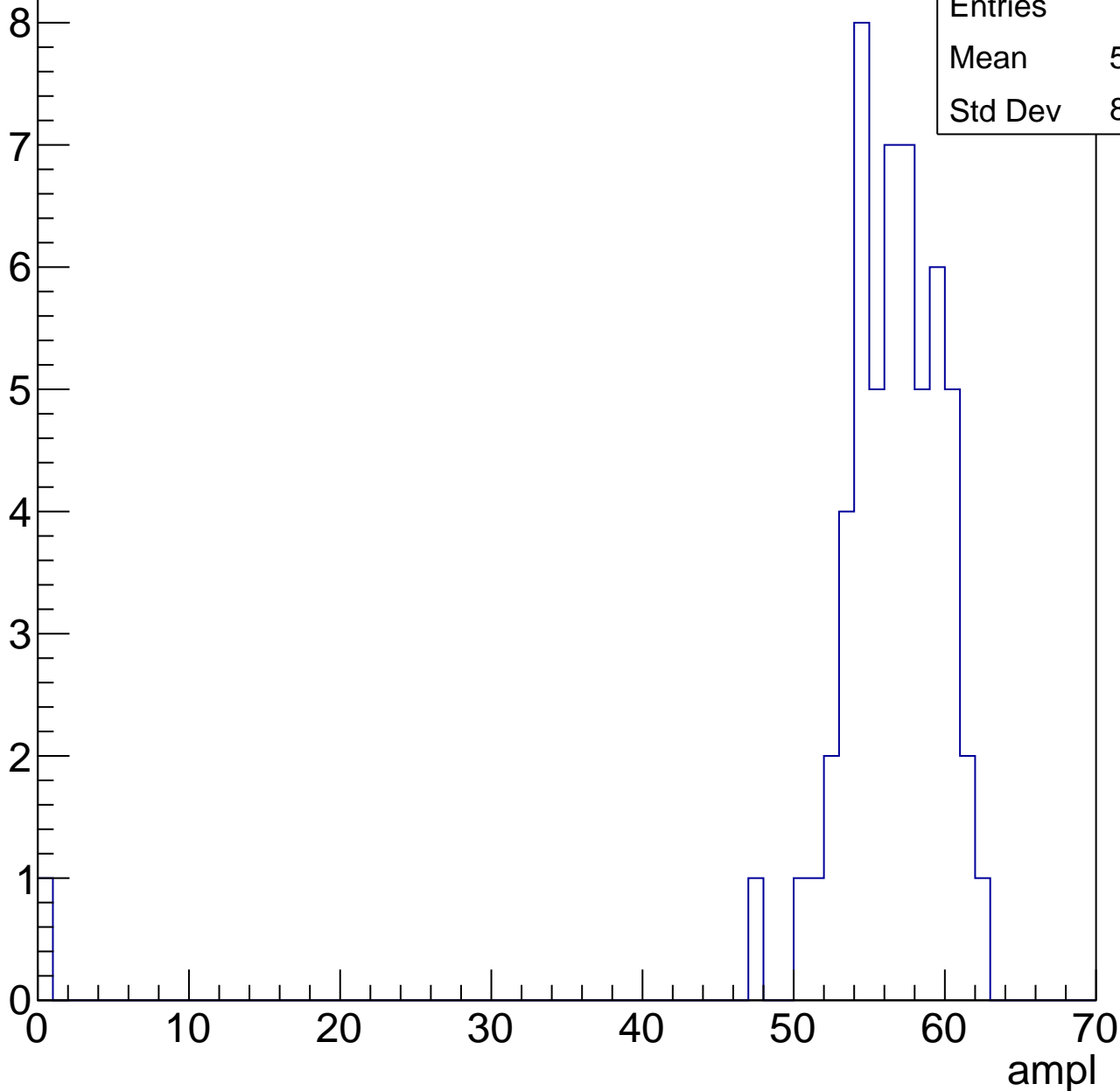


# B1L101S, U20-ch112, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	56
Mean	55.18
Std Dev	8.009

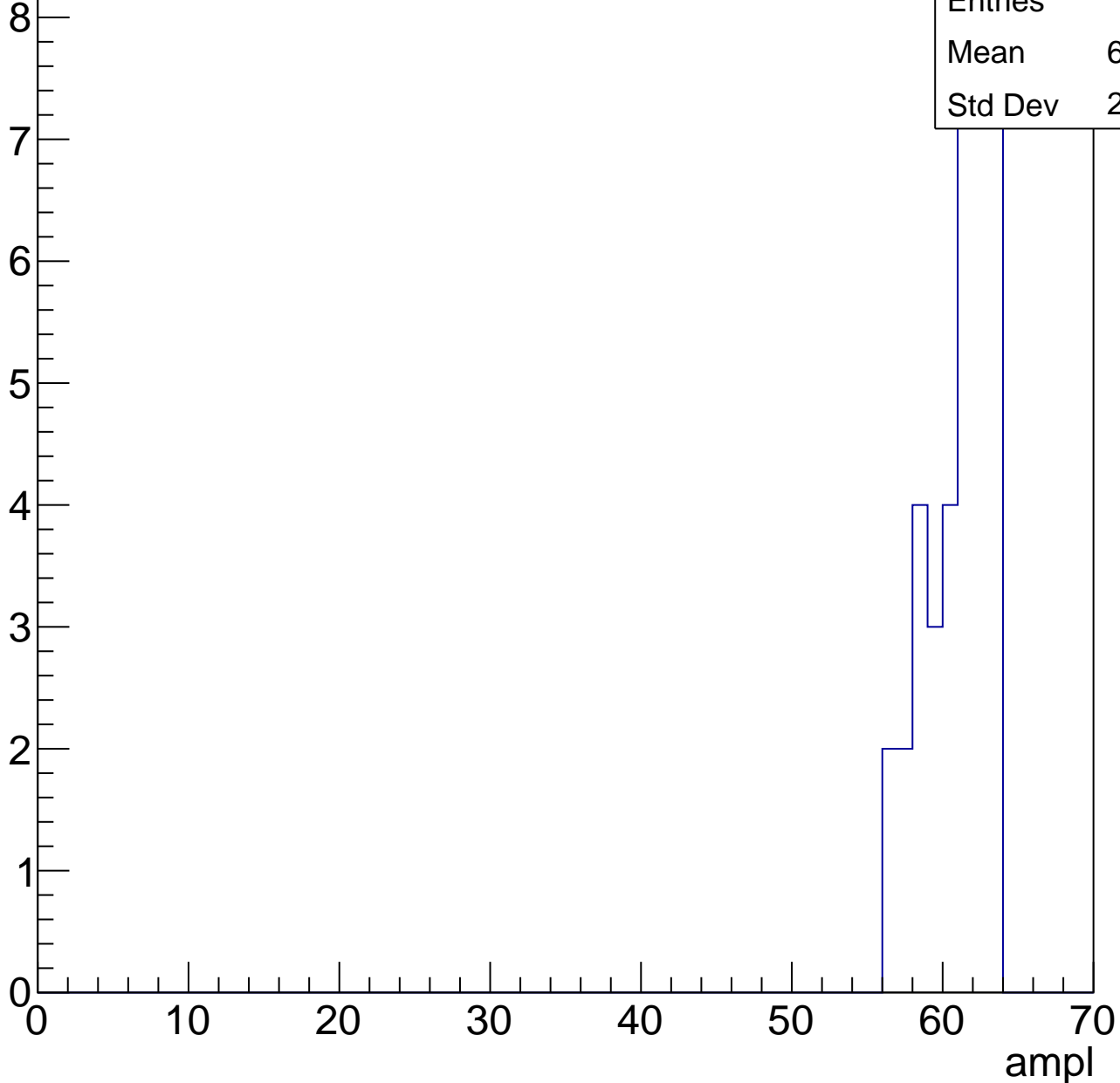


# B1L101S, U20-ch112, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

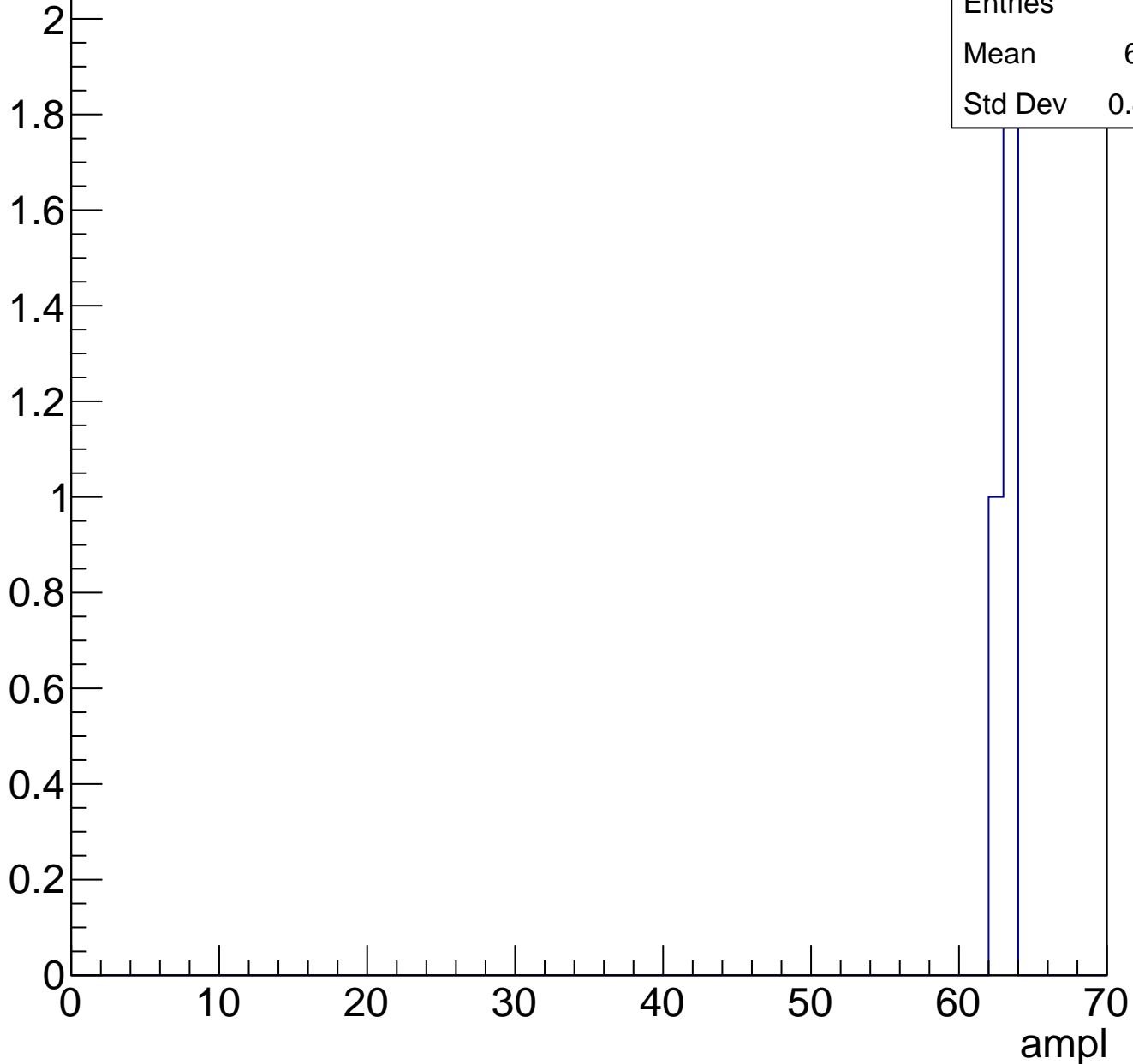
Entries	39
Mean	60.59
Std Dev	2.072



# B1L101S, U20-ch112, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U20-ch112, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L101S, U20-ch113, adc0

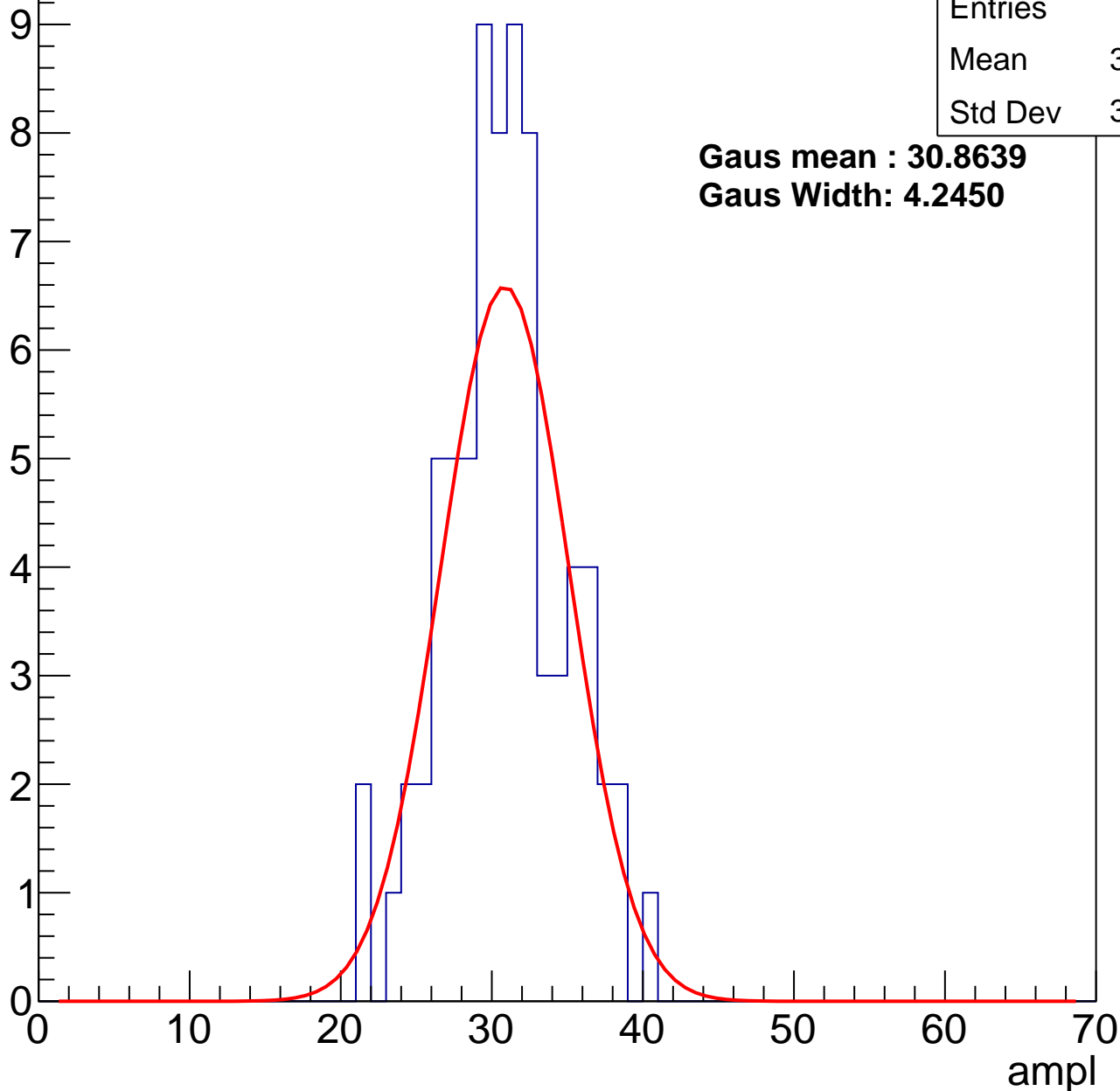
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	75
Mean	30.39
Std Dev	3.936

**Gaus mean : 30.8639**

**Gaus Width: 4.2450**



# B1L101S, U20-ch113, adc1

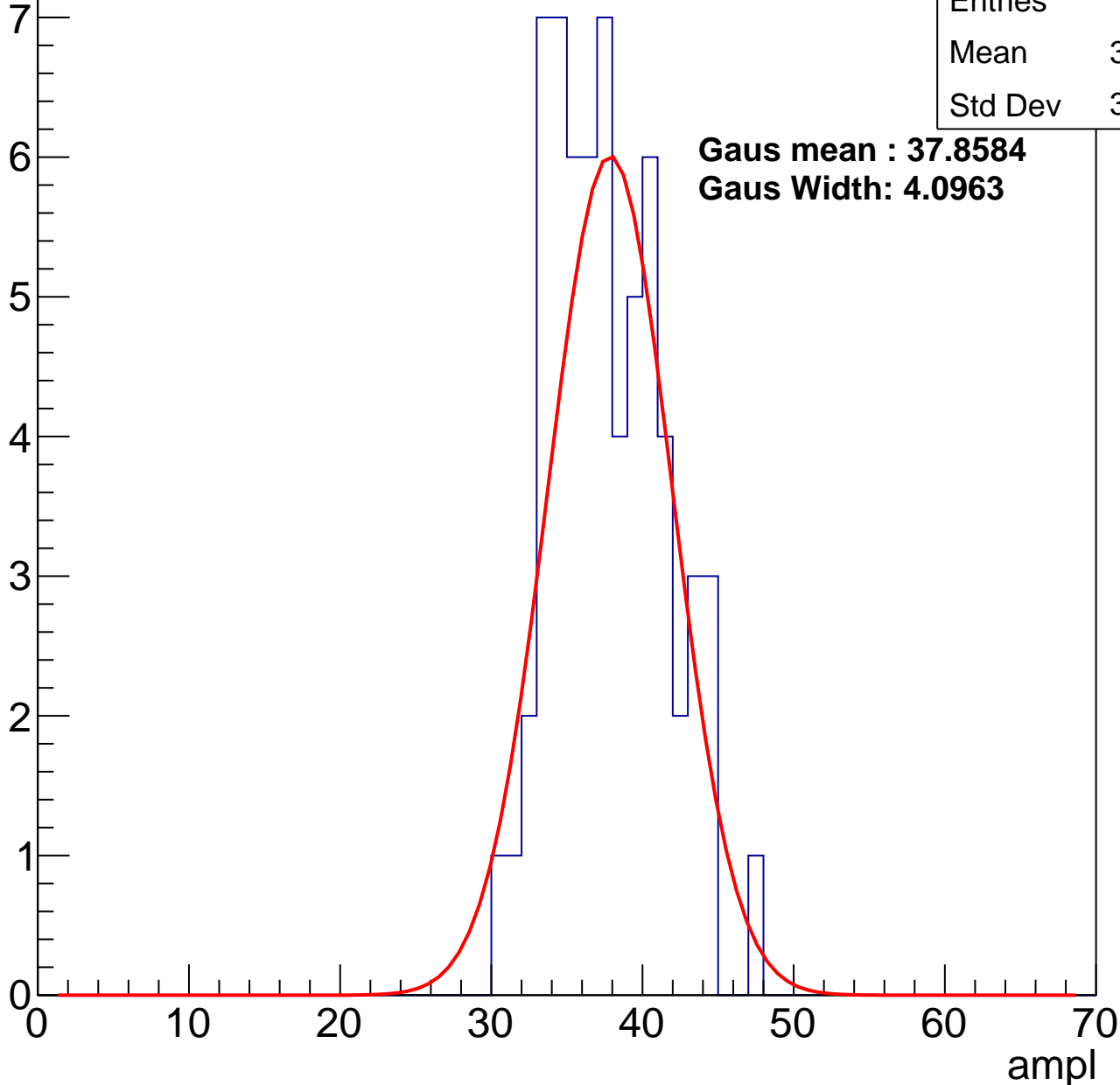
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	37.26
Std Dev	3.685

**Gaus mean : 37.8584**

**Gaus Width: 4.0963**



# B1L101S, U20-ch113, adc2

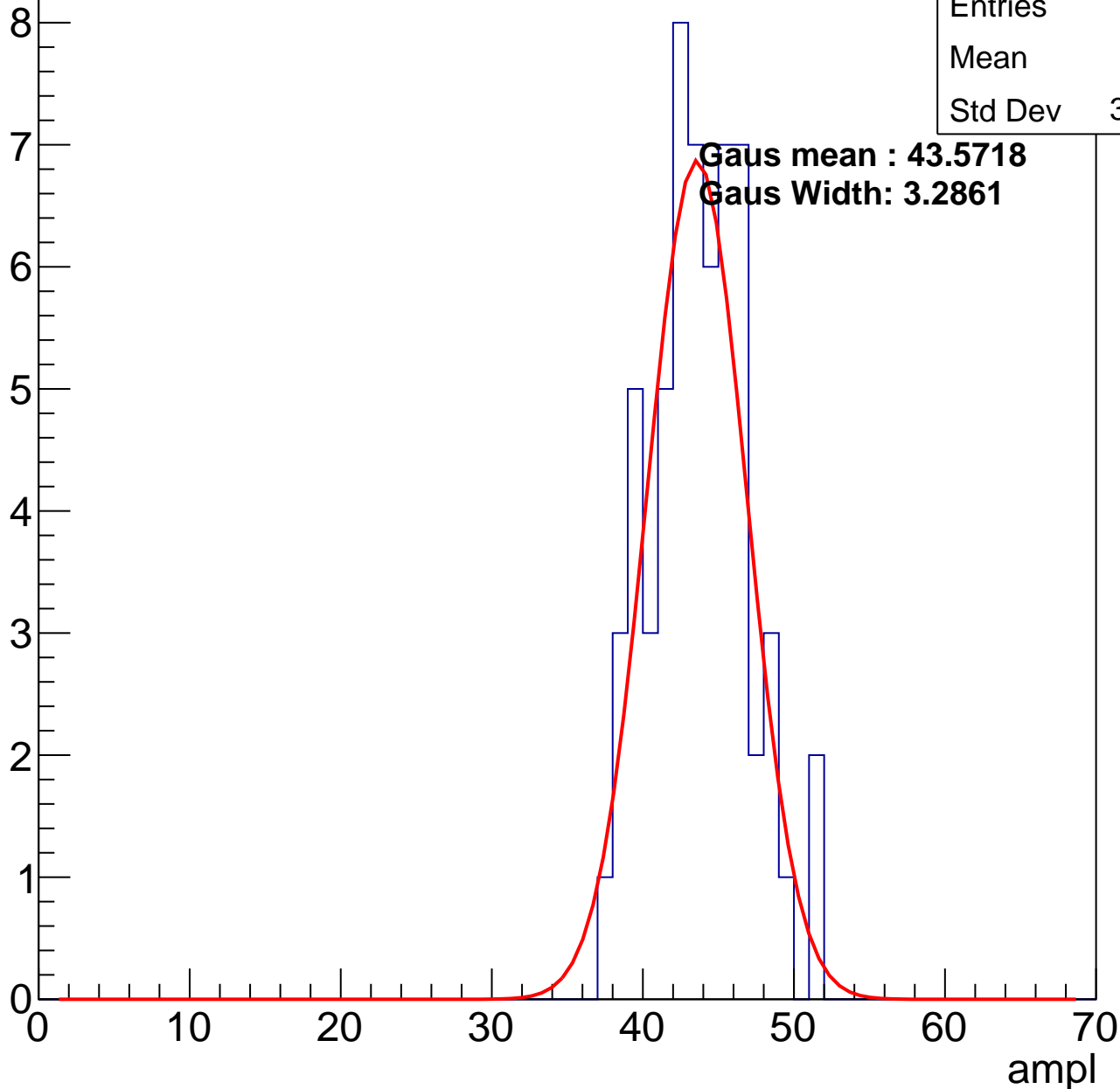
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	60
Mean	43.3
Std Dev	3.185

**Gaus mean : 43.5718**

**Gaus Width: 3.2861**

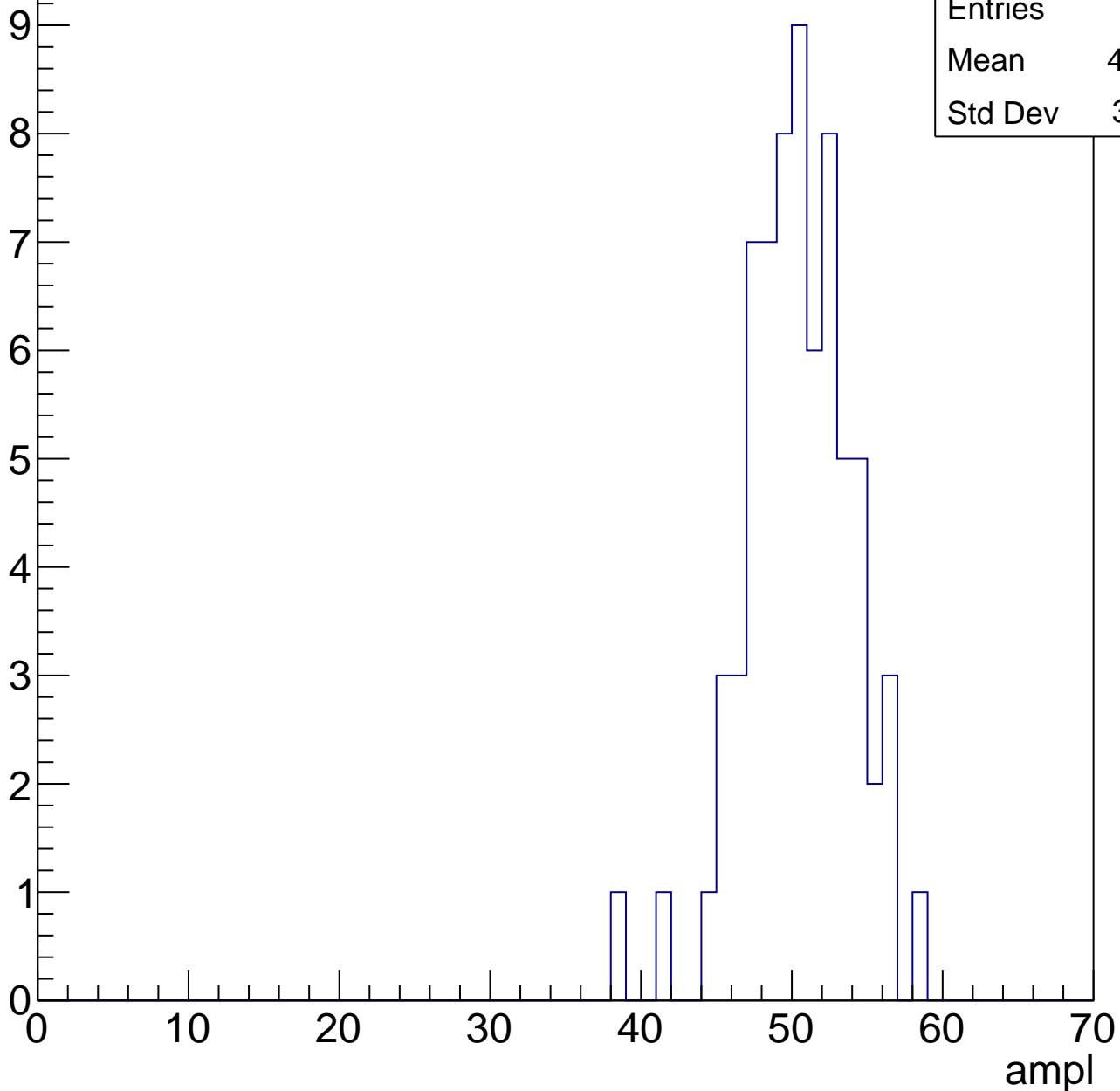


# B1L101S, U20-ch113, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	49.94
Std Dev	3.521

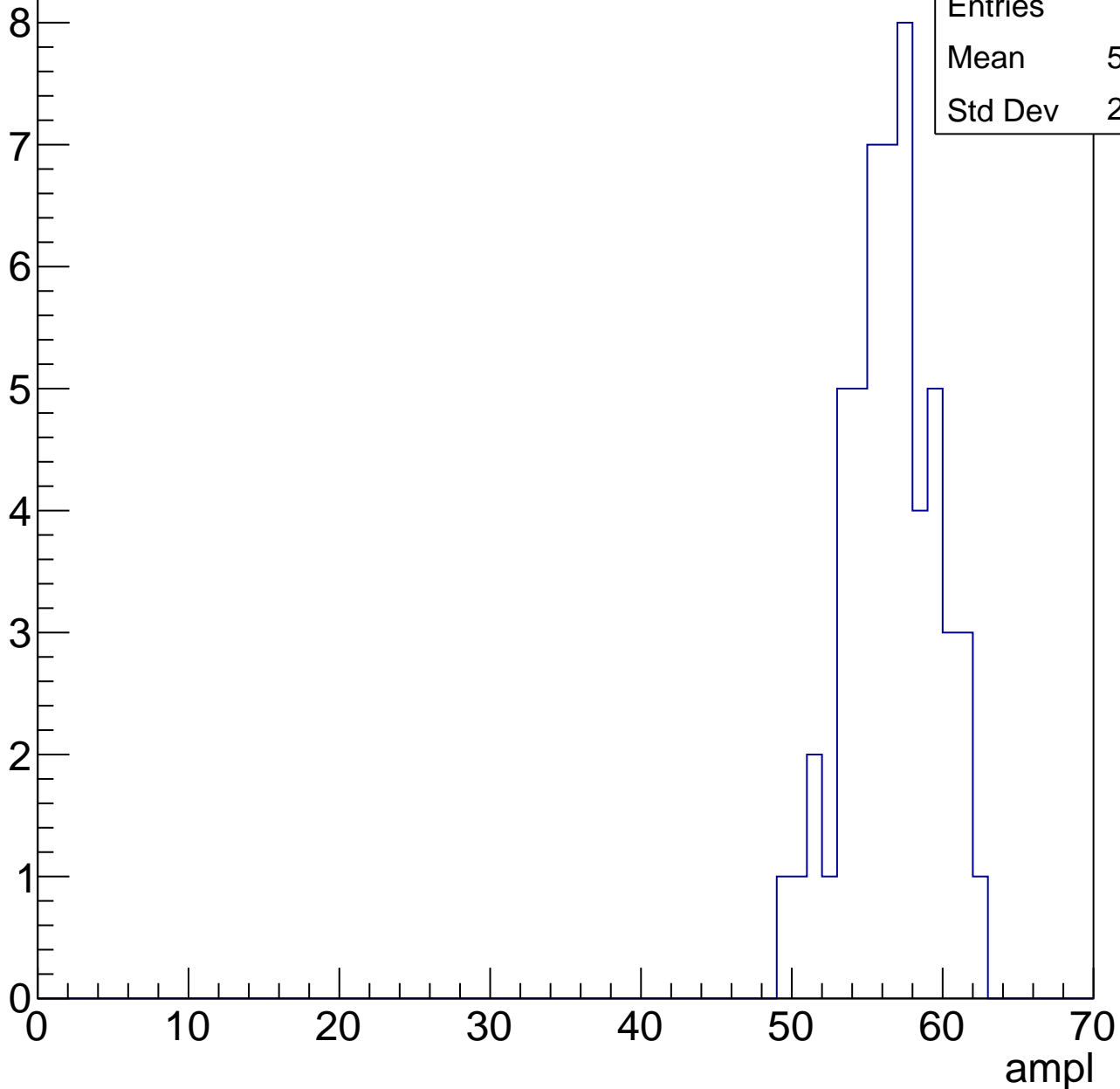


# B1L101S, U20-ch113, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	53
Mean	56.09
Std Dev	2.916

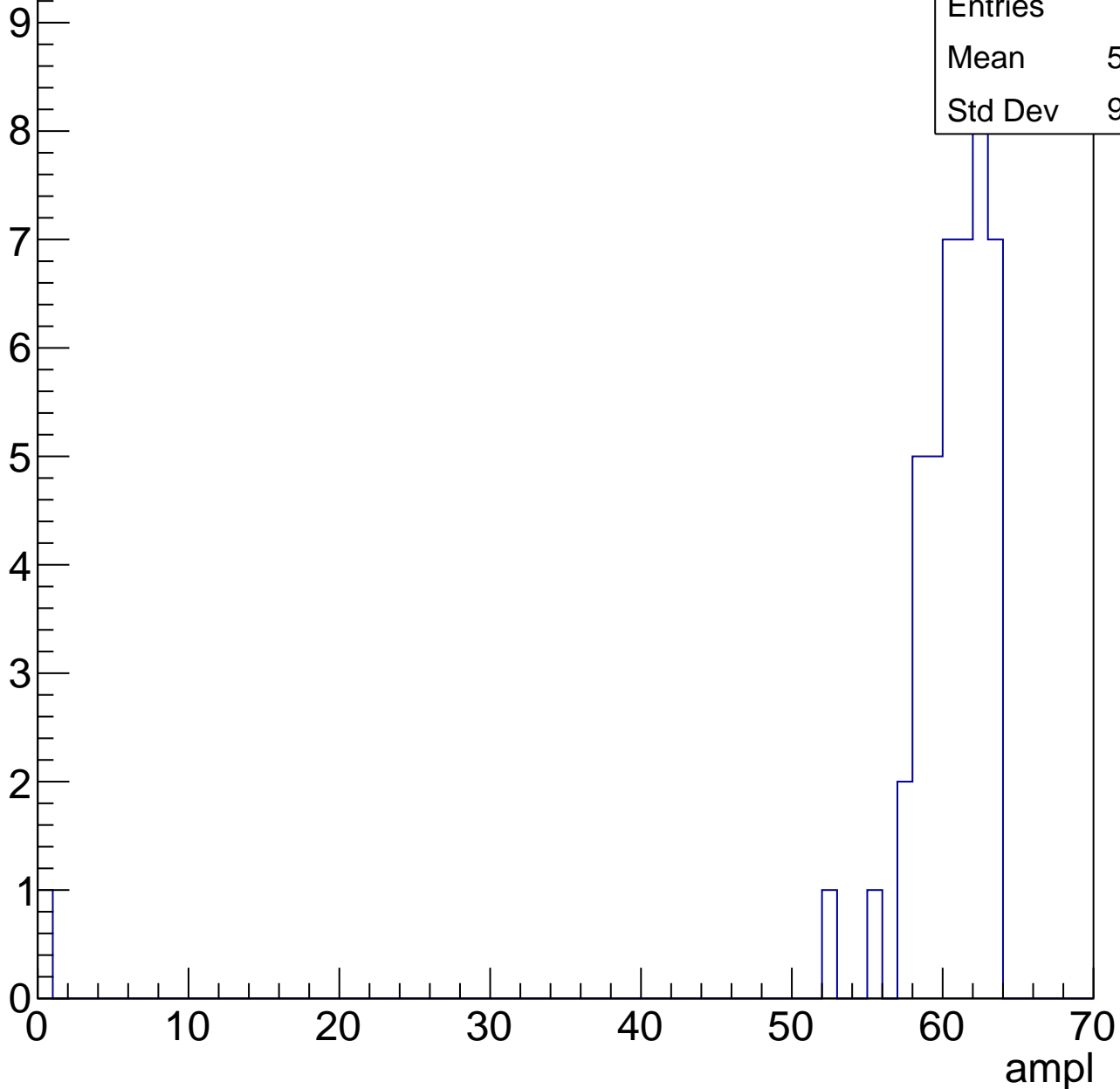


# B1L101S, U20-ch113, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	45
Mean	58.93
Std Dev	9.173



# B1L101S, U20-ch113, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U20-ch113, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U20-ch114, adc0

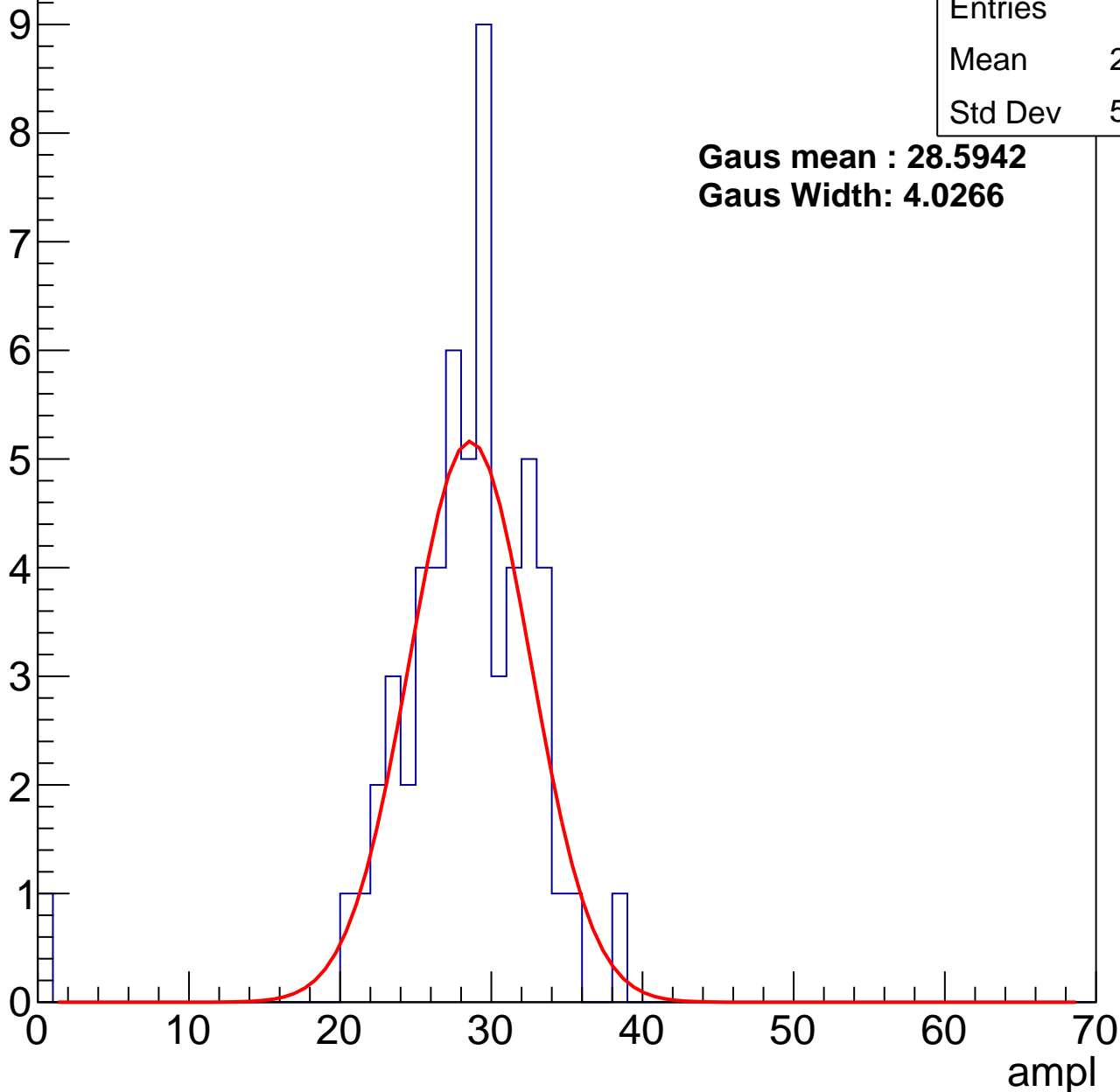
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	57
Mean	27.75
Std Dev	5.219

**Gaus mean : 28.5942**

**Gaus Width: 4.0266**



# B1L101S, U20-ch114, adc1

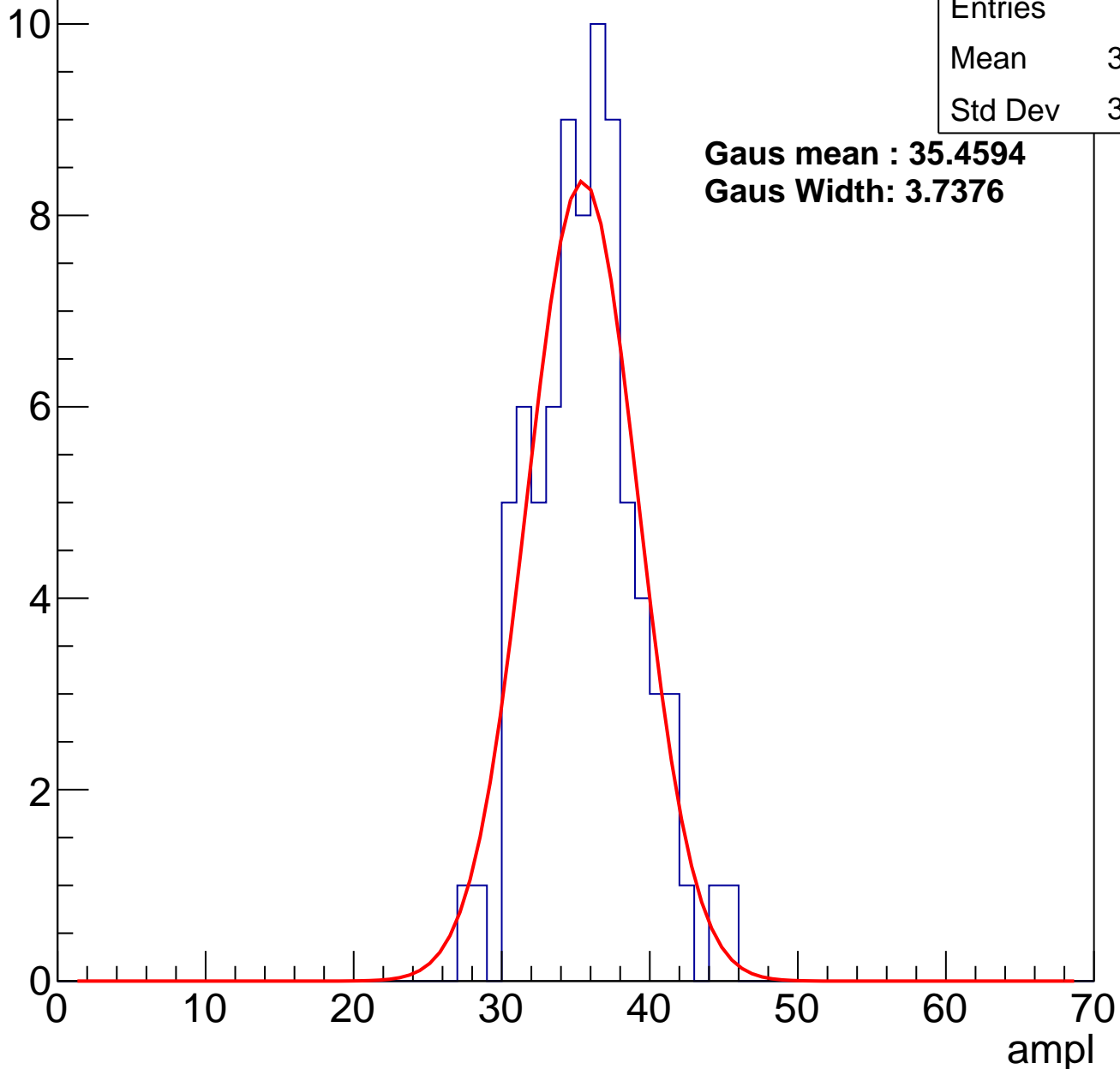
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	78
Mean	35.23
Std Dev	3.537

**Gaus mean : 35.4594**

**Gaus Width: 3.7376**

Entry



# B1L101S, U20-ch114, adc2

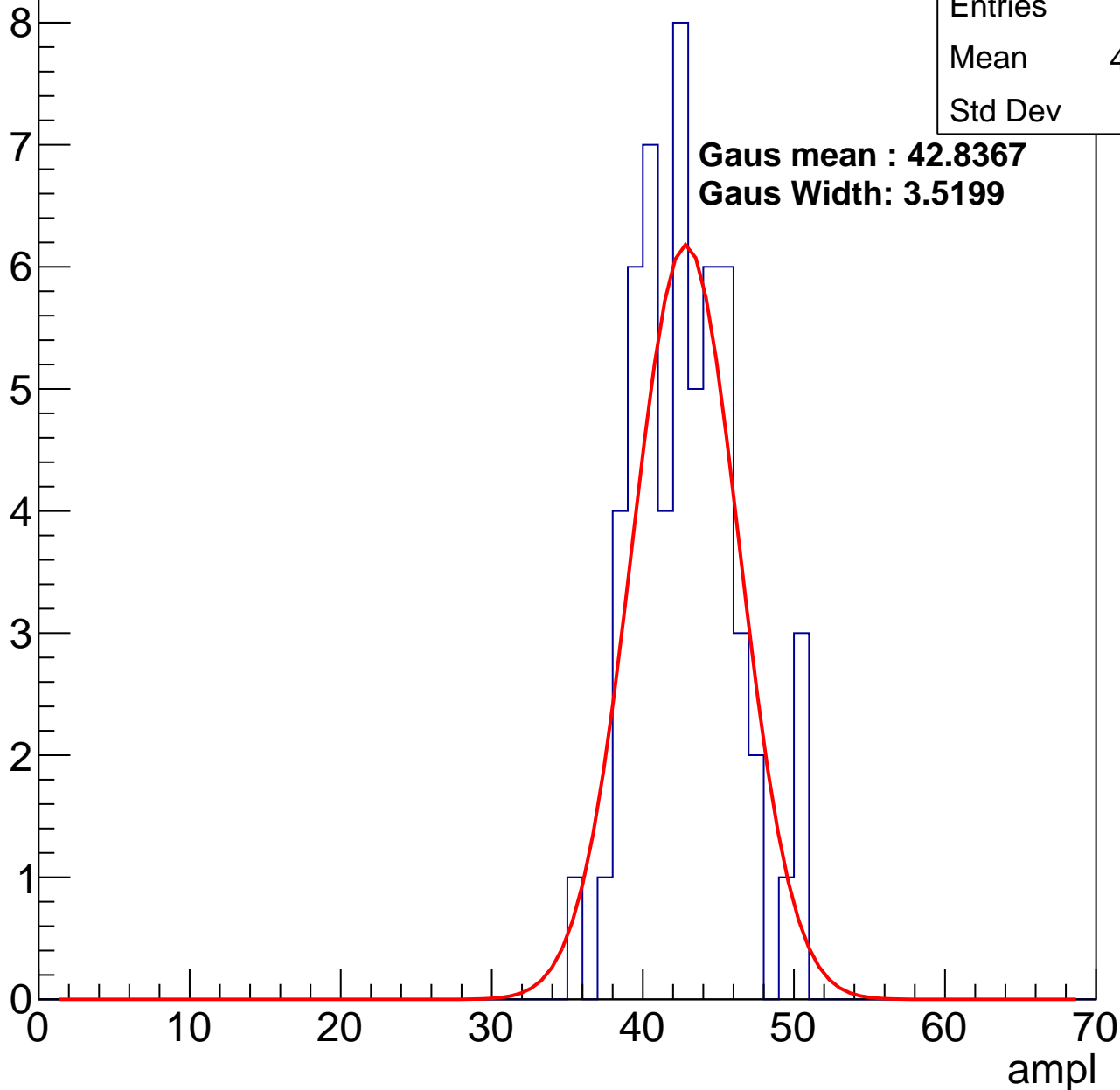
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	57
Mean	42.42
Std Dev	3.34

**Gaus mean : 42.8367**

**Gaus Width: 3.5199**

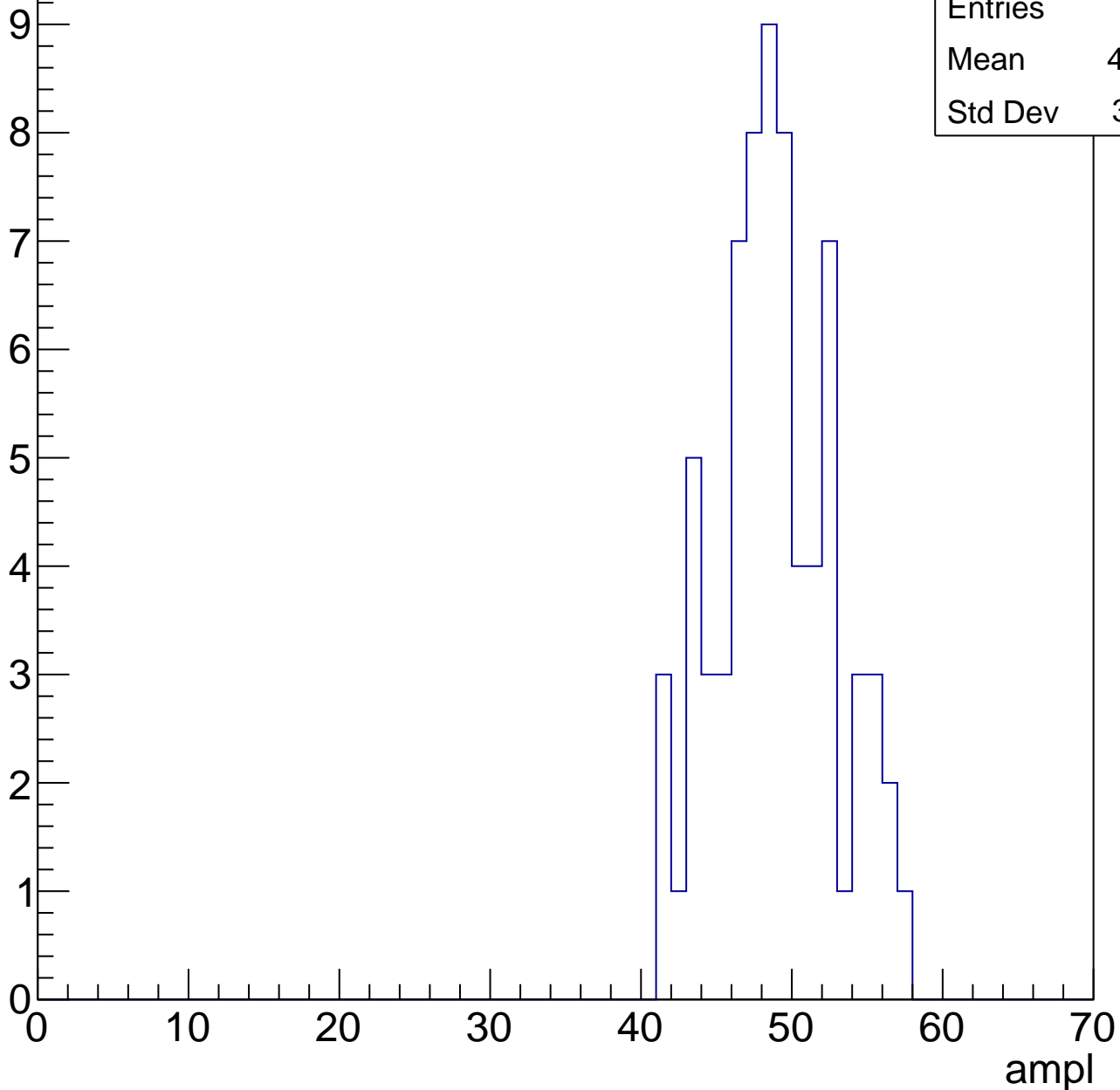


# B1L101S, U20-ch114, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

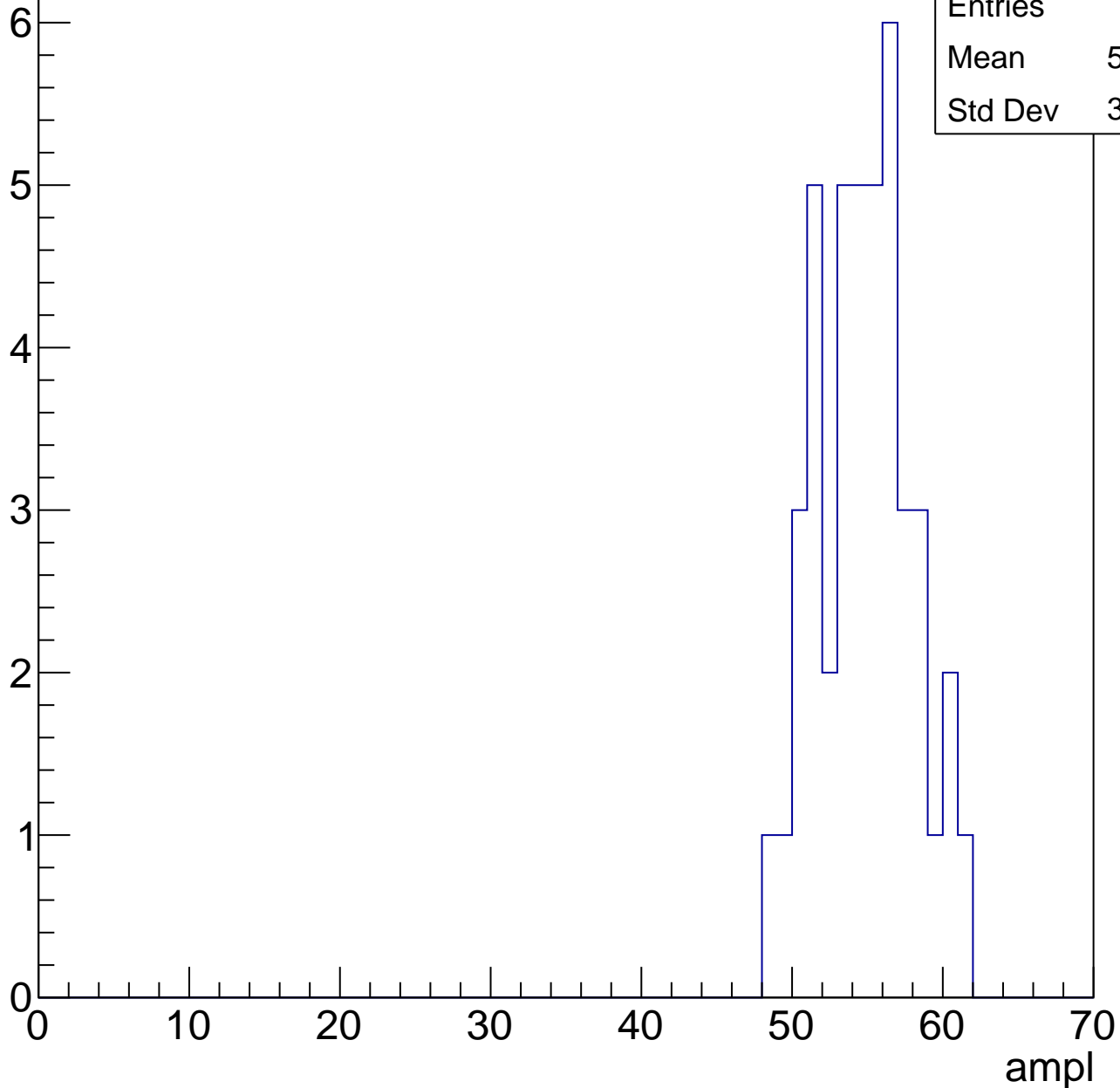
Entries	72
Mean	48.42
Std Dev	3.851



# B1L101S, U20-ch114, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

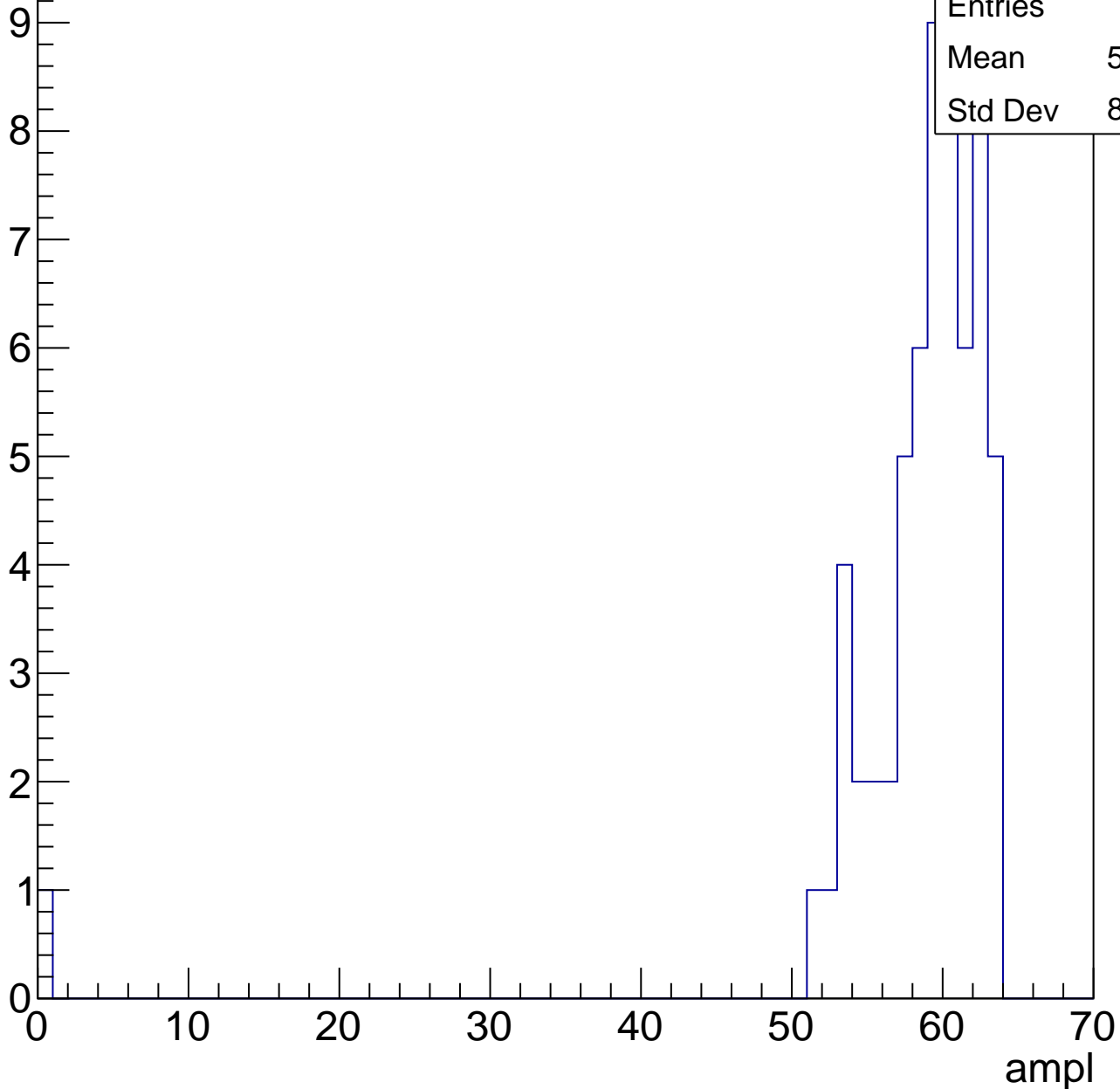


# B1L101S, U20-ch114, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	57.84
Std Dev	8.072

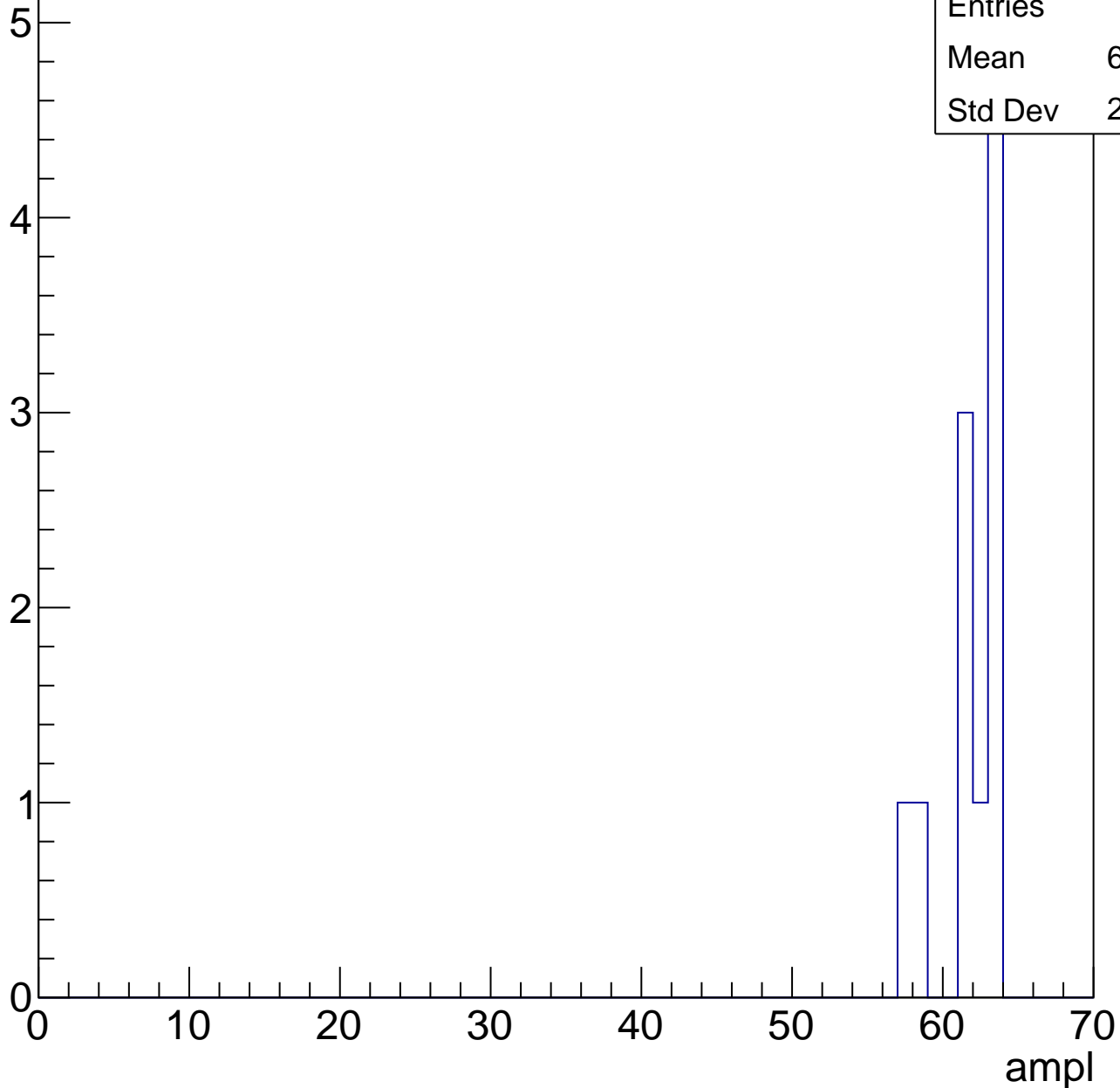


# B1L101S, U20-ch114, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	11
Mean	61.36
Std Dev	2.012





# B1L101S, U20-ch114, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U20-ch115, adc0

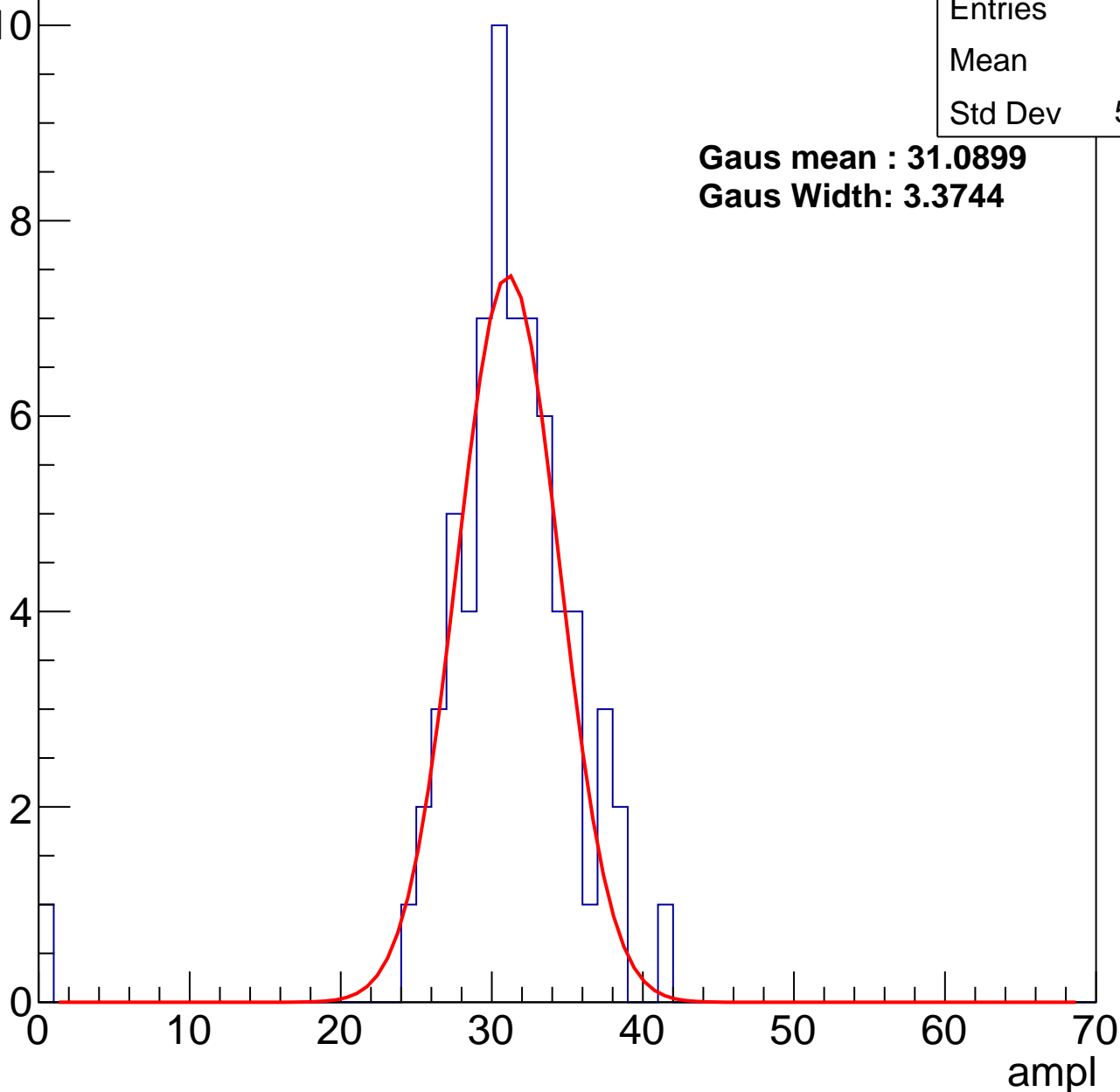
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	30.6
Std Dev	5.091

**Gaus mean : 31.0899**

**Gaus Width: 3.3744**



# B1L101S, U20-ch115, adc1

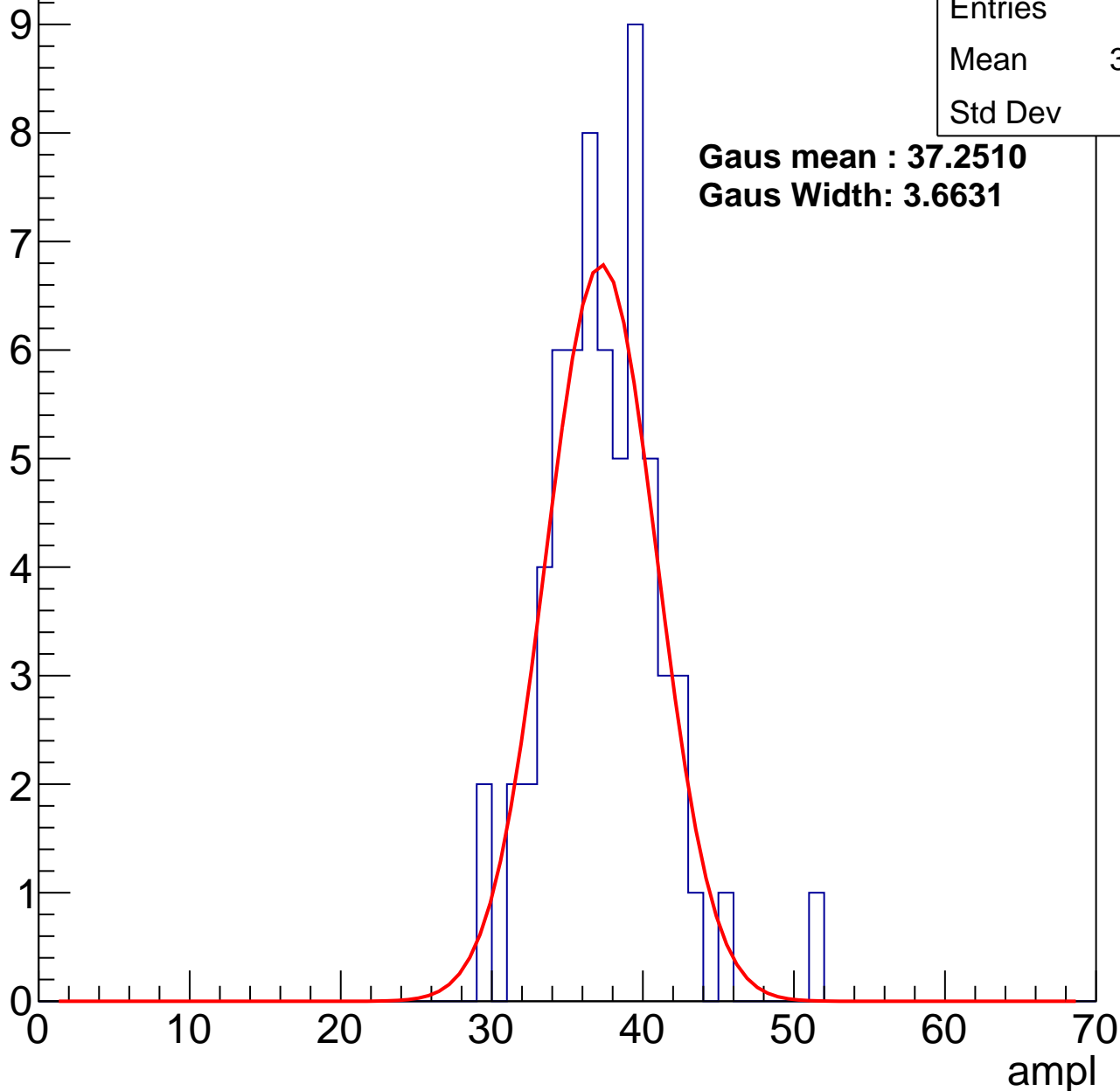
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	37.02
Std Dev	3.76

**Gaus mean : 37.2510**

**Gaus Width: 3.6631**

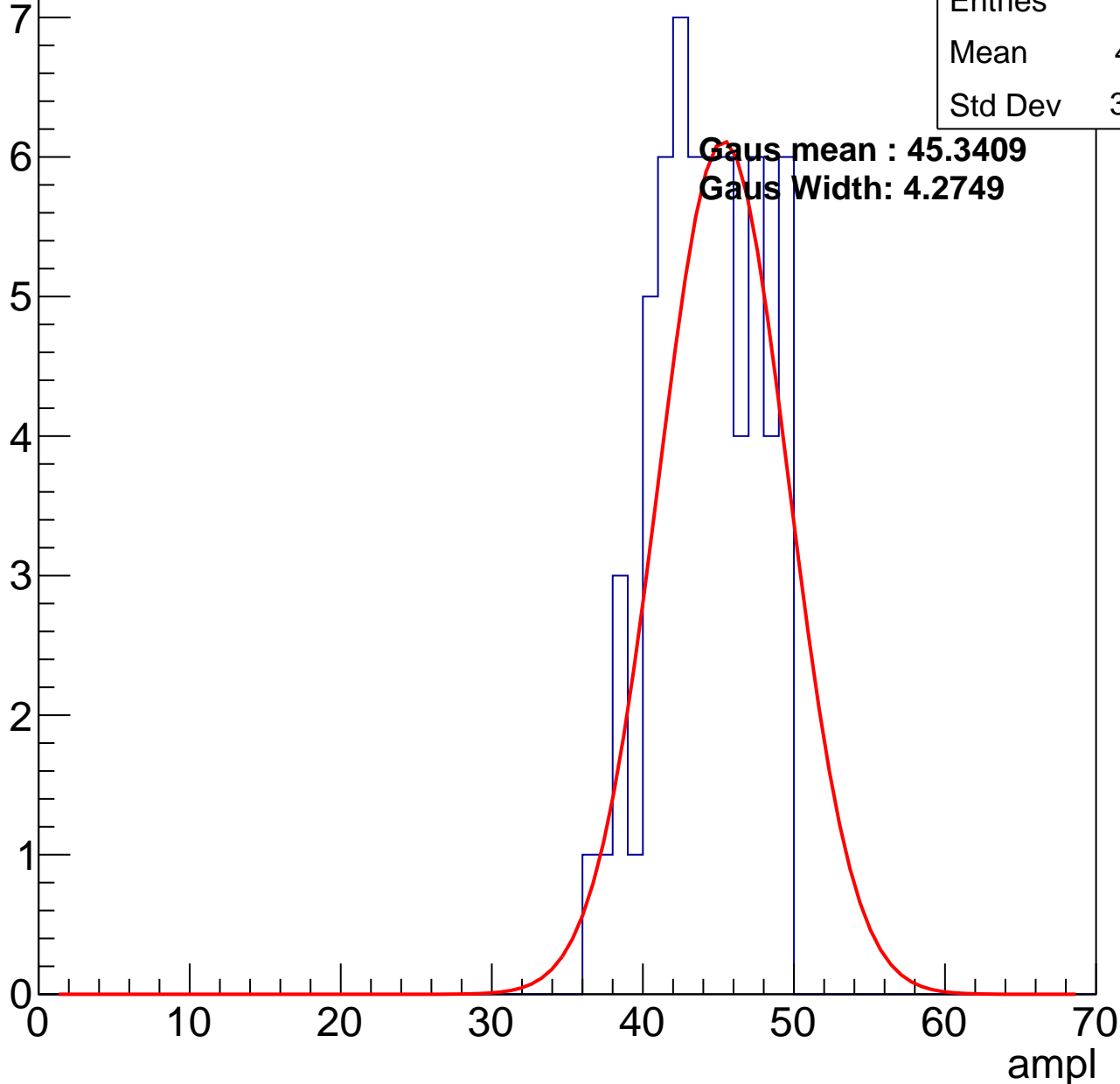


# B1L101S, U20-ch115, adc2

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	43.71
Std Dev	3.357



# B1L101S, U20-ch115, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

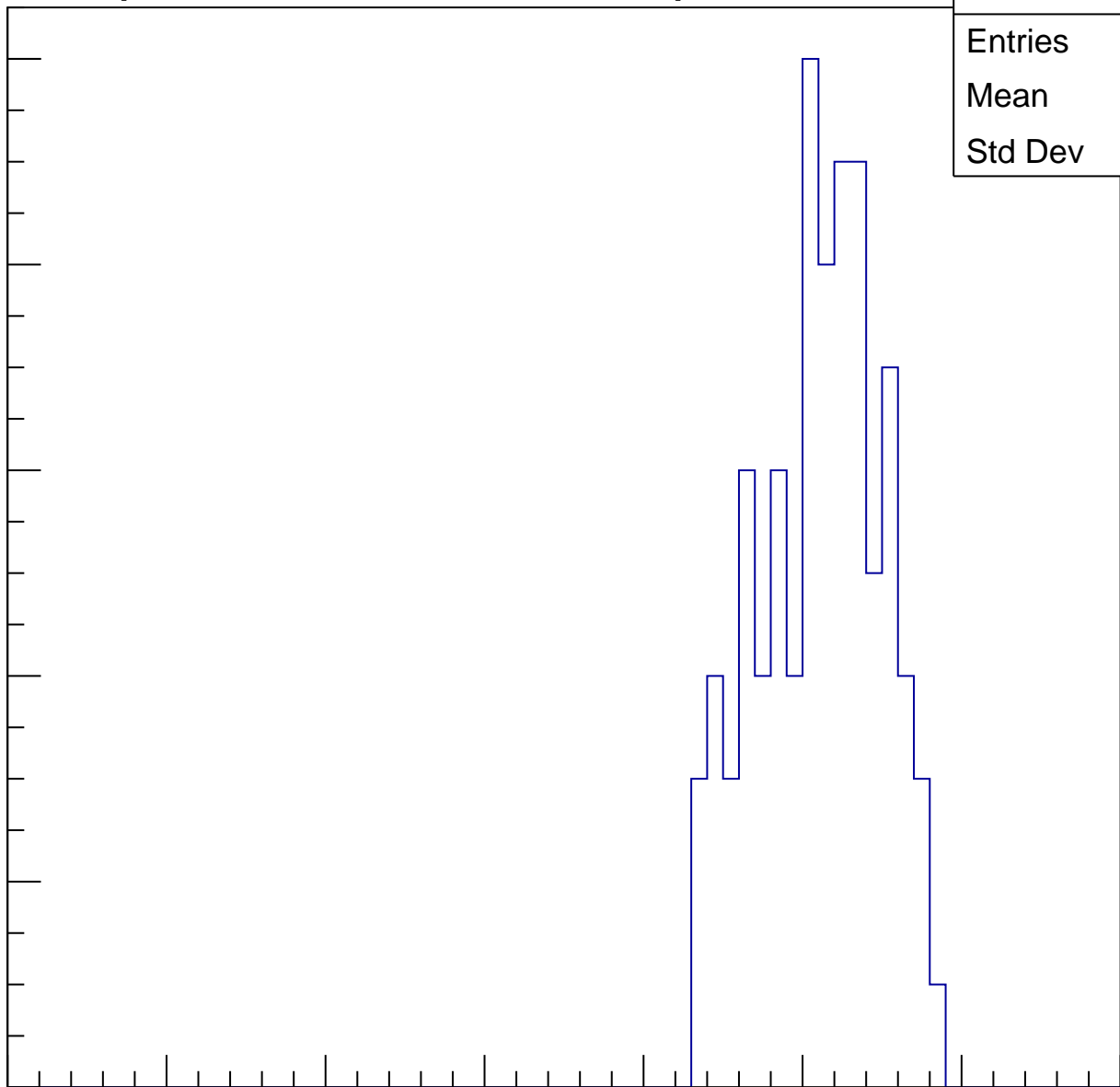
Entries	86
Mean	50.57
Std Dev	3.787

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

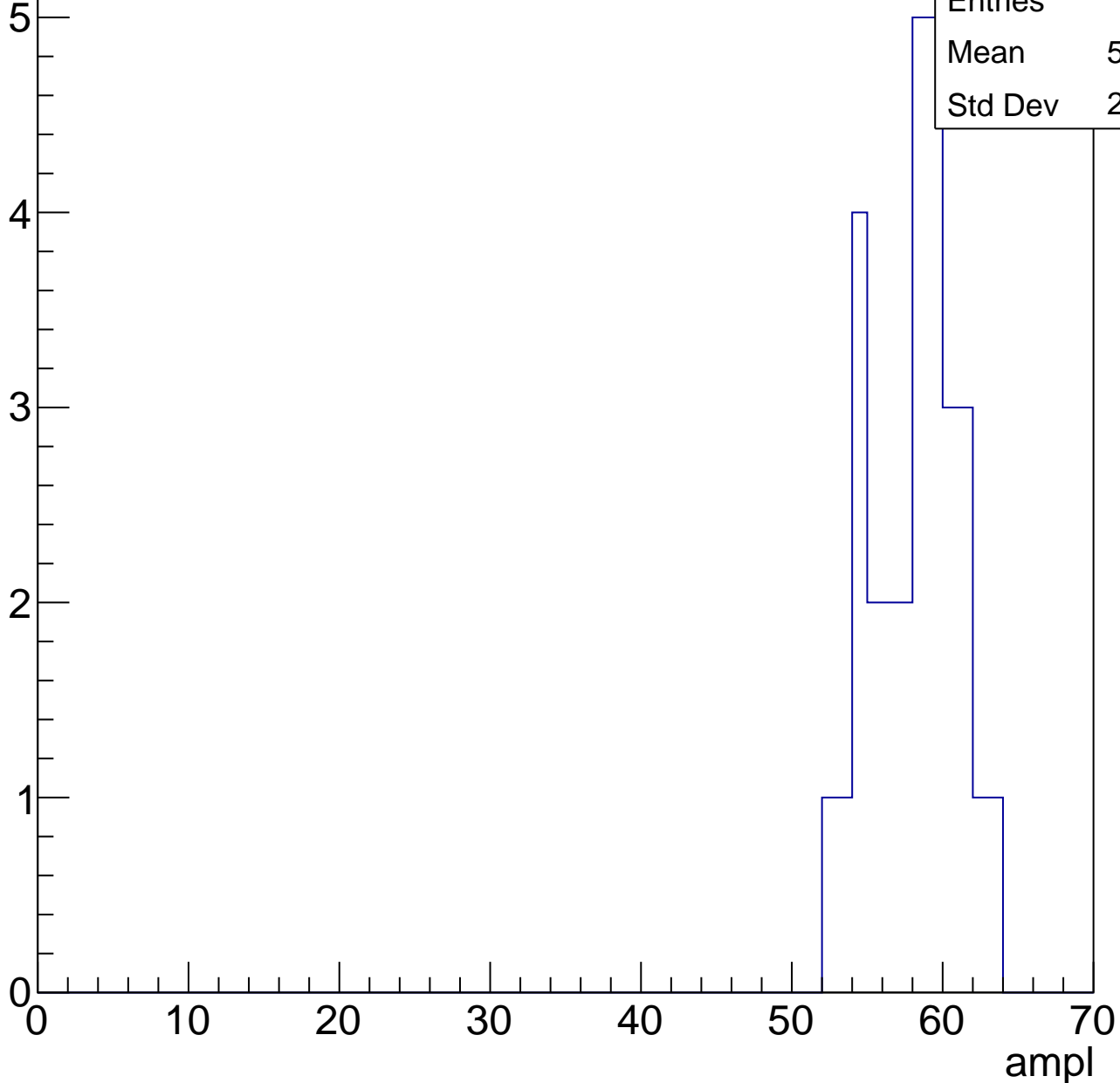


# B1L101S, U20-ch115, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	30
Mean	57.67
Std Dev	2.797

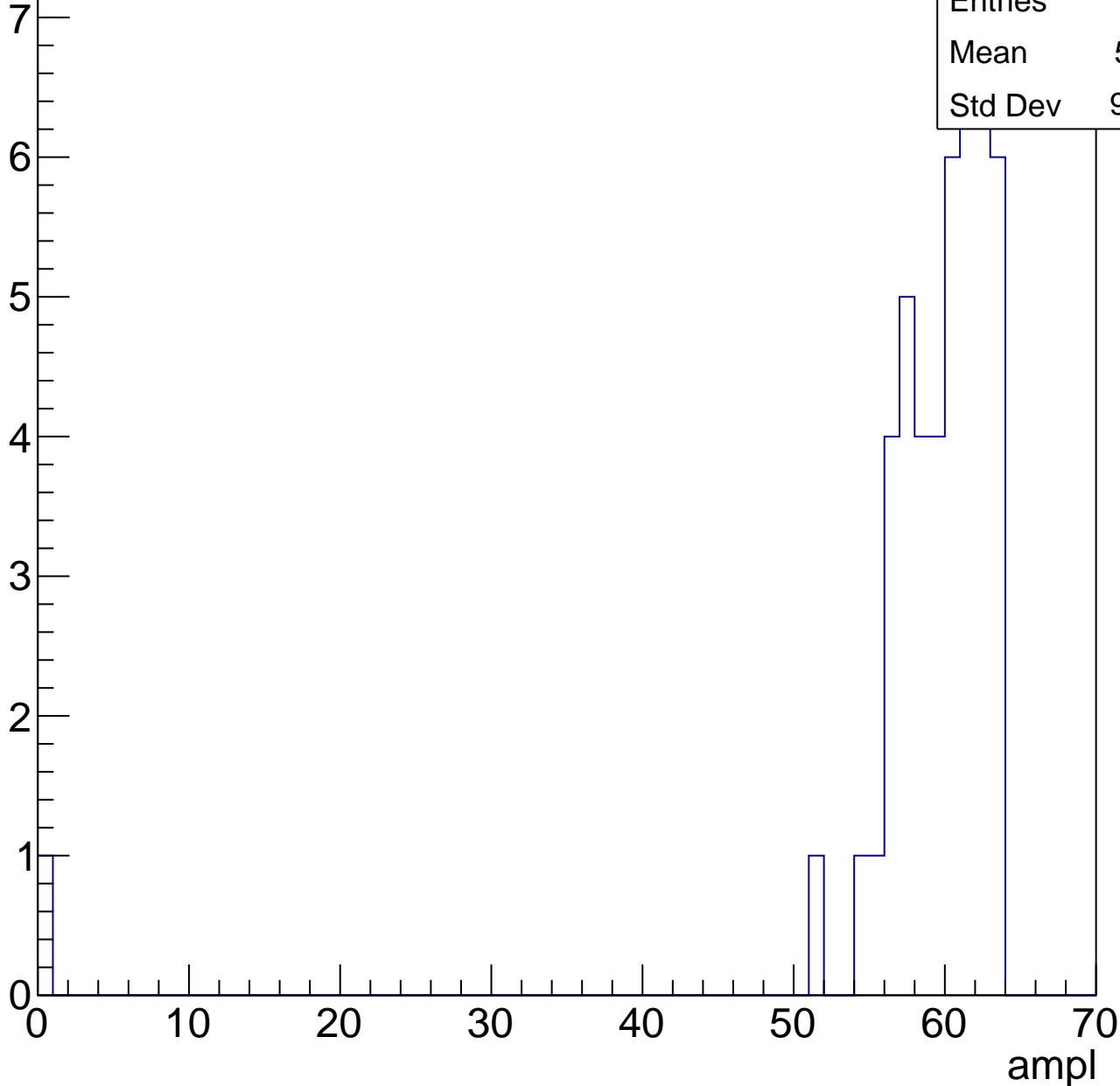


# B1L101S, U20-ch115, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

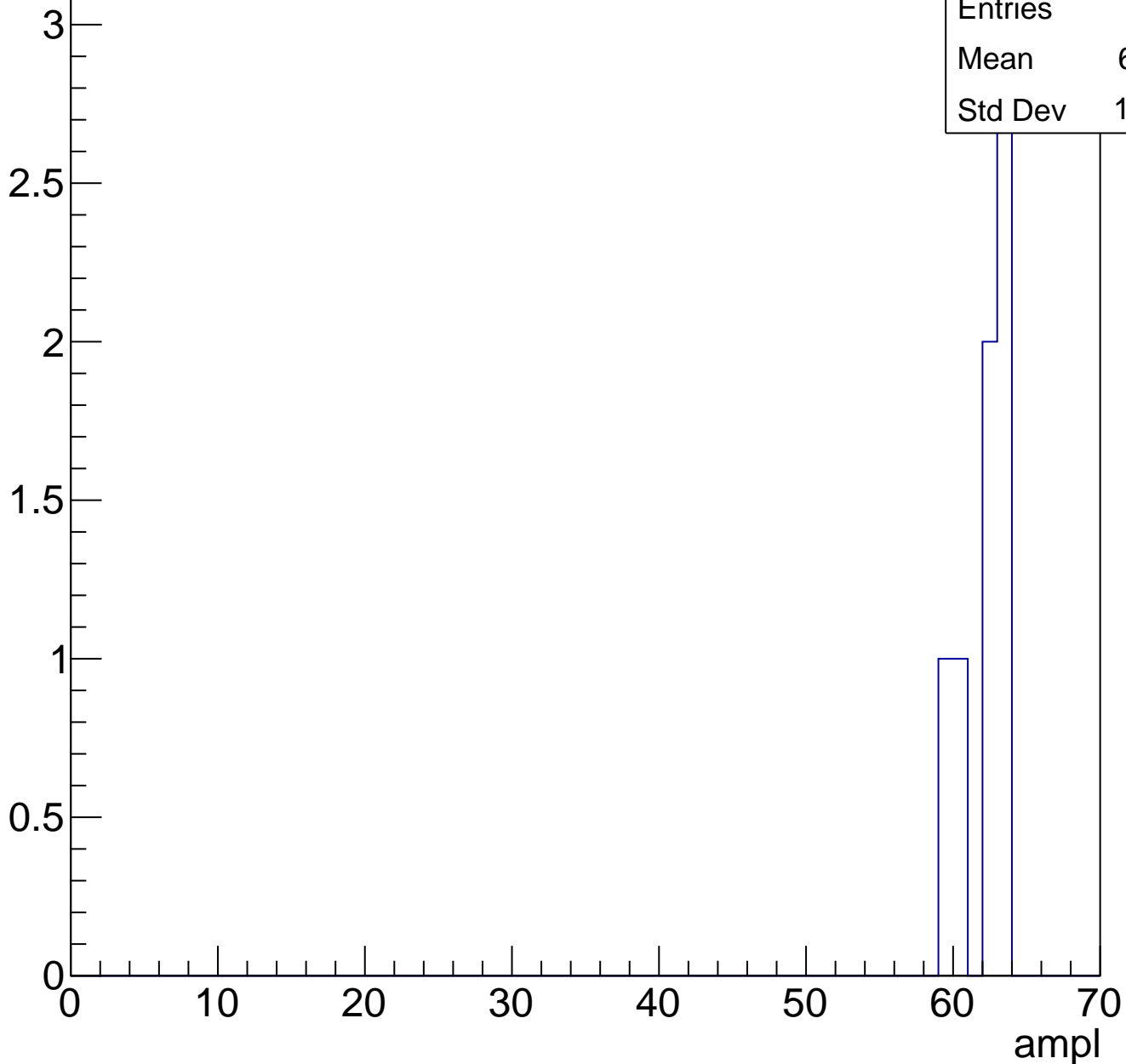
Entries	47
Mean	58.21
Std Dev	9.003



# B1L101S, U20-ch115, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U20-ch115, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U20-ch116, adc0

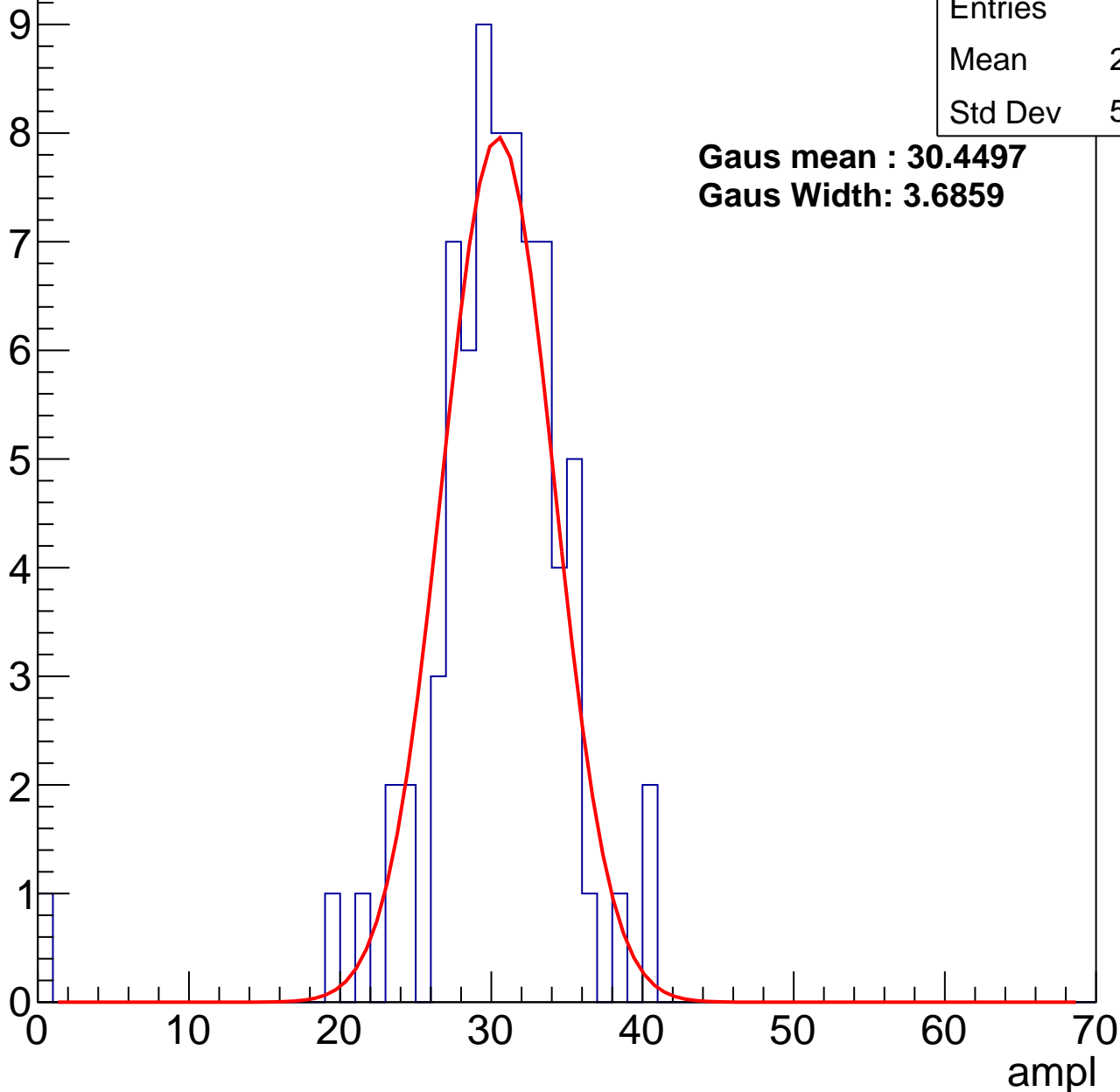
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	75
Mean	29.84
Std Dev	5.167

**Gaus mean : 30.4497**

**Gaus Width: 3.6859**



# B1L101S, U20-ch116, adc1

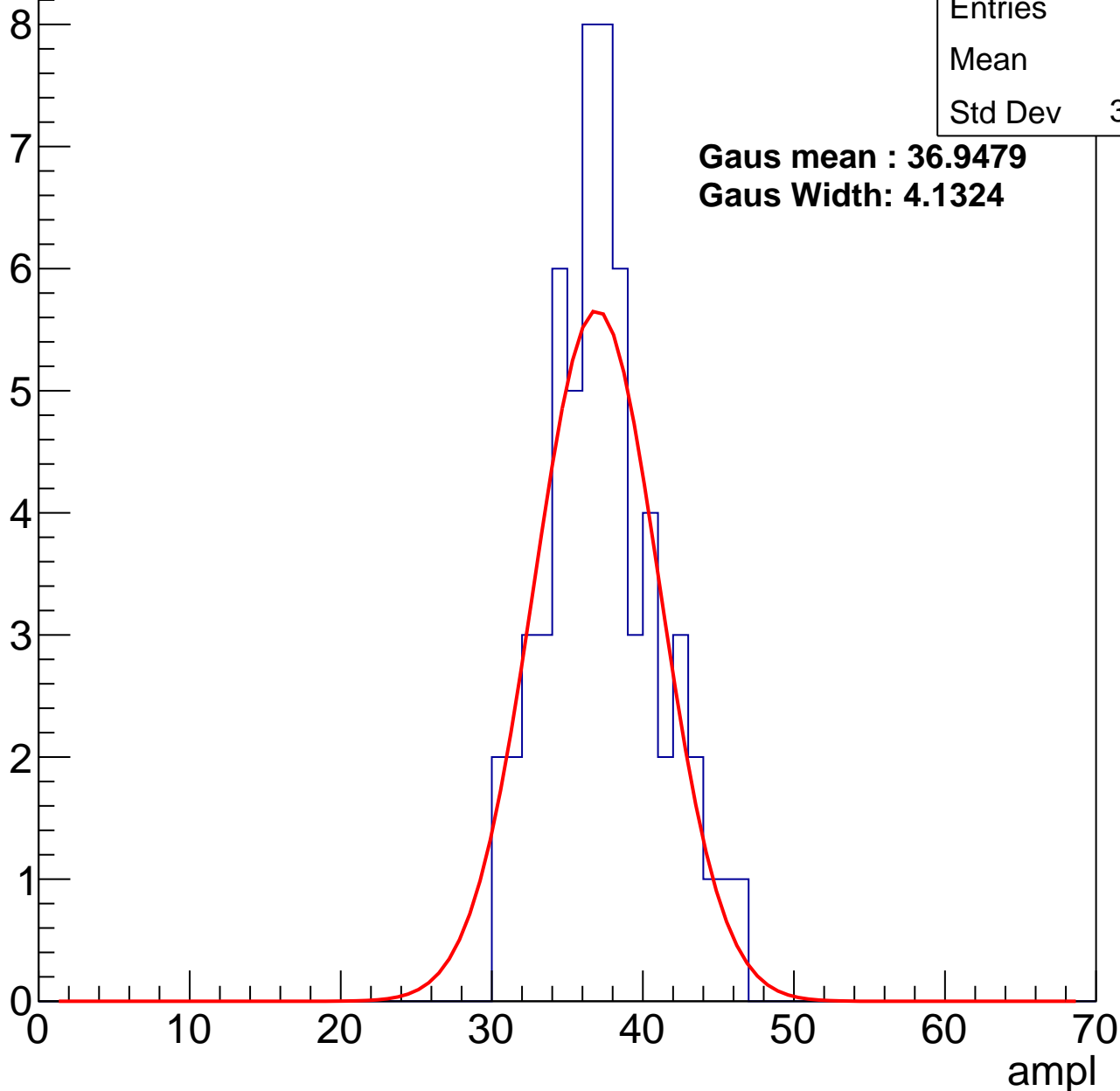
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	60
Mean	36.9
Std Dev	3.655

**Gaus mean : 36.9479**

**Gaus Width: 4.1324**



# B1L101S, U20-ch116, adc2

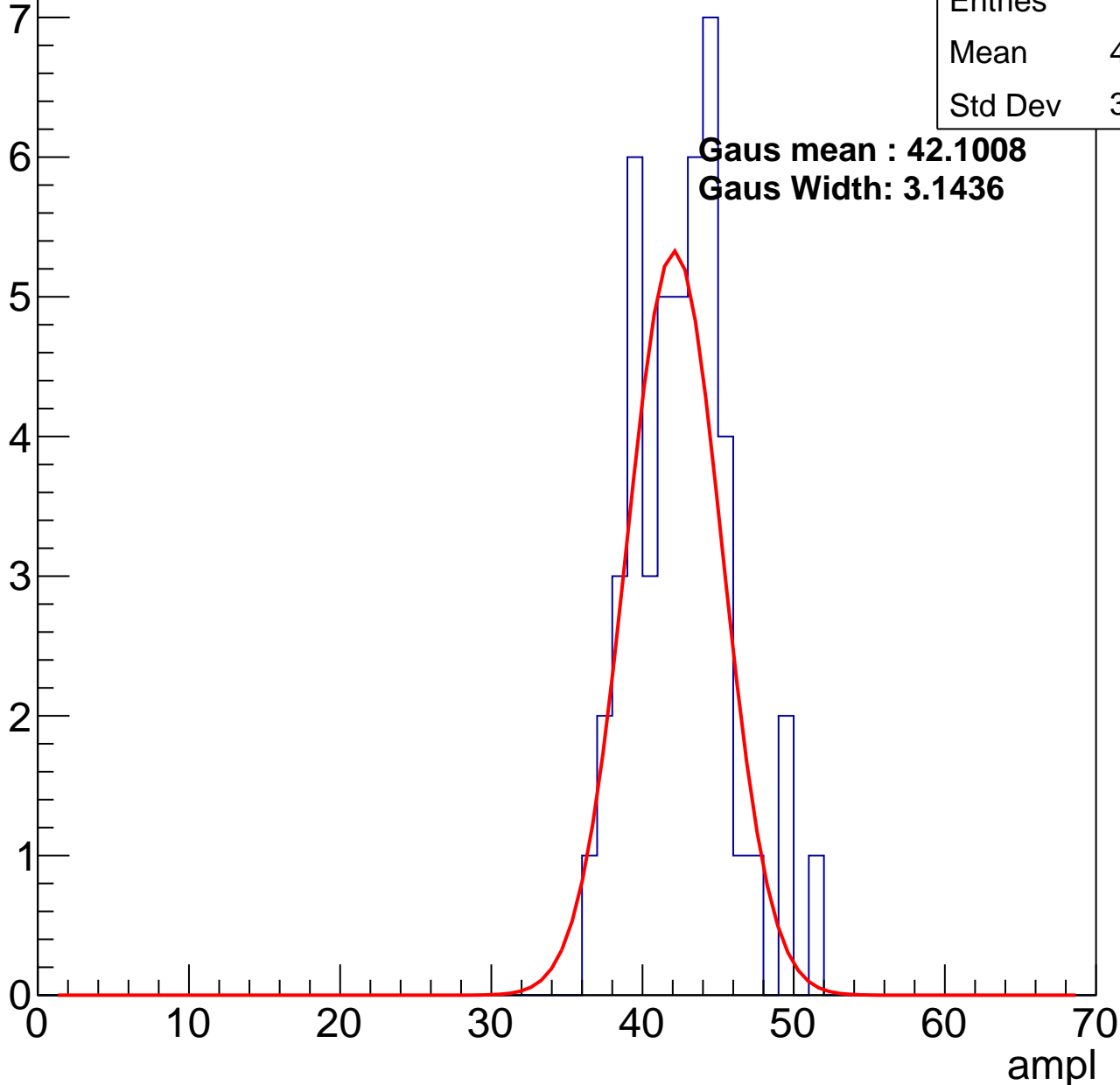
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	47
Mean	42.15
Std Dev	3.242

**Gaus mean : 42.1008**

**Gaus Width: 3.1436**

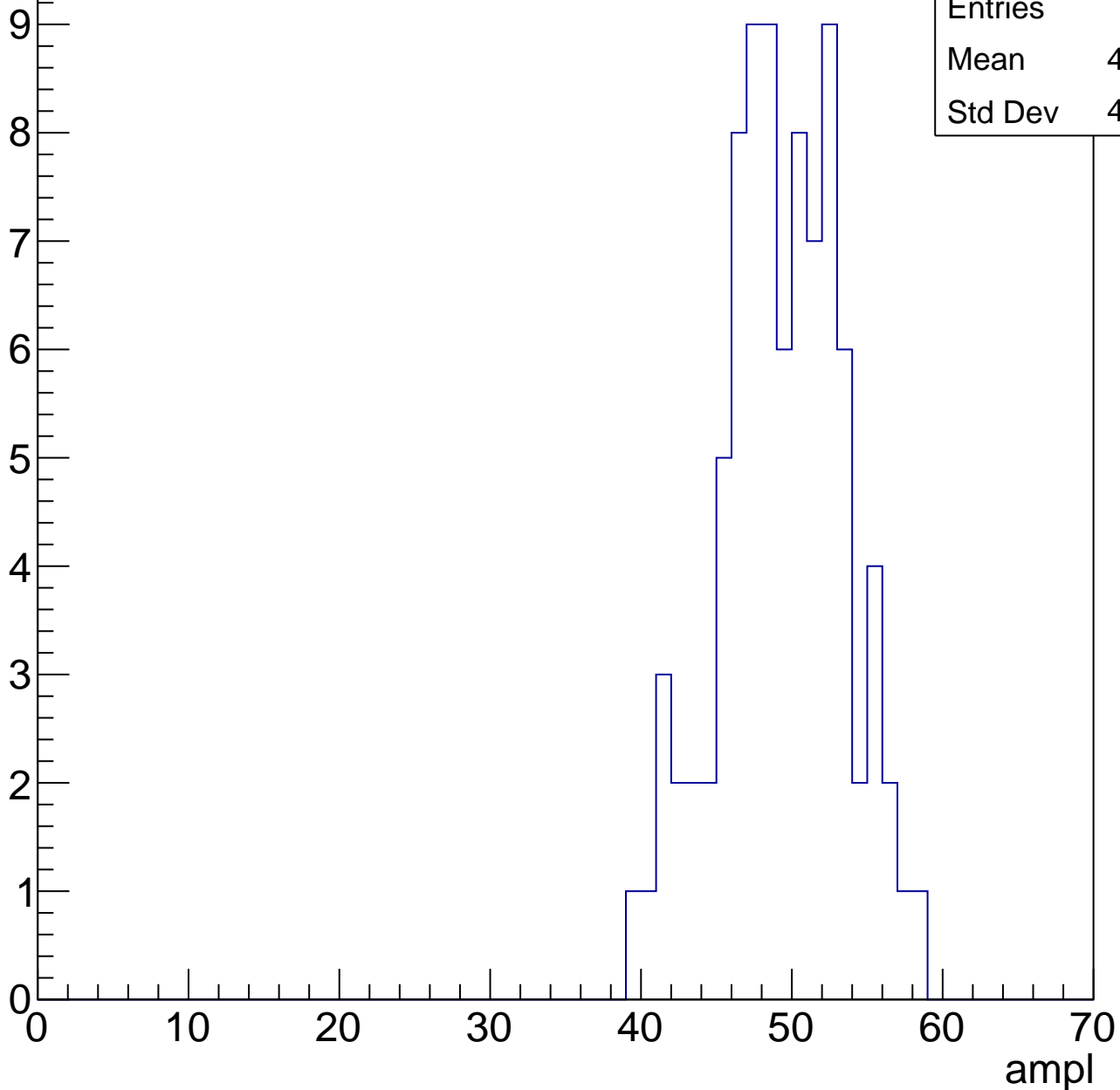


# B1L101S, U20-ch116, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	88
Mean	48.86
Std Dev	4.043

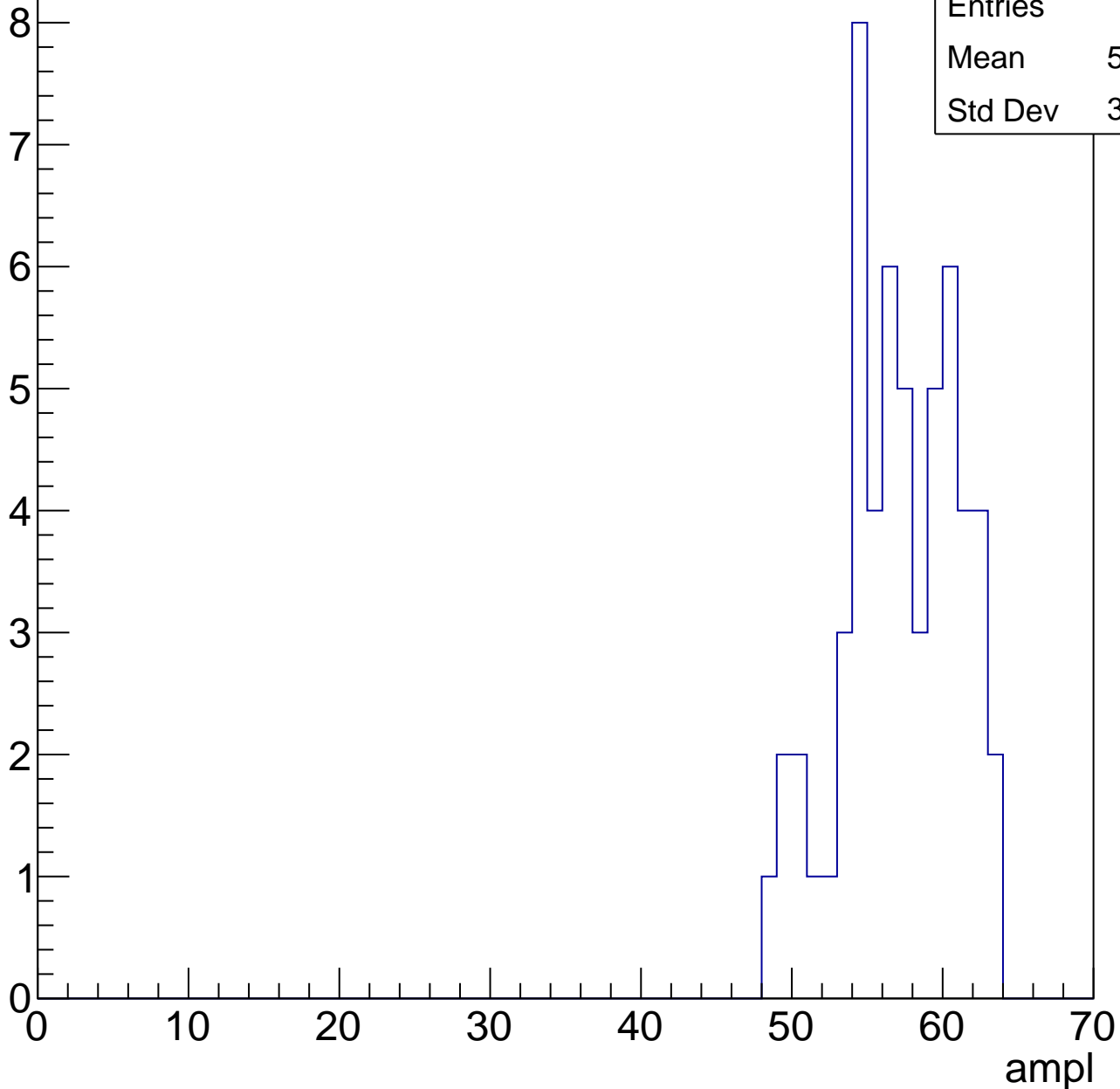


# B1L101S, U20-ch116, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	57
Mean	56.63
Std Dev	3.782

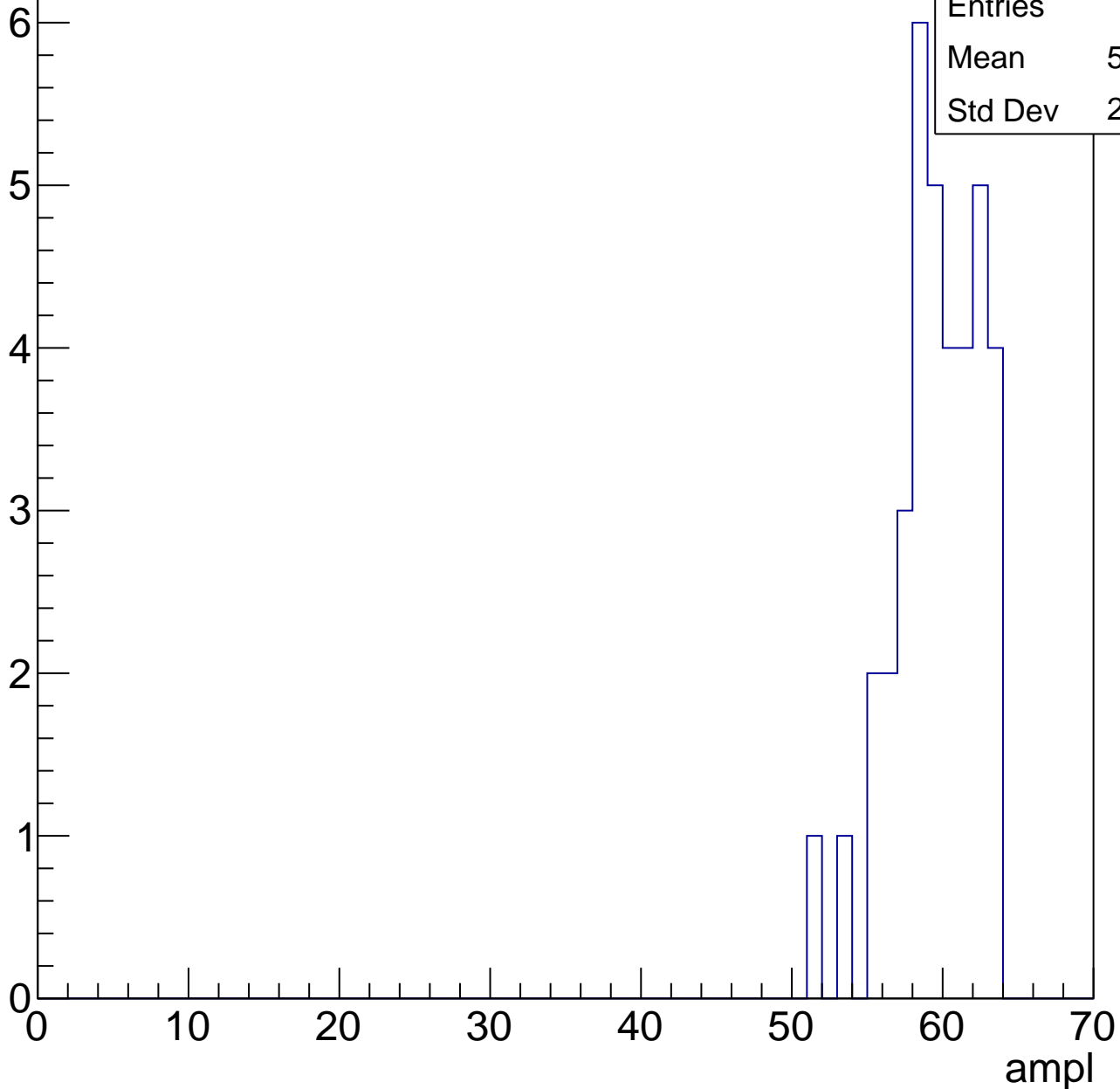


# B1L101S, U20-ch116, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

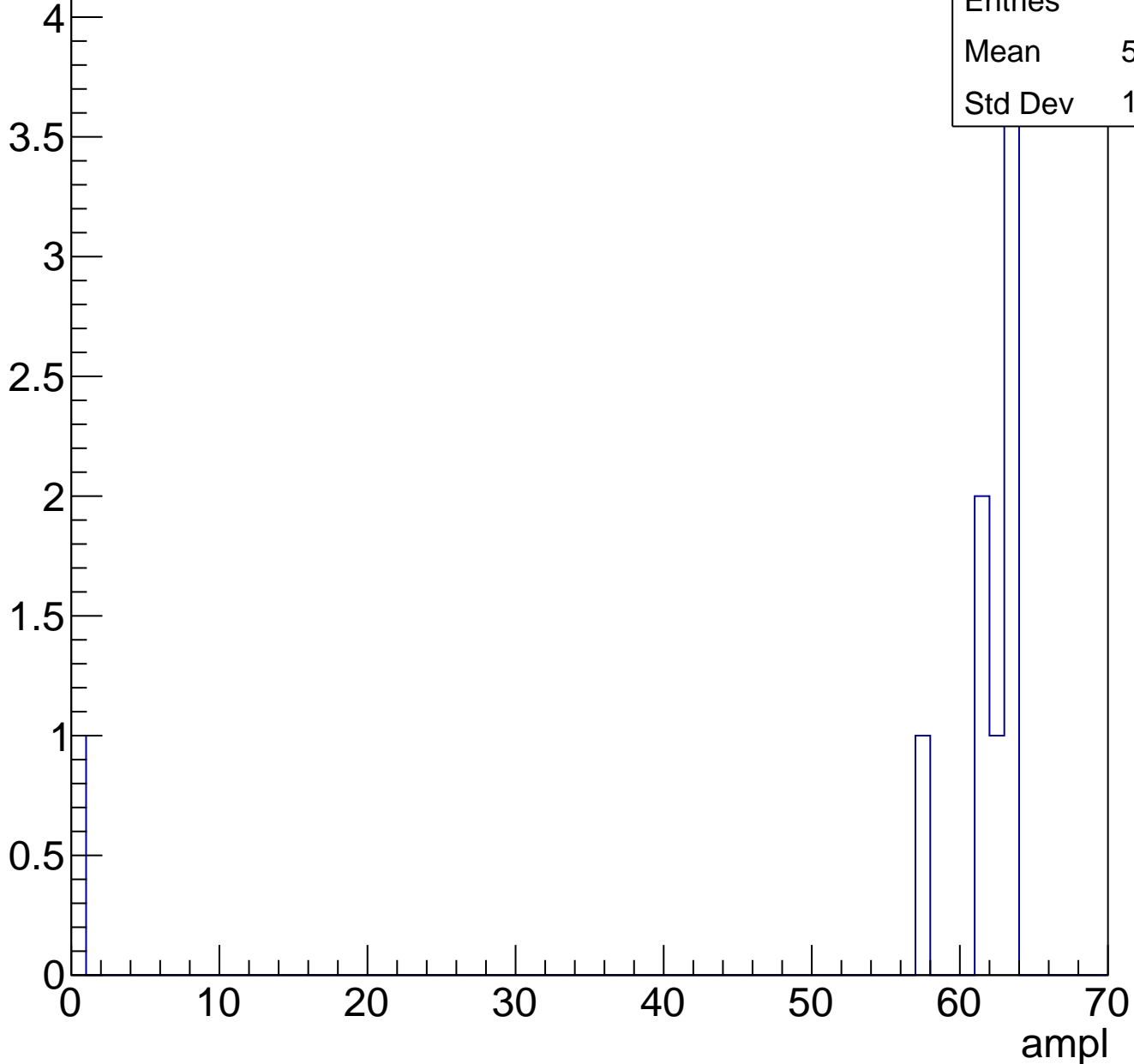
Entries	37
Mean	59.08
Std Dev	2.832



# B1L101S, U20-ch116, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U20-ch116, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U20-ch117, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	72
Mean	29.65
Std Dev	4.959

**Gaus mean : 30.3439**

**Gaus Width: 3.6485**

Entry

10

8

6

4

2

0

0

10

20

30

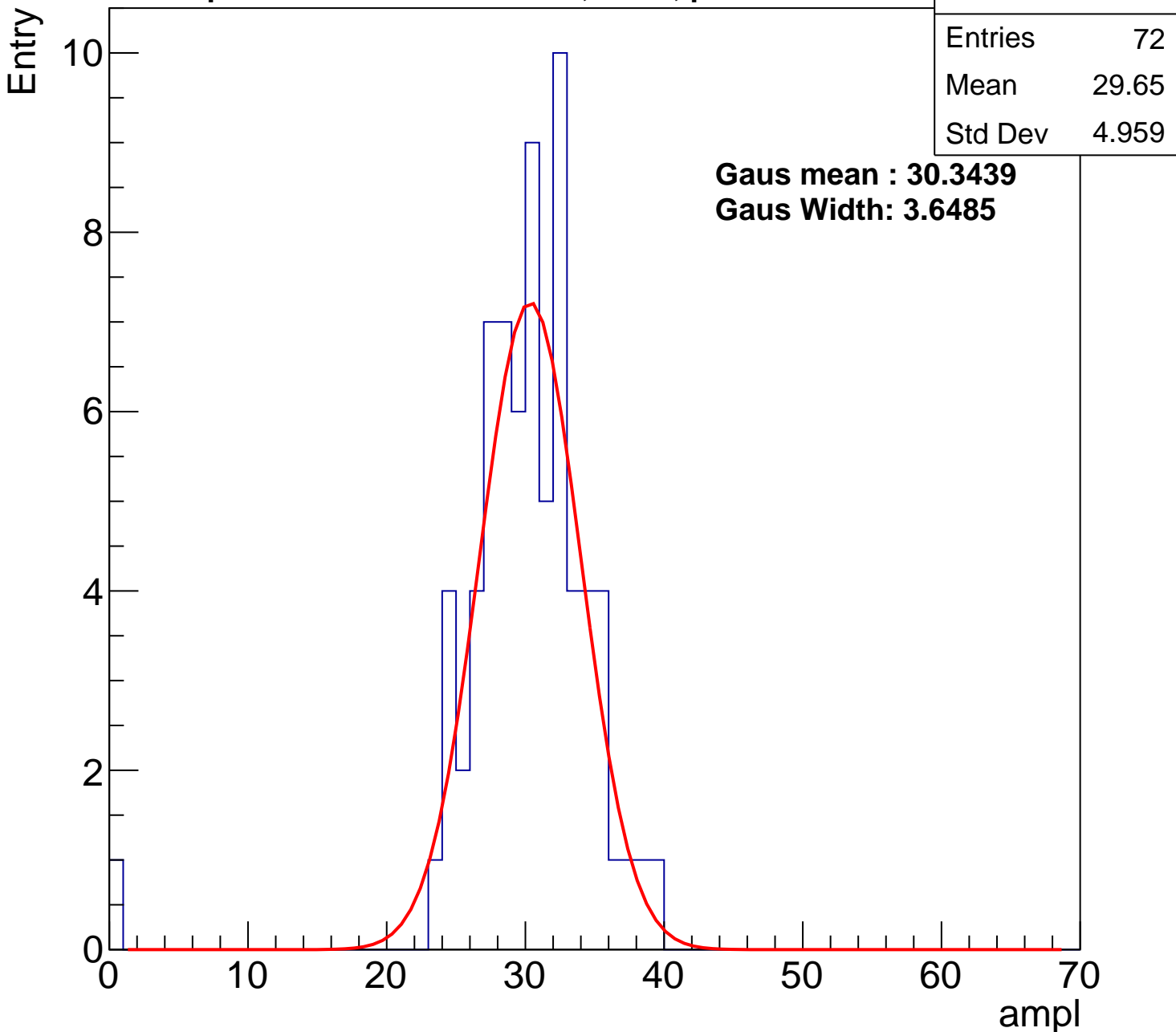
40

50

60

70

ampl



# B1L101S, U20-ch117, adc1

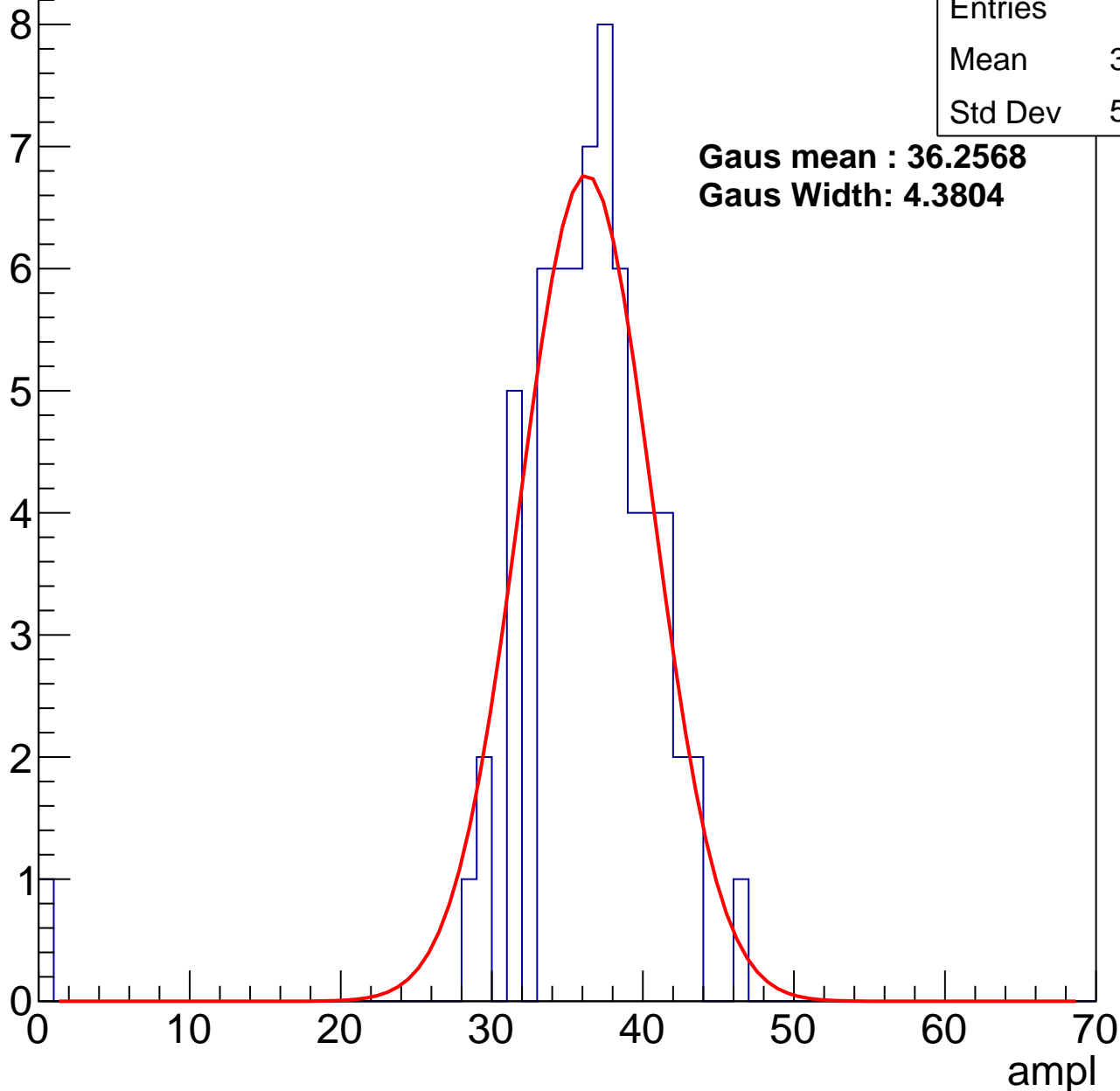
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	35.77
Std Dev	5.772

**Gaus mean : 36.2568**

**Gaus Width: 4.3804**



# B1L101S, U20-ch117, adc2

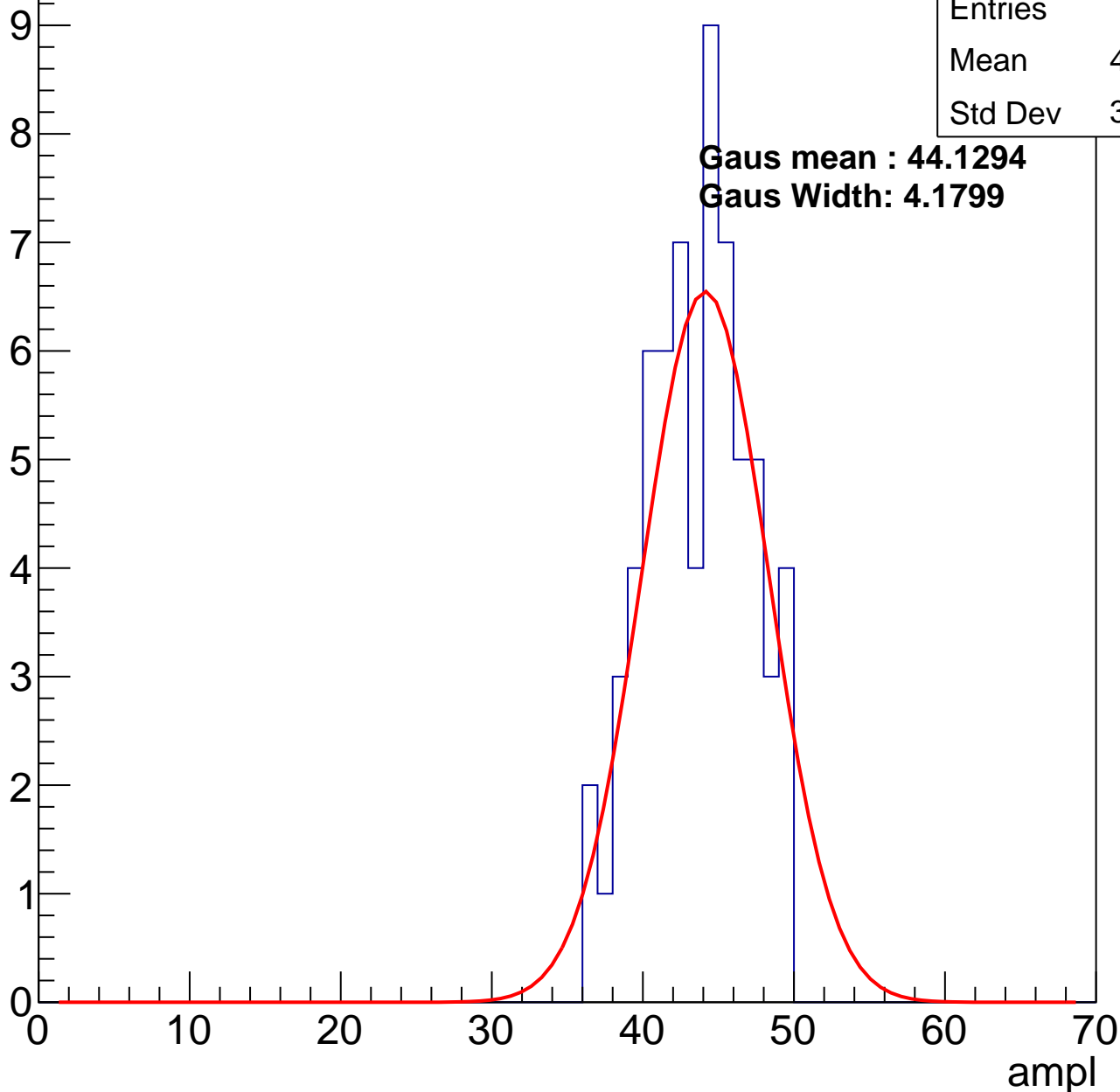
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	66
Mean	43.14
Std Dev	3.343

**Gaus mean : 44.1294**

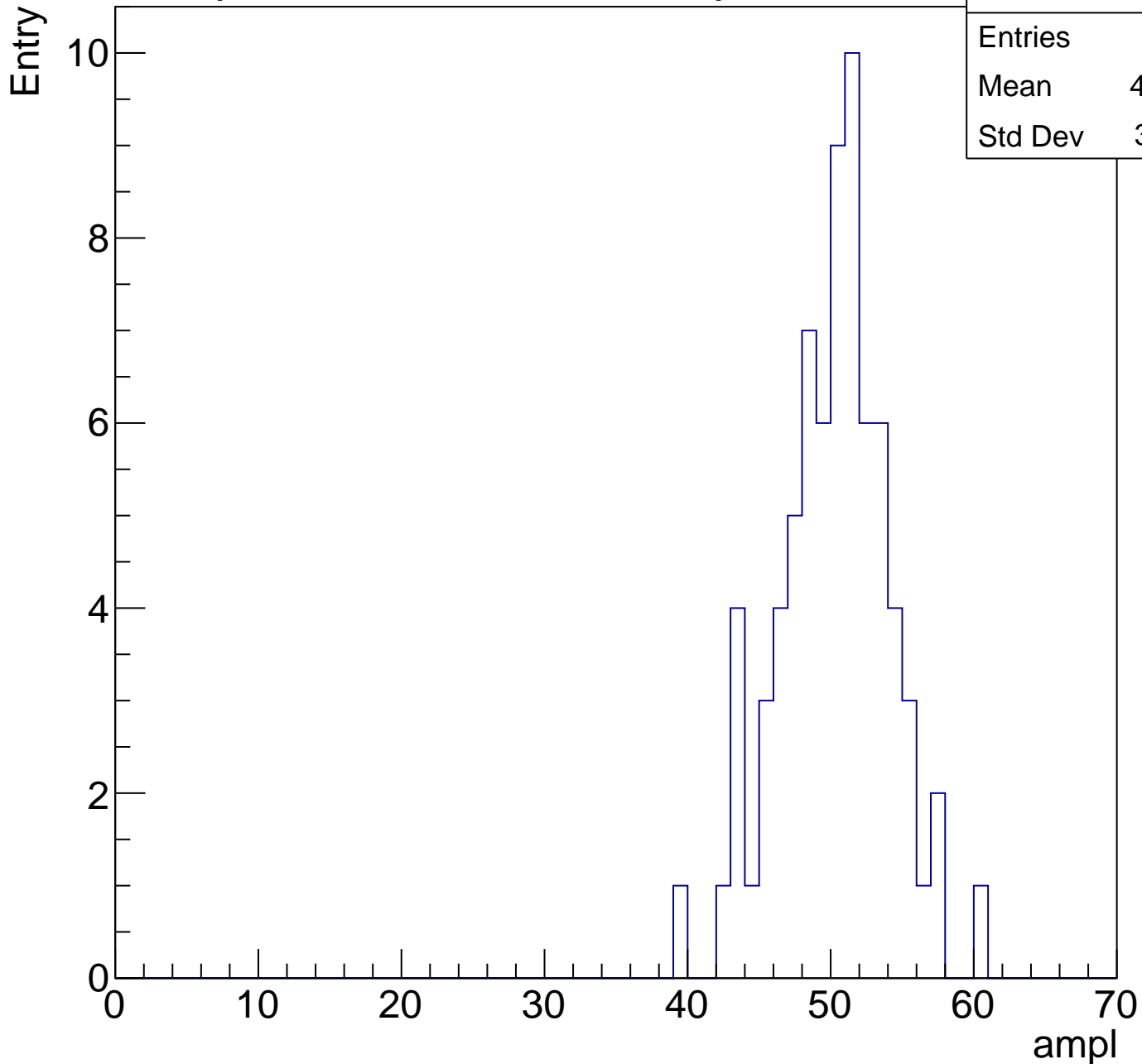
**Gaus Width: 4.1799**



# B1L101S, U20-ch117, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	74
Mean	49.76
Std Dev	3.841

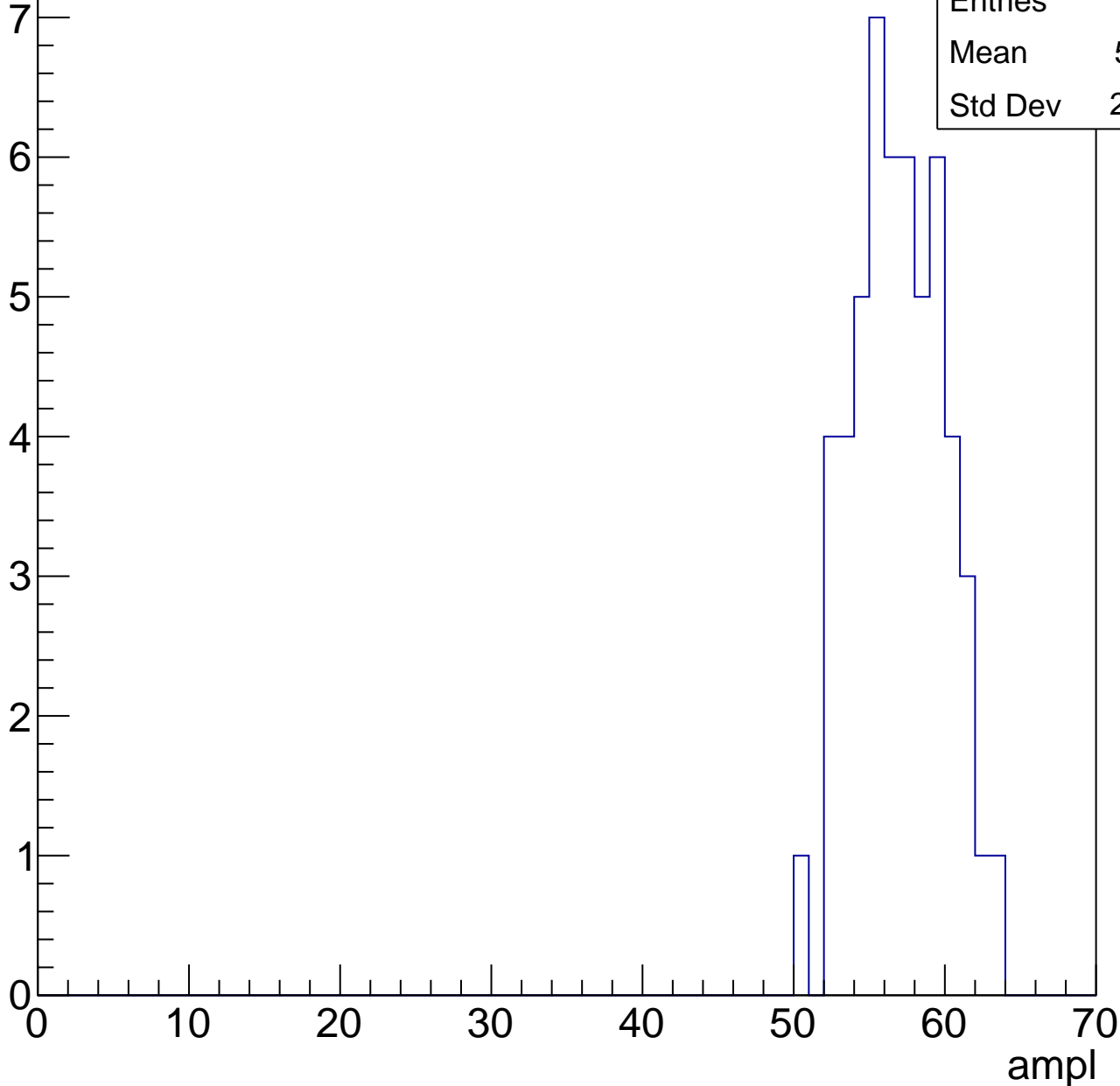


# B1L101S, U20-ch117, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	53
Mean	56.51
Std Dev	2.924

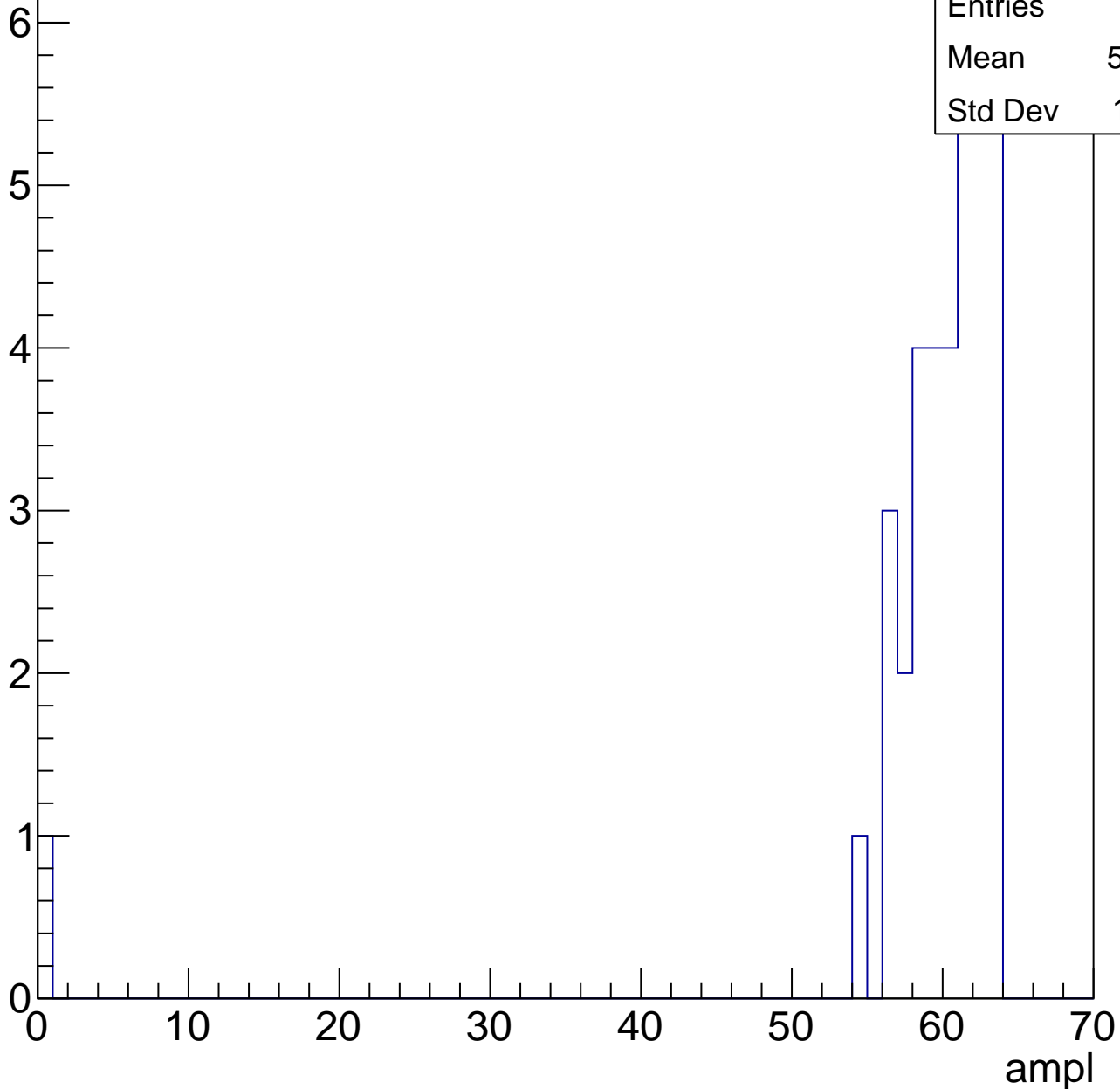


# B1L101S, U20-ch117, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

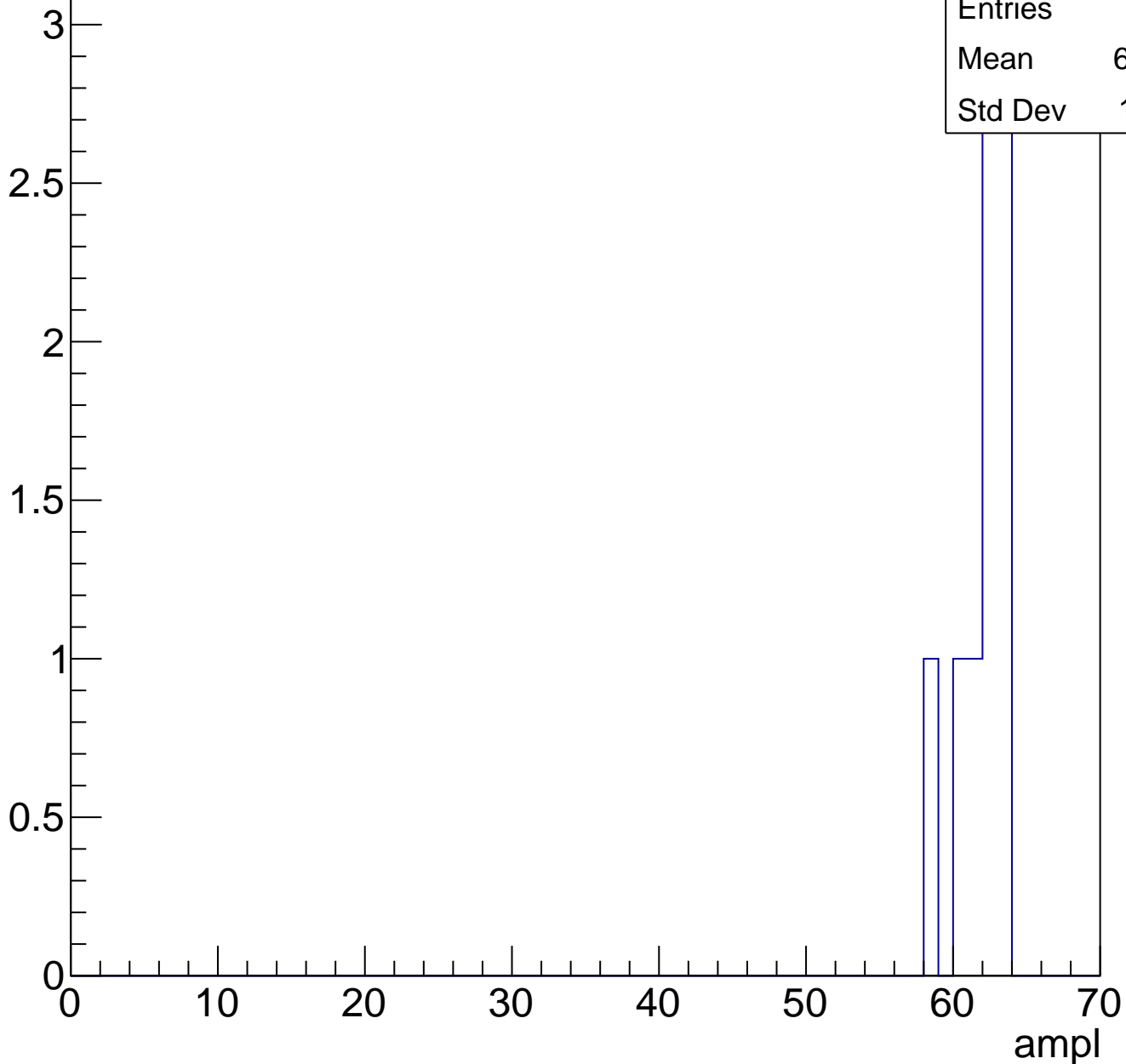
Entries	37
Mean	58.38
Std Dev	10.01



# B1L101S, U20-ch117, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

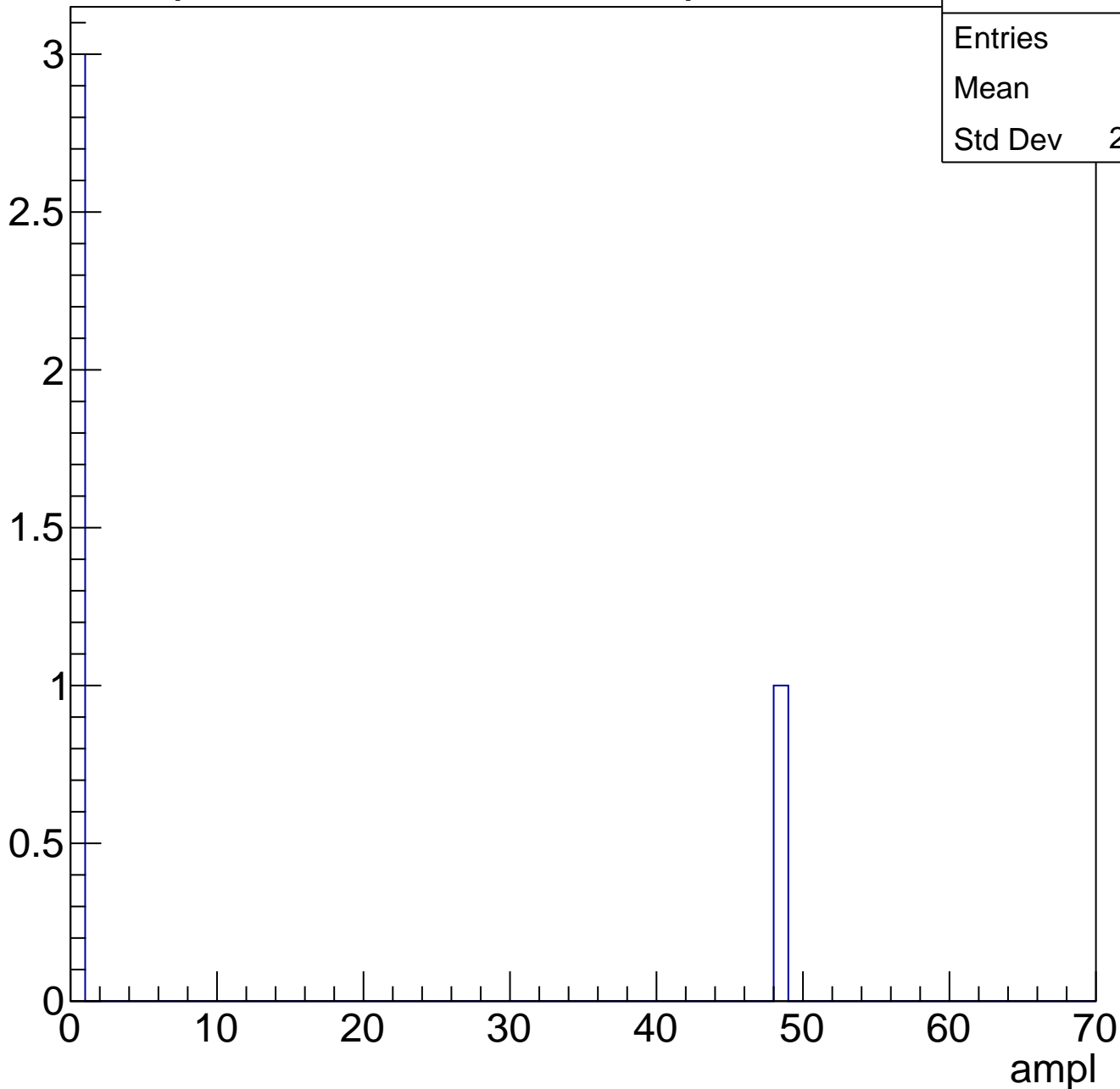




# B1L101S, U20-ch117, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U20-ch118, adc0

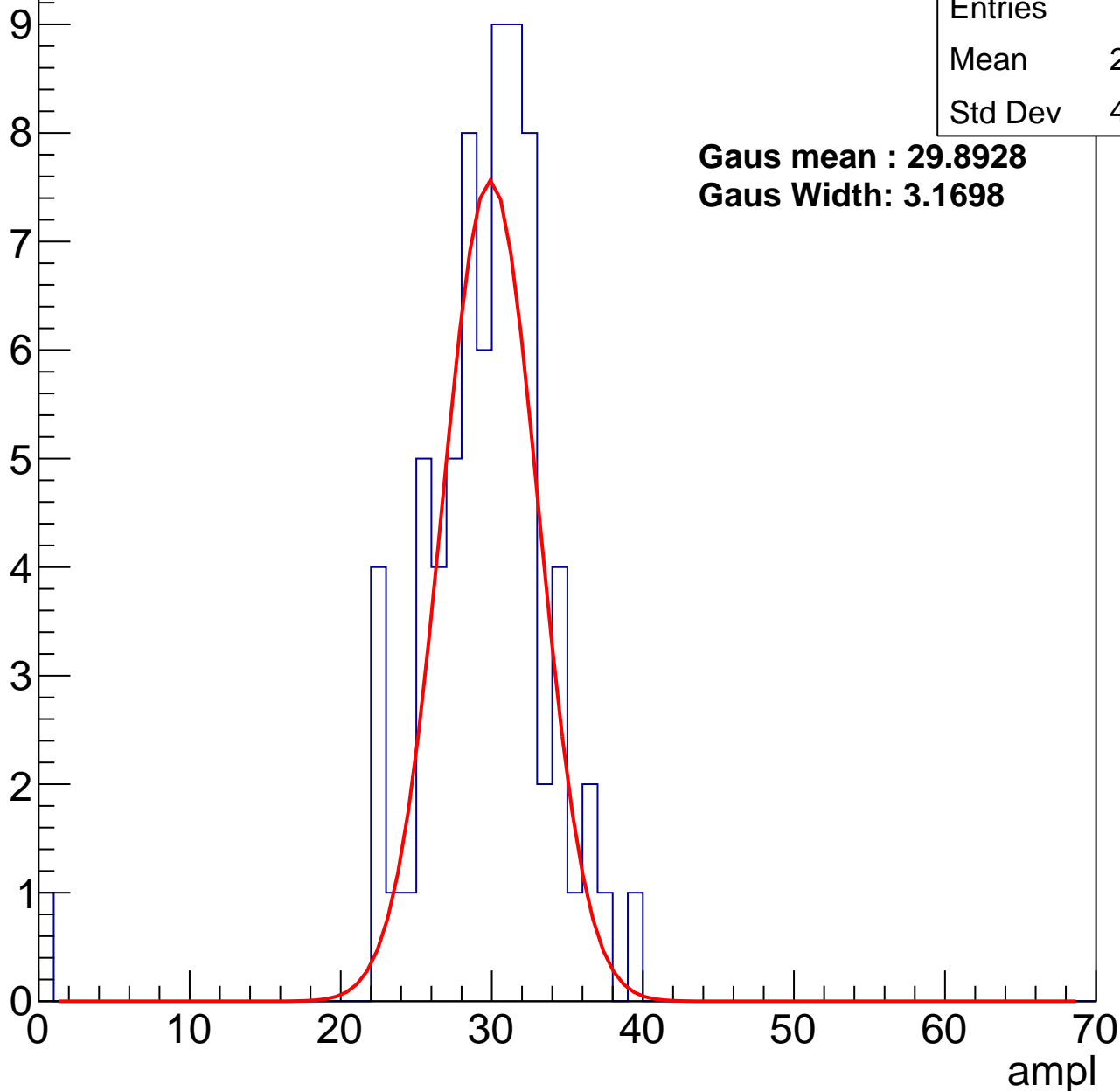
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	72
Mean	28.99
Std Dev	4.985

**Gaus mean : 29.8928**

**Gaus Width: 3.1698**



# B1L101S, U20-ch118, adc1

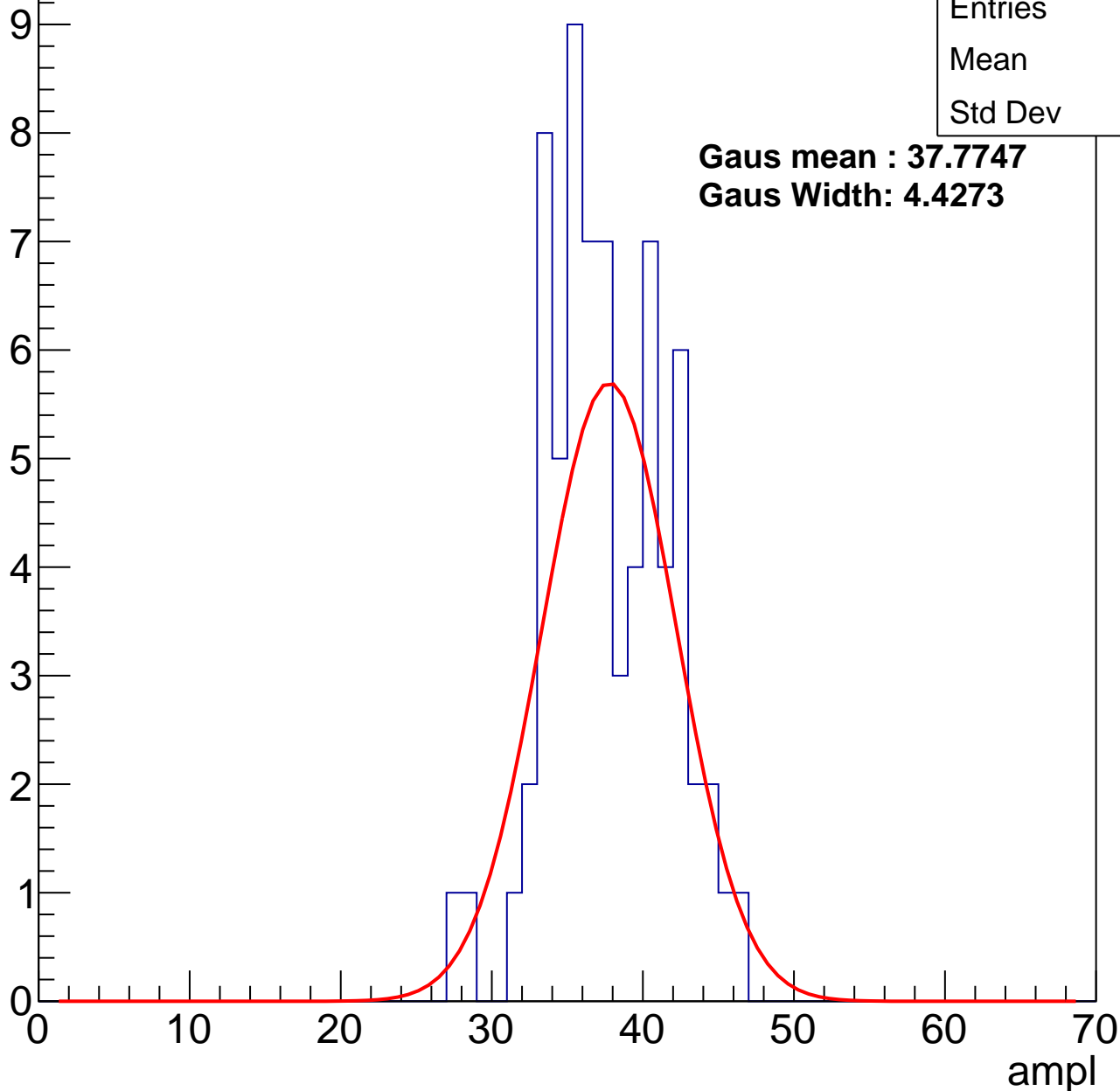
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	71
Mean	37.2
Std Dev	3.92

**Gaus mean : 37.7747**

**Gaus Width: 4.4273**



# B1L101S, U20-ch118, adc2

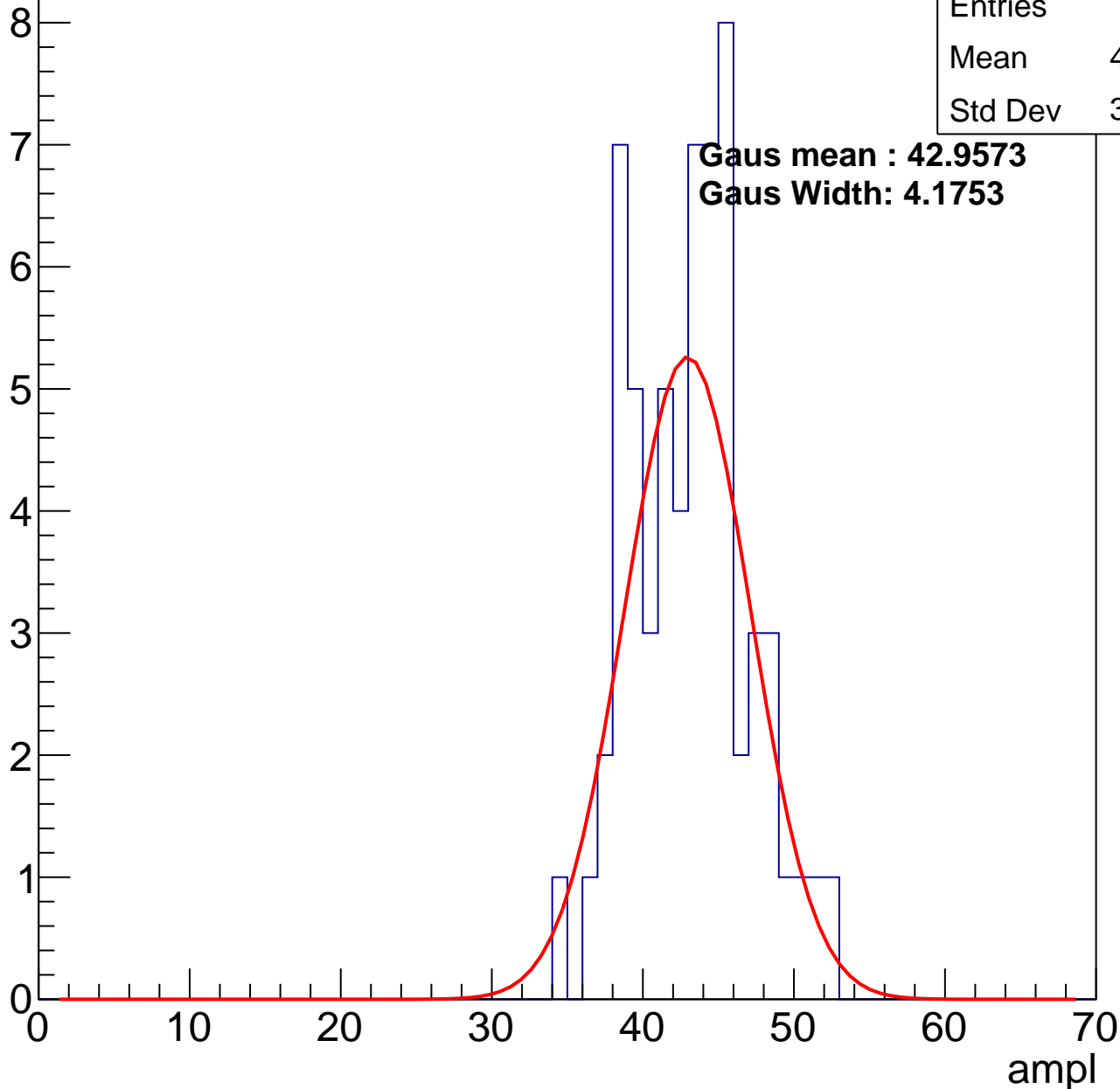
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	42.68
Std Dev	3.834

**Gaus mean : 42.9573**

**Gaus Width: 4.1753**

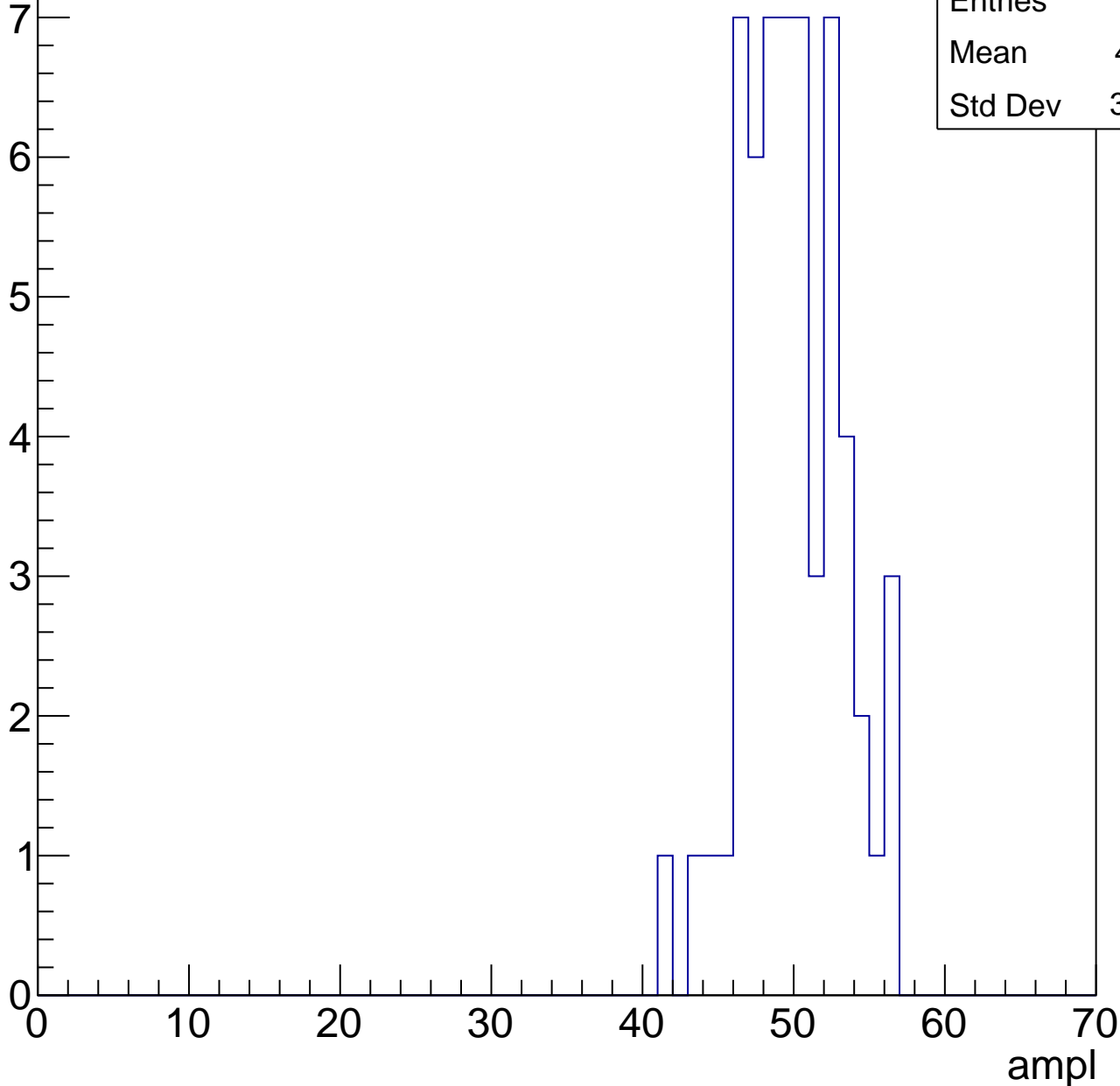


# B1L101S, U20-ch118, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	58
Mean	49.41
Std Dev	3.227

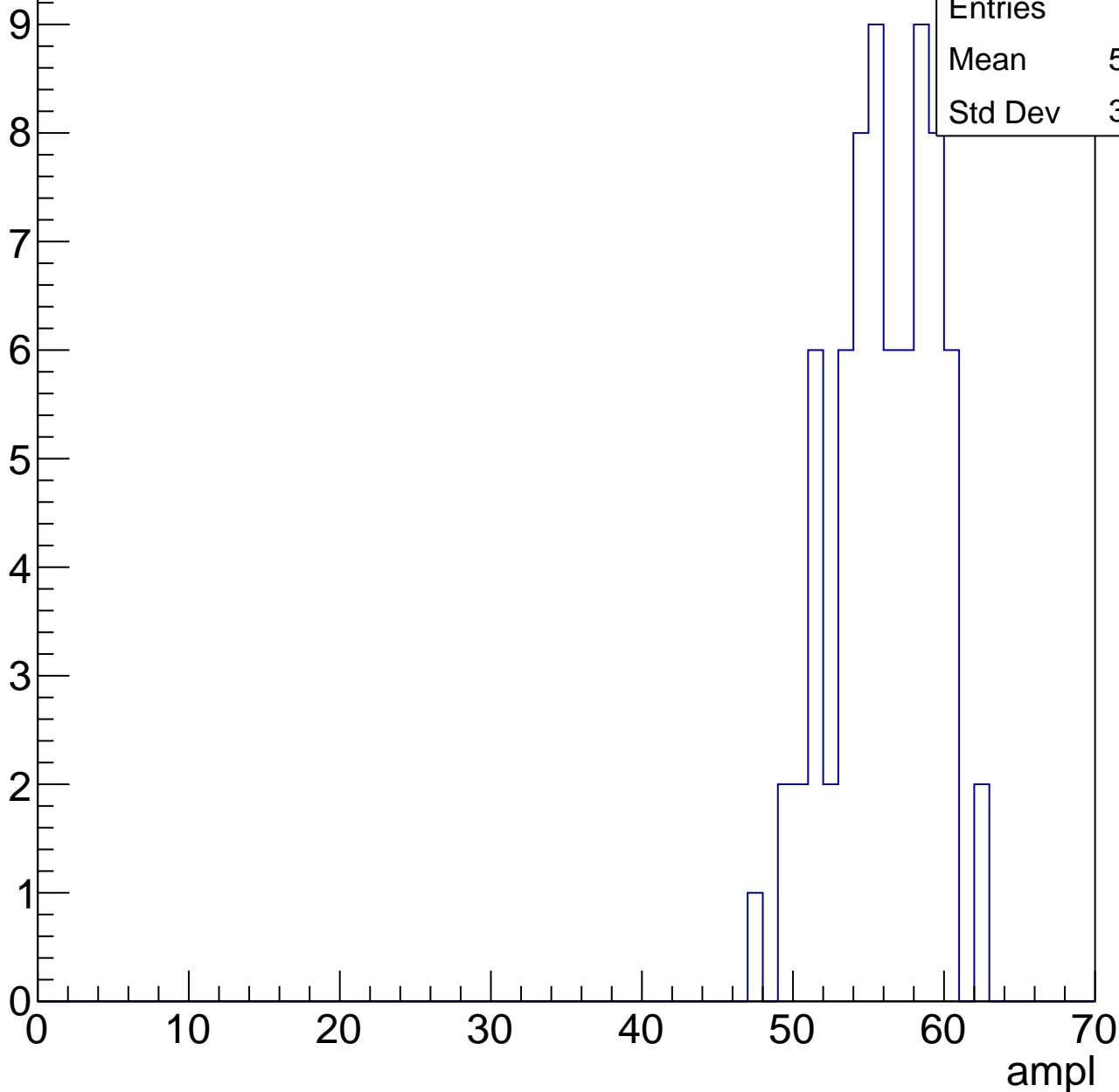


# B1L101S, U20-ch118, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	73
Mean	55.56
Std Dev	3.302

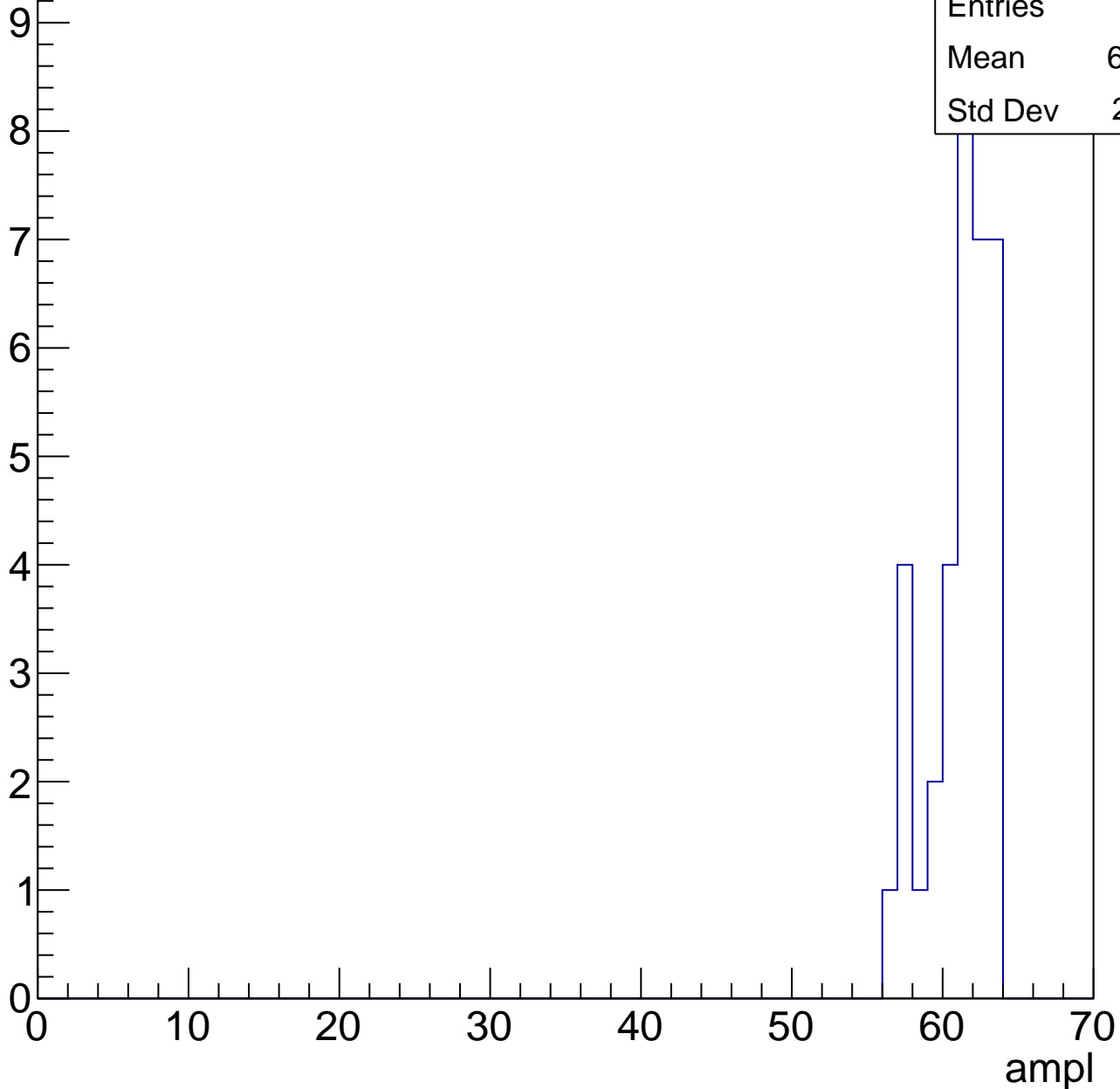


# B1L101S, U20-ch118, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	35
Mean	60.69
Std Dev	2.011



# B1L101S, U20-ch118, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

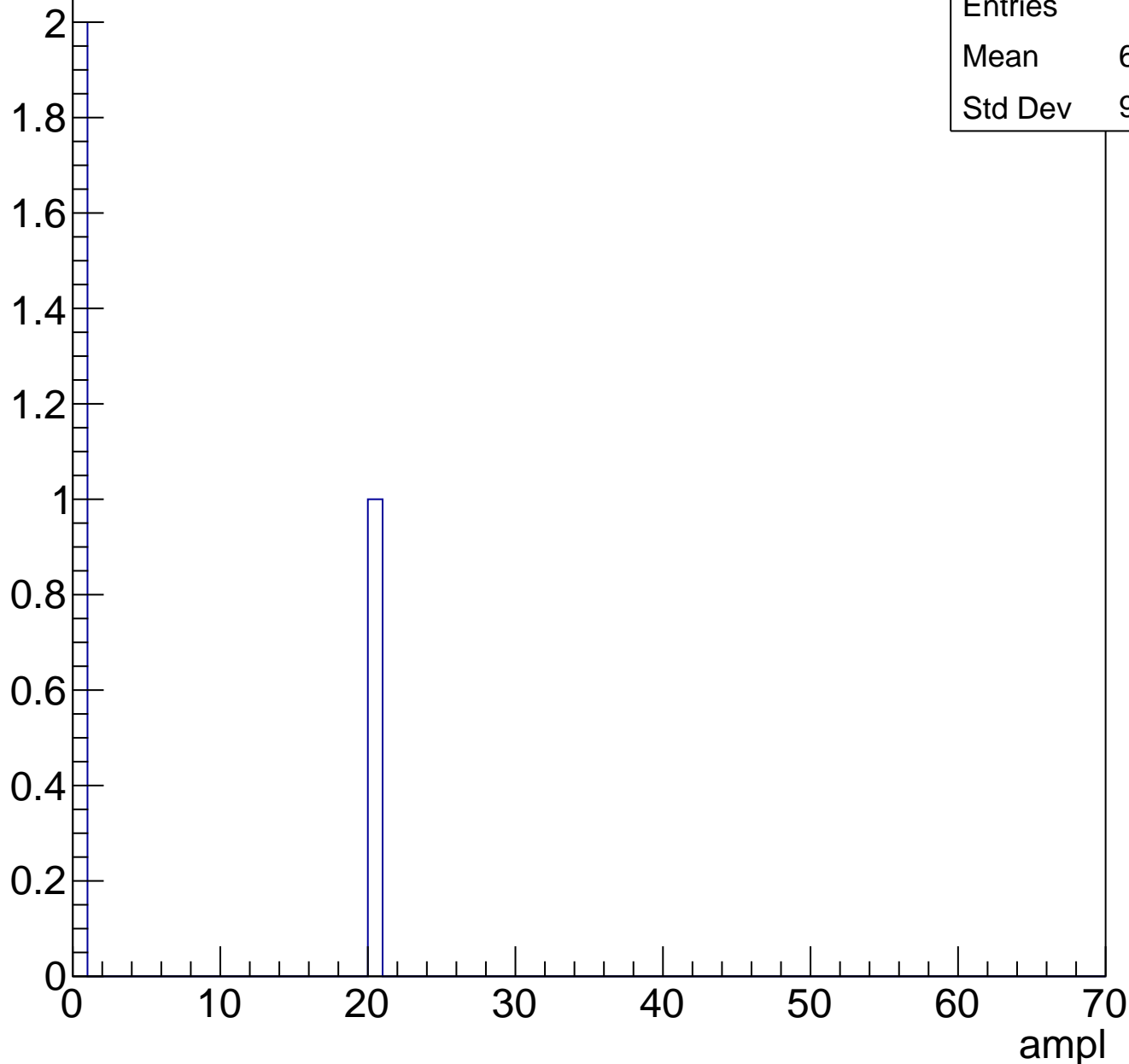




# B1L101S, U20-ch118, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	3
Mean	6.667
Std Dev	9.428

# B1L101S, U20-ch119, adc0

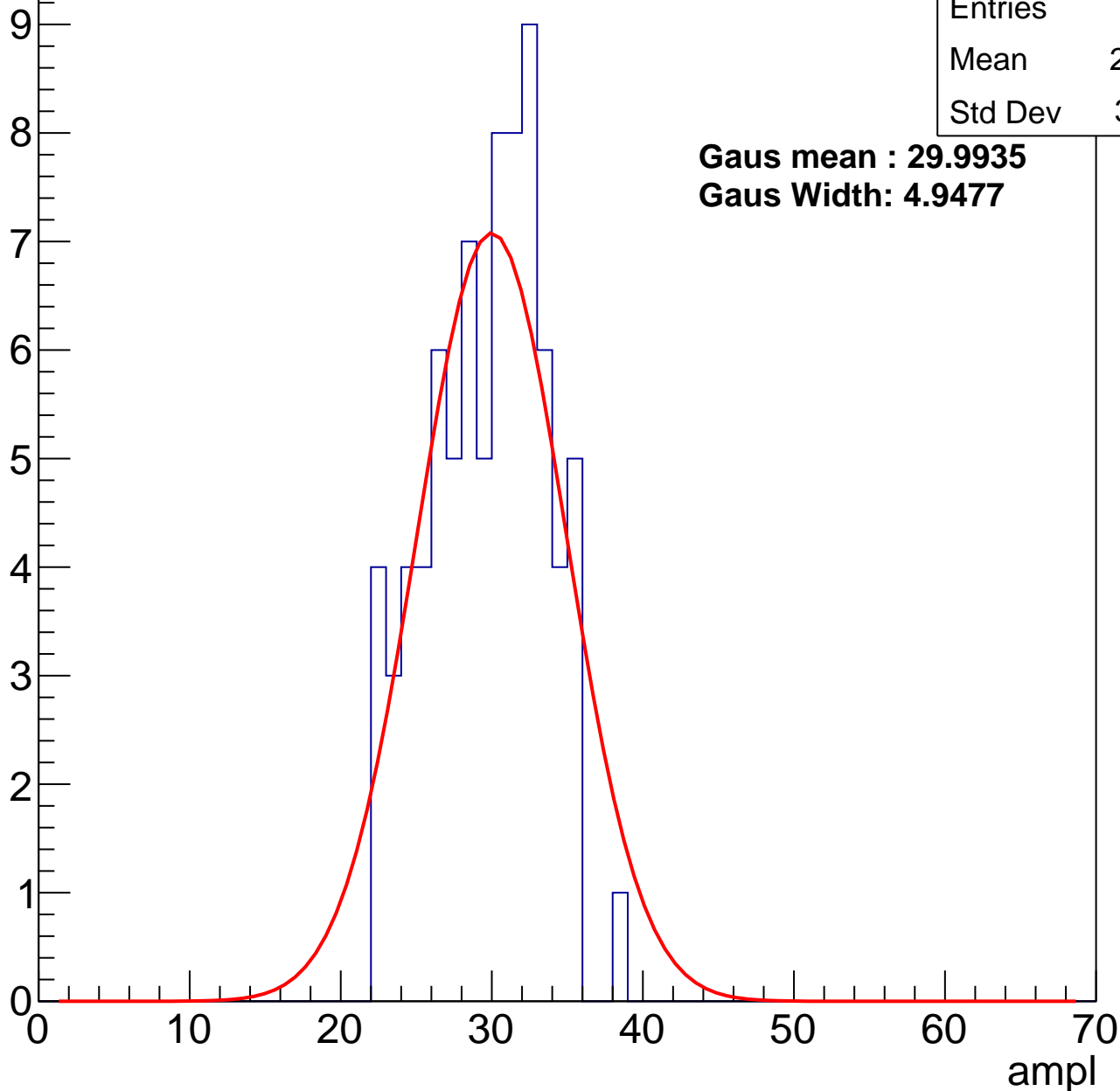
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	79
Mean	29.22
Std Dev	3.771

**Gaus mean : 29.9935**

**Gaus Width: 4.9477**



# B1L101S, U20-ch119, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	75
Mean	37.13
Std Dev	3.575

**Gaus mean : 37.7815**

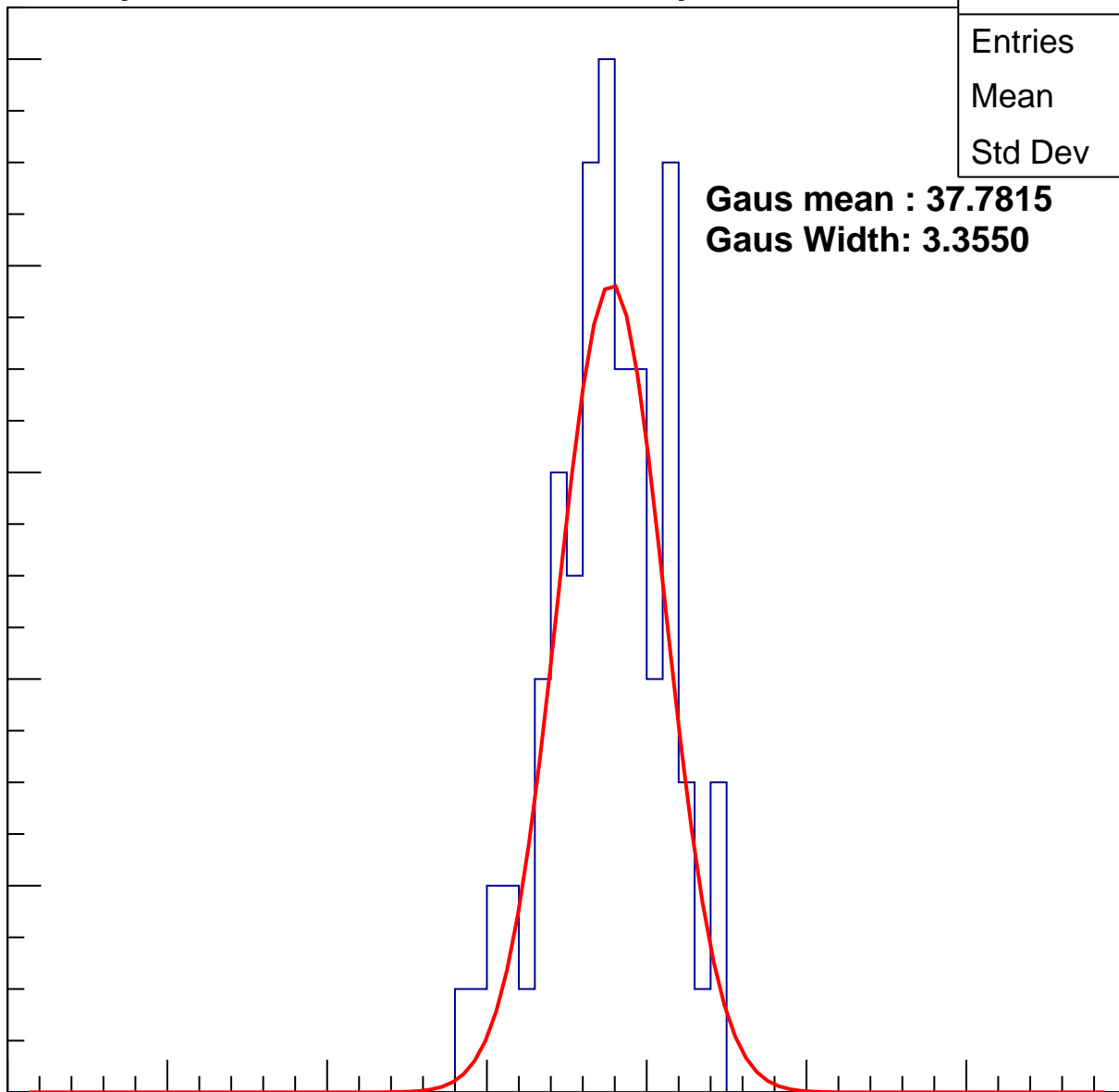
**Gaus Width: 3.3550**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B1L101S, U20-ch119, adc2

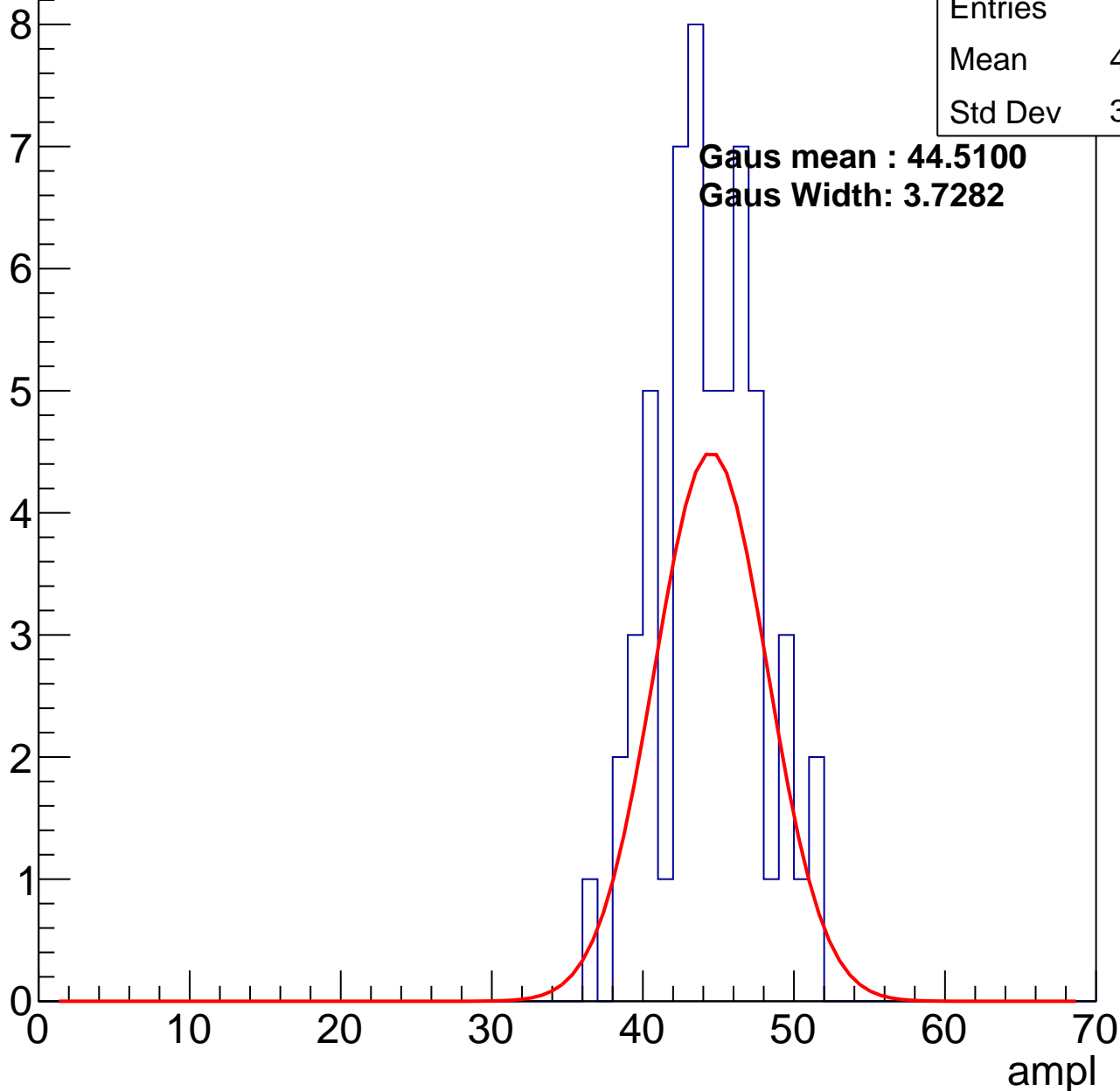
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	56
Mean	43.88
Std Dev	3.376

**Gaus mean : 44.5100**

**Gaus Width: 3.7282**

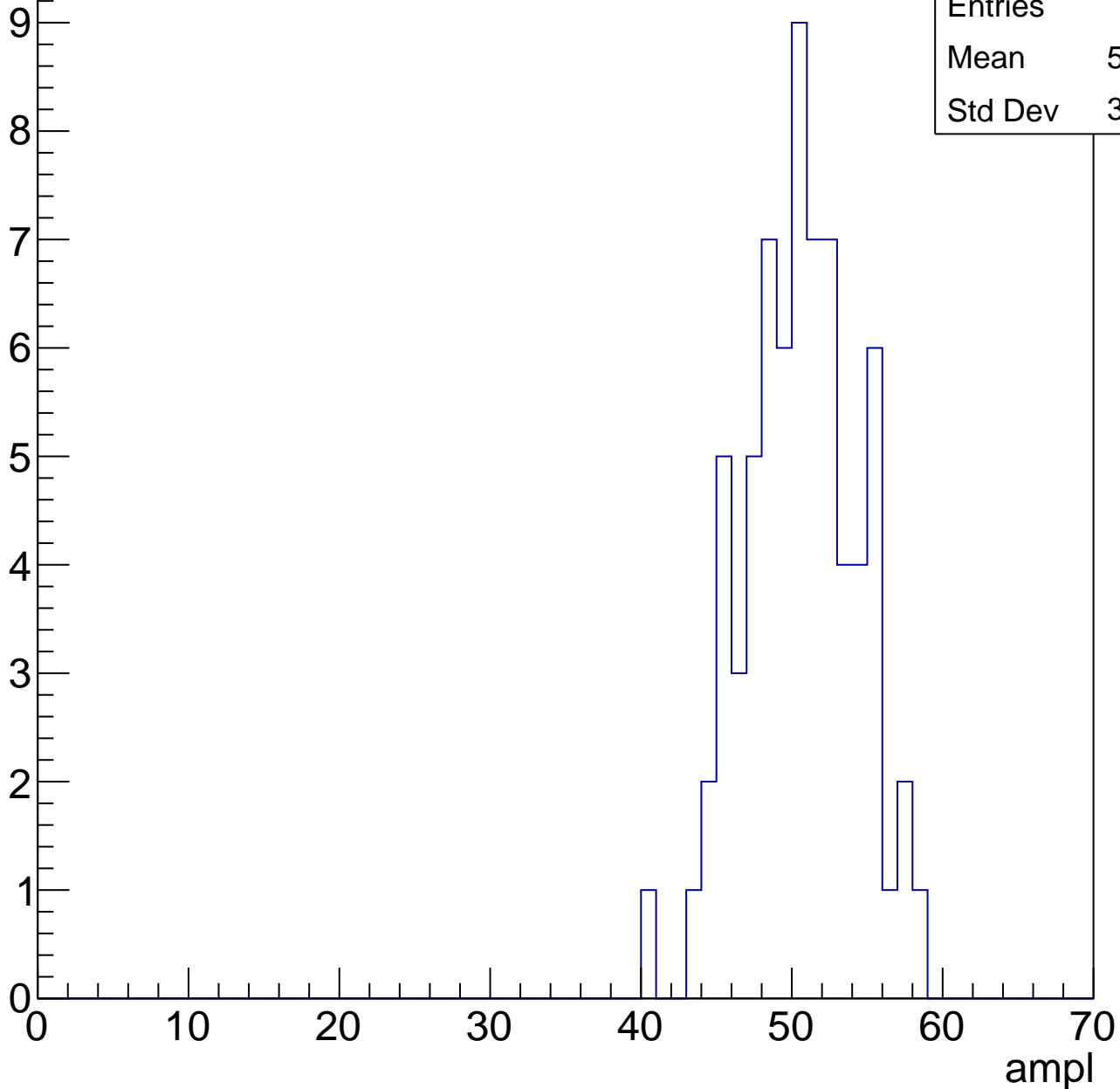


# B1L101S, U20-ch119, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	71
Mean	50.08
Std Dev	3.668

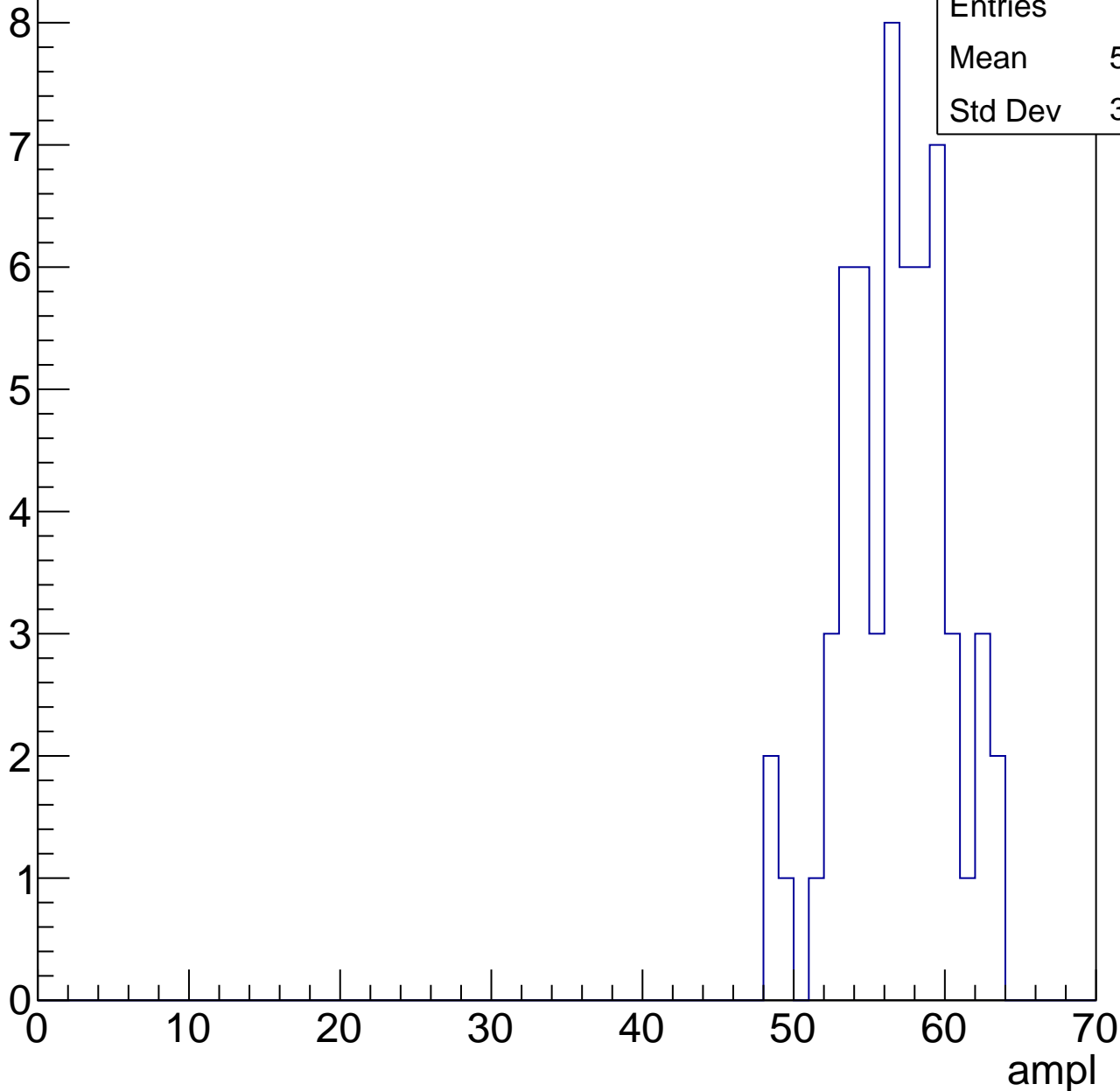


# B1L101S, U20-ch119, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	58
Mean	56.26
Std Dev	3.472

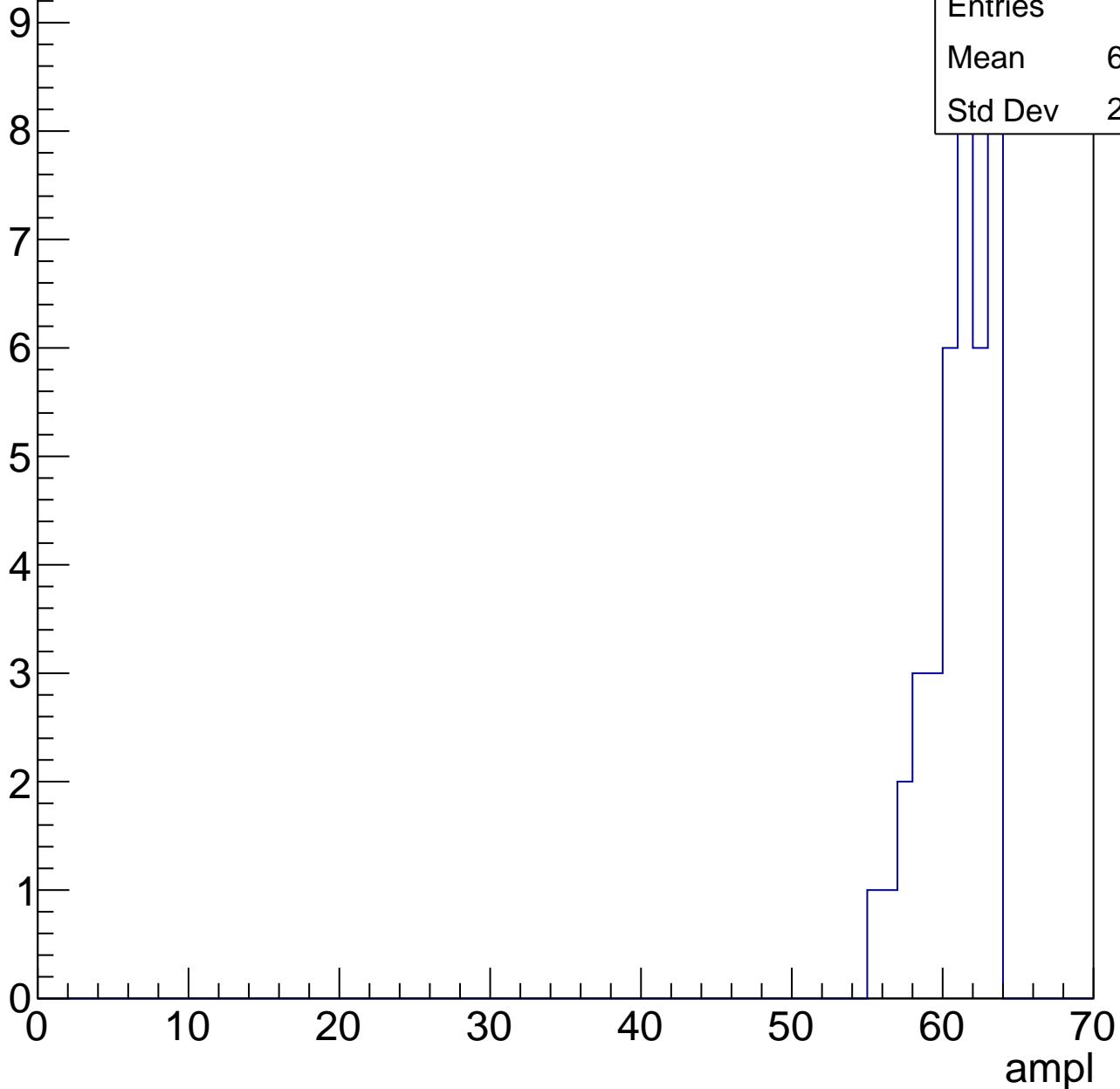


# B1L101S, U20-ch119, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

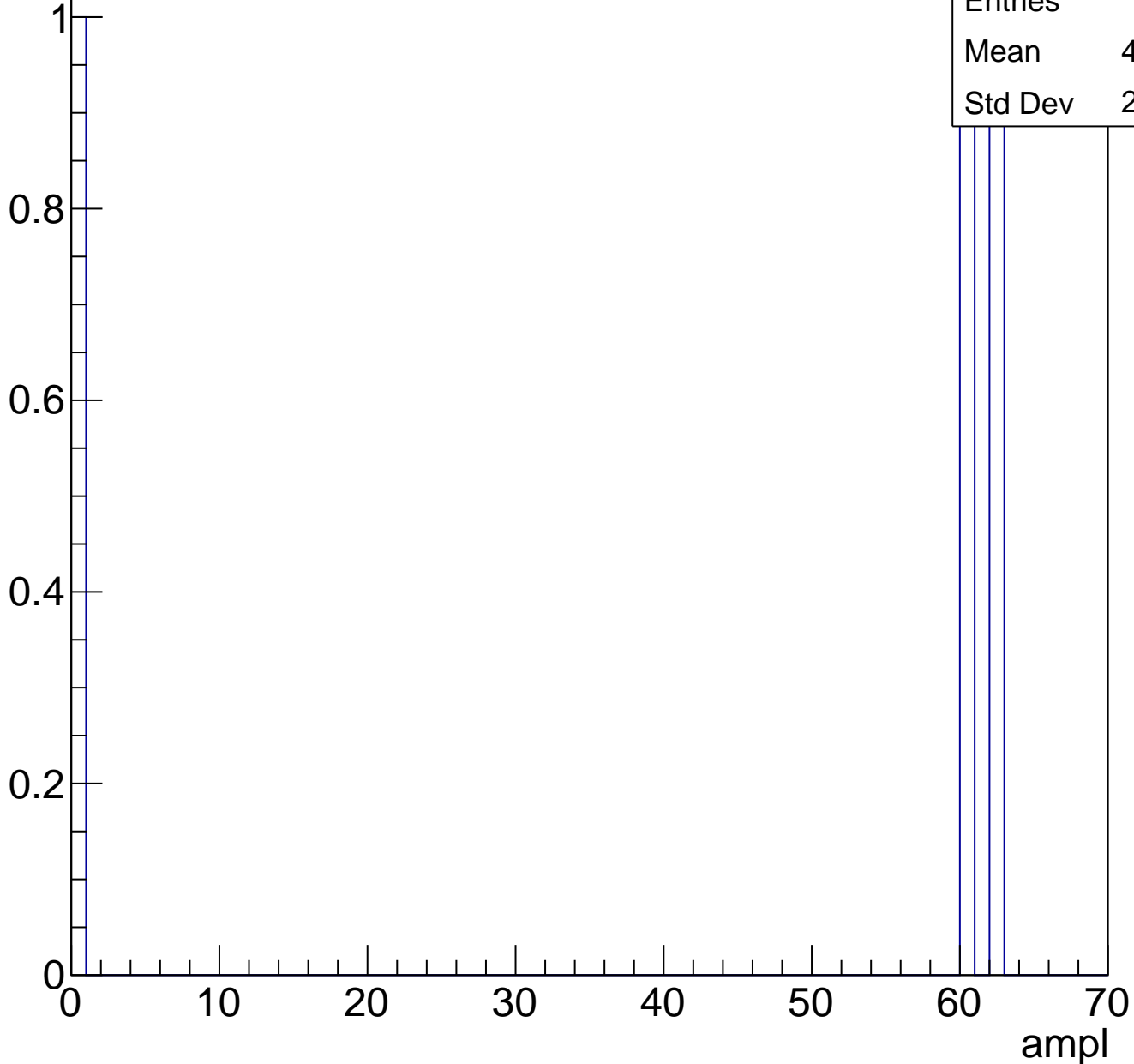
Entries	39
Mean	60.54
Std Dev	2.074



# B1L101S, U20-ch119, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U20-ch119, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U20-ch120, adc0

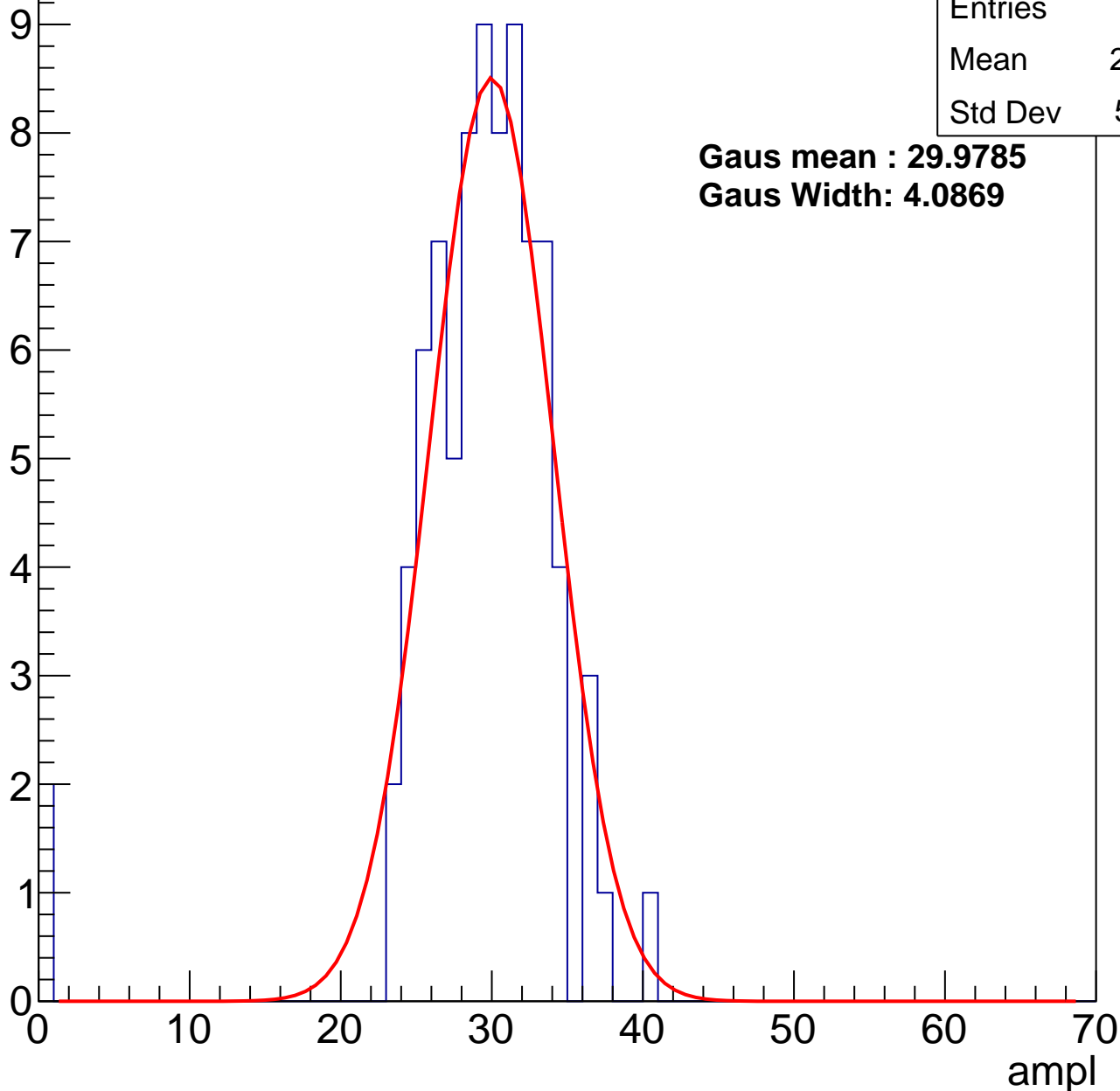
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	83
Mean	28.78
Std Dev	5.691

**Gaus mean : 29.9785**

**Gaus Width: 4.0869**



# B1L101S, U20-ch120, adc1

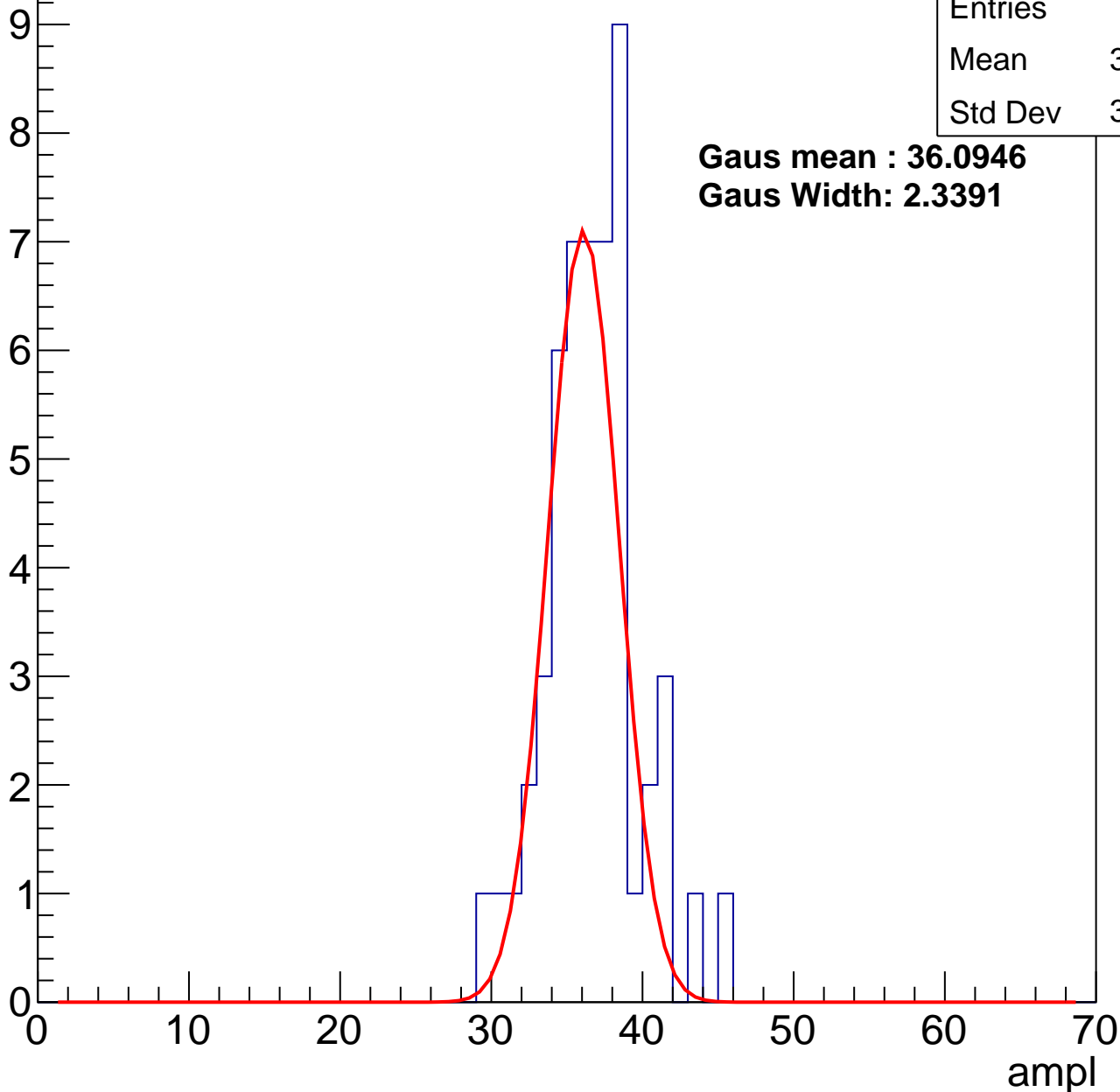
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	52
Mean	36.25
Std Dev	3.056

**Gaus mean : 36.0946**

**Gaus Width: 2.3391**



# B1L101S, U20-ch120, adc2

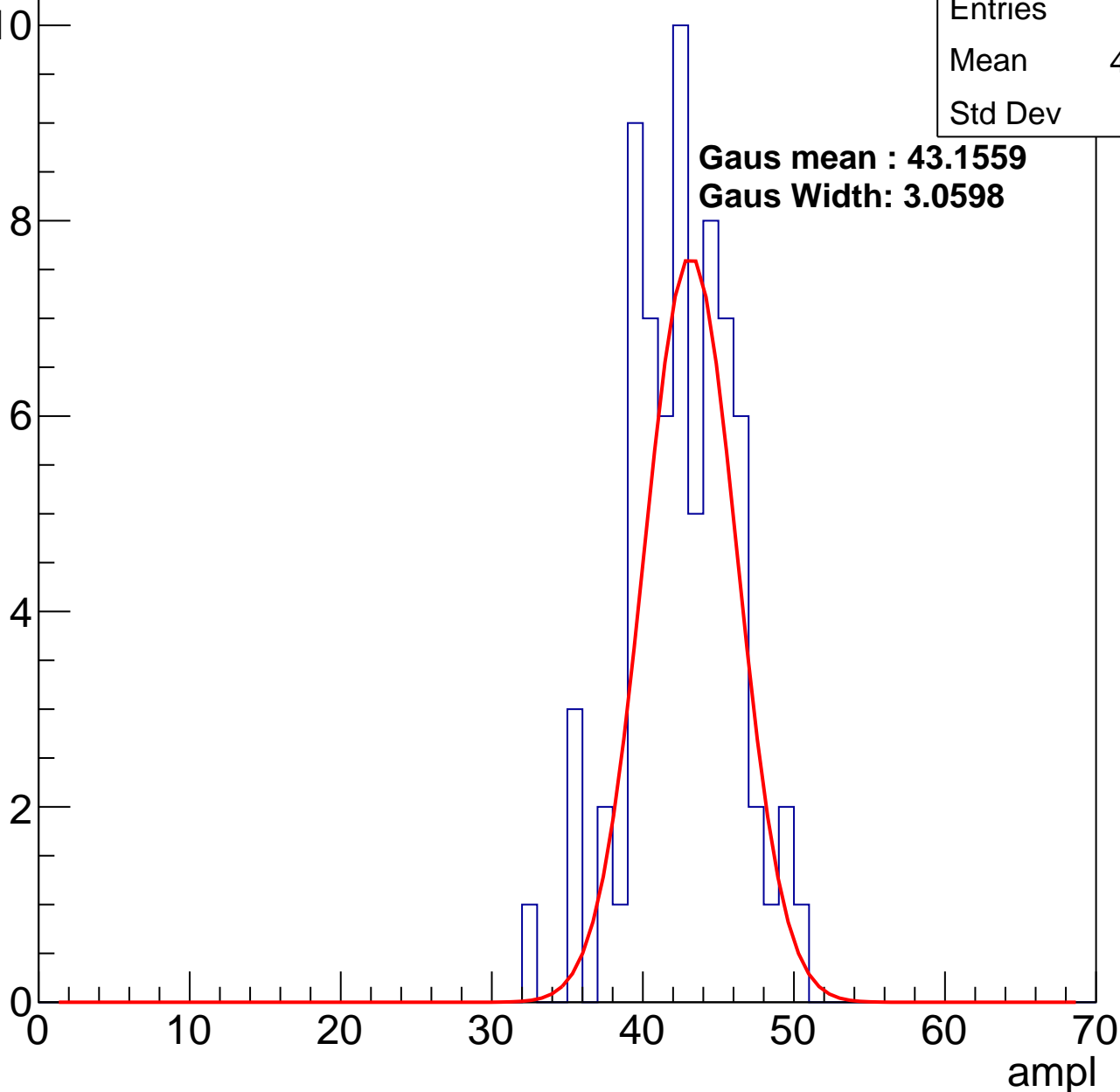
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	71
Mean	42.17
Std Dev	3.5

**Gaus mean : 43.1559**

**Gaus Width: 3.0598**

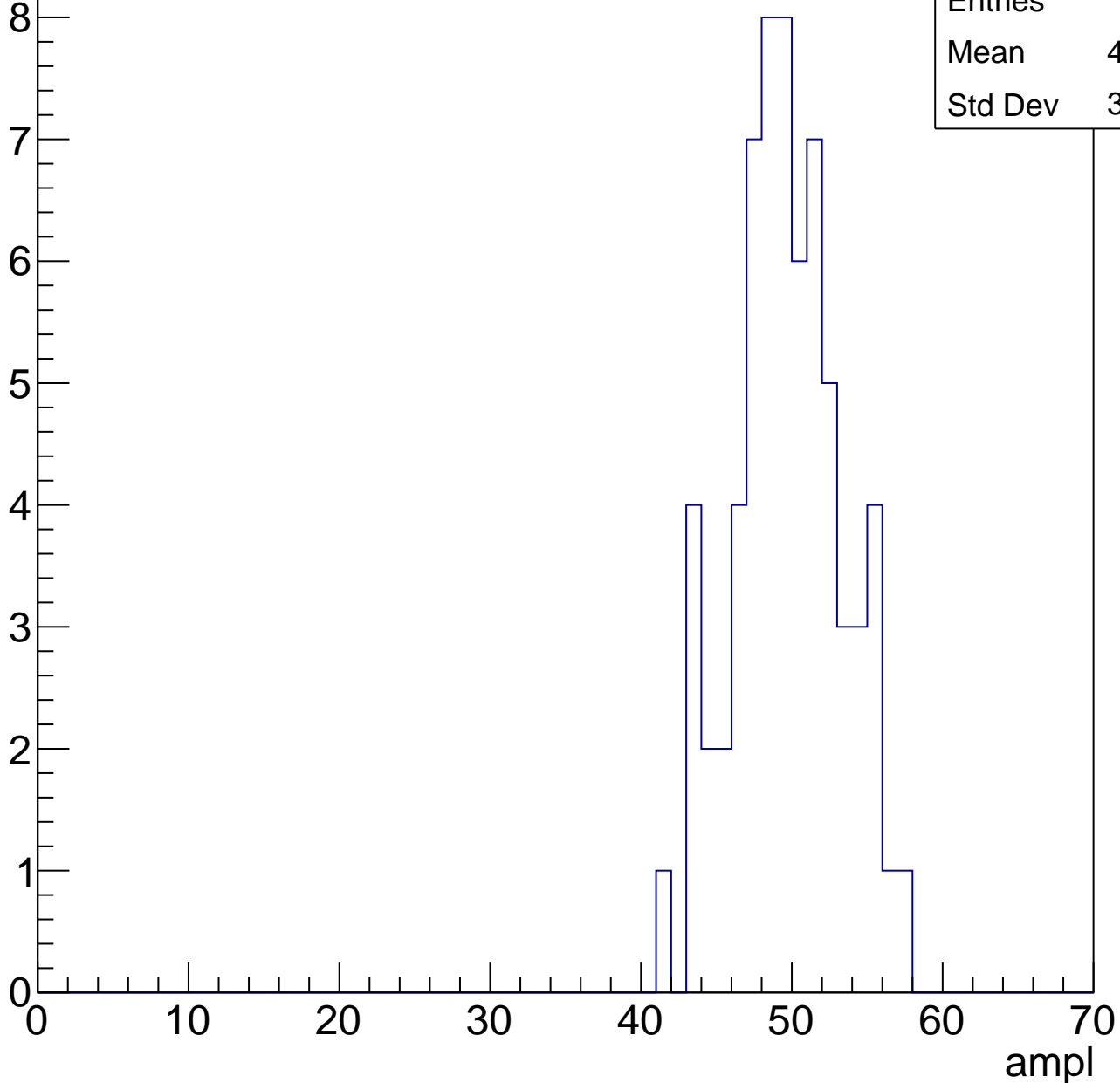


# B1L101S, U20-ch120, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	66
Mean	49.26
Std Dev	3.518

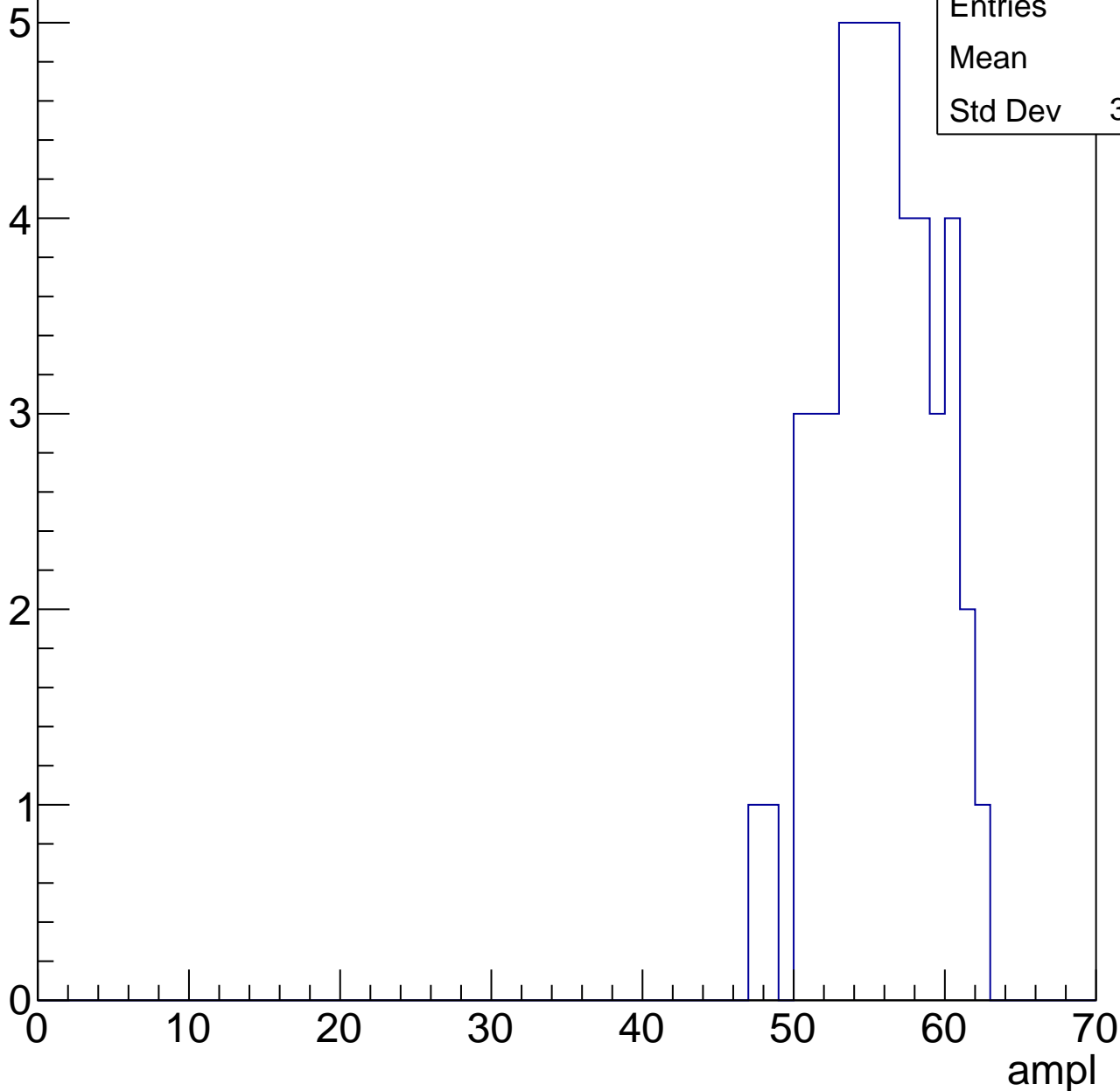


# B1L101S, U20-ch120, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	49
Mean	55.2
Std Dev	3.534

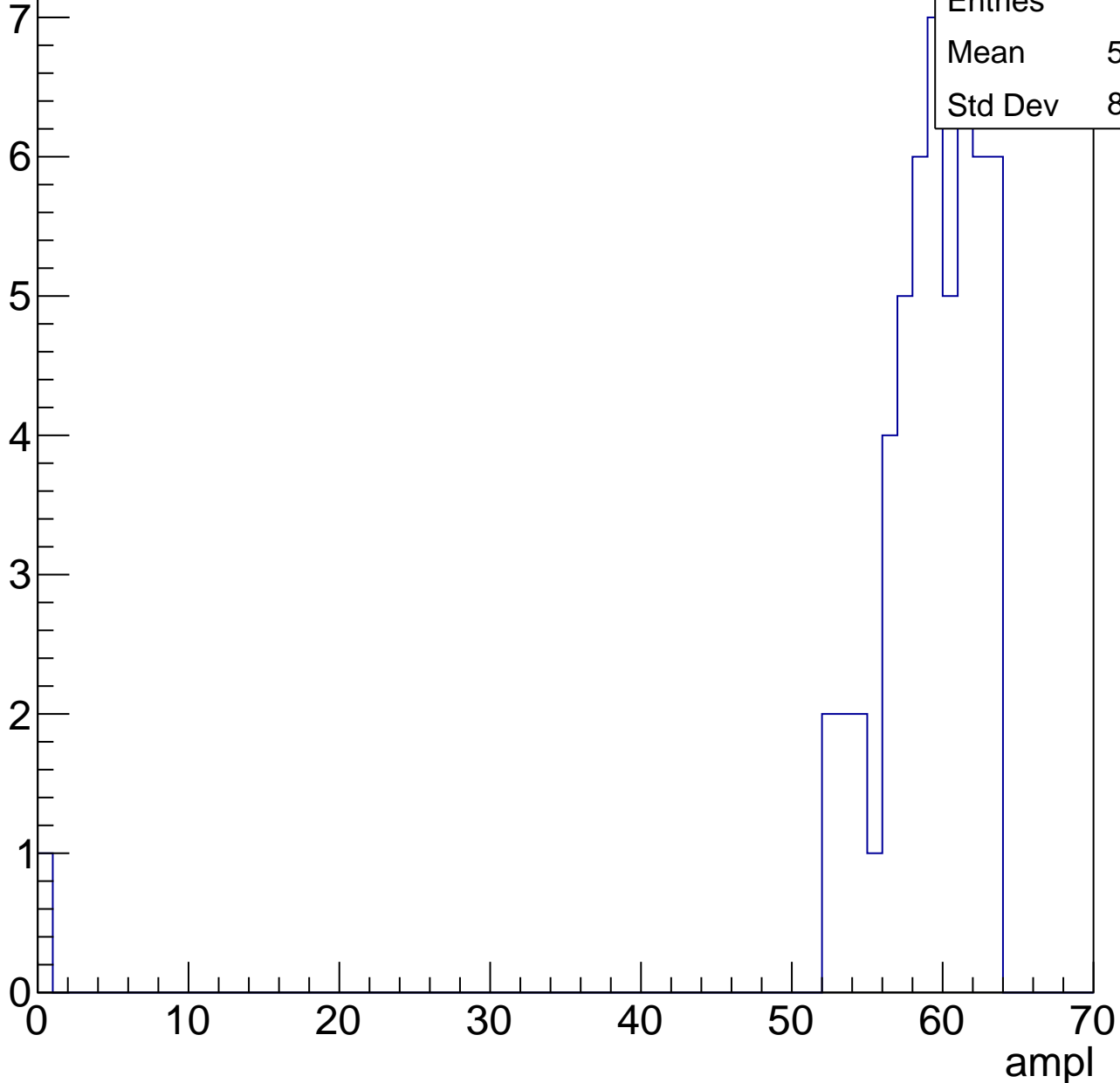


# B1L101S, U20-ch120, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	54
Mean	57.78
Std Dev	8.478



# B1L101S, U20-ch120, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U20-ch120, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U20-ch121, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	81
Mean	29.51
Std Dev	6.952

**Gaus mean : 31.4779**

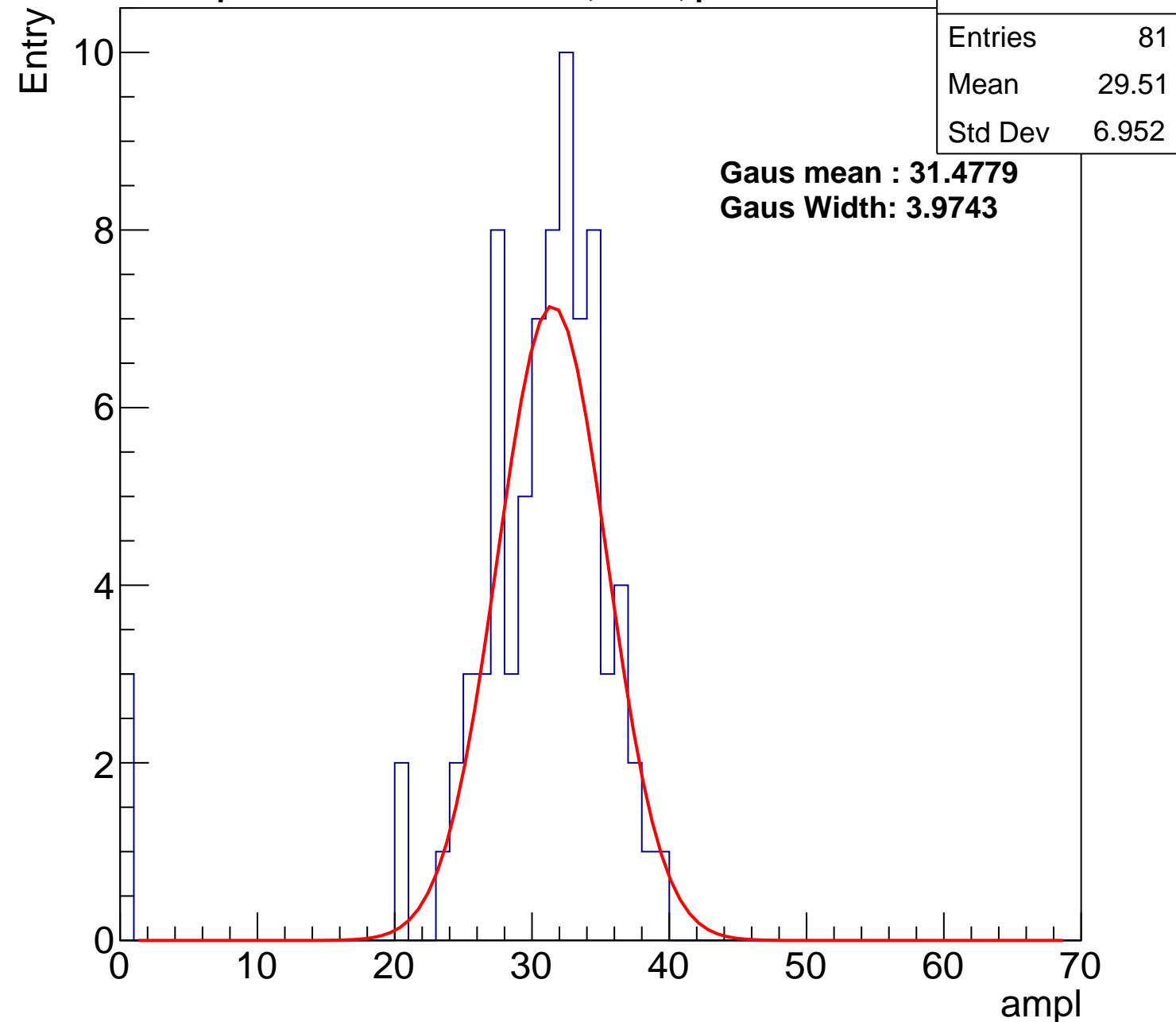
**Gaus Width: 3.9743**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U20-ch121, adc1

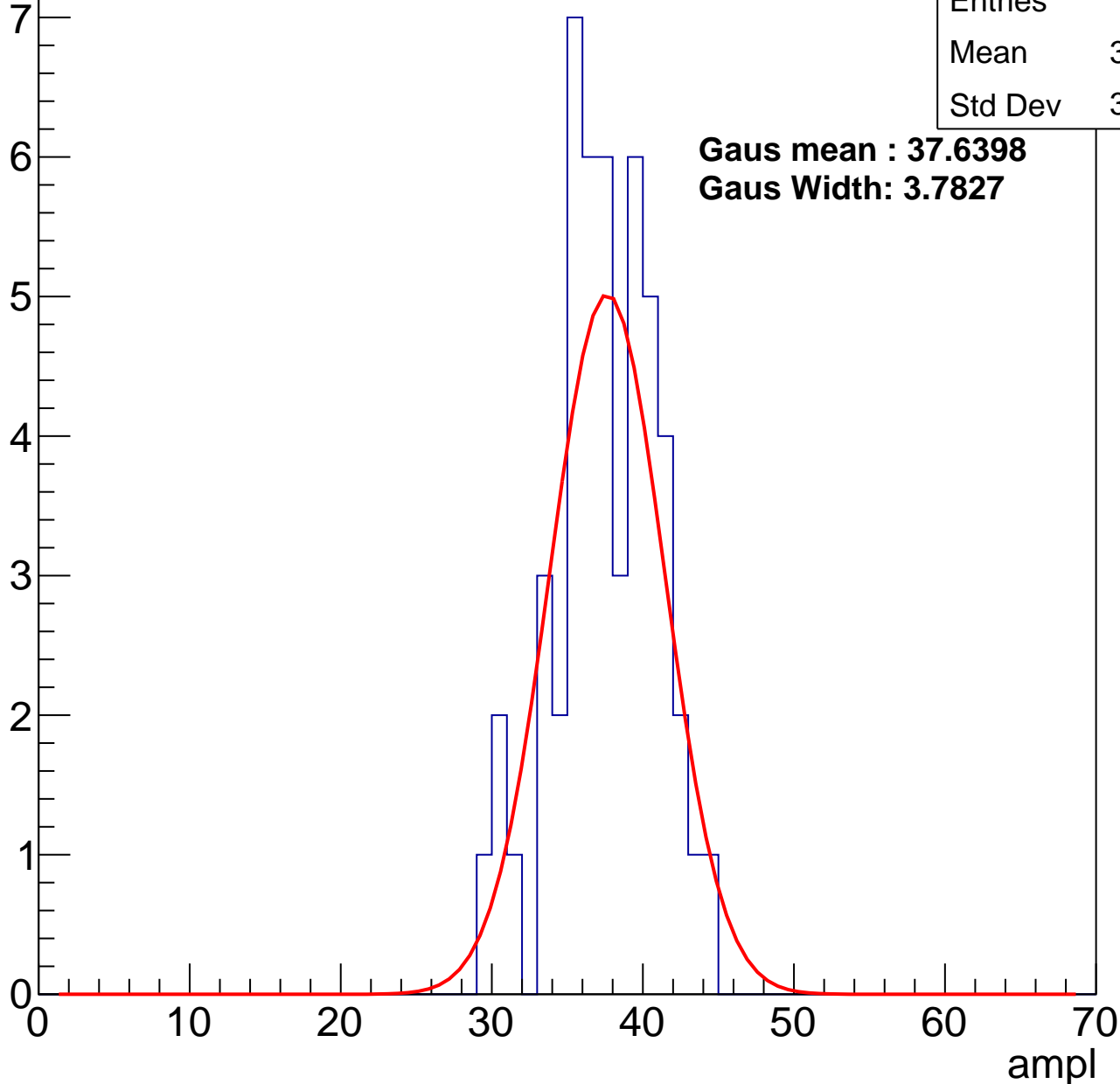
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	50
Mean	37.06
Std Dev	3.373

**Gaus mean : 37.6398**

**Gaus Width: 3.7827**



# B1L101S, U20-ch121, adc2

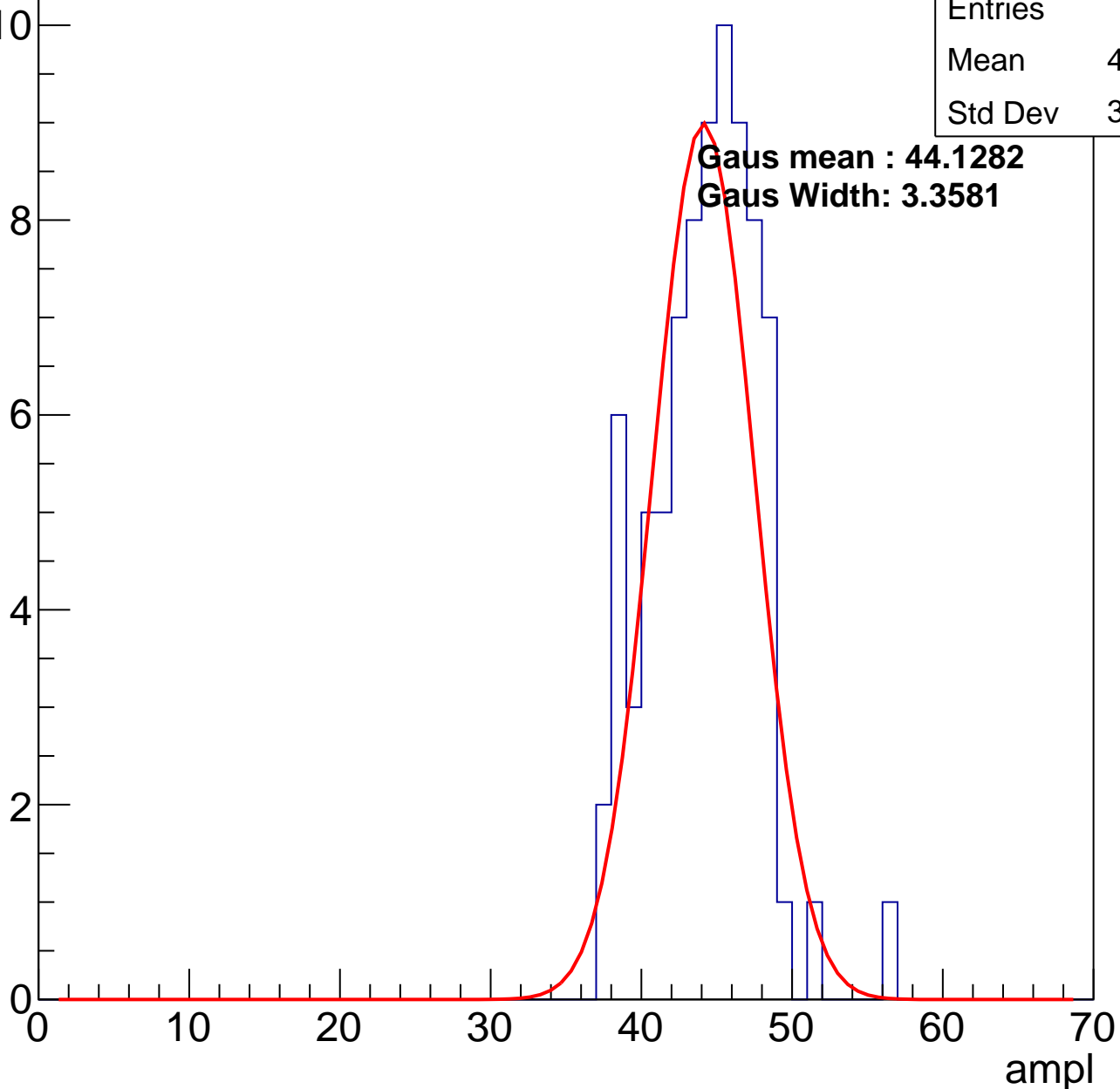
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	82
Mean	43.78
Std Dev	3.482

**Gaus mean : 44.1282**

**Gaus Width: 3.3581**

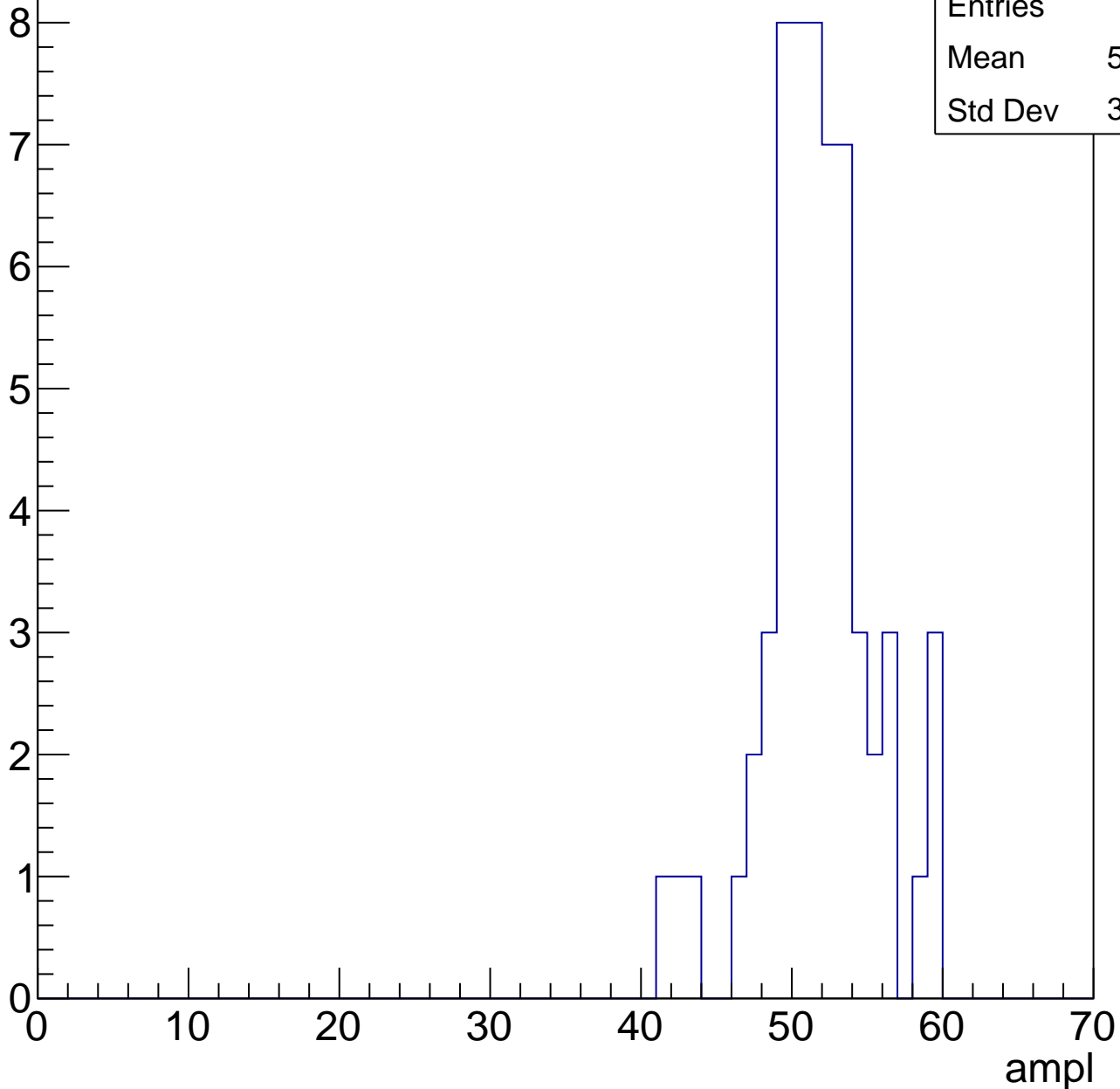


# B1L101S, U20-ch121, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

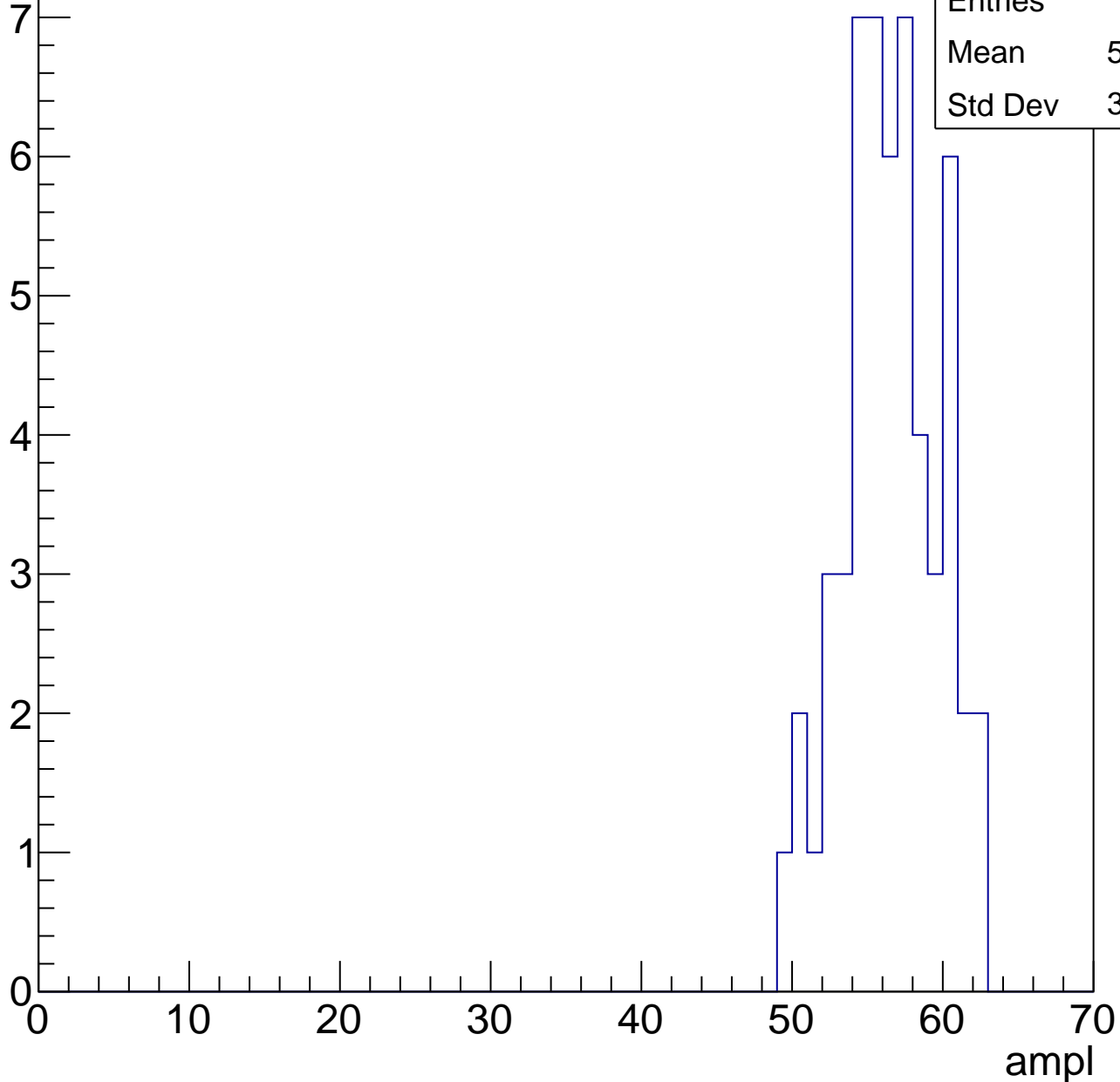
Entries	59
Mean	51.19
Std Dev	3.629



# B1L101S, U20-ch121, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



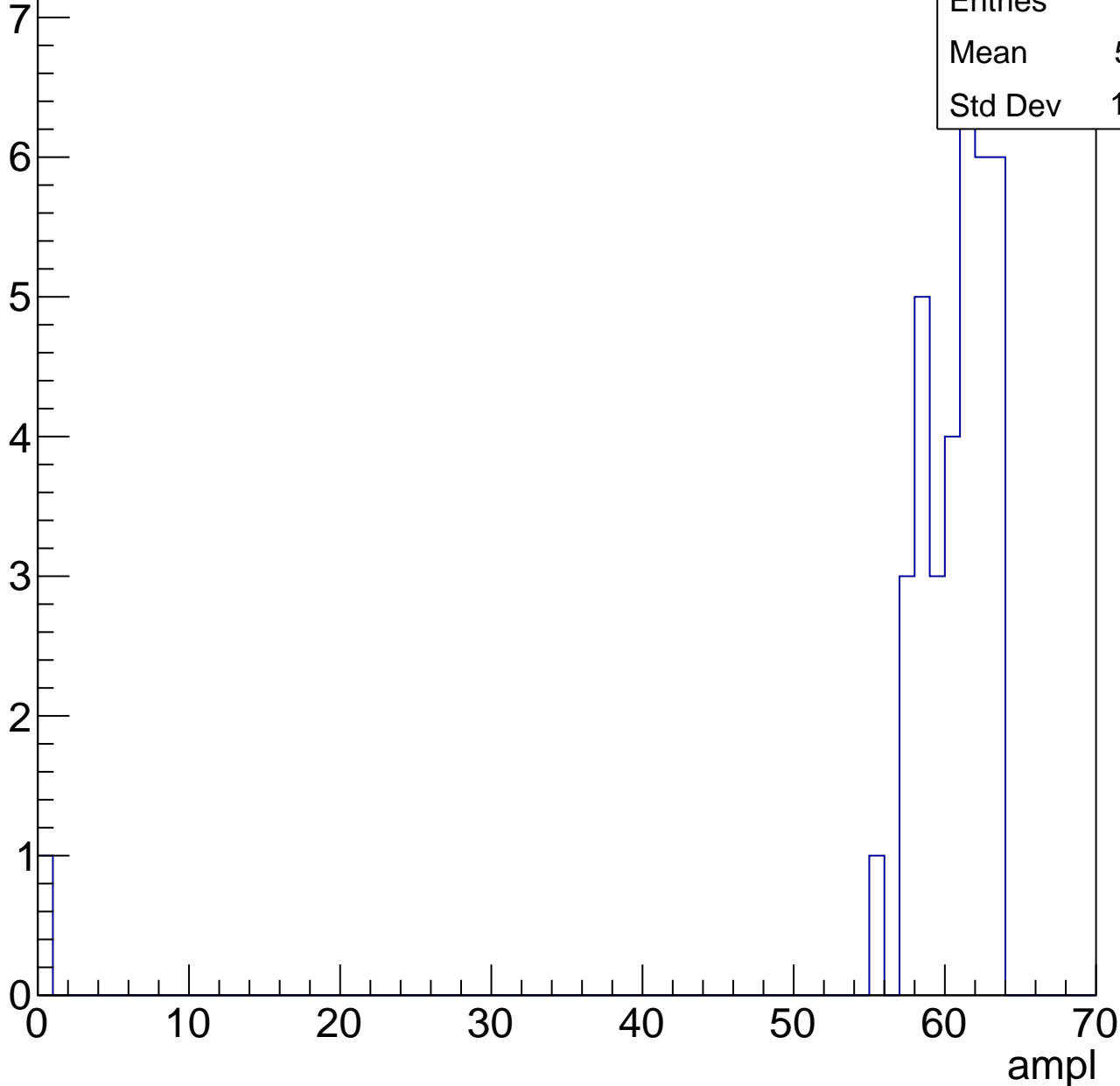
Entries	54
Mean	56.07
Std Dev	3.114

# B1L101S, U20-ch121, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

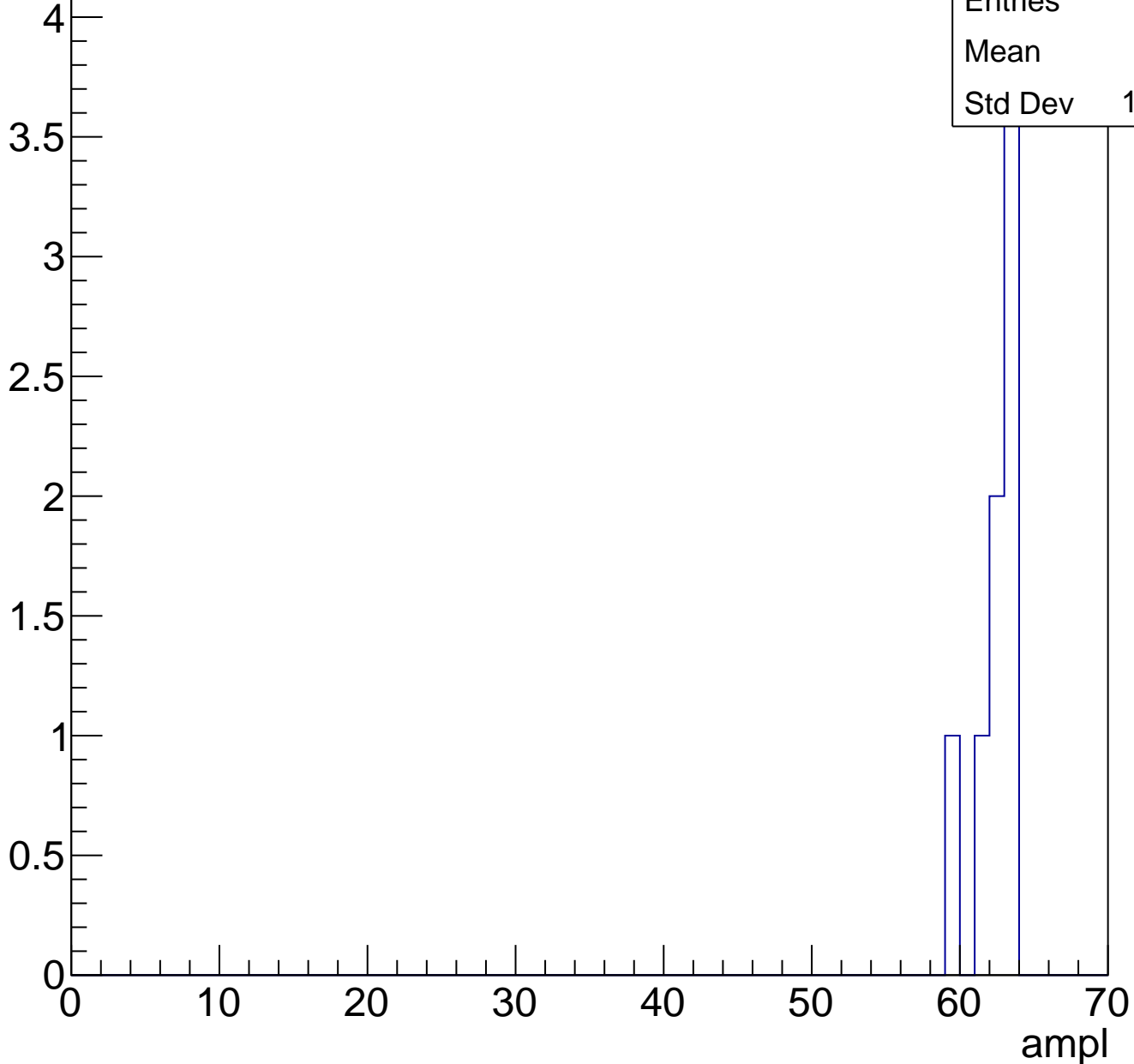
Entries	36
Mean	58.61
Std Dev	10.12



# B1L101S, U20-ch121, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U20-ch121, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L101S, U20-ch122, adc0

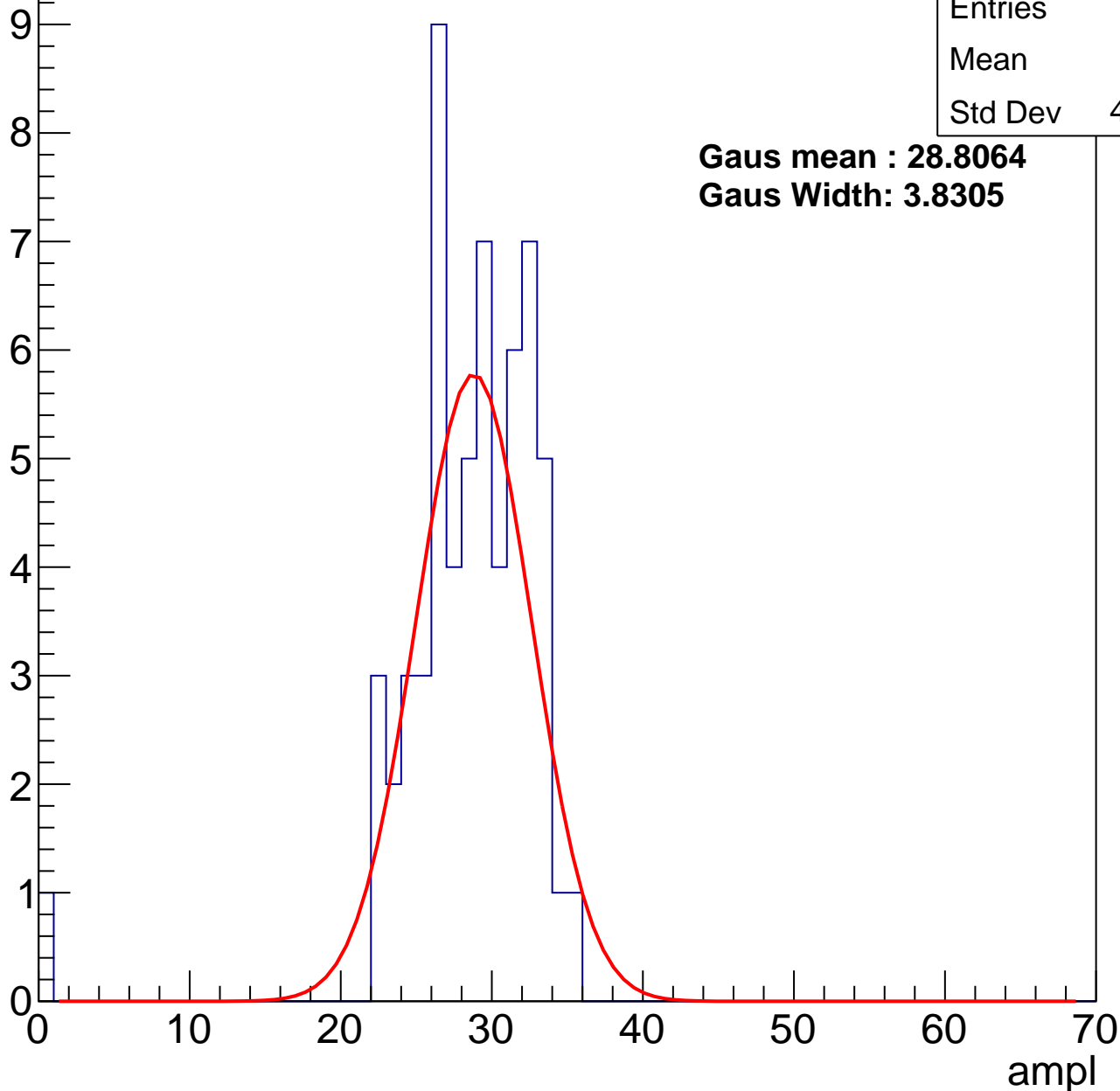
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	28
Std Dev	4.886

**Gaus mean : 28.8064**

**Gaus Width: 3.8305**



# B1L101S, U20-ch122, adc1

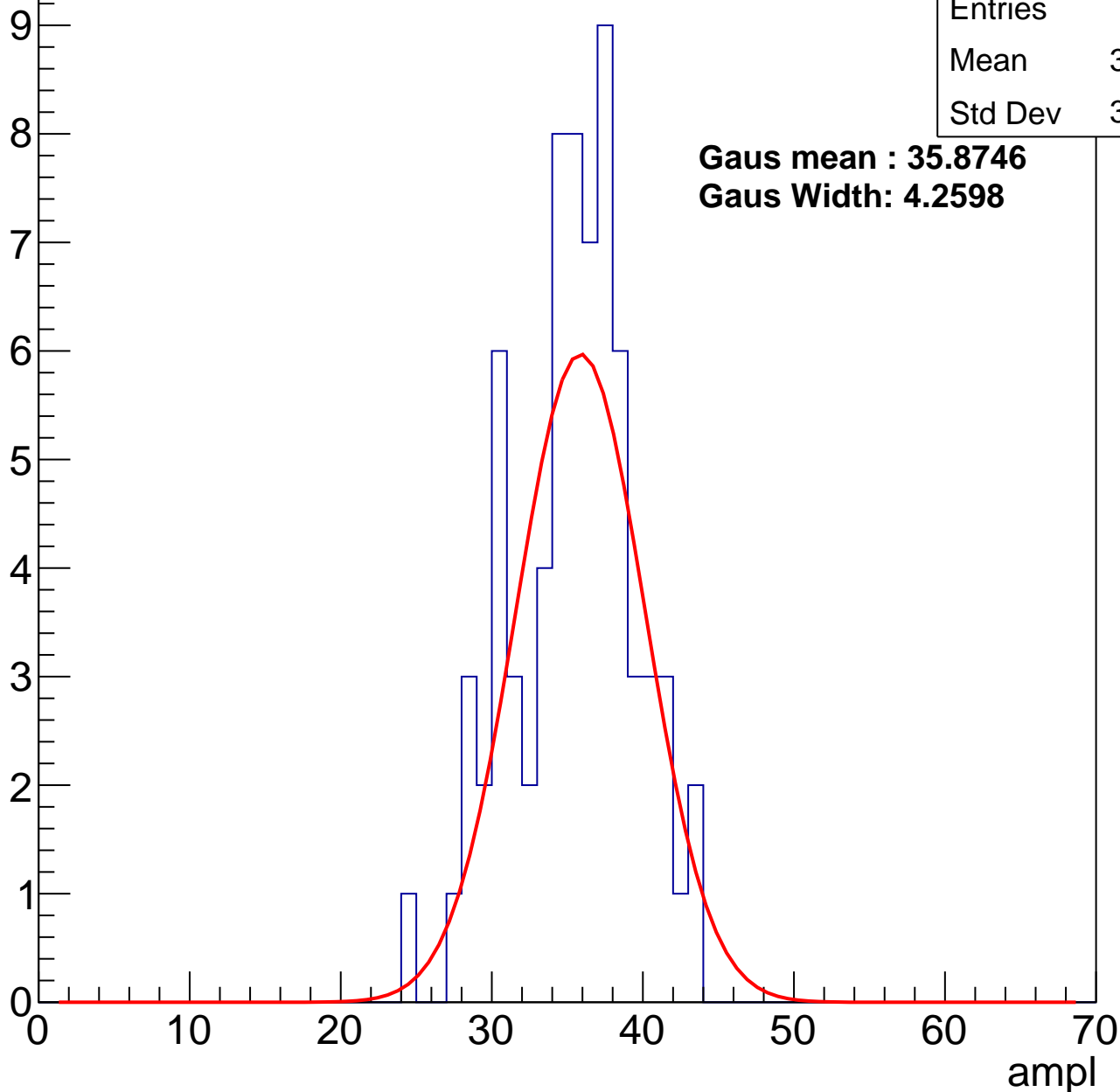
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	72
Mean	34.93
Std Dev	3.994

**Gaus mean : 35.8746**

**Gaus Width: 4.2598**

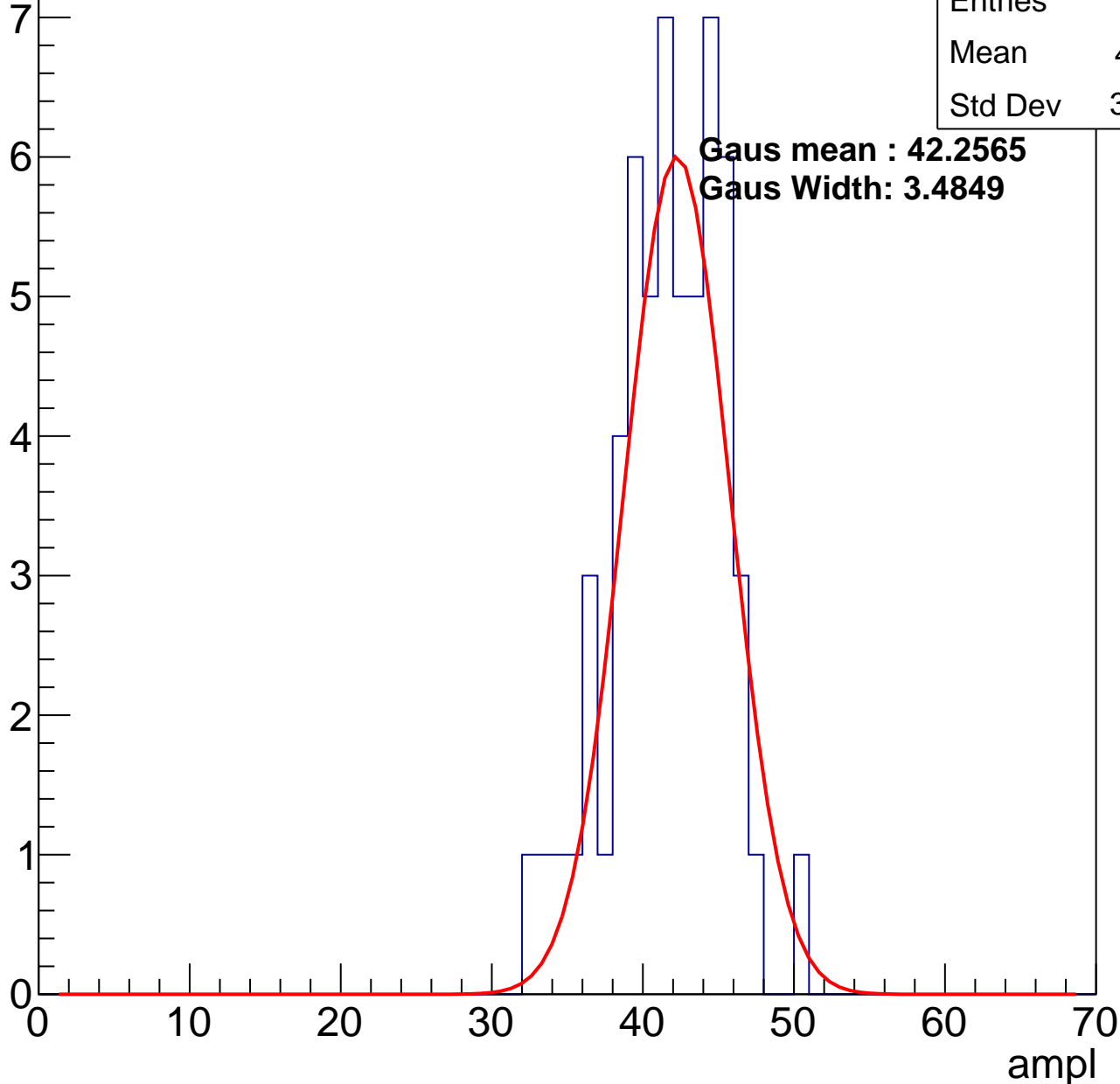


# B1L101S, U20-ch122, adc2

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	58
Mean	41.21
Std Dev	3.619

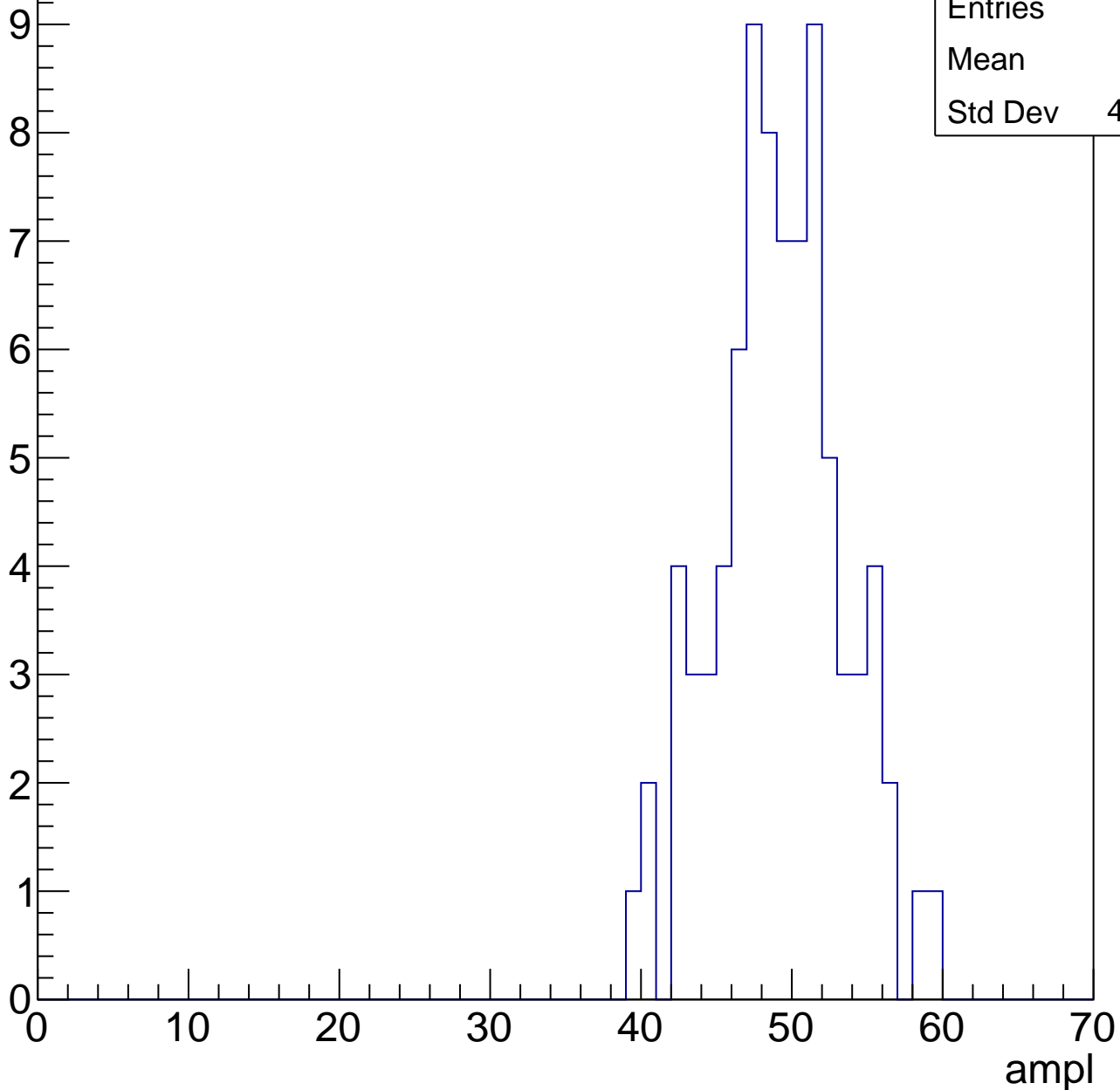


# B1L101S, U20-ch122, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	82
Mean	48.7
Std Dev	4.175

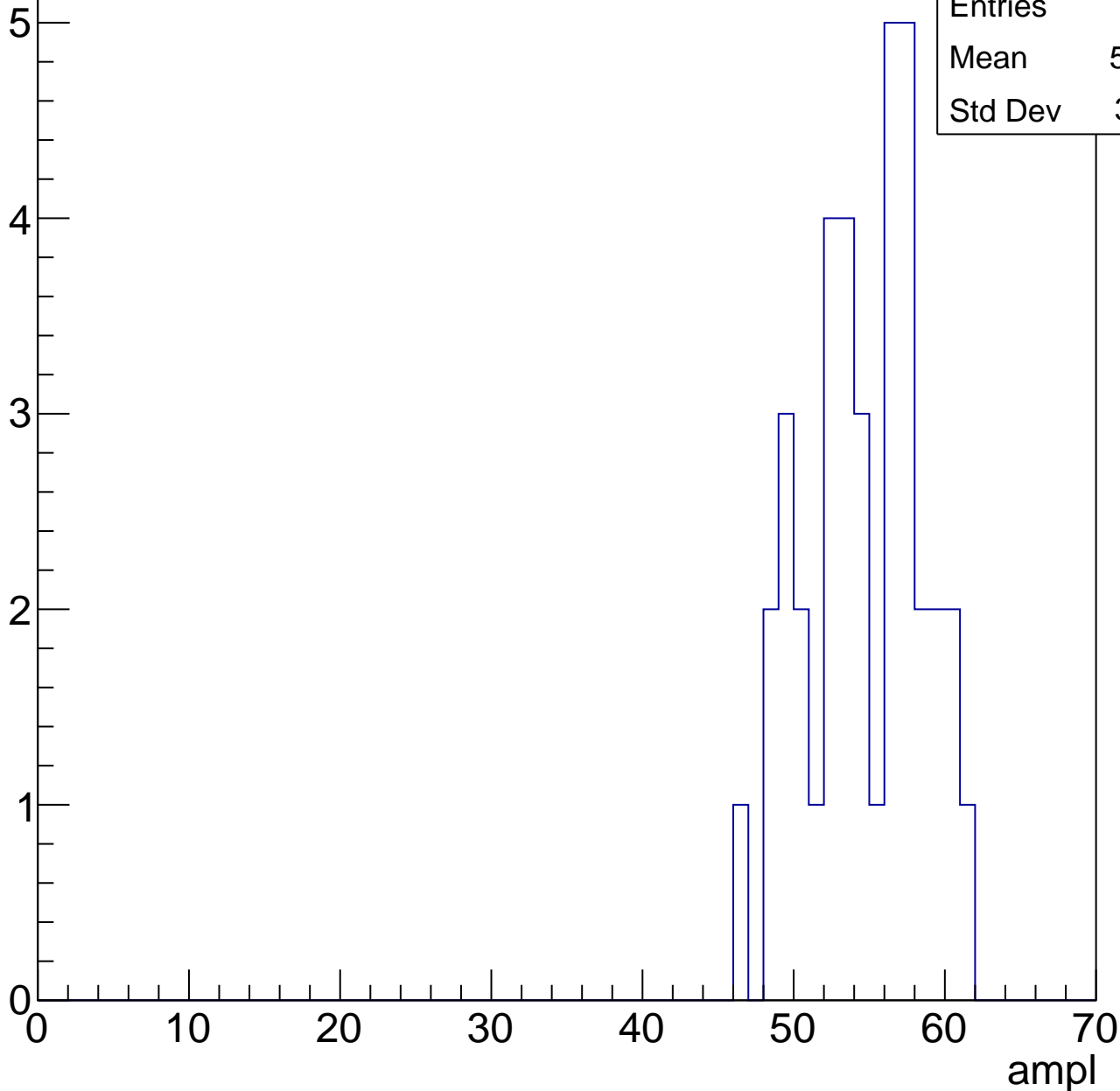


# B1L101S, U20-ch122, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	38
Mean	54.13
Std Dev	3.771

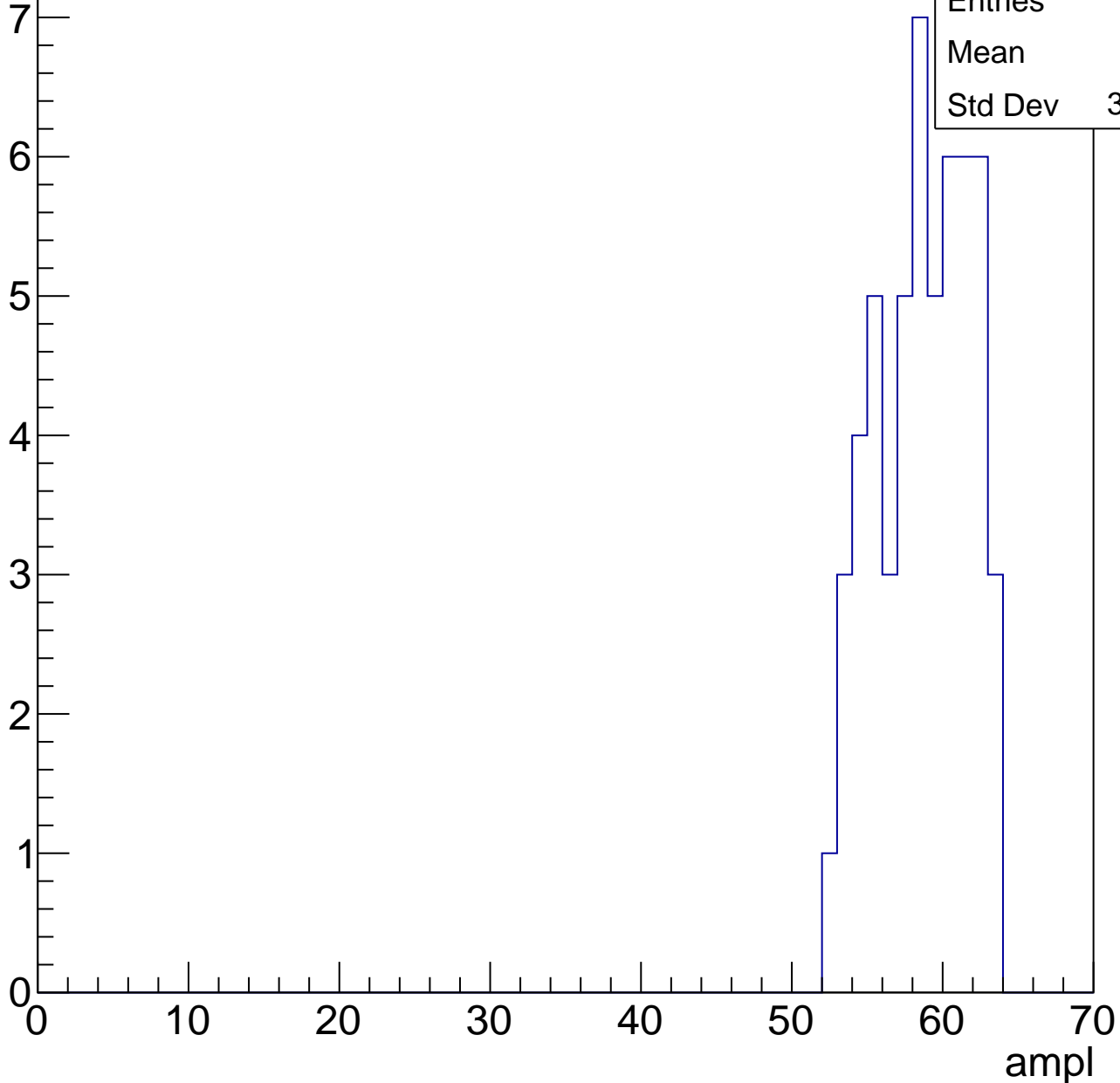


# B1L101S, U20-ch122, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	54
Mean	58.2
Std Dev	3.009

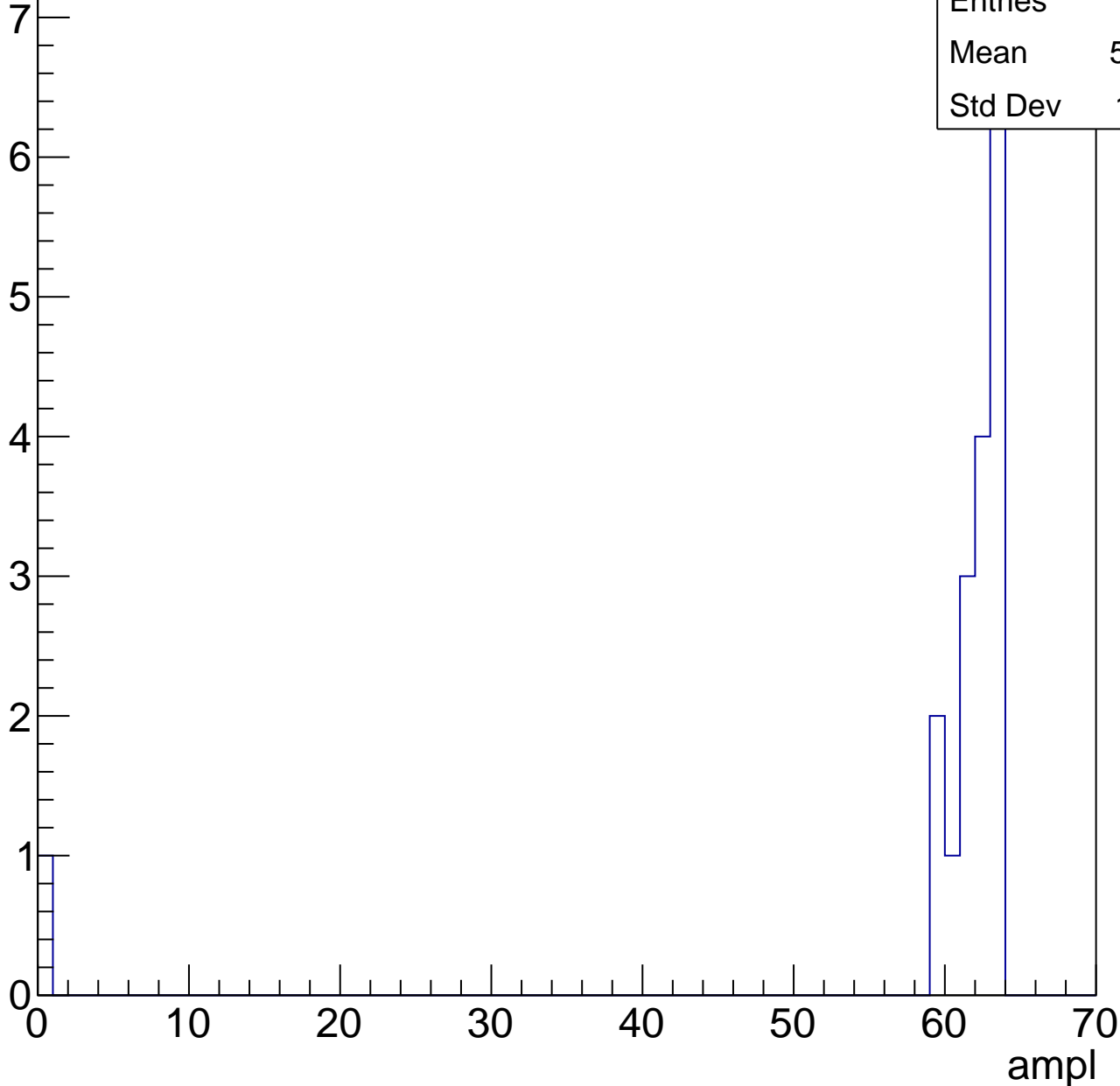


# B1L101S, U20-ch122, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	18
Mean	58.33
Std Dev	14.21





# B1L101S, U20-ch122, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U20-ch123, adc0

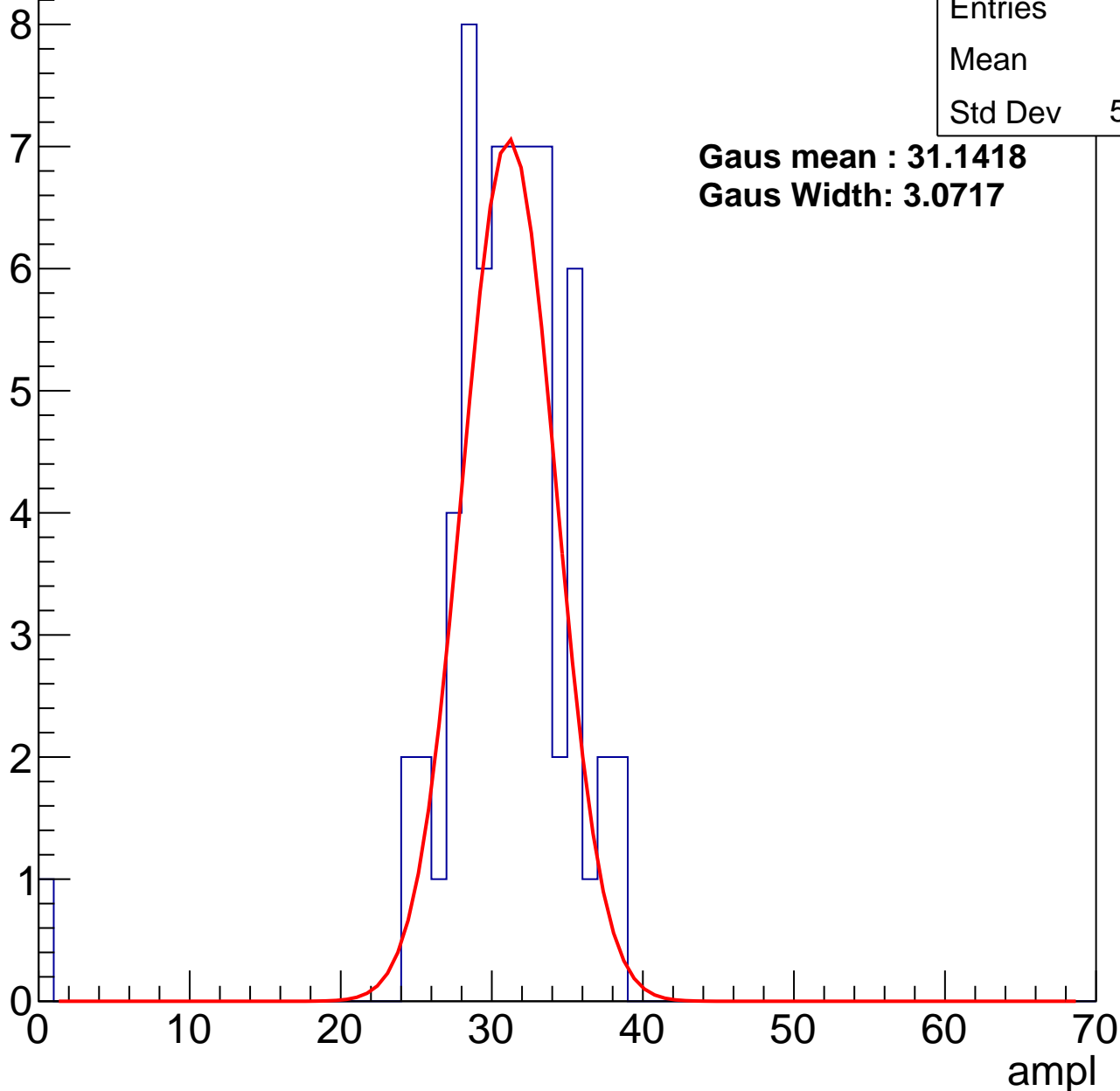
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	30.4
Std Dev	5.029

**Gaus mean : 31.1418**

**Gaus Width: 3.0717**



# B1L101S, U20-ch123, adc1

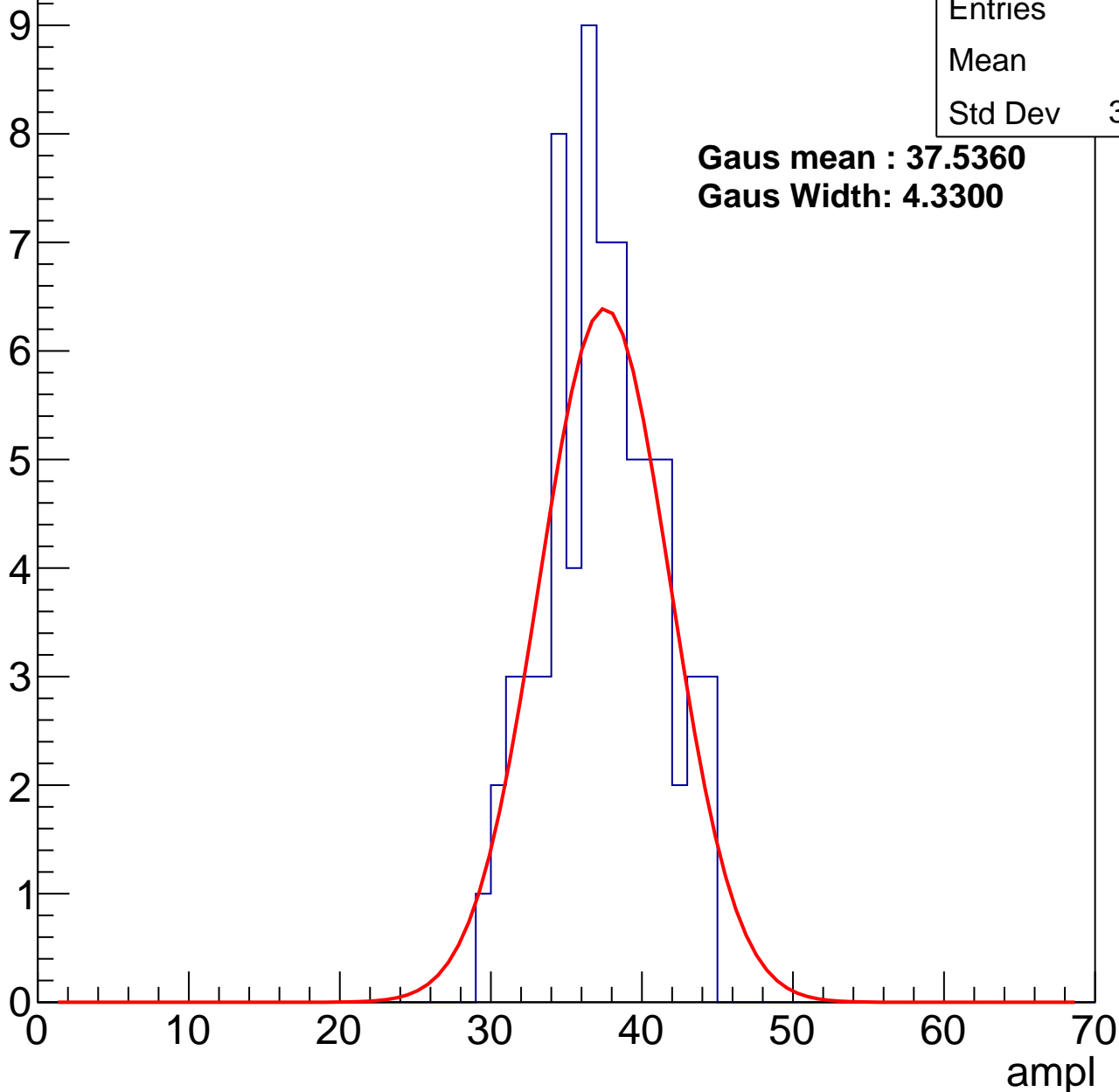
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	36.9
Std Dev	3.677

**Gaus mean : 37.5360**

**Gaus Width: 4.3300**



# B1L101S, U20-ch123, adc2

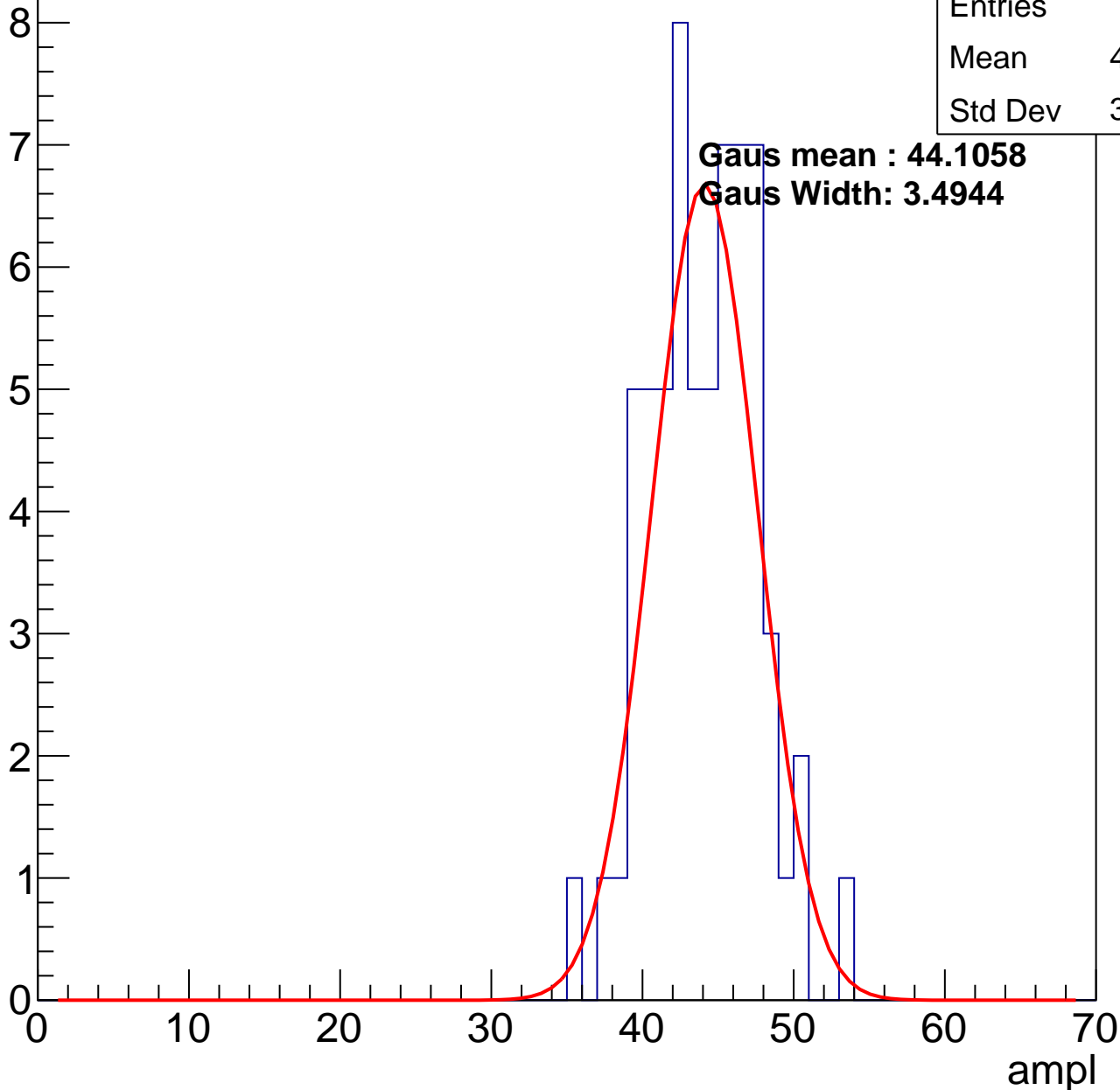
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	43.64
Std Dev	3.466

**Gaus mean : 44.1058**

**Gaus Width: 3.4944**

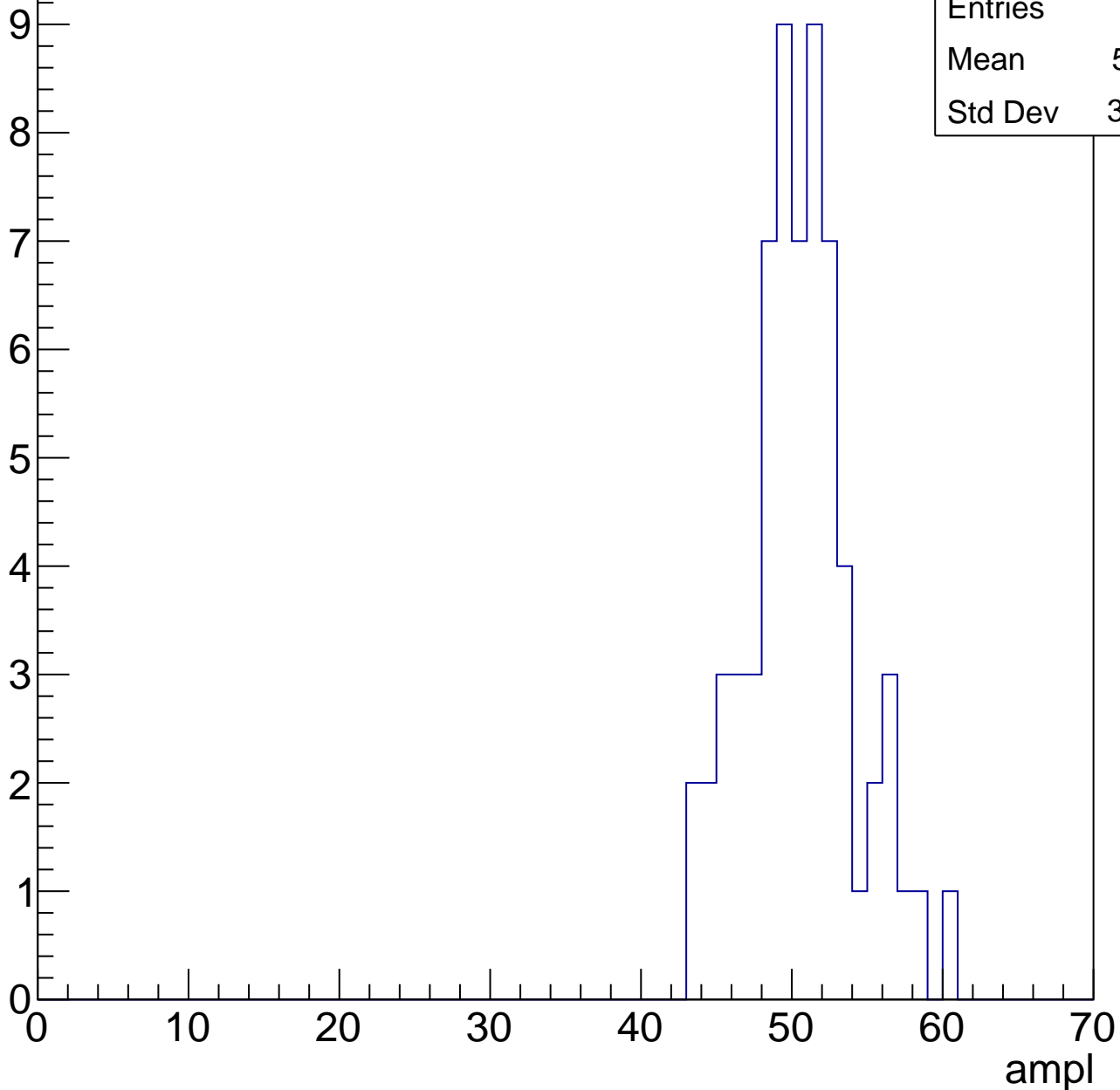


# B1L101S, U20-ch123, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	50.11
Std Dev	3.544

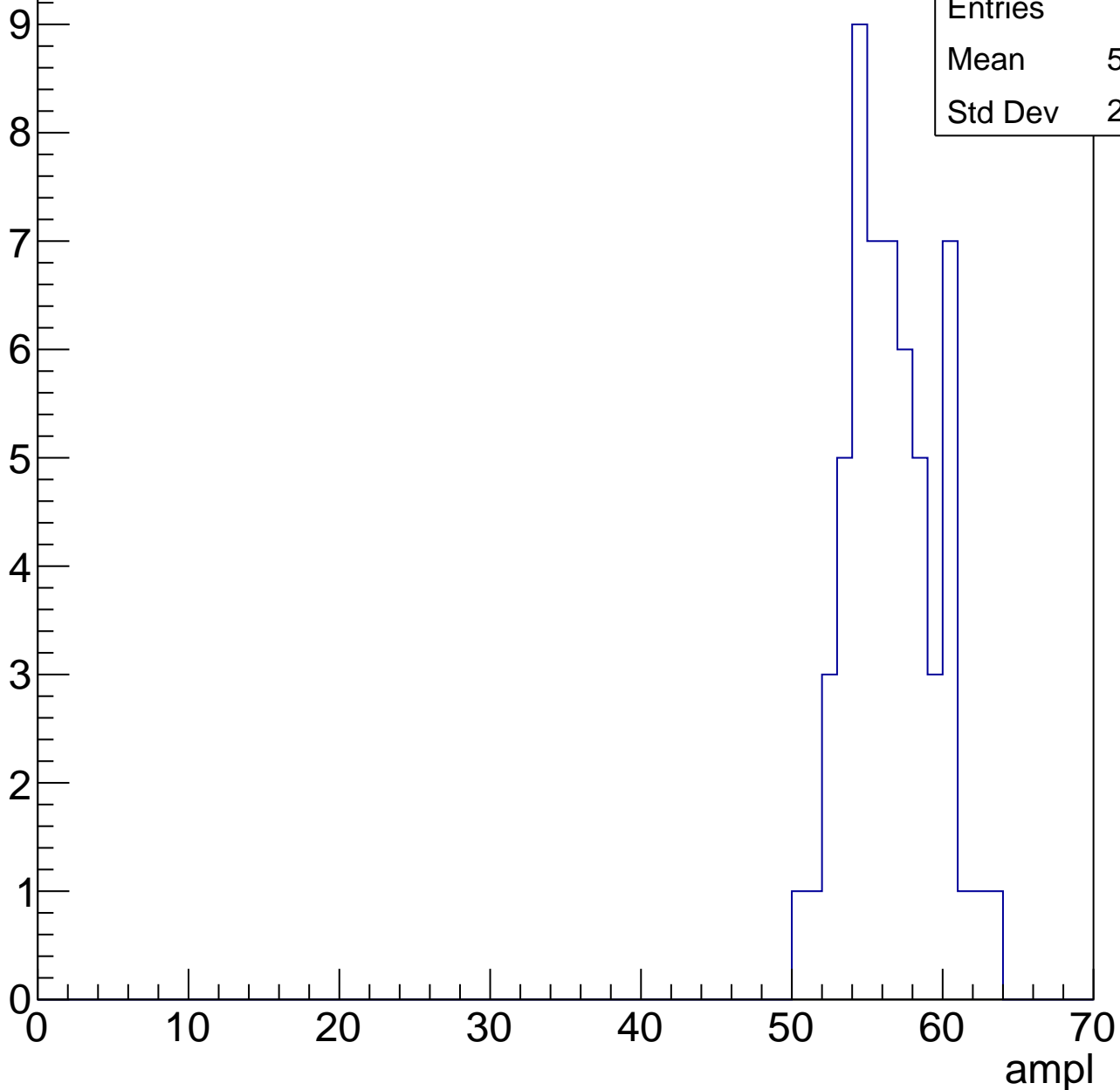


# B1L101S, U20-ch123, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	57
Mean	56.14
Std Dev	2.874

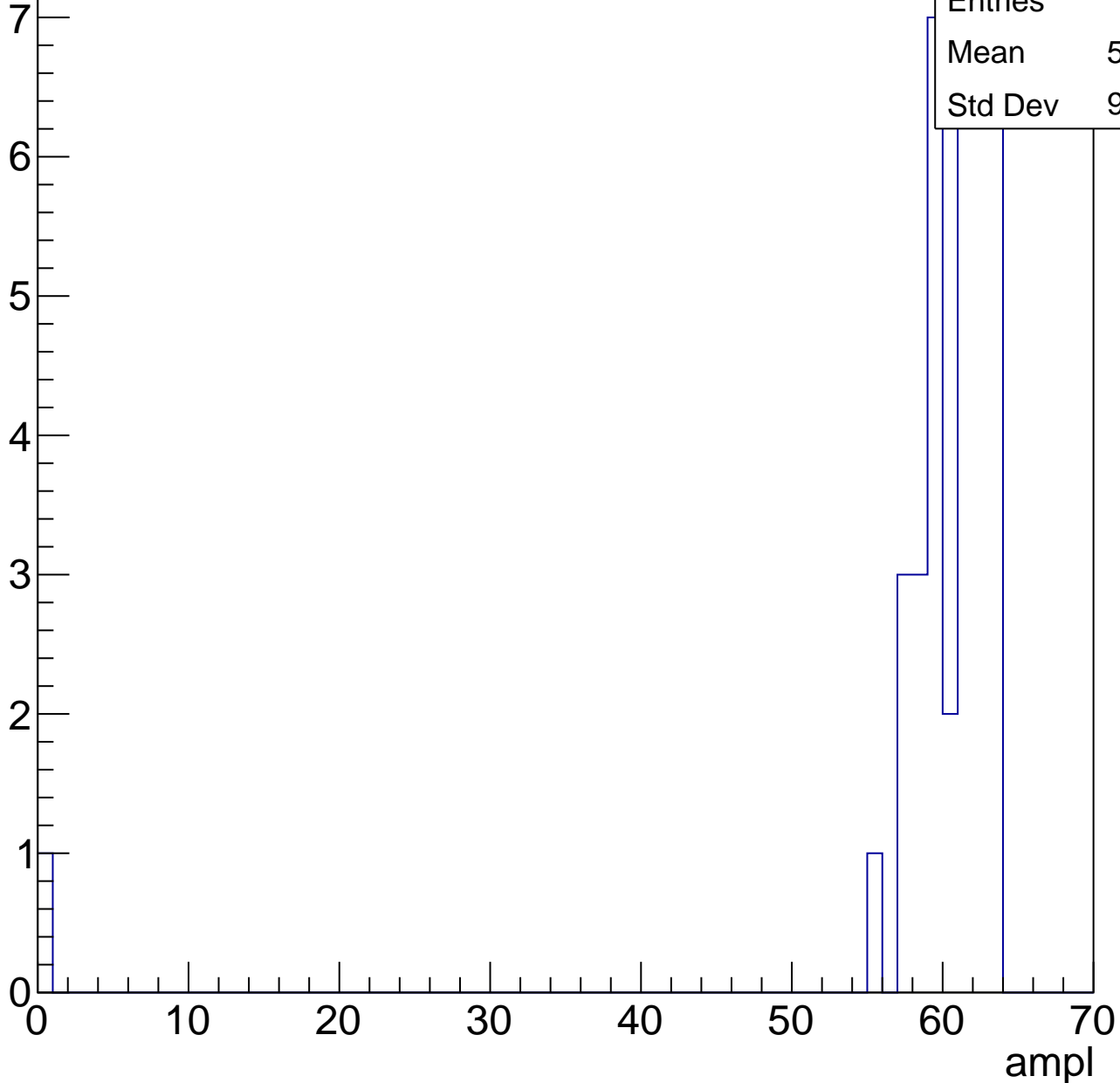


# B1L101S, U20-ch123, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	38
Mean	58.82
Std Dev	9.888



# B1L101S, U20-ch123, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

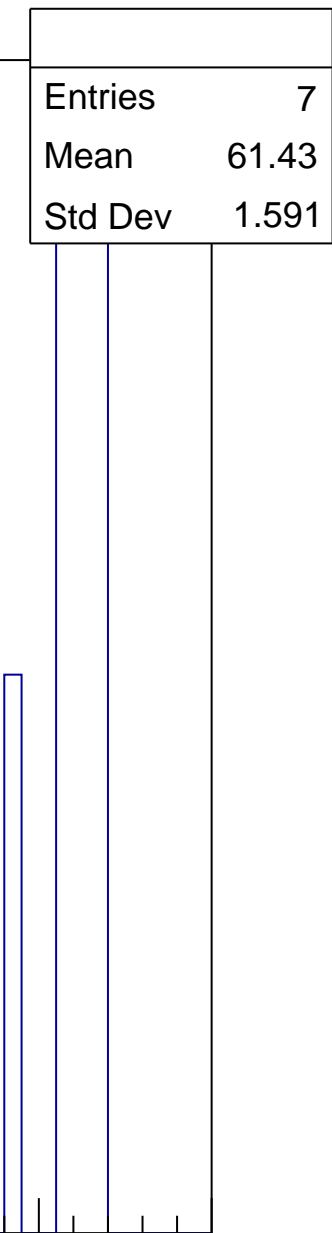
Entry

2  
1.8  
1.6  
1.4  
1.2  
1.0  
0.8  
0.6  
0.4  
0.2  
0

Entries	7
Mean	61.43
Std Dev	1.591

0 10 20 30 40 50 60 70

ampl

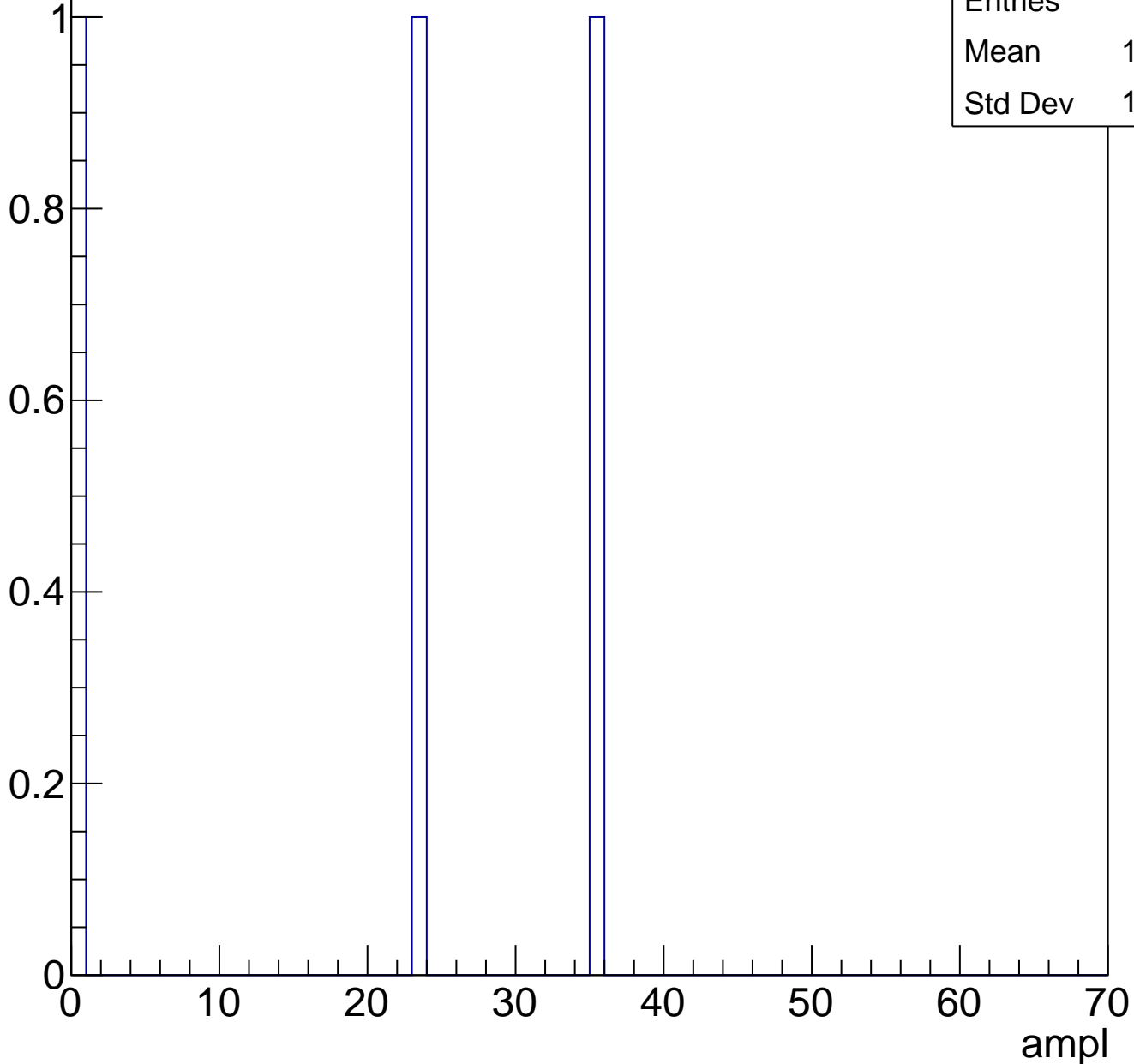




# B1L101S, U20-ch123, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	3
Mean	19.33
Std Dev	14.52

# B1L101S, U20-ch124, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	74
Mean	29.46
Std Dev	3.414

**Gaus mean : 29.3919**

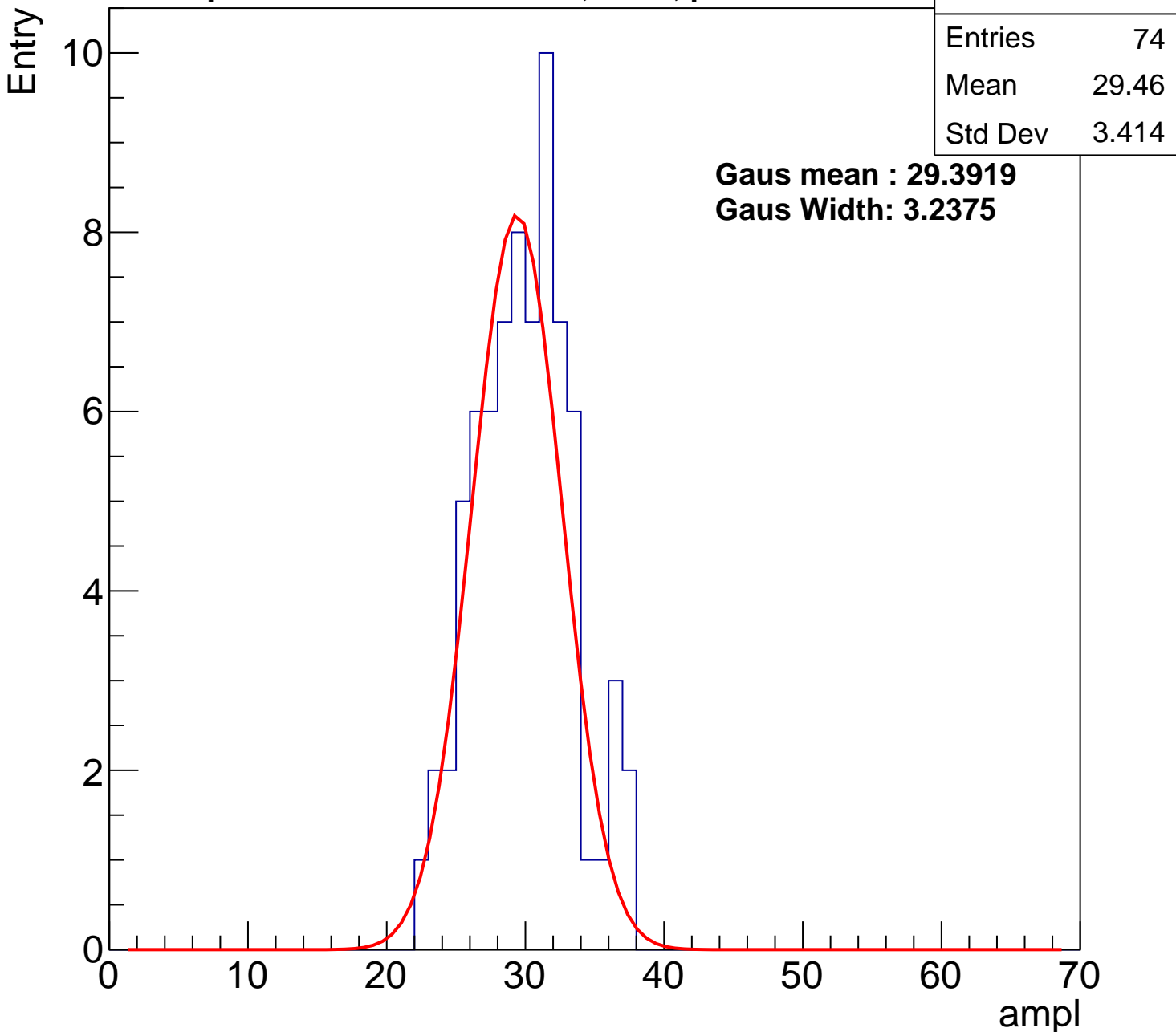
**Gaus Width: 3.2375**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U20-ch124, adc1

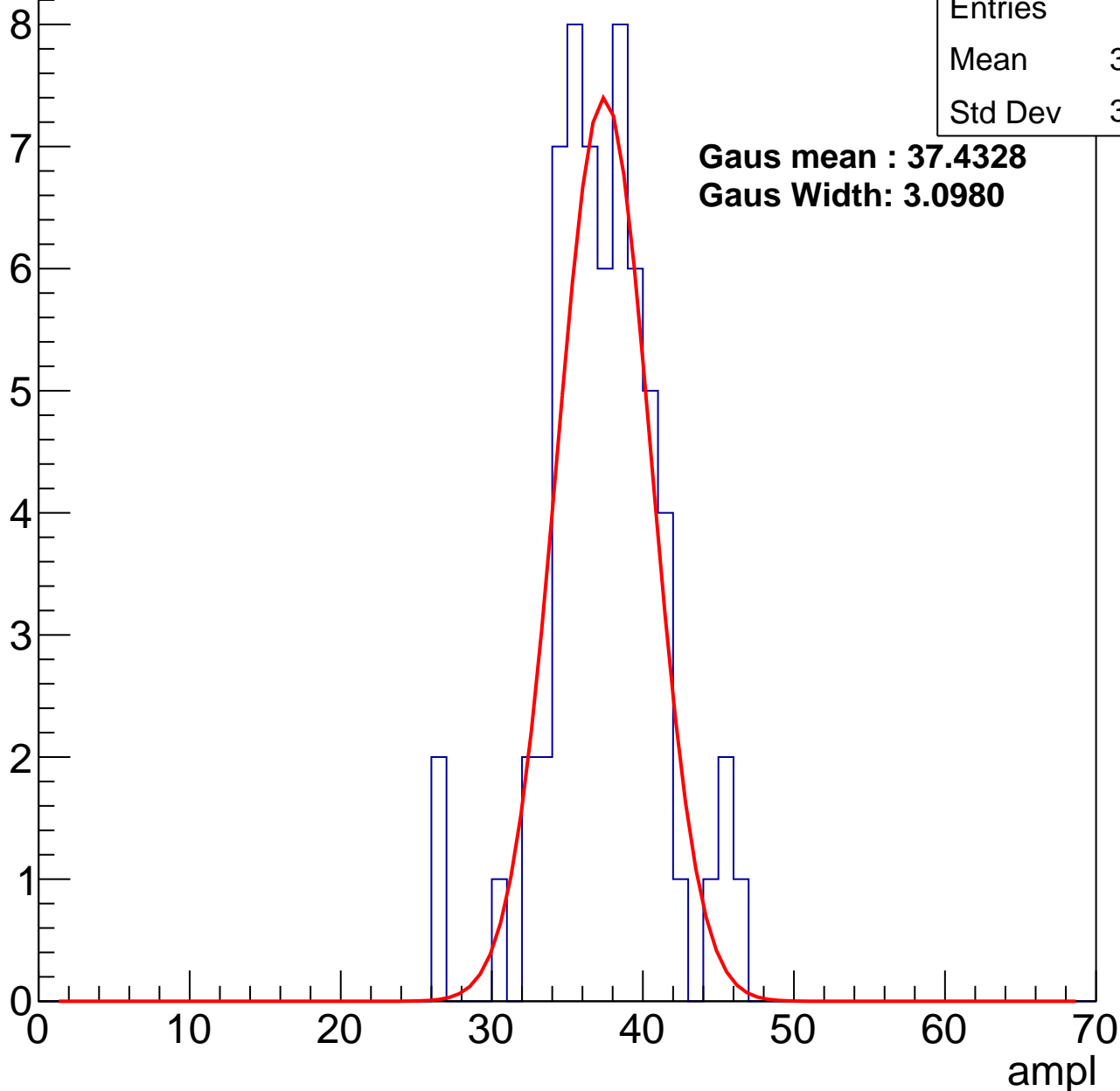
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	36.95
Std Dev	3.777

**Gaus mean : 37.4328**

**Gaus Width: 3.0980**



# B1L101S, U20-ch124, adc2

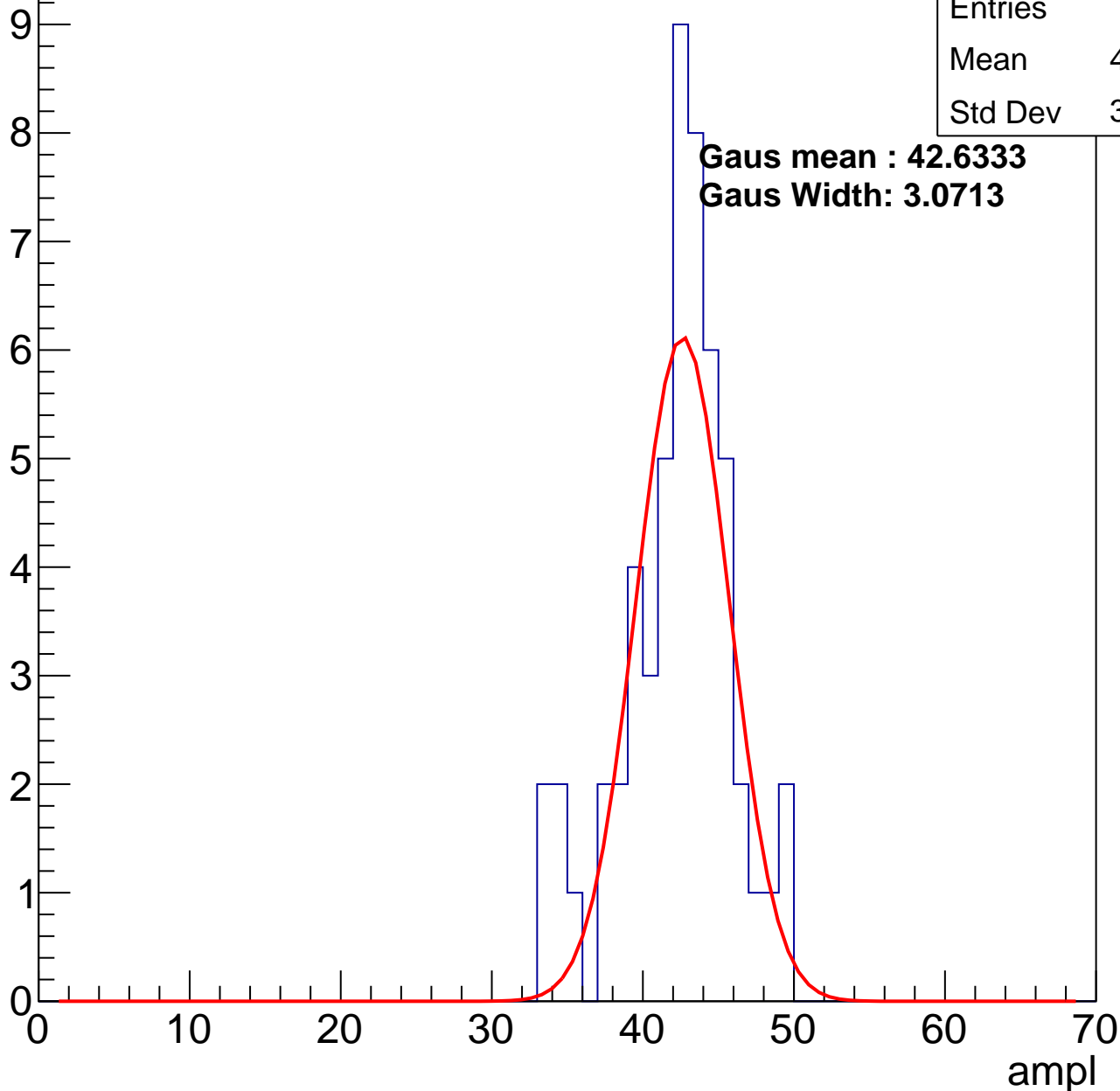
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	55
Mean	41.75
Std Dev	3.664

**Gaus mean : 42.6333**

**Gaus Width: 3.0713**

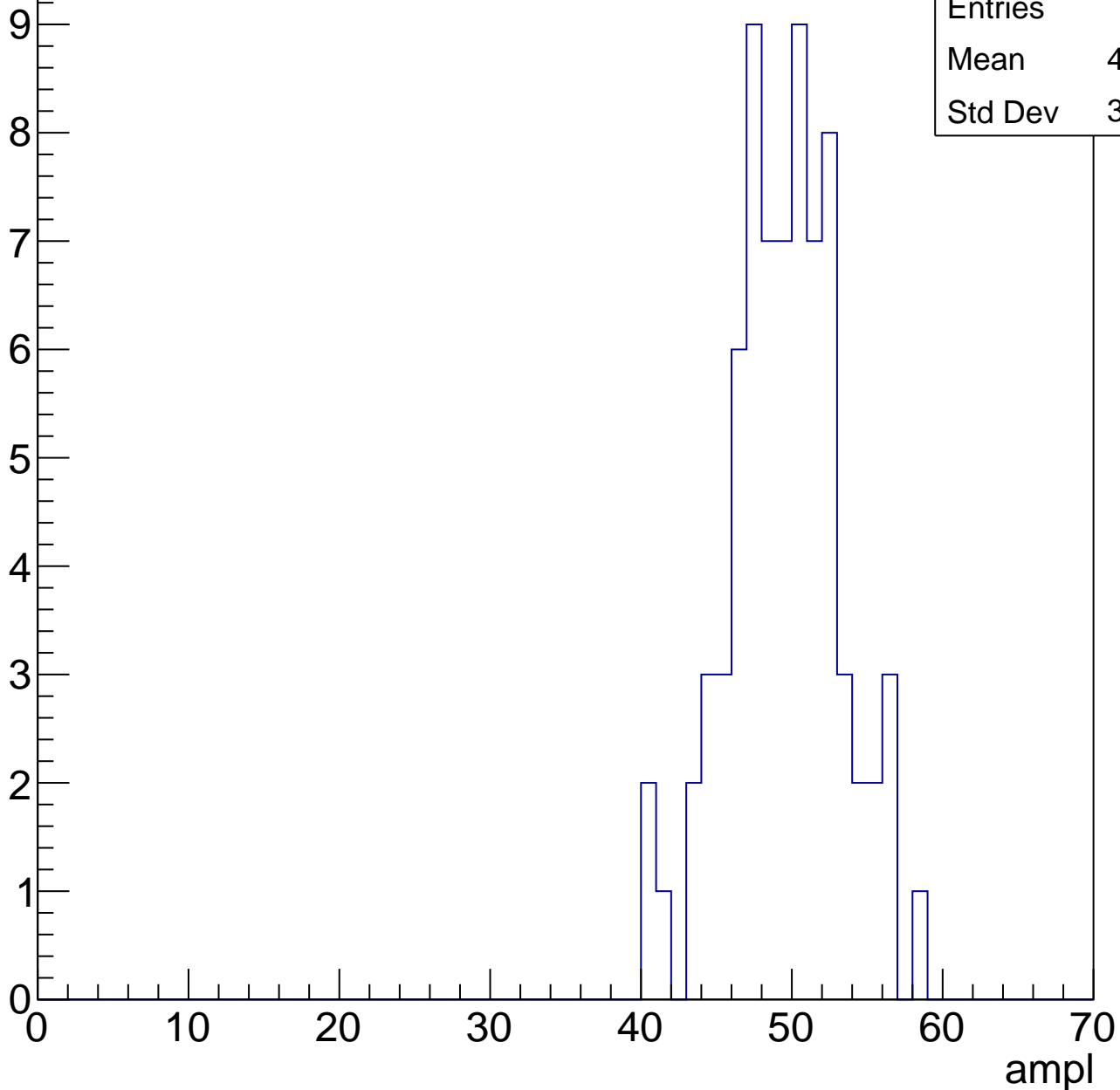


# B1L101S, U20-ch124, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	75
Mean	49.04
Std Dev	3.697

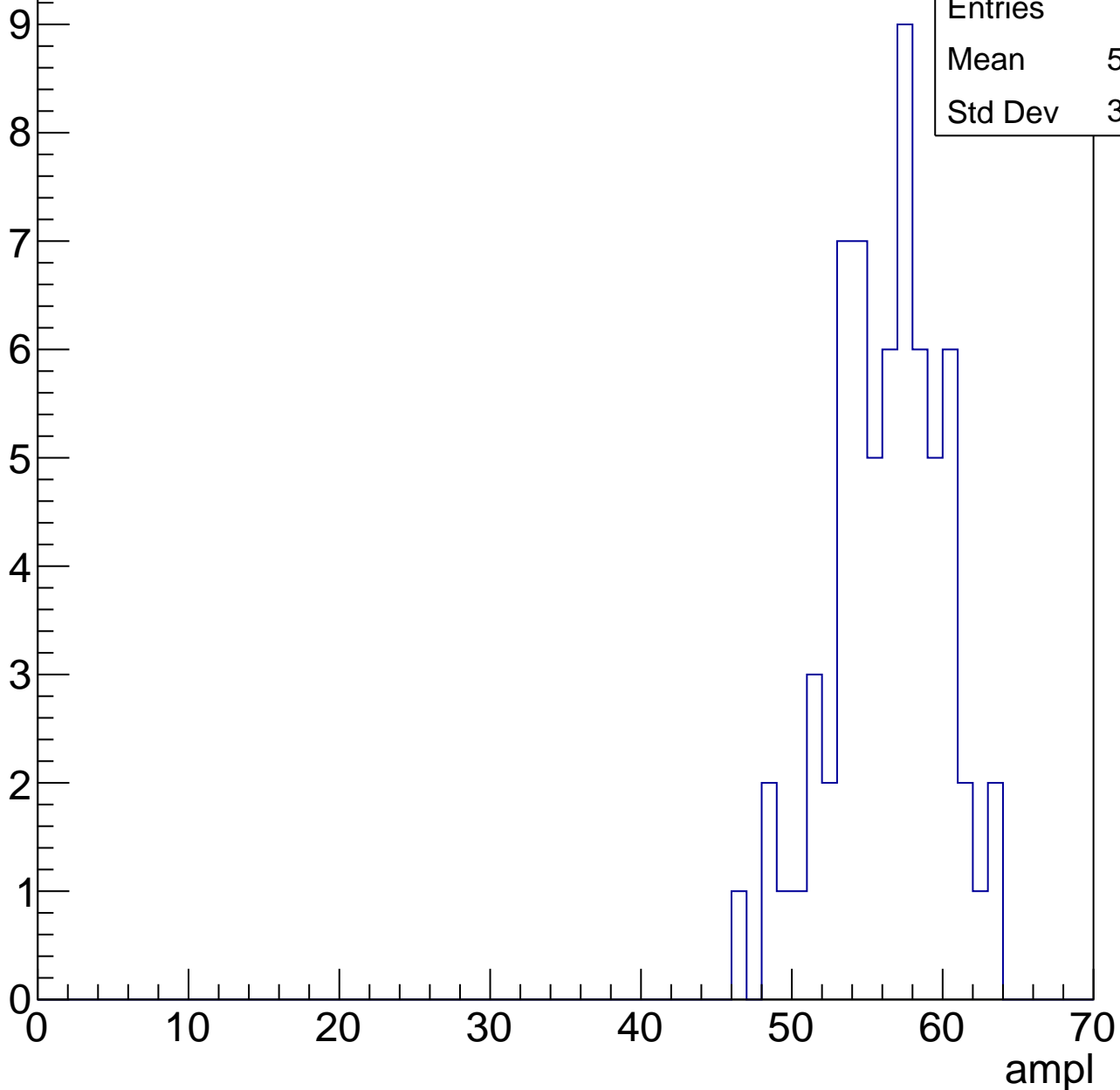


# B1L101S, U20-ch124, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	66
Mean	55.82
Std Dev	3.634

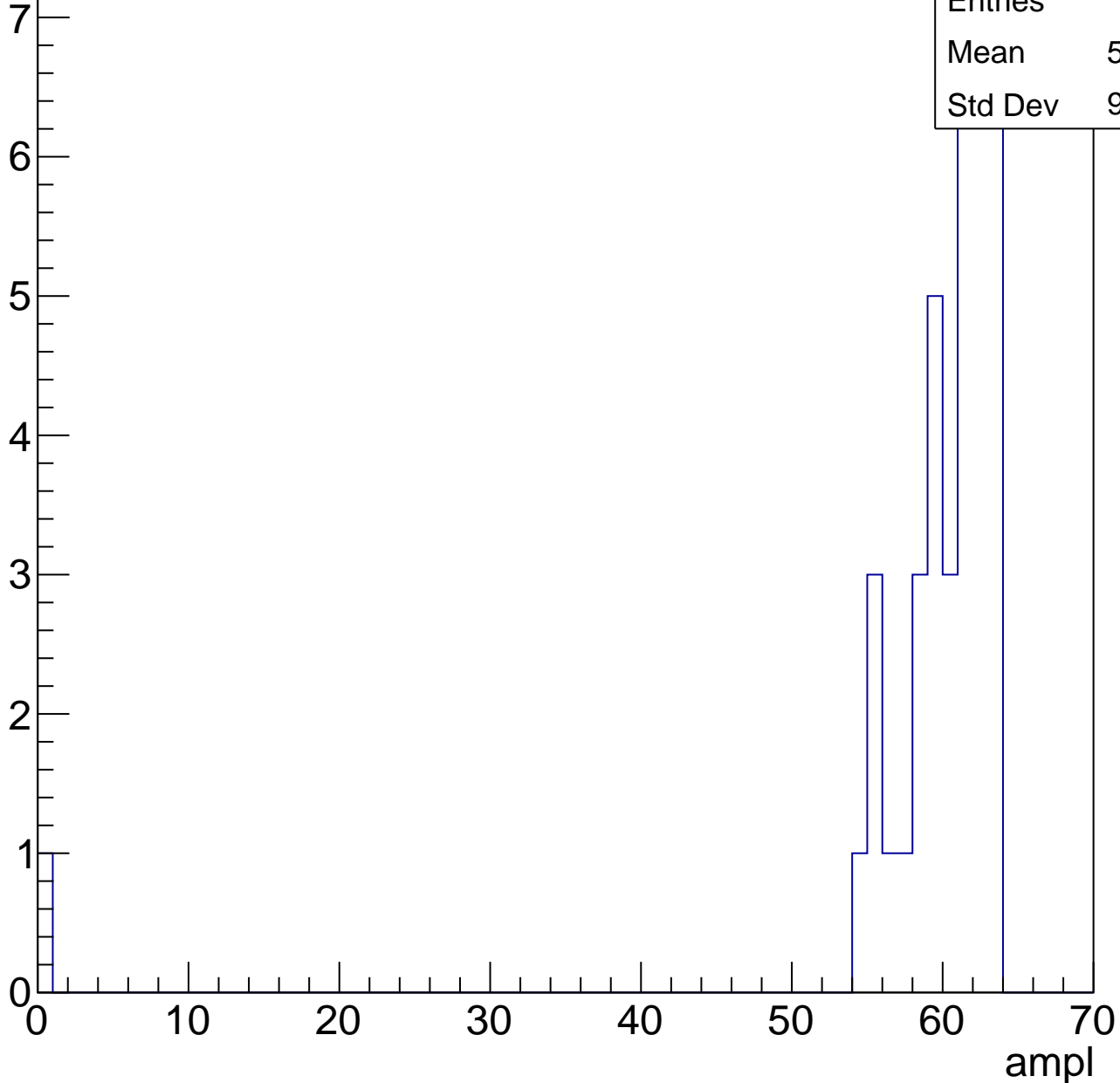


# B1L101S, U20-ch124, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	39
Mean	58.54
Std Dev	9.829



# B1L101S, U20-ch124, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

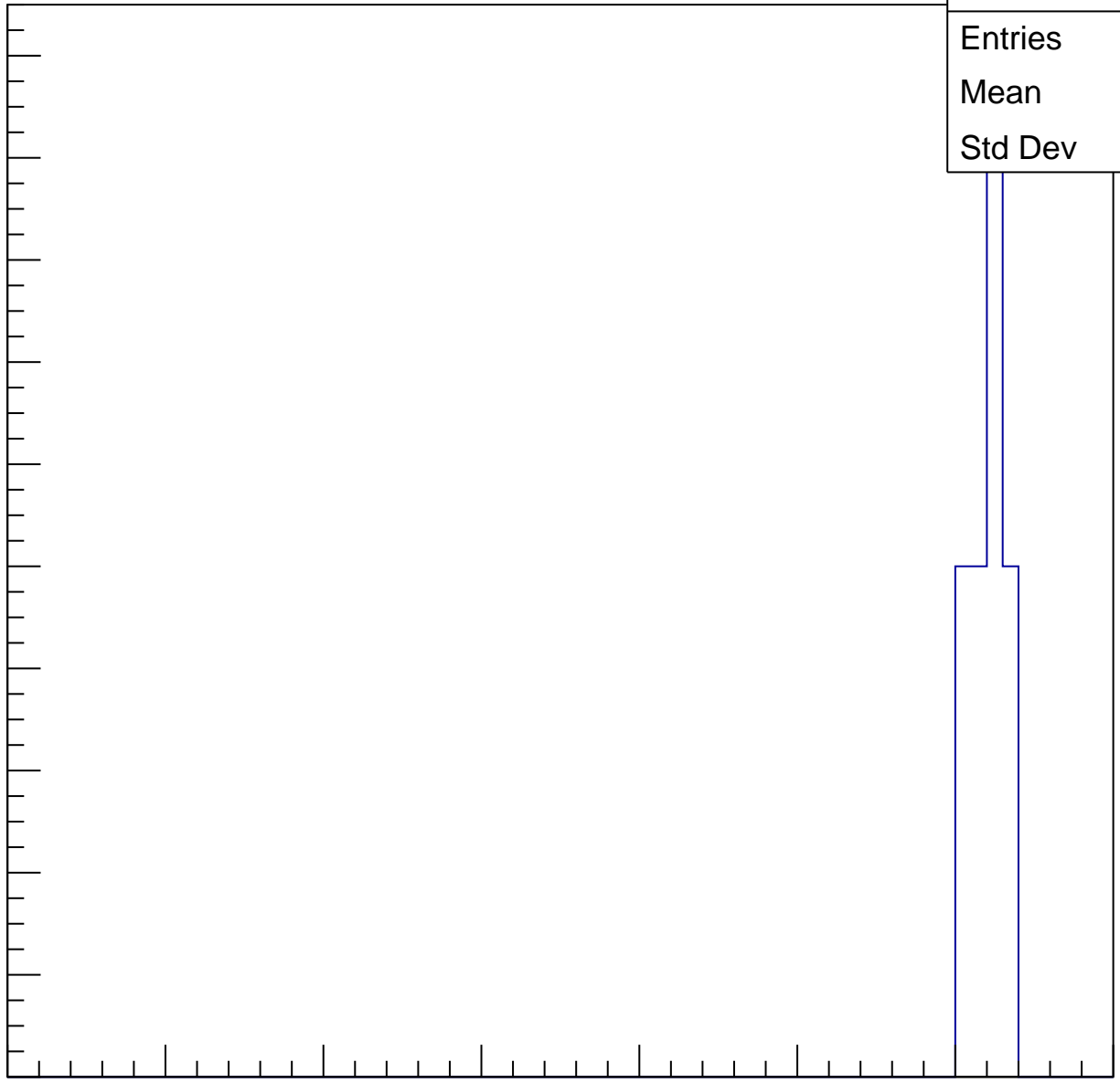
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	5
Mean	61.6
Std Dev	1.02

ampl

0 10 20 30 40 50 60 70





# B1L101S, U20-ch124, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U20-ch125, adc0

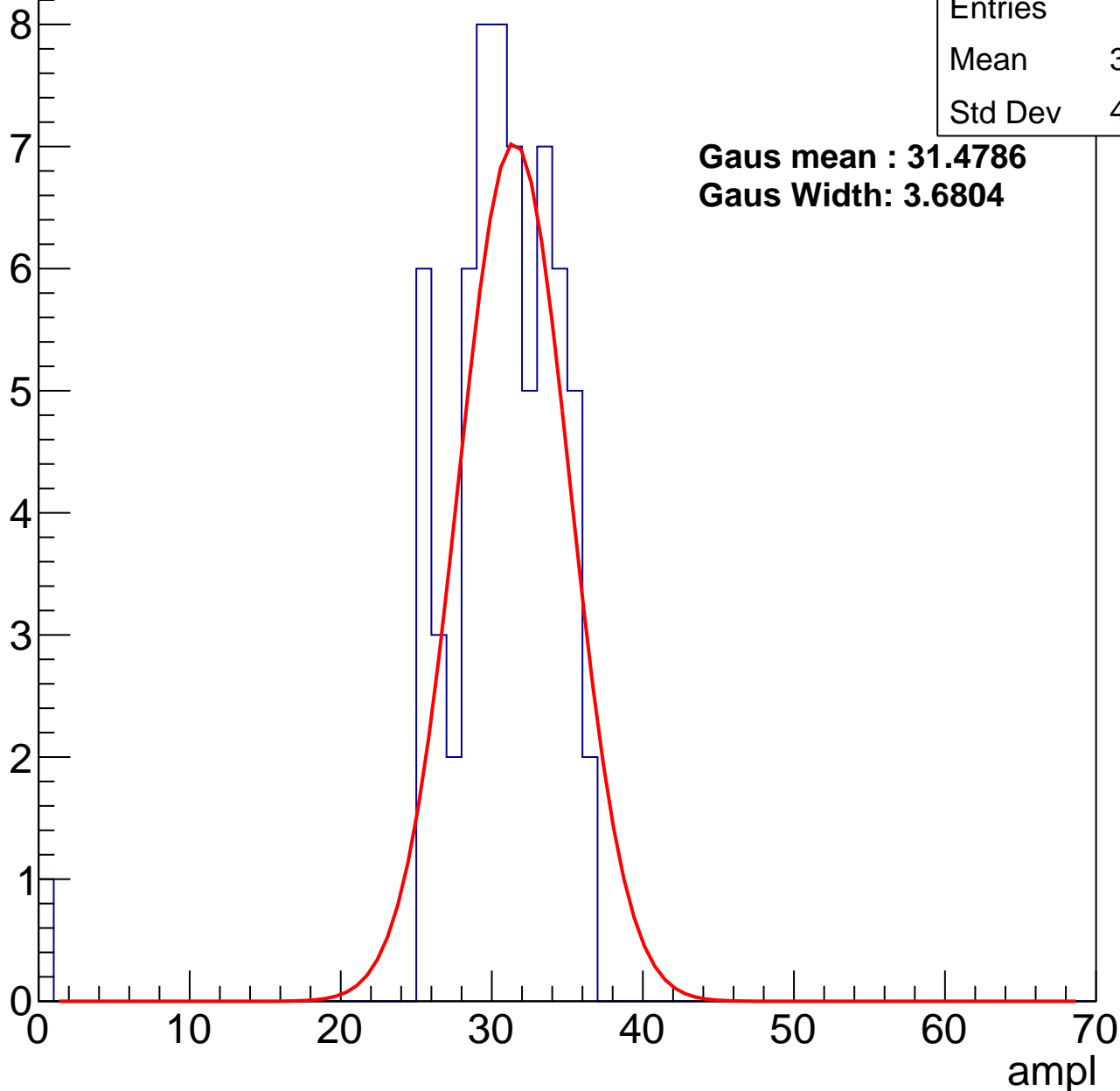
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	66
Mean	30.02
Std Dev	4.816

**Gaus mean : 31.4786**

**Gaus Width: 3.6804**



# B1L101S, U20-ch125, adc1

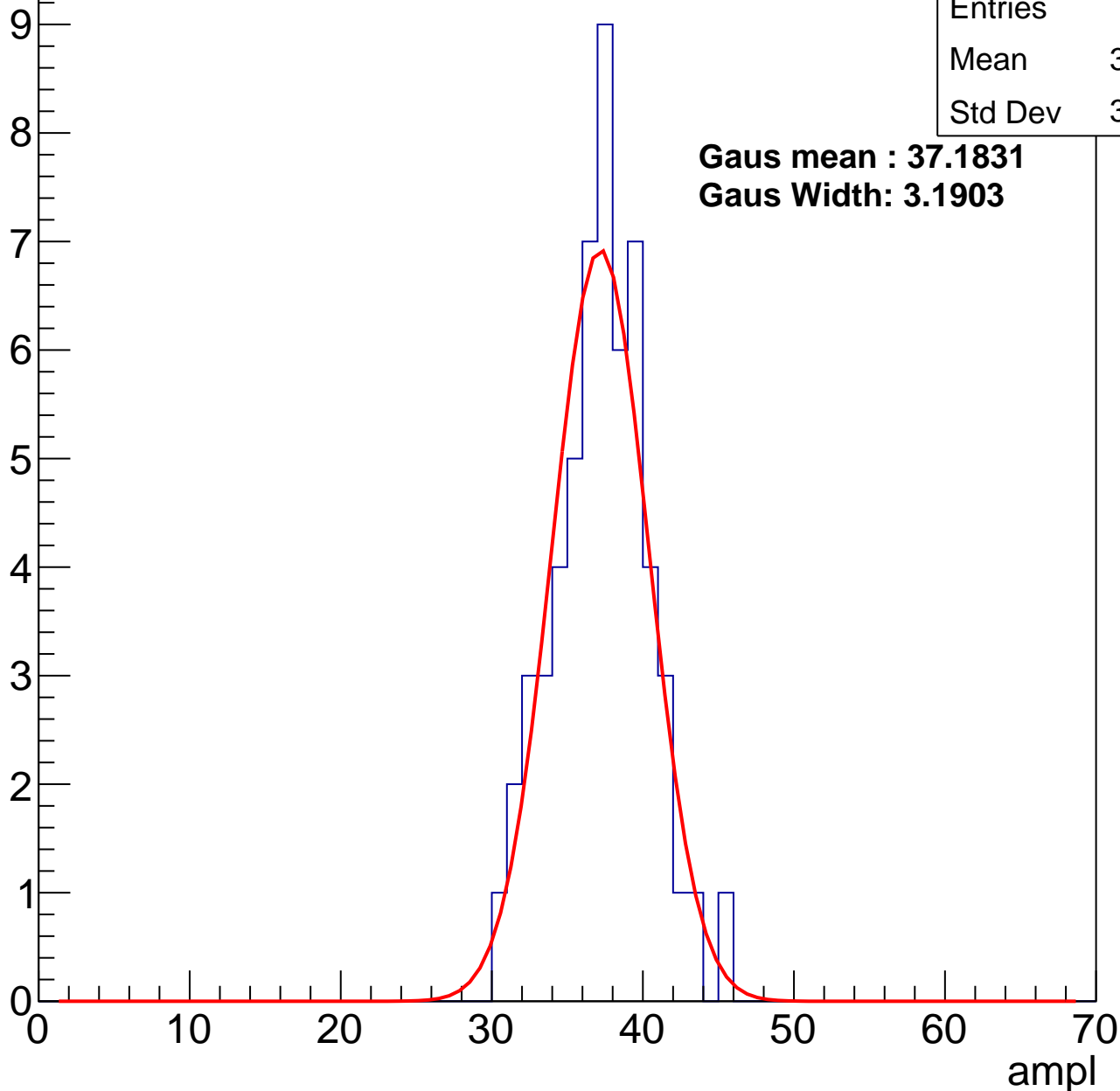
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	57
Mean	36.79
Std Dev	3.099

**Gaus mean : 37.1831**

**Gaus Width: 3.1903**



# B1L101S, U20-ch125, adc2

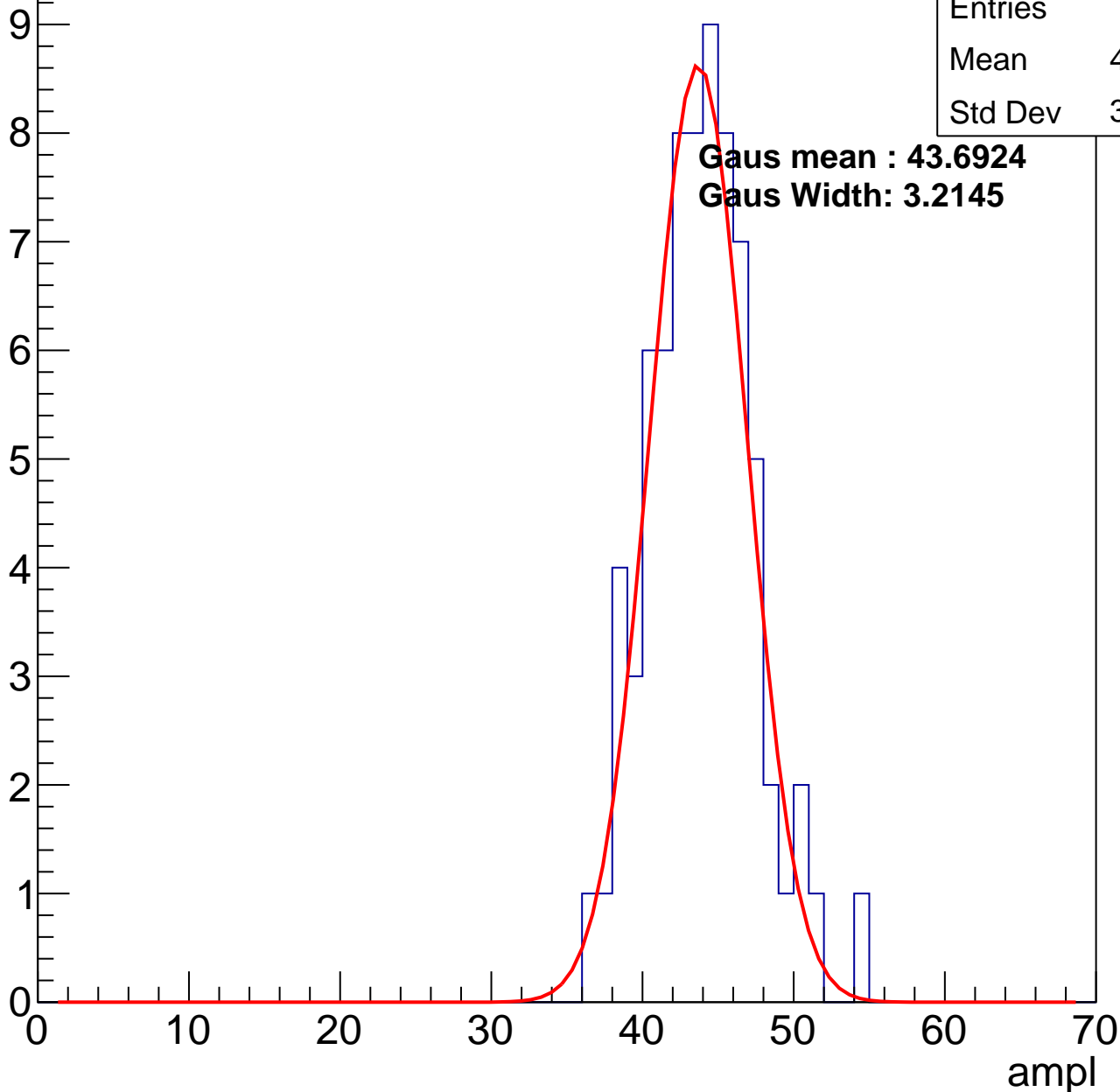
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	73
Mean	43.44
Std Dev	3.428

**Gaus mean : 43.6924**

**Gaus Width: 3.2145**

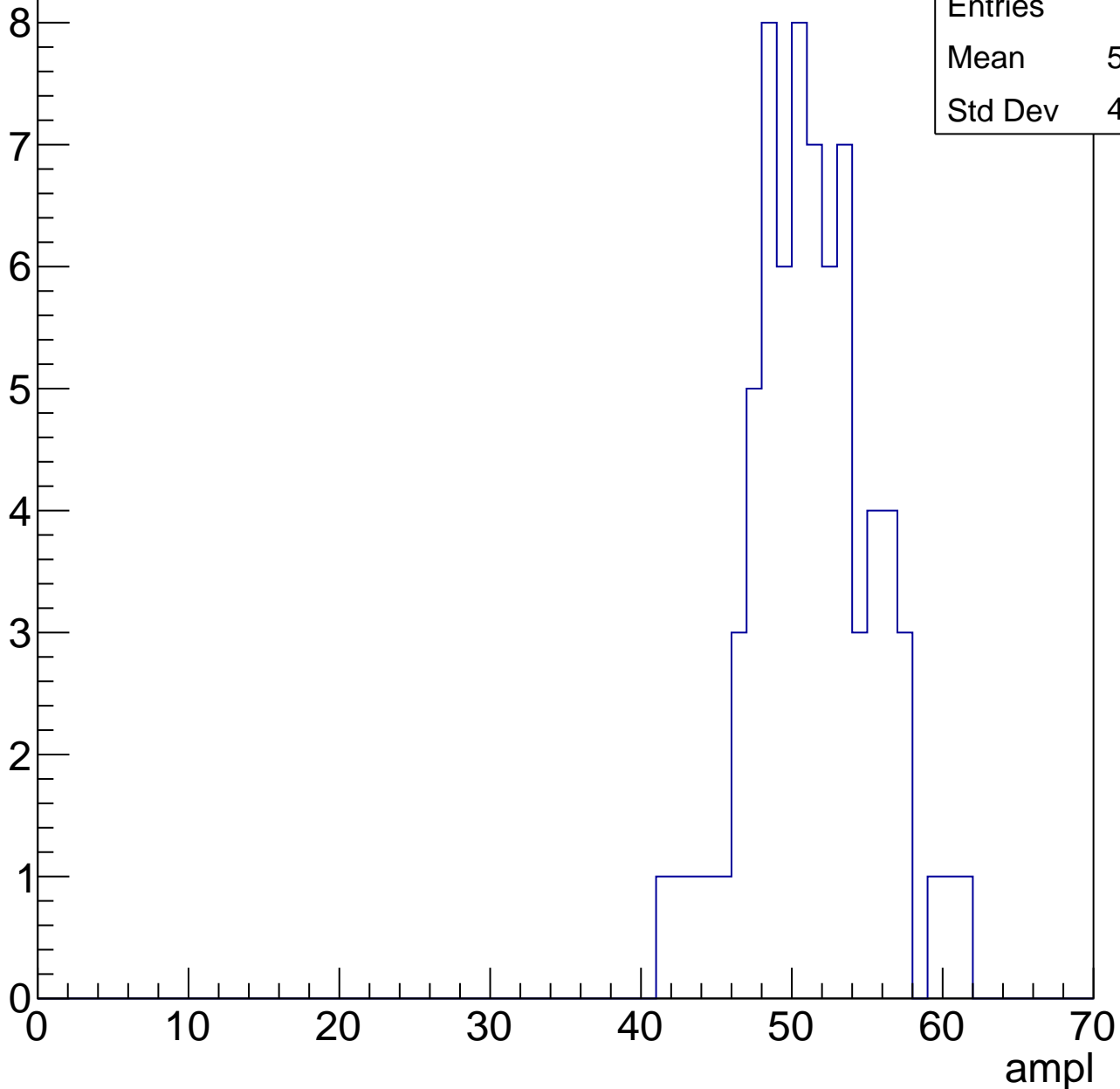


# B1L101S, U20-ch125, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	72
Mean	50.88
Std Dev	4.024

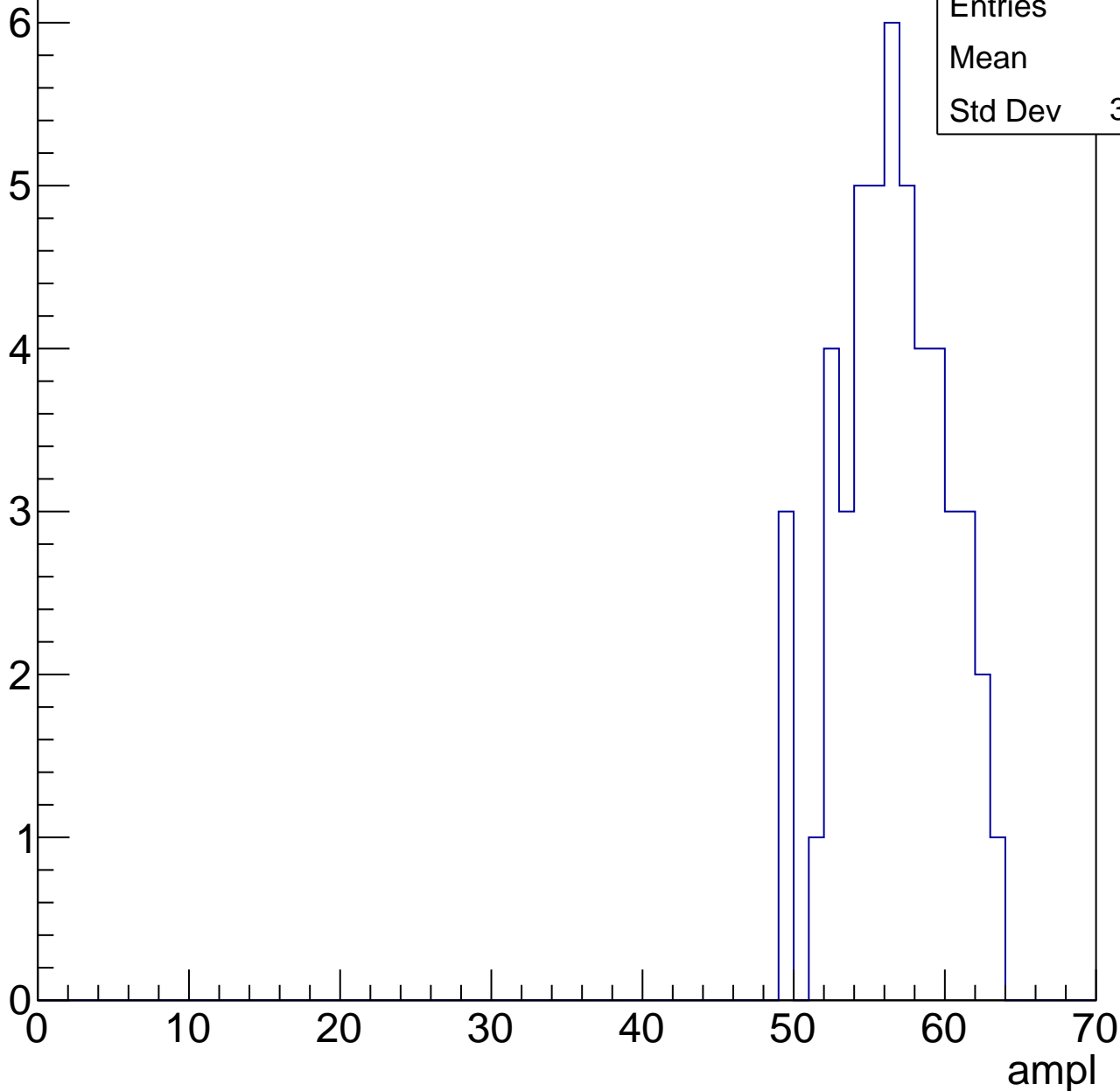


# B1L101S, U20-ch125, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	49
Mean	56.1
Std Dev	3.466

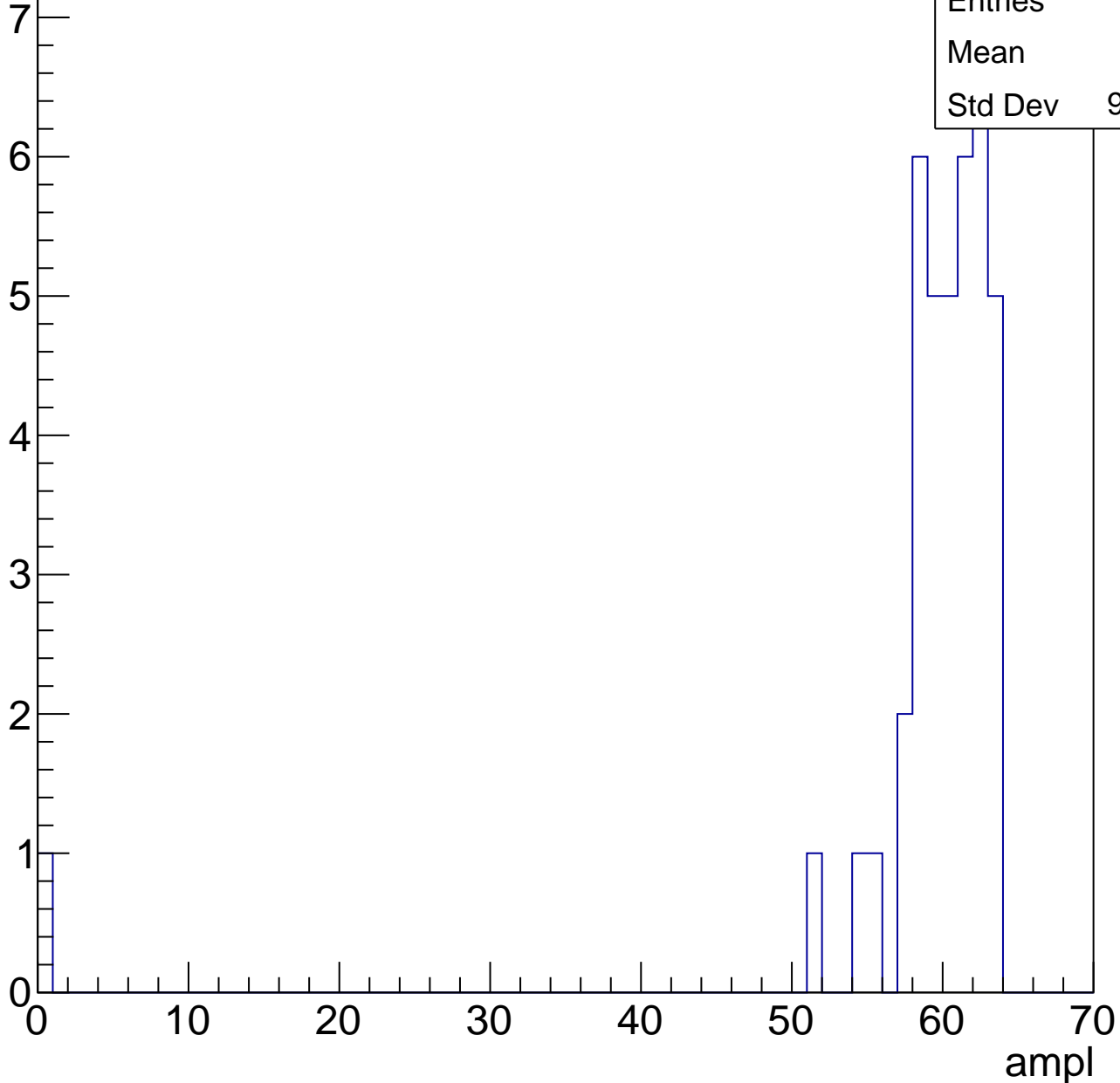


# B1L101S, U20-ch125, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

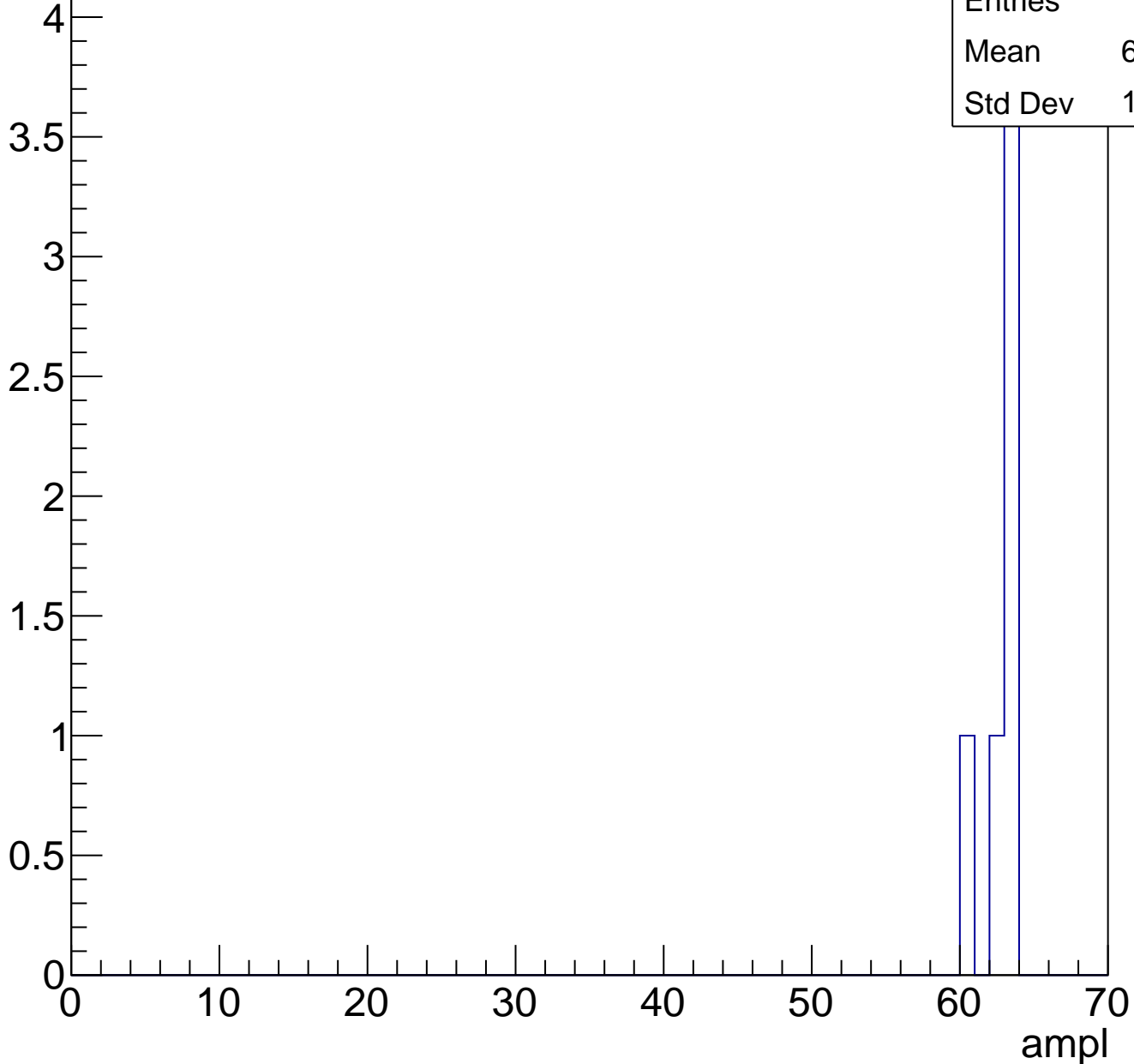
Entries	40
Mean	58.3
Std Dev	9.686



# B1L101S, U20-ch125, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U20-ch125, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U20-ch126, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	93
Mean	28.84
Std Dev	5.116

**Gaus mean : 29.4567**

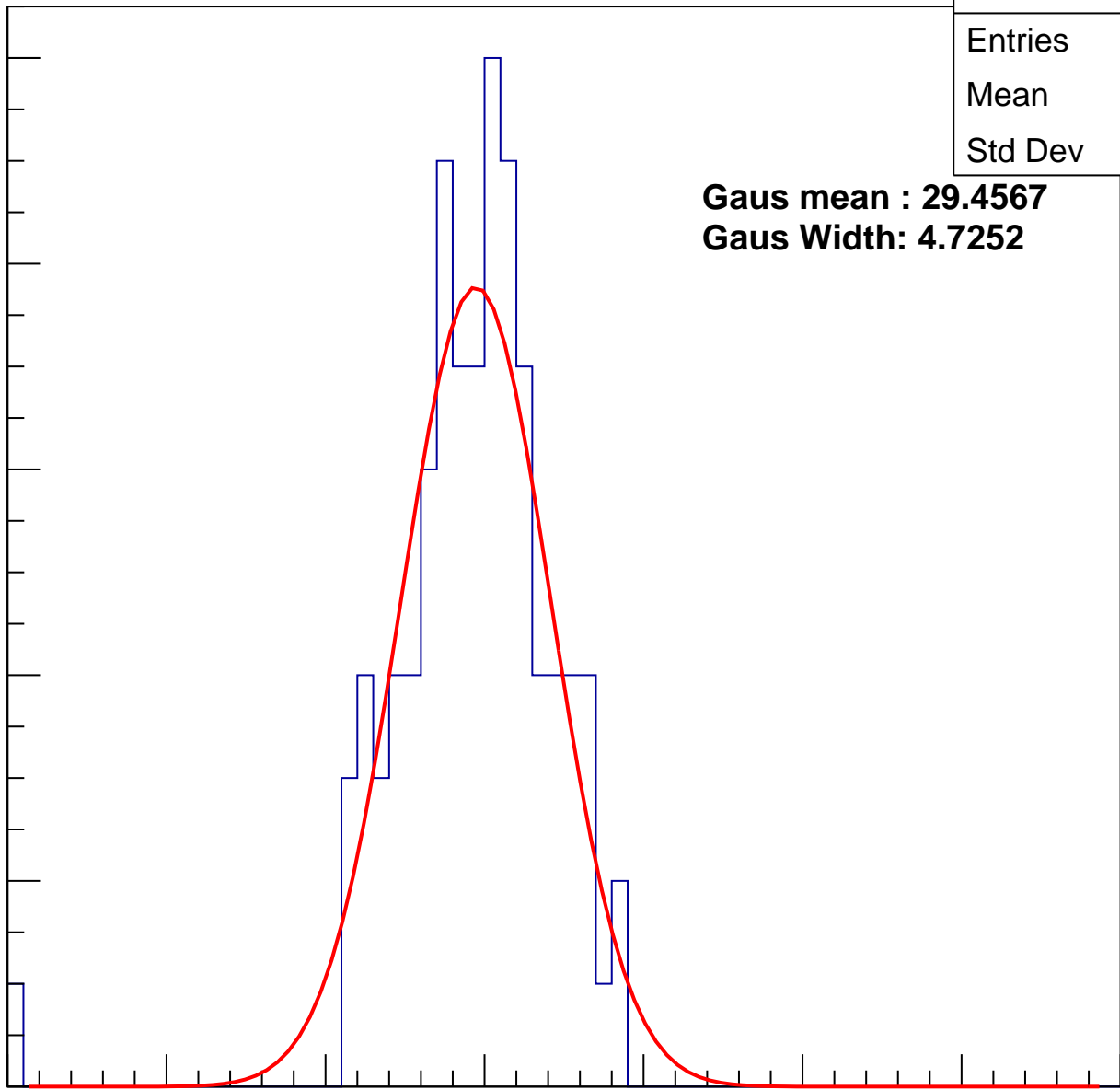
**Gaus Width: 4.7252**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U20-ch126, adc1

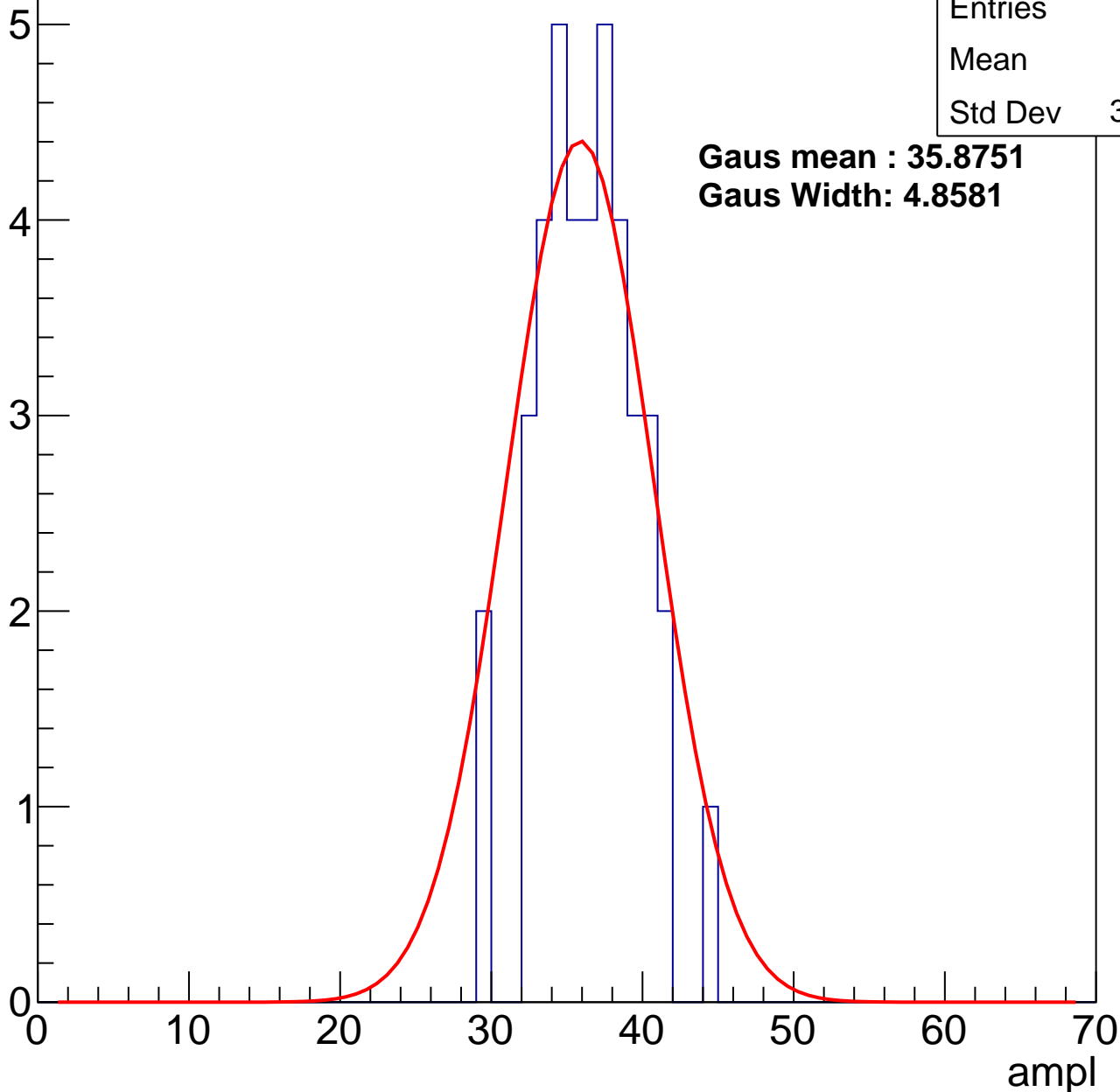
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	40
Mean	36
Std Dev	3.225

**Gaus mean : 35.8751**

**Gaus Width: 4.8581**



# B1L101S, U20-ch126, adc2

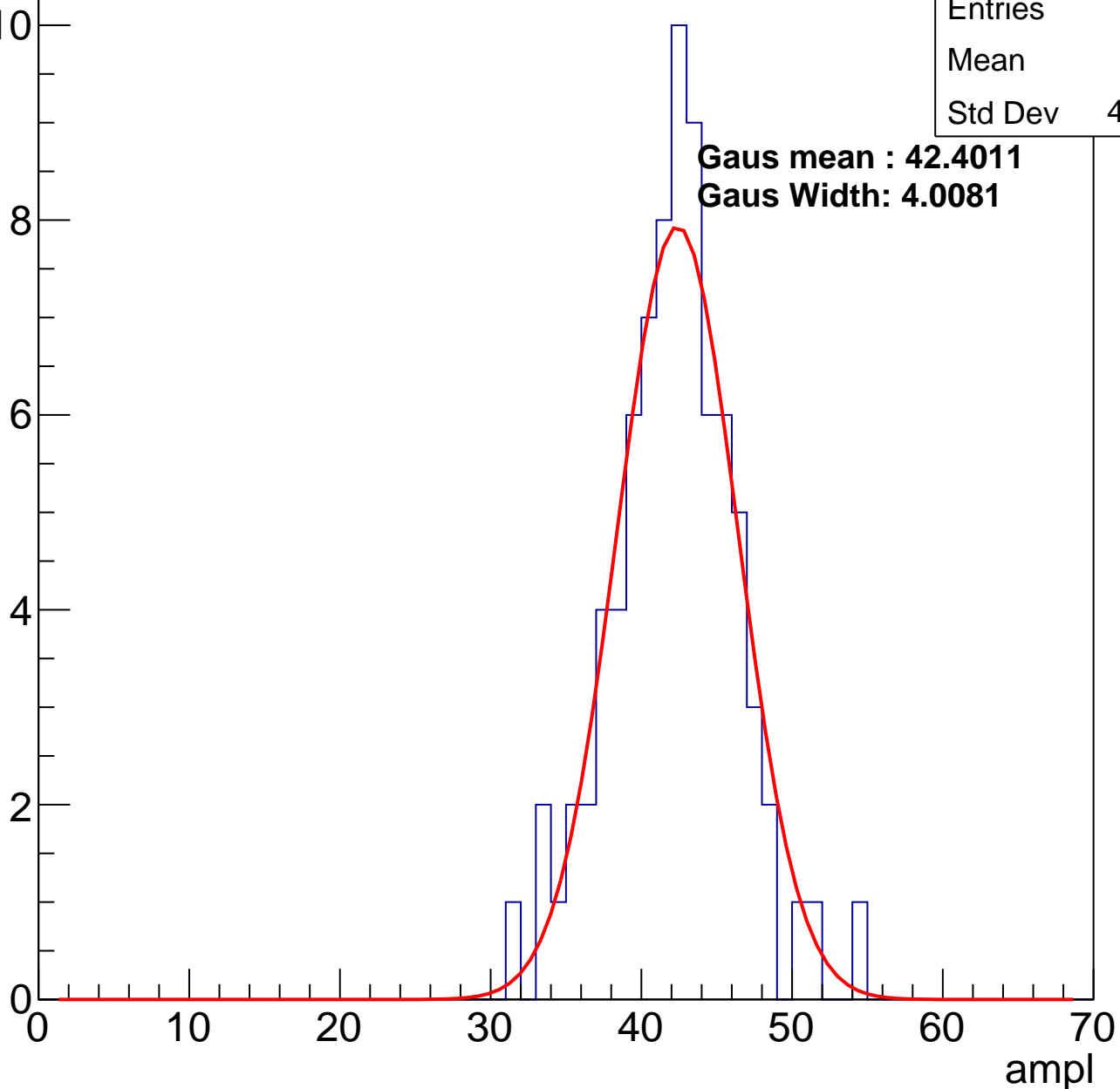
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	81
Mean	41.7
Std Dev	4.108

**Gaus mean : 42.4011**

**Gaus Width: 4.0081**

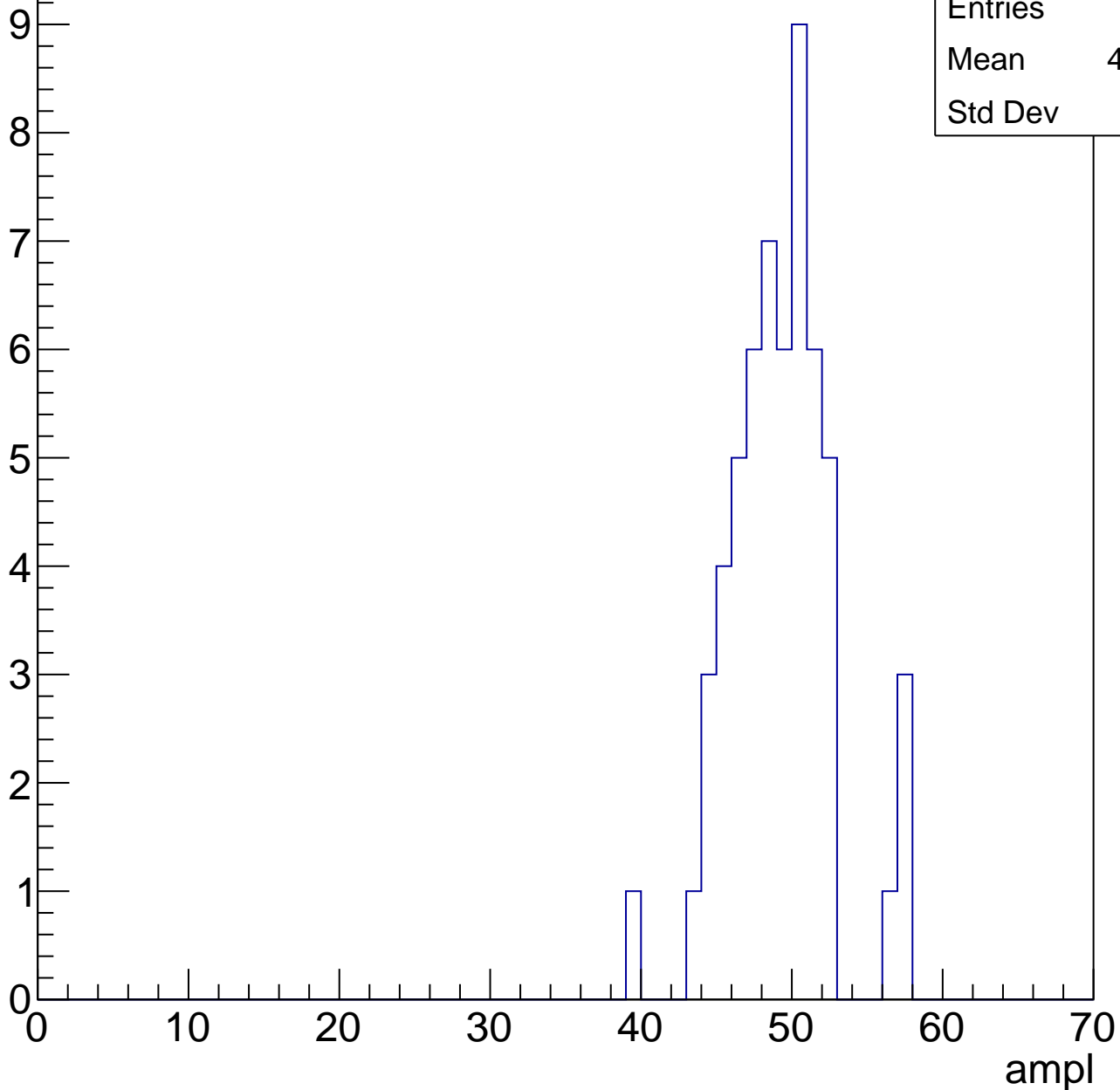


# B1L101S, U20-ch126, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	57
Mean	48.75
Std Dev	3.42



# B1L101S, U20-ch126, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	70
Mean	55.14
Std Dev	3.407

Entry

10

8

6

4

2

0

0

10

20

30

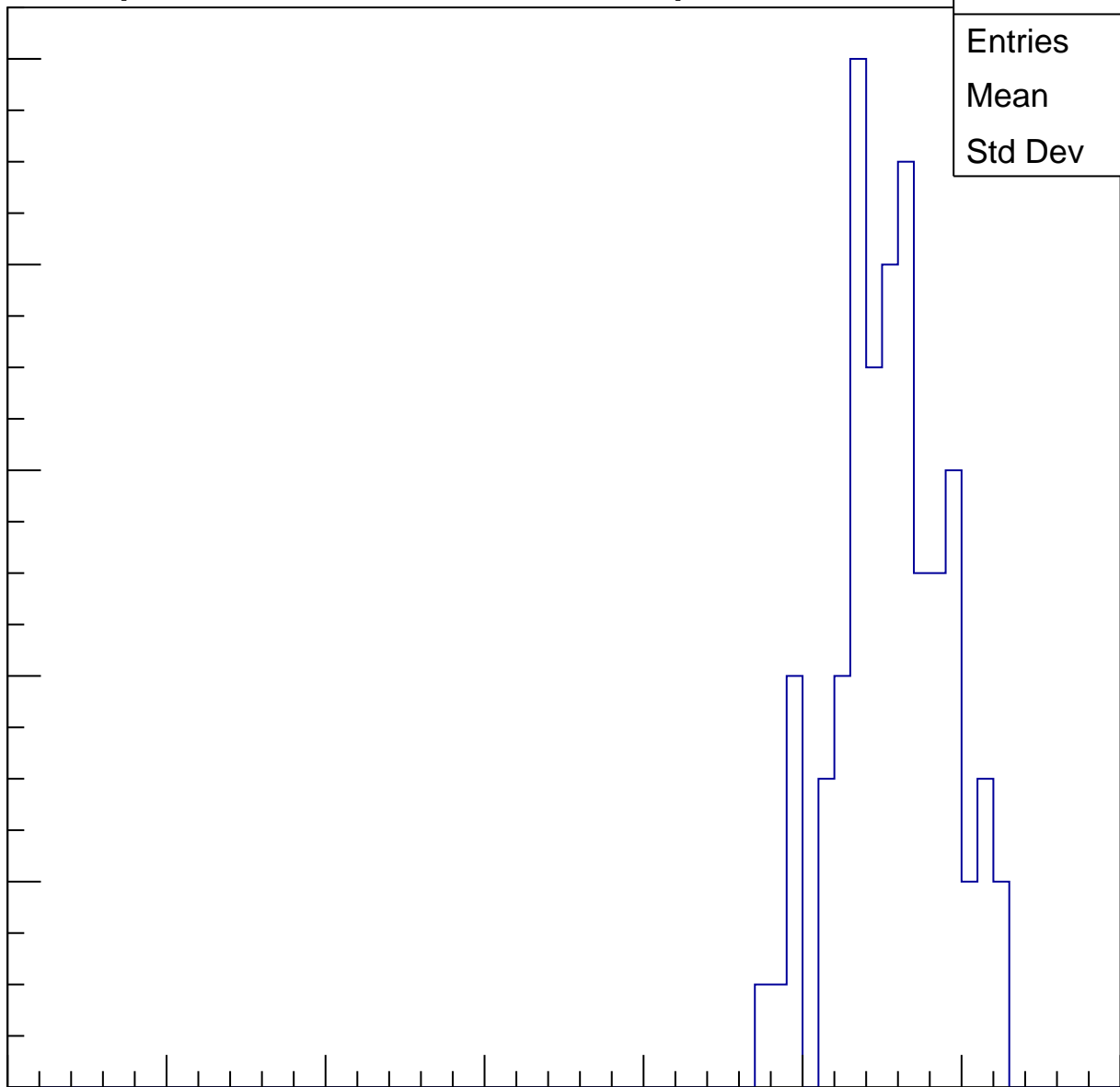
40

50

60

ampl

70

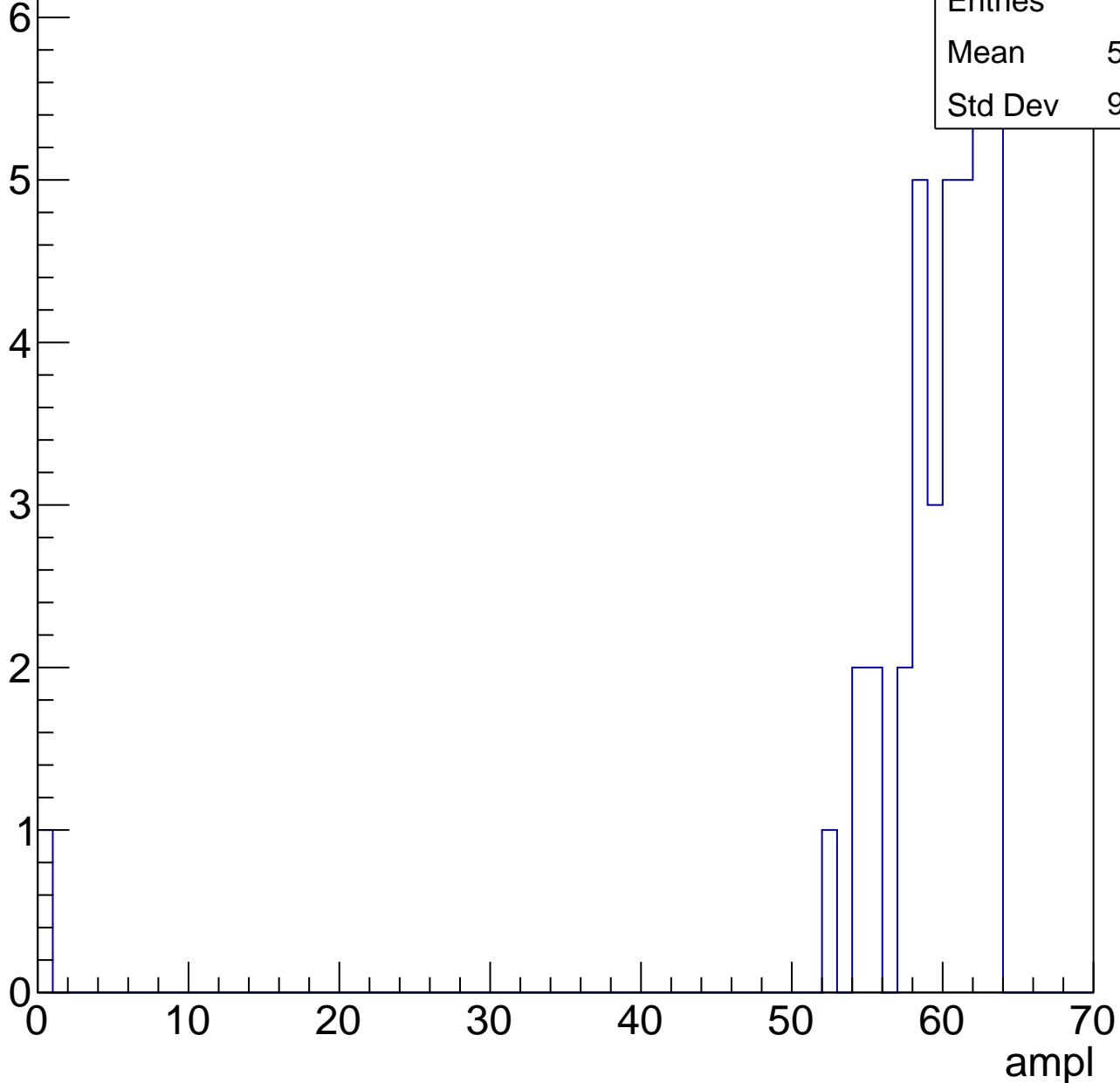


# B1L101S, U20-ch126, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

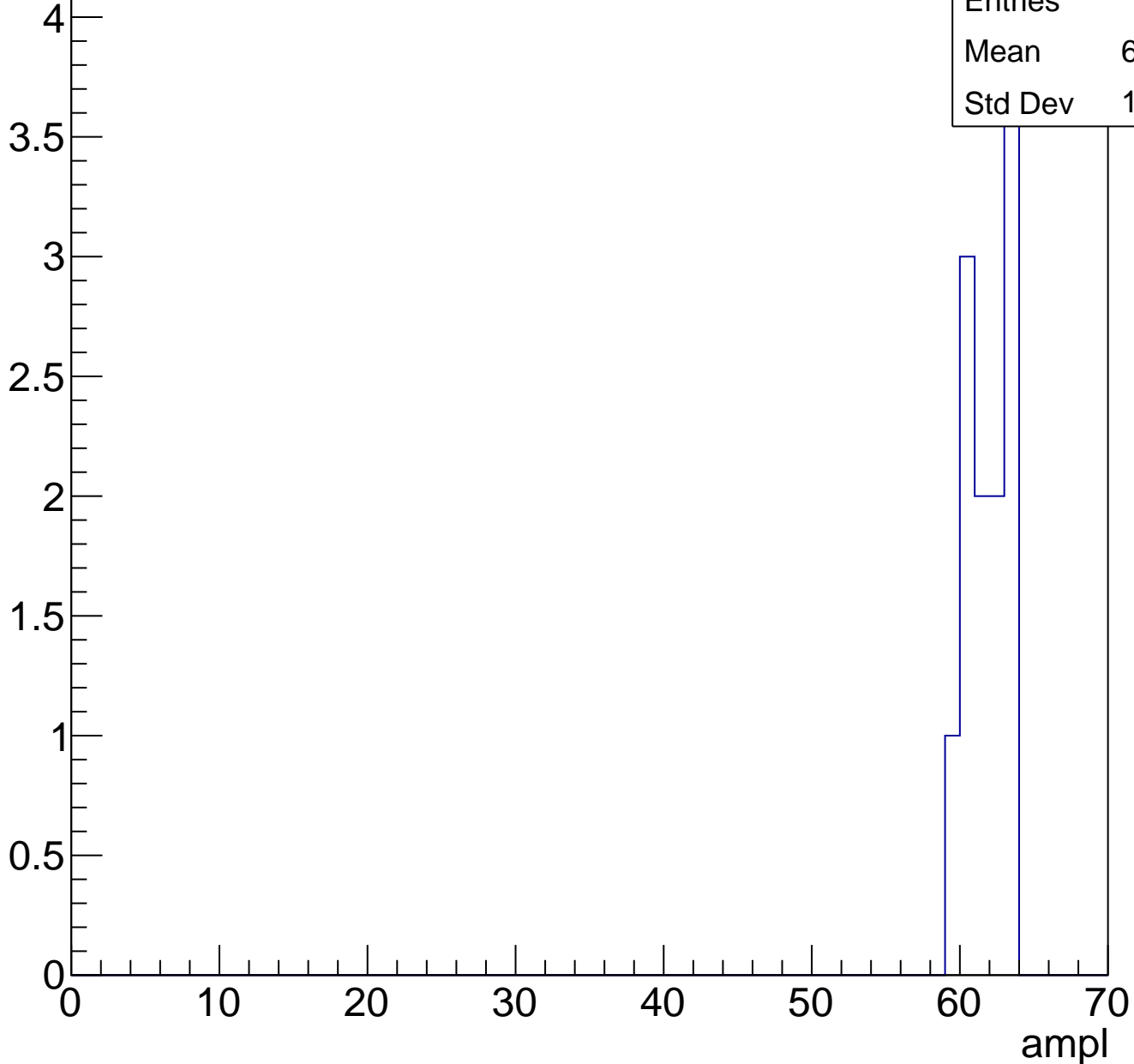
Entries	38
Mean	58.05
Std Dev	9.955



# B1L101S, U20-ch126, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U20-ch126, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U20-ch127, adc0

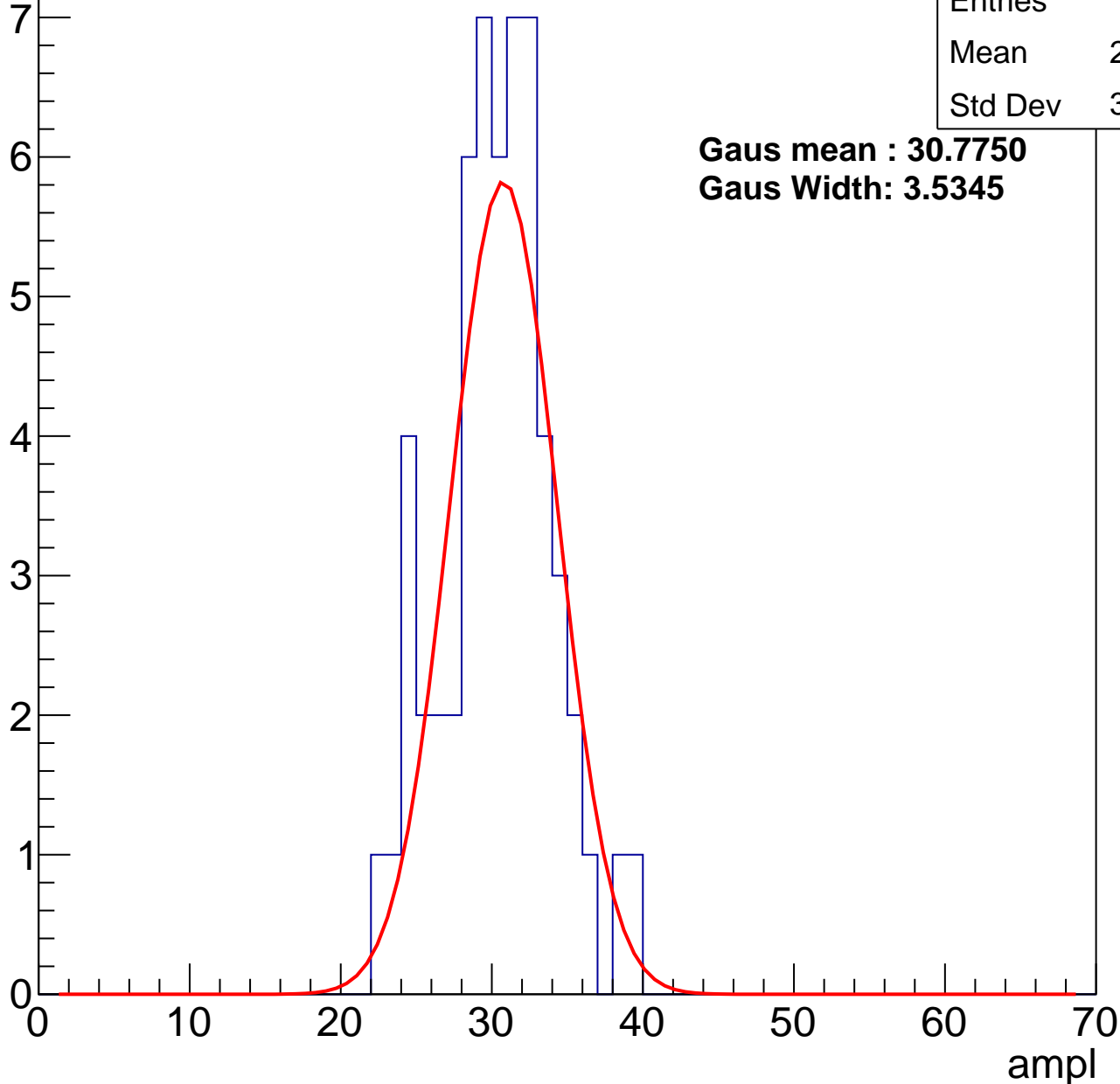
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	57
Mean	29.93
Std Dev	3.598

**Gaus mean : 30.7750**

**Gaus Width: 3.5345**



# B1L101S, U20-ch127, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	81
Mean	36.78
Std Dev	3.897

**Gaus mean : 37.6150**

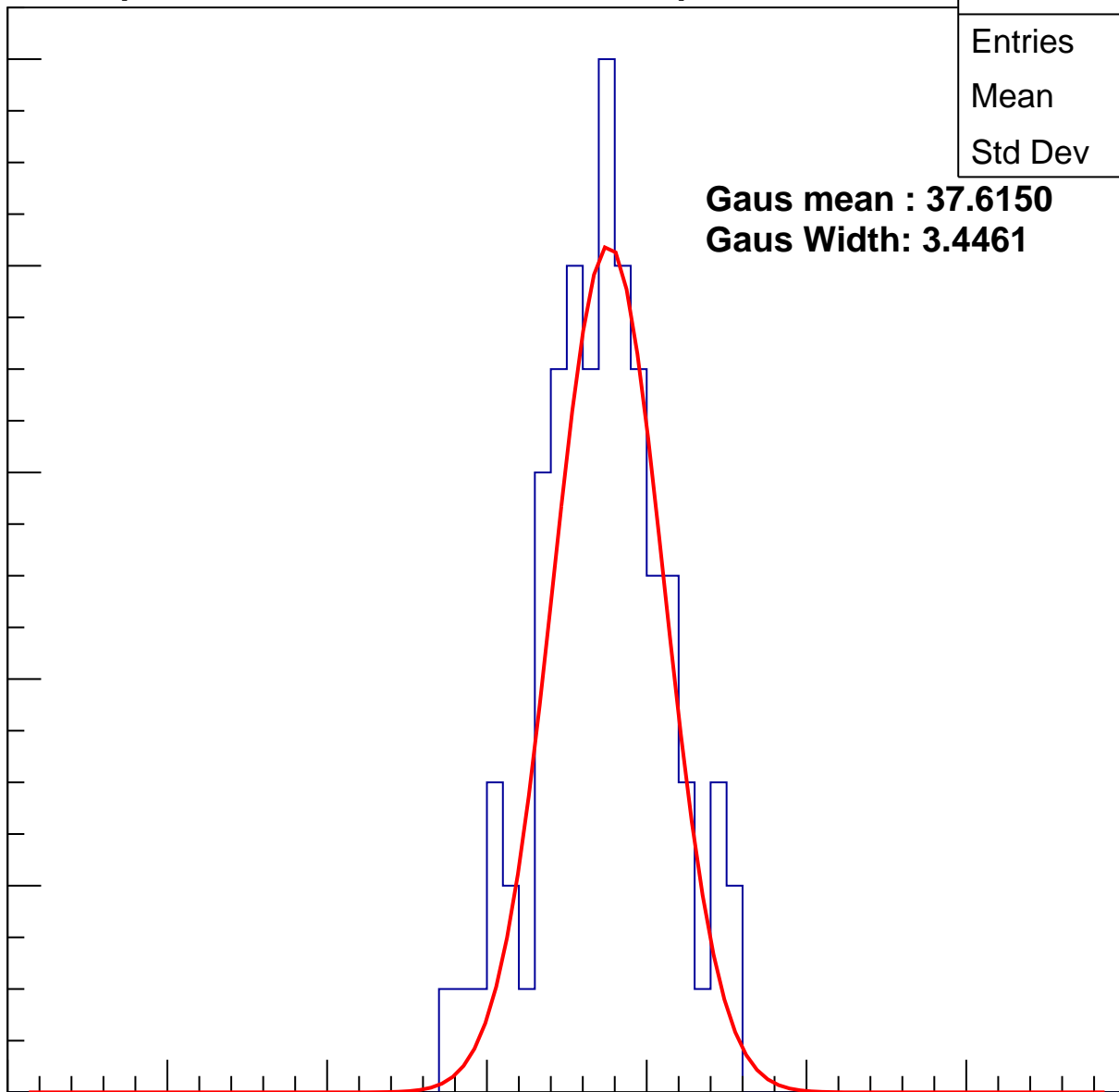
**Gaus Width: 3.4461**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B1L101S, U20-ch127, adc2

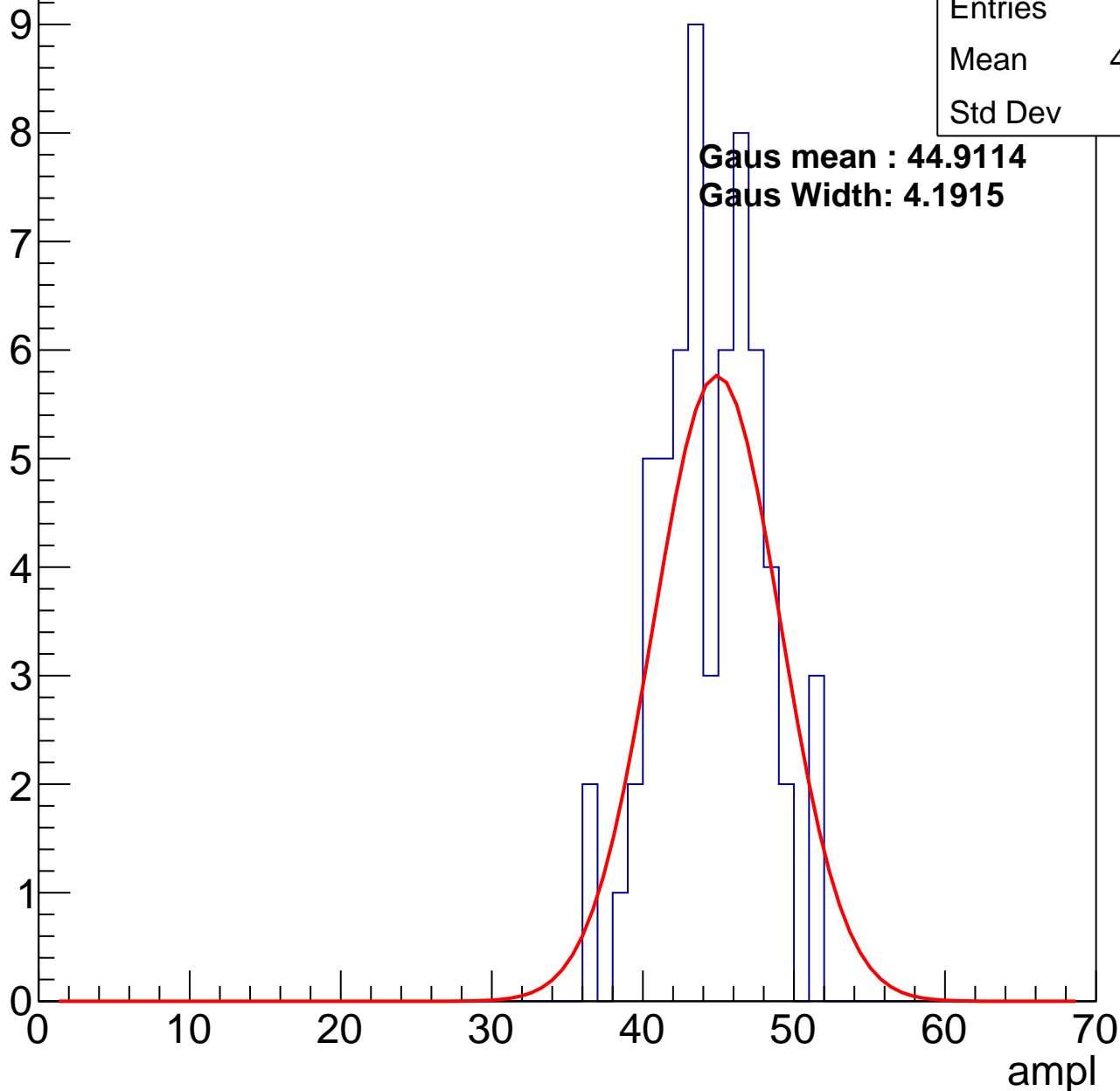
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	43.98
Std Dev	3.42

**Gaus mean : 44.9114**

**Gaus Width: 4.1915**



# B1L101S, U20-ch127, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	73
Mean	50.58
Std Dev	3.526

Entry

10

8

6

4

2

0

0

10

20

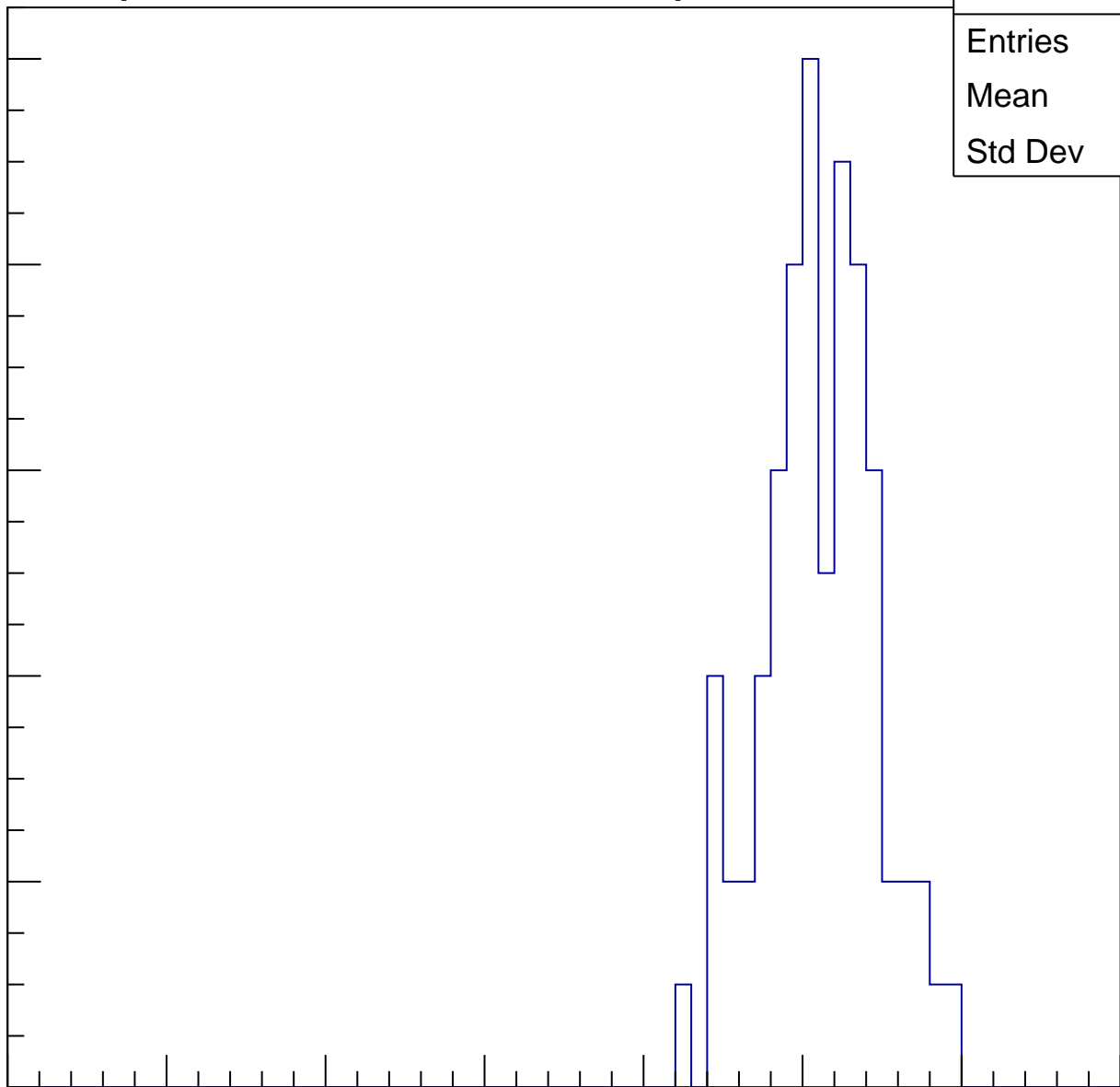
30

40

50

60

ampl



# B1L101S, U20-ch127, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

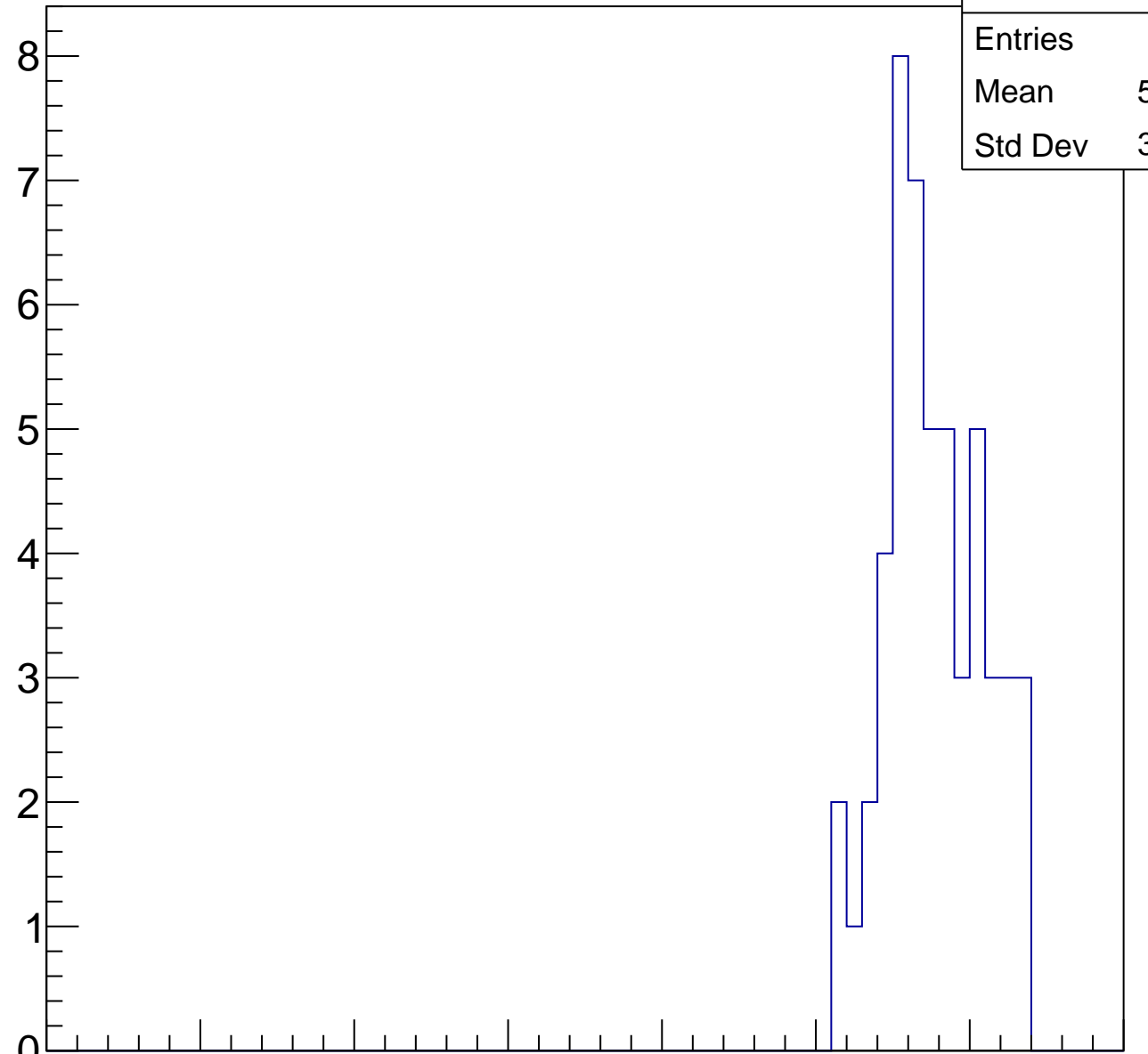
Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	51
Mean	57.22
Std Dev	3.114

ampl

0 10 20 30 40 50 60 70

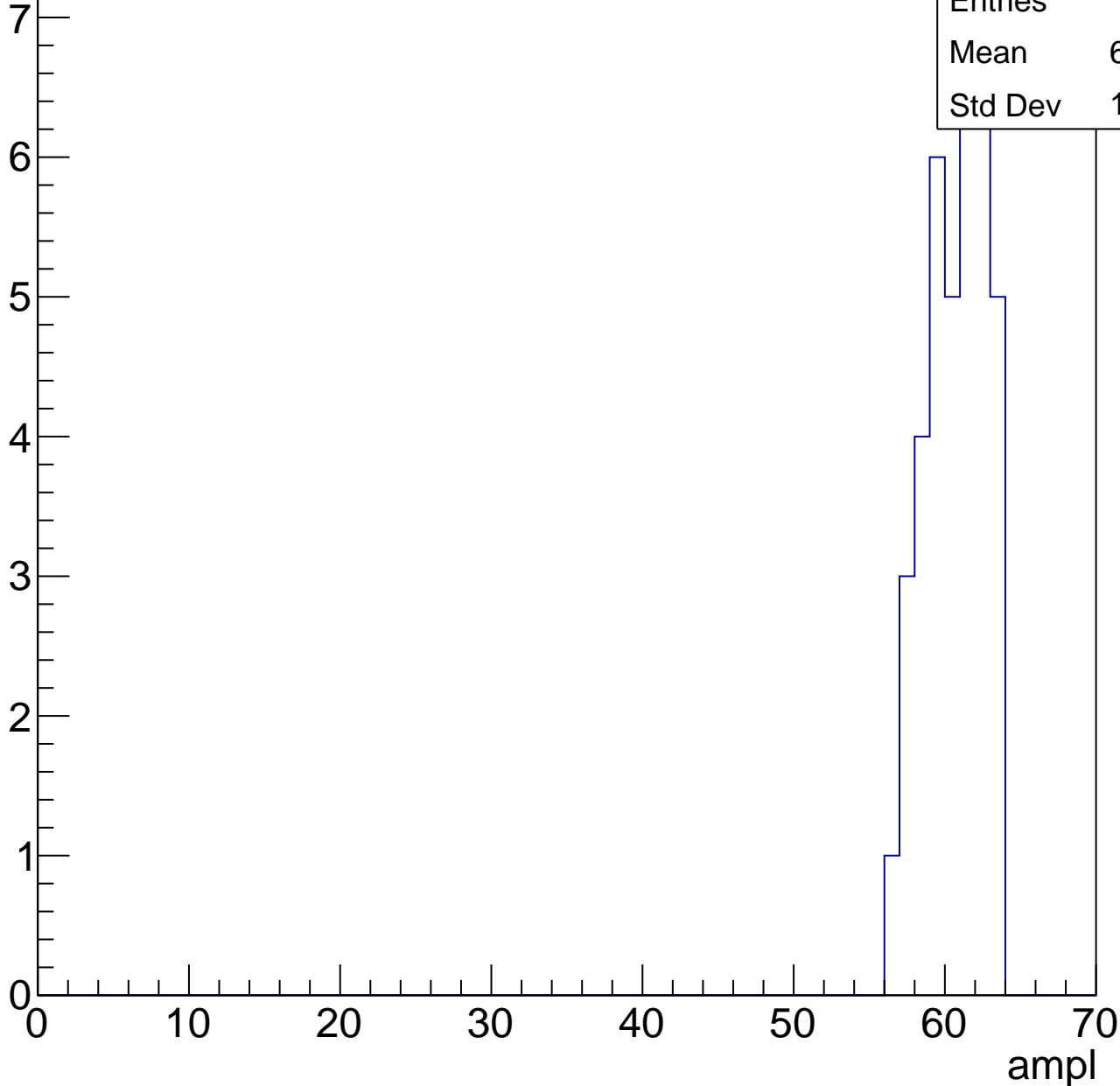


# B1L101S, U20-ch127, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	38
Mean	60.24
Std Dev	1.939



# B1L101S, U20-ch127, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	2
Mean	63
Std Dev	0

ampl



# B1L101S, U20-ch127, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L101S, U20-ch127, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

