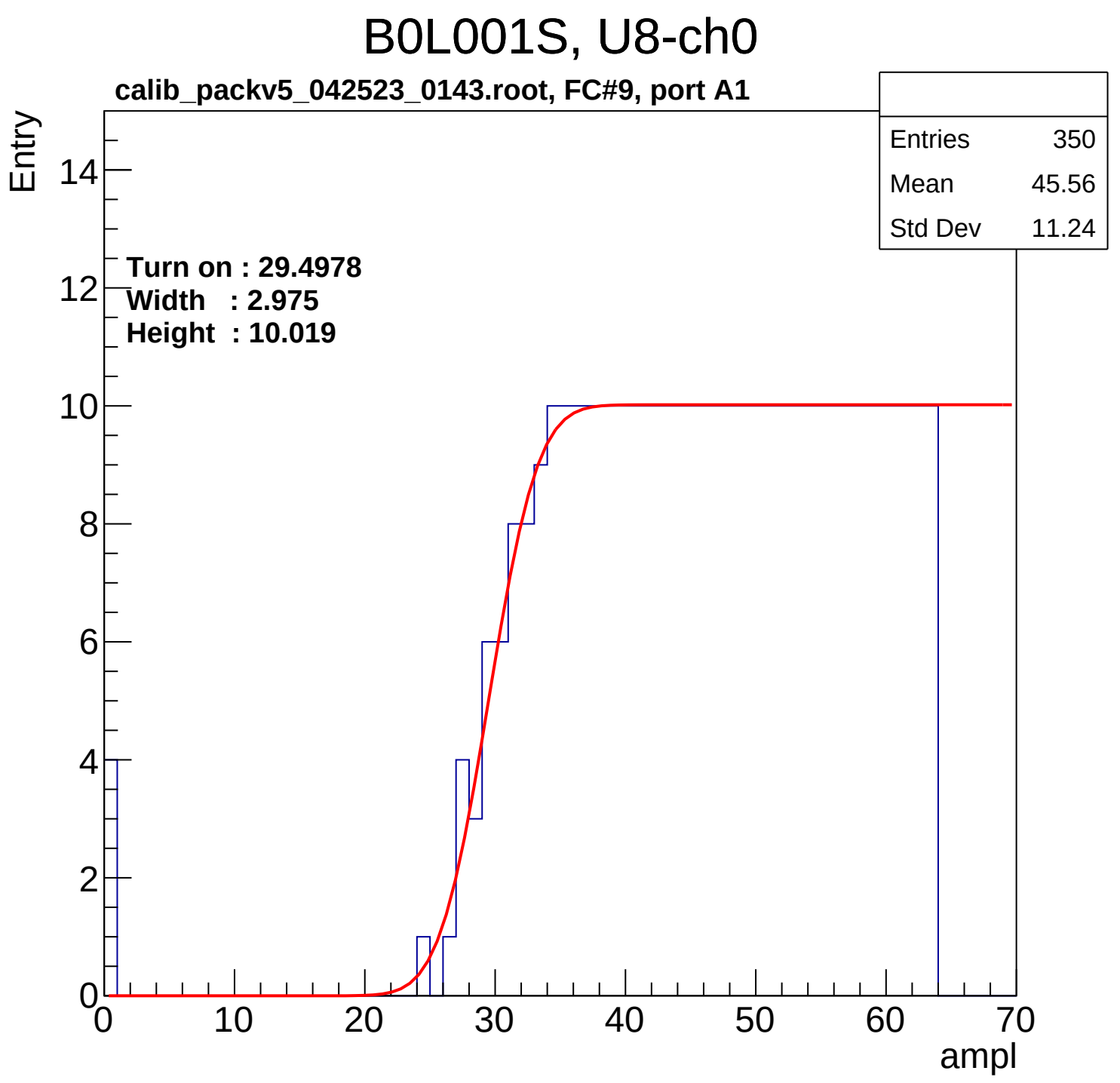
B0L001S, U8-ch0
calib_packv5_042523_0143.root, FC#9, port A1
Entries 350
Mean 45.56
Std Dev 11.24
Turn on : 29.4978
Width : 2.975
Height : 10.019
Entry
ampl
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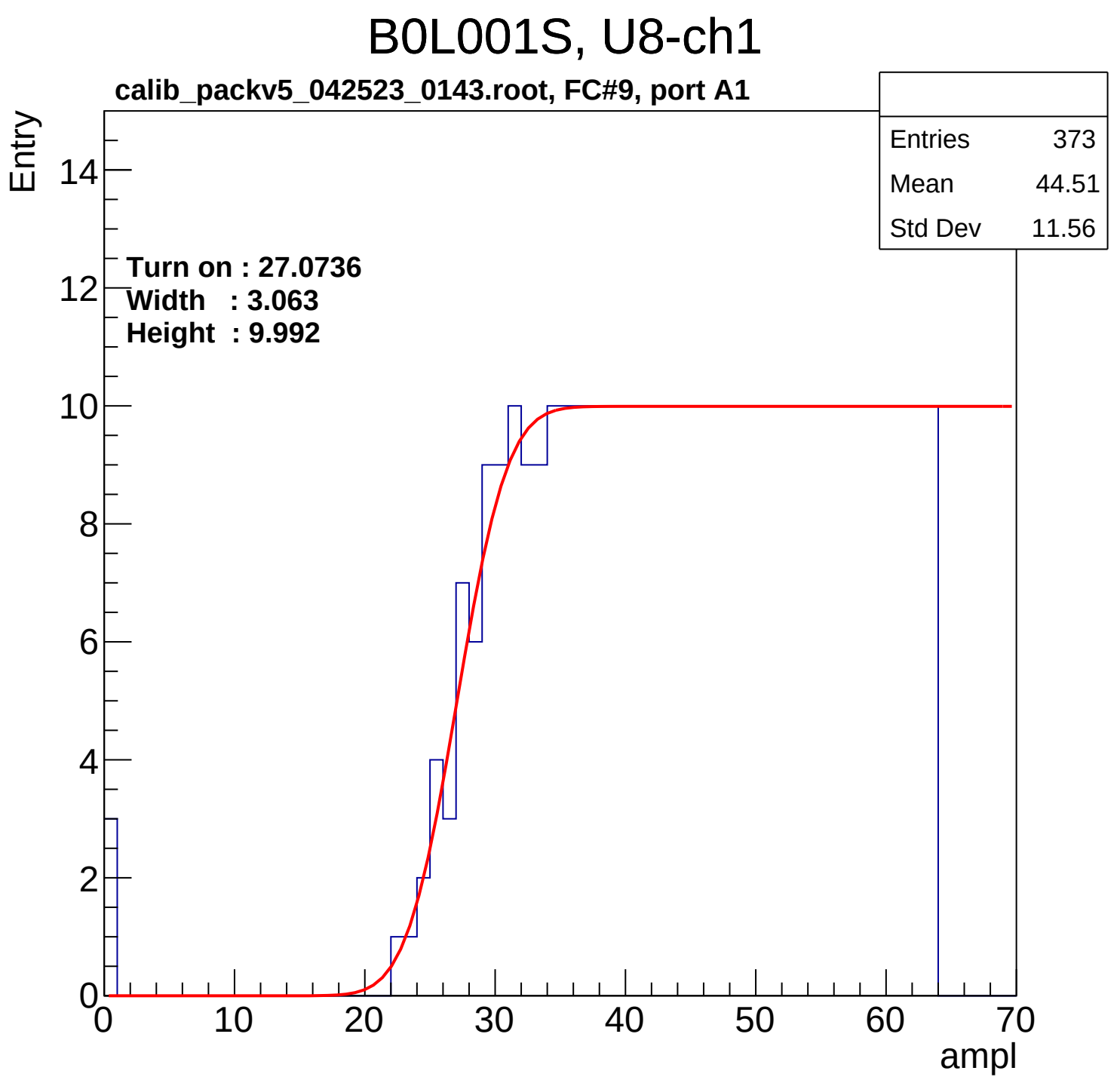
B0L001S, U8-ch1
calib_packv5_042523_0143.root, FC#9, port A1
Entries 373
Mean 44.51
Std Dev 11.56
Turn on : 27.0736
Width : 3.063
Height : 9.992
Entry
ampl
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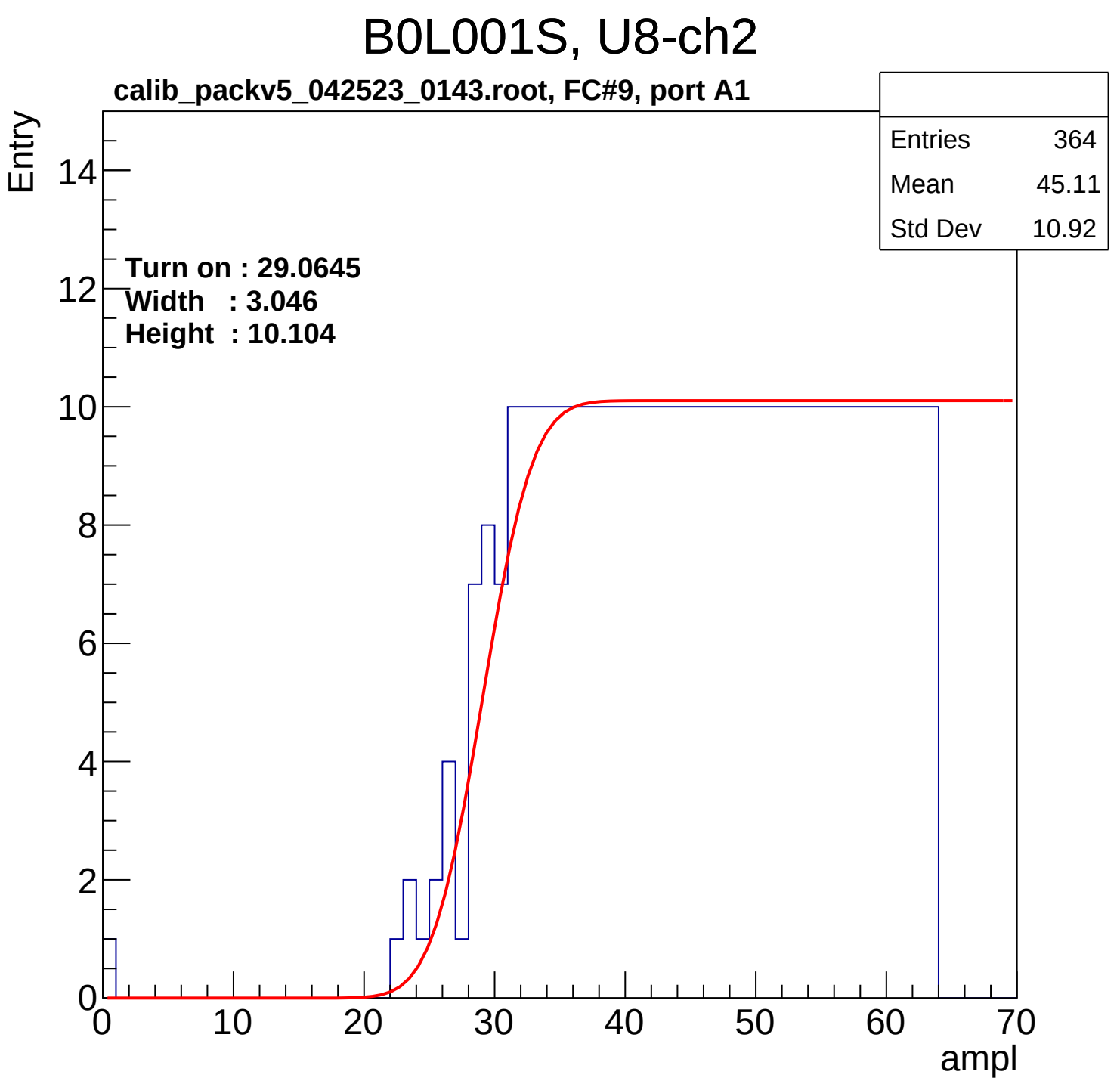
B0L001S, U8-ch2
calib_packv5_042523_0143.root, FC#9, port A1
Entries 364
Mean 45.11
Std Dev 10.92
Turn on : 29.0645
Width : 3.046
Height : 10.104
Entry
ampl
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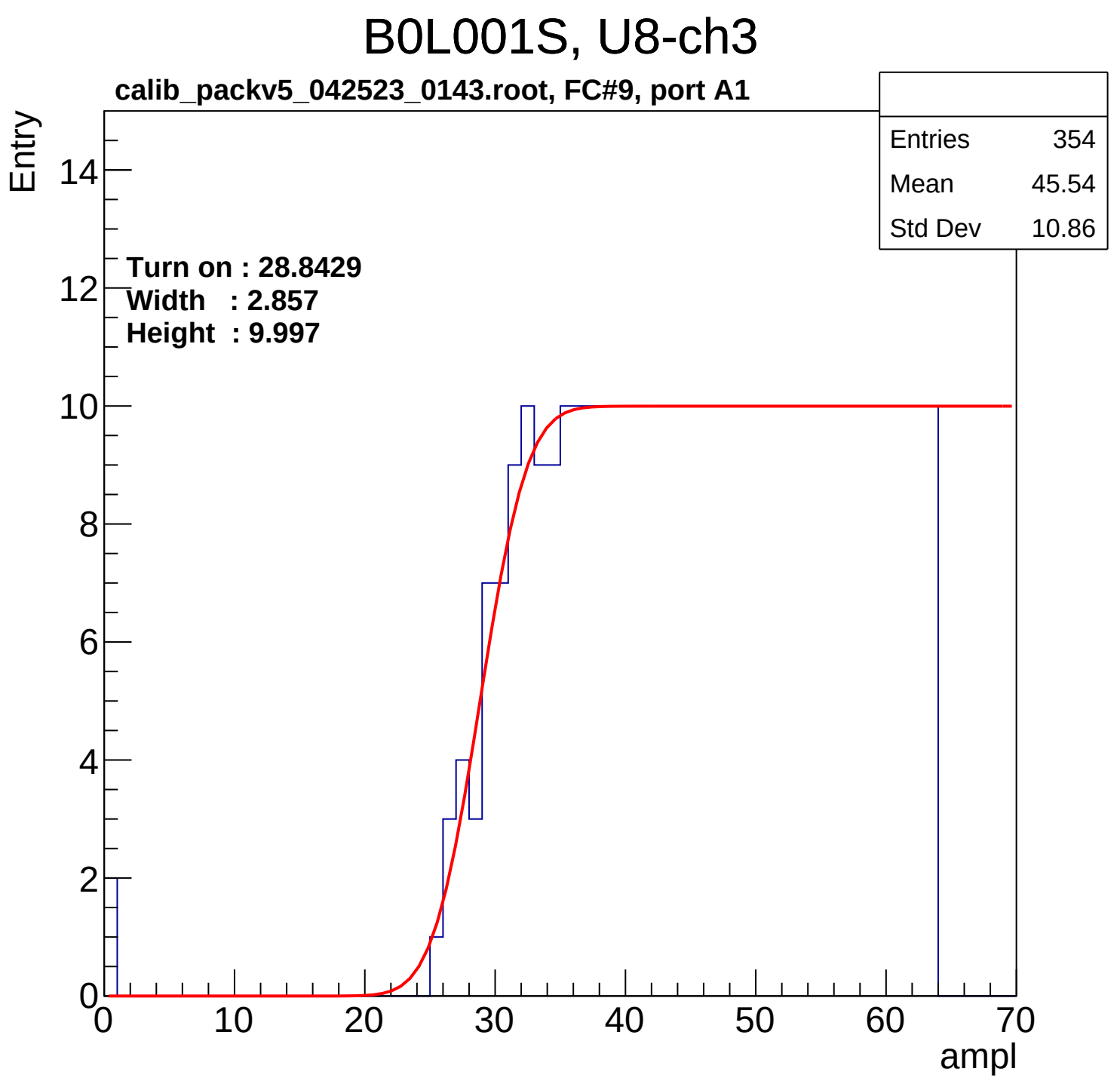
B0L001S, U8-ch3
calib_packv5_042523_0143.root, FC#9, port A1
Entries 354
Mean 45.54
Std Dev 10.86
Turn on : 28.8429
Width : 2.857
Height : 9.997
Entry
ampl
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2
4
6
8
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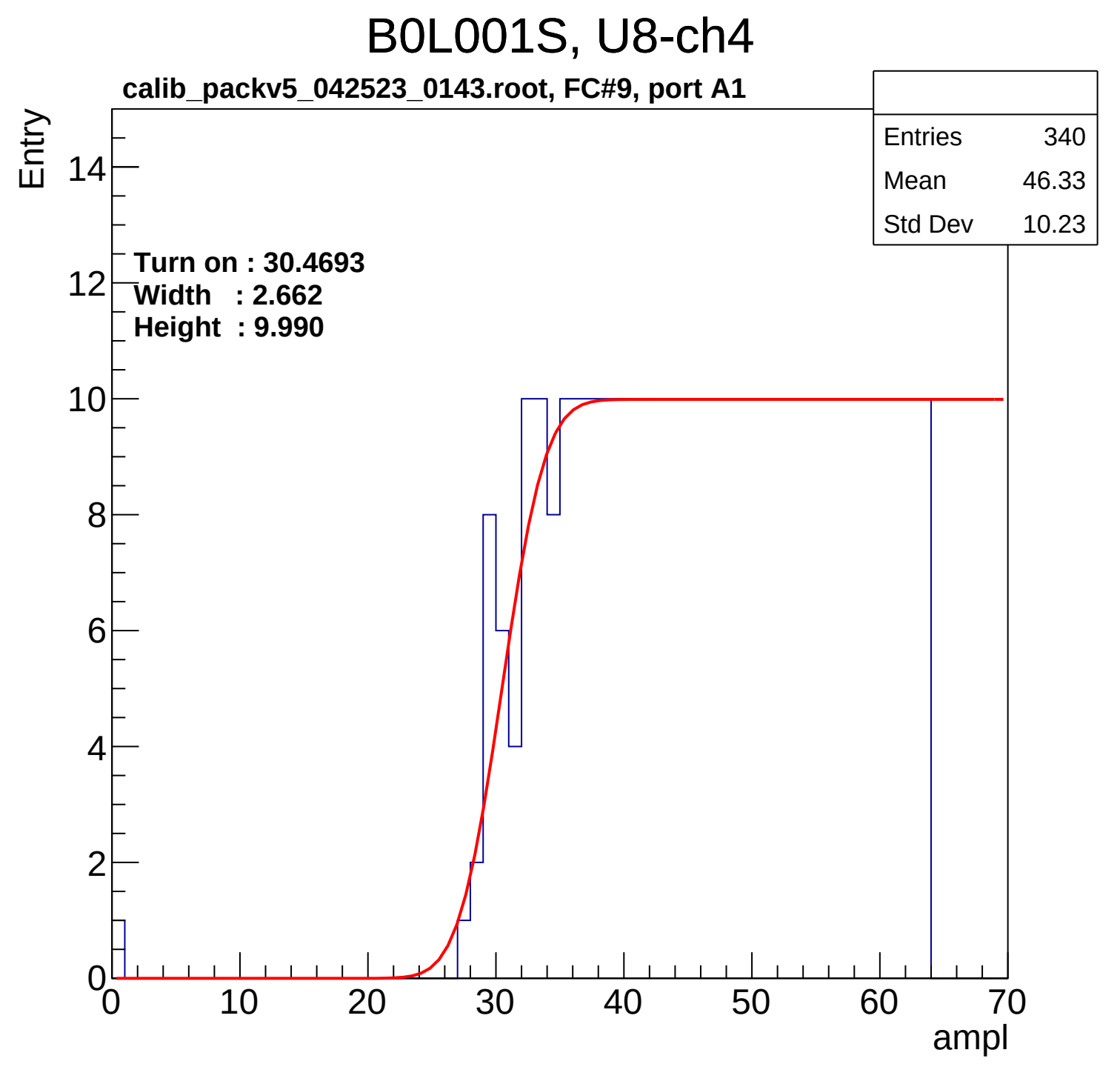
B0L001S, U8-ch4
calib_packv5_042523_0143.root, FC#9, port A1
Entries 340
Mean 46.33
Std Dev 10.23
Turn on : 30.4693
Width : 2.662
Height : 9.990
Entry
ampl
0
2
4
6
8
10
12
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0
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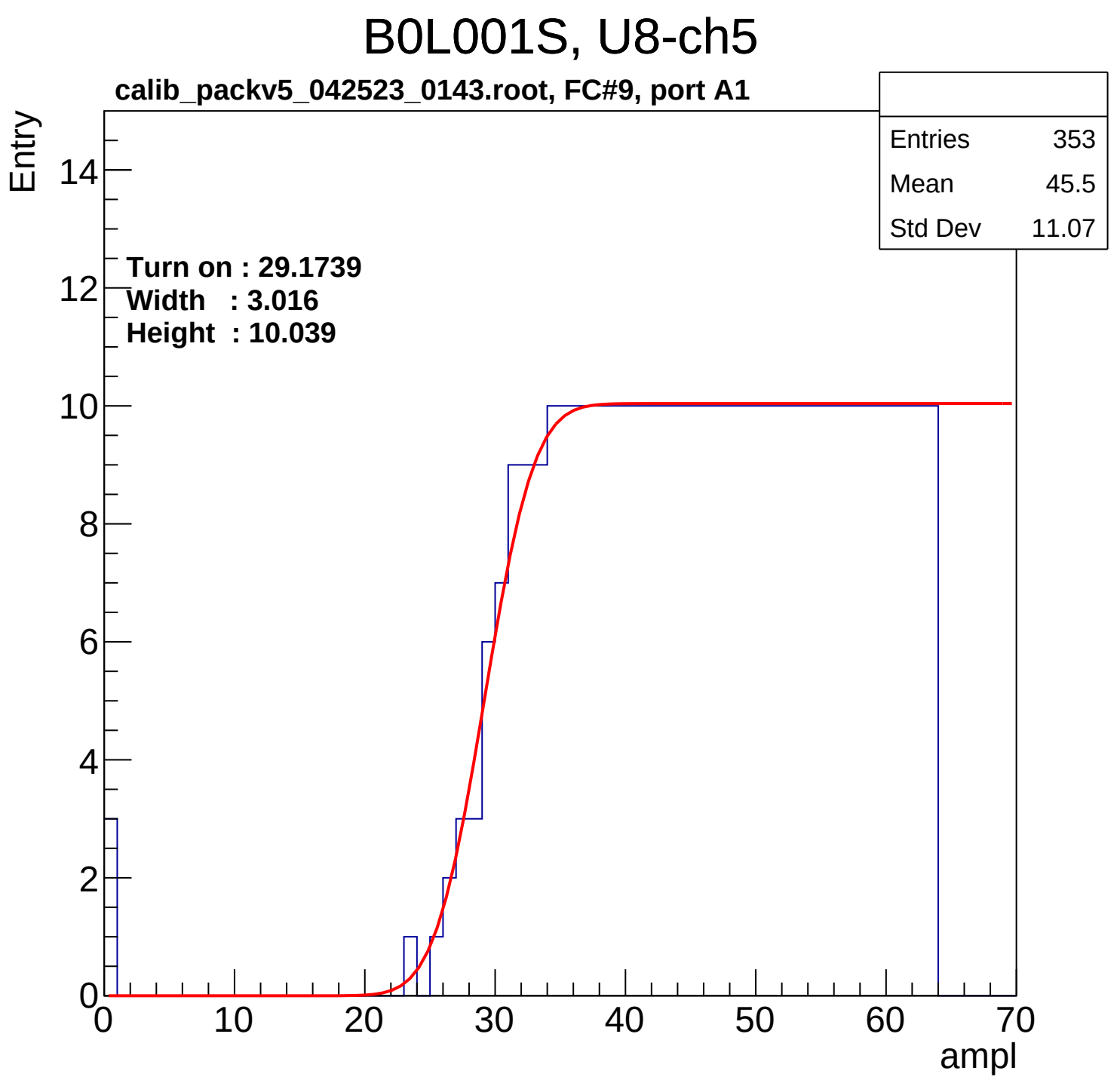
B0L001S, U8-ch5
calib_packv5_042523_0143.root, FC#9, port A1
Entries 353
Mean 45.5
Std Dev 11.07
Turn on : 29.1739
Width : 3.016
Height : 10.039
Entry
ampl
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2
4
6
8
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12
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0
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60
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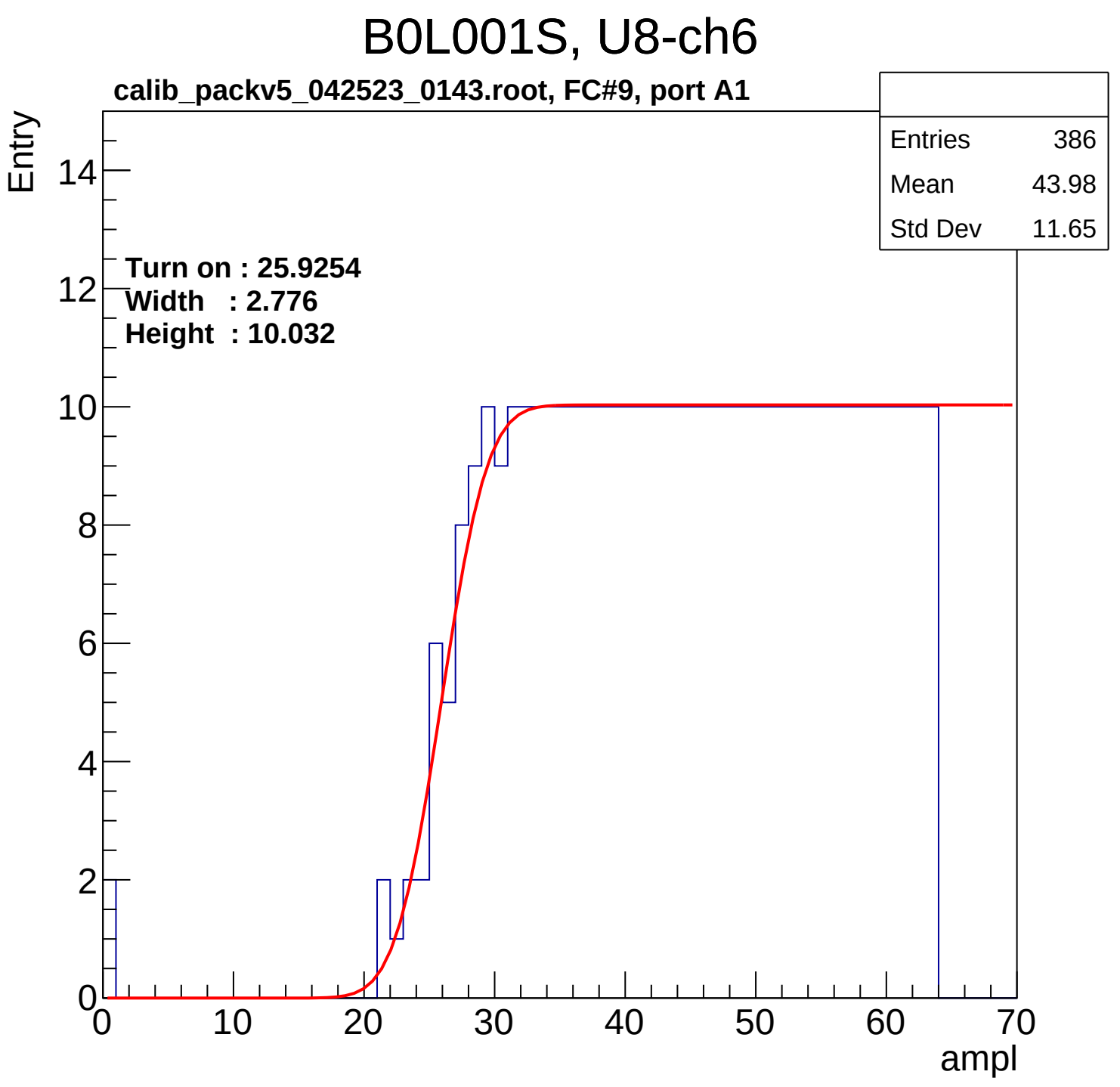
B0L001S, U8-ch6
calib_packv5_042523_0143.root, FC#9, port A1
Entries 386
Mean 43.98
Std Dev 11.65
Turn on : 25.9254
Width : 2.776
Height : 10.032
Entry
ampl
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2
4
6
8
10
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0
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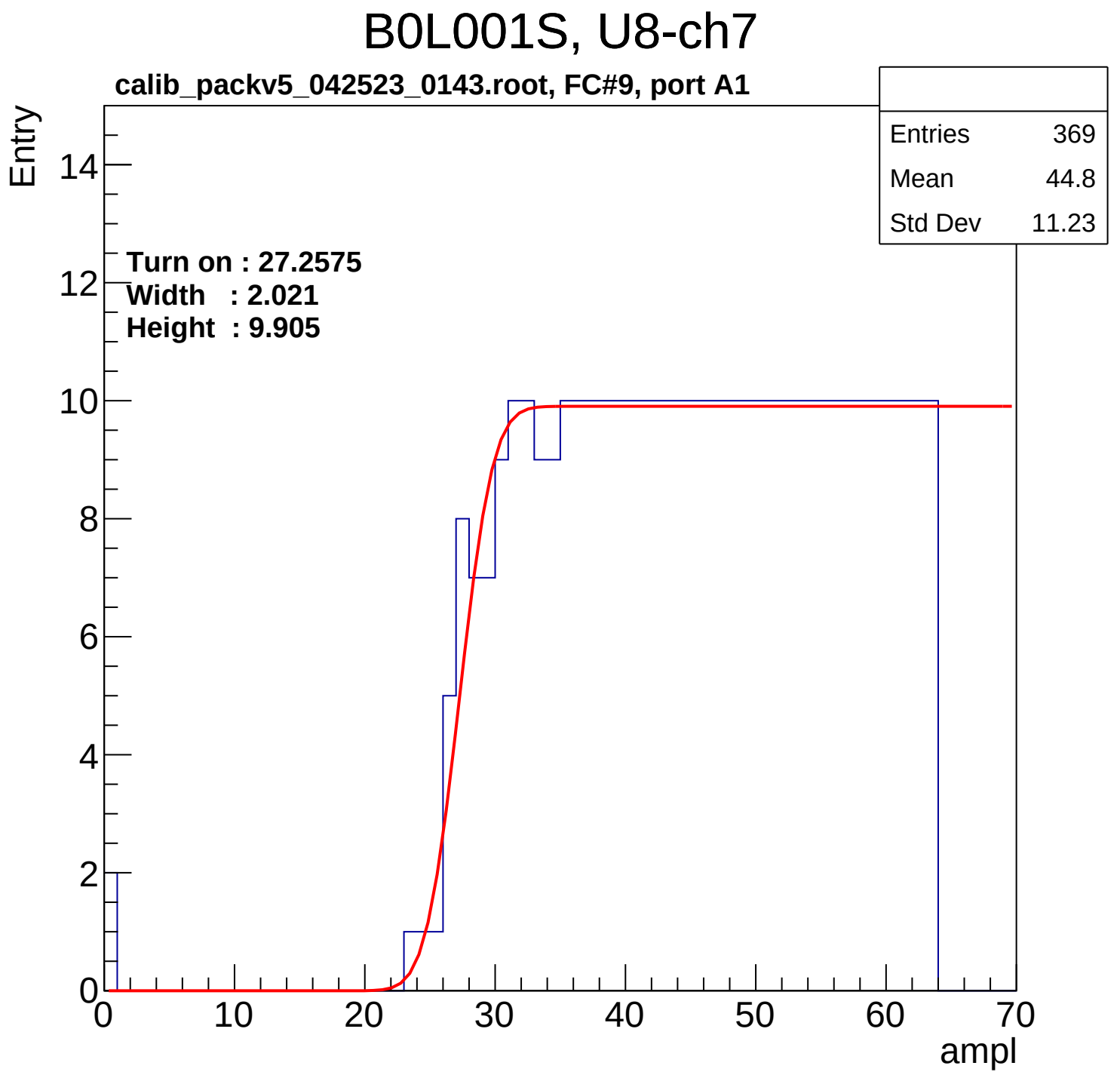
B0L001S, U8-ch7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 369
Mean 44.8
Std Dev 11.23
Turn on : 27.2575
Width : 2.021
Height : 9.905
Entry
ampl
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2
4
6
8
10
12
14
0
10
20
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40
50
60
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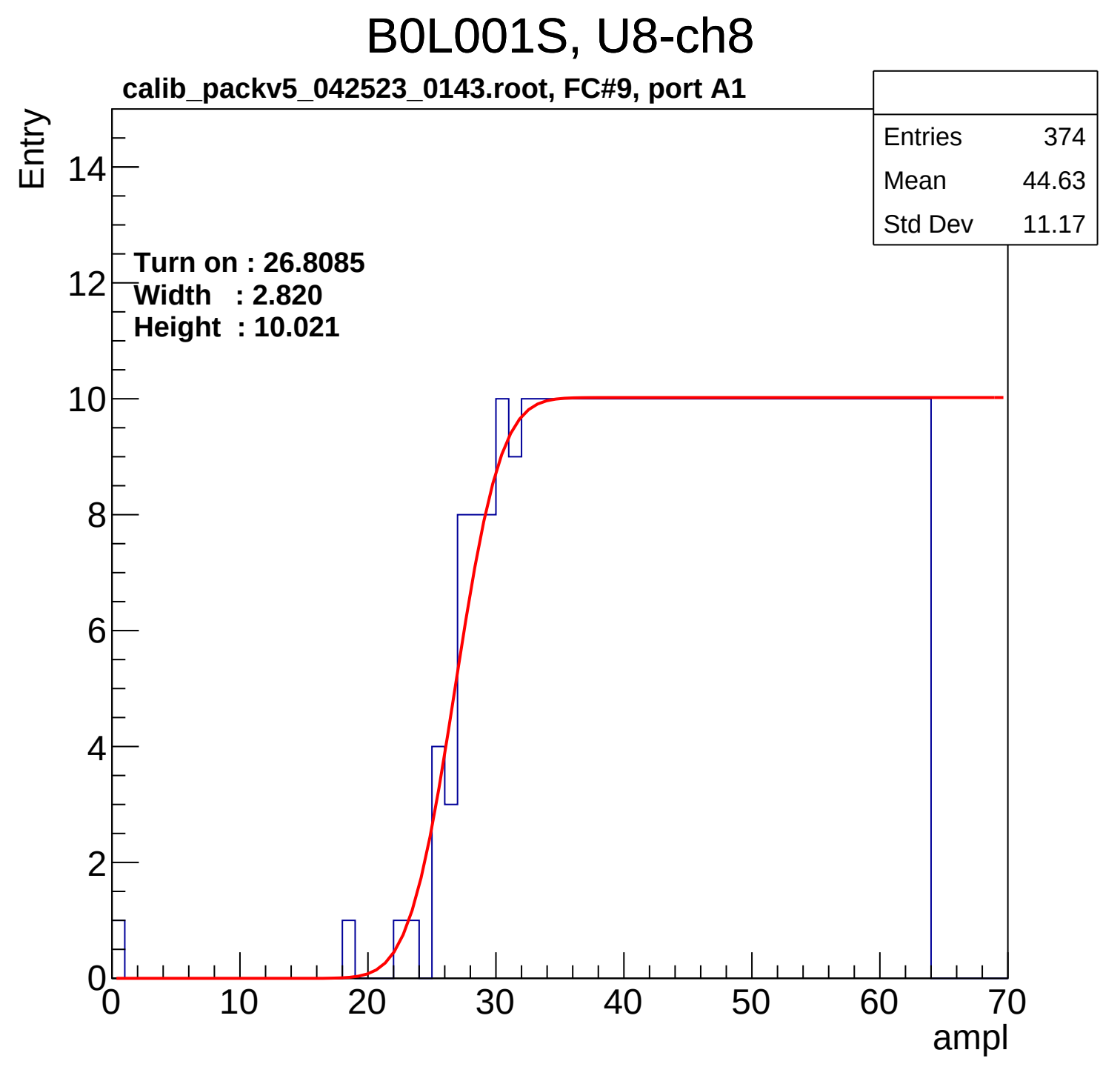
B0L001S, U8-ch8
calib_packv5_042523_0143.root, FC#9, port A1
Entries 374
Mean 44.63
Std Dev 11.17
Turn on : 26.8085
Width : 2.820
Height : 10.021
Entry
ampl
0
2
4
6
8
10
12
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0
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20
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40
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60
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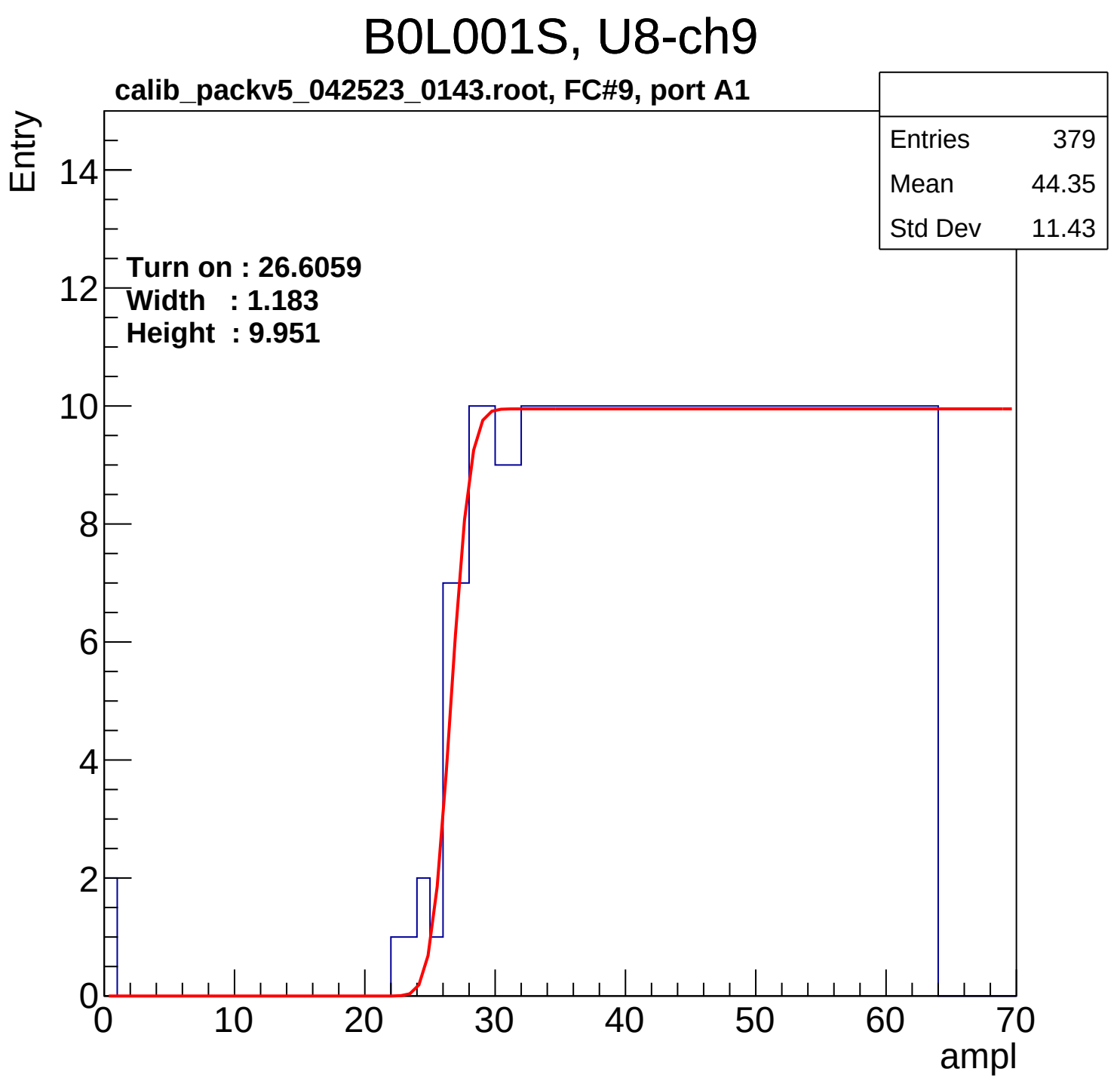
B0L001S, U8-ch9
calib_packv5_042523_0143.root, FC#9, port A1
Entries 379
Mean 44.35
Std Dev 11.43
Turn on : 26.6059
Width : 1.183
Height : 9.951
Entry
ampl
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2
4
6
8
10
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0
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20
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40
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60
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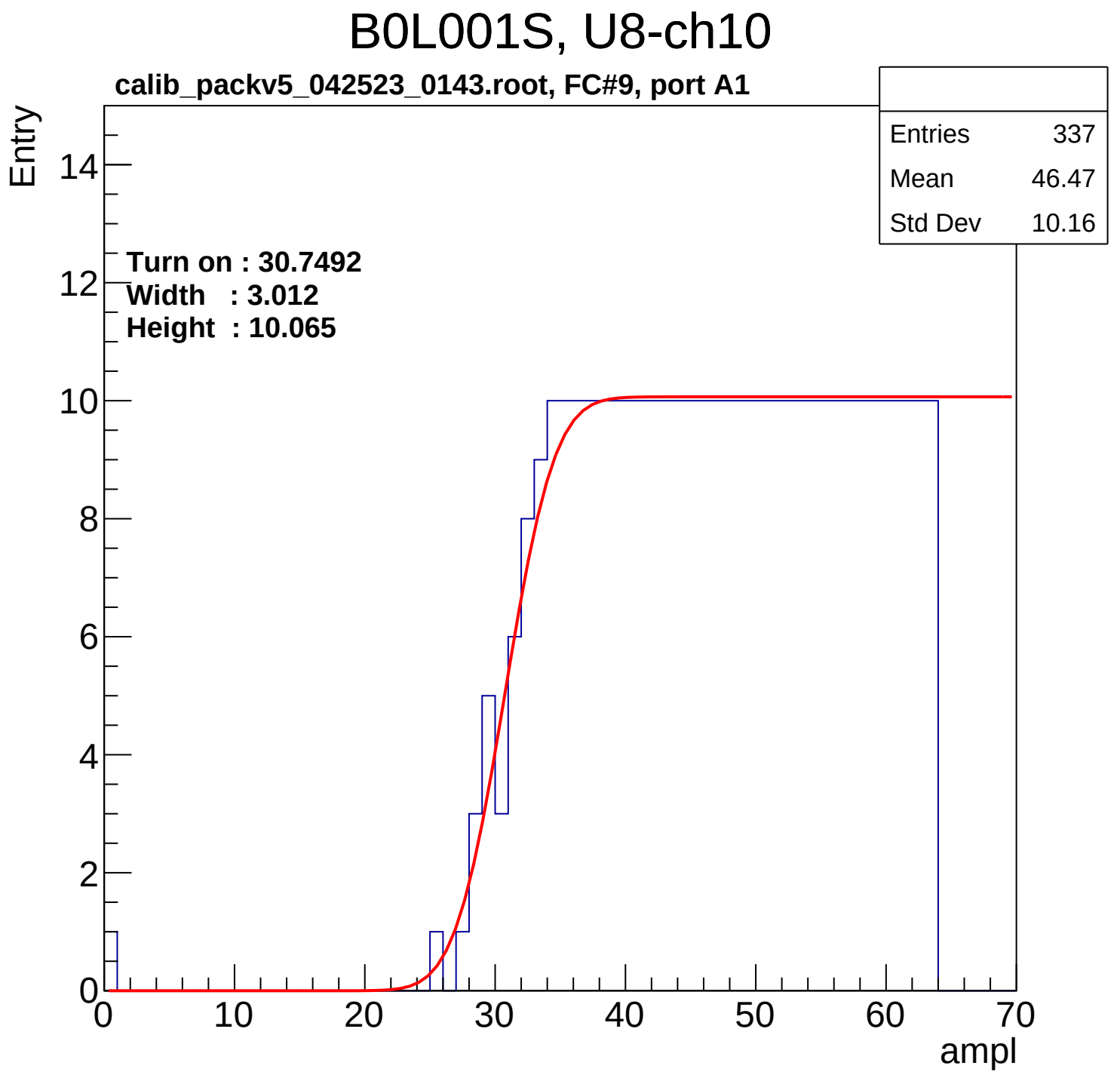
B0L001S, U8-ch10
calib_packv5_042523_0143.root, FC#9, port A1
Entries 337
Mean 46.47
Std Dev 10.16
Turn on : 30.7492
Width : 3.012
Height : 10.065
Entry
ampl
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2
4
6
8
10
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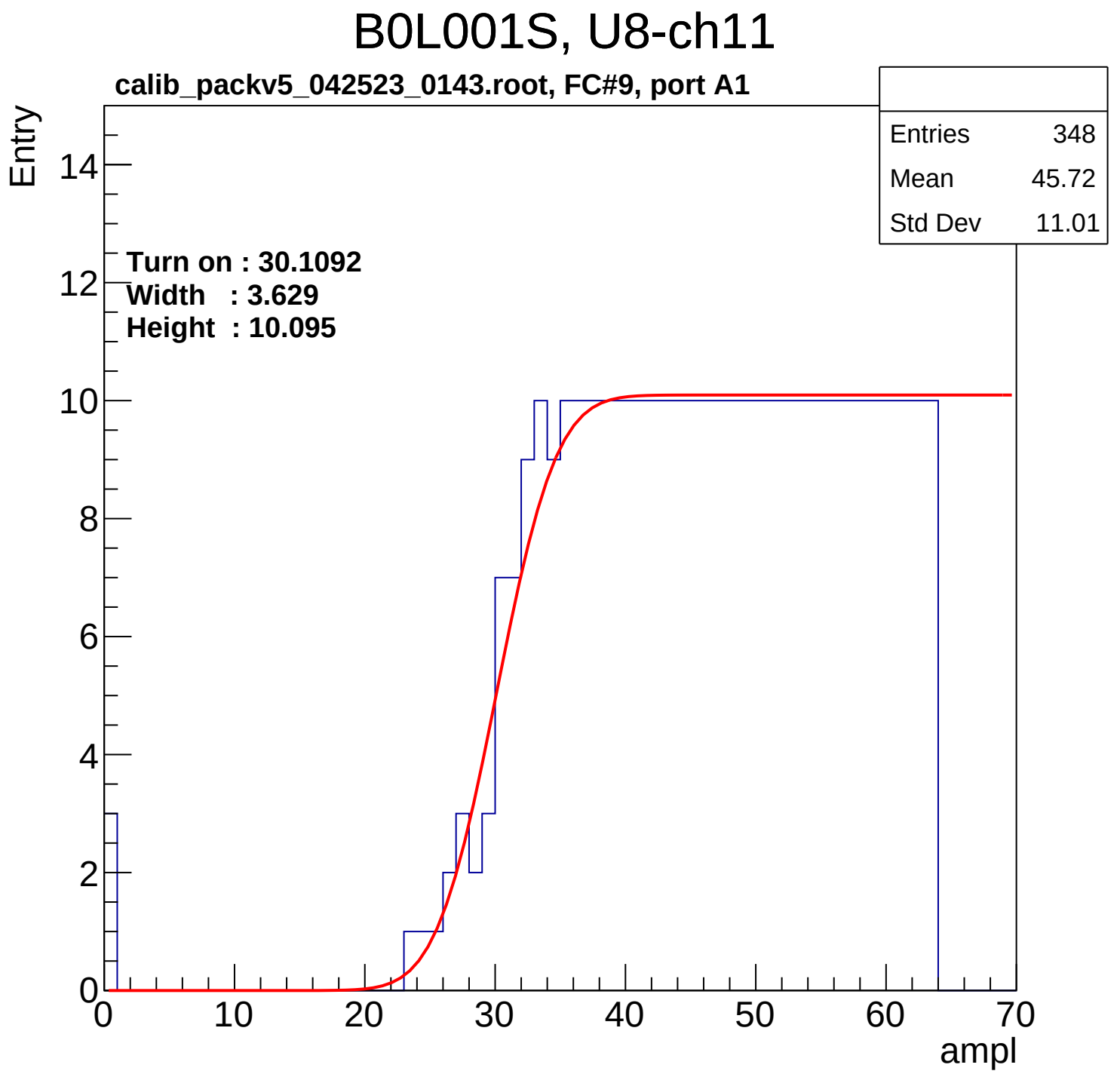
B0L001S, U8-ch11
calib_packv5_042523_0143.root, FC#9, port A1
Entries 348
Mean 45.72
Std Dev 11.01
Turn on : 30.1092
Width : 3.629
Height : 10.095
Entry
ampl
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2
4
6
8
10
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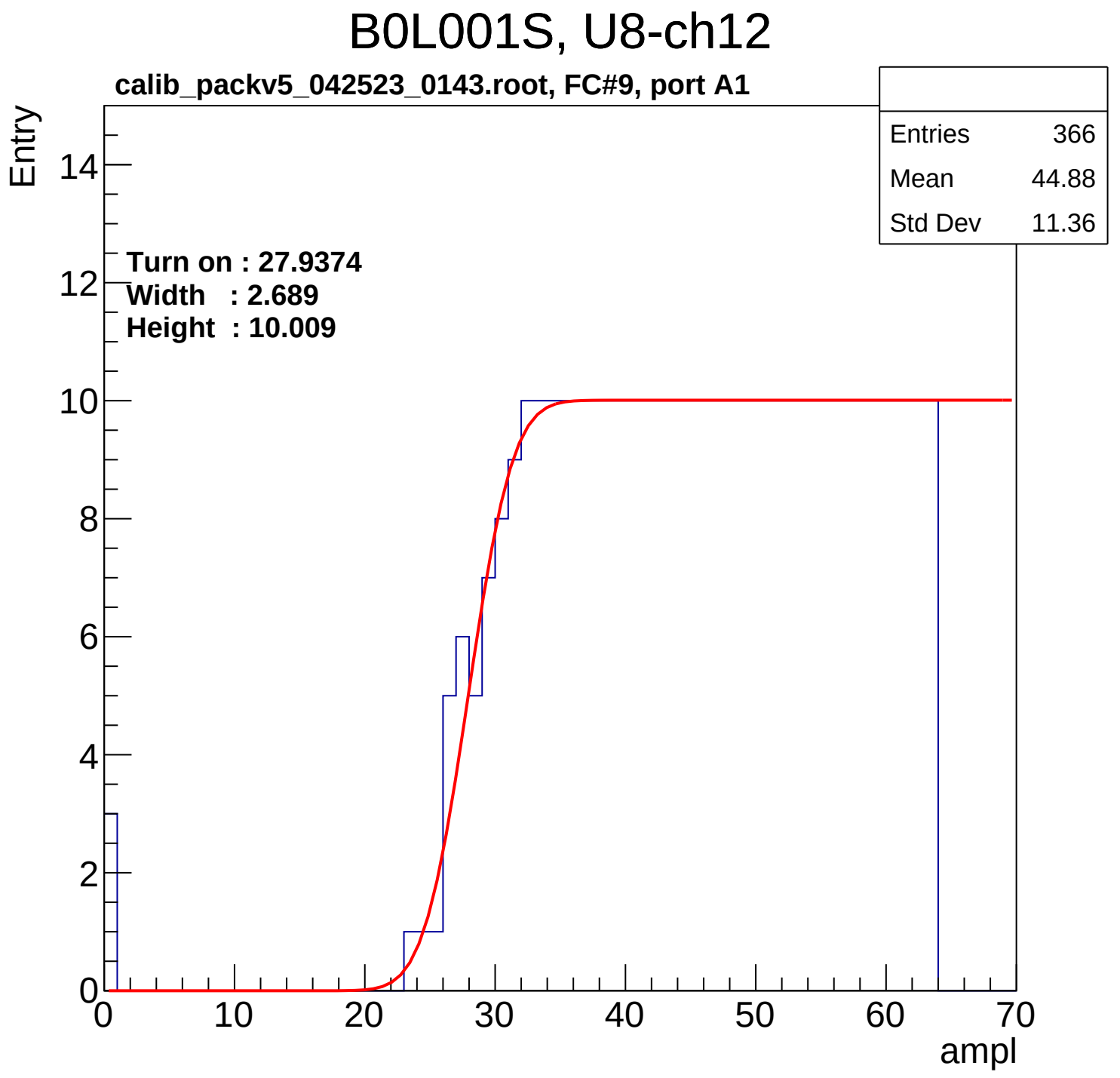
B0L001S, U8-ch12
calib_packv5_042523_0143.root, FC#9, port A1
Entries 366
Mean 44.88
Std Dev 11.36
Turn on : 27.9374
Width : 2.689
Height : 10.009
Entry
ampl
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2
4
6
8
10
12
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20
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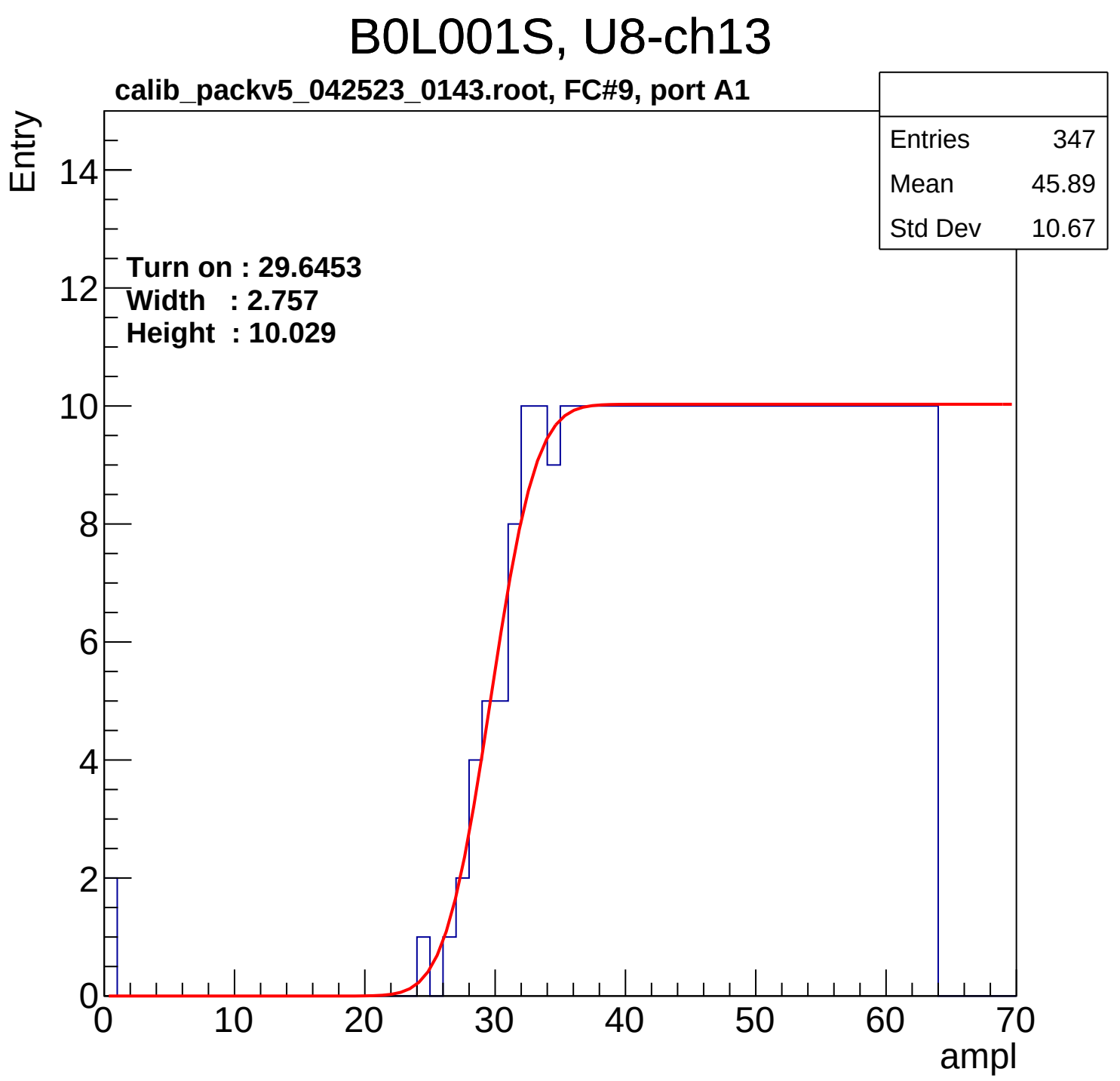
B0L001S, U8-ch13
calib_packv5_042523_0143.root, FC#9, port A1
Entries 347
Mean 45.89
Std Dev 10.67
Turn on : 29.6453
Width : 2.757
Height : 10.029
Entry
ampl
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2
4
6
8
10
12
14
0
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20
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60
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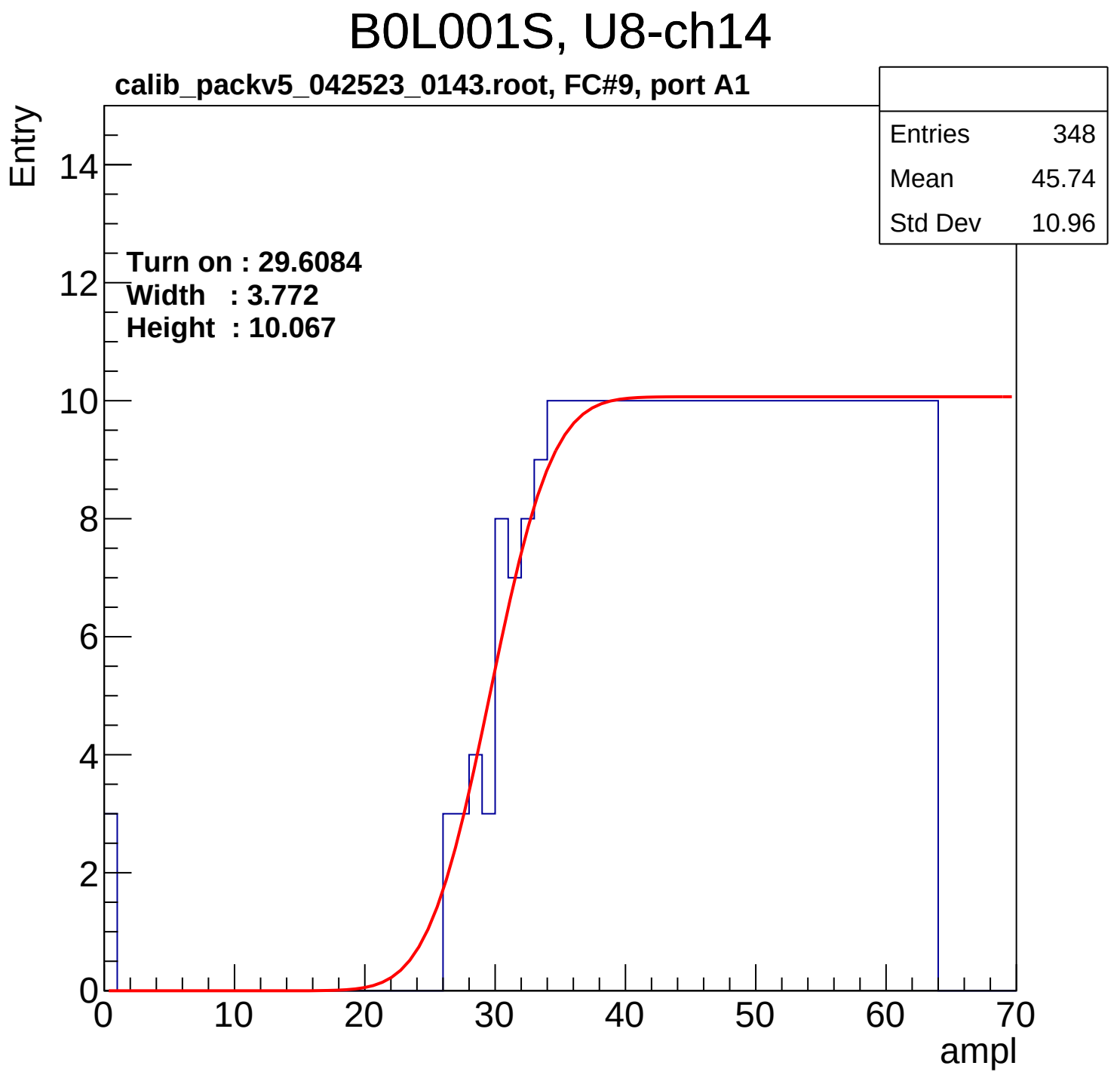
B0L001S, U8-ch14
calib_packv5_042523_0143.root, FC#9, port A1
Entries 348
Mean 45.74
Std Dev 10.96
Turn on : 29.6084
Width : 3.772
Height : 10.067
Entry
ampl
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6
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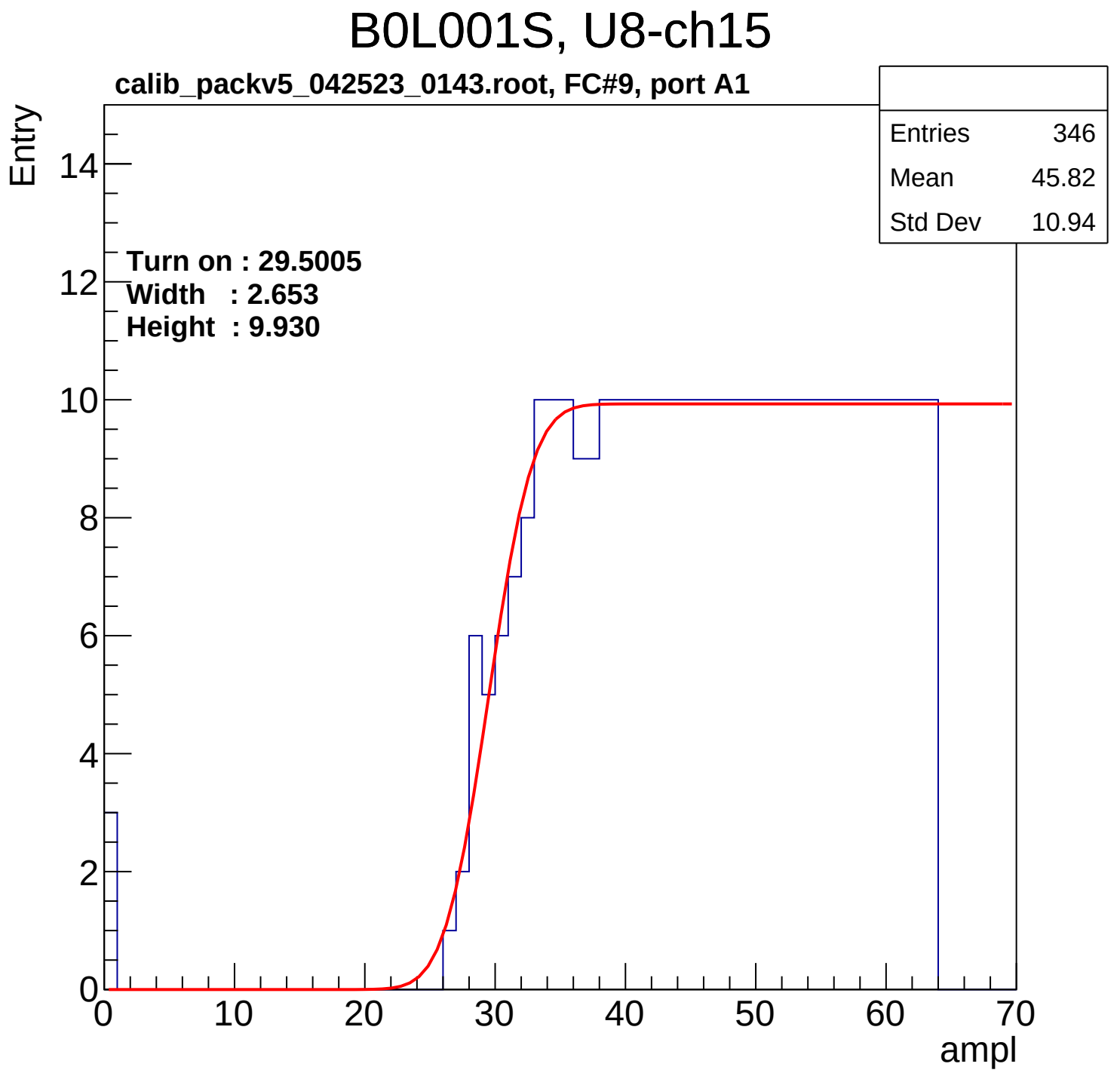
B0L001S, U8-ch15
calib_packv5_042523_0143.root, FC#9, port A1
Entries 346
Mean 45.82
Std Dev 10.94
Turn on : 29.5005
Width : 2.653
Height : 9.930
Entry
ampl
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2
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6
8
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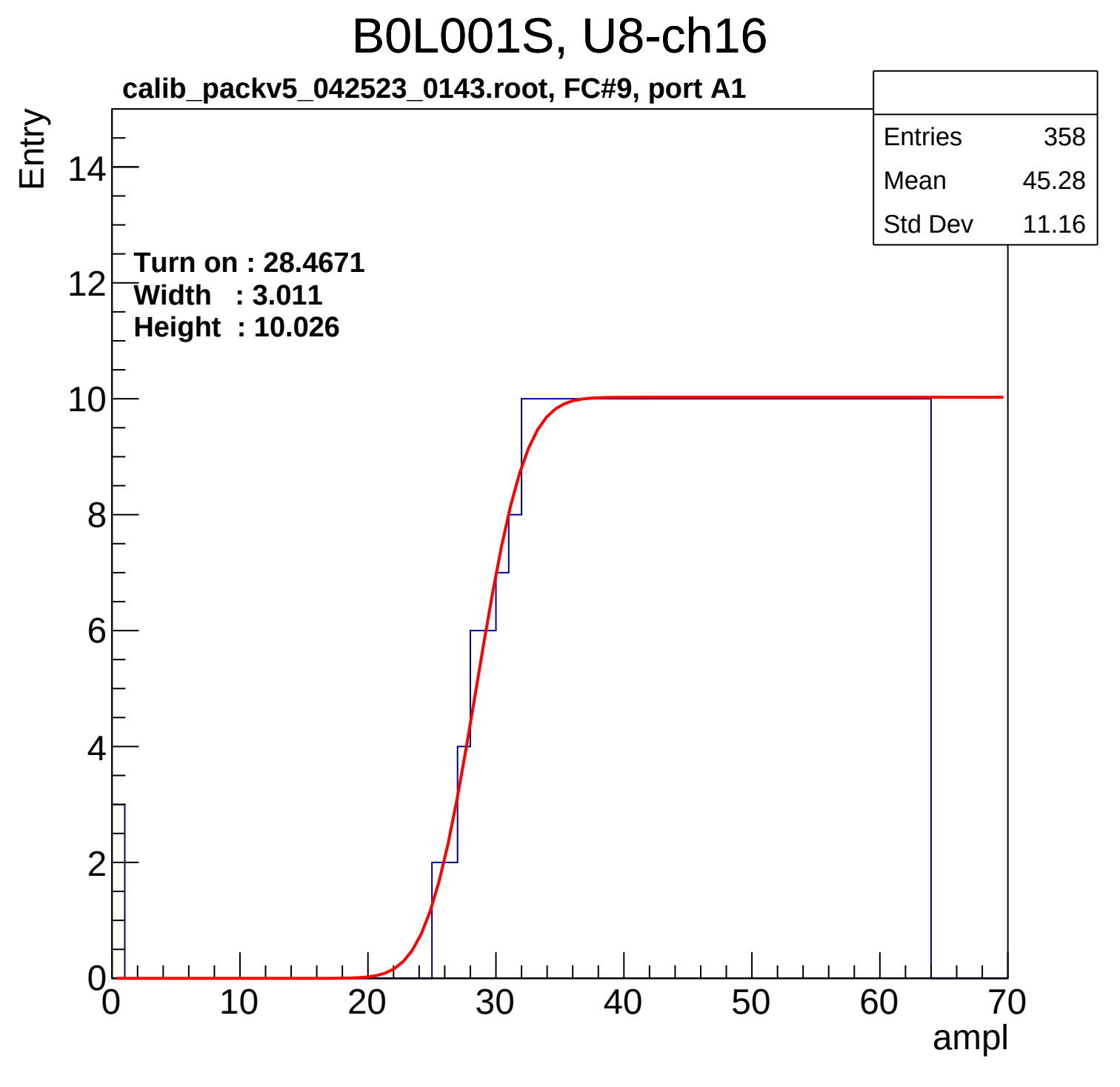
B0L001S, U8-ch16
calib_packv5_042523_0143.root, FC#9, port A1
Entries 358
Mean 45.28
Std Dev 11.16
Turn on : 28.4671
Width : 3.011
Height : 10.026
Entry
ampl
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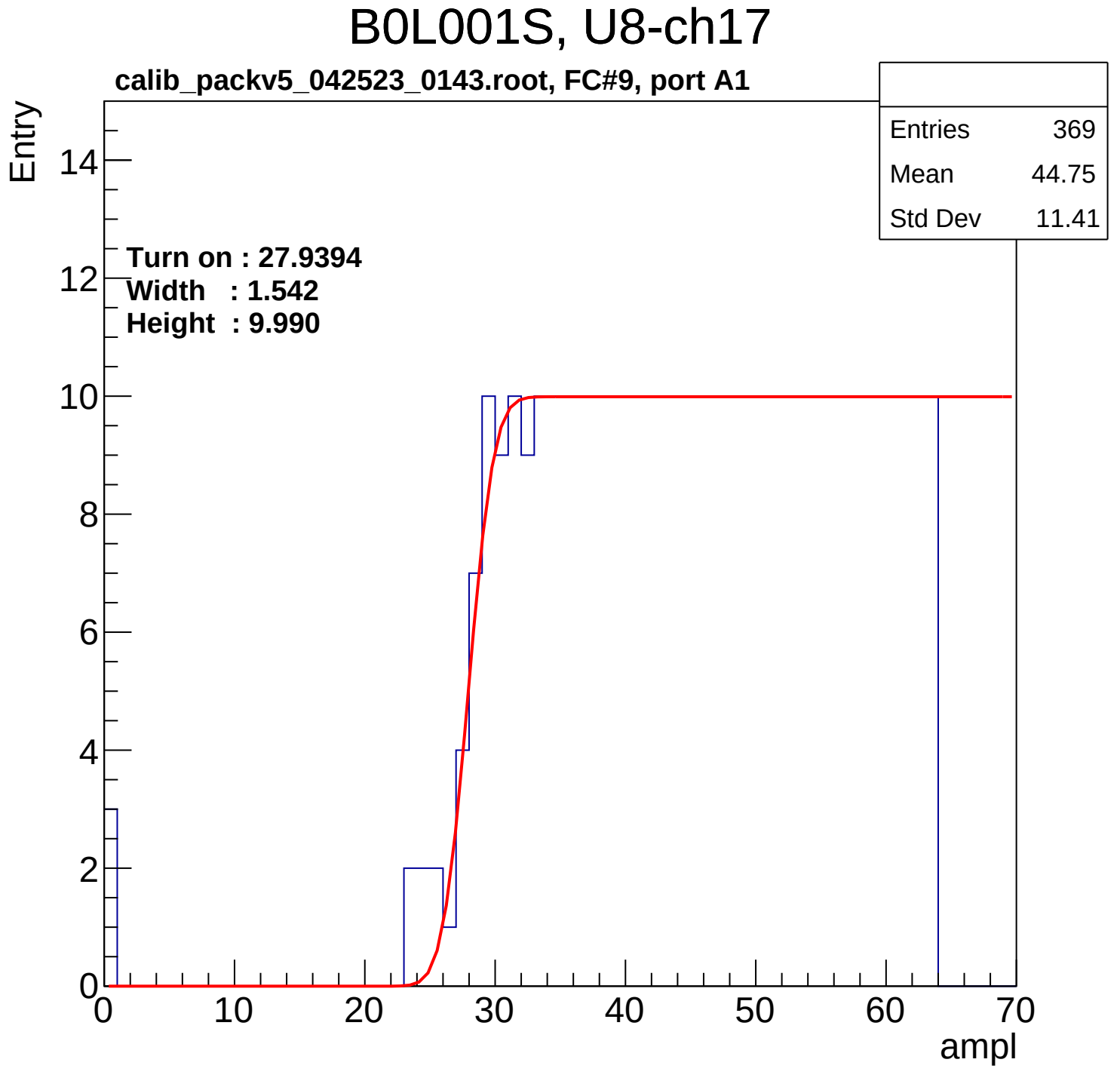
B0L001S, U8-ch17
calib_packv5_042523_0143.root, FC#9, port A1
Entries 369
Mean 44.75
Std Dev 11.41
Turn on : 27.9394
Width : 1.542
Height : 9.990
Entry
ampl
0
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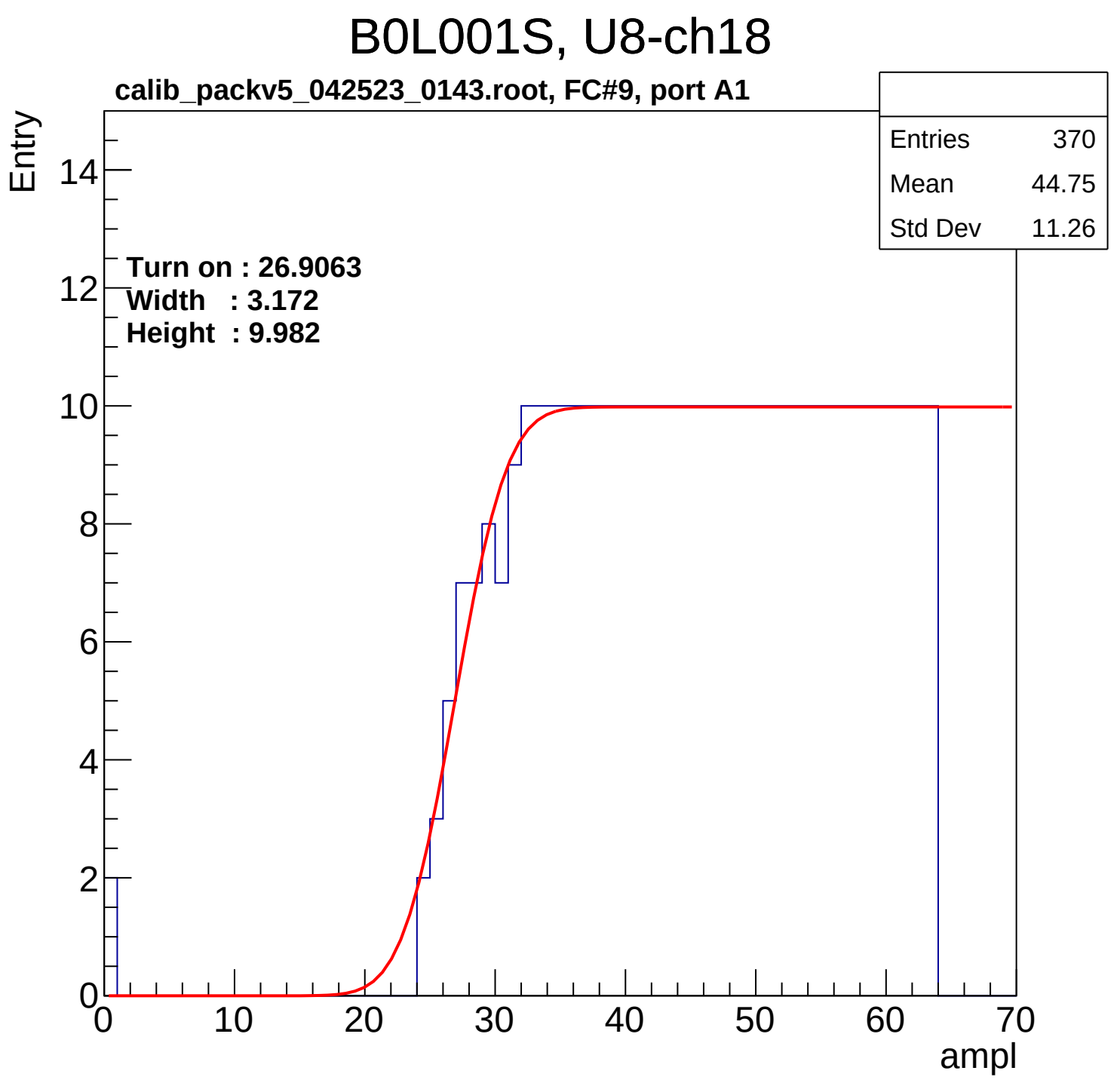
B0L001S, U8-ch18
calib_packv5_042523_0143.root, FC#9, port A1
Entries 370
Mean 44.75
Std Dev 11.26
Turn on : 26.9063
Width : 3.172
Height : 9.982
Entry
ampl
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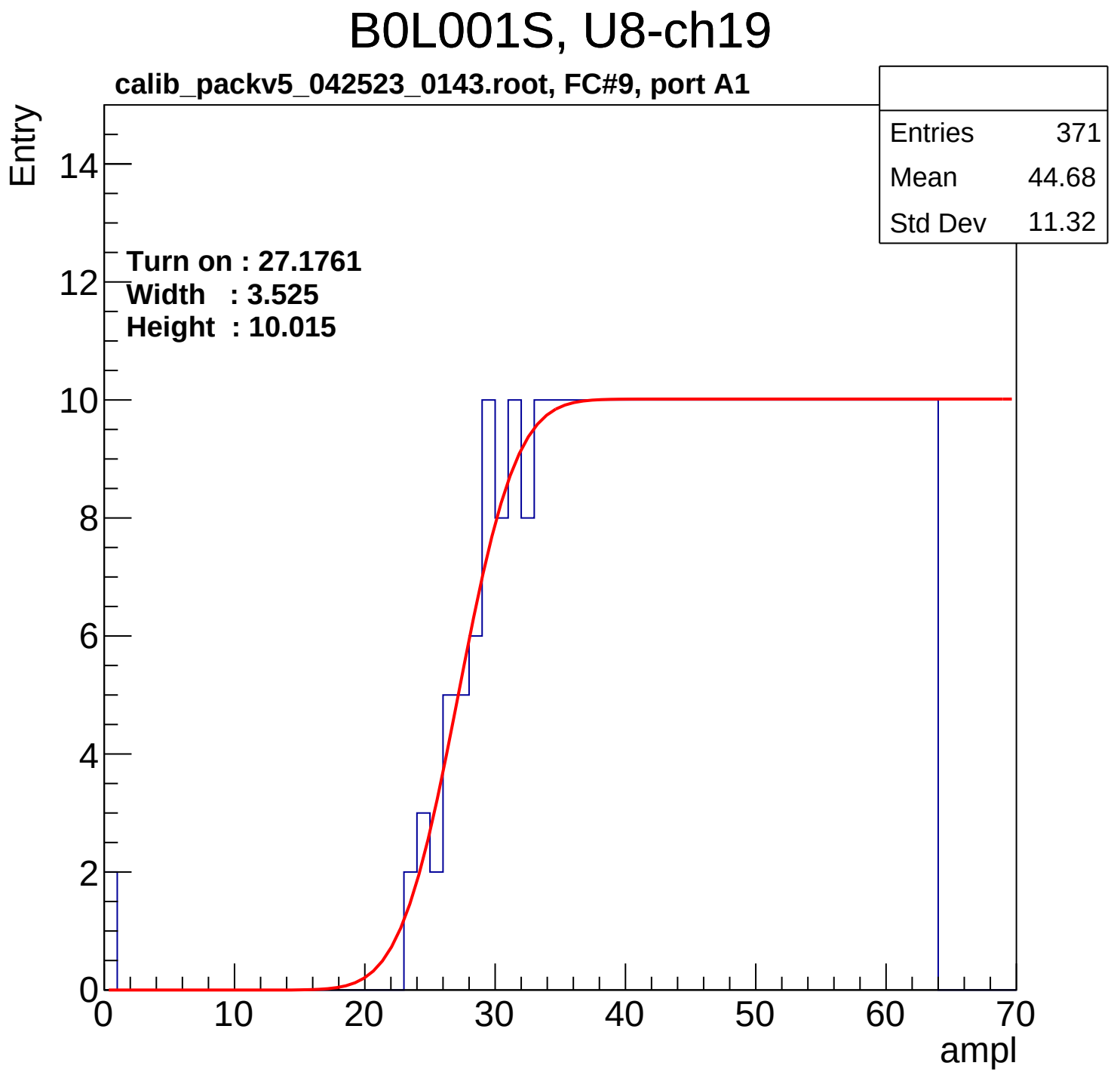
B0L001S, U8-ch19
calib_packv5_042523_0143.root, FC#9, port A1
Entries 371
Mean 44.68
Std Dev 11.32
Turn on : 27.1761
Width : 3.525
Height : 10.015
Entry
ampl
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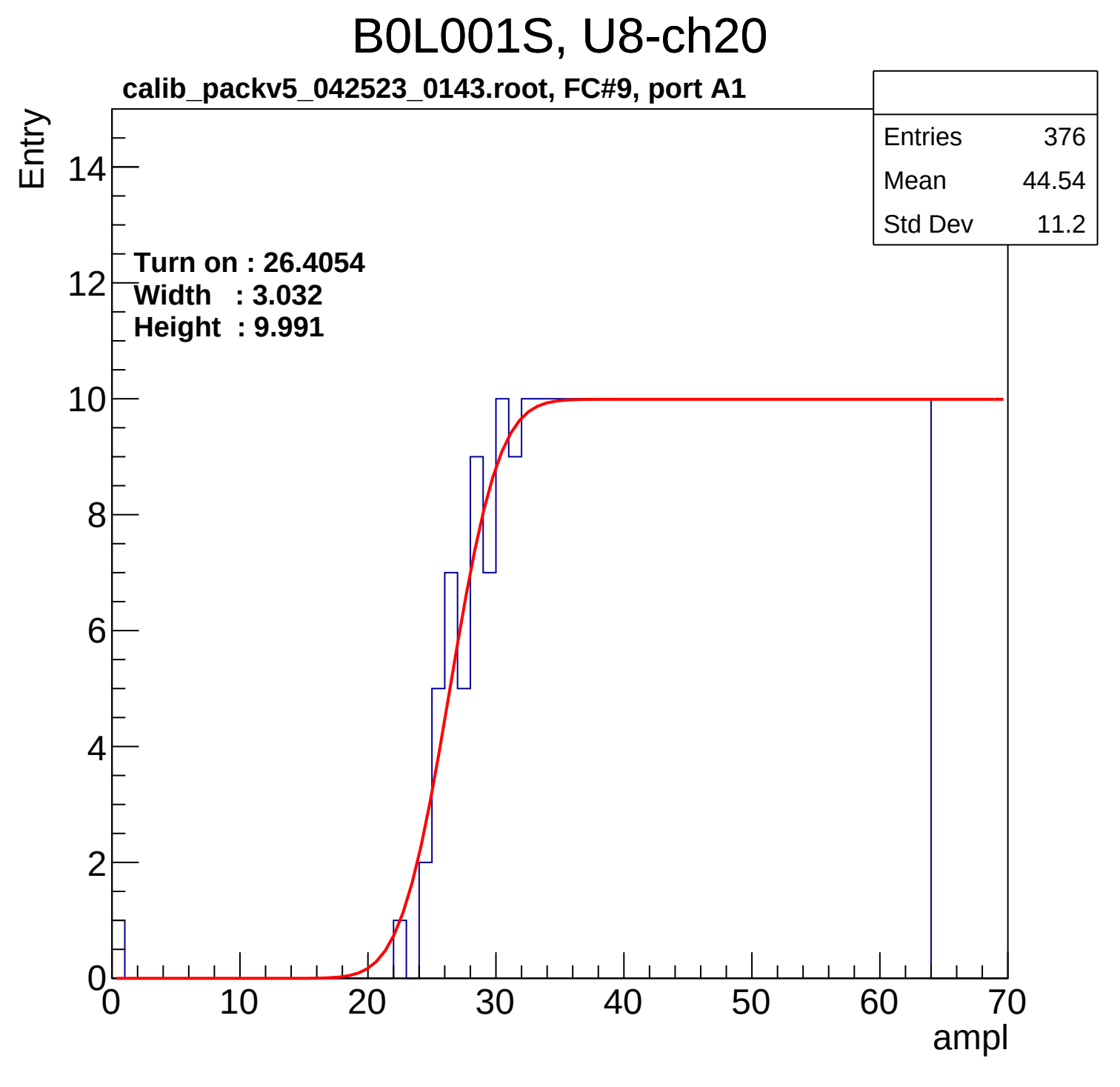
B0L001S, U8-ch20
calib_packv5_042523_0143.root, FC#9, port A1
Entries 376
Mean 44.54
Std Dev 11.2
Turn on : 26.4054
Width : 3.032
Height : 9.991
Entry
ampl
0
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4
6
8
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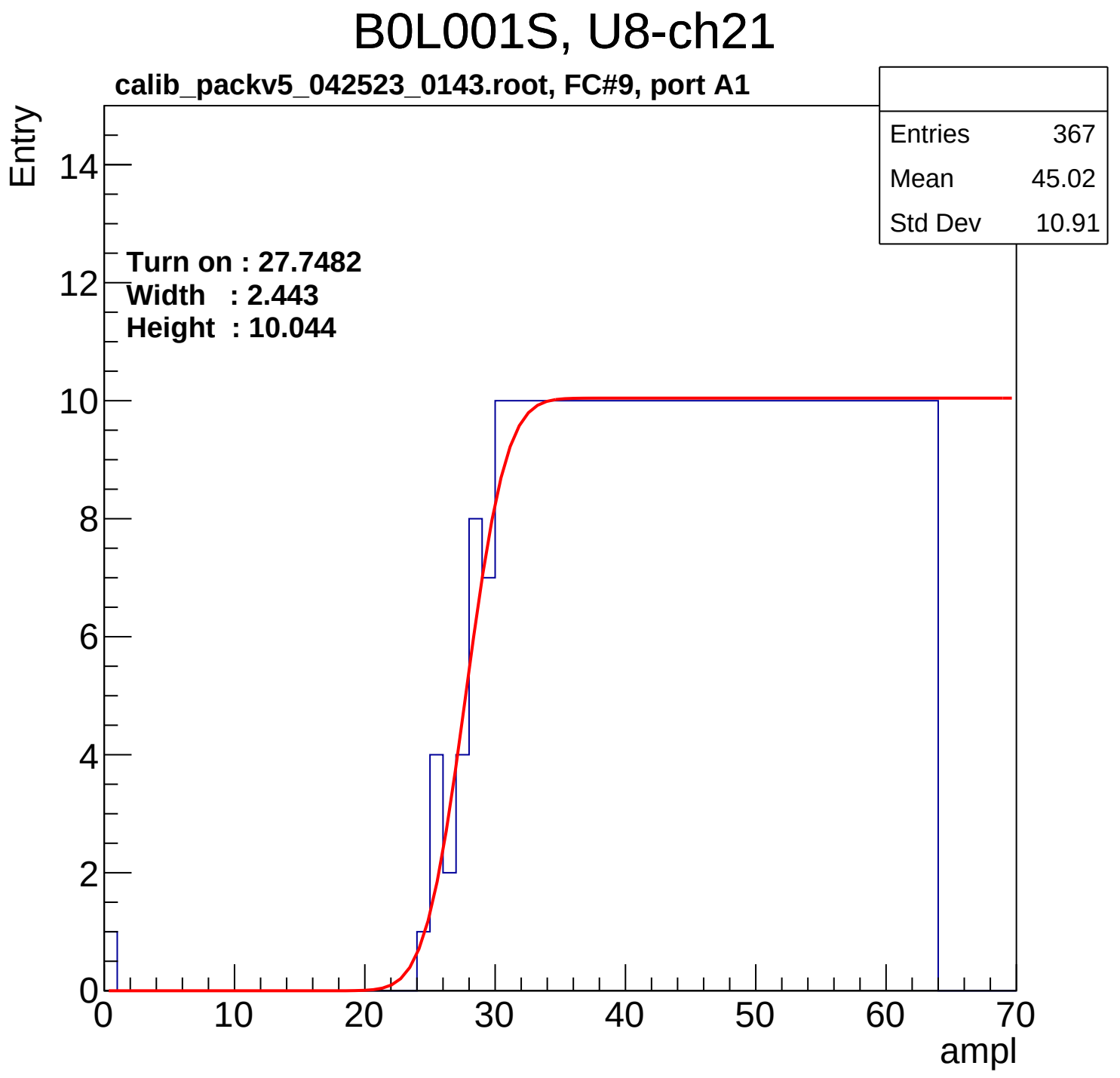
B0L001S, U8-ch21
calib_packv5_042523_0143.root, FC#9, port A1
Entries 367
Mean 45.02
Std Dev 10.91
Turn on : 27.7482
Width : 2.443
Height : 10.044
Entry
ampl
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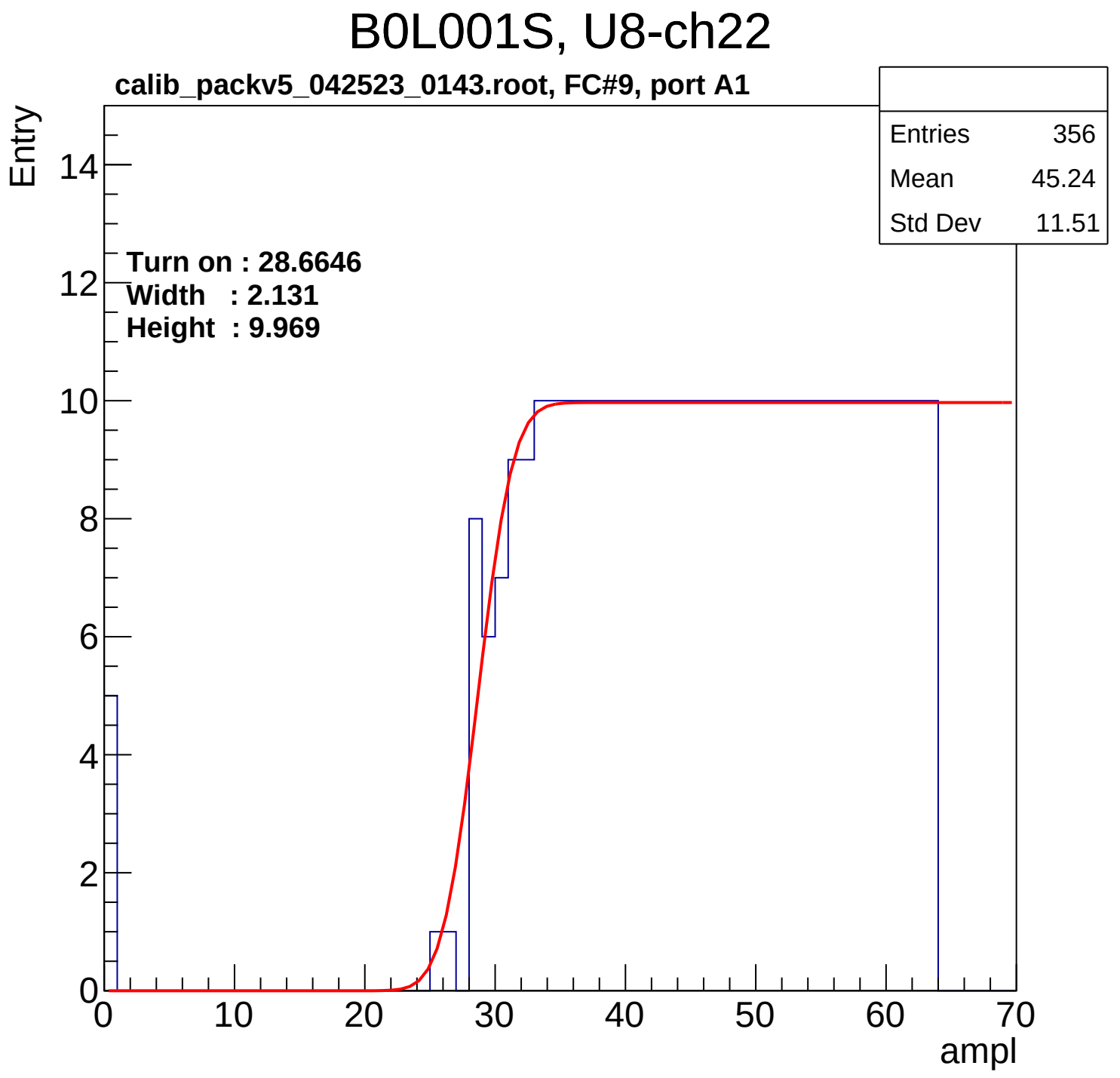
B0L001S, U8-ch22
calib_packv5_042523_0143.root, FC#9, port A1
Entries 356
Mean 45.24
Std Dev 11.51
Turn on : 28.6646
Width : 2.131
Height : 9.969
Entry
ampl
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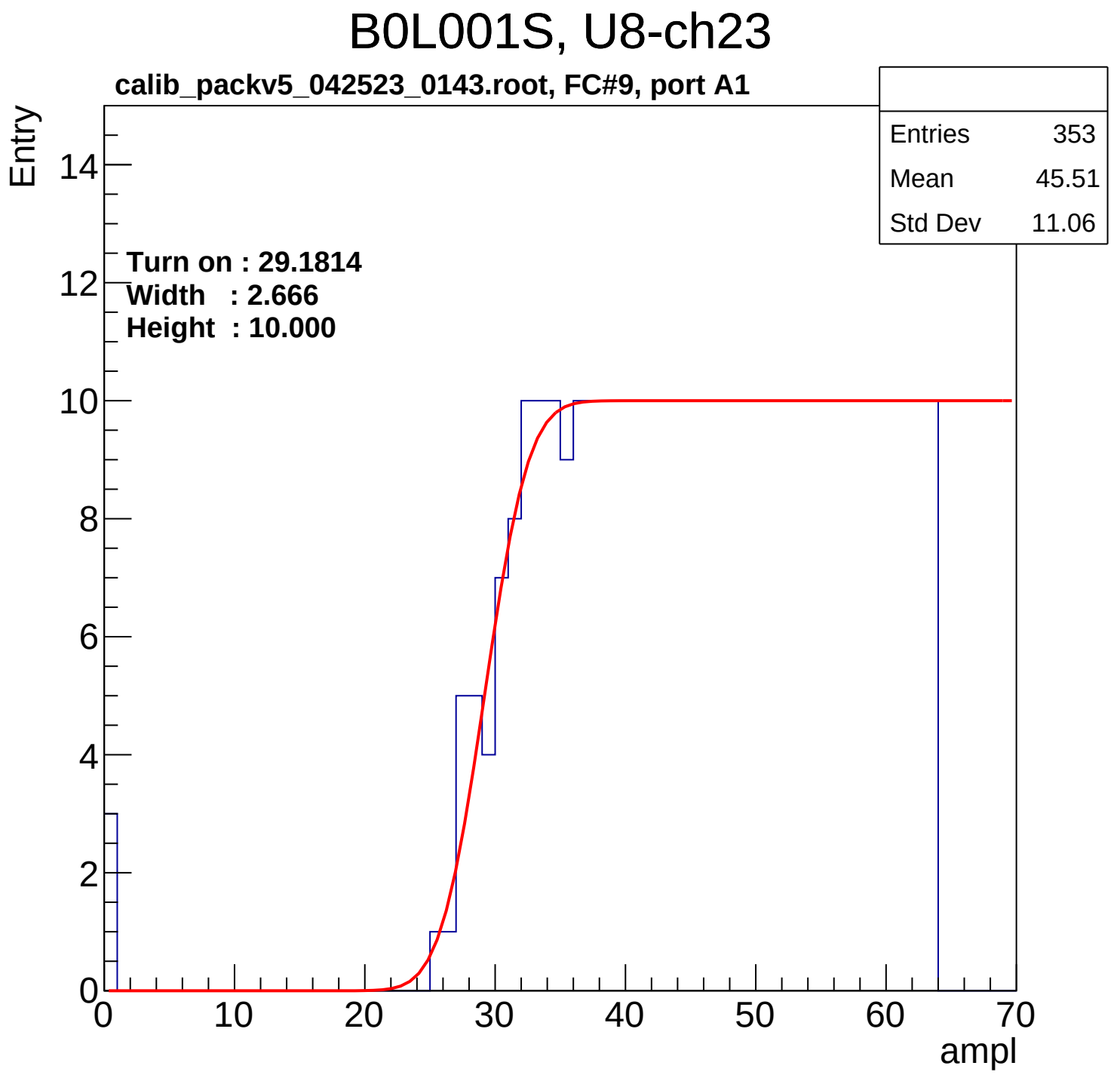
B0L001S, U8-ch23
calib_packv5_042523_0143.root, FC#9, port A1
Entries 353
Mean 45.51
Std Dev 11.06
Turn on : 29.1814
Width : 2.666
Height : 10.000
Entry
ampl
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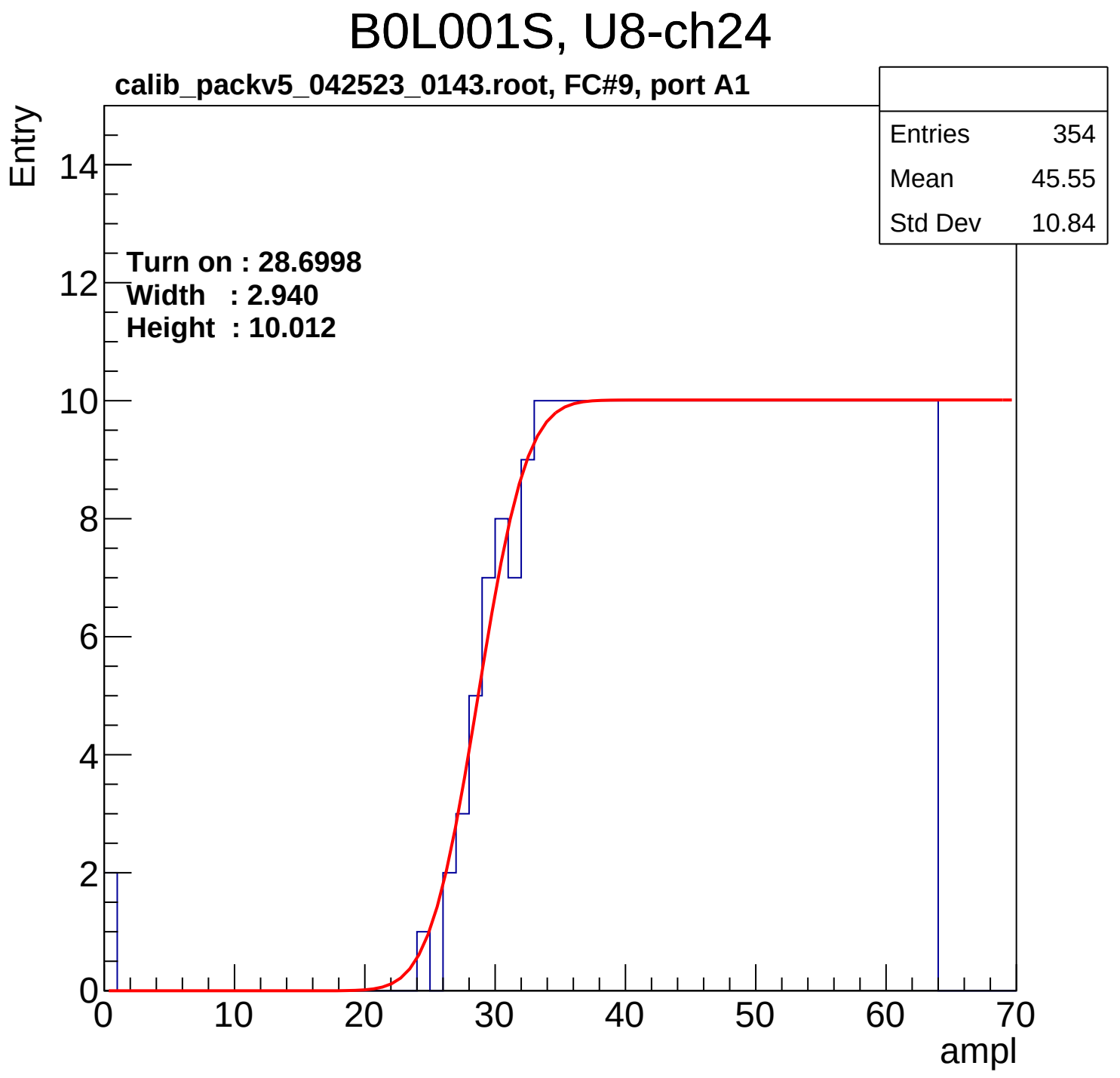
B0L001S, U8-ch24
calib_packv5_042523_0143.root, FC#9, port A1
Entries 354
Mean 45.55
Std Dev 10.84
Turn on : 28.6998
Width : 2.940
Height : 10.012
Entry
ampl
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6
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10
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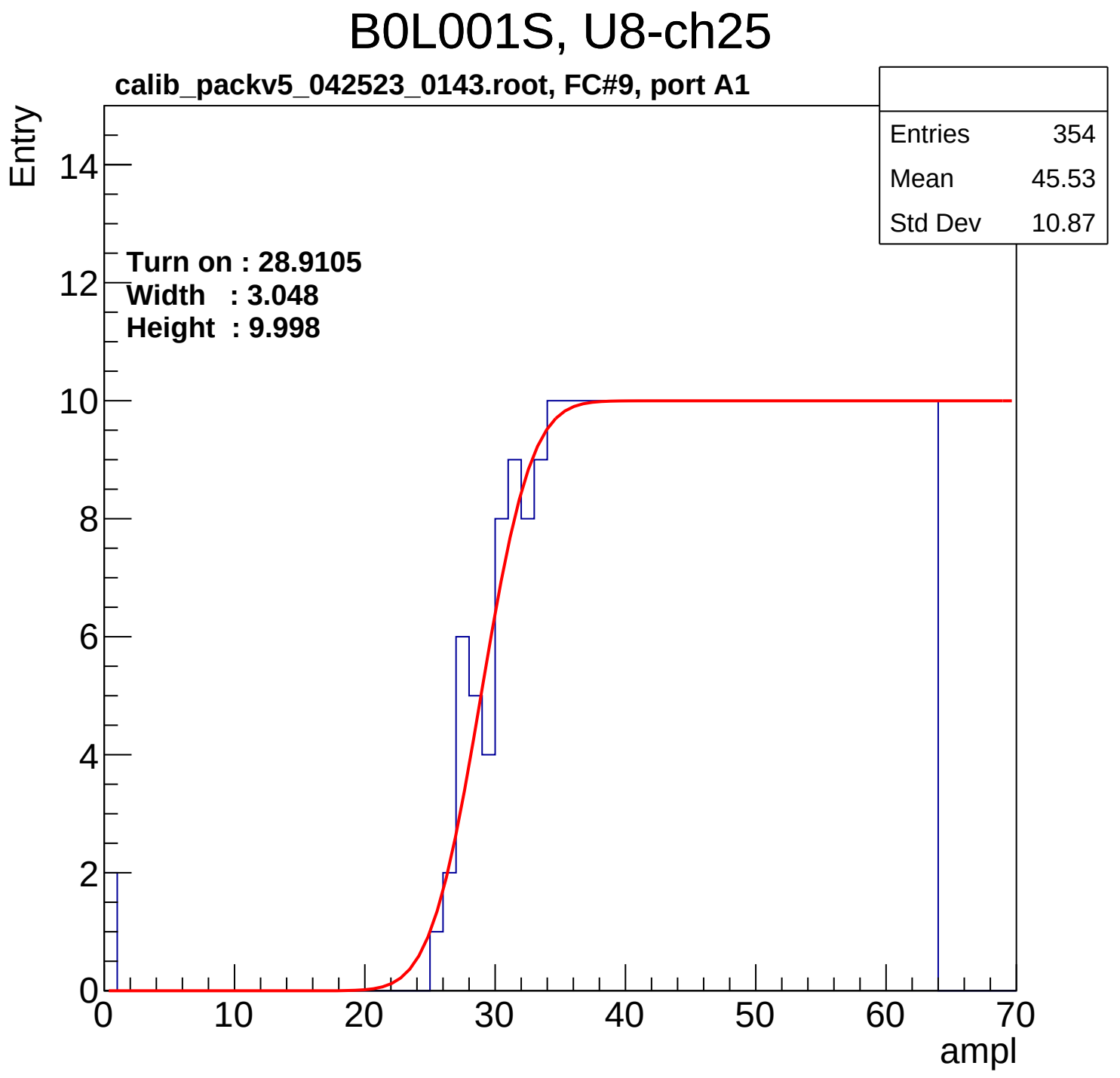
B0L001S, U8-ch25
calib_packv5_042523_0143.root, FC#9, port A1
Entries 354
Mean 45.53
Std Dev 10.87
Turn on : 28.9105
Width : 3.048
Height : 9.998
Entry
ampl
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6
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0
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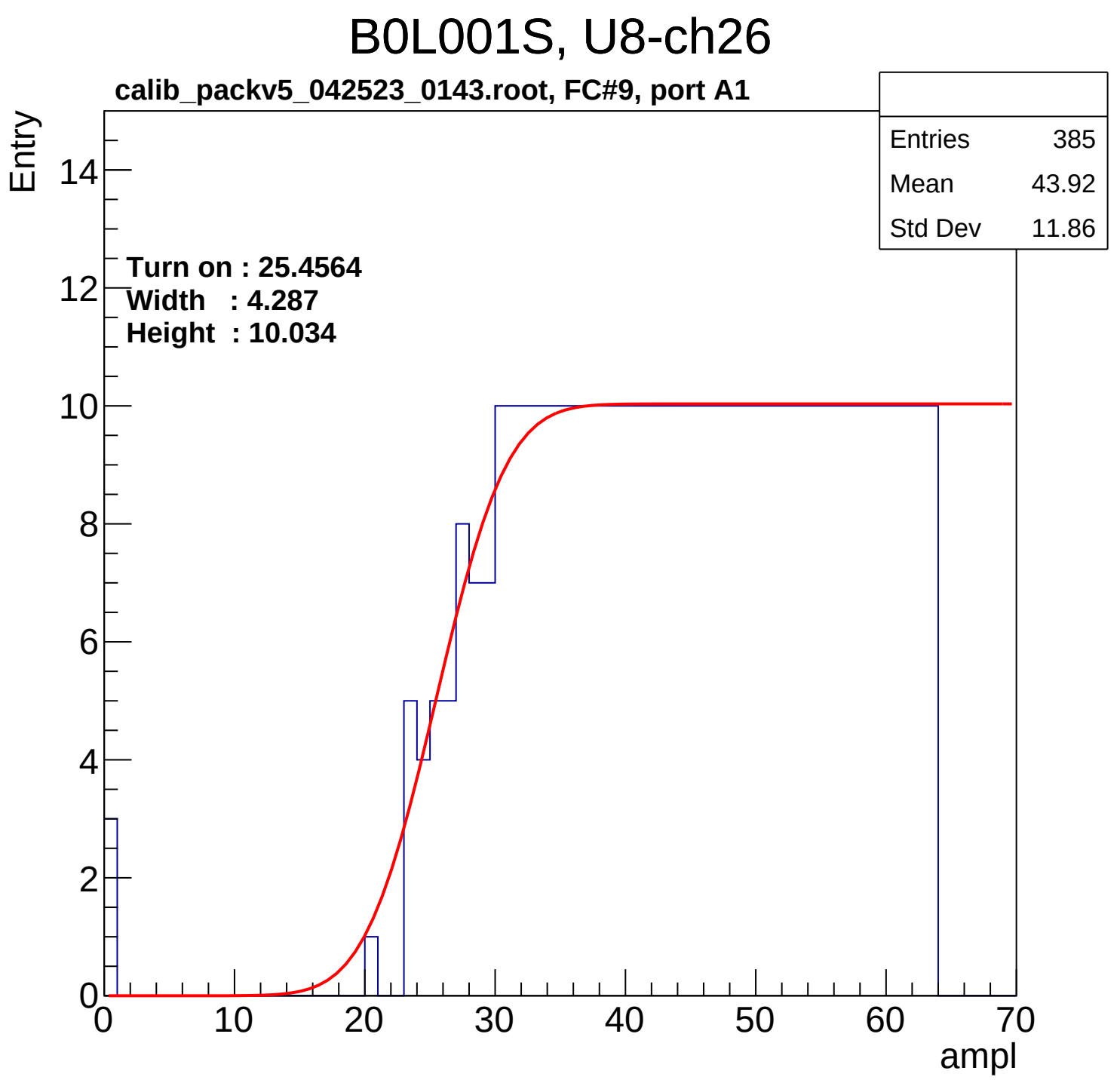
B0L001S, U8-ch26
calib_packv5_042523_0143.root, FC#9, port A1
Entries 385
Mean 43.92
Std Dev 11.86
Turn on : 25.4564
Width : 4.287
Height : 10.034
Entry
ampl
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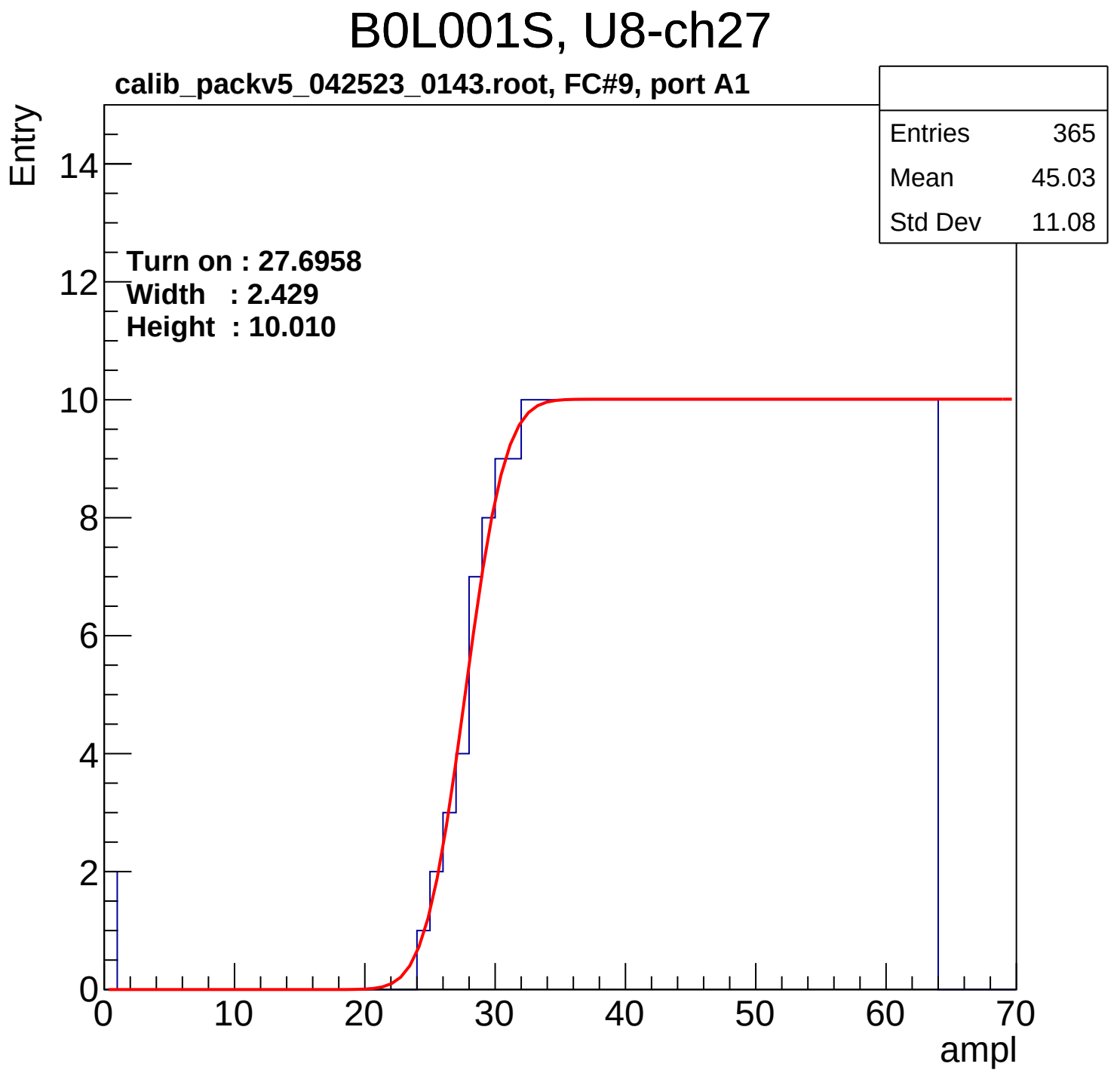
B0L001S, U8-ch27
calib_packv5_042523_0143.root, FC#9, port A1
Entries 365
Mean 45.03
Std Dev 11.08
Turn on : 27.6958
Width : 2.429
Height : 10.010
Entry
ampl
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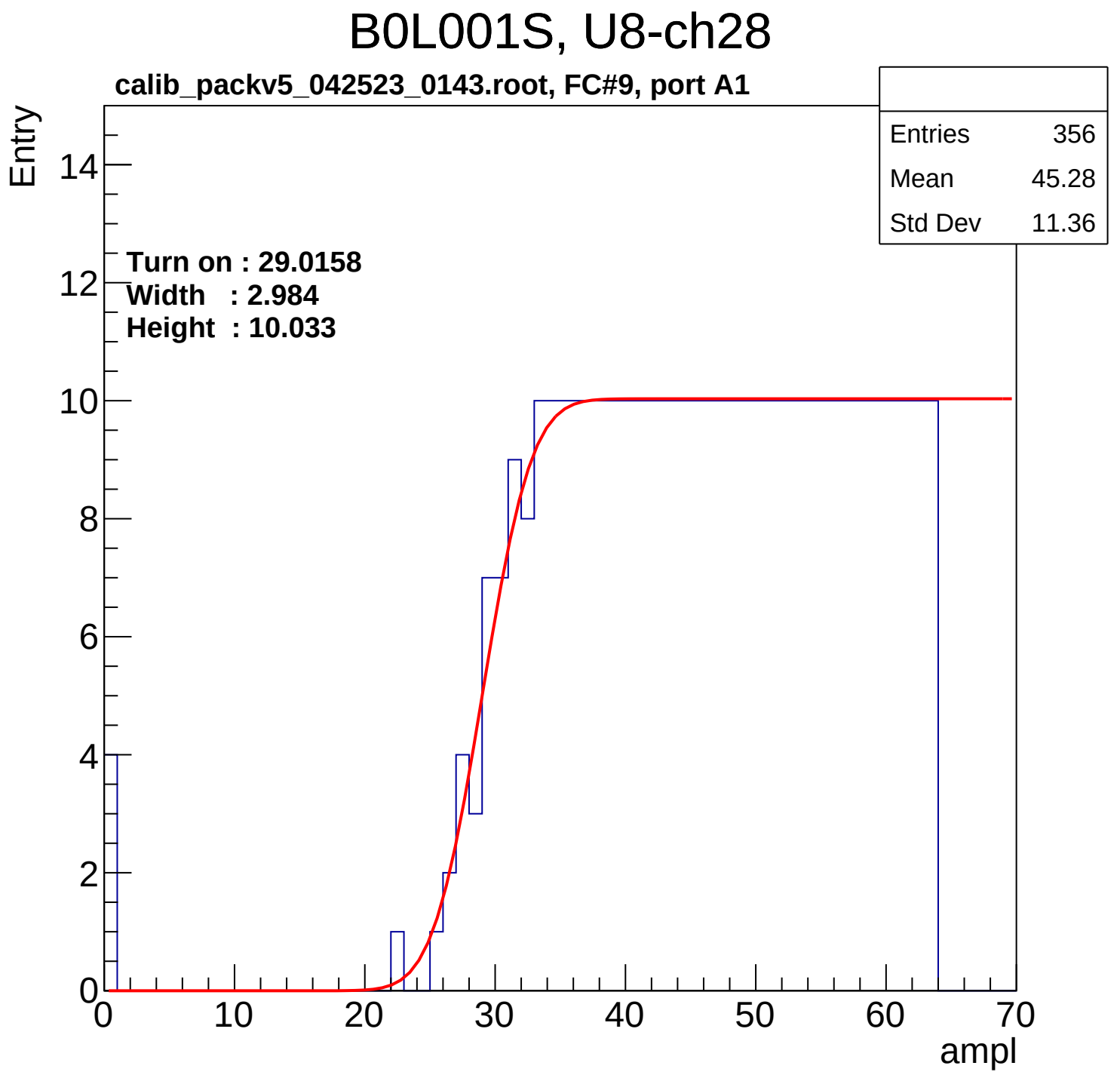
B0L001S, U8-ch28
calib_packv5_042523_0143.root, FC#9, port A1
Entries 356
Mean 45.28
Std Dev 11.36
Turn on : 29.0158
Width : 2.984
Height : 10.033
Entry
ampl
0
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4
6
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12
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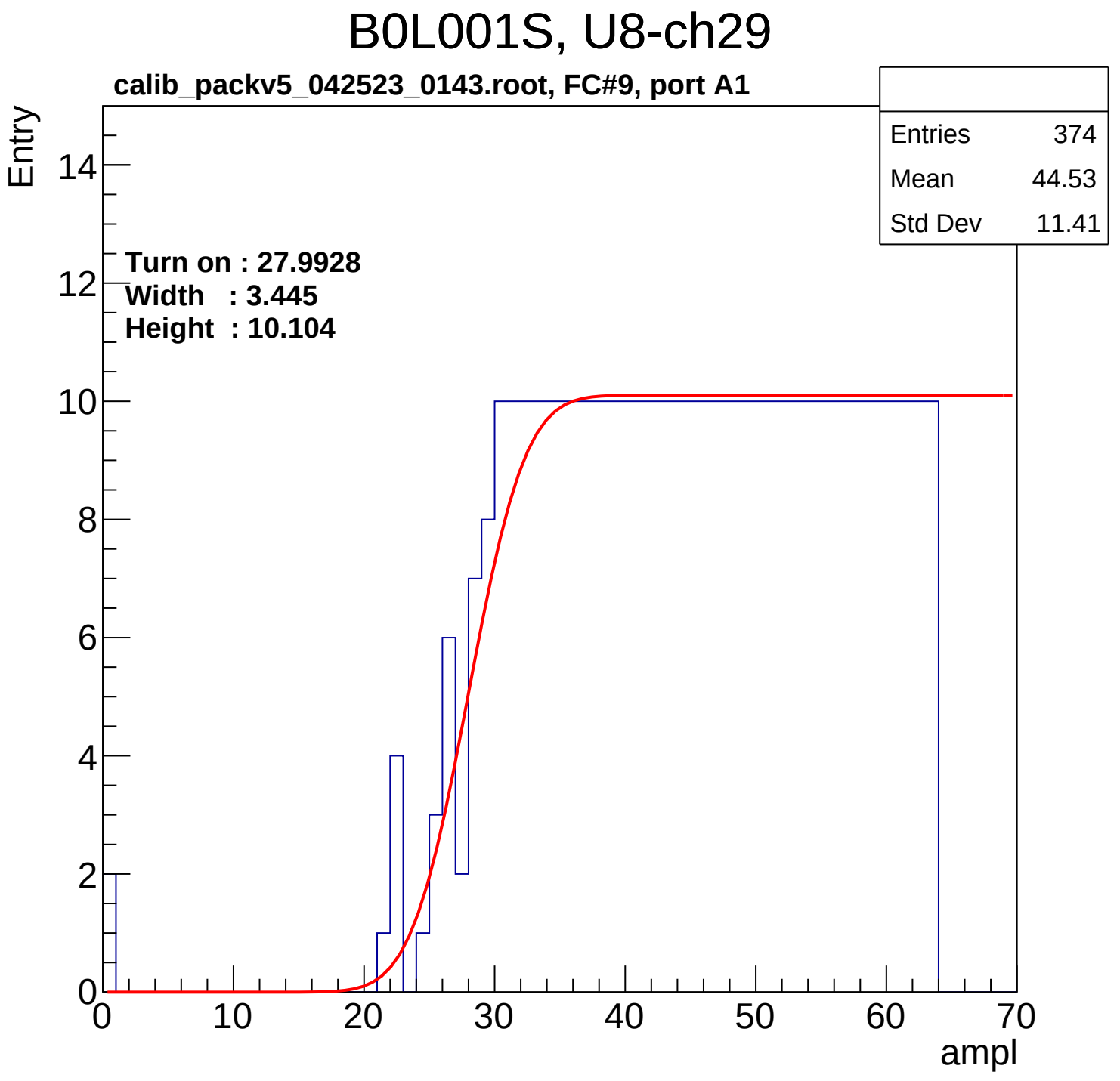
B0L001S, U8-ch29
calib_packv5_042523_0143.root, FC#9, port A1
Entries 374
Mean 44.53
Std Dev 11.41
Turn on : 27.9928
Width : 3.445
Height : 10.104
Entry
ampl
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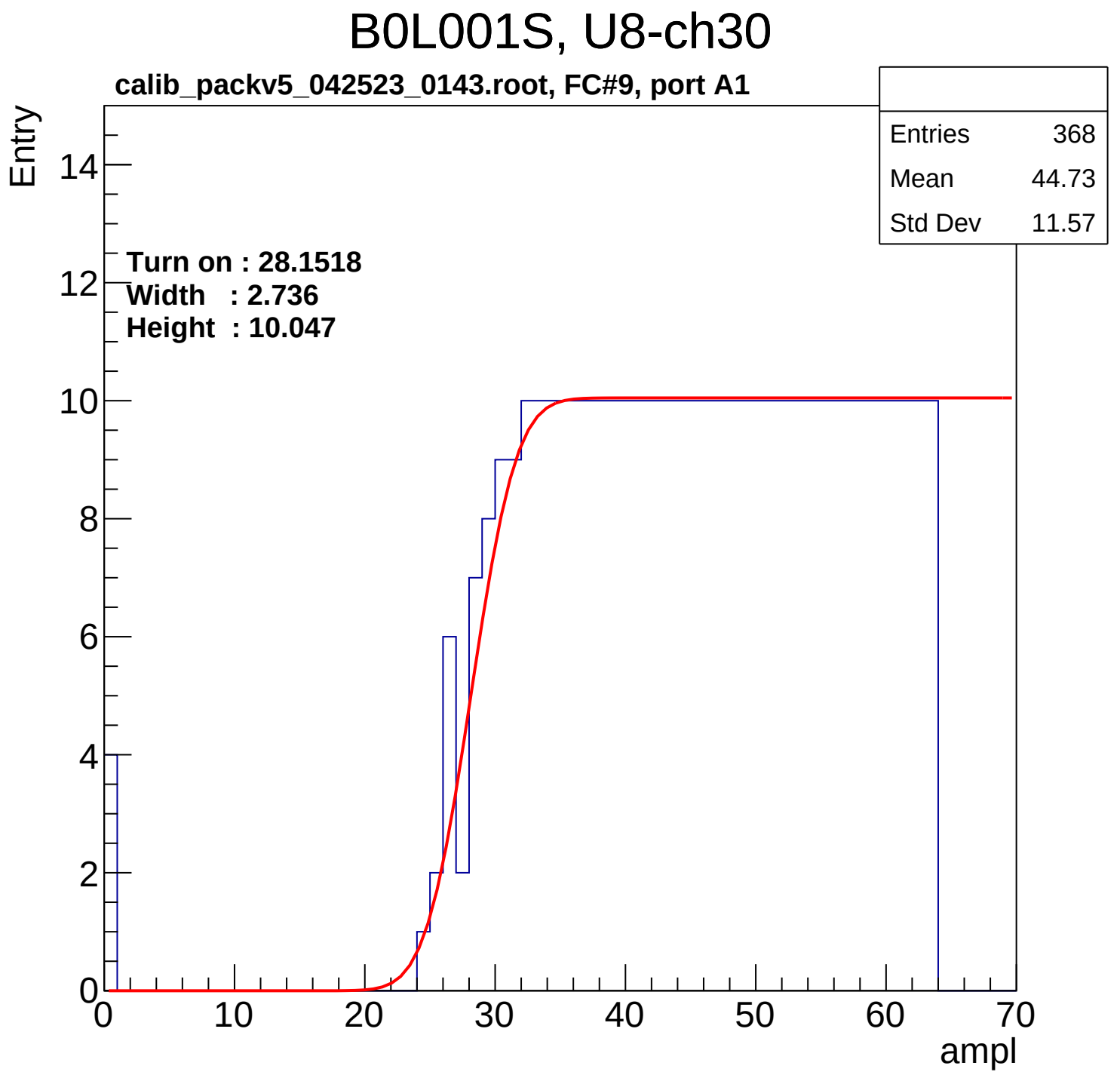
B0L001S, U8-ch30
calib_packv5_042523_0143.root, FC#9, port A1
Entries 368
Mean 44.73
Std Dev 11.57
Turn on : 28.1518
Width : 2.736
Height : 10.047
Entry
ampl
0
2
4
6
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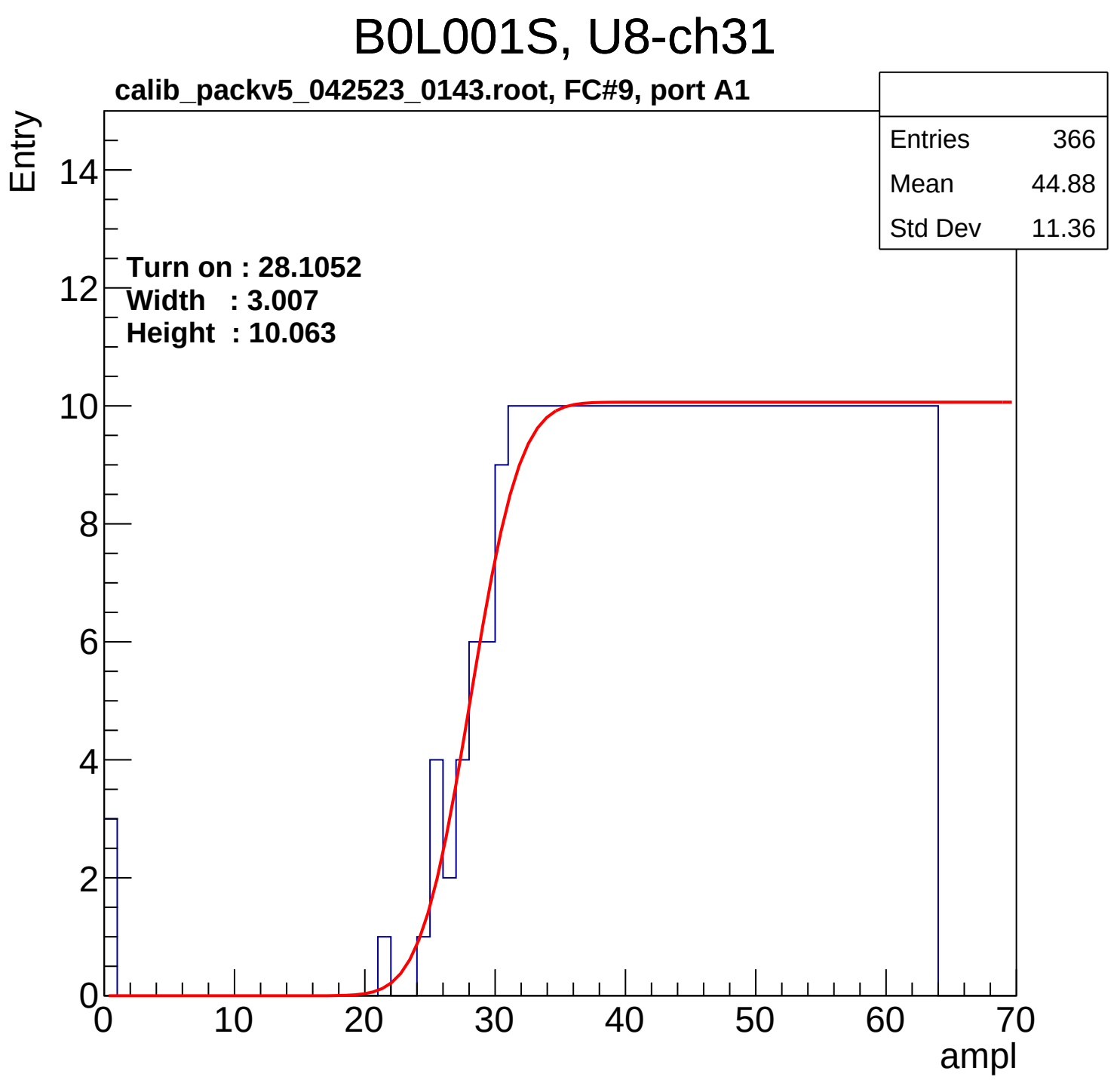
B0L001S, U8-ch31
calib_packv5_042523_0143.root, FC#9, port A1
Entries 366
Mean 44.88
Std Dev 11.36
Turn on : 28.1052
Width : 3.007
Height : 10.063
Entry
ampl
0
2
4
6
8
10
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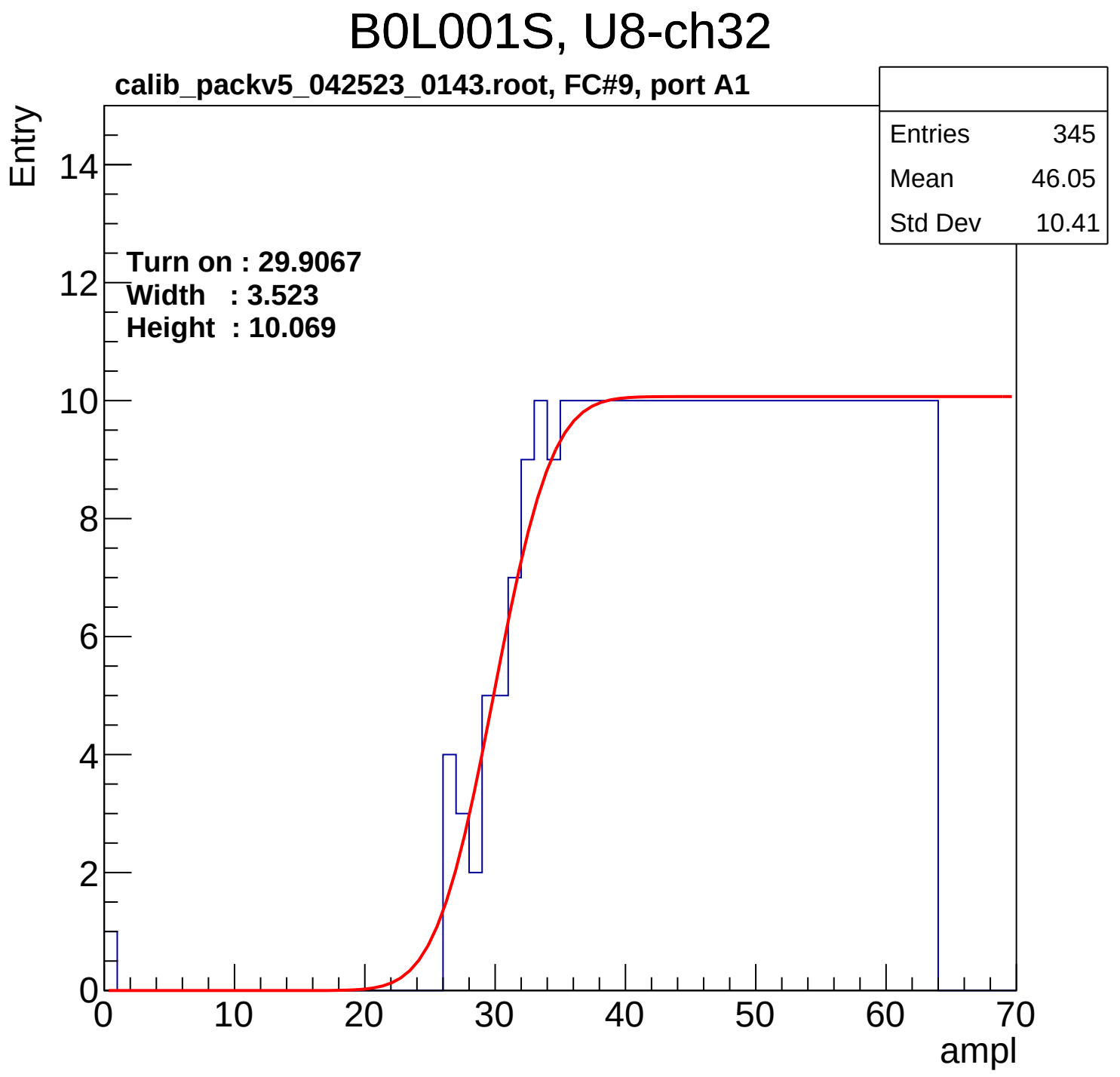
B0L001S, U8-ch32
calib_packv5_042523_0143.root, FC#9, port A1
Entries 345
Mean 46.05
Std Dev 10.41
Turn on : 29.9067
Width : 3.523
Height : 10.069
Entry
ampl
0
2
4
6
8
10
12
14
0
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20
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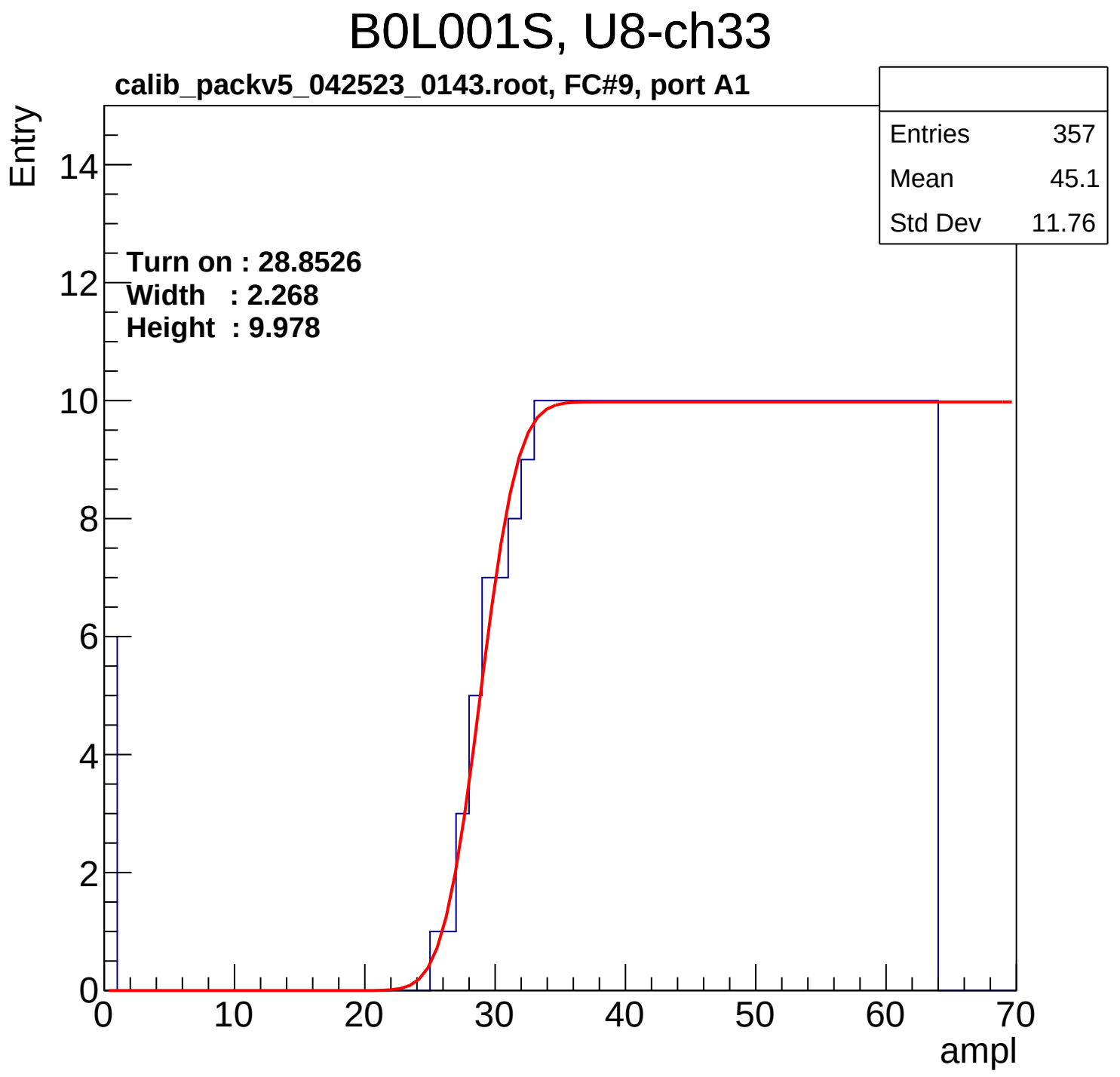
B0L001S, U8-ch33
calib_packv5_042523_0143.root, FC#9, port A1
Entries 357
Mean 45.1
Std Dev 11.76
Turn on : 28.8526
Width : 2.268
Height : 9.978
Entry
ampl
0
2
4
6
8
10
12
14
0
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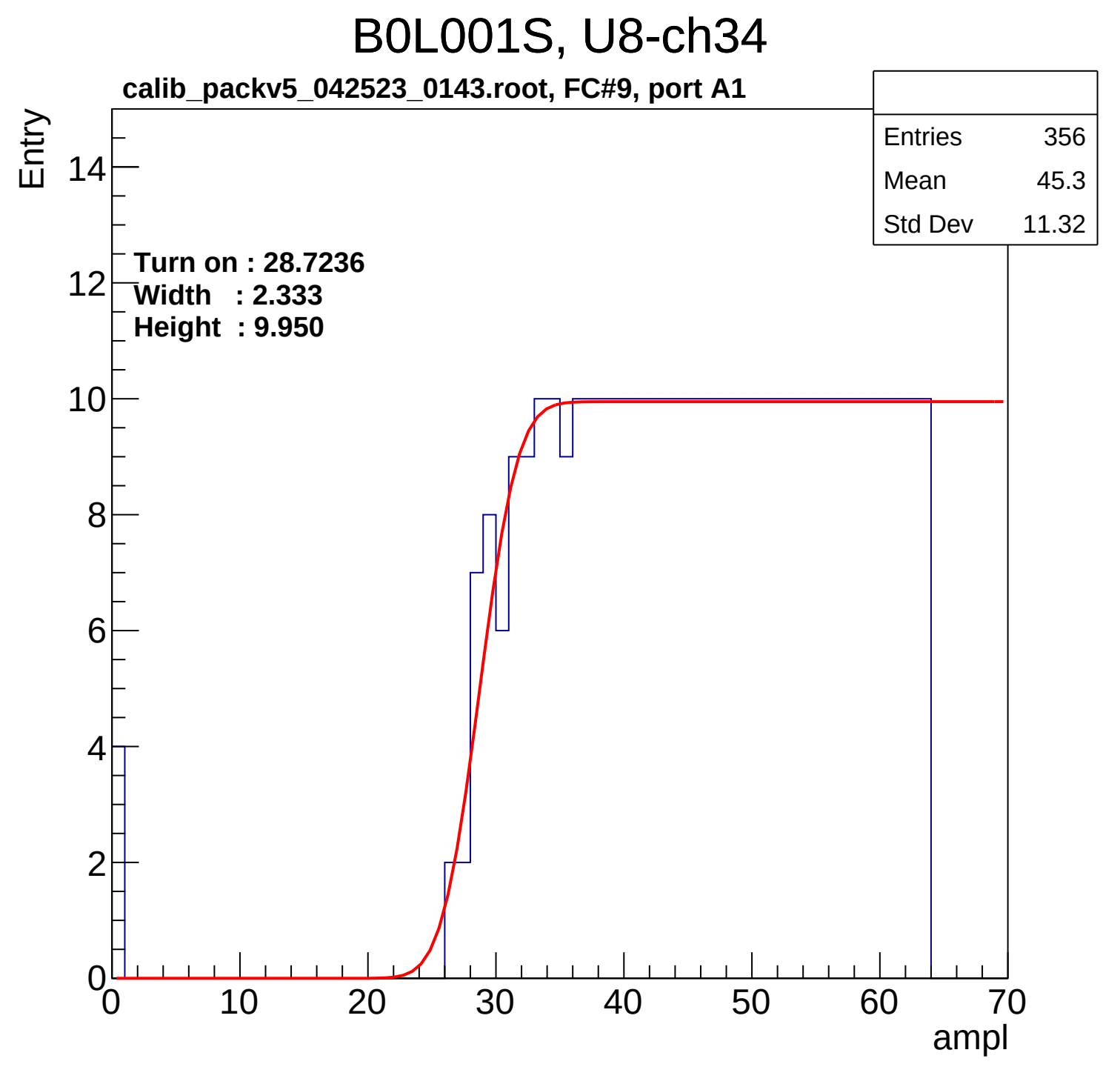
B0L001S, U8-ch34
calib_packv5_042523_0143.root, FC#9, port A1
Entries 356
Mean 45.3
Std Dev 11.32
Turn on : 28.7236
Width : 2.333
Height : 9.950
Entry
ampl
0
2
4
6
8
10
12
14
0
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20
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40
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60
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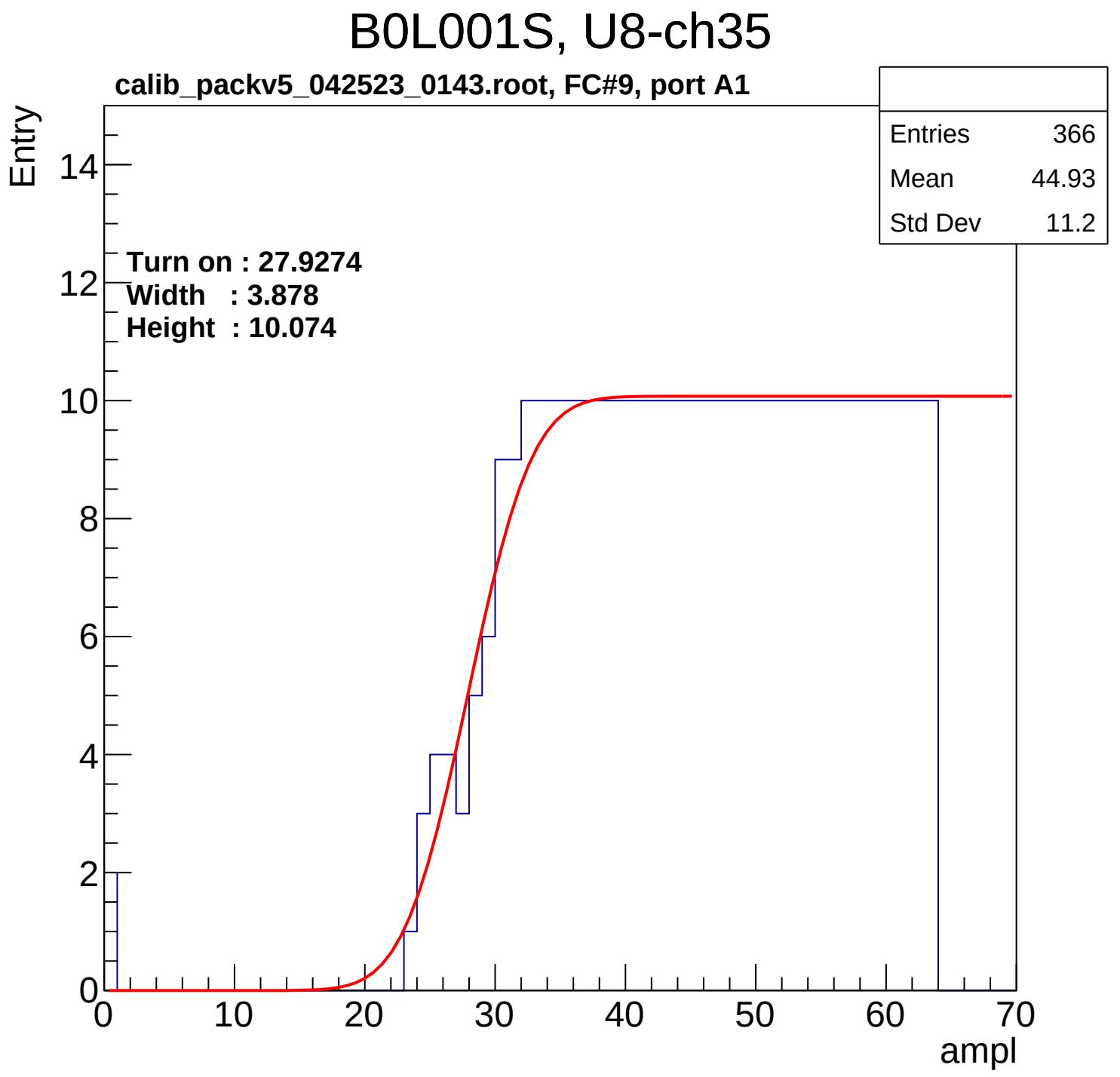
B0L001S, U8-ch35
calib_packv5_042523_0143.root, FC#9, port A1
Entries 366
Mean 44.93
Std Dev 11.2
Turn on : 27.9274
Width : 3.878
Height : 10.074
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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40
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60
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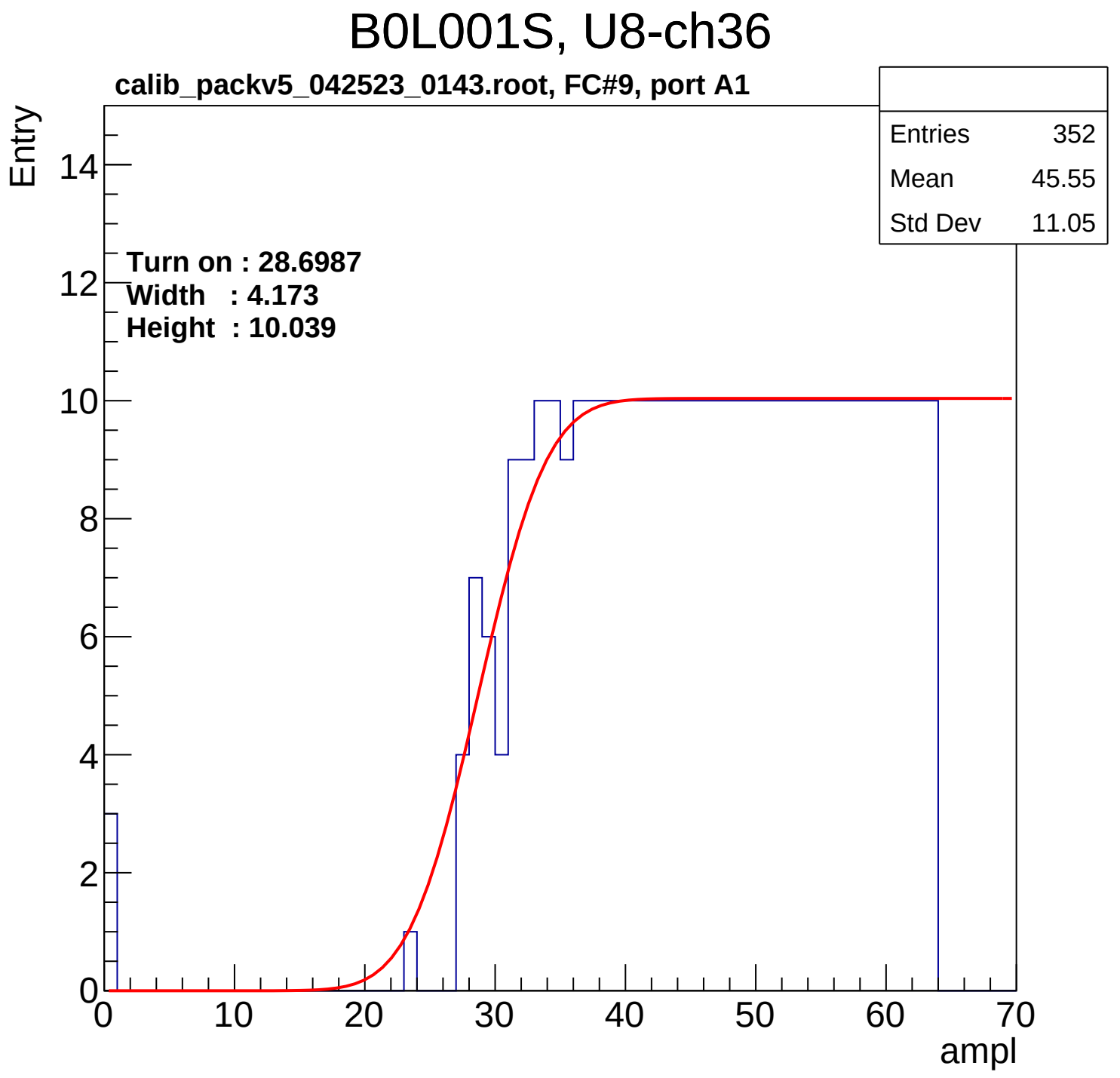
B0L001S, U8-ch36
calib_packv5_042523_0143.root, FC#9, port A1
Entries 352
Mean 45.55
Std Dev 11.05
Turn on : 28.6987
Width : 4.173
Height : 10.039
Entry
ampl
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2
4
6
8
10
12
14
0
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20
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40
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60
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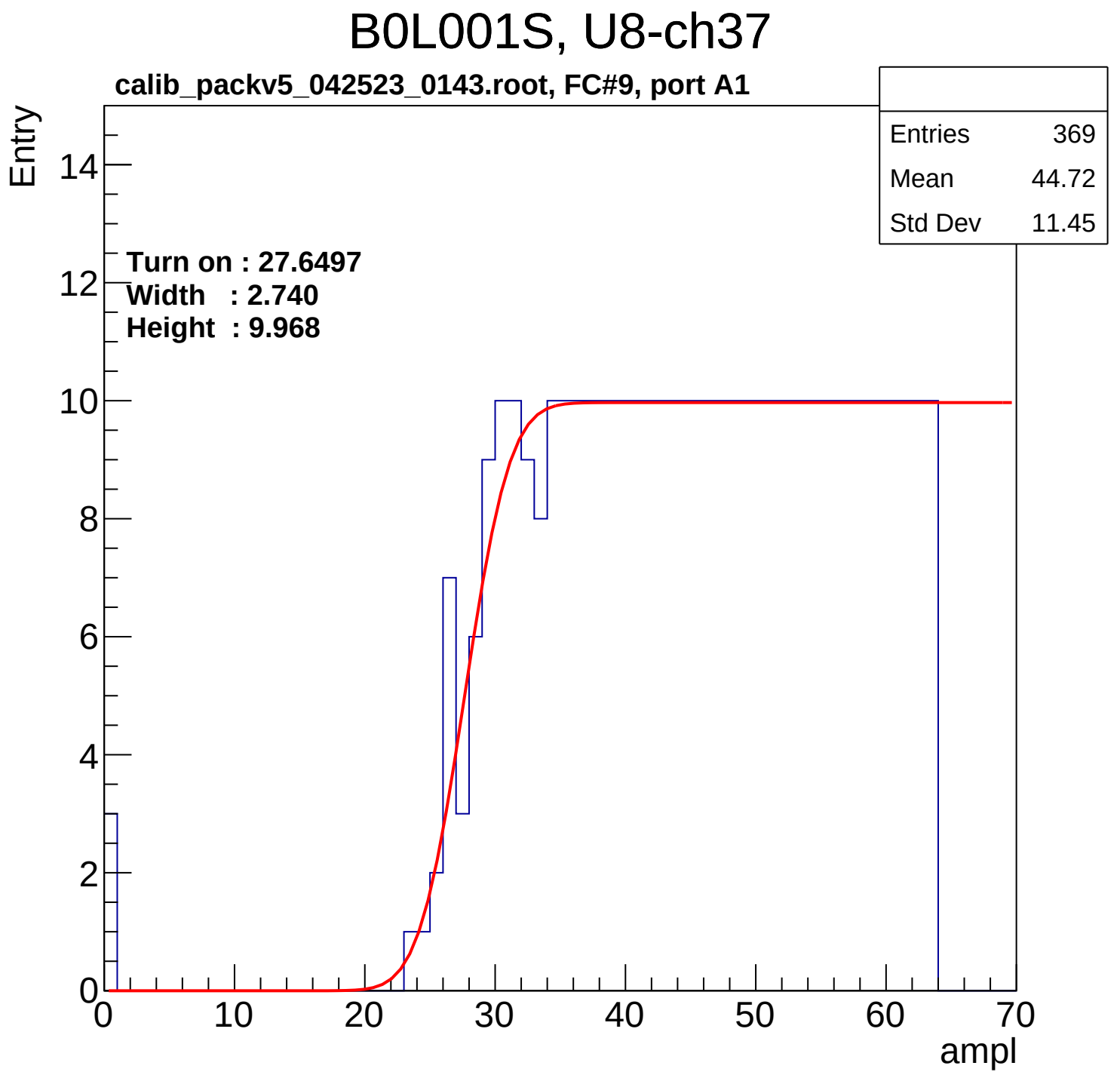
B0L001S, U8-ch37
calib_packv5_042523_0143.root, FC#9, port A1
Entries 369
Mean 44.72
Std Dev 11.45
Turn on : 27.6497
Width : 2.740
Height : 9.968
Entry
ampl
0
2
4
6
8
10
12
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0
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20
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40
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60
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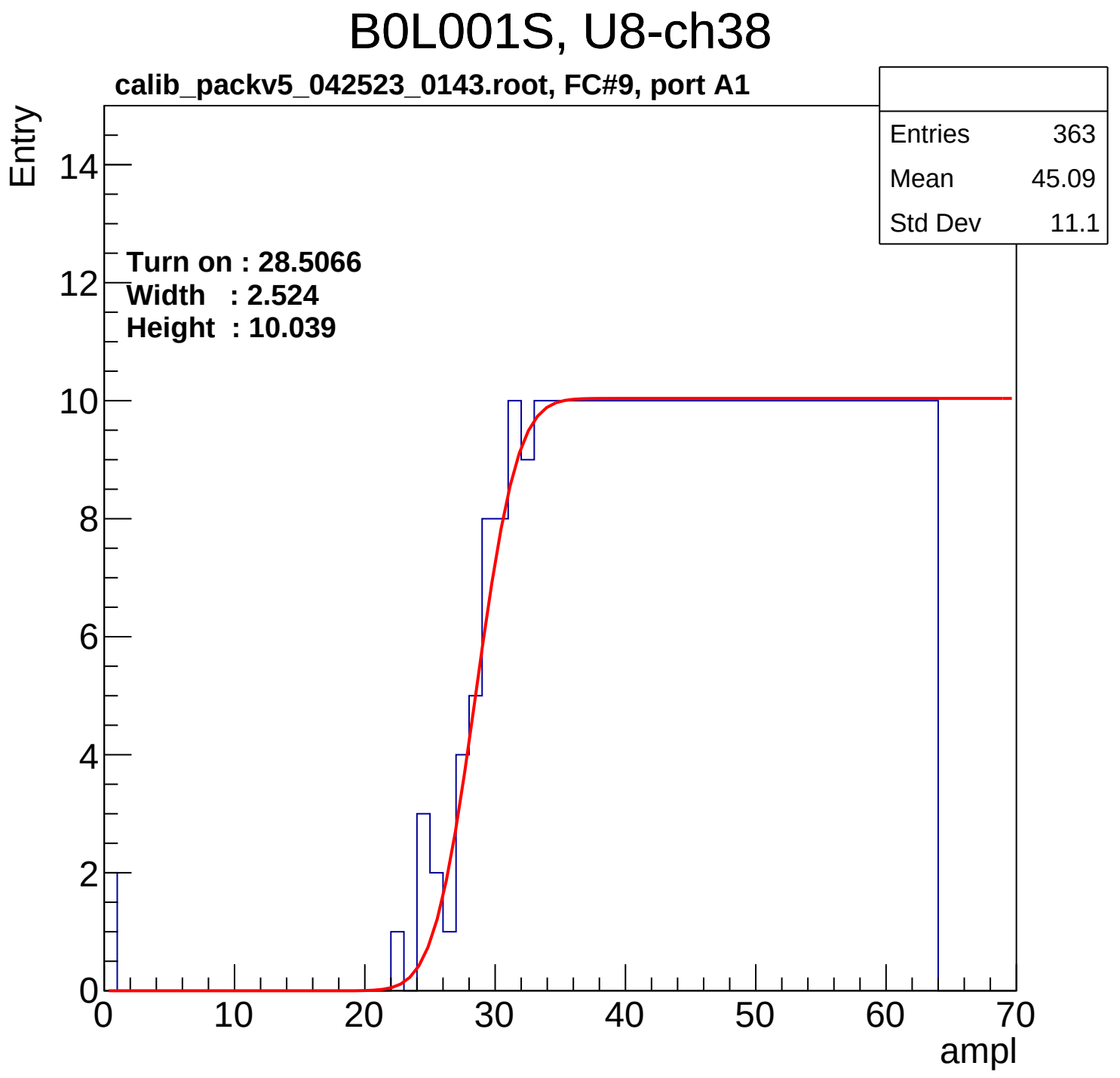
B0L001S, U8-ch38
calib_packv5_042523_0143.root, FC#9, port A1
Entries 363
Mean 45.09
Std Dev 11.1
Turn on : 28.5066
Width : 2.524
Height : 10.039
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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40
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60
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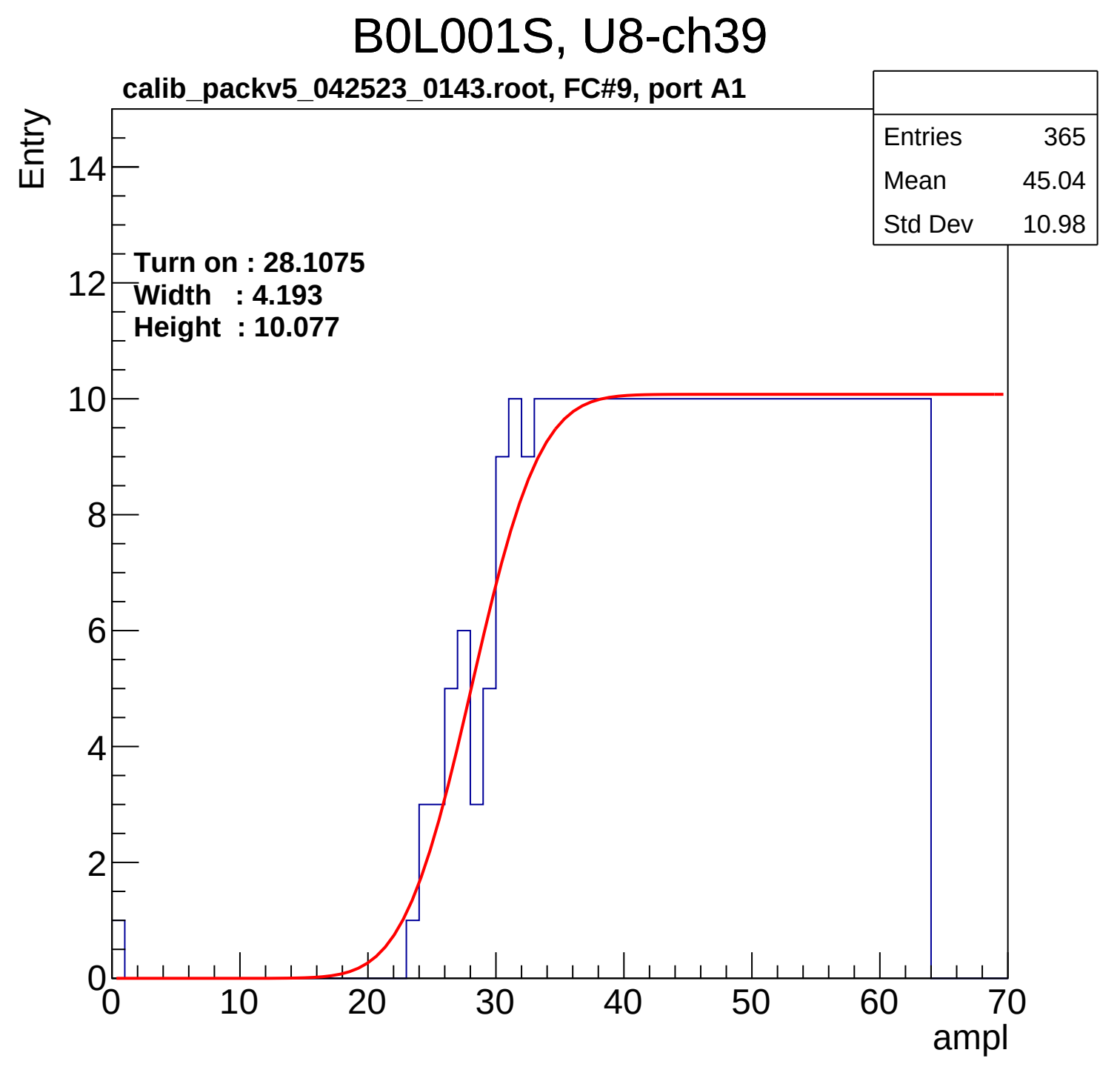
B0L001S, U8-ch39
calib_packv5_042523_0143.root, FC#9, port A1
Entries 365
Mean 45.04
Std Dev 10.98
Turn on : 28.1075
Width : 4.193
Height : 10.077
Entry
ampl
0
2
4
6
8
10
12
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0
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20
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40
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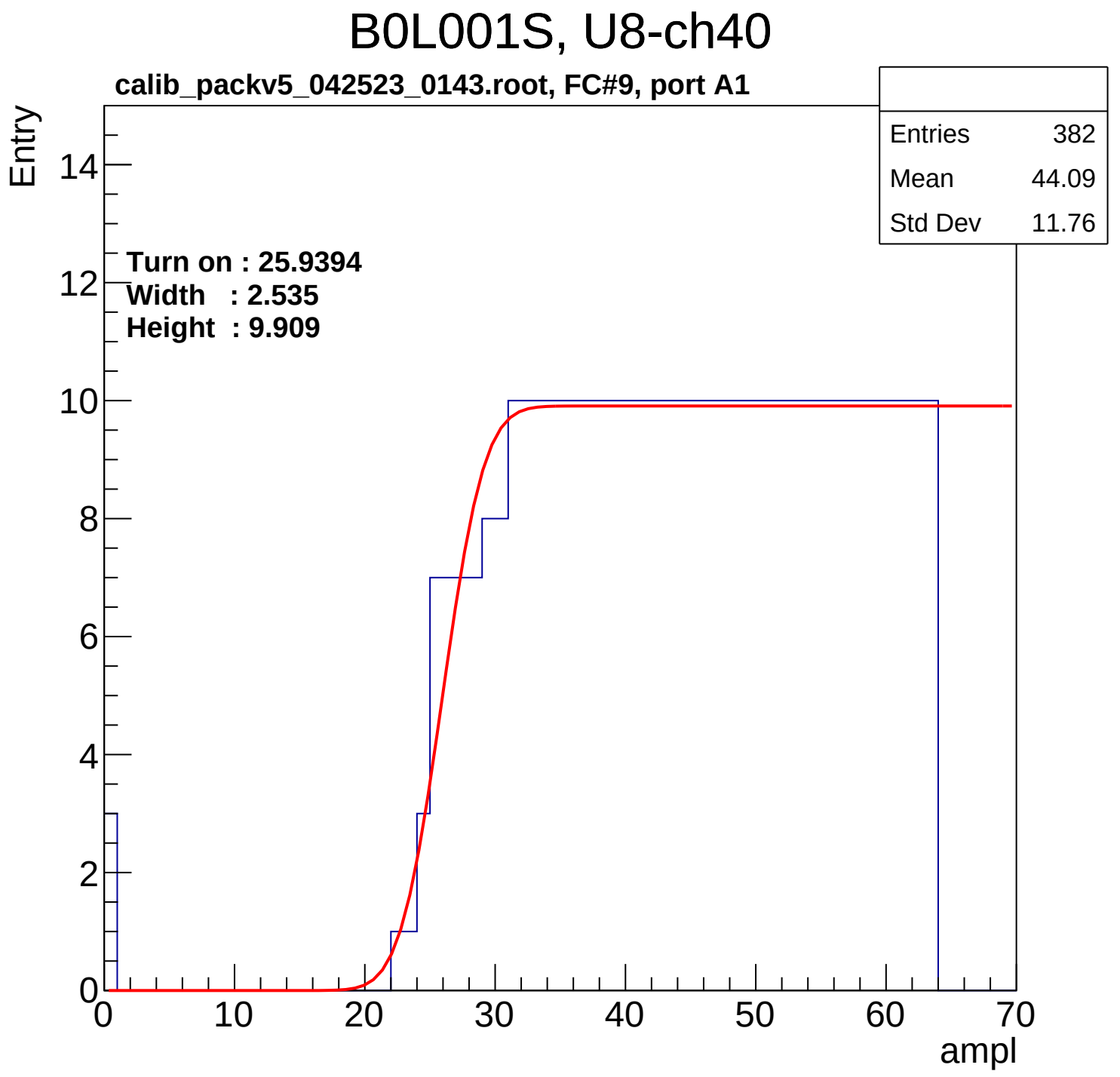
B0L001S, U8-ch40
calib_packv5_042523_0143.root, FC#9, port A1
Entries 382
Mean 44.09
Std Dev 11.76
Turn on : 25.9394
Width : 2.535
Height : 9.909
Entry
ampl
0
2
4
6
8
10
12
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0
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20
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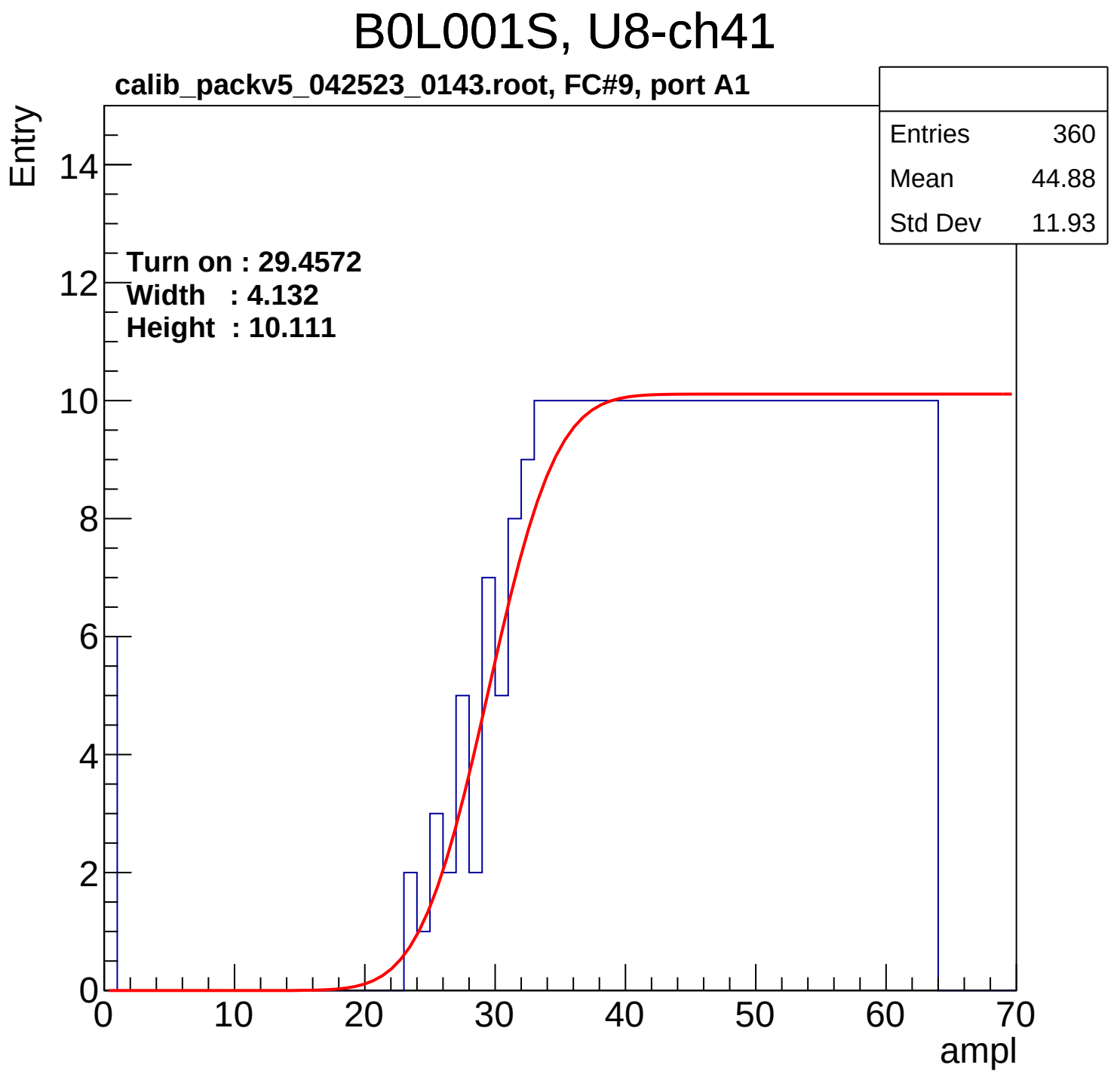
B0L001S, U8-ch41
calib_packv5_042523_0143.root, FC#9, port A1
Entries 360
Mean 44.88
Std Dev 11.93
Turn on : 29.4572
Width : 4.132
Height : 10.111
Entry
ampl
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8
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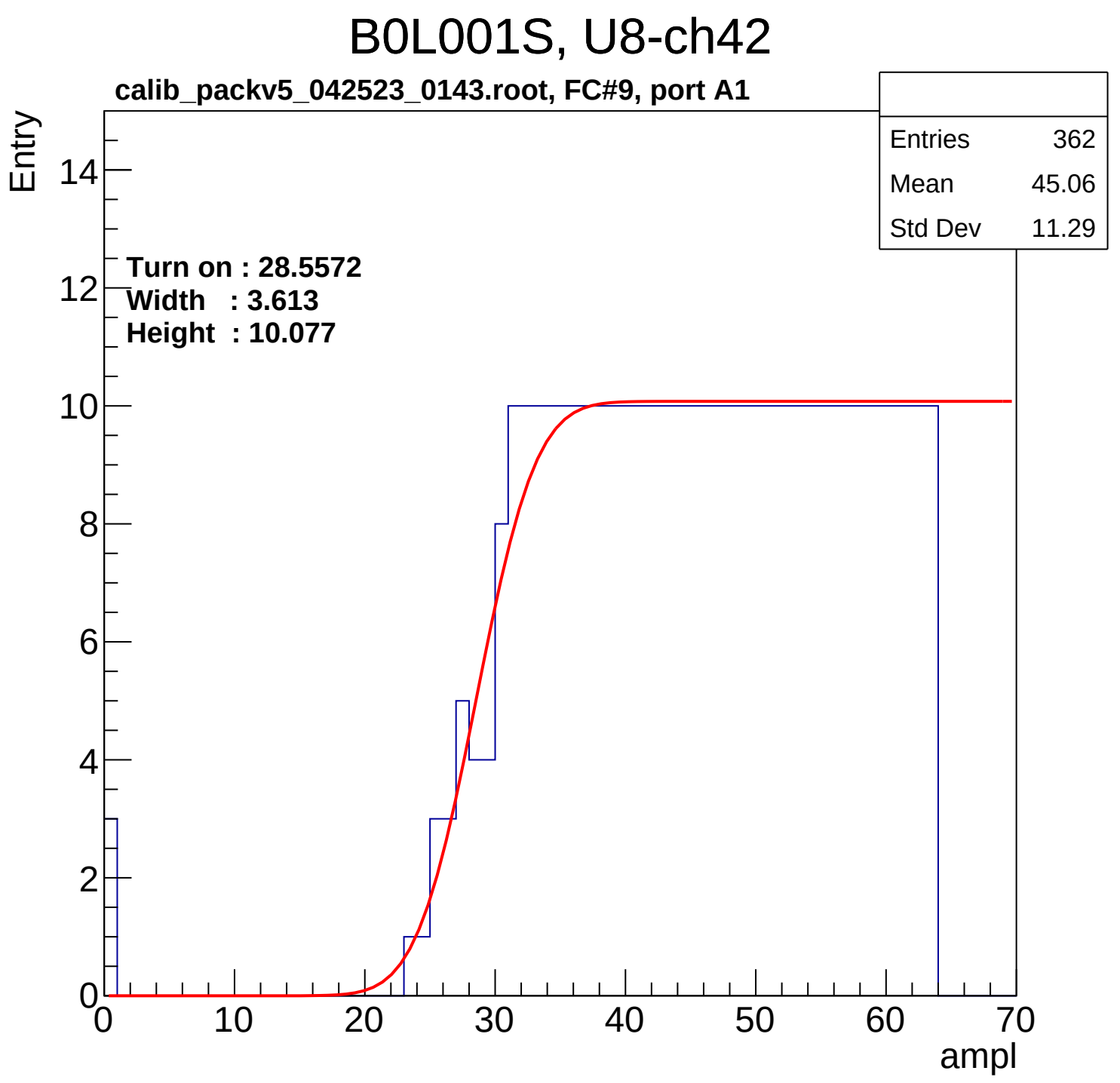
B0L001S, U8-ch42
calib_packv5_042523_0143.root, FC#9, port A1
Entries 362
Mean 45.06
Std Dev 11.29
Turn on : 28.5572
Width : 3.613
Height : 10.077
Entry
ampl
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2
4
6
8
10
12
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0
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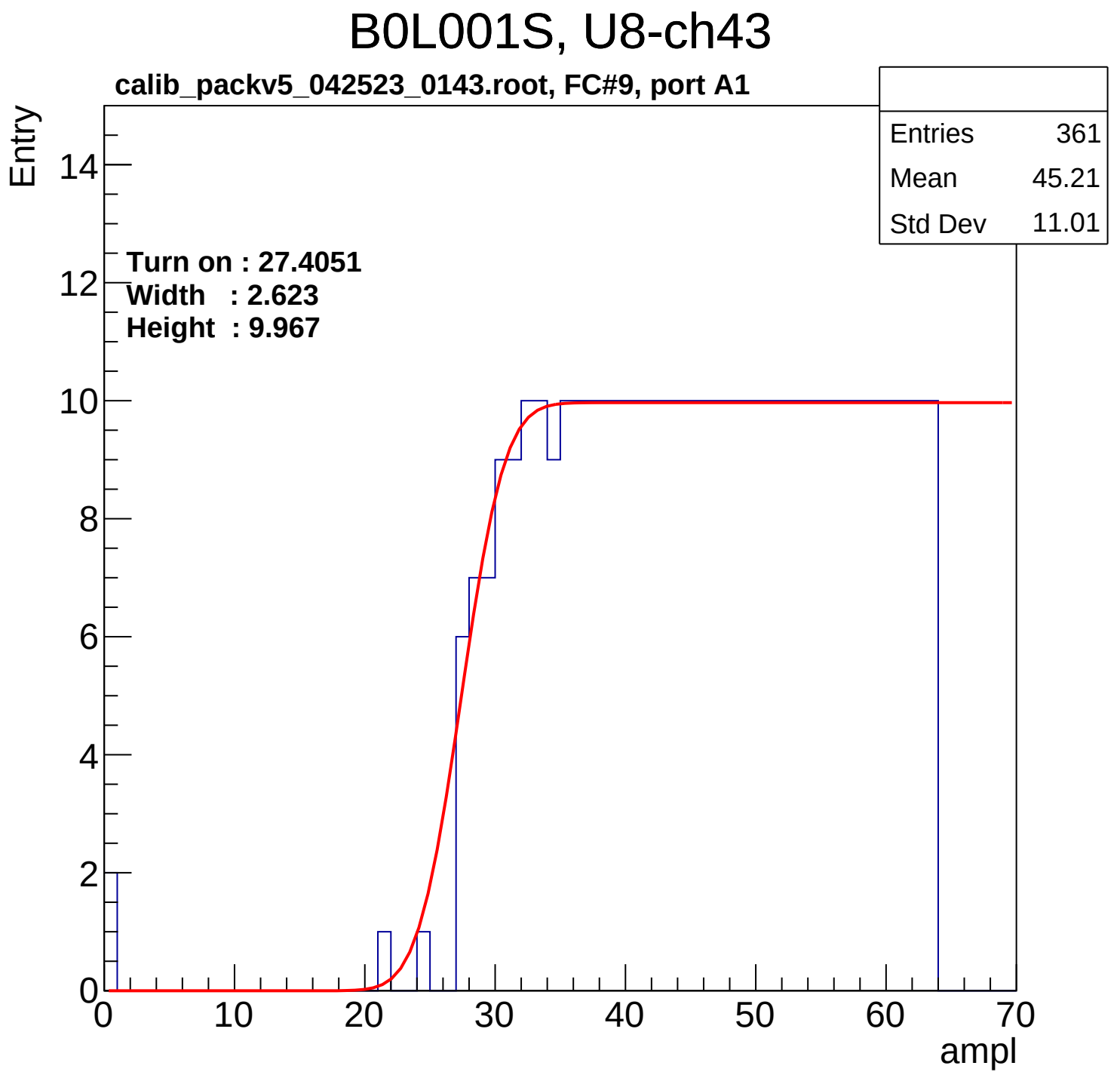
B0L001S, U8-ch43
calib_packv5_042523_0143.root, FC#9, port A1
Entries 361
Mean 45.21
Std Dev 11.01
Turn on : 27.4051
Width : 2.623
Height : 9.967
Entry
ampl
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2
4
6
8
10
12
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0
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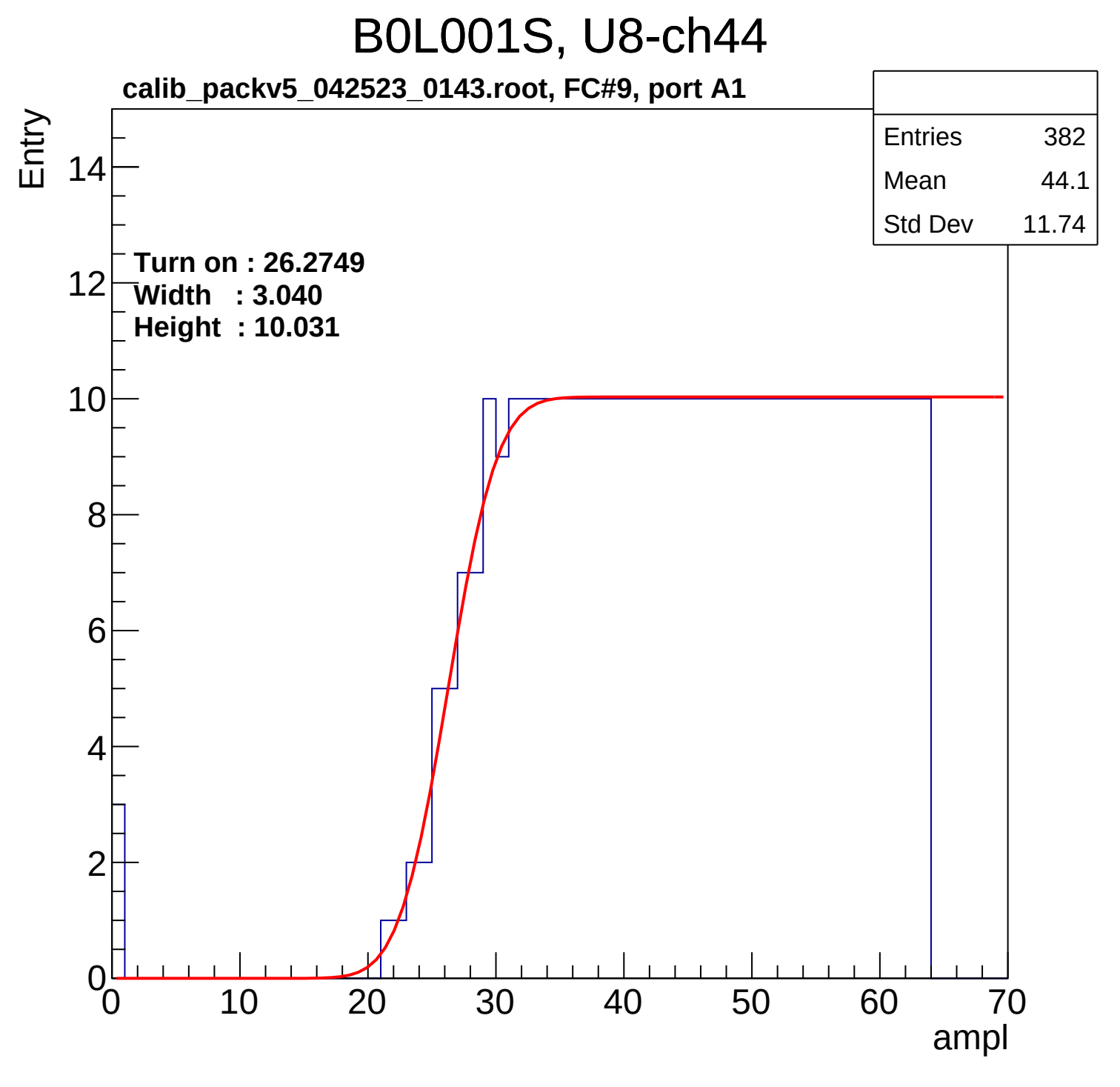
B0L001S, U8-ch44
calib_packv5_042523_0143.root, FC#9, port A1
Entries 382
Mean 44.1
Std Dev 11.74
Turn on : 26.2749
Width : 3.040
Height : 10.031
Entry
ampl
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2
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6
8
10
12
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0
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60
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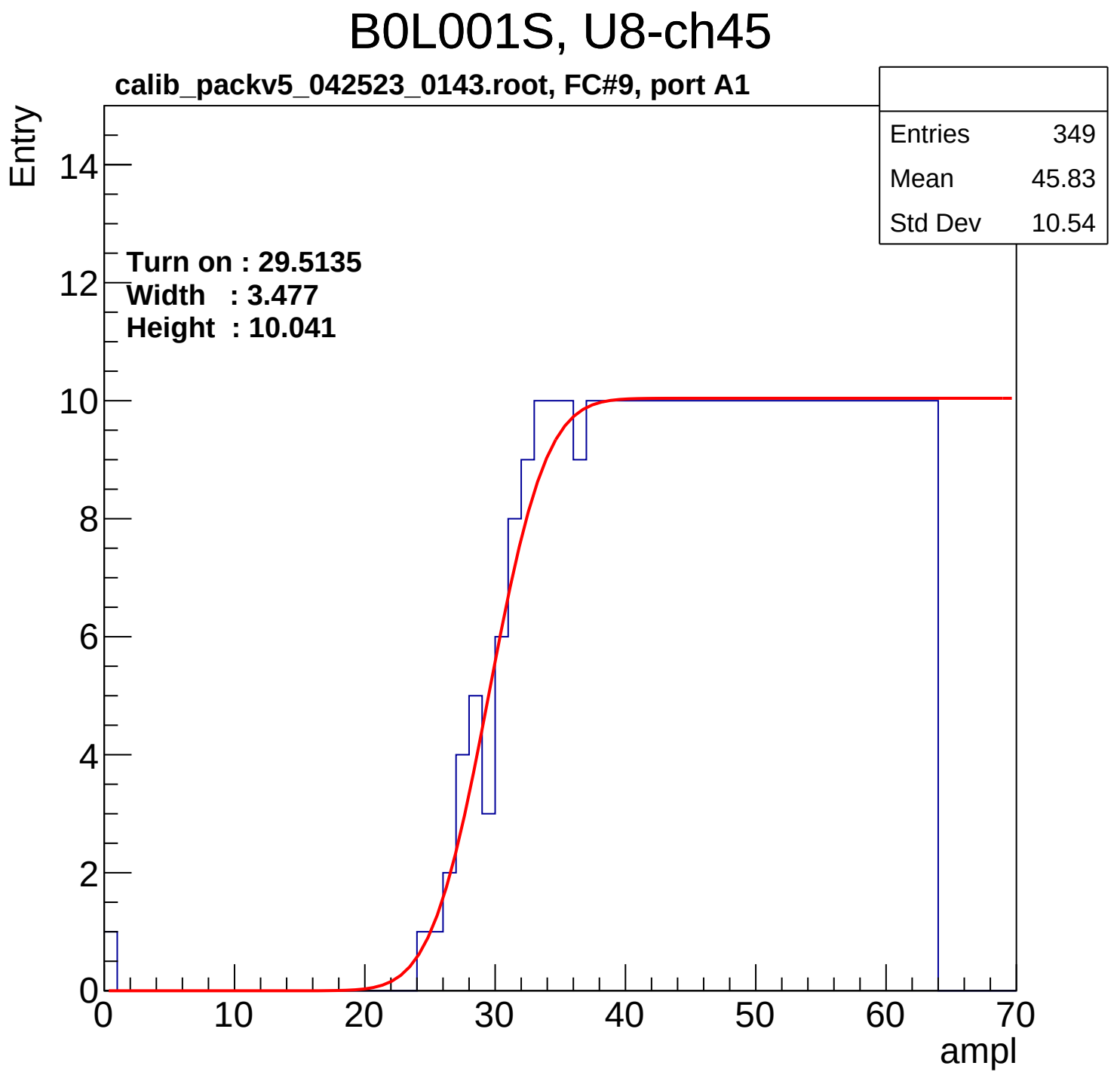
B0L001S, U8-ch45
calib_packv5_042523_0143.root, FC#9, port A1
Entries 349
Mean 45.83
Std Dev 10.54
Turn on : 29.5135
Width : 3.477
Height : 10.041
Entry
ampl
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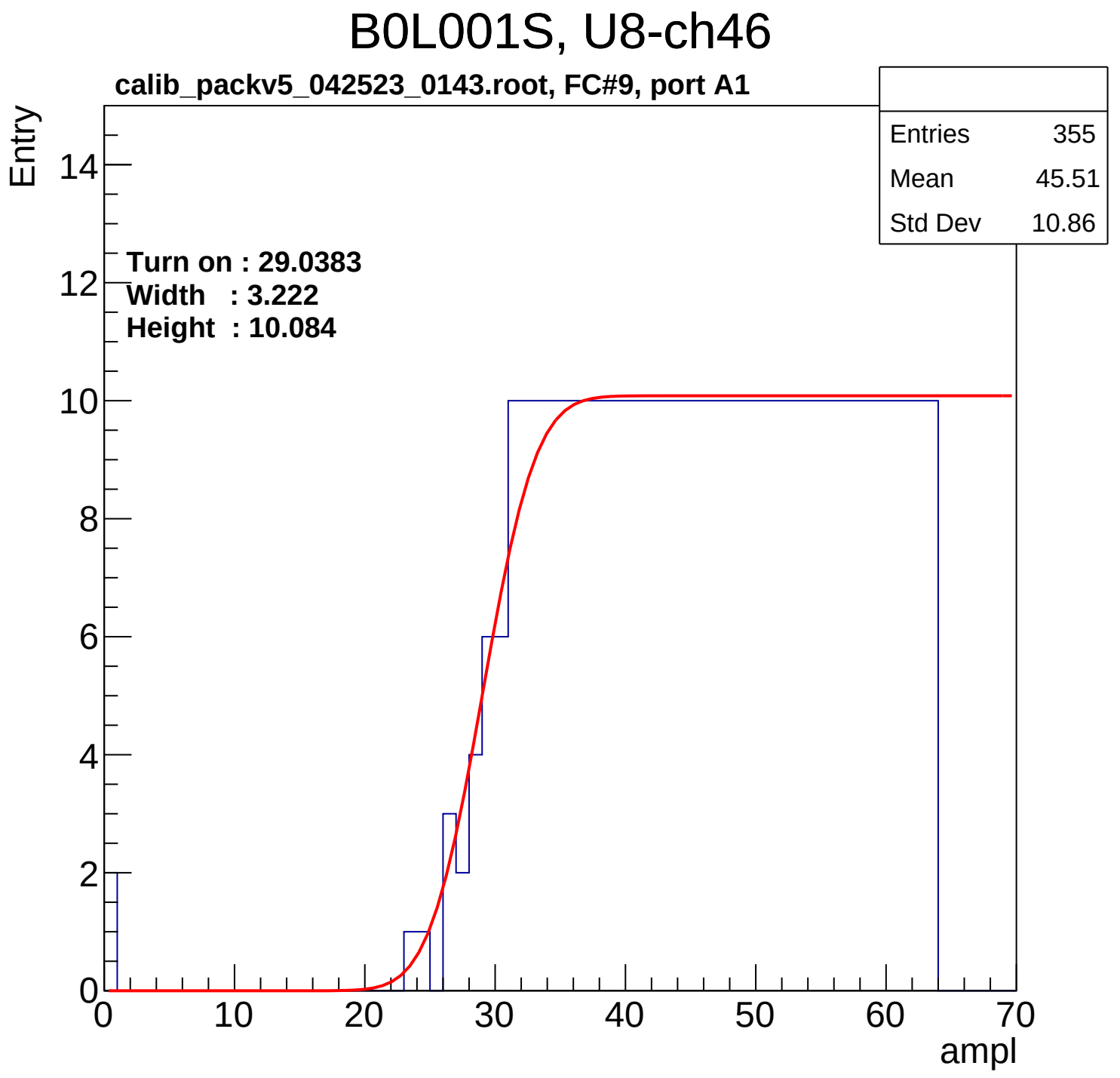
B0L001S, U8-ch46
calib_packv5_042523_0143.root, FC#9, port A1
Entries 355
Mean 45.51
Std Dev 10.86
Turn on : 29.0383
Width : 3.222
Height : 10.084
Entry
ampl
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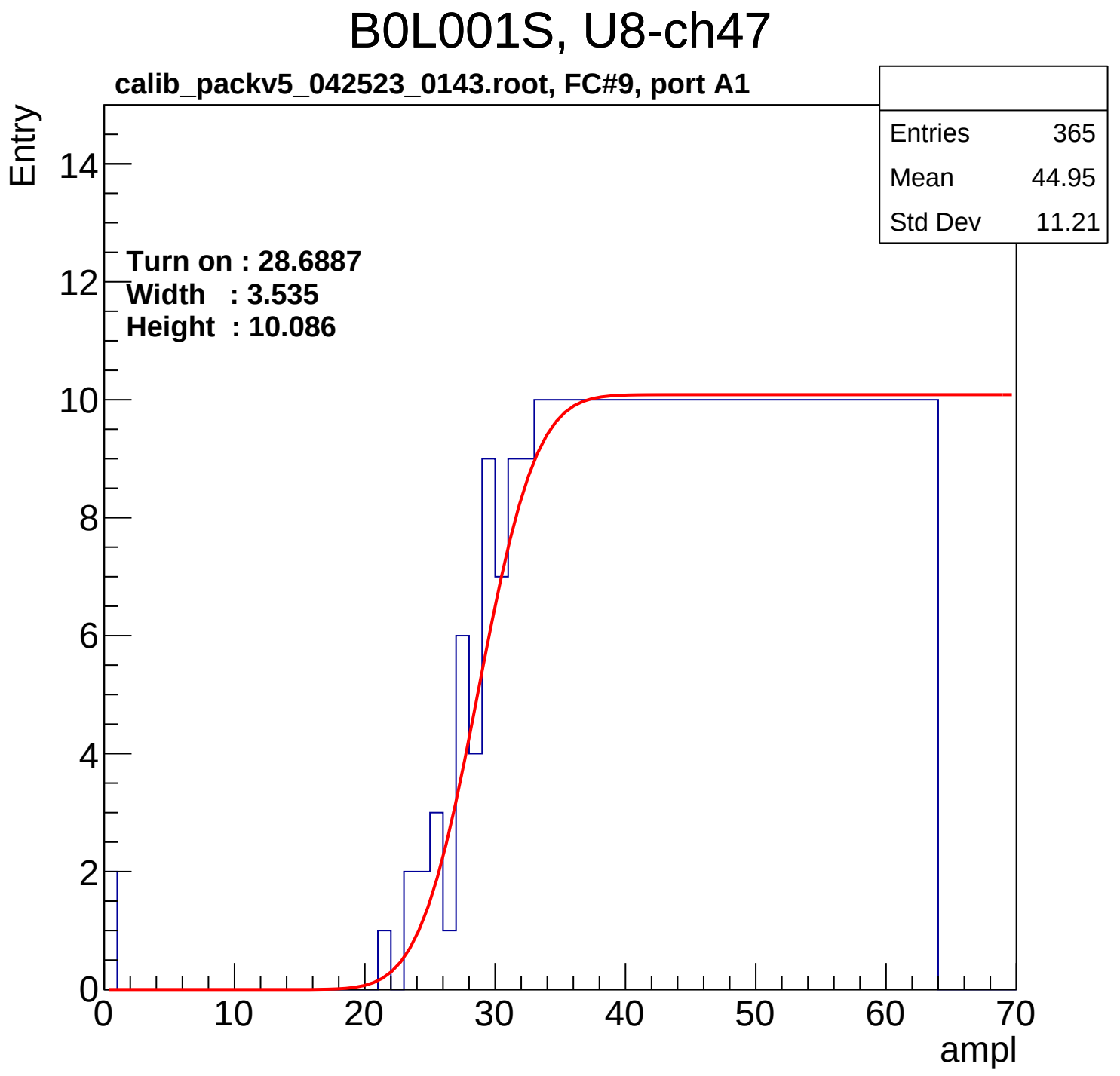
B0L001S, U8-ch47
calib_packv5_042523_0143.root, FC#9, port A1
Entries 365
Mean 44.95
Std Dev 11.21
Turn on : 28.6887
Width : 3.535
Height : 10.086
Entry
ampl
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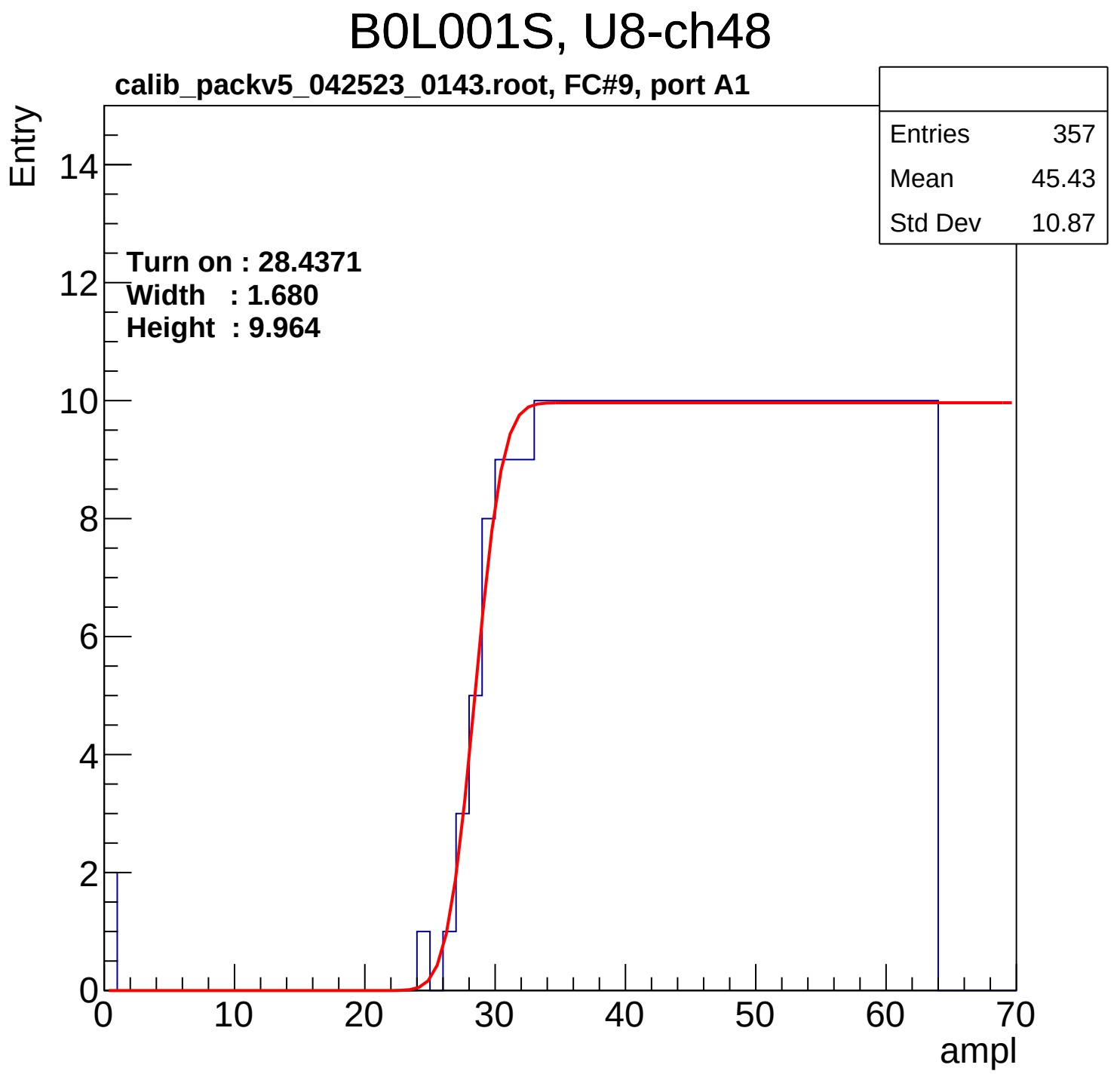
B0L001S, U8-ch48
calib_packv5_042523_0143.root, FC#9, port A1
Entries 357
Mean 45.43
Std Dev 10.87
Turn on : 28.4371
Width : 1.680
Height : 9.964
Entry
ampl
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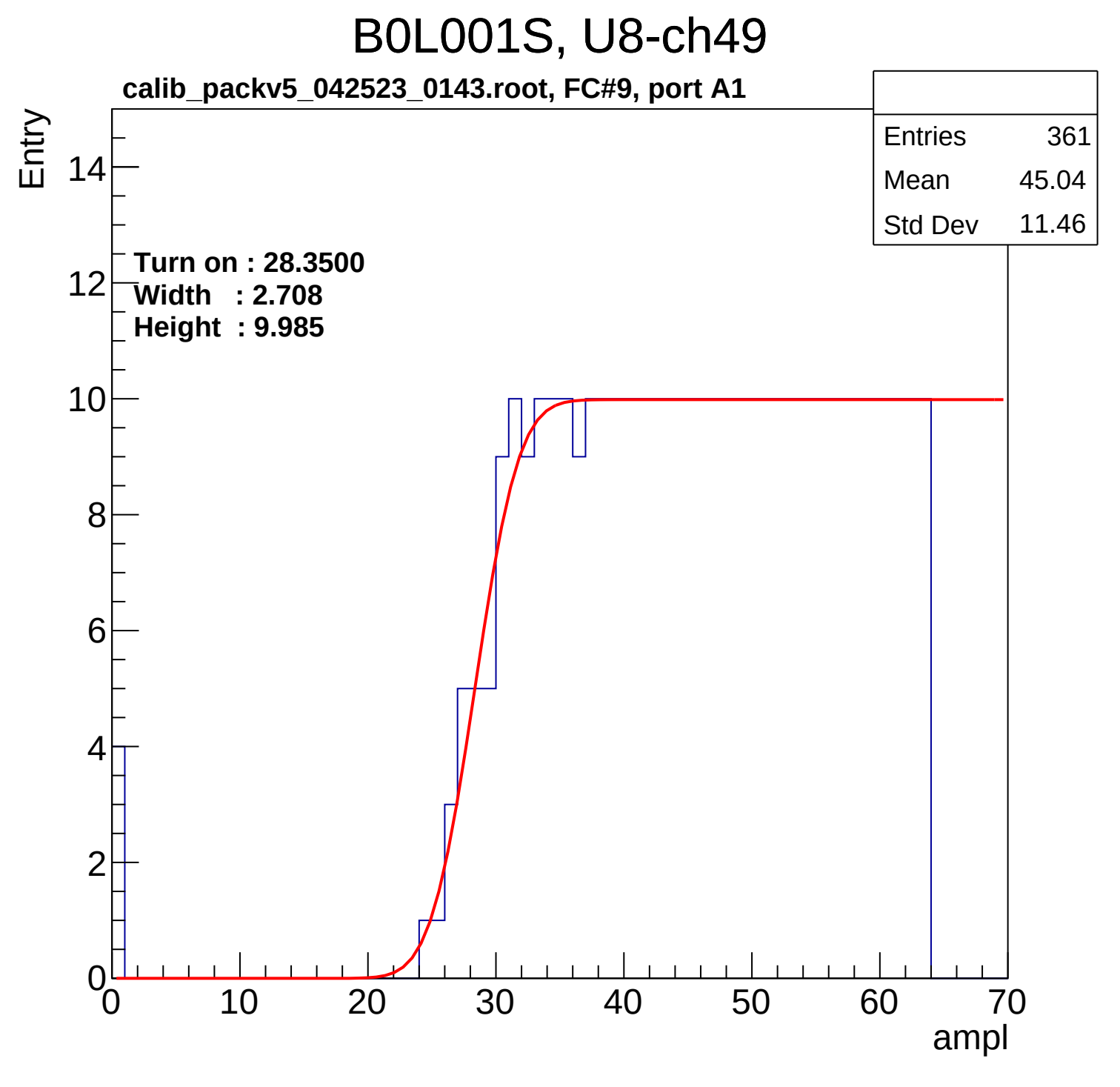
B0L001S, U8-ch49
calib_packv5_042523_0143.root, FC#9, port A1
Entries 361
Mean 45.04
Std Dev 11.46
Turn on : 28.3500
Width : 2.708
Height : 9.985
Entry
ampl
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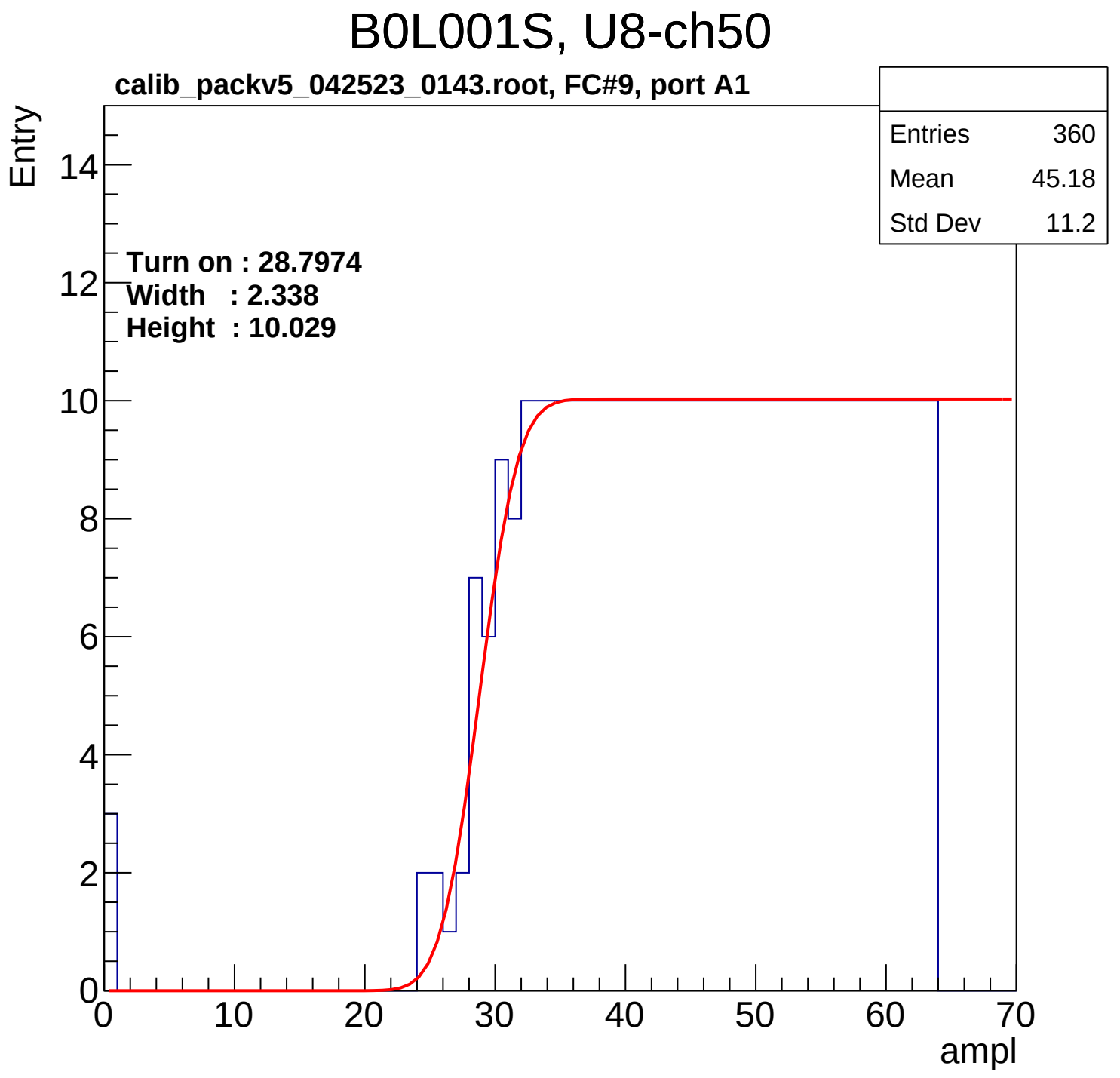
B0L001S, U8-ch50
calib_packv5_042523_0143.root, FC#9, port A1
Entries 360
Mean 45.18
Std Dev 11.2
Turn on : 28.7974
Width : 2.338
Height : 10.029
Entry
ampl
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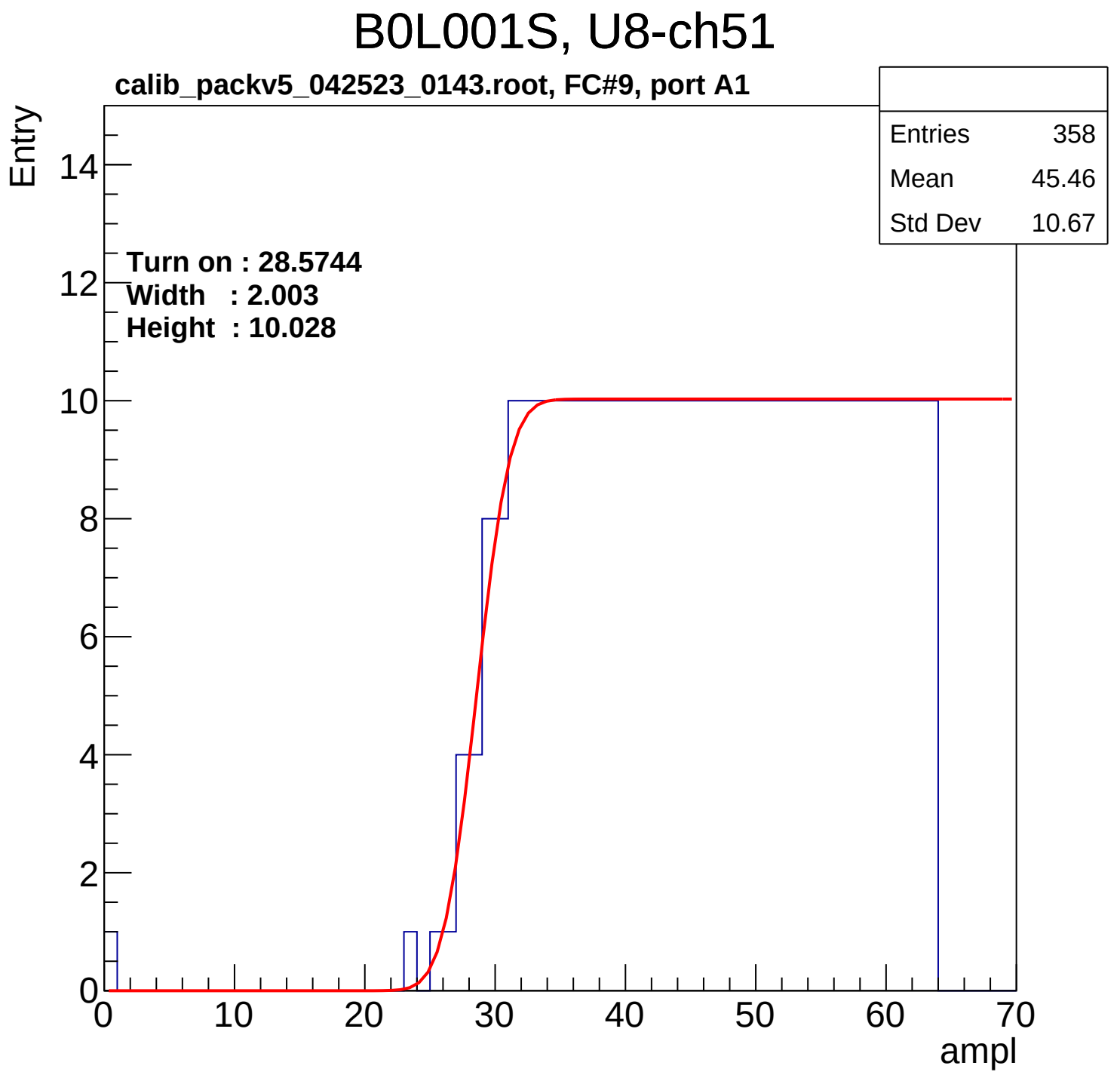
B0L001S, U8-ch51
calib_packv5_042523_0143.root, FC#9, port A1
Entries 358
Mean 45.46
Std Dev 10.67
Turn on : 28.5744
Width : 2.003
Height : 10.028
Entry
ampl
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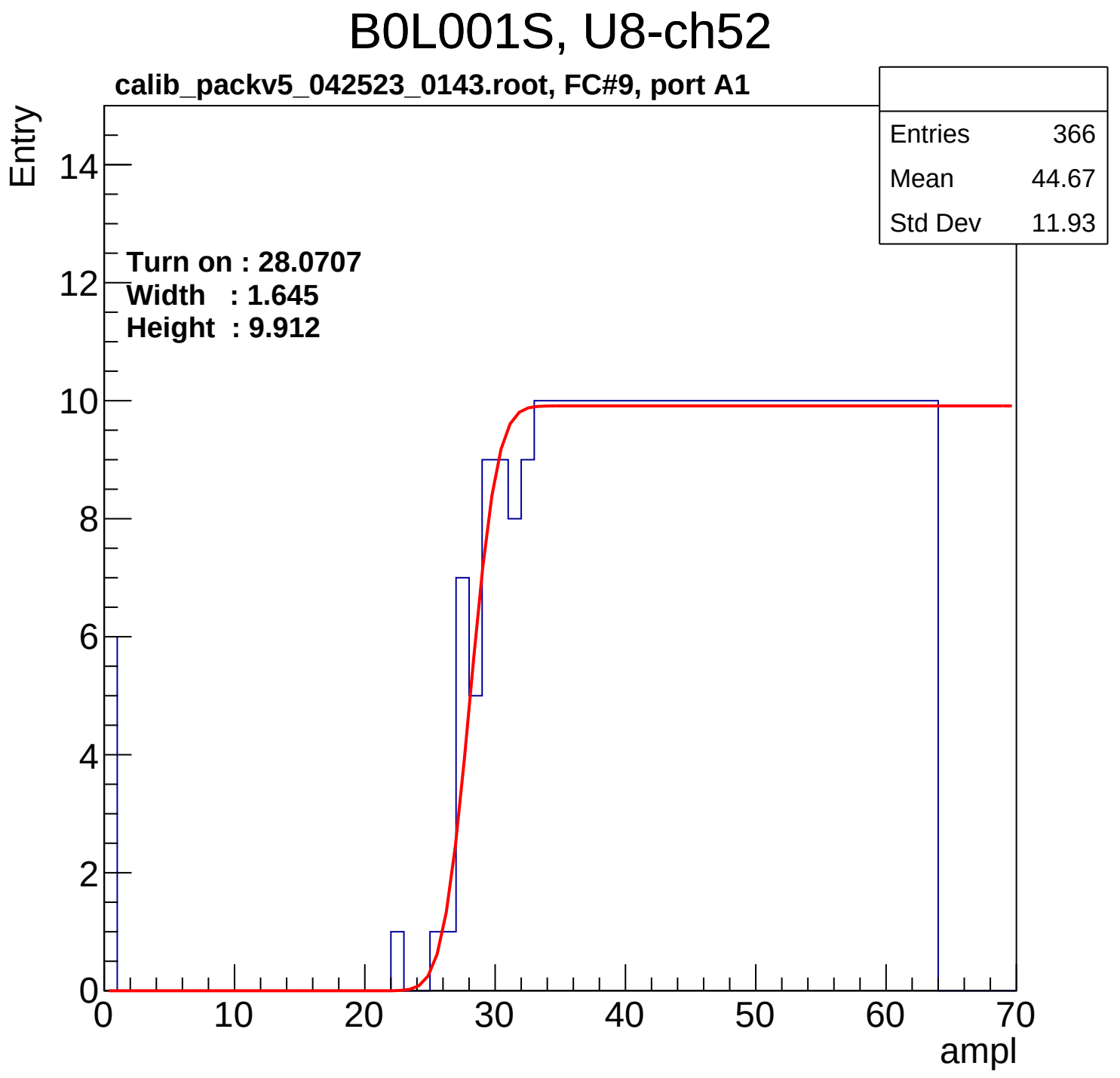
B0L001S, U8-ch52
calib_packv5_042523_0143.root, FC#9, port A1
Entries 366
Mean 44.67
Std Dev 11.93
Turn on : 28.0707
Width : 1.645
Height : 9.912
Entry
ampl
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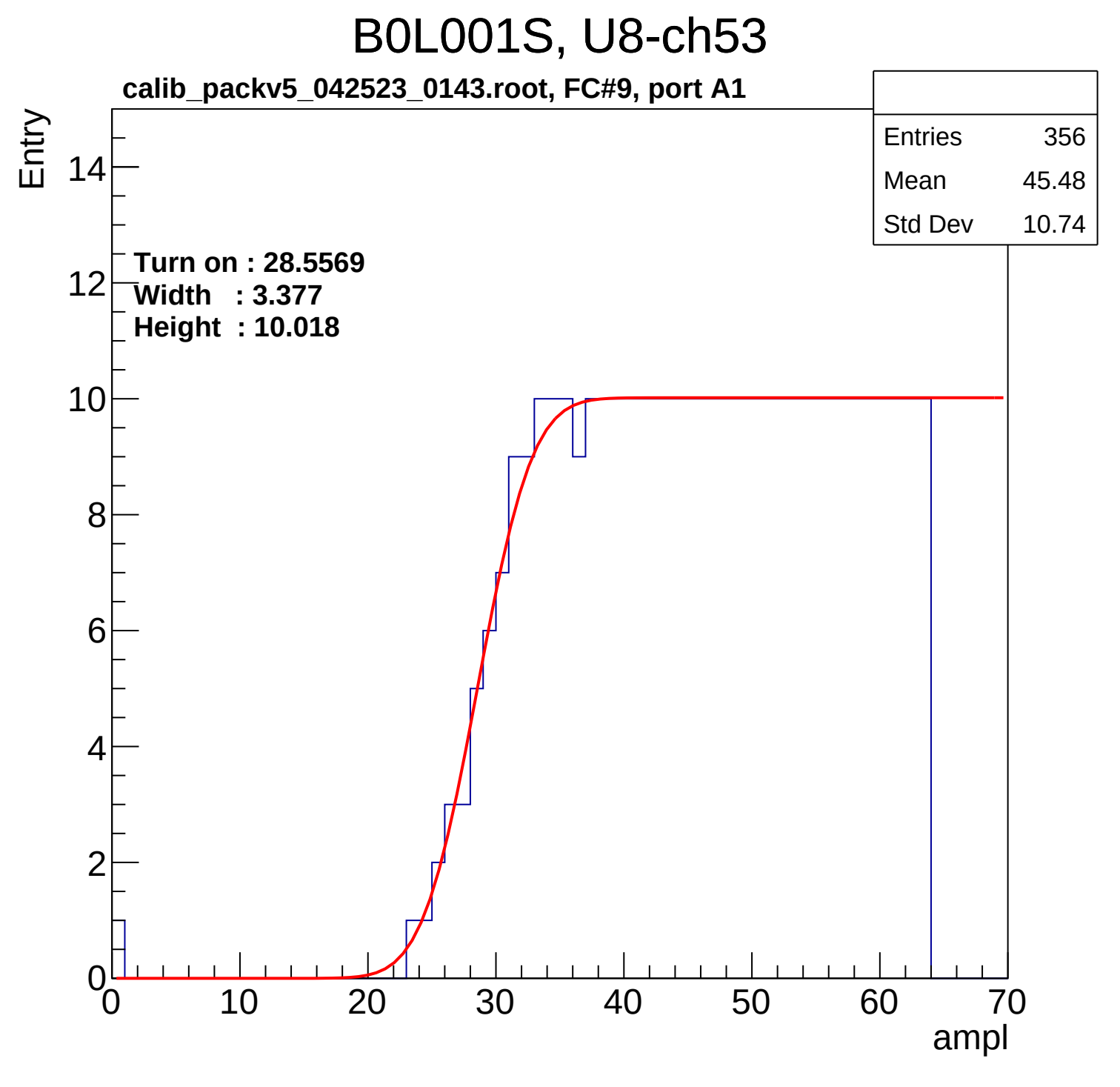
B0L001S, U8-ch53
calib_packv5_042523_0143.root, FC#9, port A1
Entries 356
Mean 45.48
Std Dev 10.74
Turn on : 28.5569
Width : 3.377
Height : 10.018
Entry
ampl
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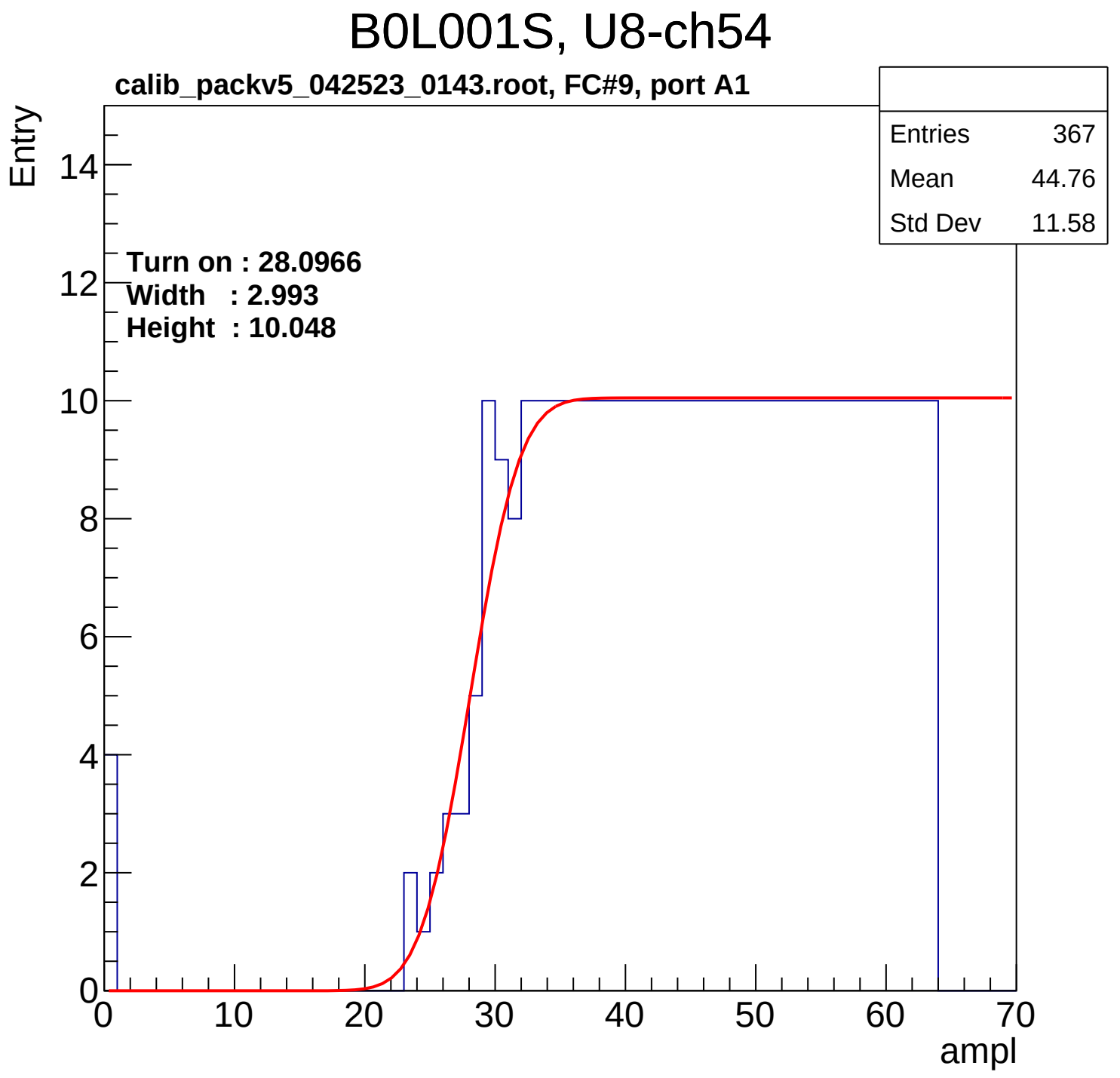
B0L001S, U8-ch54
calib_packv5_042523_0143.root, FC#9, port A1
Entries 367
Mean 44.76
Std Dev 11.58
Turn on : 28.0966
Width : 2.993
Height : 10.048
Entry
ampl
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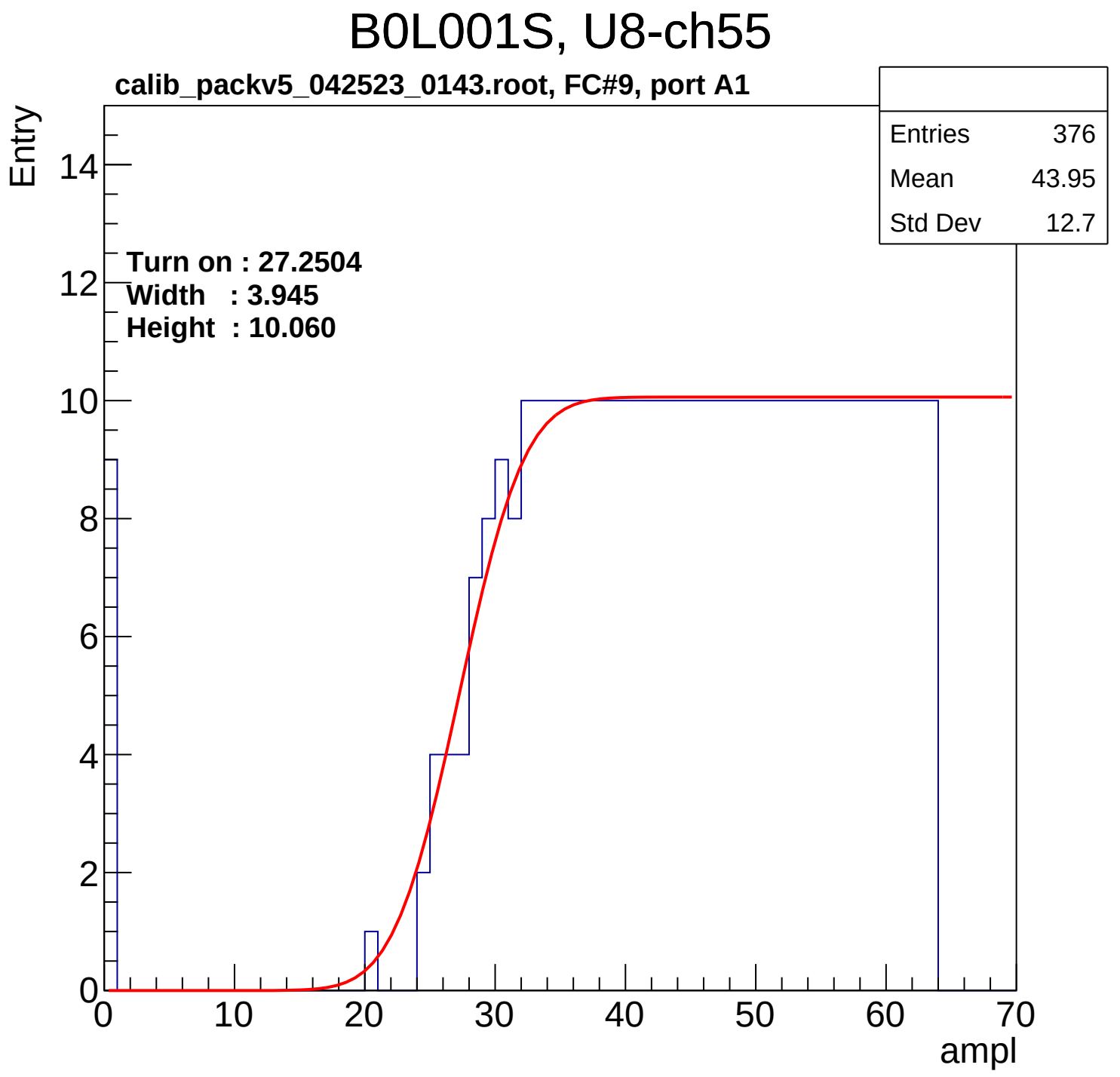
B0L001S, U8-ch55
calib_packv5_042523_0143.root, FC#9, port A1
Entries 376
Mean 43.95
Std Dev 12.7
Turn on : 27.2504
Width : 3.945
Height : 10.060
Entry
ampl
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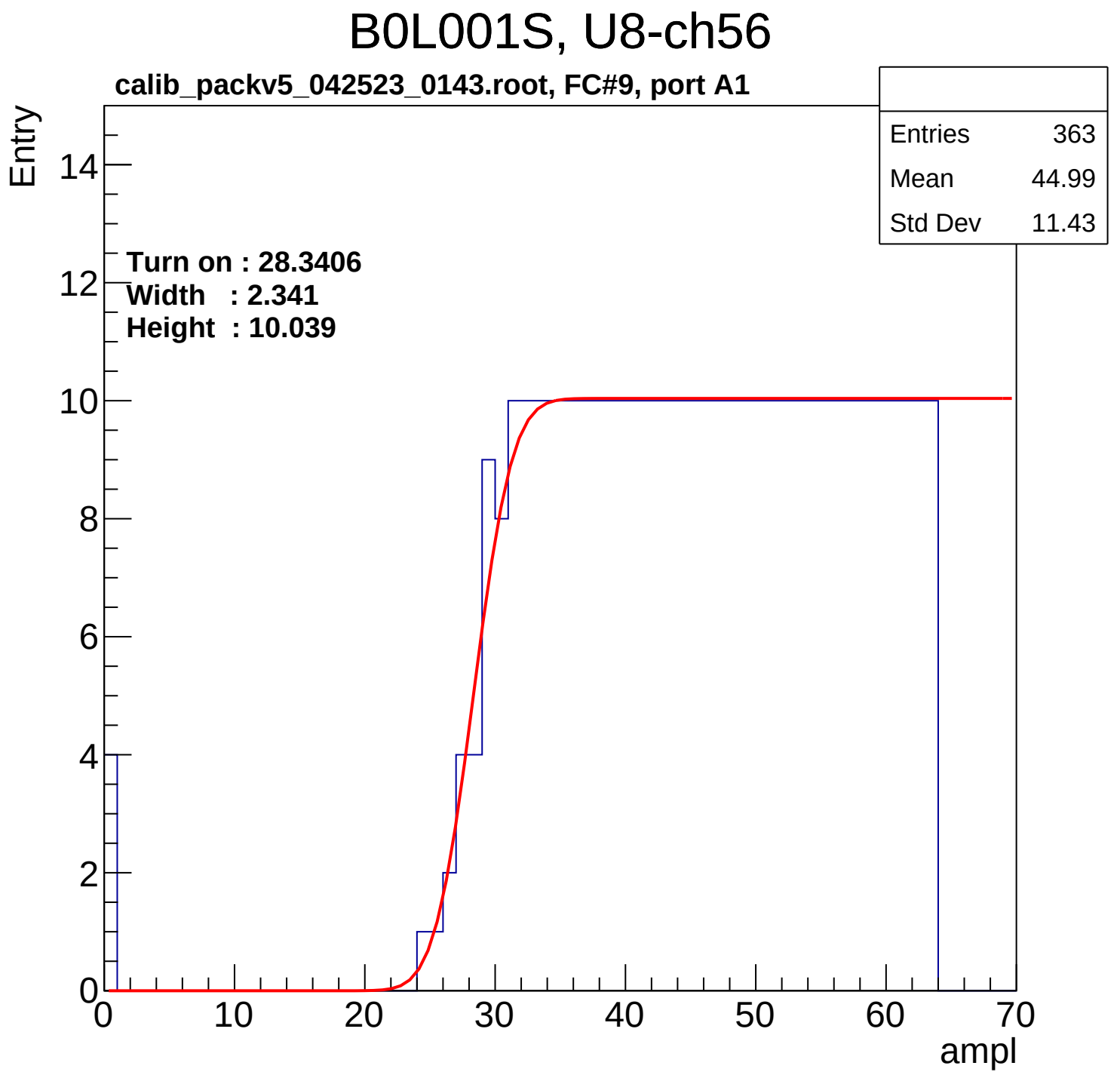
B0L001S, U8-ch56
calib_packv5_042523_0143.root, FC#9, port A1
Entries 363
Mean 44.99
Std Dev 11.43
Turn on : 28.3406
Width : 2.341
Height : 10.039
Entry
ampl
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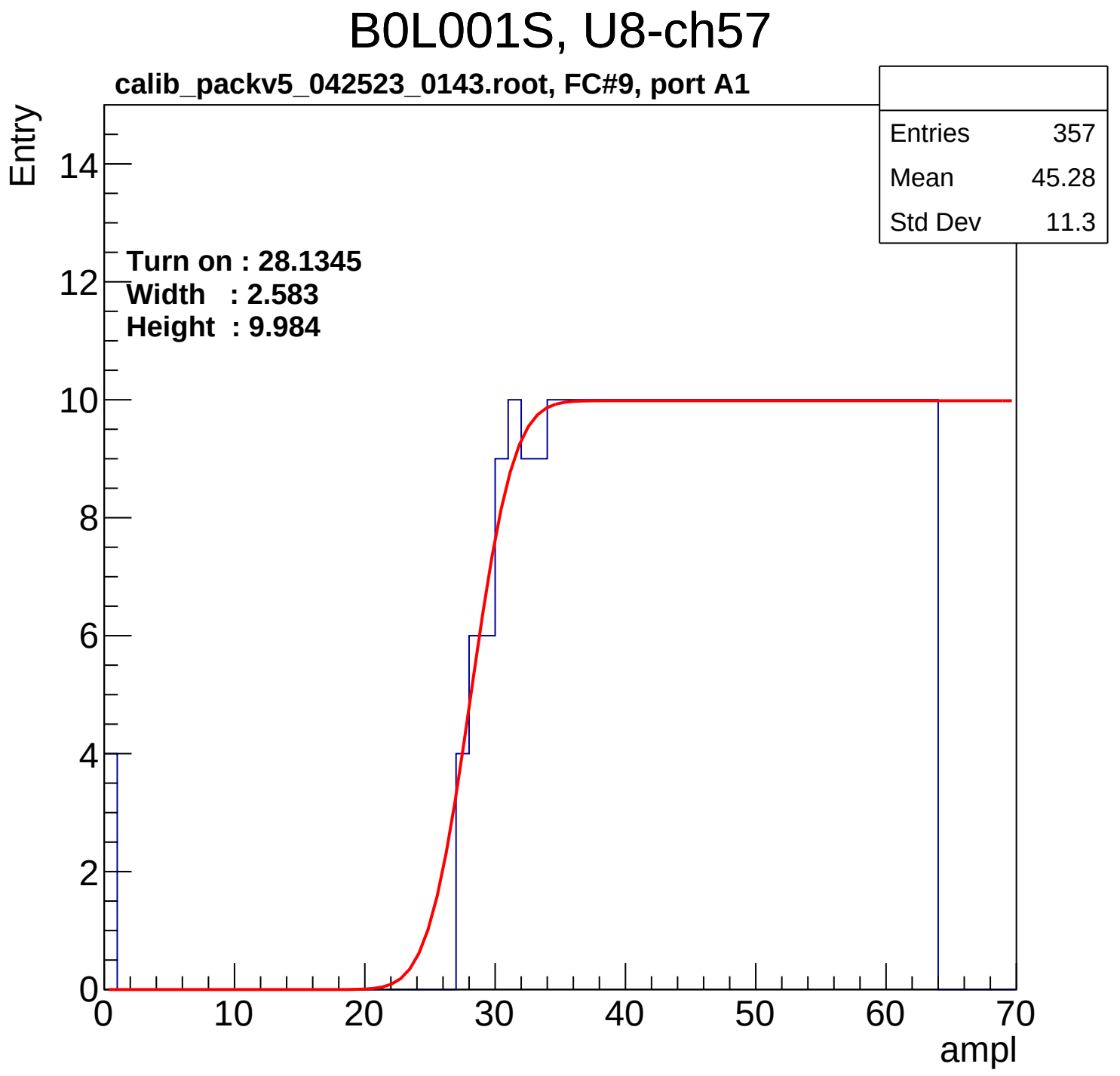
B0L001S, U8-ch57
calib_packv5_042523_0143.root, FC#9, port A1
Entries 357
Mean 45.28
Std Dev 11.3
Turn on : 28.1345
Width : 2.583
Height : 9.984
Entry
ampl
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4
6
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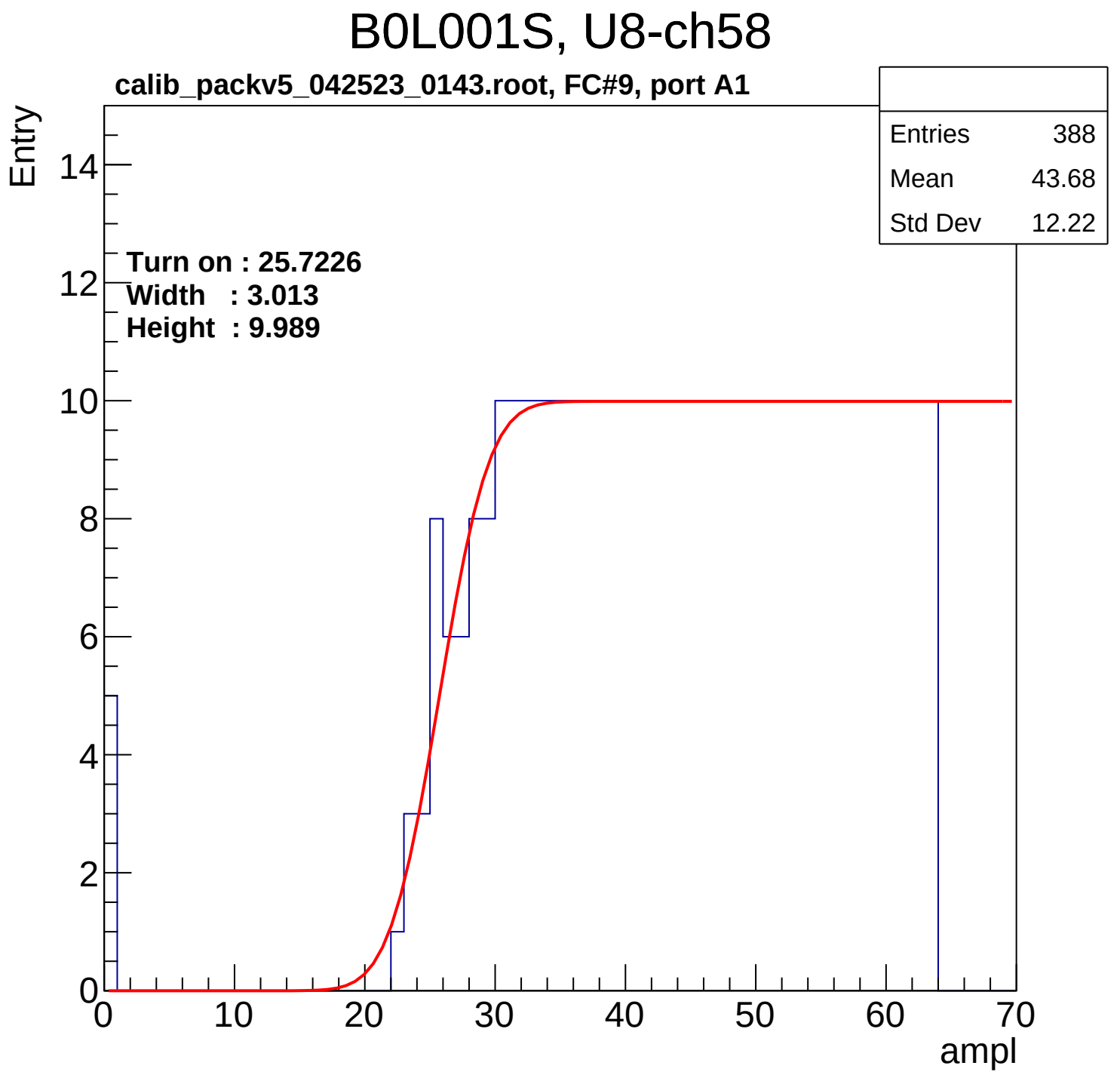
B0L001S, U8-ch58
calib_packv5_042523_0143.root, FC#9, port A1
Entries 388
Mean 43.68
Std Dev 12.22
Turn on : 25.7226
Width : 3.013
Height : 9.989
Entry
ampl
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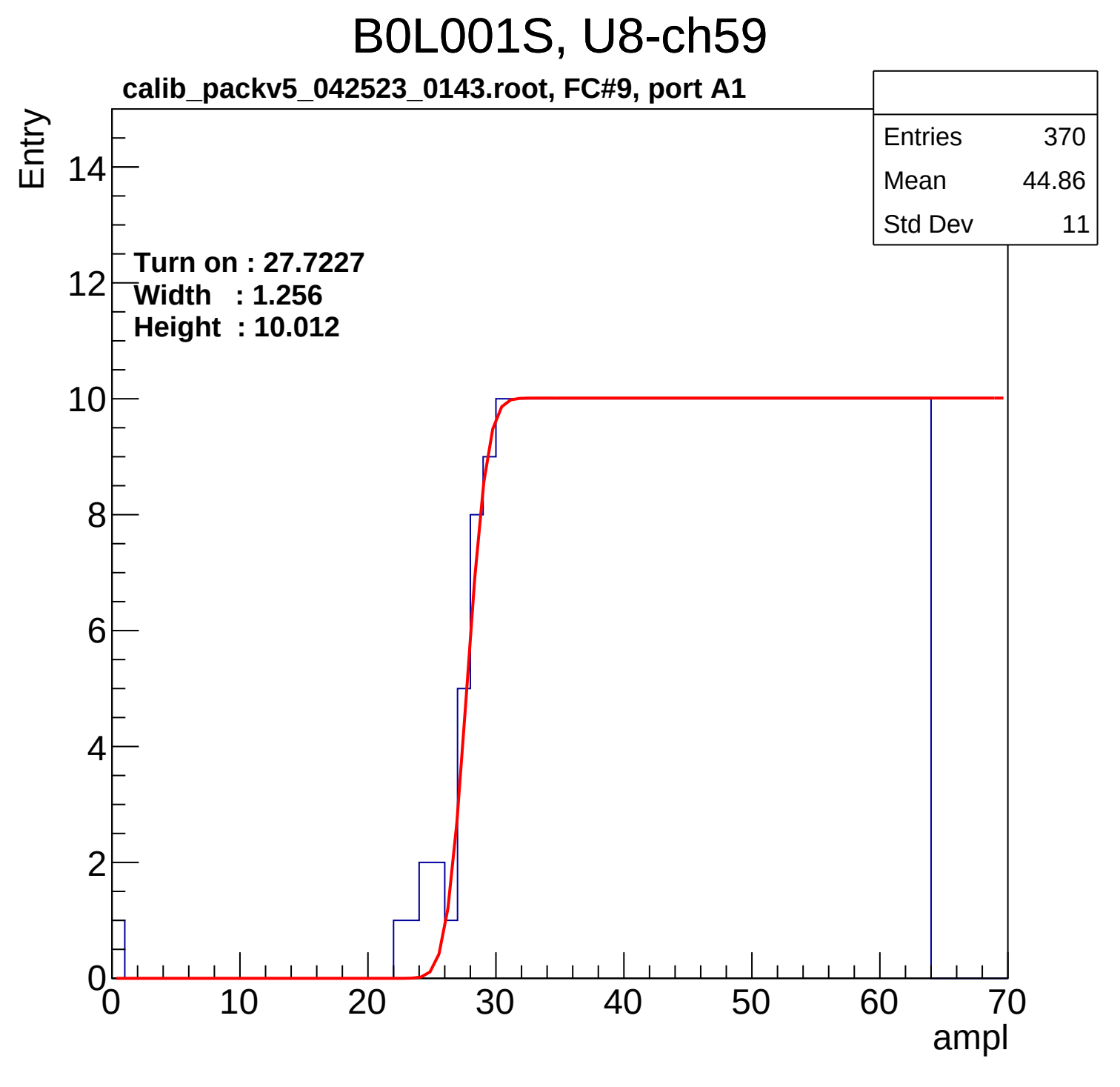
B0L001S, U8-ch59
calib_packv5_042523_0143.root, FC#9, port A1
Entries 370
Mean 44.86
Std Dev 11
Turn on : 27.7227
Width : 1.256
Height : 10.012
Entry
ampl
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6
8
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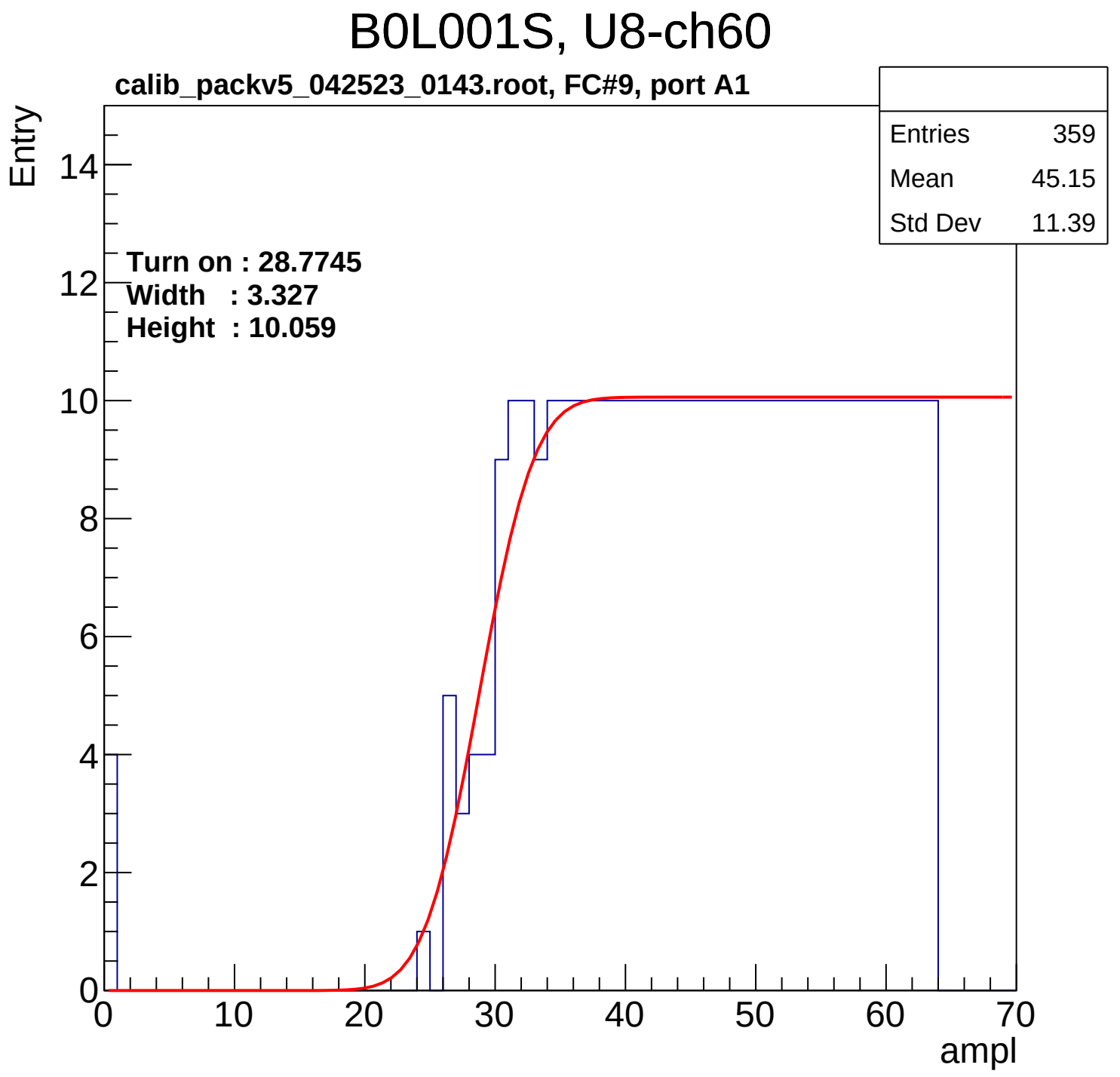
B0L001S, U8-ch60
calib_packv5_042523_0143.root, FC#9, port A1
Entries 359
Mean 45.15
Std Dev 11.39
Turn on : 28.7745
Width : 3.327
Height : 10.059
Entry
ampl
0
2
4
6
8
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0
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60
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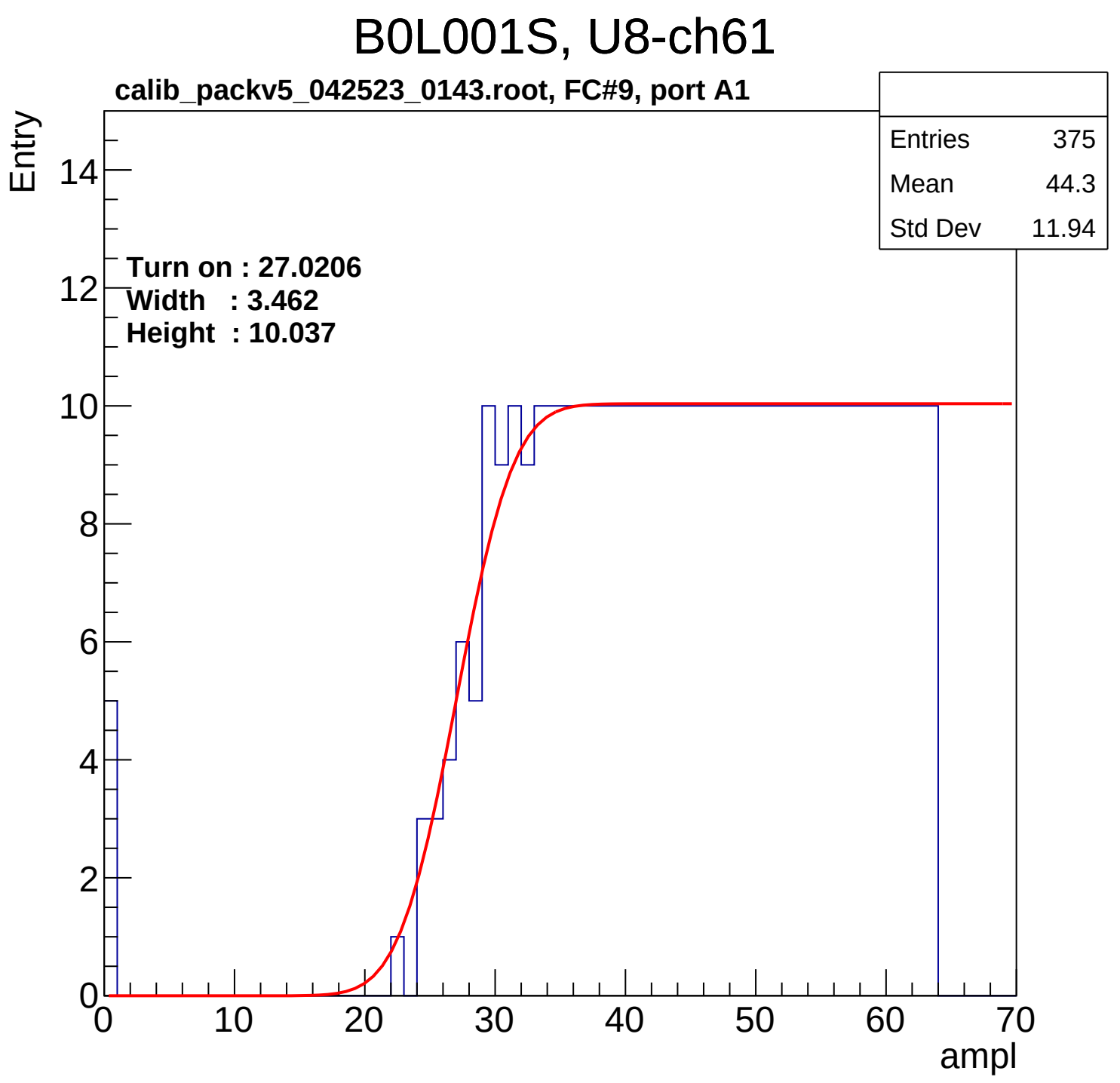
B0L001S, U8-ch61
calib_packv5_042523_0143.root, FC#9, port A1
Entries 375
Mean 44.3
Std Dev 11.94
Turn on : 27.0206
Width : 3.462
Height : 10.037
Entry
ampl
0
2
4
6
8
10
12
14
0
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60
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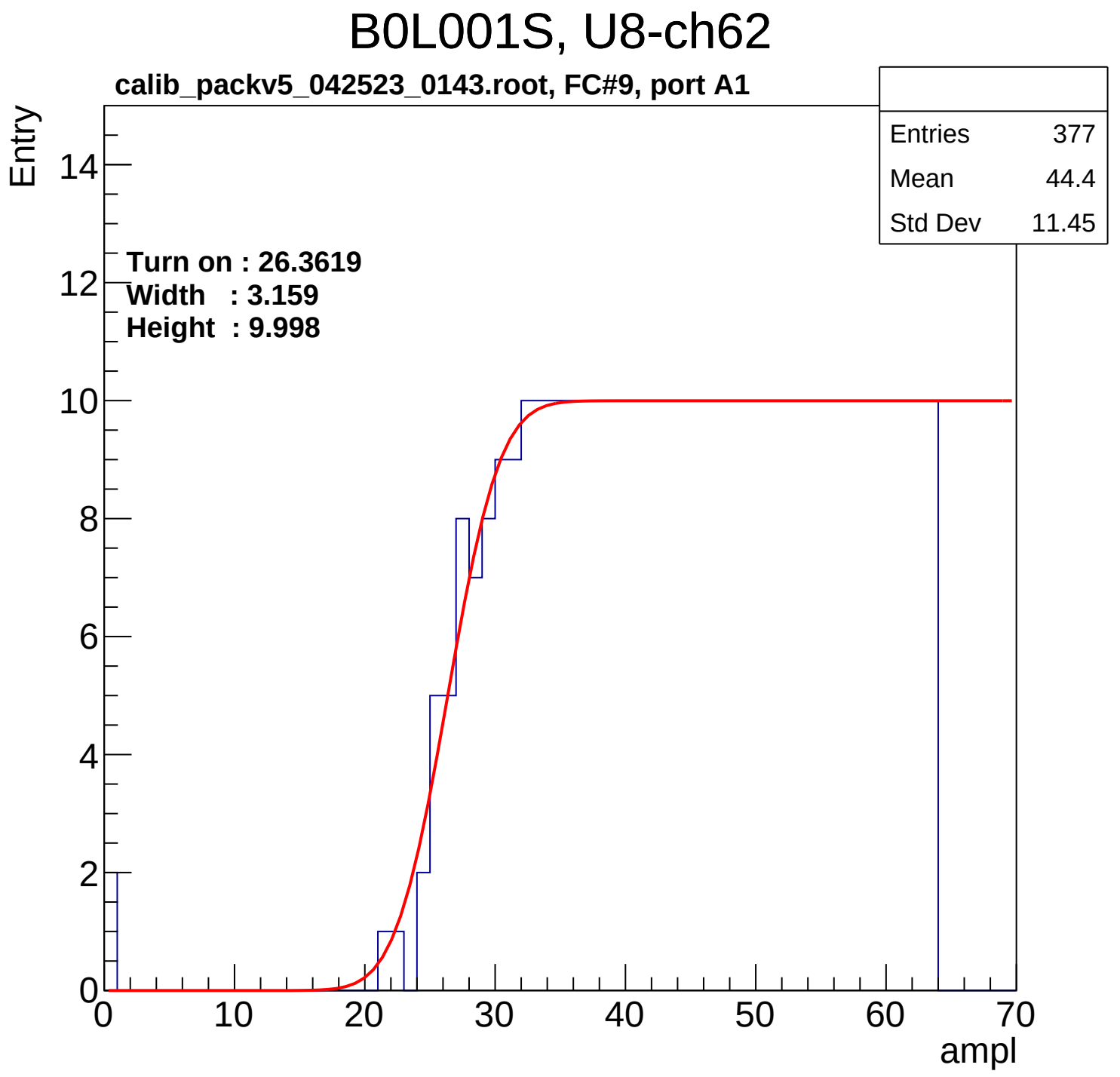
B0L001S, U8-ch62
calib_packv5_042523_0143.root, FC#9, port A1
Entries 377
Mean 44.4
Std Dev 11.45
Turn on : 26.3619
Width : 3.159
Height : 9.998
Entry
ampl
0
2
4
6
8
10
12
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0
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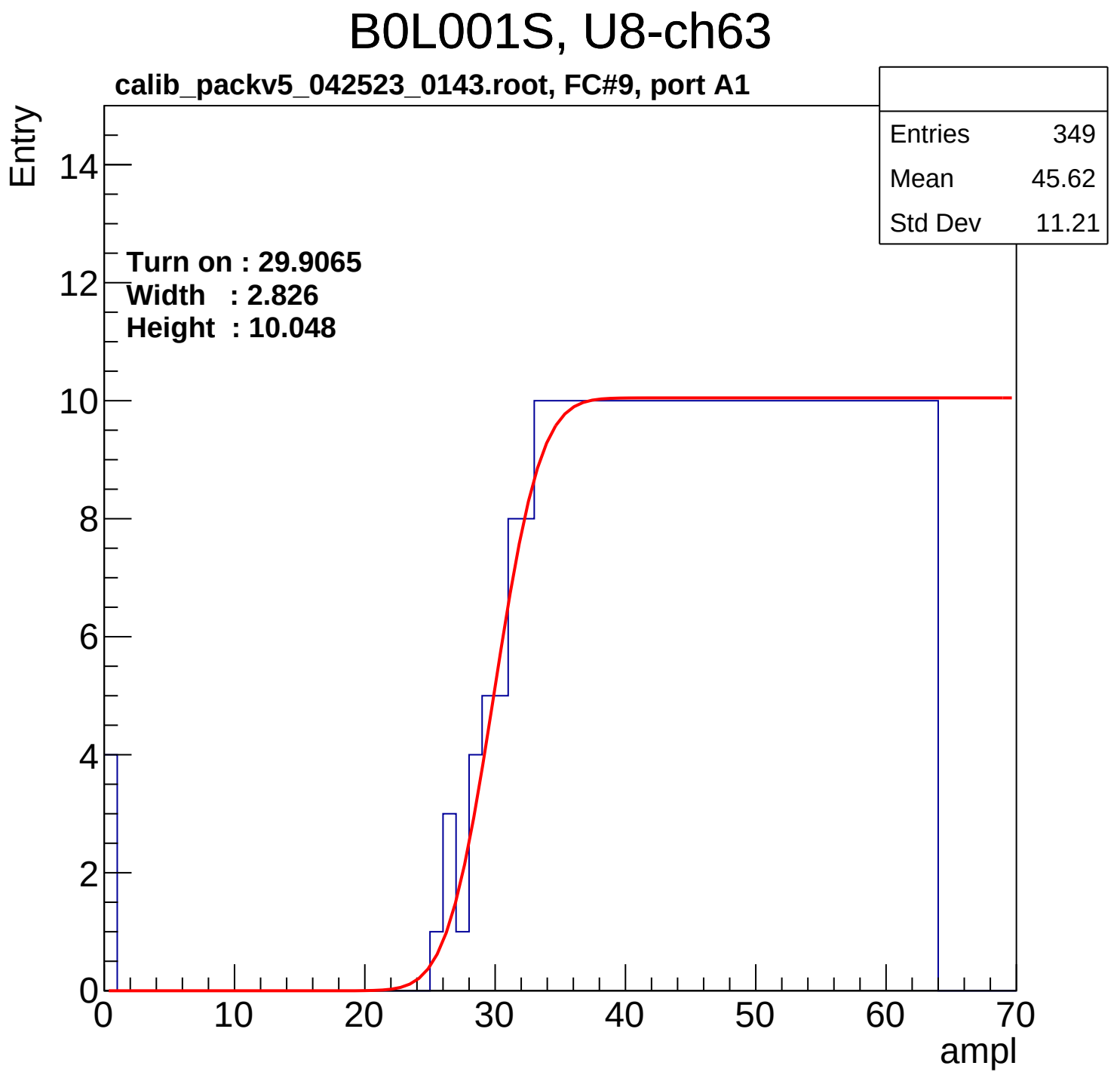
B0L001S, U8-ch63
calib_packv5_042523_0143.root, FC#9, port A1
Entries 349
Mean 45.62
Std Dev 11.21
Turn on : 29.9065
Width : 2.826
Height : 10.048
Entry
ampl
0
2
4
6
8
10
12
14
0
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40
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60
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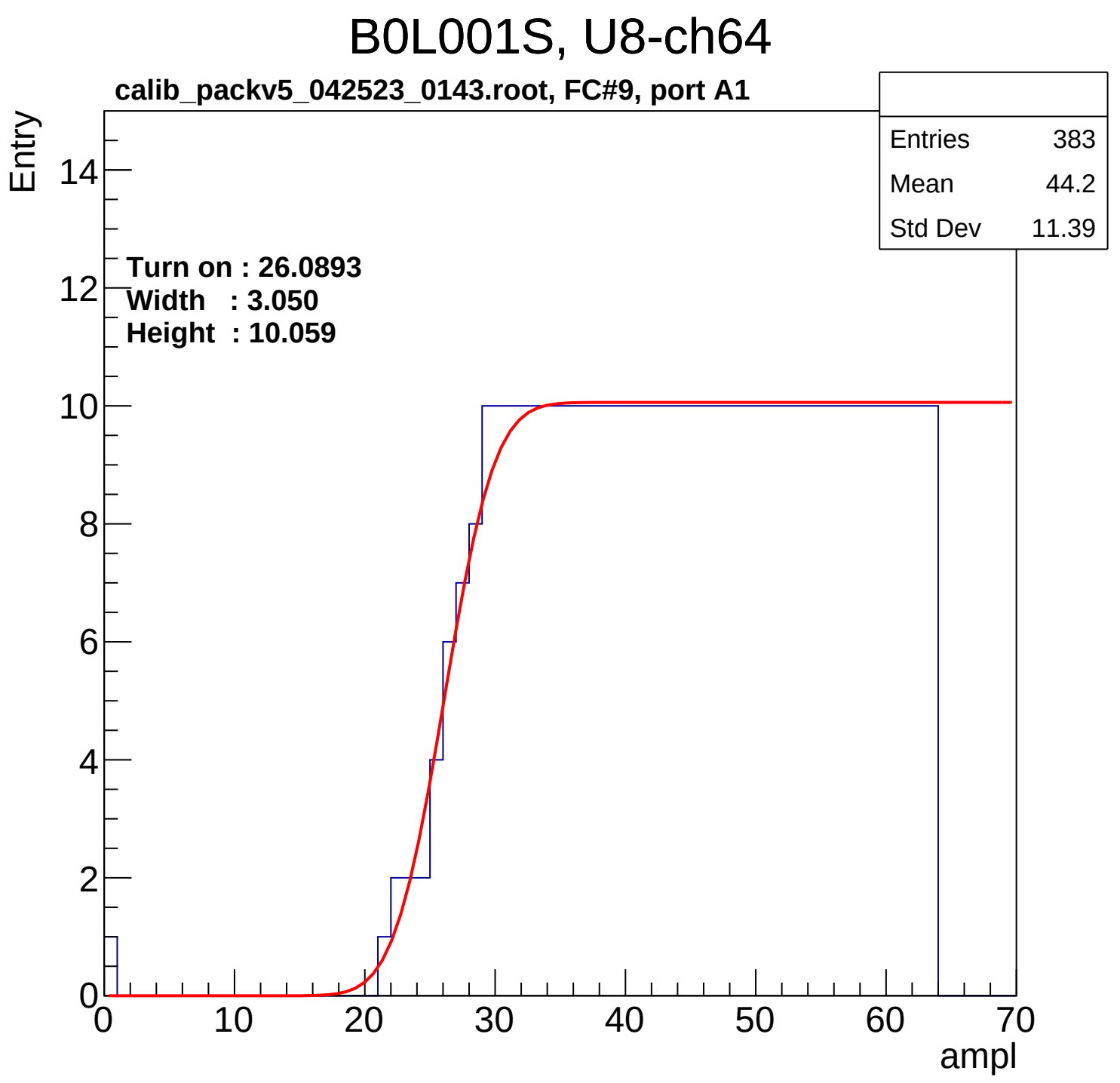
B0L001S, U8-ch64
calib_packv5_042523_0143.root, FC#9, port A1
Entries 383
Mean 44.2
Std Dev 11.39
Turn on : 26.0893
Width : 3.050
Height : 10.059
Entry
ampl
0
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4
6
8
10
12
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0
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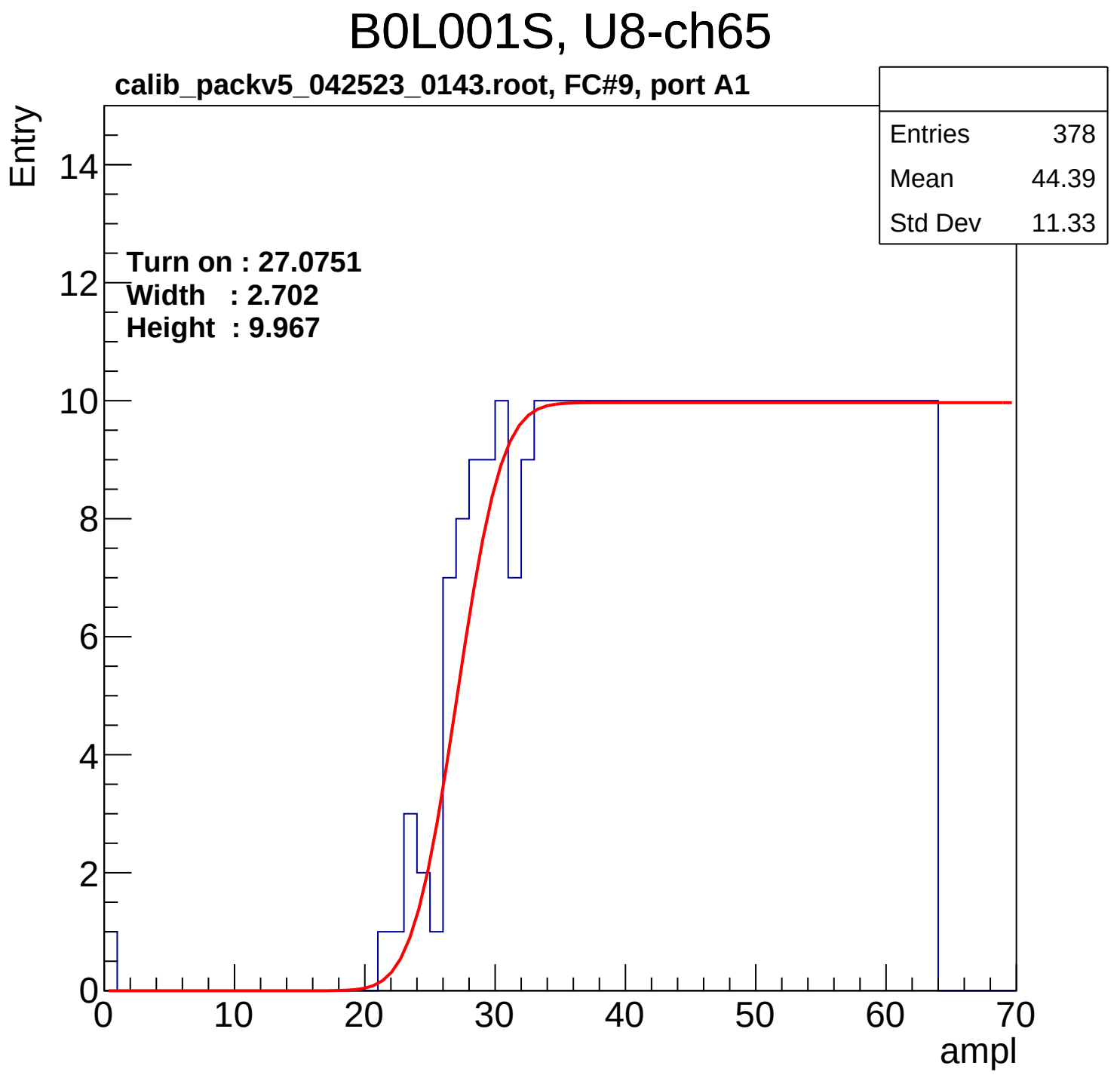
B0L001S, U8-ch65
calib_packv5_042523_0143.root, FC#9, port A1
Entries 378
Mean 44.39
Std Dev 11.33
Turn on : 27.0751
Width : 2.702
Height : 9.967
Entry
ampl
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2
4
6
8
10
12
14
0
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20
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40
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60
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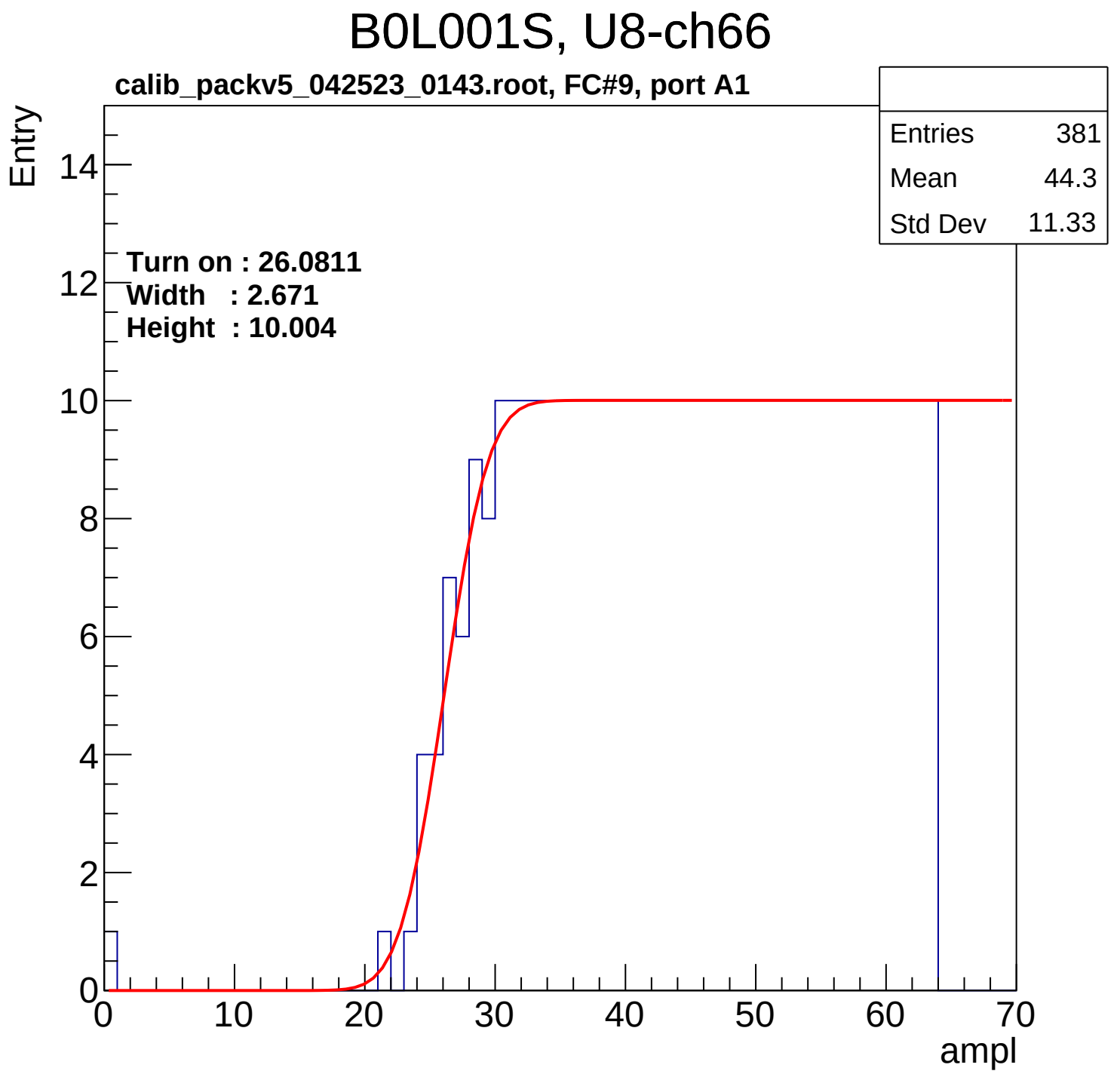
B0L001S, U8-ch66
calib_packv5_042523_0143.root, FC#9, port A1
Entries 381
Mean 44.3
Std Dev 11.33
Turn on : 26.0811
Width : 2.671
Height : 10.004
Entry
ampl
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2
4
6
8
10
12
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0
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60
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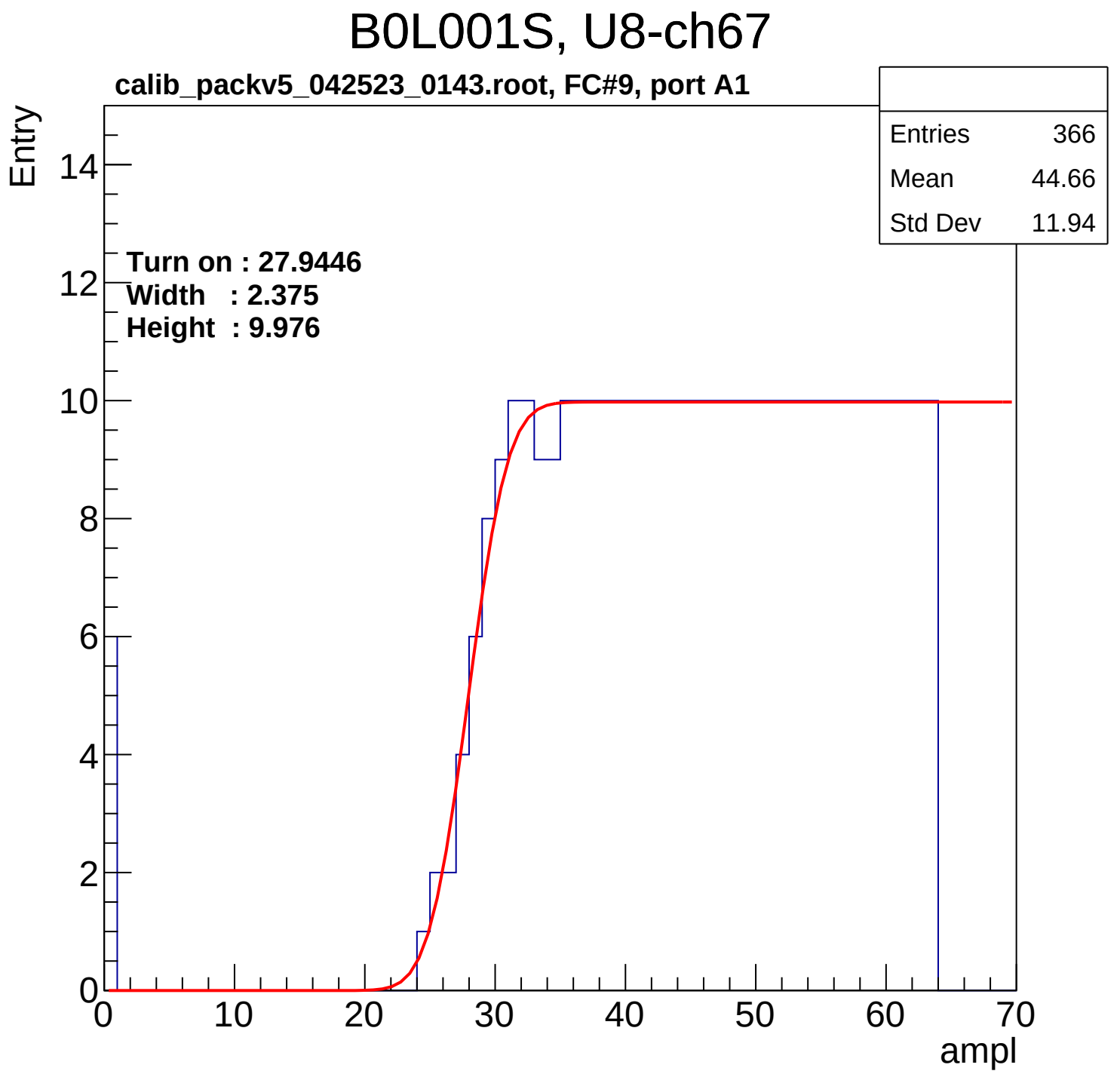
B0L001S, U8-ch67
calib_packv5_042523_0143.root, FC#9, port A1
Entries 366
Mean 44.66
Std Dev 11.94
Turn on : 27.9446
Width : 2.375
Height : 9.976
Entry
ampl
0
2
4
6
8
10
12
14
0
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20
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40
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60
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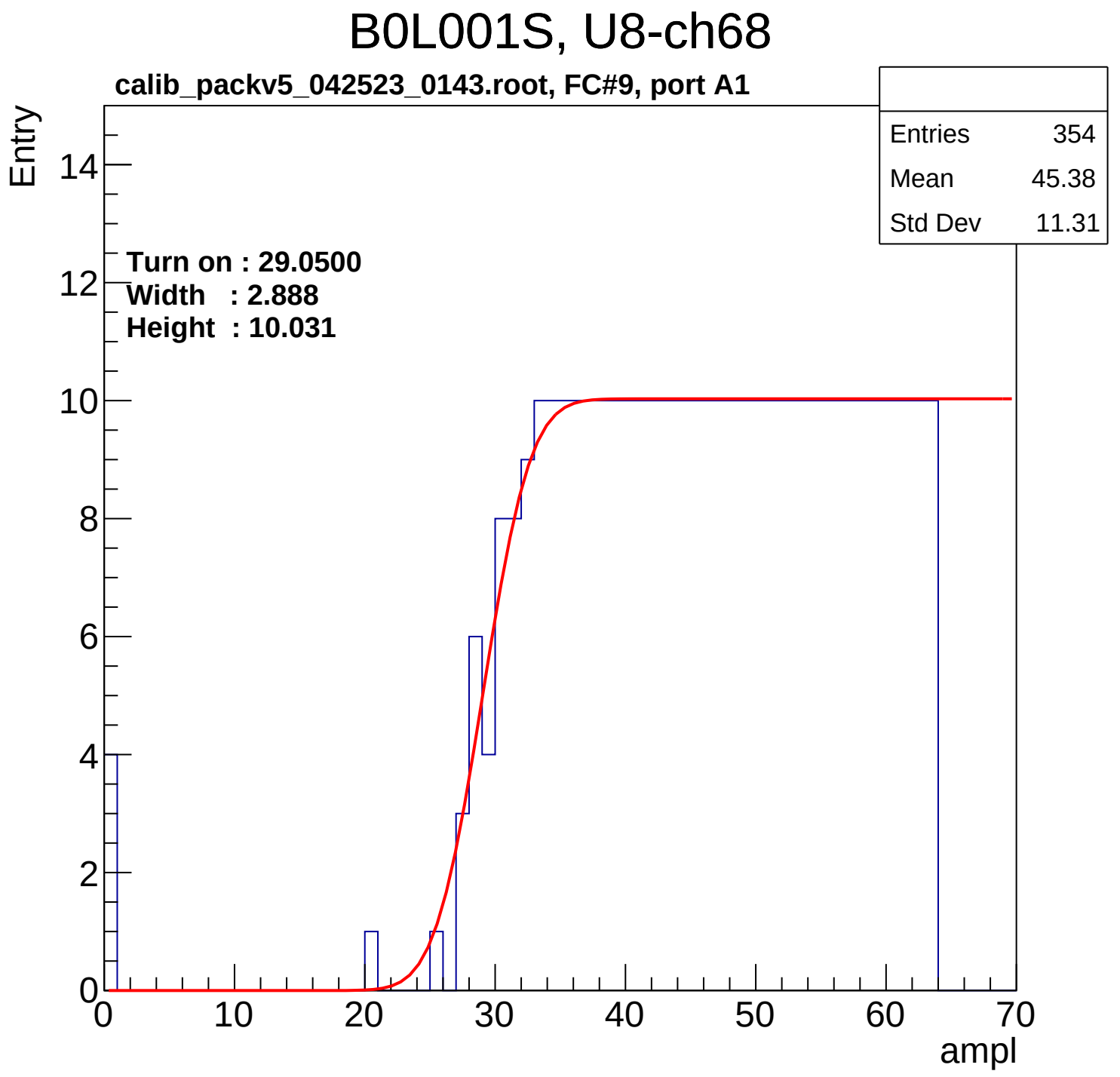
B0L001S, U8-ch68
calib_packv5_042523_0143.root, FC#9, port A1
Entries 354
Mean 45.38
Std Dev 11.31
Turn on : 29.0500
Width : 2.888
Height : 10.031
Entry
ampl
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2
4
6
8
10
12
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0
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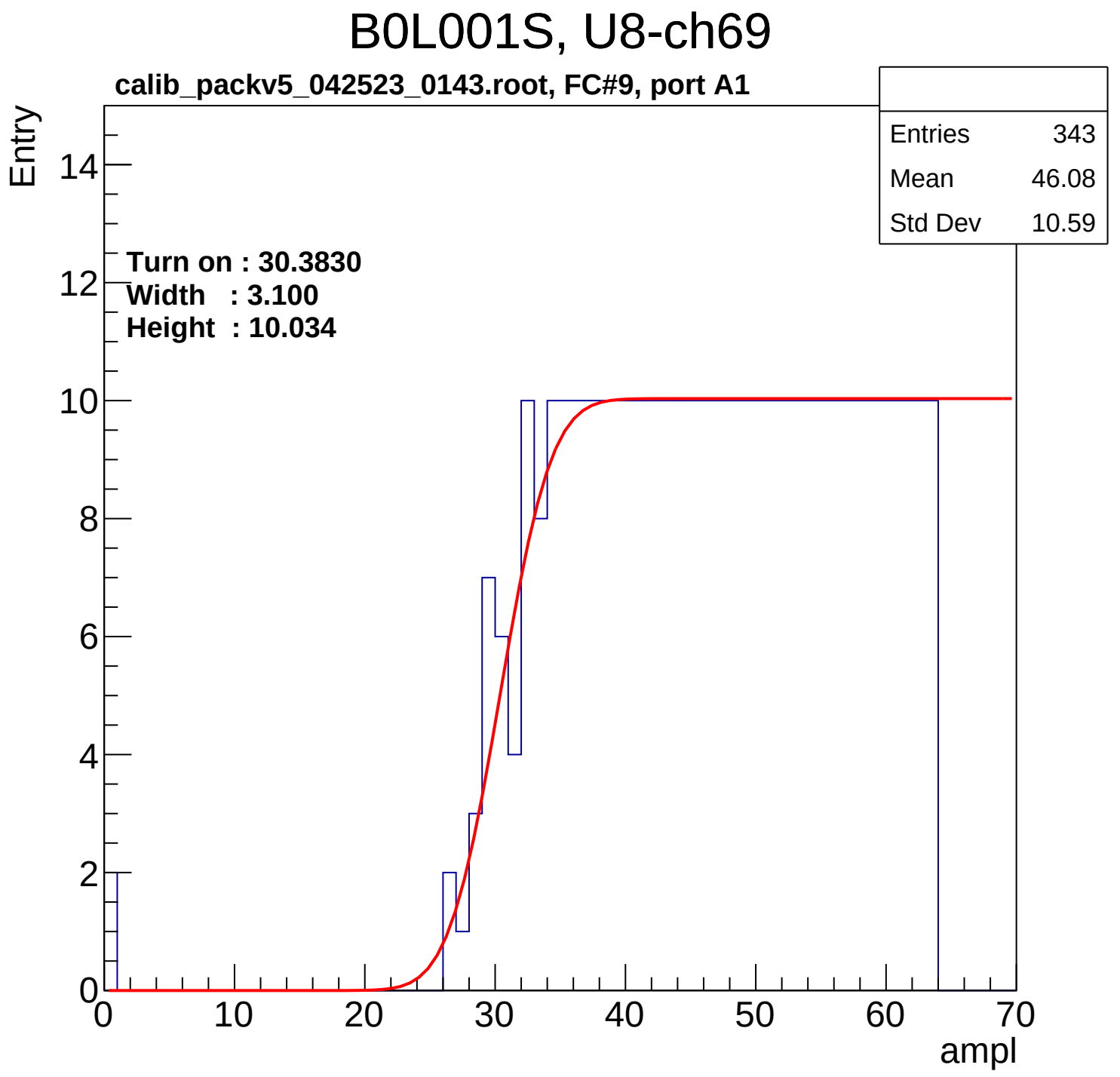
B0L001S, U8-ch69
calib_packv5_042523_0143.root, FC#9, port A1
Entries 343
Mean 46.08
Std Dev 10.59
Turn on : 30.3830
Width : 3.100
Height : 10.034
Entry
ampl
0
2
4
6
8
10
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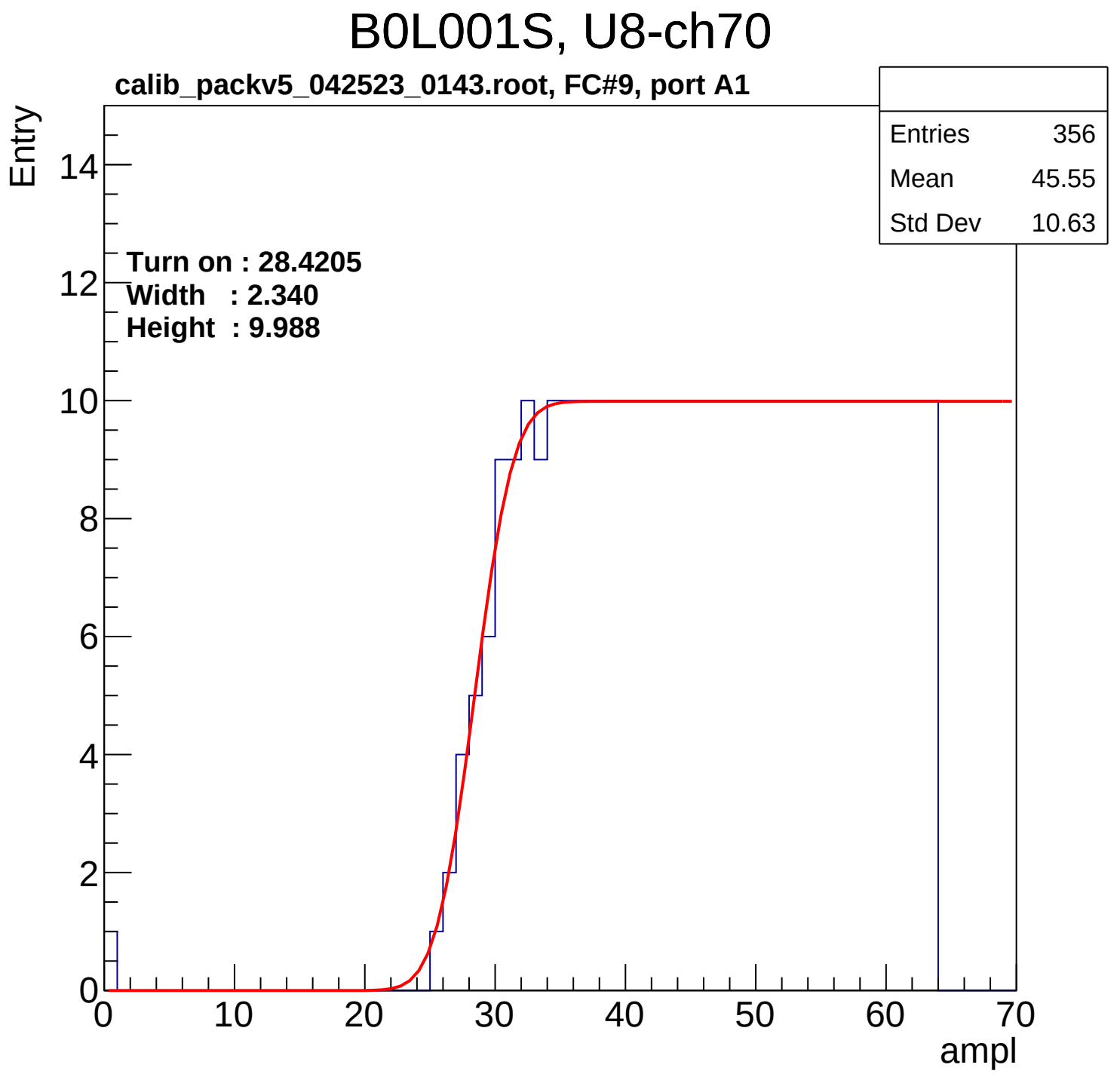
B0L001S, U8-ch70
calib_packv5_042523_0143.root, FC#9, port A1
Entries 356
Mean 45.55
Std Dev 10.63
Turn on : 28.4205
Width : 2.340
Height : 9.988
Entry
ampl
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2
4
6
8
10
12
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0
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20
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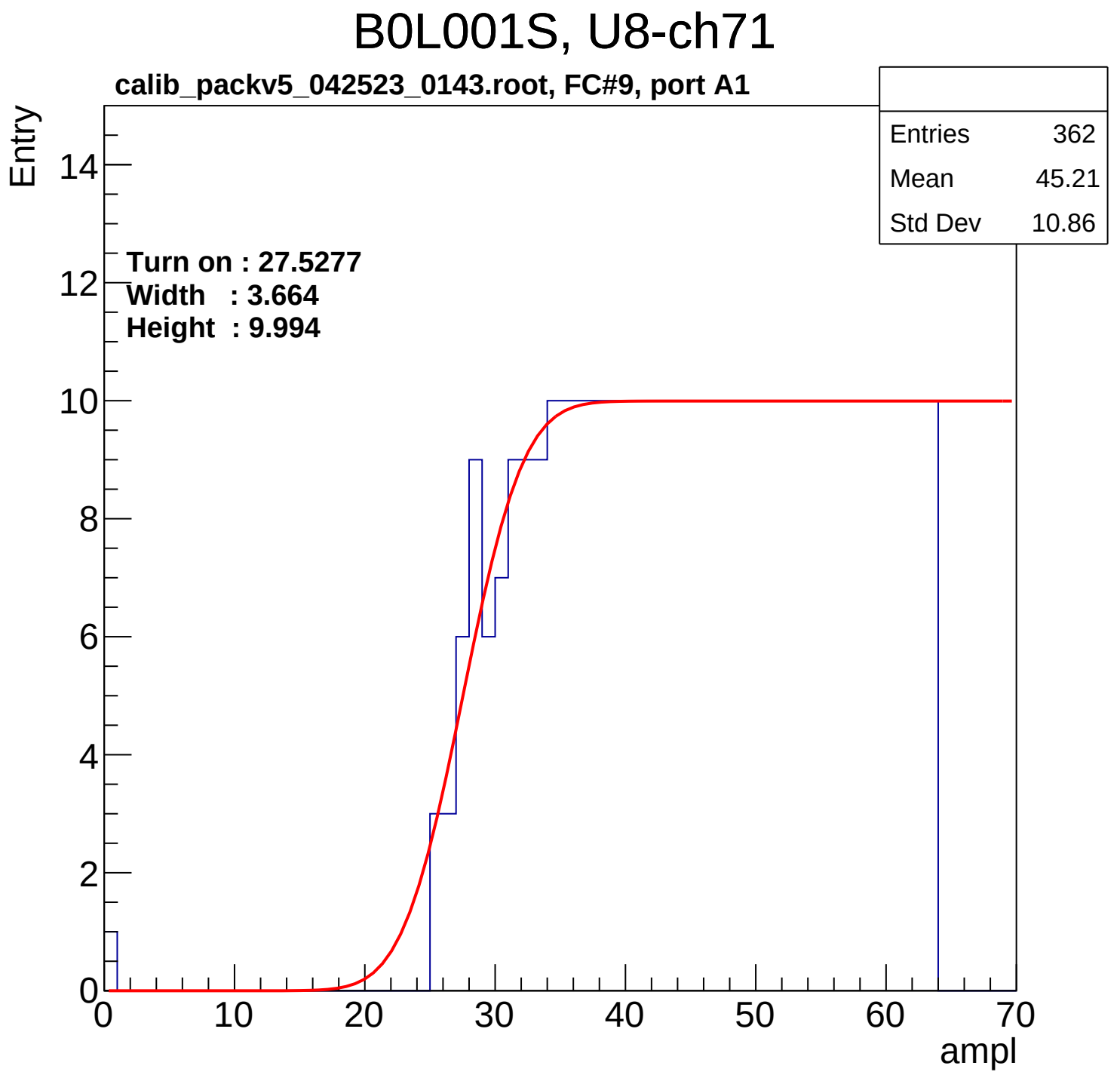
B0L001S, U8-ch71
calib_packv5_042523_0143.root, FC#9, port A1
Entries 362
Mean 45.21
Std Dev 10.86
Turn on : 27.5277
Width : 3.664
Height : 9.994
Entry
ampl
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2
4
6
8
10
12
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0
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20
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60
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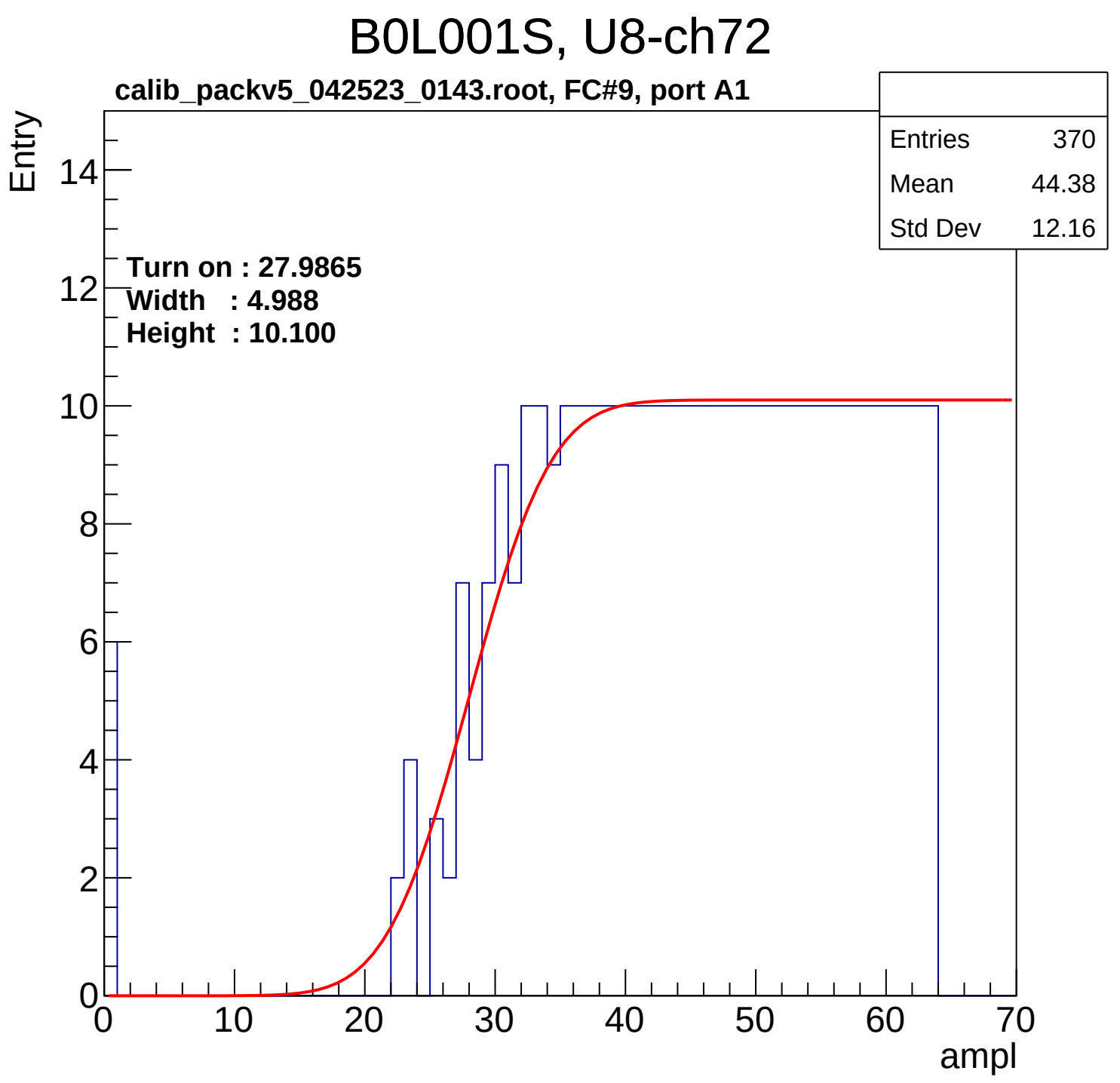
B0L001S, U8-ch72
calib_packv5_042523_0143.root, FC#9, port A1
Entries 370
Mean 44.38
Std Dev 12.16
Turn on : 27.9865
Width : 4.988
Height : 10.100
Entry
ampl
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4
6
8
10
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60
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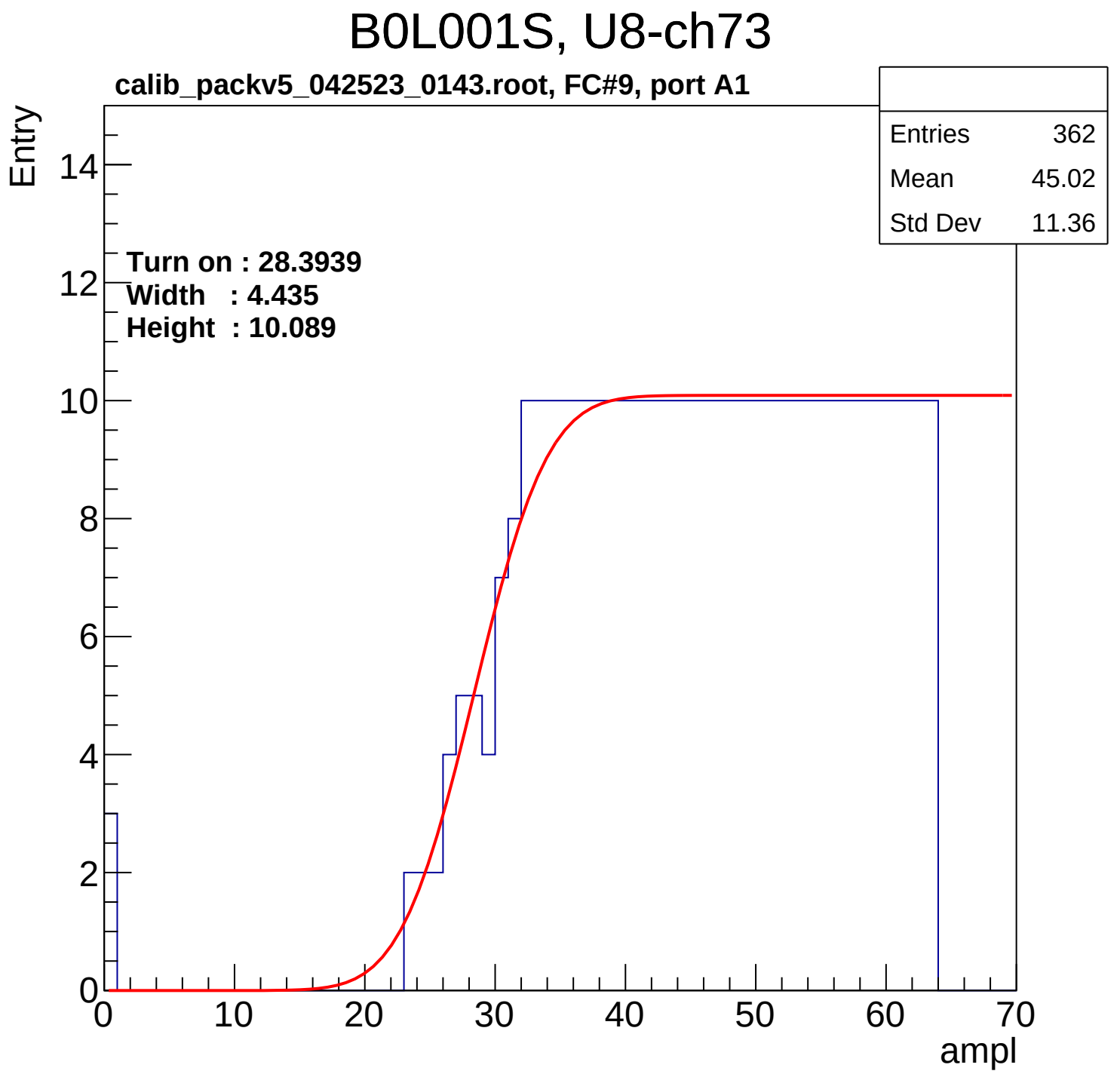
B0L001S, U8-ch73
calib_packv5_042523_0143.root, FC#9, port A1
Entries 362
Mean 45.02
Std Dev 11.36
Turn on : 28.3939
Width : 4.435
Height : 10.089
Entry
ampl
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6
8
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12
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0
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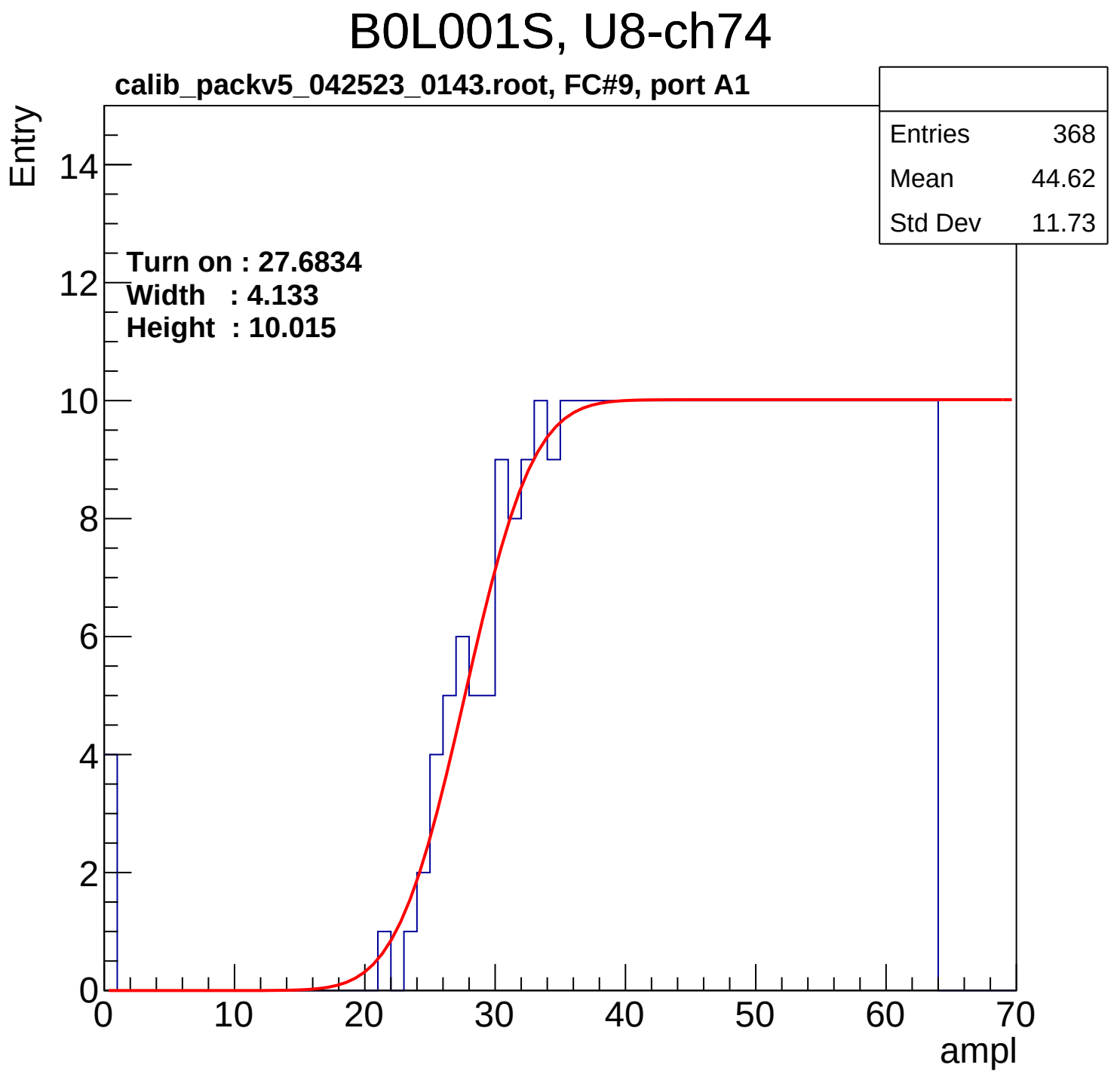
B0L001S, U8-ch74
calib_packv5_042523_0143.root, FC#9, port A1
Entries 368
Mean 44.62
Std Dev 11.73
Turn on : 27.6834
Width : 4.133
Height : 10.015
Entry
ampl
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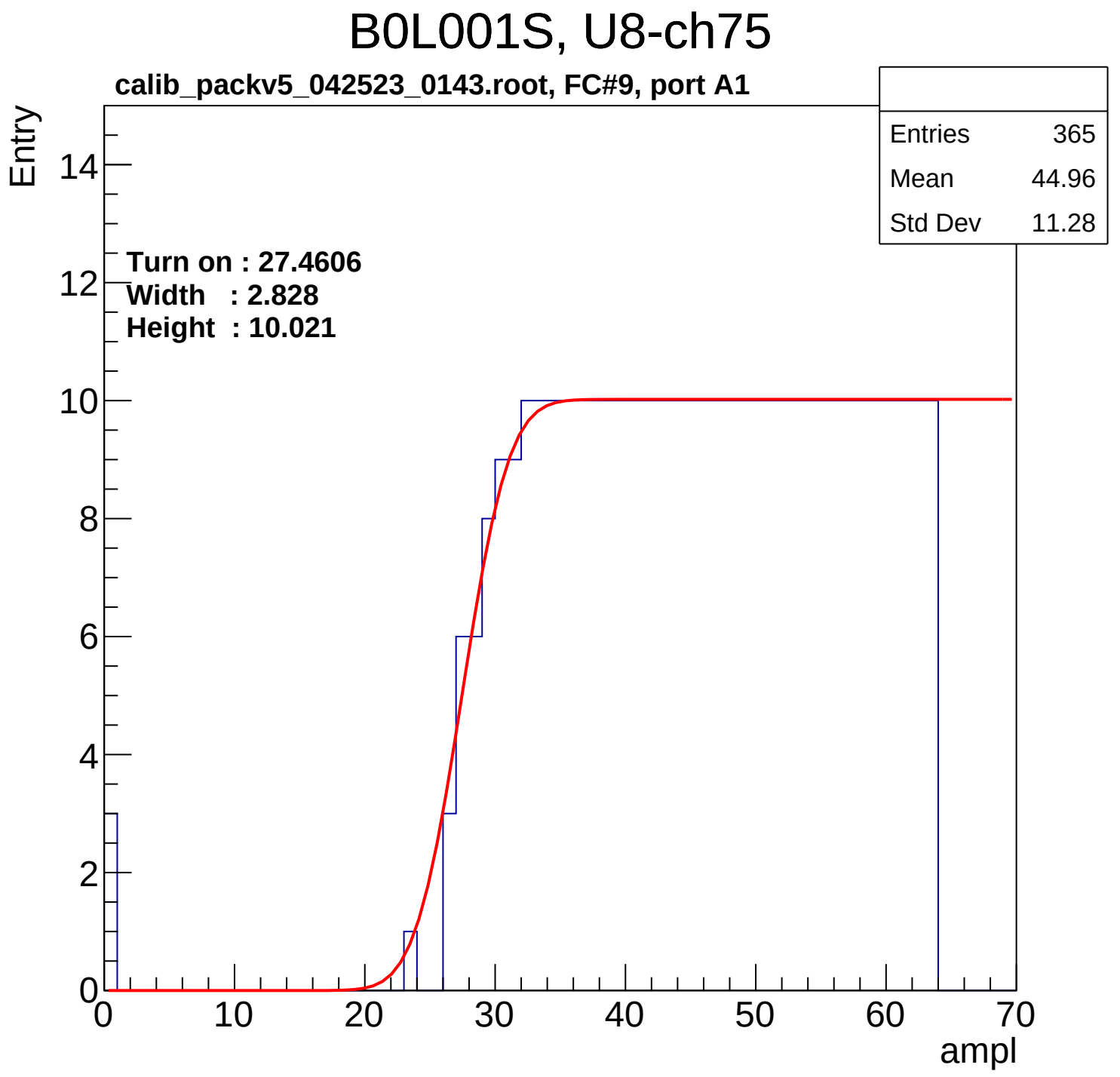
B0L001S, U8-ch75
calib_packv5_042523_0143.root, FC#9, port A1
Entries 365
Mean 44.96
Std Dev 11.28
Turn on : 27.4606
Width : 2.828
Height : 10.021
Entry
ampl
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8
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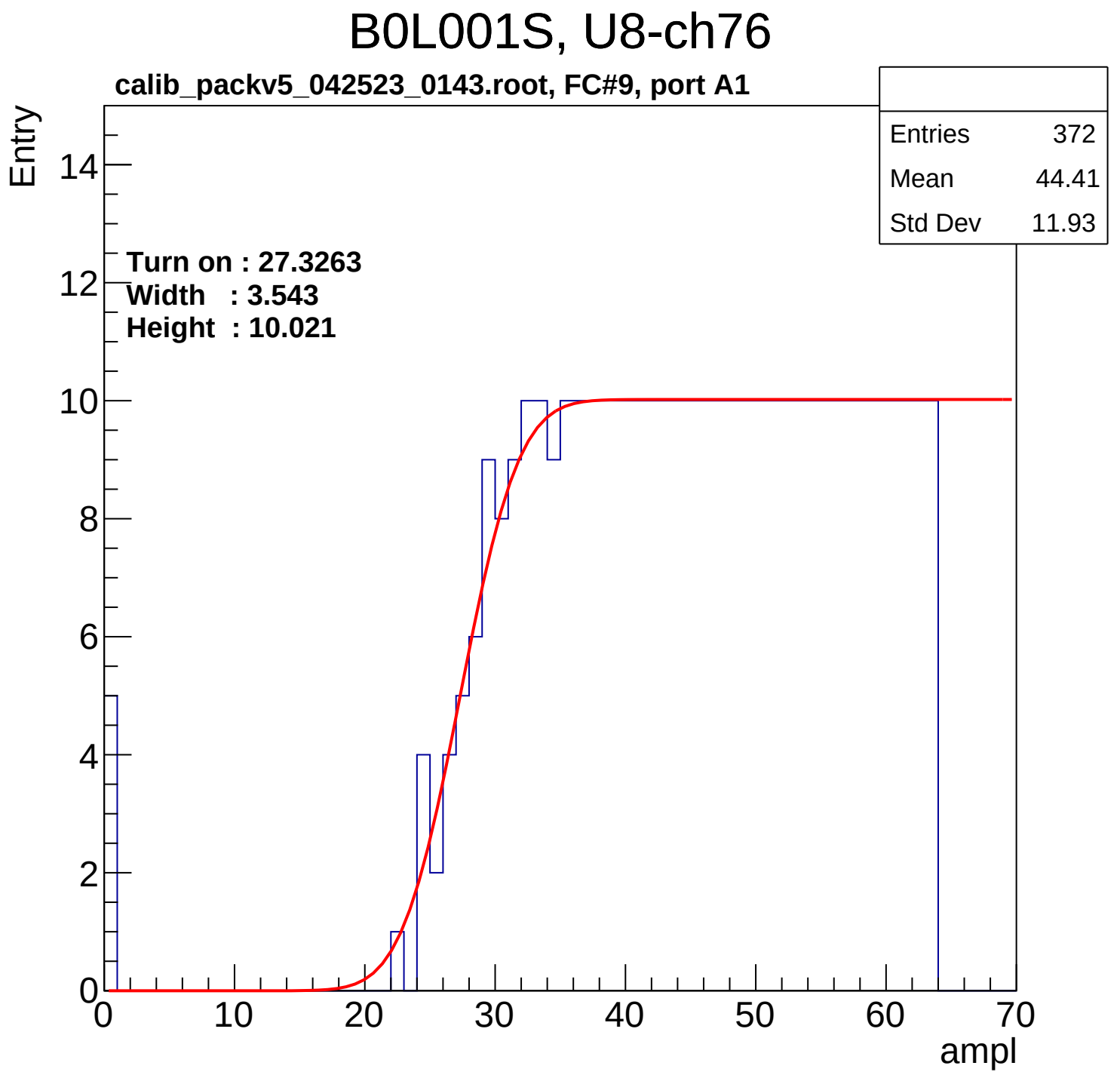
B0L001S, U8-ch76
calib_packv5_042523_0143.root, FC#9, port A1
Entries 372
Mean 44.41
Std Dev 11.93
Turn on : 27.3263
Width : 3.543
Height : 10.021
Entry
ampl
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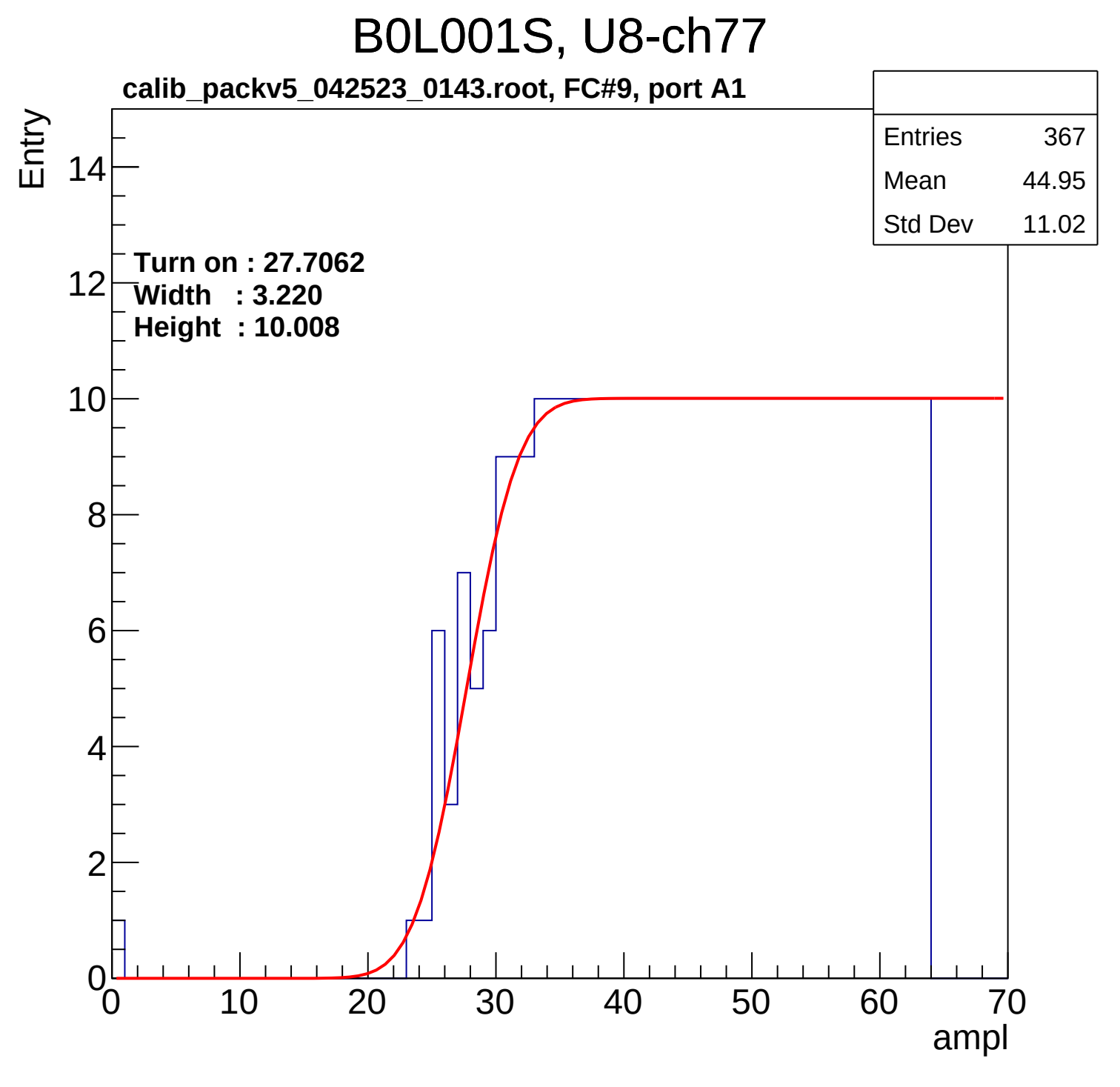
B0L001S, U8-ch77
calib_packv5_042523_0143.root, FC#9, port A1
Entries 367
Mean 44.95
Std Dev 11.02
Turn on : 27.7062
Width : 3.220
Height : 10.008
Entry
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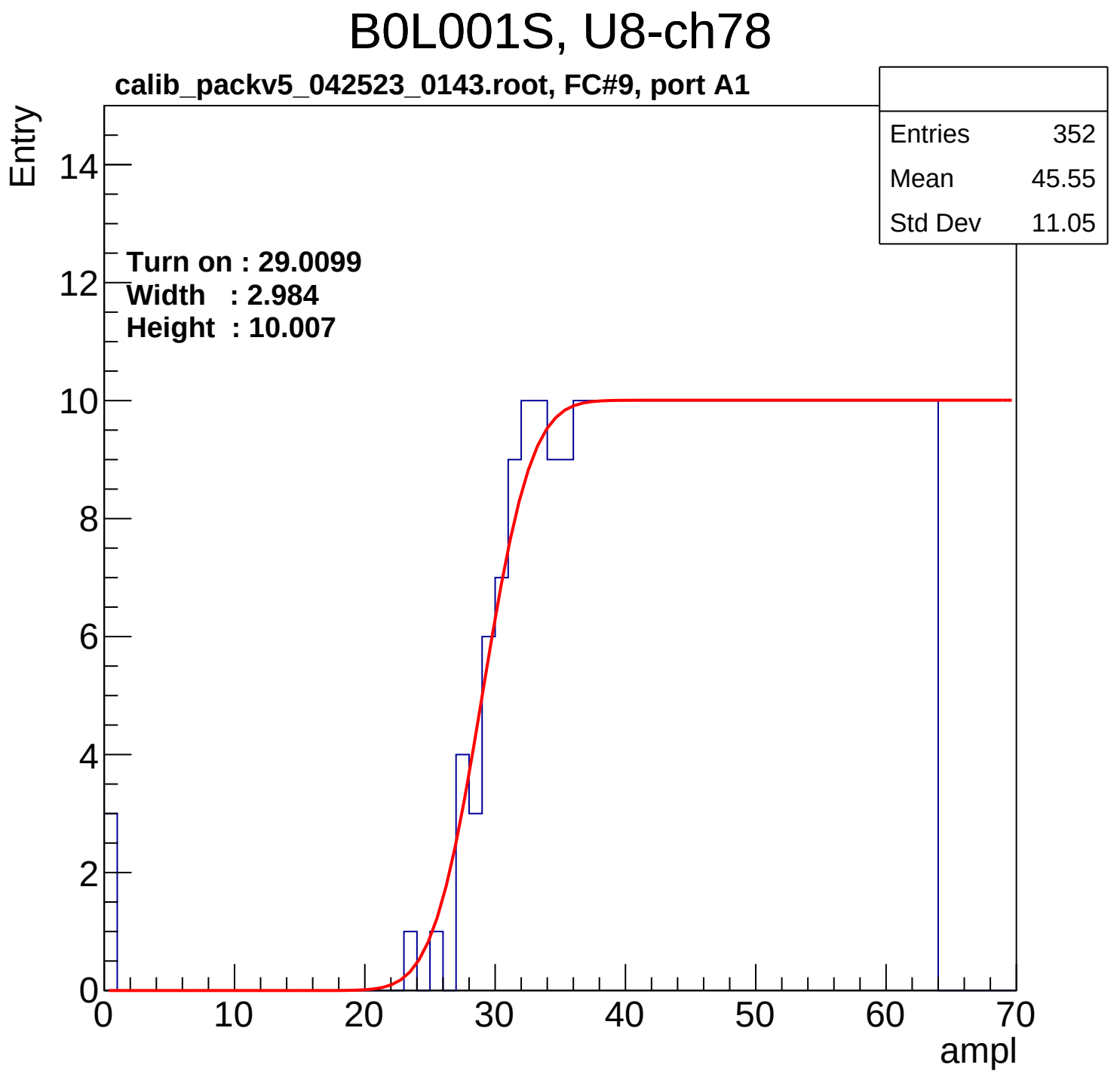
B0L001S, U8-ch78
calib_packv5_042523_0143.root, FC#9, port A1
Entries 352
Mean 45.55
Std Dev 11.05
Turn on : 29.0099
Width : 2.984
Height : 10.007
Entry
ampl
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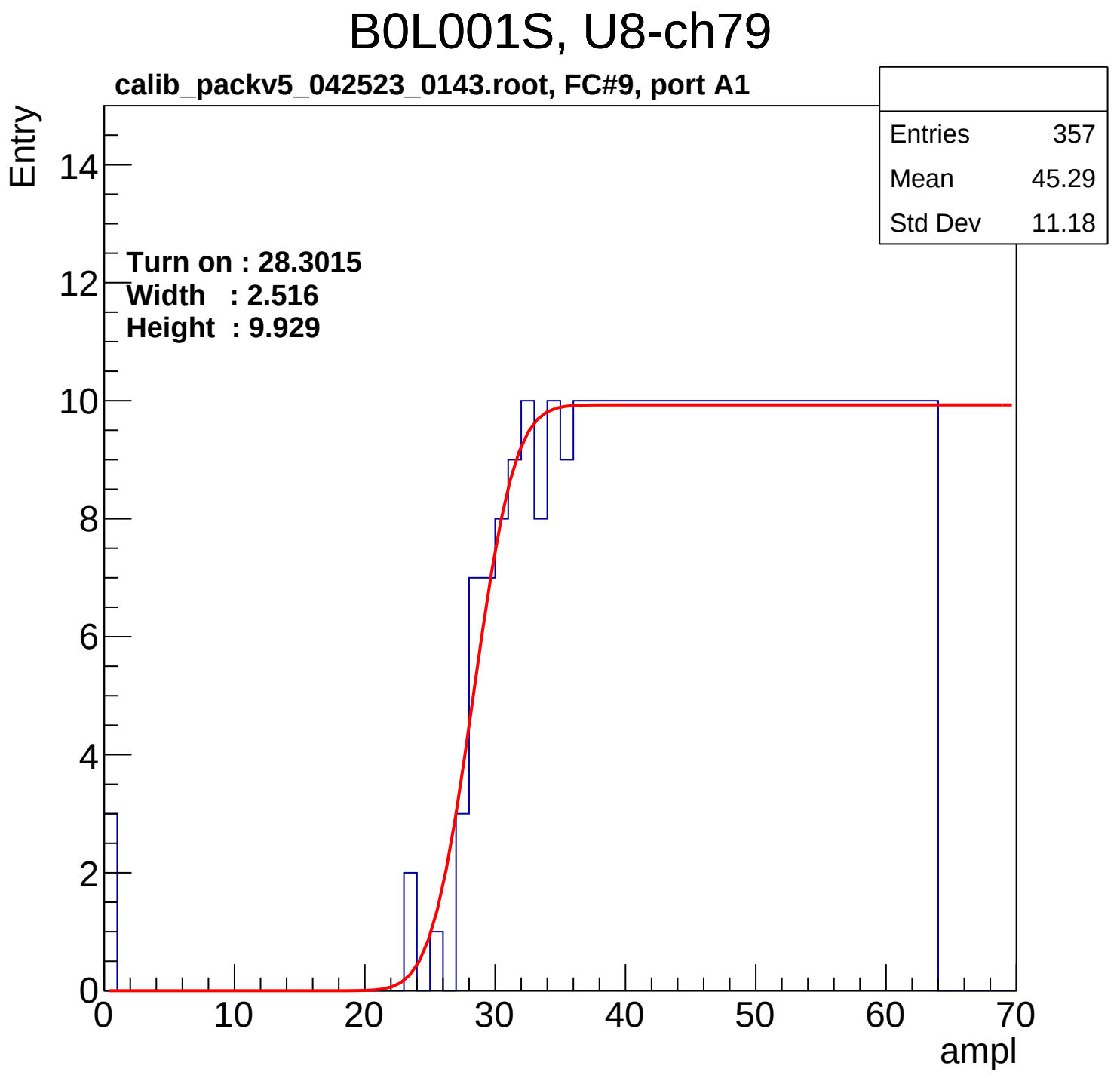
B0L001S, U8-ch79
calib_packv5_042523_0143.root, FC#9, port A1
Entries 357
Mean 45.29
Std Dev 11.18
Turn on : 28.3015
Width : 2.516
Height : 9.929
Entry
ampl
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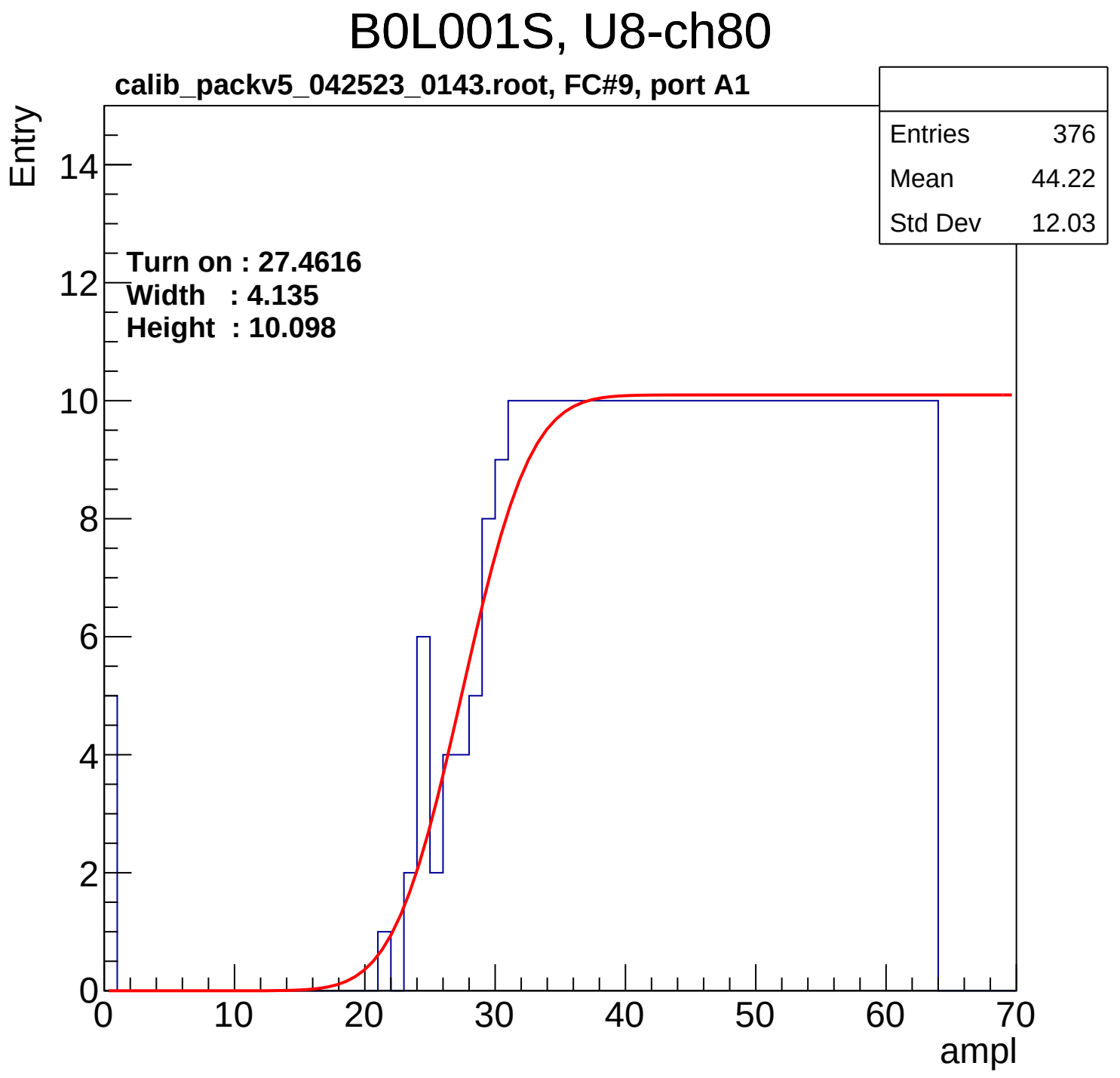
B0L001S, U8-ch80
calib_packv5_042523_0143.root, FC#9, port A1
Entries 376
Mean 44.22
Std Dev 12.03
Turn on : 27.4616
Width : 4.135
Height : 10.098
Entry
ampl
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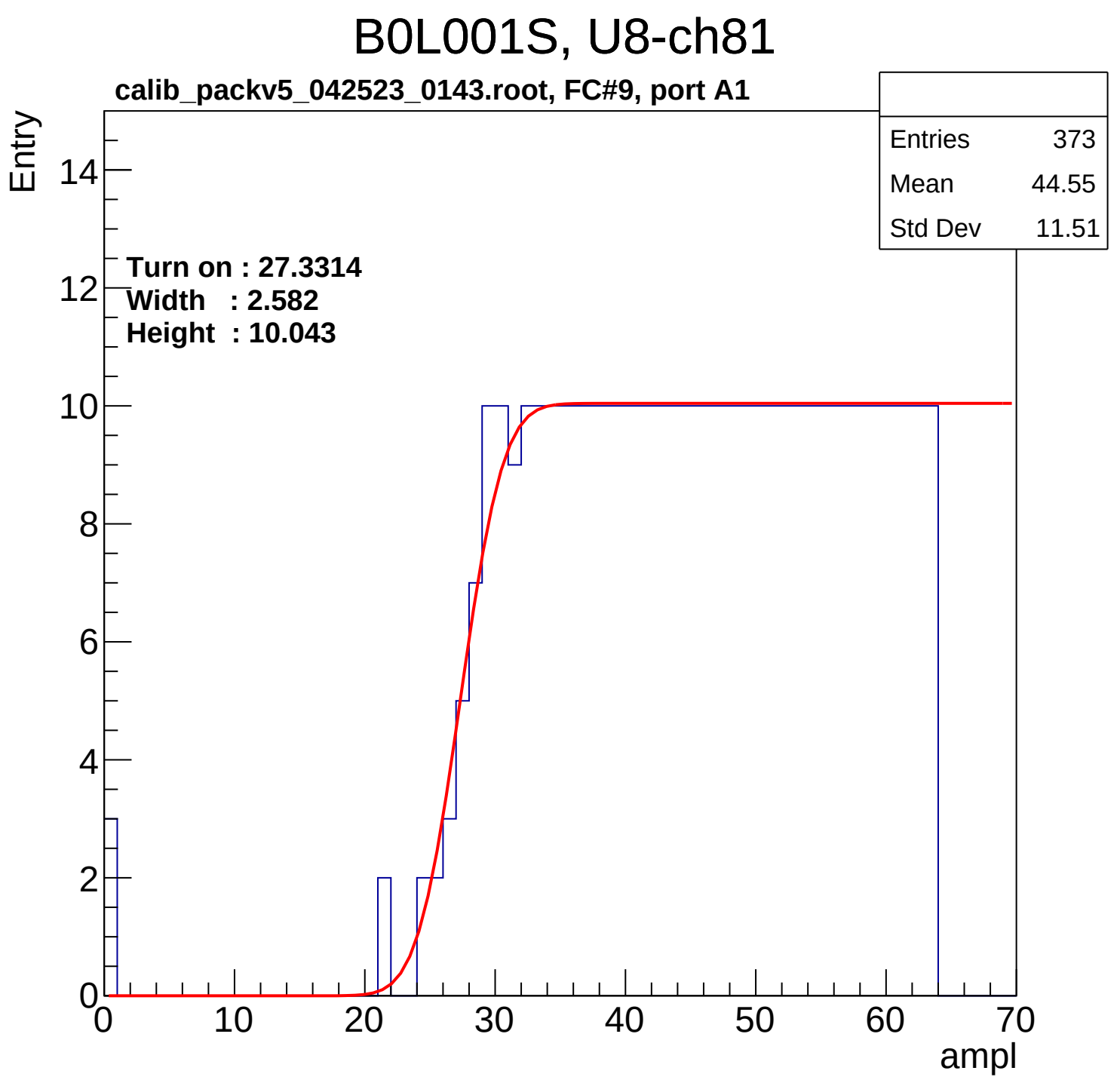
B0L001S, U8-ch81
calib_packv5_042523_0143.root, FC#9, port A1
Entries 373
Mean 44.55
Std Dev 11.51
Turn on : 27.3314
Width : 2.582
Height : 10.043
Entry
ampl
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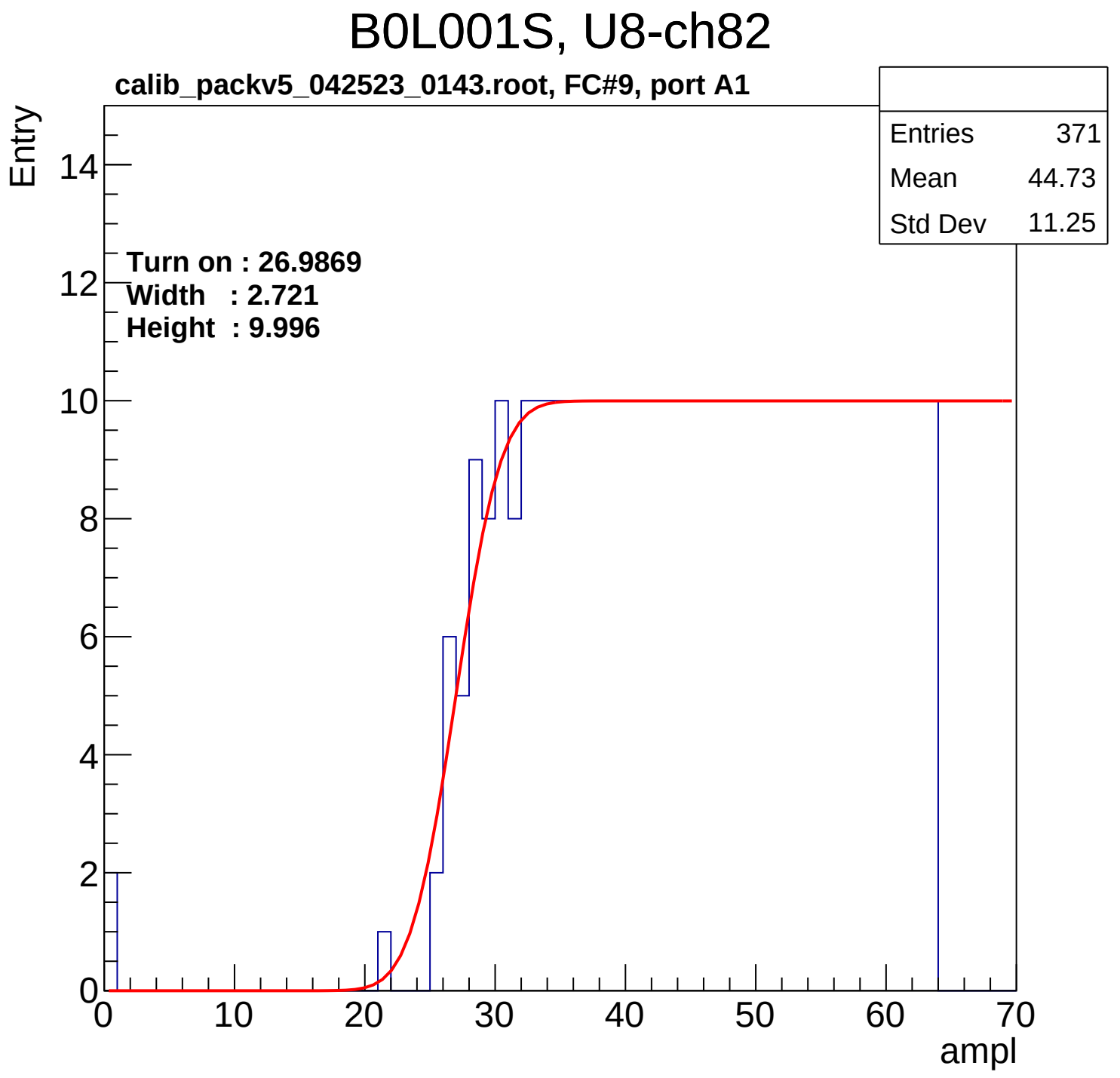
B0L001S, U8-ch82
calib_packv5_042523_0143.root, FC#9, port A1
Entries 371
Mean 44.73
Std Dev 11.25
Turn on : 26.9869
Width : 2.721
Height : 9.996
Entry
ampl
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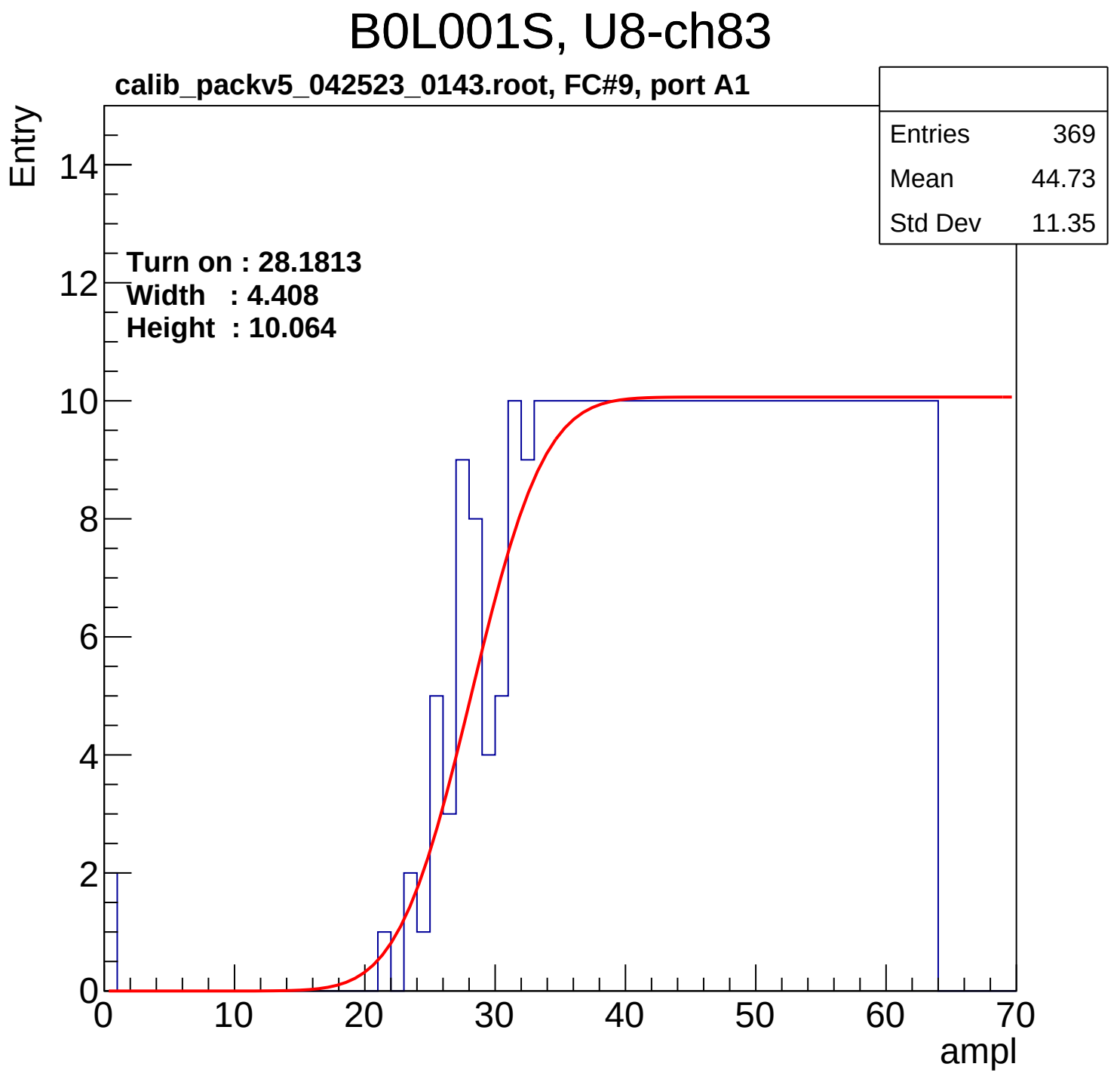
B0L001S, U8-ch83
calib_packv5_042523_0143.root, FC#9, port A1
Entries 369
Mean 44.73
Std Dev 11.35
Turn on : 28.1813
Width : 4.408
Height : 10.064
Entry
ampl
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6
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10
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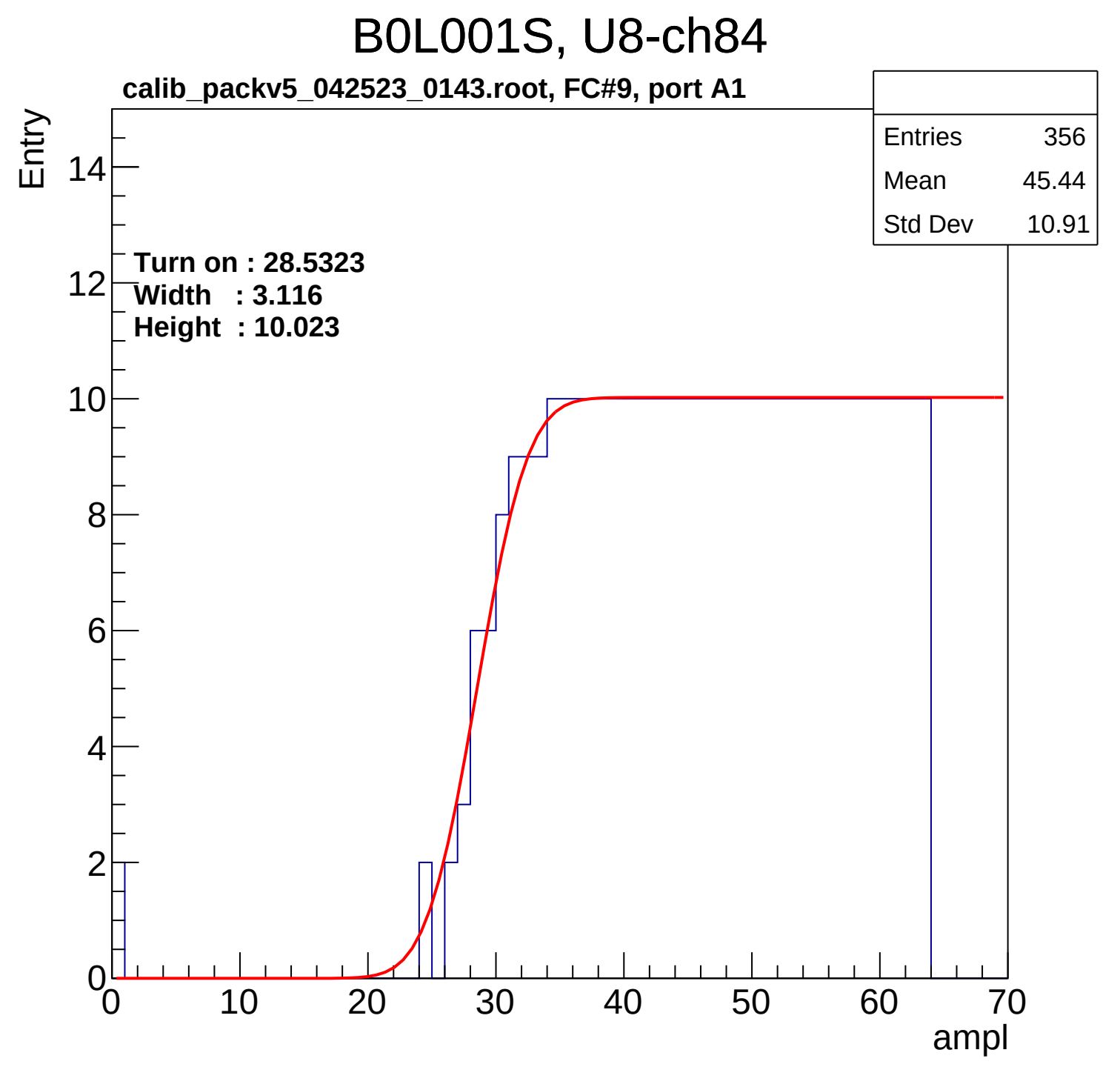
B0L001S, U8-ch84
calib_packv5_042523_0143.root, FC#9, port A1
Entries 356
Mean 45.44
Std Dev 10.91
Turn on : 28.5323
Width : 3.116
Height : 10.023
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ampl
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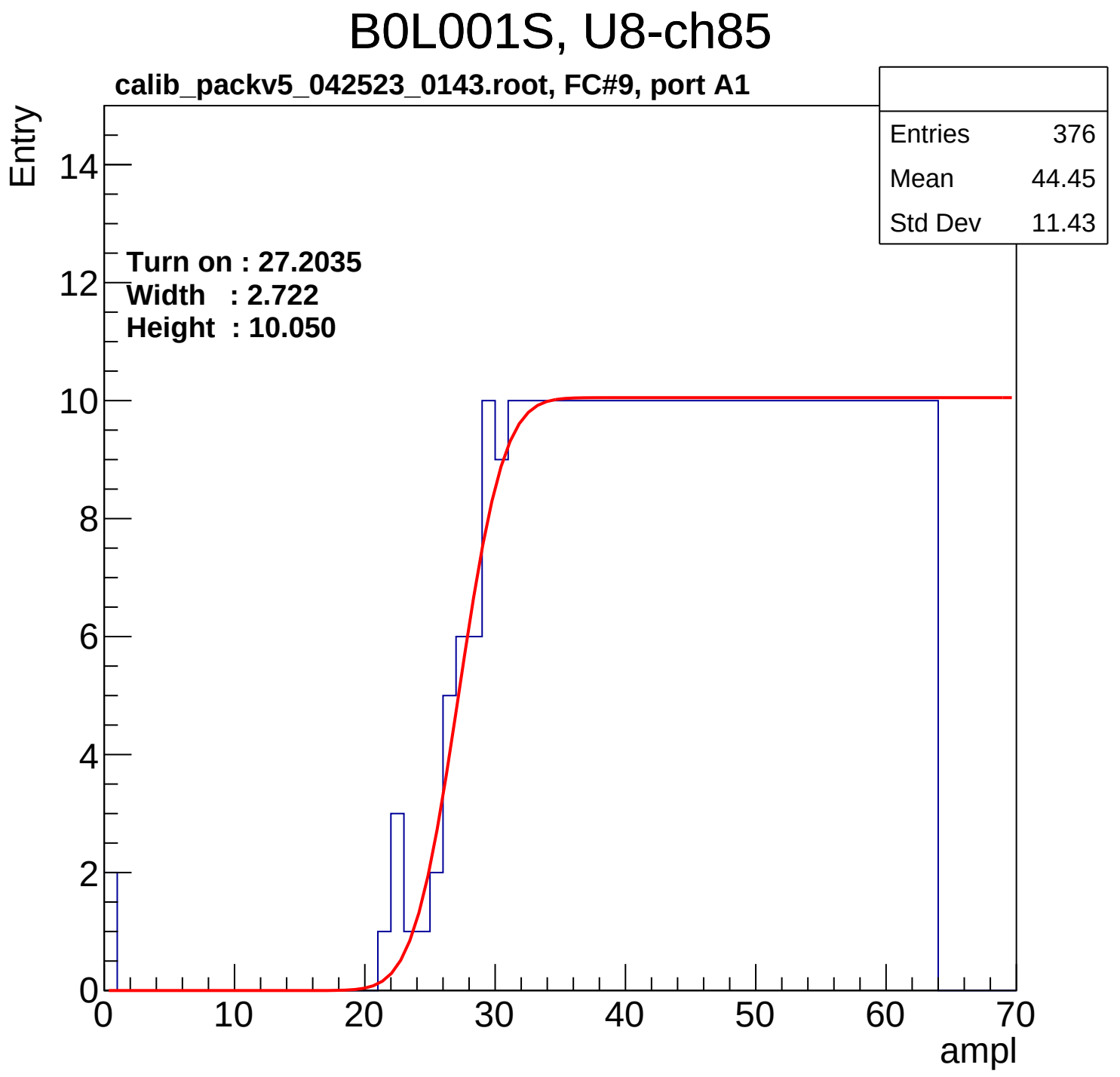
B0L001S, U8-ch85
calib_packv5_042523_0143.root, FC#9, port A1
Entries 376
Mean 44.45
Std Dev 11.43
Turn on : 27.2035
Width : 2.722
Height : 10.050
Entry
ampl
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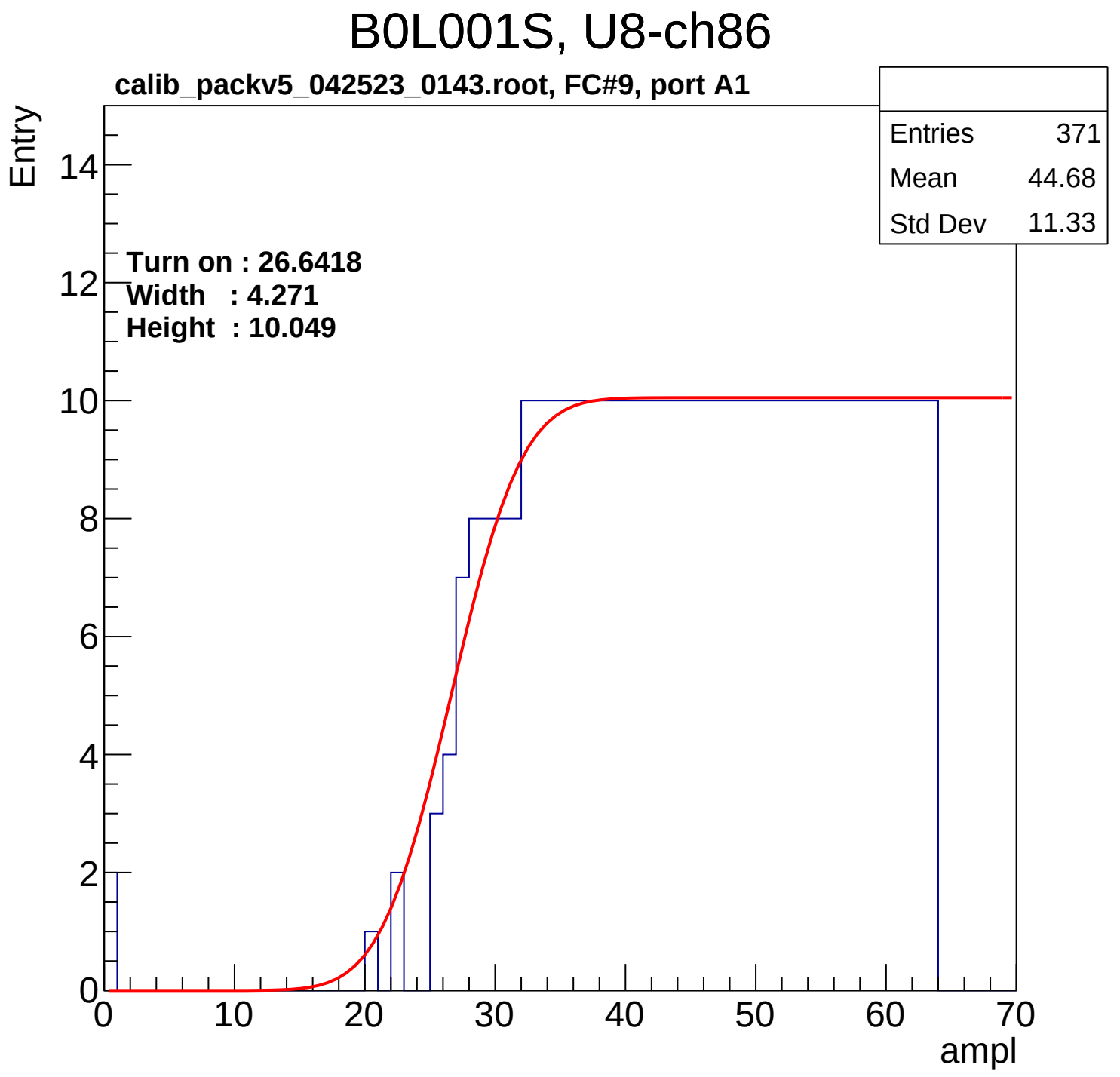
B0L001S, U8-ch86
calib_packv5_042523_0143.root, FC#9, port A1
Entries 371
Mean 44.68
Std Dev 11.33
Turn on : 26.6418
Width : 4.271
Height : 10.049
Entry
ampl
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6
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20
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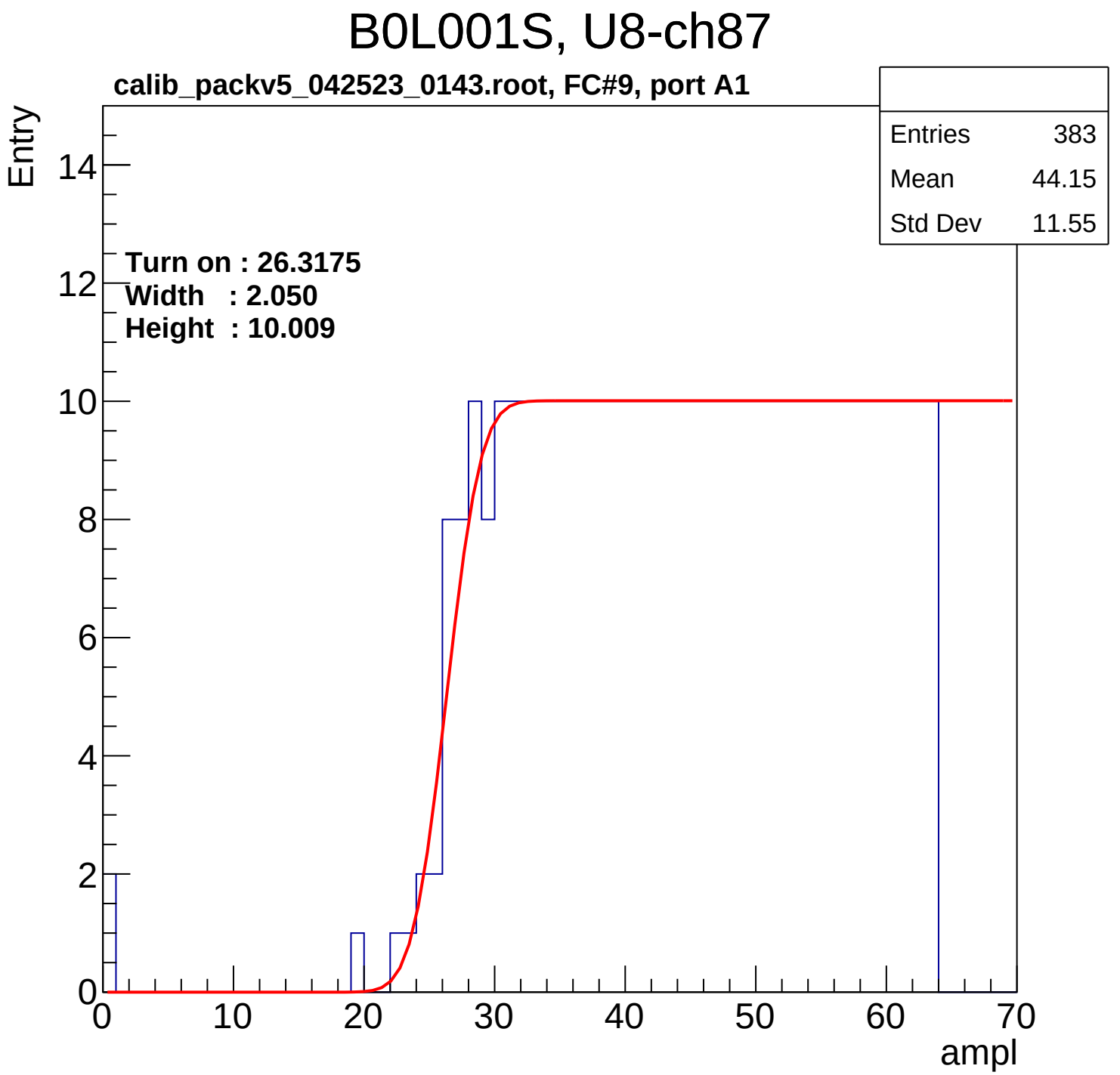
B0L001S, U8-ch87
calib_packv5_042523_0143.root, FC#9, port A1
Entries 383
Mean 44.15
Std Dev 11.55
Turn on : 26.3175
Width : 2.050
Height : 10.009
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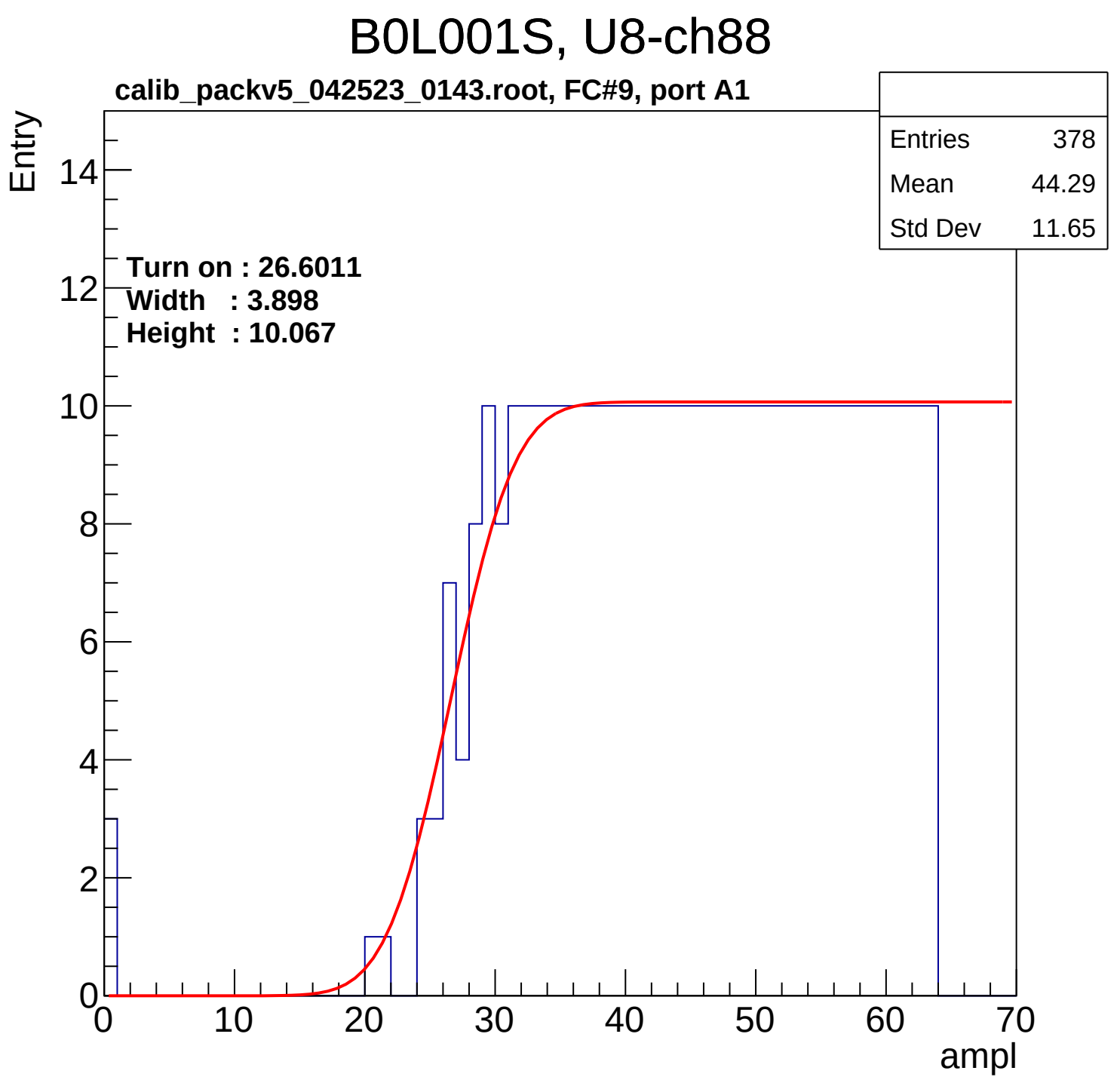
B0L001S, U8-ch88
calib_packv5_042523_0143.root, FC#9, port A1
Entries 378
Mean 44.29
Std Dev 11.65
Turn on : 26.6011
Width : 3.898
Height : 10.067
Entry
ampl
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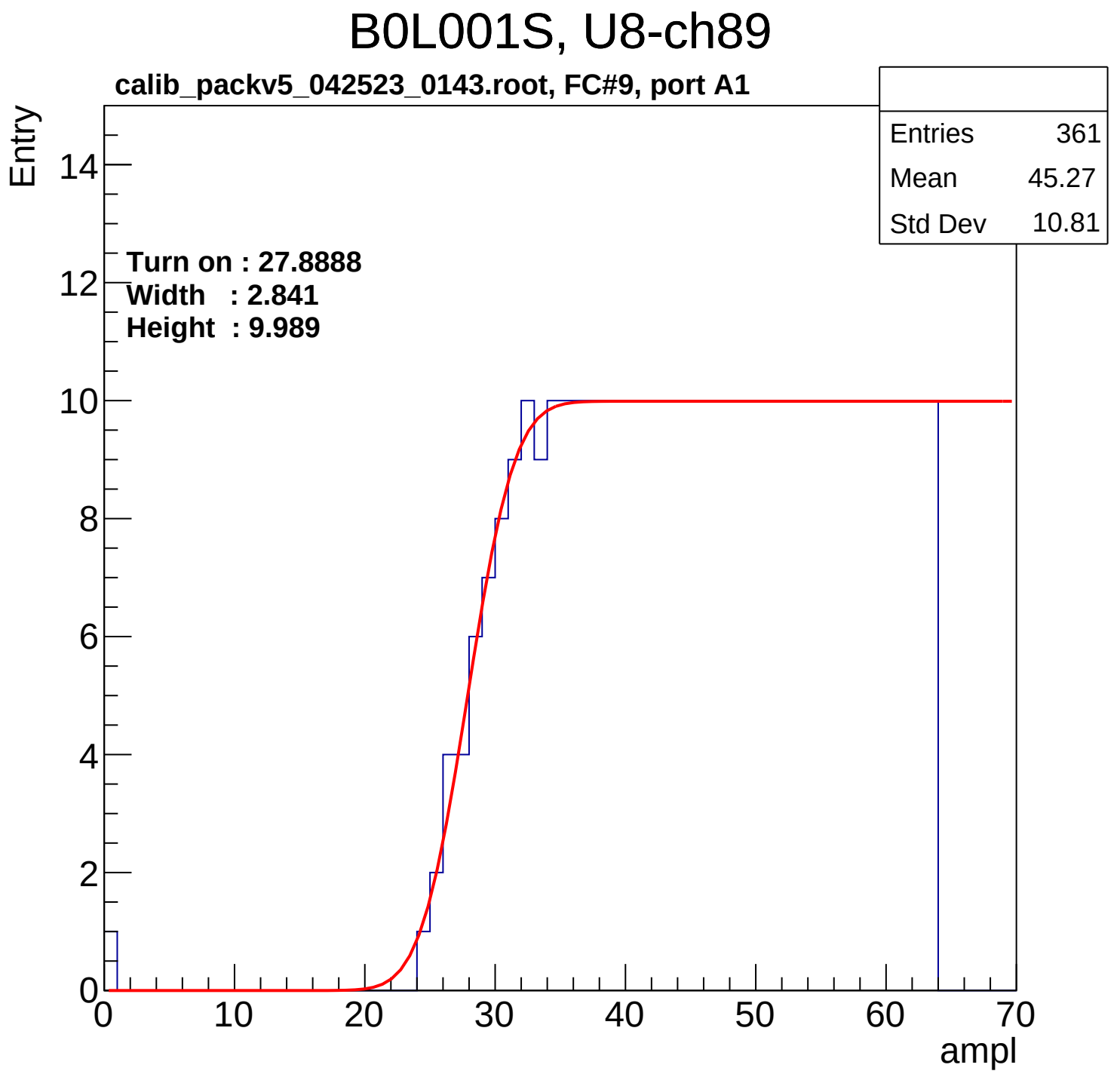
B0L001S, U8-ch89
calib_packv5_042523_0143.root, FC#9, port A1
Entries 361
Mean 45.27
Std Dev 10.81
Turn on : 27.8888
Width : 2.841
Height : 9.989
Entry
ampl
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4
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8
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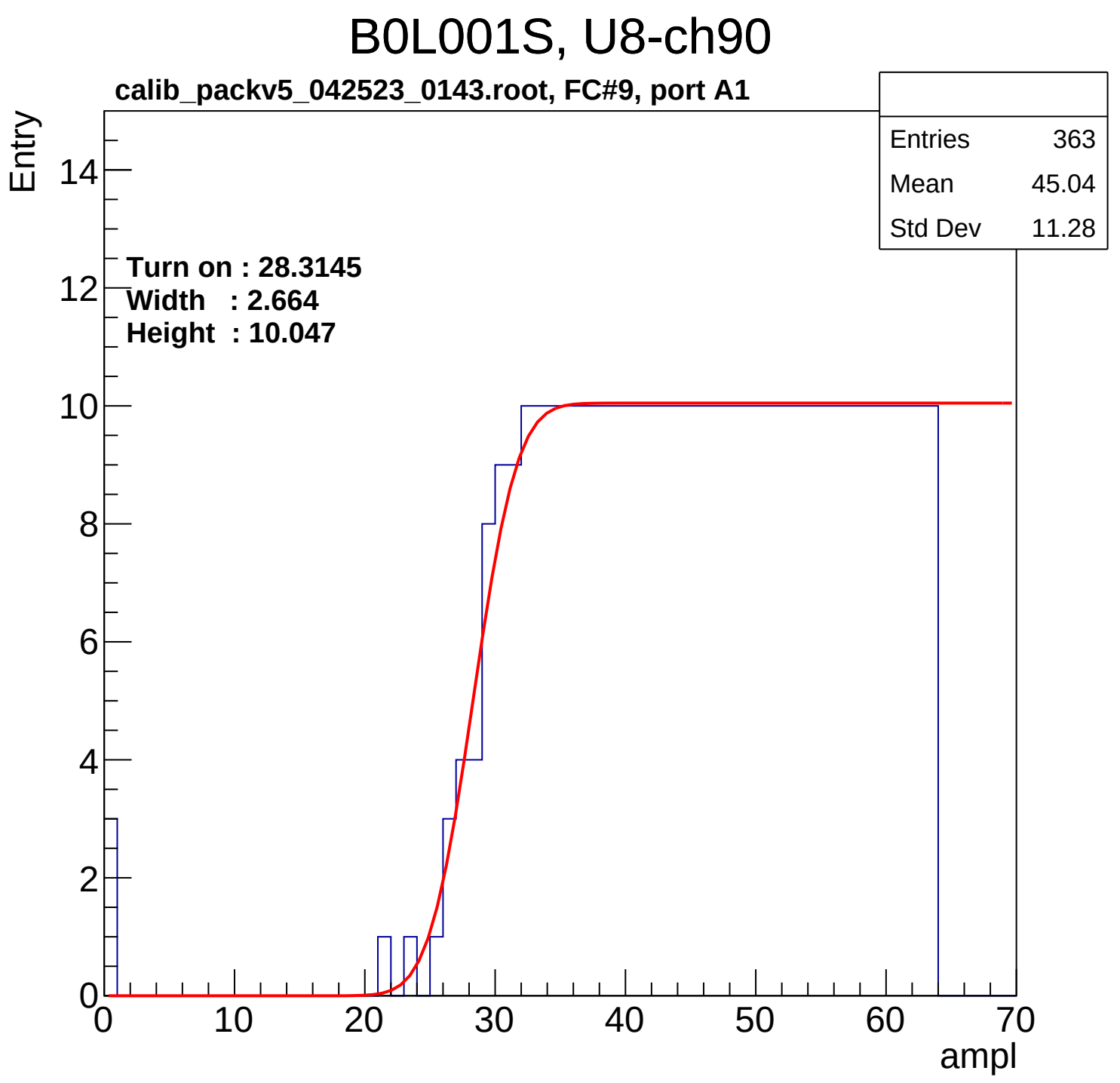
B0L001S, U8-ch90
calib_packv5_042523_0143.root, FC#9, port A1
Entries 363
Mean 45.04
Std Dev 11.28
Turn on : 28.3145
Width : 2.664
Height : 10.047
Entry
ampl
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2
4
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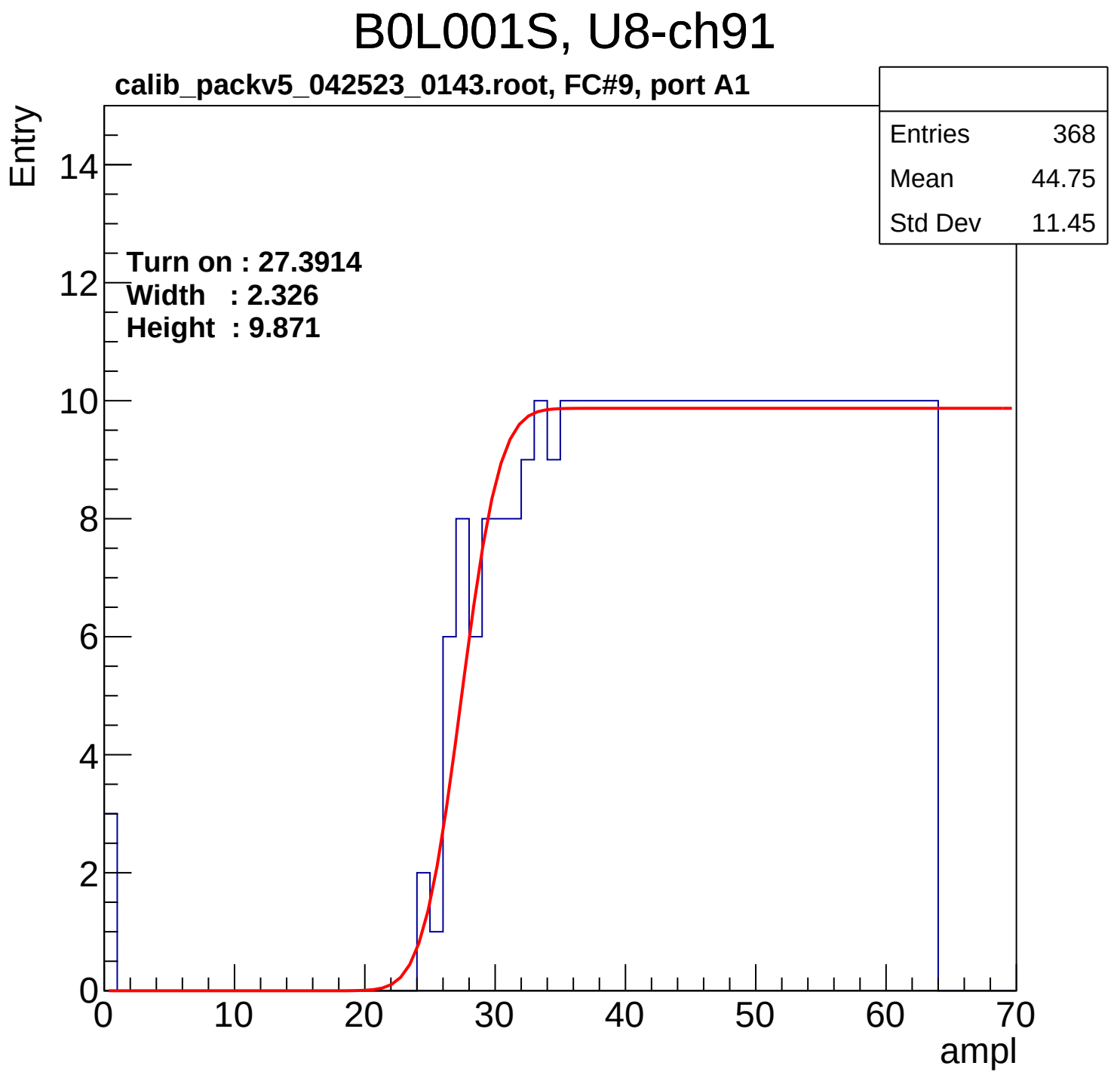
B0L001S, U8-ch91
calib_packv5_042523_0143.root, FC#9, port A1
Entries 368
Mean 44.75
Std Dev 11.45
Turn on : 27.3914
Width : 2.326
Height : 9.871
Entry
ampl
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2
4
6
8
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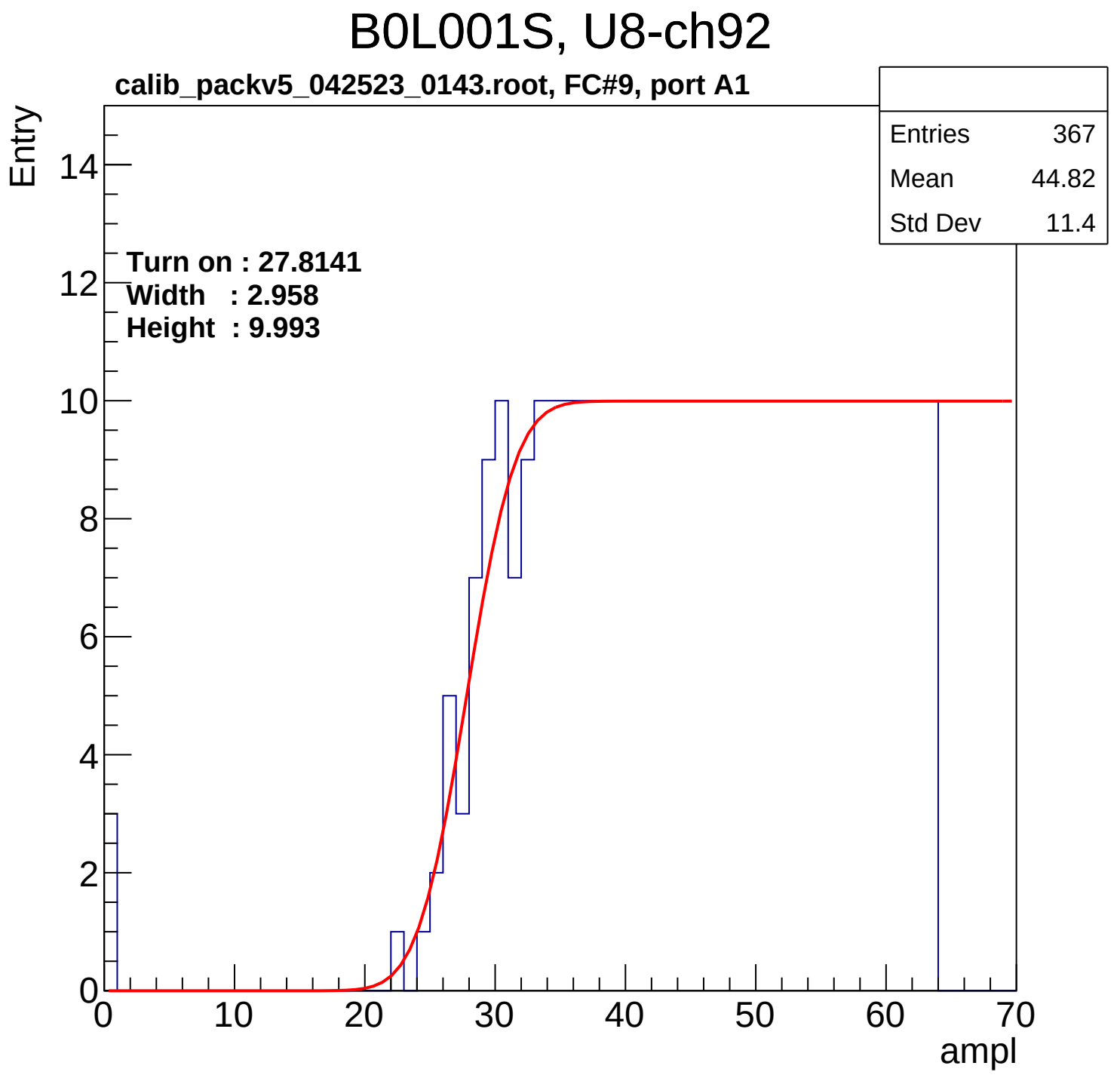
B0L001S, U8-ch92
calib_packv5_042523_0143.root, FC#9, port A1
Entries 367
Mean 44.82
Std Dev 11.4
Turn on : 27.8141
Width : 2.958
Height : 9.993
Entry
ampl
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2
4
6
8
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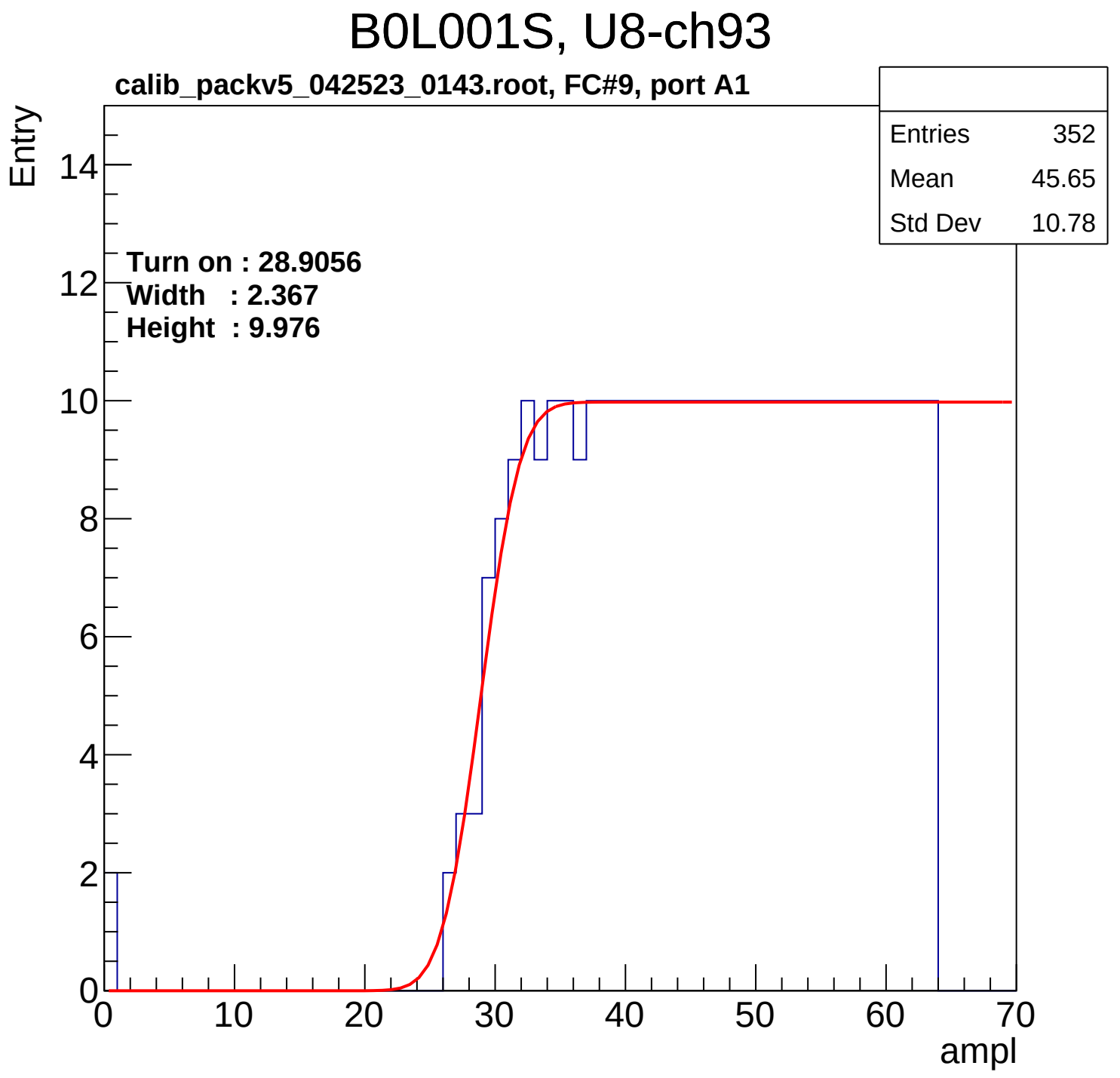
B0L001S, U8-ch93
calib_packv5_042523_0143.root, FC#9, port A1
Entries 352
Mean 45.65
Std Dev 10.78
Turn on : 28.9056
Width : 2.367
Height : 9.976
Entry
ampl
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2
4
6
8
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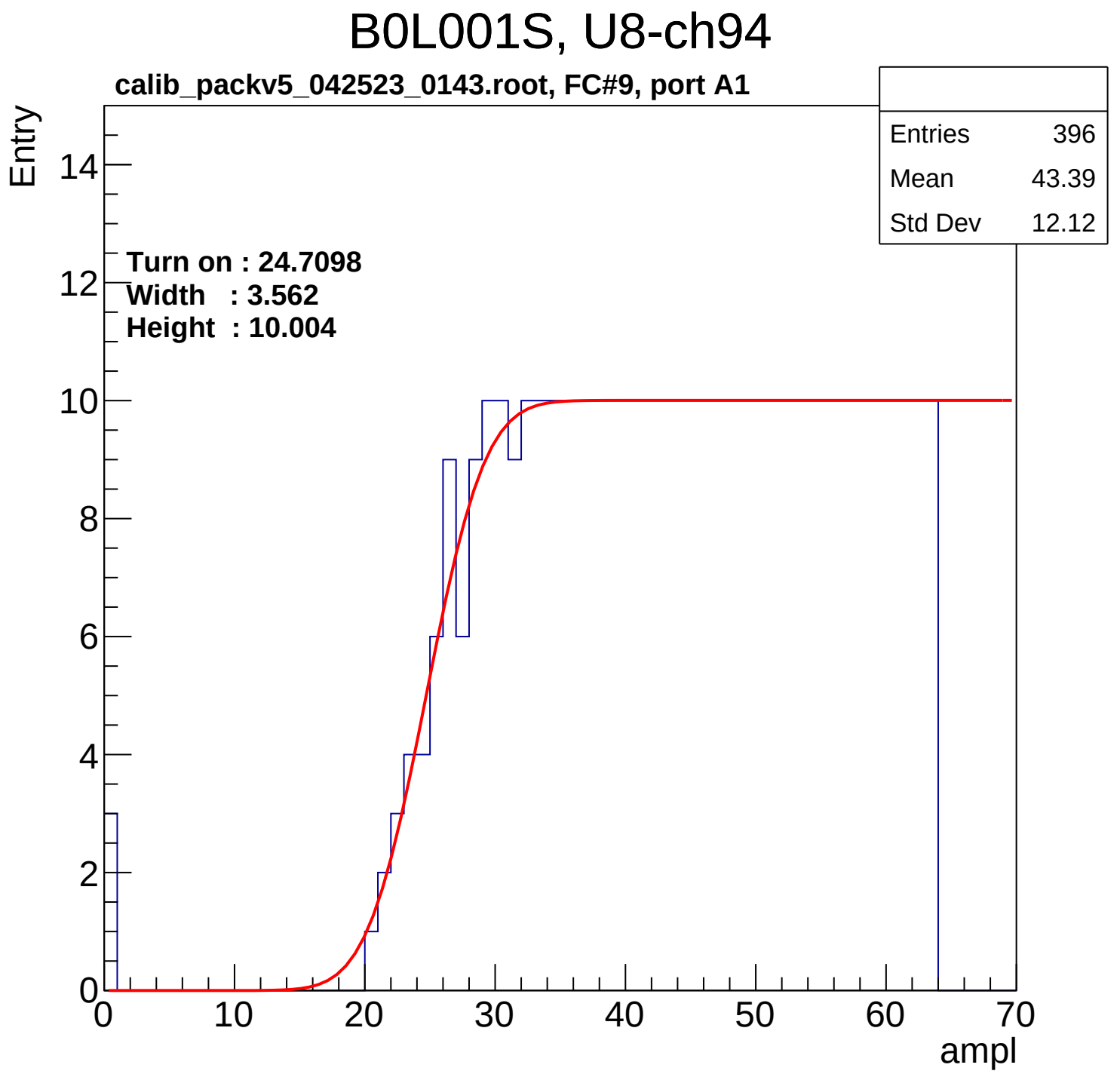
B0L001S, U8-ch94
calib_packv5_042523_0143.root, FC#9, port A1
Entries 396
Mean 43.39
Std Dev 12.12
Turn on : 24.7098
Width : 3.562
Height : 10.004
Entry
ampl
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2
4
6
8
10
12
14
0
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60
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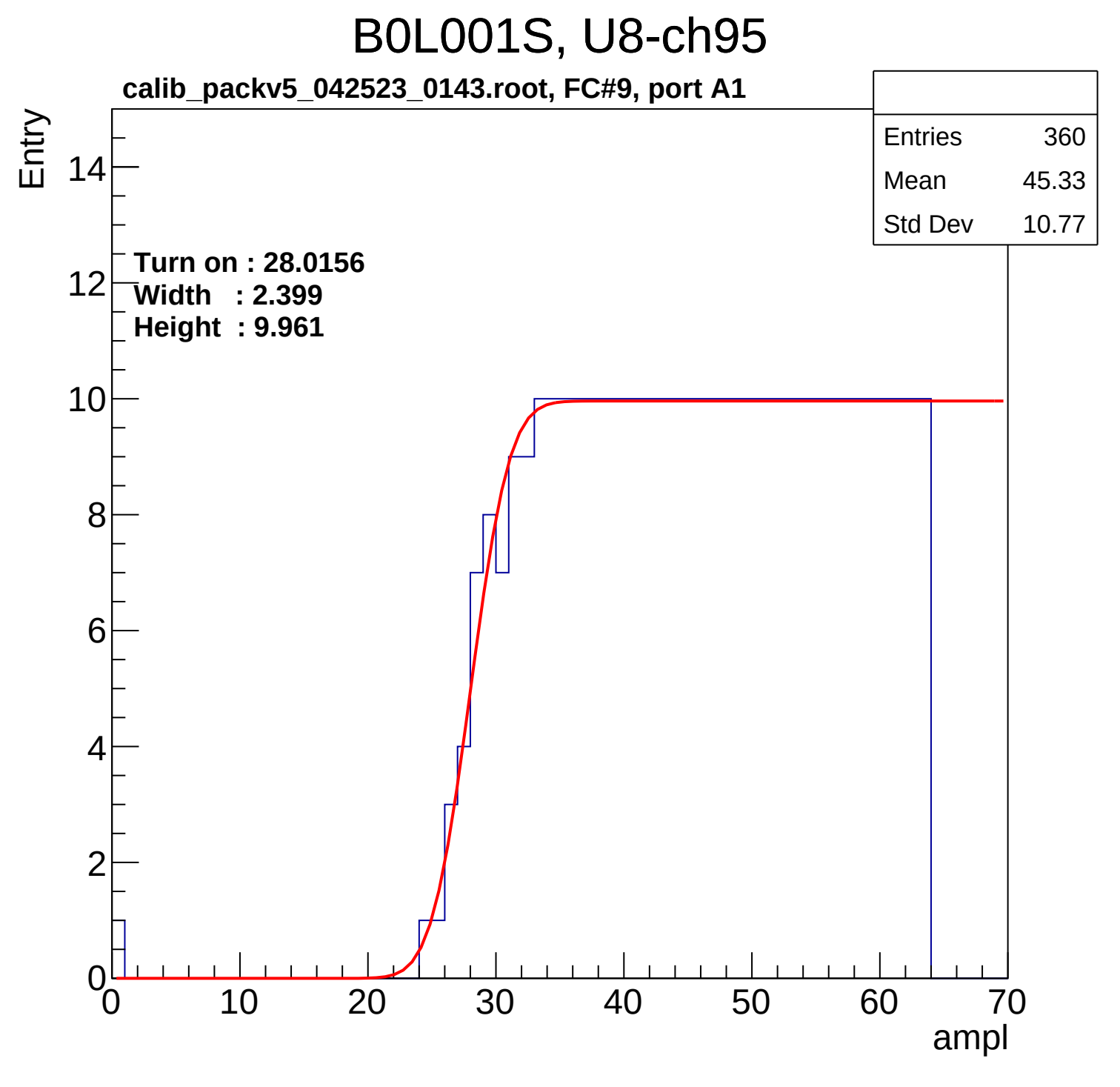
B0L001S, U8-ch95
calib_packv5_042523_0143.root, FC#9, port A1
Entries 360
Mean 45.33
Std Dev 10.77
Turn on : 28.0156
Width : 2.399
Height : 9.961
Entry
ampl
0
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6
8
10
12
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0
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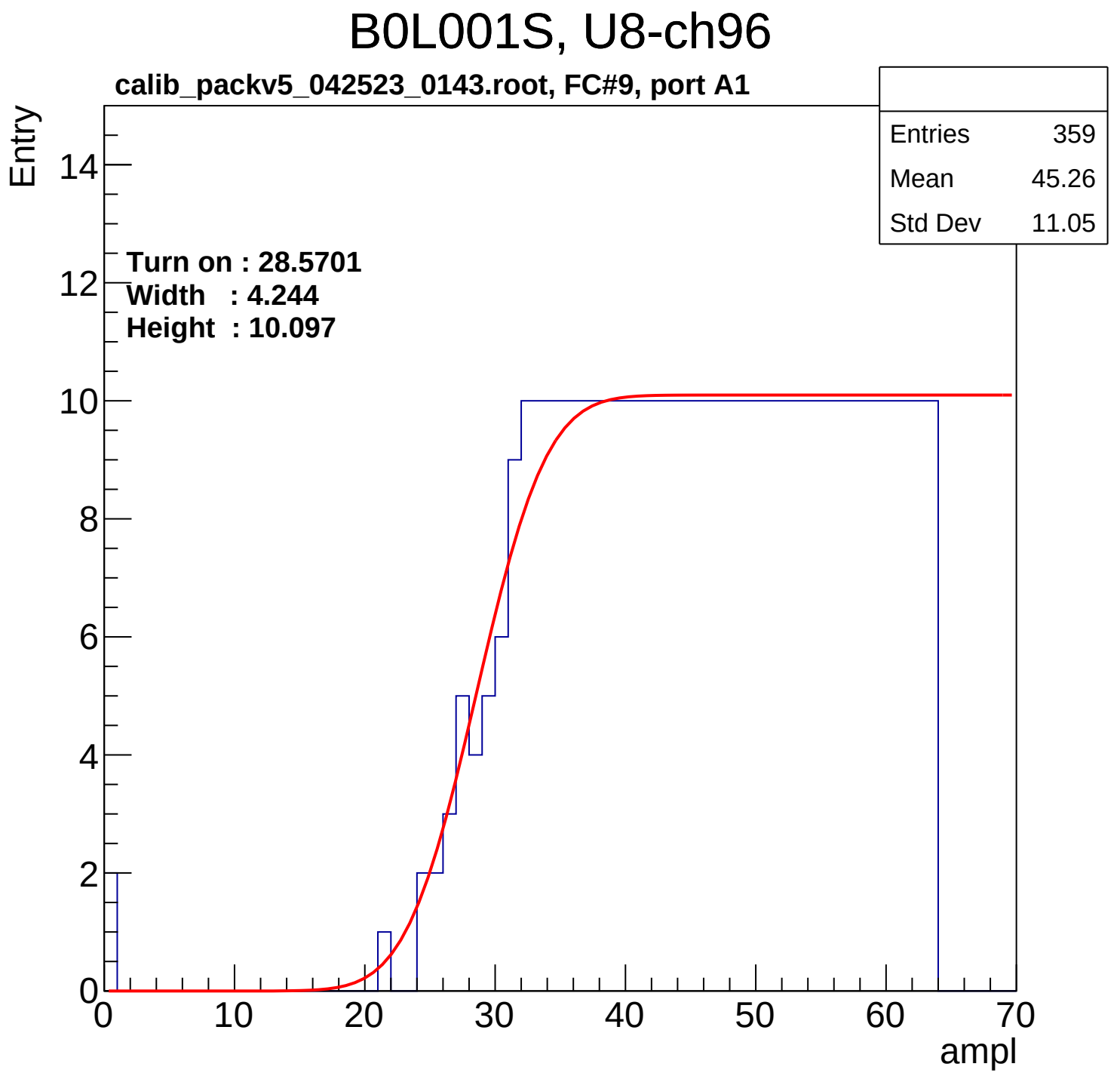
B0L001S, U8-ch96
calib_packv5_042523_0143.root, FC#9, port A1
Entries 359
Mean 45.26
Std Dev 11.05
Turn on : 28.5701
Width : 4.244
Height : 10.097
Entry
ampl
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6
8
10
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60
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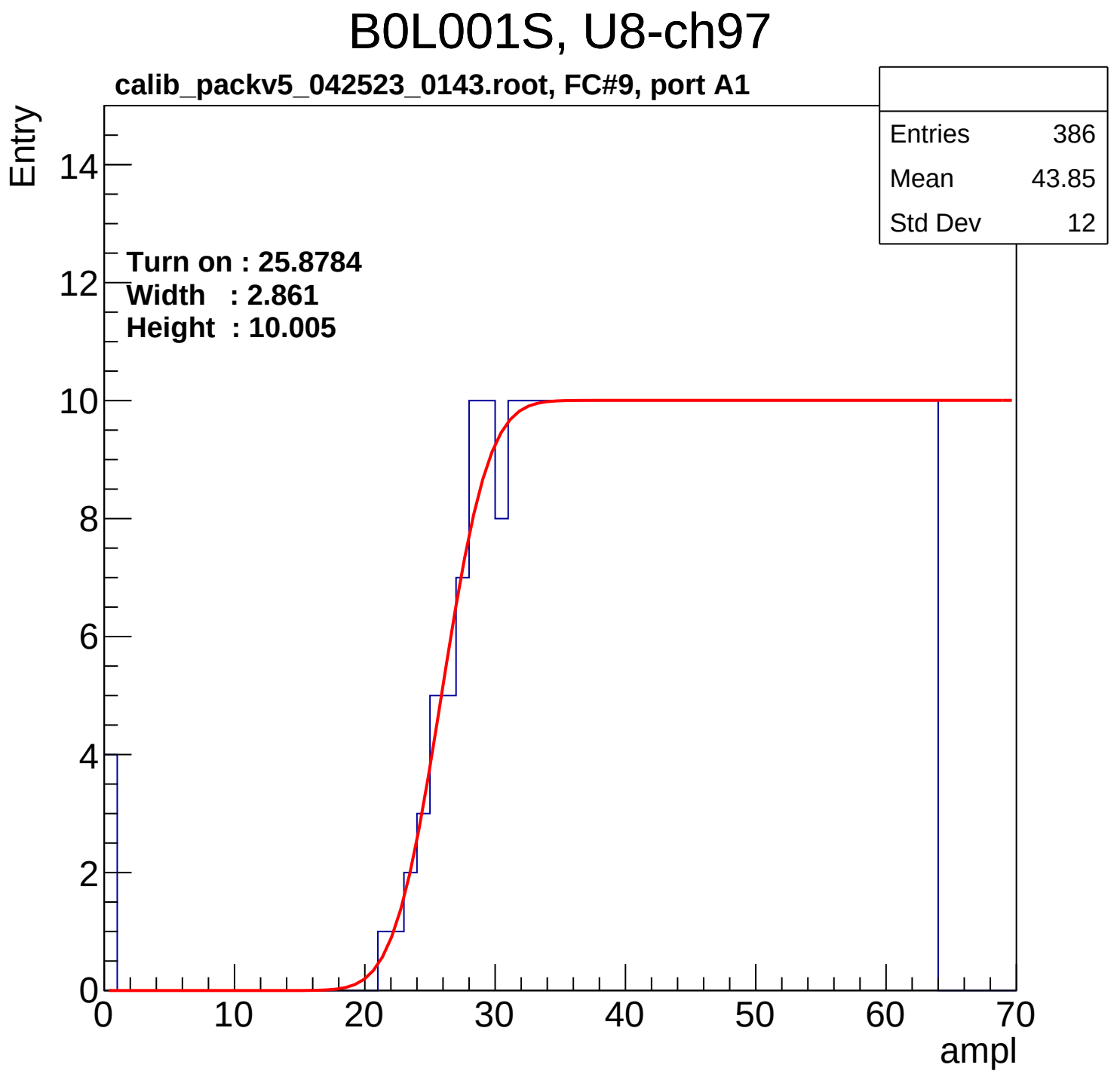
B0L001S, U8-ch97
calib_packv5_042523_0143.root, FC#9, port A1
Entries 386
Mean 43.85
Std Dev 12
Turn on : 25.8784
Width : 2.861
Height : 10.005
Entry
ampl
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6
8
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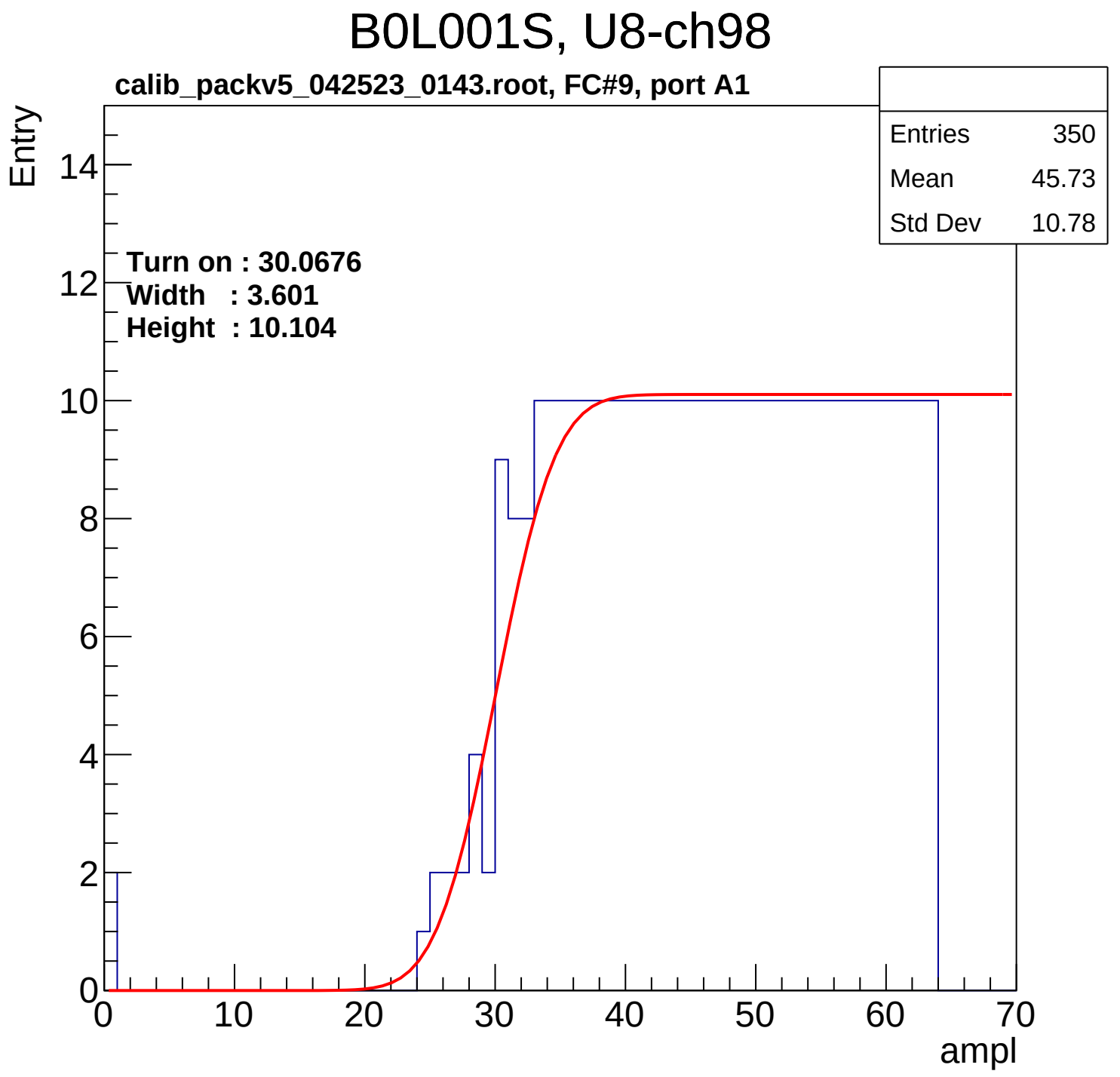
B0L001S, U8-ch98
calib_packv5_042523_0143.root, FC#9, port A1
Entries 350
Mean 45.73
Std Dev 10.78
Turn on : 30.0676
Width : 3.601
Height : 10.104
Entry
ampl
0
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6
8
10
12
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0
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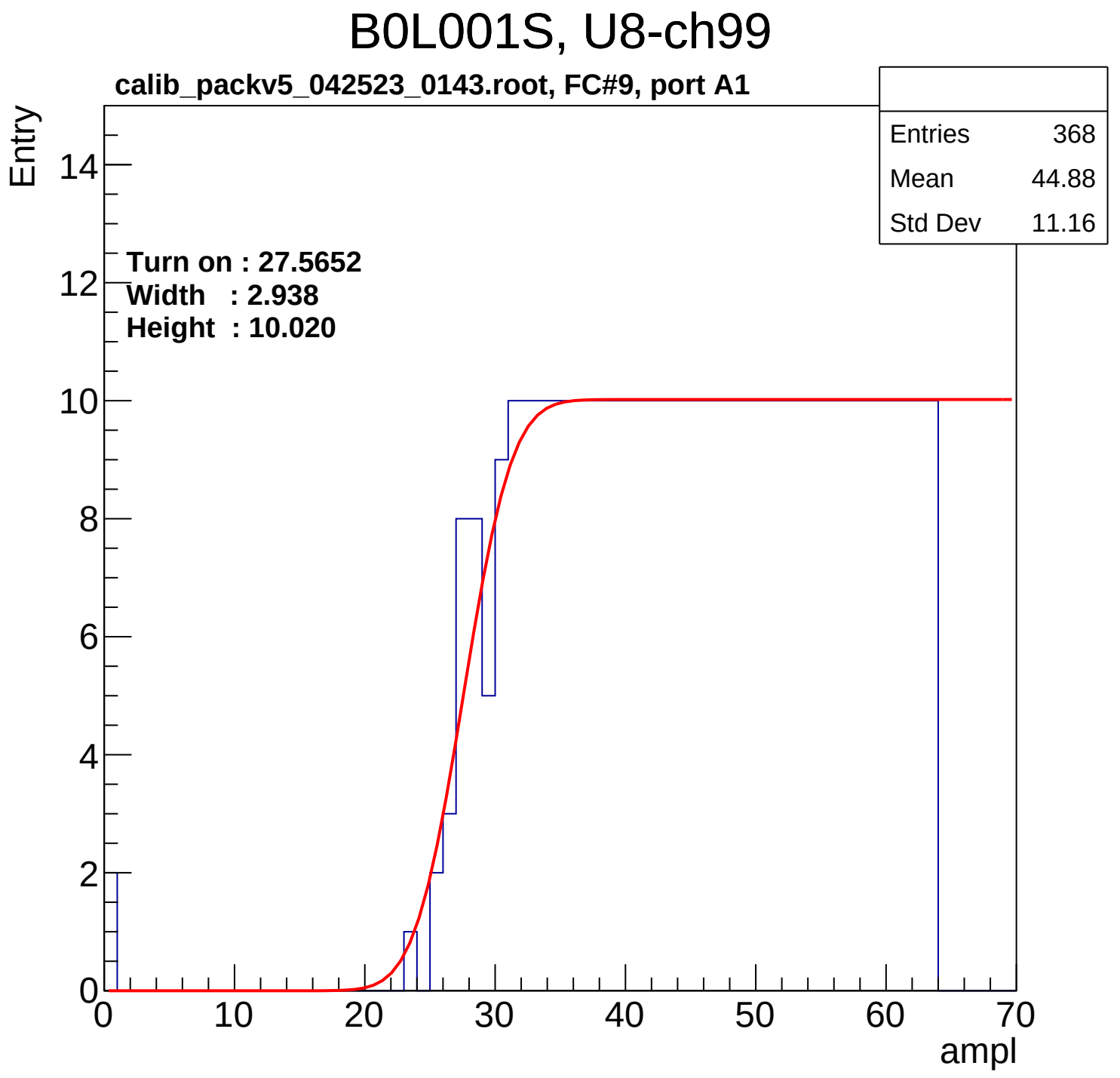
B0L001S, U8-ch99
calib_packv5_042523_0143.root, FC#9, port A1
Entries 368
Mean 44.88
Std Dev 11.16
Turn on : 27.5652
Width : 2.938
Height : 10.020
Entry
ampl
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6
8
10
12
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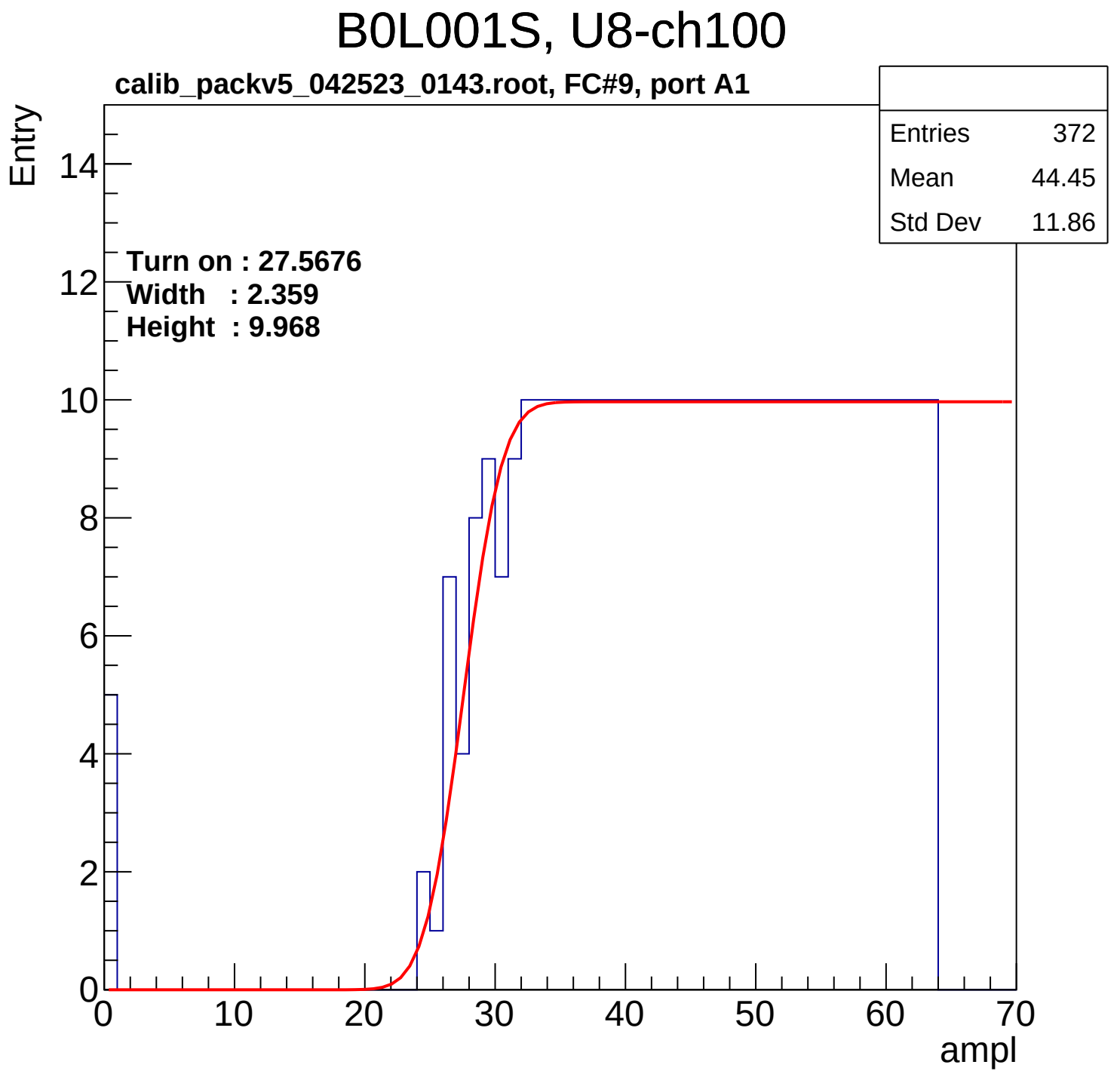
B0L001S, U8-ch100
calib_packv5_042523_0143.root, FC#9, port A1
Entries 372
Mean 44.45
Std Dev 11.86
Turn on : 27.5676
Width : 2.359
Height : 9.968
Entry
ampl
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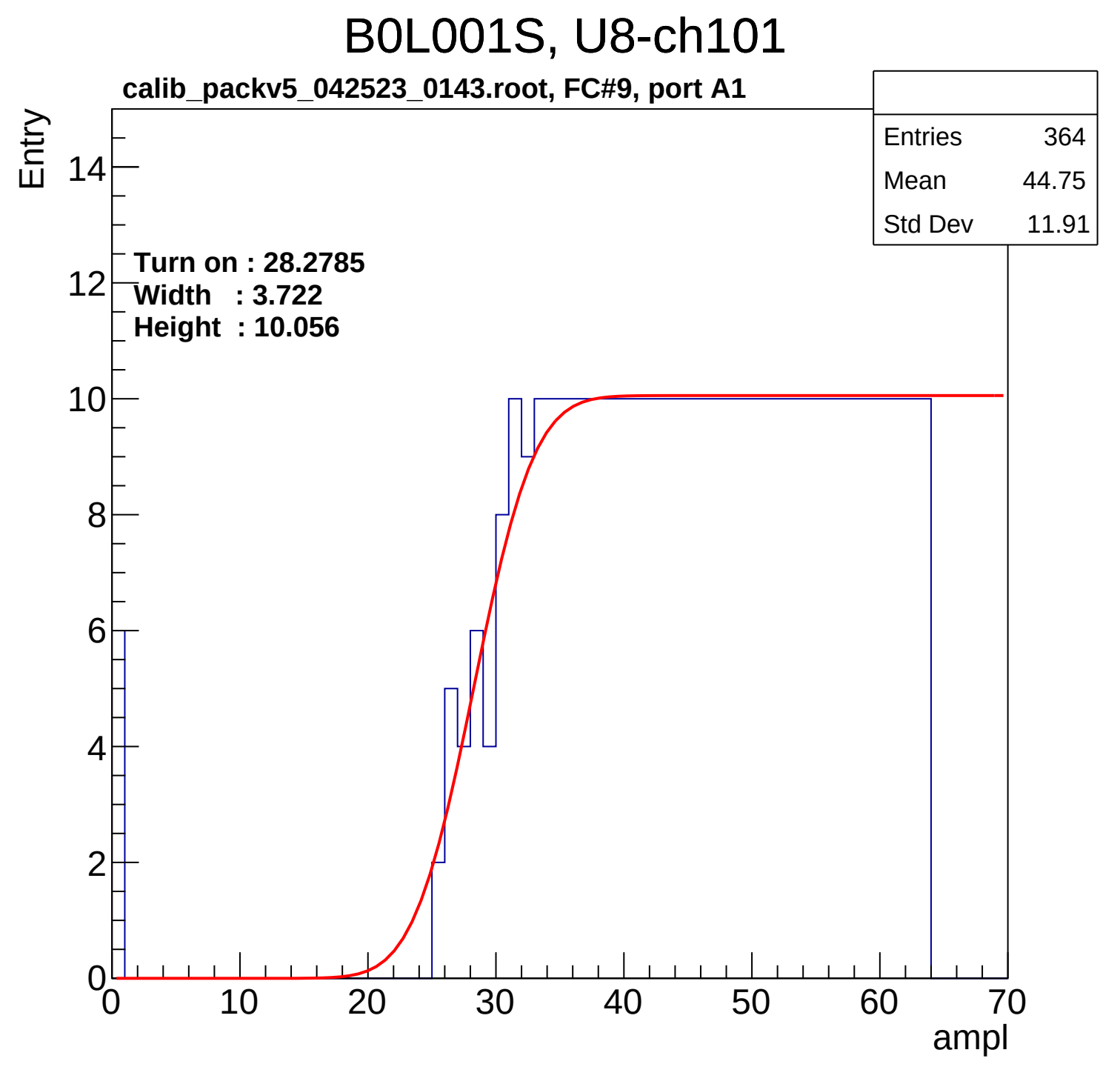
B0L001S, U8-ch101
calib_packv5_042523_0143.root, FC#9, port A1
Entries 364
Mean 44.75
Std Dev 11.91
Turn on : 28.2785
Width : 3.722
Height : 10.056
Entry
ampl
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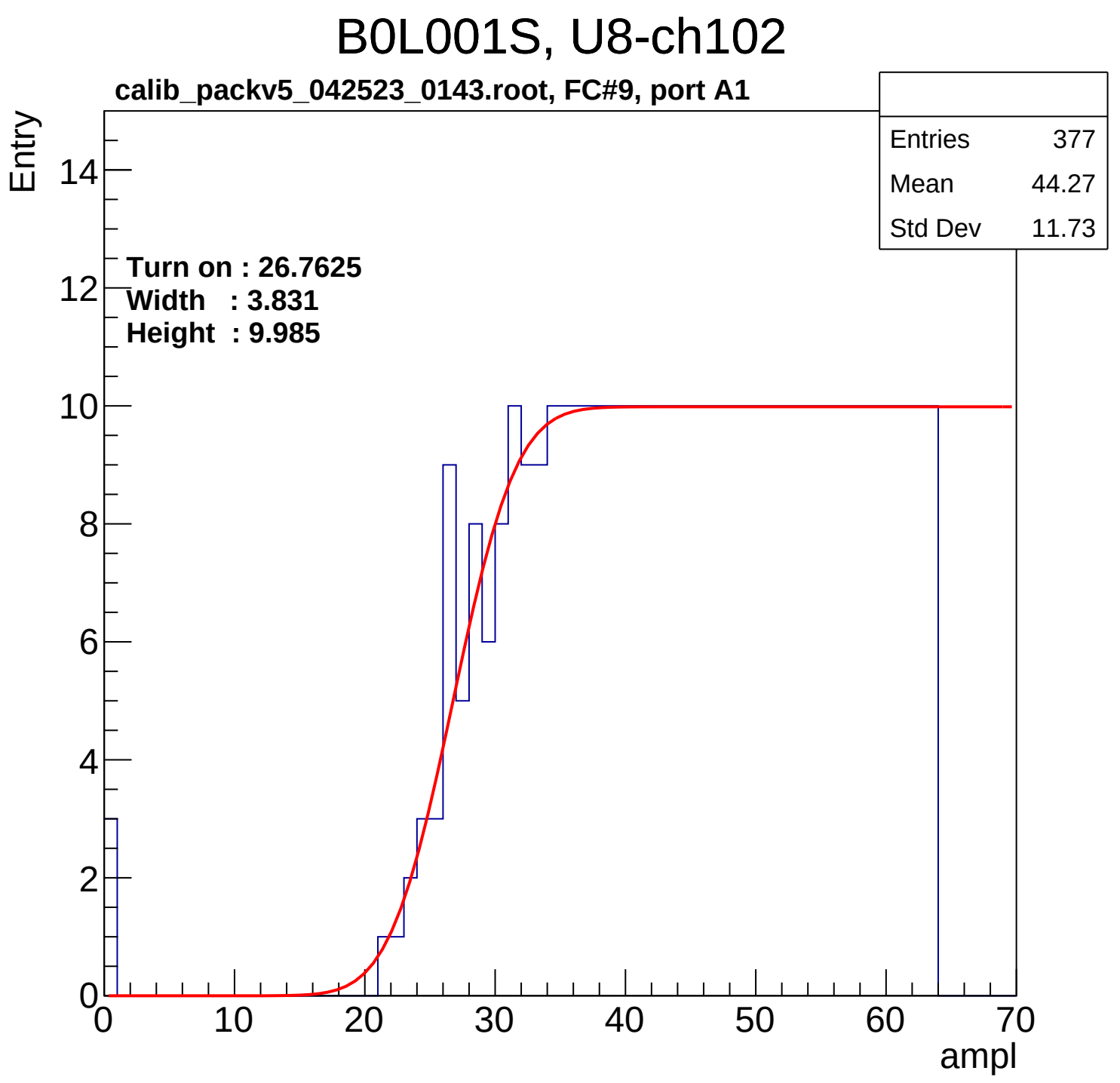
B0L001S, U8-ch102
calib_packv5_042523_0143.root, FC#9, port A1
Entries 377
Mean 44.27
Std Dev 11.73
Turn on : 26.7625
Width : 3.831
Height : 9.985
Entry
ampl
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8
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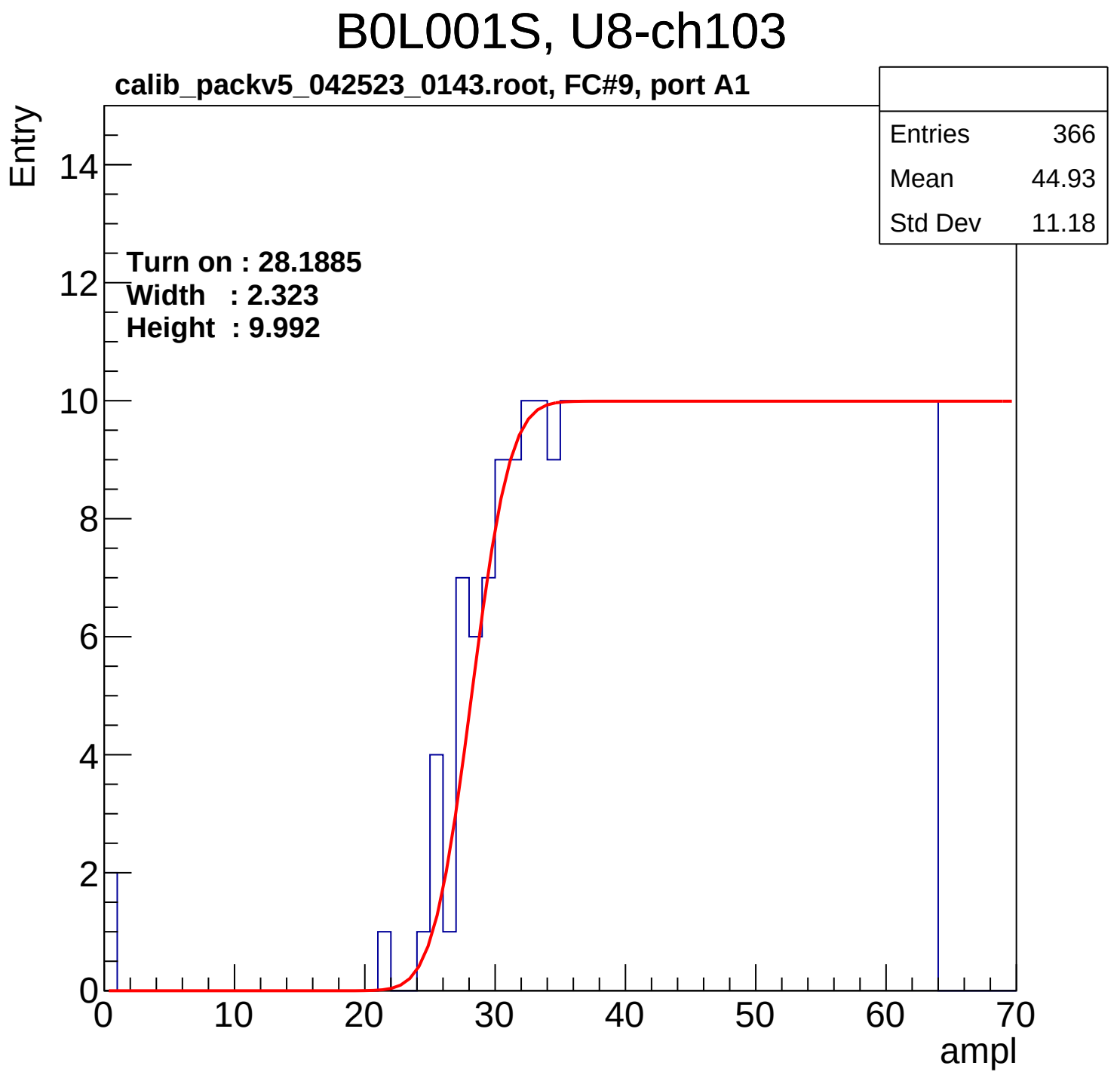
B0L001S, U8-ch103
calib_packv5_042523_0143.root, FC#9, port A1
Entries 366
Mean 44.93
Std Dev 11.18
Turn on : 28.1885
Width : 2.323
Height : 9.992
Entry
ampl
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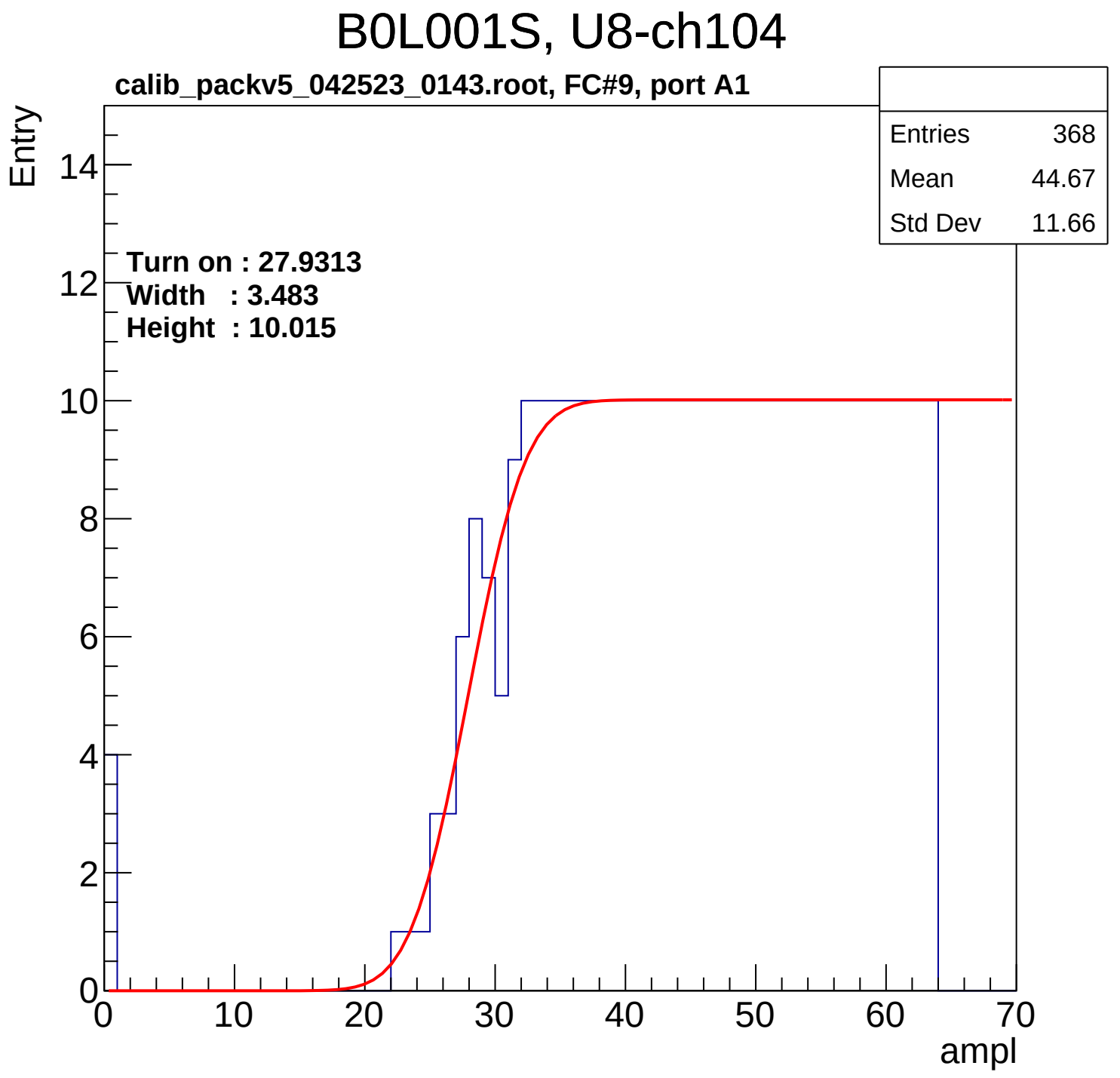
B0L001S, U8-ch104
calib_packv5_042523_0143.root, FC#9, port A1
Entries 368
Mean 44.67
Std Dev 11.66
Turn on : 27.9313
Width : 3.483
Height : 10.015
Entry
ampl
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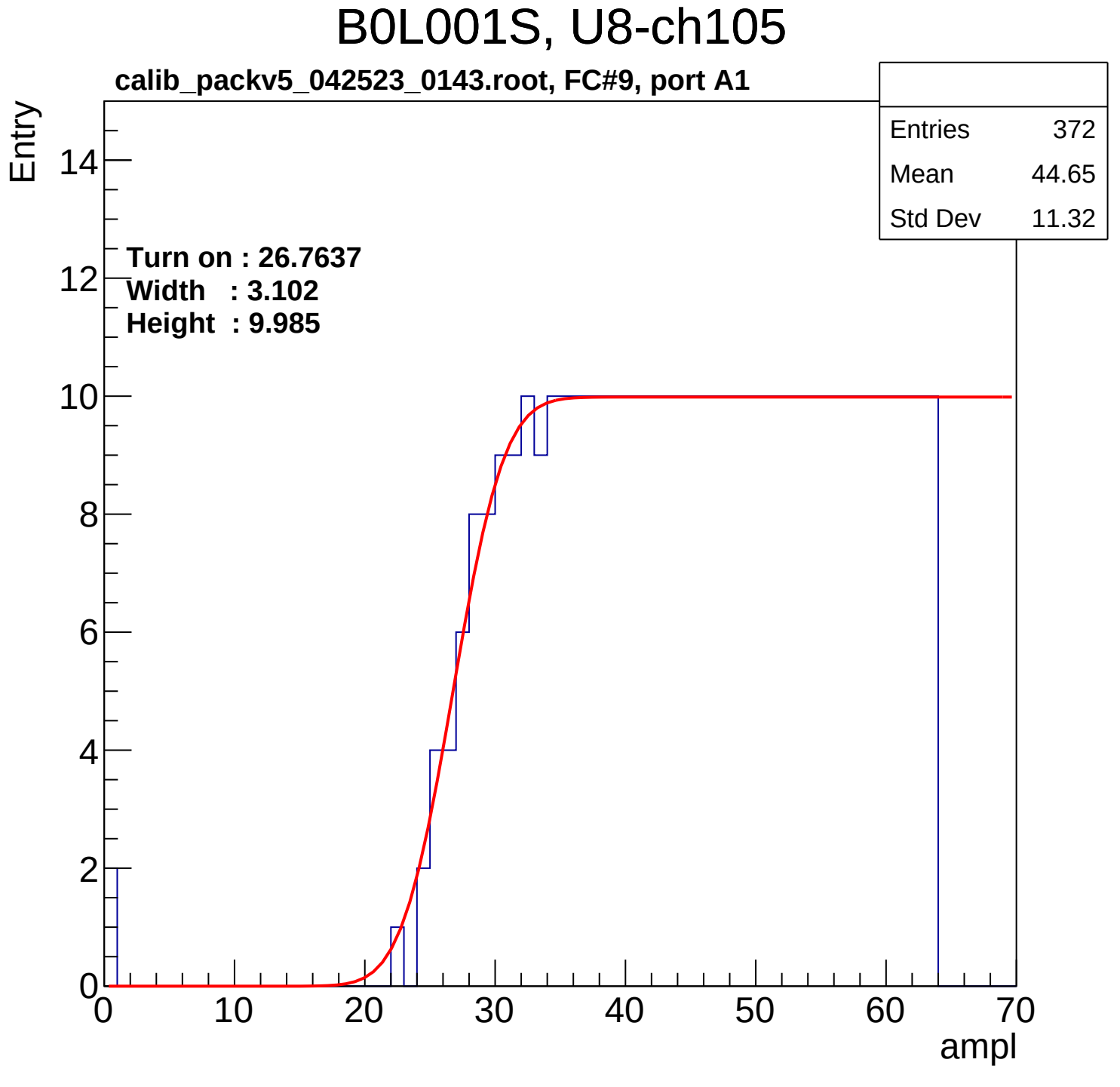
B0L001S, U8-ch105
calib_packv5_042523_0143.root, FC#9, port A1
Entries 372
Mean 44.65
Std Dev 11.32
Turn on : 26.7637
Width : 3.102
Height : 9.985
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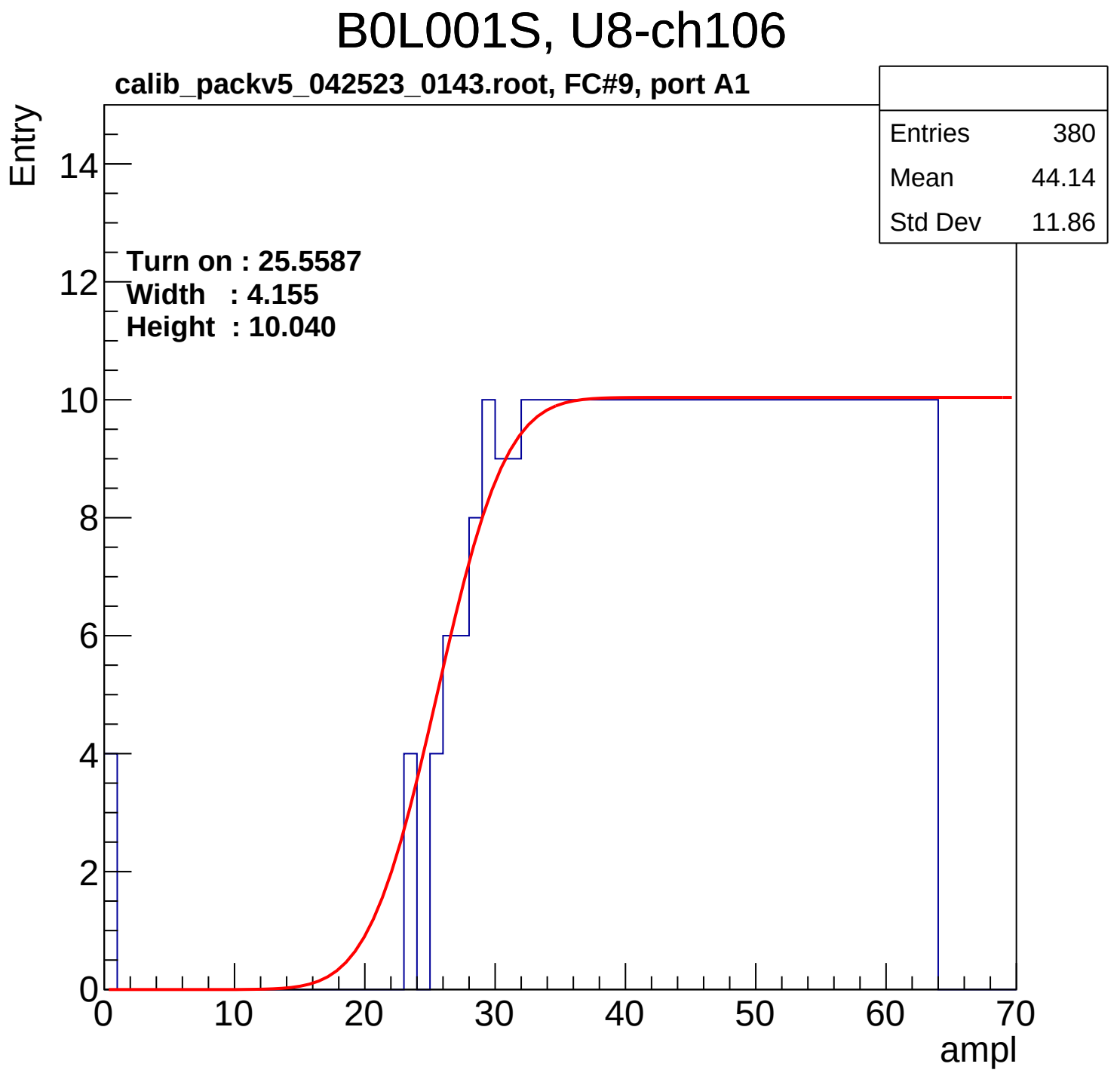
B0L001S, U8-ch106
calib_packv5_042523_0143.root, FC#9, port A1
Entries 380
Mean 44.14
Std Dev 11.86
Turn on : 25.5587
Width : 4.155
Height : 10.040
Entry
ampl
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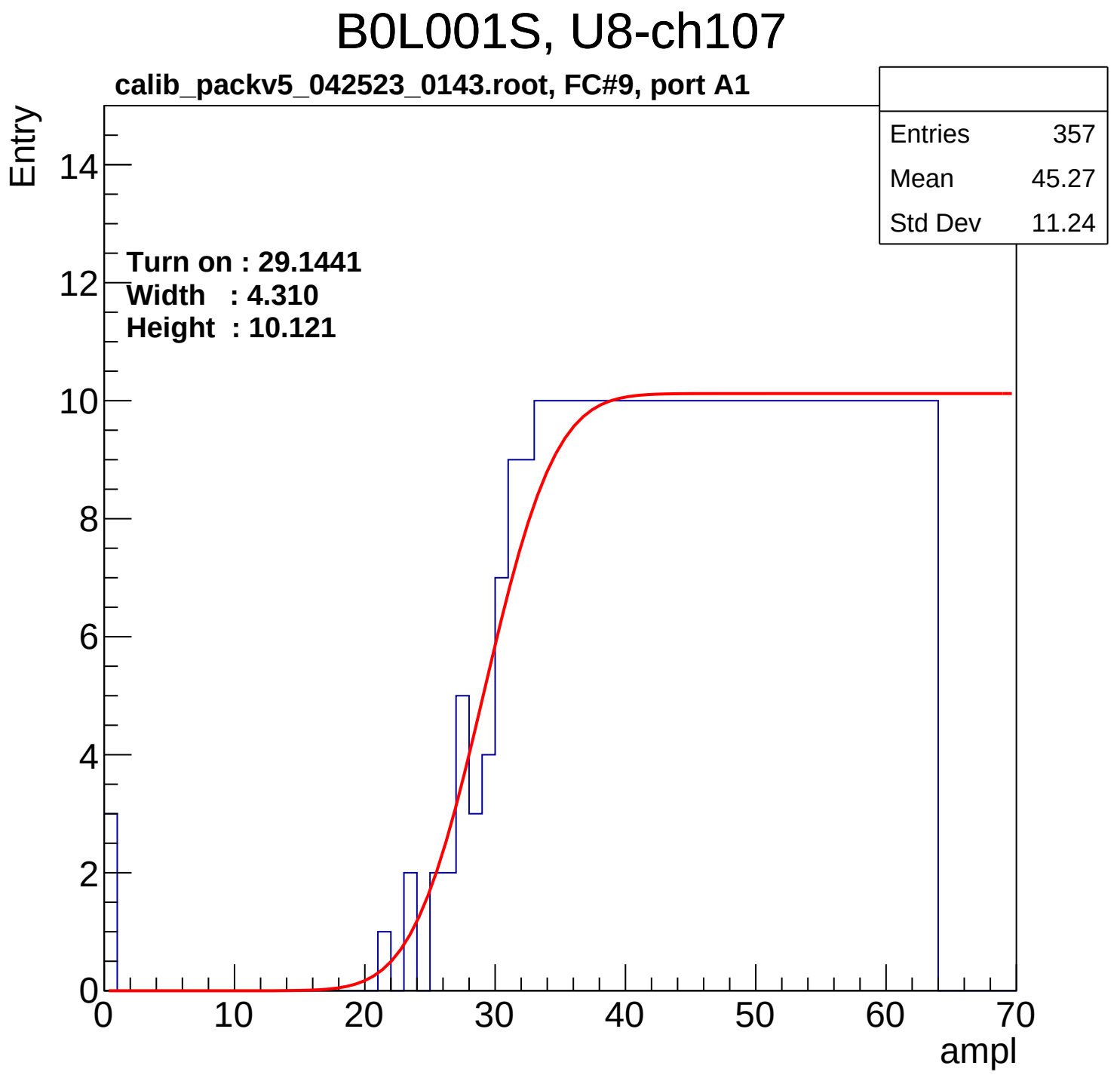
B0L001S, U8-ch107
calib_packv5_042523_0143.root, FC#9, port A1
Entries 357
Mean 45.27
Std Dev 11.24
Turn on : 29.1441
Width : 4.310
Height : 10.121
Entry
ampl
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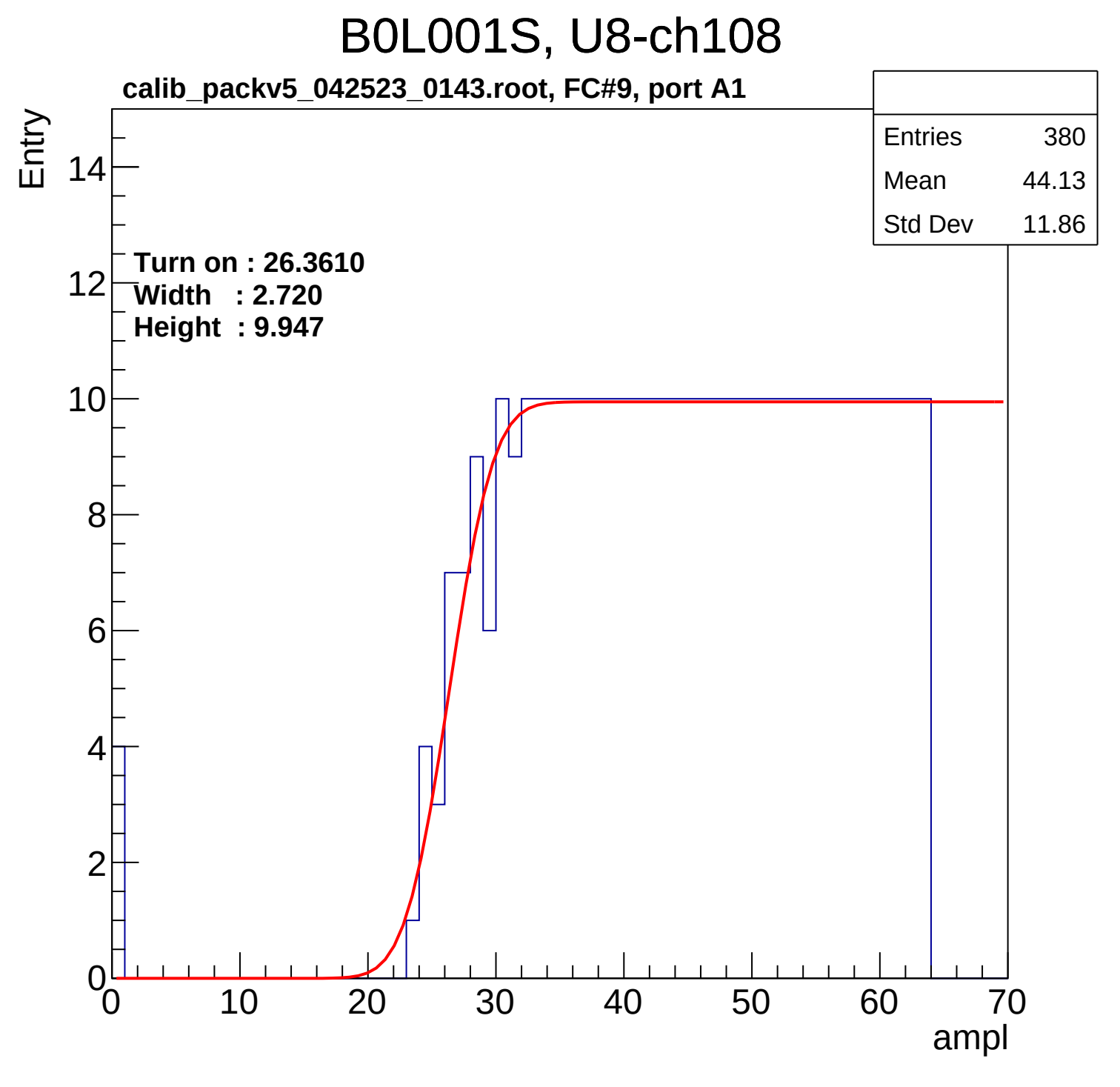
B0L001S, U8-ch108
calib_packv5_042523_0143.root, FC#9, port A1
Entries 380
Mean 44.13
Std Dev 11.86
Turn on : 26.3610
Width : 2.720
Height : 9.947
Entry
ampl
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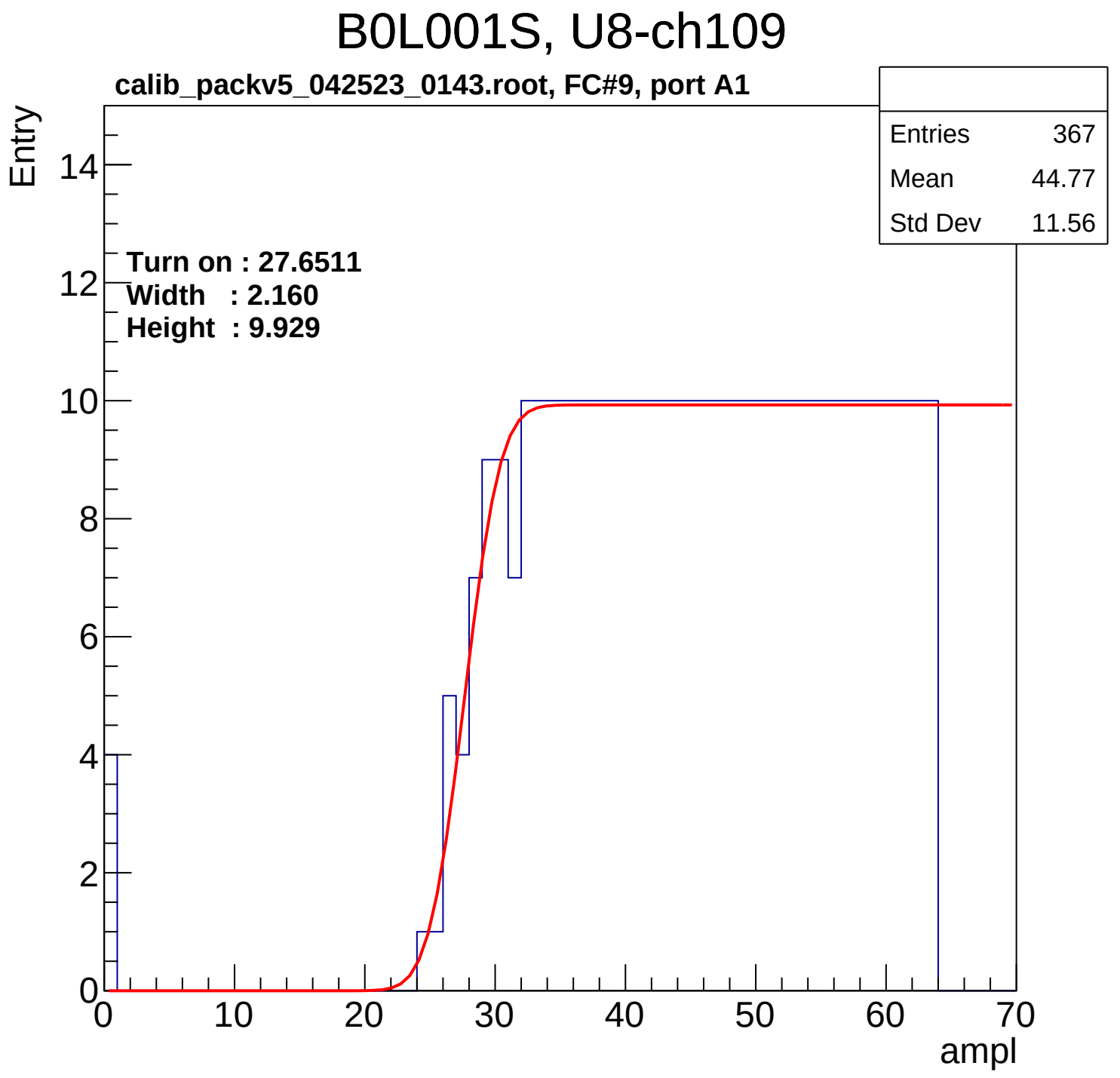
B0L001S, U8-ch109
calib_packv5_042523_0143.root, FC#9, port A1
Entries 367
Mean 44.77
Std Dev 11.56
Turn on : 27.6511
Width : 2.160
Height : 9.929
Entry
ampl
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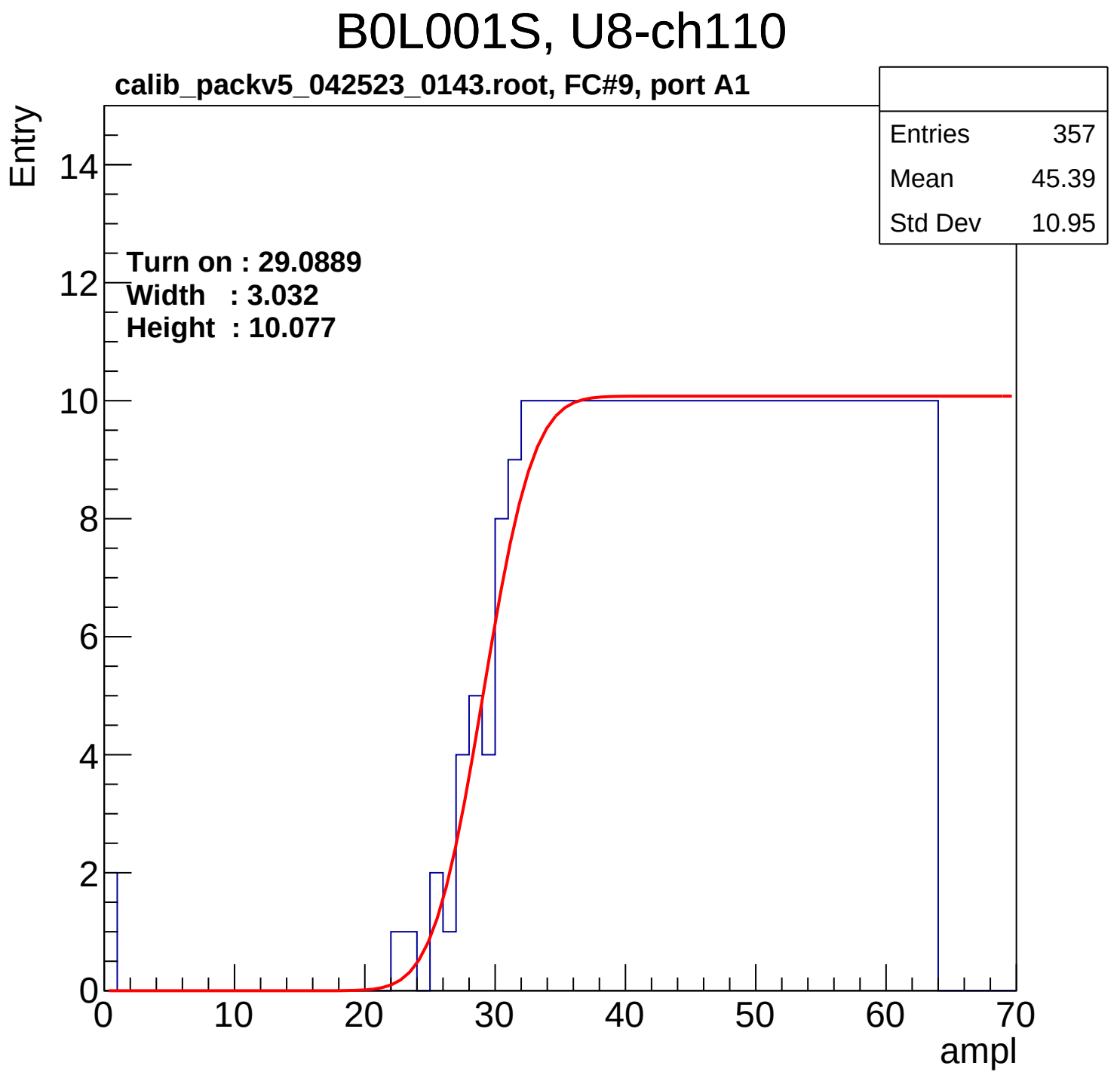
B0L001S, U8-ch110
calib_packv5_042523_0143.root, FC#9, port A1
Entries 357
Mean 45.39
Std Dev 10.95
Turn on : 29.0889
Width : 3.032
Height : 10.077
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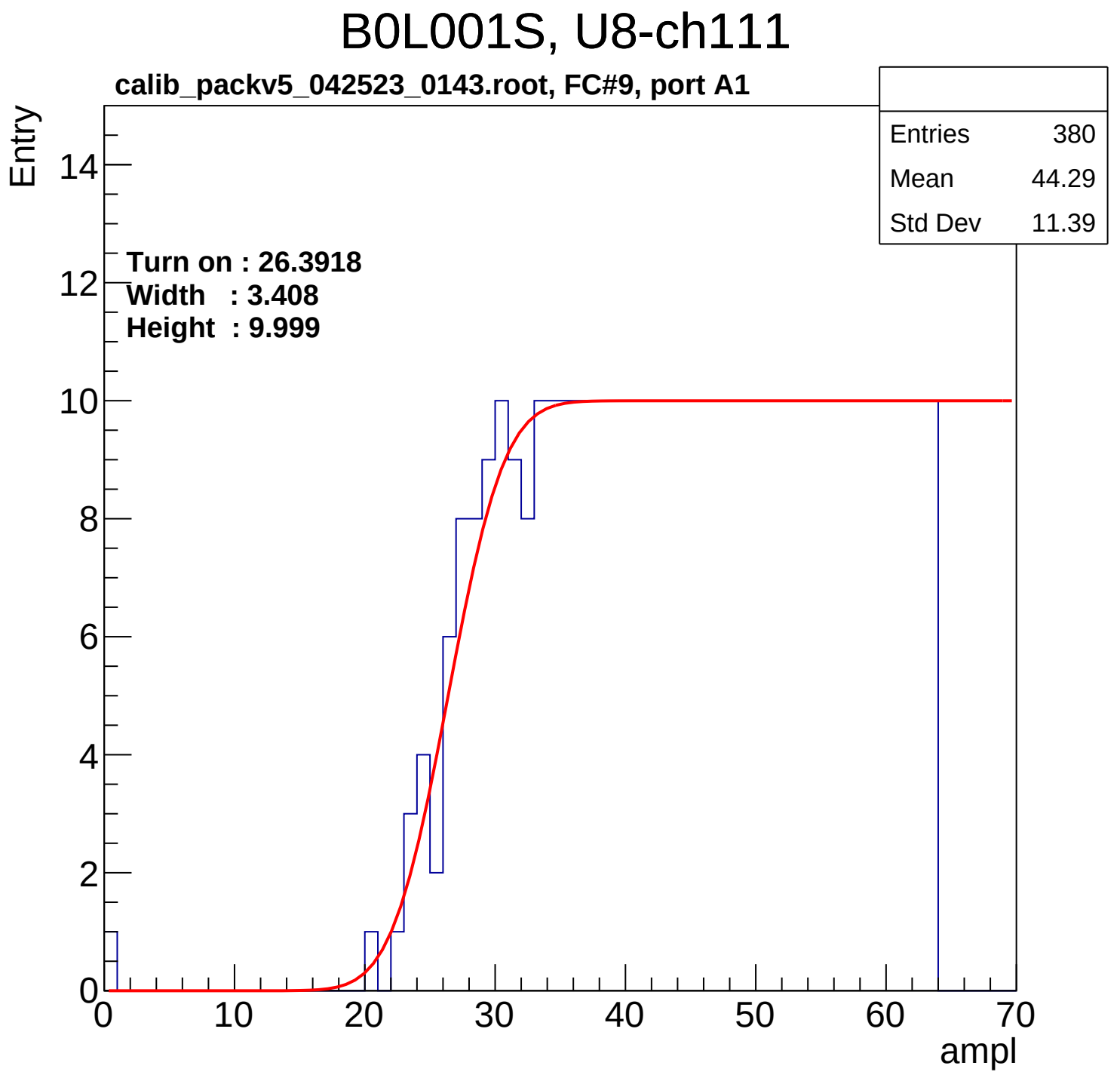
B0L001S, U8-ch111
calib_packv5_042523_0143.root, FC#9, port A1
Entries 380
Mean 44.29
Std Dev 11.39
Turn on : 26.3918
Width : 3.408
Height : 9.999
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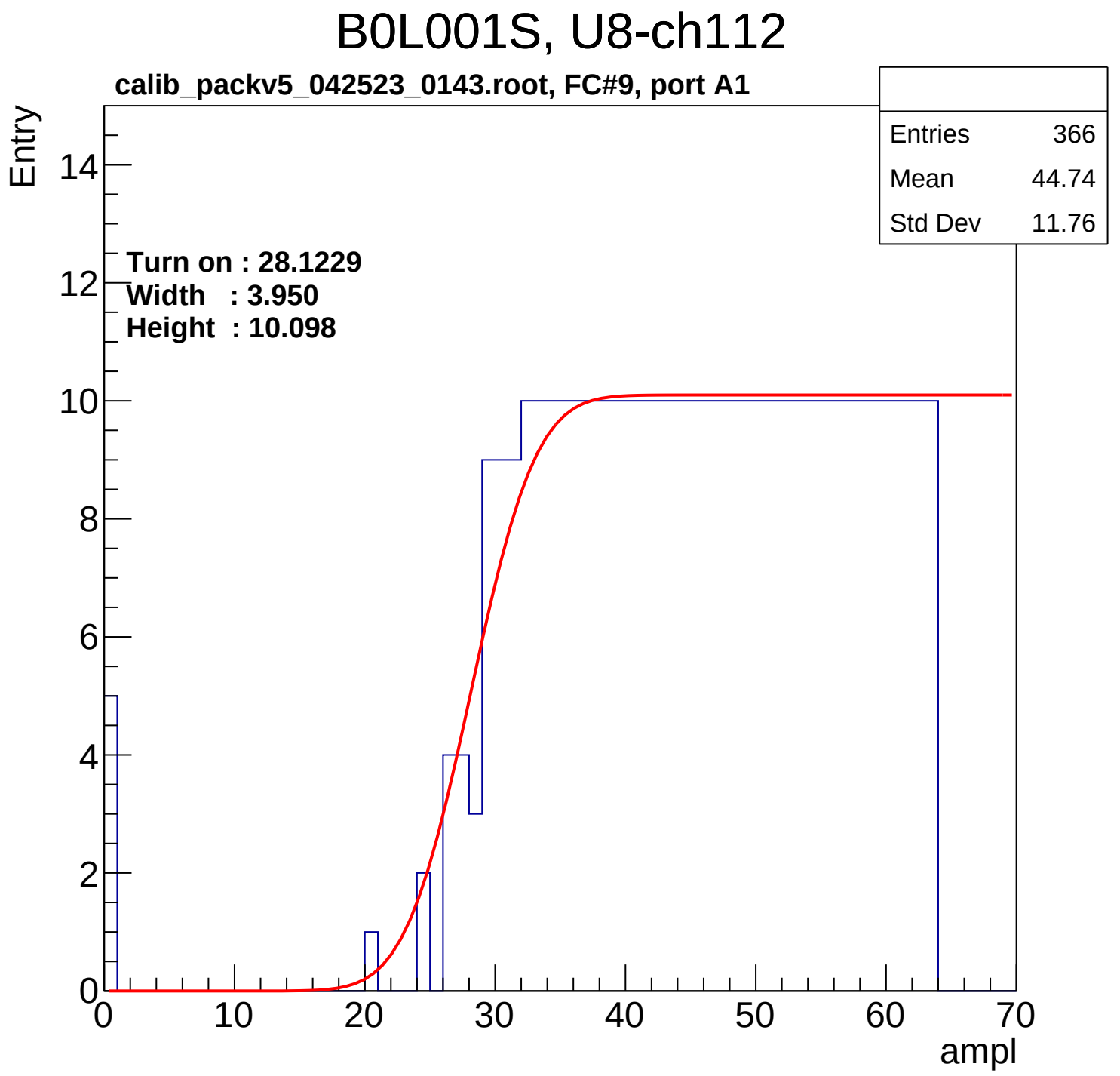
B0L001S, U8-ch112
calib_packv5_042523_0143.root, FC#9, port A1
Entries 366
Mean 44.74
Std Dev 11.76
Turn on : 28.1229
Width : 3.950
Height : 10.098
Entry
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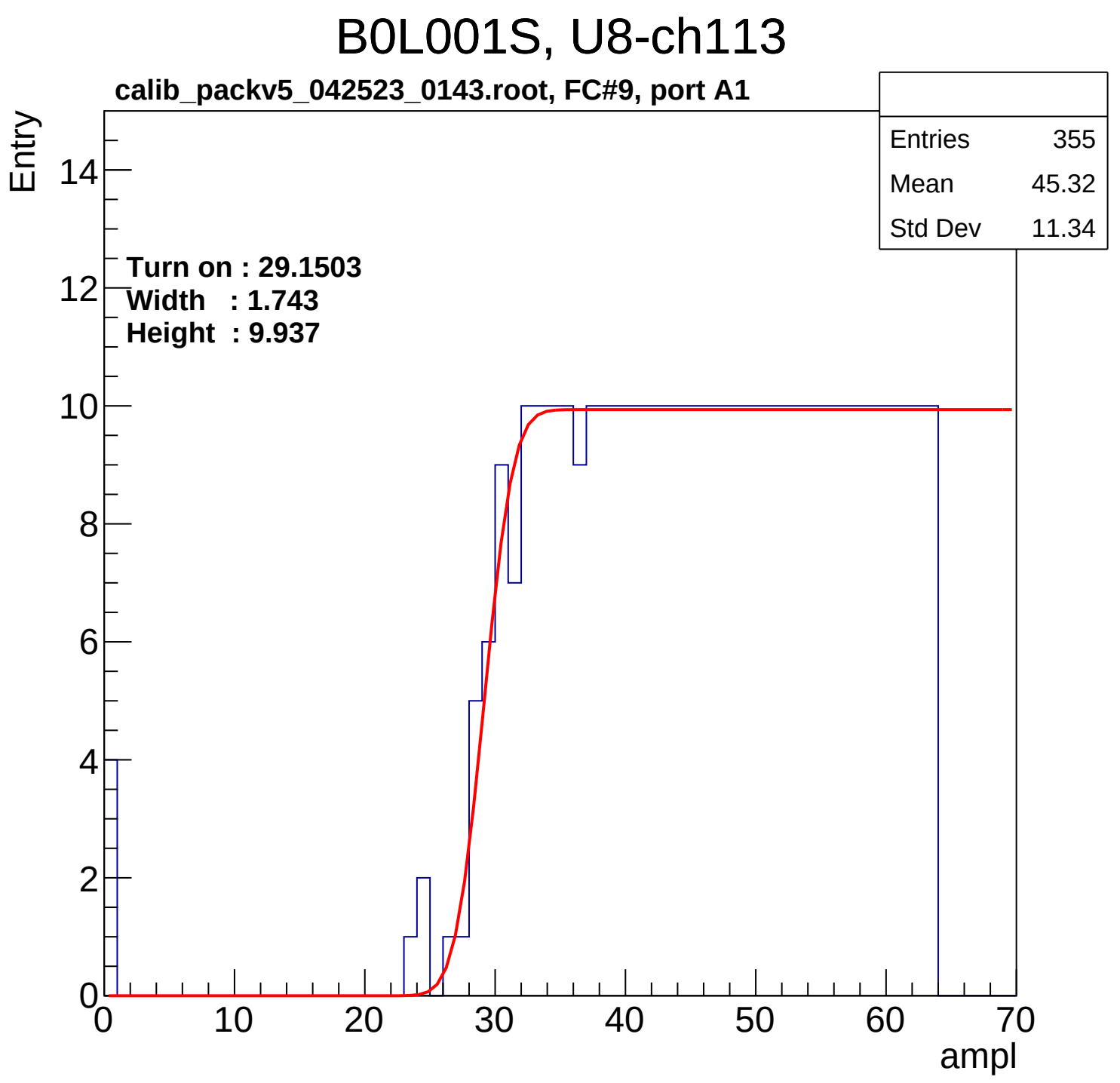
B0L001S, U8-ch113
calib_packv5_042523_0143.root, FC#9, port A1
Entries 355
Mean 45.32
Std Dev 11.34
Turn on : 29.1503
Width : 1.743
Height : 9.937
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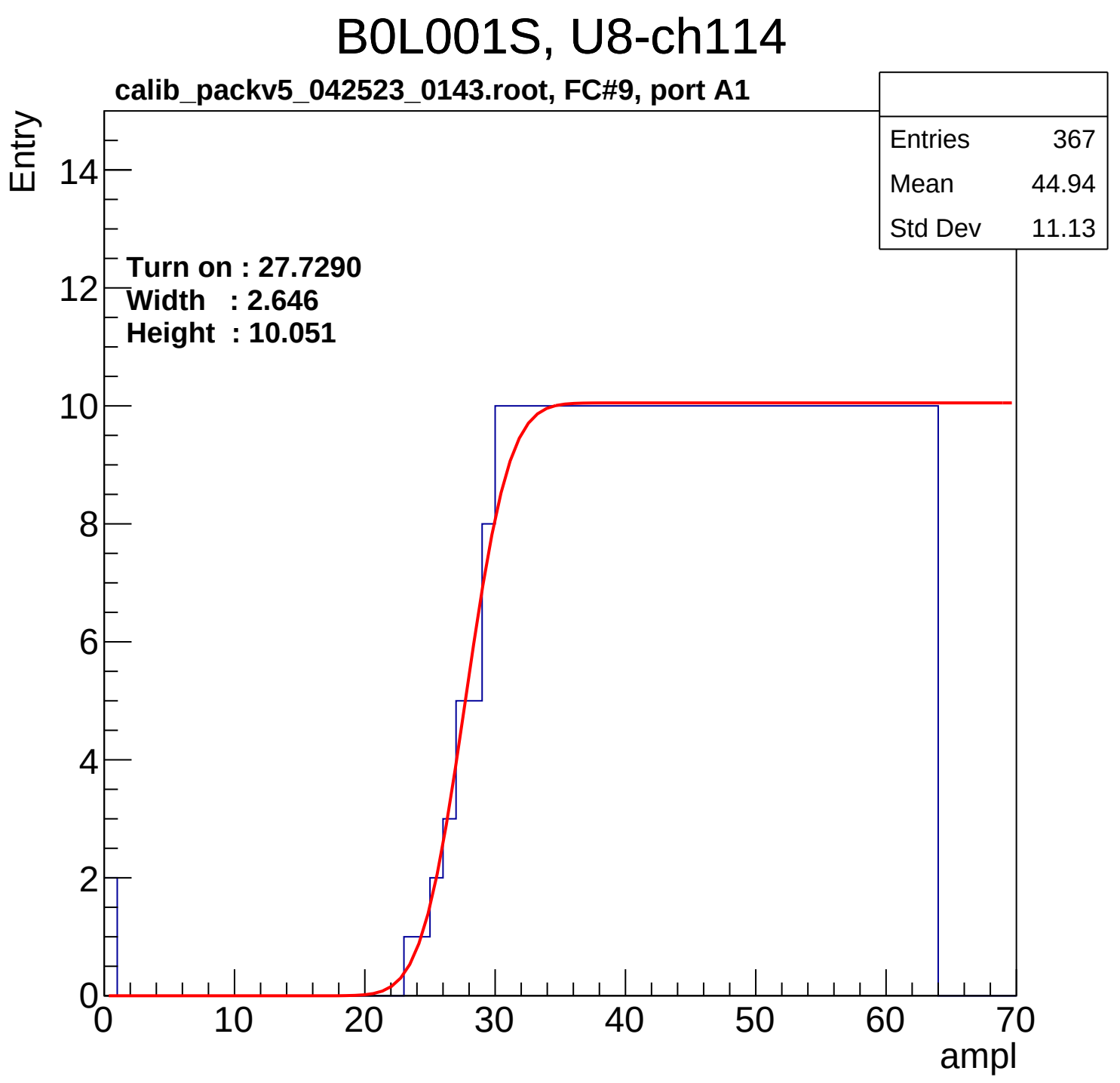
B0L001S, U8-ch114
calib_packv5_042523_0143.root, FC#9, port A1
Entries 367
Mean 44.94
Std Dev 11.13
Turn on : 27.7290
Width : 2.646
Height : 10.051
Entry
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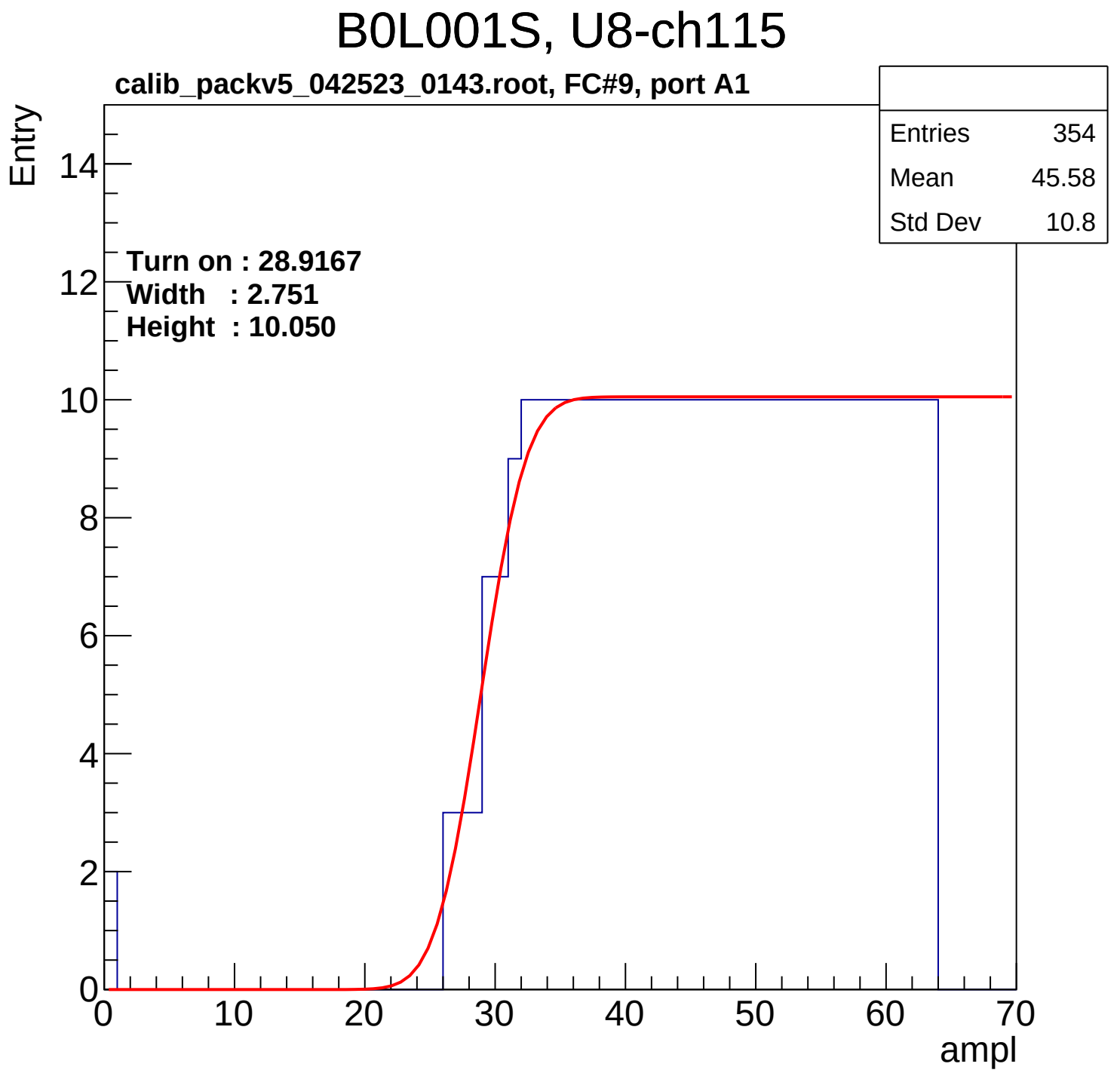
B0L001S, U8-ch115
calib_packv5_042523_0143.root, FC#9, port A1
Entries 354
Mean 45.58
Std Dev 10.8
Turn on : 28.9167
Width : 2.751
Height : 10.050
Entry
ampl
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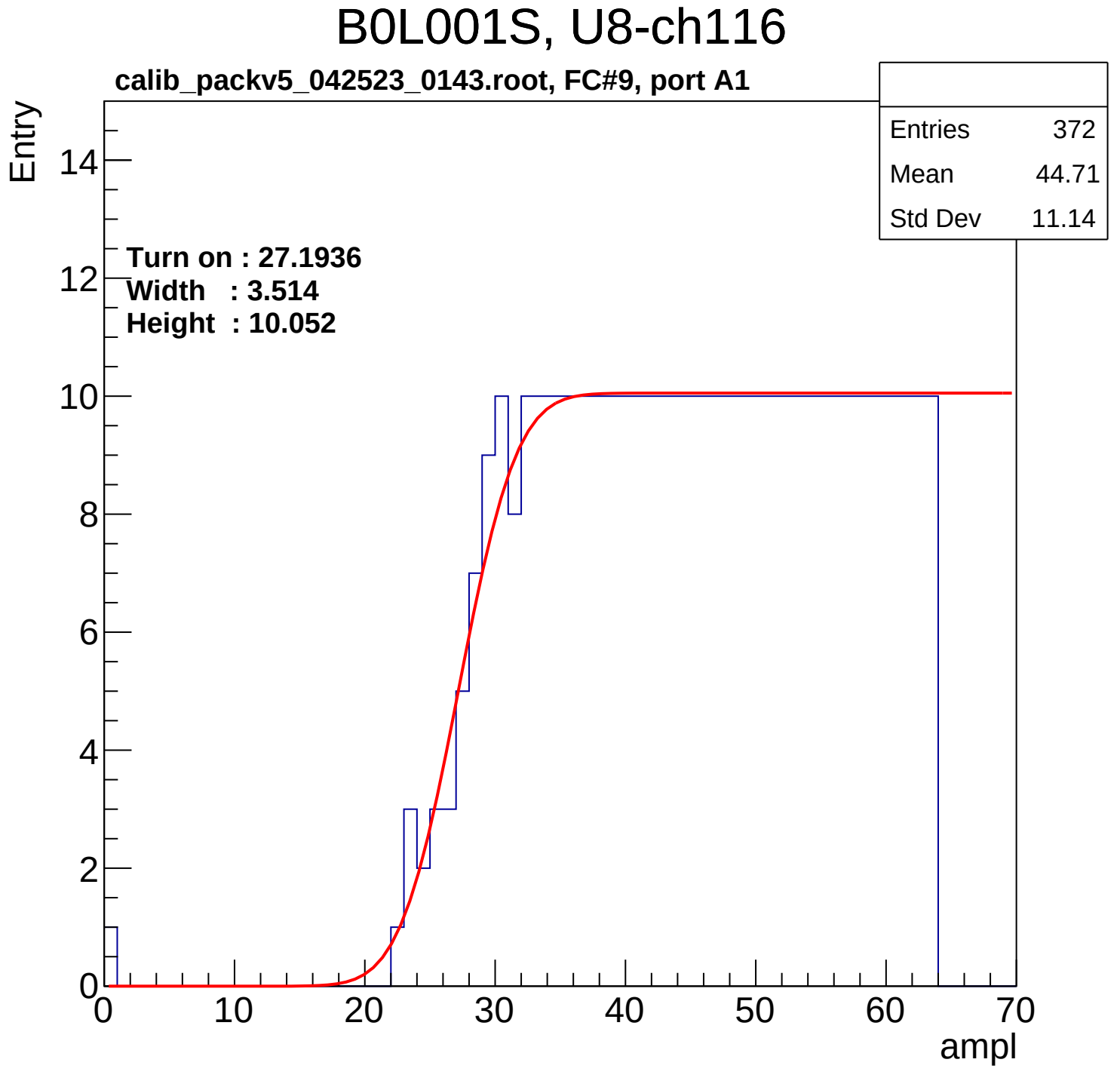
B0L001S, U8-ch116
calib_packv5_042523_0143.root, FC#9, port A1
Entries 372
Mean 44.71
Std Dev 11.14
Turn on : 27.1936
Width : 3.514
Height : 10.052
Entry
ampl
0
2
4
6
8
10
12
14
0
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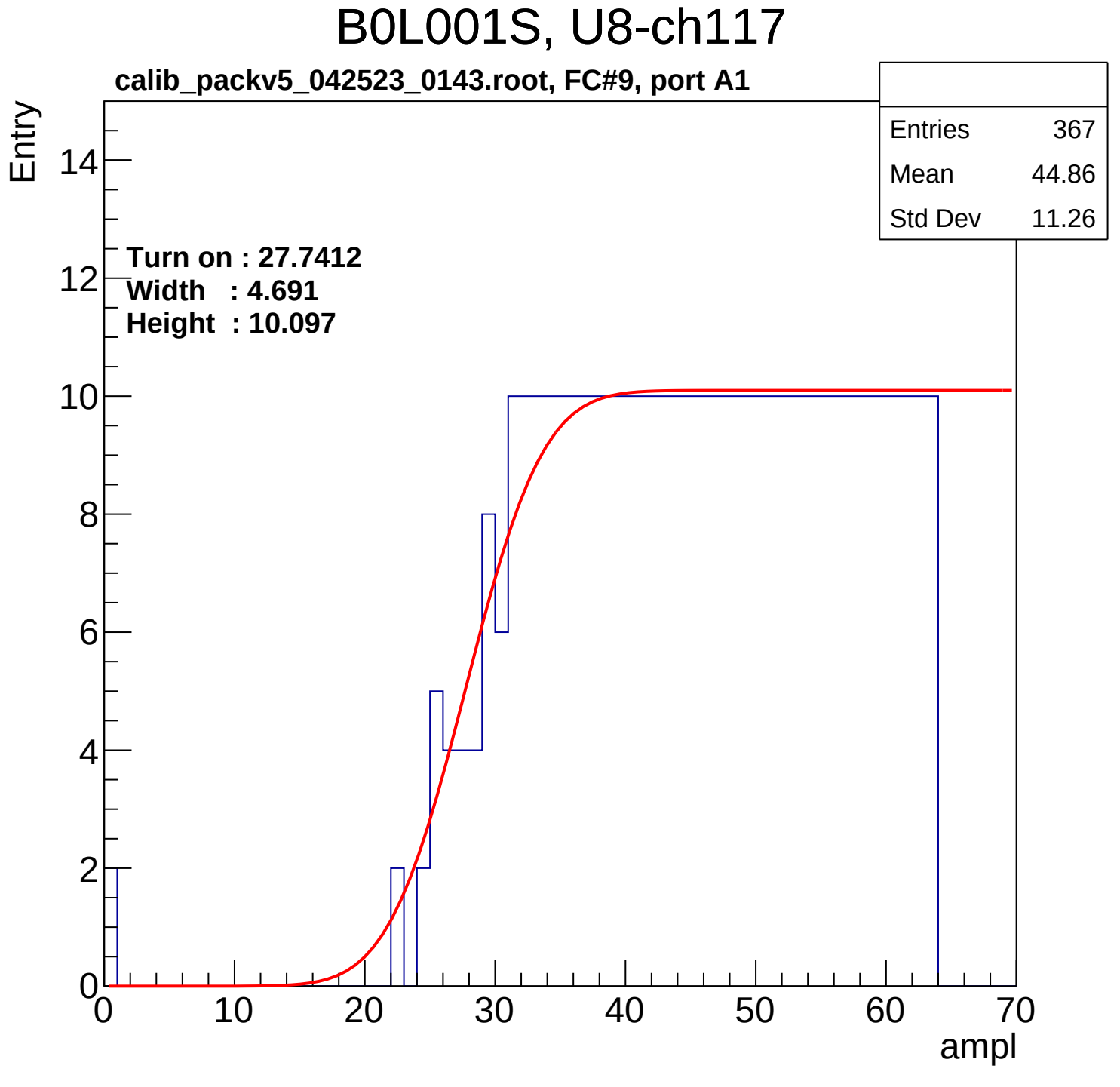
B0L001S, U8-ch117
calib_packv5_042523_0143.root, FC#9, port A1
Entries 367
Mean 44.86
Std Dev 11.26
Turn on : 27.7412
Width : 4.691
Height : 10.097
Entry
ampl
0
2
4
6
8
10
12
14
0
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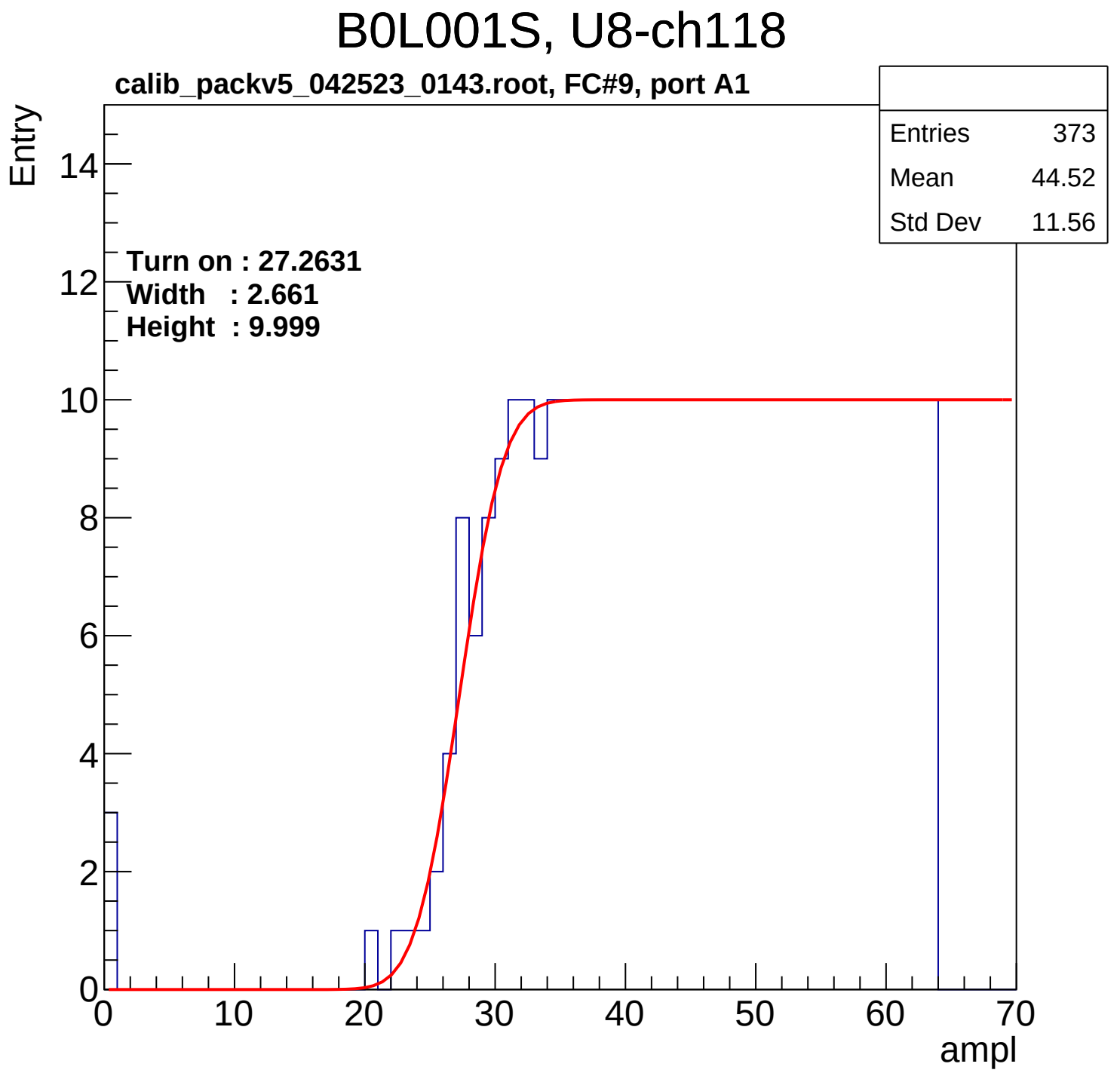
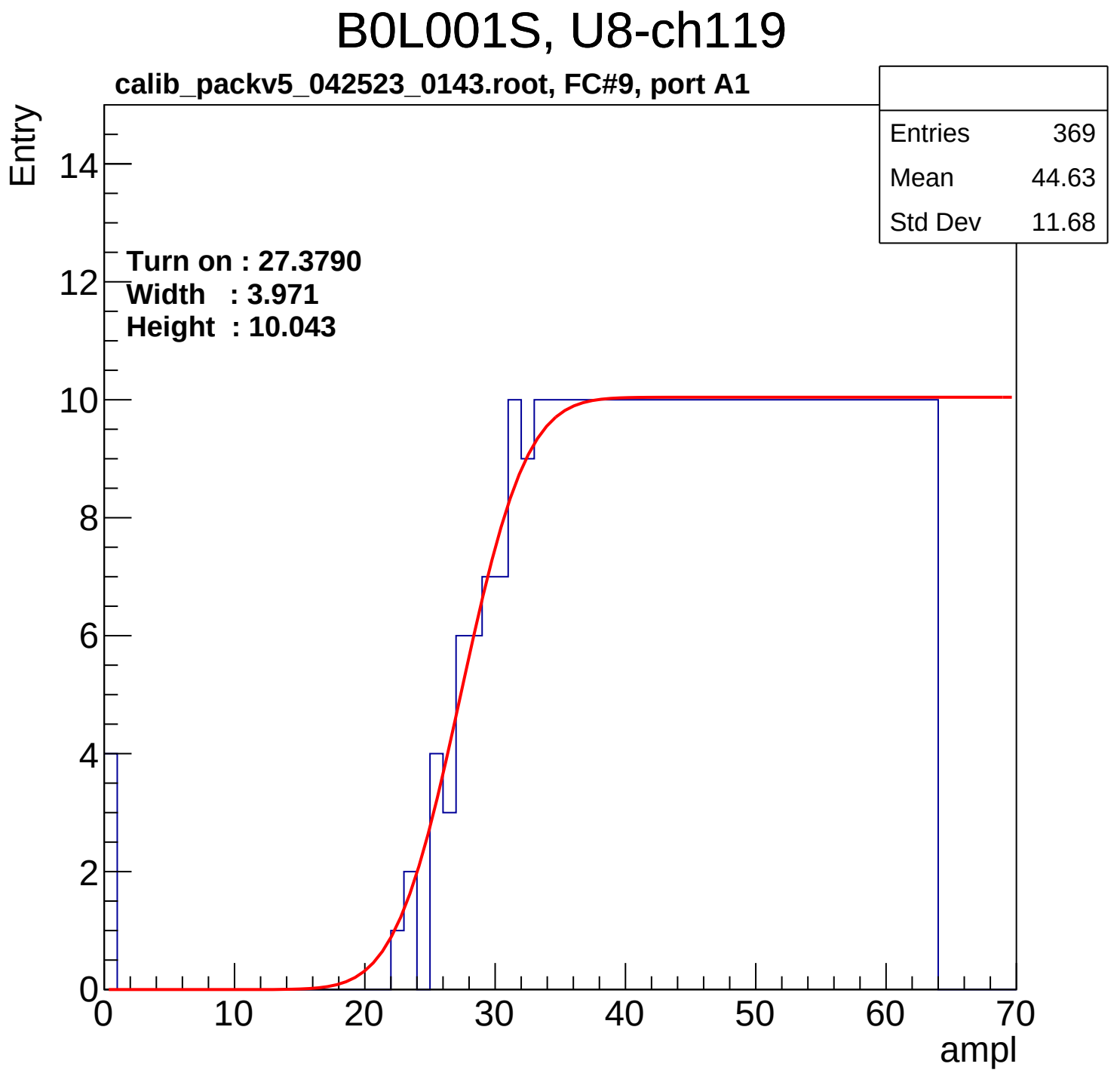
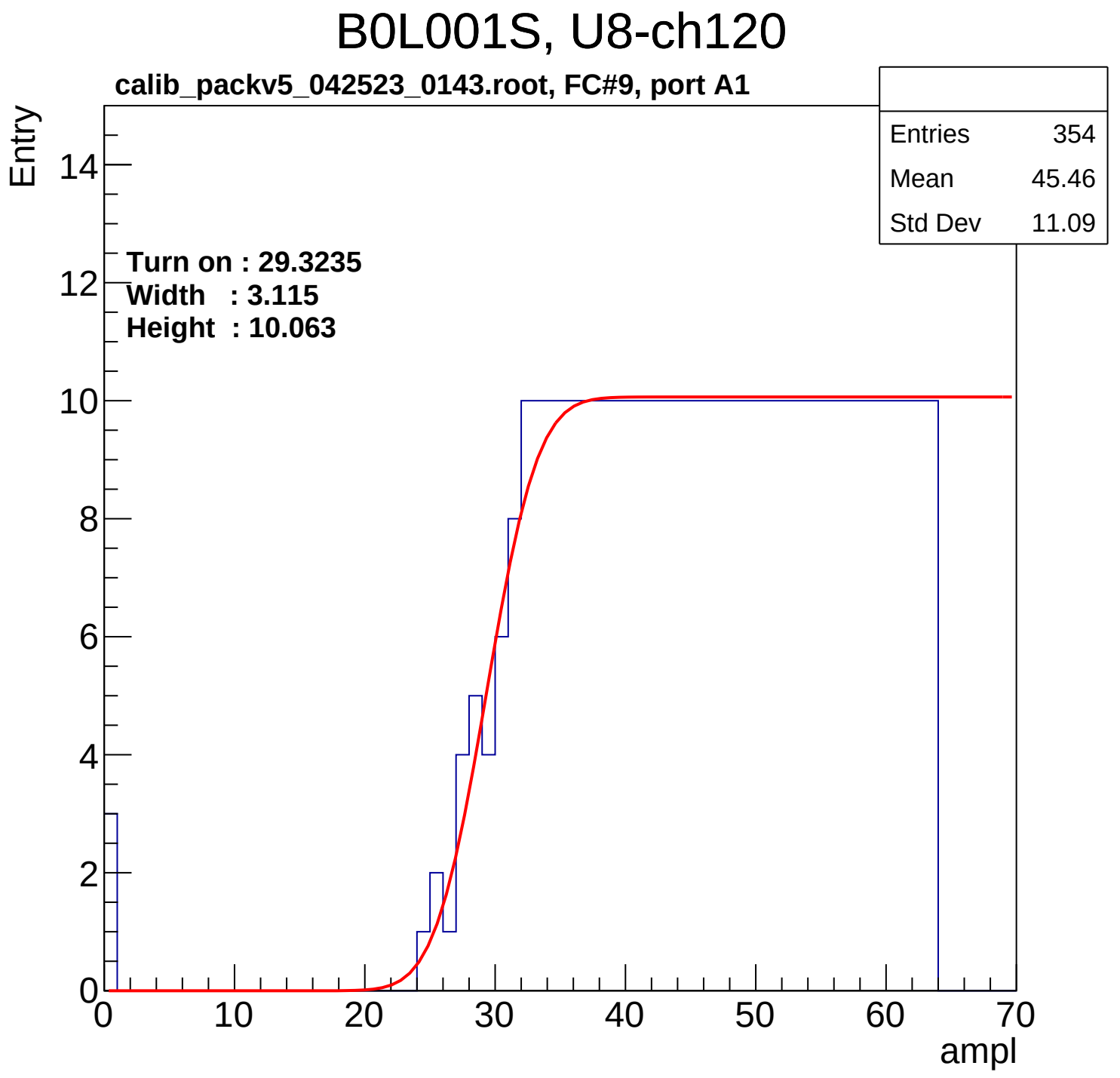

B0L001S, U8-ch118
calib_packv5_042523_0143.root, FC#9, port A1
Entries 373
Mean 44.52
Std Dev 11.56
Turn on : 27.2631
Width : 2.661
Height : 9.999
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L001S, U8-ch119
calib_packv5_042523_0143.root, FC#9, port A1
Entries 369
Mean 44.63
Std Dev 11.68
Turn on : 27.3790
Width : 3.971
Height : 10.043
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L001S, U8-ch120
calib_packv5_042523_0143.root, FC#9, port A1
Entries 354
Mean 45.46
Std Dev 11.09
Turn on : 29.3235
Width : 3.115
Height : 10.063
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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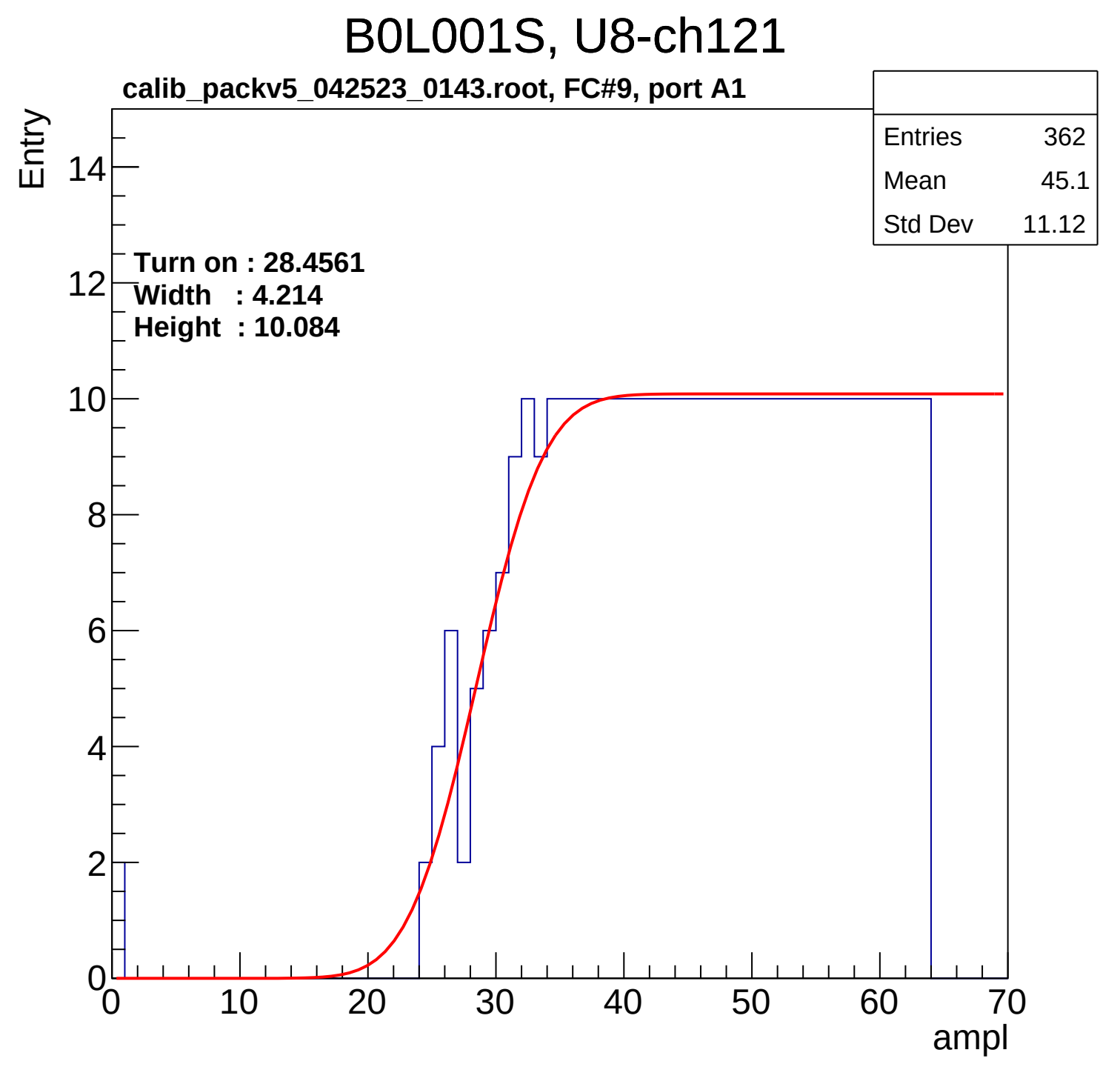
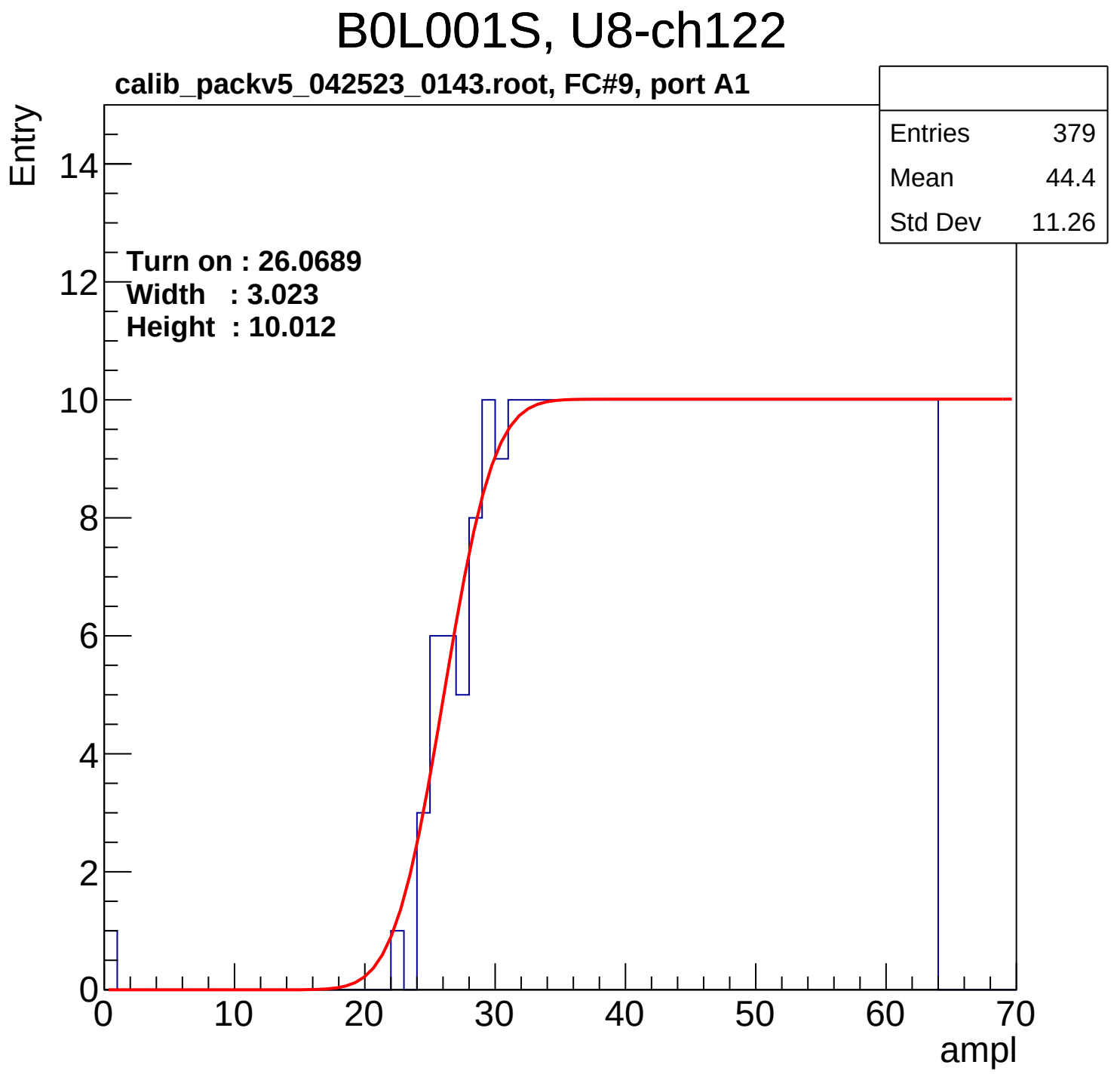
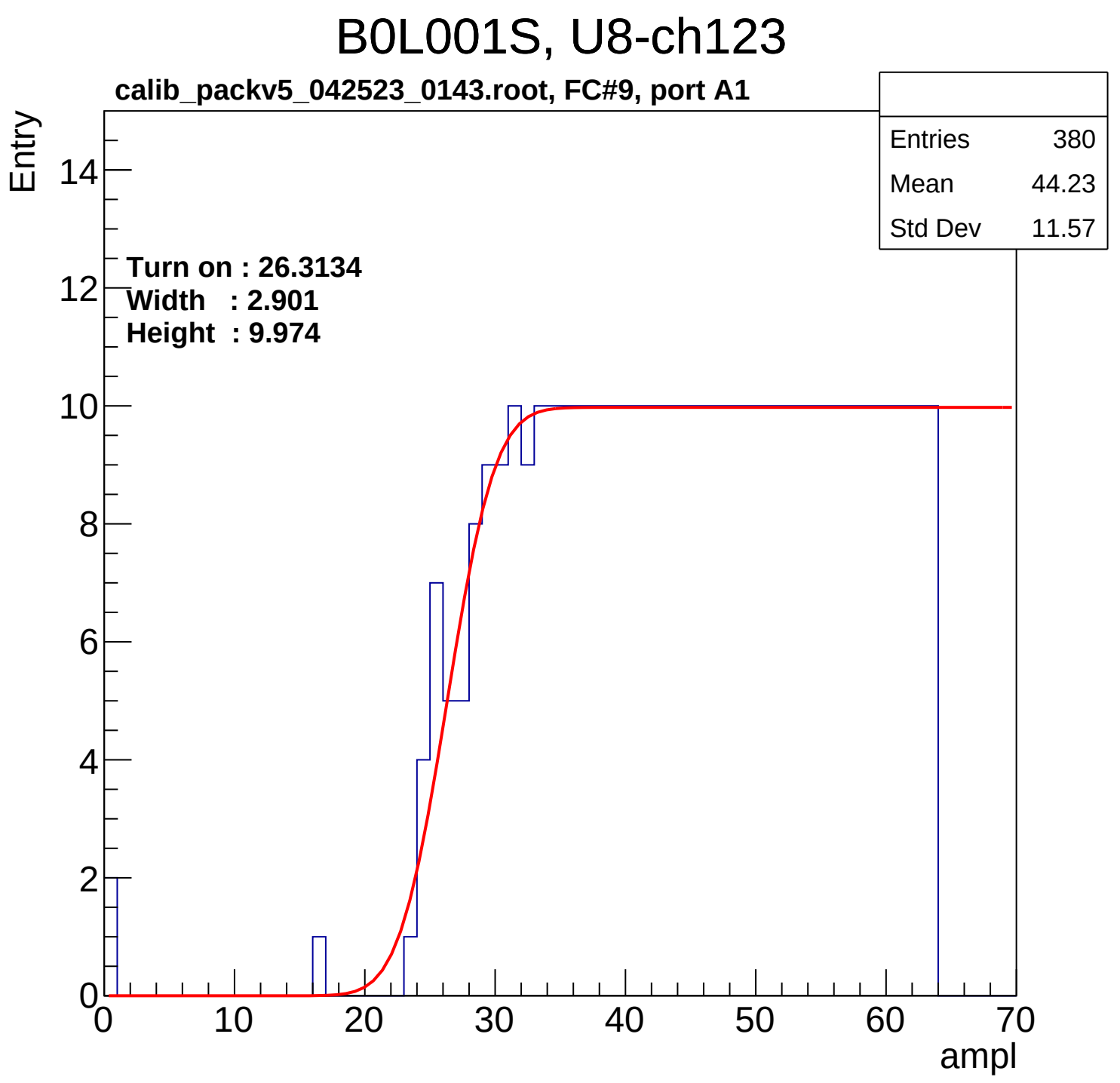
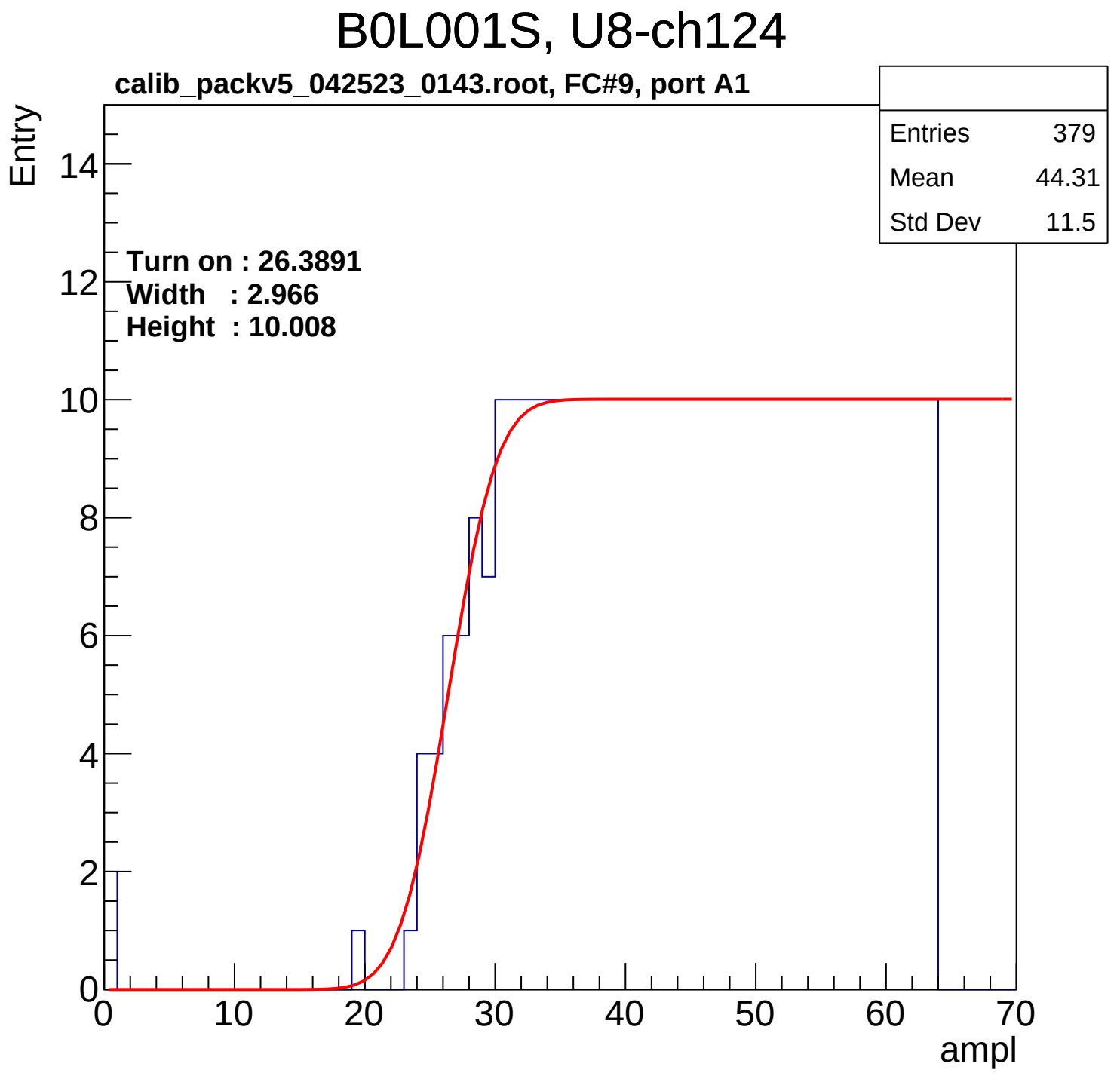
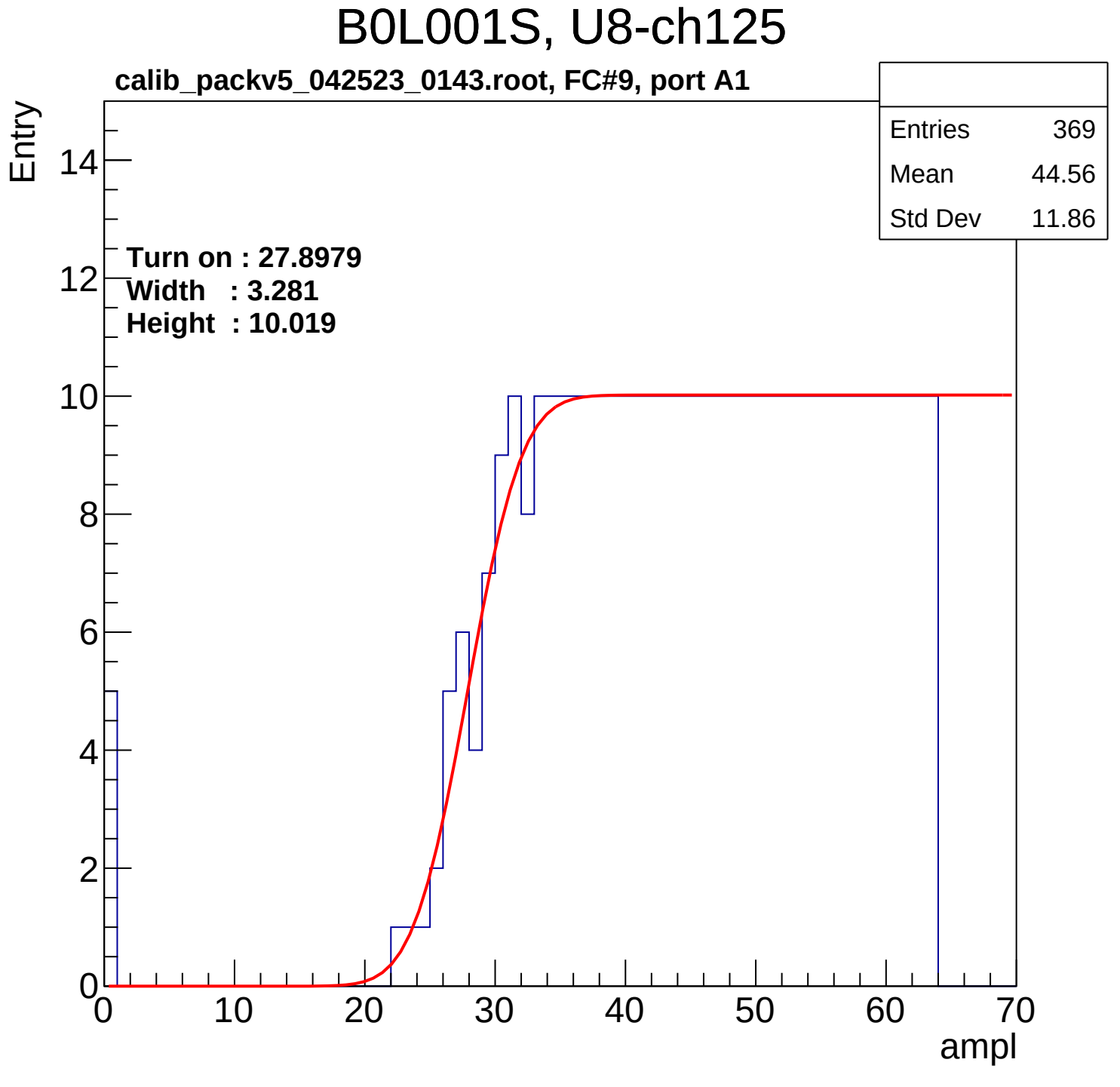
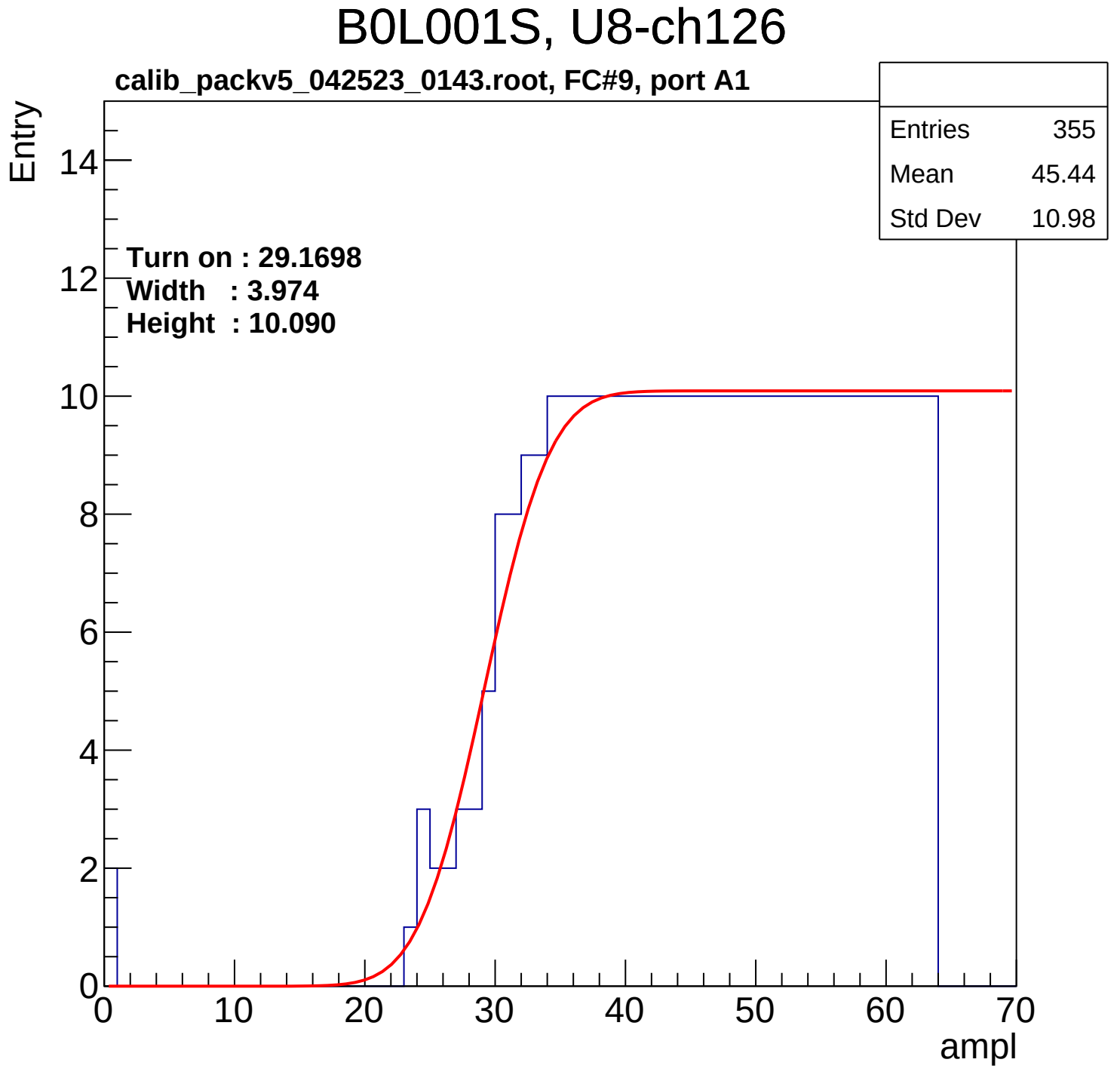

B0L001S, U8-ch121
calib_packv5_042523_0143.root, FC#9, port A1
Entries 362
Mean 45.1
Std Dev 11.12
Turn on : 28.4561
Width : 4.214
Height : 10.084
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L001S, U8-ch122
calib_packv5_042523_0143.root, FC#9, port A1
Entries 379
Mean 44.4
Std Dev 11.26
Turn on : 26.0689
Width : 3.023
Height : 10.012
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L001S, U8-ch123
calib_packv5_042523_0143.root, FC#9, port A1
Entries 380
Mean 44.23
Std Dev 11.57
Turn on : 26.3134
Width : 2.901
Height : 9.974
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L001S, U8-ch124
calib_packv5_042523_0143.root, FC#9, port A1
Entries 379
Mean 44.31
Std Dev 11.5
Turn on : 26.3891
Width : 2.966
Height : 10.008
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L001S, U8-ch125
calib_packv5_042523_0143.root, FC#9, port A1
Entries 369
Mean 44.56
Std Dev 11.86
Turn on : 27.8979
Width : 3.281
Height : 10.019
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L001S, U8-ch126
calib_packv5_042523_0143.root, FC#9, port A1
Entries 355
Mean 45.44
Std Dev 10.98
Turn on : 29.1698
Width : 3.974
Height : 10.090
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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40
50
60
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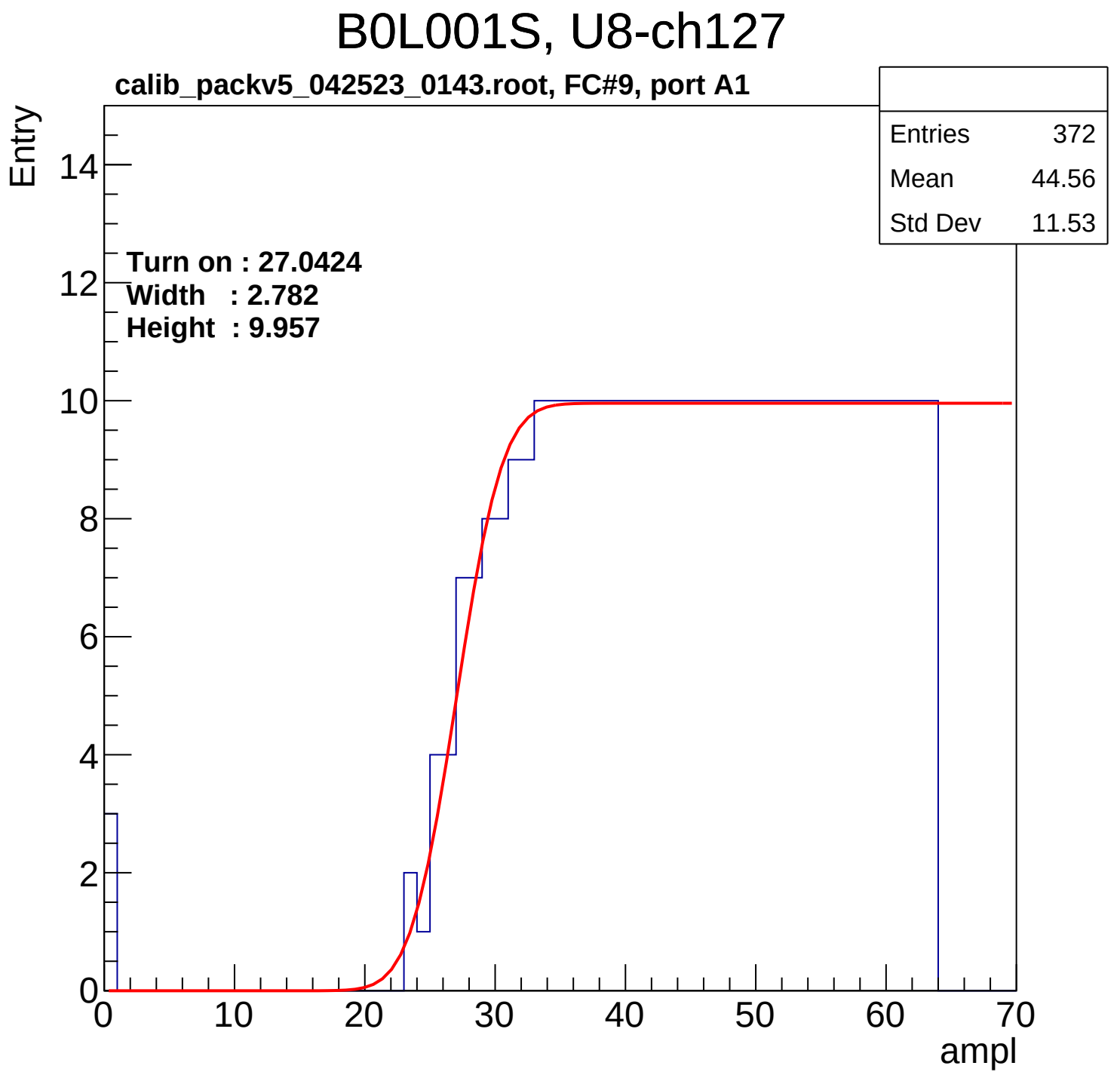
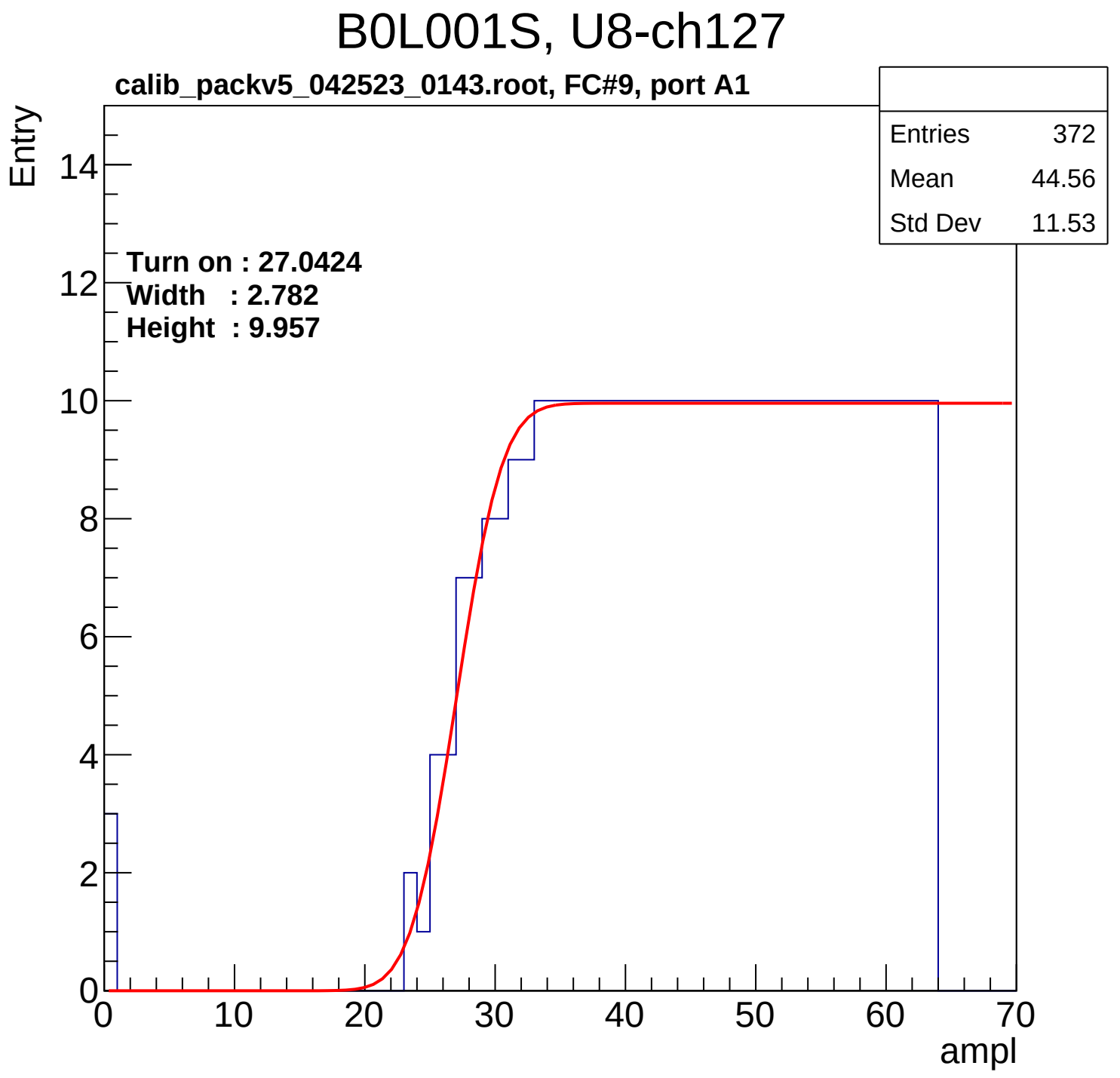

B0L001S, U8-ch127
calib_packv5_042523_0143.root, FC#9, port A1
Entries 372
Mean 44.56
Std Dev 11.53
Turn on : 27.0424
Width : 2.782
Height : 9.957
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L001S, U8-ch127
calib_packv5_042523_0143.root, FC#9, port A1
Entries 372
Mean 44.56
Std Dev 11.53
Turn on : 27.0424
Width : 2.782
Height : 9.957
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70