

B1L103S, U18-ch0

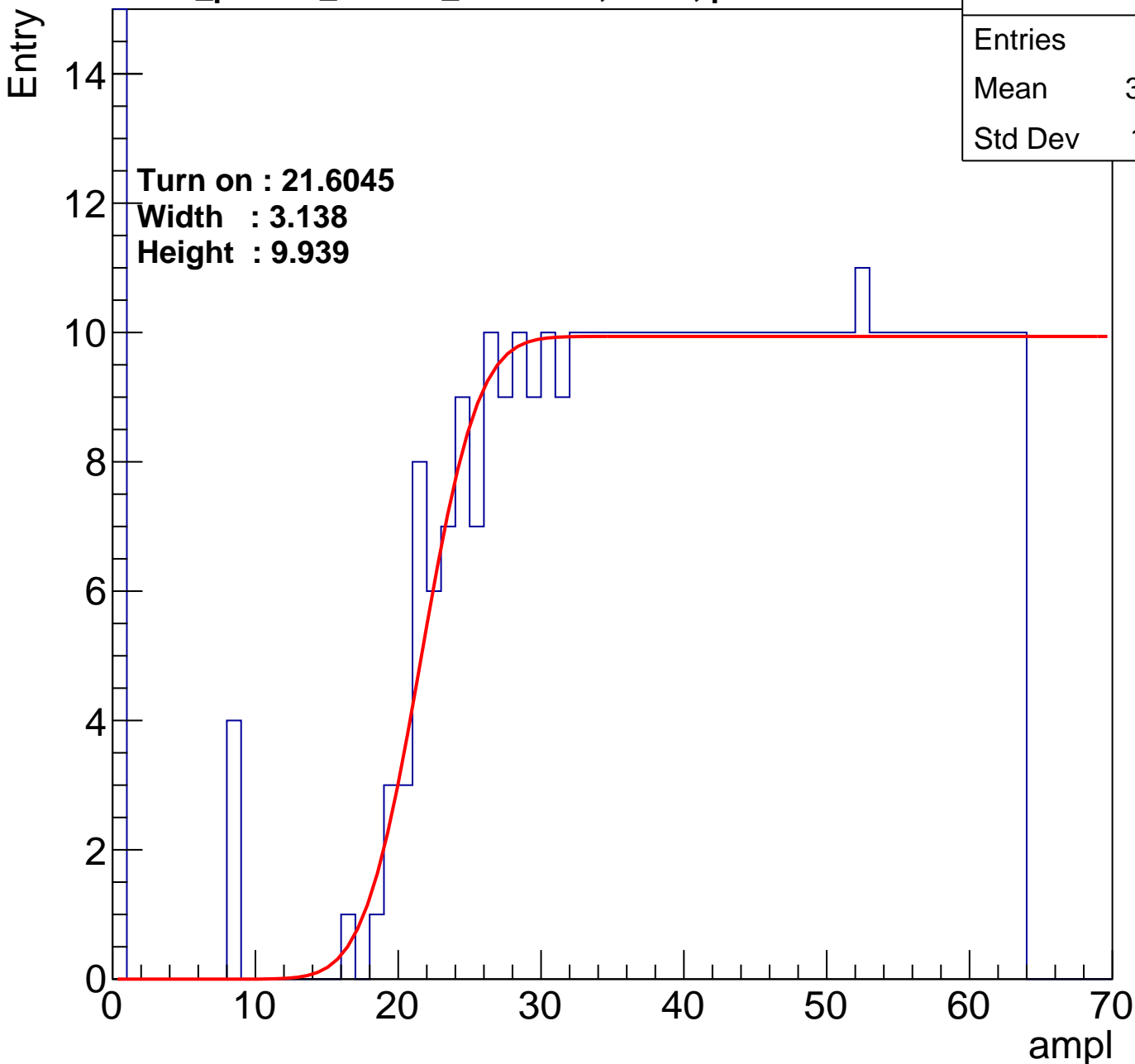
calib_packv5_041523_1651.root, FC#0, port C2

Entries	481
Mean	37.23
Std Dev	17.91

Turn on : 21.6045

Width : 3.138

Height : 9.939



B1L103S, U18-ch1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	424
Mean	39.92
Std Dev	16.93

Turn on : 26.2835

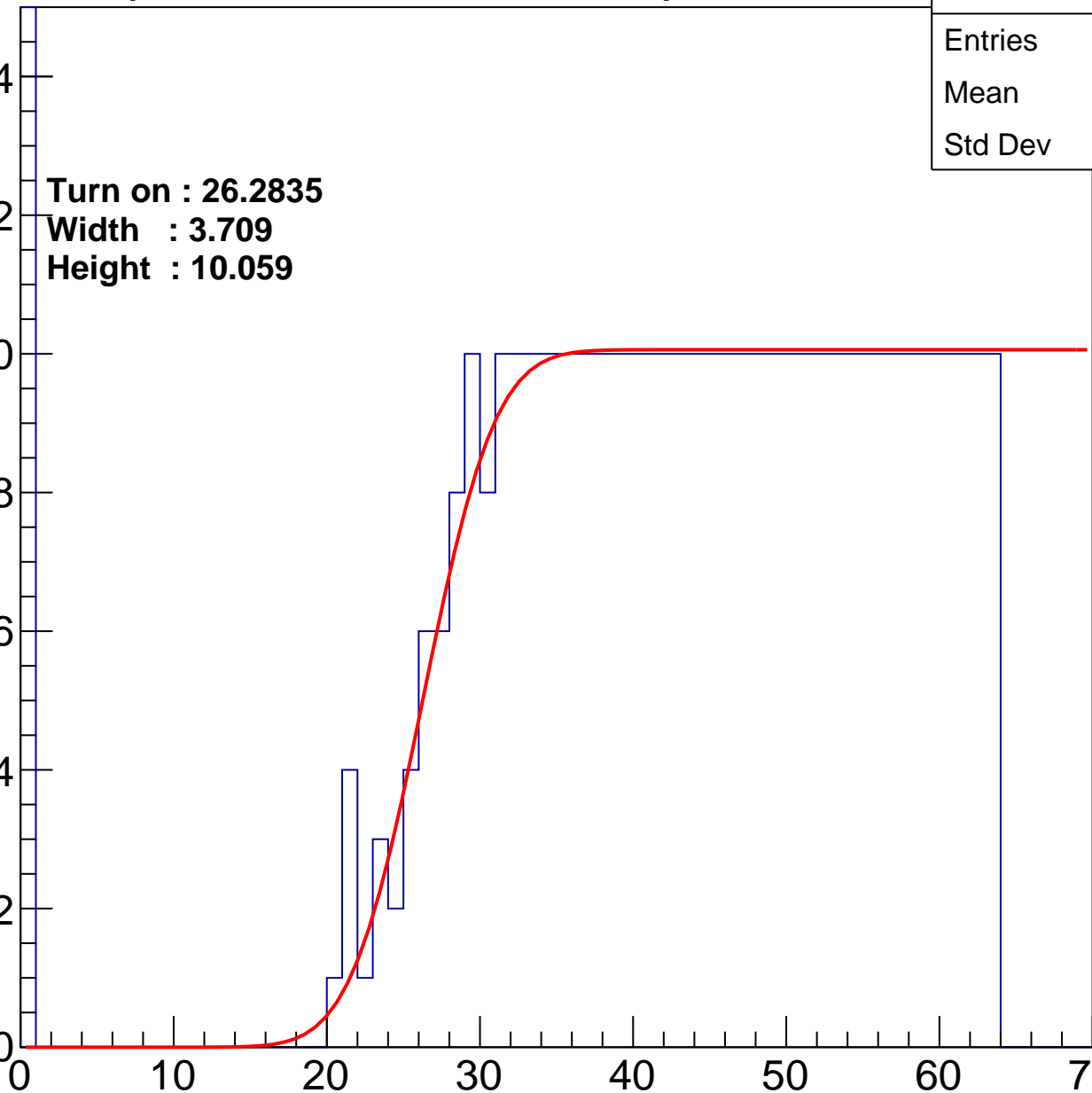
Width : 3.709

Height : 10.059

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U18-ch2

calib_packv5_041523_1651.root, FC#0, port C2

Entries	448
Mean	37.99
Std Dev	18.46

Turn on : 25.6603

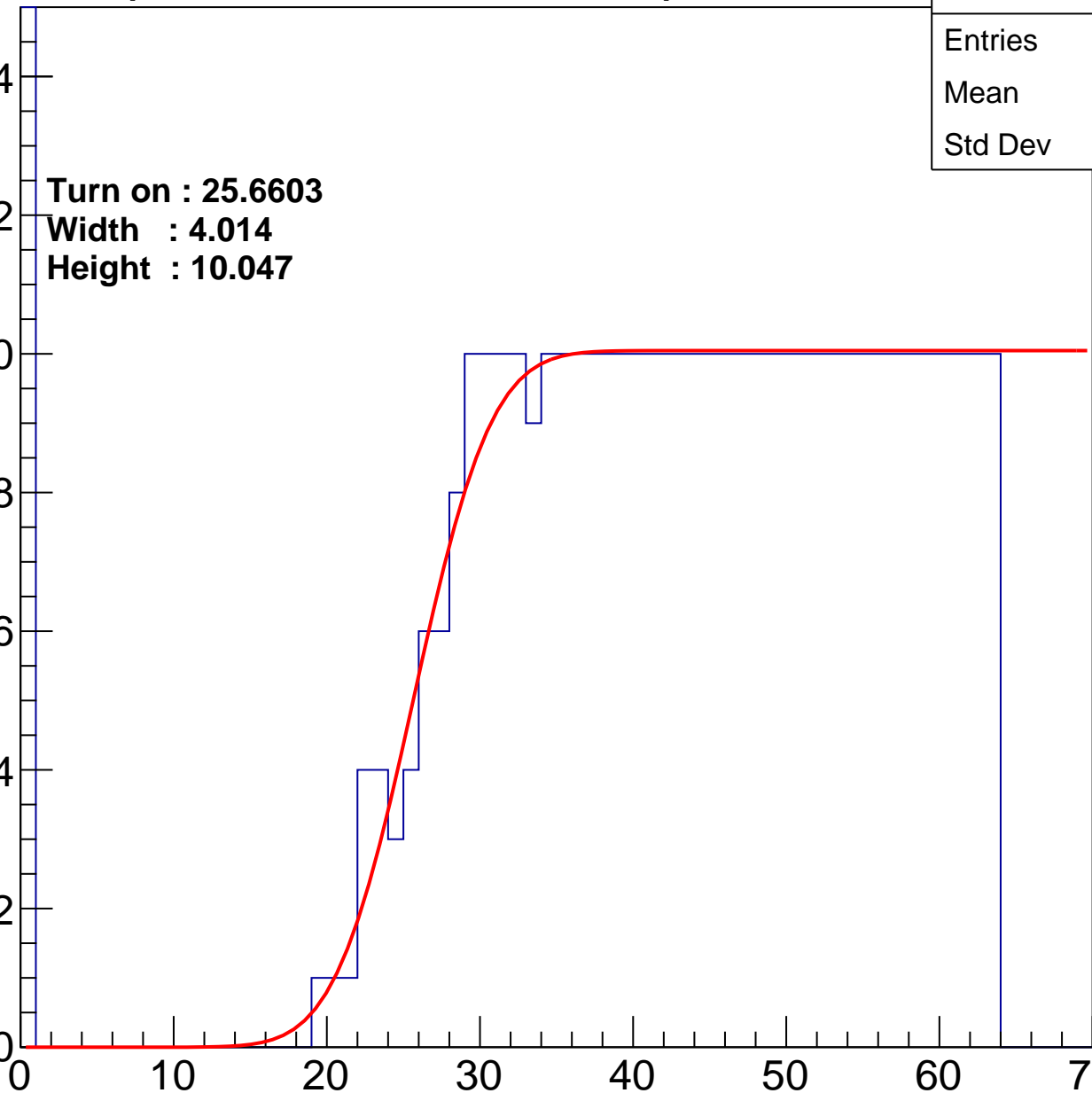
Width : 4.014

Height : 10.047

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U18-ch3

calib_packv5_041523_1651.root, FC#0, port C2

Entries	437
Mean	39.15
Std Dev	17.39

Turn on : 25.9740

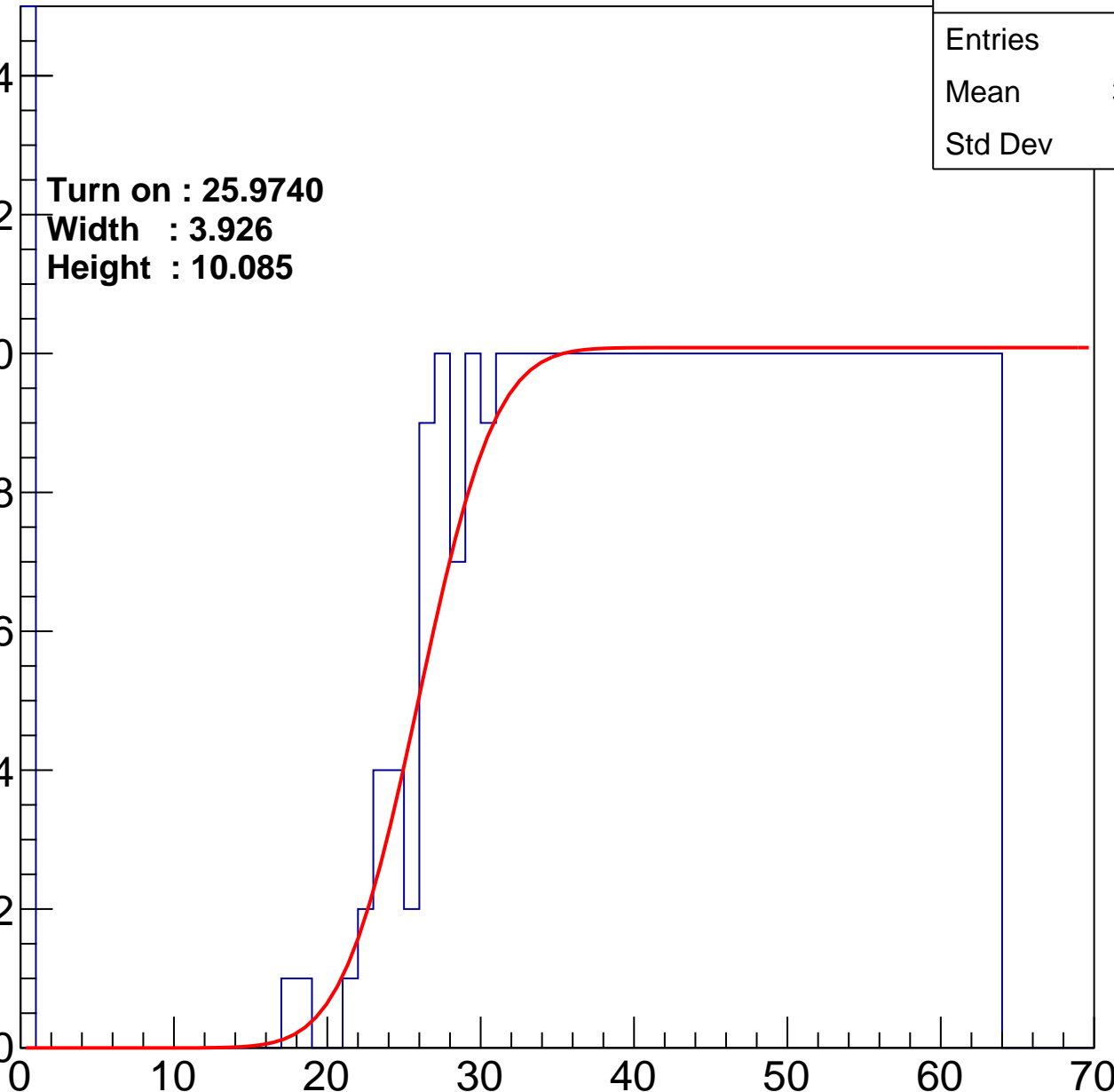
Width : 3.926

Height : 10.085

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U18-ch4

calib_packv5_041523_1651.root, FC#0, port C2

Entries	421
Mean	40.03
Std Dev	16.92

Turn on : 26.1711

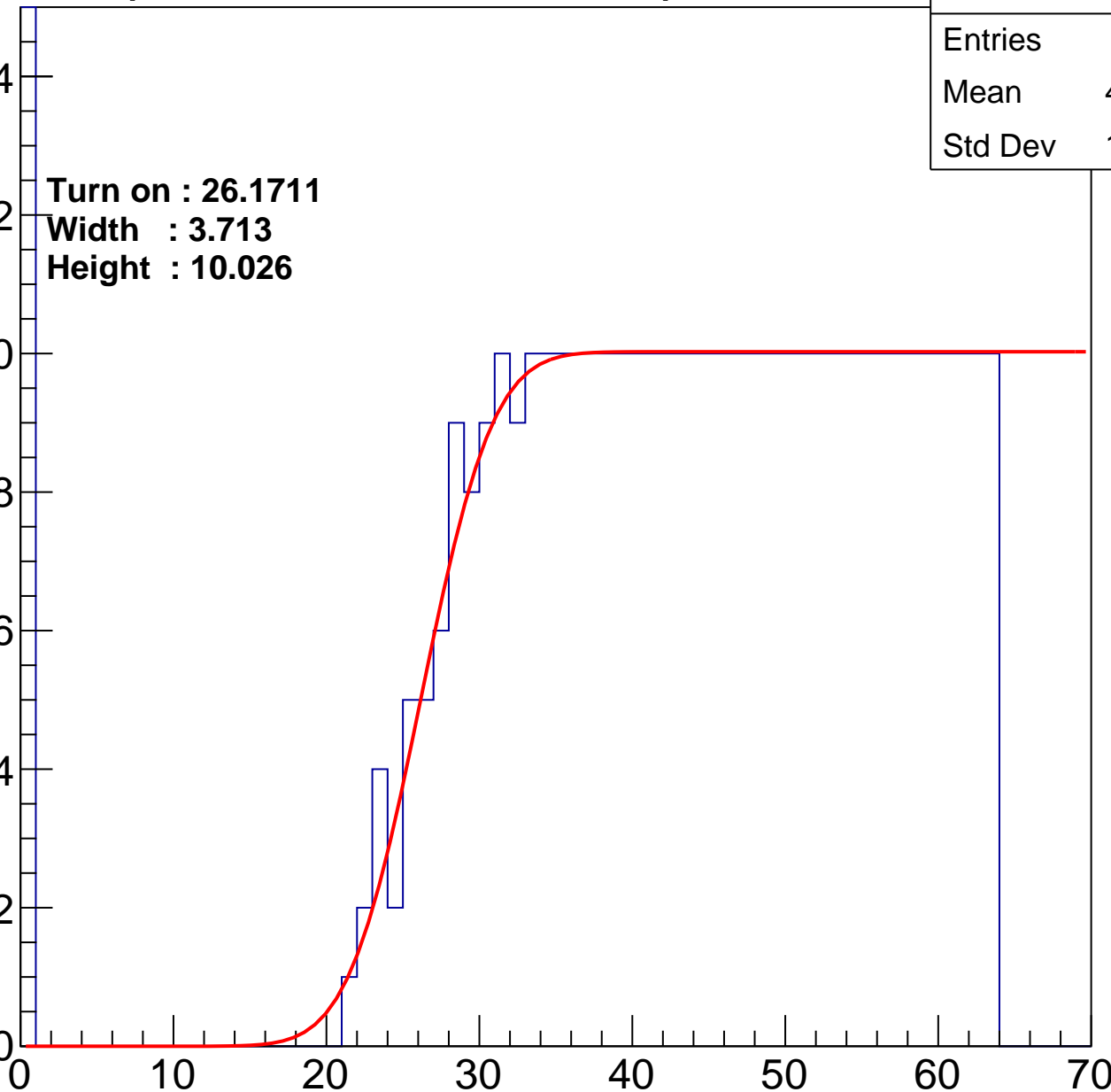
Width : 3.713

Height : 10.026

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U18-ch5

calib_packv5_041523_1651.root, FC#0, port C2

Entries	436
Mean	38.73
Std Dev	18.07

Turn on : 26.3389

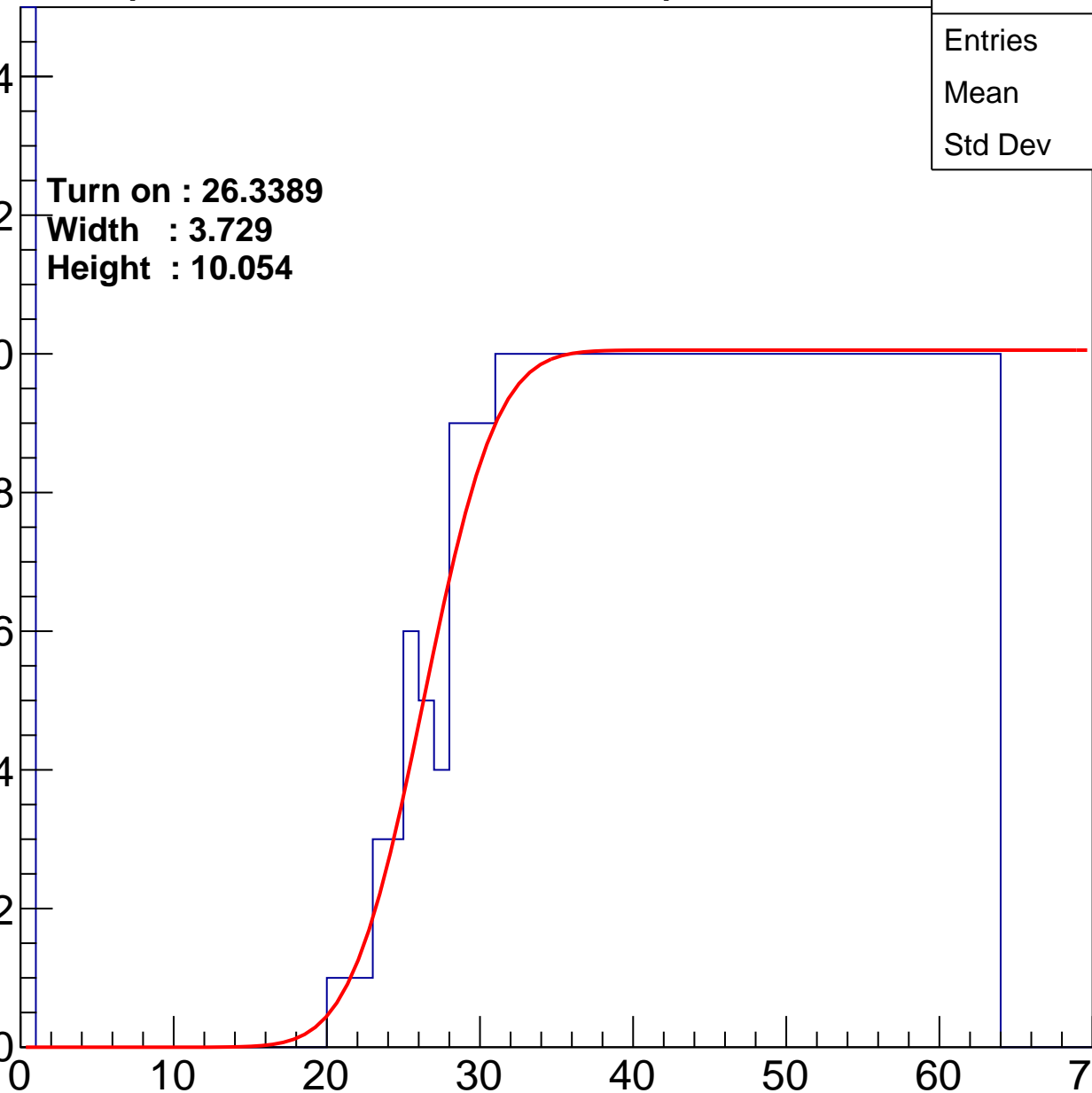
Width : 3.729

Height : 10.054

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U18-ch6

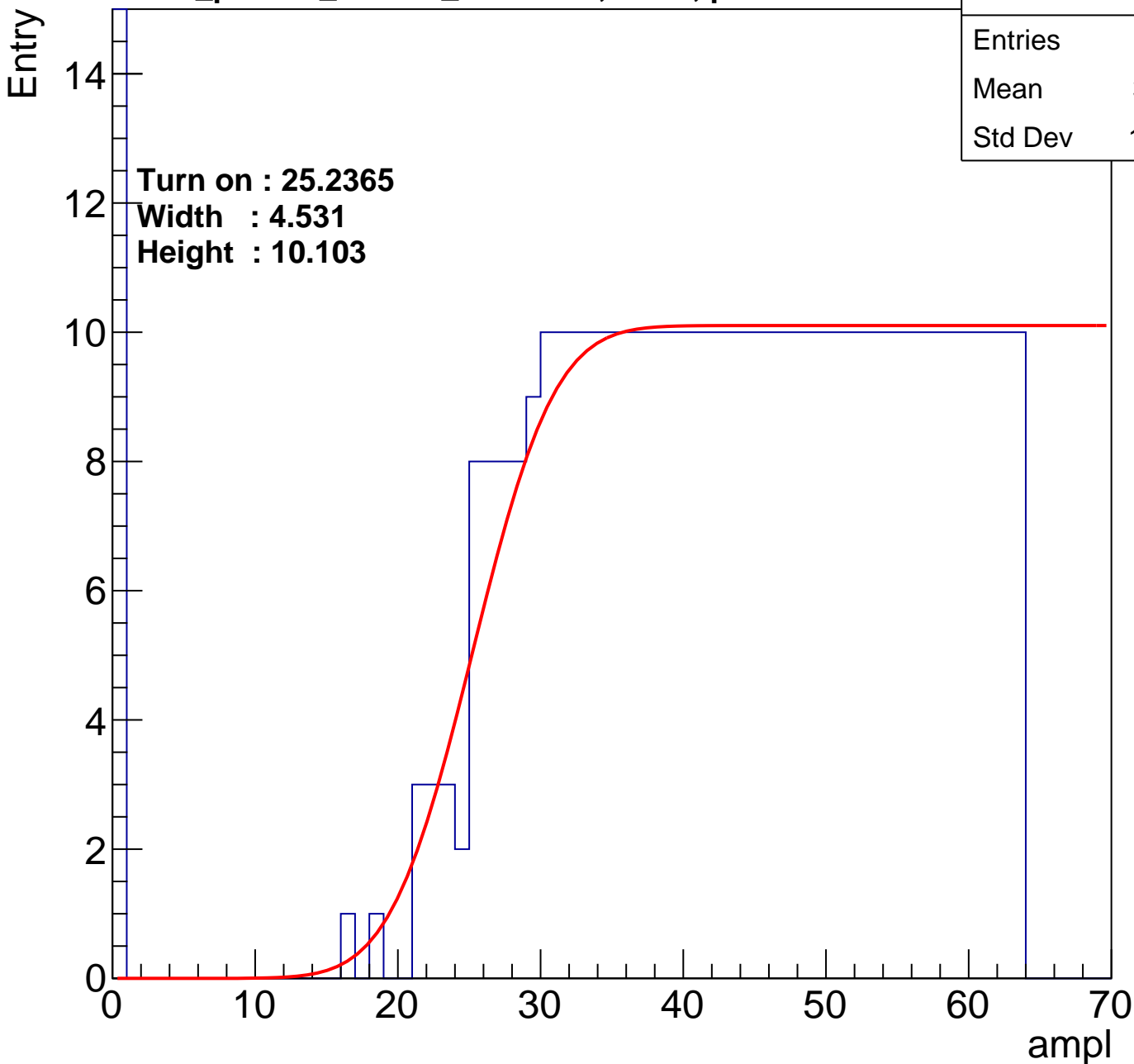
calib_packv5_041523_1651.root, FC#0, port C2

Entries	449
Mean	38.31
Std Dev	17.99

Turn on : 25.2365

Width : 4.531

Height : 10.103



B1L103S, U18-ch7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	413
Mean	39.83
Std Dev	17.73

Turn on : 27.8964

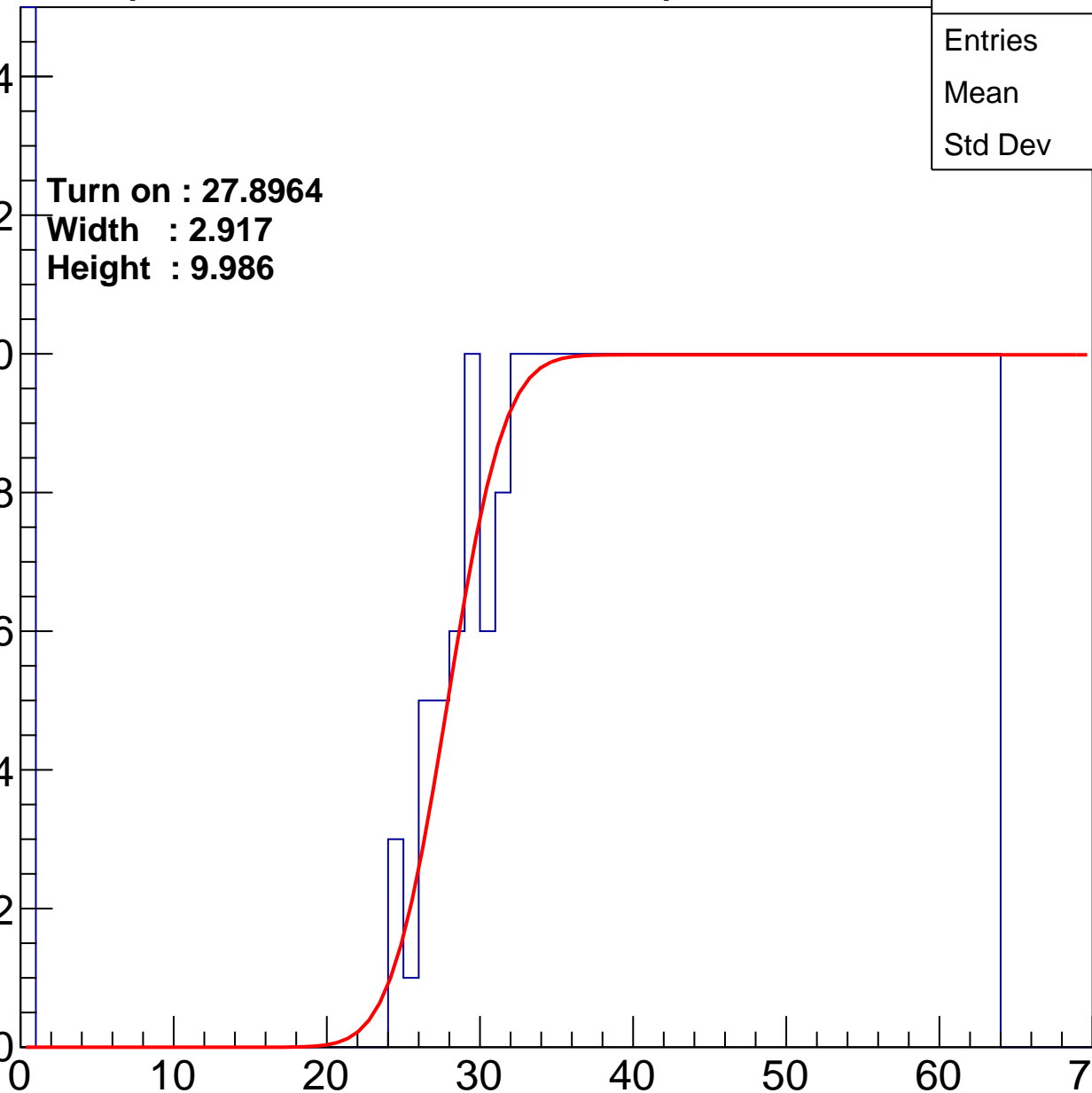
Width : 2.917

Height : 9.986

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U18-ch8

calib_packv5_041523_1651.root, FC#0, port C2

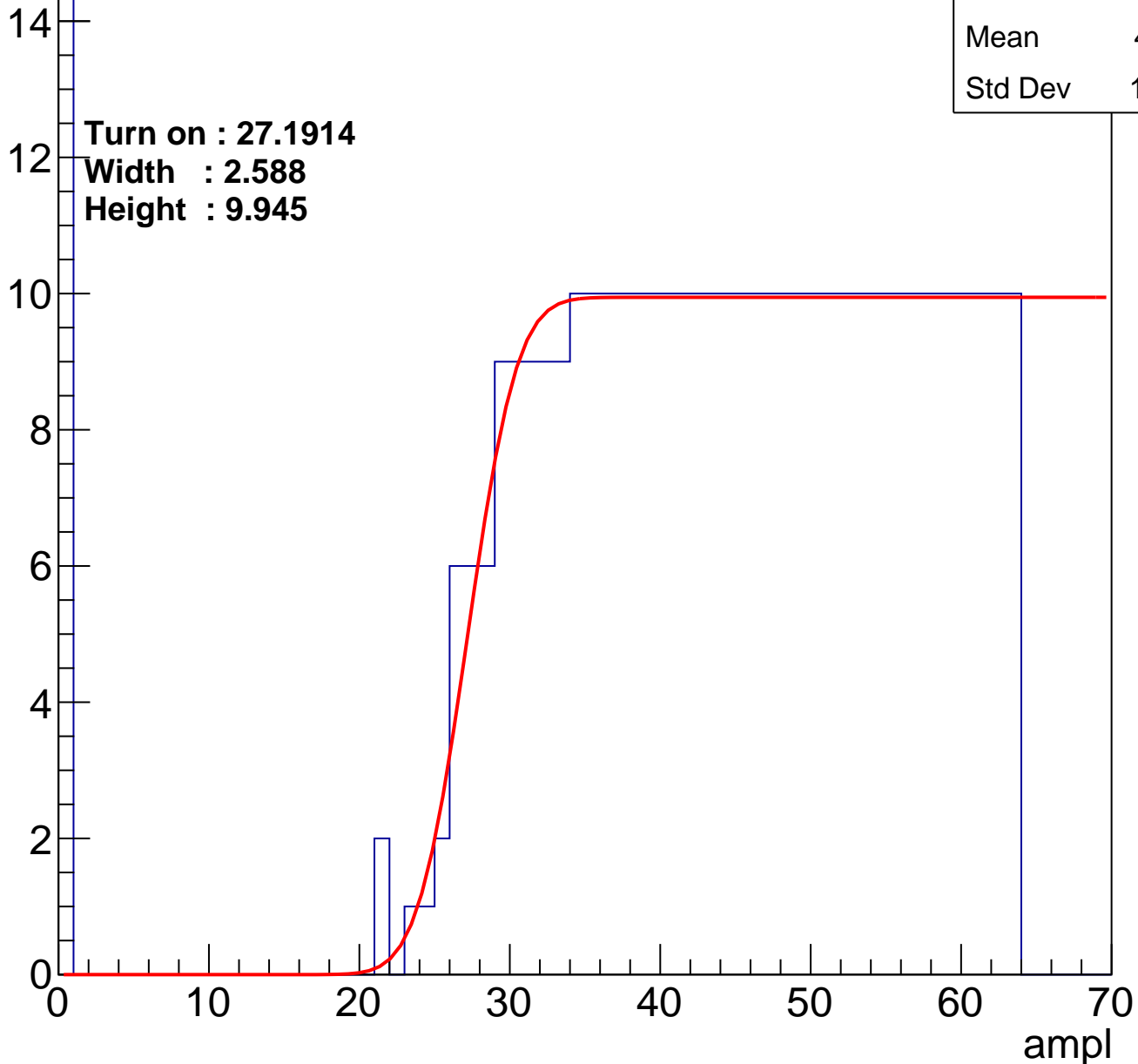
Entry

Entries	404
Mean	41.01
Std Dev	16.37

Turn on : 27.1914

Width : 2.588

Height : 9.945



B1L103S, U18-ch9

calib_packv5_041523_1651.root, FC#0, port C2

Entries	421
Mean	39.61
Std Dev	17.63

Turn on : 26.7637

Width : 2.238

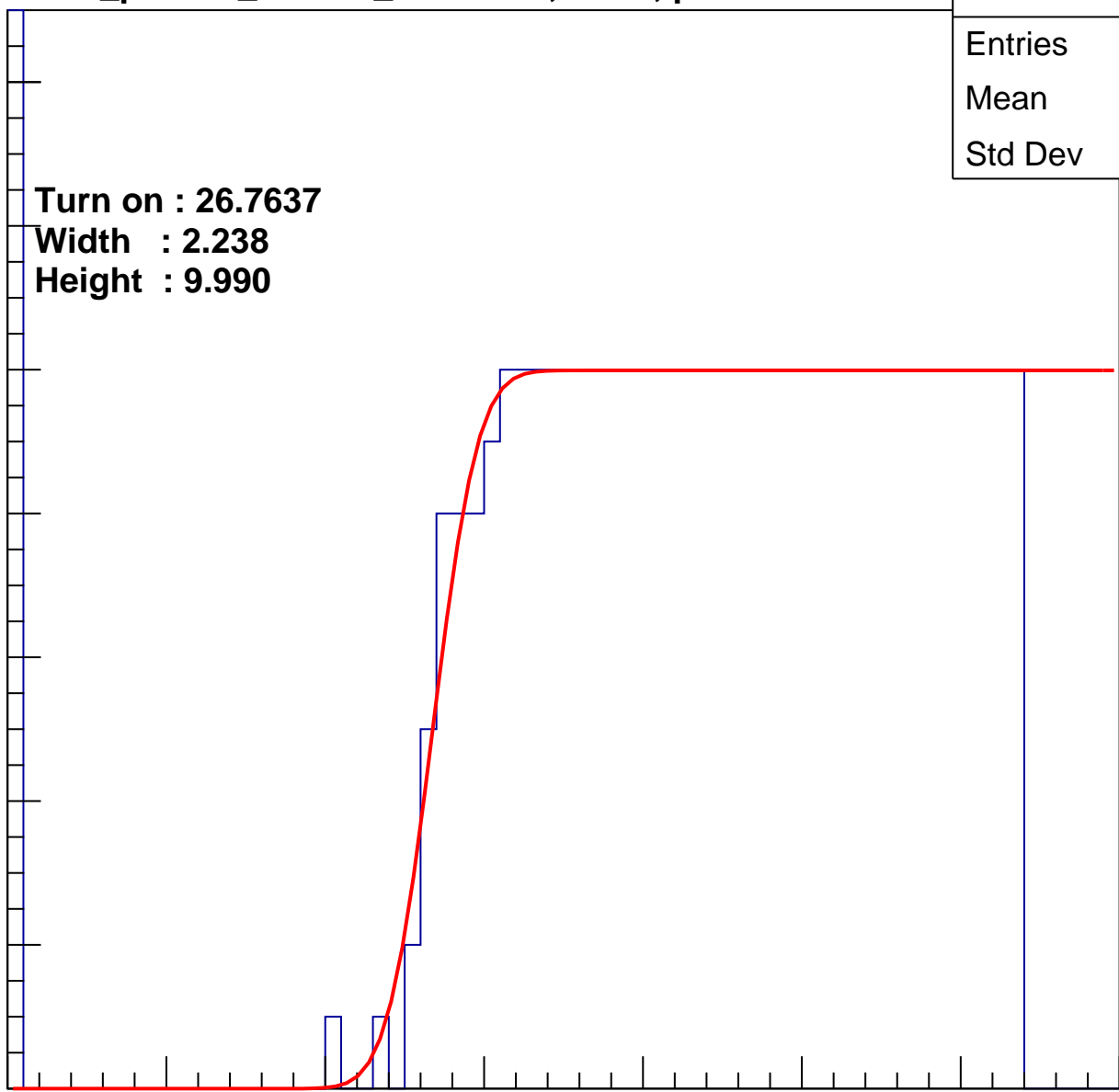
Height : 9.990

Entry

14
12
10
8
6
4
2
0

ampl

0 10 20 30 40 50 60 70



B1L103S, U18-ch10

calib_packv5_041523_1651.root, FC#0, port C2

Entries	428
Mean	39.36
Std Dev	17.56

Turn on : 26.2735

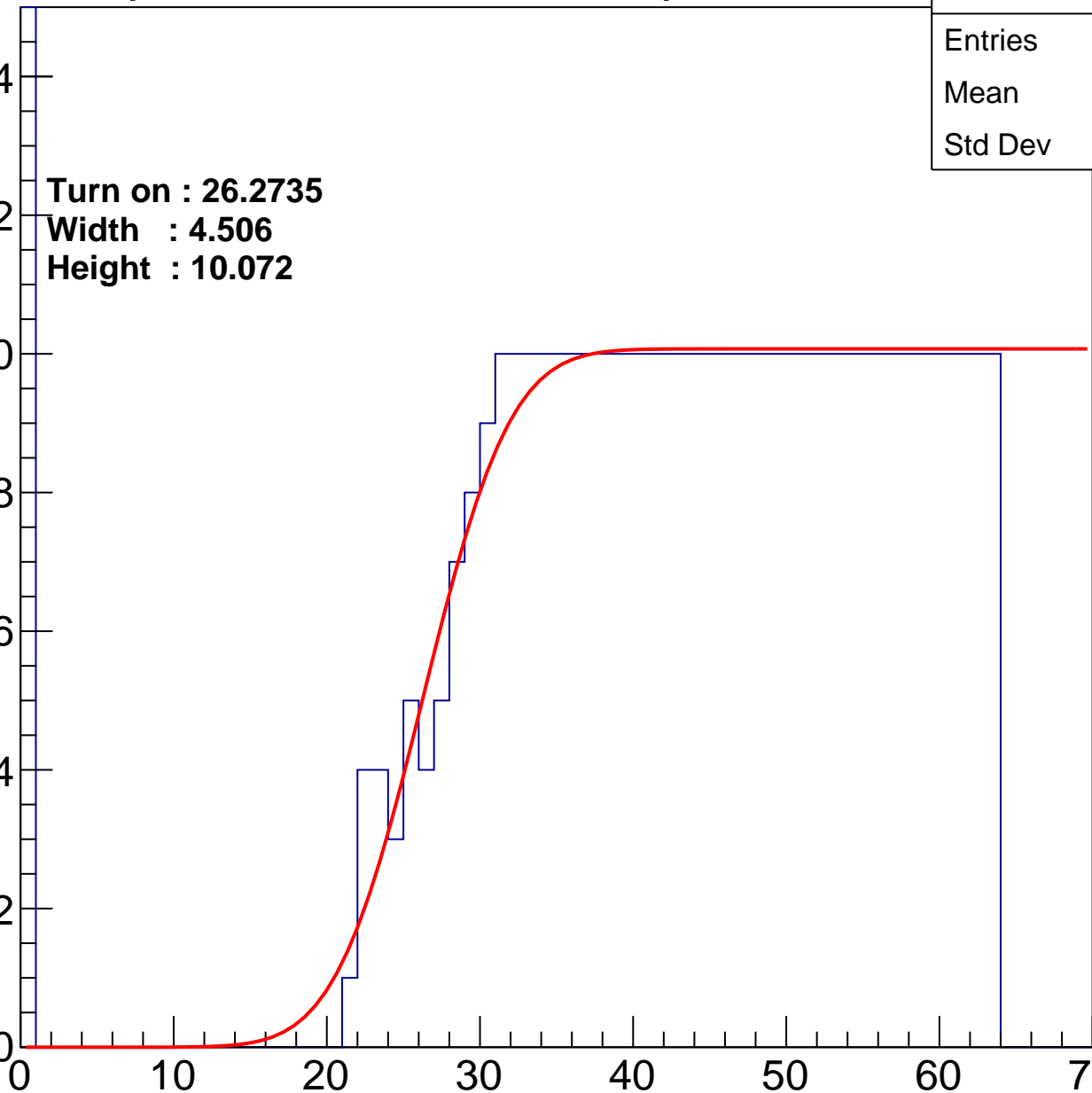
Width : 4.506

Height : 10.072

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U18-ch11

calib_packv5_041523_1651.root, FC#0, port C2

Entries	392
Mean	41.55
Std Dev	16.28

Turn on : 28.7388

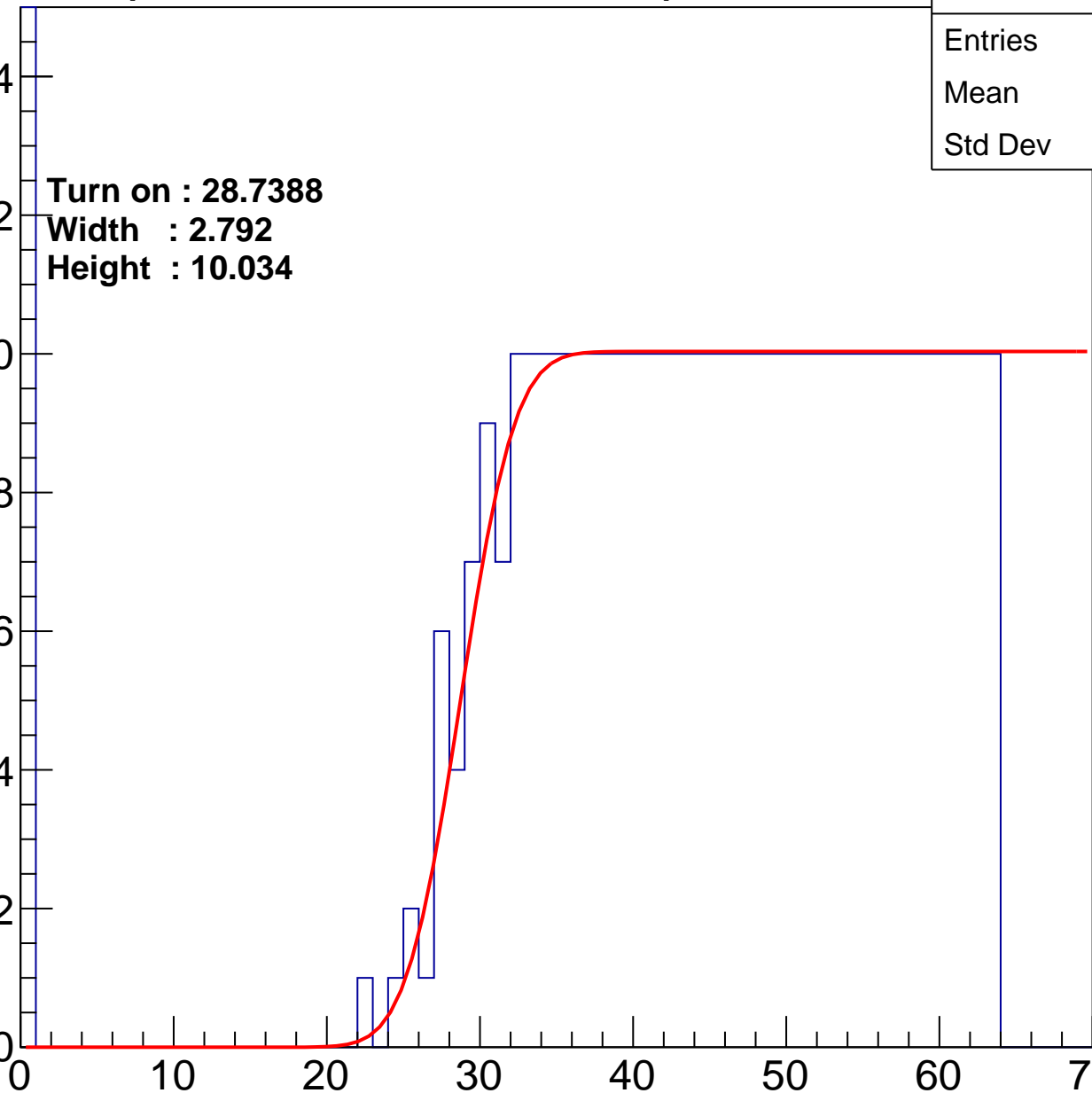
Width : 2.792

Height : 10.034

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U18-ch12

calib_packv5_041523_1651.root, FC#0, port C2

Entries	421
Mean	39.79
Std Dev	17.35

Turn on : 26.7312

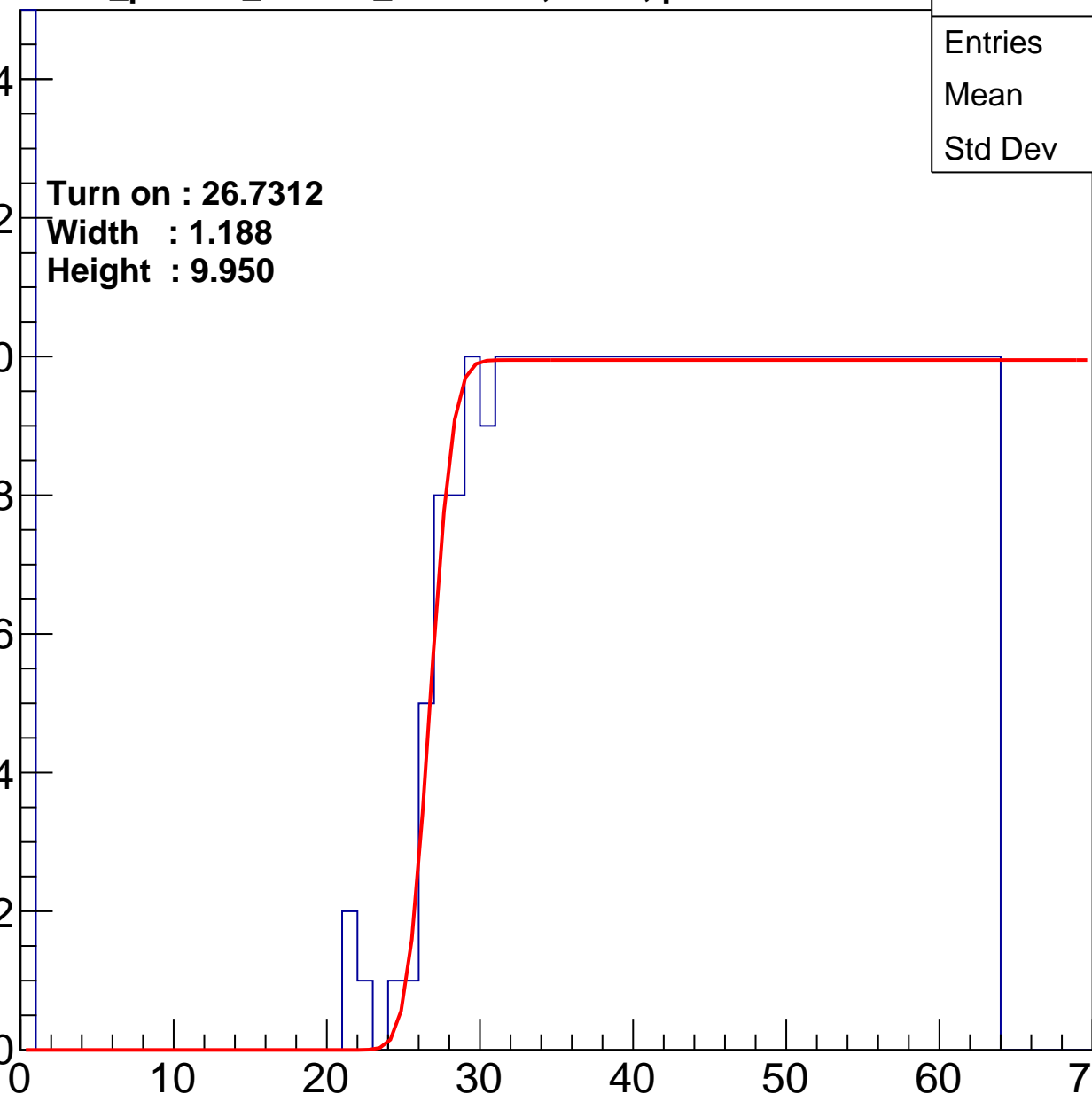
Width : 1.188

Height : 9.950

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U18-ch13

calib_packv5_041523_1651.root, FC#0, port C2

Entries	409
Mean	40.78
Std Dev	16.5

Turn on : 26.6627

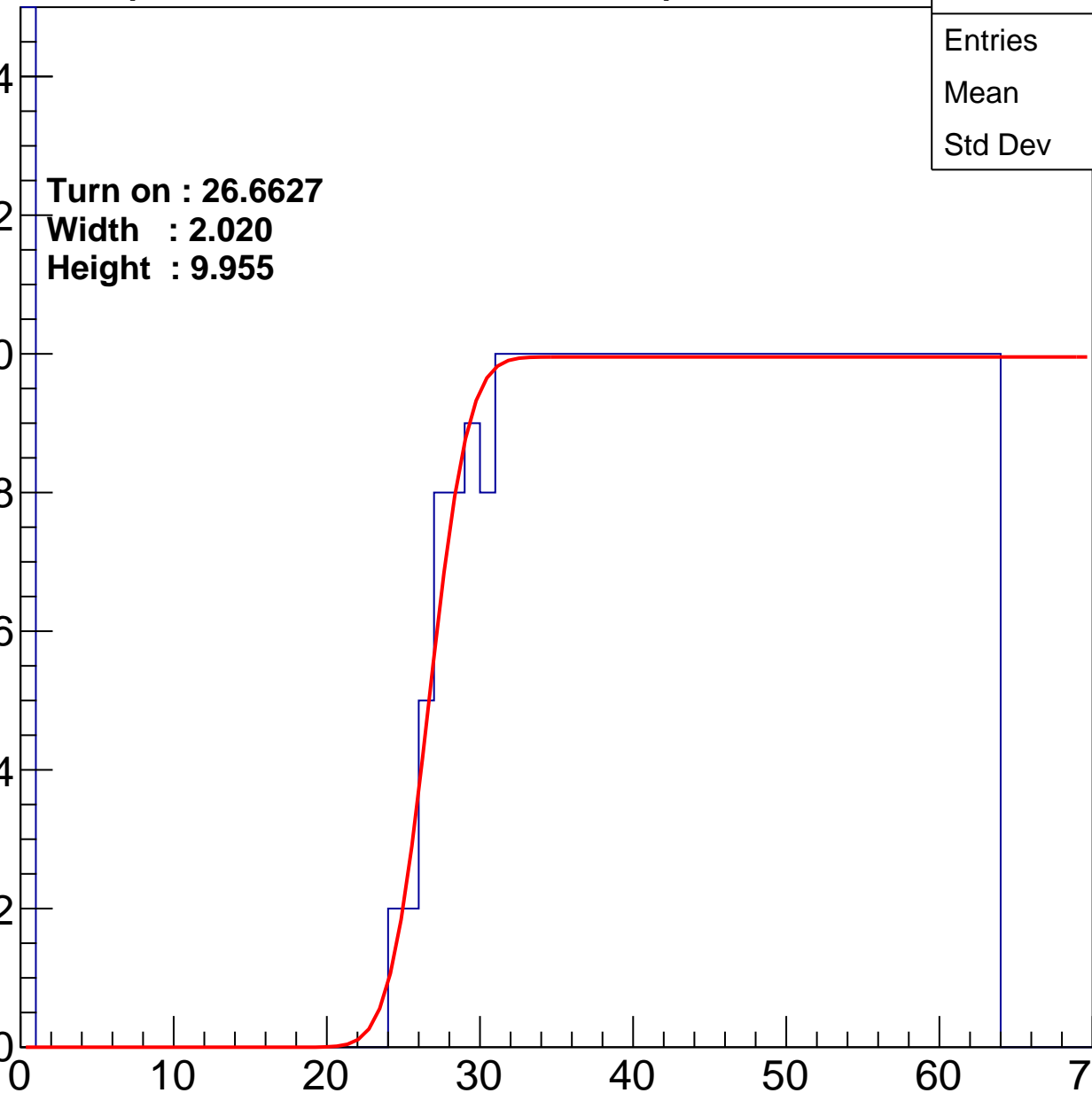
Width : 2.020

Height : 9.955

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U18-ch14

calib_packv5_041523_1651.root, FC#0, port C2

Entries	451
Mean	37.97
Std Dev	18.39

Turn on : 24.9829

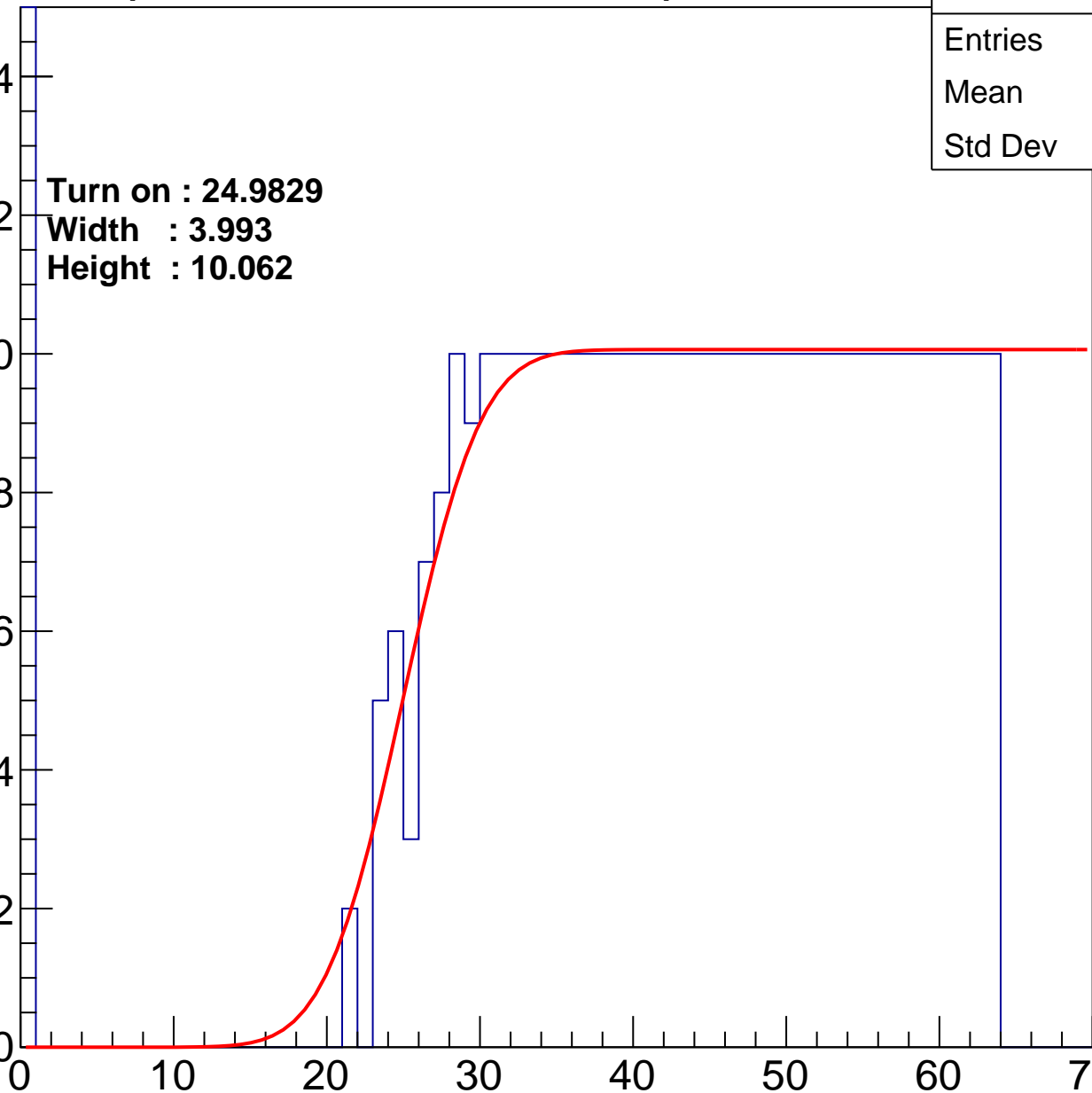
Width : 3.993

Height : 10.062

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U18-ch15

calib_packv5_041523_1651.root, FC#0, port C2

Entries	428
Mean	39.45
Std Dev	17.44

Turn on : 25.8807

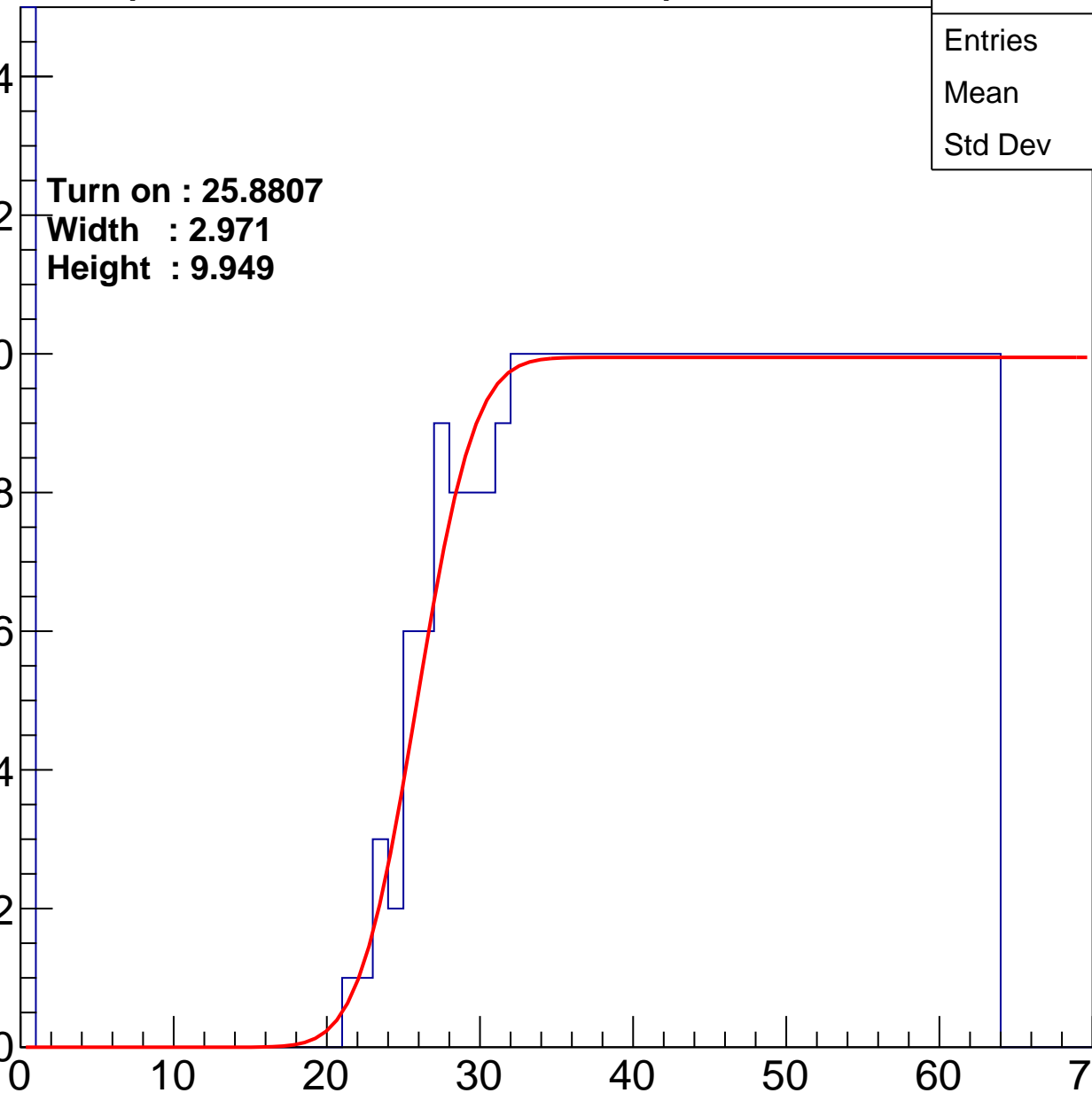
Width : 2.971

Height : 9.949

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U18-ch16

calib_packv5_041523_1651.root, FC#0, port C2

Entries	444
Mean	38.89
Std Dev	17.51

Turn on : 25.8980

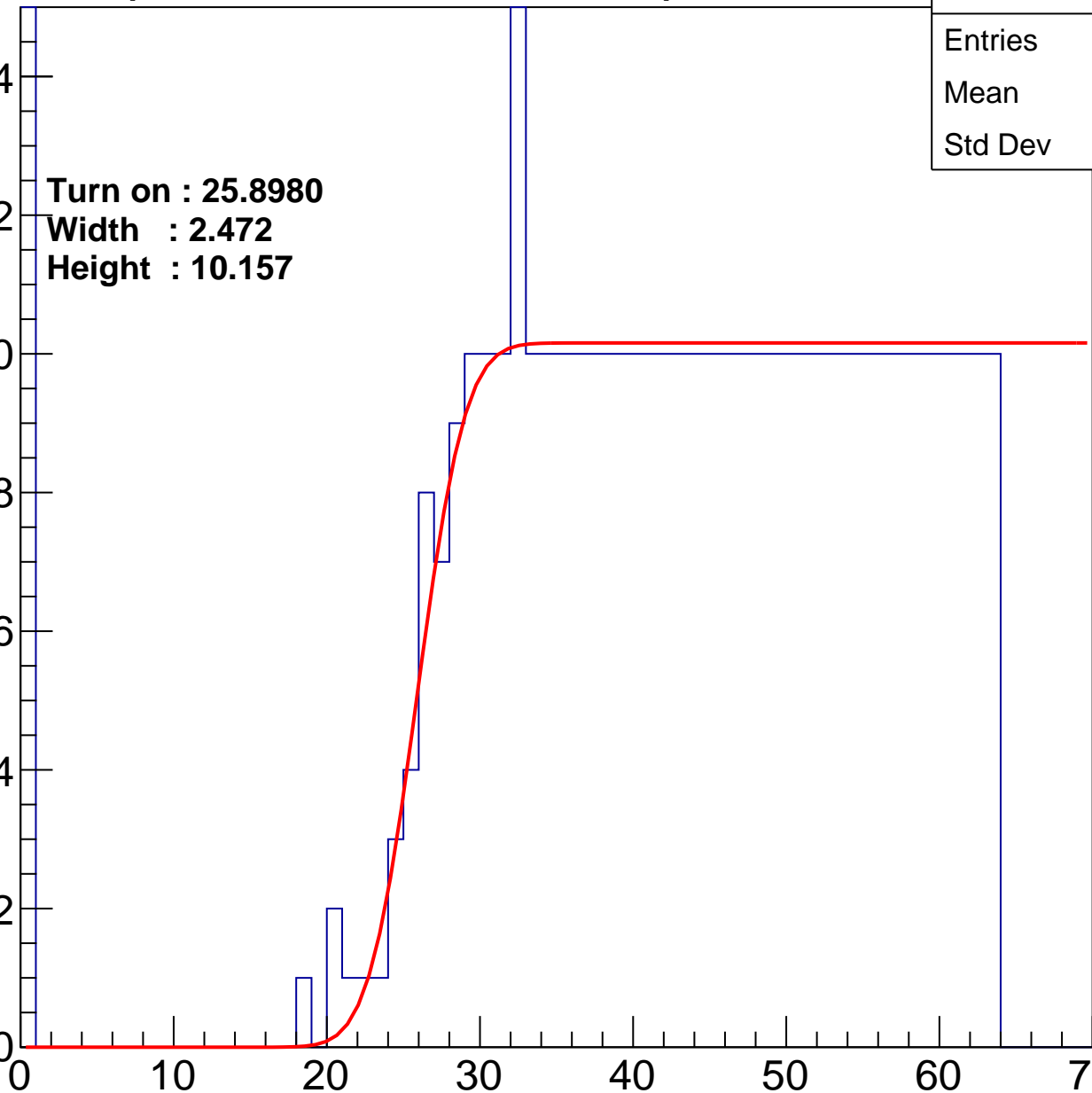
Width : 2.472

Height : 10.157

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U18-ch17

calib_packv5_041523_1651.root, FC#0, port C2

Entries	393
Mean	40.89
Std Dev	17.23

Turn on : 29.4739

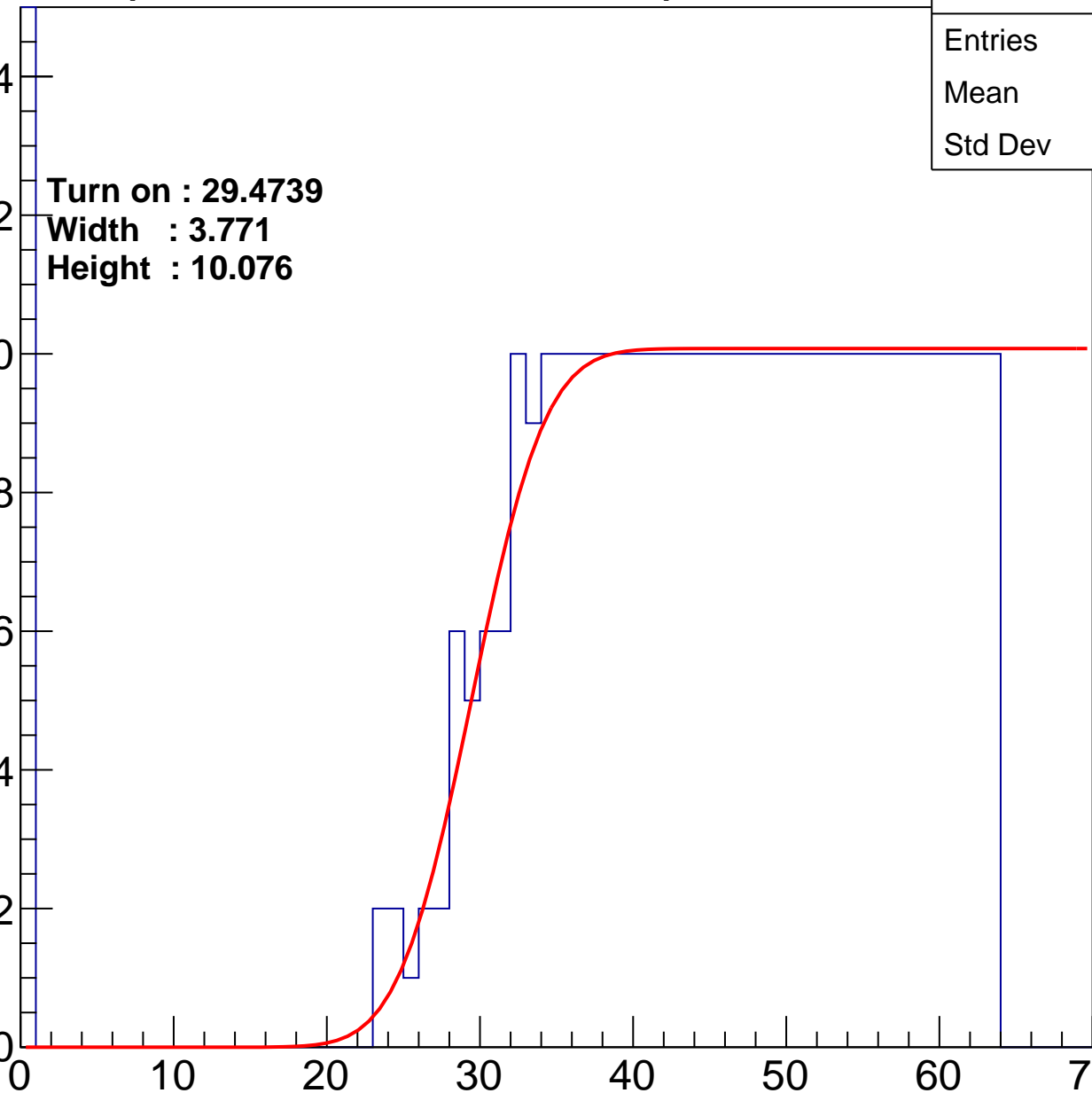
Width : 3.771

Height : 10.076

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U18-ch18

calib_packv5_041523_1651.root, FC#0, port C2

Entries	429
Mean	39.3
Std Dev	17.61

Turn on : 26.0576

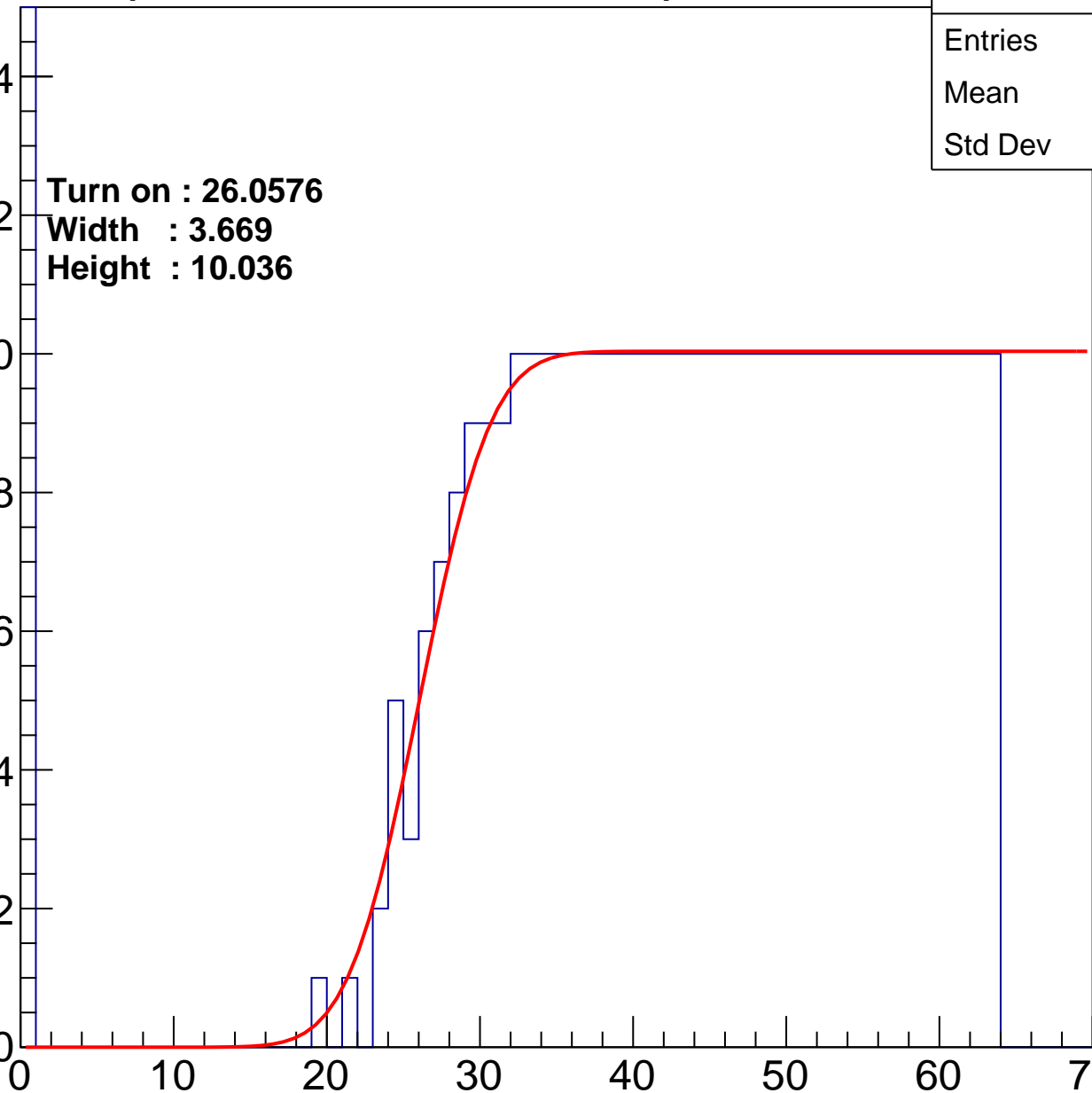
Width : 3.669

Height : 10.036

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U18-ch19

calib_packv5_041523_1651.root, FC#0, port C2

Entries	411
Mean	39.72
Std Dev	17.97

Turn on : 28.5156

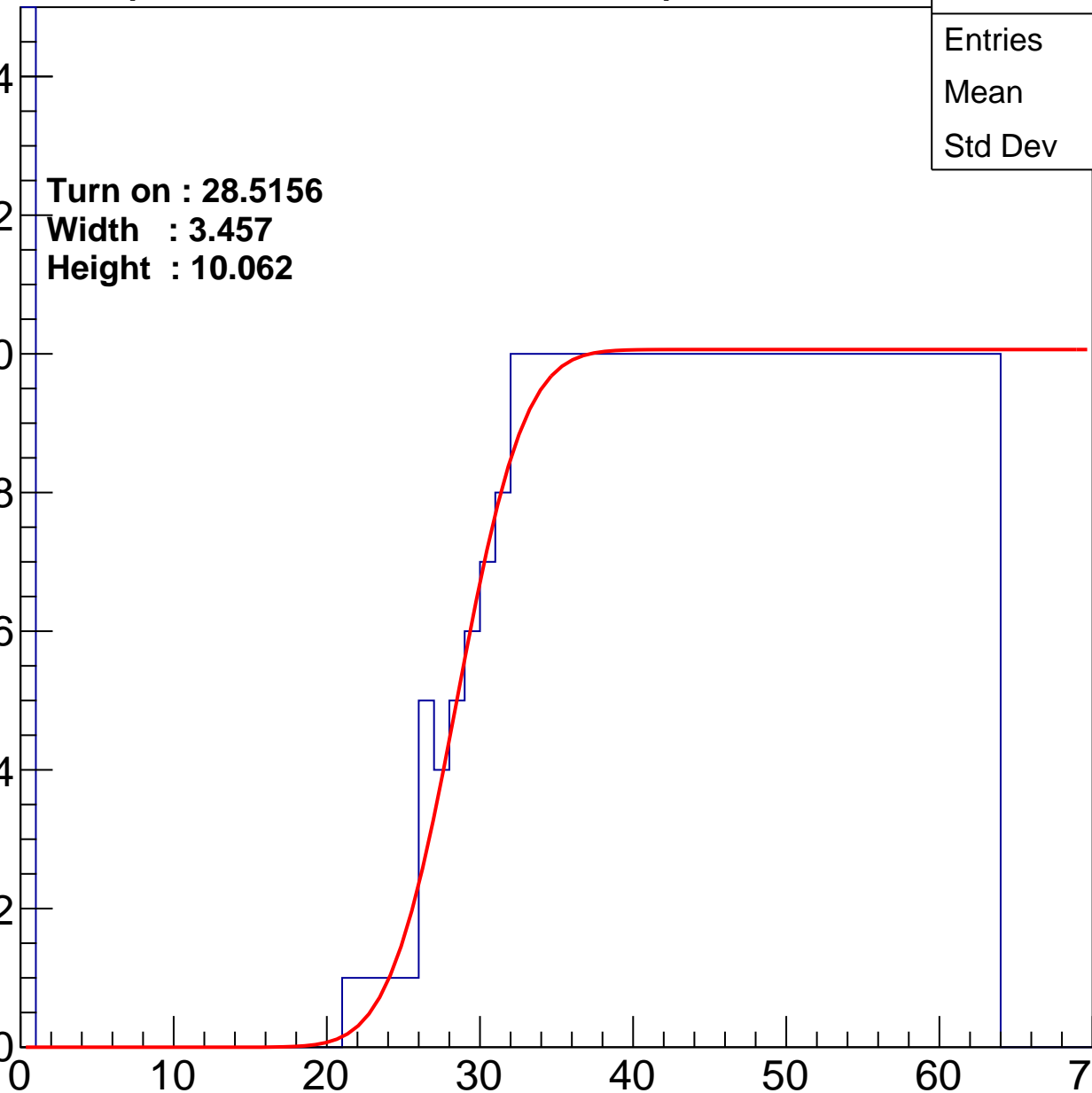
Width : 3.457

Height : 10.062

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U18-ch20

calib_packv5_041523_1651.root, FC#0, port C2

Entries	421
Mean	39.92
Std Dev	17.11

Turn on : 26.0938

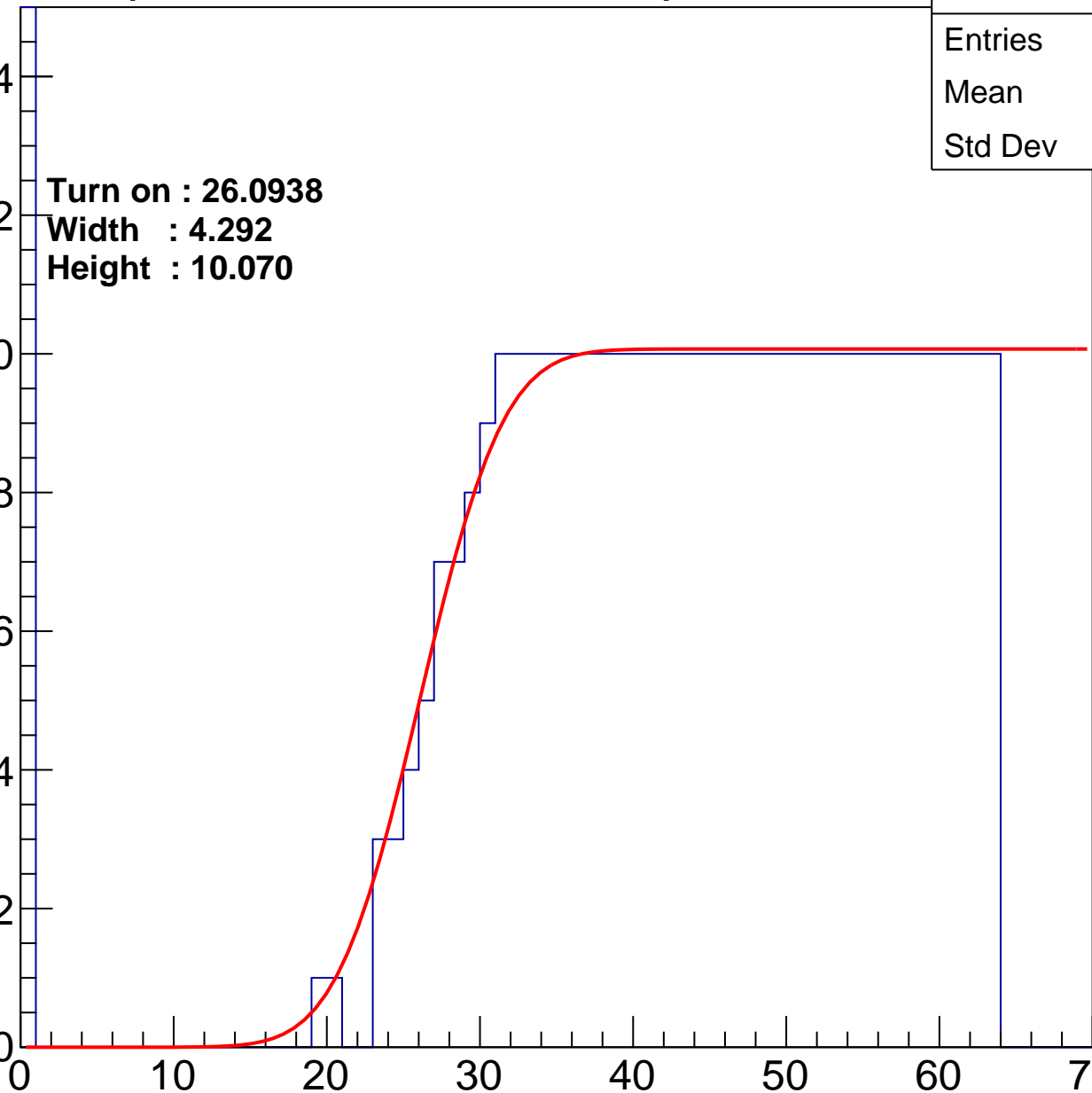
Width : 4.292

Height : 10.070

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U18-ch21

calib_packv5_041523_1651.root, FC#0, port C2

Entries	415
Mean	40.47
Std Dev	16.62

Turn on : 26.5680

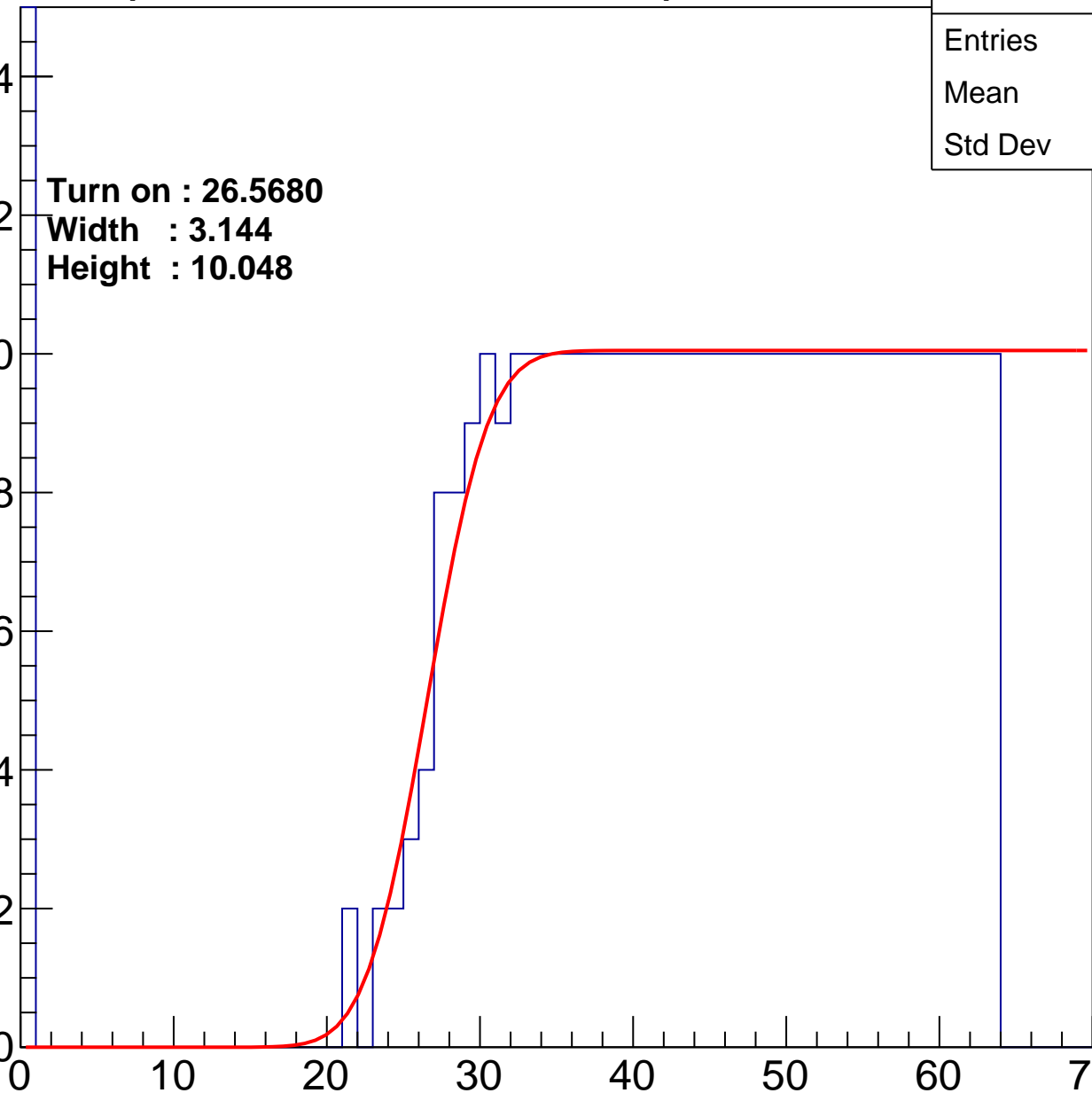
Width : 3.144

Height : 10.048

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U18-ch22

calib_packv5_041523_1651.root, FC#0, port C2

Entries	418
Mean	39.43
Std Dev	18.04

Turn on : 27.4614

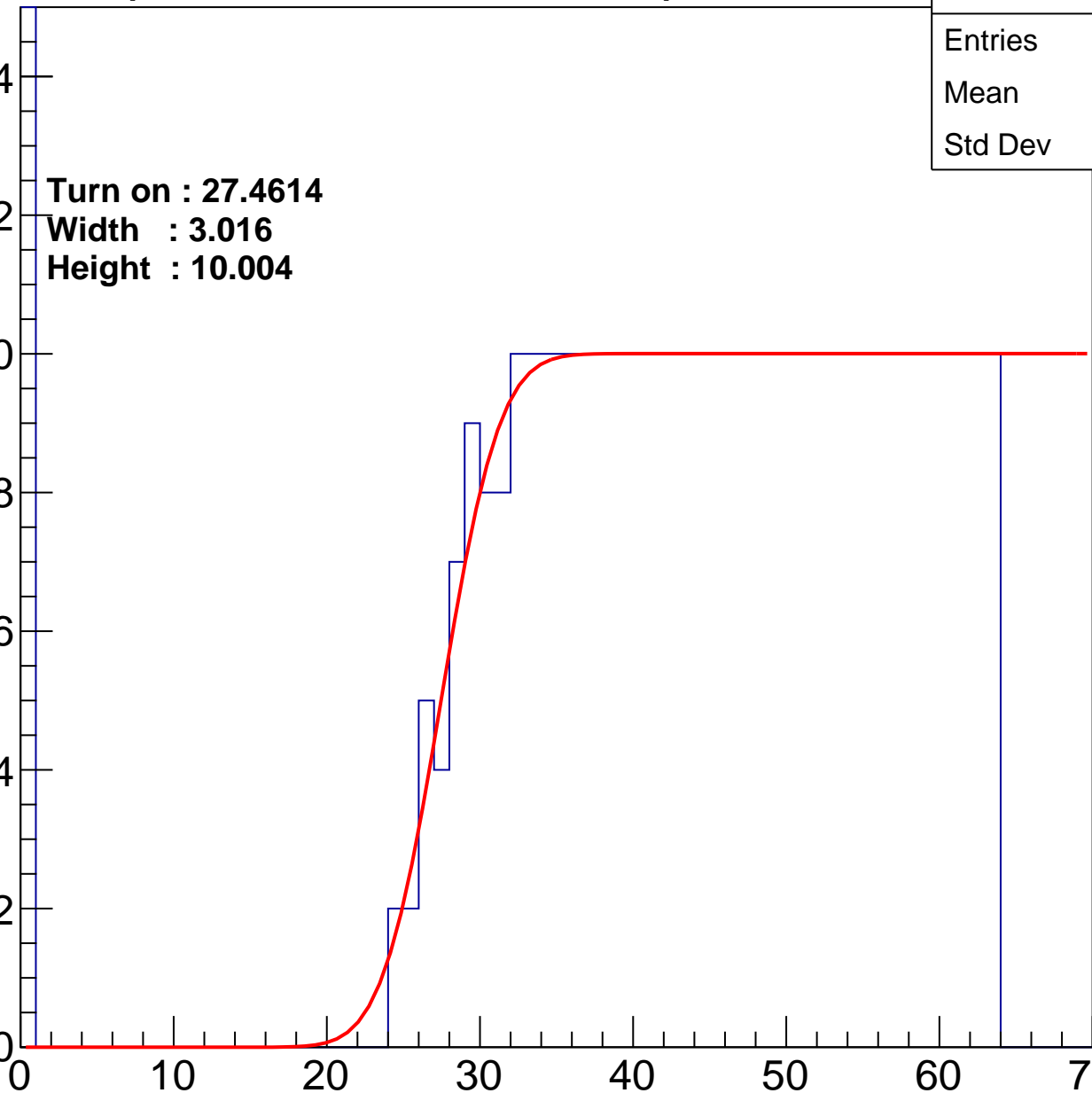
Width : 3.016

Height : 10.004

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U18-ch23

calib_packv5_041523_1651.root, FC#0, port C2

Entries	418
Mean	39.97
Std Dev	17.22

Turn on : 26.7623

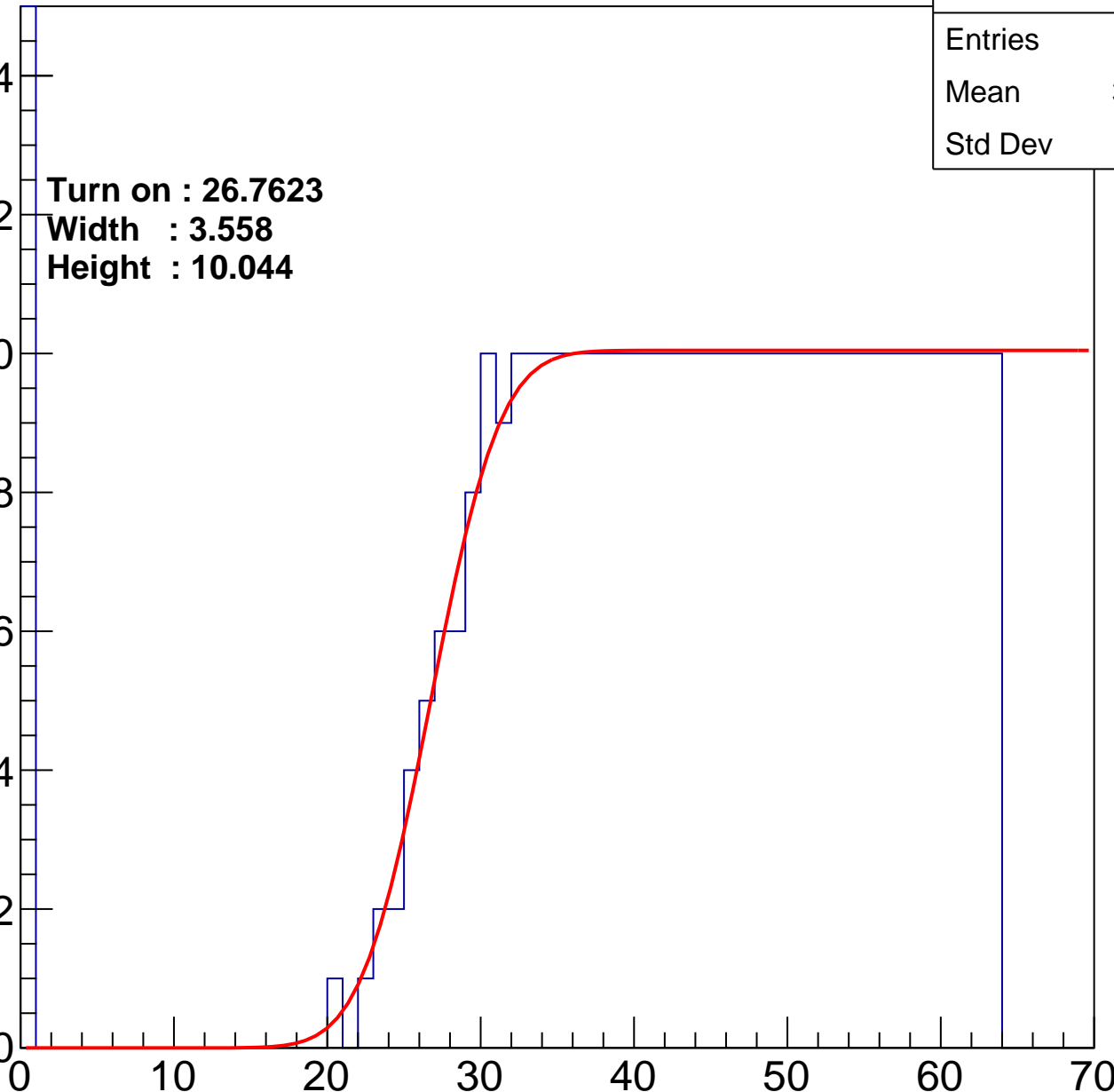
Width : 3.558

Height : 10.044

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U18-ch24

calib_packv5_041523_1651.root, FC#0, port C2

Entries	432
Mean	39.6
Std Dev	17.01

Turn on : 25.1086

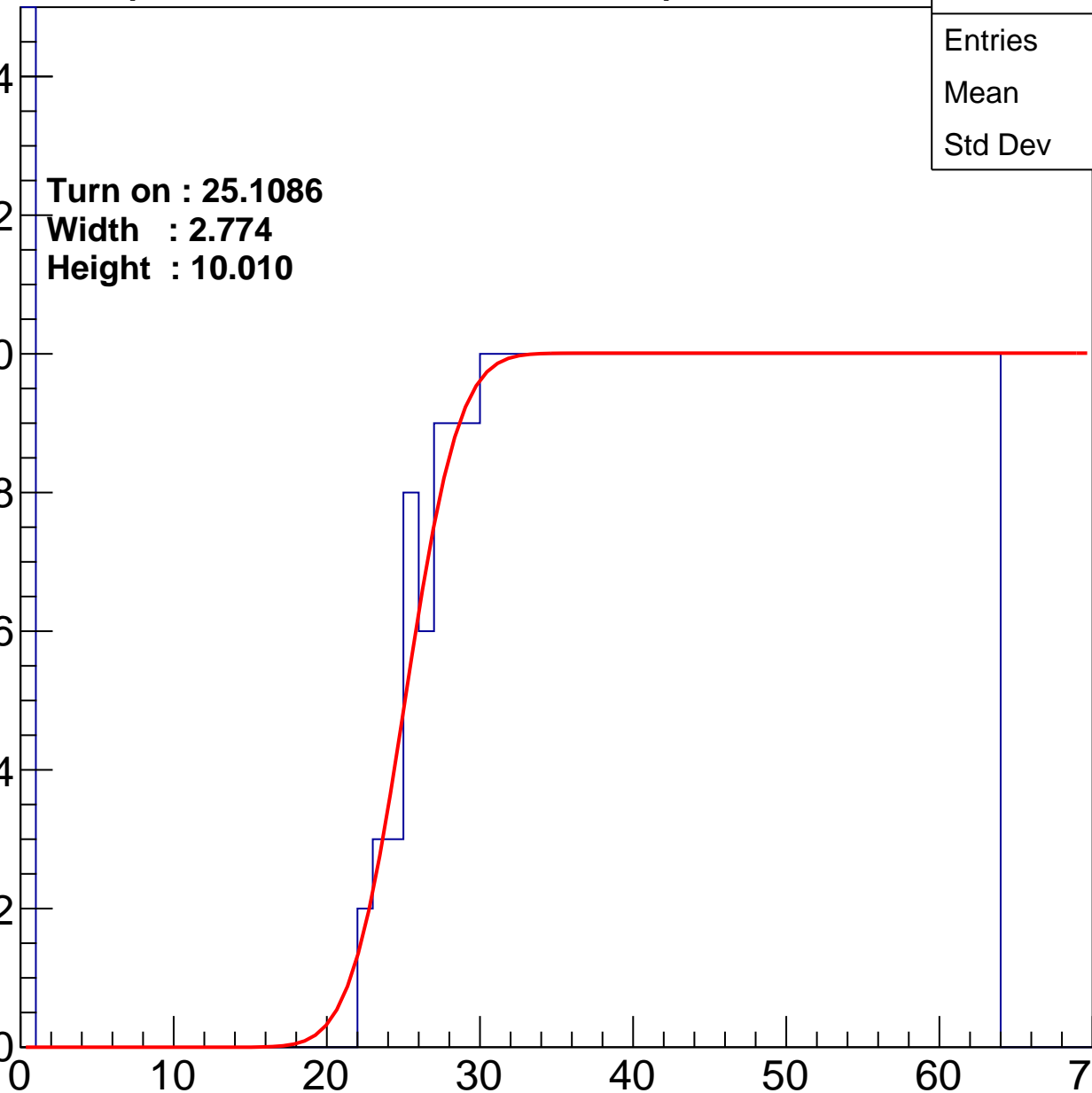
Width : 2.774

Height : 10.010

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U18-ch25

calib_packv5_041523_1651.root, FC#0, port C2

Entries	405
Mean	40.8
Std Dev	16.68

Turn on : 28.3492

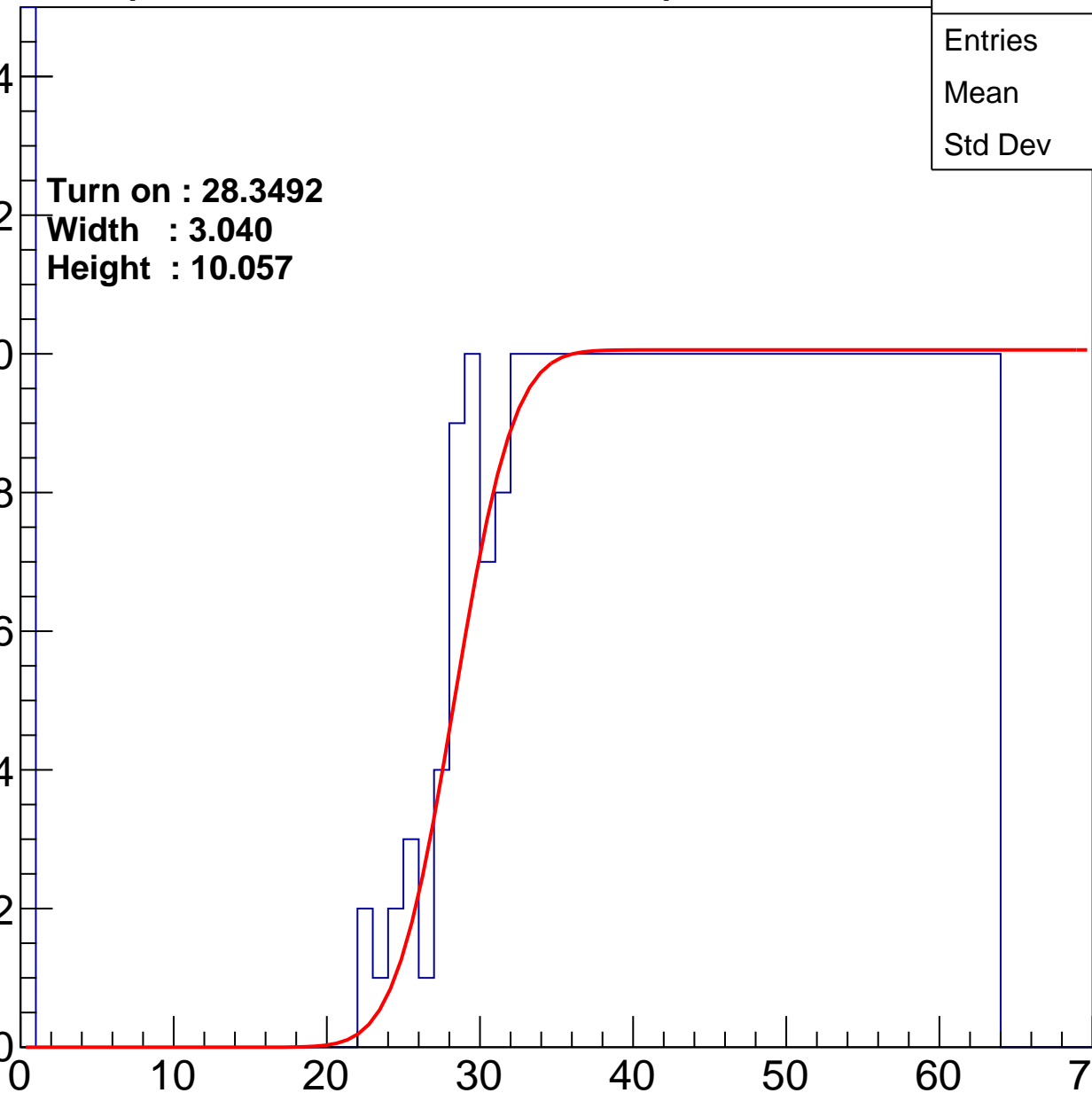
Width : 3.040

Height : 10.057

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U18-ch26

calib_packv5_041523_1651.root, FC#0, port C2

Entries	416
Mean	40.36
Std Dev	16.69

Turn on : 26.0611

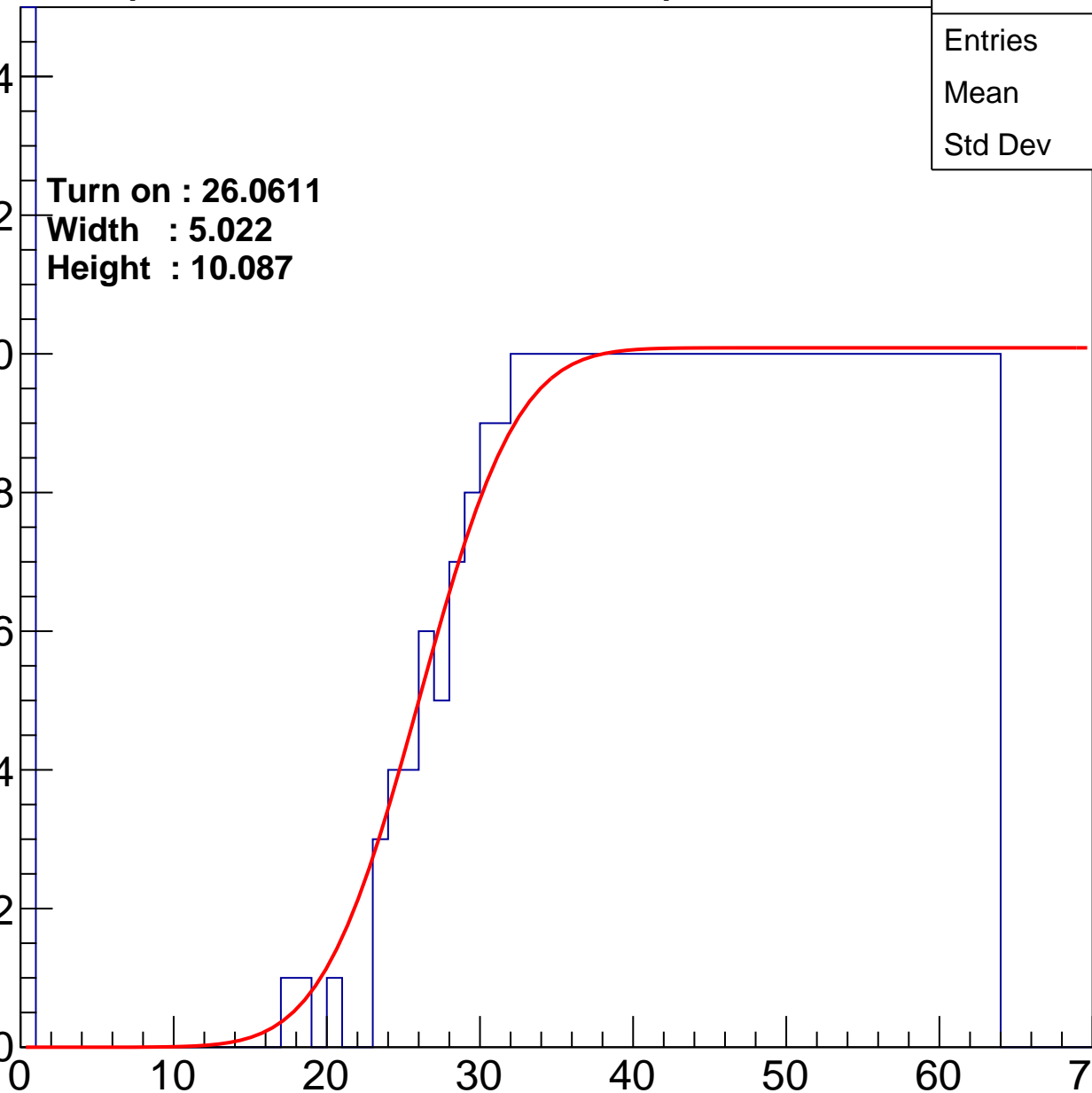
Width : 5.022

Height : 10.087

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U18-ch27

calib_packv5_041523_1651.root, FC#0, port C2

Entries	398
Mean	40.71
Std Dev	17.26

Turn on : 28.5984

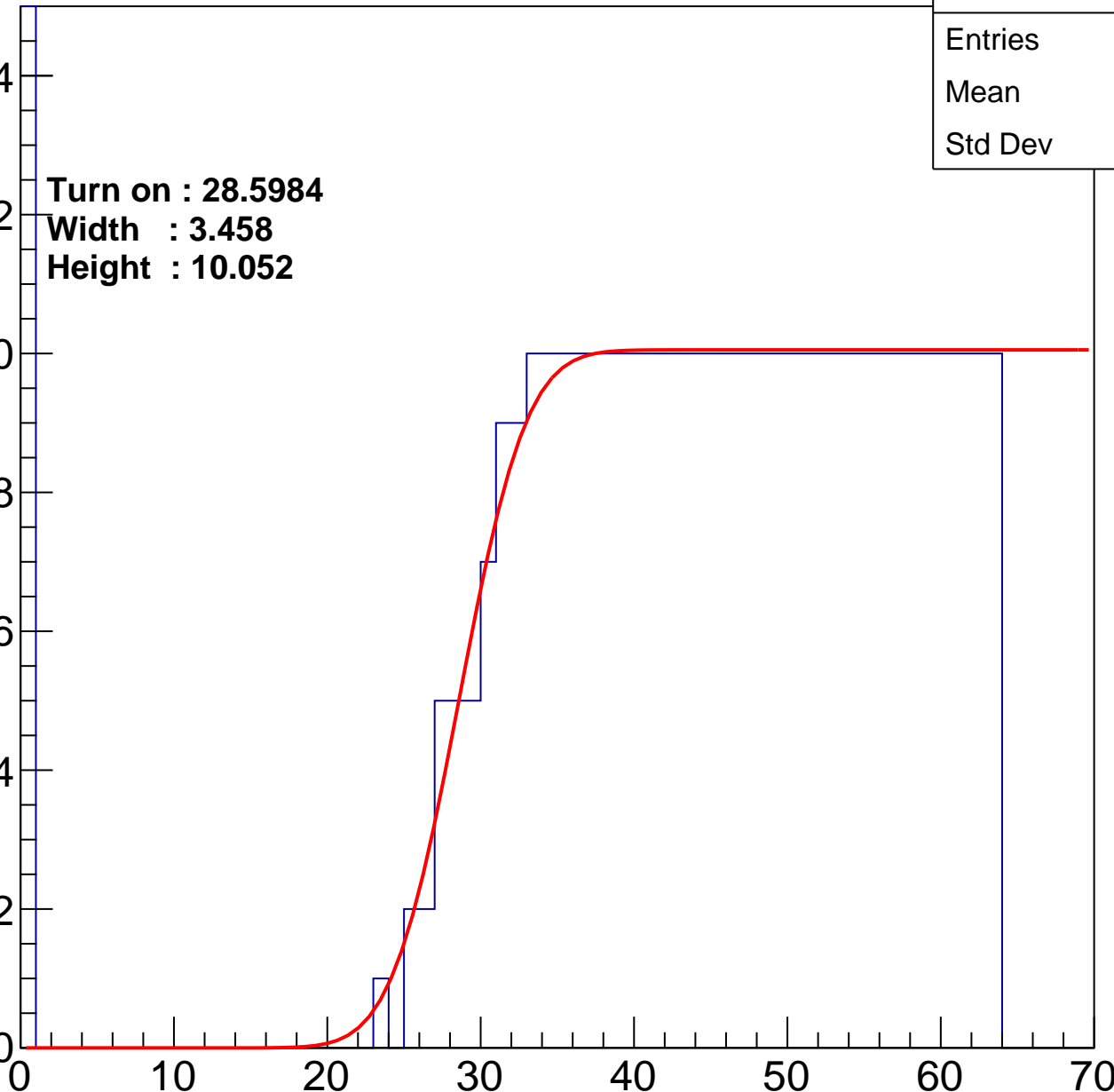
Width : 3.458

Height : 10.052

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U18-ch28

calib_packv5_041523_1651.root, FC#0, port C2

Entries	446
Mean	38.97
Std Dev	17.23

Turn on : 24.2608

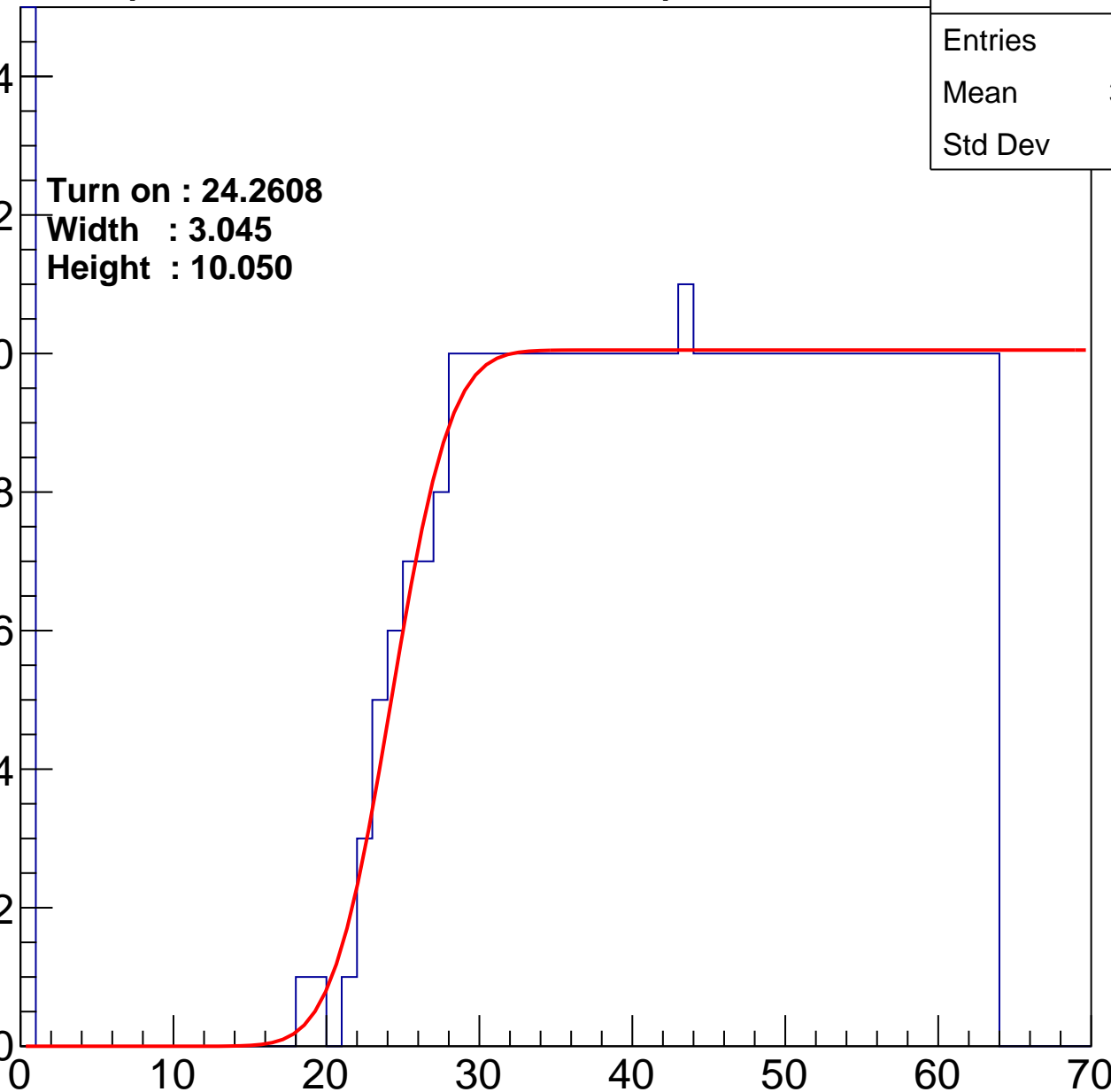
Width : 3.045

Height : 10.050

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U18-ch29

calib_packv5_041523_1651.root, FC#0, port C2

Entries	423
Mean	40.38
Std Dev	16.28

Turn on : 25.8094

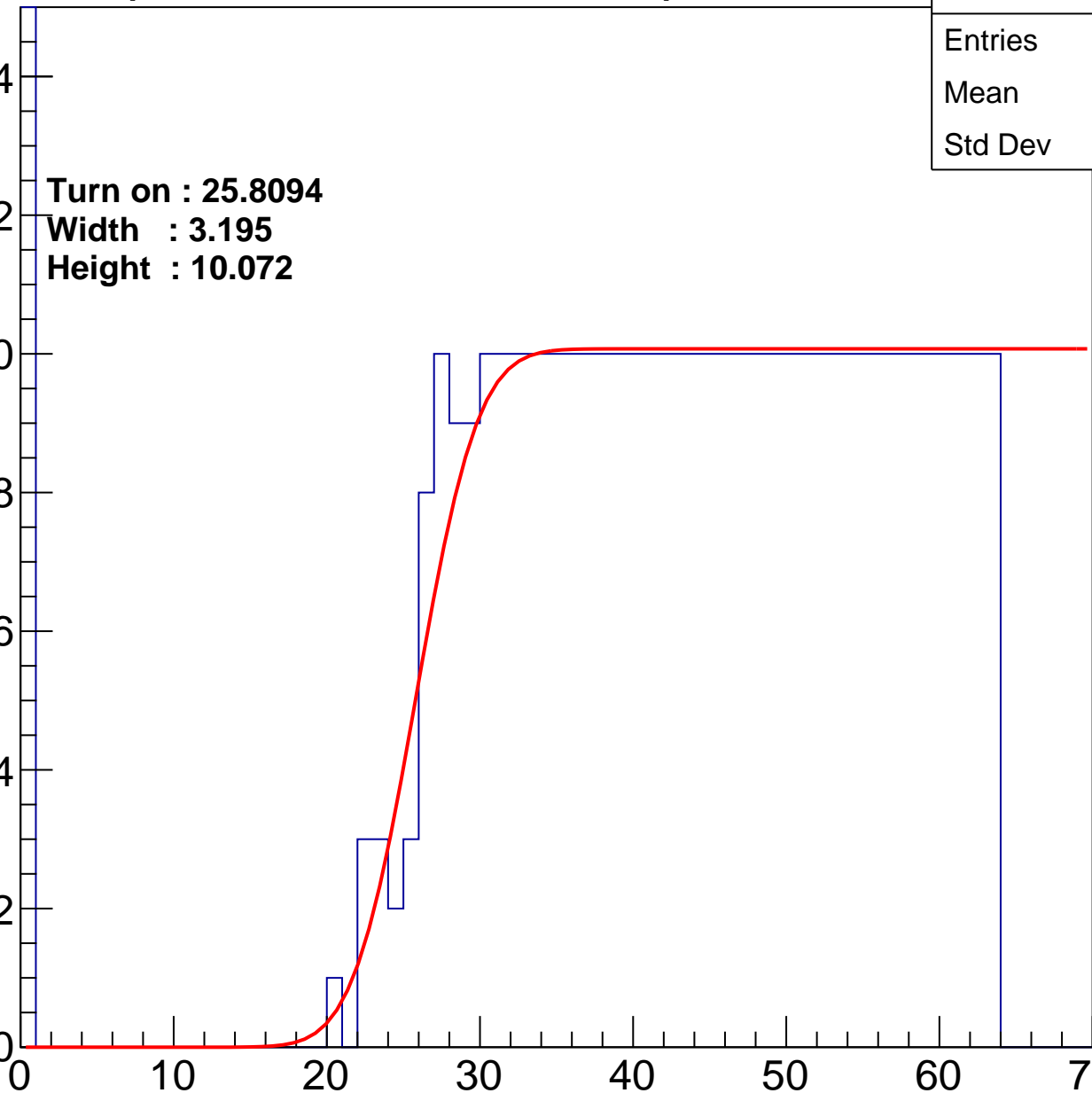
Width : 3.195

Height : 10.072

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U18-ch30

calib_packv5_041523_1651.root, FC#0, port C2

Entries	462
Mean	37.34
Std Dev	18.68

Turn on : 24.6990

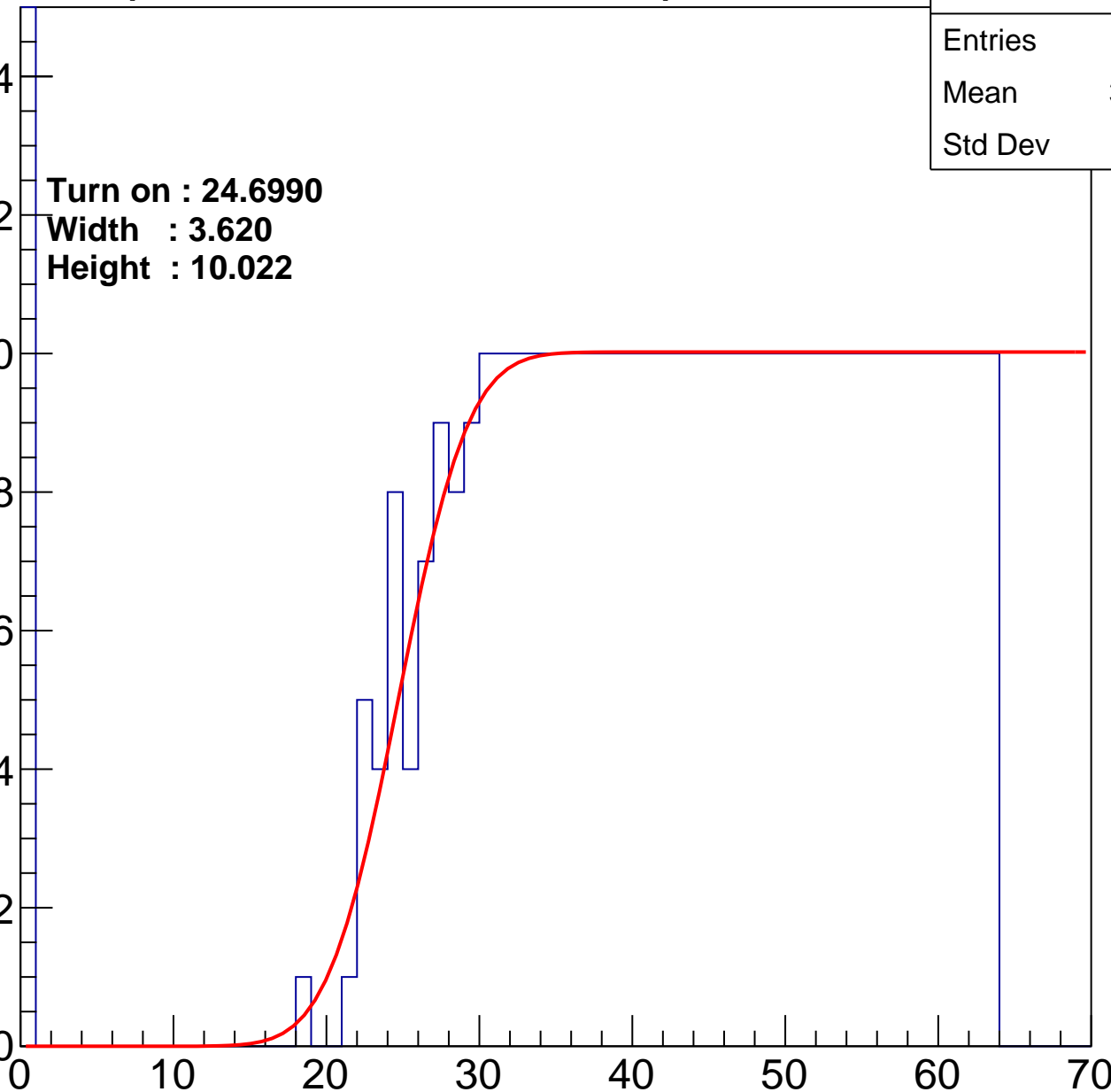
Width : 3.620

Height : 10.022

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U18-ch31

calib_packv5_041523_1651.root, FC#0, port C2

Entries	443
Mean	38.43
Std Dev	18.15

Turn on : 25.7758

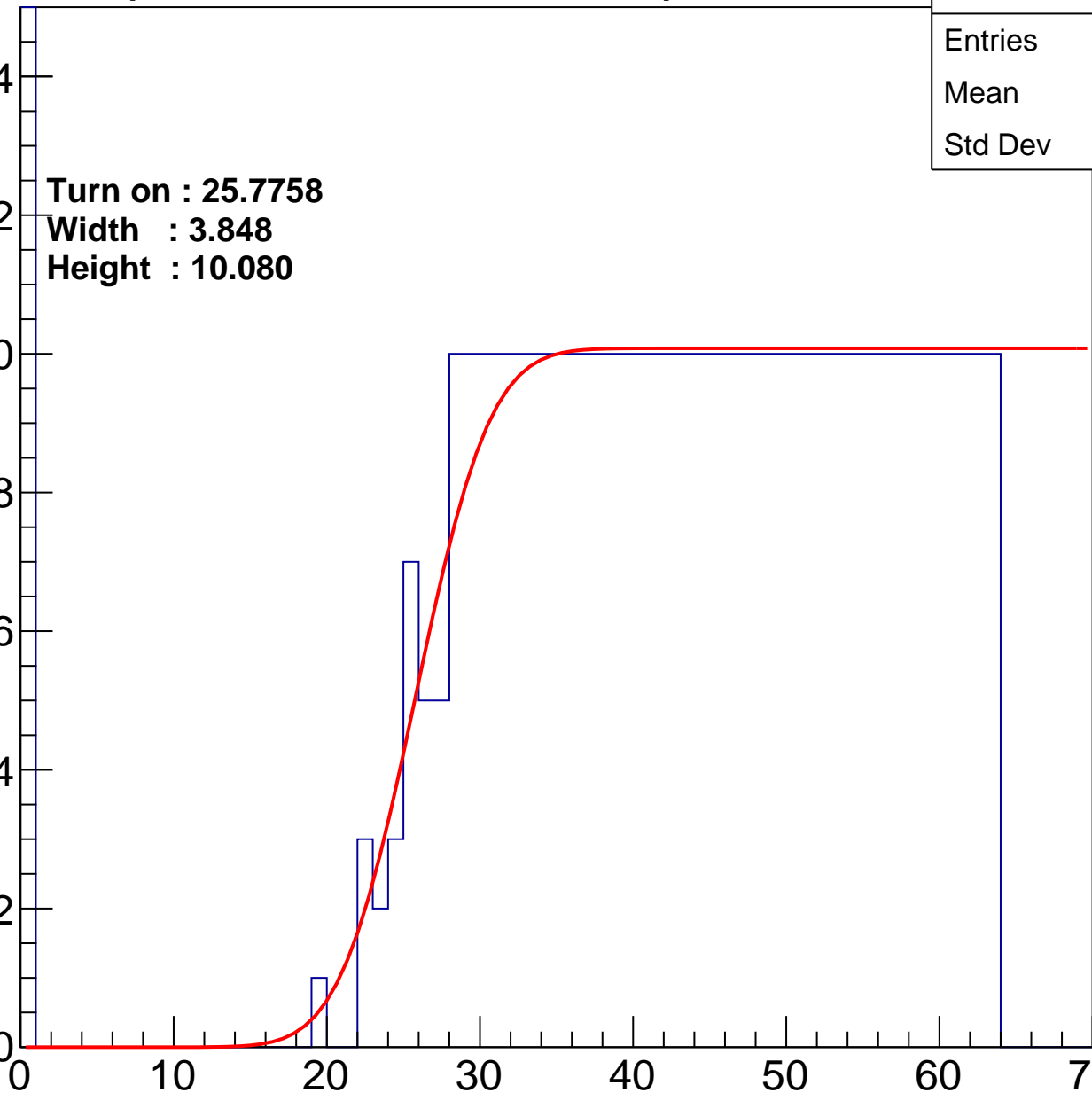
Width : 3.848

Height : 10.080

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U18-ch32

calib_packv5_041523_1651.root, FC#0, port C2

Entries	453
Mean	38.51
Std Dev	17.51

Turn on : 24.1040

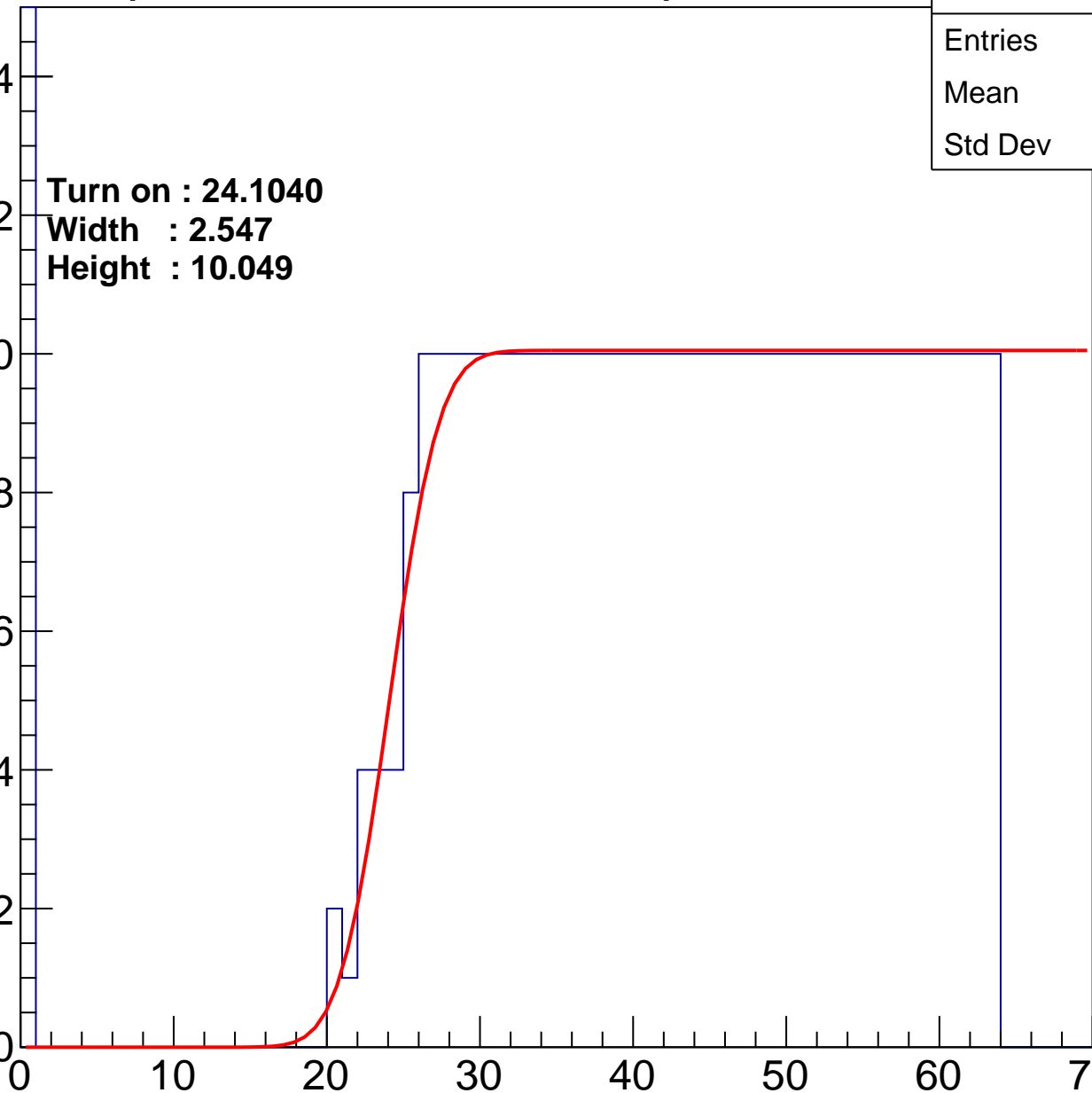
Width : 2.547

Height : 10.049

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U18-ch33

calib_packv5_041523_1651.root, FC#0, port C2

Entries	435
Mean	38.51
Std Dev	18.46

Turn on : 26.8114

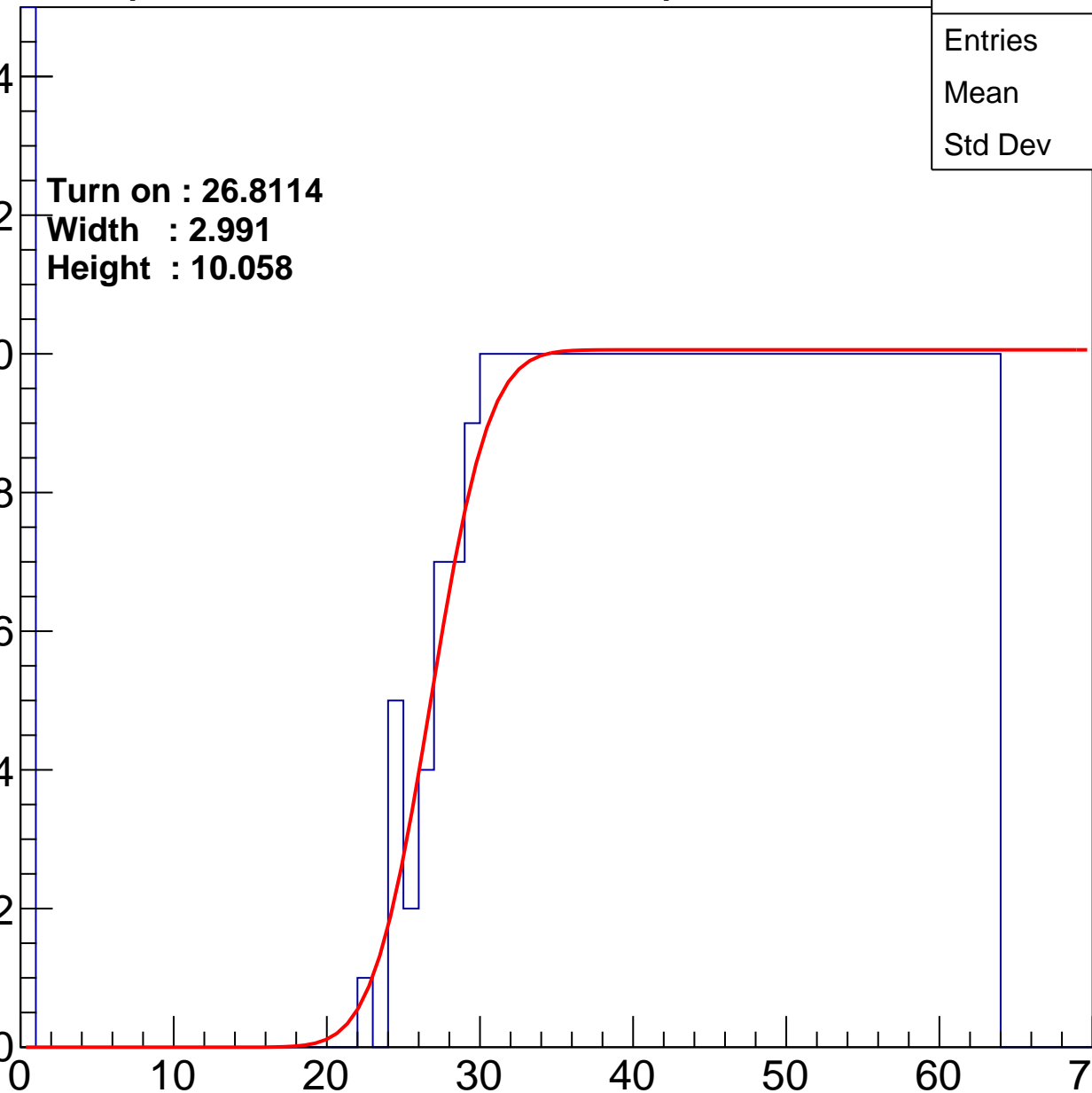
Width : 2.991

Height : 10.058

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U18-ch34

calib_packv5_041523_1651.root, FC#0, port C2

Entries	434
Mean	38.98
Std Dev	17.79

Turn on : 26.1158

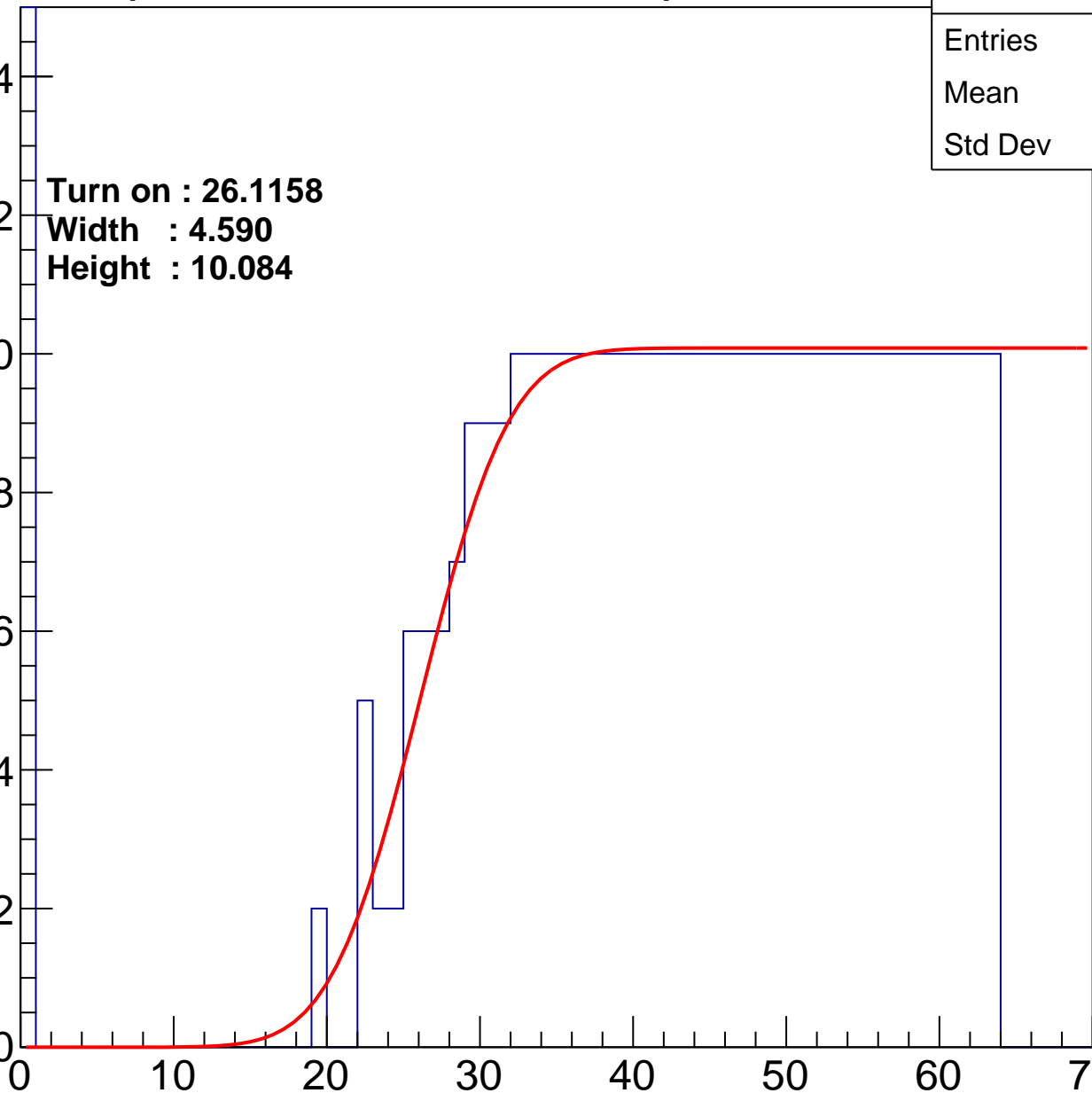
Width : 4.590

Height : 10.084

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U18-ch35

calib_packv5_041523_1651.root, FC#0, port C2

Entries	407
Mean	40.02
Std Dev	17.78

Turn on : 28.4894

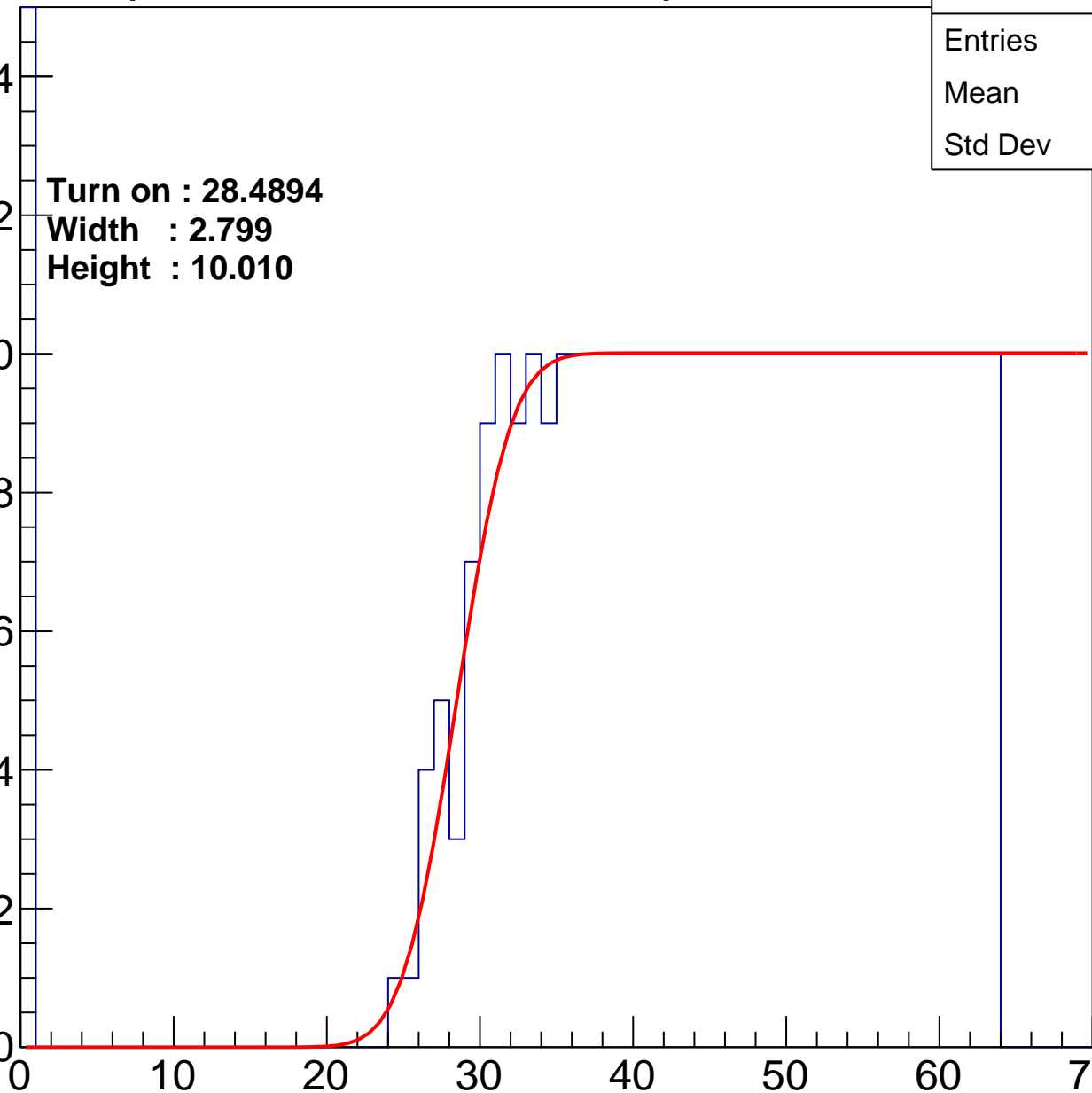
Width : 2.799

Height : 10.010

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U18-ch36

calib_packv5_041523_1651.root, FC#0, port C2

Entries	434
Mean	38.77
Std Dev	18.09

Turn on : 25.8782

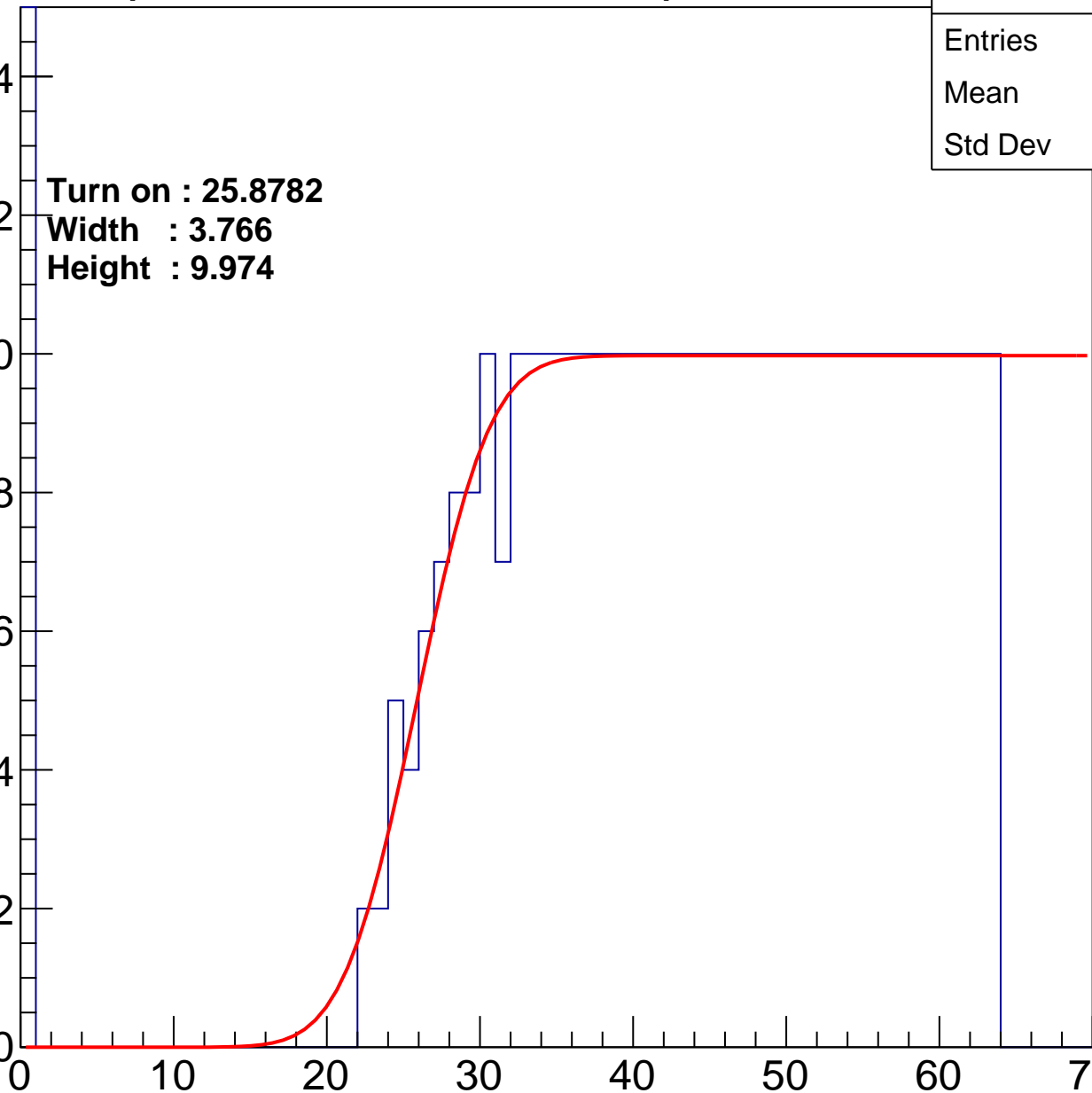
Width : 3.766

Height : 9.974

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U18-ch37

calib_packv5_041523_1651.root, FC#0, port C2

Entries	405
Mean	40.66
Std Dev	16.9

Turn on : 27.5291

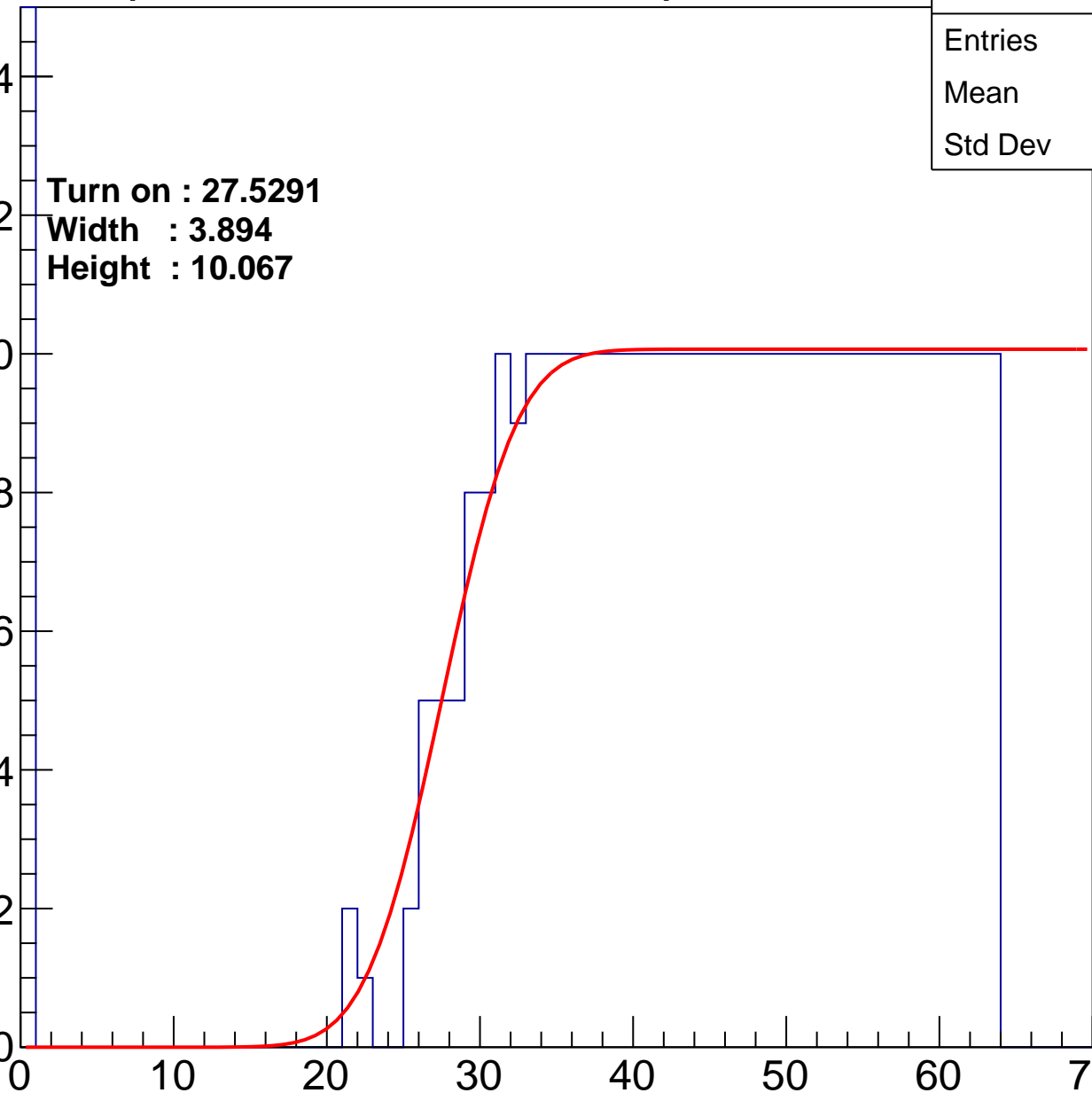
Width : 3.894

Height : 10.067

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U18-ch38

calib_packv5_041523_1651.root, FC#0, port C2

Entries	457
Mean	38.26
Std Dev	17.66

Turn on : 23.6104

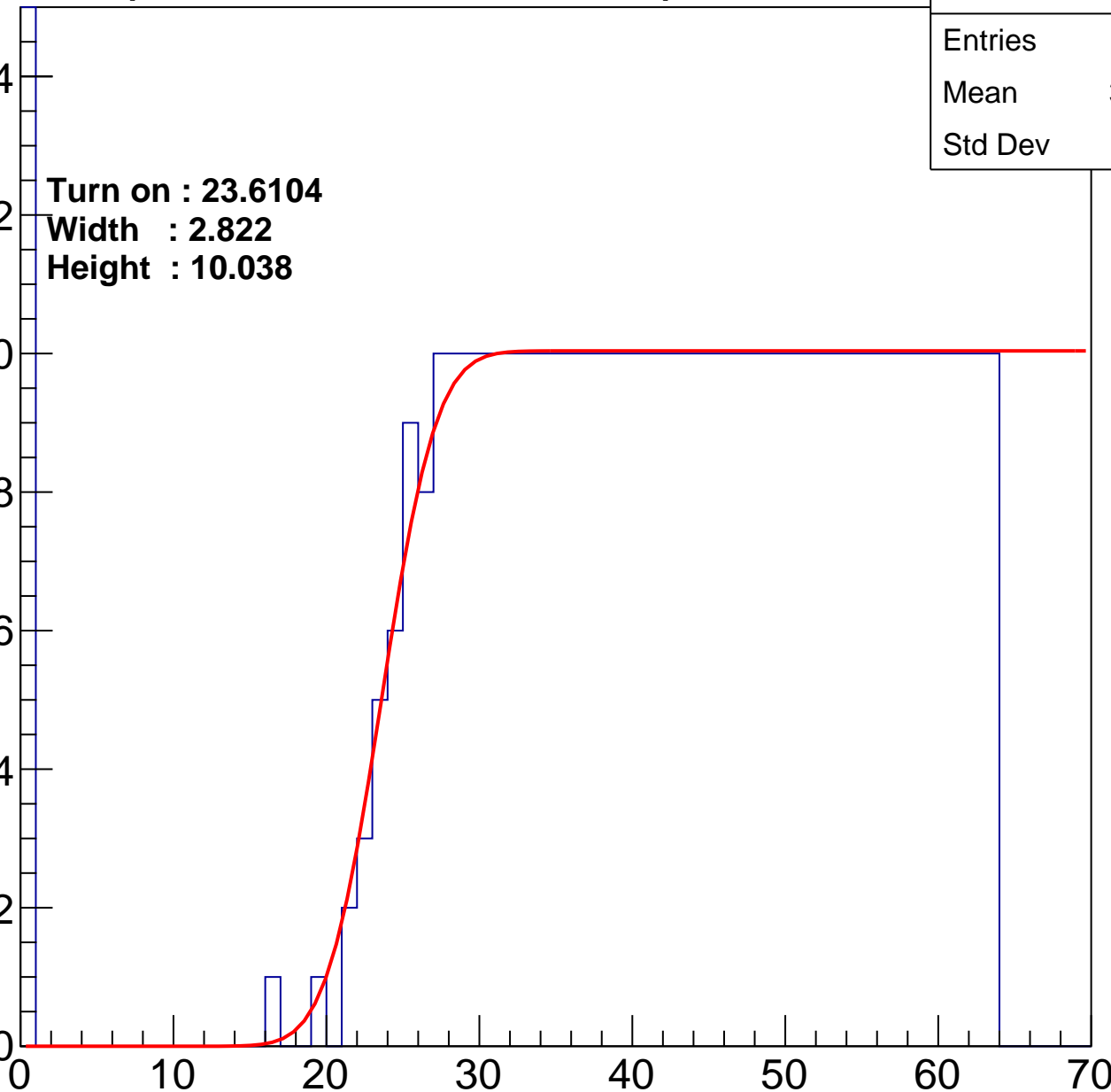
Width : 2.822

Height : 10.038

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U18-ch39

calib_packv5_041523_1651.root, FC#0, port C2

Entries	429
Mean	38.9
Std Dev	18.21

Turn on : 26.9275

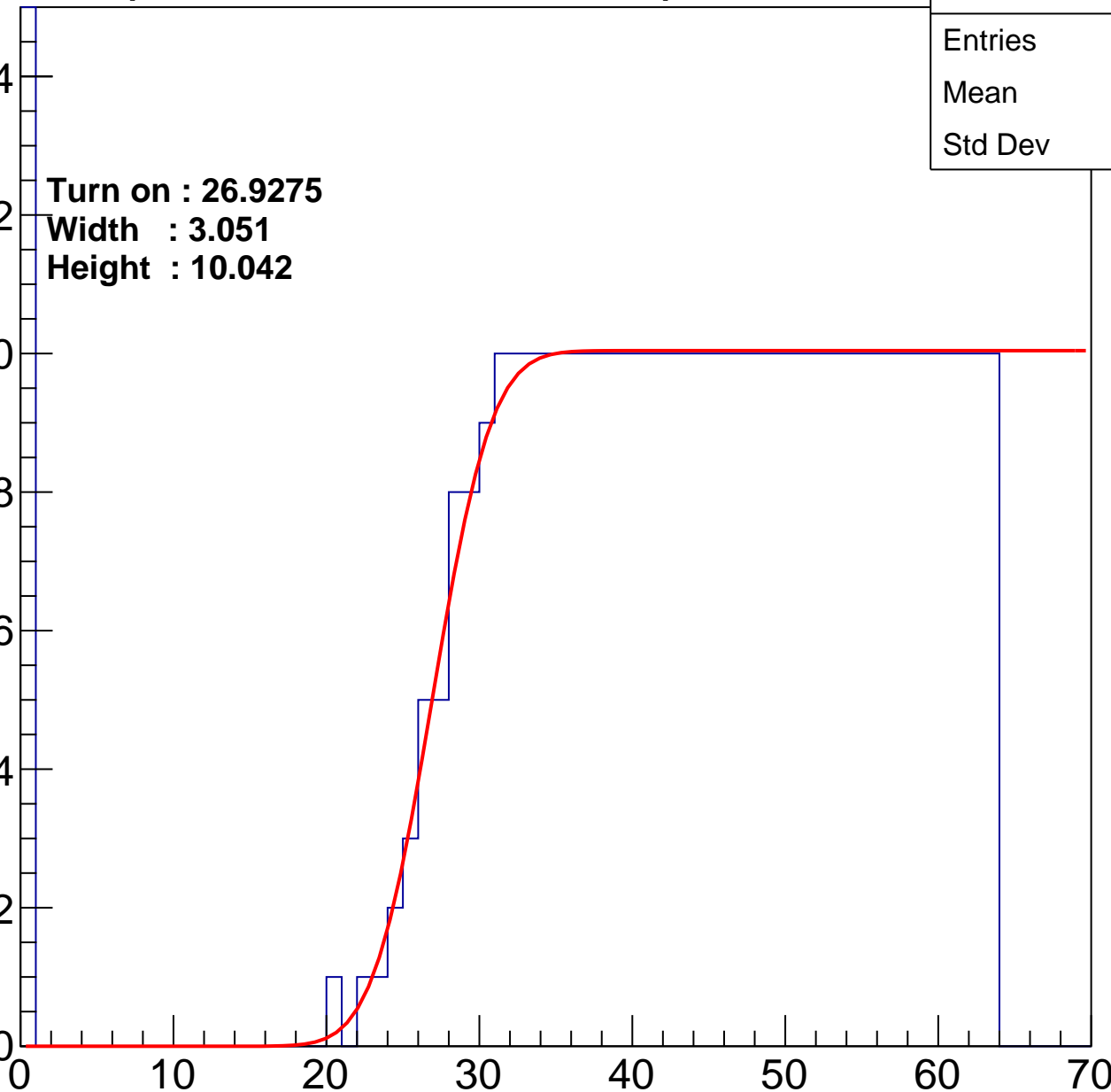
Width : 3.051

Height : 10.042

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U18-ch40

calib_packv5_041523_1651.root, FC#0, port C2

Entries	422
Mean	40.32
Std Dev	16.61

Turn on : 26.0190

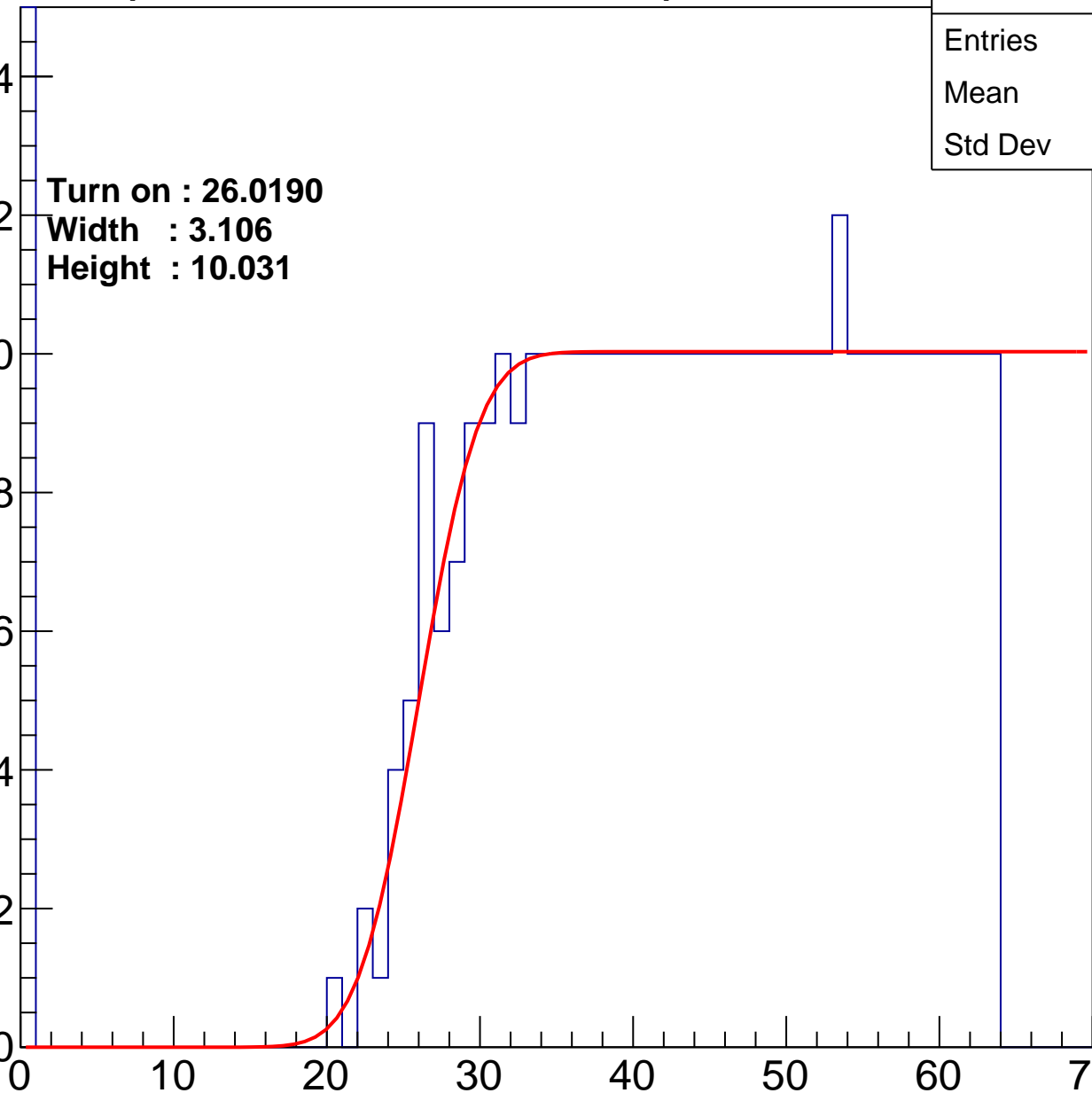
Width : 3.106

Height : 10.031

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U18-ch41

calib_packv5_041523_1651.root, FC#0, port C2

Entries	412
Mean	40.28
Std Dev	17.07

Turn on : 27.1604

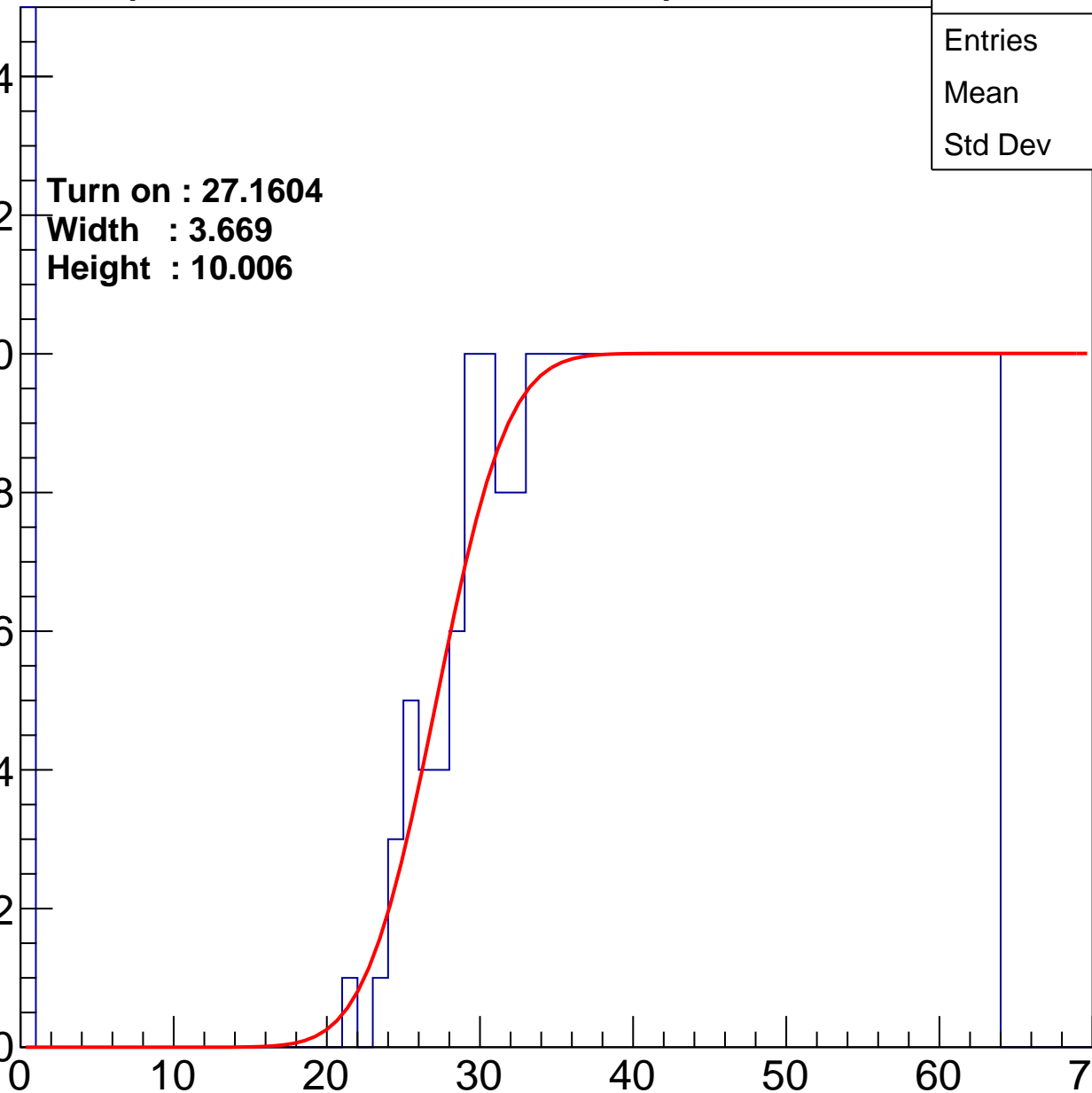
Width : 3.669

Height : 10.006

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U18-ch42

calib_packv5_041523_1651.root, FC#0, port C2

Entries	446
Mean	37.82
Std Dev	18.83

Turn on : 26.5488

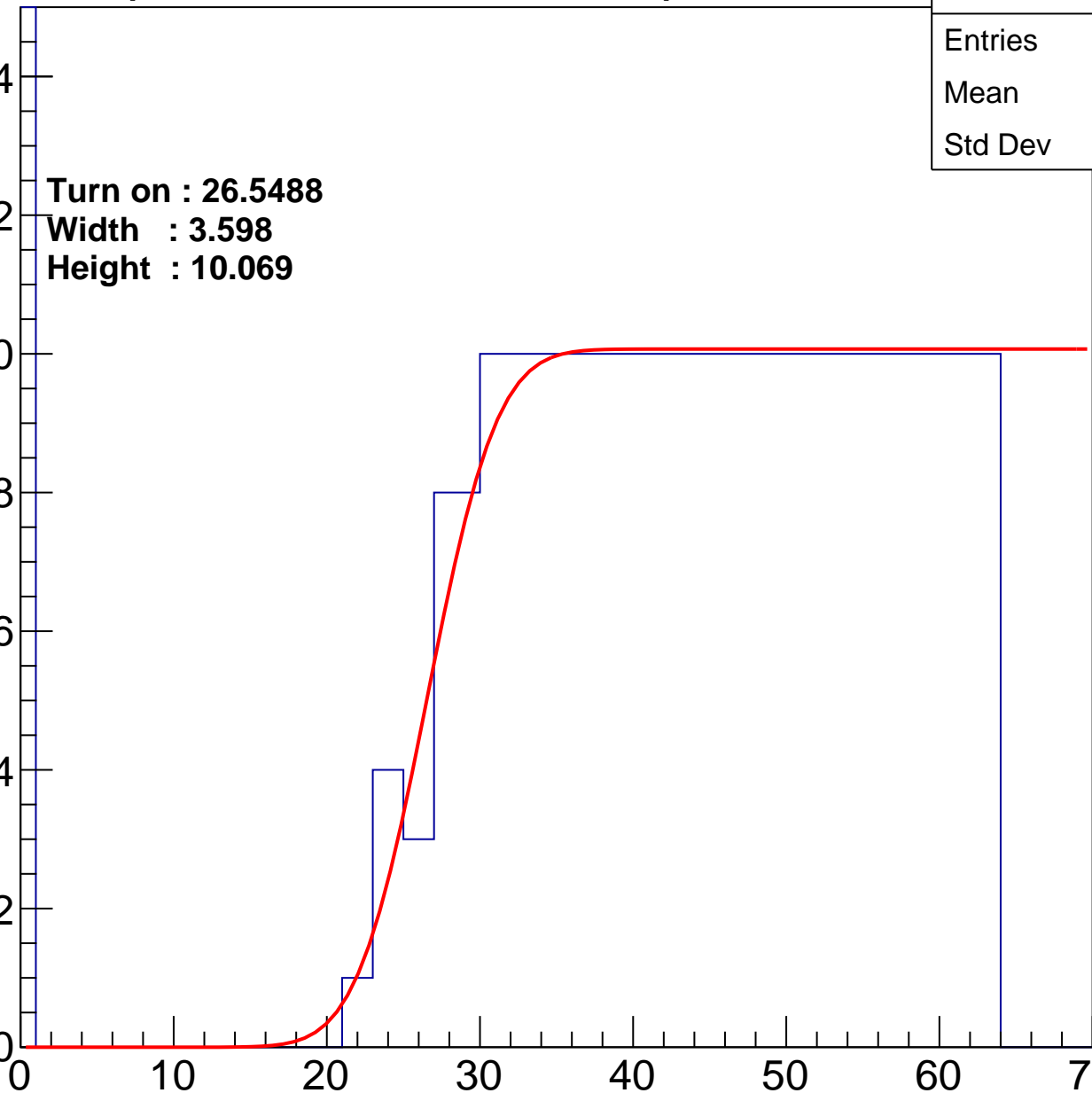
Width : 3.598

Height : 10.069

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U18-ch43

calib_packv5_041523_1651.root, FC#0, port C2

Entries	431
Mean	39.41
Std Dev	17.33

Turn on : 25.4787

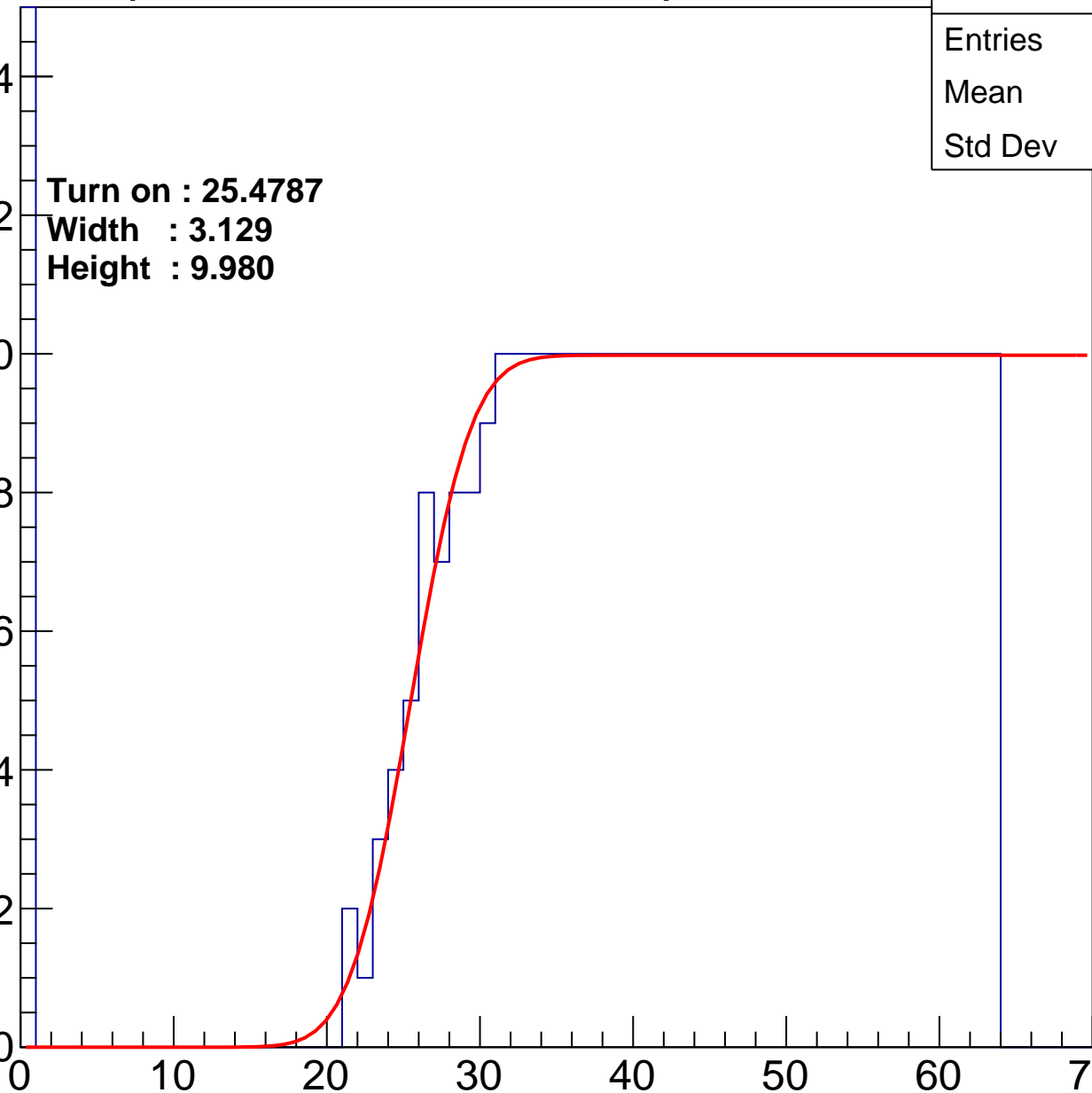
Width : 3.129

Height : 9.980

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U18-ch44

calib_packv5_041523_1651.root, FC#0, port C2

Entries	438
Mean	39.1
Std Dev	17.39

Turn on : 25.2296

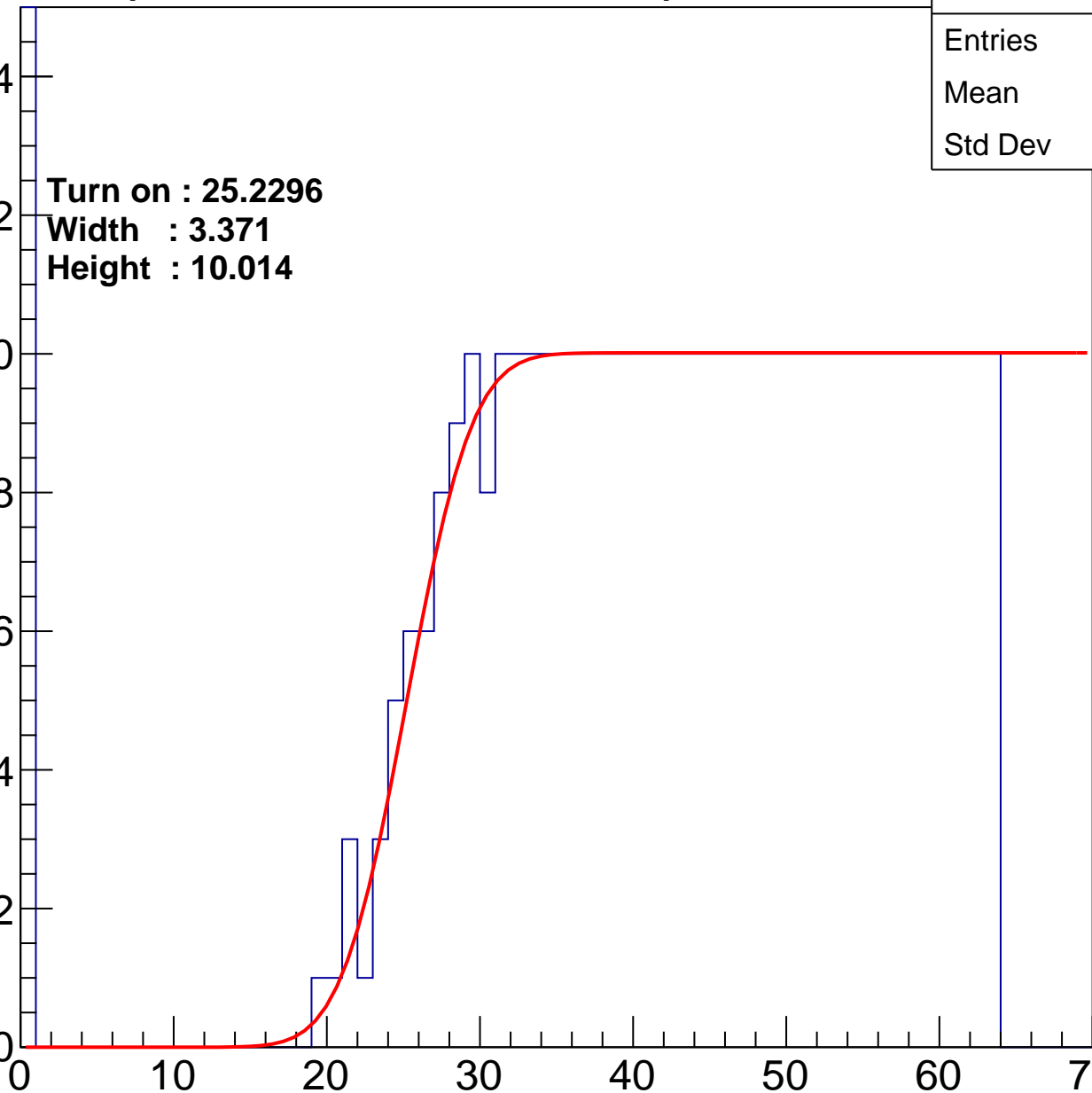
Width : 3.371

Height : 10.014

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U18-ch45

calib_packv5_041523_1651.root, FC#0, port C2

Entries	417
Mean	40.03
Std Dev	17.15

Turn on : 26.3203

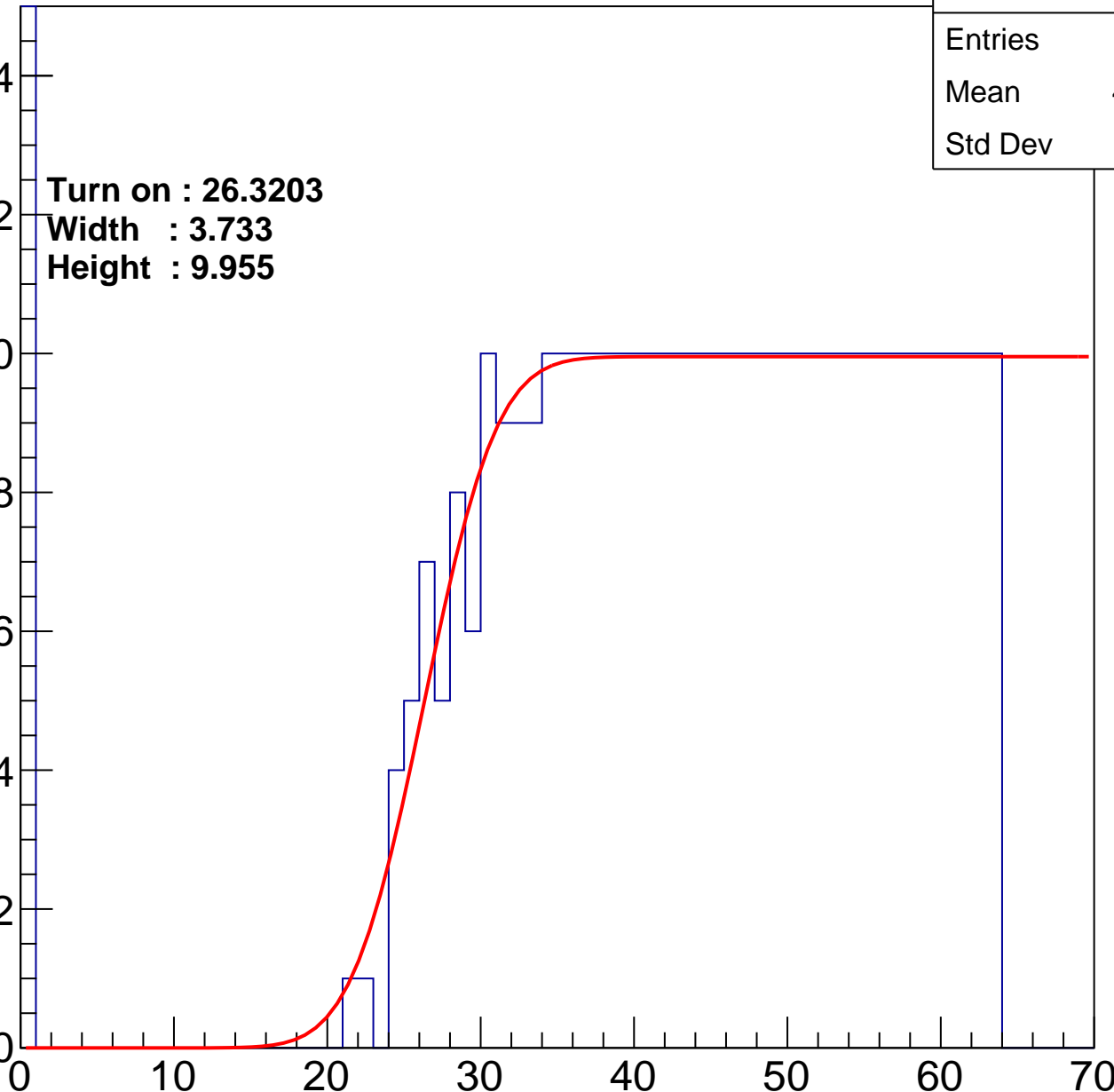
Width : 3.733

Height : 9.955

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U18-ch46

calib_packv5_041523_1651.root, FC#0, port C2

Entries	437
Mean	39.04
Std Dev	17.56

Turn on : 25.6804

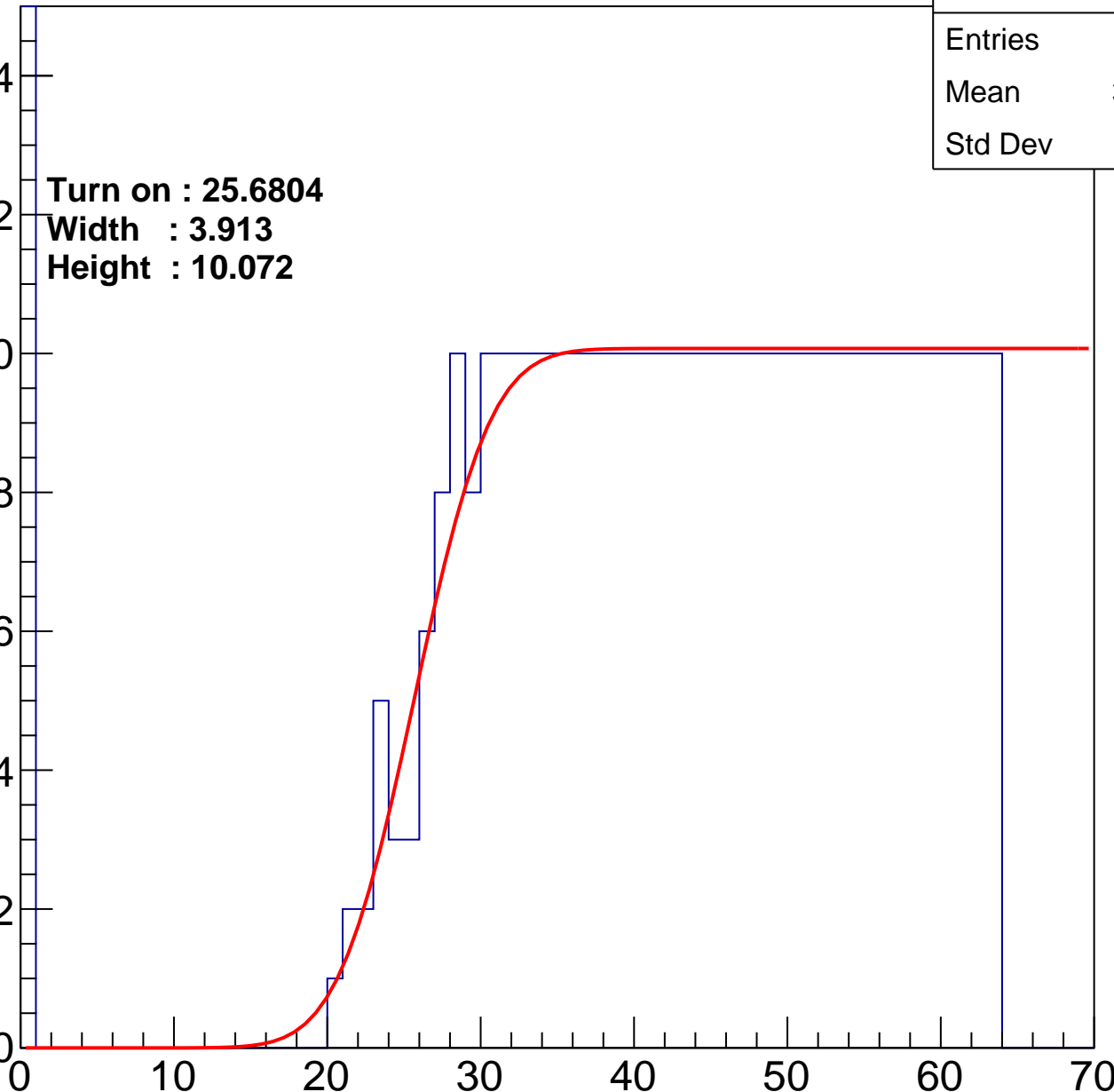
Width : 3.913

Height : 10.072

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U18-ch47

calib_packv5_041523_1651.root, FC#0, port C2

Entries	449
Mean	38.33
Std Dev	17.96

Turn on : 24.7171

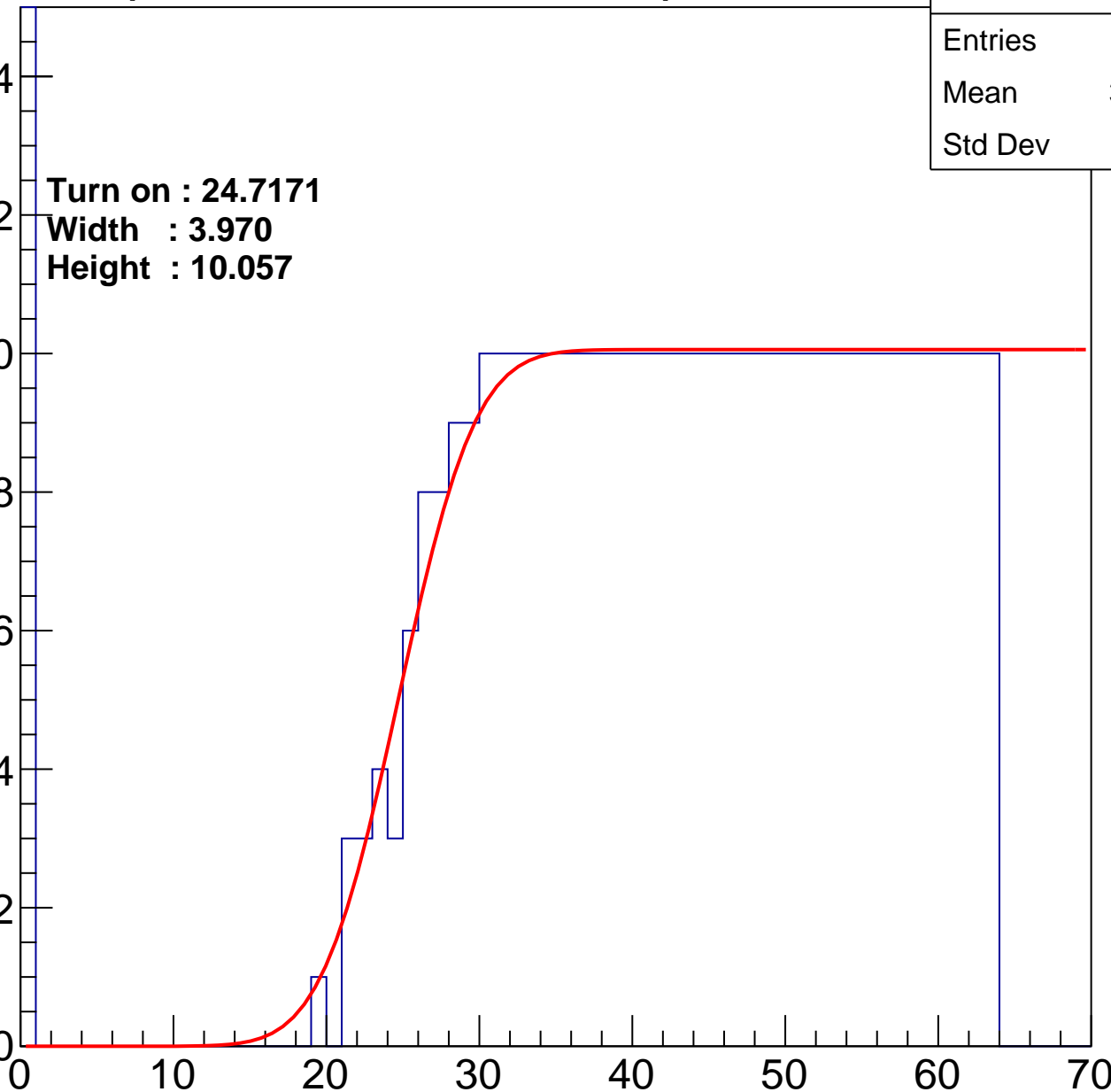
Width : 3.970

Height : 10.057

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U18-ch48

calib_packv5_041523_1651.root, FC#0, port C2

Entries	449
Mean	38.54
Std Dev	17.65

Turn on : 24.4922

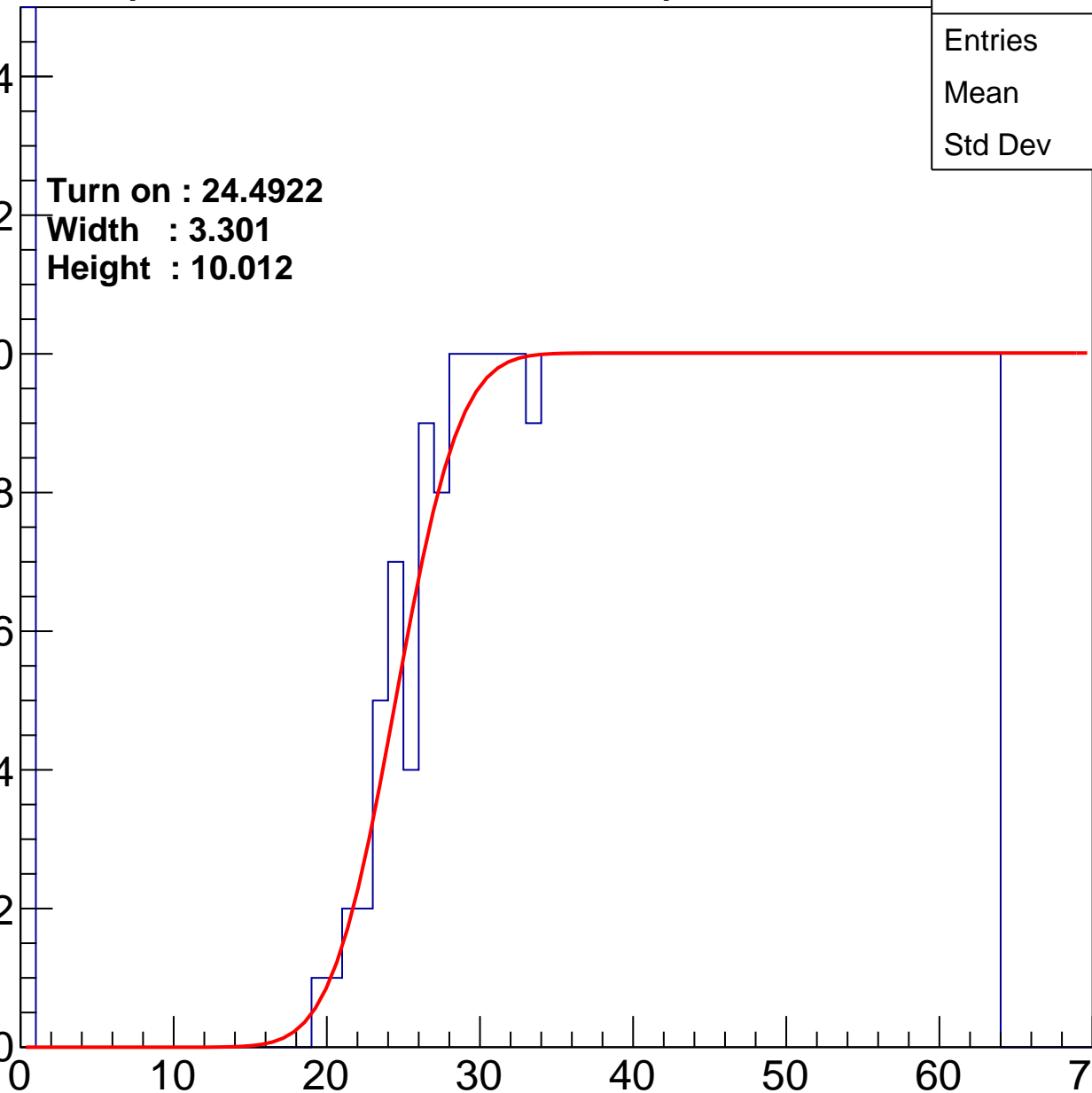
Width : 3.301

Height : 10.012

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U18-ch49

calib_packv5_041523_1651.root, FC#0, port C2

Entries	432
Mean	38.72
Std Dev	18.28

Turn on : 26.8309

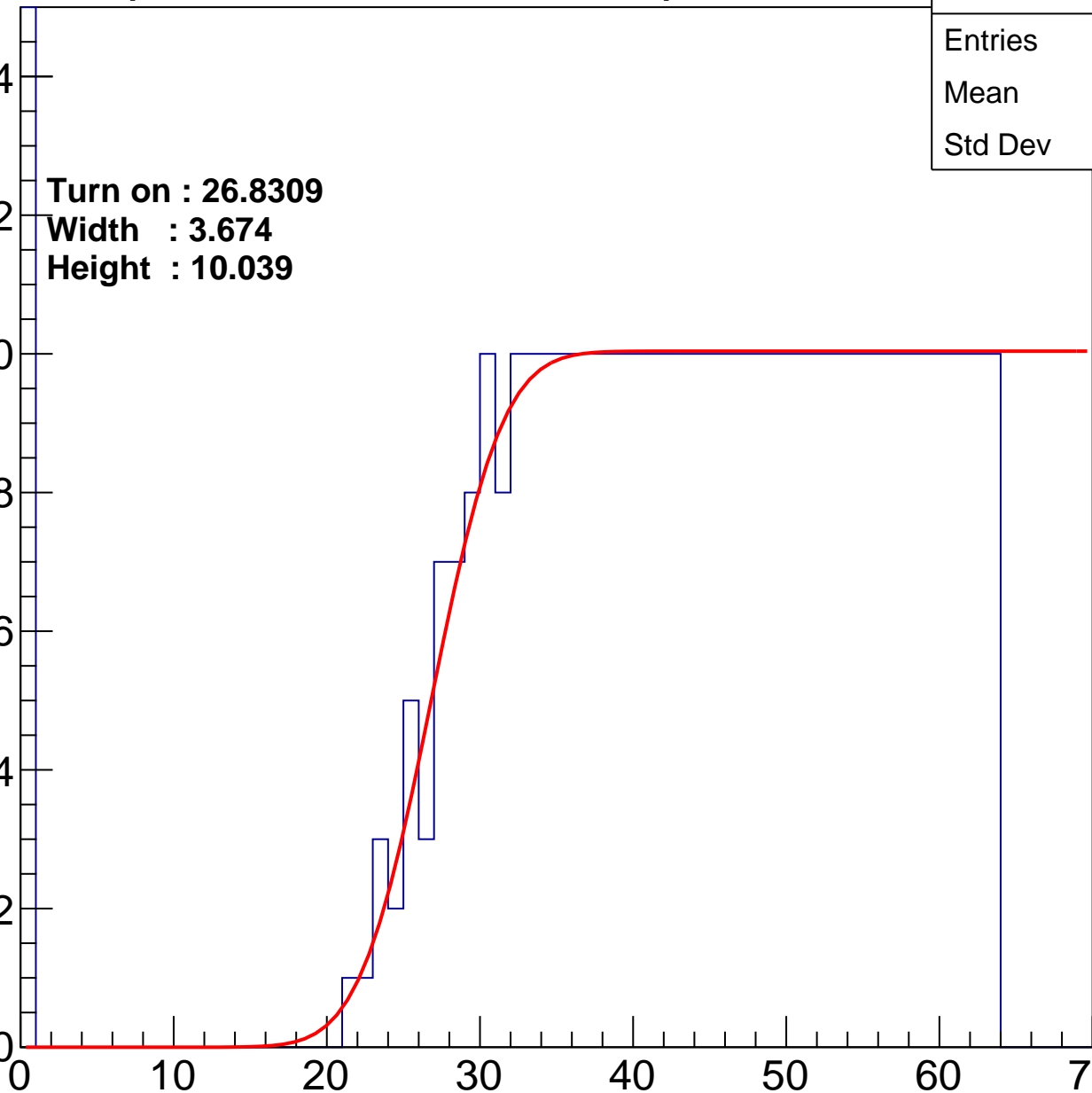
Width : 3.674

Height : 10.039

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U18-ch50

calib_packv5_041523_1651.root, FC#0, port C2

Entries	455
Mean	37.99
Std Dev	18.14

Turn on : 24.5756

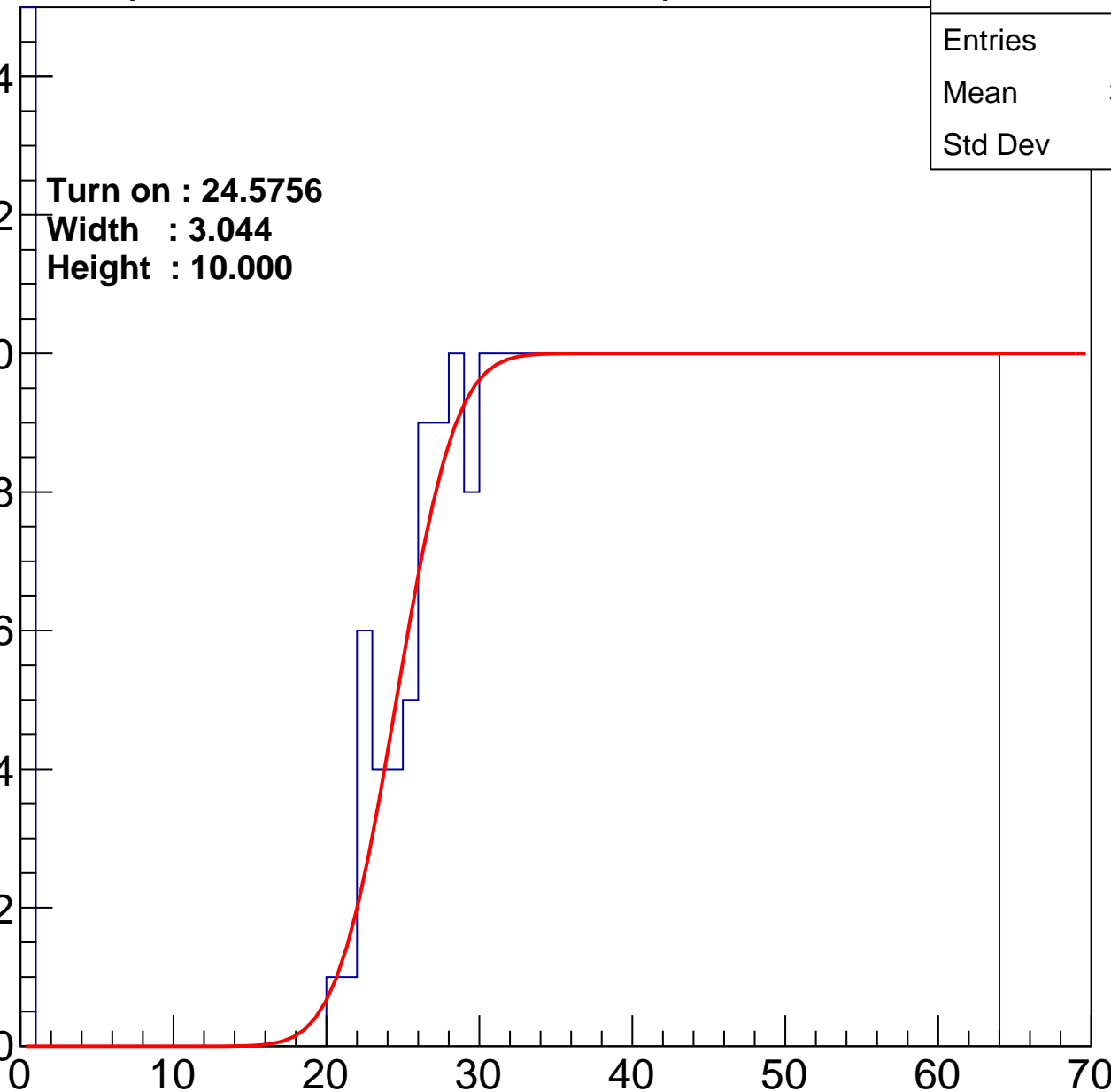
Width : 3.044

Height : 10.000

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U18-ch51

calib_packv5_041523_1651.root, FC#0, port C2

Entries	409
Mean	40.47
Std Dev	16.97

Turn on : 27.4115

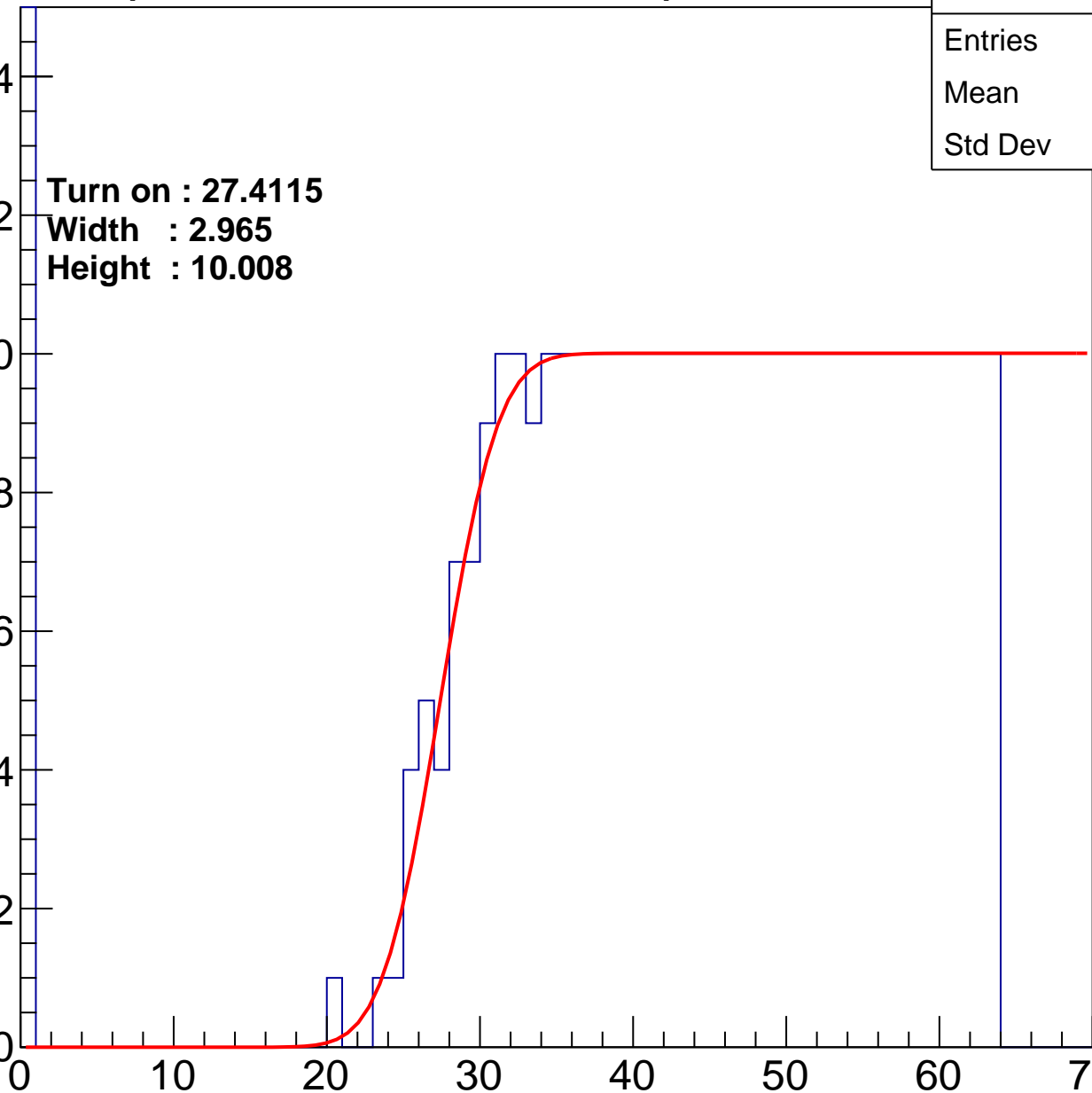
Width : 2.965

Height : 10.008

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U18-ch52

calib_packv5_041523_1651.root, FC#0, port C2

Entries	433
Mean	38.74
Std Dev	18.19

Turn on : 26.8192

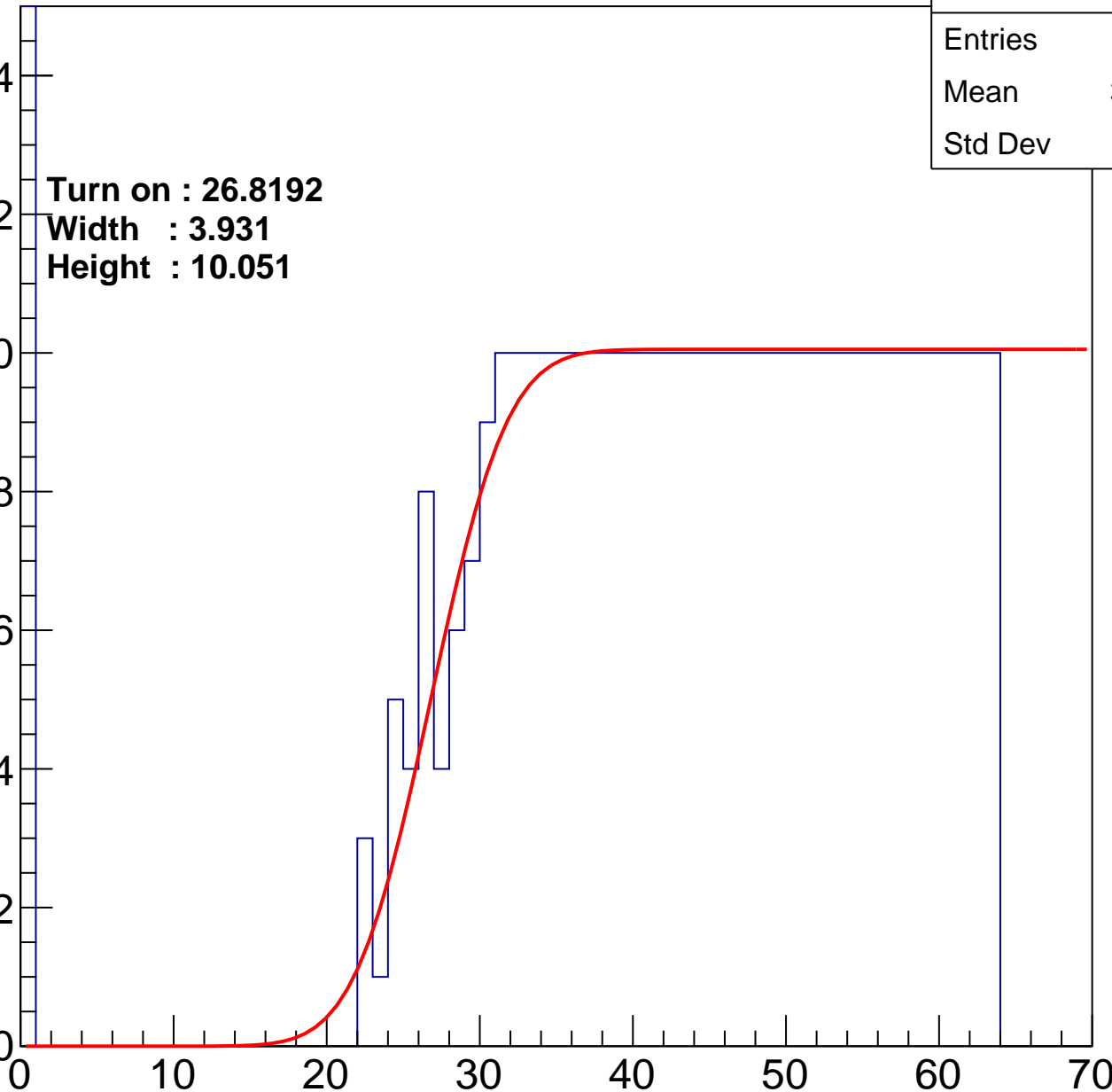
Width : 3.931

Height : 10.051

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U18-ch53

calib_packv5_041523_1651.root, FC#0, port C2

Entries	420
Mean	39.27
Std Dev	18.14

Turn on : 27.3746

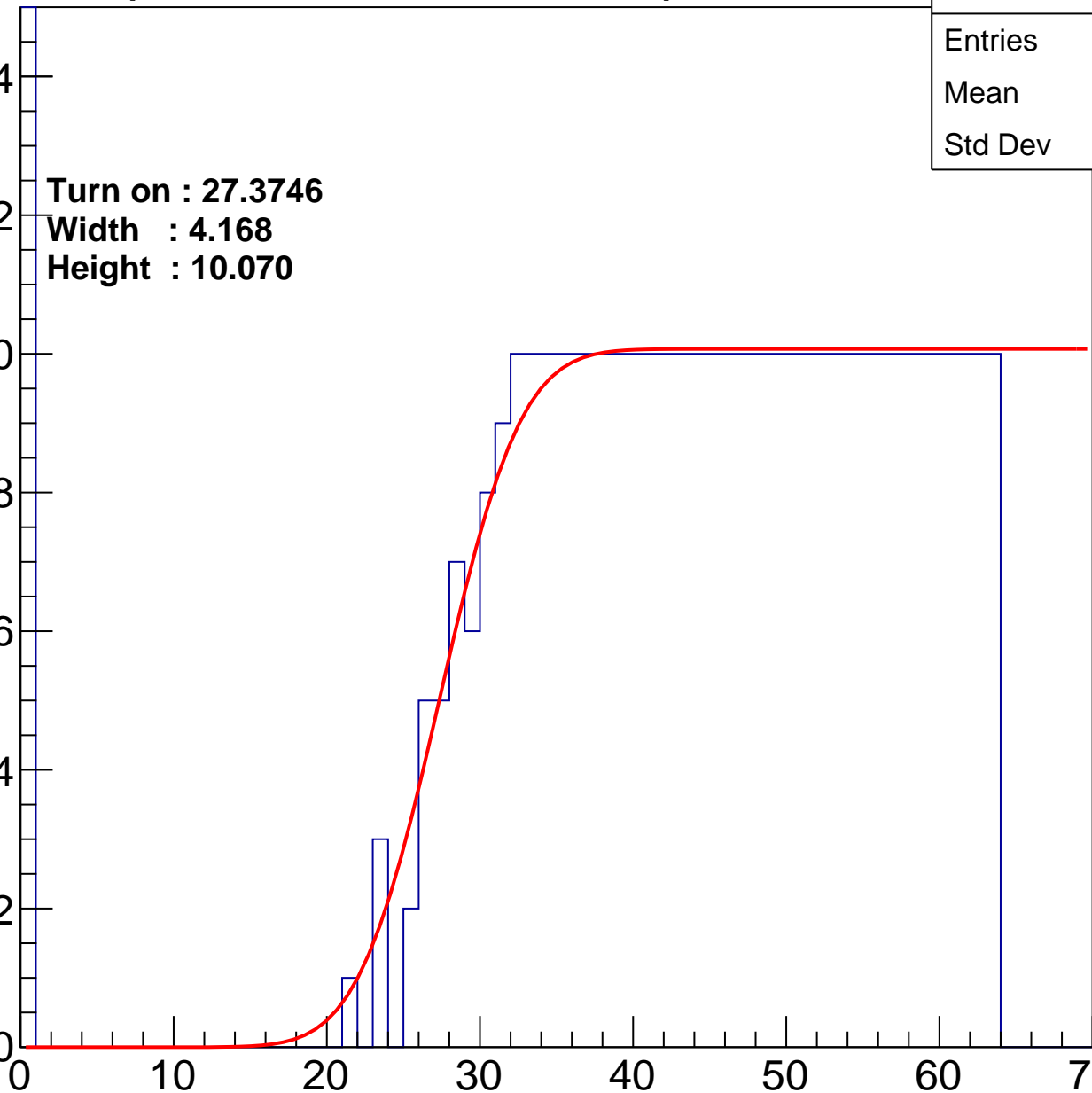
Width : 4.168

Height : 10.070

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U18-ch54

calib_packv5_041523_1651.root, FC#0, port C2

Entries	446
Mean	38.91
Std Dev	17.26

Turn on : 24.3317

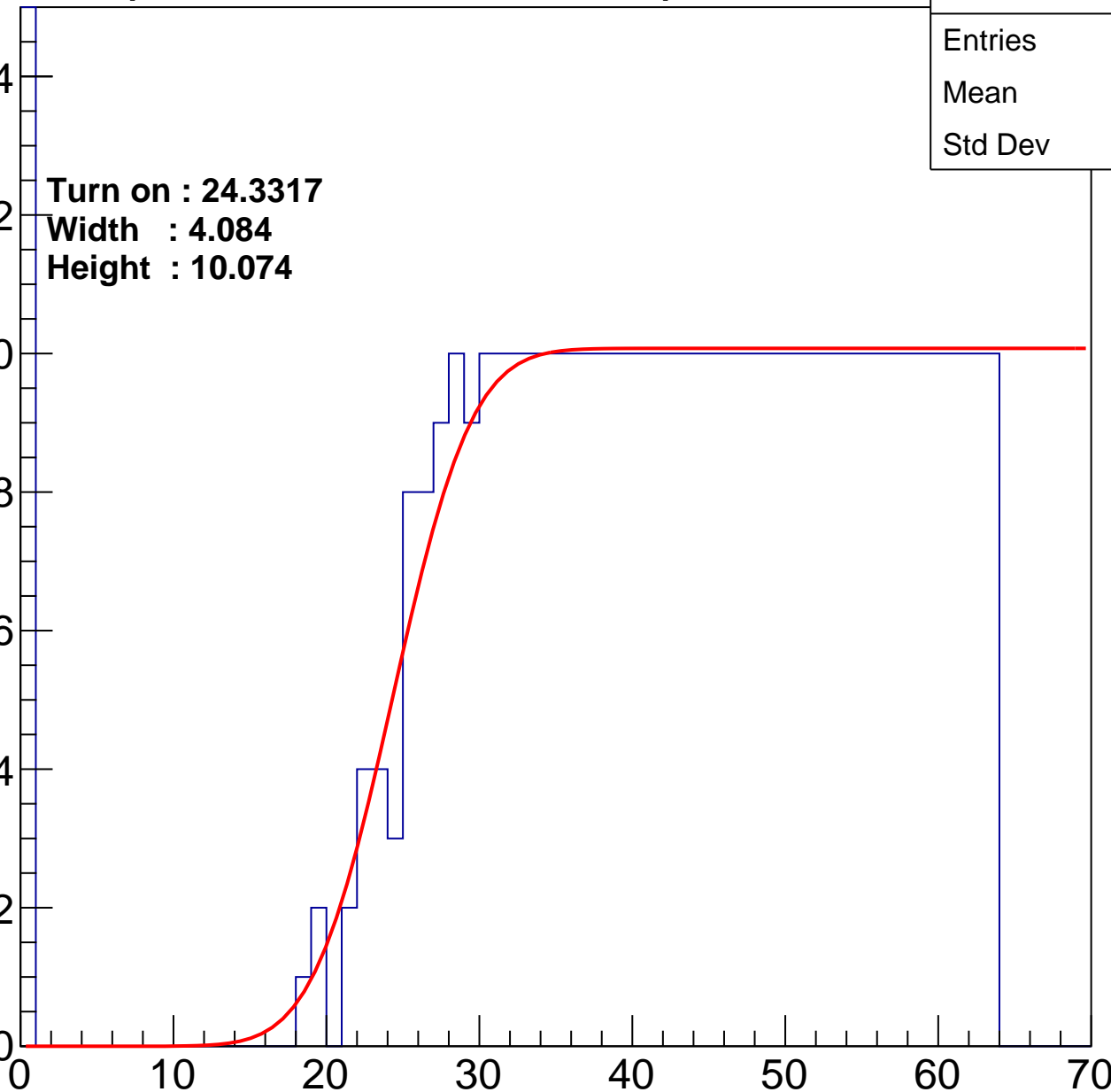
Width : 4.084

Height : 10.074

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U18-ch55

calib_packv5_041523_1651.root, FC#0, port C2

Entries	401
Mean	39.84
Std Dev	18.36

Turn on : 29.7983

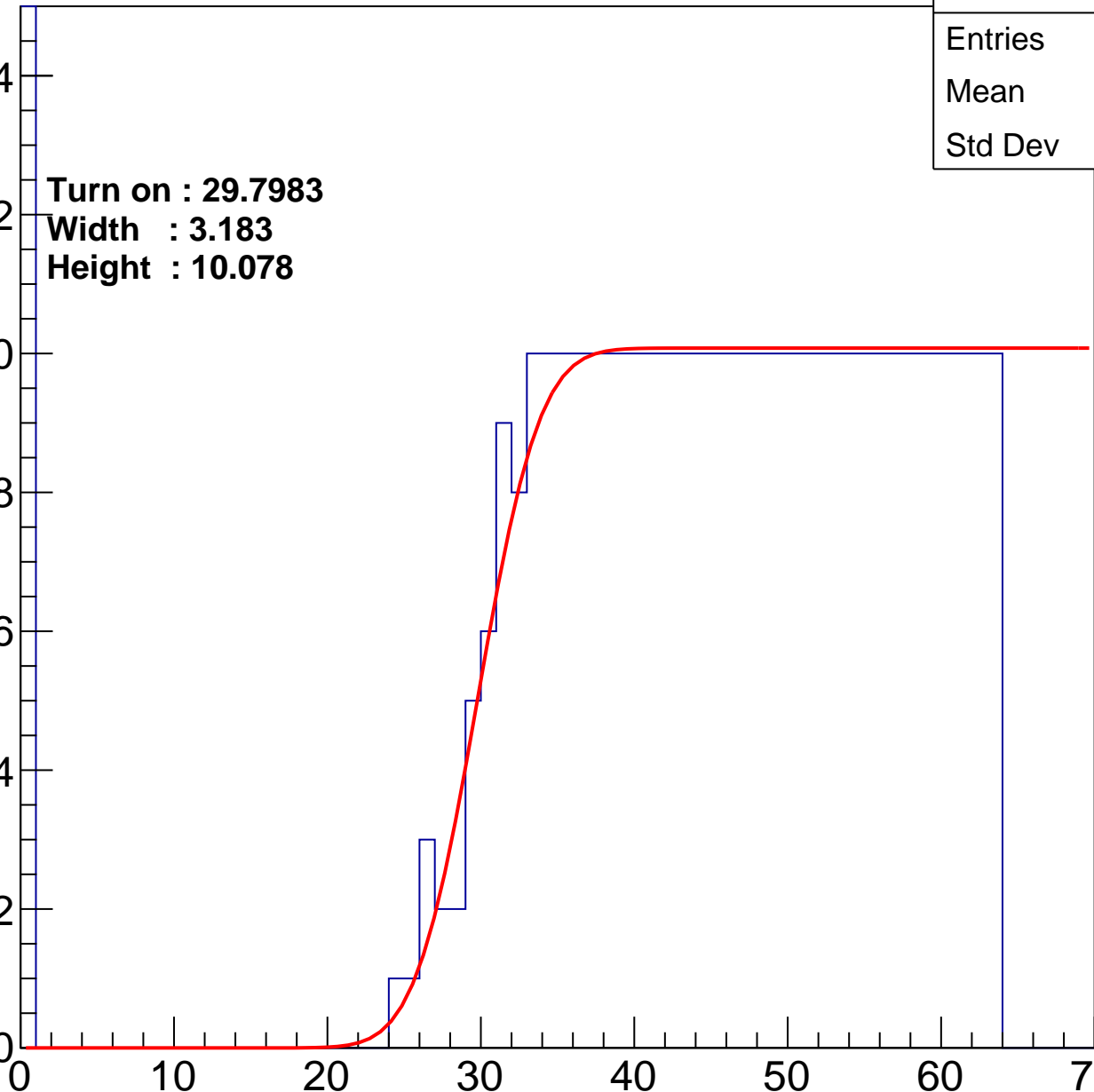
Width : 3.183

Height : 10.078

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U18-ch56

calib_packv5_041523_1651.root, FC#0, port C2

Entries	437
Mean	38.49
Std Dev	18.37

Turn on : 26.8498

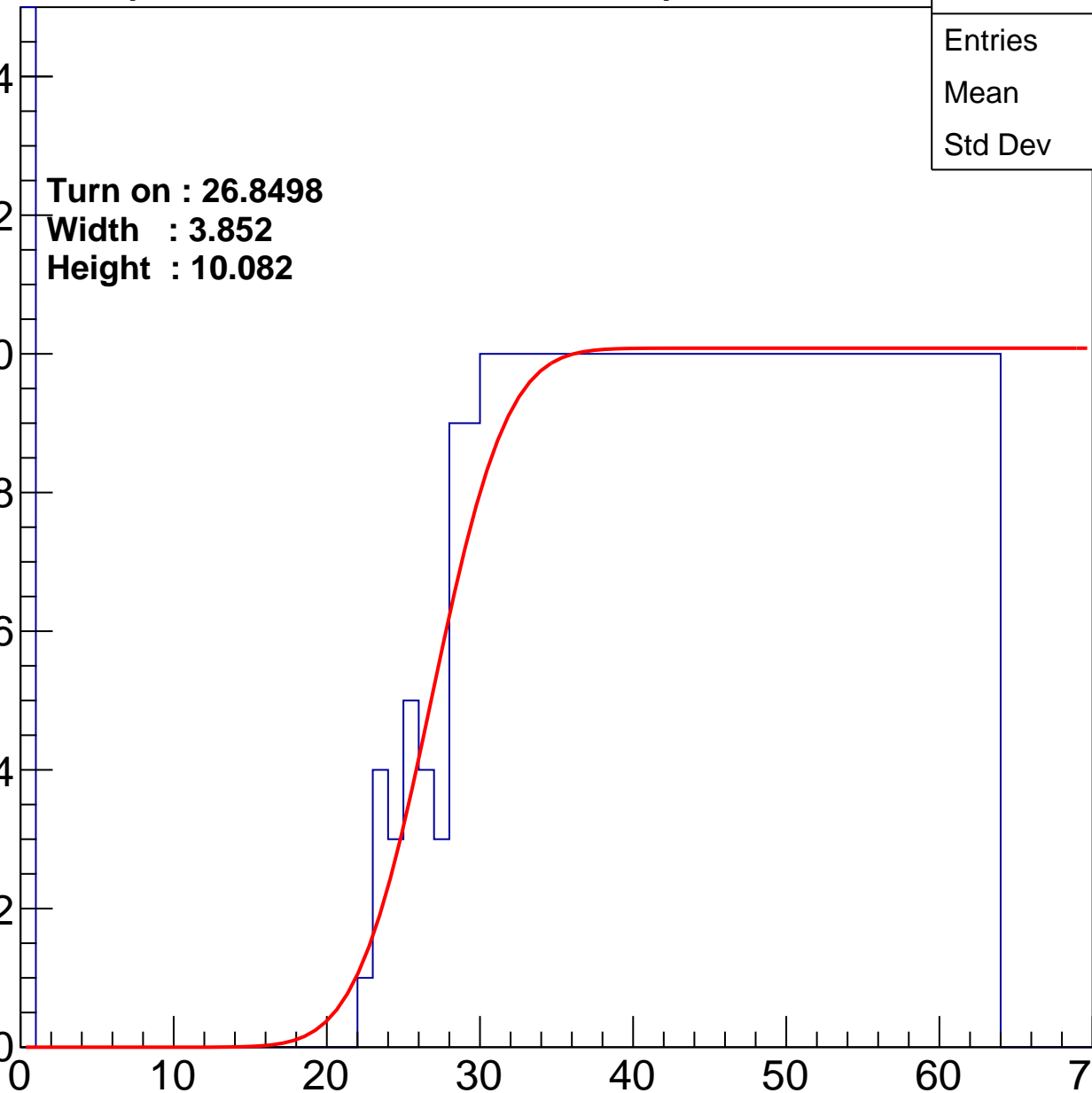
Width : 3.852

Height : 10.082

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U18-ch57

calib_packv5_041523_1651.root, FC#0, port C2

Entries	433
Mean	39.21
Std Dev	17.55

Turn on : 25.6232

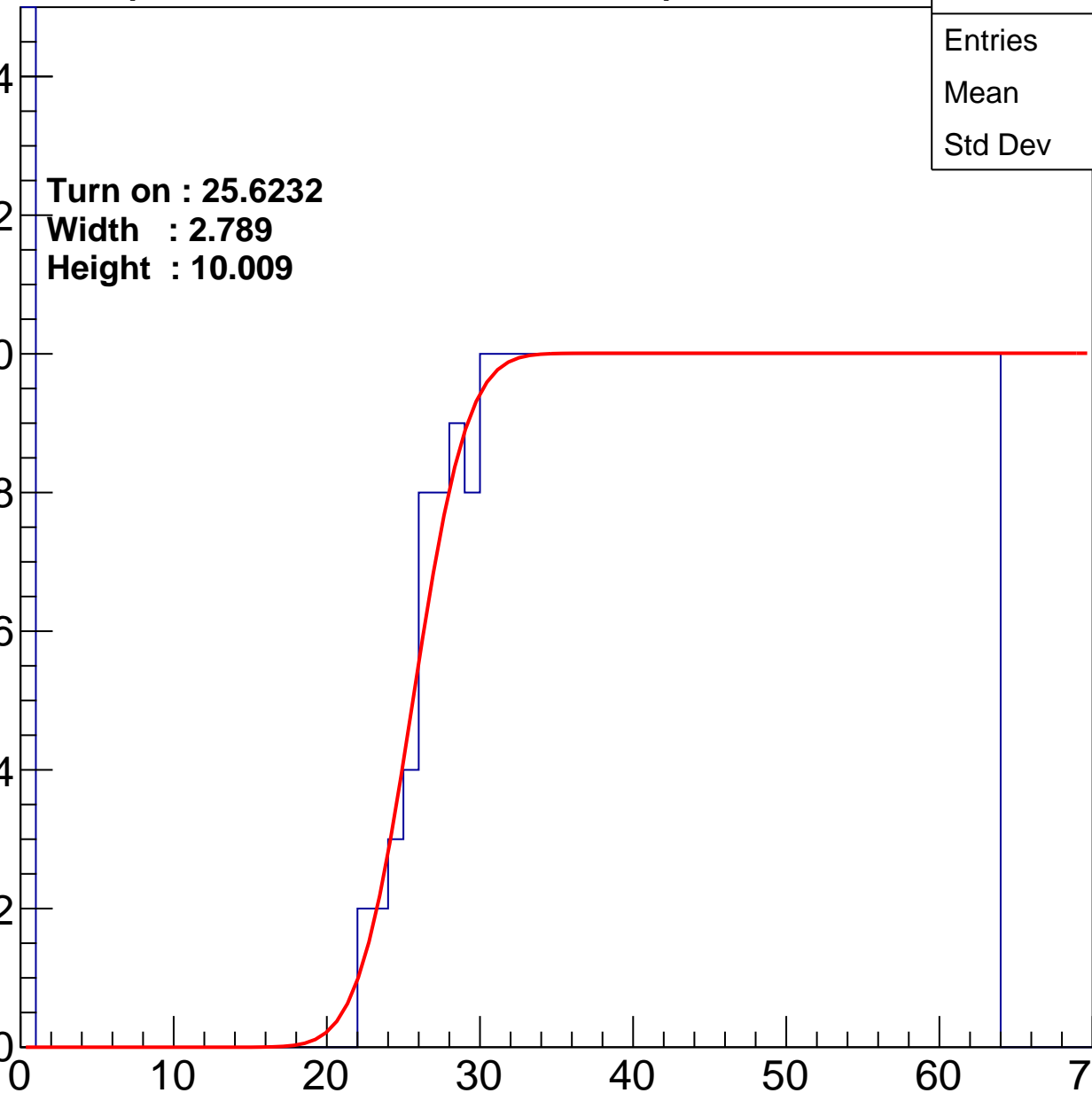
Width : 2.789

Height : 10.009

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U18-ch58

calib_packv5_041523_1651.root, FC#0, port C2

Entries	433
Mean	40
Std Dev	16.23

Turn on : 24.0202

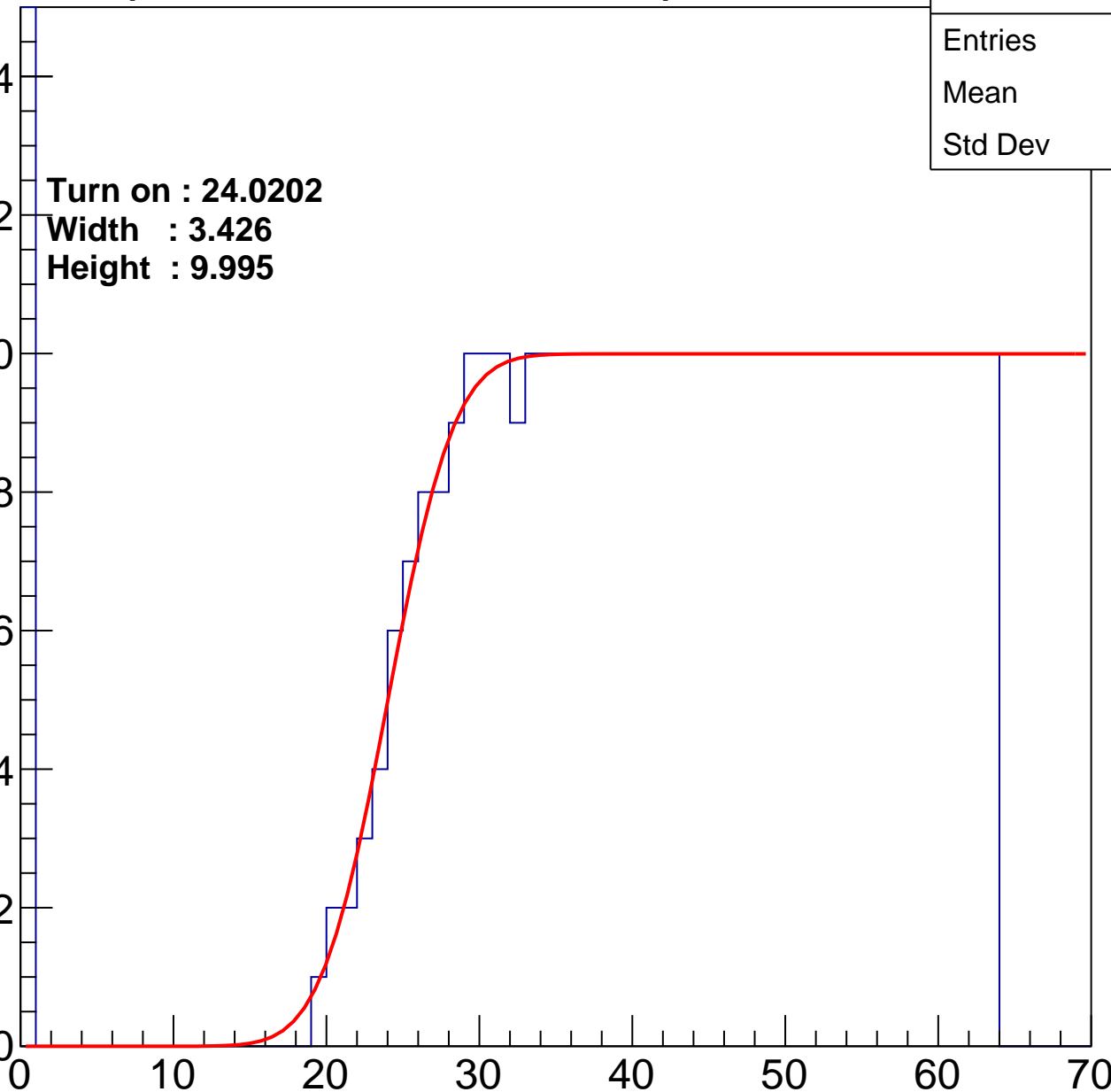
Width : 3.426

Height : 9.995

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U18-ch59

calib_packv5_041523_1651.root, FC#0, port C2

Entries	455
Mean	37.61
Std Dev	18.66

Turn on : 25.0604

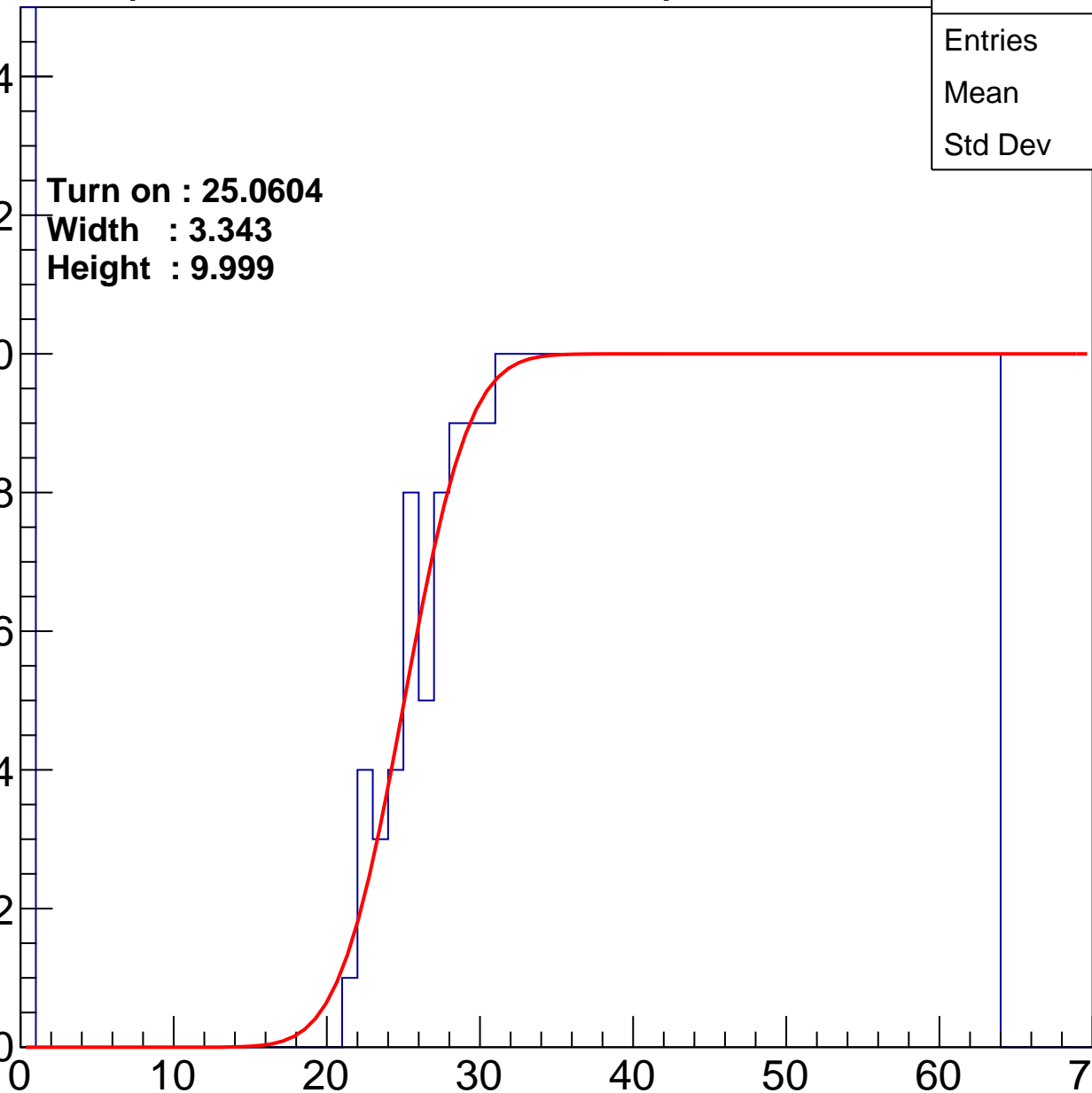
Width : 3.343

Height : 9.999

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U18-ch60

calib_packv5_041523_1651.root, FC#0, port C2

Entries	444
Mean	38.04
Std Dev	18.63

Turn on : 26.3681

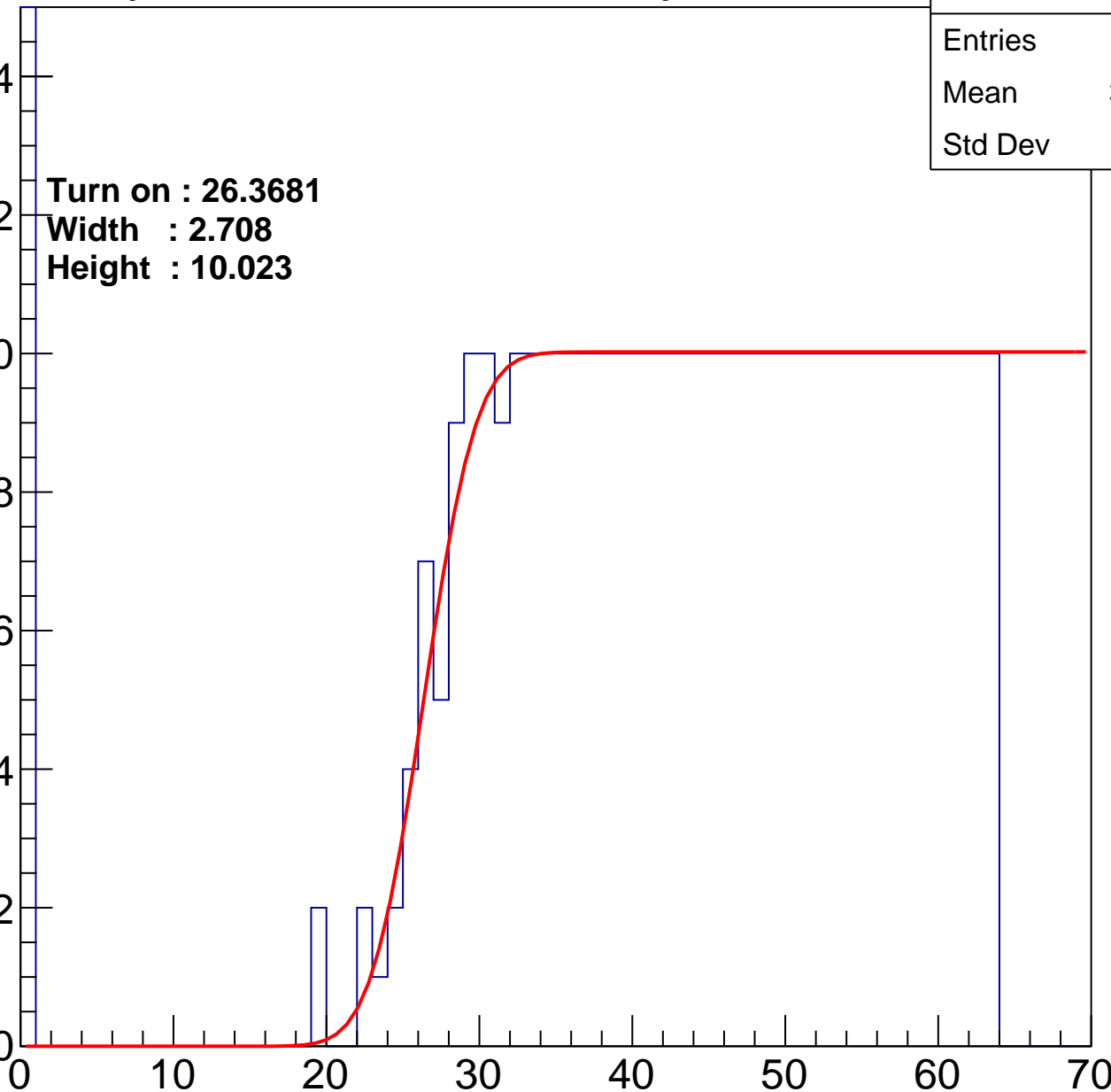
Width : 2.708

Height : 10.023

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U18-ch61

calib_packv5_041523_1651.root, FC#0, port C2

Entries	432
Mean	38.79
Std Dev	18.15

Turn on : 26.5954

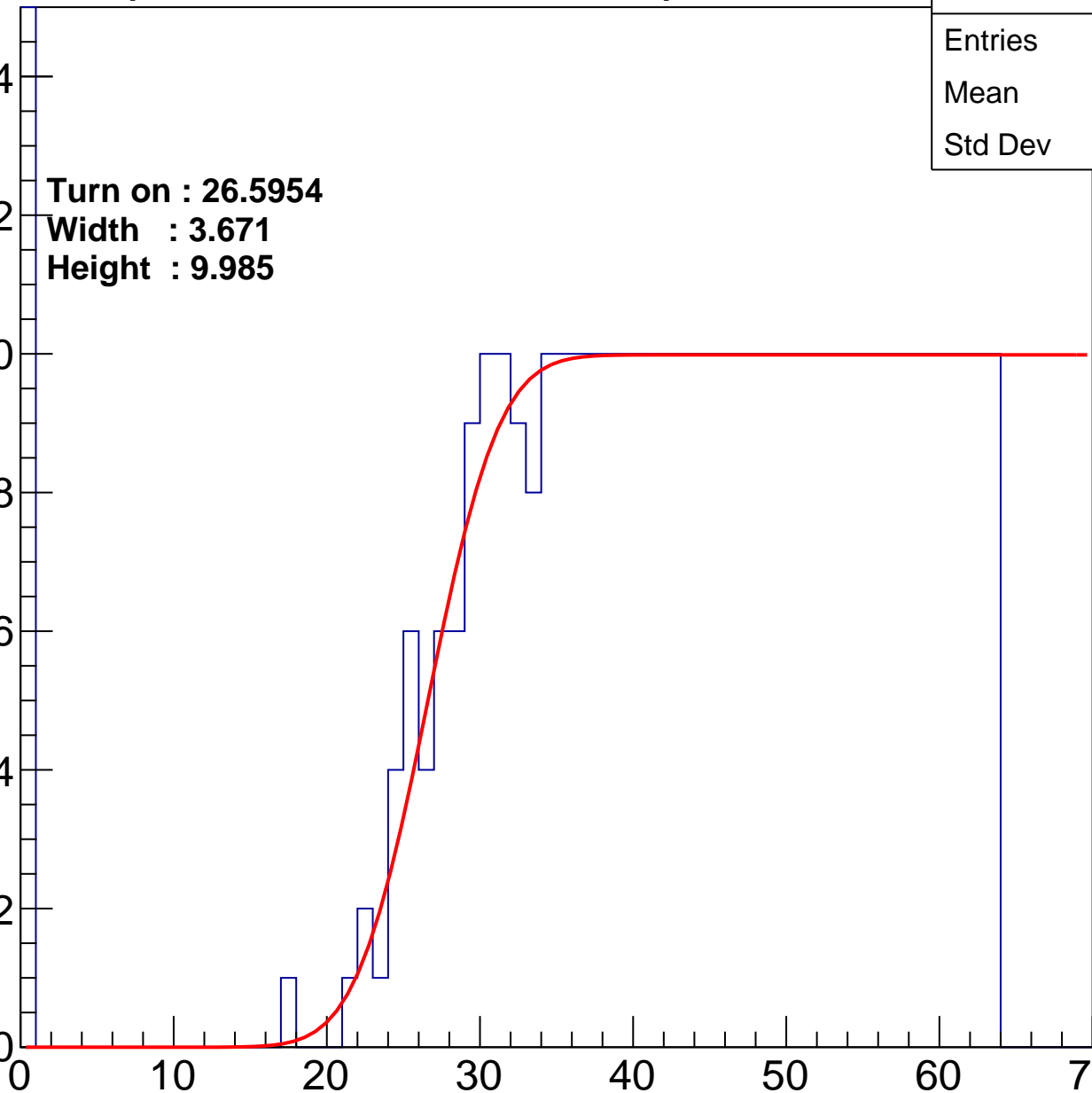
Width : 3.671

Height : 9.985

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U18-ch62

calib_packv5_041523_1651.root, FC#0, port C2

Entries	456
Mean	38.4
Std Dev	17.5

Turn on : 23.2218

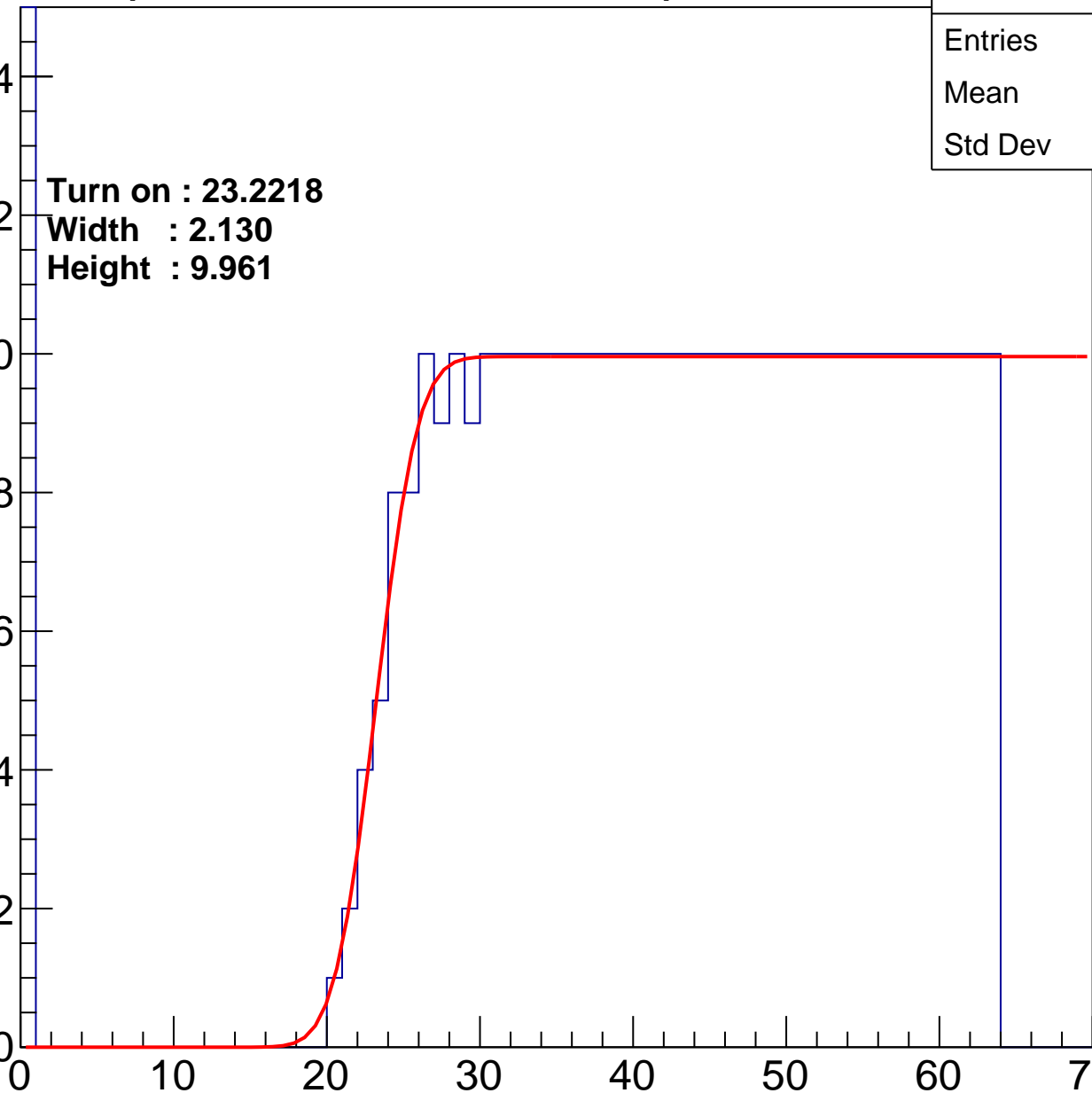
Width : 2.130

Height : 9.961

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U18-ch63

calib_packv5_041523_1651.root, FC#0, port C2

Entries	410
Mean	40.22
Std Dev	17.29

Turn on : 27.8328

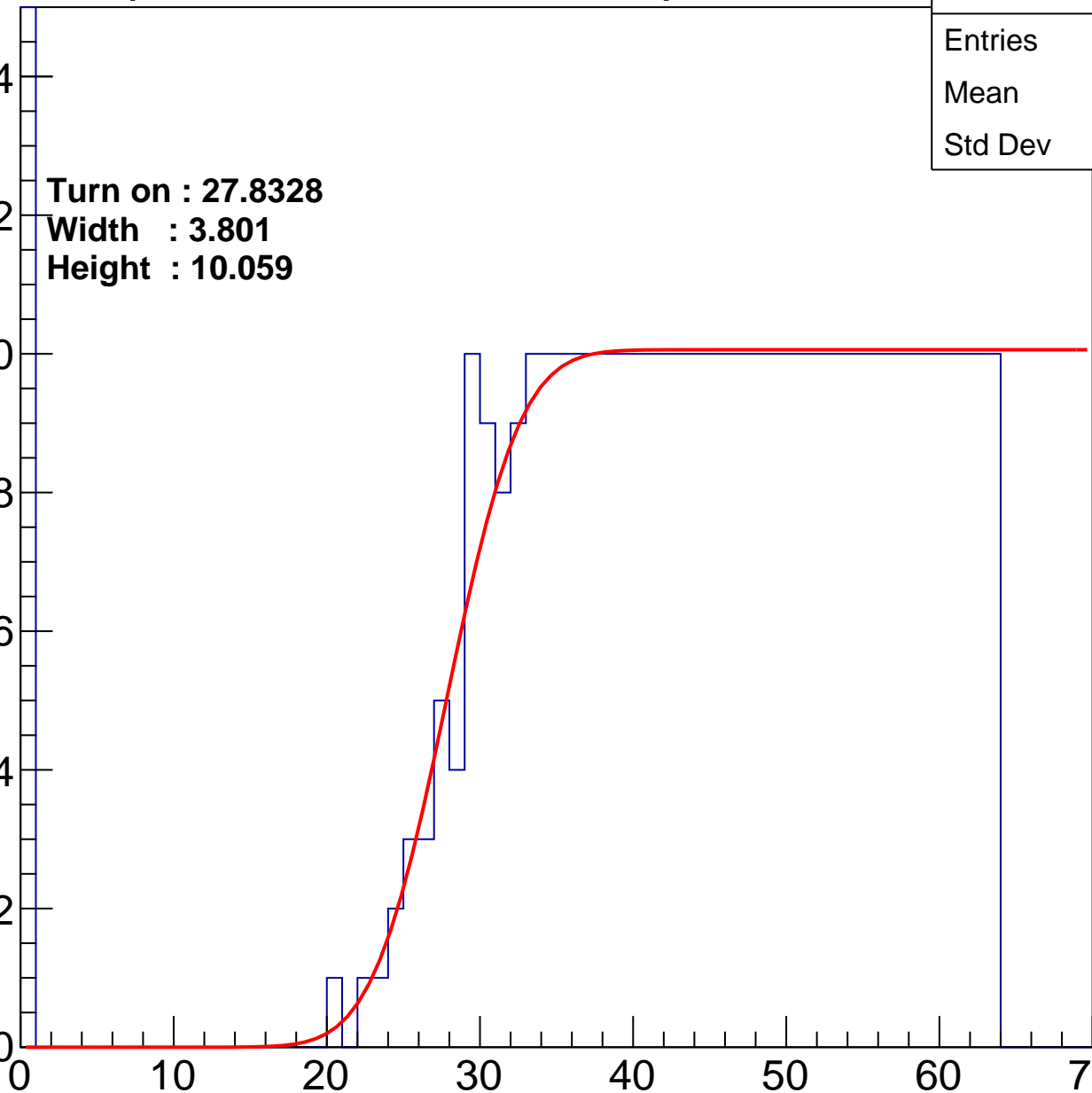
Width : 3.801

Height : 10.059

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U18-ch64

calib_packv5_041523_1651.root, FC#0, port C2

Entries	439
Mean	39.33
Std Dev	17.01

Turn on : 24.7228

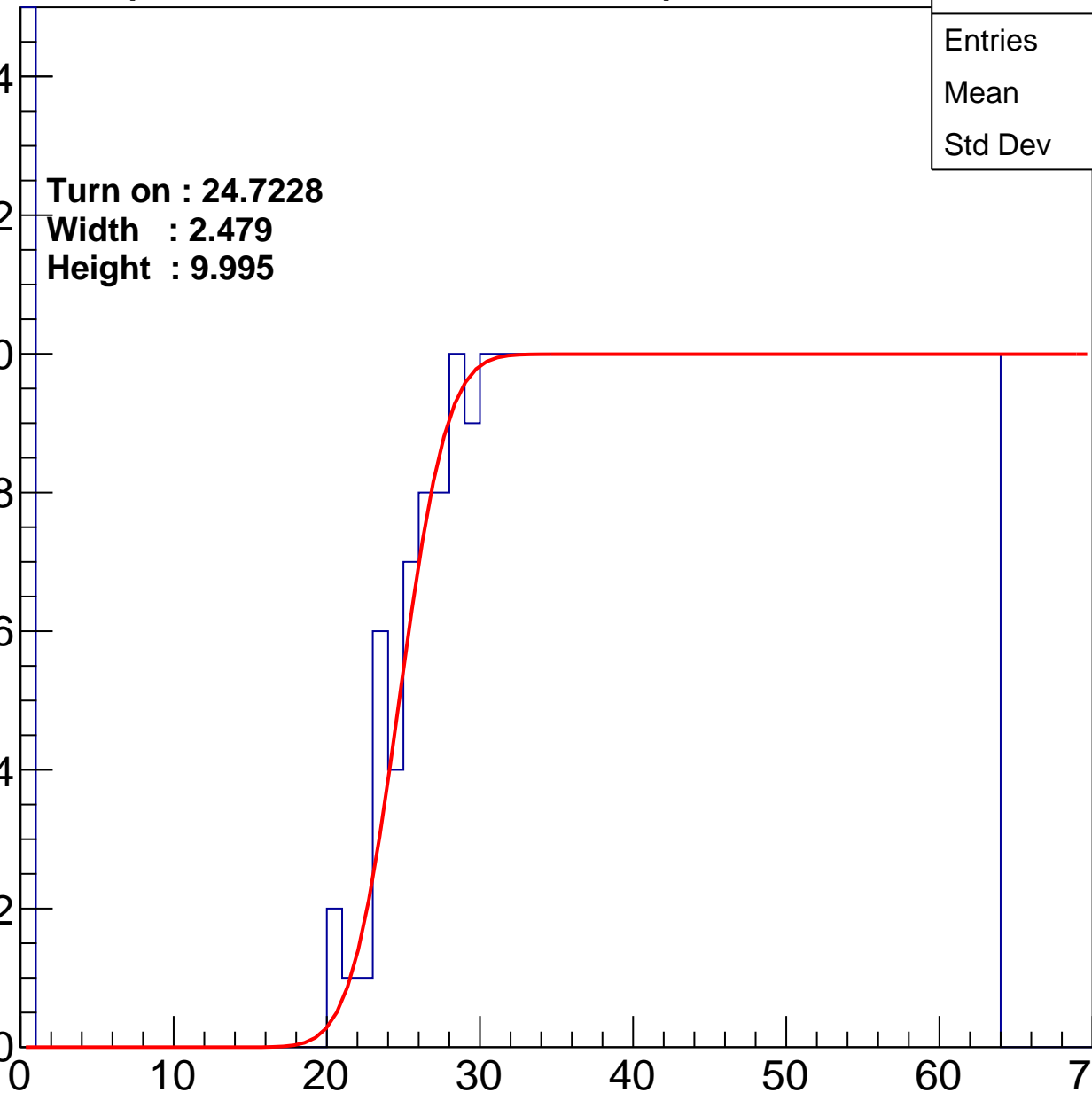
Width : 2.479

Height : 9.995

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U18-ch65

calib_packv5_041523_1651.root, FC#0, port C2

Entries	408
Mean	41.08
Std Dev	16.01

Turn on : 26.5263

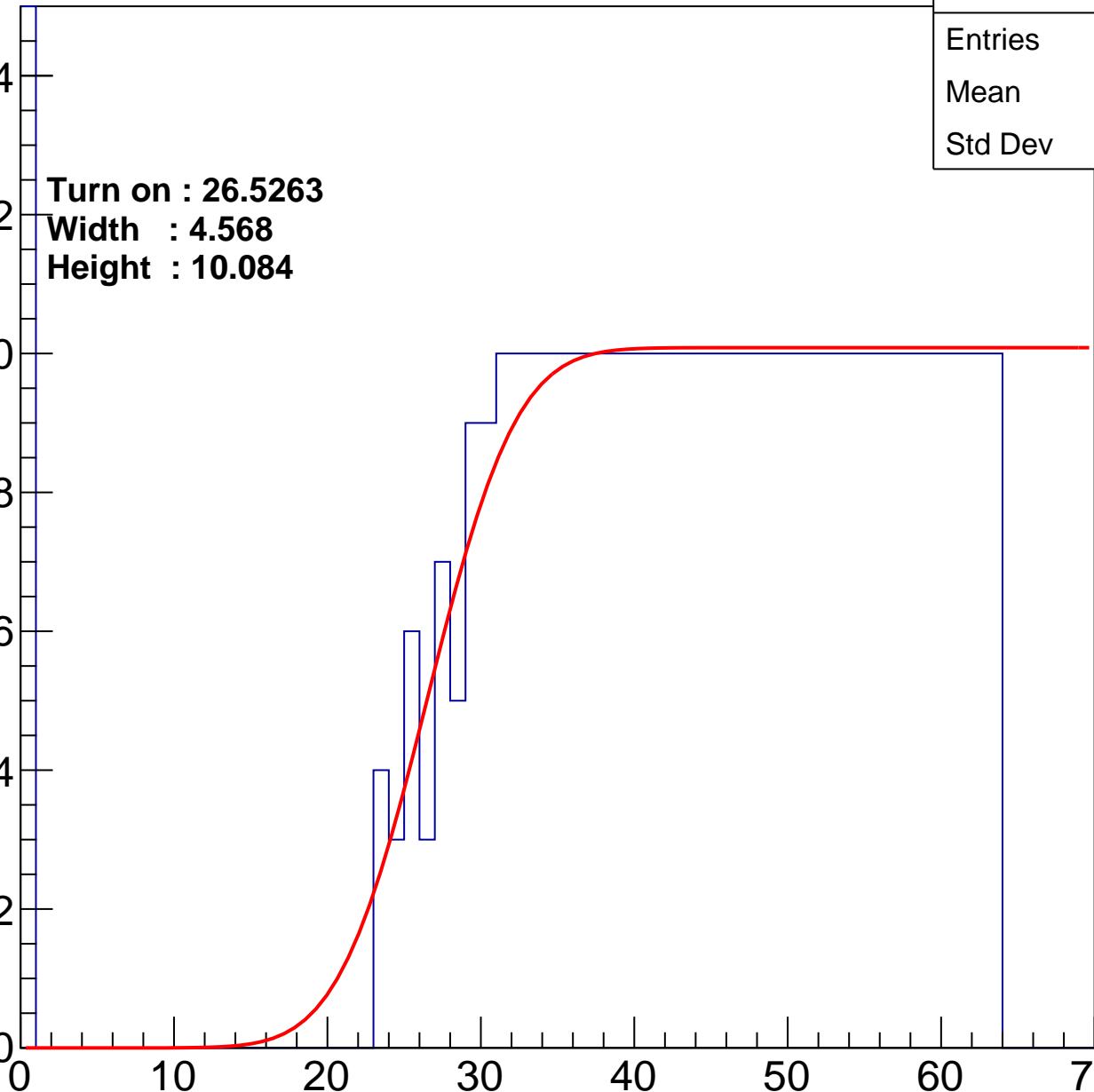
Width : 4.568

Height : 10.084

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U18-ch66

calib_packv5_041523_1651.root, FC#0, port C2

Entries	424
Mean	40.14
Std Dev	16.59

Turn on : 25.9494

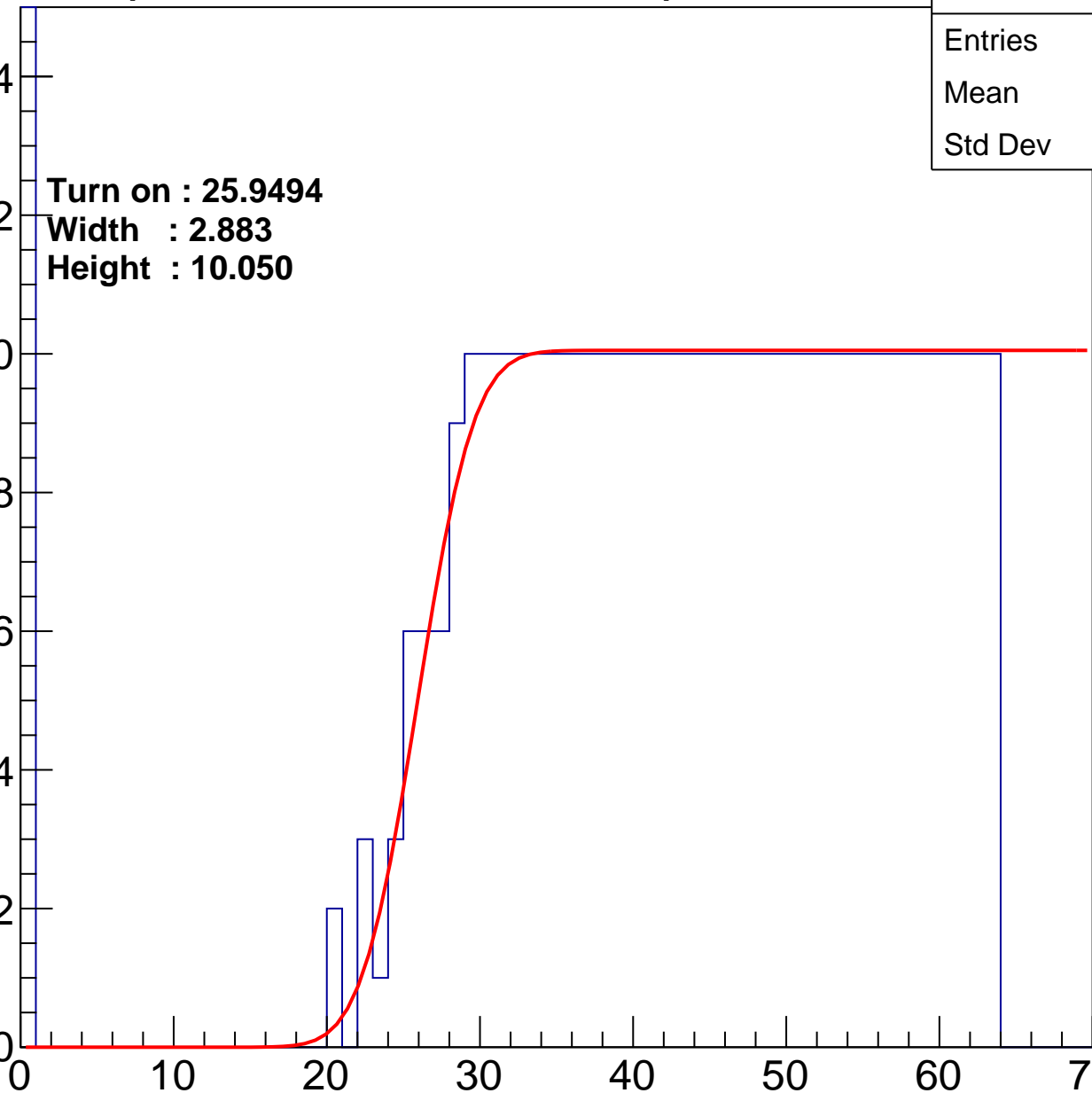
Width : 2.883

Height : 10.050

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U18-ch67

calib_packv5_041523_1651.root, FC#0, port C2

Entries	429
Mean	39.48
Std Dev	17.34

Turn on : 25.4759

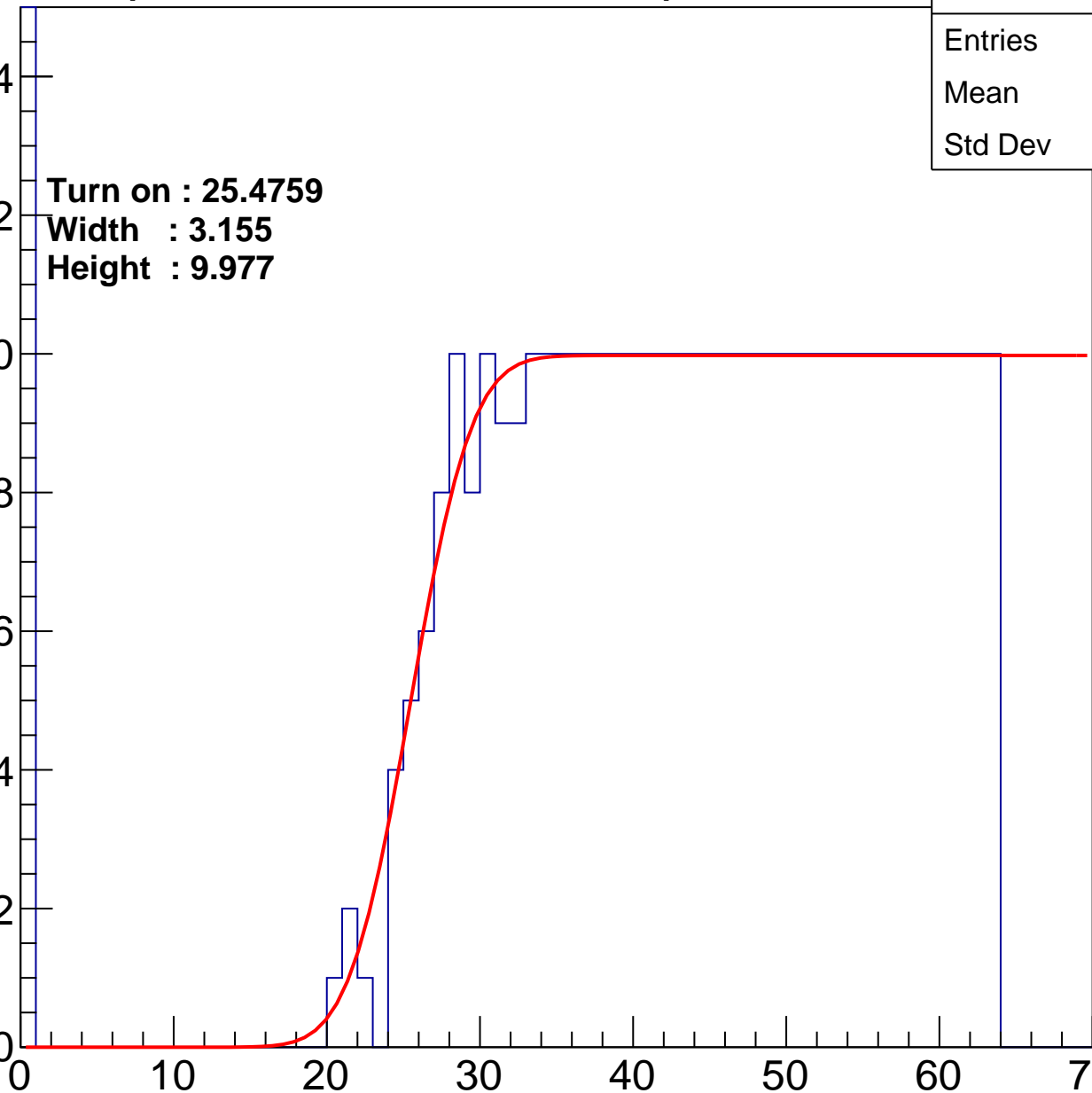
Width : 3.155

Height : 9.977

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U18-ch68

calib_packv5_041523_1651.root, FC#0, port C2

Entries	439
Mean	39.29
Std Dev	17.05

Turn on : 24.9006

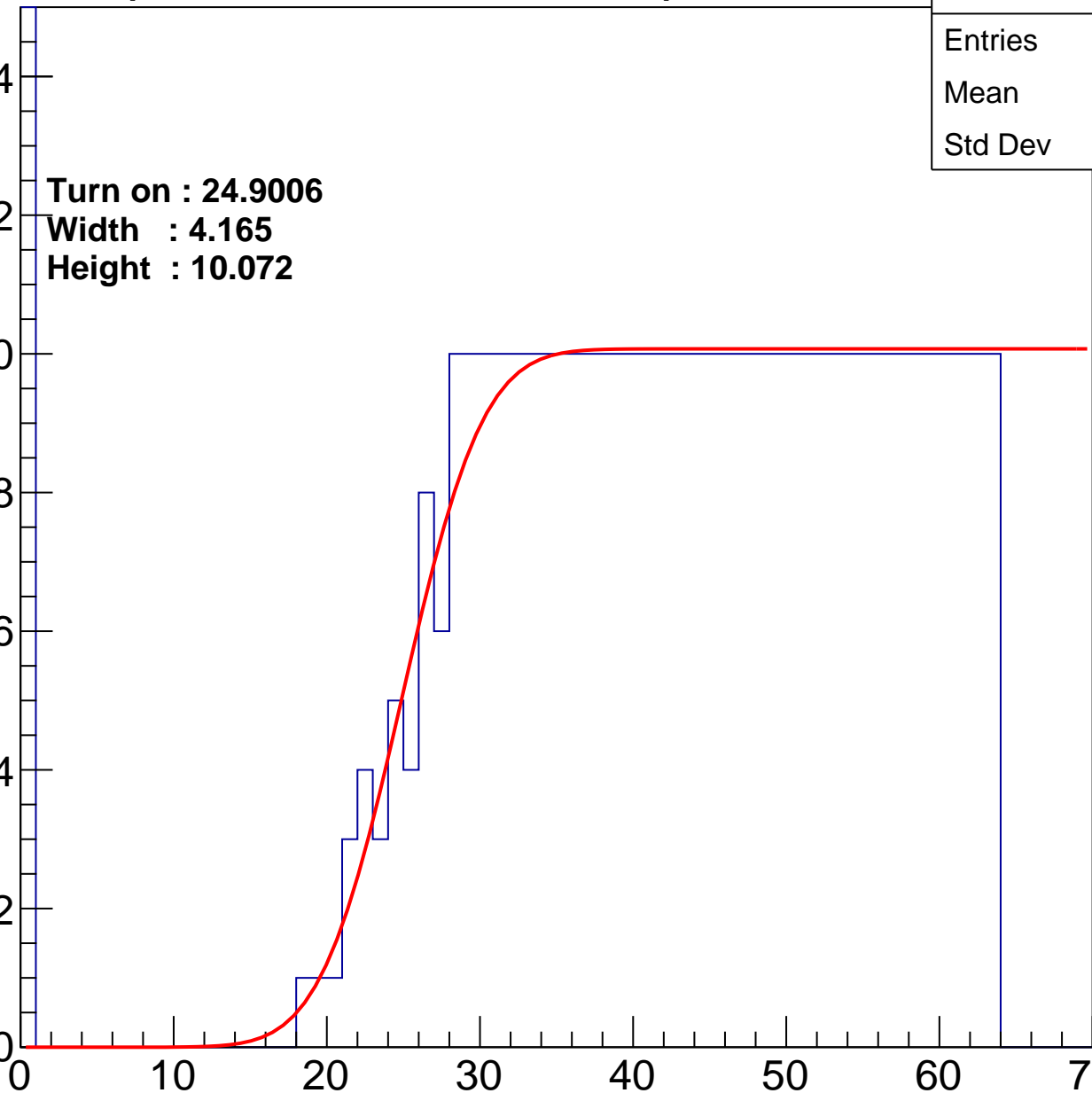
Width : 4.165

Height : 10.072

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U18-ch69

calib_packv5_041523_1651.root, FC#0, port C2

Entries	409
Mean	40.25
Std Dev	17.34

Turn on : 27.6885

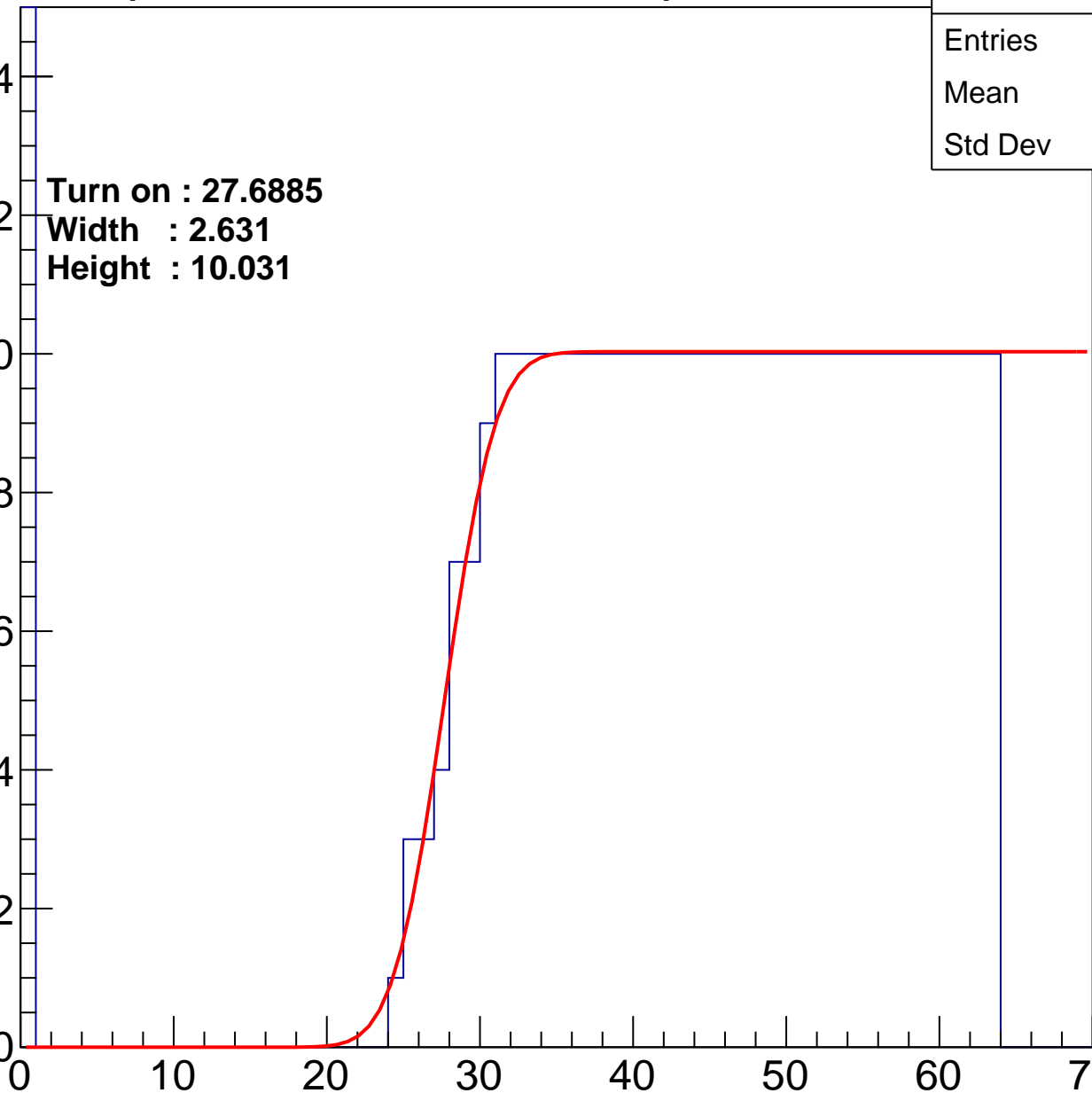
Width : 2.631

Height : 10.031

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U18-ch70

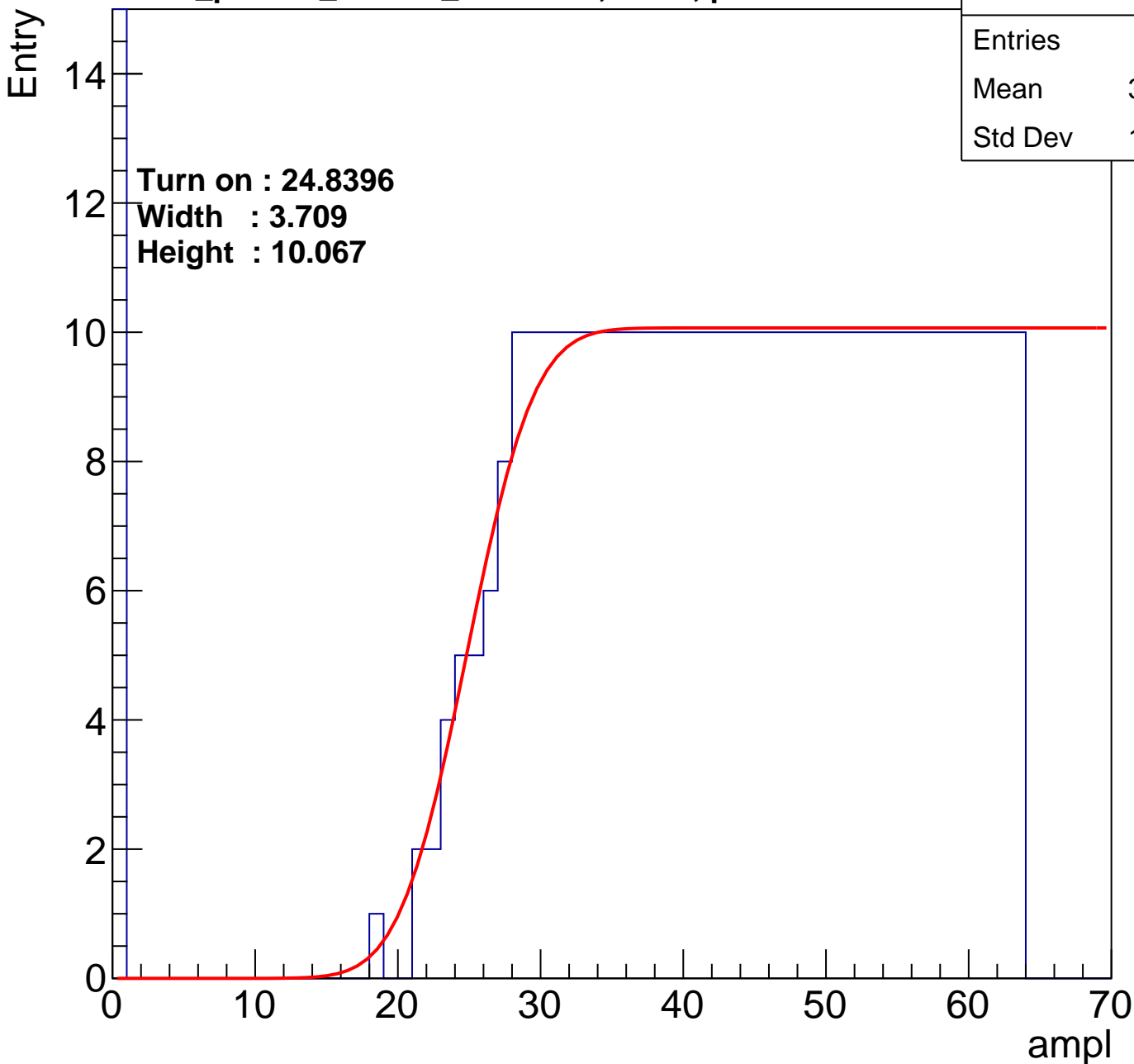
calib_packv5_041523_1651.root, FC#0, port C2

Entries	447
Mean	38.46
Std Dev	17.89

Turn on : 24.8396

Width : 3.709

Height : 10.067



B1L103S, U18-ch71

calib_packv5_041523_1651.root, FC#0, port C2

Entries	408
Mean	40.33
Std Dev	17.26

Turn on : 27.7347

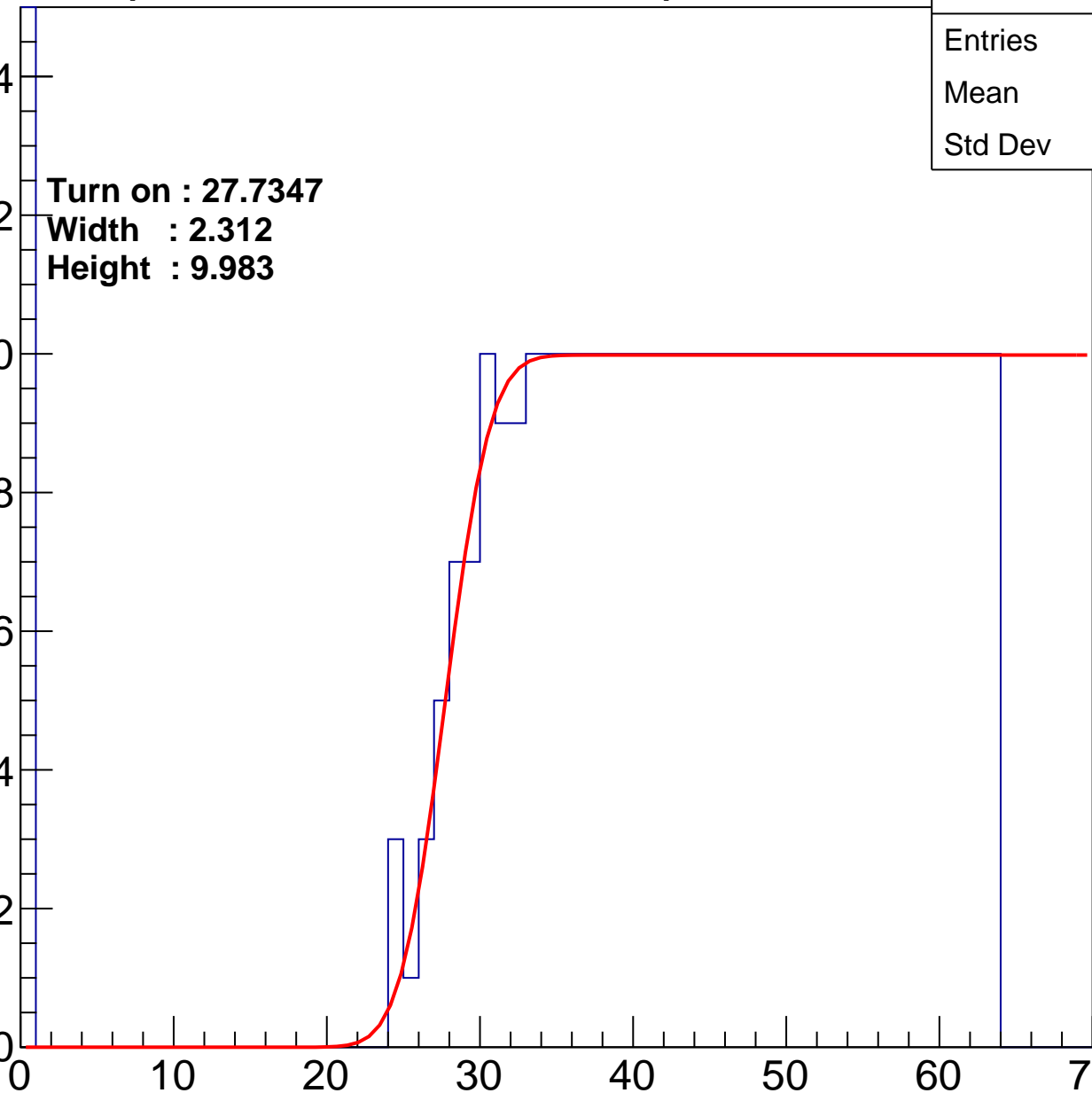
Width : 2.312

Height : 9.983

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U18-ch72

calib_packv5_041523_1651.root, FC#0, port C2

Entries	435
Mean	39.12
Std Dev	17.56

Turn on : 25.6259

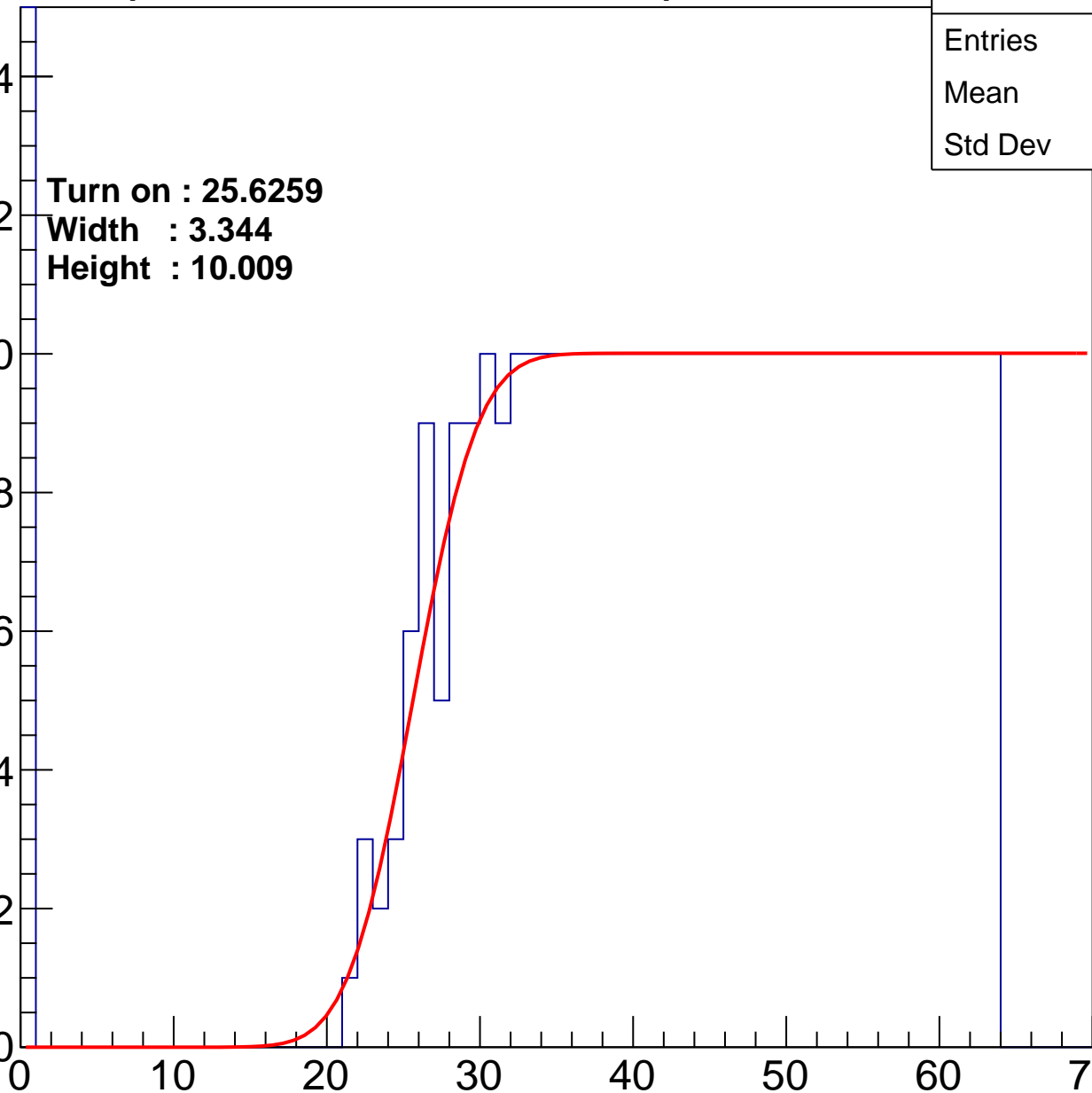
Width : 3.344

Height : 10.009

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U18-ch73

calib_packv5_041523_1651.root, FC#0, port C2

Entries	418
Mean	39.93
Std Dev	17.29

Turn on : 26.7552

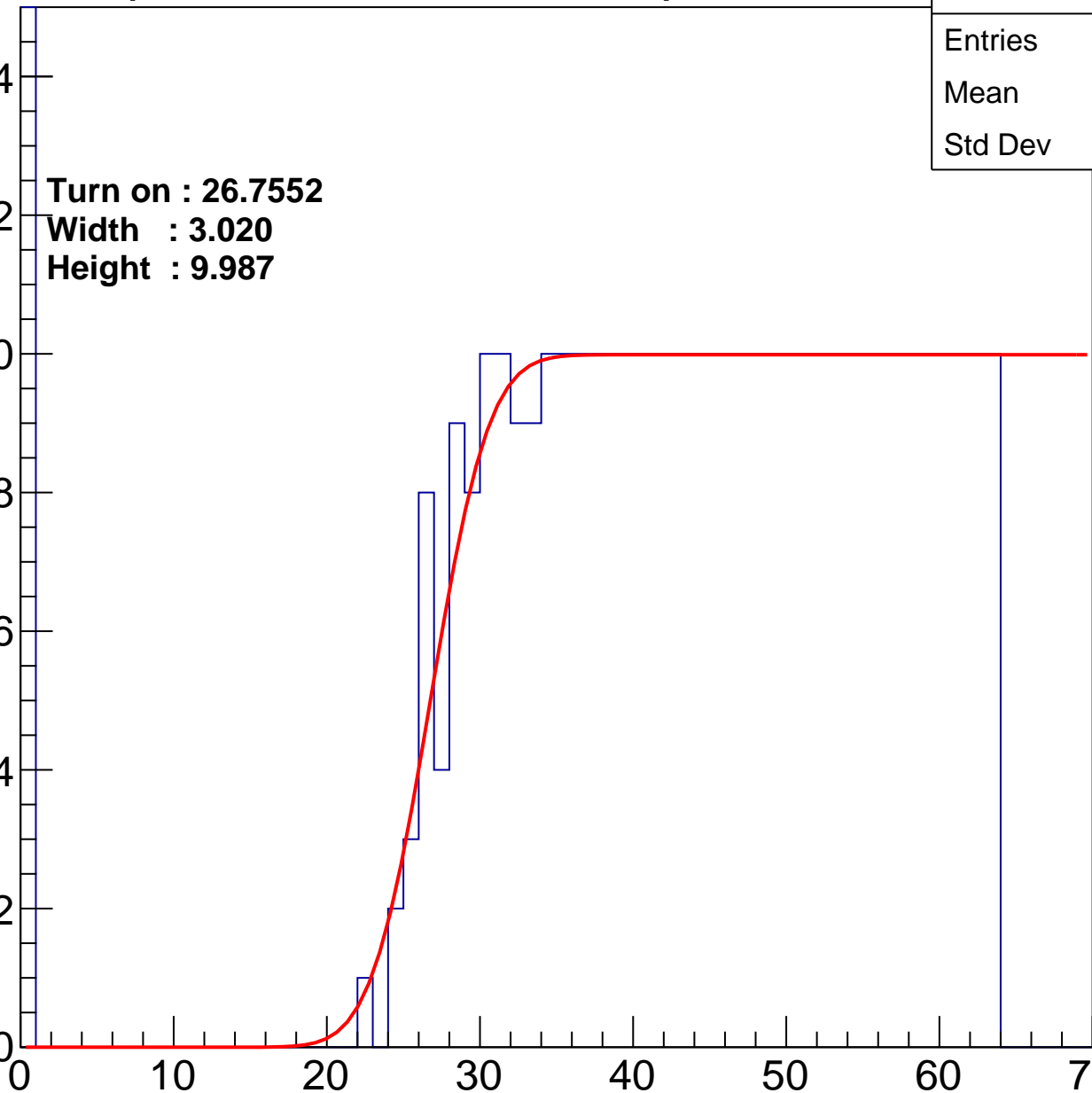
Width : 3.020

Height : 9.987

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U18-ch74

calib_packv5_041523_1651.root, FC#0, port C2

Entries	446
Mean	38.72
Std Dev	17.57

Turn on : 24.5947

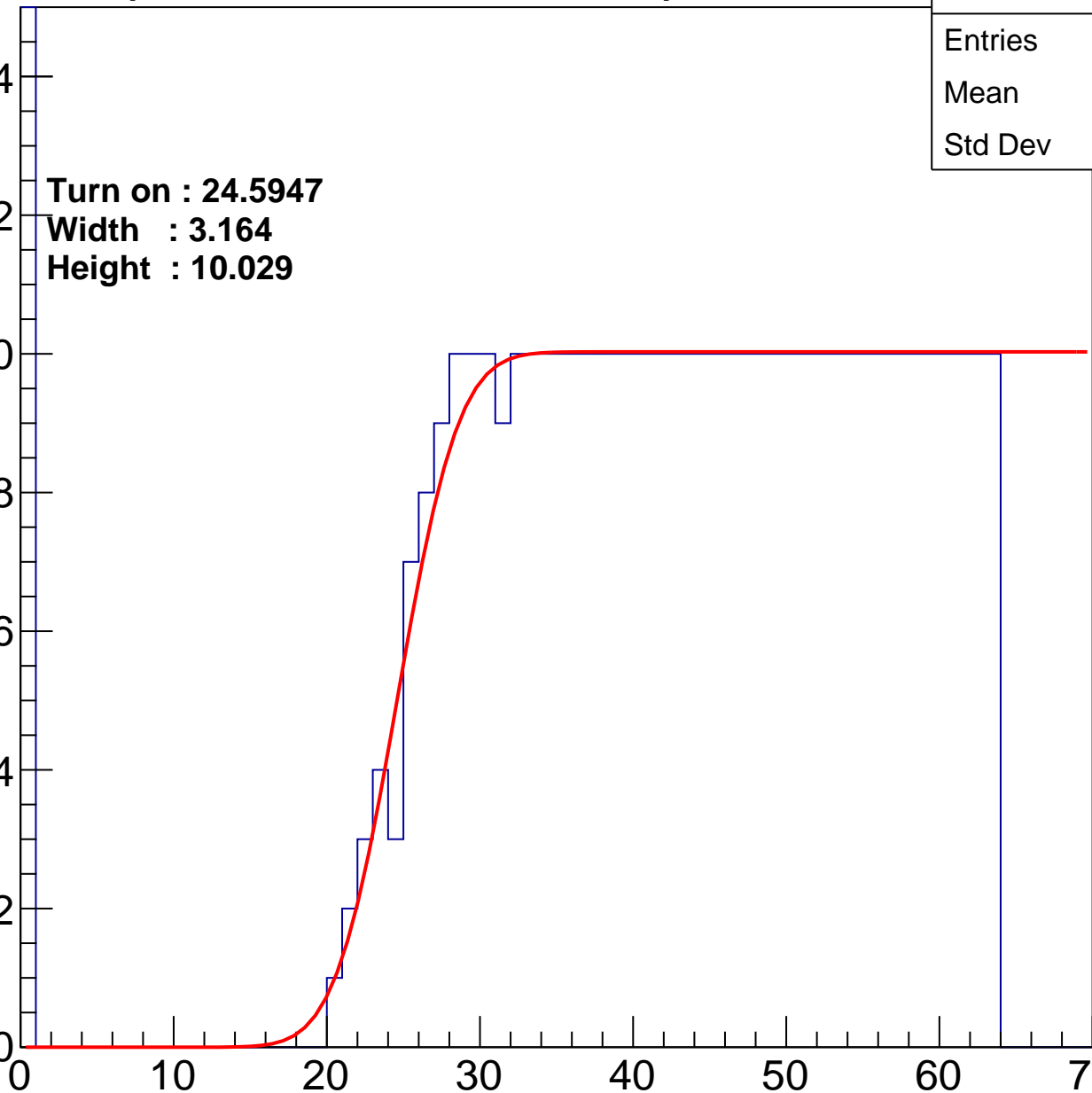
Width : 3.164

Height : 10.029

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U18-ch75

calib_packv5_041523_1651.root, FC#0, port C2

Entries	412
Mean	40.39
Std Dev	16.88

Turn on : 27.0438

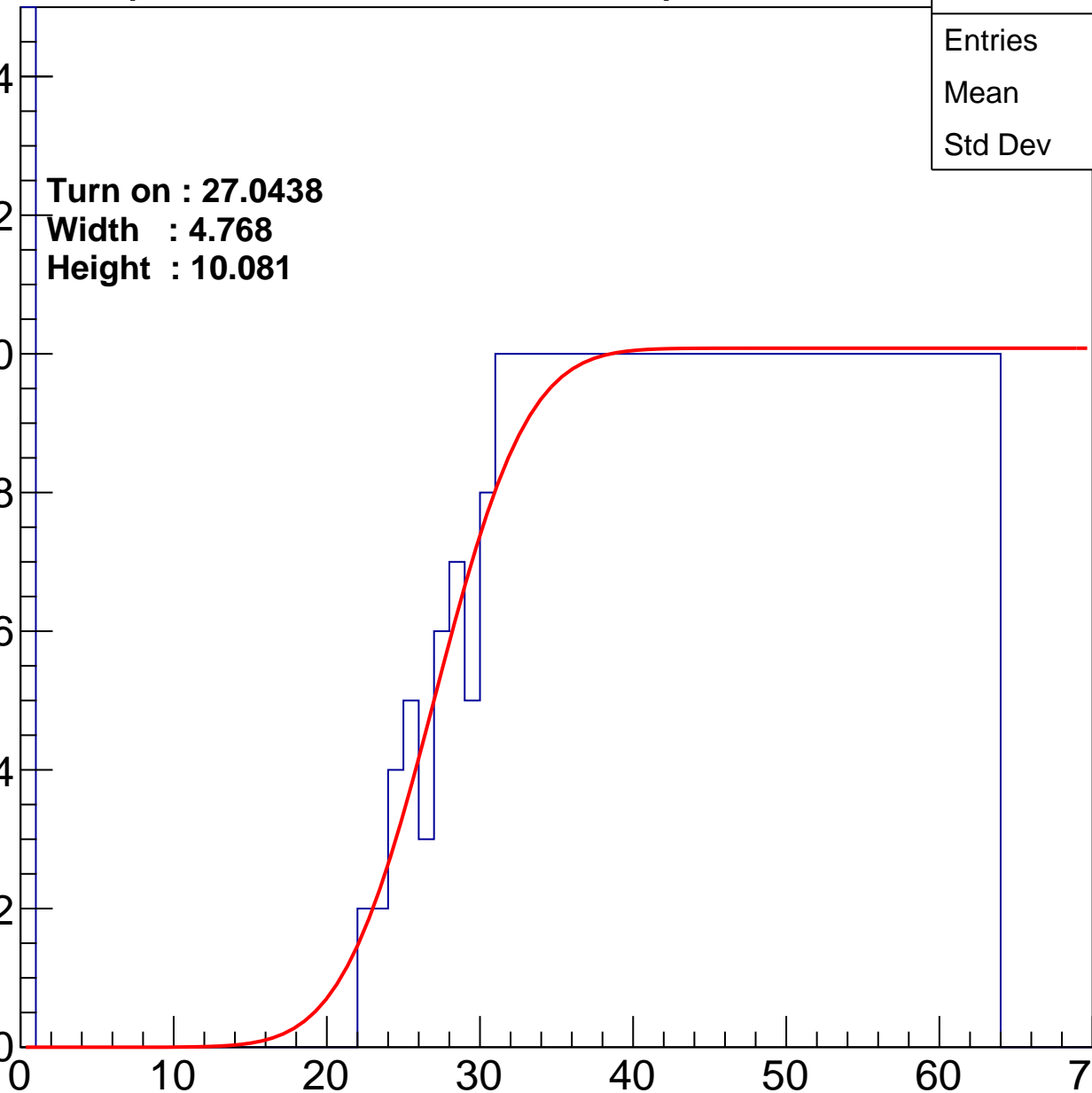
Width : 4.768

Height : 10.081

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U18-ch76

calib_packv5_041523_1651.root, FC#0, port C2

Entries	435
Mean	39.11
Std Dev	17.56

Turn on : 25.3426

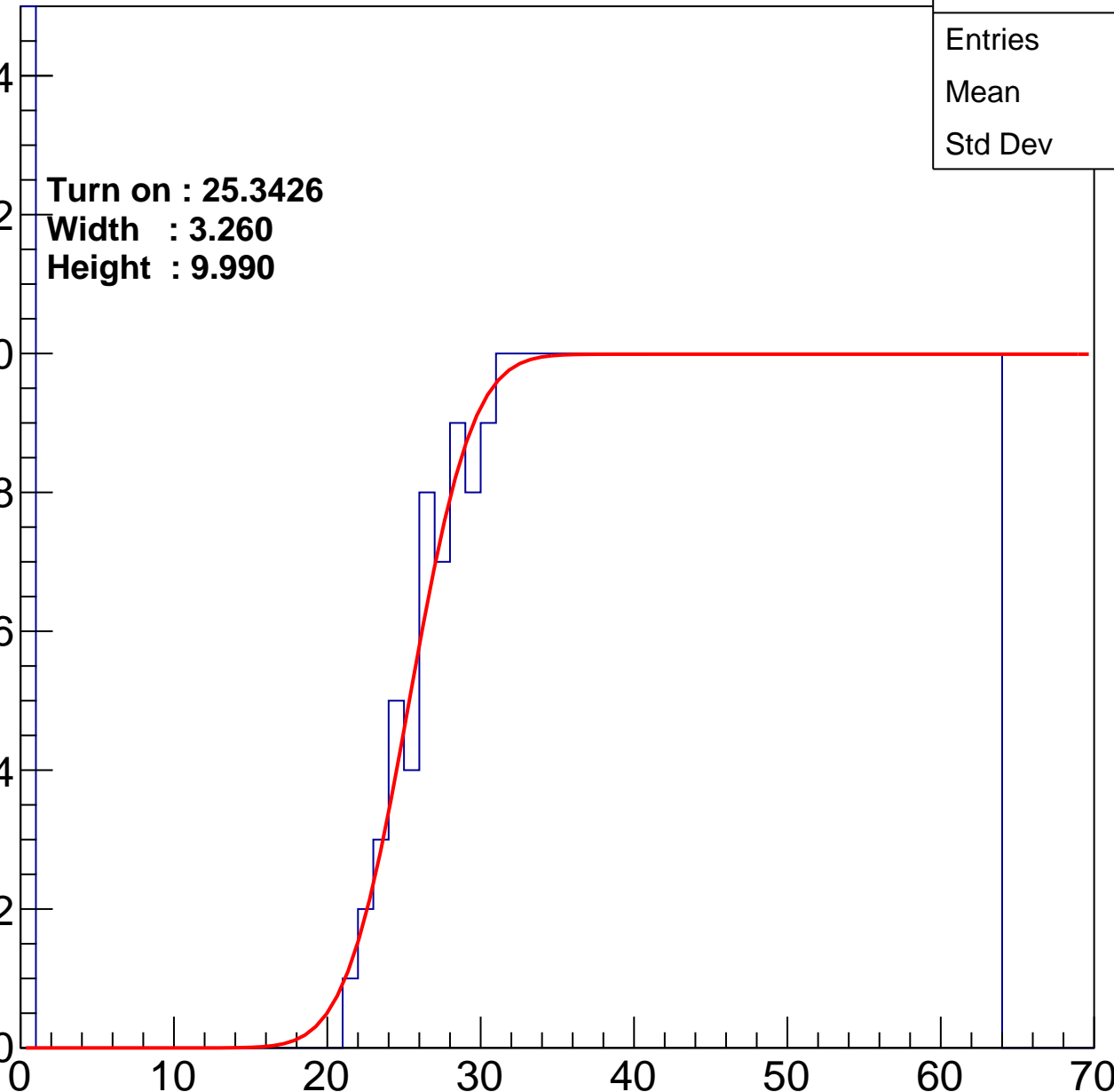
Width : 3.260

Height : 9.990

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U18-ch77

calib_packv5_041523_1651.root, FC#0, port C2

Entries	443
Mean	38.51
Std Dev	18.01

Turn on : 25.6042

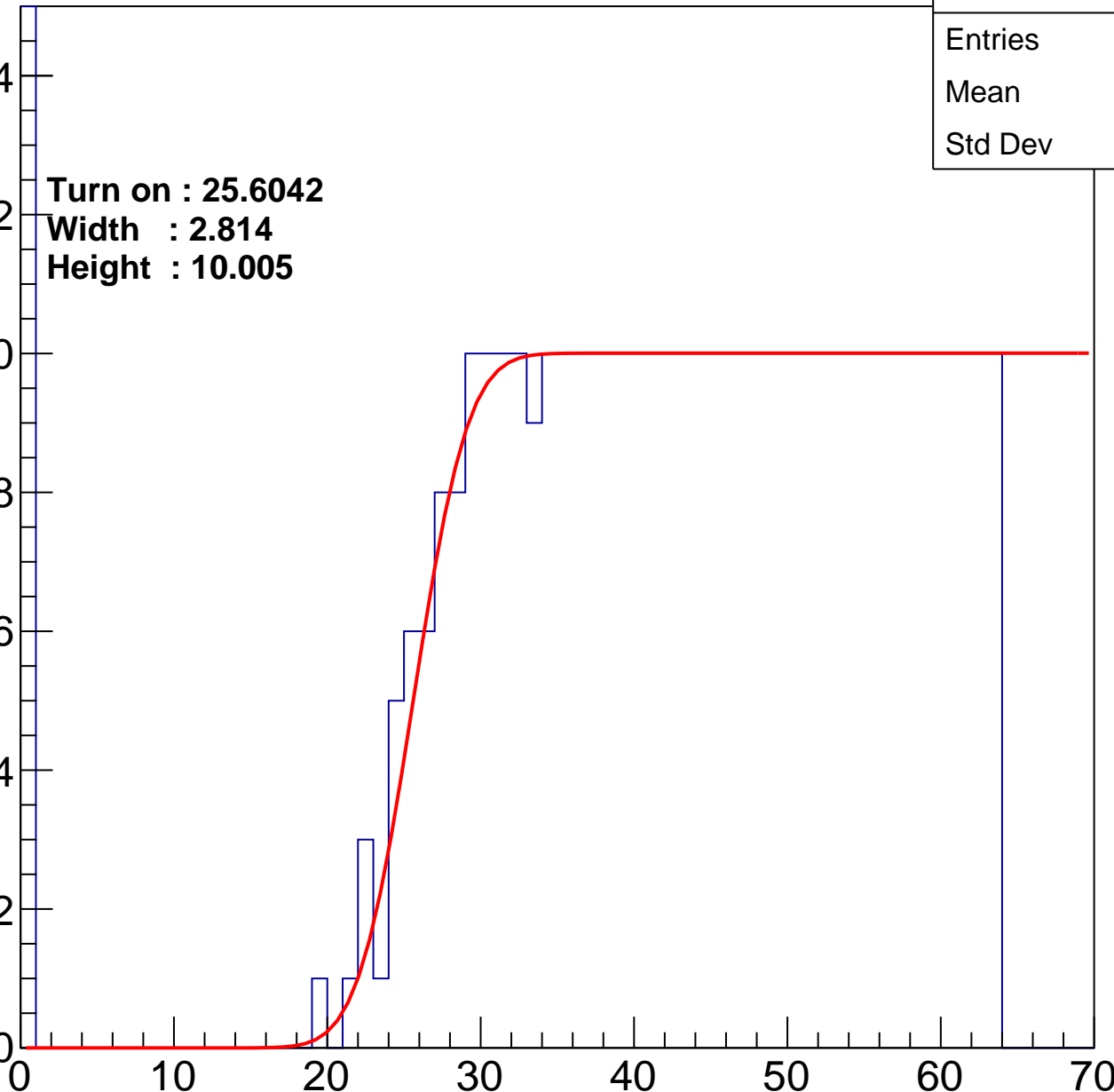
Width : 2.814

Height : 10.005

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U18-ch78

calib_packv5_041523_1651.root, FC#0, port C2

Entries	465
Mean	38.32
Std Dev	17.09

Turn on : 22.8438

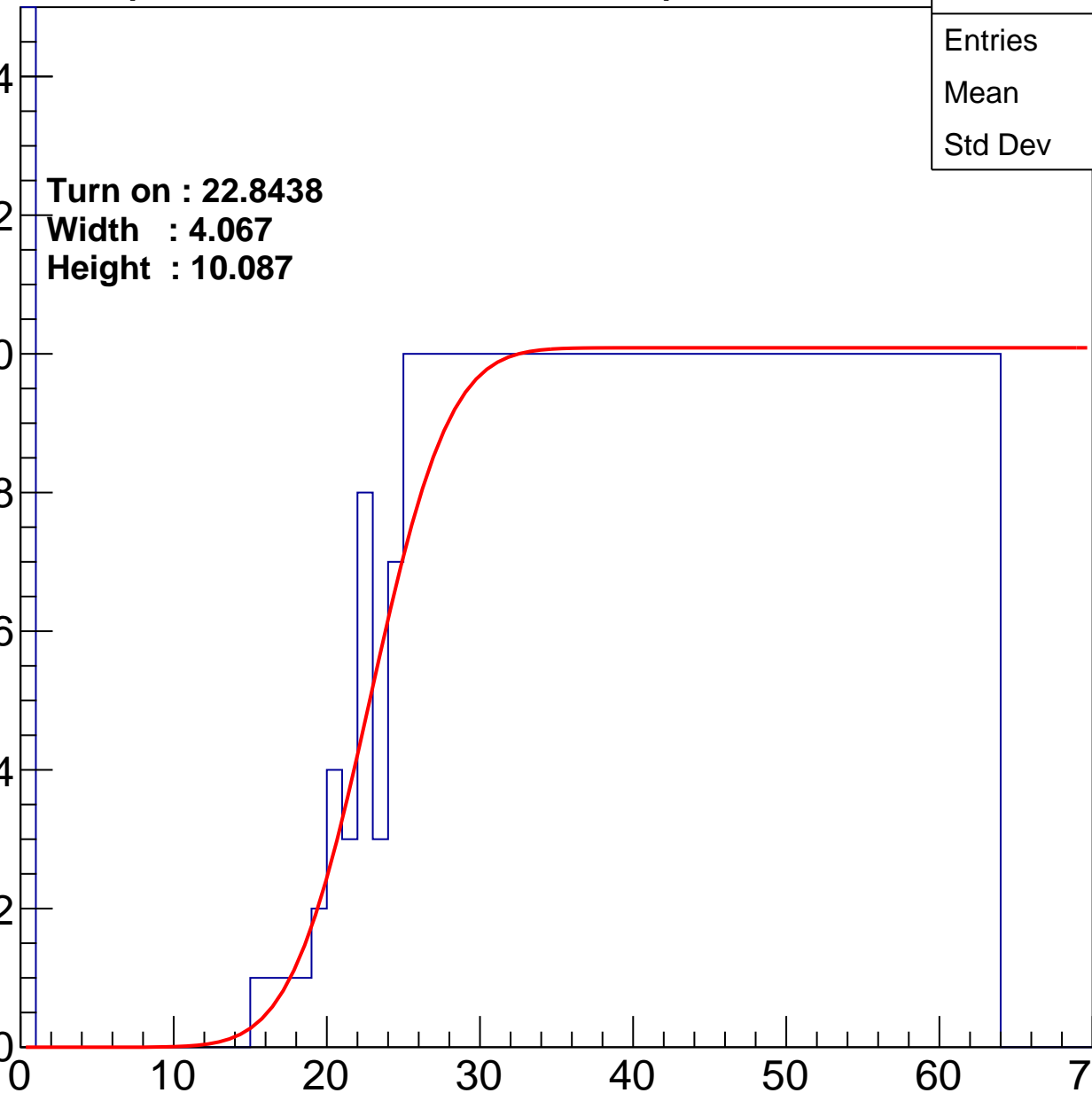
Width : 4.067

Height : 10.087

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U18-ch79

calib_packv5_041523_1651.root, FC#0, port C2

Entries	416
Mean	39.67
Std Dev	17.8

Turn on : 28.3021

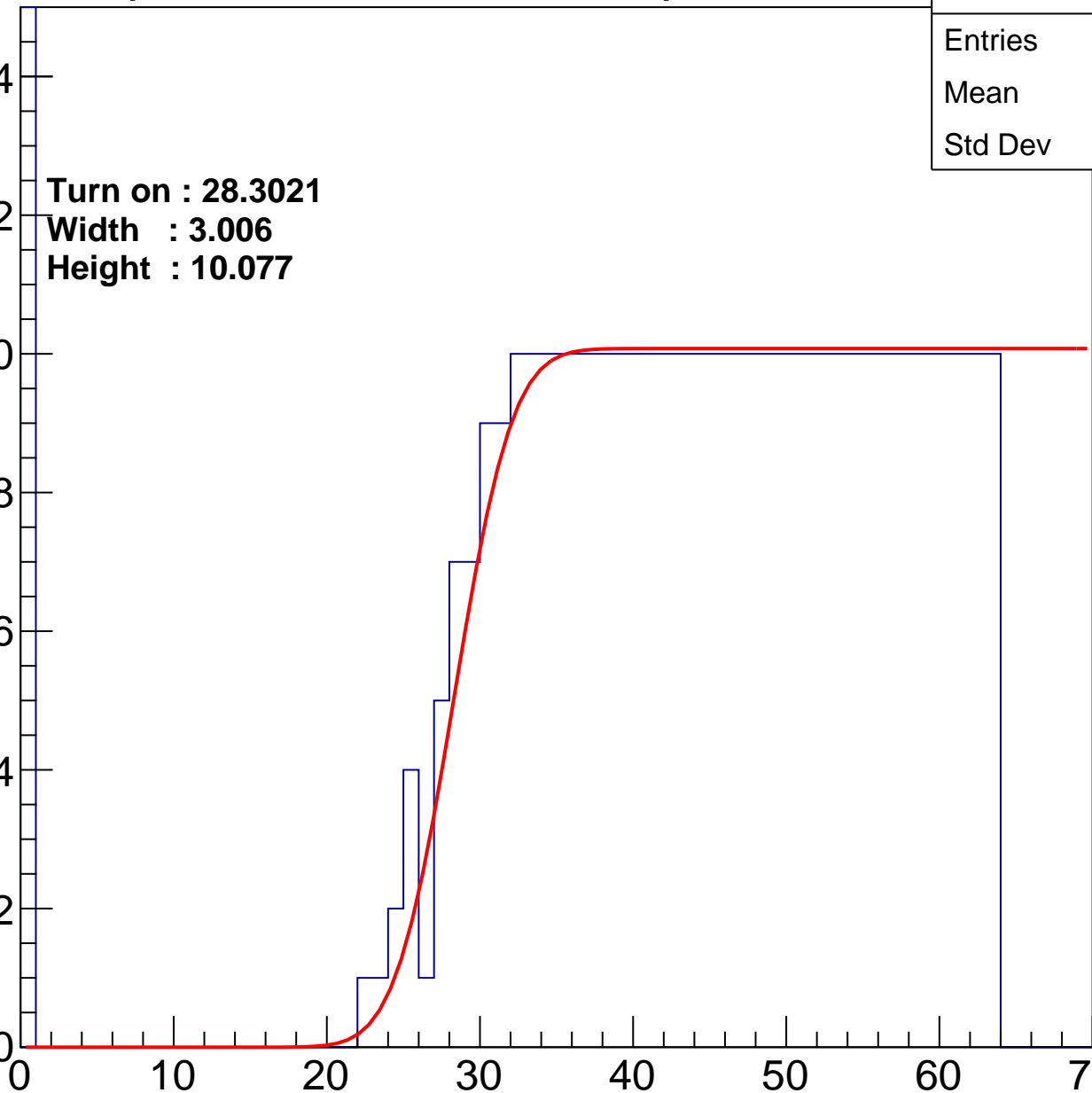
Width : 3.006

Height : 10.077

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U18-ch80

calib_packv5_041523_1651.root, FC#0, port C2

Entries	436
Mean	39.28
Std Dev	17.28

Turn on : 24.0831

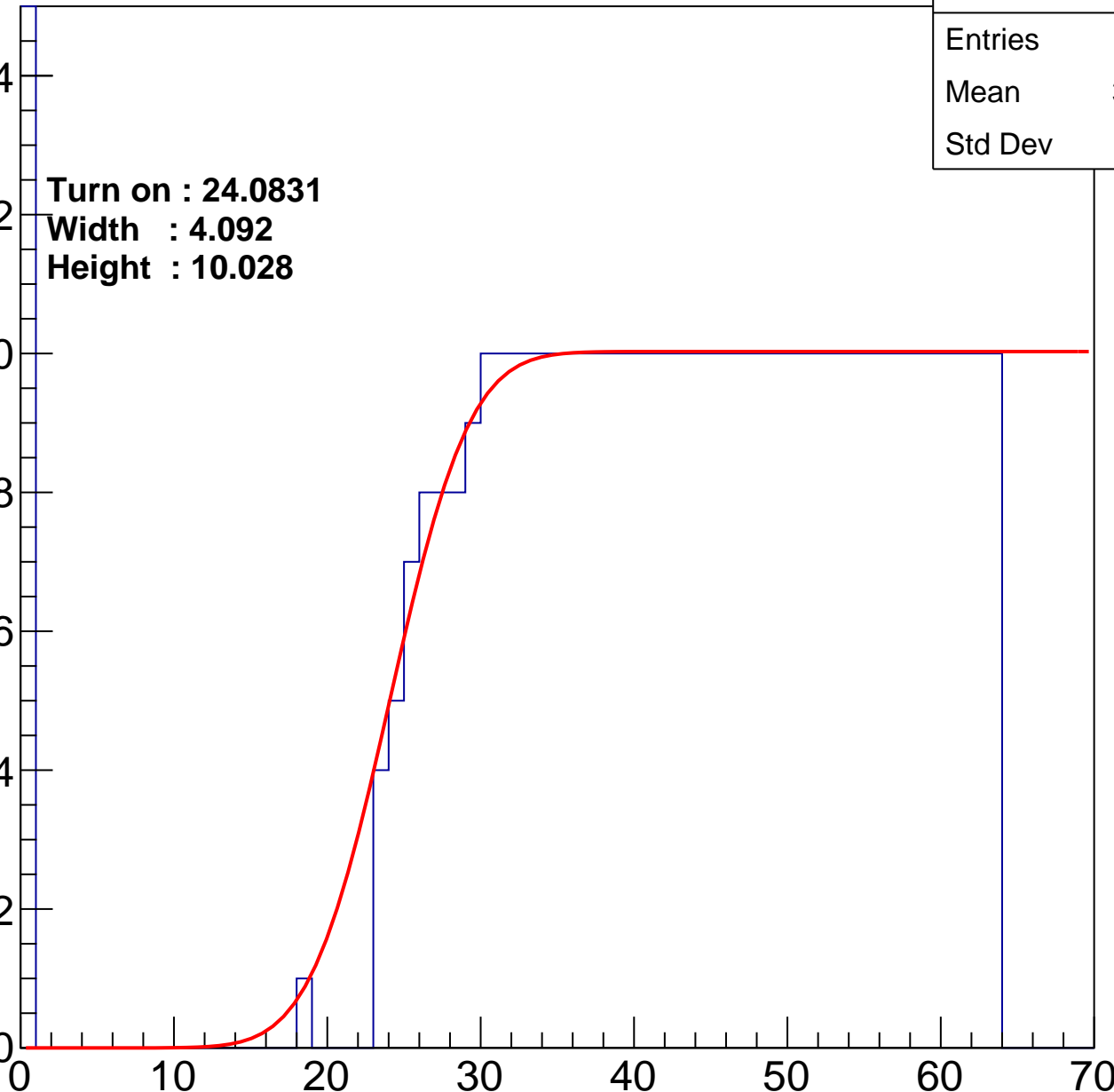
Width : 4.092

Height : 10.028

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U18-ch81

calib_packv5_041523_1651.root, FC#0, port C2

Entries	435
Mean	39.03
Std Dev	17.67

Turn on : 25.5300

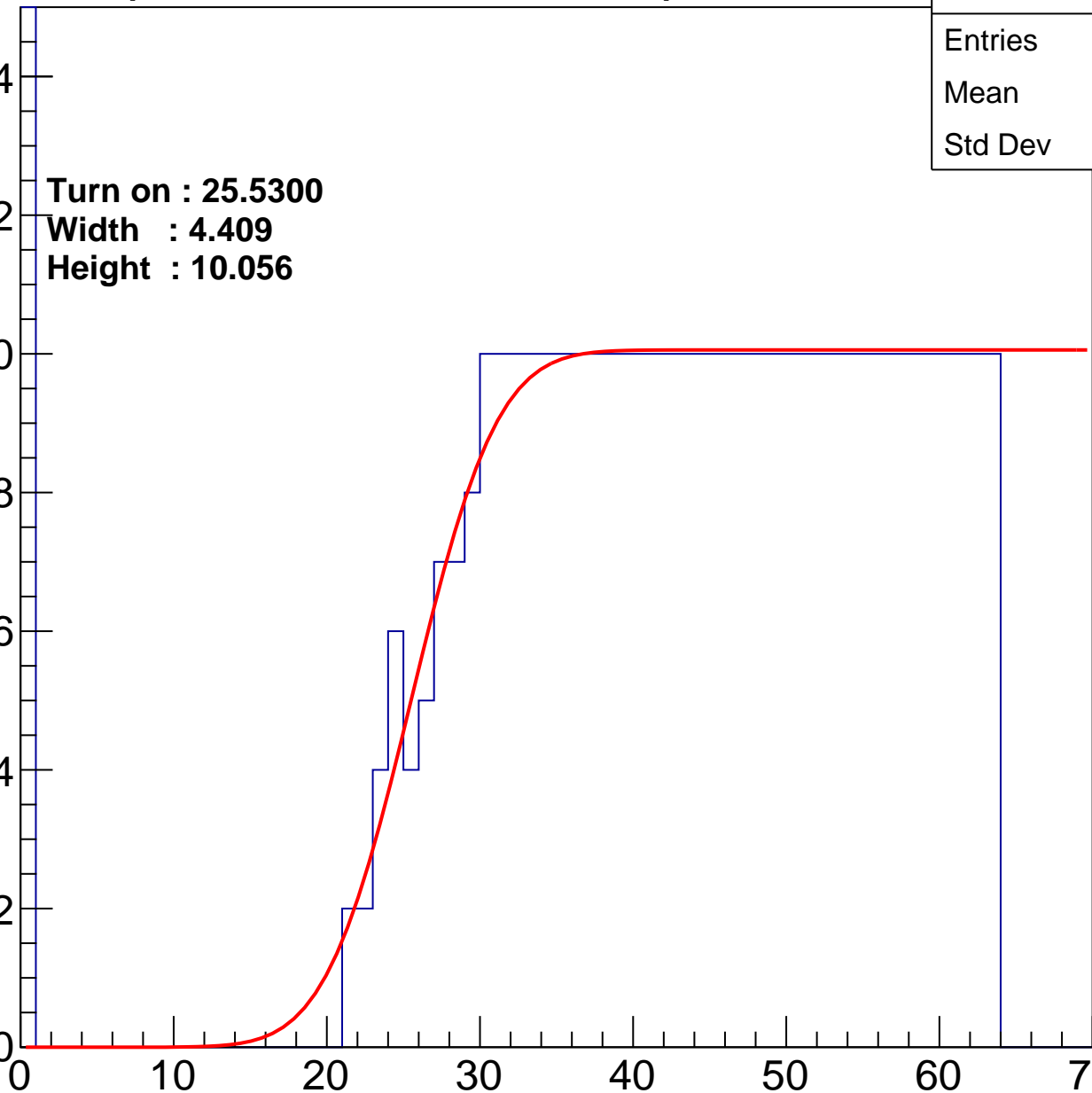
Width : 4.409

Height : 10.056

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U18-ch82

calib_packv5_041523_1651.root, FC#0, port C2

Entries	570
Mean	31.03
Std Dev	21.46

Turn on : 23.9506

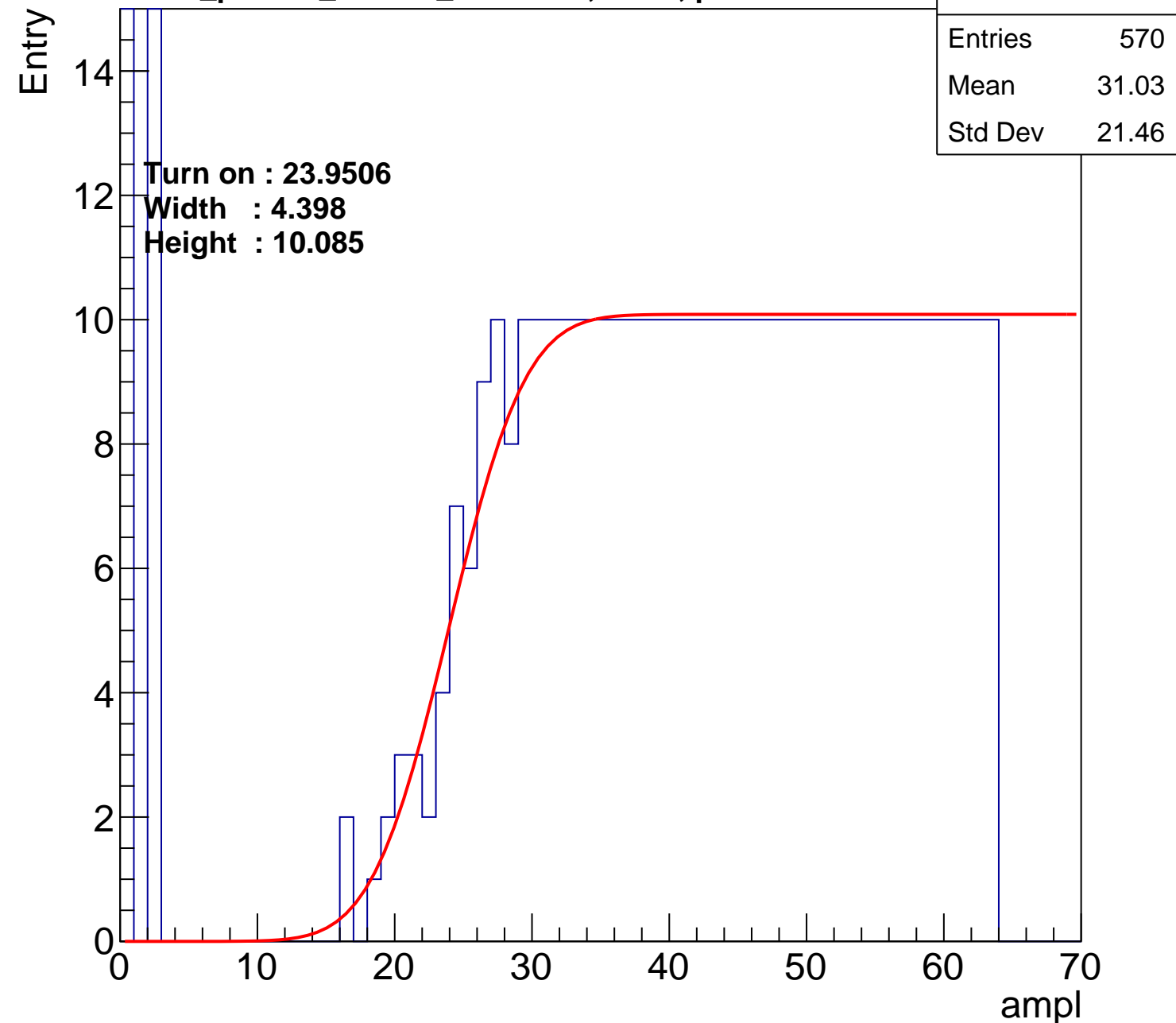
Width : 4.398

Height : 10.085

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U18-ch83

calib_packv5_041523_1651.root, FC#0, port C2

Entries	434
Mean	38.77
Std Dev	18.14

Turn on : 25.9880

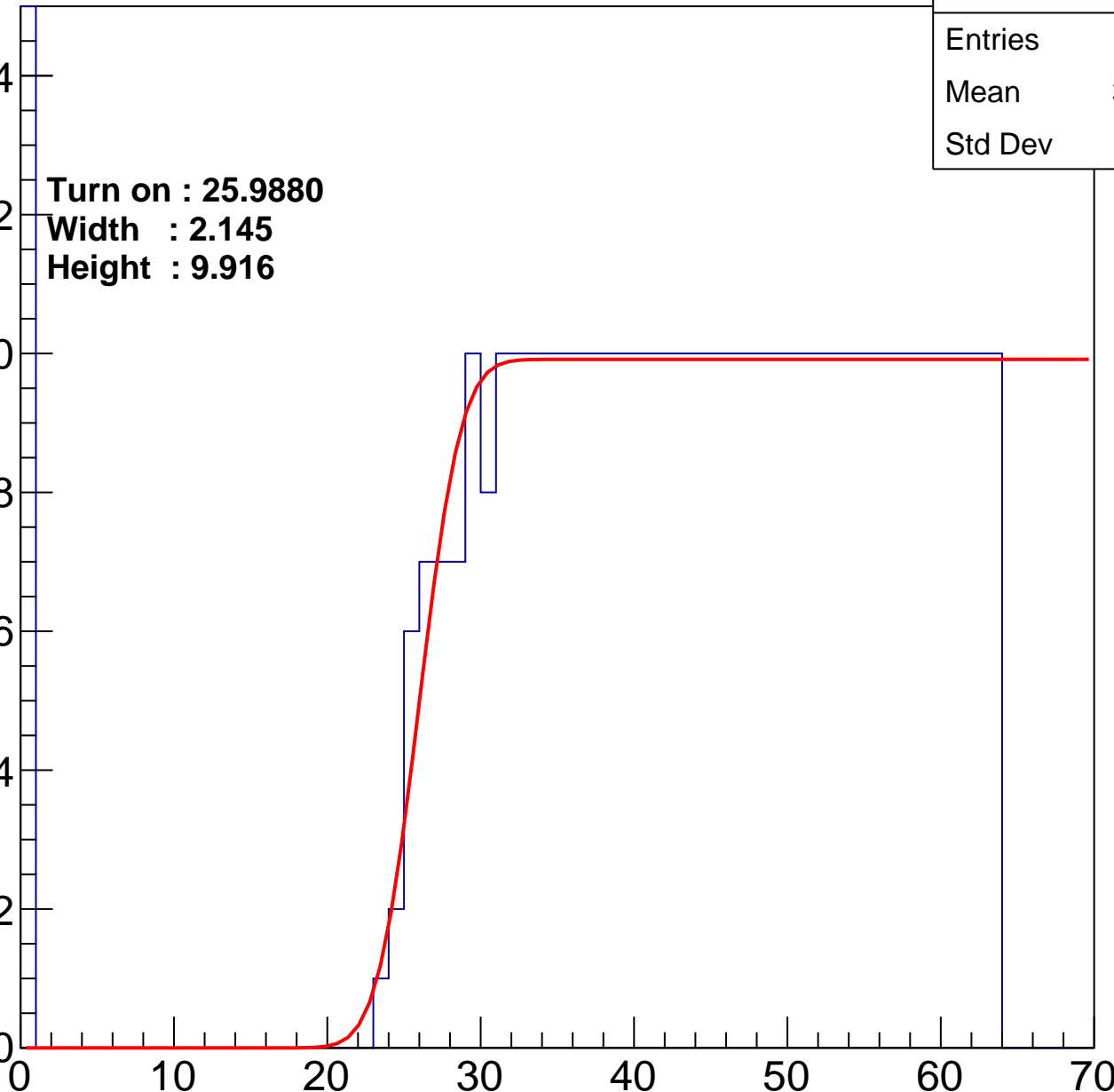
Width : 2.145

Height : 9.916

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U18-ch84

calib_packv5_041523_1651.root, FC#0, port C2

Entries	419
Mean	39.95
Std Dev	17.16

Turn on : 26.8218

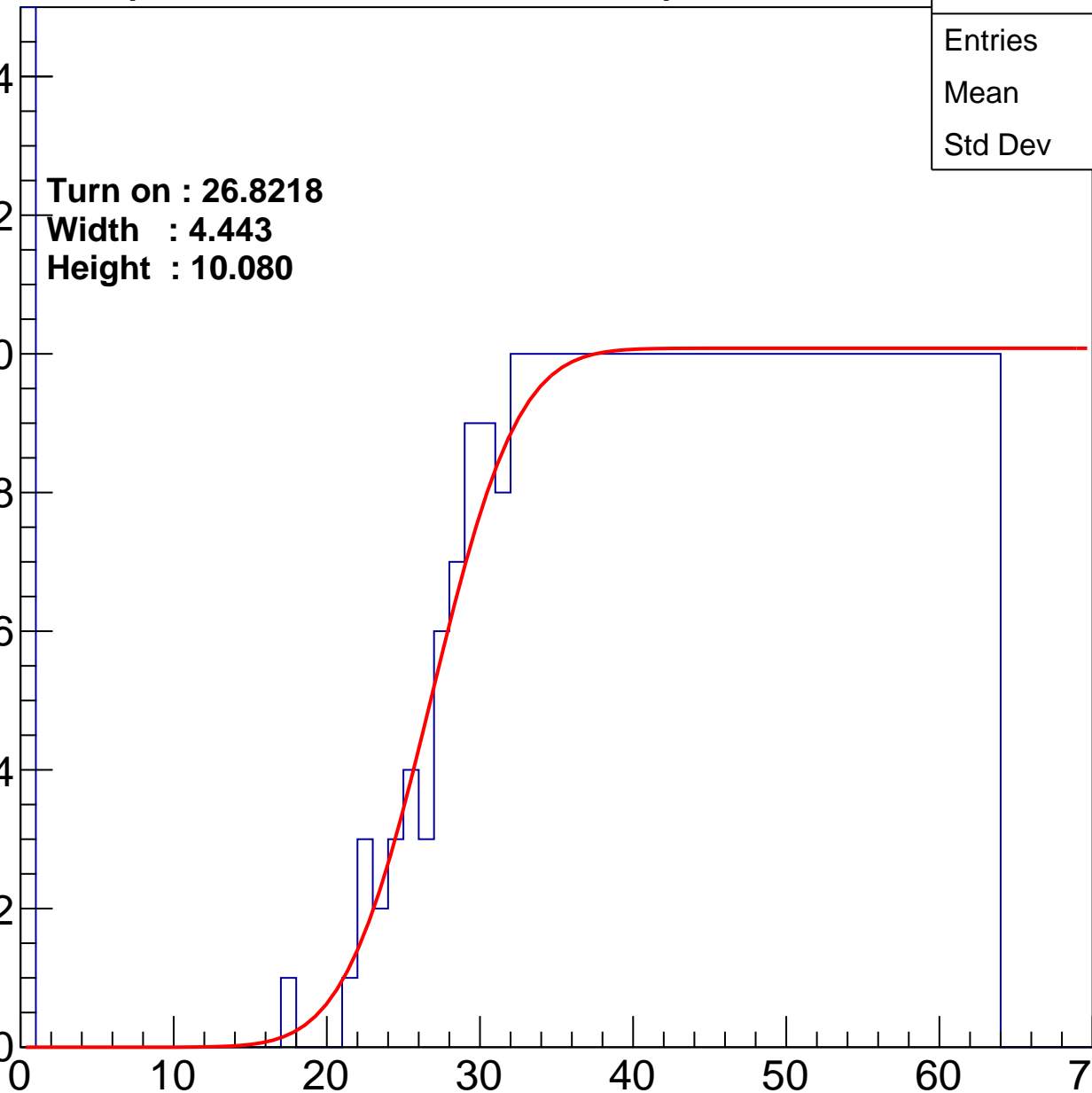
Width : 4.443

Height : 10.080

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U18-ch85

calib_packv5_041523_1651.root, FC#0, port C2

Entries	419
Mean	39.11
Std Dev	18.42

Turn on : 28.2056

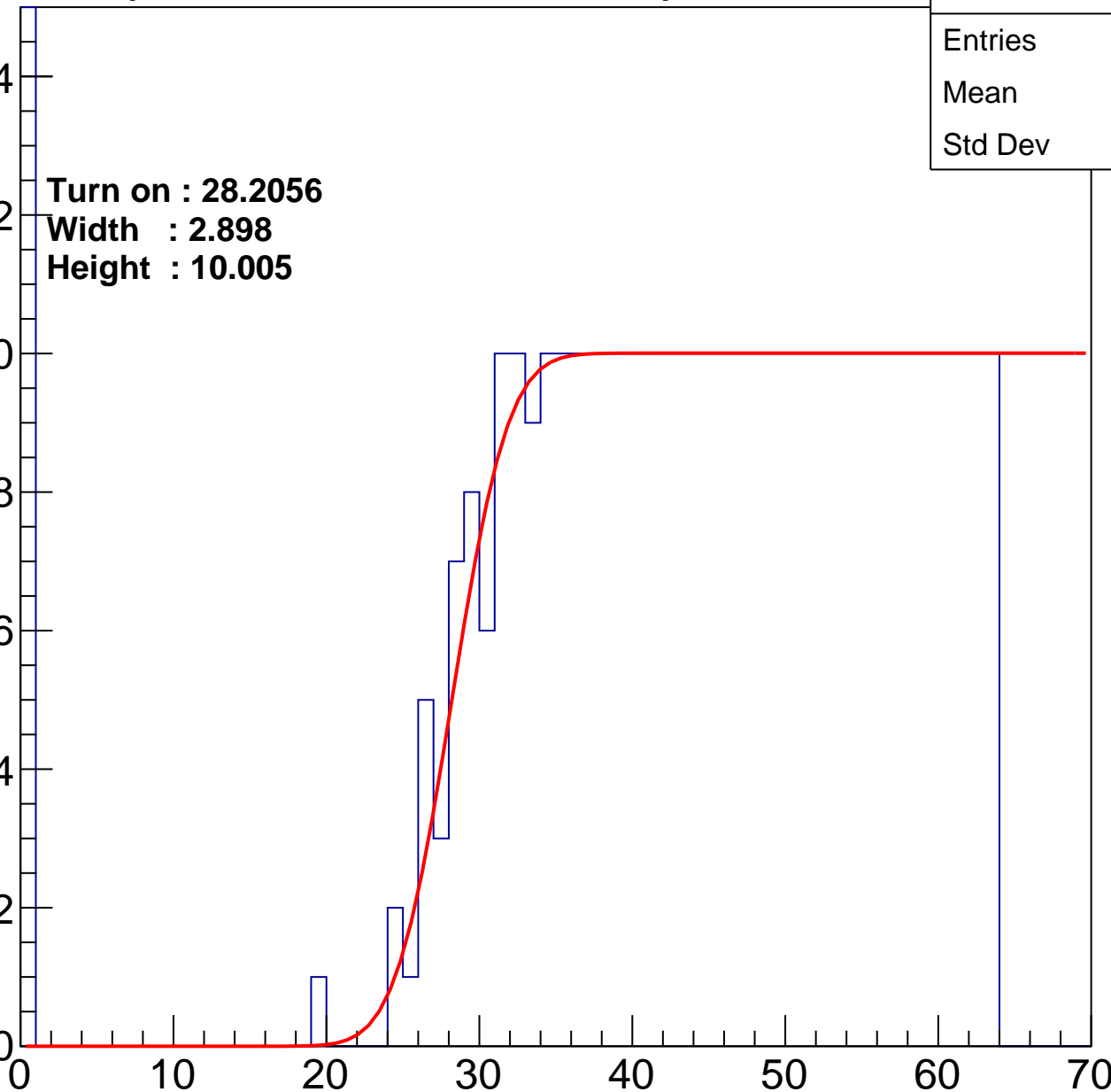
Width : 2.898

Height : 10.005

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U18-ch86

calib_packv5_041523_1651.root, FC#0, port C2

Entries	439
Mean	38.1
Std Dev	18.74

Turn on : 27.1287

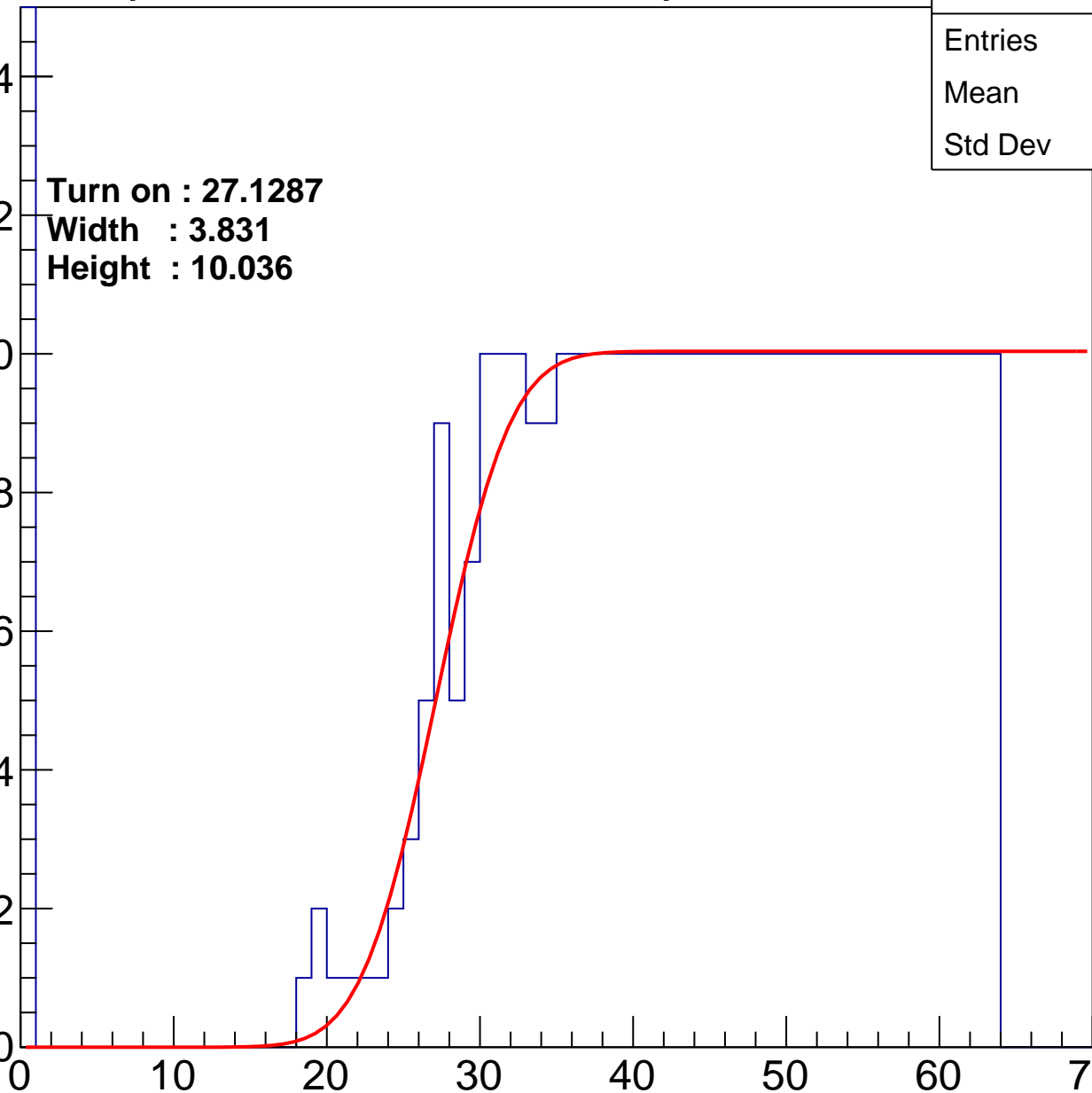
Width : 3.831

Height : 10.036

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U18-ch87

calib_packv5_041523_1651.root, FC#0, port C2

Entries	437
Mean	39.01
Std Dev	17.62

Turn on : 25.3849

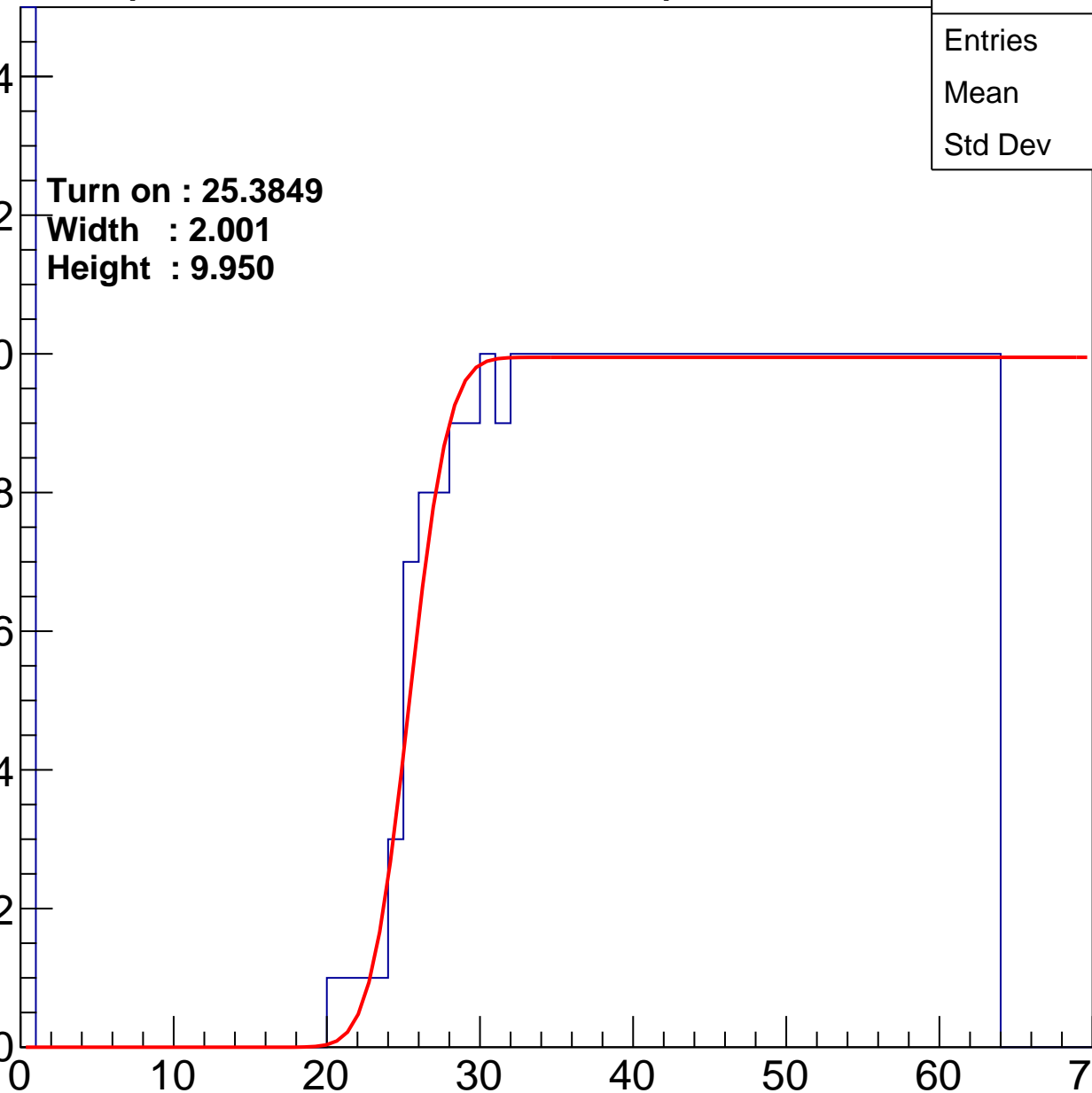
Width : 2.001

Height : 9.950

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U18-ch88

calib_packv5_041523_1651.root, FC#0, port C2

Entries	448
Mean	38.19
Std Dev	18.21

Turn on : 24.8120

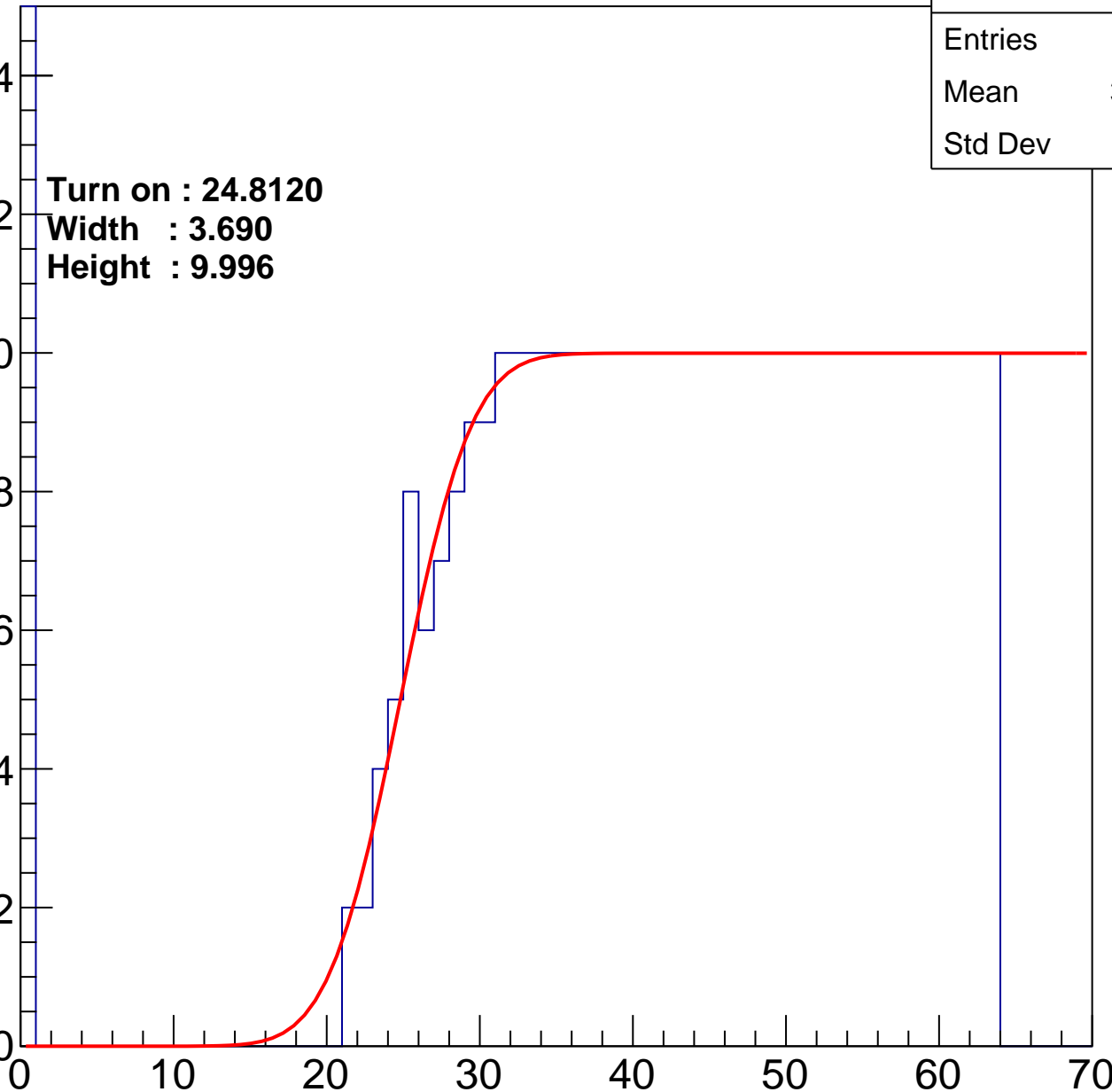
Width : 3.690

Height : 9.996

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U18-ch89

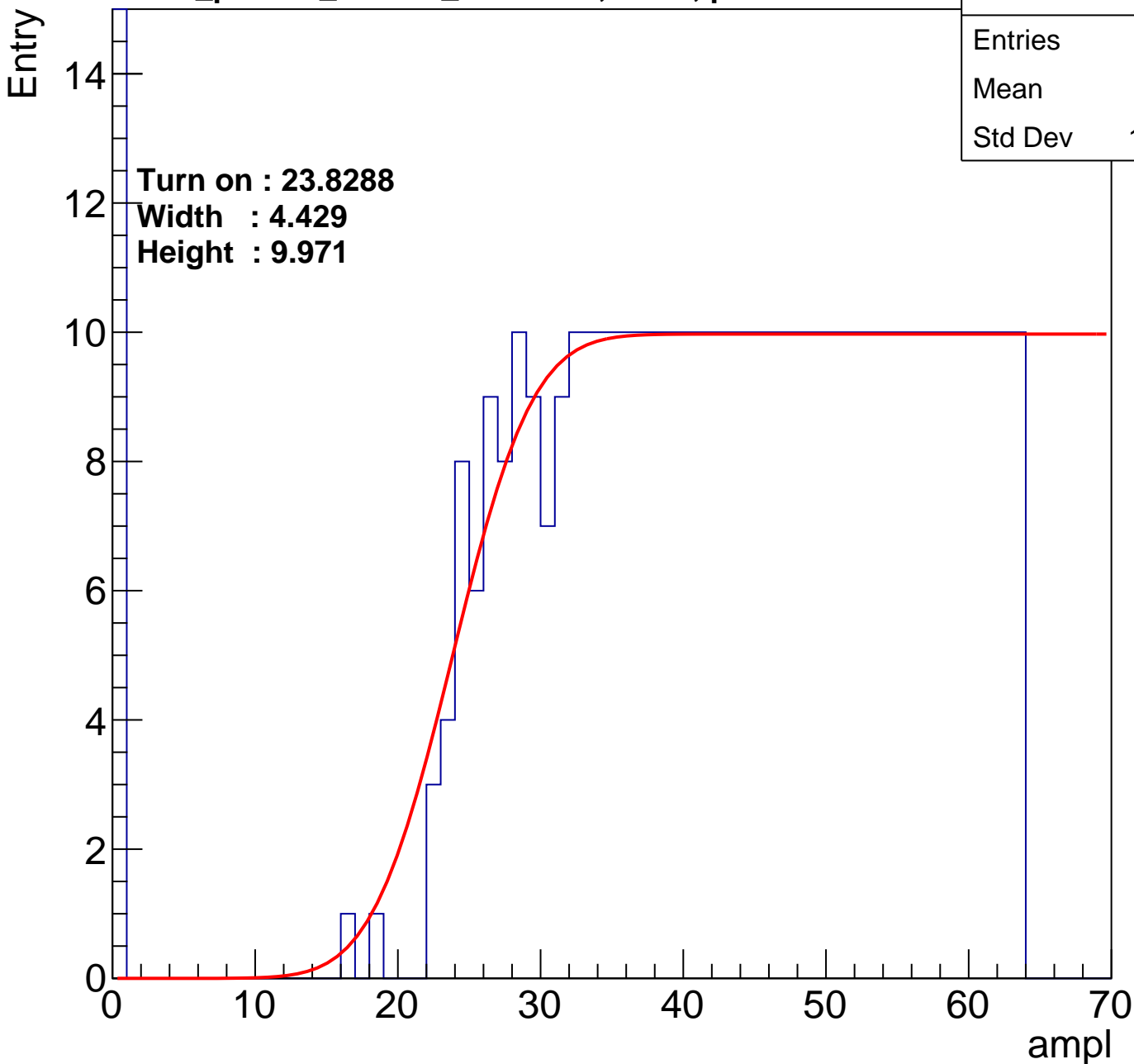
calib_packv5_041523_1651.root, FC#0, port C2

Entries	453
Mean	38
Std Dev	18.19

Turn on : 23.8288

Width : 4.429

Height : 9.971



B1L103S, U18-ch90

calib_packv5_041523_1651.root, FC#0, port C2

Entries	444
Mean	38.96
Std Dev	17.28

Turn on : 24.8629

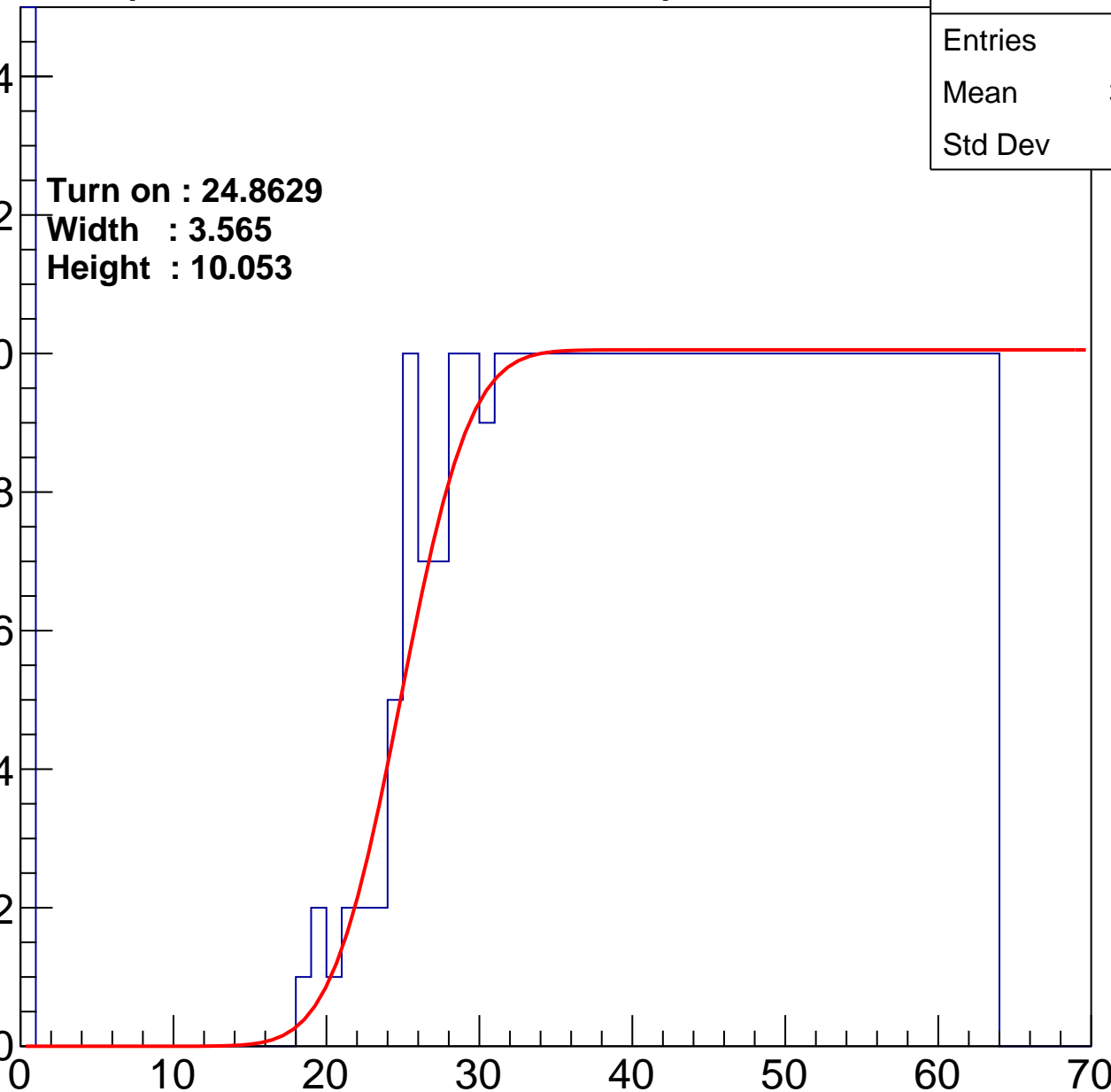
Width : 3.565

Height : 10.053

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U18-ch91

calib_packv5_041523_1651.root, FC#0, port C2

Entries	441
Mean	38.91
Std Dev	17.53

Turn on : 24.9604

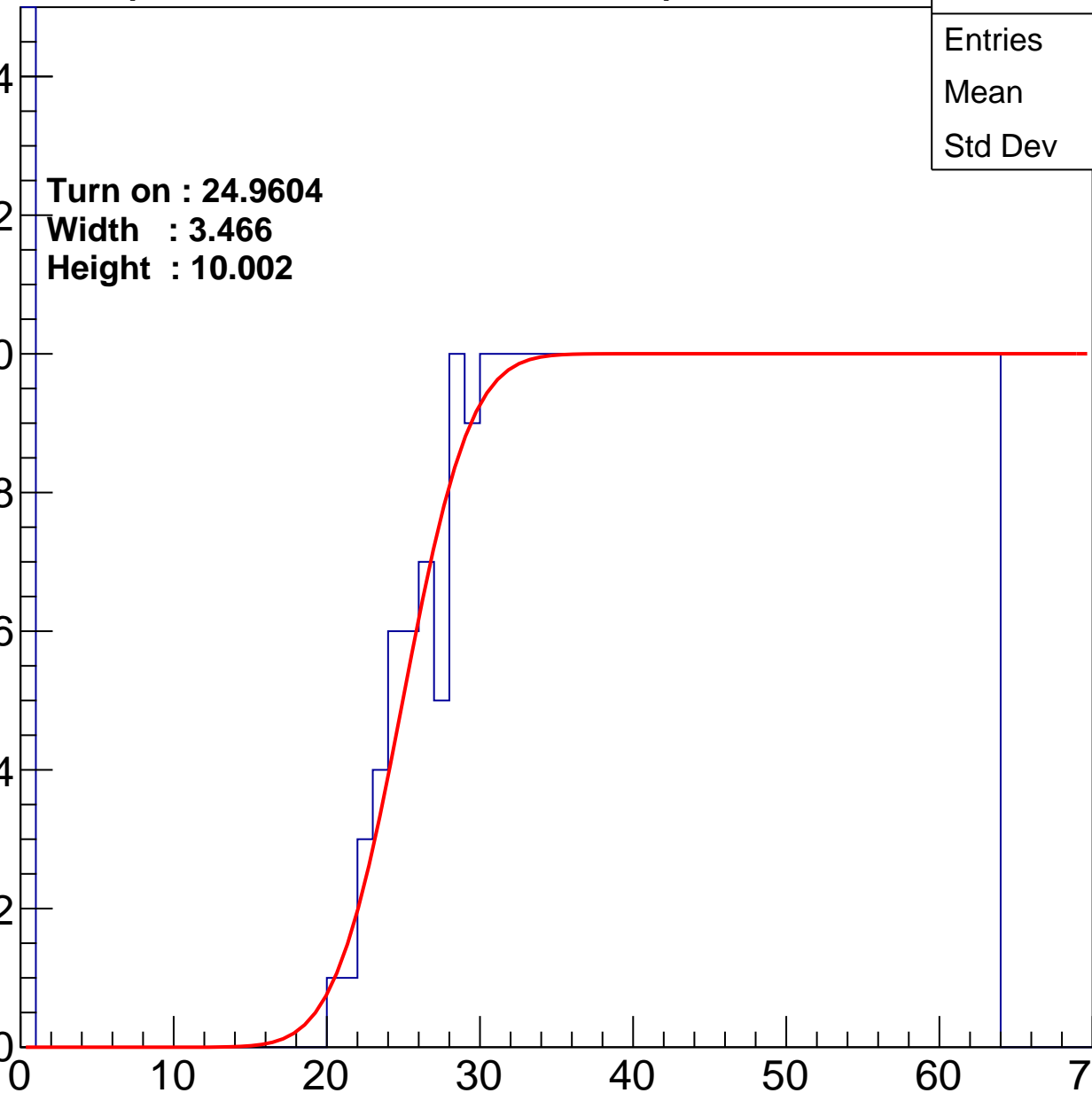
Width : 3.466

Height : 10.002

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U18-ch92

calib_packv5_041523_1651.root, FC#0, port C2

Entries	443
Mean	38.28
Std Dev	18.32

Turn on : 25.0390

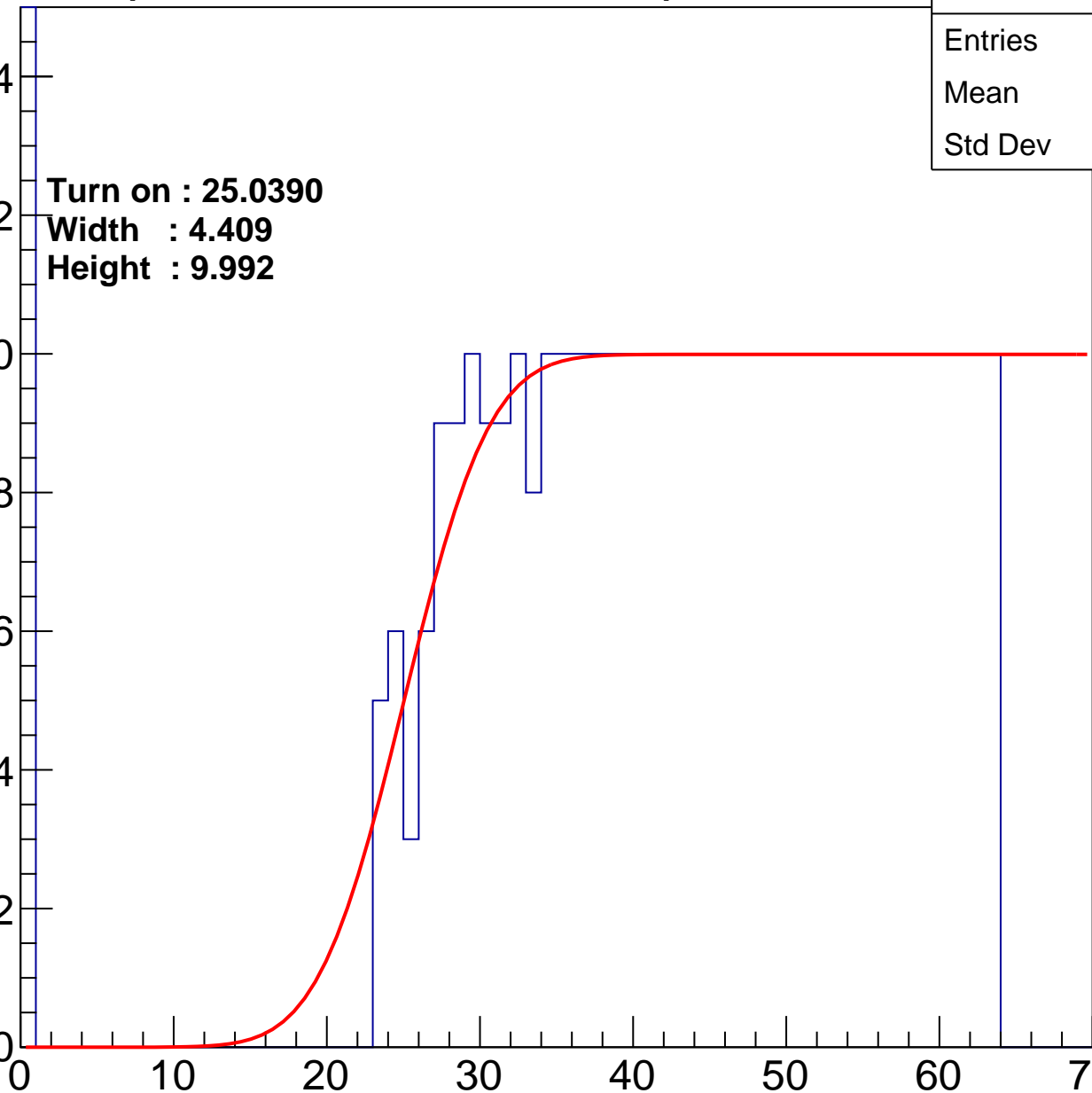
Width : 4.409

Height : 9.992

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U18-ch93

calib_packv5_041523_1651.root, FC#0, port C2

Entries	424
Mean	38.82
Std Dev	18.55

Turn on : 27.6215

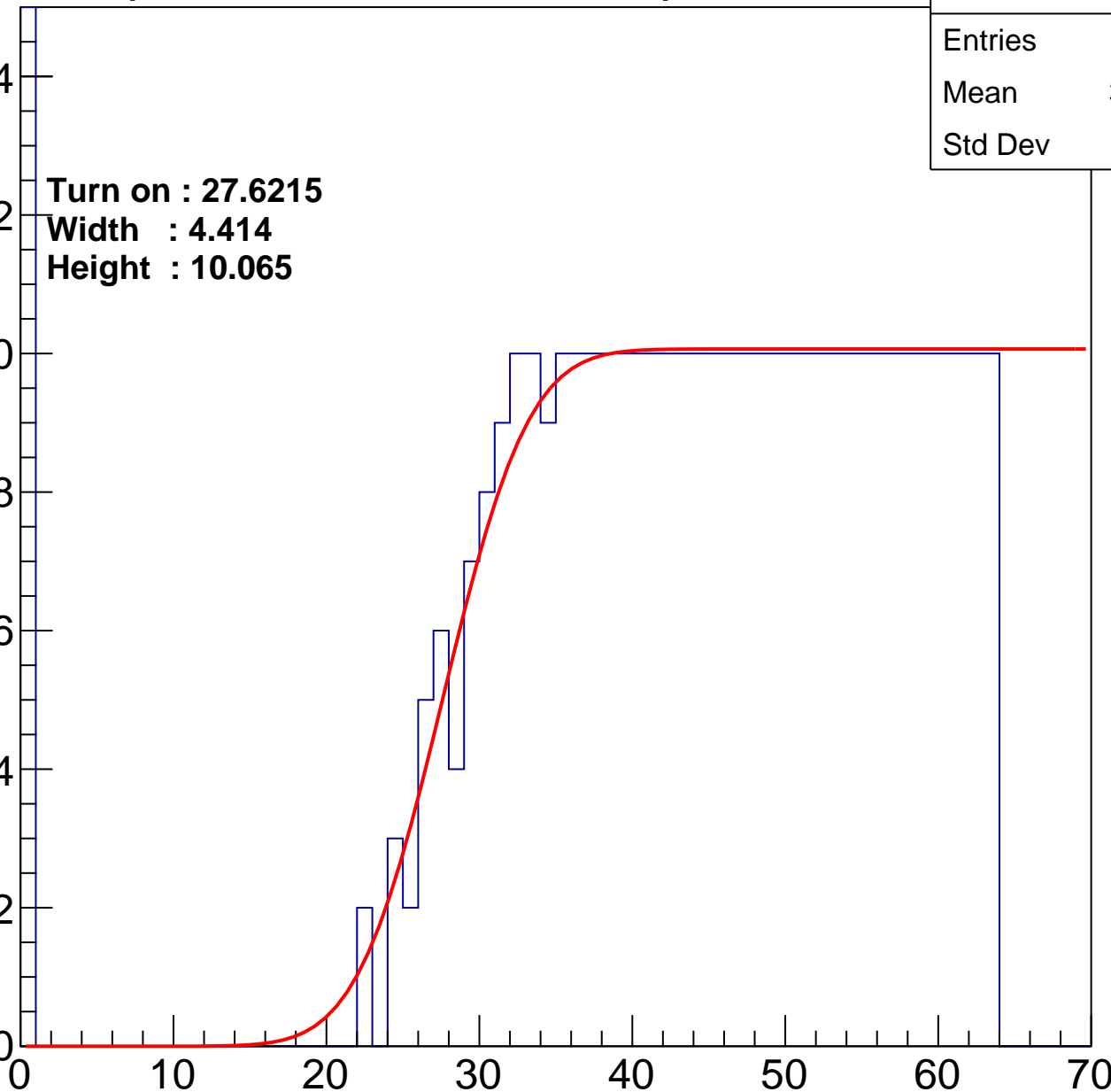
Width : 4.414

Height : 10.065

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U18-ch94

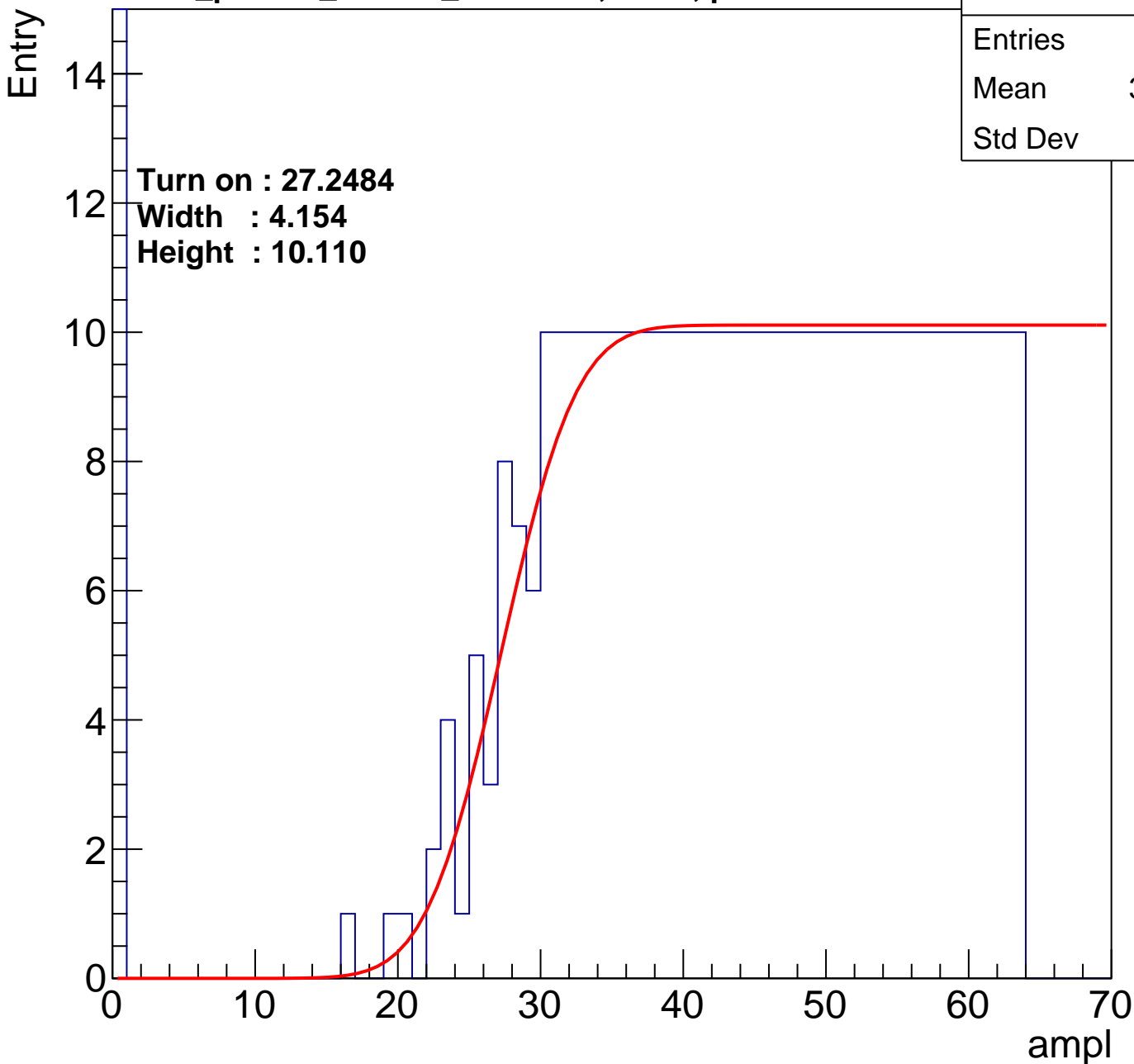
calib_packv5_041523_1651.root, FC#0, port C2

Entries	431
Mean	39.01
Std Dev	17.9

Turn on : 27.2484

Width : 4.154

Height : 10.110



B1L103S, U18-ch95

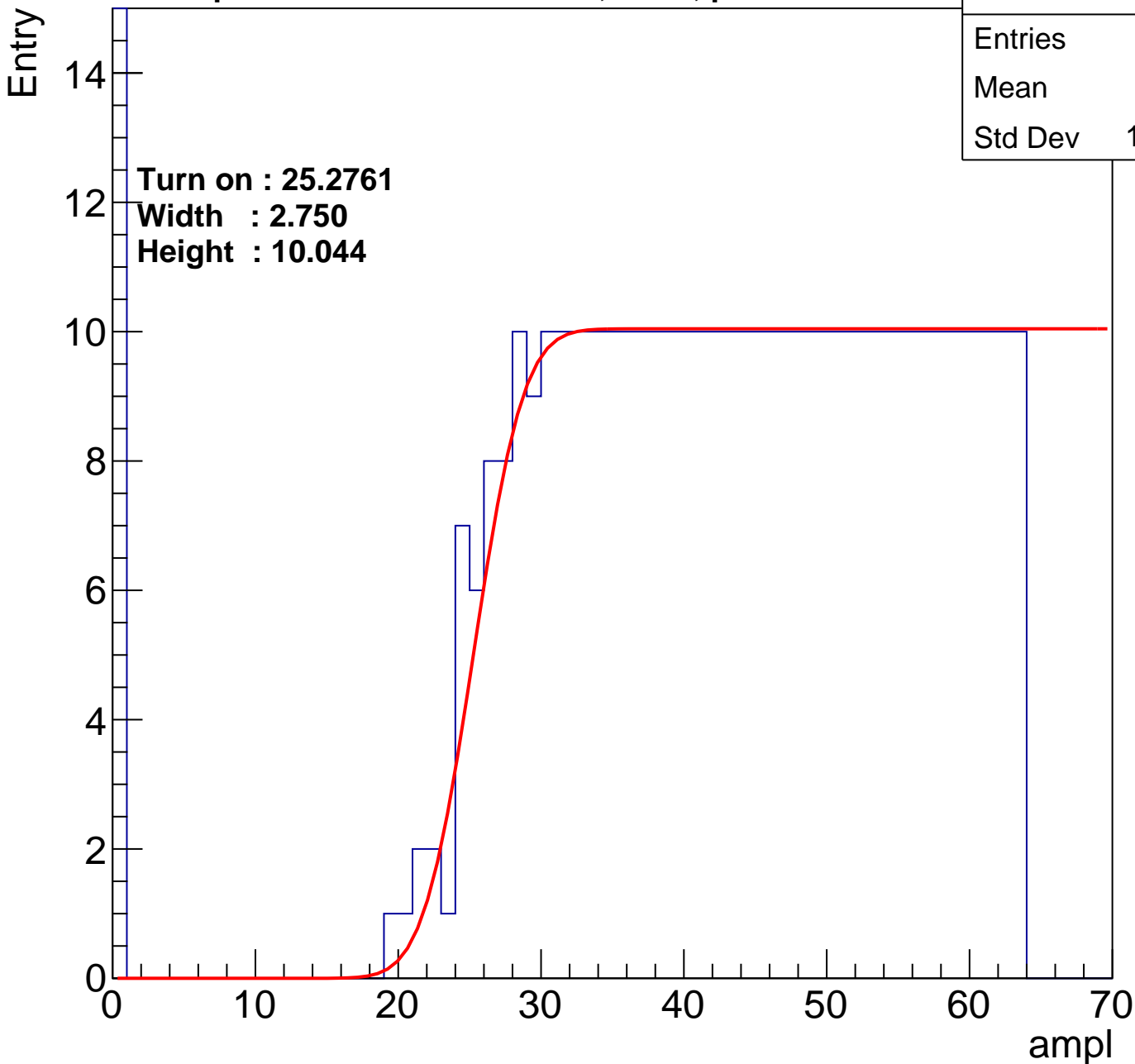
calib_packv5_041523_1651.root, FC#0, port C2

Entries	431
Mean	40
Std Dev	16.39

Turn on : 25.2761

Width : 2.750

Height : 10.044



B1L103S, U18-ch96

calib_packv5_041523_1651.root, FC#0, port C2

Entries	438
Mean	39.03
Std Dev	17.49

Turn on : 25.2358

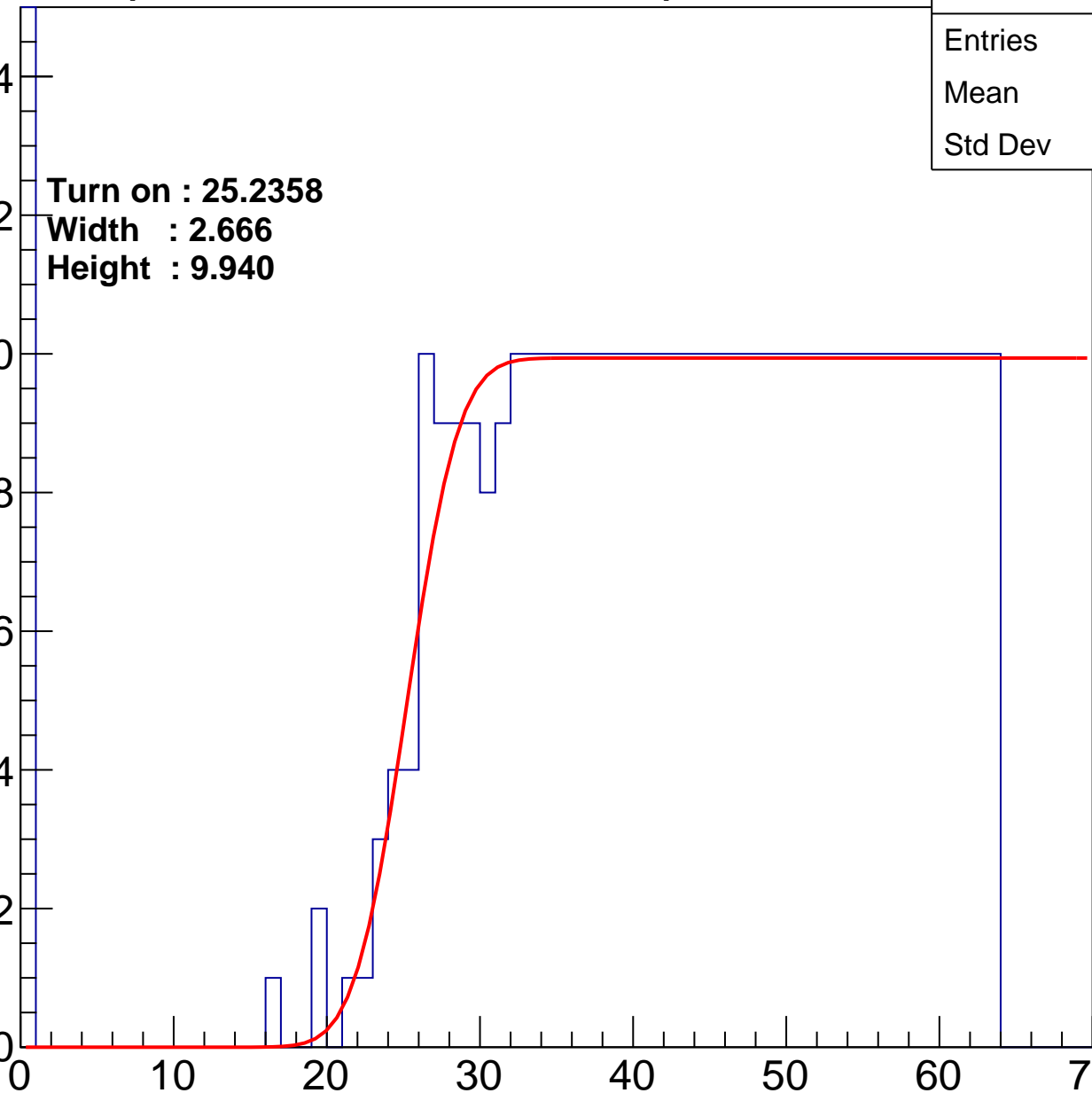
Width : 2.666

Height : 9.940

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U18-ch97

calib_packv5_041523_1651.root, FC#0, port C2

Entries	434
Mean	38.91
Std Dev	17.91

Turn on : 26.0258

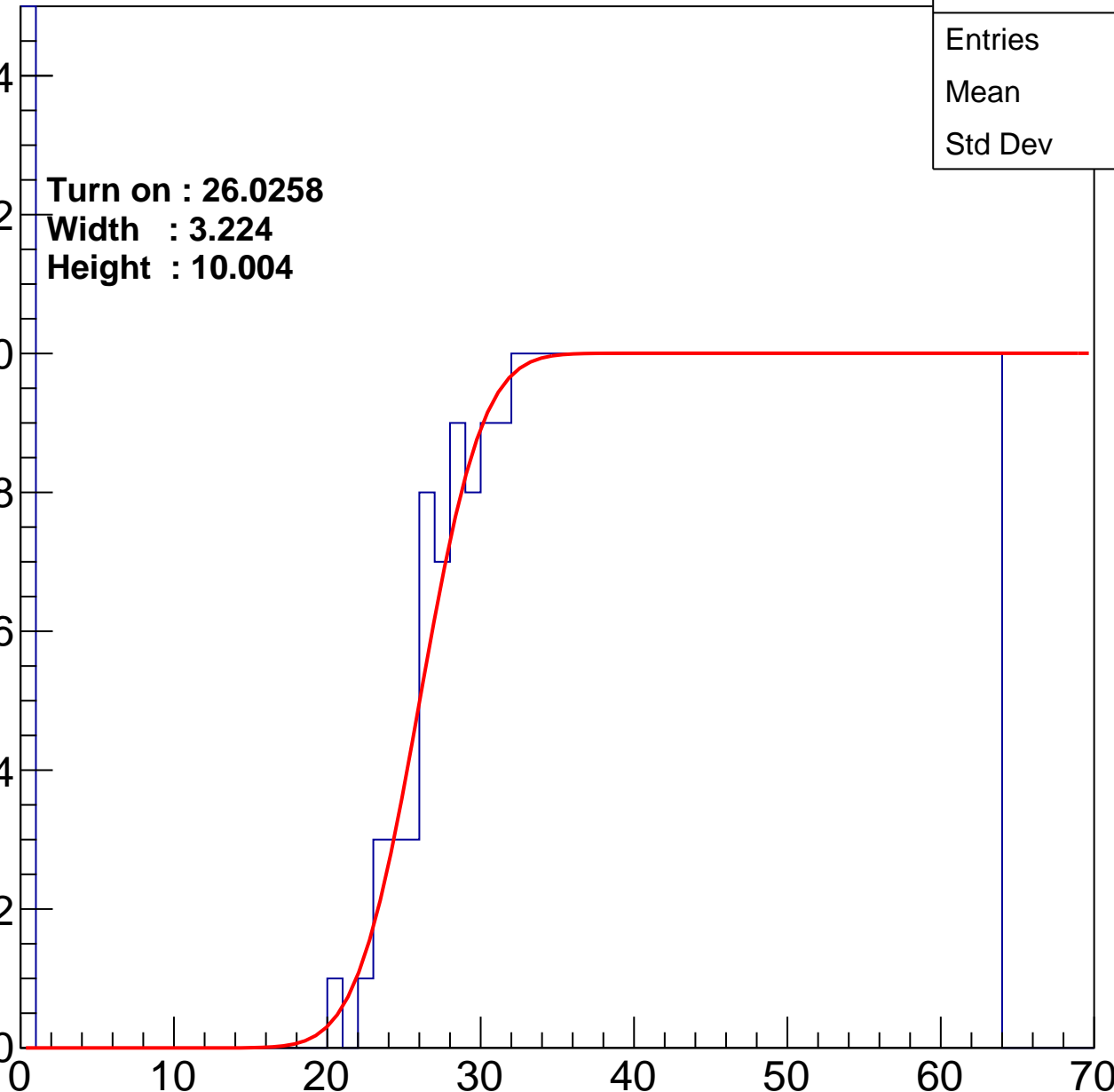
Width : 3.224

Height : 10.004

Entry

14
12
10
8
6
4
2
0

ampl

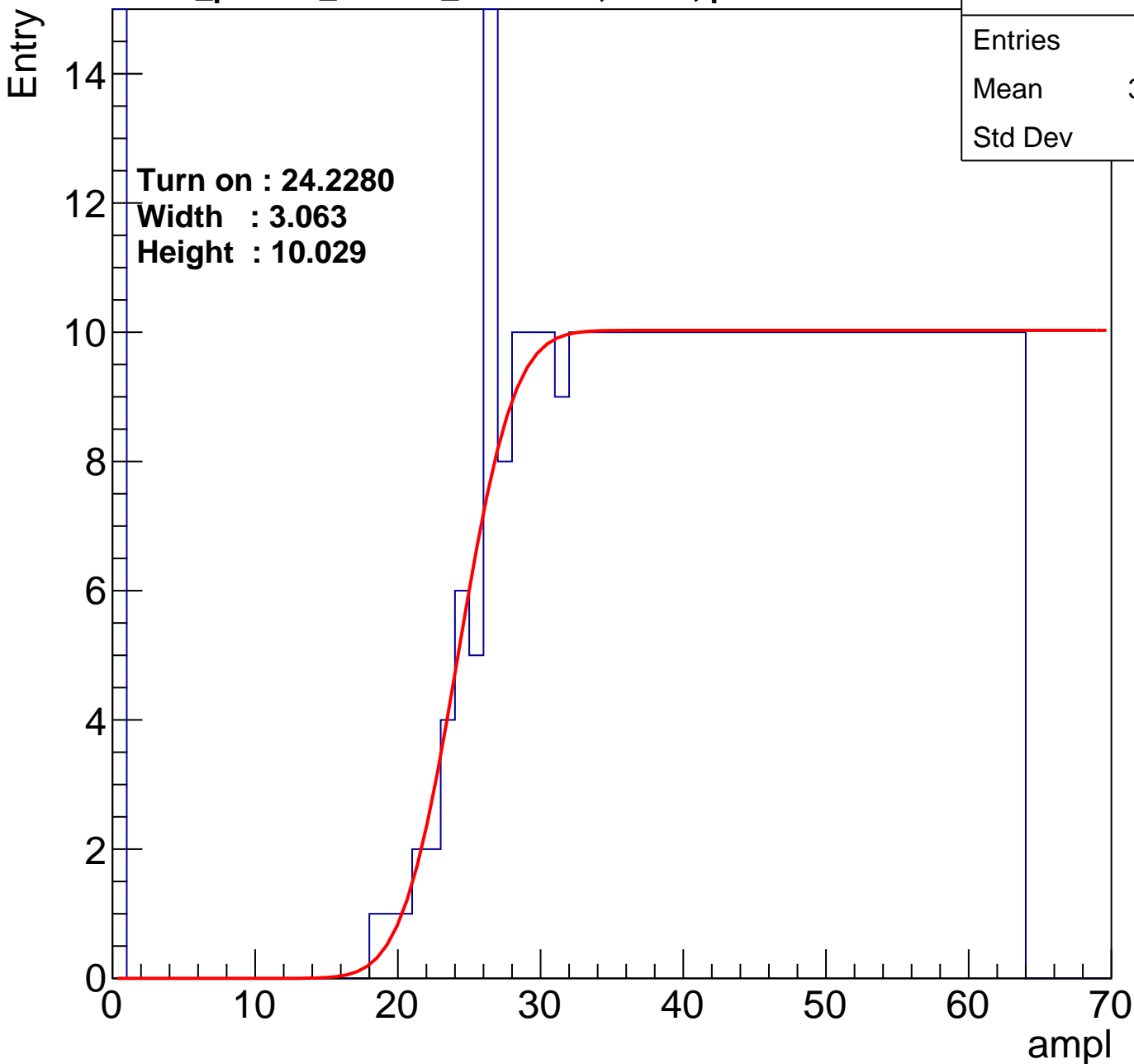


B1L103S, U18-ch98

calib_packv5_041523_1651.root, FC#0, port C2

Entries	445
Mean	39.23
Std Dev	16.81

Turn on : 24.2280
Width : 3.063
Height : 10.029



B1L103S, U18-ch99

calib_packv5_041523_1651.root, FC#0, port C2

Entries	434
Mean	39.16
Std Dev	17.52

Turn on : 25.5378

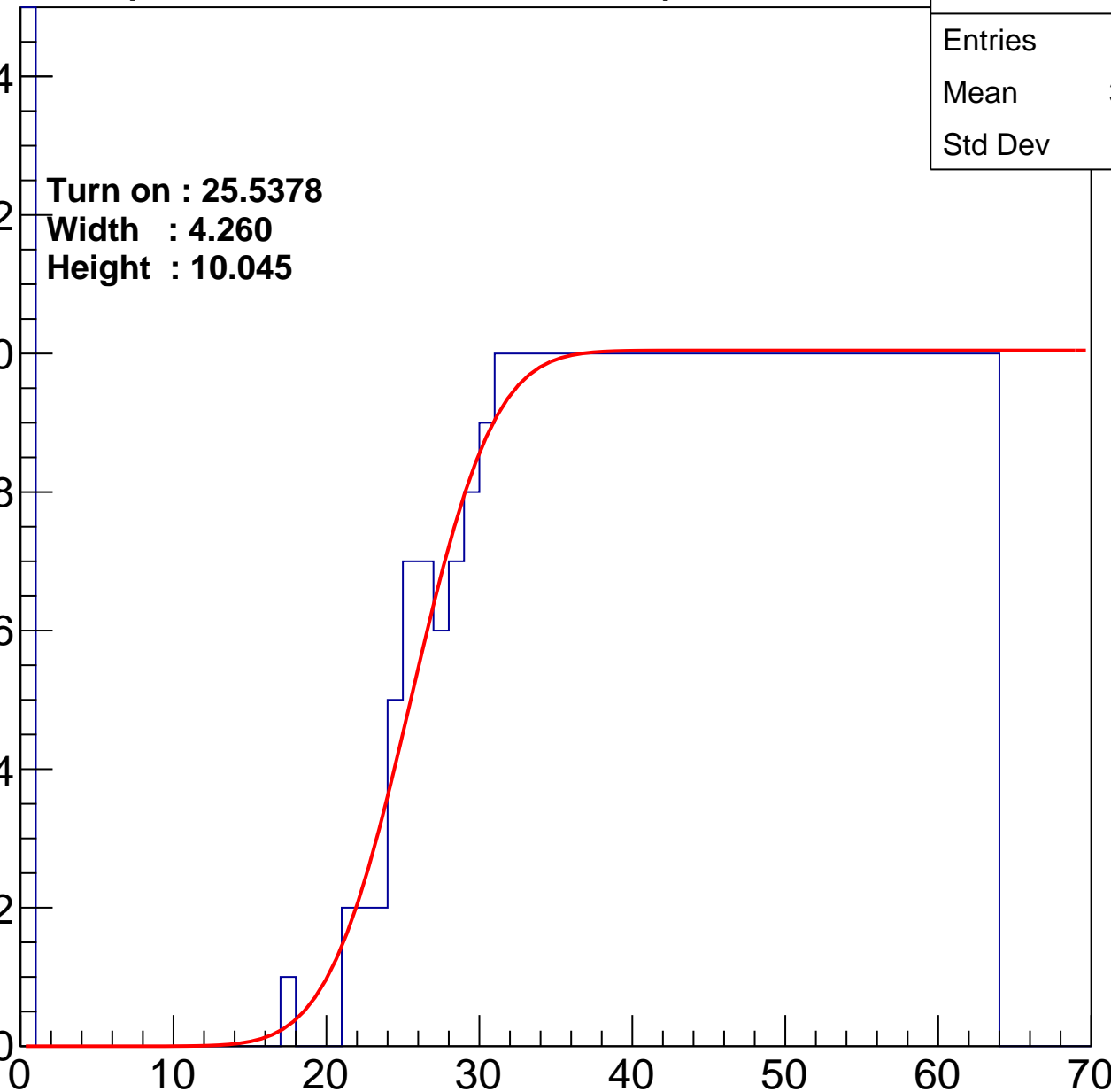
Width : 4.260

Height : 10.045

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U18-ch100

calib_packv5_041523_1651.root, FC#0, port C2

Entries	477
Mean	36.96
Std Dev	18.45

Turn on : 22.9505

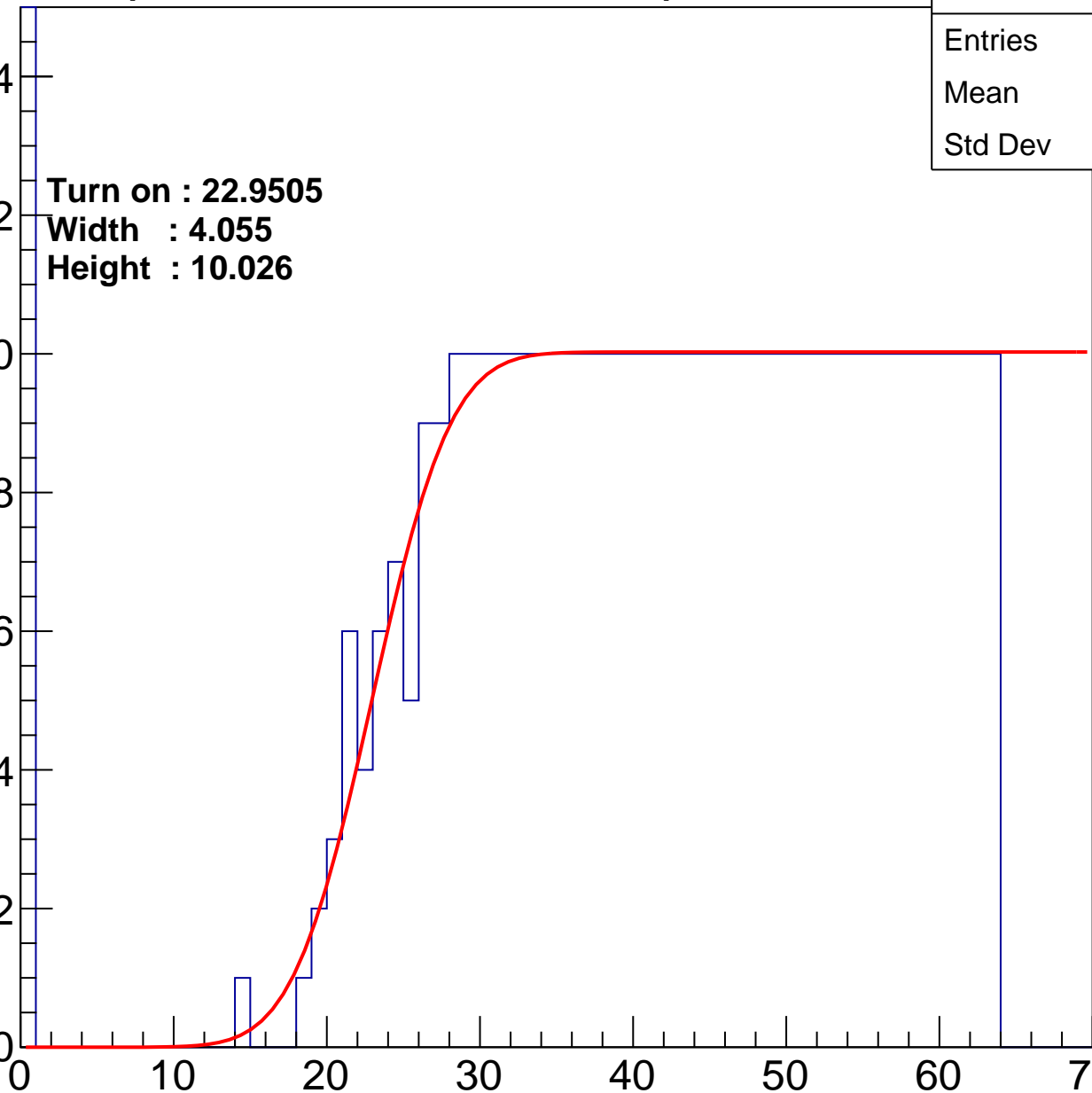
Width : 4.055

Height : 10.026

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U18-ch101

calib_packv5_041523_1651.root, FC#0, port C2

Entries	413
Mean	40.16
Std Dev	17.18

Turn on : 27.0638

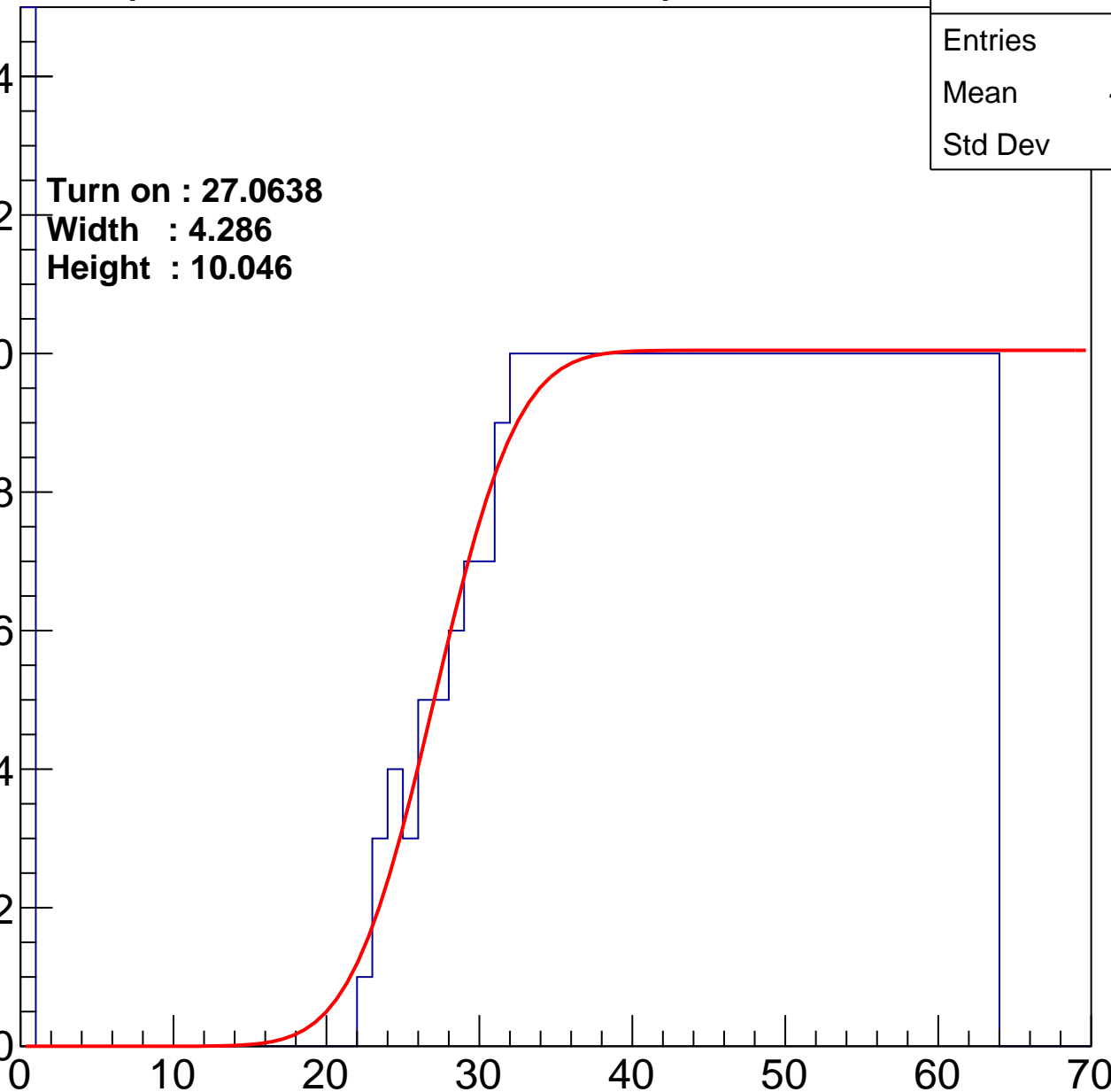
Width : 4.286

Height : 10.046

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U18-ch102

calib_packv5_041523_1651.root, FC#0, port C2

Entries	458
Mean	37.86
Std Dev	18.15

Turn on : 24.1450

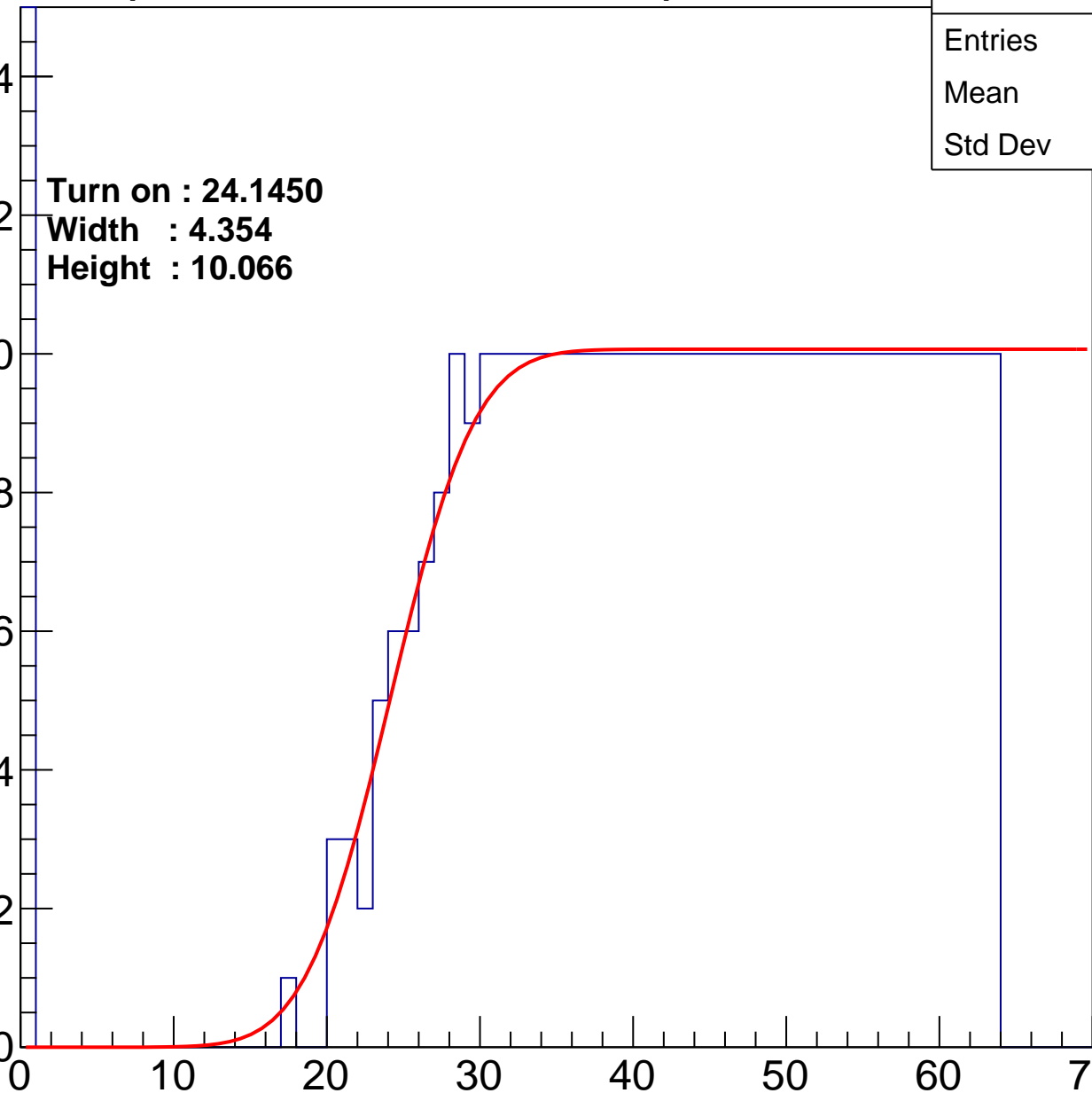
Width : 4.354

Height : 10.066

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U18-ch103

calib_packv5_041523_1651.root, FC#0, port C2

Entries	429
Mean	38.68
Std Dev	18.54

Turn on : 27.7346

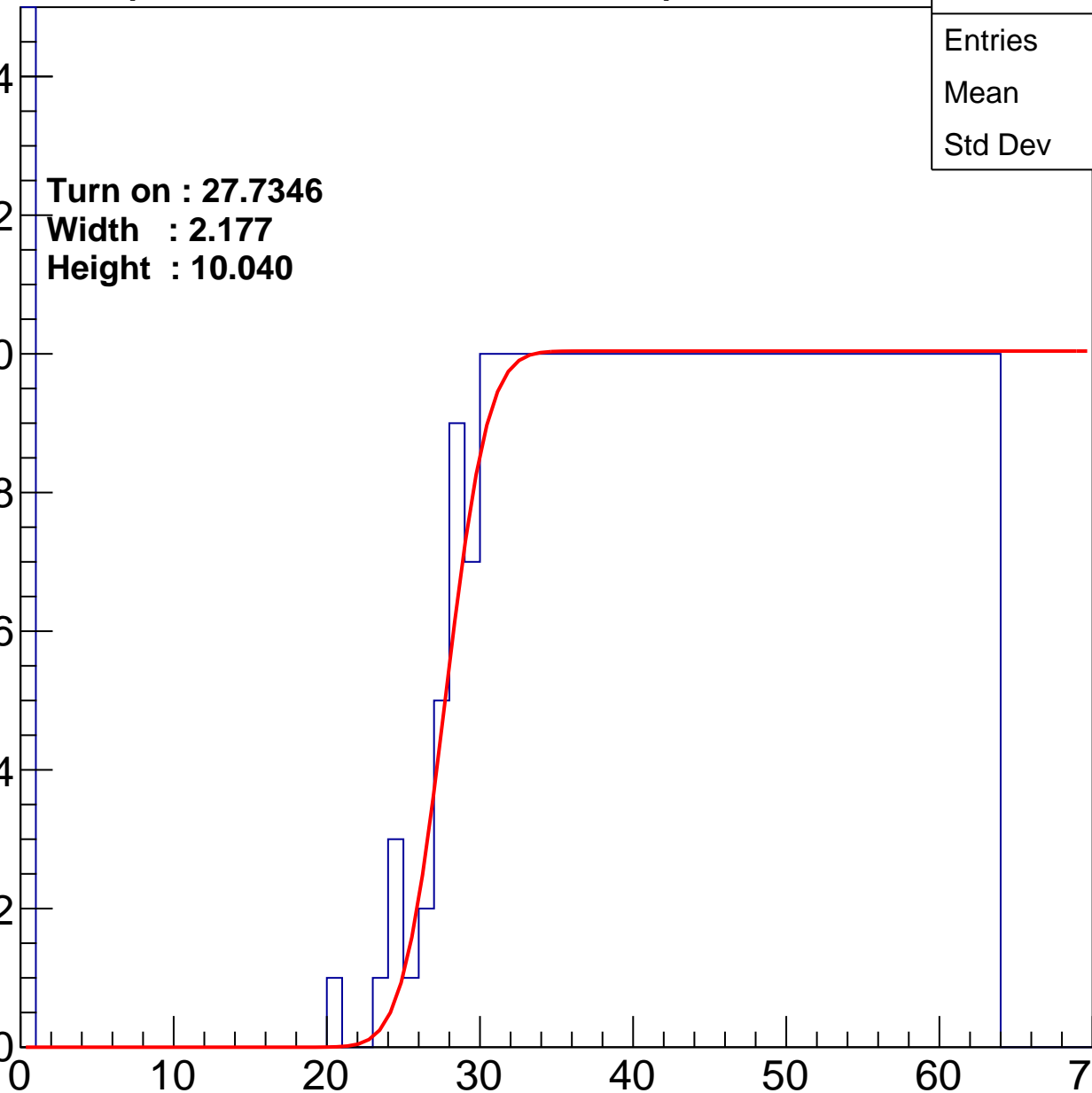
Width : 2.177

Height : 10.040

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U18-ch104

calib_packv5_041523_1651.root, FC#0, port C2

Entries	482
Mean	36.01
Std Dev	19.46

Turn on : 24.1732

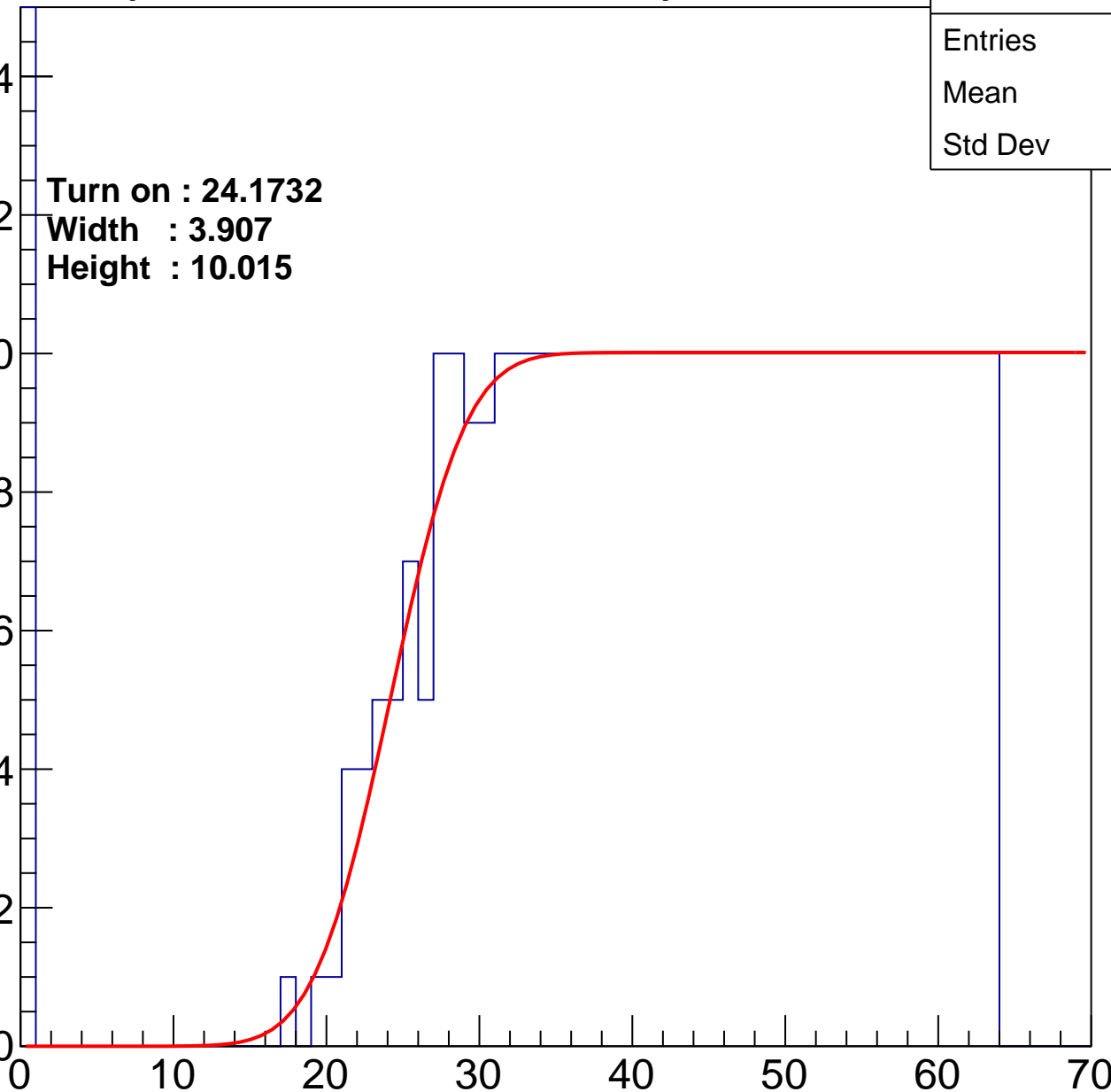
Width : 3.907

Height : 10.015

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U18-ch105

calib_packv5_041523_1651.root, FC#0, port C2

Entries	452
Mean	38.1
Std Dev	18.11

Turn on : 24.7424

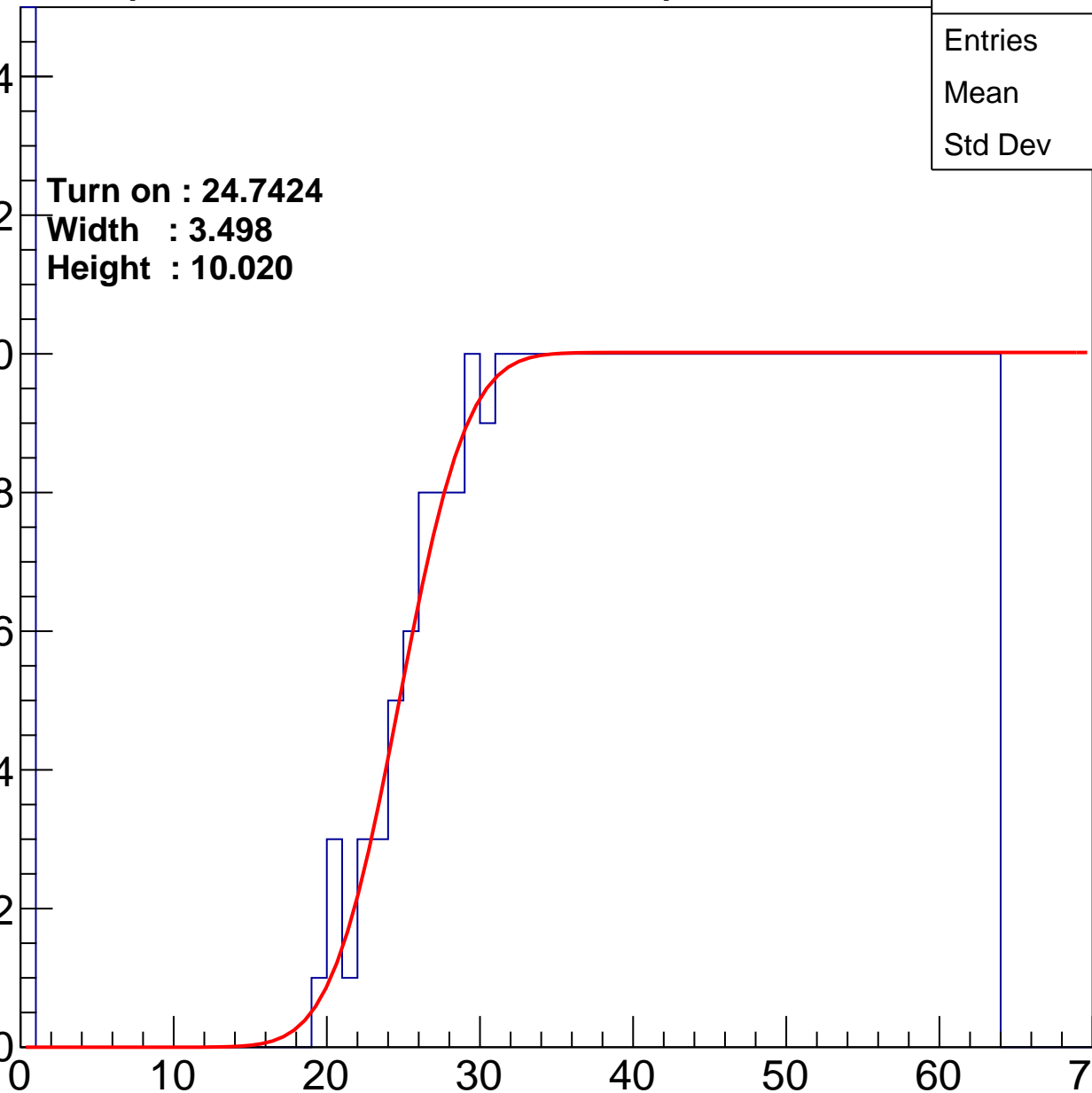
Width : 3.498

Height : 10.020

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U18-ch106

calib_packv5_041523_1651.root, FC#0, port C2

Entries	441
Mean	39.49
Std Dev	16.61

Turn on : 24.0301

Width : 3.490

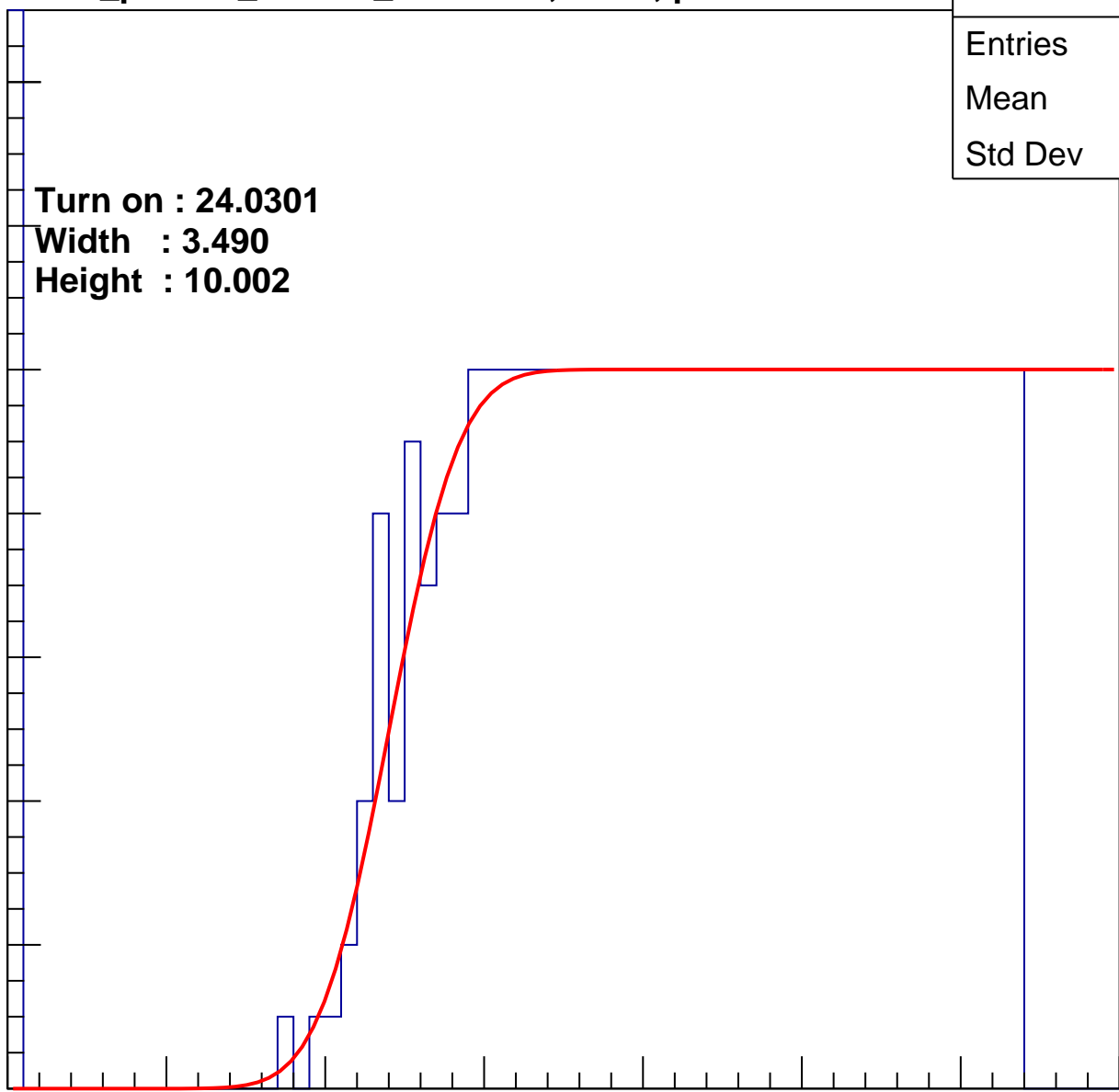
Height : 10.002

Entry

14
12
10
8
6
4
2
0

ampl

0 10 20 30 40 50 60 70



B1L103S, U18-ch107

calib_packv5_041523_1651.root, FC#0, port C2

Entries	408
Mean	41
Std Dev	16.19

Turn on : 26.8955

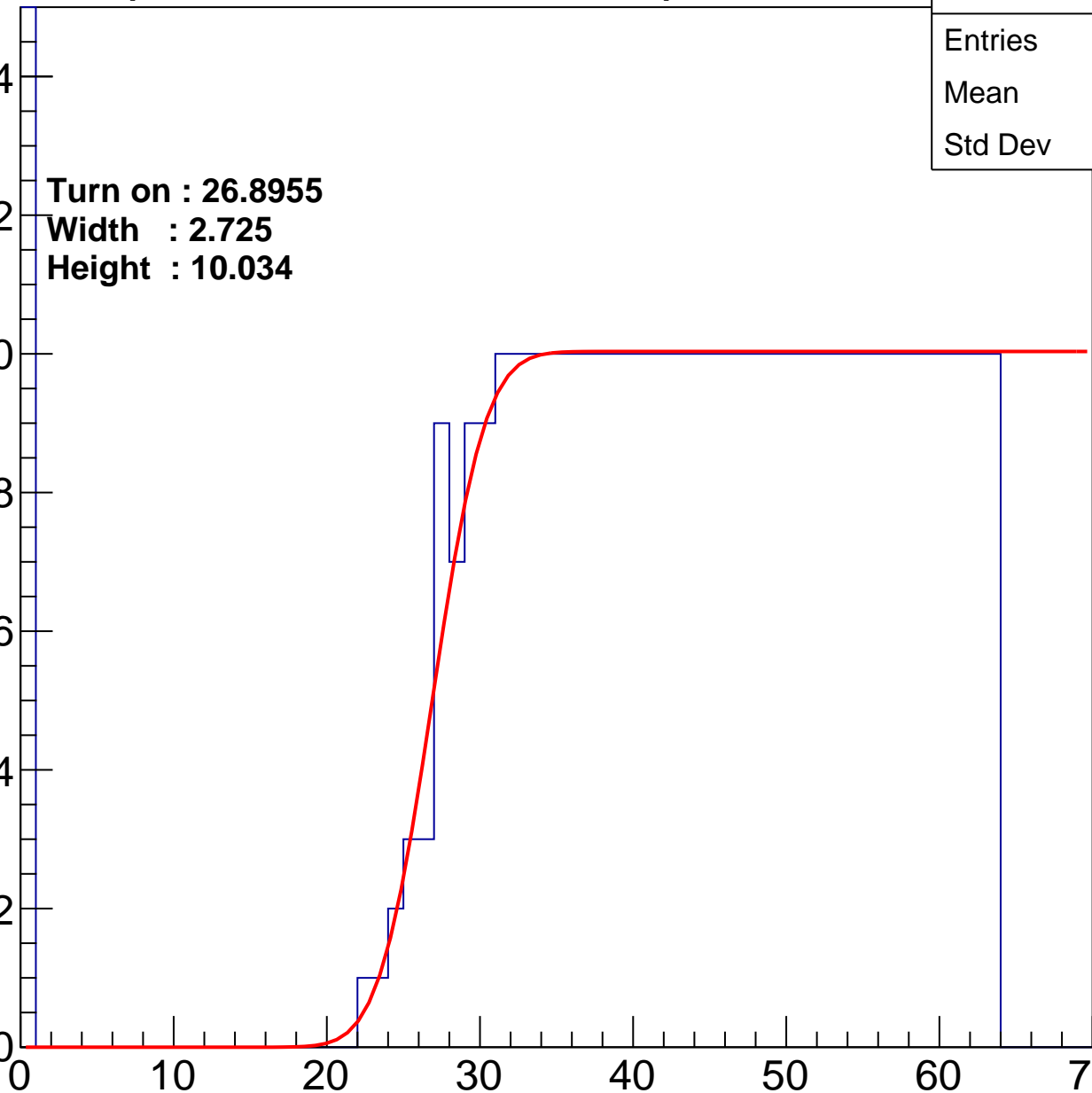
Width : 2.725

Height : 10.034

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U18-ch108

calib_packv5_041523_1651.root, FC#0, port C2

Entries	458
Mean	37.96
Std Dev	18.04

Turn on : 24.1599

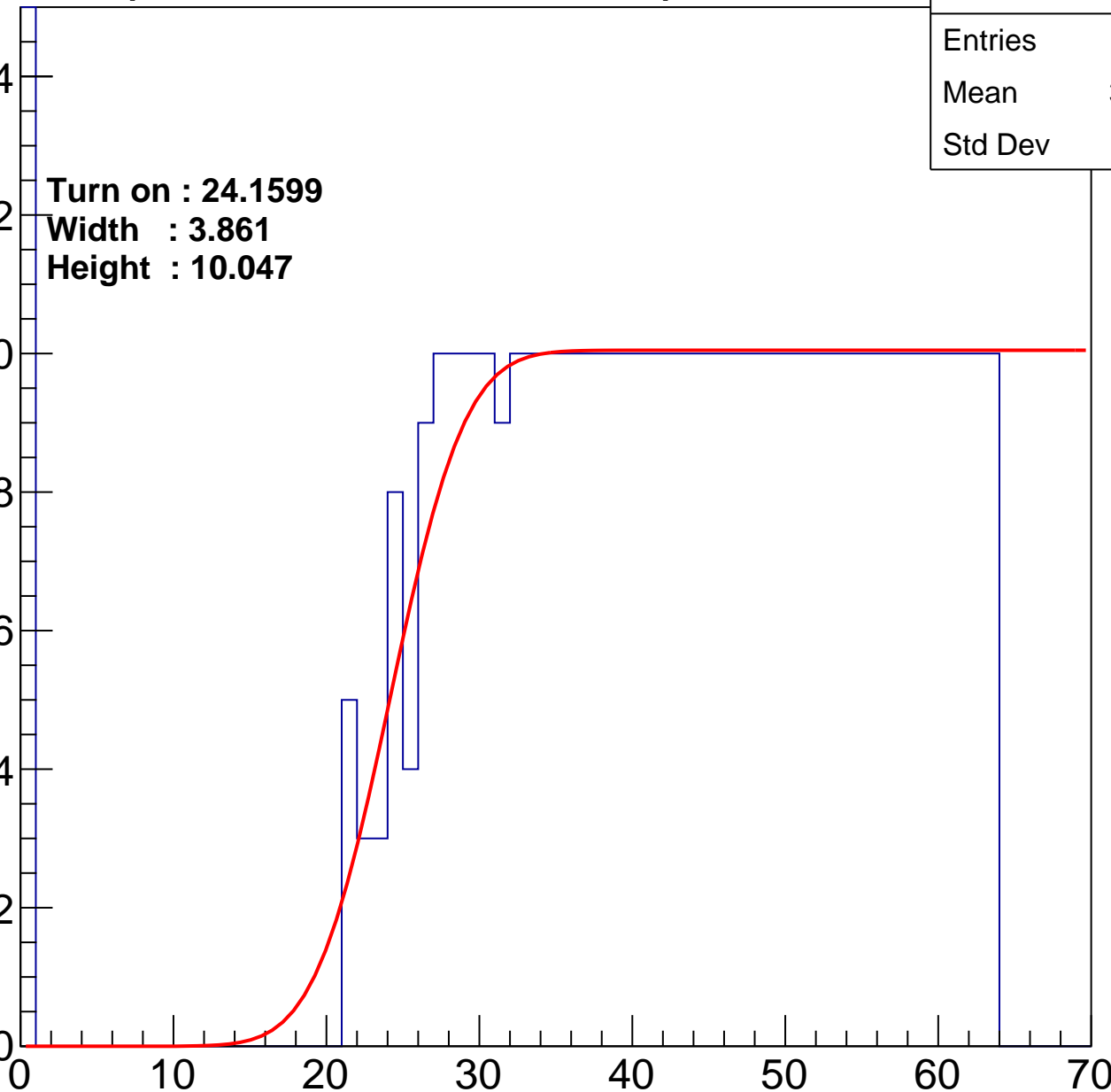
Width : 3.861

Height : 10.047

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U18-ch109

calib_packv5_041523_1651.root, FC#0, port C2

Entries	414
Mean	40.2
Std Dev	17.07

Turn on : 26.8797

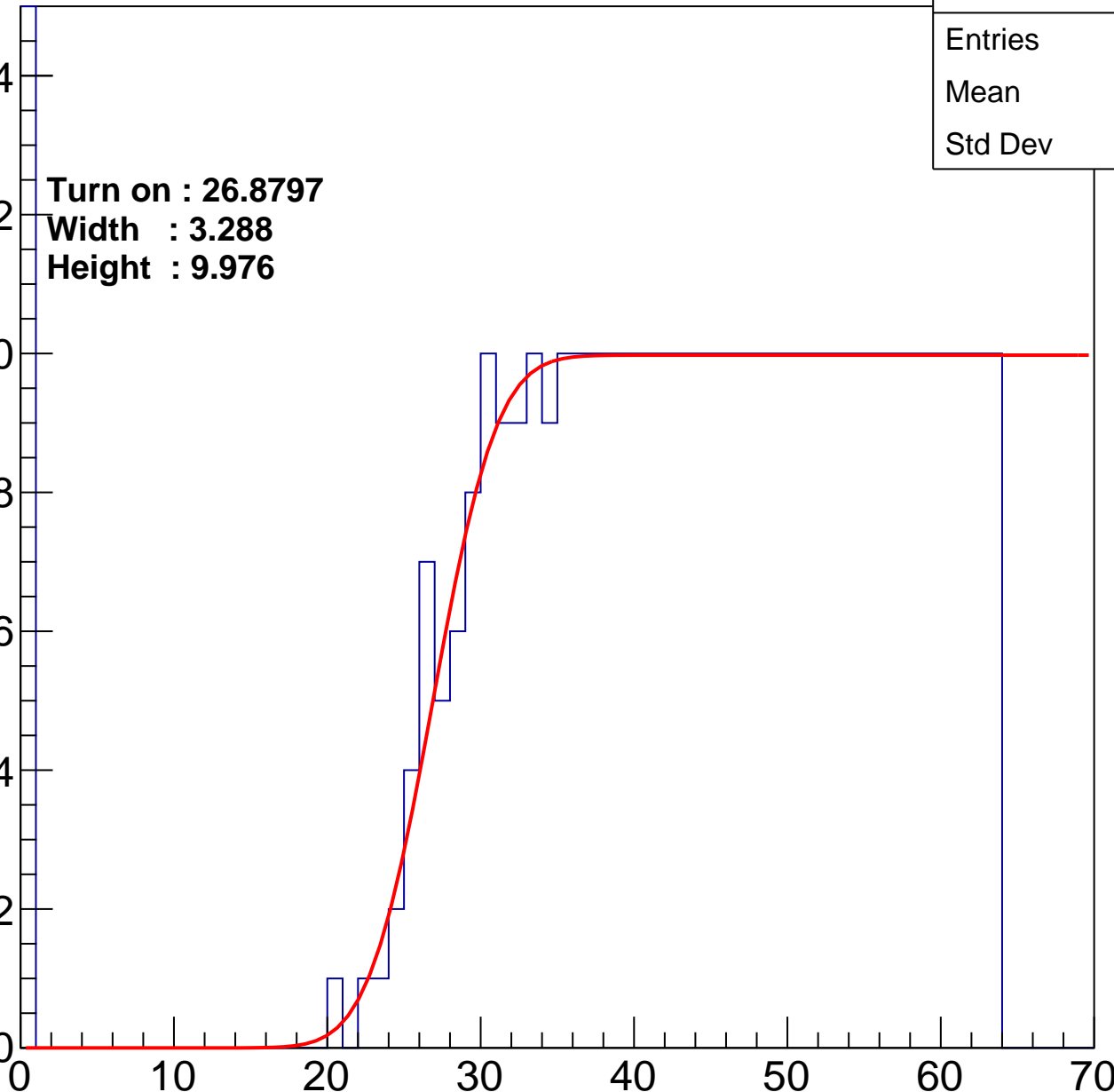
Width : 3.288

Height : 9.976

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U18-ch110

calib_packv5_041523_1651.root, FC#0, port C2

Entries	473
Mean	36.14
Std Dev	19.73

Turn on : 25.8755

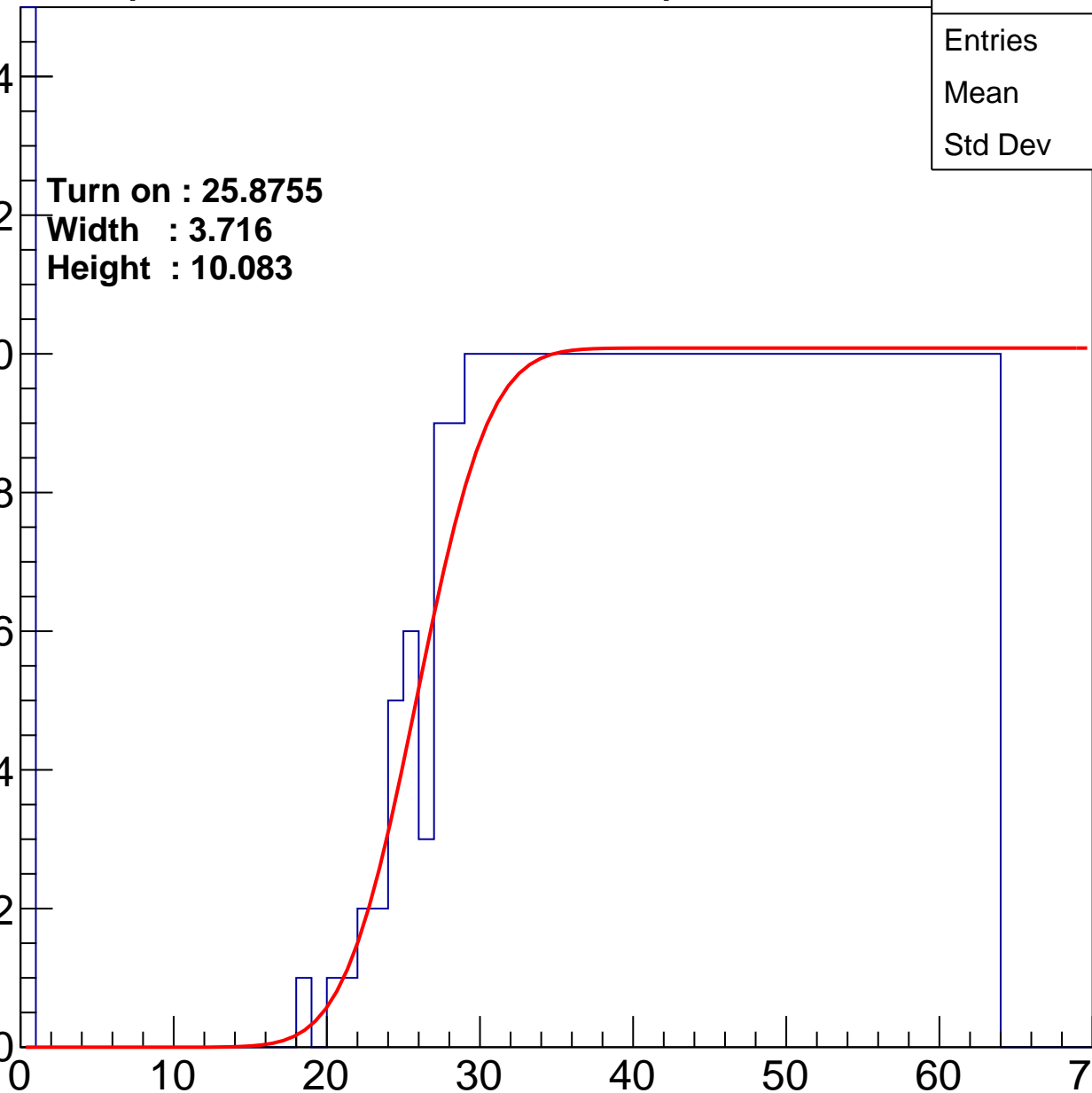
Width : 3.716

Height : 10.083

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U18-ch111

calib_packv5_041523_1651.root, FC#0, port C2

Entries	436
Mean	38.4
Std Dev	18.51

Turn on : 27.2480

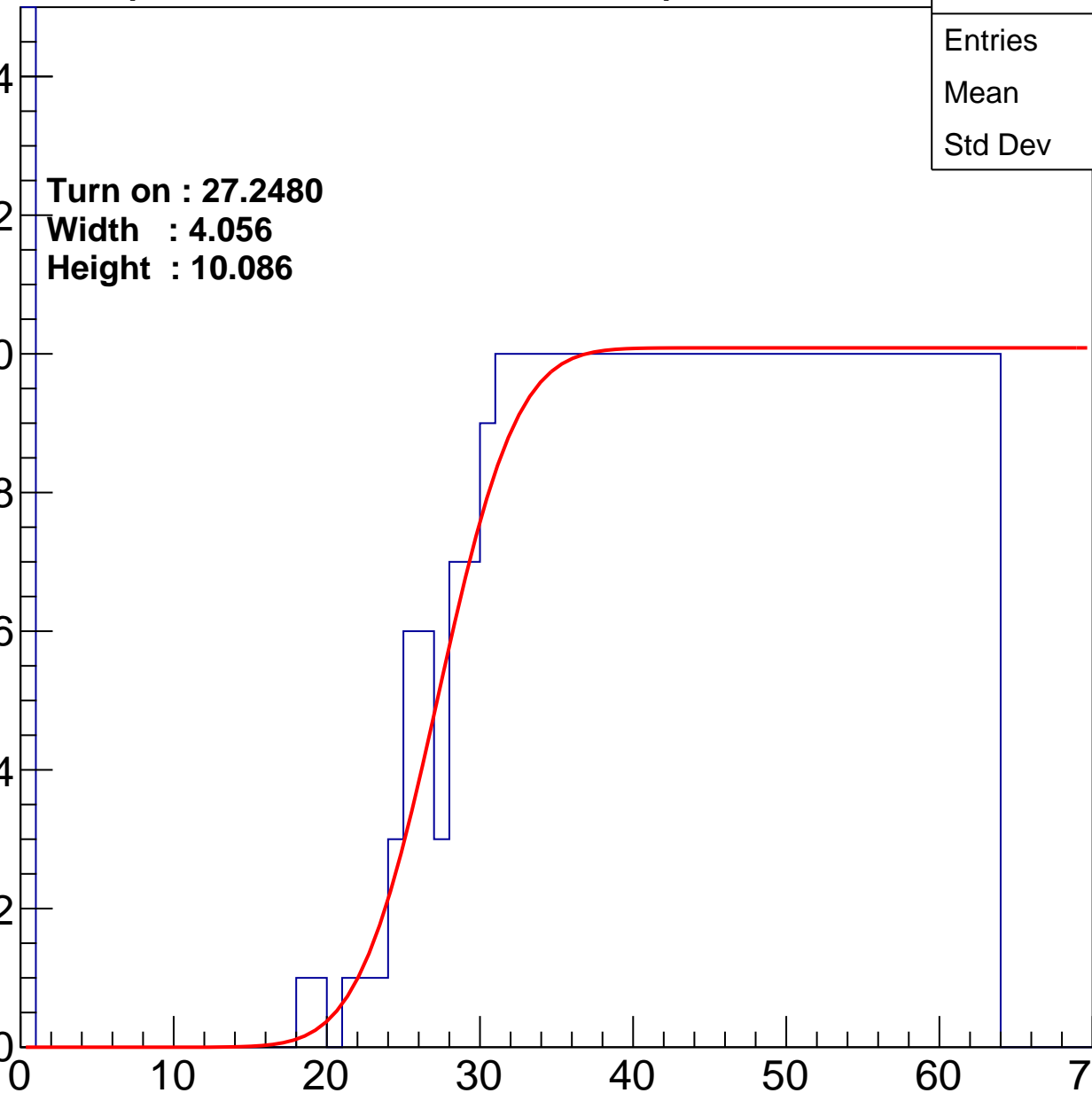
Width : 4.056

Height : 10.086

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U18-ch112

calib_packv5_041523_1651.root, FC#0, port C2

Entries	430
Mean	39.32
Std Dev	17.63

Turn on : 26.0539

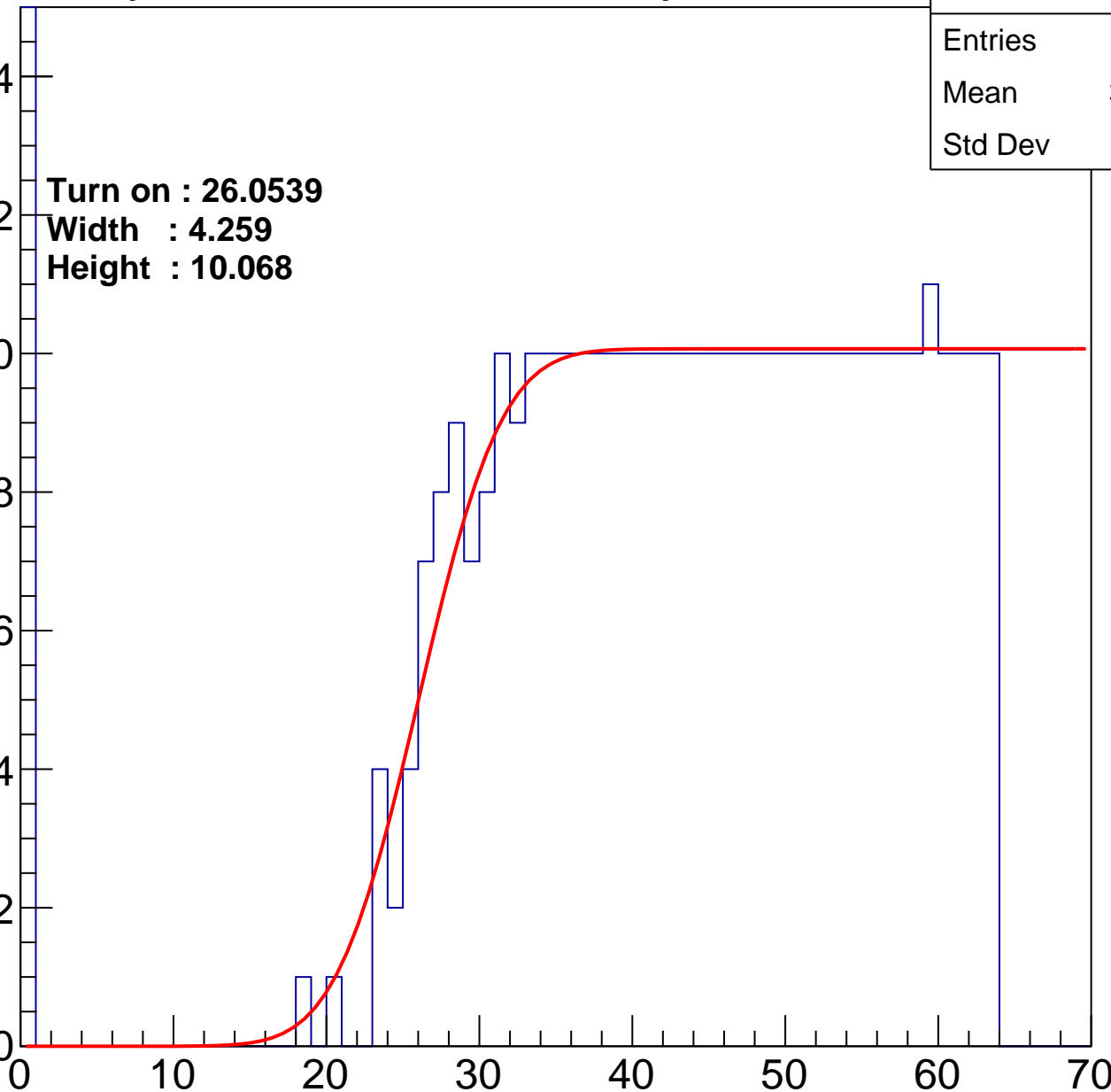
Width : 4.259

Height : 10.068

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U18-ch113

calib_packv5_041523_1651.root, FC#0, port C2

Entries	435
Mean	38.42
Std Dev	18.52

Turn on : 26.9965

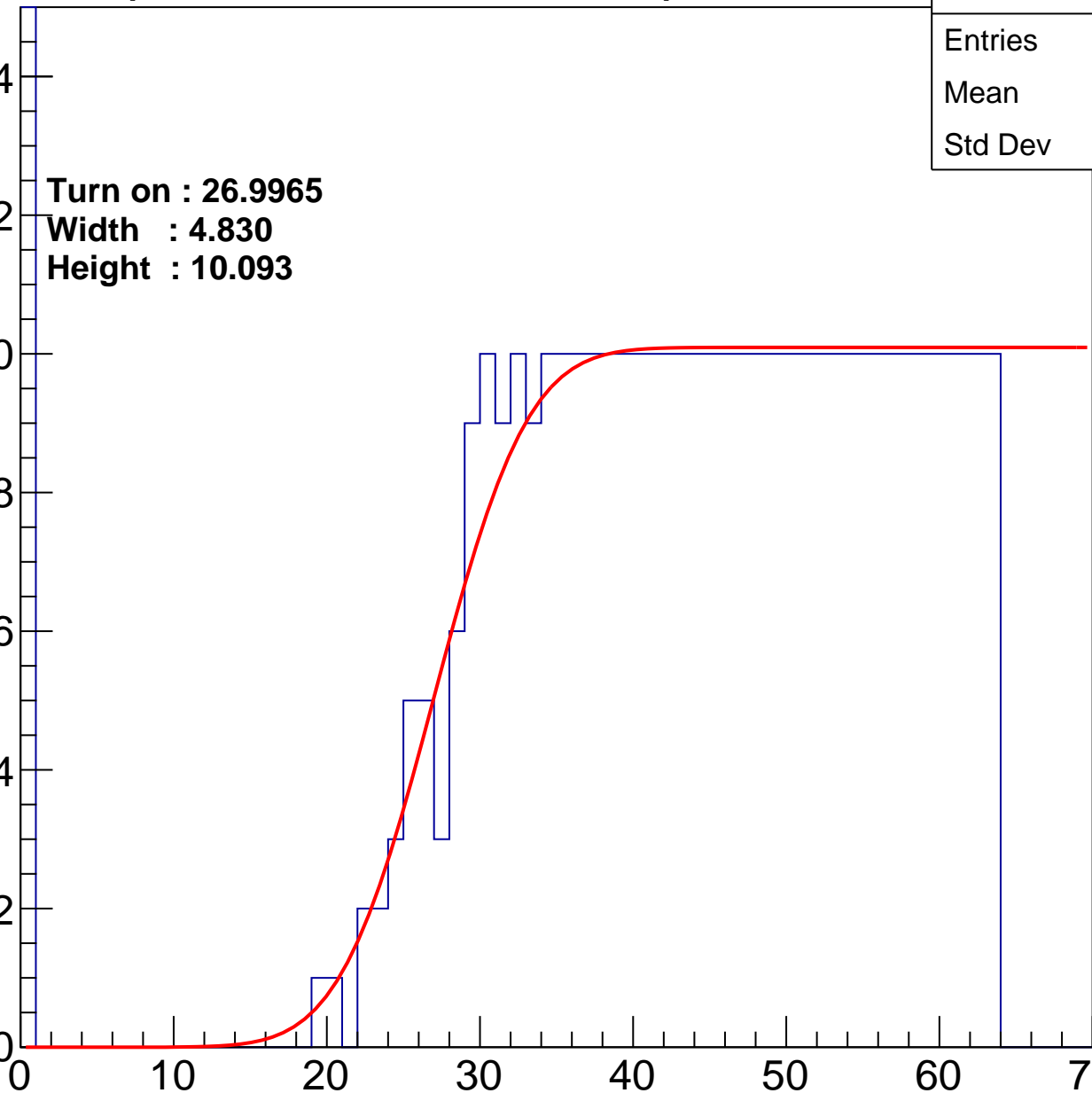
Width : 4.830

Height : 10.093

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U18-ch114

calib_packv5_041523_1651.root, FC#0, port C2

Entries	442
Mean	38.58
Std Dev	17.94

Turn on : 25.1710

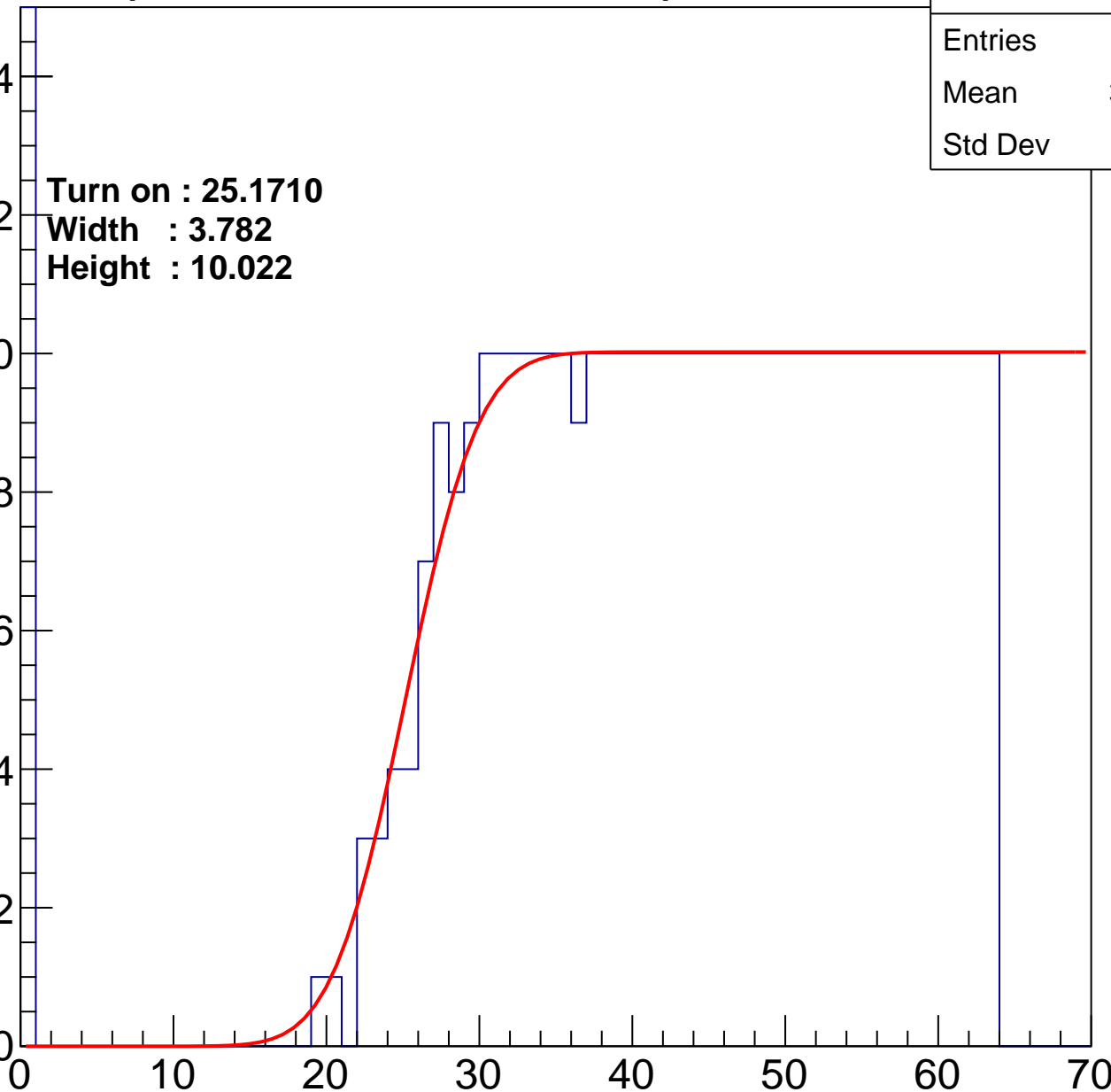
Width : 3.782

Height : 10.022

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U18-ch115

calib_packv5_041523_1651.root, FC#0, port C2

Entries	456
Mean	37.53
Std Dev	18.73

Turn on : 25.1963

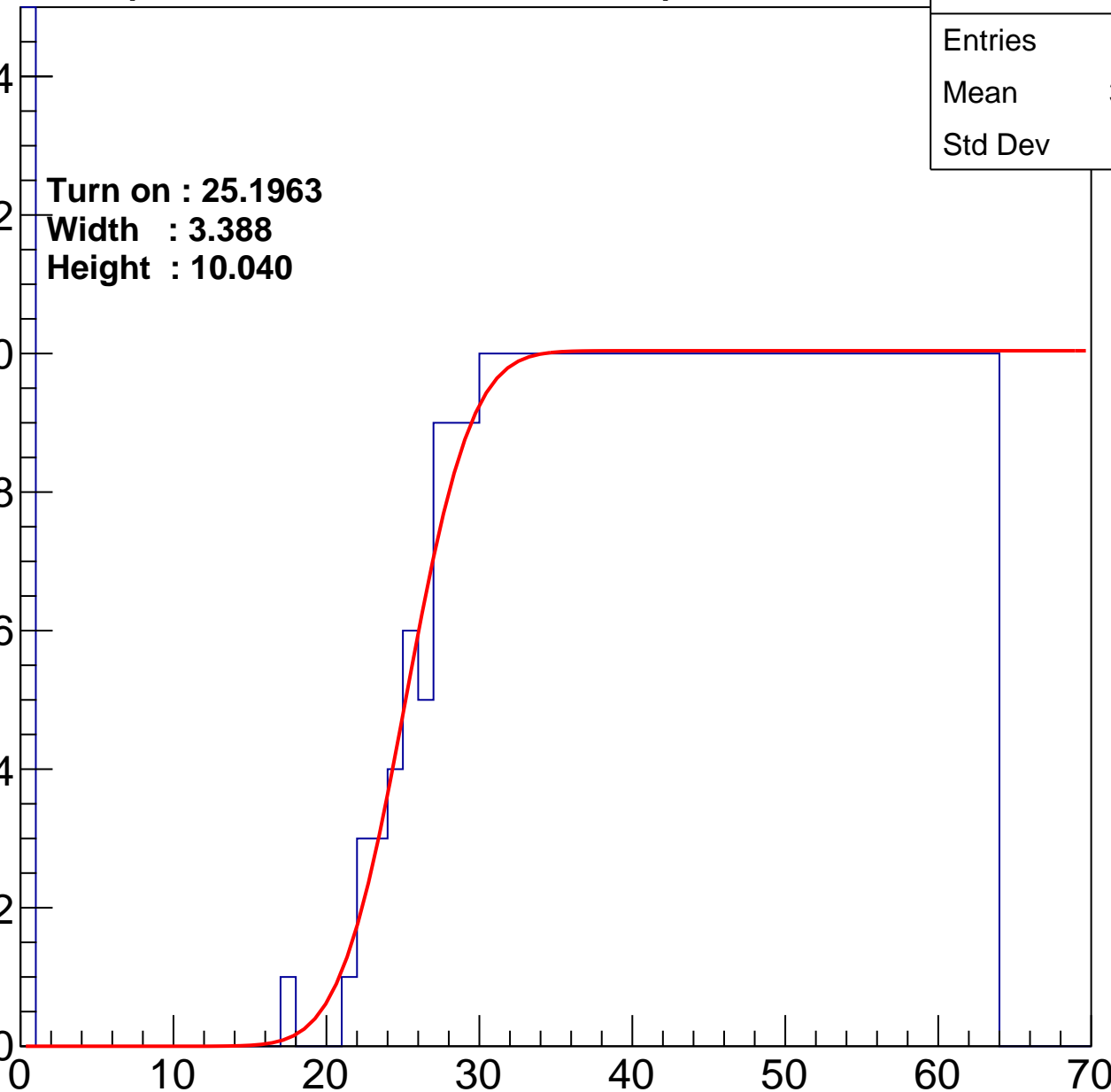
Width : 3.388

Height : 10.040

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U18-ch116

calib_packv5_041523_1651.root, FC#0, port C2

Entries	471
Mean	37.02
Std Dev	18.68

Turn on : 24.1652

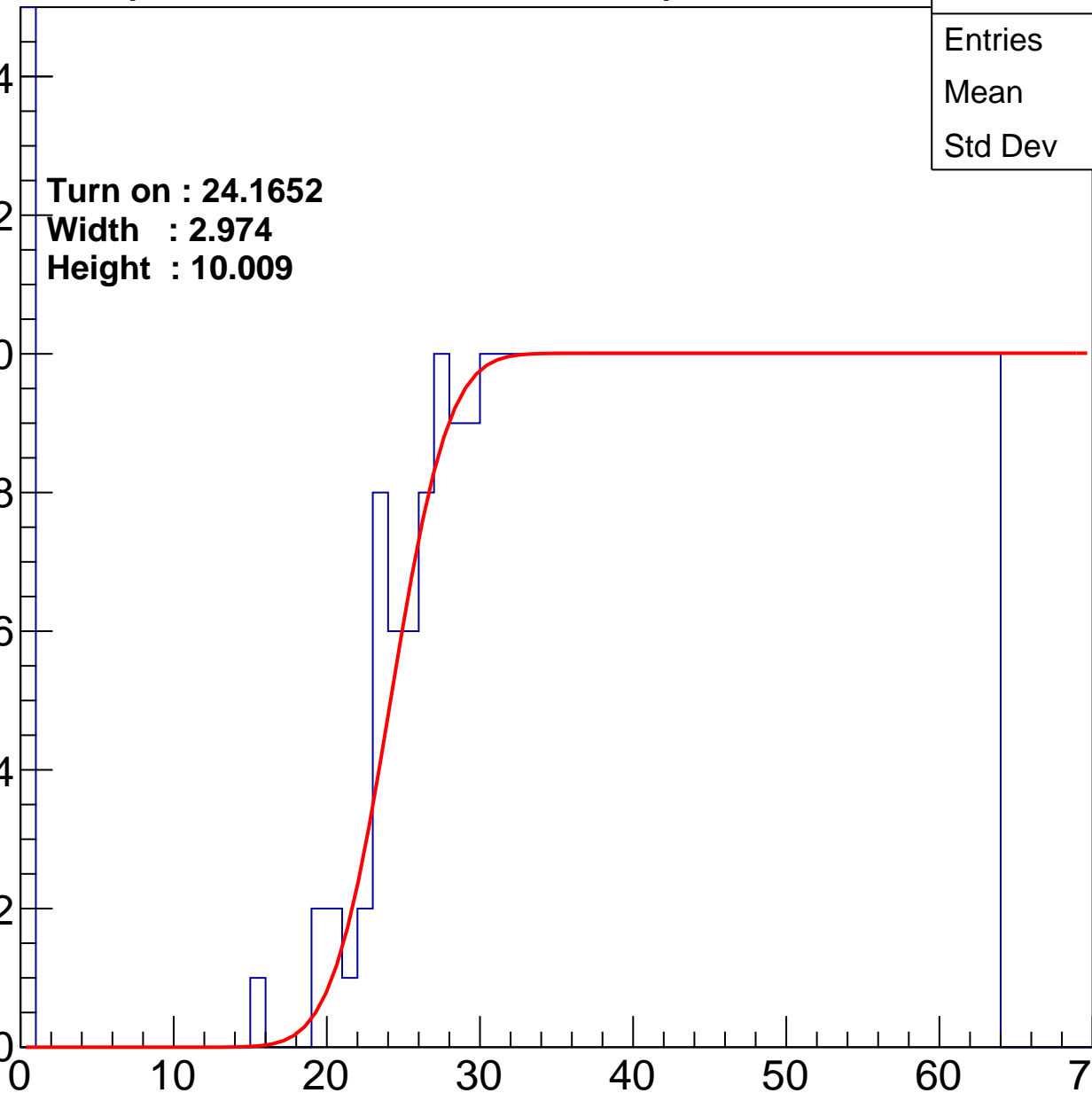
Width : 2.974

Height : 10.009

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U18-ch117

calib_packv5_041523_1651.root, FC#0, port C2

Entries	438
Mean	38.32
Std Dev	18.54

Turn on : 26.6574

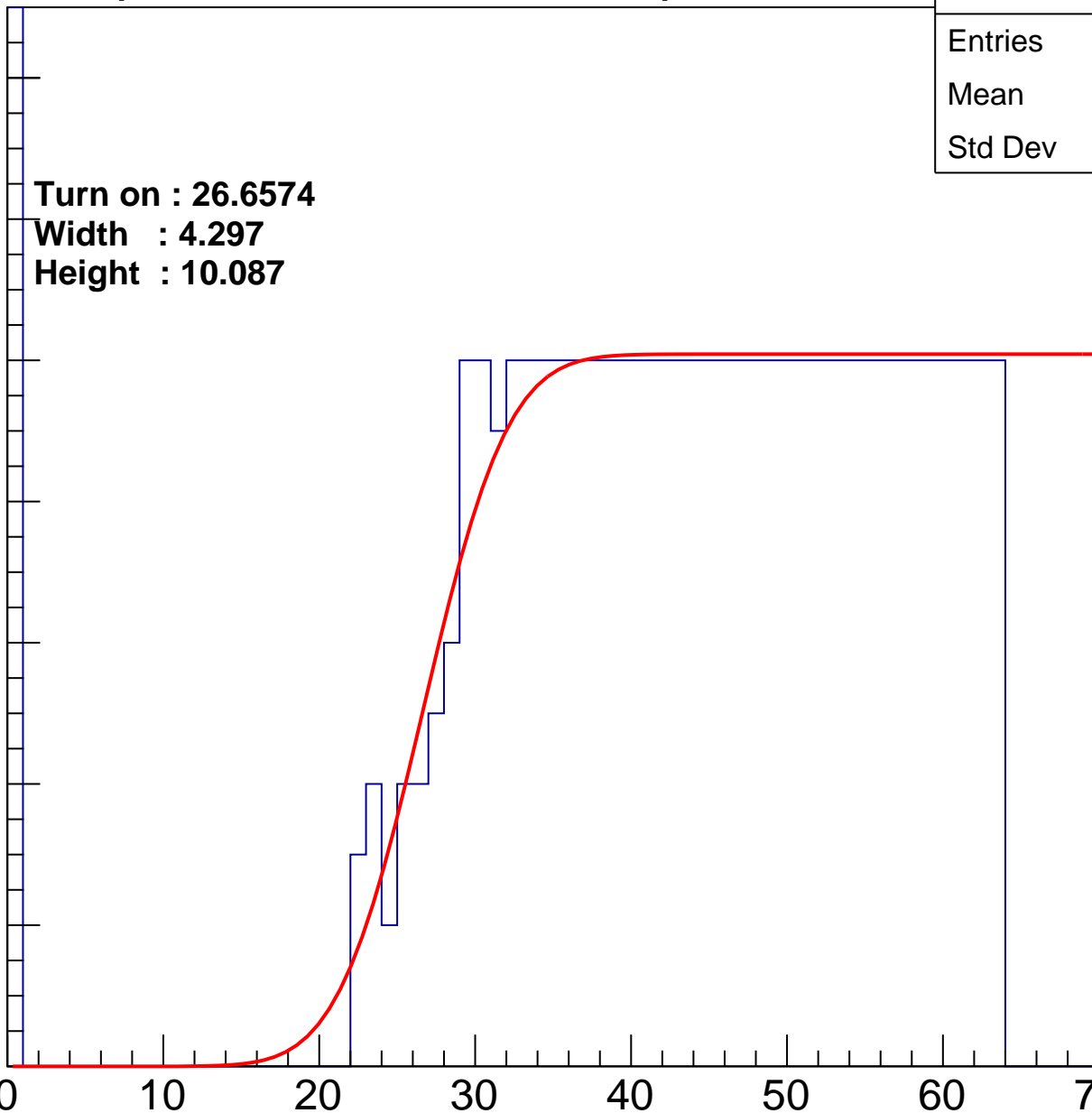
Width : 4.297

Height : 10.087

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U18-ch118

calib_packv5_041523_1651.root, FC#0, port C2

Entries	417
Mean	39.77
Std Dev	17.54

Turn on : 27.1159

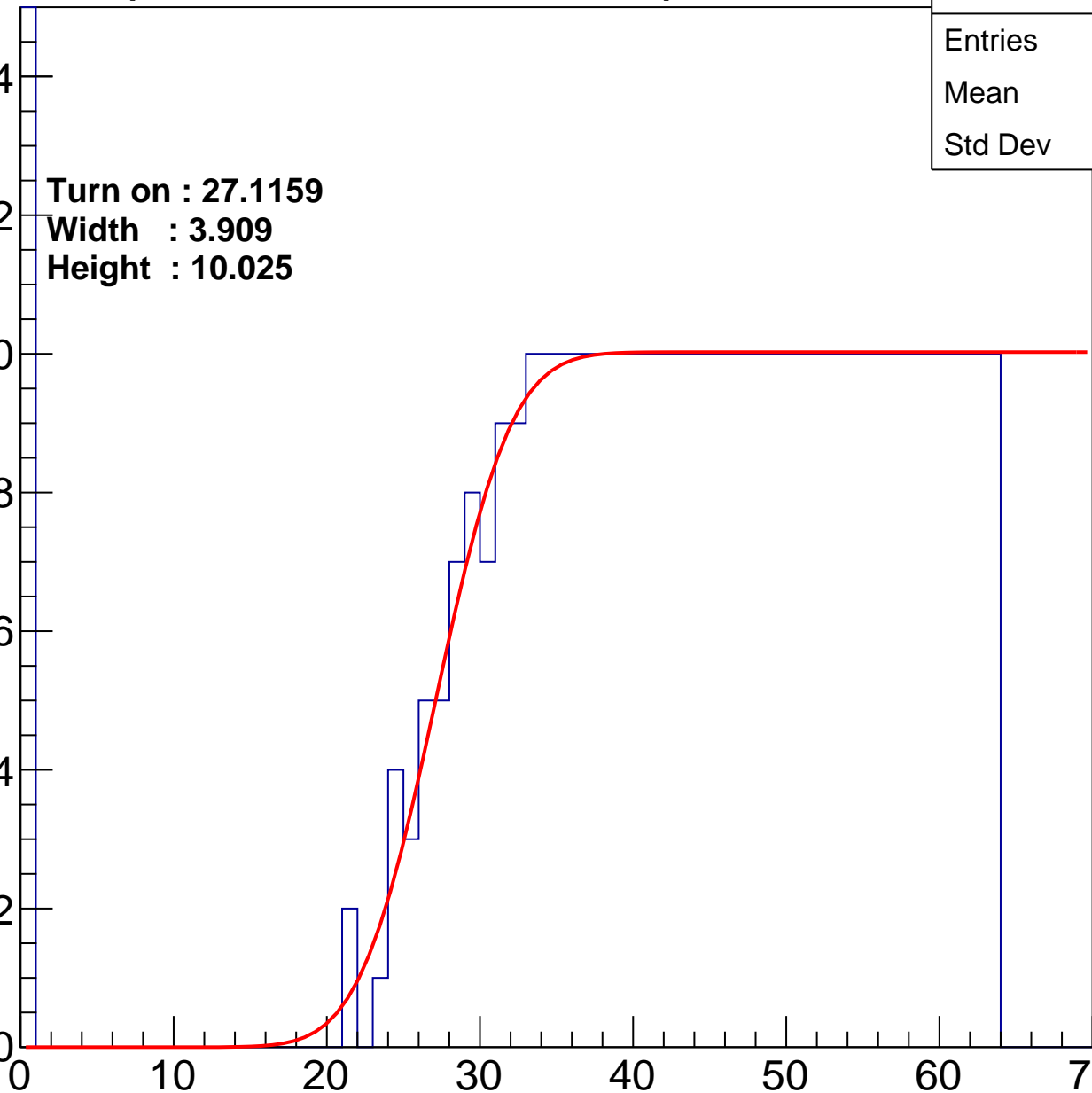
Width : 3.909

Height : 10.025

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U18-ch119

calib_packv5_041523_1651.root, FC#0, port C2

Entries	424
Mean	39.75
Std Dev	17.19

Turn on : 26.6163

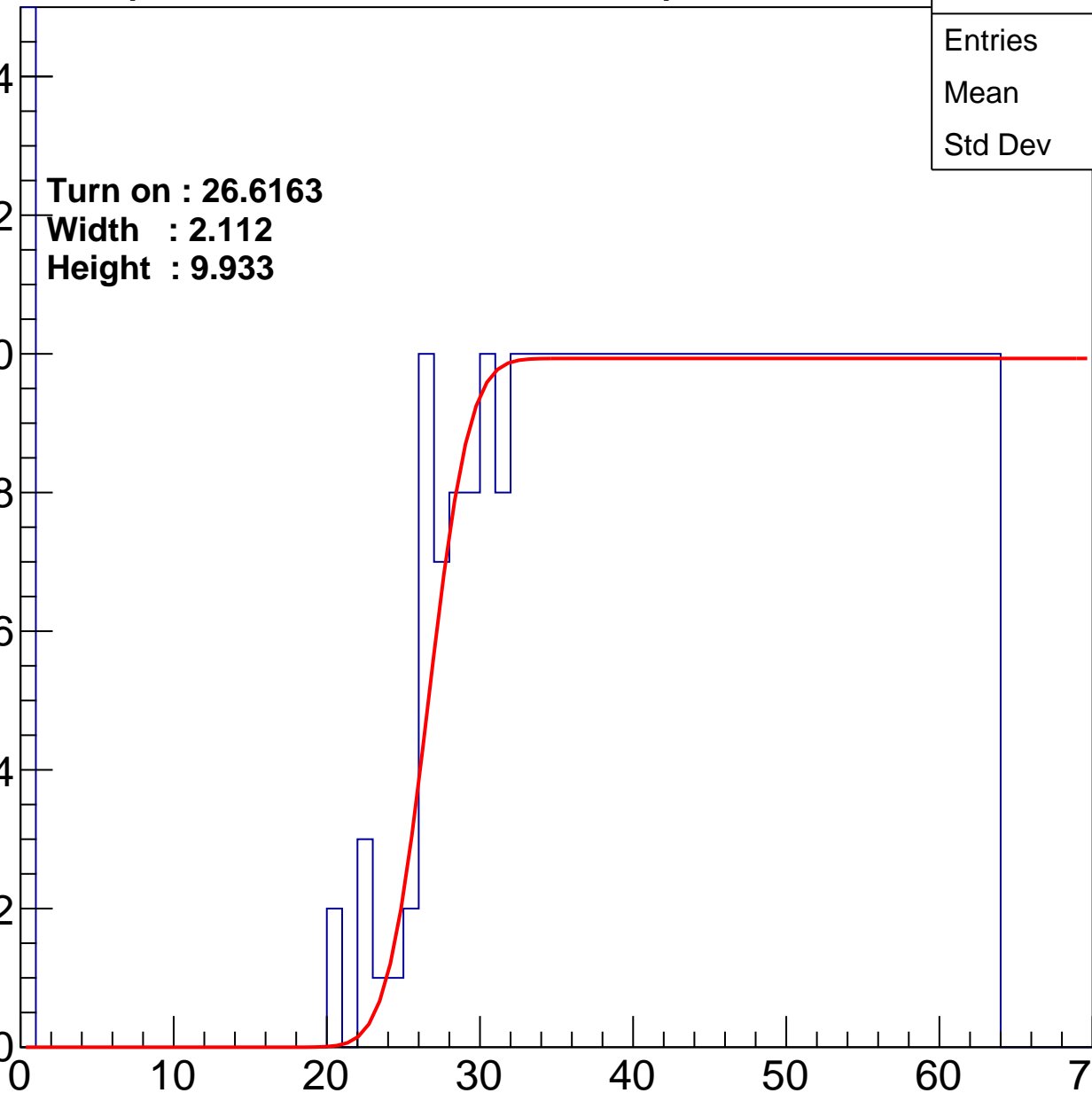
Width : 2.112

Height : 9.933

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U18-ch120

calib_packv5_041523_1651.root, FC#0, port C2

Entries	472
Mean	37.01
Std Dev	18.65

Turn on : 23.3349

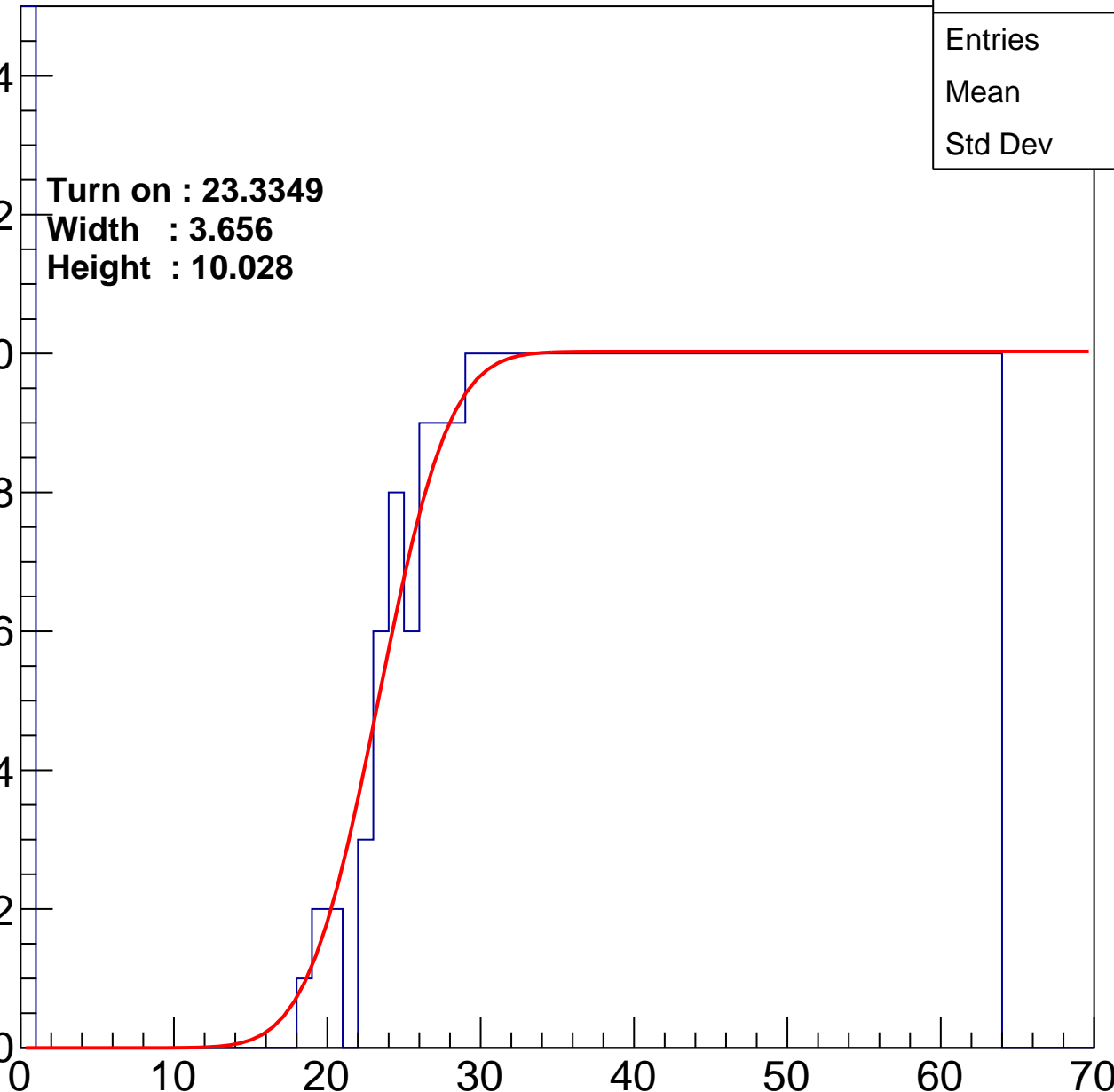
Width : 3.656

Height : 10.028

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U18-ch121

calib_packv5_041523_1651.root, FC#0, port C2

Entries	449
Mean	37.7
Std Dev	18.82

Turn on : 26.0529

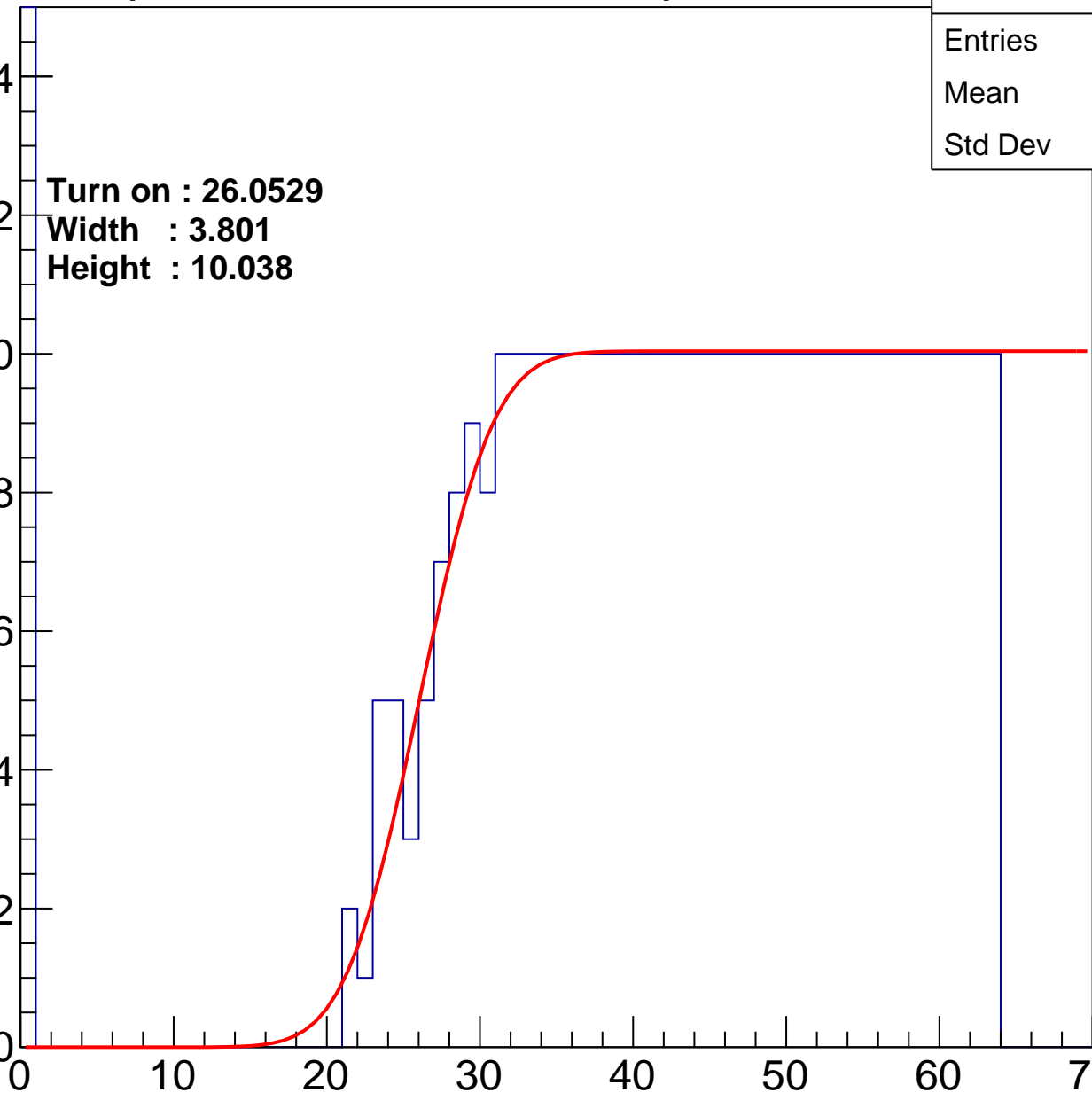
Width : 3.801

Height : 10.038

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U18-ch122

calib_packv5_041523_1651.root, FC#0, port C2

Entries	464
Mean	37.23
Std Dev	18.79

Turn on : 24.5290

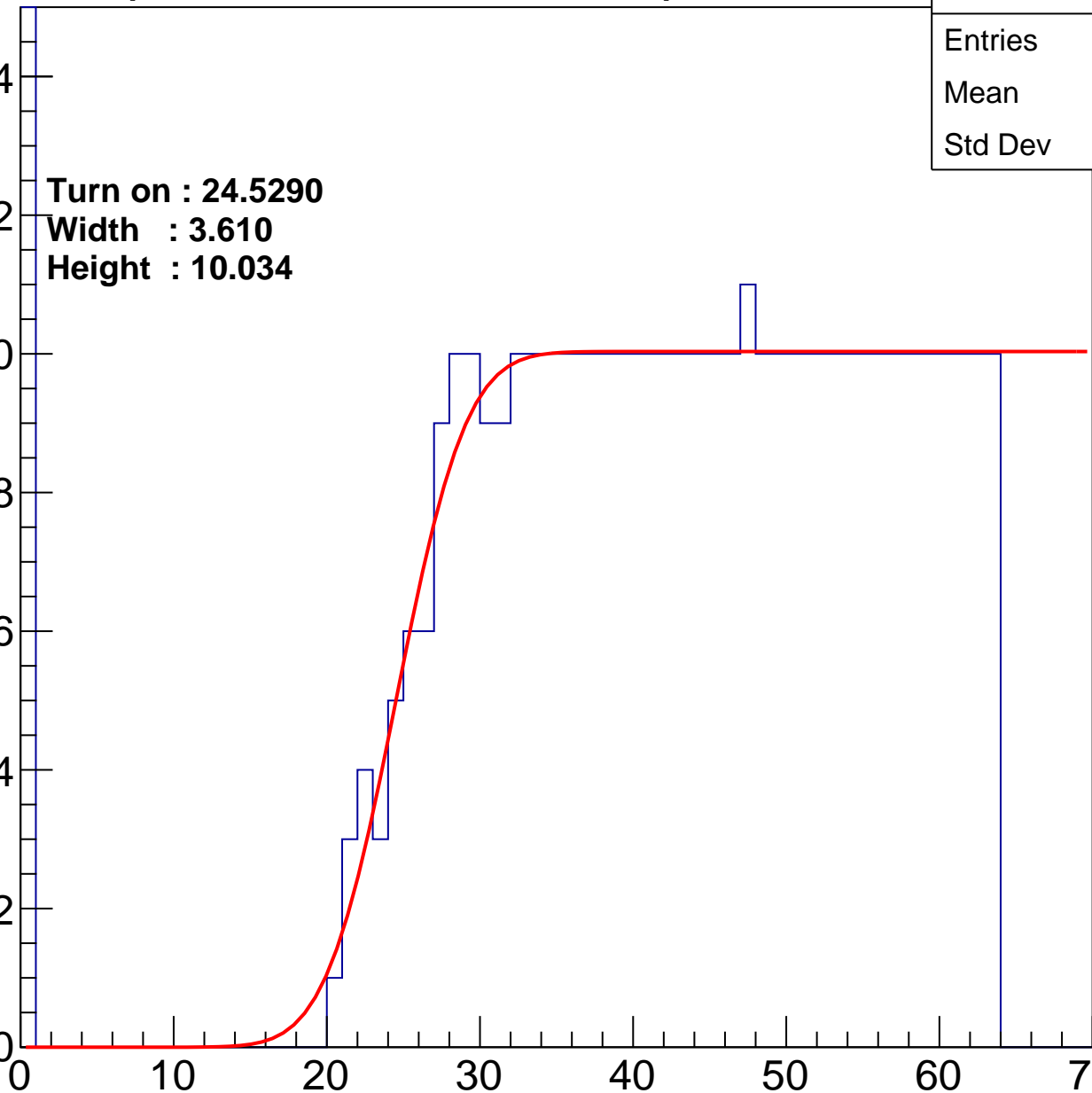
Width : 3.610

Height : 10.034

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U18-ch123

calib_packv5_041523_1651.root, FC#0, port C2

Entries	438
Mean	38.47
Std Dev	18.31

Turn on : 26.3826

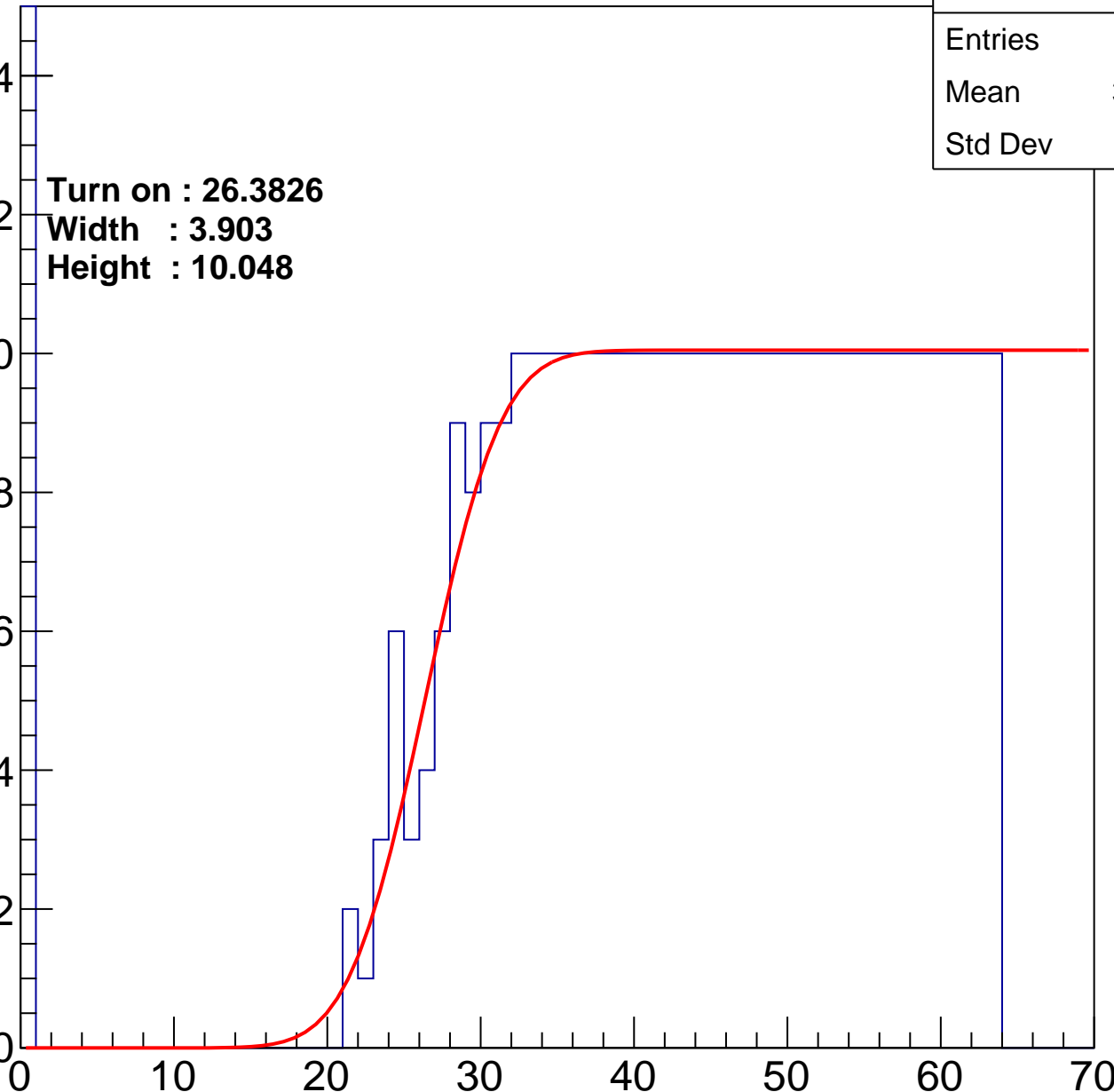
Width : 3.903

Height : 10.048

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U18-ch124

calib_packv5_041523_1651.root, FC#0, port C2

Entries	479
Mean	36.37
Std Dev	19.11

Turn on : 23.7187

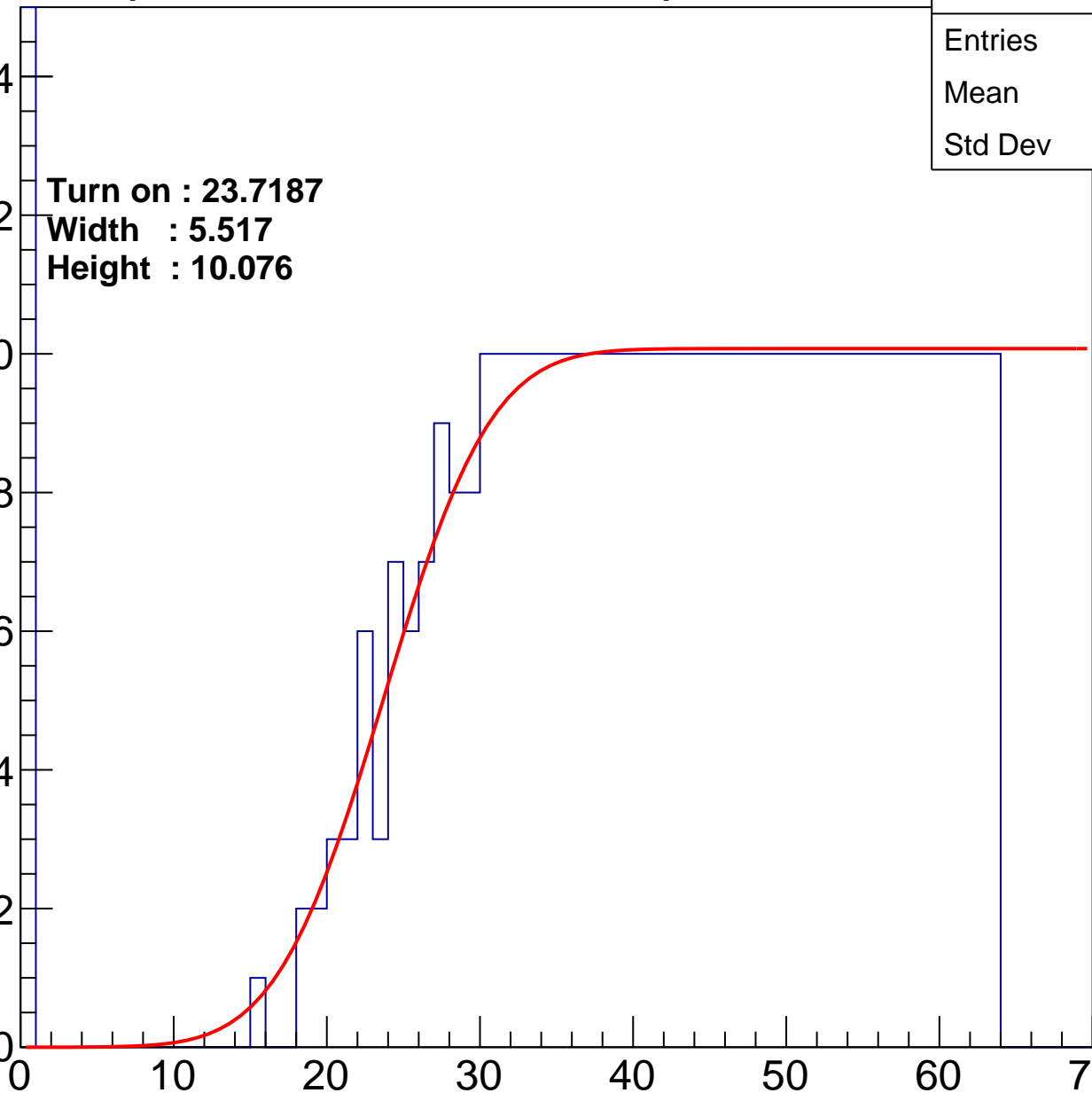
Width : 5.517

Height : 10.076

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U18-ch125

calib_packv5_041523_1651.root, FC#0, port C2

Entries	449
Mean	37.92
Std Dev	18.56

Turn on : 25.2461

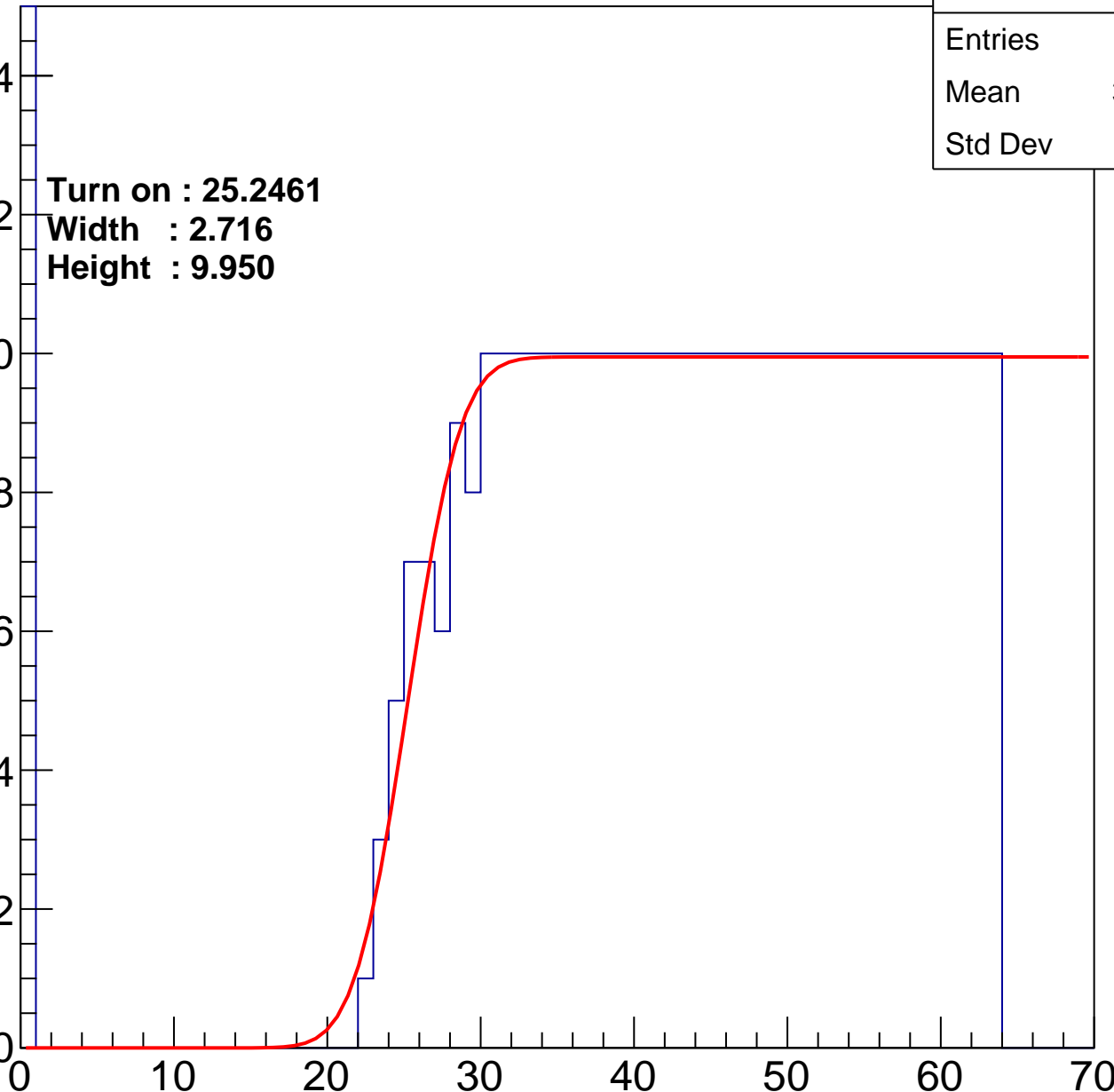
Width : 2.716

Height : 9.950

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U18-ch126

calib_packv5_041523_1651.root, FC#0, port C2

Entries	443
Mean	38.58
Std Dev	17.88

Turn on : 25.1053

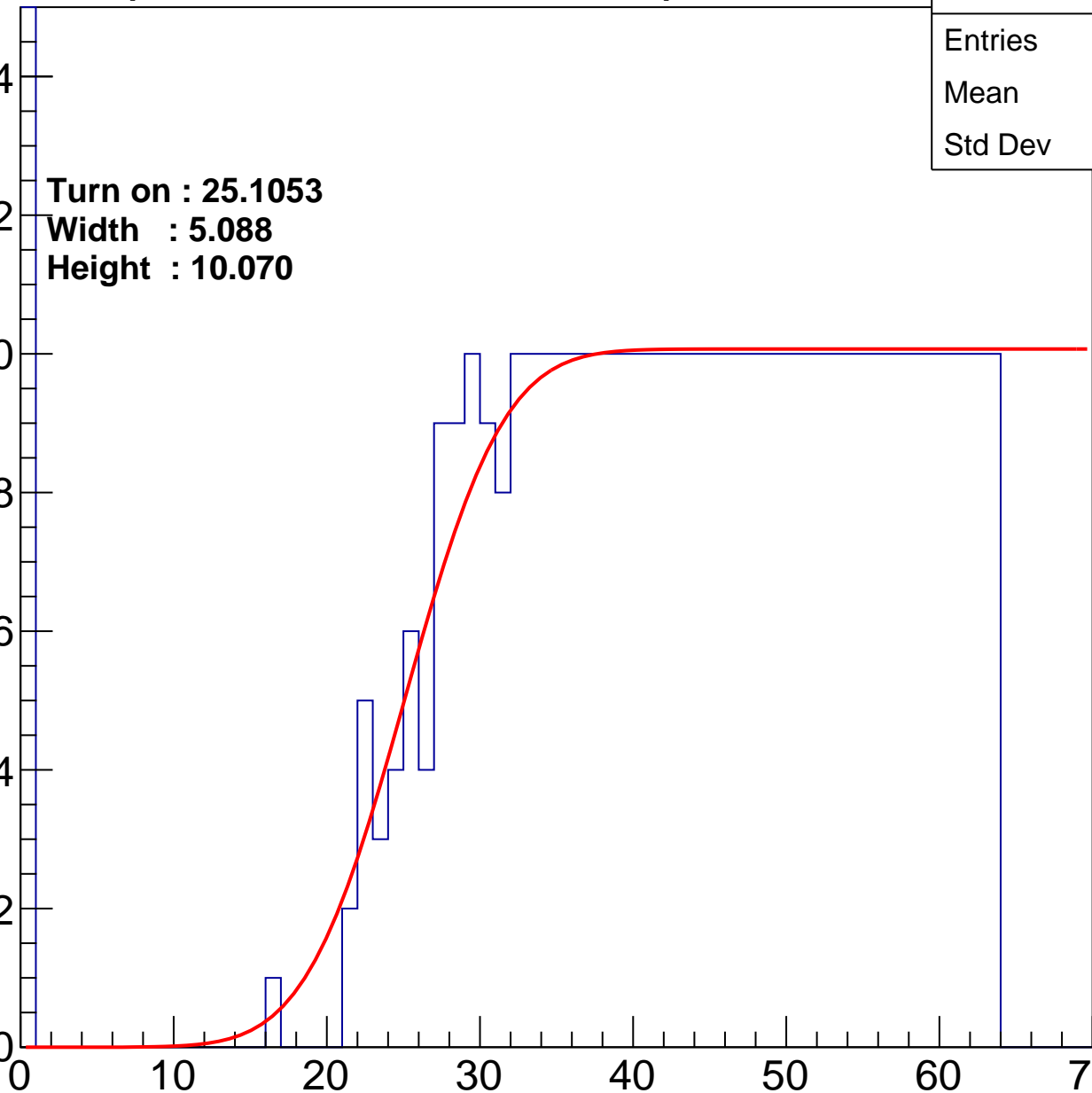
Width : 5.088

Height : 10.070

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U18-ch127

calib_packv5_041523_1651.root, FC#0, port C2

Entries	486
Mean	35.99
Std Dev	19.34

Turn on : 23.6291

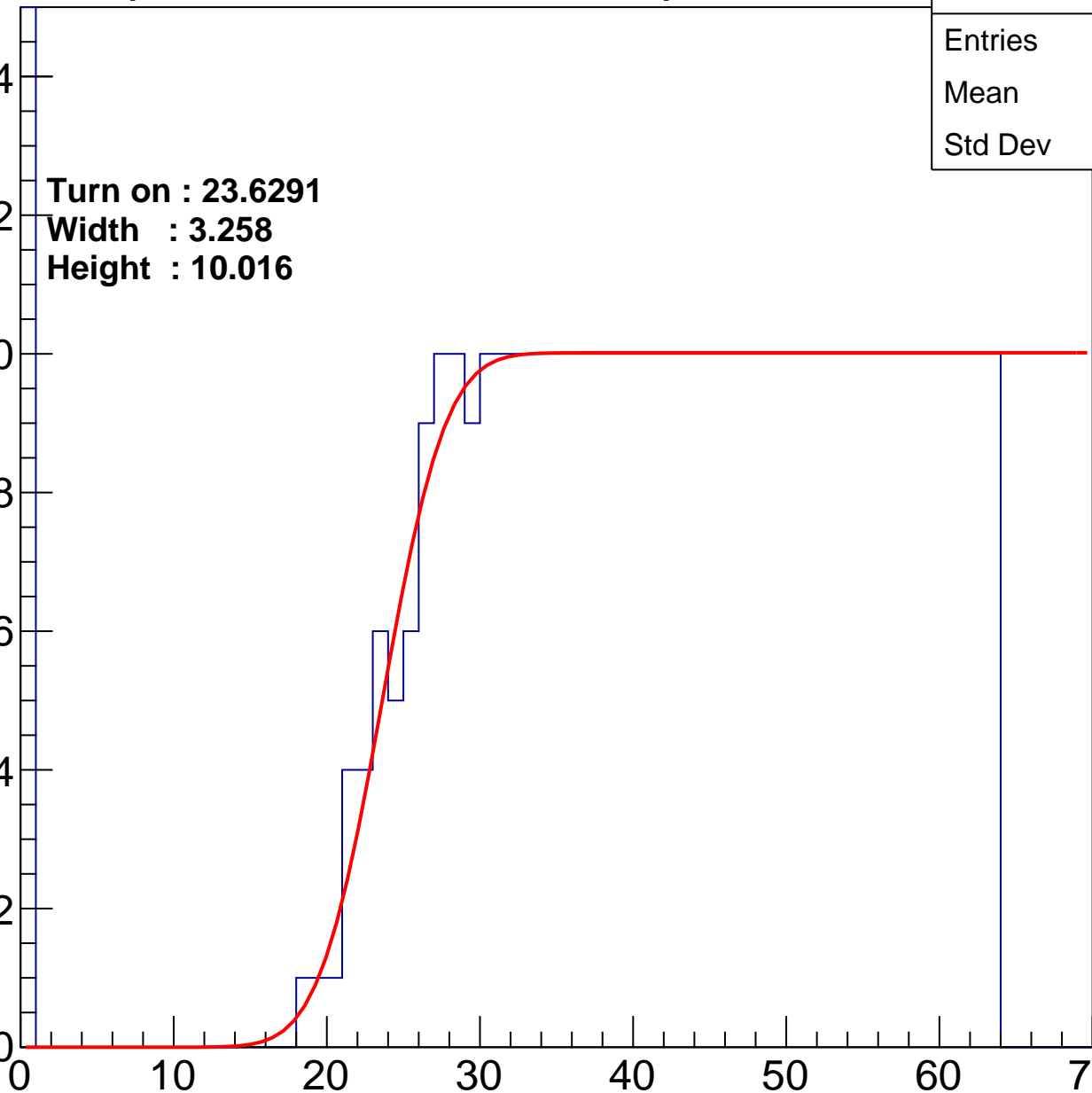
Width : 3.258

Height : 10.016

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U18-ch127

calib_packv5_041523_1651.root, FC#0, port C2

Entries	486
Mean	35.99
Std Dev	19.34

Turn on : 23.6291

Width : 3.258

Height : 10.016

Entry

14
12
10
8
6
4
2
0

ampl

