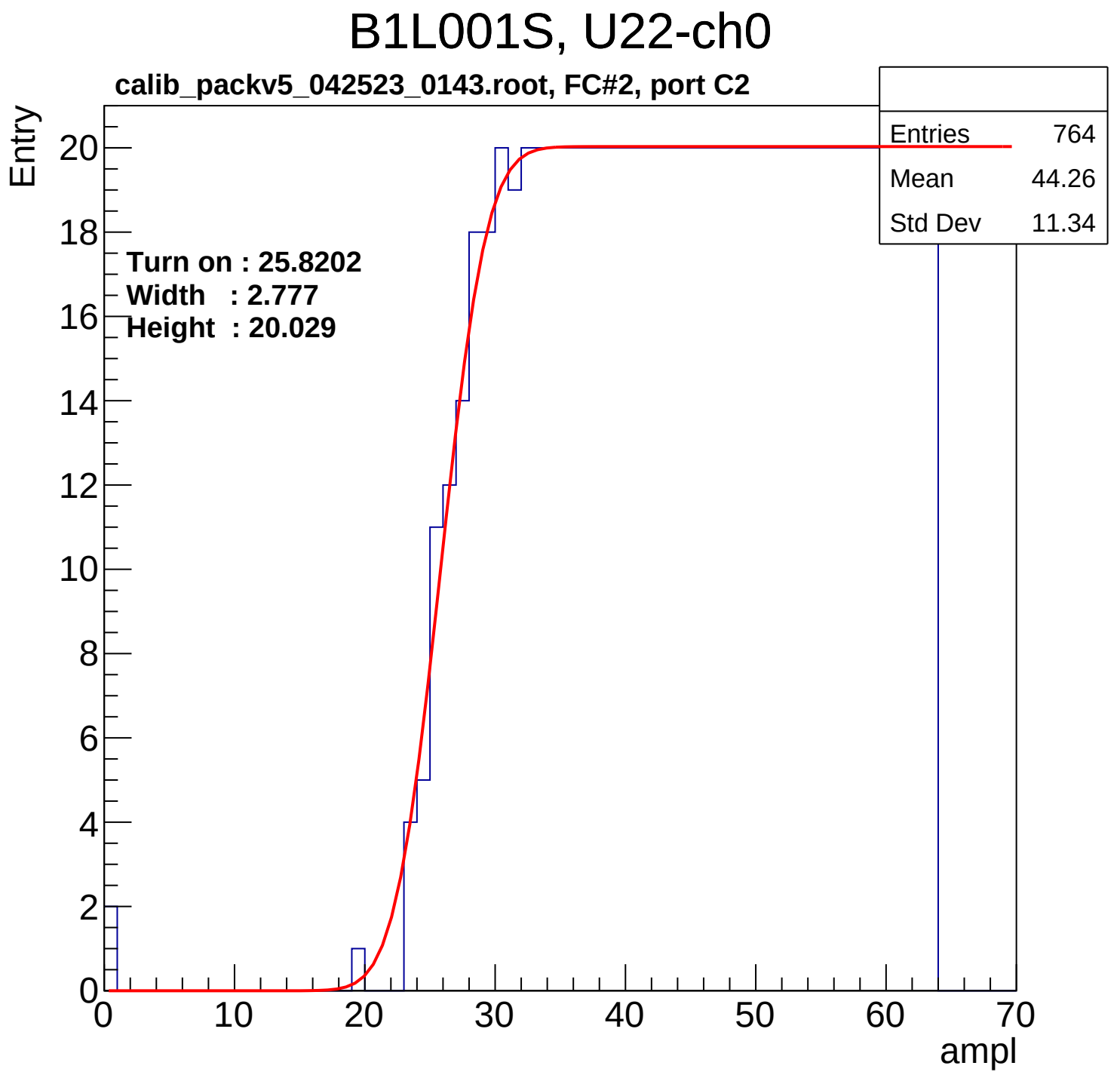
B1L001S, U22-ch0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 764
Mean 44.26
Std Dev 11.34
Turn on : 25.8202
Width : 2.777
Height : 20.029
Entry
ampl
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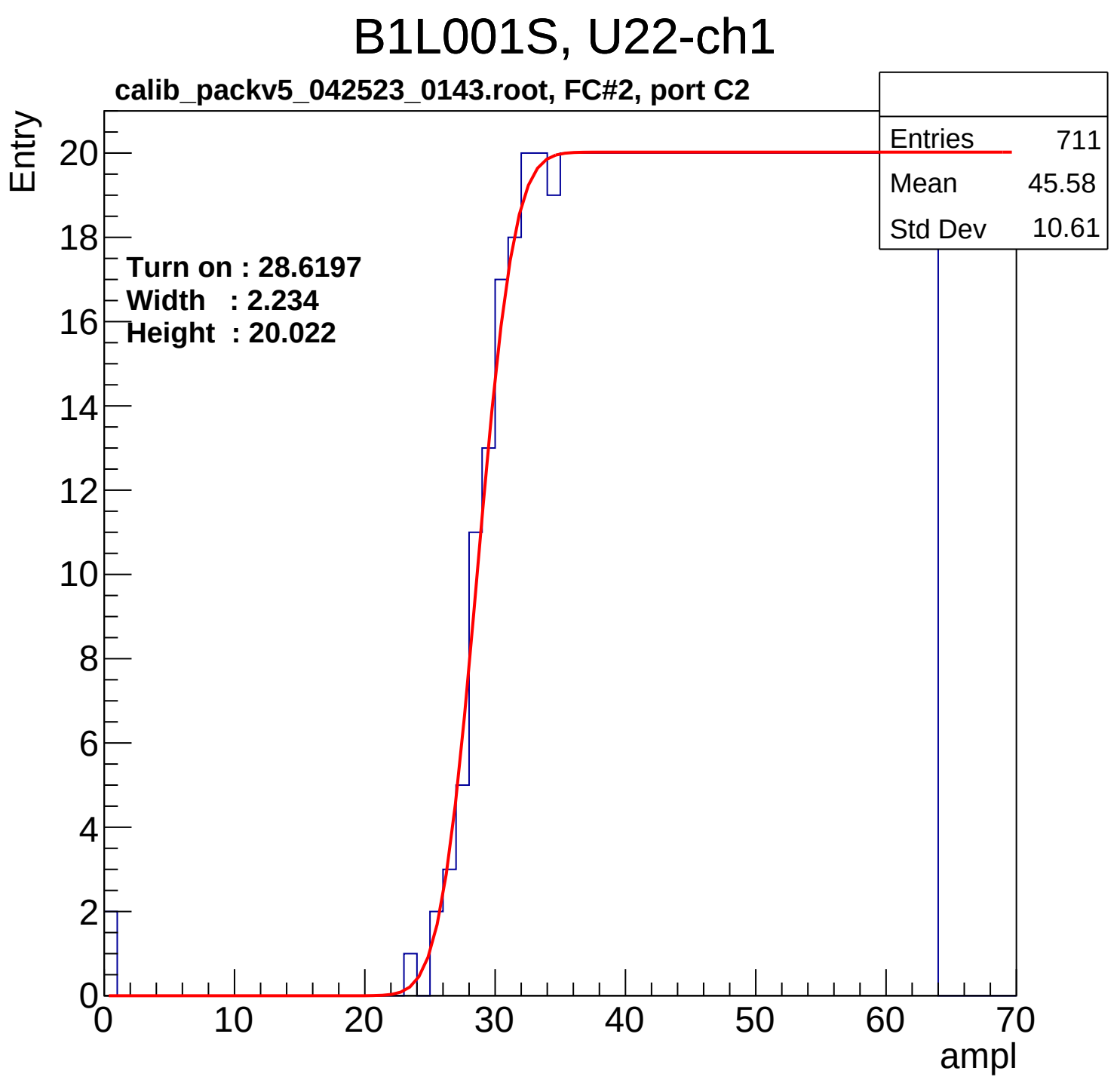
B1L001S, U22-ch1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 711
Mean 45.58
Std Dev 10.61
Turn on : 28.6197
Width : 2.234
Height : 20.022
Entry
ampl
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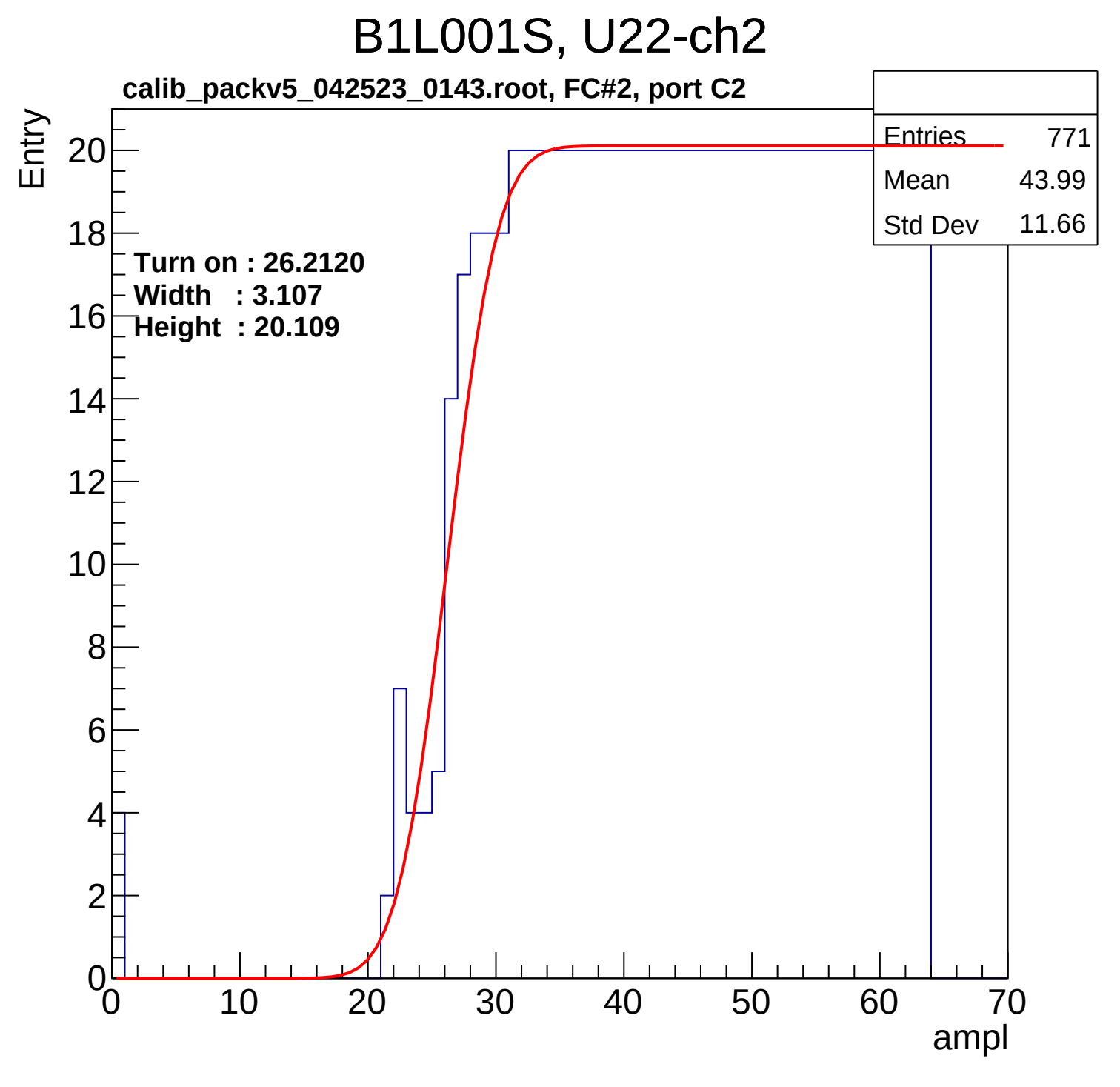
B1L001S, U22-ch2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 771
Mean 43.99
Std Dev 11.66
Turn on : 26.2120
Width : 3.107
Height : 20.109
Entry
ampl
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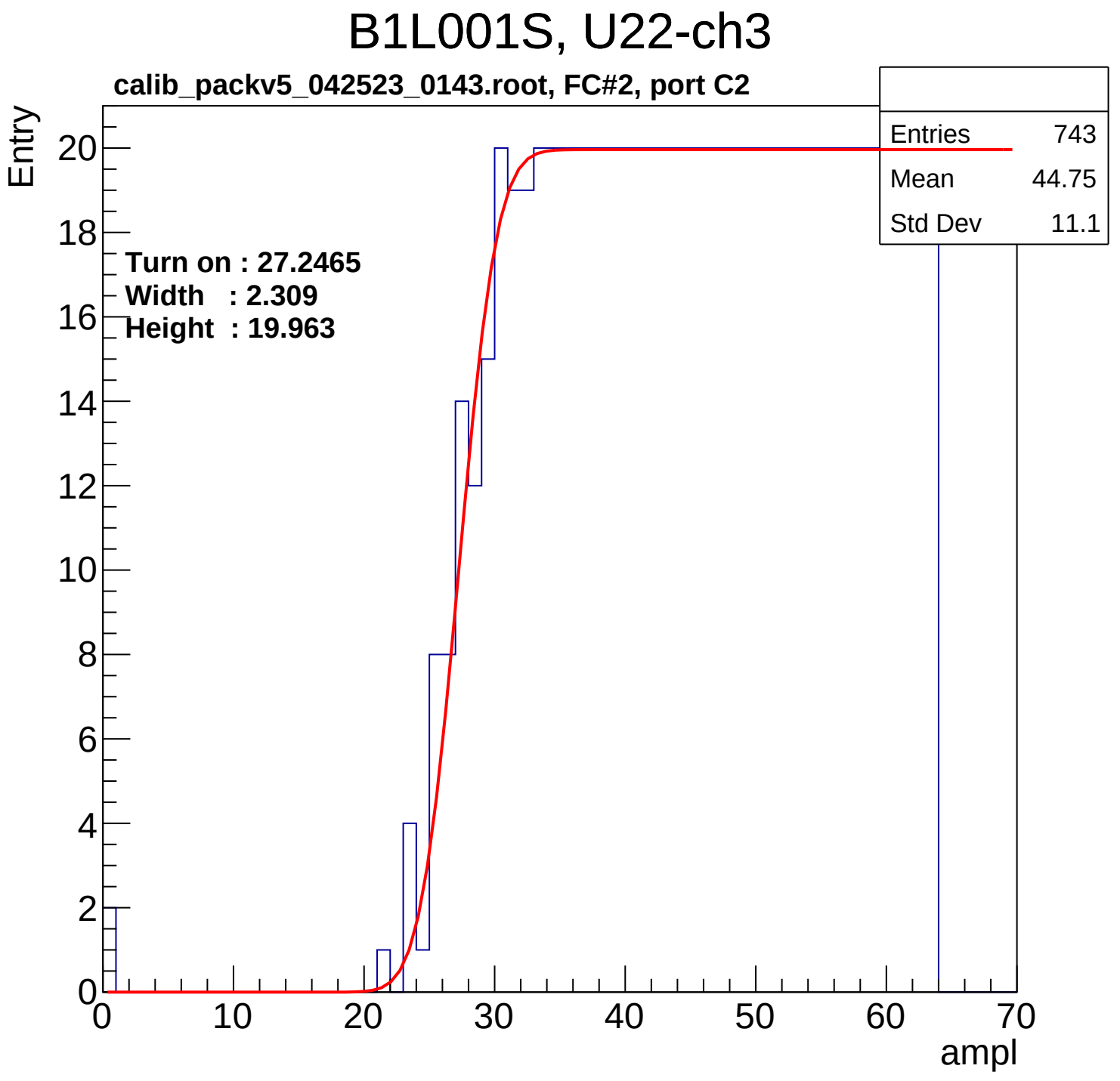
B1L001S, U22-ch3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 743
Mean 44.75
Std Dev 11.1
Turn on : 27.2465
Width : 2.309
Height : 19.963
Entry
ampl
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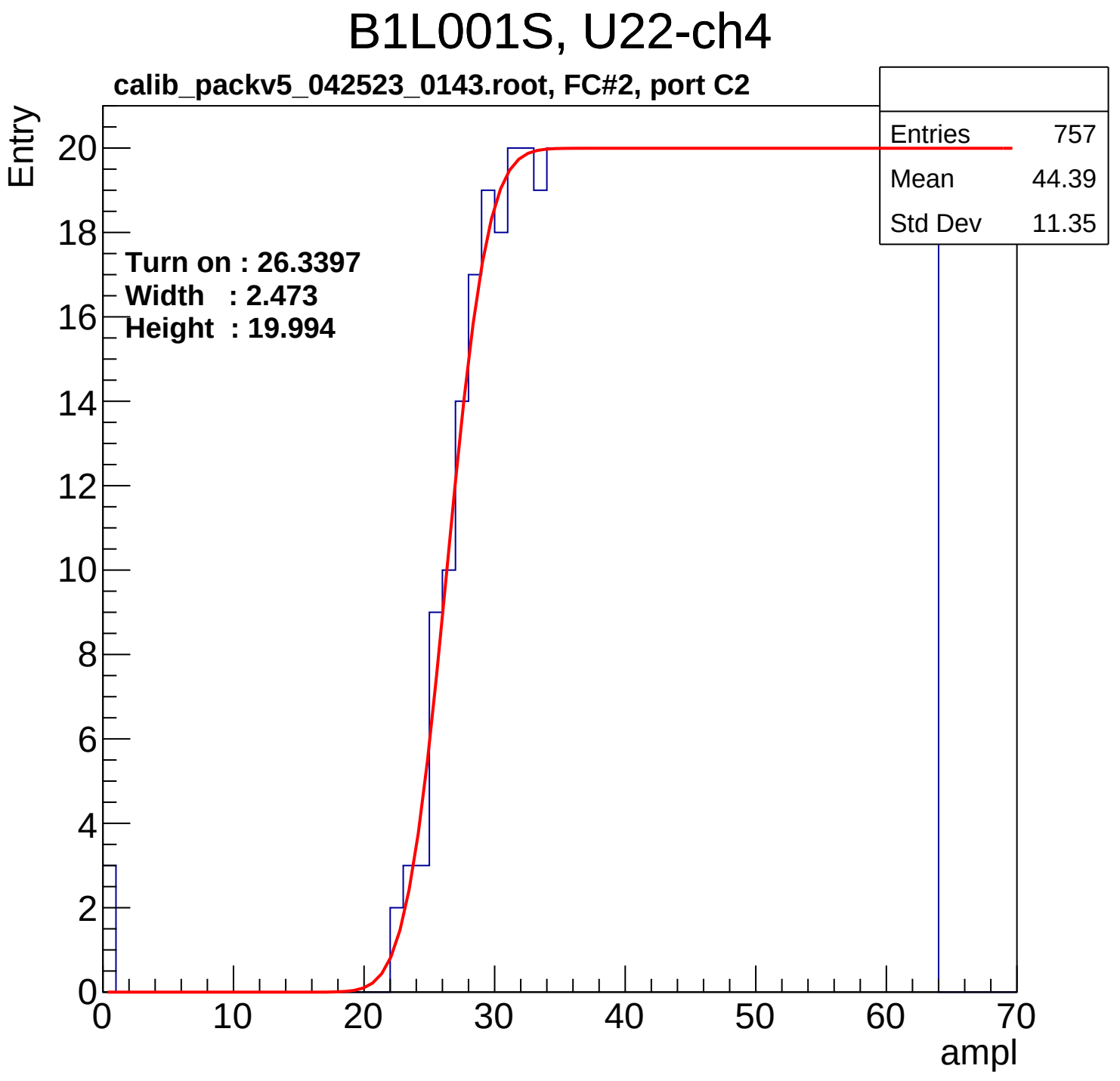
B1L001S, U22-ch4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 757
Mean 44.39
Std Dev 11.35
Turn on : 26.3397
Width : 2.473
Height : 19.994
Entry
ampl
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8
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14
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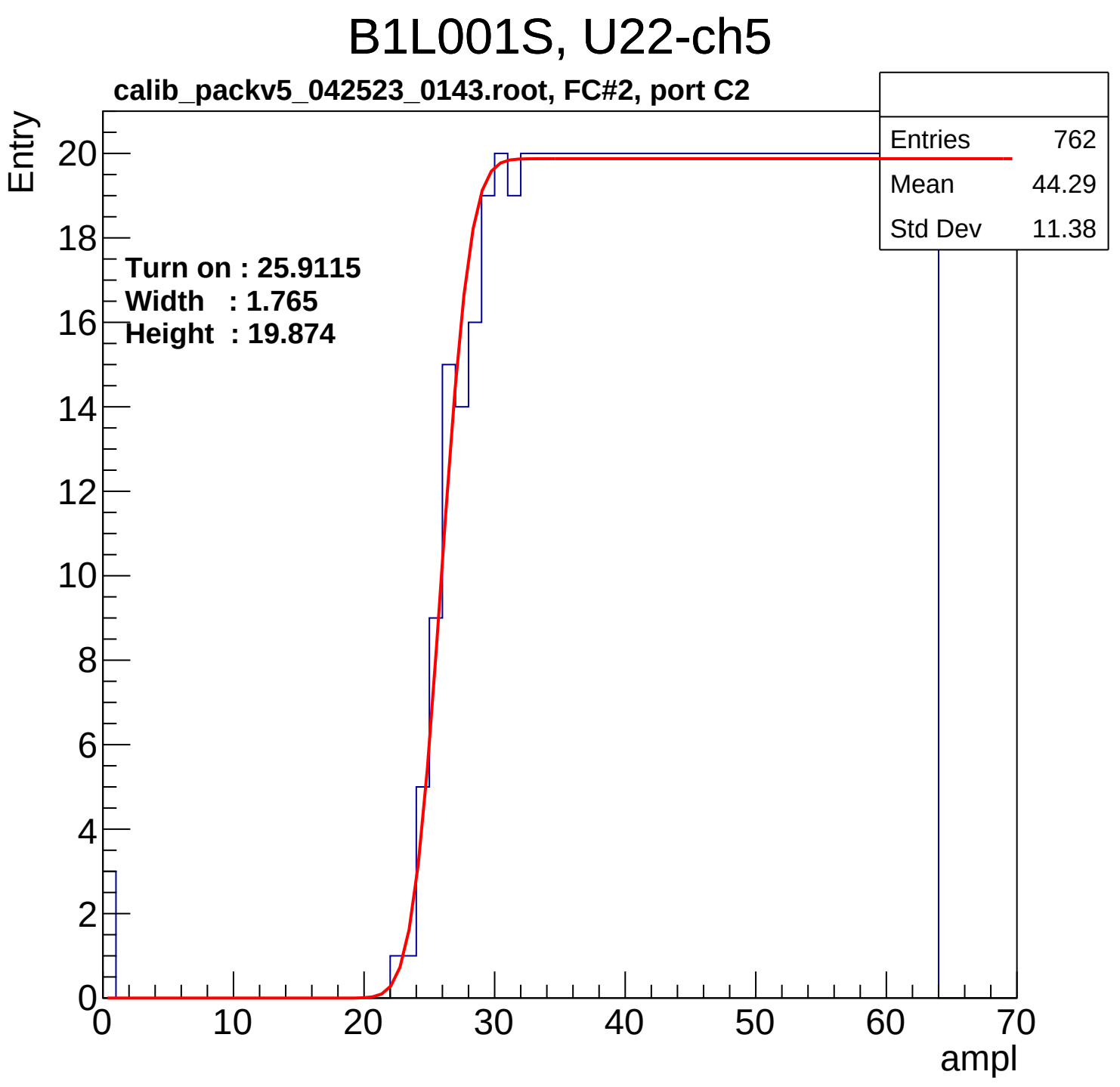
B1L001S, U22-ch5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 762
Mean 44.29
Std Dev 11.38
Turn on : 25.9115
Width : 1.765
Height : 19.874
Entry
ampl
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6
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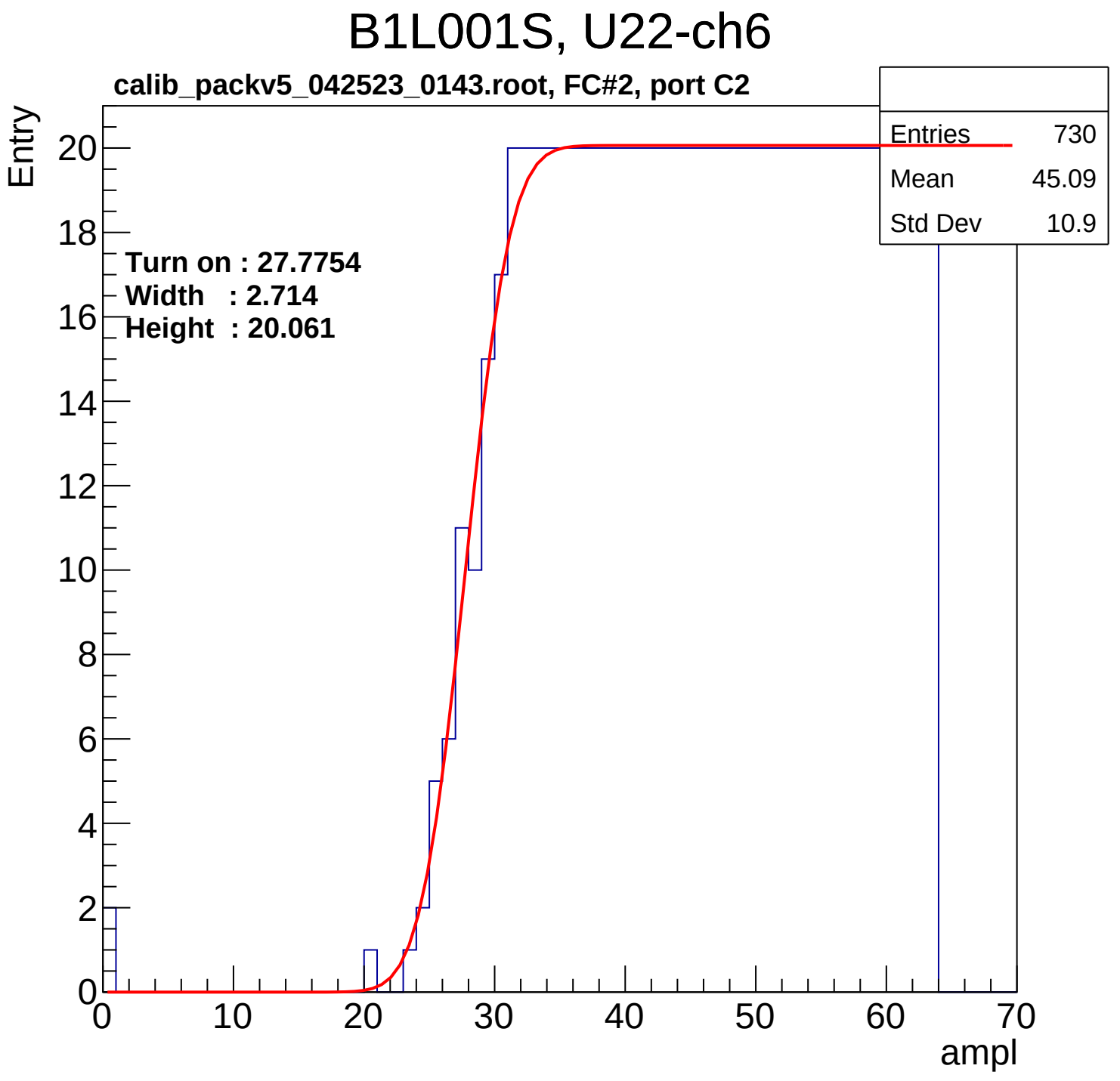
B1L001S, U22-ch6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 730
Mean 45.09
Std Dev 10.9
Turn on : 27.7754
Width : 2.714
Height : 20.061
Entry
ampl
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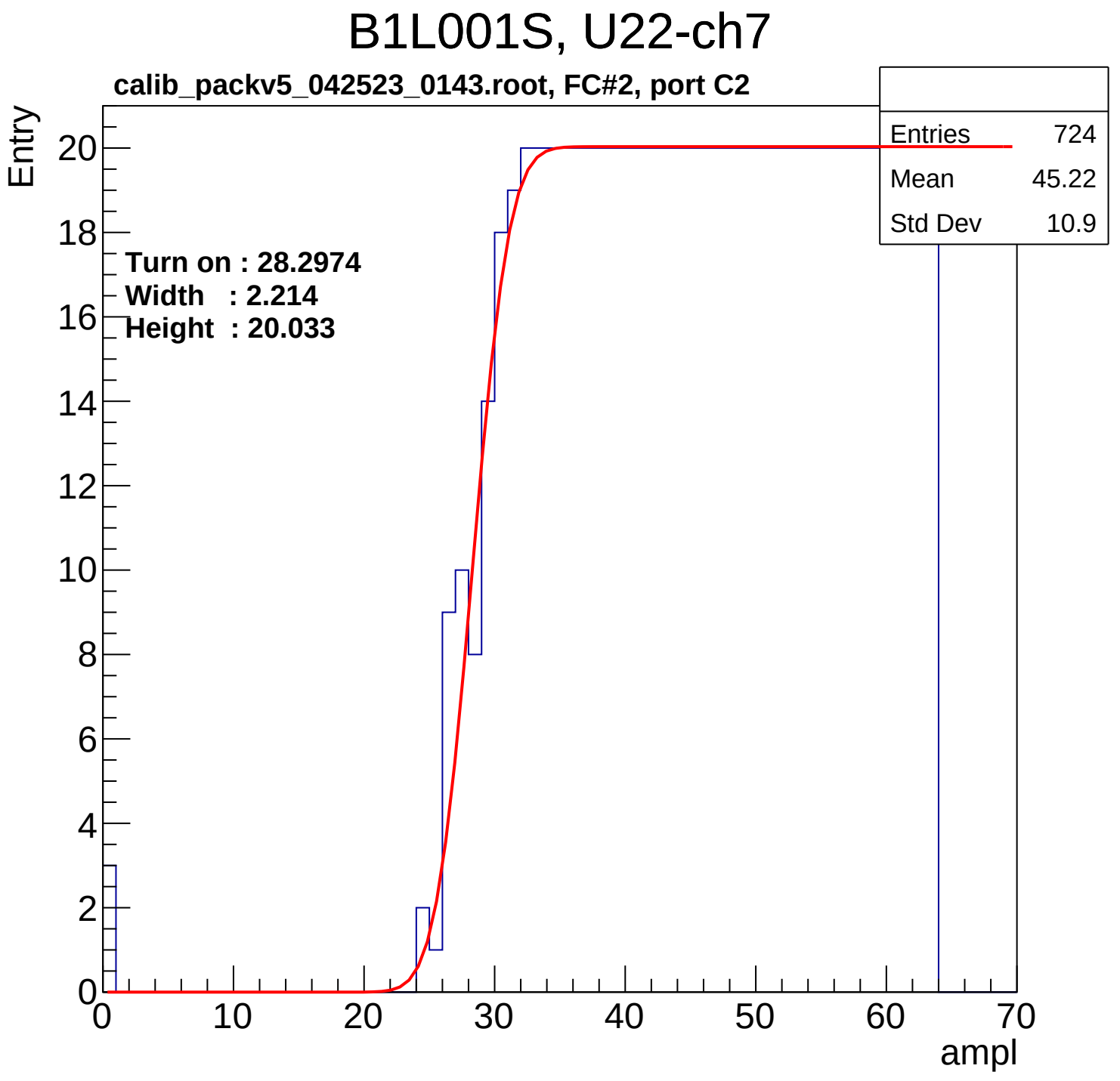
B1L001S, U22-ch7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 724
Mean 45.22
Std Dev 10.9
Turn on : 28.2974
Width : 2.214
Height : 20.033
Entry
ampl
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6
8
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12
14
16
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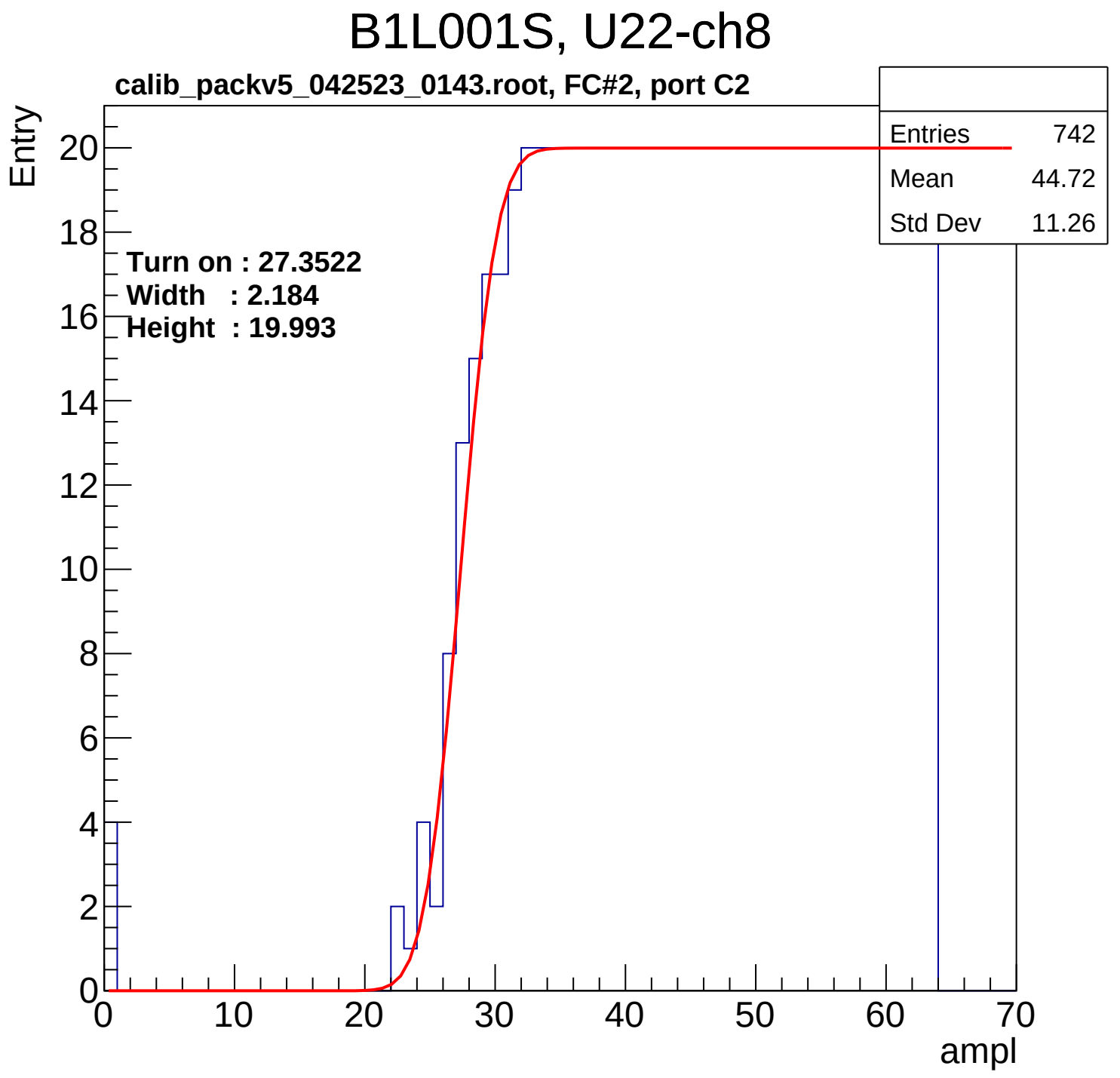
B1L001S, U22-ch8
calib_packv5_042523_0143.root, FC#2, port C2
Entries 742
Mean 44.72
Std Dev 11.26
Turn on : 27.3522
Width : 2.184
Height : 19.993
Entry
ampl
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6
8
10
12
14
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0
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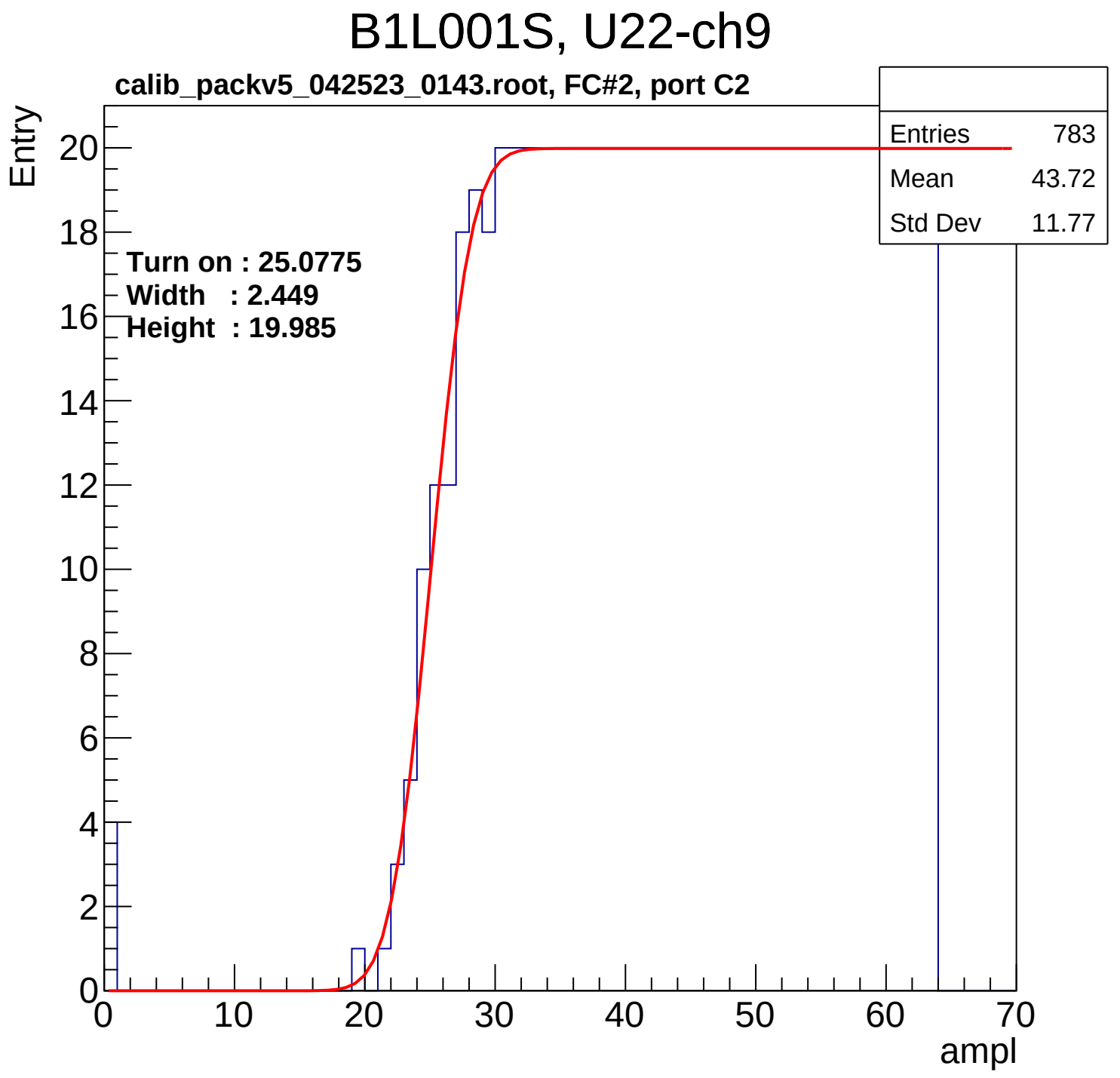
B1L001S, U22-ch9
calib_packv5_042523_0143.root, FC#2, port C2
Entries 783
Mean 43.72
Std Dev 11.77
Turn on : 25.0775
Width : 2.449
Height : 19.985
Entry
ampl
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6
8
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14
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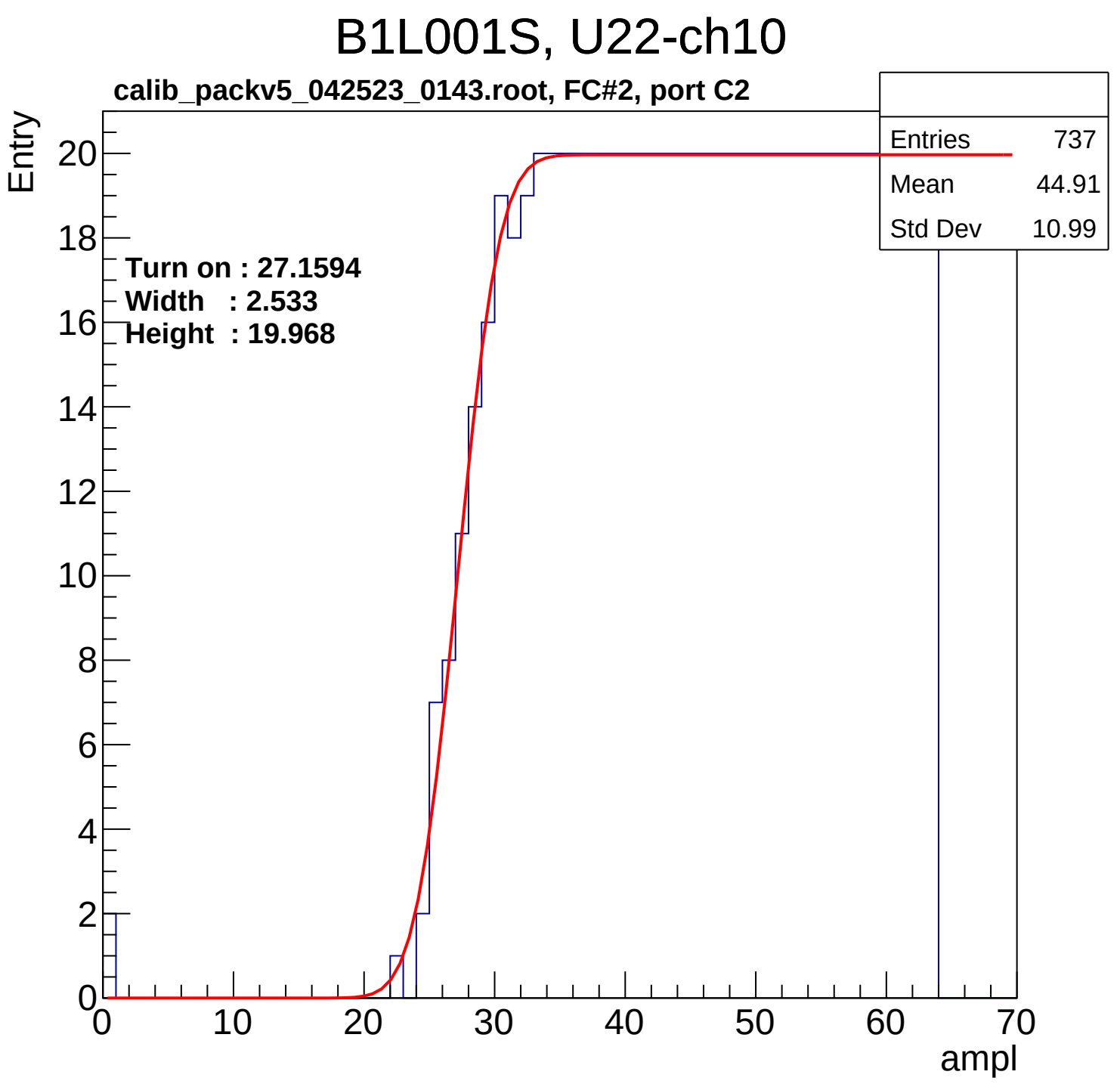
B1L001S, U22-ch10
calib_packv5_042523_0143.root, FC#2, port C2
Entries 737
Mean 44.91
Std Dev 10.99
Turn on : 27.1594
Width : 2.533
Height : 19.968
Entry
ampl
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6
8
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12
14
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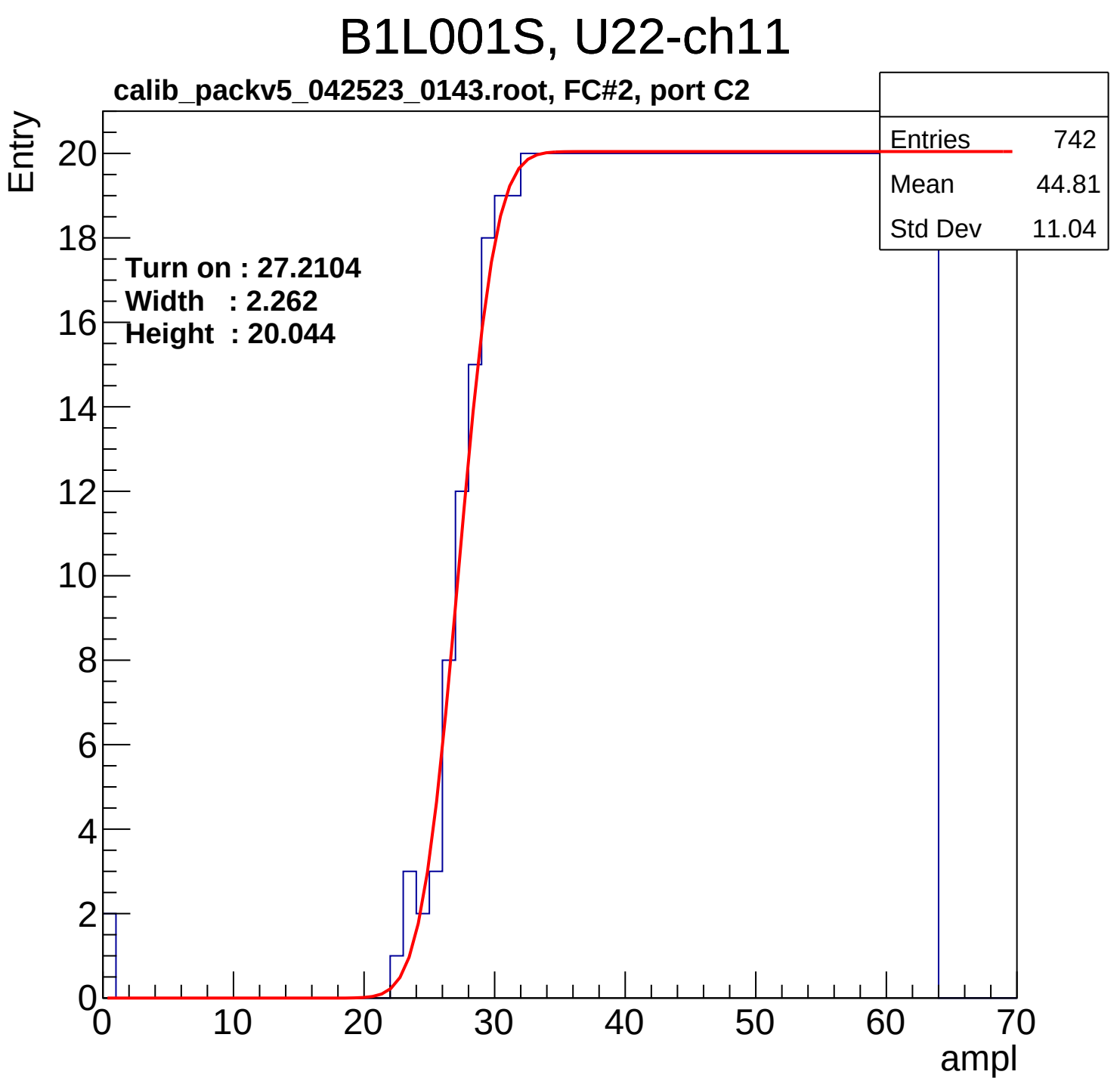
B1L001S, U22-ch11
calib_packv5_042523_0143.root, FC#2, port C2
Entries 742
Mean 44.81
Std Dev 11.04
Turn on : 27.2104
Width : 2.262
Height : 20.044
Entry
ampl
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6
8
10
12
14
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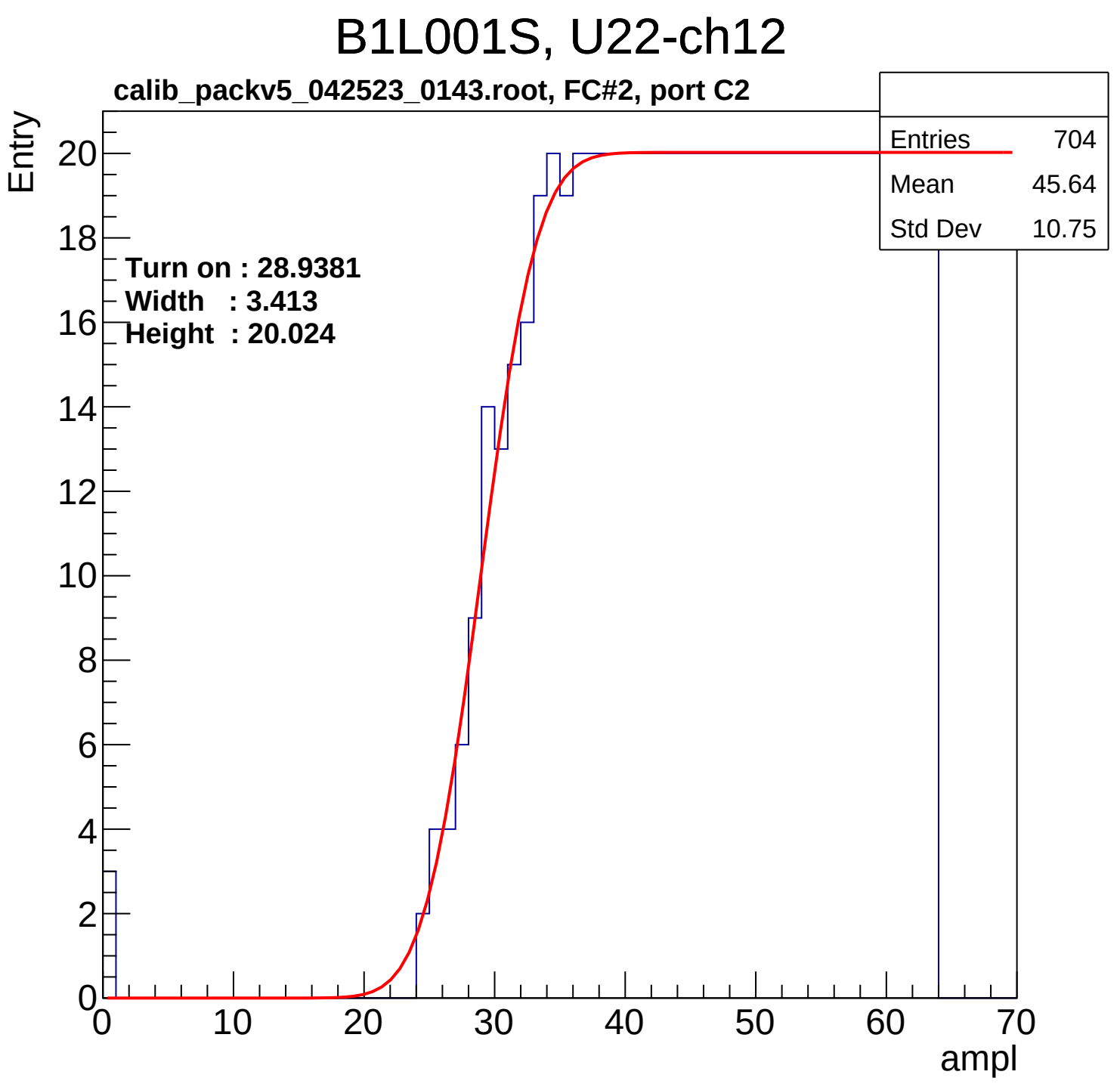
B1L001S, U22-ch12
calib_packv5_042523_0143.root, FC#2, port C2
Entries 704
Mean 45.64
Std Dev 10.75
Turn on : 28.9381
Width : 3.413
Height : 20.024
Entry
ampl
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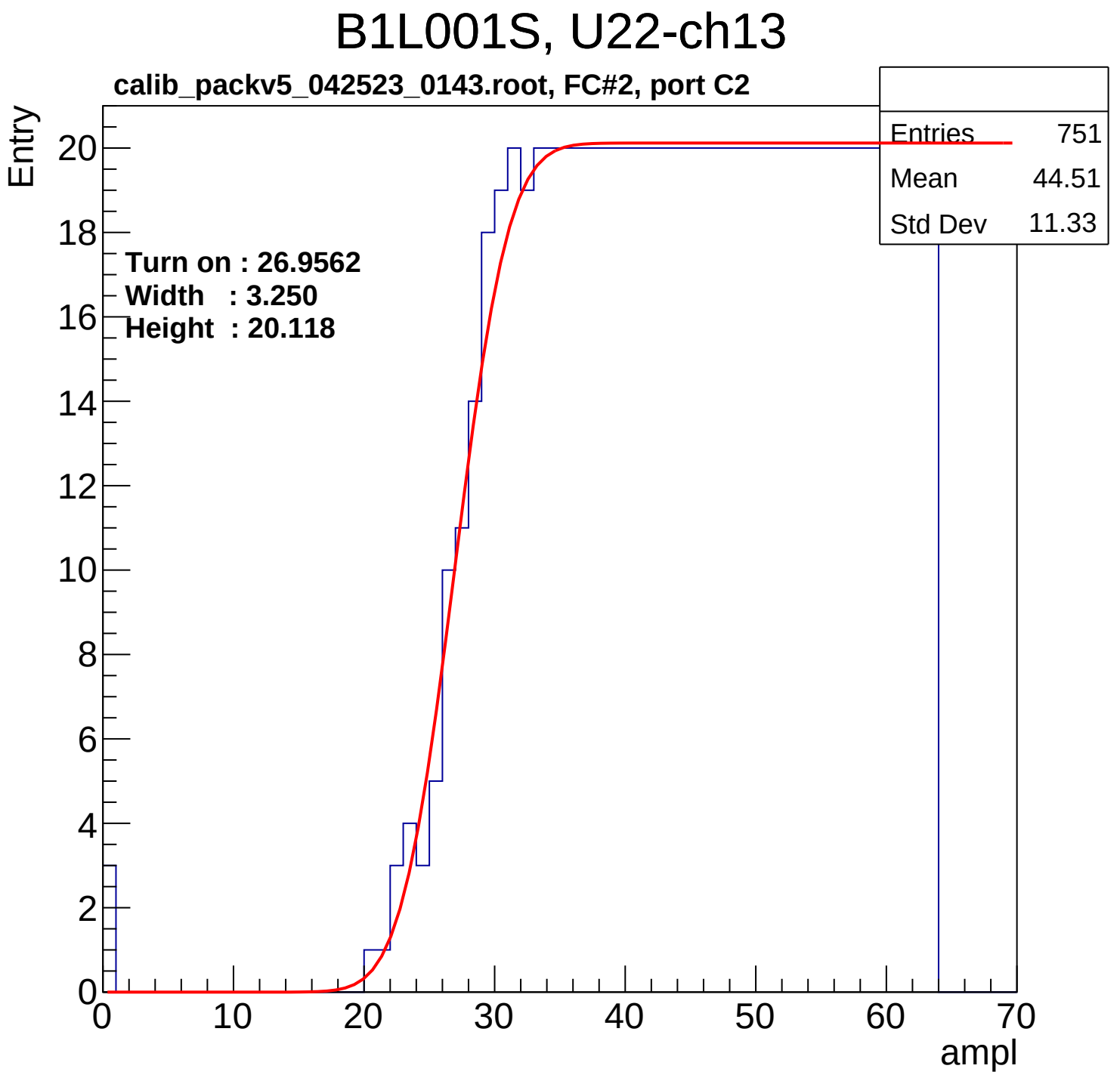
B1L001S, U22-ch13
calib_packv5_042523_0143.root, FC#2, port C2
Entries 751
Mean 44.51
Std Dev 11.33
Turn on : 26.9562
Width : 3.250
Height : 20.118
Entry
ampl
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10
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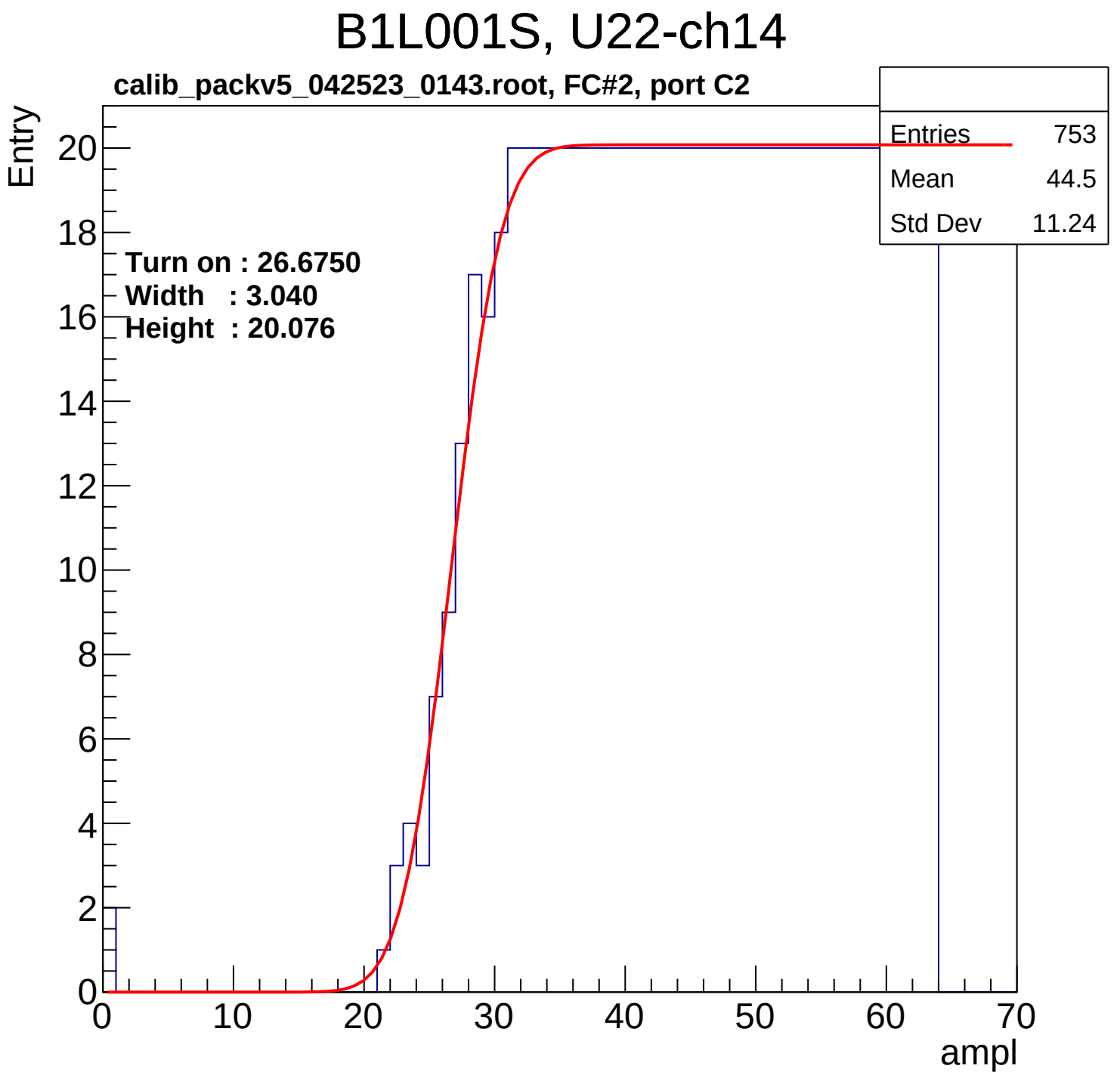
B1L001S, U22-ch14
calib_packv5_042523_0143.root, FC#2, port C2
Entries 753
Mean 44.5
Std Dev 11.24
Turn on : 26.6750
Width : 3.040
Height : 20.076
Entry
ampl
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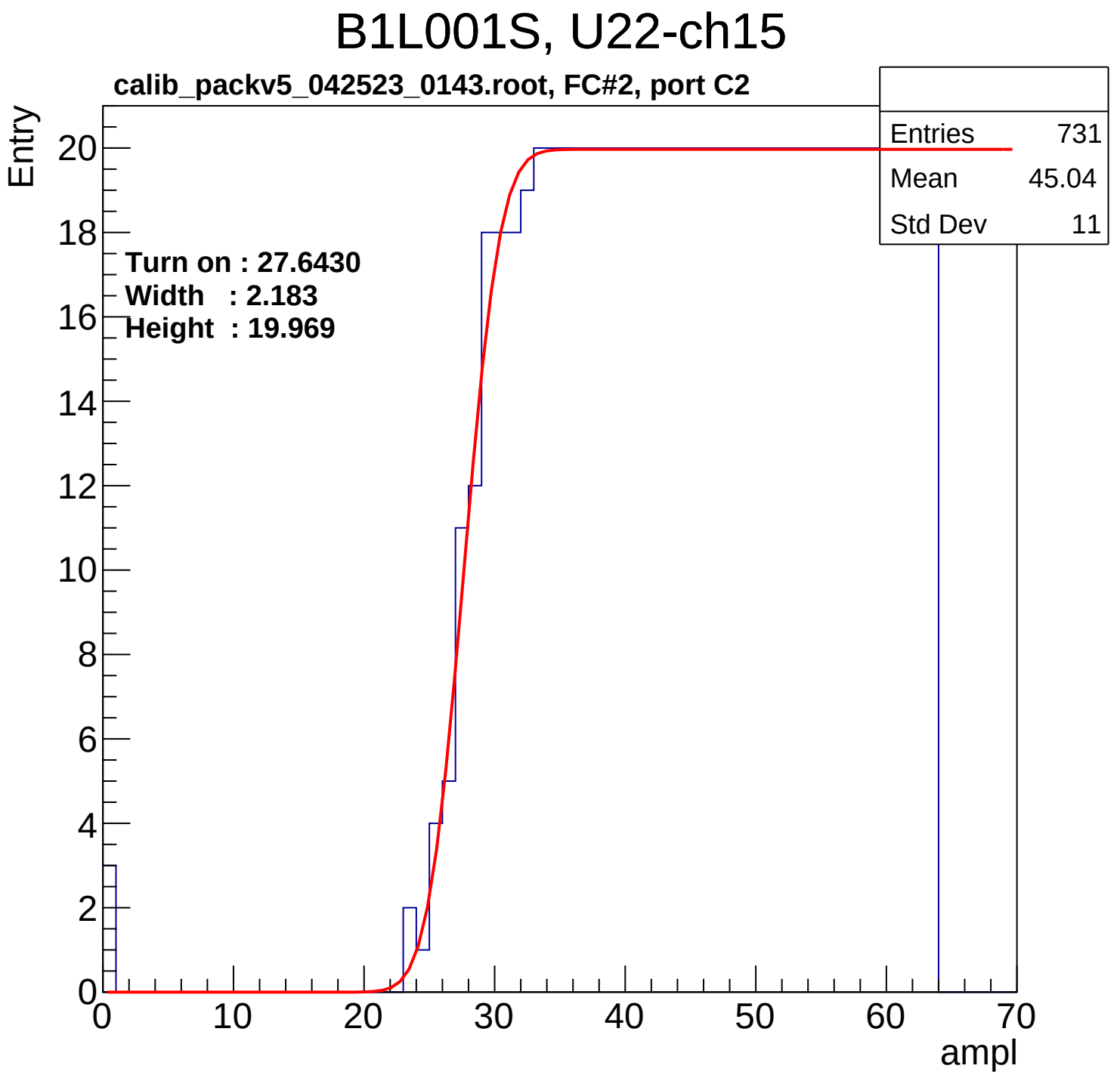
B1L001S, U22-ch15
calib_packv5_042523_0143.root, FC#2, port C2
Entries 731
Mean 45.04
Std Dev 11
Turn on : 27.6430
Width : 2.183
Height : 19.969
Entry
ampl
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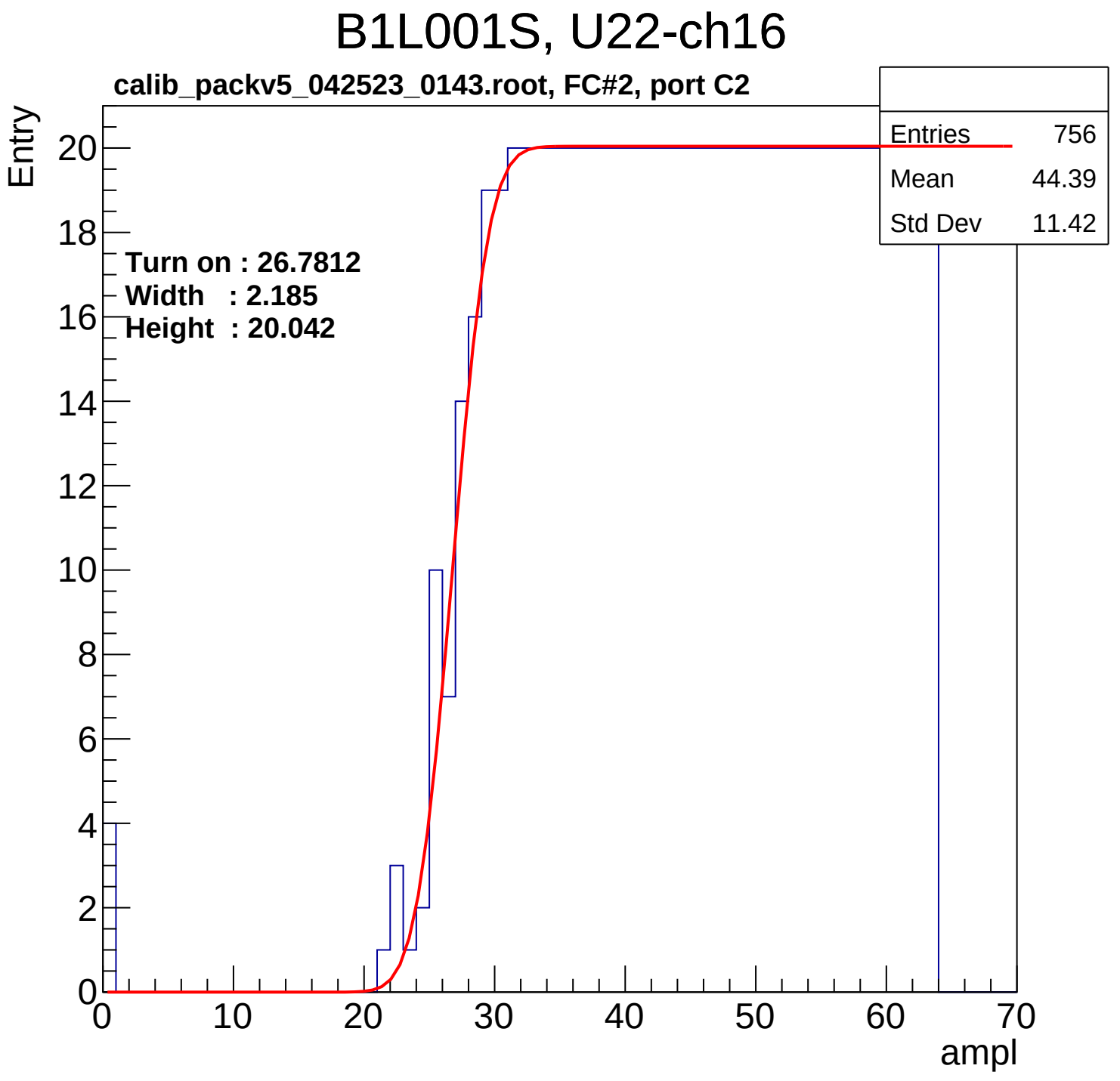
B1L001S, U22-ch16
calib_packv5_042523_0143.root, FC#2, port C2
Entries 756
Mean 44.39
Std Dev 11.42
Turn on : 26.7812
Width : 2.185
Height : 20.042
Entry
ampl
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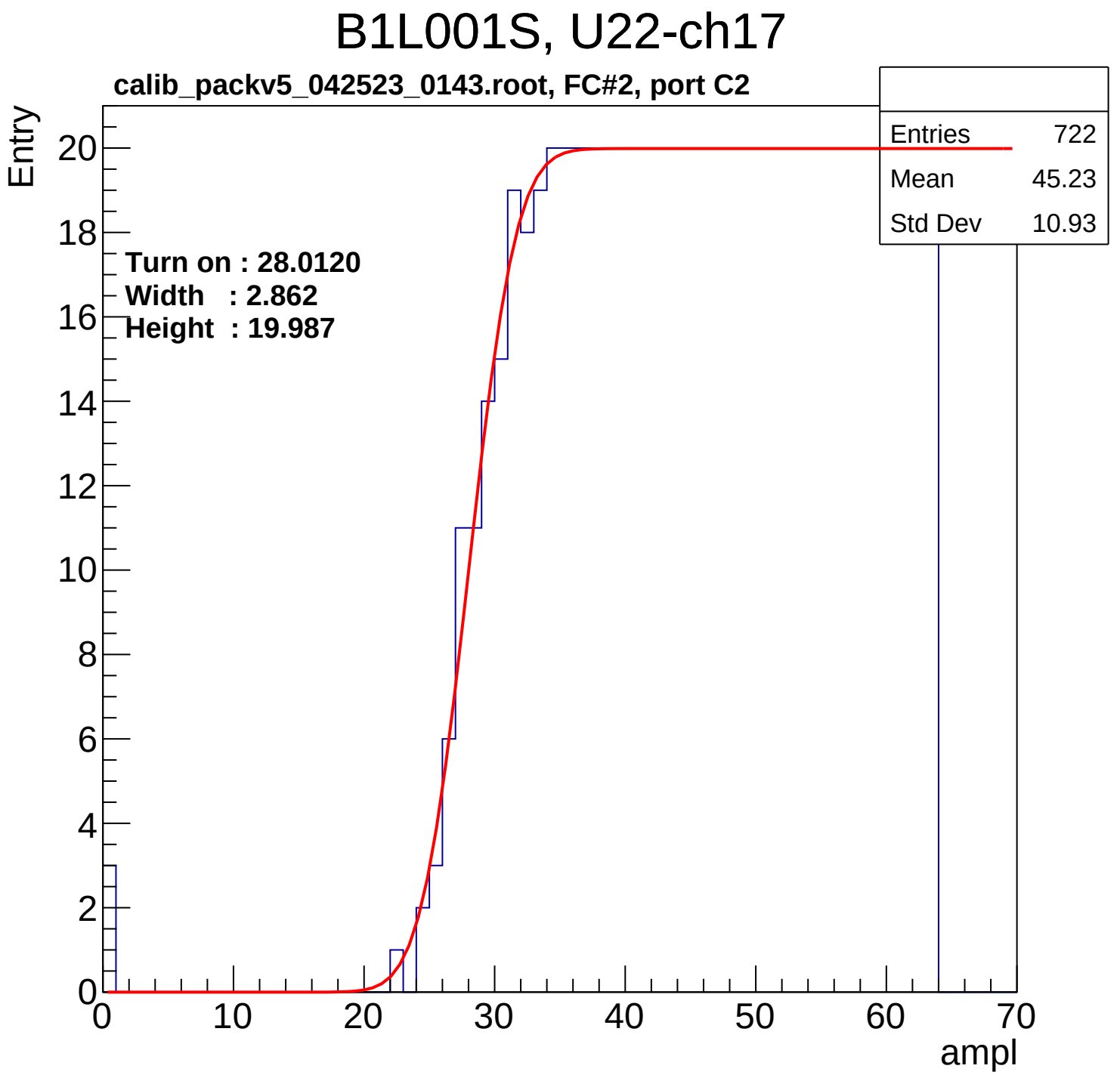
B1L001S, U22-ch17
calib_packv5_042523_0143.root, FC#2, port C2
Entries 722
Mean 45.23
Std Dev 10.93
Turn on : 28.0120
Width : 2.862
Height : 19.987
Entry
ampl
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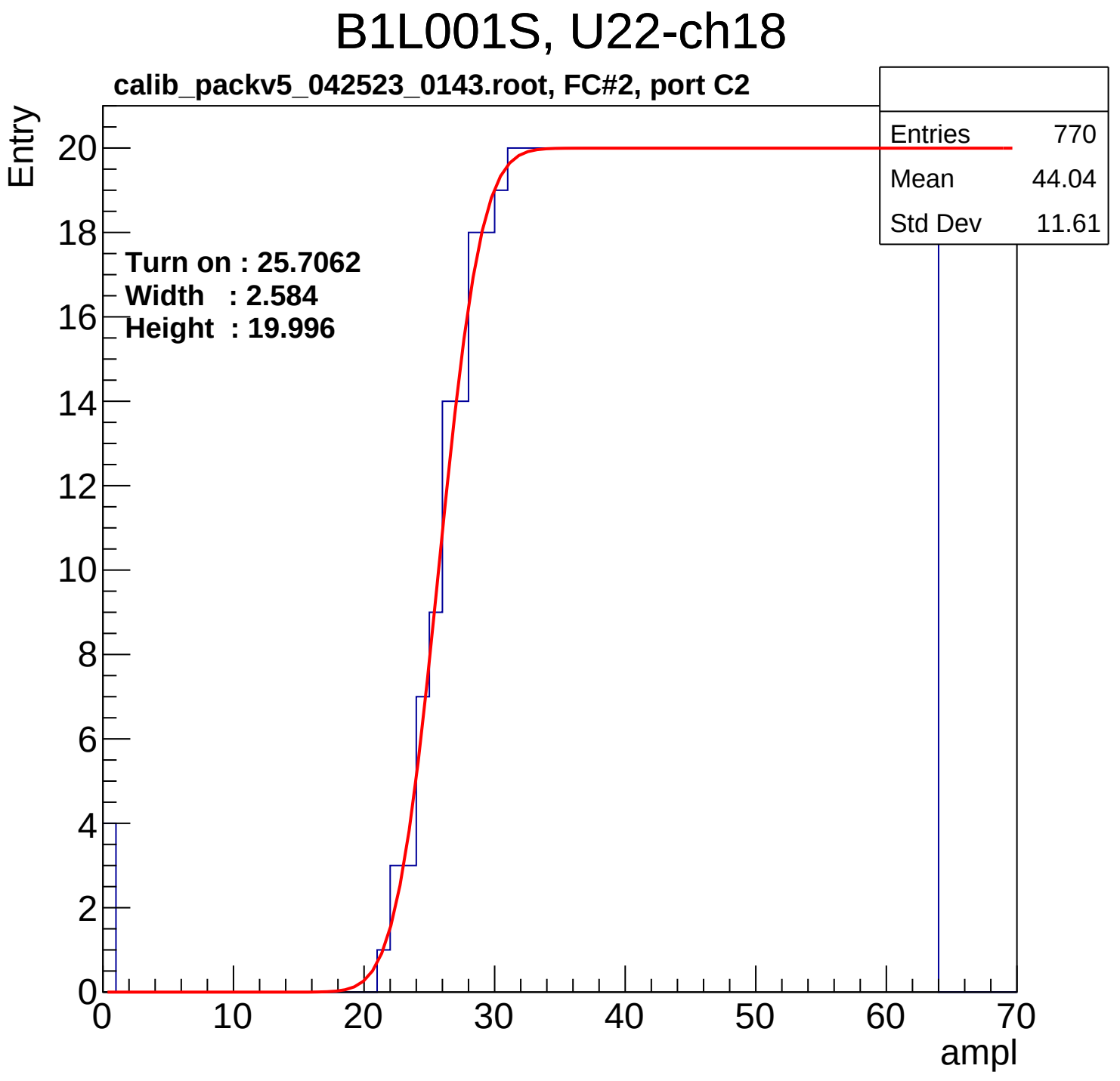
B1L001S, U22-ch18
calib_packv5_042523_0143.root, FC#2, port C2
Entries 770
Mean 44.04
Std Dev 11.61
Turn on : 25.7062
Width : 2.584
Height : 19.996
Entry
ampl
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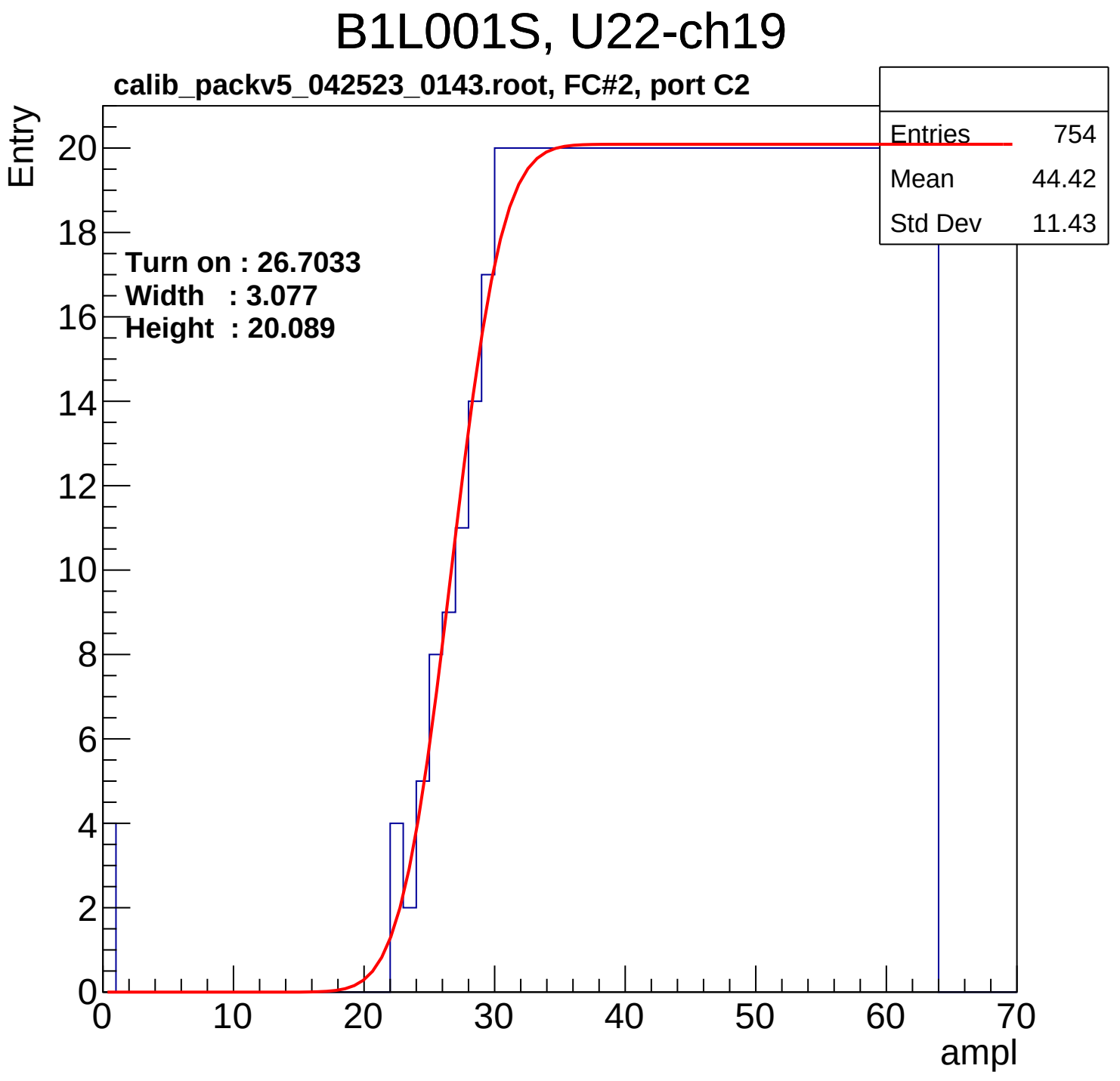
B1L001S, U22-ch19
calib_packv5_042523_0143.root, FC#2, port C2
Entries 754
Mean 44.42
Std Dev 11.43
Turn on : 26.7033
Width : 3.077
Height : 20.089
Entry
ampl
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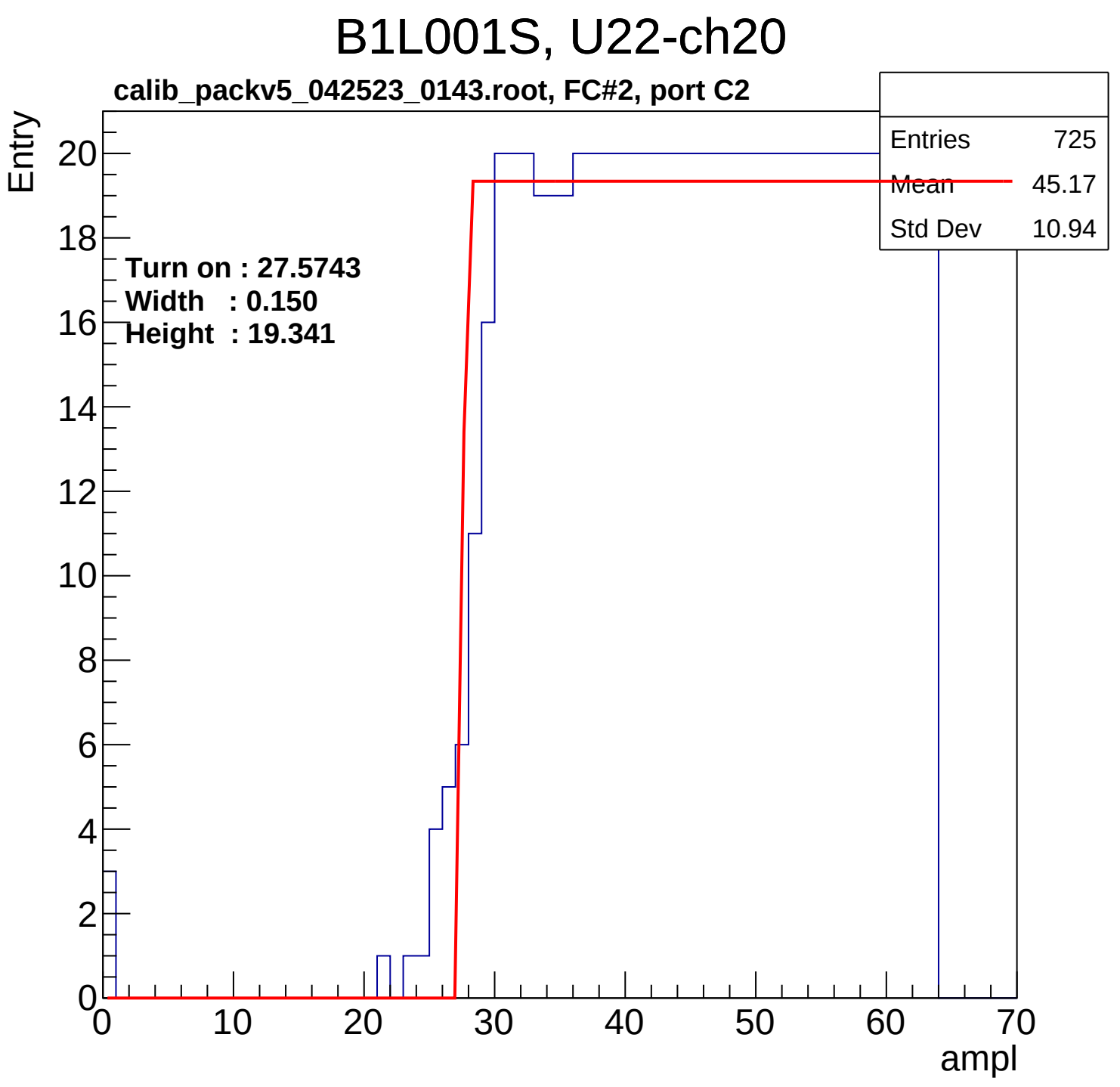
B1L001S, U22-ch20
calib_packv5_042523_0143.root, FC#2, port C2
Entries 725
Mean 45.17
Std Dev 10.94
Turn on : 27.5743
Width : 0.150
Height : 19.341
Entry
ampl
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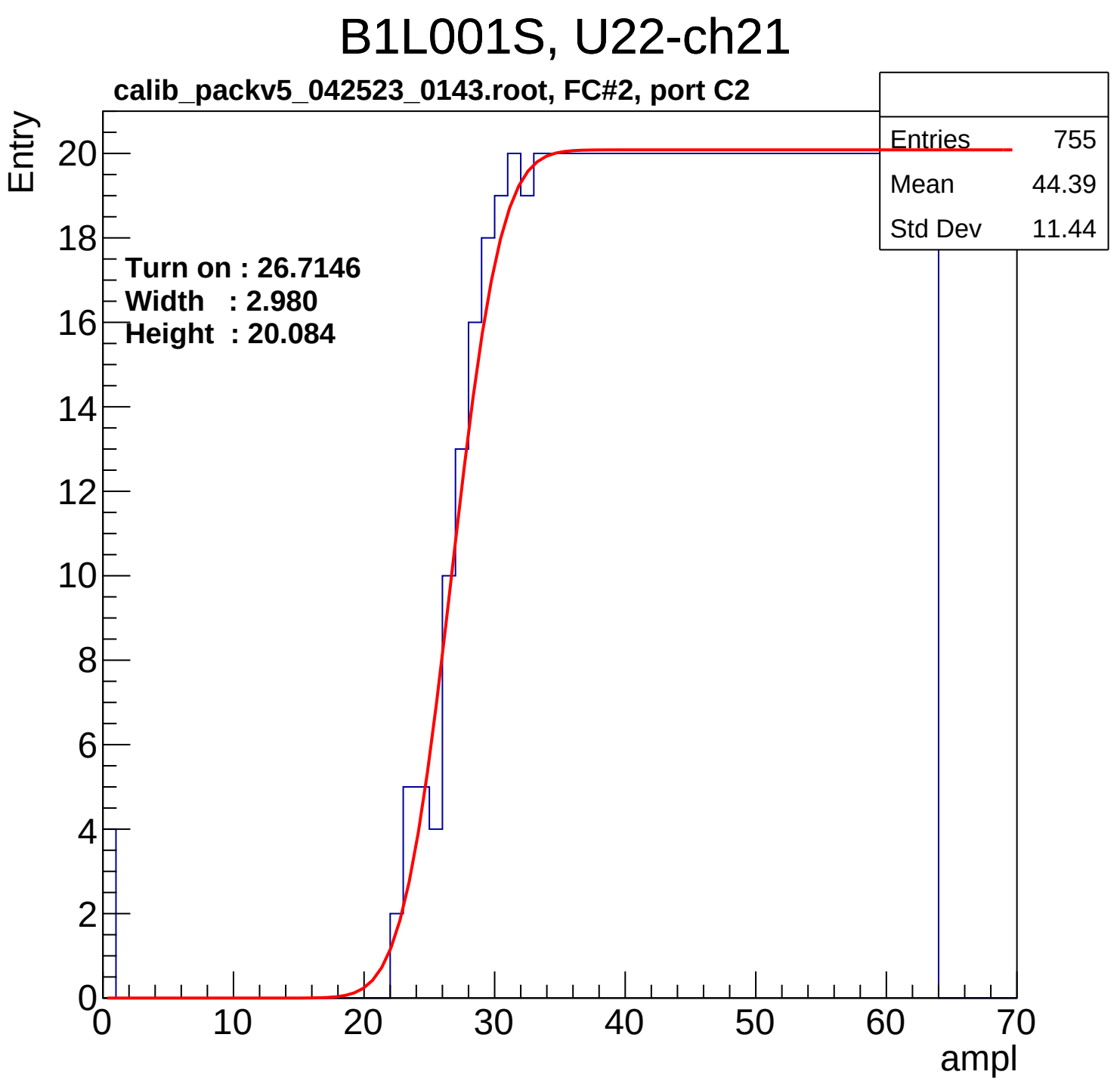
B1L001S, U22-ch21
calib_packv5_042523_0143.root, FC#2, port C2
Entries 755
Mean 44.39
Std Dev 11.44
Turn on : 26.7146
Width : 2.980
Height : 20.084
Entry
ampl
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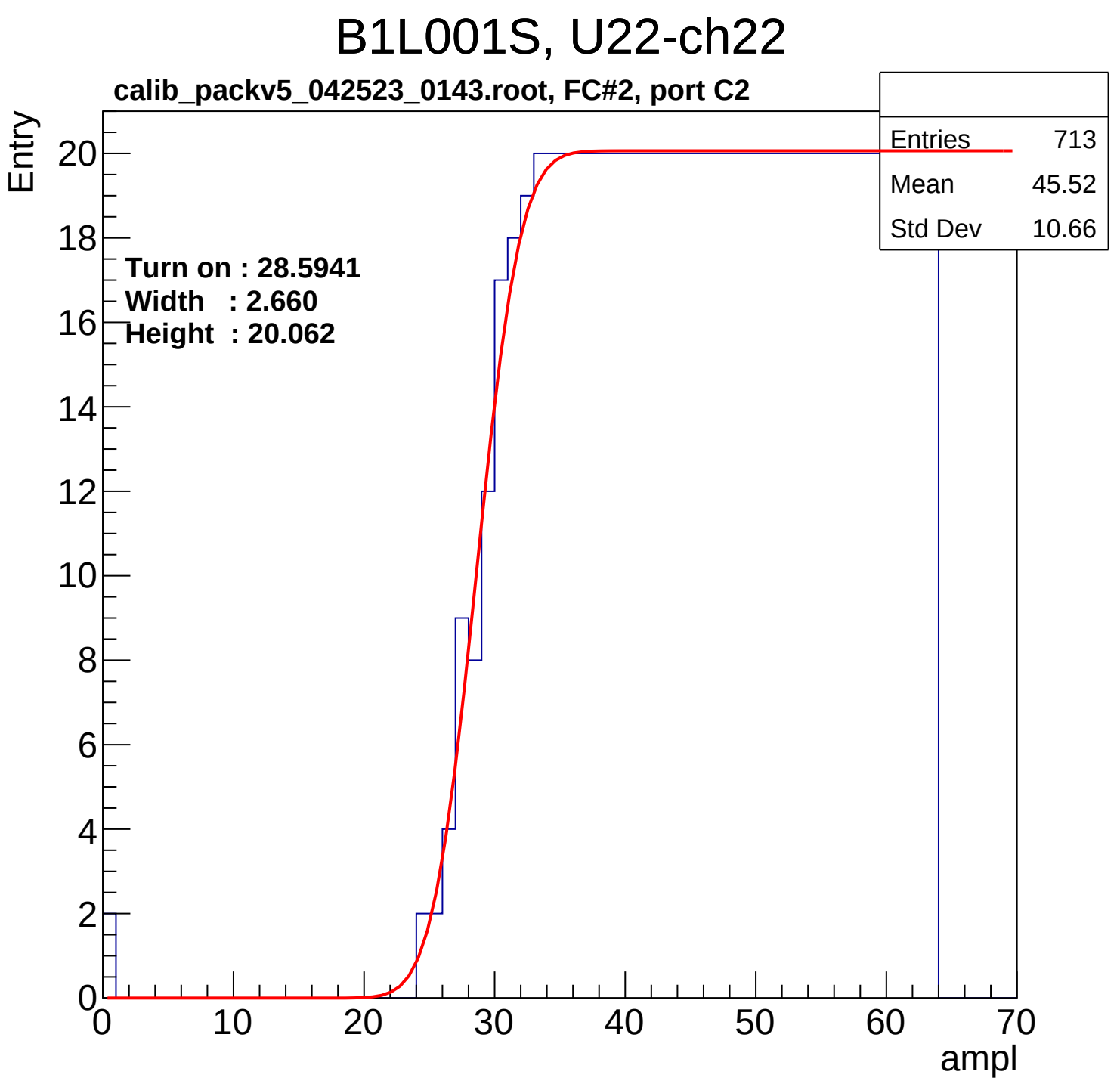
B1L001S, U22-ch22
calib_packv5_042523_0143.root, FC#2, port C2
Entries 713
Mean 45.52
Std Dev 10.66
Turn on : 28.5941
Width : 2.660
Height : 20.062
Entry
ampl
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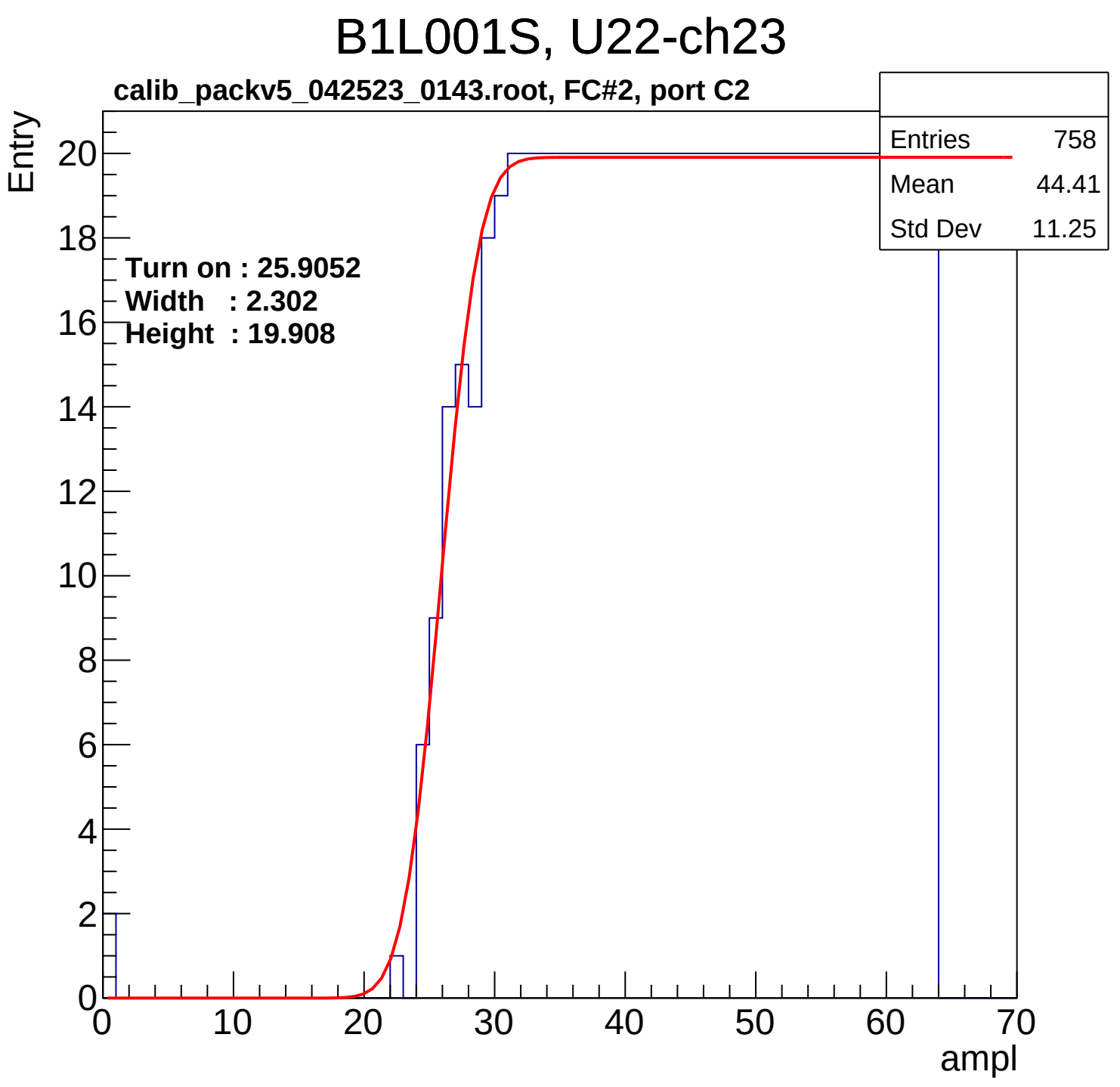
B1L001S, U22-ch23
calib_packv5_042523_0143.root, FC#2, port C2
Entries 758
Mean 44.41
Std Dev 11.25
Turn on : 25.9052
Width : 2.302
Height : 19.908
Entry
ampl
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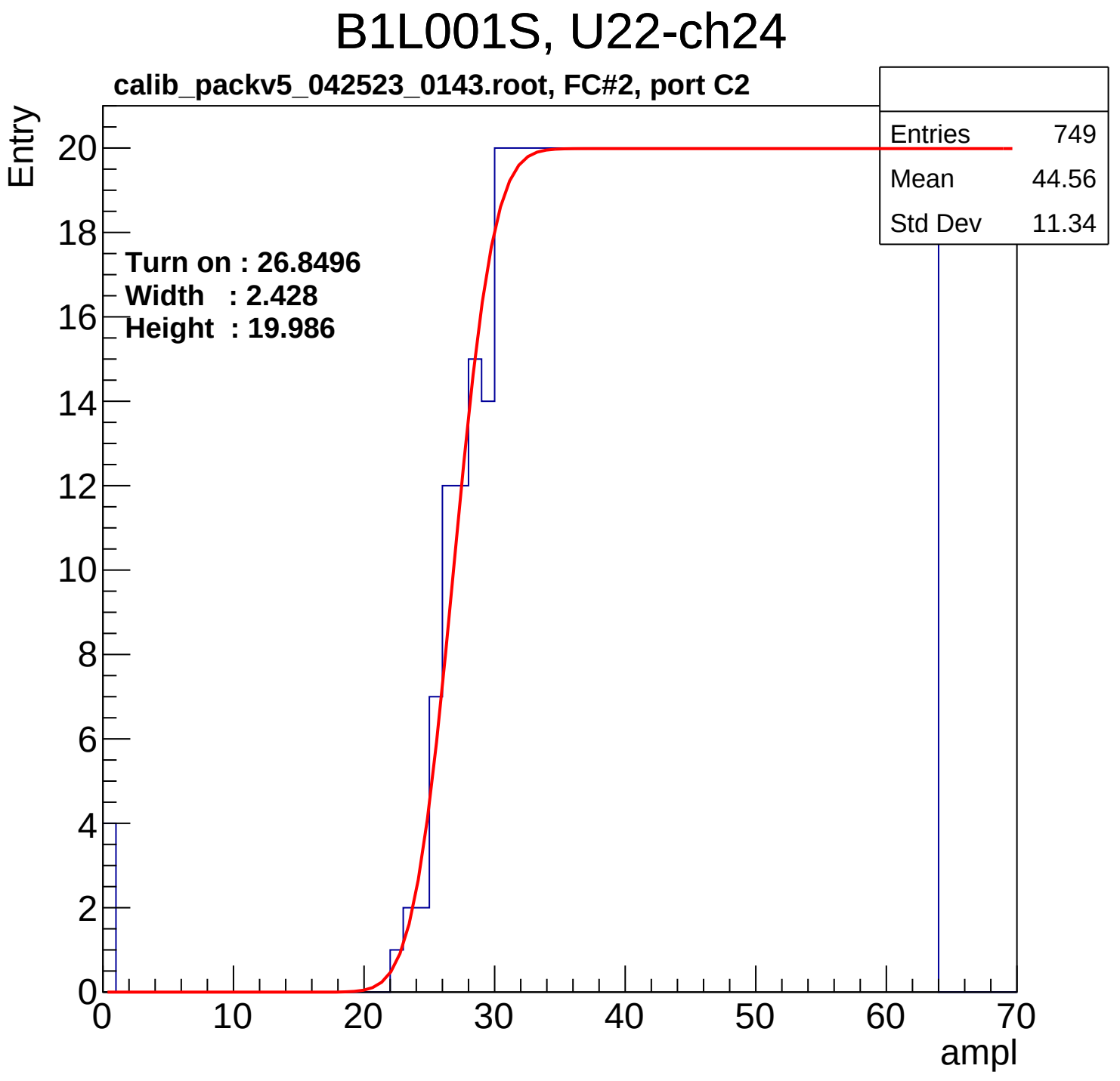
B1L001S, U22-ch24
calib_packv5_042523_0143.root, FC#2, port C2
Entries 749
Mean 44.56
Std Dev 11.34
Turn on : 26.8496
Width : 2.428
Height : 19.986
Entry
ampl
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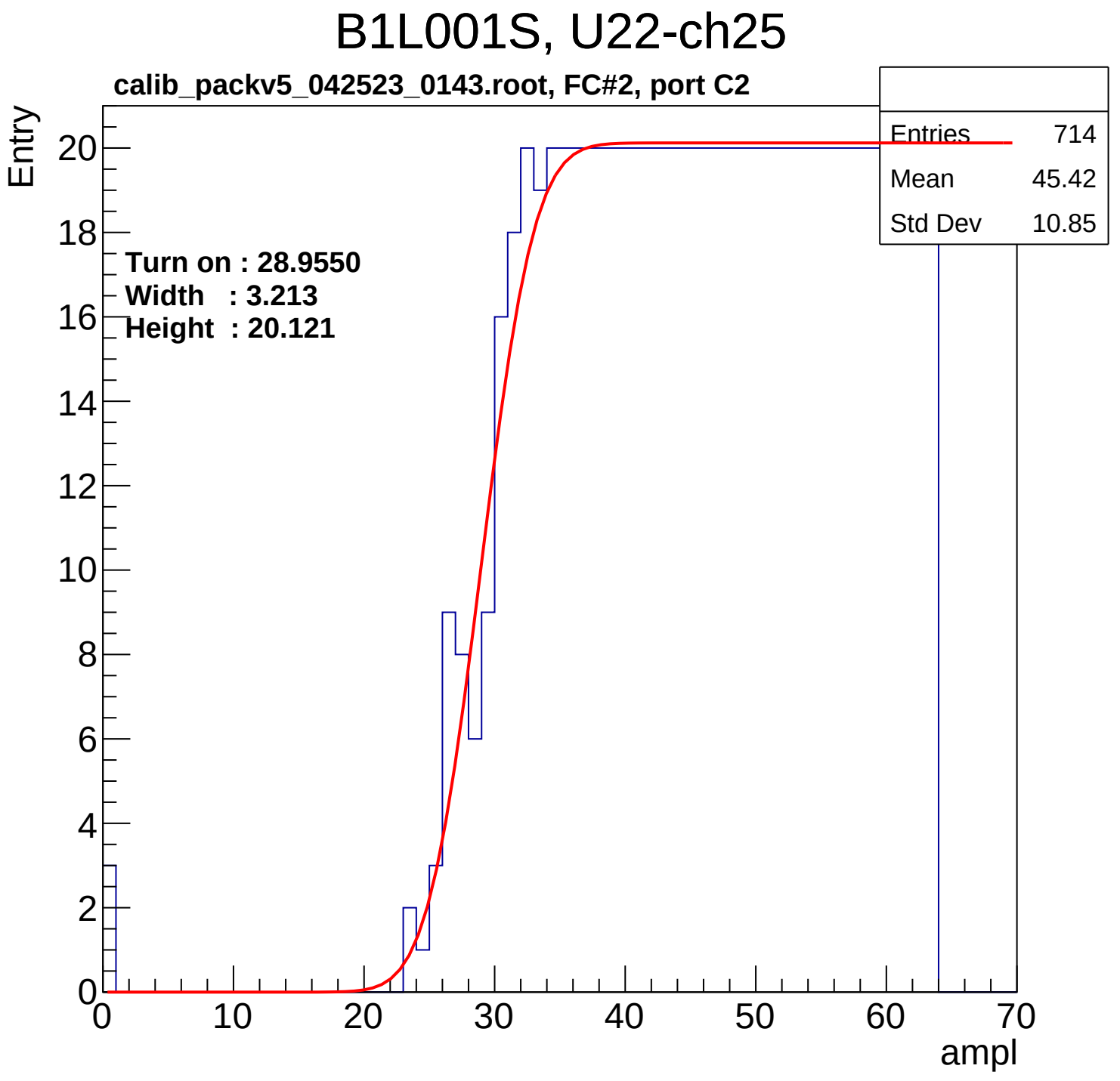
B1L001S, U22-ch25
calib_packv5_042523_0143.root, FC#2, port C2
Entries 714
Mean 45.42
Std Dev 10.85
Turn on : 28.9550
Width : 3.213
Height : 20.121
Entry
ampl
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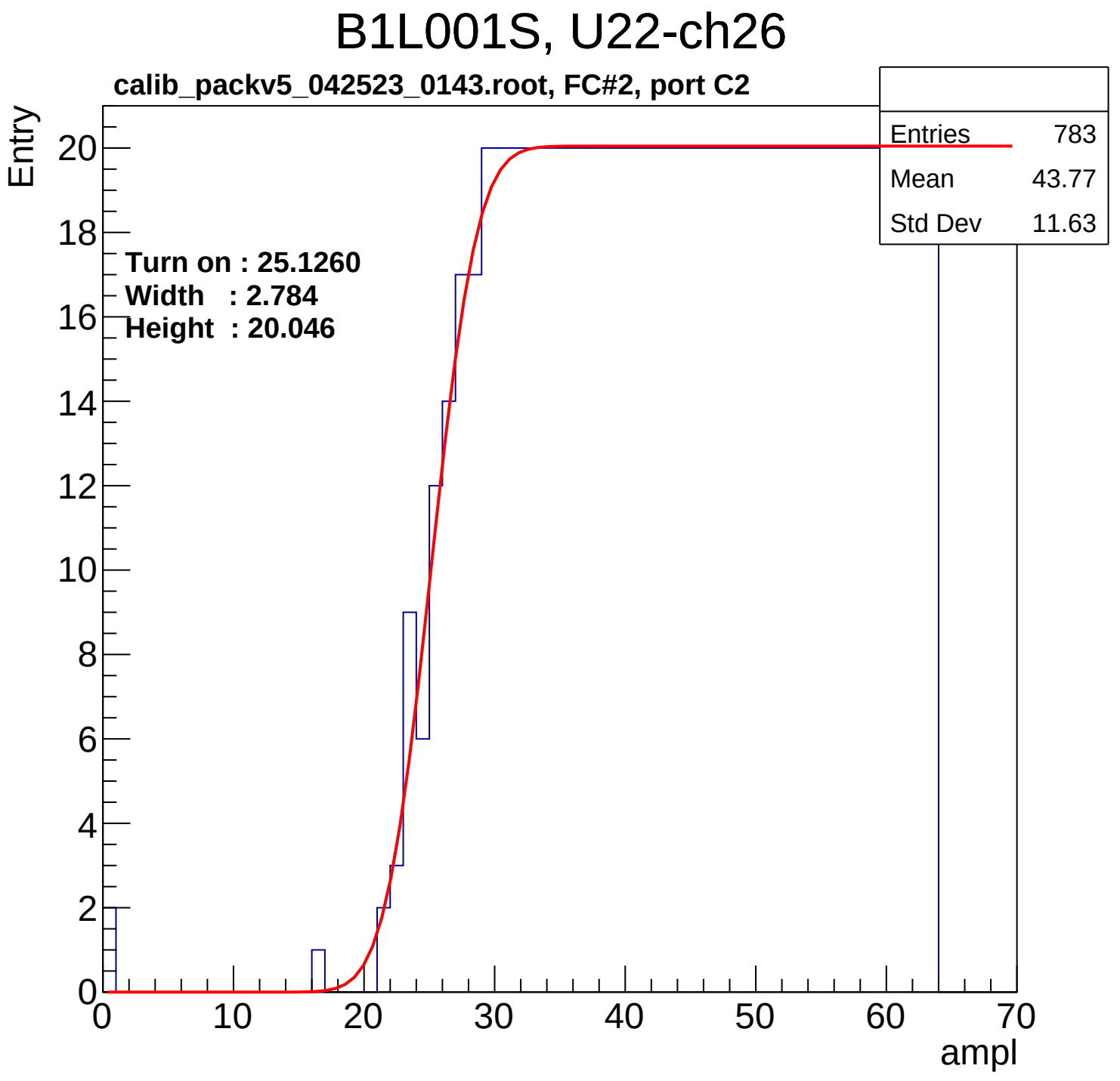
B1L001S, U22-ch26
calib_packv5_042523_0143.root, FC#2, port C2
Entries 783
Mean 43.77
Std Dev 11.63
Turn on : 25.1260
Width : 2.784
Height : 20.046
Entry
ampl
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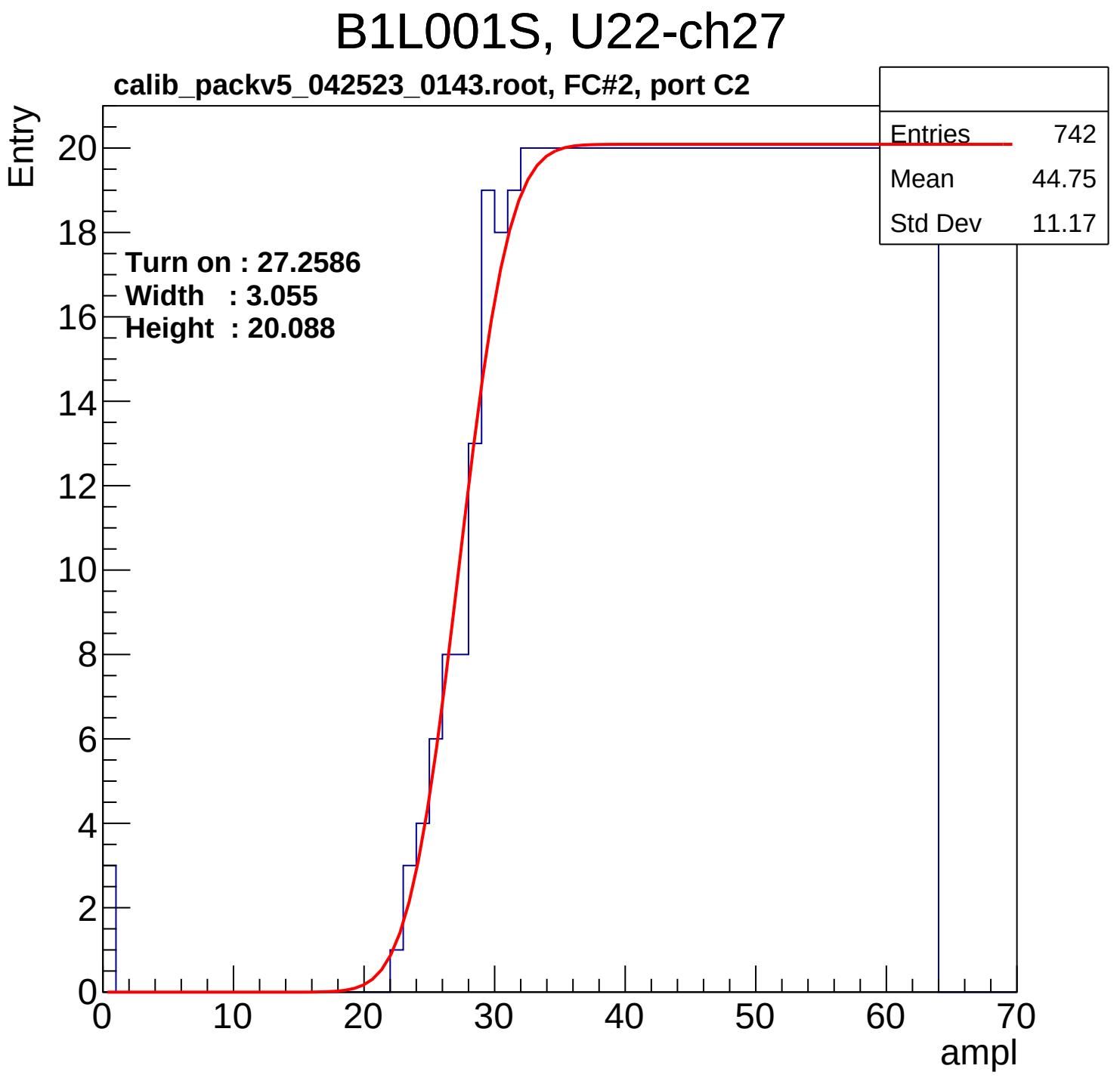
B1L001S, U22-ch27
calib_packv5_042523_0143.root, FC#2, port C2
Entries 742
Mean 44.75
Std Dev 11.17
Turn on : 27.2586
Width : 3.055
Height : 20.088
Entry
ampl
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6
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12
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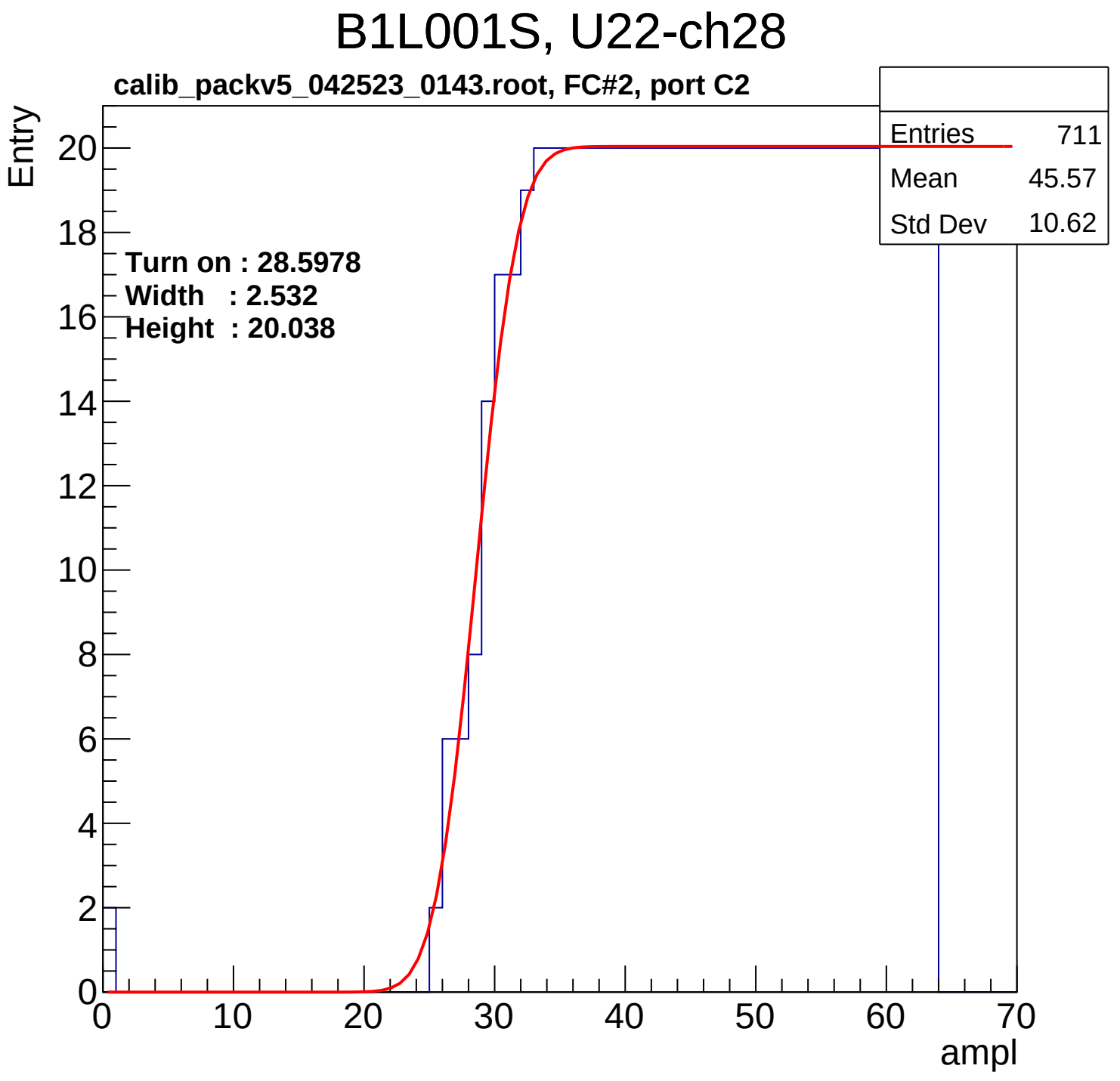
B1L001S, U22-ch28
calib_packv5_042523_0143.root, FC#2, port C2
Entries 711
Mean 45.57
Std Dev 10.62
Turn on : 28.5978
Width : 2.532
Height : 20.038
Entry
ampl
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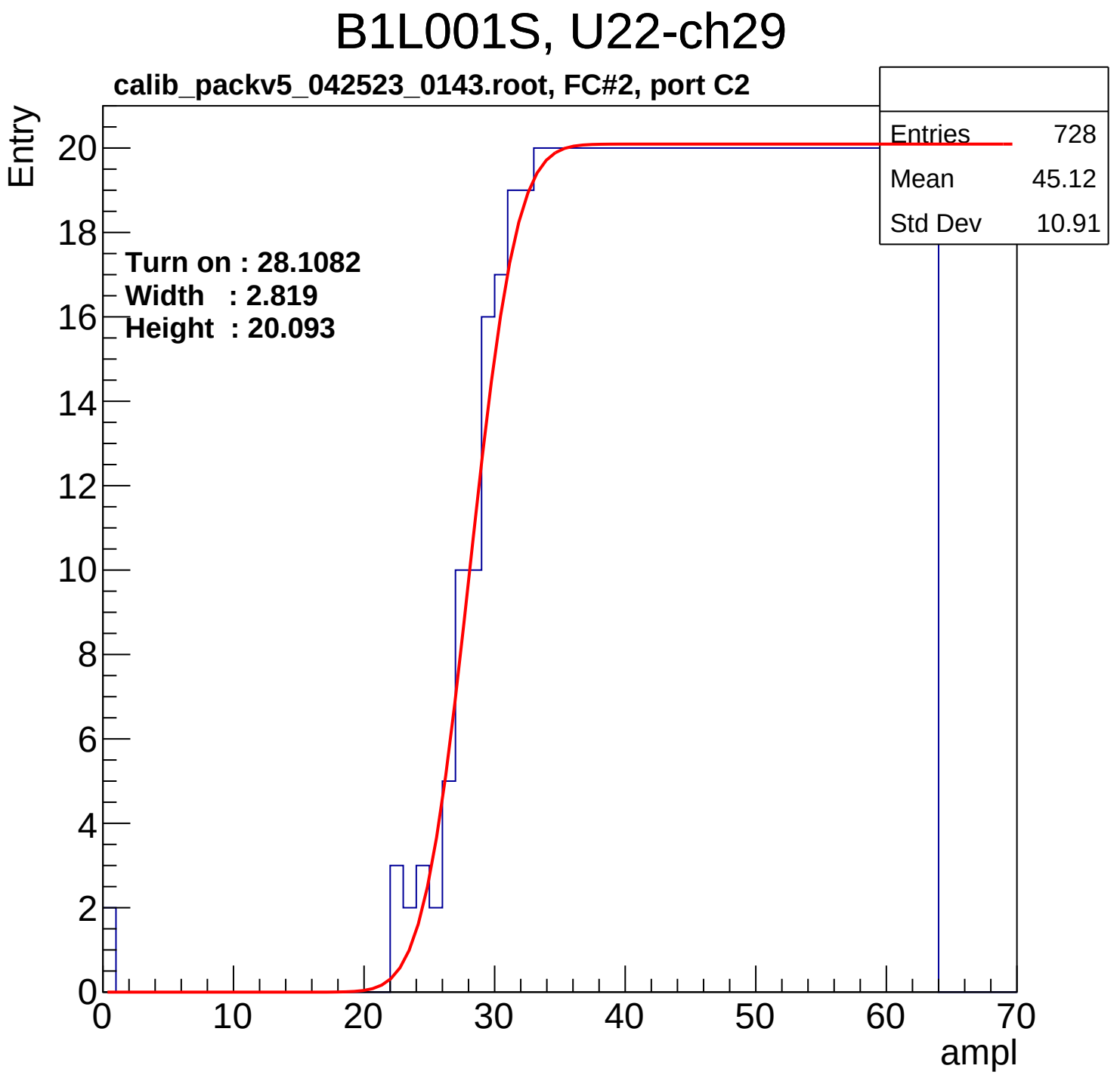
B1L001S, U22-ch29
calib_packv5_042523_0143.root, FC#2, port C2
Entries 728
Mean 45.12
Std Dev 10.91
Turn on : 28.1082
Width : 2.819
Height : 20.093
Entry
ampl
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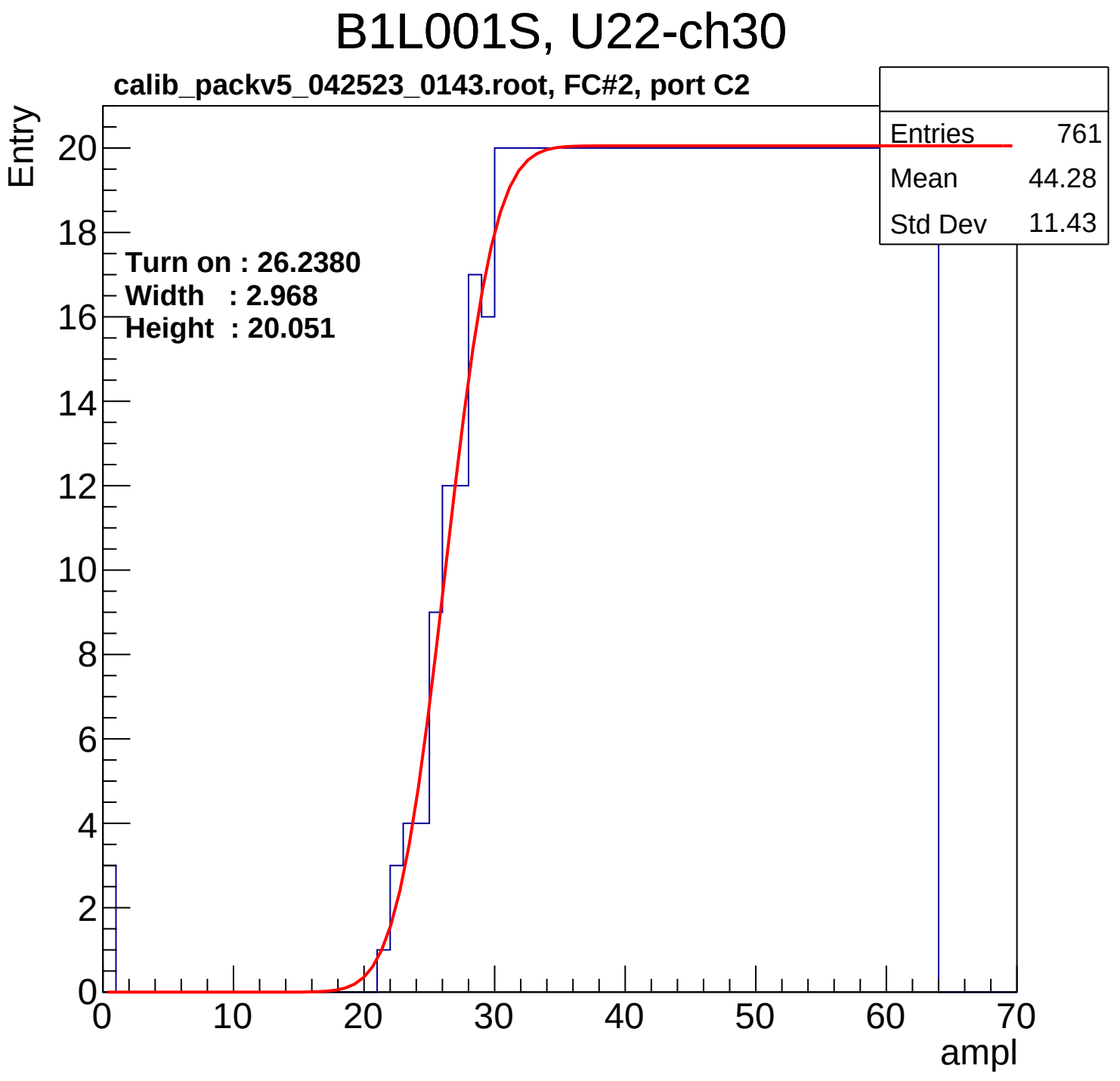
B1L001S, U22-ch30
calib_packv5_042523_0143.root, FC#2, port C2
Entries 761
Mean 44.28
Std Dev 11.43
Turn on : 26.2380
Width : 2.968
Height : 20.051
Entry
ampl
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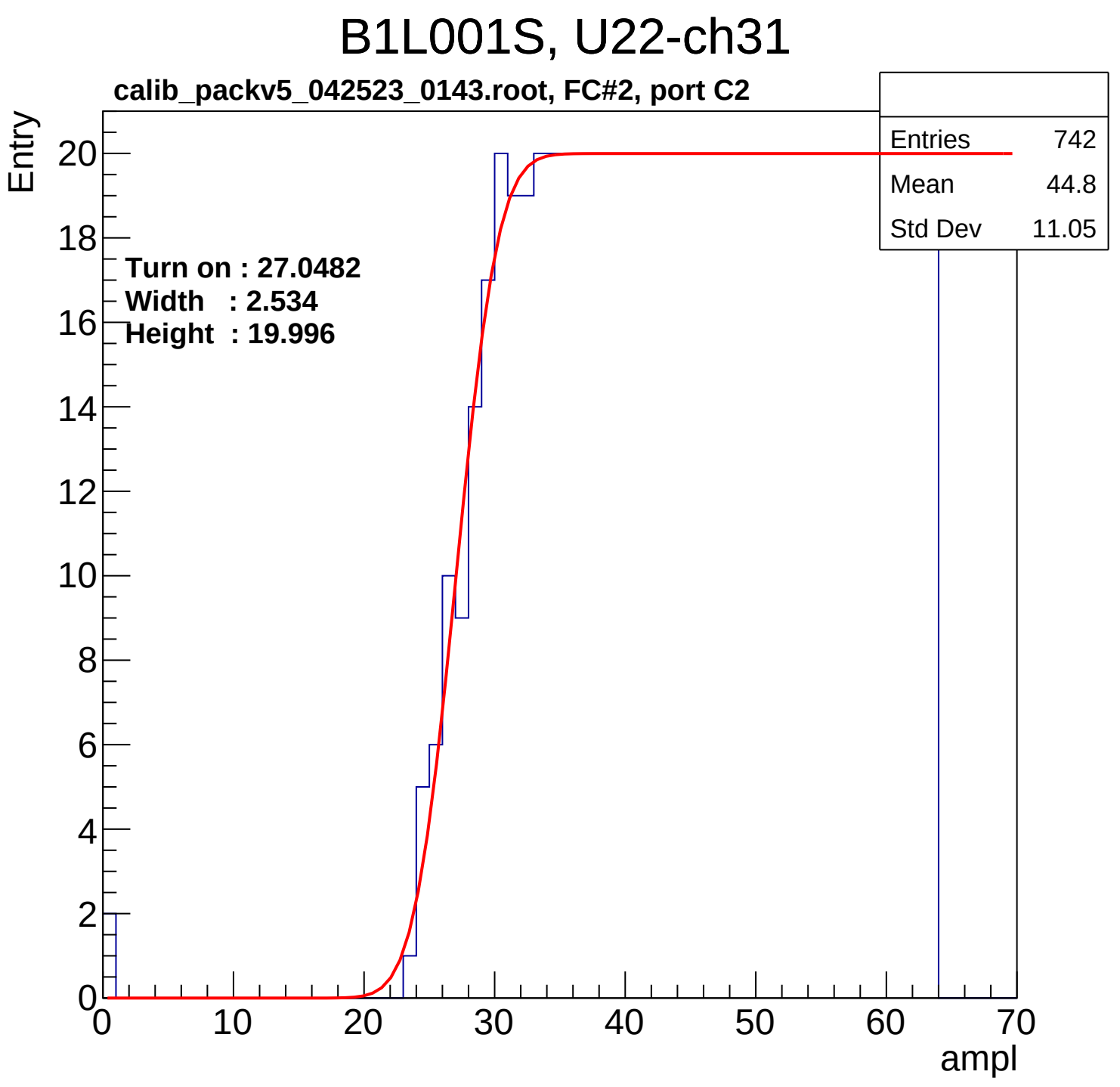
B1L001S, U22-ch31
calib_packv5_042523_0143.root, FC#2, port C2
Entries 742
Mean 44.8
Std Dev 11.05
Turn on : 27.0482
Width : 2.534
Height : 19.996
Entry
ampl
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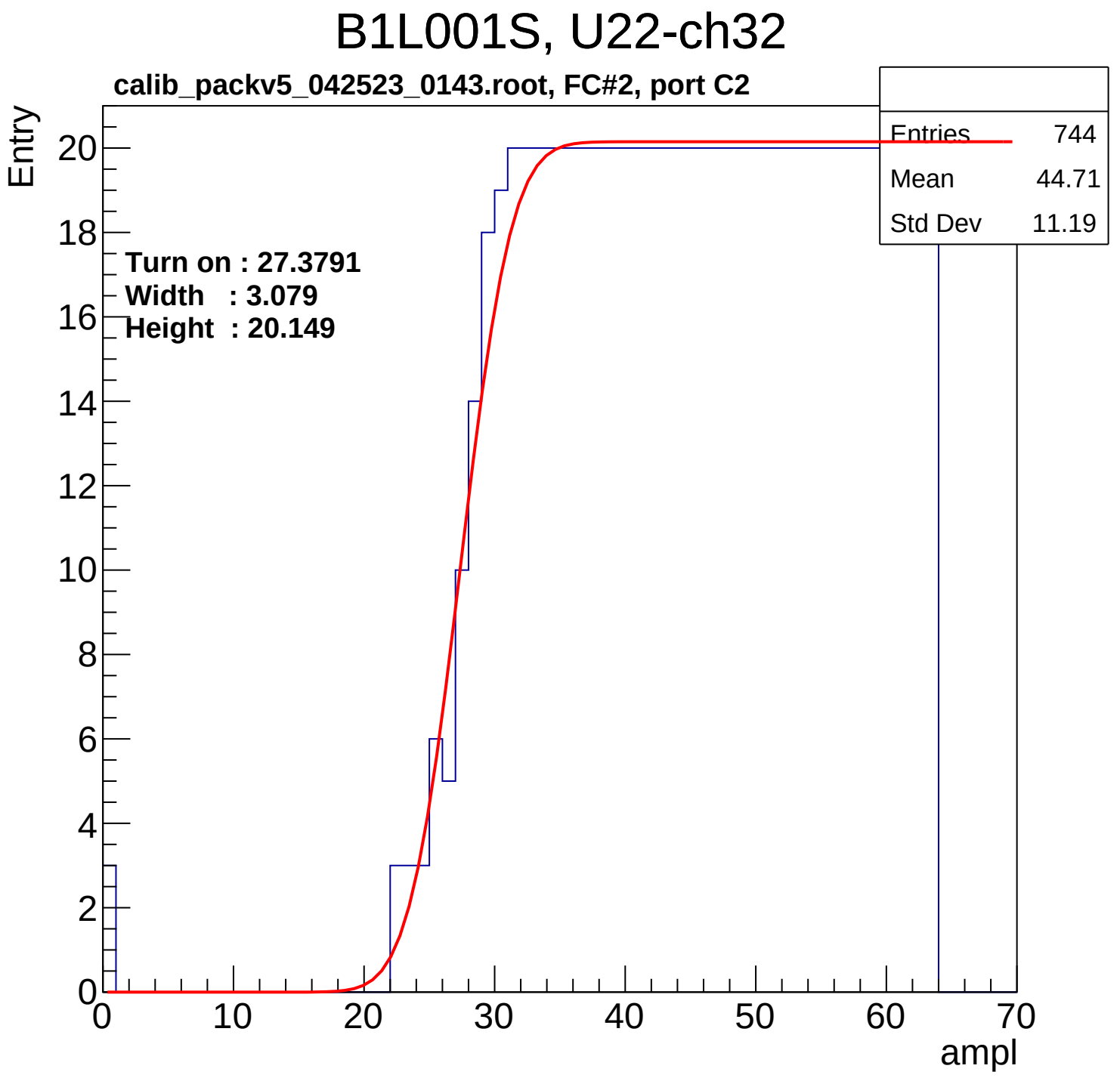
B1L001S, U22-ch32
calib_packv5_042523_0143.root, FC#2, port C2
Entries 744
Mean 44.71
Std Dev 11.19
Turn on : 27.3791
Width : 3.079
Height : 20.149
Entry
ampl
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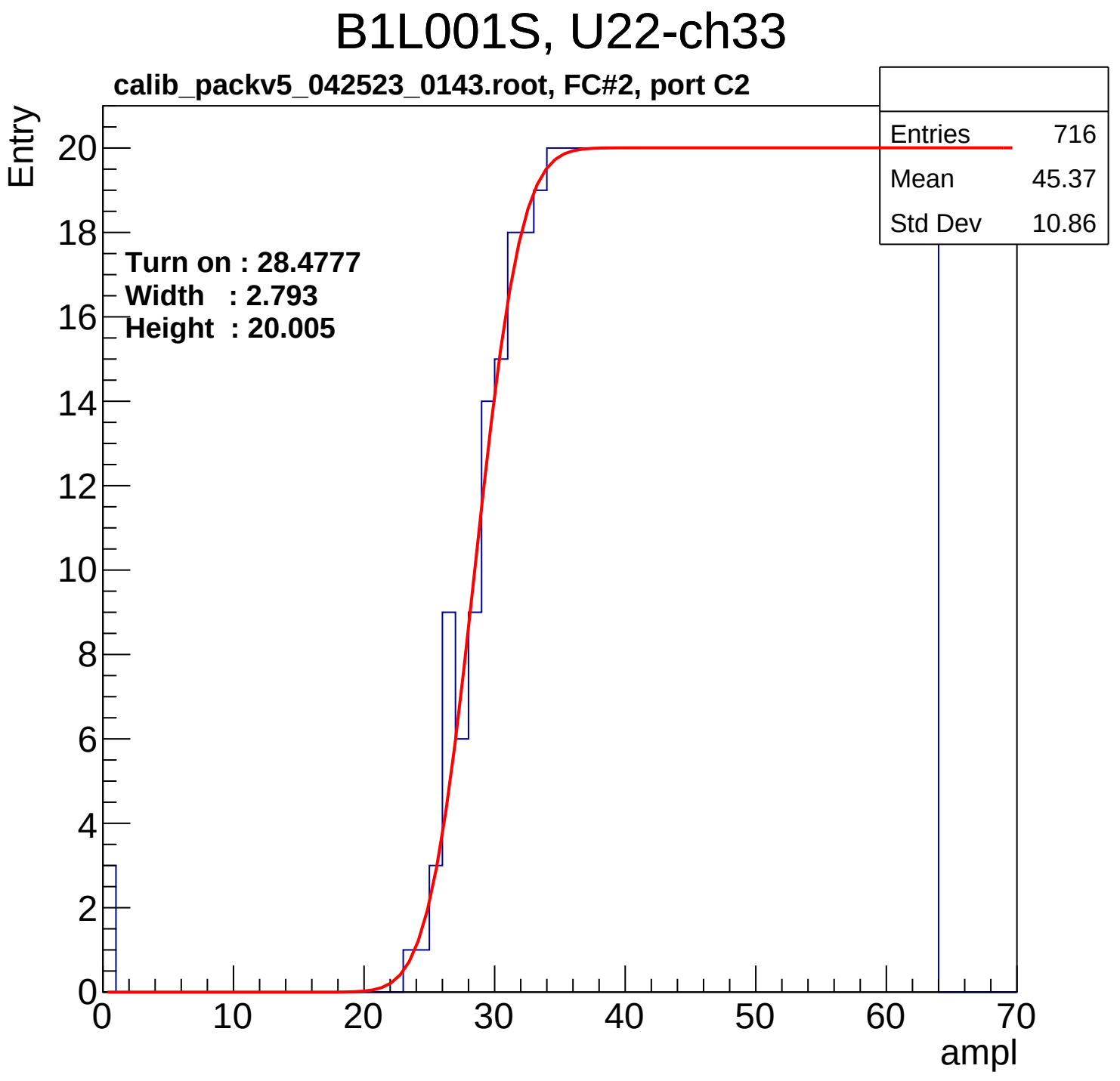
B1L001S, U22-ch33
calib_packv5_042523_0143.root, FC#2, port C2
Entries 716
Mean 45.37
Std Dev 10.86
Turn on : 28.4777
Width : 2.793
Height : 20.005
Entry
ampl
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6
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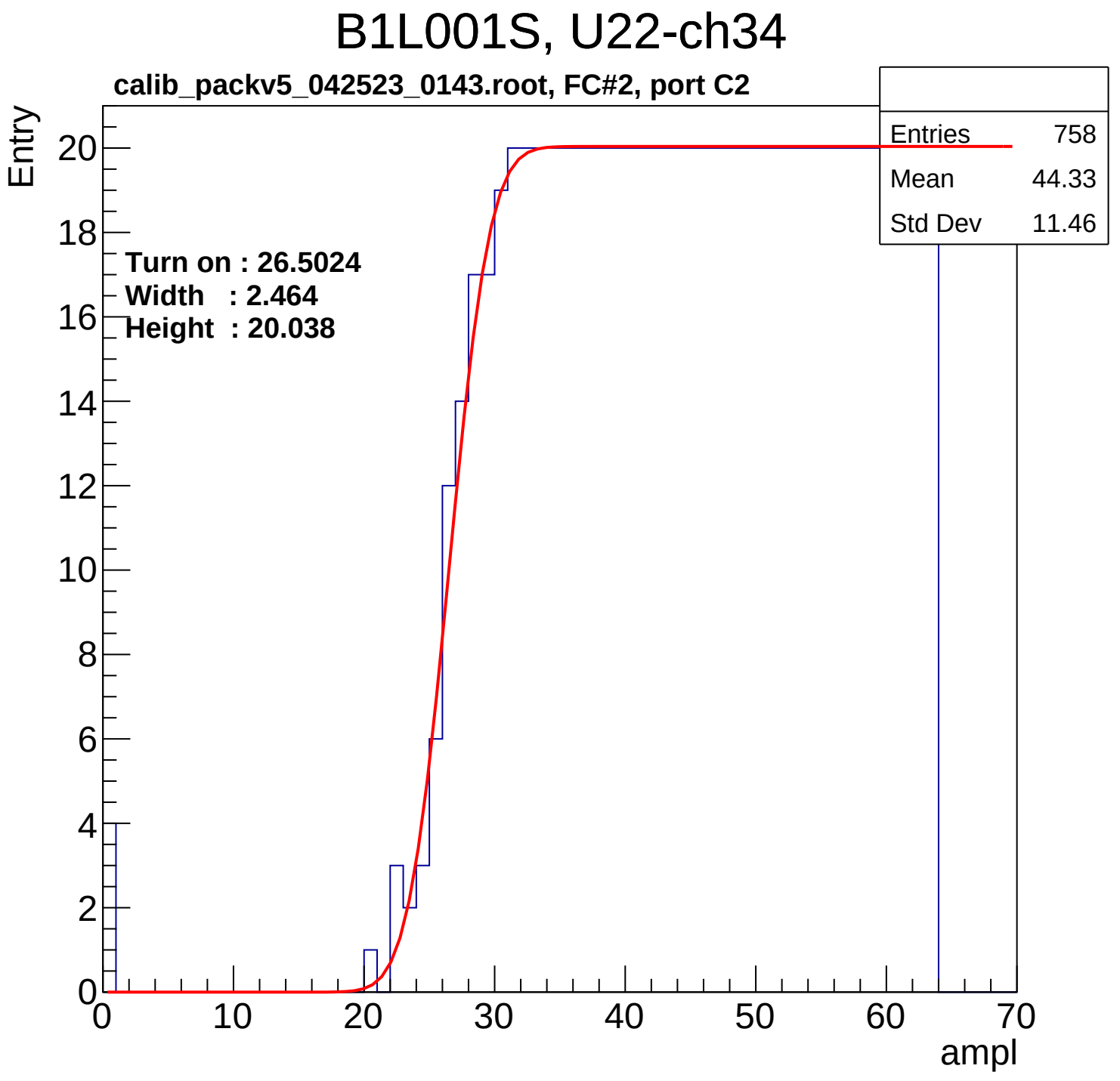
B1L001S, U22-ch34
calib_packv5_042523_0143.root, FC#2, port C2
Entries 758
Mean 44.33
Std Dev 11.46
Turn on : 26.5024
Width : 2.464
Height : 20.038
Entry
ampl
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6
8
10
12
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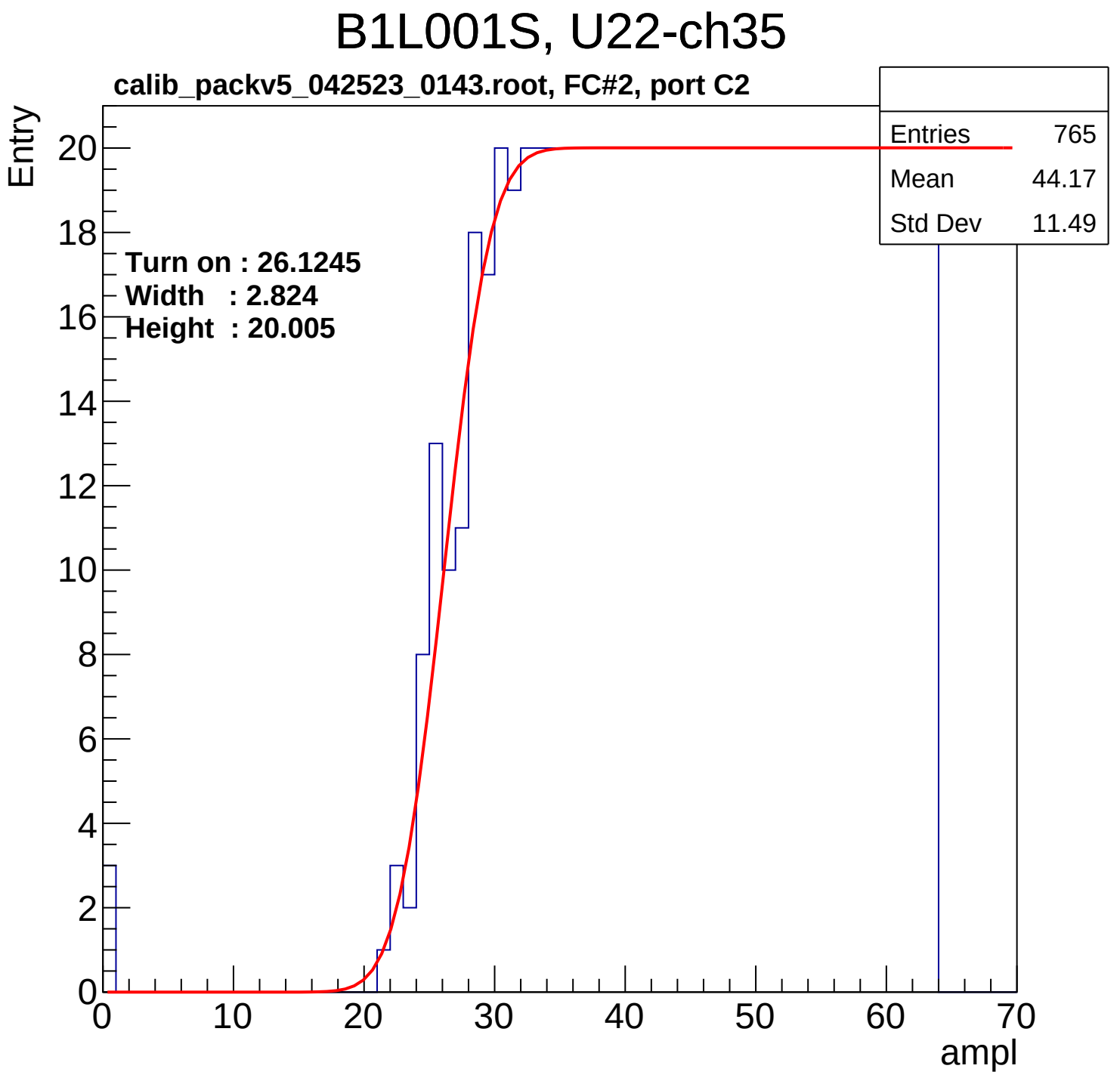
B1L001S, U22-ch35
calib_packv5_042523_0143.root, FC#2, port C2
Entries 765
Mean 44.17
Std Dev 11.49
Turn on : 26.1245
Width : 2.824
Height : 20.005
Entry
ampl
0
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6
8
10
12
14
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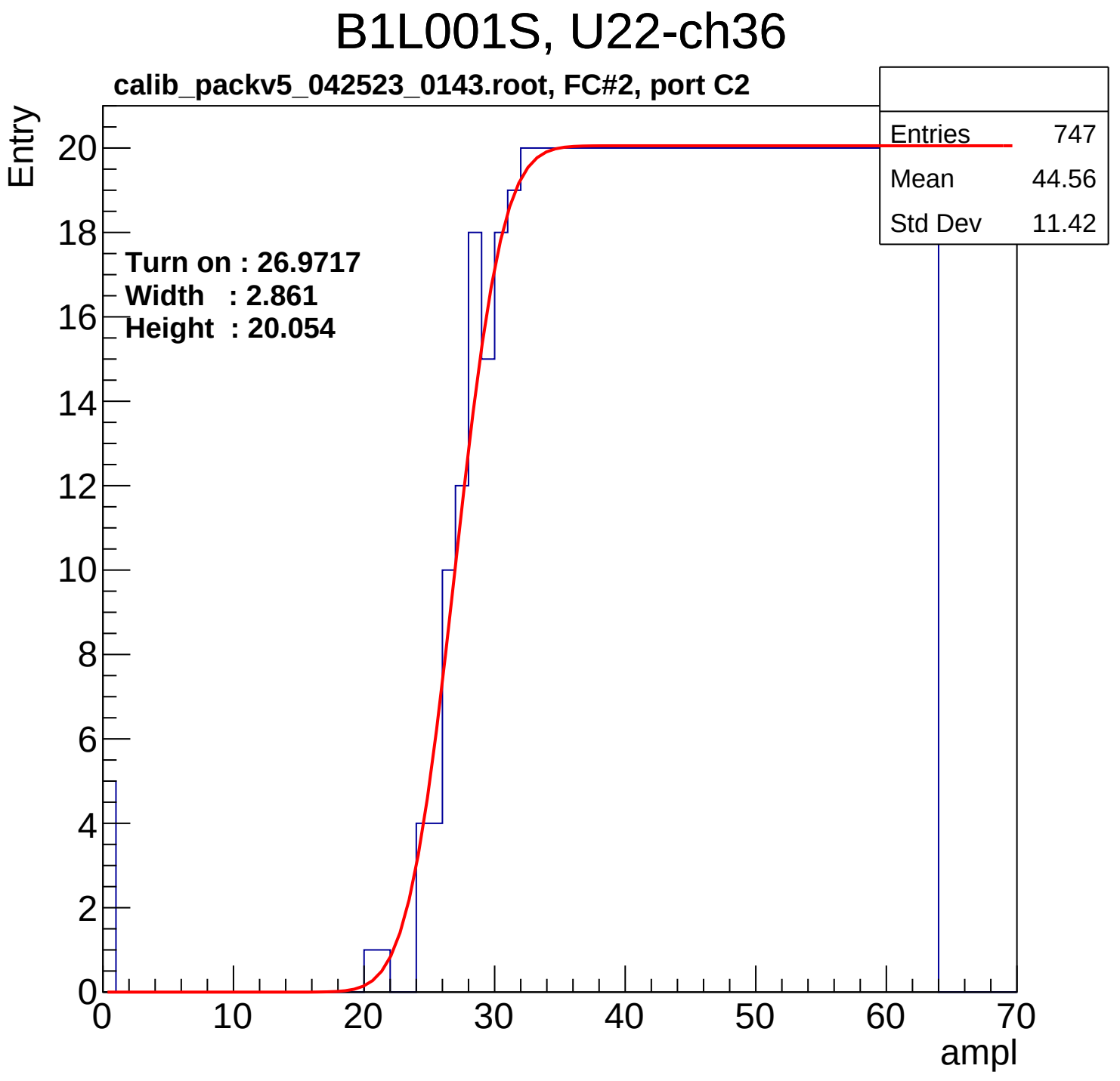
B1L001S, U22-ch36
calib_packv5_042523_0143.root, FC#2, port C2
Entries 747
Mean 44.56
Std Dev 11.42
Turn on : 26.9717
Width : 2.861
Height : 20.054
Entry
ampl
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6
8
10
12
14
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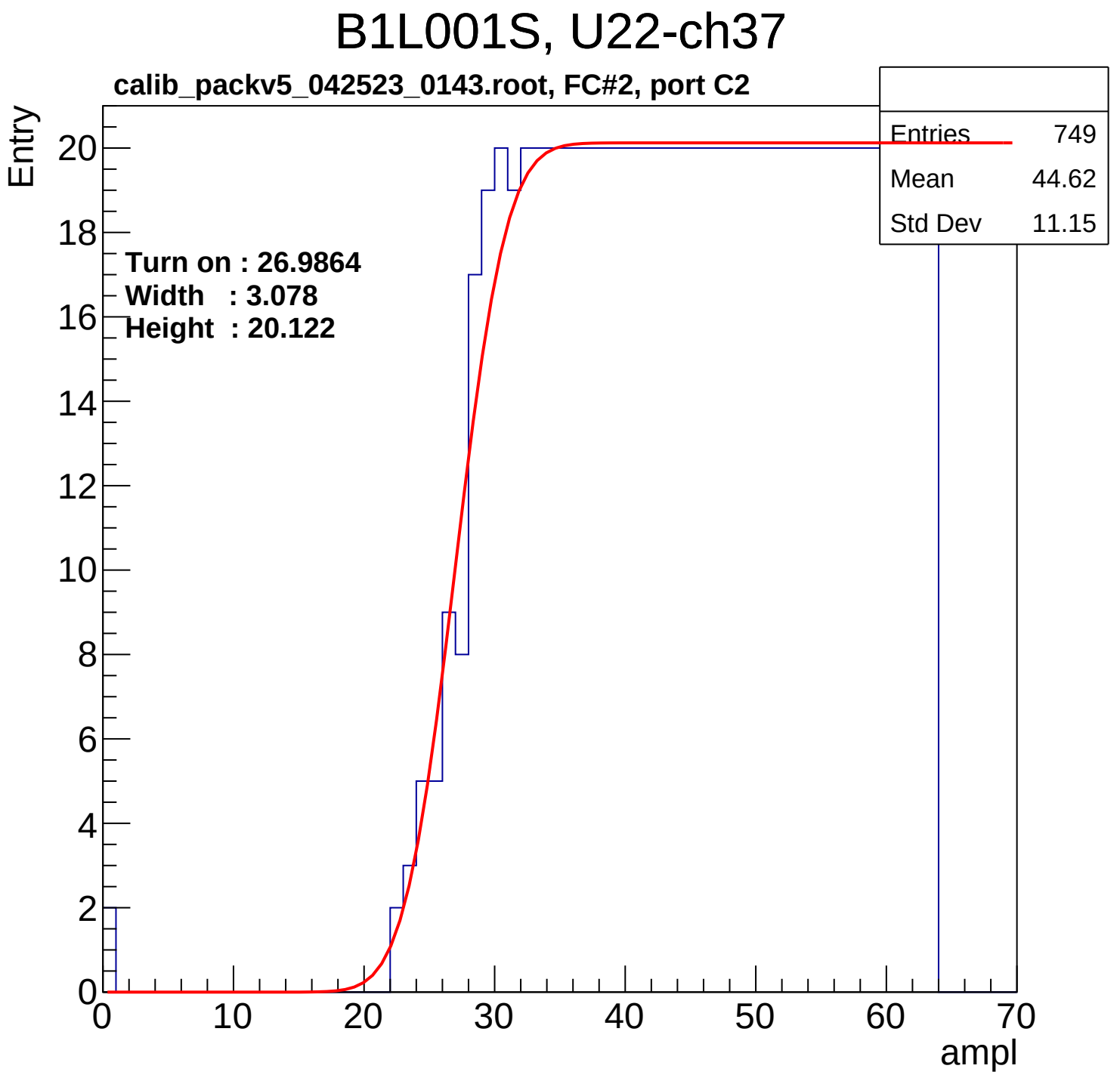
B1L001S, U22-ch37
calib_packv5_042523_0143.root, FC#2, port C2
Entries 749
Mean 44.62
Std Dev 11.15
Turn on : 26.9864
Width : 3.078
Height : 20.122
Entry
ampl
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6
8
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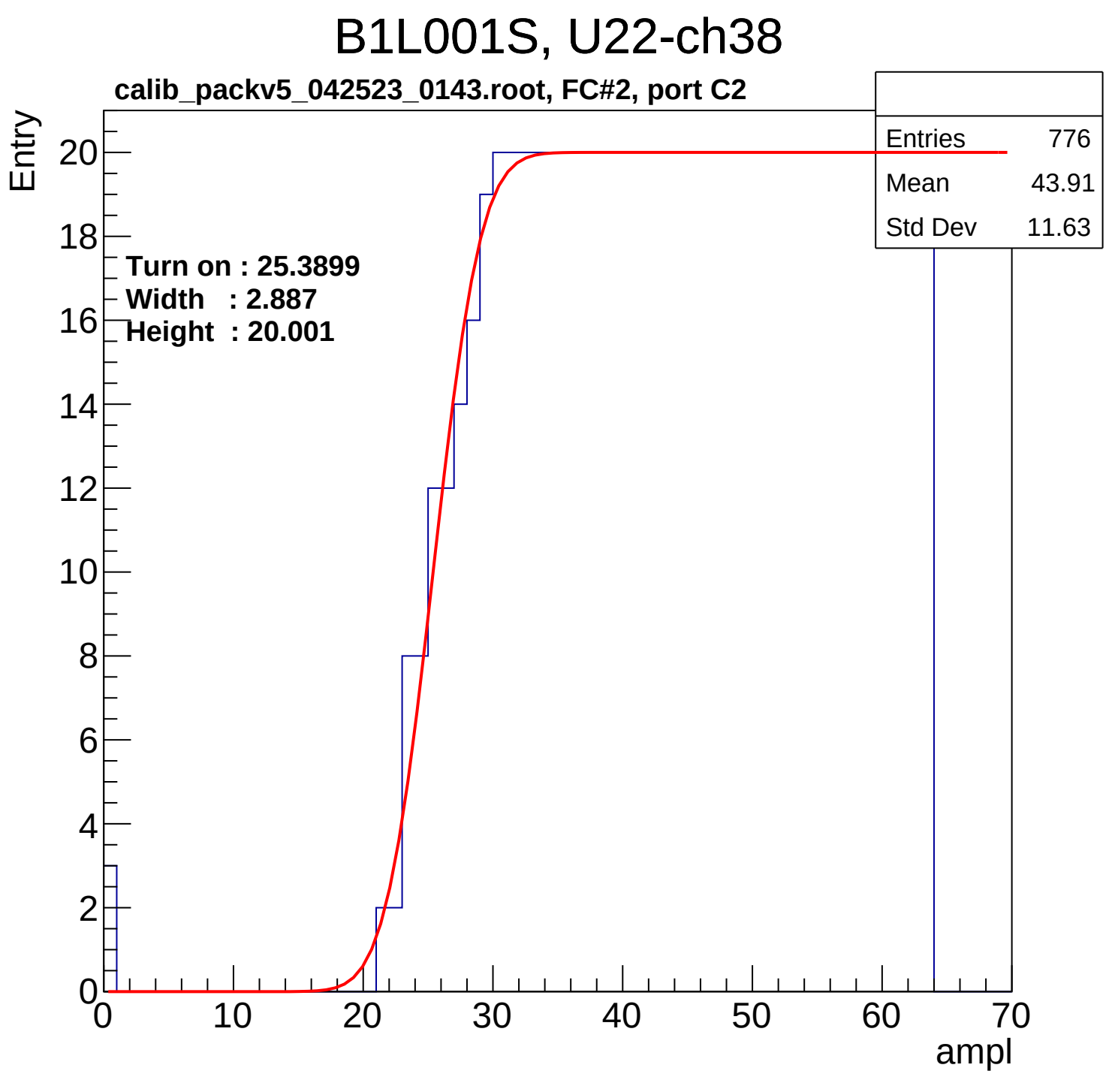
B1L001S, U22-ch38
calib_packv5_042523_0143.root, FC#2, port C2
Entries 776
Mean 43.91
Std Dev 11.63
Turn on : 25.3899
Width : 2.887
Height : 20.001
Entry
ampl
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6
8
10
12
14
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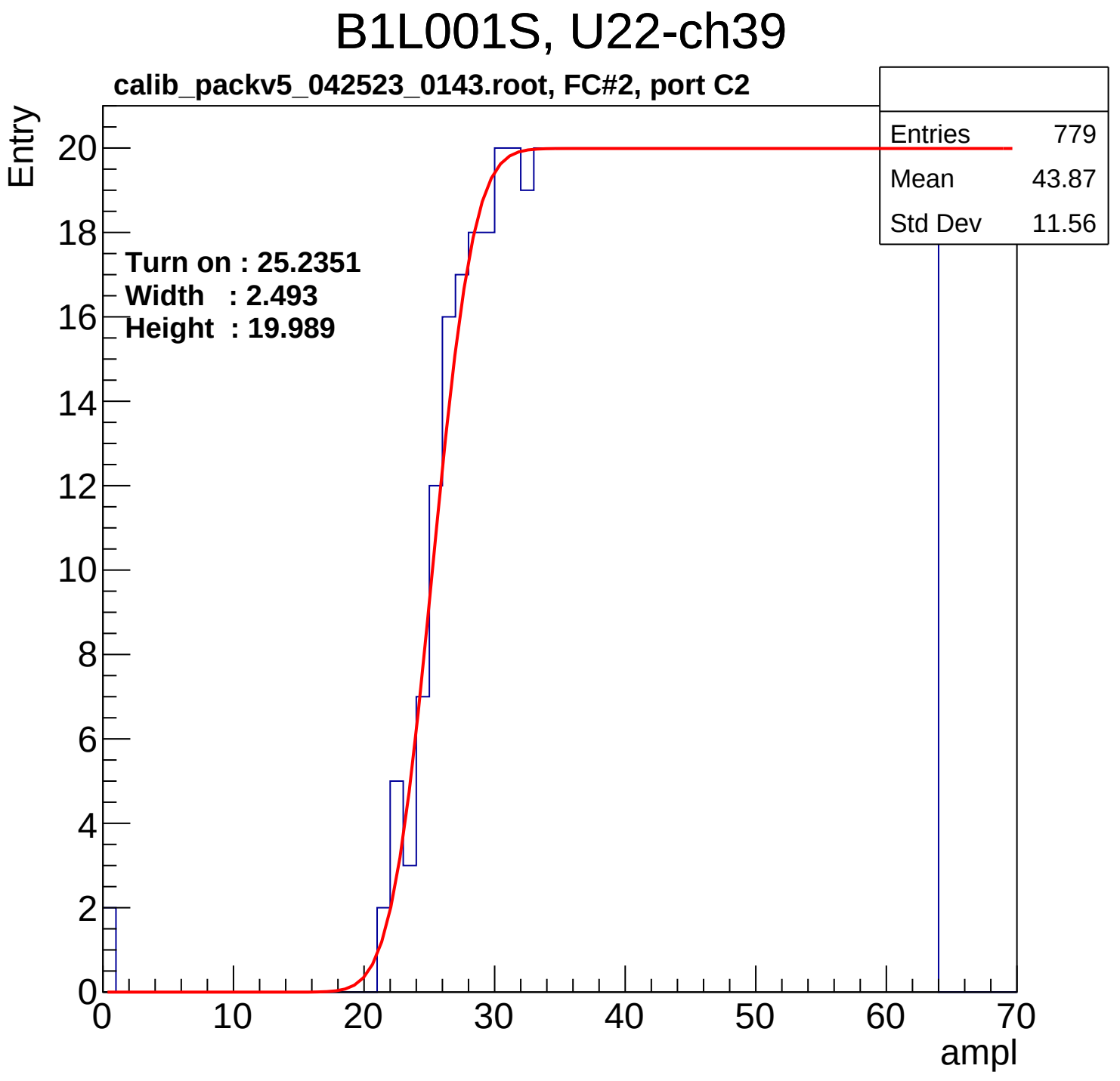
B1L001S, U22-ch39
calib_packv5_042523_0143.root, FC#2, port C2
Entries 779
Mean 43.87
Std Dev 11.56
Turn on : 25.2351
Width : 2.493
Height : 19.989
Entry
ampl
0
2
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6
8
10
12
14
16
18
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0
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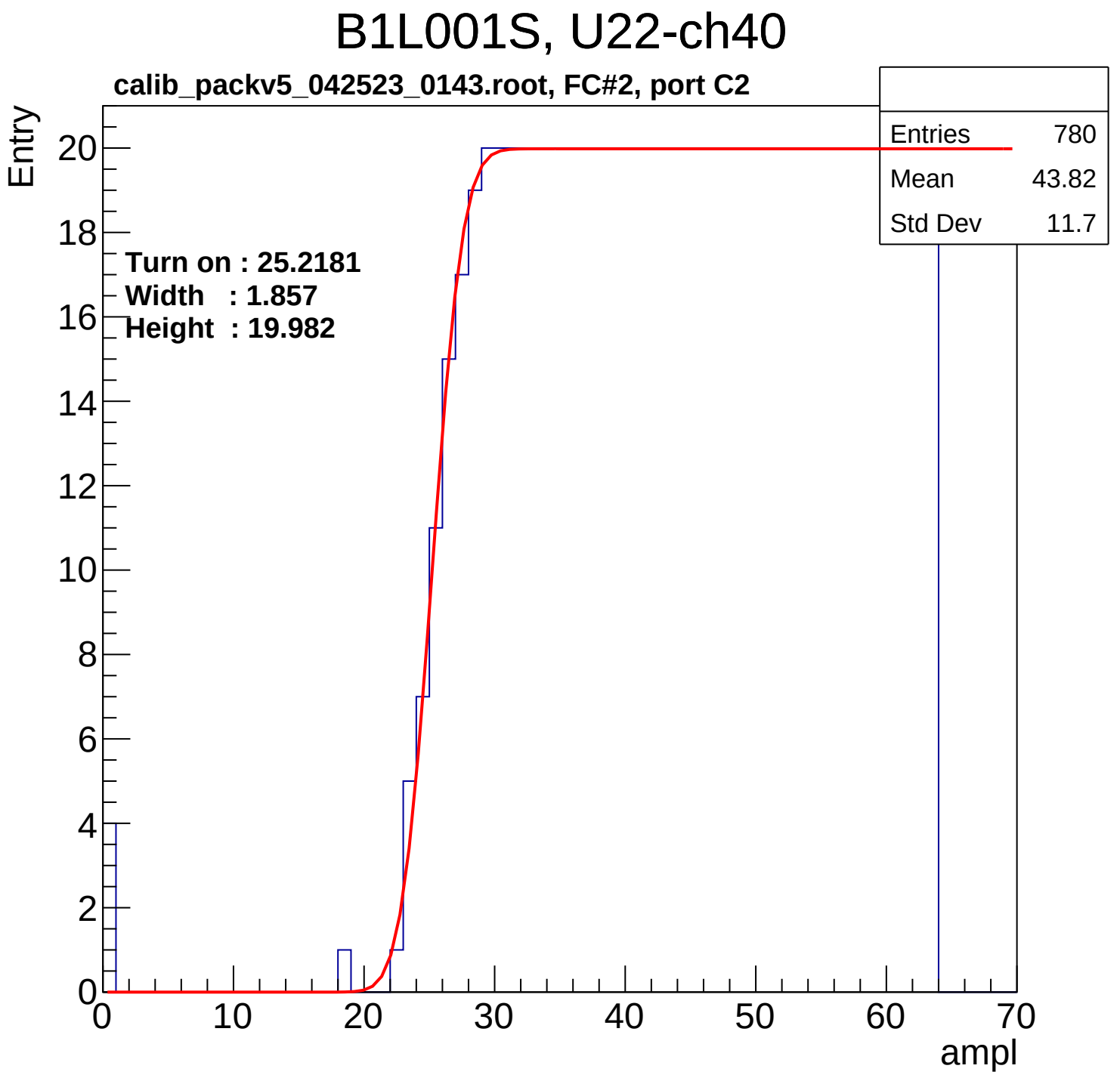
B1L001S, U22-ch40
calib_packv5_042523_0143.root, FC#2, port C2
Entries 780
Mean 43.82
Std Dev 11.7
Turn on : 25.2181
Width : 1.857
Height : 19.982
Entry
ampl
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6
8
10
12
14
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0
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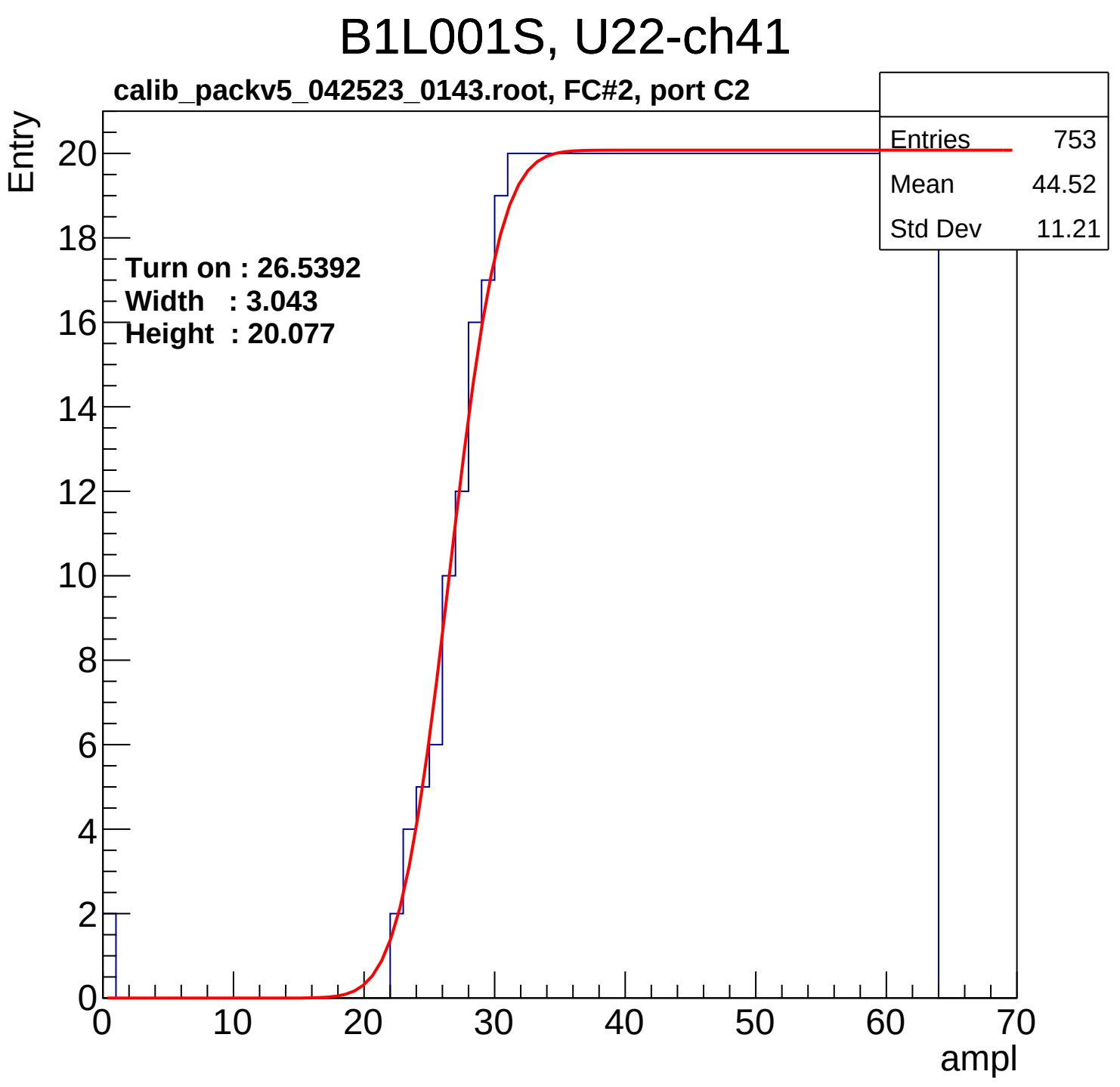
B1L001S, U22-ch41
calib_packv5_042523_0143.root, FC#2, port C2
Entries 753
Mean 44.52
Std Dev 11.21
Turn on : 26.5392
Width : 3.043
Height : 20.077
Entry
ampl
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12
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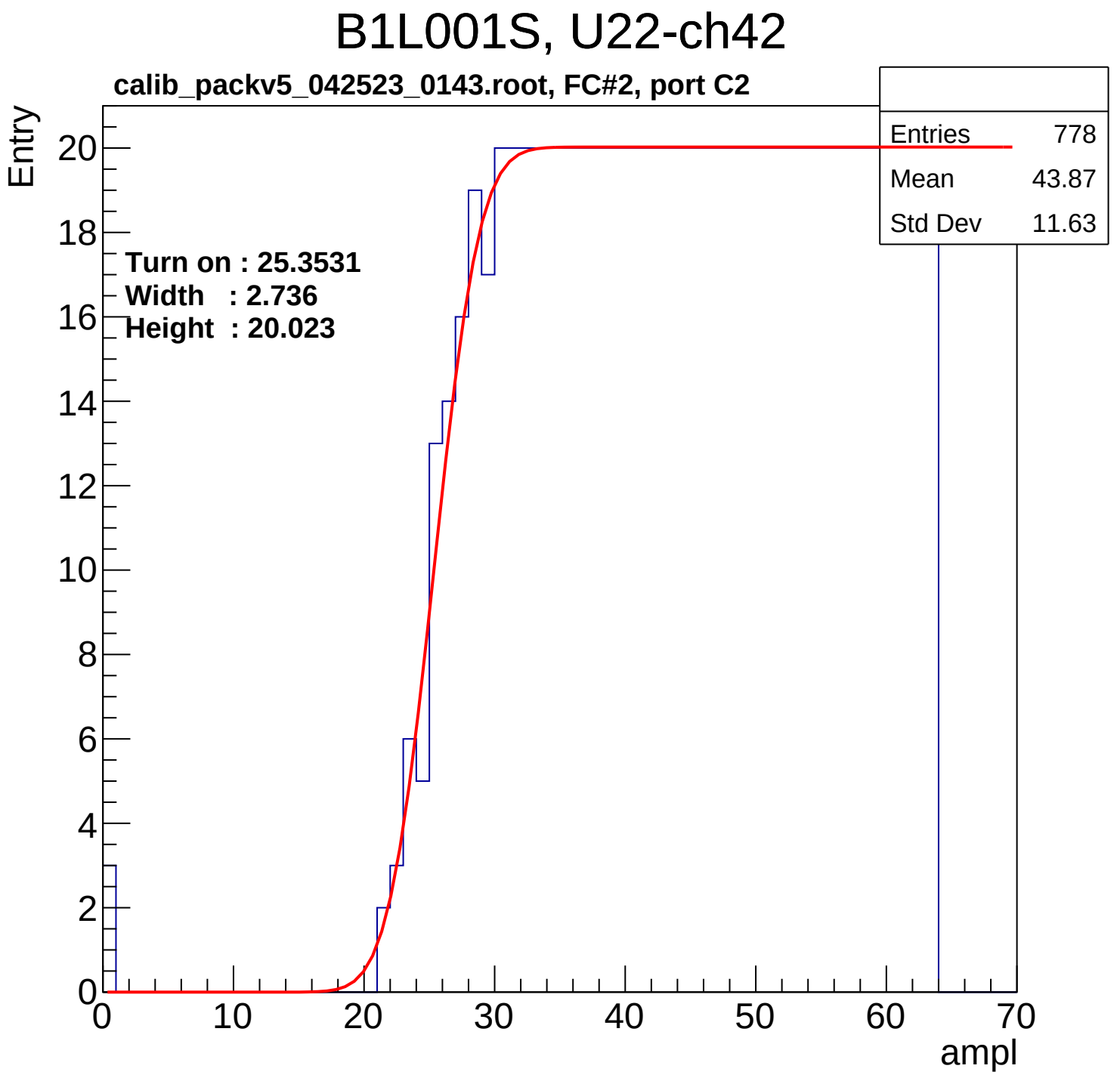
B1L001S, U22-ch42
calib_packv5_042523_0143.root, FC#2, port C2
Entries 778
Mean 43.87
Std Dev 11.63
Turn on : 25.3531
Width : 2.736
Height : 20.023
Entry
ampl
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6
8
10
12
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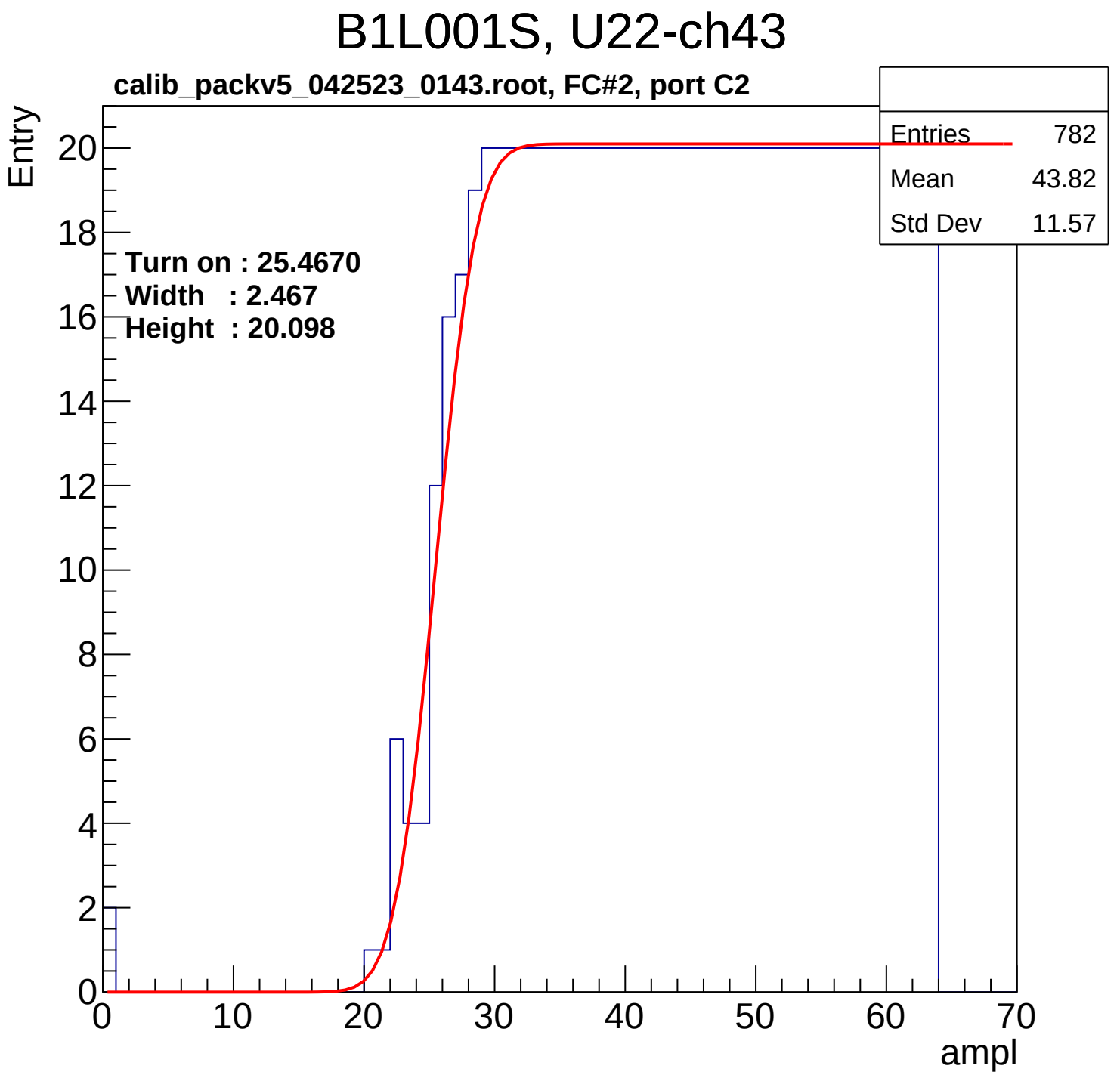
B1L001S, U22-ch43
calib_packv5_042523_0143.root, FC#2, port C2
Entries 782
Mean 43.82
Std Dev 11.57
Turn on : 25.4670
Width : 2.467
Height : 20.098
Entry
ampl
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6
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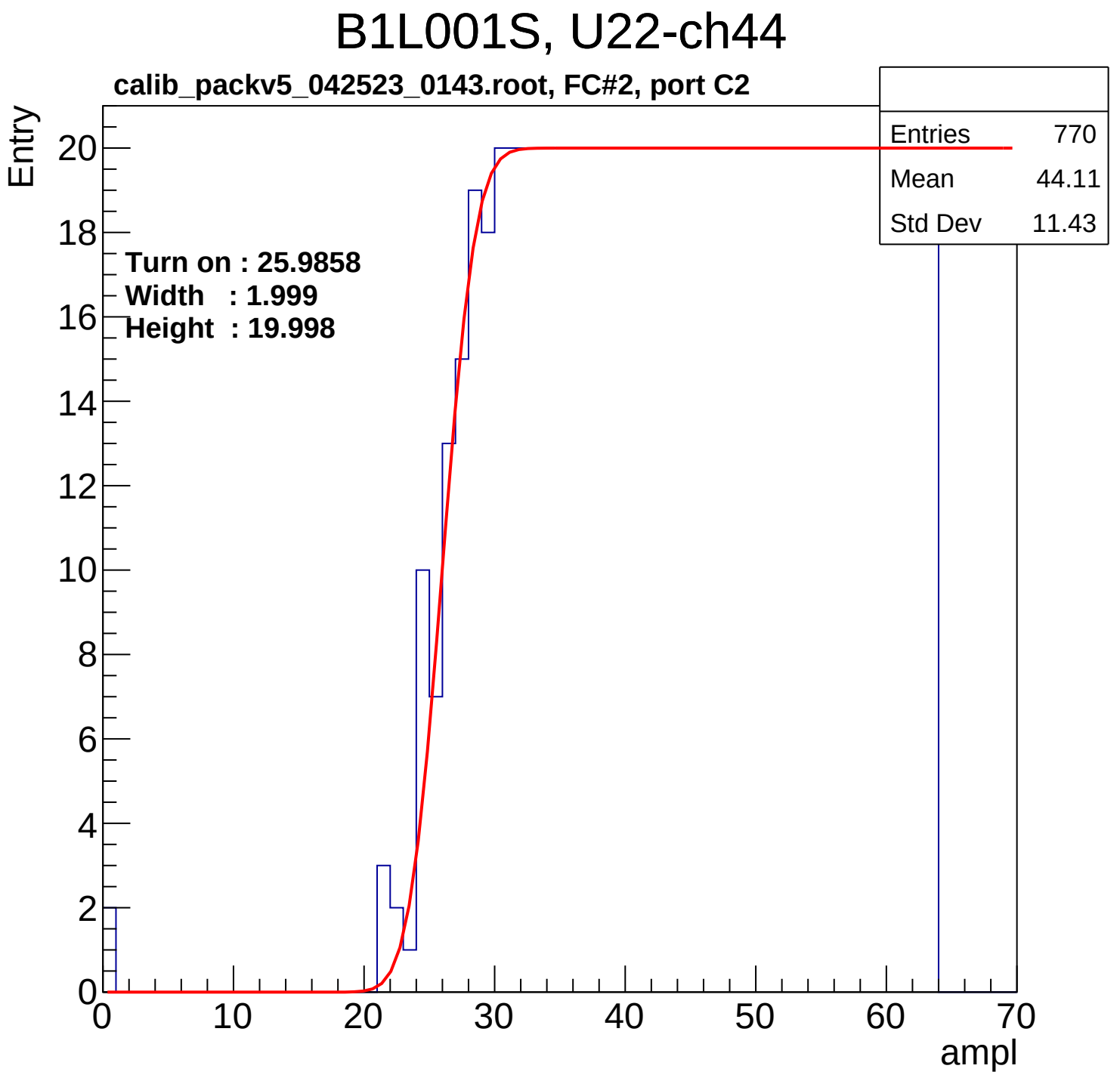
B1L001S, U22-ch44
calib_packv5_042523_0143.root, FC#2, port C2
Entries 770
Mean 44.11
Std Dev 11.43
Turn on : 25.9858
Width : 1.999
Height : 19.998
Entry
ampl
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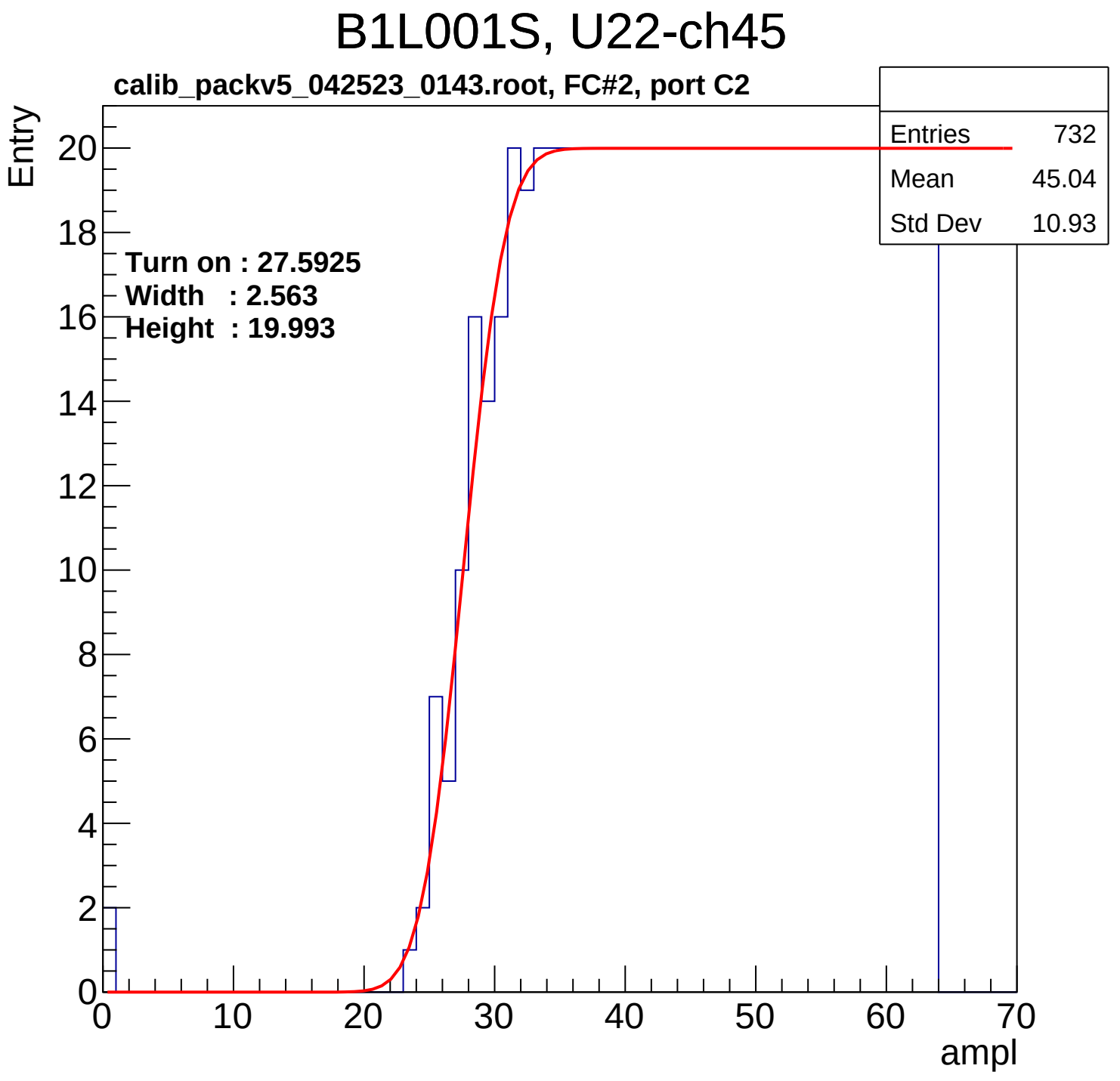
B1L001S, U22-ch45
calib_packv5_042523_0143.root, FC#2, port C2
Entries 732
Mean 45.04
Std Dev 10.93
Turn on : 27.5925
Width : 2.563
Height : 19.993
Entry
ampl
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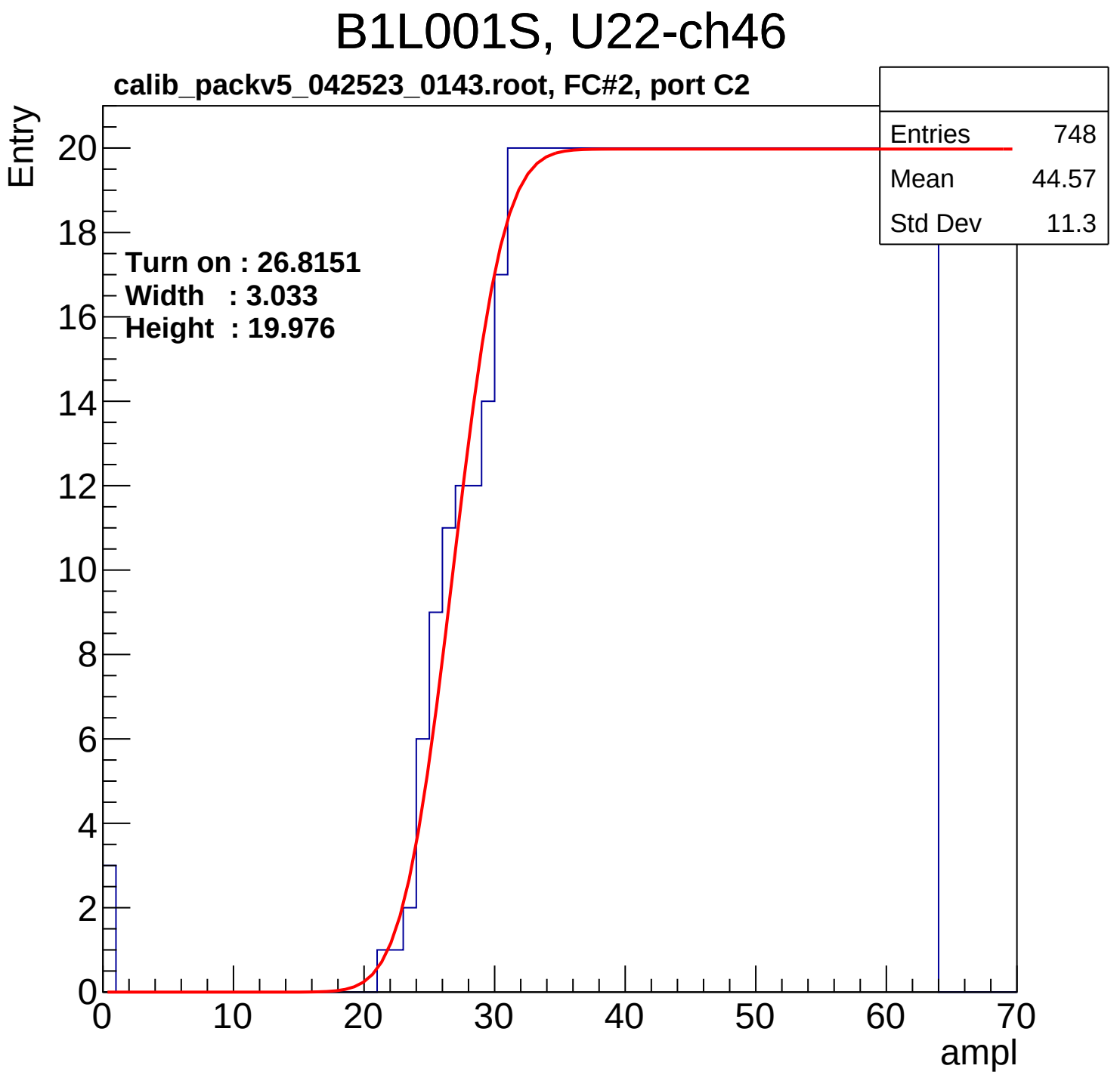
B1L001S, U22-ch46
calib_packv5_042523_0143.root, FC#2, port C2
Entries 748
Mean 44.57
Std Dev 11.3
Turn on : 26.8151
Width : 3.033
Height : 19.976
Entry
ampl
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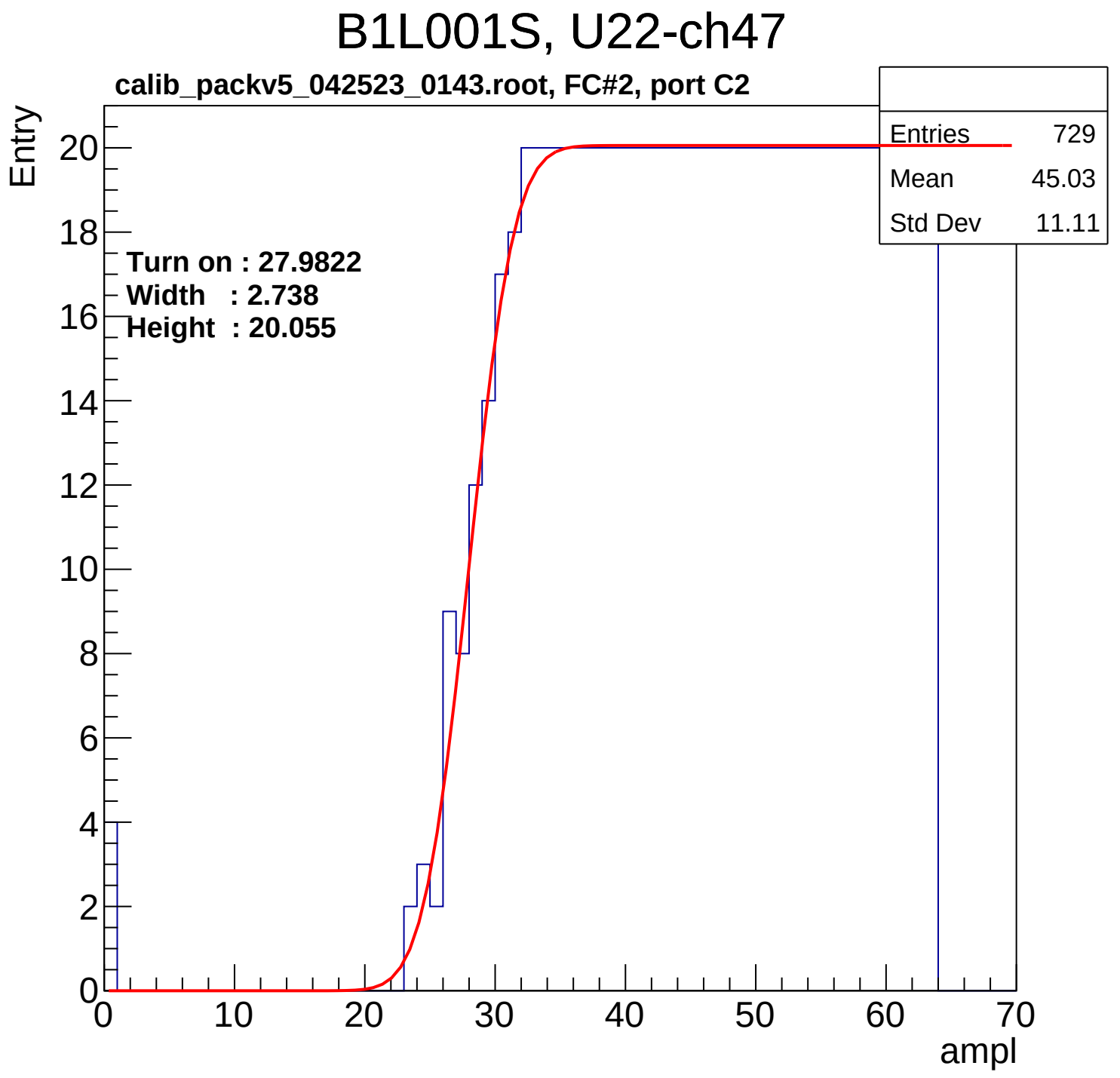
B1L001S, U22-ch47
calib_packv5_042523_0143.root, FC#2, port C2
Entries 729
Mean 45.03
Std Dev 11.11
Turn on : 27.9822
Width : 2.738
Height : 20.055
Entry
ampl
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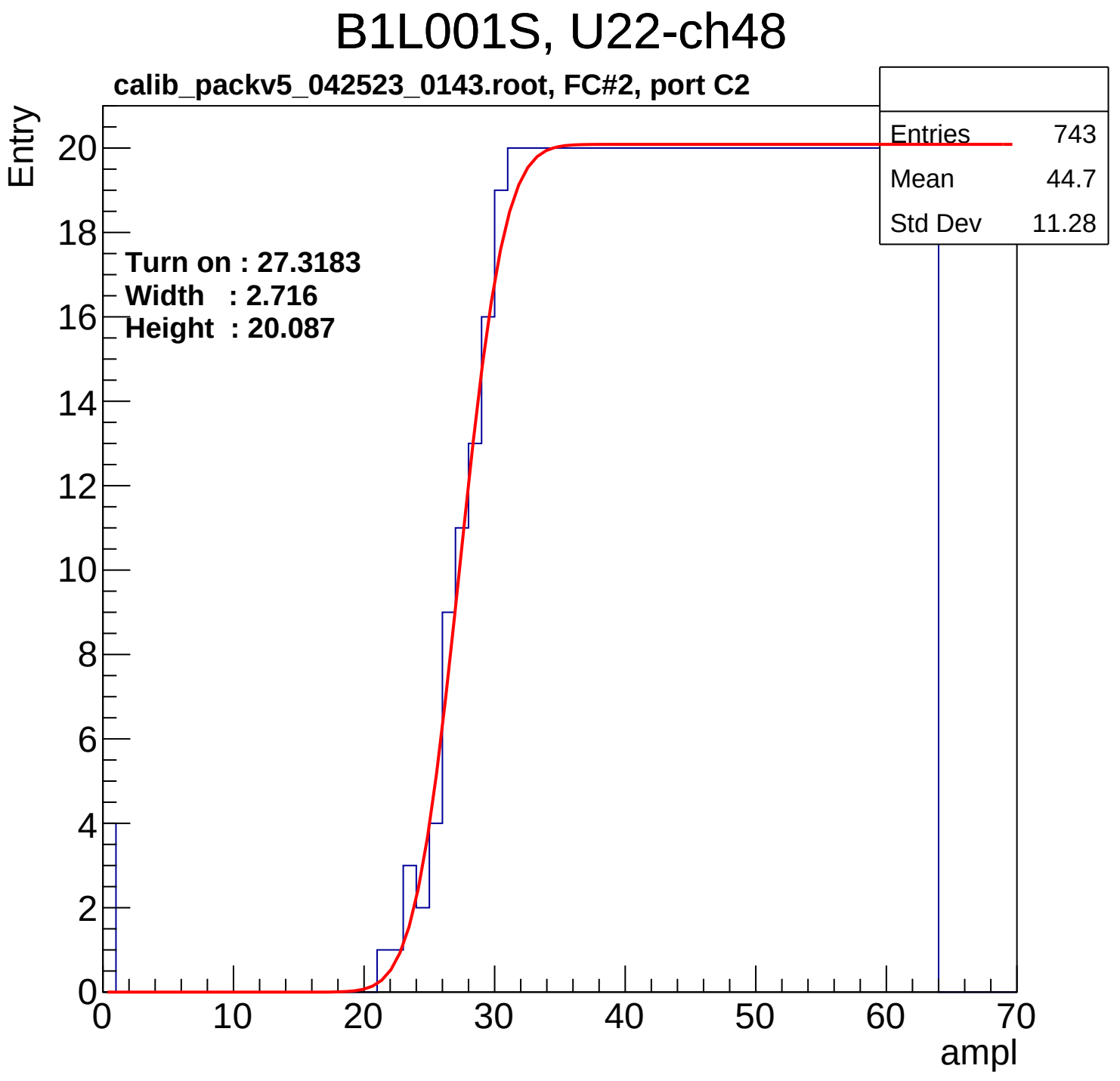
B1L001S, U22-ch48
calib_packv5_042523_0143.root, FC#2, port C2
Entries 743
Mean 44.7
Std Dev 11.28
Turn on : 27.3183
Width : 2.716
Height : 20.087
Entry
ampl
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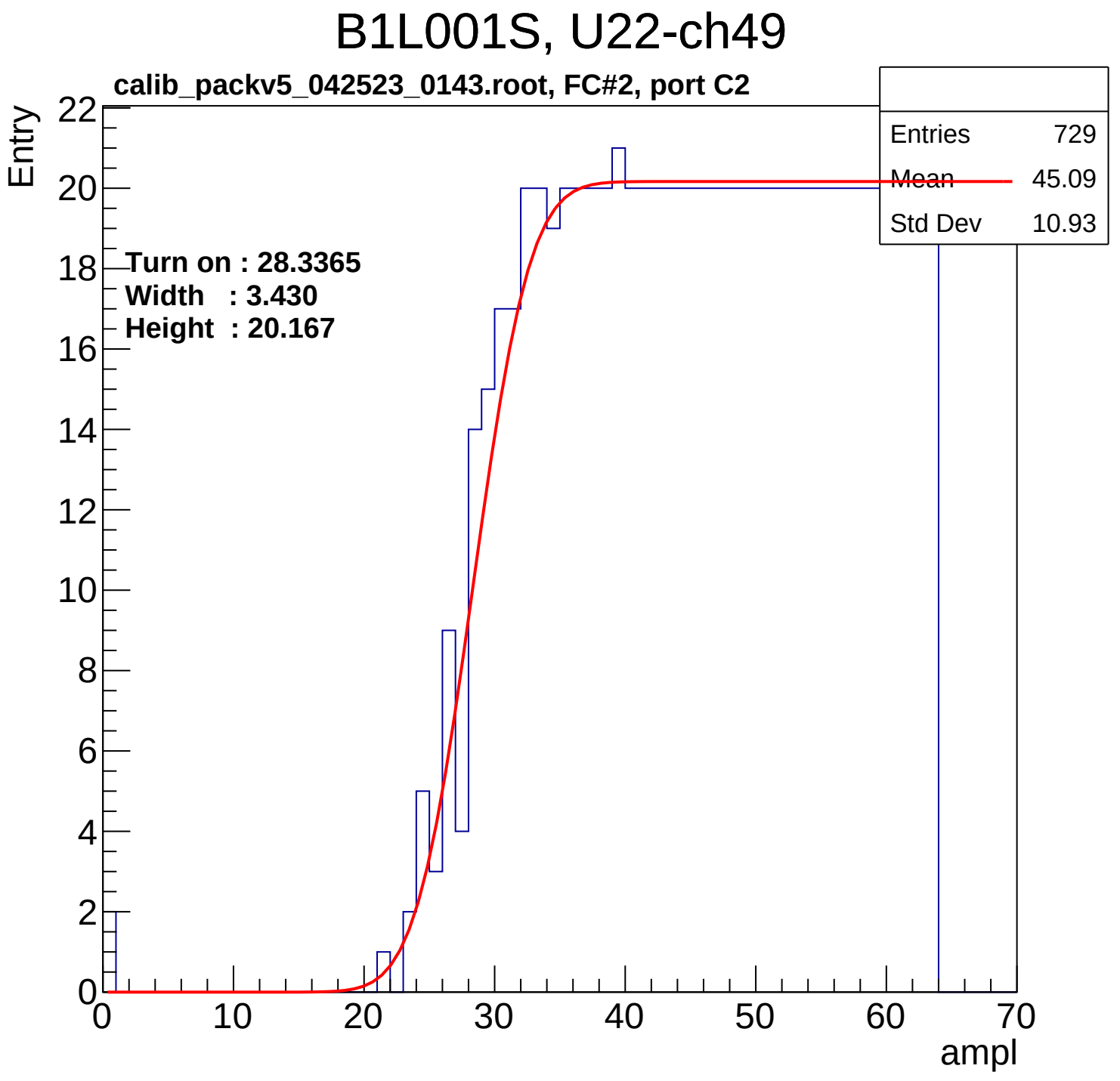
B1L001S, U22-ch49
calib_packv5_042523_0143.root, FC#2, port C2
Entries 729
Mean 45.09
Std Dev 10.93
Turn on : 28.3365
Width : 3.430
Height : 20.167
Entry
ampl
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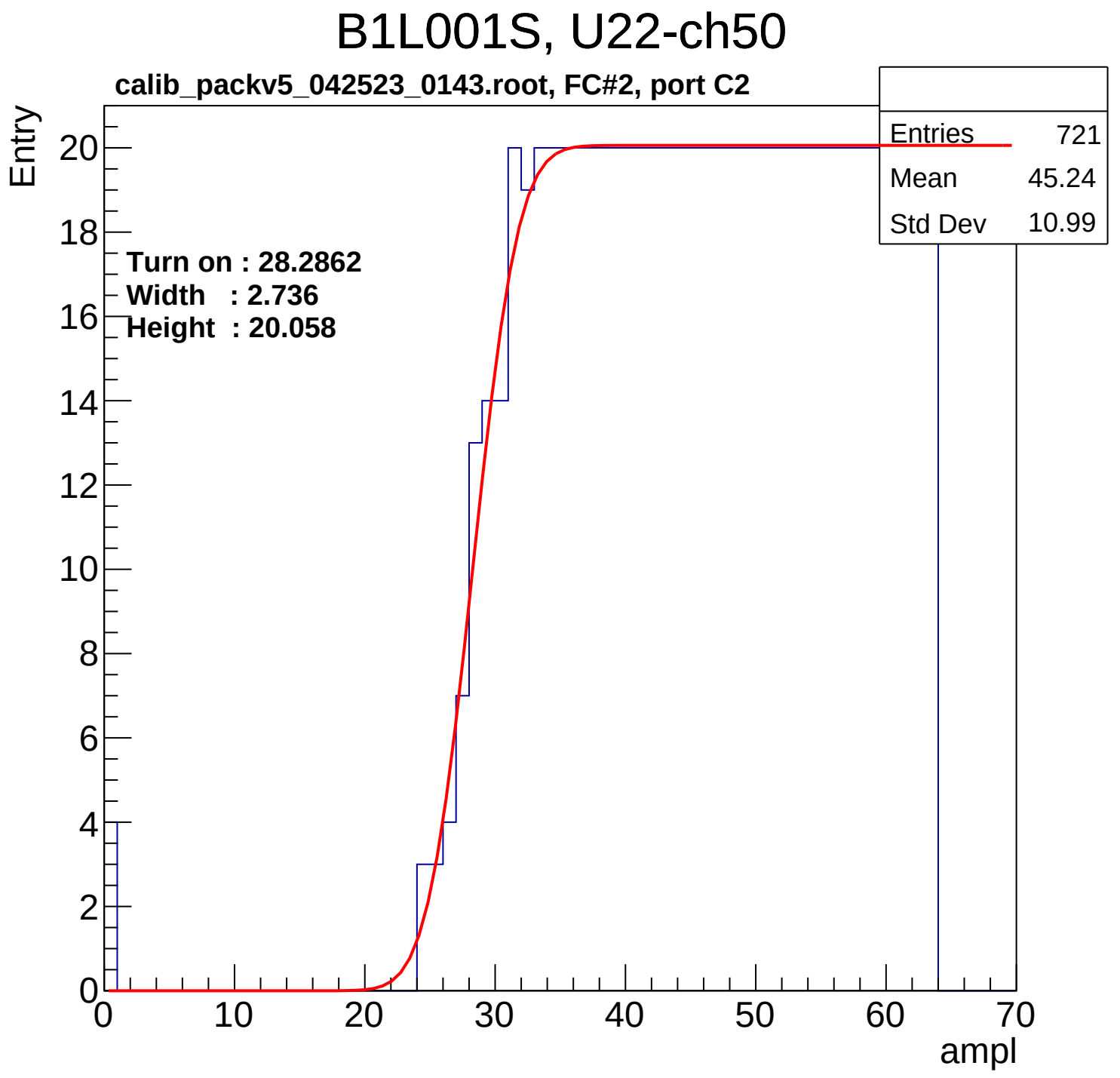
B1L001S, U22-ch50
calib_packv5_042523_0143.root, FC#2, port C2
Entries 721
Mean 45.24
Std Dev 10.99
Turn on : 28.2862
Width : 2.736
Height : 20.058
Entry
ampl
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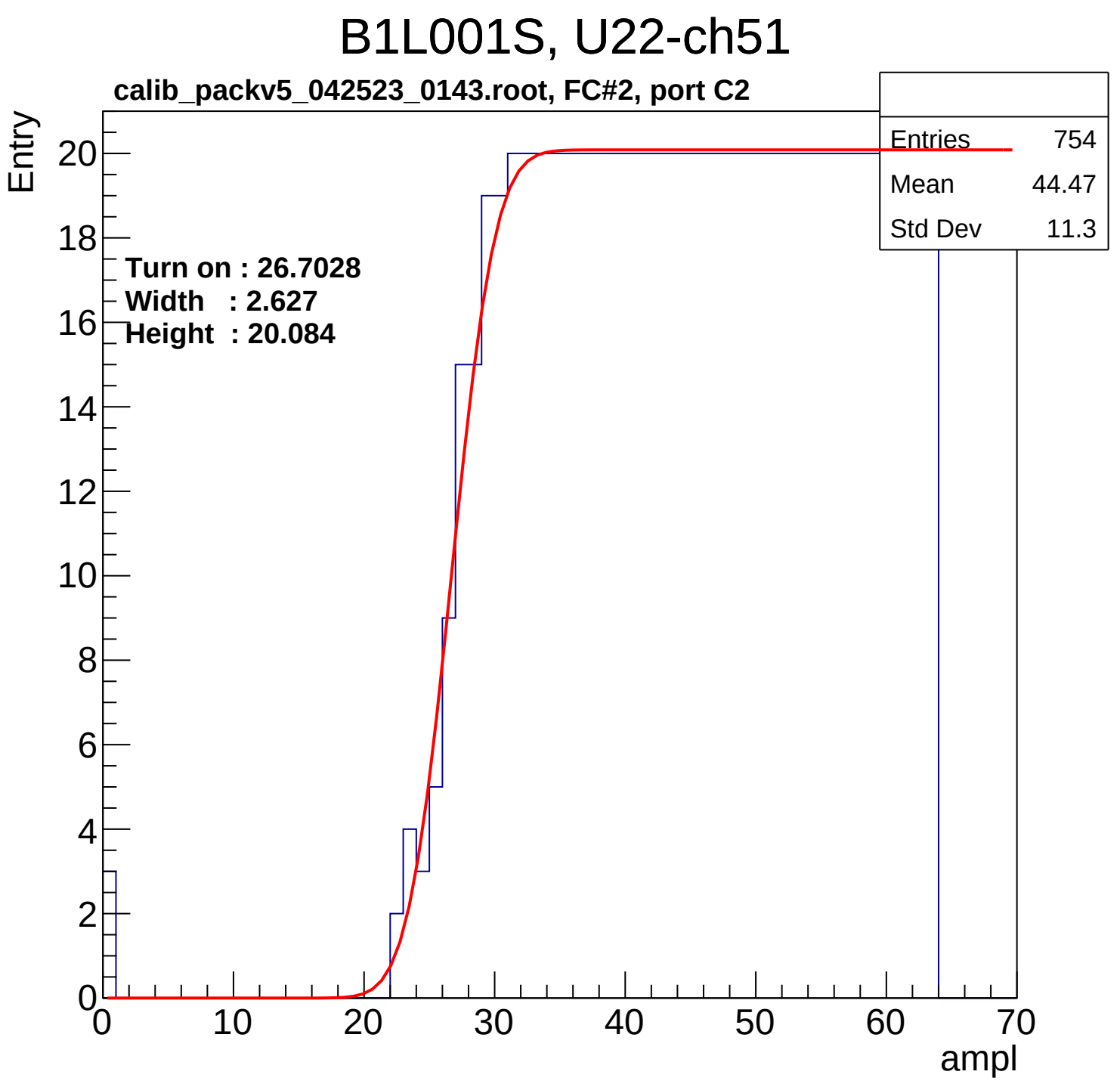
B1L001S, U22-ch51
calib_packv5_042523_0143.root, FC#2, port C2
Entries 754
Mean 44.47
Std Dev 11.3
Turn on : 26.7028
Width : 2.627
Height : 20.084
Entry
ampl
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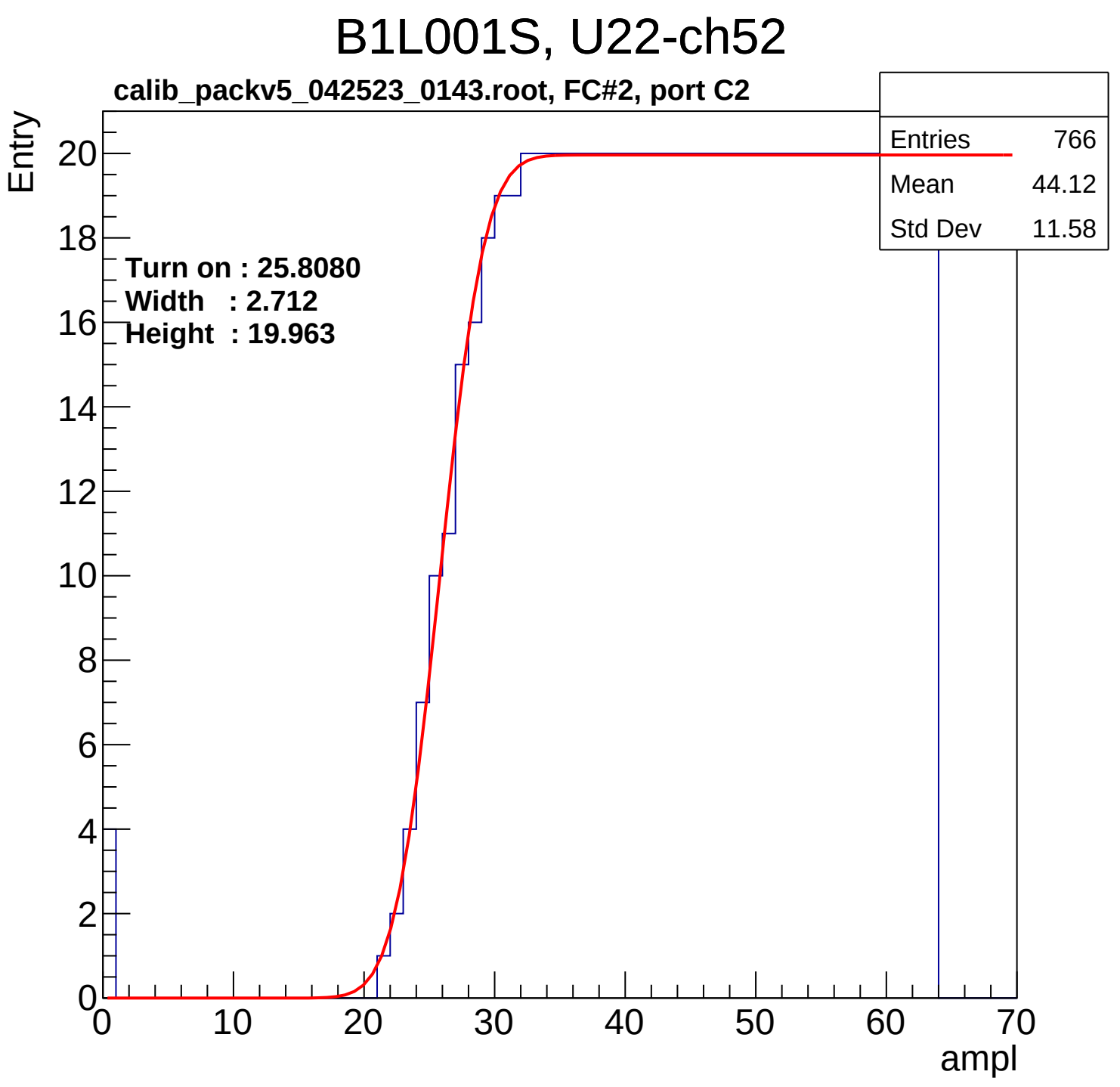
B1L001S, U22-ch52
calib_packv5_042523_0143.root, FC#2, port C2
Entries 766
Mean 44.12
Std Dev 11.58
Turn on : 25.8080
Width : 2.712
Height : 19.963
Entry
ampl
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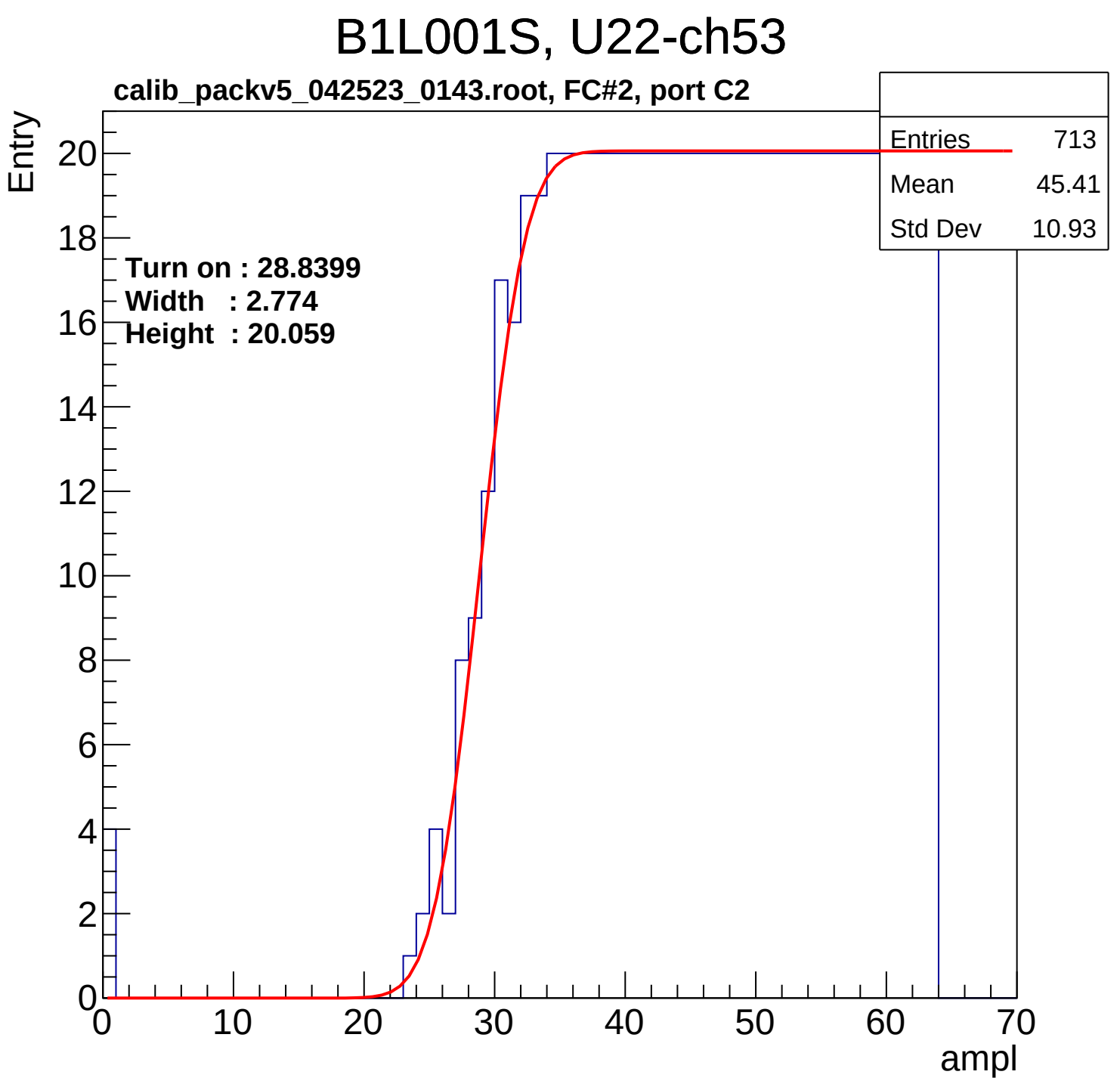
B1L001S, U22-ch53
calib_packv5_042523_0143.root, FC#2, port C2
Entries 713
Mean 45.41
Std Dev 10.93
Turn on : 28.8399
Width : 2.774
Height : 20.059
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ampl
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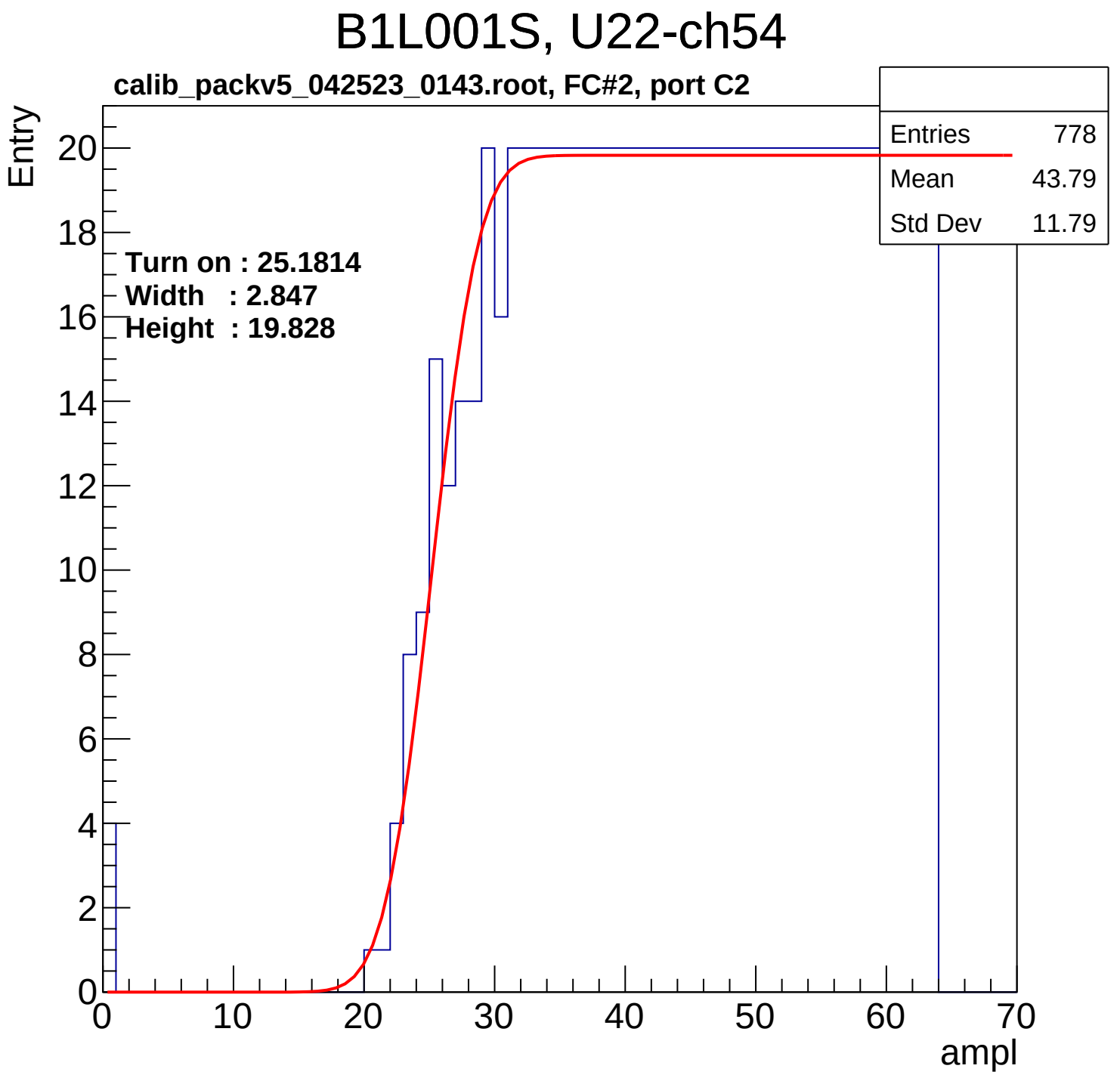
B1L001S, U22-ch54
calib_packv5_042523_0143.root, FC#2, port C2
Entries 778
Mean 43.79
Std Dev 11.79
Turn on : 25.1814
Width : 2.847
Height : 19.828
Entry
ampl
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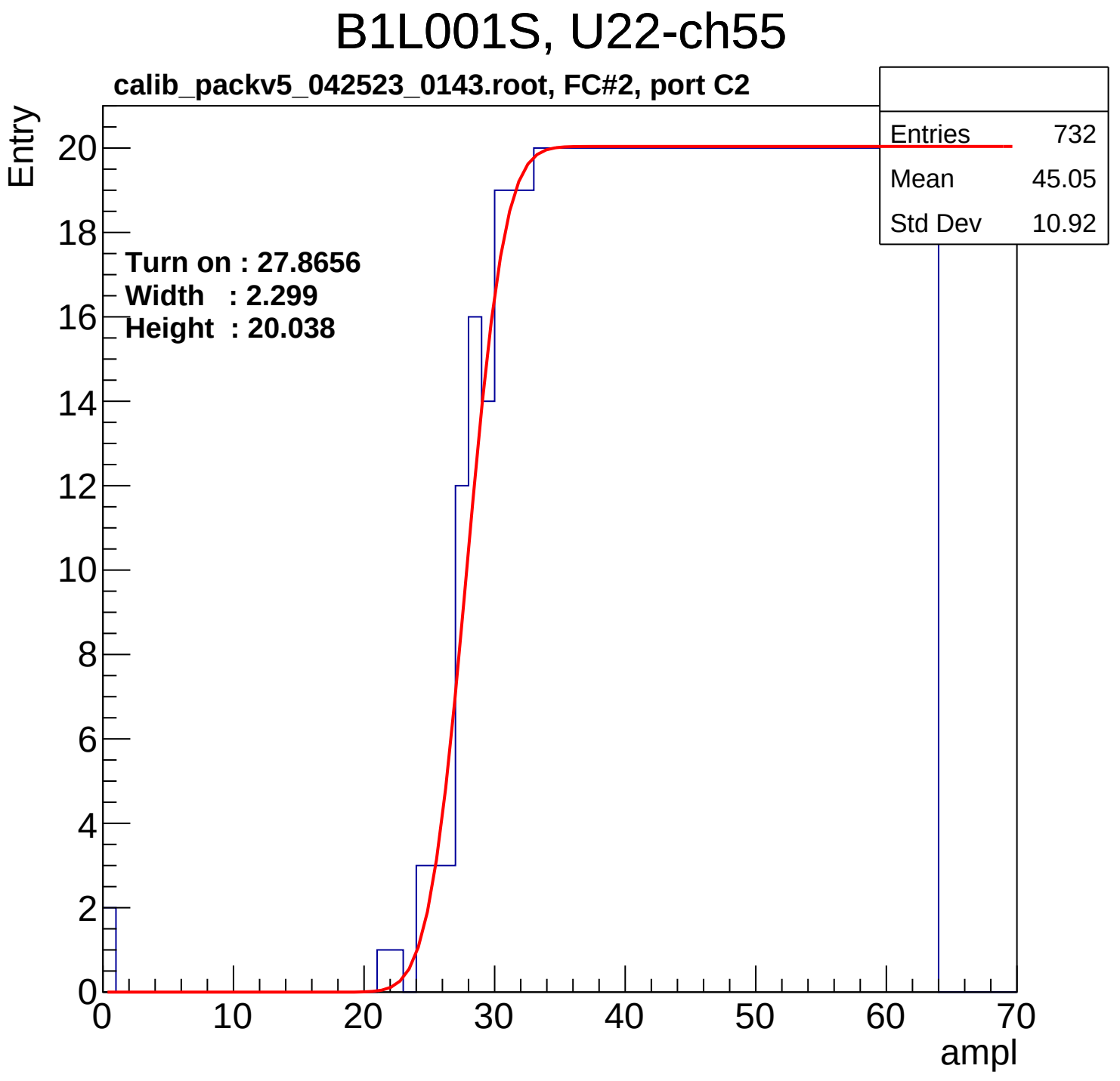
B1L001S, U22-ch55
calib_packv5_042523_0143.root, FC#2, port C2
Entries 732
Mean 45.05
Std Dev 10.92
Turn on : 27.8656
Width : 2.299
Height : 20.038
Entry
ampl
0
2
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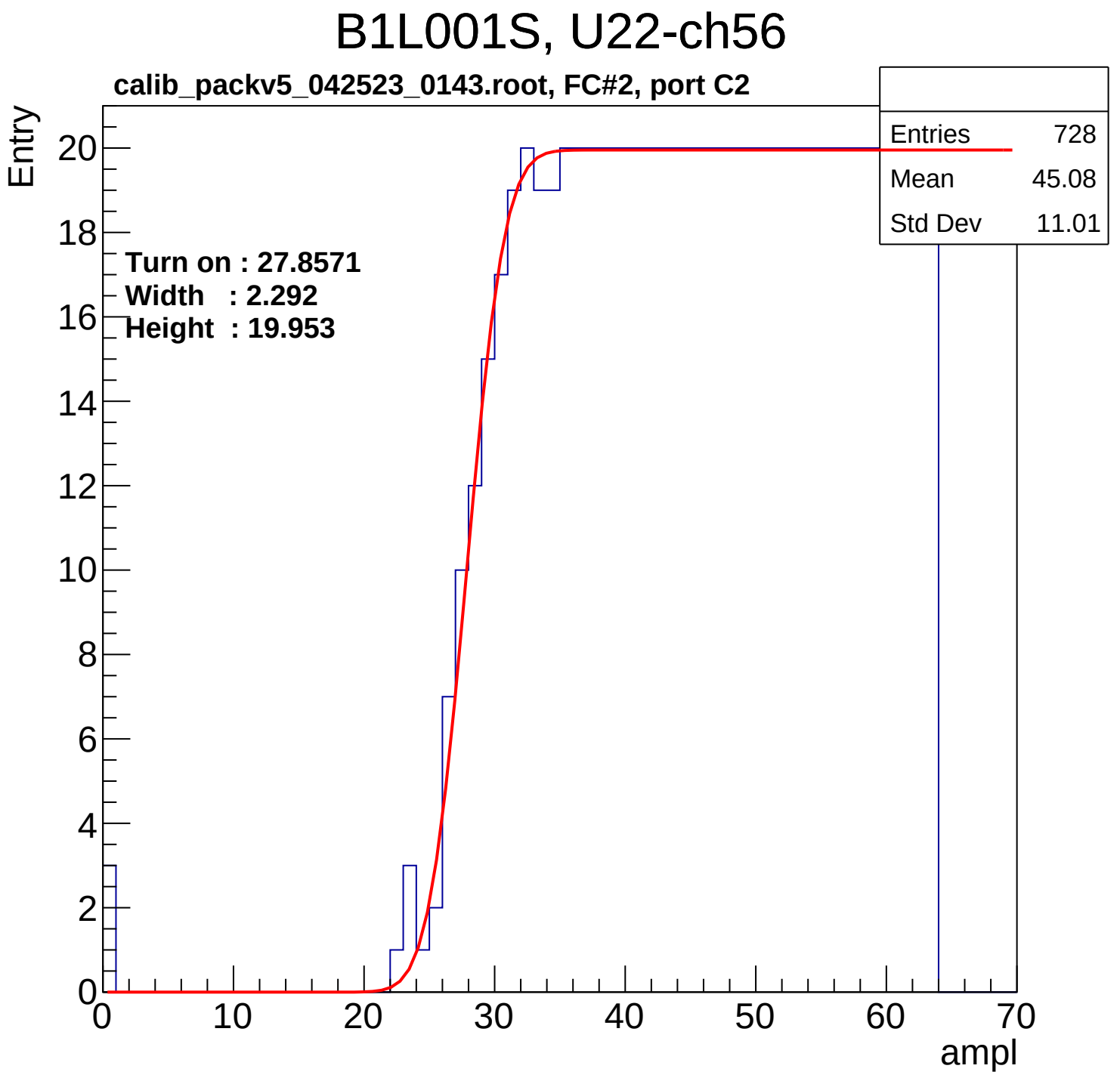
B1L001S, U22-ch56
calib_packv5_042523_0143.root, FC#2, port C2
Entries 728
Mean 45.08
Std Dev 11.01
Turn on : 27.8571
Width : 2.292
Height : 19.953
Entry
ampl
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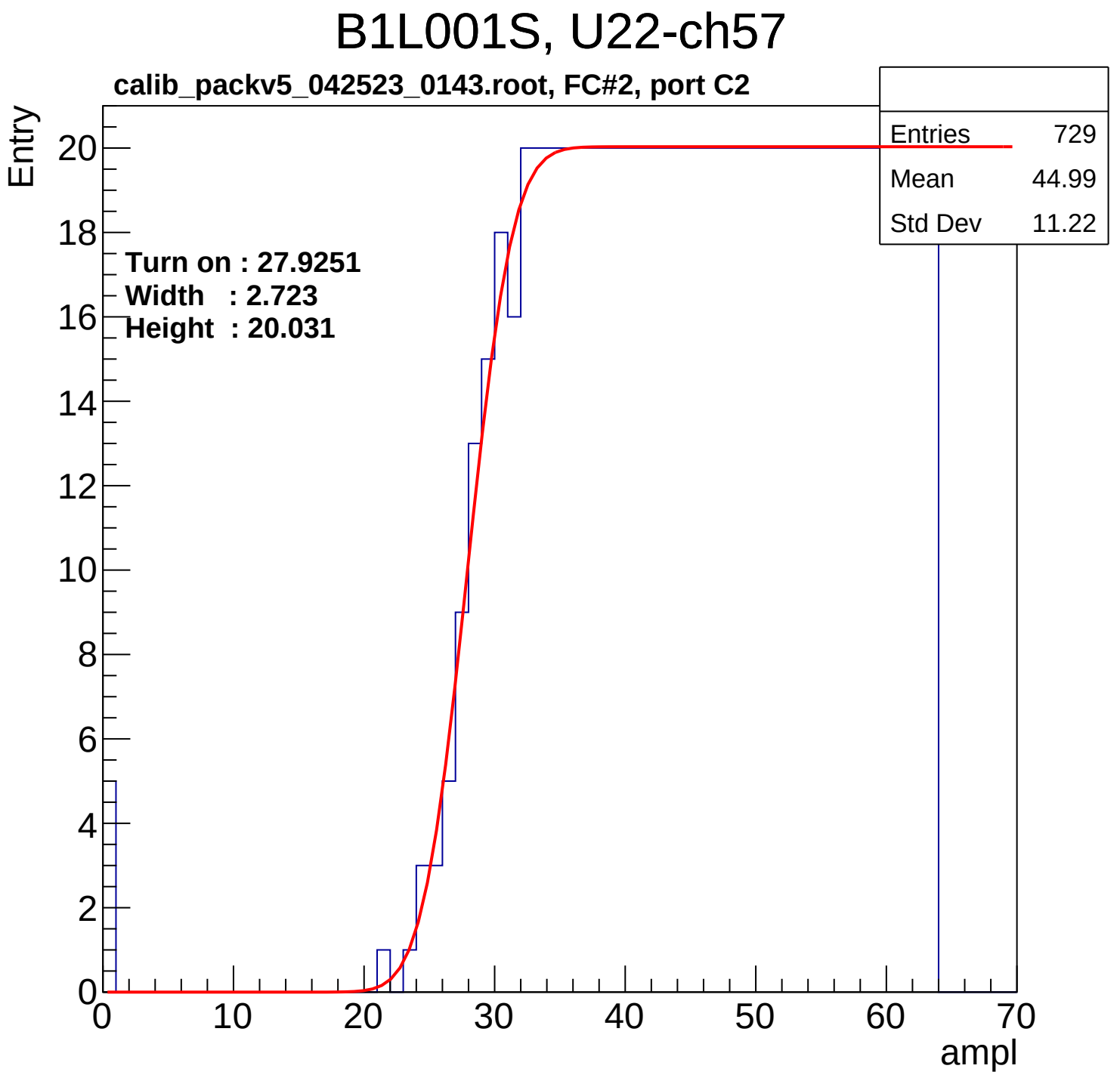
B1L001S, U22-ch57
calib_packv5_042523_0143.root, FC#2, port C2
Entries 729
Mean 44.99
Std Dev 11.22
Turn on : 27.9251
Width : 2.723
Height : 20.031
Entry
ampl
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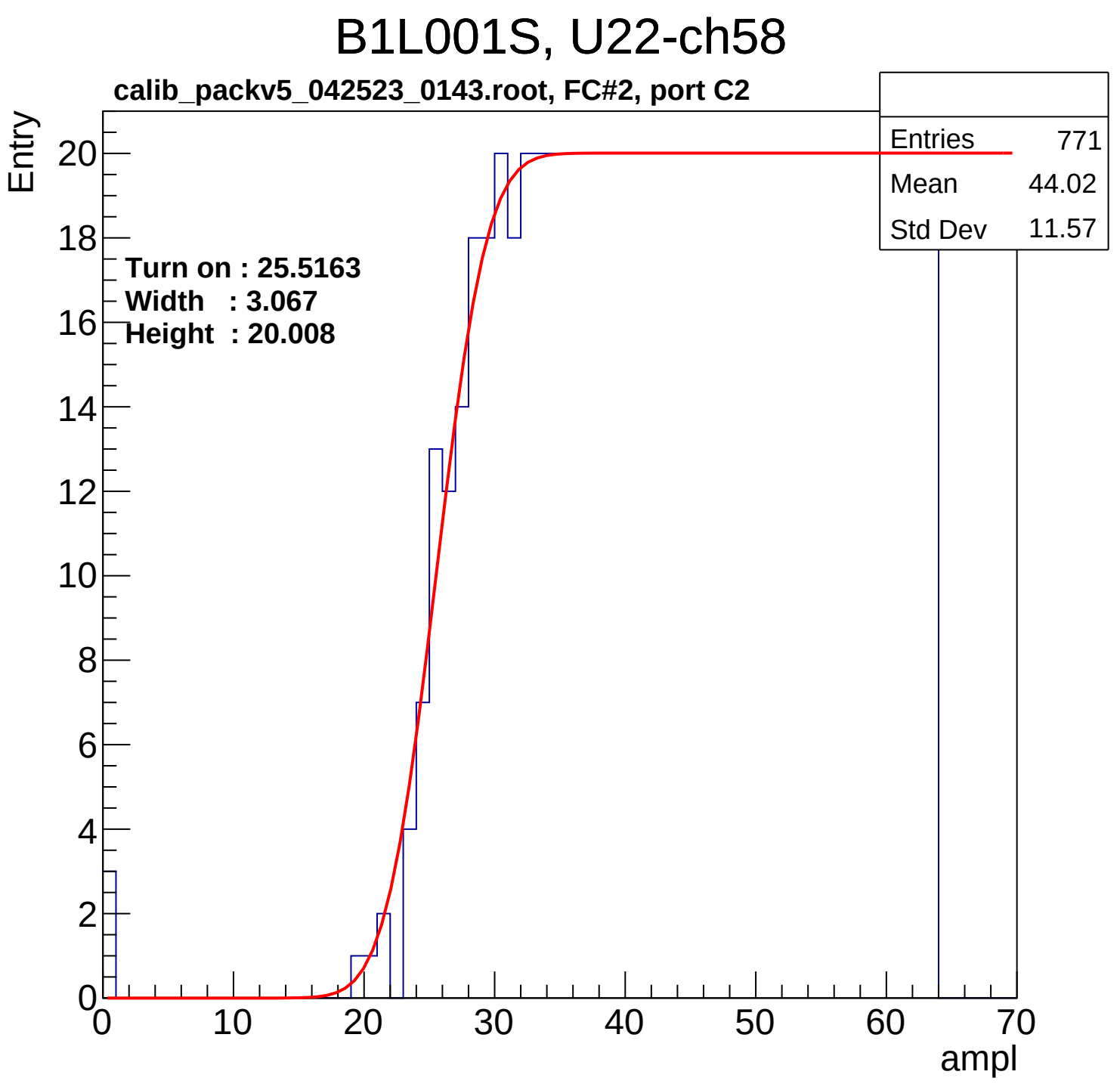
B1L001S, U22-ch58
calib_packv5_042523_0143.root, FC#2, port C2
Entries 771
Mean 44.02
Std Dev 11.57
Turn on : 25.5163
Width : 3.067
Height : 20.008
Entry
ampl
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8
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16
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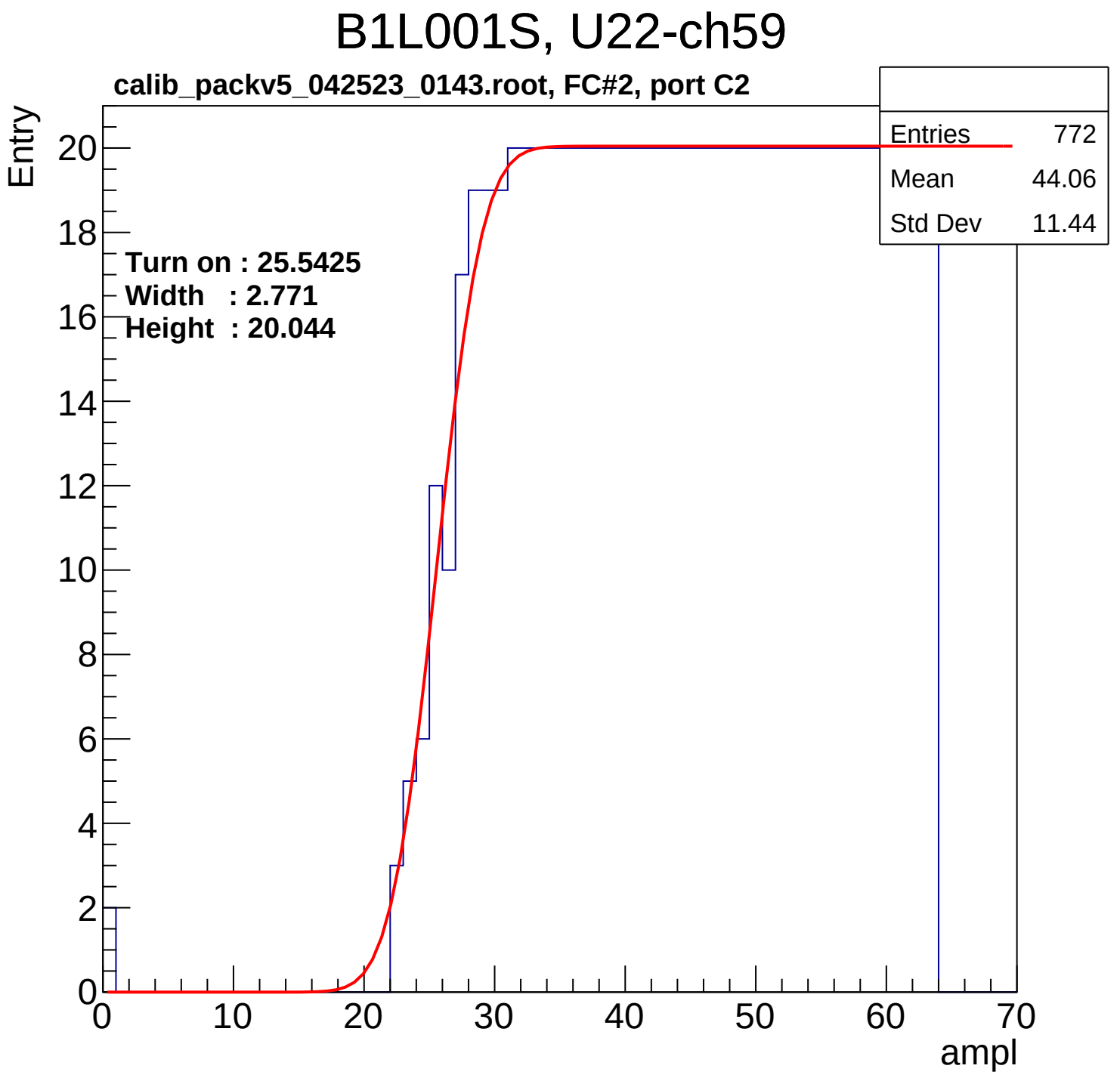
B1L001S, U22-ch59
calib_packv5_042523_0143.root, FC#2, port C2
Entries 772
Mean 44.06
Std Dev 11.44
Turn on : 25.5425
Width : 2.771
Height : 20.044
Entry
ampl
0
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6
8
10
12
14
16
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0
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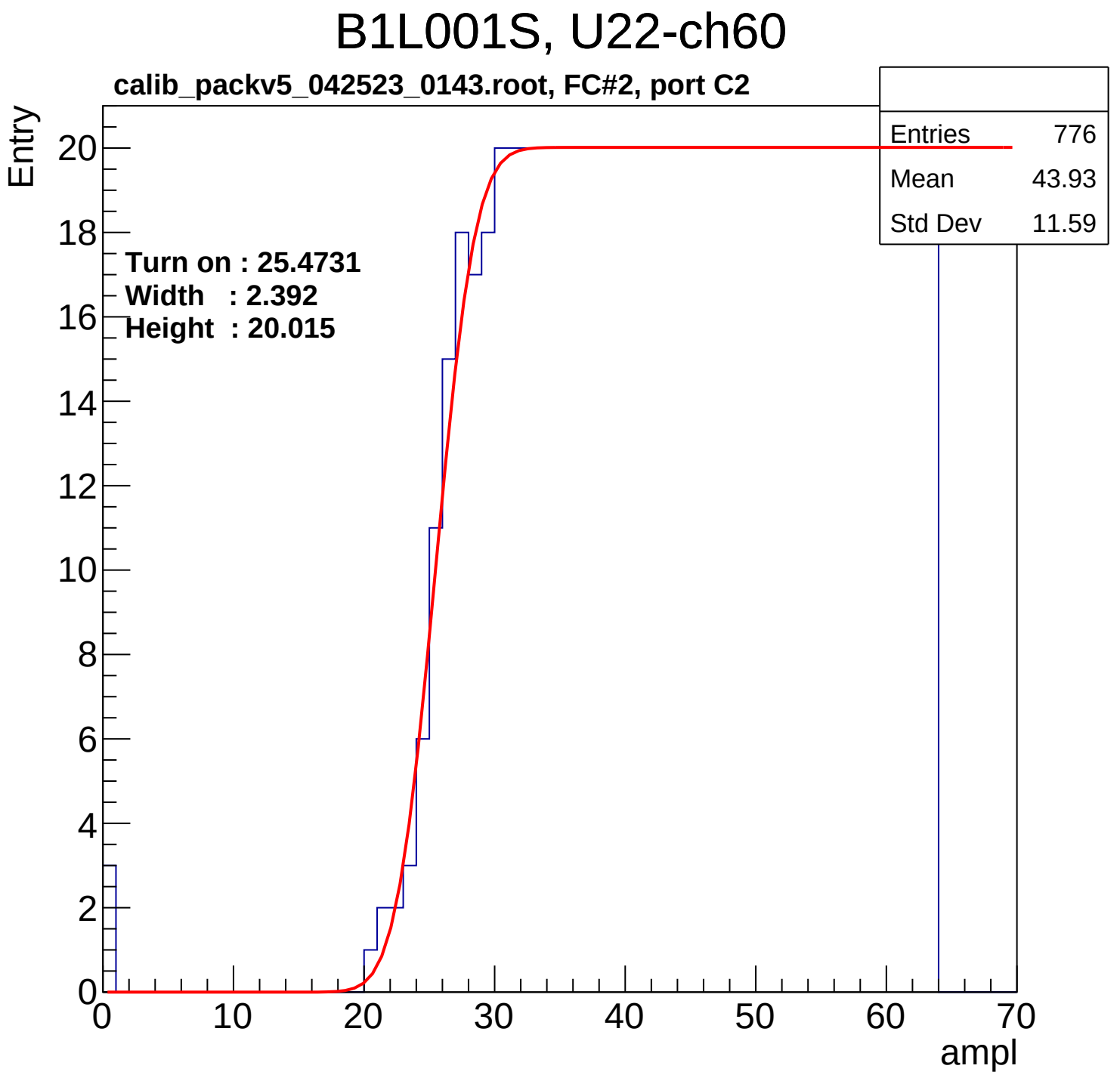
B1L001S, U22-ch60
calib_packv5_042523_0143.root, FC#2, port C2
Entries 776
Mean 43.93
Std Dev 11.59
Turn on : 25.4731
Width : 2.392
Height : 20.015
Entry
ampl
0
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4
6
8
10
12
14
16
18
20
0
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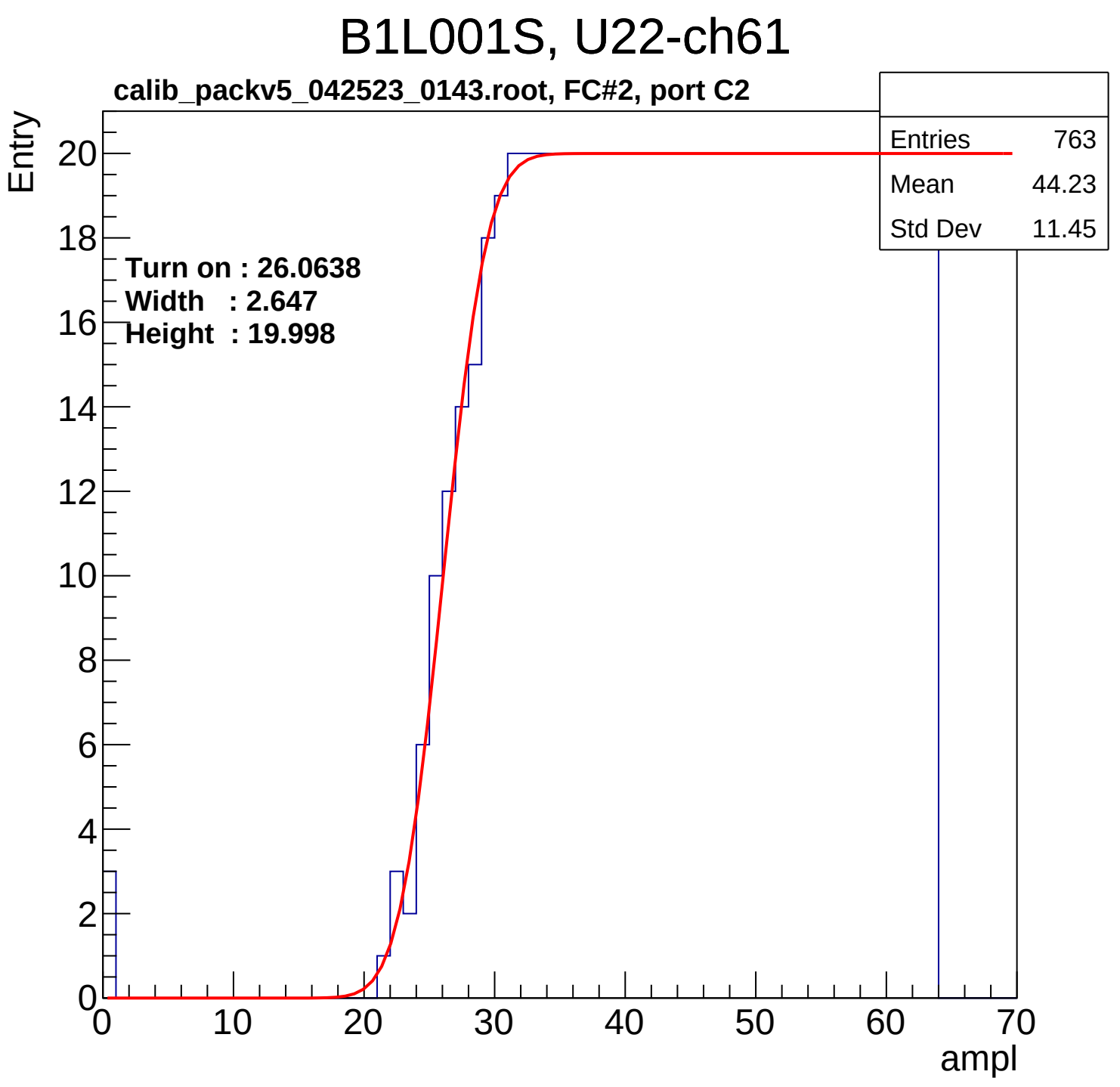
B1L001S, U22-ch61
calib_packv5_042523_0143.root, FC#2, port C2
Entries 763
Mean 44.23
Std Dev 11.45
Turn on : 26.0638
Width : 2.647
Height : 19.998
Entry
ampl
0
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4
6
8
10
12
14
16
18
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0
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60
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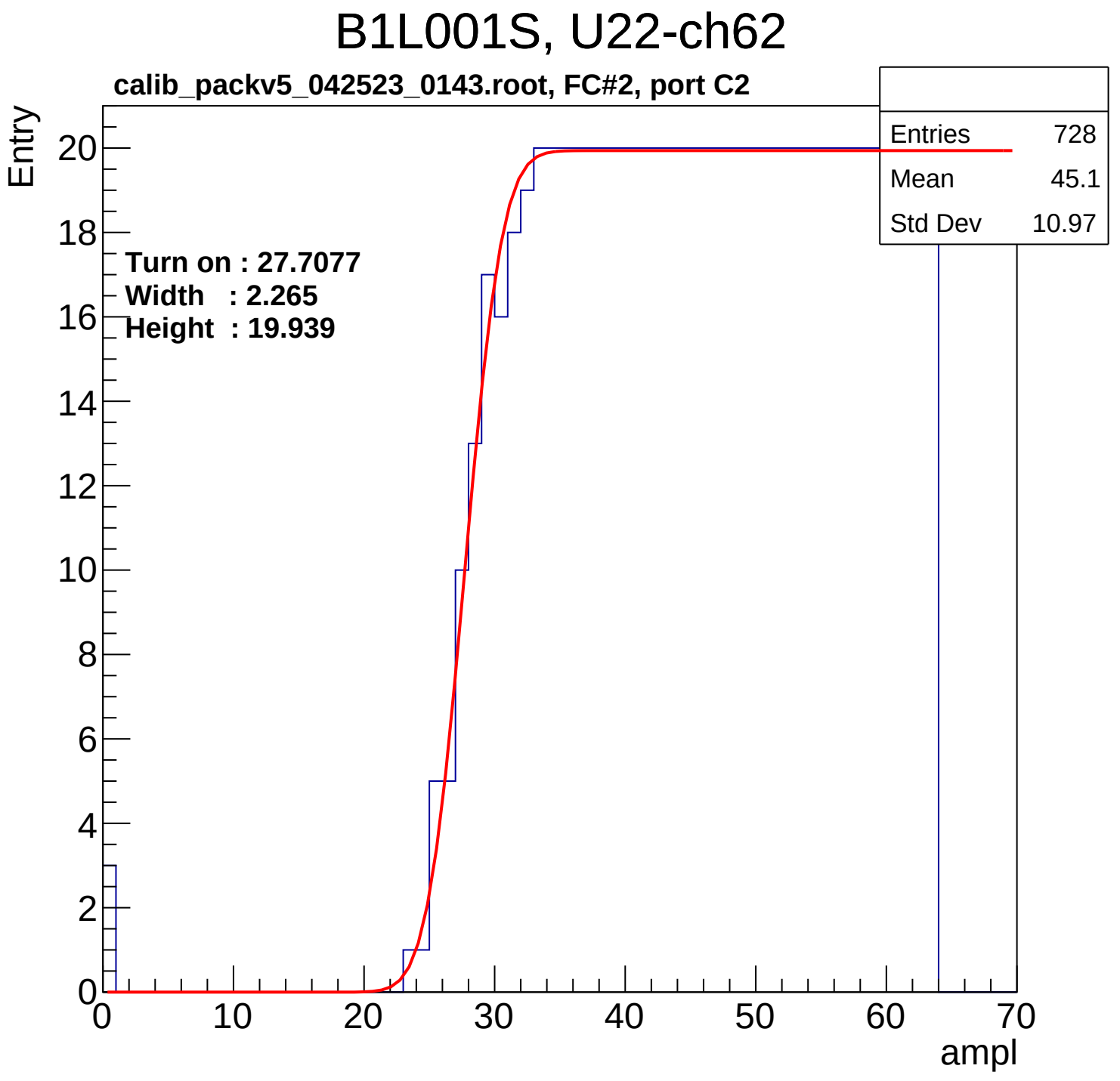
B1L001S, U22-ch62
calib_packv5_042523_0143.root, FC#2, port C2
Entries 728
Mean 45.1
Std Dev 10.97
Turn on : 27.7077
Width : 2.265
Height : 19.939
Entry
ampl
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6
8
10
12
14
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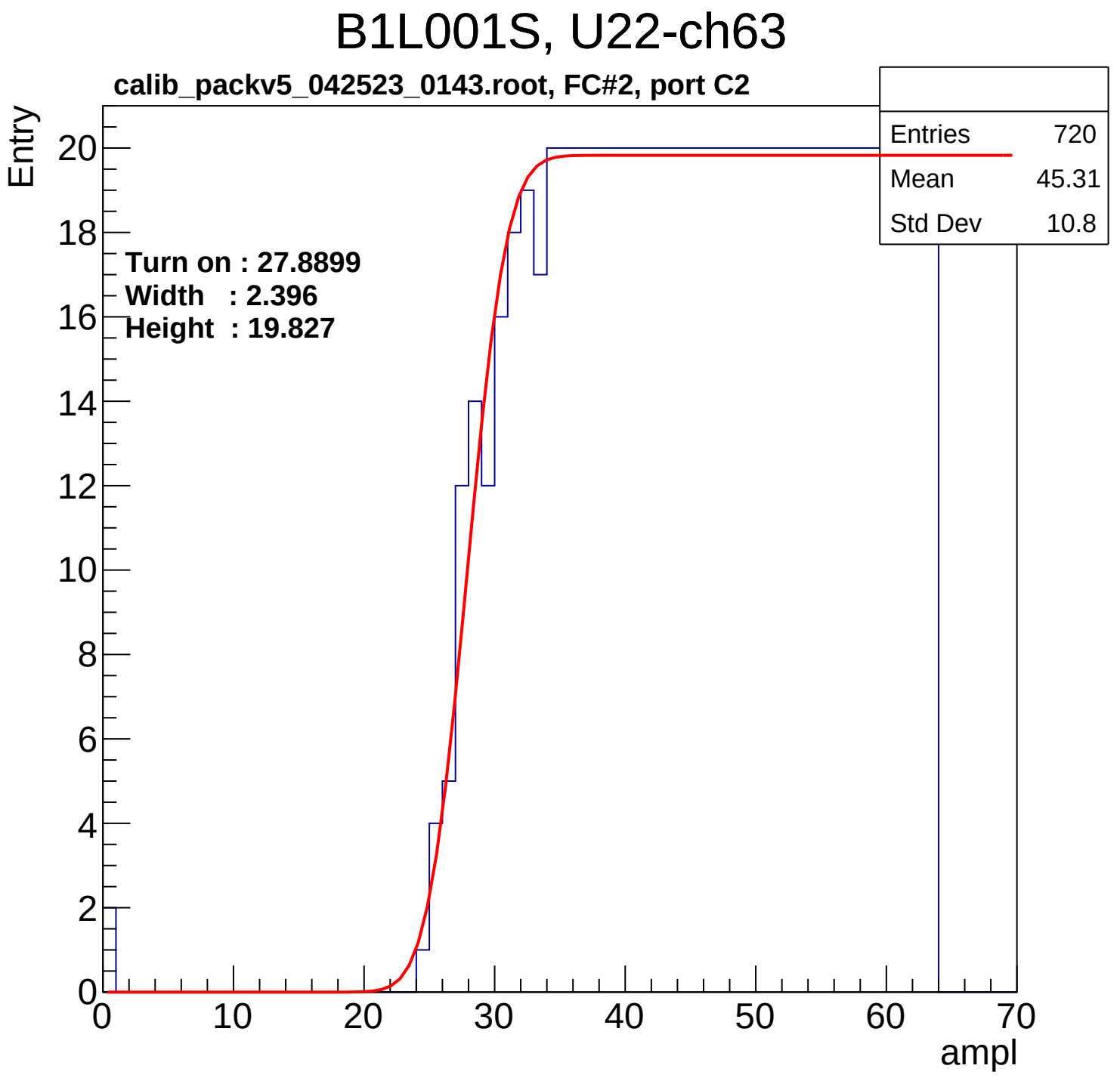
B1L001S, U22-ch63
calib_packv5_042523_0143.root, FC#2, port C2
Entries 720
Mean 45.31
Std Dev 10.8
Turn on : 27.8899
Width : 2.396
Height : 19.827
Entry
ampl
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6
8
10
12
14
16
18
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0
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60
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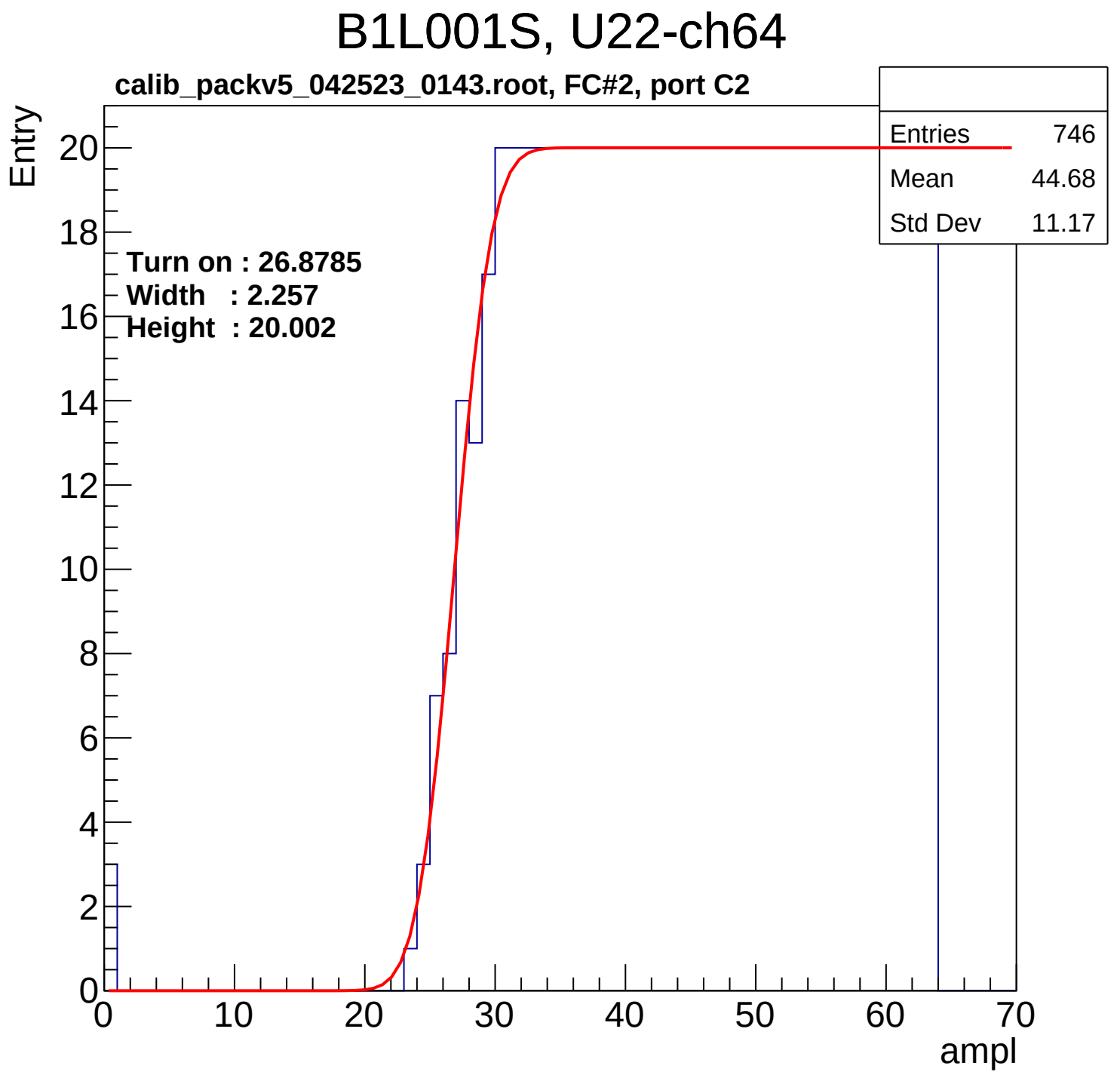
B1L001S, U22-ch64
calib_packv5_042523_0143.root, FC#2, port C2
Entries 746
Mean 44.68
Std Dev 11.17
Turn on : 26.8785
Width : 2.257
Height : 20.002
Entry
ampl
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6
8
10
12
14
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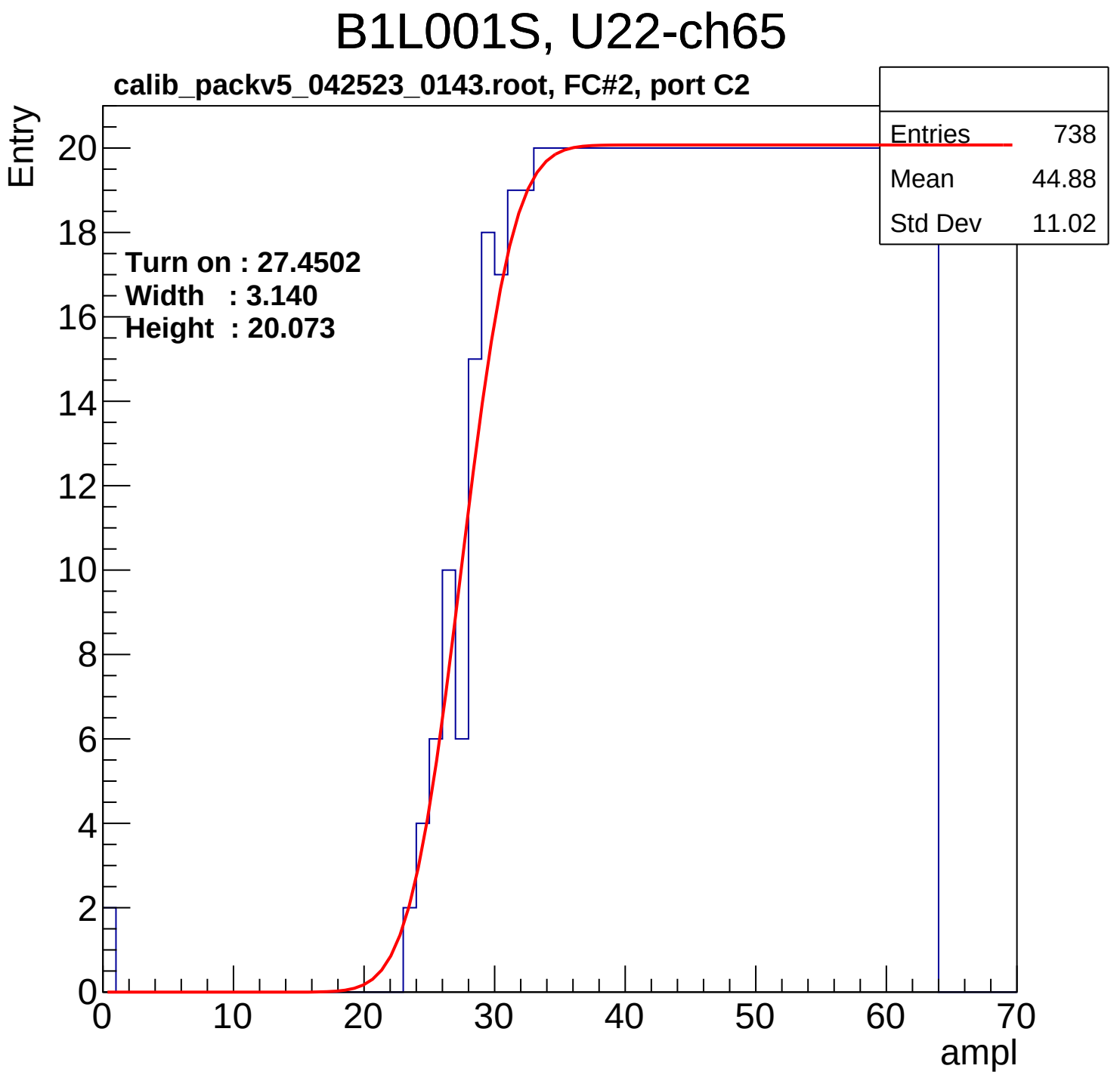
B1L001S, U22-ch65
calib_packv5_042523_0143.root, FC#2, port C2
Entries 738
Mean 44.88
Std Dev 11.02
Turn on : 27.4502
Width : 3.140
Height : 20.073
Entry
ampl
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6
8
10
12
14
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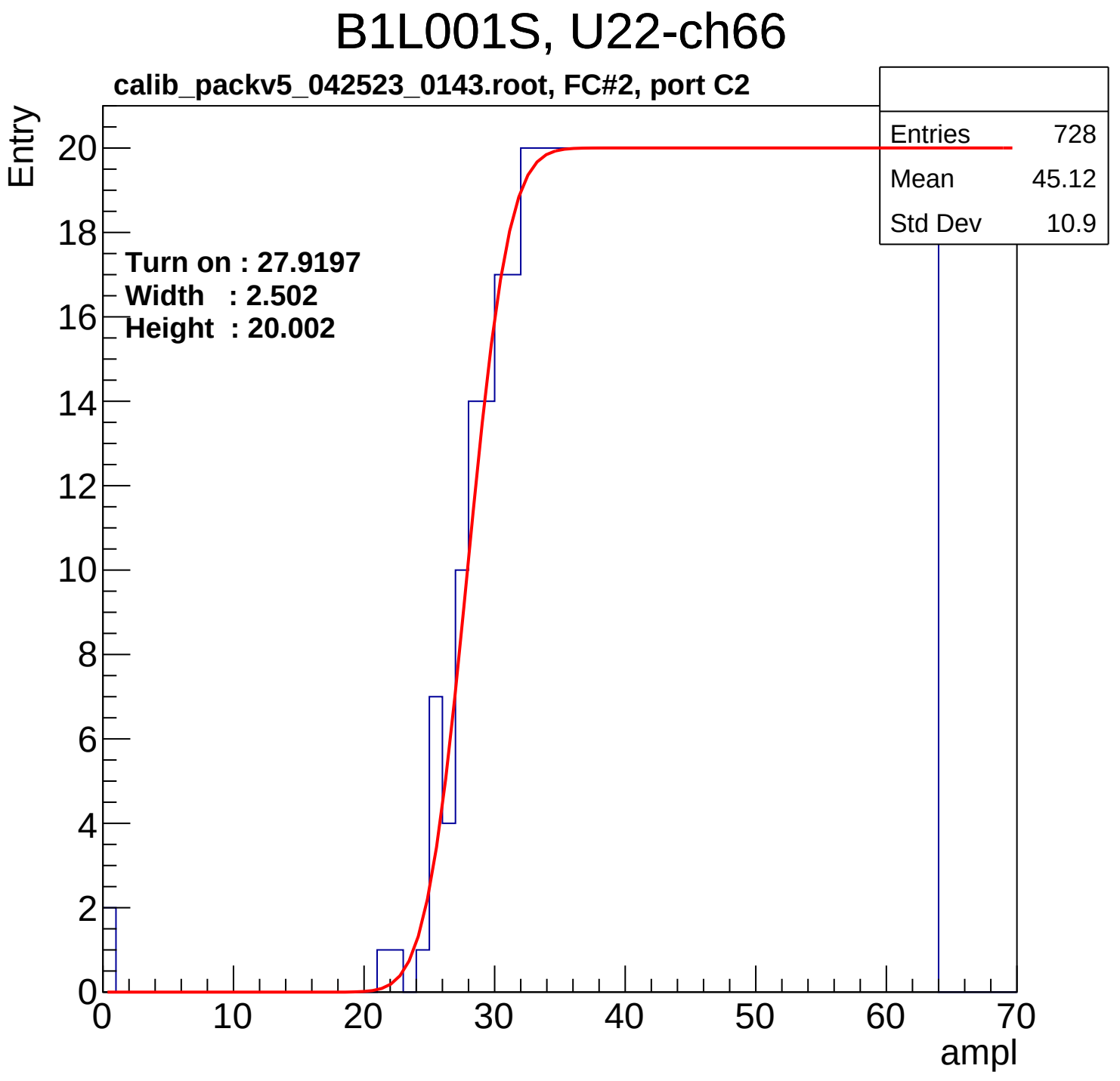
B1L001S, U22-ch66
calib_packv5_042523_0143.root, FC#2, port C2
Entries 728
Mean 45.12
Std Dev 10.9
Turn on : 27.9197
Width : 2.502
Height : 20.002
Entry
ampl
0
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6
8
10
12
14
16
18
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0
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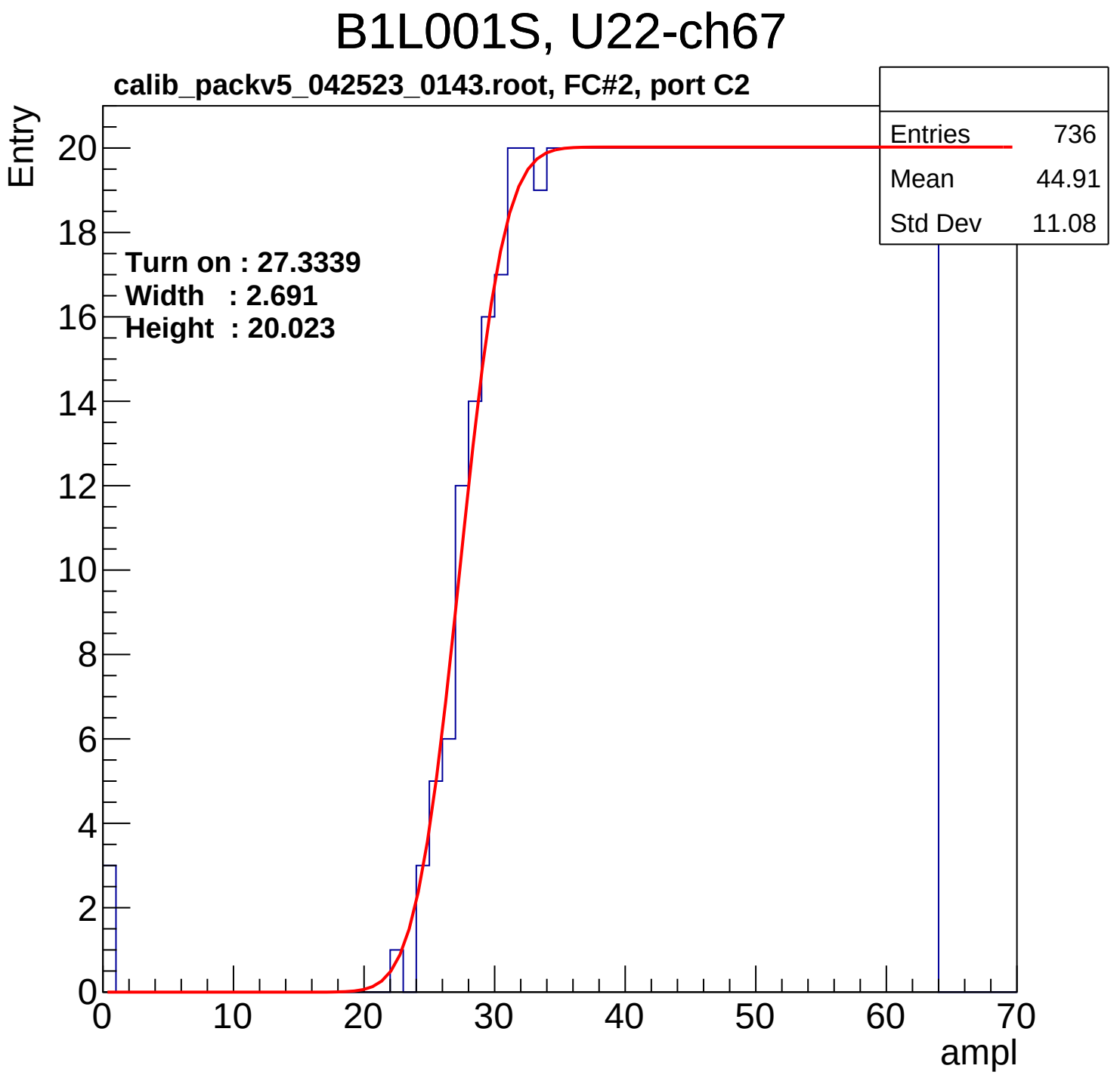
B1L001S, U22-ch67
calib_packv5_042523_0143.root, FC#2, port C2
Entries 736
Mean 44.91
Std Dev 11.08
Turn on : 27.3339
Width : 2.691
Height : 20.023
Entry
ampl
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6
8
10
12
14
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0
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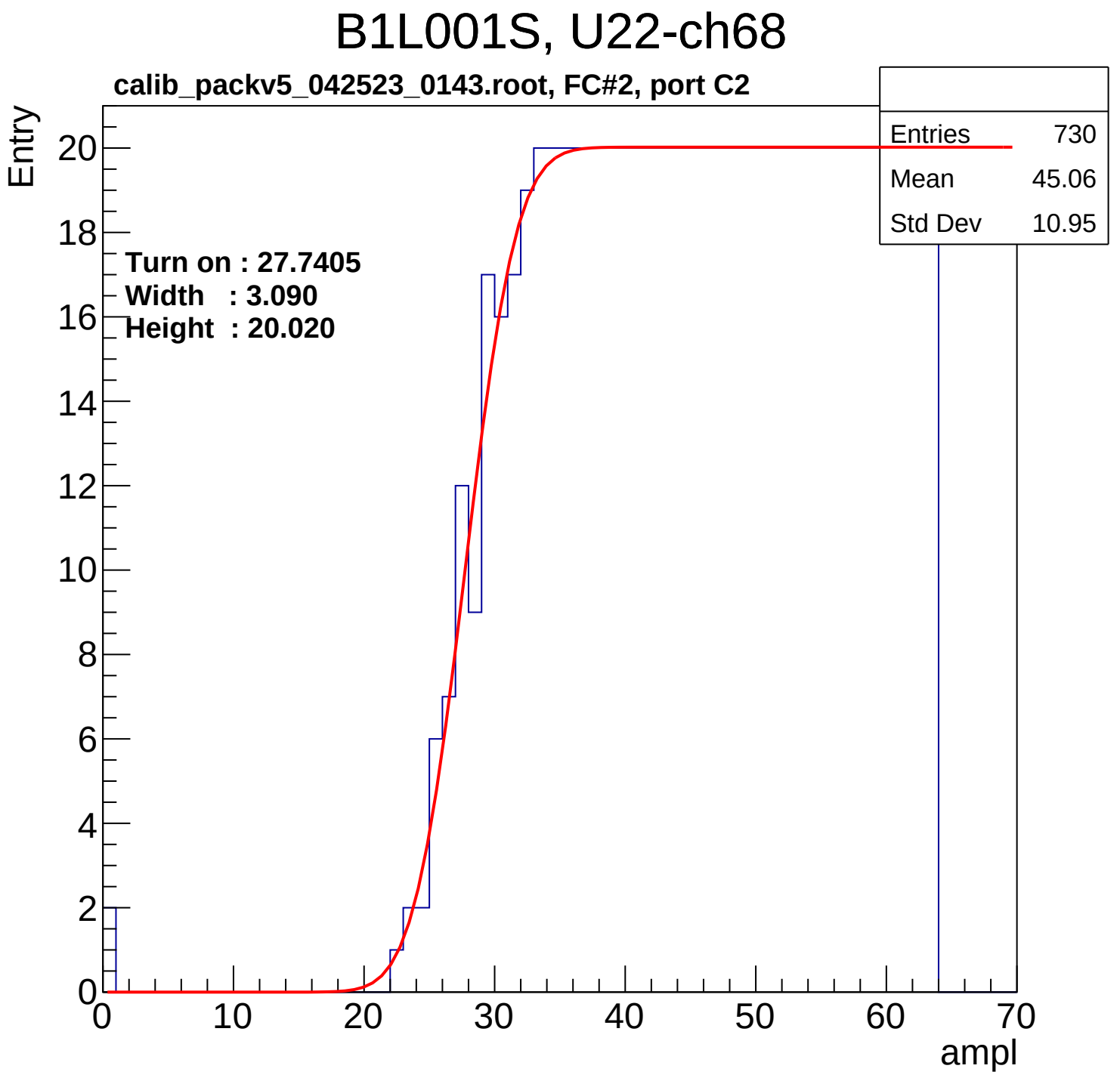
B1L001S, U22-ch68
calib_packv5_042523_0143.root, FC#2, port C2
Entries 730
Mean 45.06
Std Dev 10.95
Turn on : 27.7405
Width : 3.090
Height : 20.020
Entry
ampl
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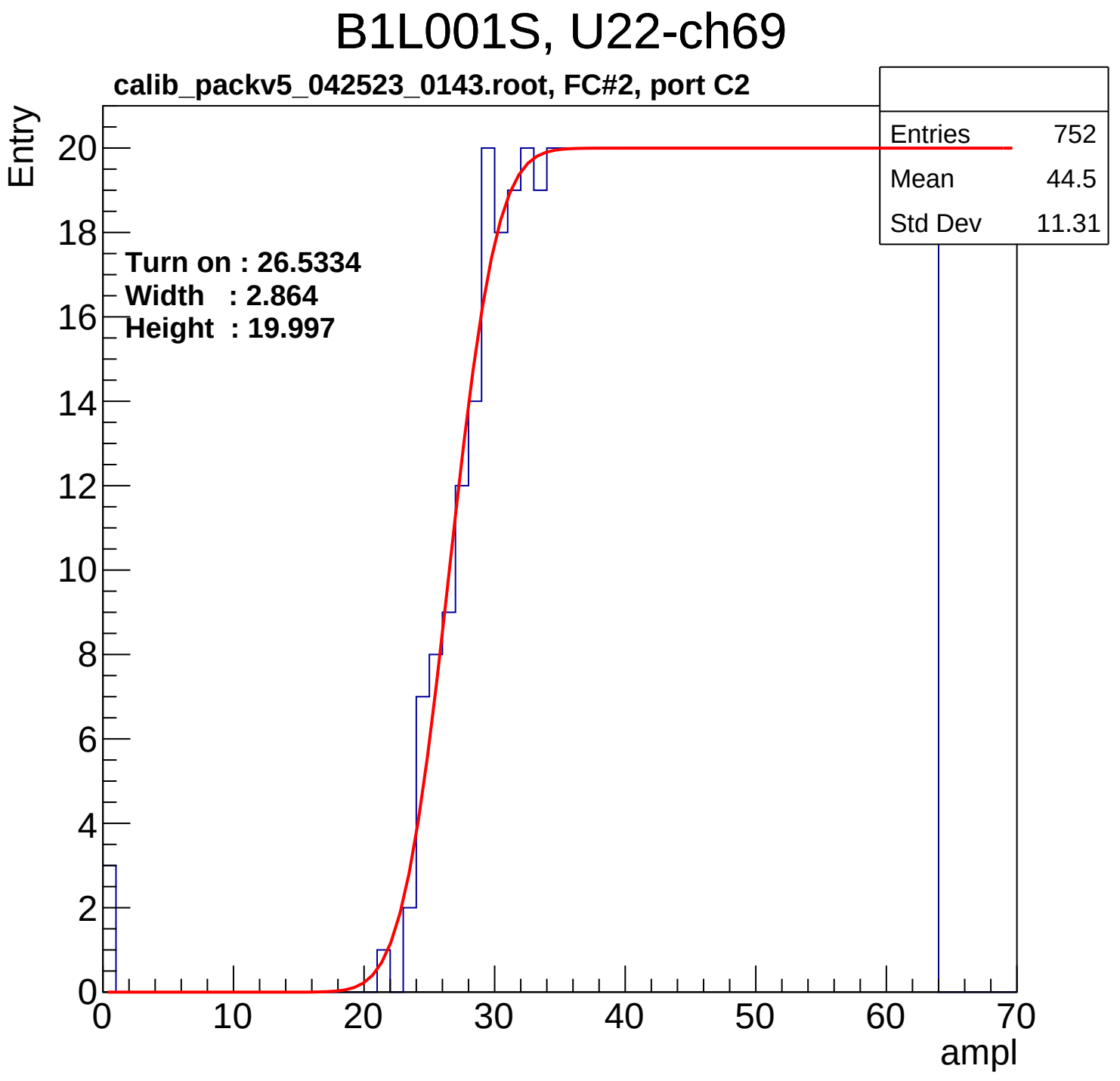
B1L001S, U22-ch69
calib_packv5_042523_0143.root, FC#2, port C2
Entries 752
Mean 44.5
Std Dev 11.31
Turn on : 26.5334
Width : 2.864
Height : 19.997
Entry
ampl
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6
8
10
12
14
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0
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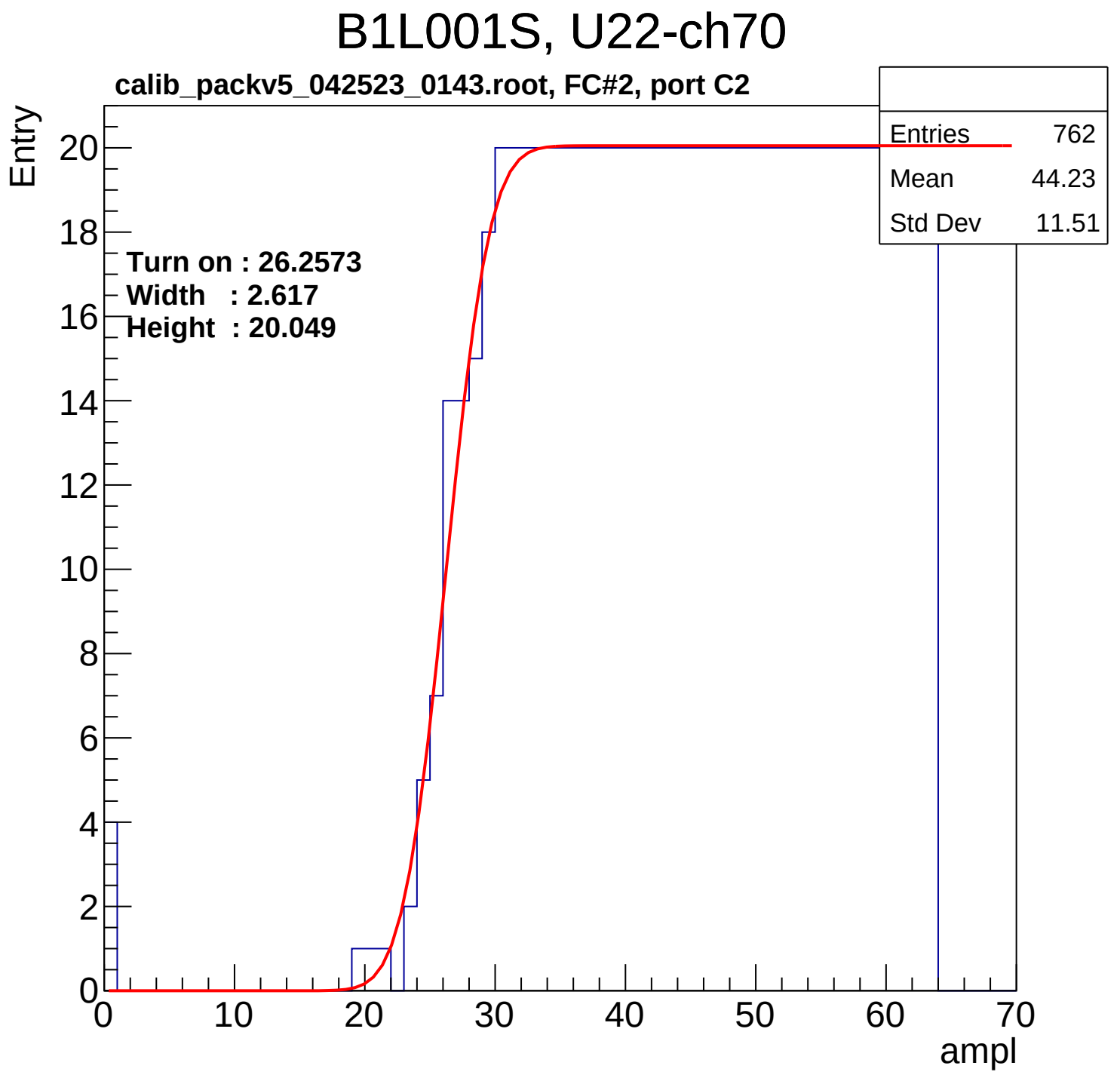
B1L001S, U22-ch70
calib_packv5_042523_0143.root, FC#2, port C2
Entries 762
Mean 44.23
Std Dev 11.51
Turn on : 26.2573
Width : 2.617
Height : 20.049
Entry
ampl
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6
8
10
12
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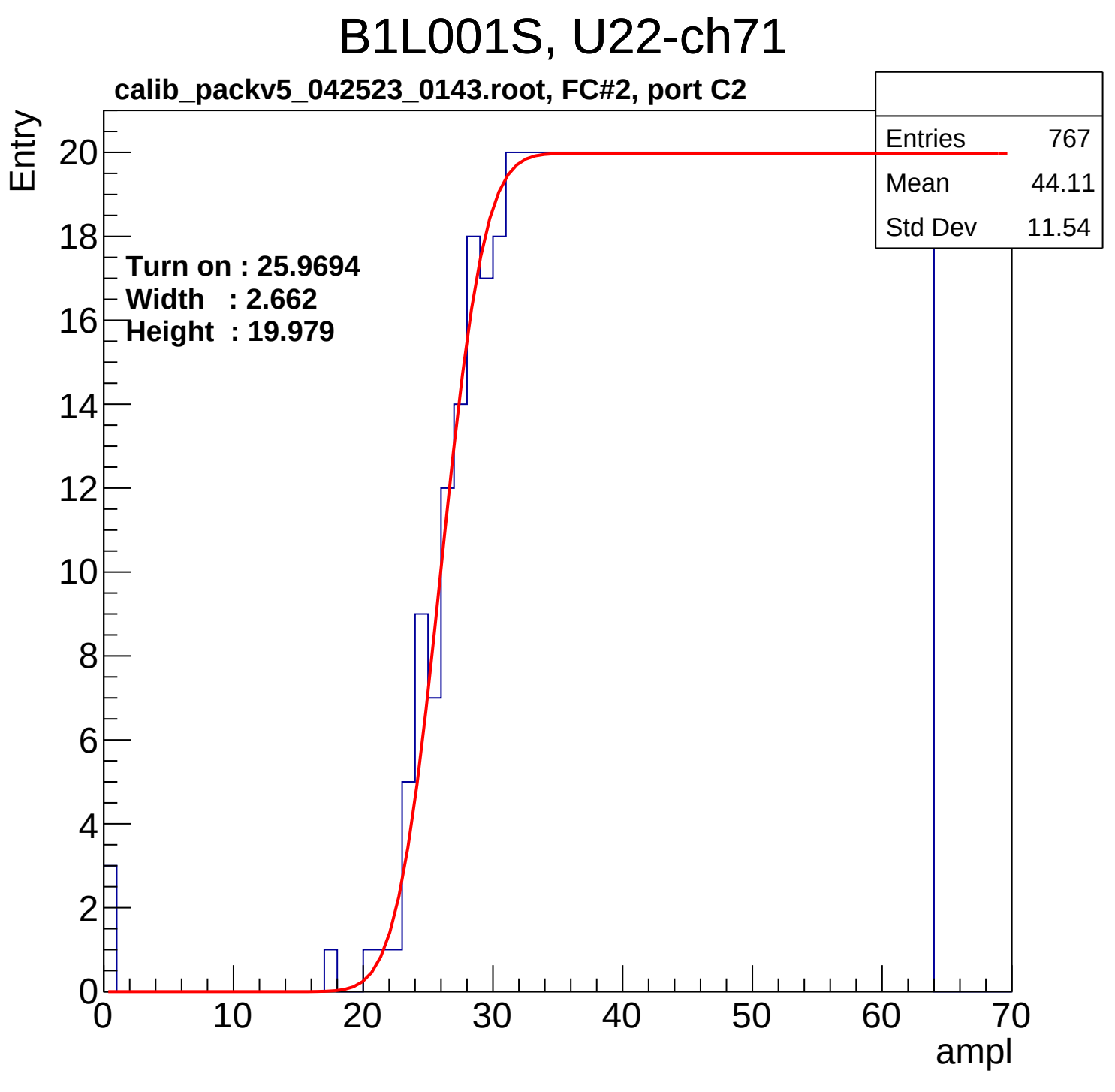
B1L001S, U22-ch71
calib_packv5_042523_0143.root, FC#2, port C2
Entries 767
Mean 44.11
Std Dev 11.54
Turn on : 25.9694
Width : 2.662
Height : 19.979
Entry
ampl
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8
10
12
14
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0
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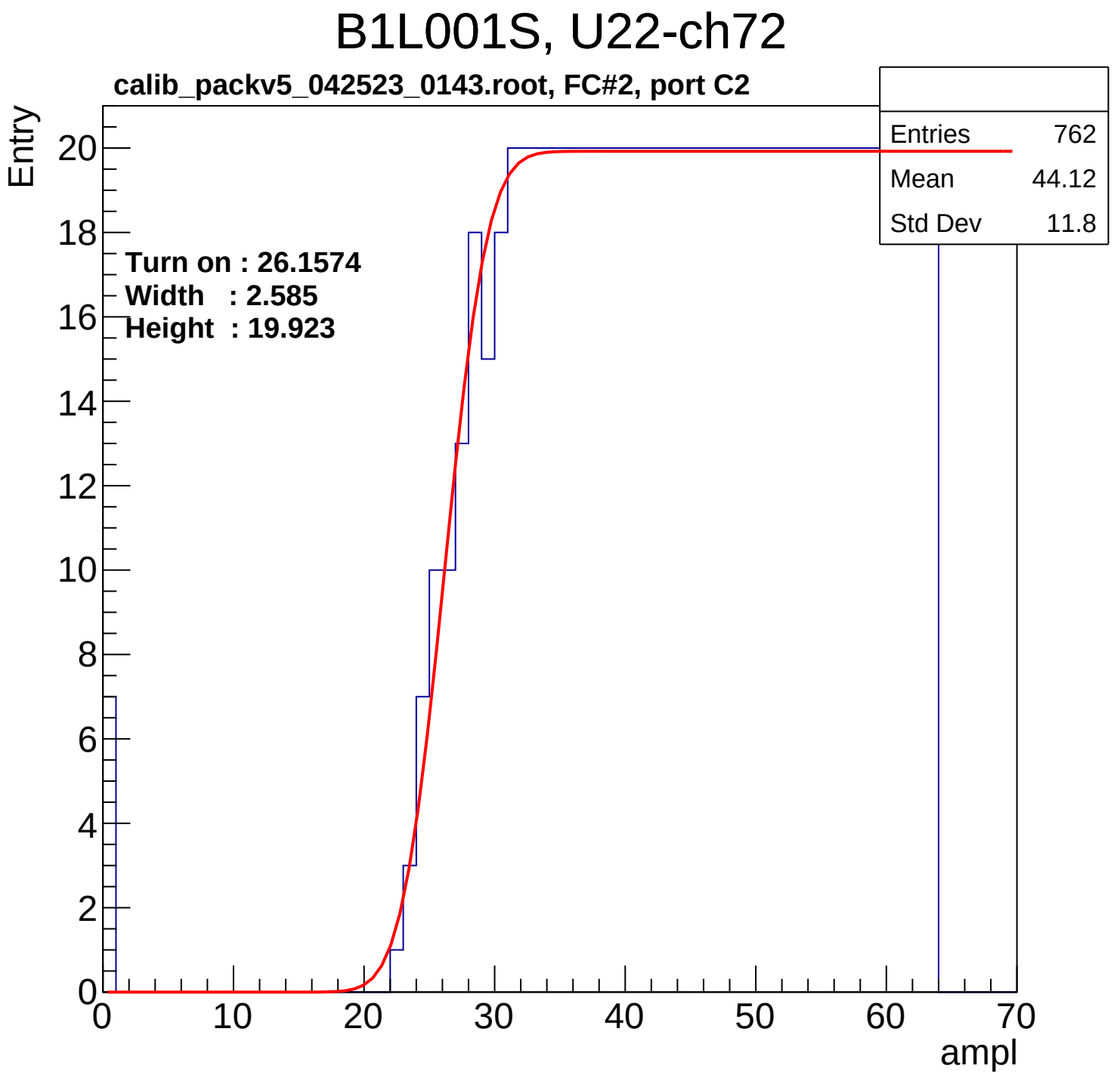
B1L001S, U22-ch72
calib_packv5_042523_0143.root, FC#2, port C2
Entries 762
Mean 44.12
Std Dev 11.8
Turn on : 26.1574
Width : 2.585
Height : 19.923
Entry
ampl
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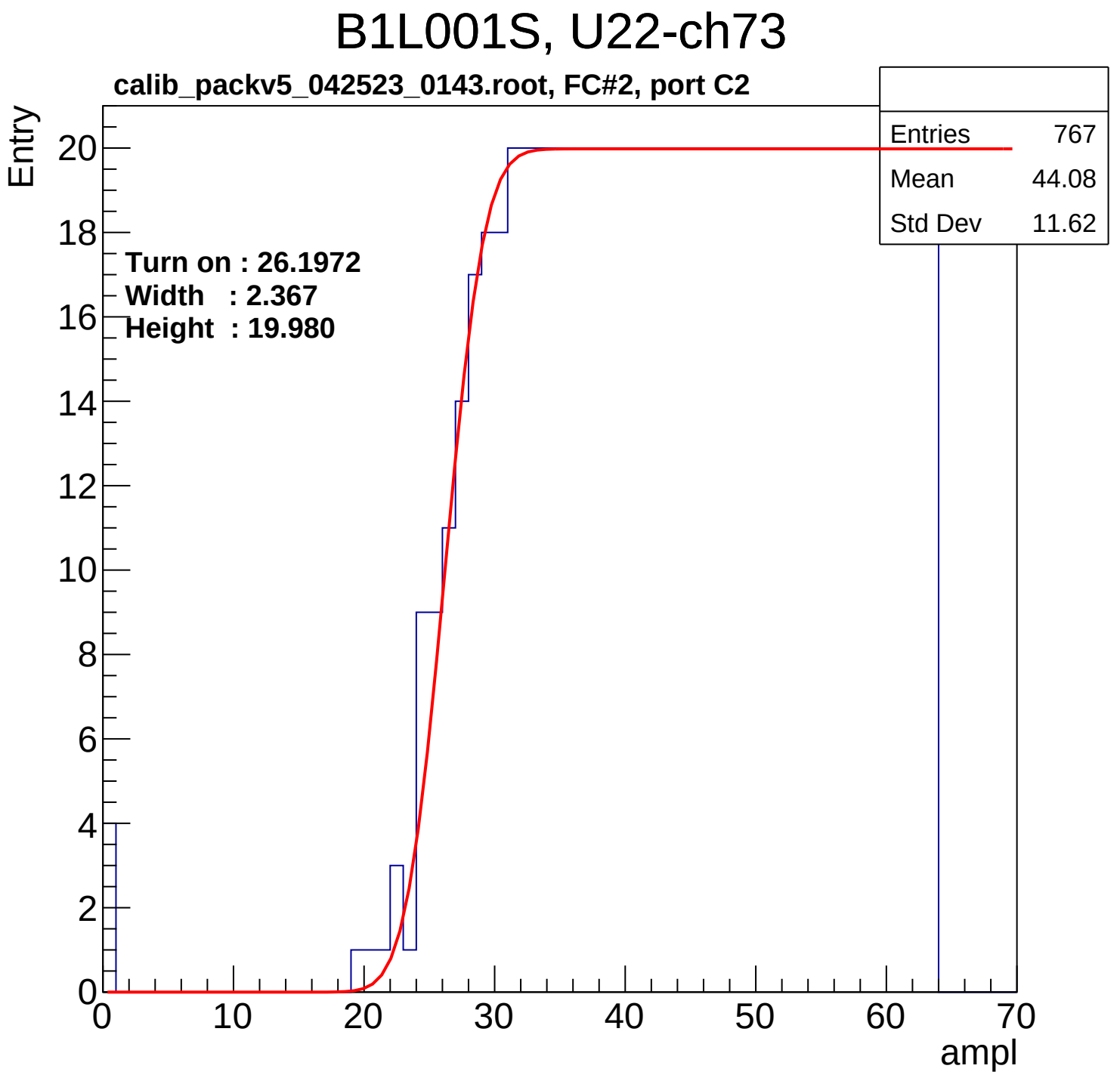
B1L001S, U22-ch73
calib_packv5_042523_0143.root, FC#2, port C2
Entries 767
Mean 44.08
Std Dev 11.62
Turn on : 26.1972
Width : 2.367
Height : 19.980
Entry
ampl
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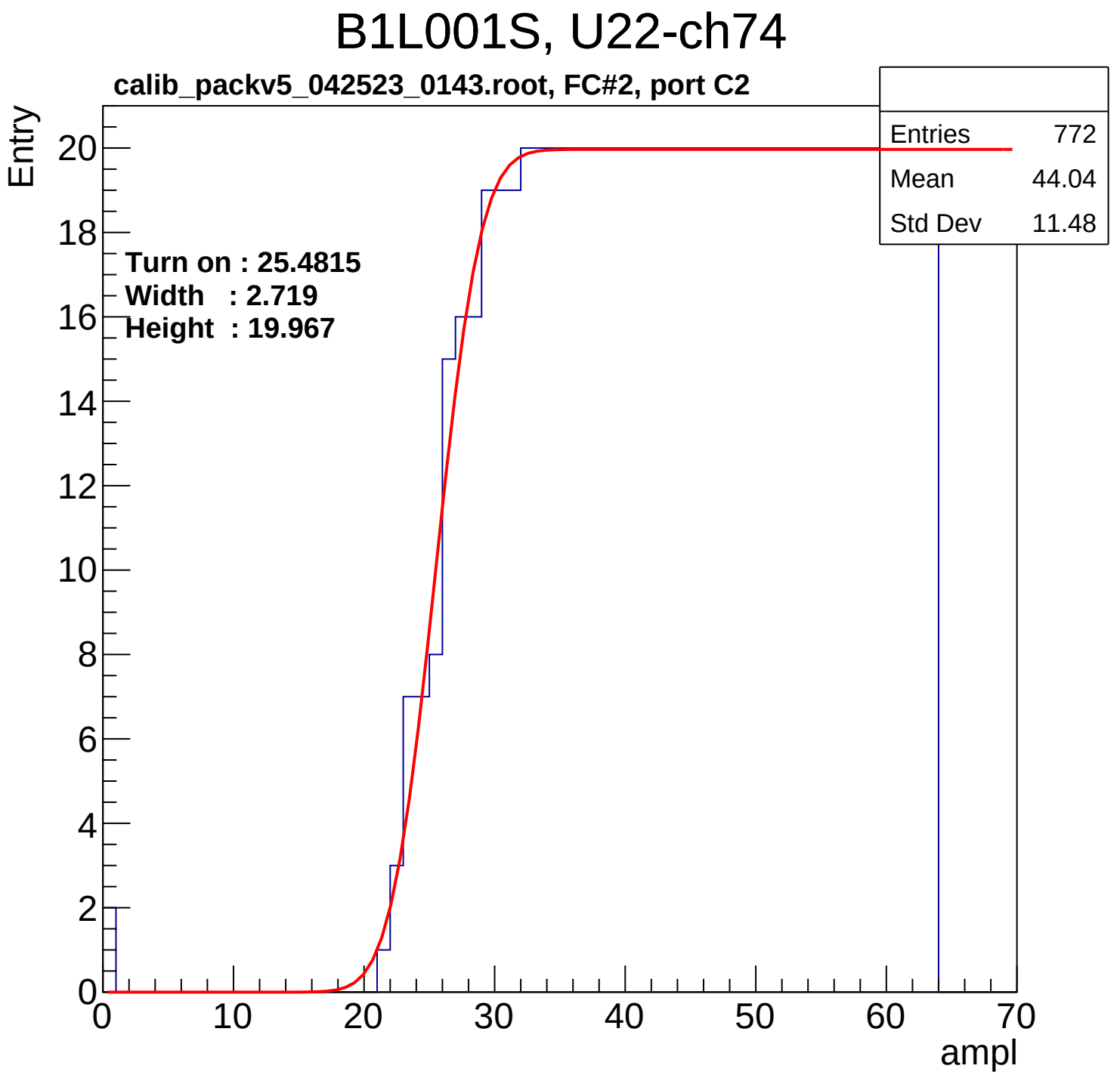
B1L001S, U22-ch74
calib_packv5_042523_0143.root, FC#2, port C2
Entries 772
Mean 44.04
Std Dev 11.48
Turn on : 25.4815
Width : 2.719
Height : 19.967
Entry
ampl
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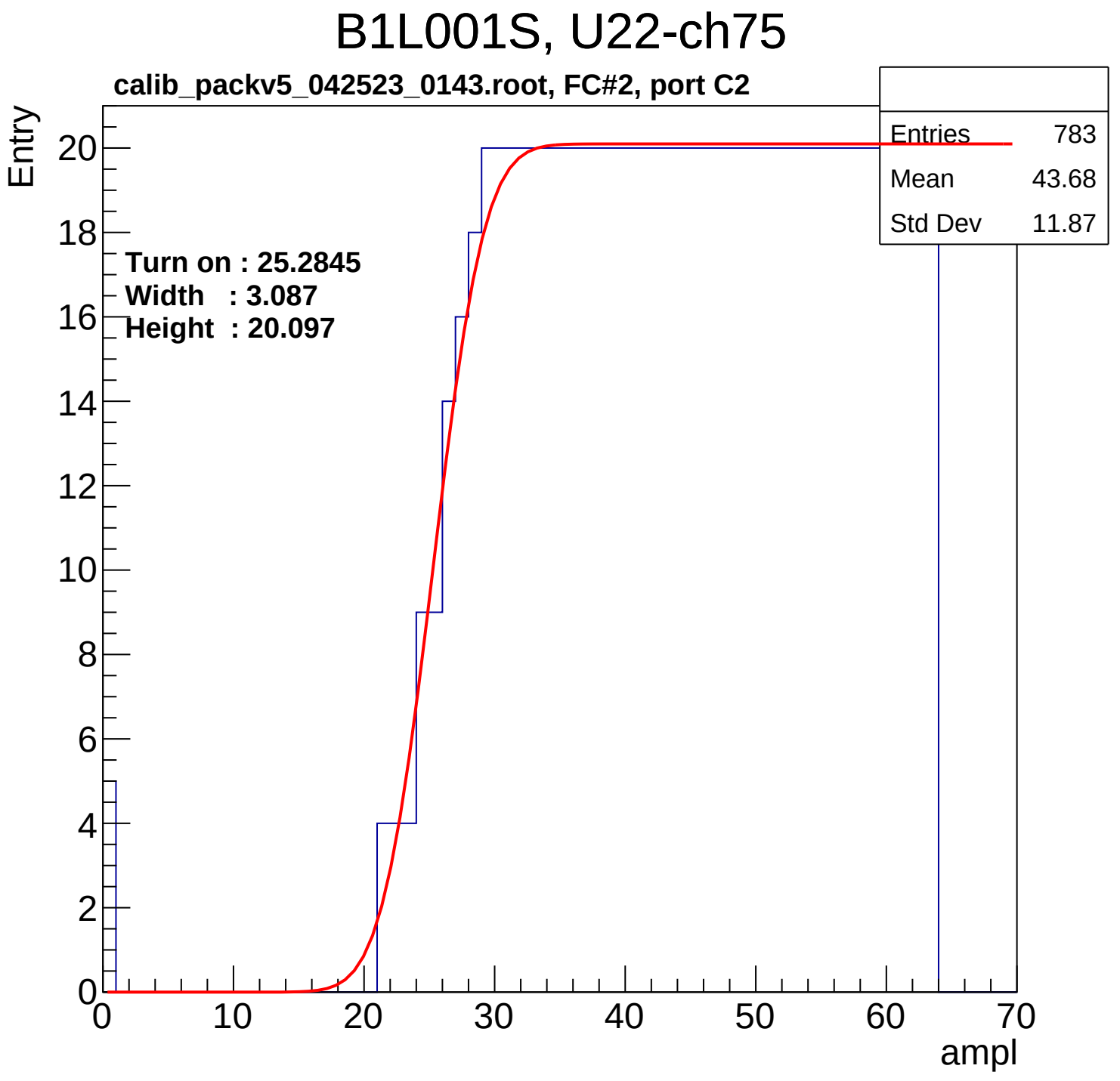
B1L001S, U22-ch75
calib_packv5_042523_0143.root, FC#2, port C2
Entries 783
Mean 43.68
Std Dev 11.87
Turn on : 25.2845
Width : 3.087
Height : 20.097
Entry
ampl
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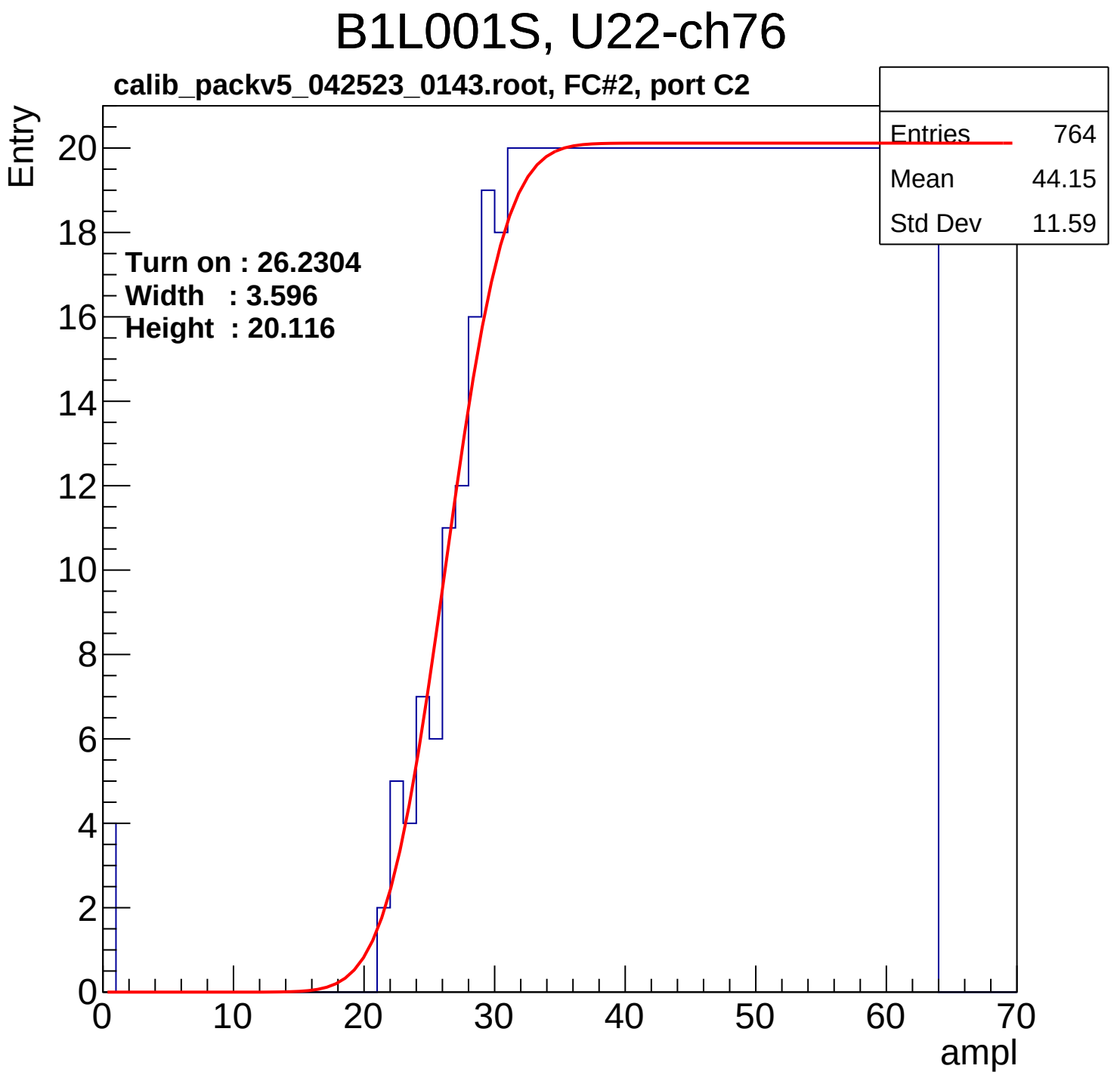
B1L001S, U22-ch76
calib_packv5_042523_0143.root, FC#2, port C2
Entries 764
Mean 44.15
Std Dev 11.59
Turn on : 26.2304
Width : 3.596
Height : 20.116
Entry
ampl
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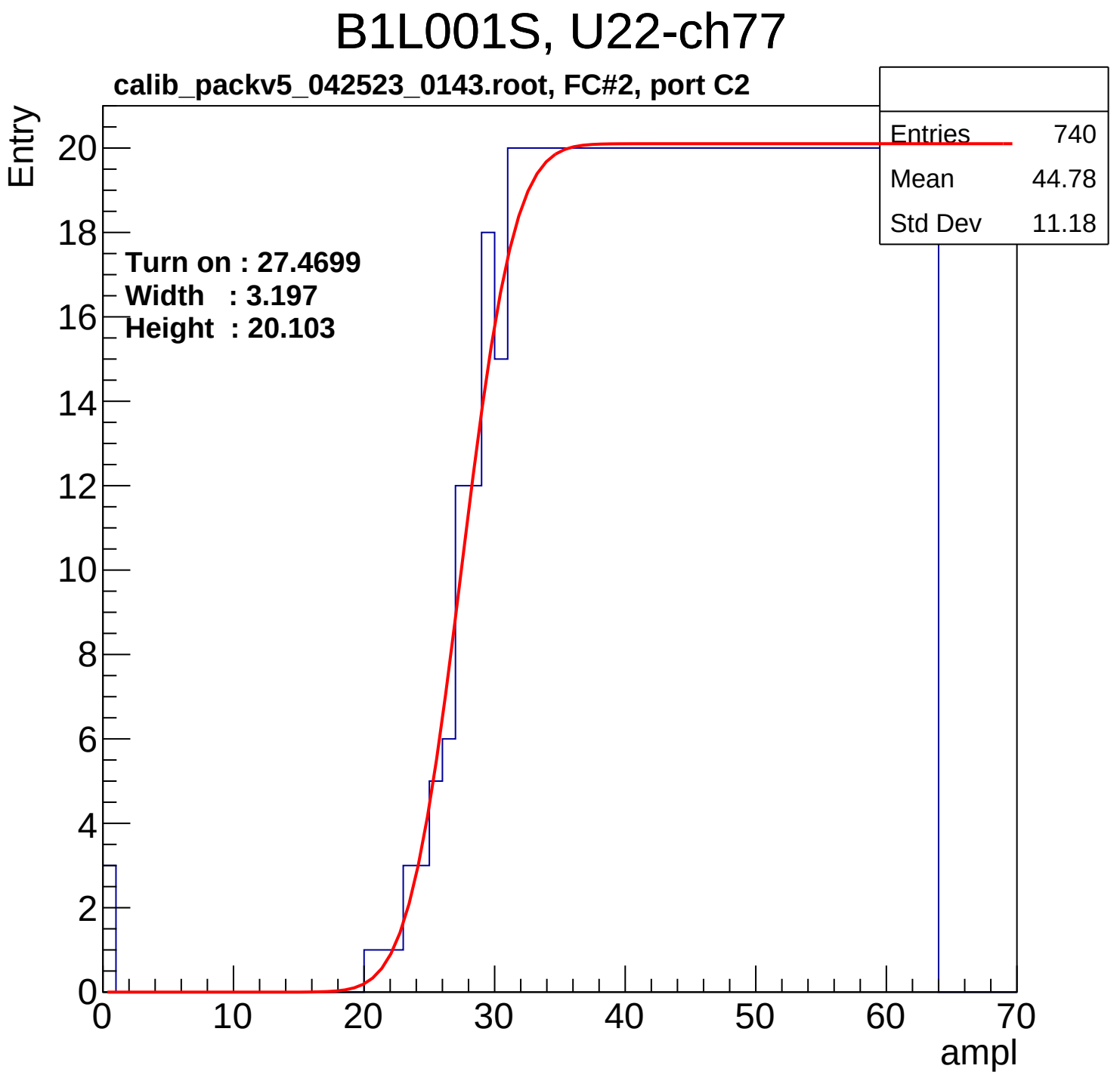
B1L001S, U22-ch77
calib_packv5_042523_0143.root, FC#2, port C2
Entries 740
Mean 44.78
Std Dev 11.18
Turn on : 27.4699
Width : 3.197
Height : 20.103
Entry
ampl
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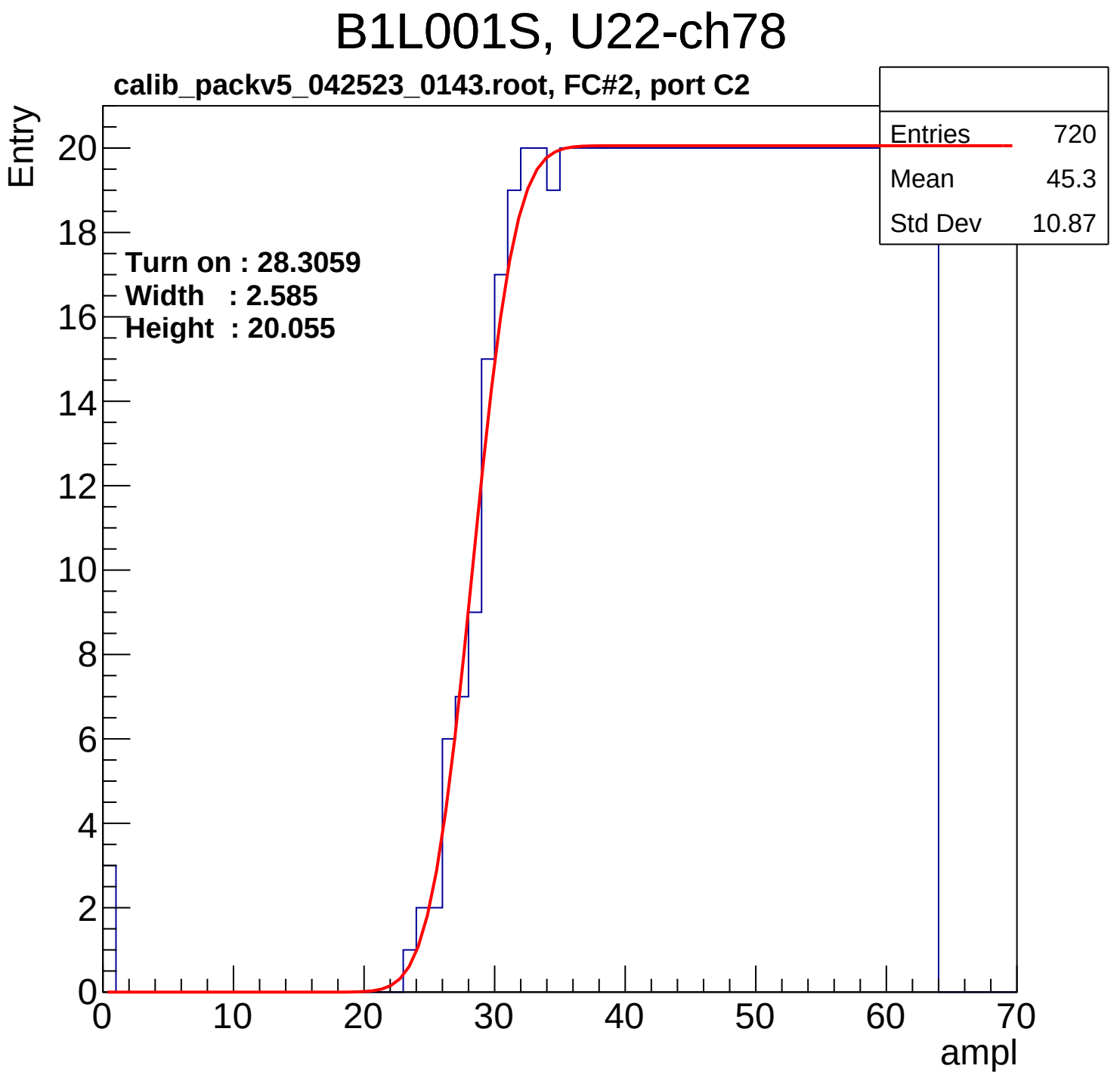
B1L001S, U22-ch78
calib_packv5_042523_0143.root, FC#2, port C2
Entries 720
Mean 45.3
Std Dev 10.87
Turn on : 28.3059
Width : 2.585
Height : 20.055
Entry
ampl
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6
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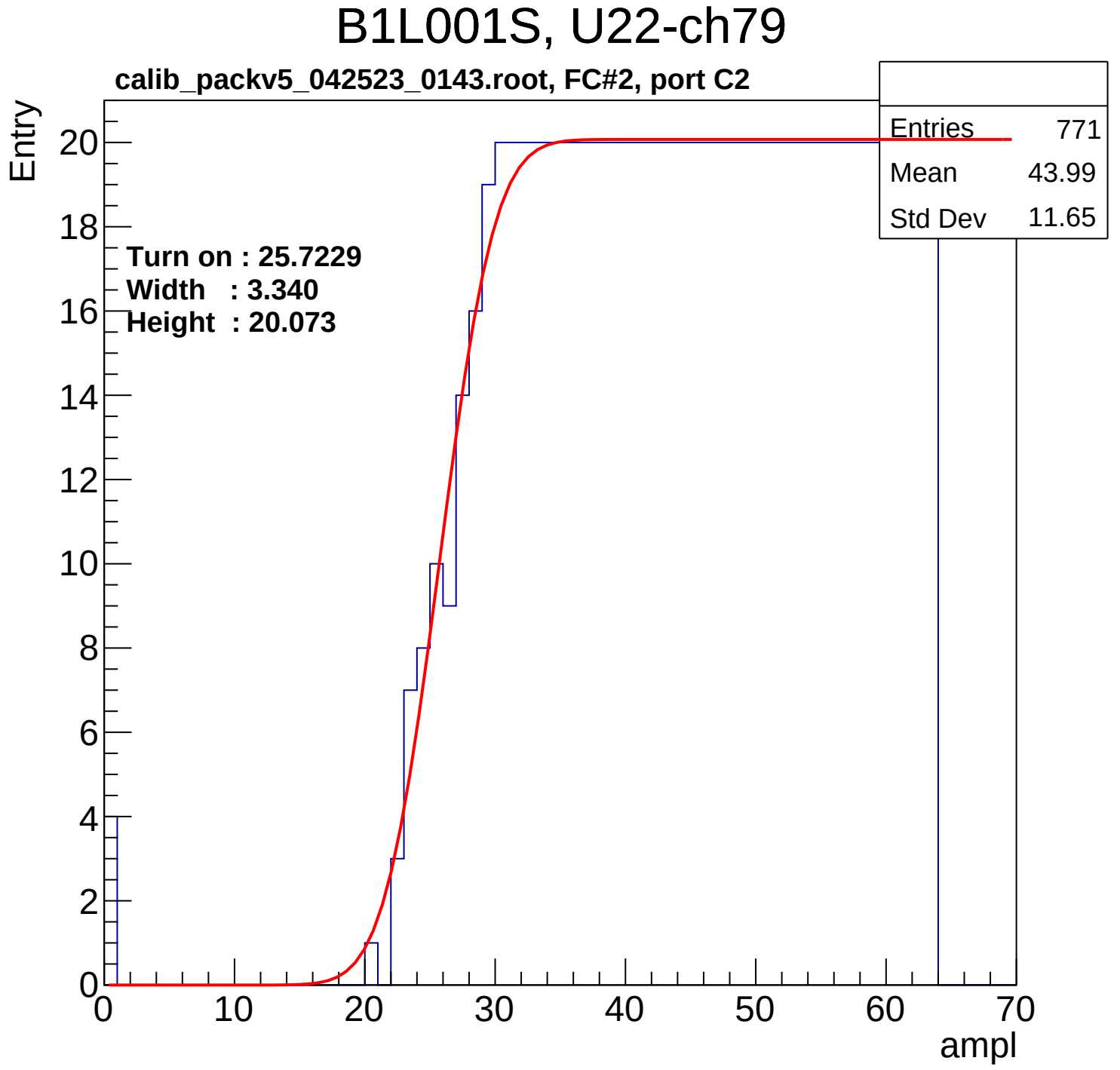
B1L001S, U22-ch79
calib_packv5_042523_0143.root, FC#2, port C2
Entries 771
Mean 43.99
Std Dev 11.65
Turn on : 25.7229
Width : 3.340
Height : 20.073
Entry
ampl
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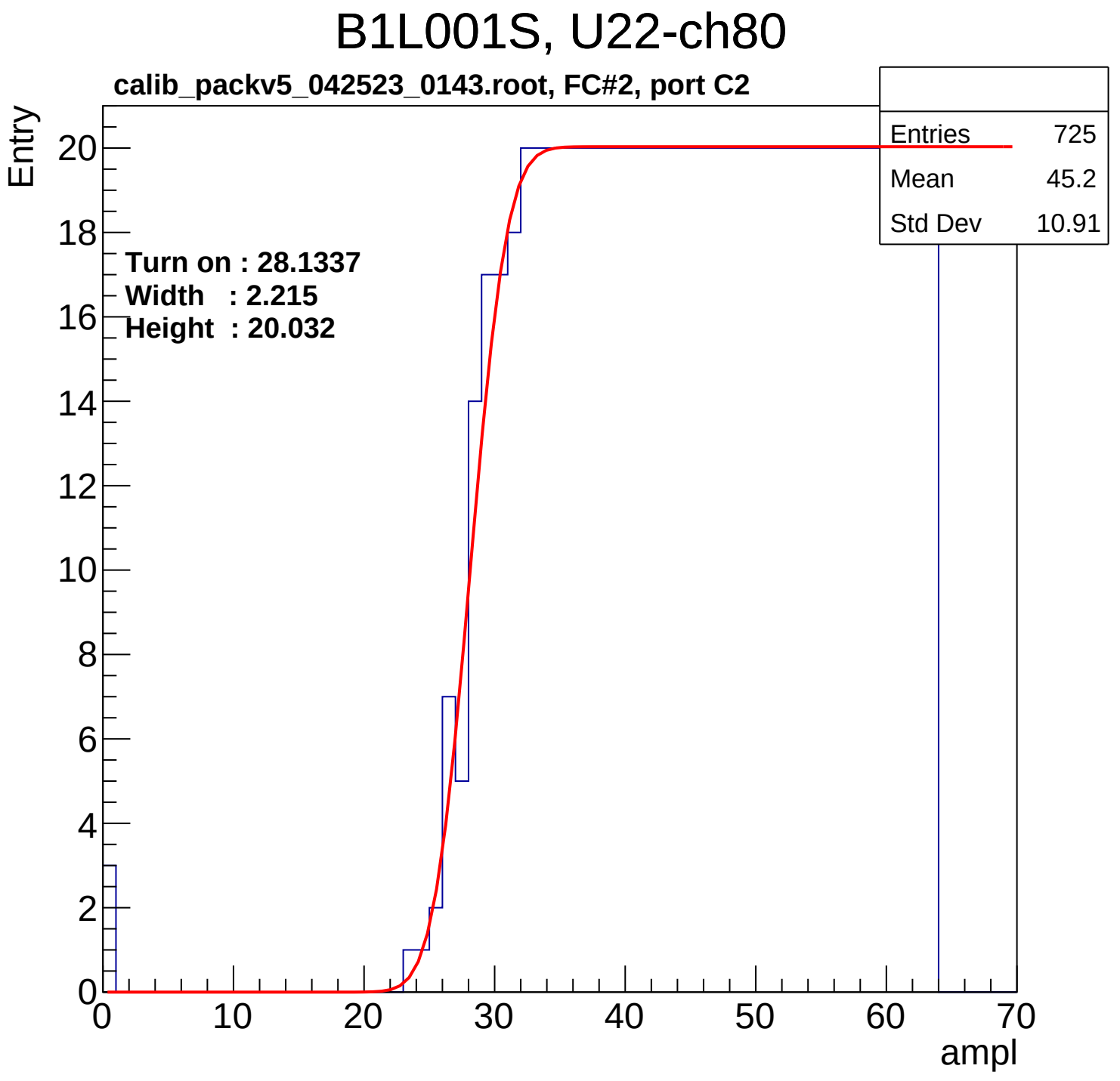
B1L001S, U22-ch80
calib_packv5_042523_0143.root, FC#2, port C2
Entries 725
Mean 45.2
Std Dev 10.91
Turn on : 28.1337
Width : 2.215
Height : 20.032
Entry
ampl
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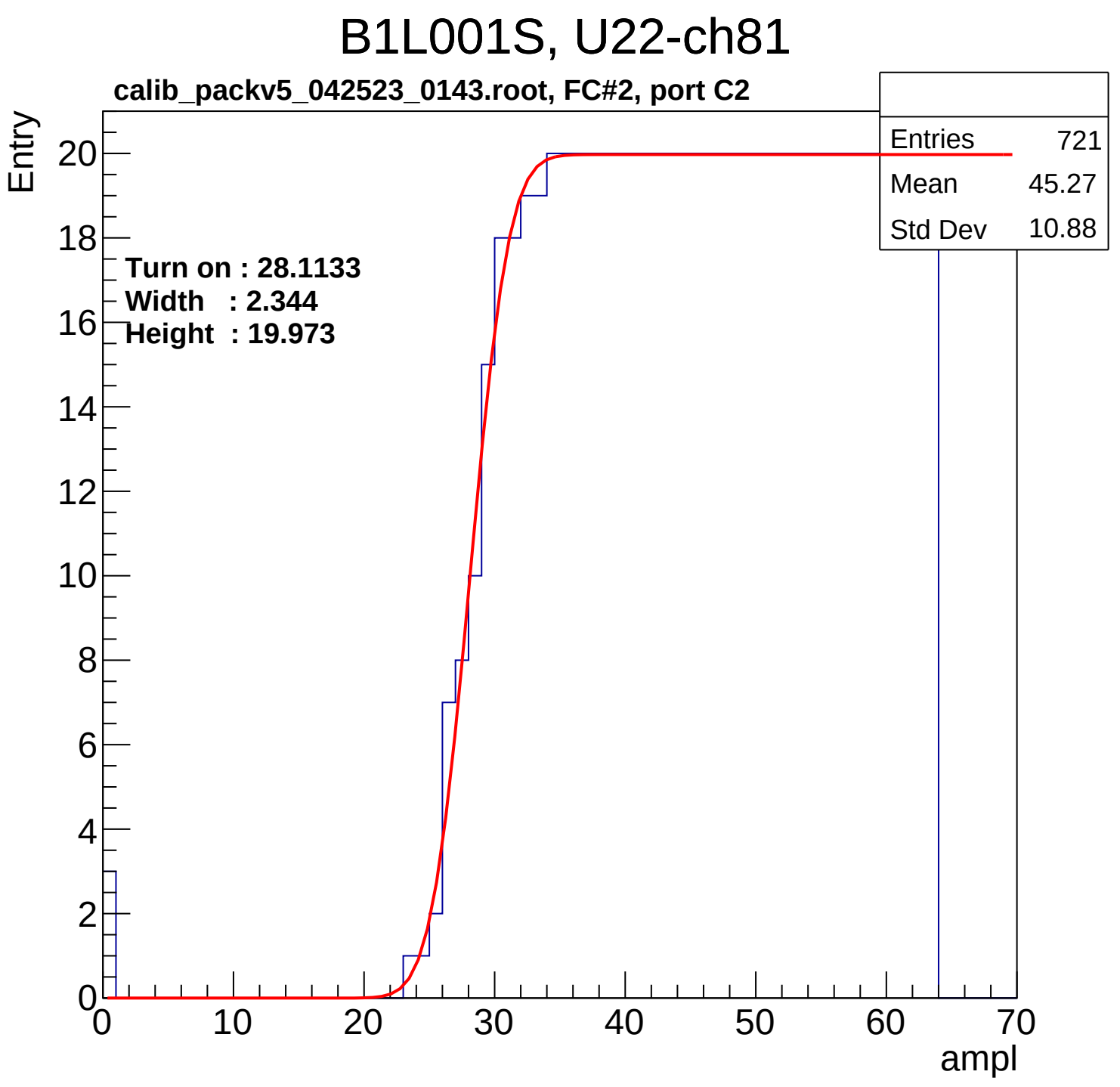
B1L001S, U22-ch81
calib_packv5_042523_0143.root, FC#2, port C2
Entries 721
Mean 45.27
Std Dev 10.88
Turn on : 28.1133
Width : 2.344
Height : 19.973
Entry
ampl
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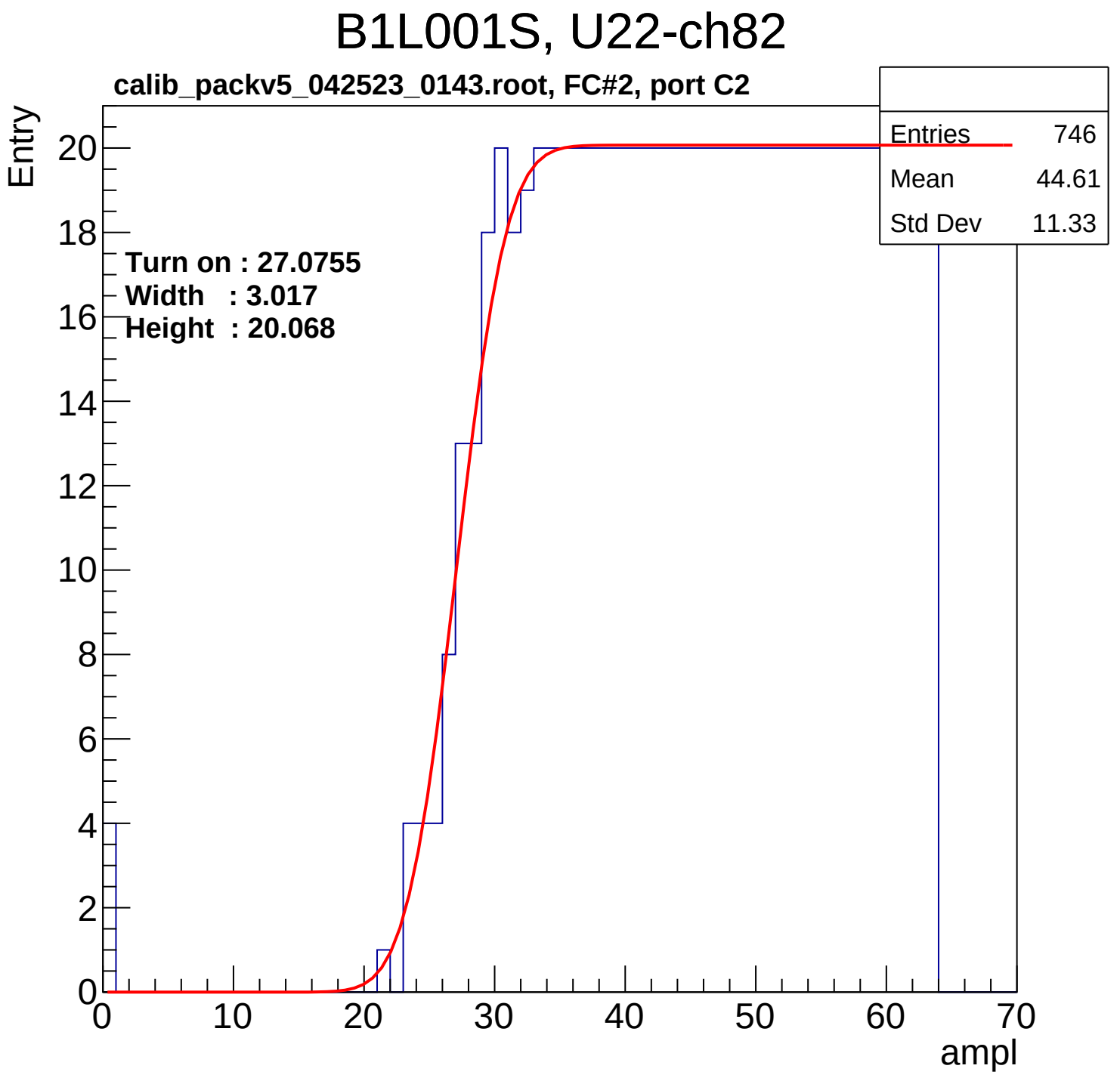
B1L001S, U22-ch82
calib_packv5_042523_0143.root, FC#2, port C2
Entries 746
Mean 44.61
Std Dev 11.33
Turn on : 27.0755
Width : 3.017
Height : 20.068
Entry
ampl
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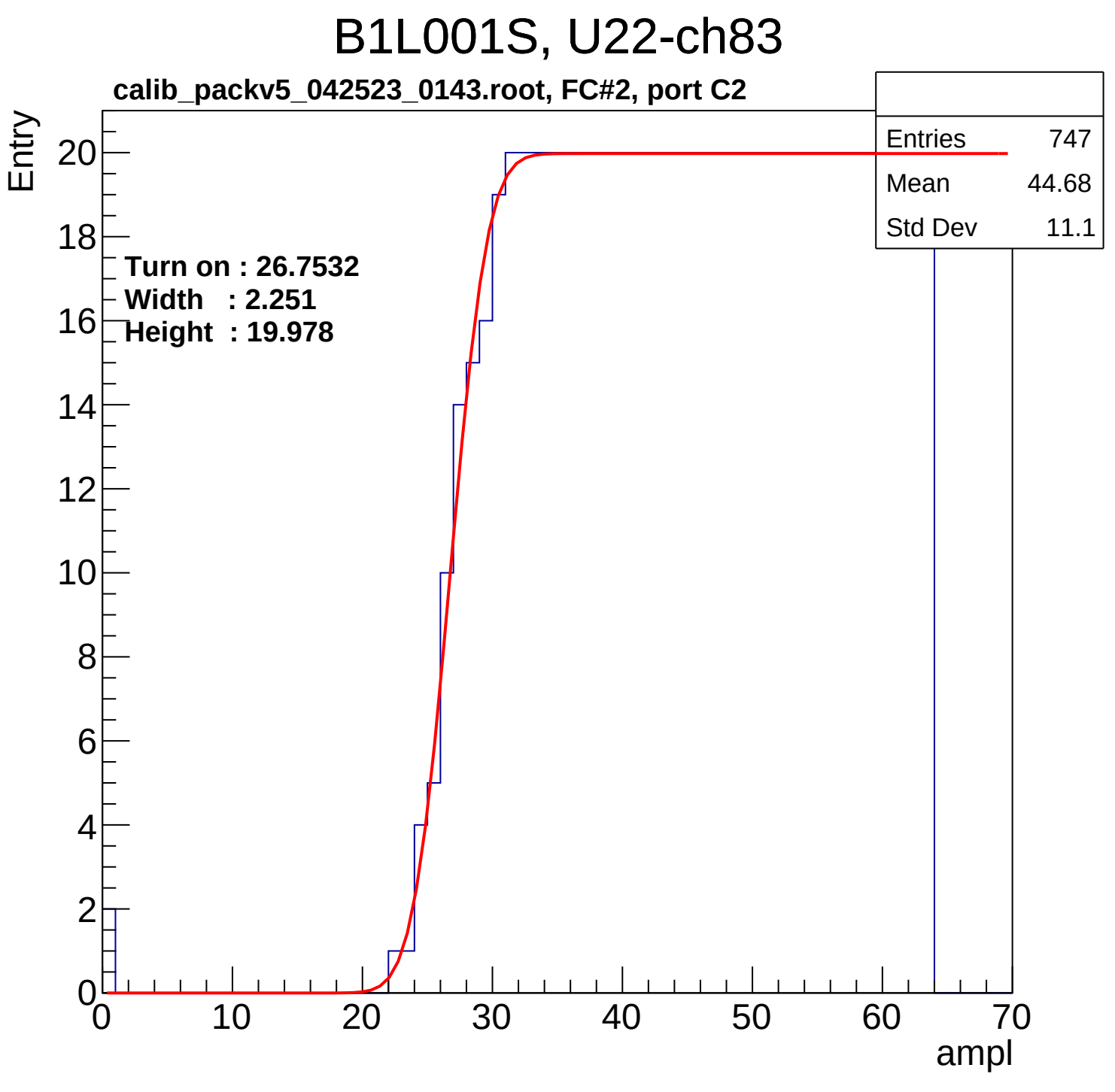
B1L001S, U22-ch83
calib_packv5_042523_0143.root, FC#2, port C2
Entries 747
Mean 44.68
Std Dev 11.1
Turn on : 26.7532
Width : 2.251
Height : 19.978
Entry
ampl
0
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6
8
10
12
14
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18
20
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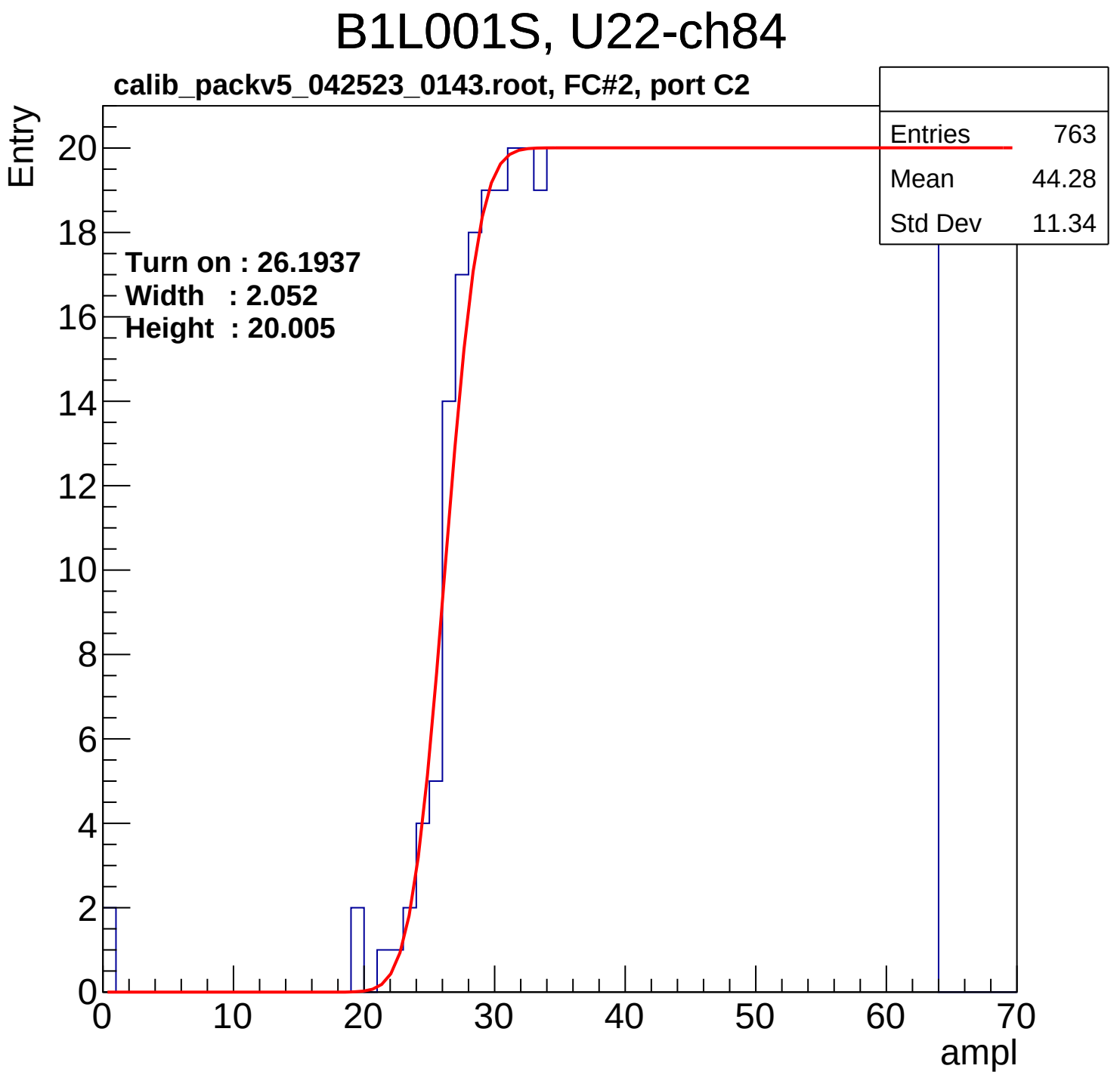
B1L001S, U22-ch84
calib_packv5_042523_0143.root, FC#2, port C2
Entries 763
Mean 44.28
Std Dev 11.34
Turn on : 26.1937
Width : 2.052
Height : 20.005
Entry
ampl
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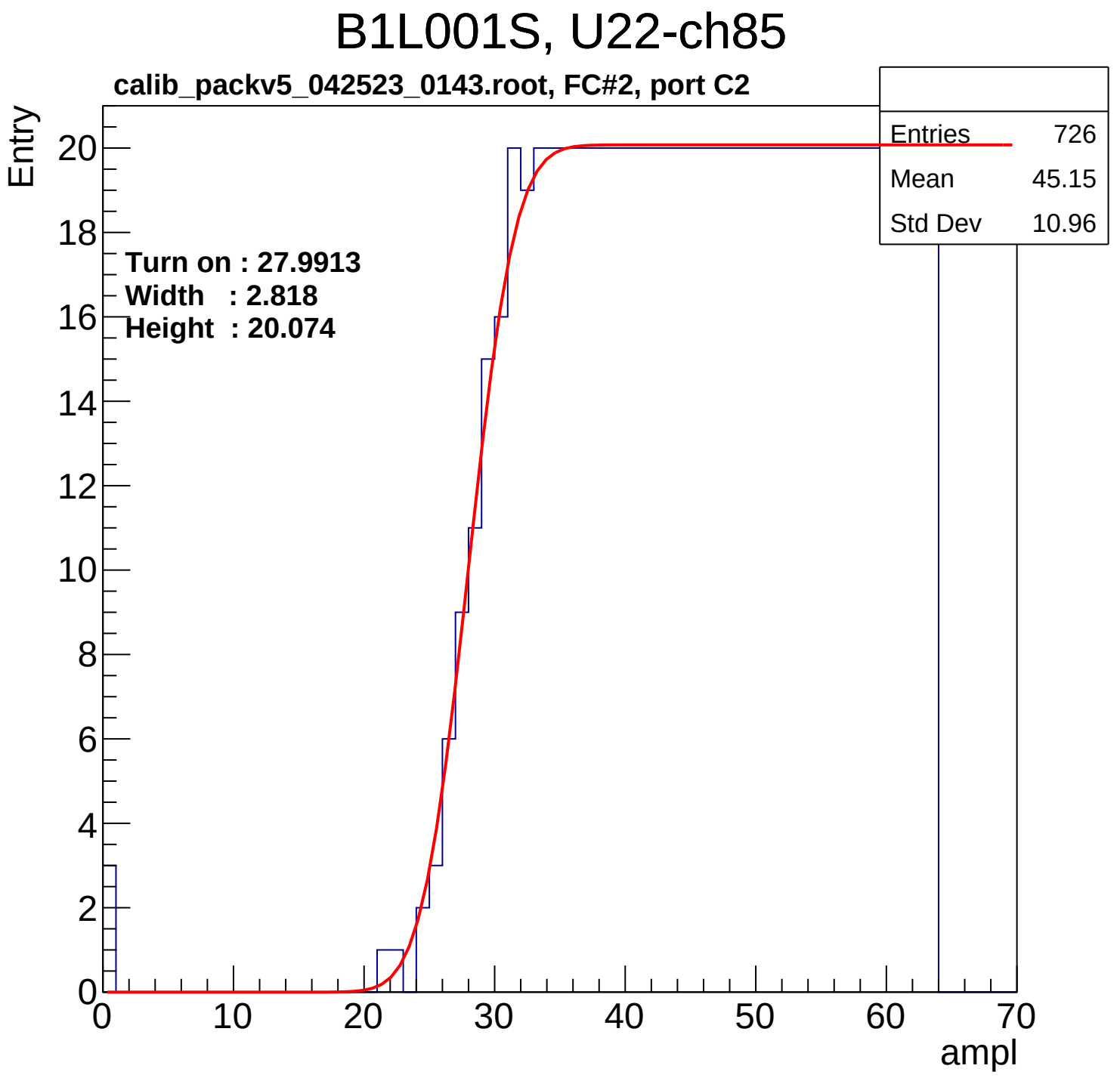
B1L001S, U22-ch85
calib_packv5_042523_0143.root, FC#2, port C2
Entries 726
Mean 45.15
Std Dev 10.96
Turn on : 27.9913
Width : 2.818
Height : 20.074
Entry
ampl
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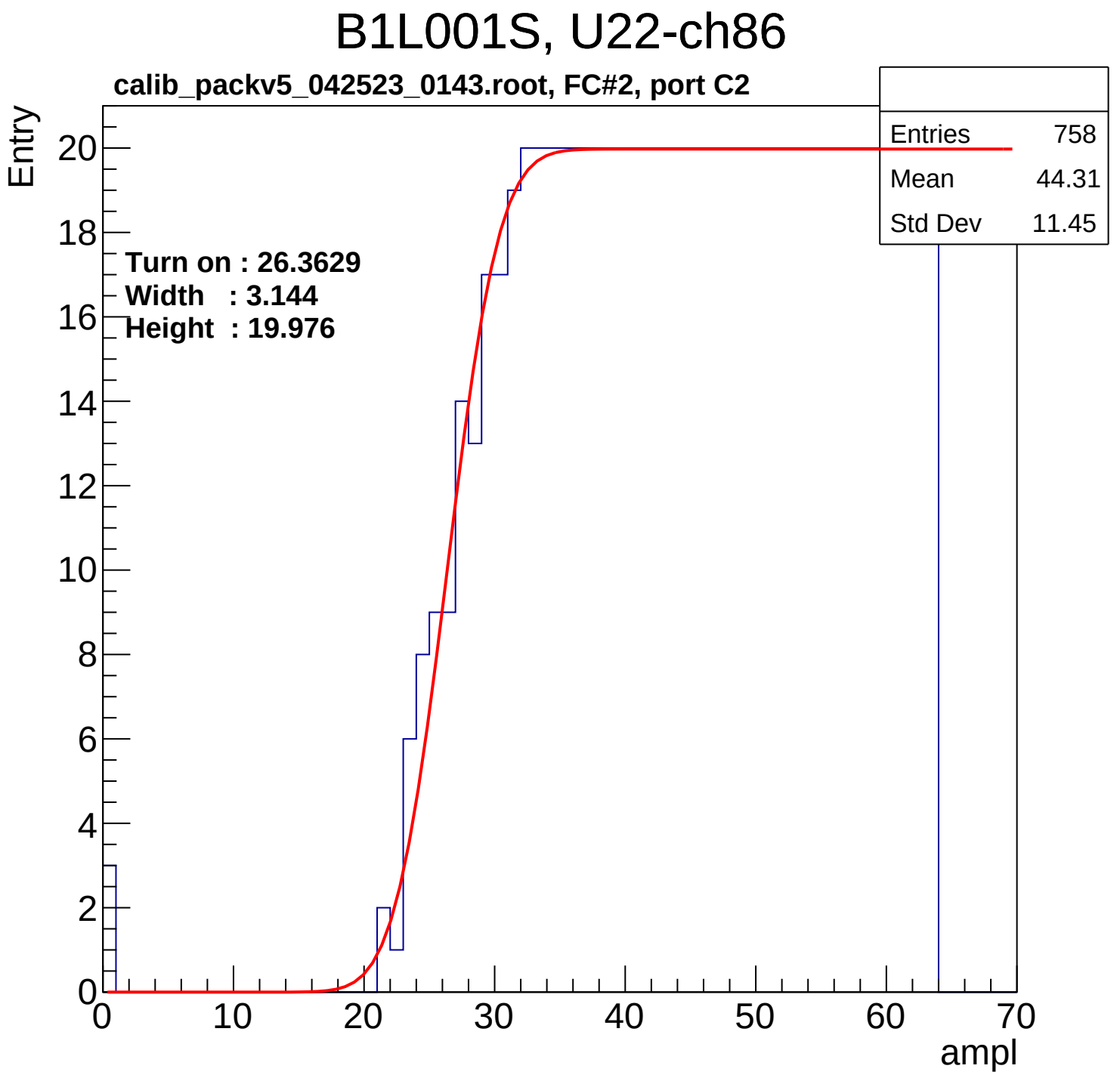
B1L001S, U22-ch86
calib_packv5_042523_0143.root, FC#2, port C2
Entries 758
Mean 44.31
Std Dev 11.45
Turn on : 26.3629
Width : 3.144
Height : 19.976
Entry
ampl
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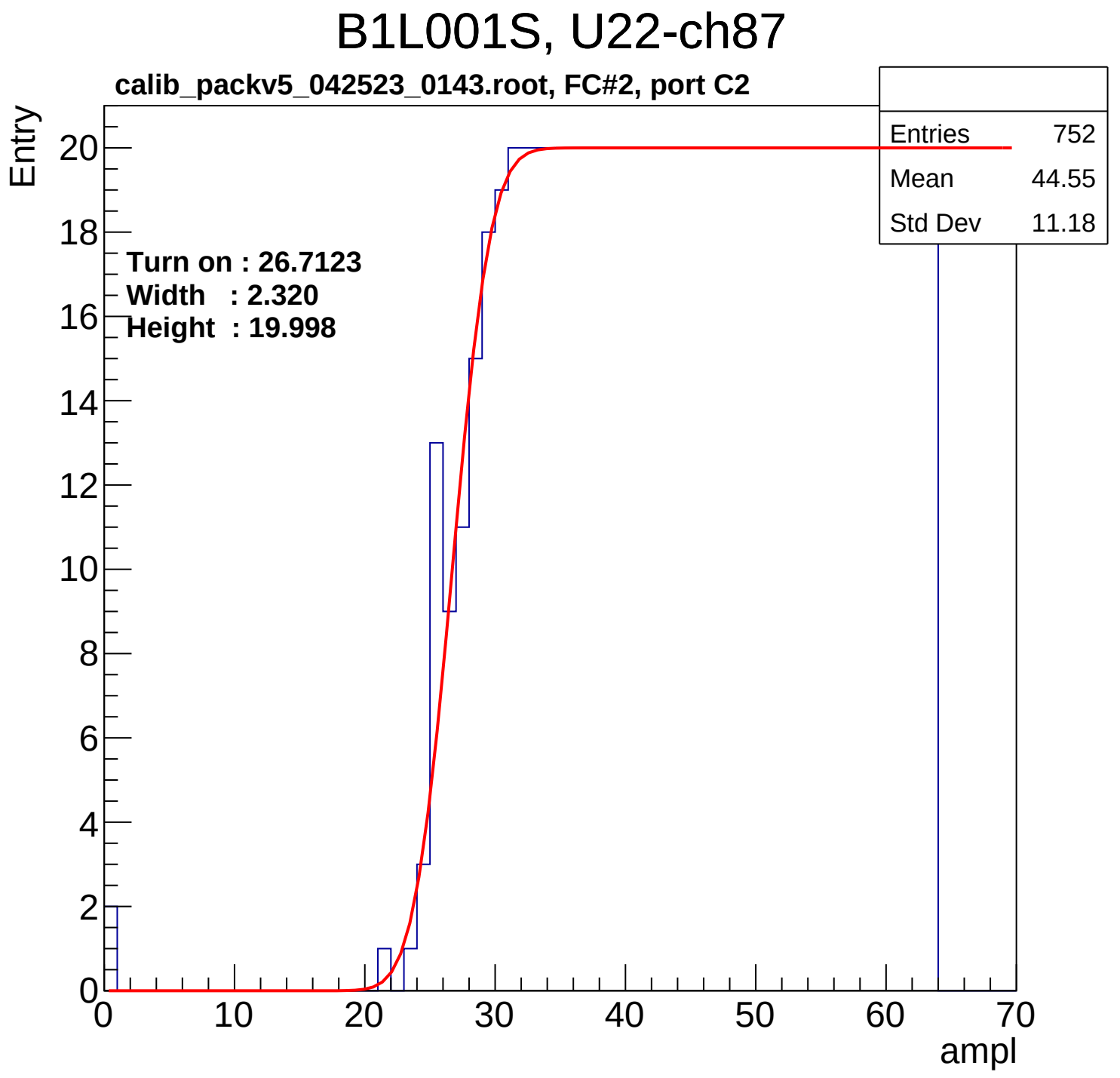
B1L001S, U22-ch87
calib_packv5_042523_0143.root, FC#2, port C2
Entries 752
Mean 44.55
Std Dev 11.18
Turn on : 26.7123
Width : 2.320
Height : 19.998
Entry
ampl
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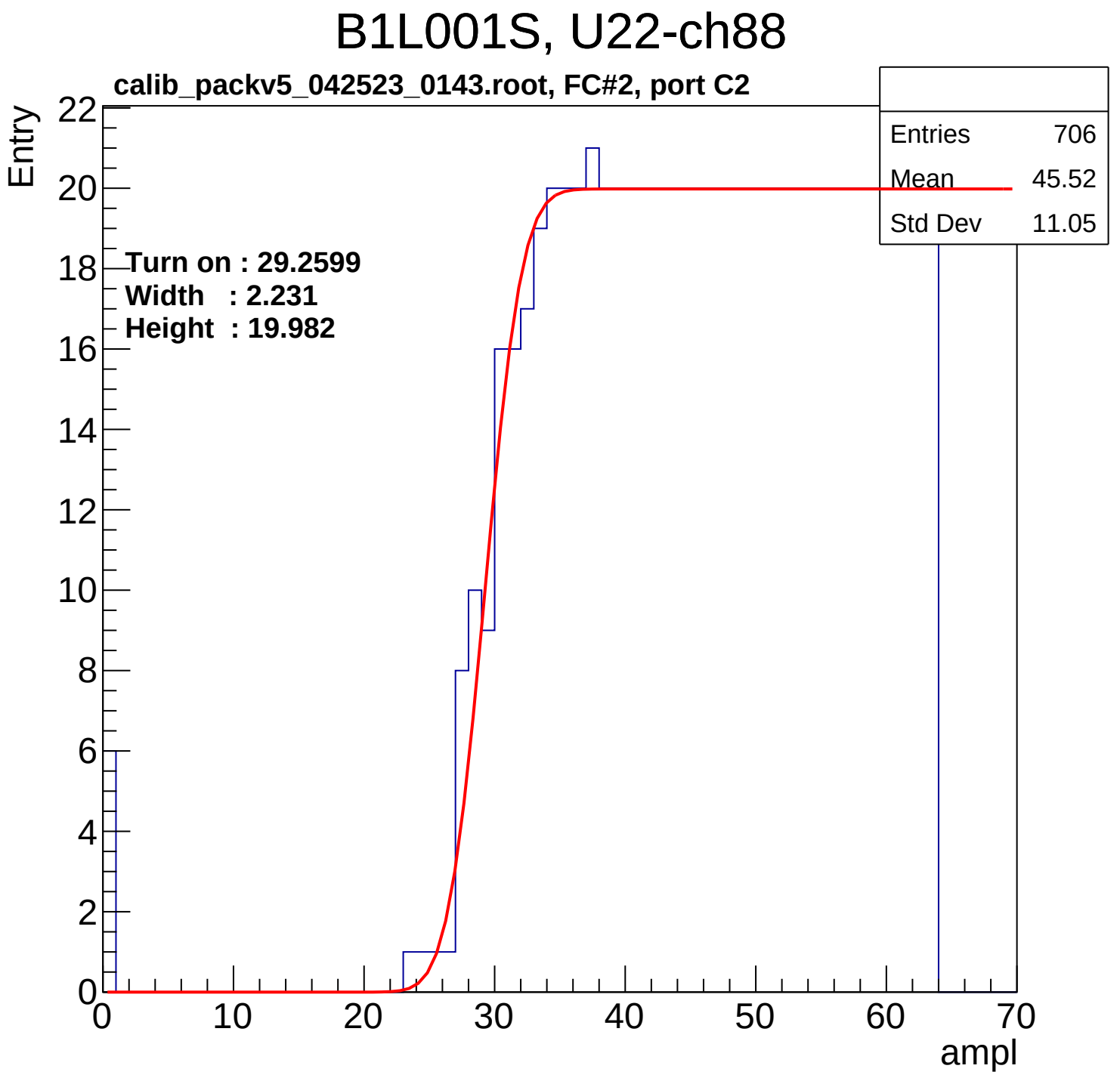
B1L001S, U22-ch88
calib_packv5_042523_0143.root, FC#2, port C2
Entries 706
Mean 45.52
Std Dev 11.05
Turn on : 29.2599
Width : 2.231
Height : 19.982
Entry
ampl
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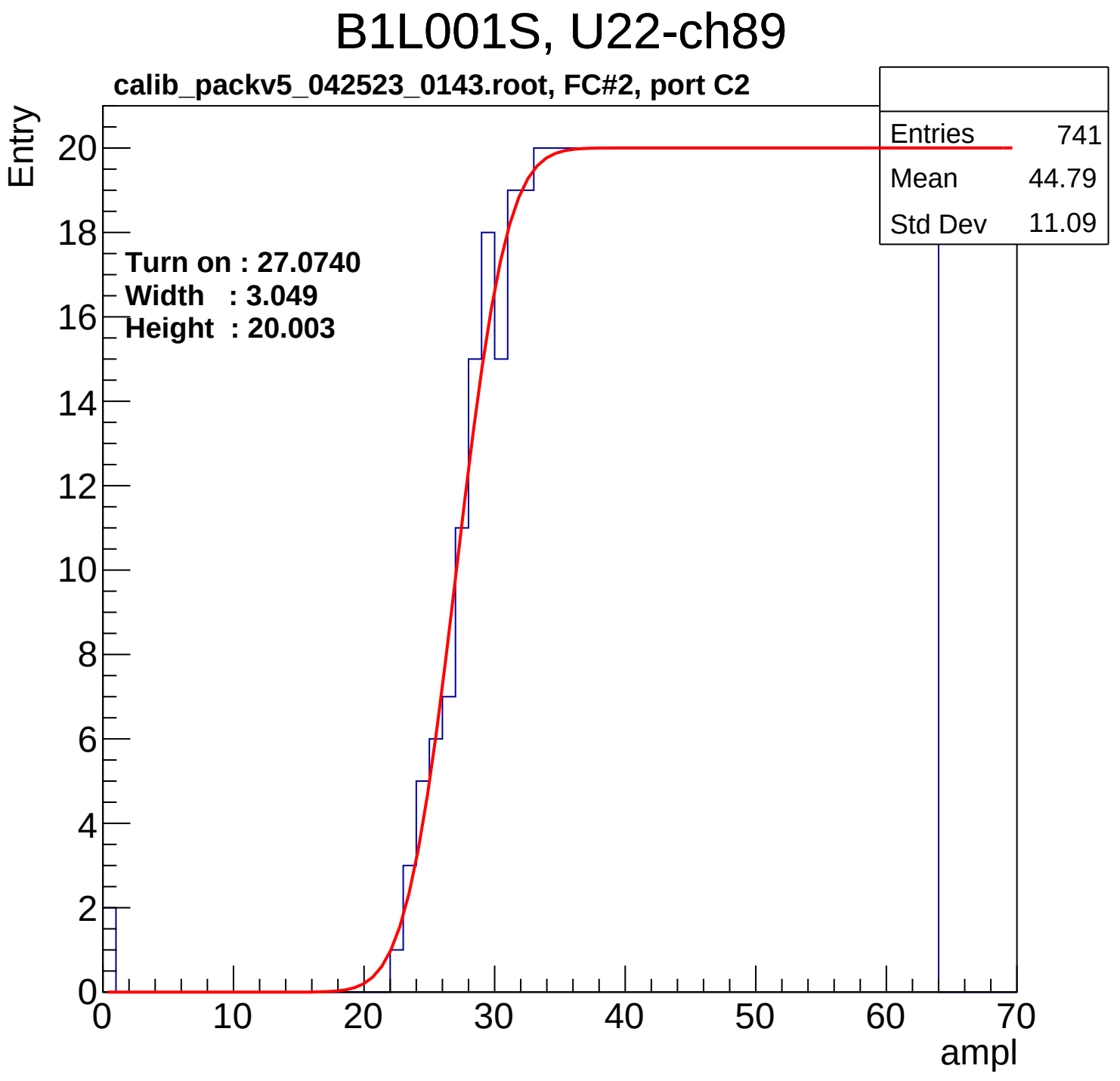
B1L001S, U22-ch89
calib_packv5_042523_0143.root, FC#2, port C2
Entries 741
Mean 44.79
Std Dev 11.09
Turn on : 27.0740
Width : 3.049
Height : 20.003
Entry
ampl
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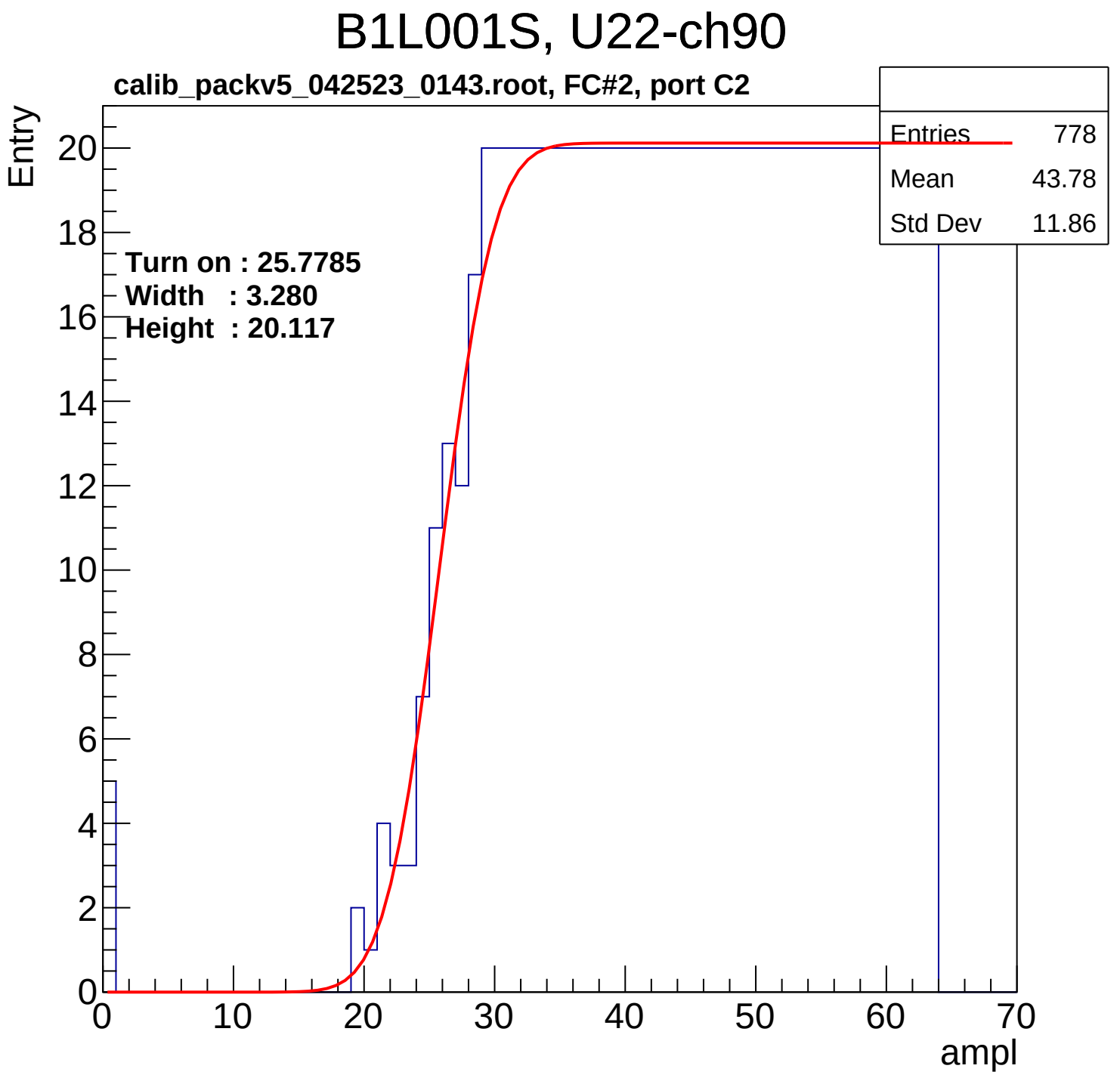
B1L001S, U22-ch90
calib_packv5_042523_0143.root, FC#2, port C2
Entries 778
Mean 43.78
Std Dev 11.86
Turn on : 25.7785
Width : 3.280
Height : 20.117
Entry
ampl
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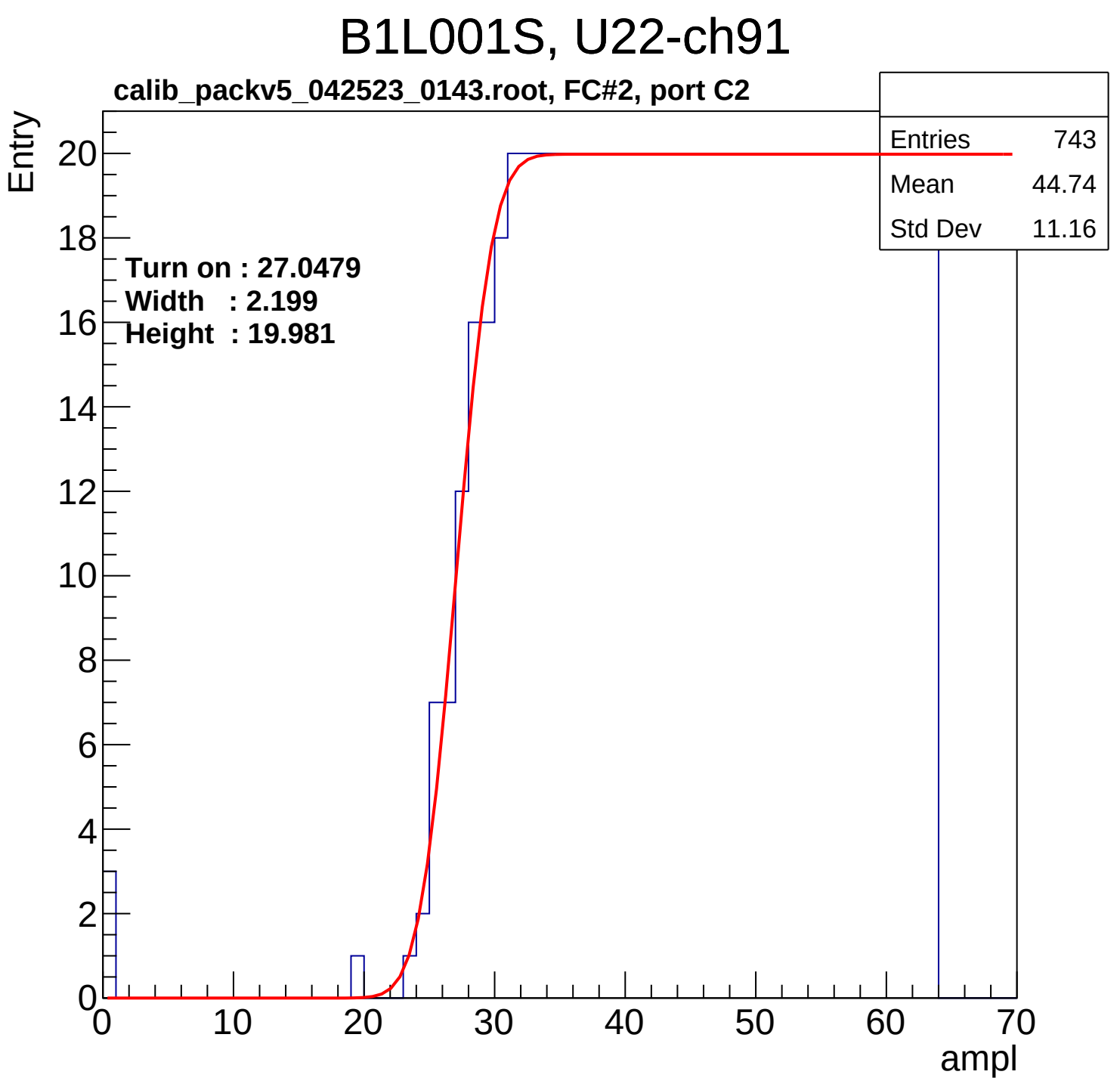
B1L001S, U22-ch91
calib_packv5_042523_0143.root, FC#2, port C2
Entries 743
Mean 44.74
Std Dev 11.16
Turn on : 27.0479
Width : 2.199
Height : 19.981
Entry
ampl
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6
8
10
12
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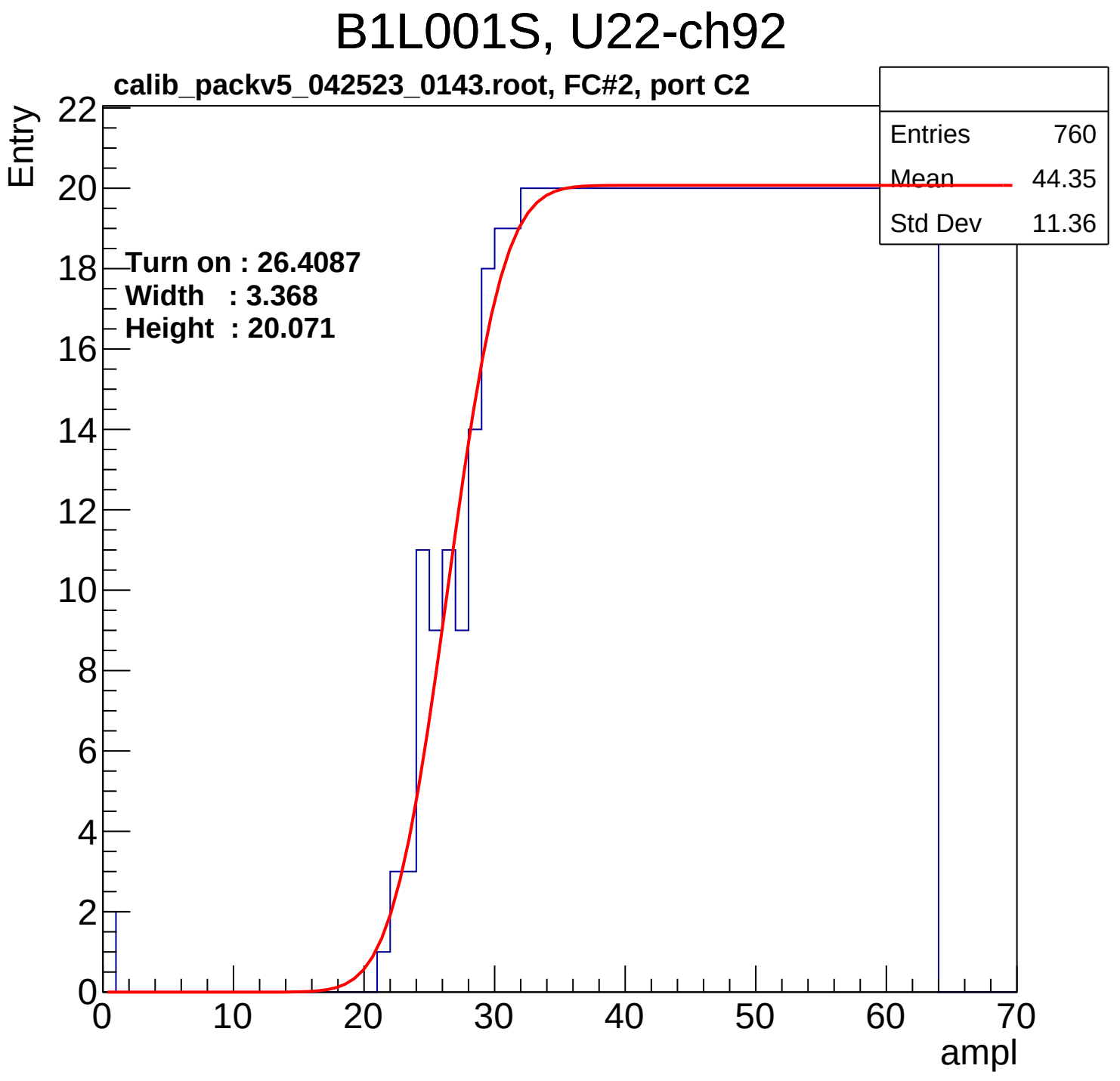
B1L001S, U22-ch92
calib_packv5_042523_0143.root, FC#2, port C2
Entries 760
Mean 44.35
Std Dev 11.36
Turn on : 26.4087
Width : 3.368
Height : 20.071
Entry
ampl
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8
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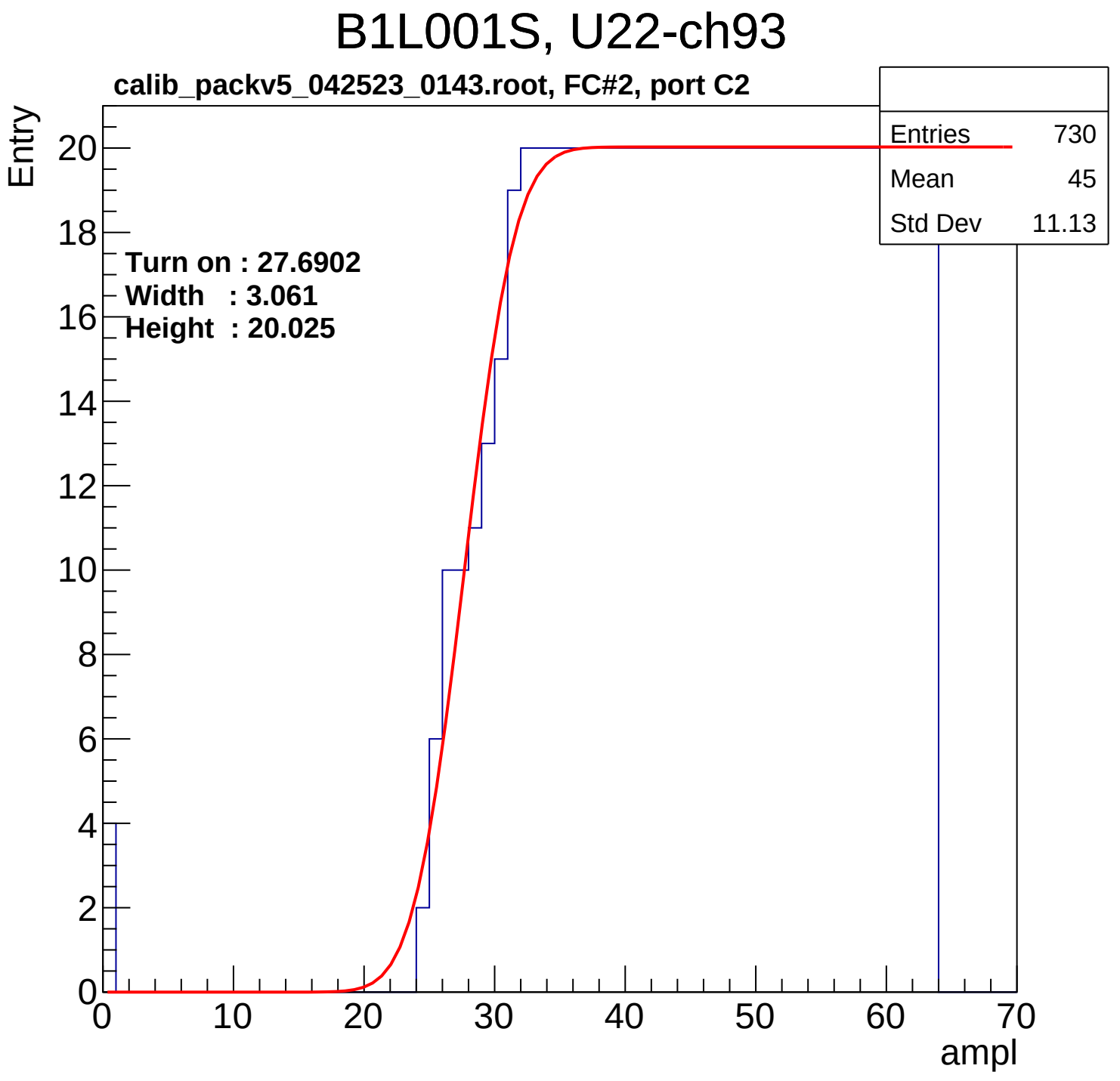
B1L001S, U22-ch93
calib_packv5_042523_0143.root, FC#2, port C2
Entries 730
Mean 45
Std Dev 11.13
Turn on : 27.6902
Width : 3.061
Height : 20.025
Entry
ampl
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8
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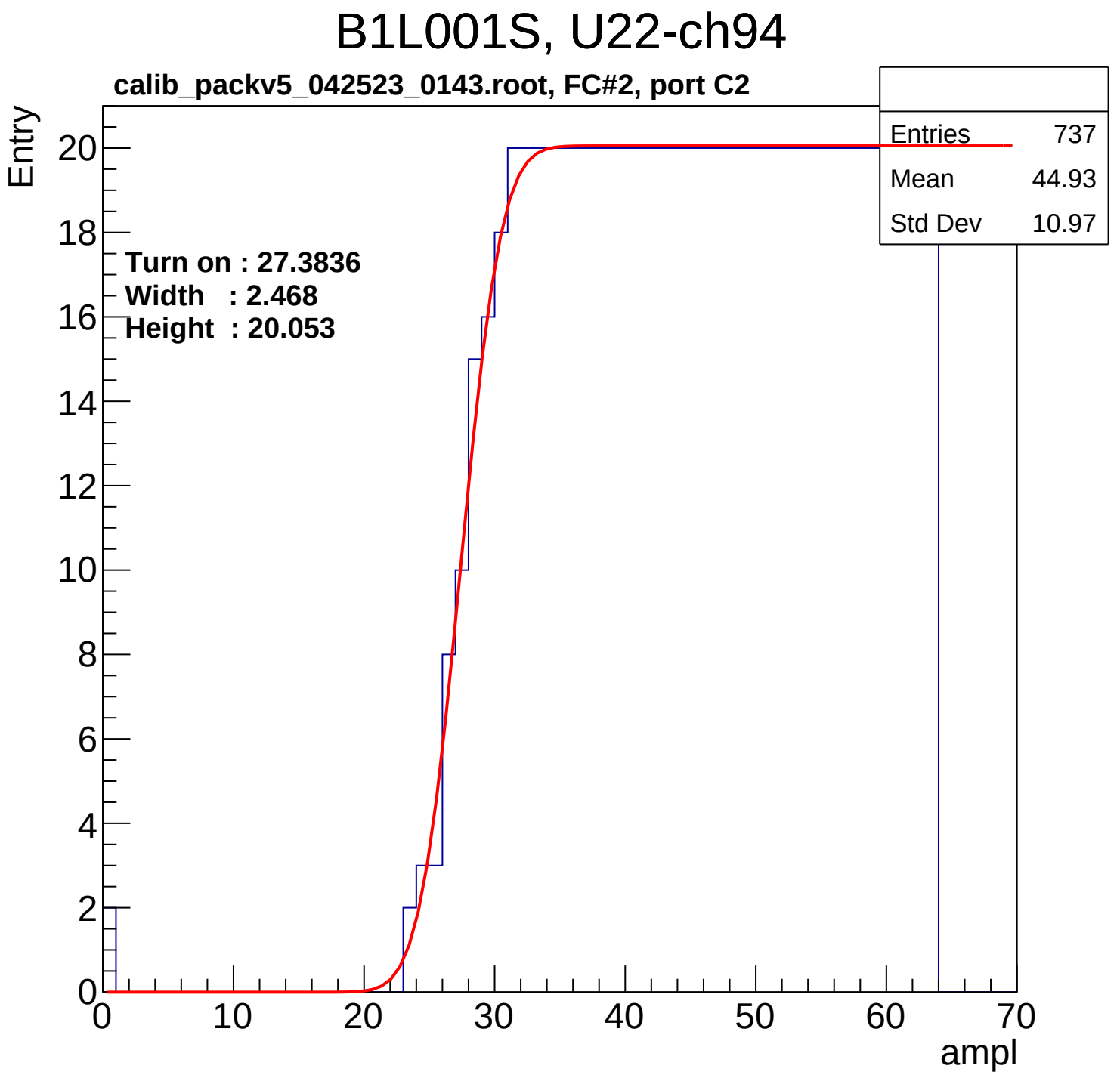
B1L001S, U22-ch94
calib_packv5_042523_0143.root, FC#2, port C2
Entries 737
Mean 44.93
Std Dev 10.97
Turn on : 27.3836
Width : 2.468
Height : 20.053
Entry
ampl
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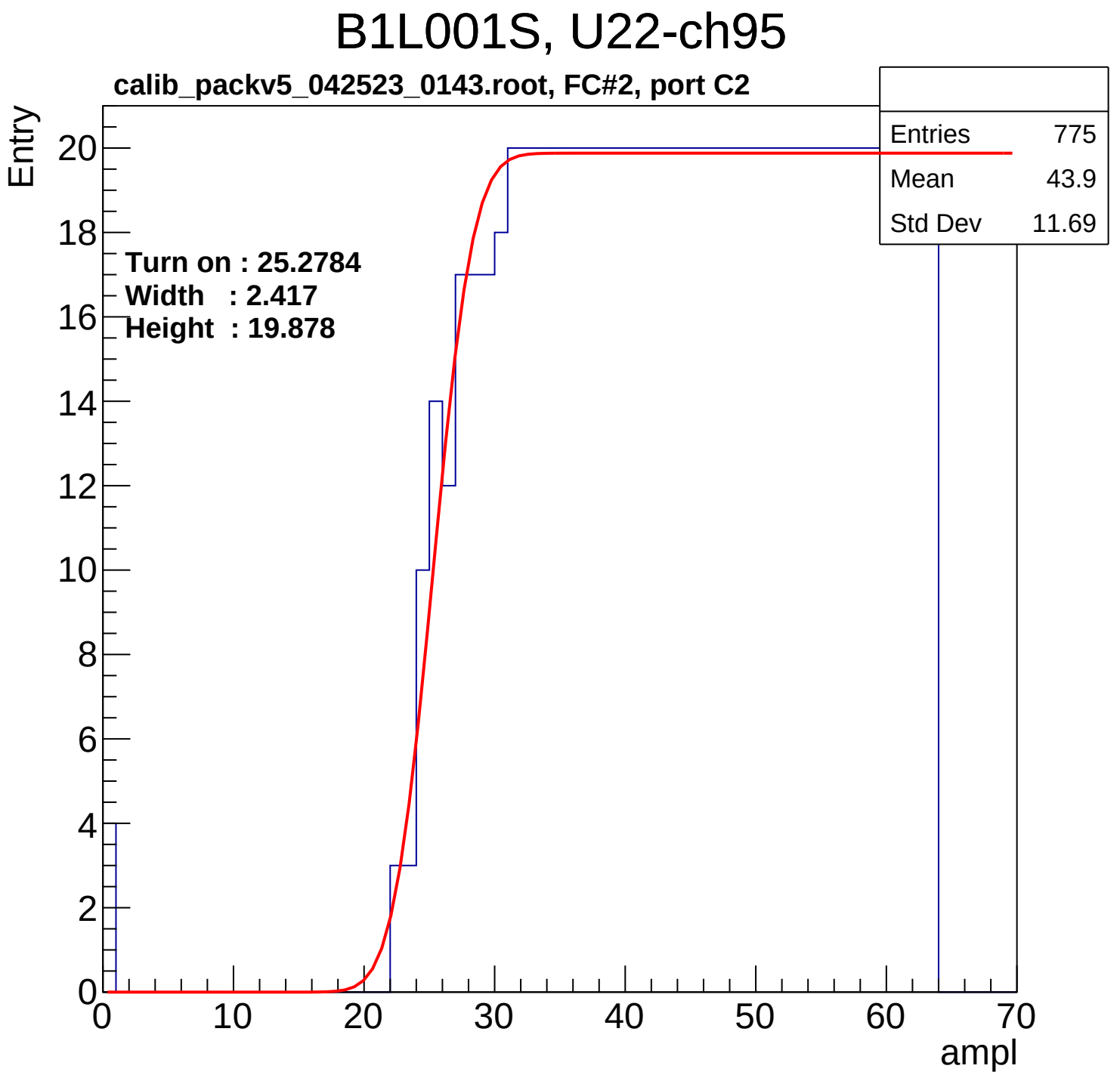
B1L001S, U22-ch95
calib_packv5_042523_0143.root, FC#2, port C2
Entries 775
Mean 43.9
Std Dev 11.69
Turn on : 25.2784
Width : 2.417
Height : 19.878
Entry
ampl
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8
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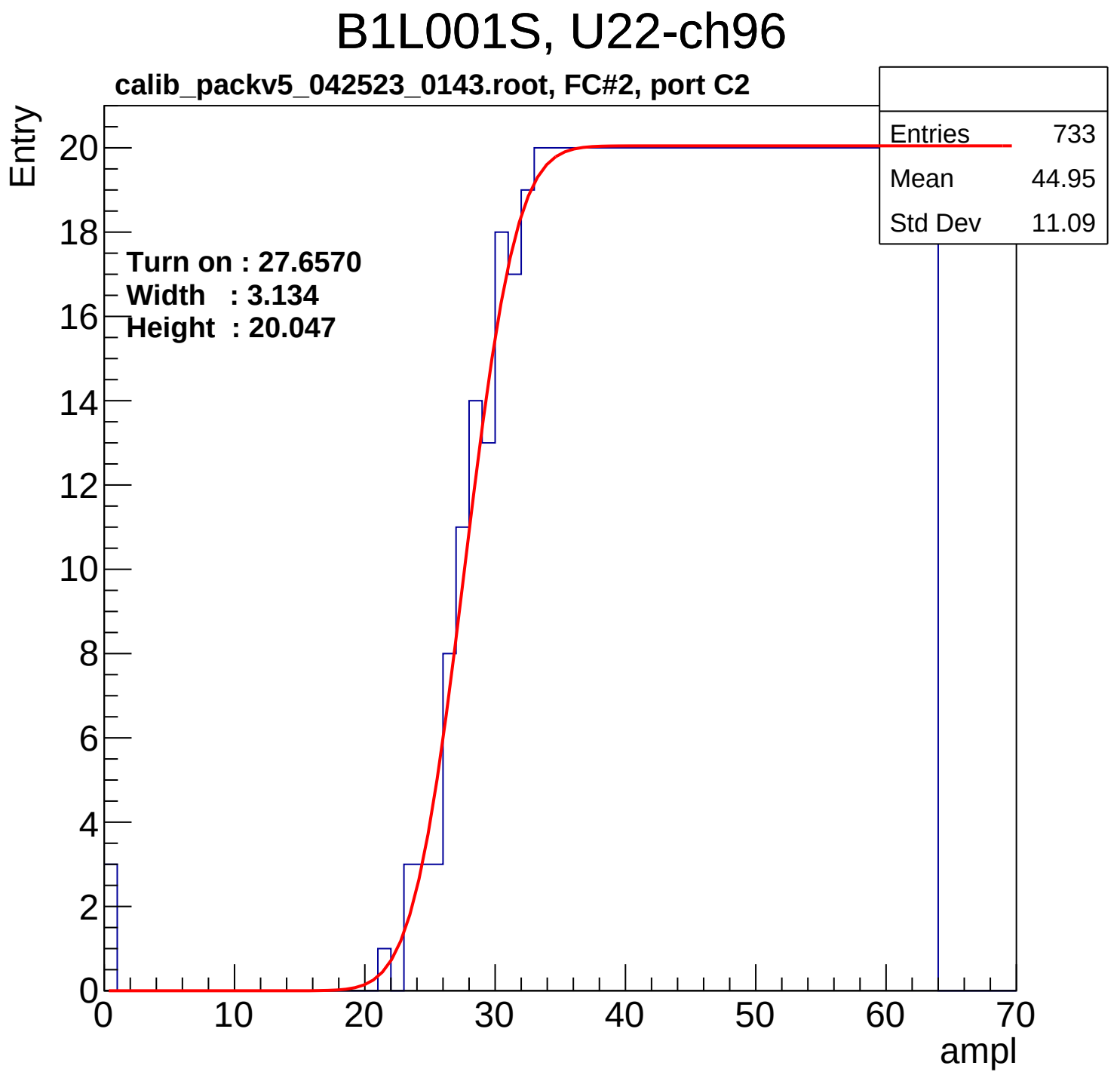
B1L001S, U22-ch96
calib_packv5_042523_0143.root, FC#2, port C2
Entries 733
Mean 44.95
Std Dev 11.09
Turn on : 27.6570
Width : 3.134
Height : 20.047
Entry
ampl
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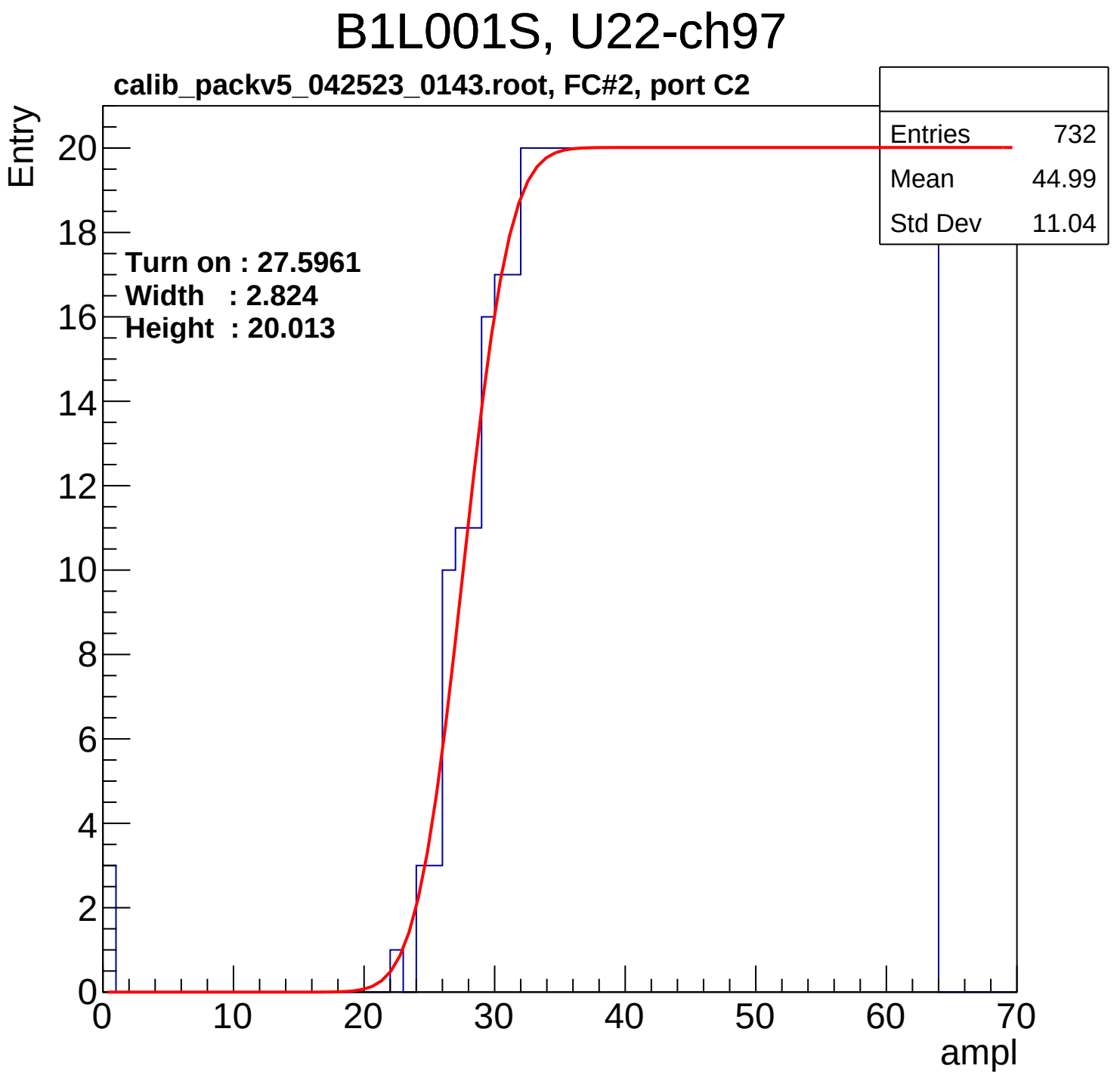
B1L001S, U22-ch97
calib_packv5_042523_0143.root, FC#2, port C2
Entries 732
Mean 44.99
Std Dev 11.04
Turn on : 27.5961
Width : 2.824
Height : 20.013
Entry
ampl
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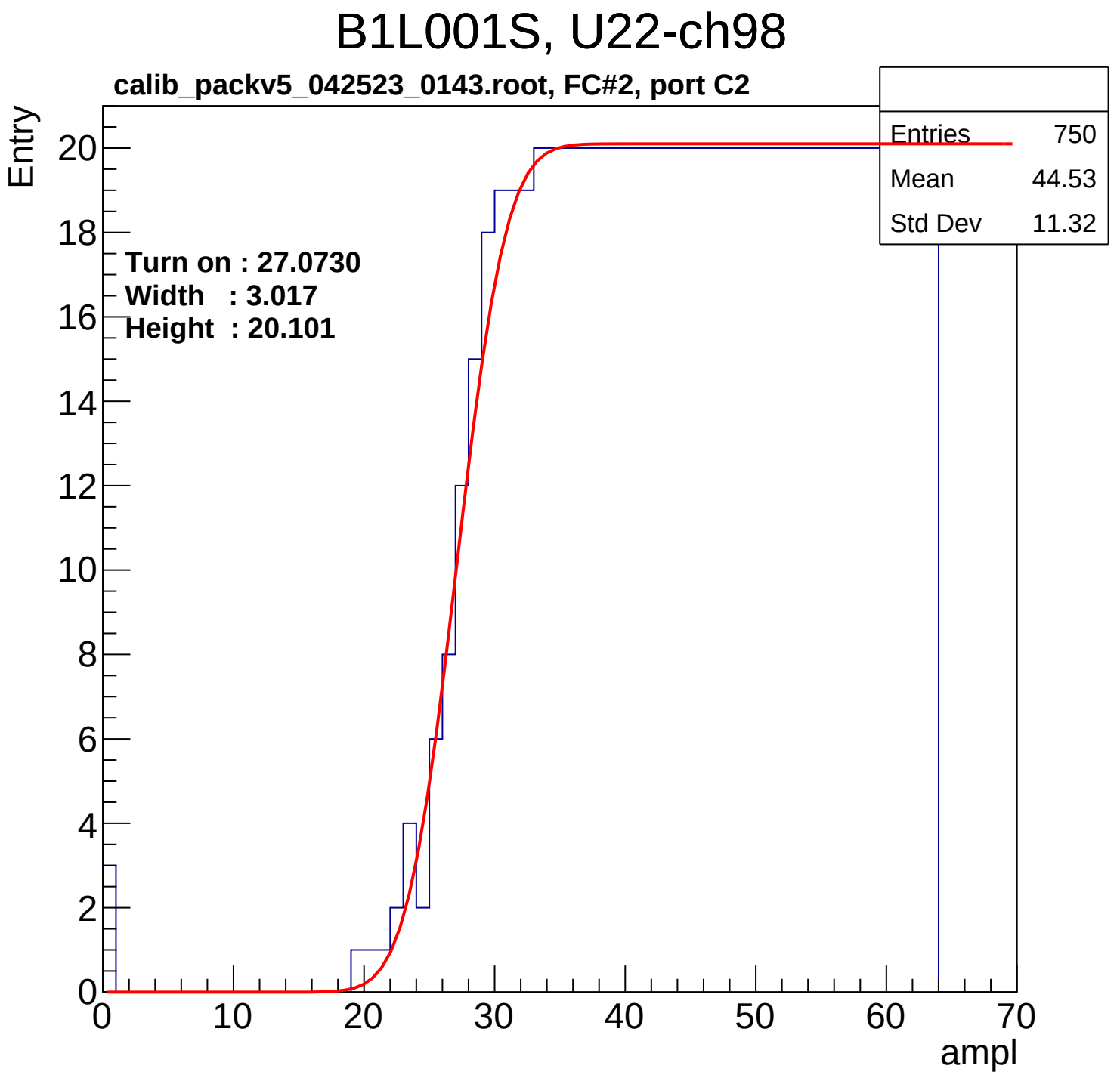
B1L001S, U22-ch98
calib_packv5_042523_0143.root, FC#2, port C2
Entries 750
Mean 44.53
Std Dev 11.32
Turn on : 27.0730
Width : 3.017
Height : 20.101
Entry
ampl
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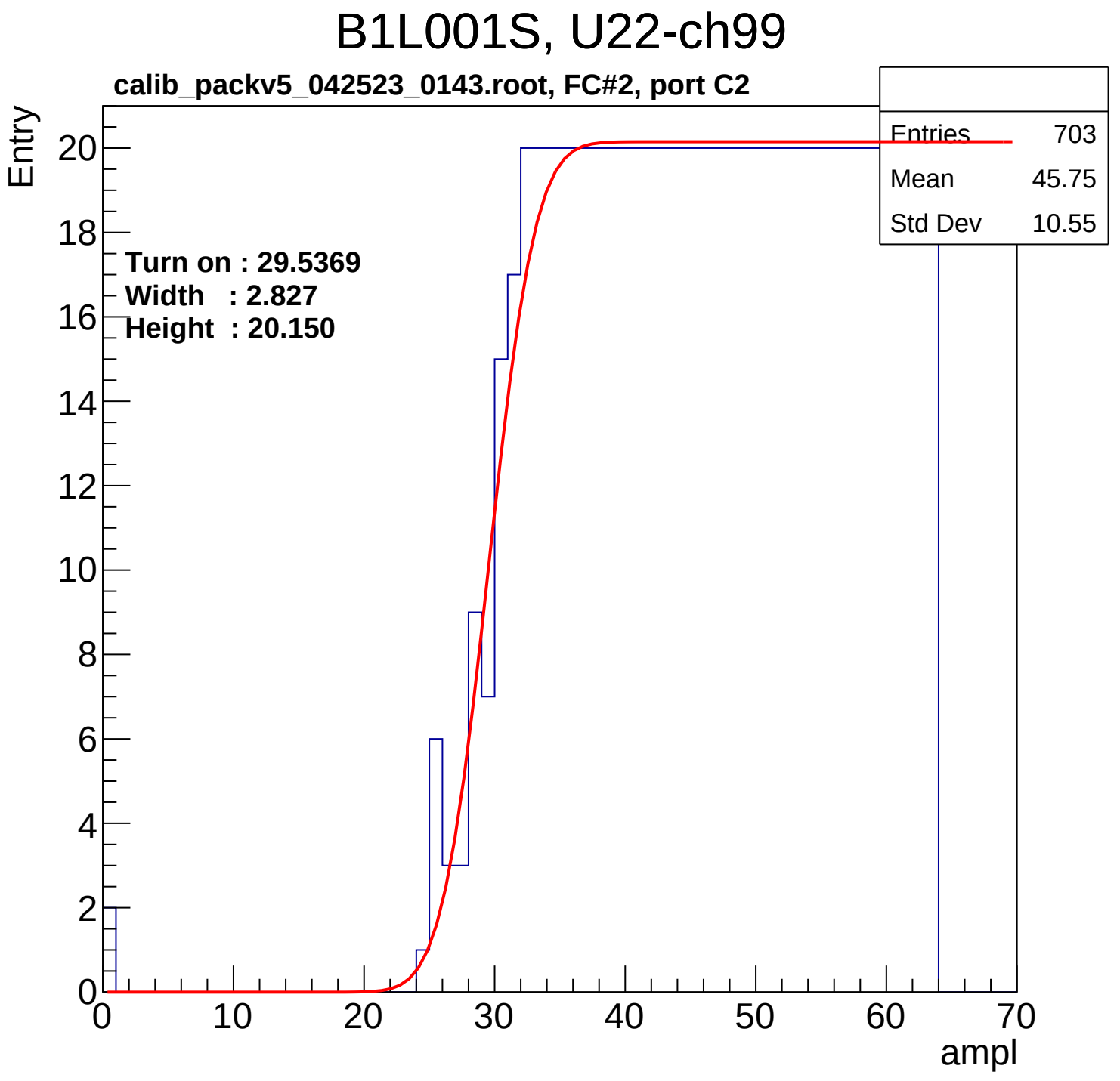
B1L001S, U22-ch99
calib_packv5_042523_0143.root, FC#2, port C2
Entries 703
Mean 45.75
Std Dev 10.55
Turn on : 29.5369
Width : 2.827
Height : 20.150
Entry
ampl
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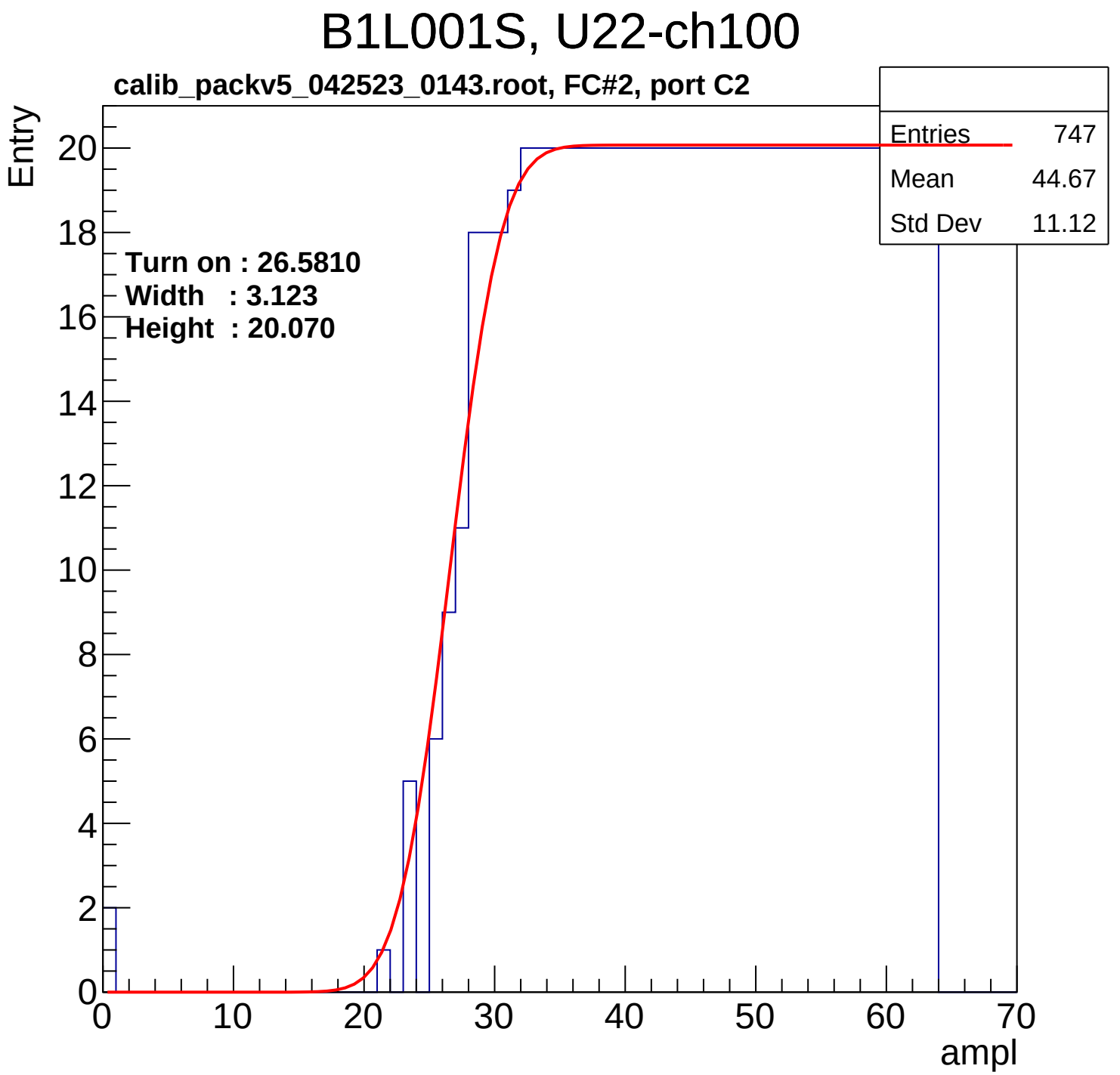
B1L001S, U22-ch100
calib_packv5_042523_0143.root, FC#2, port C2
Entries 747
Mean 44.67
Std Dev 11.12
Turn on : 26.5810
Width : 3.123
Height : 20.070
Entry
ampl
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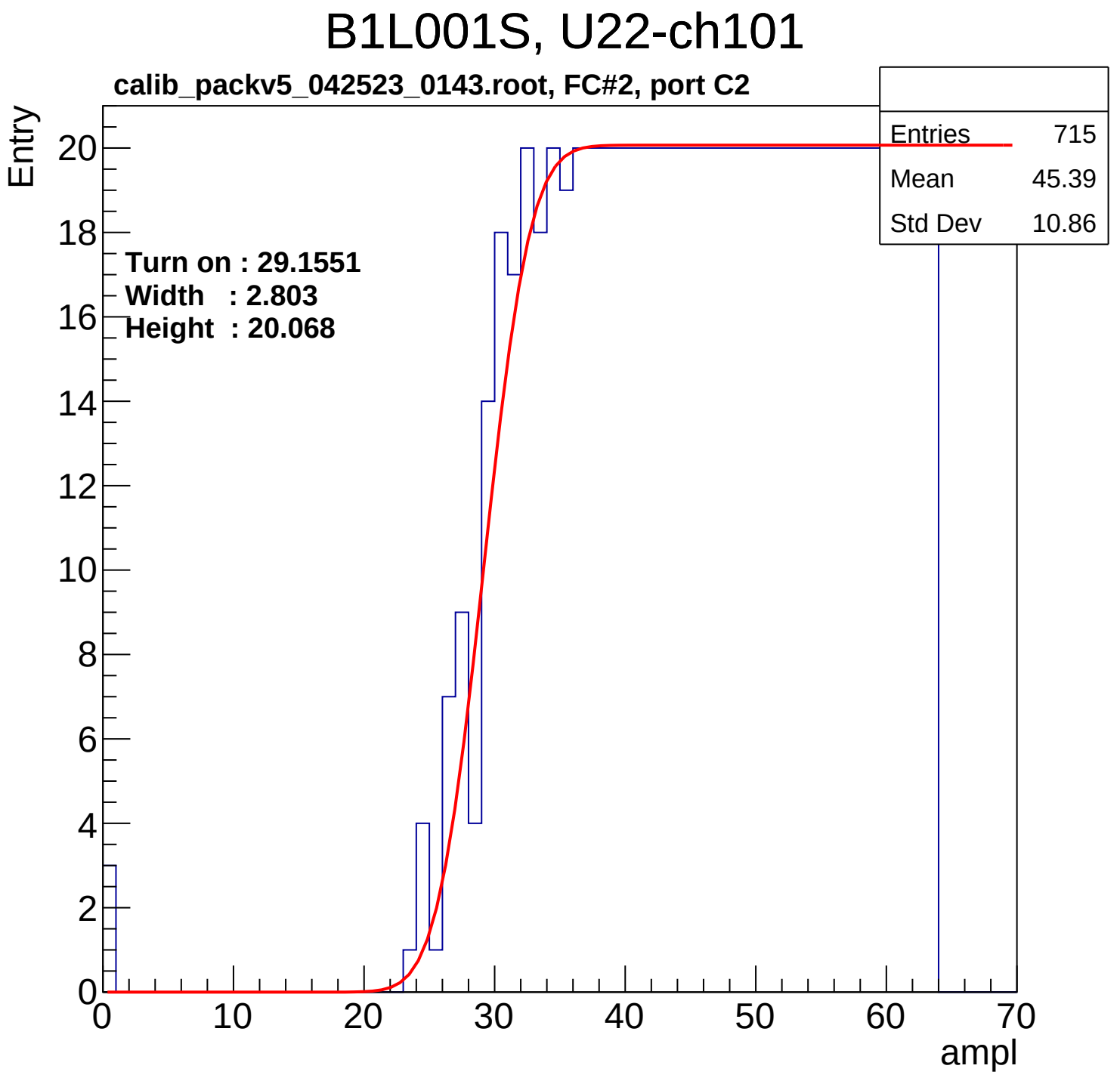
B1L001S, U22-ch101
calib_packv5_042523_0143.root, FC#2, port C2
Entries 715
Mean 45.39
Std Dev 10.86
Turn on : 29.1551
Width : 2.803
Height : 20.068
Entry
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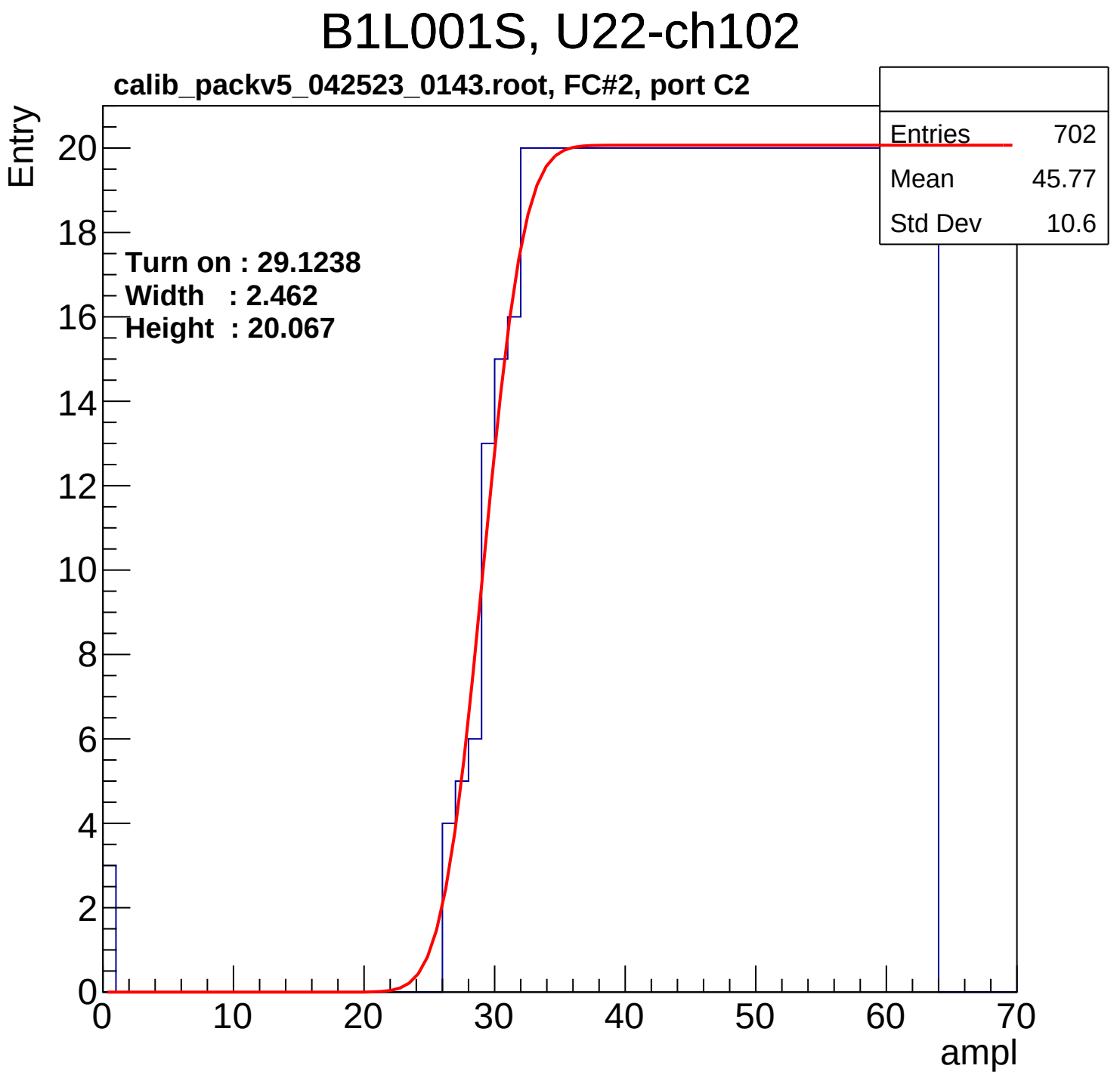
B1L001S, U22-ch102
calib_packv5_042523_0143.root, FC#2, port C2
Entries 702
Mean 45.77
Std Dev 10.6
Turn on : 29.1238
Width : 2.462
Height : 20.067
Entry
ampl
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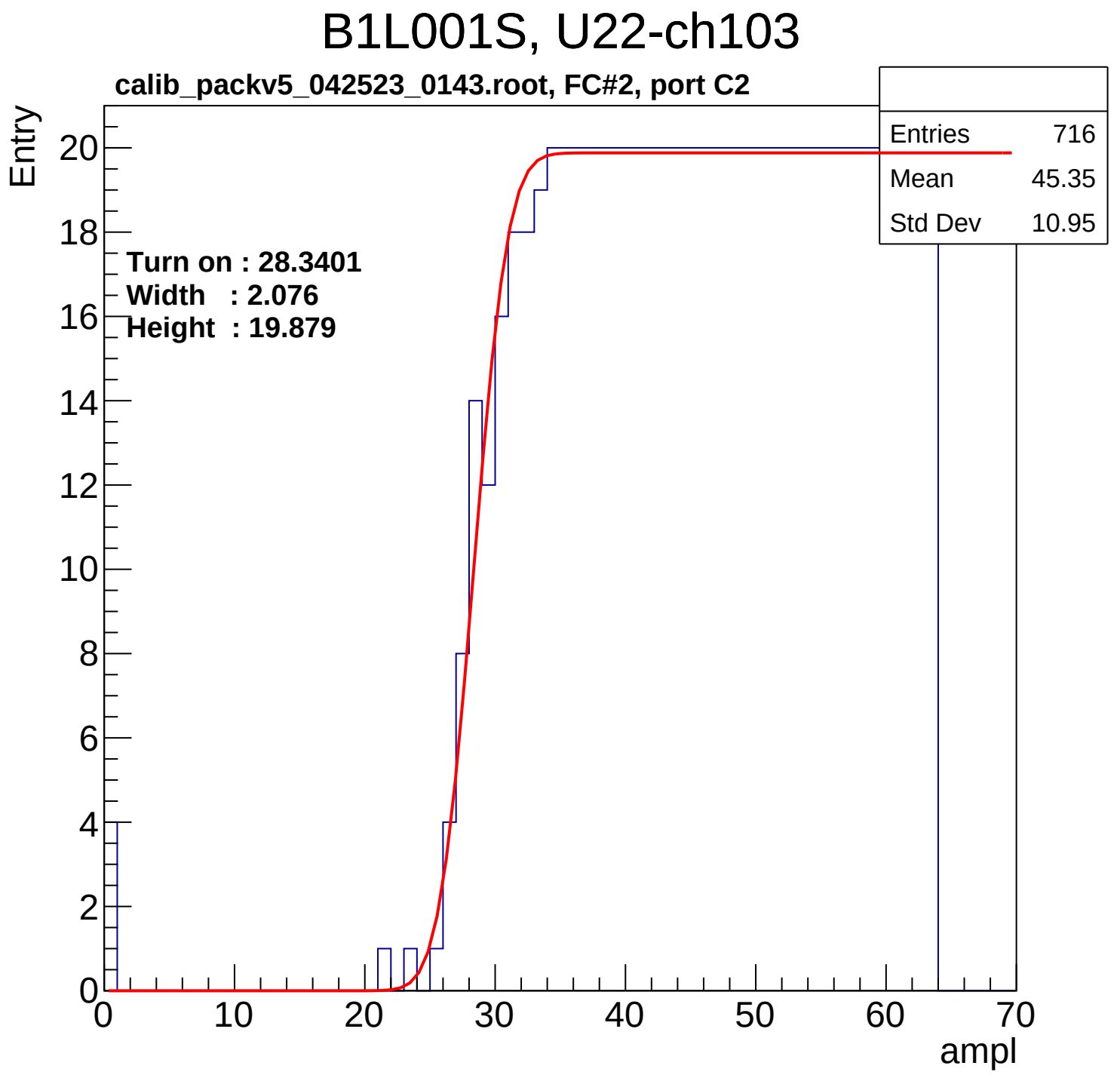
B1L001S, U22-ch103
calib_packv5_042523_0143.root, FC#2, port C2
Entries 716
Mean 45.35
Std Dev 10.95
Turn on : 28.3401
Width : 2.076
Height : 19.879
Entry
ampl
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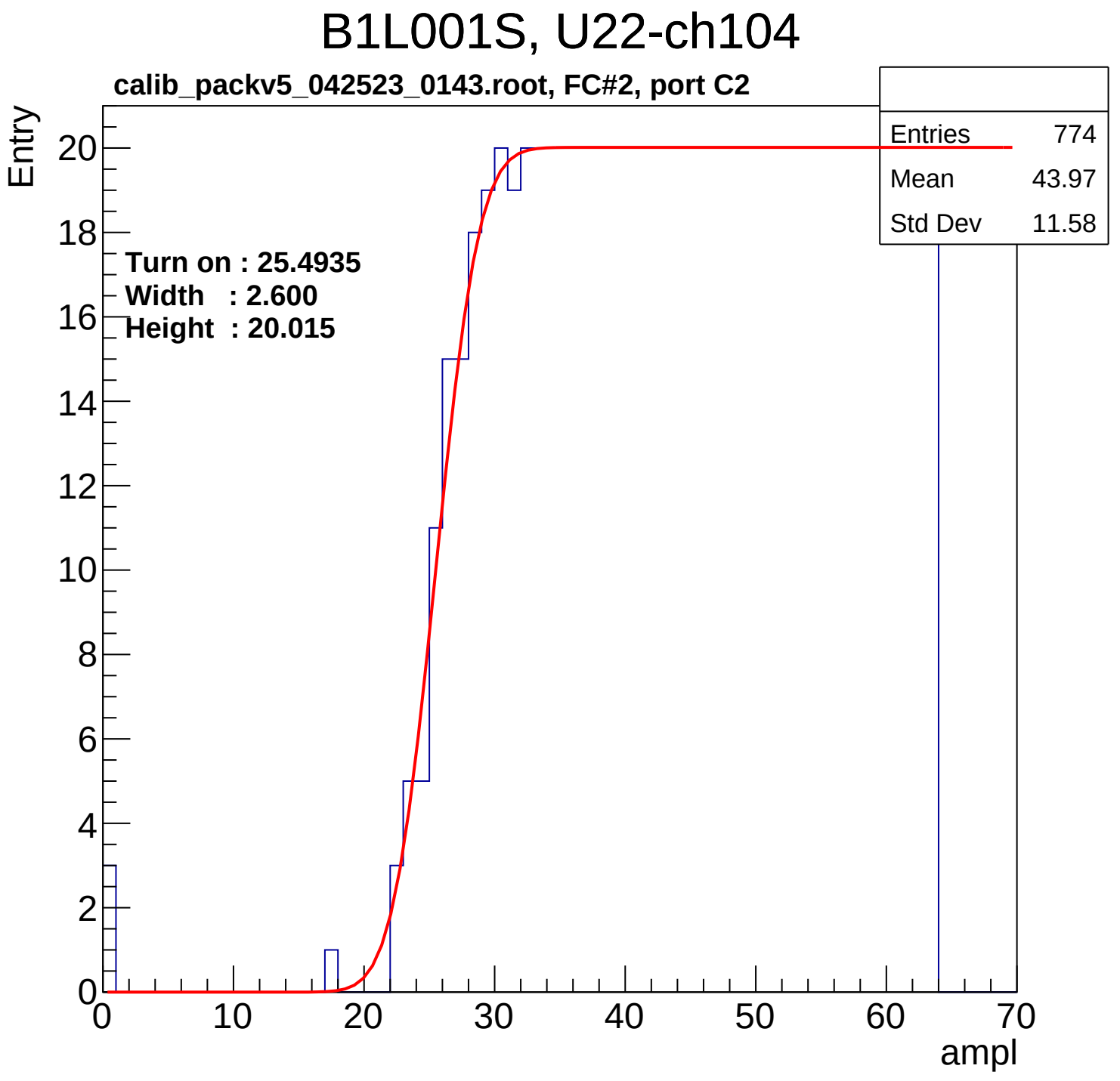
B1L001S, U22-ch104
calib_packv5_042523_0143.root, FC#2, port C2
Entries 774
Mean 43.97
Std Dev 11.58
Turn on : 25.4935
Width : 2.600
Height : 20.015
Entry
ampl
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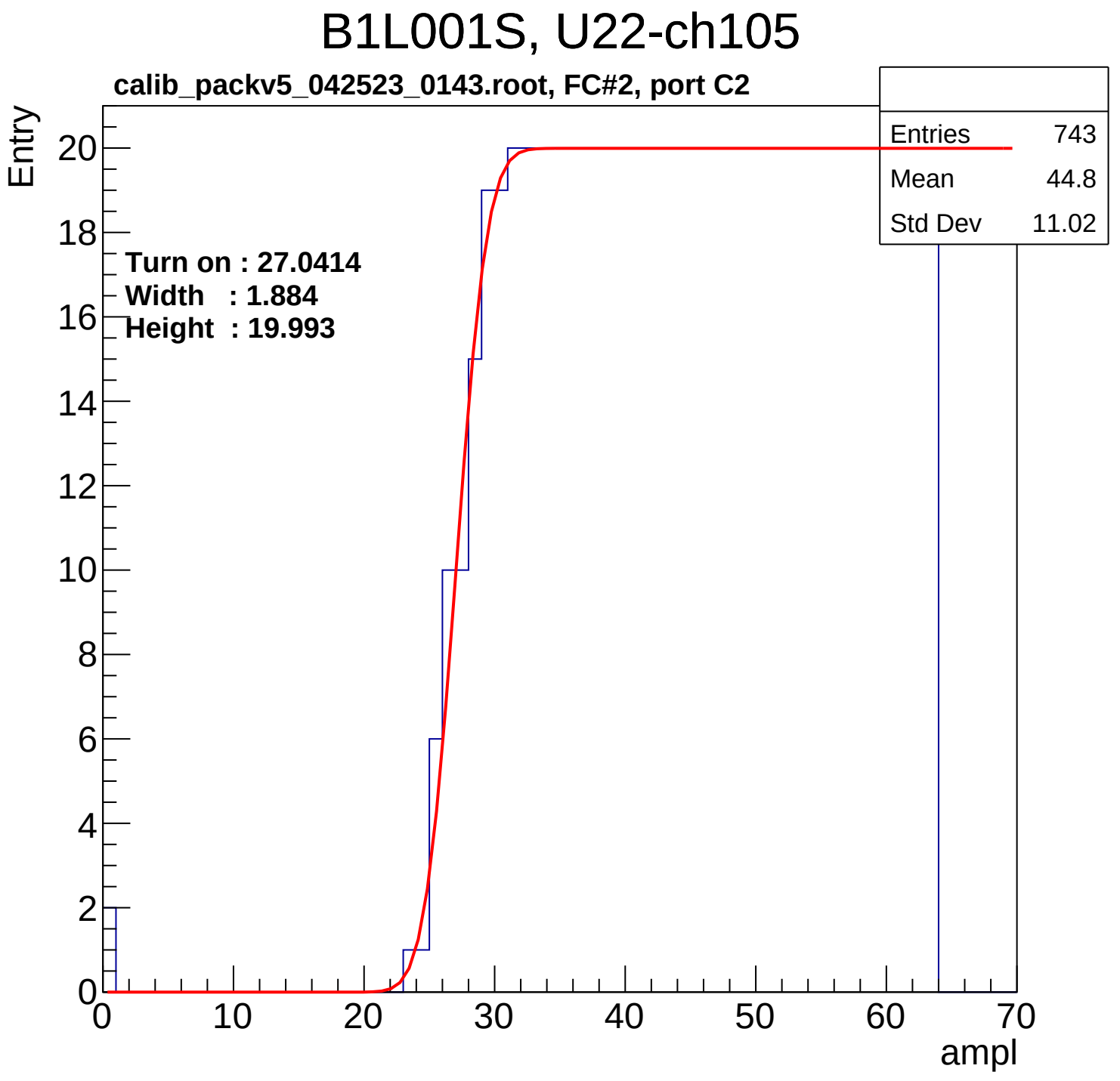
B1L001S, U22-ch105
calib_packv5_042523_0143.root, FC#2, port C2
Entries 743
Mean 44.8
Std Dev 11.02
Turn on : 27.0414
Width : 1.884
Height : 19.993
Entry
ampl
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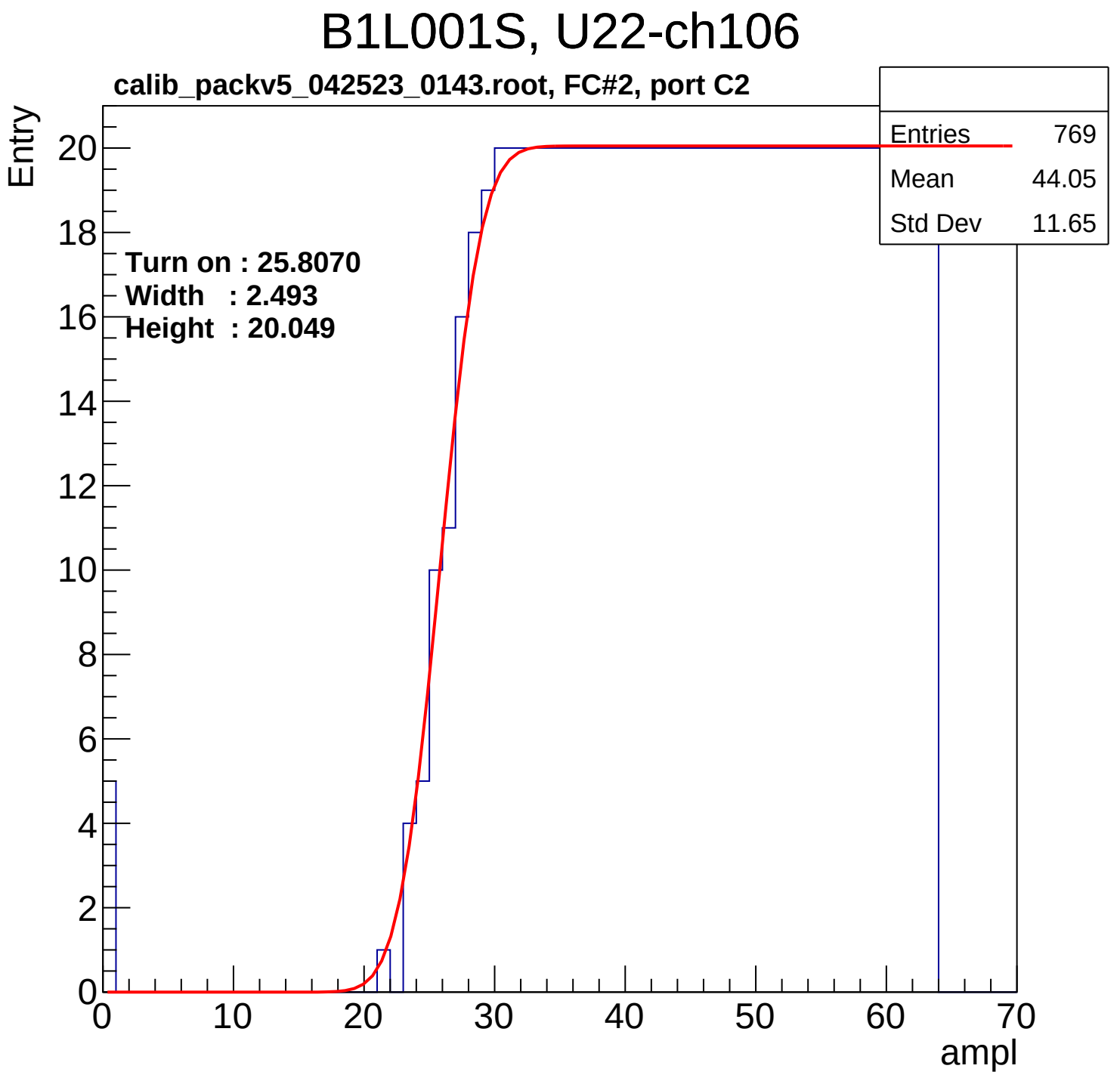
B1L001S, U22-ch106
calib_packv5_042523_0143.root, FC#2, port C2
Entries 769
Mean 44.05
Std Dev 11.65
Turn on : 25.8070
Width : 2.493
Height : 20.049
Entry
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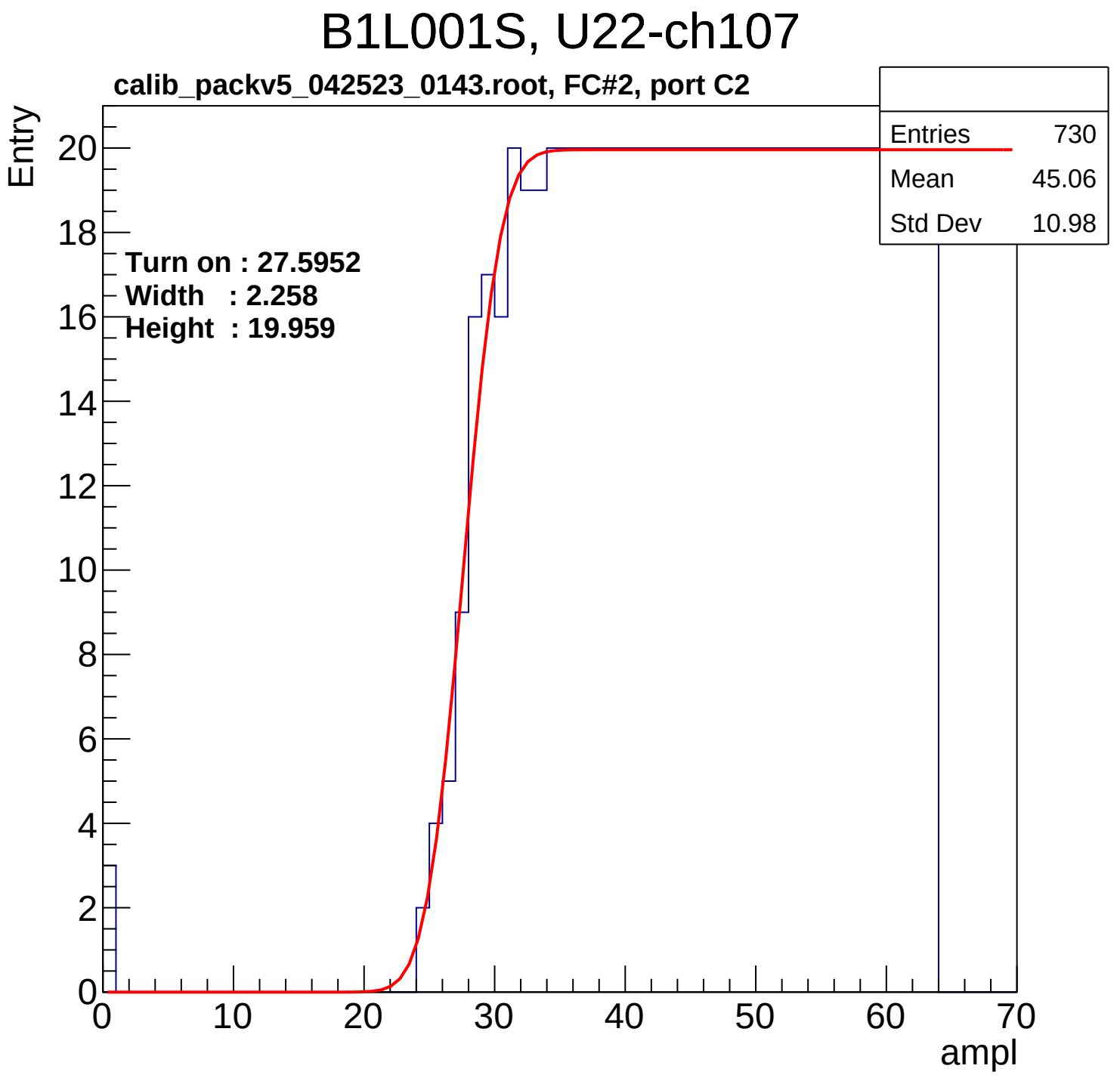
B1L001S, U22-ch107
calib_packv5_042523_0143.root, FC#2, port C2
Entries 730
Mean 45.06
Std Dev 10.98
Turn on : 27.5952
Width : 2.258
Height : 19.959
Entry
ampl
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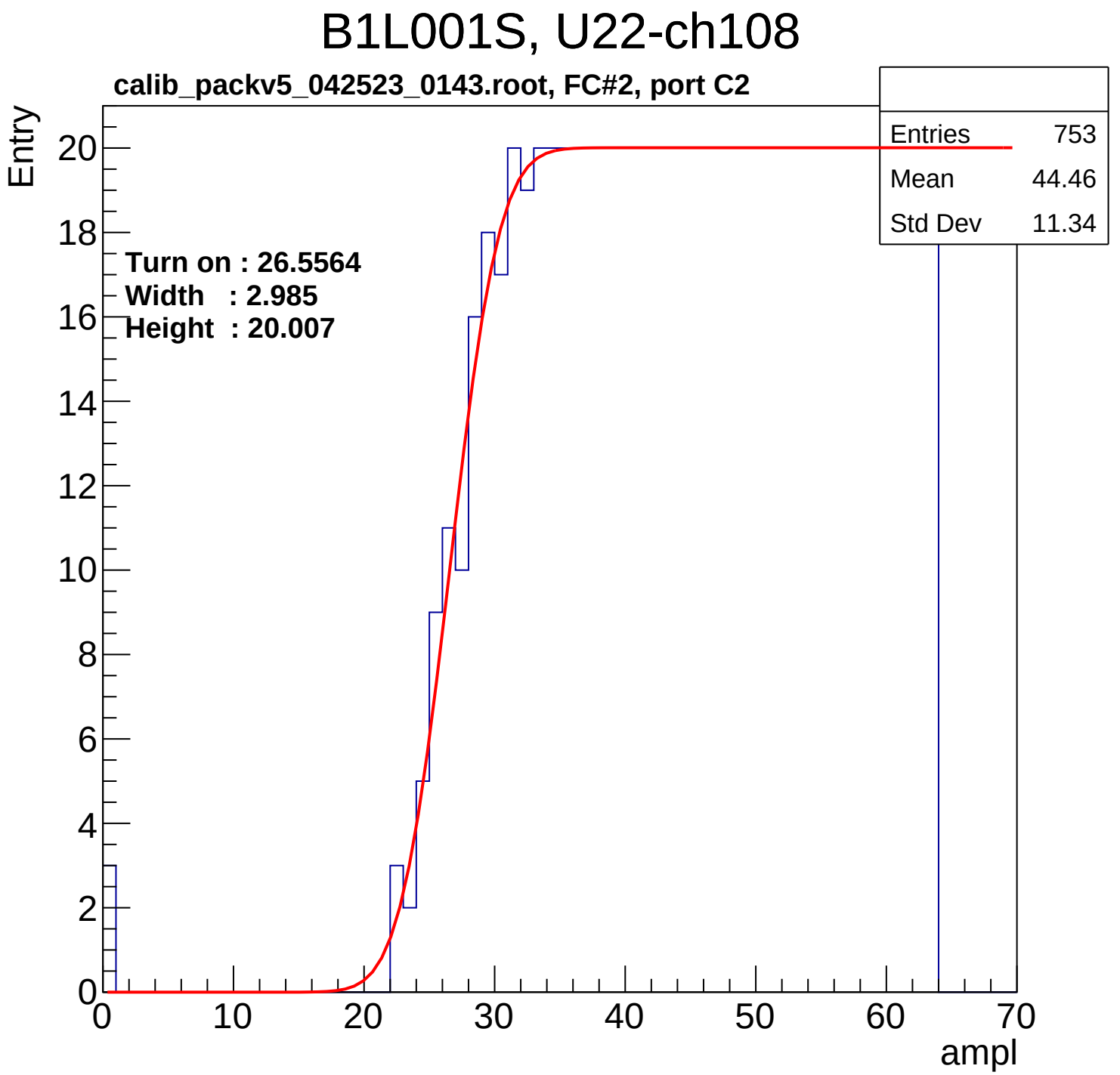
B1L001S, U22-ch108
calib_packv5_042523_0143.root, FC#2, port C2
Entries 753
Mean 44.46
Std Dev 11.34
Turn on : 26.5564
Width : 2.985
Height : 20.007
Entry
ampl
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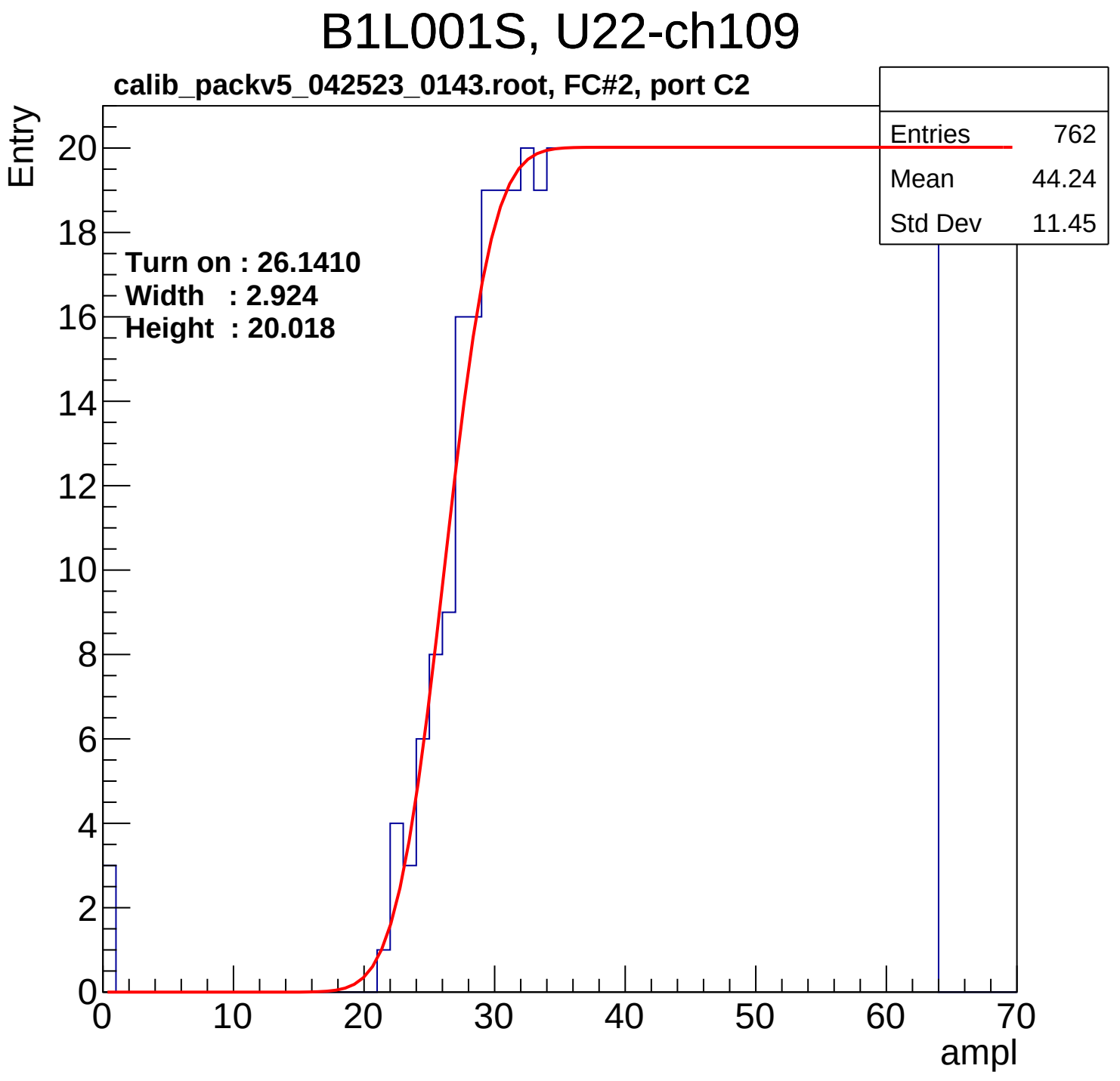
B1L001S, U22-ch109
calib_packv5_042523_0143.root, FC#2, port C2
Entries 762
Mean 44.24
Std Dev 11.45
Turn on : 26.1410
Width : 2.924
Height : 20.018
Entry
ampl
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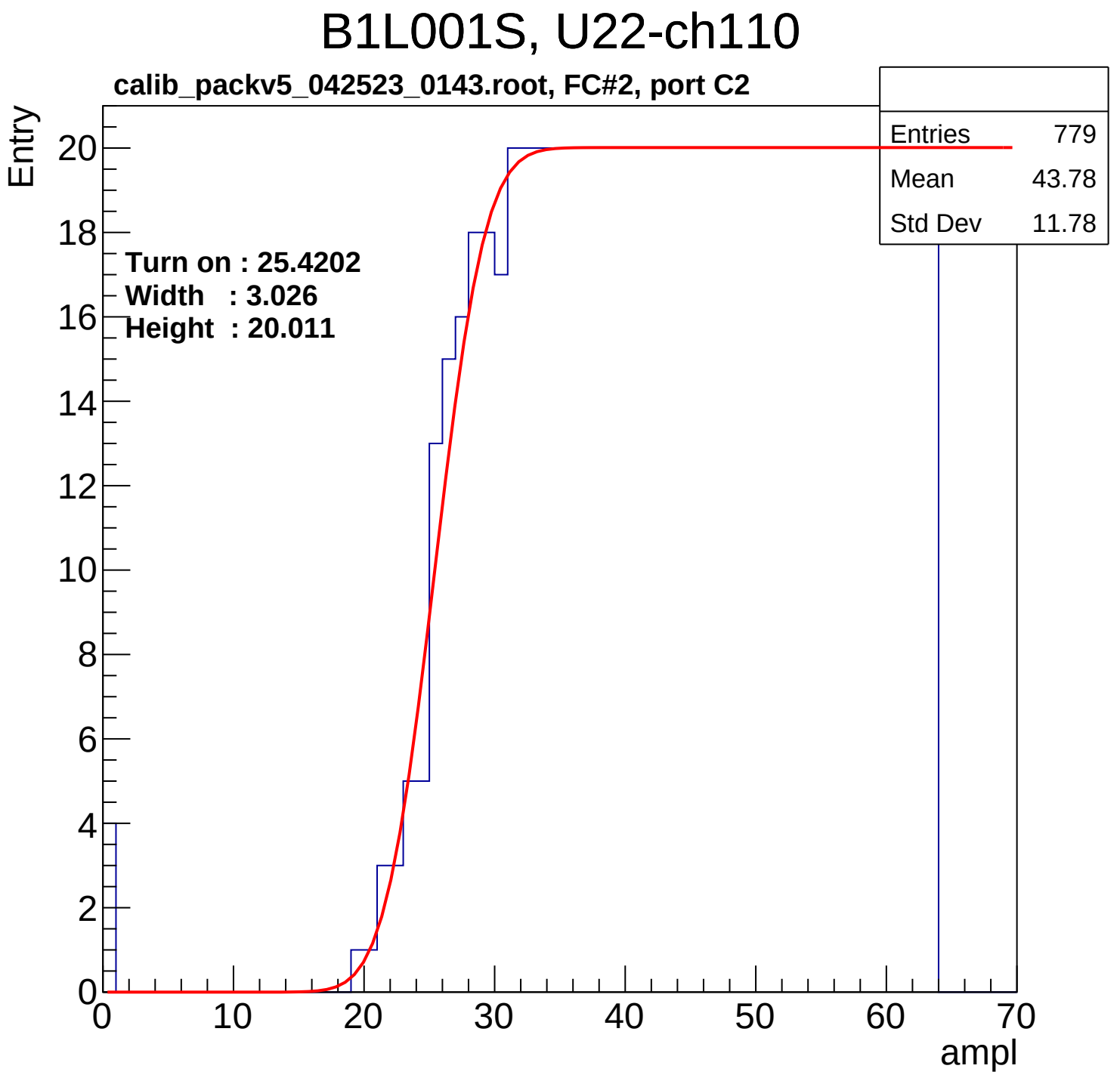
B1L001S, U22-ch110
calib_packv5_042523_0143.root, FC#2, port C2
Entries 779
Mean 43.78
Std Dev 11.78
Turn on : 25.4202
Width : 3.026
Height : 20.011
Entry
ampl
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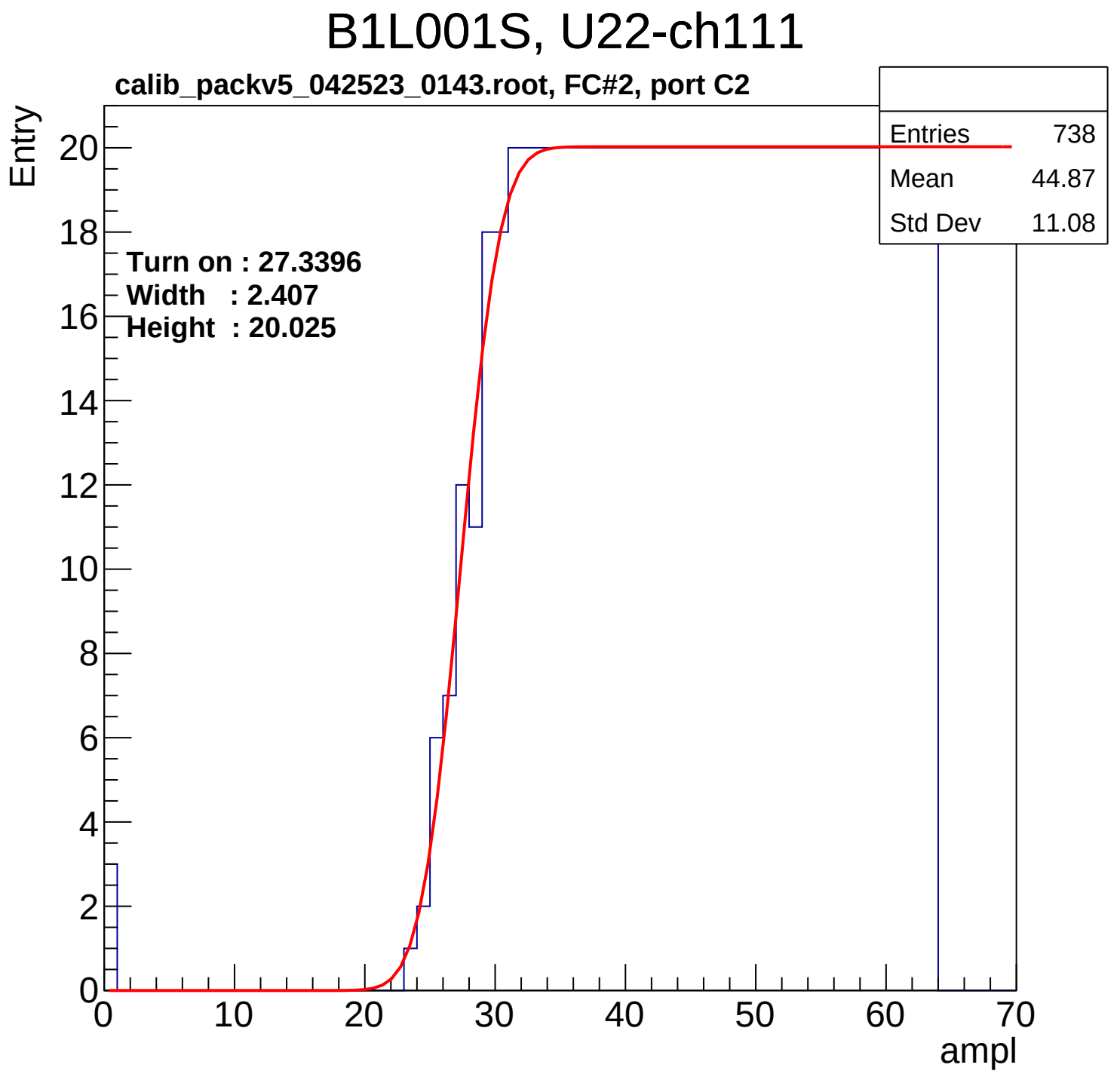
B1L001S, U22-ch111
calib_packv5_042523_0143.root, FC#2, port C2
Entries 738
Mean 44.87
Std Dev 11.08
Turn on : 27.3396
Width : 2.407
Height : 20.025
Entry
ampl
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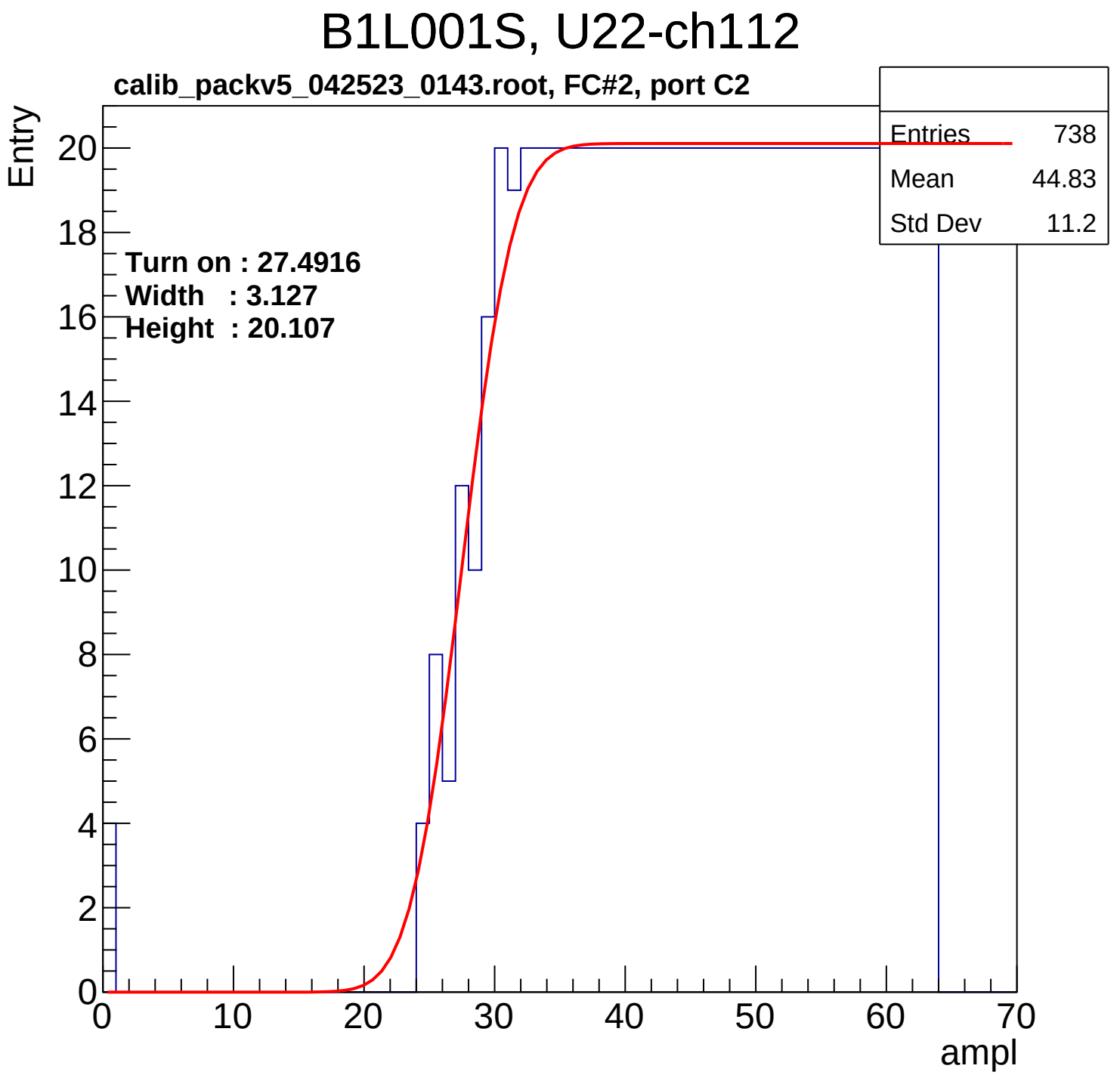
B1L001S, U22-ch112
calib_packv5_042523_0143.root, FC#2, port C2
Entries 738
Mean 44.83
Std Dev 11.2
Turn on : 27.4916
Width : 3.127
Height : 20.107
Entry
ampl
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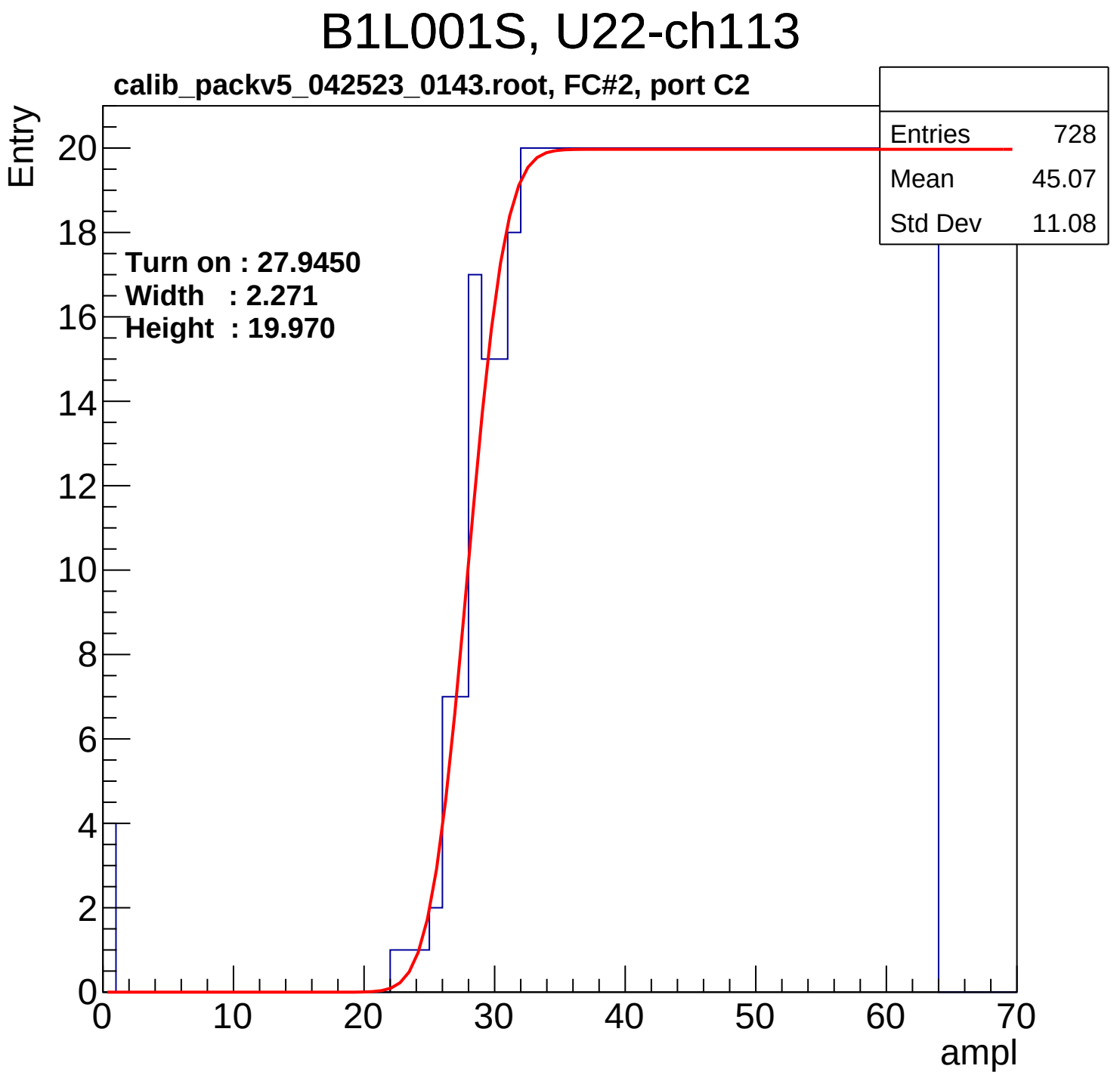
B1L001S, U22-ch113
calib_packv5_042523_0143.root, FC#2, port C2
Entries 728
Mean 45.07
Std Dev 11.08
Turn on : 27.9450
Width : 2.271
Height : 19.970
Entry
ampl
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2
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6
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14
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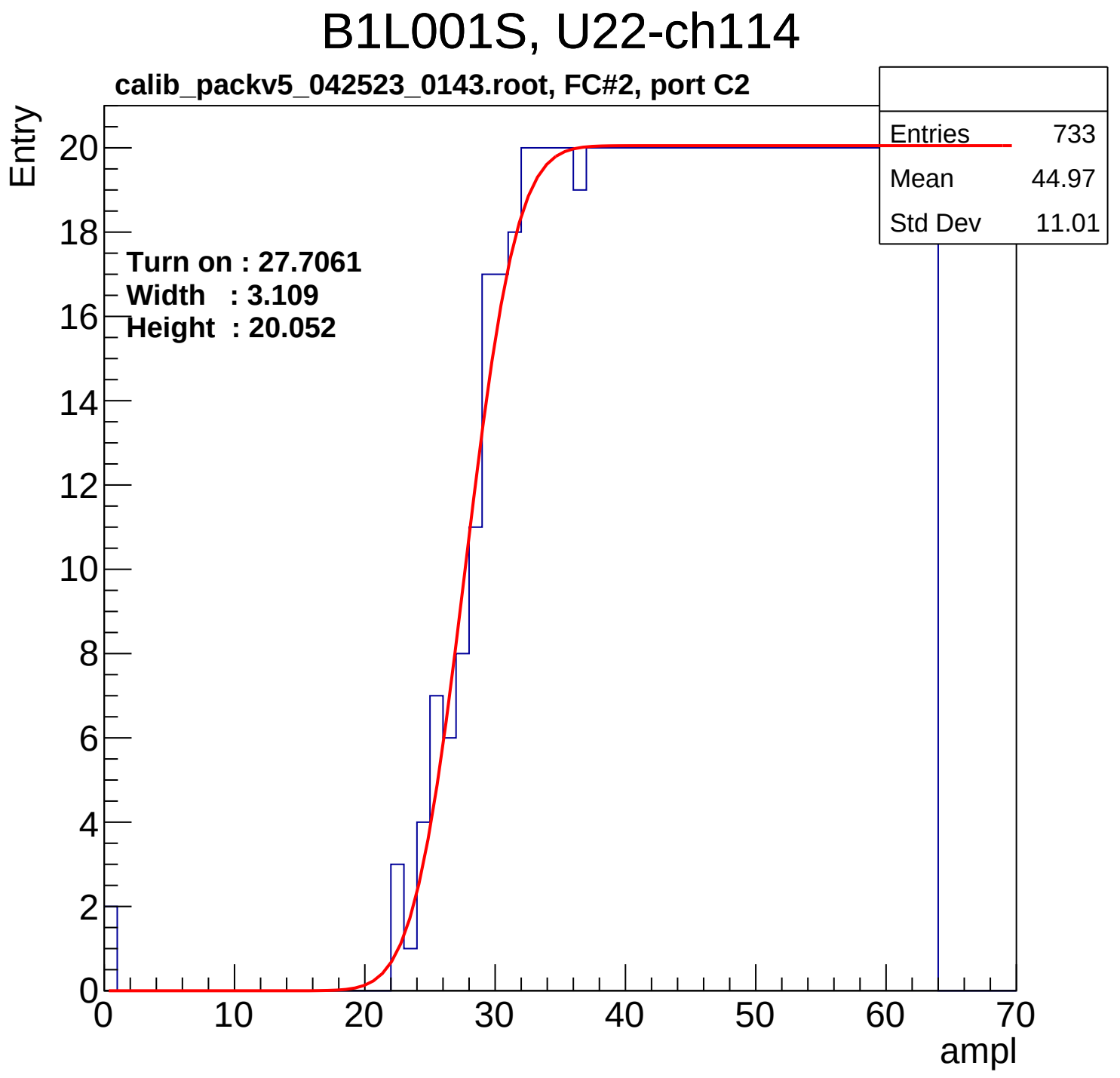
B1L001S, U22-ch114
calib_packv5_042523_0143.root, FC#2, port C2
Entries 733
Mean 44.97
Std Dev 11.01
Turn on : 27.7061
Width : 3.109
Height : 20.052
Entry
ampl
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6
8
10
12
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16
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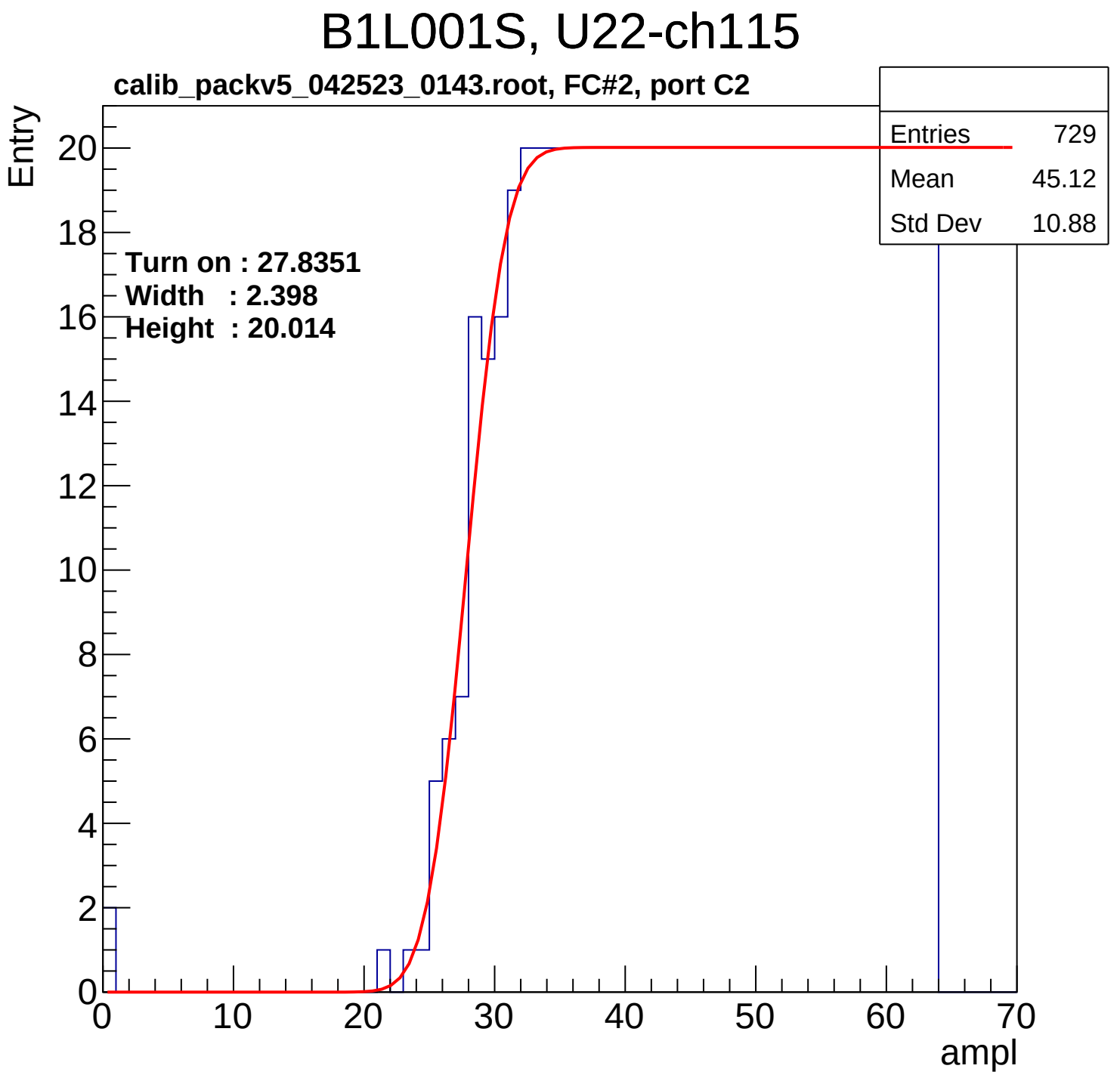
B1L001S, U22-ch115
calib_packv5_042523_0143.root, FC#2, port C2
Entries 729
Mean 45.12
Std Dev 10.88
Turn on : 27.8351
Width : 2.398
Height : 20.014
Entry
ampl
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6
8
10
12
14
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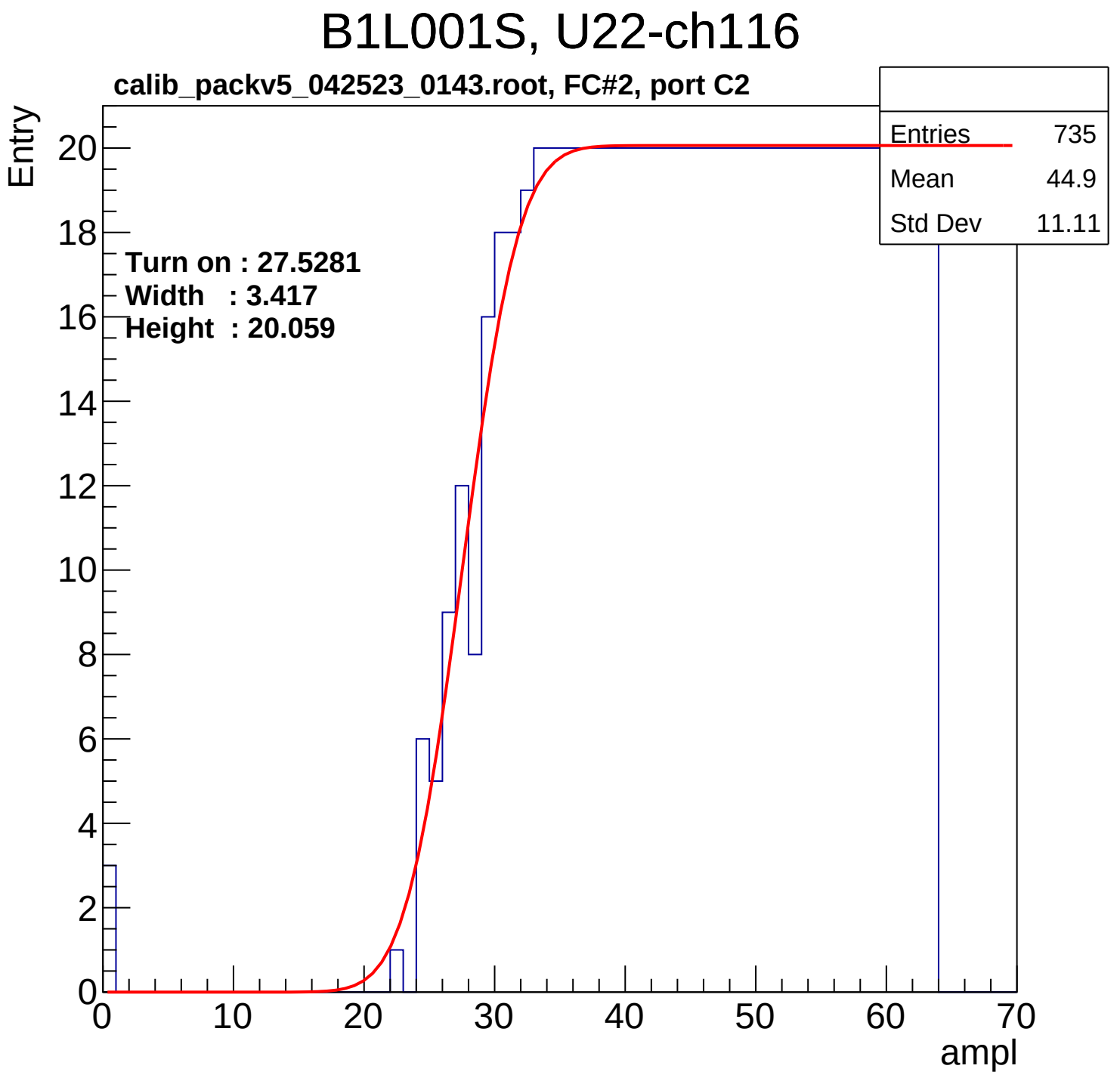
B1L001S, U22-ch116
calib_packv5_042523_0143.root, FC#2, port C2
Entries 735
Mean 44.9
Std Dev 11.11
Turn on : 27.5281
Width : 3.417
Height : 20.059
Entry
ampl
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6
8
10
12
14
16
18
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0
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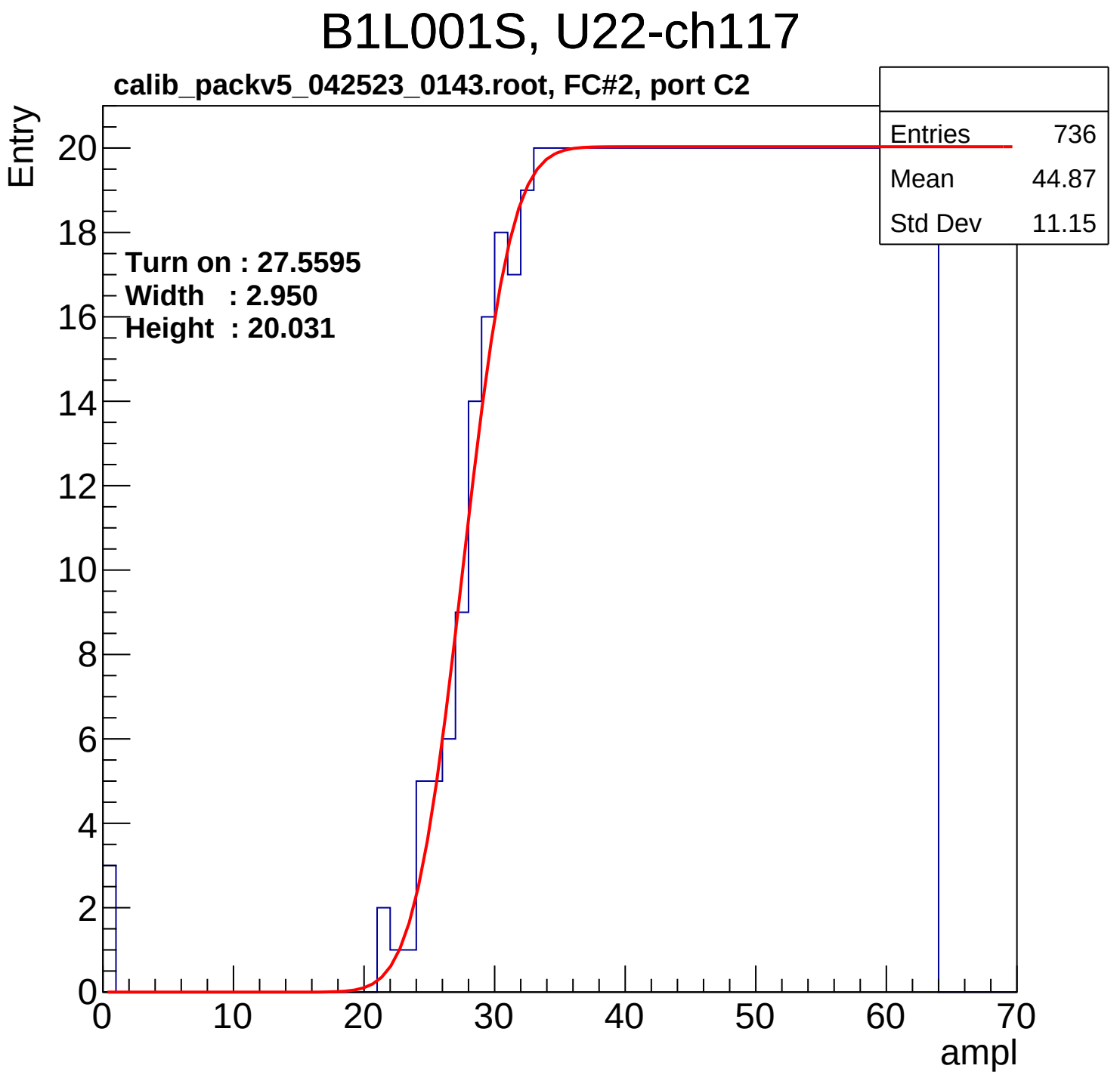
B1L001S, U22-ch117
calib_packv5_042523_0143.root, FC#2, port C2
Entries 736
Mean 44.87
Std Dev 11.15
Turn on : 27.5595
Width : 2.950
Height : 20.031
Entry
ampl
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6
8
10
12
14
16
18
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20
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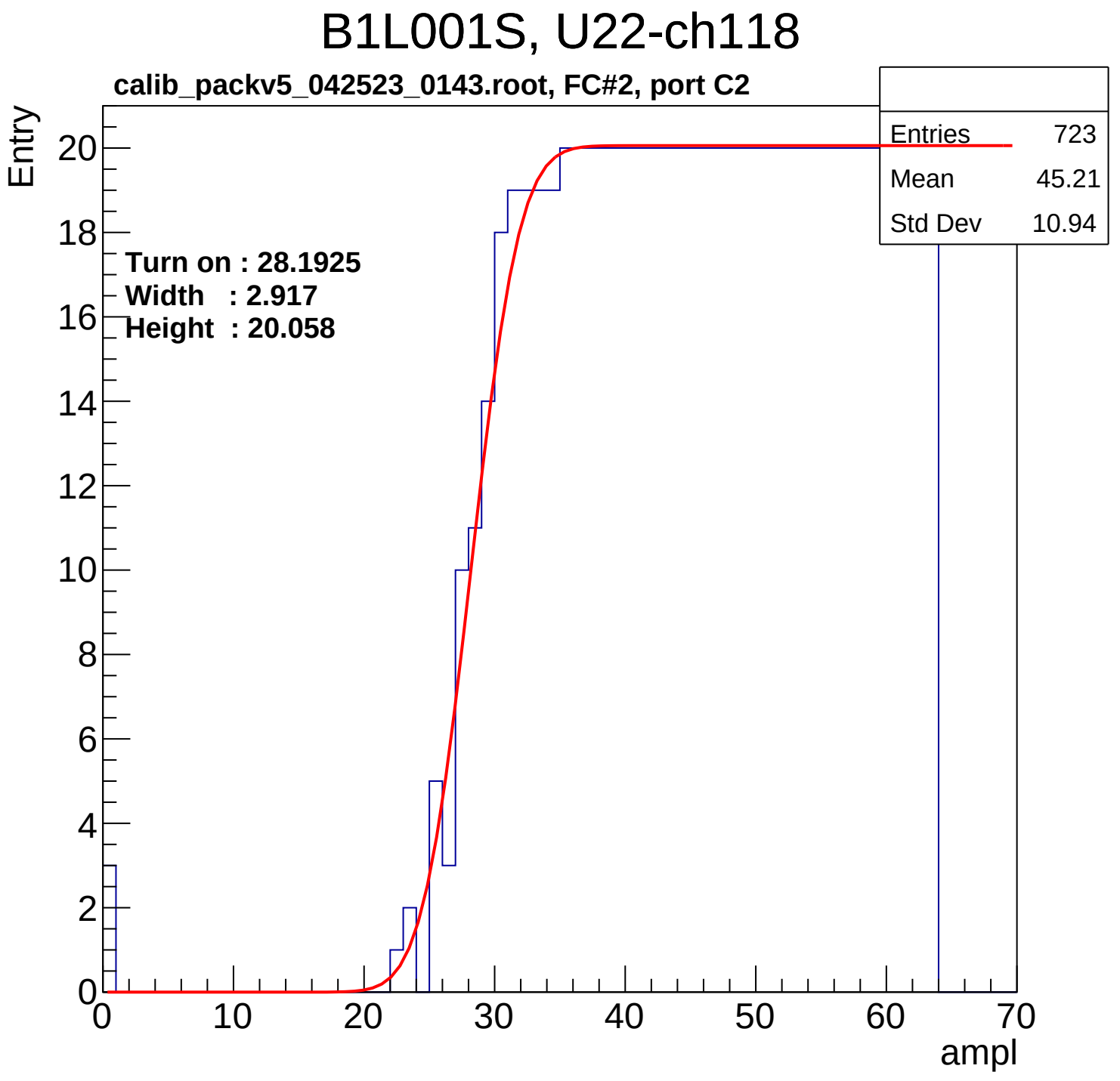
B1L001S, U22-ch118
calib_packv5_042523_0143.root, FC#2, port C2
Entries 723
Mean 45.21
Std Dev 10.94
Turn on : 28.1925
Width : 2.917
Height : 20.058
Entry
ampl
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6
8
10
12
14
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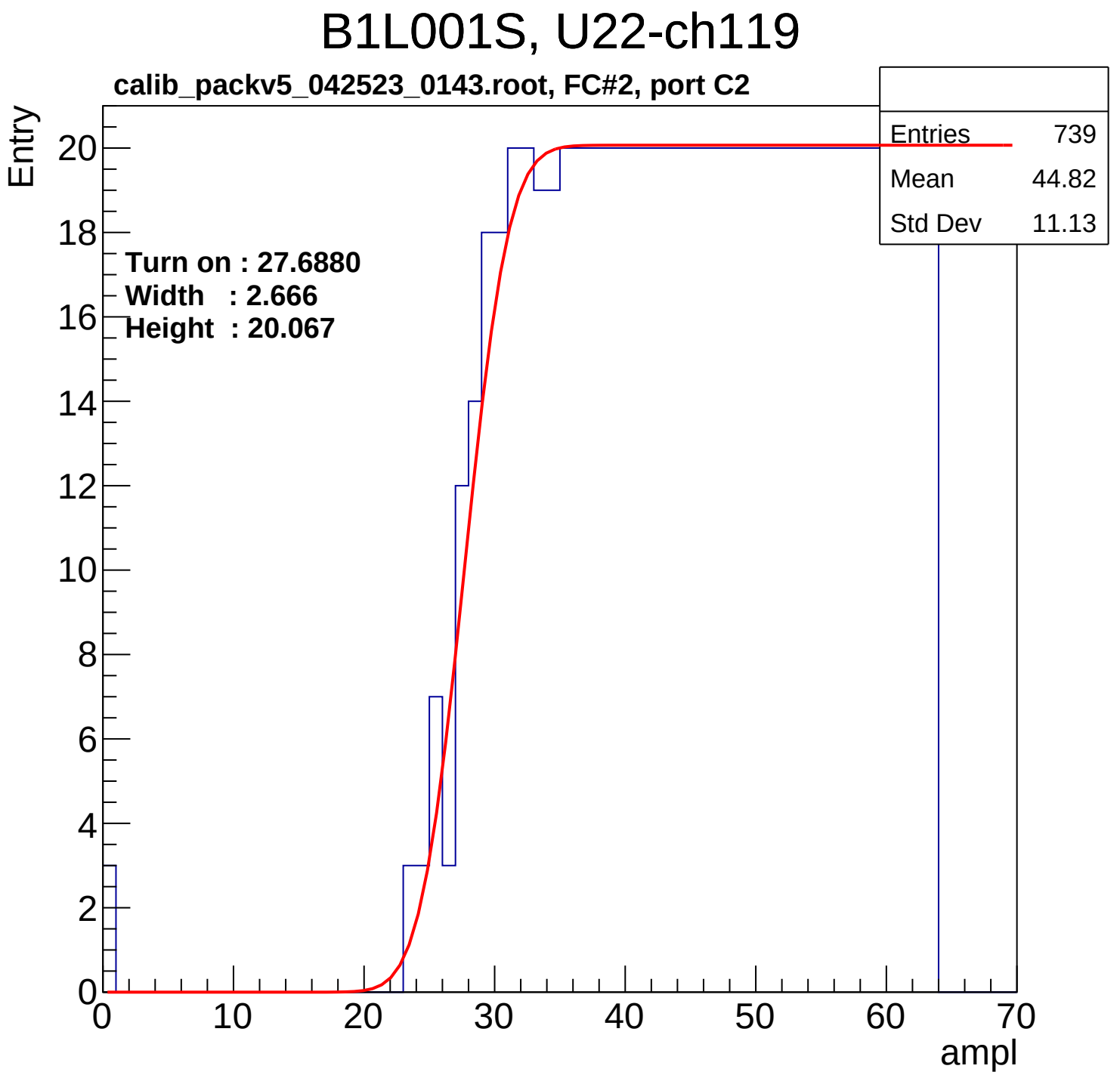
B1L001S, U22-ch119
calib_packv5_042523_0143.root, FC#2, port C2
Entries 739
Mean 44.82
Std Dev 11.13
Turn on : 27.6880
Width : 2.666
Height : 20.067
Entry
ampl
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6
8
10
12
14
16
18
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0
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20
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40
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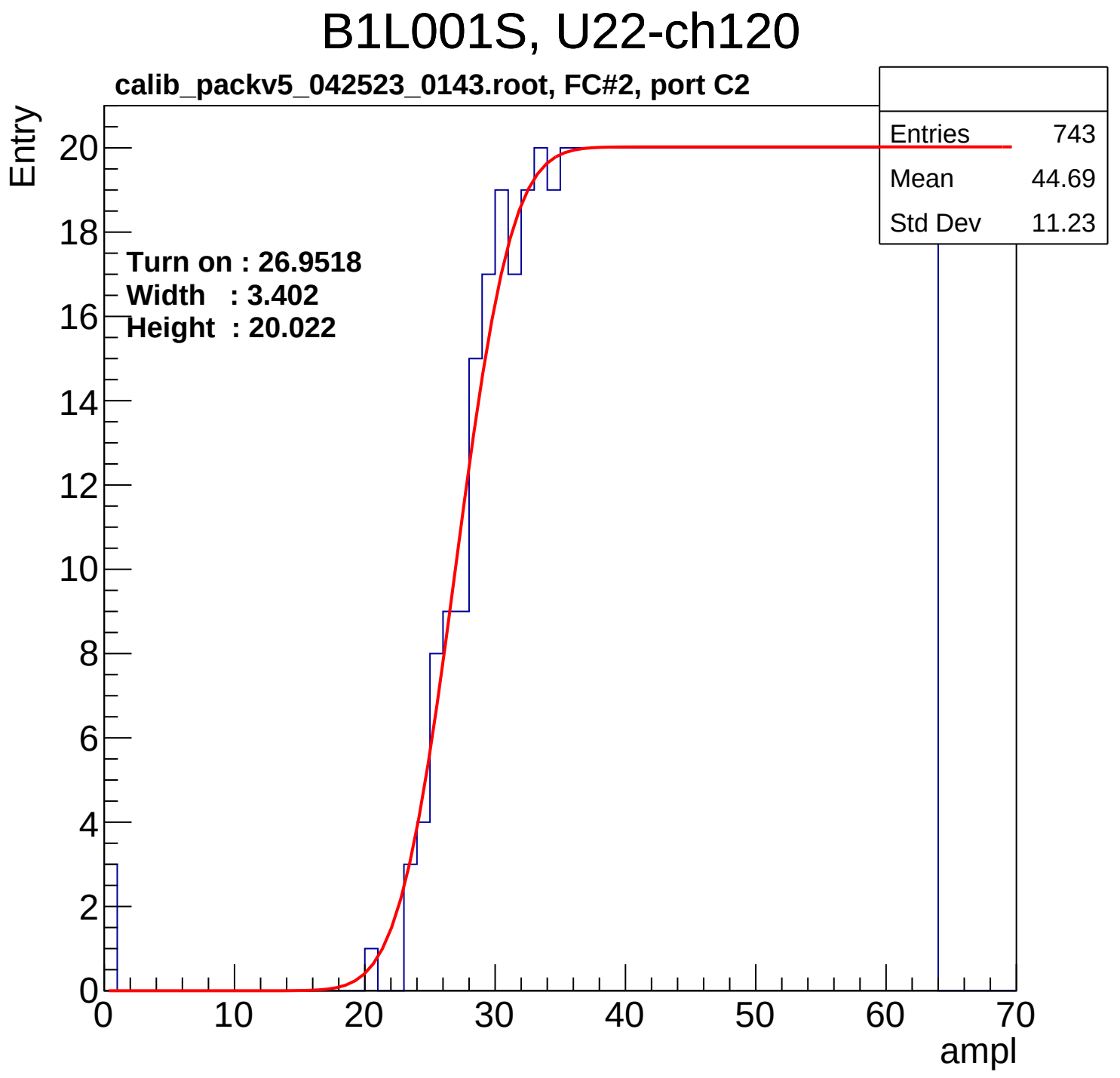
B1L001S, U22-ch120
calib_packv5_042523_0143.root, FC#2, port C2
Entries 743
Mean 44.69
Std Dev 11.23
Turn on : 26.9518
Width : 3.402
Height : 20.022
Entry
ampl
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6
8
10
12
14
16
18
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0
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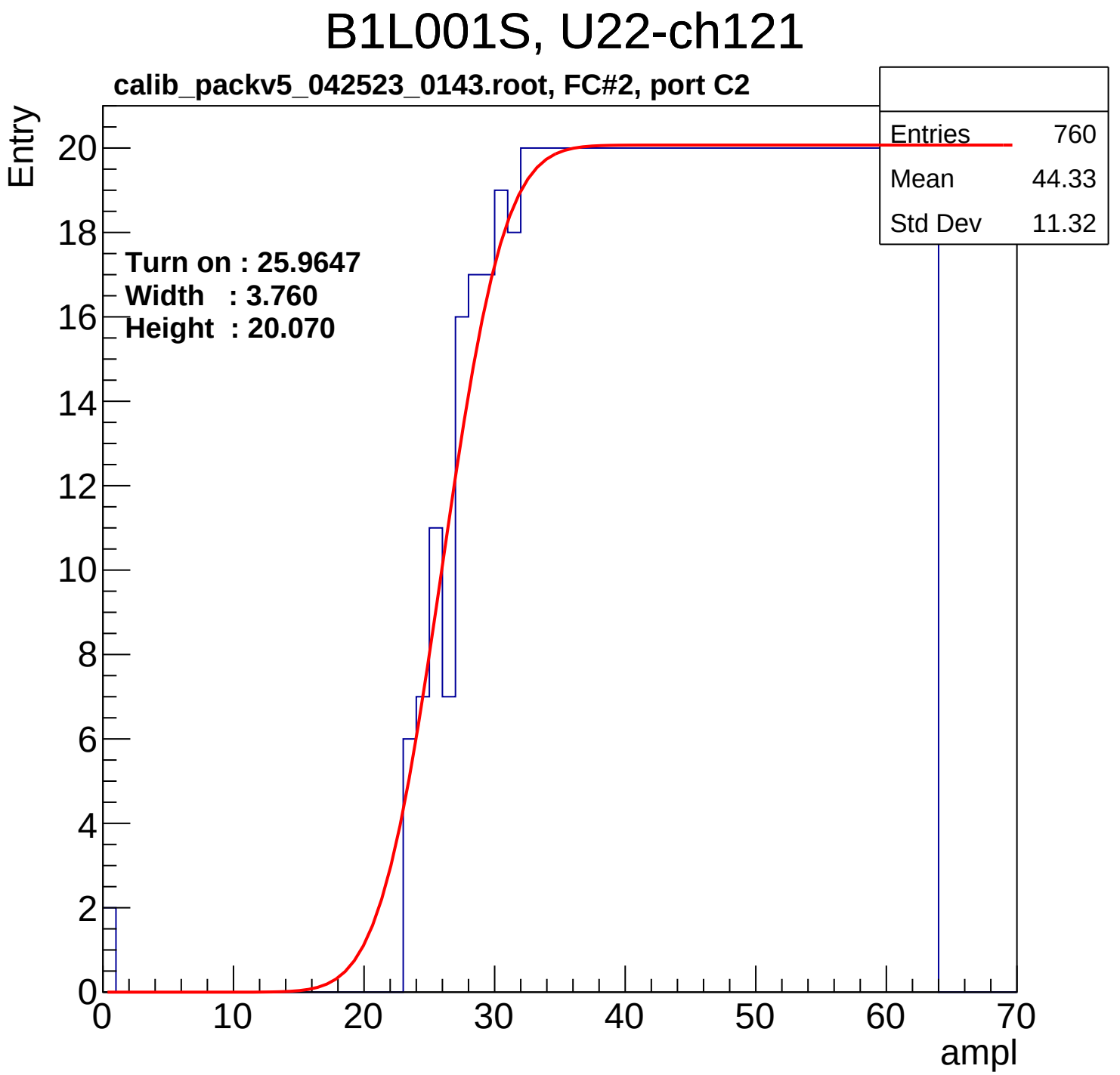
B1L001S, U22-ch121
calib_packv5_042523_0143.root, FC#2, port C2
Entries 760
Mean 44.33
Std Dev 11.32
Turn on : 25.9647
Width : 3.760
Height : 20.070
Entry
ampl
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6
8
10
12
14
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18
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0
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20
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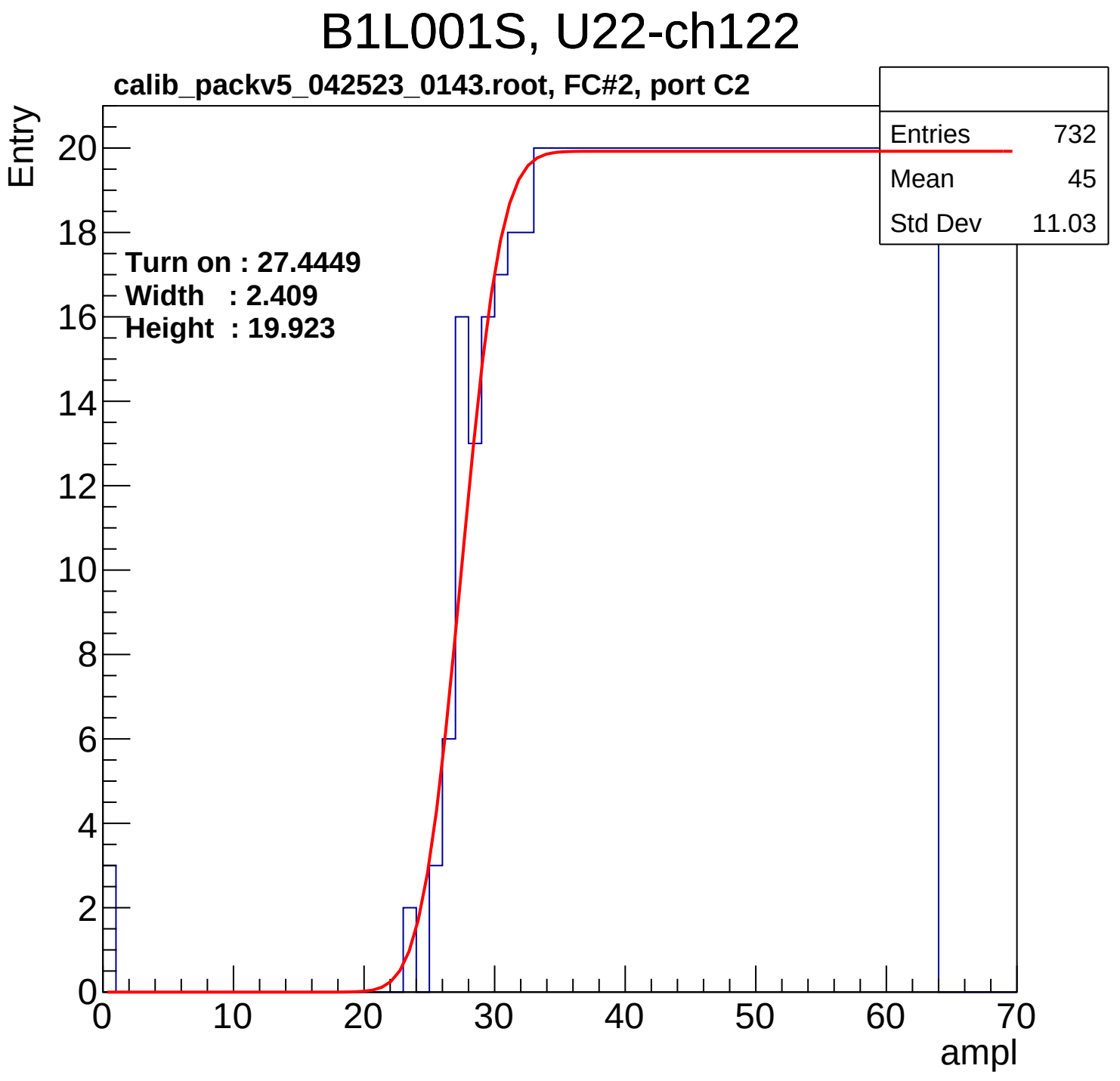
B1L001S, U22-ch122
calib_packv5_042523_0143.root, FC#2, port C2
Entries 732
Mean 45
Std Dev 11.03
Turn on : 27.4449
Width : 2.409
Height : 19.923
Entry
ampl
0
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6
8
10
12
14
16
18
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0
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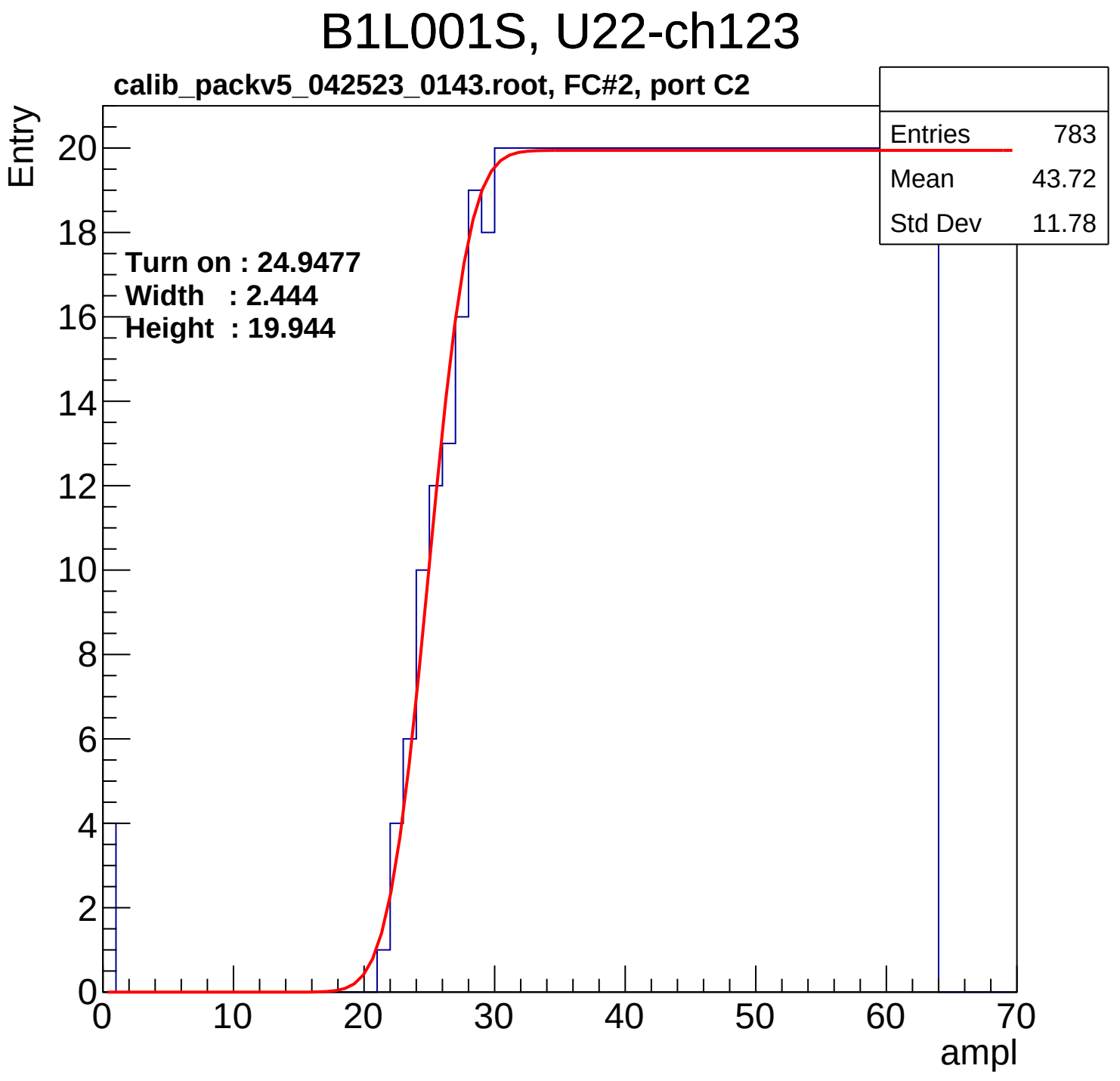
B1L001S, U22-ch123
calib_packv5_042523_0143.root, FC#2, port C2
Entries 783
Mean 43.72
Std Dev 11.78
Turn on : 24.9477
Width : 2.444
Height : 19.944
Entry
ampl
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6
8
10
12
14
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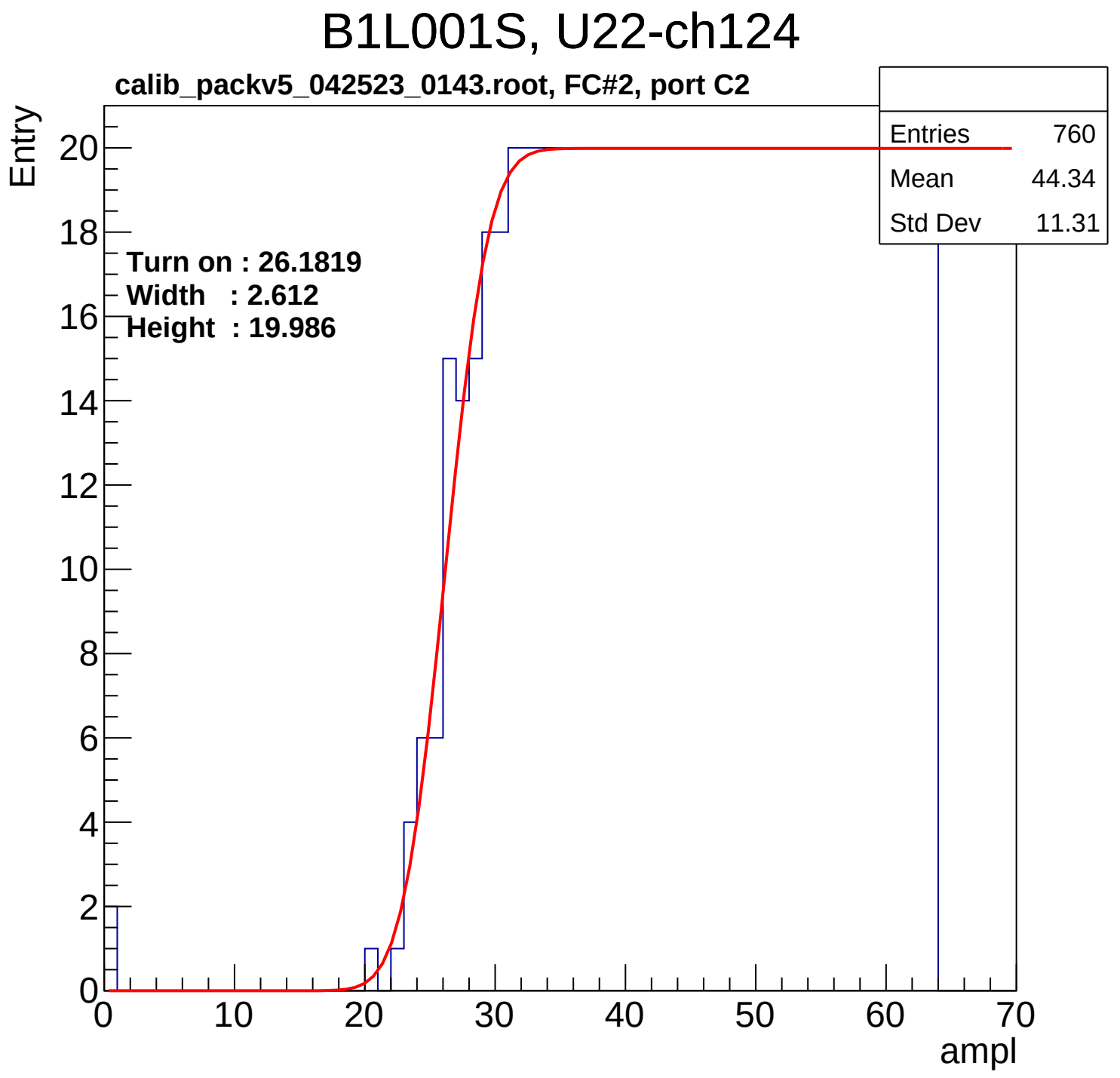
B1L001S, U22-ch124
calib_packv5_042523_0143.root, FC#2, port C2
Entries 760
Mean 44.34
Std Dev 11.31
Turn on : 26.1819
Width : 2.612
Height : 19.986
Entry
ampl
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6
8
10
12
14
16
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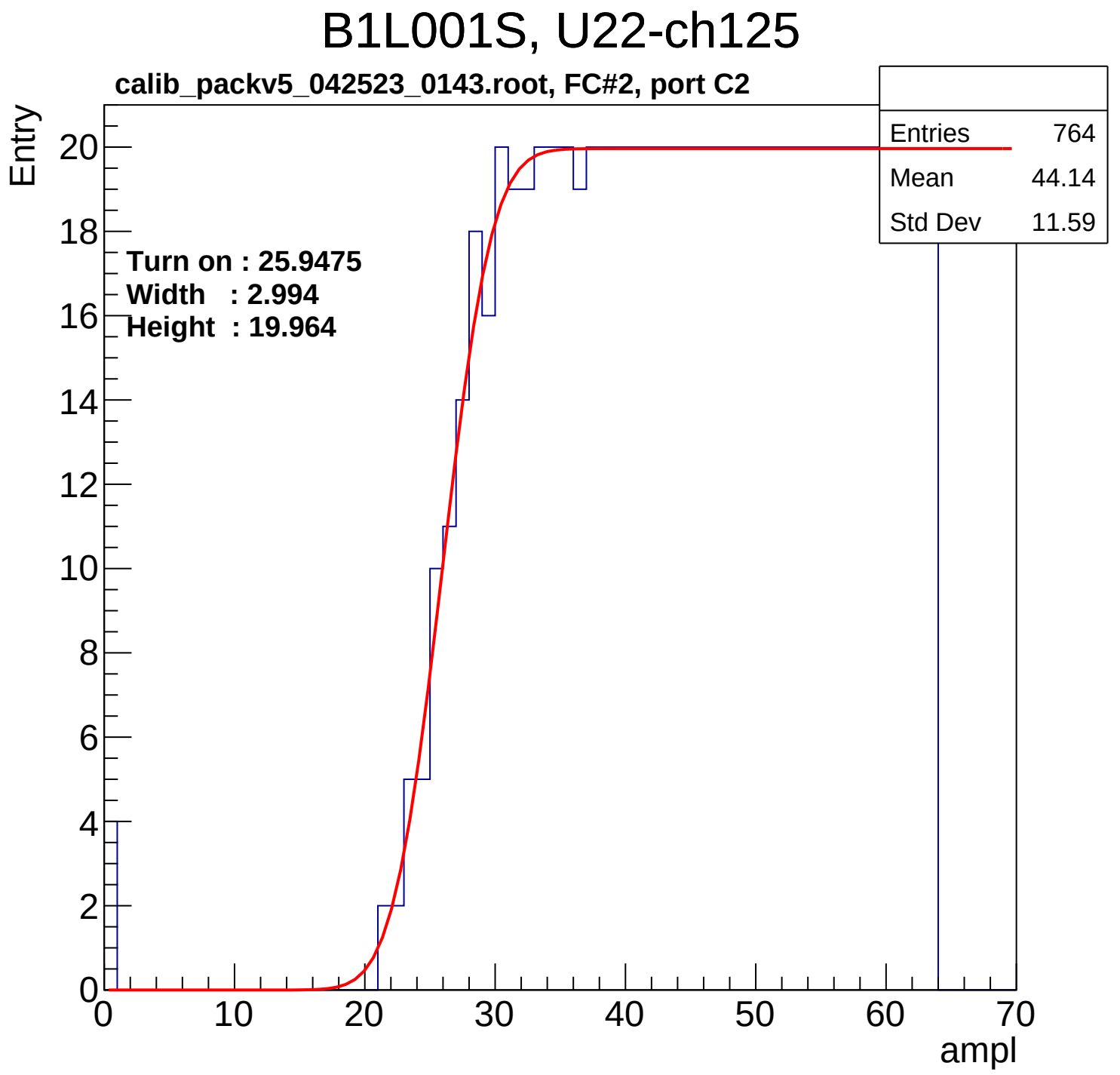
B1L001S, U22-ch125
calib_packv5_042523_0143.root, FC#2, port C2
Entries 764
Mean 44.14
Std Dev 11.59
Turn on : 25.9475
Width : 2.994
Height : 19.964
Entry
ampl
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10
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14
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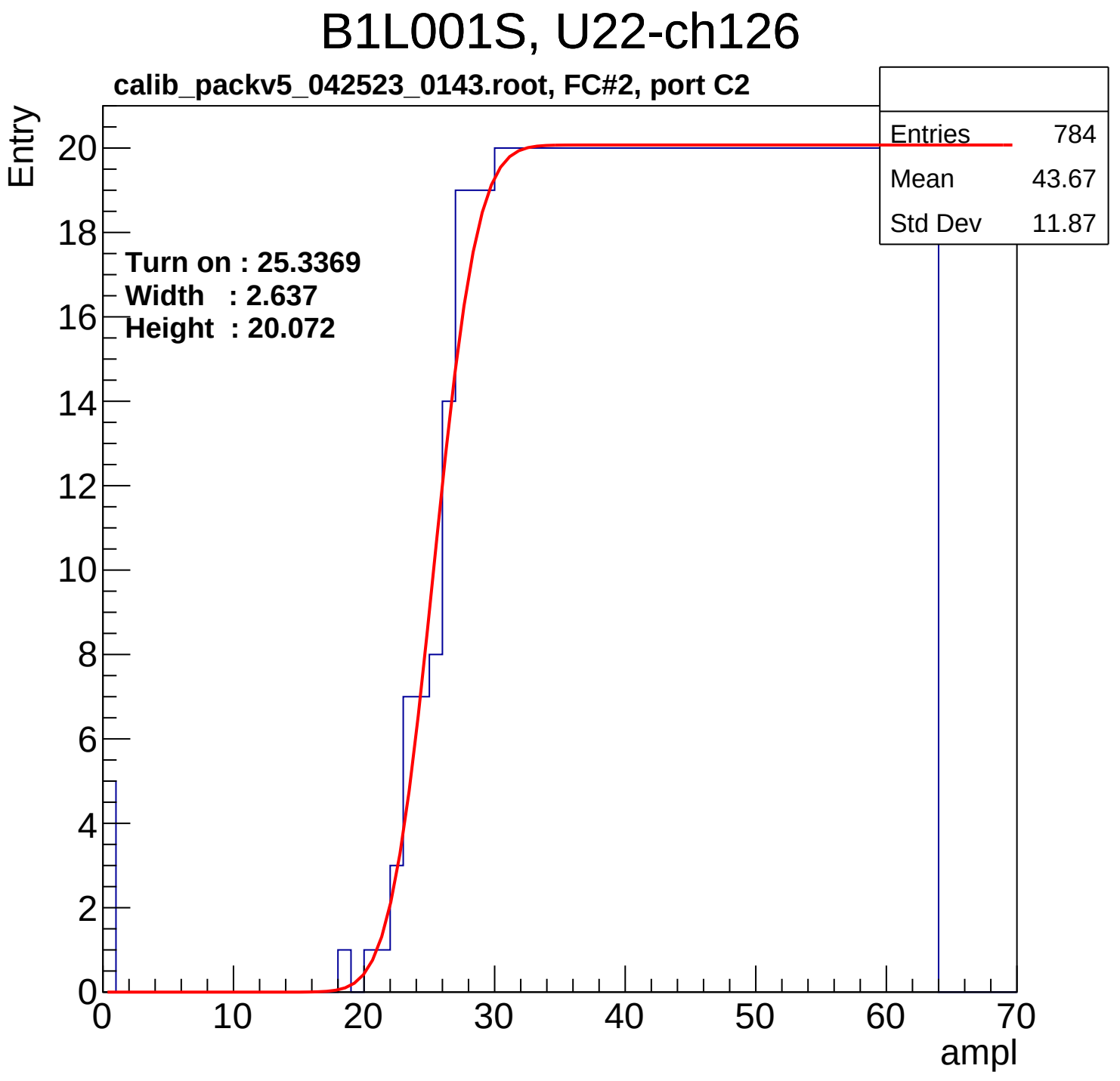
B1L001S, U22-ch126
calib_packv5_042523_0143.root, FC#2, port C2
Entries 784
Mean 43.67
Std Dev 11.87
Turn on : 25.3369
Width : 2.637
Height : 20.072
Entry
ampl
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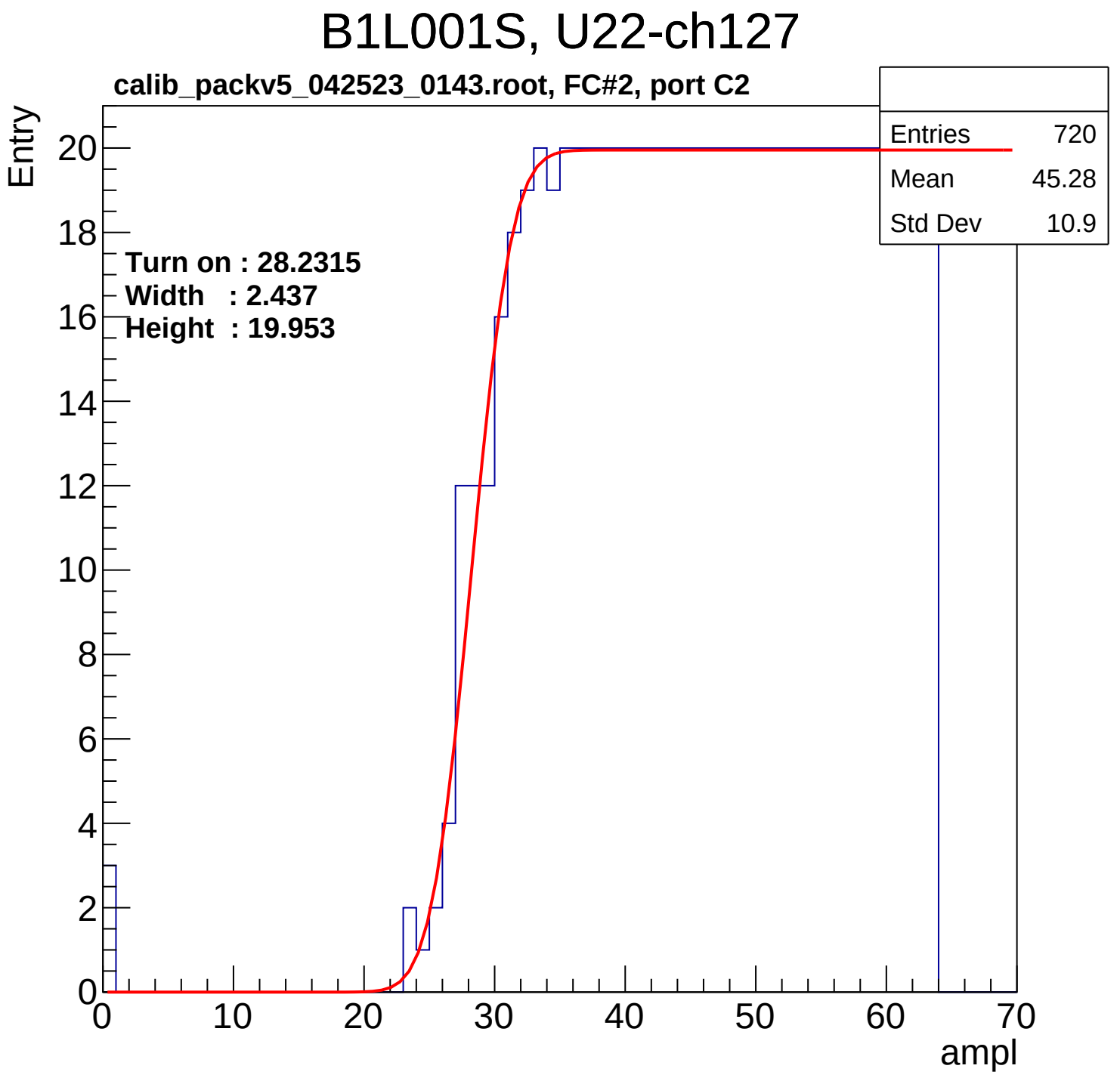
B1L001S, U22-ch127
calib_packv5_042523_0143.root, FC#2, port C2
Entries 720
Mean 45.28
Std Dev 10.9
Turn on : 28.2315
Width : 2.437
Height : 19.953
Entry
ampl
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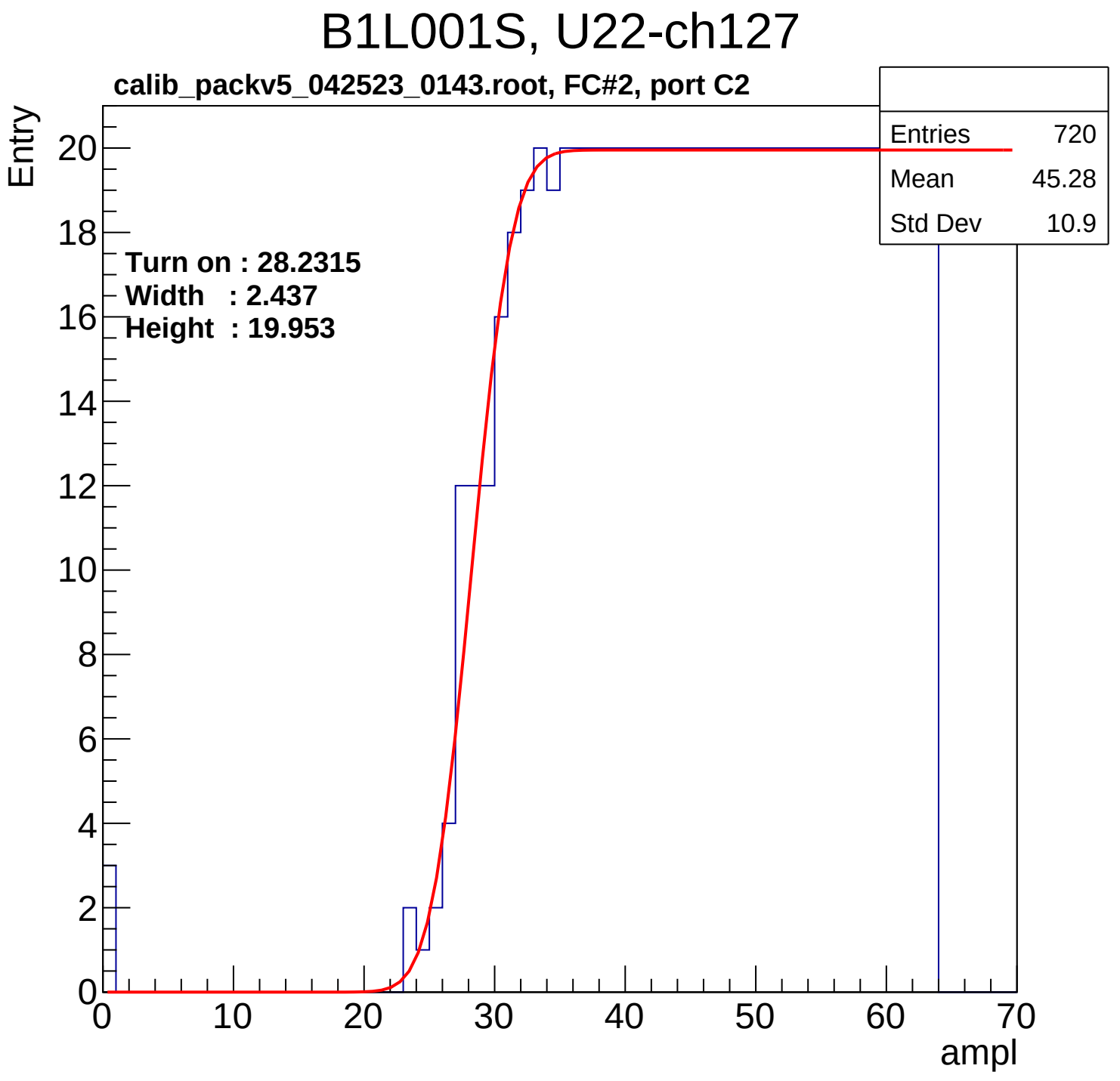
B1L001S, U22-ch127
calib_packv5_042523_0143.root, FC#2, port C2
Entries 720
Mean 45.28
Std Dev 10.9
Turn on : 28.2315
Width : 2.437
Height : 19.953
Entry
ampl
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