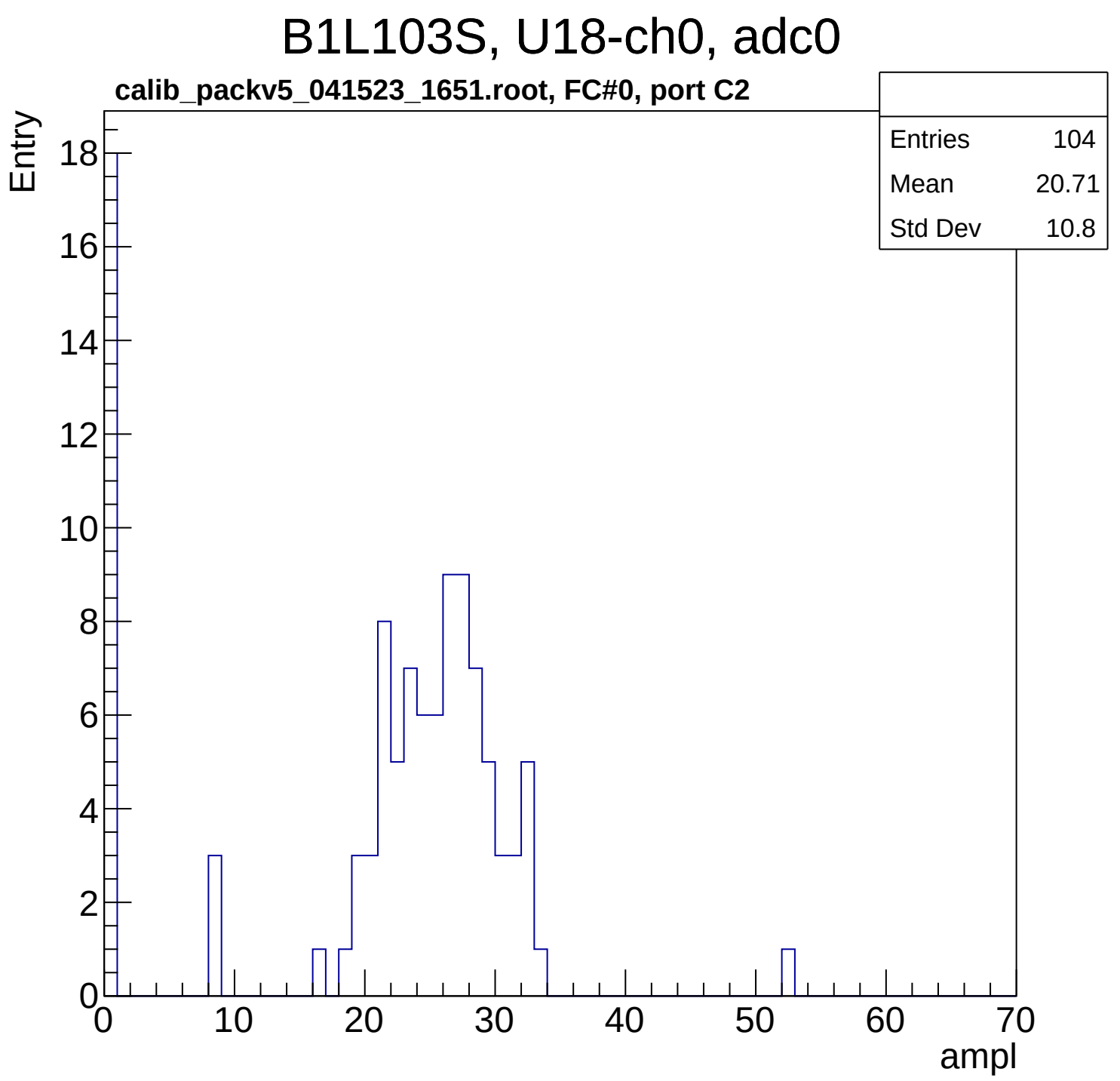
B1L103S, U18-ch0, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 104
Mean 20.71
Std Dev 10.8
Entry
ampl
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4
6
8
10
12
14
16
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0
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60
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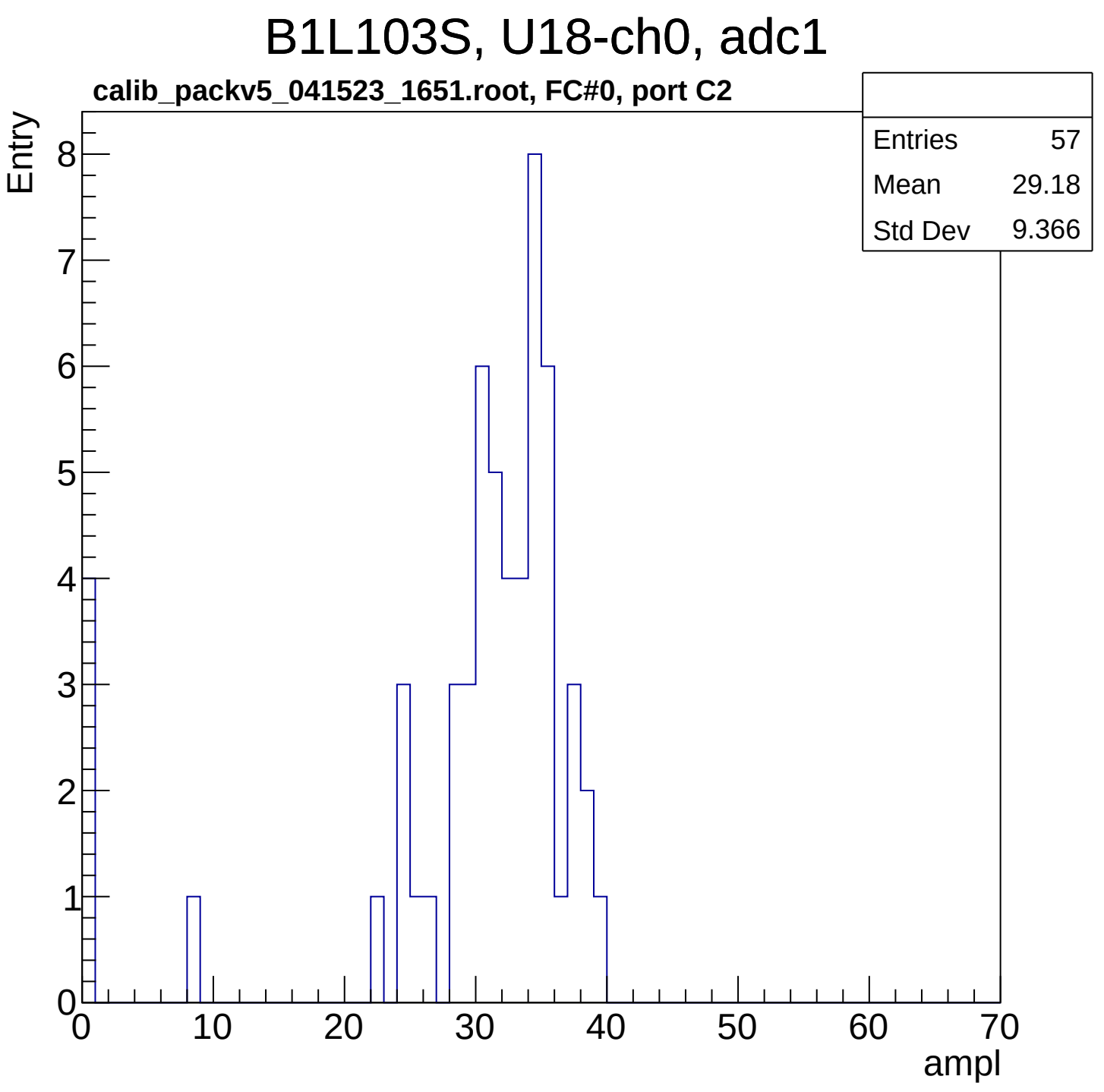
B1L103S, U18-ch0, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 29.18
Std Dev 9.366
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
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40
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60
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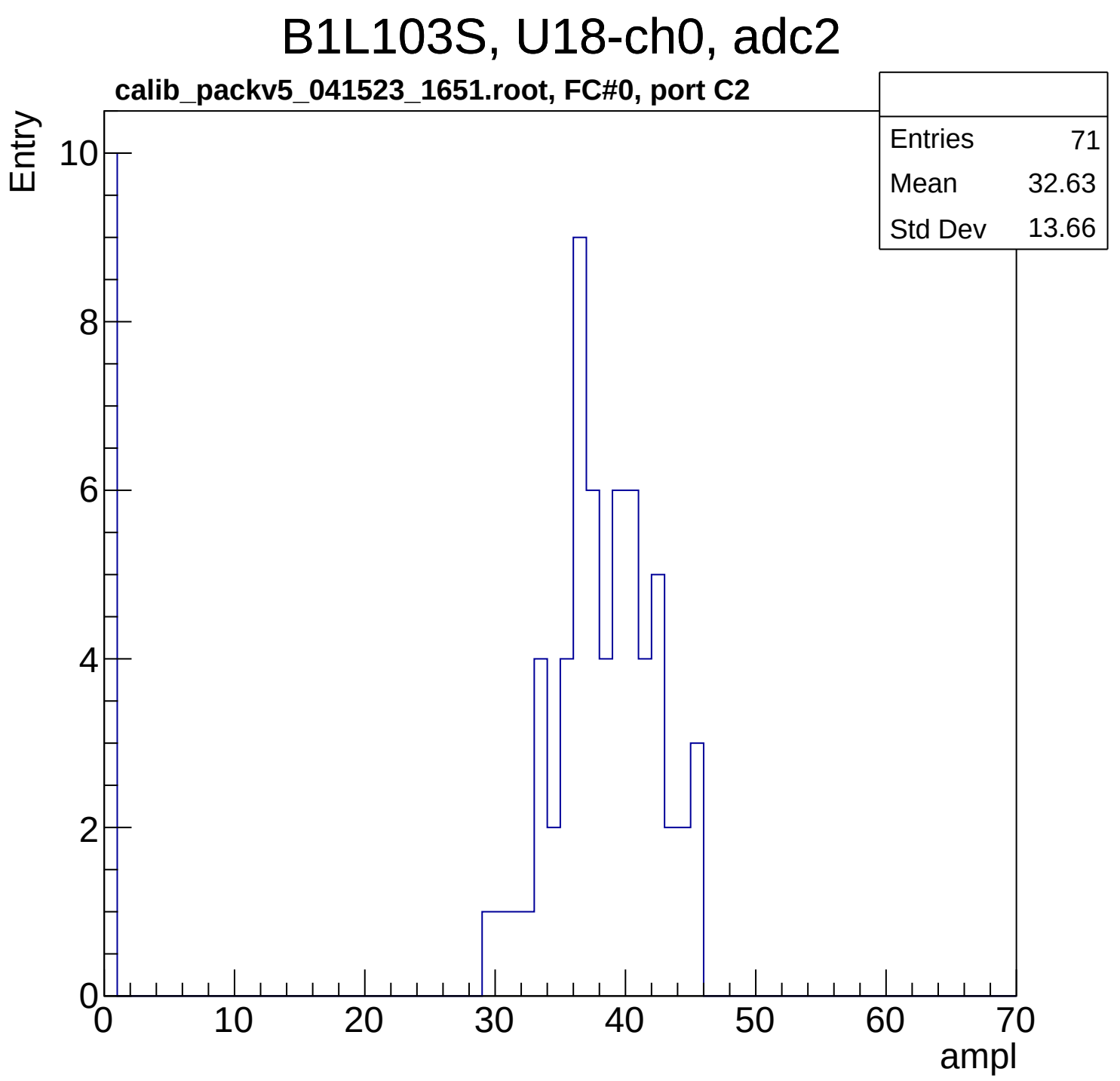
B1L103S, U18-ch0, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 32.63
Std Dev 13.66
Entry
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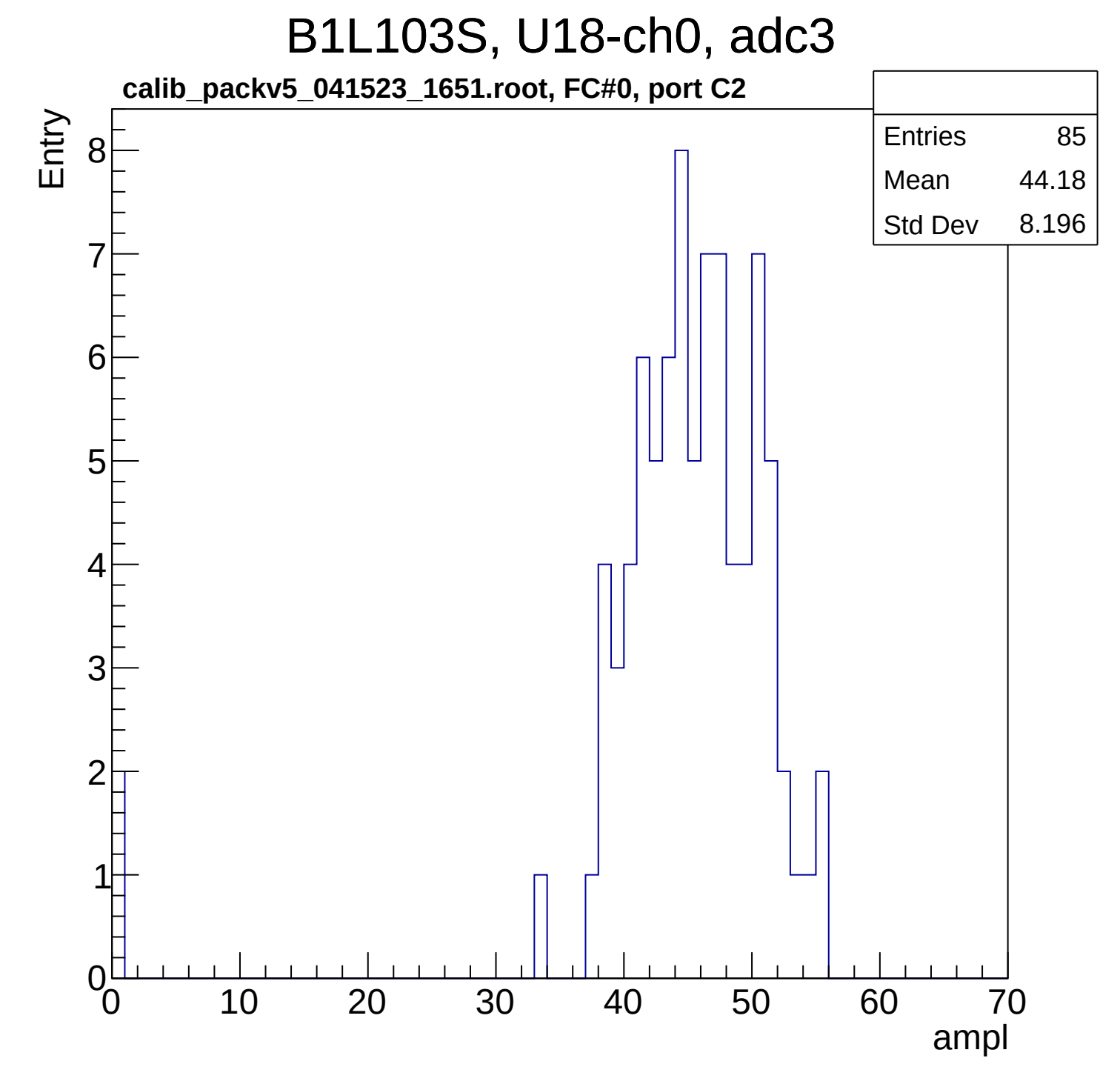
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch0, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 44.18
Std Dev 8.196
Entry
ampl
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2
3
4
5
6
7
8
0
10
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40
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60
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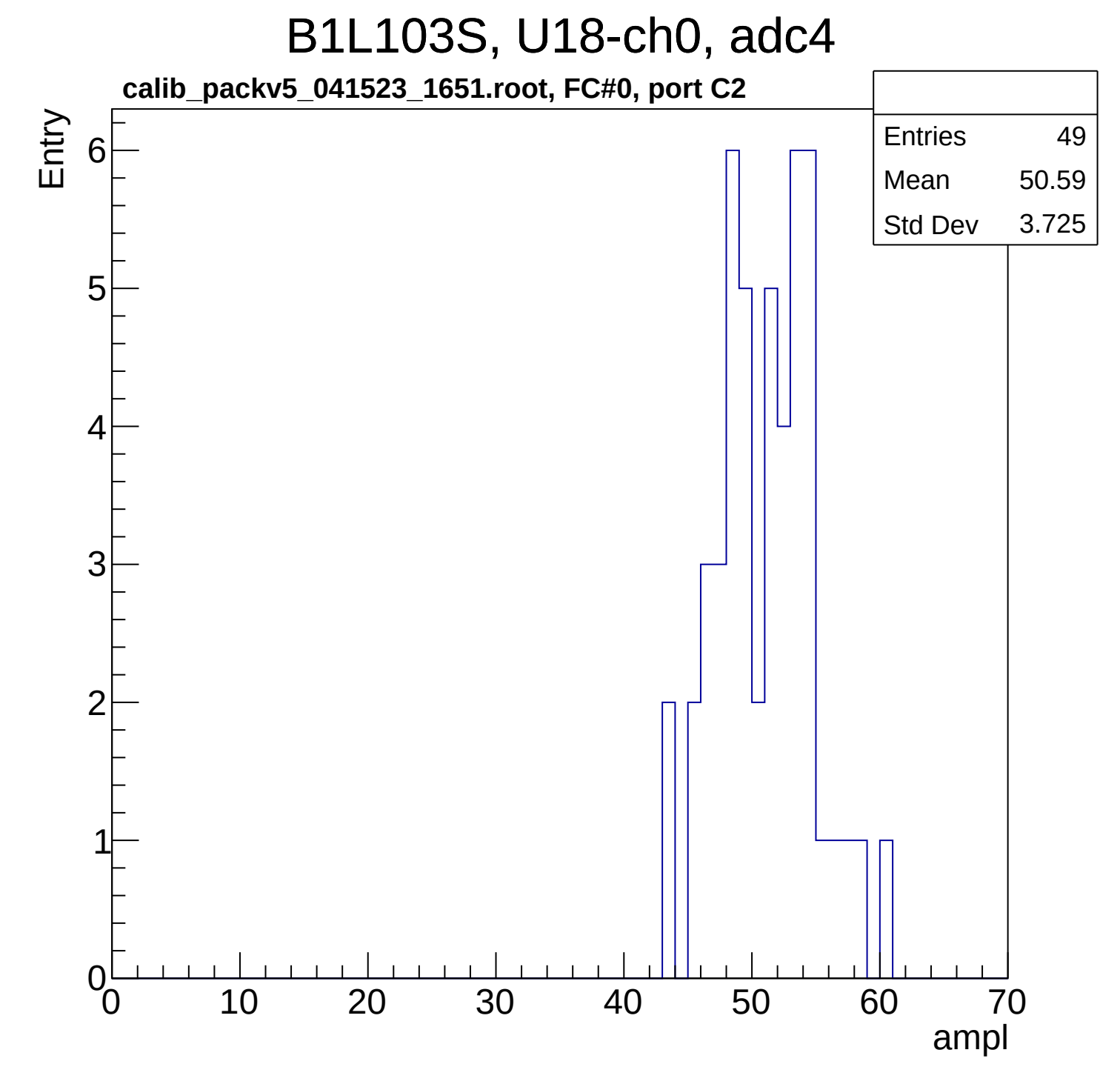
B1L103S, U18-ch0, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 50.59
Std Dev 3.725
Entry
ampl
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2
3
4
5
6
0
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20
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40
50
60
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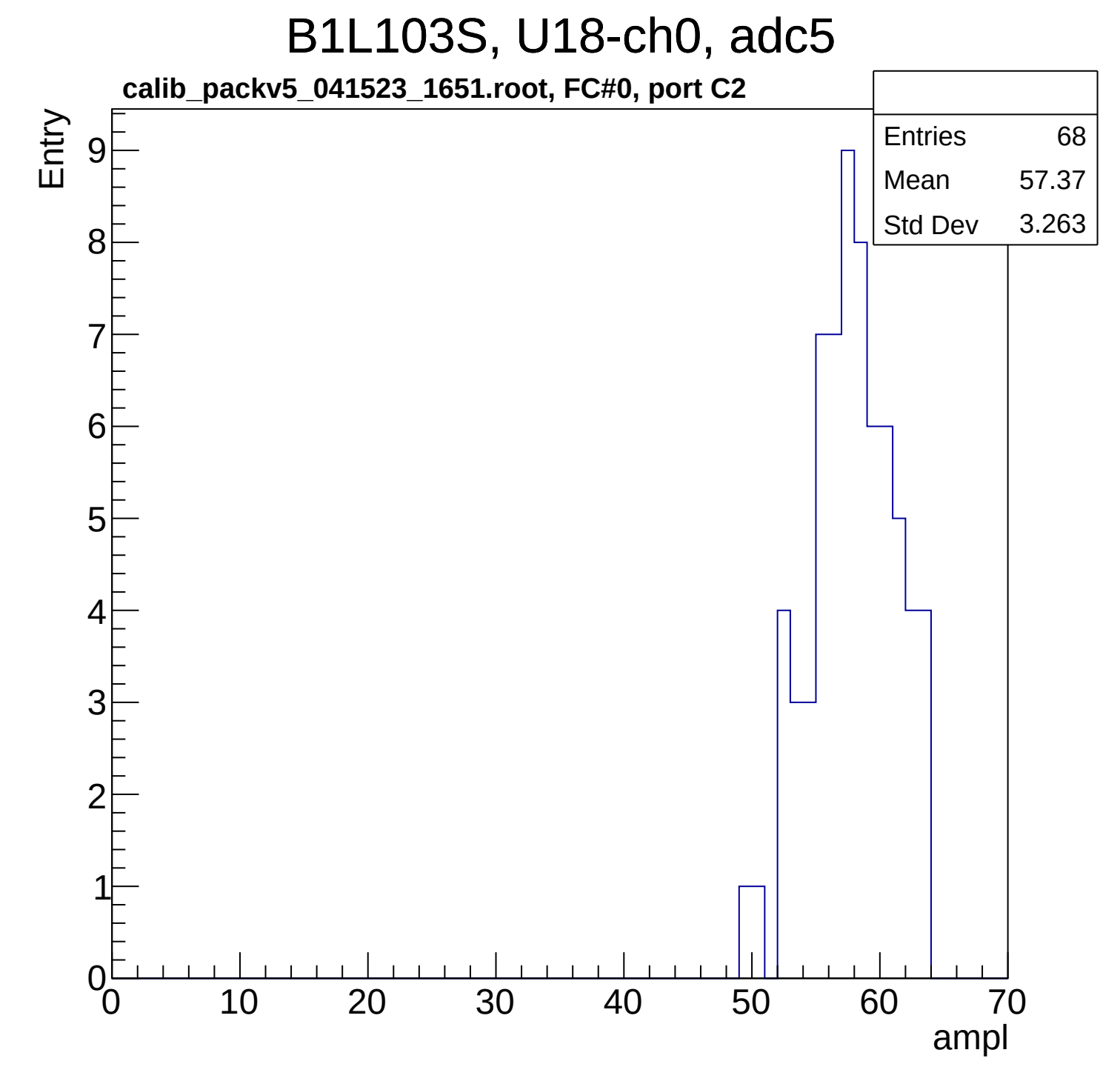
B1L103S, U18-ch0, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 57.37
Std Dev 3.263
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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40
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60
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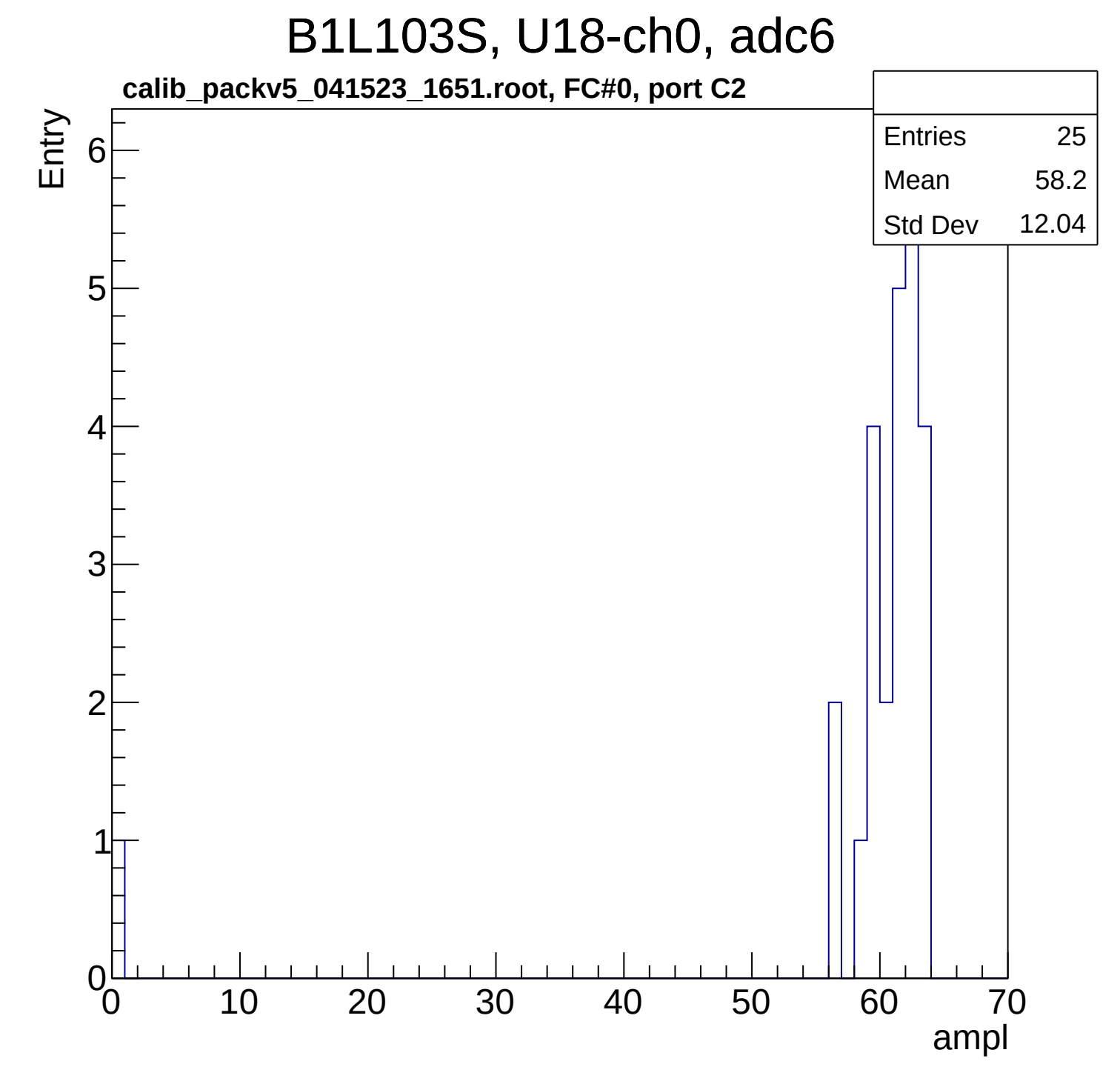
B1L103S, U18-ch0, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 25
Mean 58.2
Std Dev 12.04
Entry
ampl
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1
2
3
4
5
6
0
10
20
30
40
50
60
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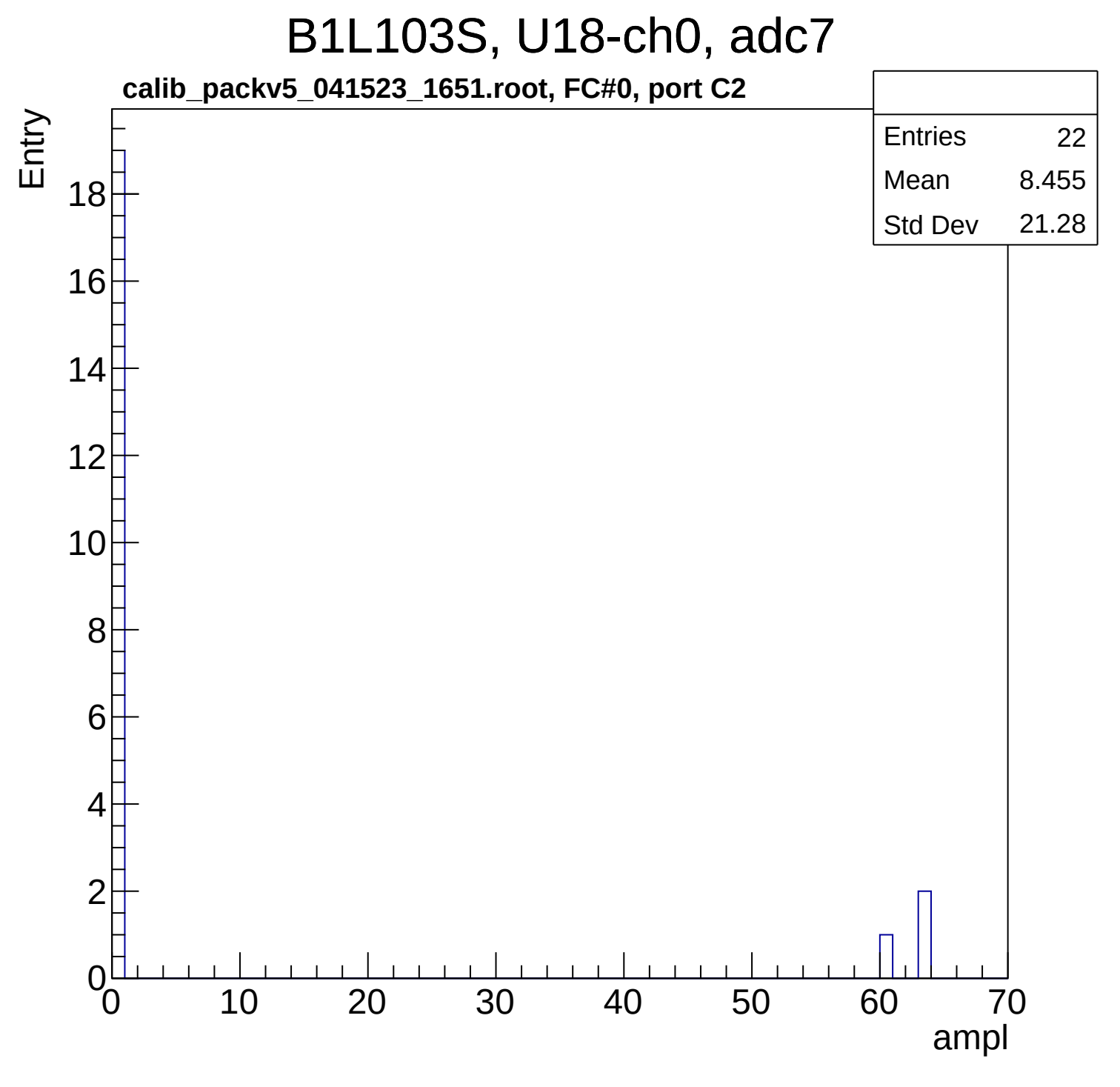
B1L103S, U18-ch0, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 8.455
Std Dev 21.28
Entry
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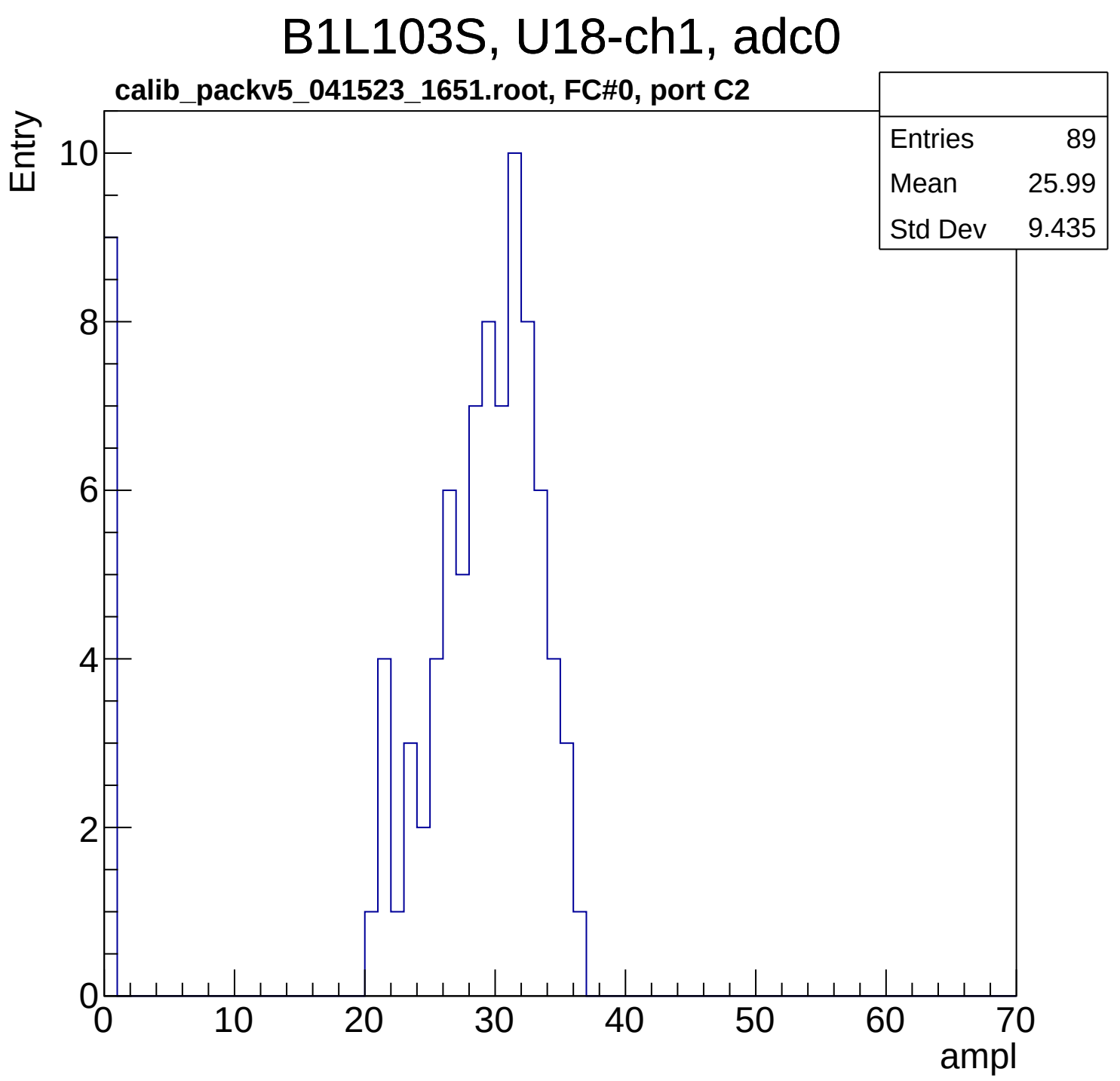
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch1, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 89
Mean 25.99
Std Dev 9.435
Entry
ampl
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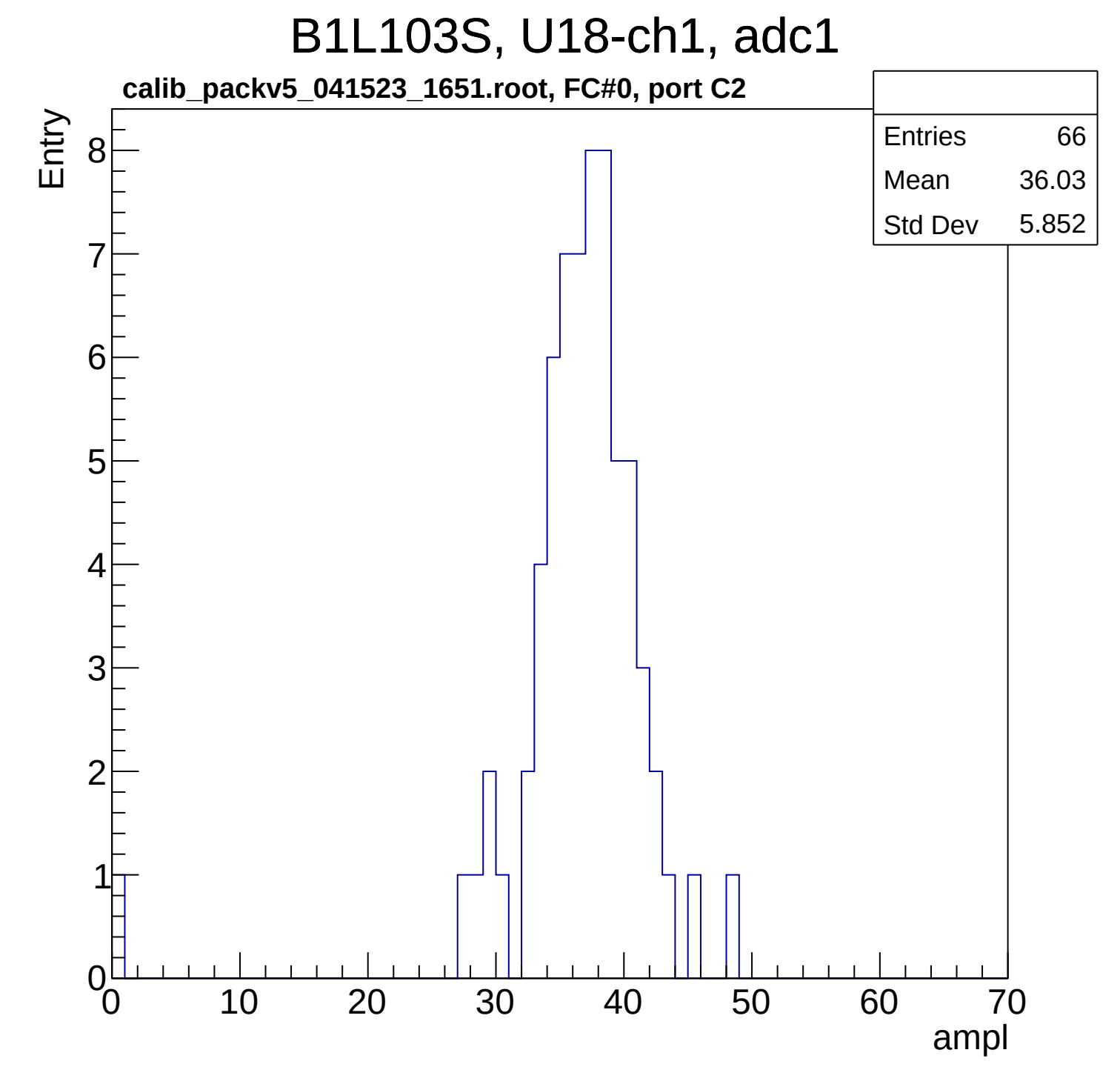
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U18-ch1, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 36.03
Std Dev 5.852
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
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60
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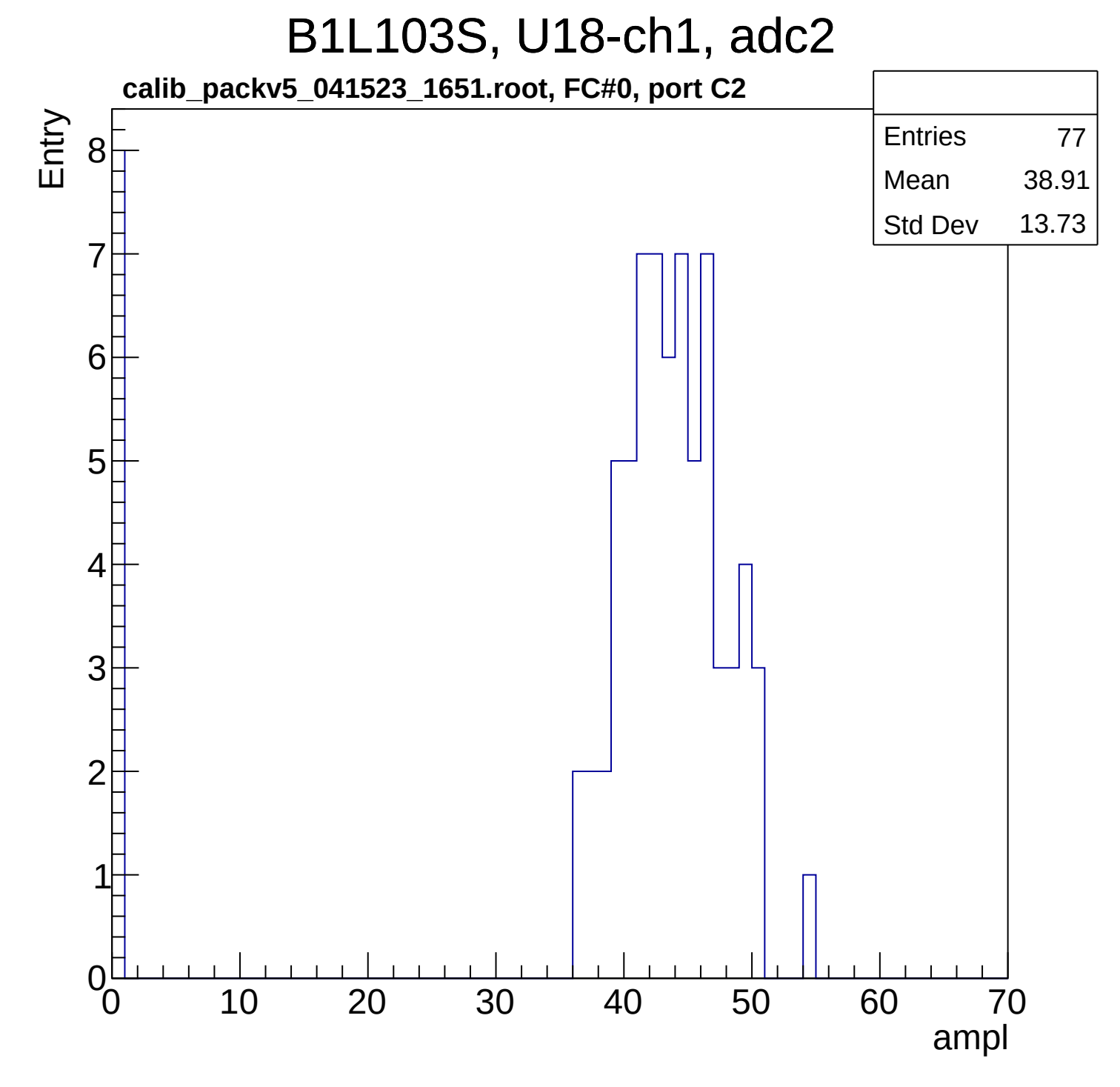
B1L103S, U18-ch1, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 38.91
Std Dev 13.73
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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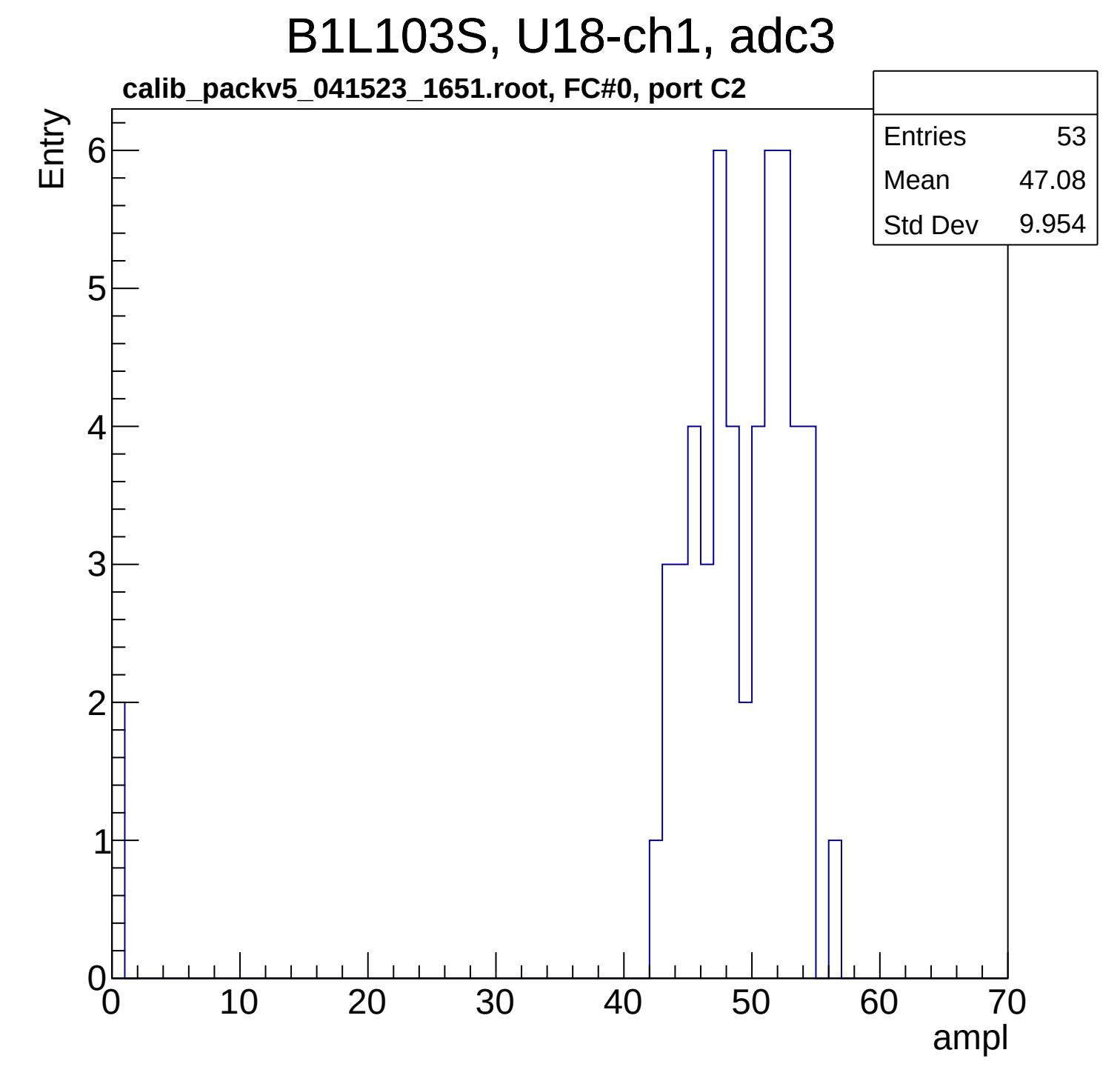
B1L103S, U18-ch1, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 47.08
Std Dev 9.954
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
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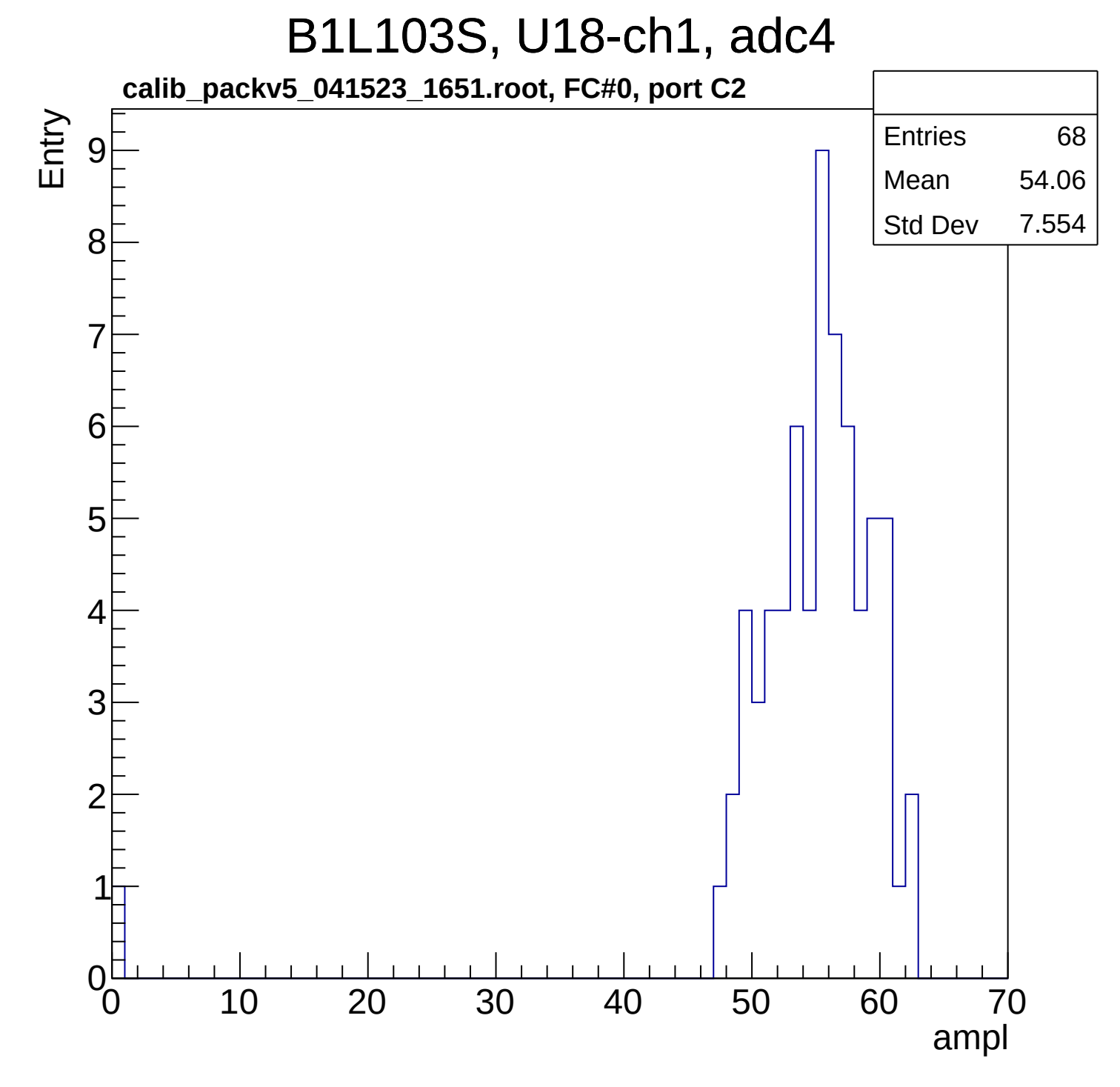
B1L103S, U18-ch1, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 54.06
Std Dev 7.554
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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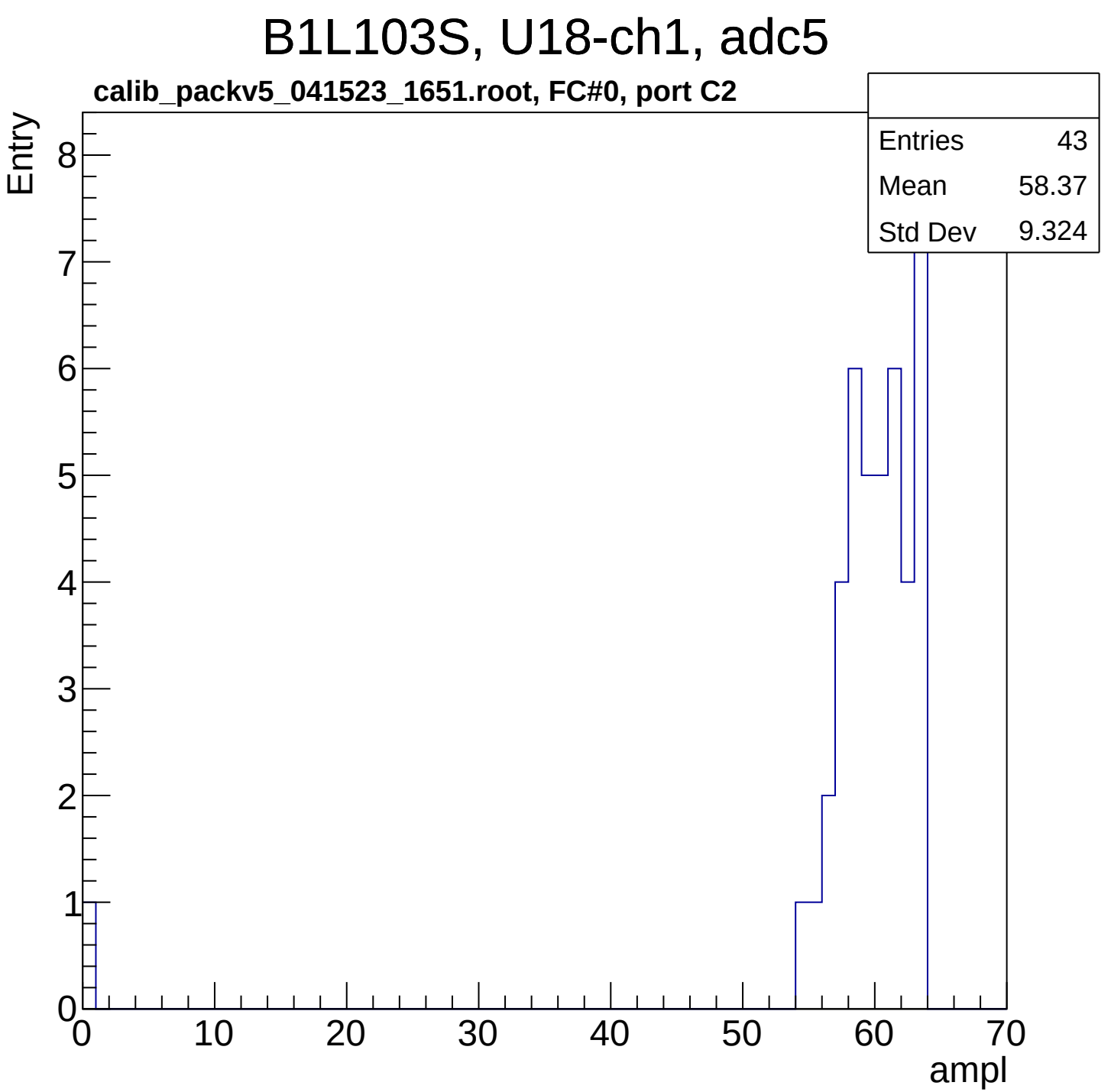
B1L103S, U18-ch1, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 43
Mean 58.37
Std Dev 9.324
Entry
ampl
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2
3
4
5
6
7
8
0
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20
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40
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60
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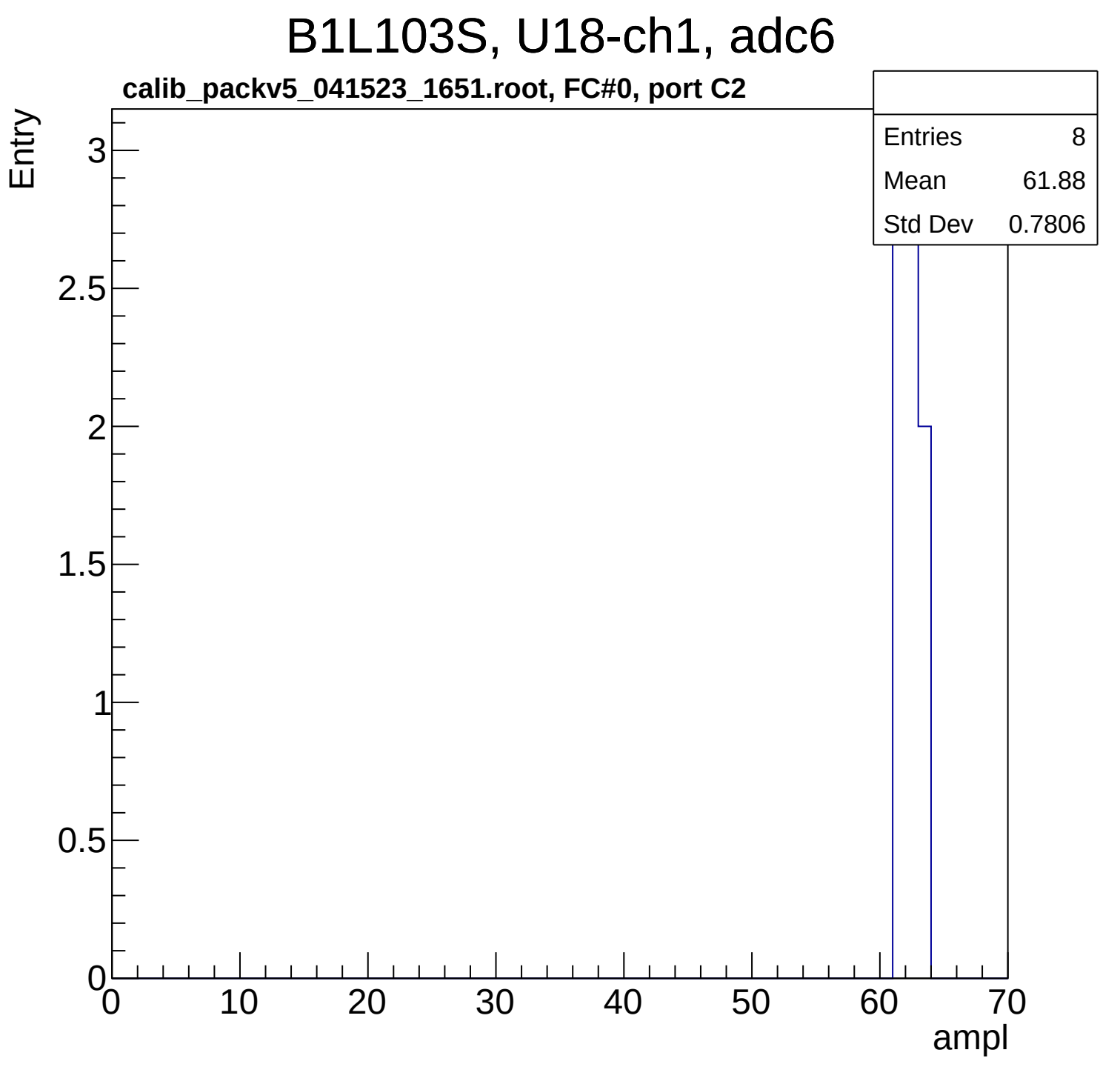
B1L103S, U18-ch1, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 61.88
Std Dev 0.7806
Entry
ampl
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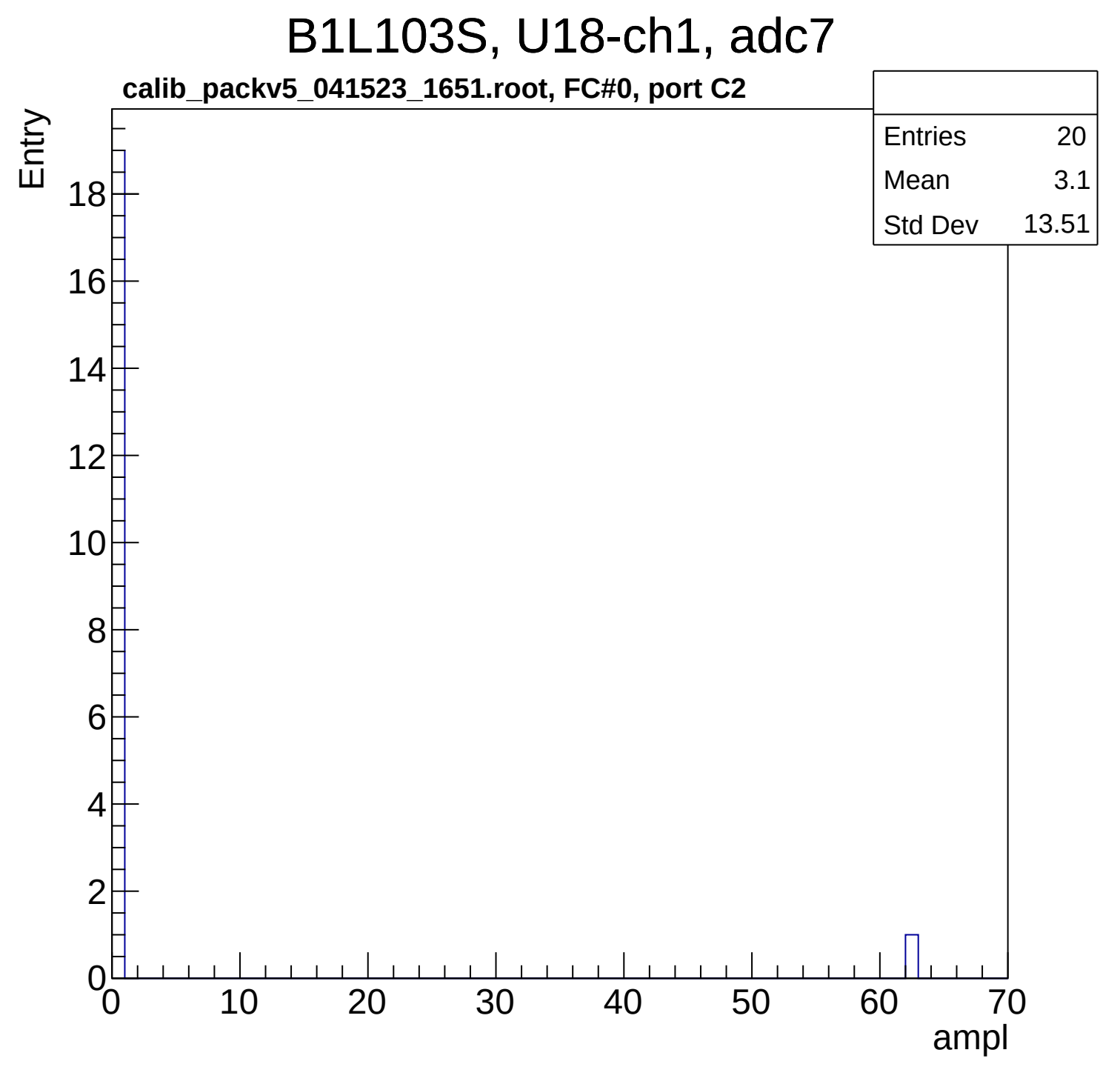
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U18-ch1, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.1
Std Dev 13.51
Entry
ampl
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4
6
8
10
12
14
16
18
0
10
20
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40
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60
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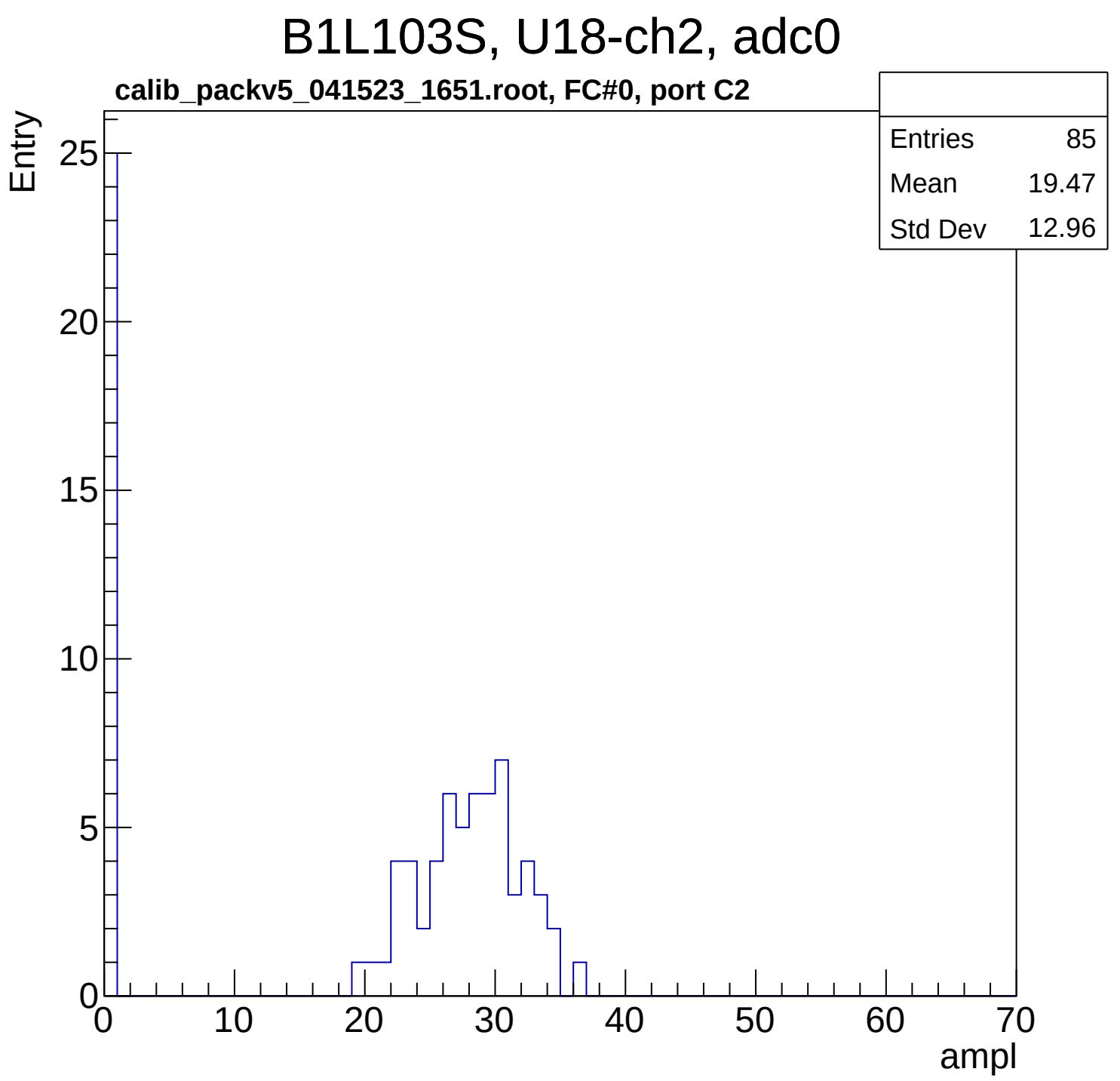
B1L103S, U18-ch2, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 19.47
Std Dev 12.96
Entry
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15
20
25
0
10
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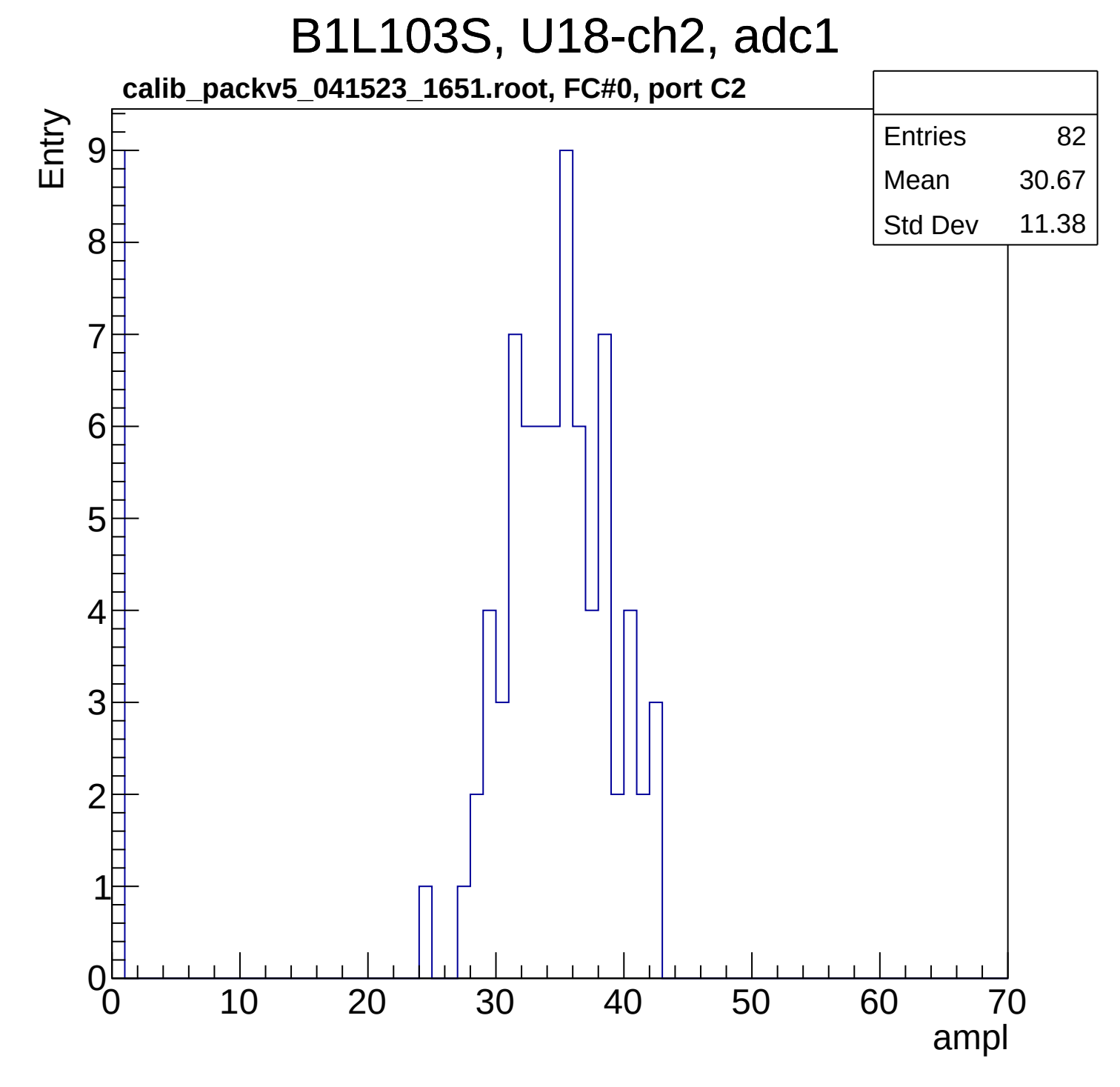
40
50
60
70
ampl


B1L103S, U18-ch2, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 30.67
Std Dev 11.38
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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50
60
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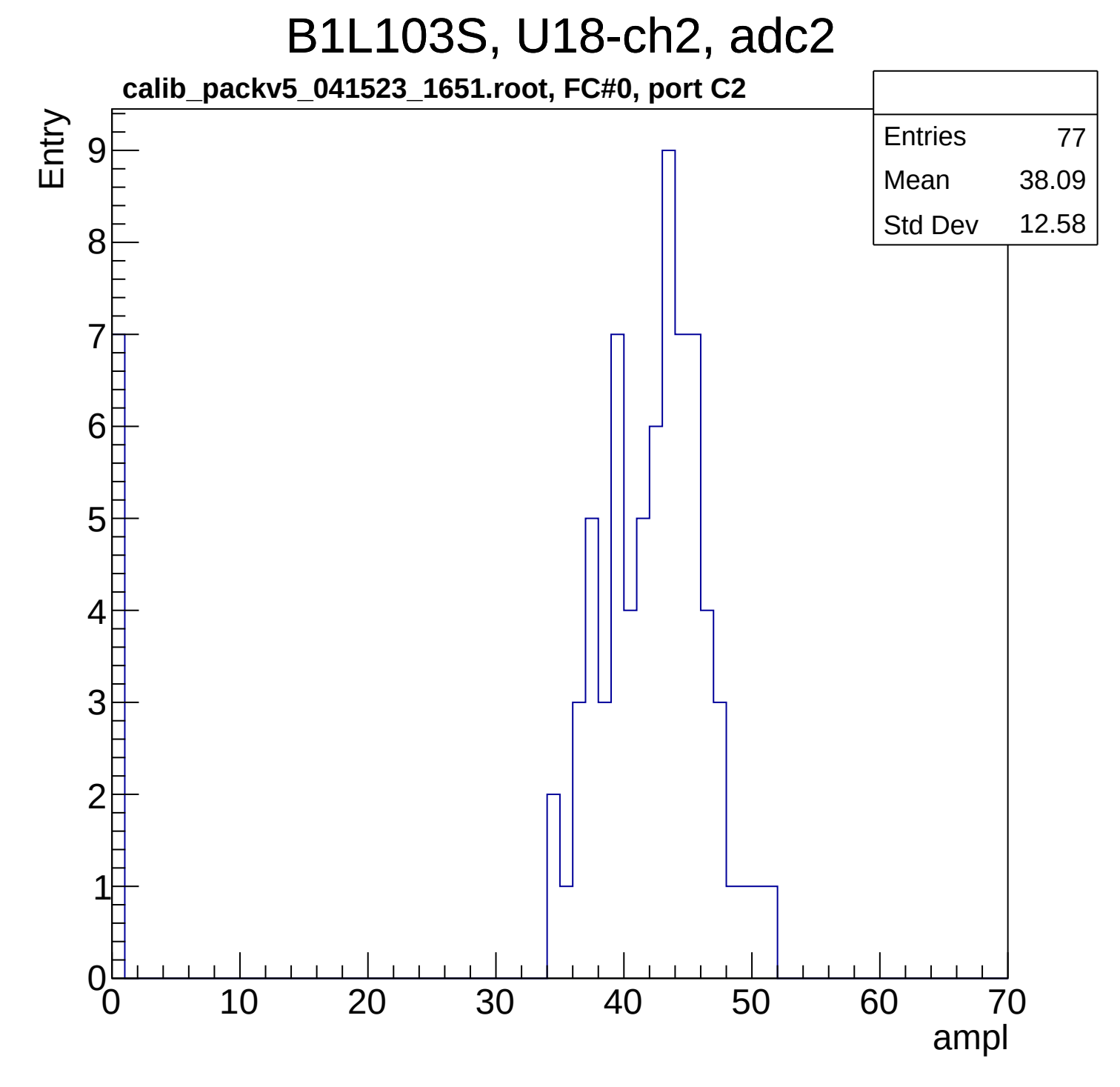
B1L103S, U18-ch2, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 38.09
Std Dev 12.58
Entry
ampl
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2
3
4
5
6
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8
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0
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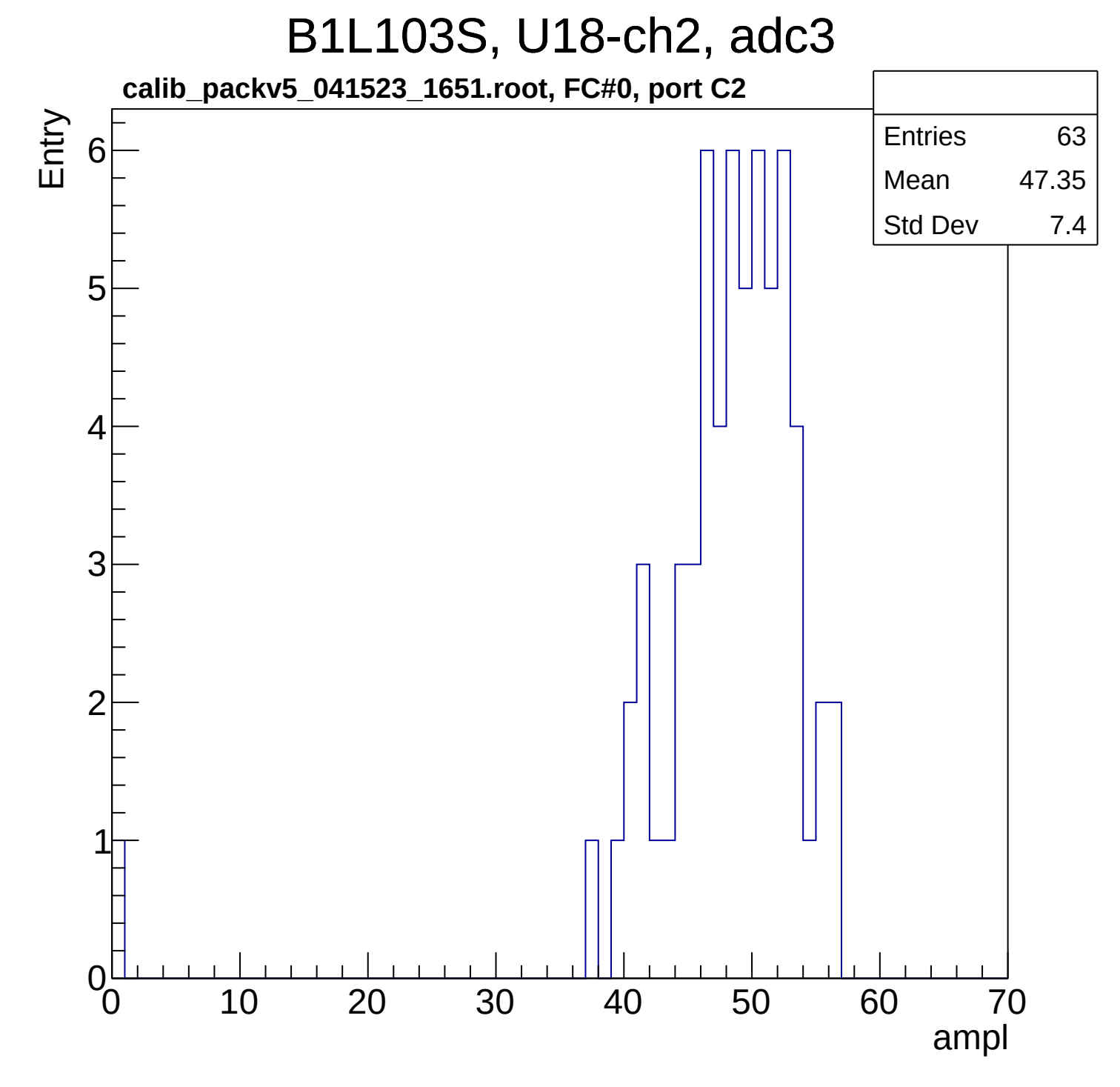
B1L103S, U18-ch2, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 47.35
Std Dev 7.4
Entry
ampl
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3
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5
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0
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60
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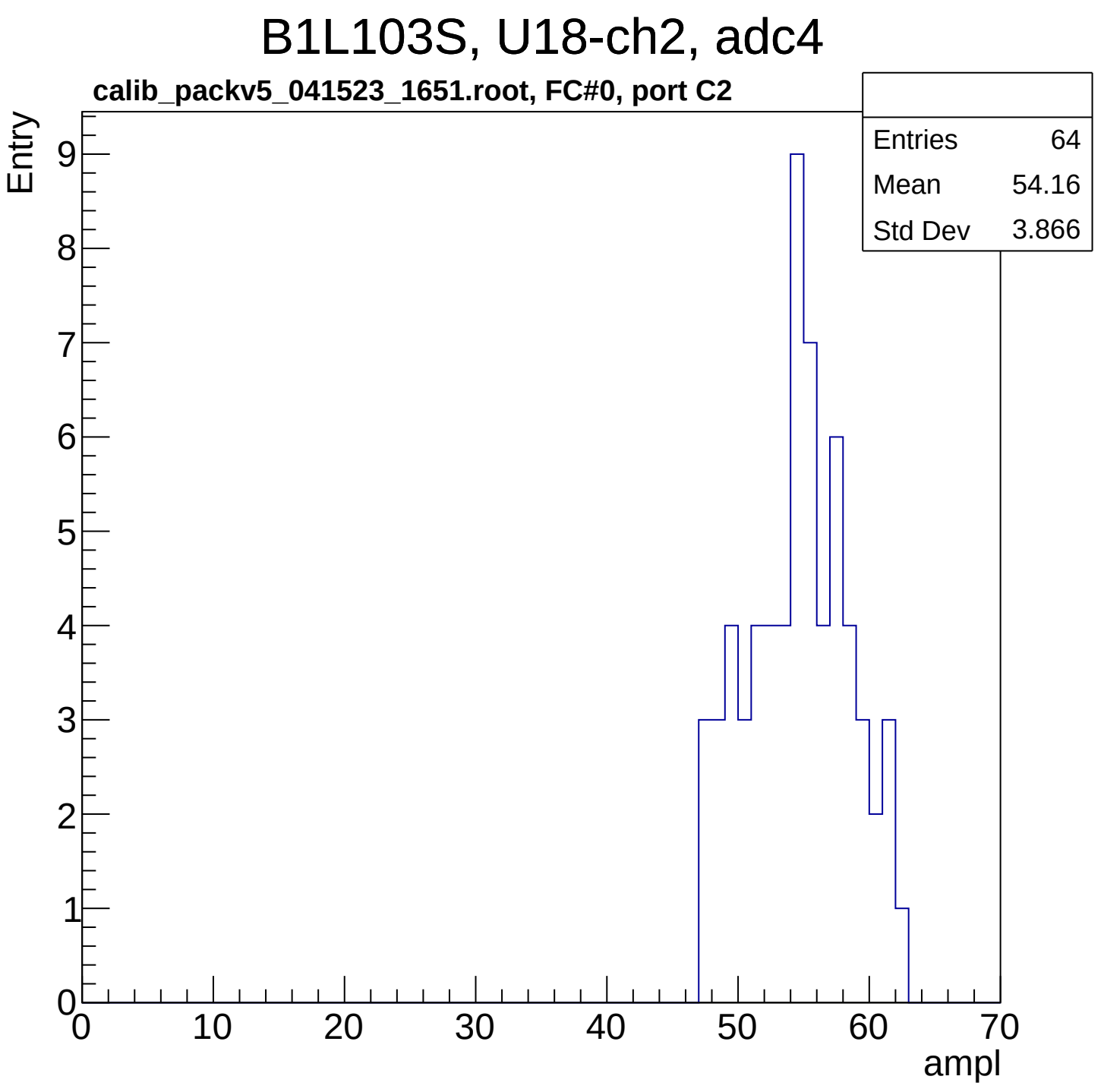
B1L103S, U18-ch2, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 54.16
Std Dev 3.866
Entry
ampl
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3
4
5
6
7
8
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0
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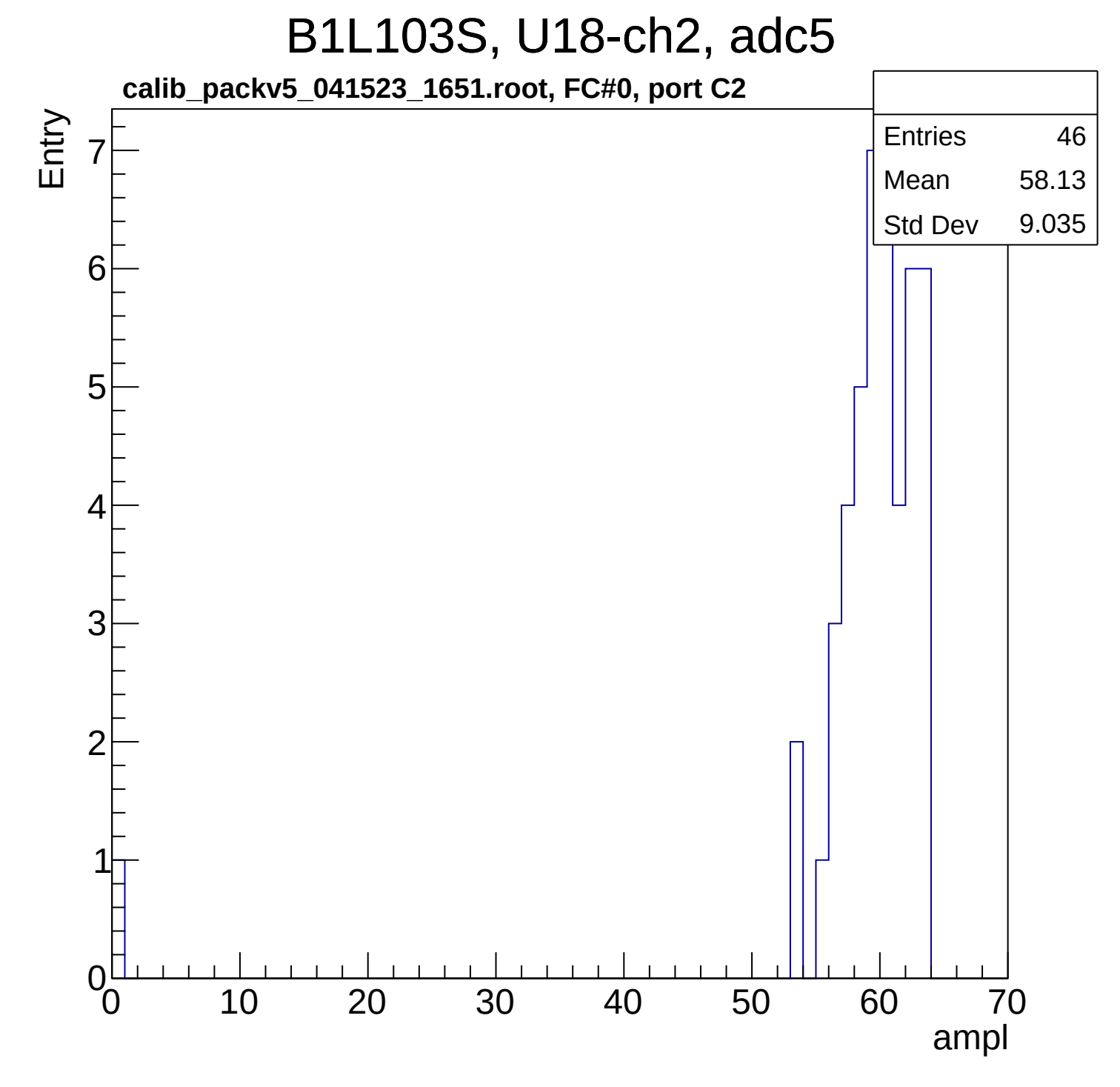
B1L103S, U18-ch2, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 58.13
Std Dev 9.035
Entry
ampl
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2
3
4
5
6
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0
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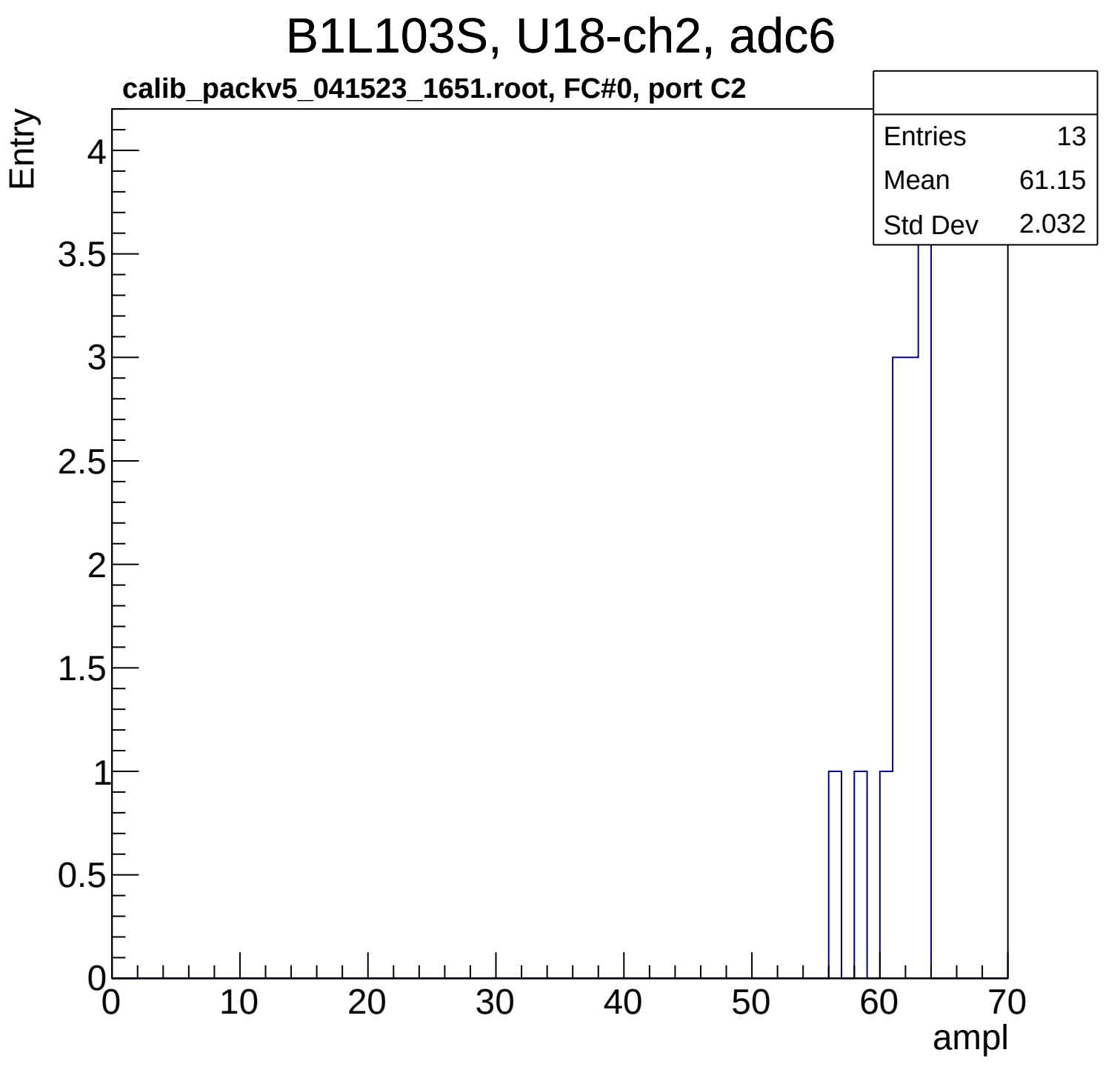
60
70


B1L103S, U18-ch2, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 13
Mean 61.15
Std Dev 2.032
Entry
ampl
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0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
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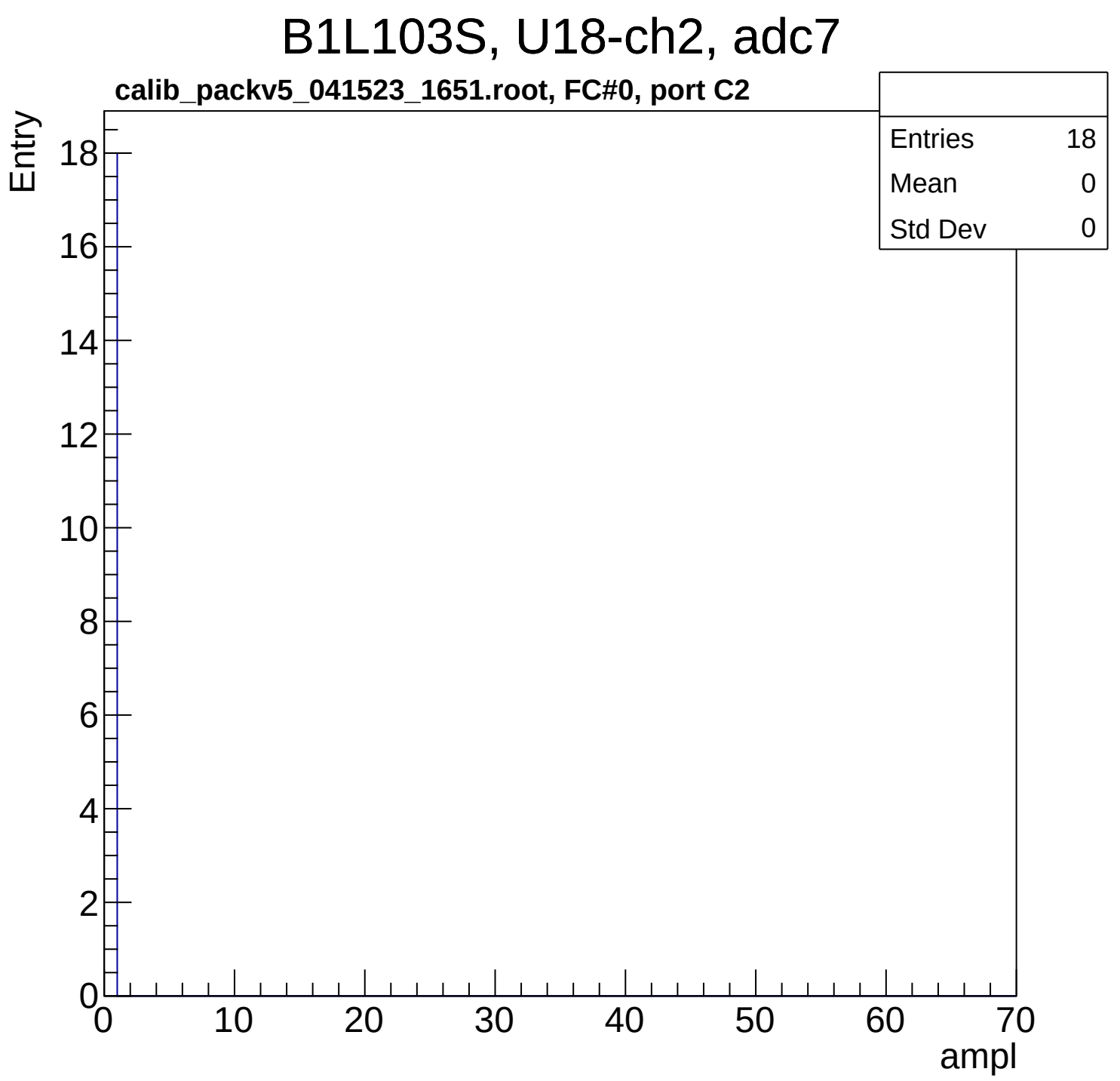
40
50
60
70


B1L103S, U18-ch2, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
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6
8
10
12
14
16
18
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10
20
30
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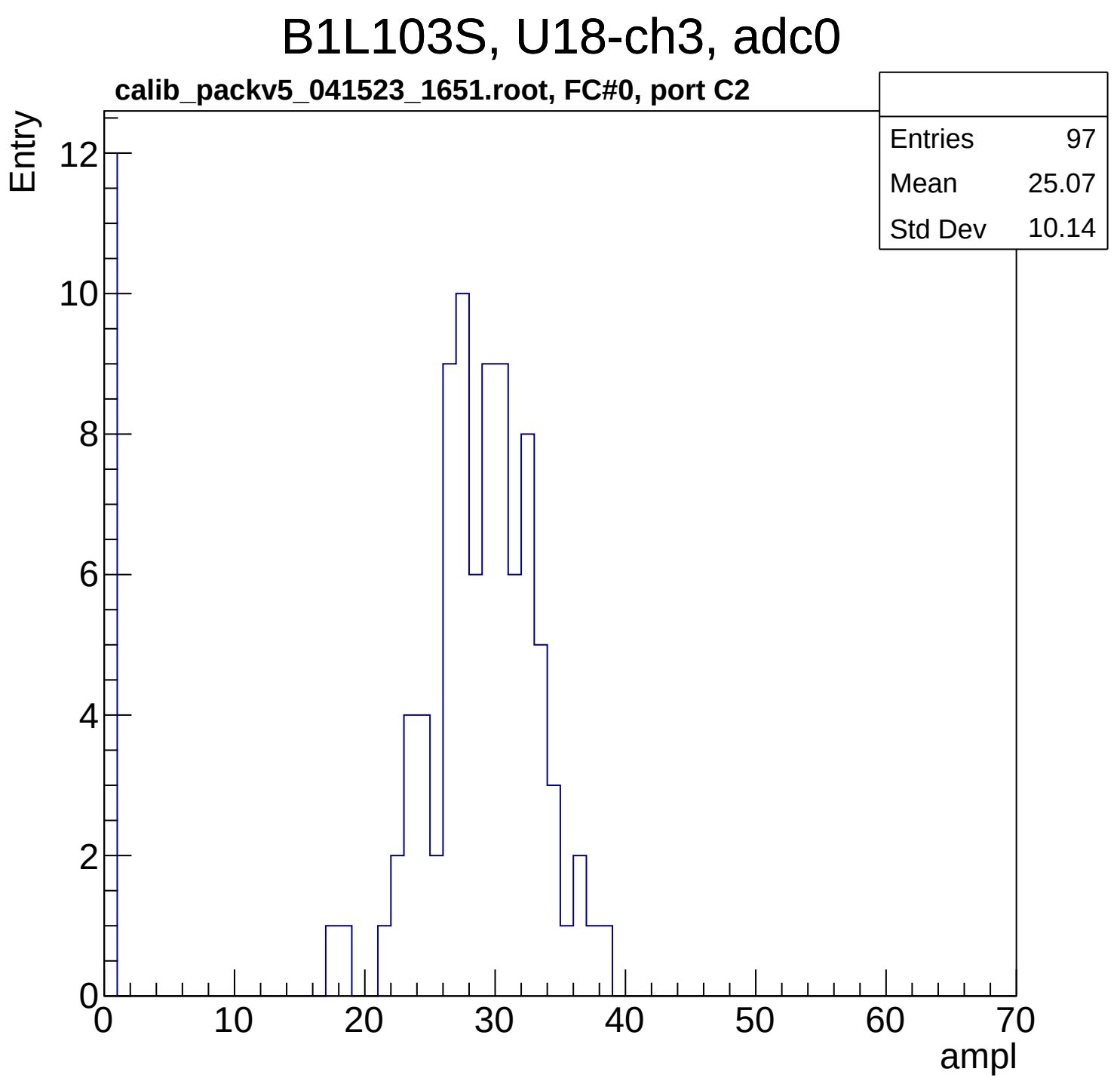
50
60
70
ampl


B1L103S, U18-ch3, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 97
Mean 25.07
Std Dev 10.14
Entry
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10
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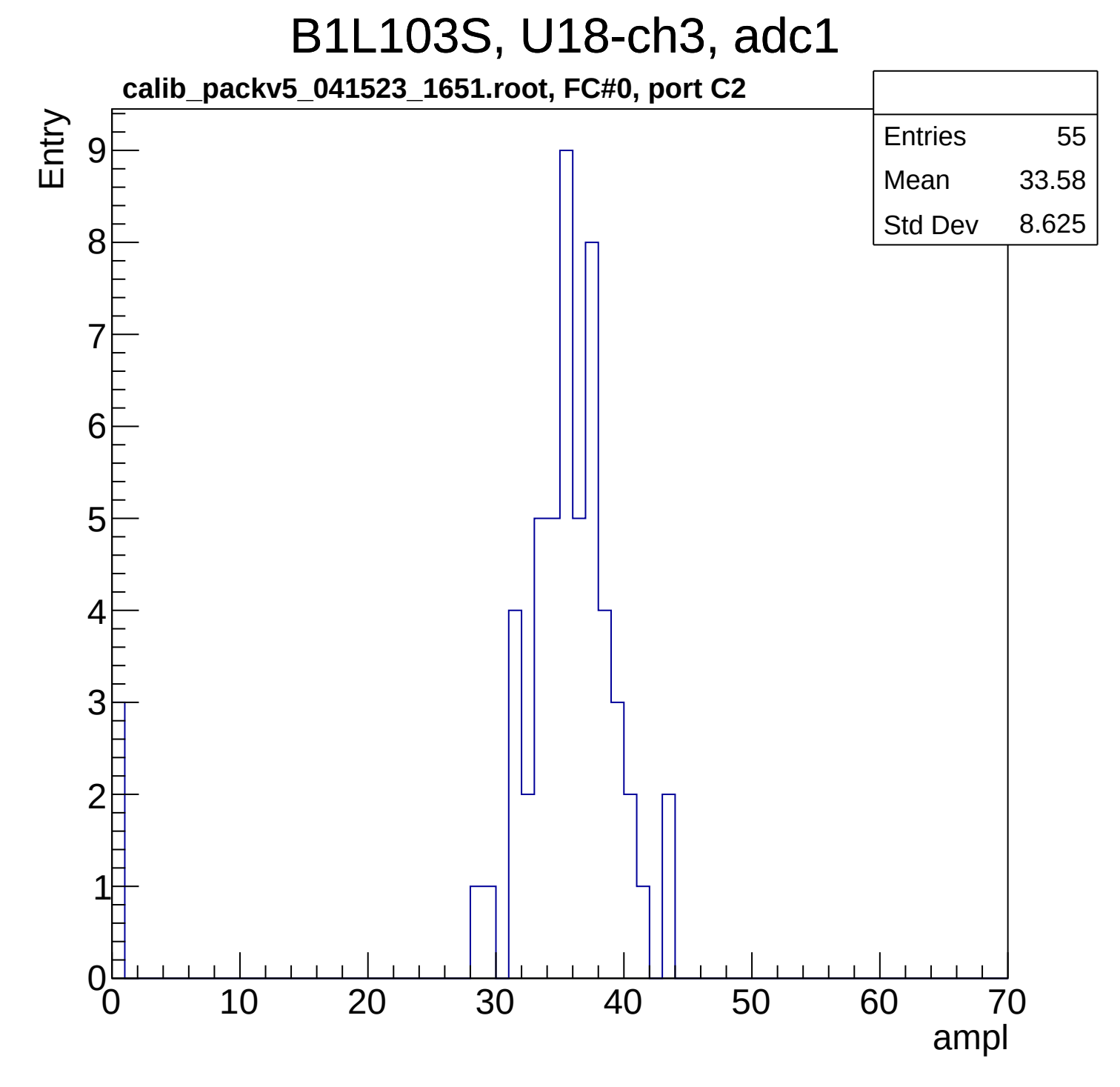
70
ampl


B1L103S, U18-ch3, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 33.58
Std Dev 8.625
Entry
ampl
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0
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50
60
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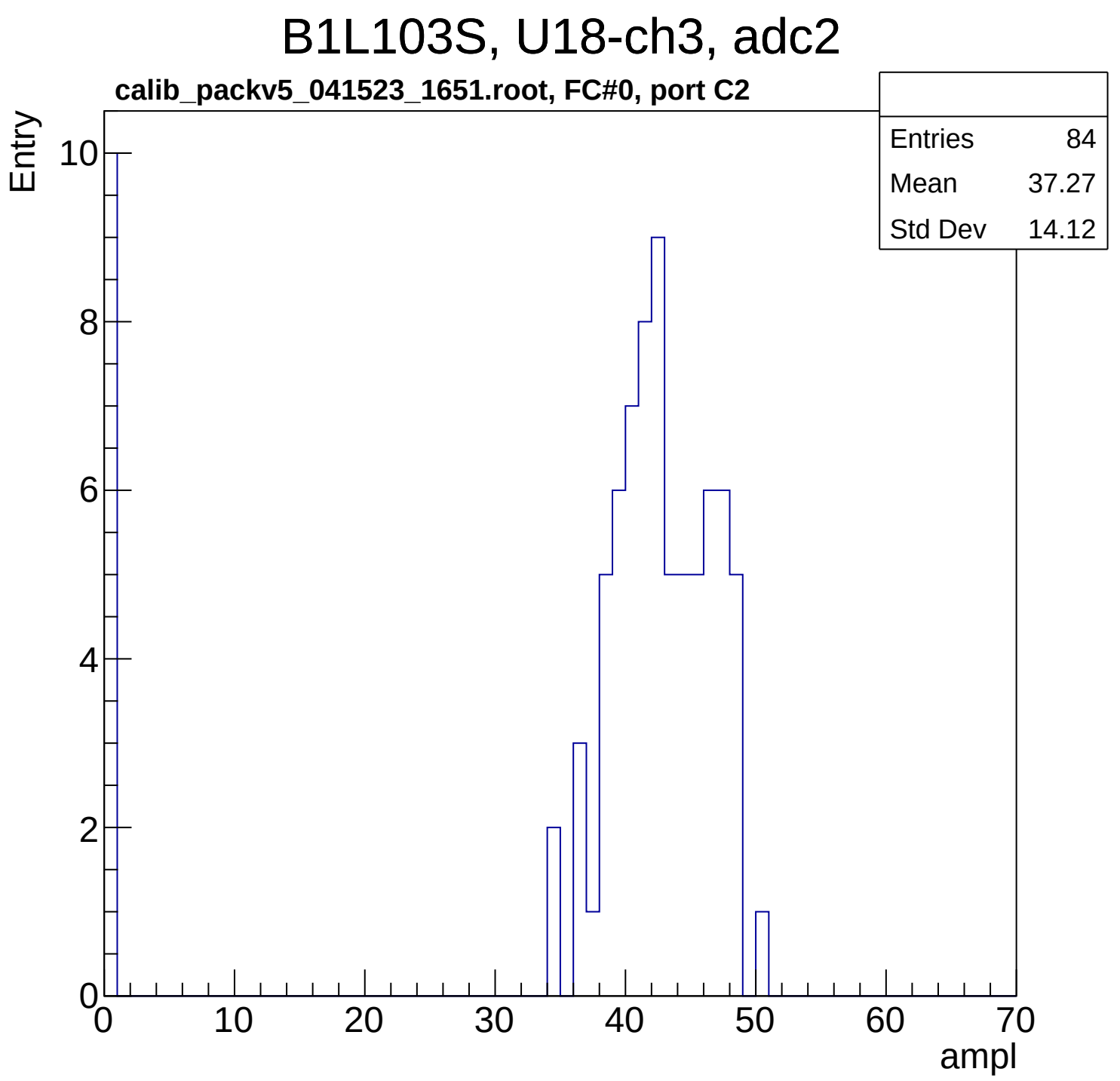
B1L103S, U18-ch3, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 37.27
Std Dev 14.12
Entry
ampl
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20
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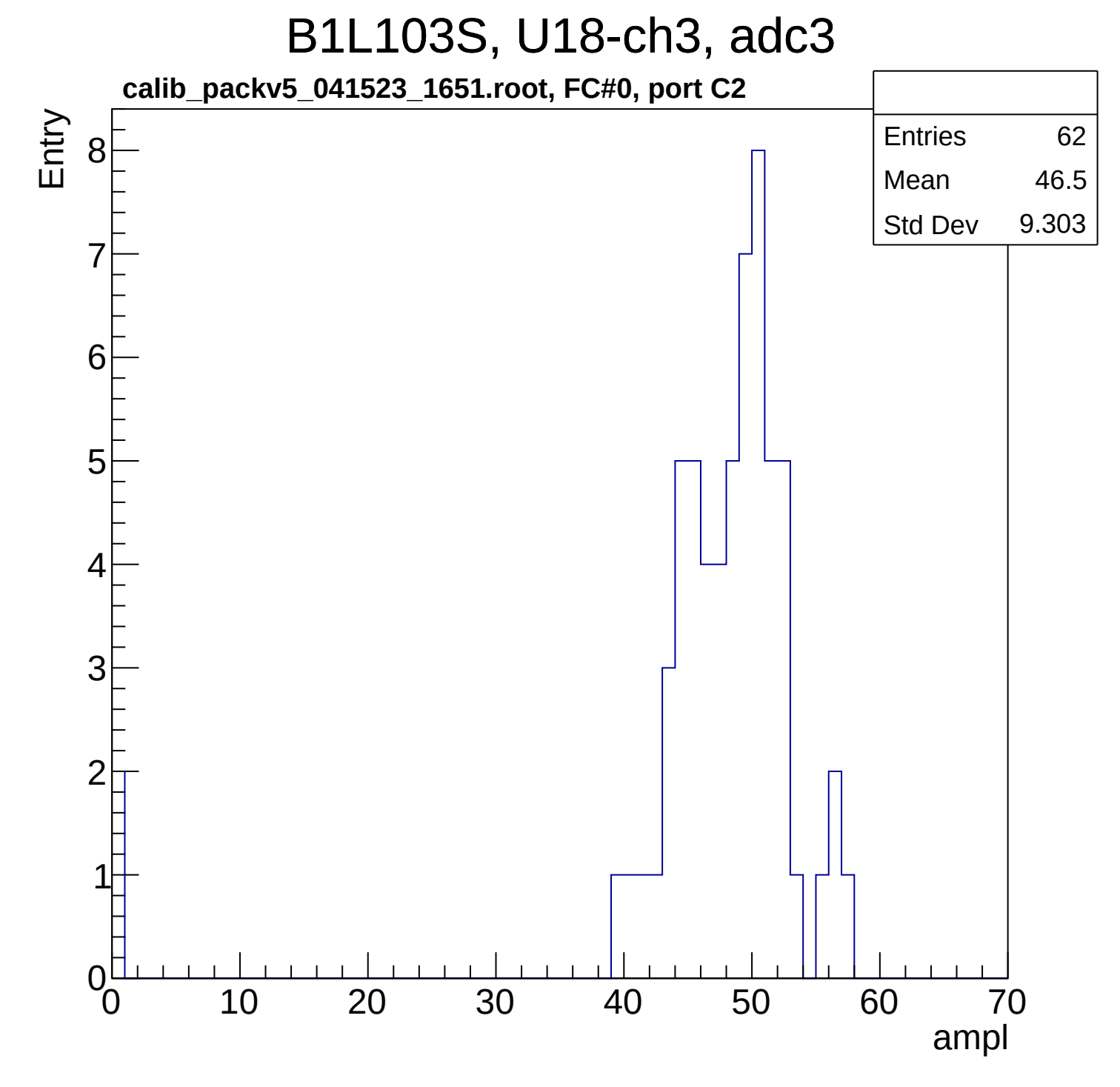
40
50
60
70


B1L103S, U18-ch3, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 46.5
Std Dev 9.303
Entry
ampl
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2
3
4
5
6
7
8
0
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20
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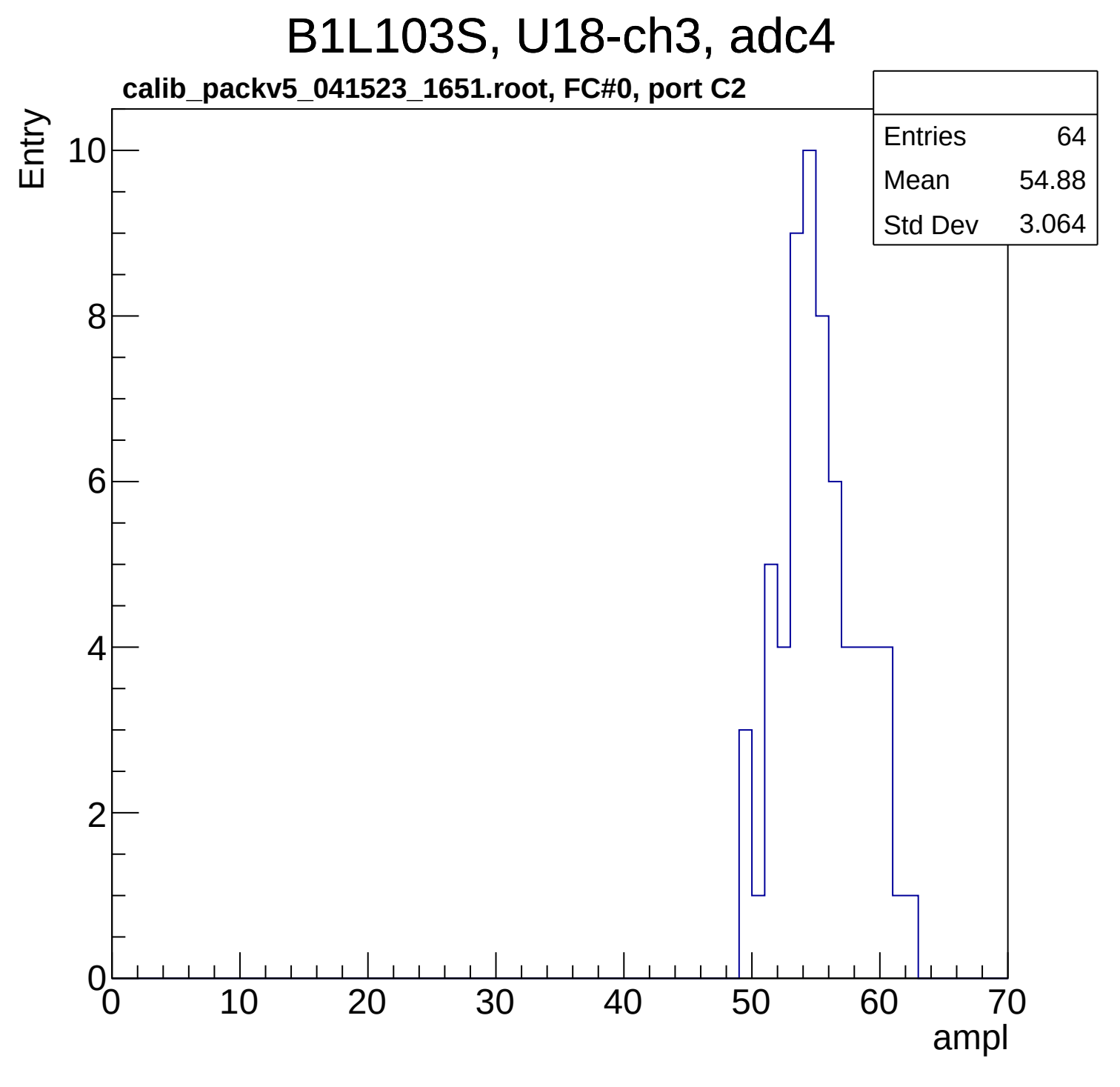
40
50
60
70


B1L103S, U18-ch3, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 54.88
Std Dev 3.064
Entry
ampl
0
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4
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8
10
0
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20
30
40
50
60
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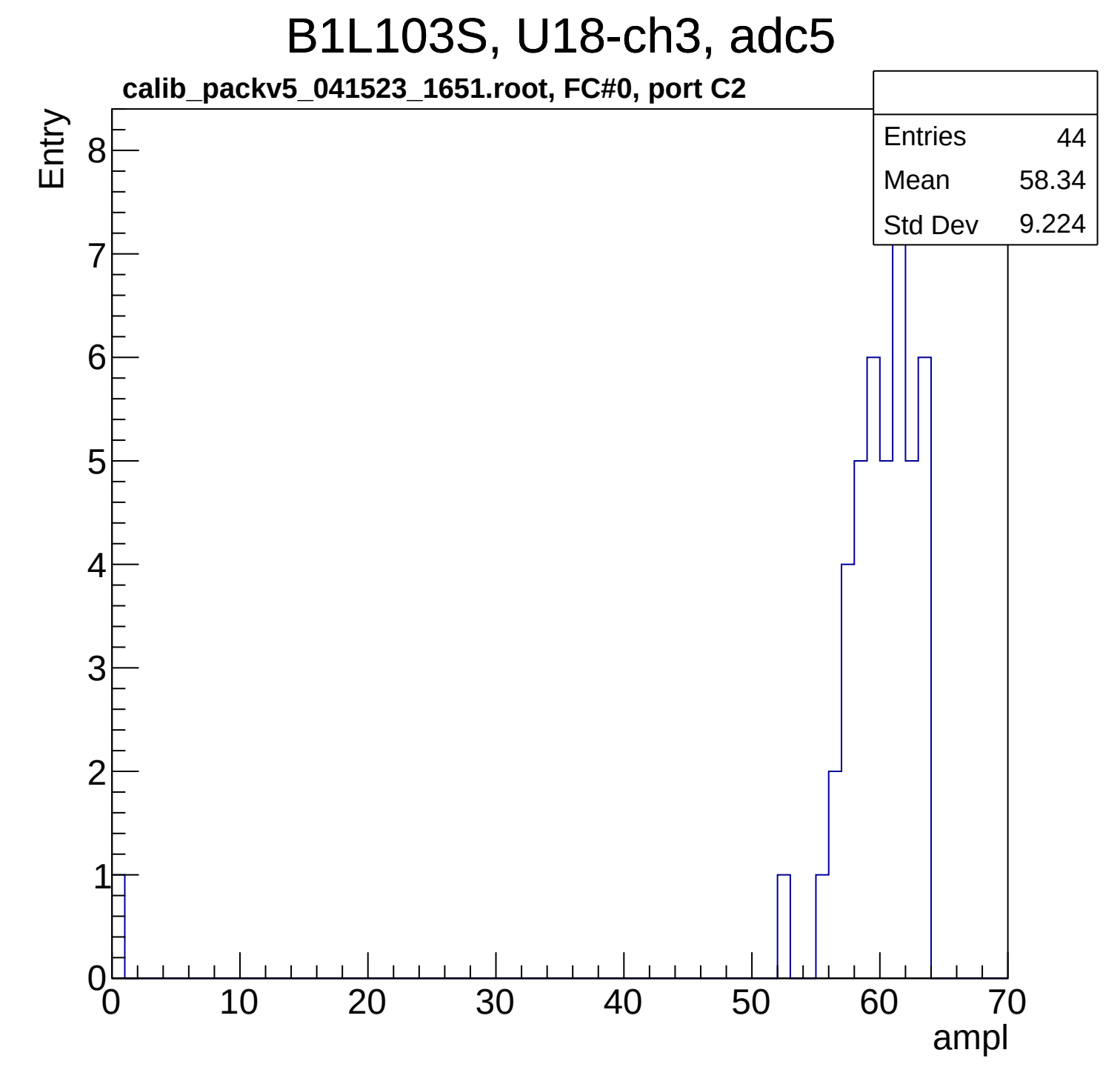
B1L103S, U18-ch3, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 58.34
Std Dev 9.224
Entry
ampl
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1
2
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4
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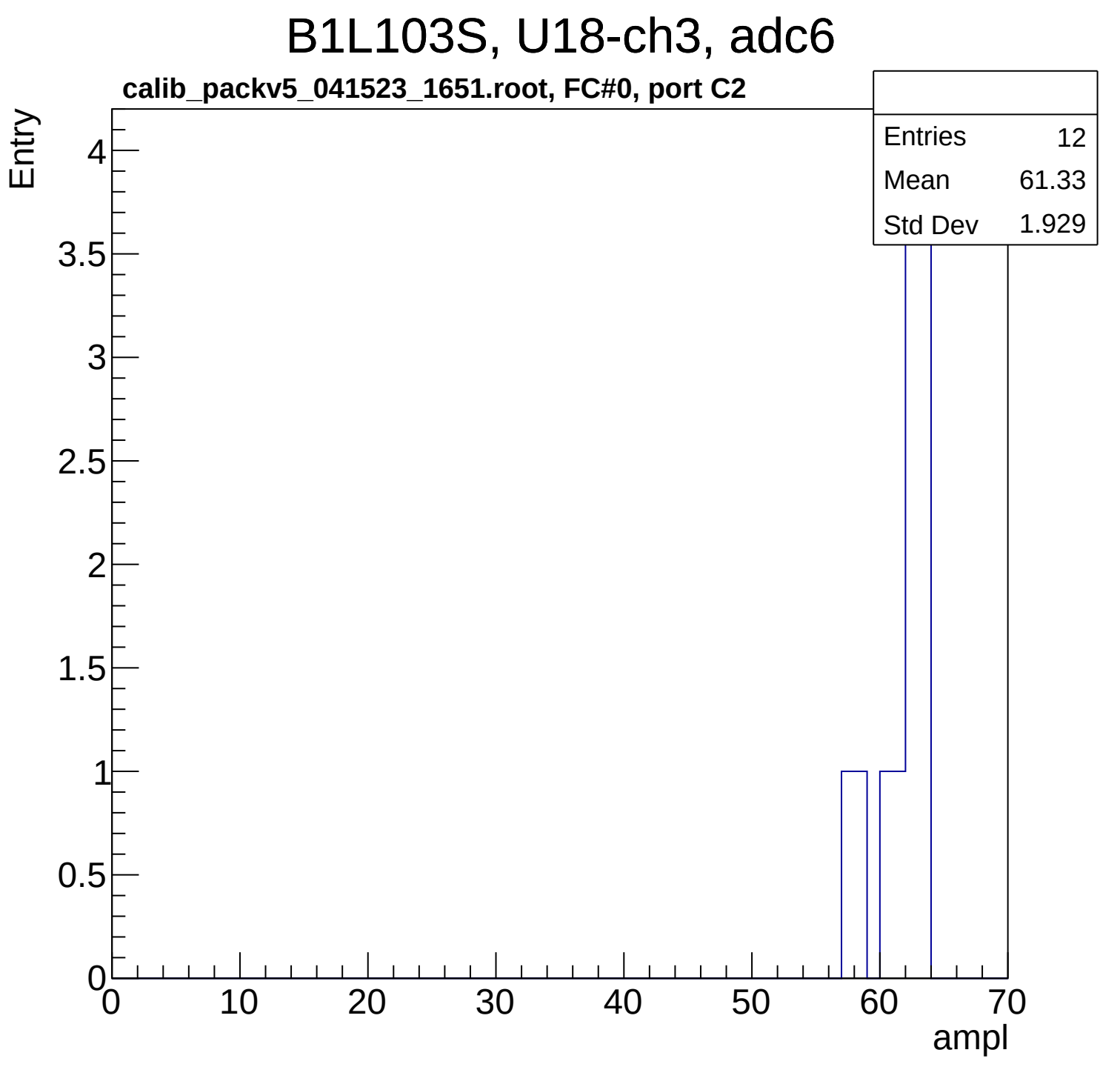
B1L103S, U18-ch3, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 61.33
Std Dev 1.929
Entry
ampl
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1.5
2
2.5
3
3.5
4
0
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20
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40
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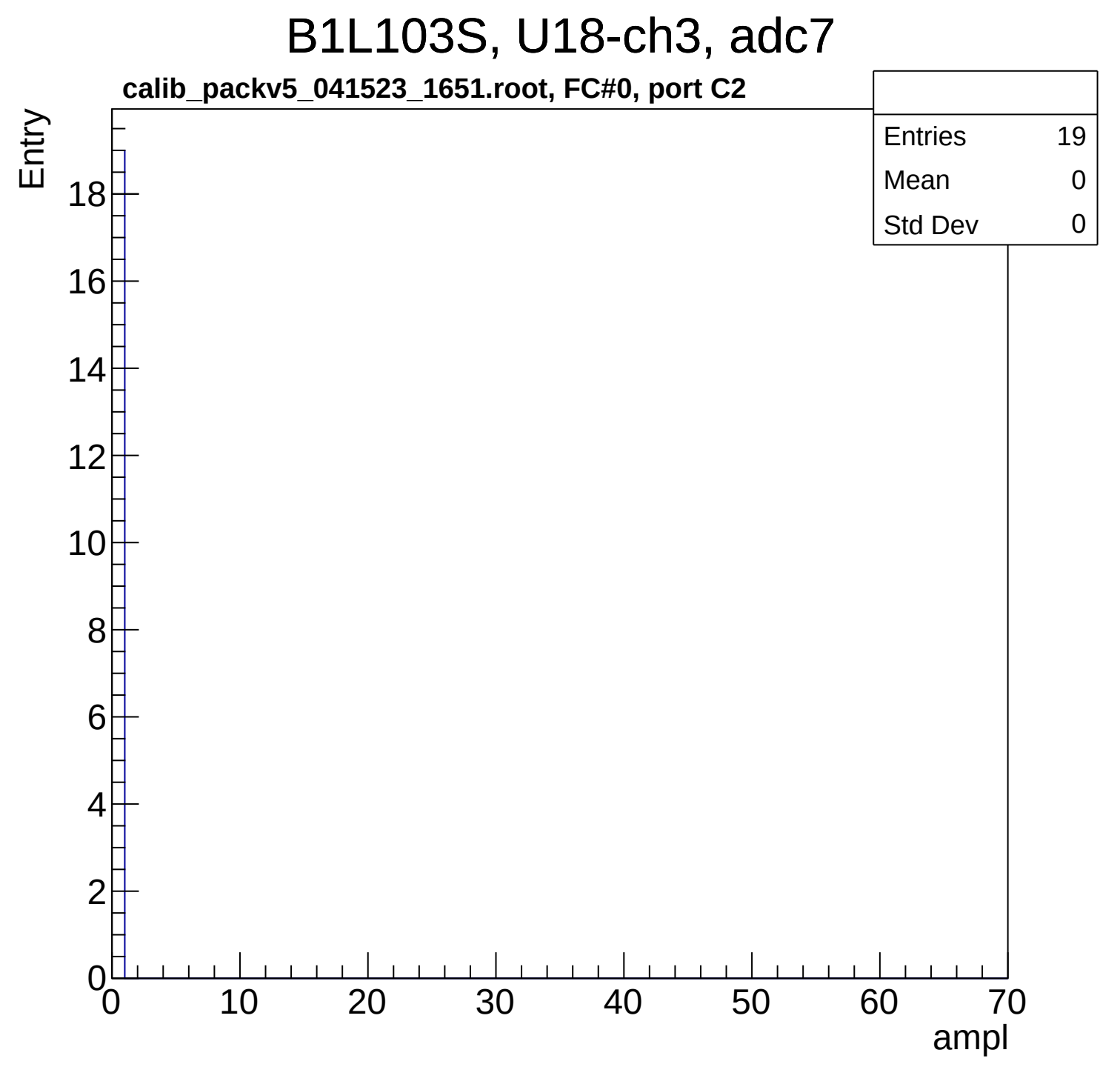
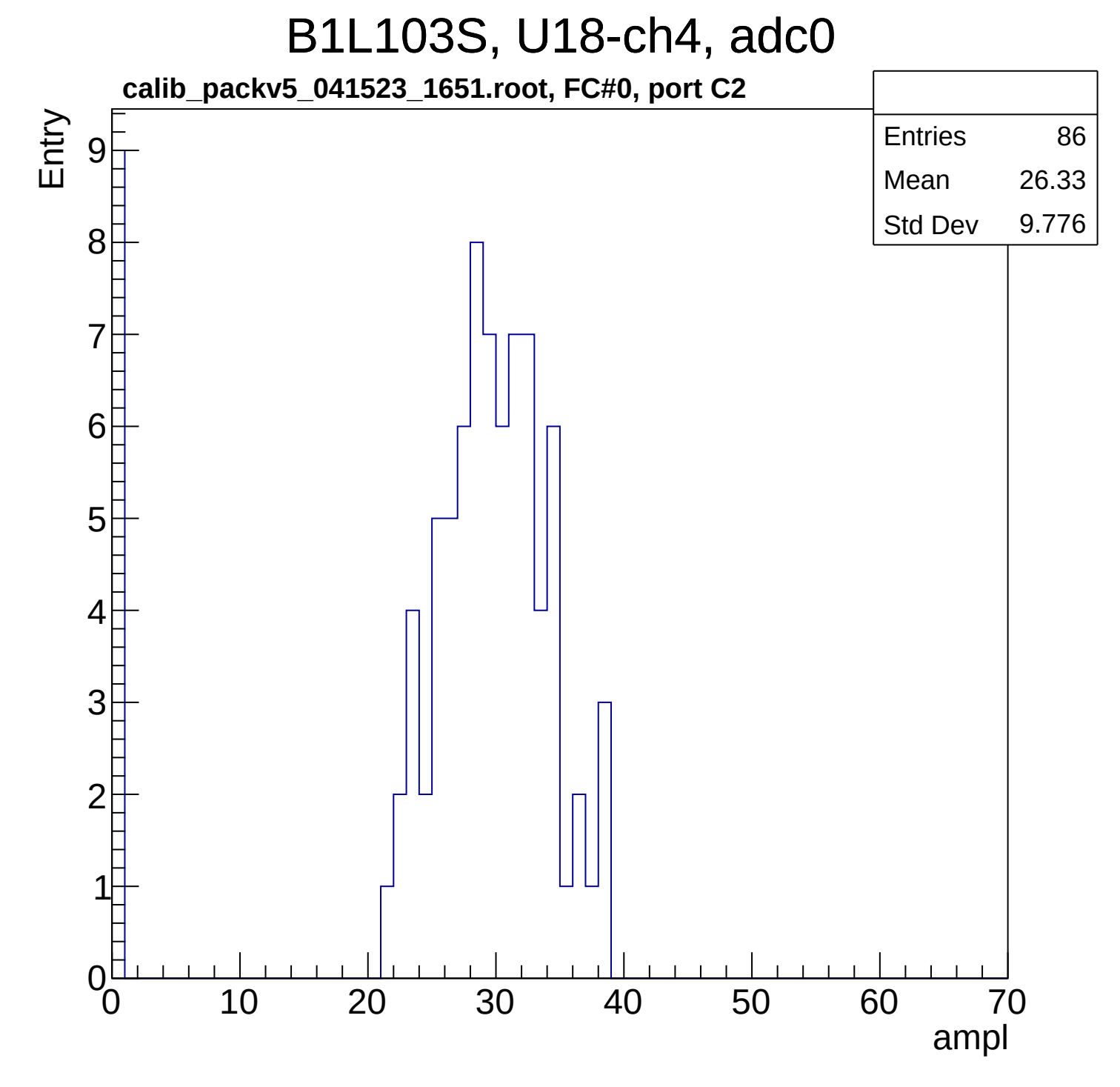
60
70


B1L103S, U18-ch3, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch4, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 26.33
Std Dev 9.776
Entry
ampl
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1
2
3
4
5
6
7
8
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0
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60
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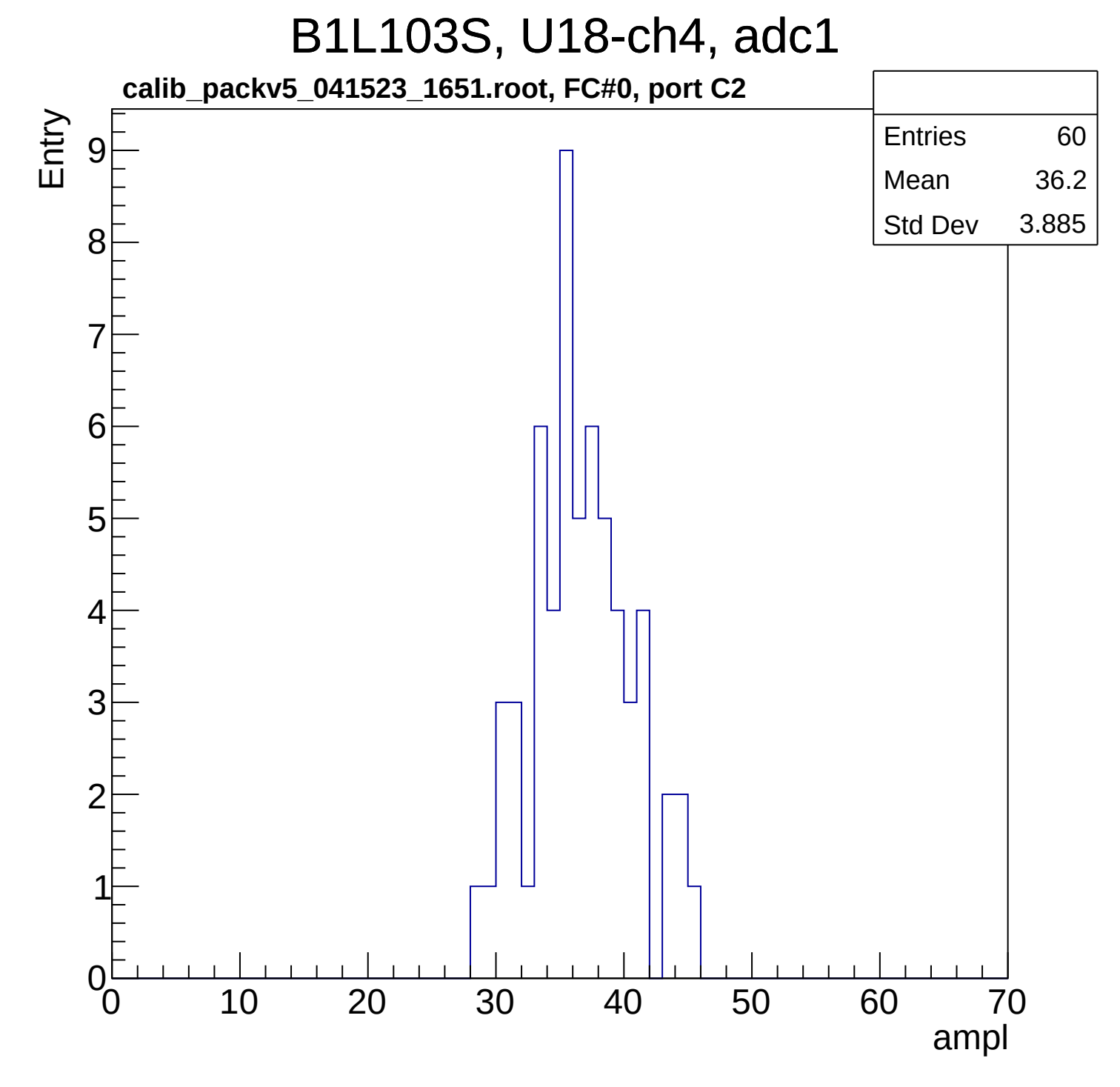
B1L103S, U18-ch4, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 36.2
Std Dev 3.885
Entry
ampl
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2
3
4
5
6
7
8
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0
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40
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60
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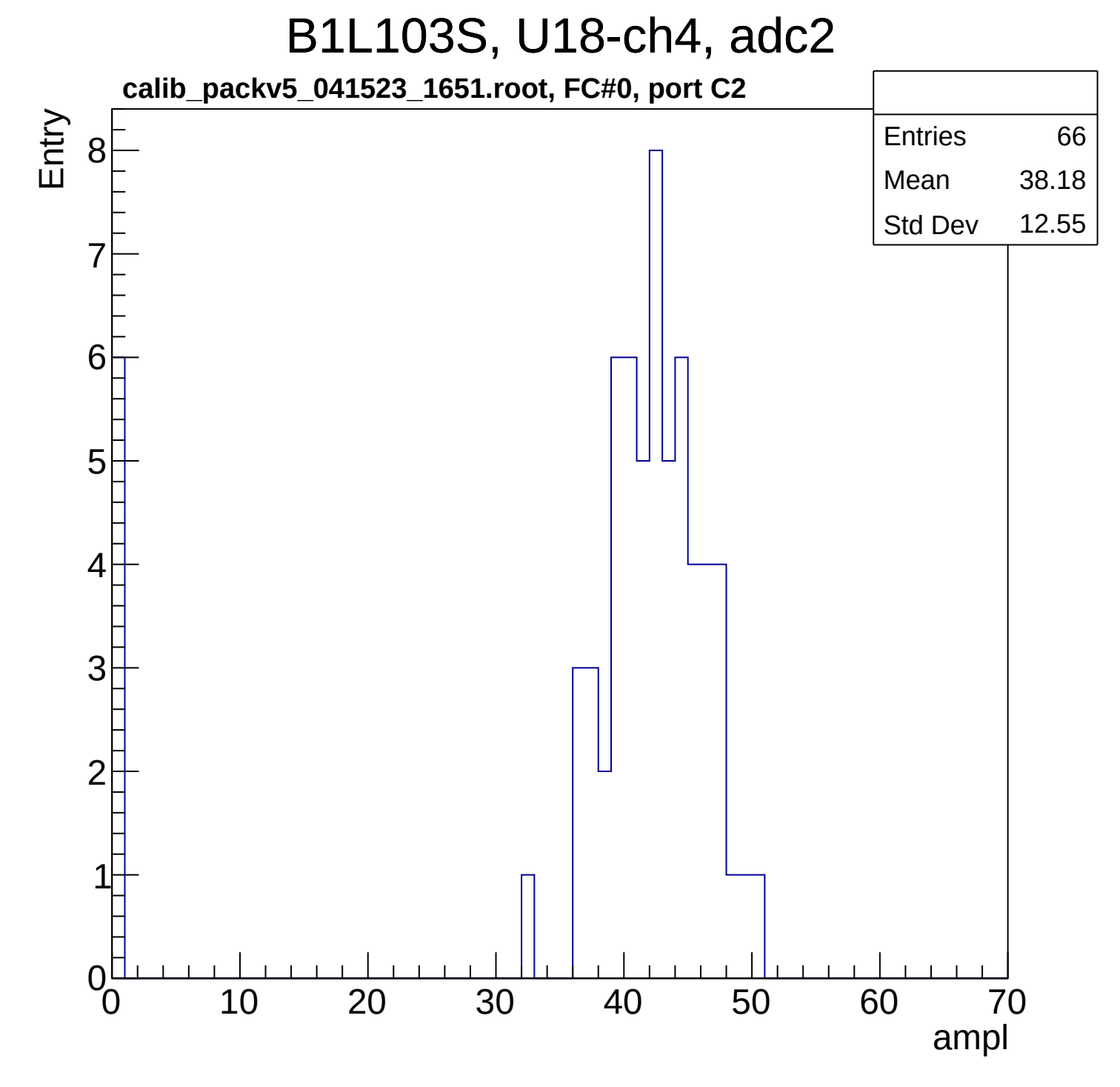
B1L103S, U18-ch4, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 38.18
Std Dev 12.55
Entry
ampl
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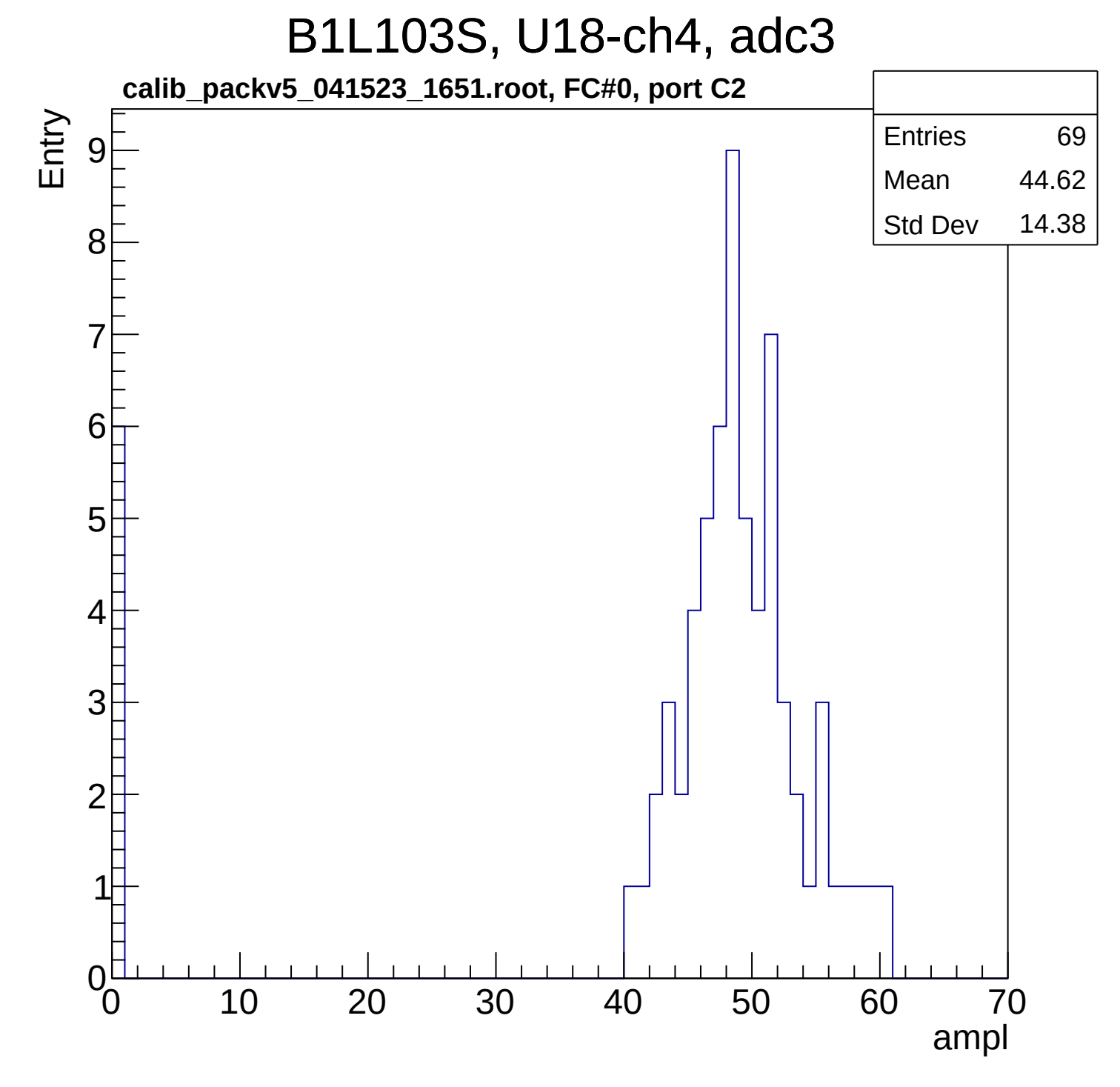
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch4, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 44.62
Std Dev 14.38
Entry
ampl
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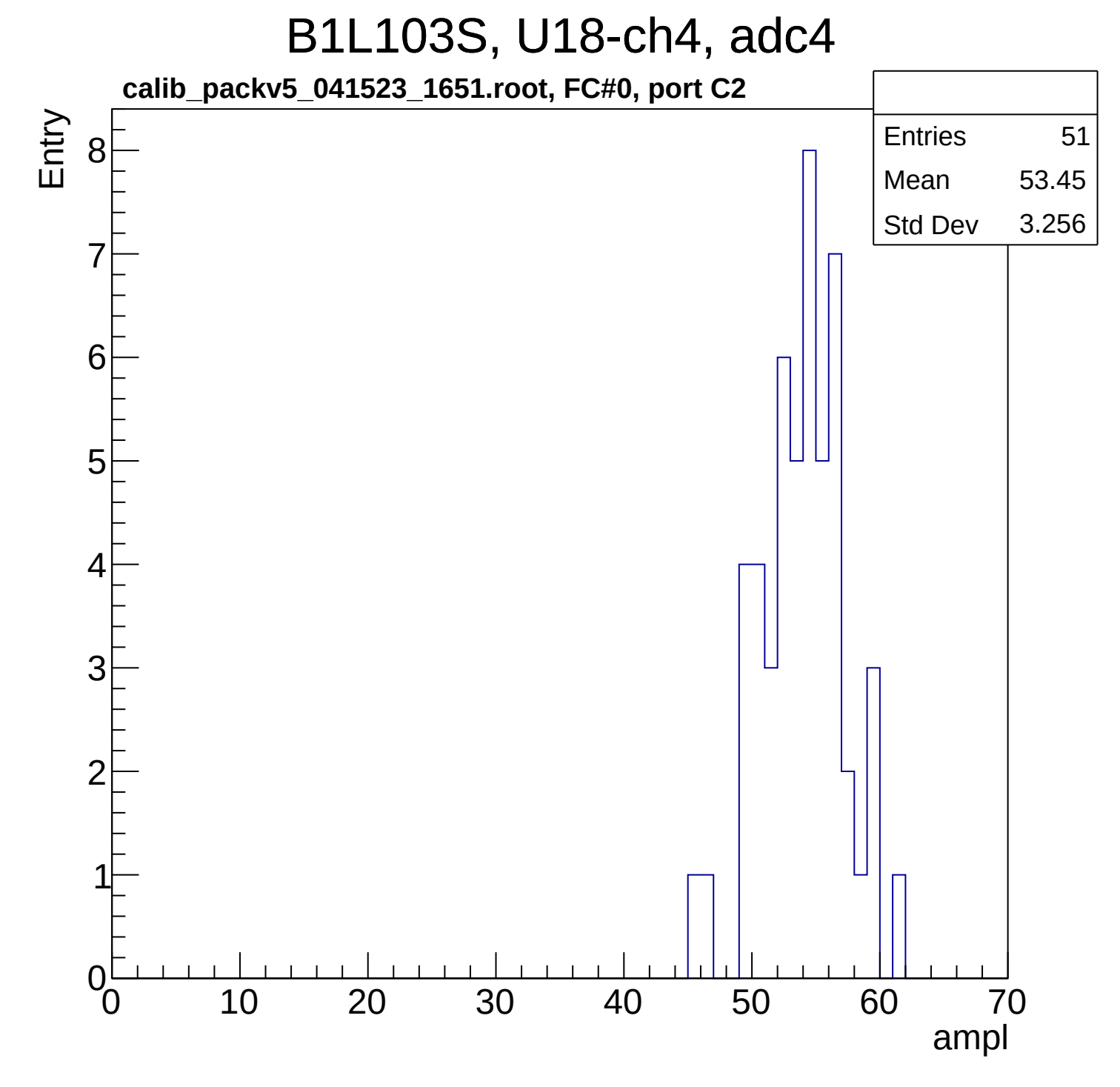
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U18-ch4, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 53.45
Std Dev 3.256
Entry
ampl
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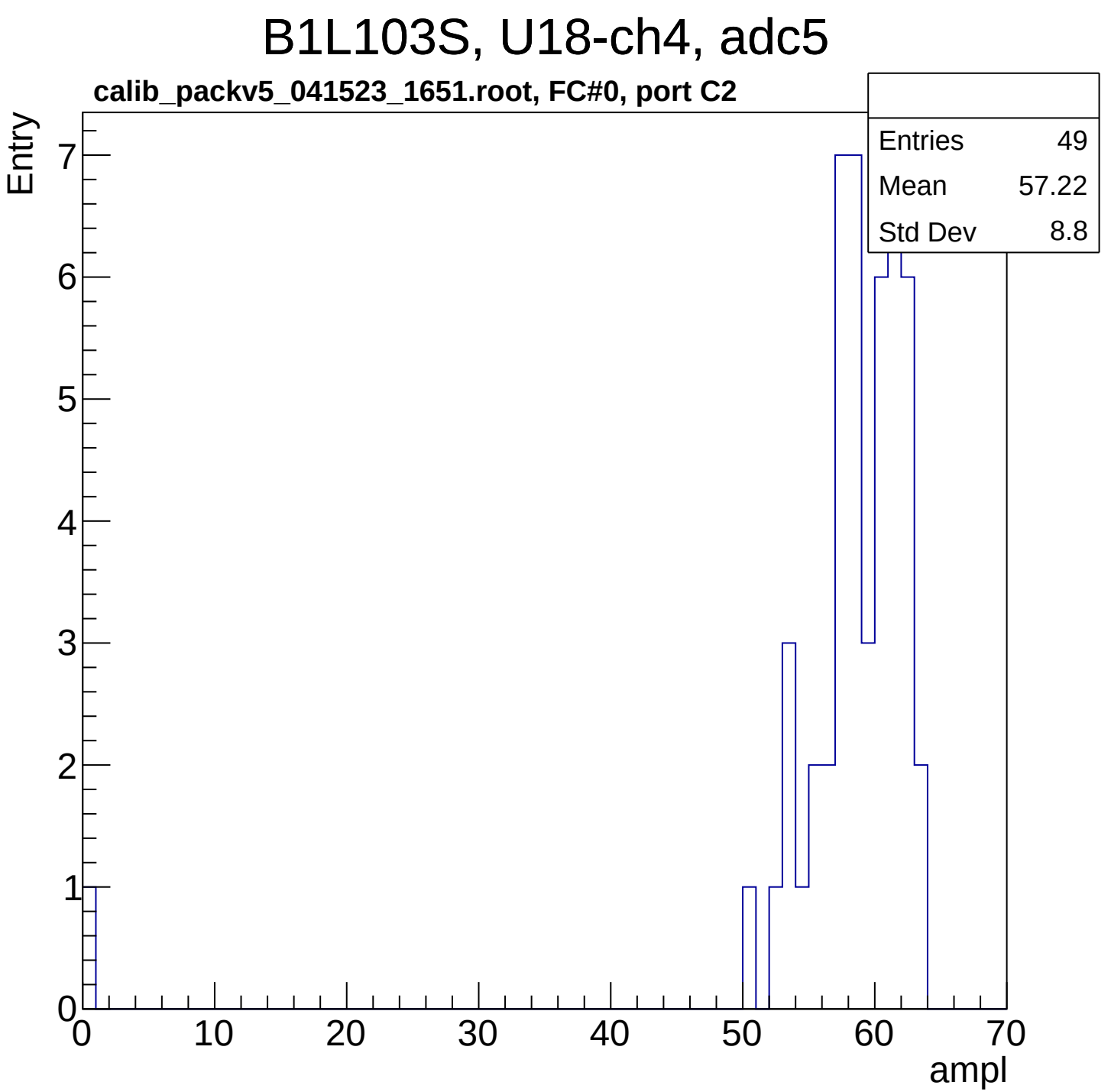
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch4, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 57.22
Std Dev 8.8
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
30
40
50
60
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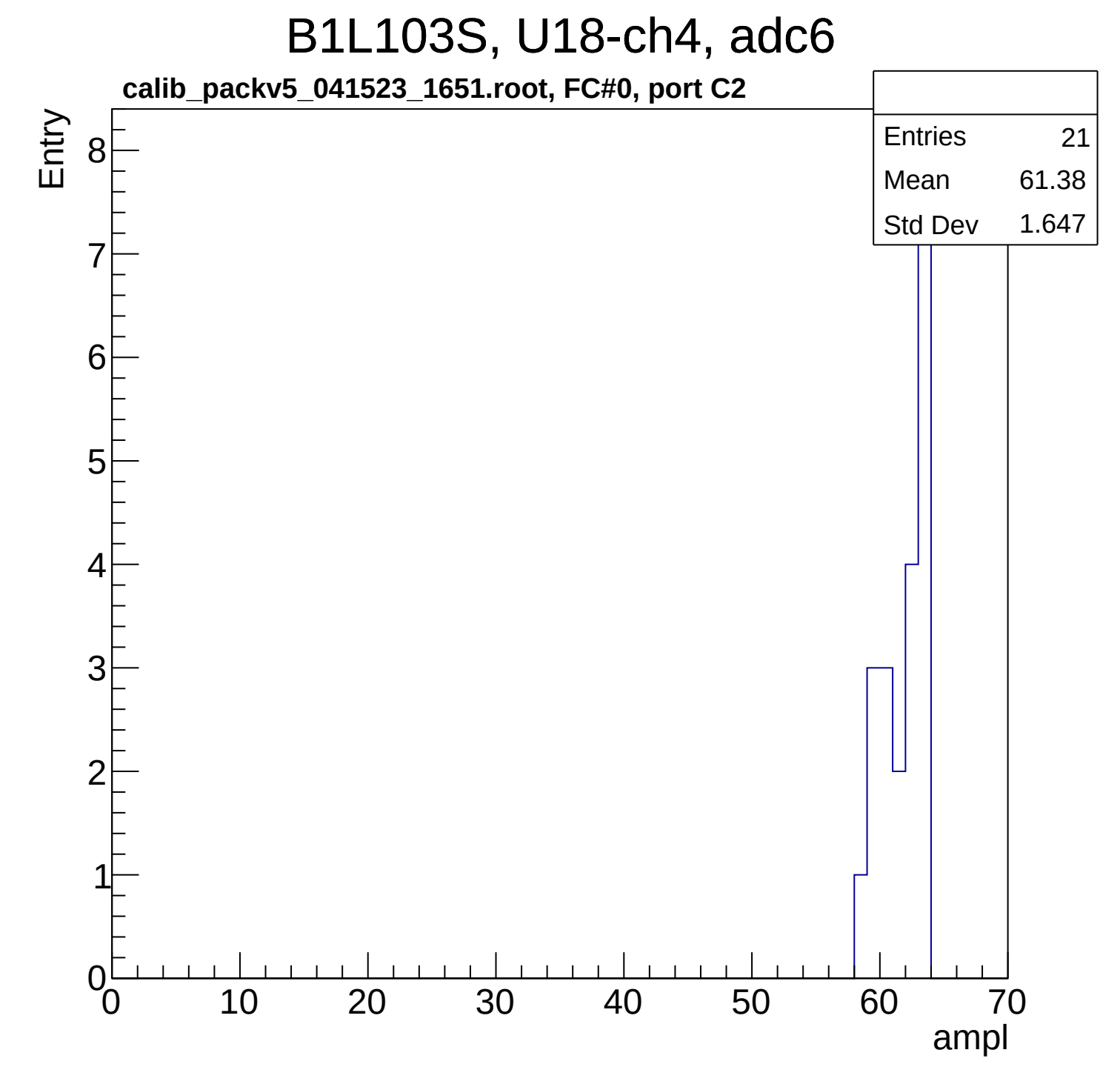
B1L103S, U18-ch4, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 61.38
Std Dev 1.647
Entry
ampl
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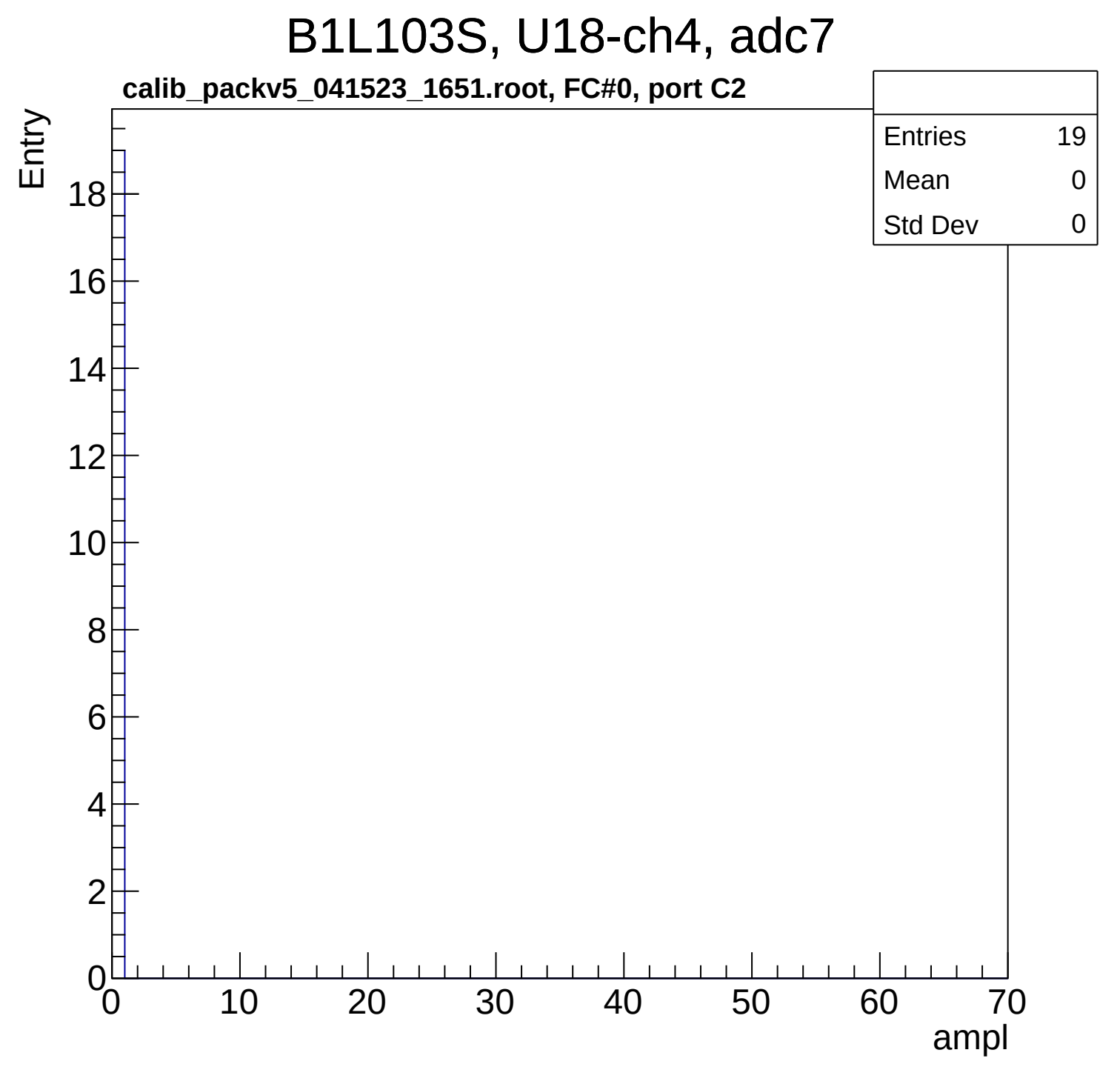
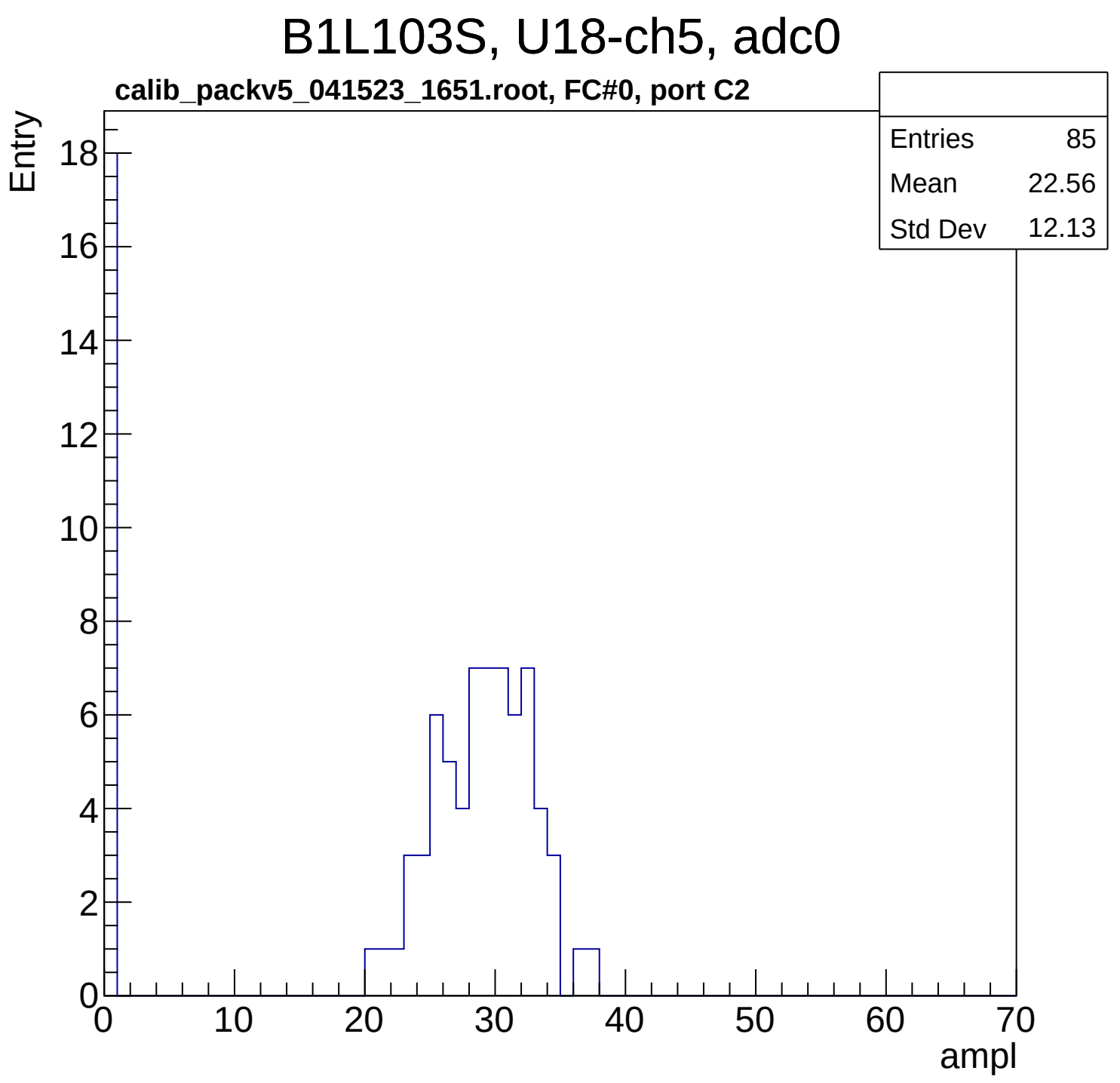
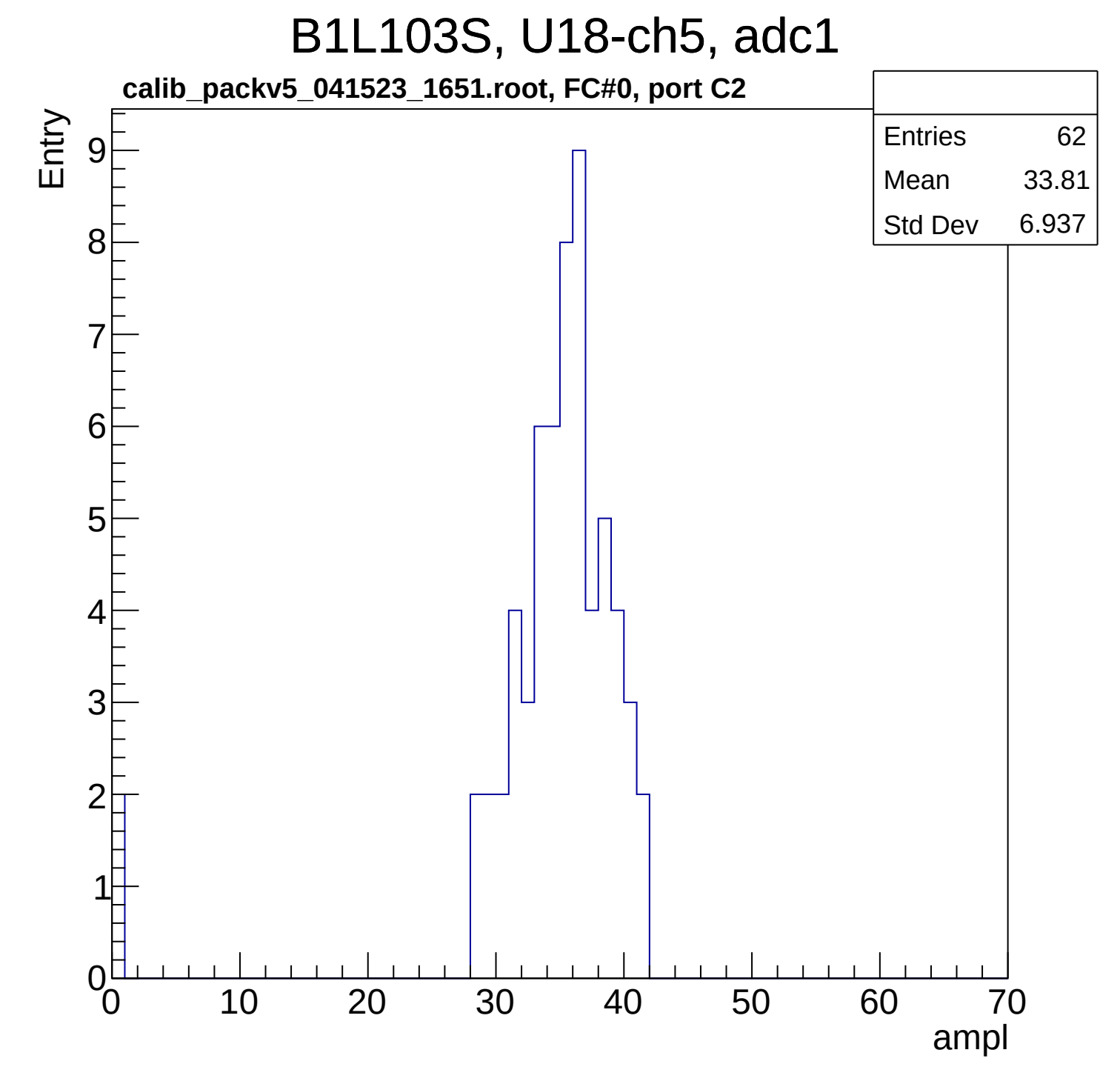
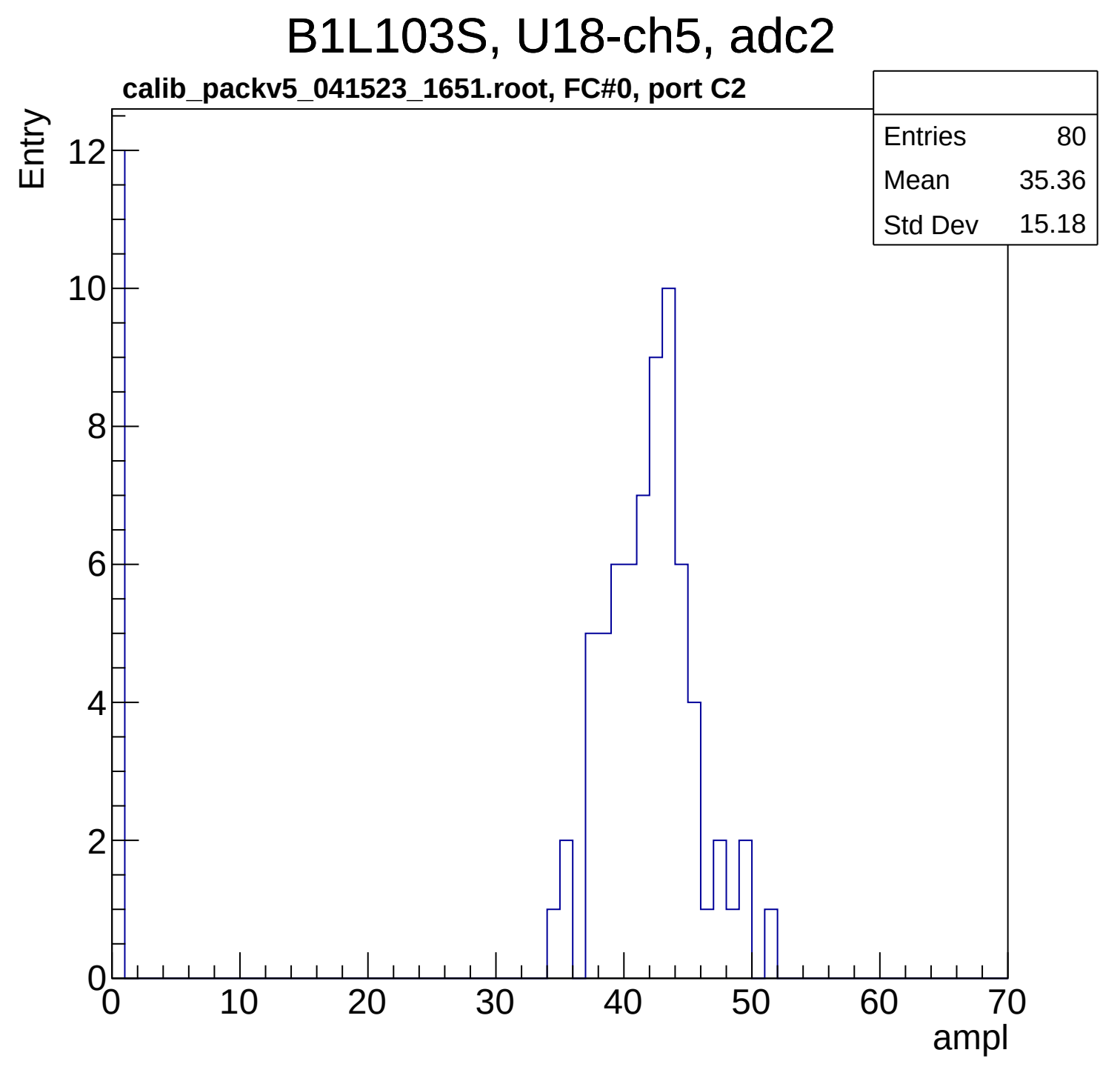
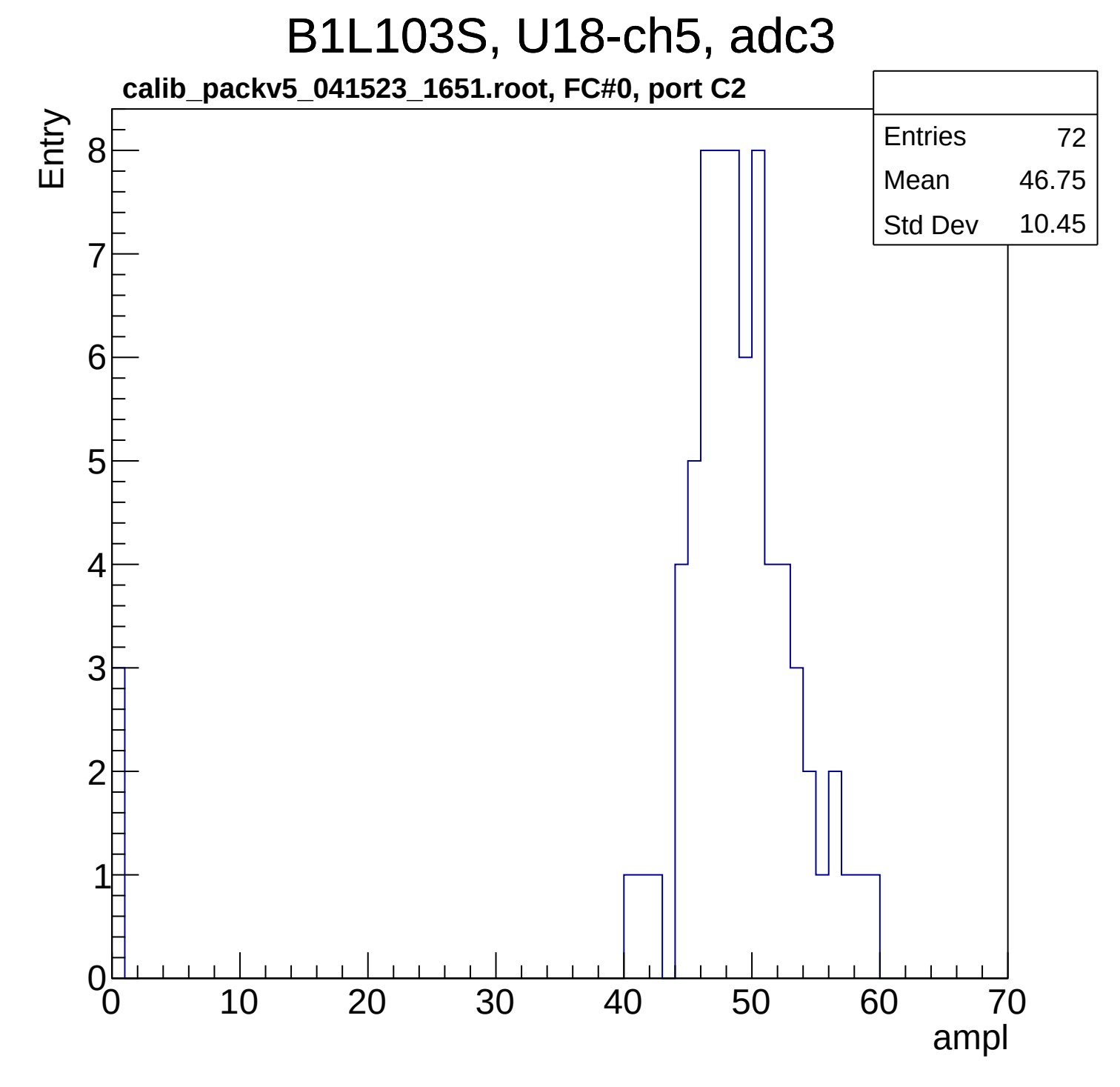
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch4, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch5, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 22.56
Std Dev 12.13
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch5, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 33.81
Std Dev 6.937
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U18-ch5, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 35.36
Std Dev 15.18
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch5, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 46.75
Std Dev 10.45
Entry
ampl
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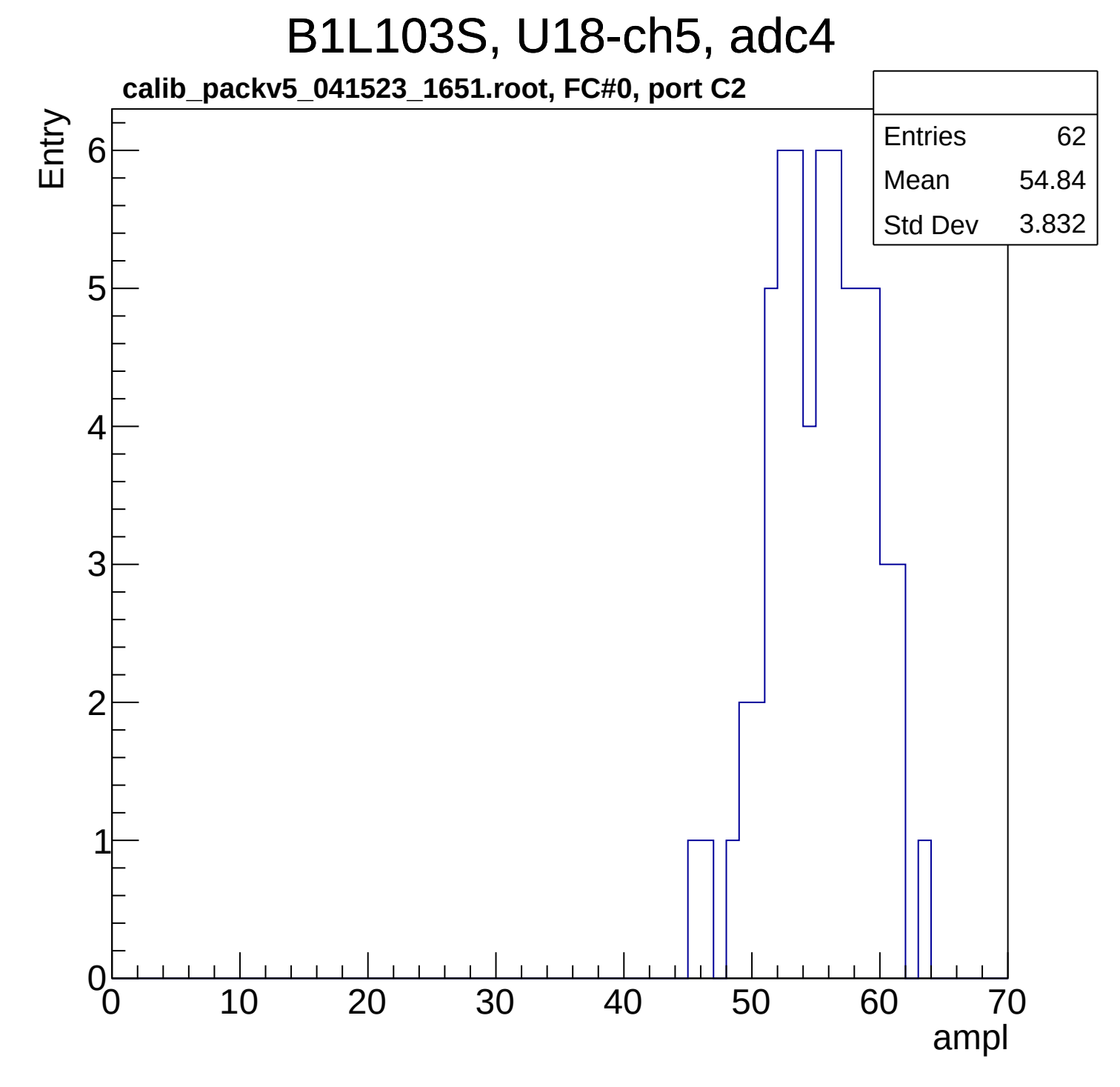
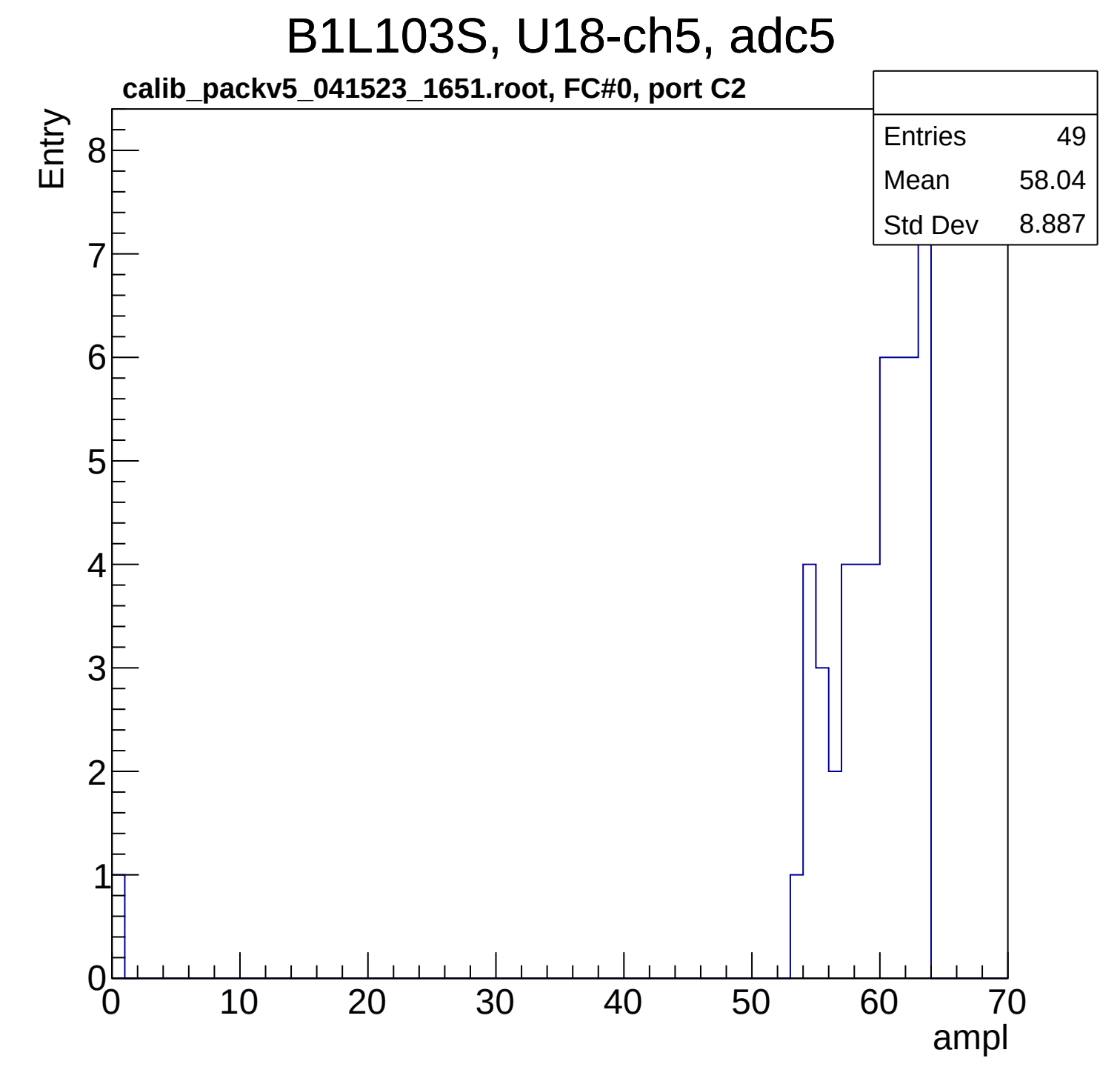
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch5, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 54.84
Std Dev 3.832
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U18-ch5, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 58.04
Std Dev 8.887
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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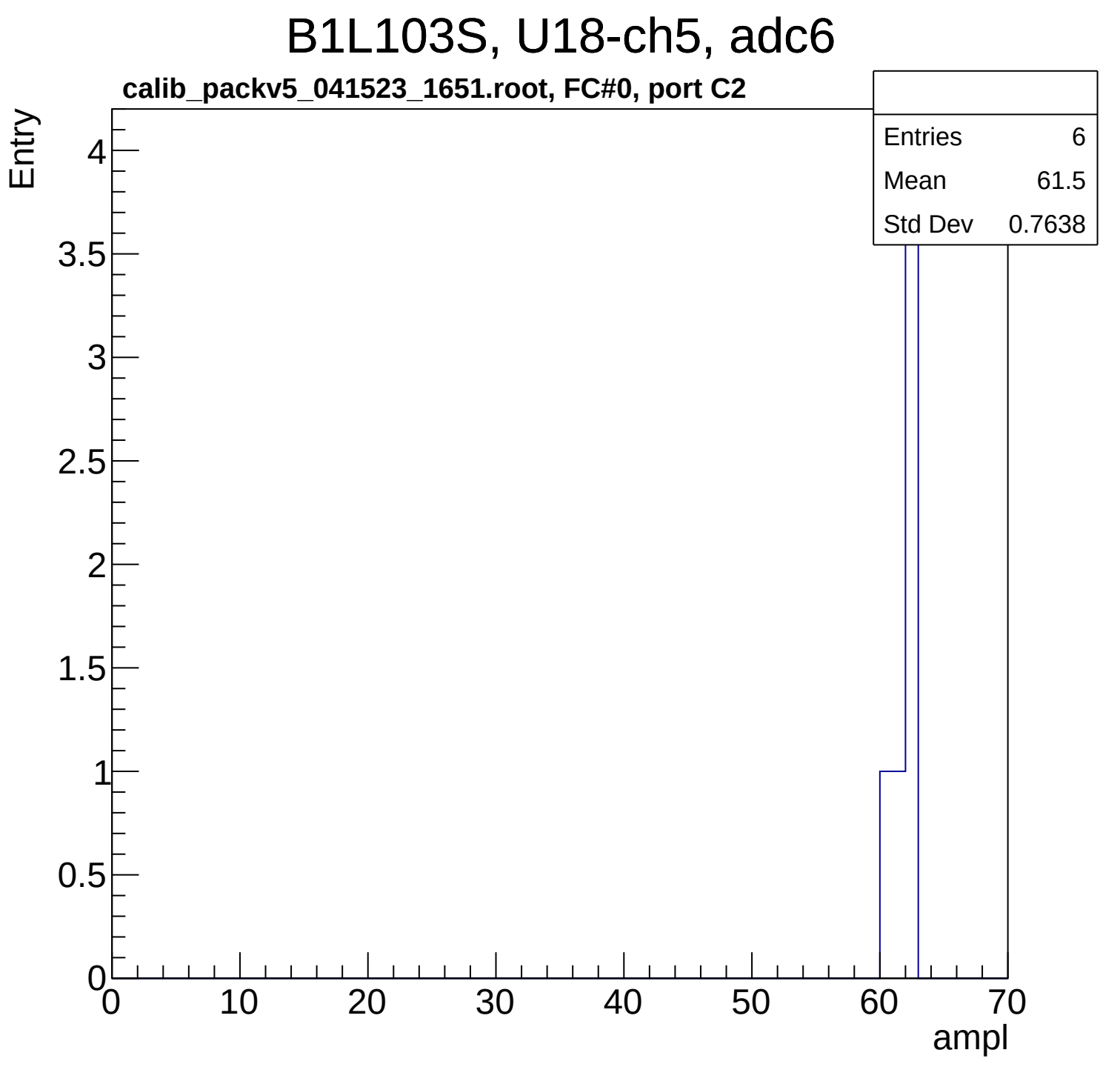
B1L103S, U18-ch5, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 61.5
Std Dev 0.7638
Entry
ampl
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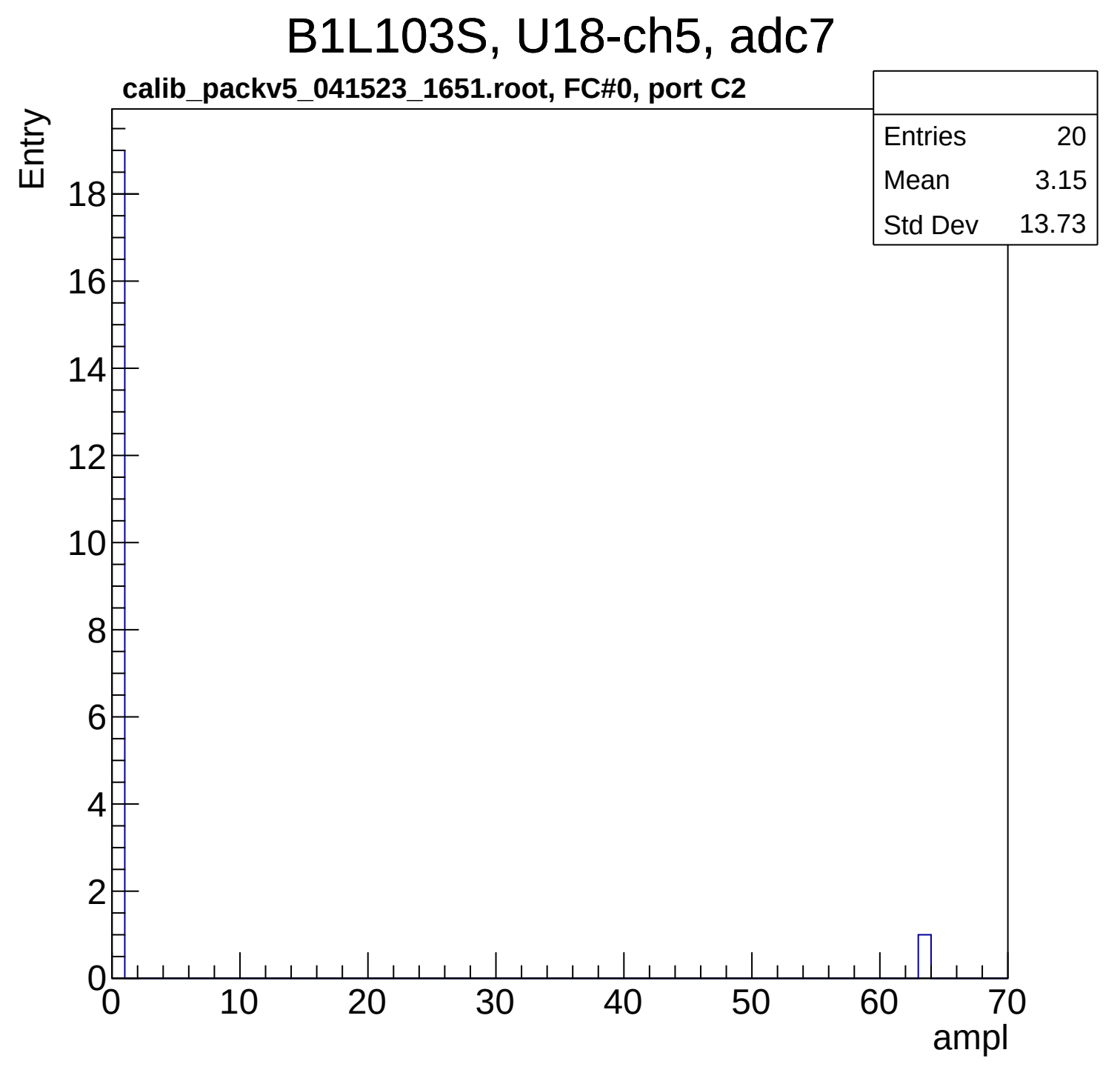
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U18-ch5, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
0
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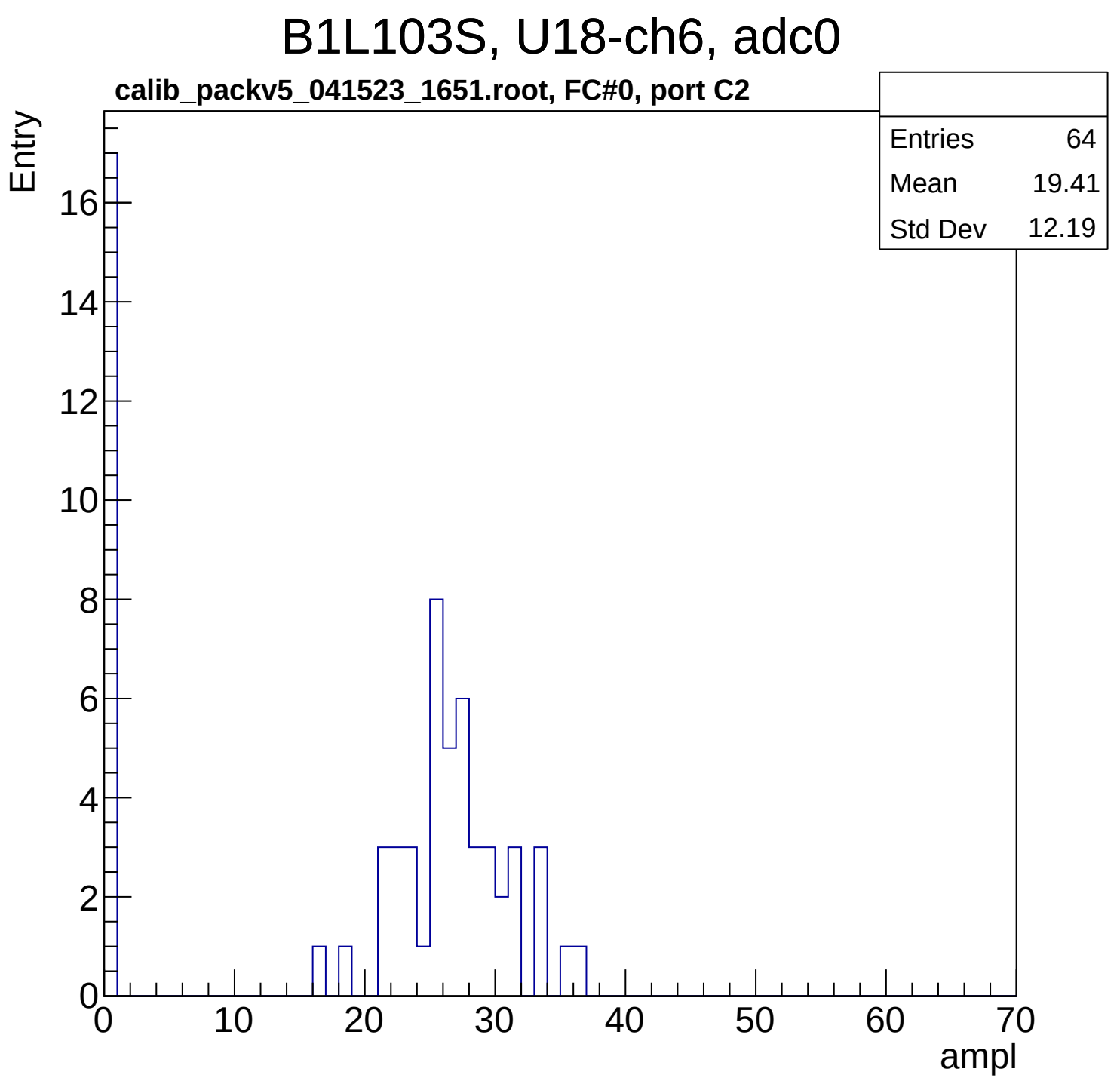
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch6, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 19.41
Std Dev 12.19
Entry
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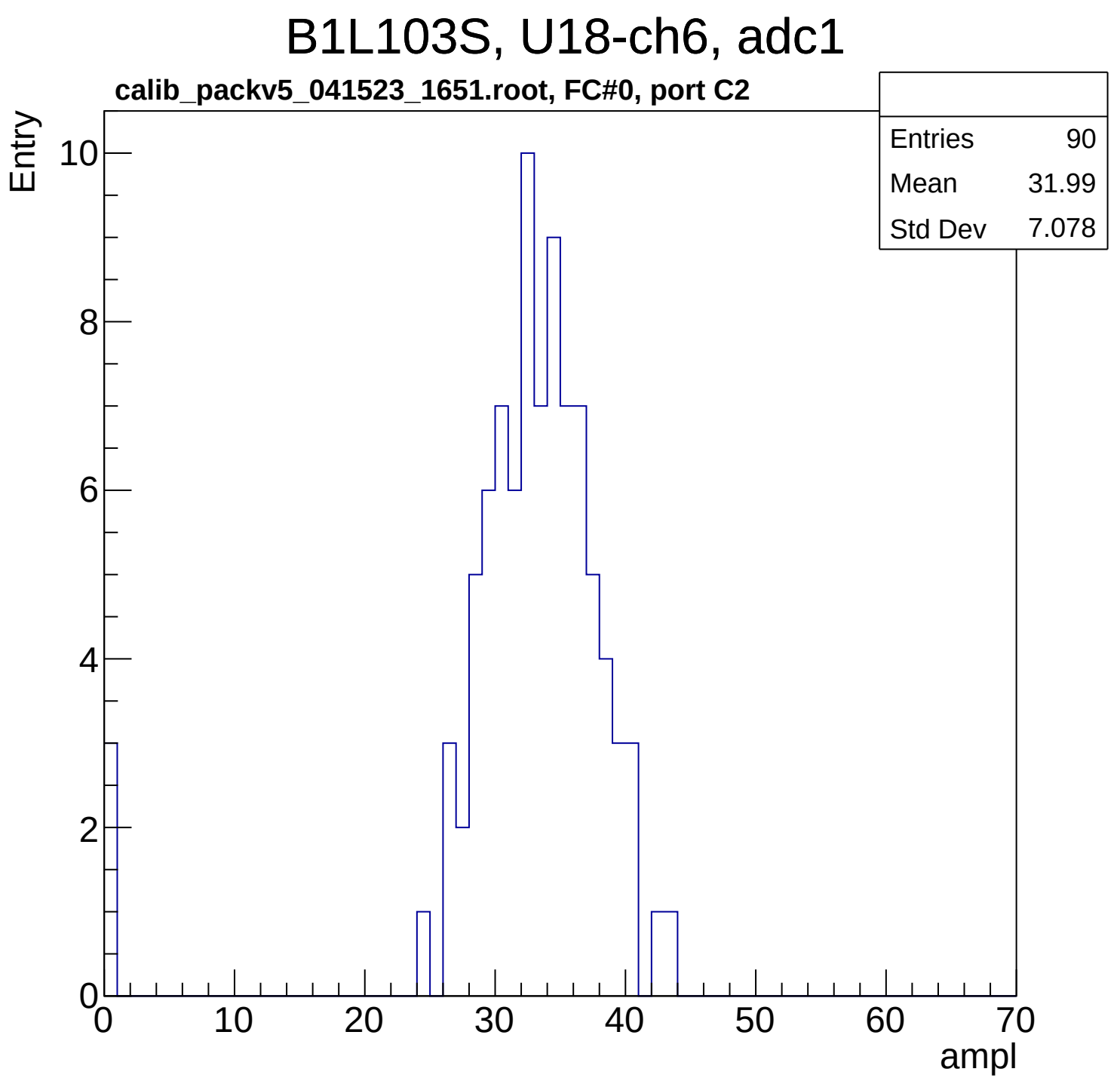
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch6, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 90
Mean 31.99
Std Dev 7.078
Entry
ampl
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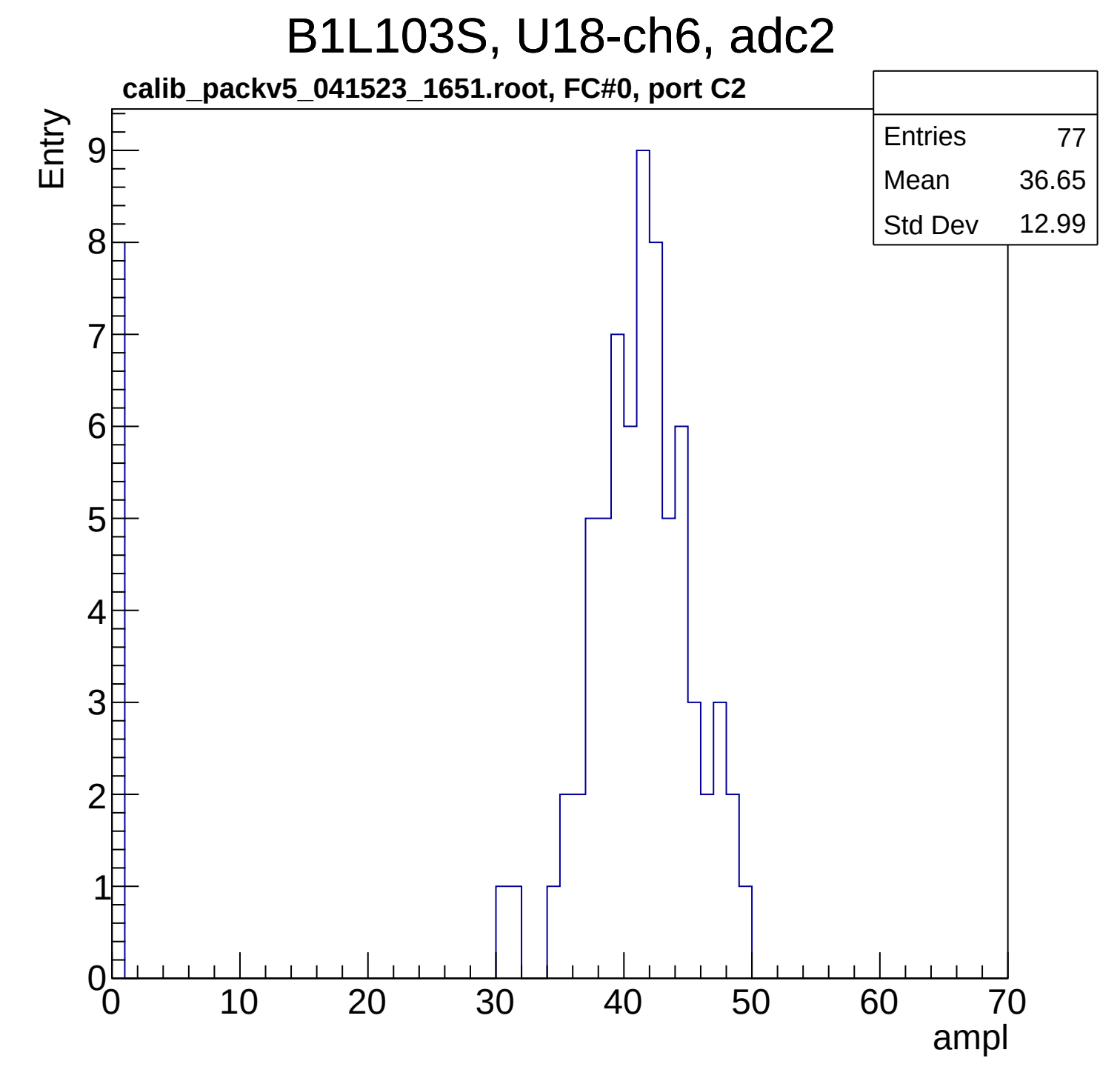
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U18-ch6, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 36.65
Std Dev 12.99
Entry
ampl
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3
4
5
6
7
8
9
0
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20
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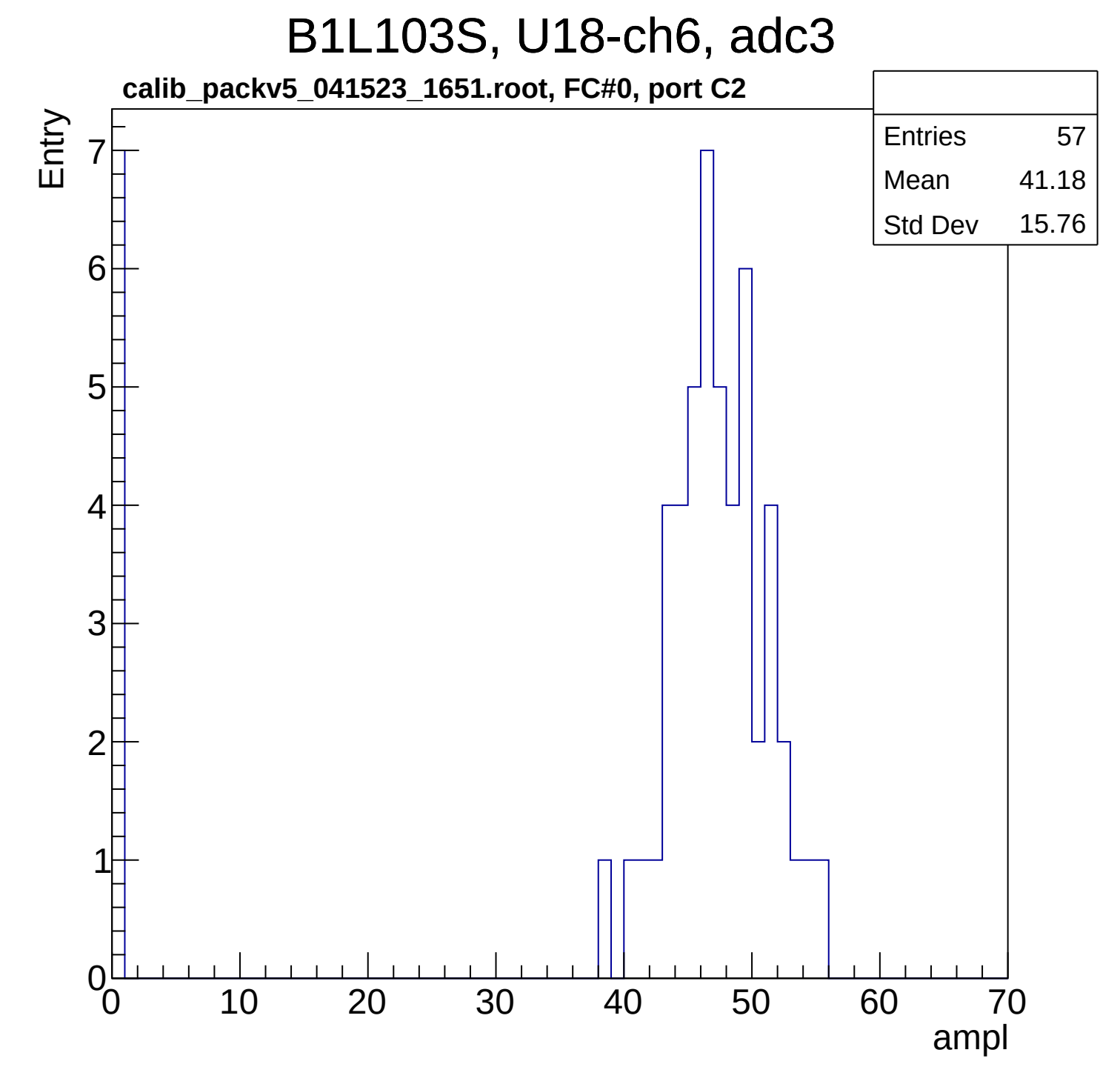
40
50
60
70


B1L103S, U18-ch6, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 41.18
Std Dev 15.76
Entry
ampl
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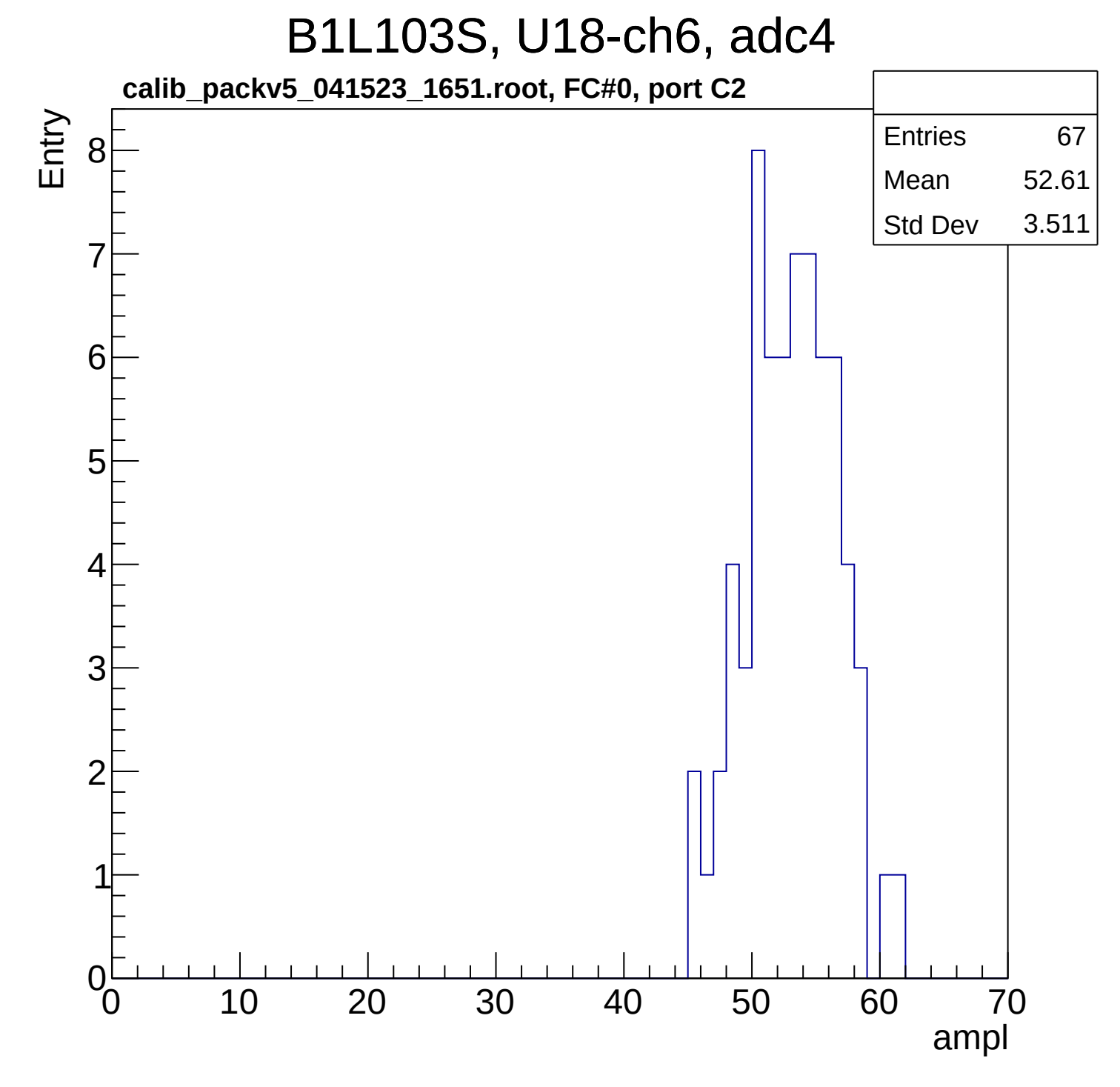
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U18-ch6, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 52.61
Std Dev 3.511
Entry
ampl
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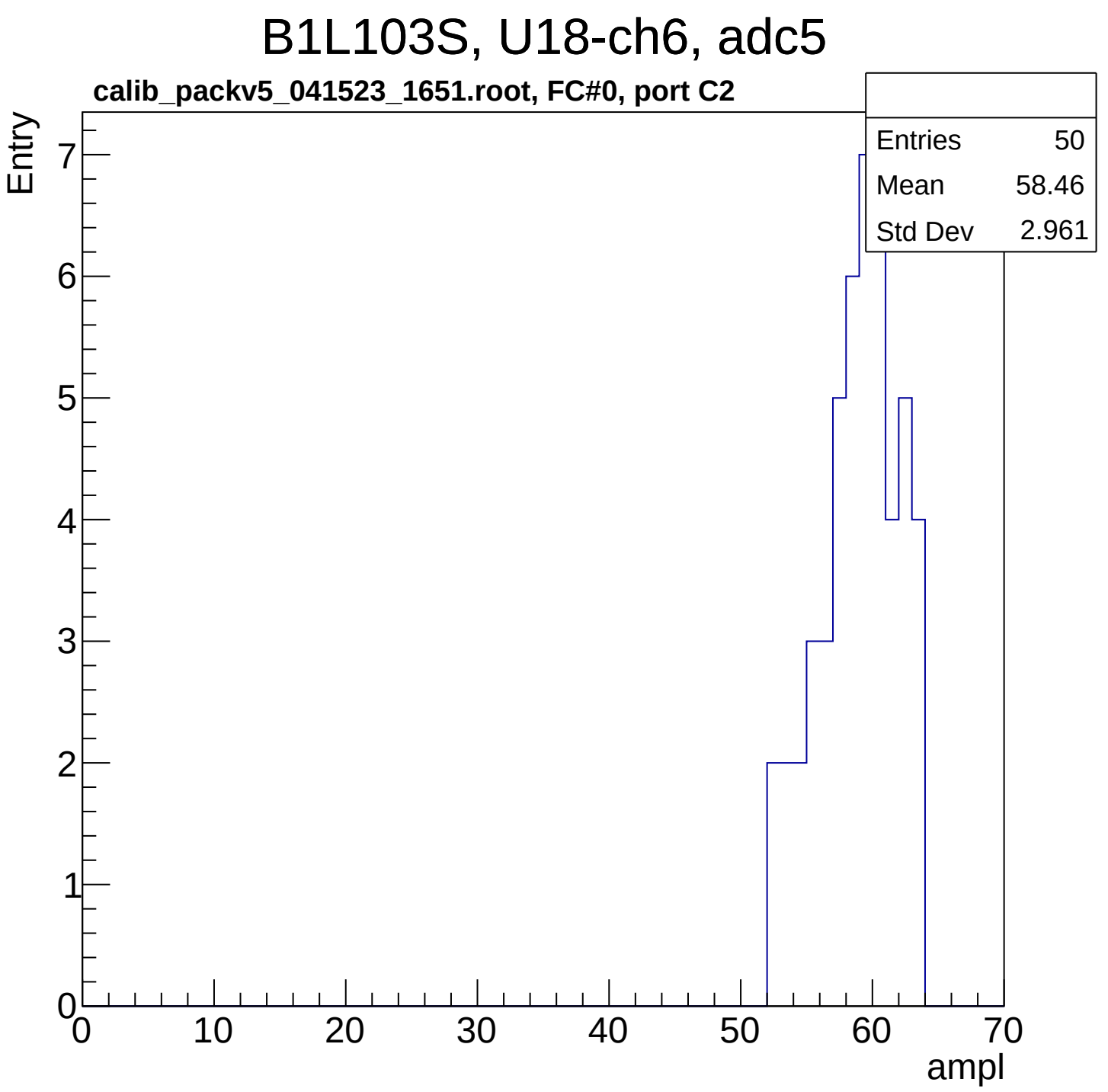
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch6, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 58.46
Std Dev 2.961
Entry
ampl
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1
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3
4
5
6
7
0
10
20
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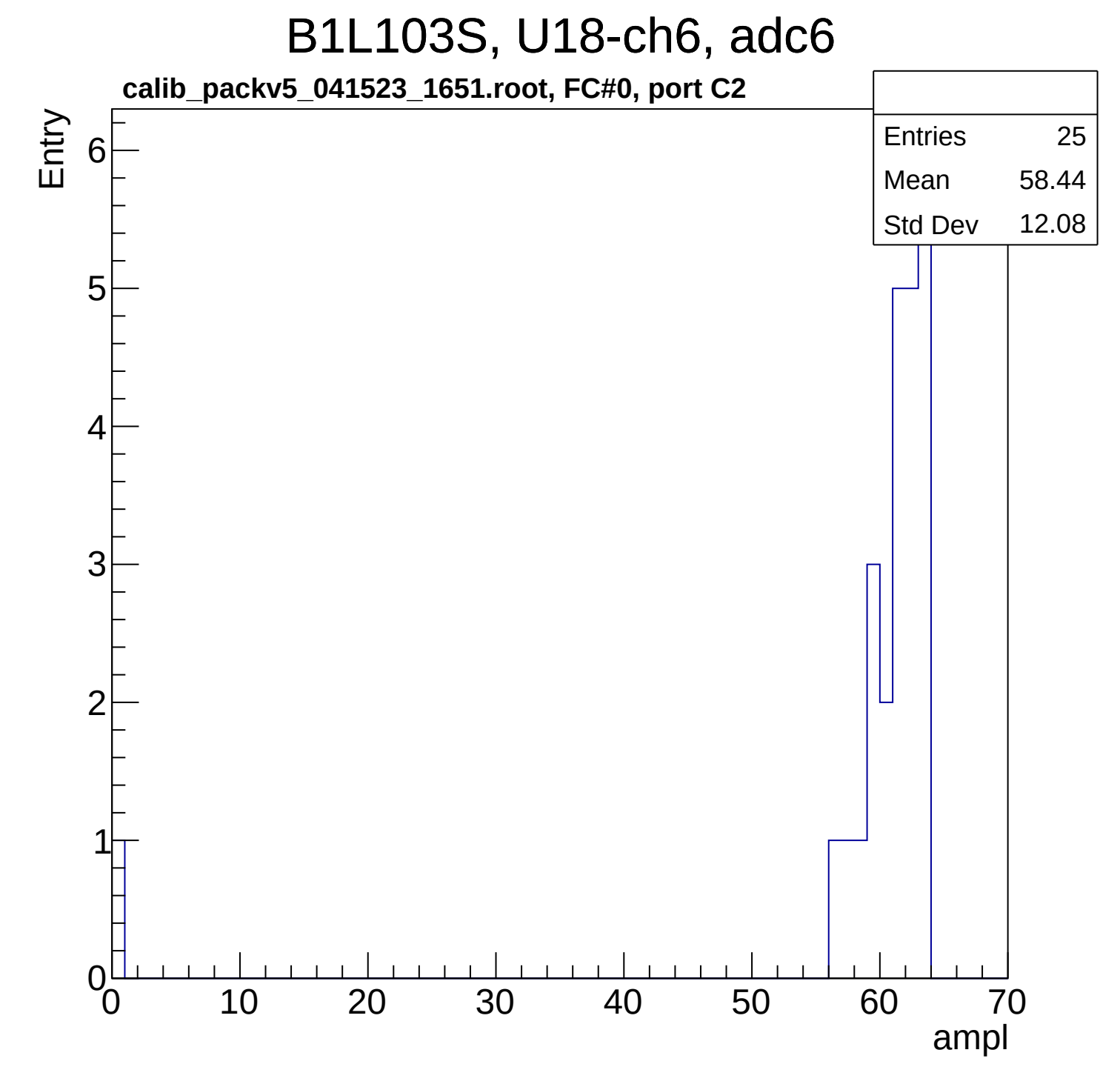
40
50
60
70


B1L103S, U18-ch6, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 25
Mean 58.44
Std Dev 12.08
Entry
ampl
0
1
2
3
4
5
6
0
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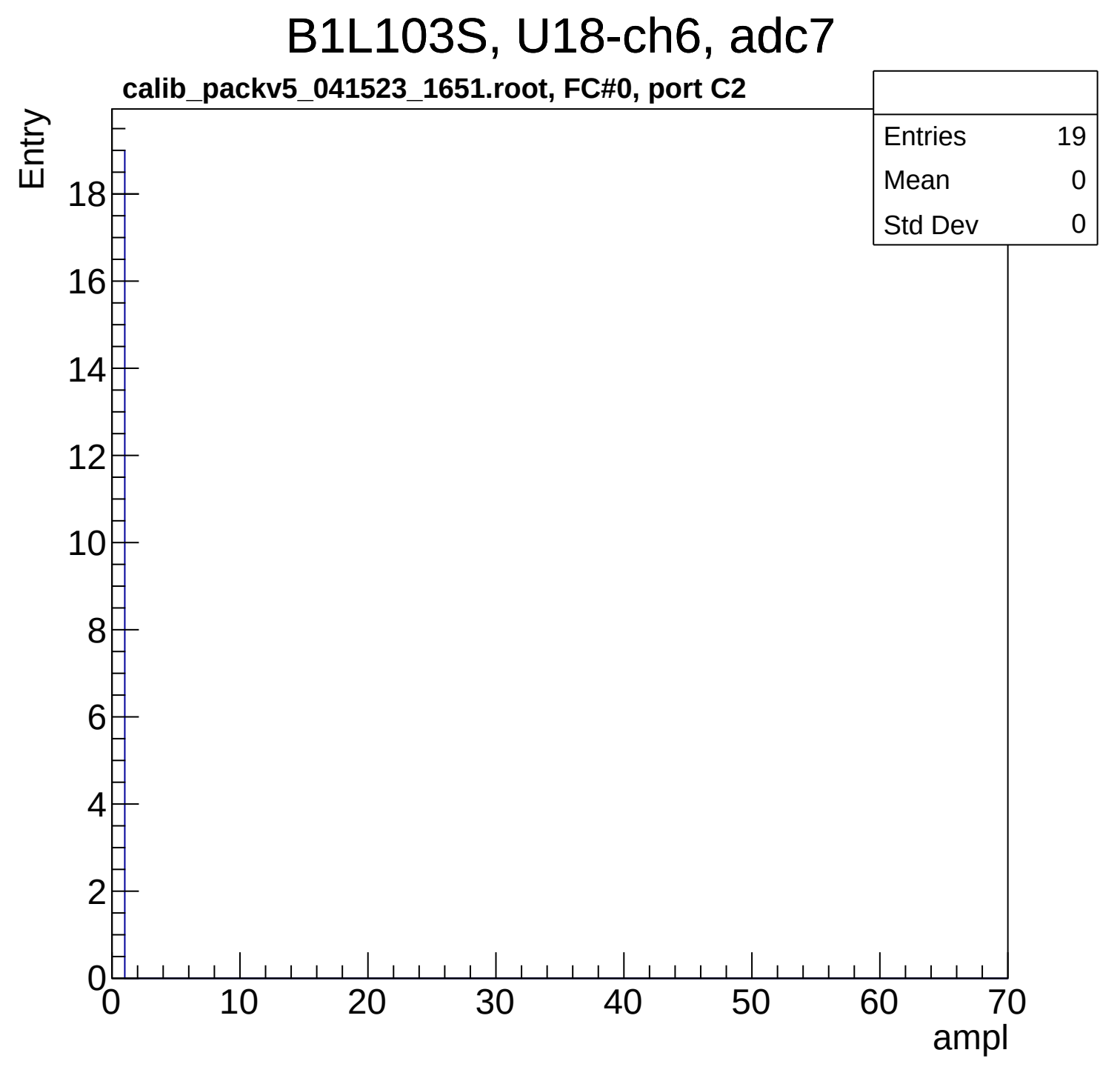
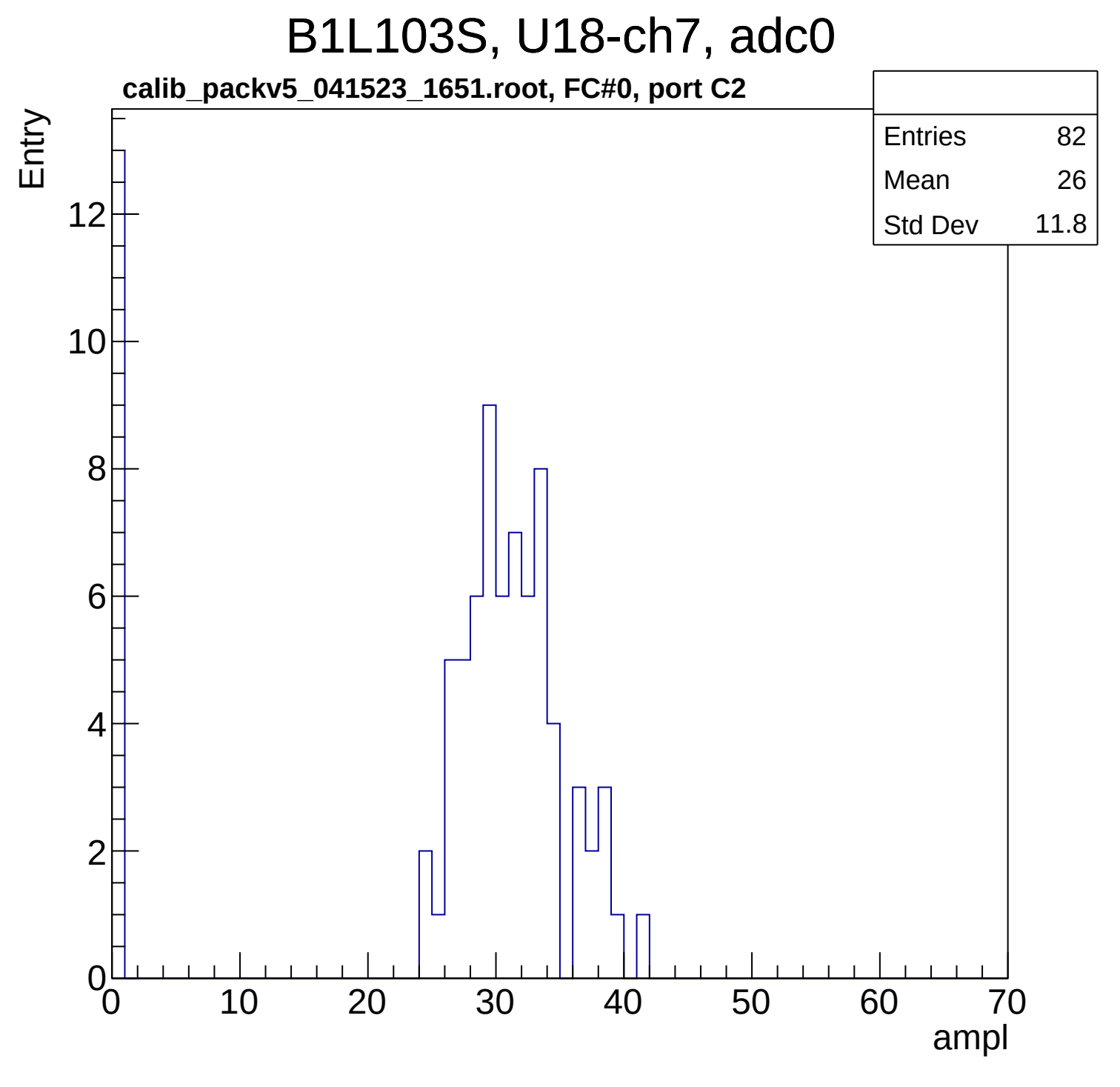
20
30
40
50
60
70


B1L103S, U18-ch6, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch7, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 26
Std Dev 11.8
Entry
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8
10
12
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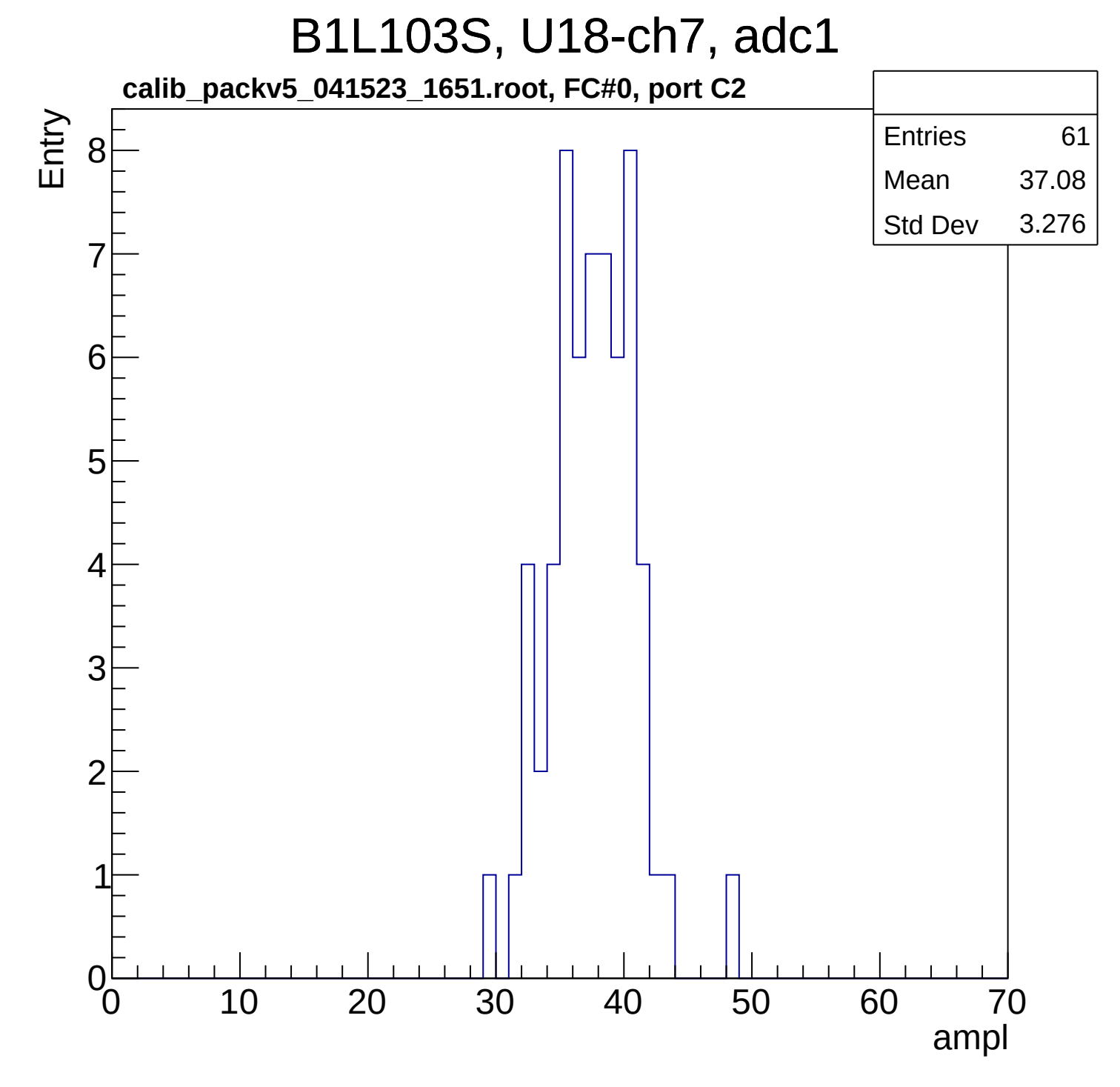
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch7, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 37.08
Std Dev 3.276
Entry
ampl
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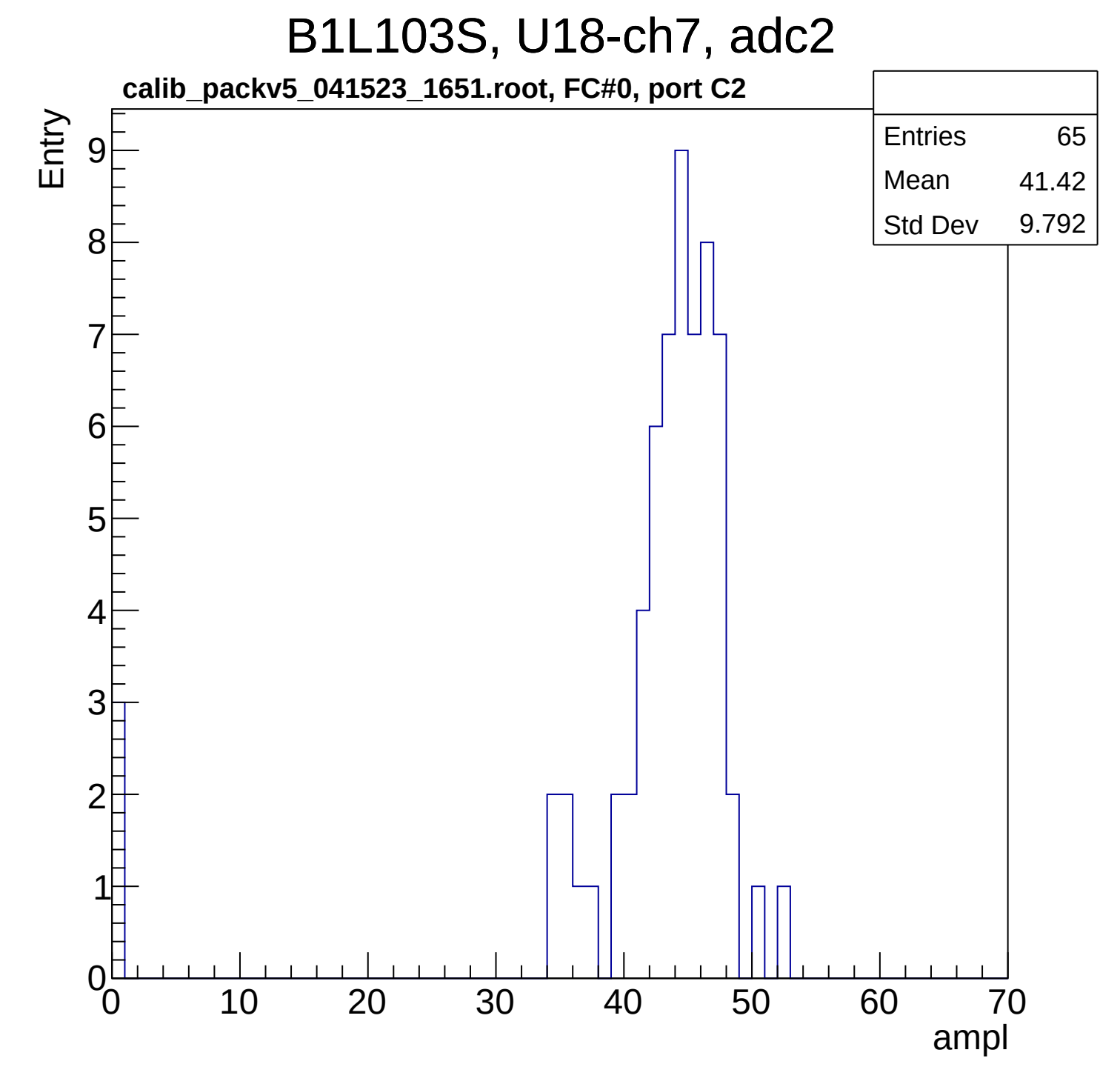
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch7, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 41.42
Std Dev 9.792
Entry
ampl
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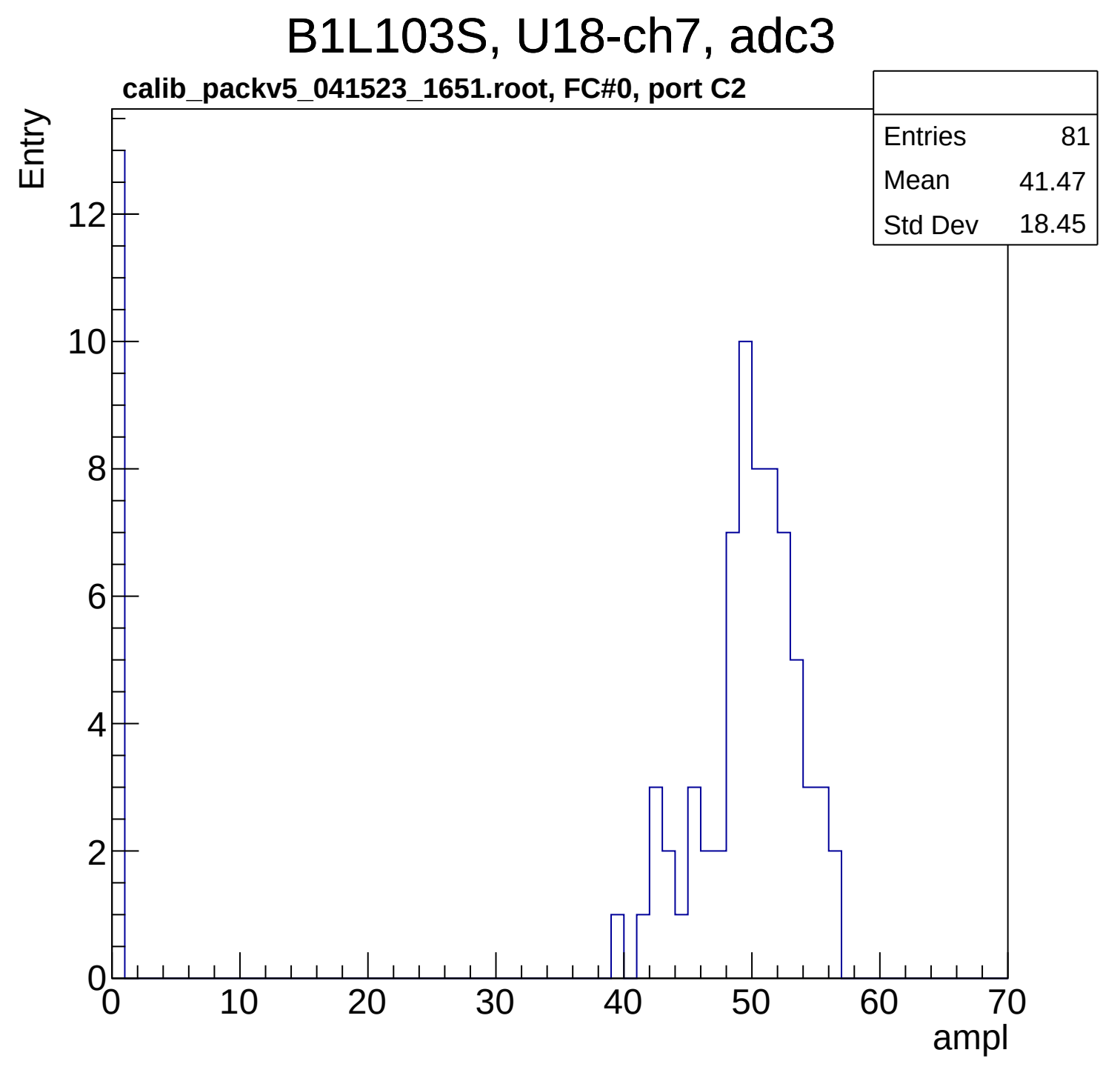
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U18-ch7, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 41.47
Std Dev 18.45
Entry
ampl
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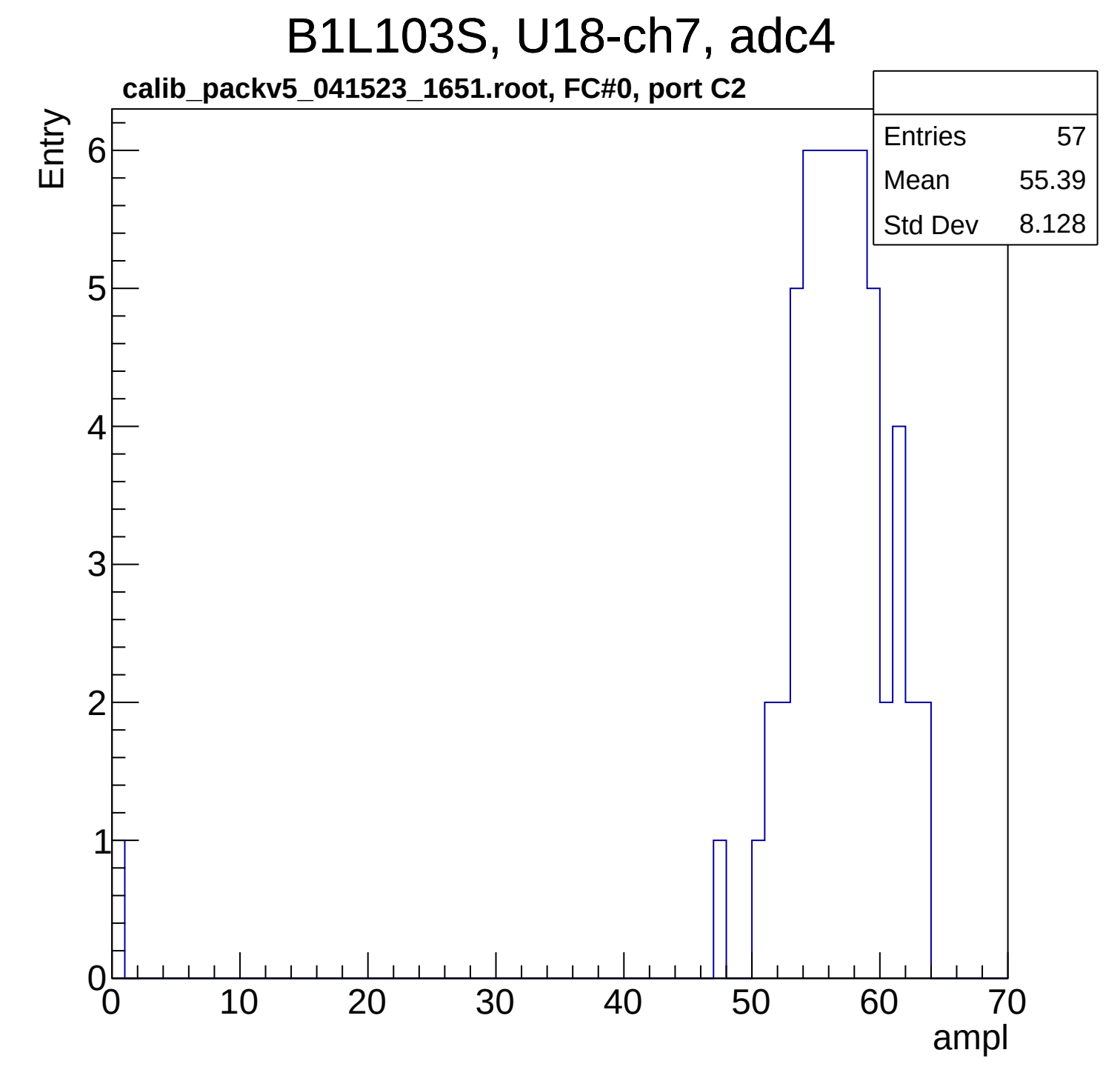
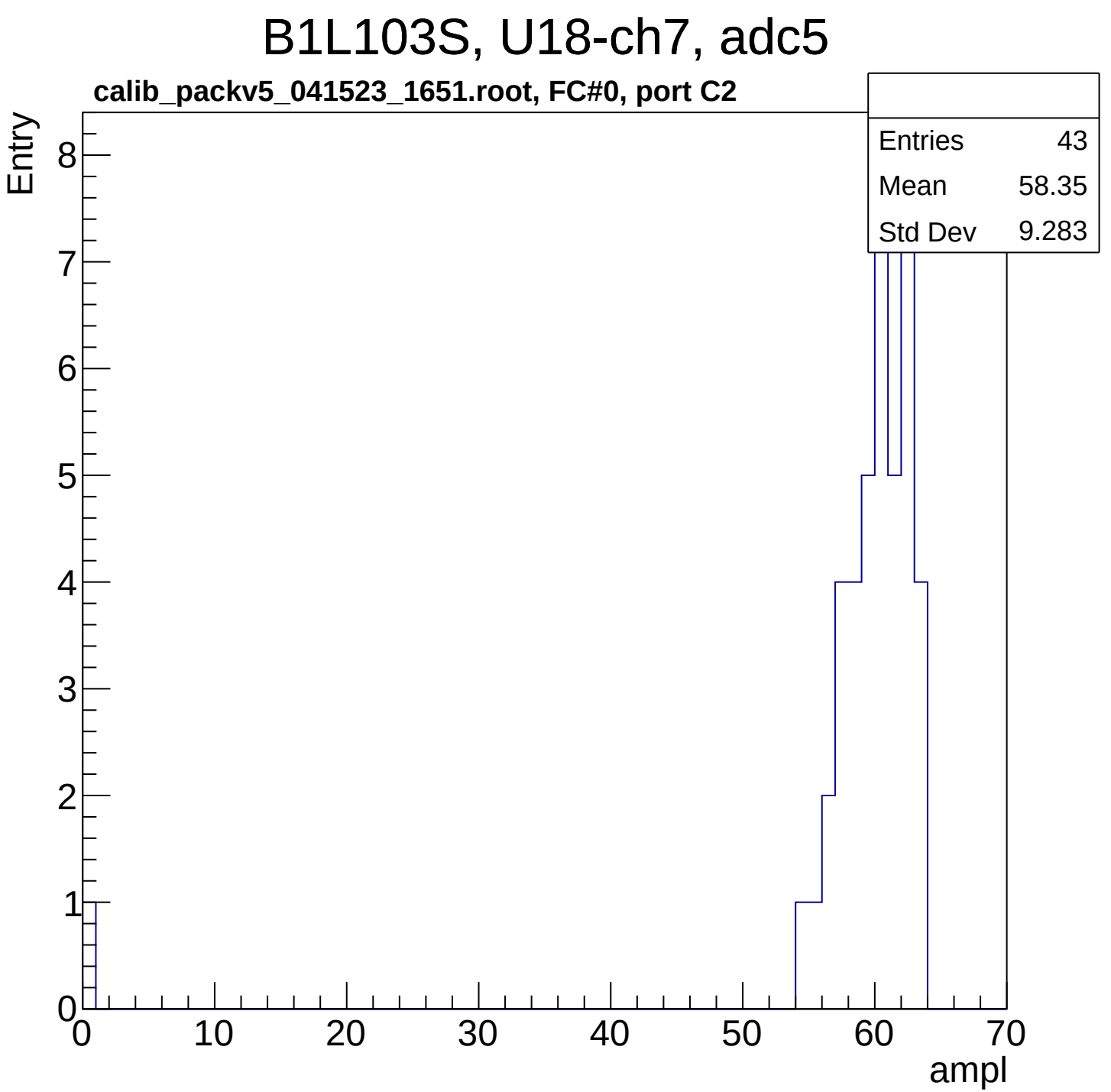
4
6
8
10
12
0
10
20
30
40
50
60
70


B1L103S, U18-ch7, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 55.39
Std Dev 8.128
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U18-ch7, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 43
Mean 58.35
Std Dev 9.283
Entry
ampl
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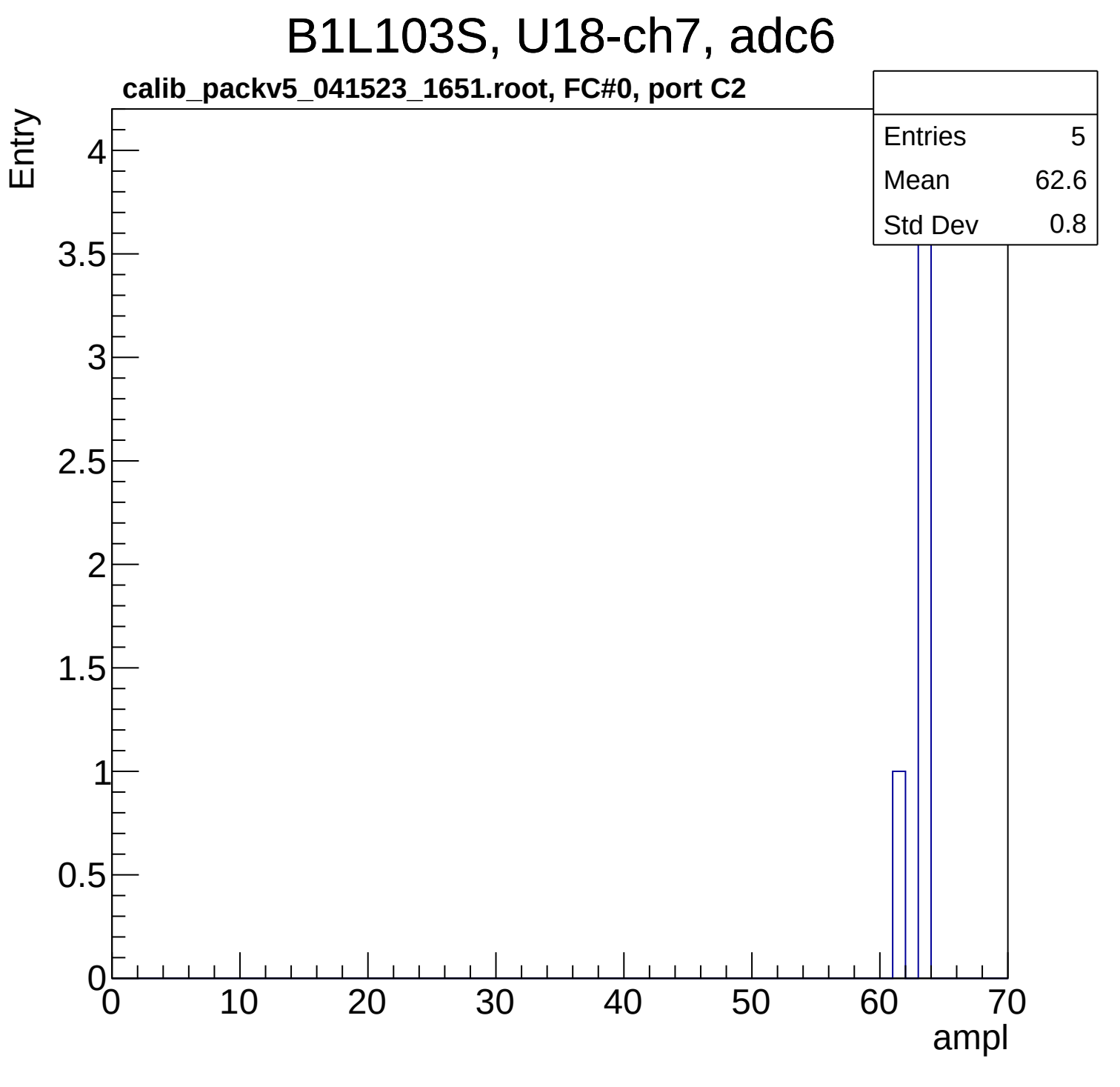
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch7, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 5
Mean 62.6
Std Dev 0.8
Entry
ampl
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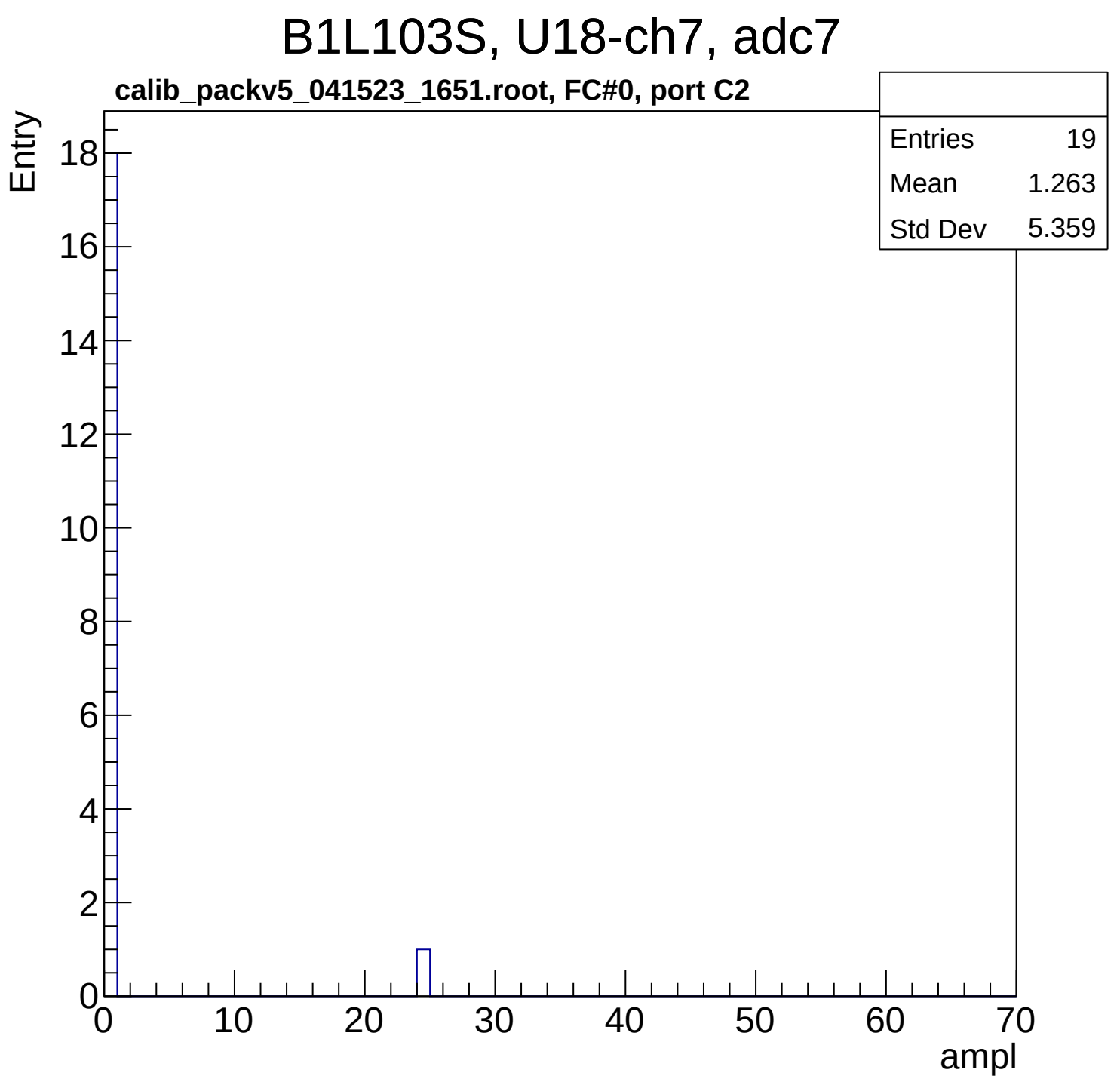
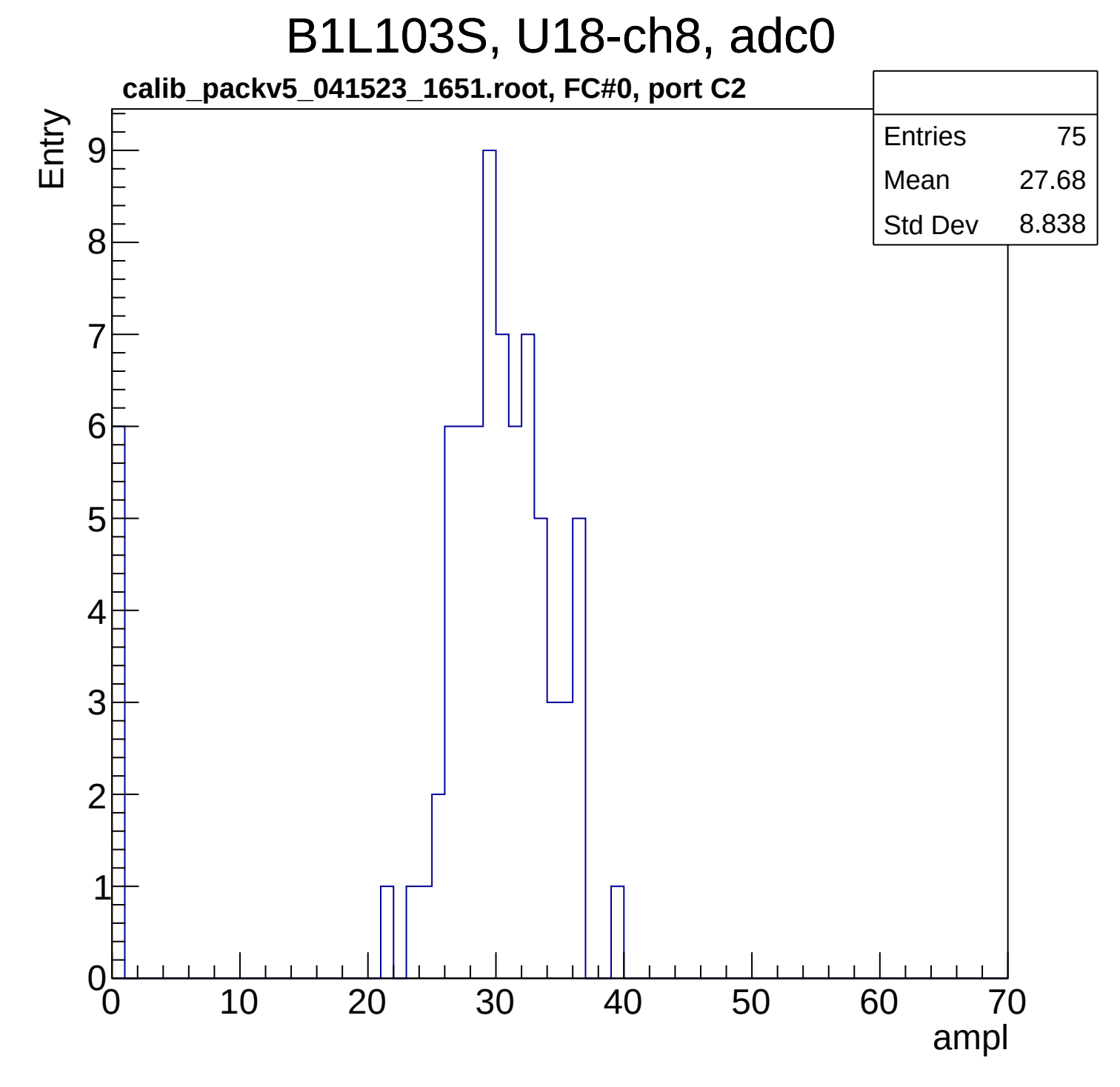
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U18-ch7, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.263
Std Dev 5.359
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch8, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 27.68
Std Dev 8.838
Entry
ampl
0
1
2
3
4
5
6
7
8
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0
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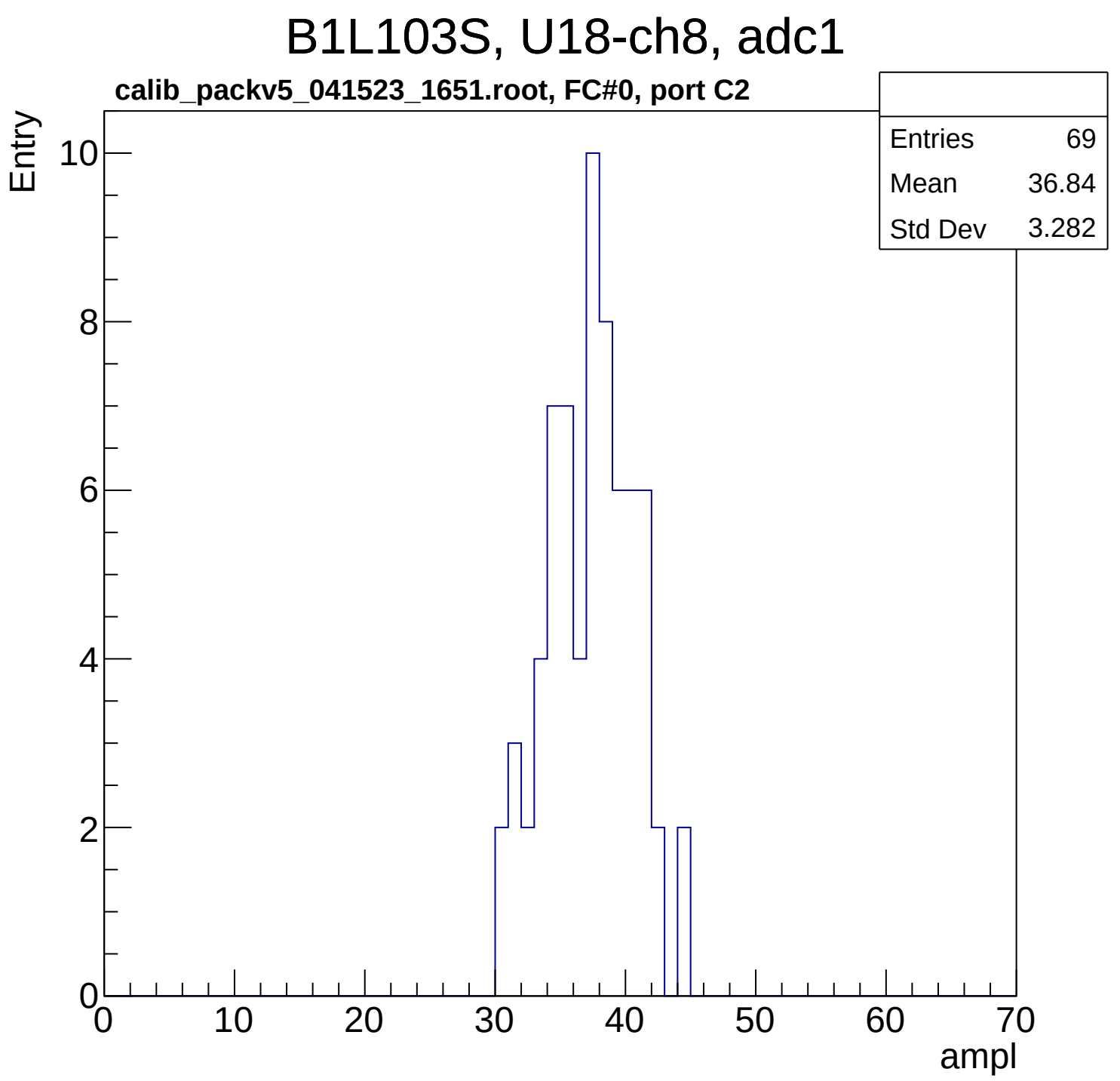
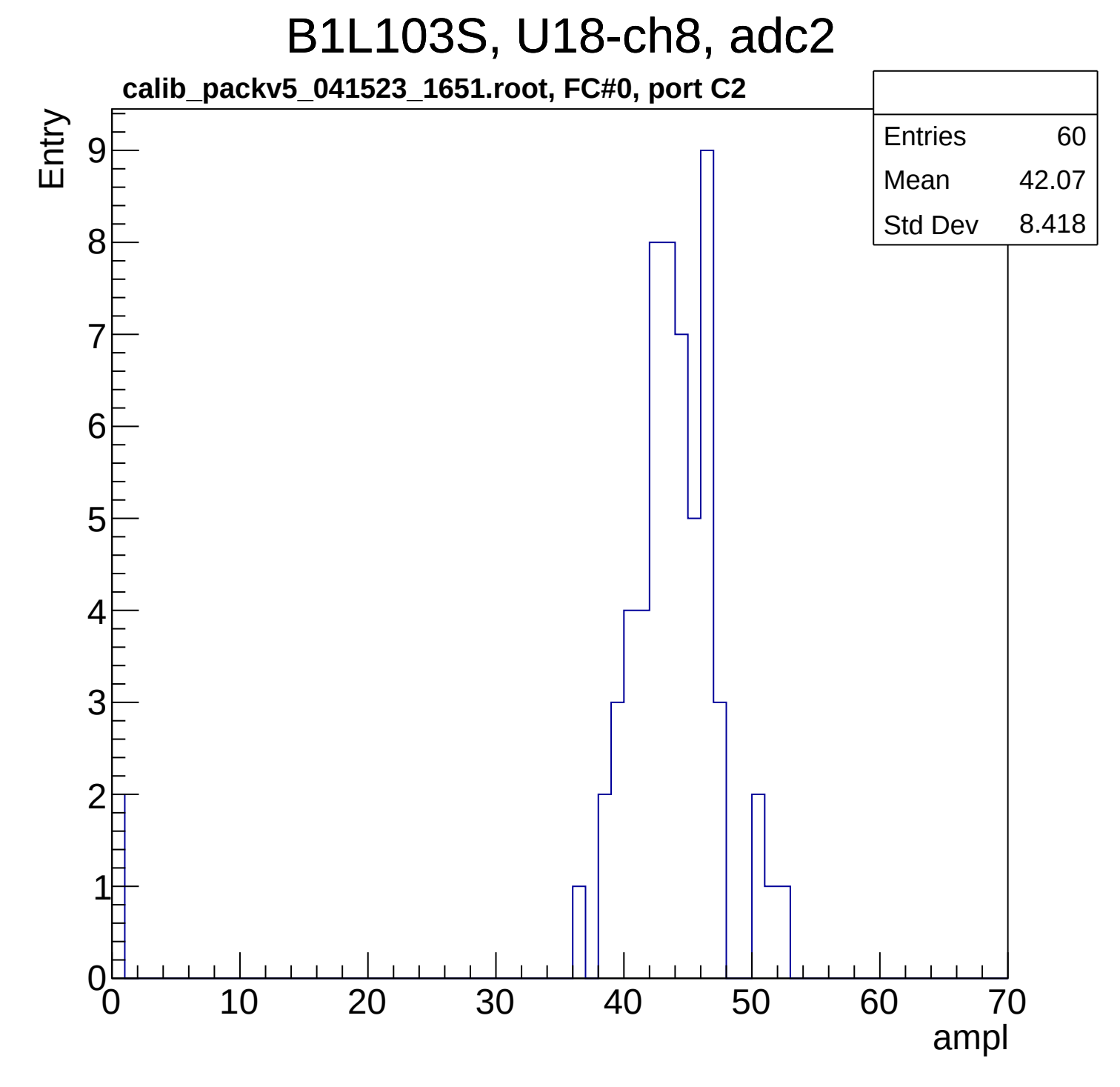
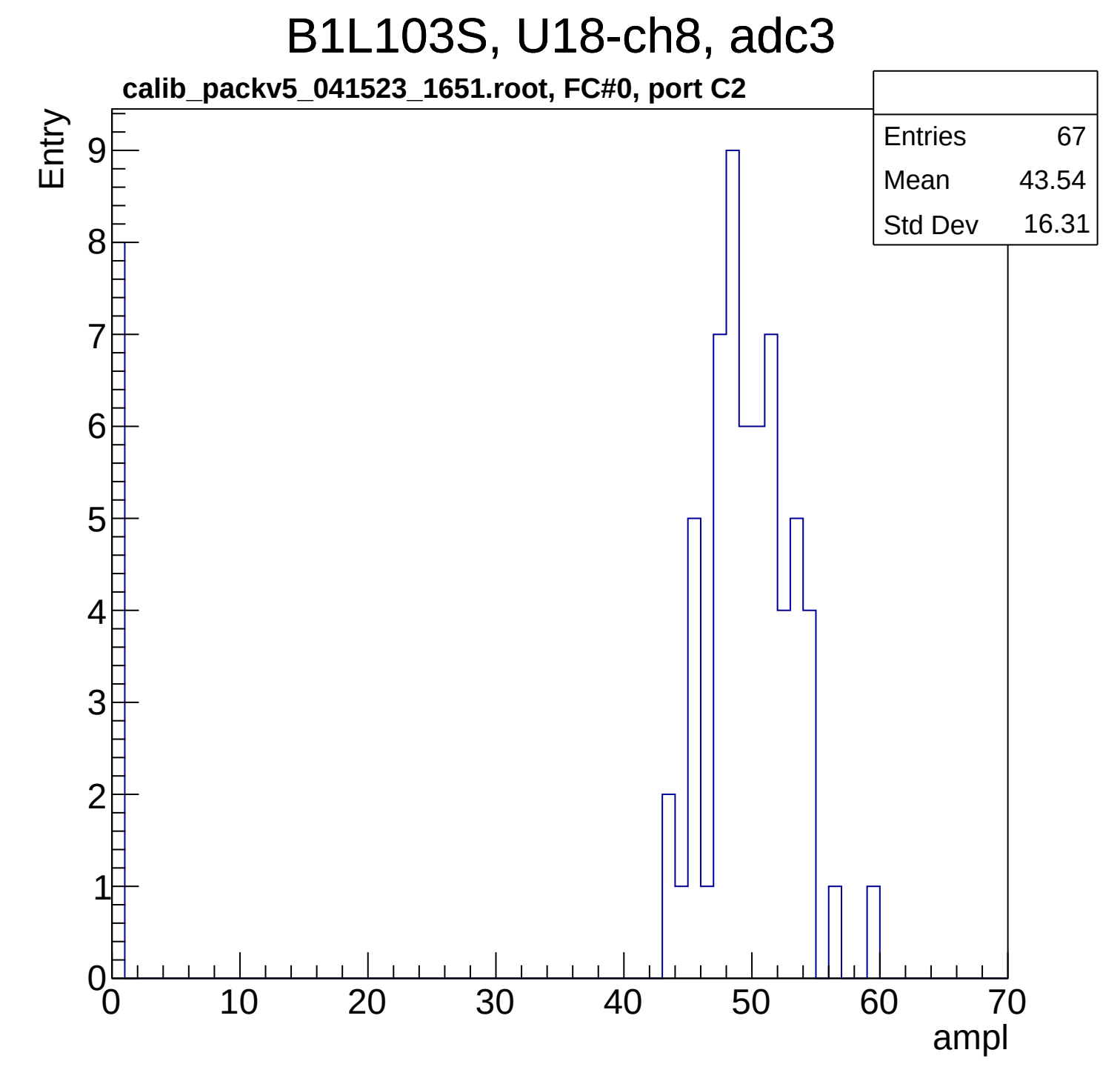
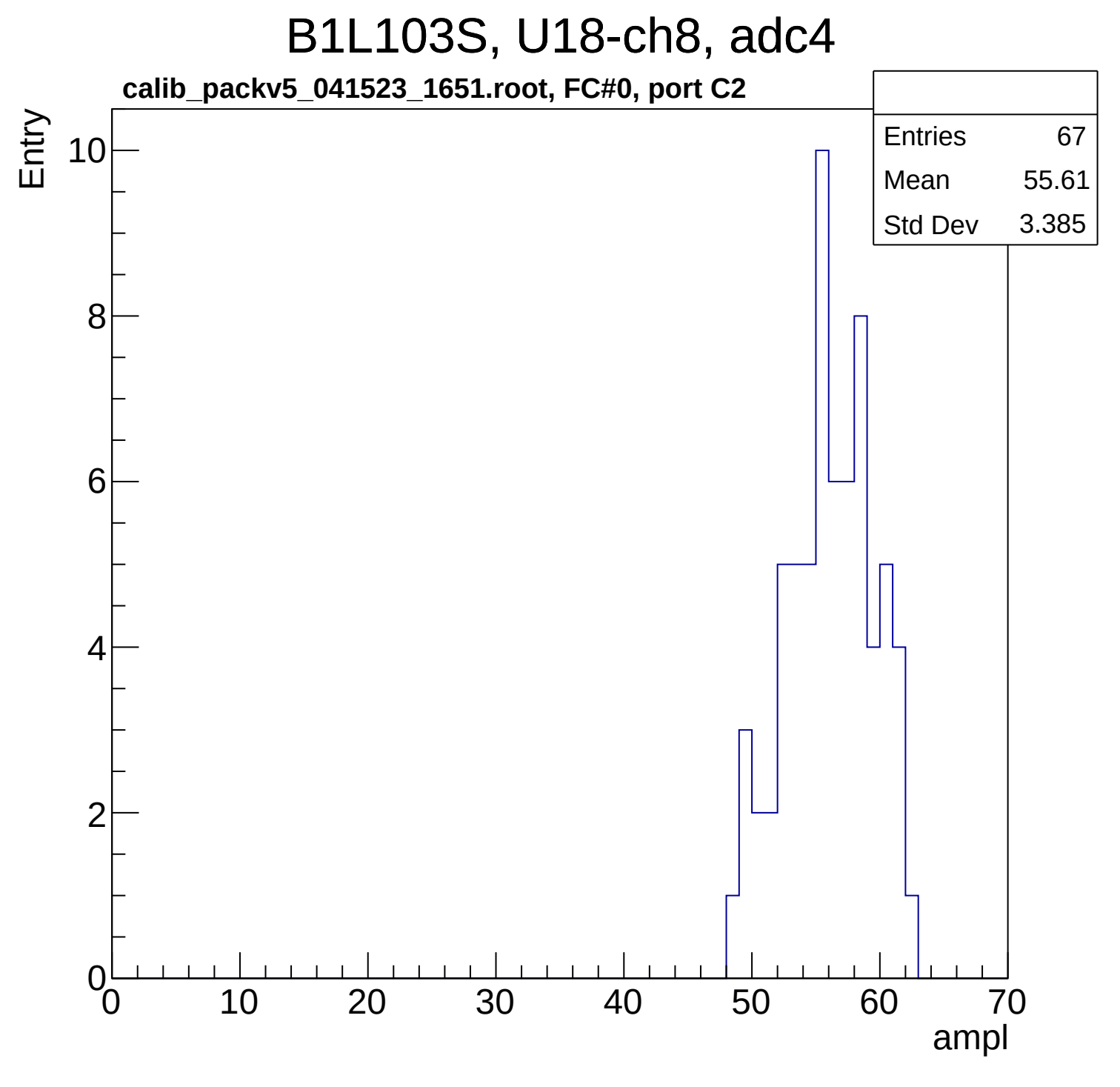
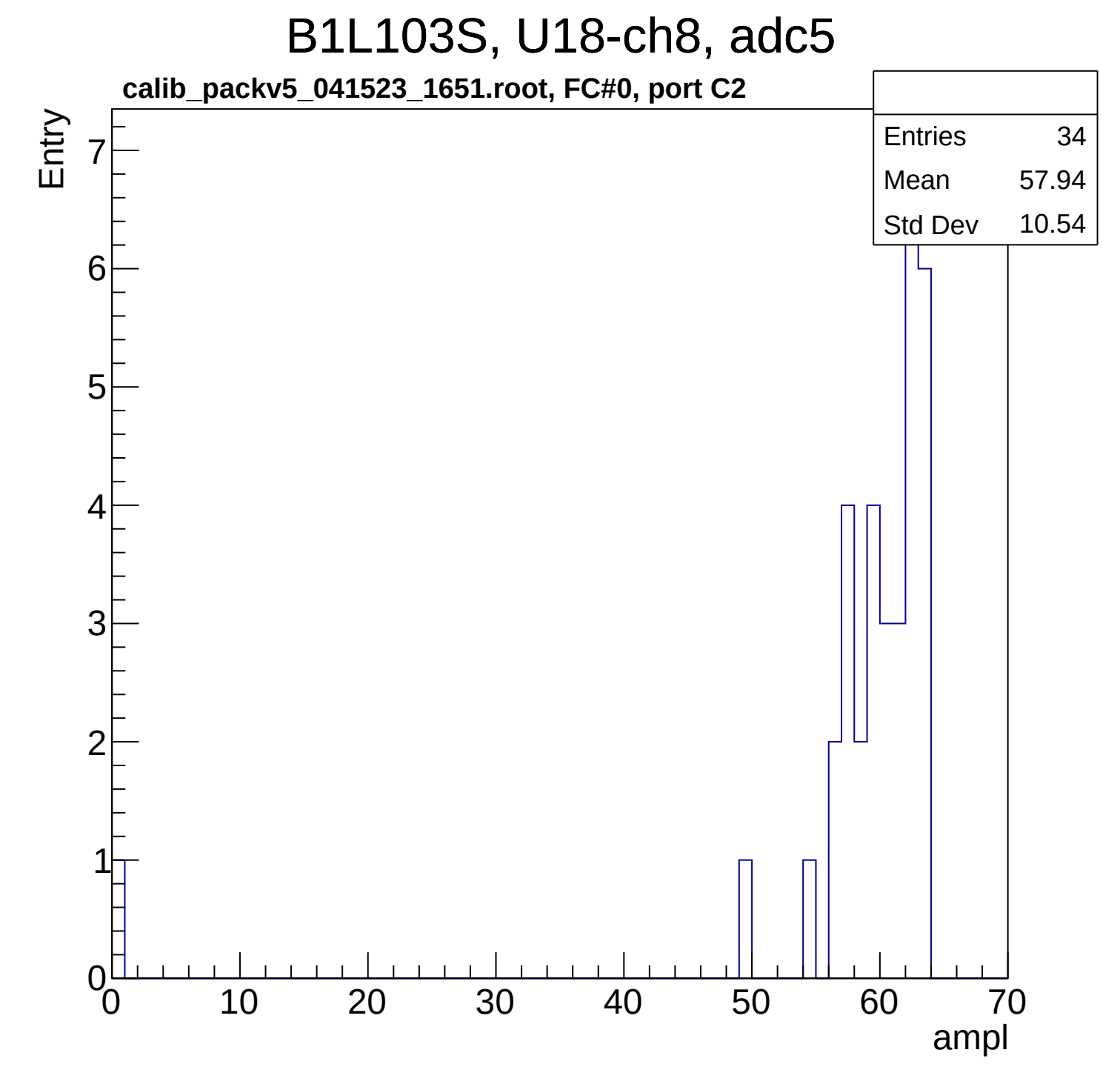
40
50
60
70

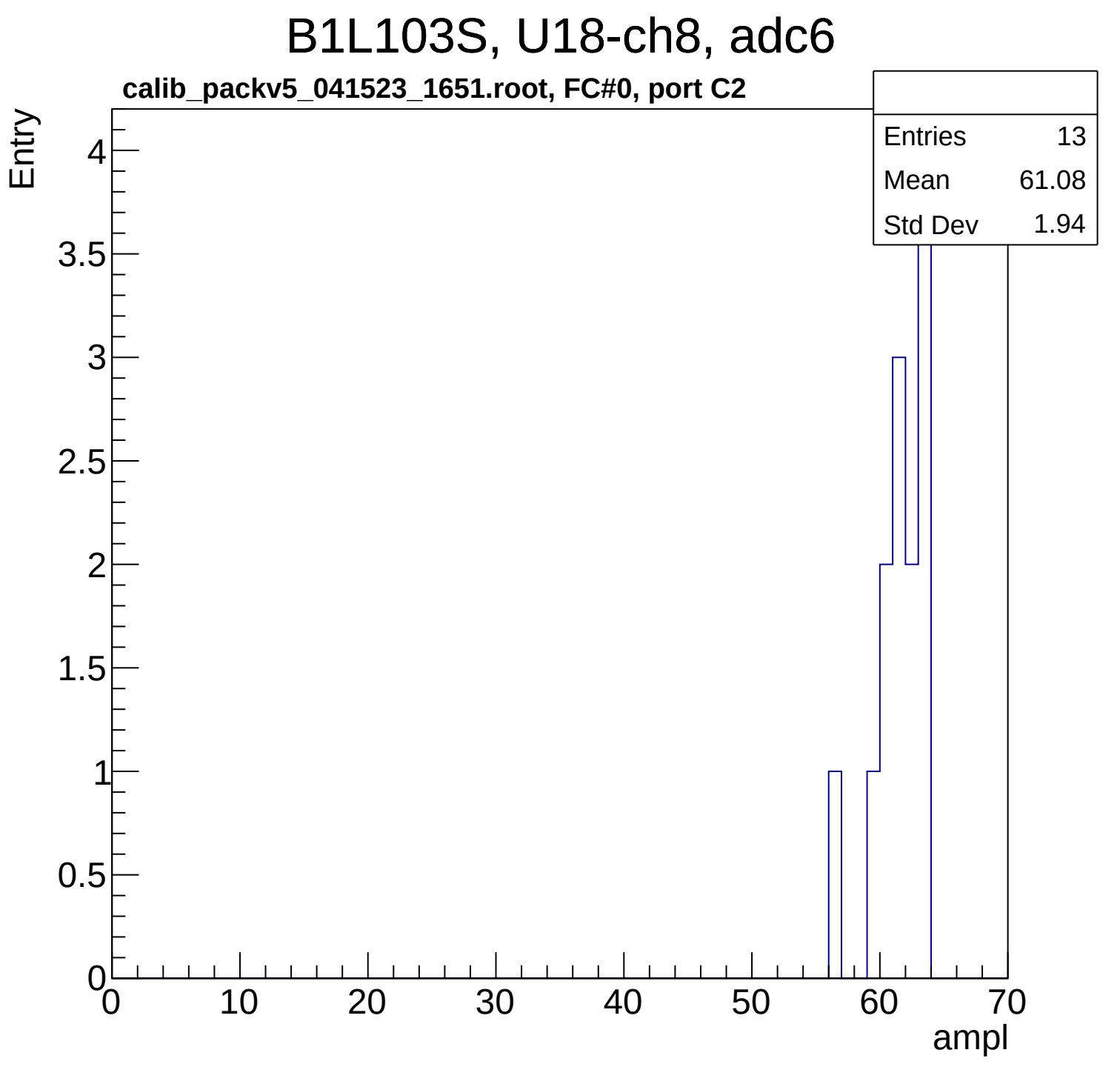

B1L103S, U18-ch8, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 36.84
Std Dev 3.282
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

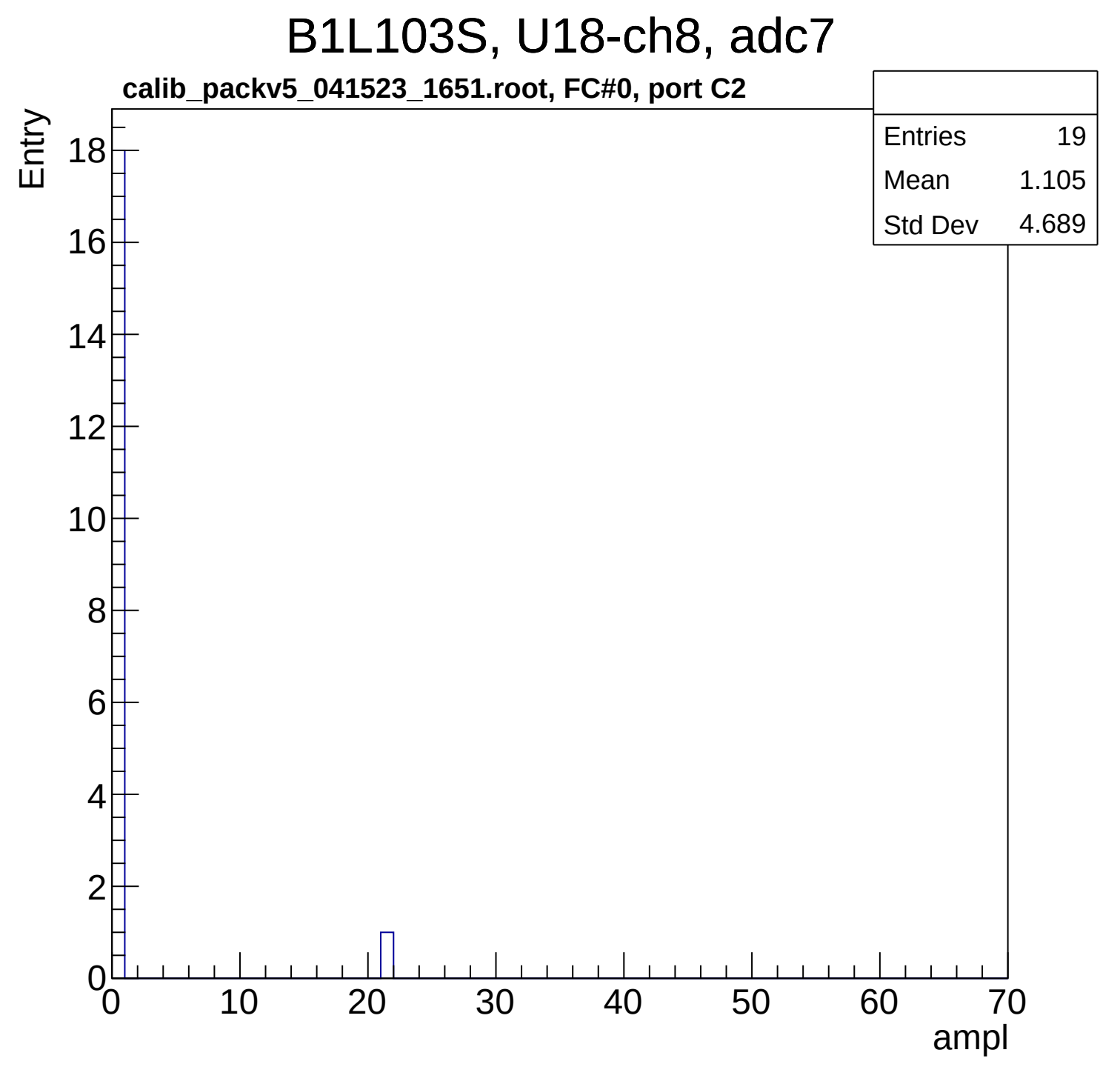

B1L103S, U18-ch8, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 42.07
Std Dev 8.418
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U18-ch8, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 43.54
Std Dev 16.31
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U18-ch8, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 55.61
Std Dev 3.385
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U18-ch8, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 34
Mean 57.94
Std Dev 10.54
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U18-ch8, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 13
Mean 61.08
Std Dev 1.94
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U18-ch8, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.105
Std Dev 4.689
Entry
ampl
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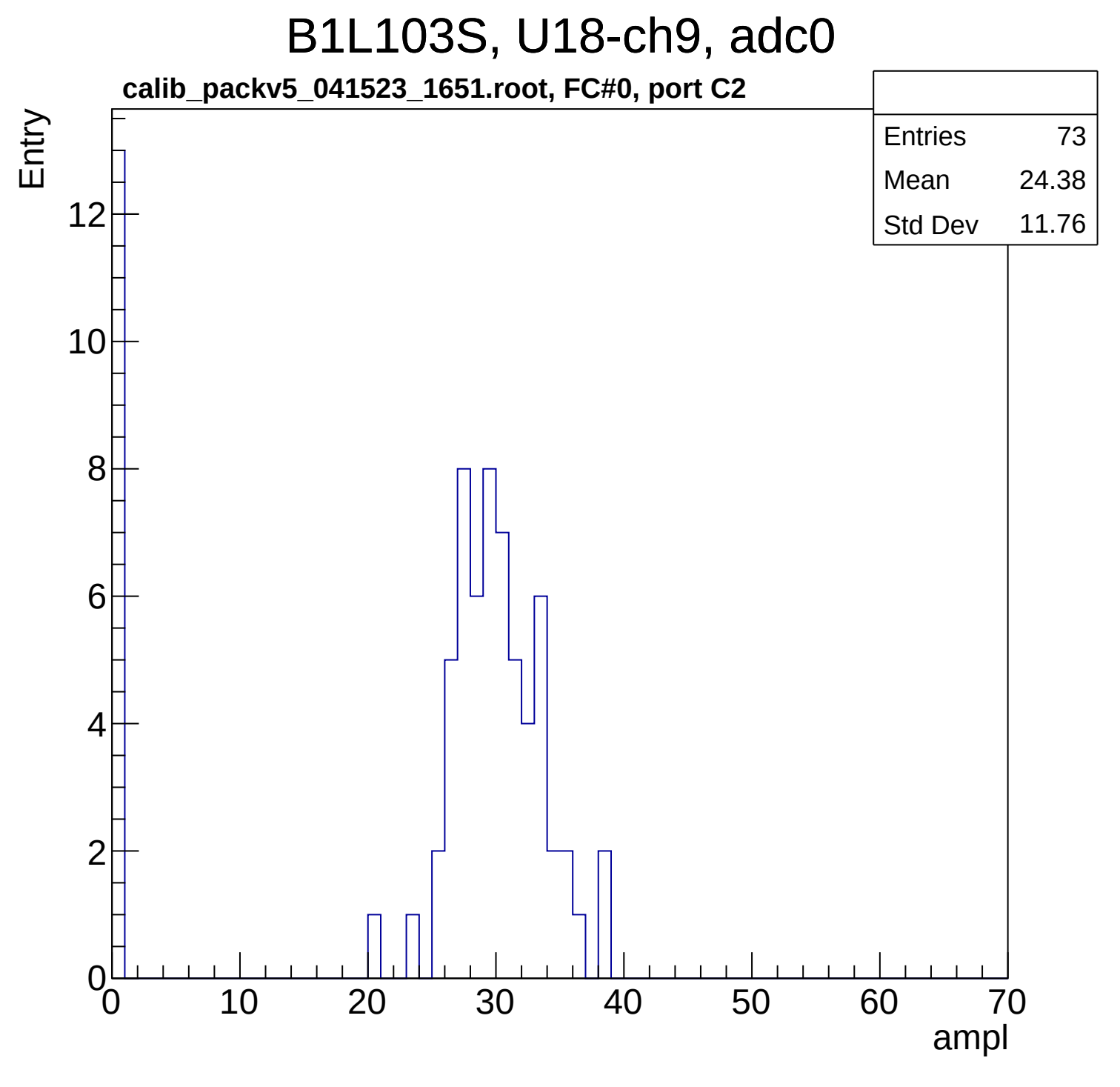
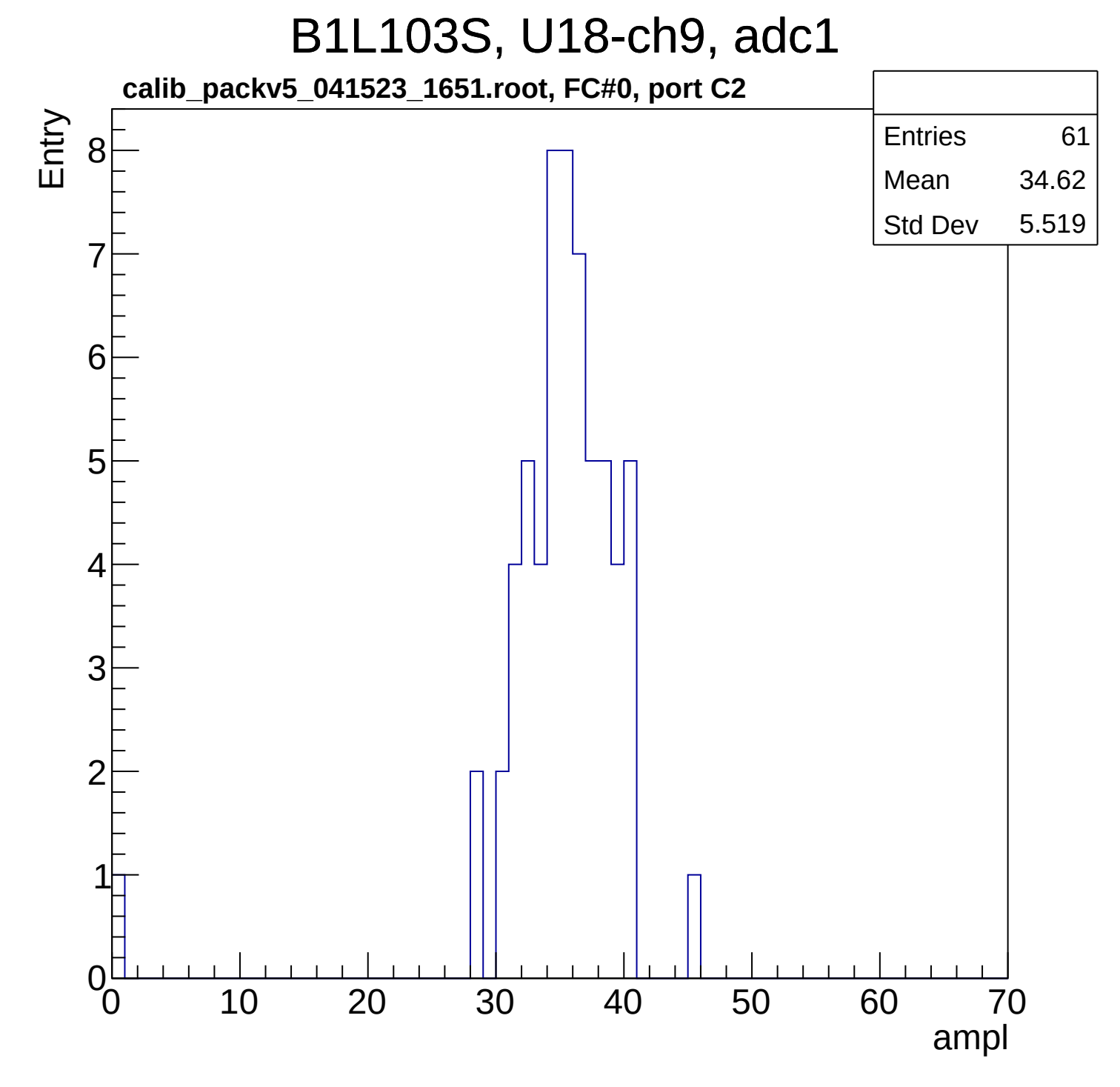
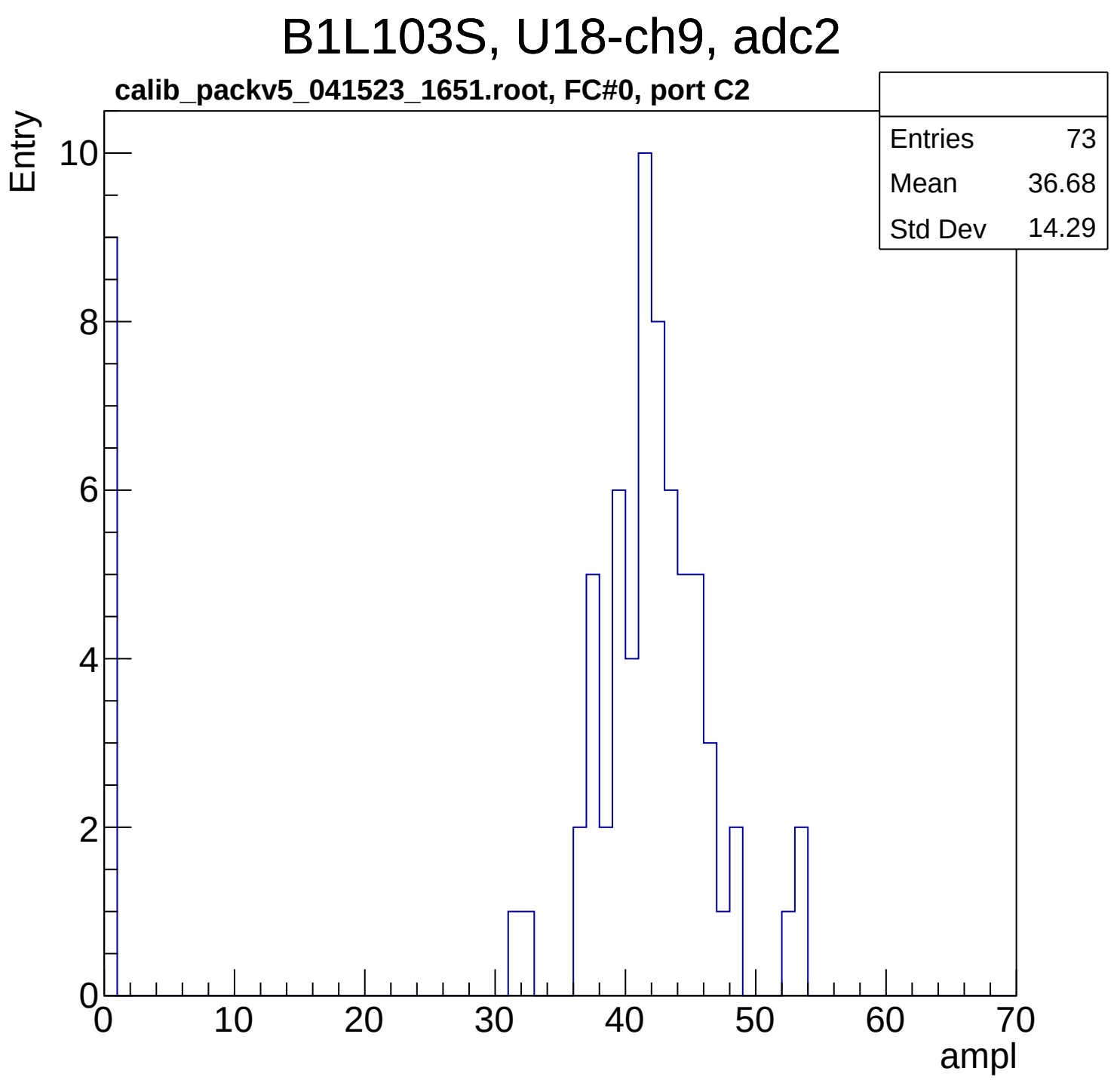
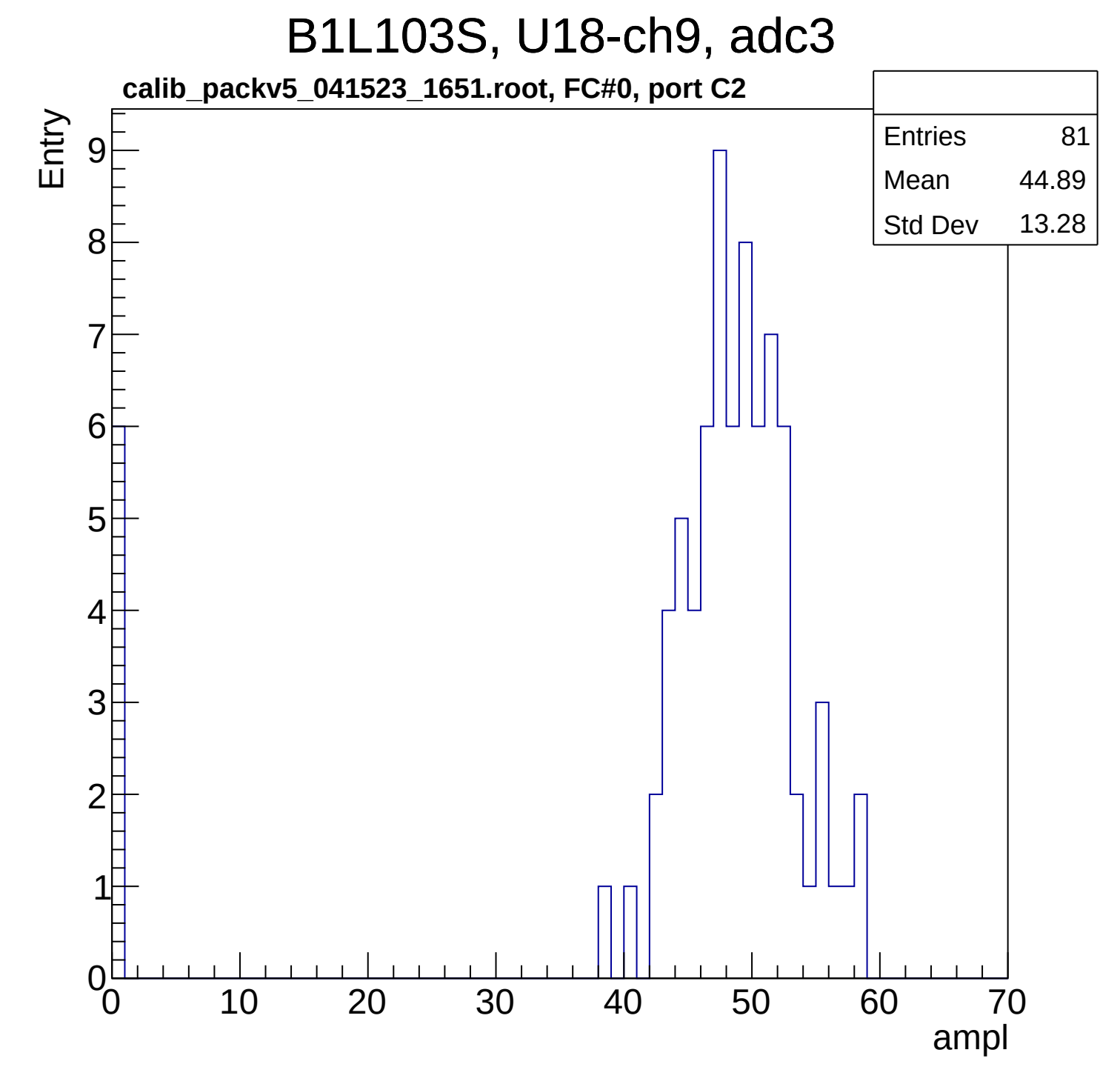
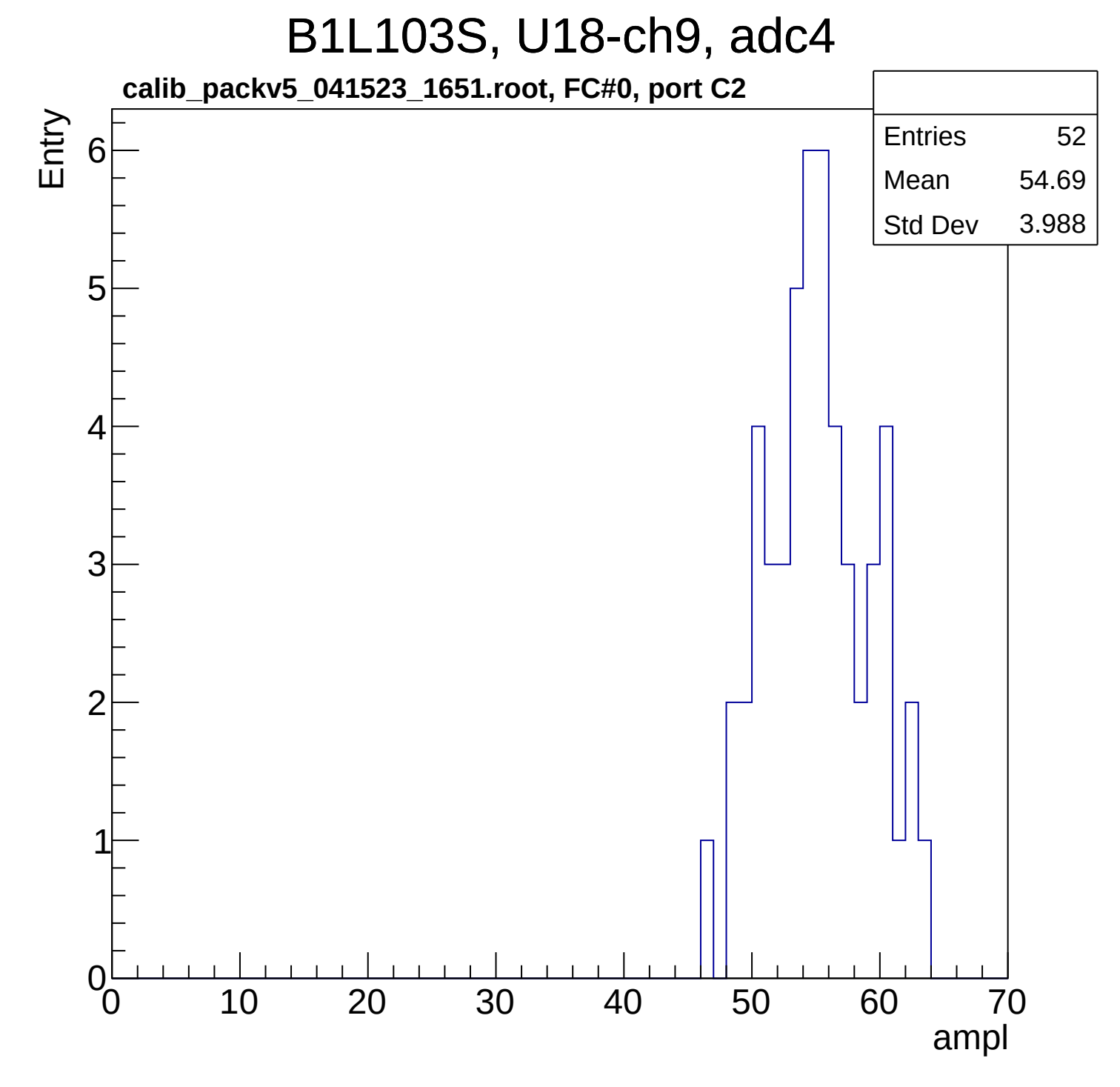
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

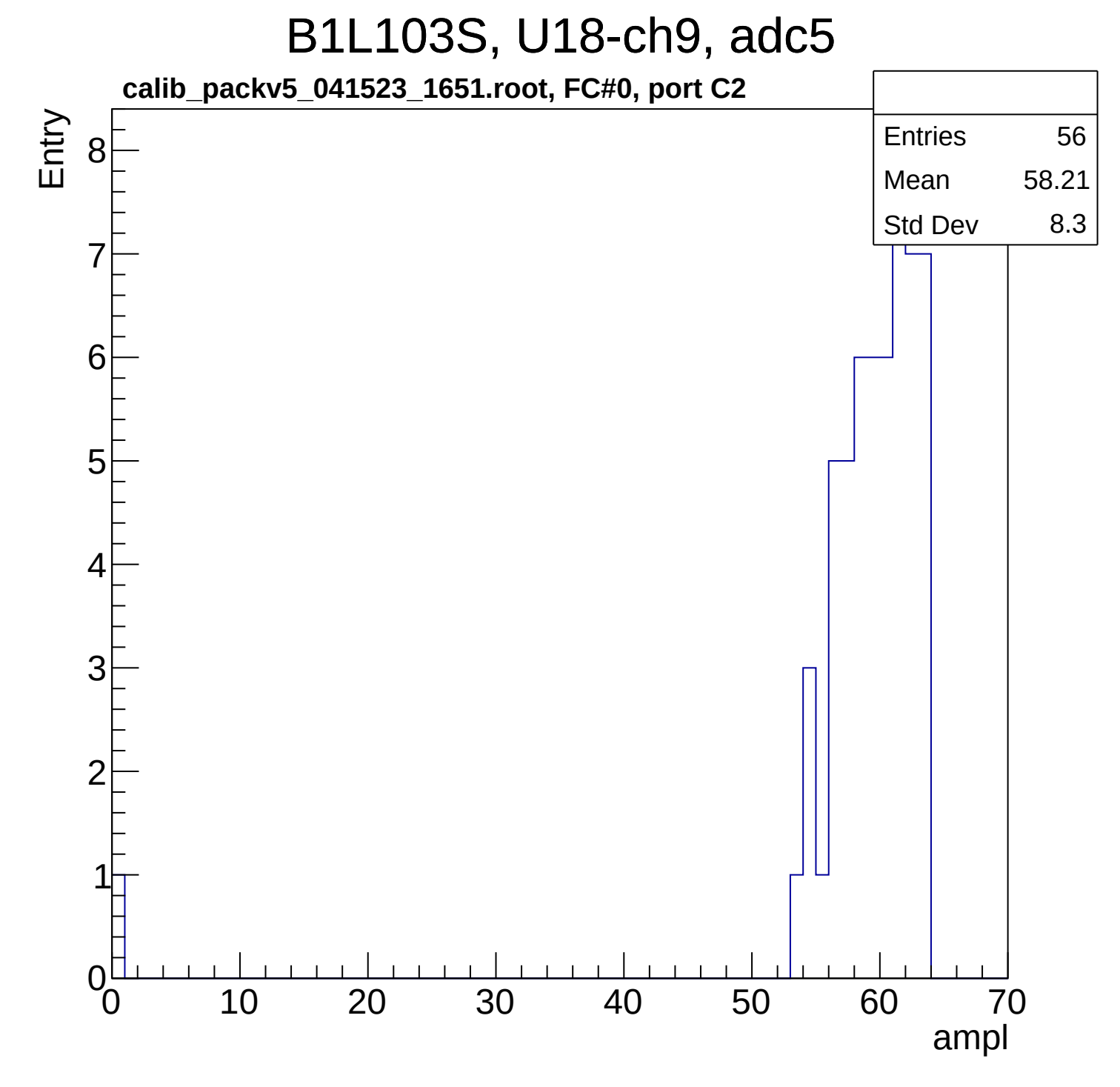

B1L103S, U18-ch9, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 24.38
Std Dev 11.76
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch9, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 34.62
Std Dev 5.519
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch9, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 36.68
Std Dev 14.29
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U18-ch9, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 44.89
Std Dev 13.28
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U18-ch9, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 54.69
Std Dev 3.988
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U18-ch9, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 58.21
Std Dev 8.3
Entry
ampl
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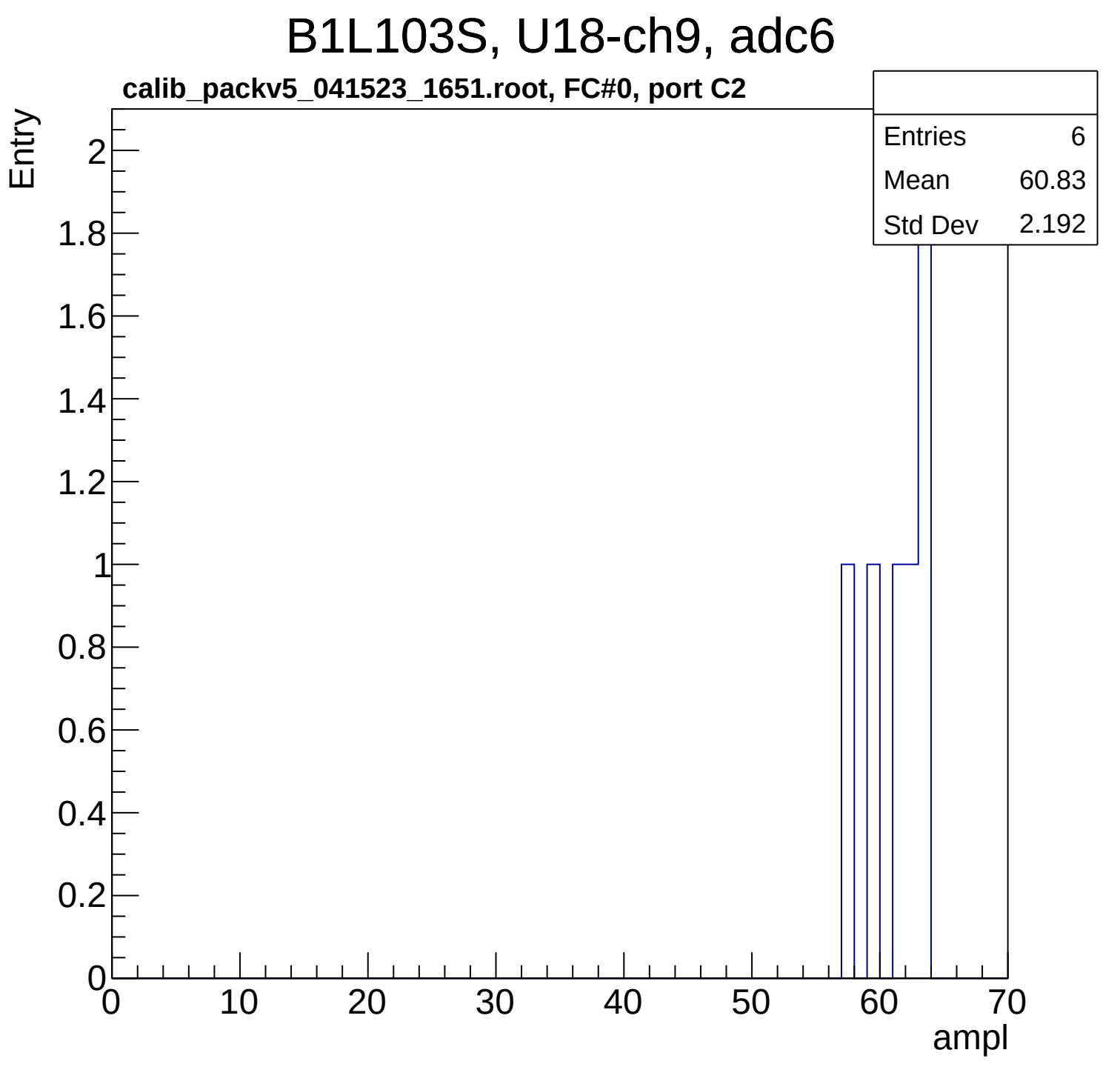
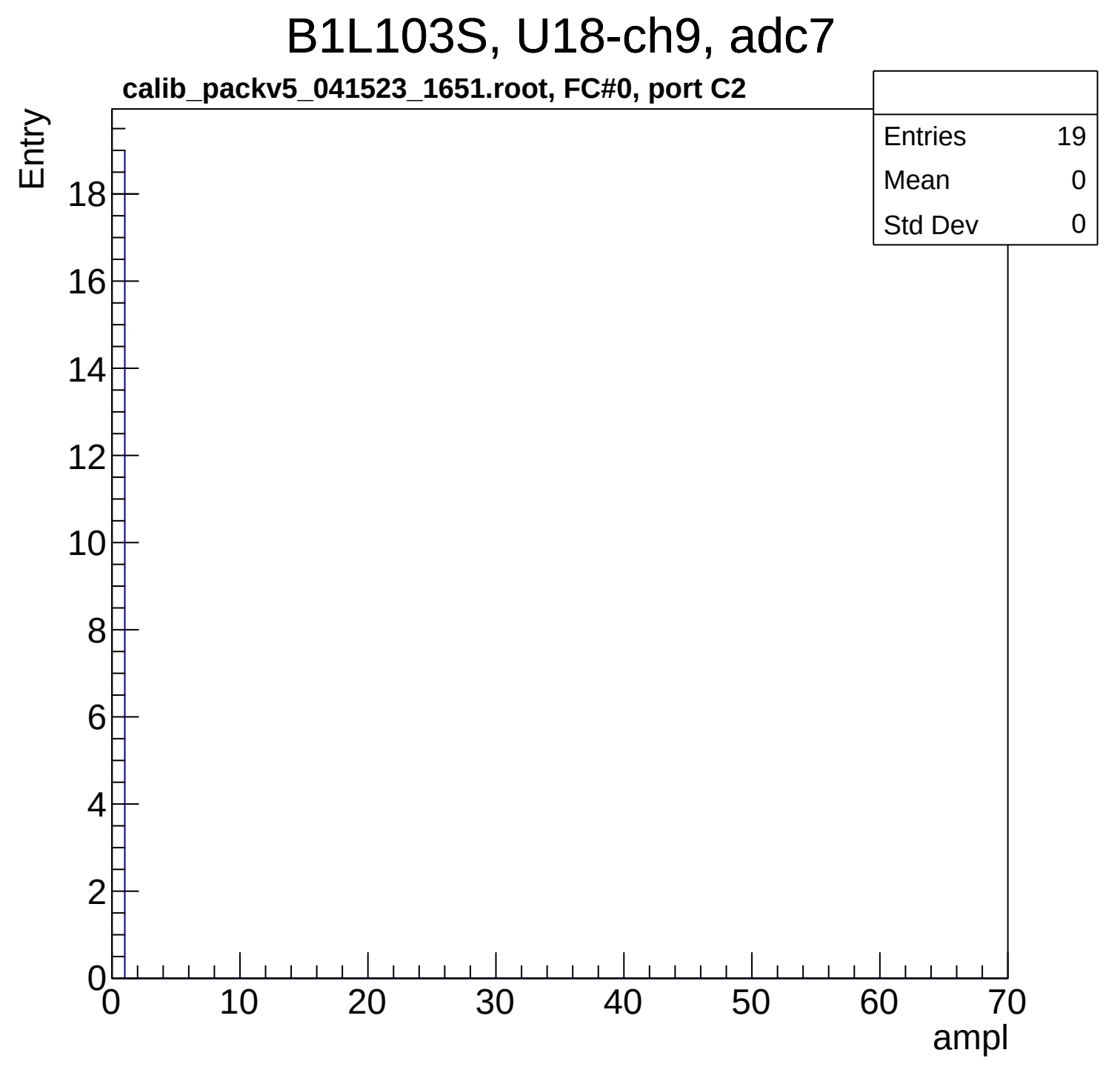
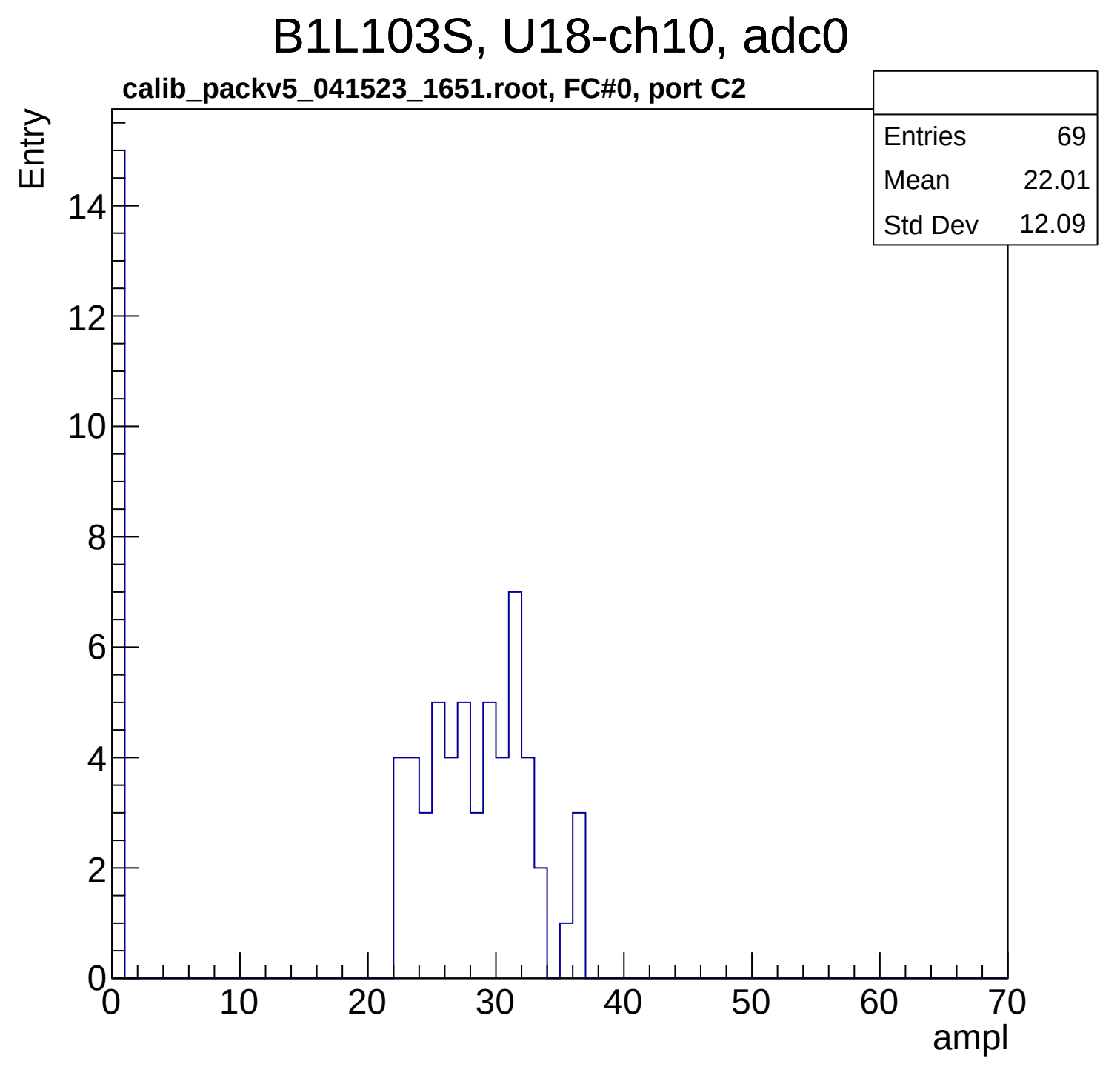
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch9, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 60.83
Std Dev 2.192
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U18-ch9, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch10, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 22.01
Std Dev 12.09
Entry
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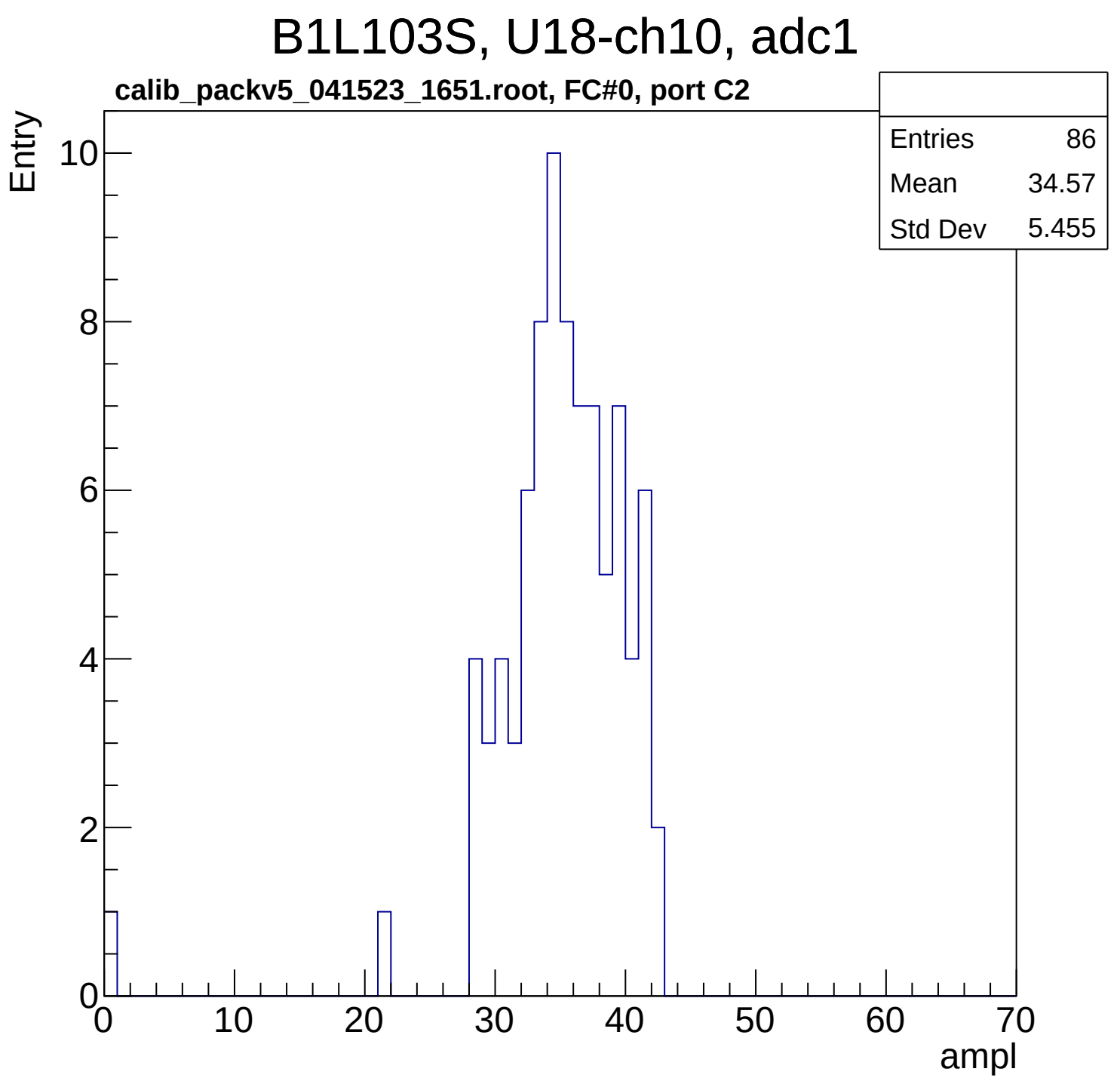
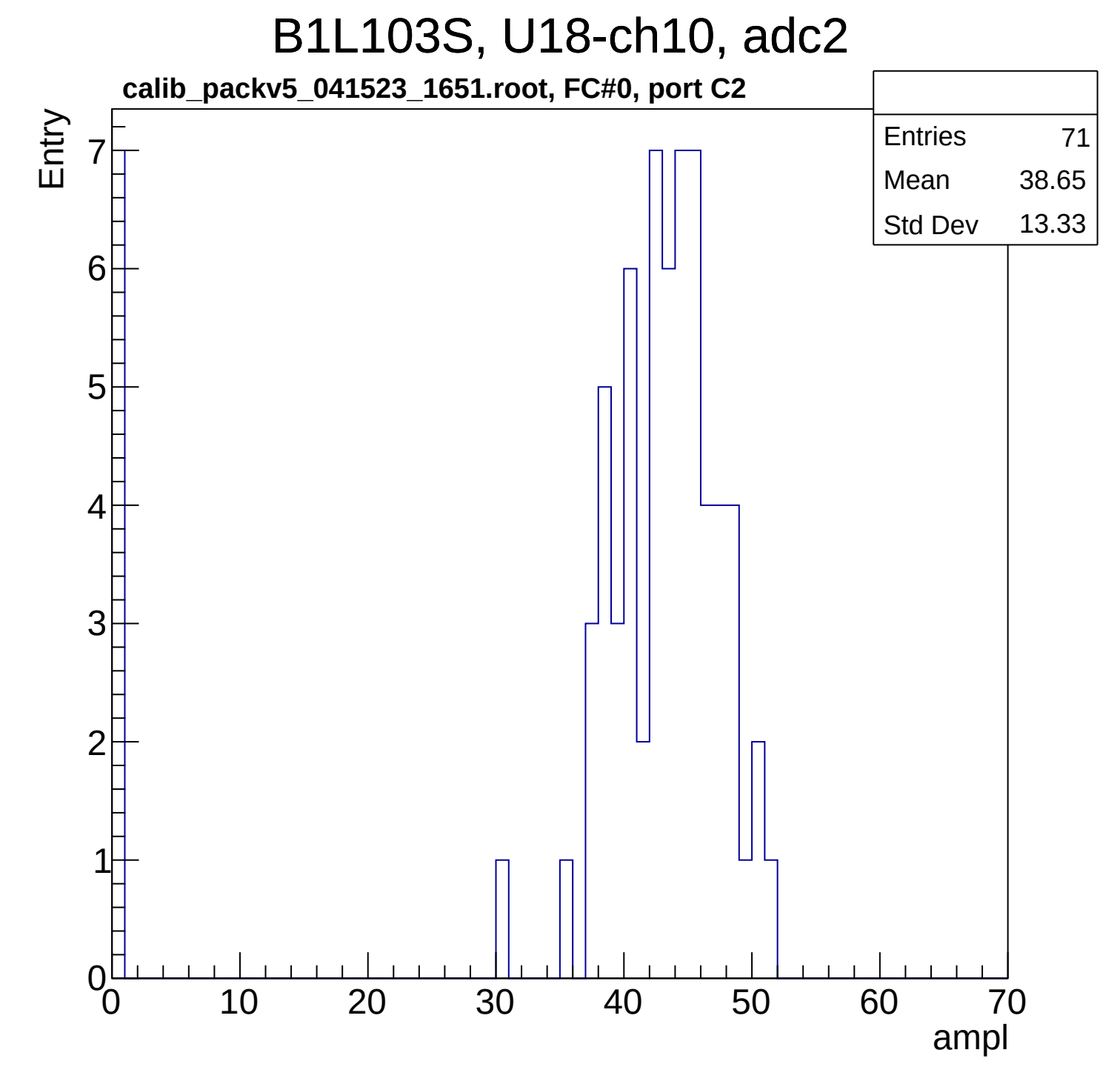
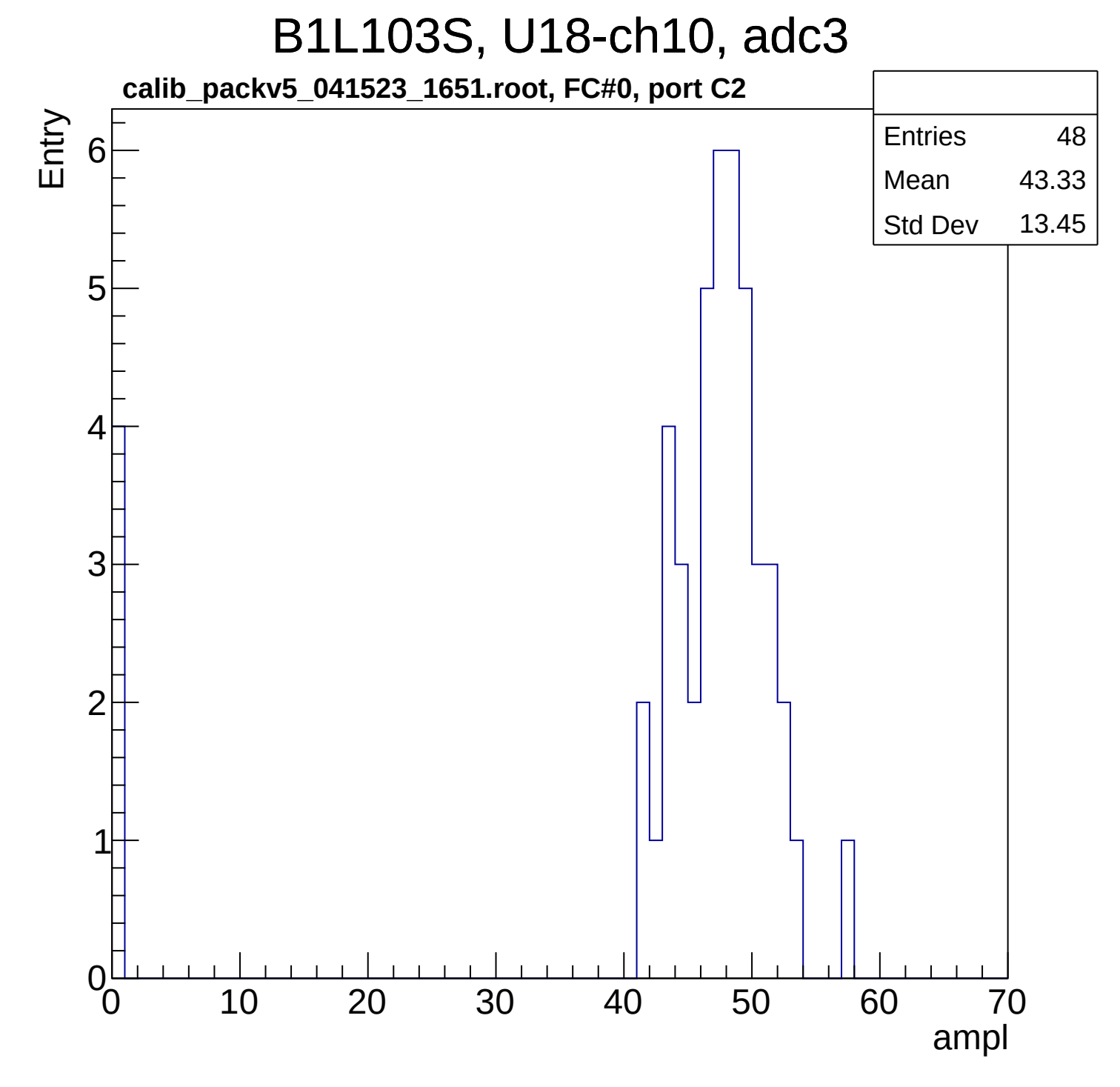
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch10, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 34.57
Std Dev 5.455
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U18-ch10, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 38.65
Std Dev 13.33
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U18-ch10, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 43.33
Std Dev 13.45
Entry
ampl
0
1
2
3
4
5
6
0
10
20
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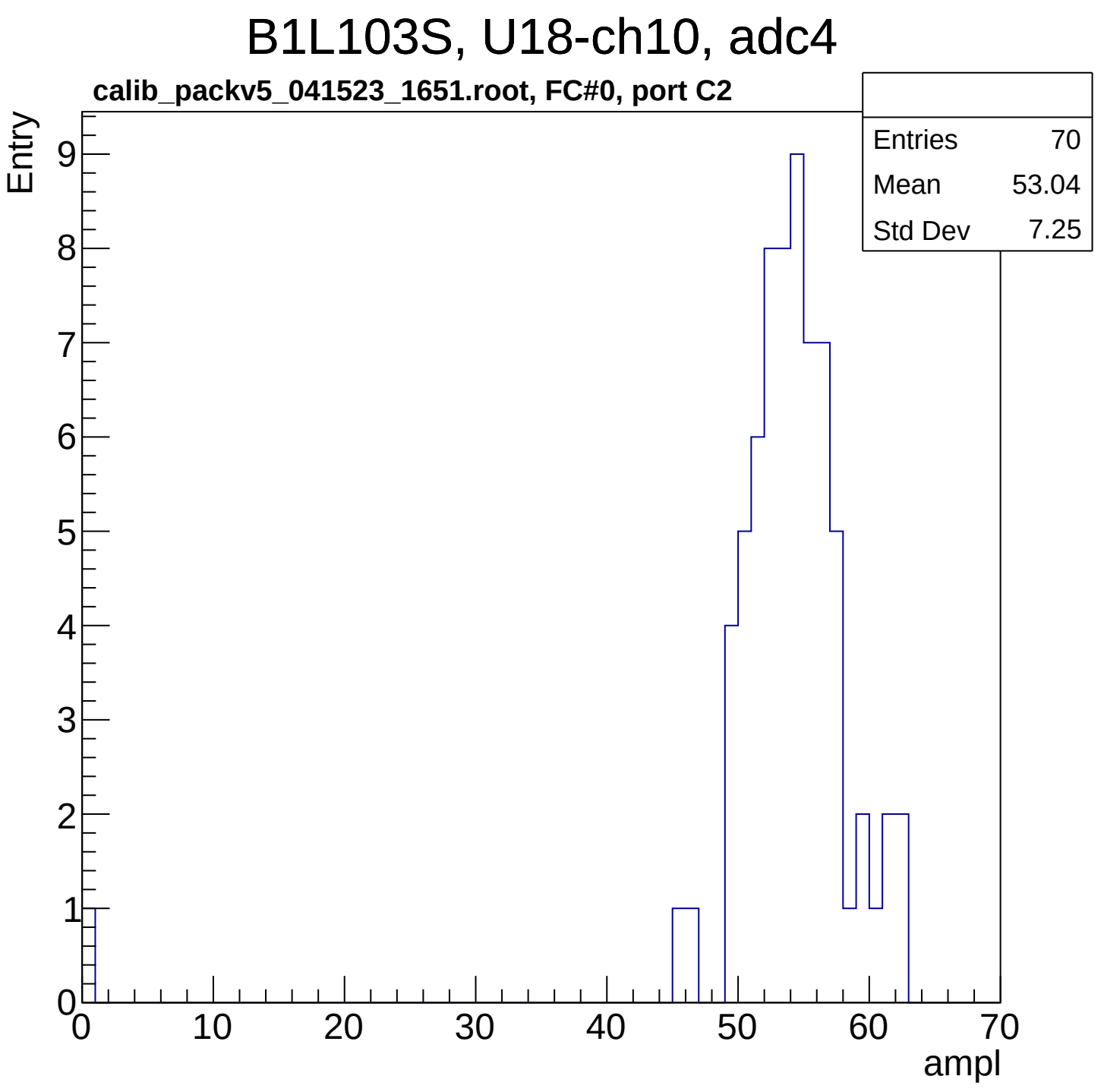
40
50
60
70


B1L103S, U18-ch10, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 53.04
Std Dev 7.25
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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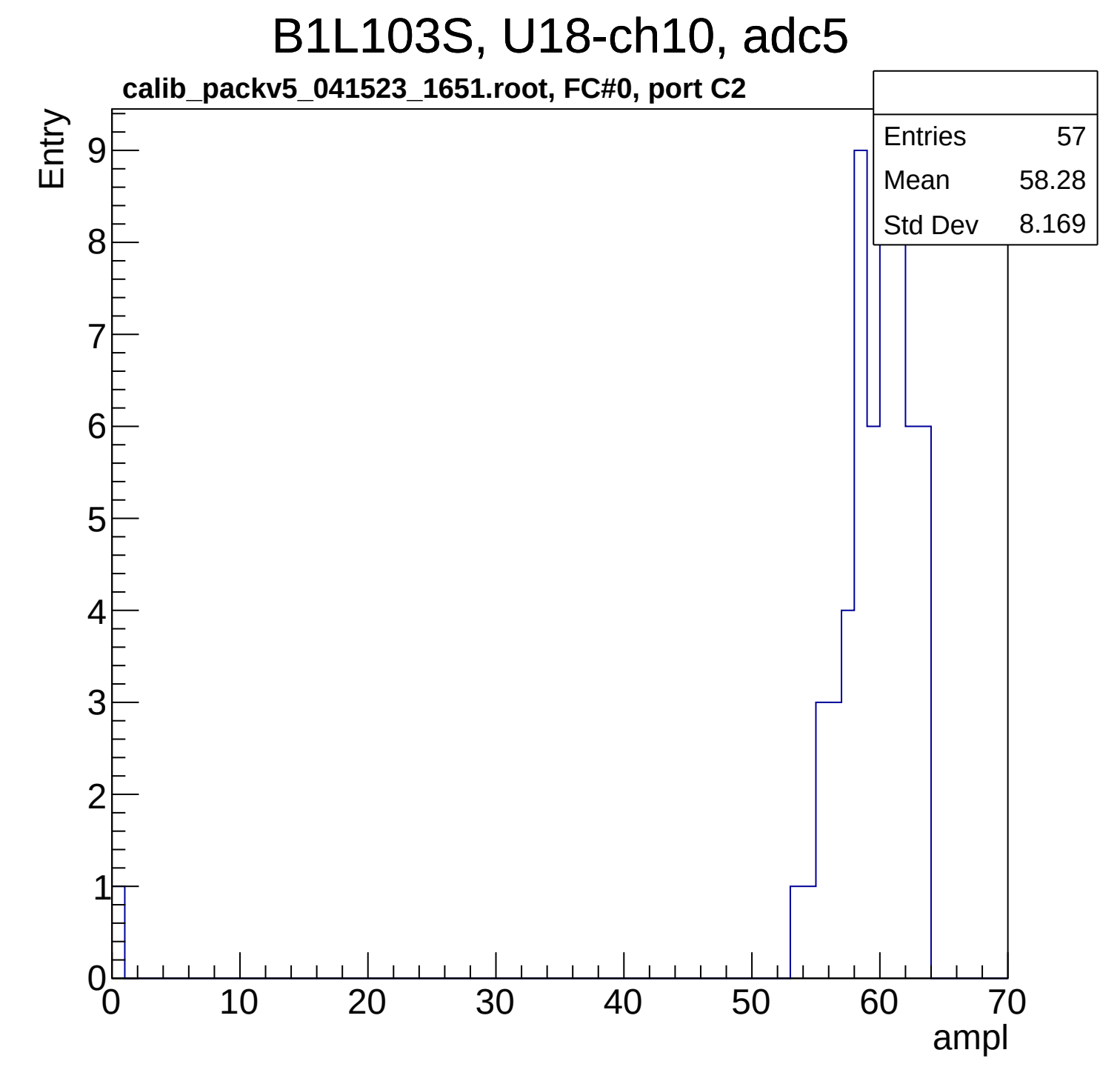
B1L103S, U18-ch10, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 58.28
Std Dev 8.169
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
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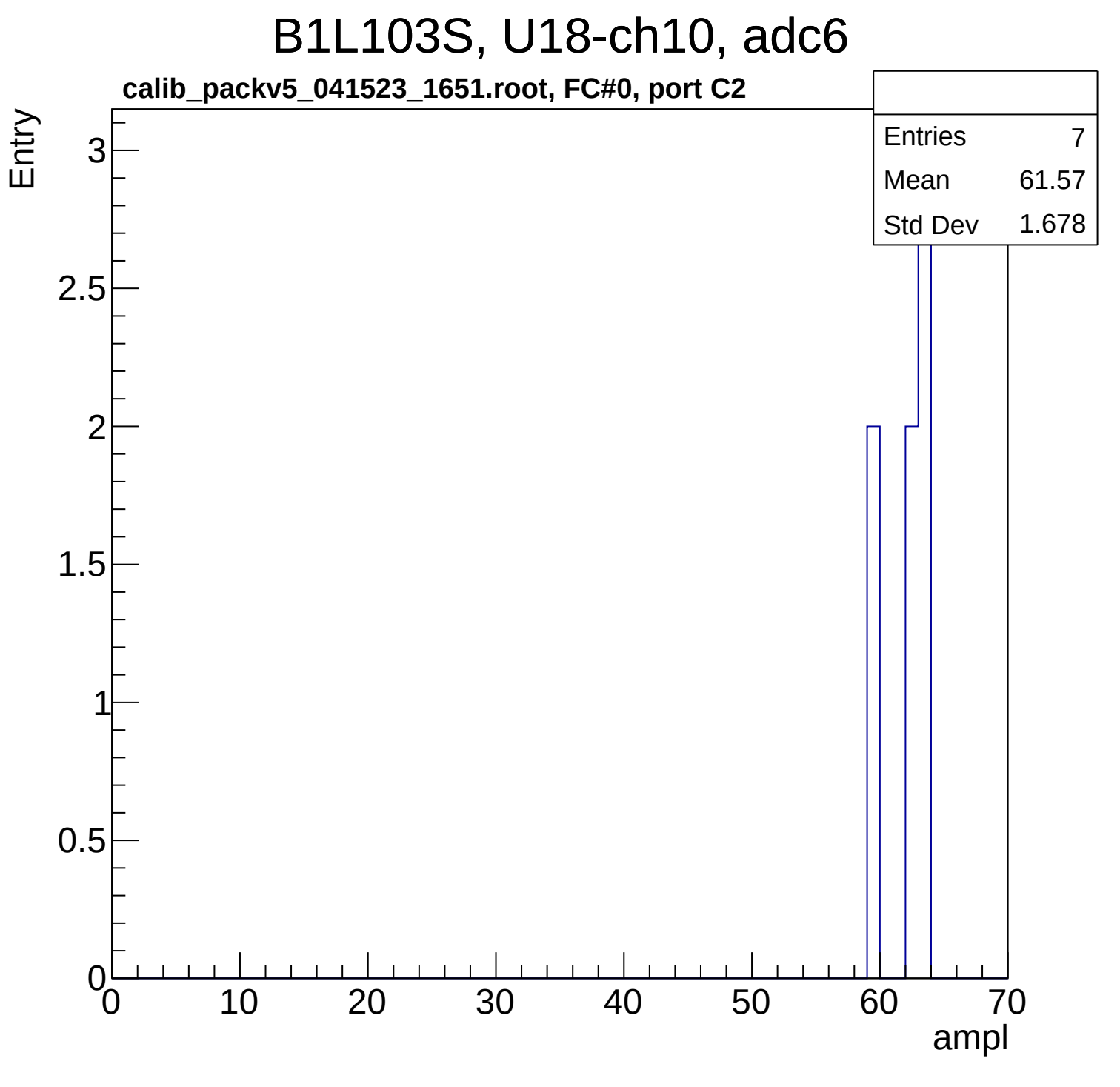
40
50
60
70


B1L103S, U18-ch10, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 61.57
Std Dev 1.678
Entry
ampl
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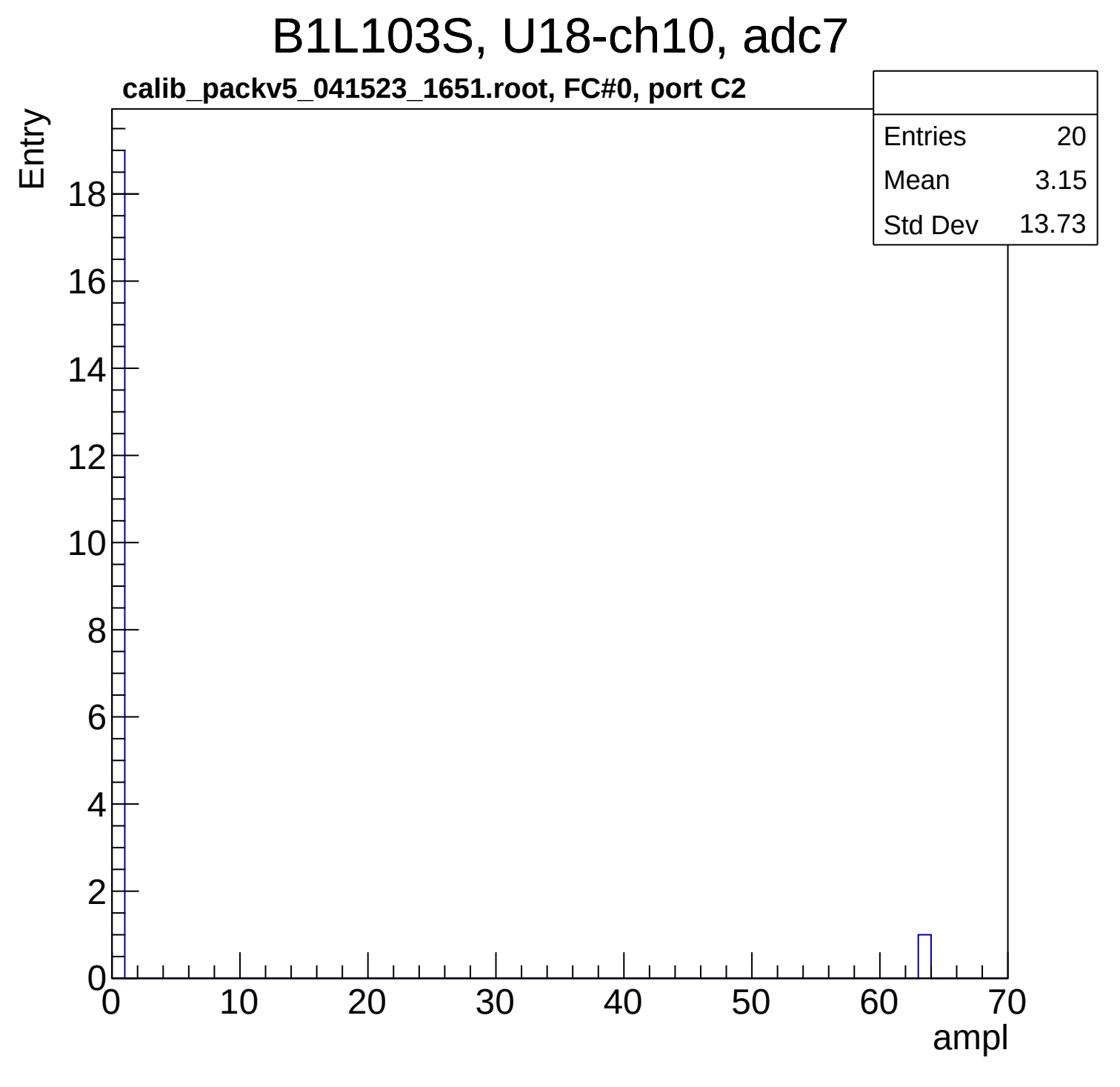
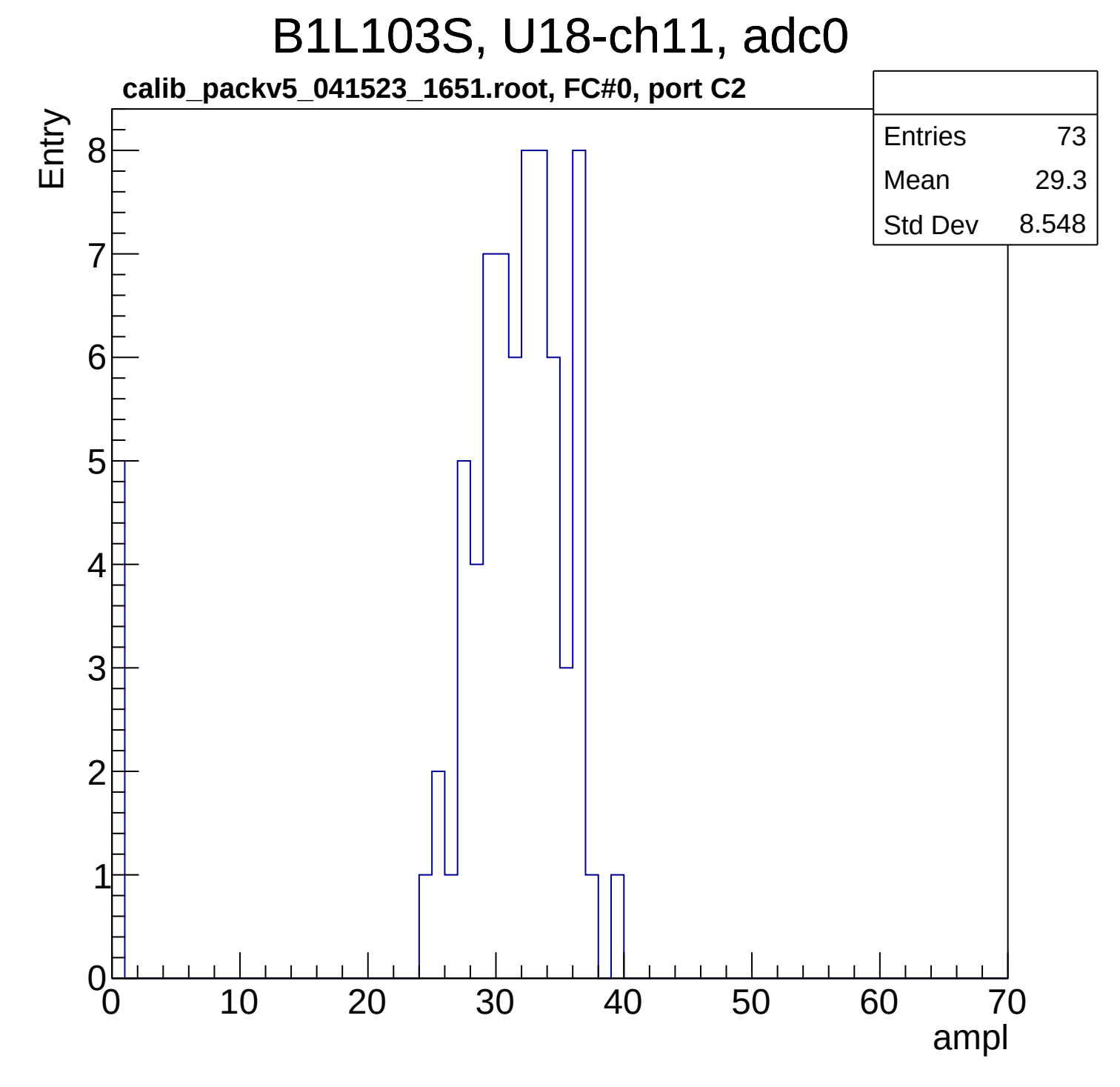
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U18-ch10, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch11, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 29.3
Std Dev 8.548
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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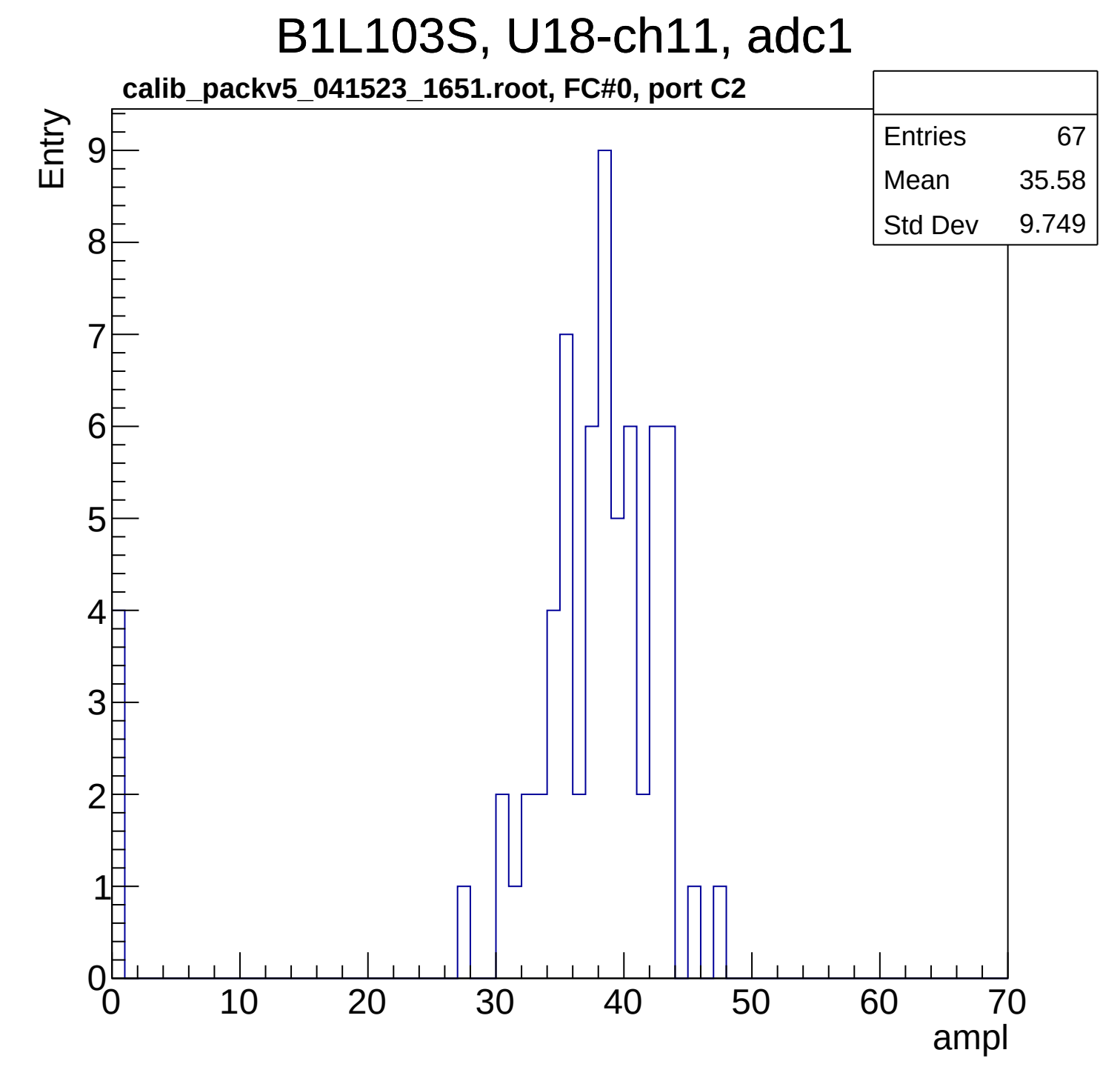
40
50
60
70


B1L103S, U18-ch11, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 35.58
Std Dev 9.749
Entry
ampl
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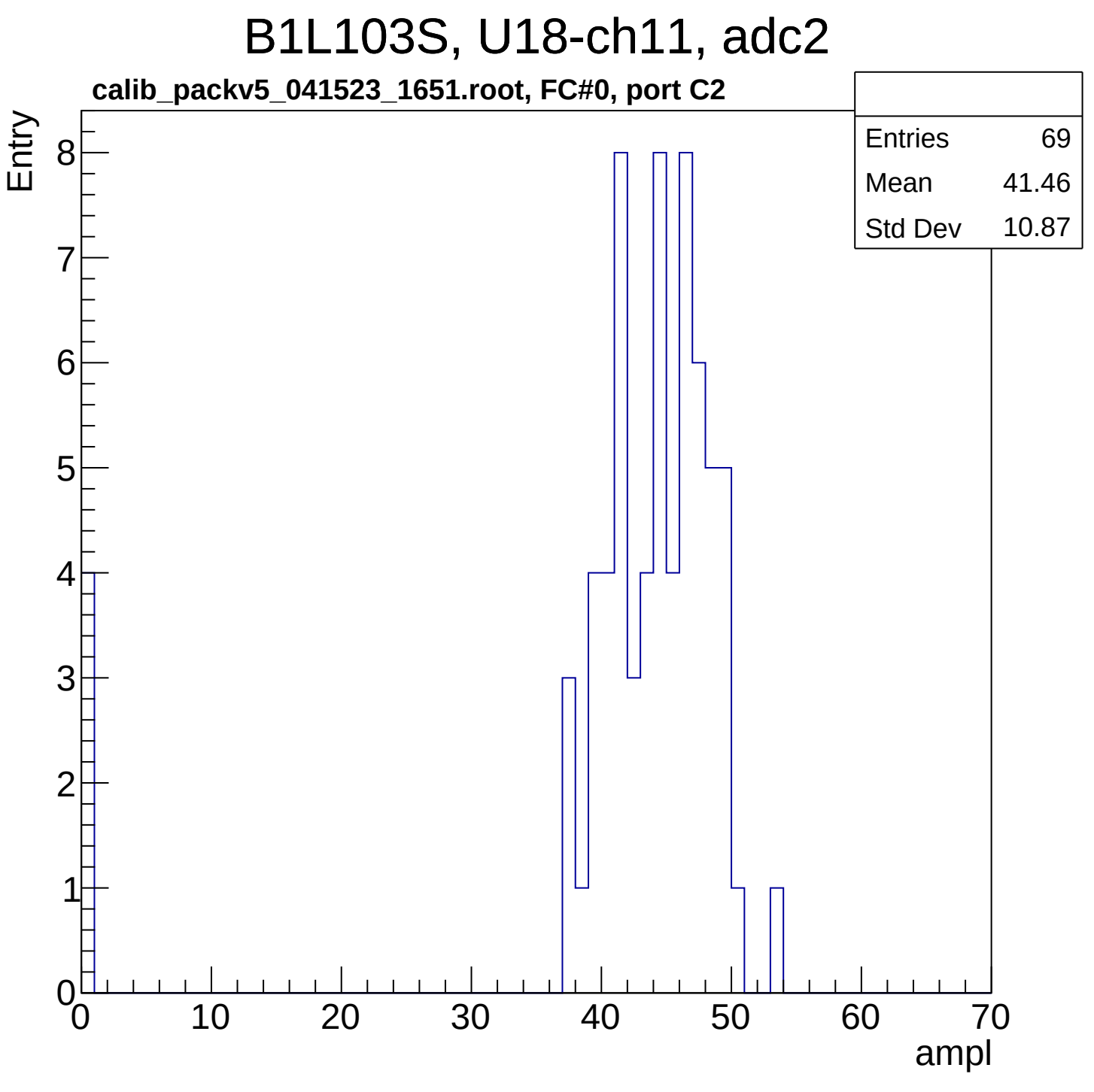
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U18-ch11, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 41.46
Std Dev 10.87
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
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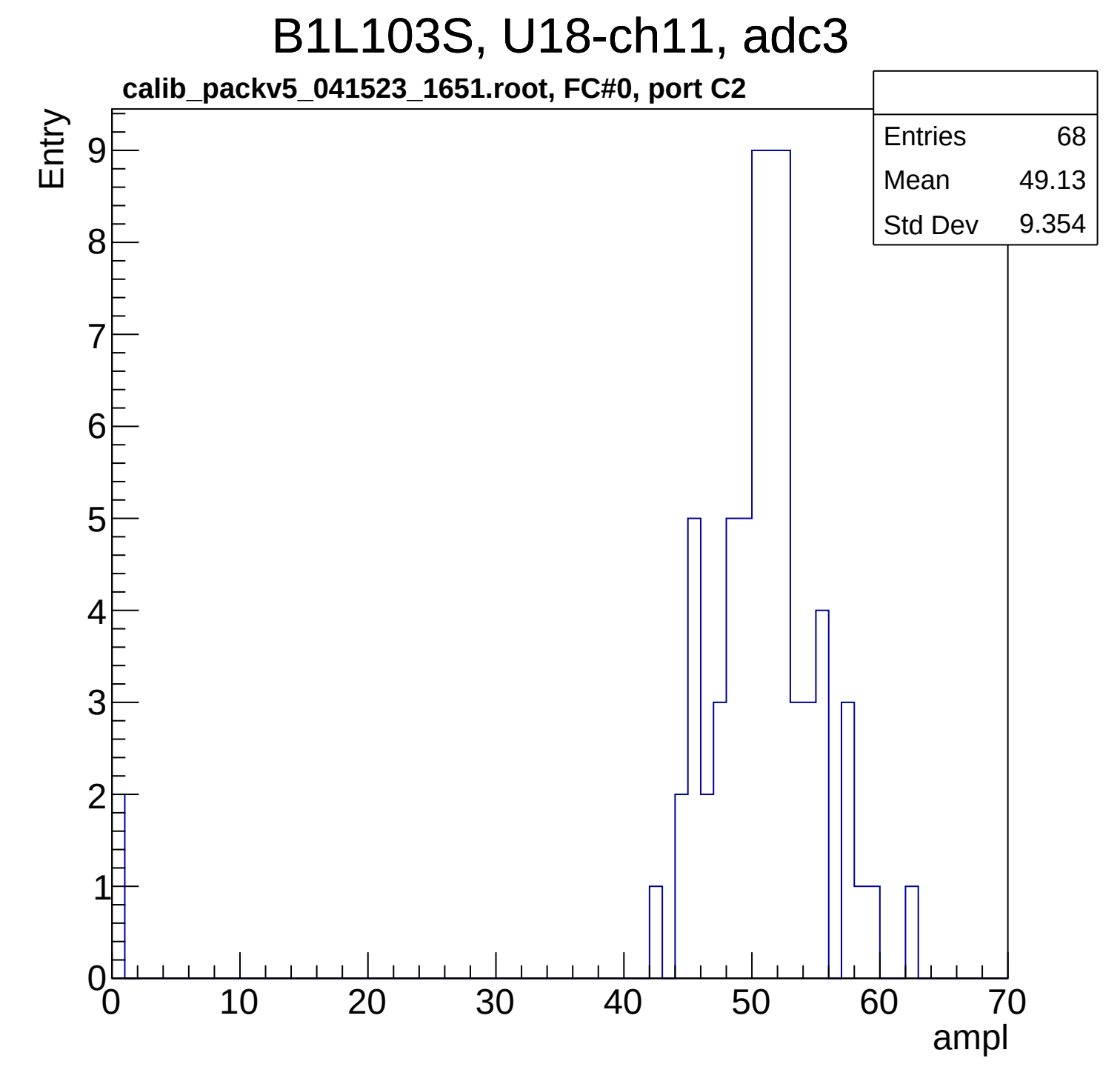
50
60
70


B1L103S, U18-ch11, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 49.13
Std Dev 9.354
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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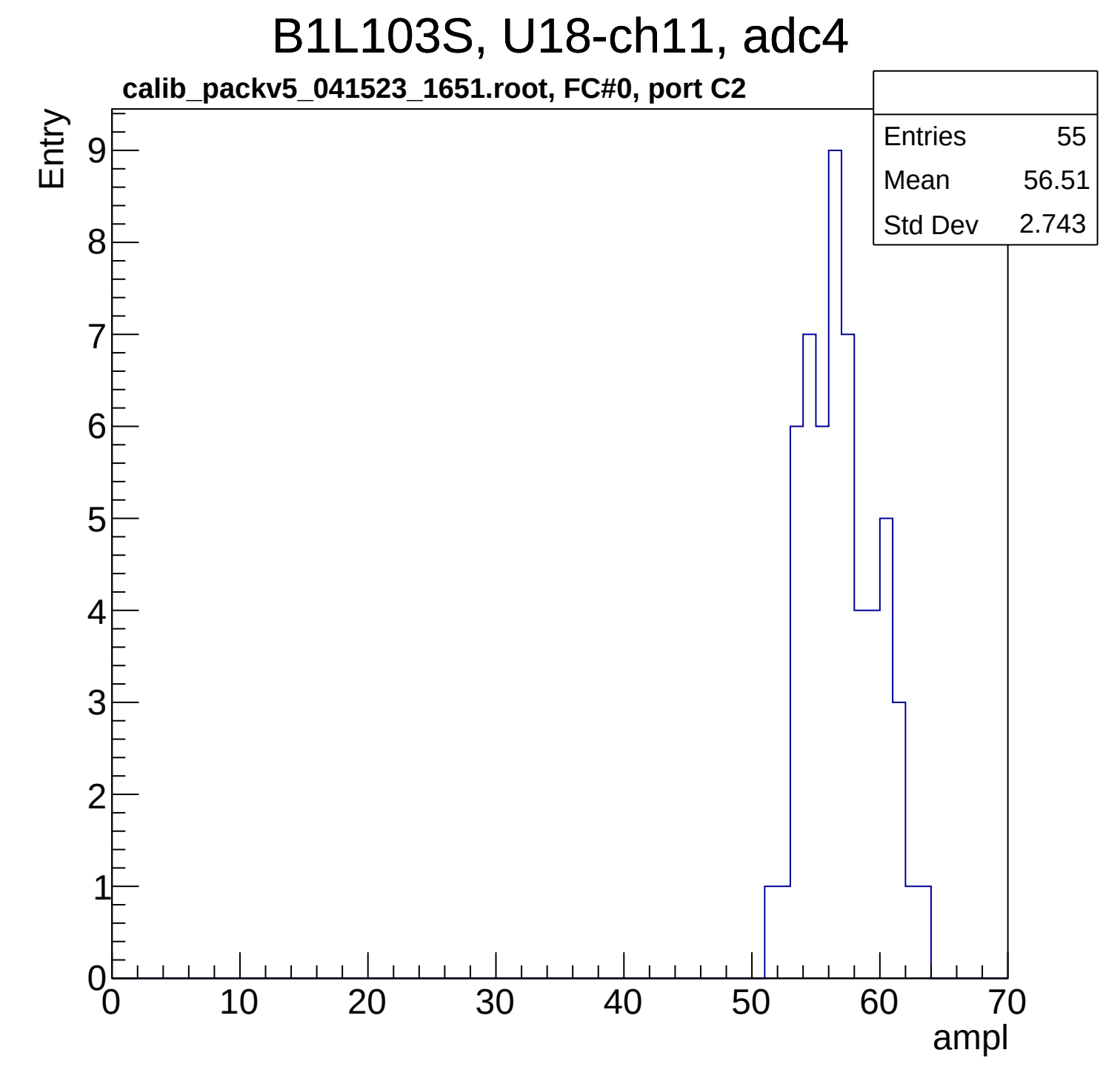
40
50
60
70


B1L103S, U18-ch11, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 56.51
Std Dev 2.743
Entry
ampl
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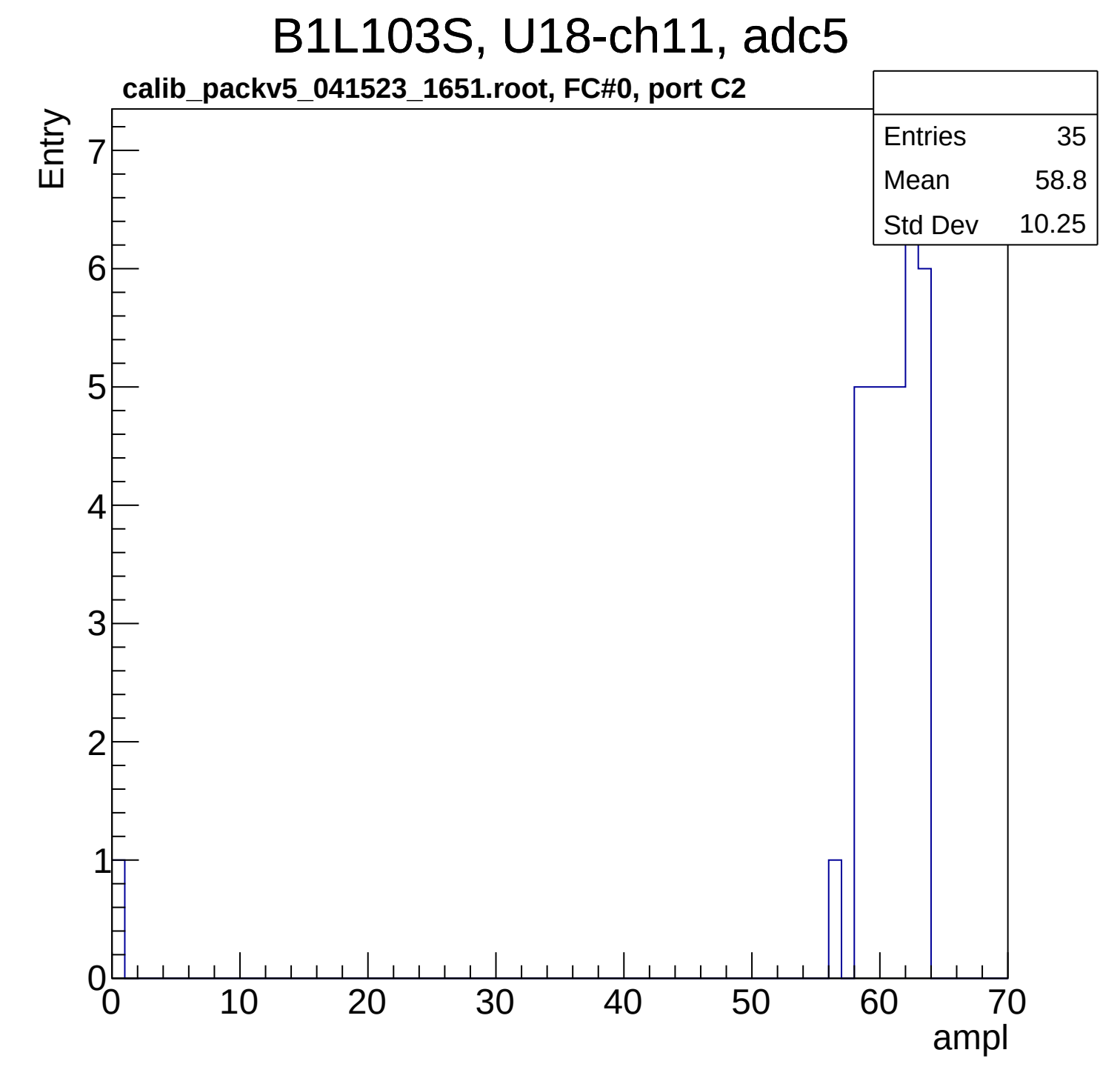
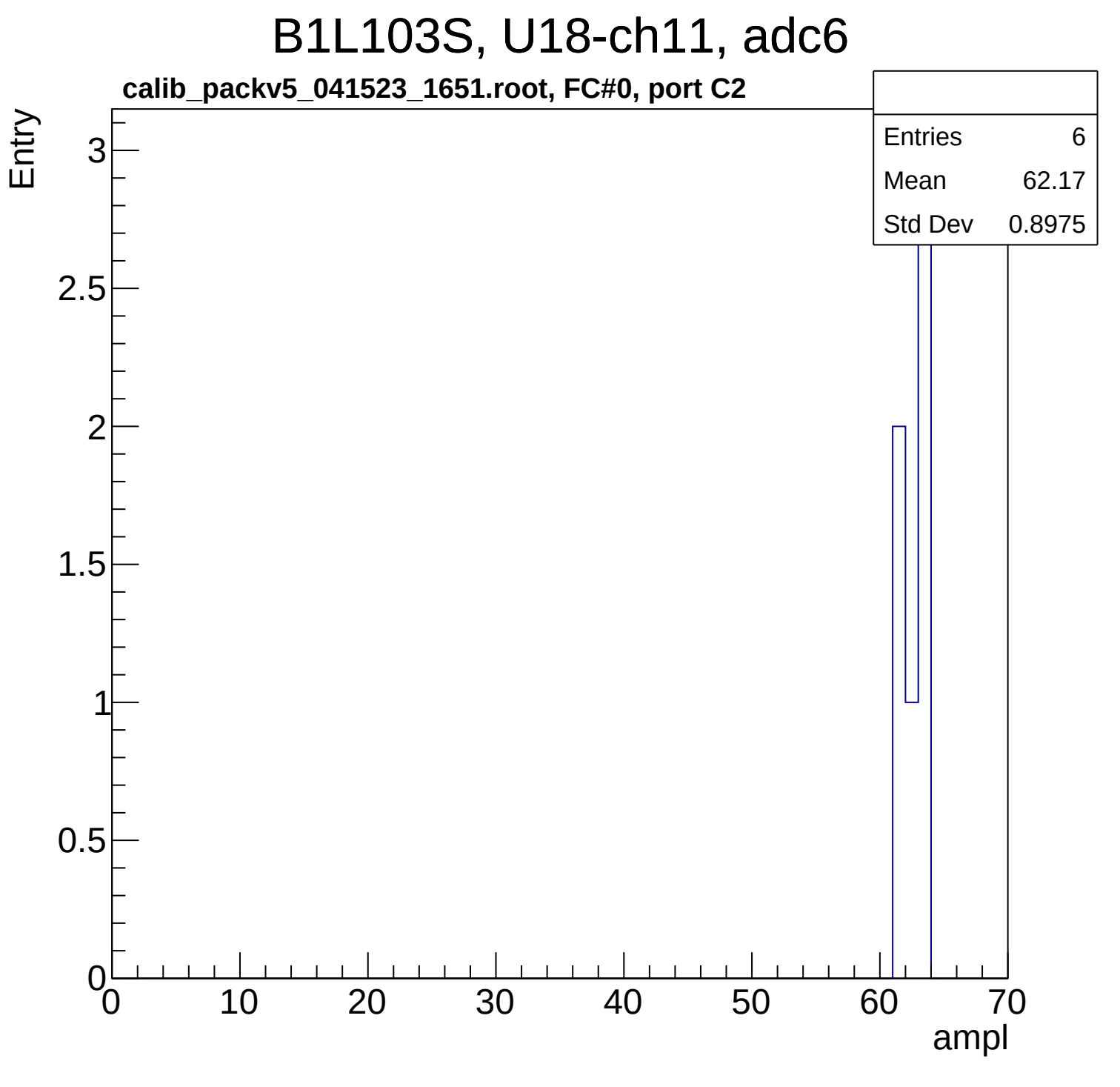
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U18-ch11, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 35
Mean 58.8
Std Dev 10.25
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U18-ch11, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 62.17
Std Dev 0.8975
Entry
ampl
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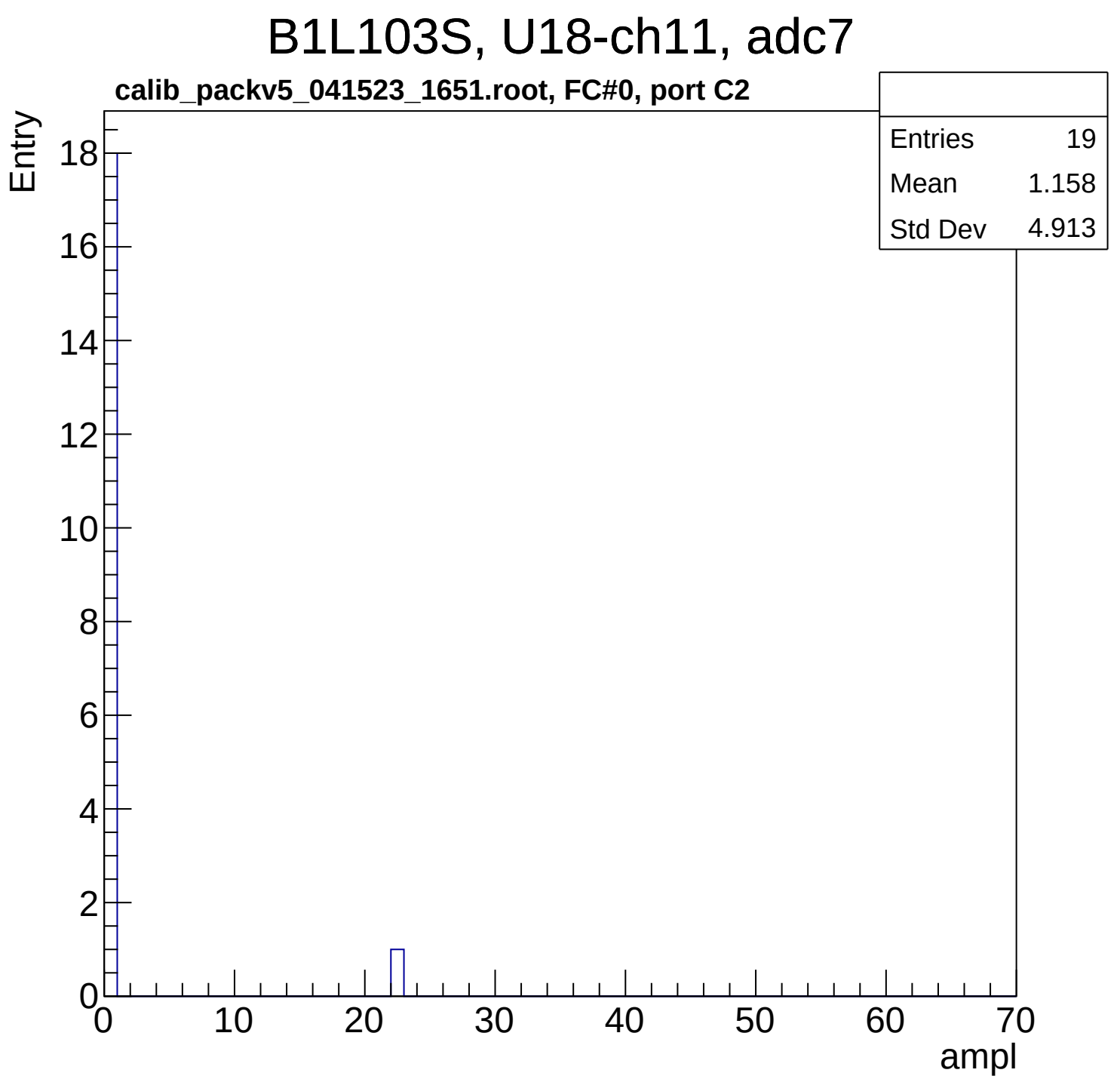
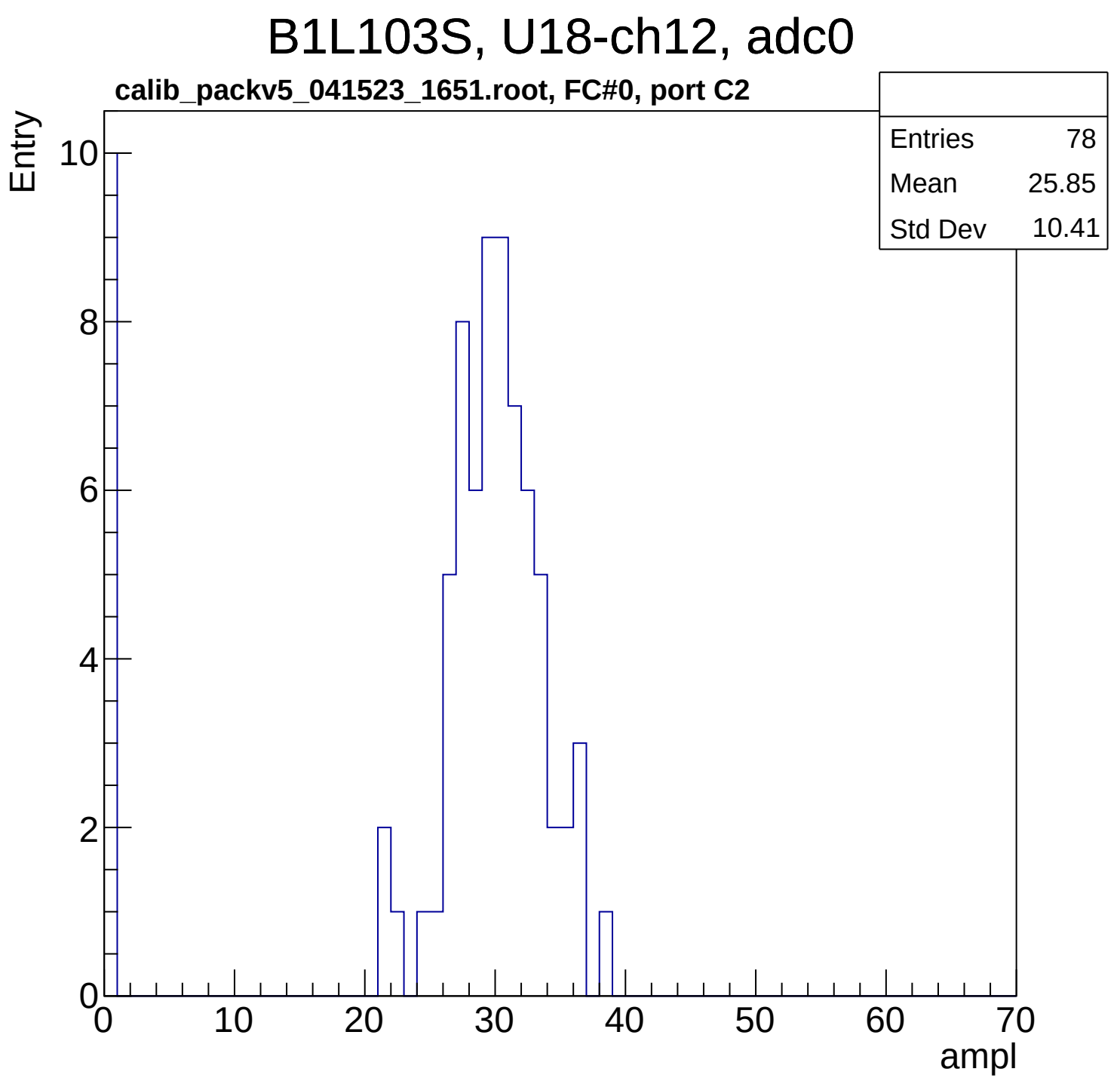
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U18-ch11, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.158
Std Dev 4.913
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch12, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 25.85
Std Dev 10.41
Entry
ampl
0
2
4
6
8
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0
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40
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60
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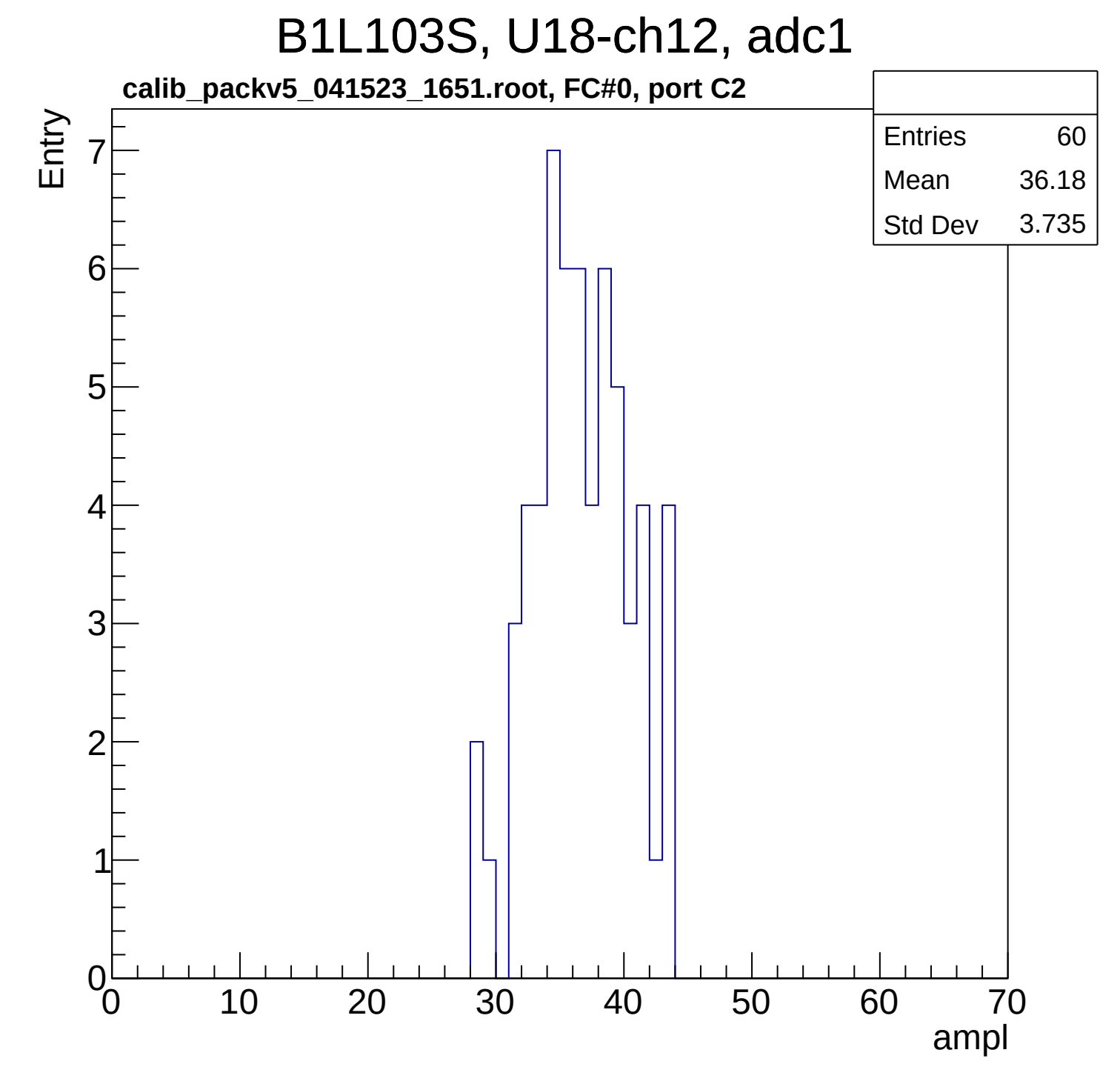
B1L103S, U18-ch12, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 36.18
Std Dev 3.735
Entry
ampl
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2
3
4
5
6
7
0
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20
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40
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60
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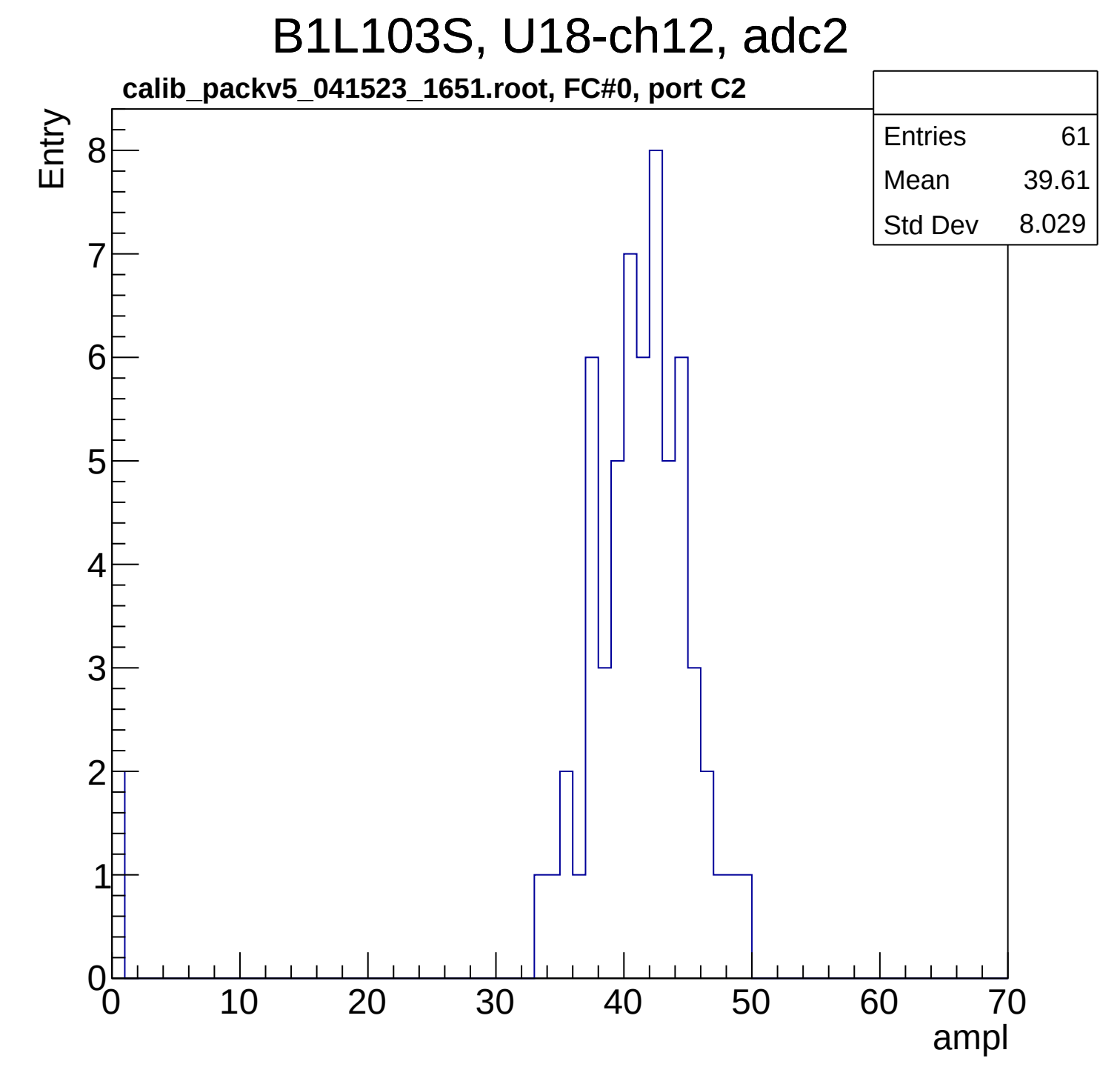
B1L103S, U18-ch12, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 39.61
Std Dev 8.029
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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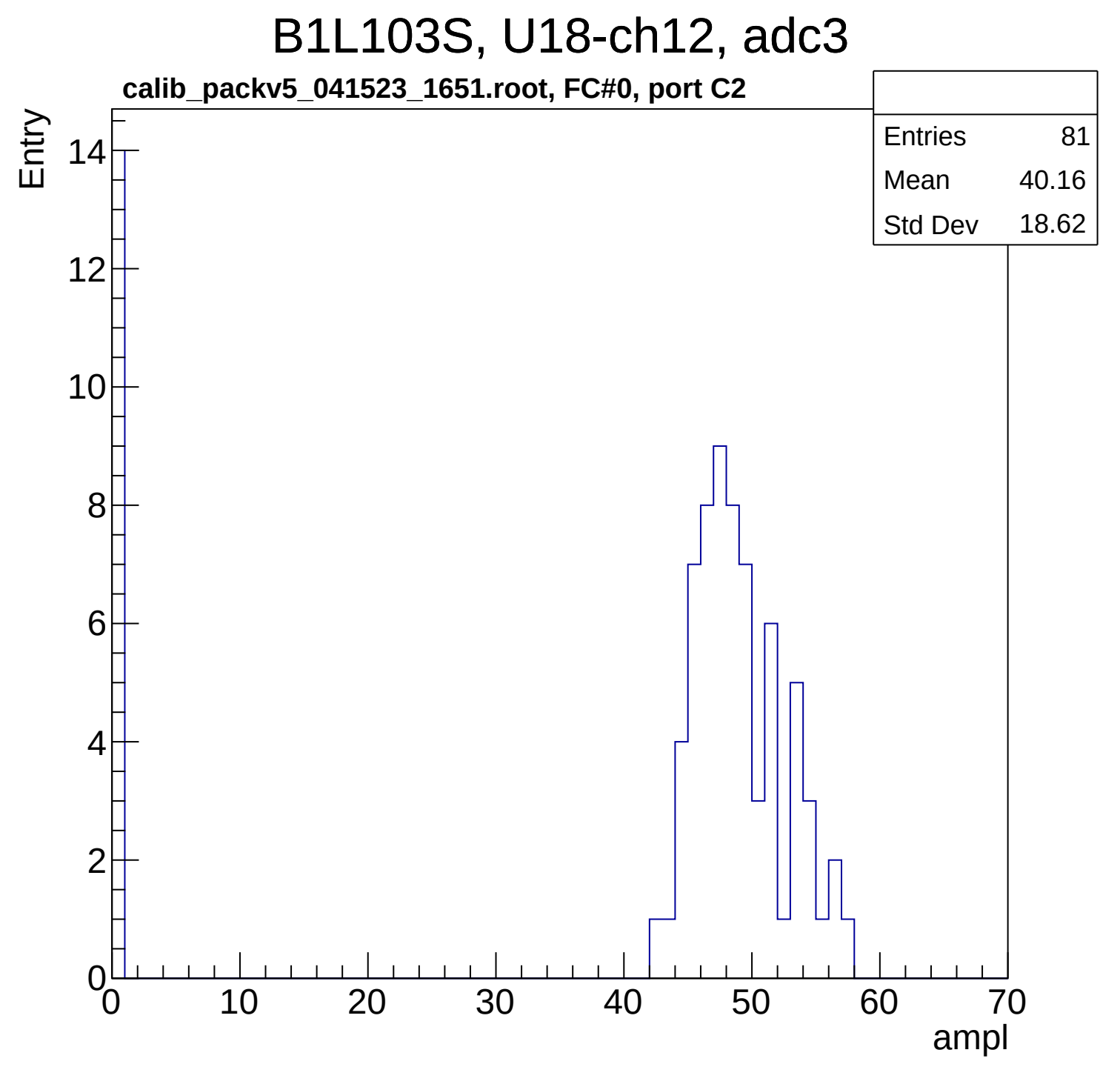
B1L103S, U18-ch12, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 40.16
Std Dev 18.62
Entry
ampl
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2
4
6
8
10
12
14
0
10
20
30
40
50
60
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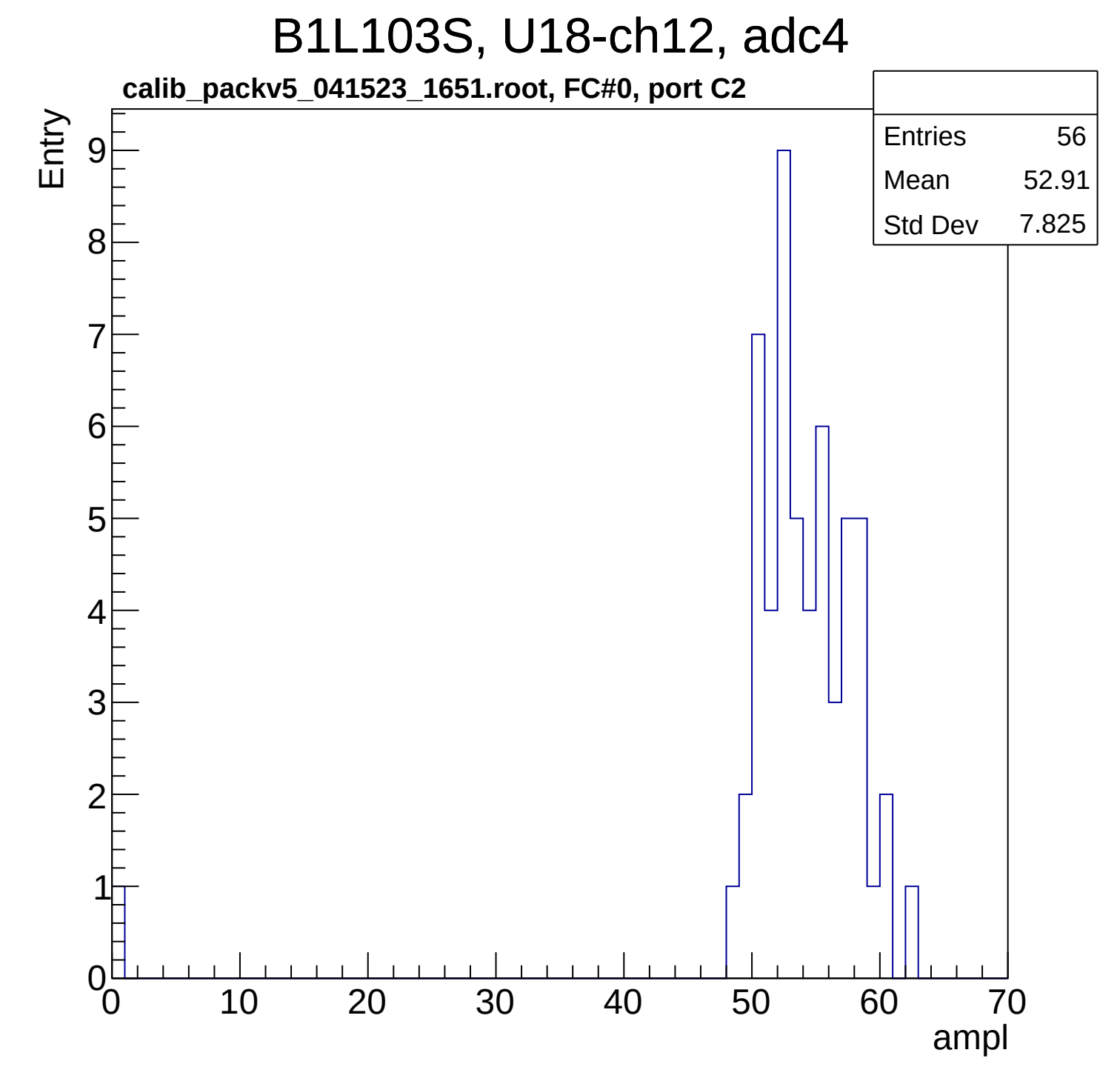
B1L103S, U18-ch12, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 52.91
Std Dev 7.825
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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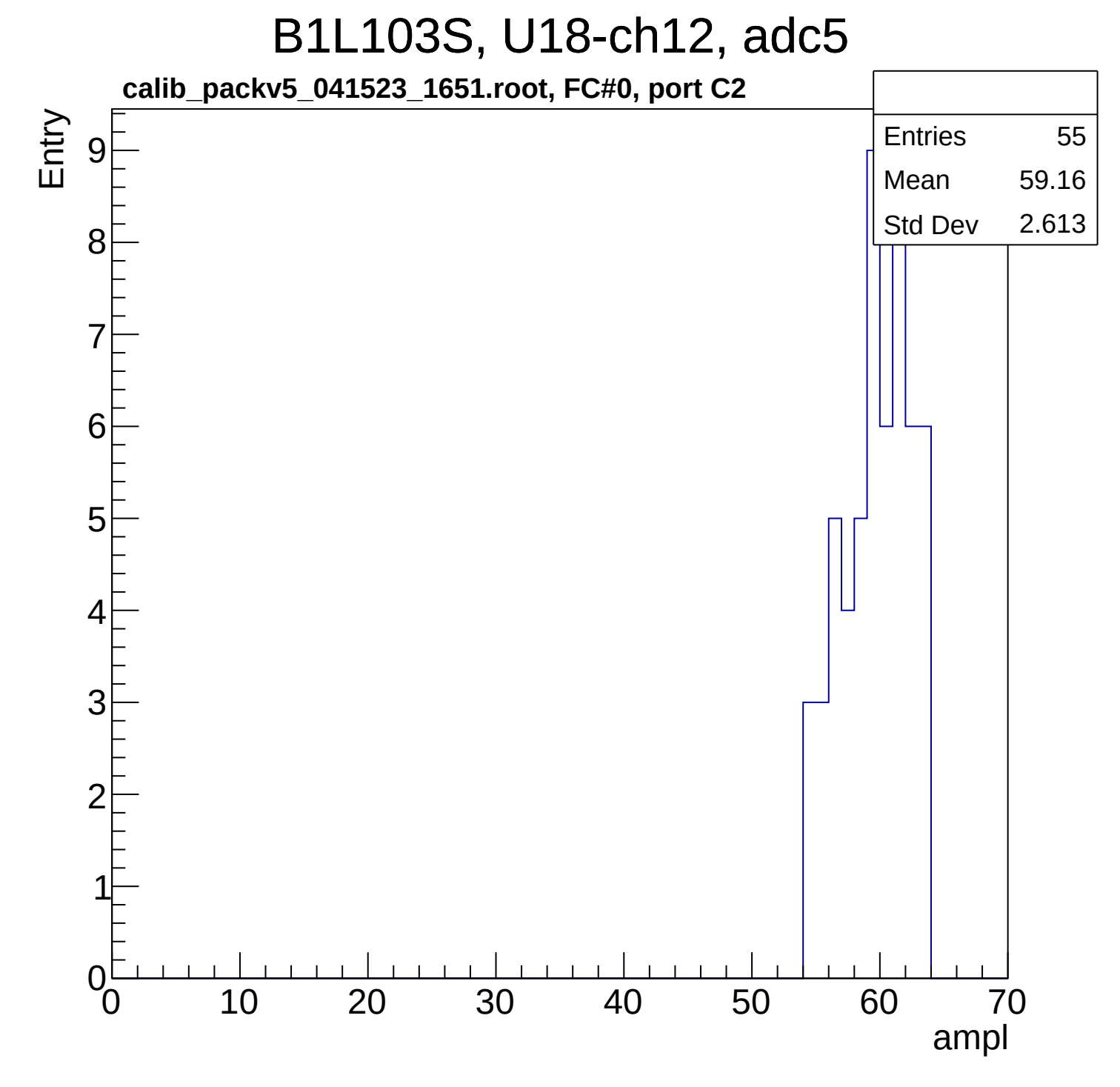
B1L103S, U18-ch12, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 59.16
Std Dev 2.613
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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60
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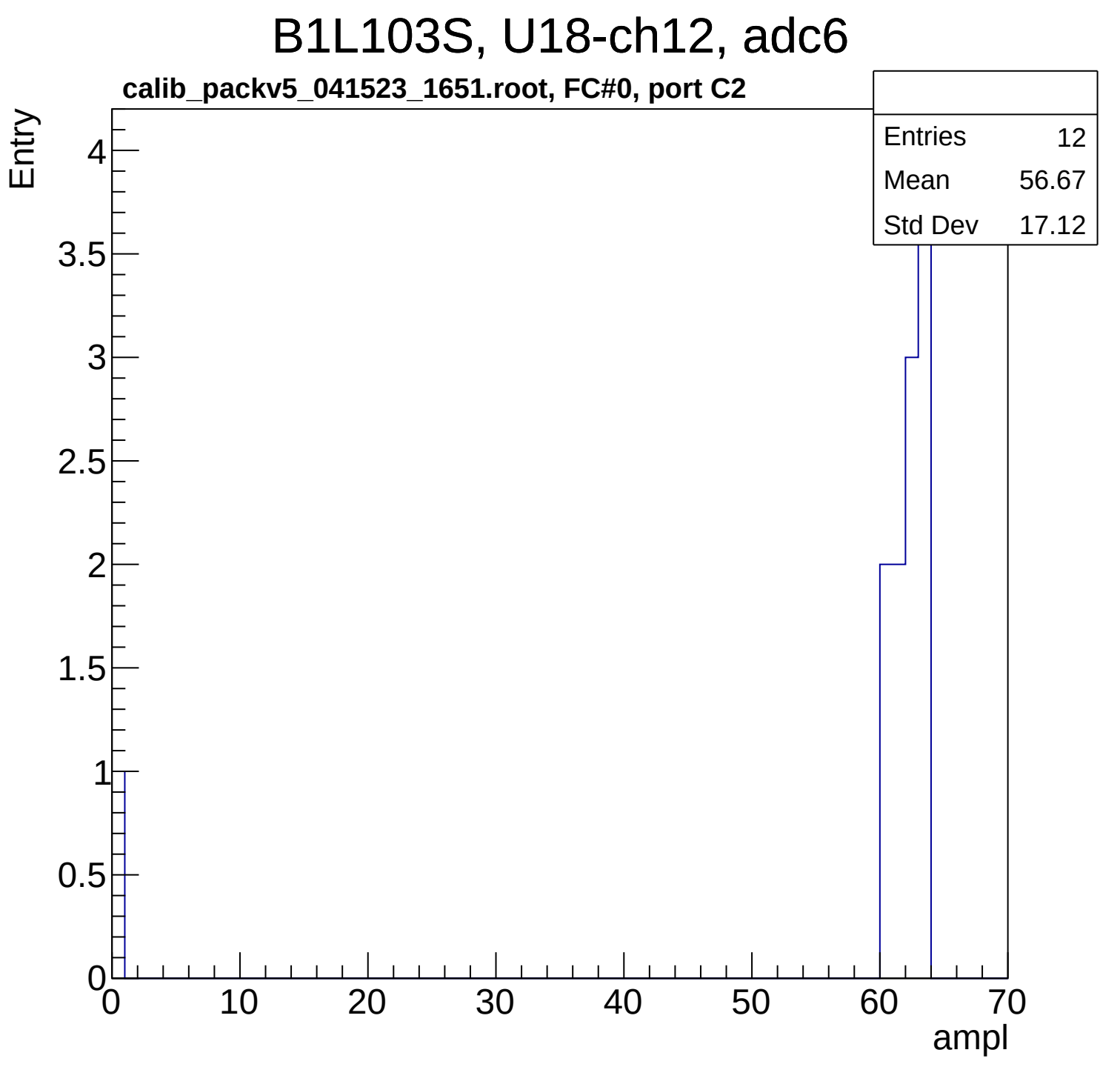
B1L103S, U18-ch12, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 56.67
Std Dev 17.12
Entry
ampl
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0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
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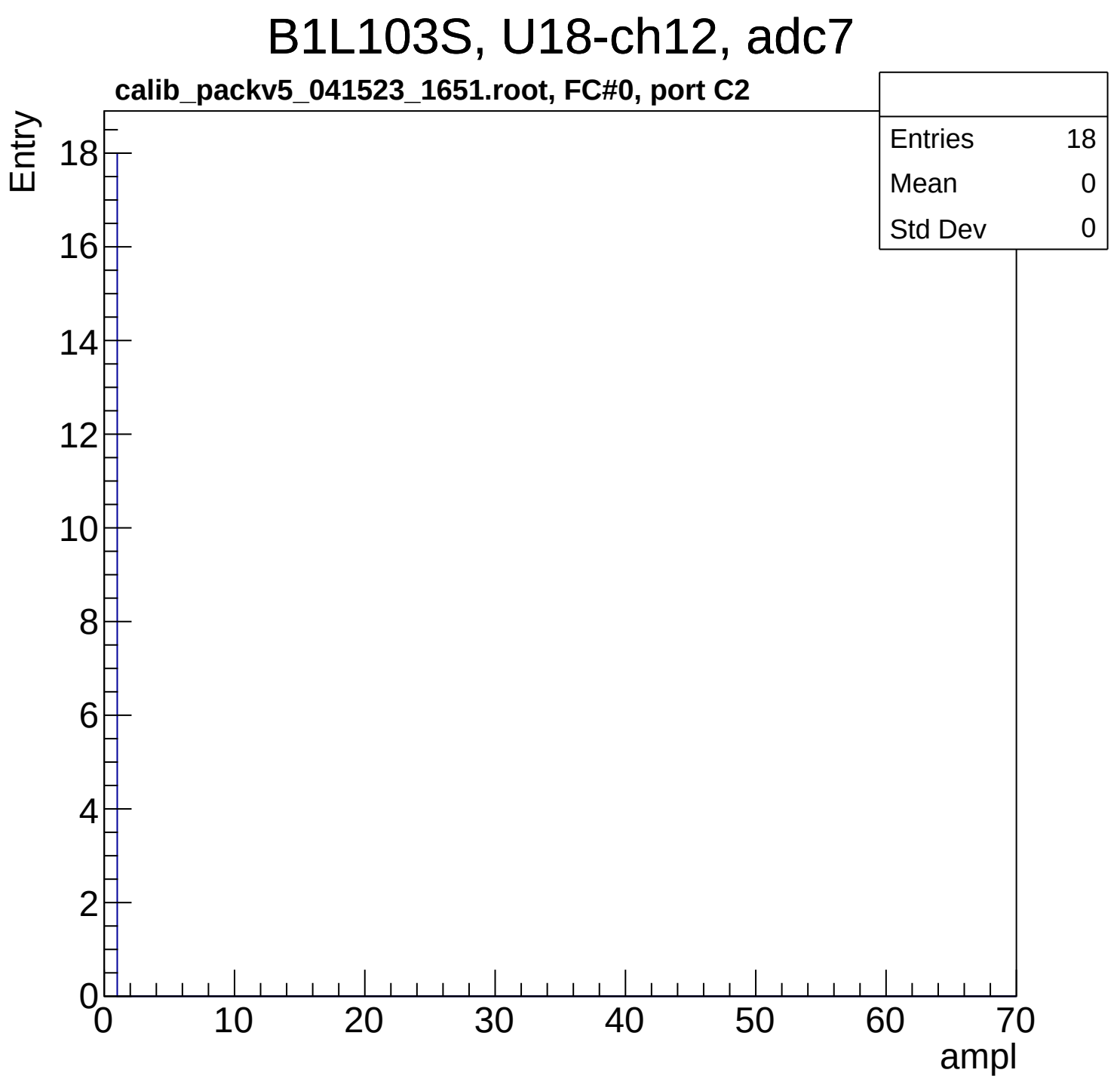
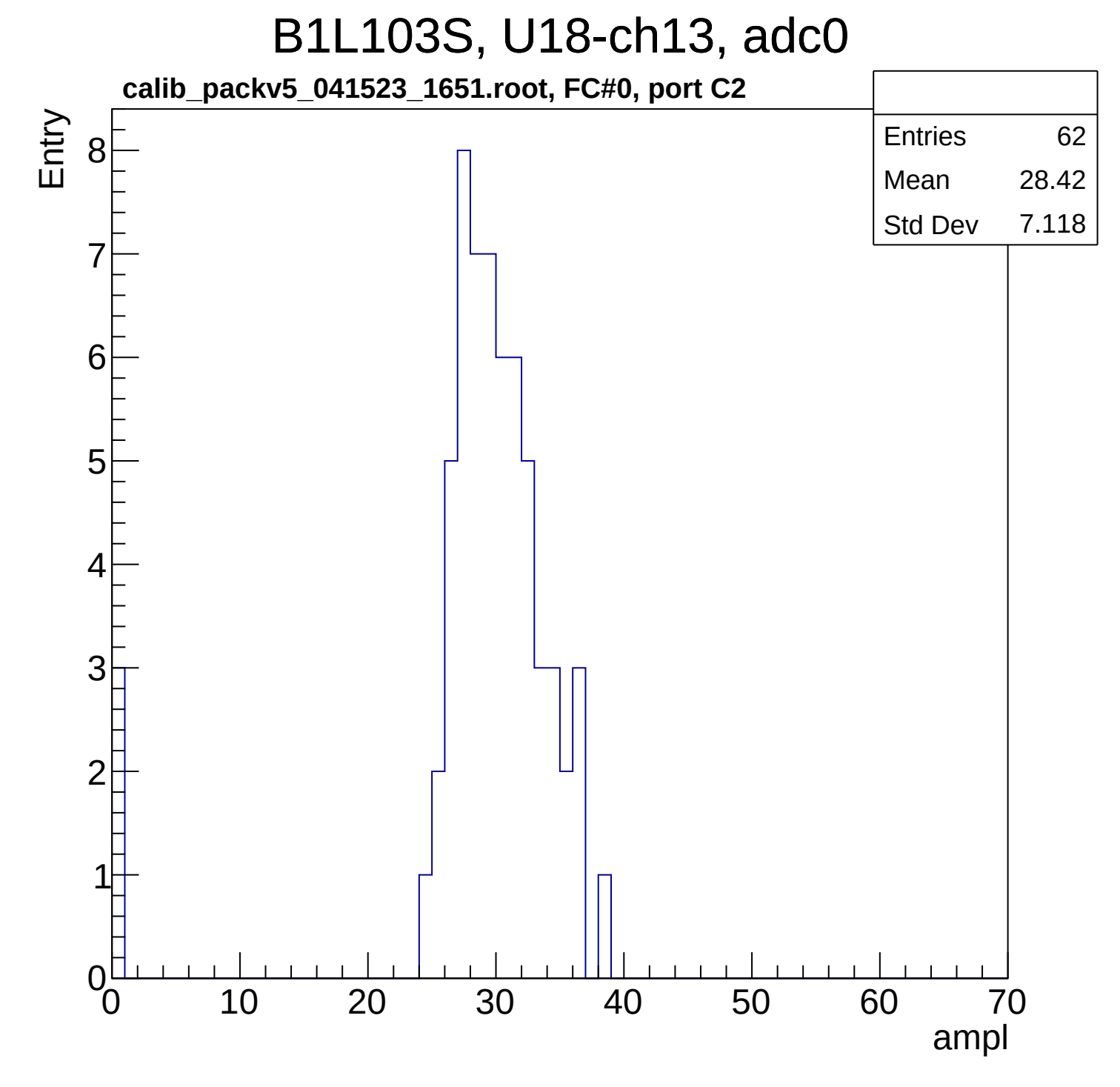

B1L103S, U18-ch12, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch13, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 28.42
Std Dev 7.118
Entry
ampl
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1
2
3
4
5
6
7
8
0
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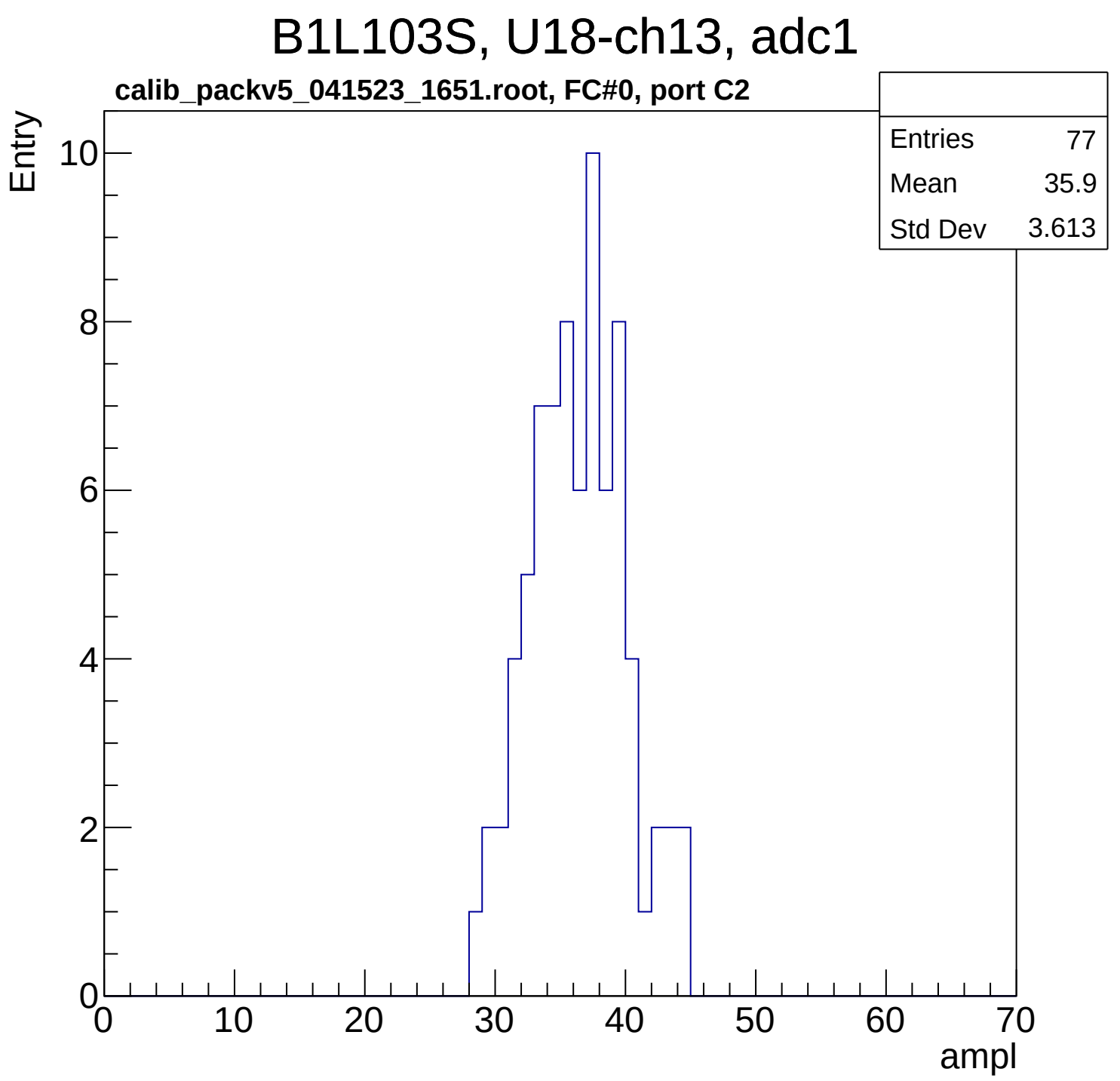
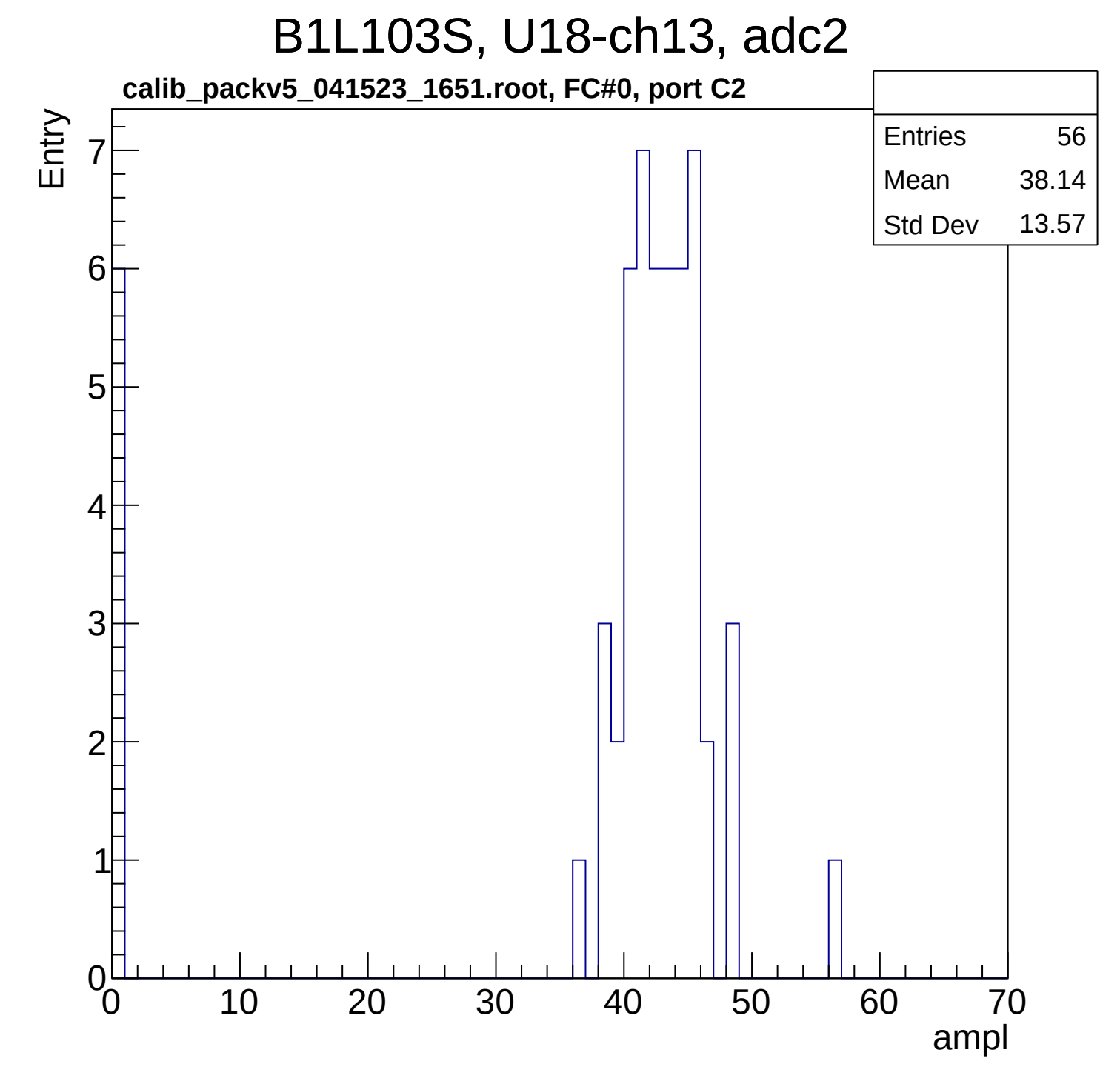
20
30
40
50
60
70


B1L103S, U18-ch13, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 35.9
Std Dev 3.613
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch13, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 38.14
Std Dev 13.57
Entry
ampl
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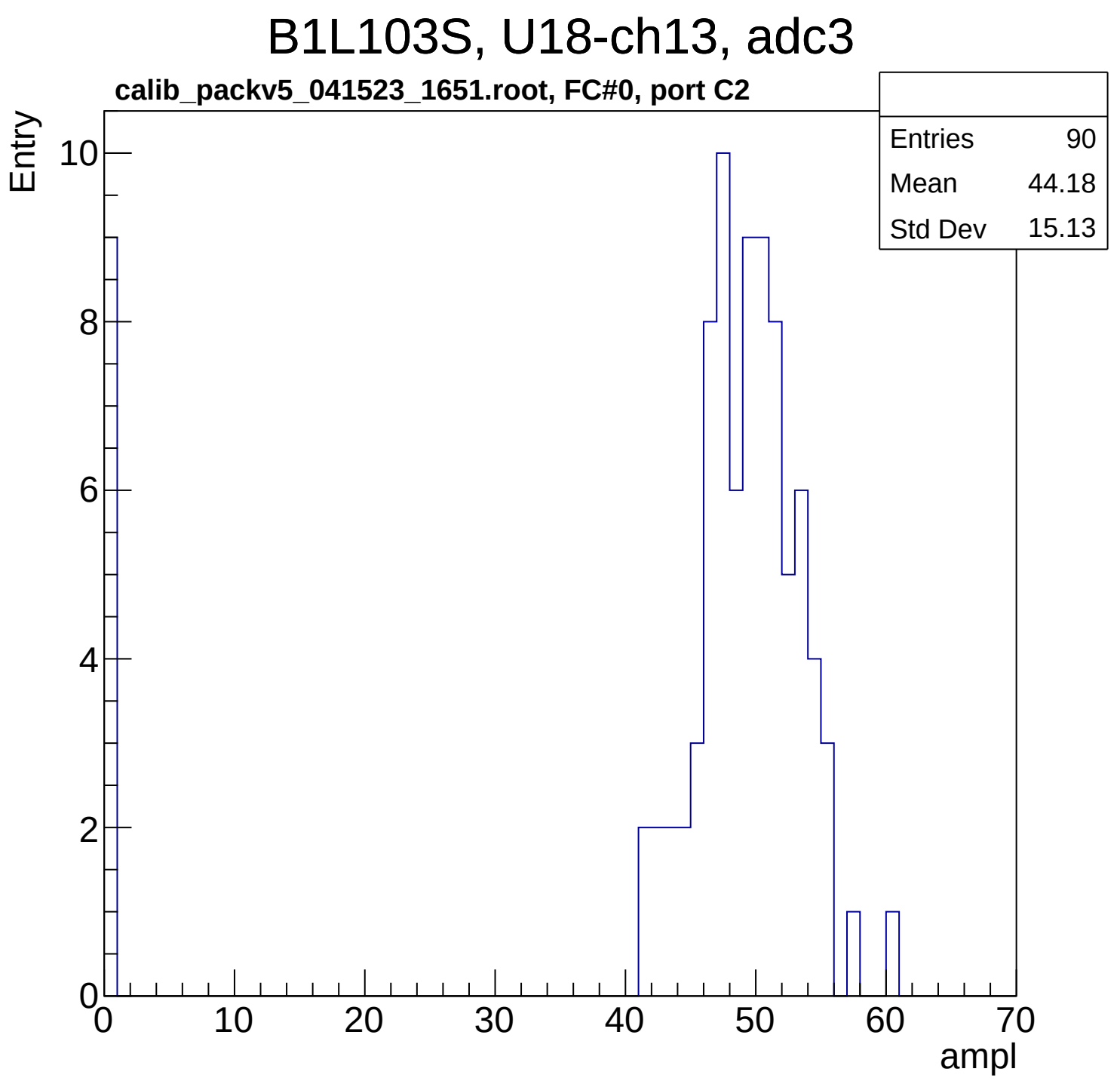
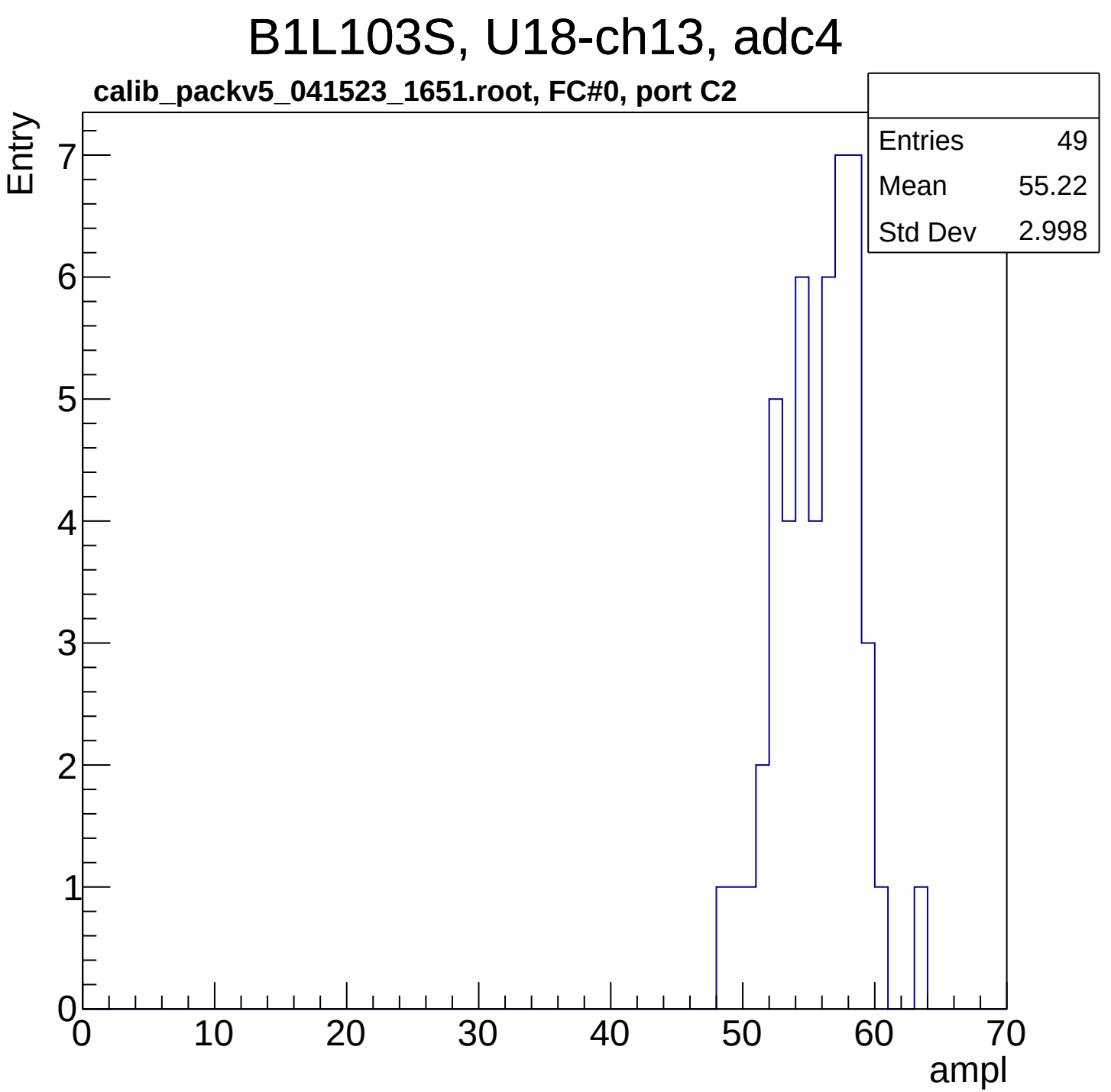
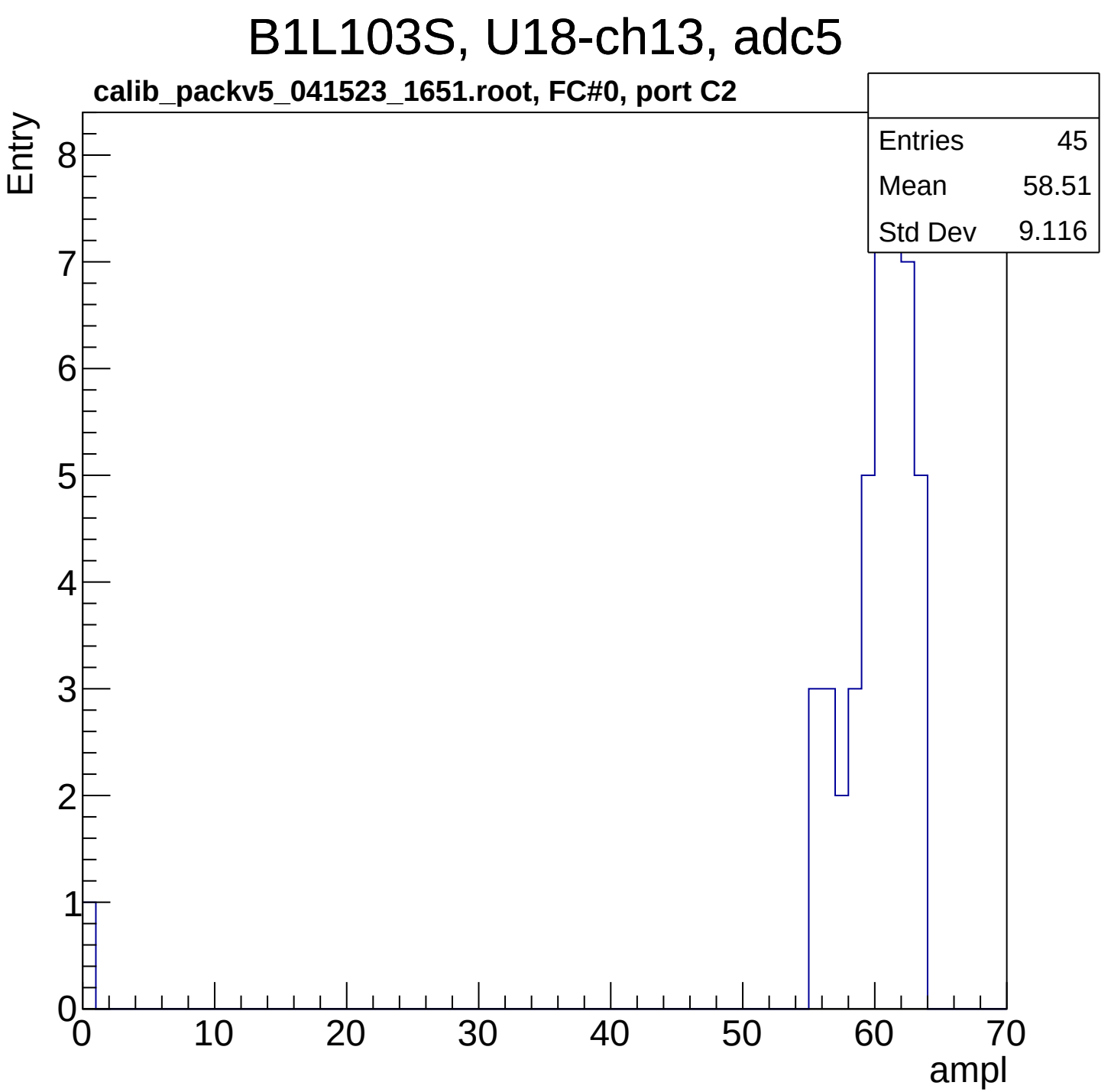
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U18-ch13, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 90
Mean 44.18
Std Dev 15.13
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U18-ch13, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 55.22
Std Dev 2.998
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U18-ch13, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 58.51
Std Dev 9.116
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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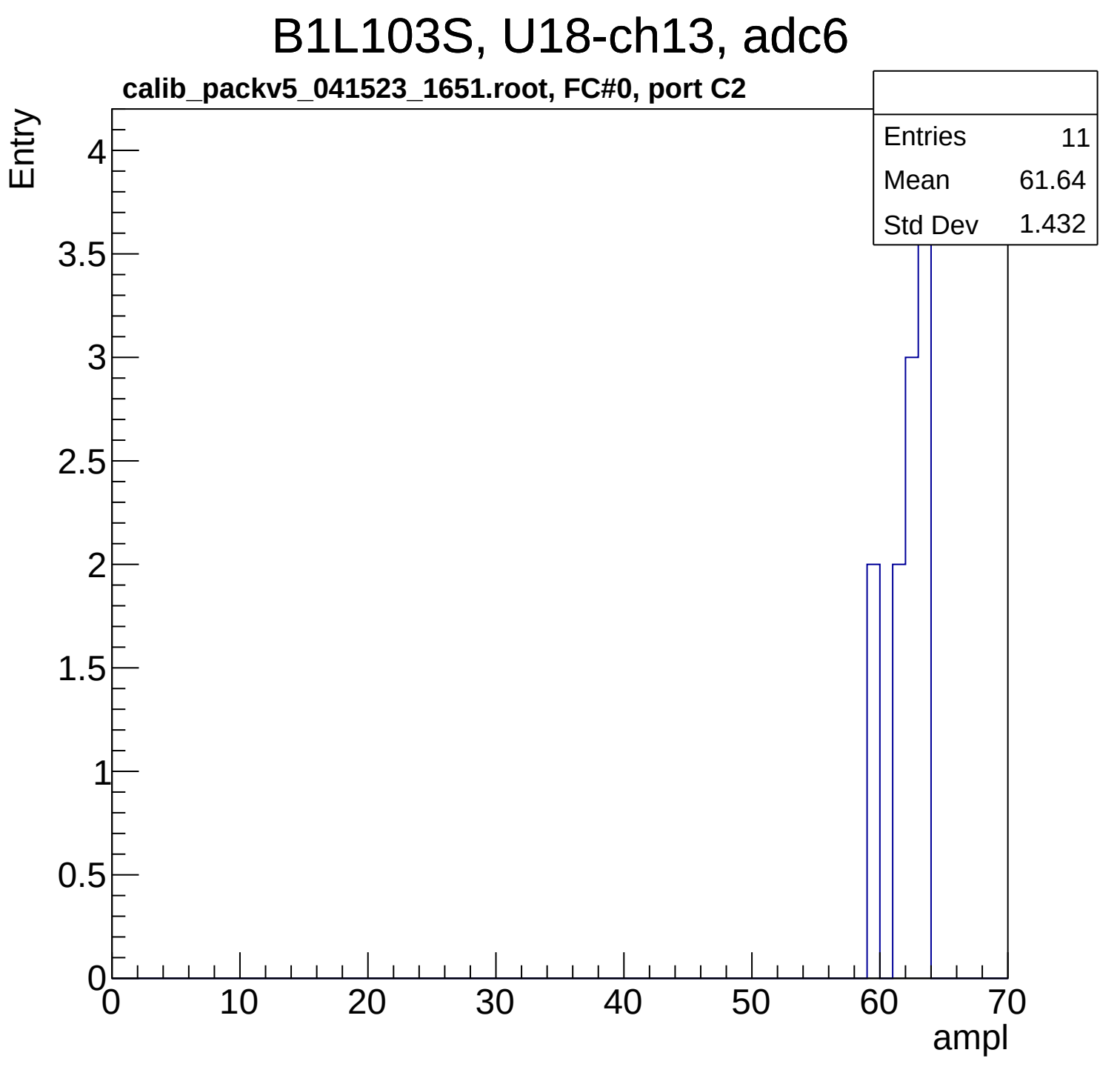
B1L103S, U18-ch13, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 61.64
Std Dev 1.432
Entry
ampl
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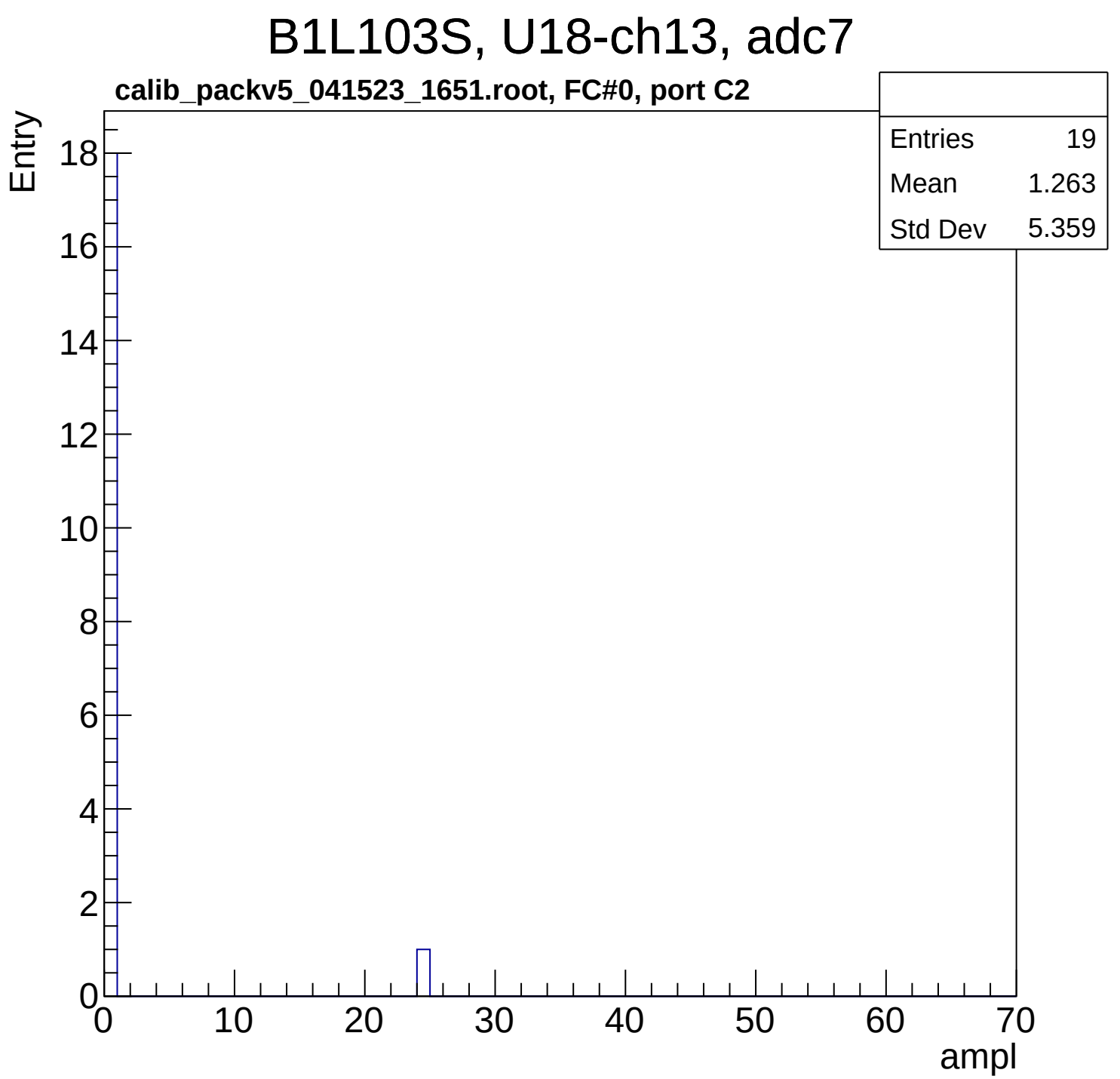
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U18-ch13, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.263
Std Dev 5.359
Entry
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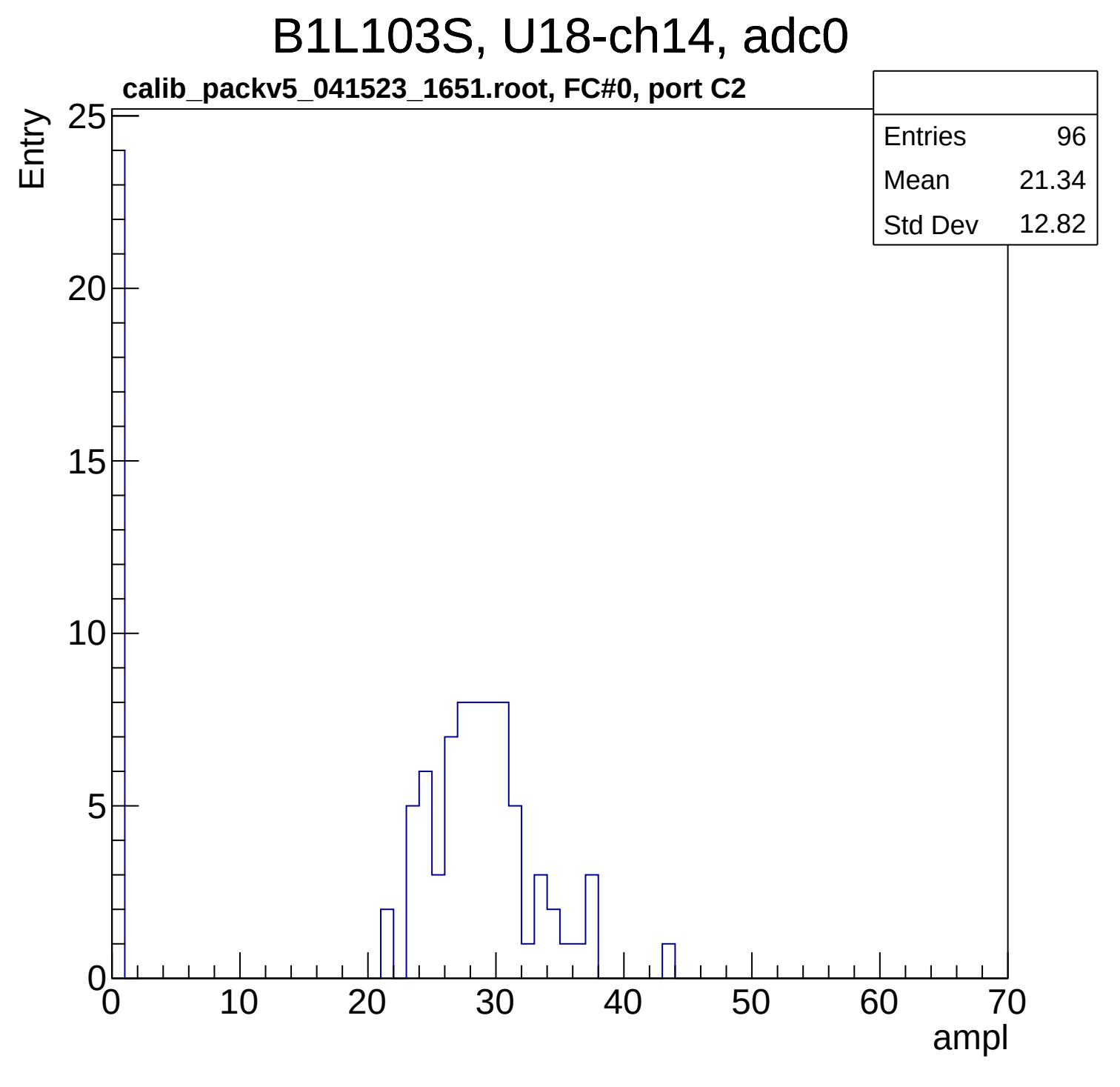
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch14, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 96
Mean 21.34
Std Dev 12.82
Entry
ampl
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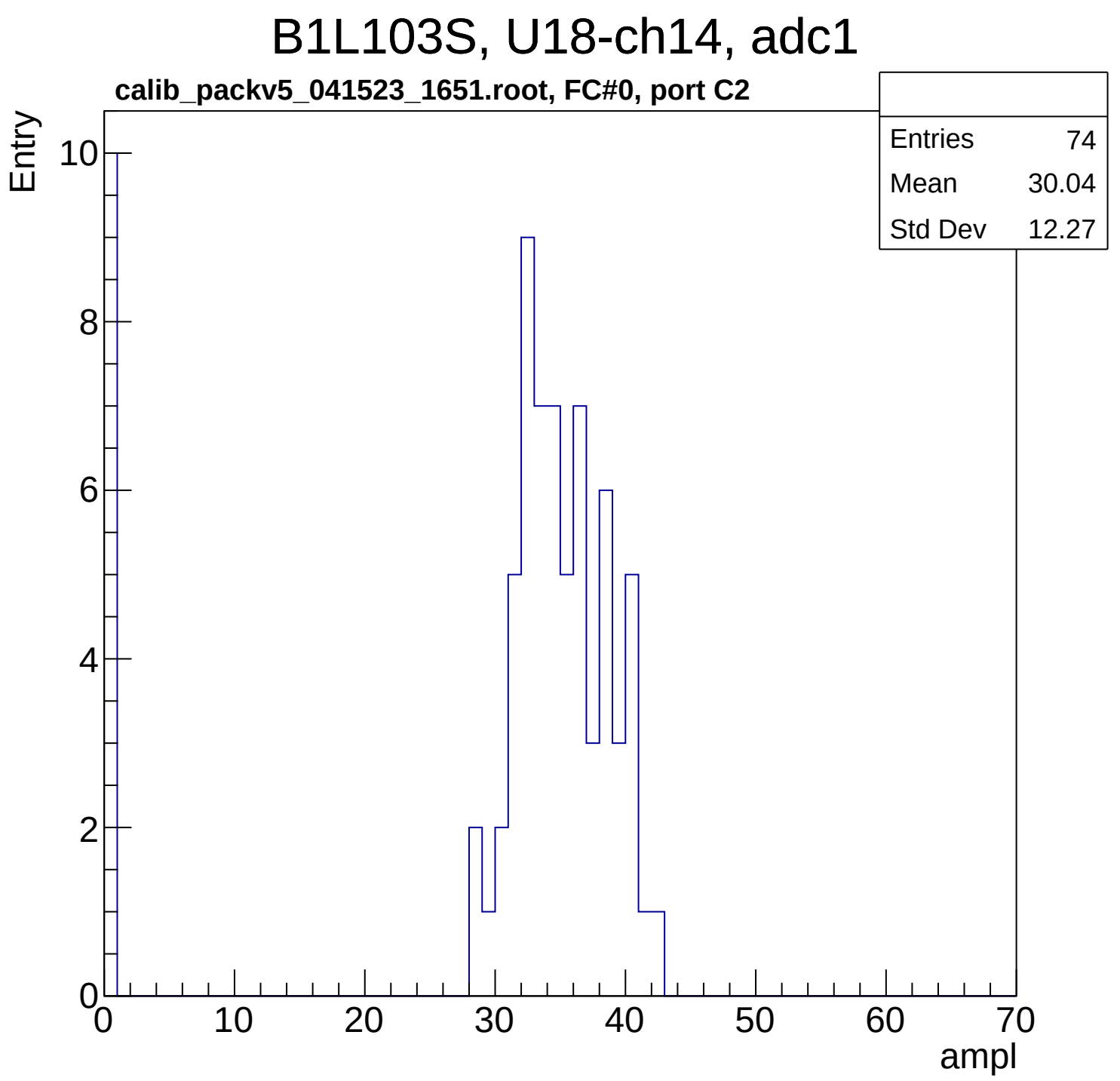
5
10
15
20
25
0
10
20
30
40
50
60
70


B1L103S, U18-ch14, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 30.04
Std Dev 12.27
Entry
ampl
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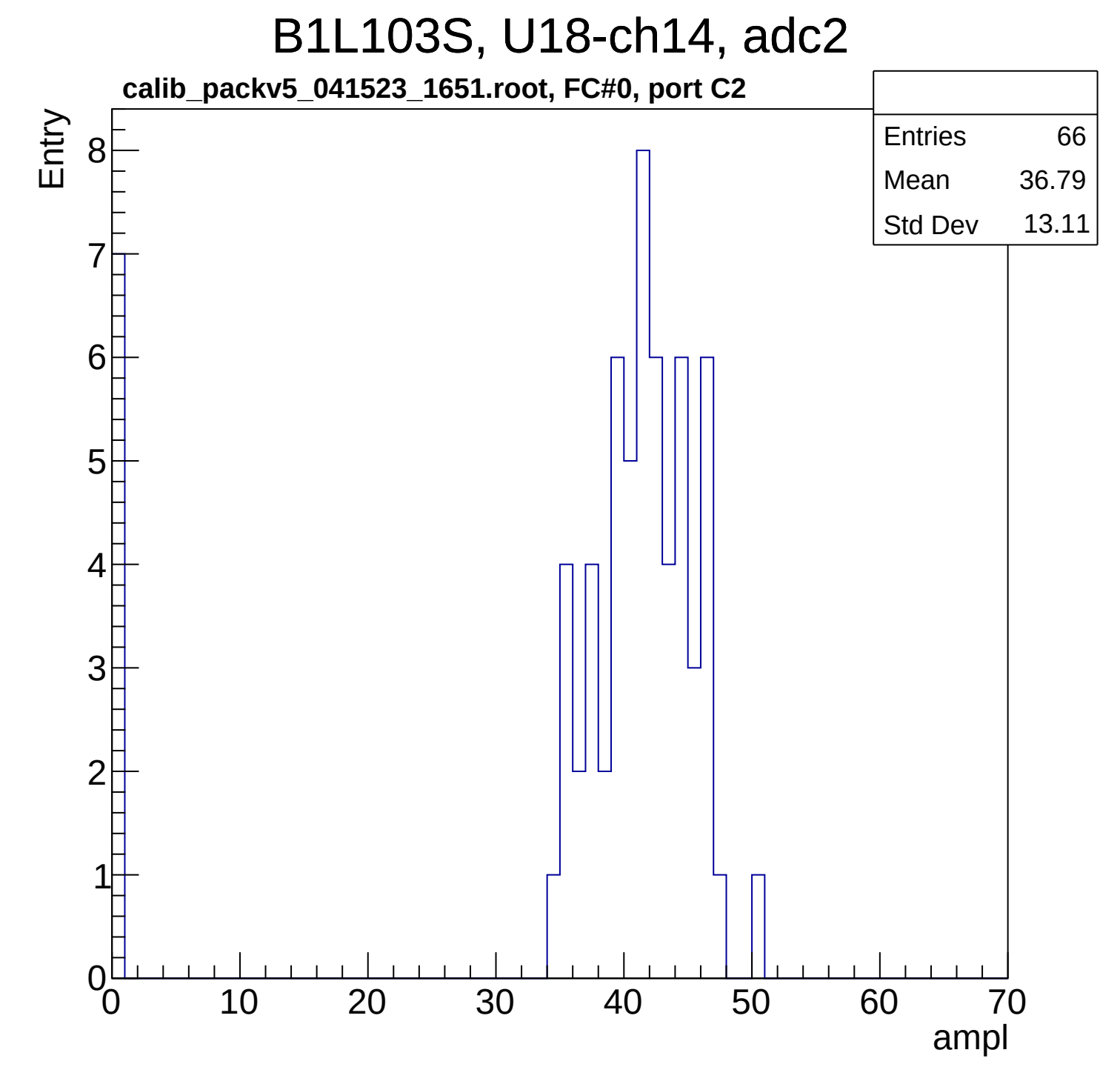
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U18-ch14, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 36.79
Std Dev 13.11
Entry
ampl
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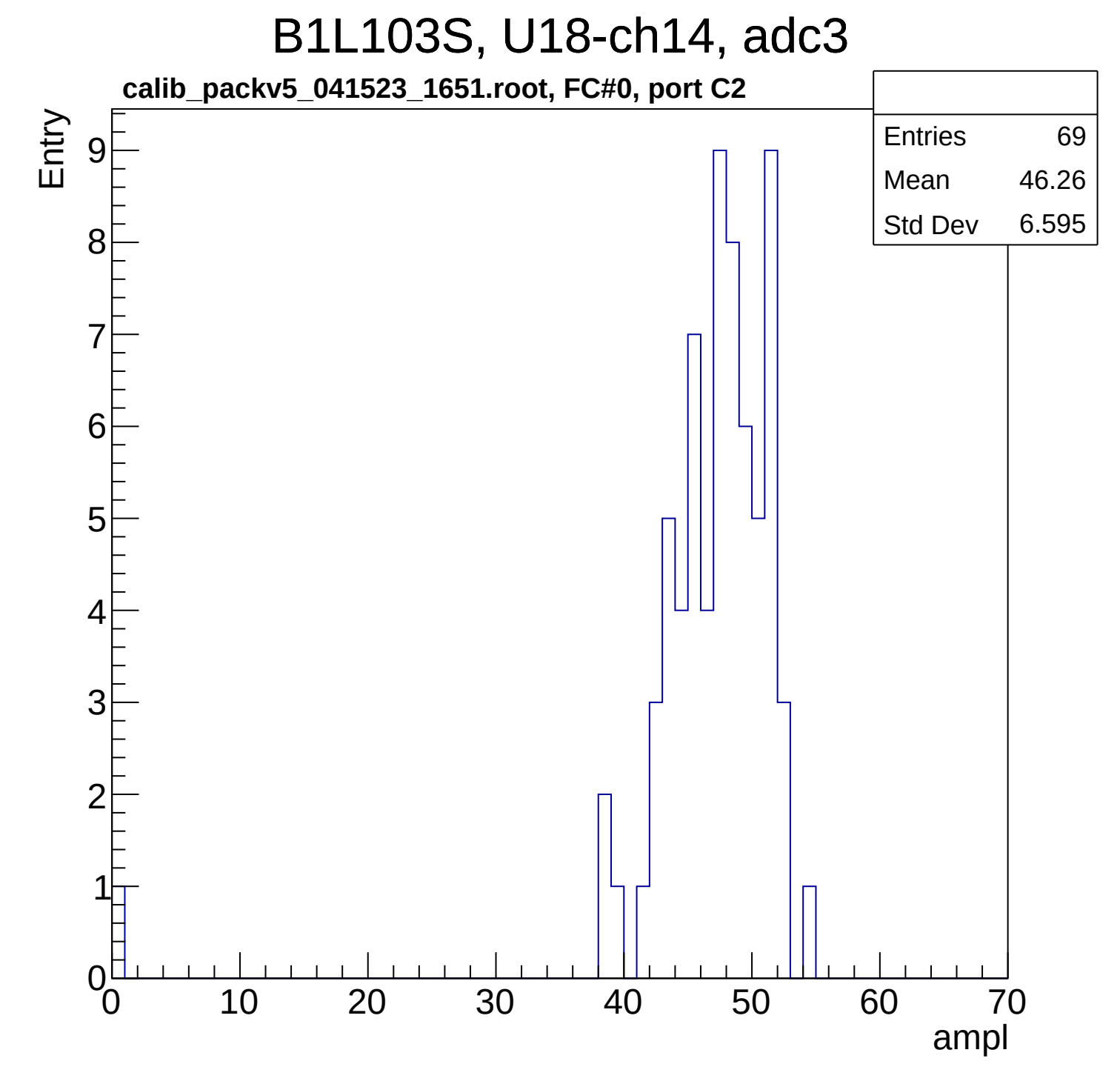
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch14, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 46.26
Std Dev 6.595
Entry
ampl
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3
4
5
6
7
8
9
0
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40
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60
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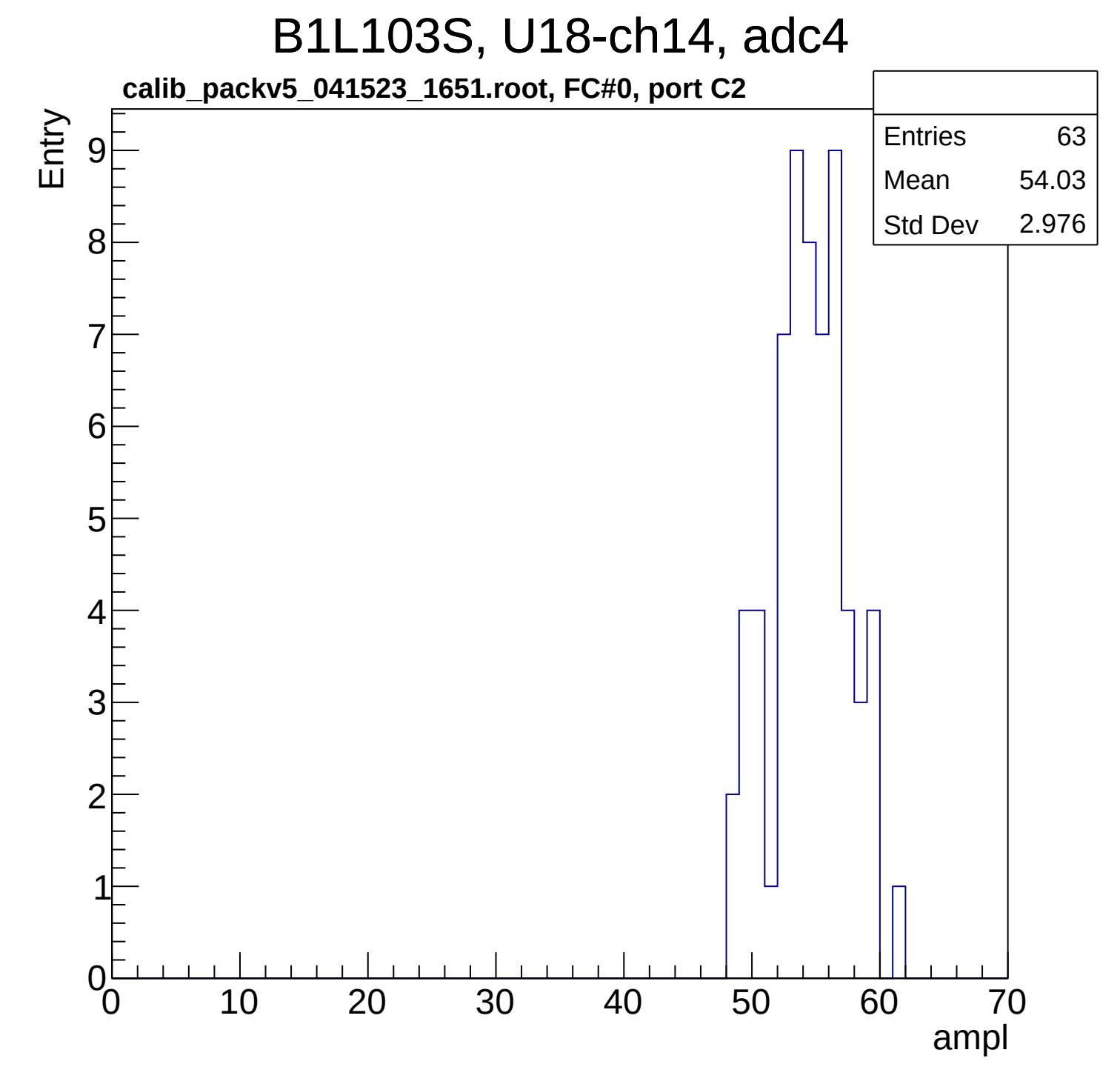
B1L103S, U18-ch14, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 54.03
Std Dev 2.976
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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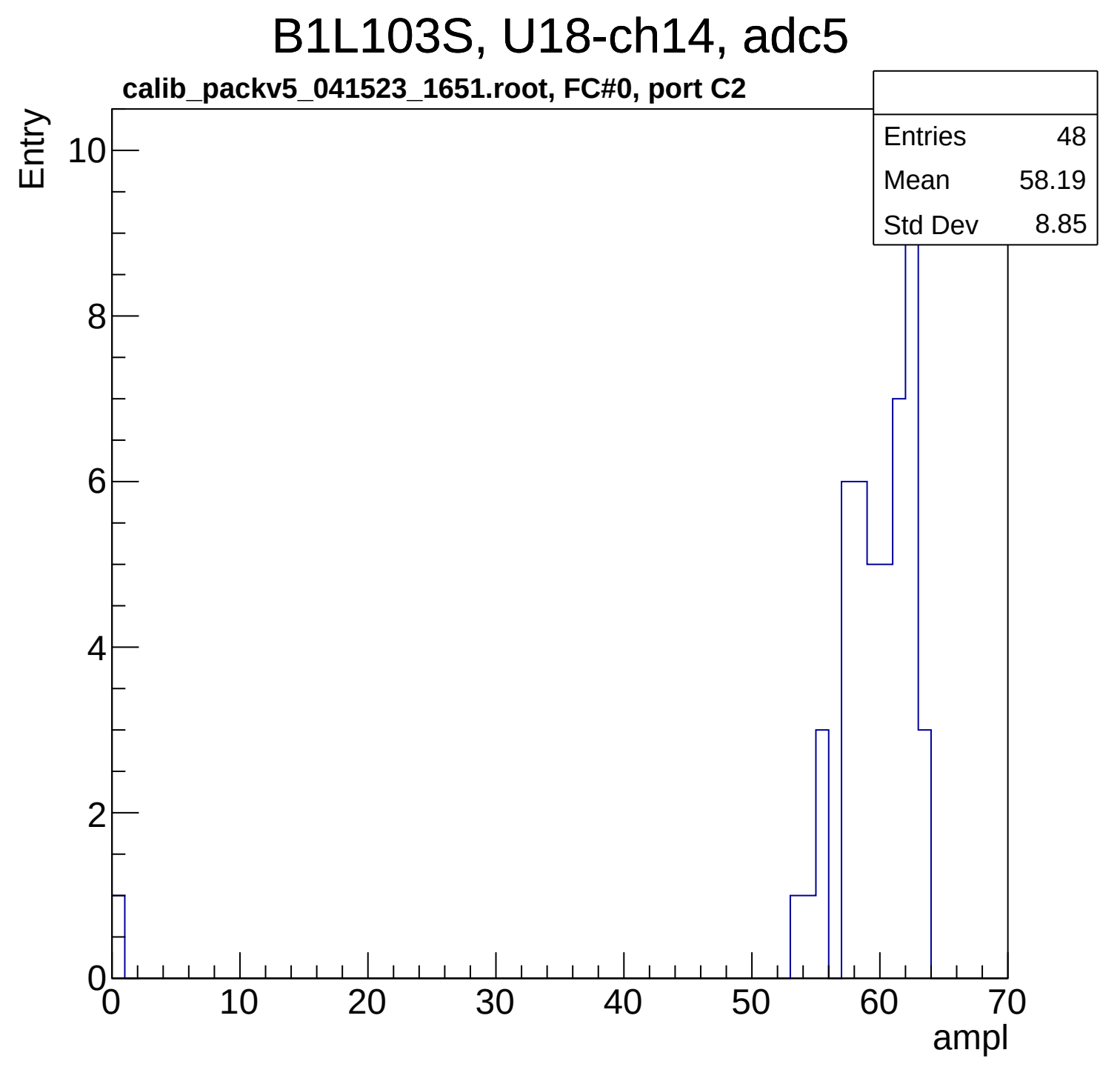
40
50
60
70


B1L103S, U18-ch14, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 58.19
Std Dev 8.85
Entry
ampl
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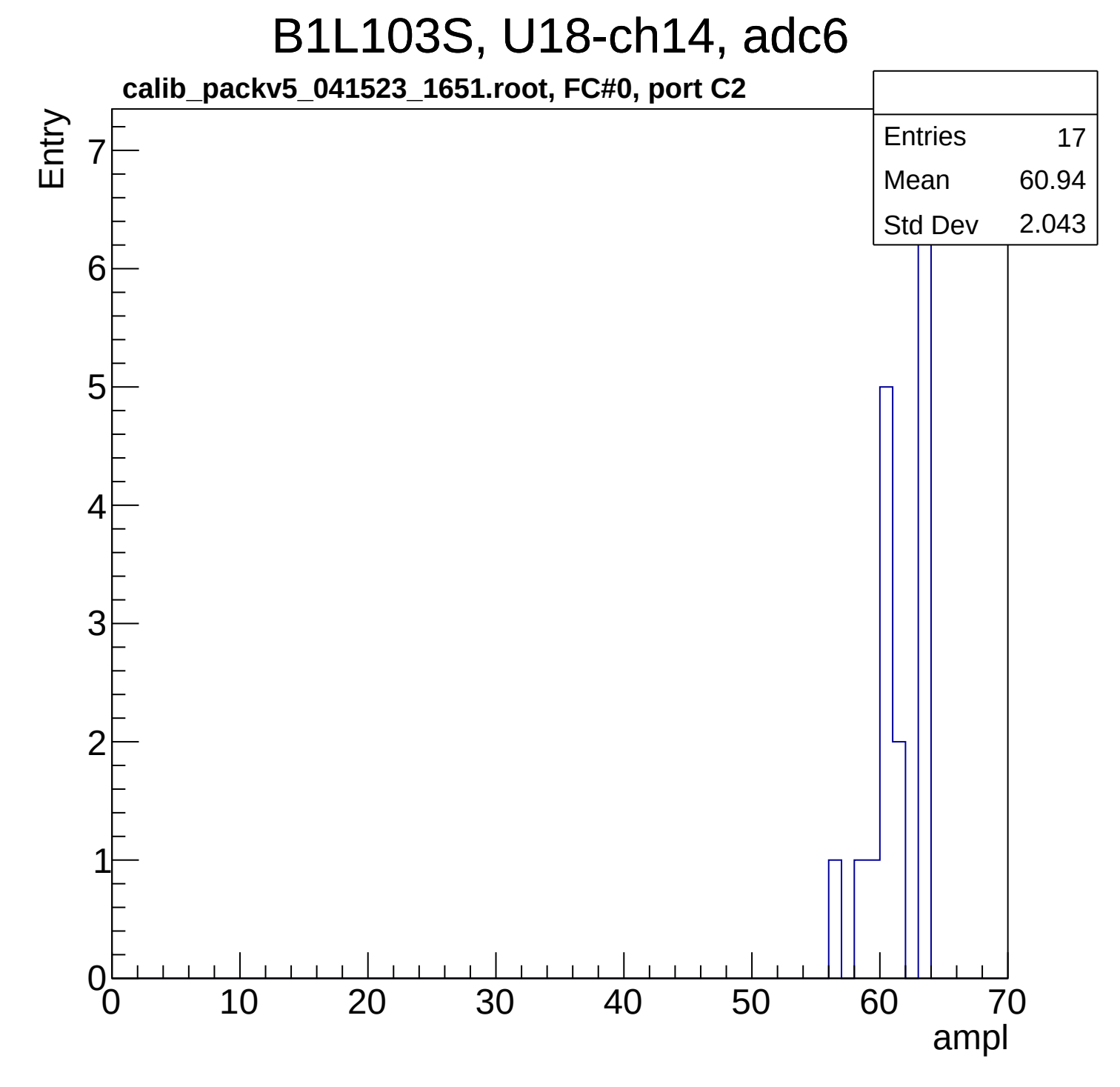
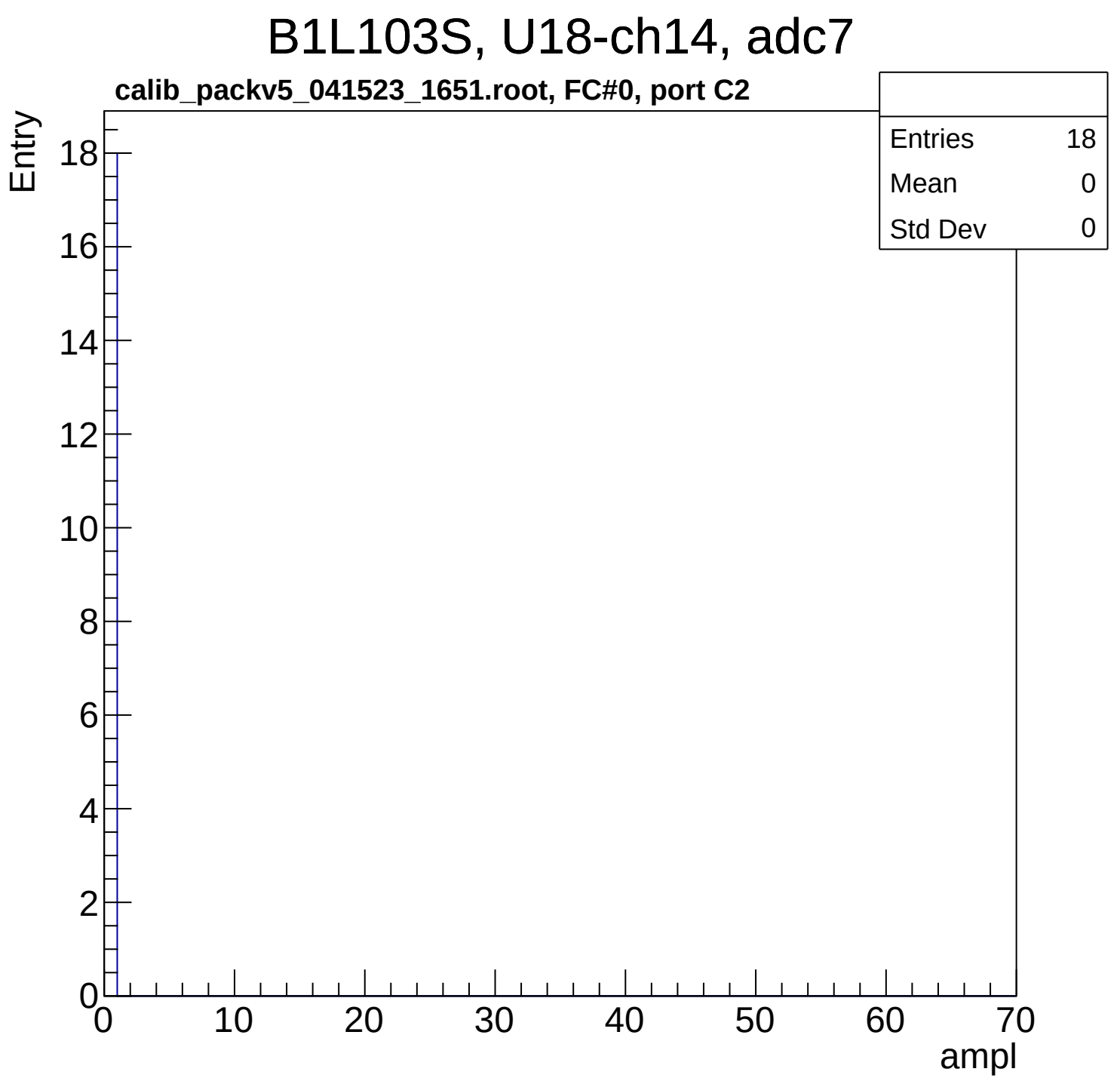
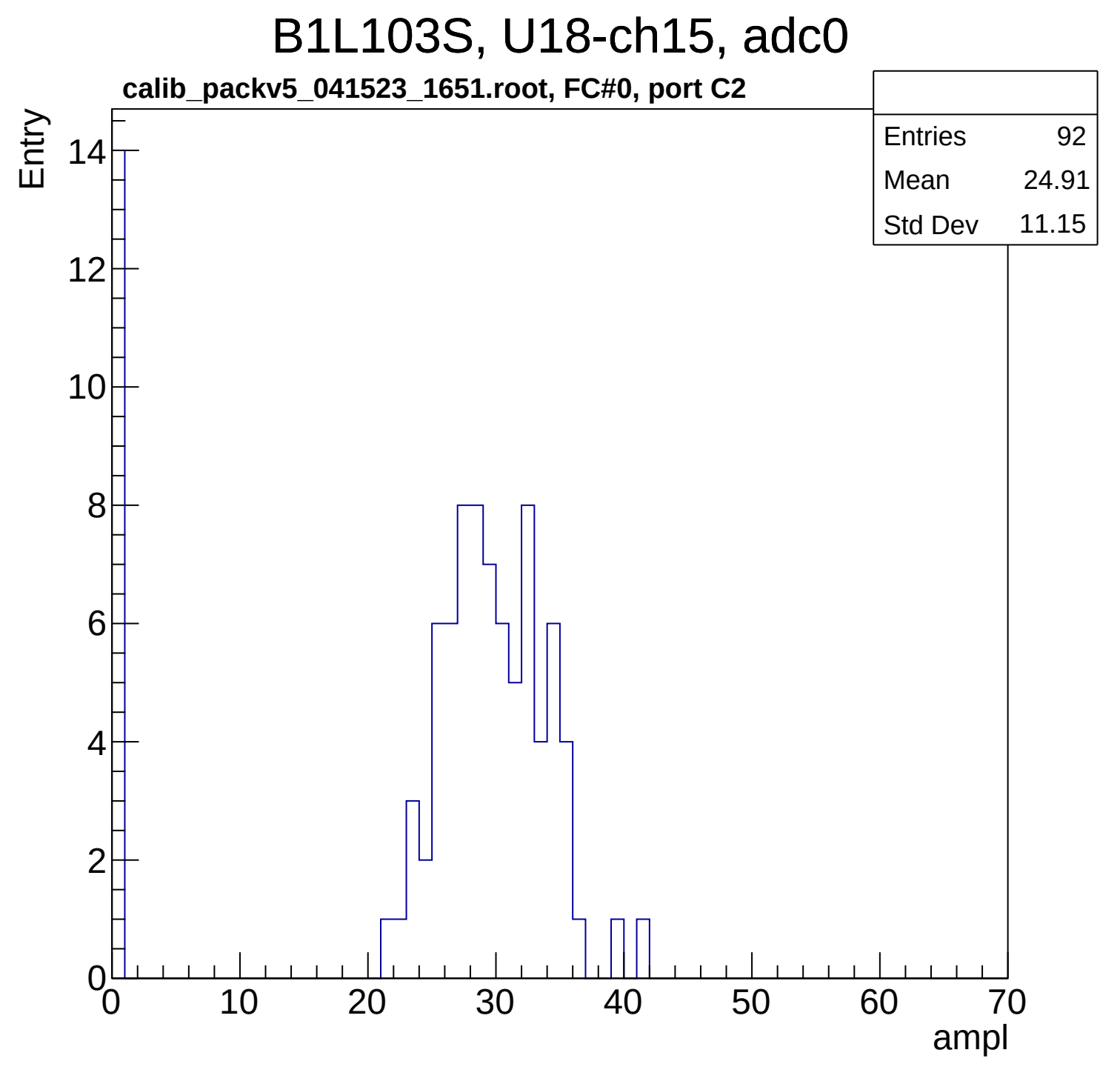
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U18-ch14, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 17
Mean 60.94
Std Dev 2.043
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U18-ch14, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch15, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 92
Mean 24.91
Std Dev 11.15
Entry
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4
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8
10
12
14
0
10
20
30
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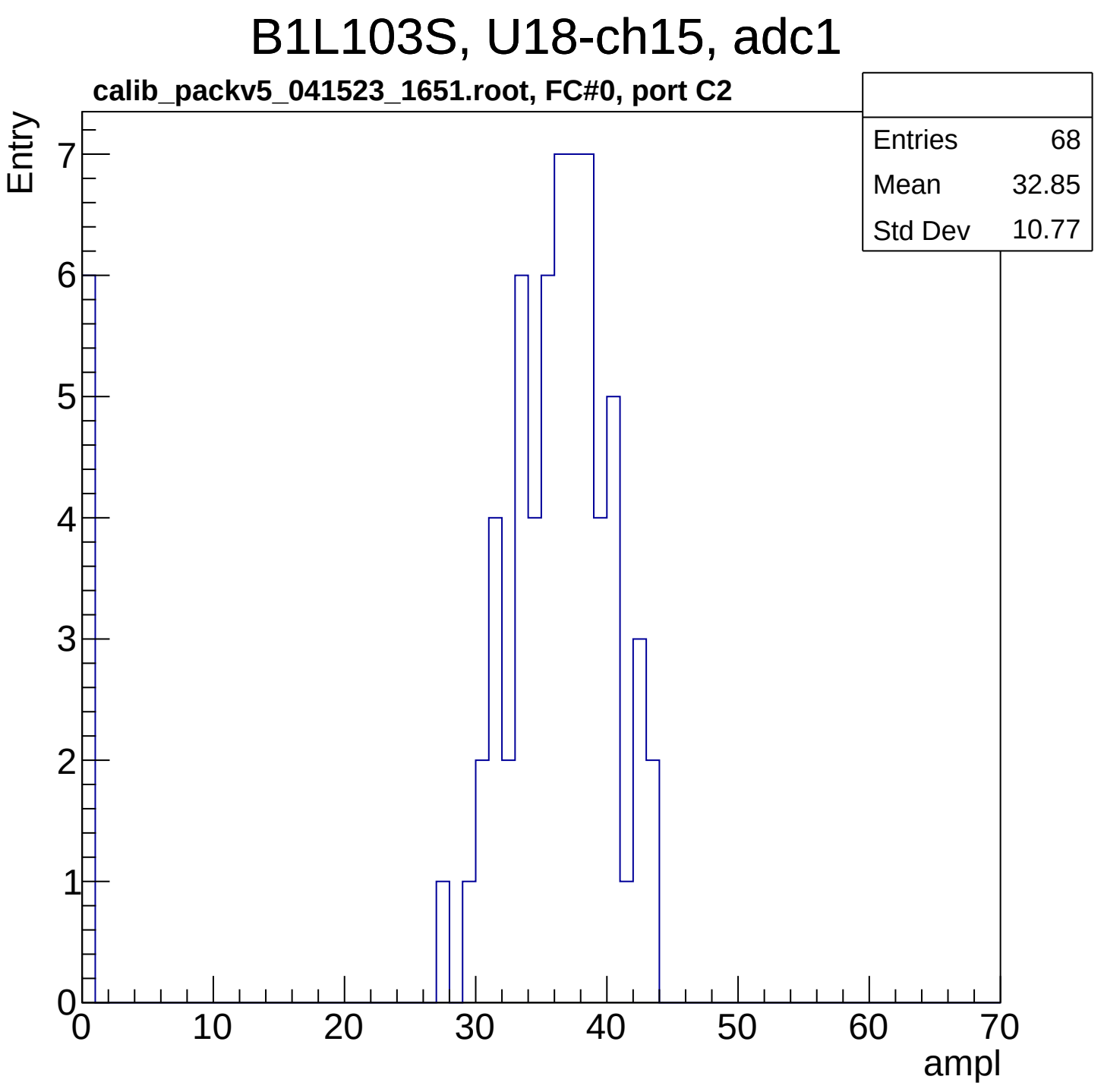
50
60
70
ampl


B1L103S, U18-ch15, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 32.85
Std Dev 10.77
Entry
ampl
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2
3
4
5
6
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0
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20
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40
50
60
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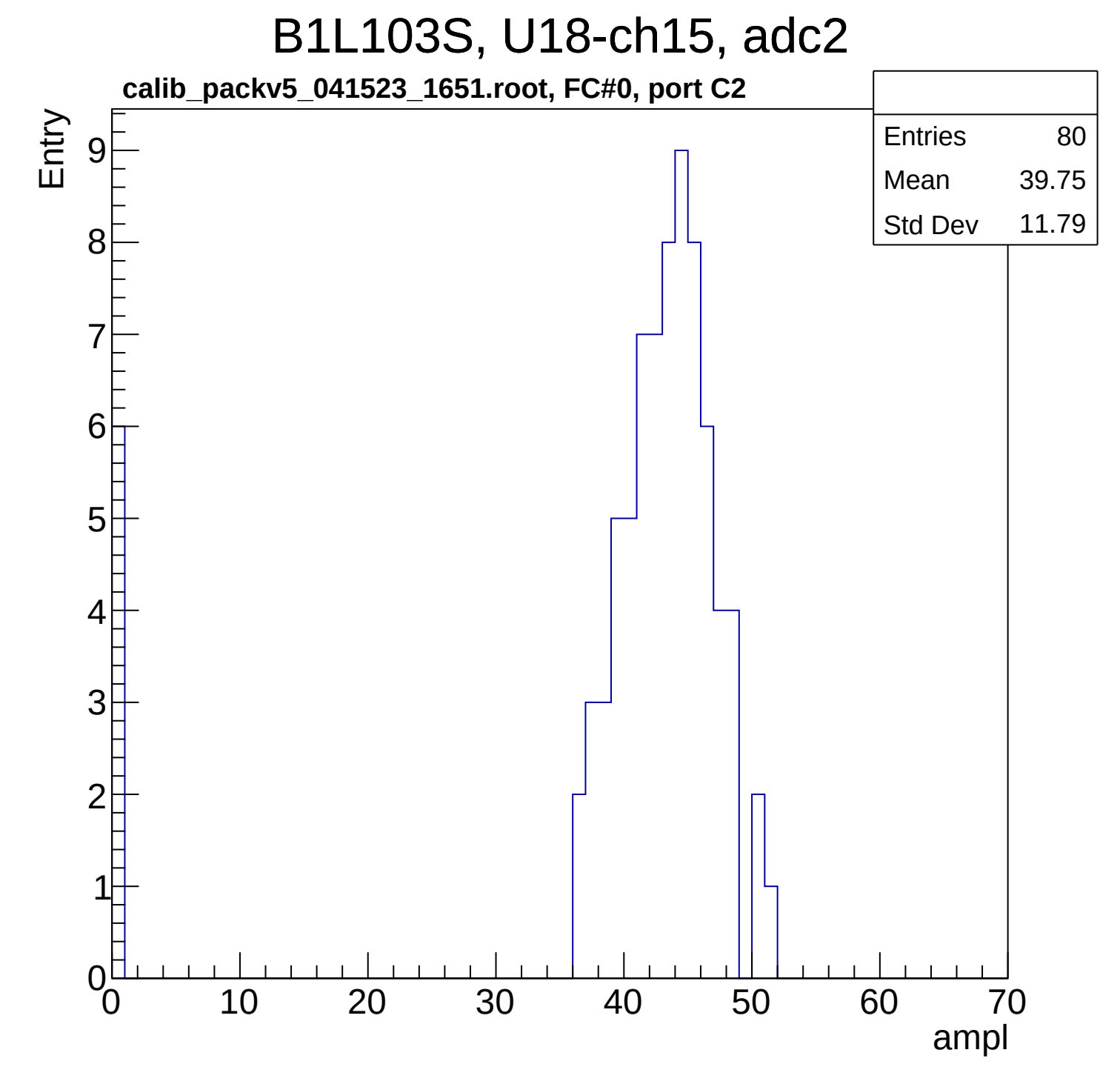
B1L103S, U18-ch15, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 39.75
Std Dev 11.79
Entry
ampl
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6
7
8
9
0
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60
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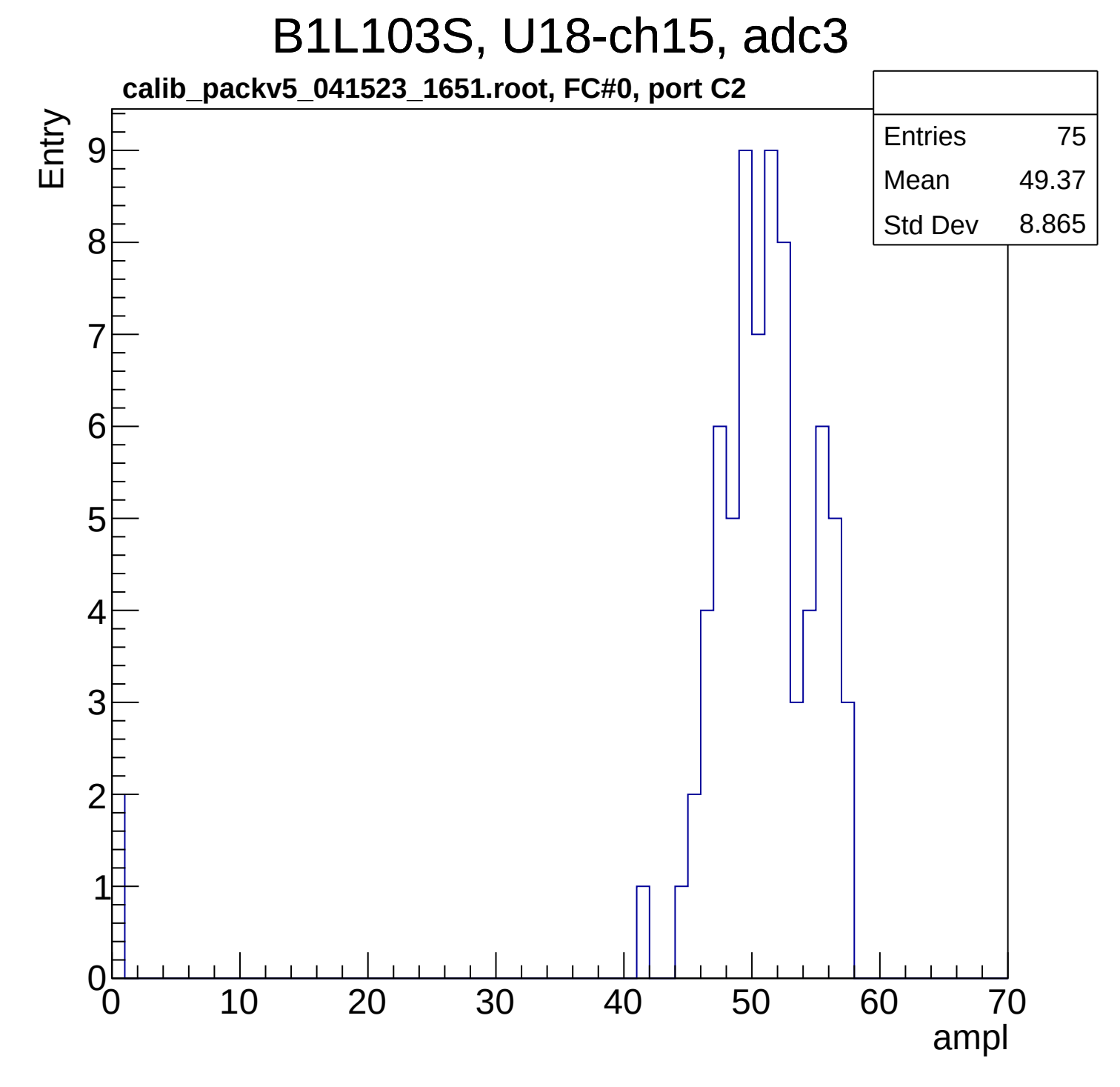
B1L103S, U18-ch15, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 49.37
Std Dev 8.865
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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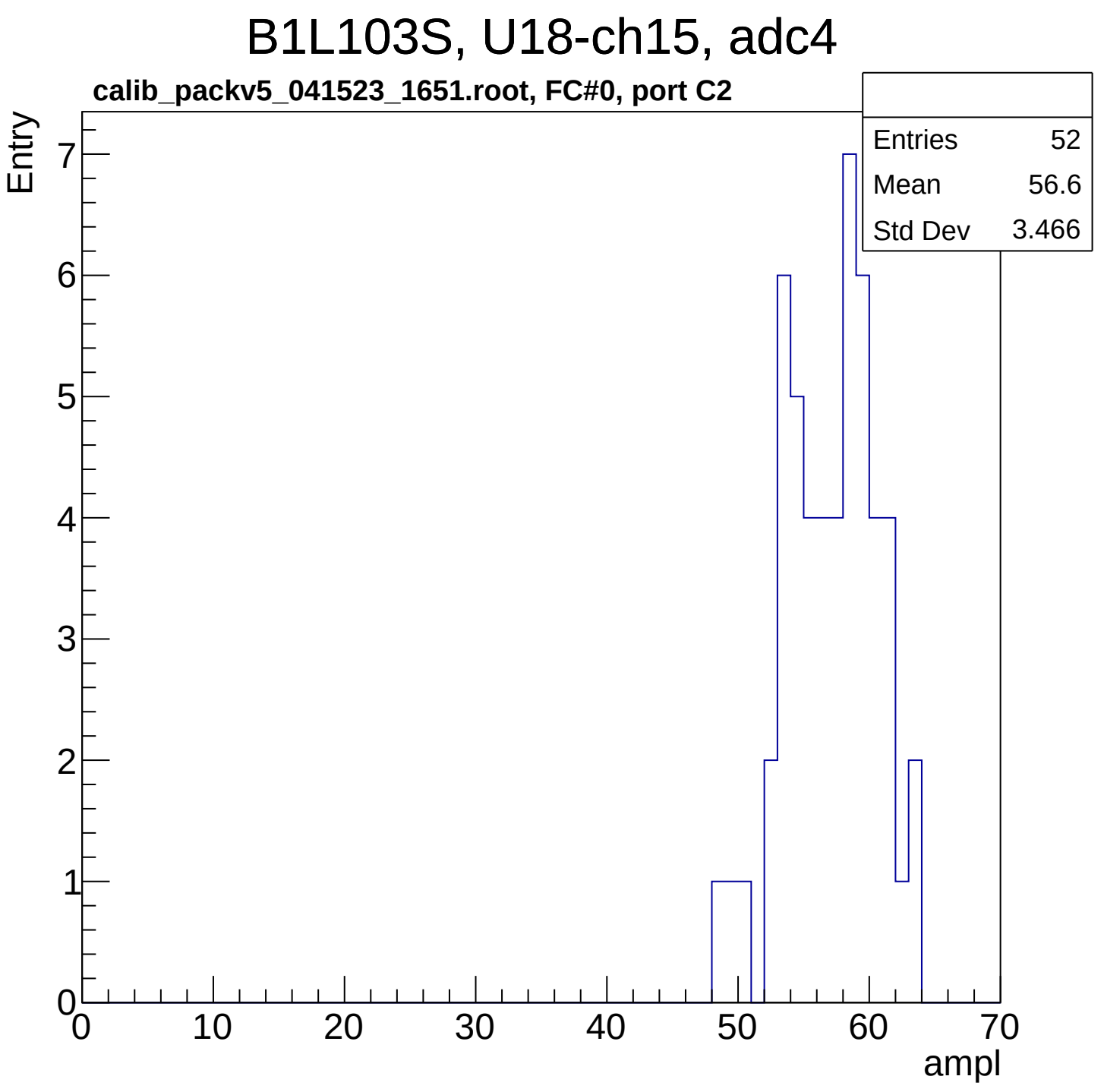
40
50
60
70


B1L103S, U18-ch15, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 56.6
Std Dev 3.466
Entry
ampl
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2
3
4
5
6
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0
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20
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40
50
60
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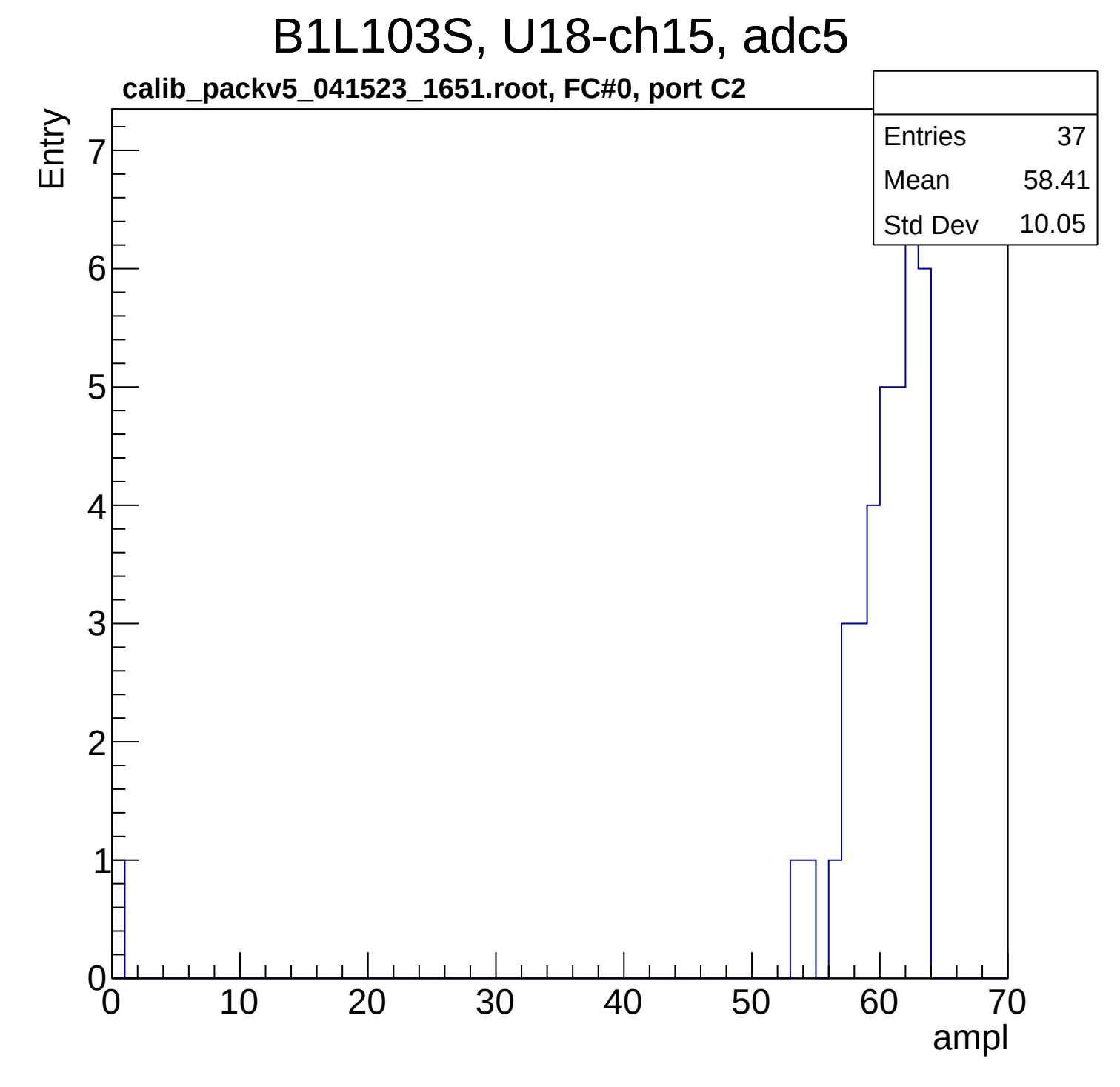
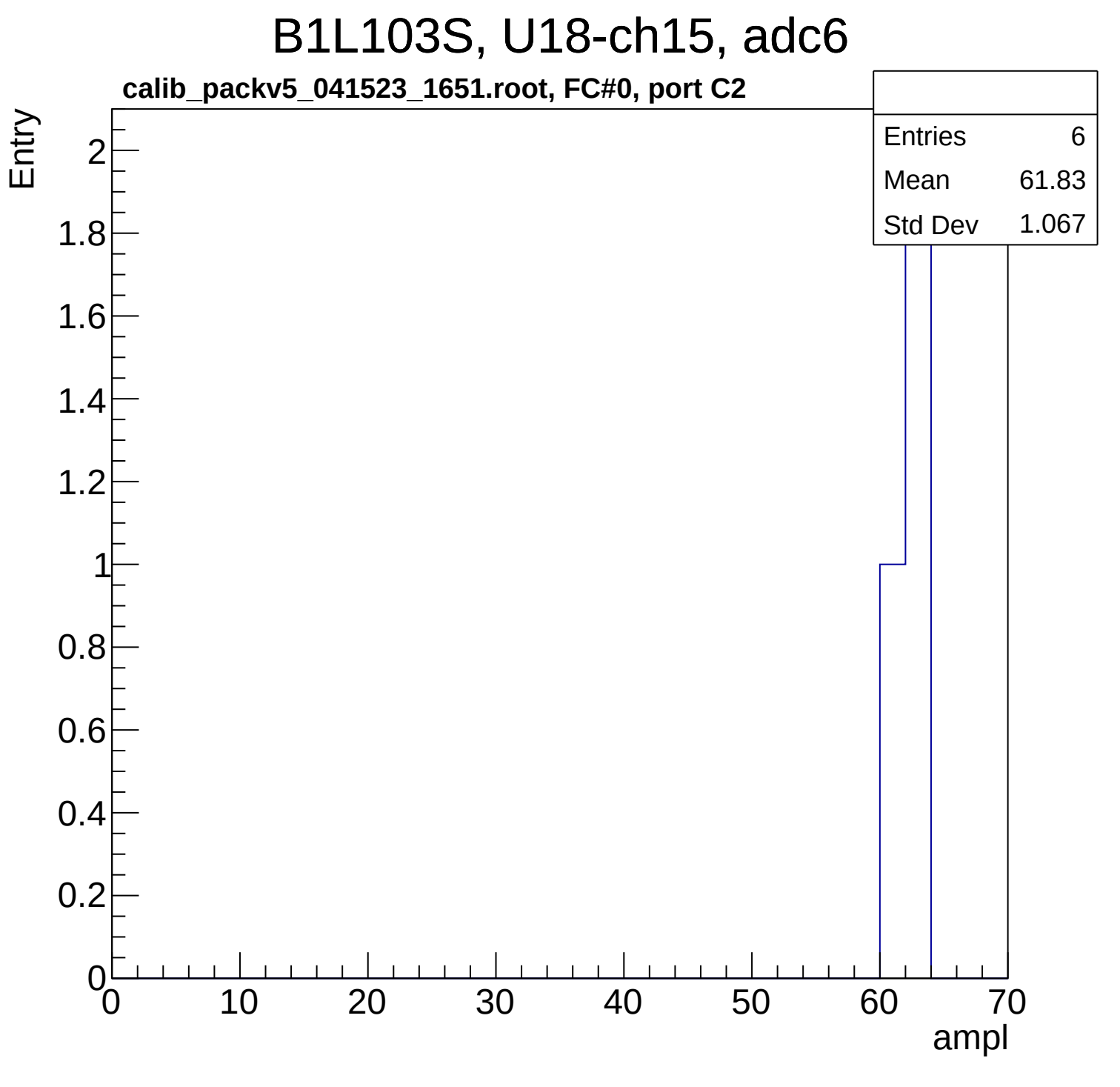

B1L103S, U18-ch15, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 37
Mean 58.41
Std Dev 10.05
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U18-ch15, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 61.83
Std Dev 1.067
Entry
ampl
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0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
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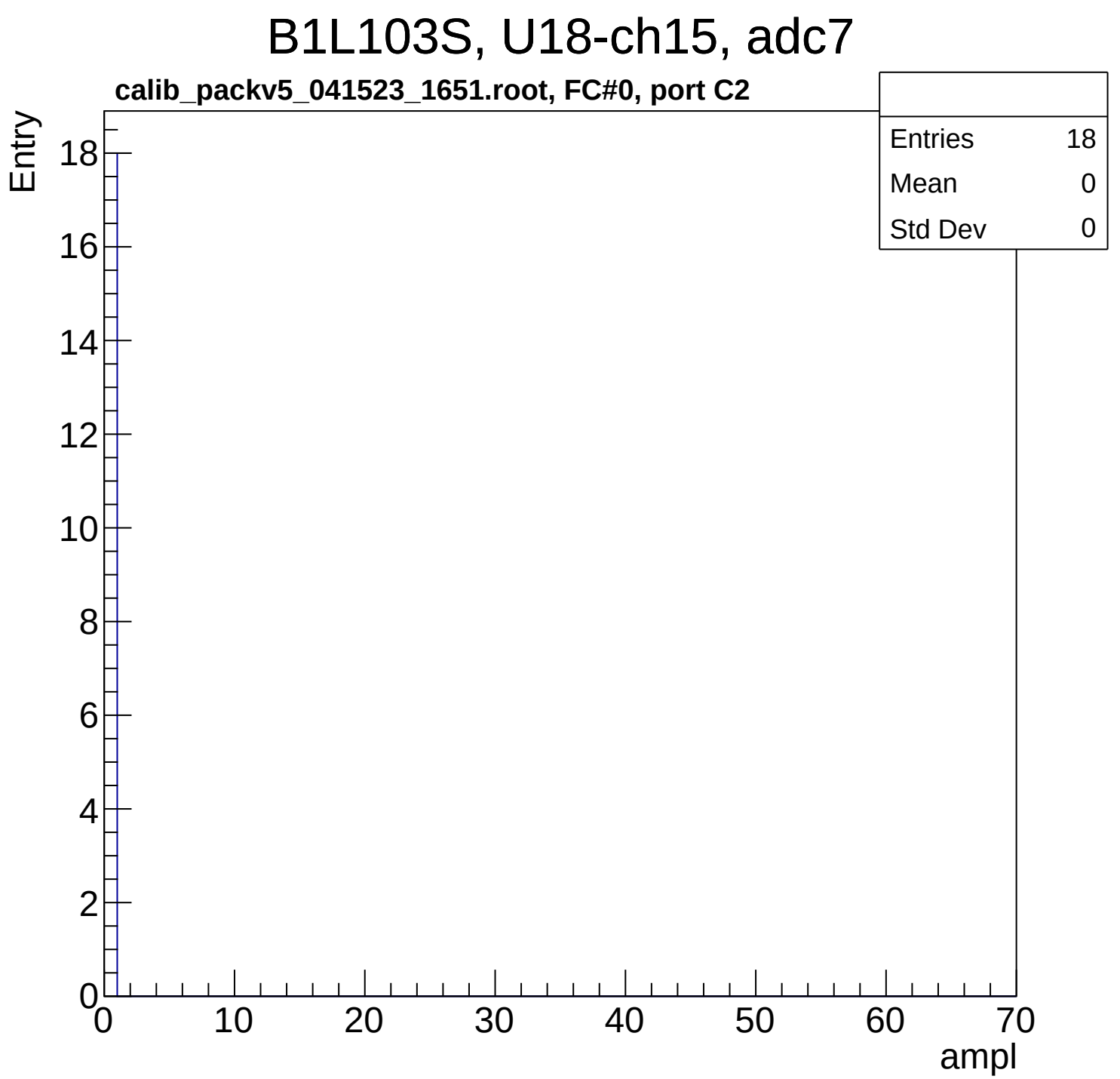
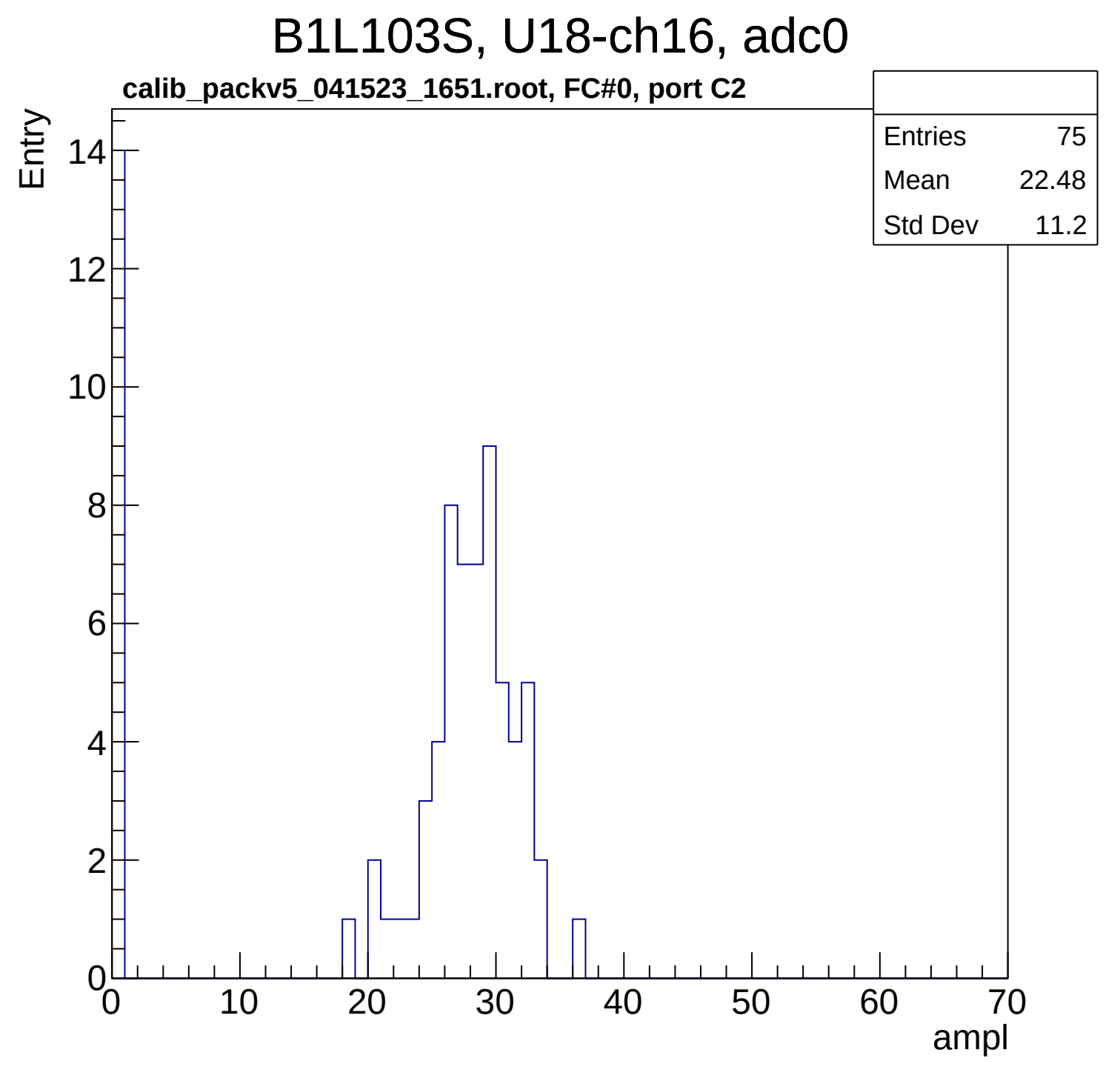
40
50
60
70


B1L103S, U18-ch15, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch16, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 22.48
Std Dev 11.2
Entry
ampl
0
2
4
6
8
10
12
14
0
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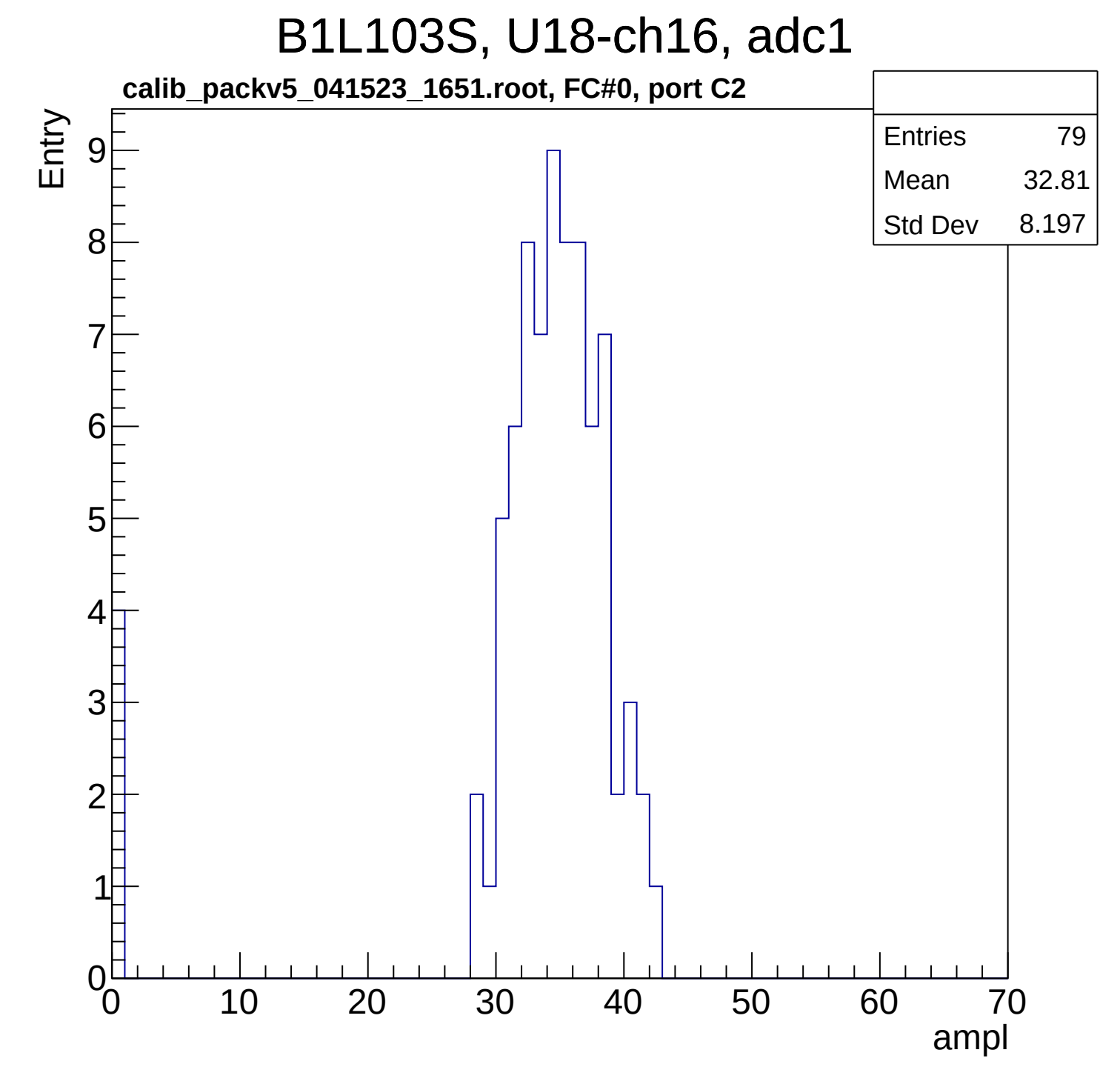
40
50
60
70


B1L103S, U18-ch16, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 32.81
Std Dev 8.197
Entry
ampl
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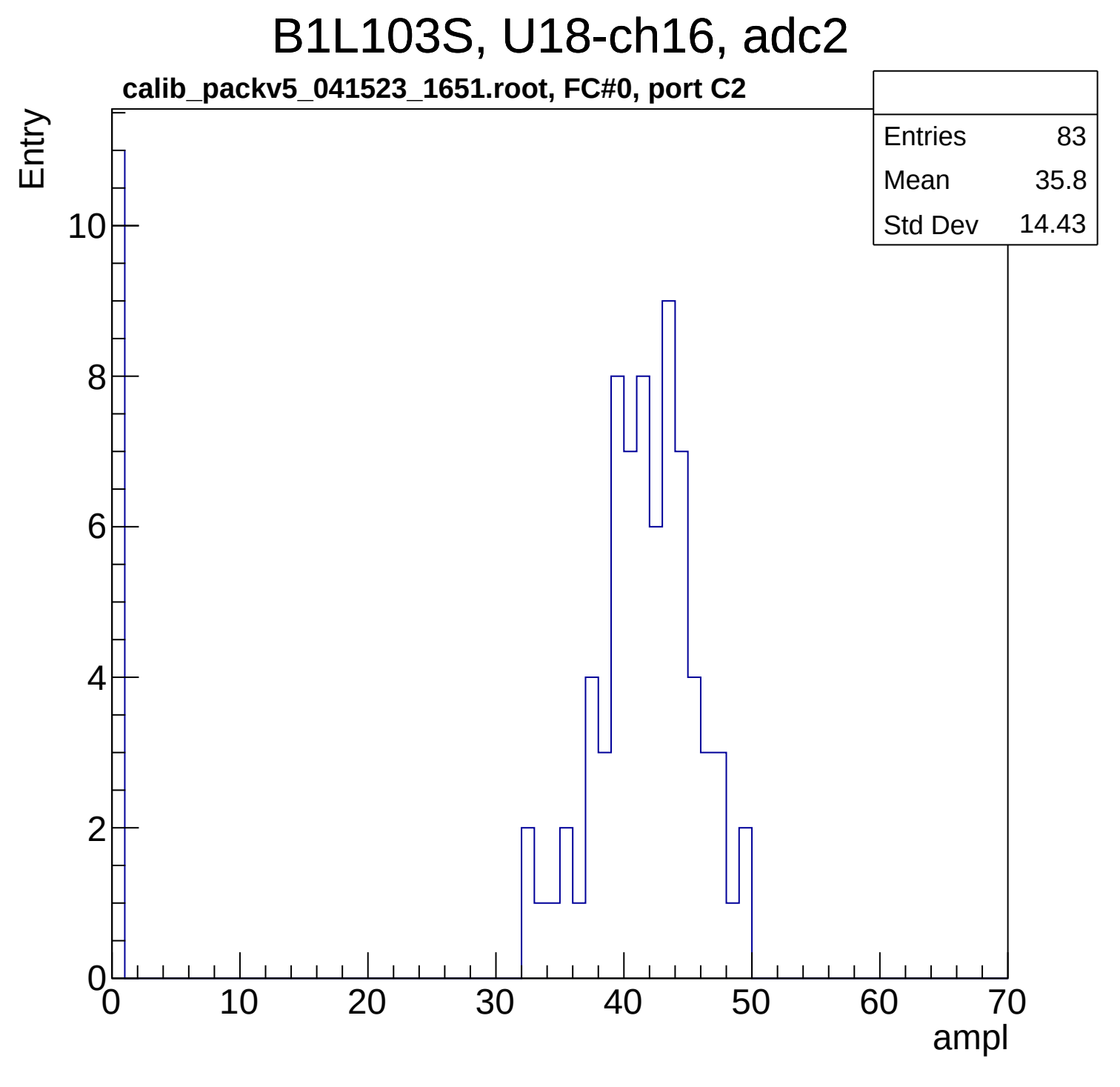
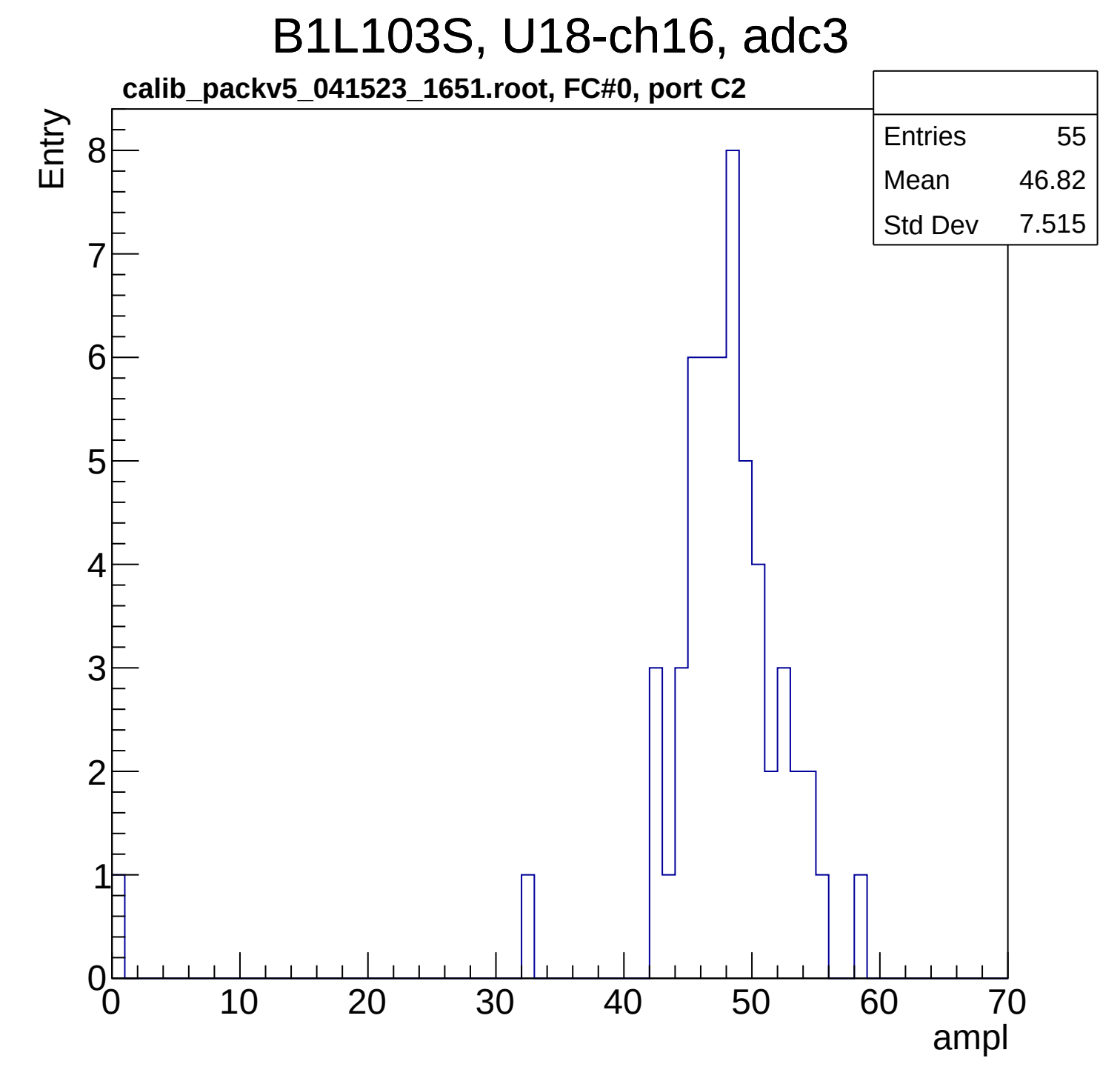
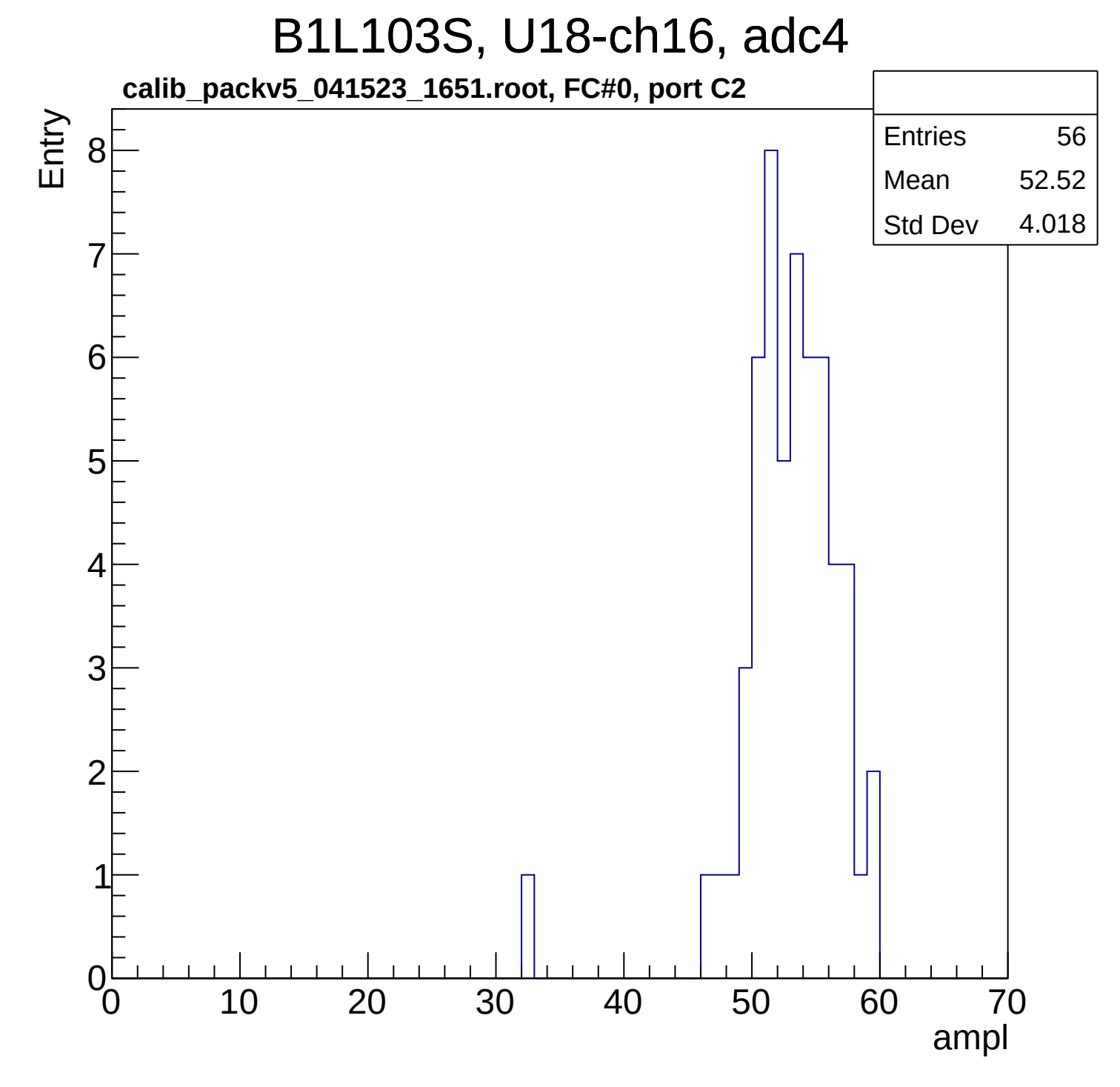
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U18-ch16, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 35.8
Std Dev 14.43
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch16, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 46.82
Std Dev 7.515
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch16, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 52.52
Std Dev 4.018
Entry
ampl
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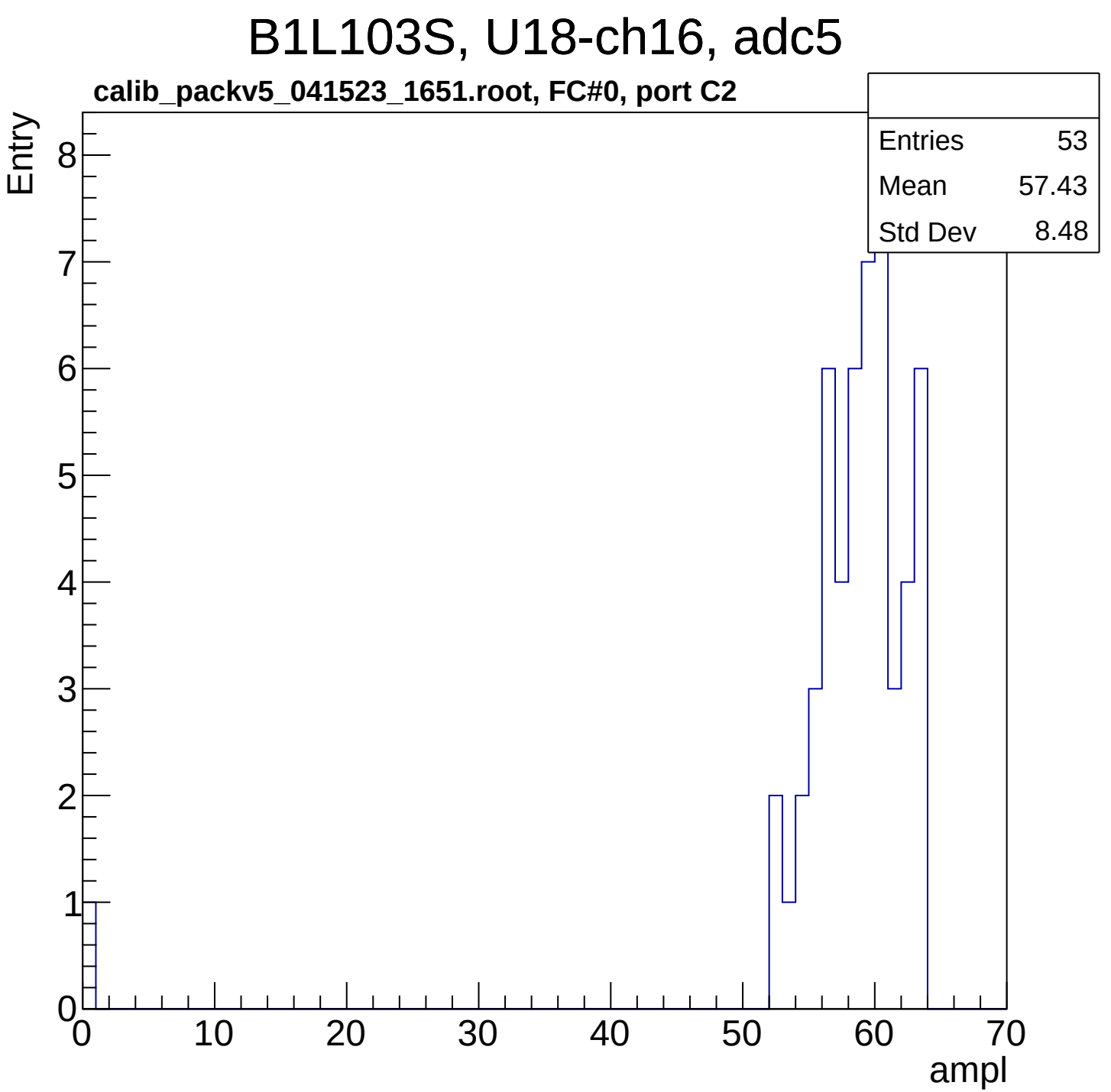
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch16, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 57.43
Std Dev 8.48
Entry
ampl
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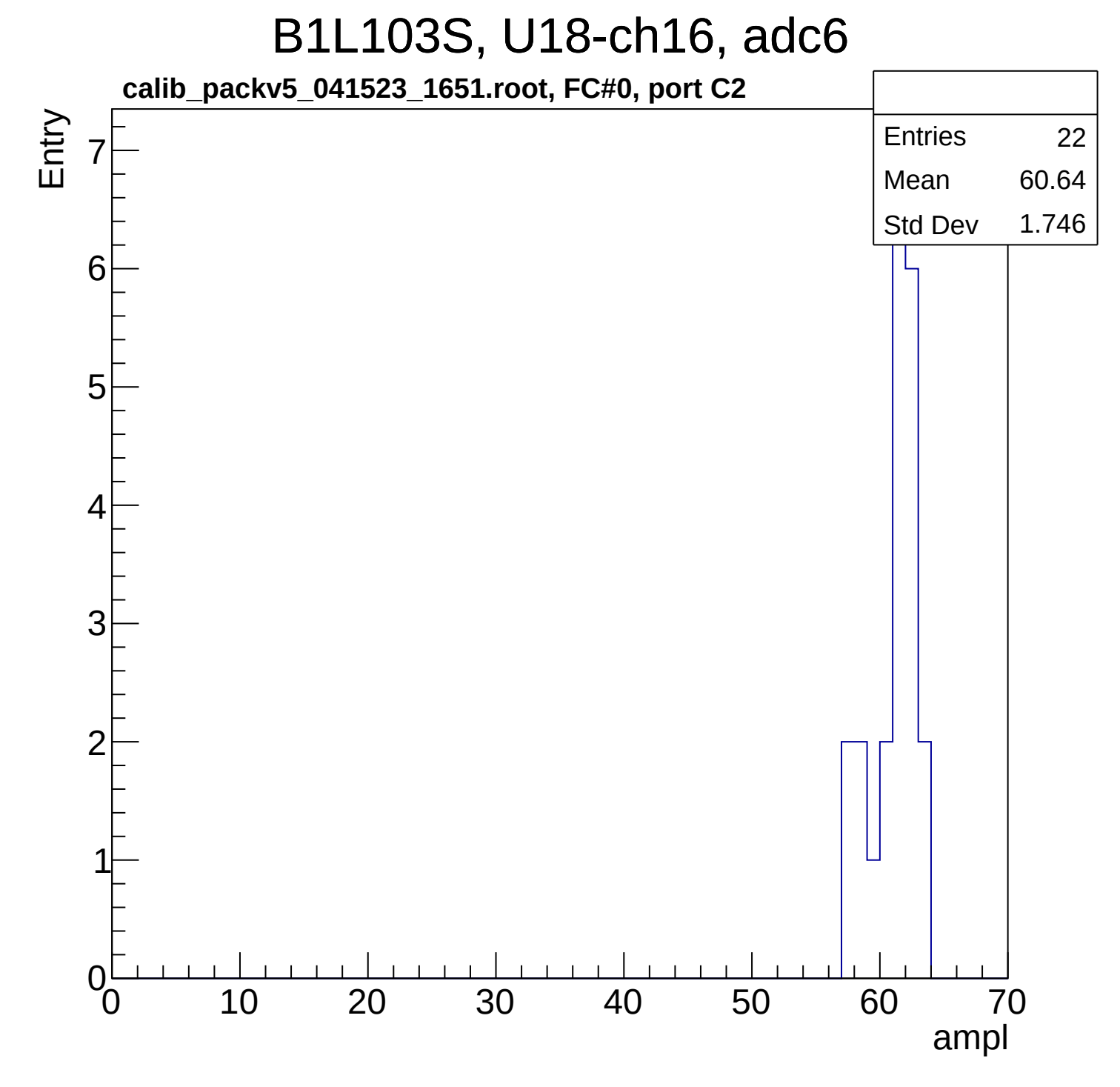
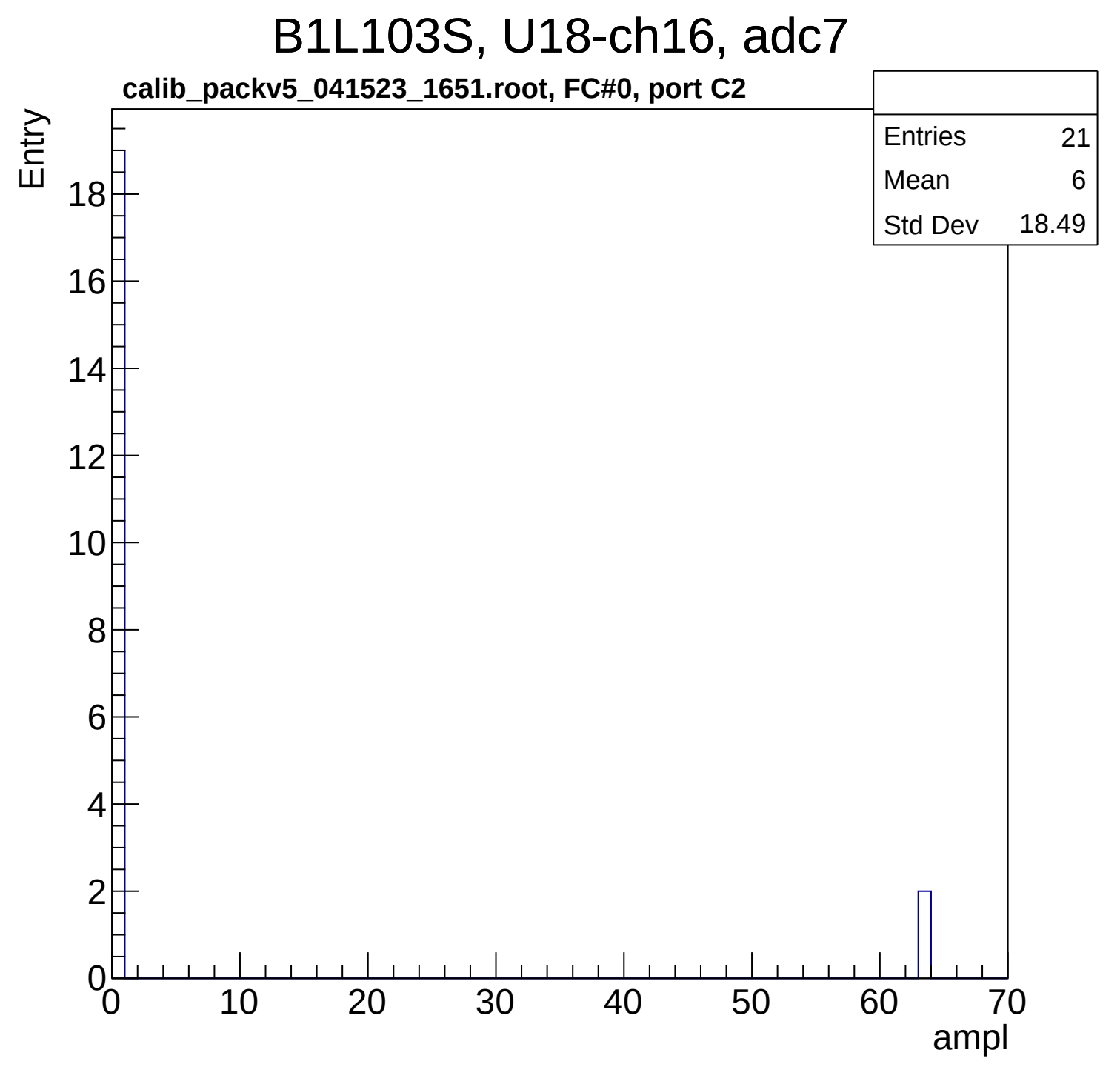
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch16, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 60.64
Std Dev 1.746
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U18-ch16, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 6
Std Dev 18.49
Entry
0
2
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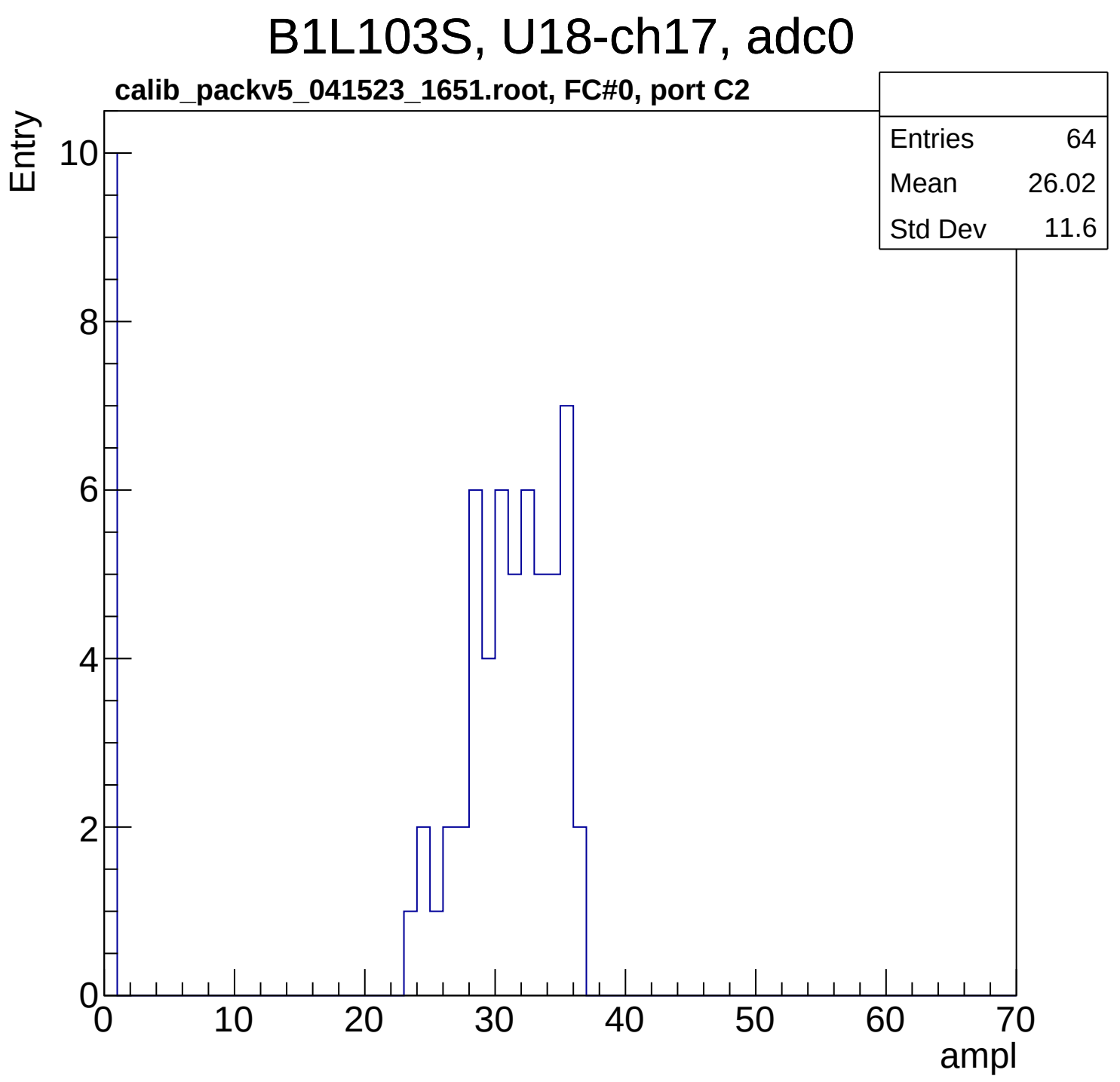
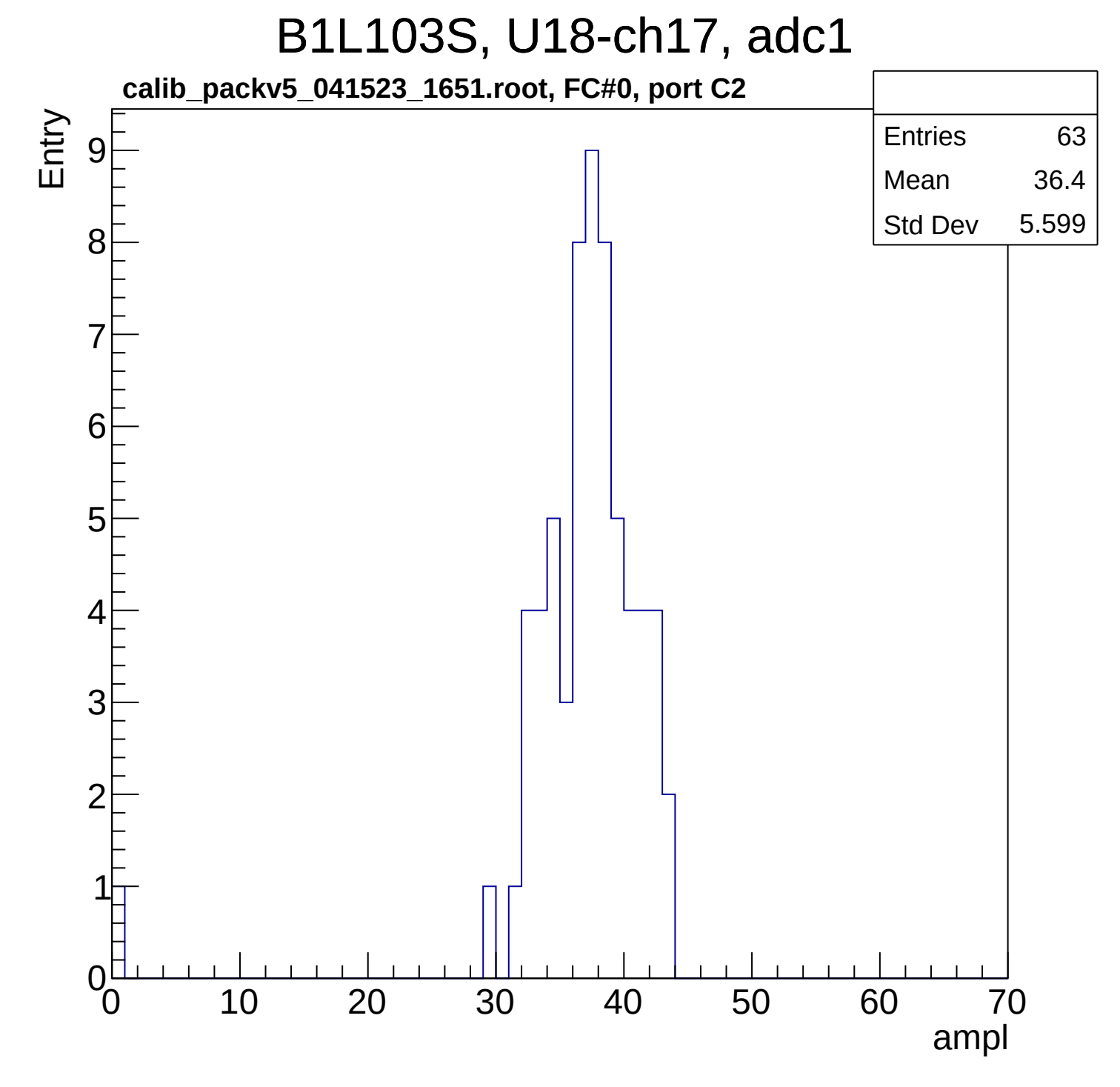
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch17, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 26.02
Std Dev 11.6
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch17, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 36.4
Std Dev 5.599
Entry
ampl
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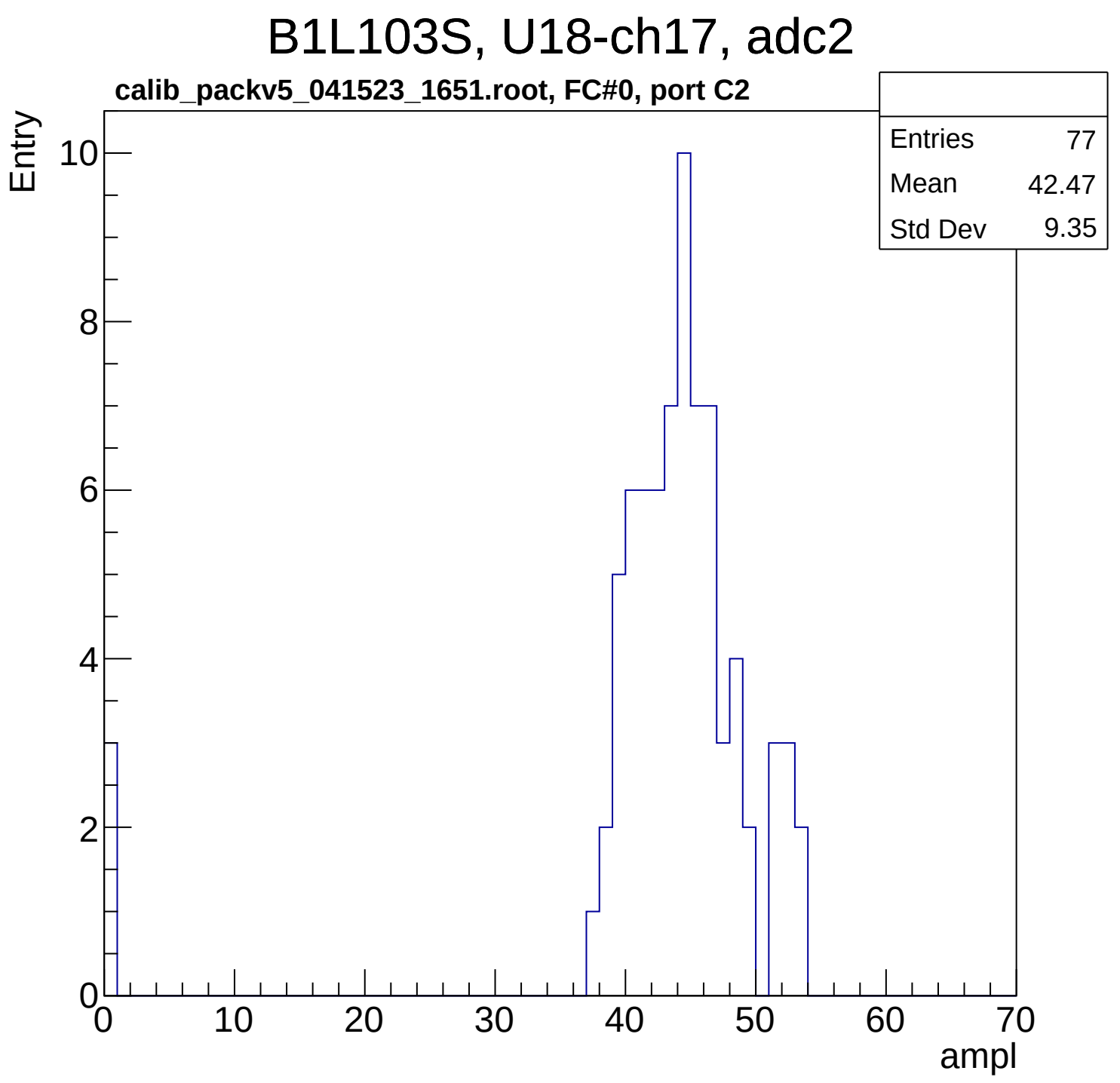
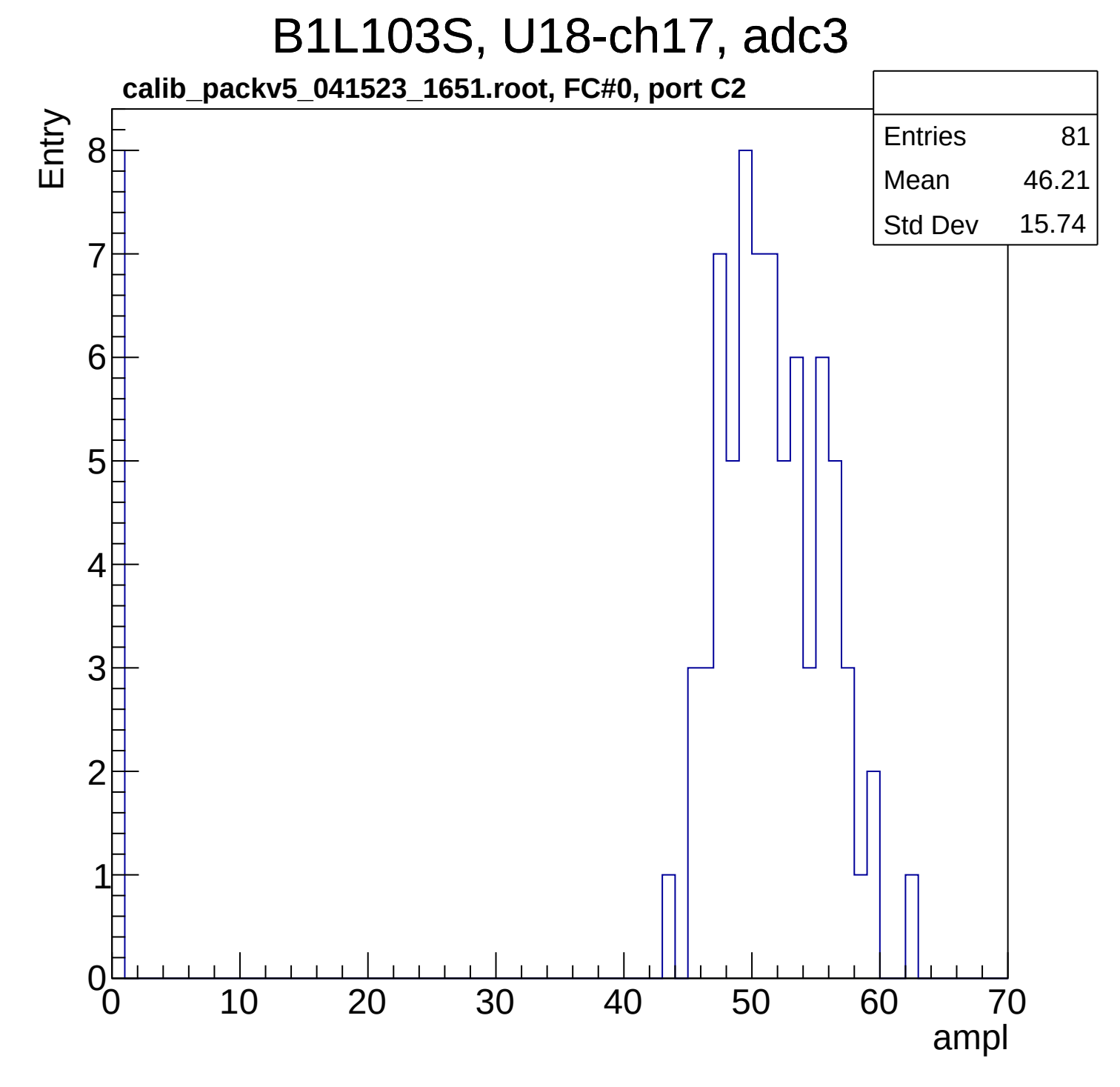
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U18-ch17, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 42.47
Std Dev 9.35
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U18-ch17, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 46.21
Std Dev 15.74
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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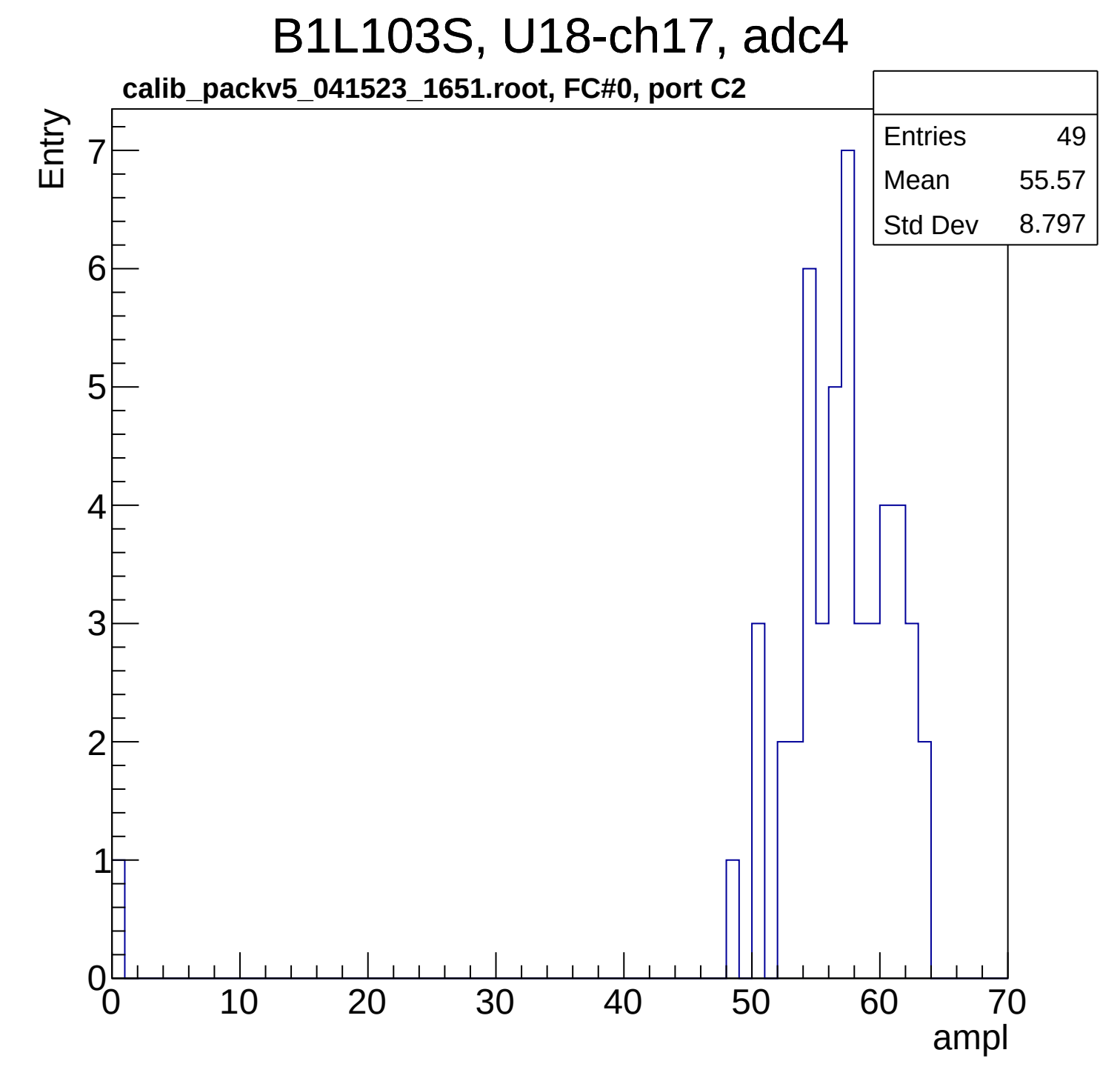
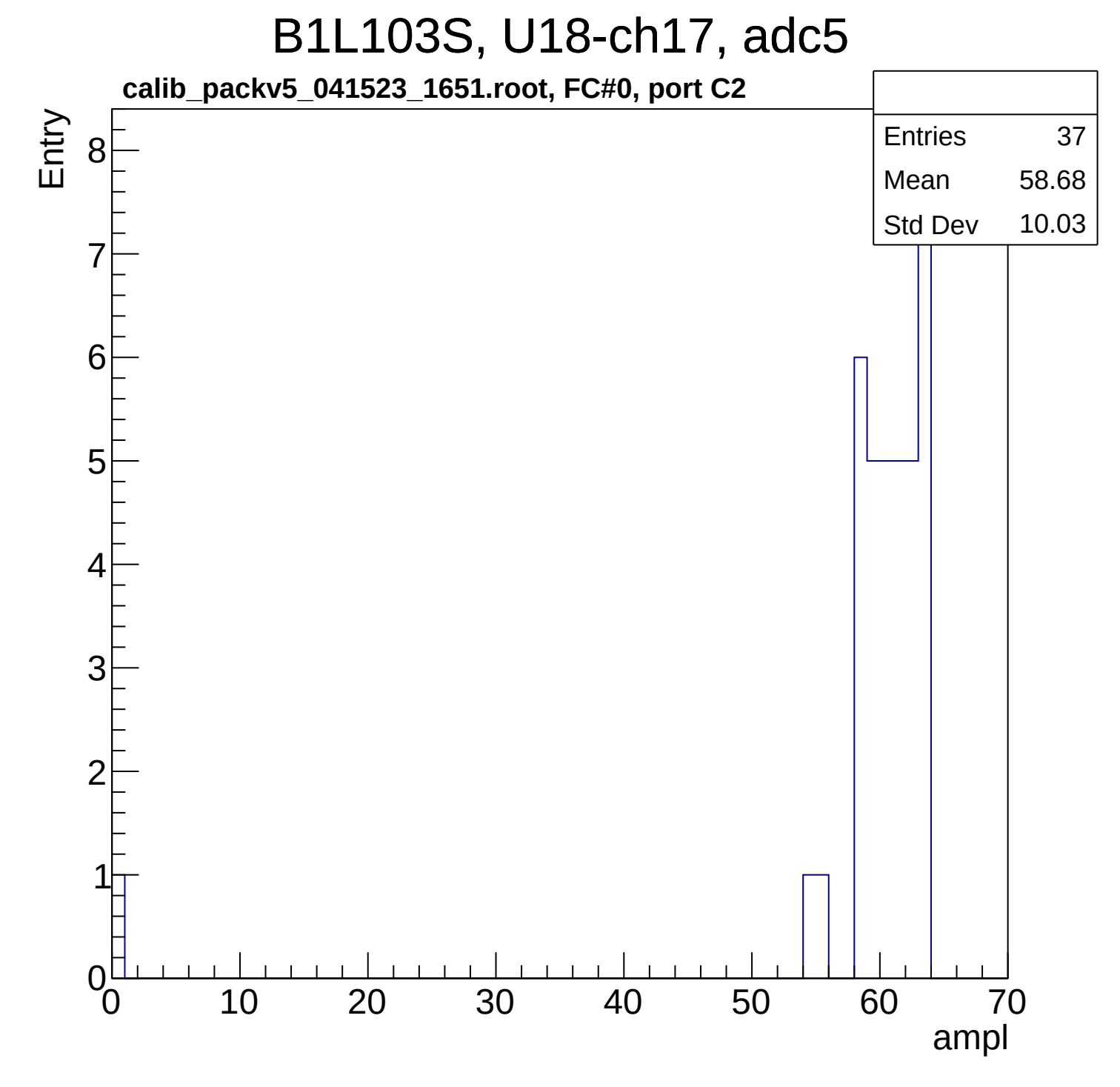

B1L103S, U18-ch17, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 55.57
Std Dev 8.797
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U18-ch17, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 37
Mean 58.68
Std Dev 10.03
Entry
ampl
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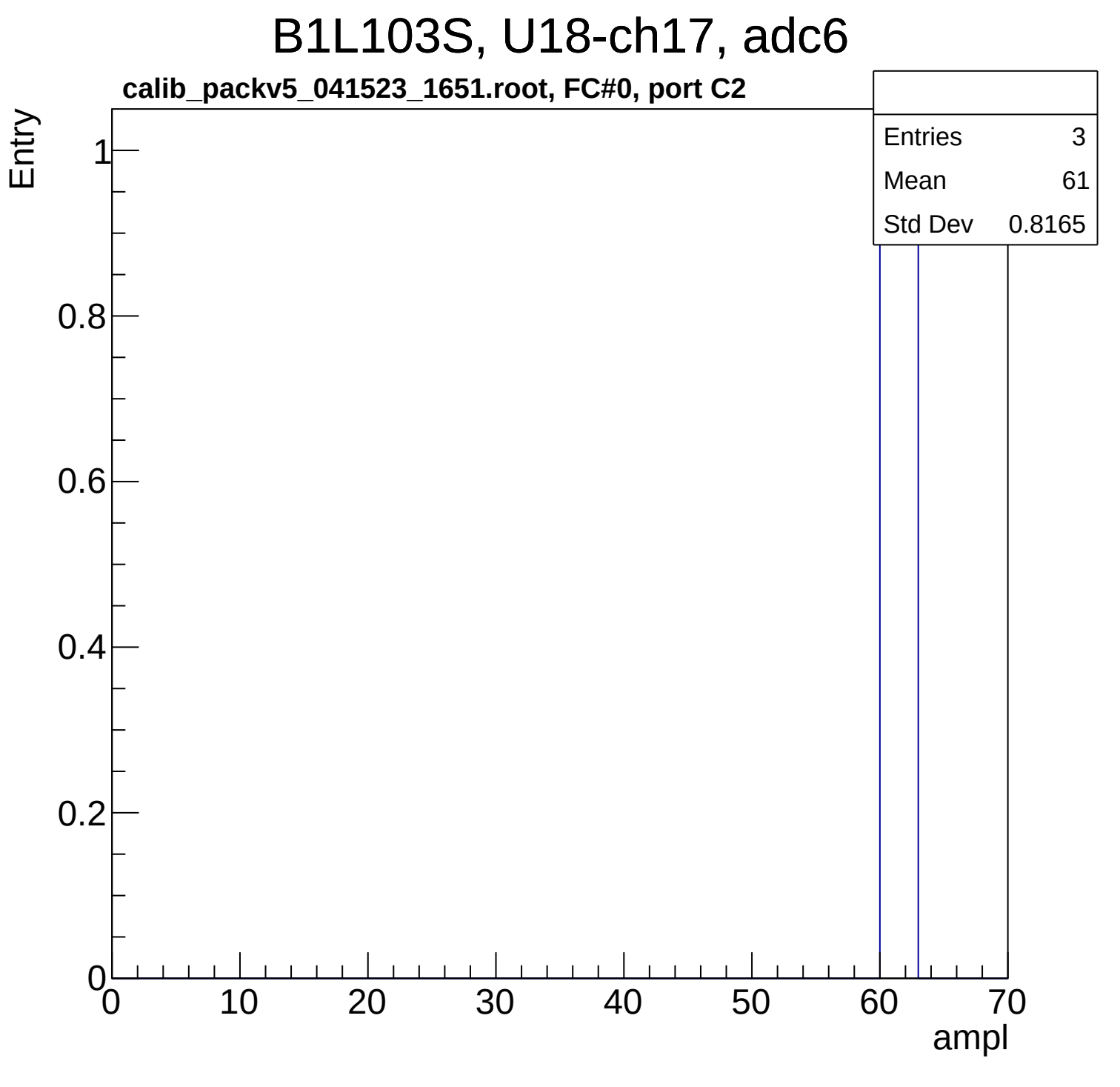
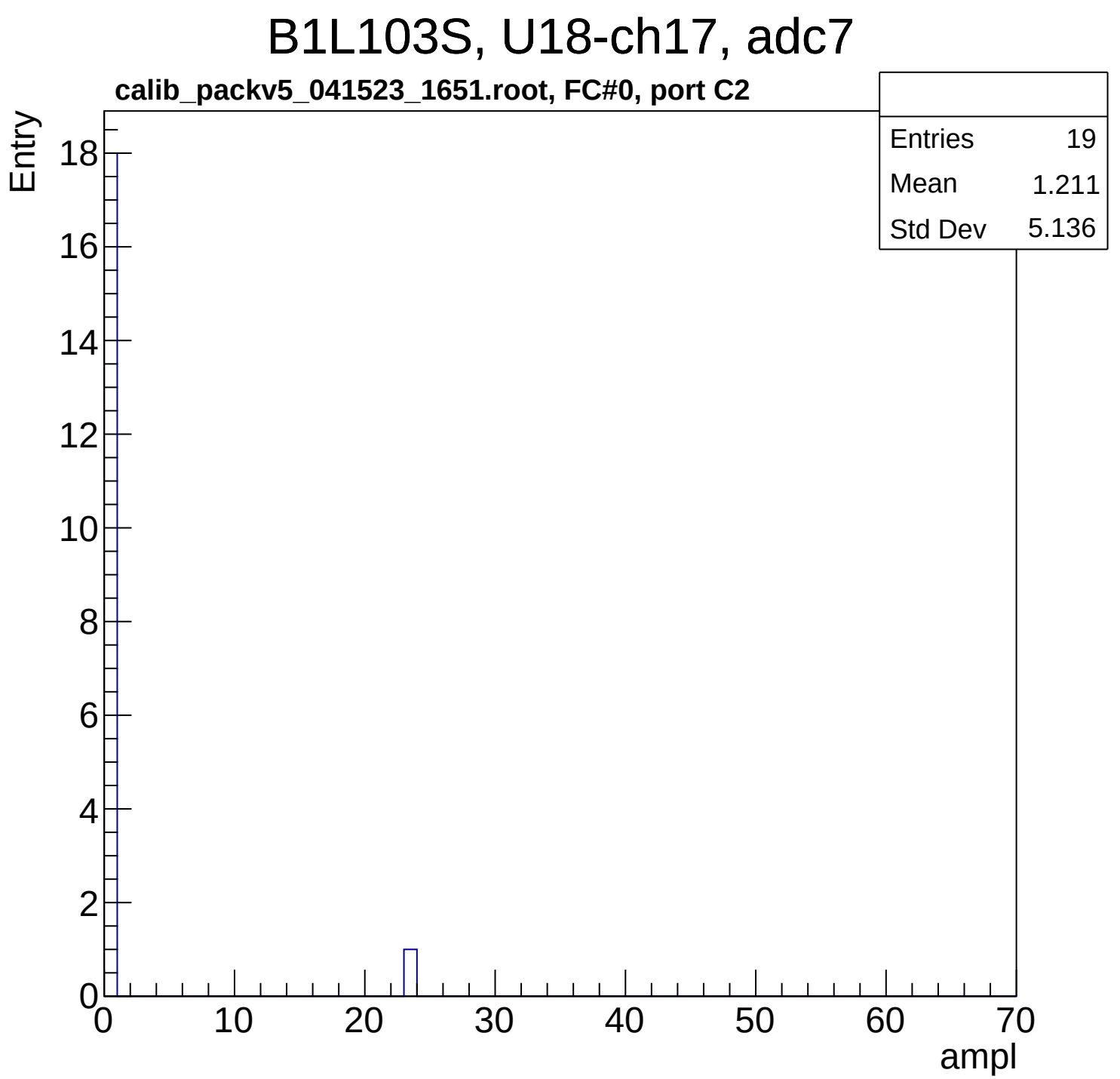
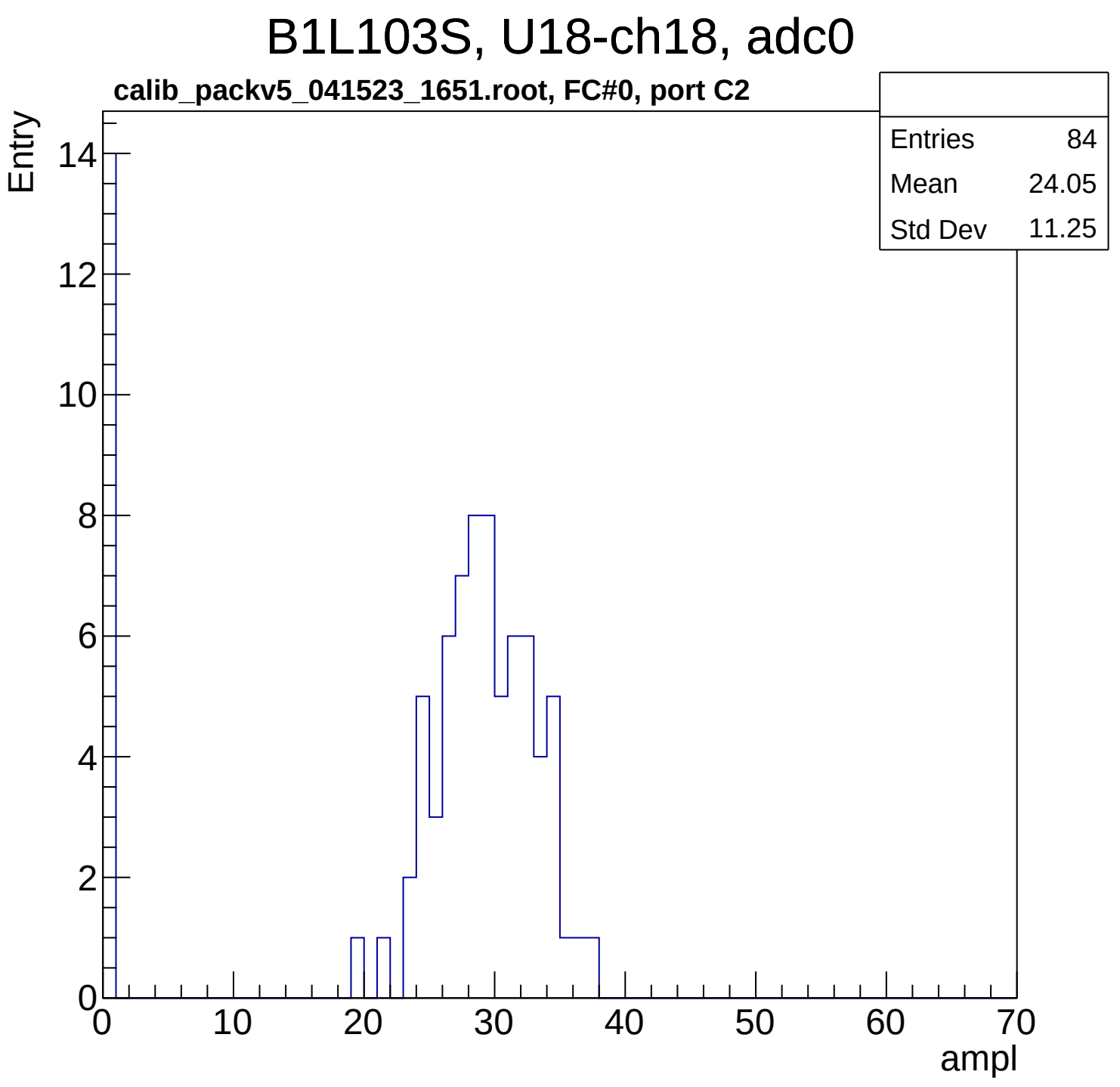
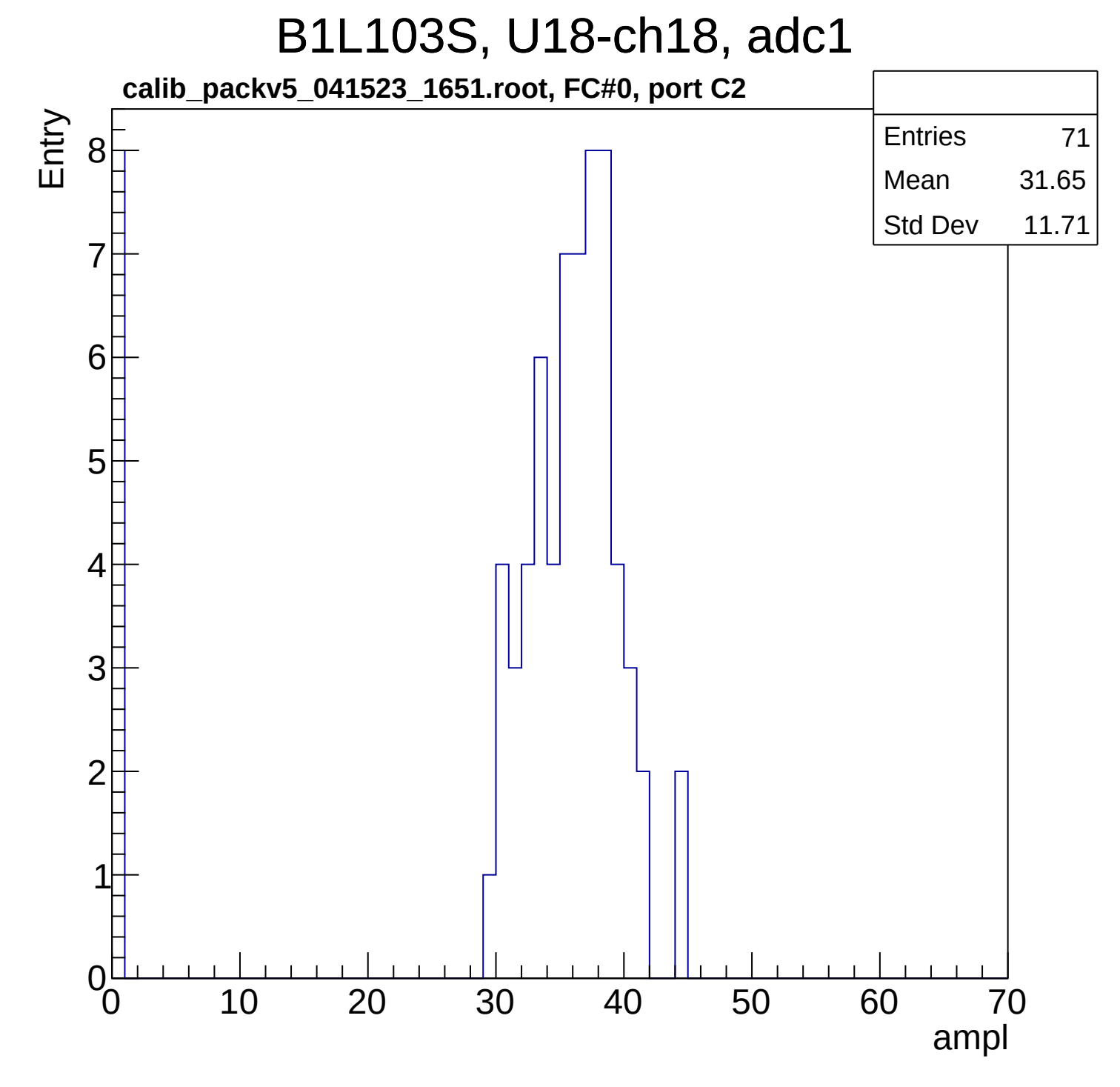
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch17, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 3
Mean 61
Std Dev 0.8165
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch17, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.211
Std Dev 5.136
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70


B1L103S, U18-ch18, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 24.05
Std Dev 11.25
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch18, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 31.65
Std Dev 11.71
Entry
ampl
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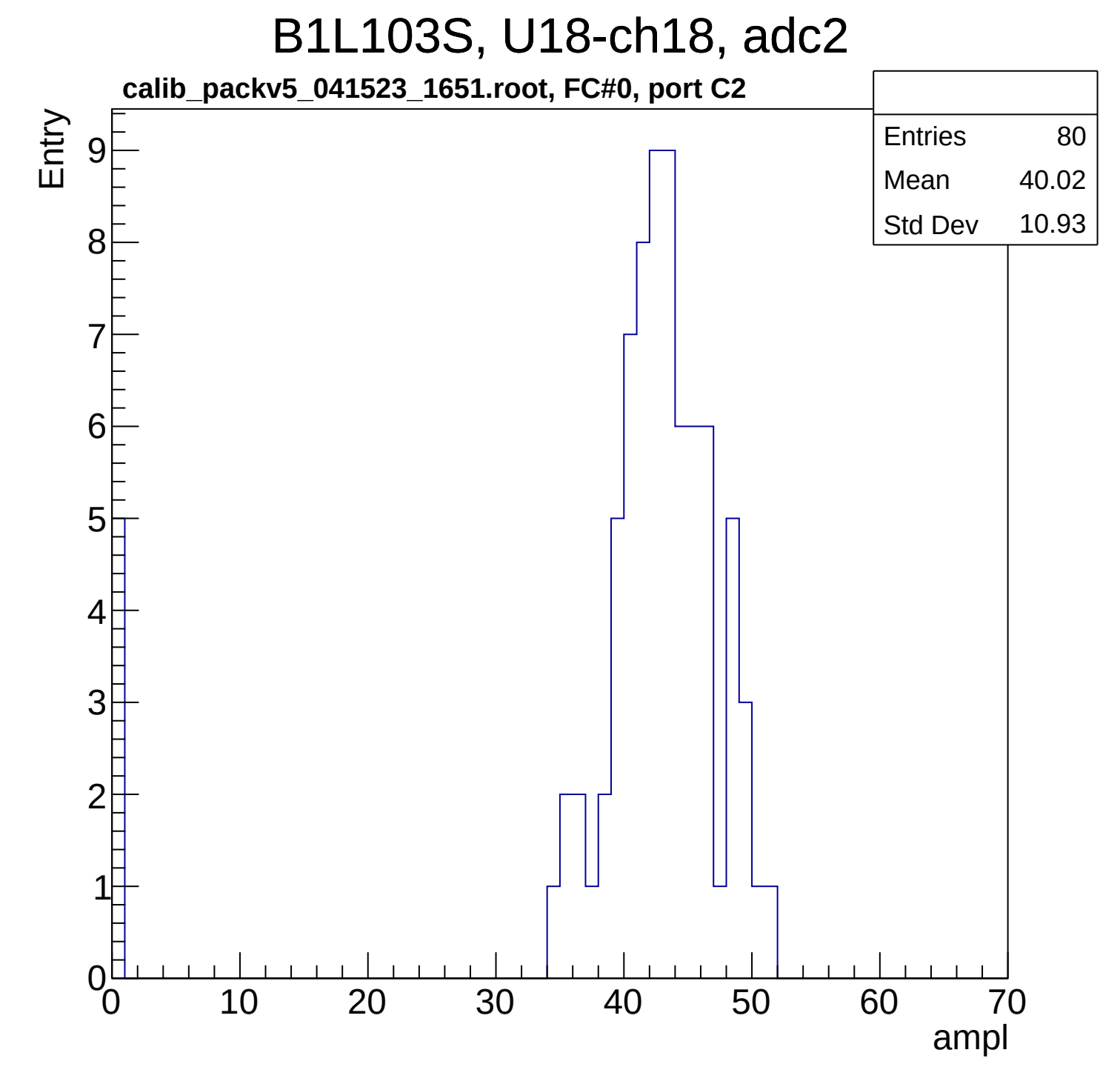
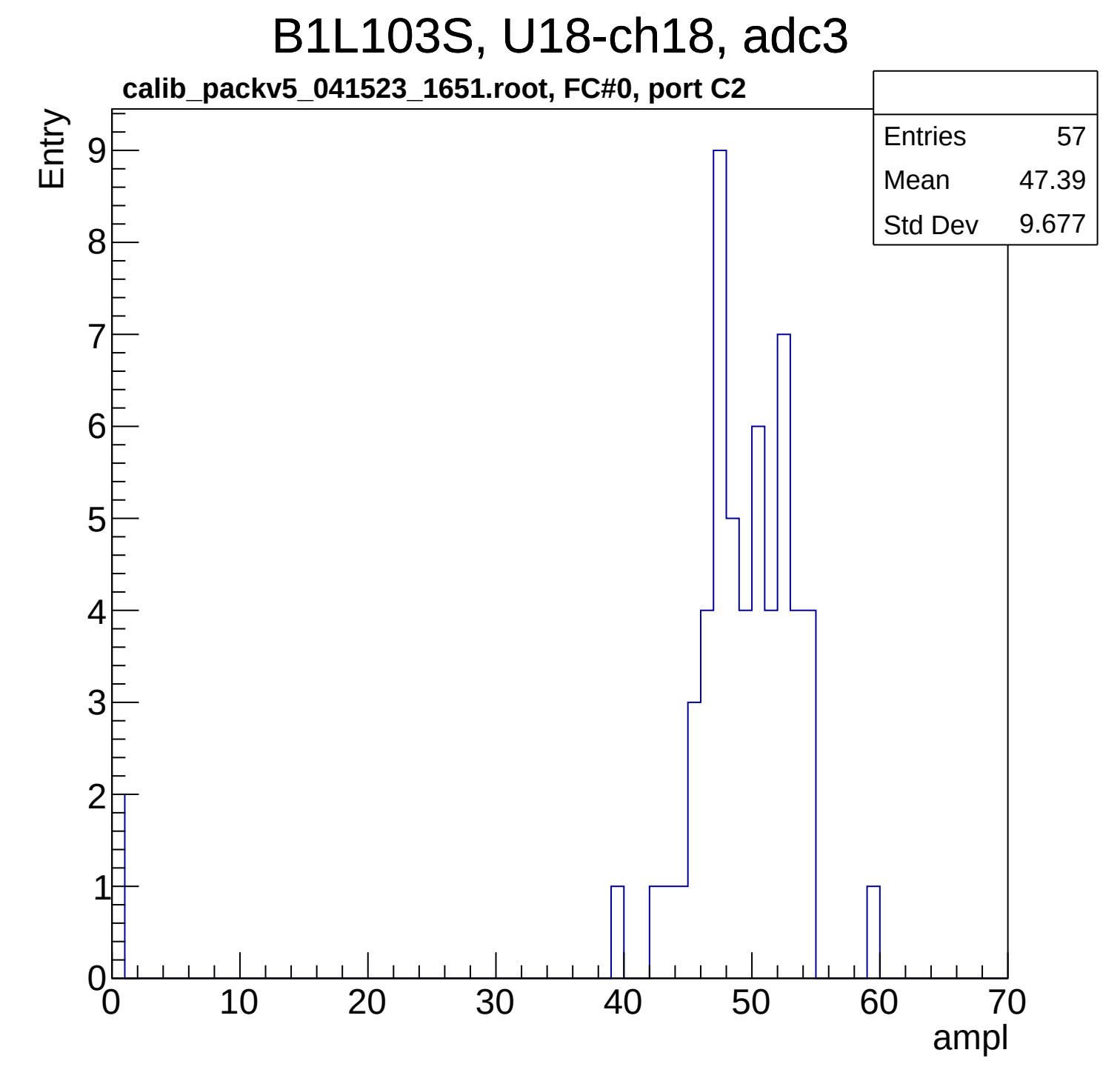
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch18, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 40.02
Std Dev 10.93
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U18-ch18, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 47.39
Std Dev 9.677
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
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50
60
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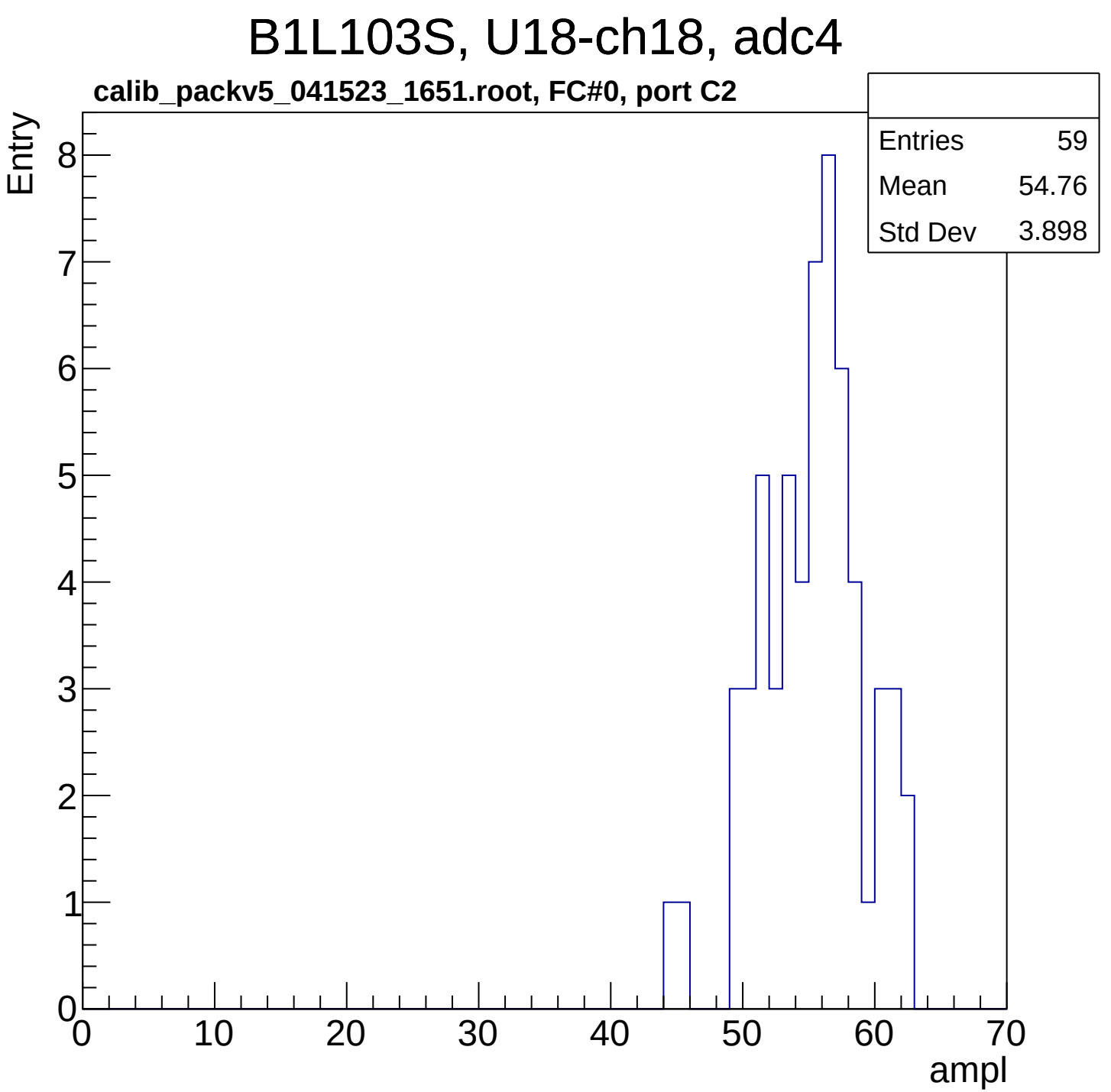
B1L103S, U18-ch18, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 54.76
Std Dev 3.898
Entry
ampl
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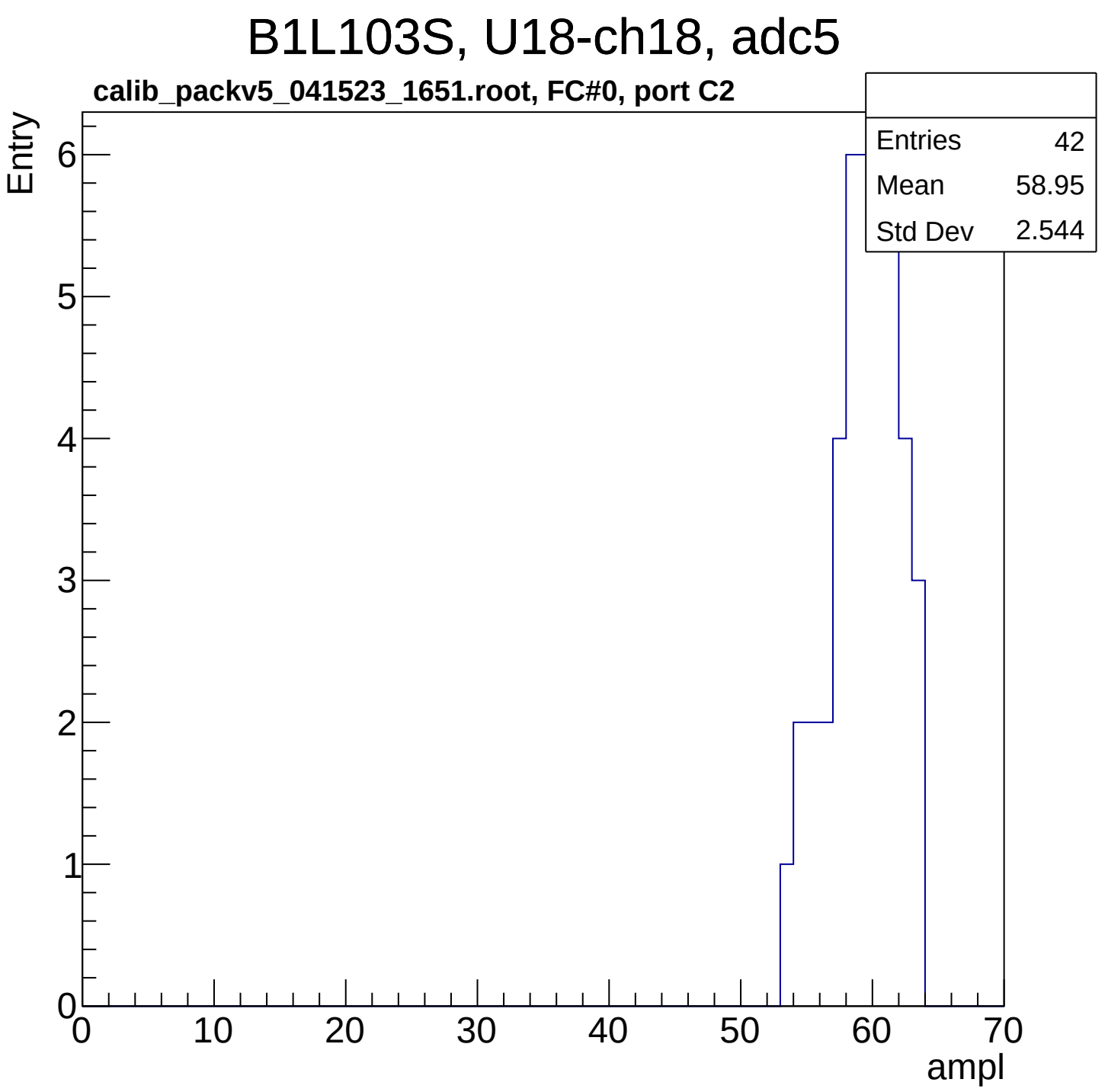
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch18, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 42
Mean 58.95
Std Dev 2.544
Entry
ampl
0
1
2
3
4
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6
0
10
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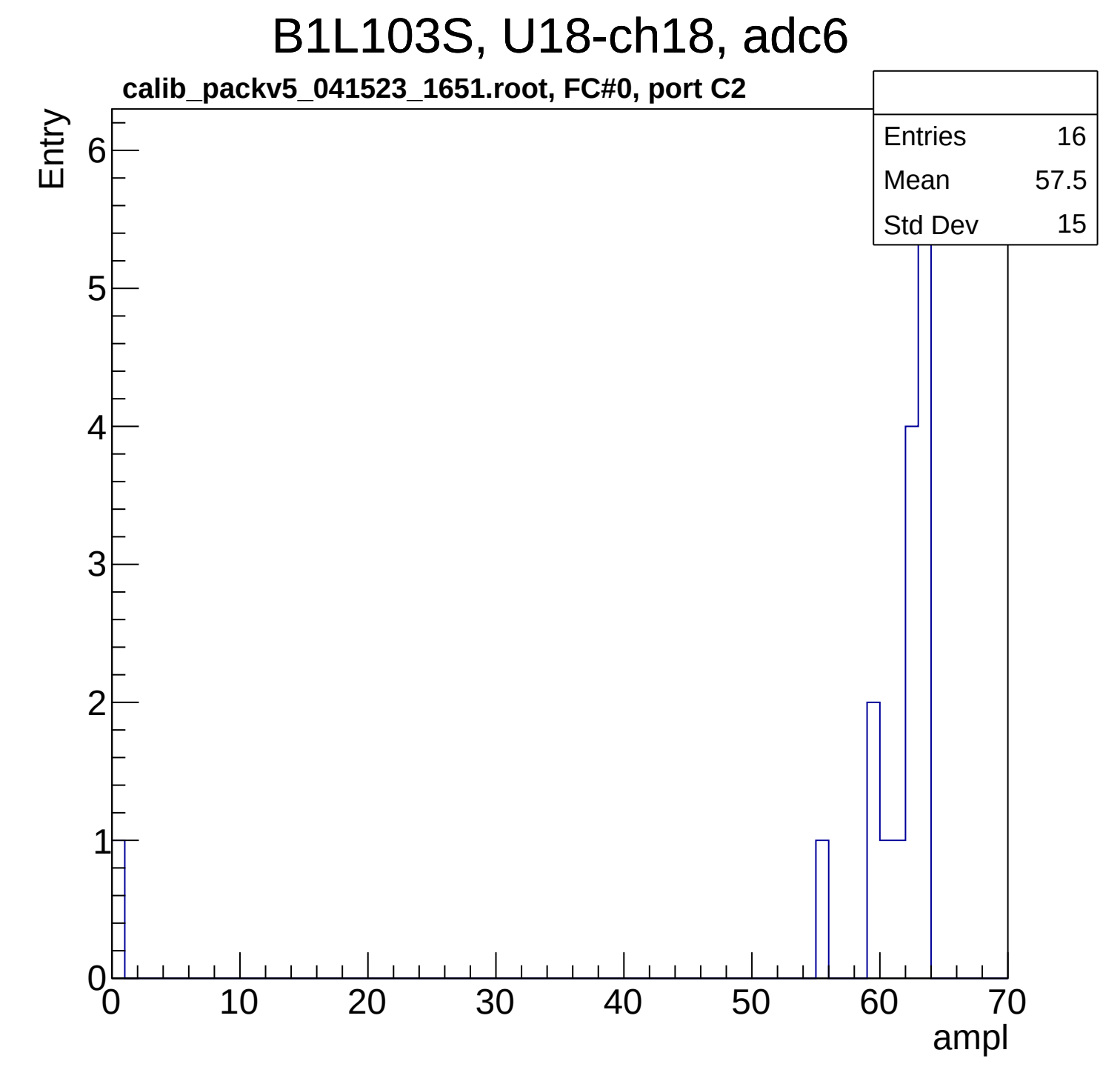
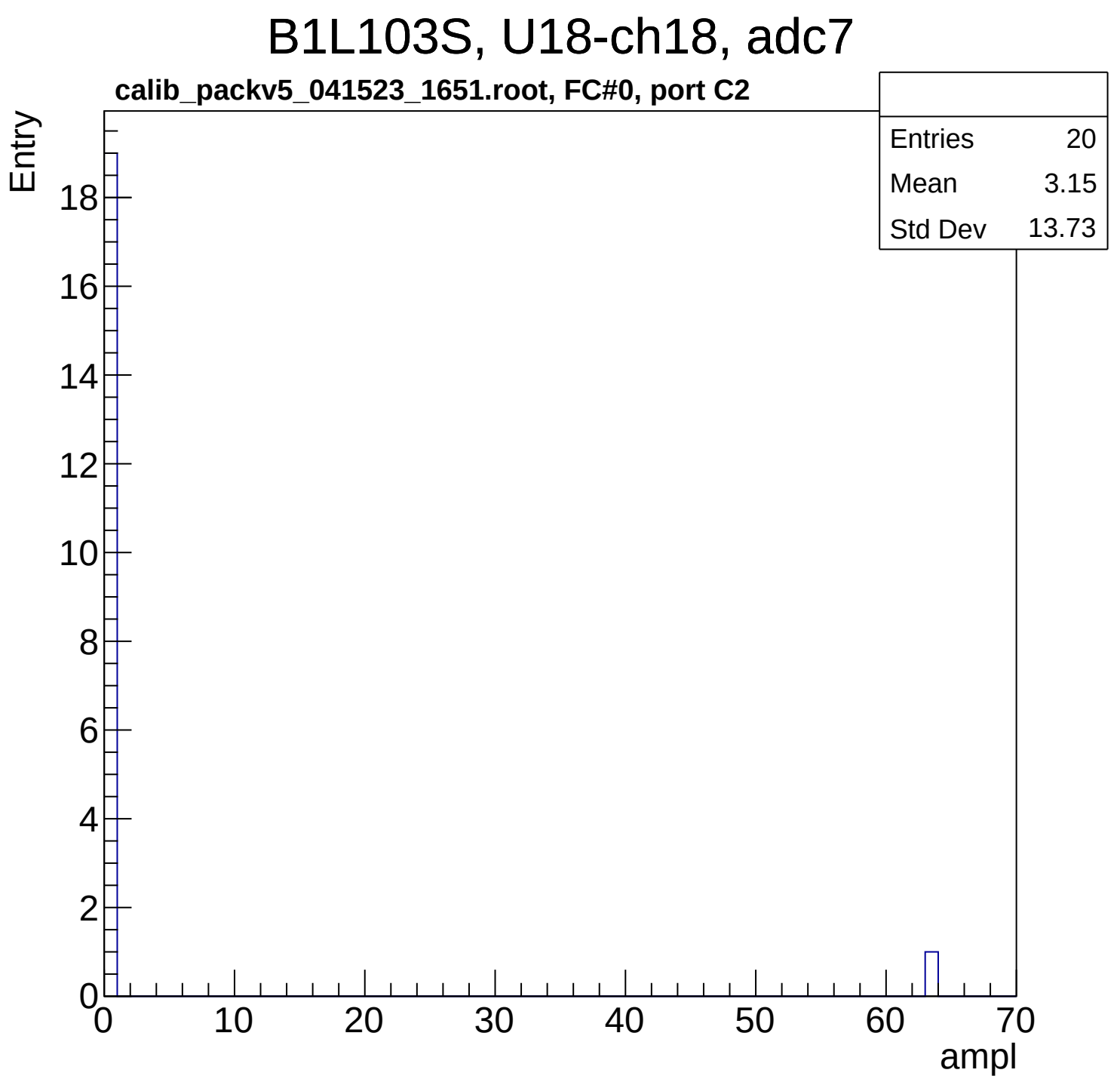
30
40
50
60
70


B1L103S, U18-ch18, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 16
Mean 57.5
Std Dev 15
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U18-ch18, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
0
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4
6
8
10
12
14
16
18
0
10
20
30
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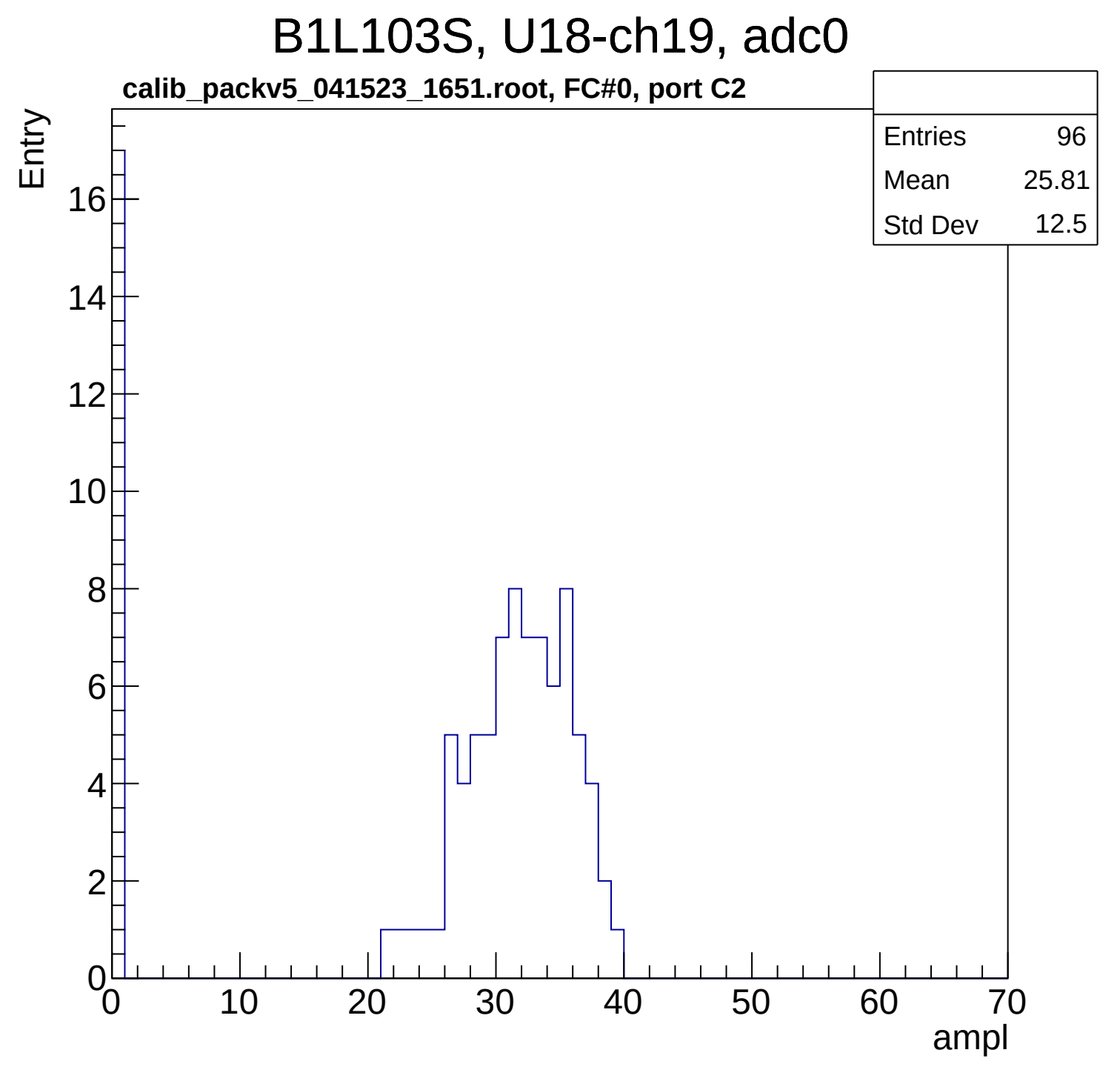
50
60
70
ampl


B1L103S, U18-ch19, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 96
Mean 25.81
Std Dev 12.5
Entry
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4
6
8
10
12
14
16
0
10
20
30
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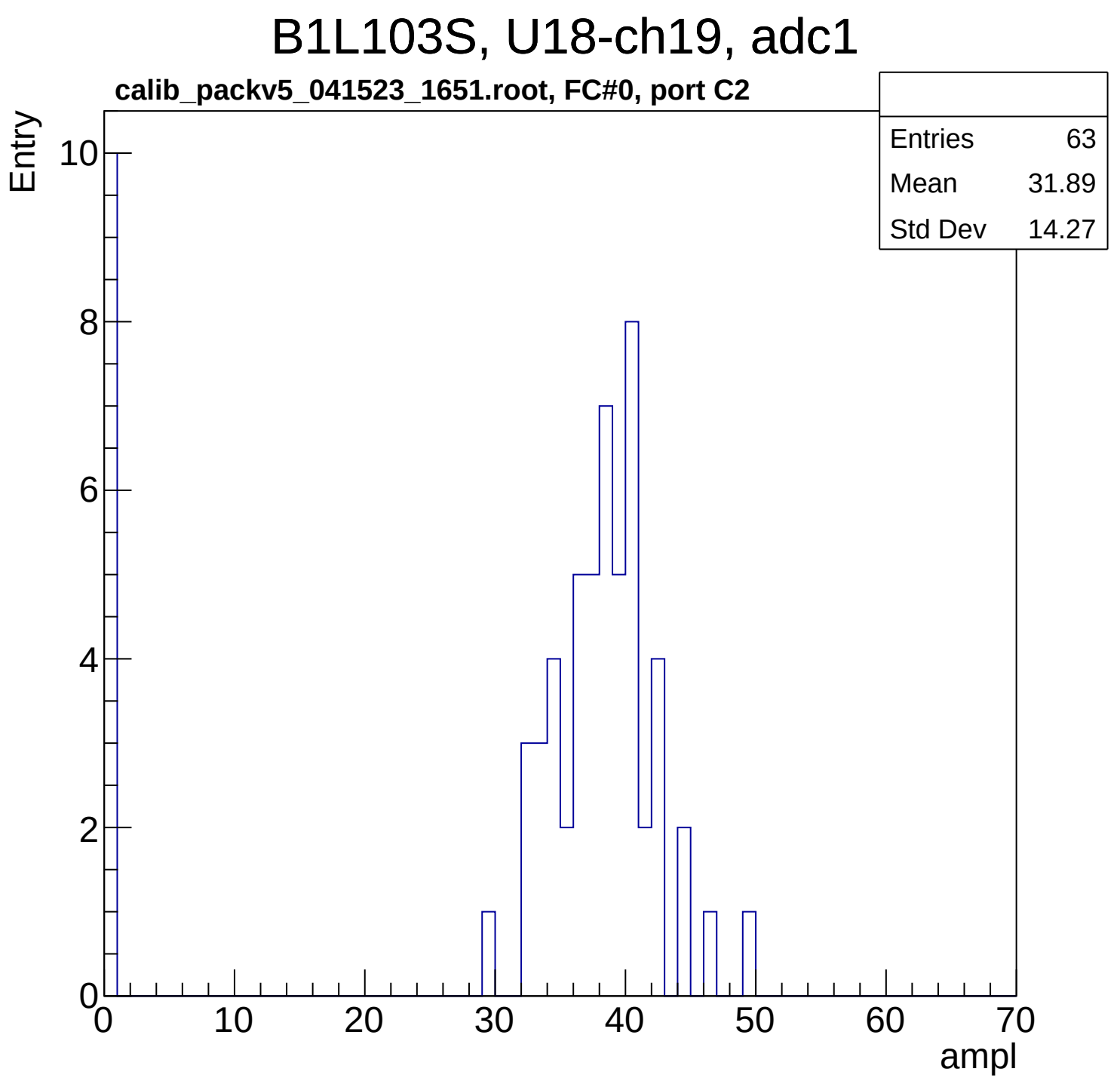
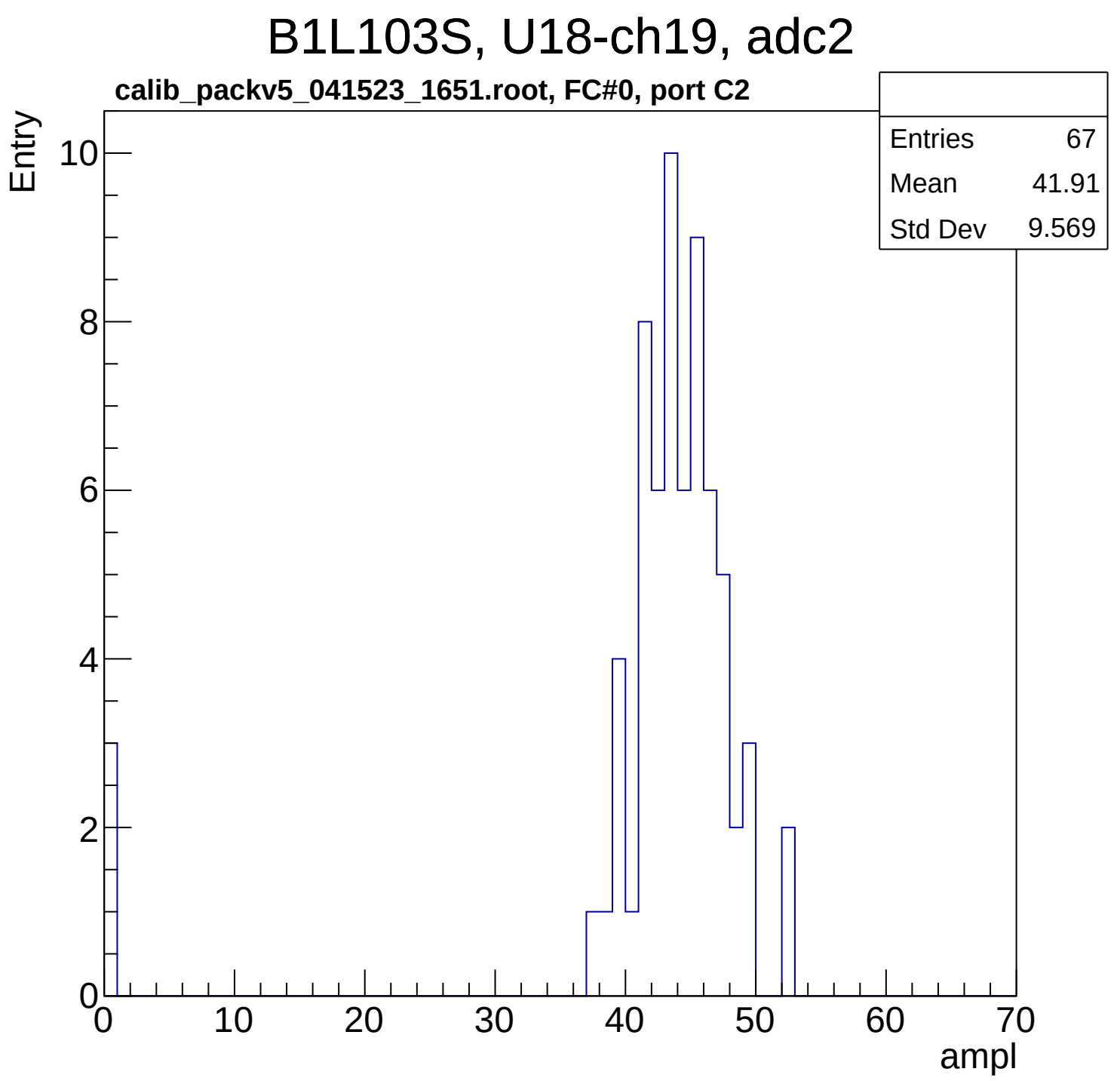
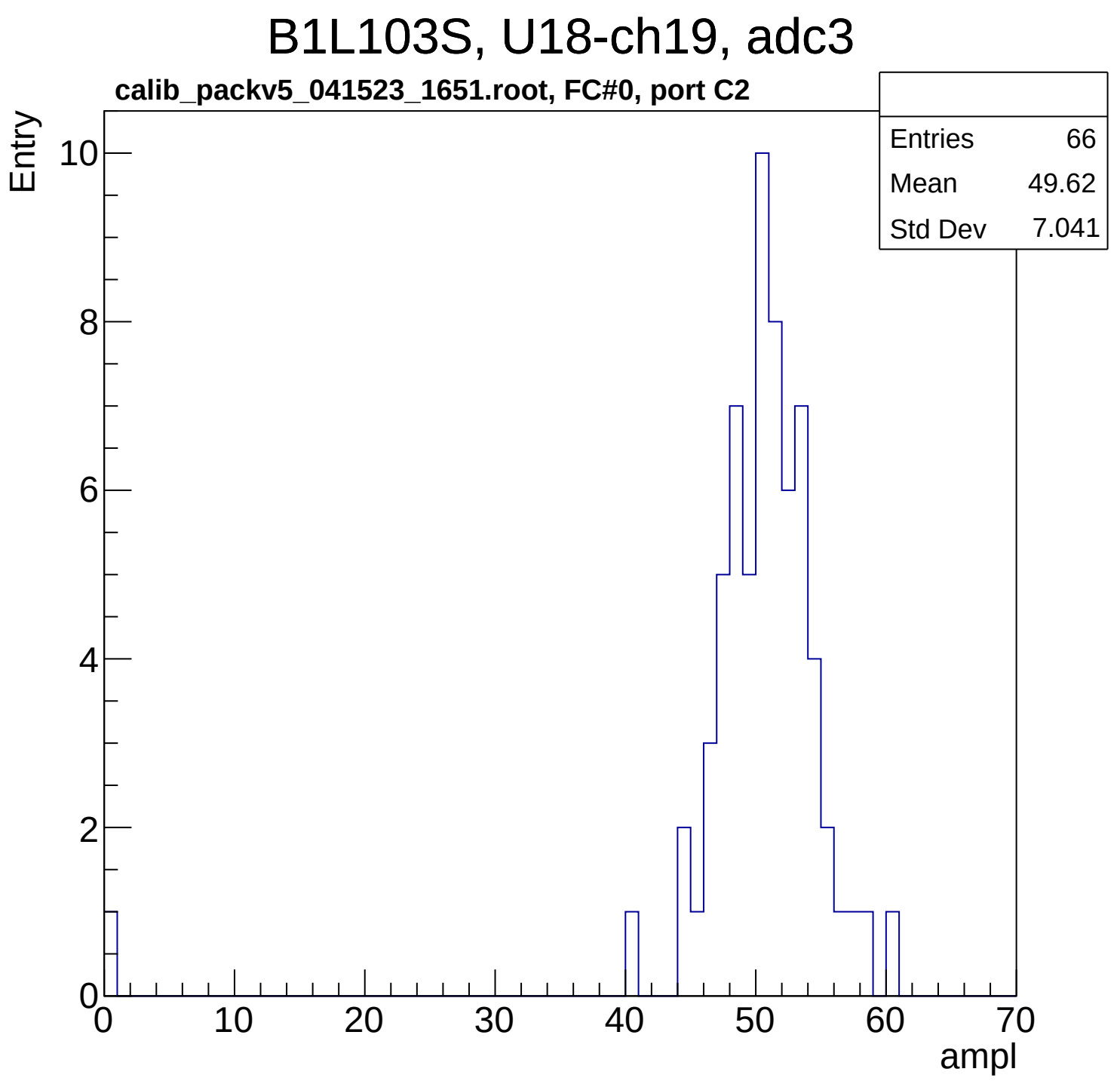
50
60
70
ampl


B1L103S, U18-ch19, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 31.89
Std Dev 14.27
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U18-ch19, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 41.91
Std Dev 9.569
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U18-ch19, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 49.62
Std Dev 7.041
Entry
ampl
0
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4
6
8
10
0
10
20
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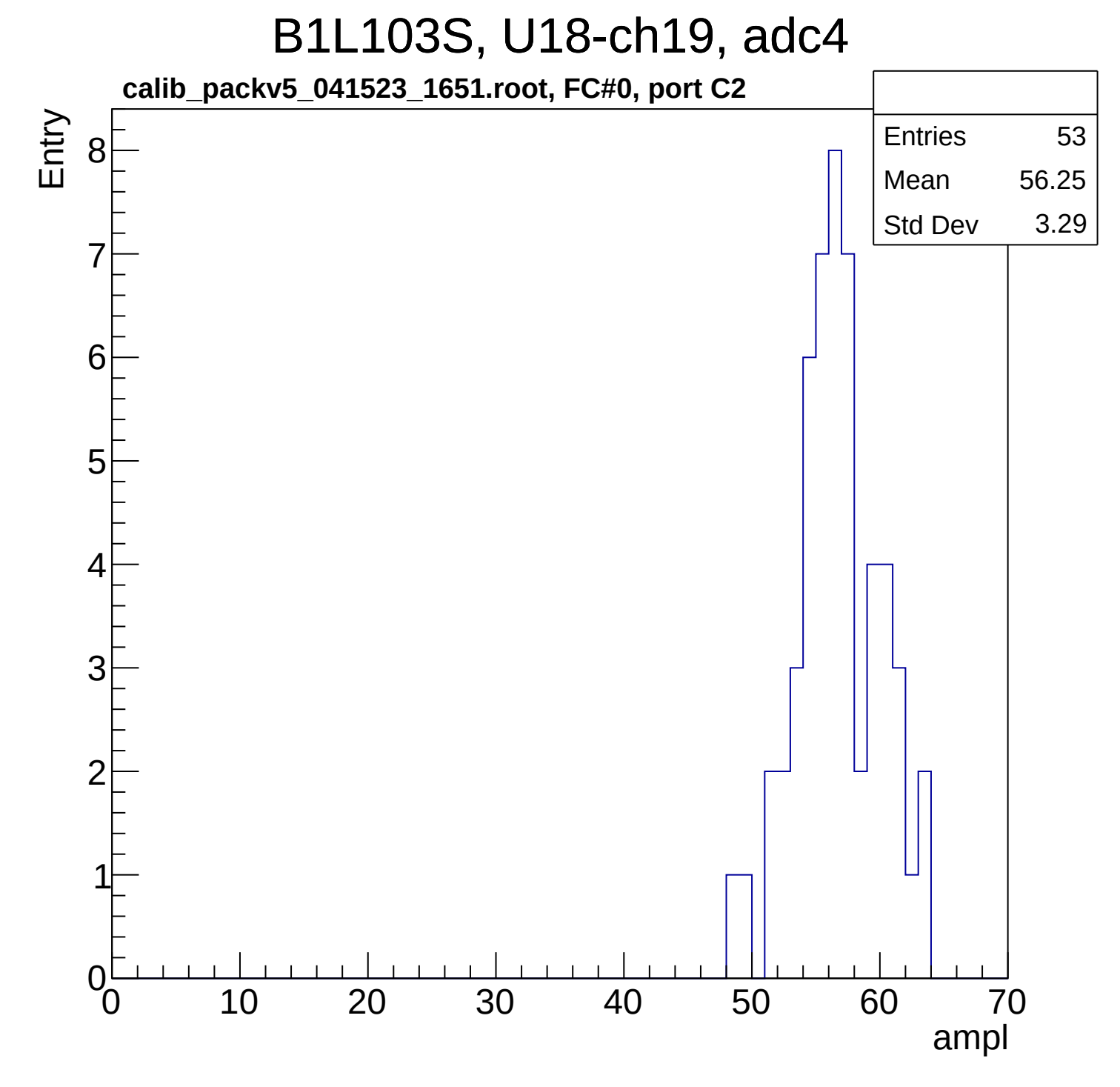
40
50
60
70


B1L103S, U18-ch19, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 56.25
Std Dev 3.29
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
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60
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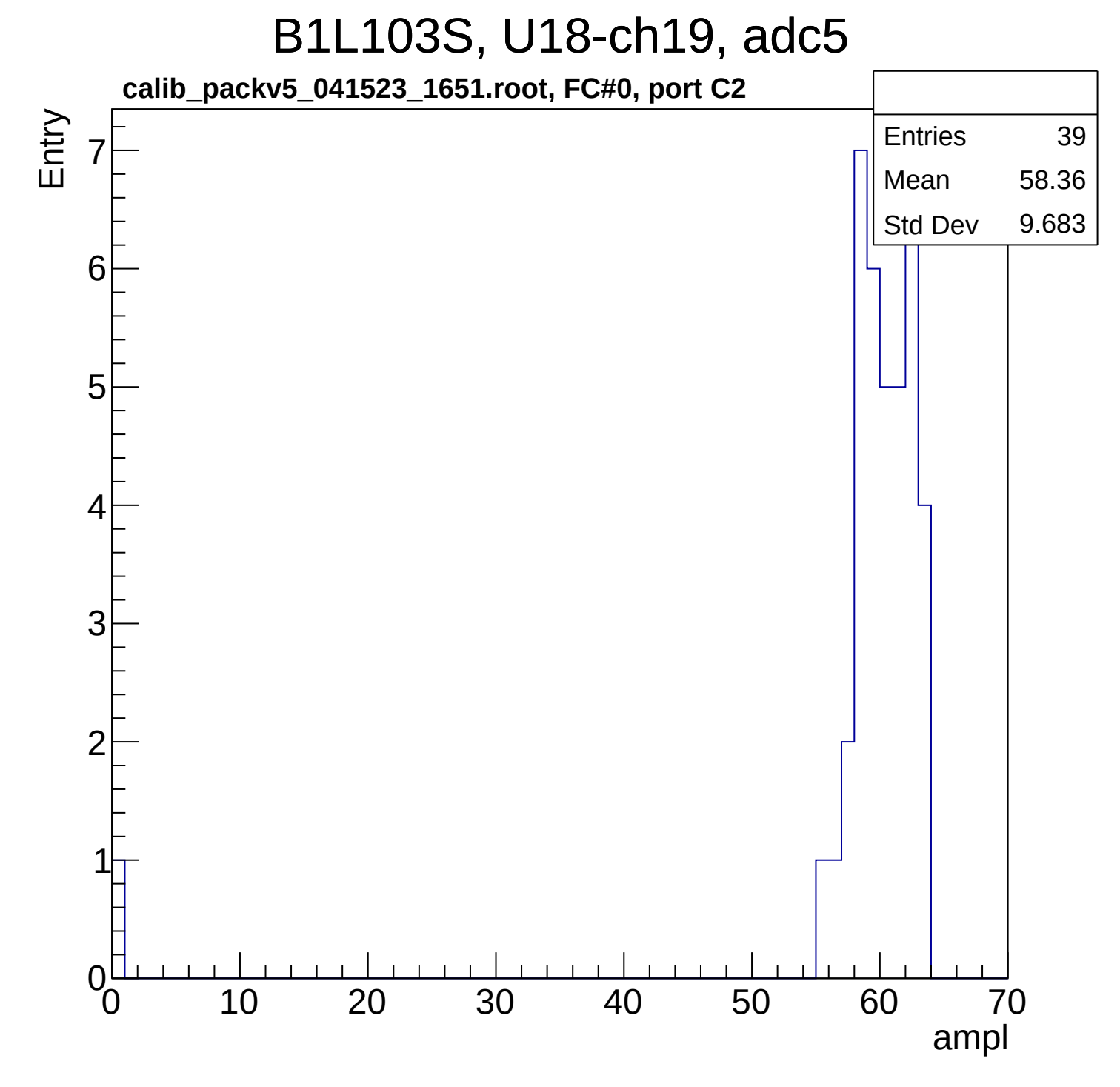
B1L103S, U18-ch19, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 39
Mean 58.36
Std Dev 9.683
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
30
40
50
60
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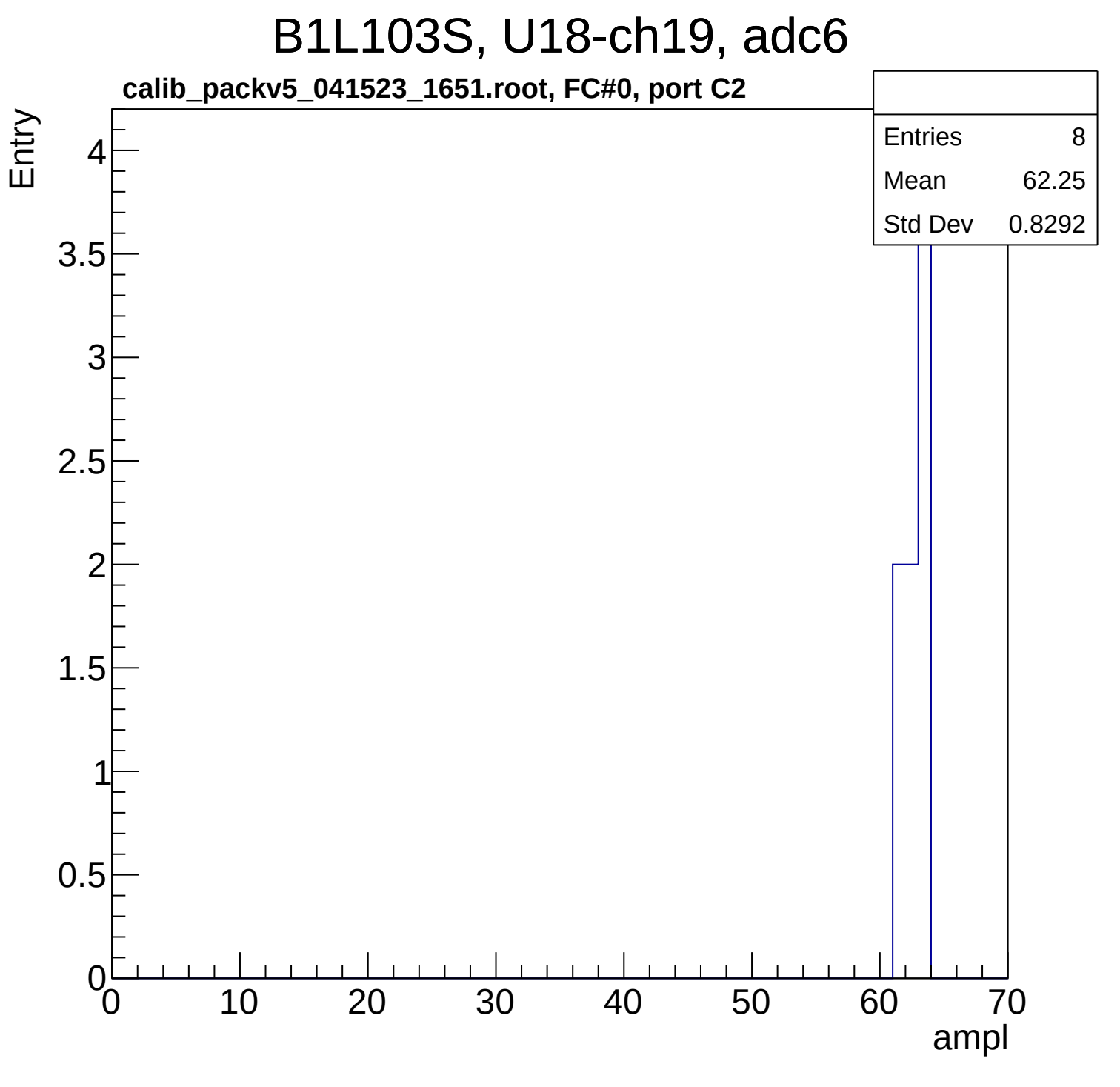
B1L103S, U18-ch19, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 62.25
Std Dev 0.8292
Entry
ampl
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0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
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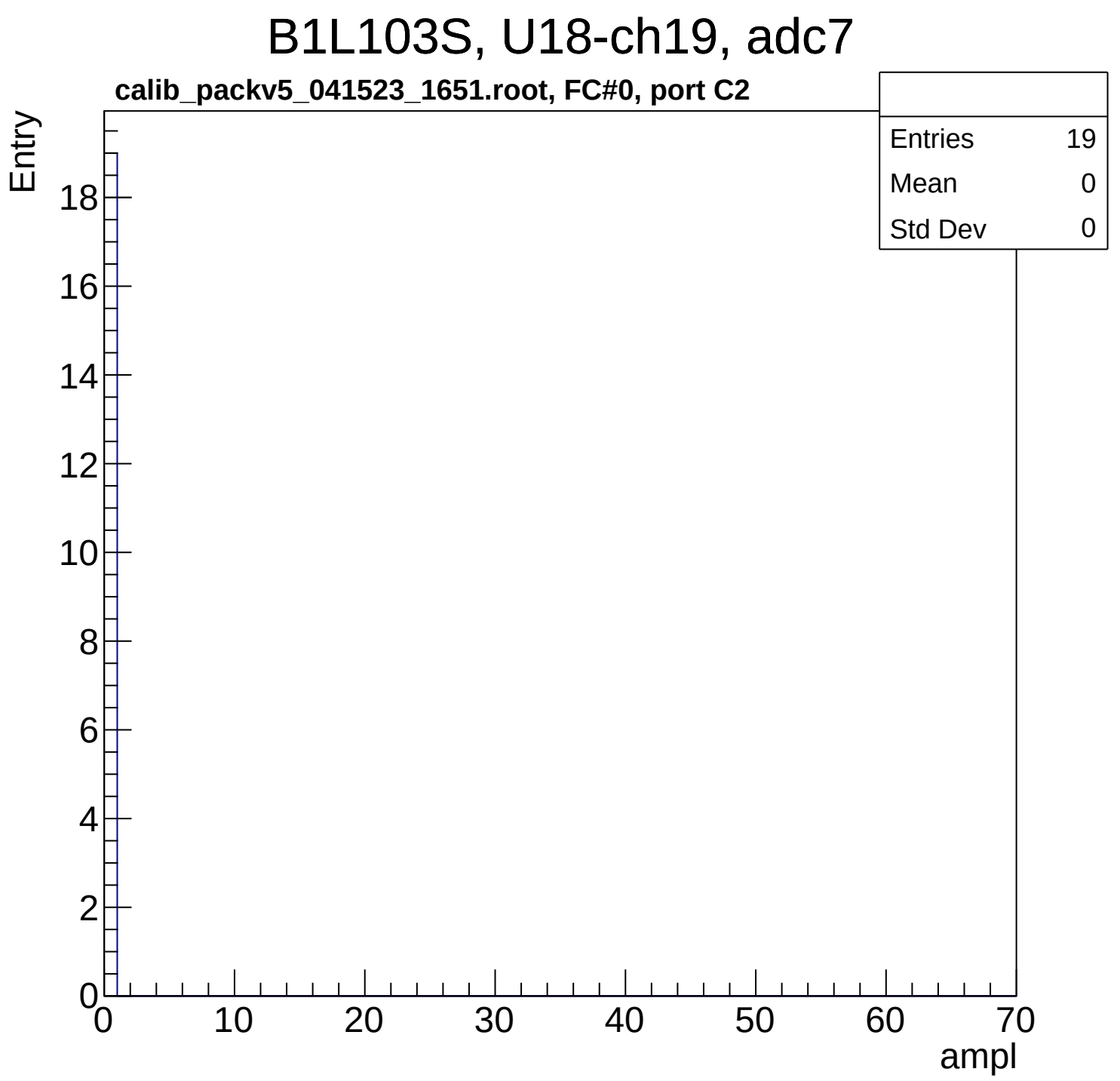
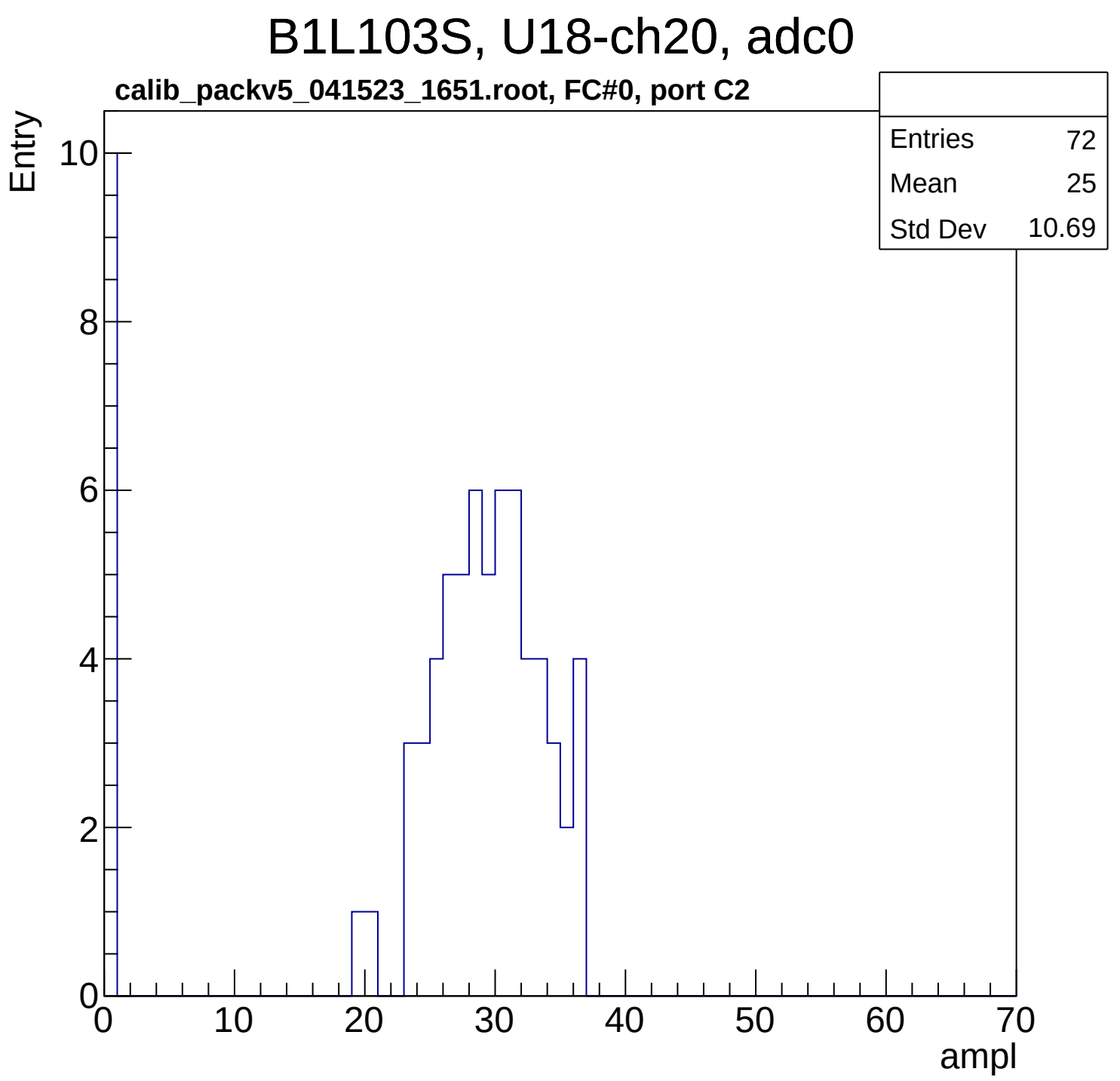
40
50
60
70


B1L103S, U18-ch19, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch20, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 25
Std Dev 10.69
Entry
0
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4
6
8
10
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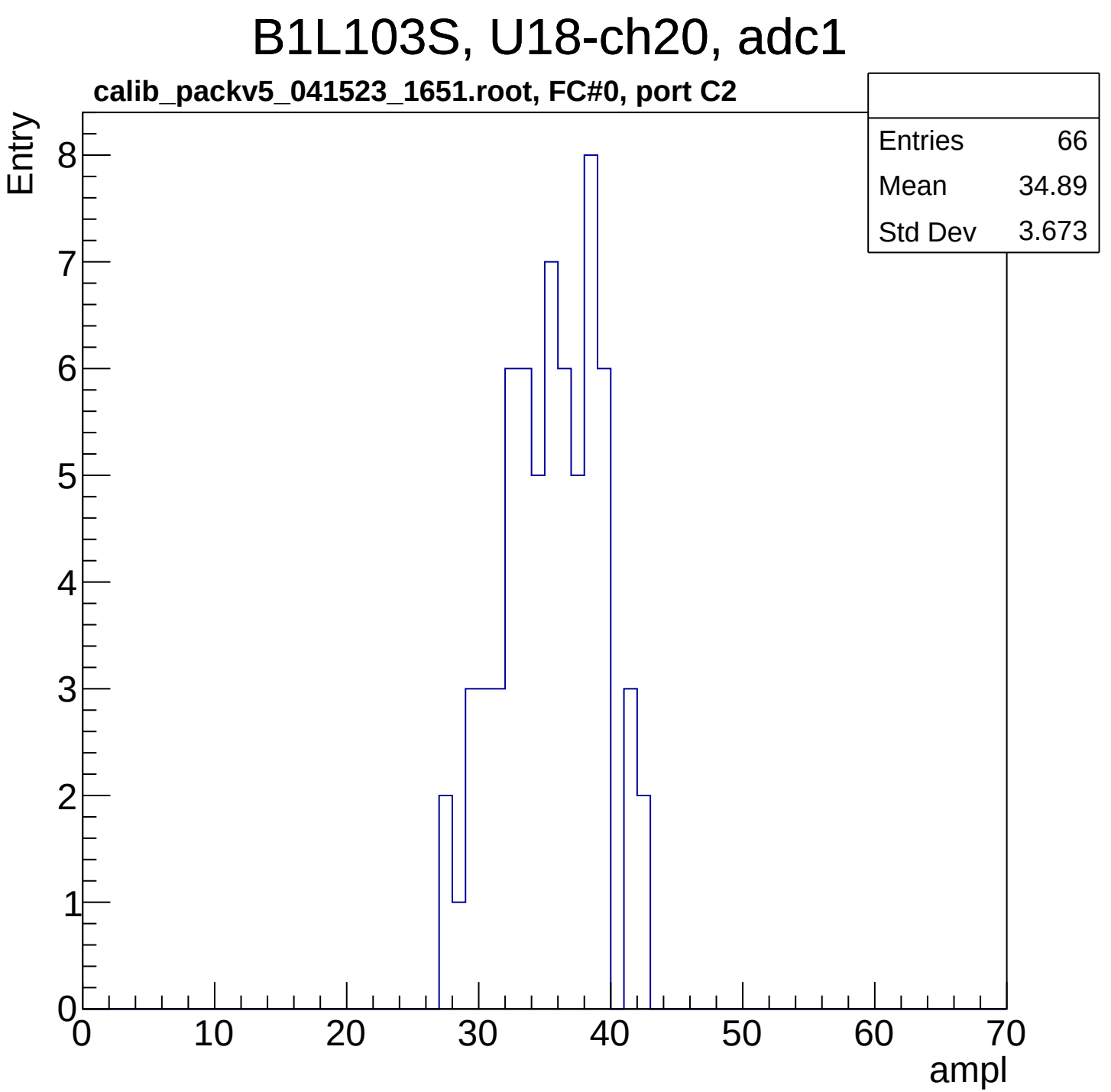
70
ampl


B1L103S, U18-ch20, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 34.89
Std Dev 3.673
Entry
ampl
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2
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60
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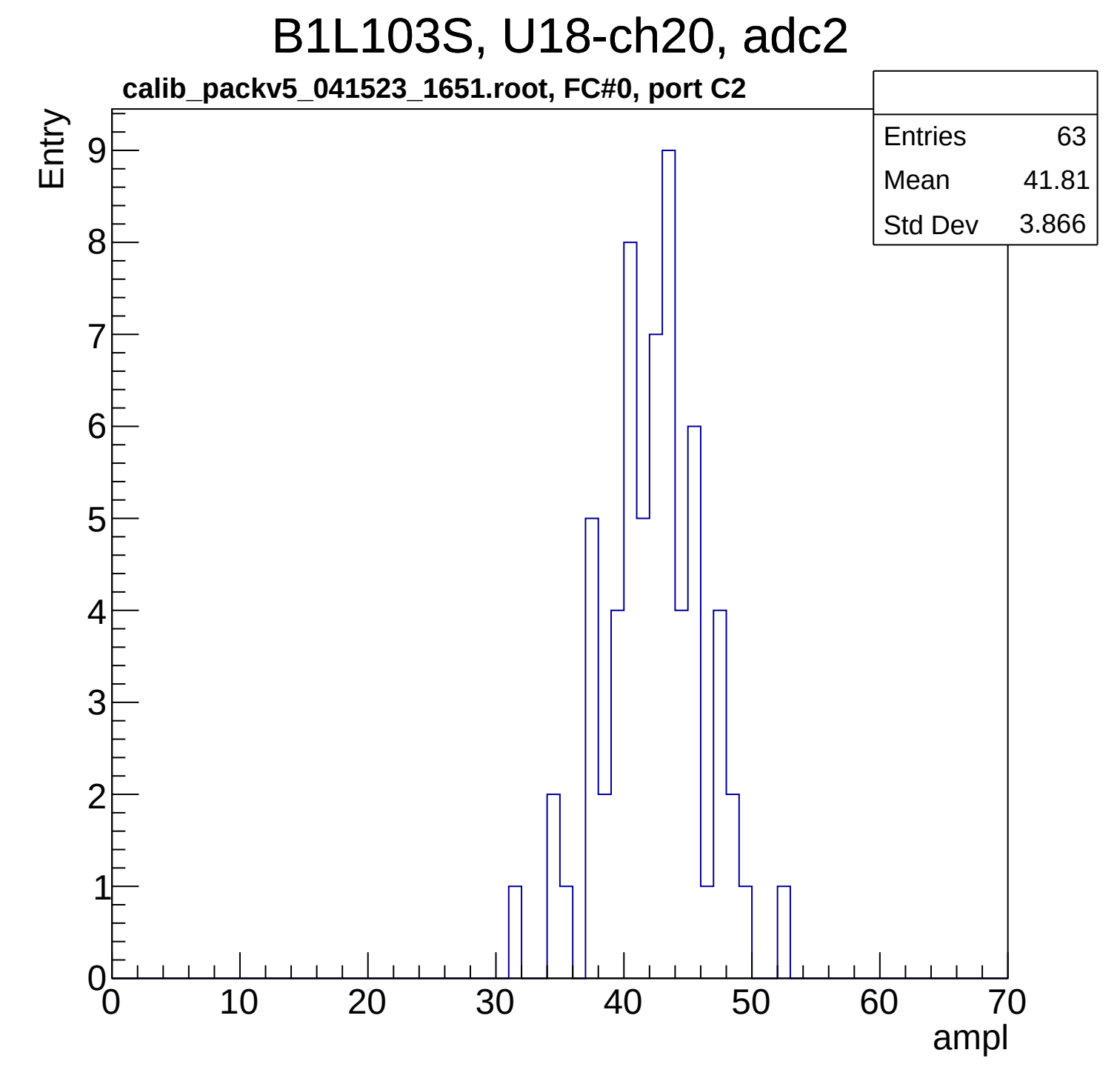
B1L103S, U18-ch20, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 41.81
Std Dev 3.866
Entry
ampl
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3
4
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6
7
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0
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60
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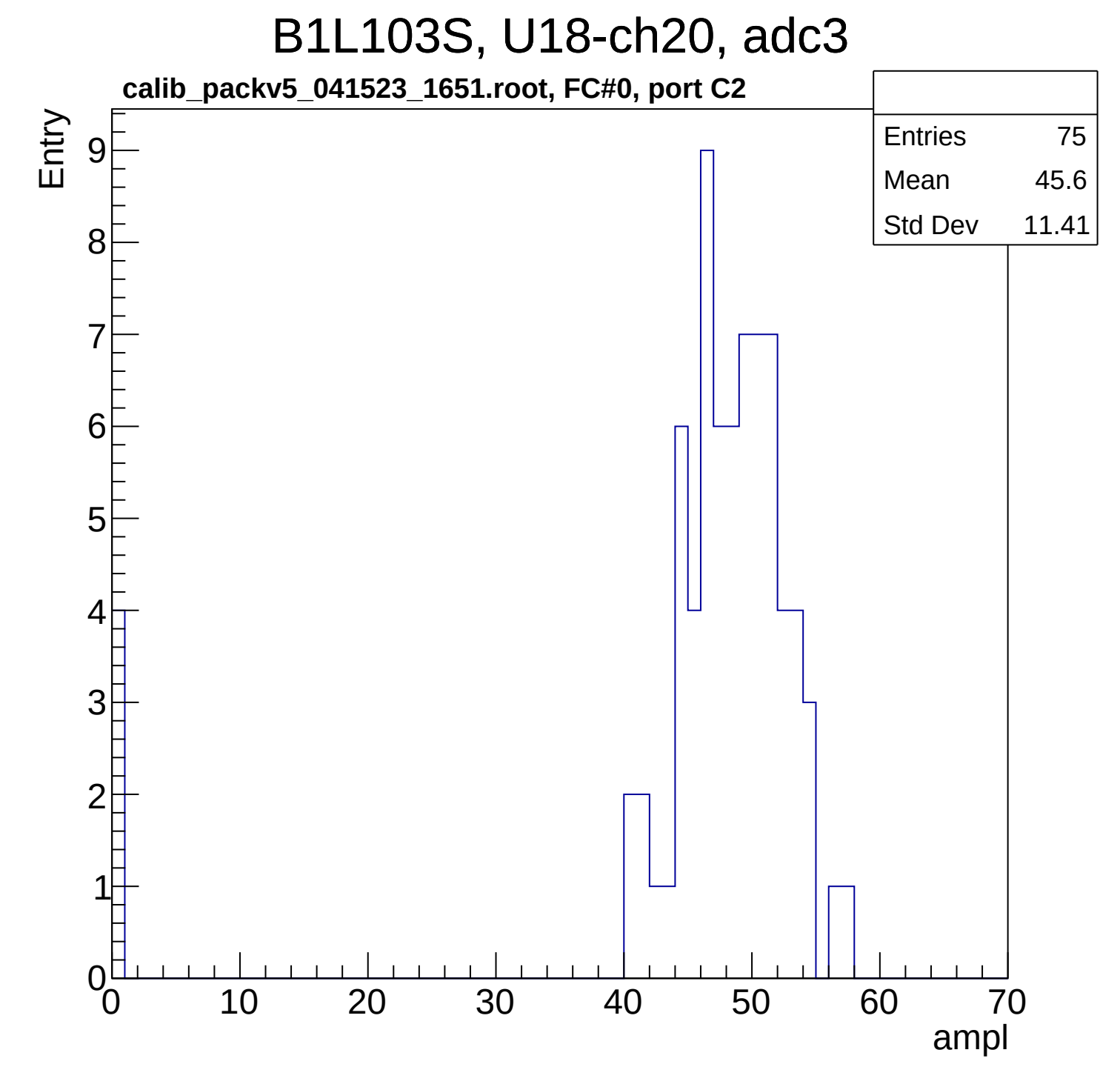
B1L103S, U18-ch20, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 45.6
Std Dev 11.41
Entry
ampl
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2
3
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6
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8
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0
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40
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60
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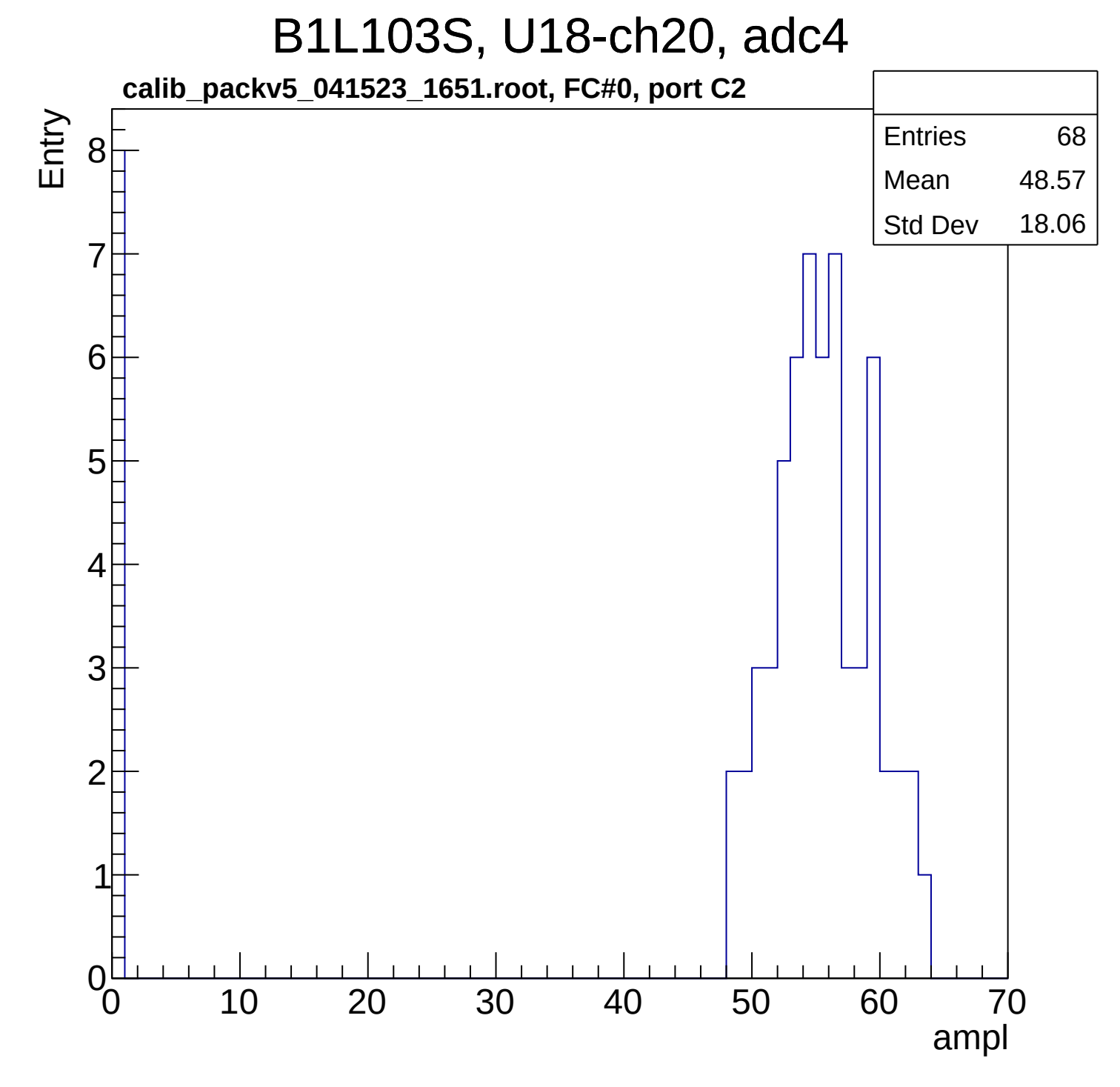
B1L103S, U18-ch20, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 48.57
Std Dev 18.06
Entry
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2
3
4
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8
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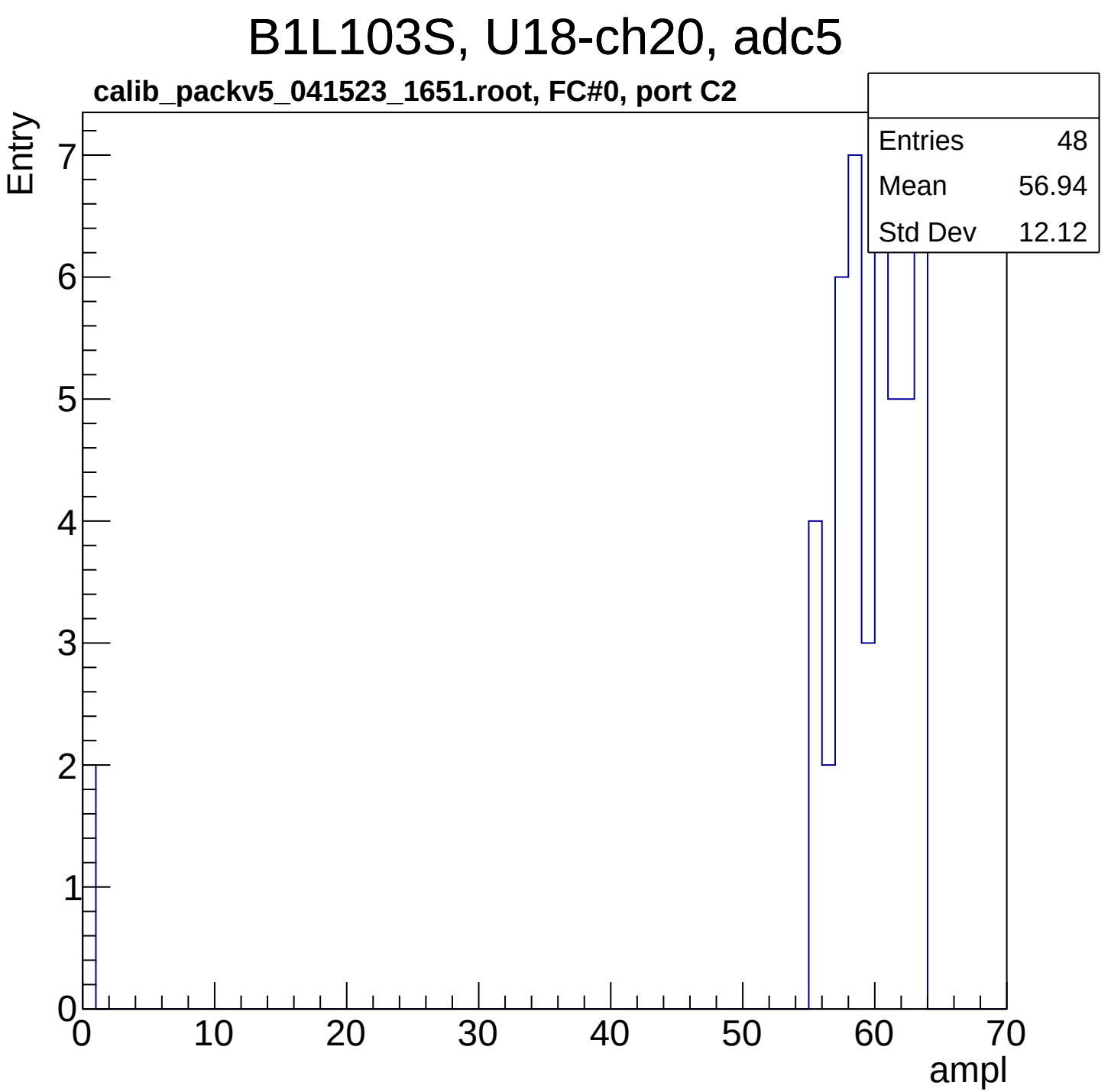
50
60
70
ampl


B1L103S, U18-ch20, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 56.94
Std Dev 12.12
Entry
ampl
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1
2
3
4
5
6
7
0
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20
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40
50
60
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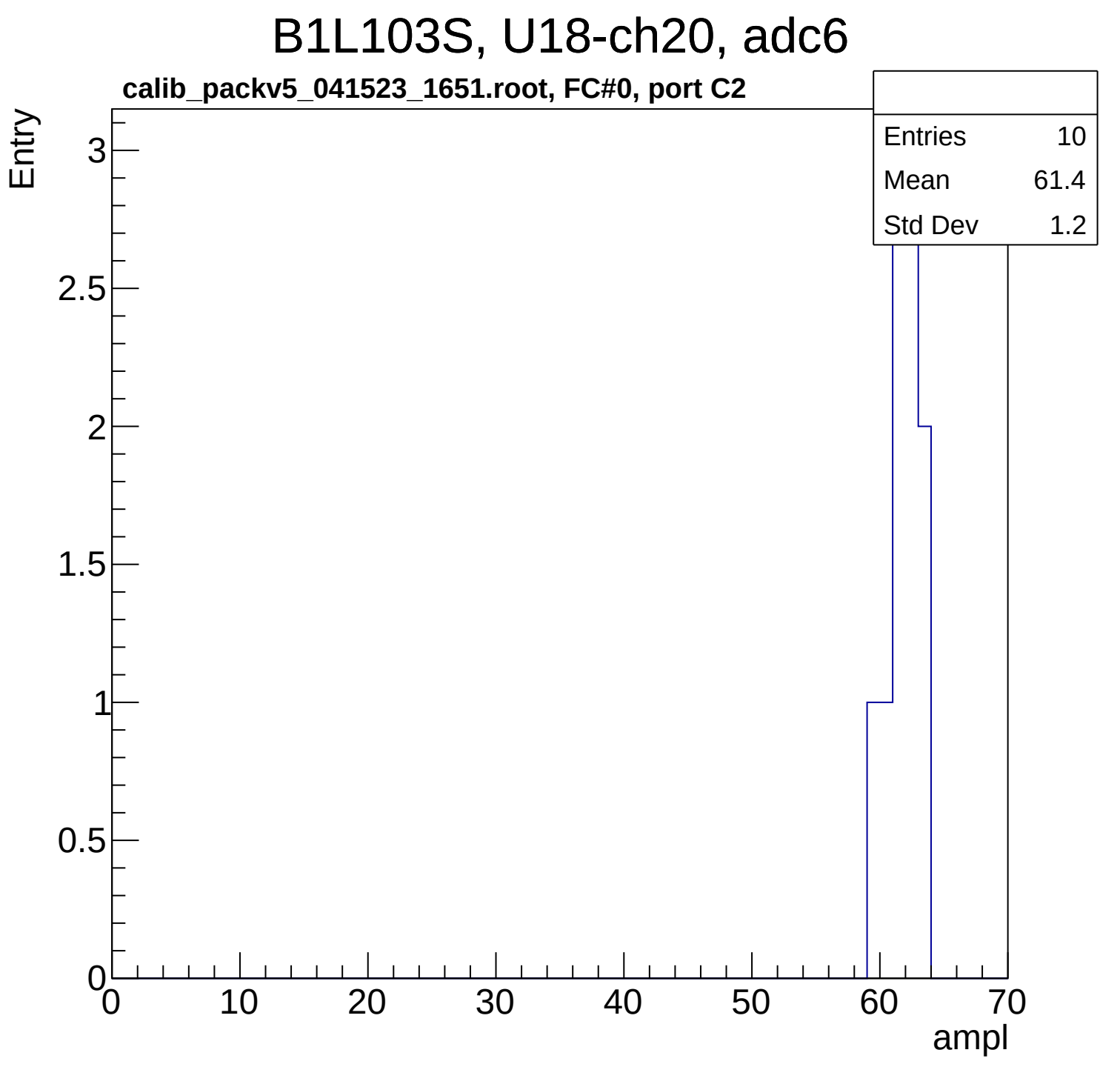
B1L103S, U18-ch20, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 61.4
Std Dev 1.2
Entry
ampl
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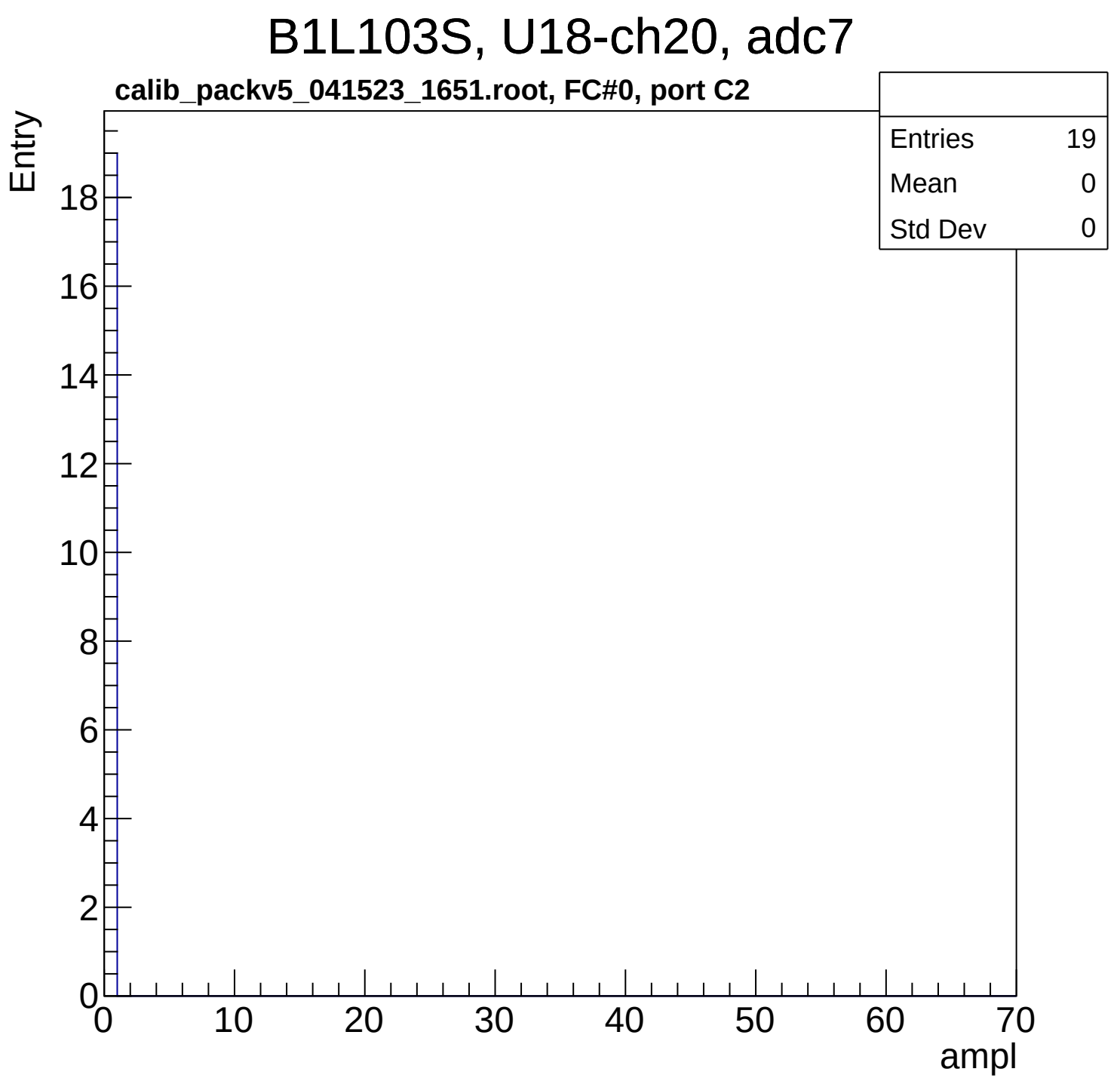
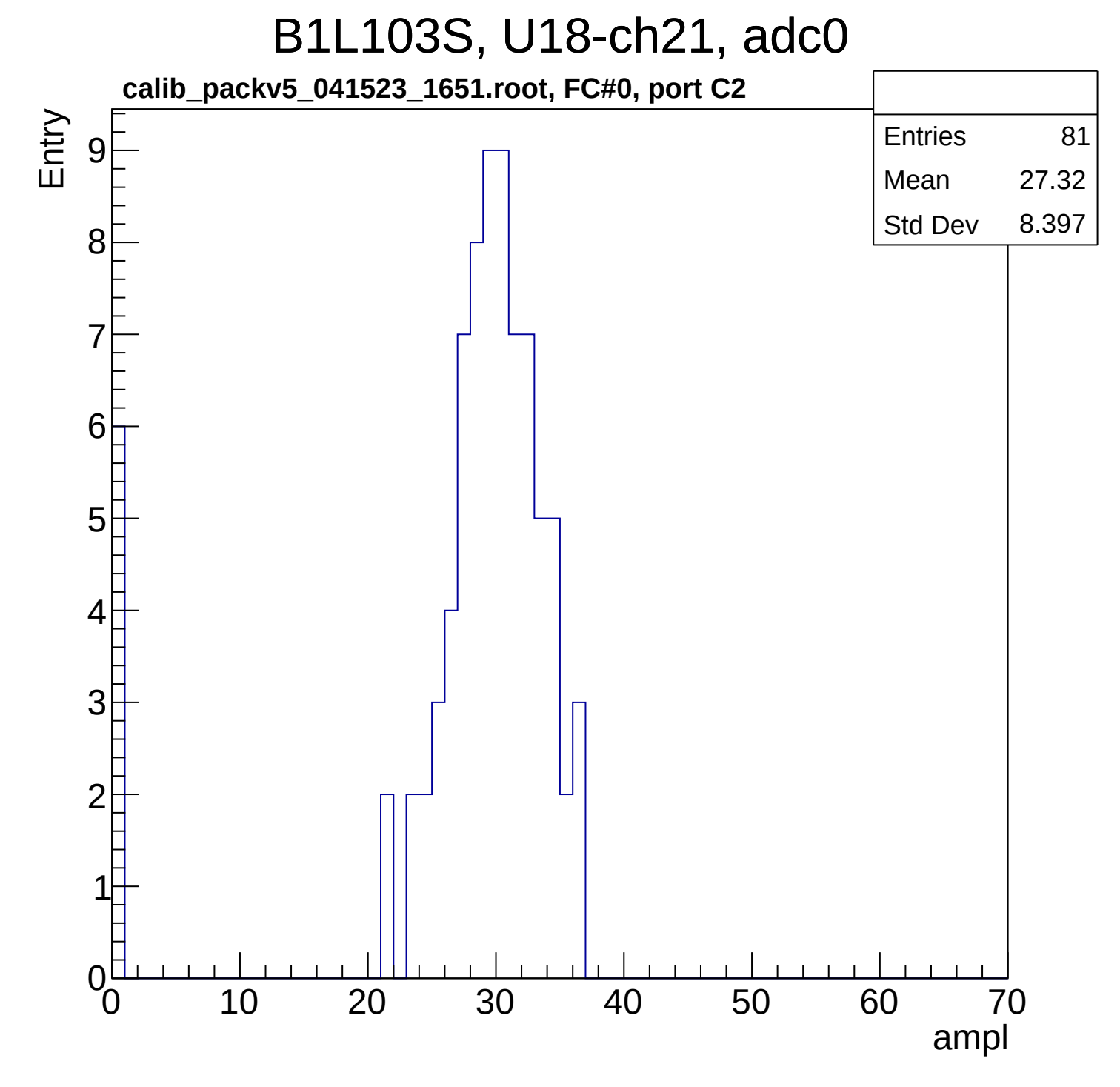
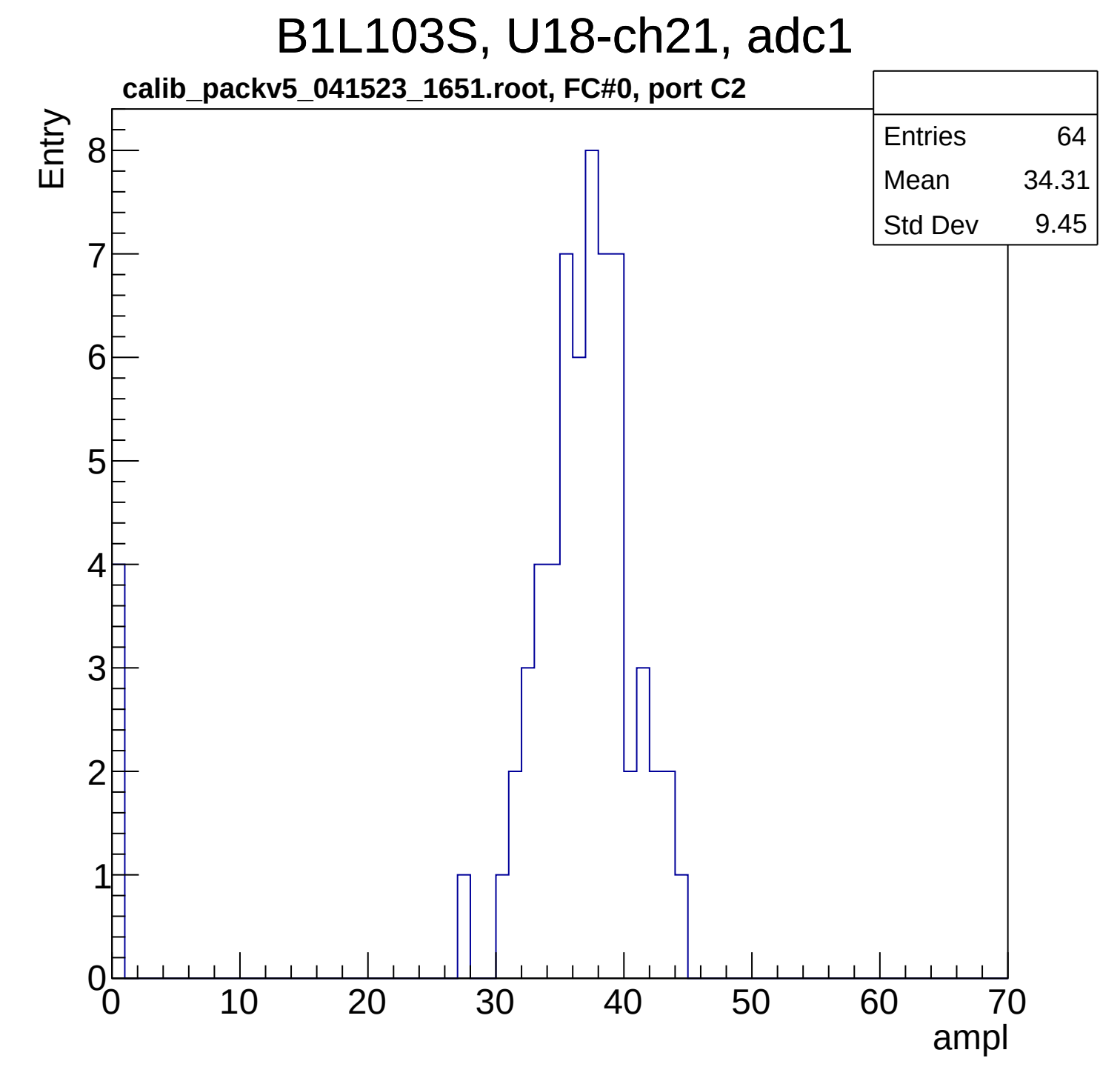
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U18-ch20, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch21, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 27.32
Std Dev 8.397
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U18-ch21, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 34.31
Std Dev 9.45
Entry
ampl
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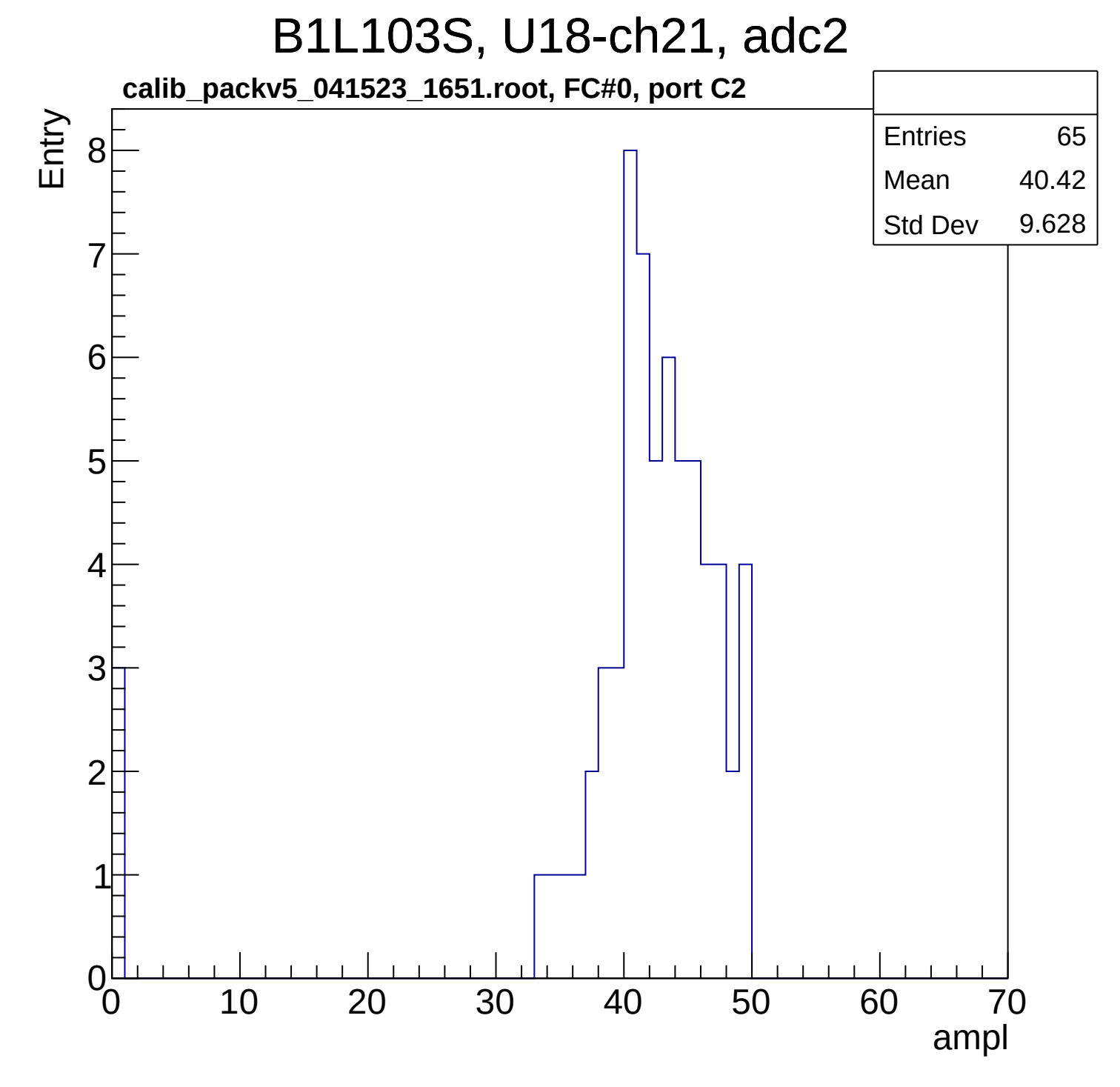
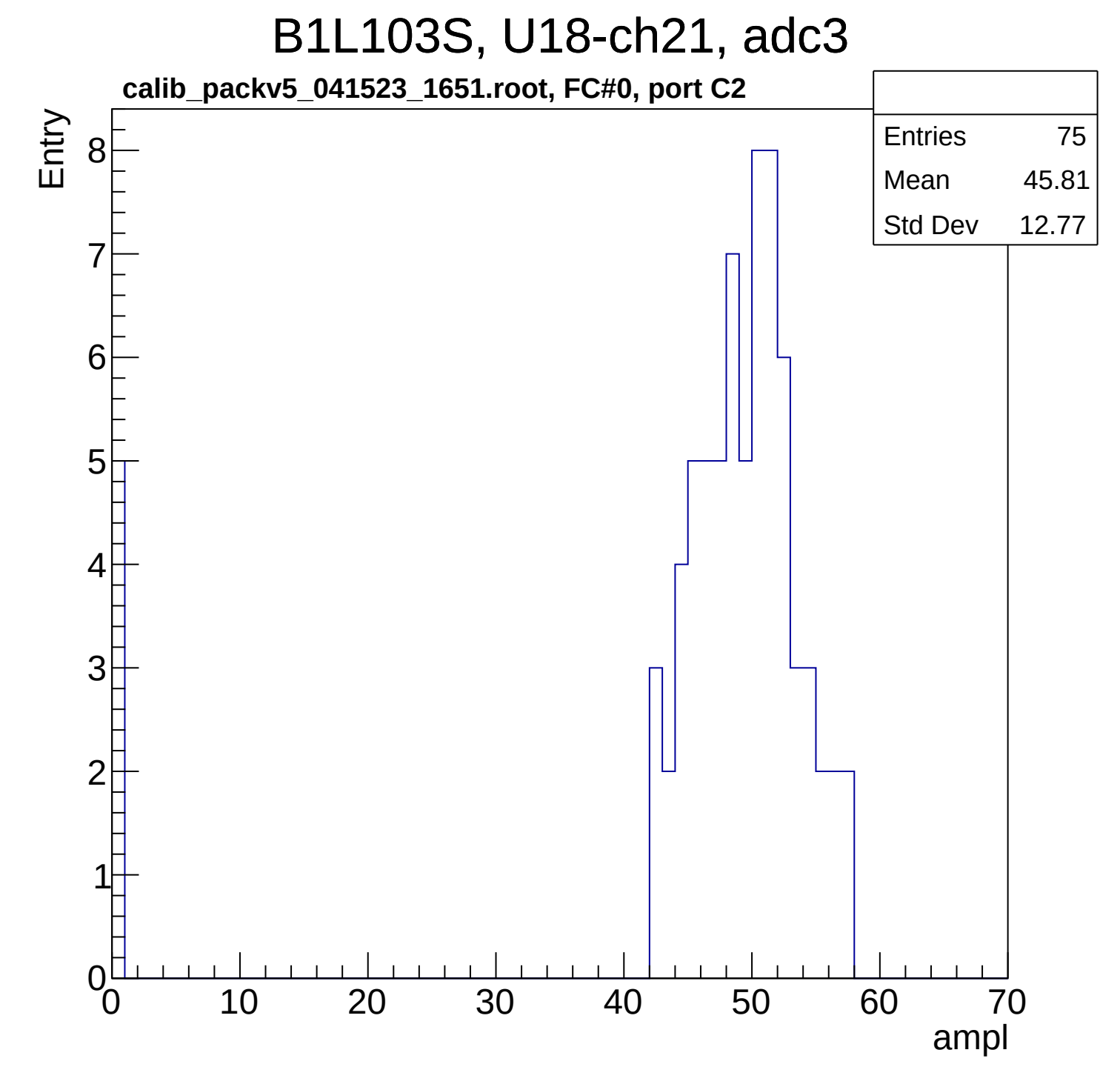
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch21, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 40.42
Std Dev 9.628
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch21, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 45.81
Std Dev 12.77
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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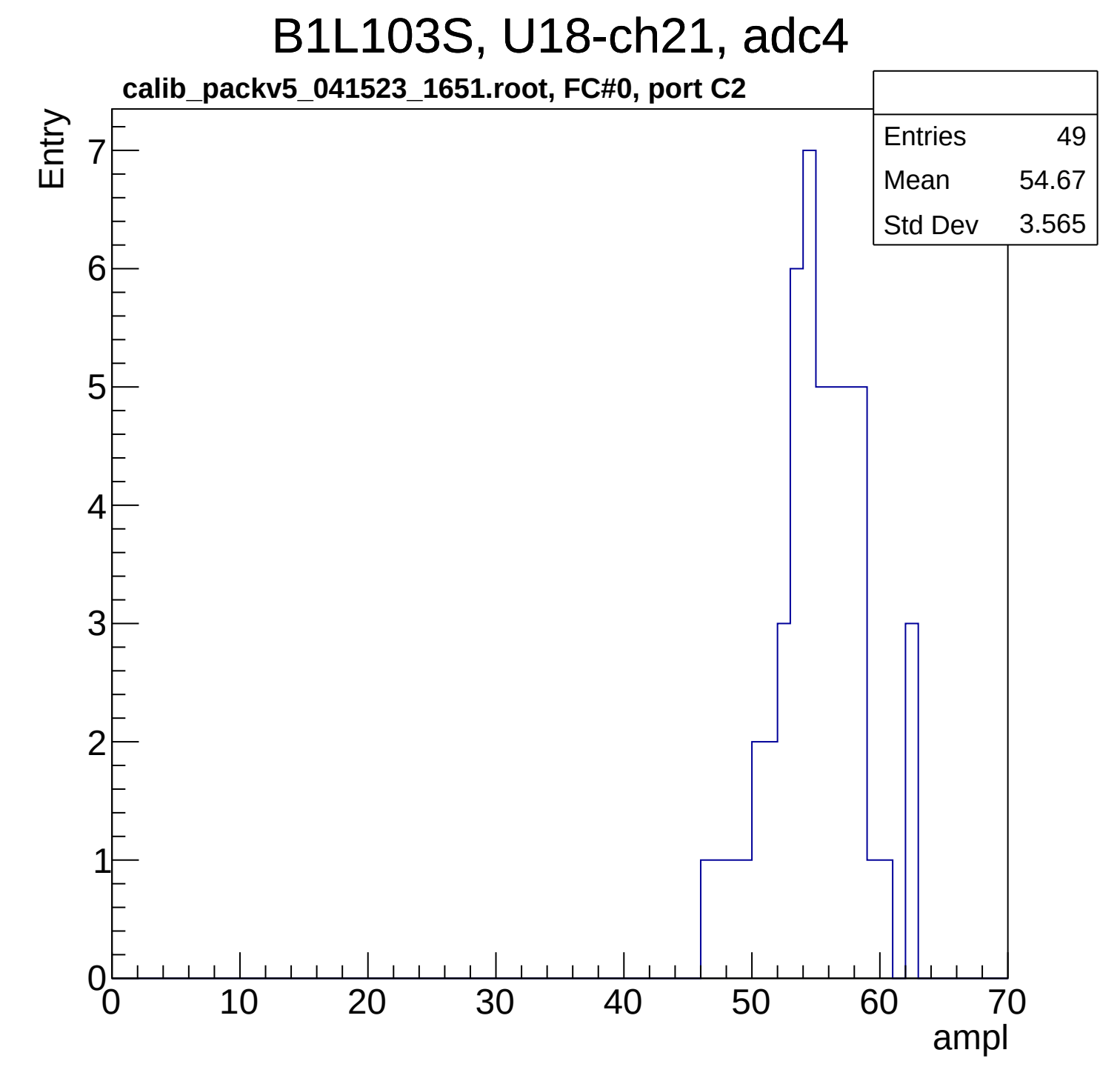
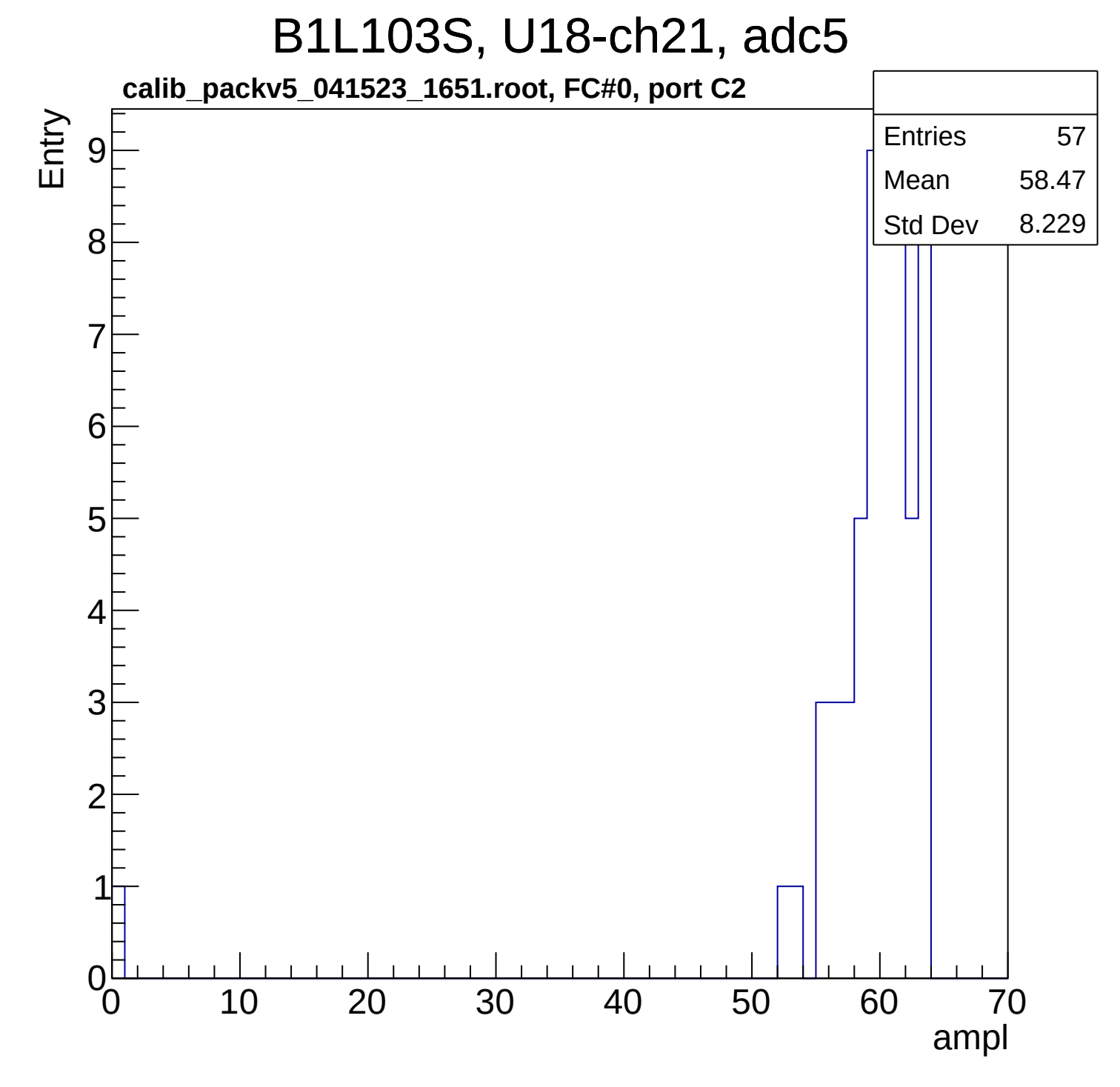
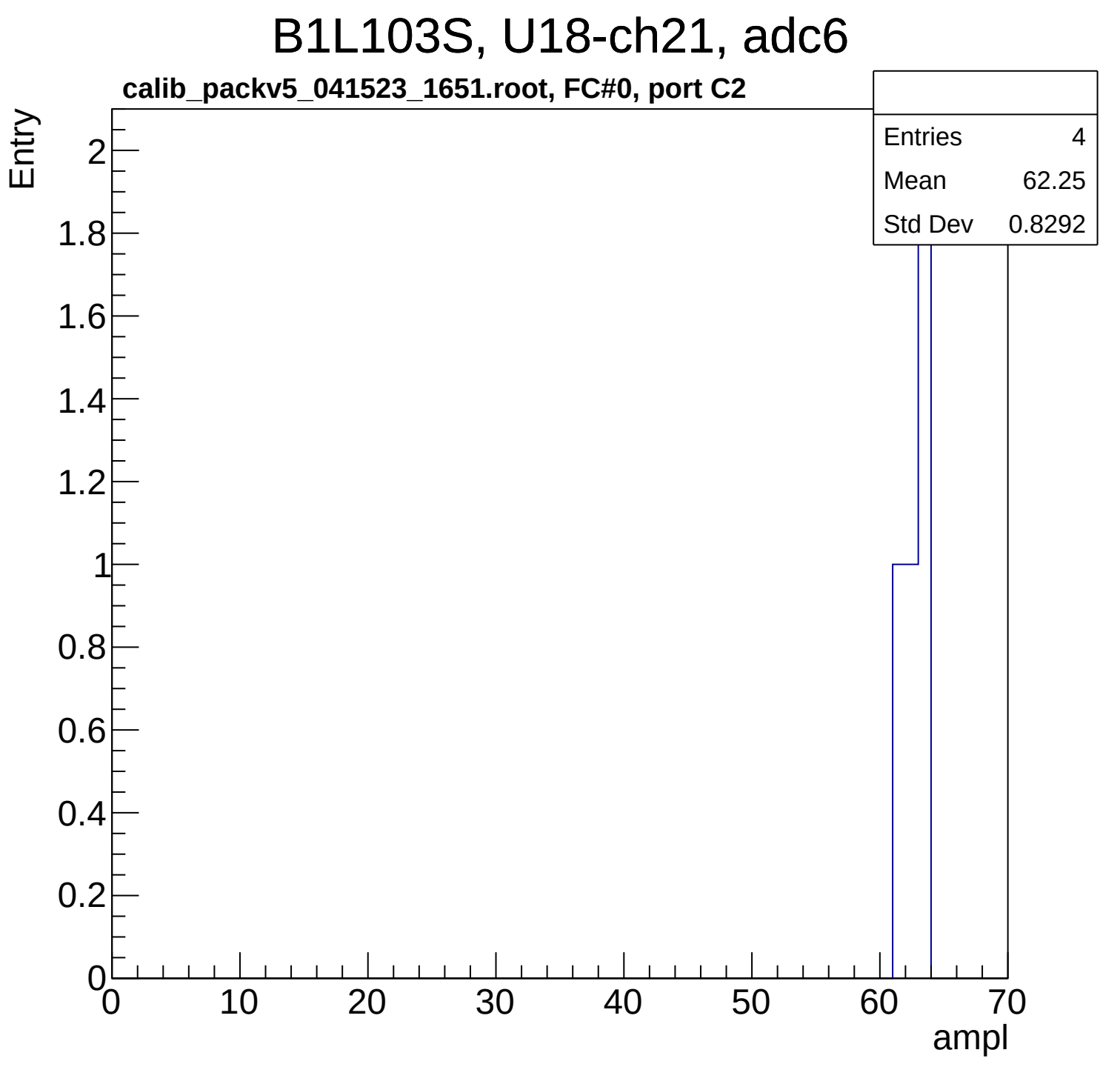
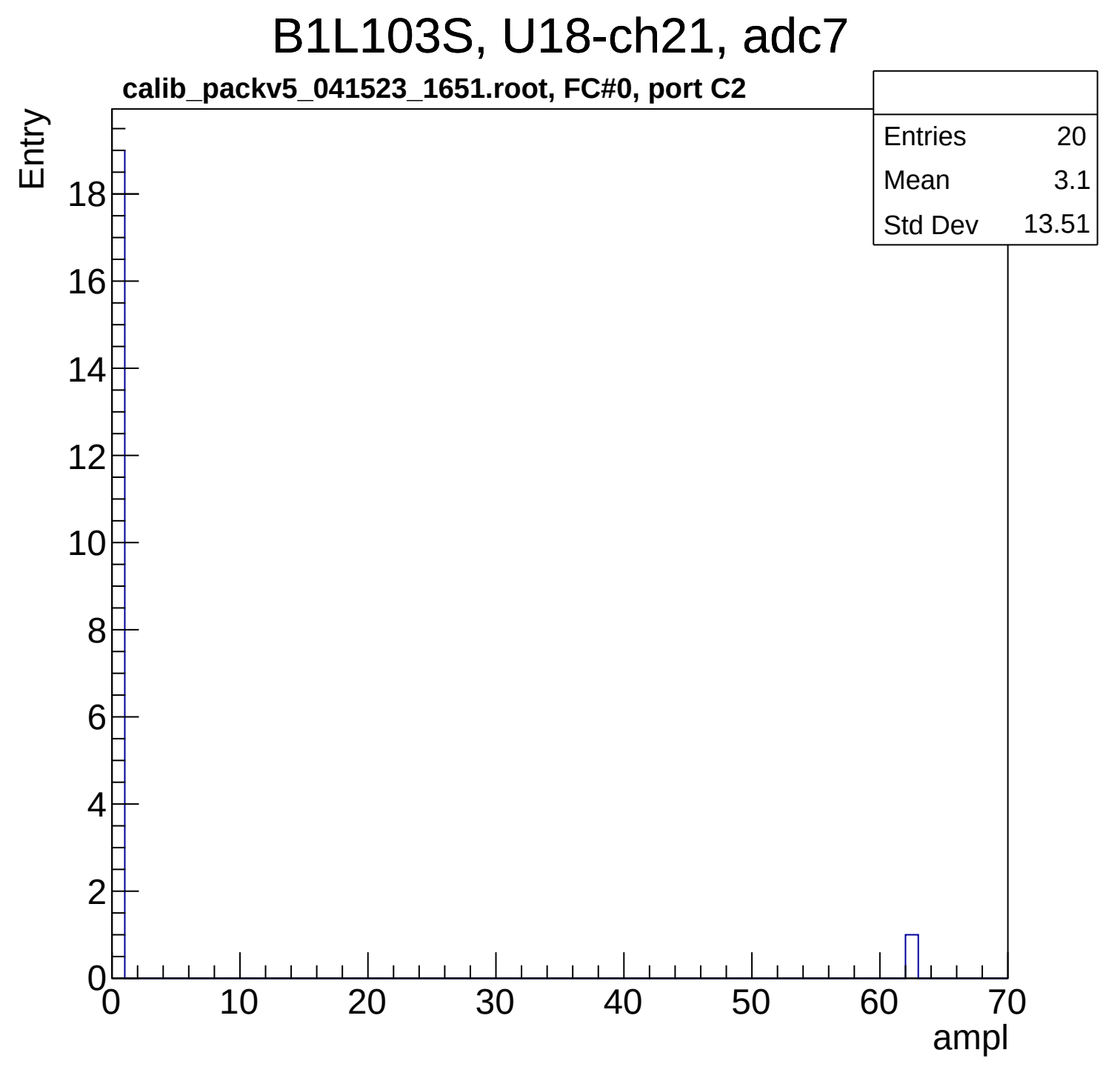
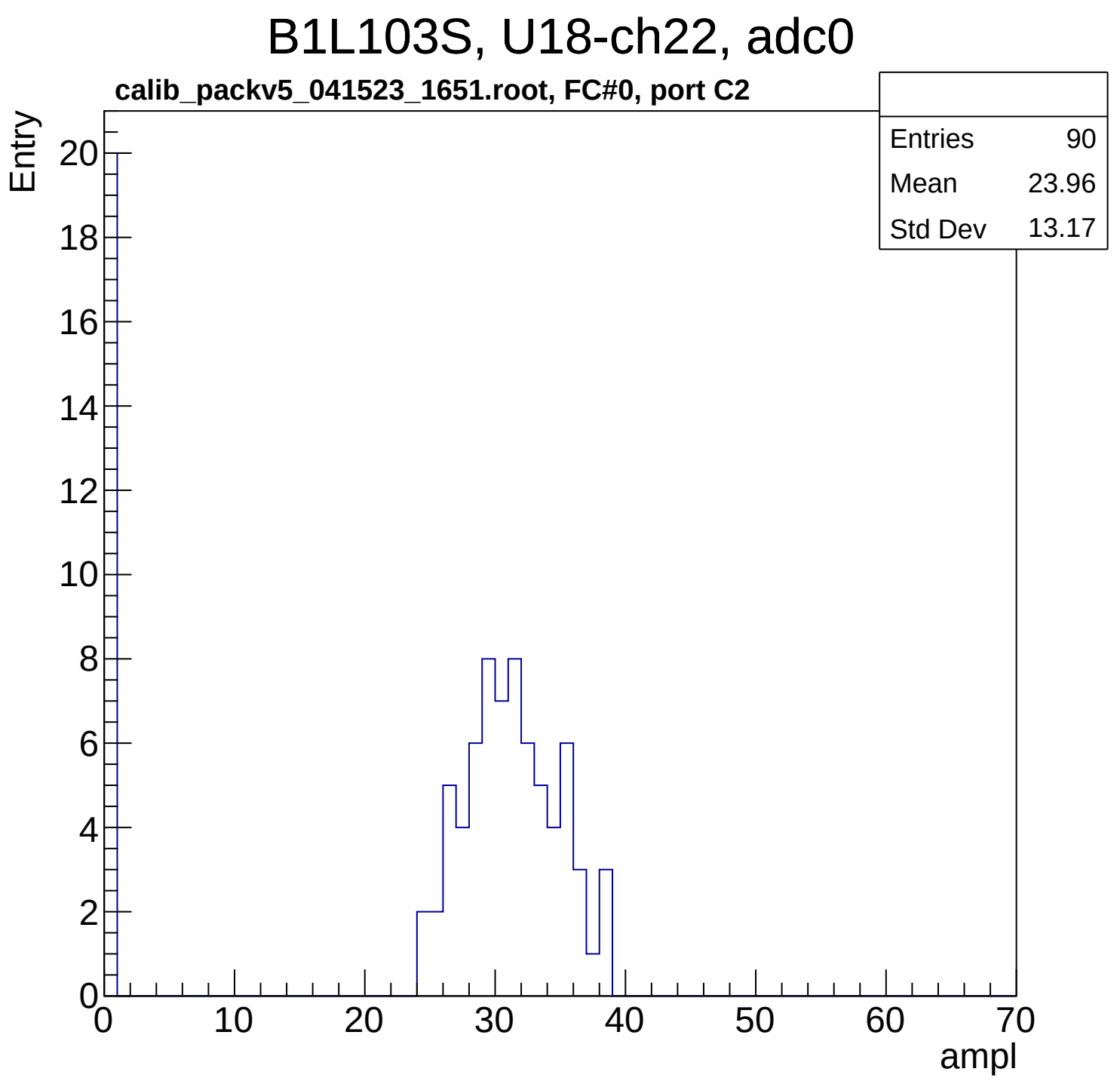

B1L103S, U18-ch21, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 54.67
Std Dev 3.565
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U18-ch21, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 58.47
Std Dev 8.229
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U18-ch21, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 4
Mean 62.25
Std Dev 0.8292
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U18-ch21, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.1
Std Dev 13.51
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch22, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 90
Mean 23.96
Std Dev 13.17
Entry
ampl
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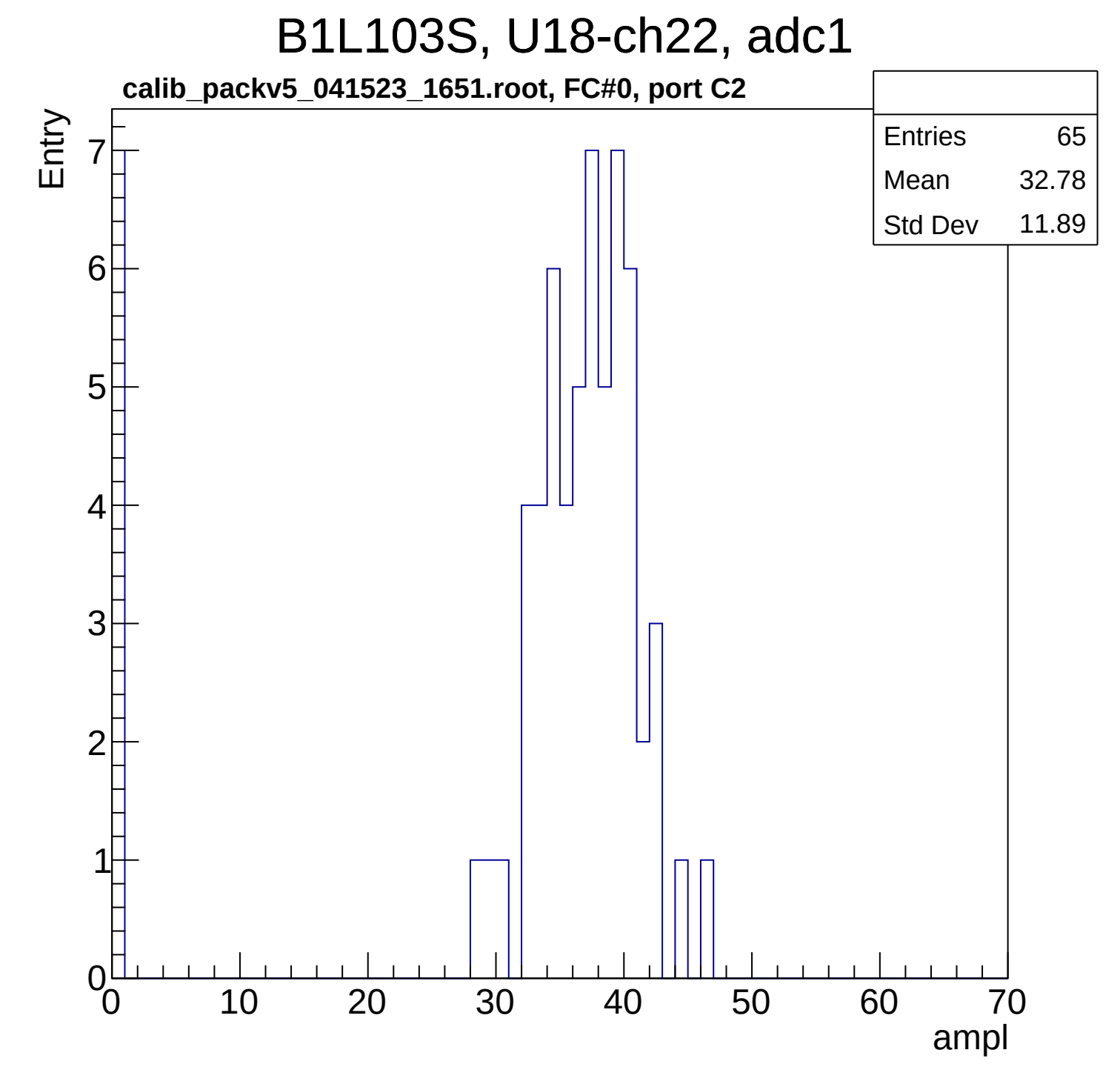
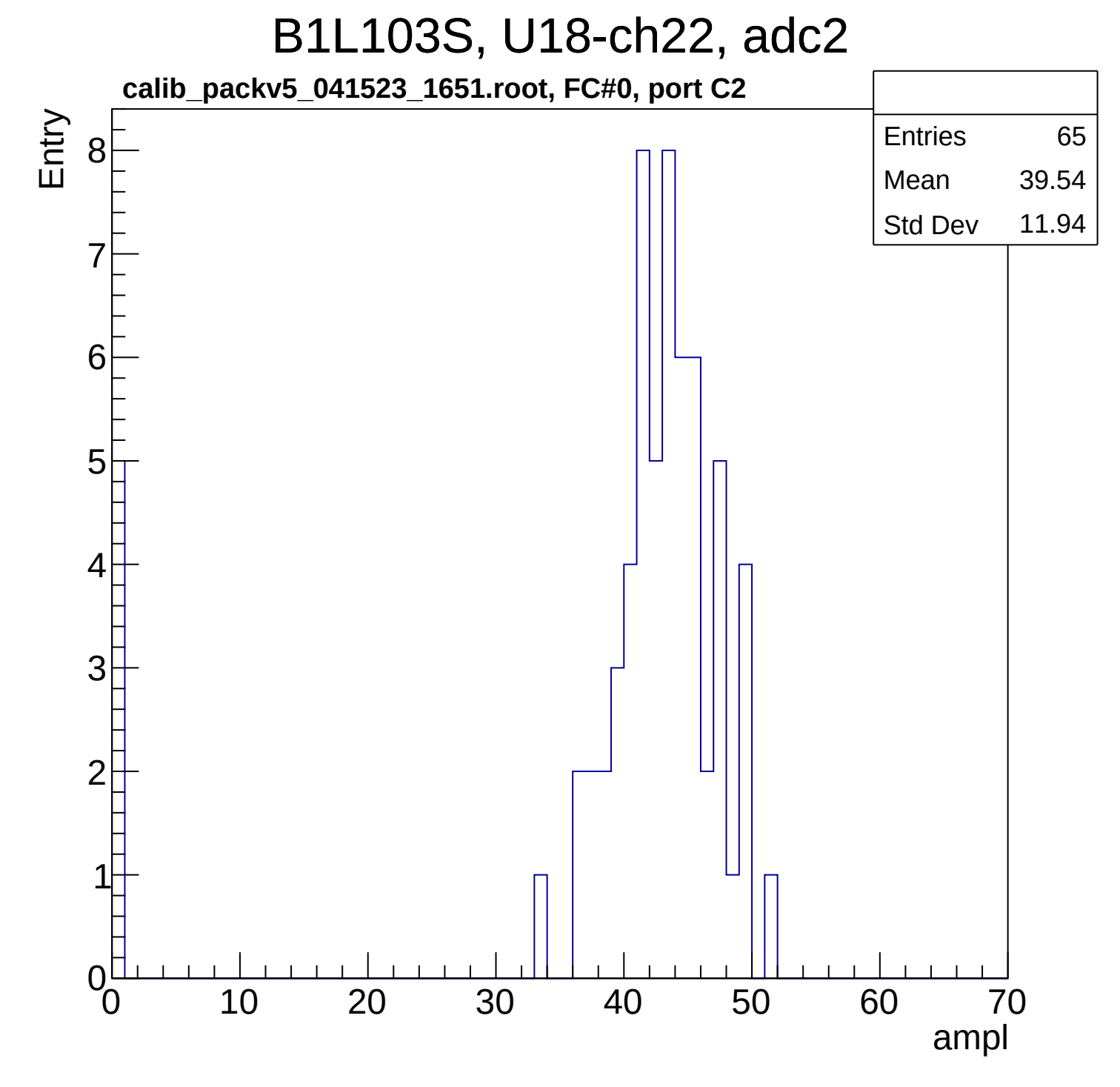
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70


B1L103S, U18-ch22, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 32.78
Std Dev 11.89
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U18-ch22, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 39.54
Std Dev 11.94
Entry
ampl
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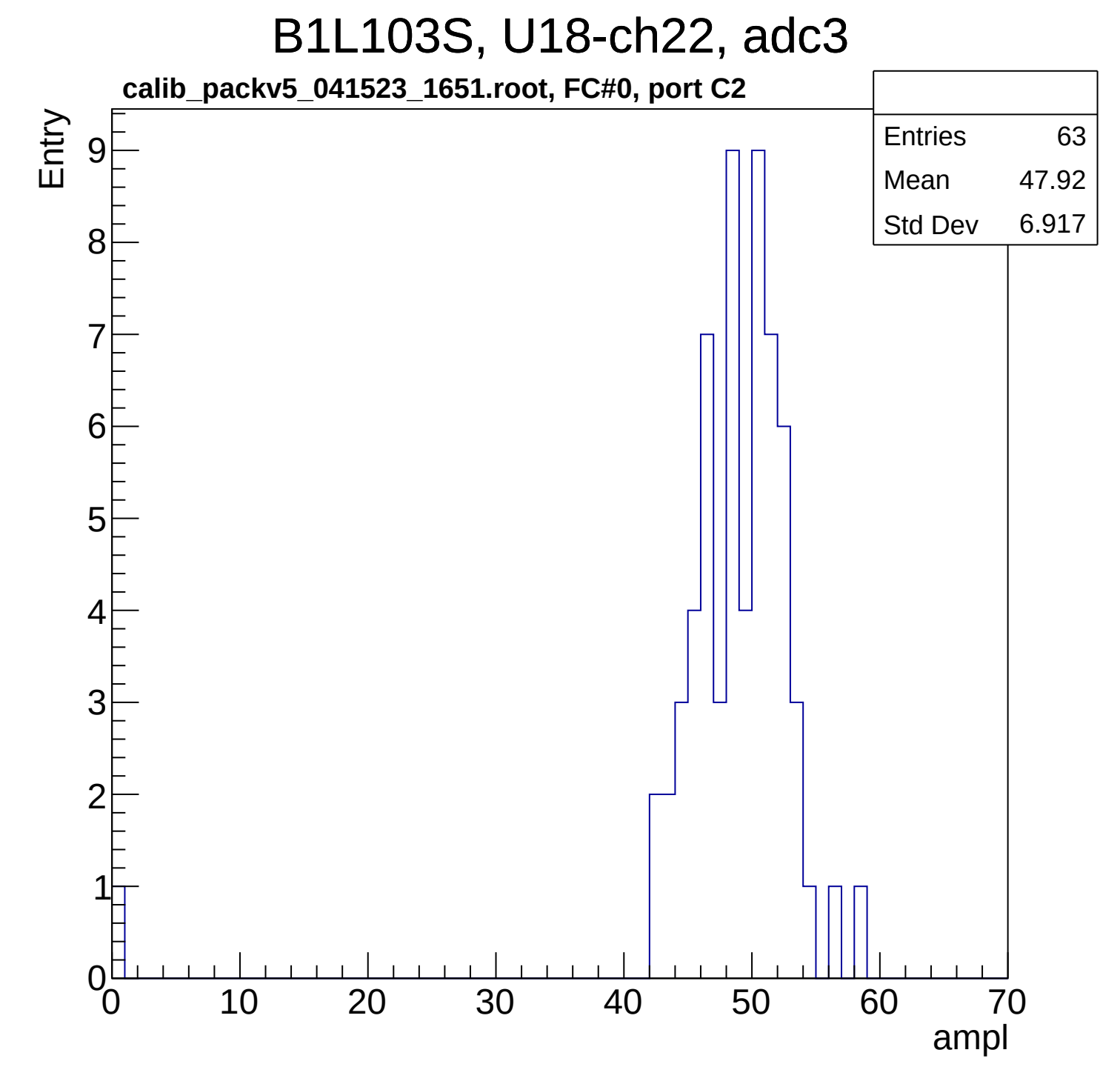
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch22, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 47.92
Std Dev 6.917
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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40
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60
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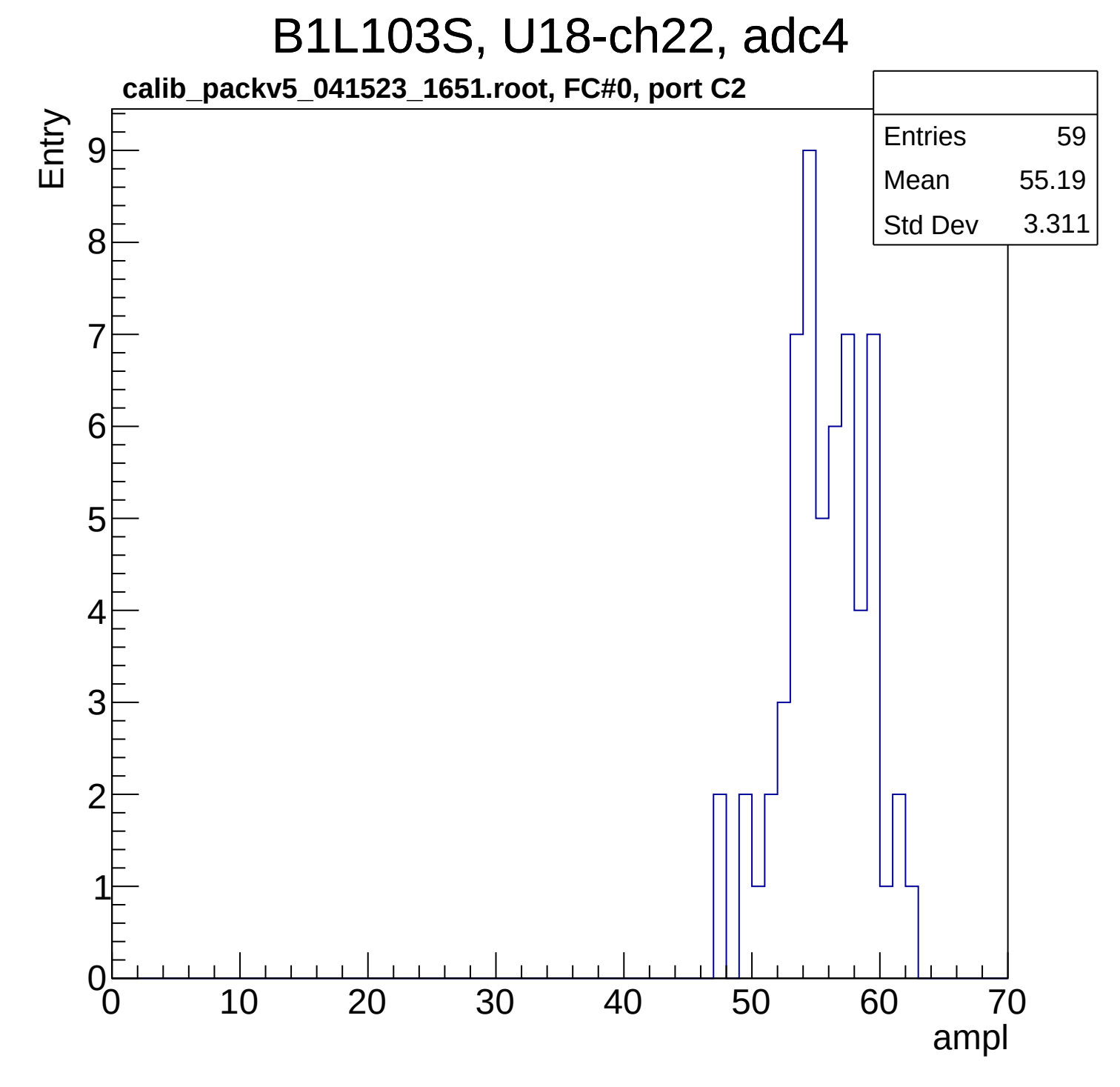
B1L103S, U18-ch22, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 55.19
Std Dev 3.311
Entry
ampl
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3
4
5
6
7
8
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0
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40
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60
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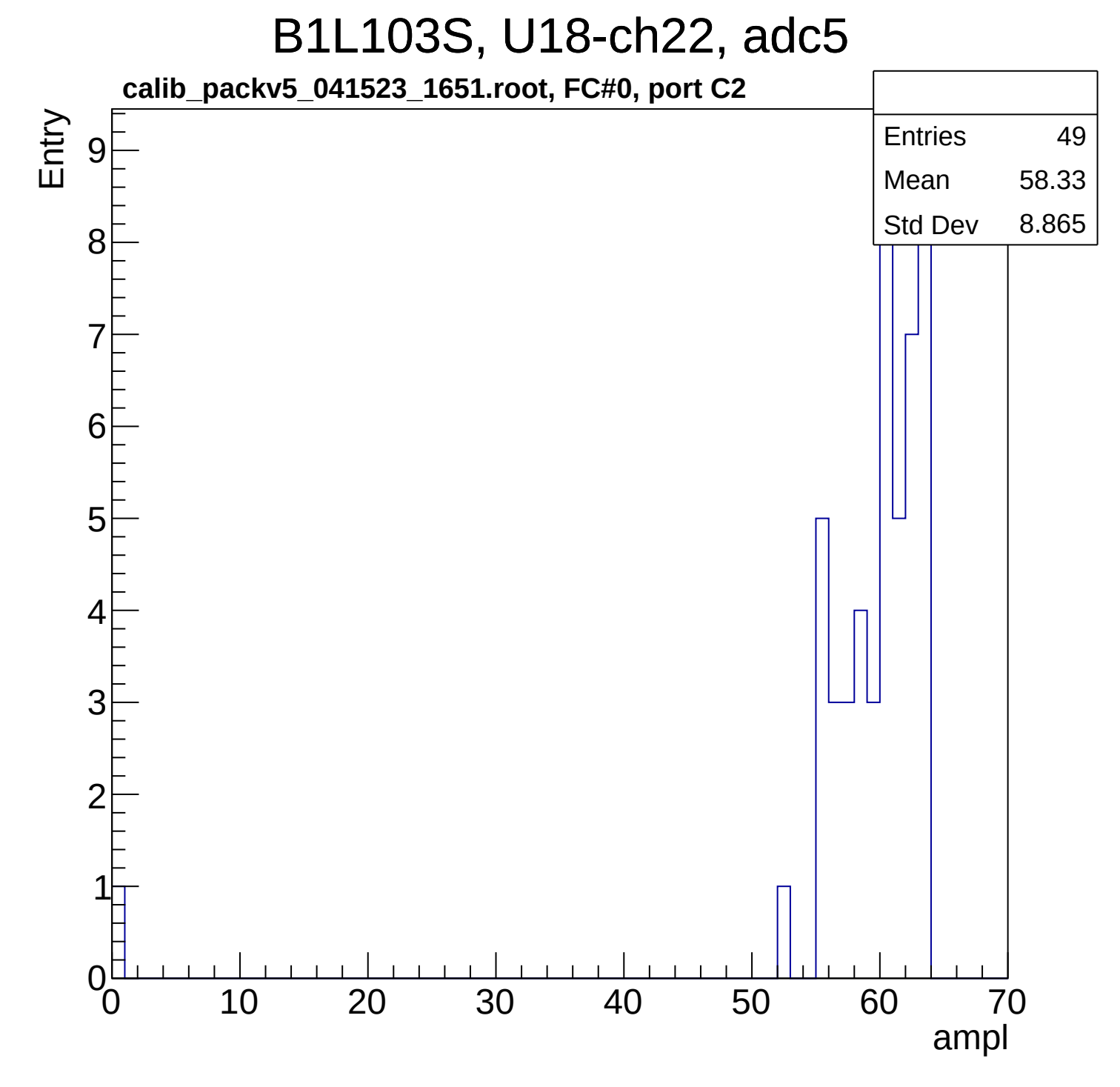
B1L103S, U18-ch22, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 58.33
Std Dev 8.865
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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40
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60
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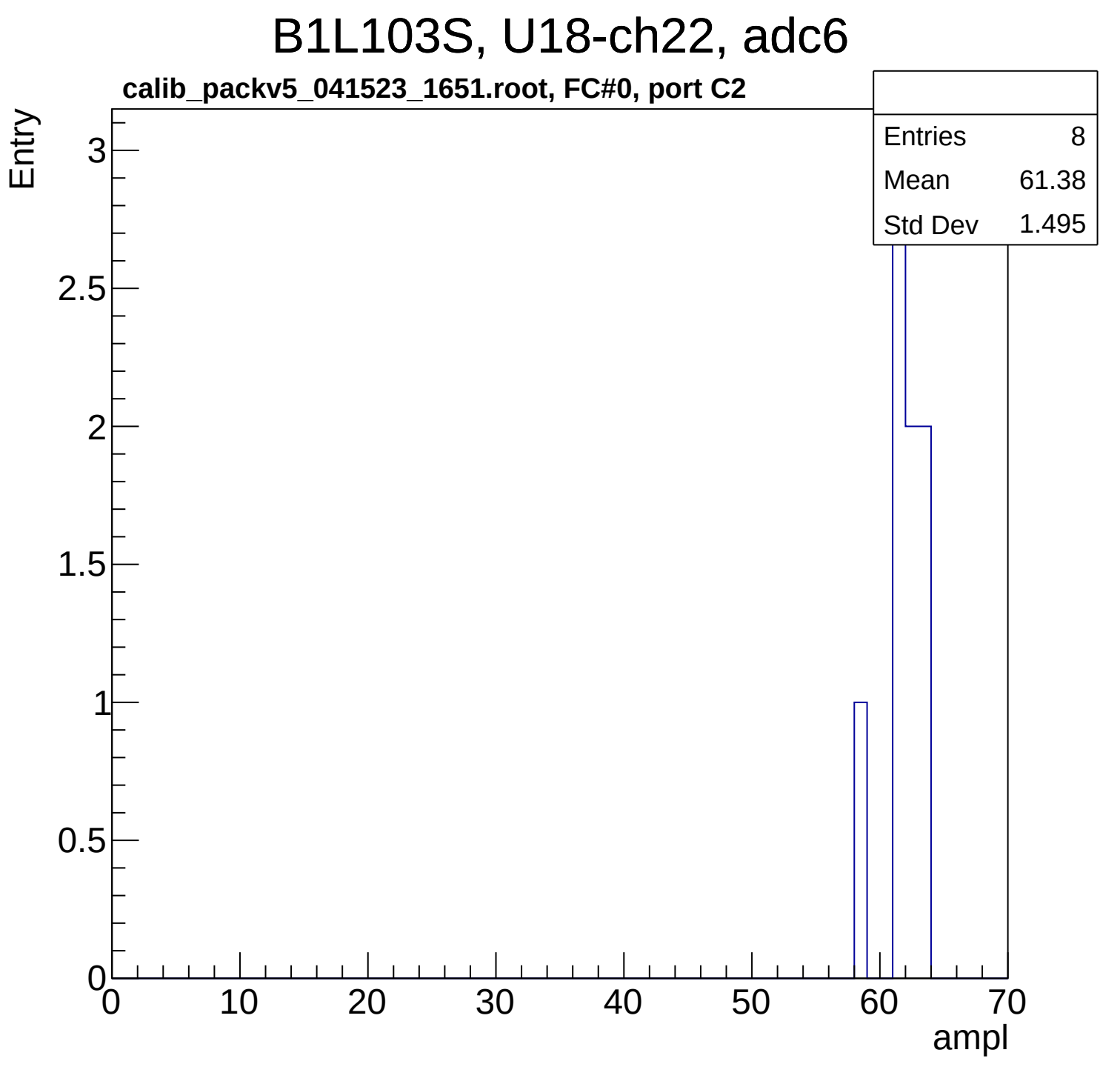
B1L103S, U18-ch22, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 61.38
Std Dev 1.495
Entry
ampl
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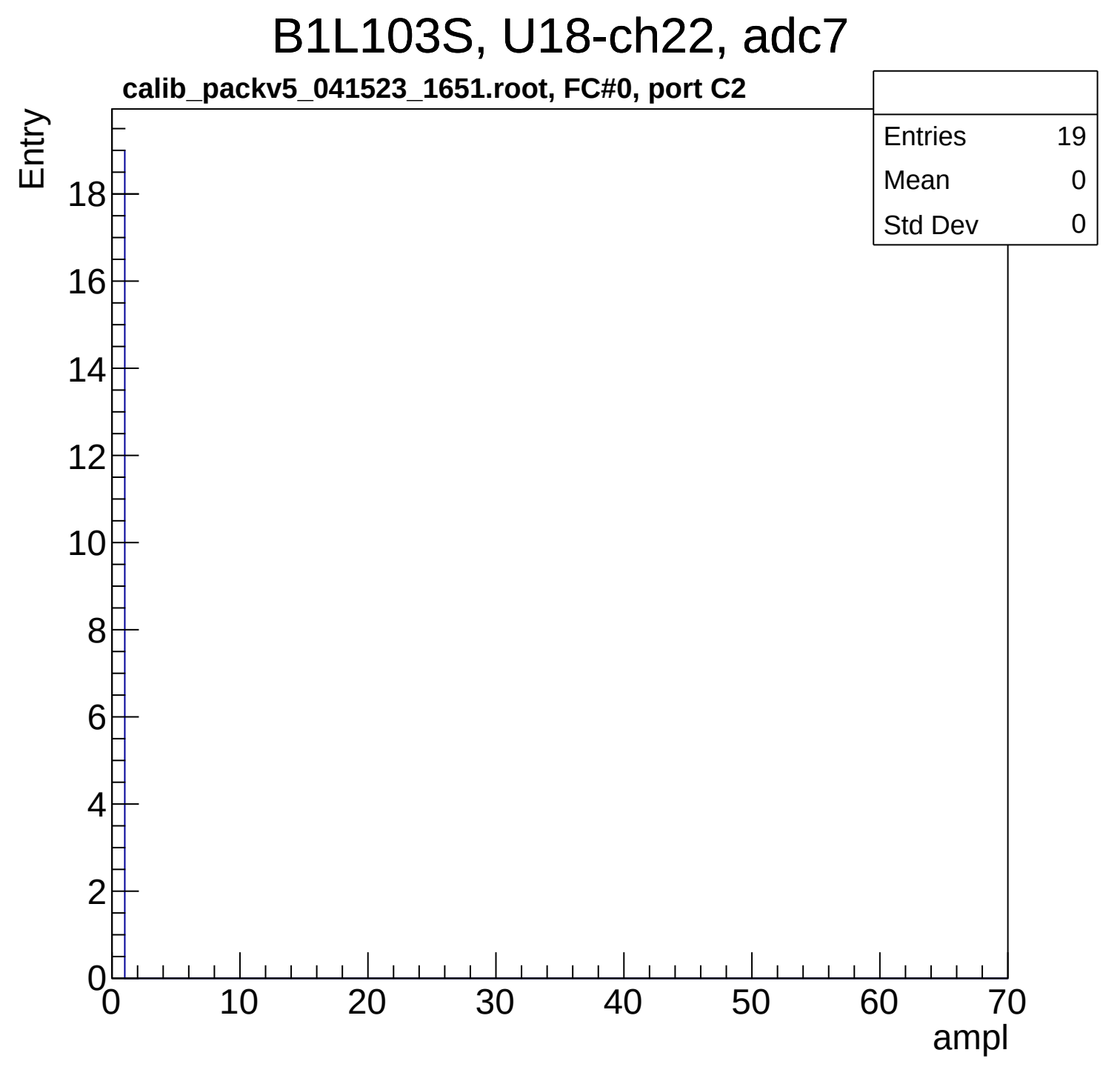
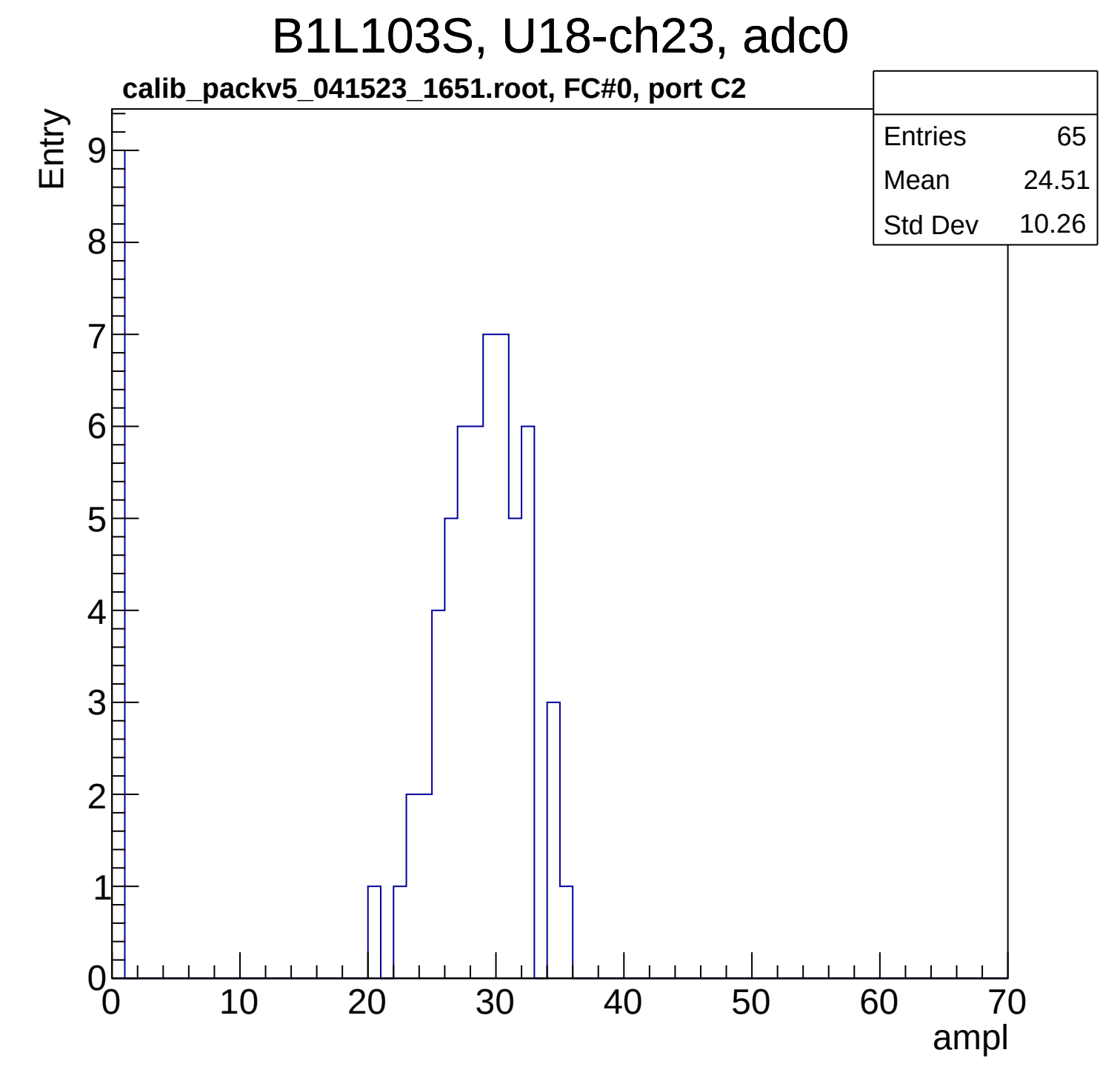
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U18-ch22, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch23, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 24.51
Std Dev 10.26
Entry
ampl
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3
4
5
6
7
8
9
0
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60
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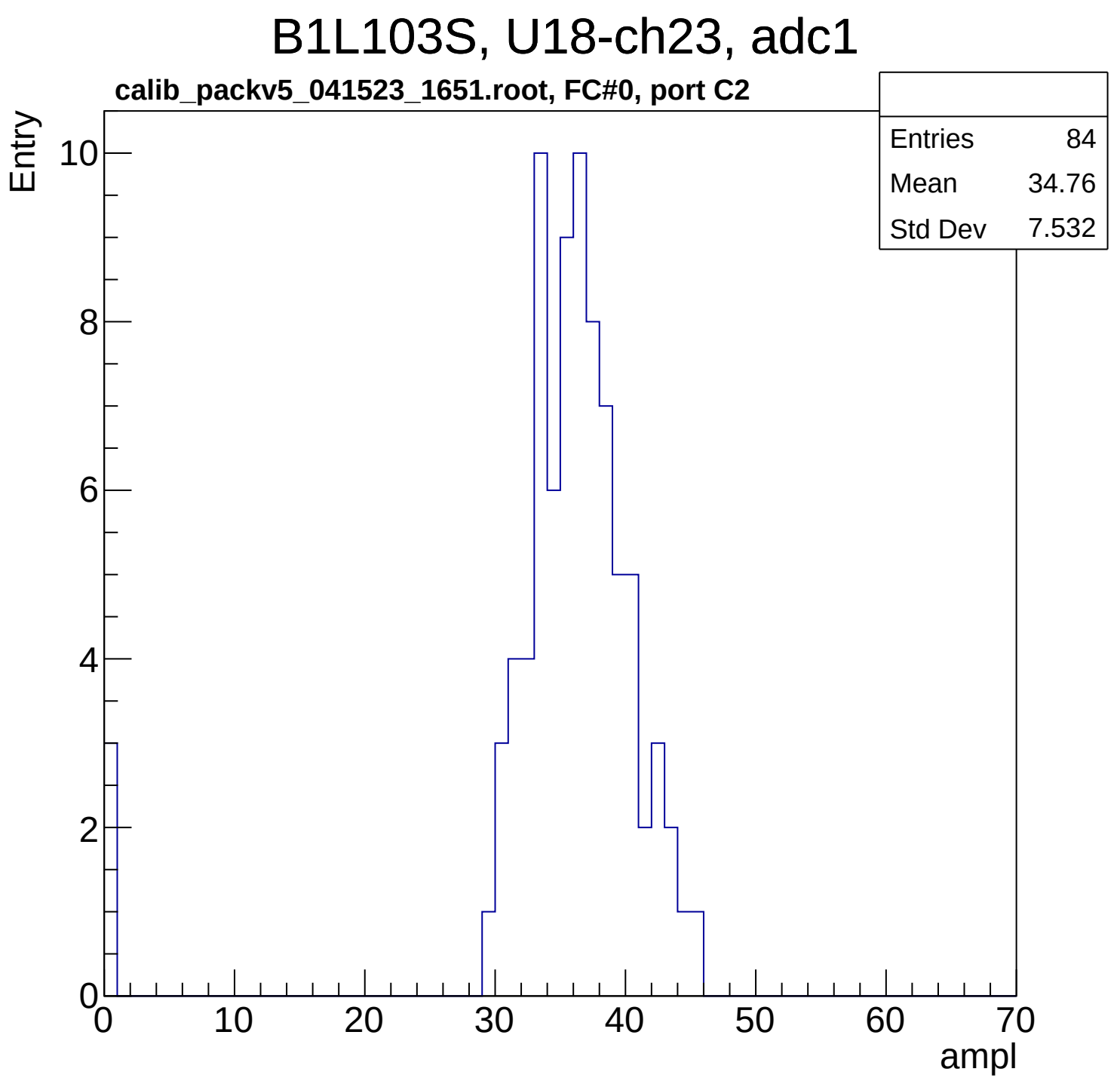
B1L103S, U18-ch23, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 34.76
Std Dev 7.532
Entry
ampl
0
2
4
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8
10
0
10
20
30
40
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60
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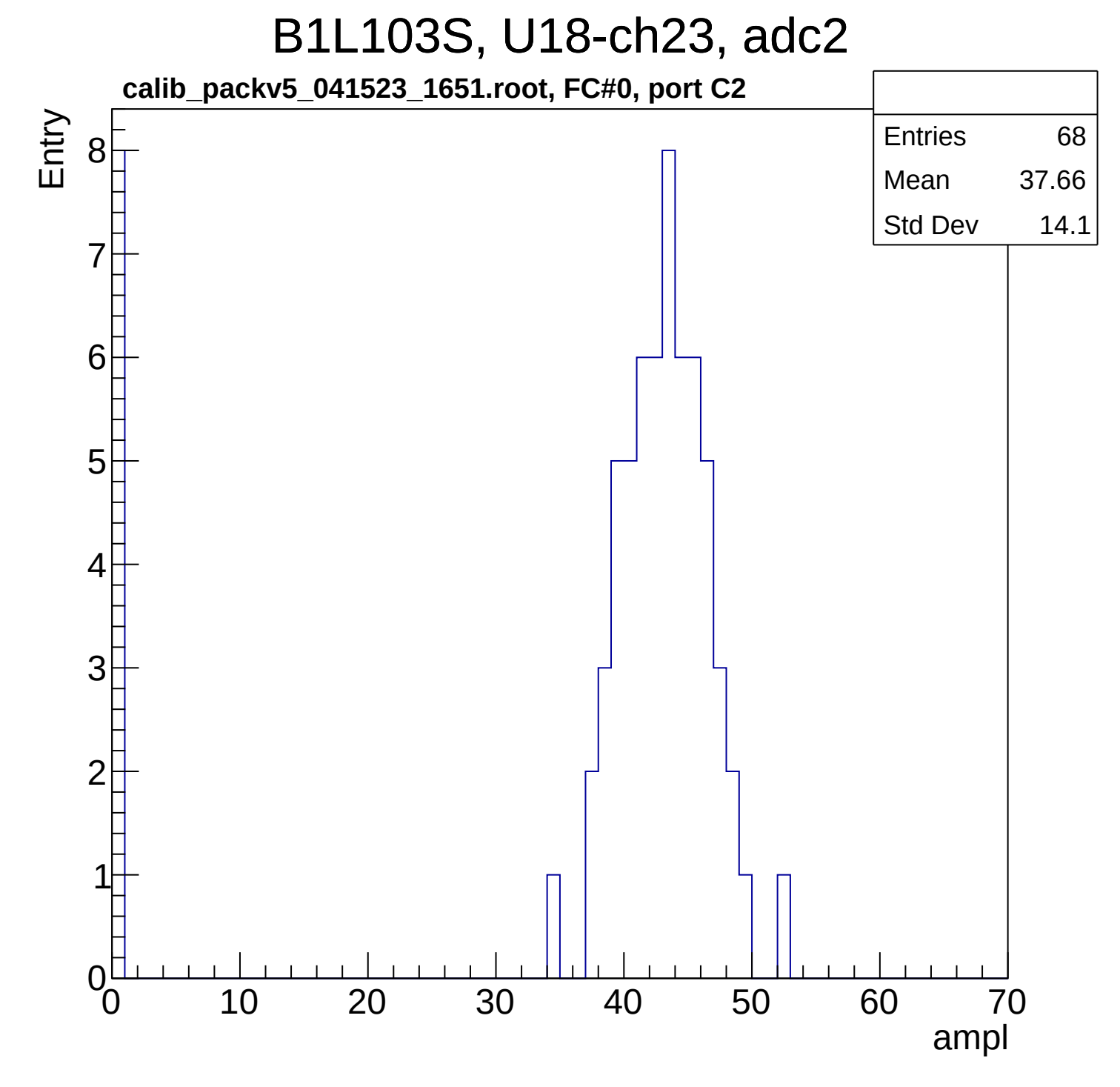
B1L103S, U18-ch23, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 37.66
Std Dev 14.1
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
30
40
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60
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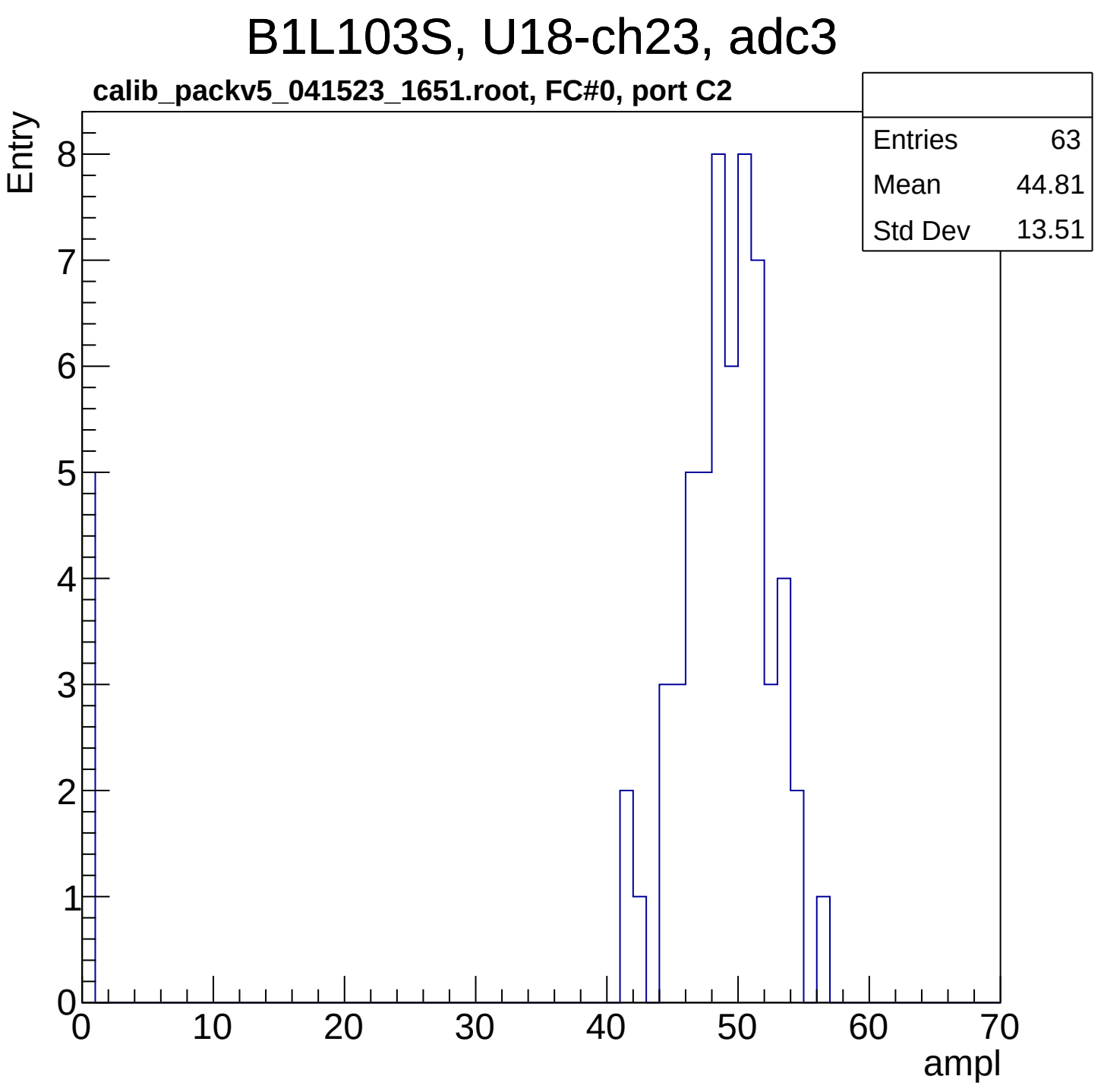
B1L103S, U18-ch23, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 44.81
Std Dev 13.51
Entry
ampl
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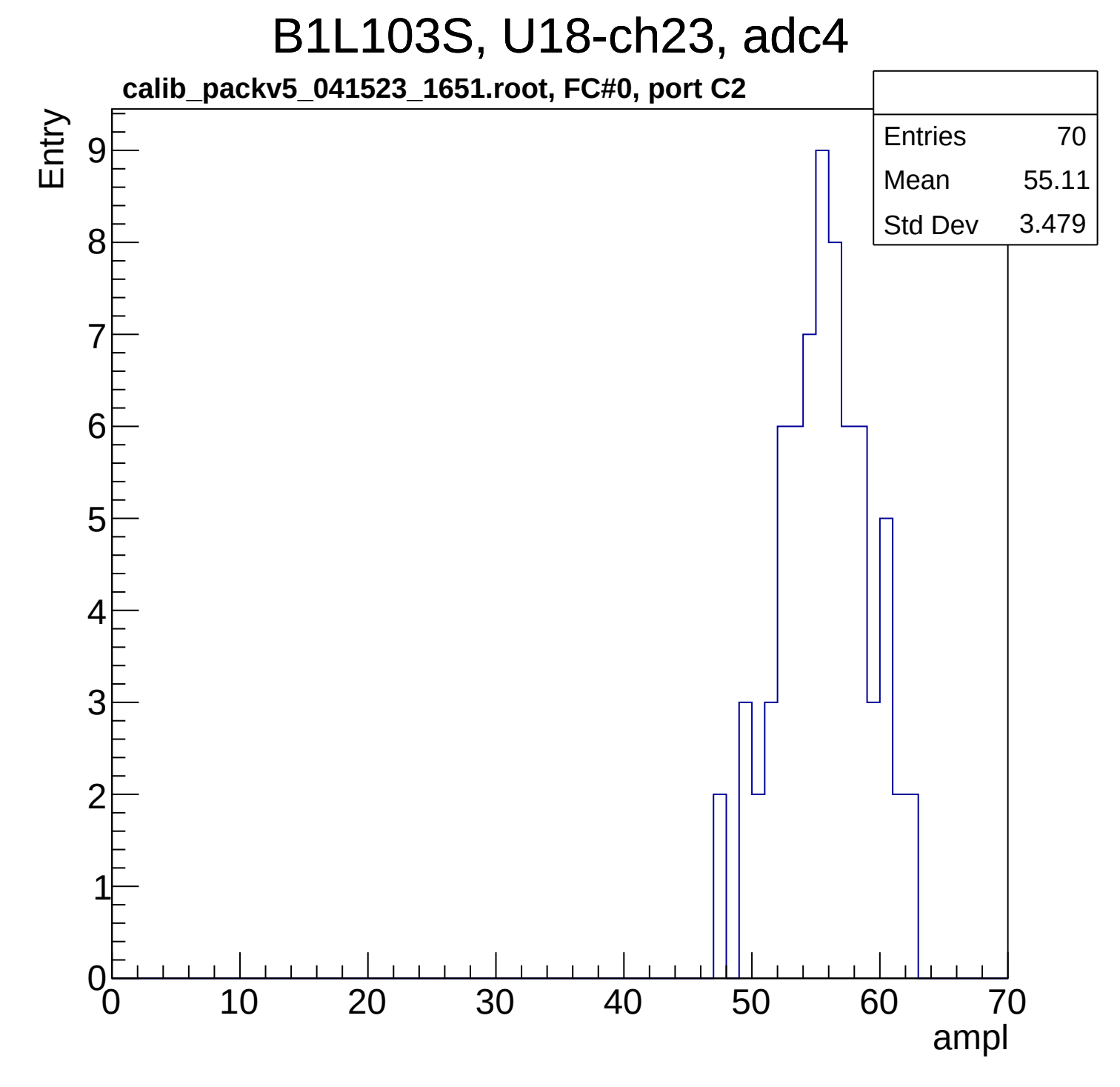
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch23, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 55.11
Std Dev 3.479
Entry
ampl
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3
4
5
6
7
8
9
0
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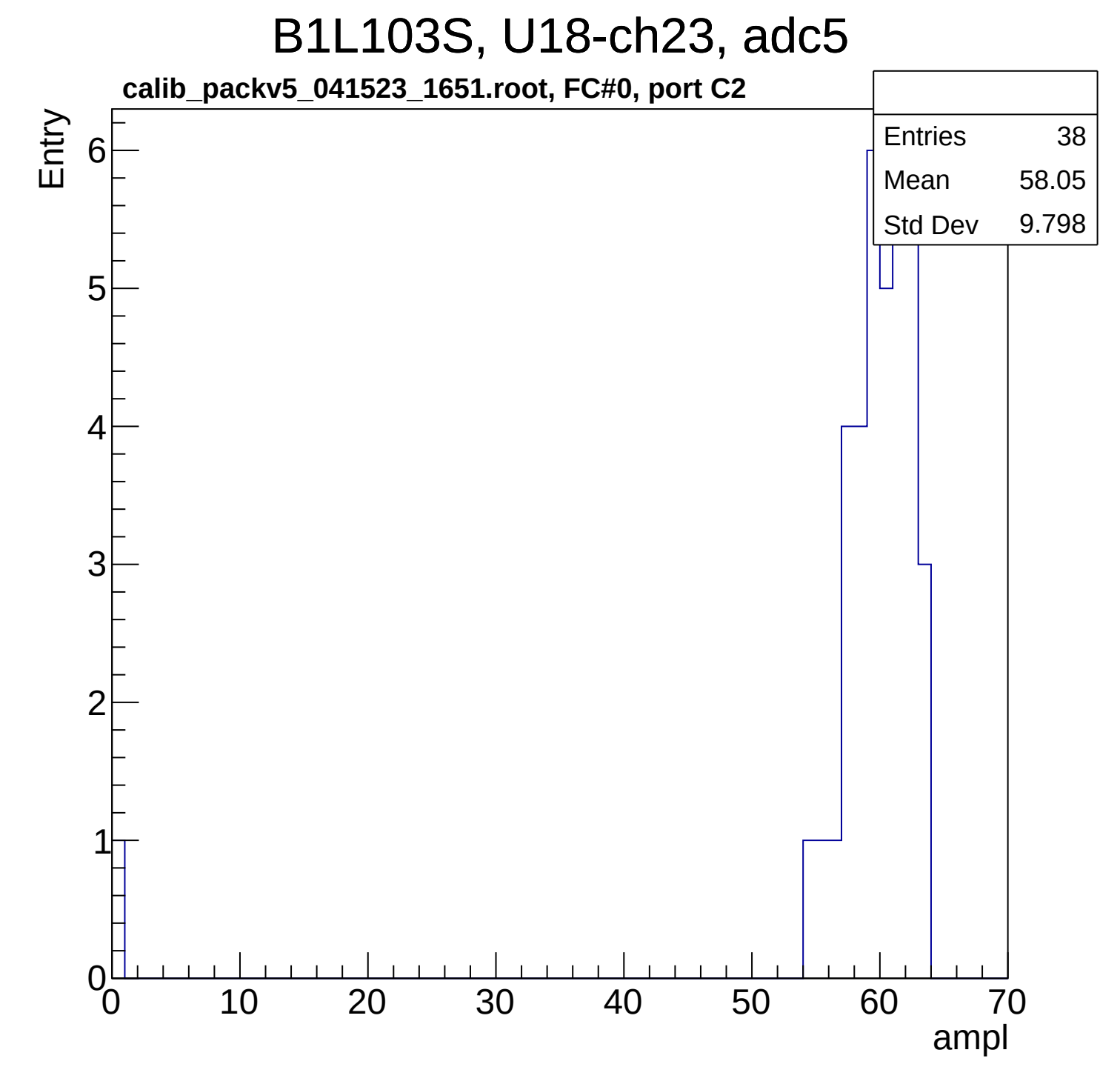
B1L103S, U18-ch23, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 38
Mean 58.05
Std Dev 9.798
Entry
ampl
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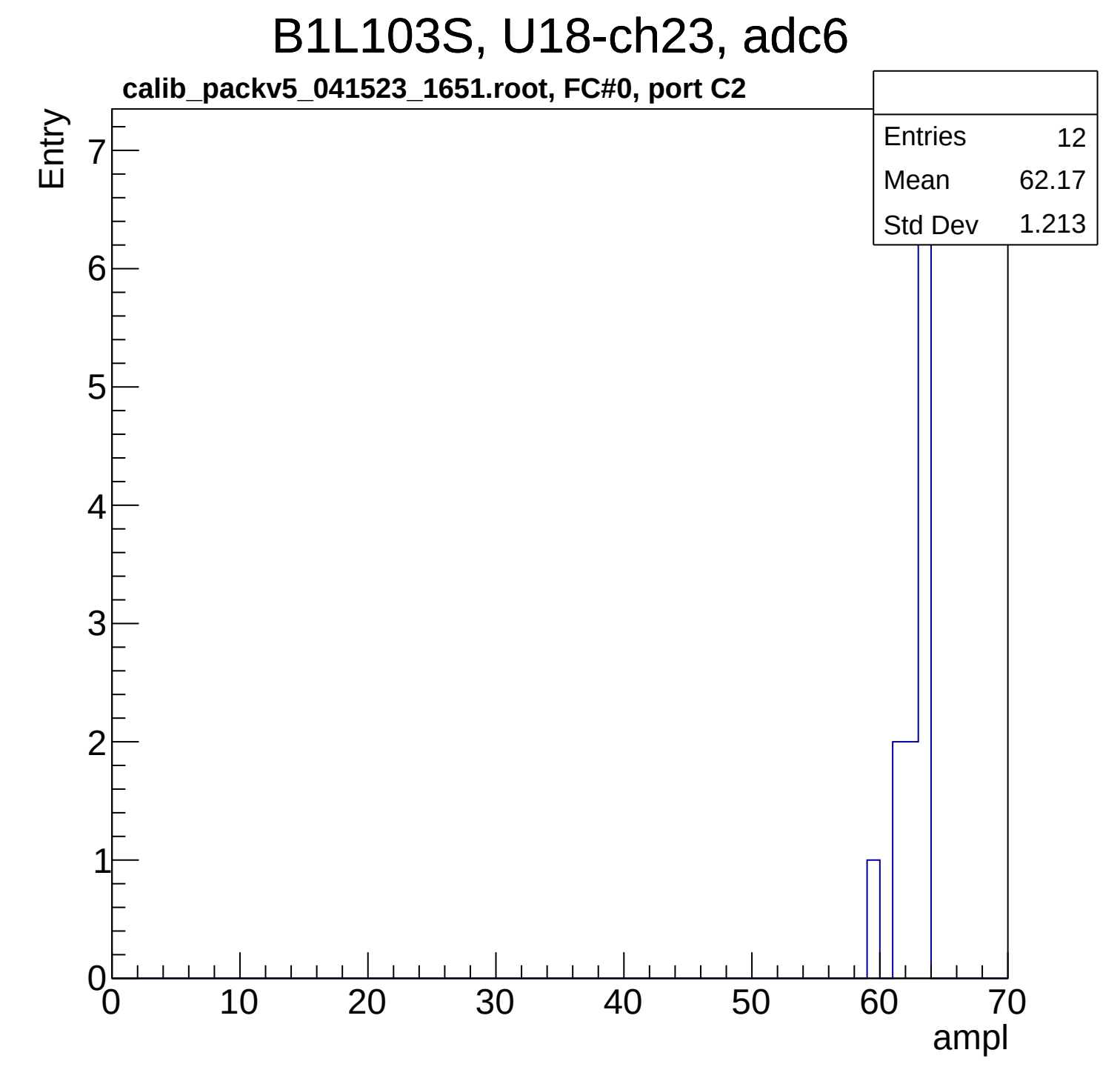
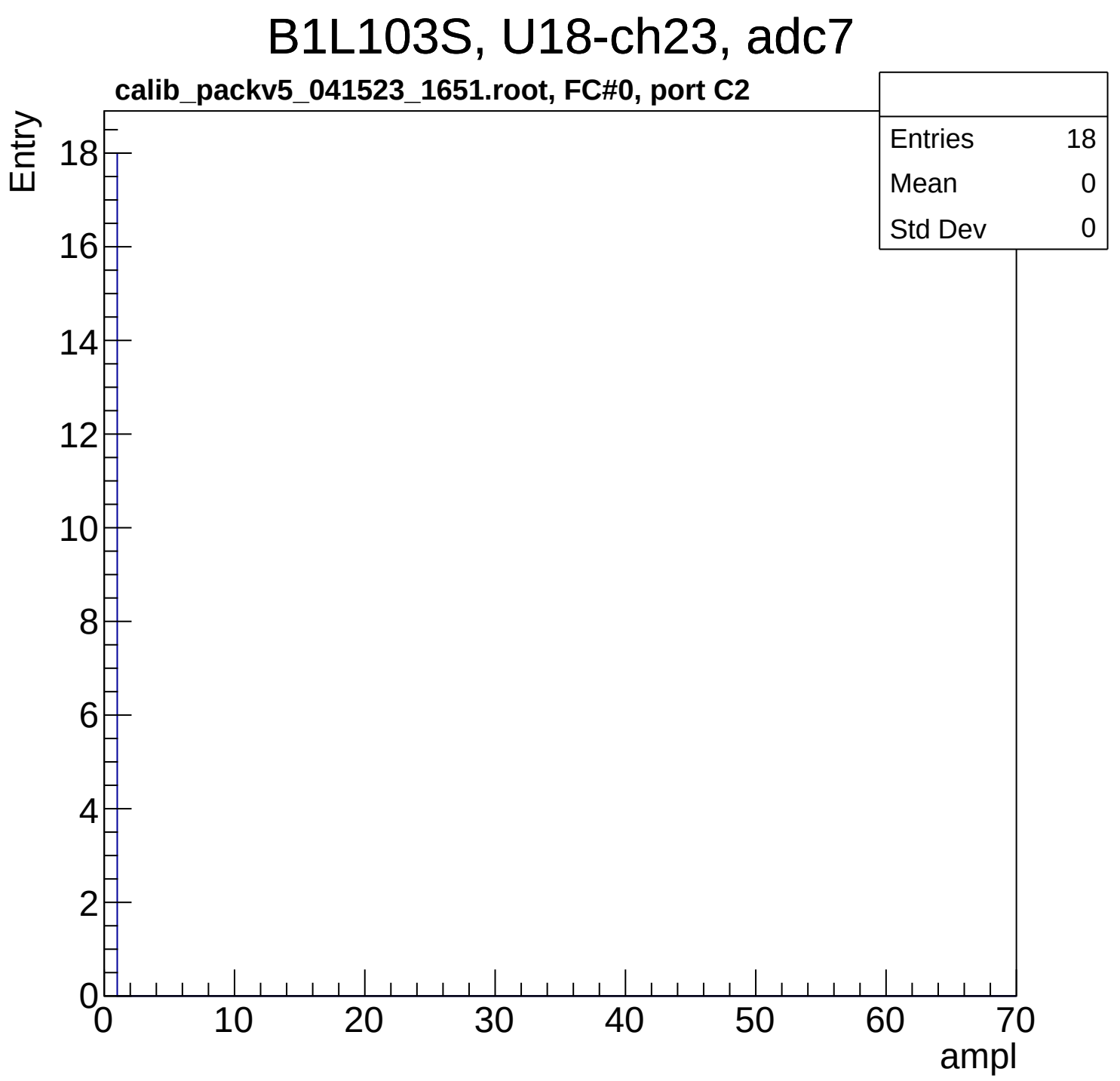
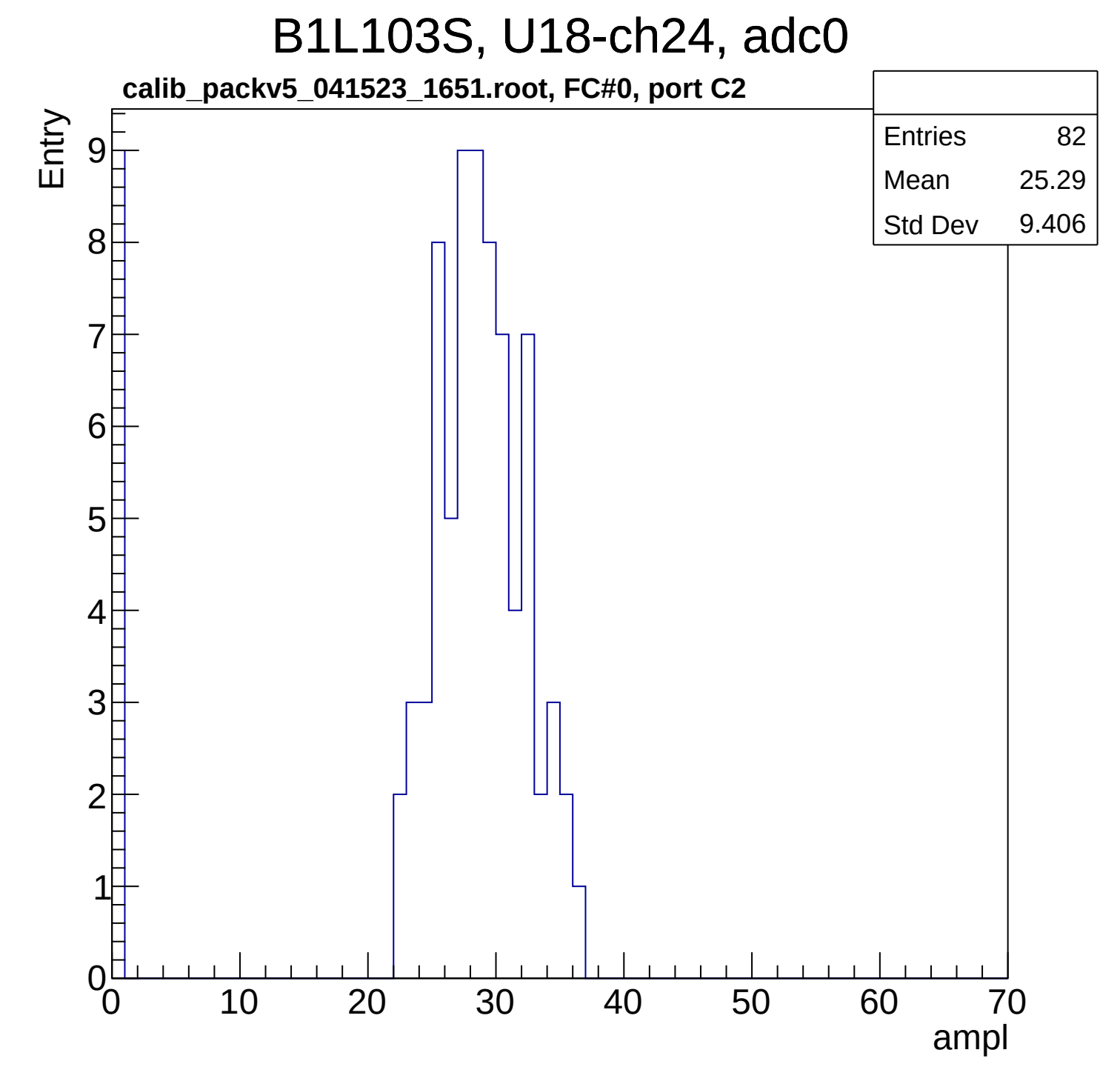
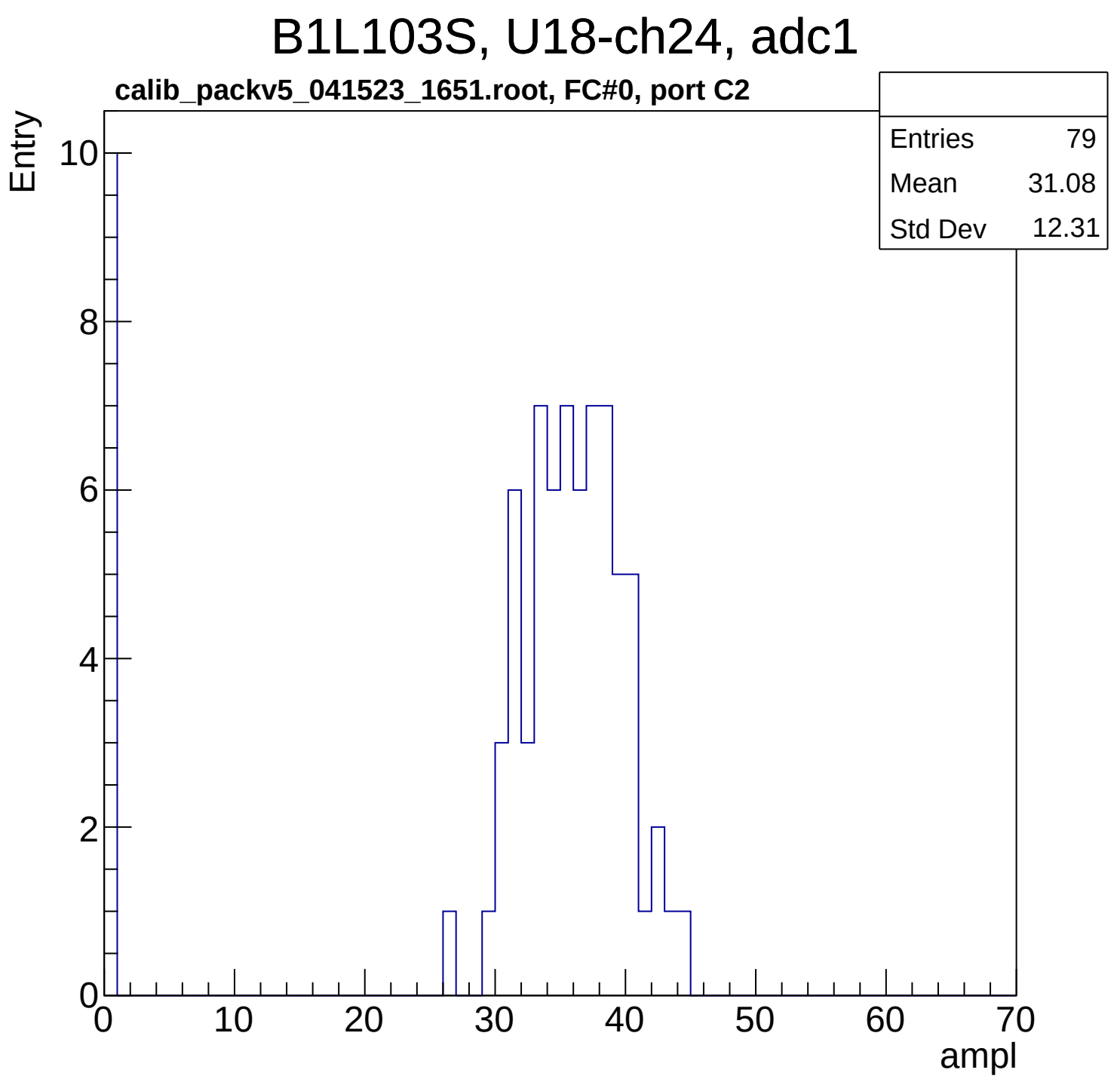
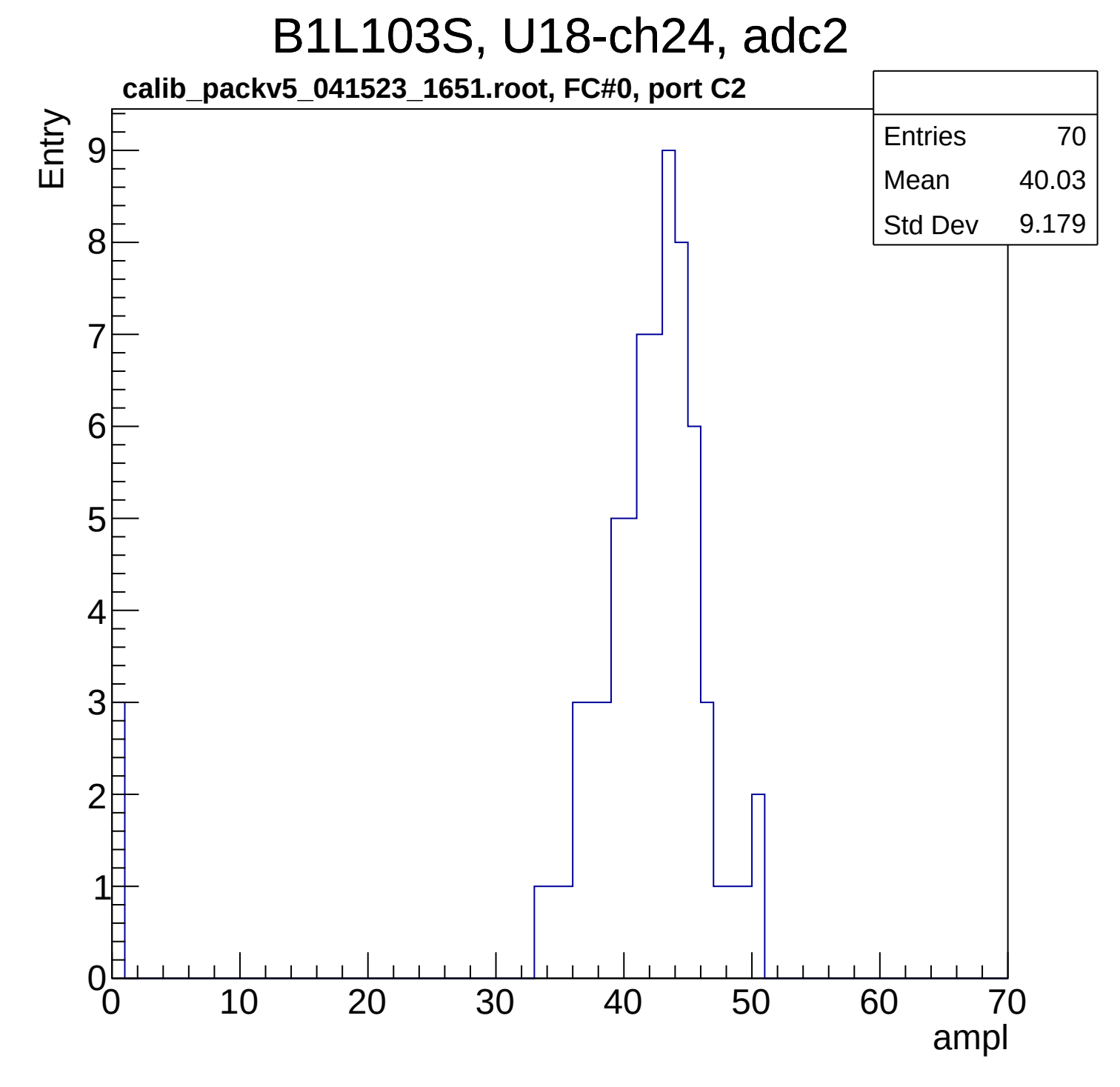
4
5
6
0
10
20
30
40
50
60
70

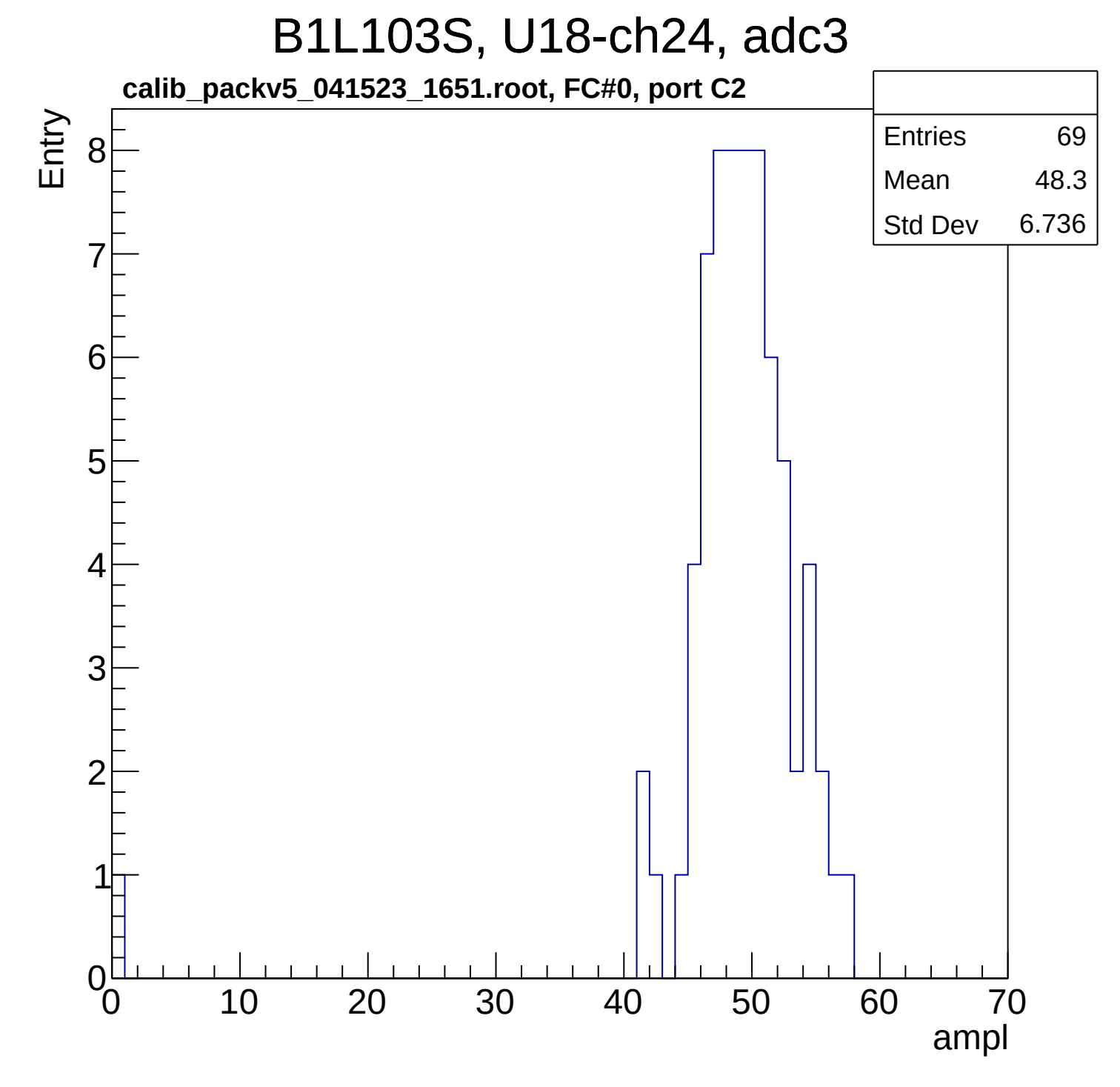

B1L103S, U18-ch23, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 62.17
Std Dev 1.213
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

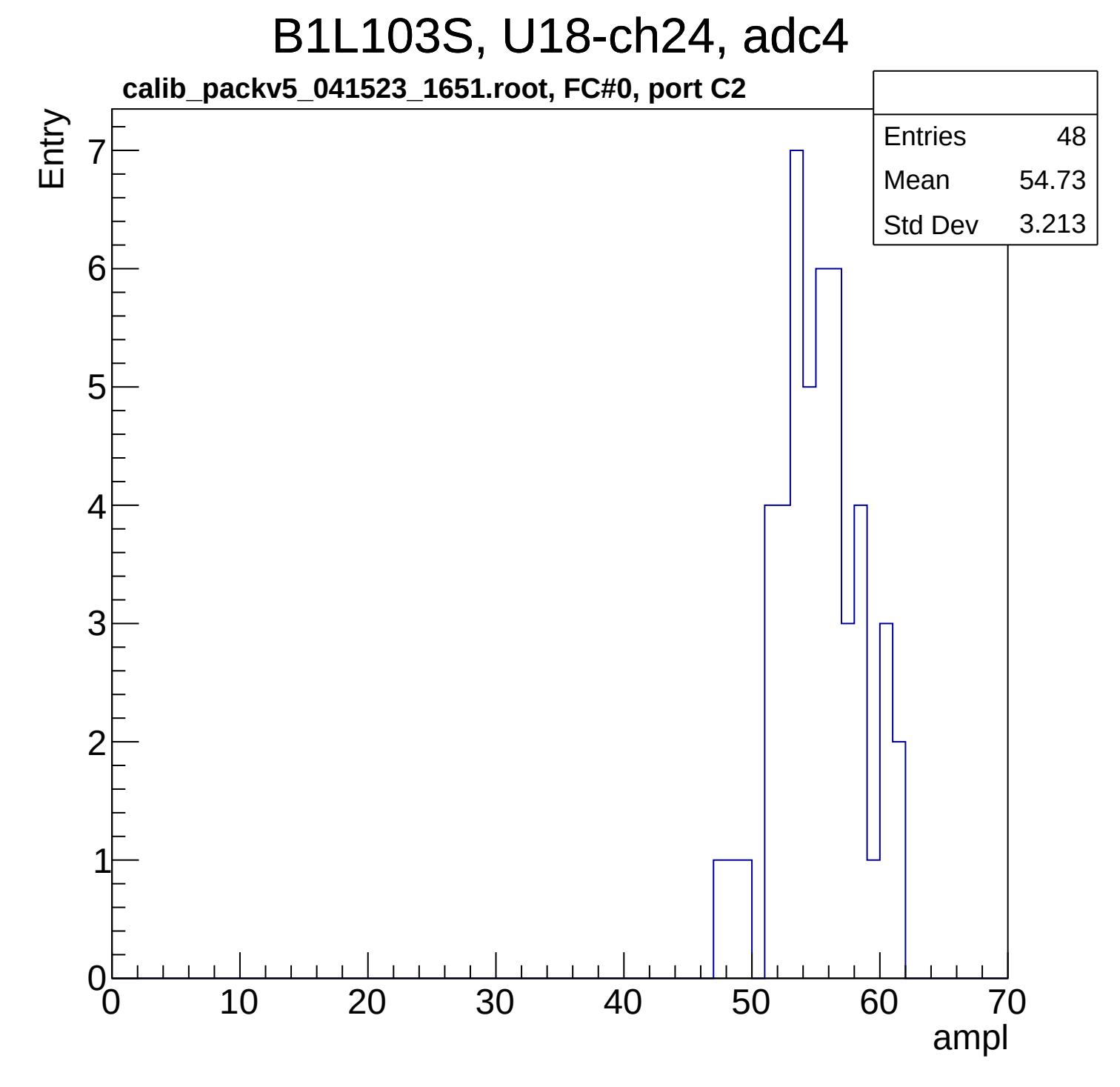

B1L103S, U18-ch23, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

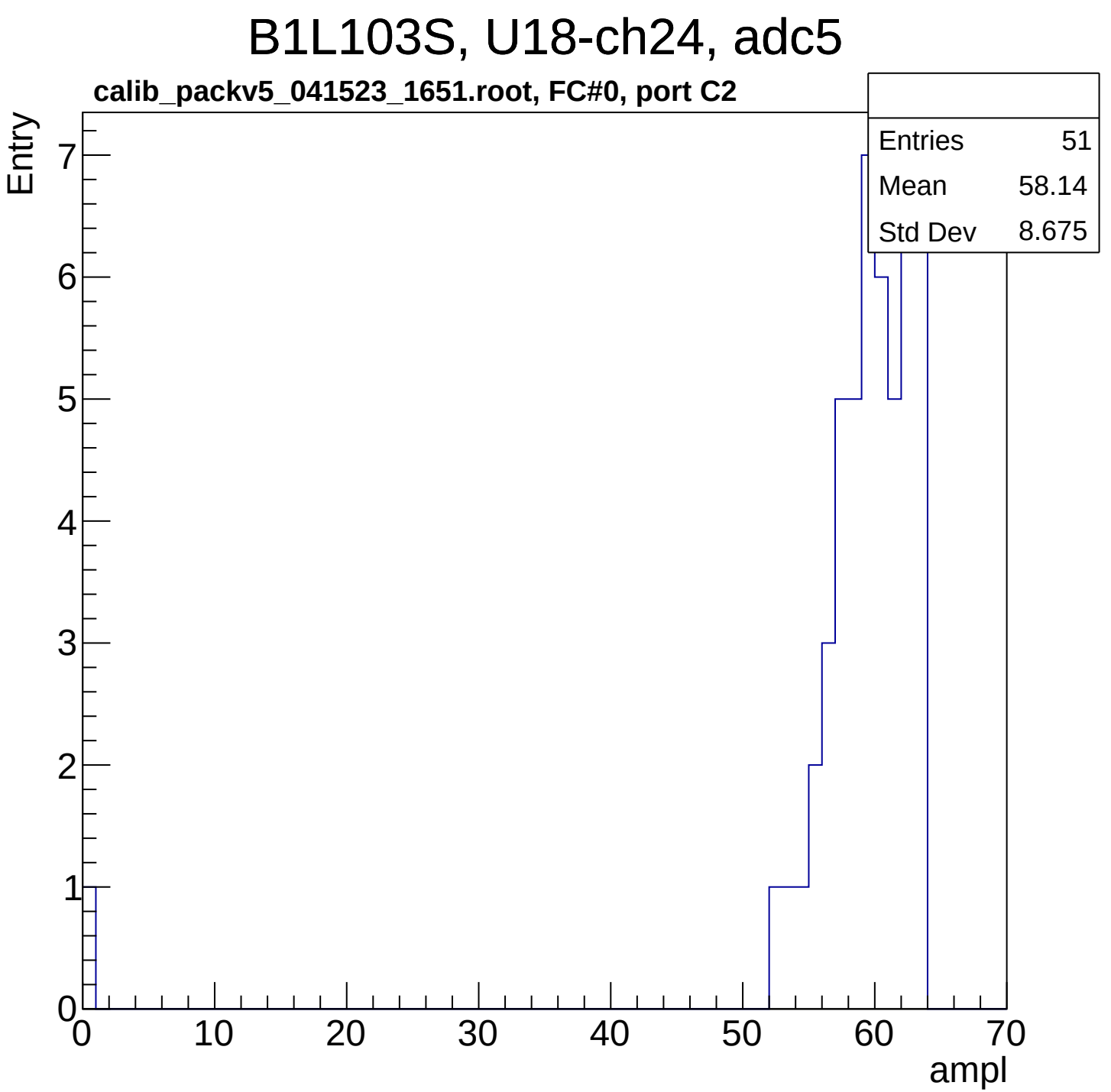

B1L103S, U18-ch24, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 25.29
Std Dev 9.406
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

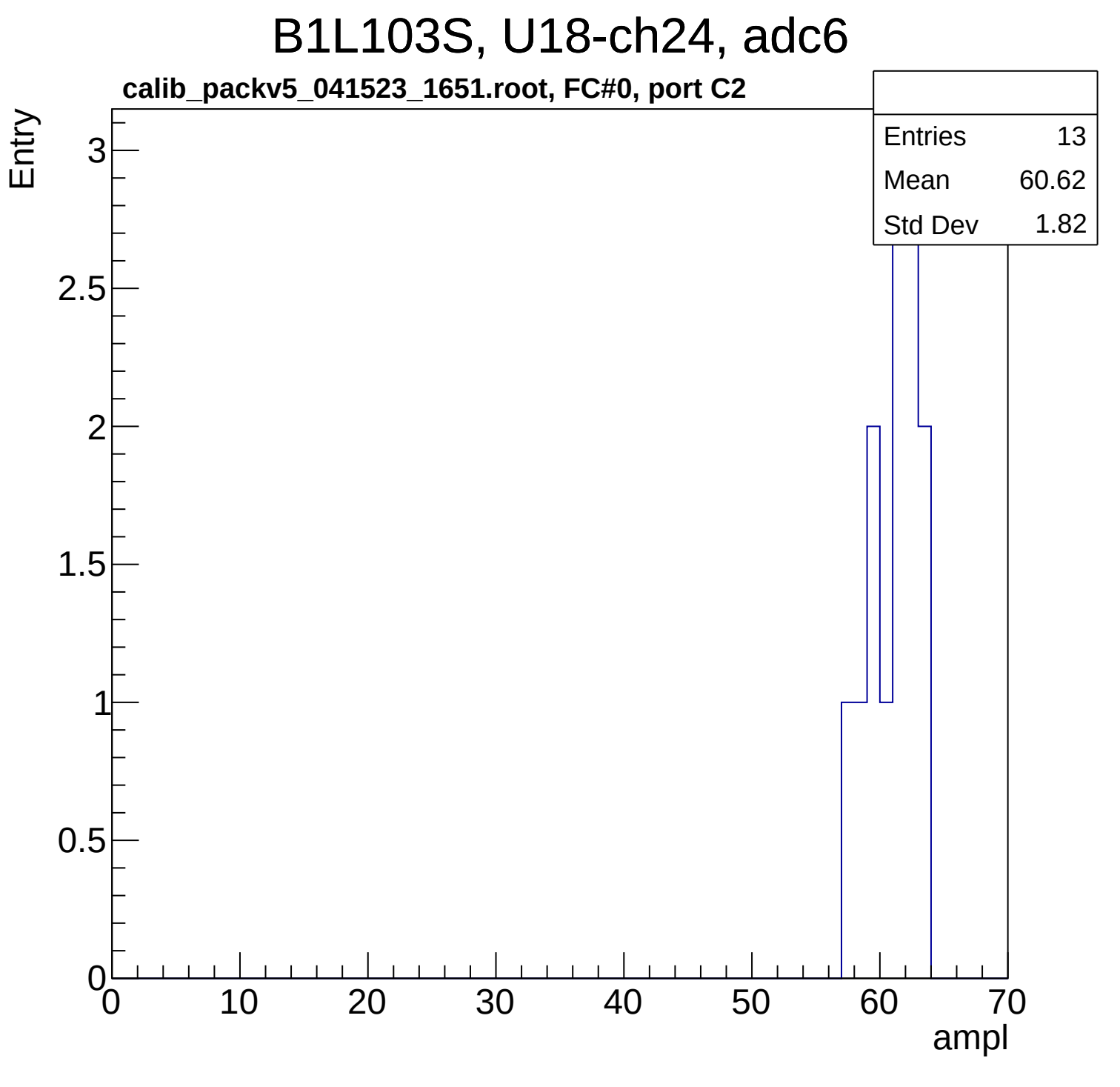

B1L103S, U18-ch24, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 31.08
Std Dev 12.31
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

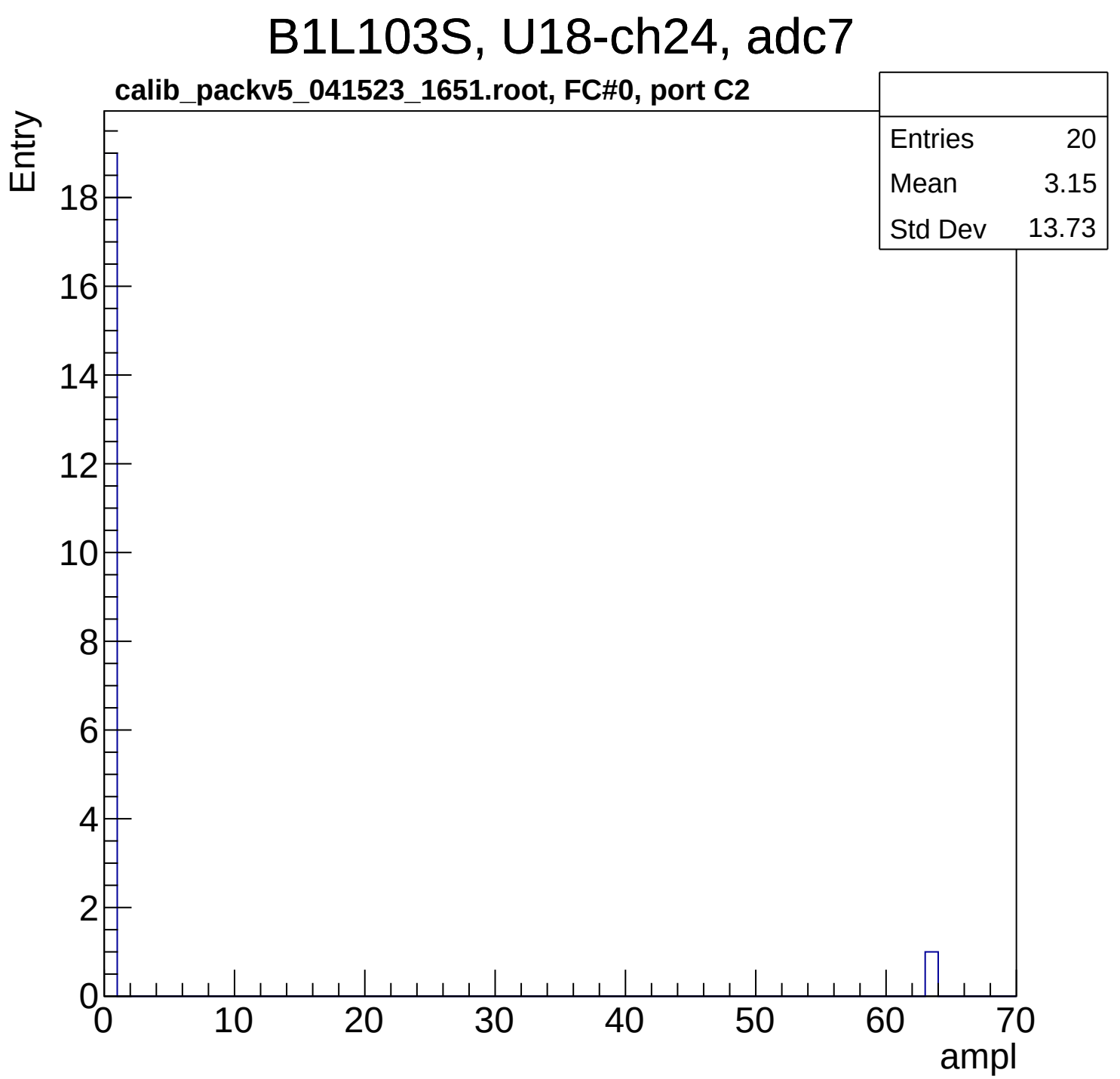

B1L103S, U18-ch24, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 40.03
Std Dev 9.179
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

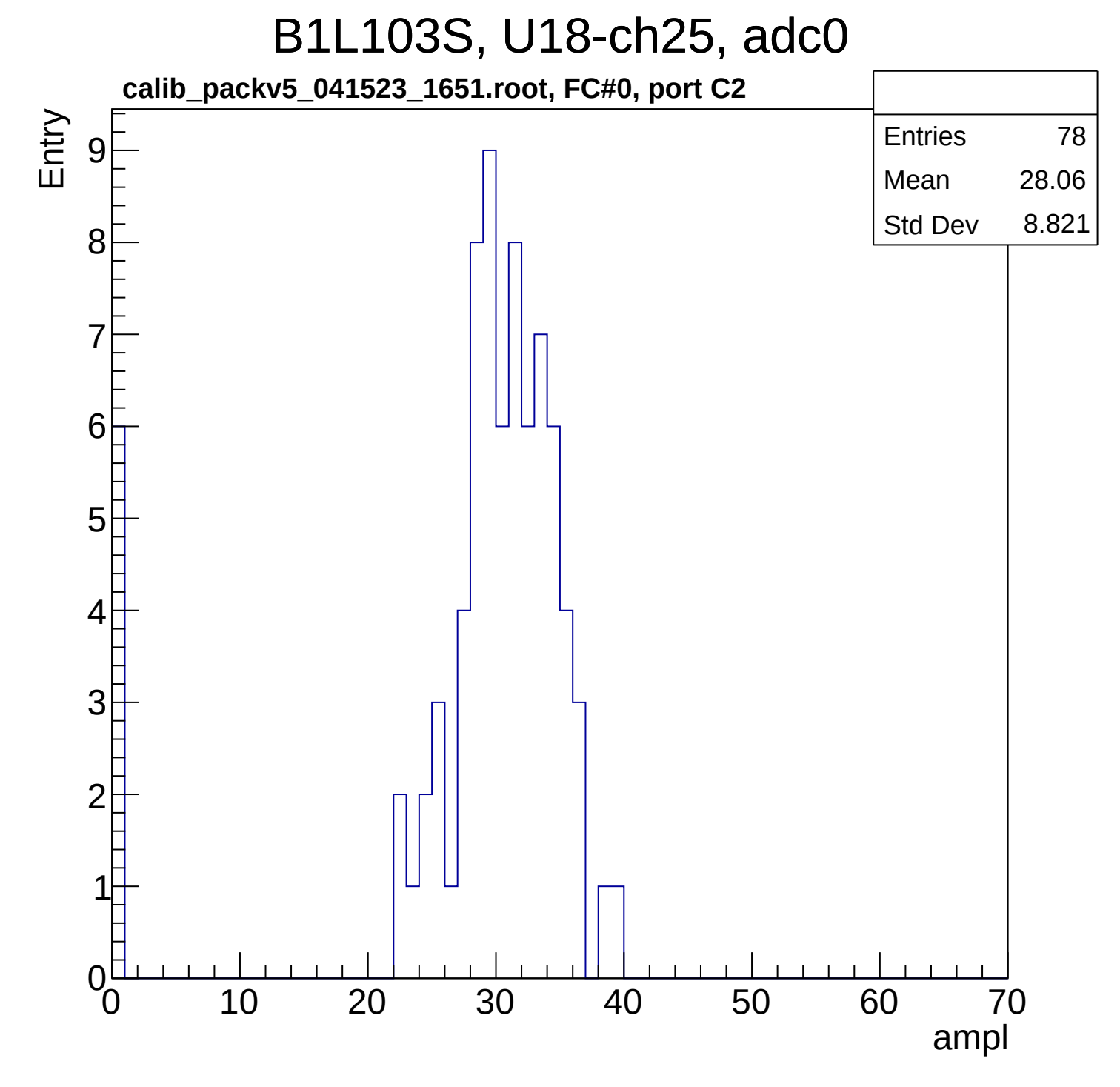

B1L103S, U18-ch24, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 48.3
Std Dev 6.736
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

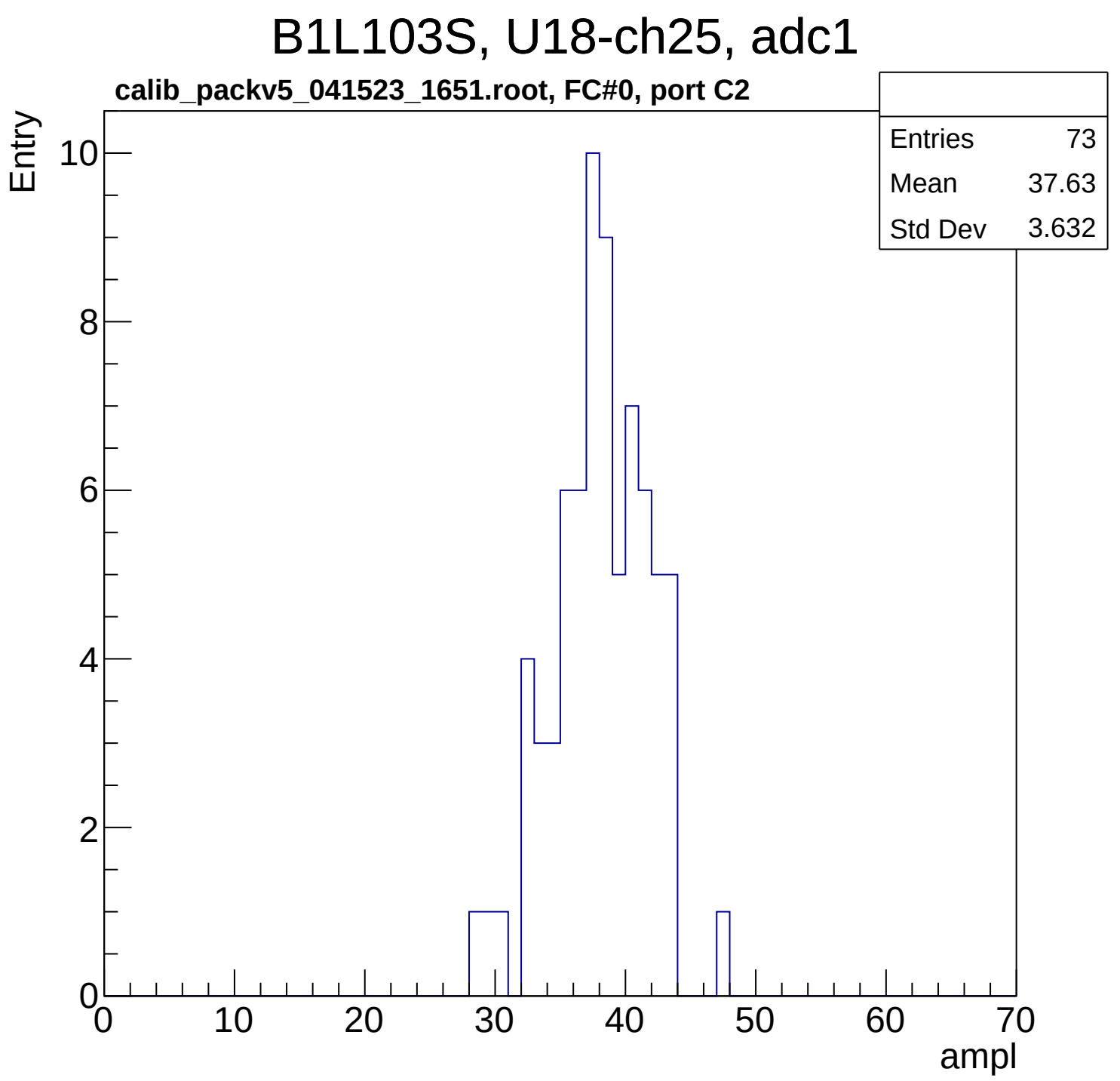

B1L103S, U18-ch24, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 54.73
Std Dev 3.213
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

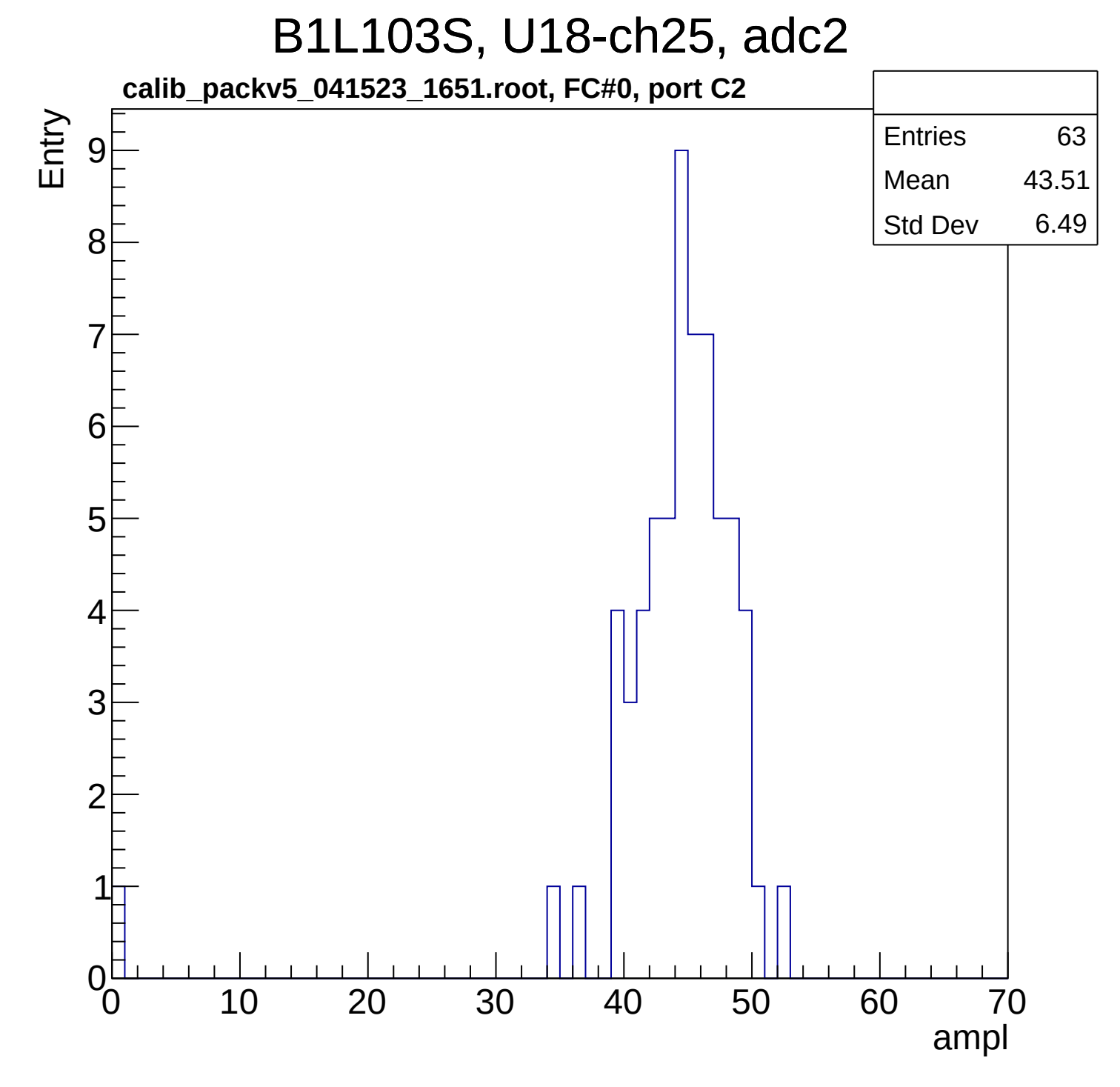

B1L103S, U18-ch24, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 58.14
Std Dev 8.675
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

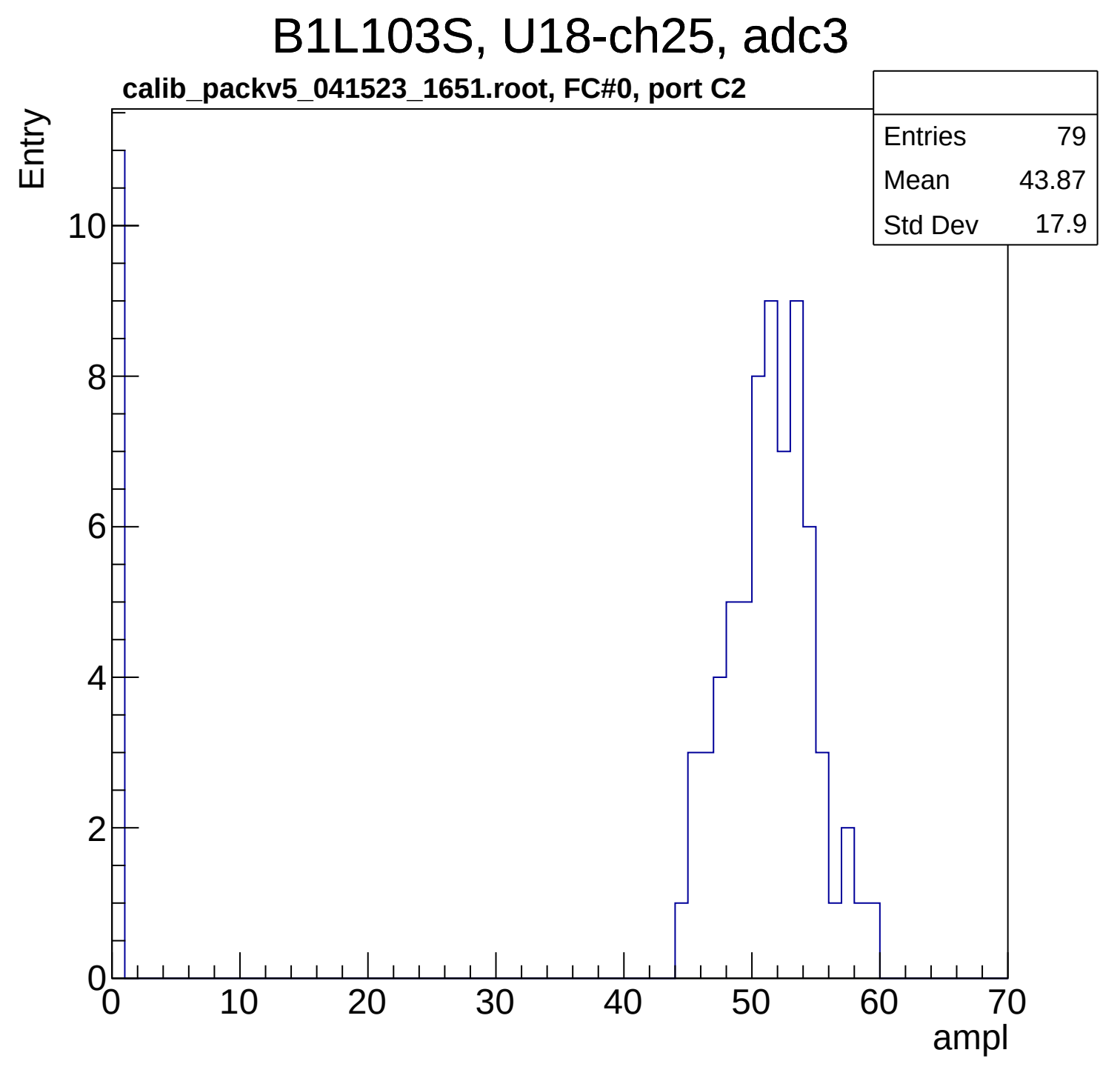

B1L103S, U18-ch24, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 13
Mean 60.62
Std Dev 1.82
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

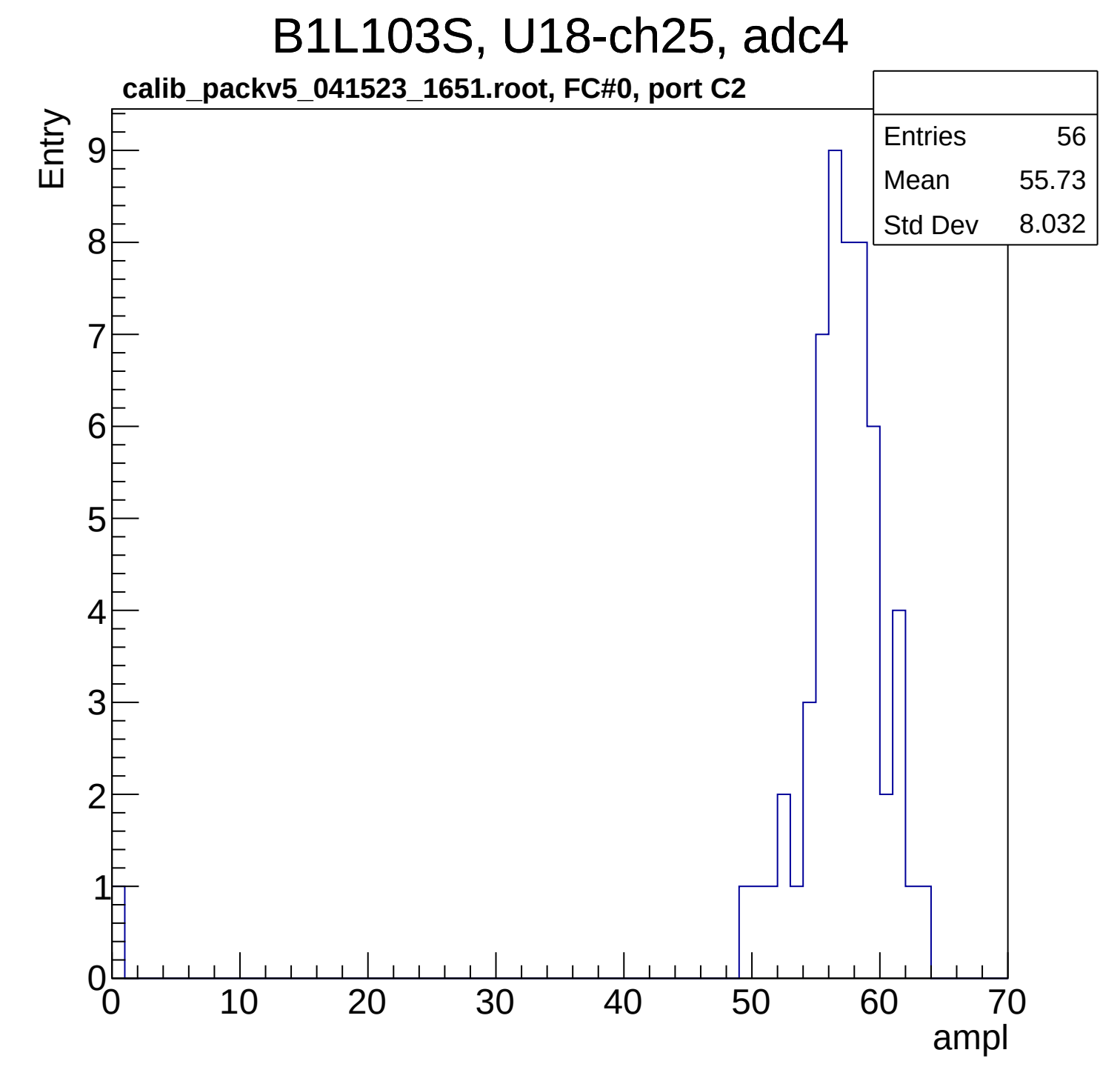

B1L103S, U18-ch24, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

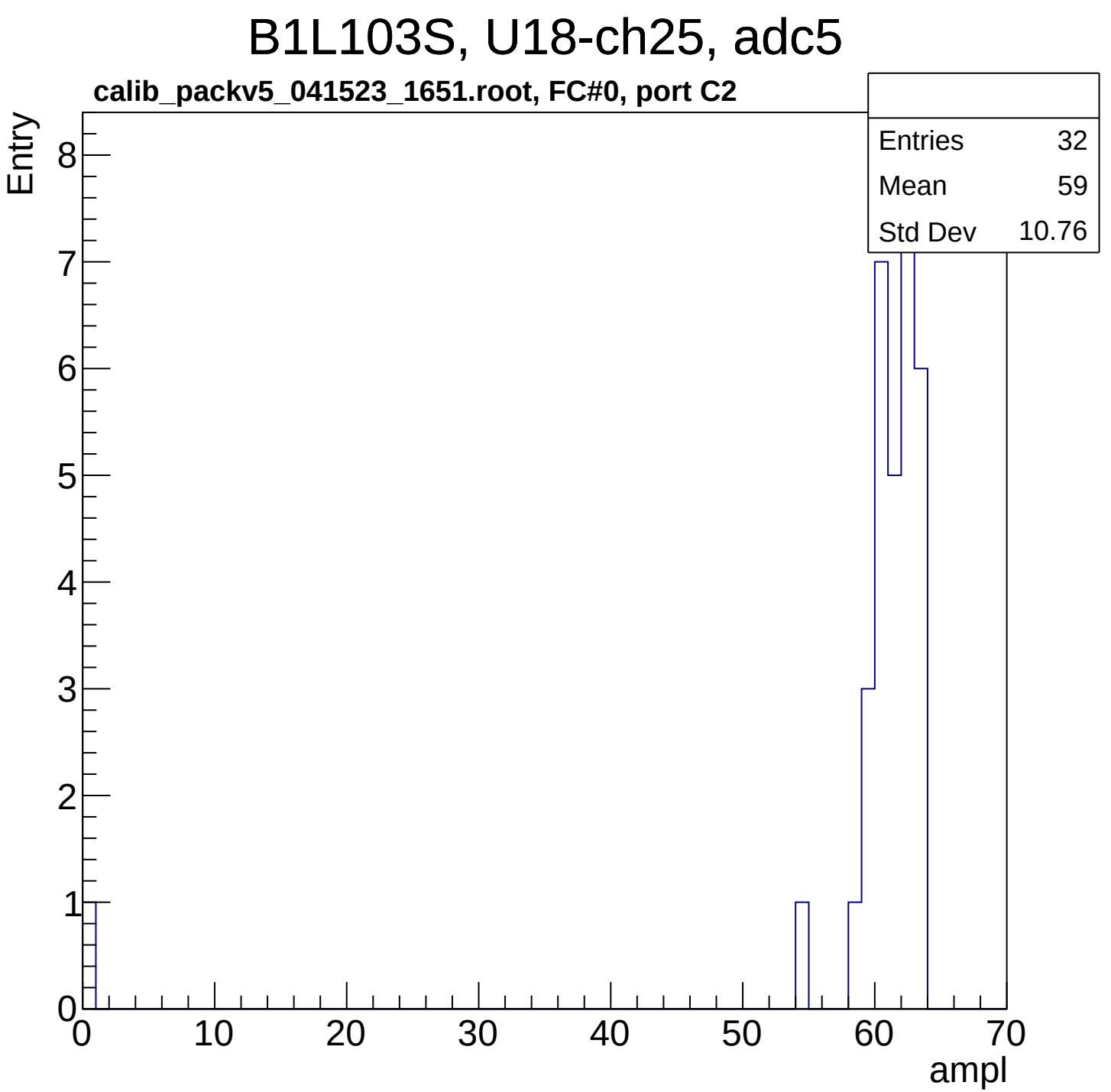

B1L103S, U18-ch25, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 28.06
Std Dev 8.821
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

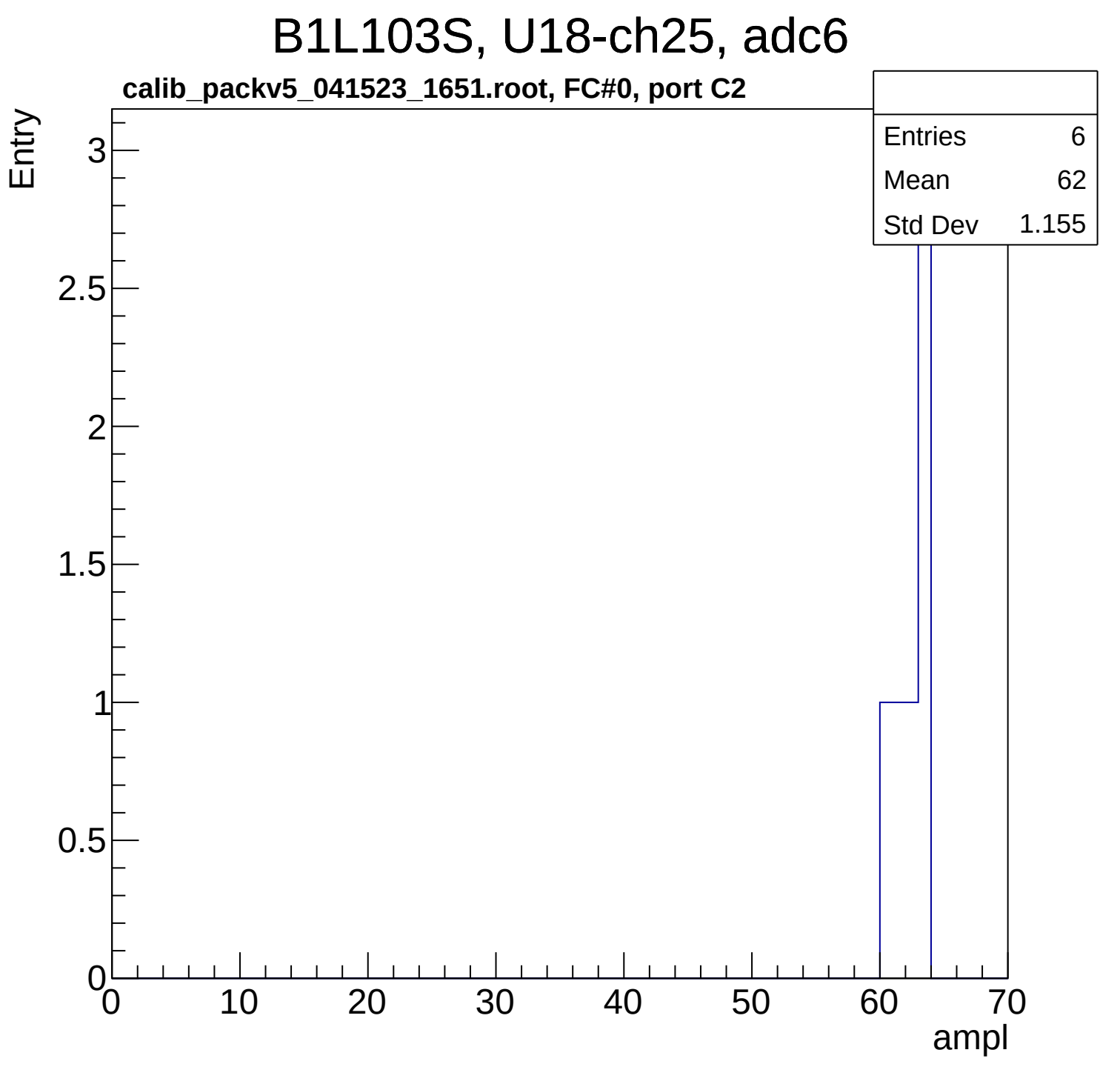

B1L103S, U18-ch25, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 37.63
Std Dev 3.632
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U18-ch25, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 43.51
Std Dev 6.49
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U18-ch25, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 43.87
Std Dev 17.9
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch25, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 55.73
Std Dev 8.032
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U18-ch25, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 32
Mean 59
Std Dev 10.76
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch25, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 62
Std Dev 1.155
Entry
ampl
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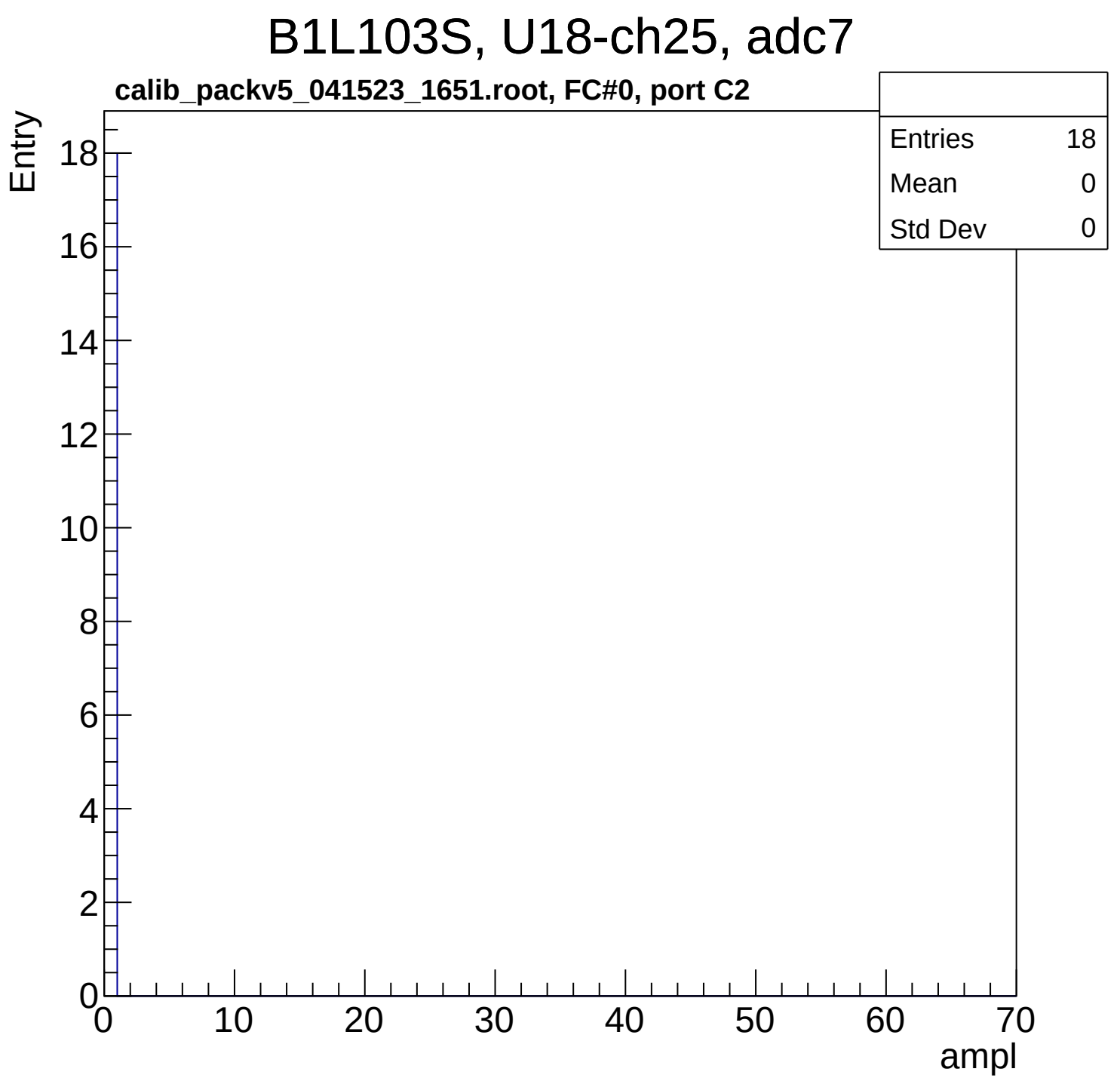
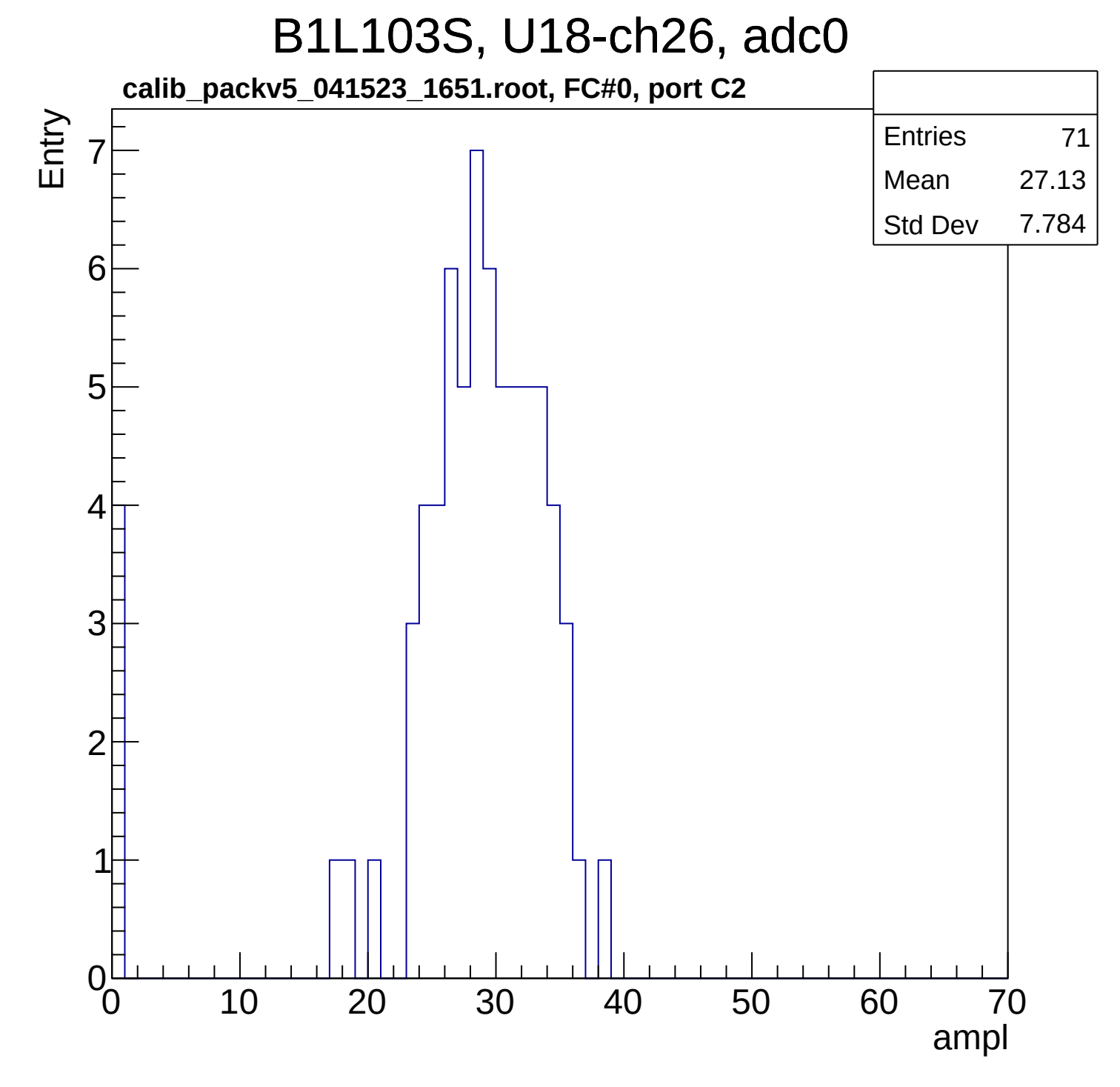
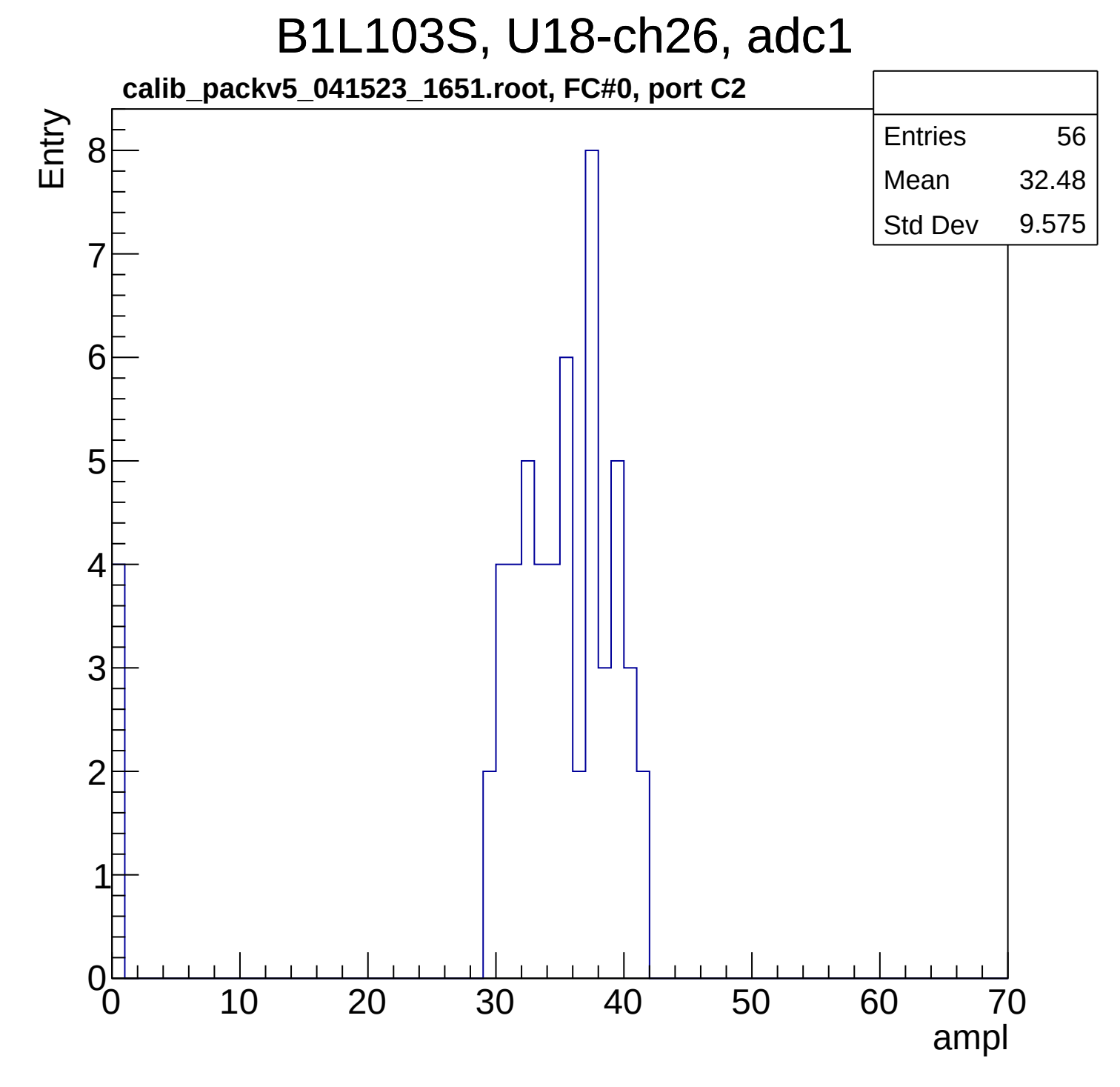
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U18-ch25, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch26, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 27.13
Std Dev 7.784
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U18-ch26, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 32.48
Std Dev 9.575
Entry
ampl
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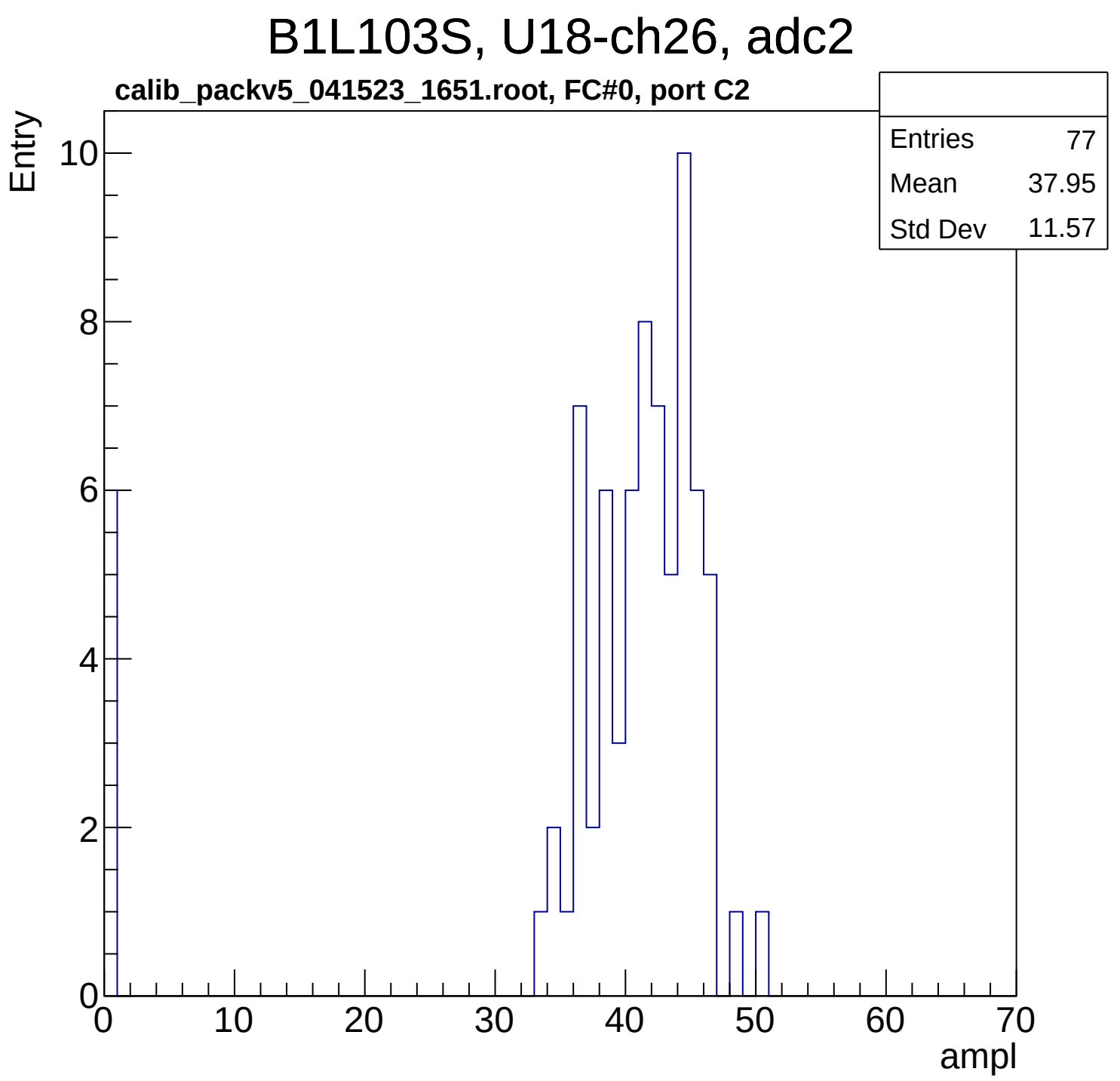
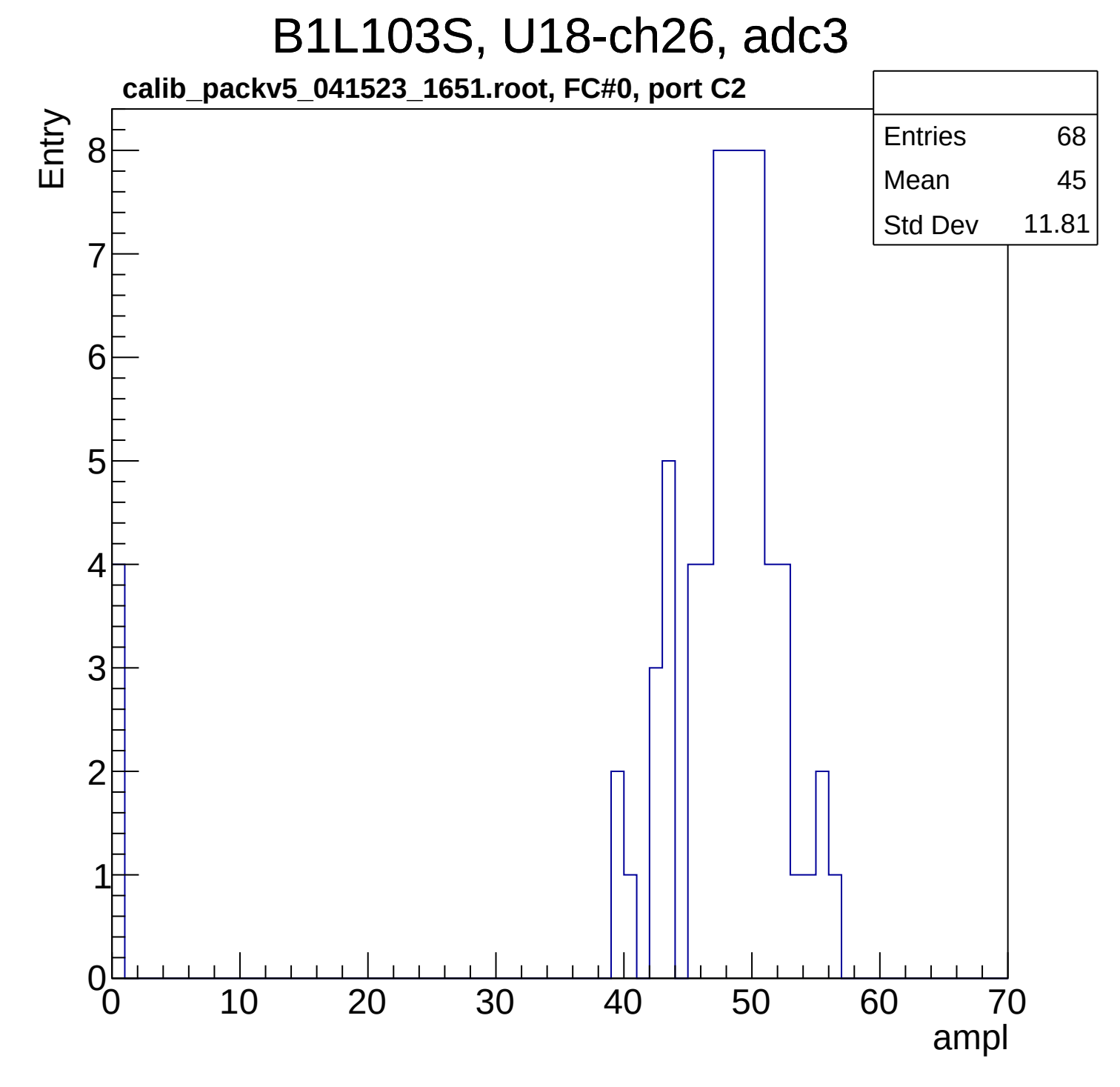
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch26, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 37.95
Std Dev 11.57
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U18-ch26, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 45
Std Dev 11.81
Entry
ampl
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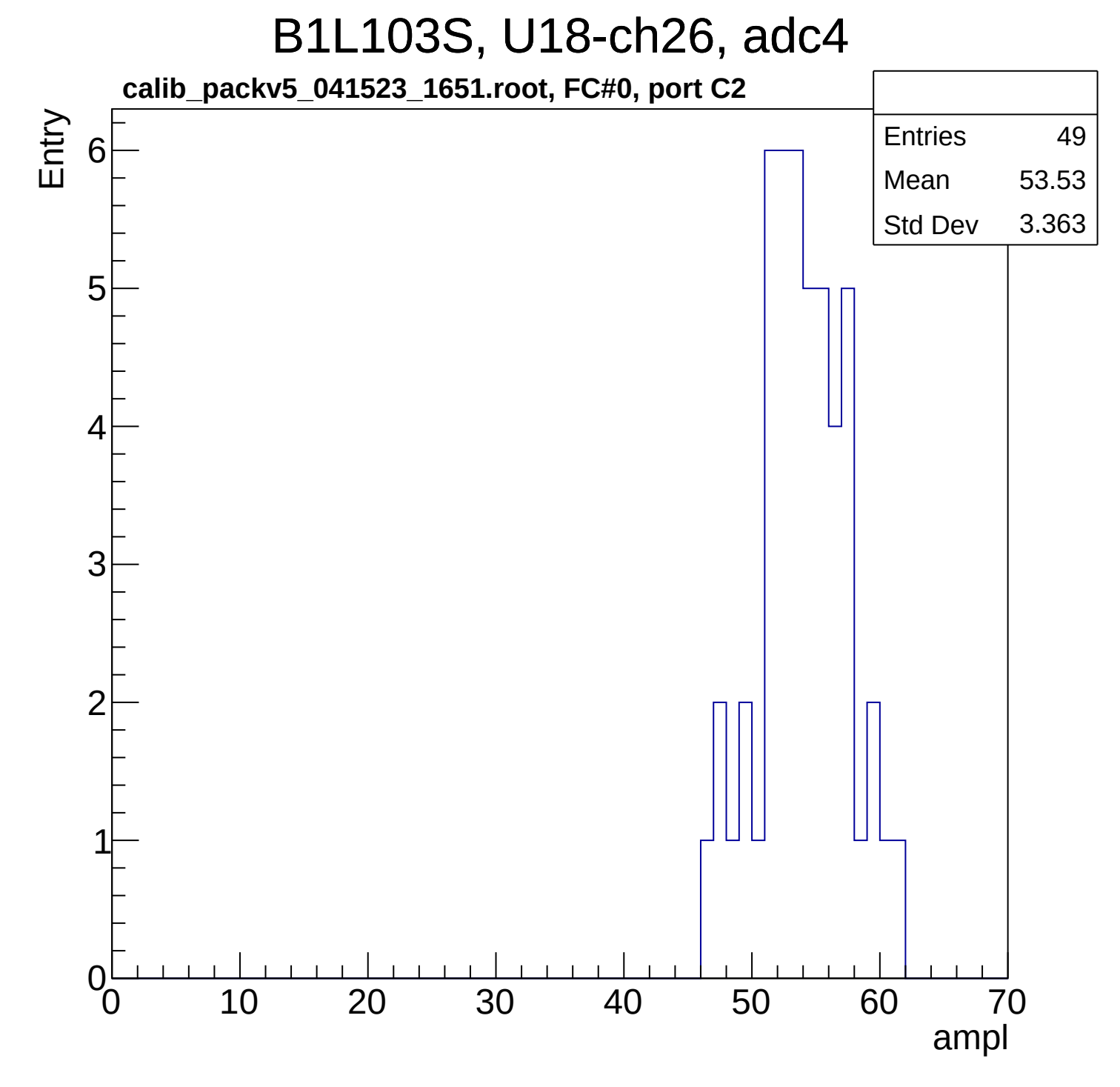
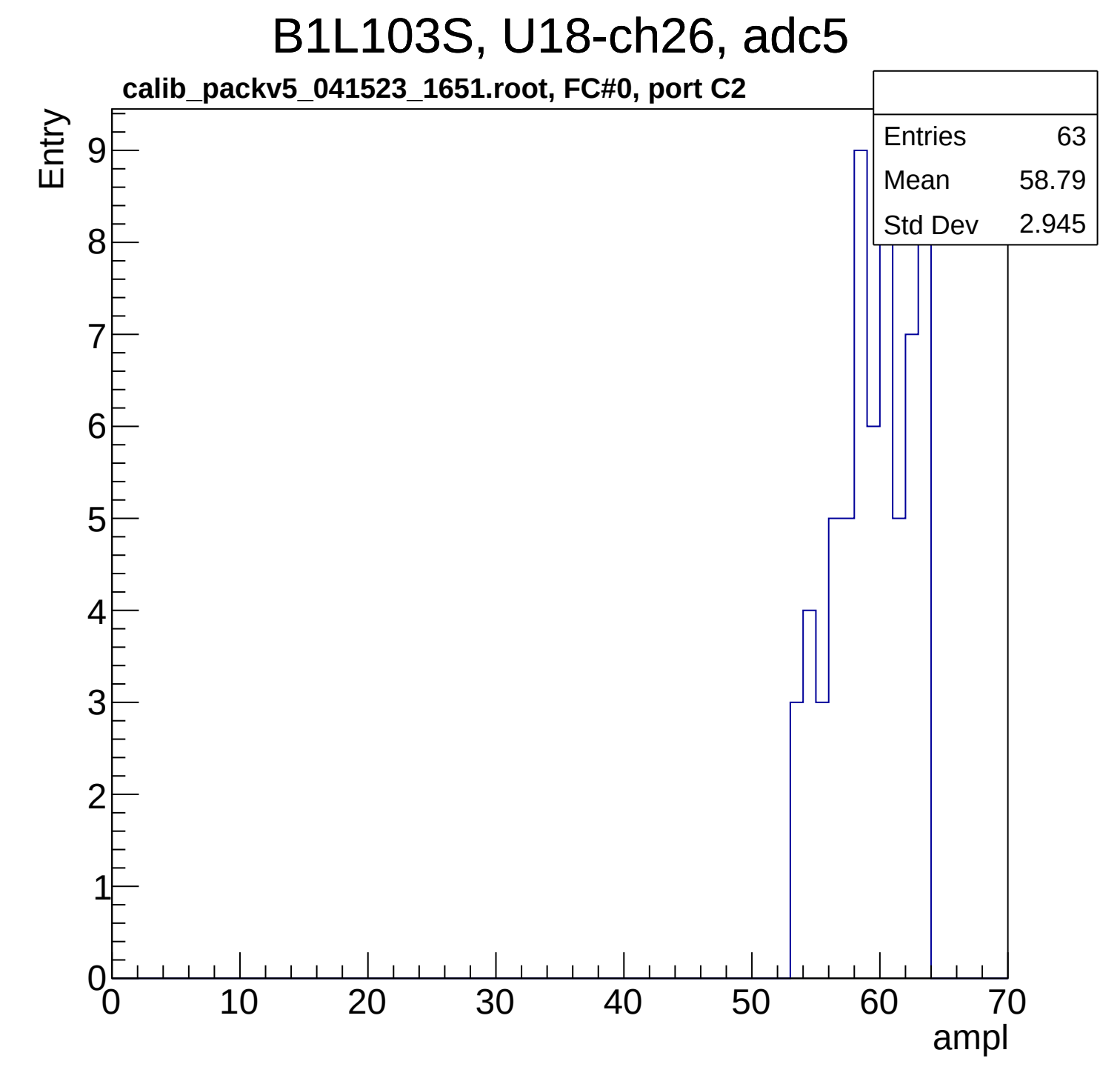
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch26, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 53.53
Std Dev 3.363
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U18-ch26, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 58.79
Std Dev 2.945
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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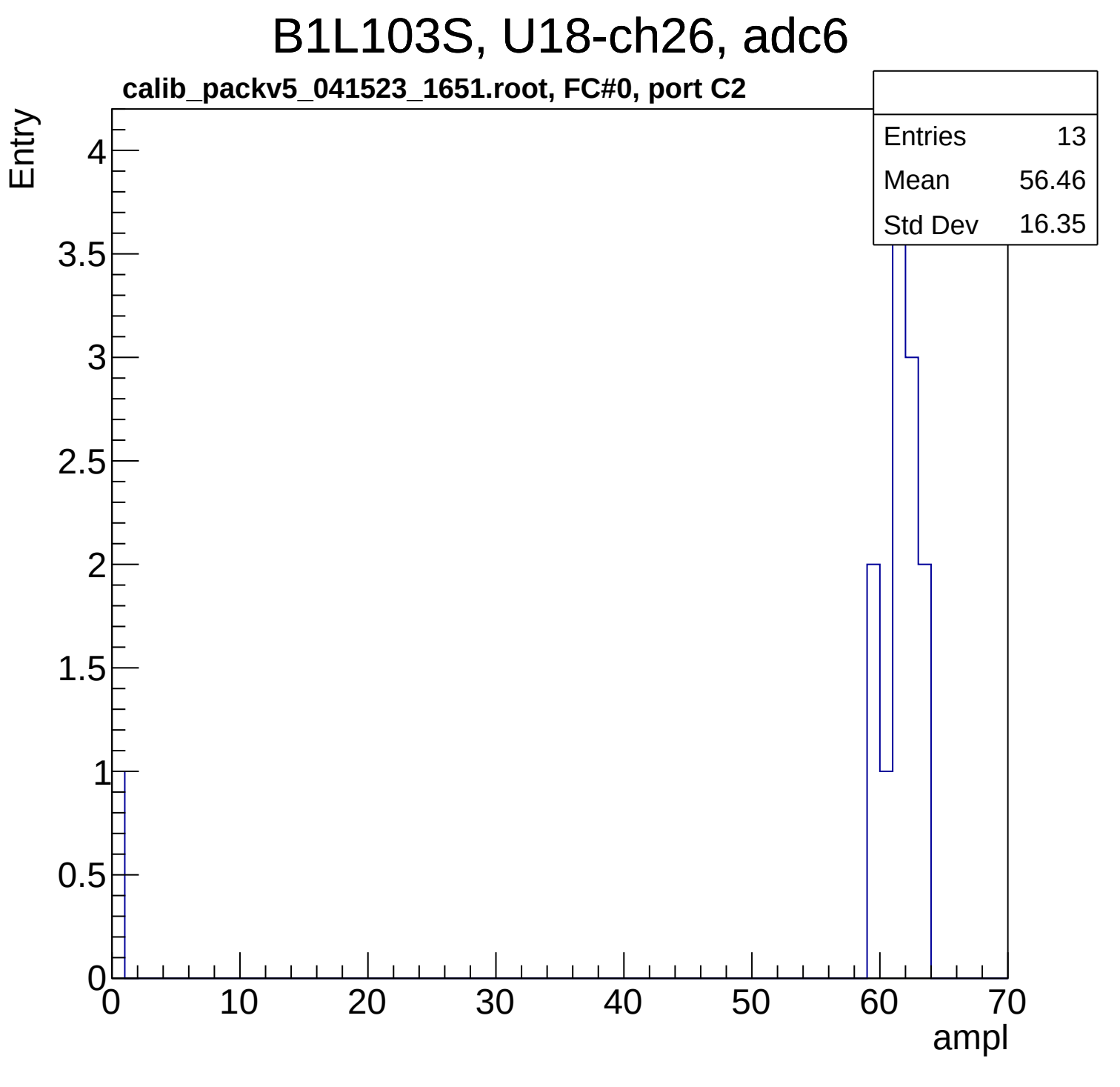
60
70


B1L103S, U18-ch26, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 13
Mean 56.46
Std Dev 16.35
Entry
ampl
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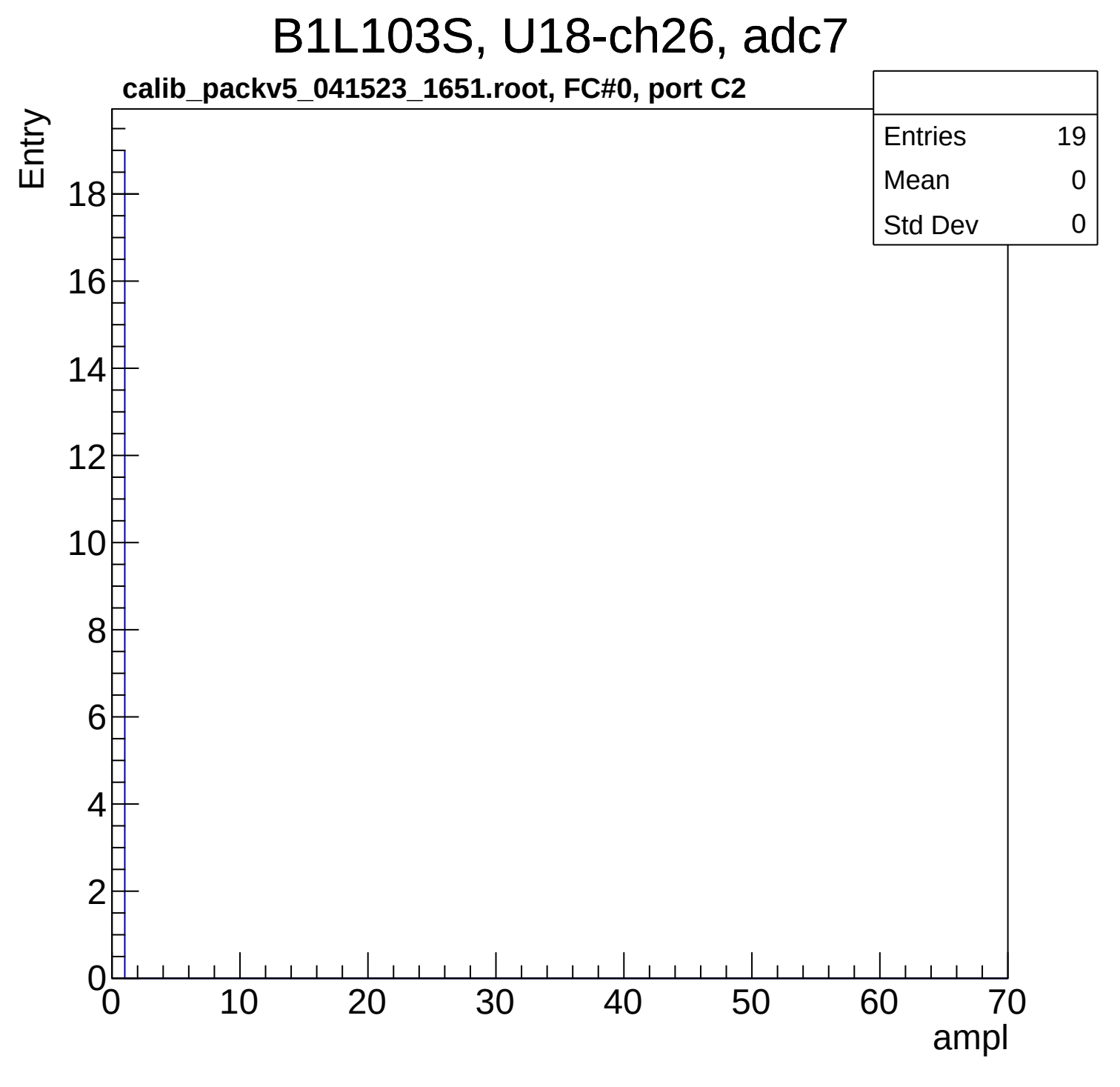
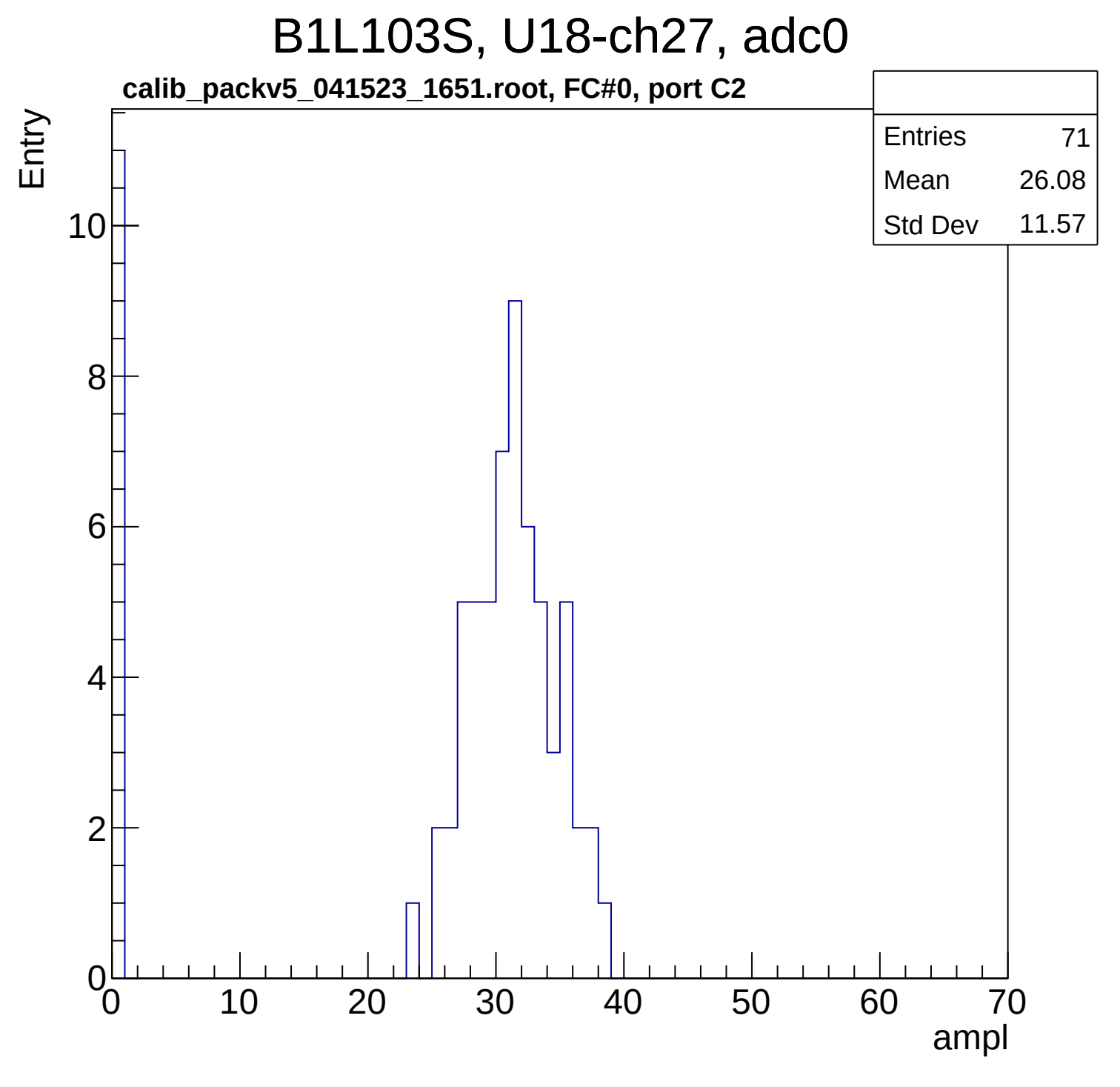
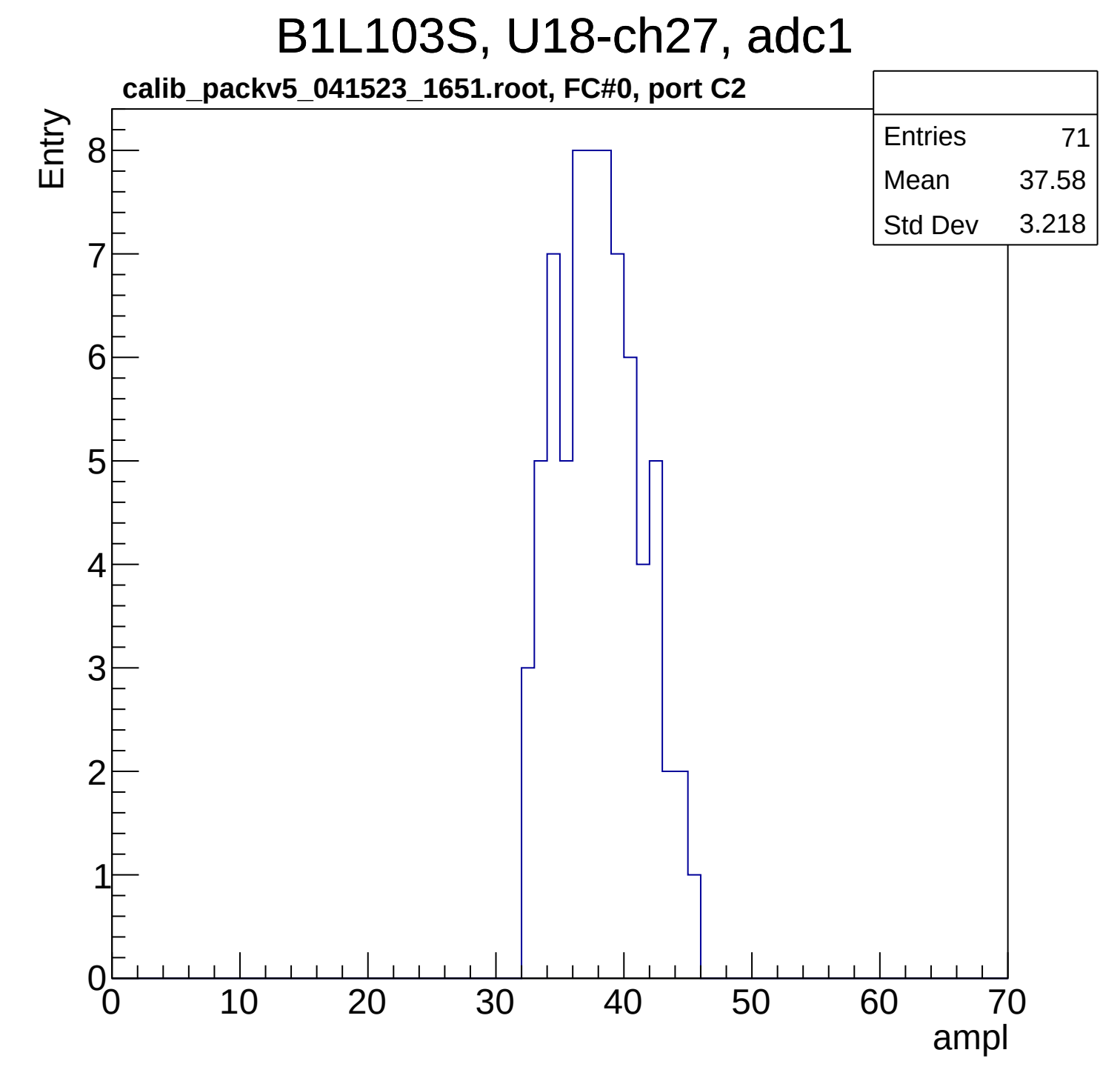
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U18-ch26, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch27, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 26.08
Std Dev 11.57
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch27, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 37.58
Std Dev 3.218
Entry
ampl
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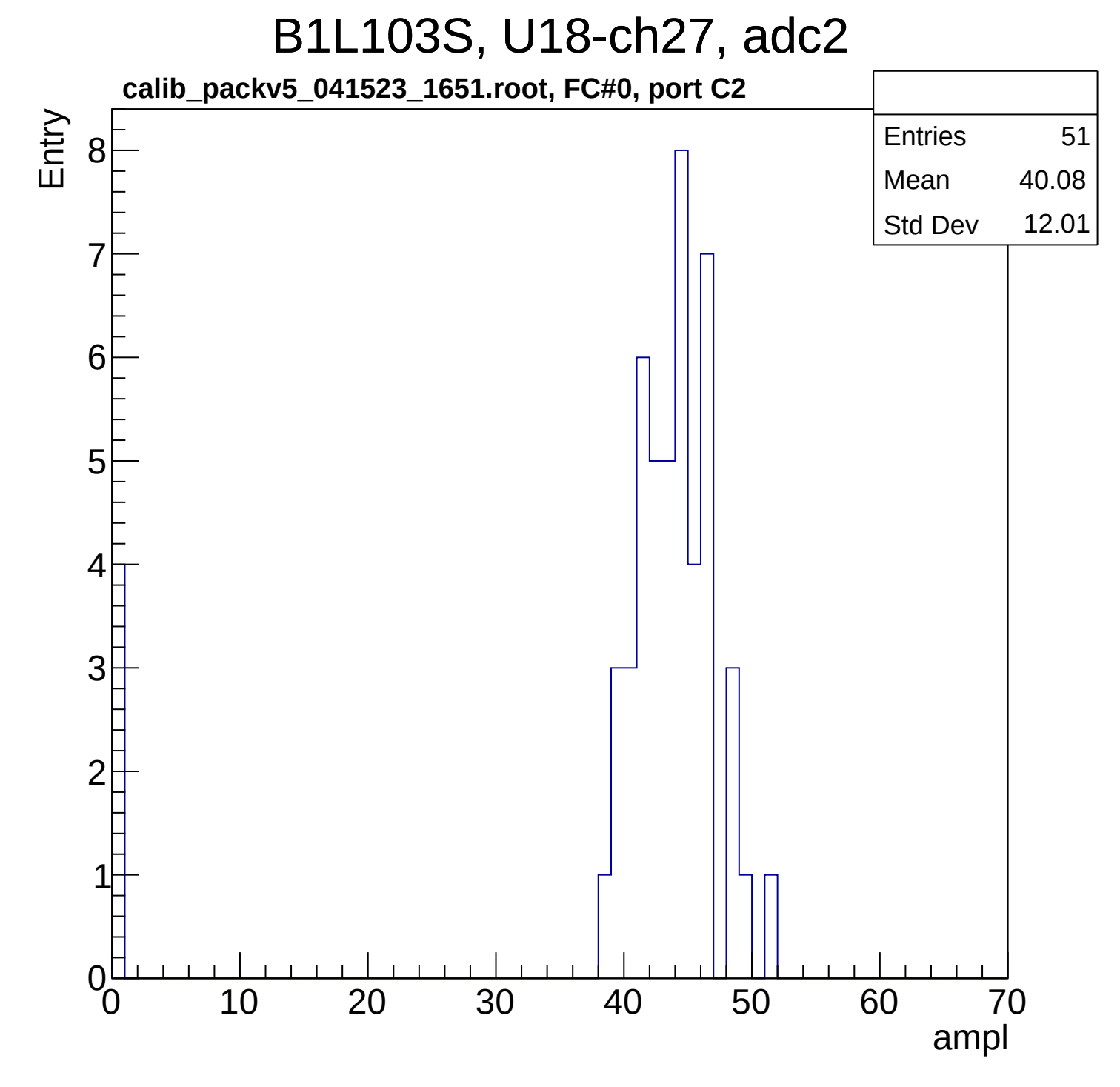
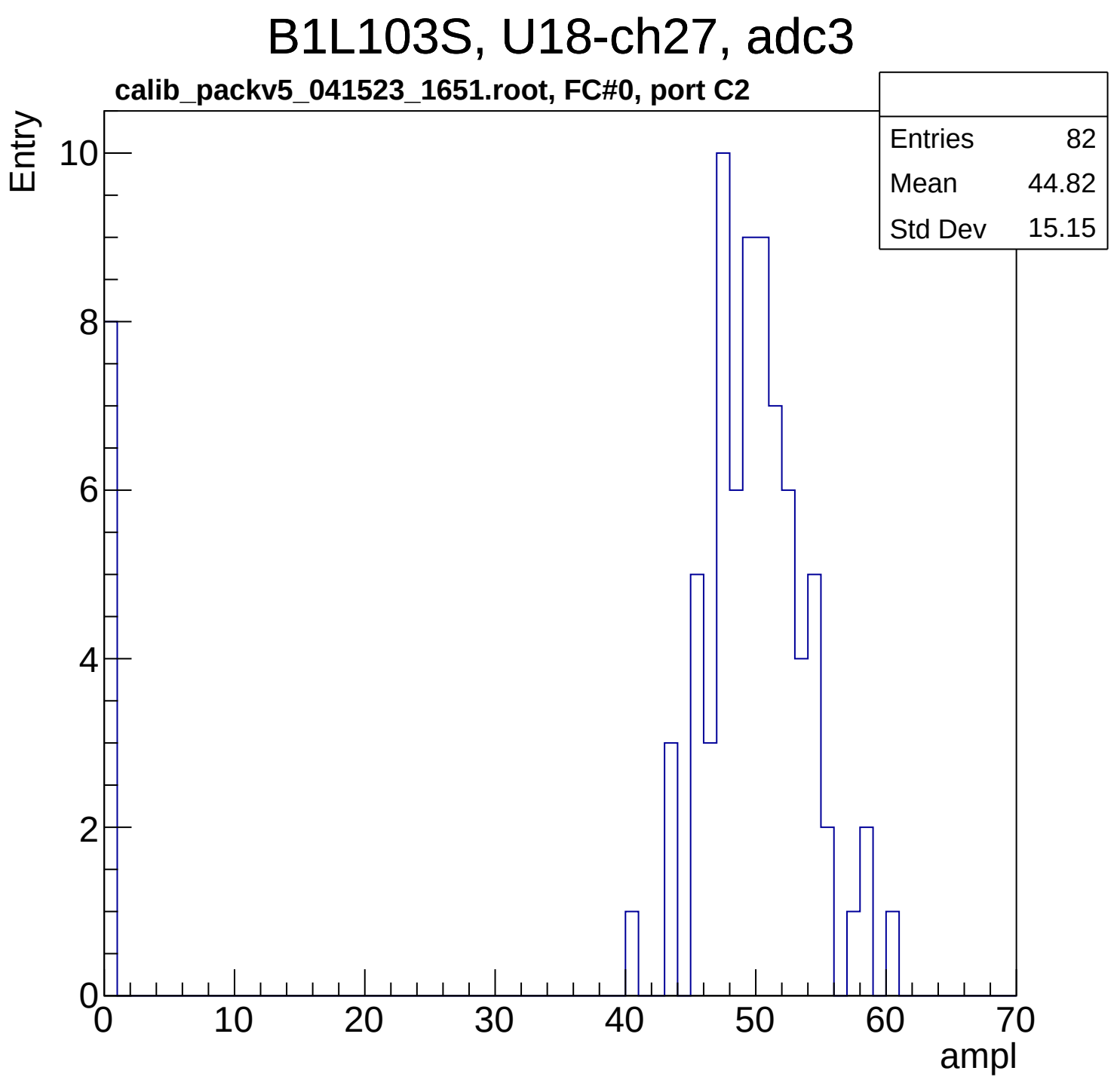
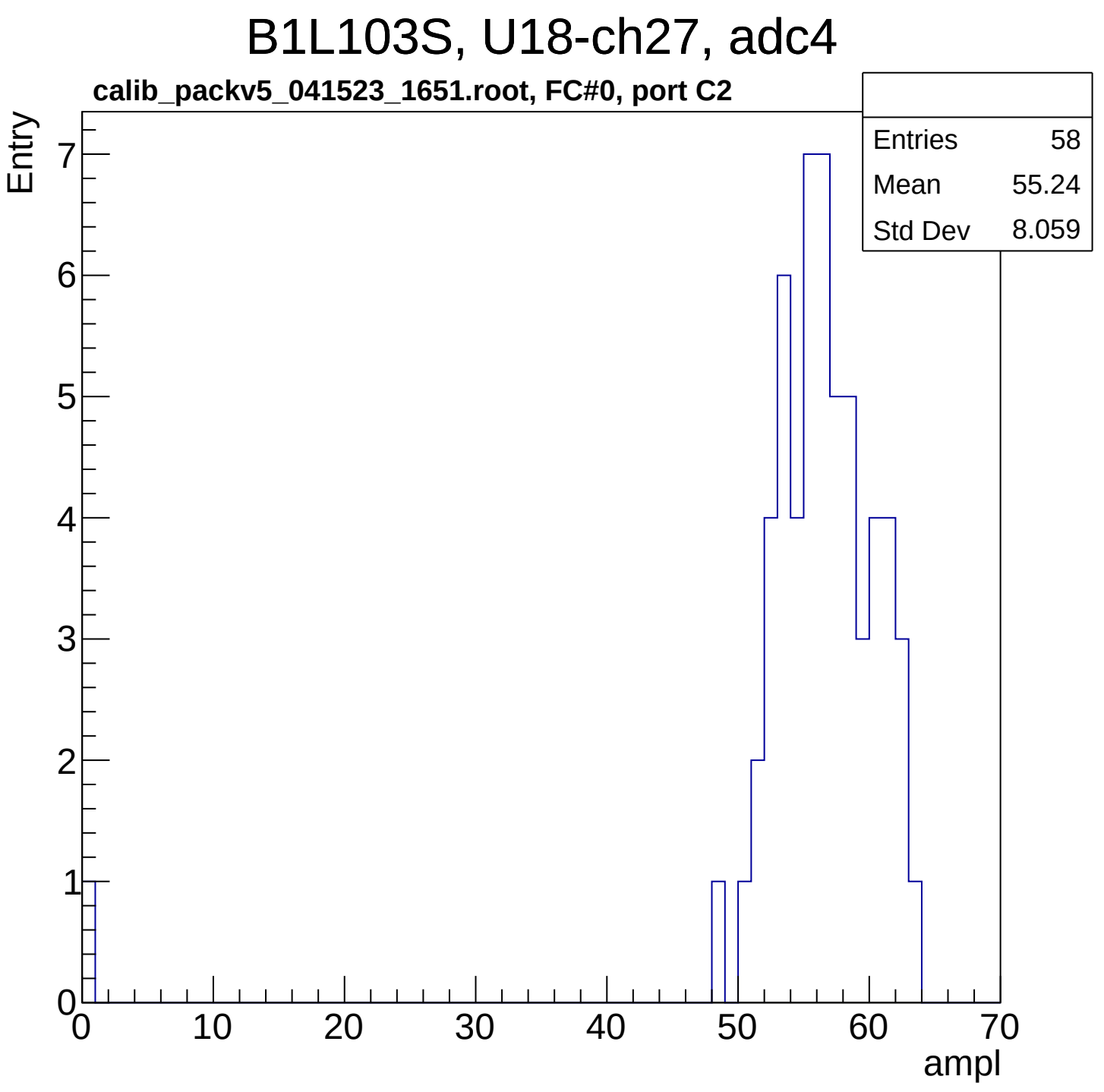
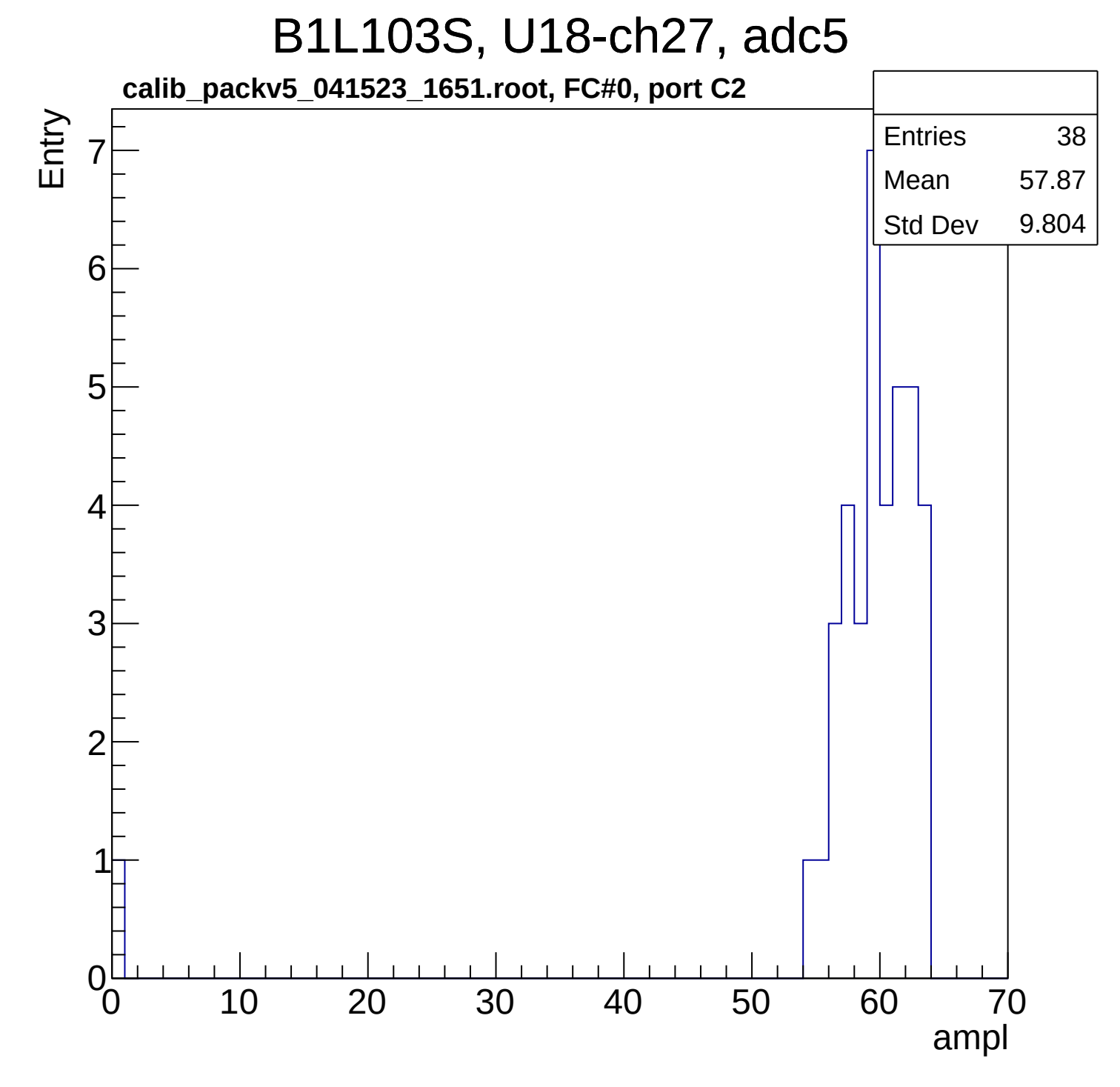
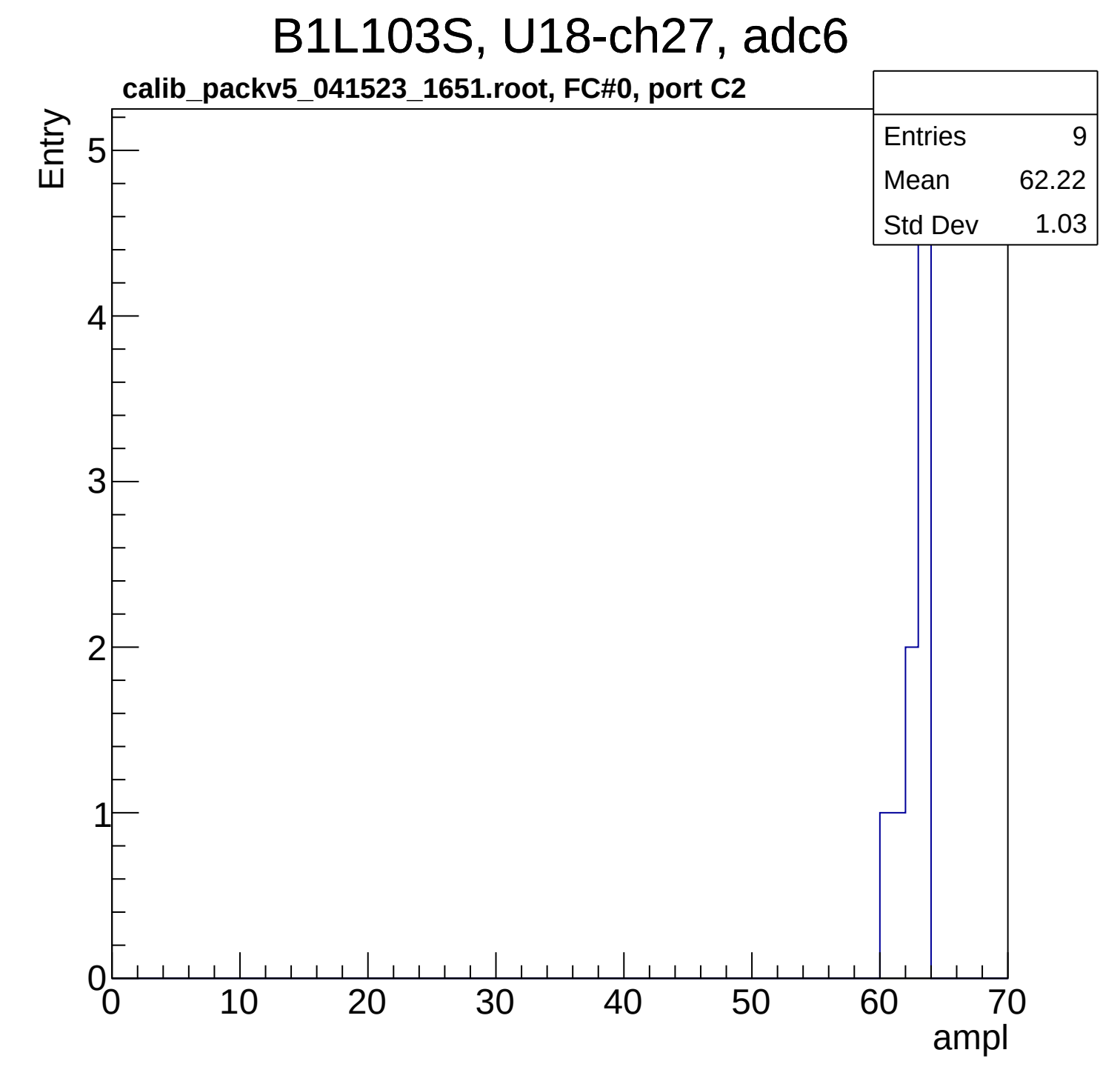
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

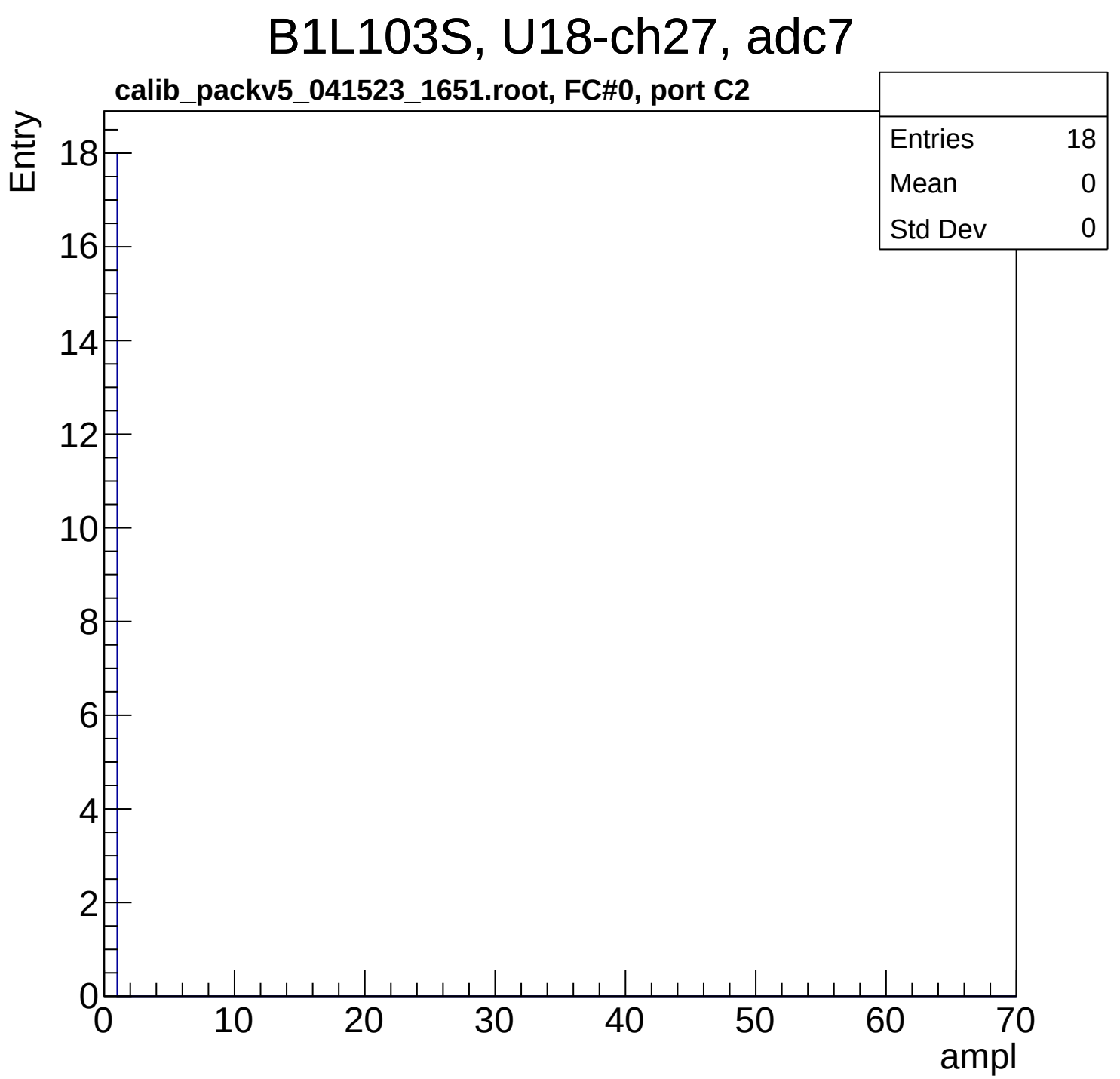

B1L103S, U18-ch27, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 40.08
Std Dev 12.01
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch27, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 44.82
Std Dev 15.15
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U18-ch27, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 55.24
Std Dev 8.059
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U18-ch27, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 38
Mean 57.87
Std Dev 9.804
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U18-ch27, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 9
Mean 62.22
Std Dev 1.03
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U18-ch27, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
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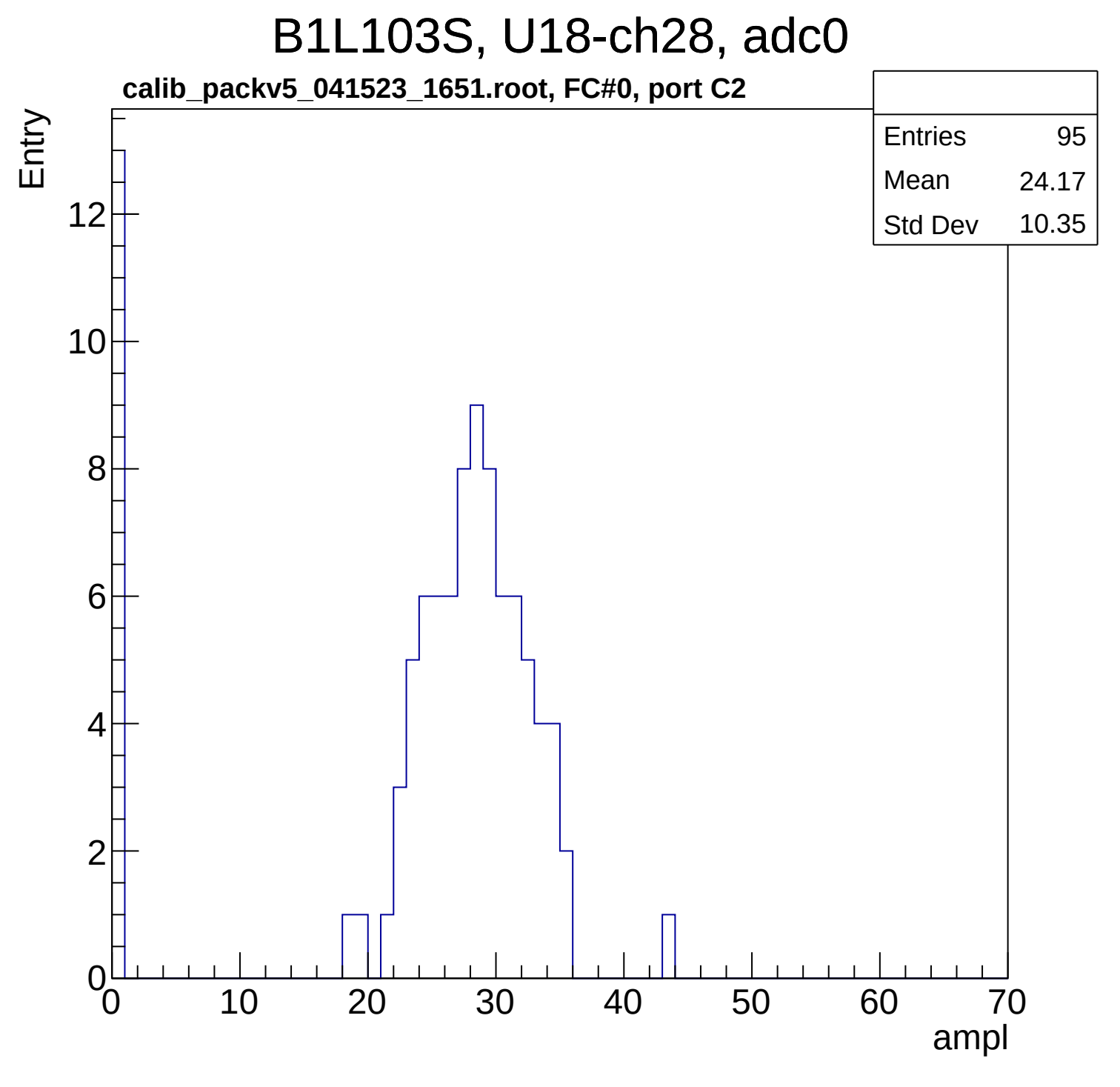
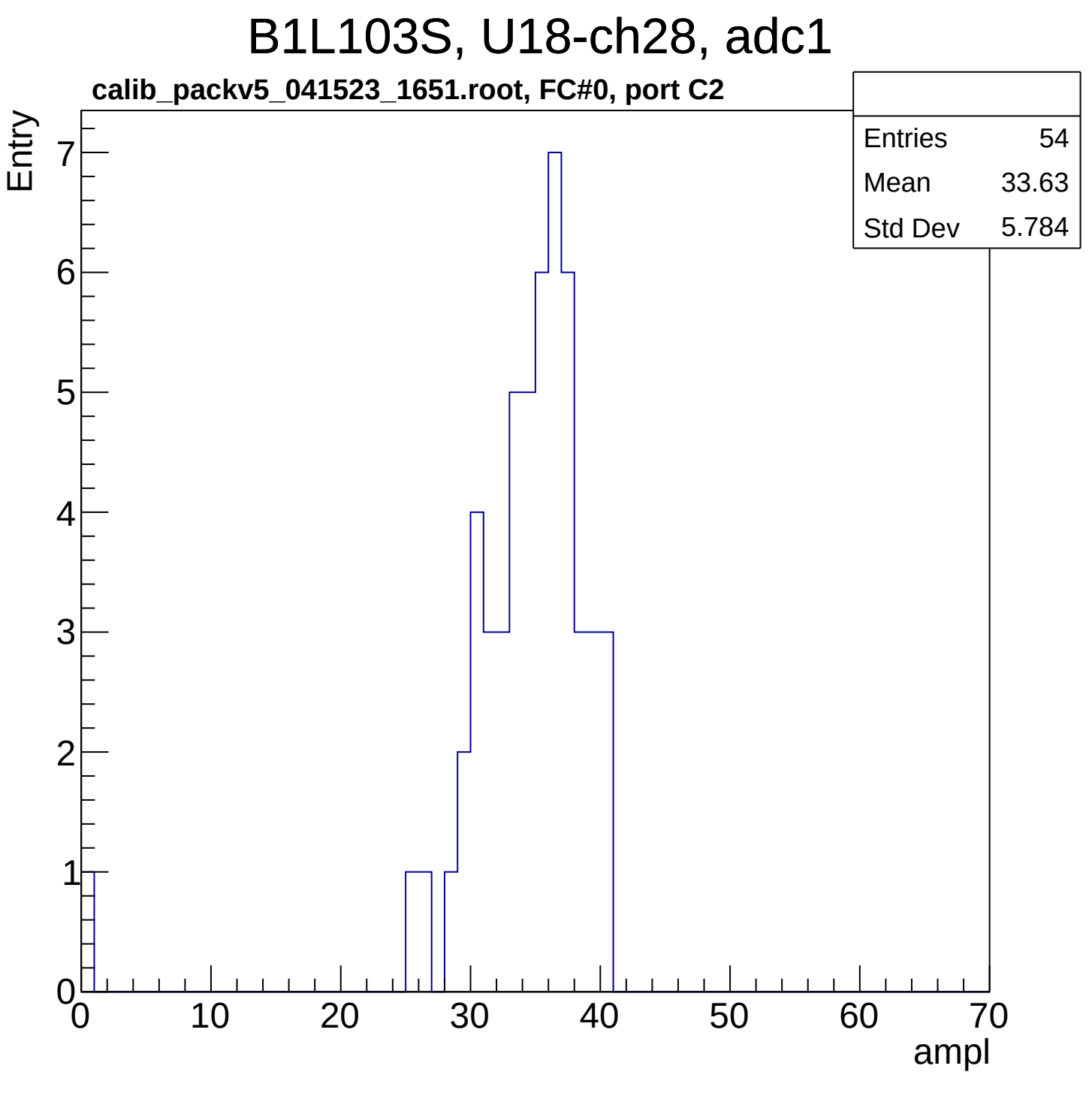
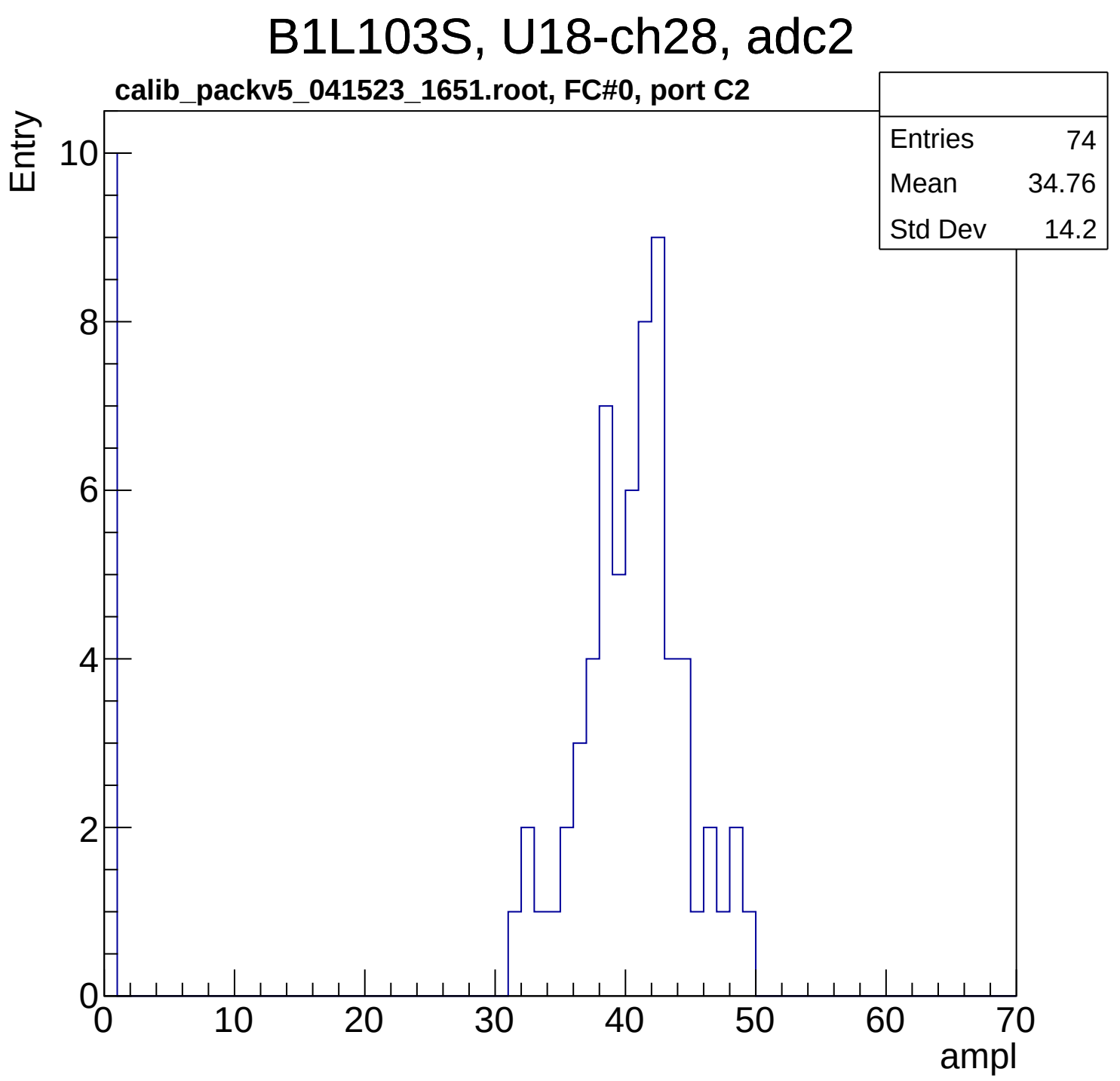
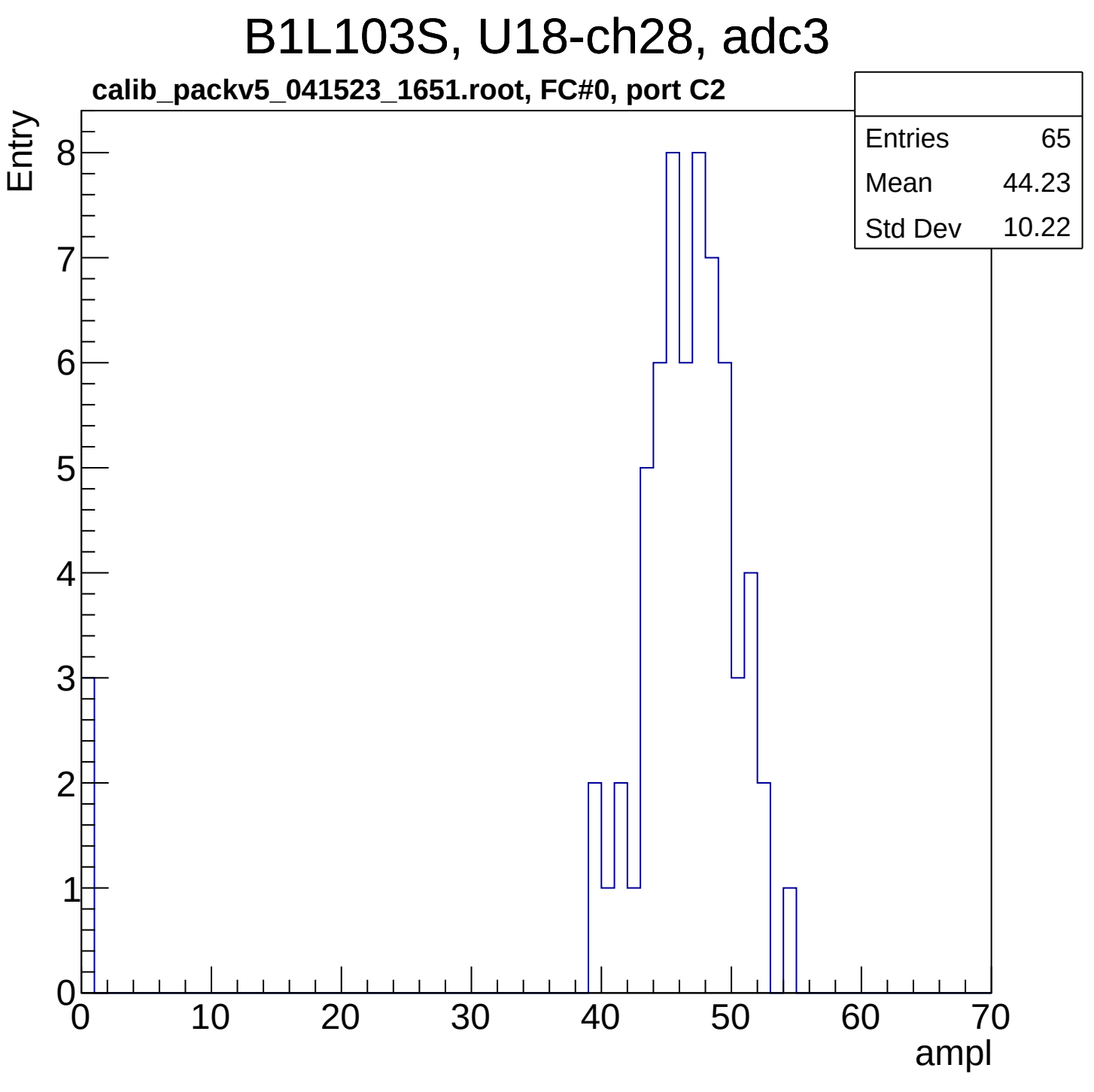
50
60
70
ampl


B1L103S, U18-ch28, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 95
Mean 24.17
Std Dev 10.35
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch28, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 33.63
Std Dev 5.784
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U18-ch28, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 34.76
Std Dev 14.2
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch28, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 44.23
Std Dev 10.22
Entry
ampl
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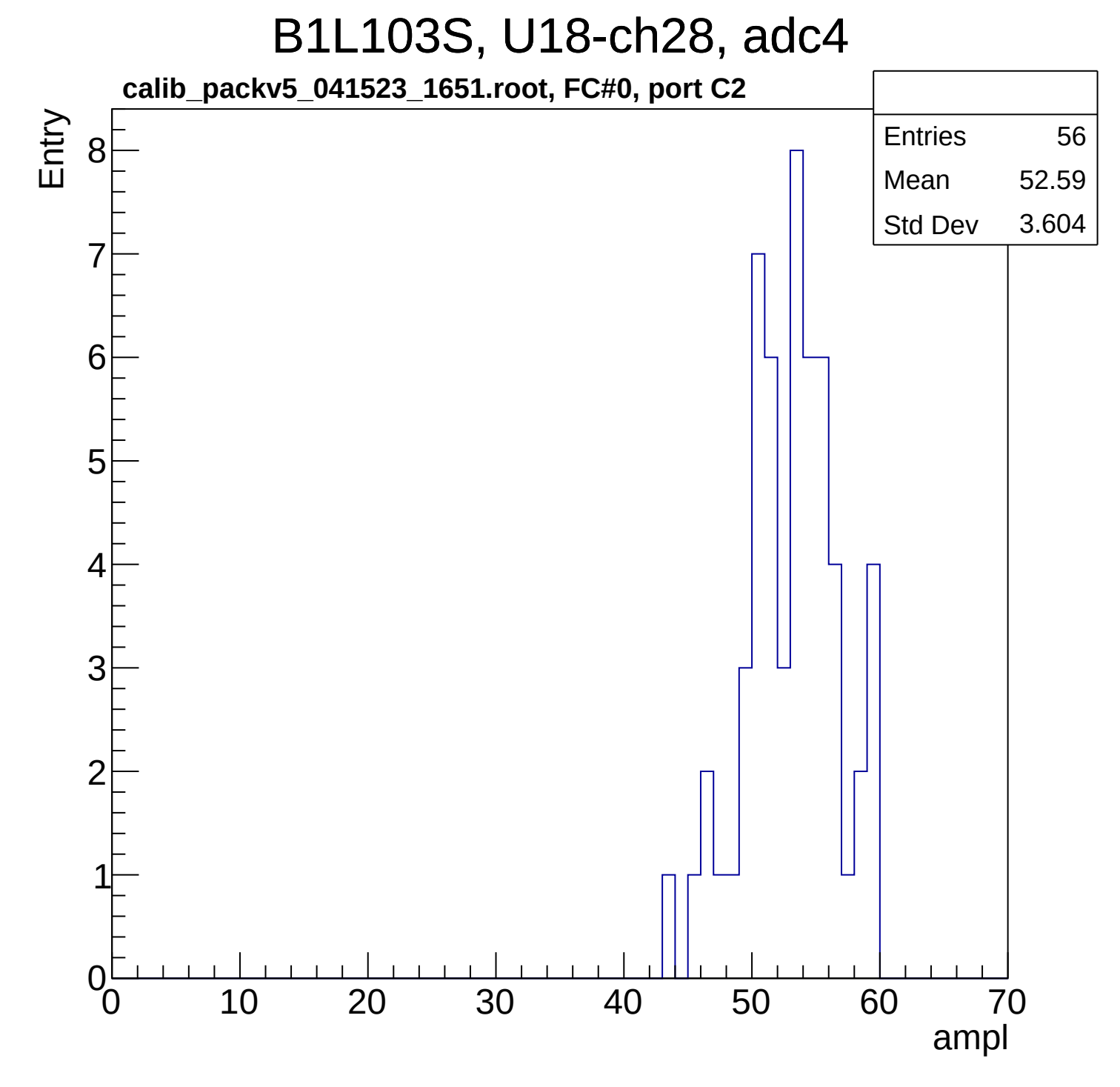
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch28, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 52.59
Std Dev 3.604
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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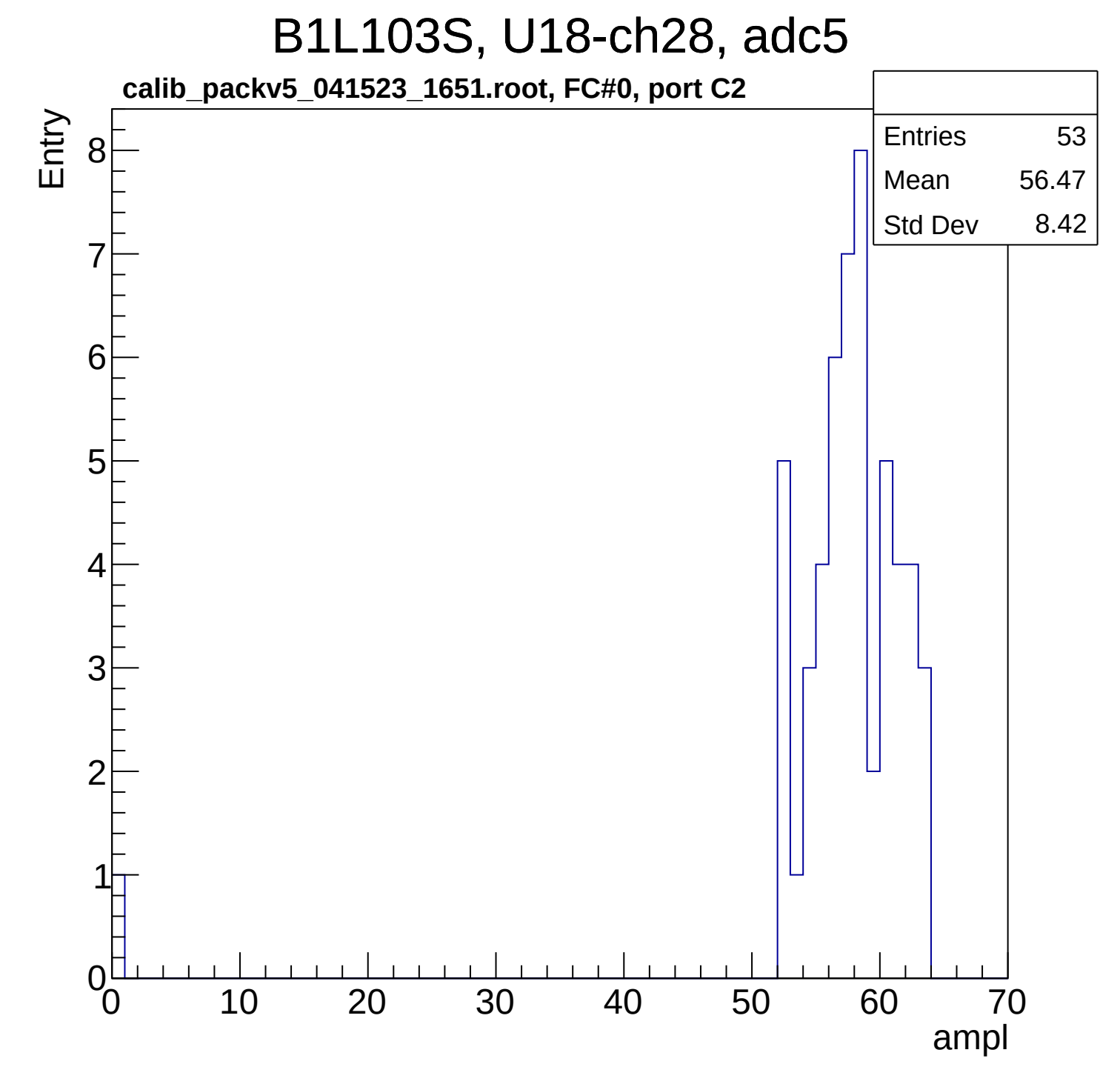
B1L103S, U18-ch28, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 56.47
Std Dev 8.42
Entry
ampl
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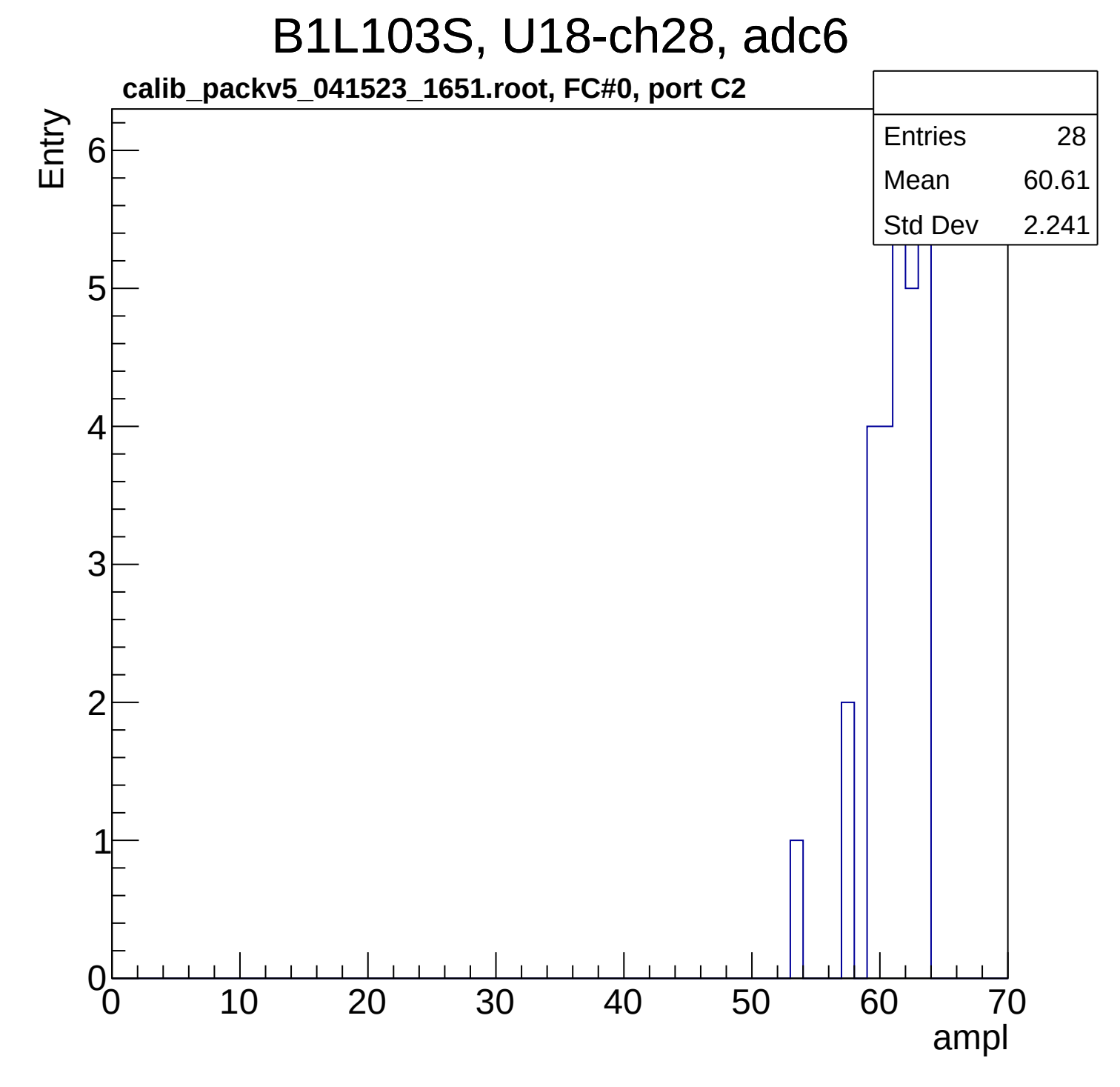
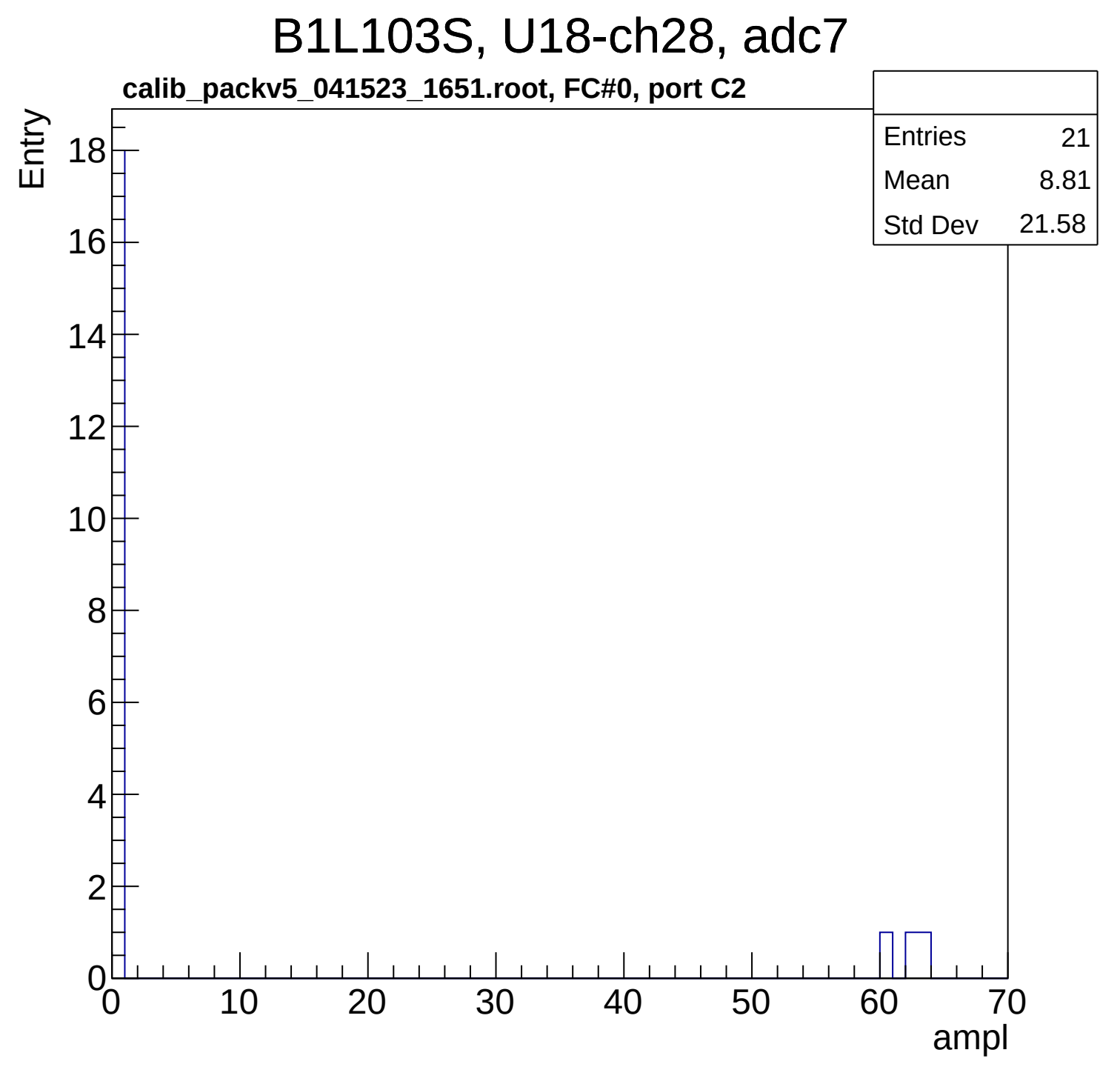
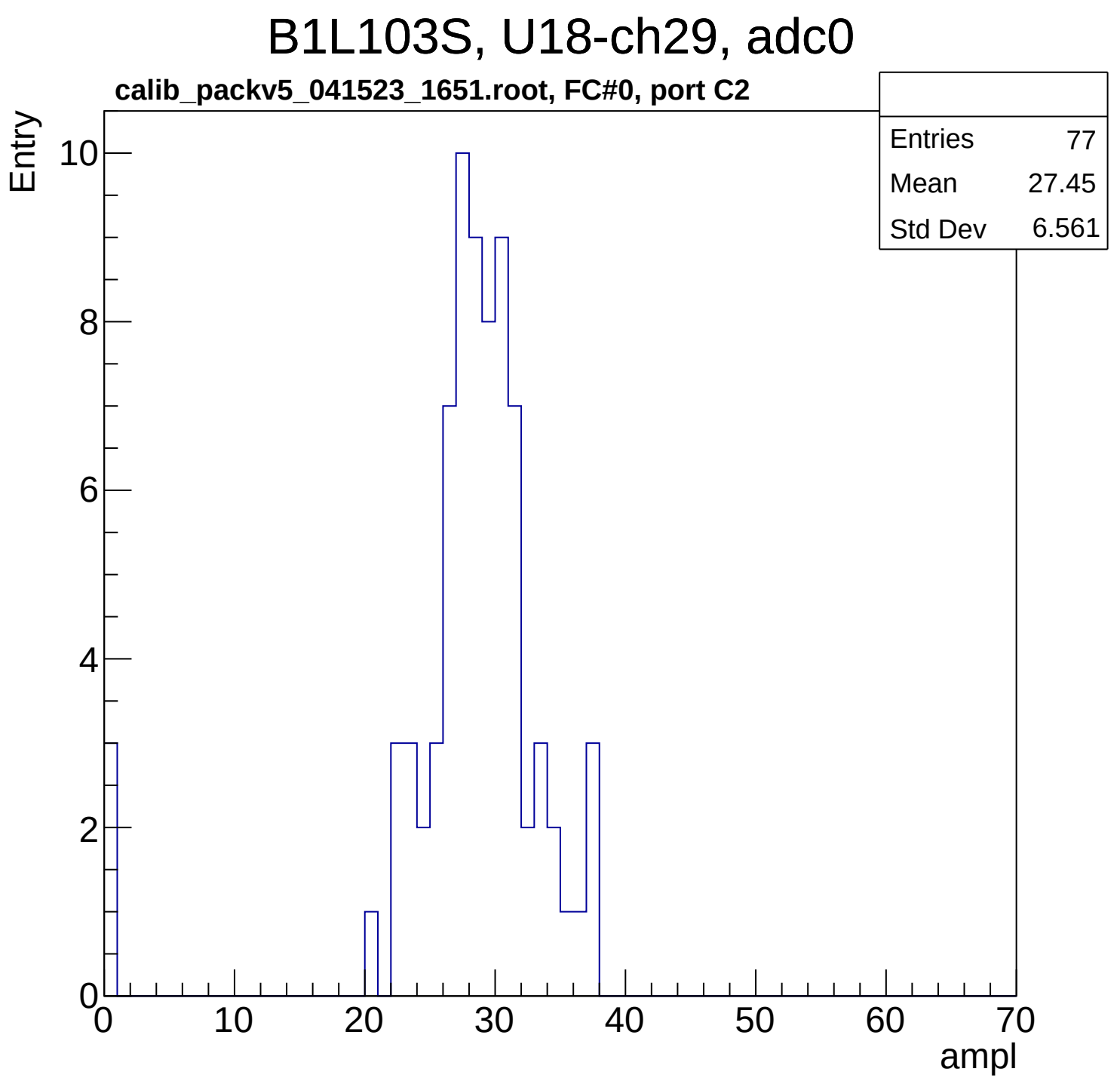
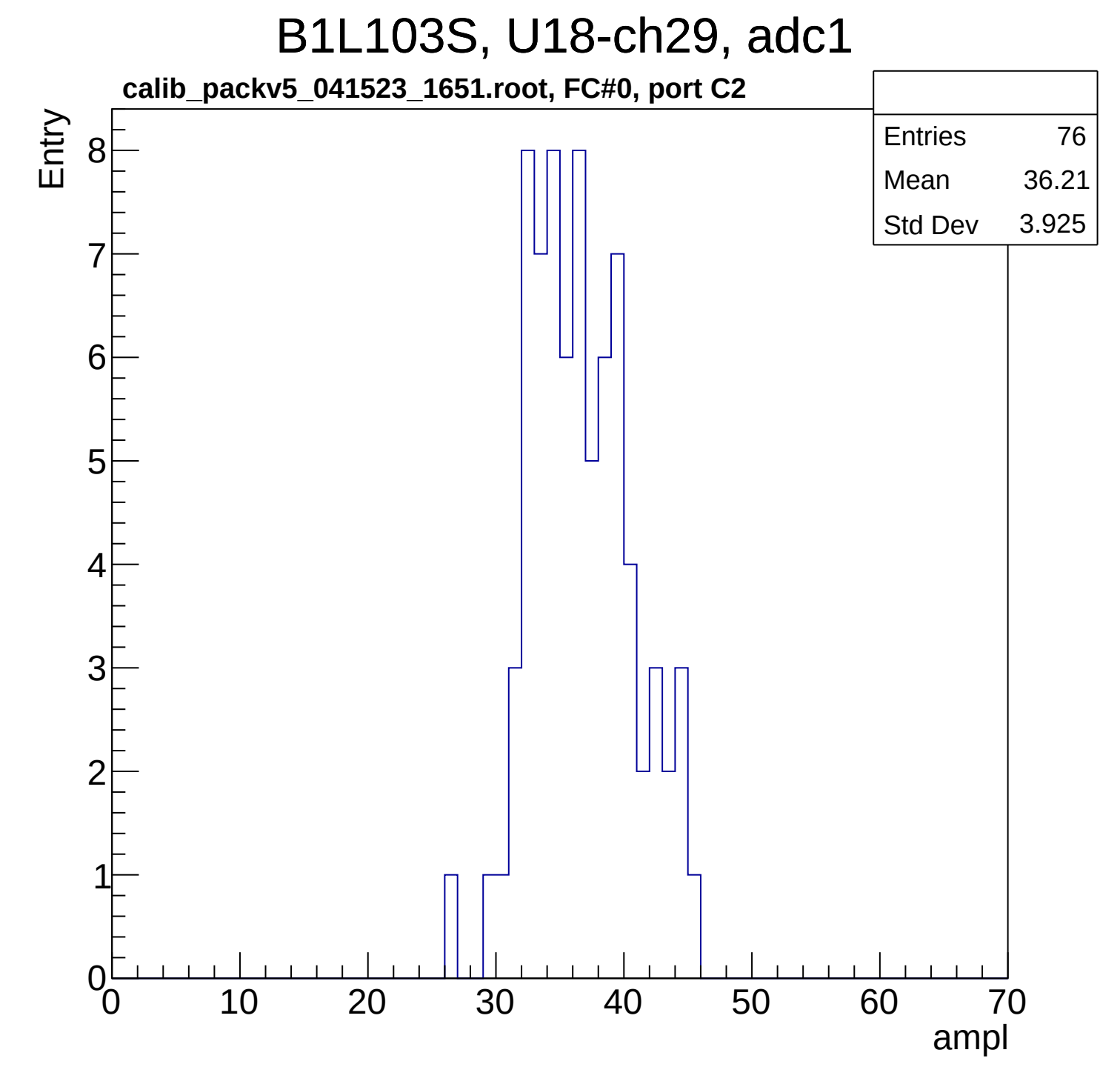
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch28, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 28
Mean 60.61
Std Dev 2.241
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U18-ch28, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 8.81
Std Dev 21.58
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch29, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 27.45
Std Dev 6.561
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U18-ch29, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 36.21
Std Dev 3.925
Entry
ampl
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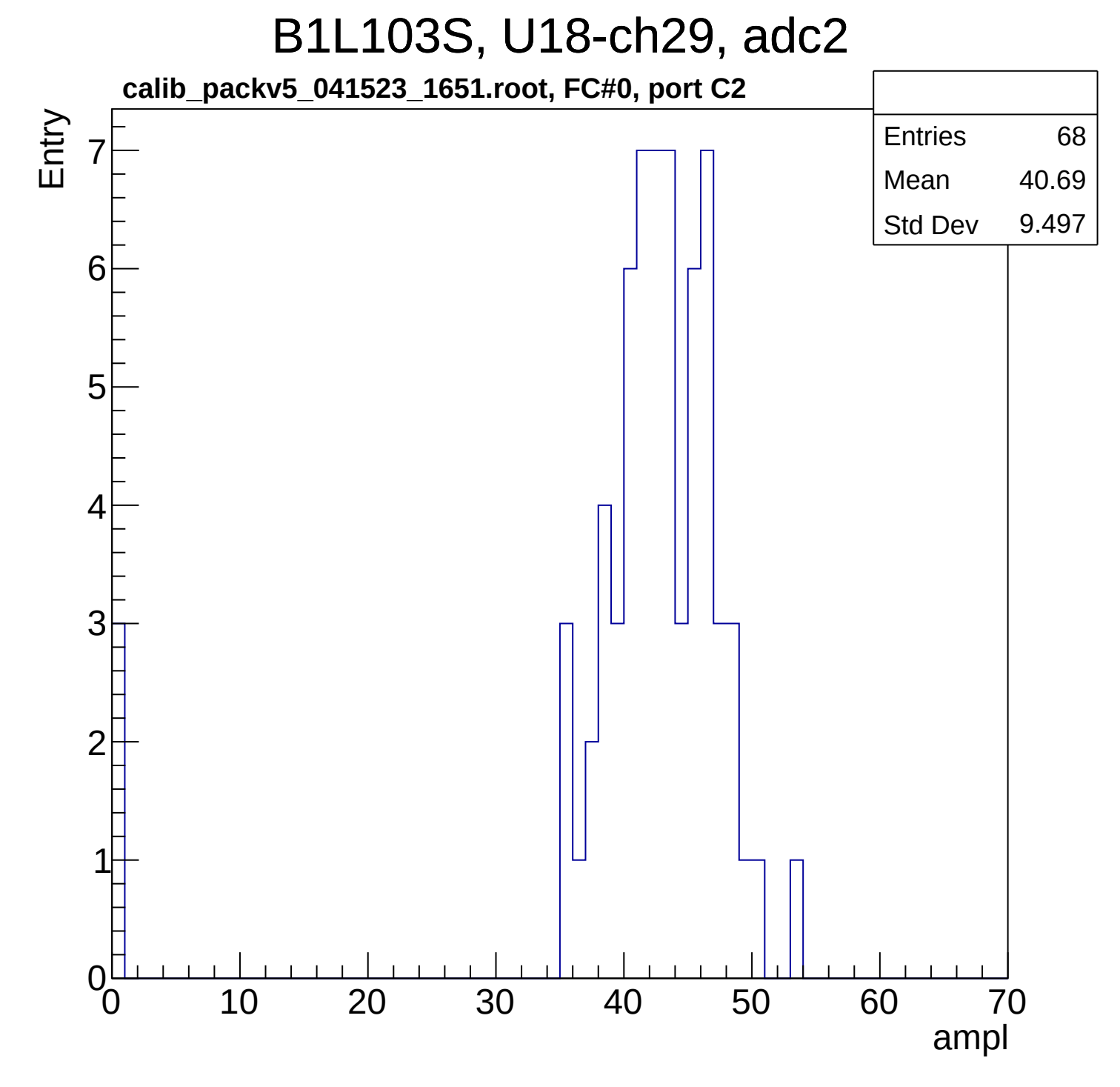
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch29, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 40.69
Std Dev 9.497
Entry
ampl
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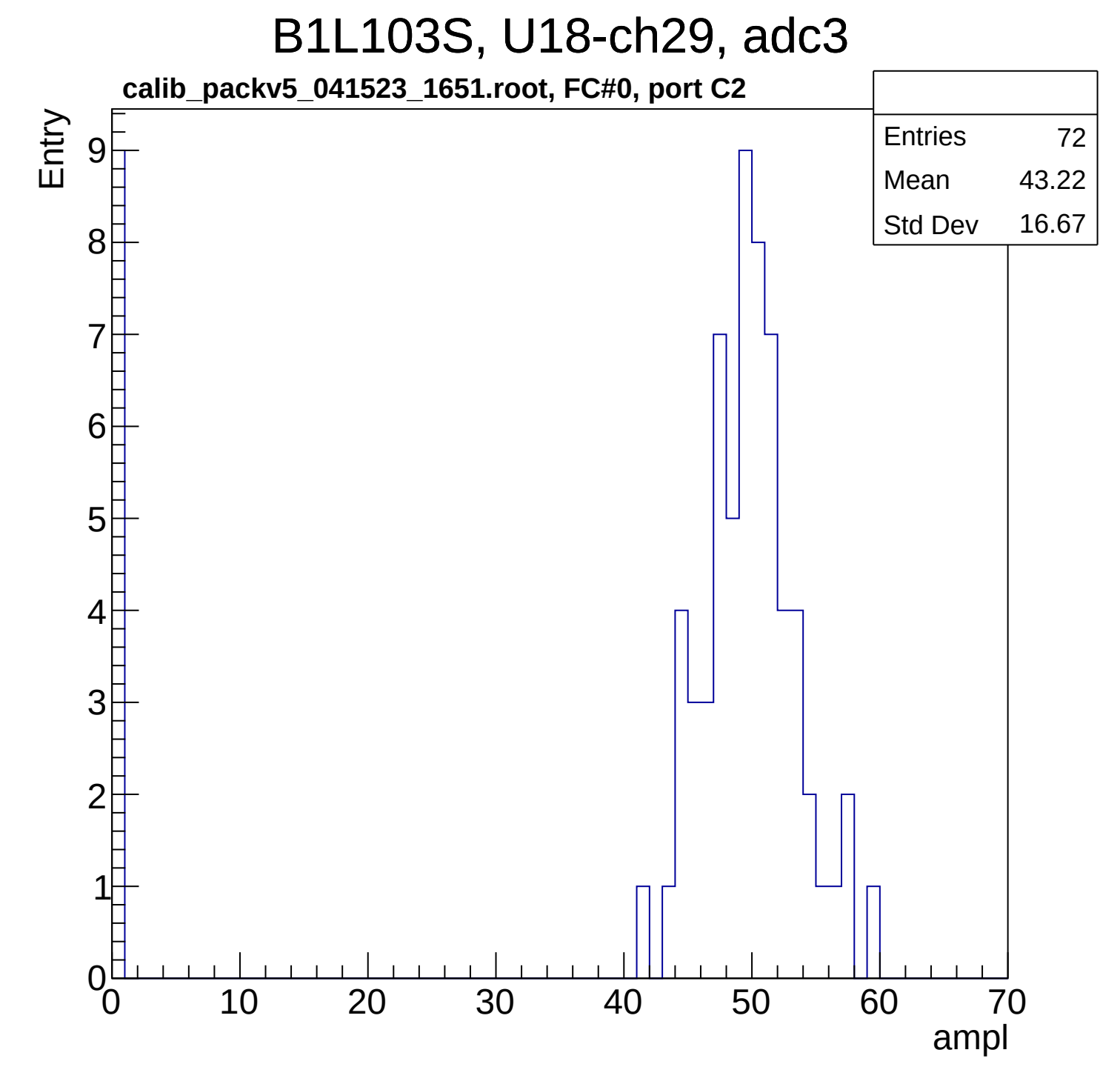
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U18-ch29, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 43.22
Std Dev 16.67
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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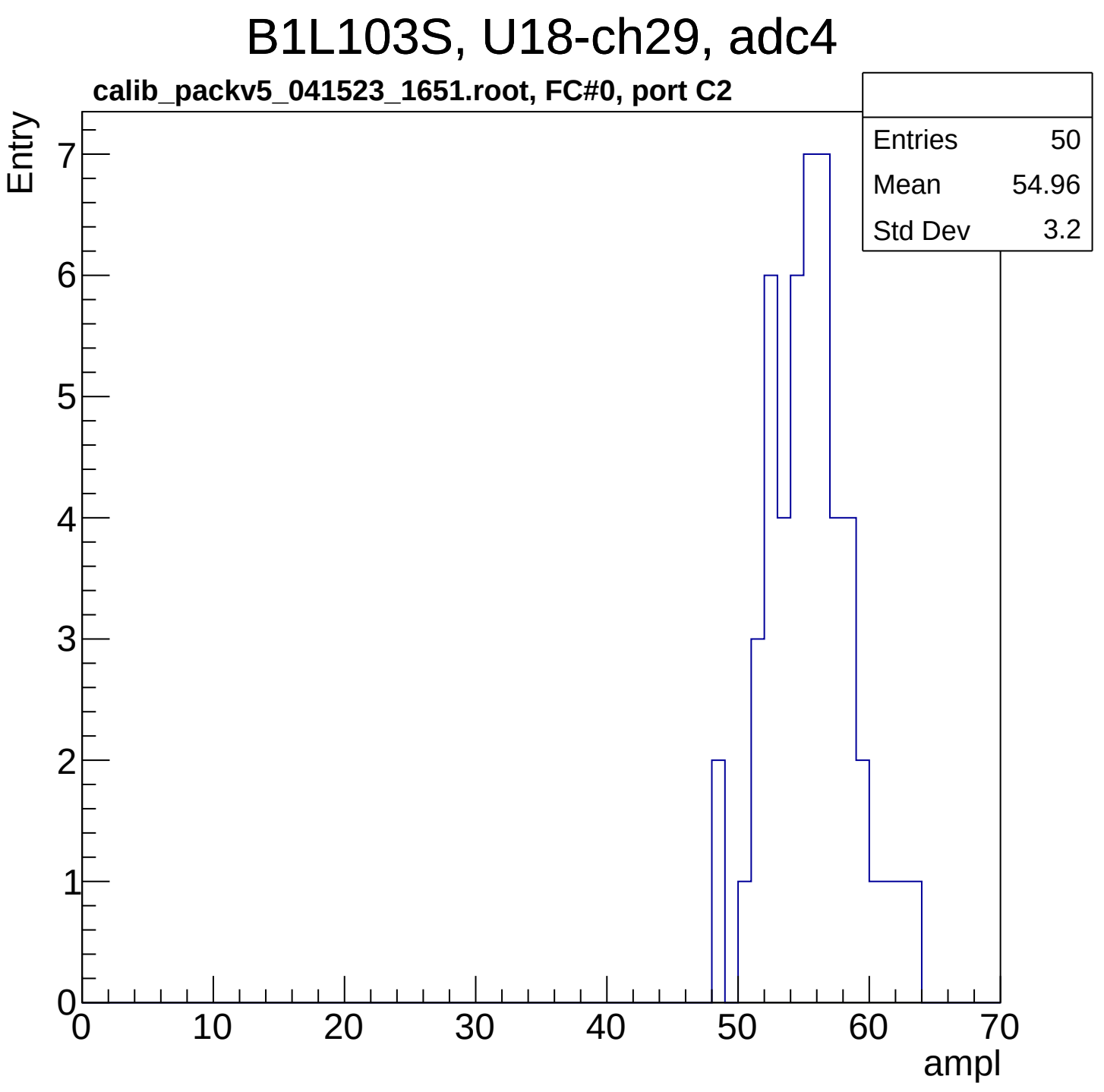
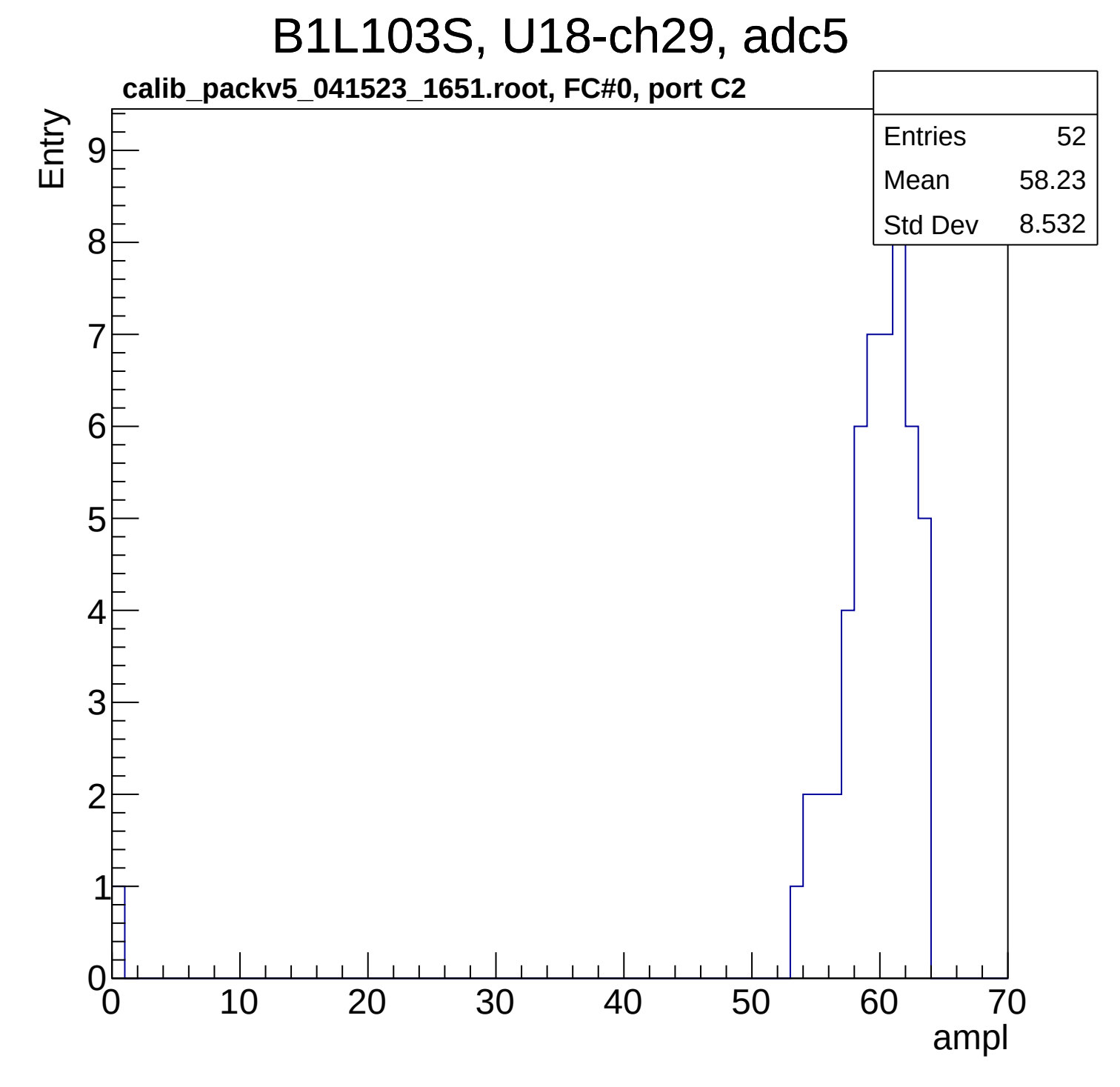

B1L103S, U18-ch29, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 54.96
Std Dev 3.2
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U18-ch29, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 58.23
Std Dev 8.532
Entry
ampl
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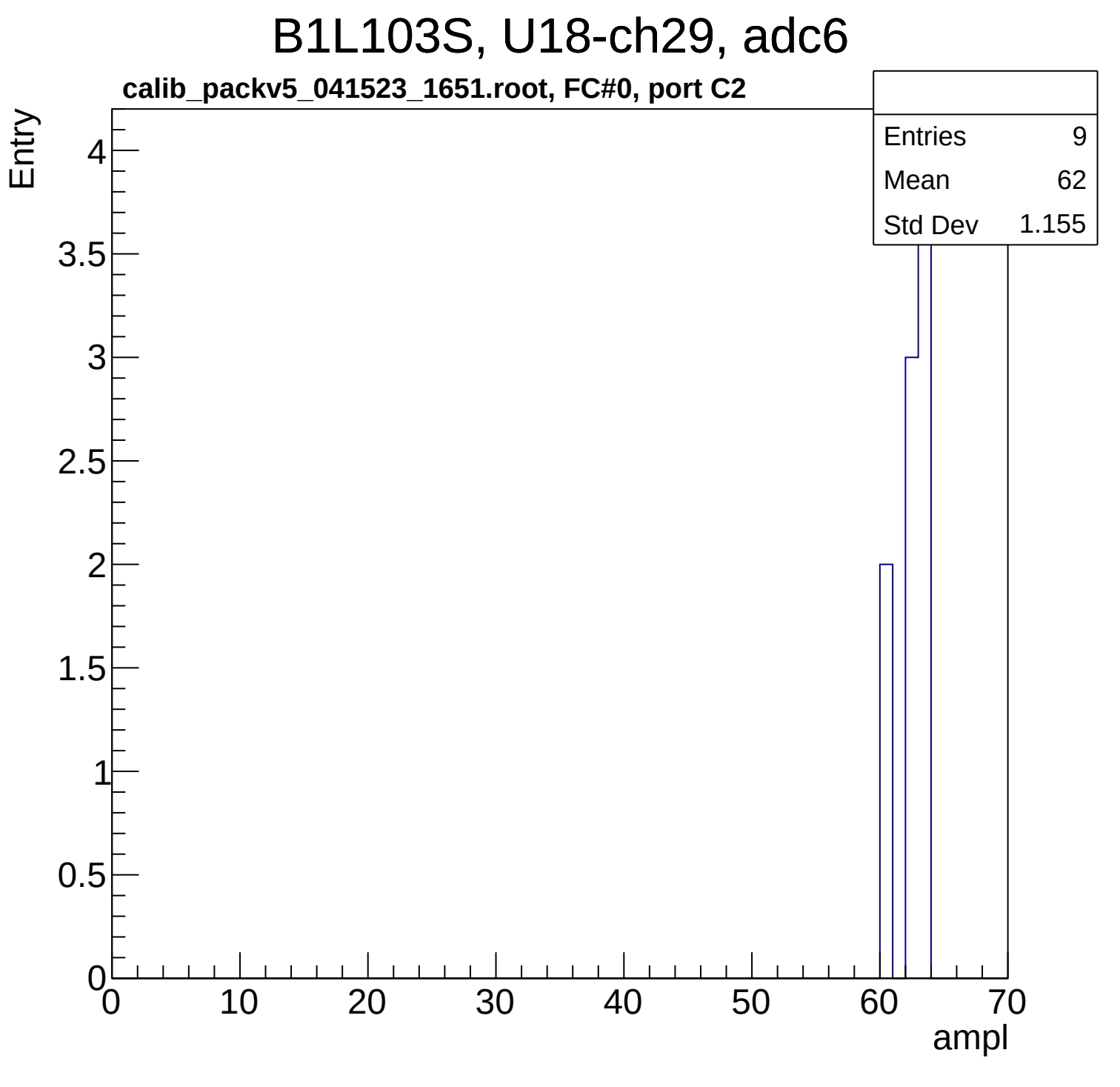
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U18-ch29, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 9
Mean 62
Std Dev 1.155
Entry
ampl
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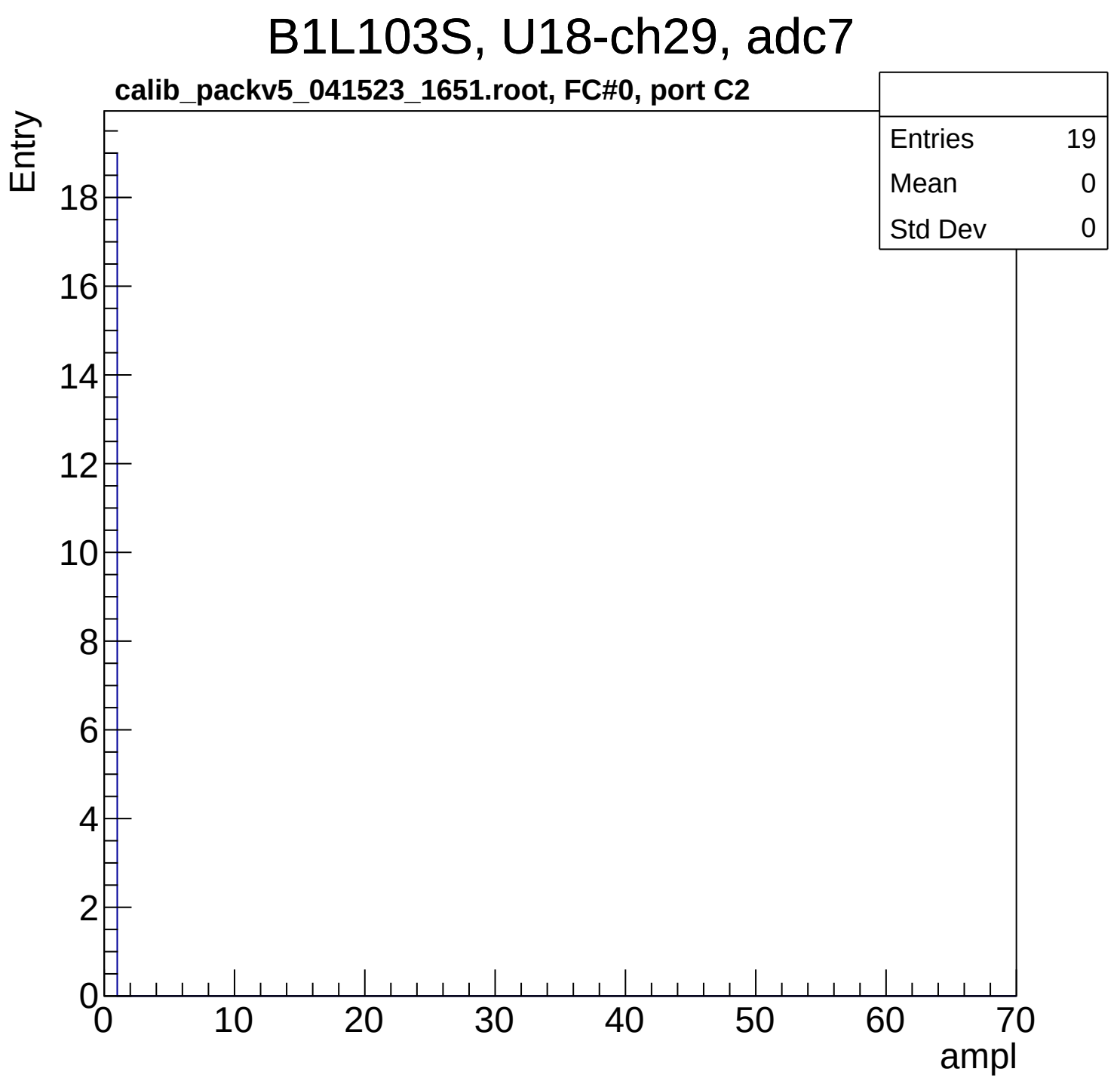
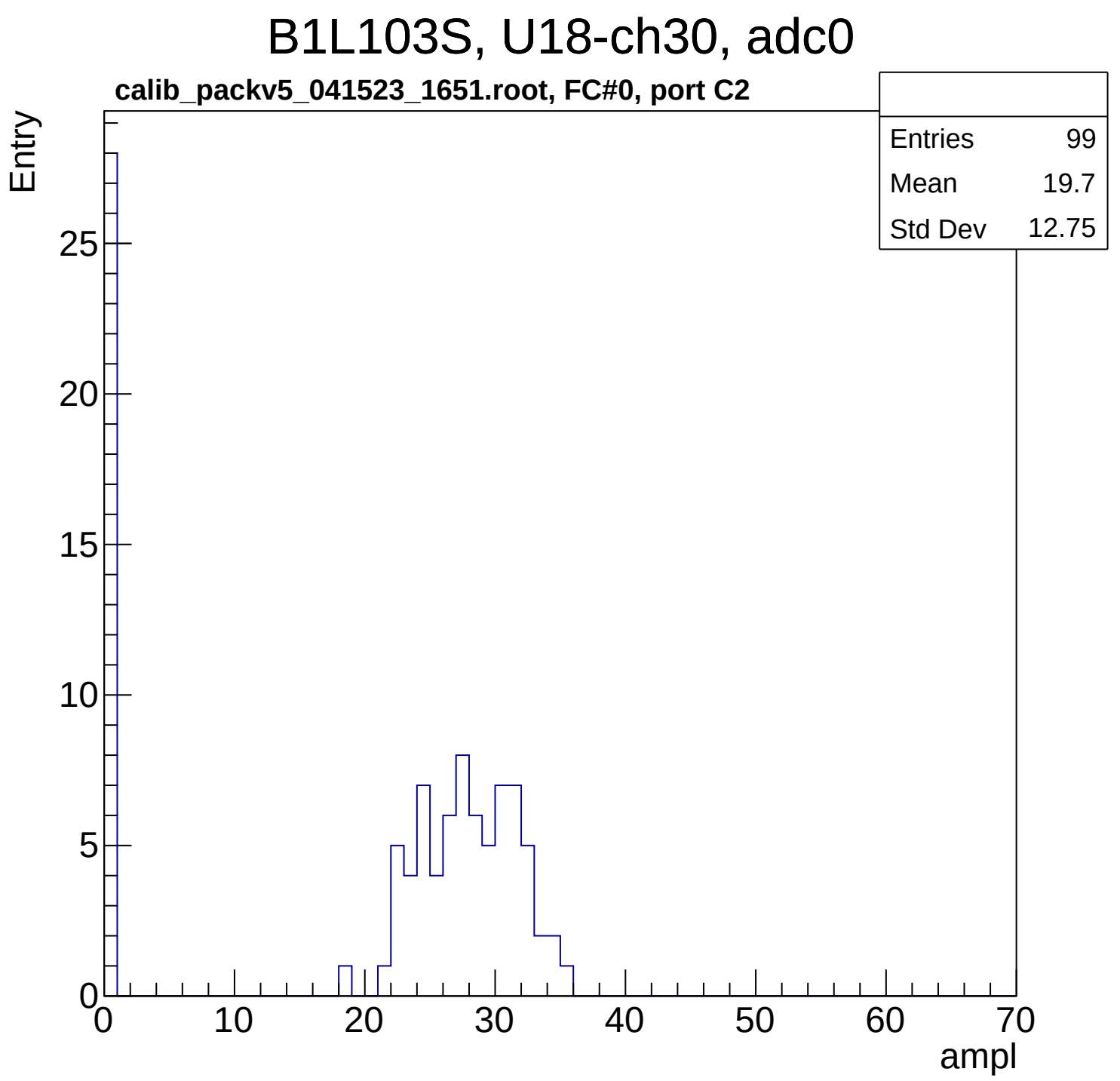
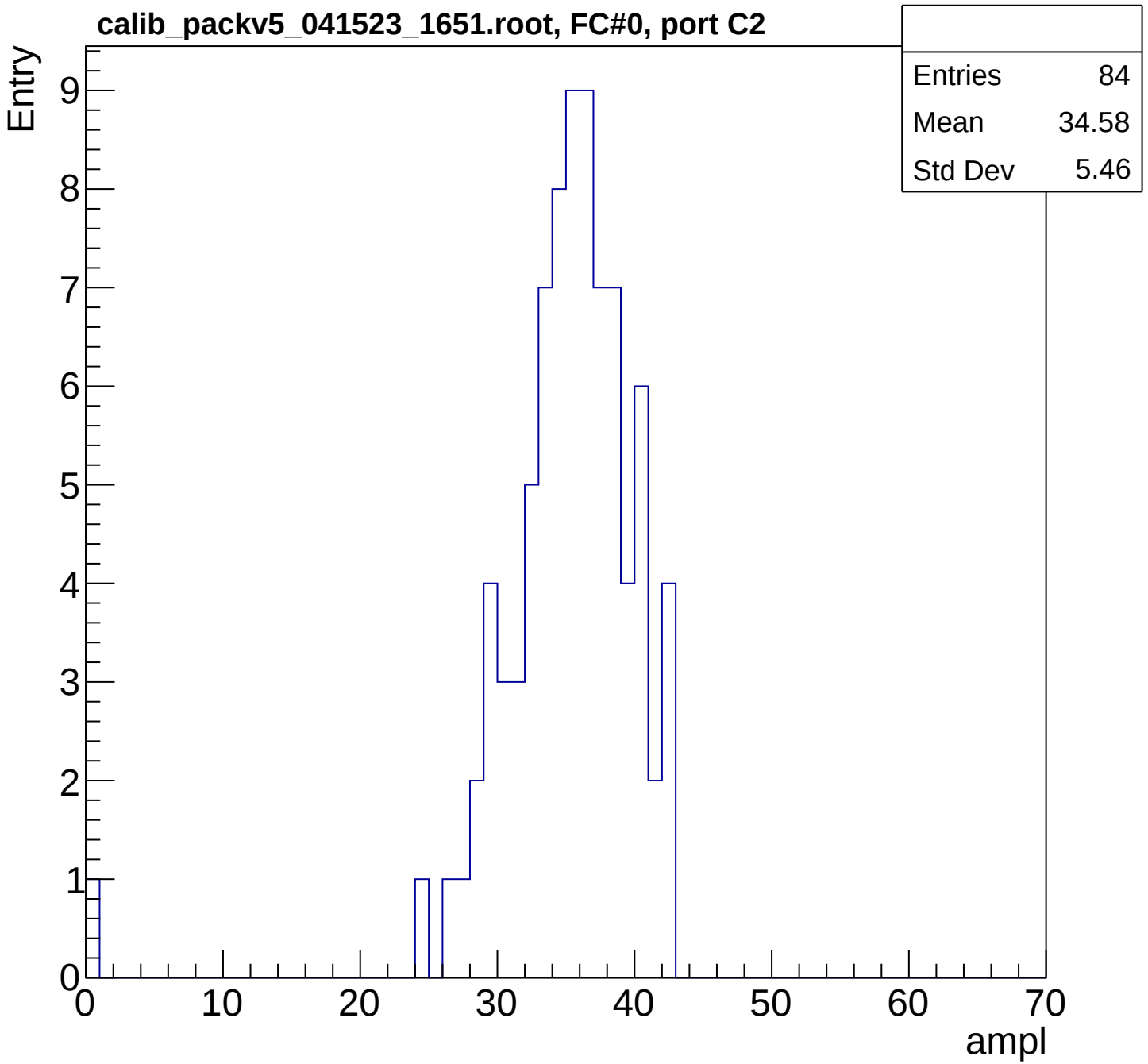
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U18-ch29, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch30, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 99
Mean 19.7
Std Dev 12.75
Entry
0
5
10
15
20
25
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch30, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 34.58
Std Dev 5.46
Entry
ampl
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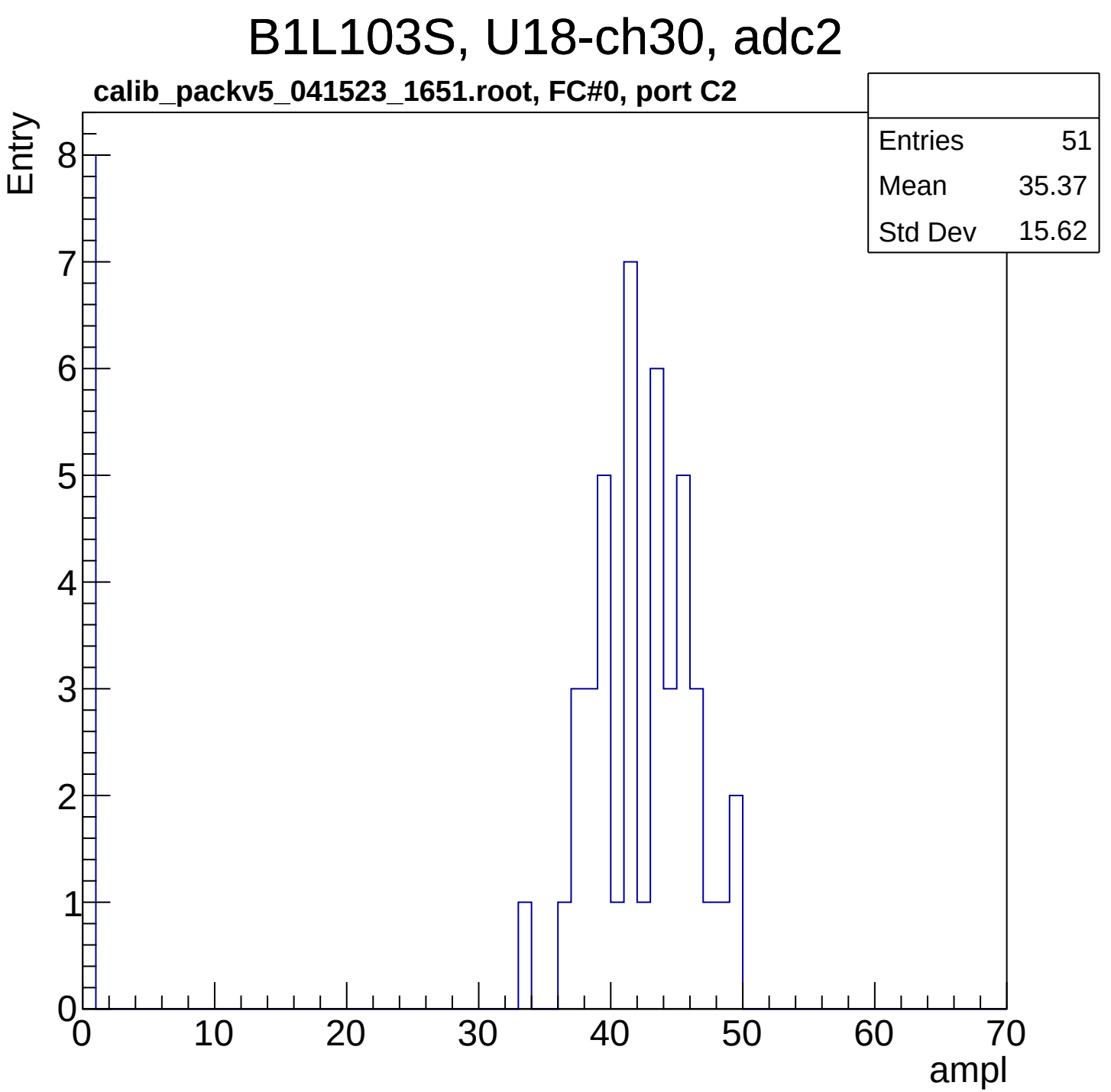
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U18-ch30, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 35.37
Std Dev 15.62
Entry
ampl
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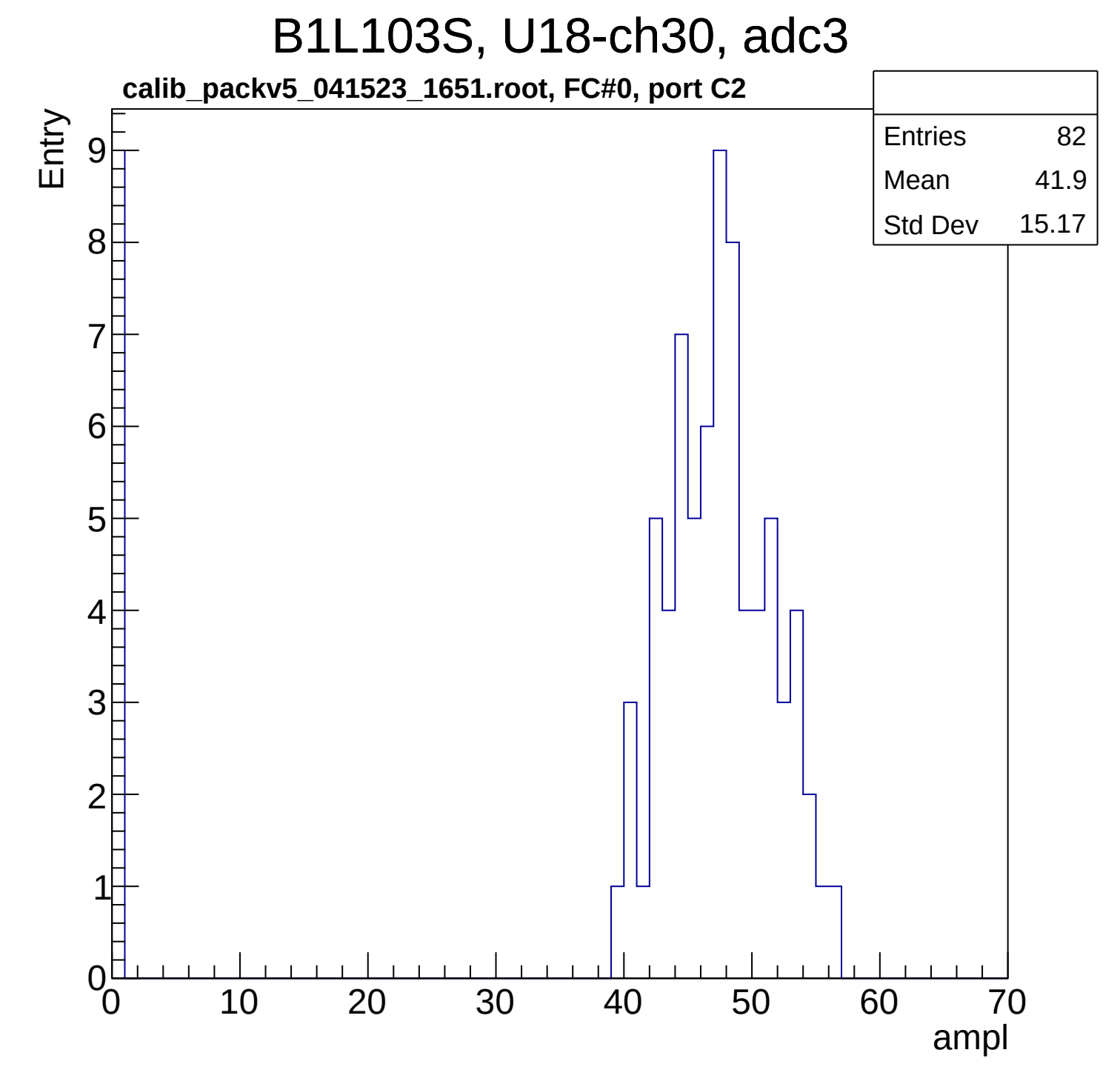
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch30, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 41.9
Std Dev 15.17
Entry
ampl
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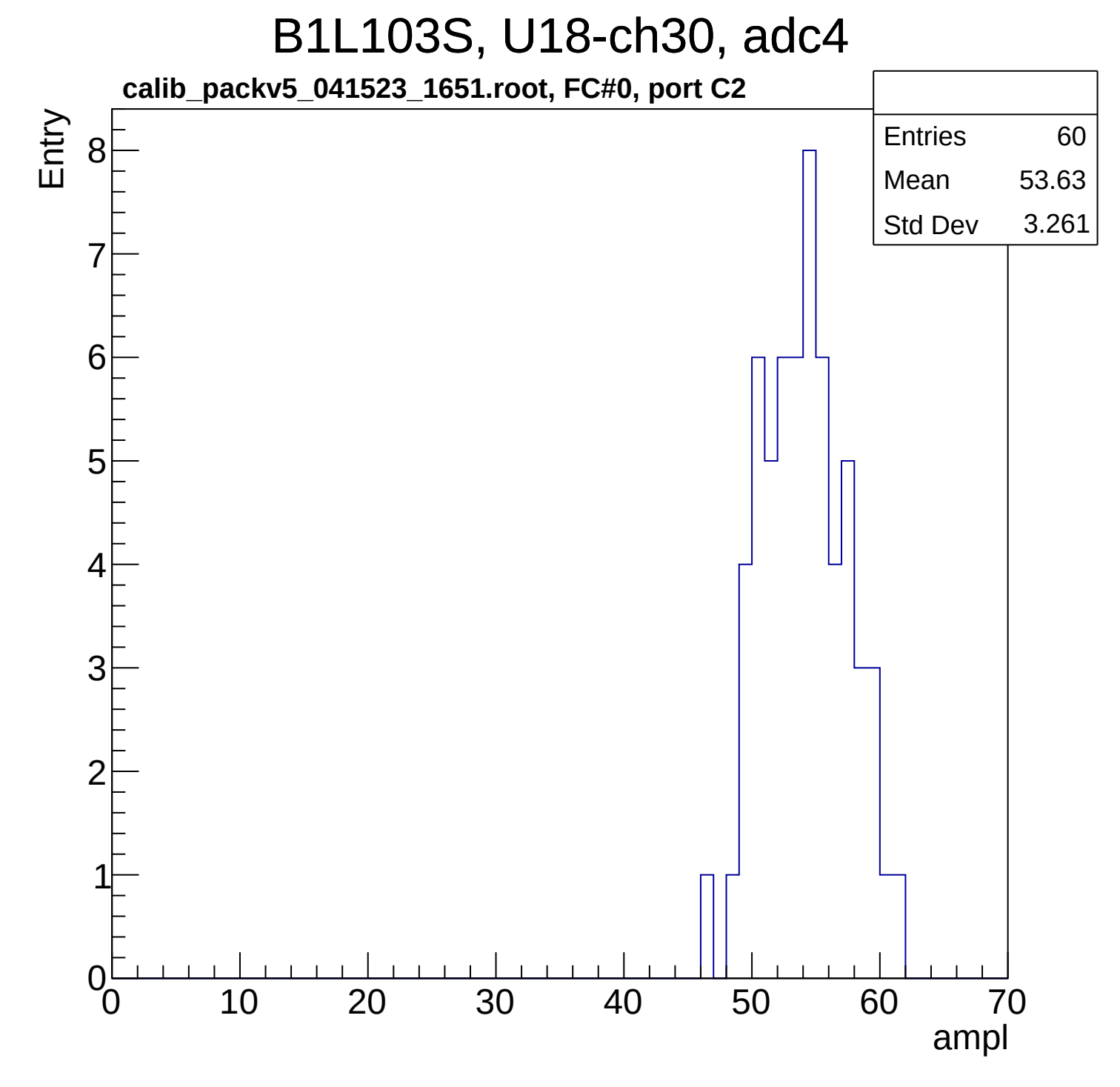
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U18-ch30, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 53.63
Std Dev 3.261
Entry
ampl
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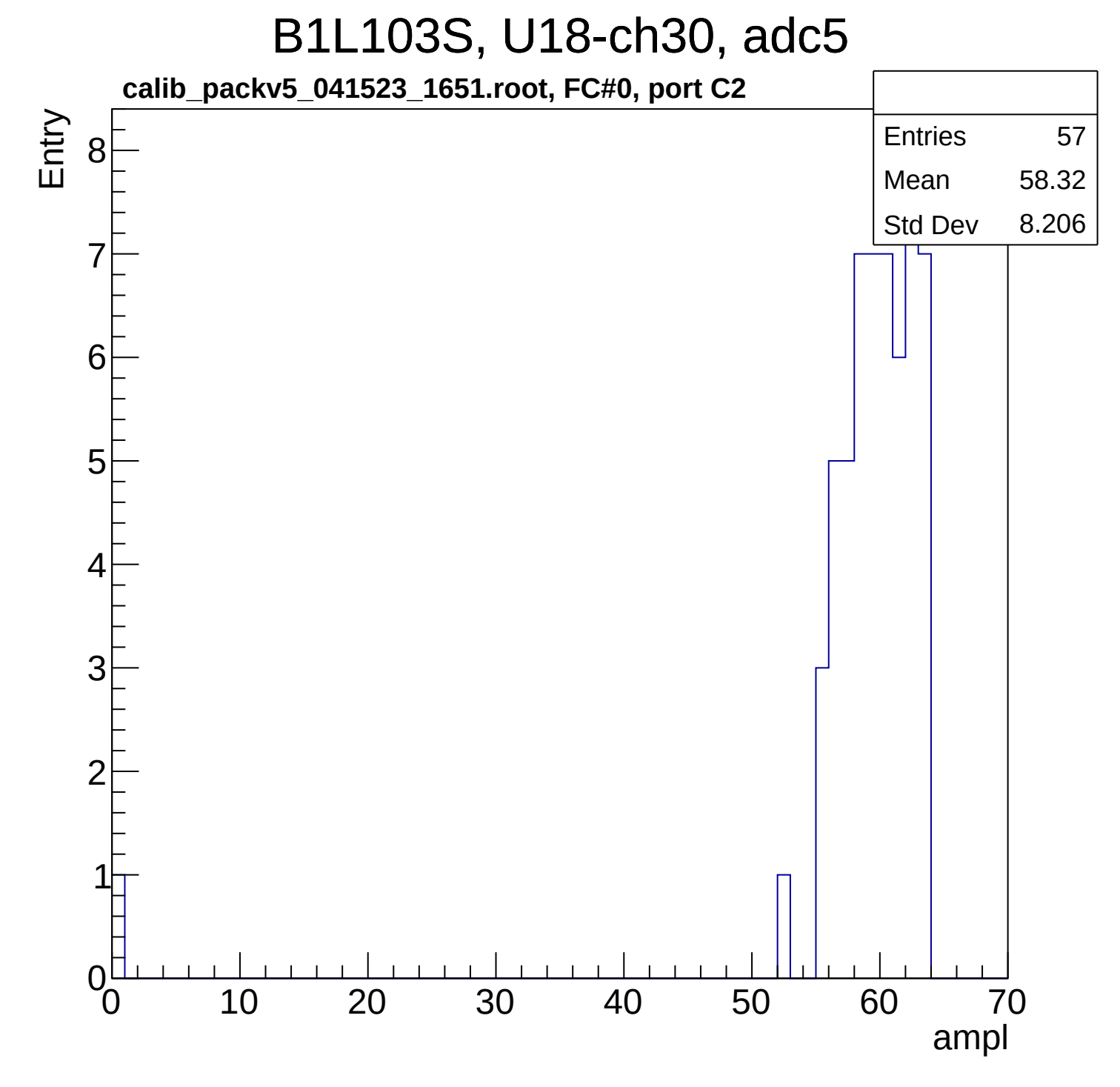
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch30, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 58.32
Std Dev 8.206
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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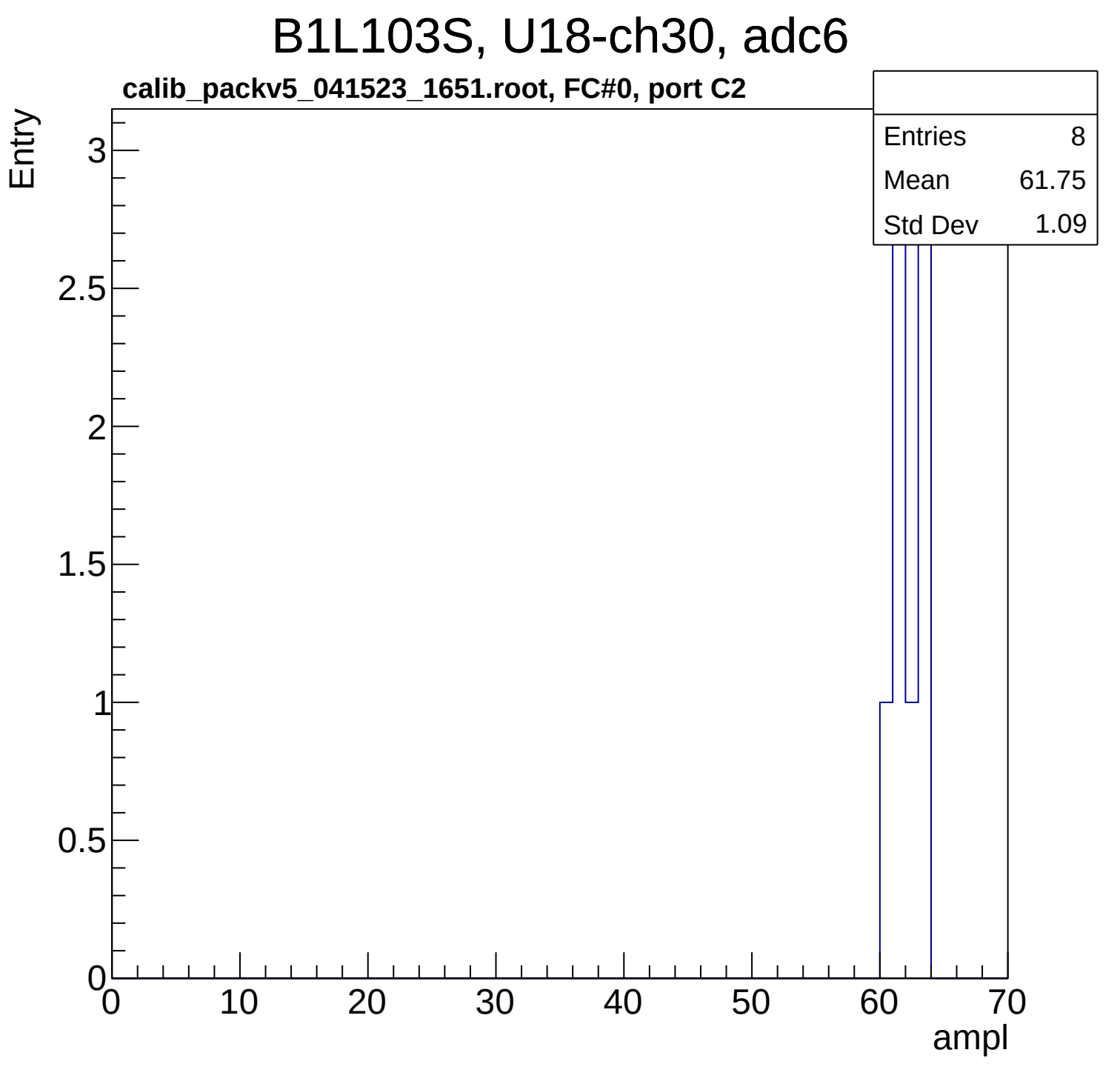
40
50
60
70


B1L103S, U18-ch30, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 61.75
Std Dev 1.09
Entry
ampl
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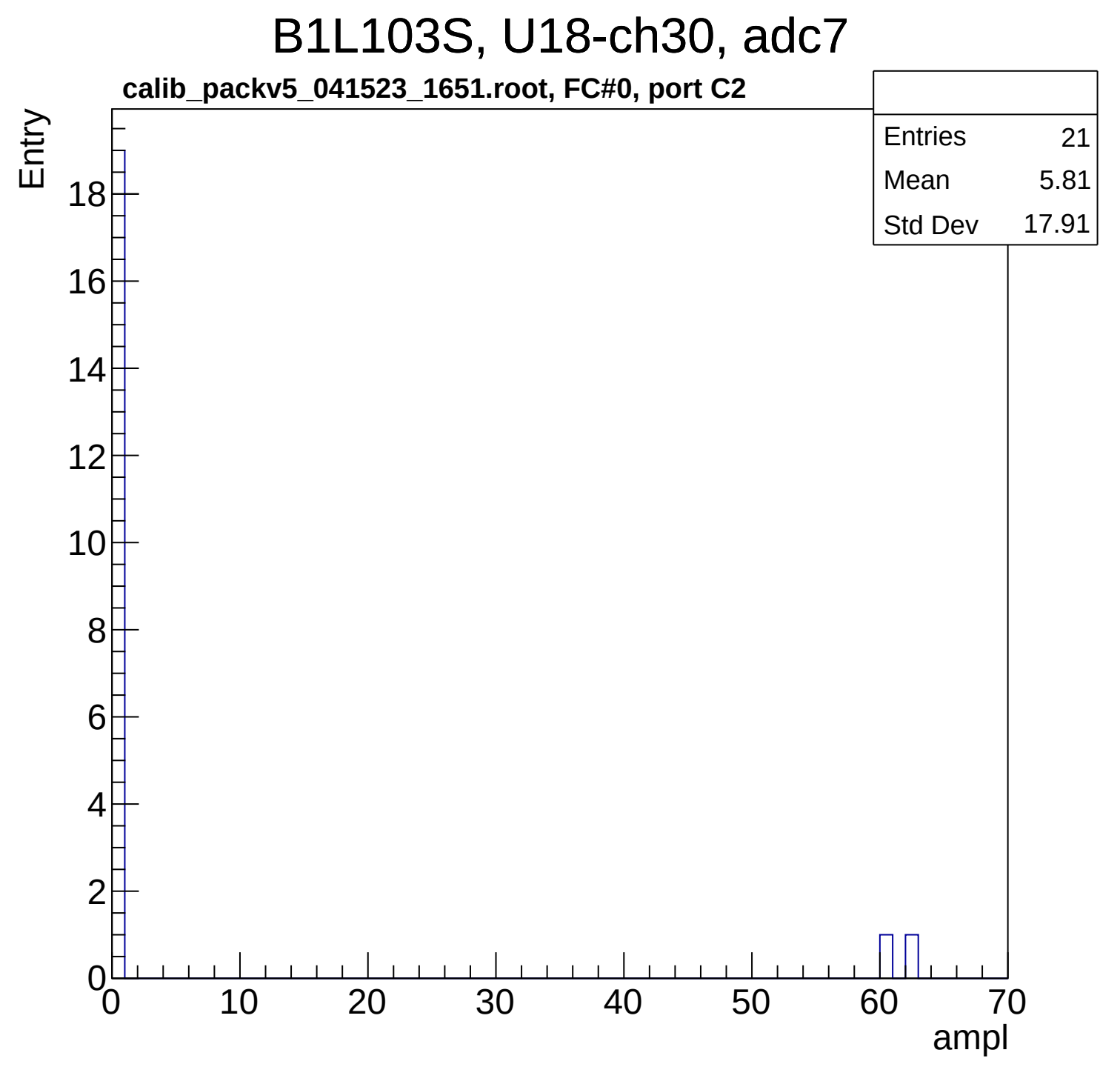
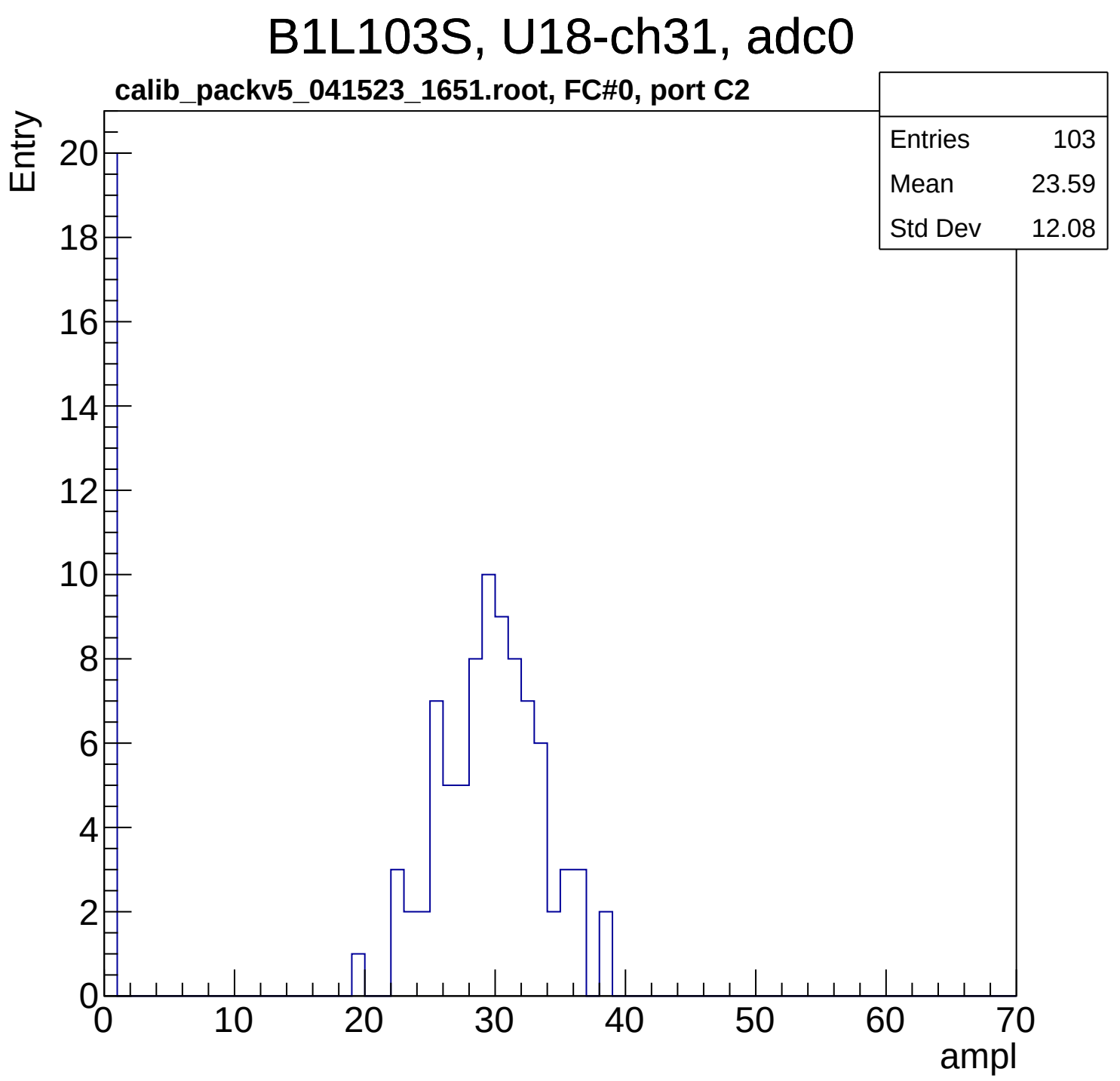
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U18-ch30, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 5.81
Std Dev 17.91
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch31, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 103
Mean 23.59
Std Dev 12.08
Entry
ampl
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6
8
10
12
14
16
18
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0
10
20
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40
50
60
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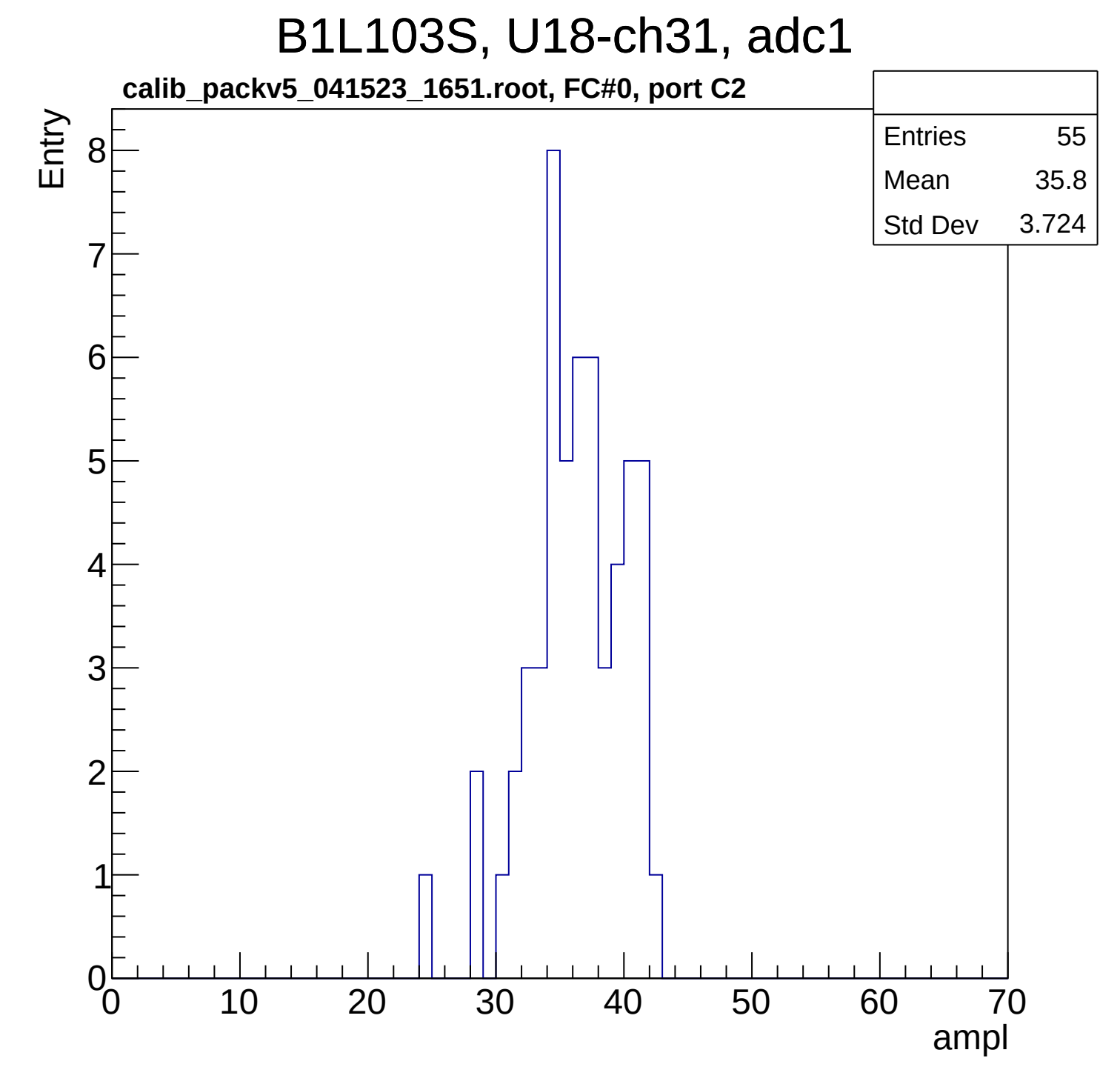
B1L103S, U18-ch31, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 35.8
Std Dev 3.724
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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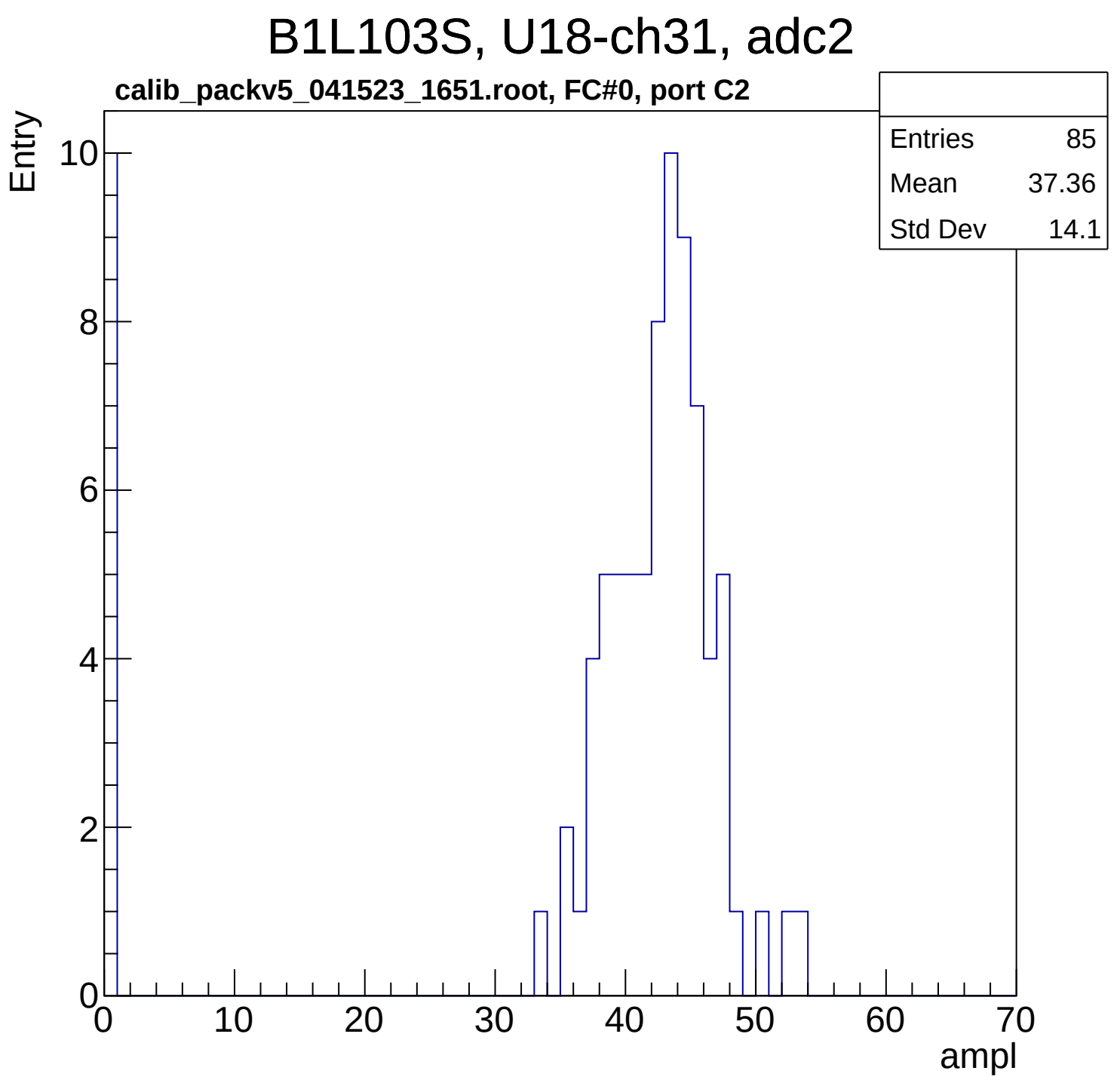
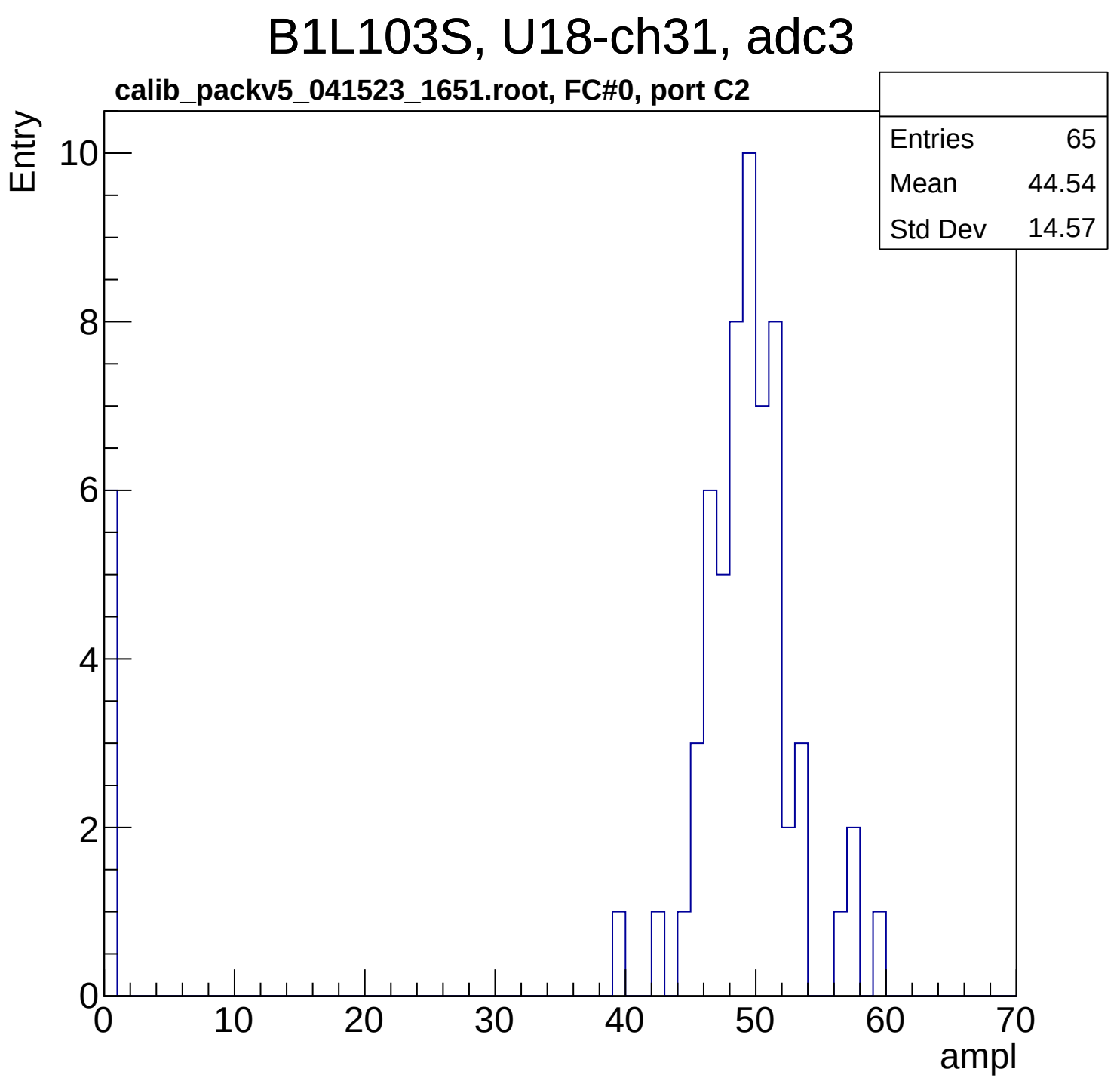
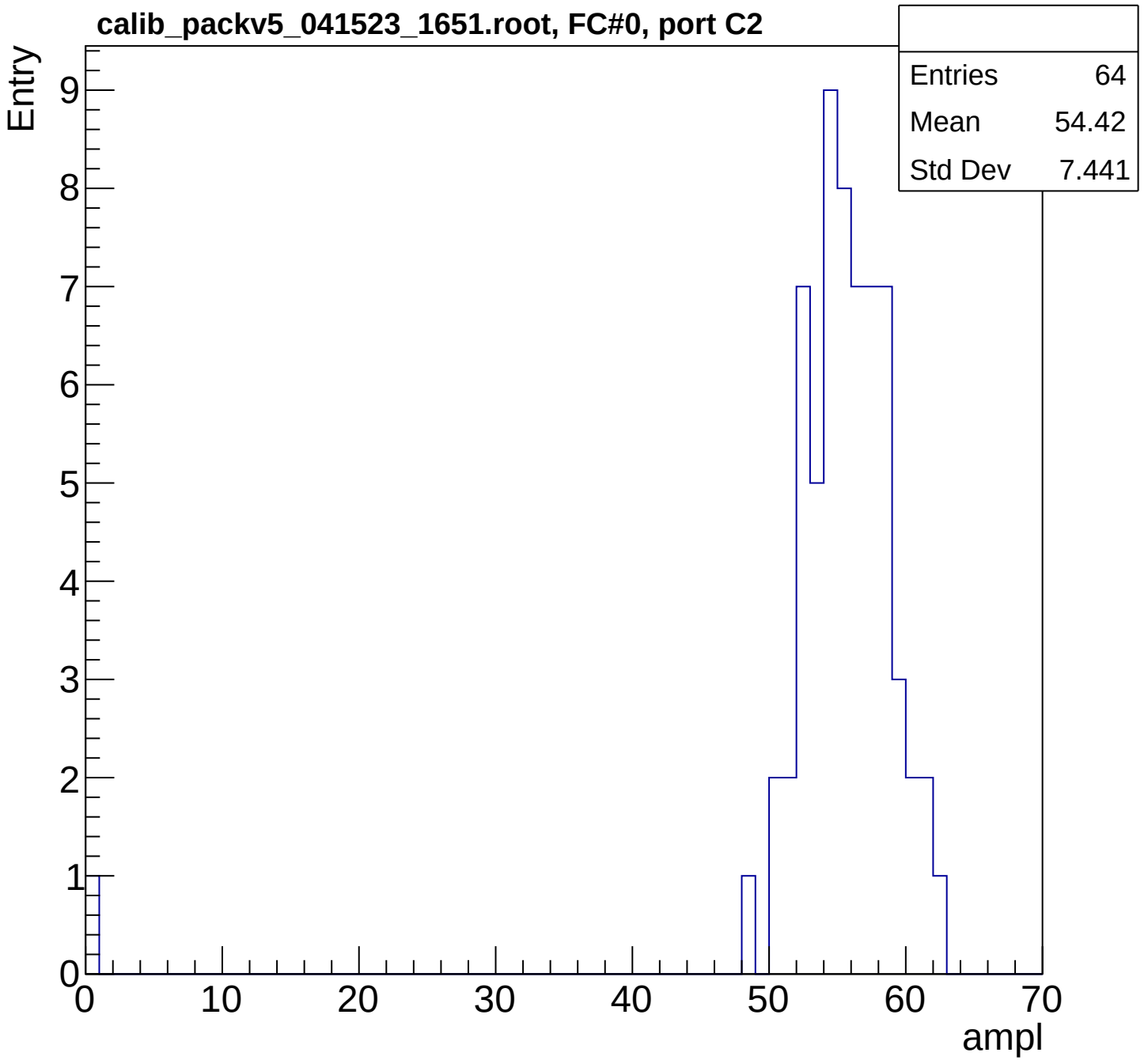

B1L103S, U18-ch31, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 37.36
Std Dev 14.1
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U18-ch31, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 44.54
Std Dev 14.57
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U18-ch31, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 54.42
Std Dev 7.441
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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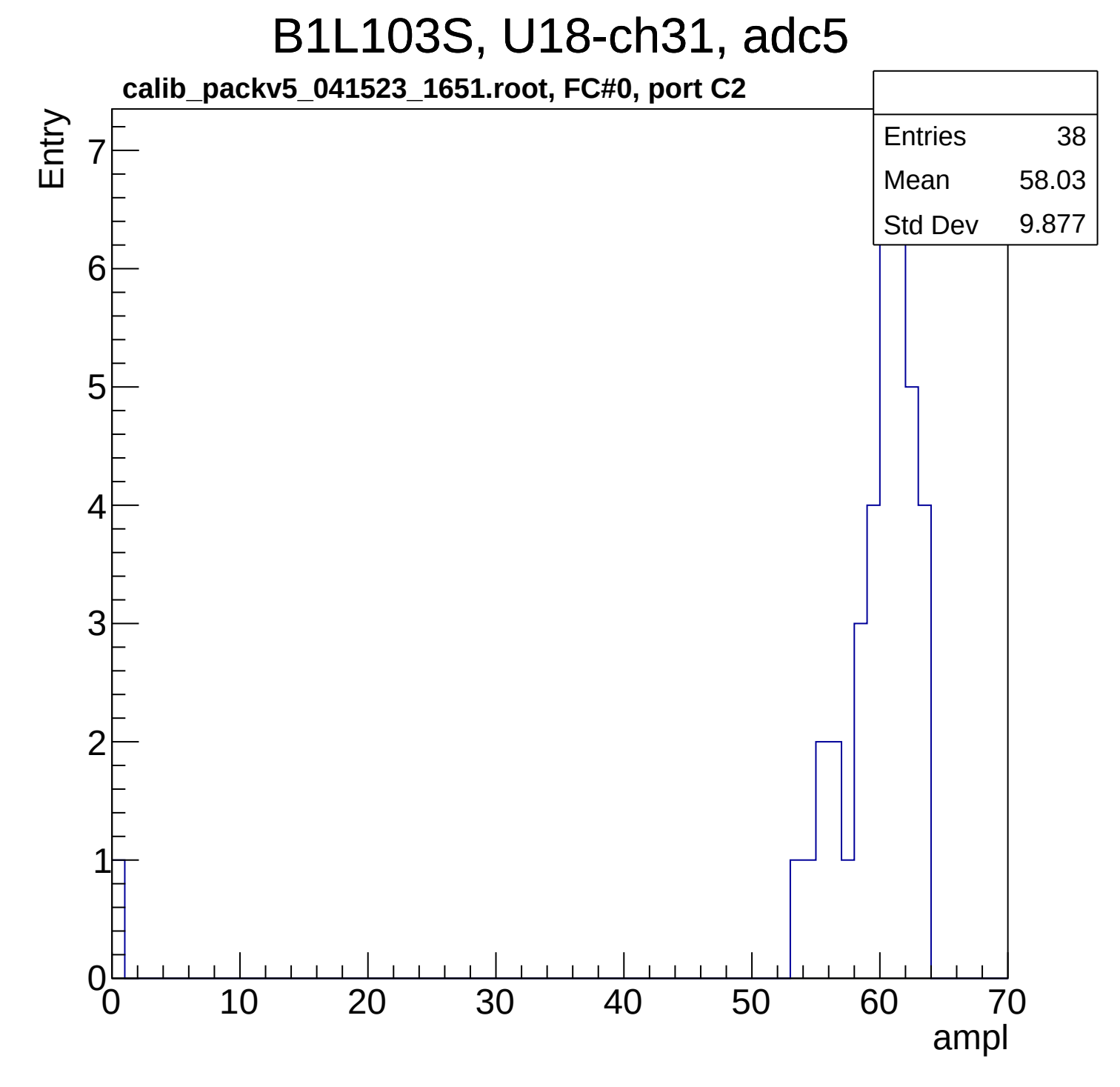
40
50
60
70


B1L103S, U18-ch31, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 38
Mean 58.03
Std Dev 9.877
Entry
ampl
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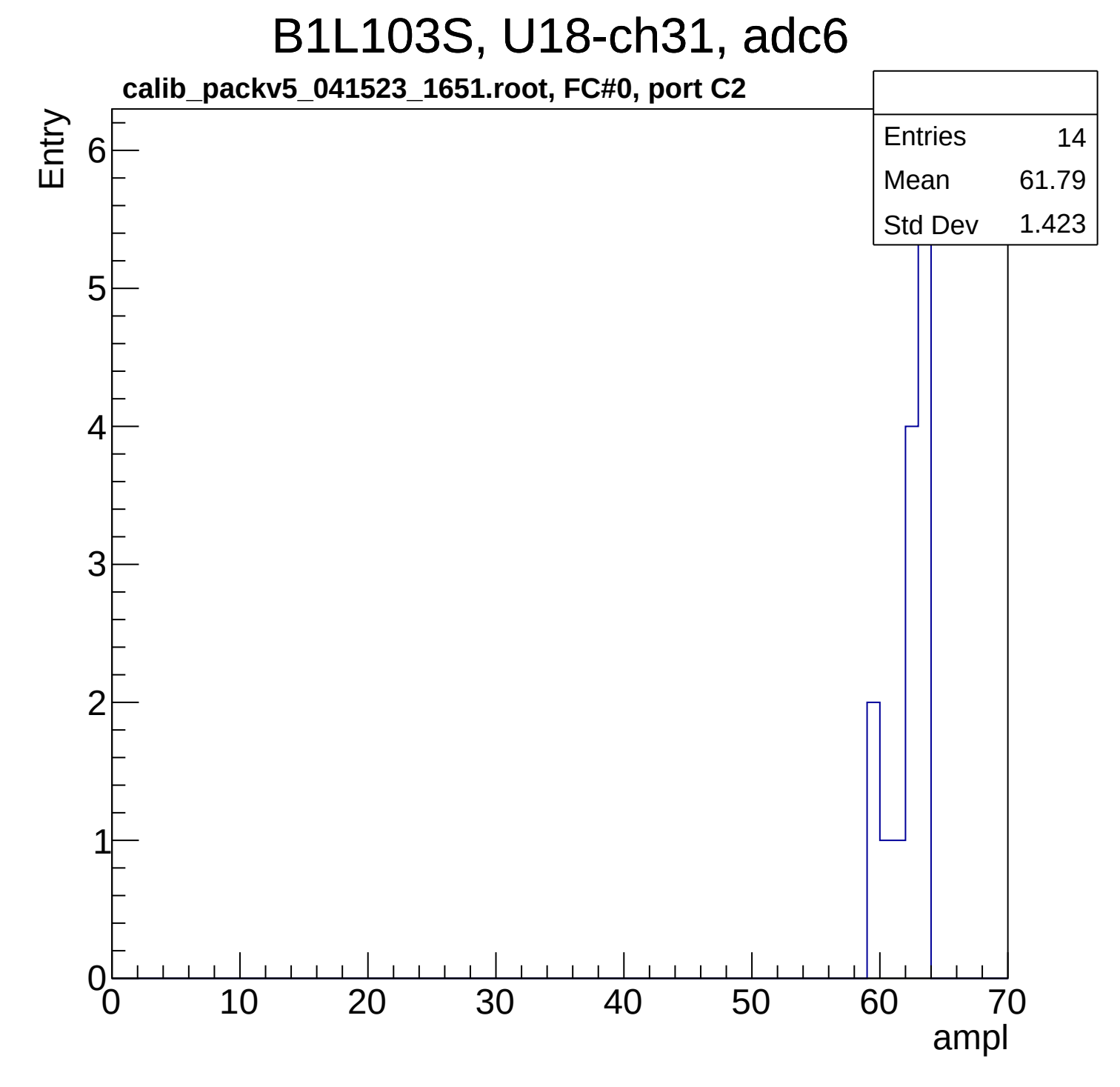
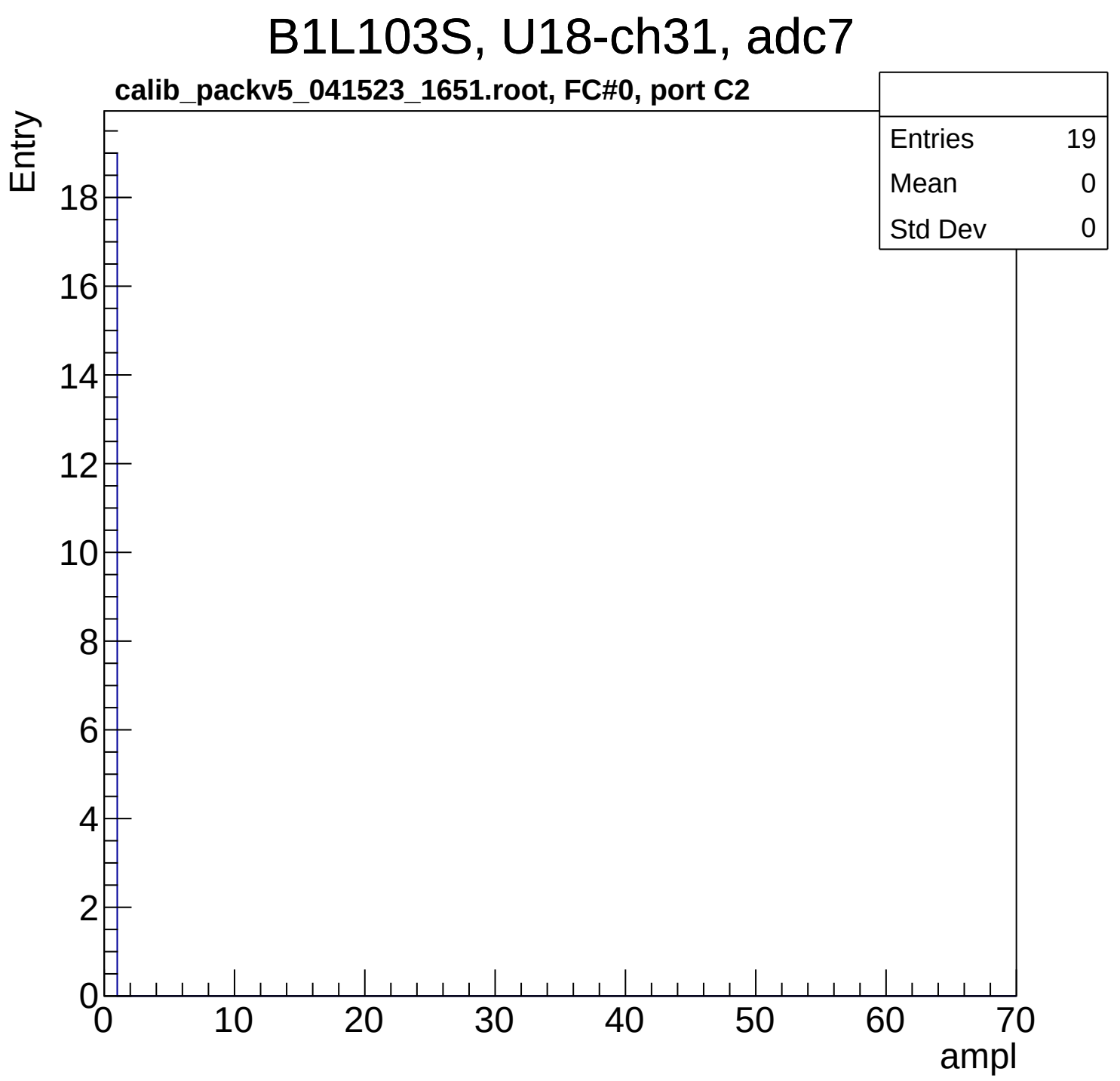
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U18-ch31, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 14
Mean 61.79
Std Dev 1.423
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U18-ch31, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
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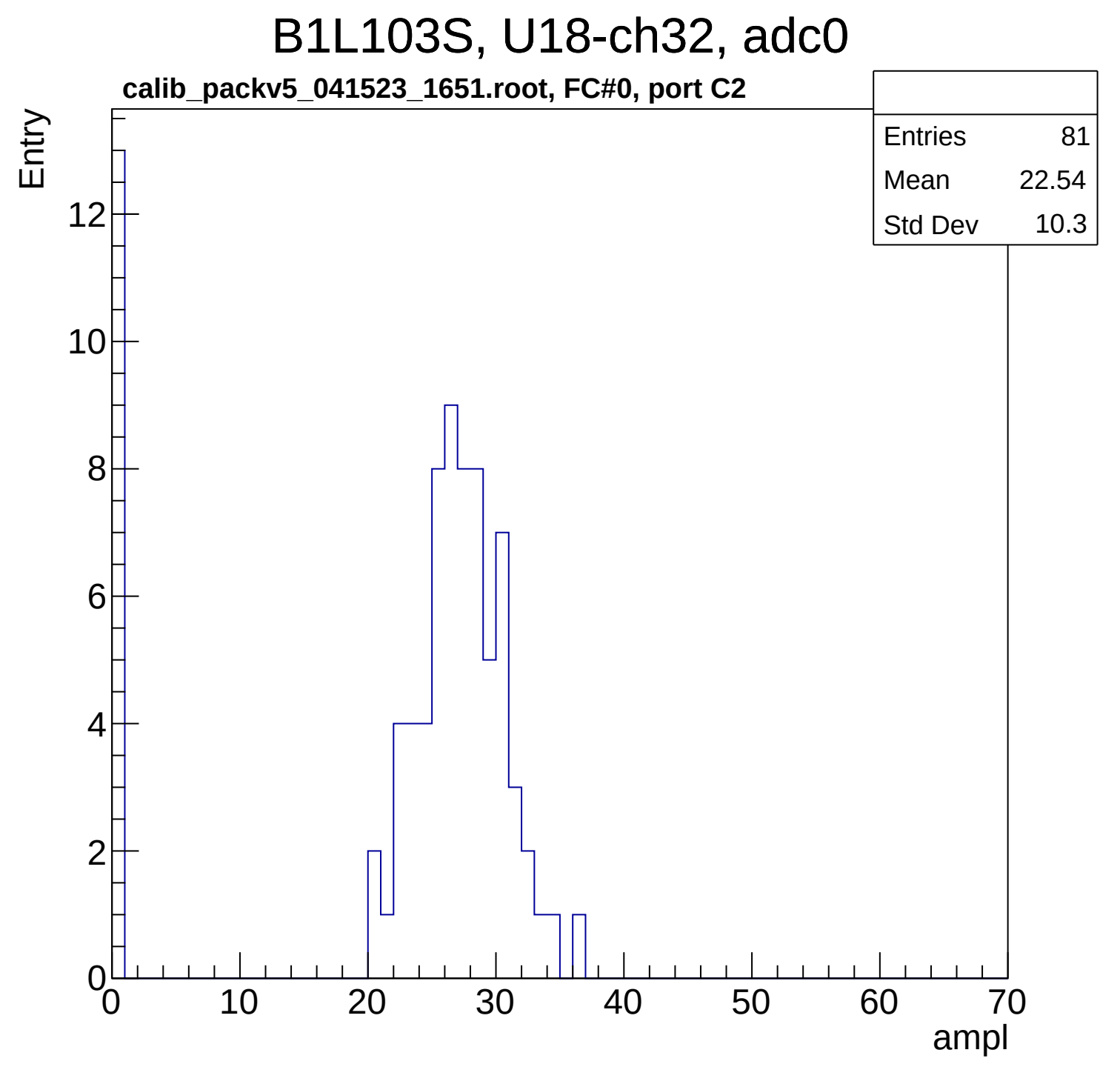
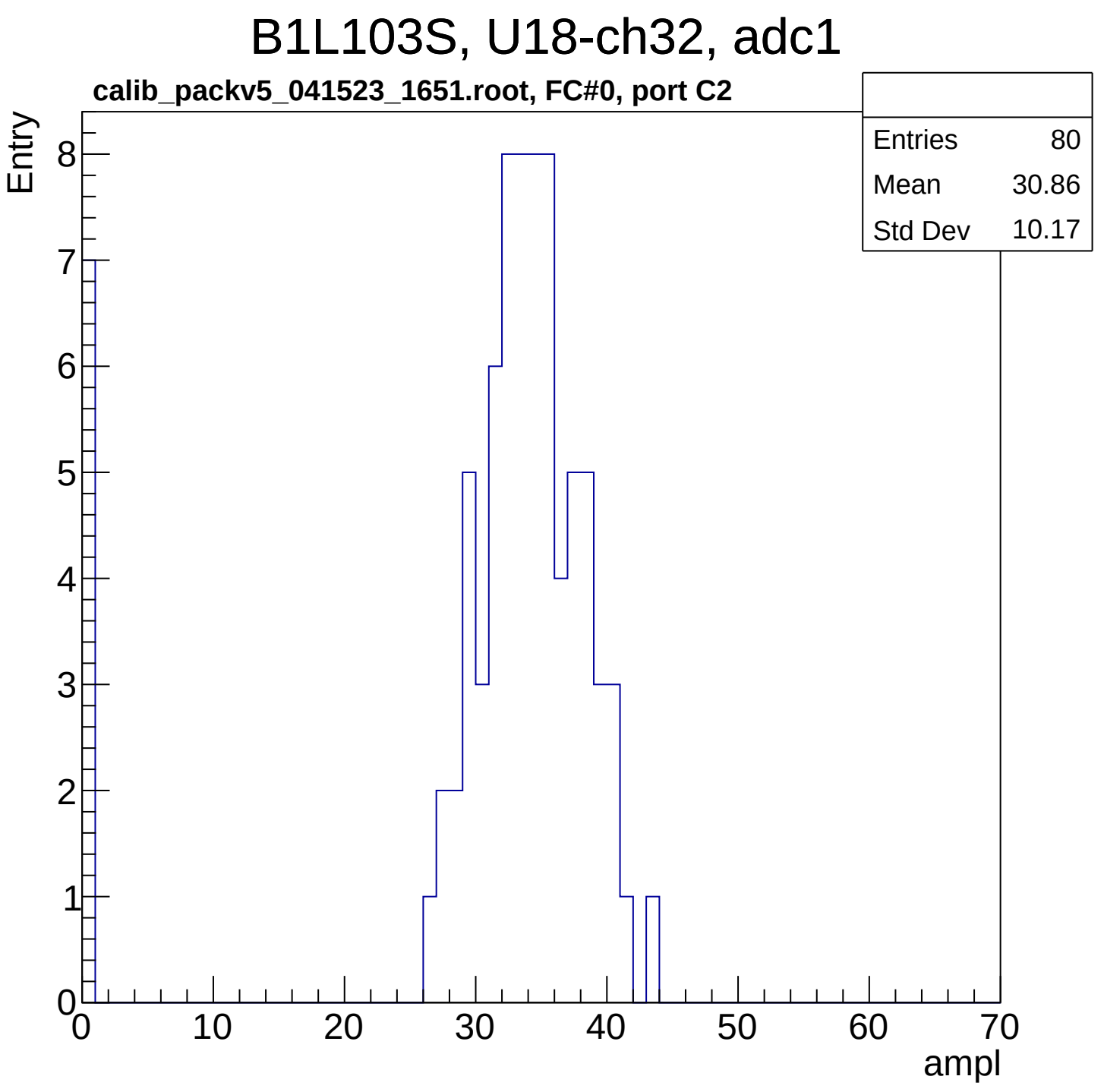
50
60
70
ampl


B1L103S, U18-ch32, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 22.54
Std Dev 10.3
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch32, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 30.86
Std Dev 10.17
Entry
ampl
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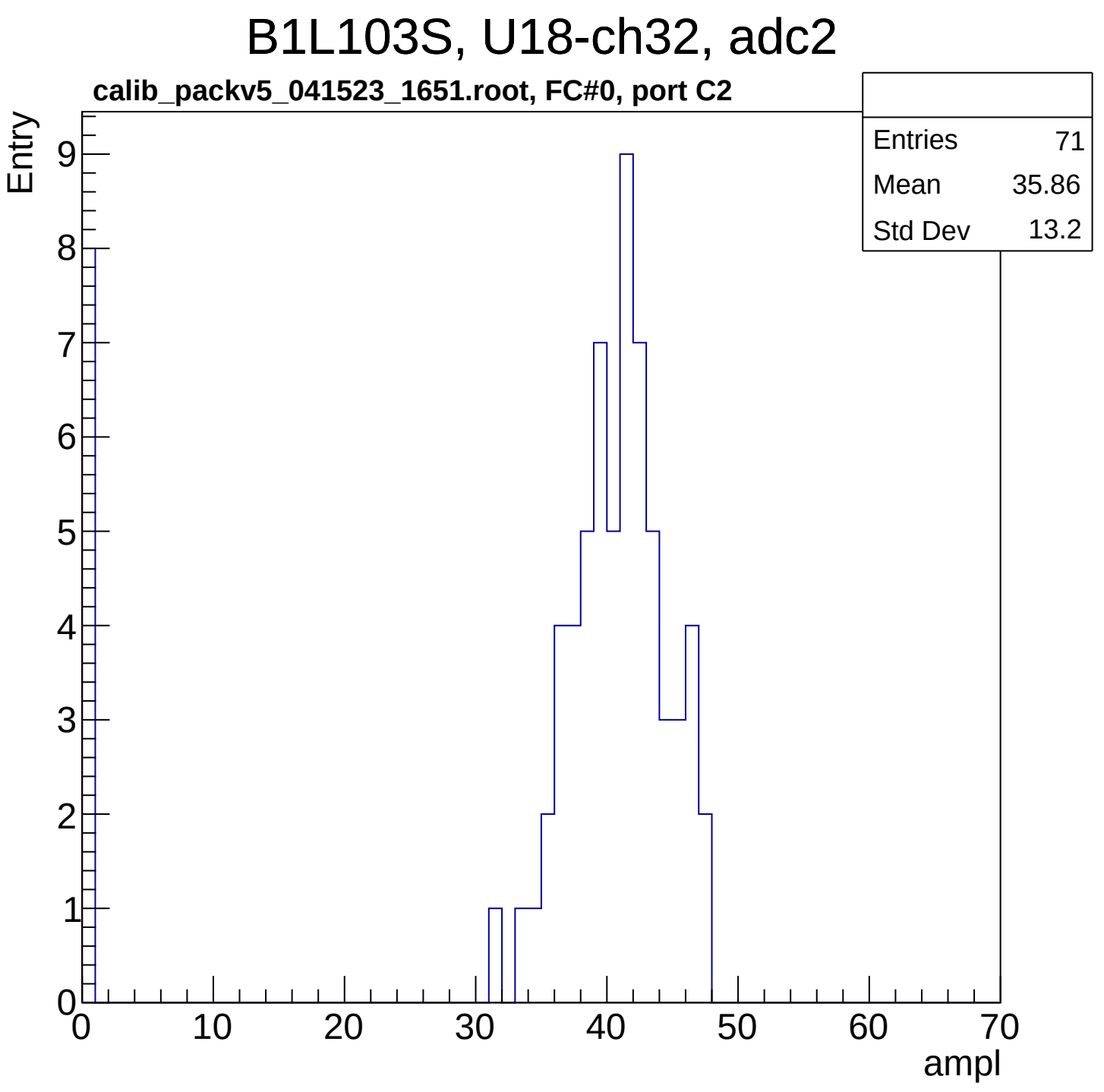
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch32, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 35.86
Std Dev 13.2
Entry
ampl
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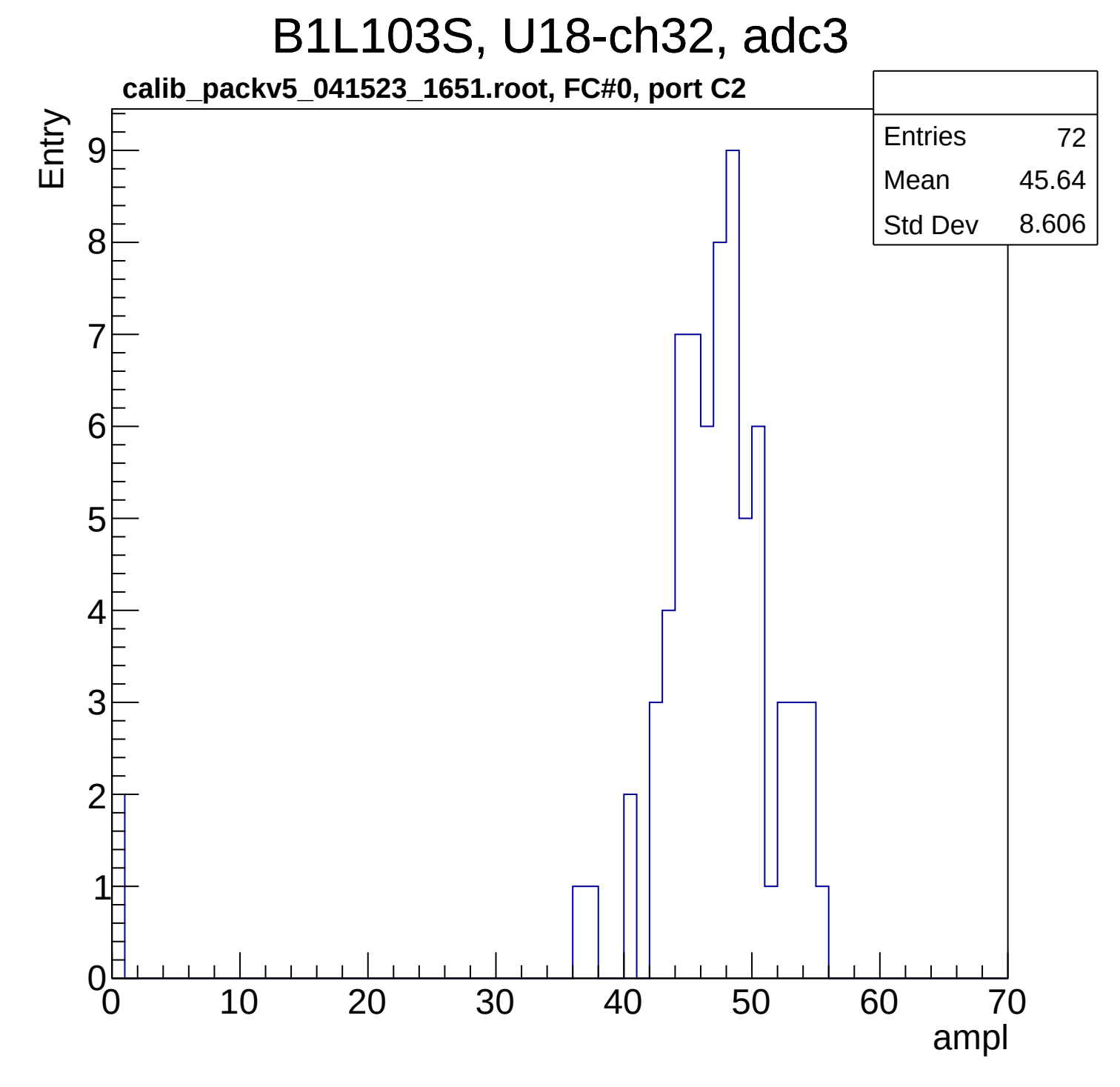
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U18-ch32, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 45.64
Std Dev 8.606
Entry
ampl
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2
3
4
5
6
7
8
9
0
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40
50
60
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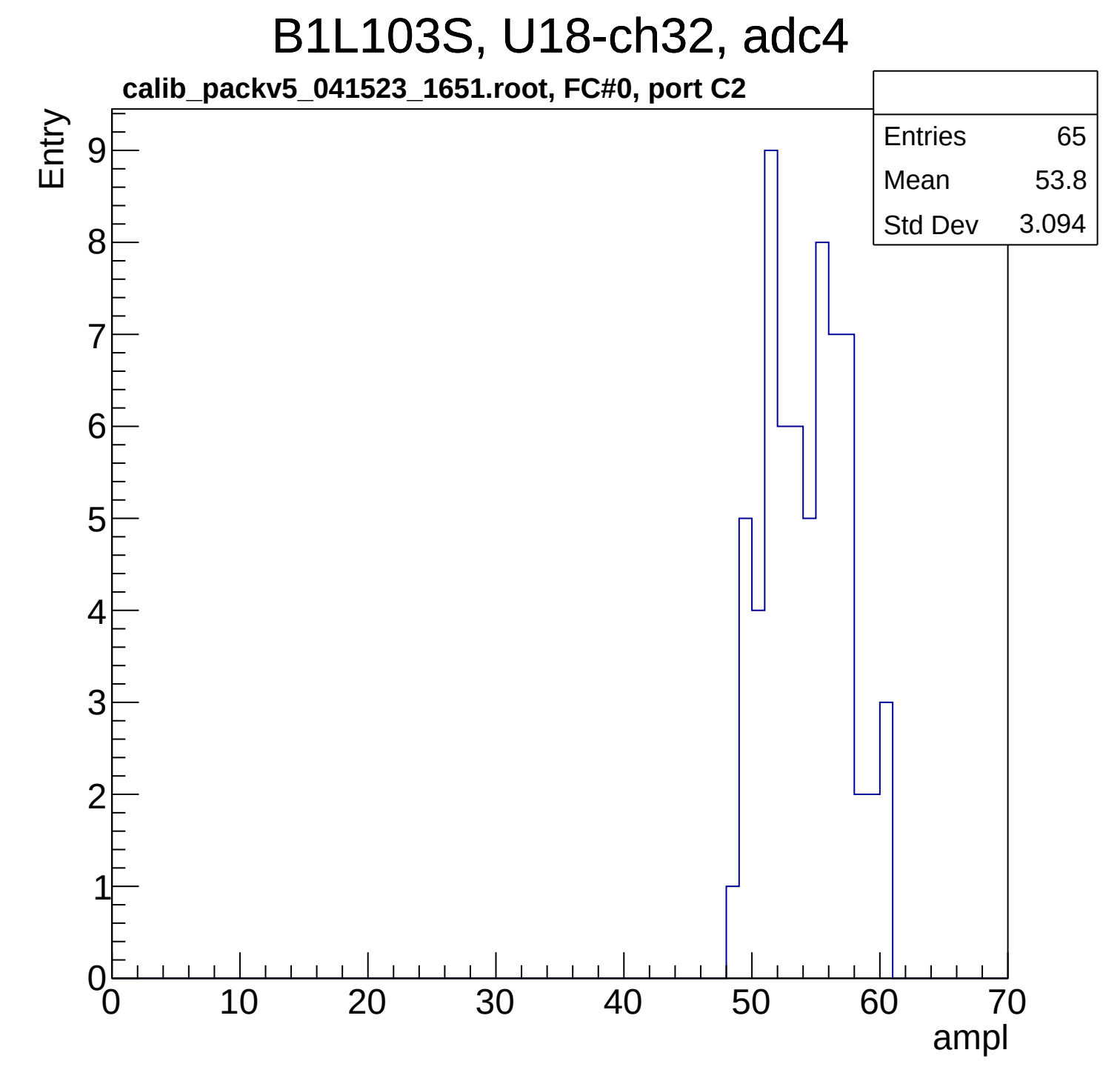
B1L103S, U18-ch32, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 53.8
Std Dev 3.094
Entry
ampl
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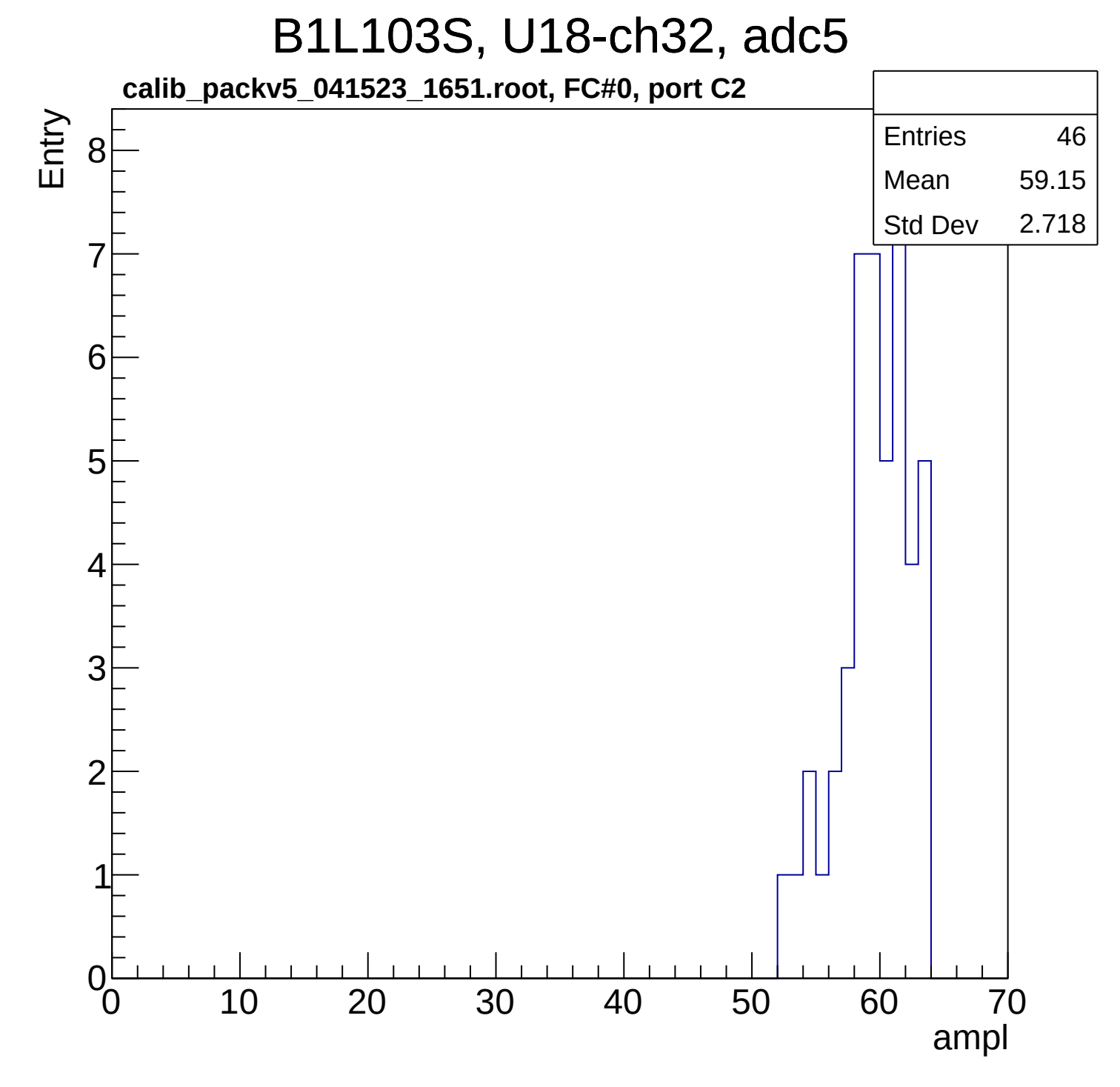
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U18-ch32, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 59.15
Std Dev 2.718
Entry
ampl
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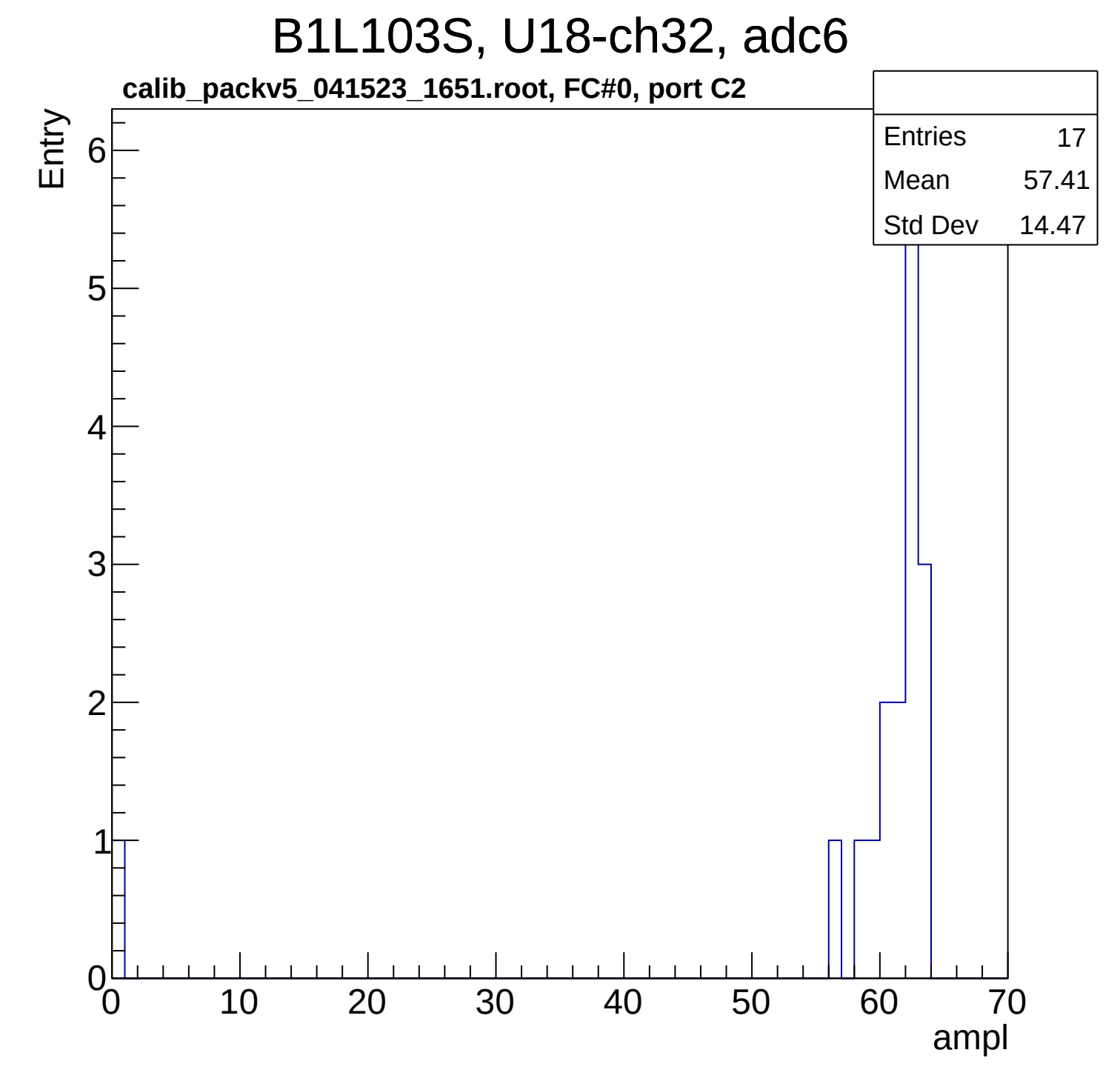
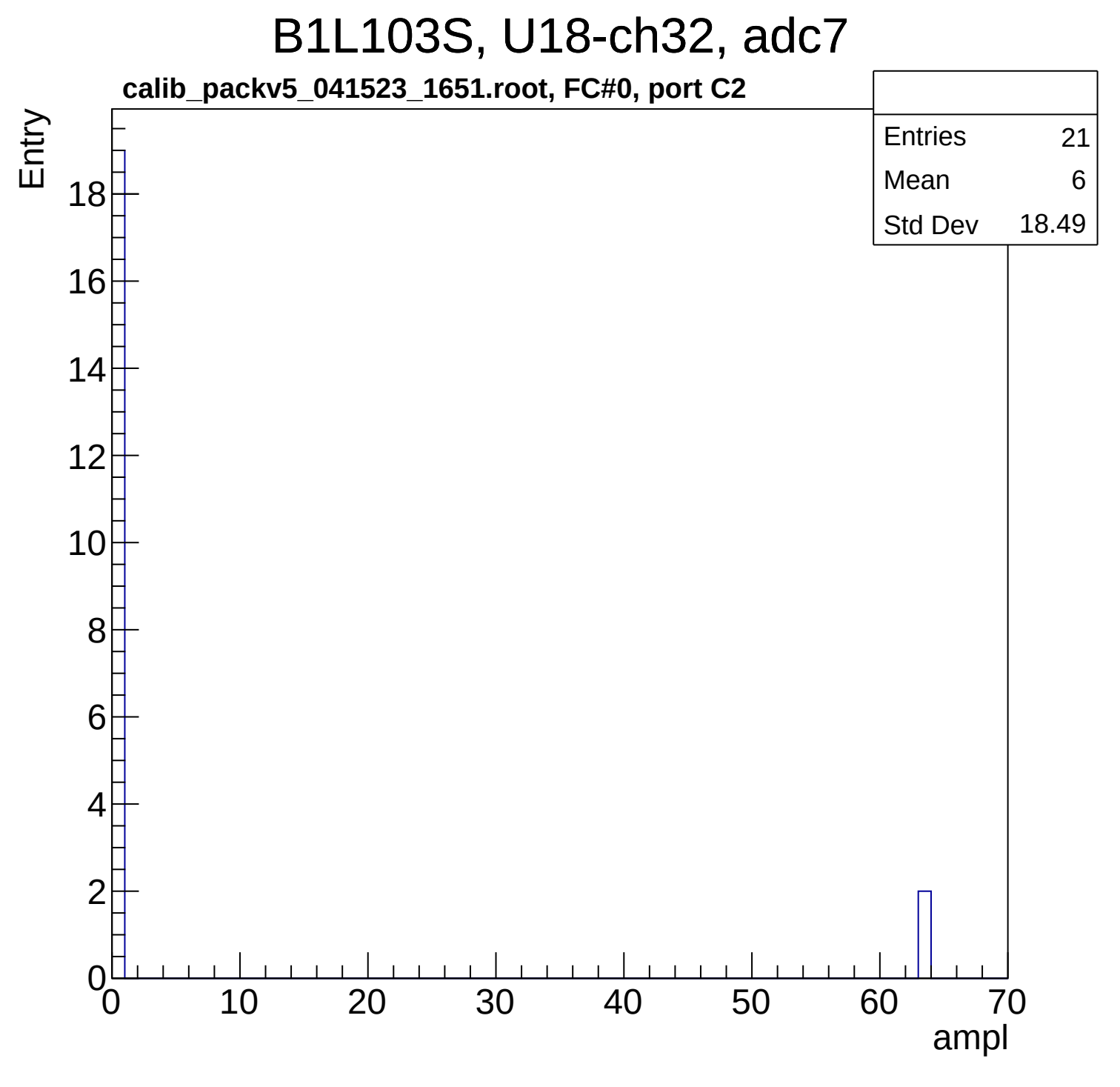
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch32, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 17
Mean 57.41
Std Dev 14.47
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U18-ch32, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 6
Std Dev 18.49
Entry
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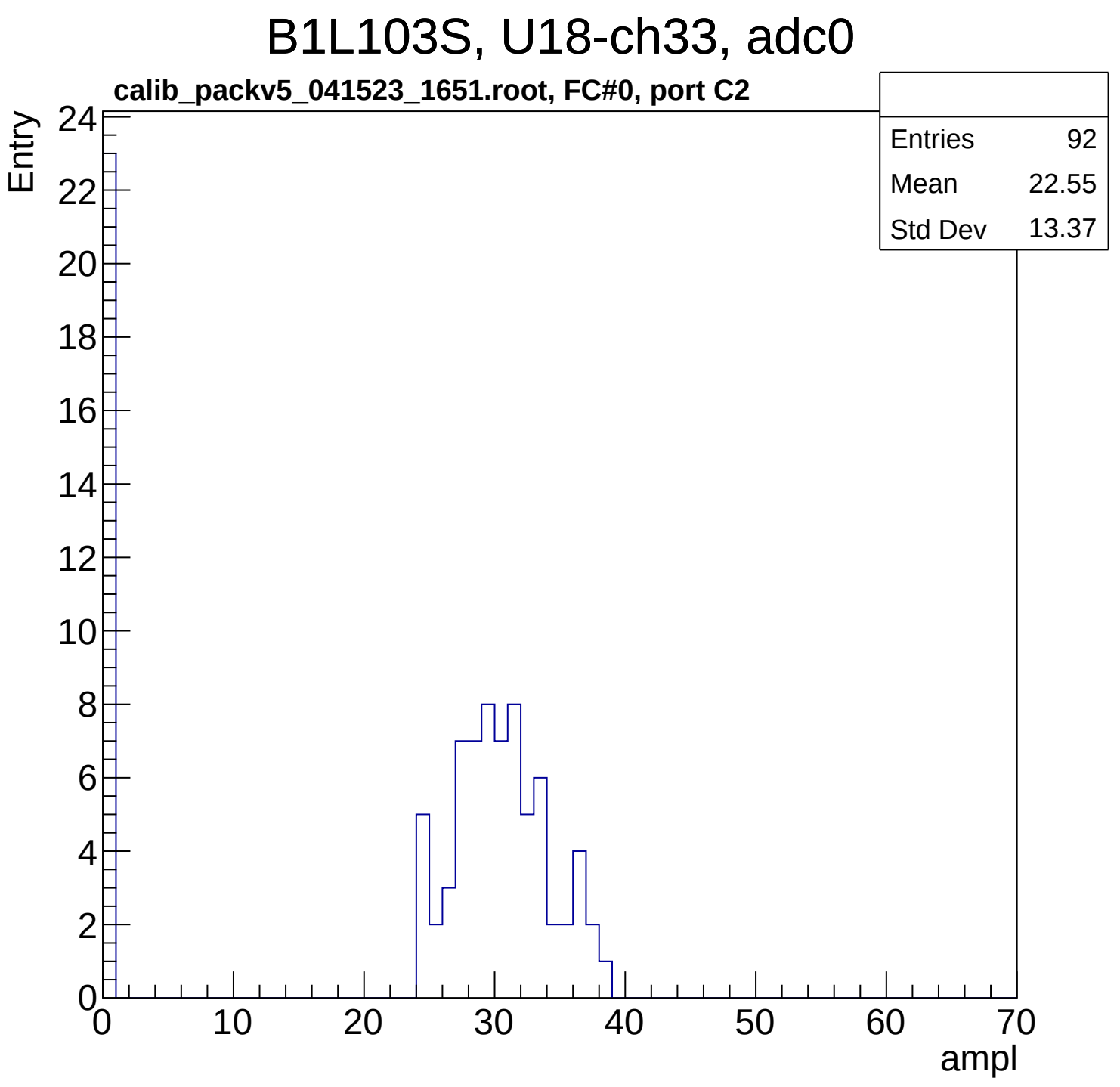
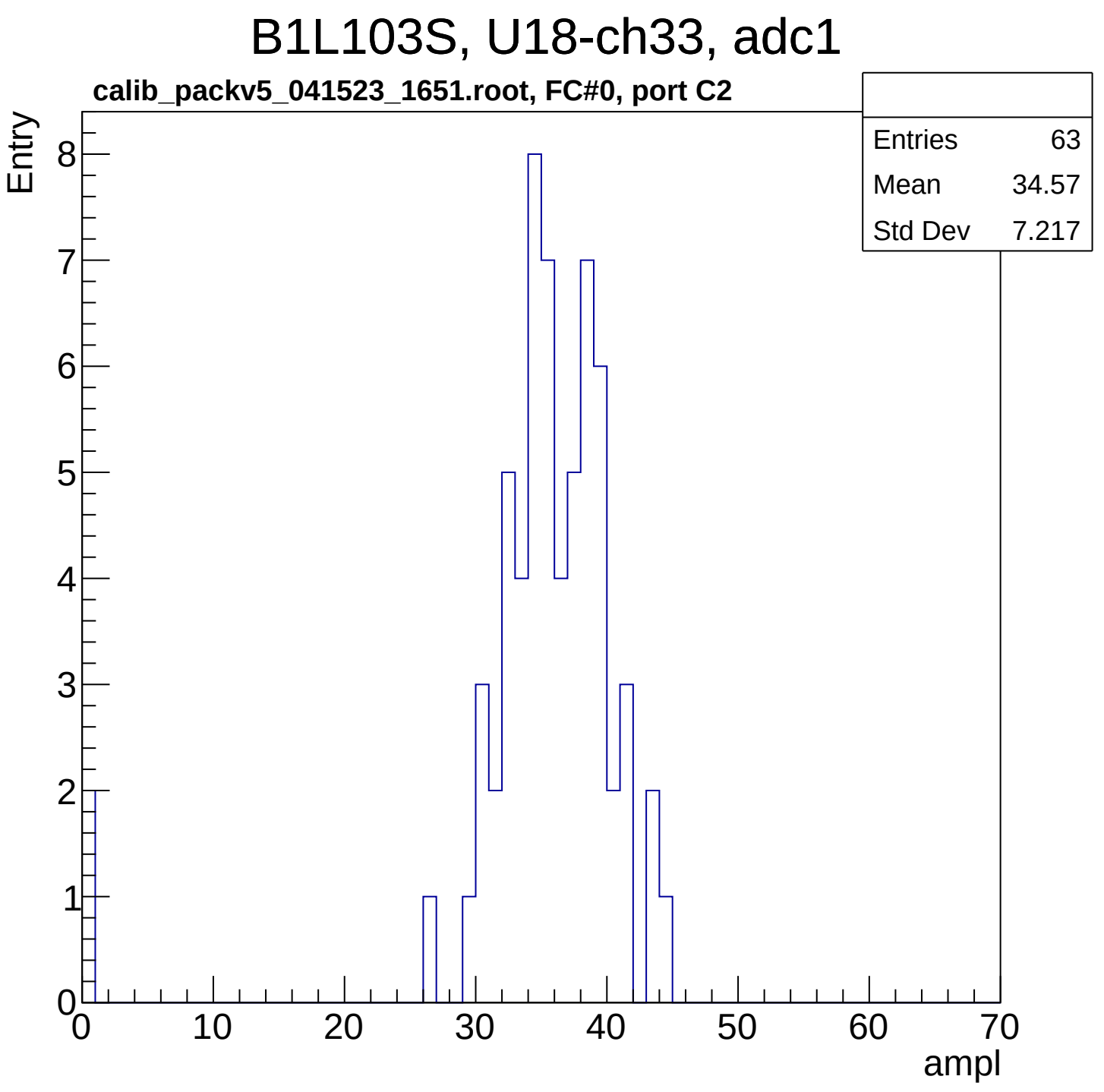
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch33, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 92
Mean 22.55
Std Dev 13.37
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
22
24
0
10
20
30
40
50
60
70


B1L103S, U18-ch33, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 34.57
Std Dev 7.217
Entry
ampl
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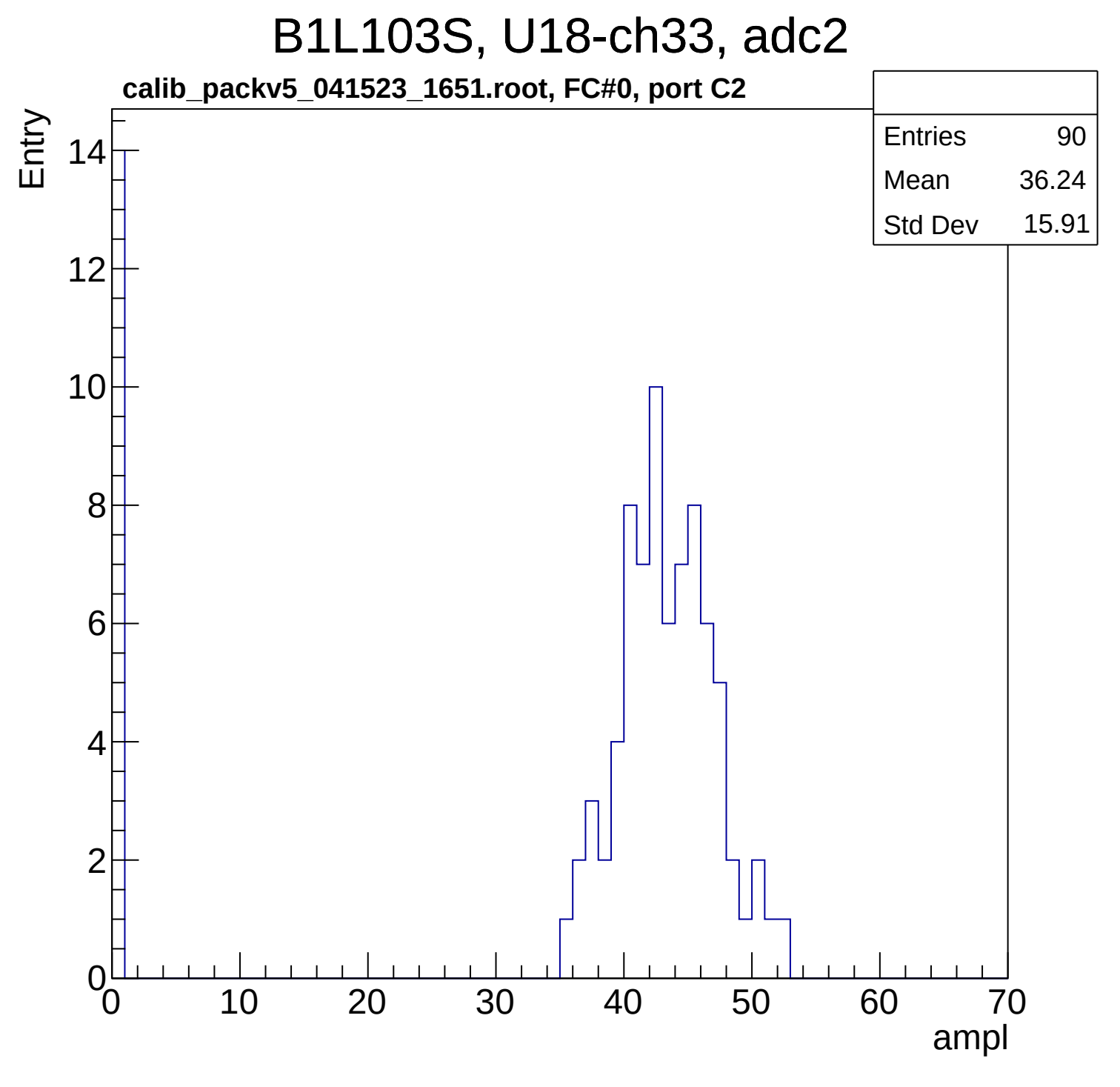
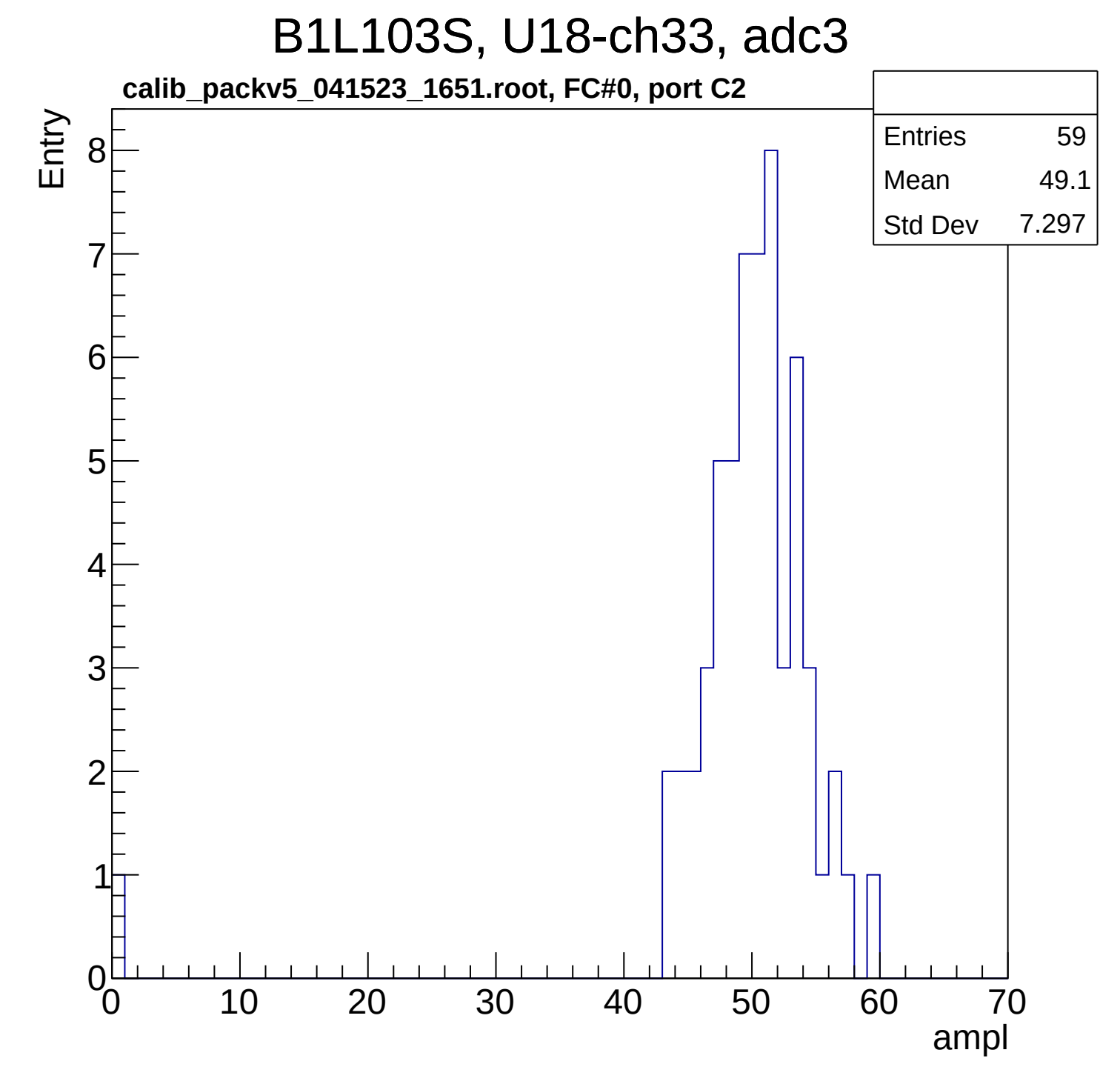
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch33, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 90
Mean 36.24
Std Dev 15.91
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch33, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 49.1
Std Dev 7.297
Entry
ampl
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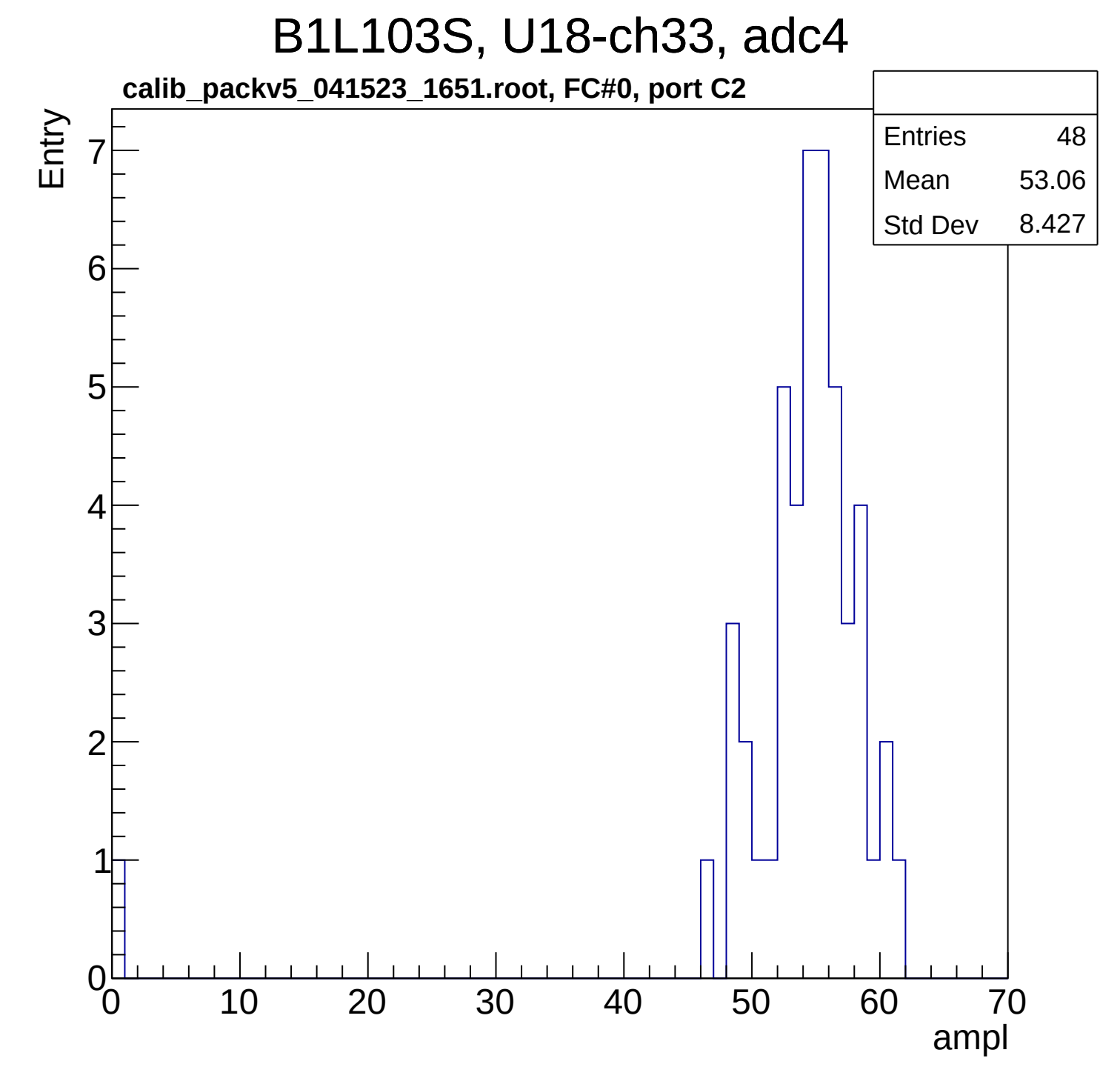
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch33, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 53.06
Std Dev 8.427
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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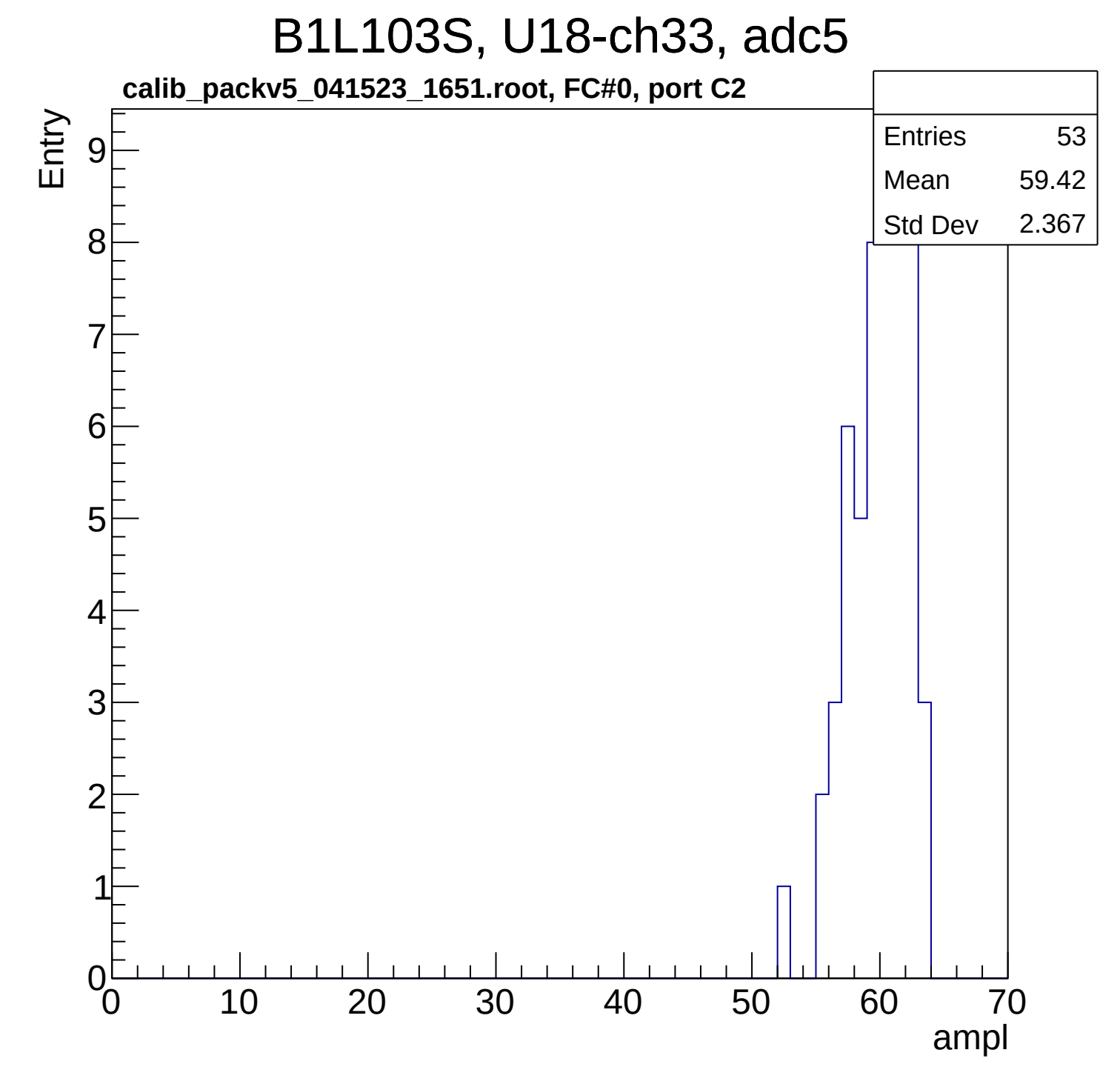
B1L103S, U18-ch33, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 59.42
Std Dev 2.367
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
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40
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60
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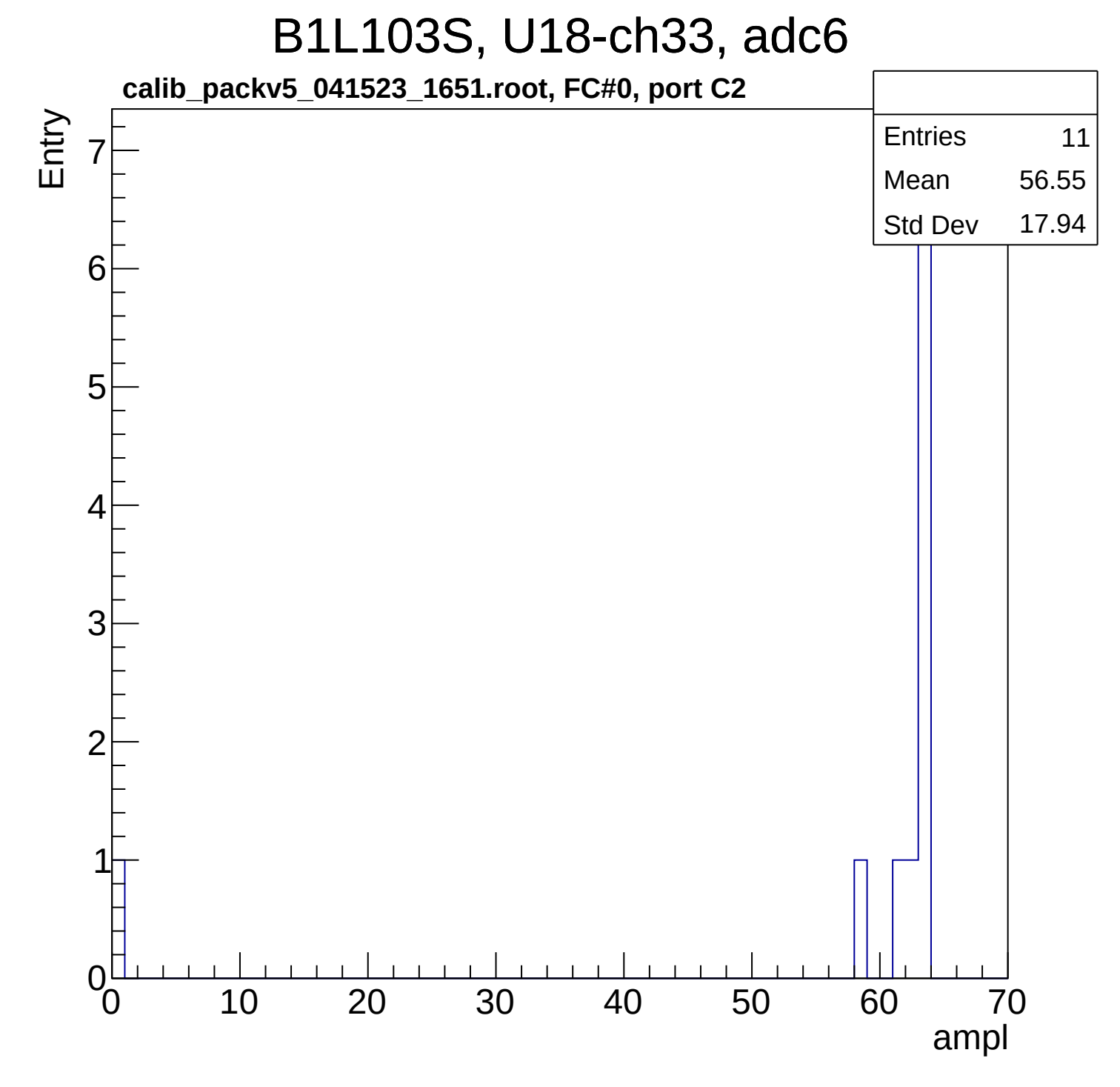
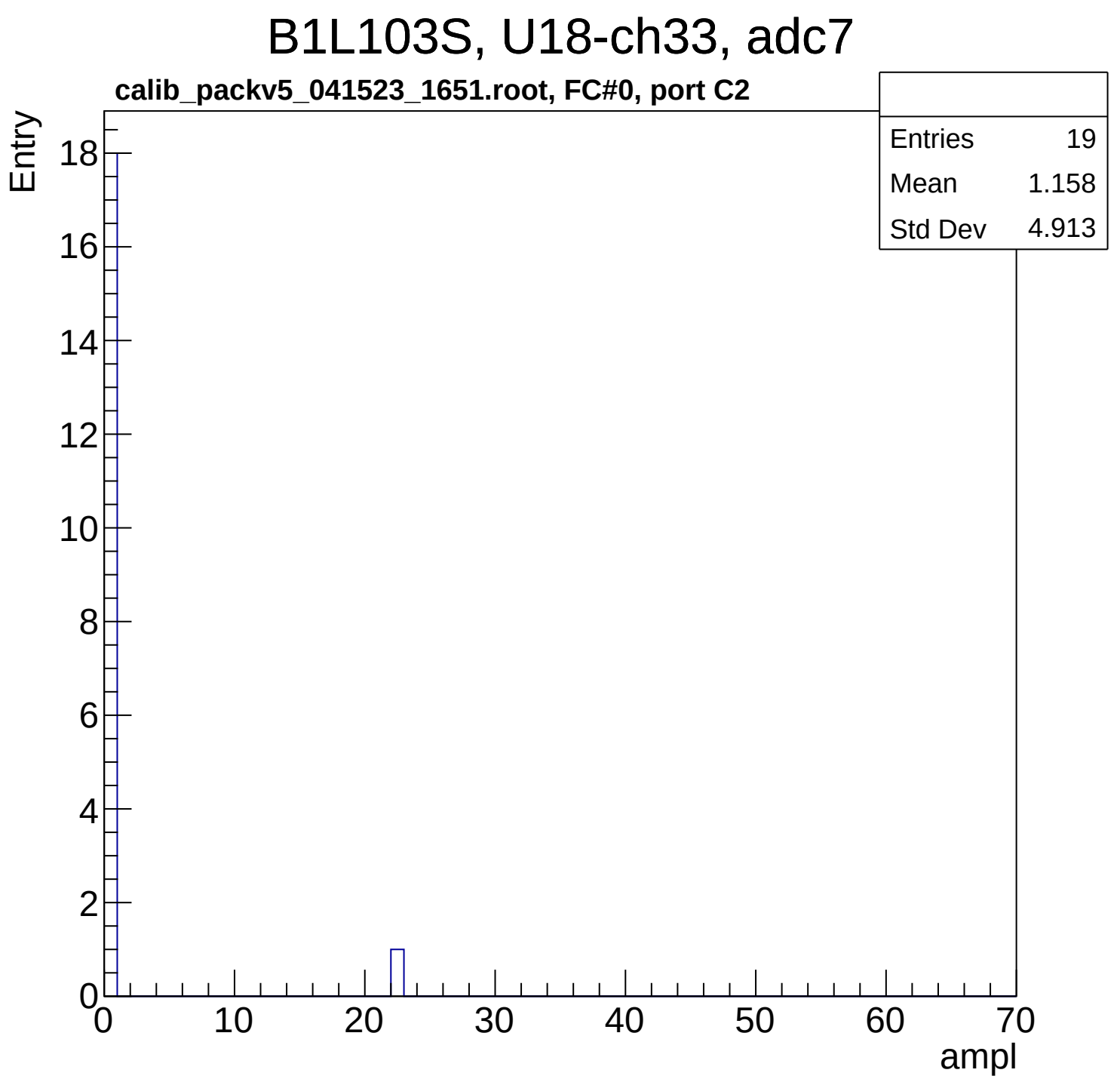

B1L103S, U18-ch33, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 56.55
Std Dev 17.94
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U18-ch33, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.158
Std Dev 4.913
Entry
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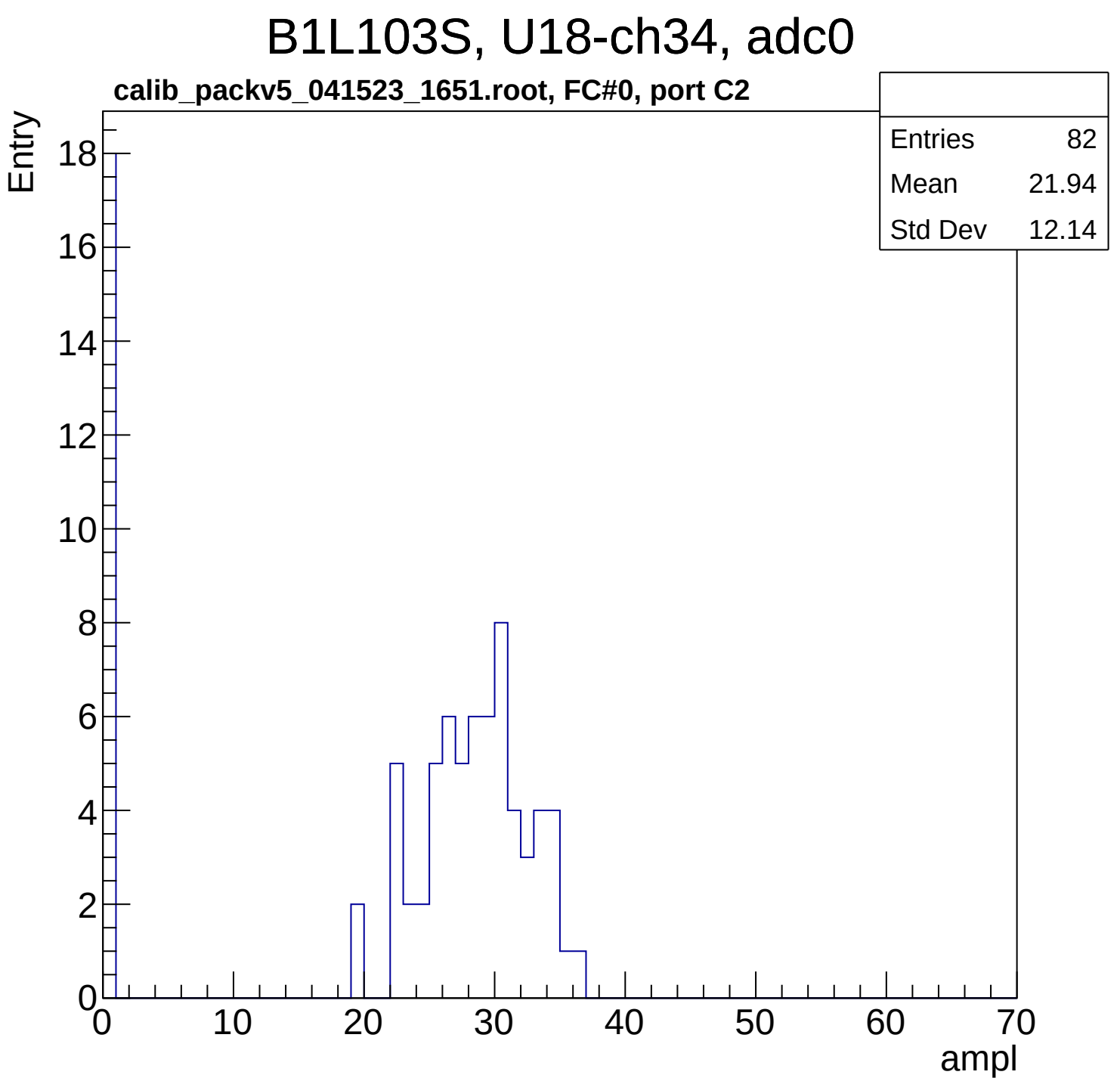
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch34, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 21.94
Std Dev 12.14
Entry
0
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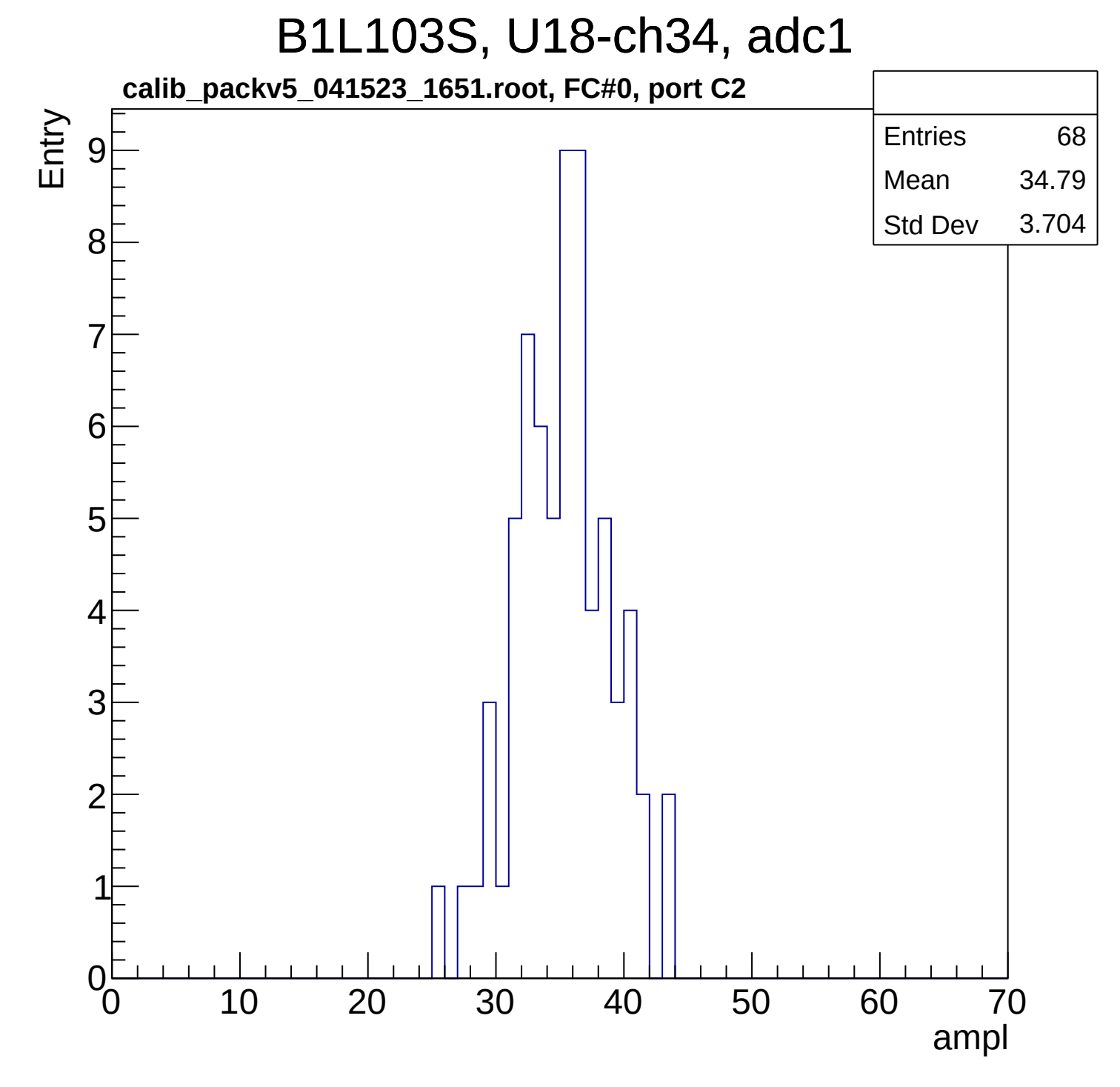
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch34, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 34.79
Std Dev 3.704
Entry
ampl
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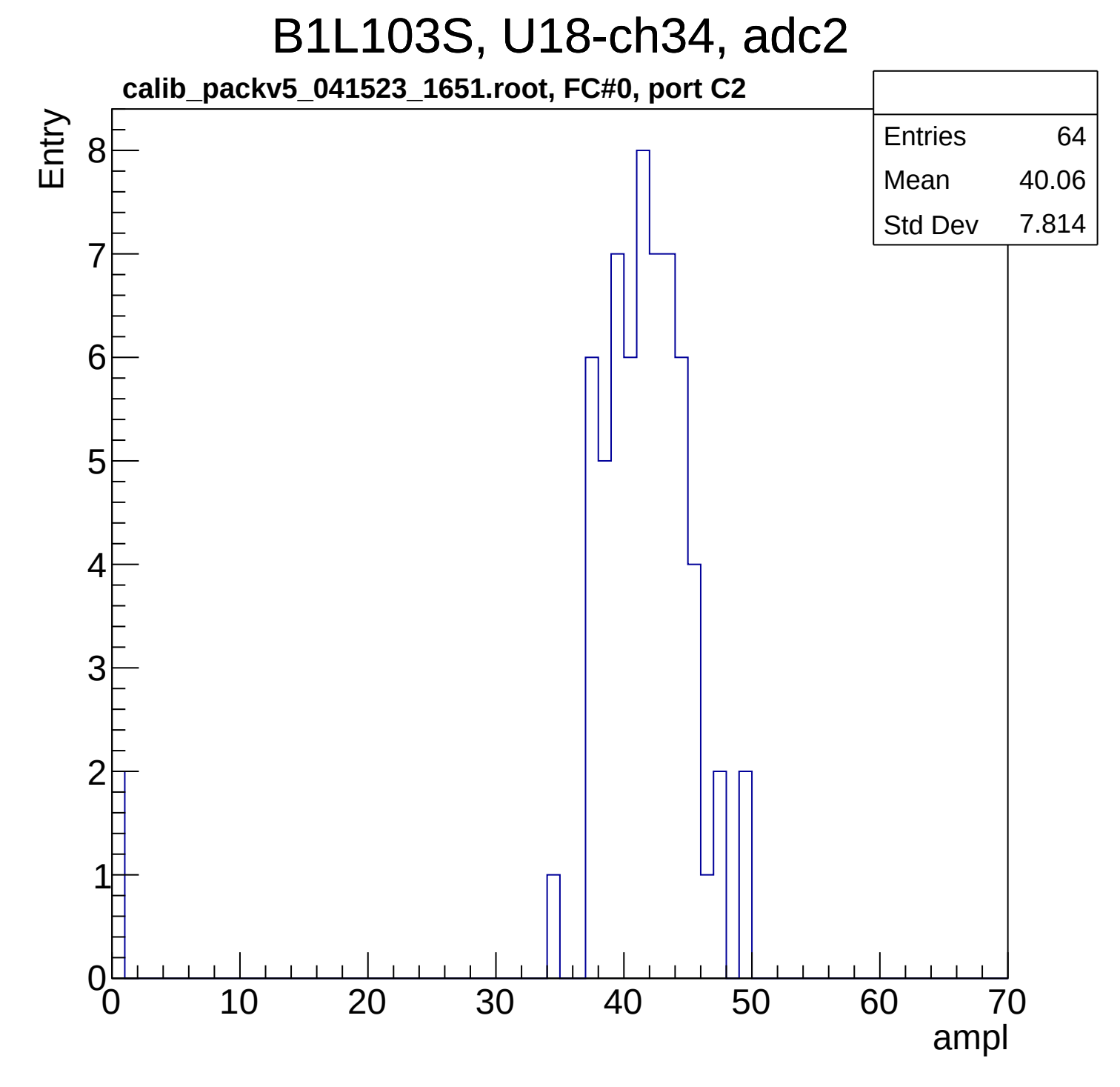
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U18-ch34, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 40.06
Std Dev 7.814
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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40
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60
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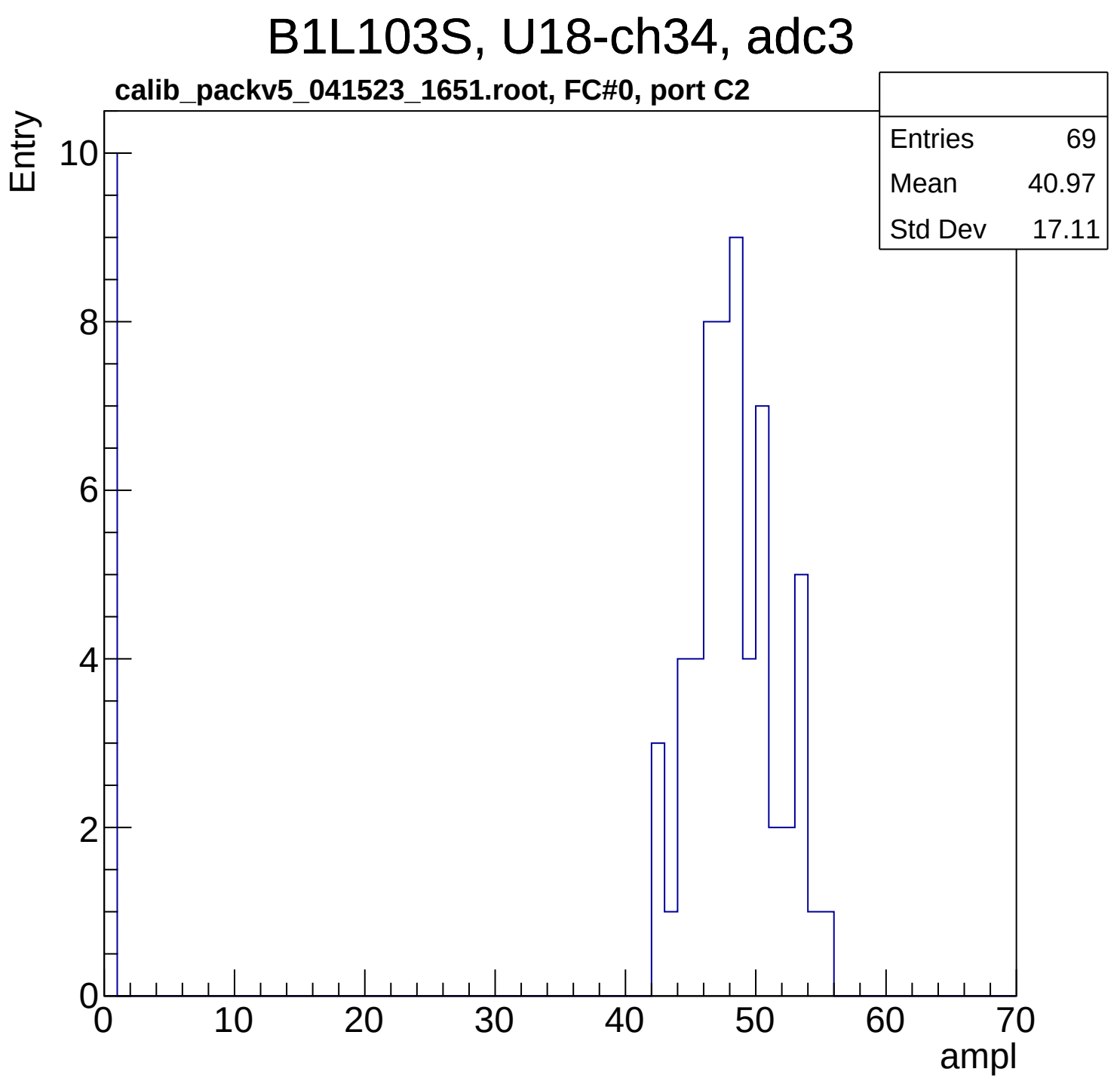
B1L103S, U18-ch34, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 40.97
Std Dev 17.11
Entry
ampl
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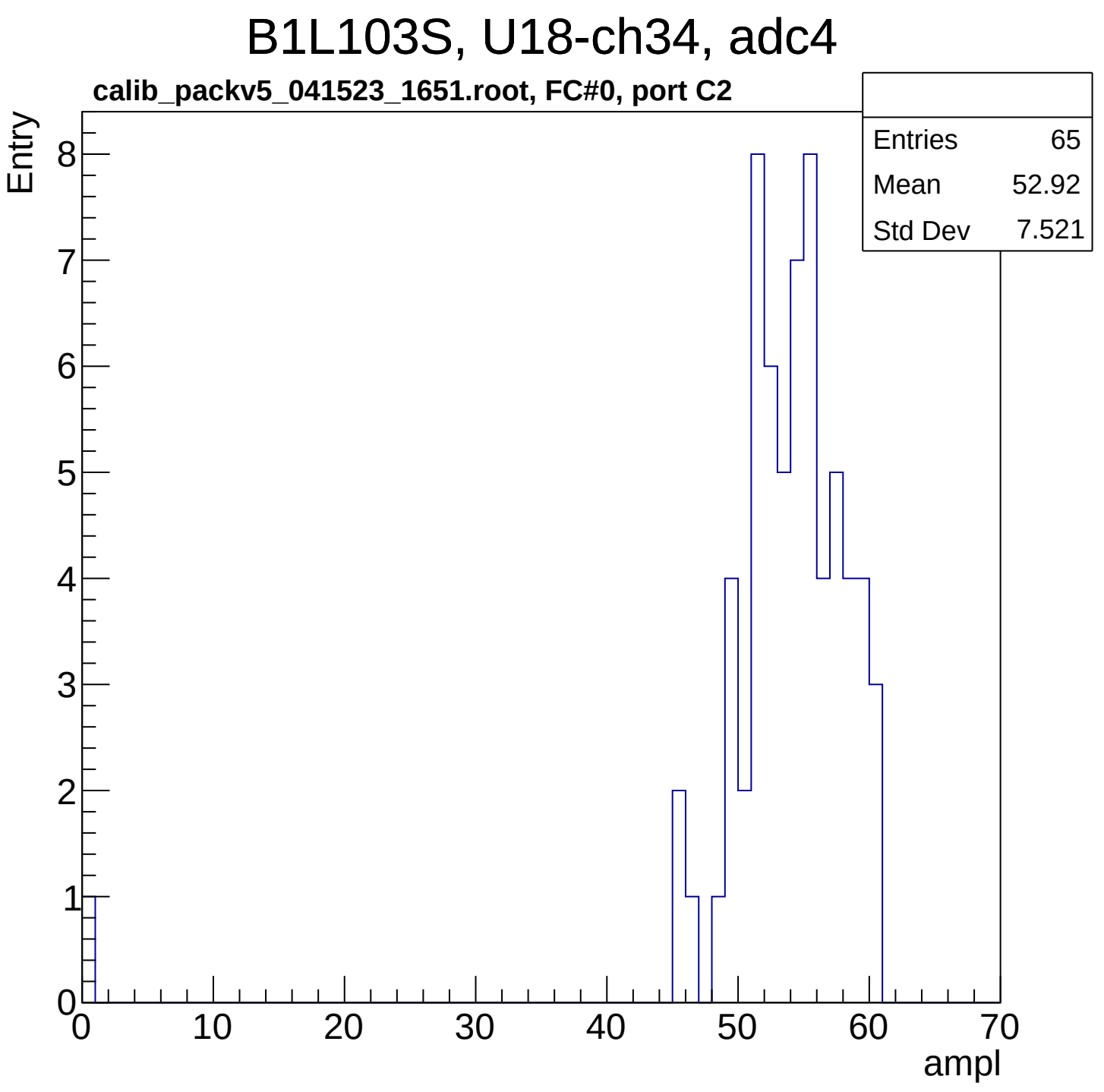
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U18-ch34, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 52.92
Std Dev 7.521
Entry
ampl
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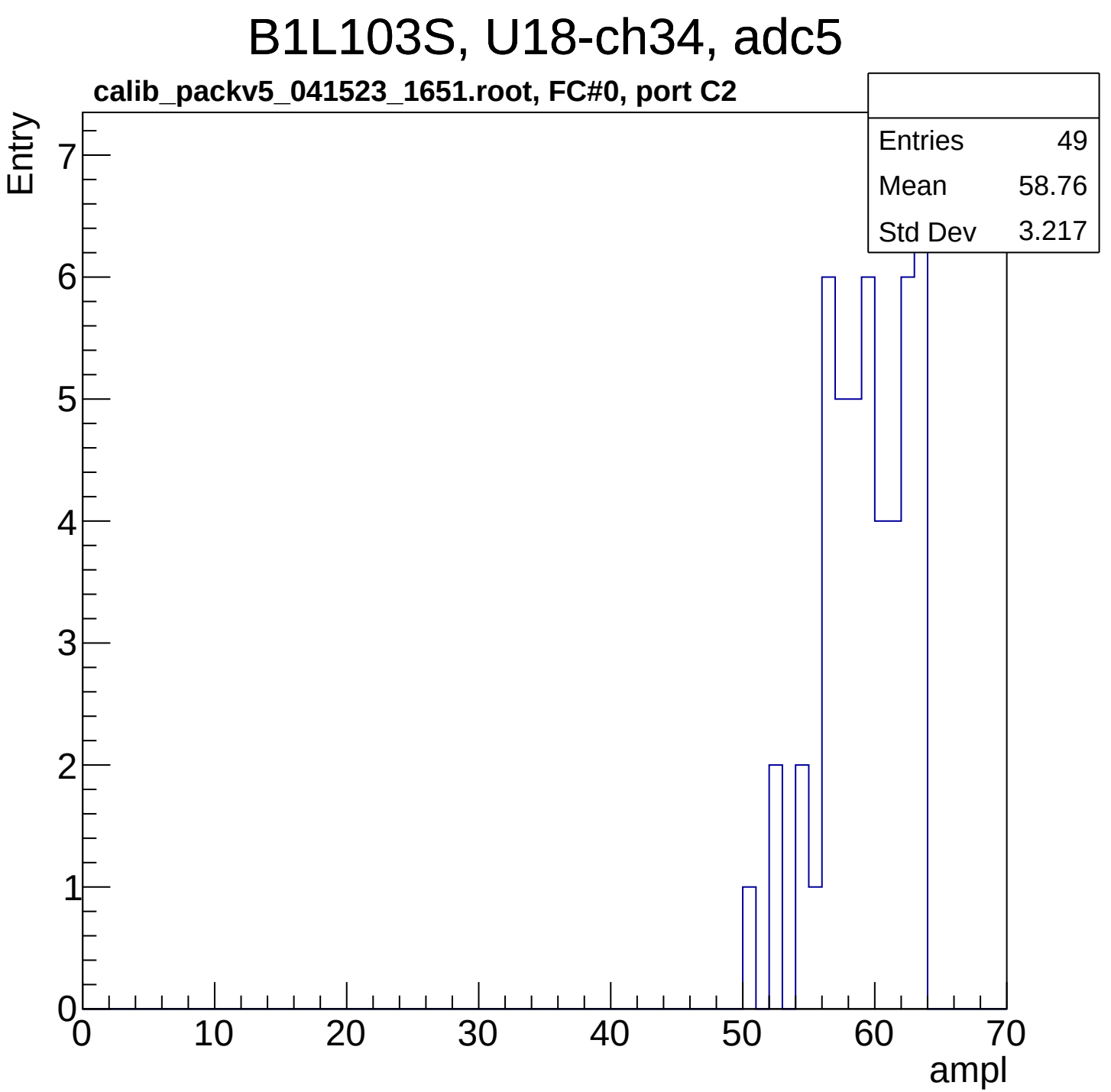
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch34, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 58.76
Std Dev 3.217
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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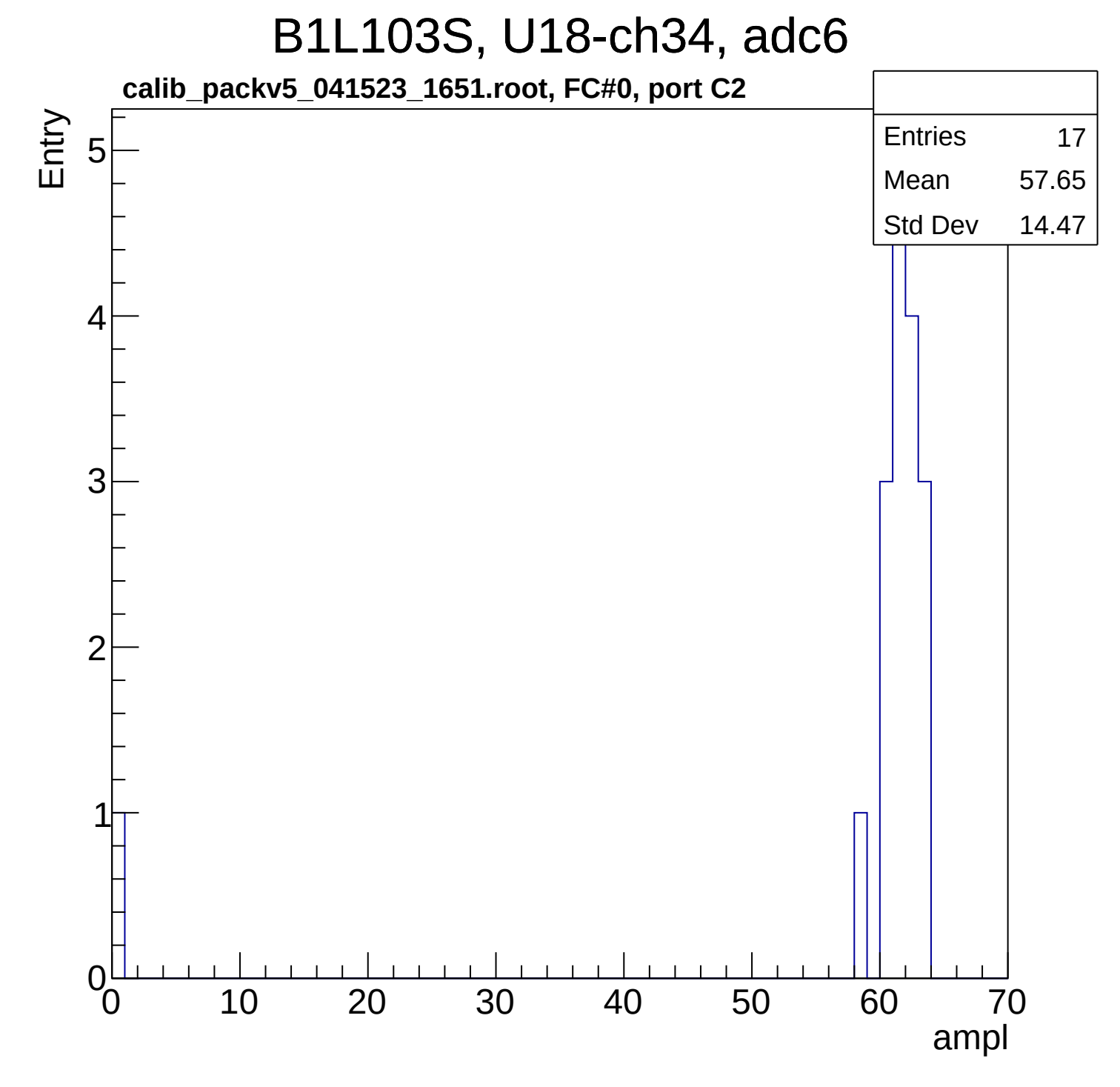
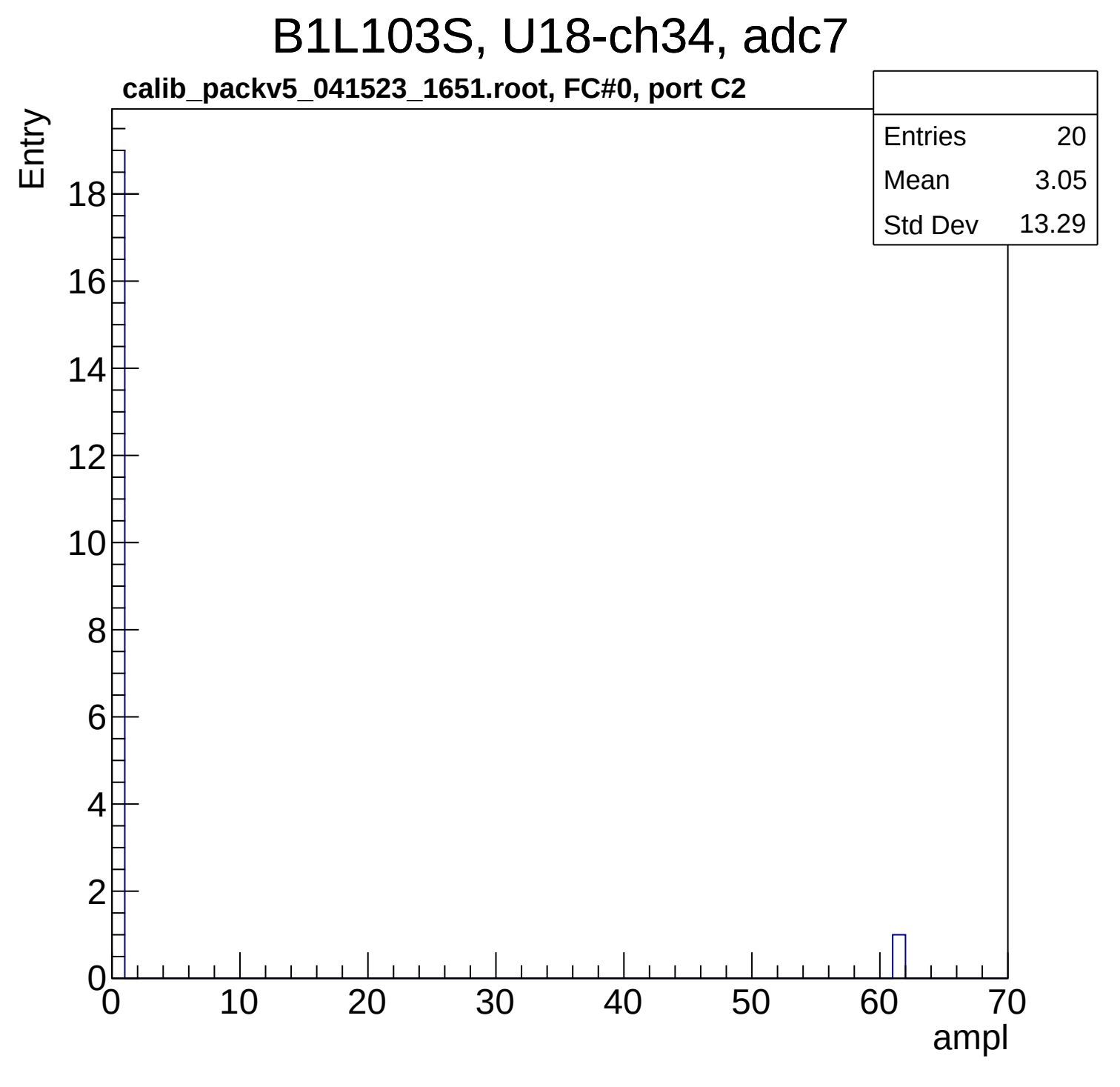

B1L103S, U18-ch34, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 17
Mean 57.65
Std Dev 14.47
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U18-ch34, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.05
Std Dev 13.29
Entry
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6
8
10
12
14
16
18
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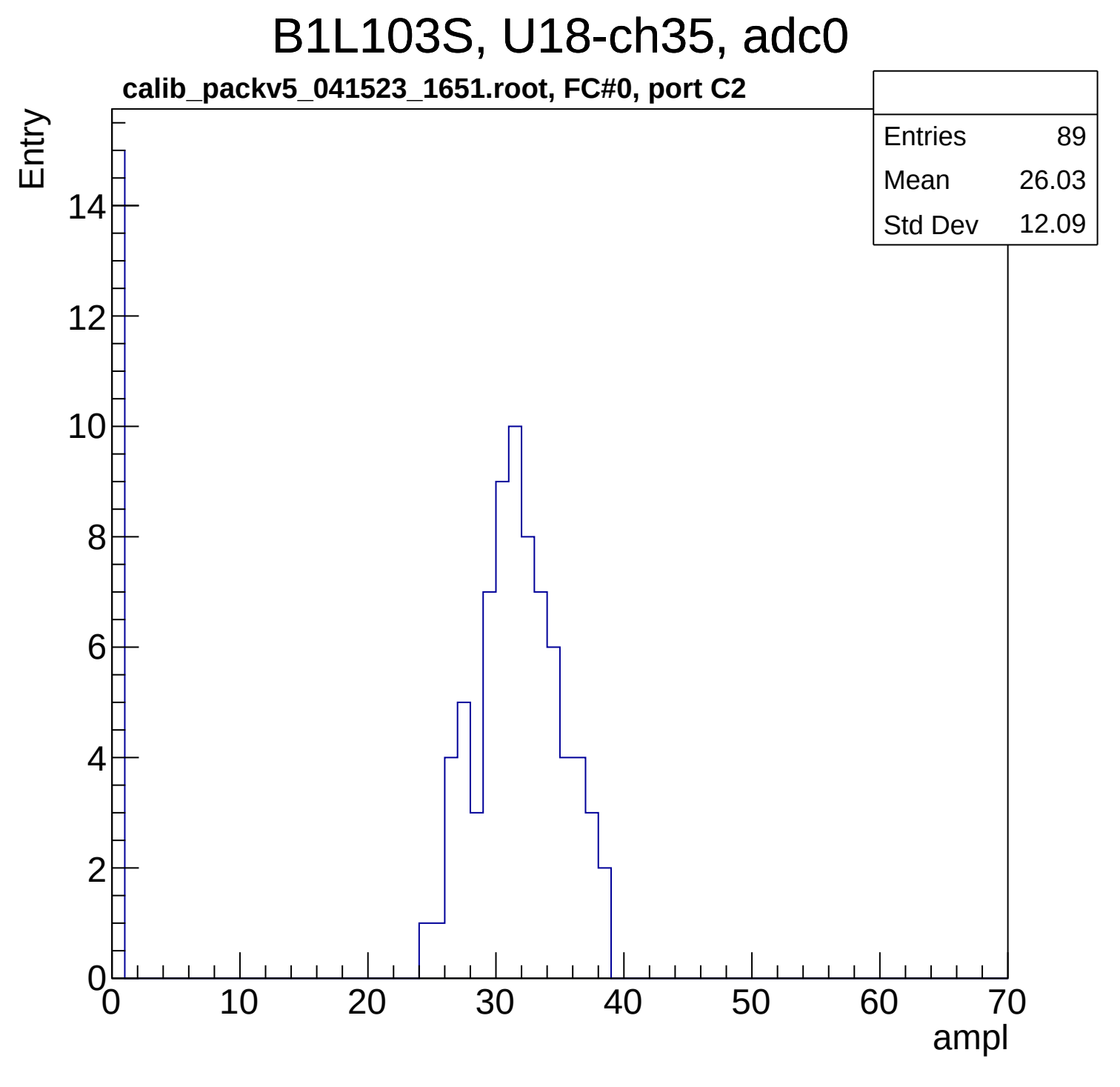
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch35, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 89
Mean 26.03
Std Dev 12.09
Entry
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4
6
8
10
12
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10
20
30
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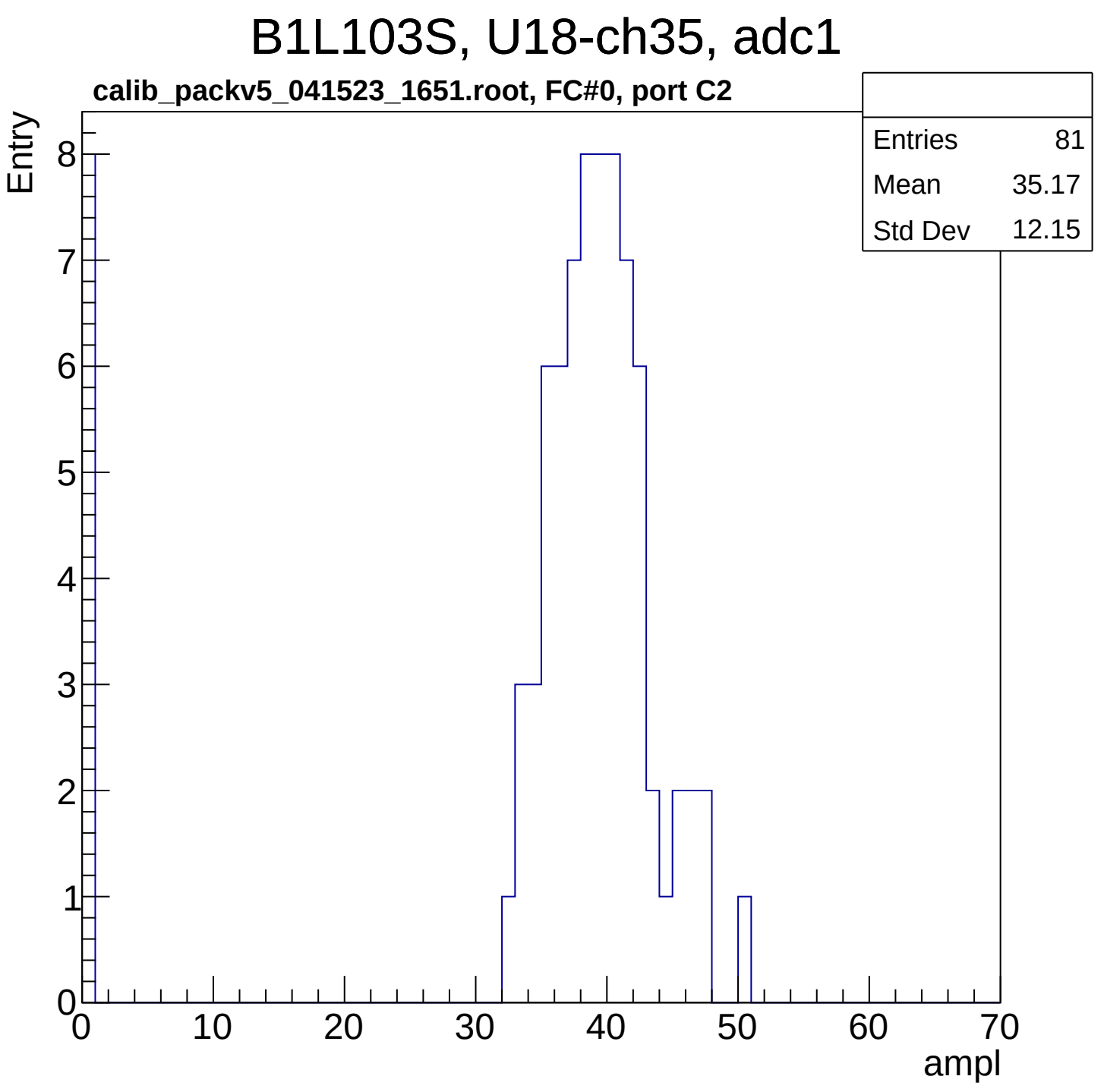
50
60
70
ampl


B1L103S, U18-ch35, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 35.17
Std Dev 12.15
Entry
ampl
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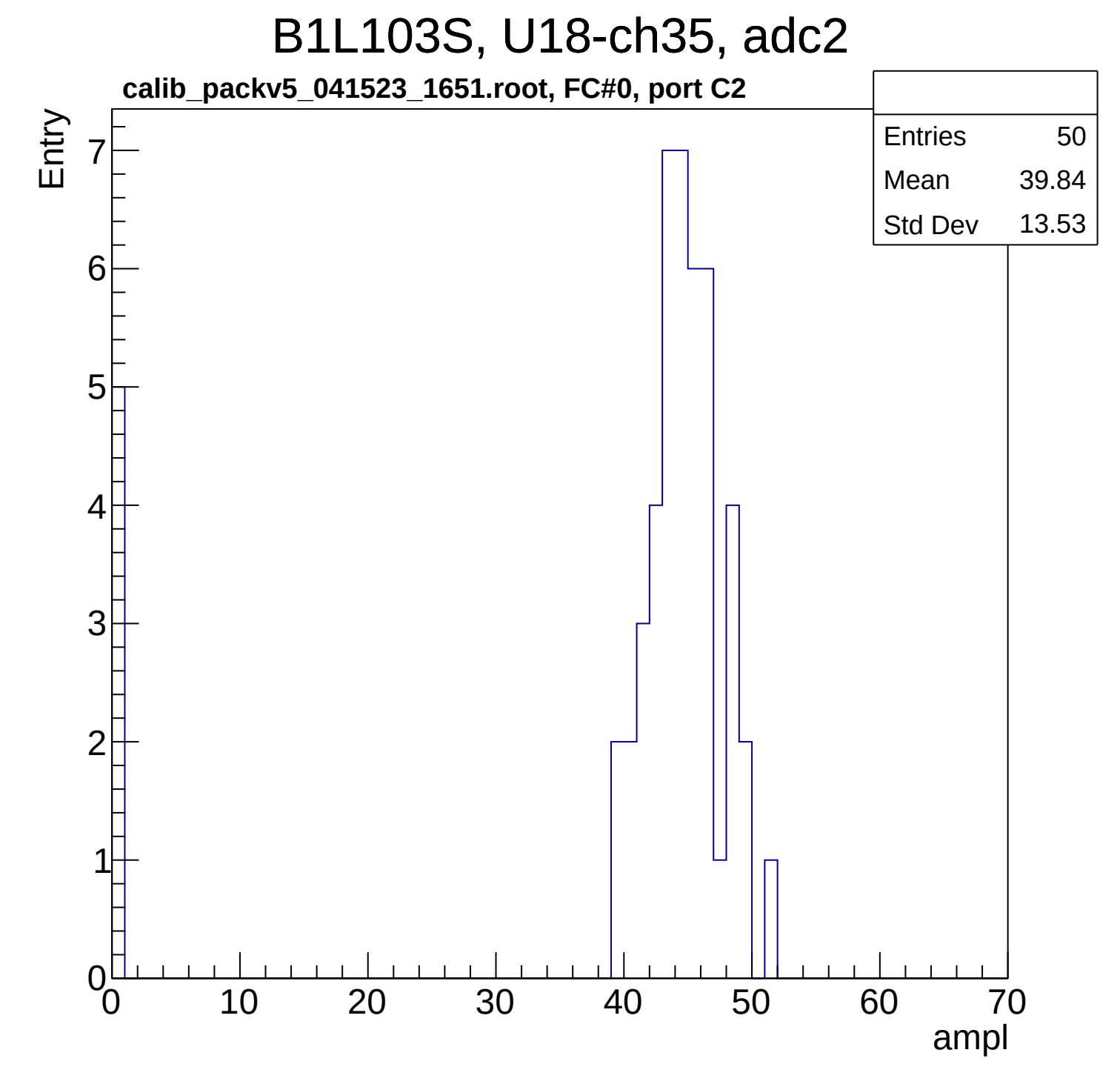
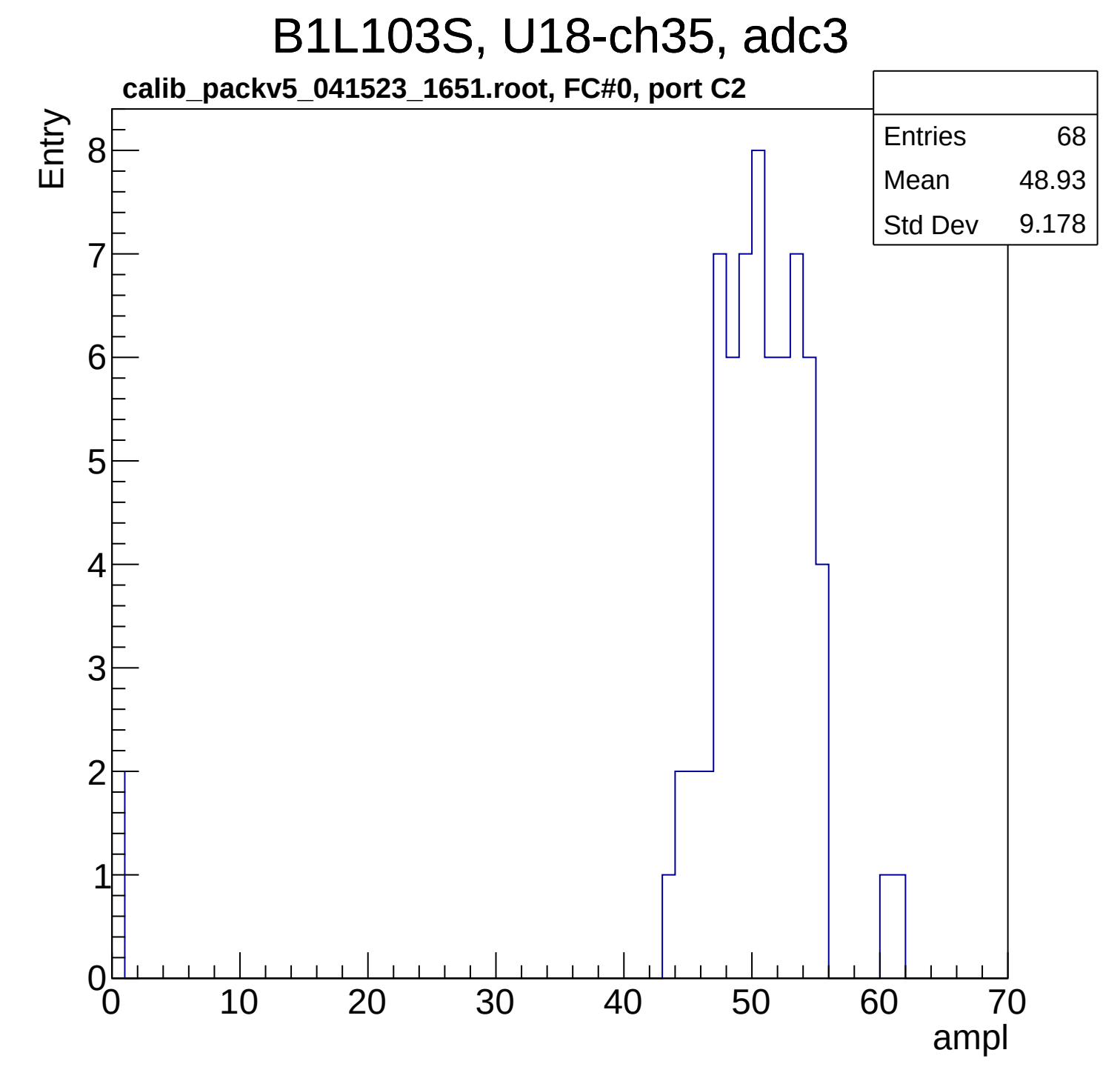
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch35, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 39.84
Std Dev 13.53
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U18-ch35, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 48.93
Std Dev 9.178
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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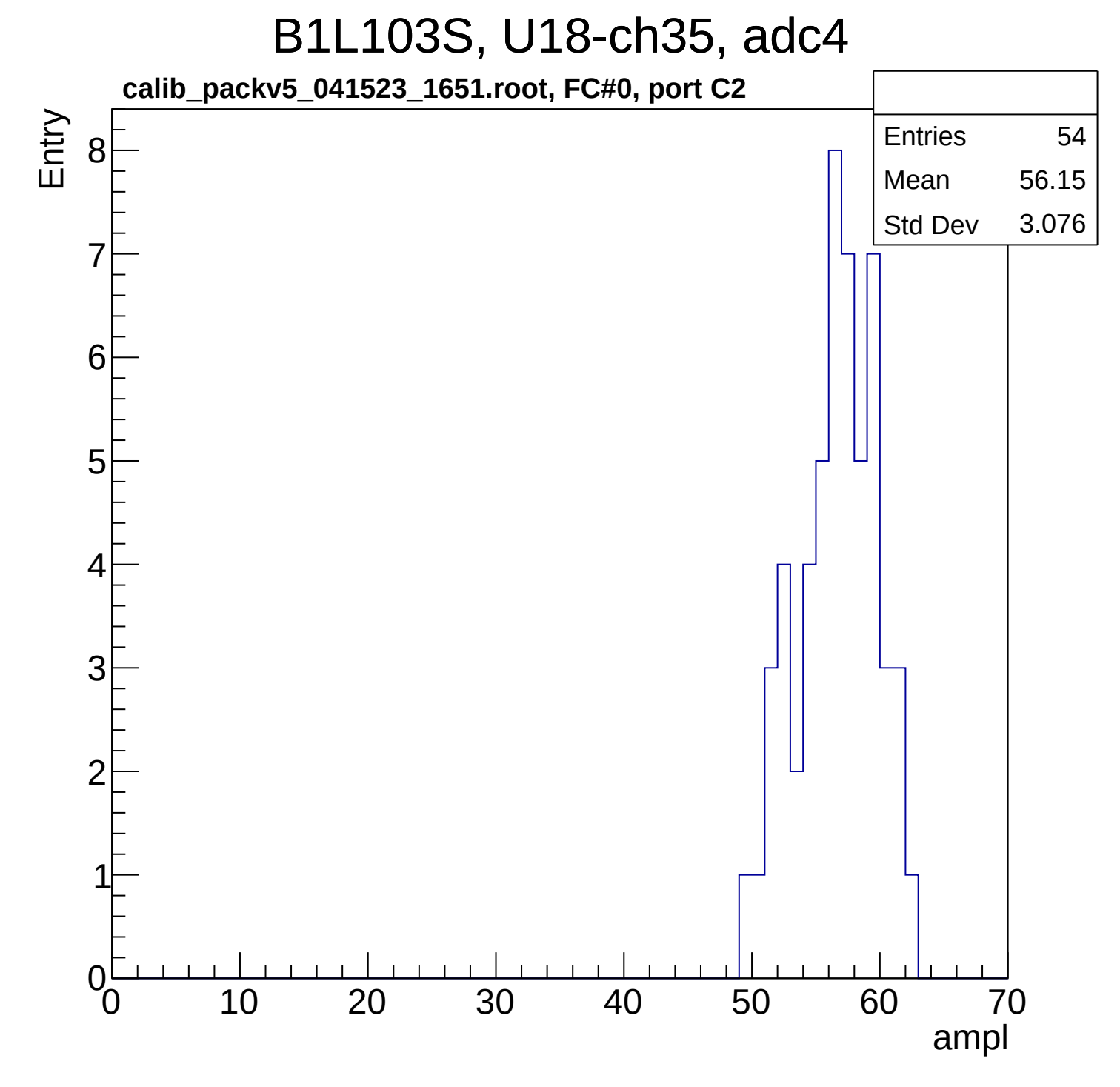
40
50
60
70


B1L103S, U18-ch35, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 56.15
Std Dev 3.076
Entry
ampl
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2
3
4
5
6
7
8
0
10
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40
50
60
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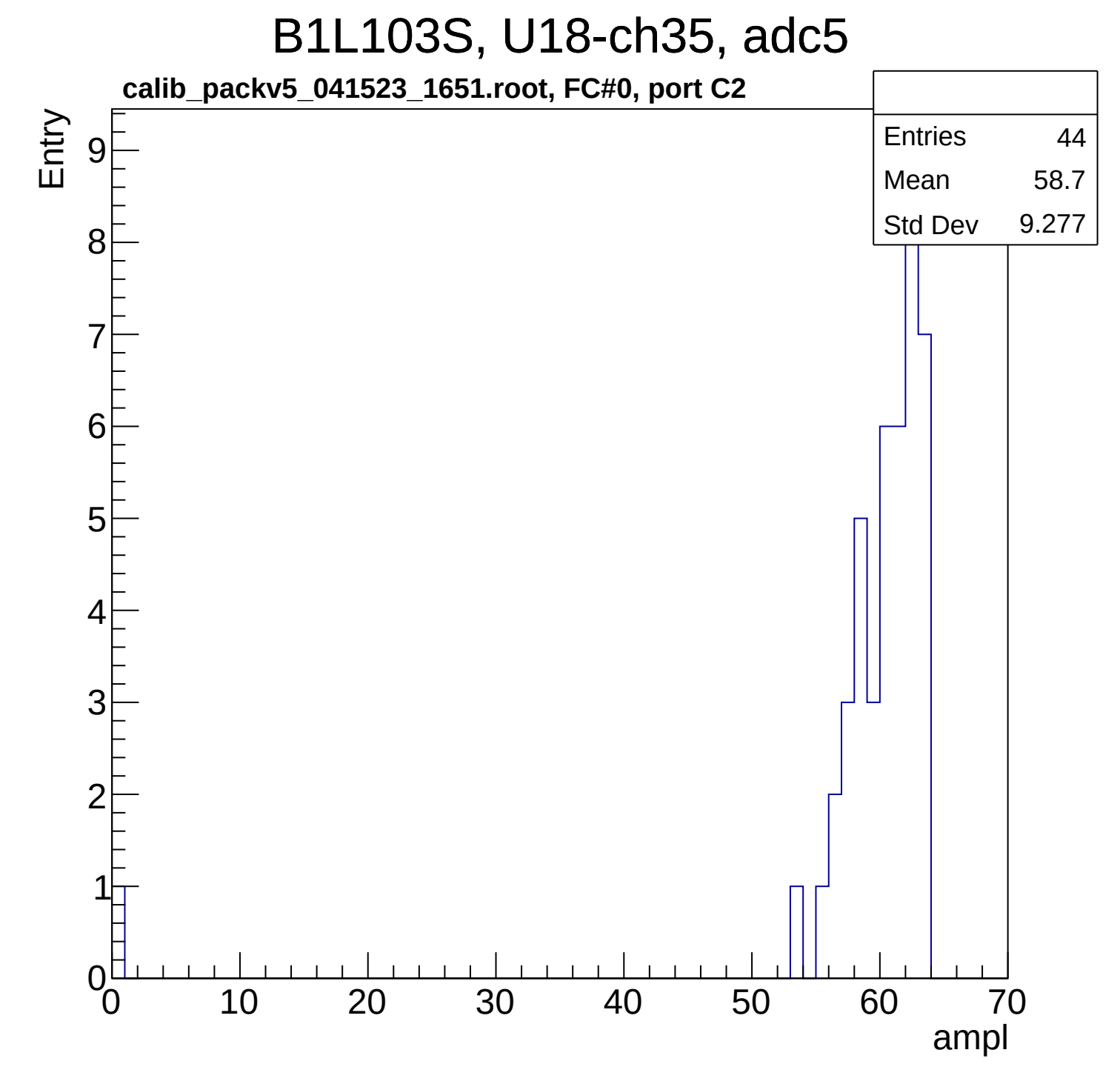
B1L103S, U18-ch35, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 58.7
Std Dev 9.277
Entry
ampl
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6
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8
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0
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20
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60
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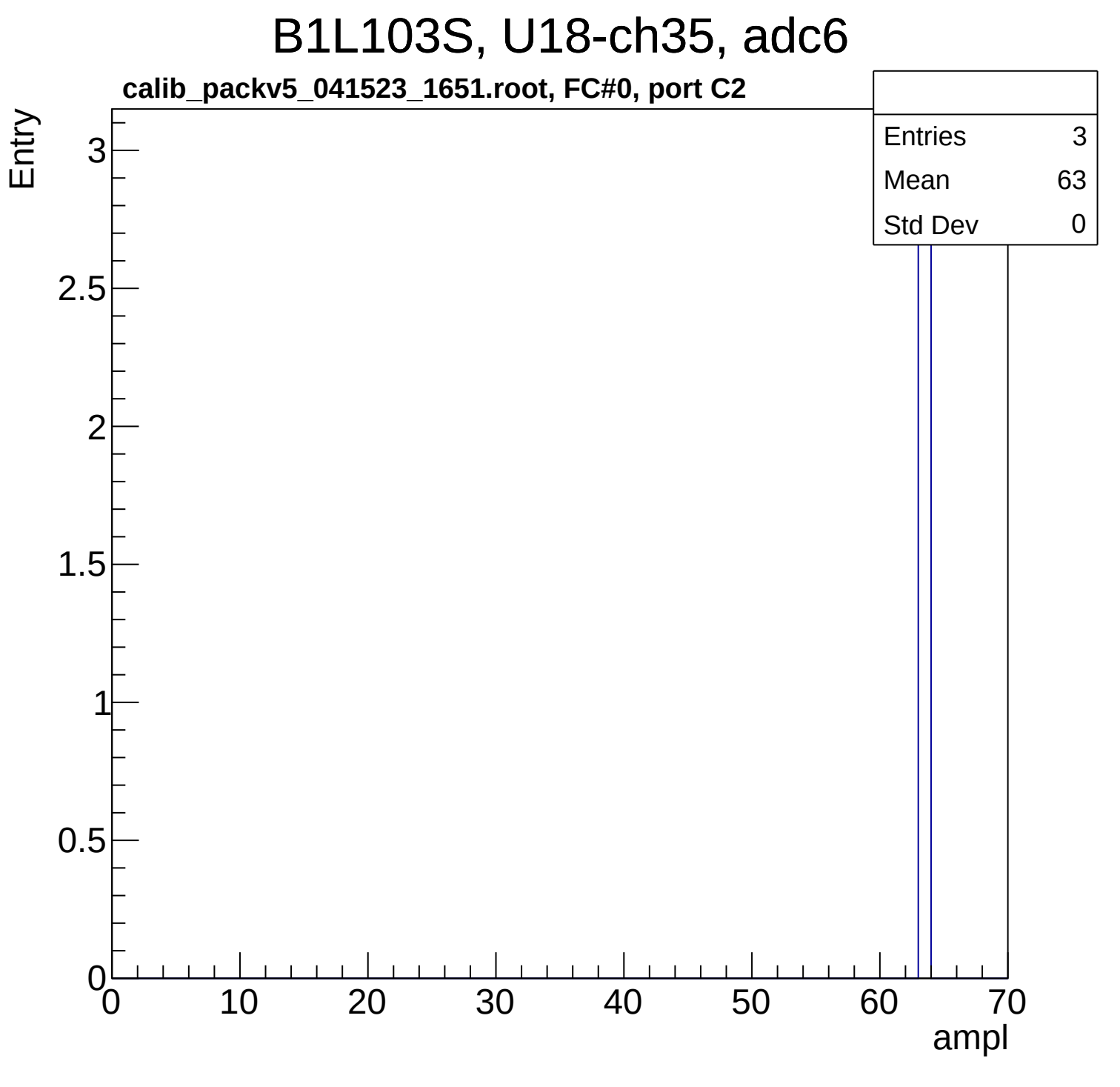
B1L103S, U18-ch35, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 3
Mean 63
Std Dev 0
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
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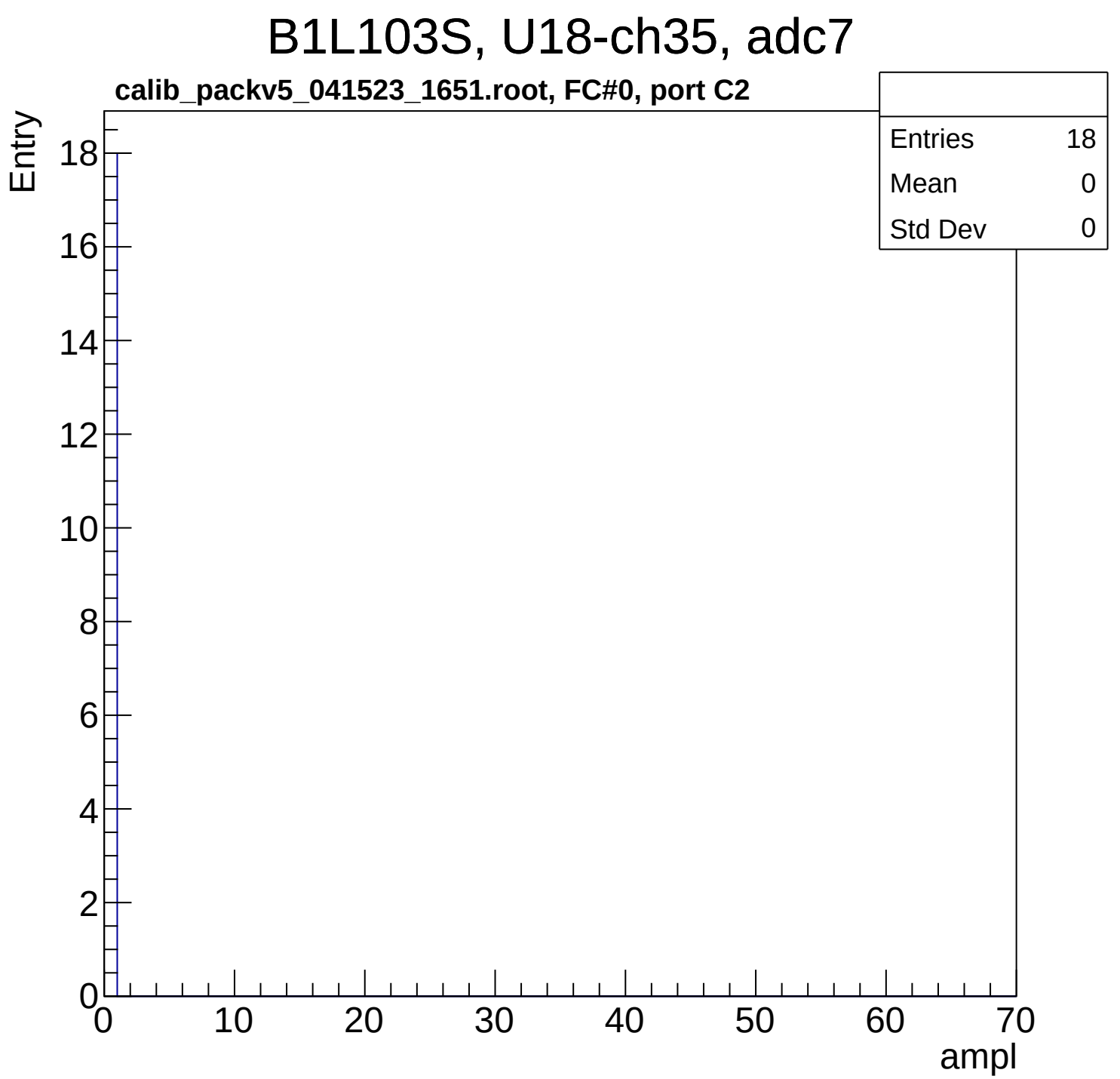
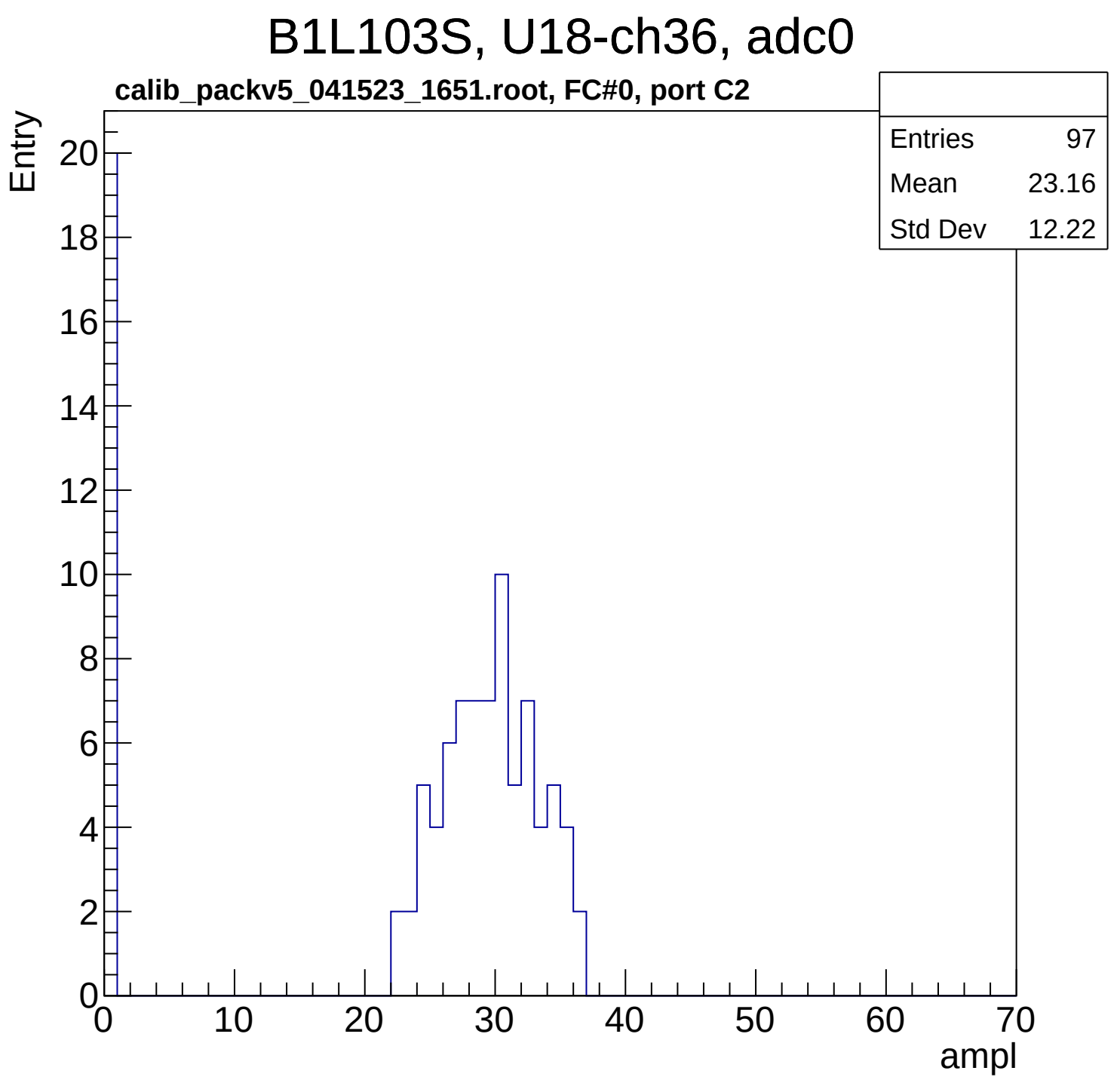
40
50
60
70


B1L103S, U18-ch35, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch36, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 97
Mean 23.16
Std Dev 12.22
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
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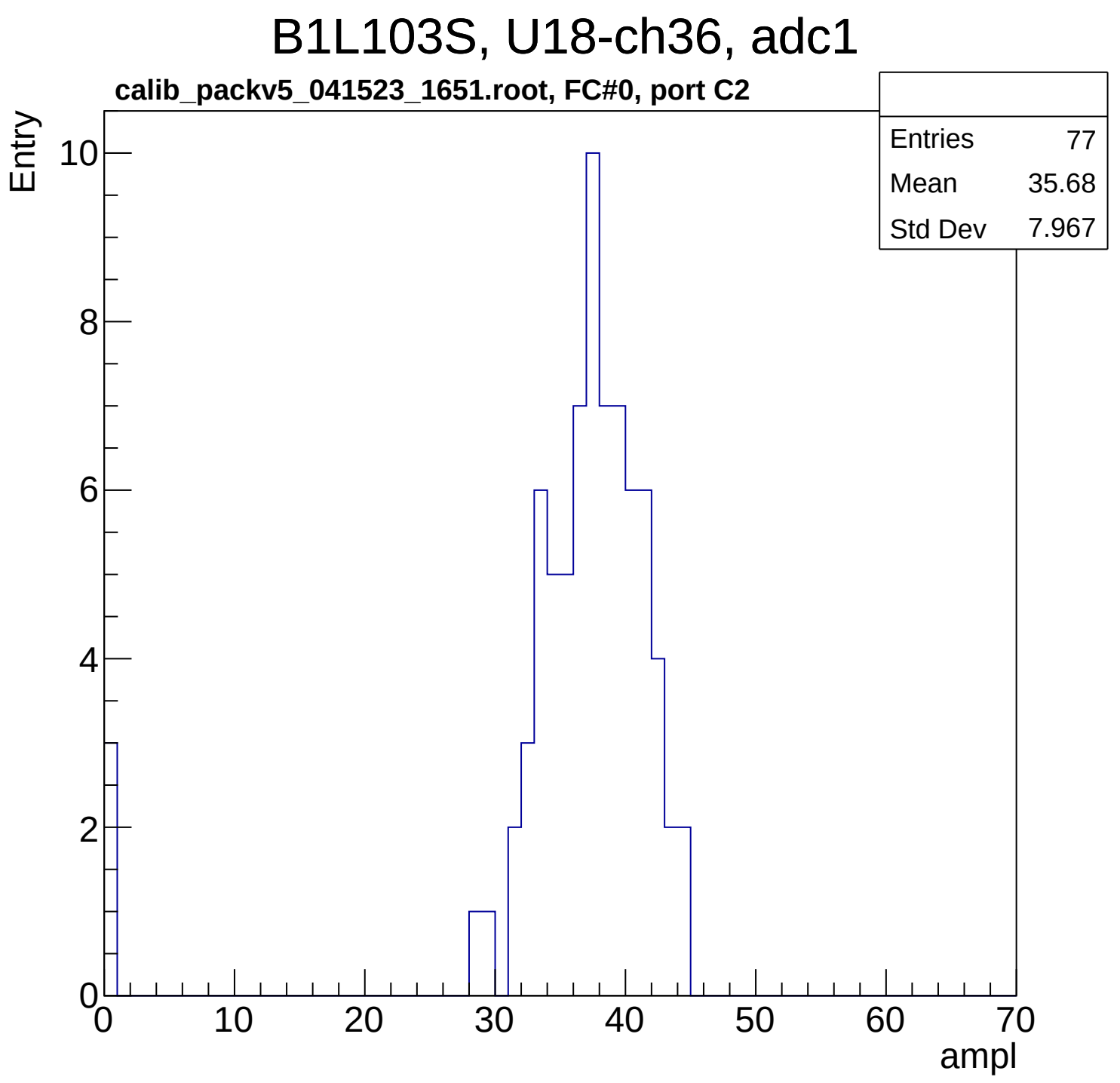
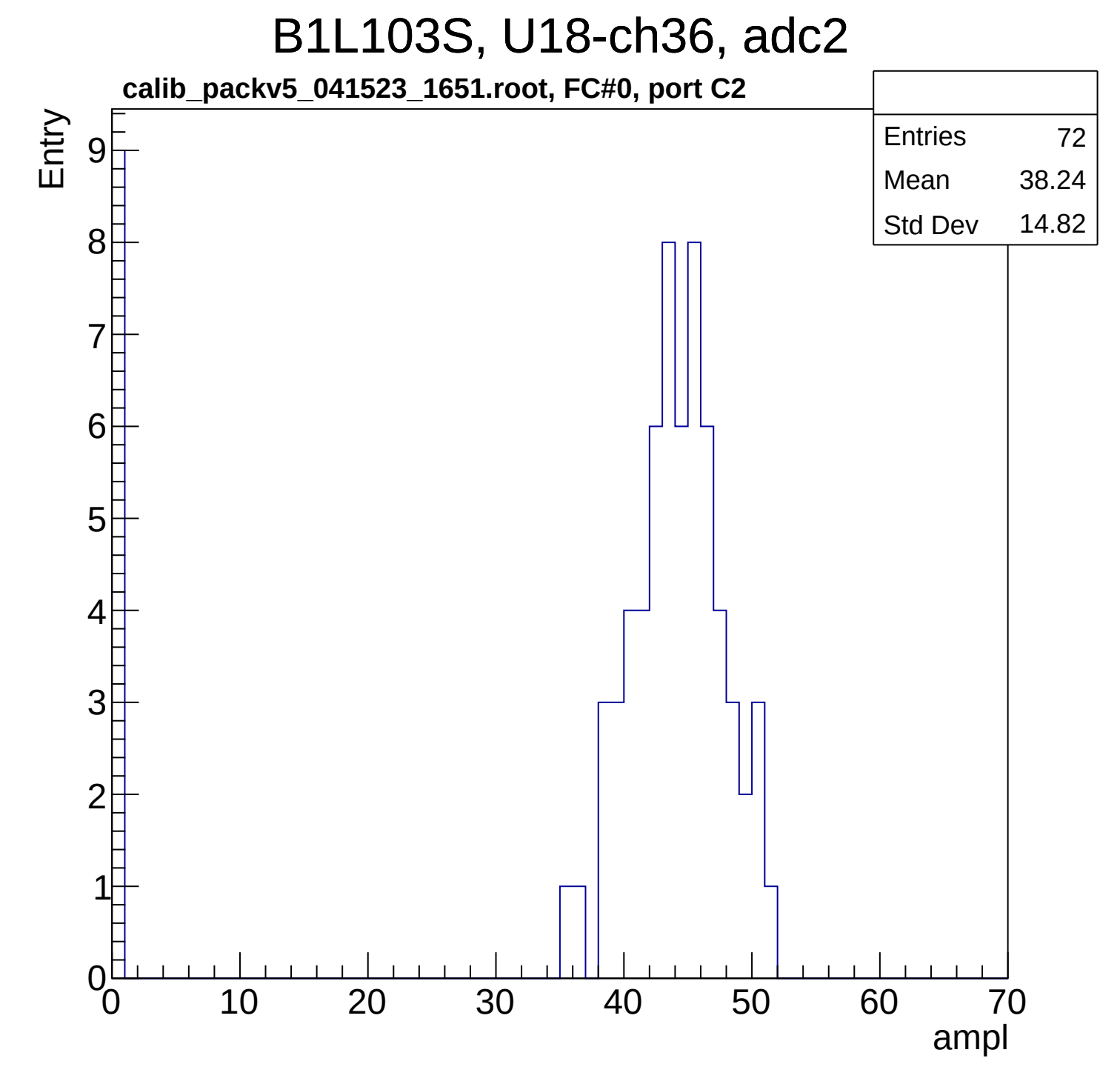

B1L103S, U18-ch36, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 35.68
Std Dev 7.967
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U18-ch36, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 38.24
Std Dev 14.82
Entry
ampl
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2
3
4
5
6
7
8
9
0
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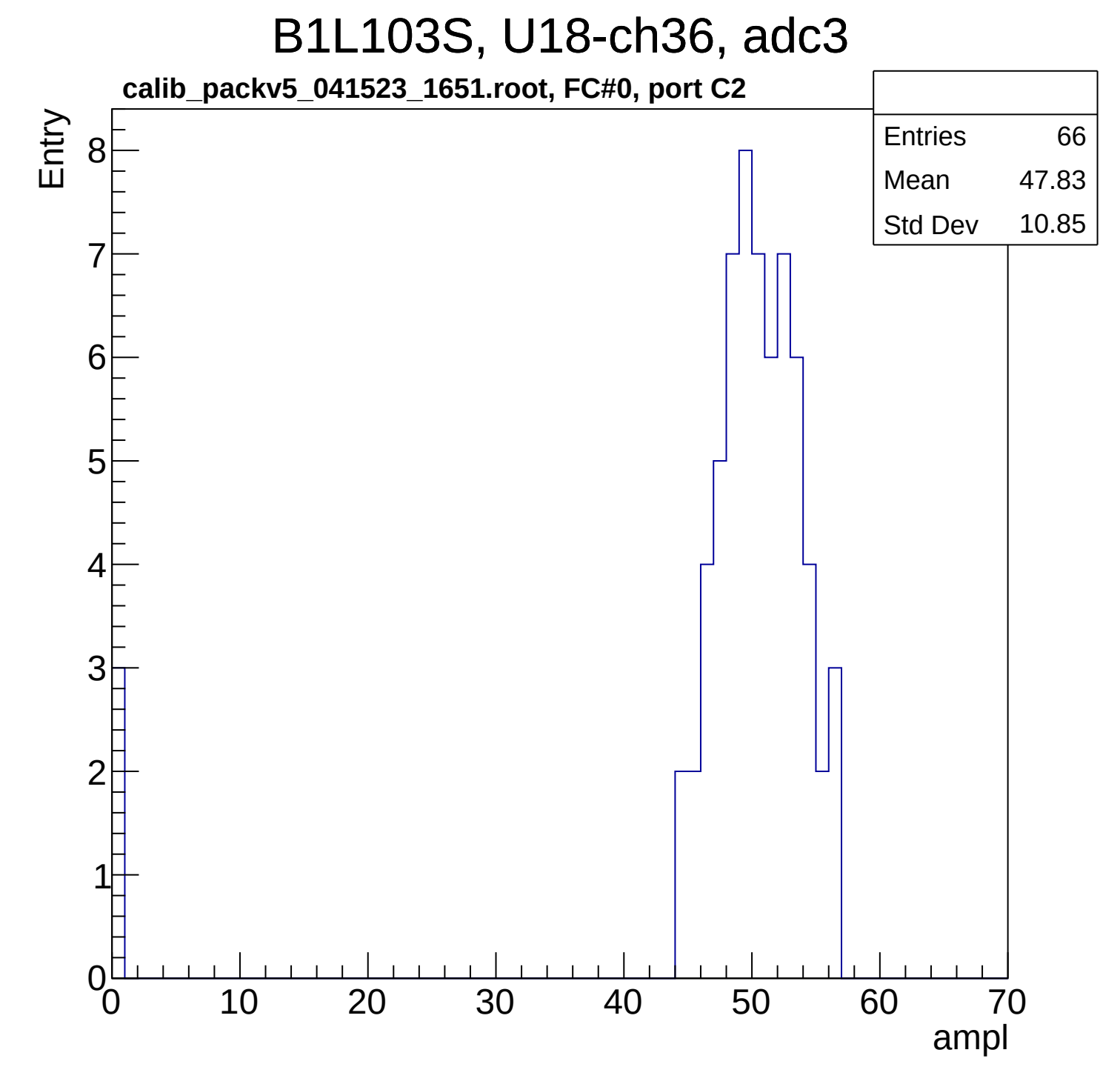
20
30
40
50
60
70


B1L103S, U18-ch36, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 47.83
Std Dev 10.85
Entry
ampl
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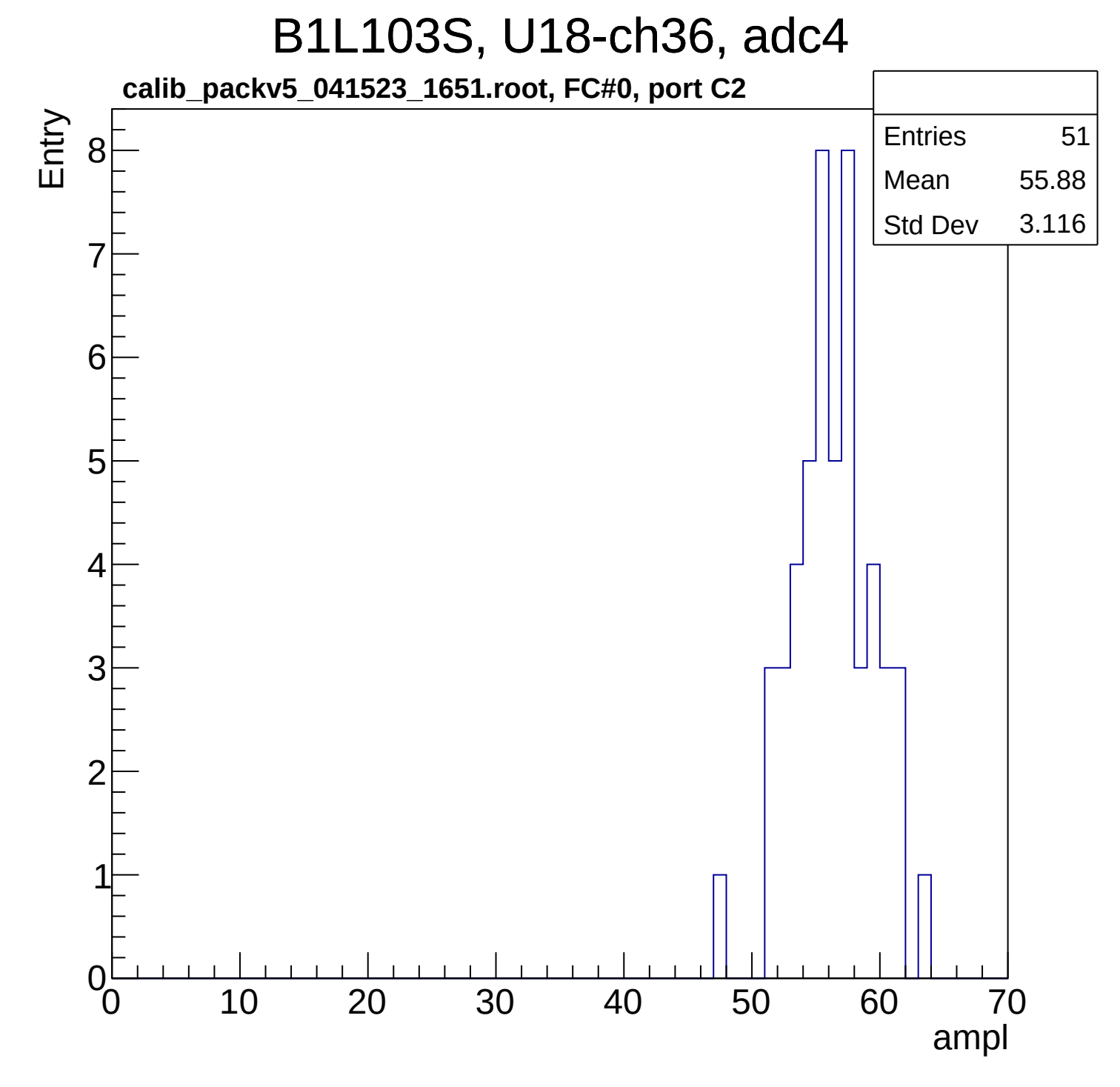
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch36, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 55.88
Std Dev 3.116
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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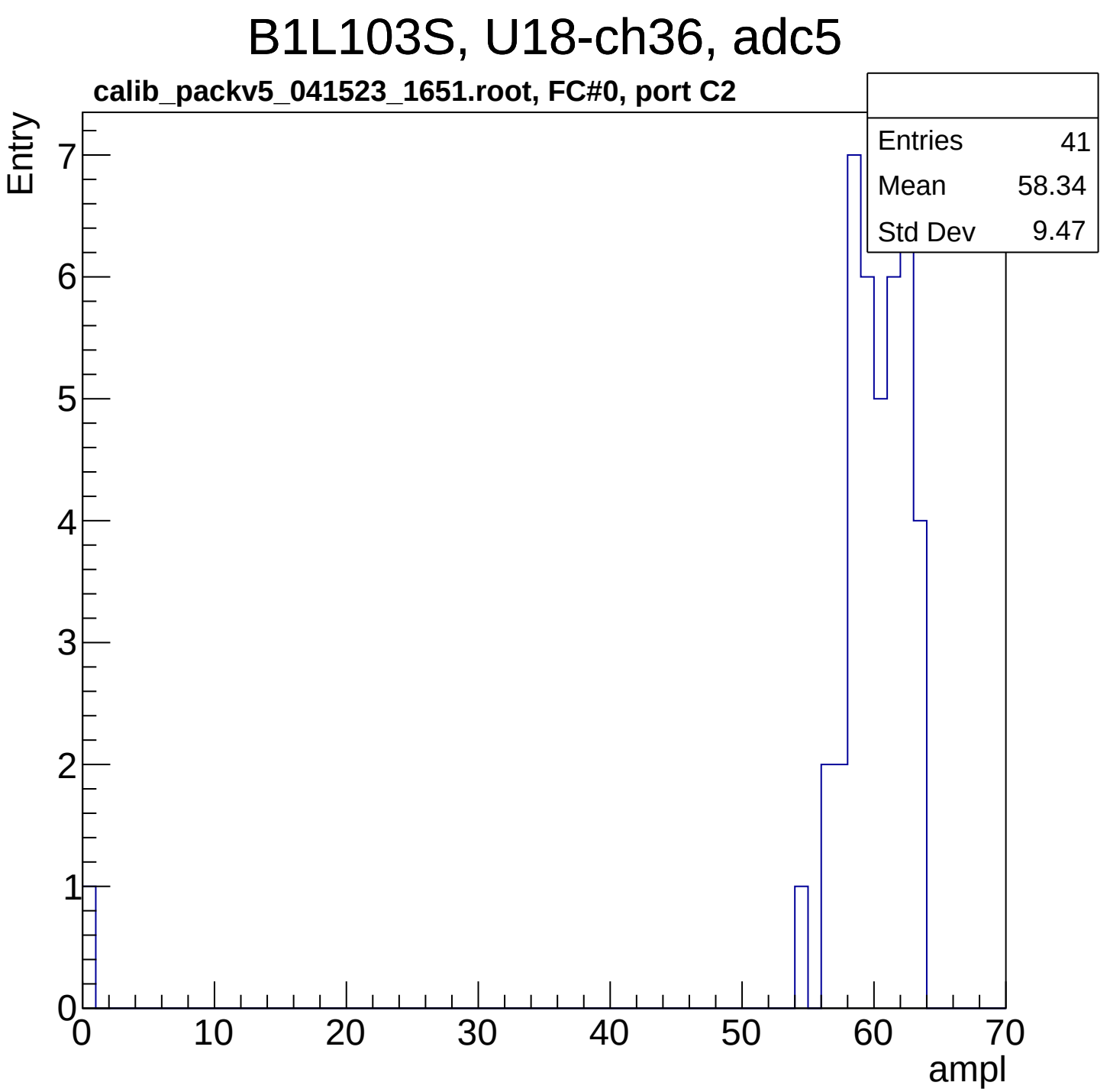
B1L103S, U18-ch36, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 41
Mean 58.34
Std Dev 9.47
Entry
ampl
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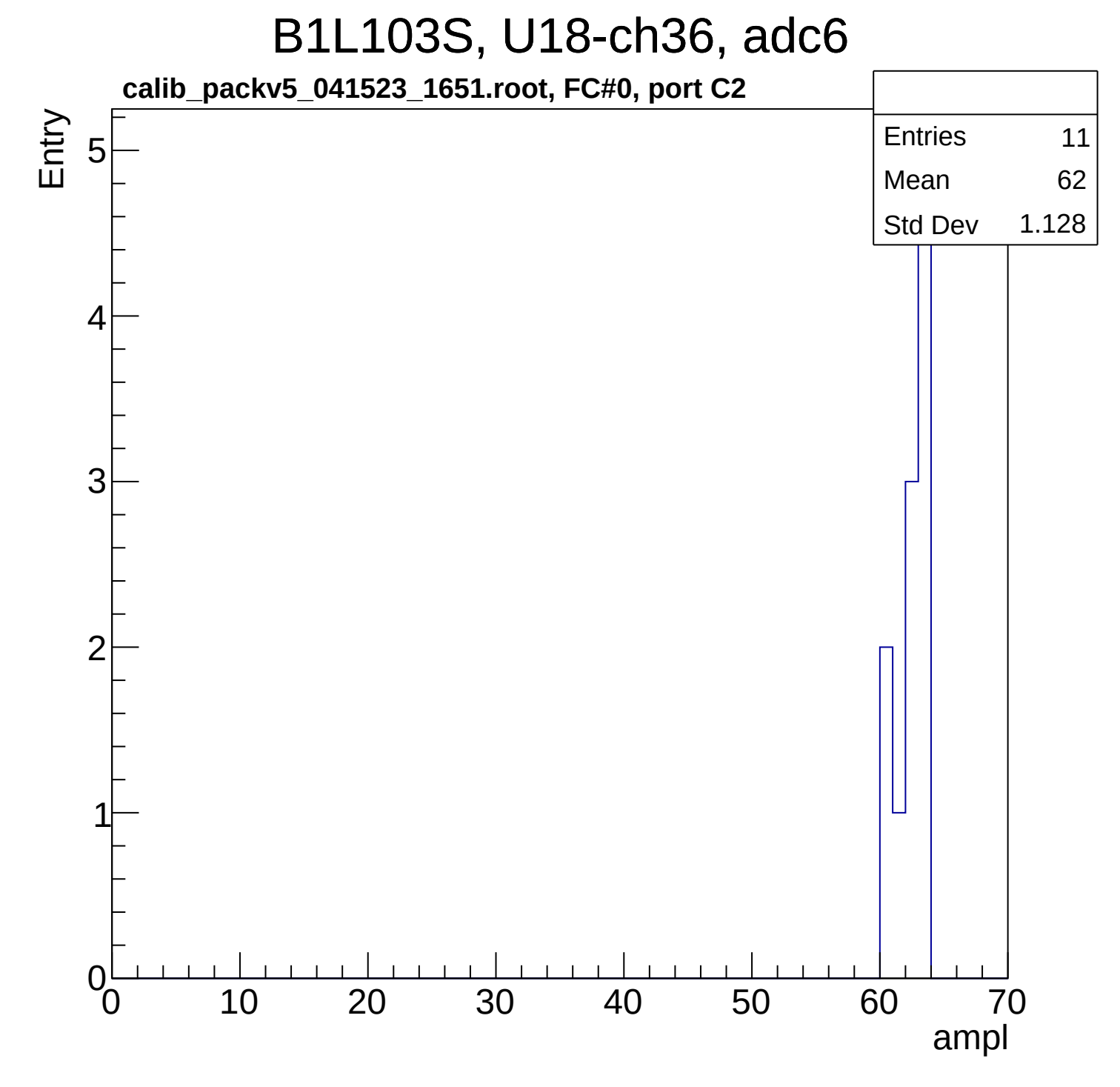
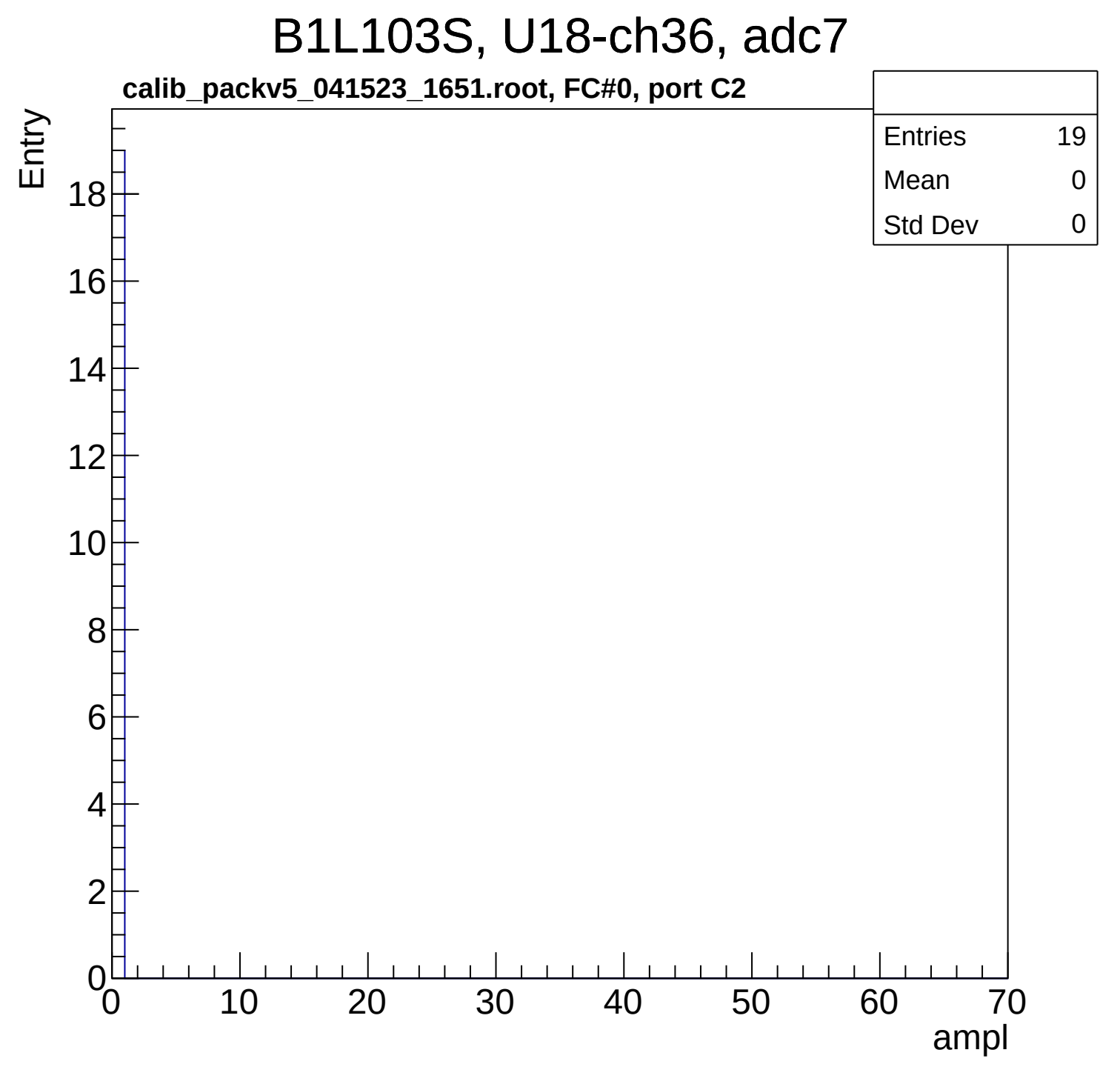
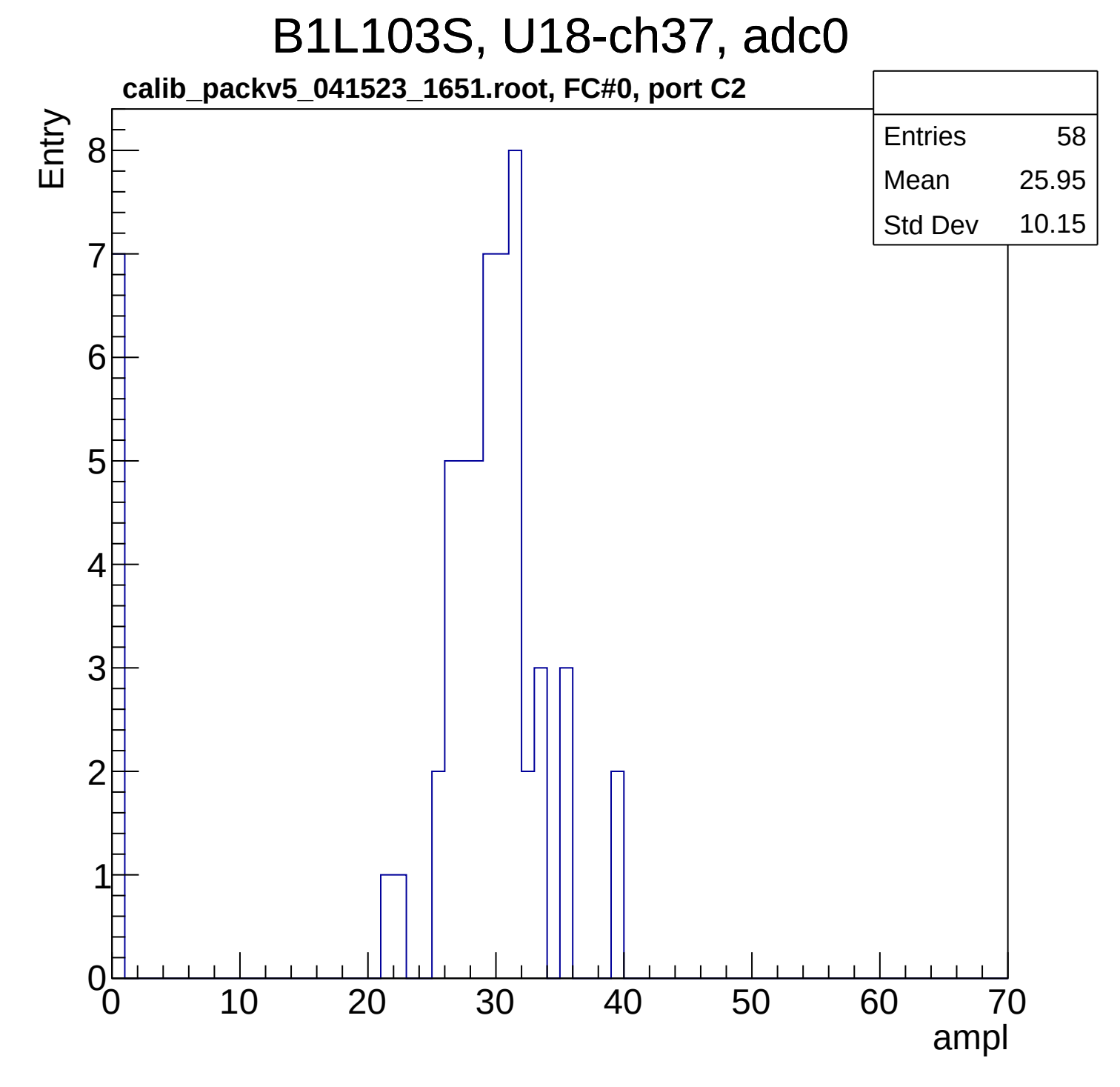
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U18-ch36, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 62
Std Dev 1.128
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch36, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch37, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 25.95
Std Dev 10.15
Entry
ampl
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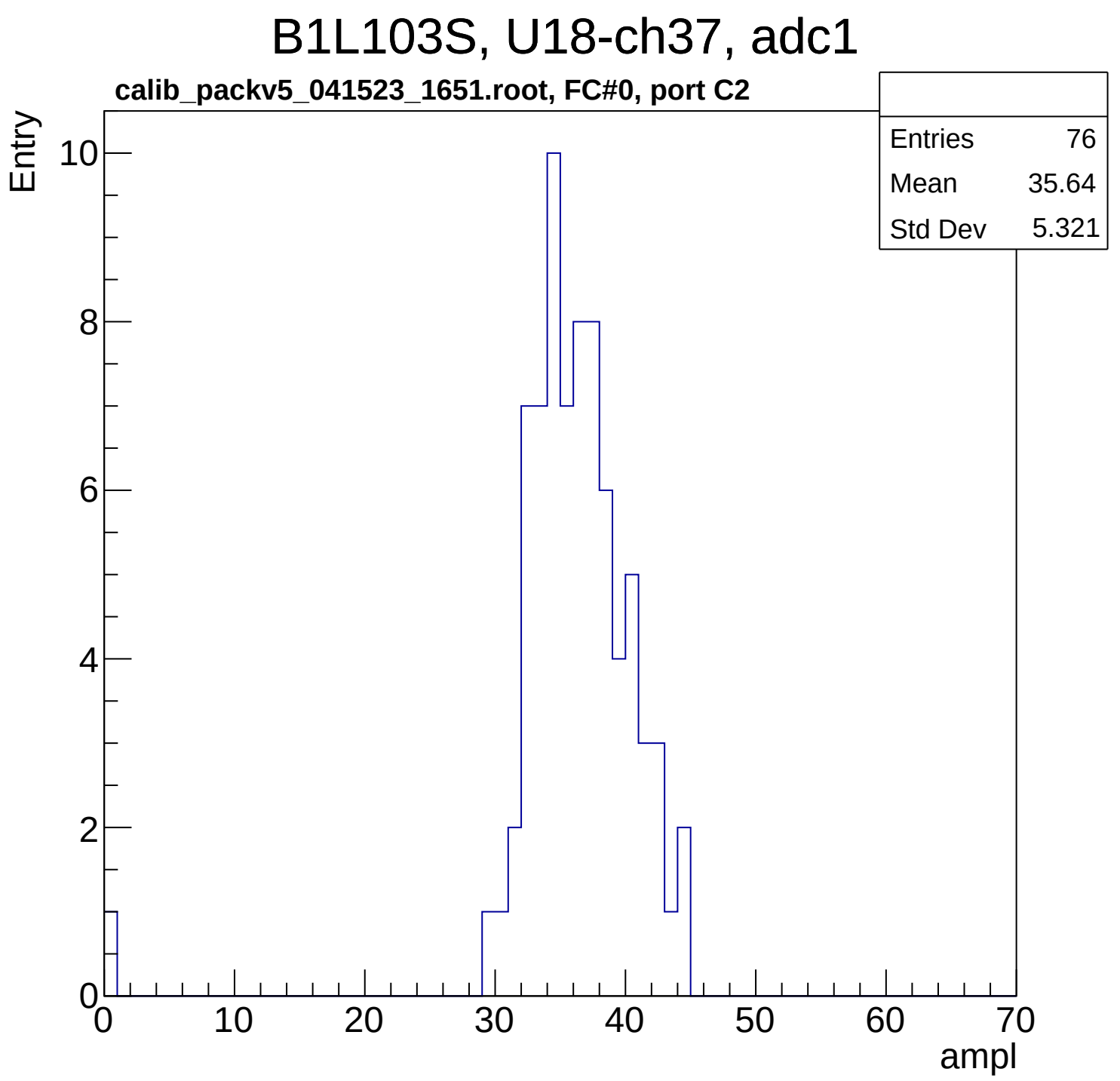
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch37, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 35.64
Std Dev 5.321
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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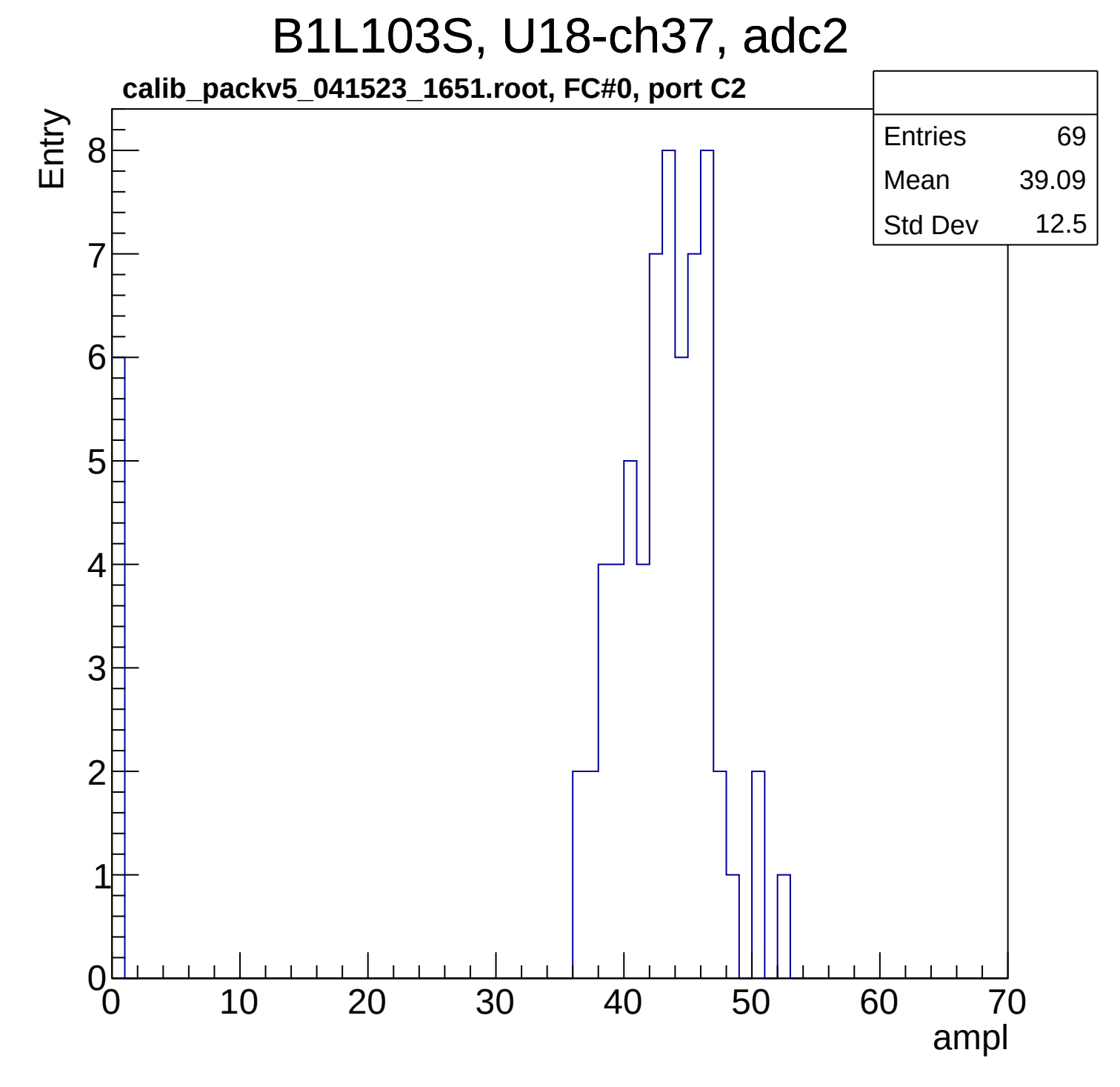
B1L103S, U18-ch37, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 39.09
Std Dev 12.5
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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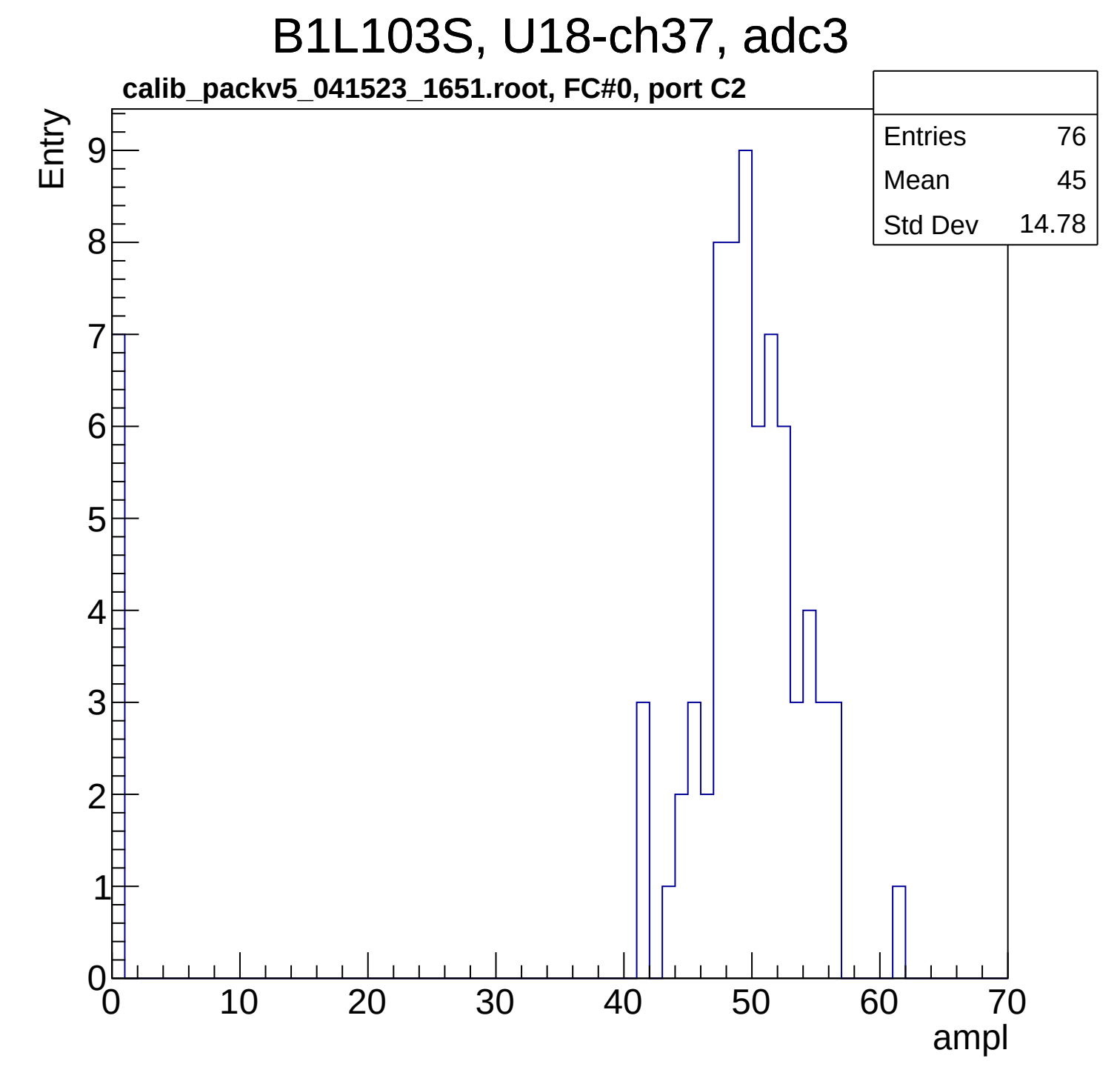
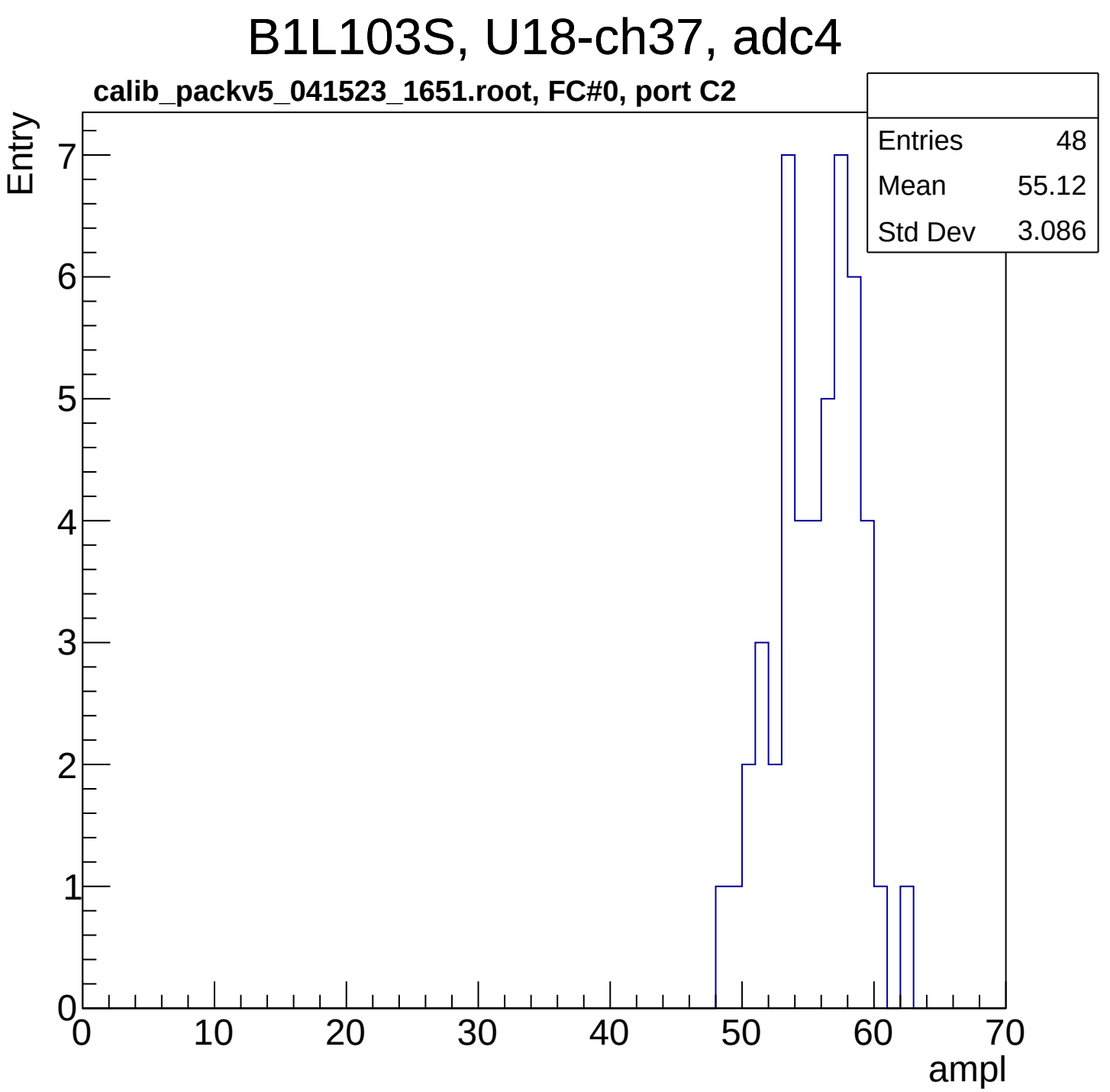
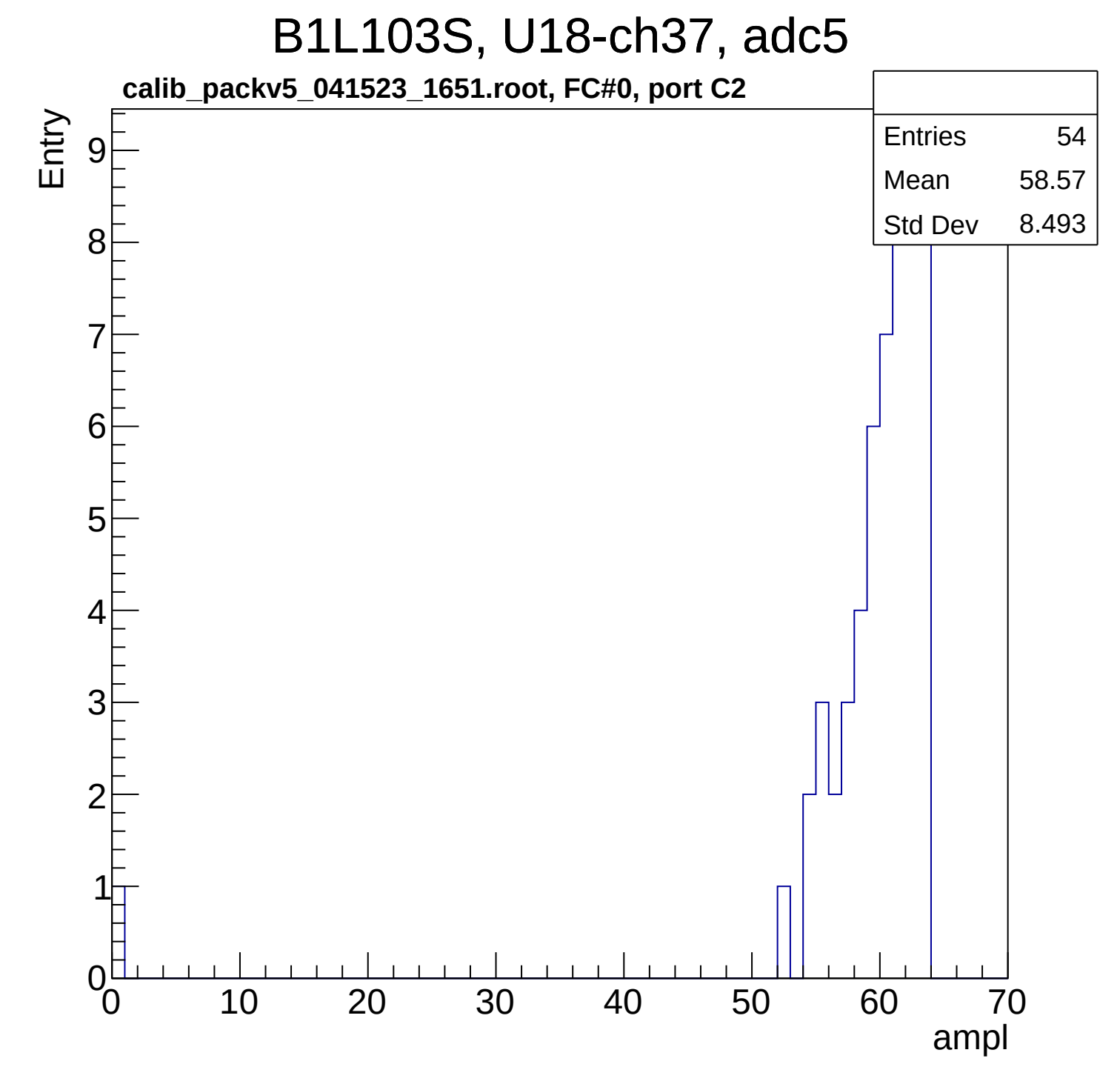

B1L103S, U18-ch37, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 45
Std Dev 14.78
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U18-ch37, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 55.12
Std Dev 3.086
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U18-ch37, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 58.57
Std Dev 8.493
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
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40
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60
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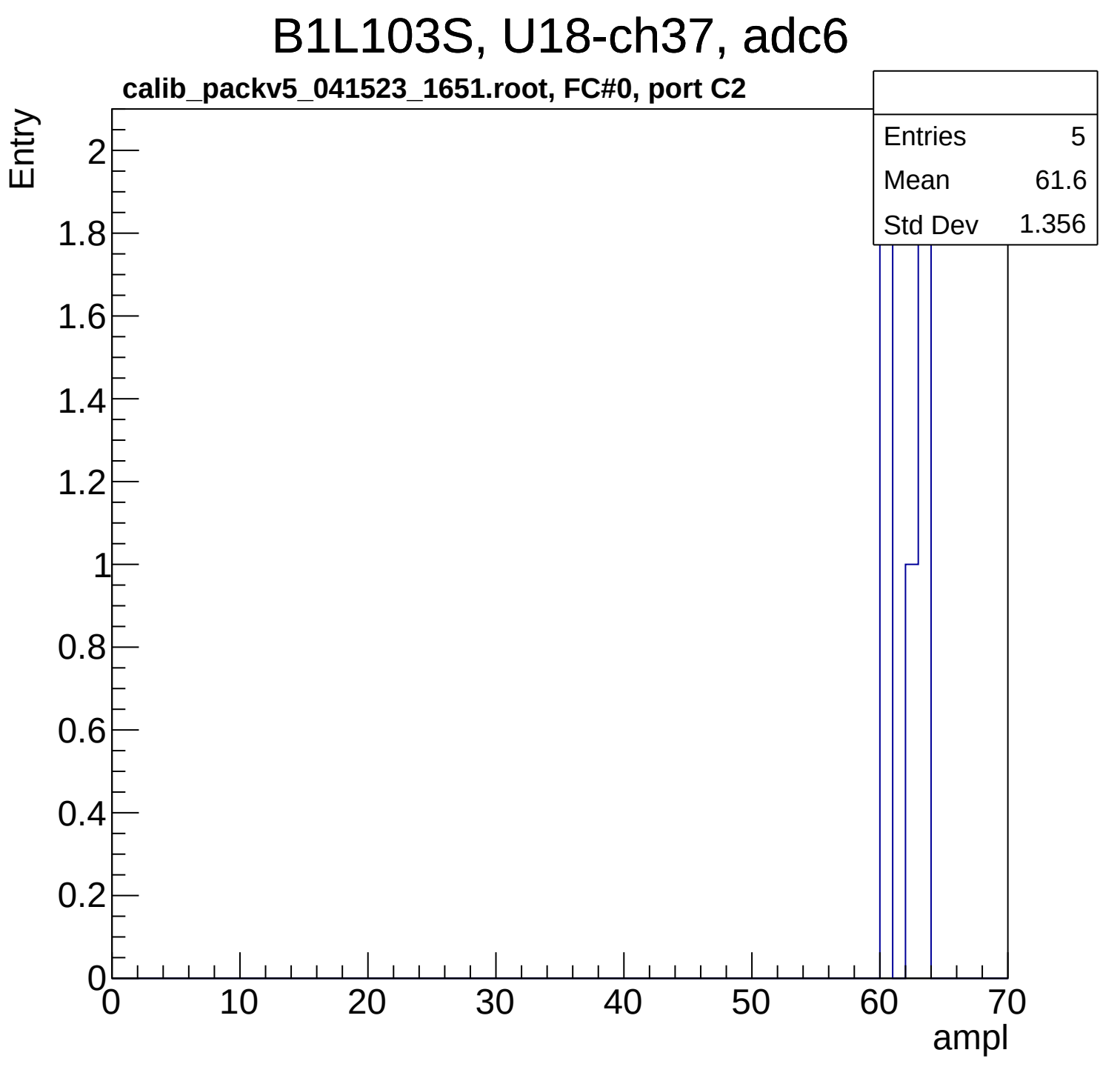
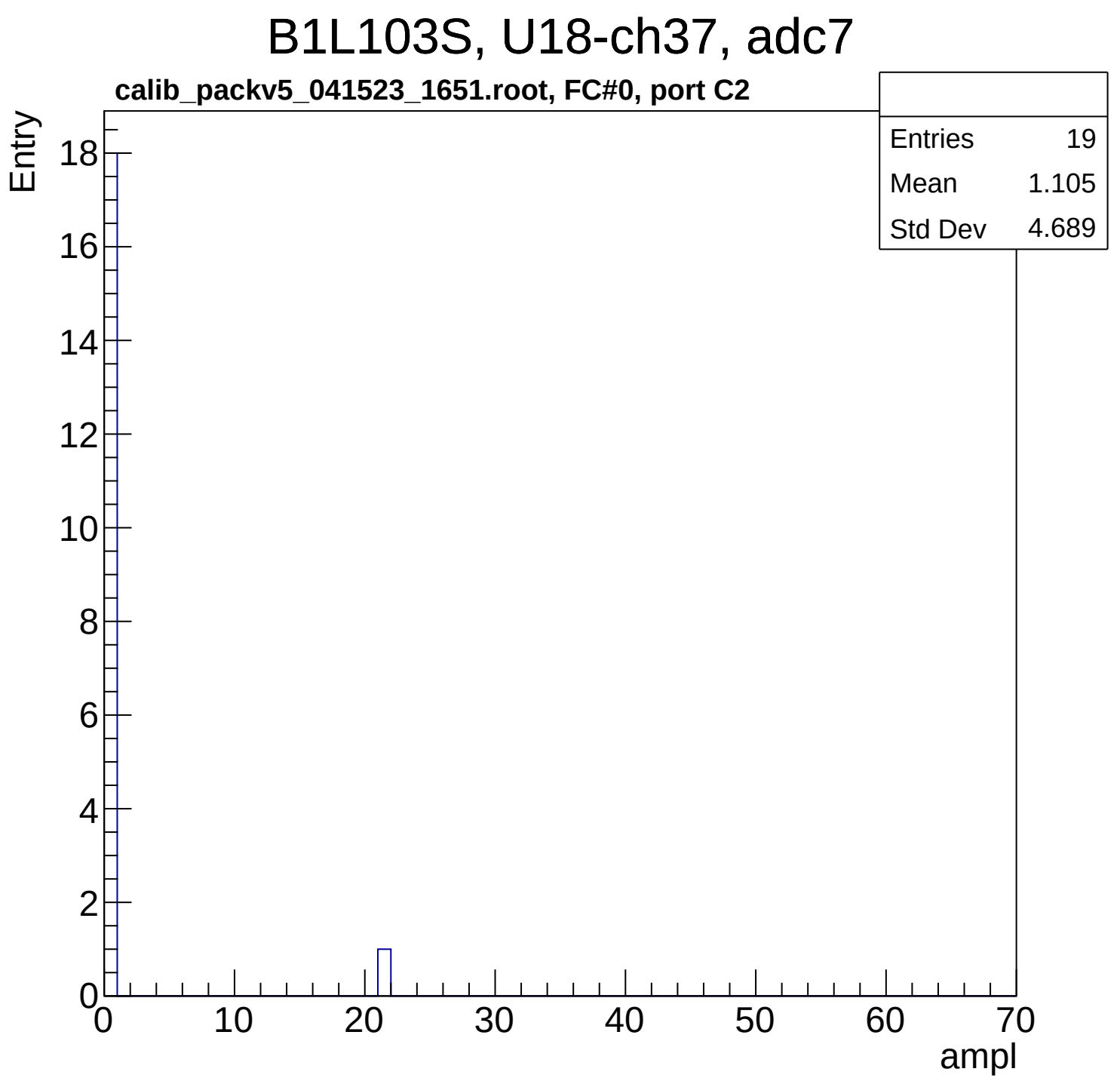

B1L103S, U18-ch37, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 5
Mean 61.6
Std Dev 1.356
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U18-ch37, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.105
Std Dev 4.689
Entry
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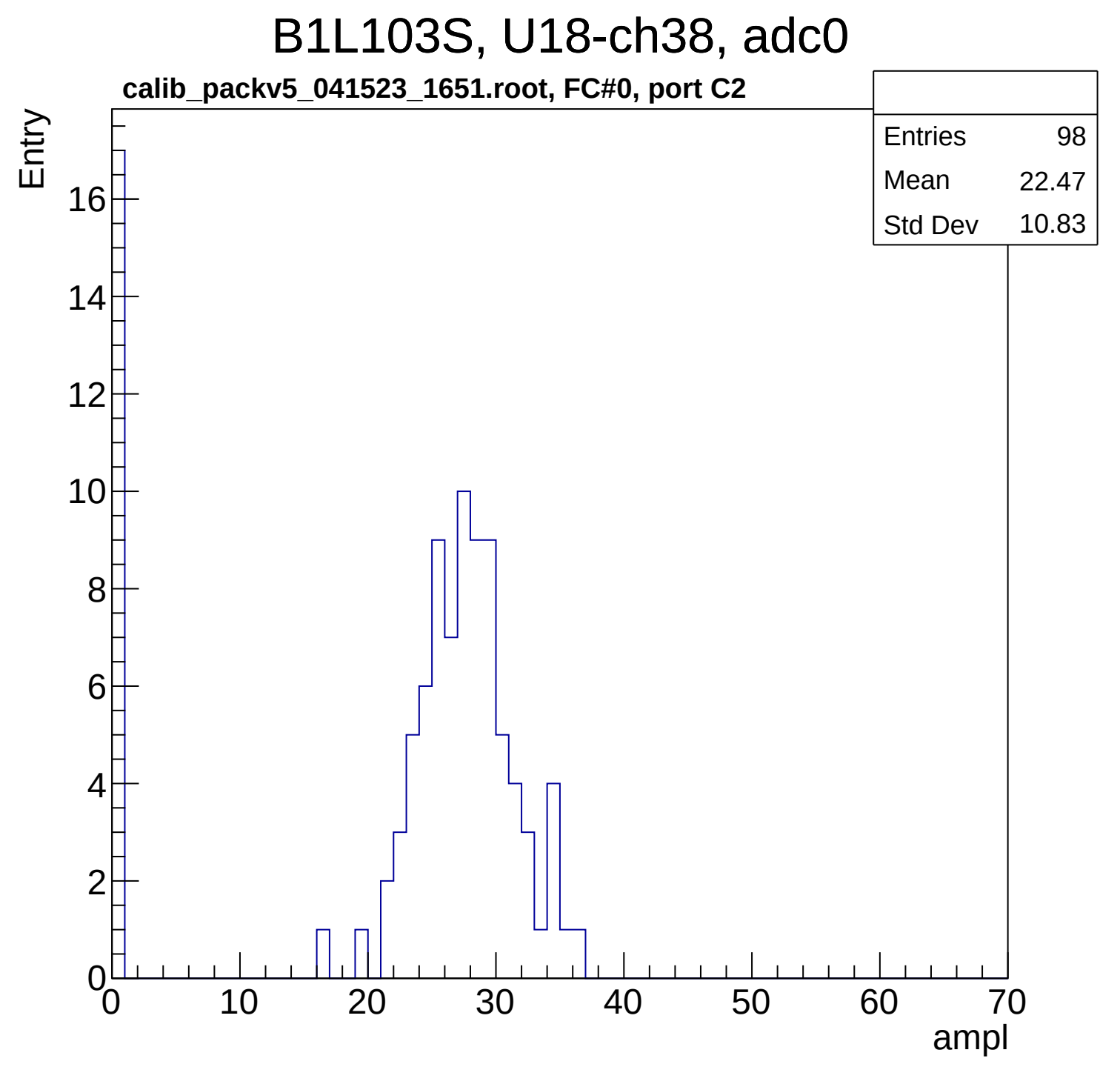
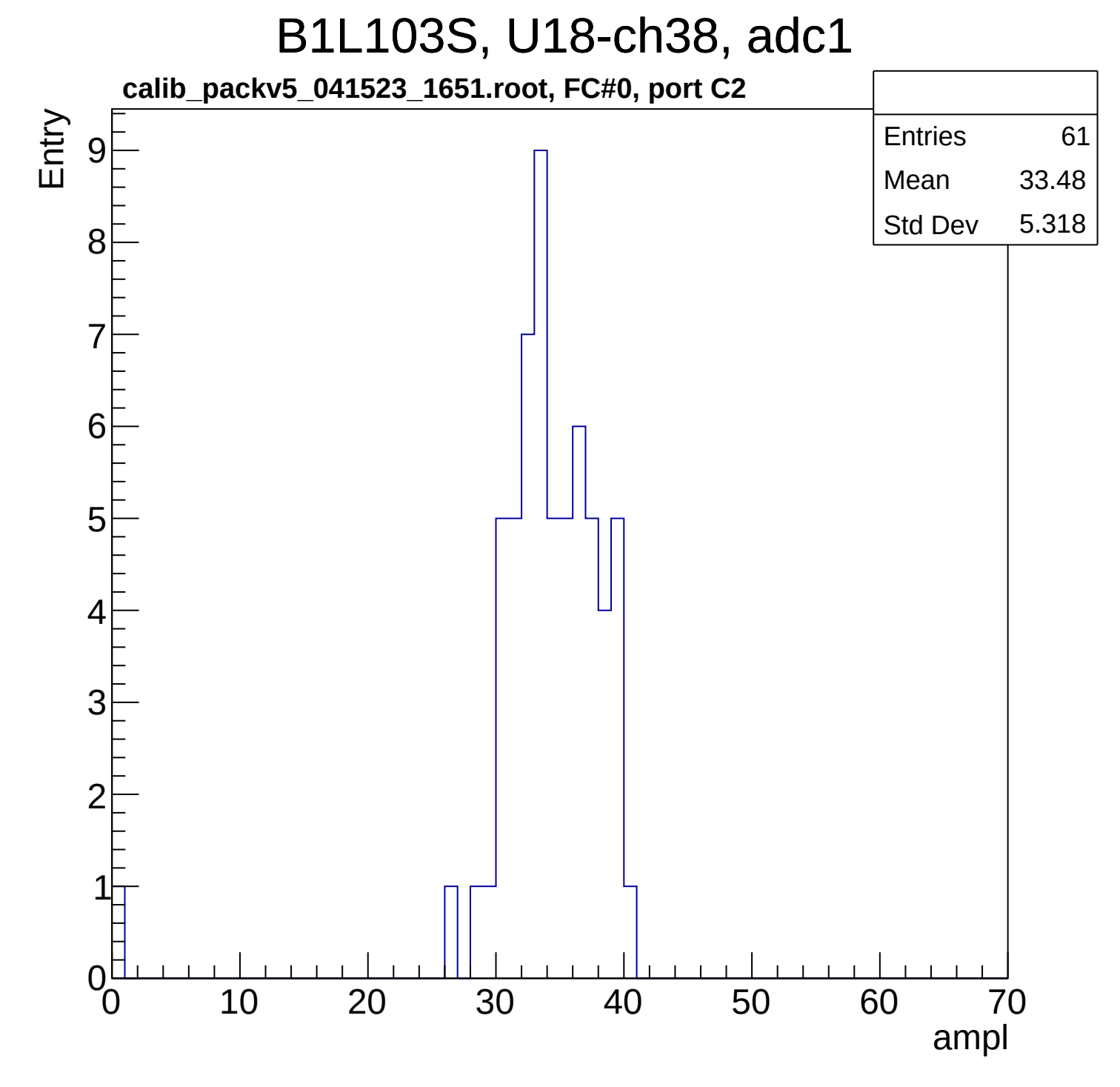
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch38, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 98
Mean 22.47
Std Dev 10.83
Entry
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch38, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 33.48
Std Dev 5.318
Entry
ampl
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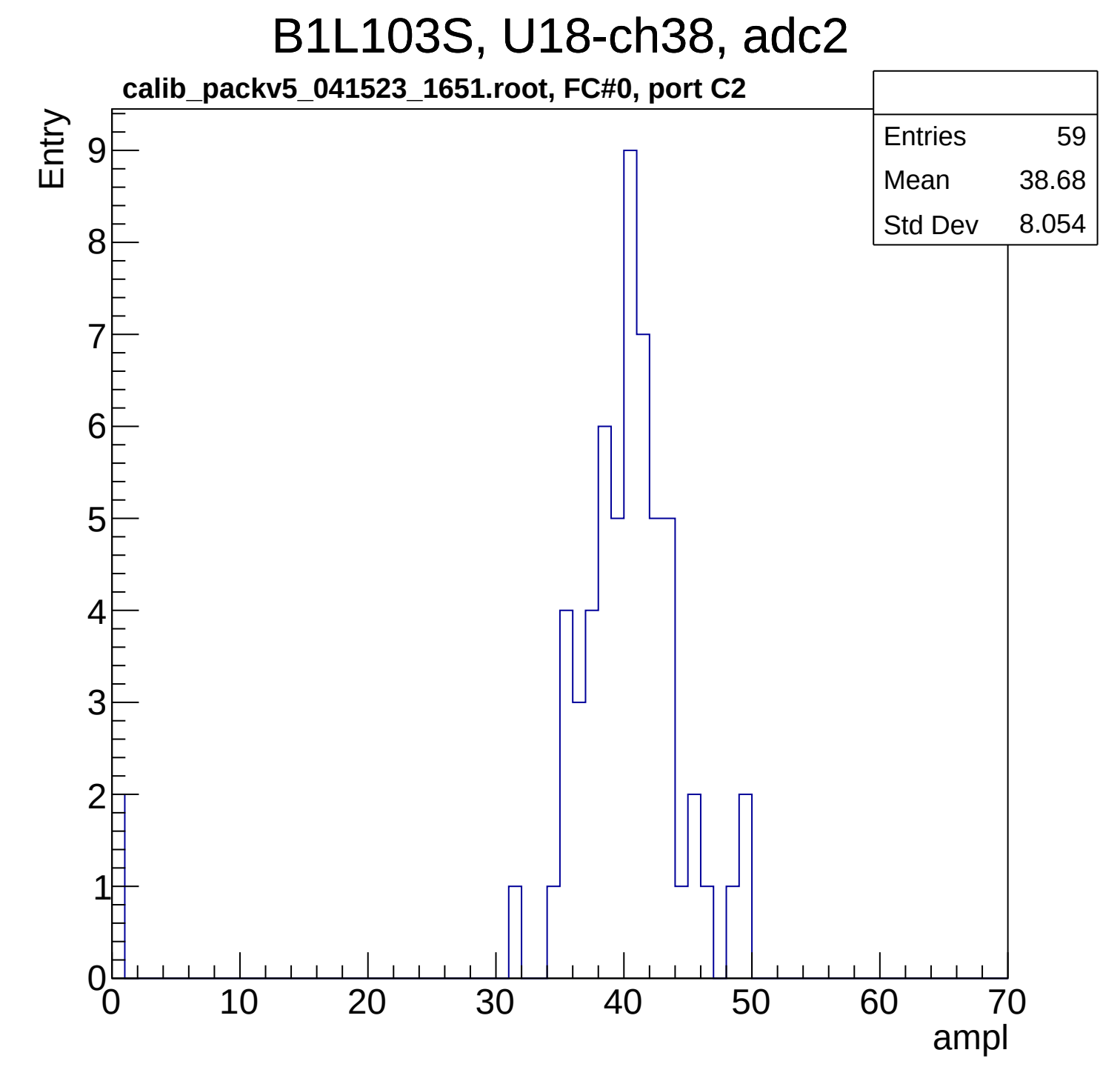
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U18-ch38, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 38.68
Std Dev 8.054
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
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20
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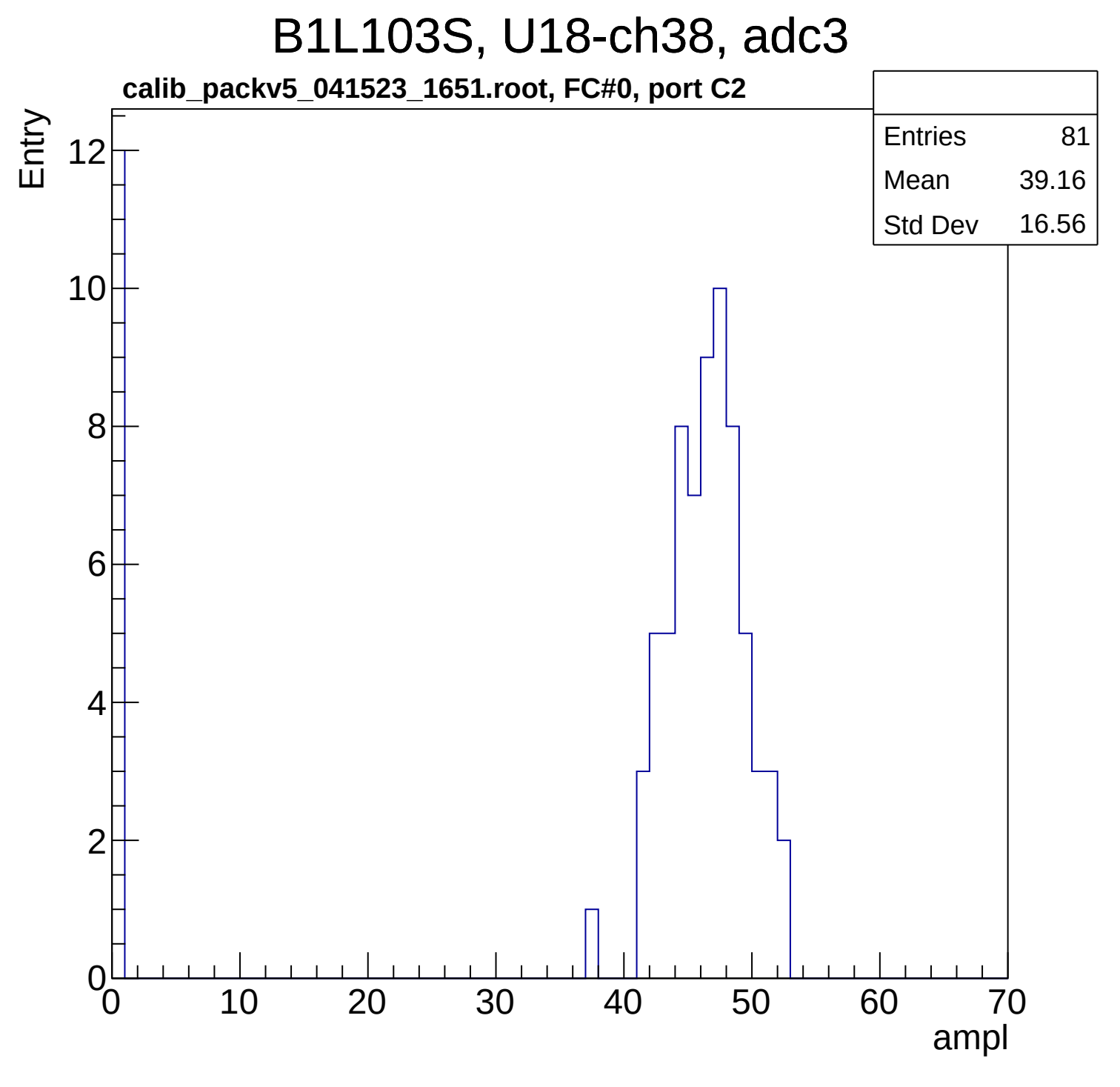
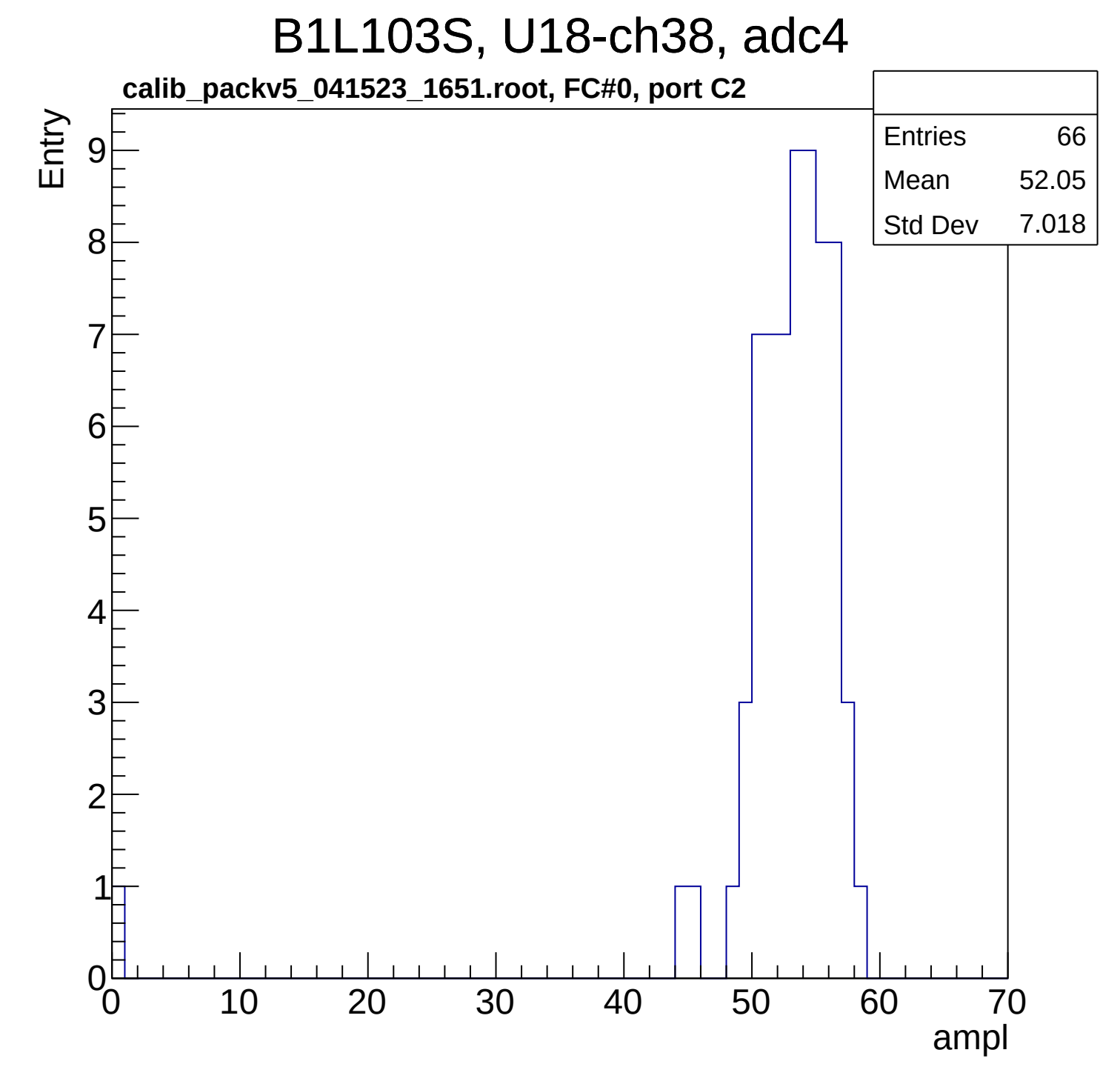
40
50
60
70


B1L103S, U18-ch38, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 39.16
Std Dev 16.56
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch38, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 52.05
Std Dev 7.018
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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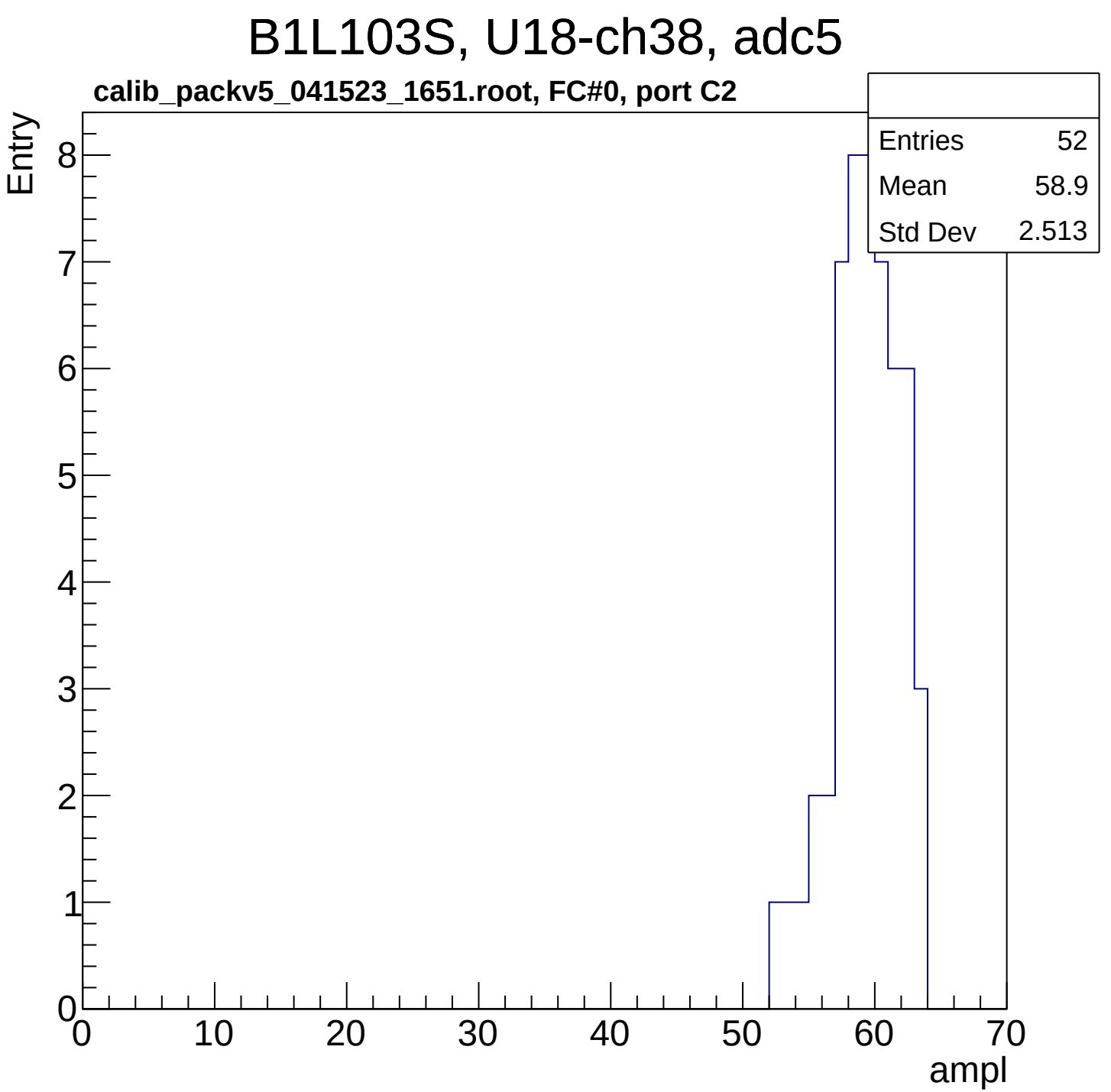
40
50
60
70


B1L103S, U18-ch38, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 58.9
Std Dev 2.513
Entry
ampl
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2
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4
5
6
7
8
0
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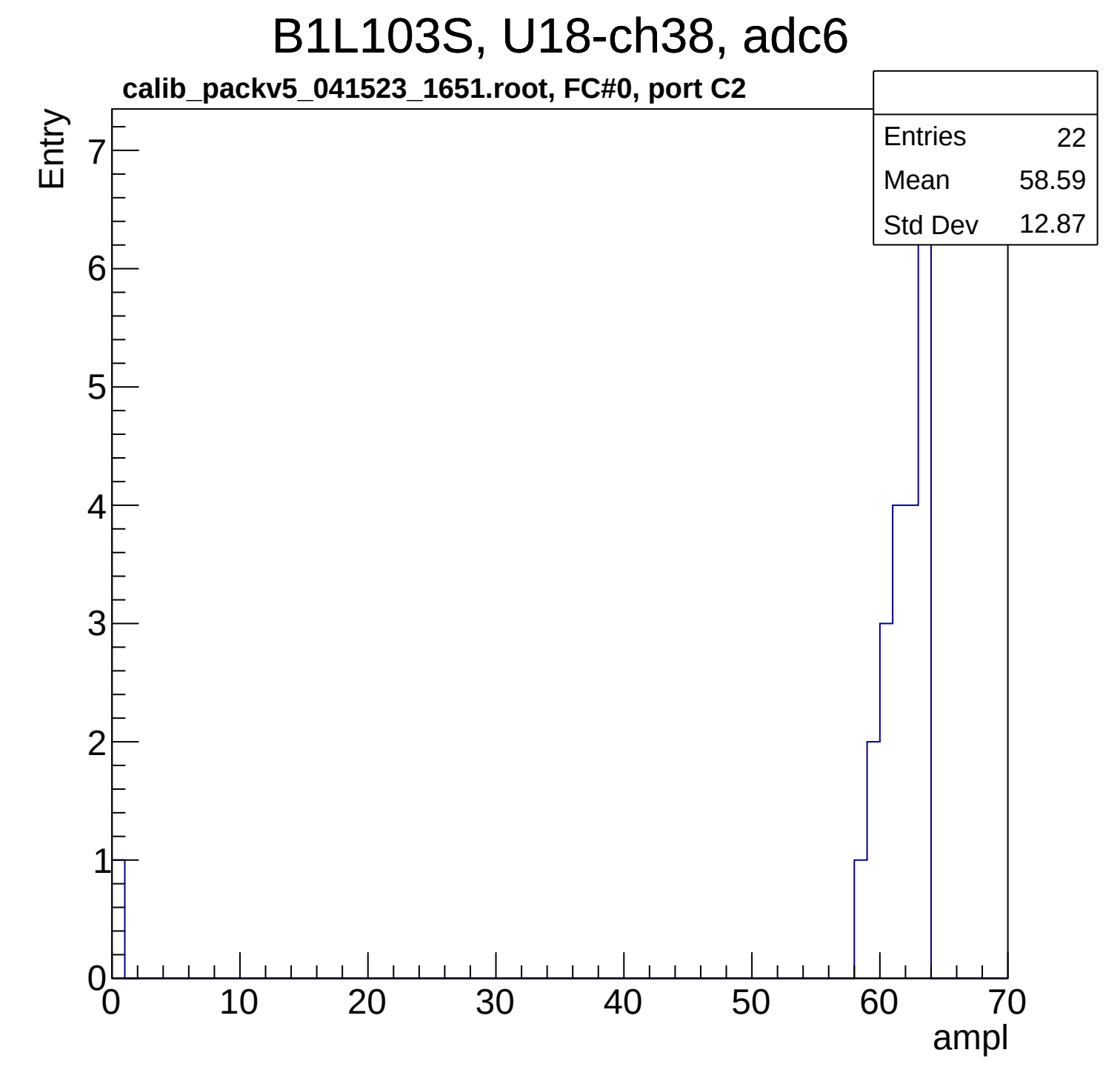
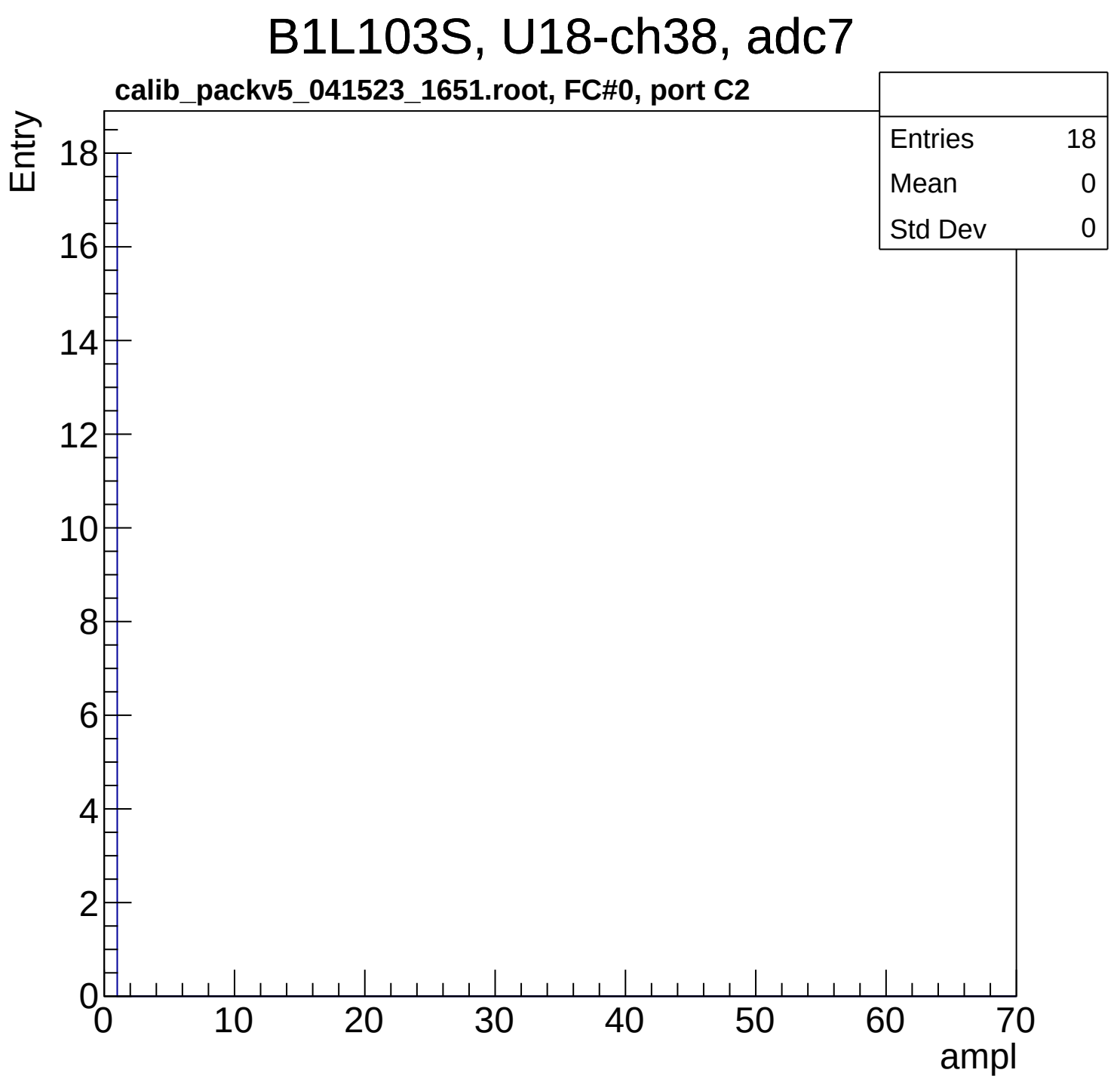
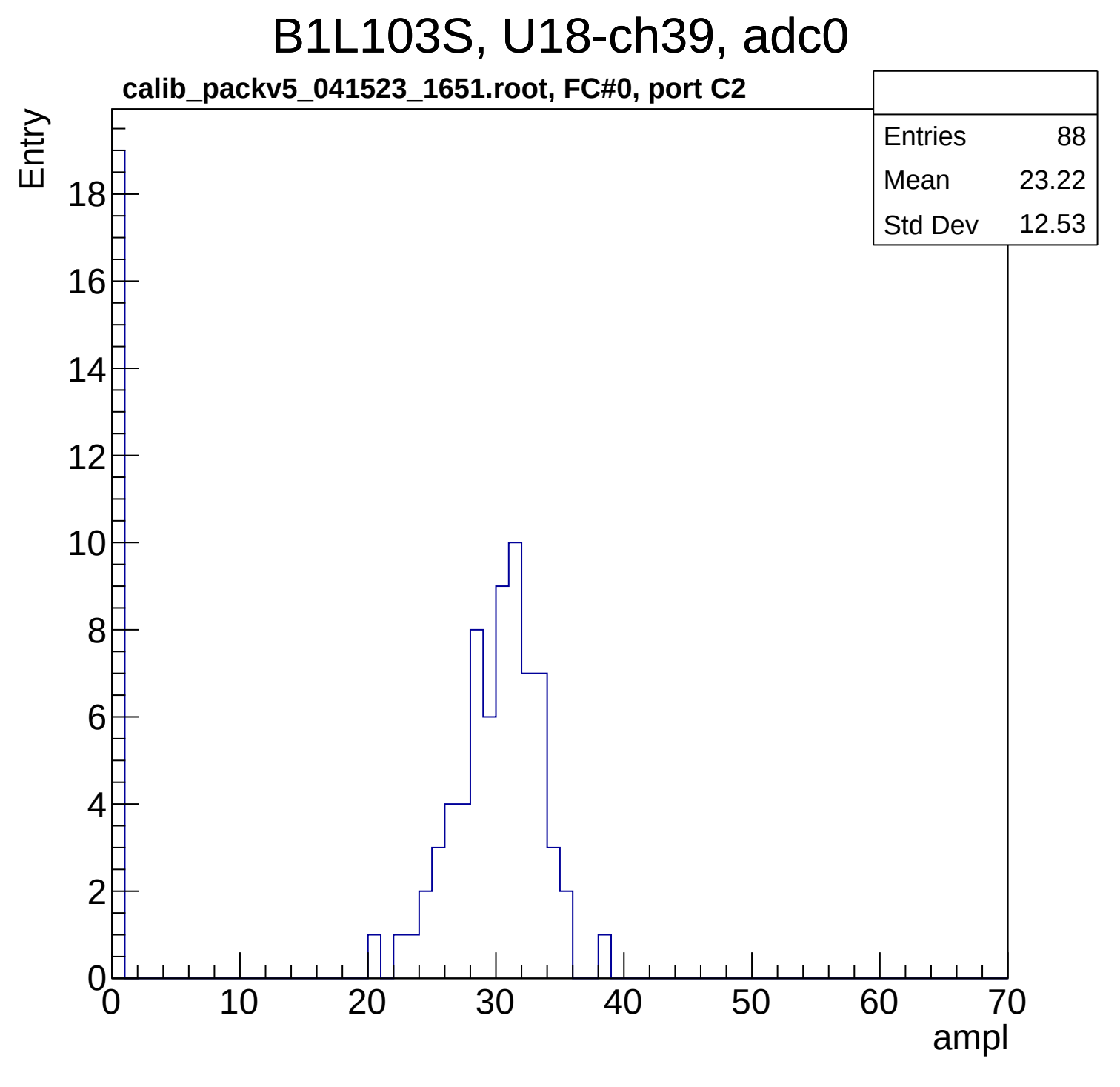
40
50
60
70


B1L103S, U18-ch38, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 58.59
Std Dev 12.87
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U18-ch38, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch39, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 88
Mean 23.22
Std Dev 12.53
Entry
ampl
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6
8
10
12
14
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0
10
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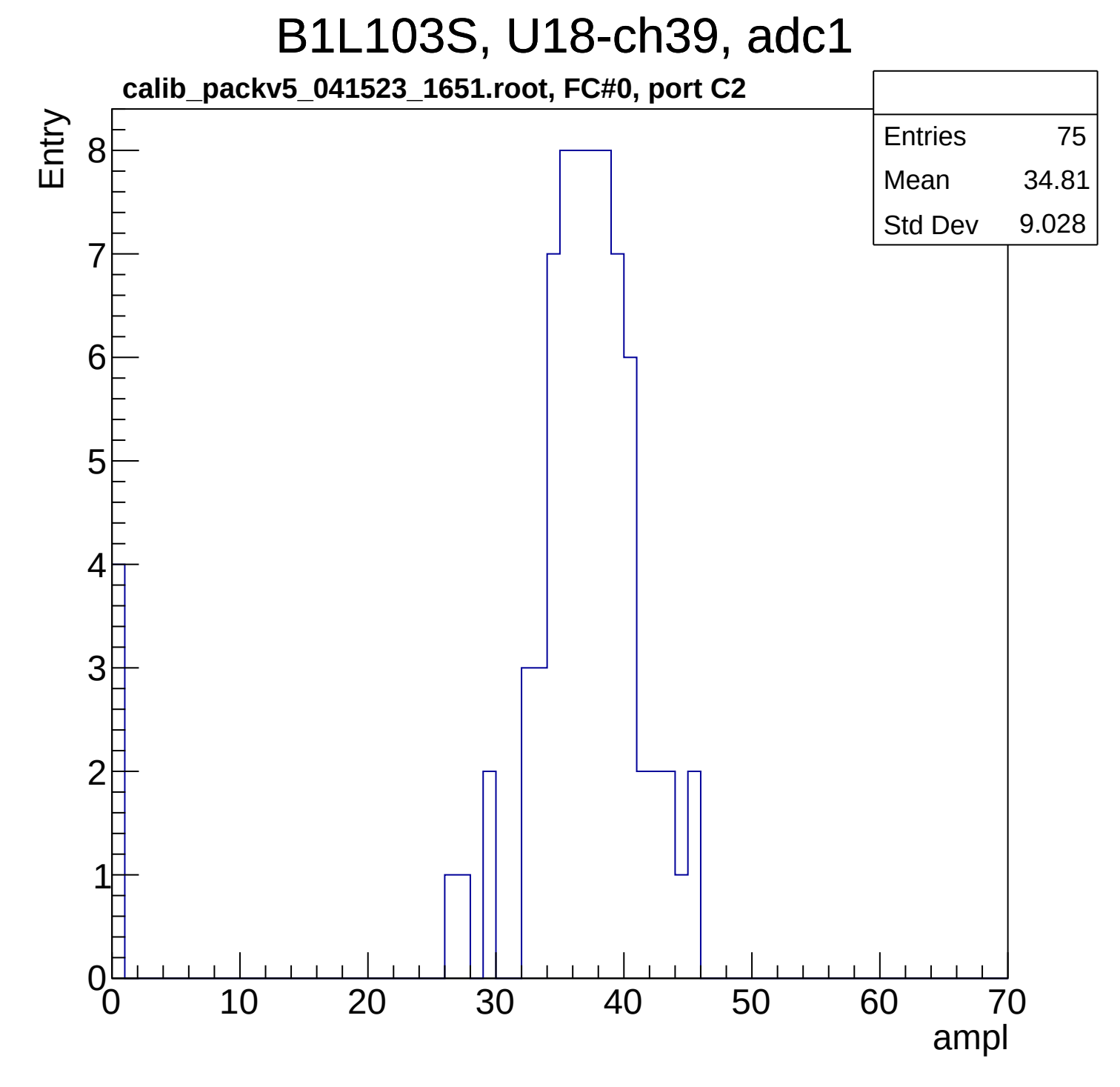
30
40
50
60
70


B1L103S, U18-ch39, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 34.81
Std Dev 9.028
Entry
ampl
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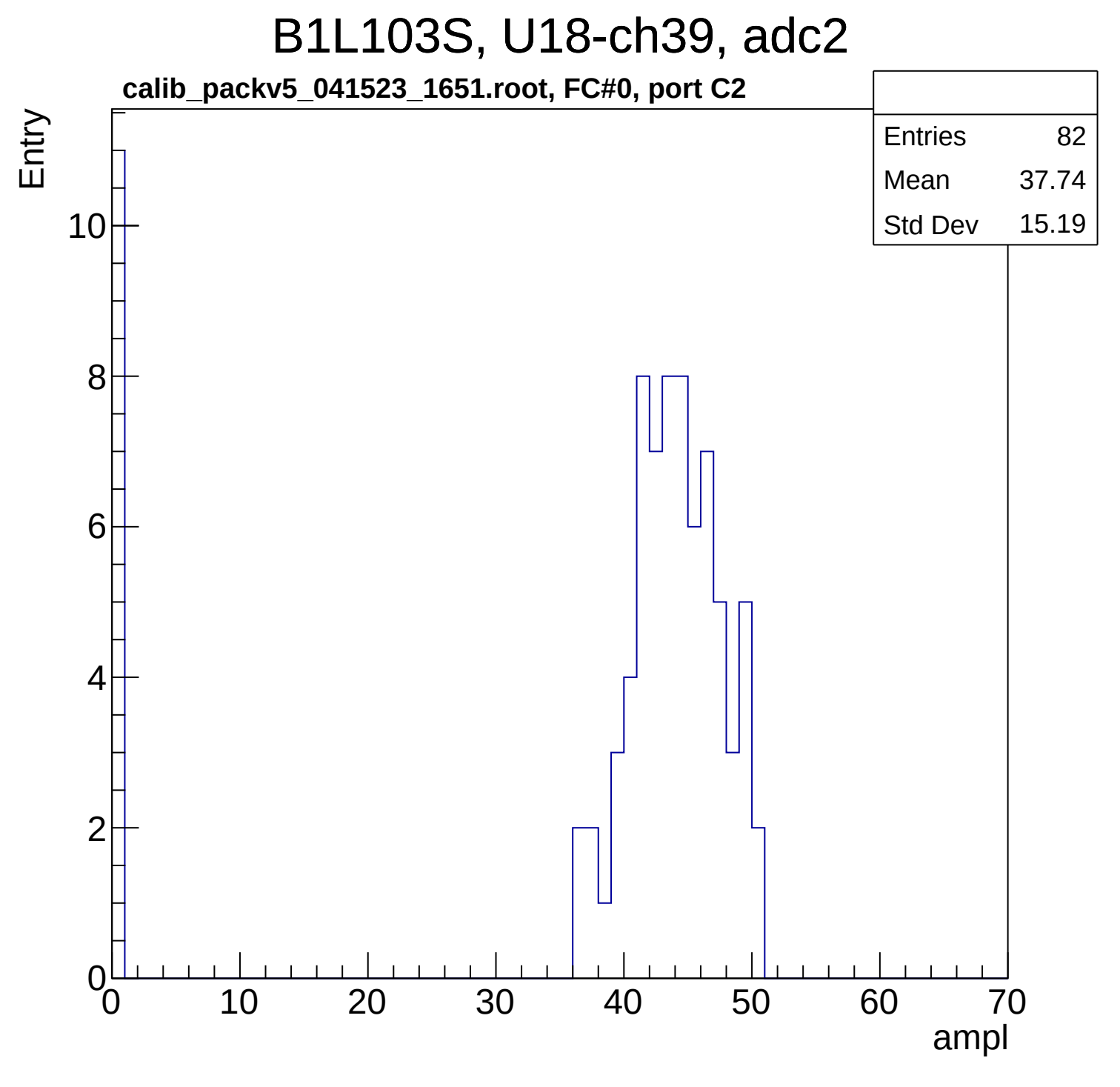
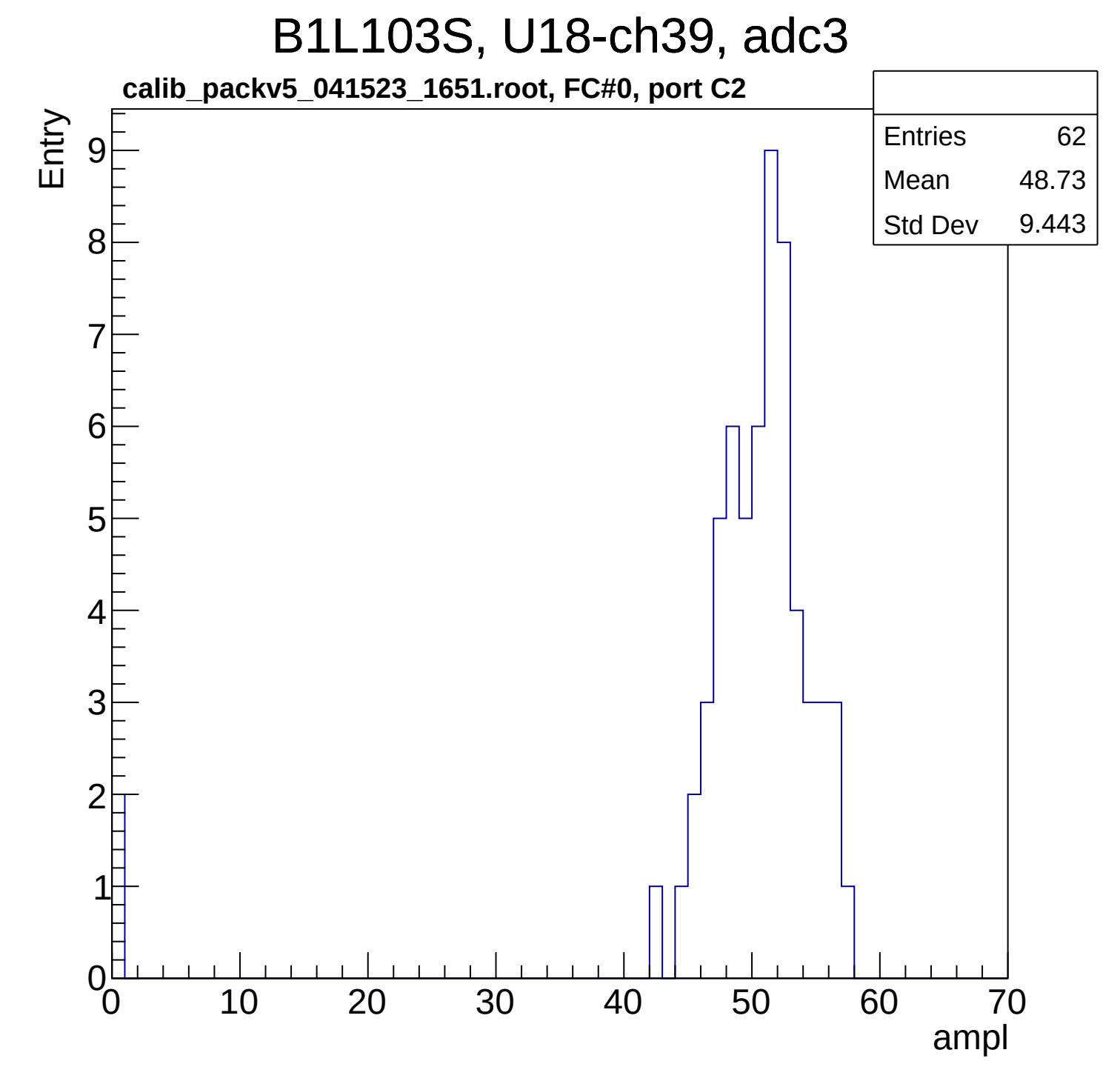
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch39, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 37.74
Std Dev 15.19
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch39, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 48.73
Std Dev 9.443
Entry
ampl
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2
3
4
5
6
7
8
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0
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40
50
60
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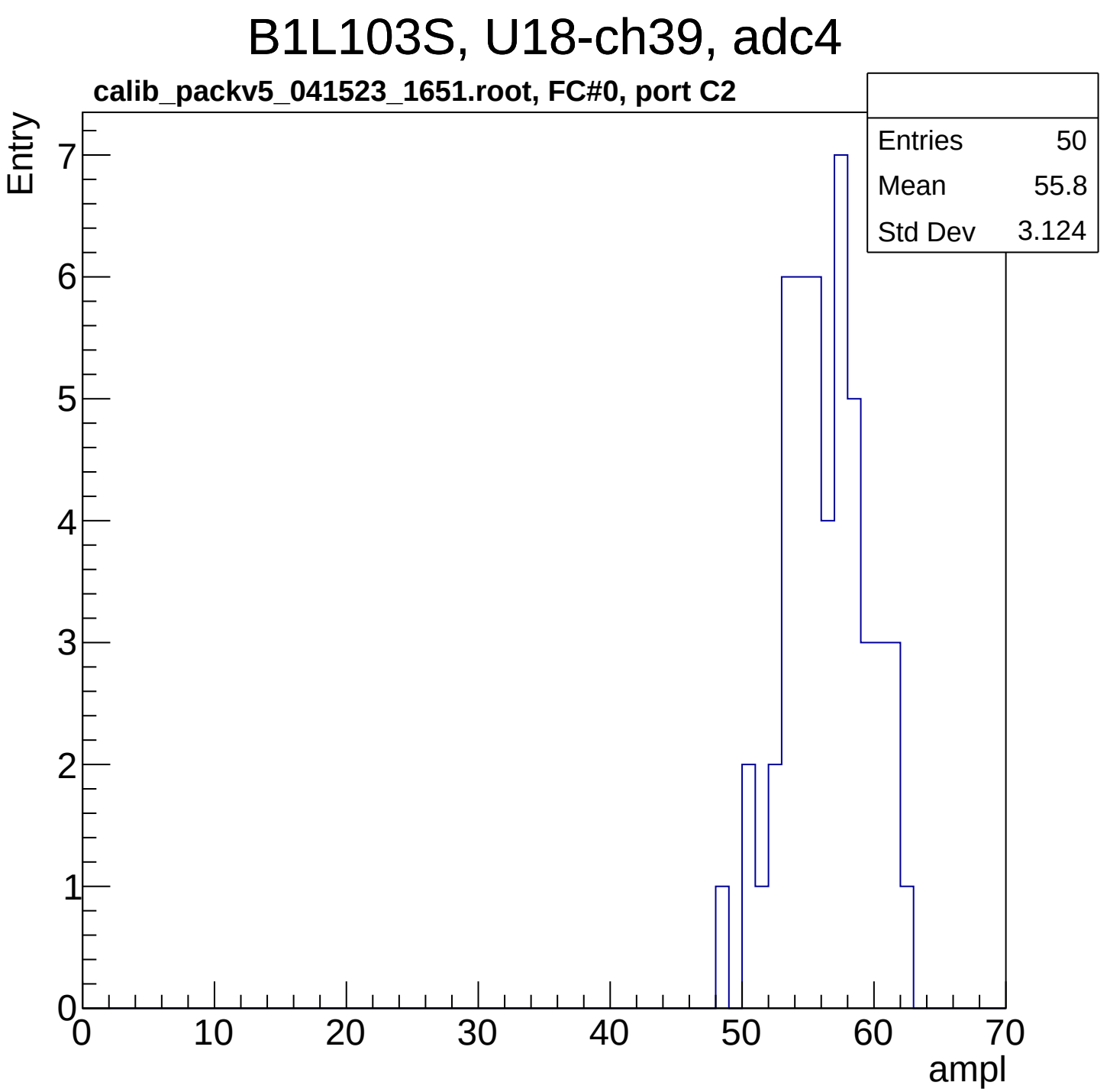
B1L103S, U18-ch39, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 55.8
Std Dev 3.124
Entry
ampl
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4
5
6
7
0
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30
40
50
60
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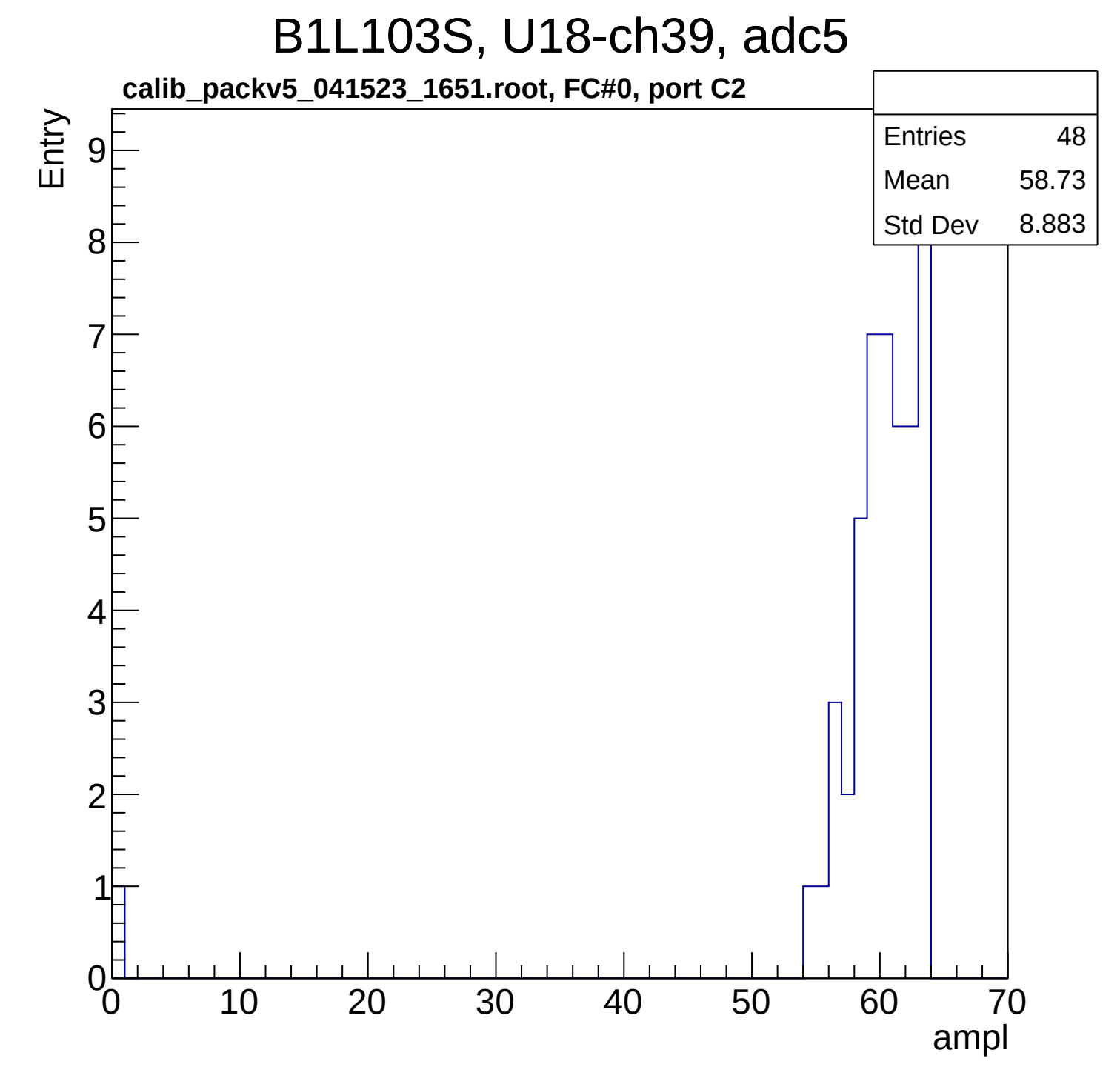
B1L103S, U18-ch39, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 58.73
Std Dev 8.883
Entry
ampl
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3
4
5
6
7
8
9
0
10
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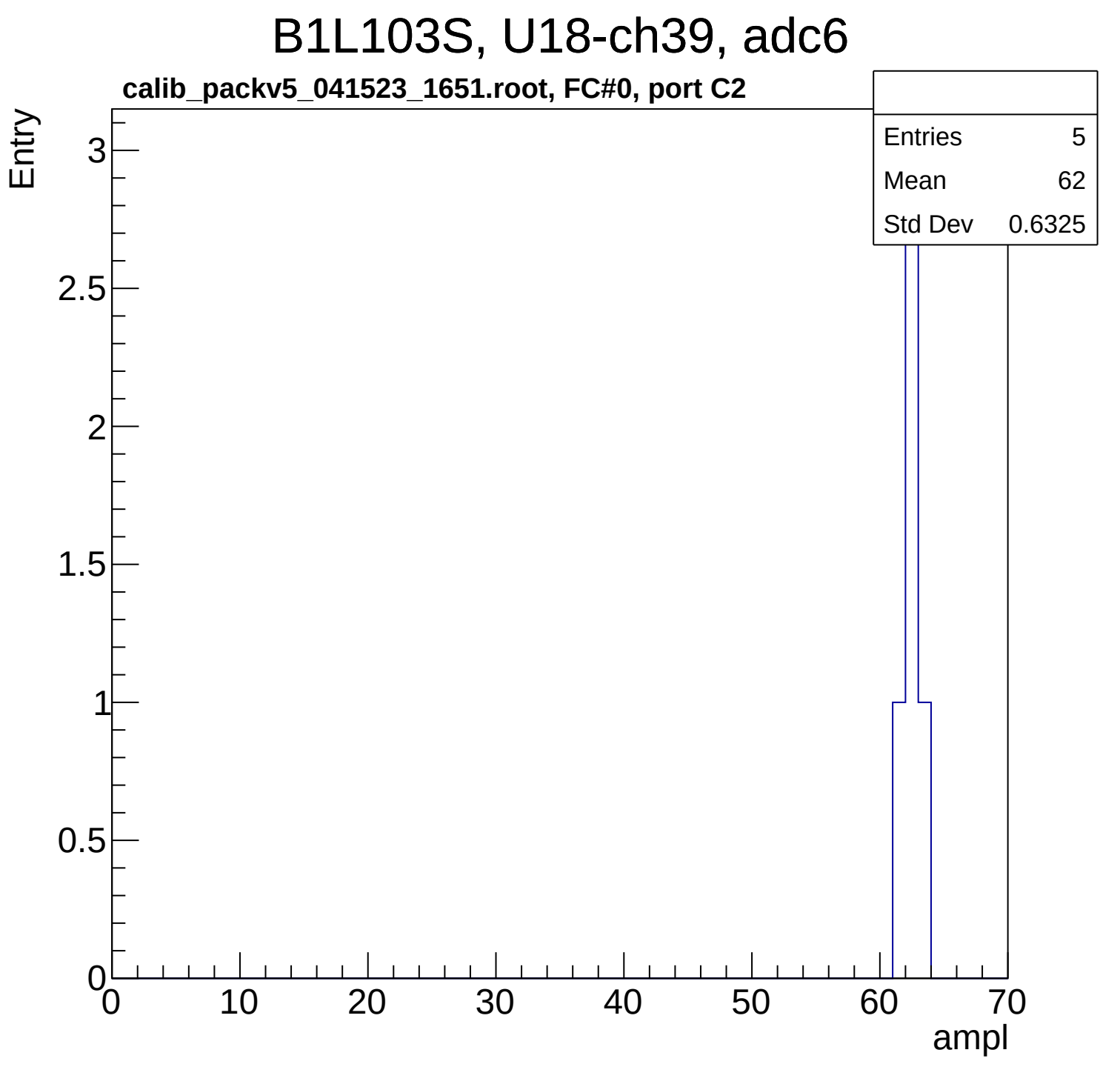
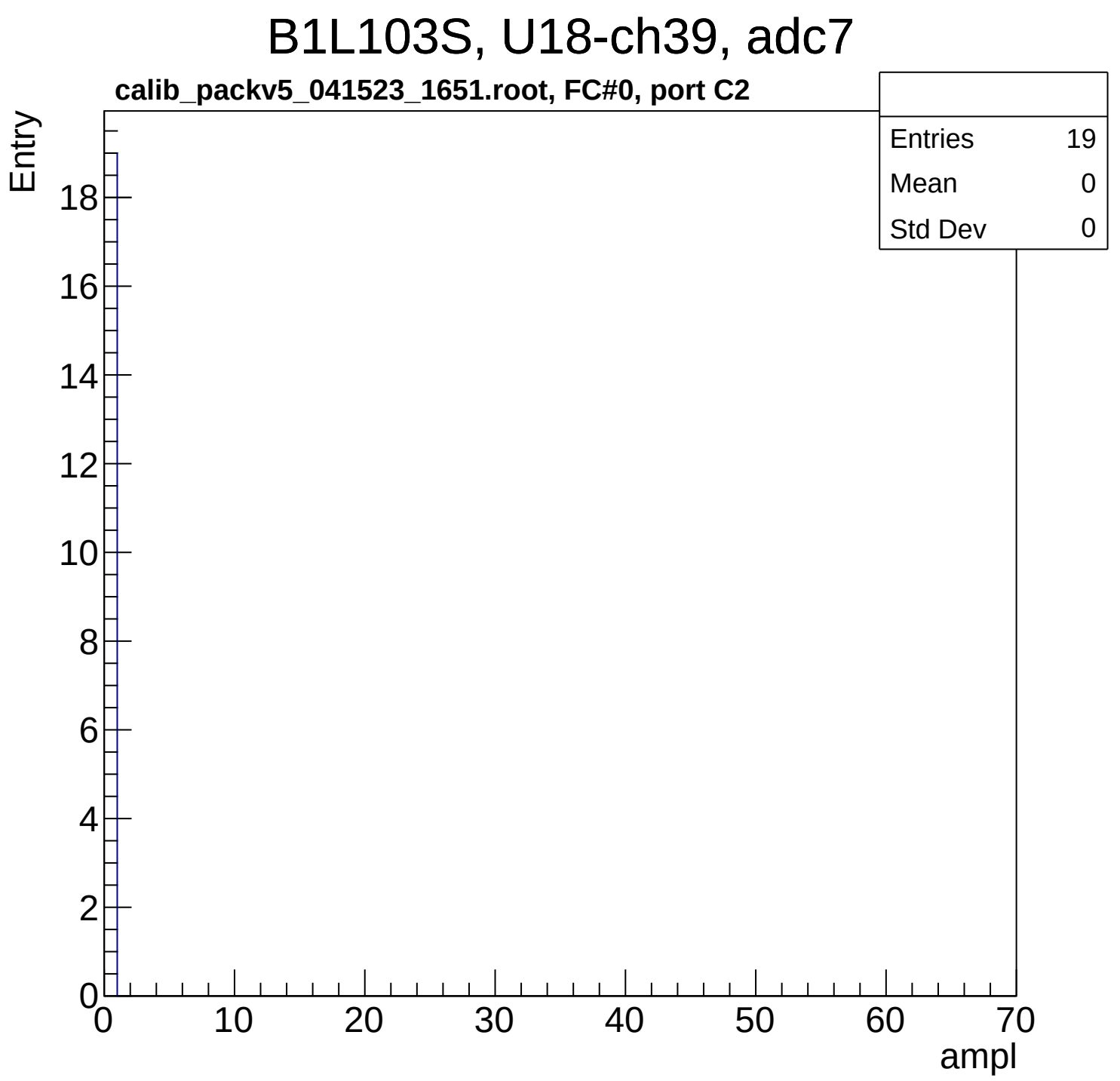
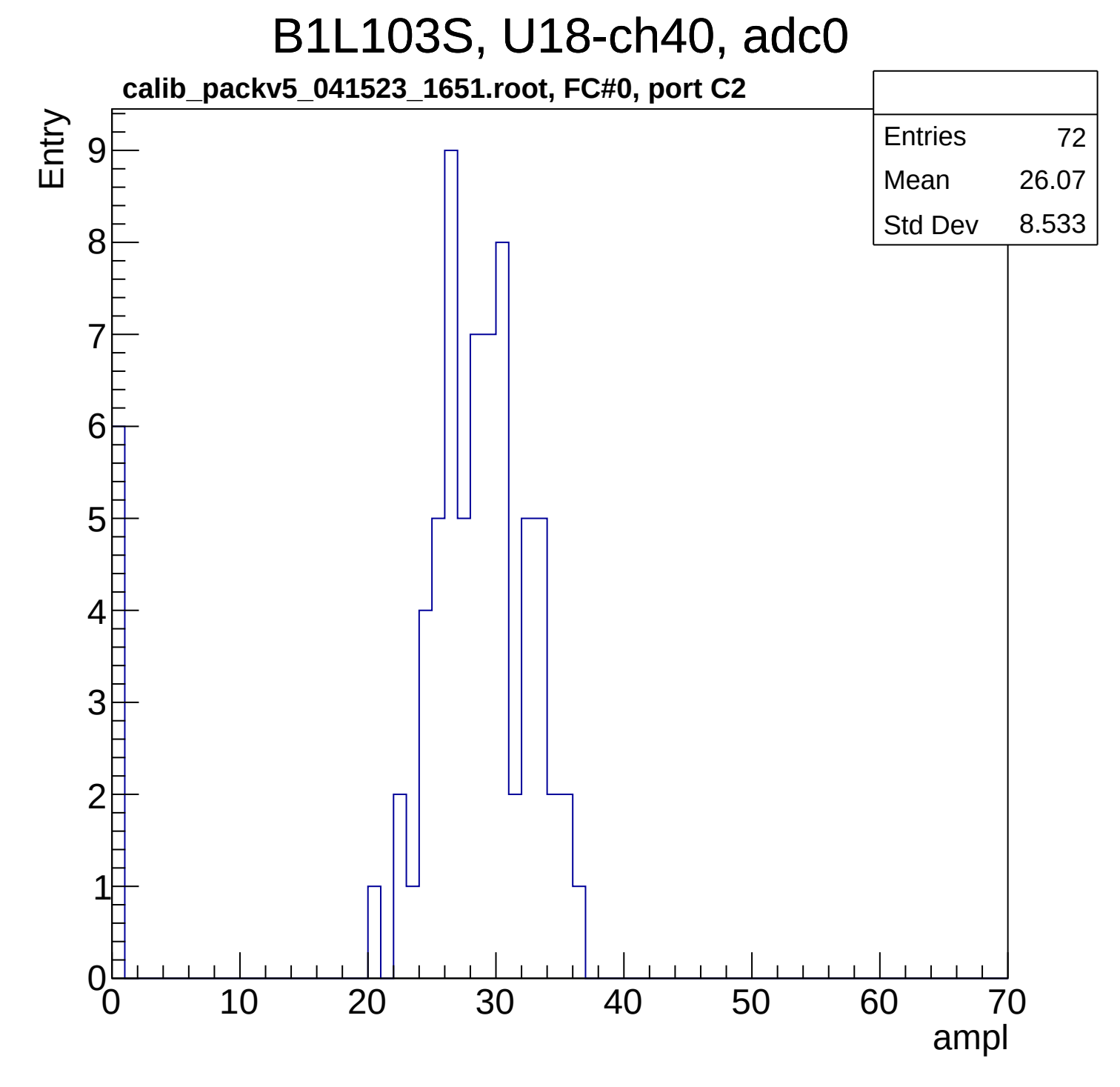
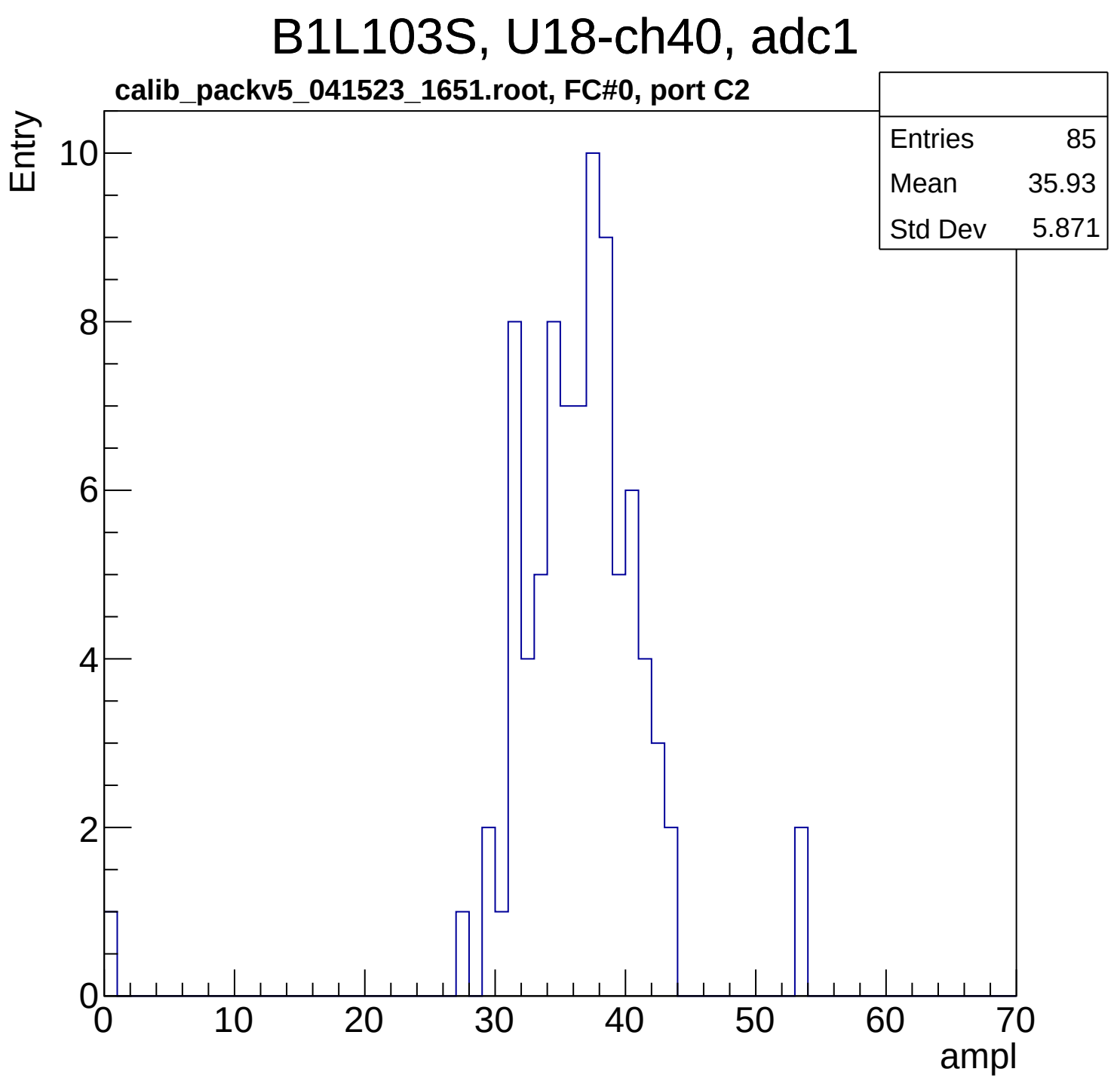
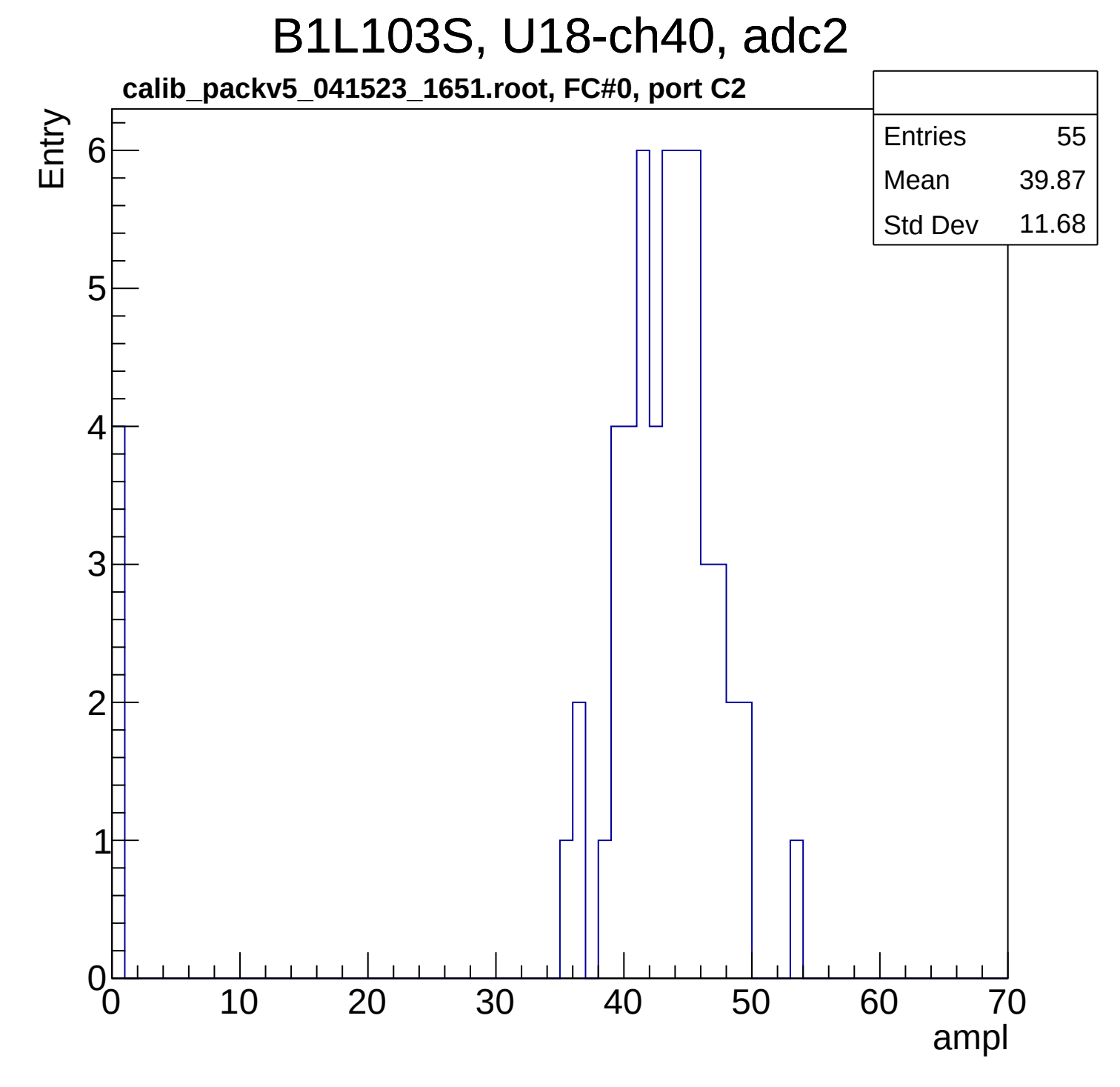
30
40
50
60
70

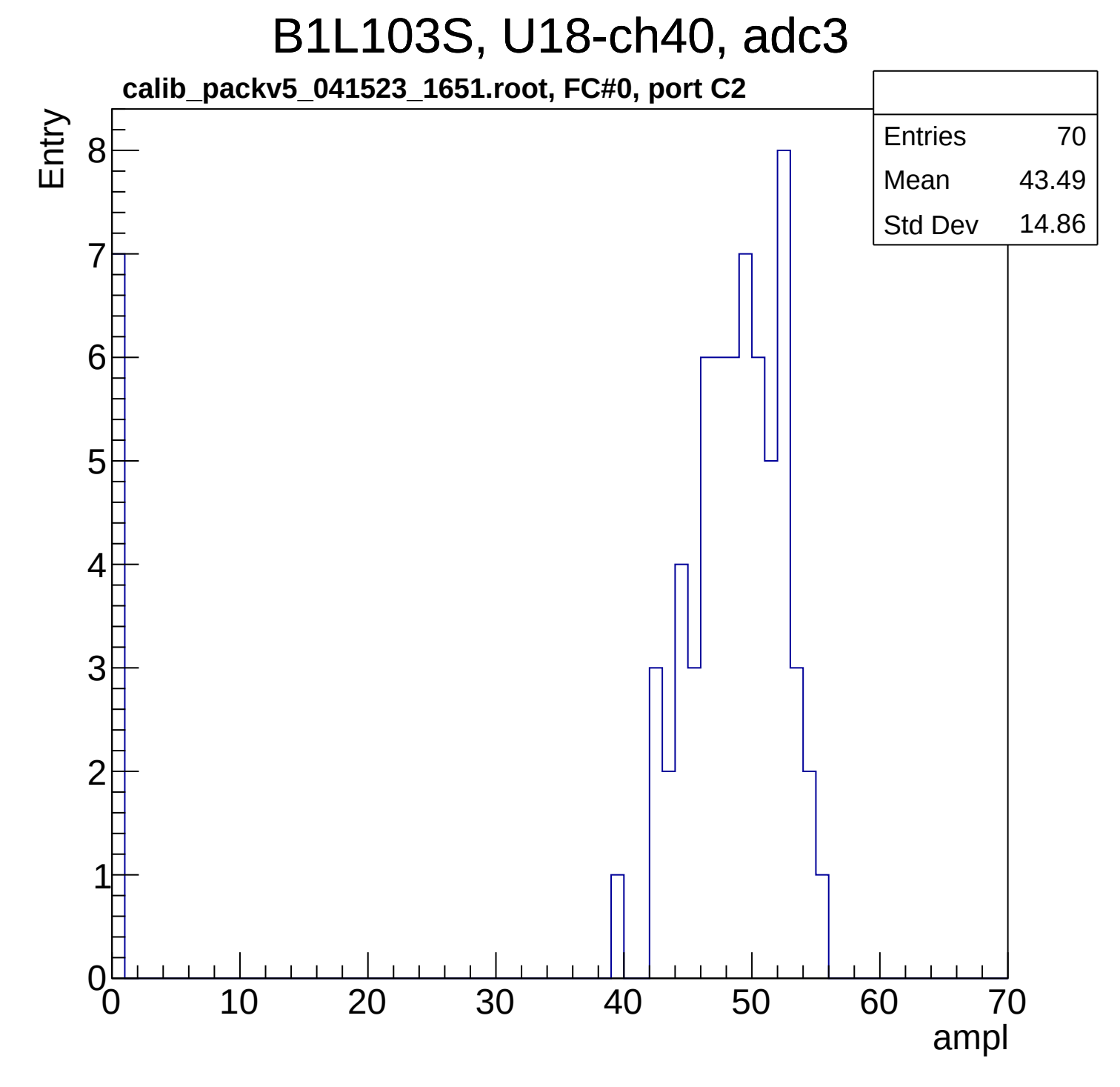

B1L103S, U18-ch39, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 5
Mean 62
Std Dev 0.6325
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

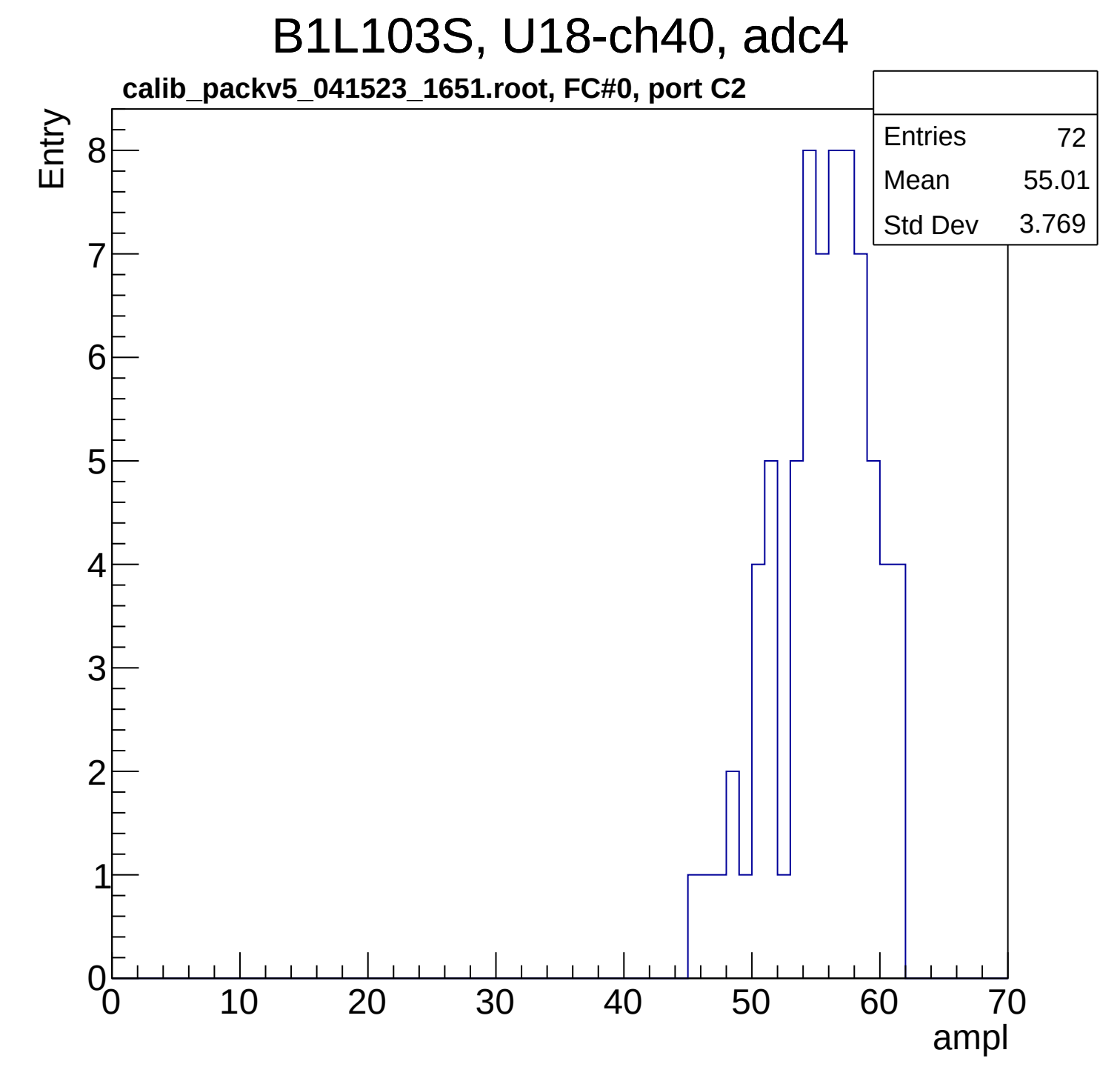

B1L103S, U18-ch39, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch40, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 26.07
Std Dev 8.533
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U18-ch40, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 35.93
Std Dev 5.871
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U18-ch40, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 39.87
Std Dev 11.68
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch40, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 43.49
Std Dev 14.86
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch40, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 55.01
Std Dev 3.769
Entry
ampl
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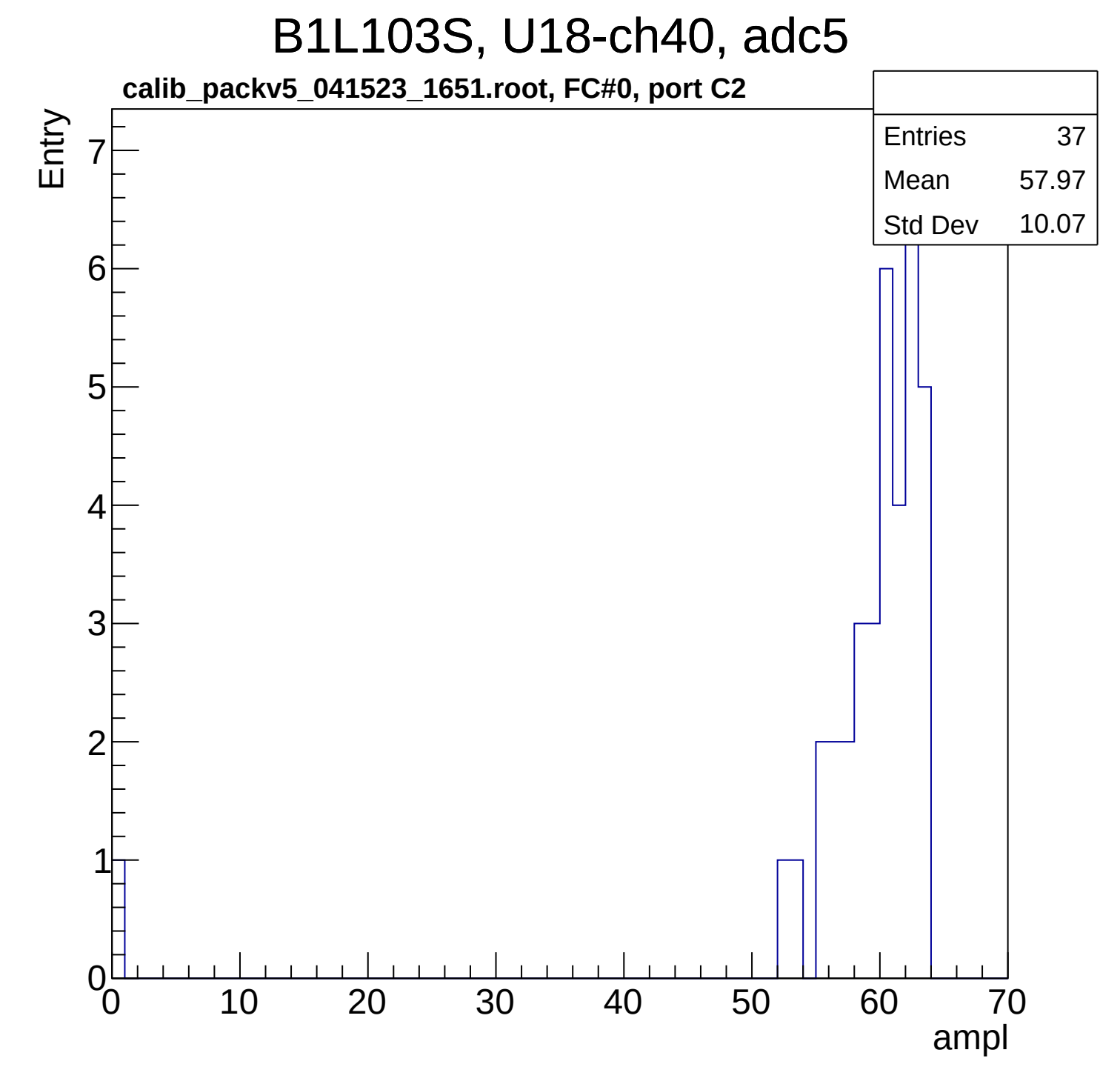
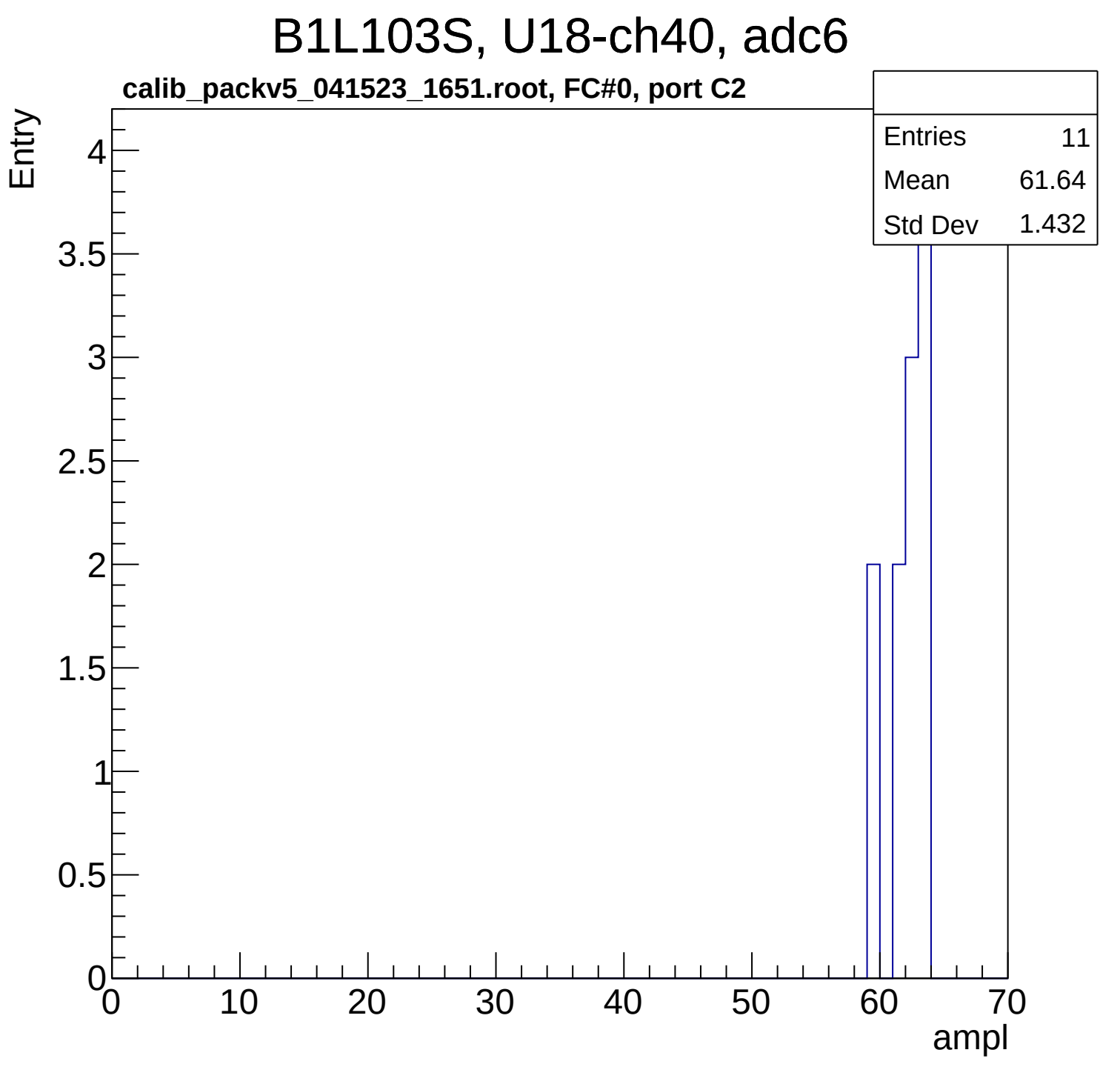
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch40, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 37
Mean 57.97
Std Dev 10.07
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U18-ch40, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 61.64
Std Dev 1.432
Entry
ampl
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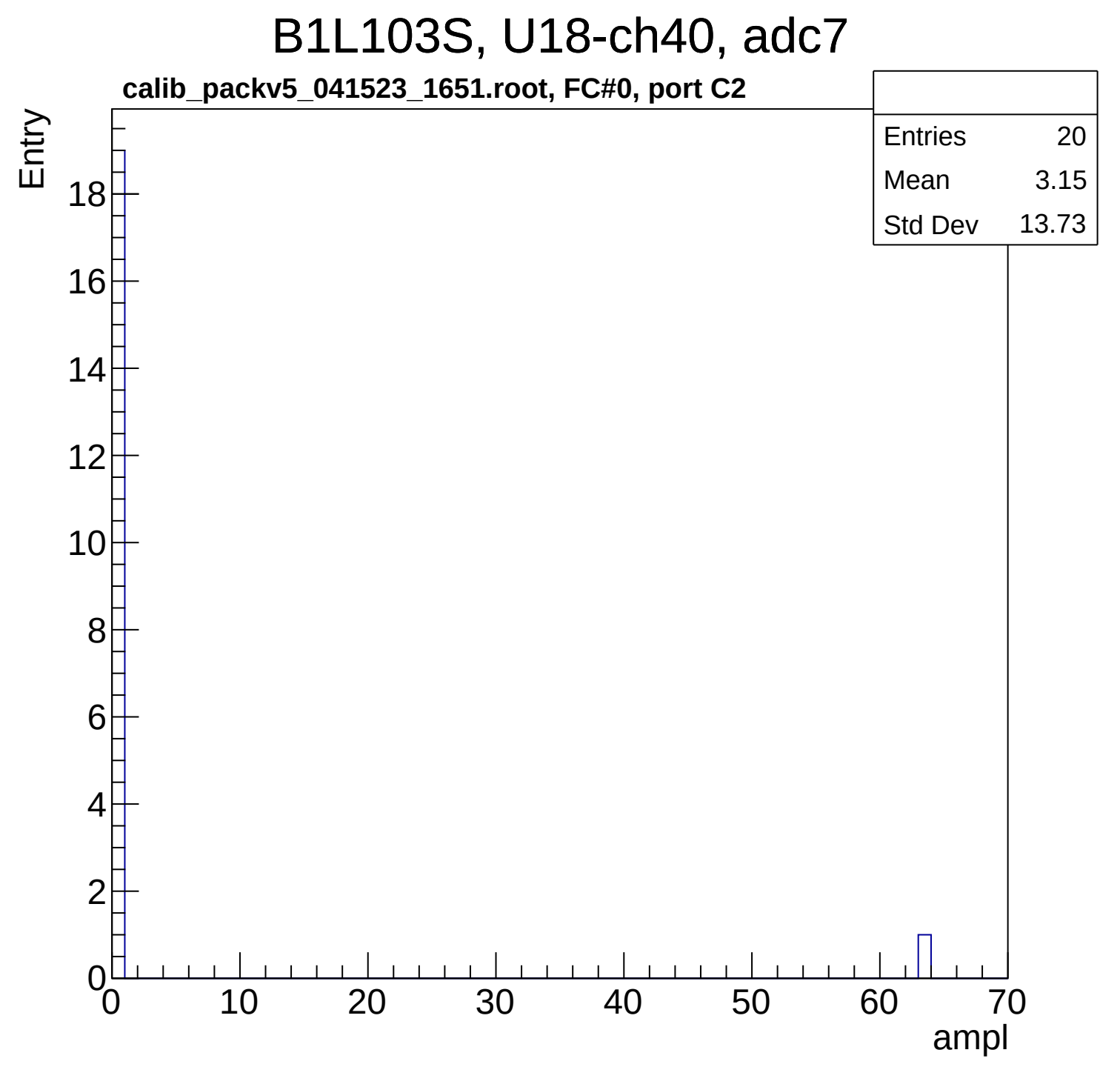
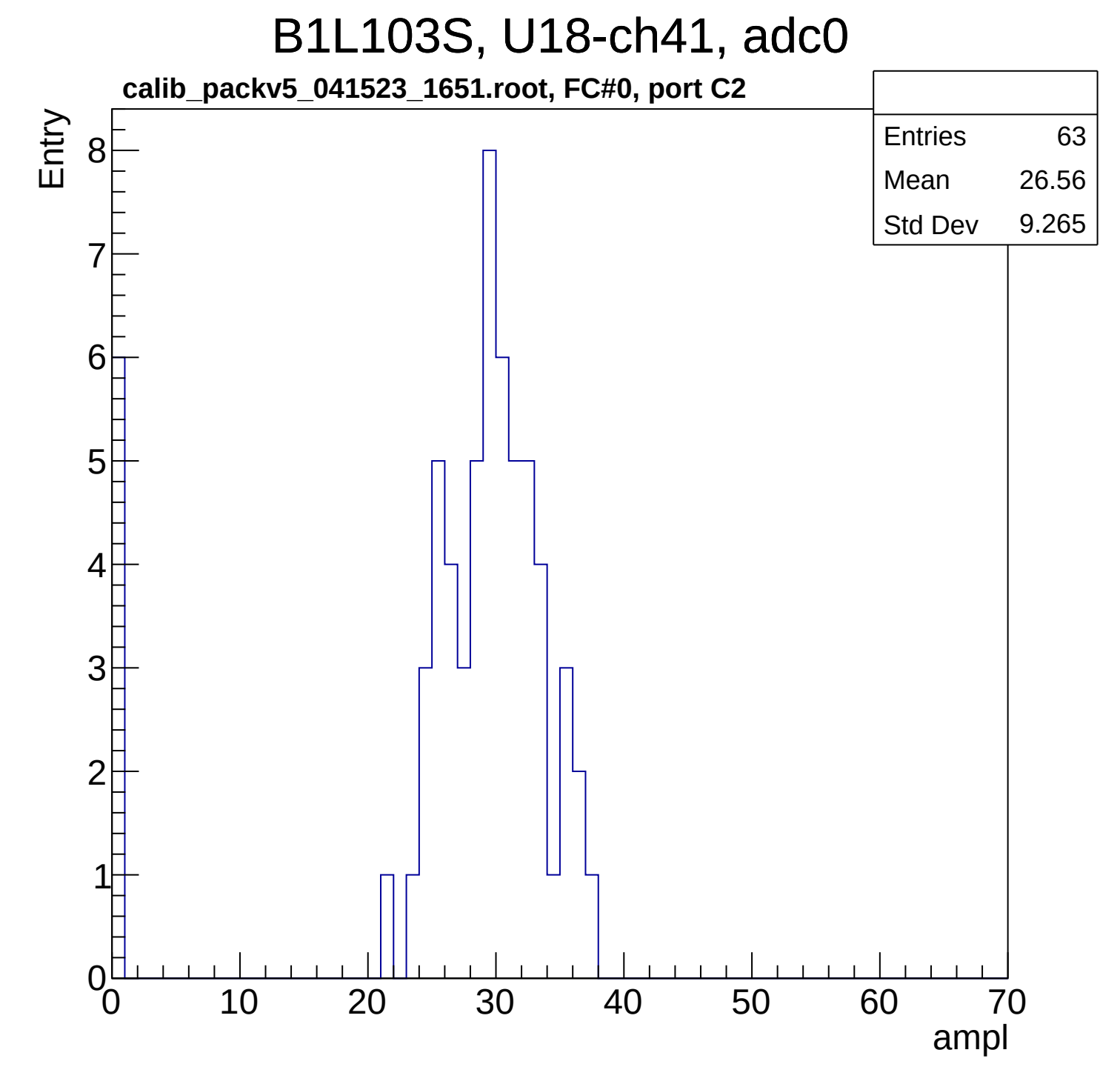
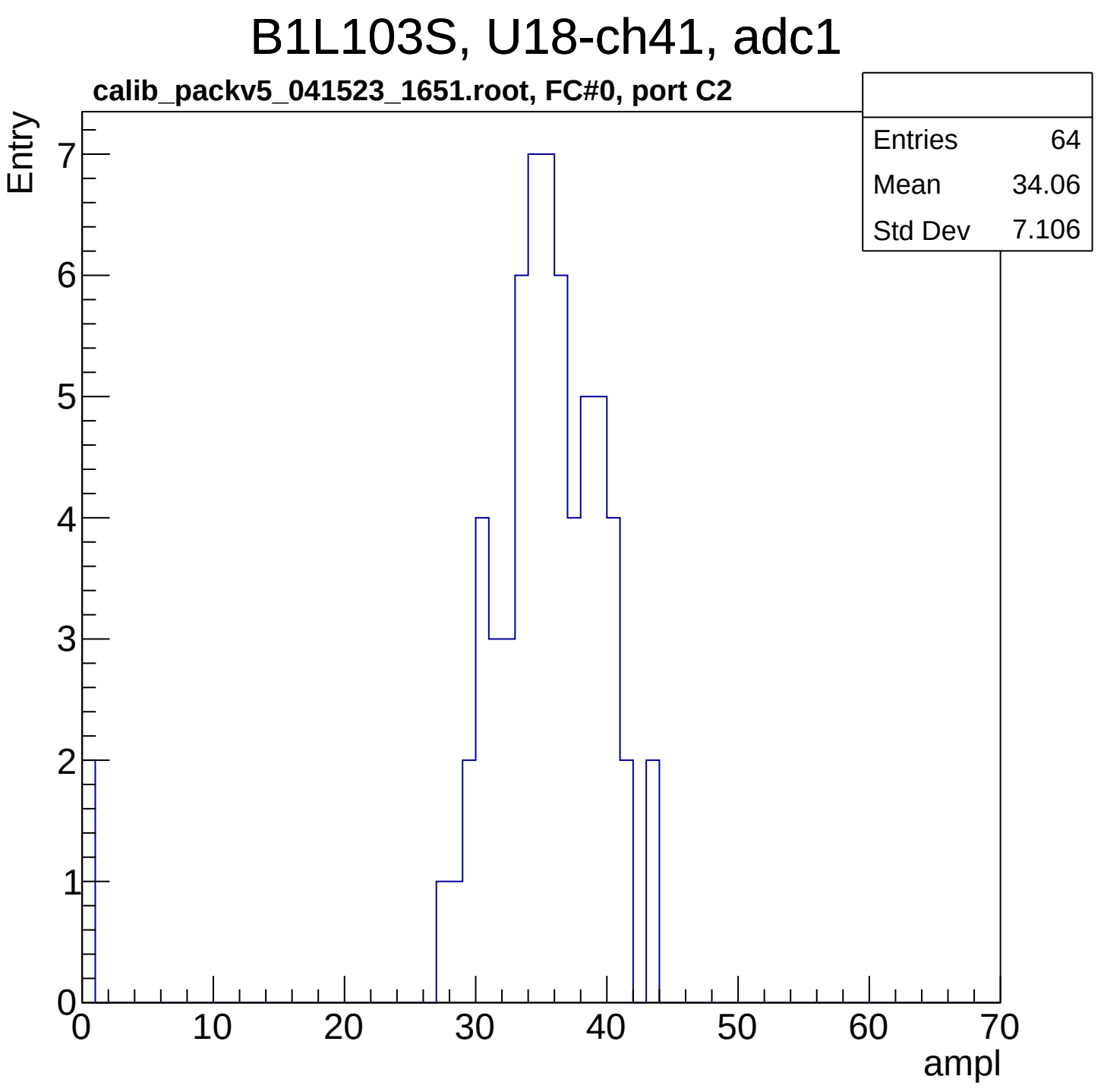
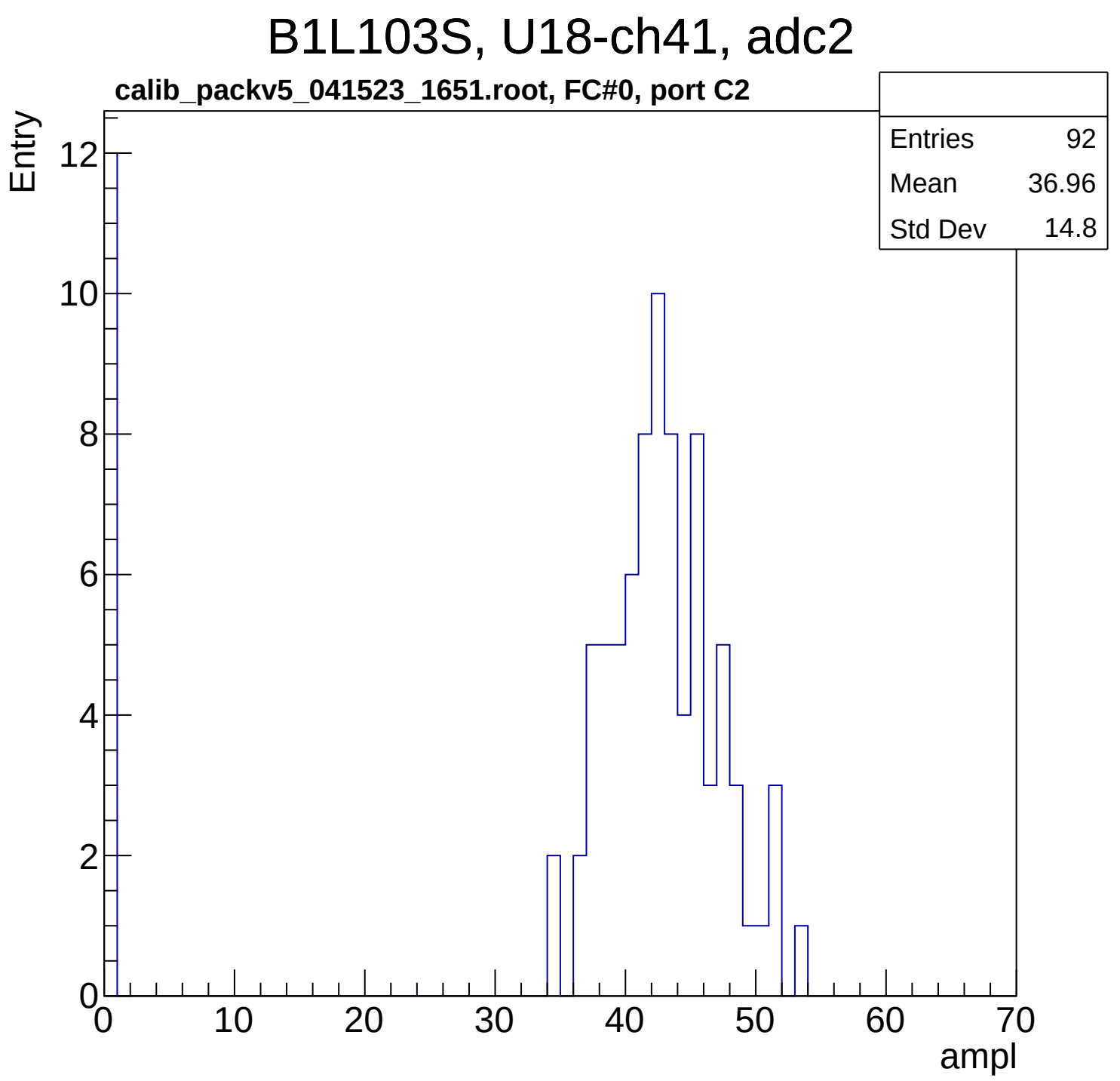
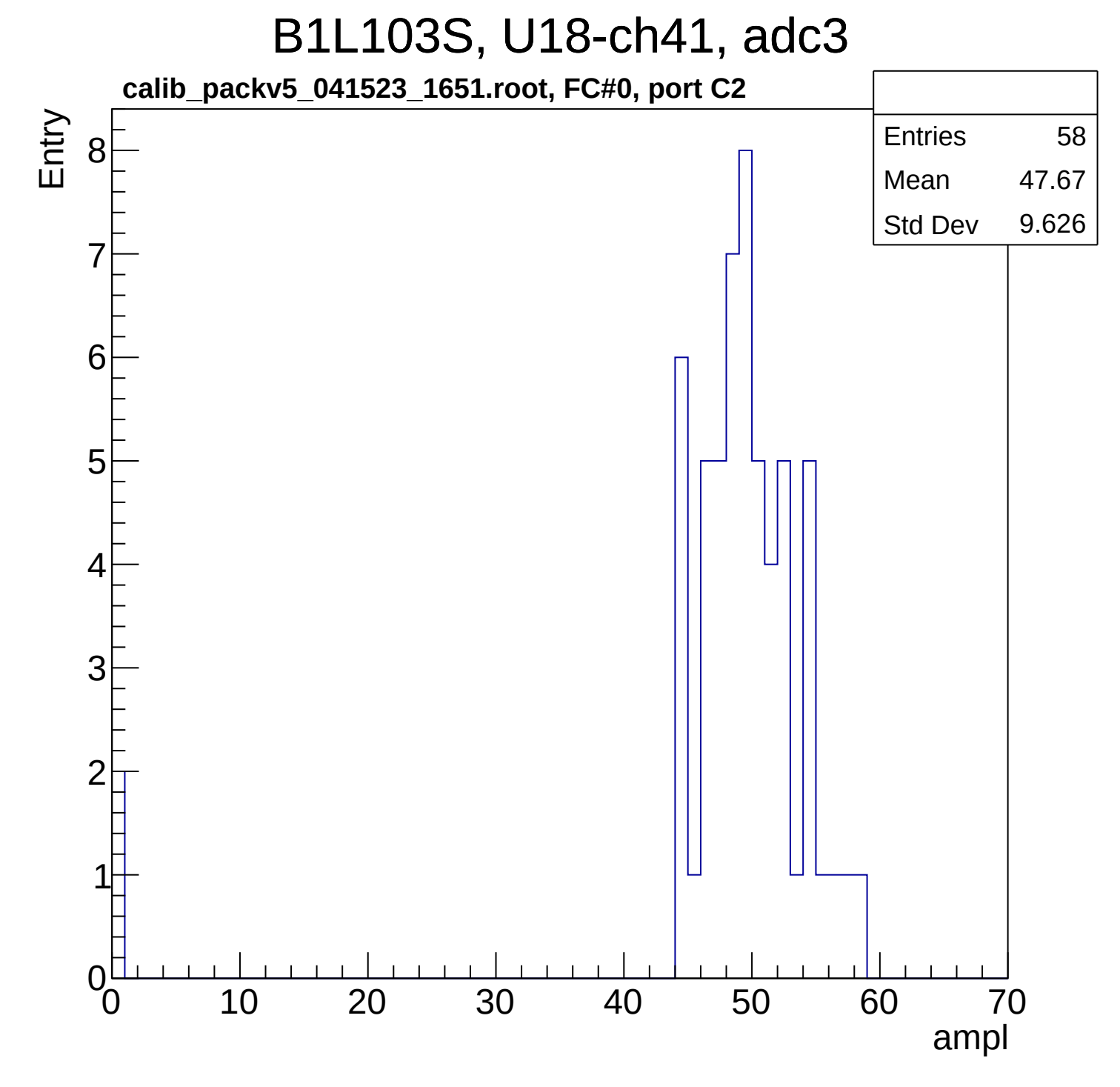
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U18-ch40, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch41, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 26.56
Std Dev 9.265
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch41, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 34.06
Std Dev 7.106
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U18-ch41, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 92
Mean 36.96
Std Dev 14.8
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch41, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 47.67
Std Dev 9.626
Entry
ampl
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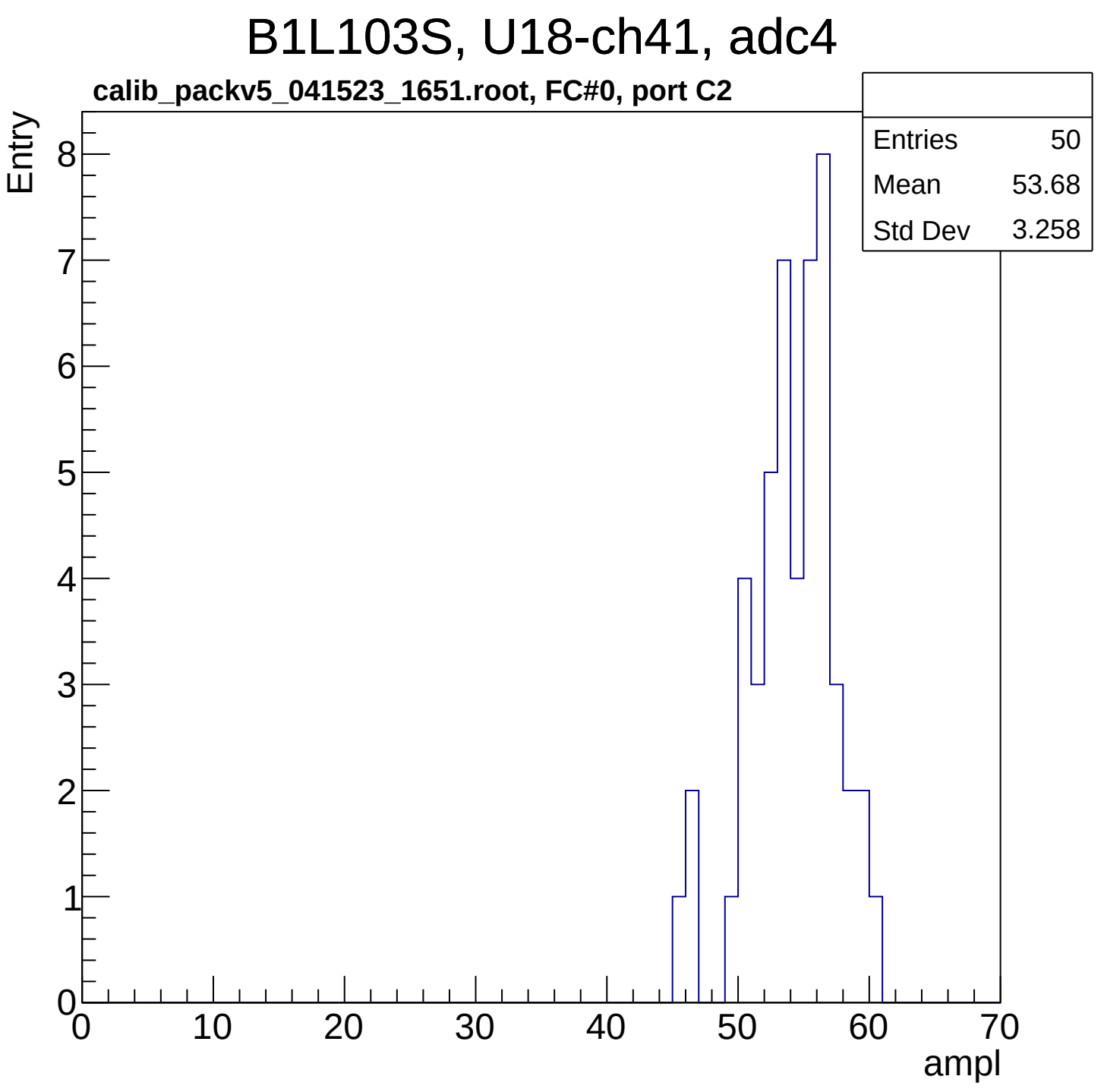
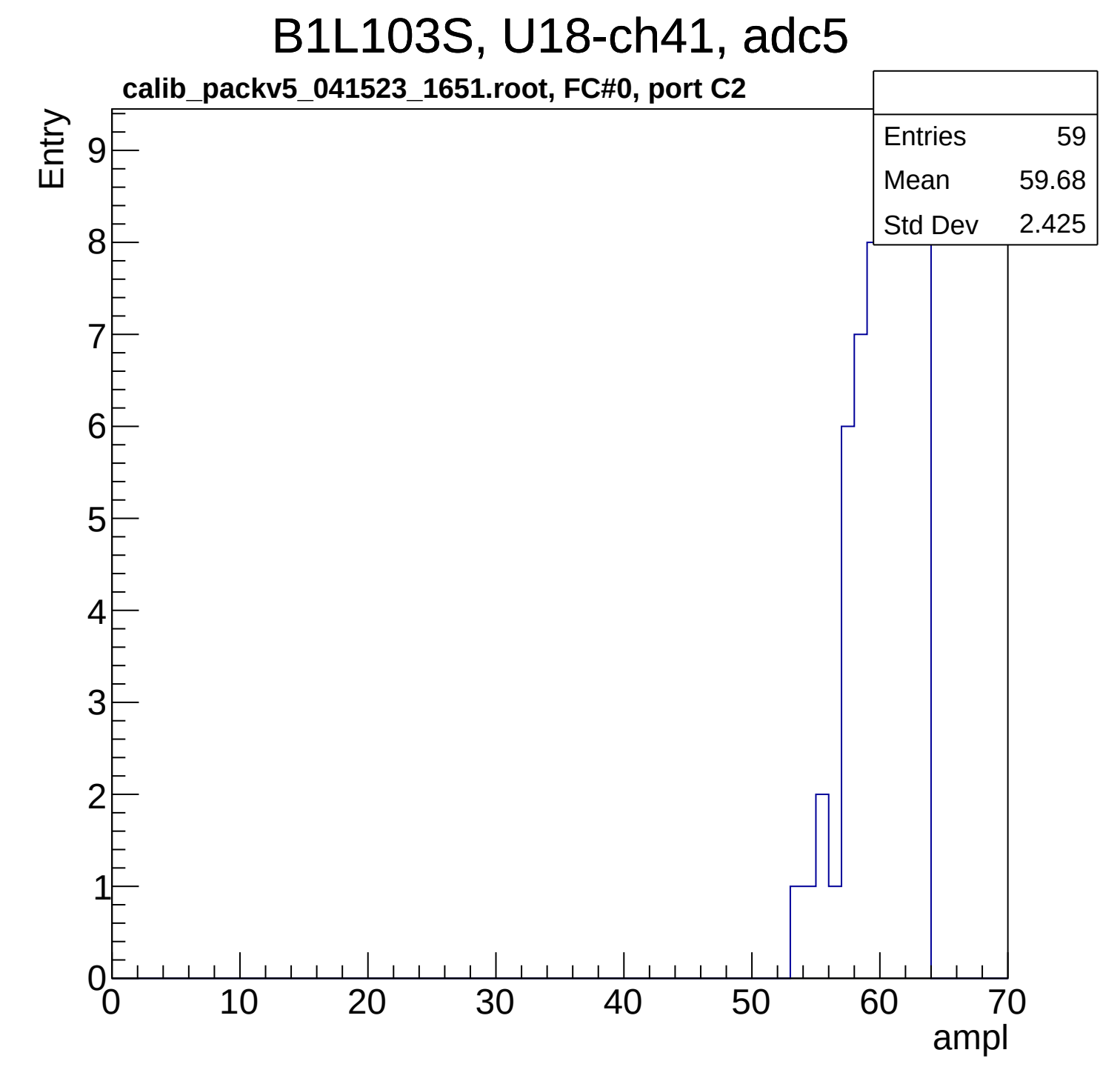
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch41, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 53.68
Std Dev 3.258
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch41, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 59.68
Std Dev 2.425
Entry
ampl
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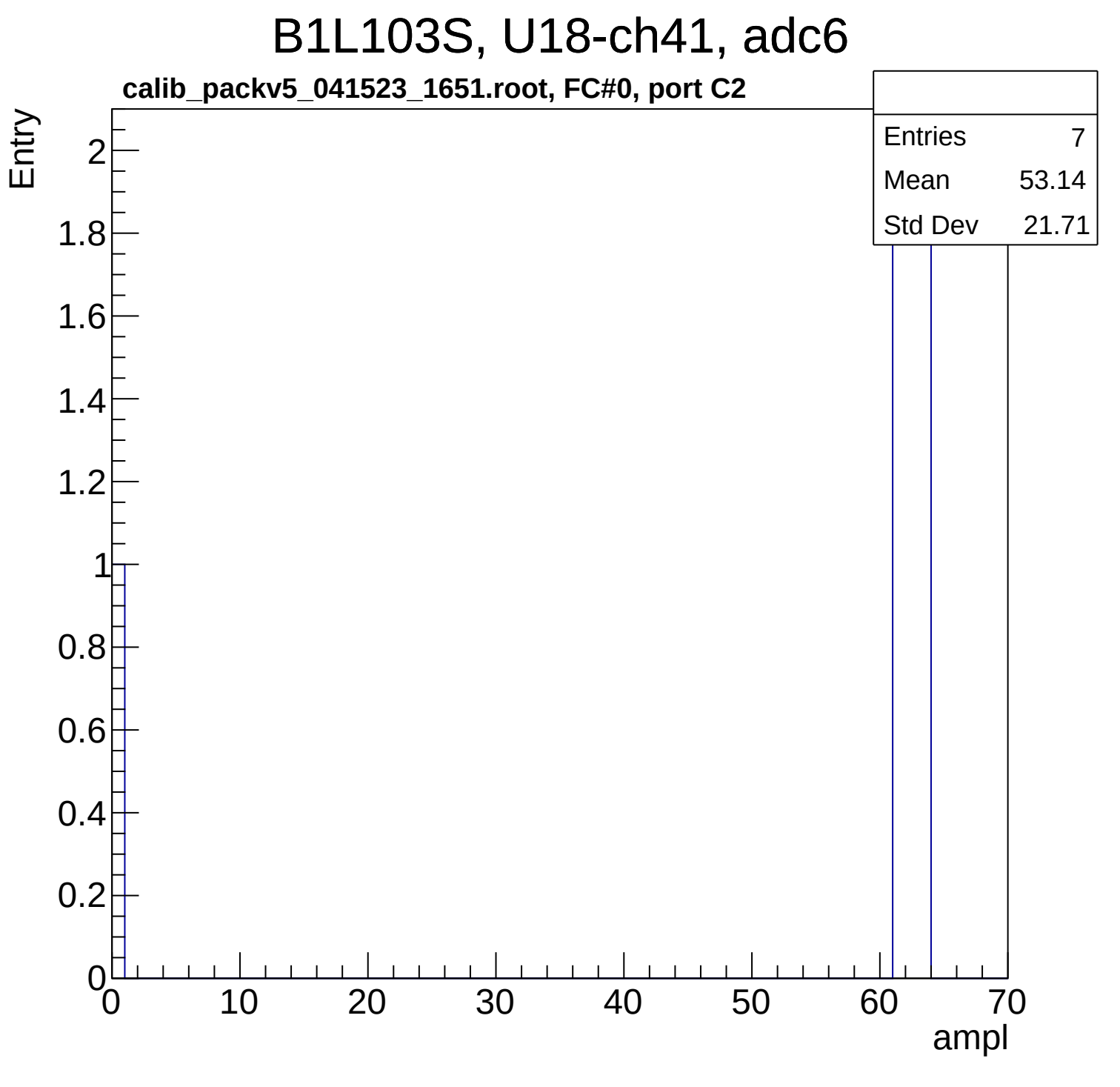
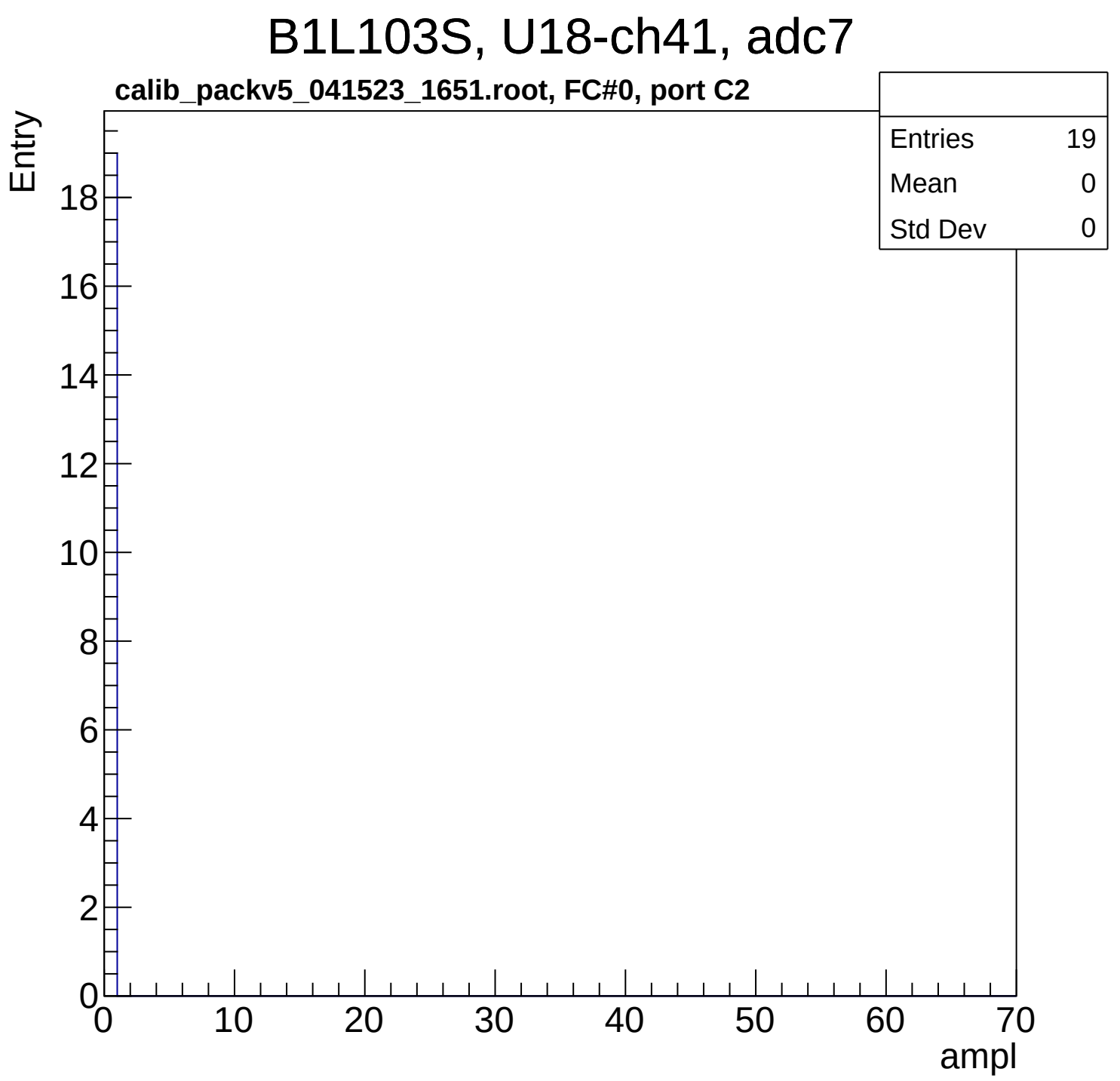
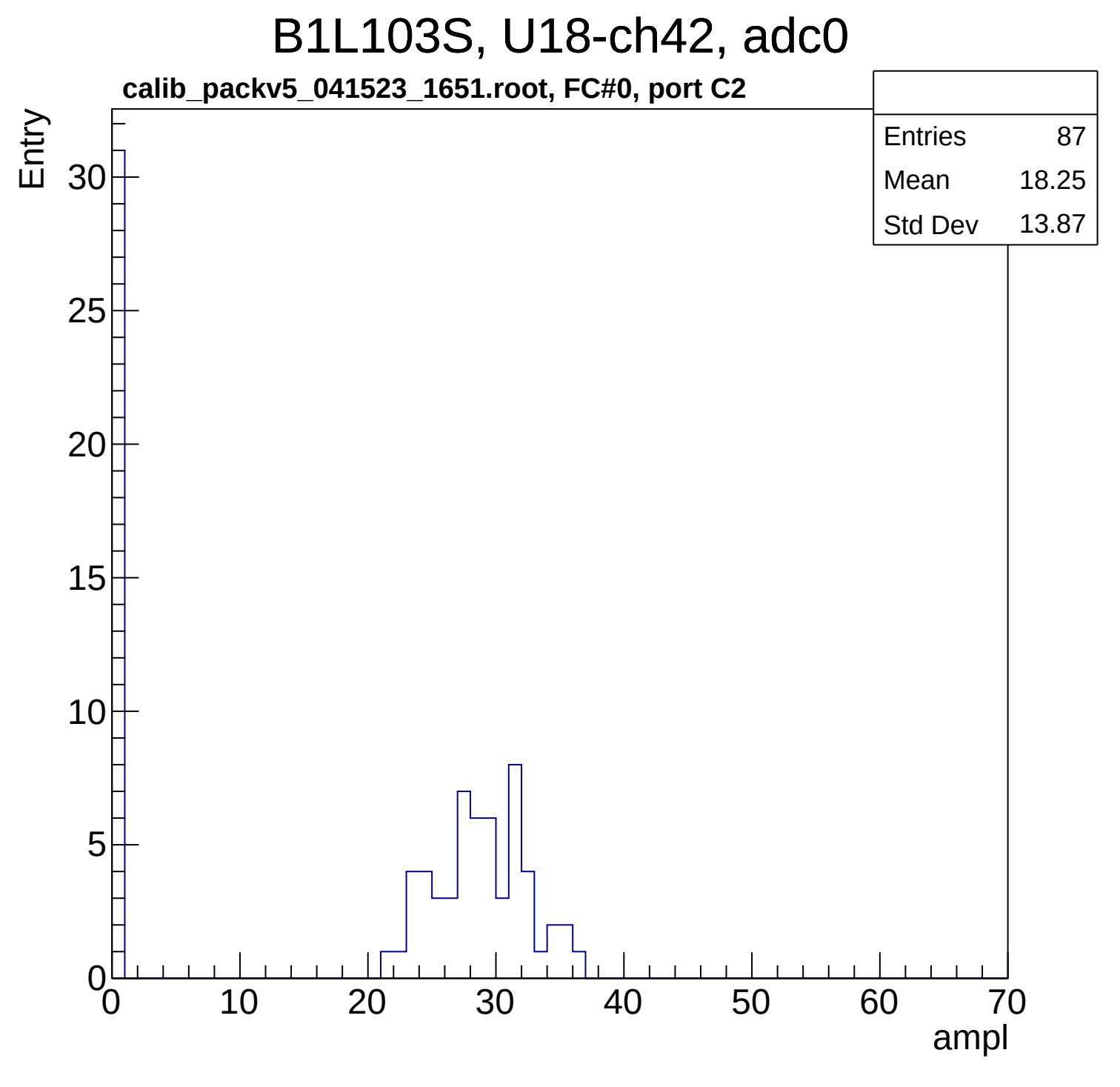
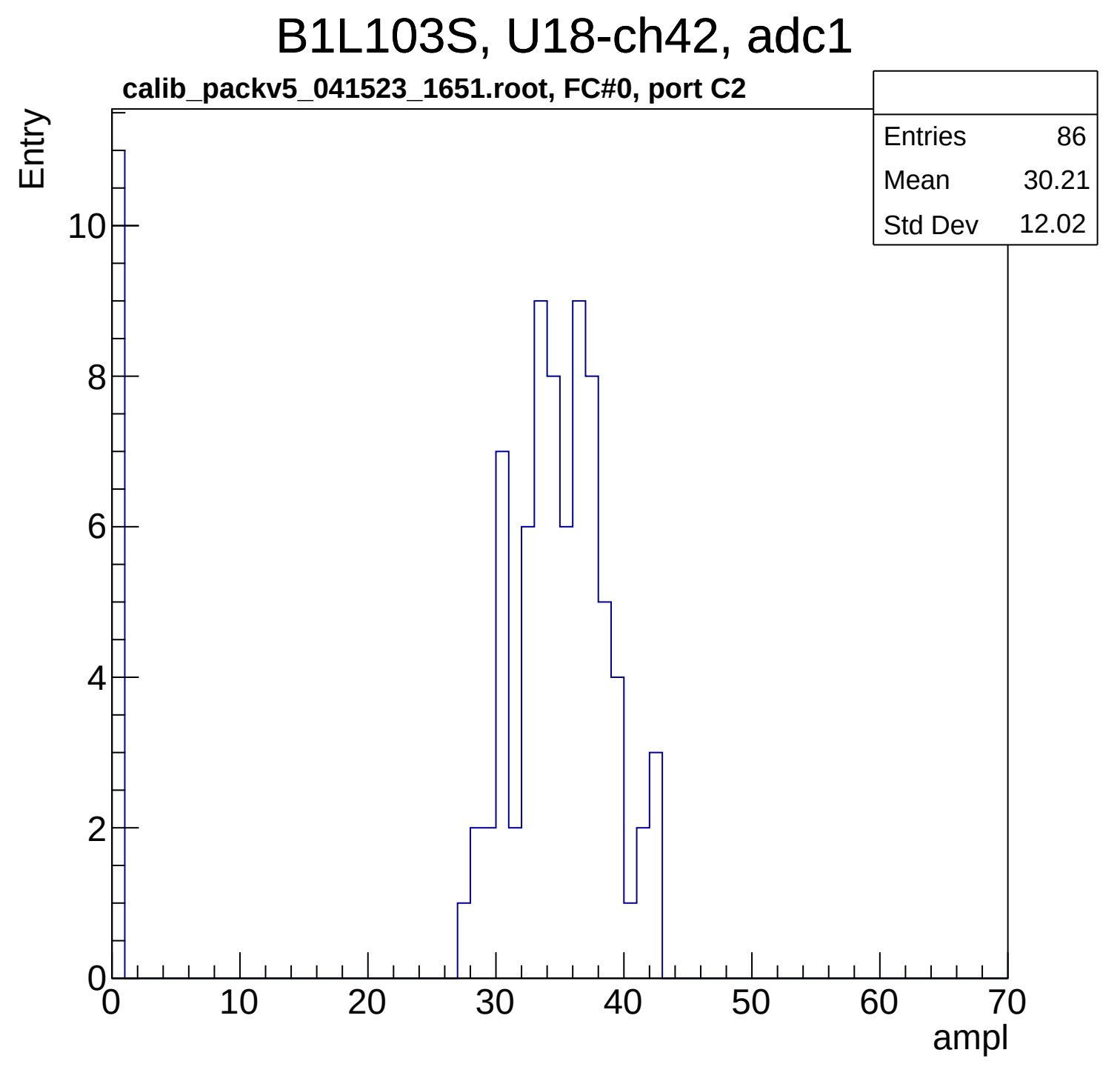
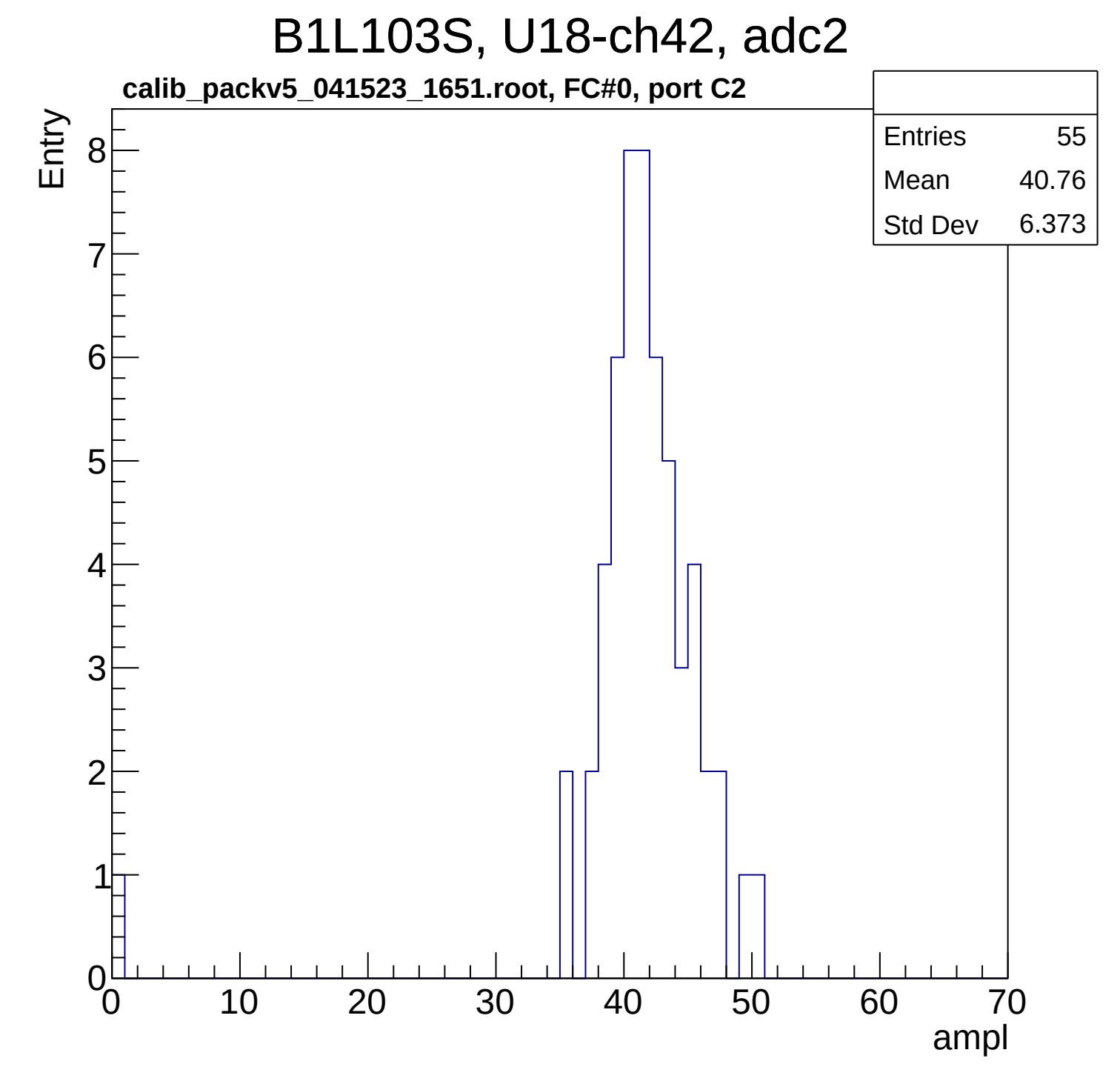
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U18-ch41, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 53.14
Std Dev 21.71
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U18-ch41, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch42, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 87
Mean 18.25
Std Dev 13.87
Entry
0
5
10
15
20
25
30
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch42, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 30.21
Std Dev 12.02
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch42, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 40.76
Std Dev 6.373
Entry
ampl
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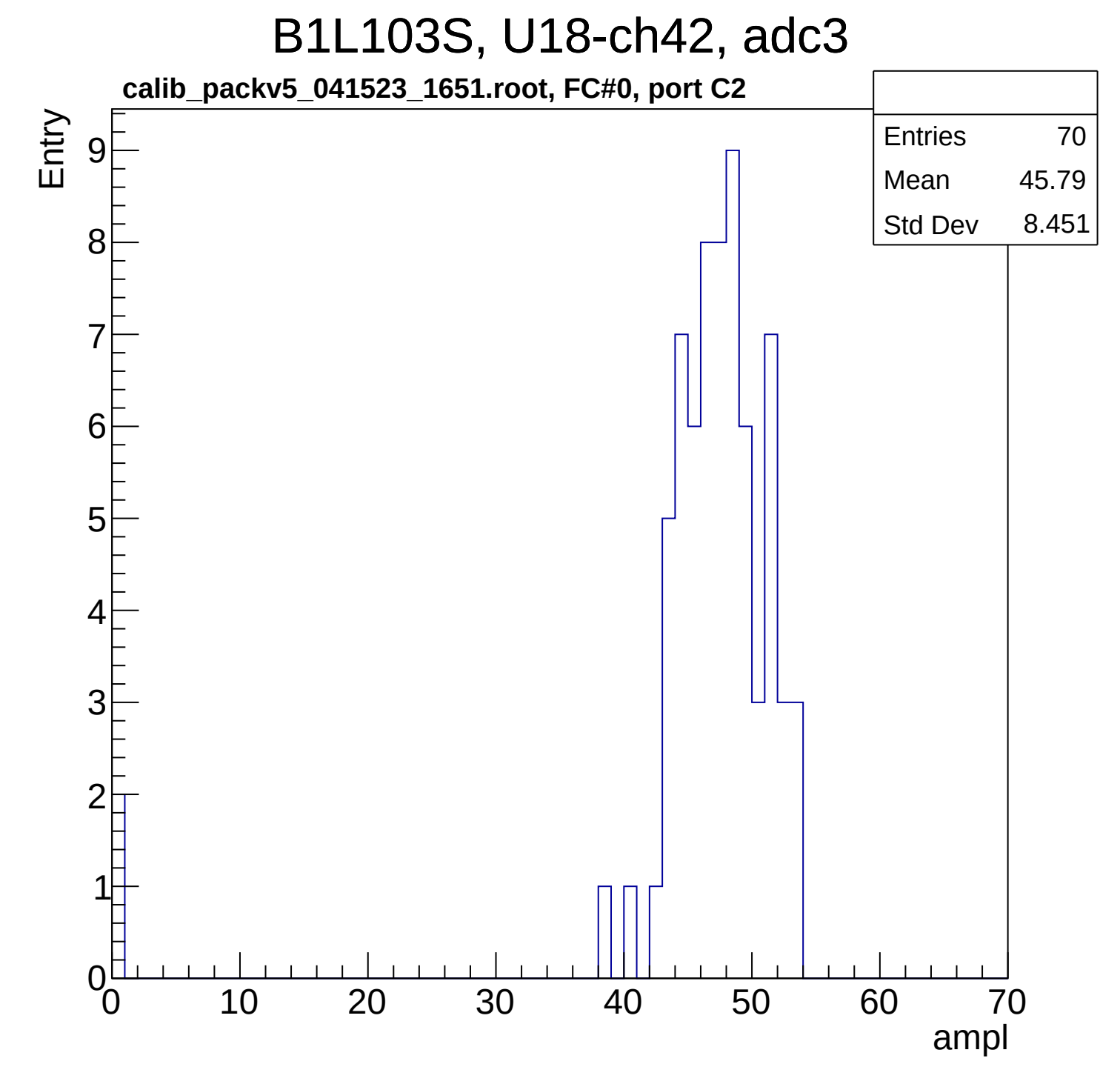
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch42, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 45.79
Std Dev 8.451
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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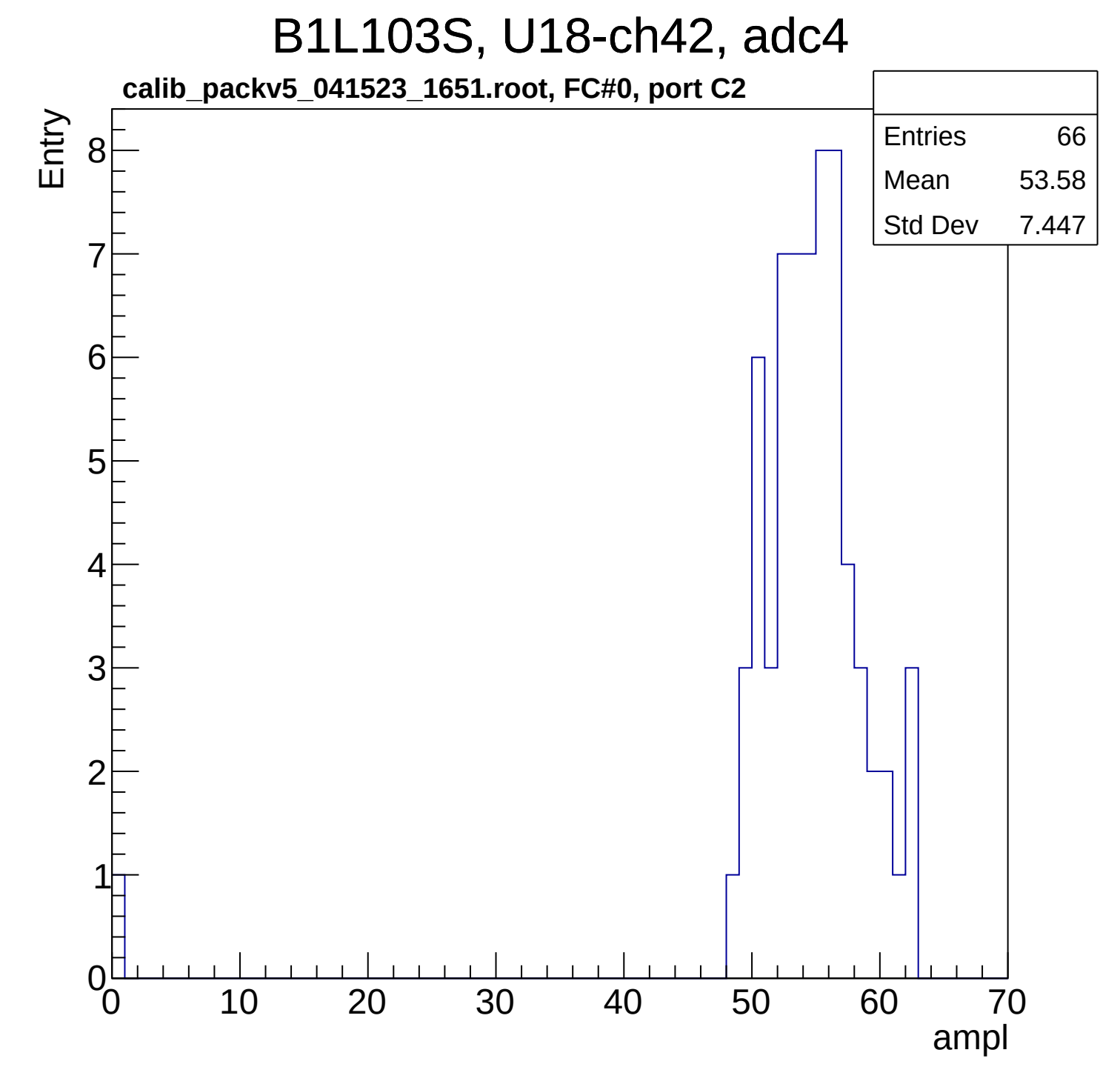
40
50
60
70


B1L103S, U18-ch42, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 53.58
Std Dev 7.447
Entry
ampl
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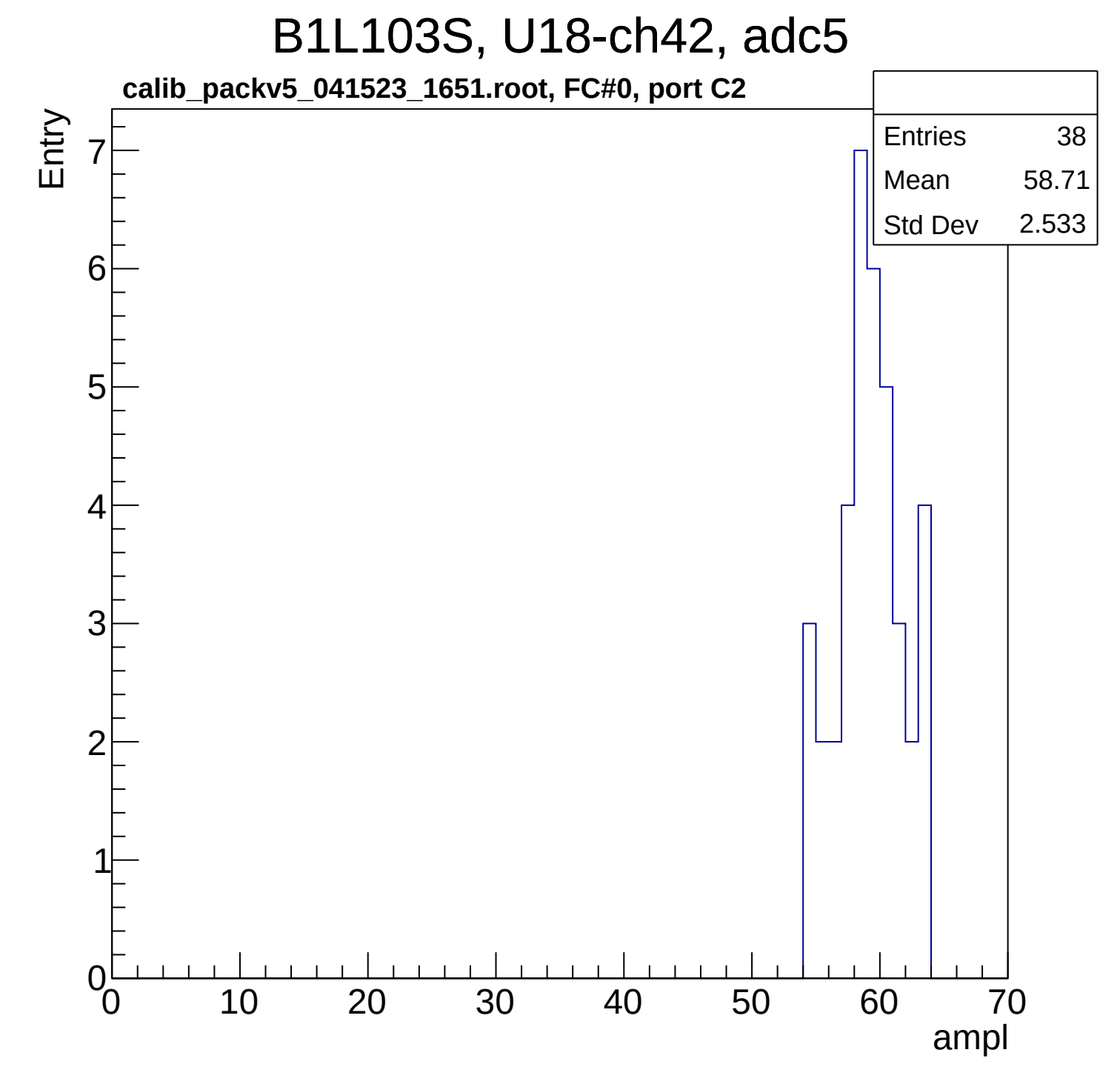
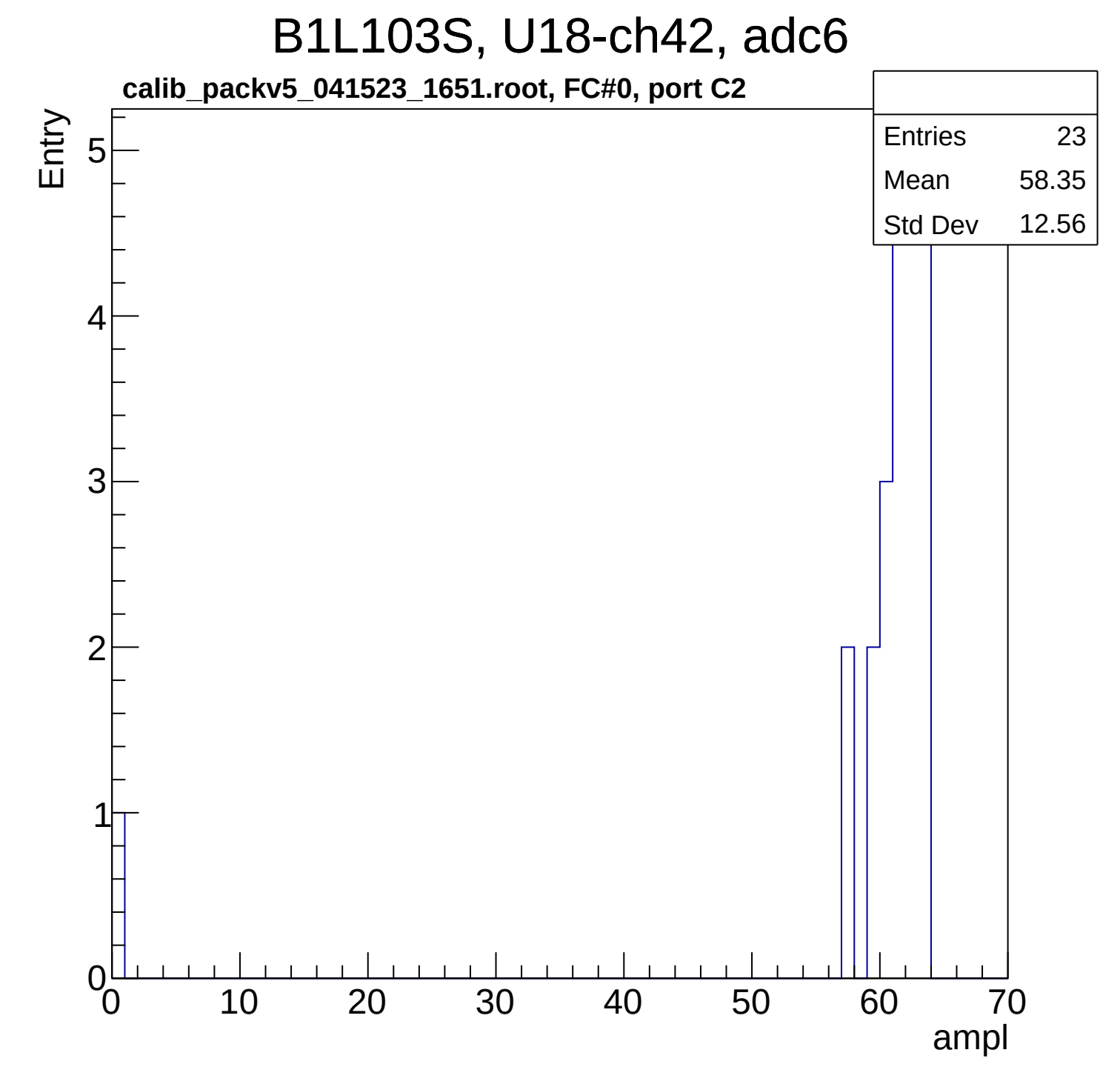
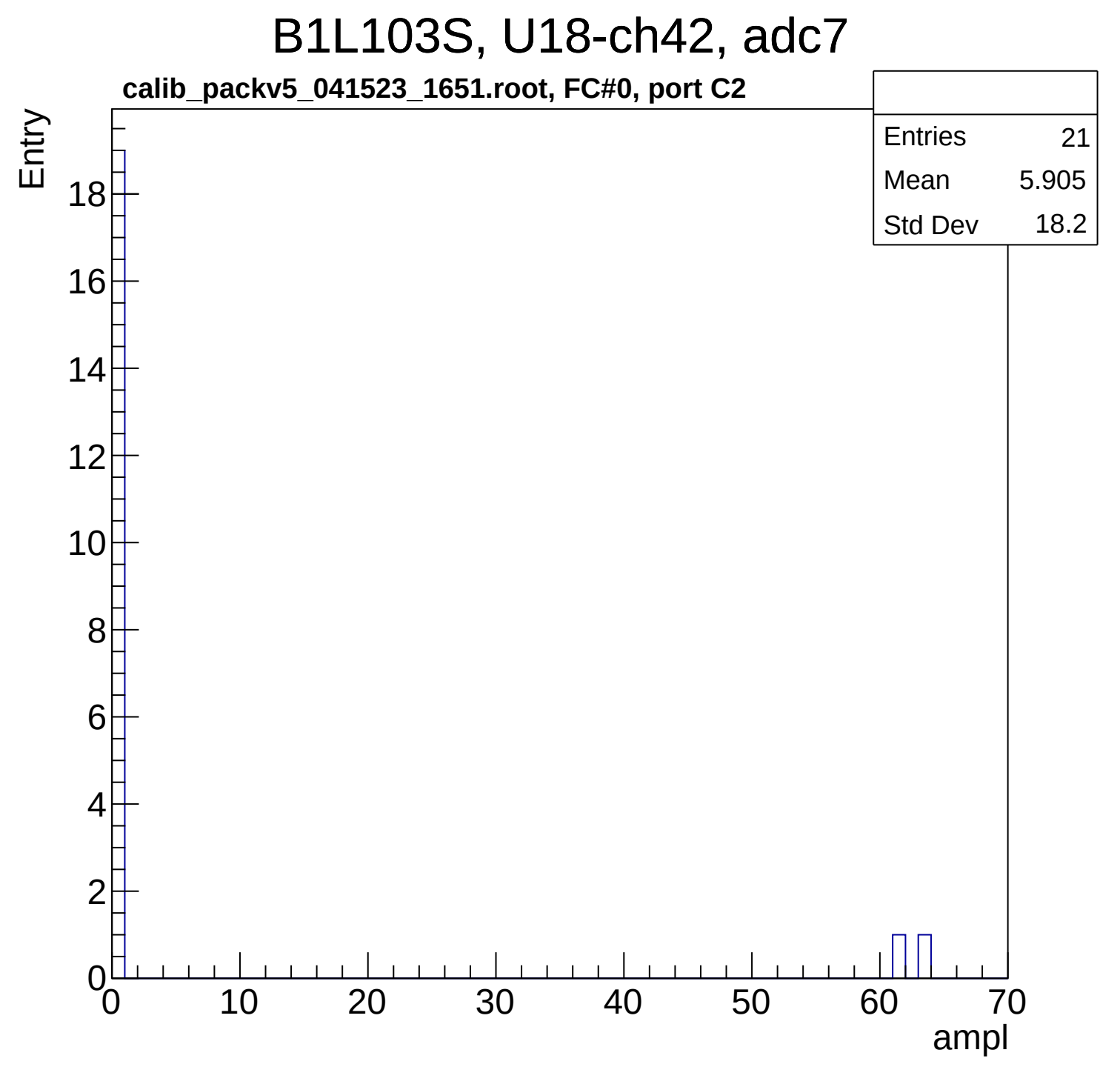
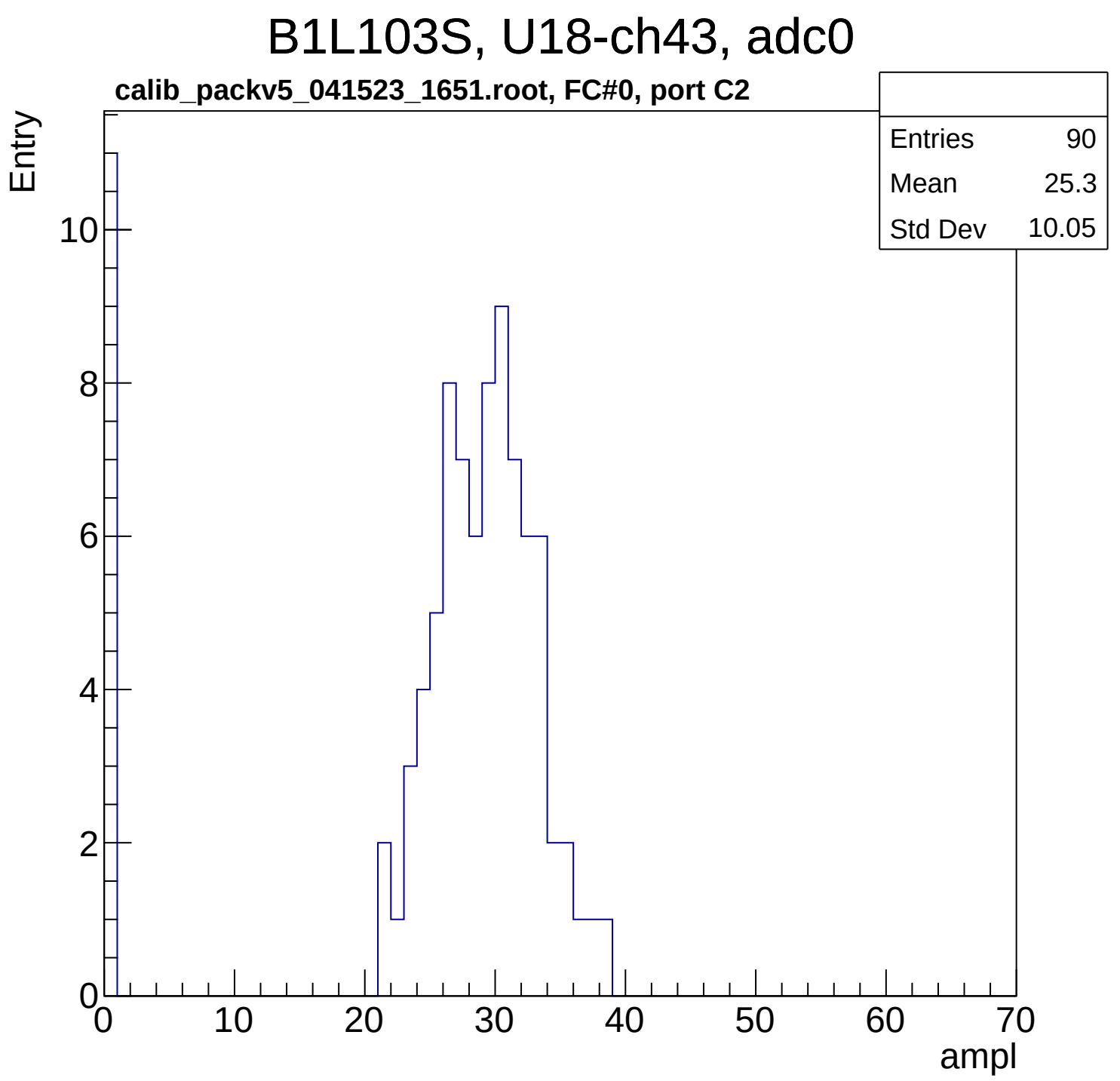
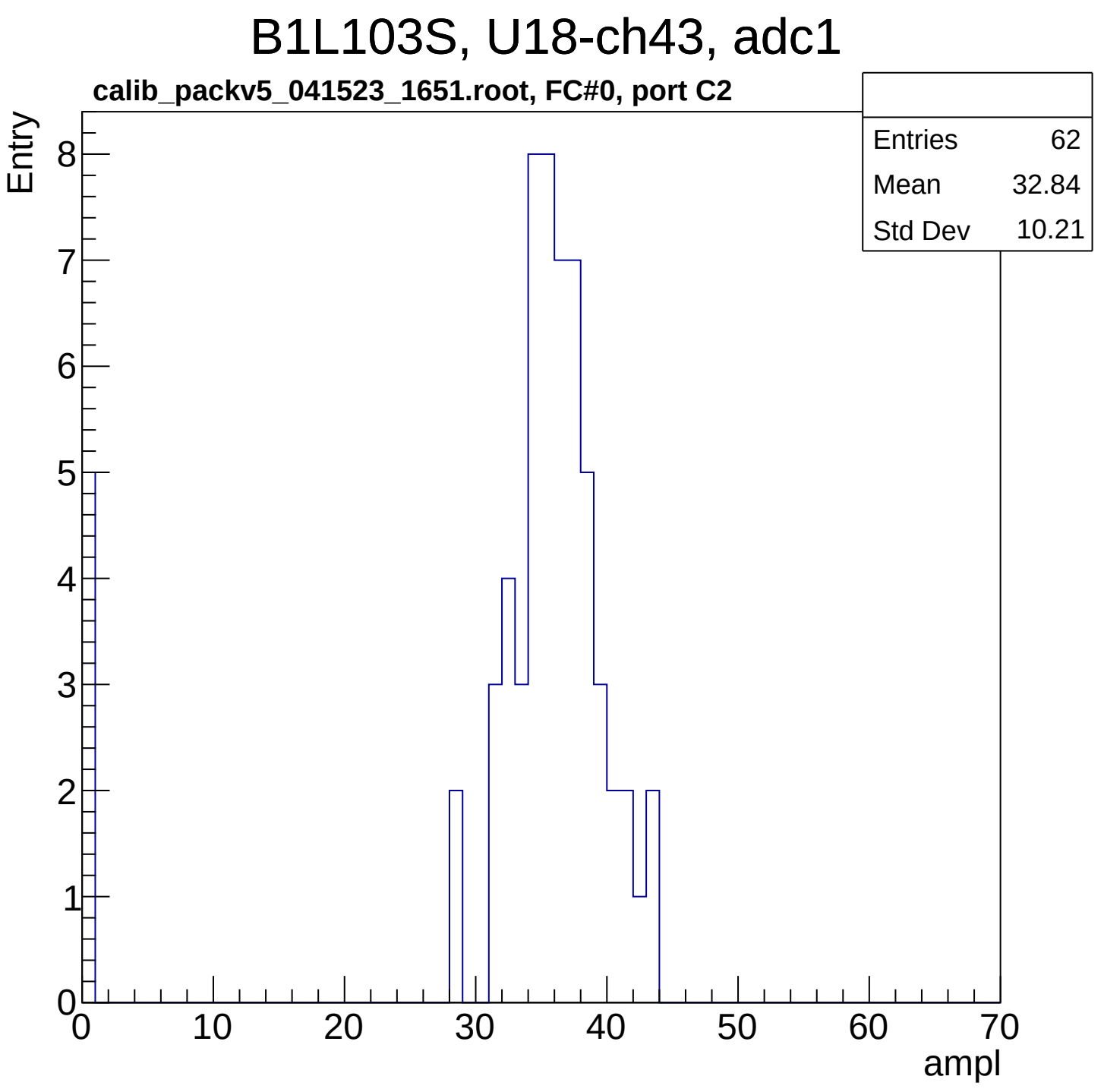
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch42, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 38
Mean 58.71
Std Dev 2.533
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U18-ch42, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 23
Mean 58.35
Std Dev 12.56
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U18-ch42, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 5.905
Std Dev 18.2
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch43, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 90
Mean 25.3
Std Dev 10.05
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch43, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 32.84
Std Dev 10.21
Entry
ampl
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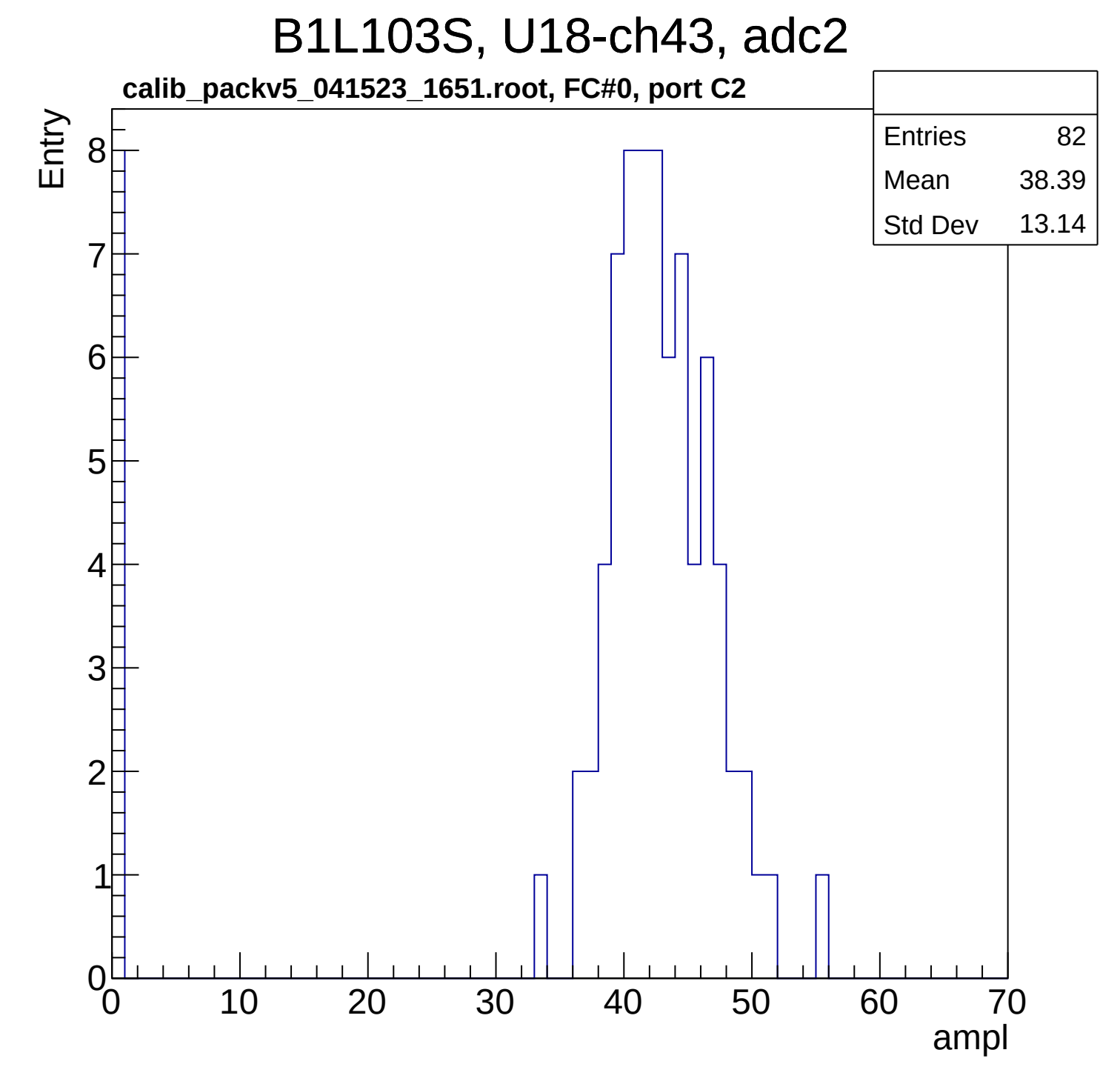
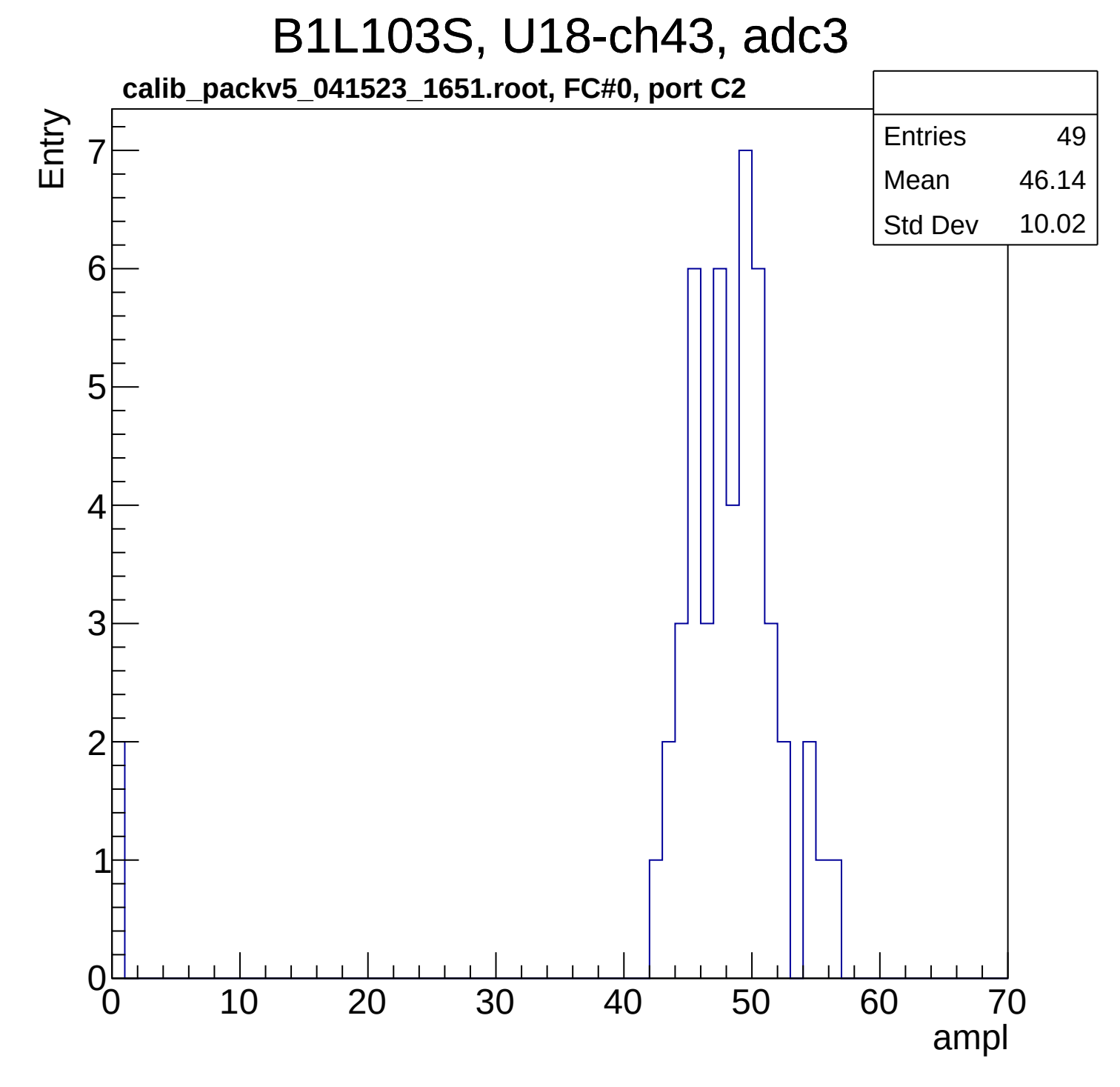
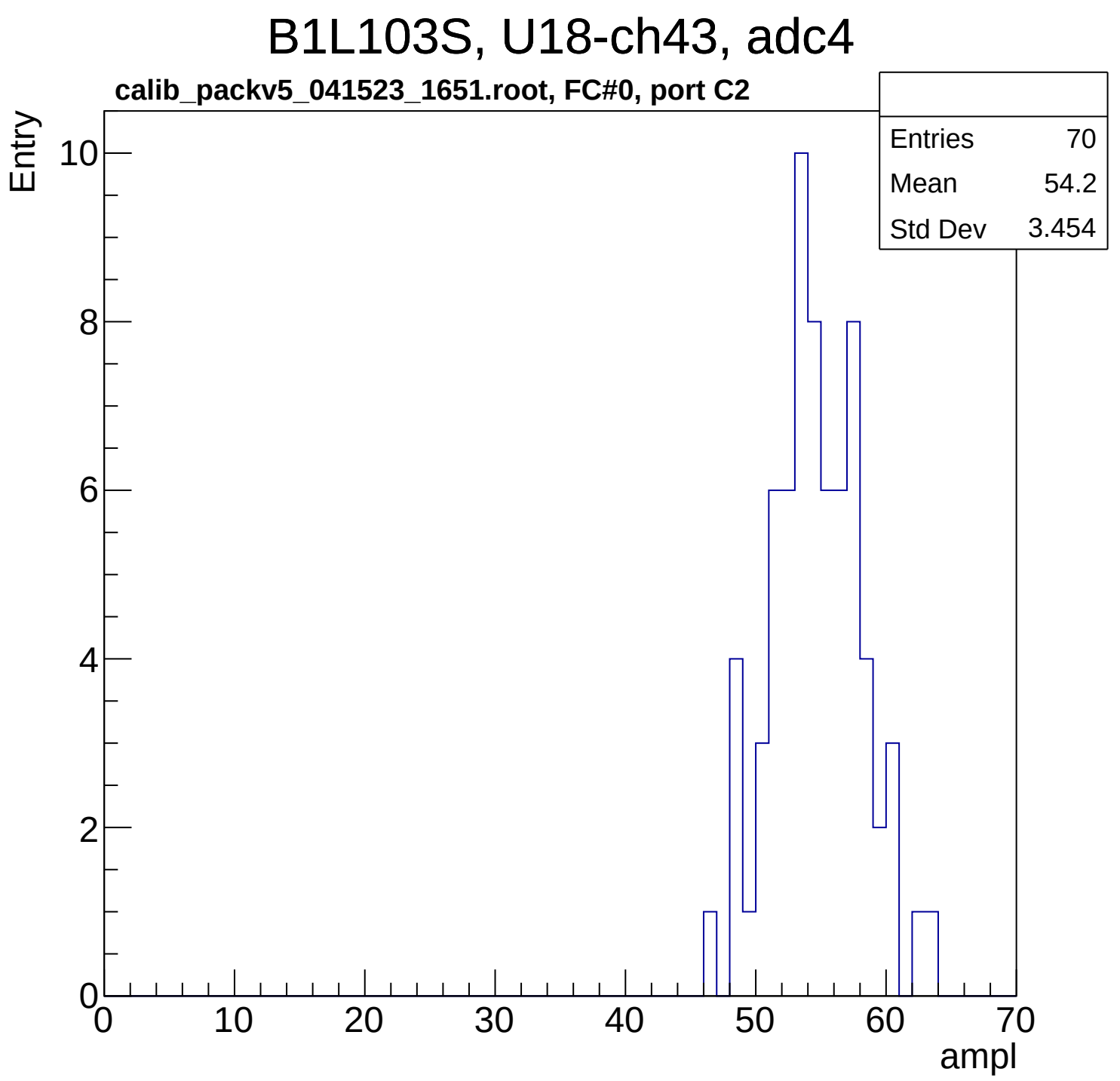
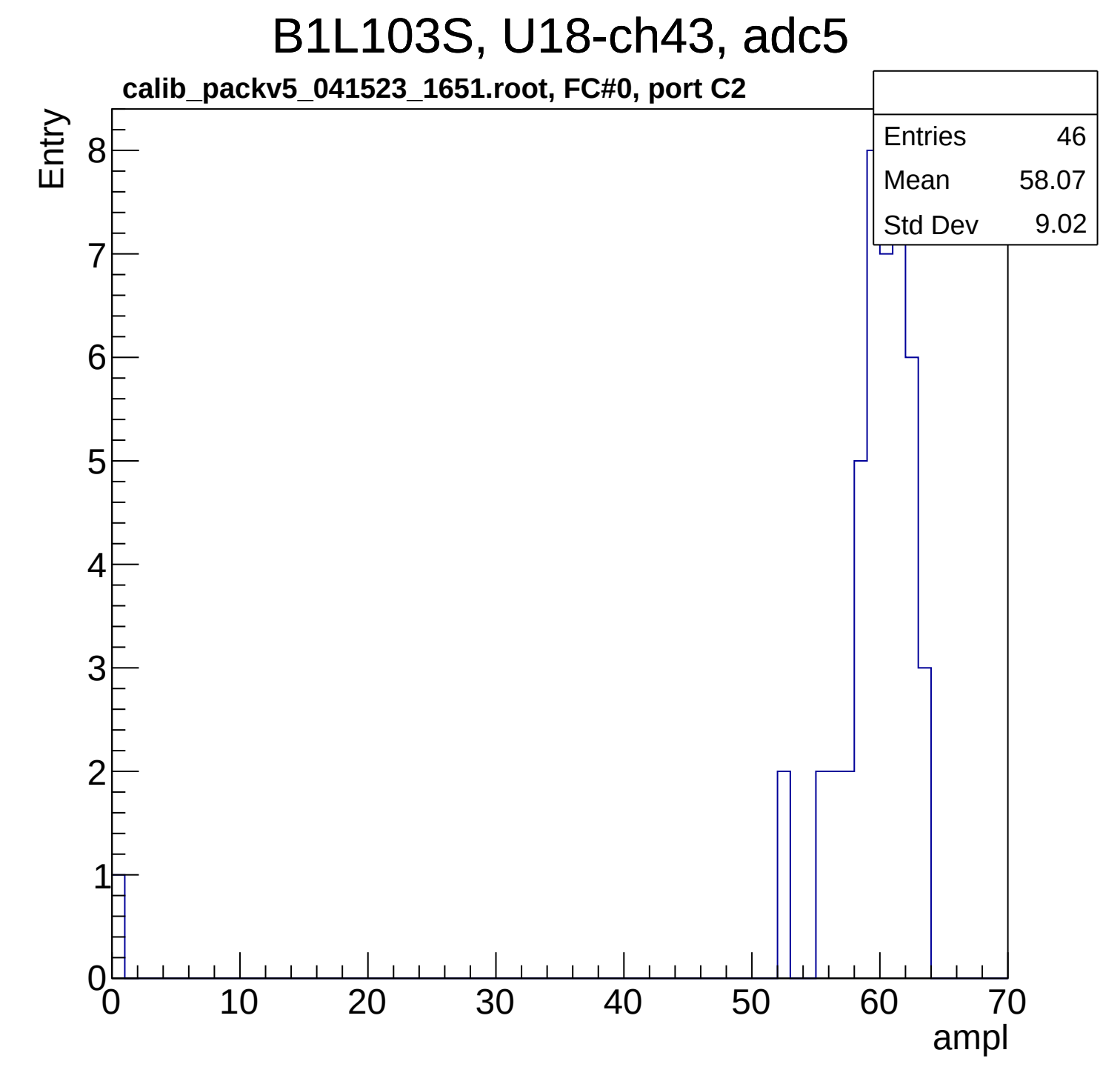
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch43, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 38.39
Std Dev 13.14
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch43, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 46.14
Std Dev 10.02
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U18-ch43, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 54.2
Std Dev 3.454
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch43, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 58.07
Std Dev 9.02
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
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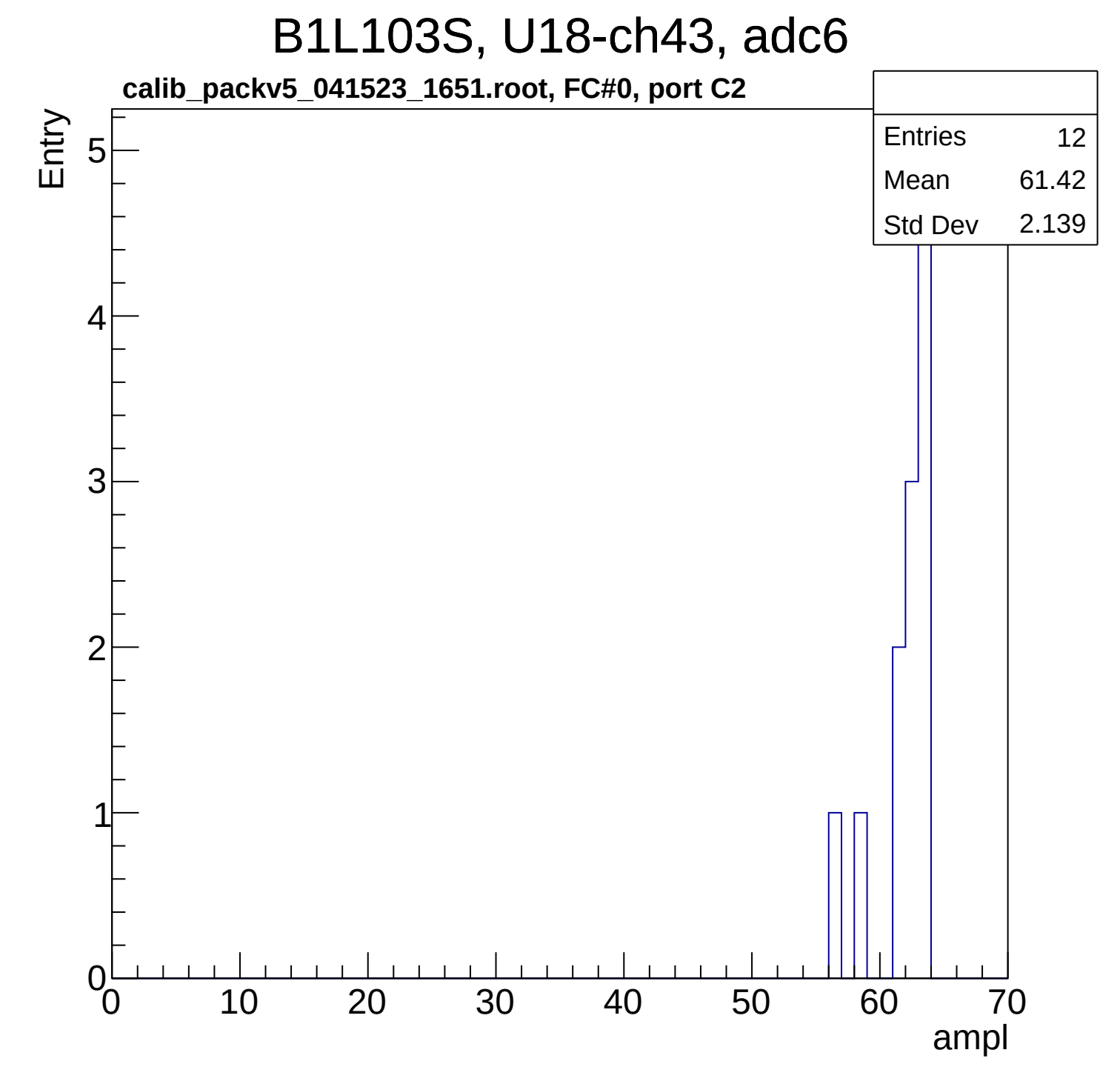
30
40
50
60
70


B1L103S, U18-ch43, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 61.42
Std Dev 2.139
Entry
ampl
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1
2
3
4
5
0
10
20
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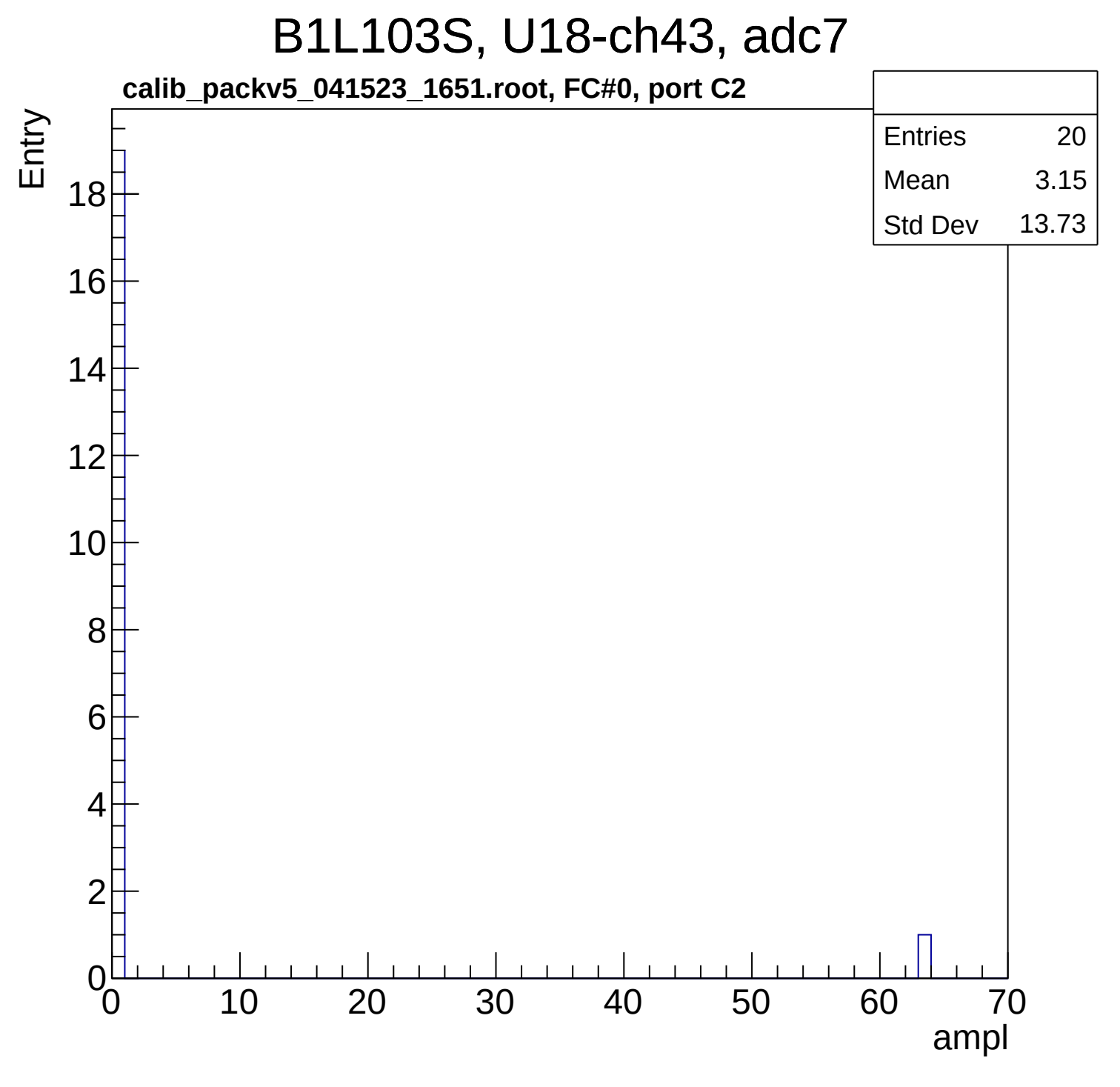
40
50
60
70


B1L103S, U18-ch43, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
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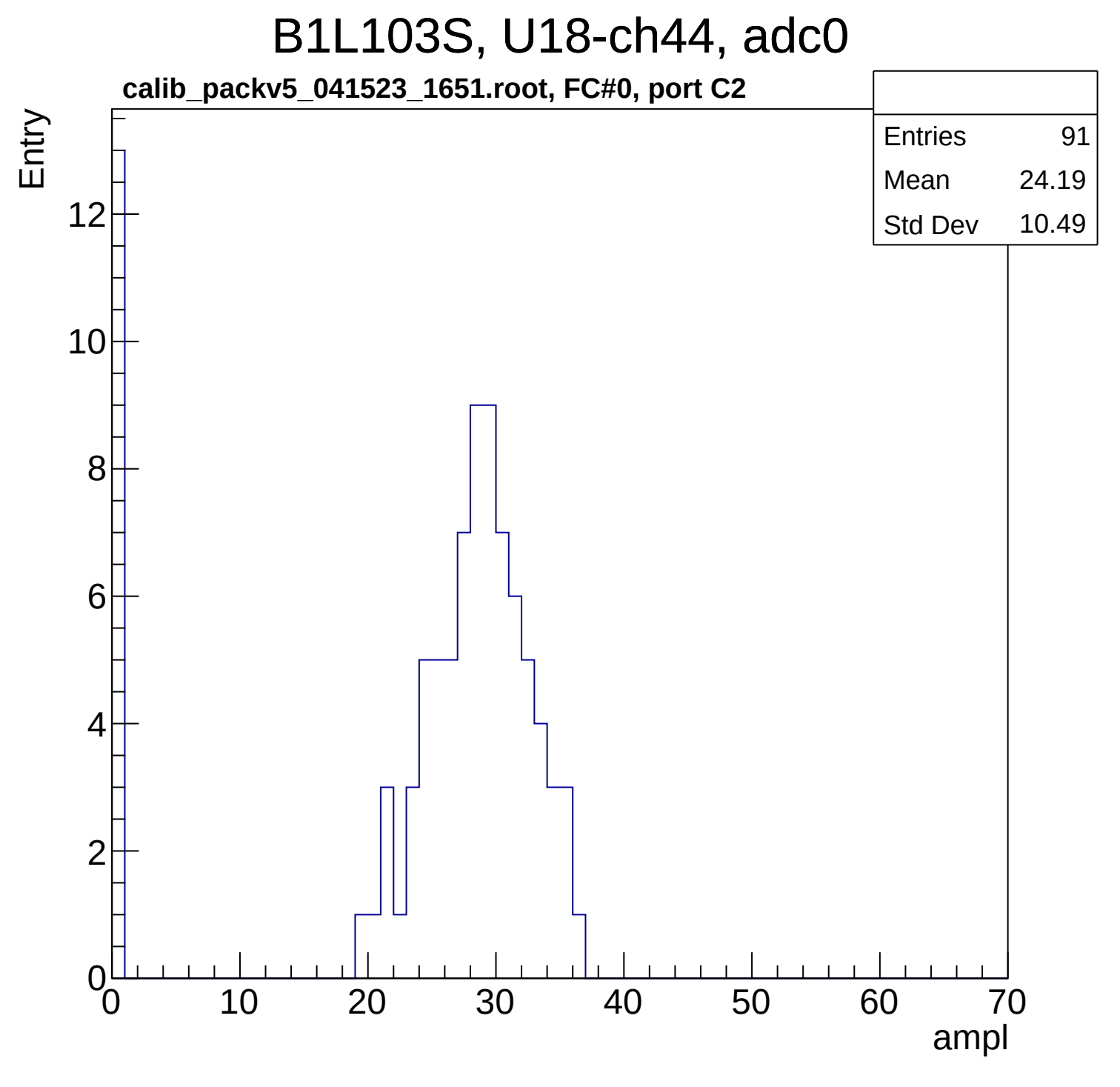
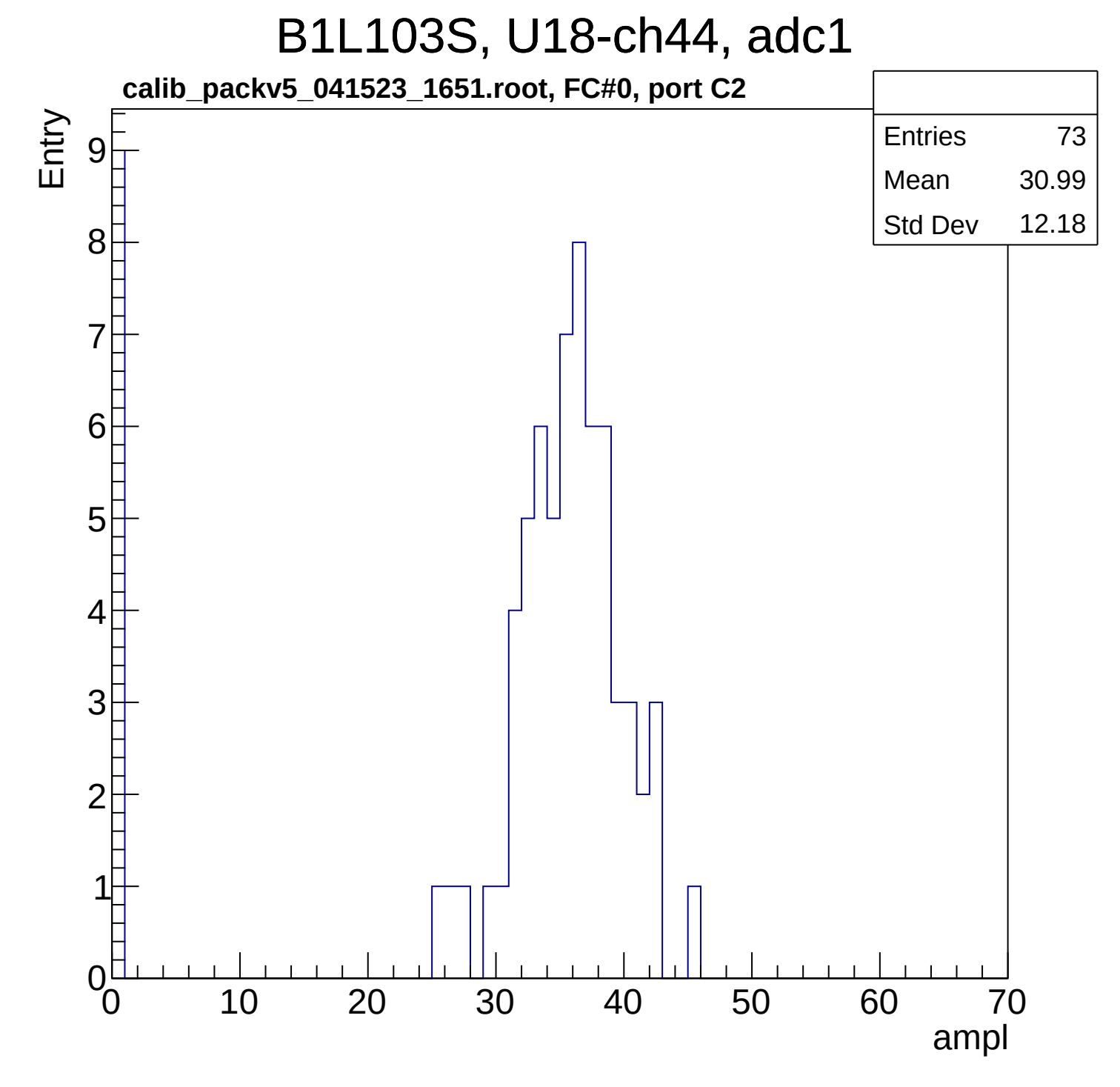
60
70
ampl


B1L103S, U18-ch44, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 91
Mean 24.19
Std Dev 10.49
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch44, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 30.99
Std Dev 12.18
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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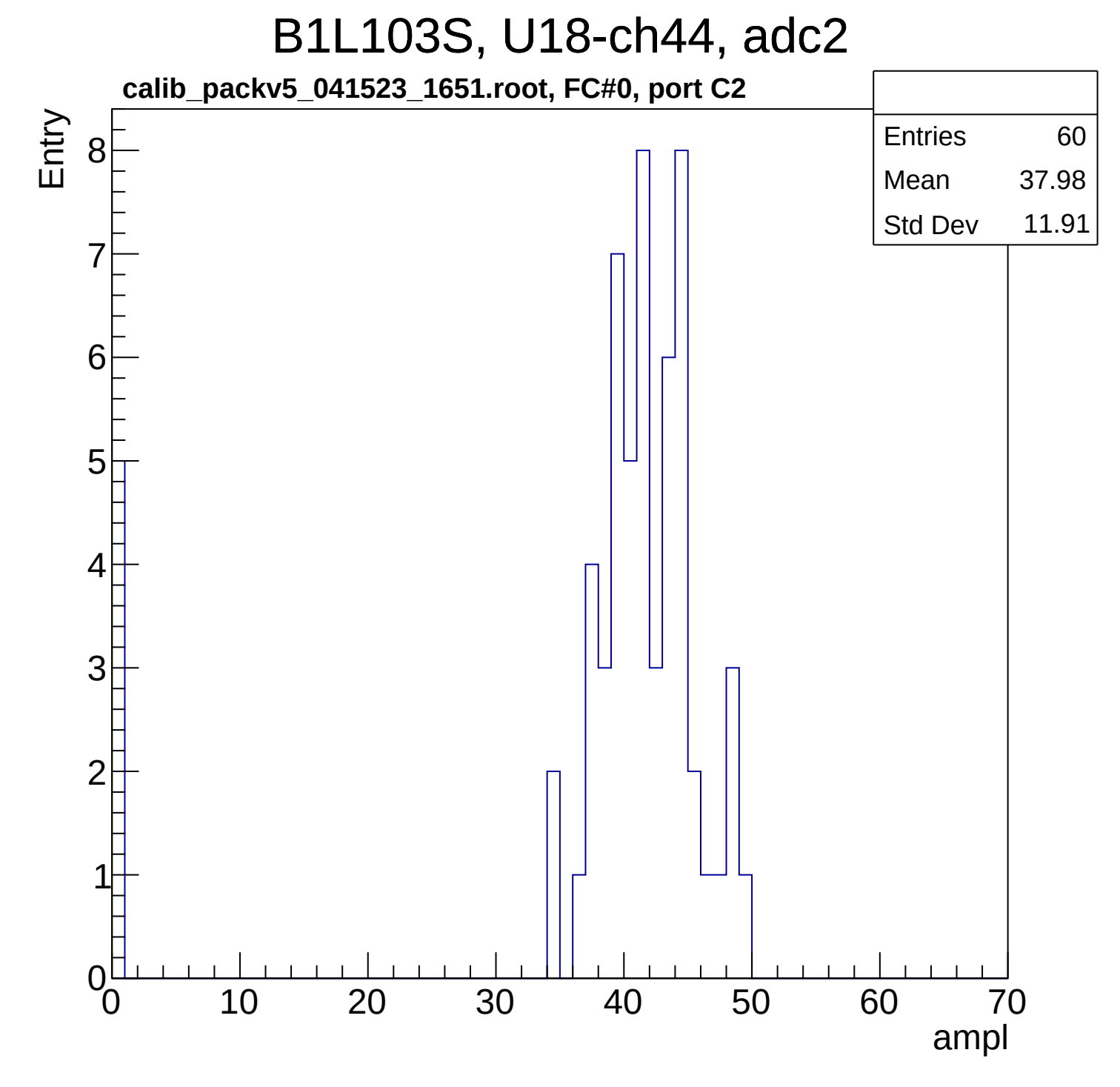
B1L103S, U18-ch44, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 37.98
Std Dev 11.91
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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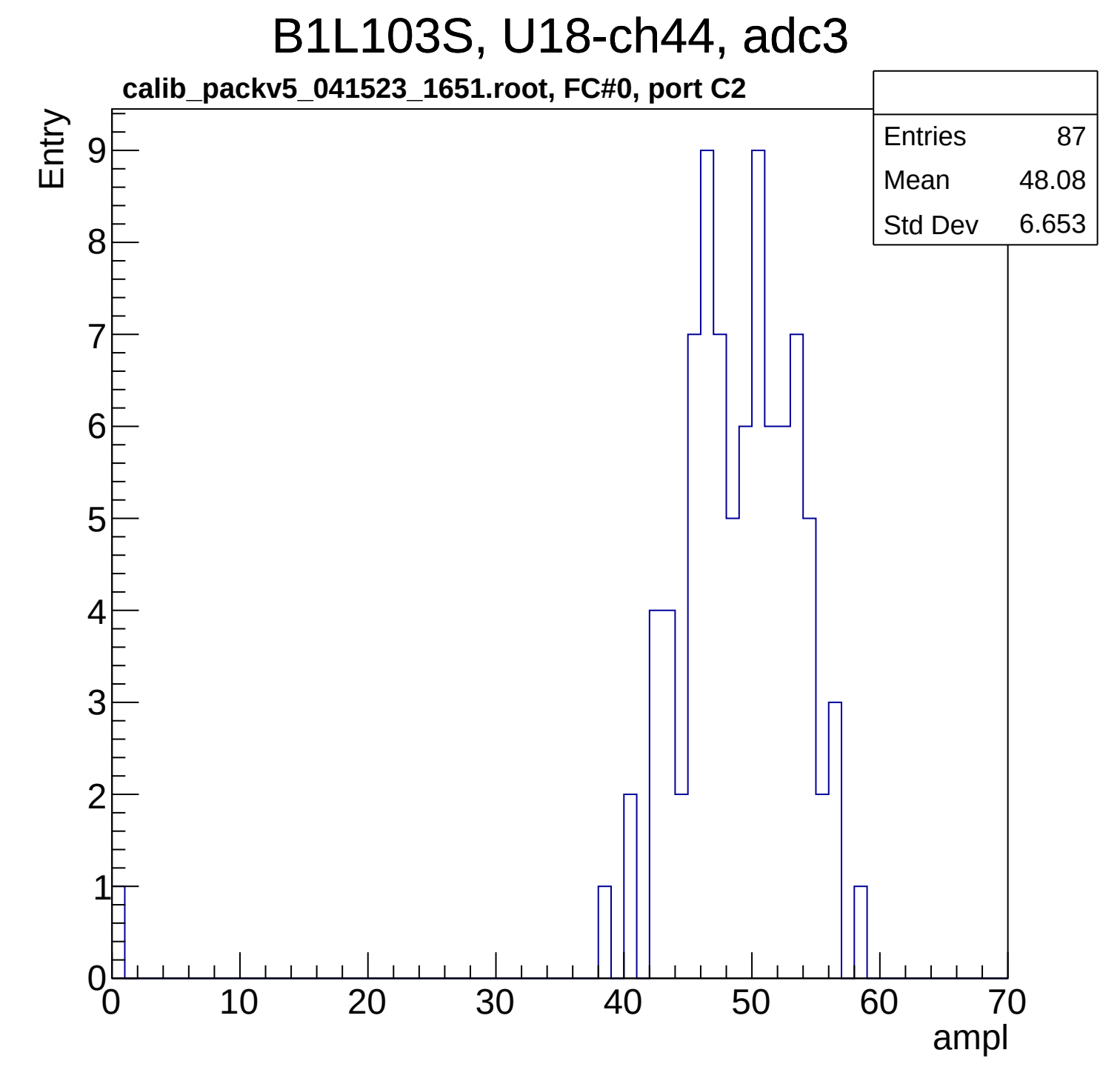
B1L103S, U18-ch44, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 87
Mean 48.08
Std Dev 6.653
Entry
ampl
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3
4
5
6
7
8
9
0
10
20
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40
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60
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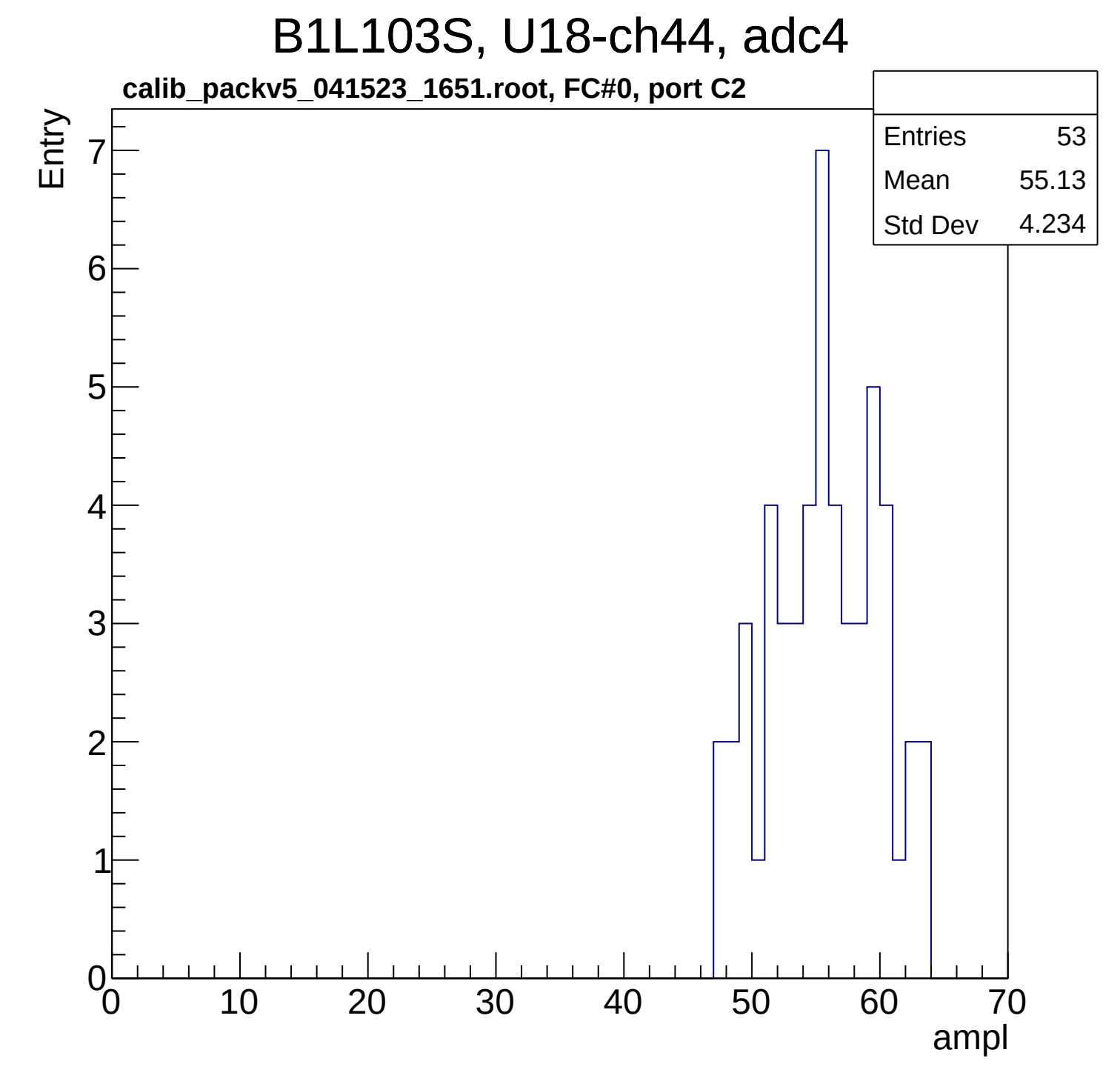
B1L103S, U18-ch44, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 55.13
Std Dev 4.234
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
30
40
50
60
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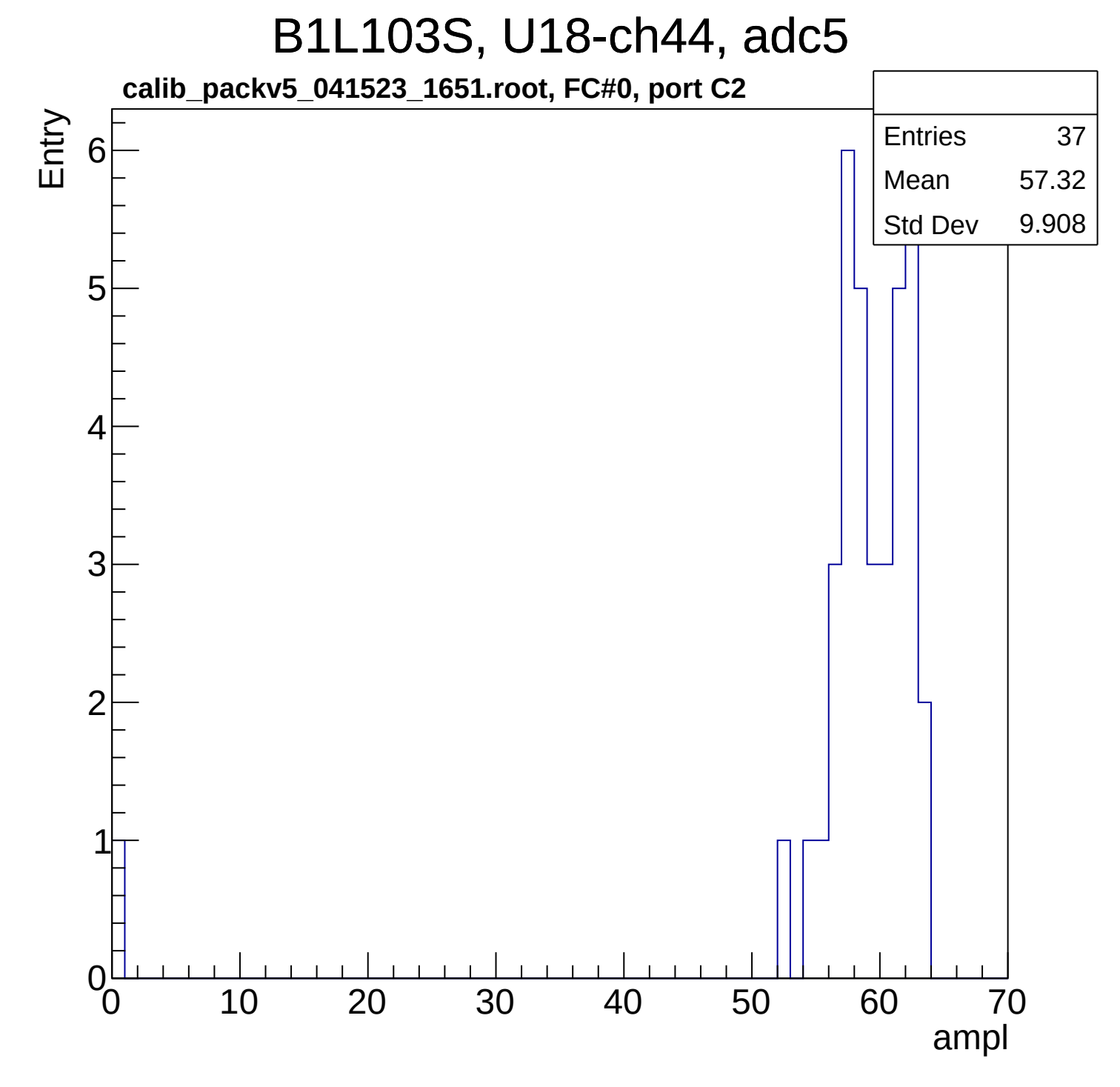
B1L103S, U18-ch44, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 37
Mean 57.32
Std Dev 9.908
Entry
ampl
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1
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3
4
5
6
0
10
20
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40
50
60
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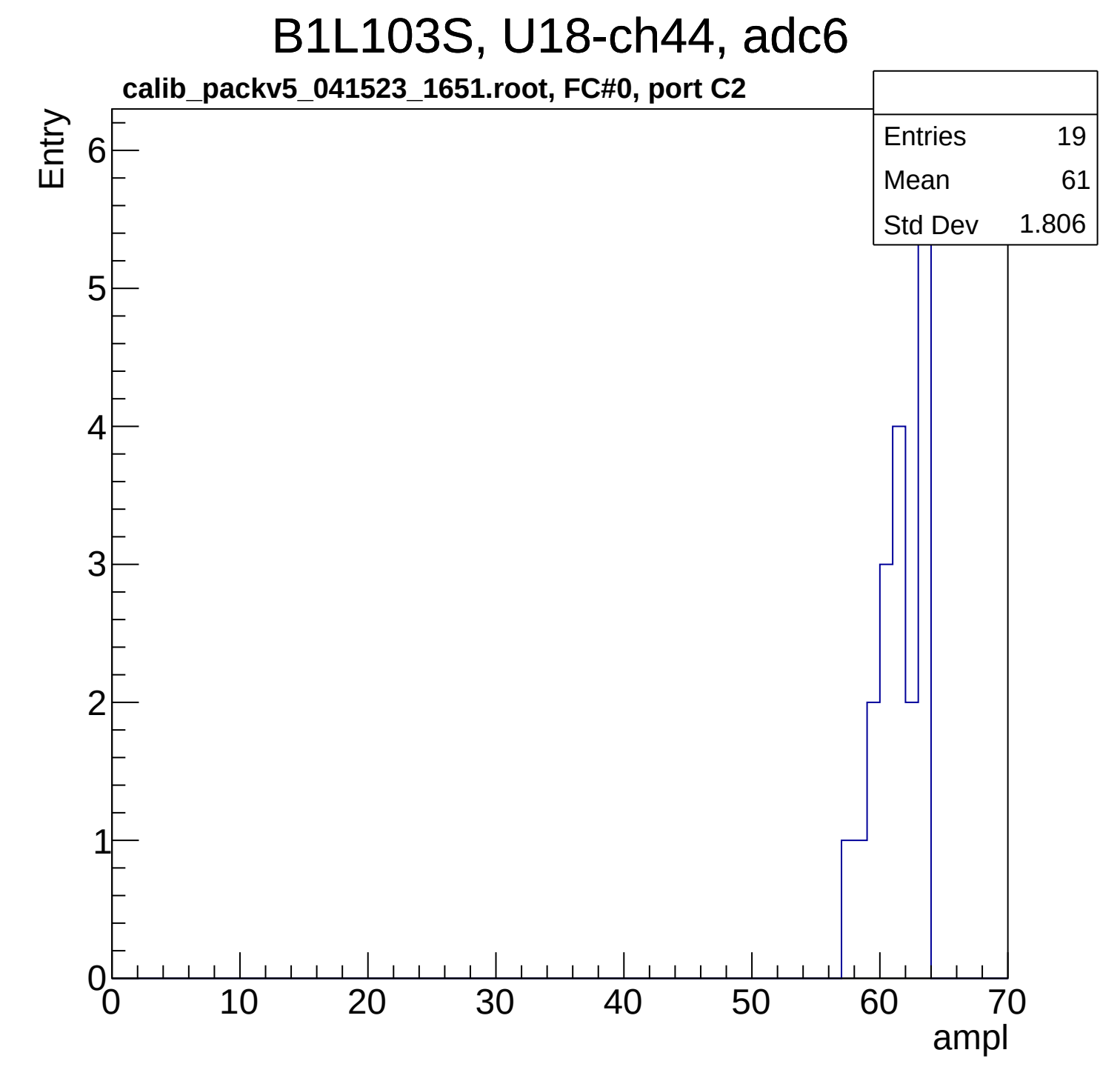
B1L103S, U18-ch44, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 61
Std Dev 1.806
Entry
ampl
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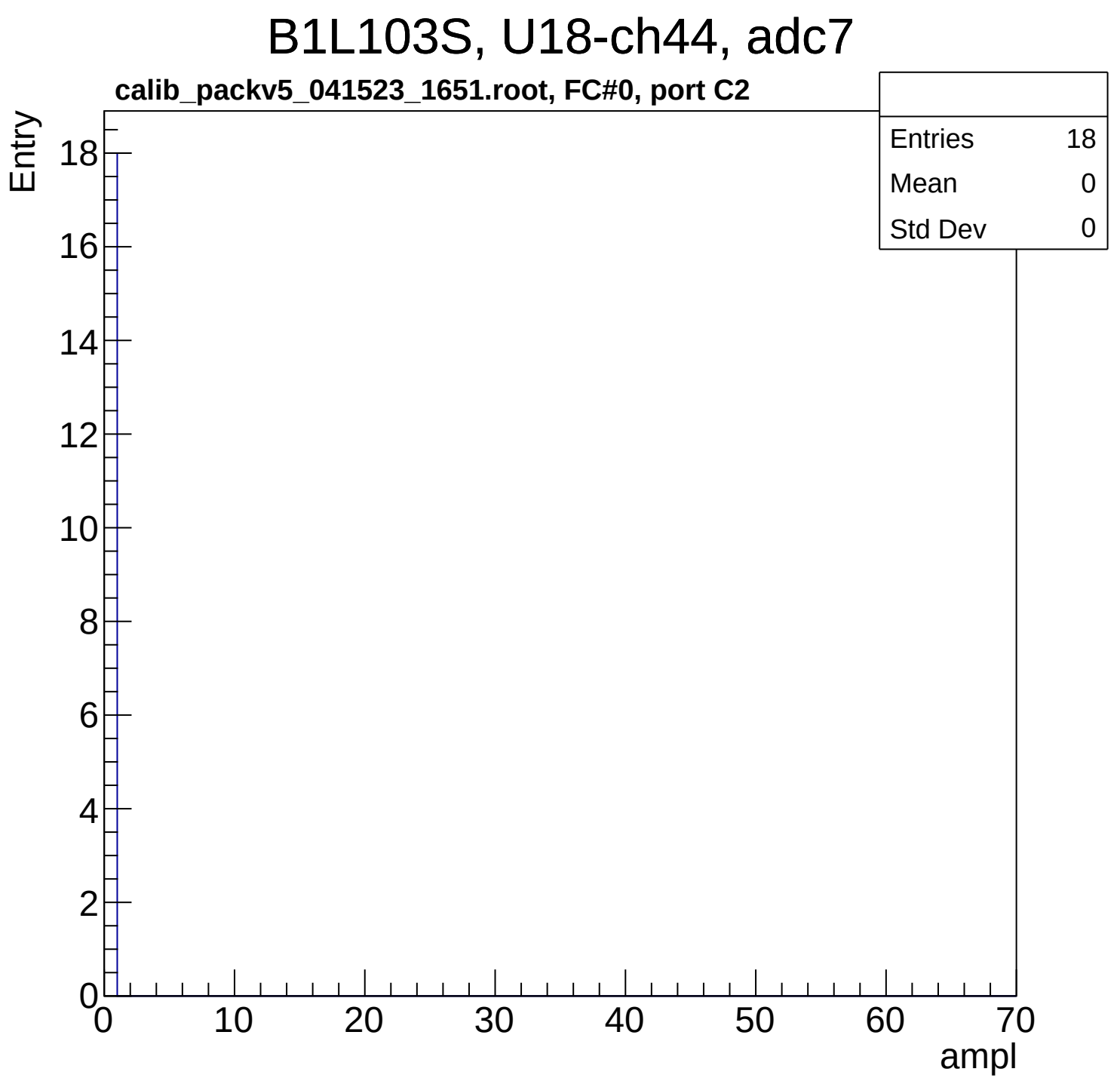
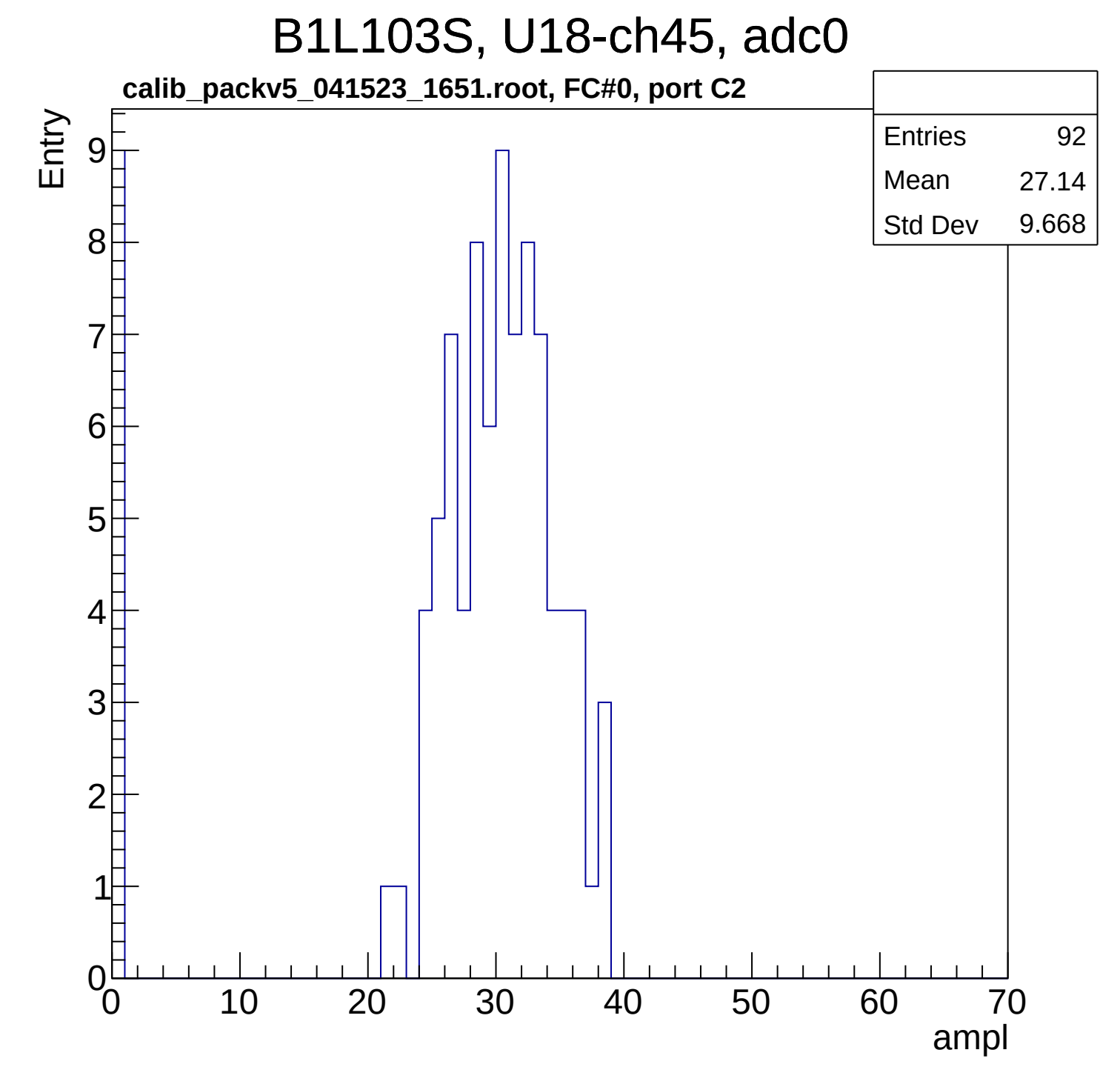
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U18-ch44, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch45, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 92
Mean 27.14
Std Dev 9.668
Entry
ampl
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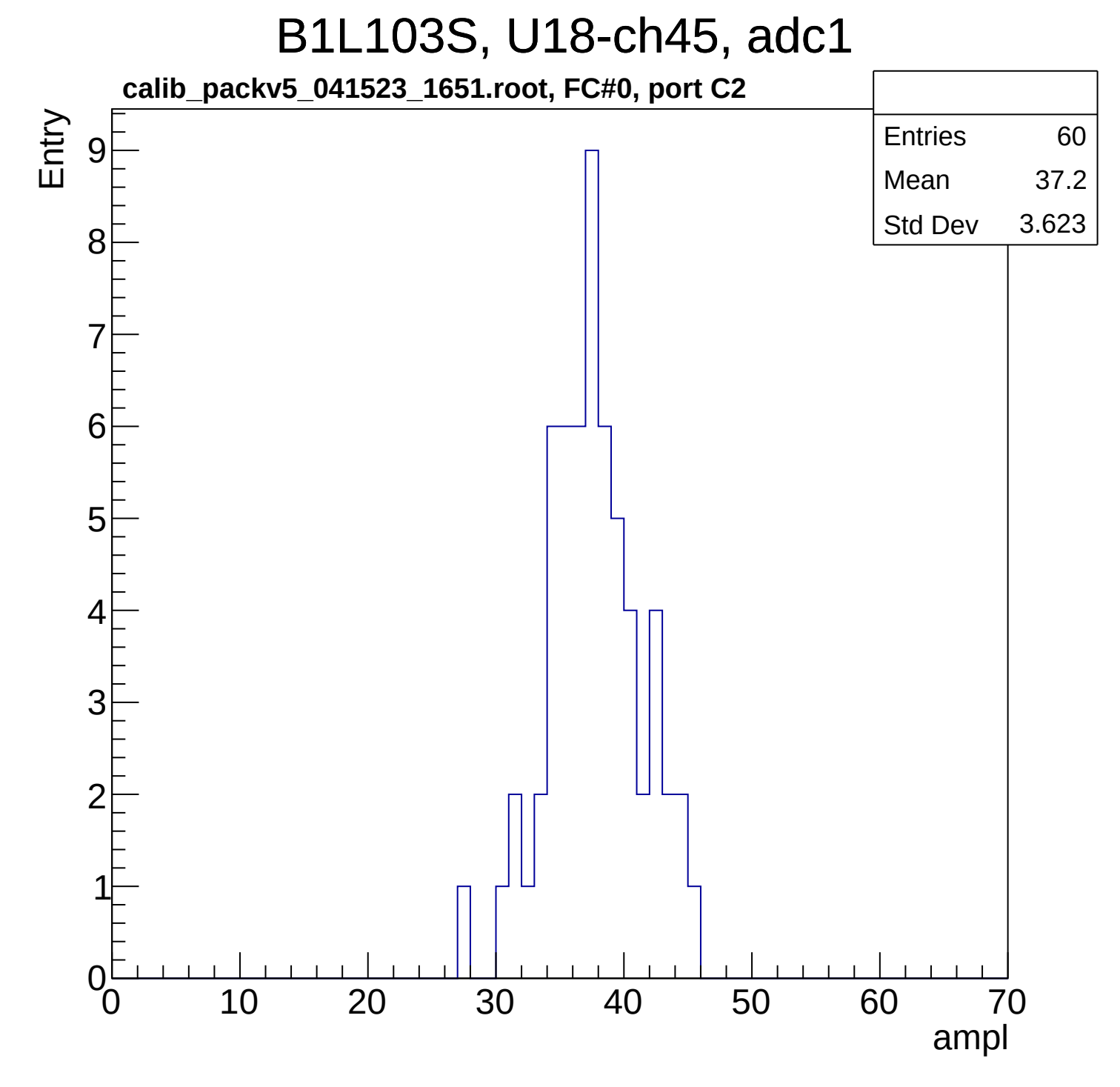
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U18-ch45, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 37.2
Std Dev 3.623
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
30
40
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60
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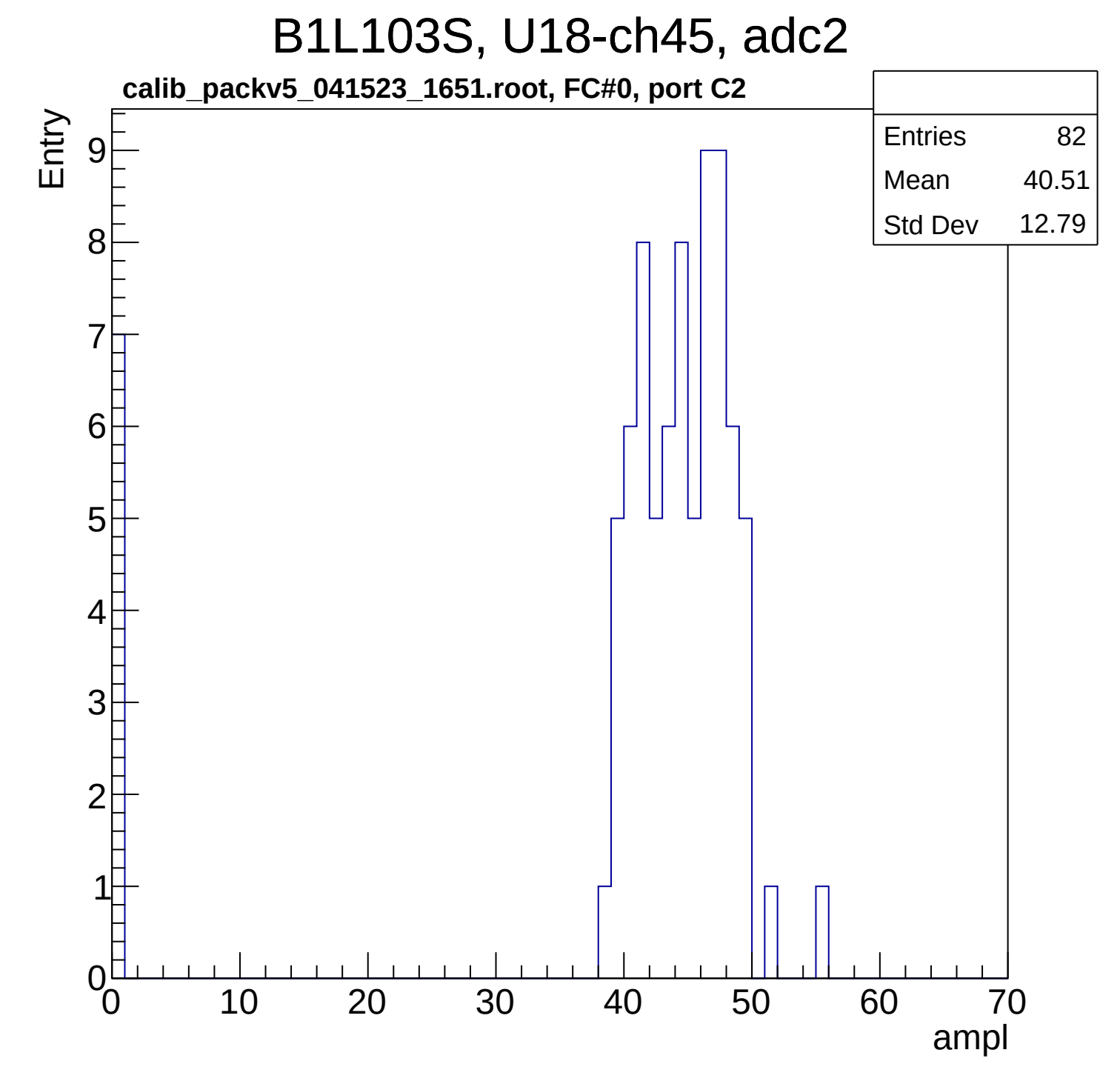
B1L103S, U18-ch45, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 40.51
Std Dev 12.79
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
50
60
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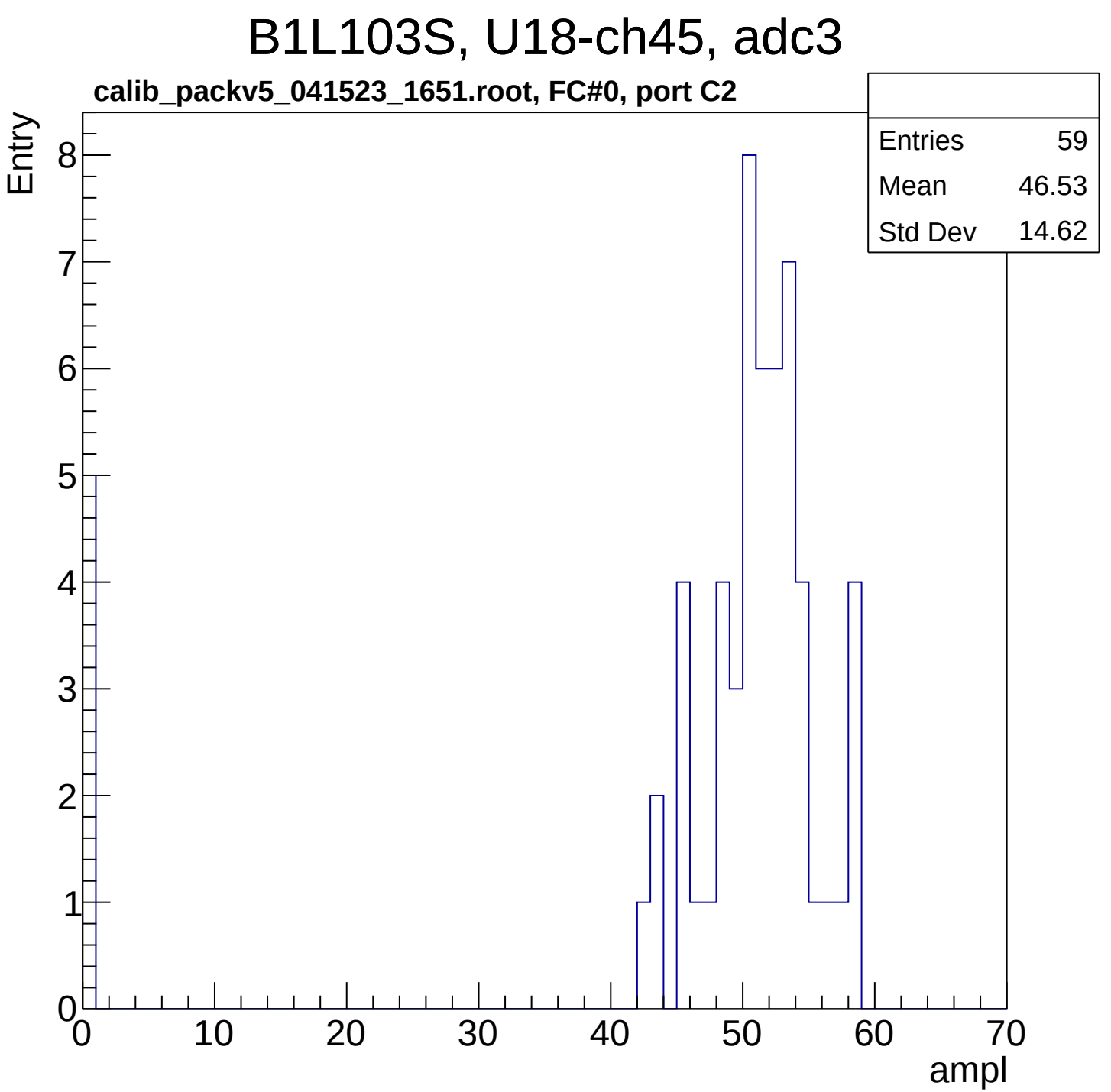
B1L103S, U18-ch45, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 46.53
Std Dev 14.62
Entry
ampl
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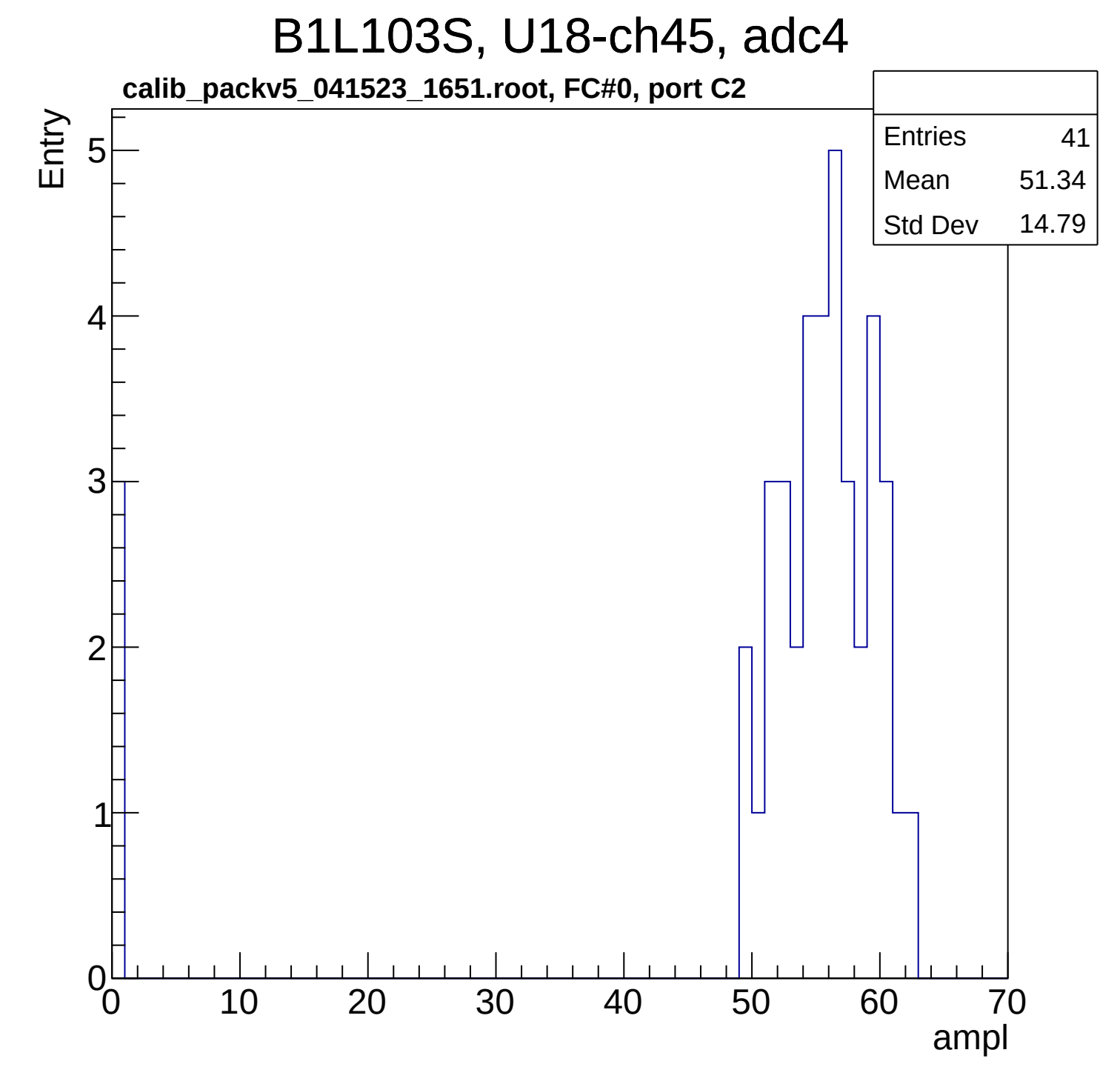
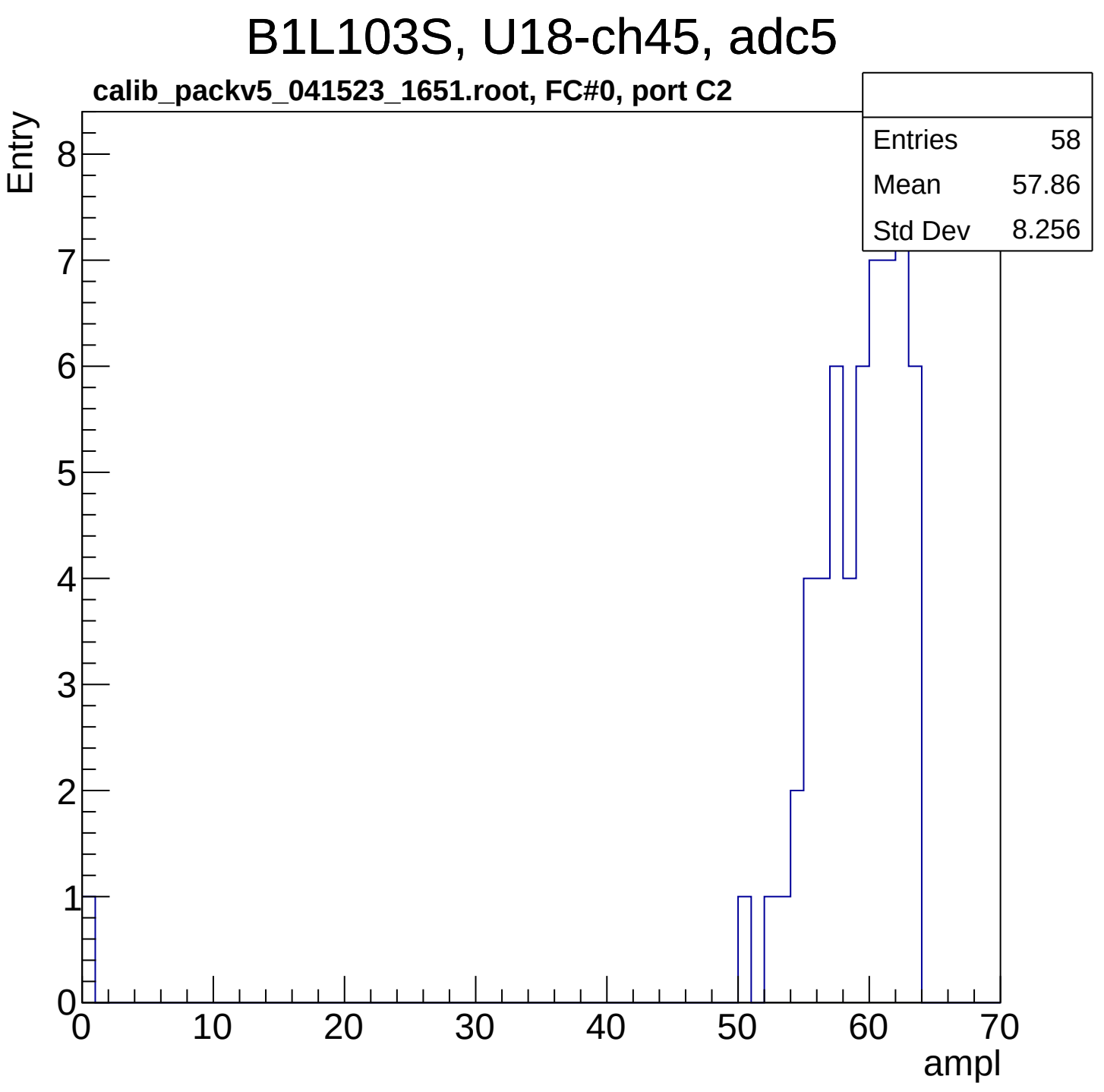
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch45, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 41
Mean 51.34
Std Dev 14.79
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch45, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 57.86
Std Dev 8.256
Entry
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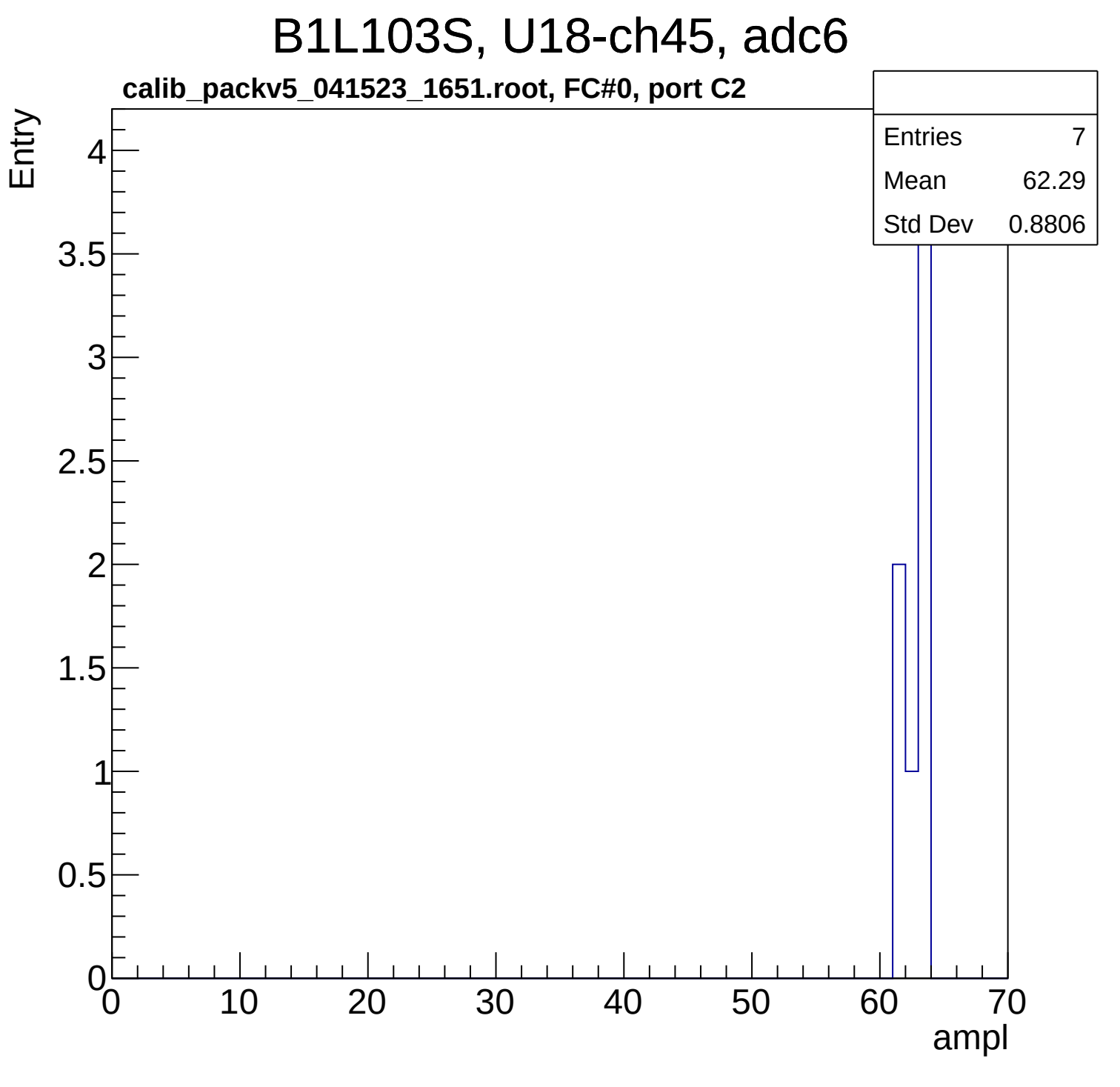
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch45, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 62.29
Std Dev 0.8806
Entry
ampl
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0.5
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1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
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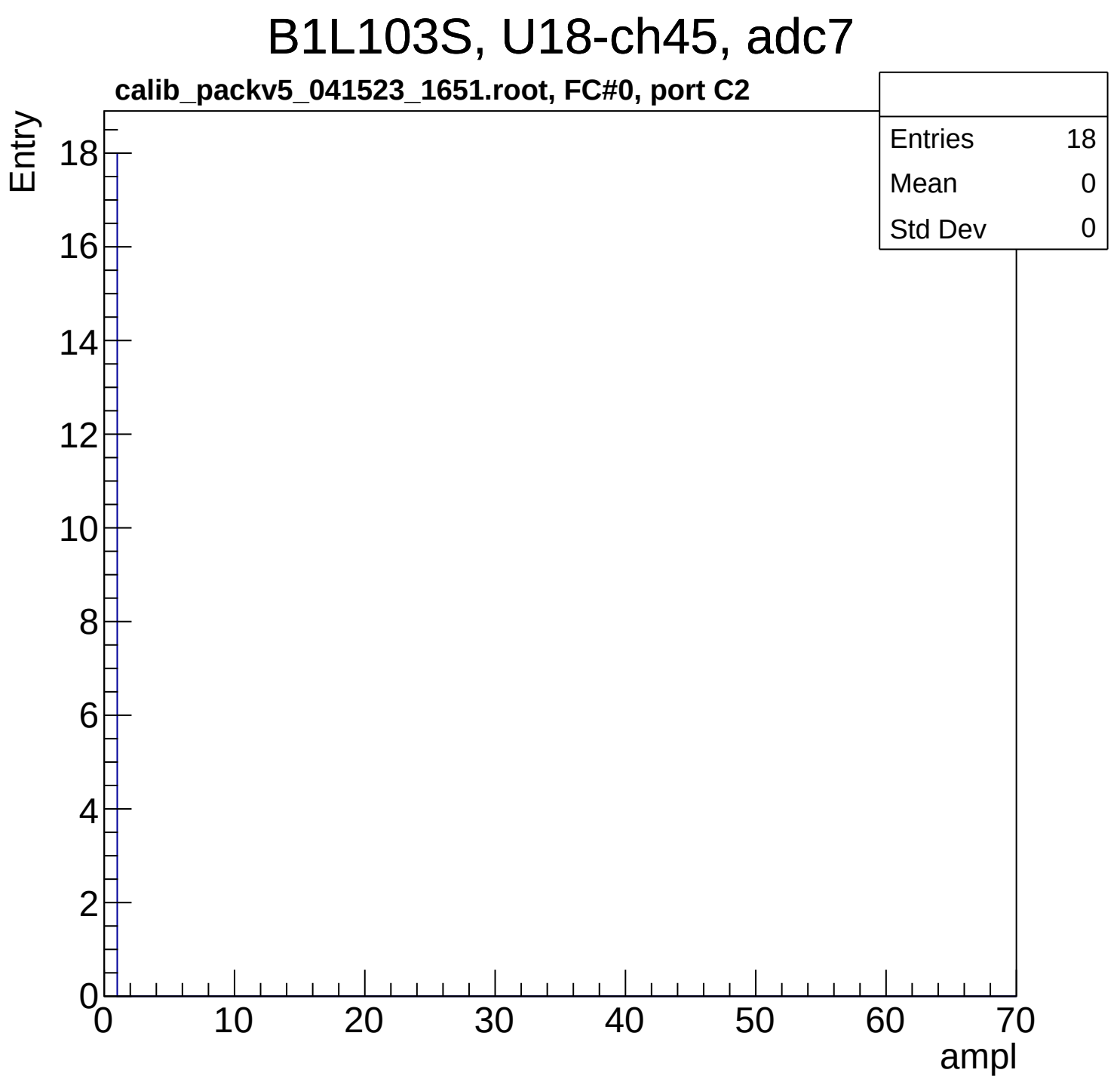
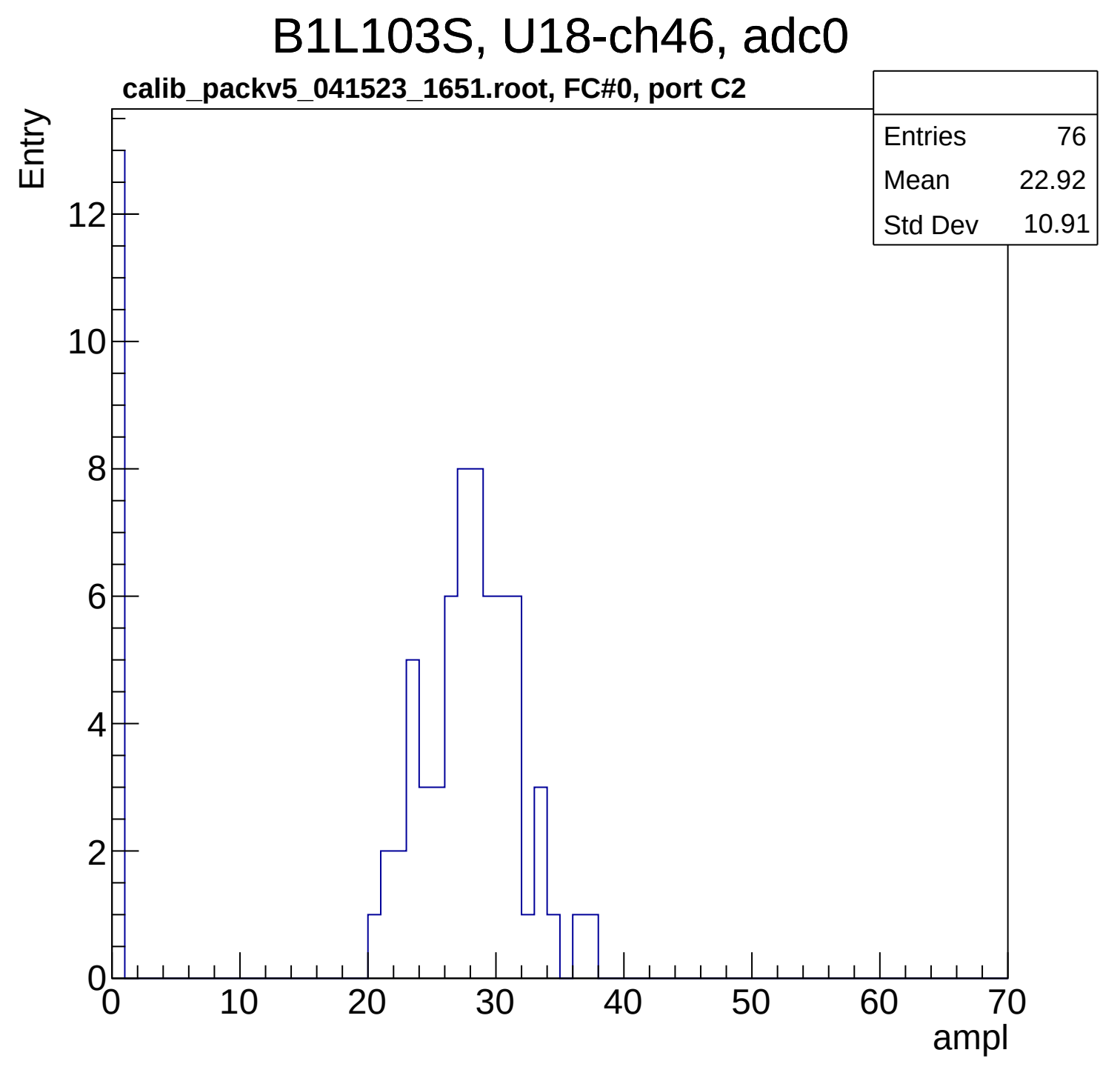

B1L103S, U18-ch45, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch46, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 22.92
Std Dev 10.91
Entry
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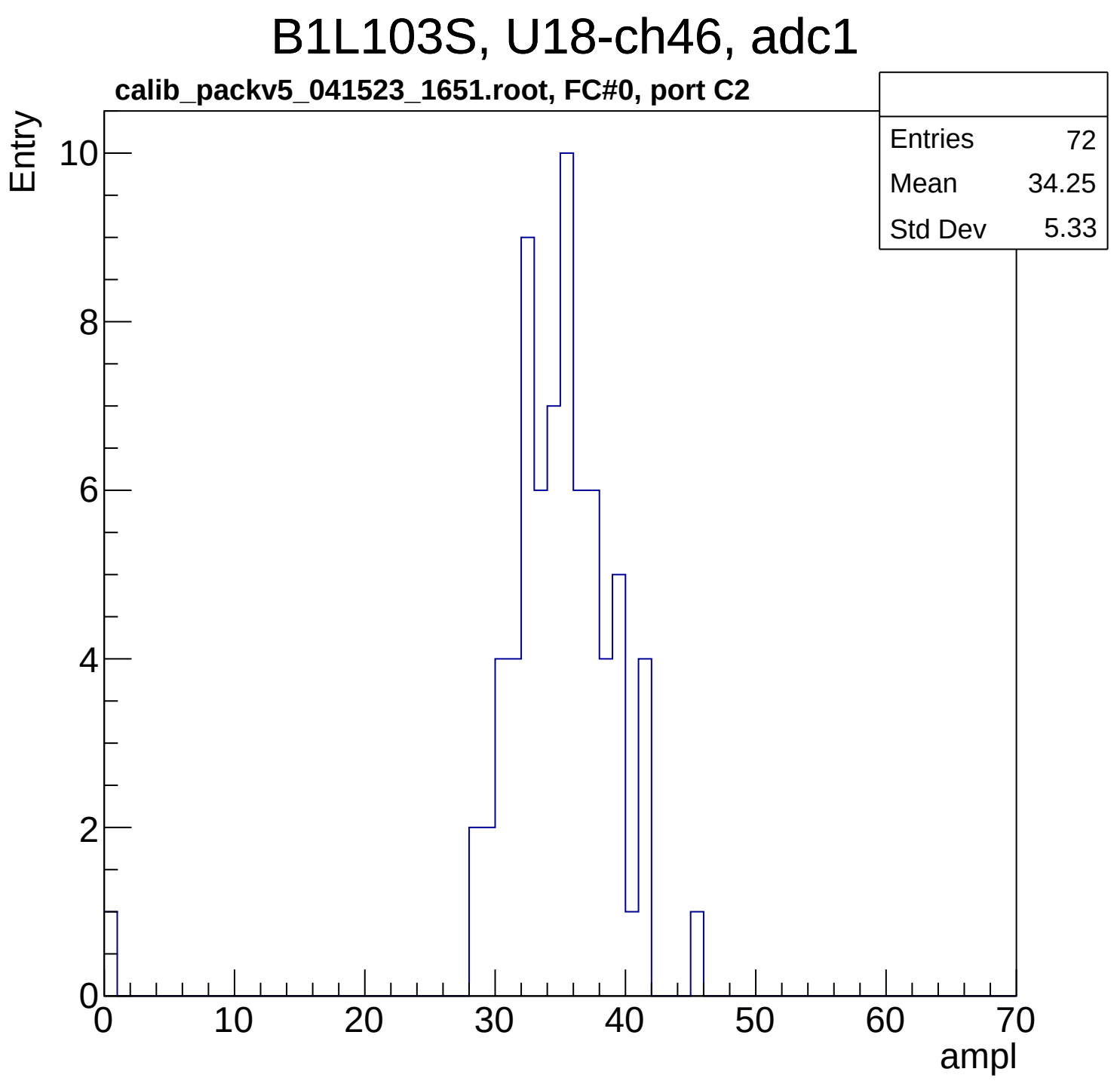
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch46, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 34.25
Std Dev 5.33
Entry
ampl
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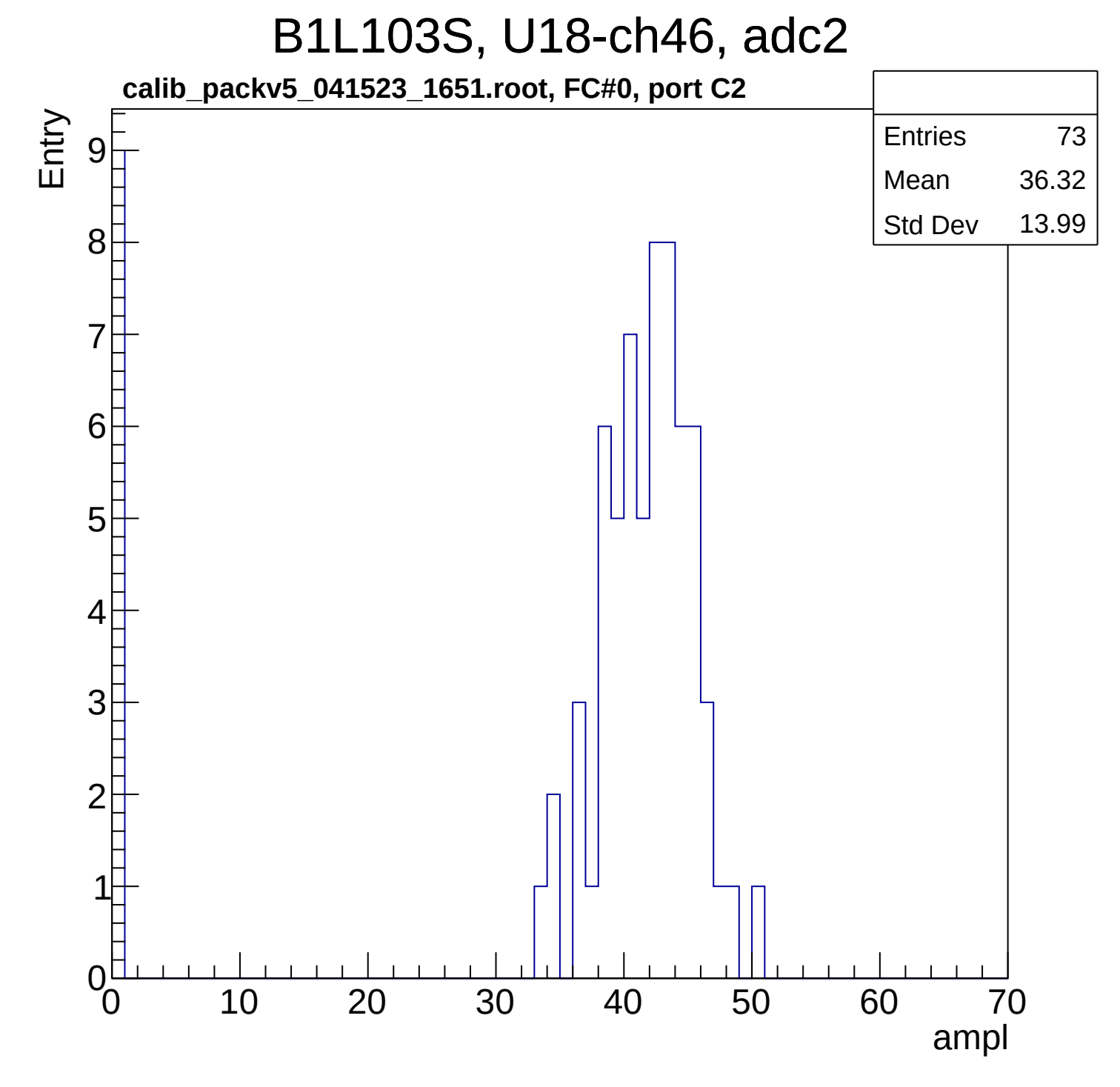
8
10
0
10
20
30
40
50
60
70


B1L103S, U18-ch46, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 36.32
Std Dev 13.99
Entry
ampl
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3
4
5
6
7
8
9
0
10
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30
40
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60
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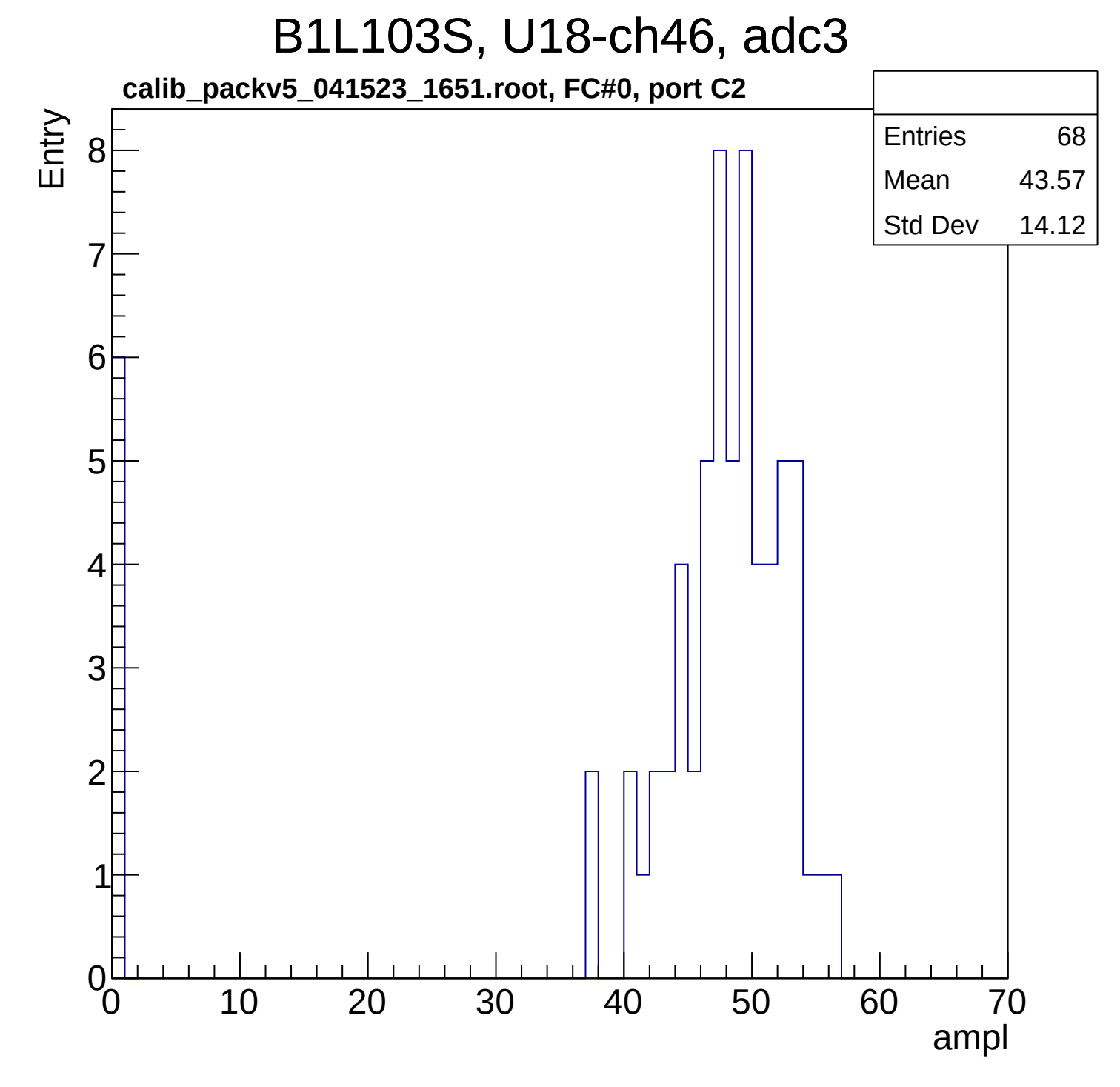
B1L103S, U18-ch46, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 43.57
Std Dev 14.12
Entry
ampl
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5
6
7
8
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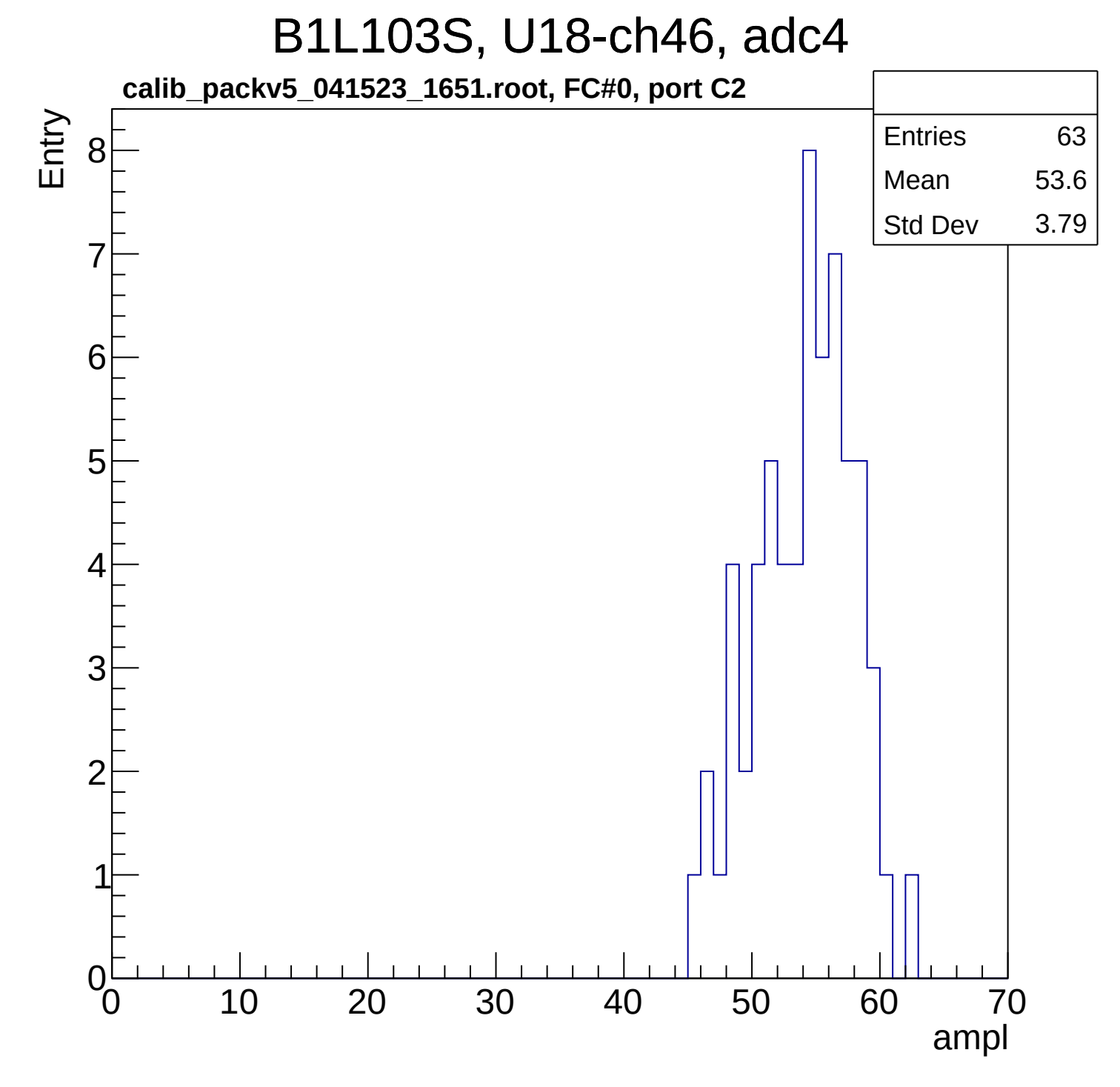
60
70


B1L103S, U18-ch46, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 53.6
Std Dev 3.79
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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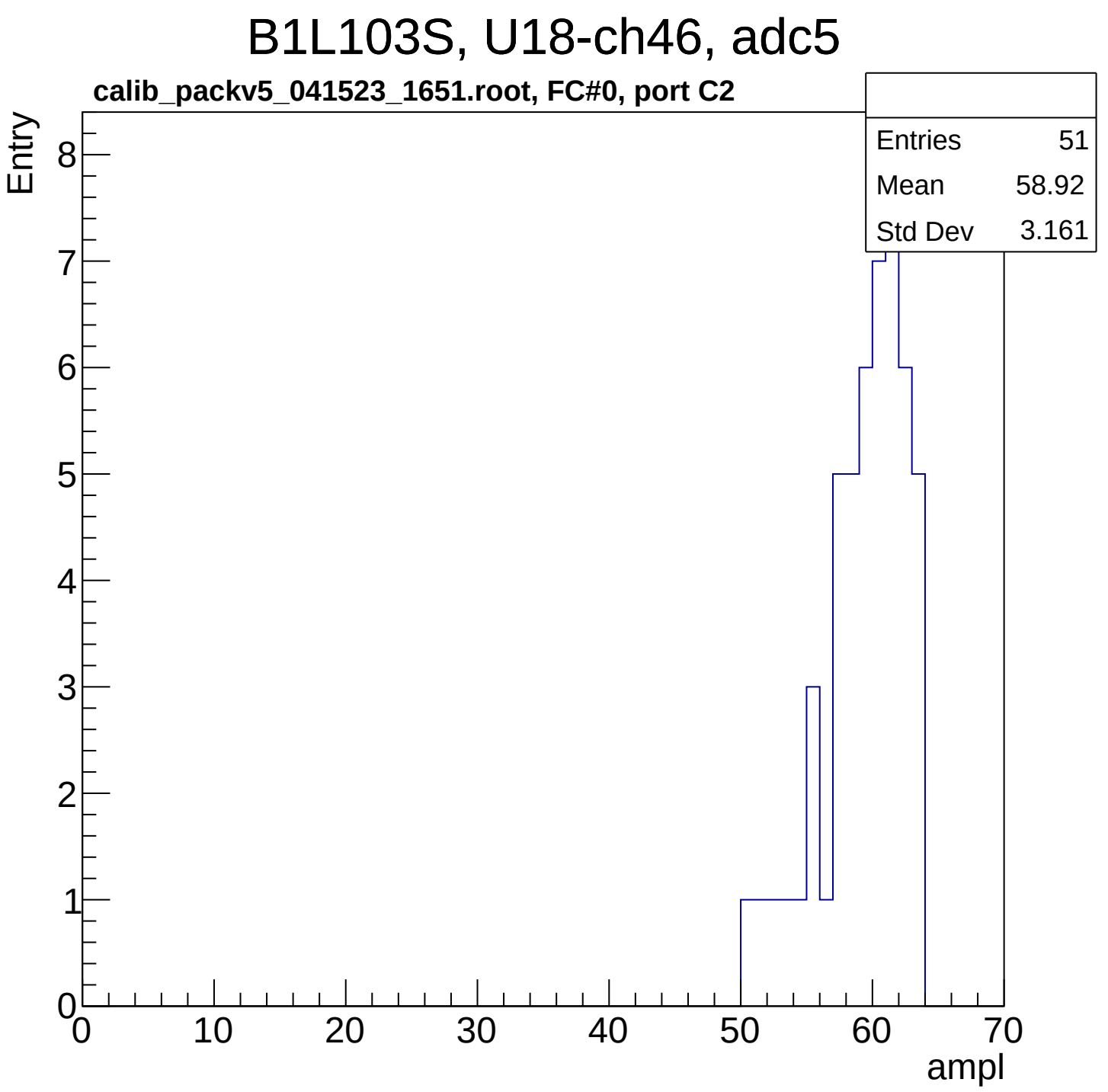
B1L103S, U18-ch46, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 58.92
Std Dev 3.161
Entry
ampl
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3
4
5
6
7
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0
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20
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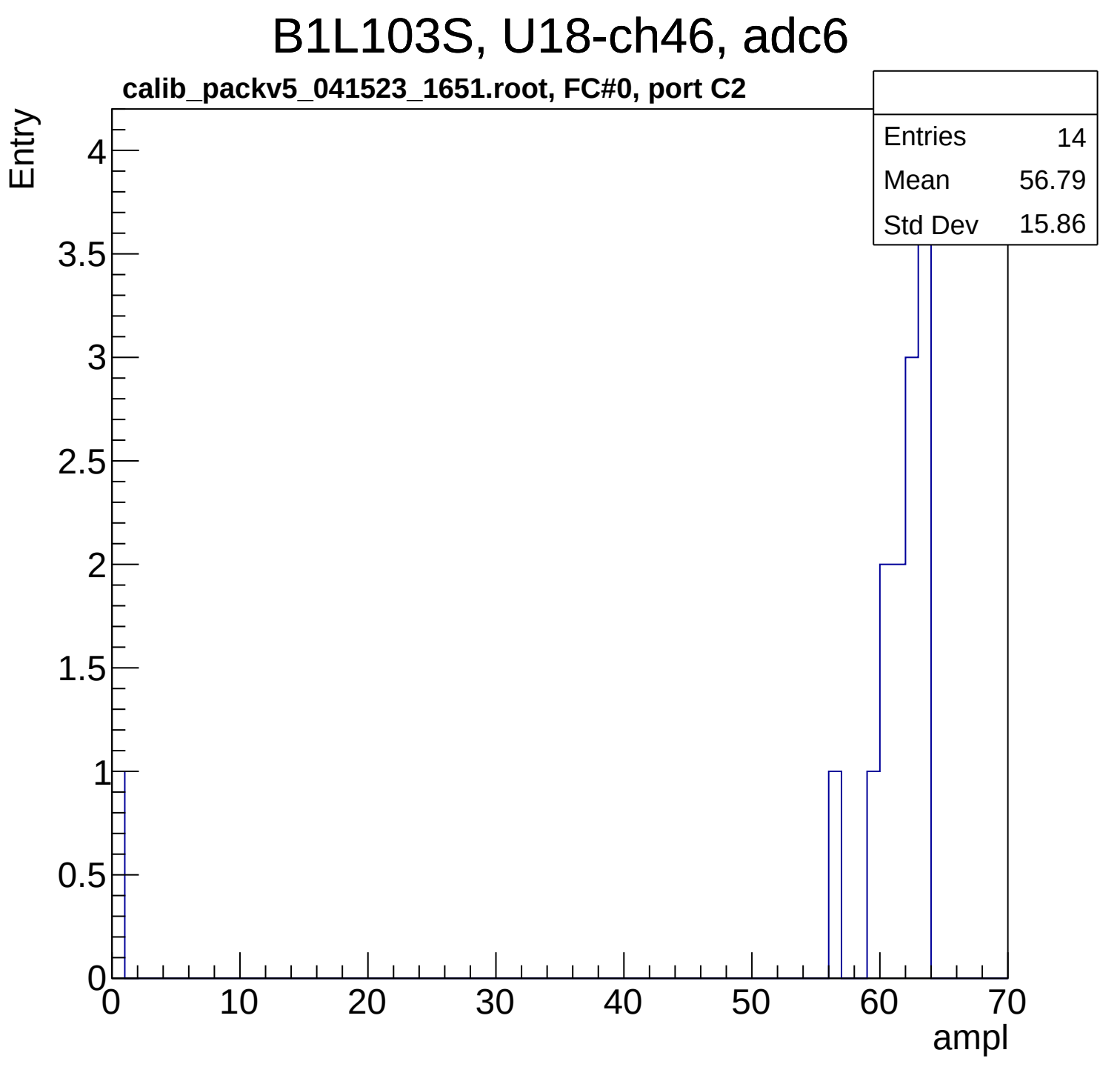
40
50
60
70


B1L103S, U18-ch46, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 14
Mean 56.79
Std Dev 15.86
Entry
ampl
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1.5
2
2.5
3
3.5
4
0
10
20
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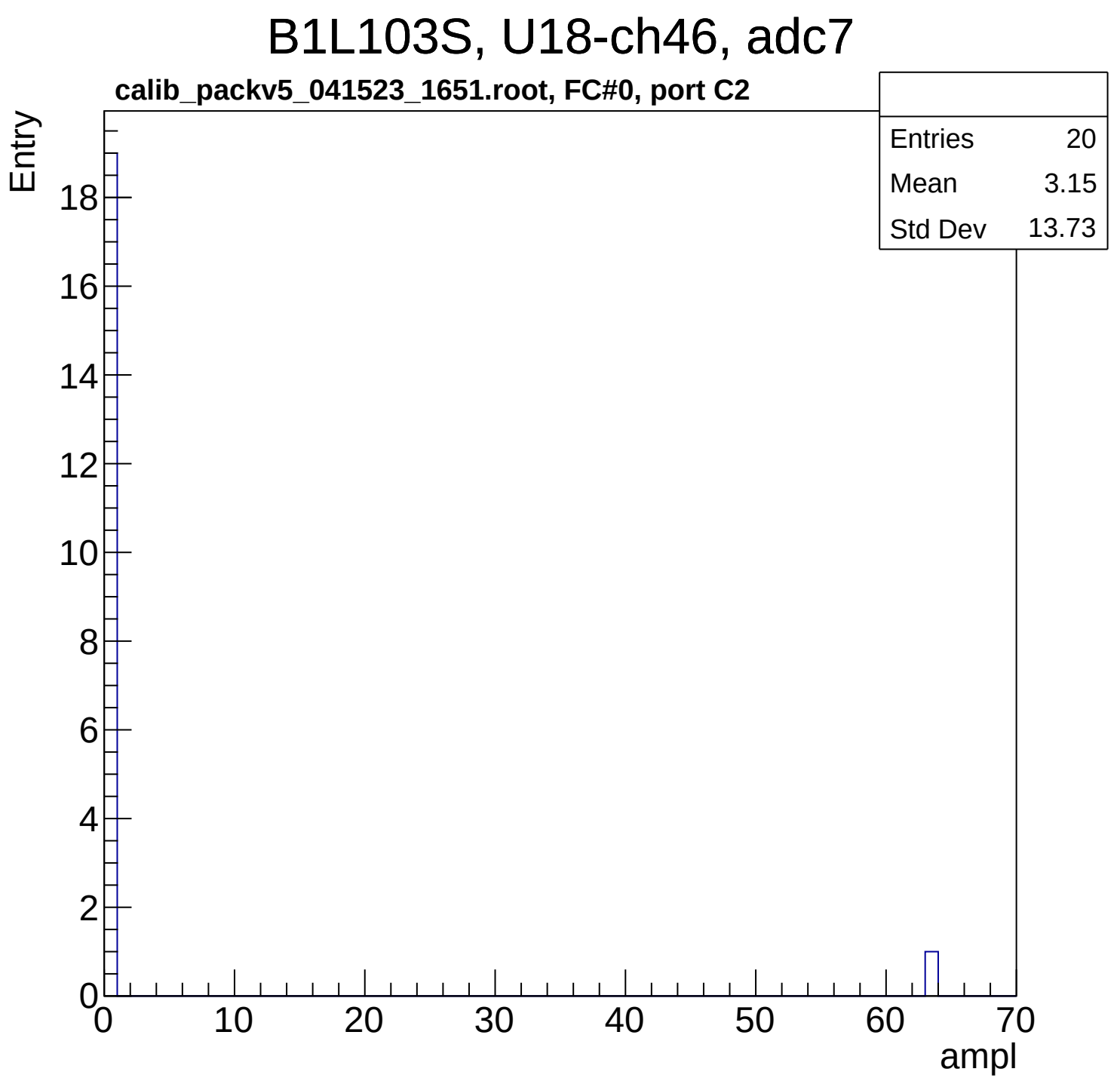
40
50
60
70


B1L103S, U18-ch46, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
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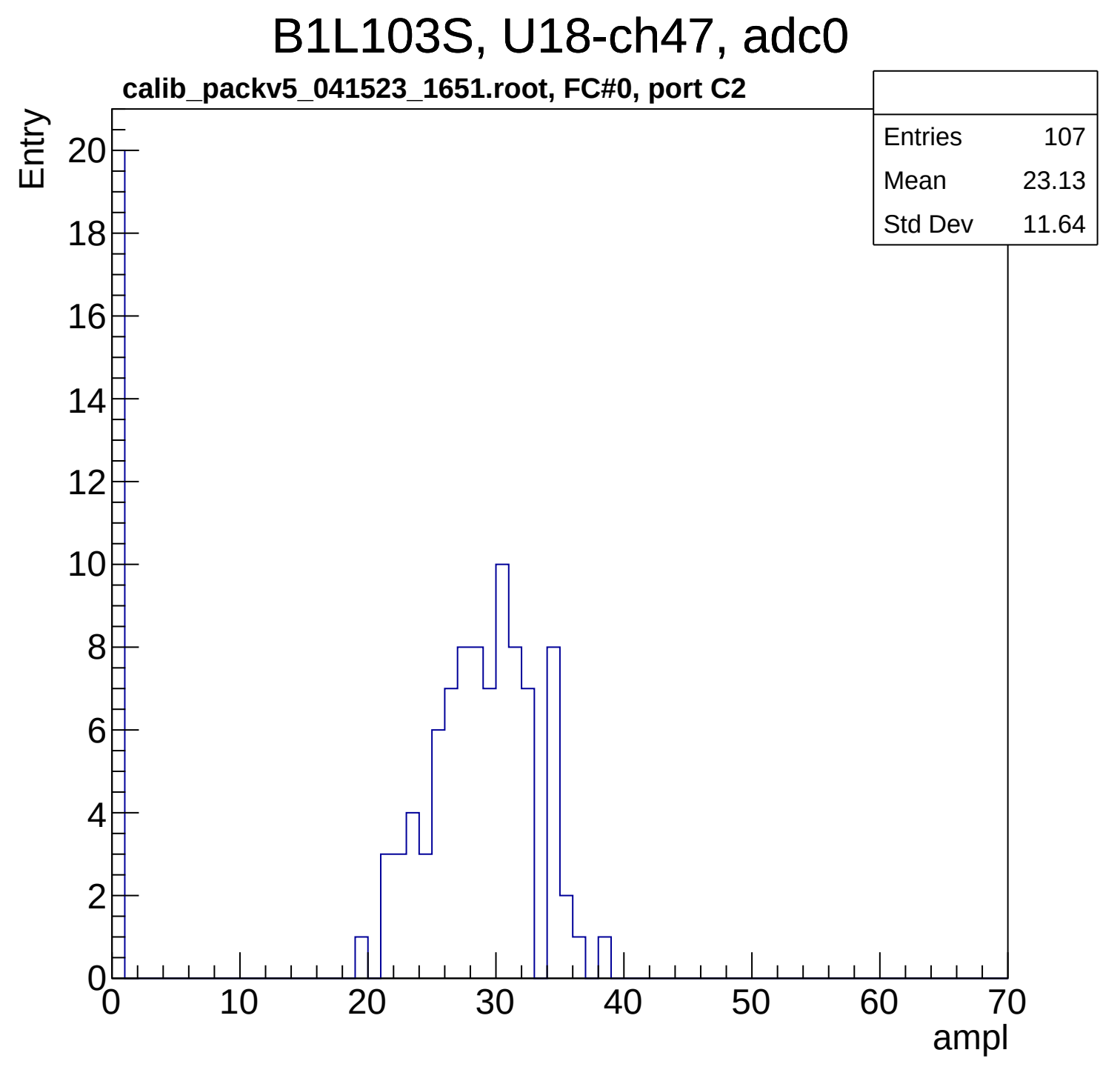
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch47, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 107
Mean 23.13
Std Dev 11.64
Entry
ampl
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6
8
10
12
14
16
18
20
0
10
20
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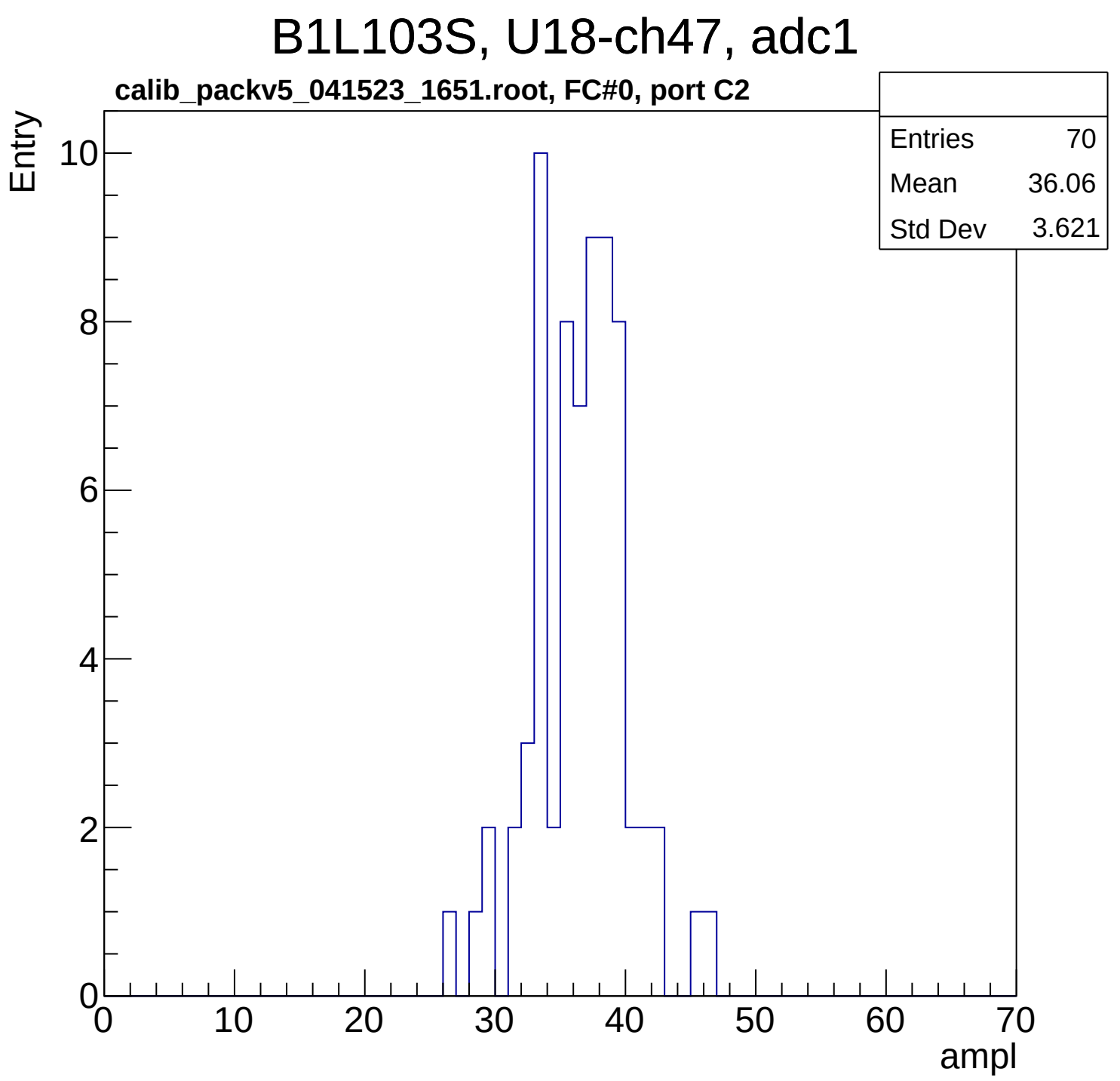
B1L103S, U18-ch47, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 36.06
Std Dev 3.621
Entry
ampl
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6
8
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0
10
20
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40
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60
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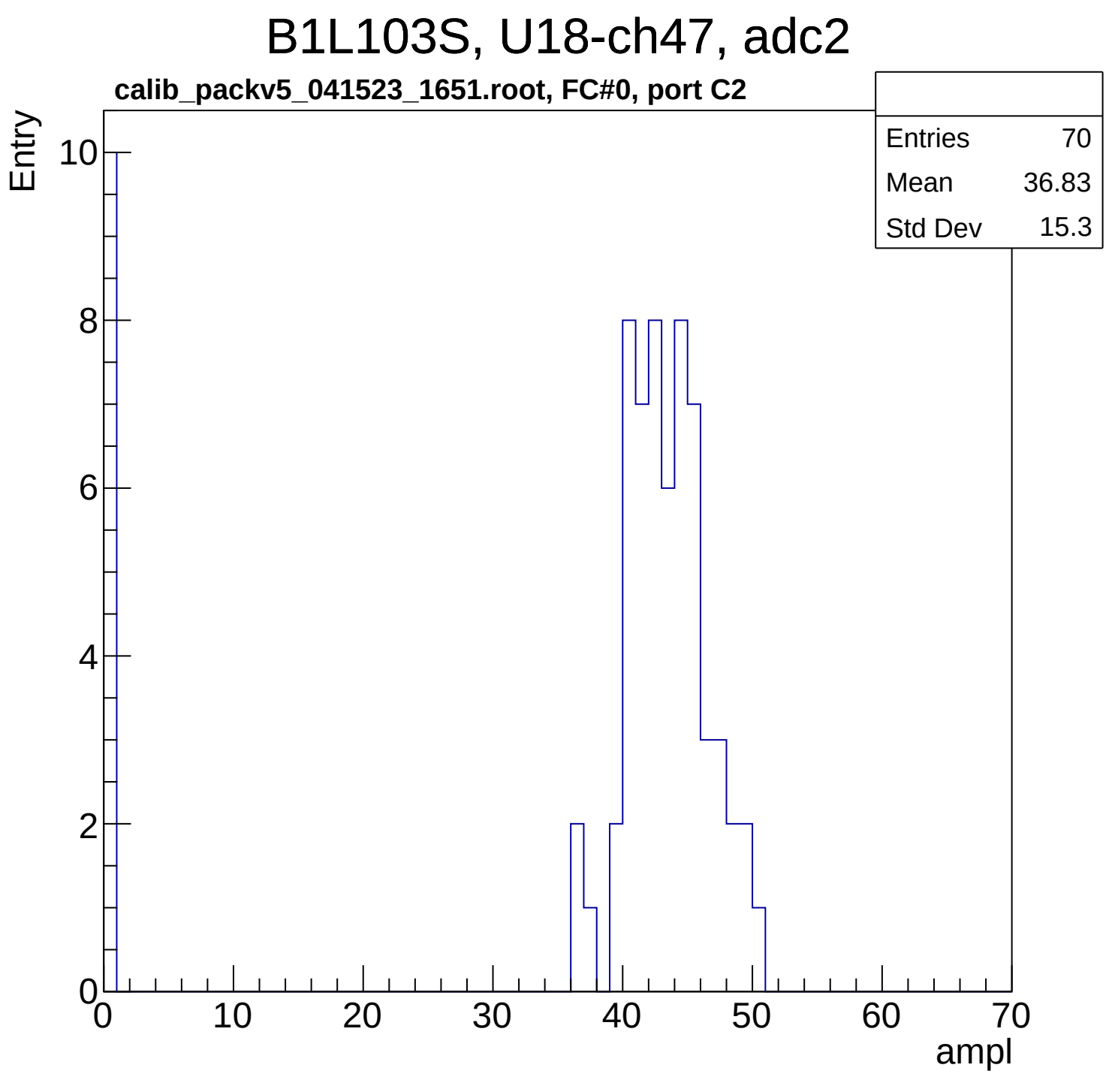
B1L103S, U18-ch47, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 36.83
Std Dev 15.3
Entry
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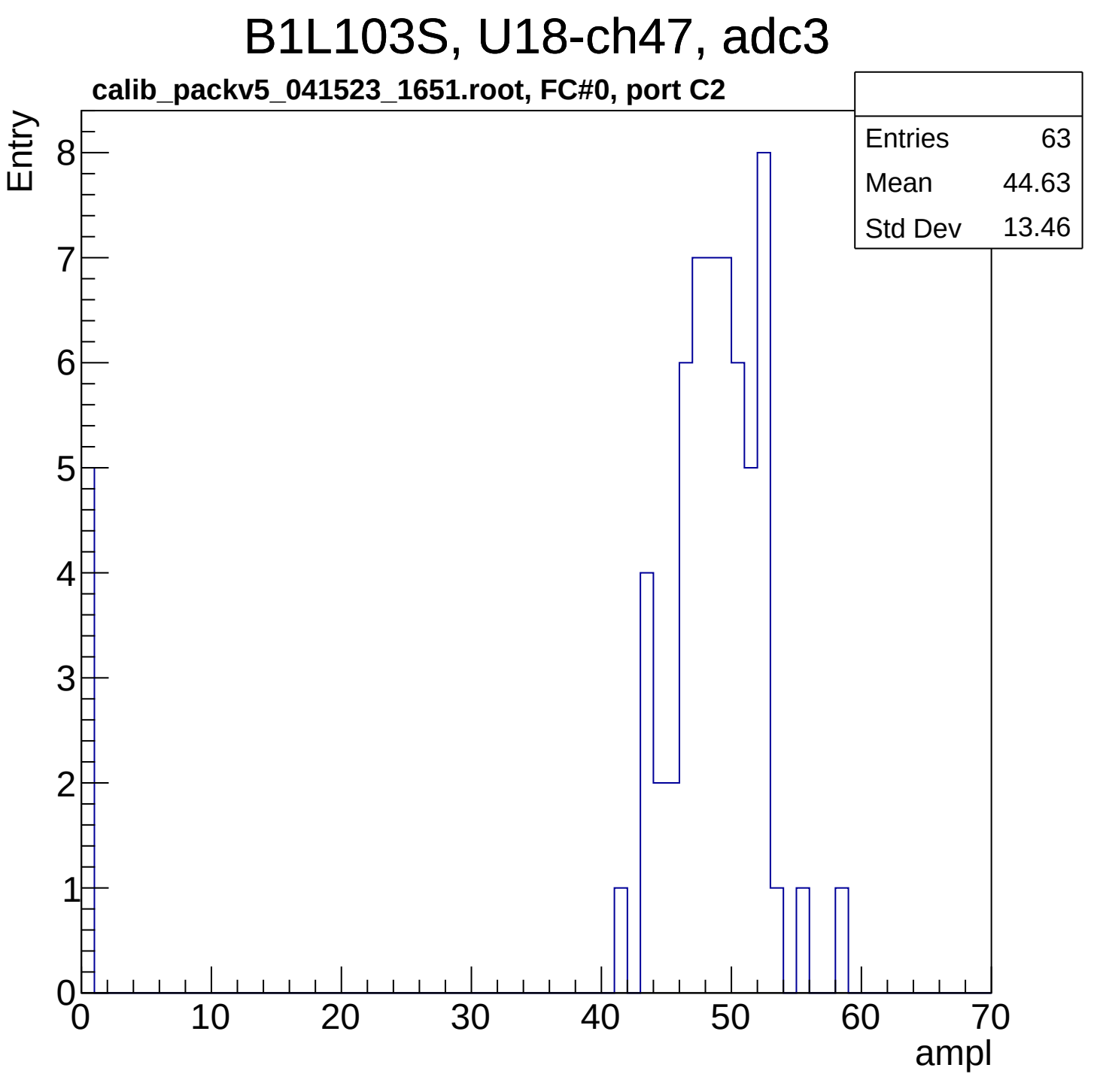
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch47, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 44.63
Std Dev 13.46
Entry
ampl
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4
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60
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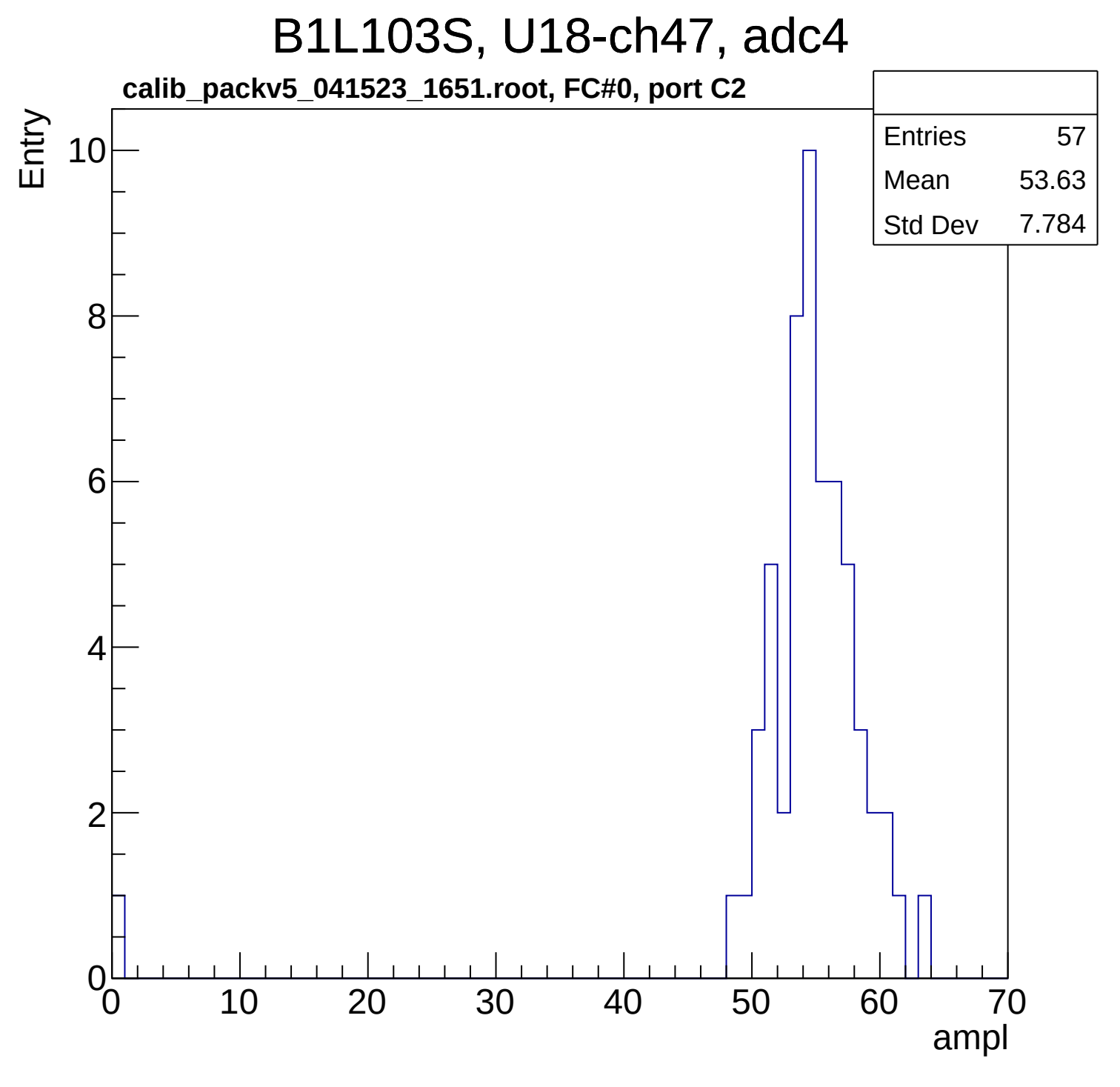
B1L103S, U18-ch47, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 53.63
Std Dev 7.784
Entry
ampl
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8
10
0
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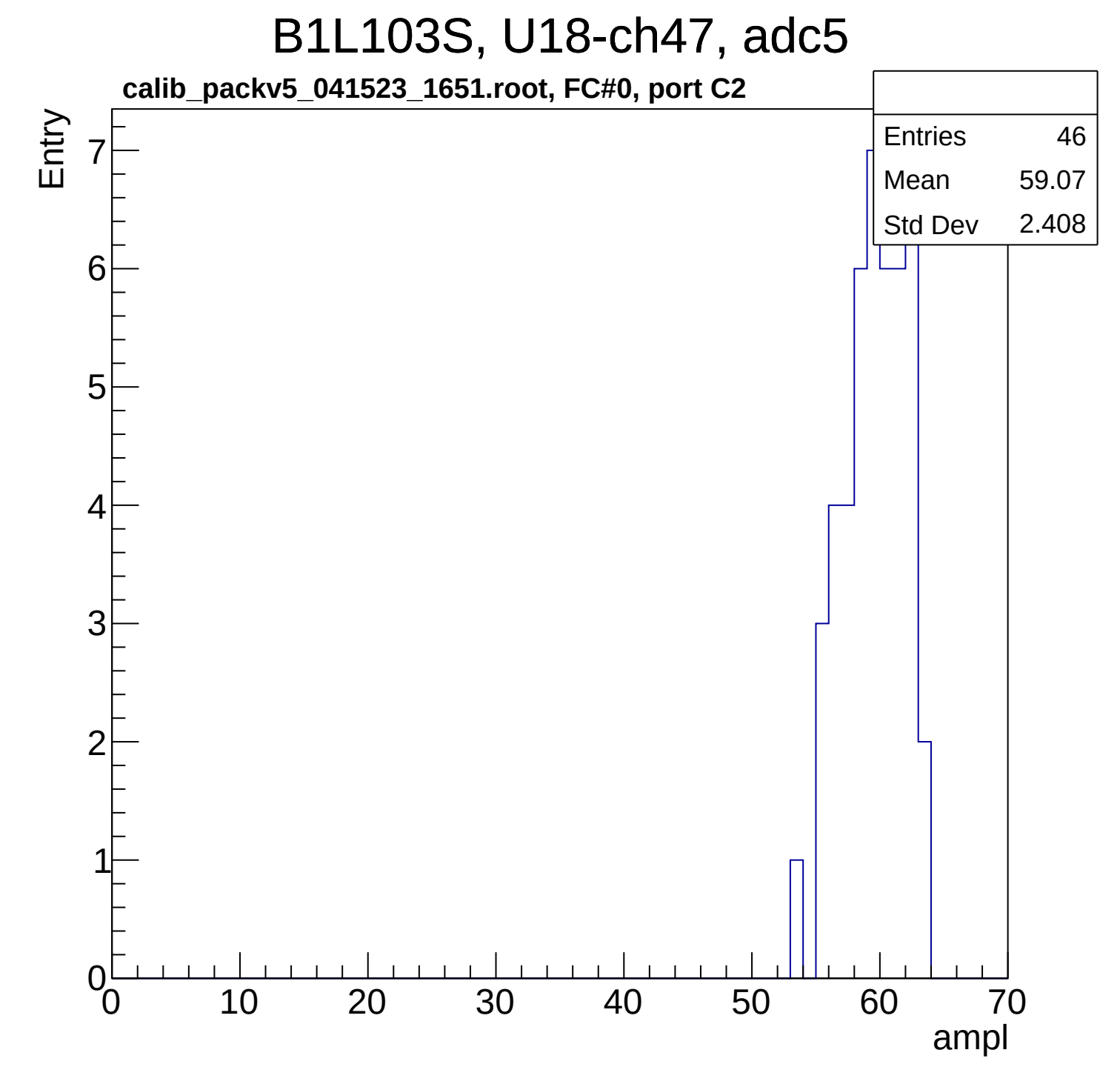
60
70


B1L103S, U18-ch47, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 59.07
Std Dev 2.408
Entry
ampl
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0
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40
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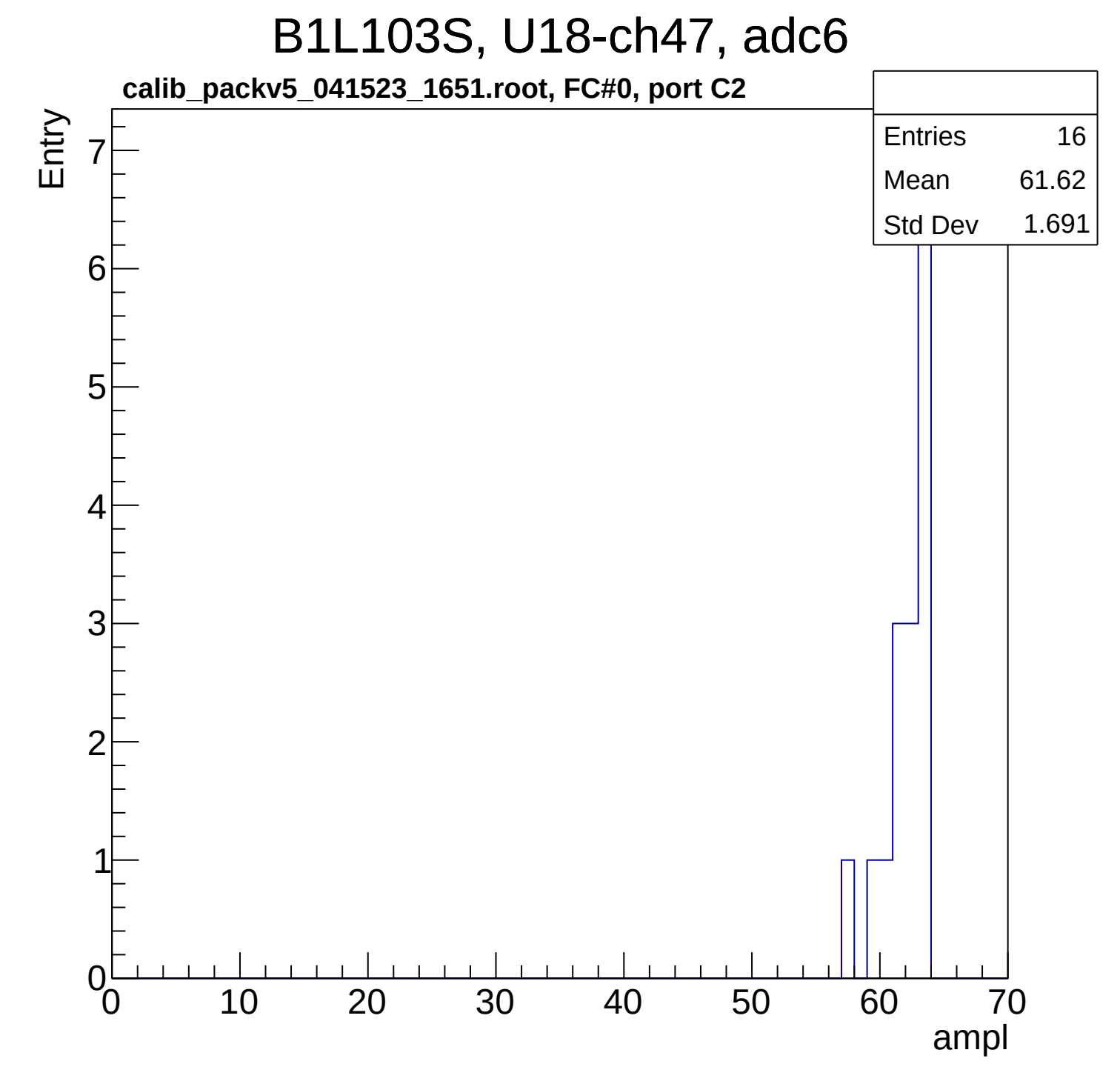
60
70


B1L103S, U18-ch47, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 16
Mean 61.62
Std Dev 1.691
Entry
ampl
0
1
2
3
4
5
6
7
0
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40
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60
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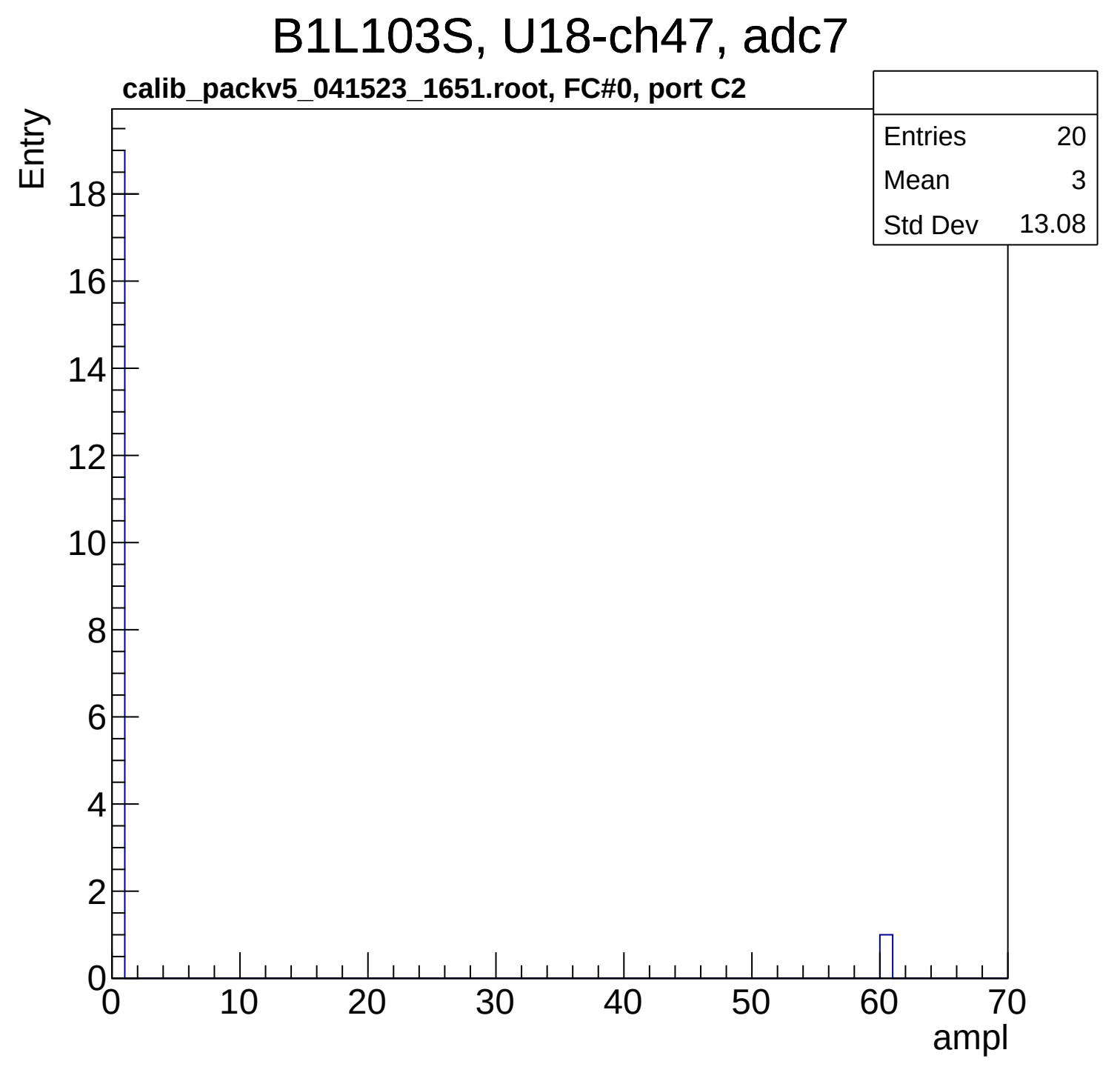
B1L103S, U18-ch47, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3
Std Dev 13.08
Entry
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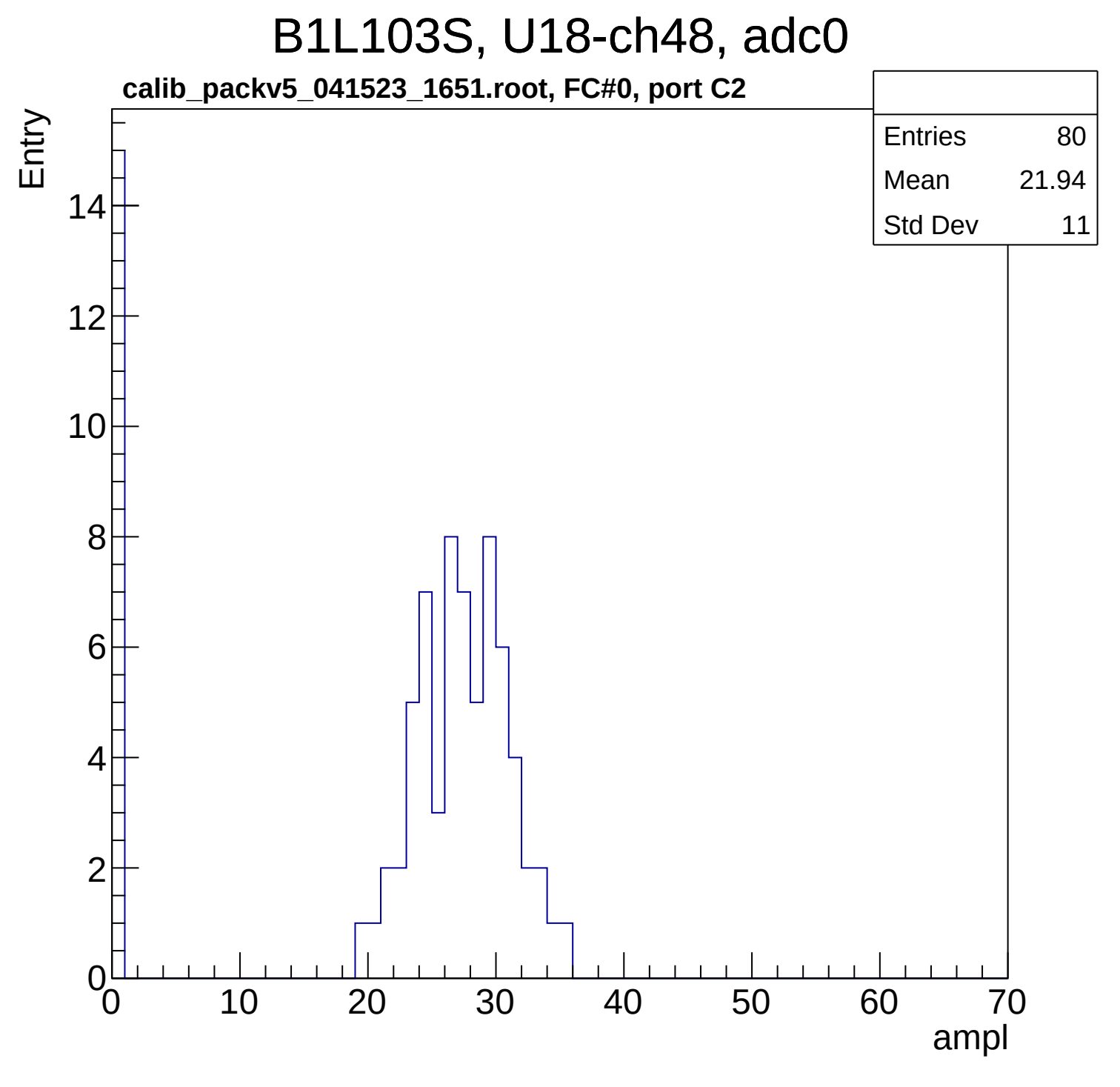
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch48, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 21.94
Std Dev 11
Entry
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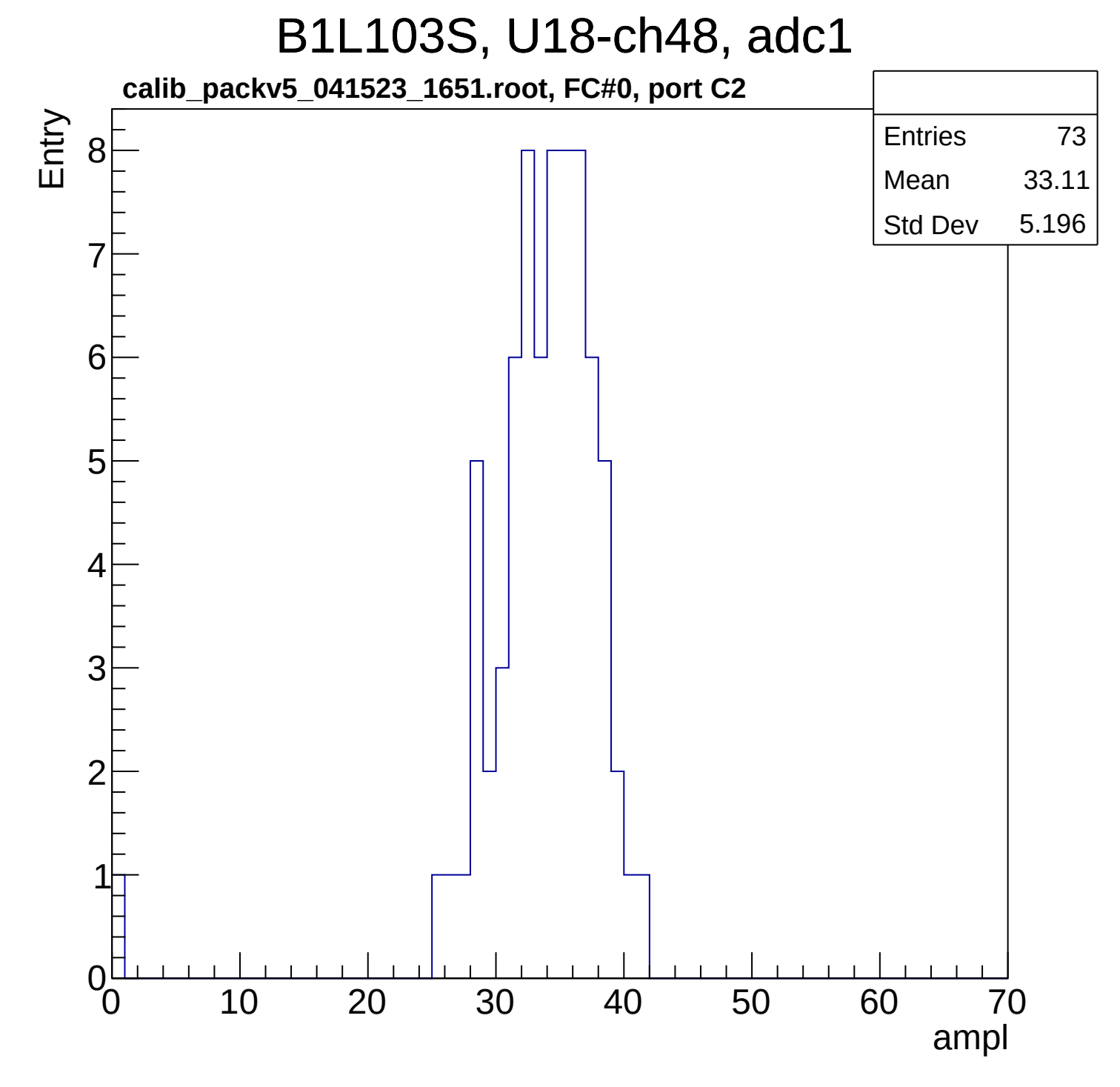
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch48, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 33.11
Std Dev 5.196
Entry
ampl
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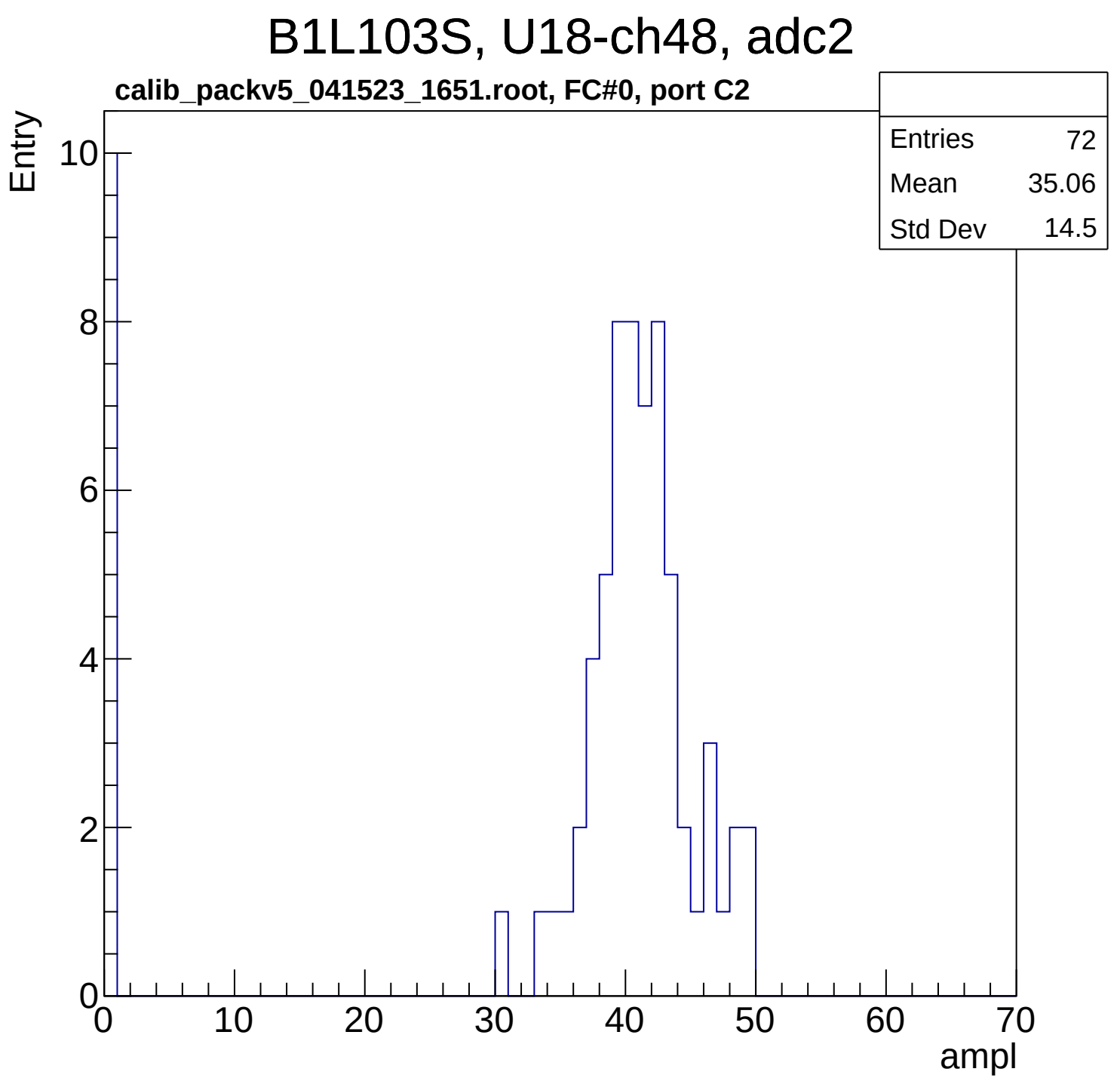
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch48, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 35.06
Std Dev 14.5
Entry
ampl
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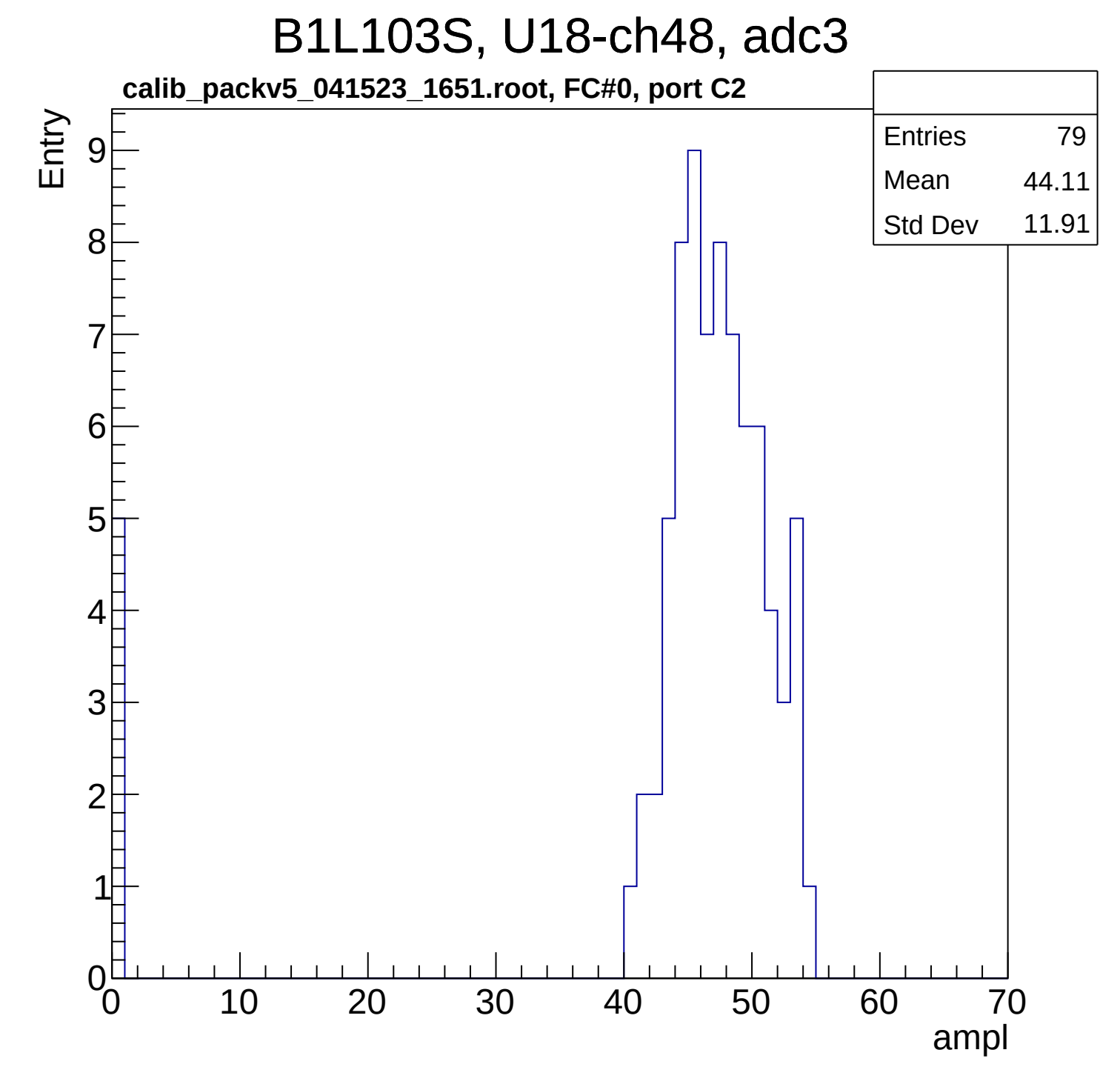
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U18-ch48, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 44.11
Std Dev 11.91
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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40
50
60
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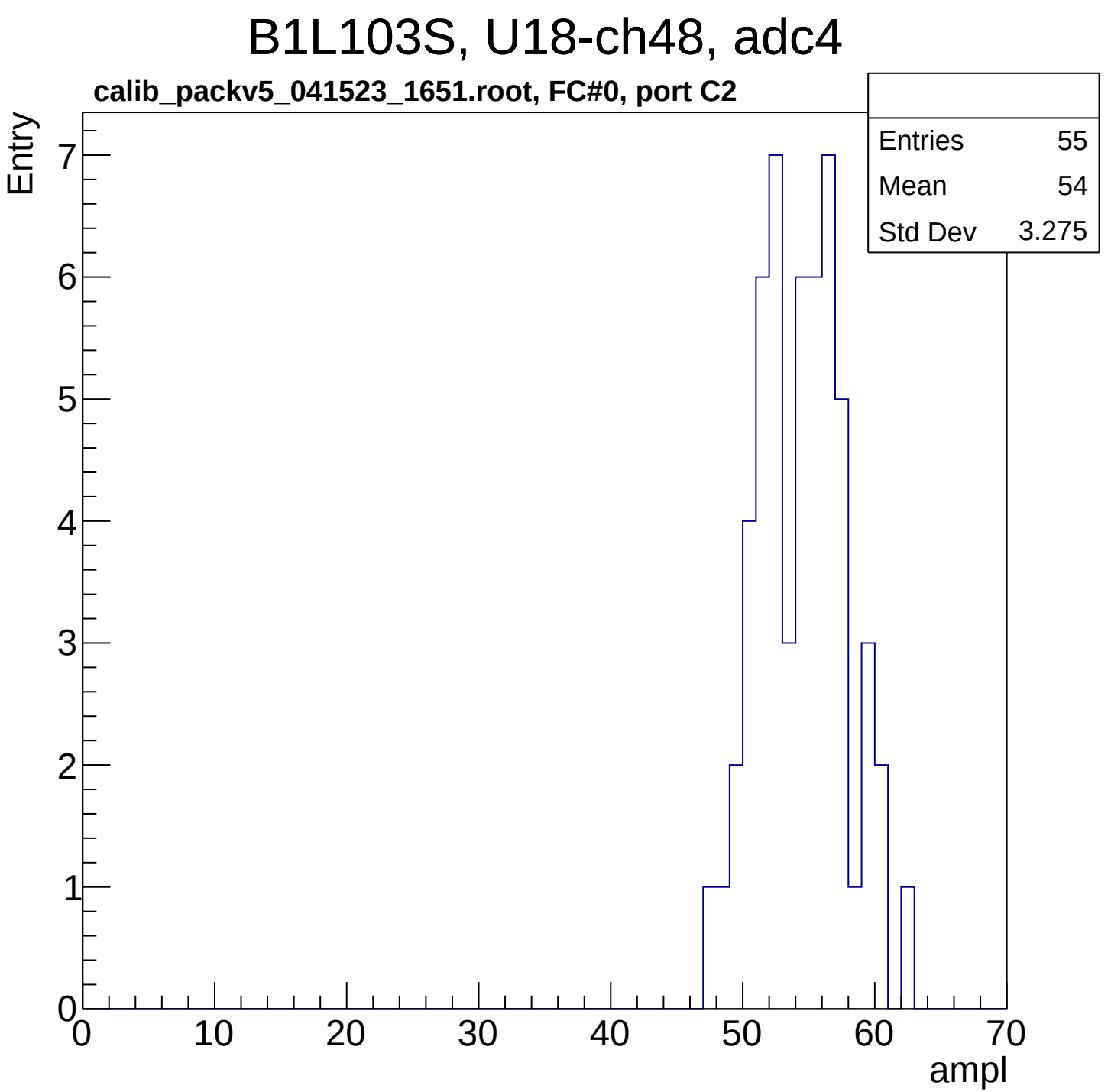
B1L103S, U18-ch48, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 54
Std Dev 3.275
Entry
ampl
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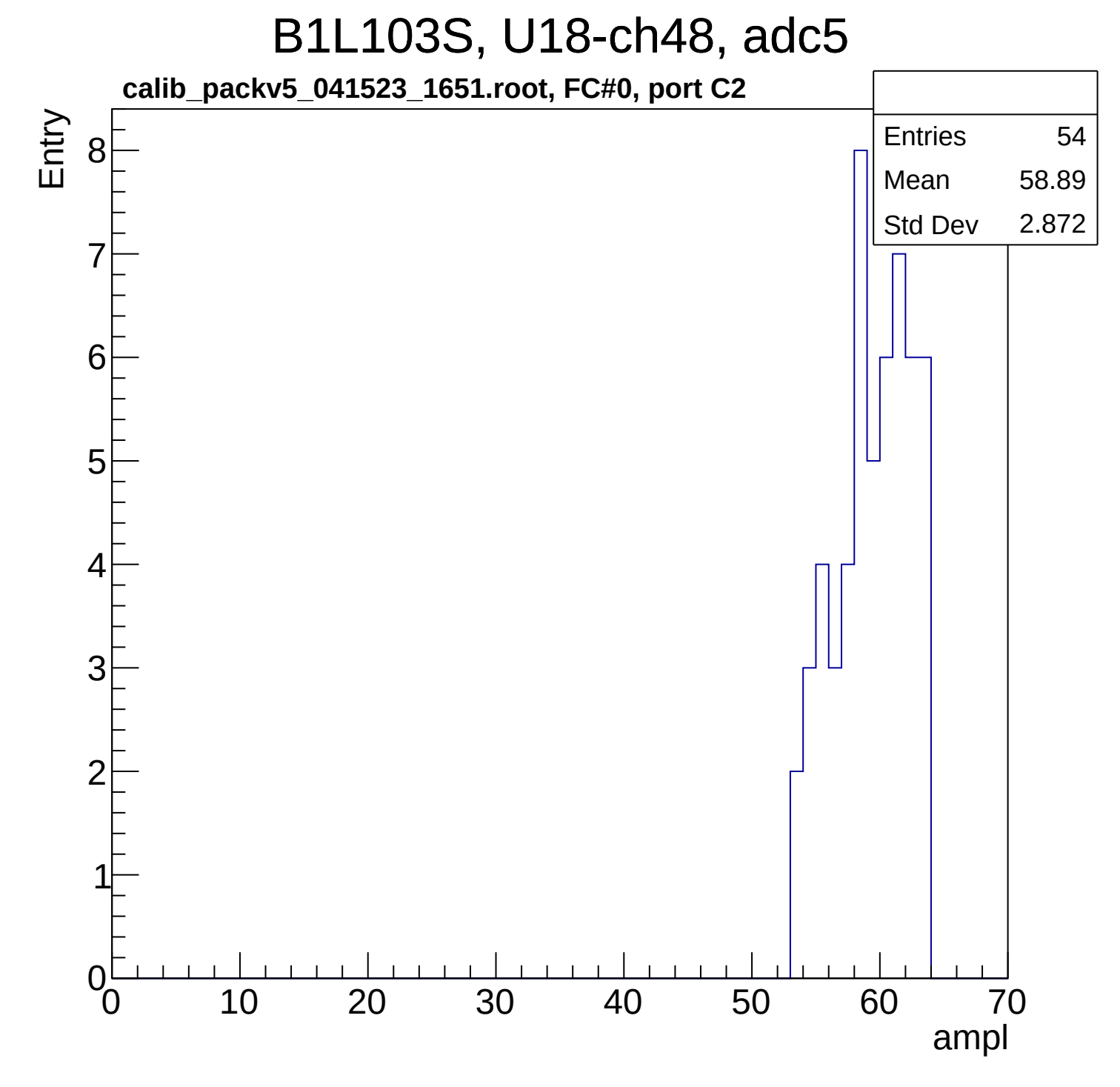
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U18-ch48, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 58.89
Std Dev 2.872
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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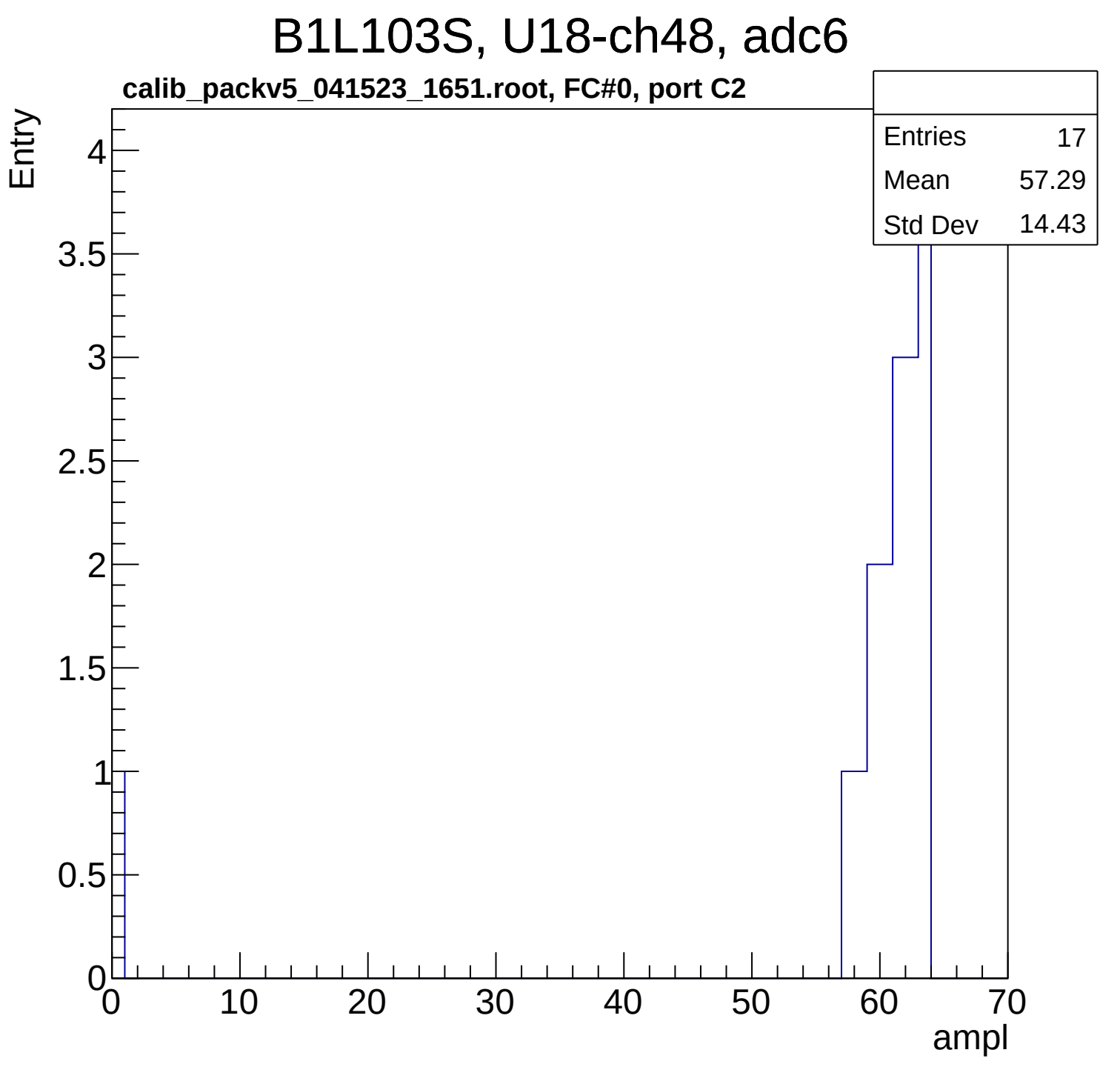
B1L103S, U18-ch48, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 17
Mean 57.29
Std Dev 14.43
Entry
ampl
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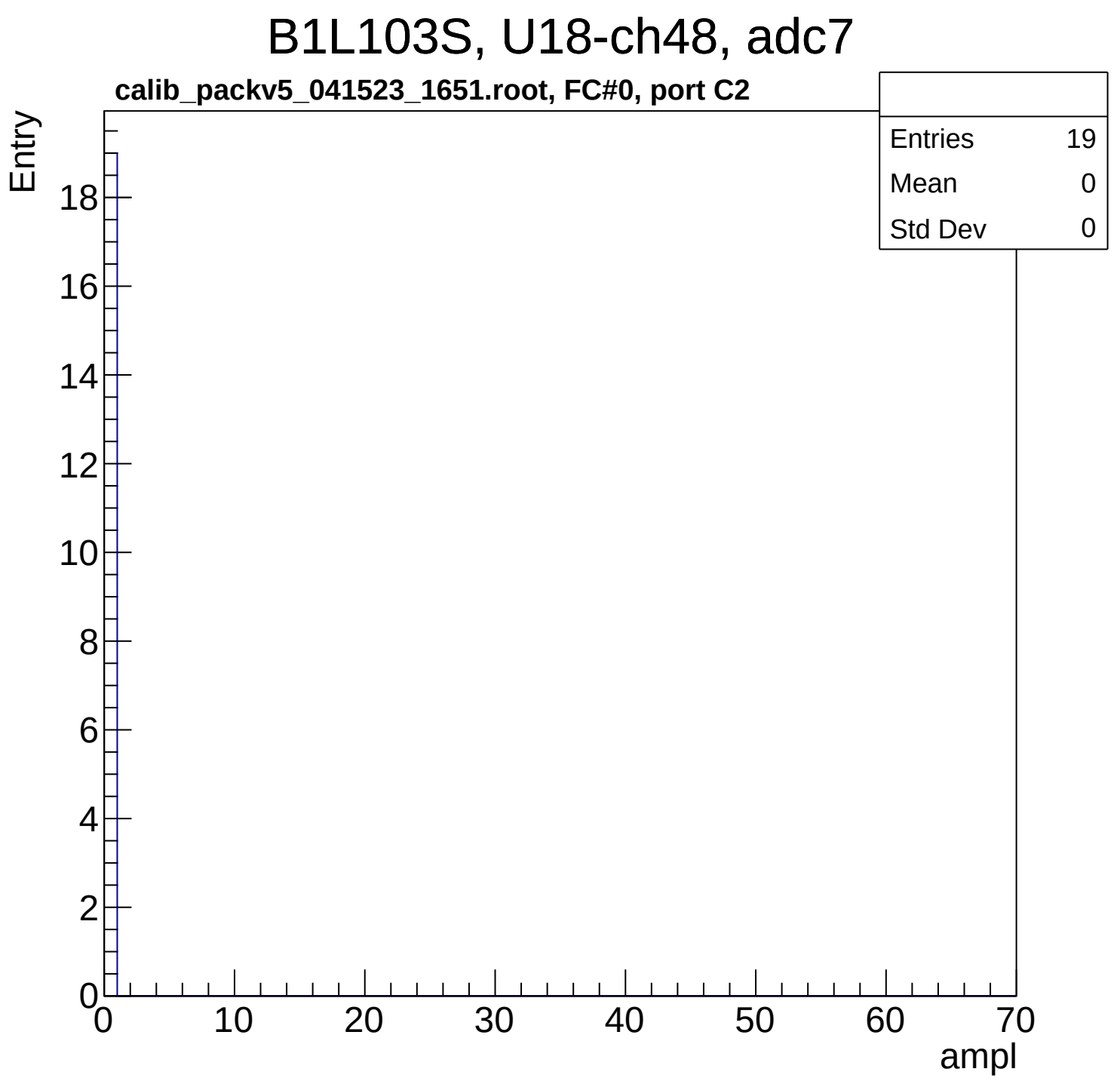
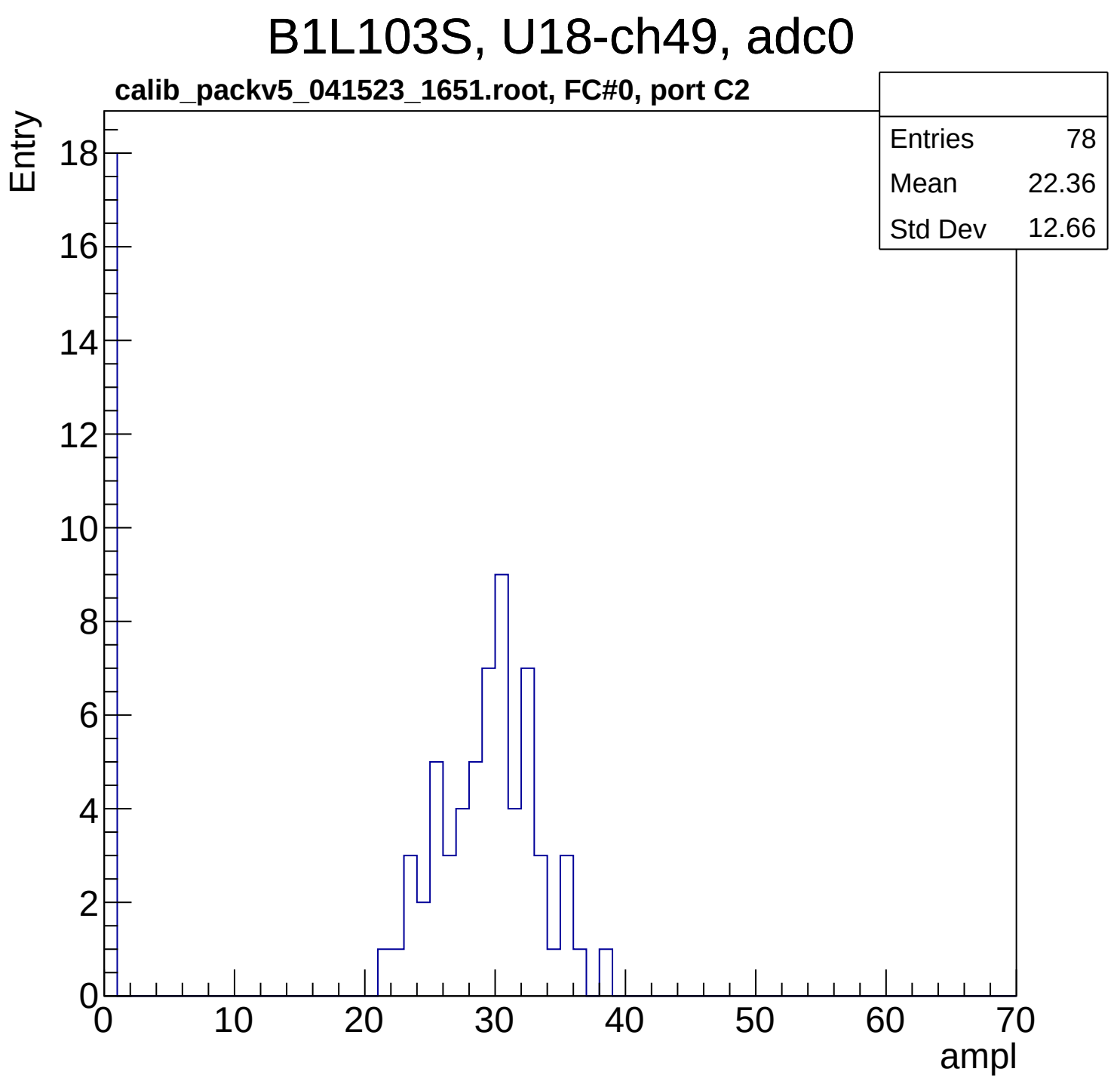
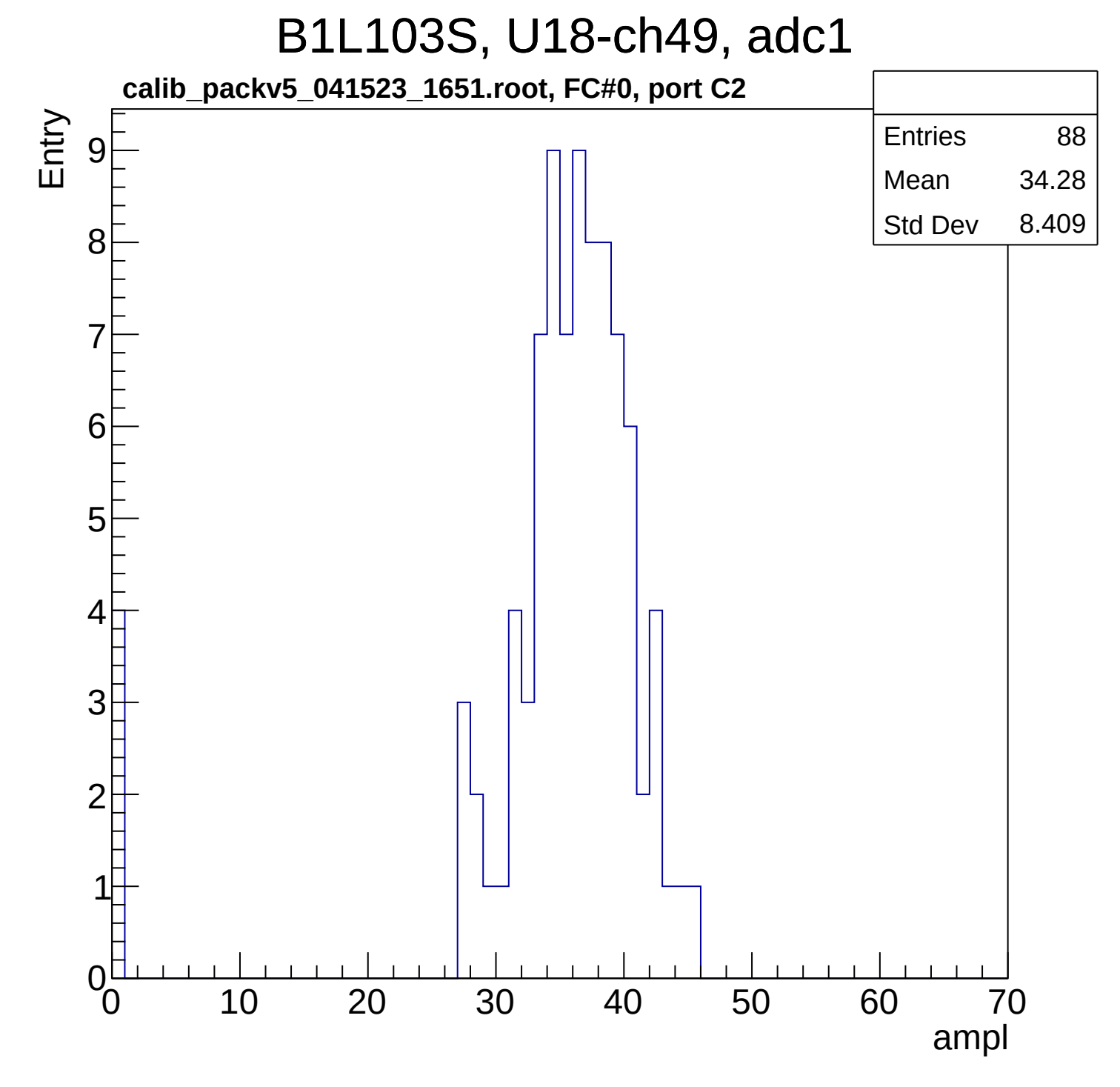
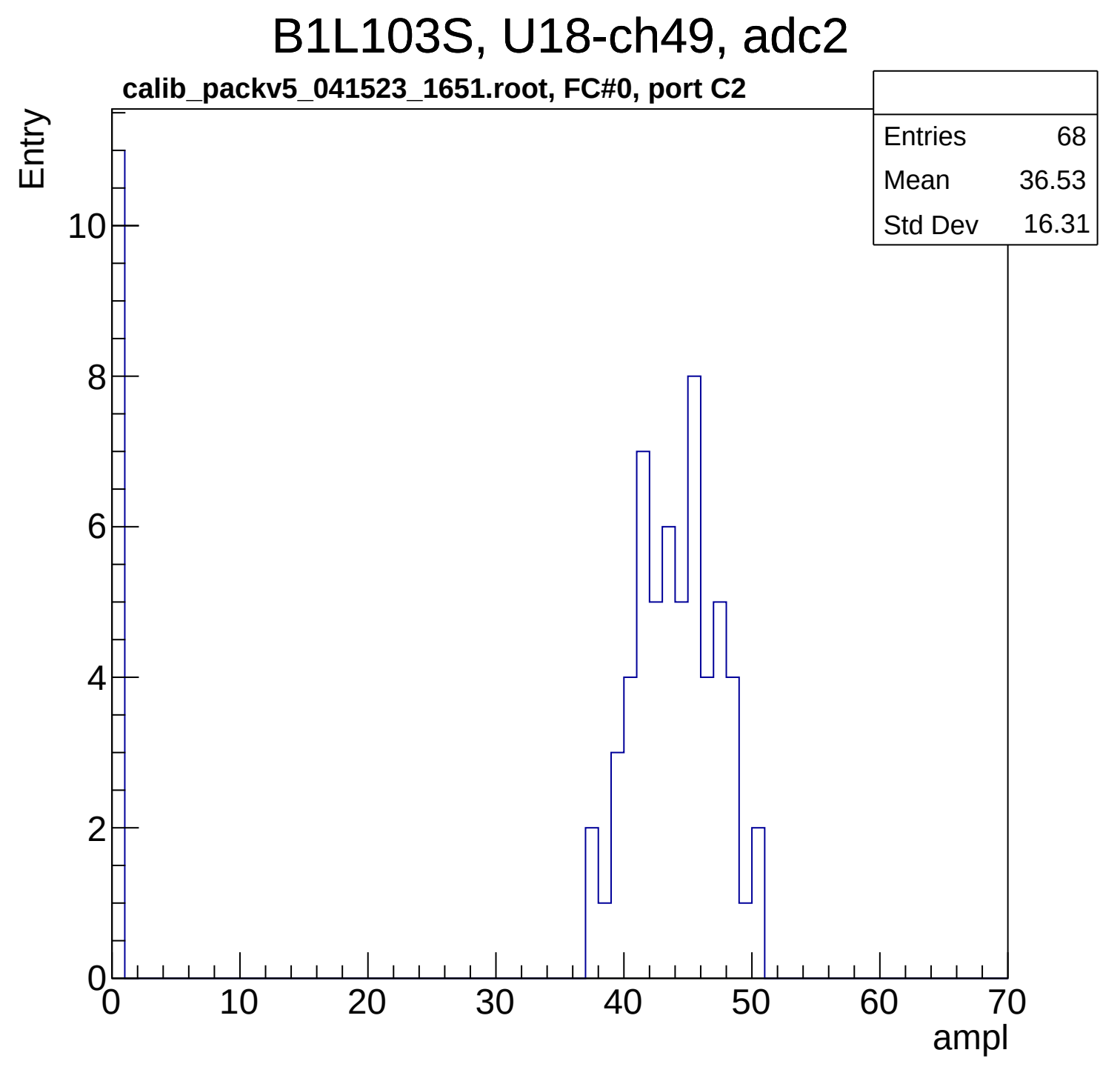
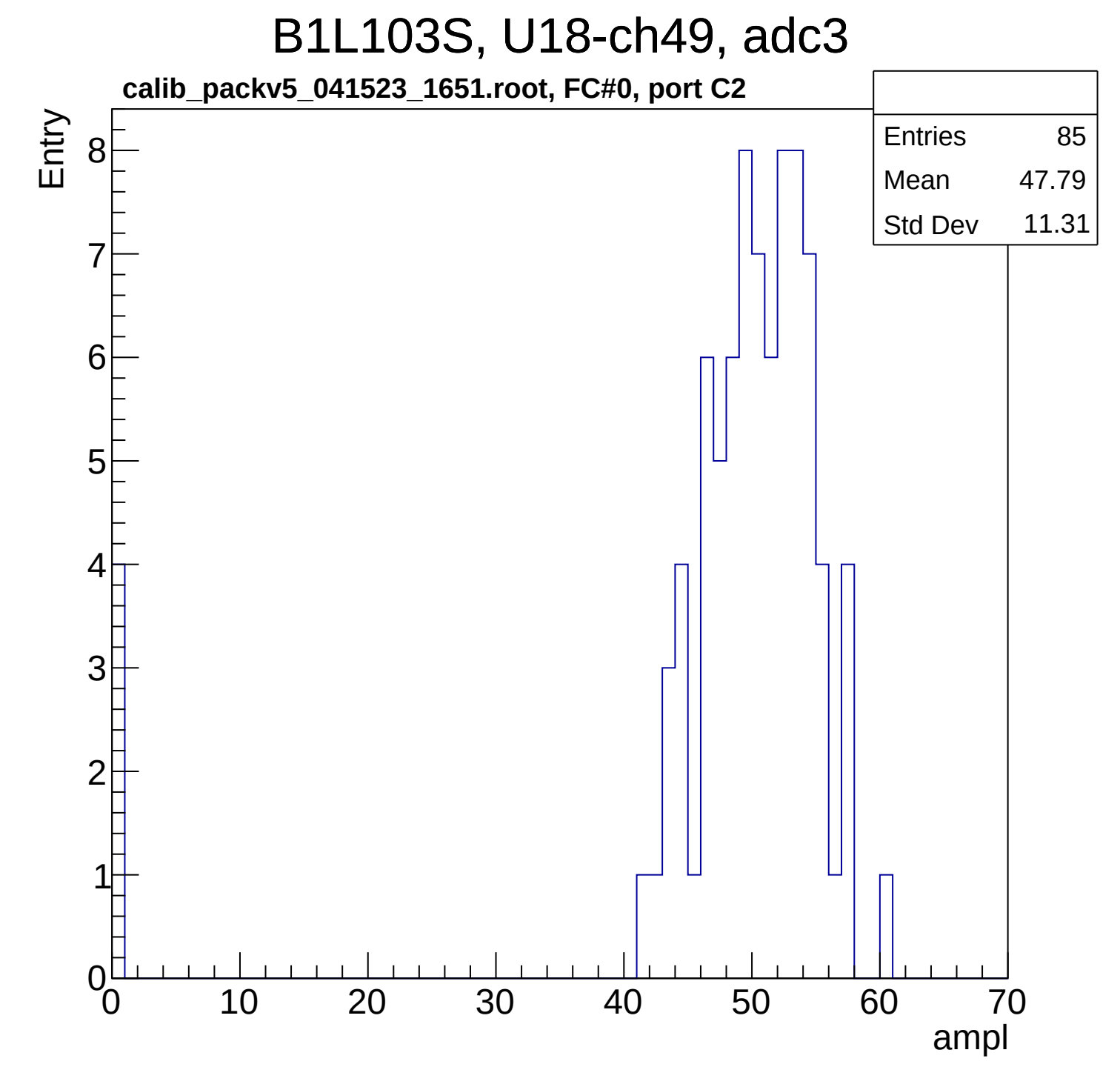
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U18-ch48, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch49, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 22.36
Std Dev 12.66
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch49, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 88
Mean 34.28
Std Dev 8.409
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U18-ch49, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 36.53
Std Dev 16.31
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U18-ch49, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 47.79
Std Dev 11.31
Entry
ampl
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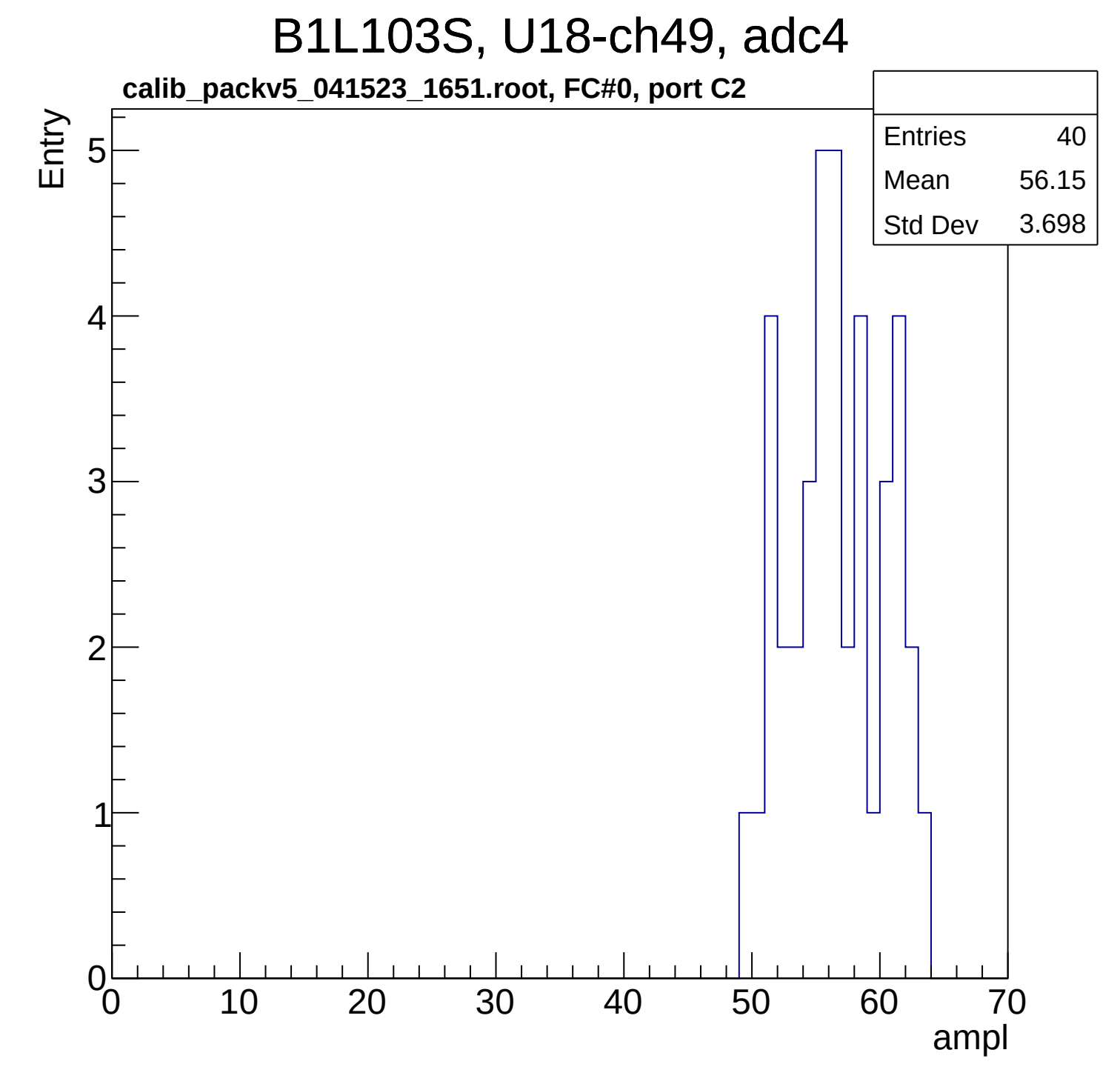
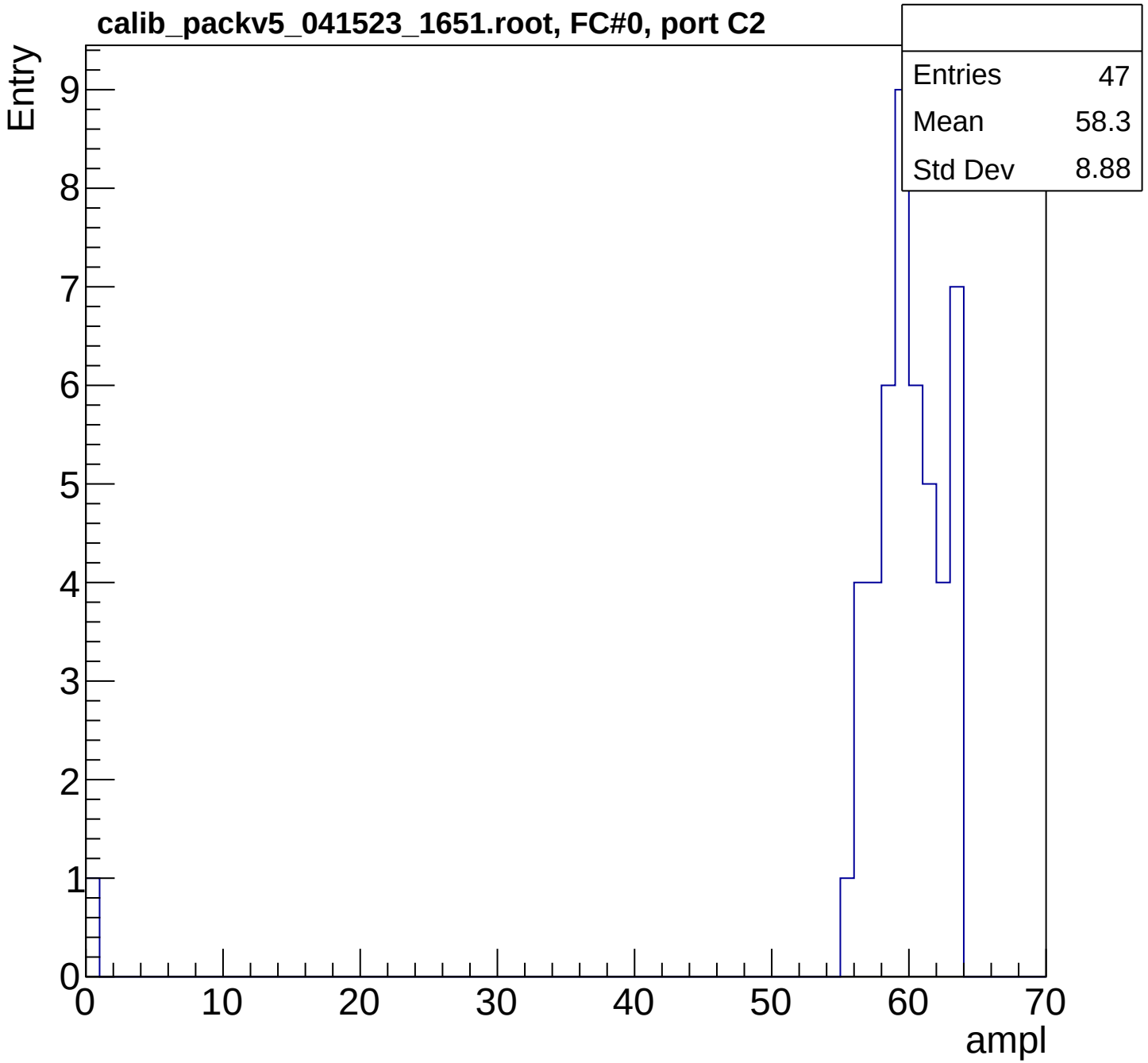
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch49, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 40
Mean 56.15
Std Dev 3.698
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch49, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 58.3
Std Dev 8.88
Entry
ampl
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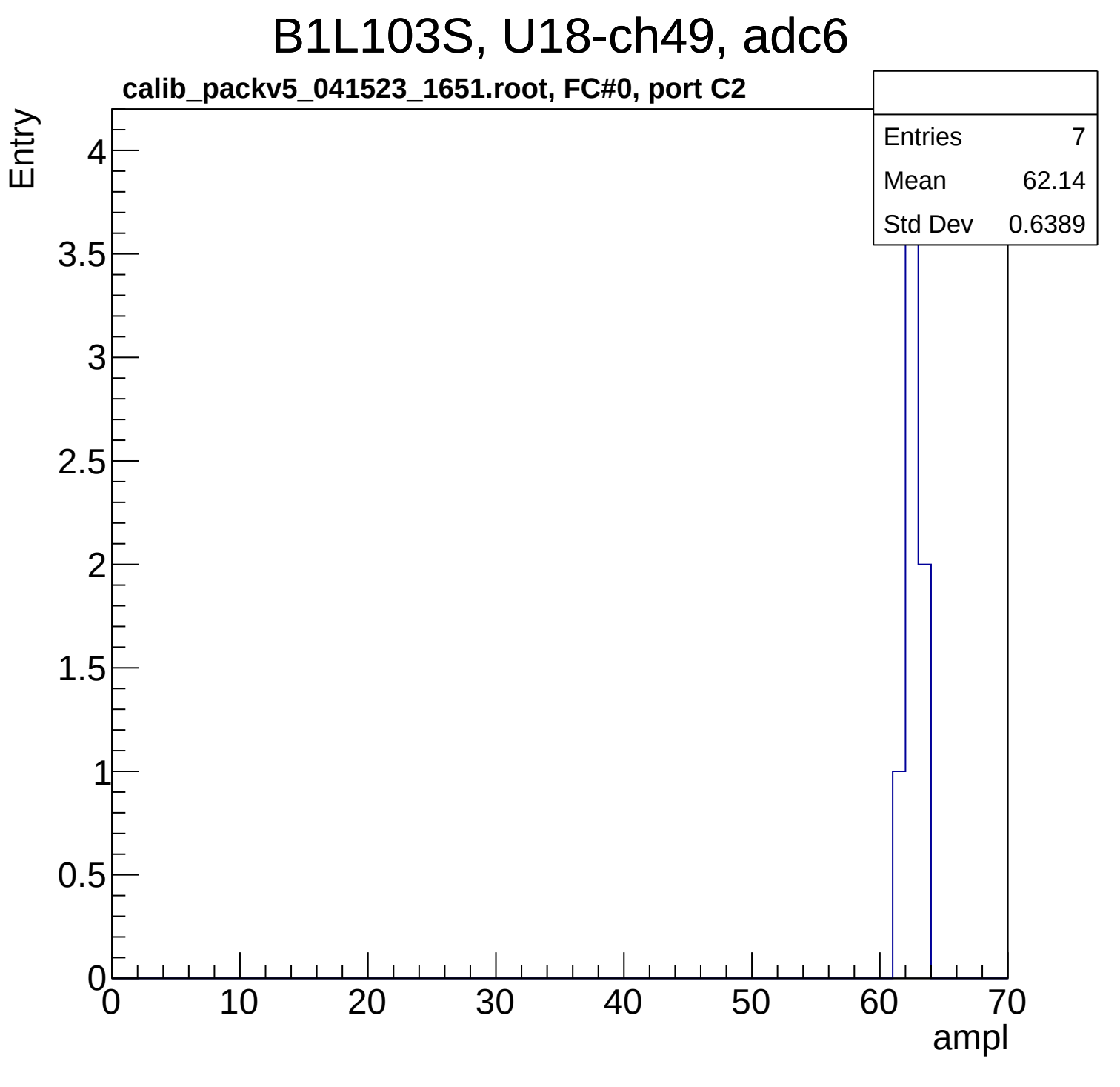
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U18-ch49, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 62.14
Std Dev 0.6389
Entry
ampl
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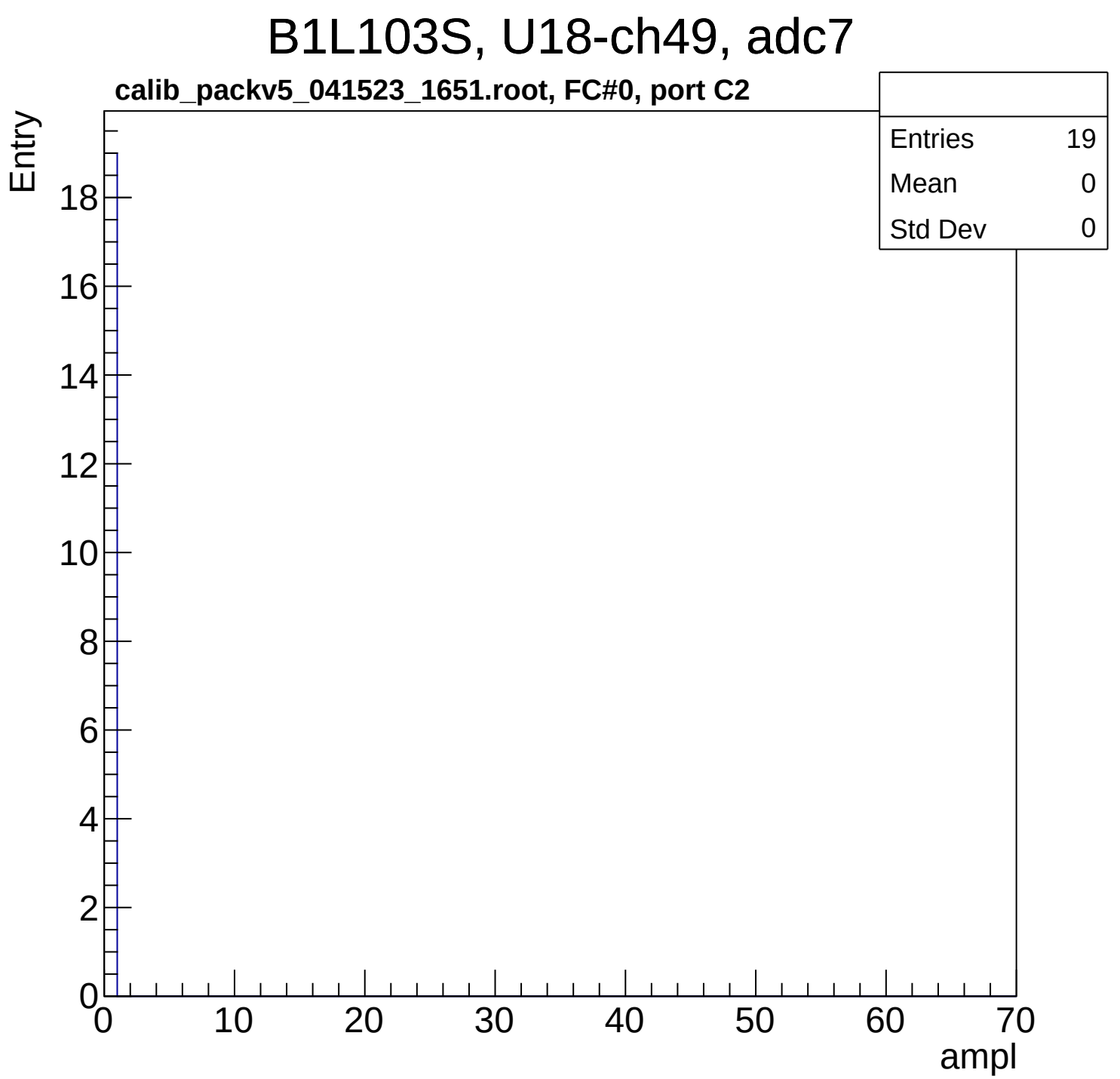
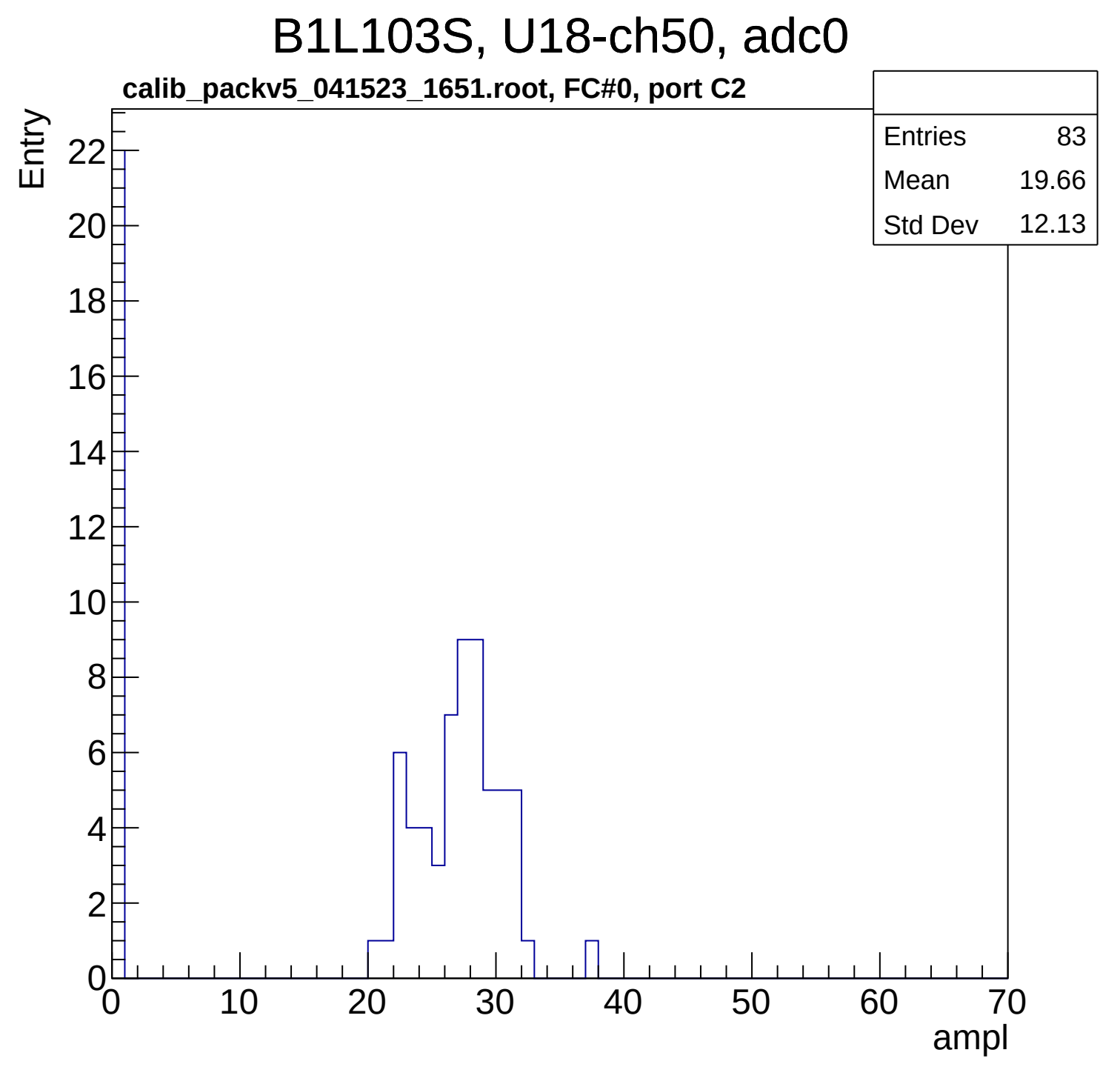
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U18-ch49, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch50, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 19.66
Std Dev 12.13
Entry
ampl
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2
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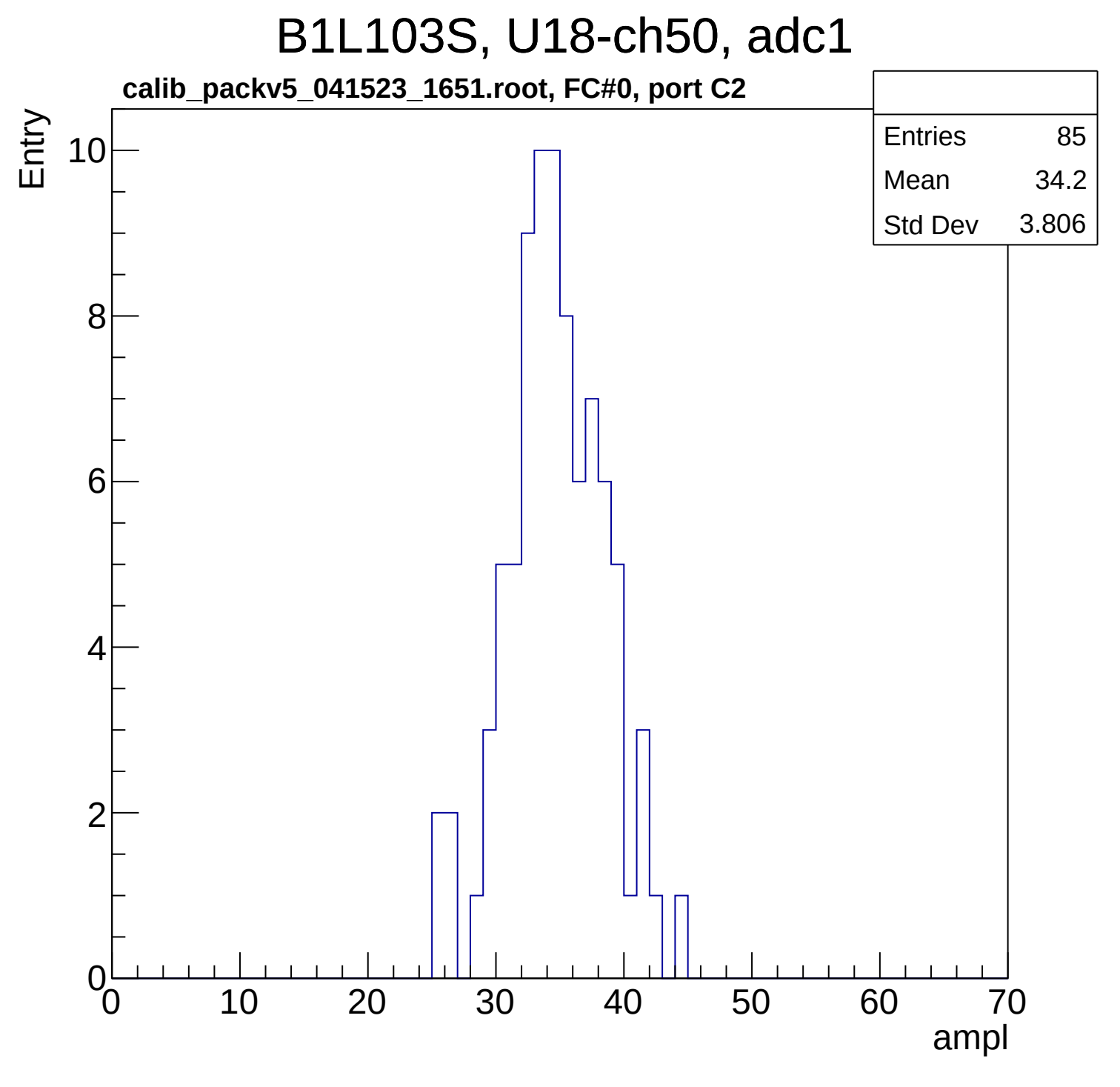
8
10
12
14
16
18
20
22
0
10
20
30
40
50
60
70


B1L103S, U18-ch50, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 34.2
Std Dev 3.806
Entry
ampl
0
2
4
6
8
10
0
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20
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40
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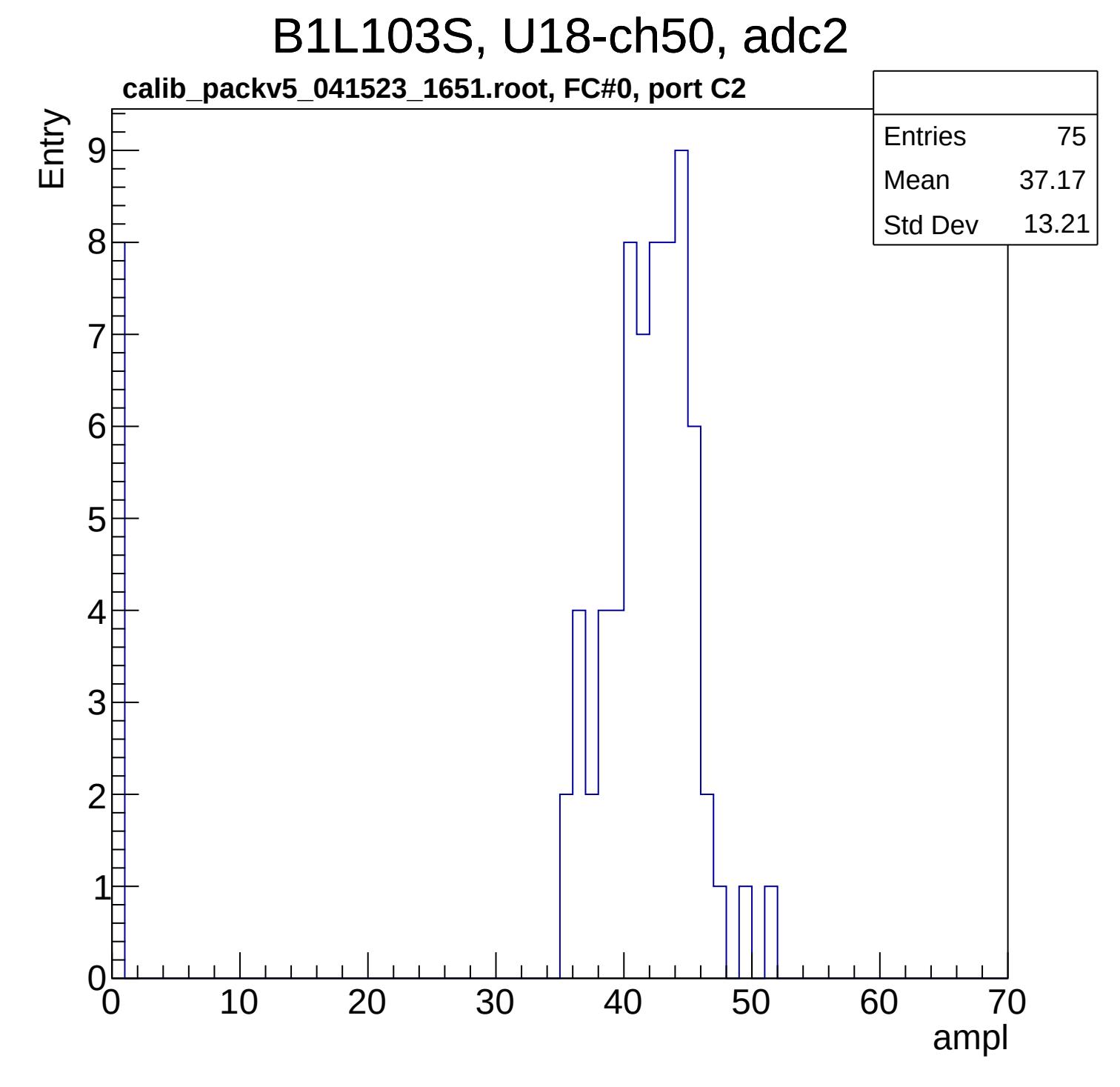
60
70


B1L103S, U18-ch50, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 37.17
Std Dev 13.21
Entry
ampl
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3
4
5
6
7
8
9
0
10
20
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40
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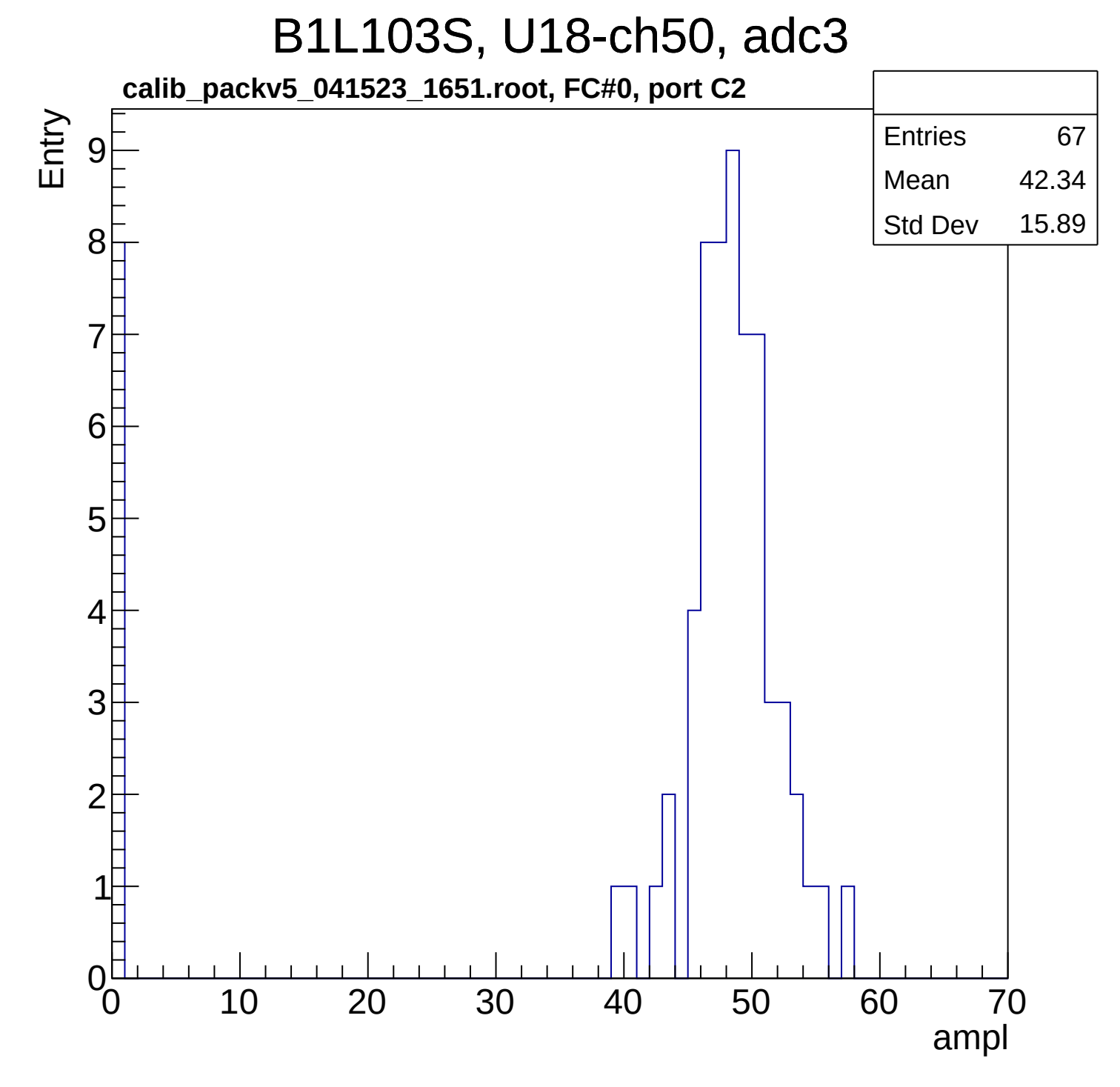
60
70


B1L103S, U18-ch50, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 42.34
Std Dev 15.89
Entry
ampl
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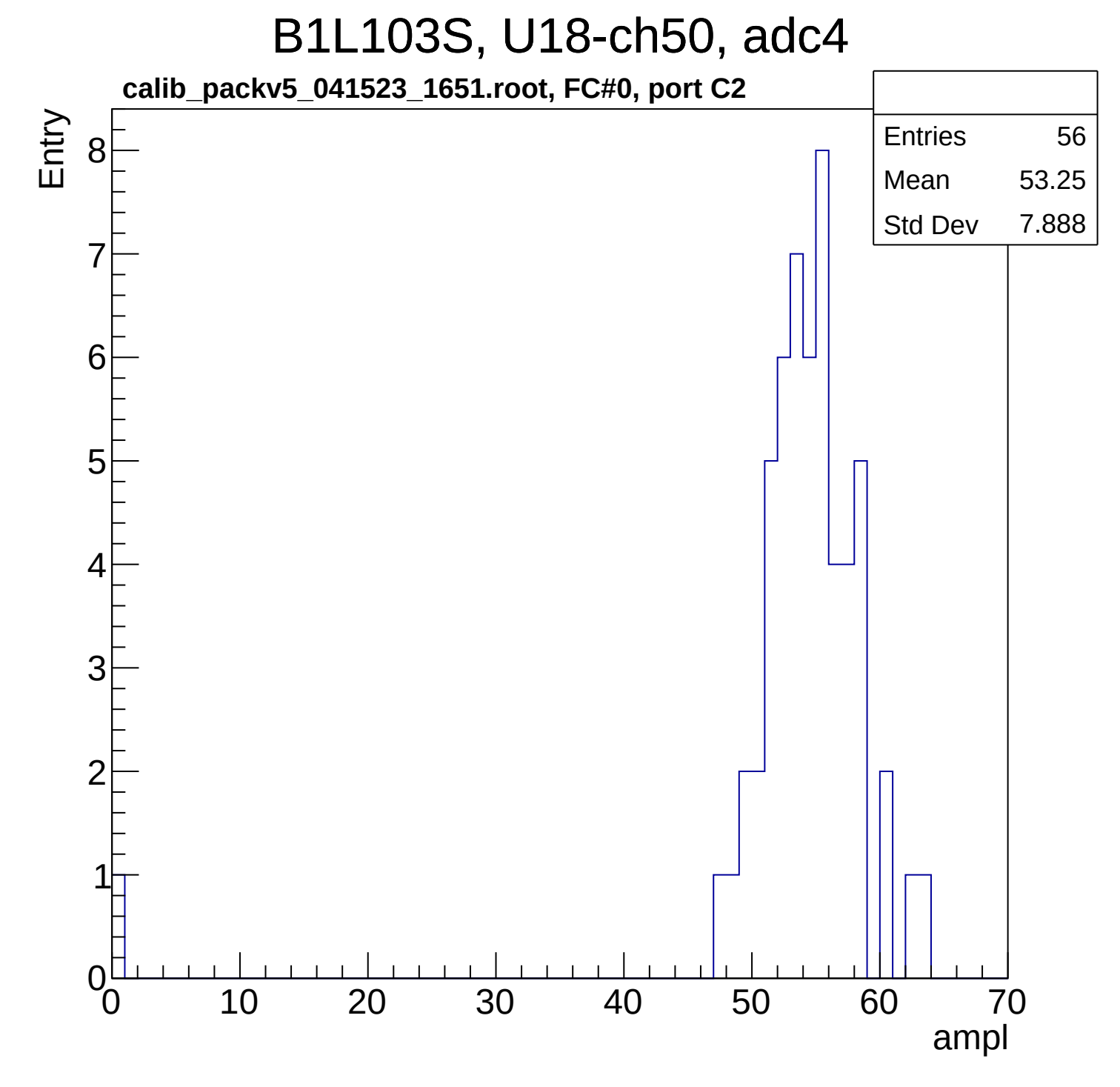
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U18-ch50, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 53.25
Std Dev 7.888
Entry
ampl
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2
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4
5
6
7
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0
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20
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60
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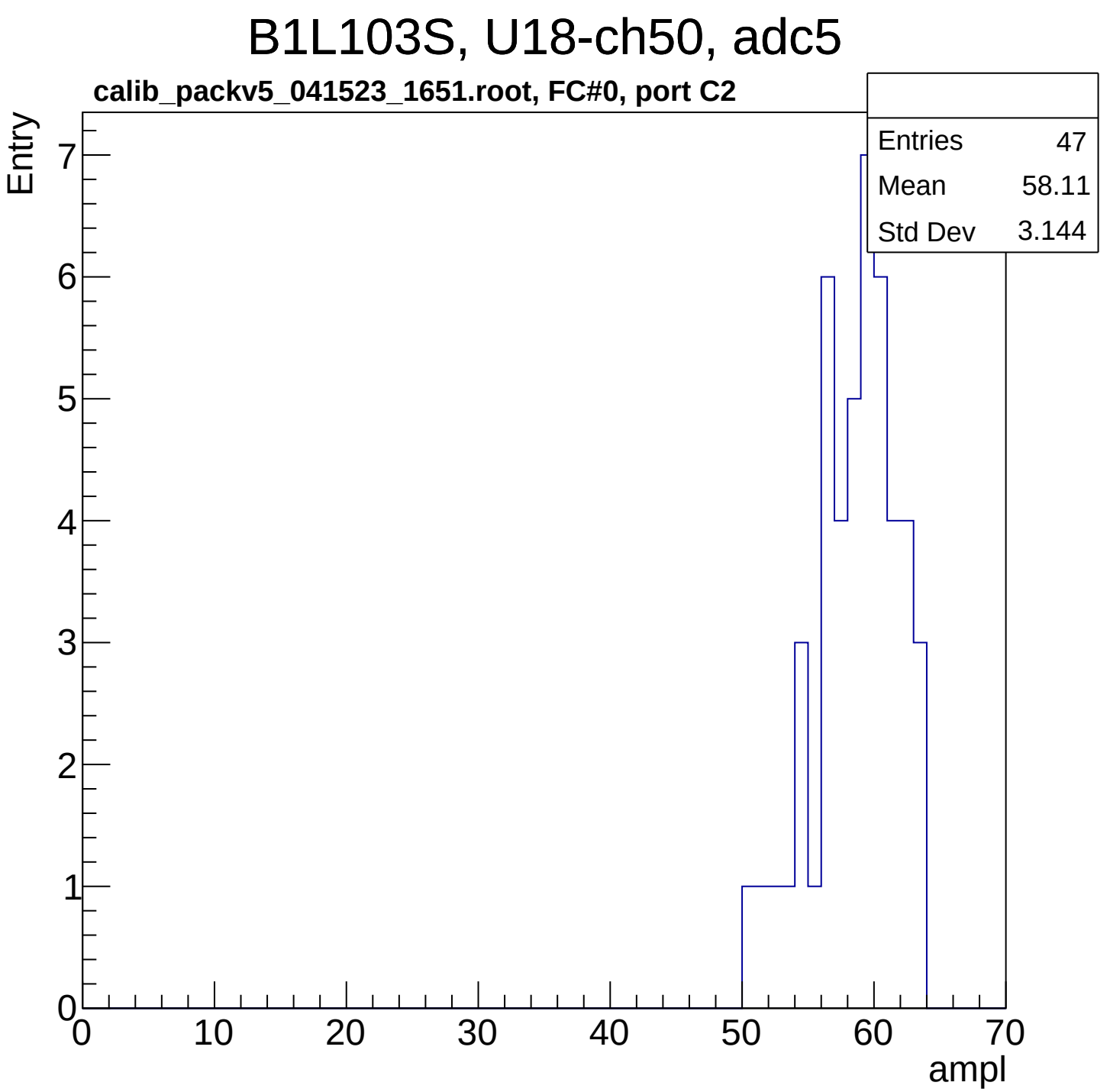
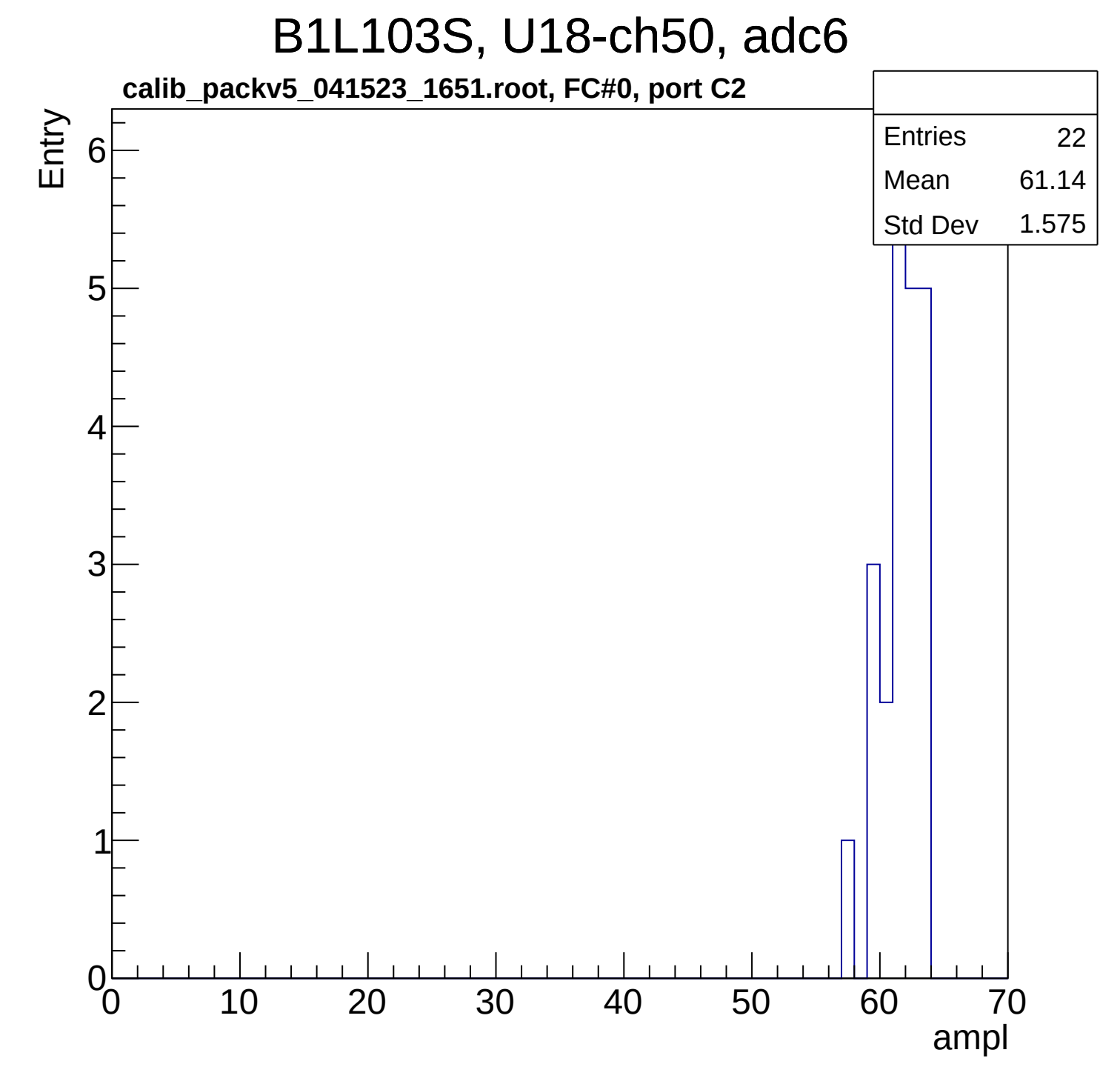

B1L103S, U18-ch50, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 58.11
Std Dev 3.144
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U18-ch50, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 61.14
Std Dev 1.575
Entry
ampl
0
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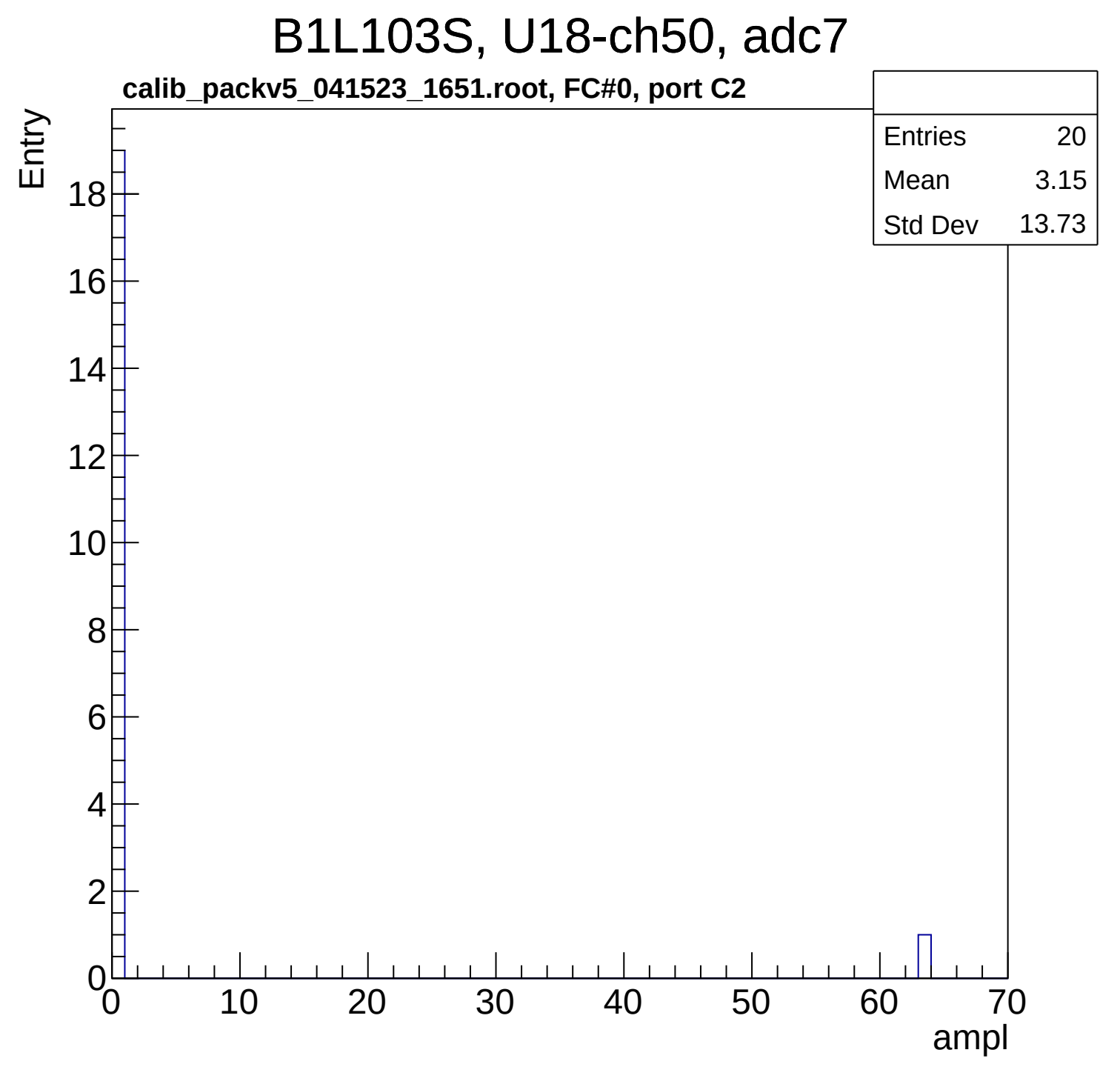
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U18-ch50, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
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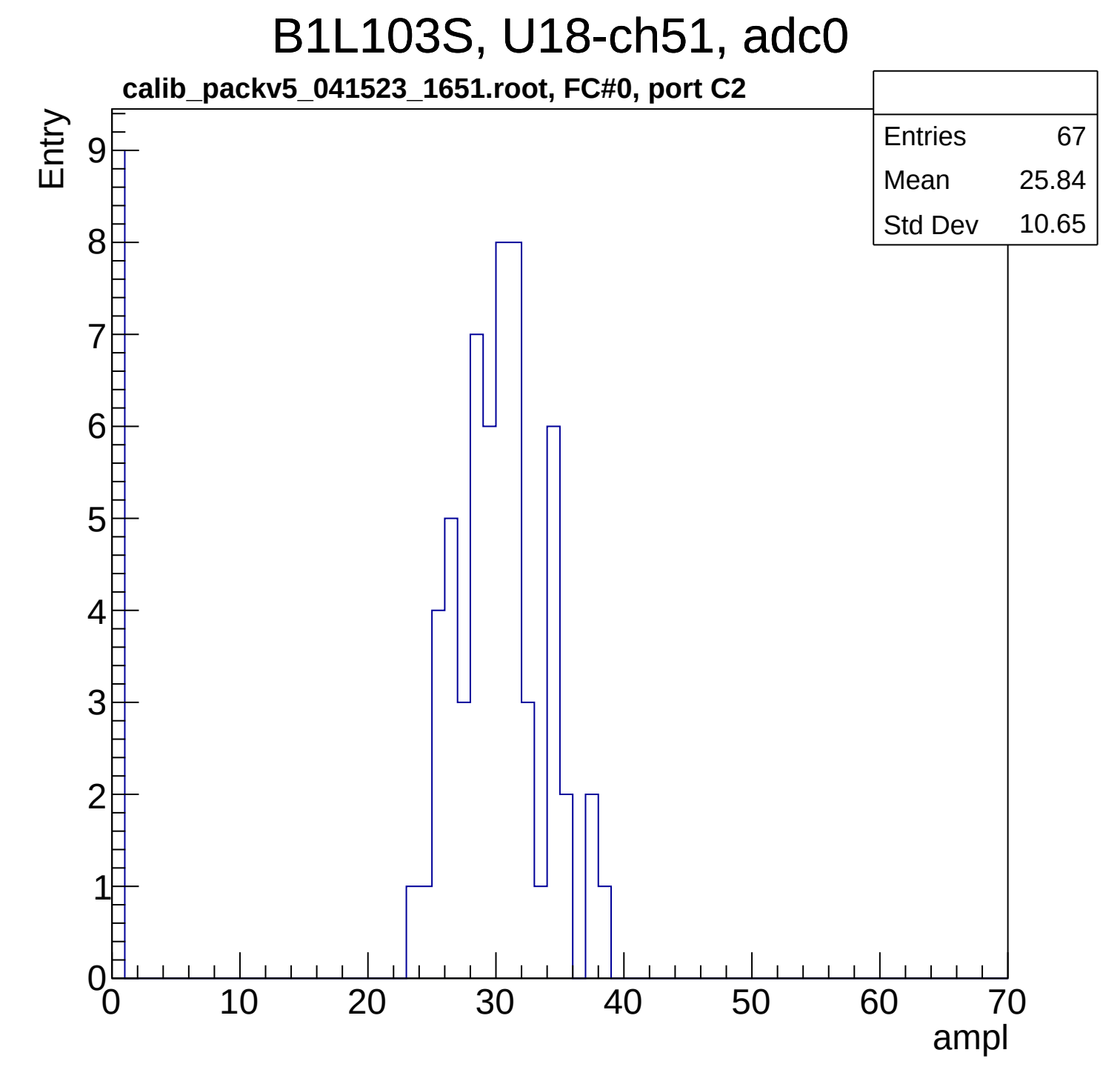
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch51, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 25.84
Std Dev 10.65
Entry
ampl
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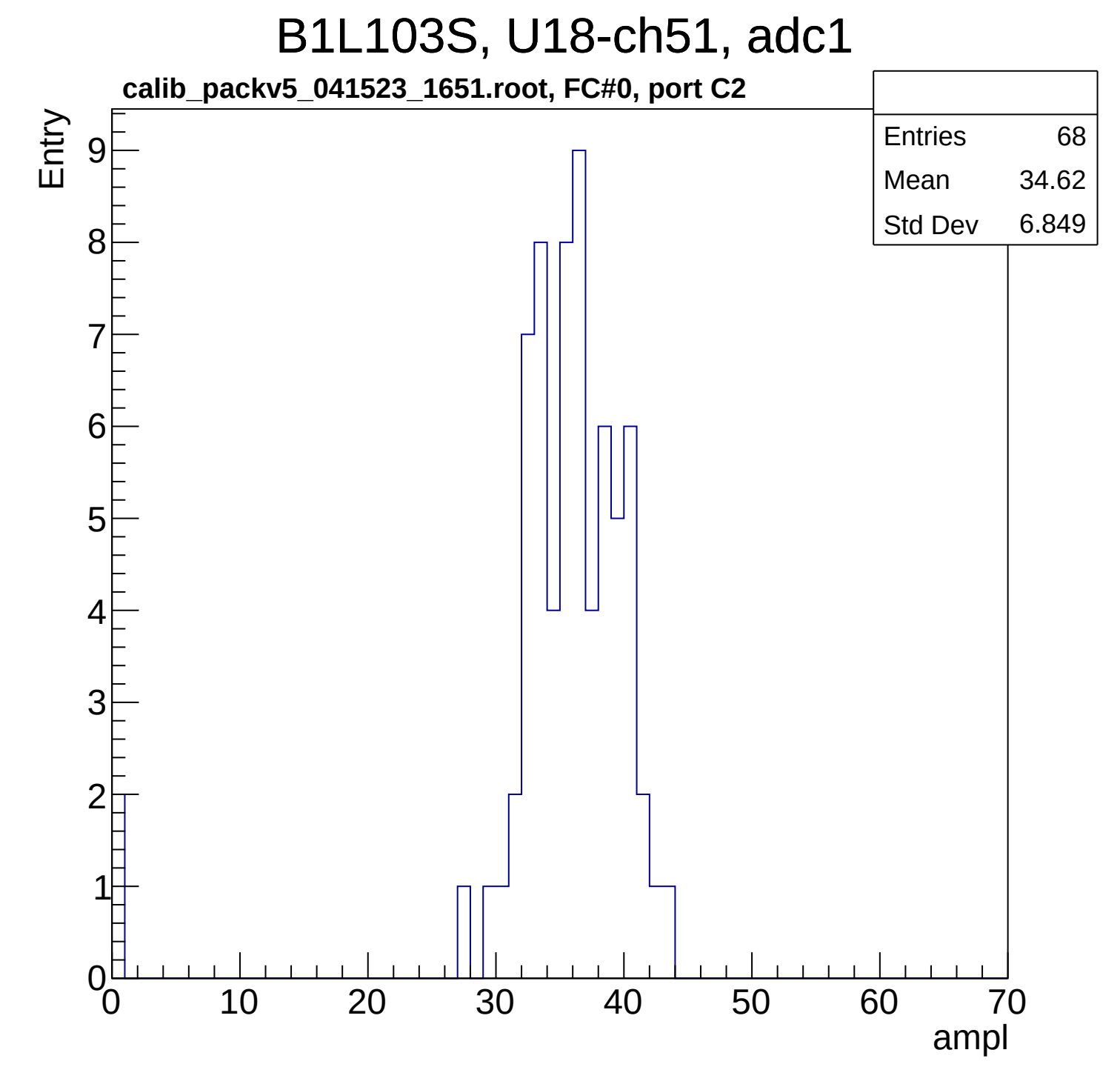
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U18-ch51, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 34.62
Std Dev 6.849
Entry
ampl
0
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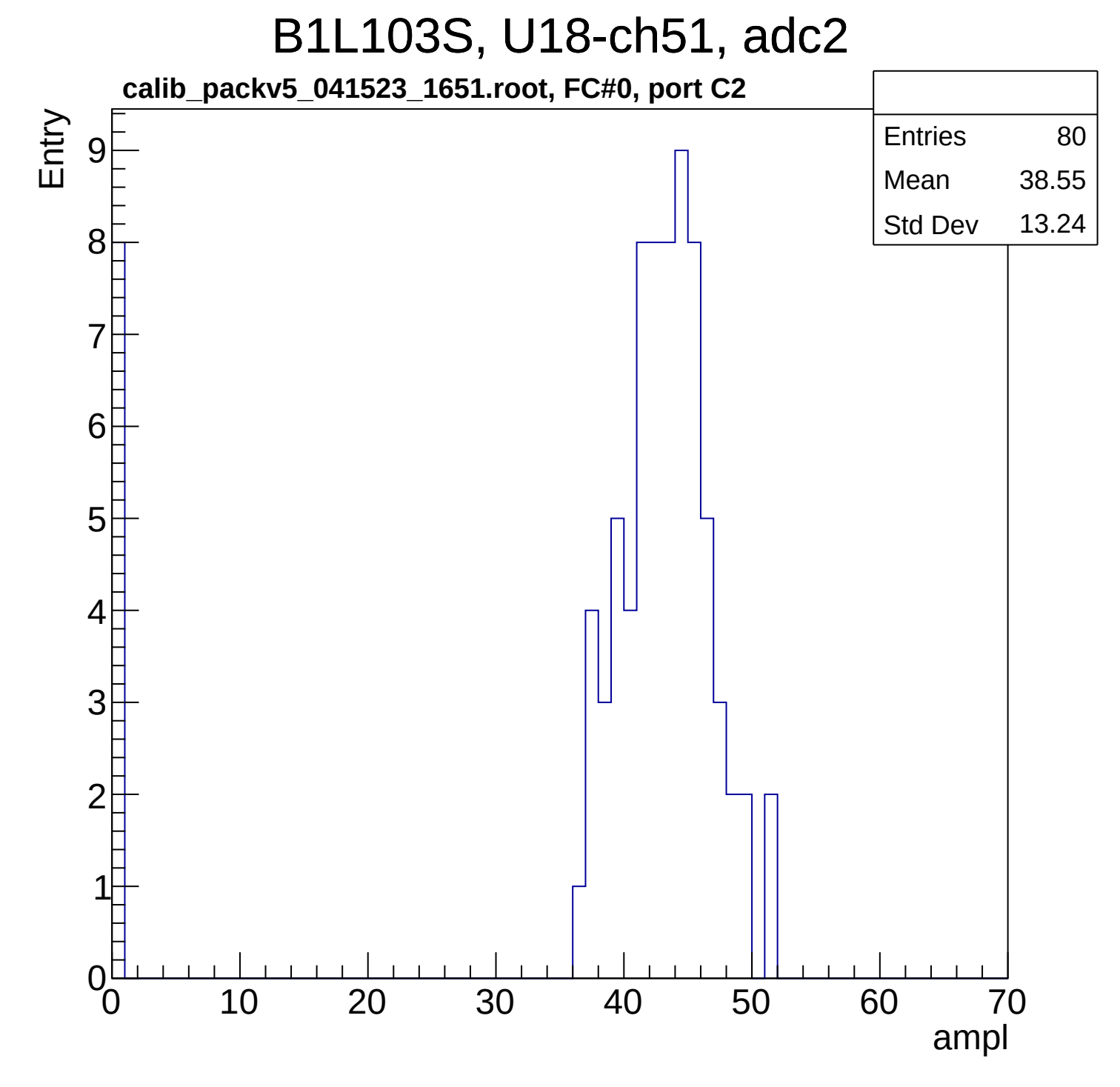
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U18-ch51, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 38.55
Std Dev 13.24
Entry
ampl
0
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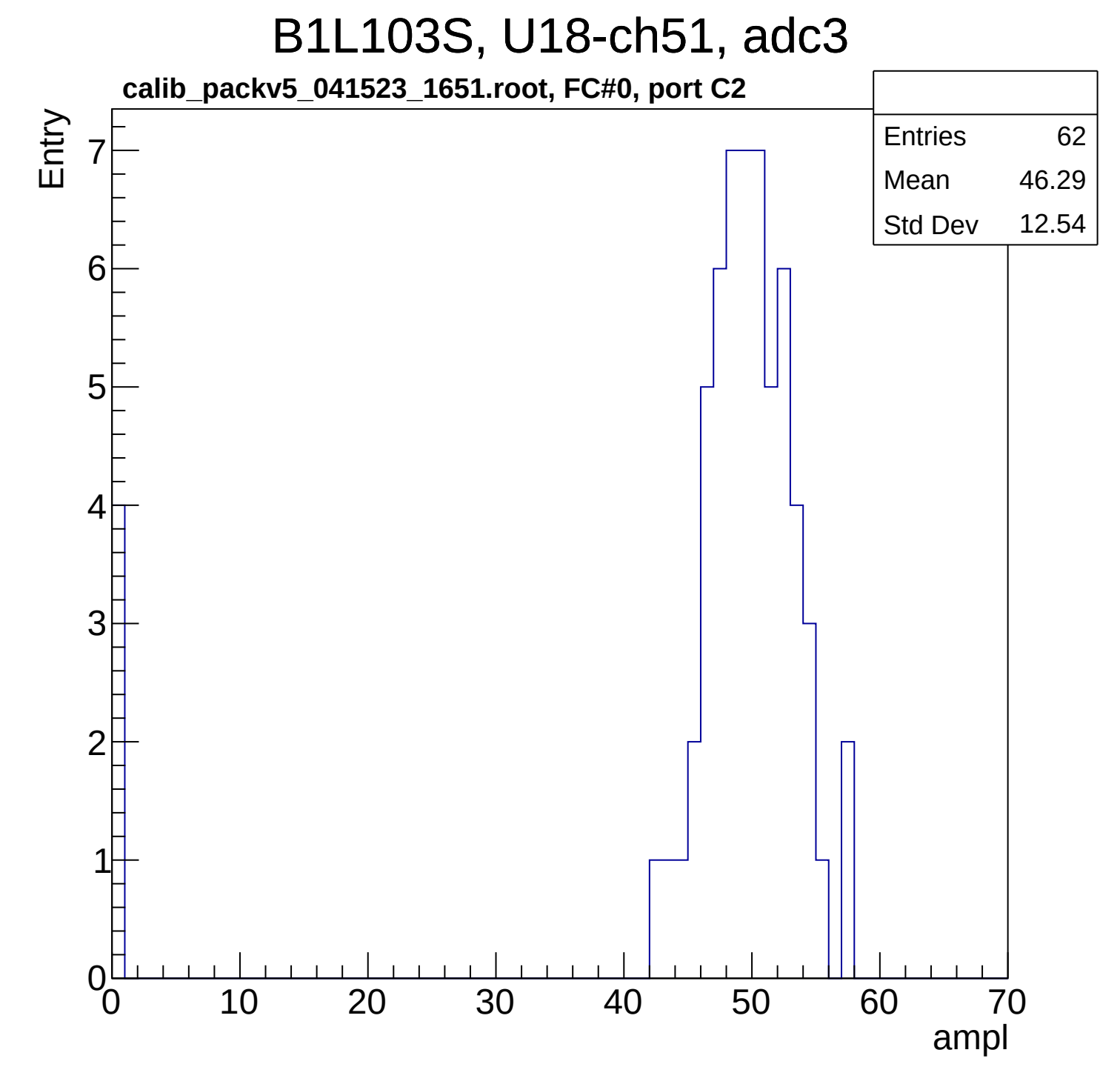
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U18-ch51, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 46.29
Std Dev 12.54
Entry
ampl
0
1
2
3
4
5
6
7
0
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20
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40
50
60
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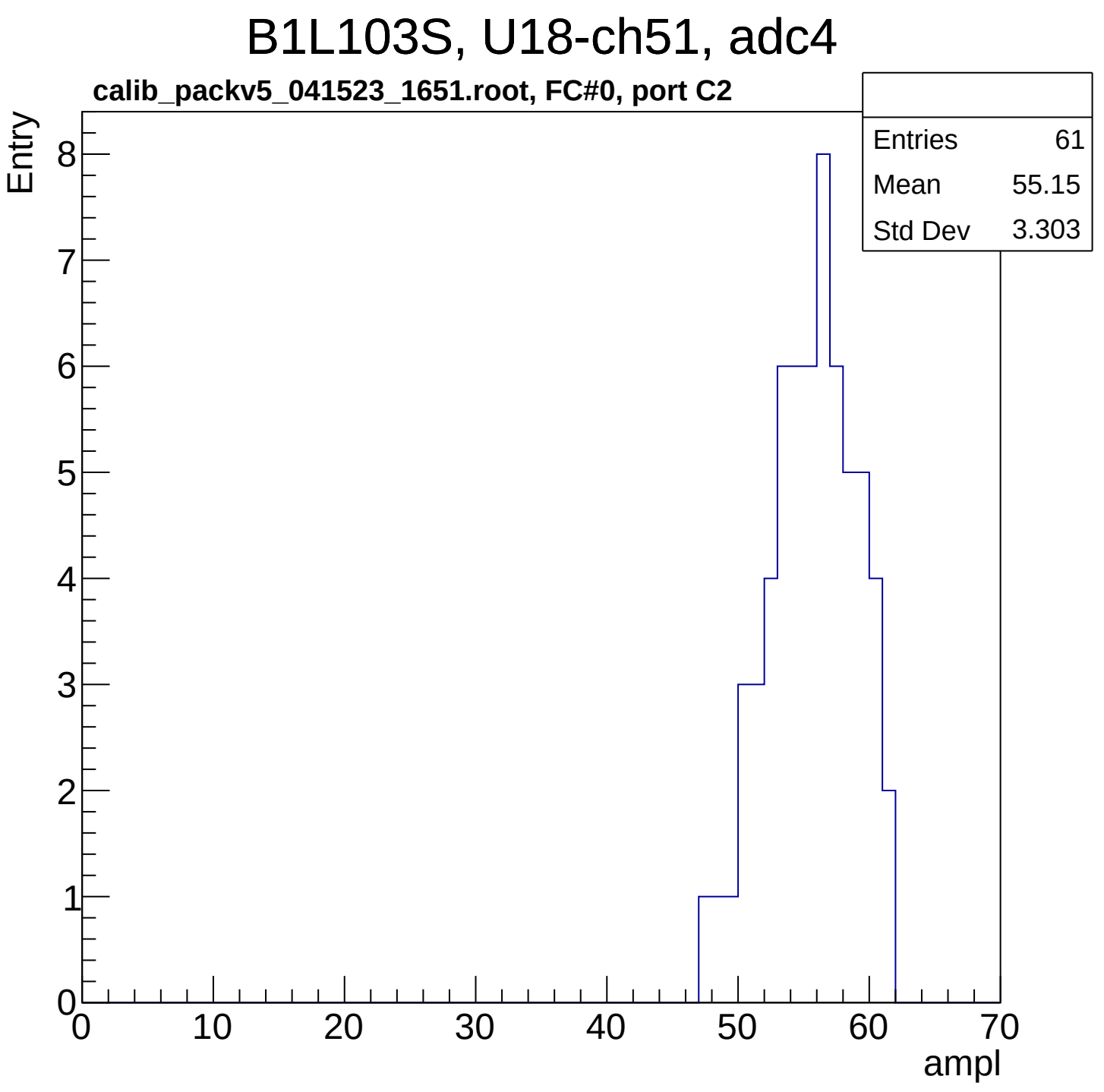
B1L103S, U18-ch51, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 55.15
Std Dev 3.303
Entry
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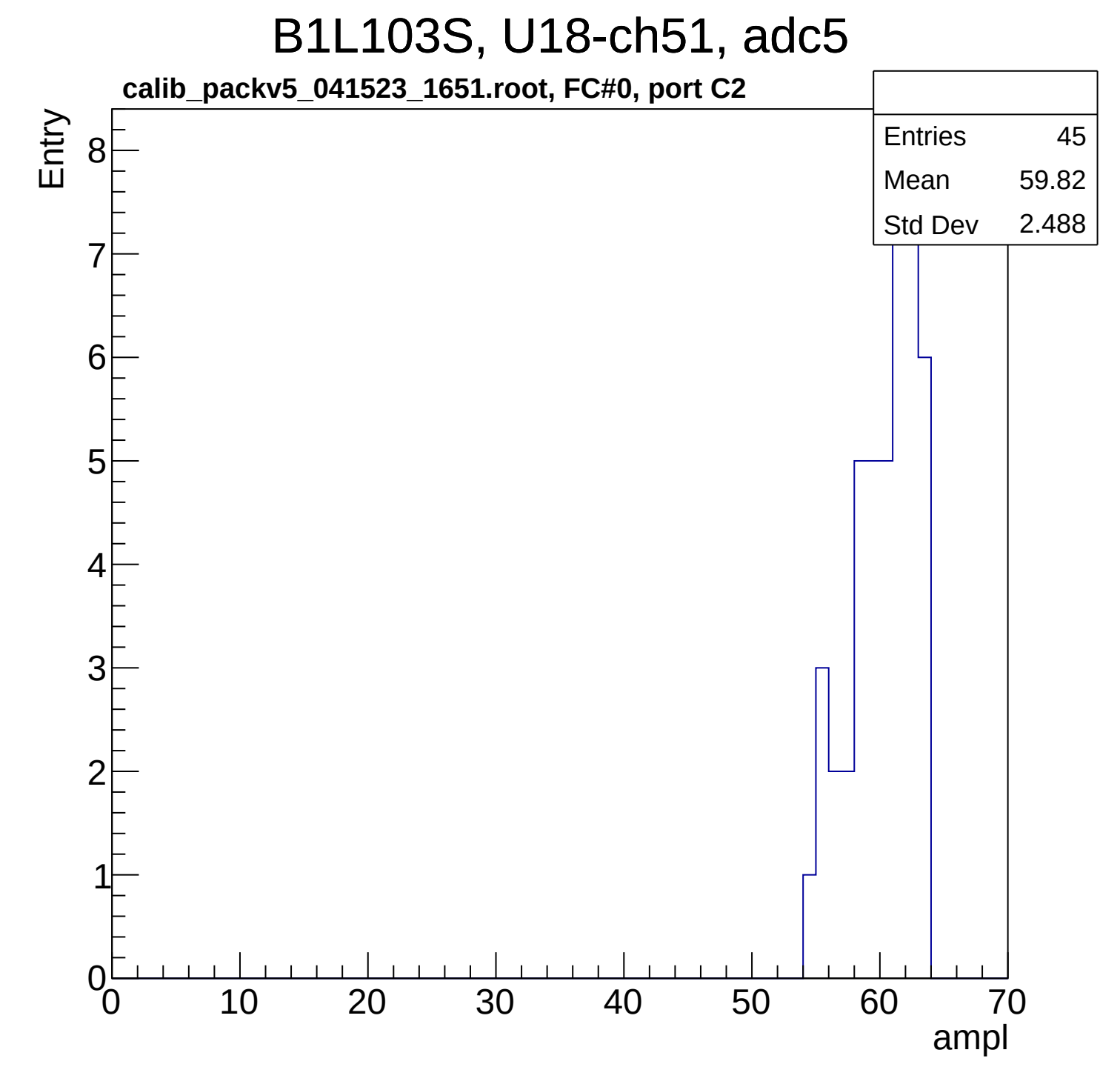
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch51, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 59.82
Std Dev 2.488
Entry
ampl
0
1
2
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4
5
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7
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0
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60
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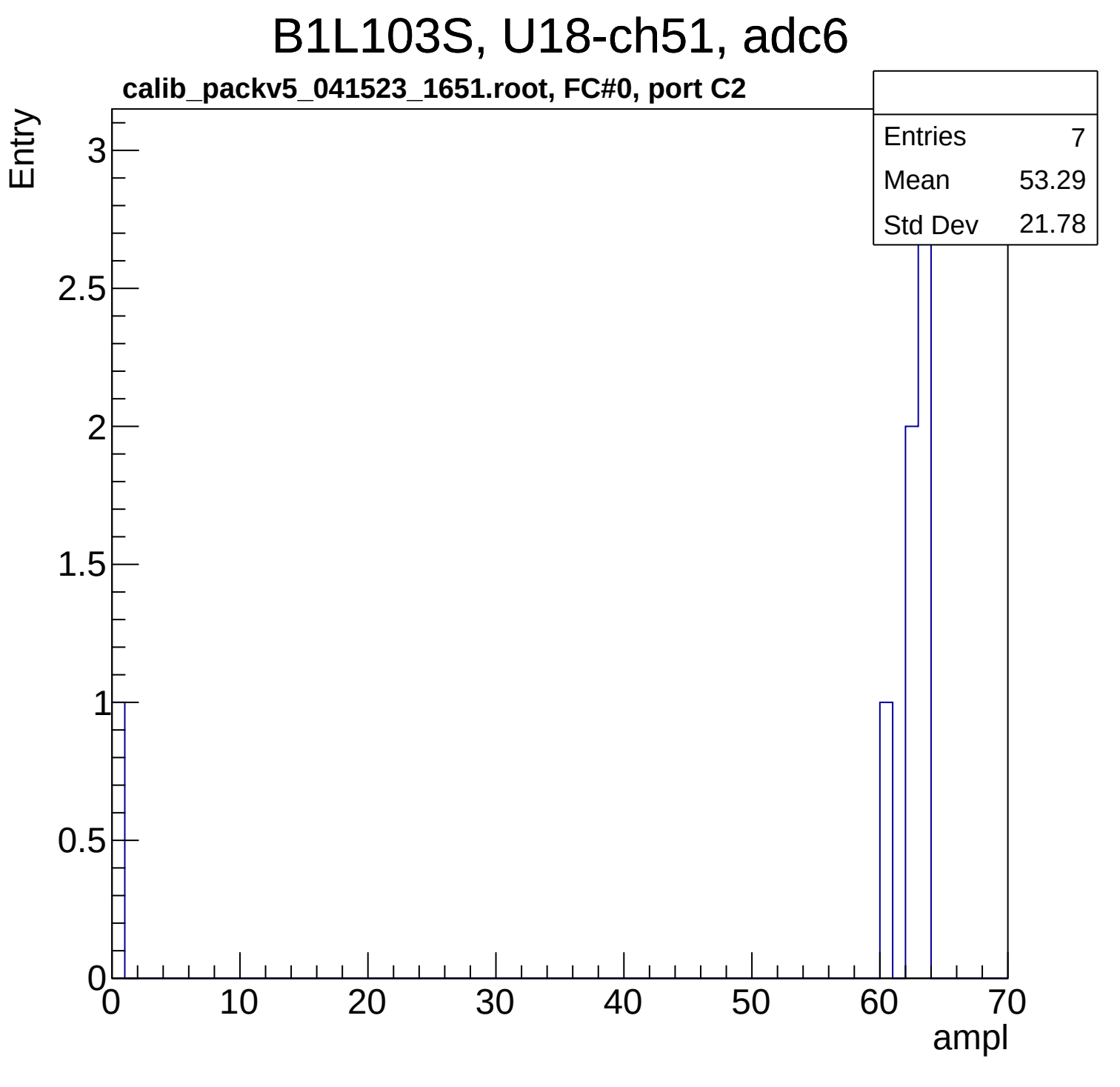
B1L103S, U18-ch51, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 53.29
Std Dev 21.78
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
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20
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40
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60
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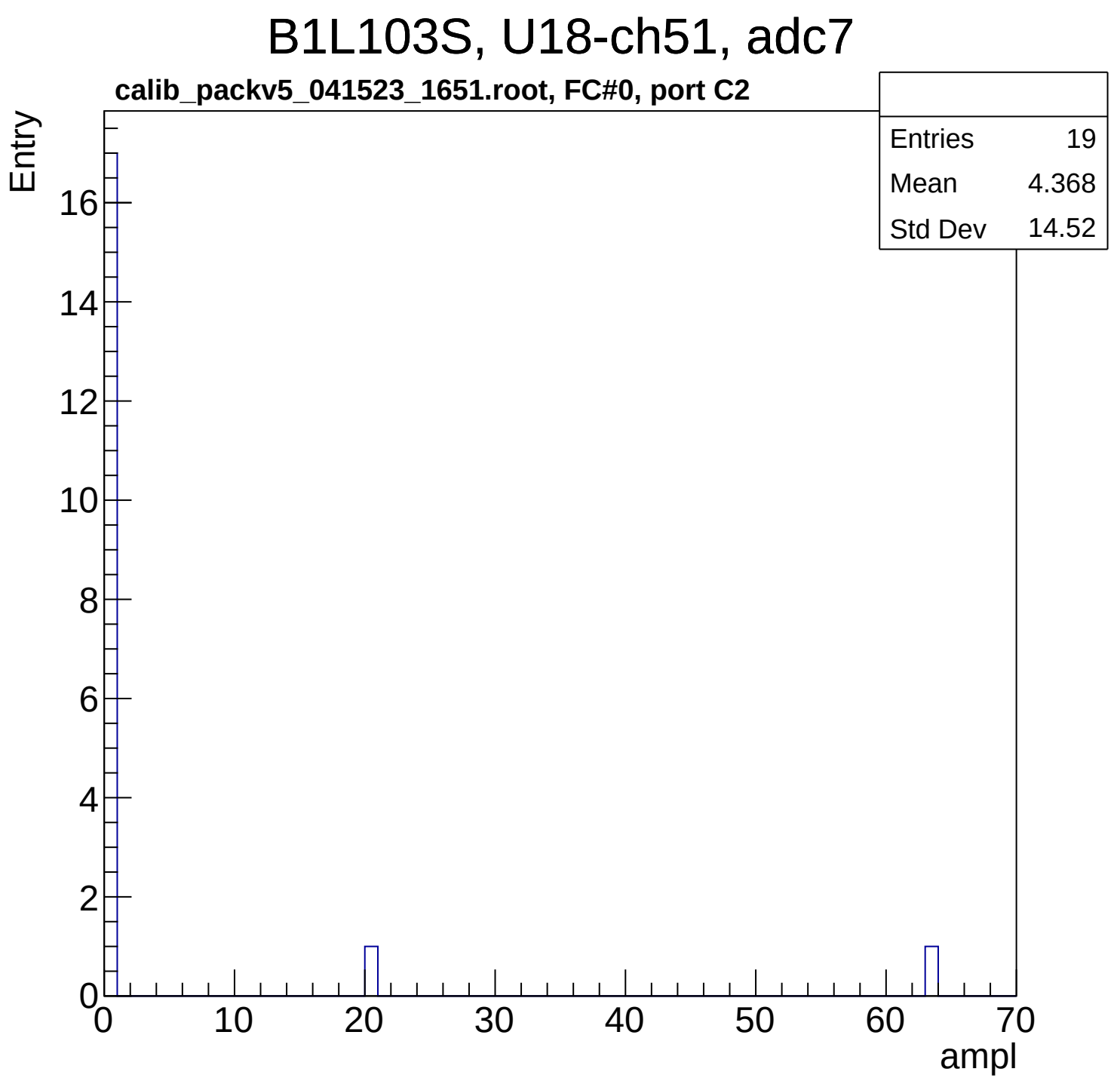
B1L103S, U18-ch51, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 4.368
Std Dev 14.52
Entry
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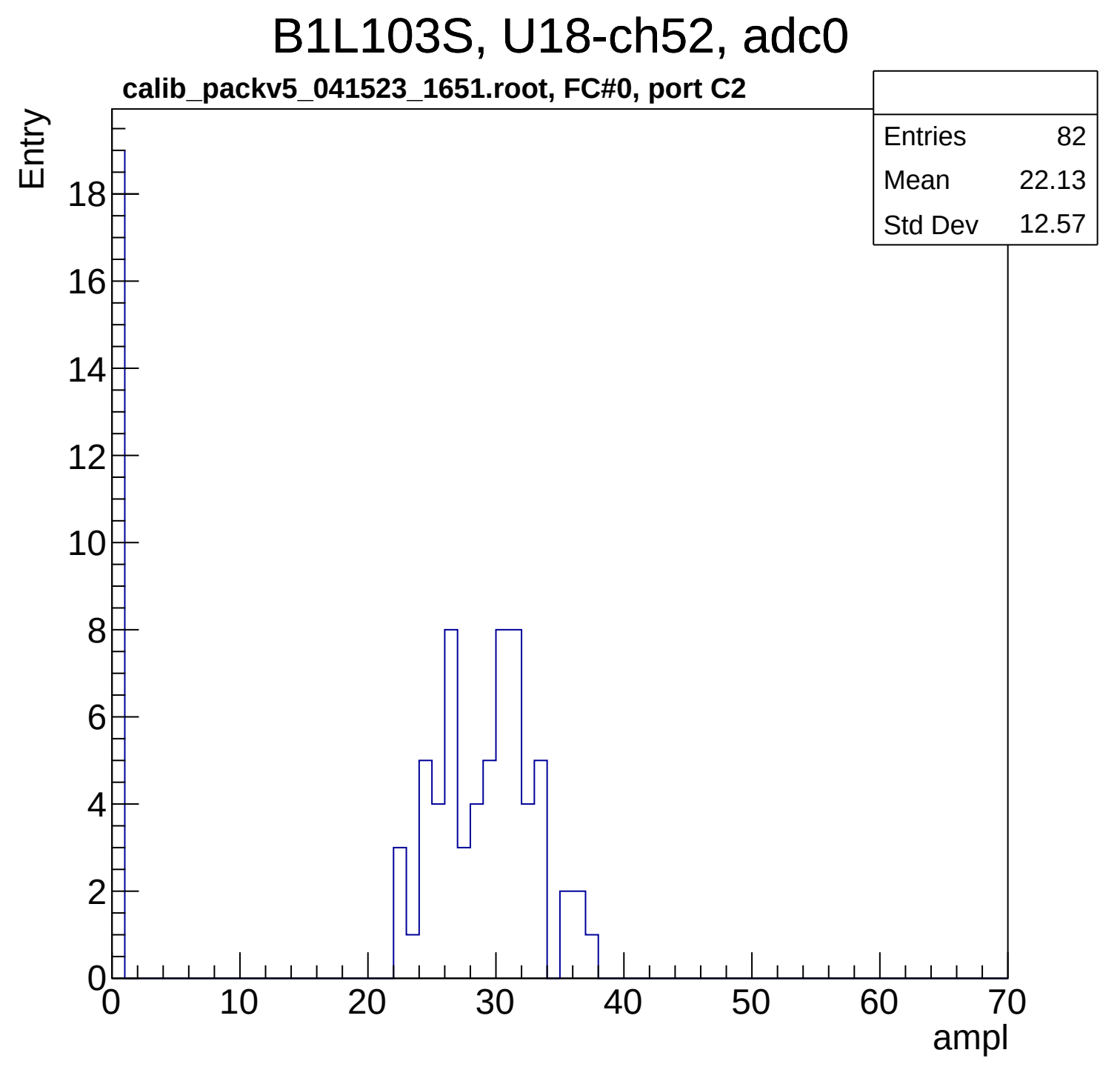
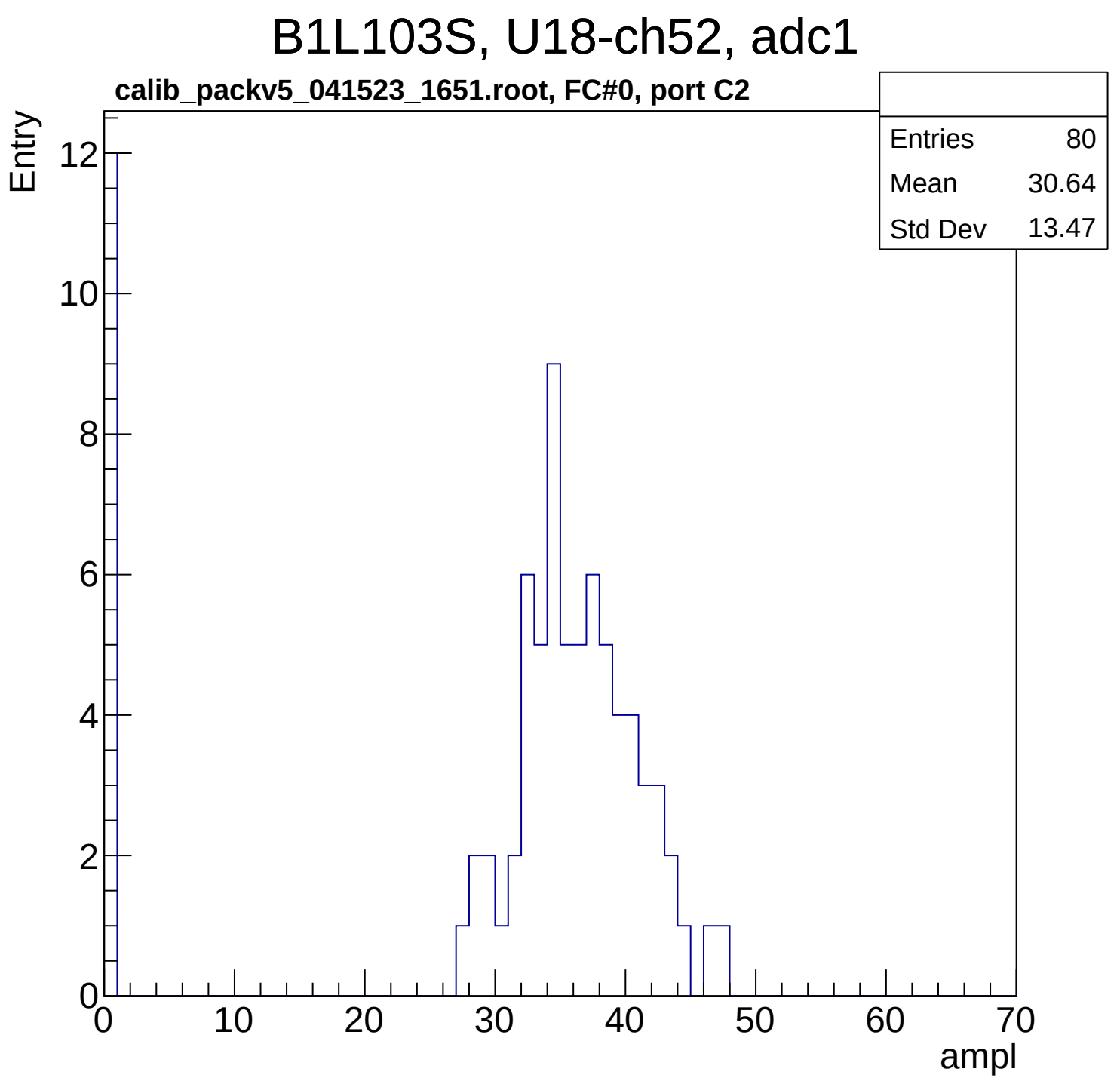
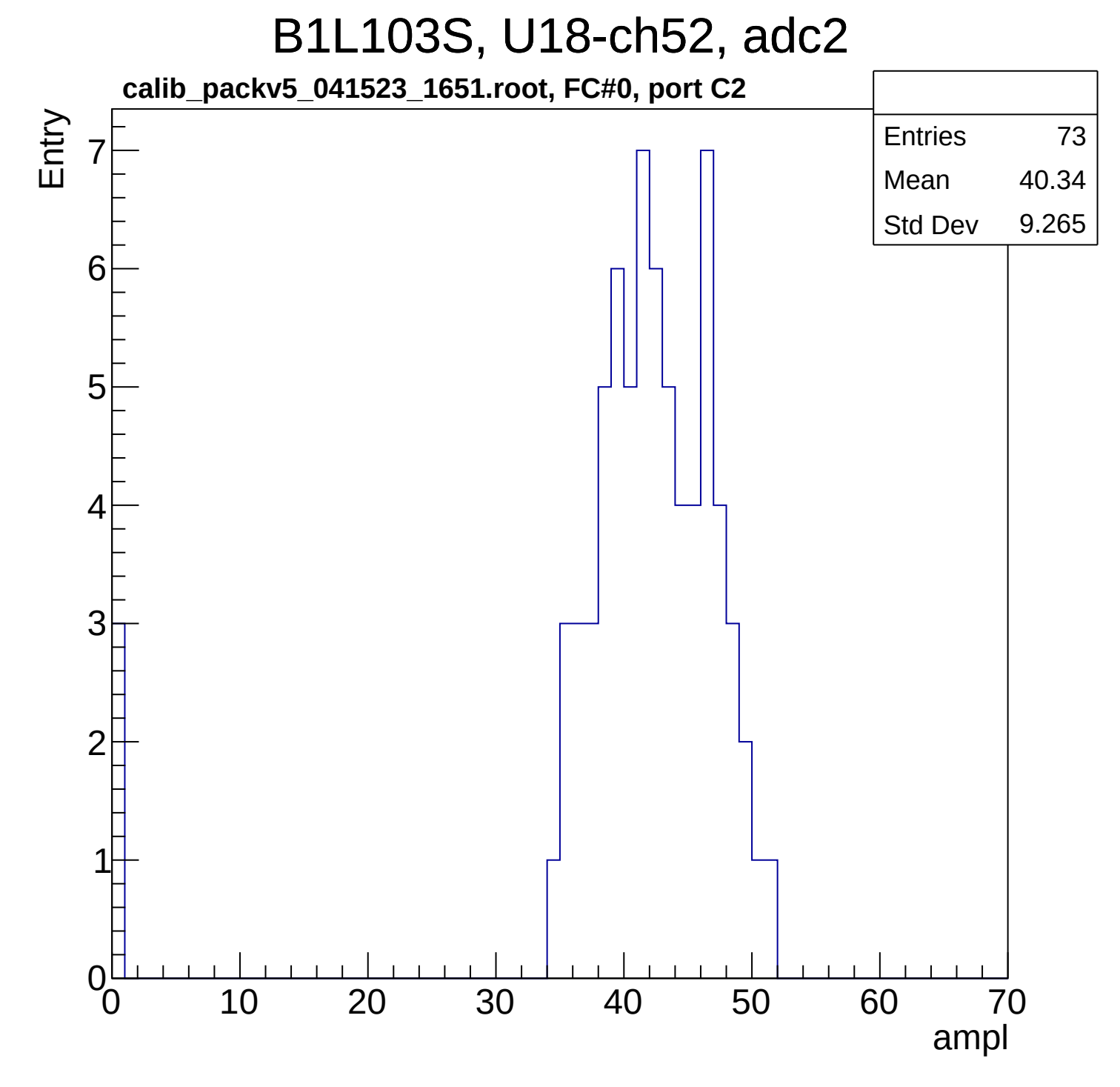
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch52, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 22.13
Std Dev 12.57
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch52, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 30.64
Std Dev 13.47
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch52, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 40.34
Std Dev 9.265
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
30
40
50
60
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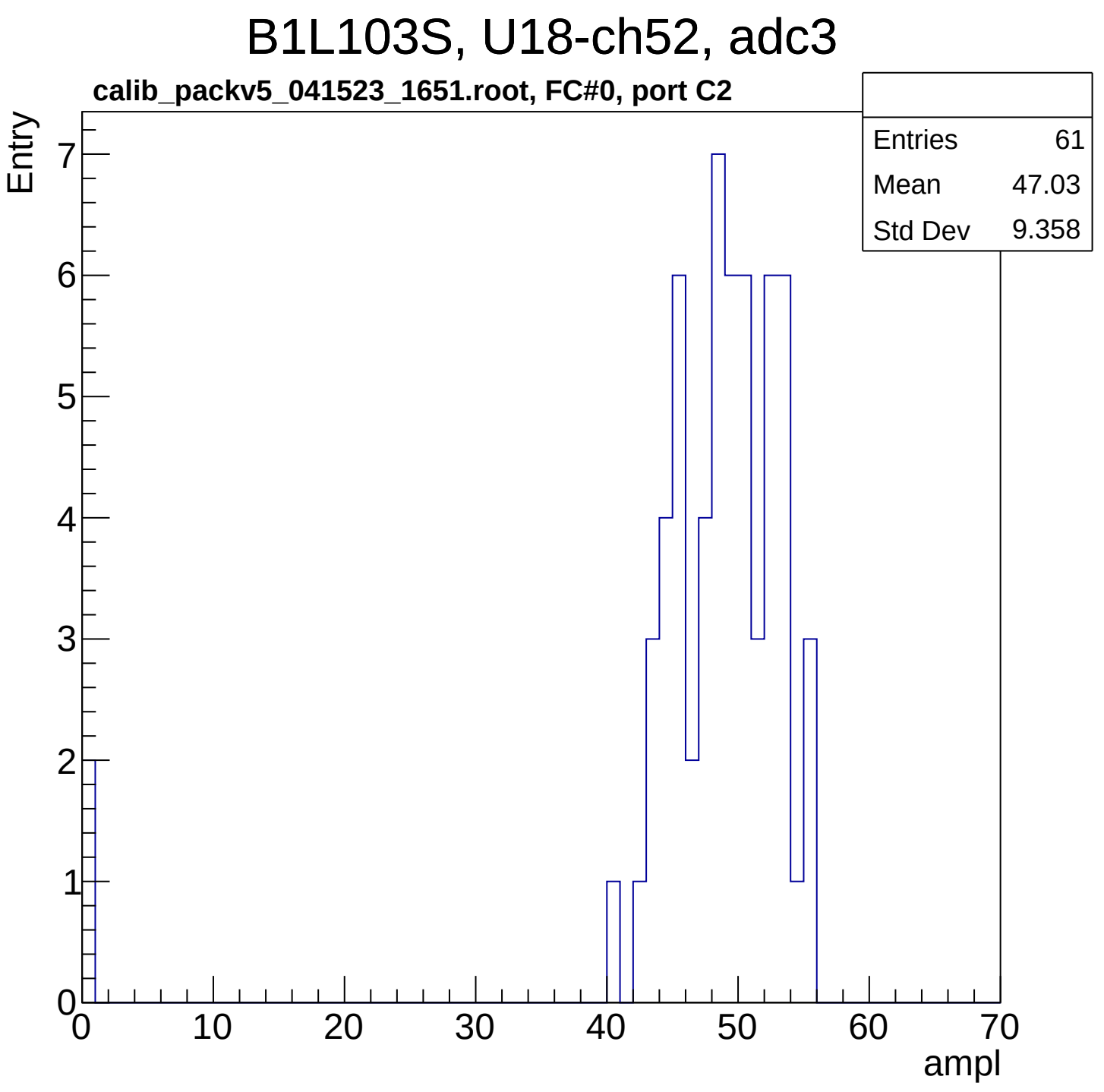
B1L103S, U18-ch52, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 47.03
Std Dev 9.358
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
30
40
50
60
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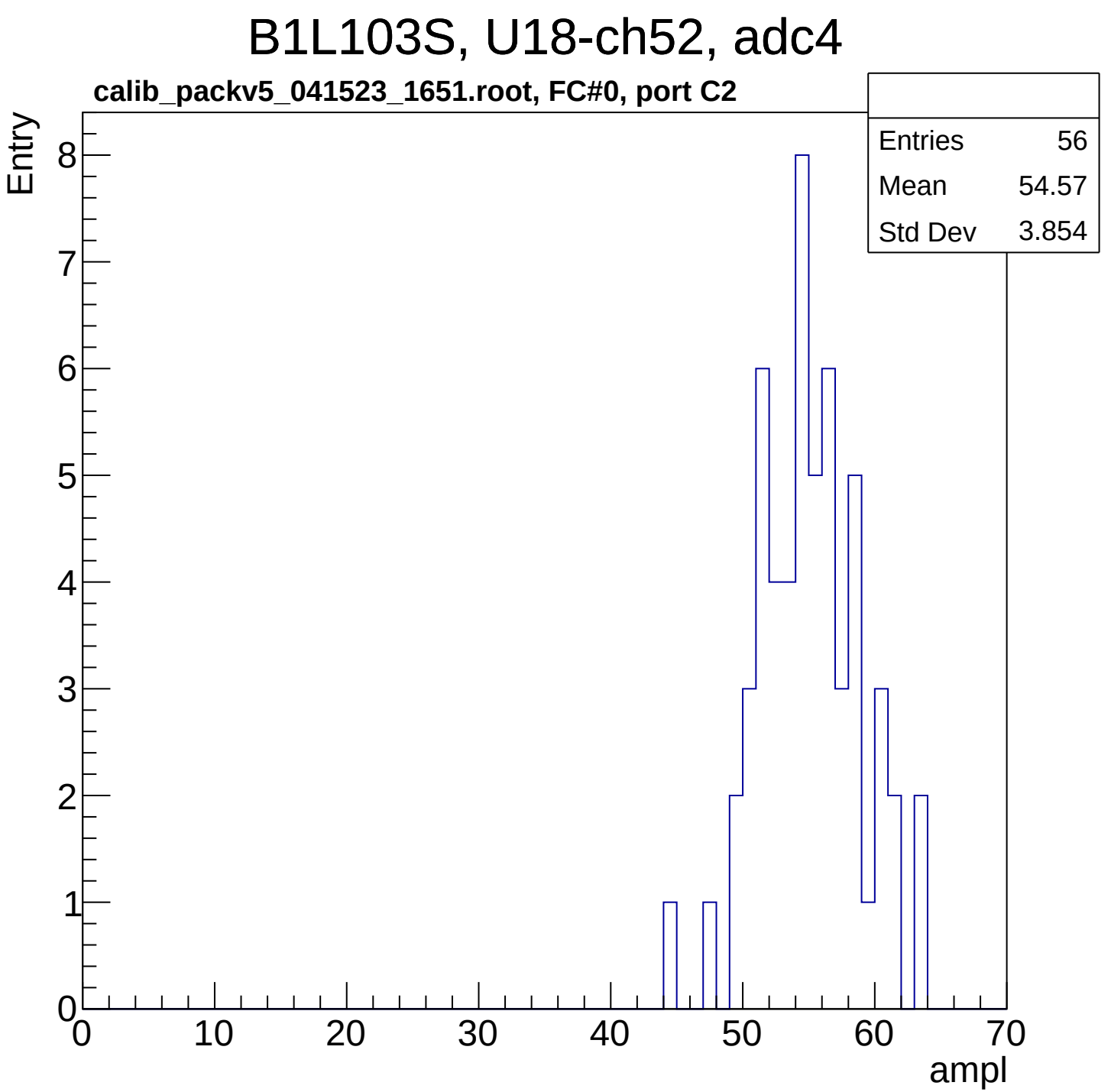
B1L103S, U18-ch52, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 54.57
Std Dev 3.854
Entry
ampl
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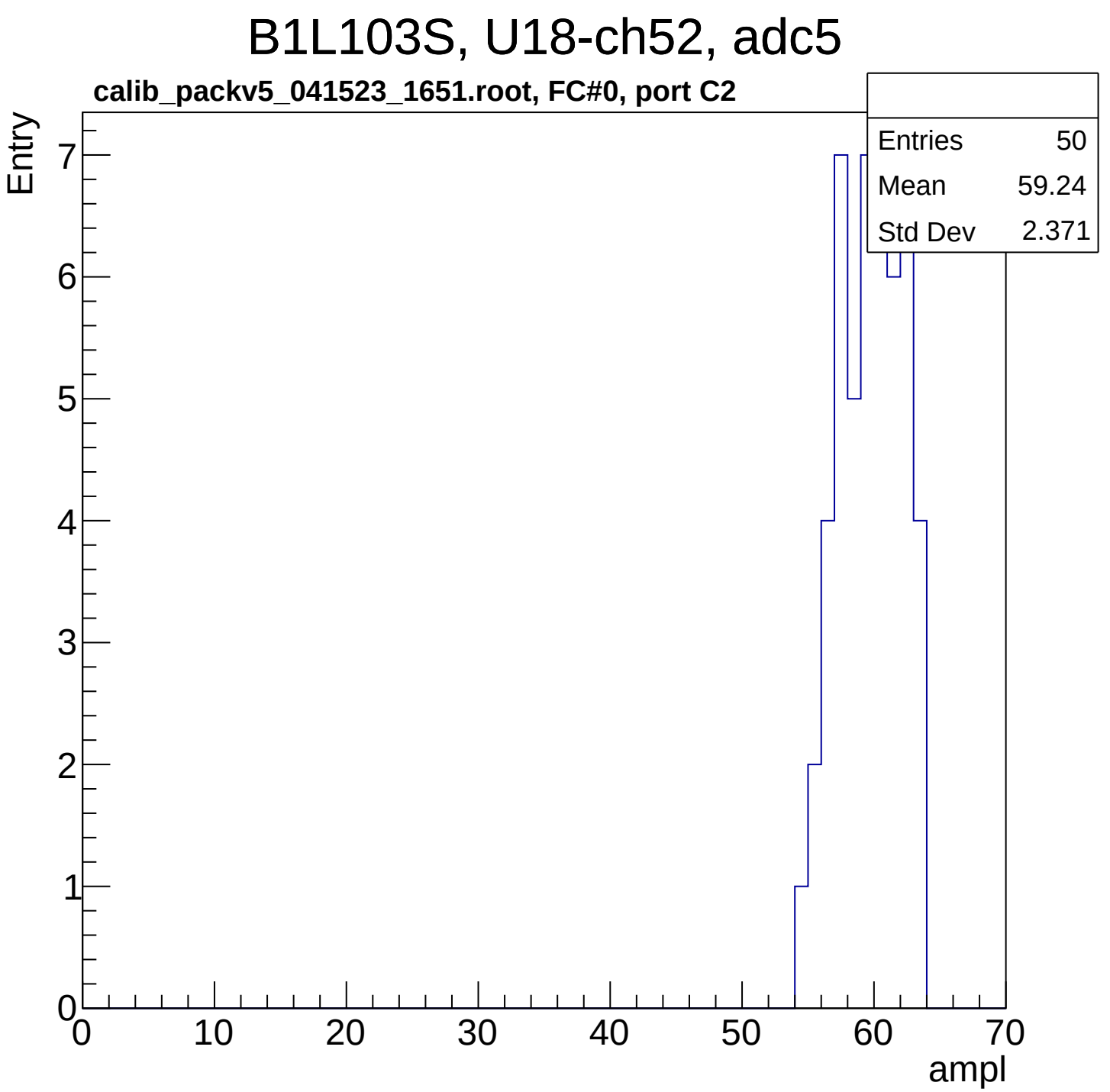
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch52, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 59.24
Std Dev 2.371
Entry
ampl
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1
2
3
4
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6
7
0
10
20
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40
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60
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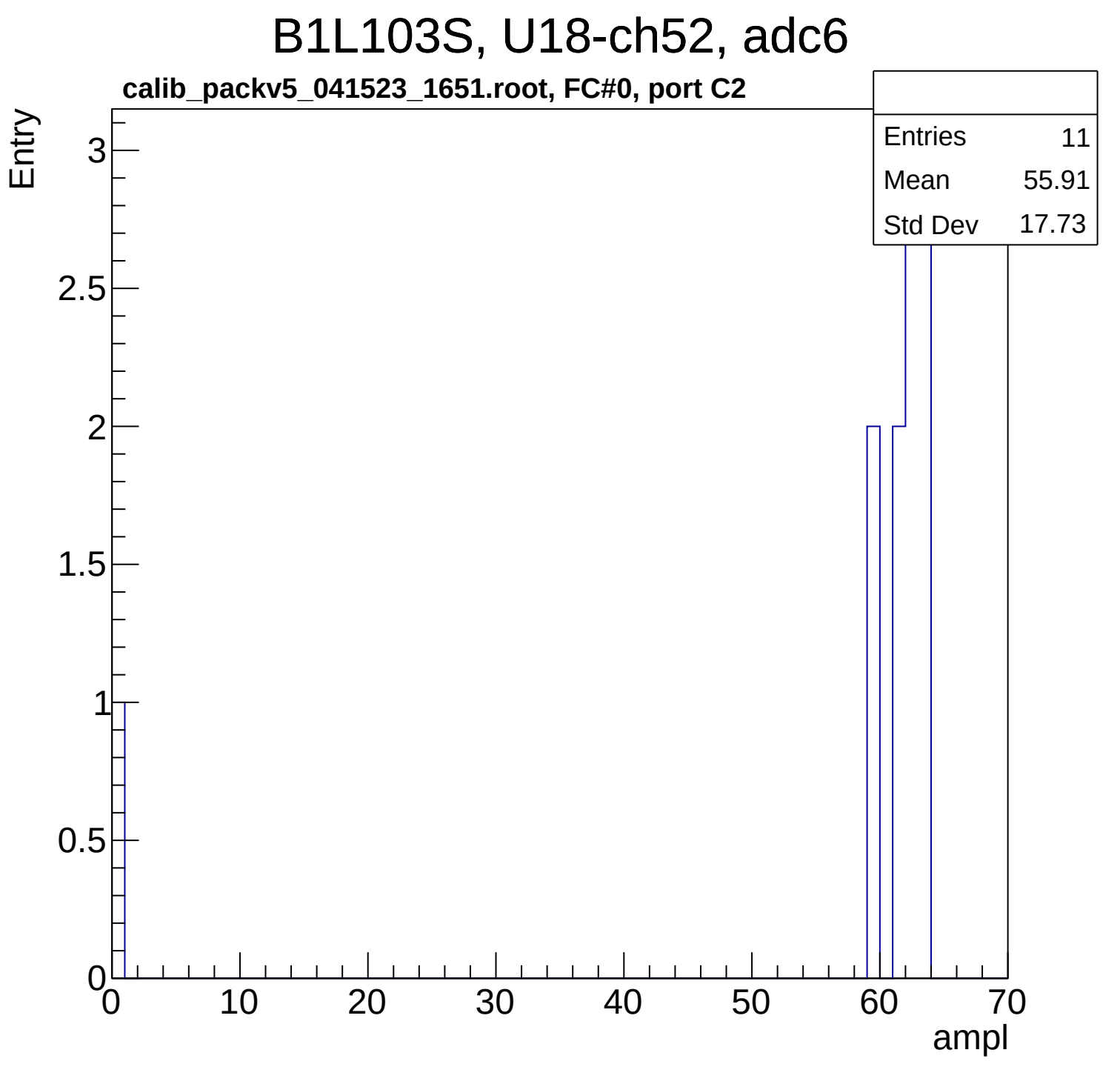
B1L103S, U18-ch52, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 55.91
Std Dev 17.73
Entry
ampl
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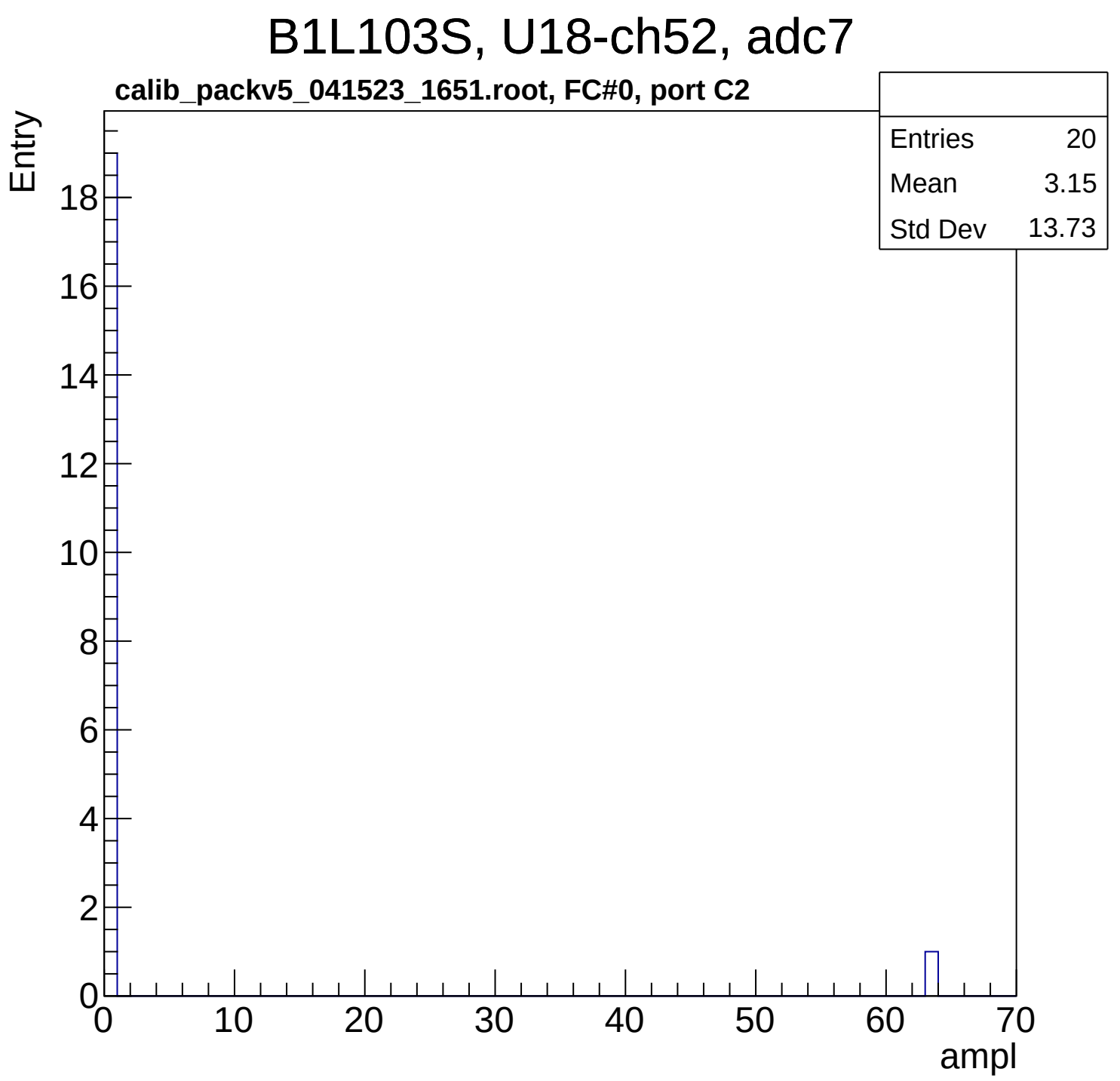
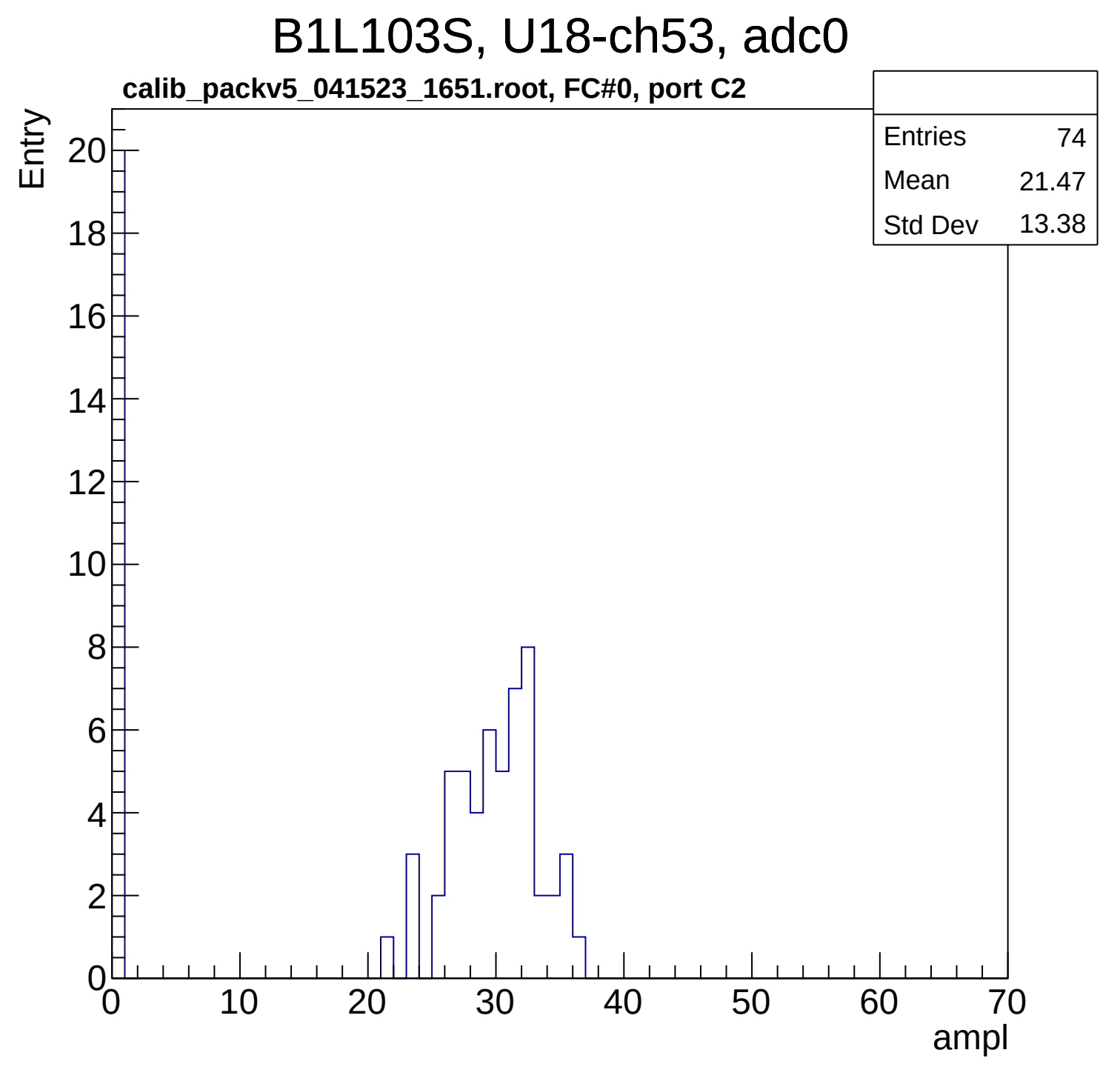
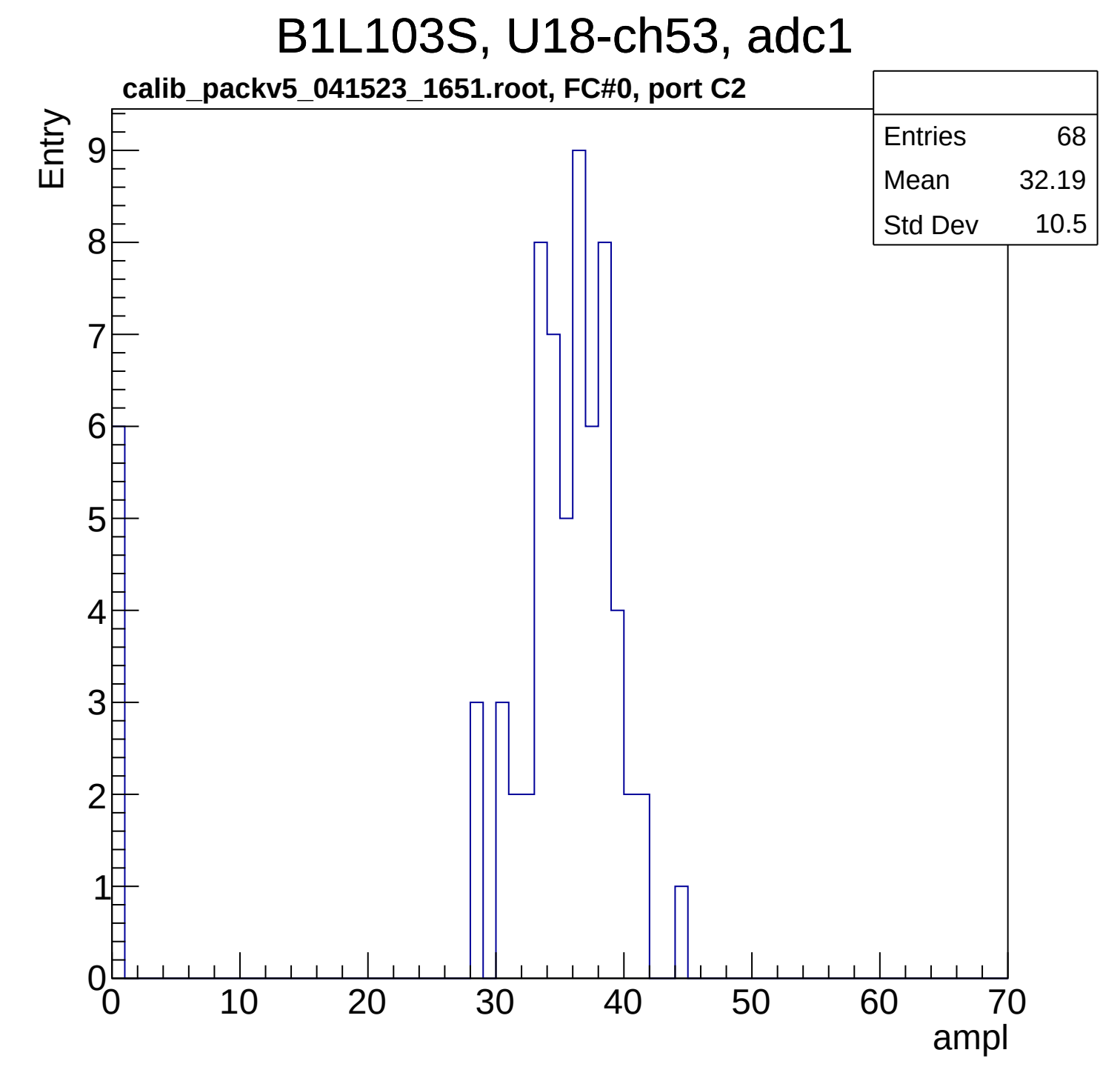
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U18-ch52, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch53, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 21.47
Std Dev 13.38
Entry
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch53, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 32.19
Std Dev 10.5
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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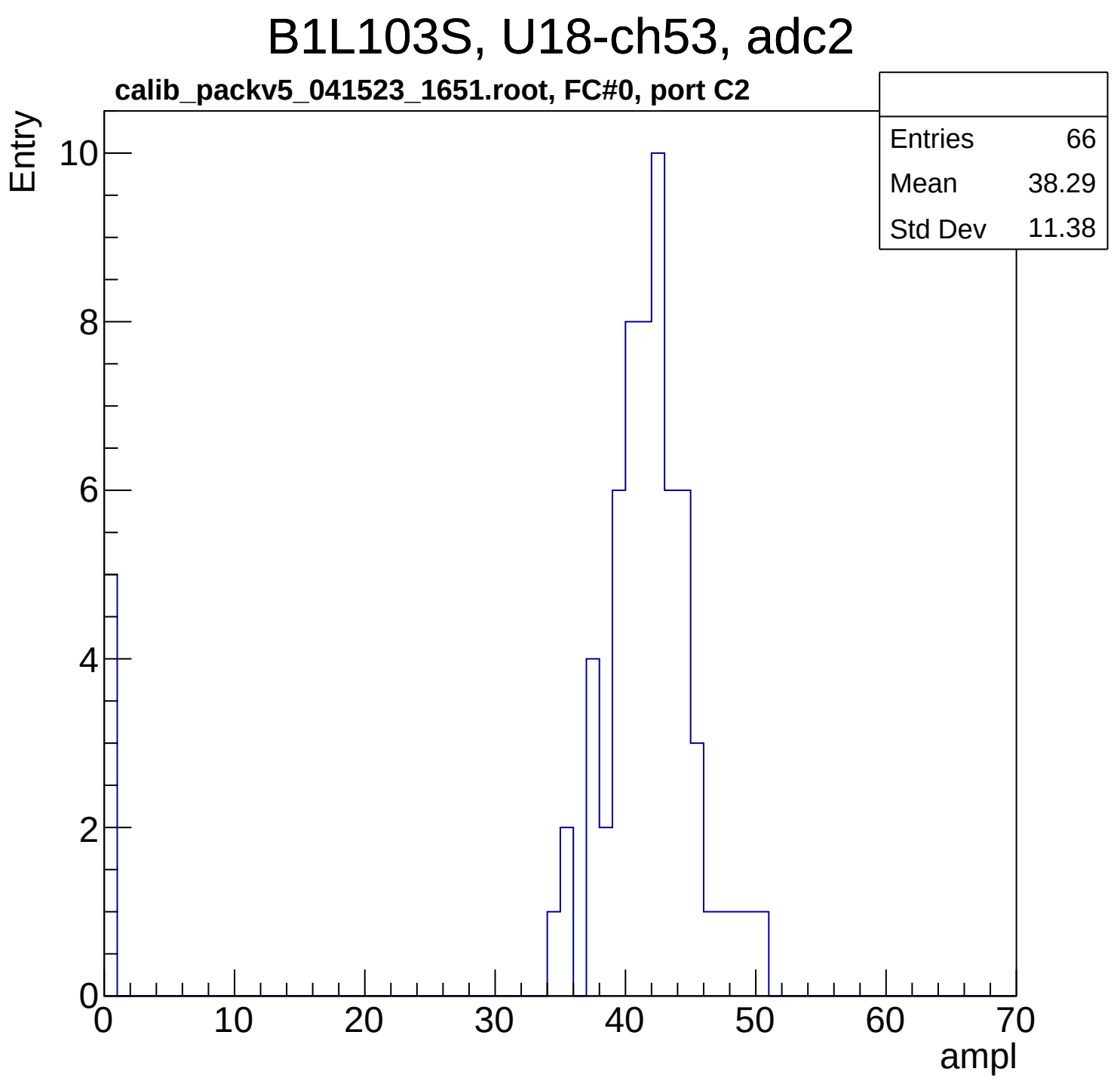
B1L103S, U18-ch53, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 38.29
Std Dev 11.38
Entry
ampl
0
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4
6
8
10
0
10
20
30
40
50
60
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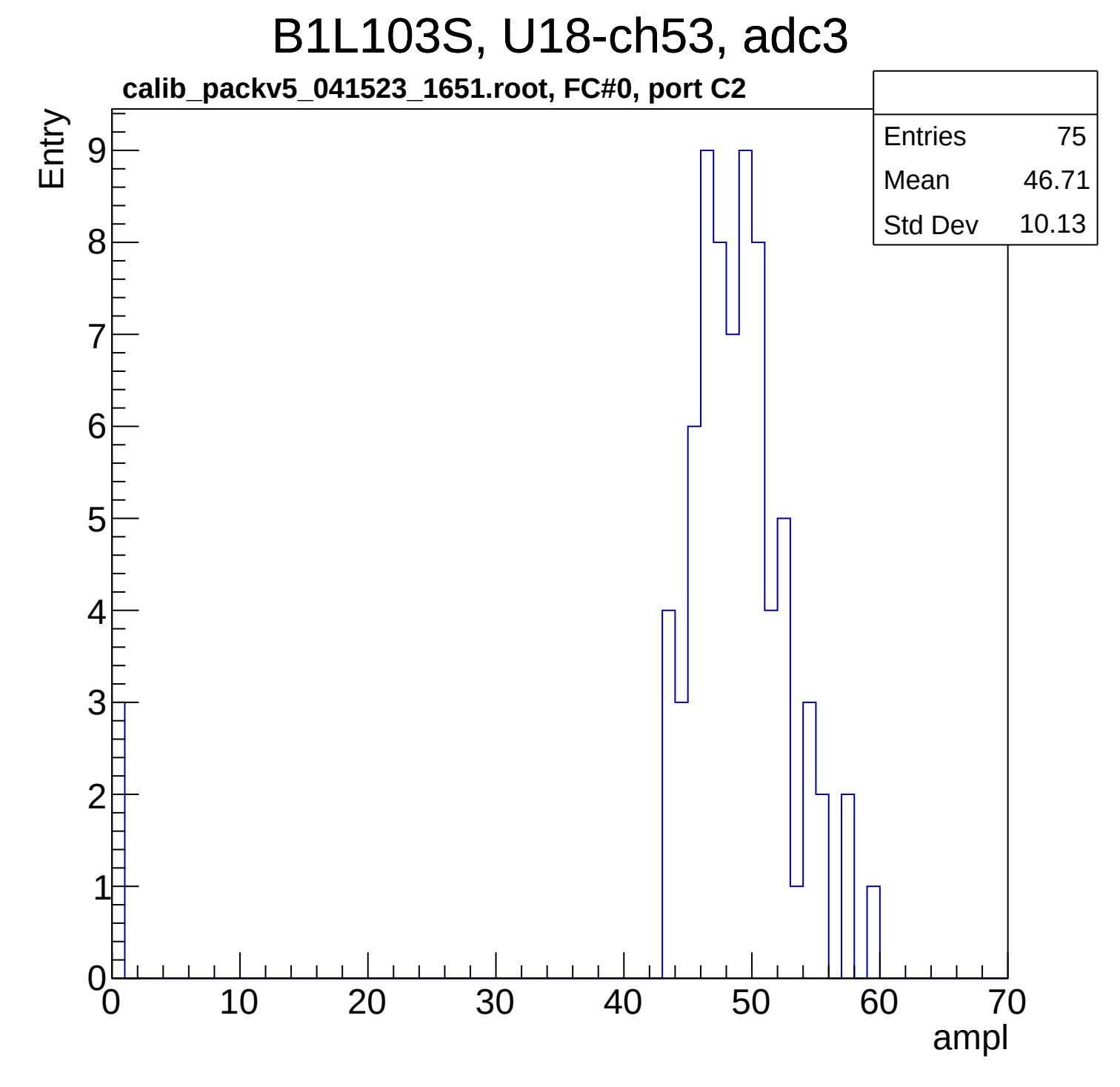
B1L103S, U18-ch53, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 46.71
Std Dev 10.13
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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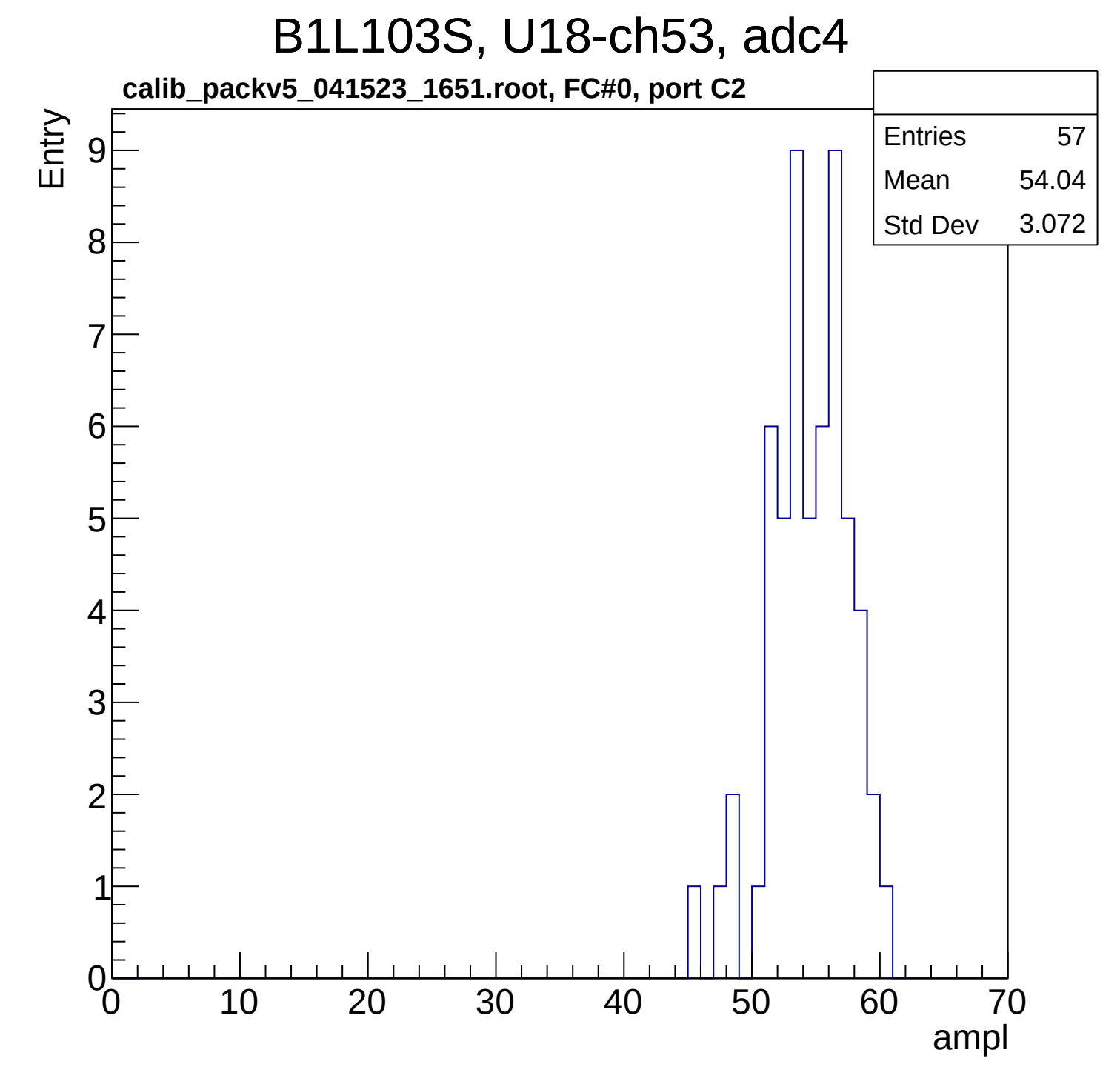
50
60
70


B1L103S, U18-ch53, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 54.04
Std Dev 3.072
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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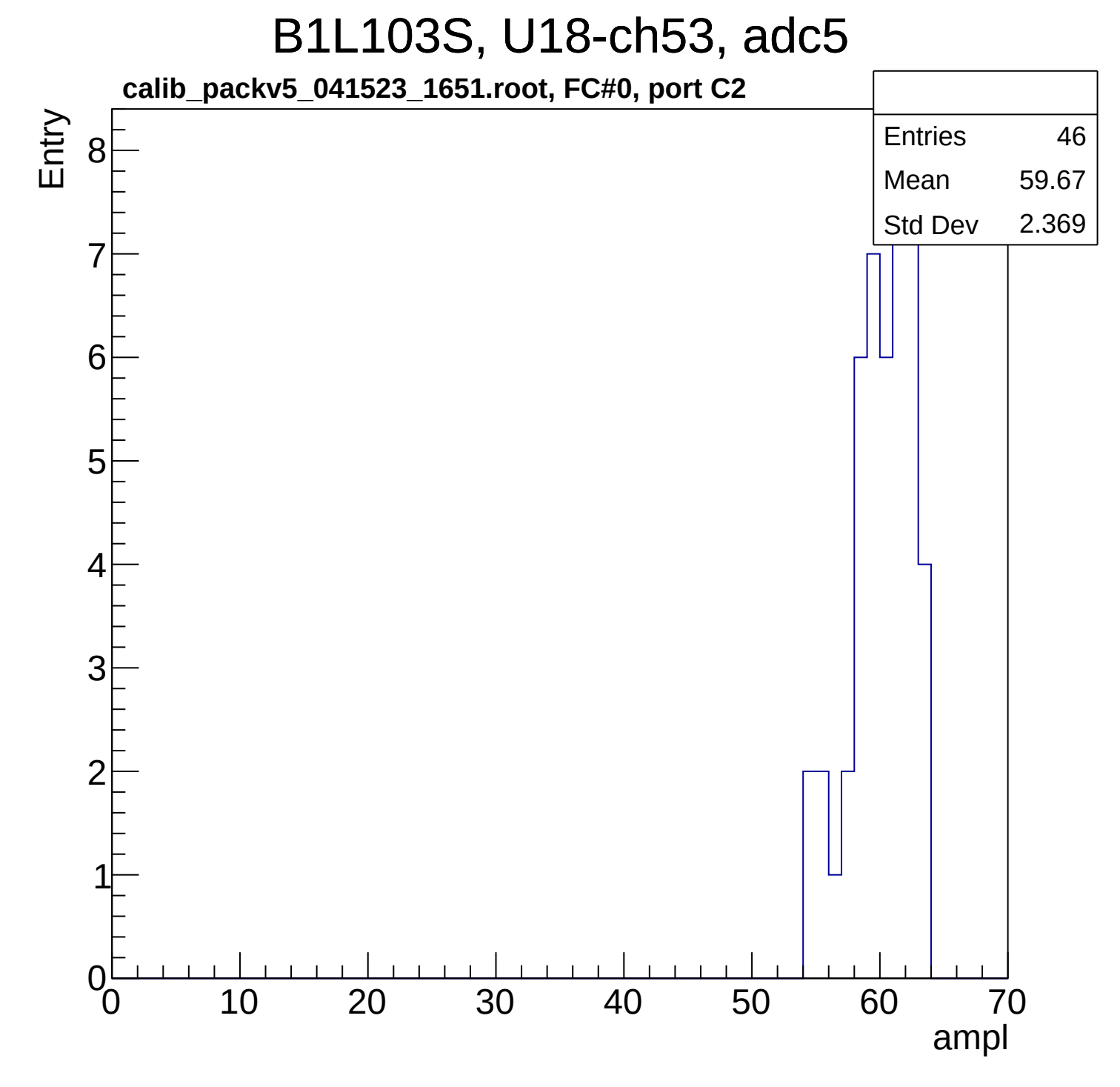
B1L103S, U18-ch53, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 59.67
Std Dev 2.369
Entry
ampl
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2
3
4
5
6
7
8
0
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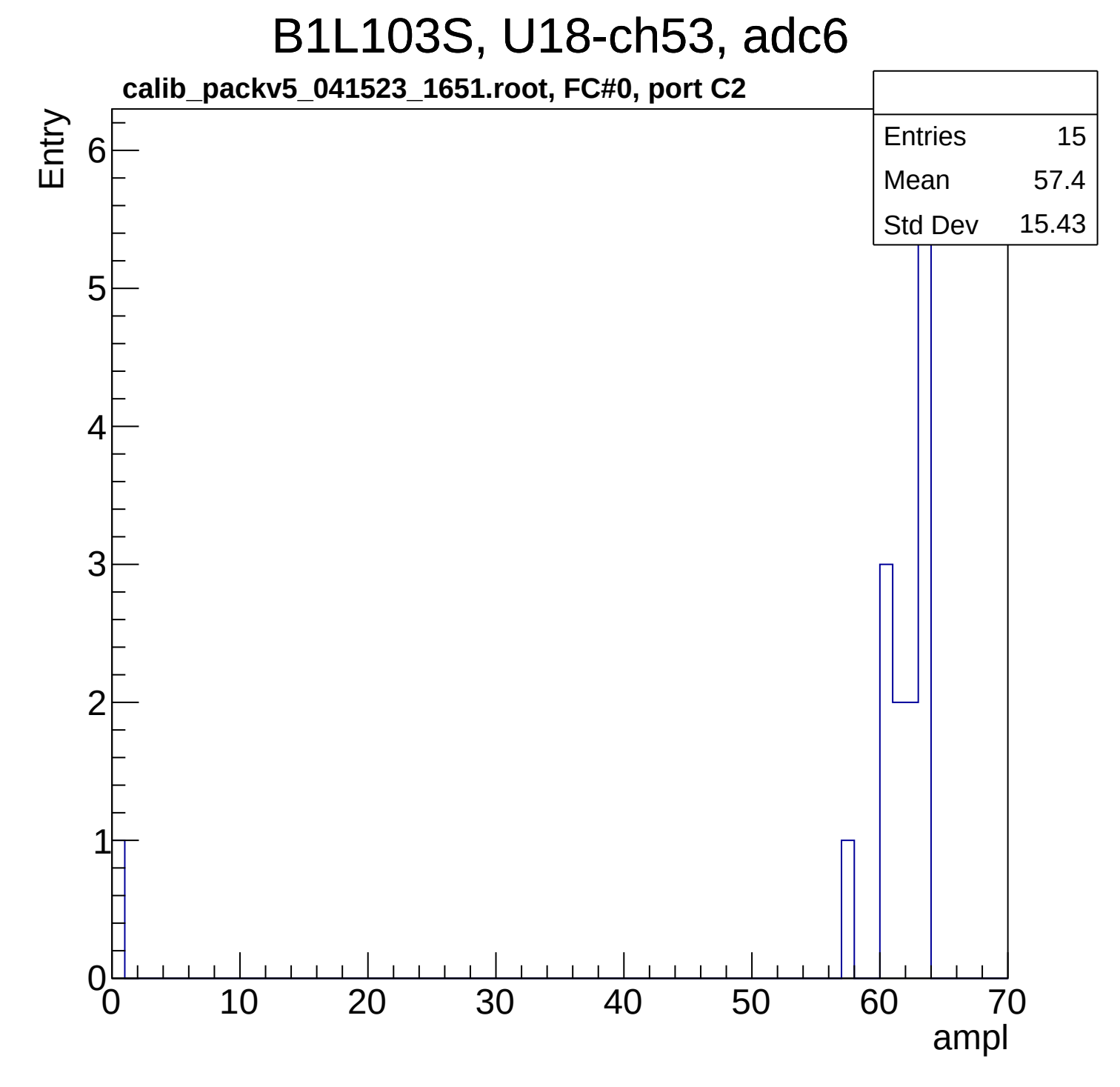
20
30
40
50
60
70


B1L103S, U18-ch53, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 15
Mean 57.4
Std Dev 15.43
Entry
ampl
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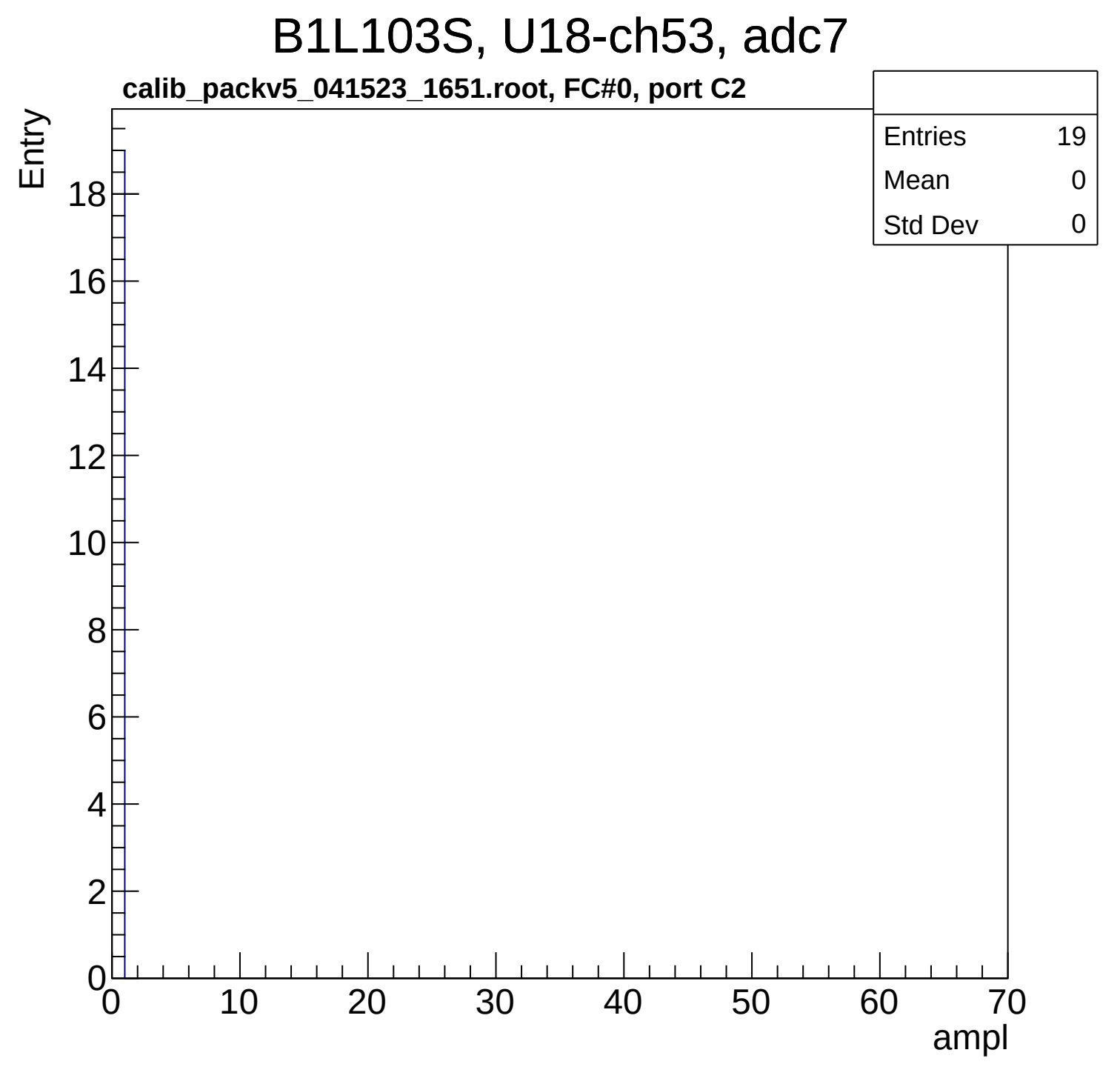
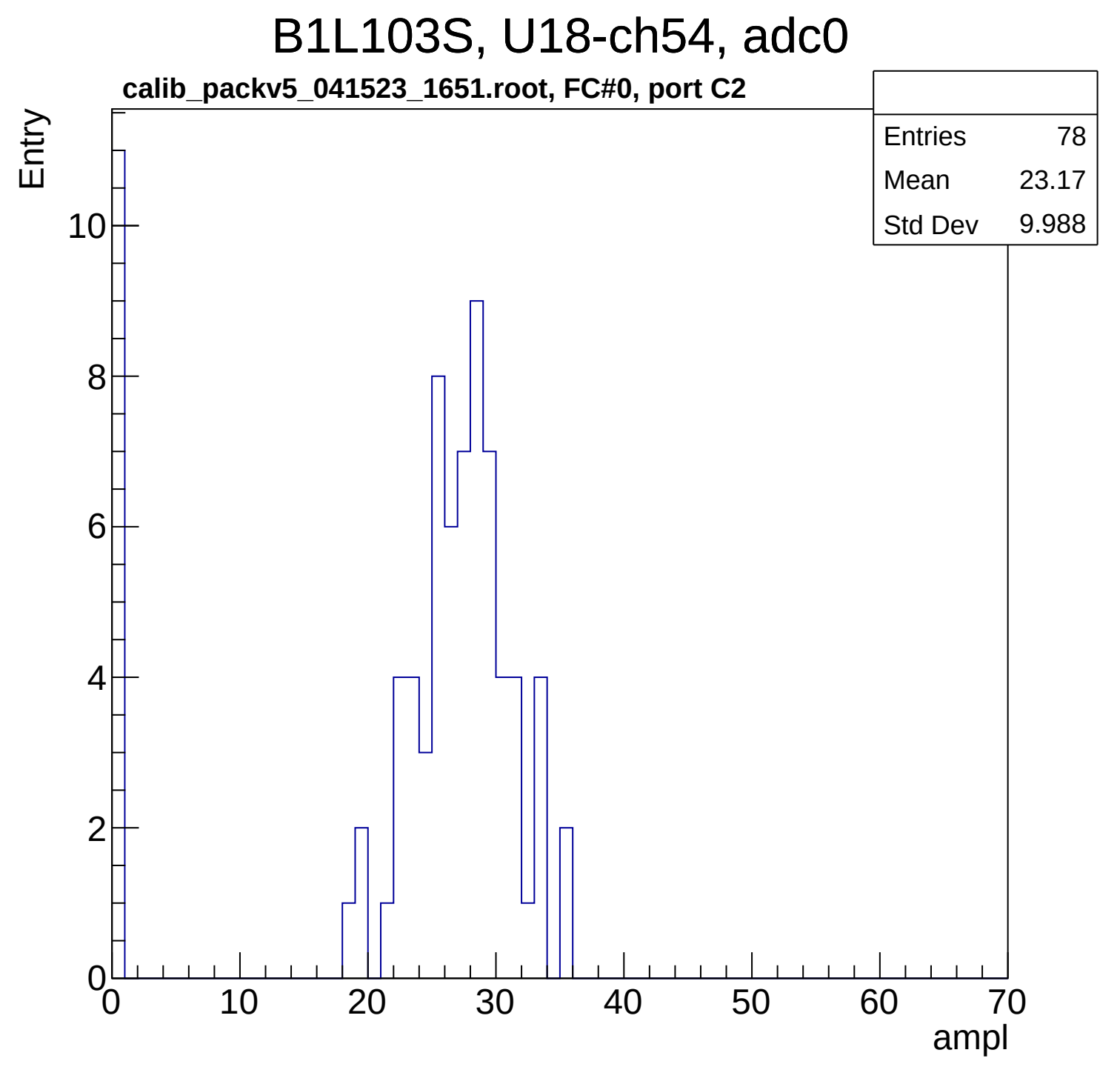
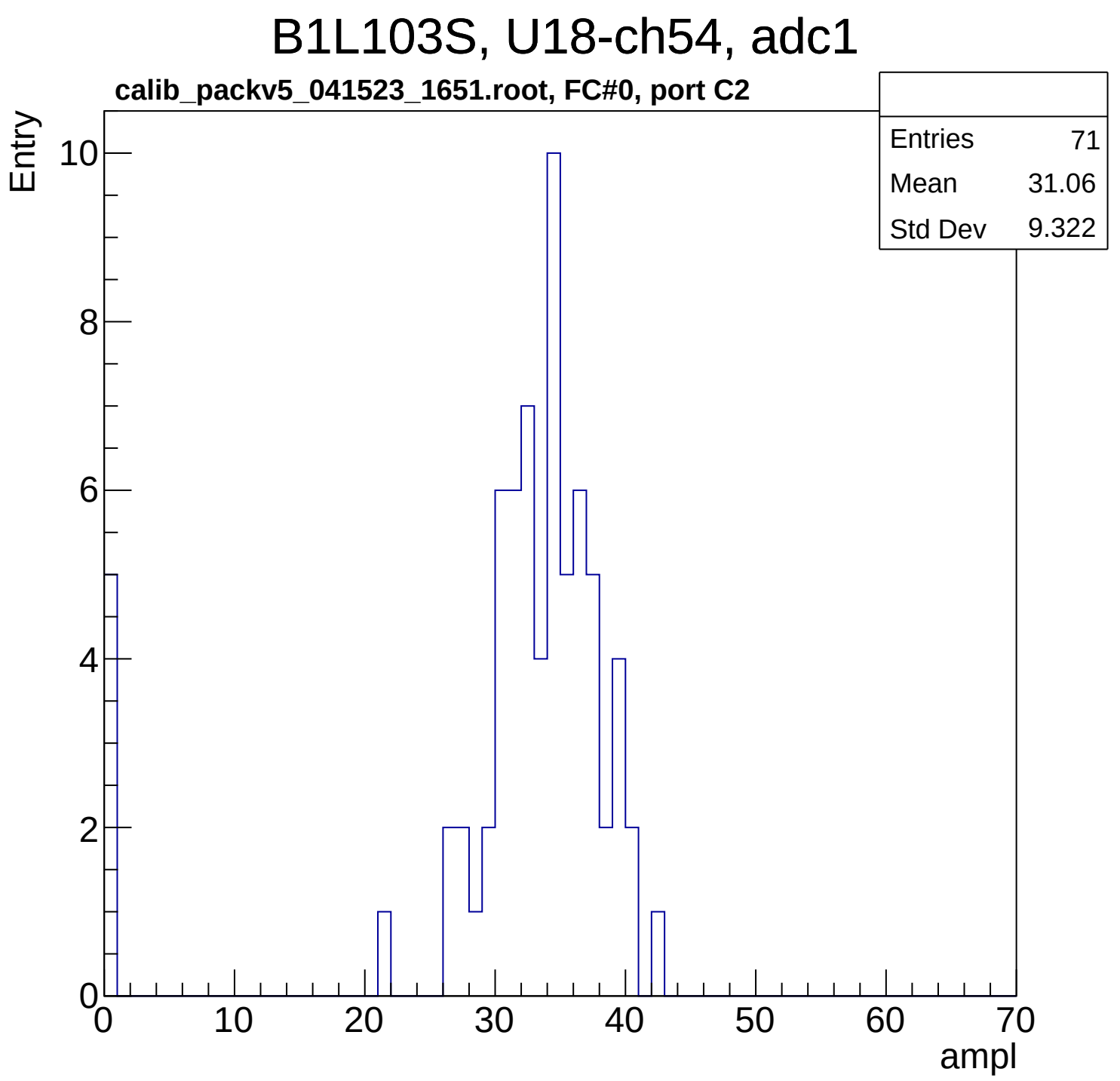
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U18-ch53, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch54, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 23.17
Std Dev 9.988
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U18-ch54, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 31.06
Std Dev 9.322
Entry
0
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6
8
10
0
10
20
30
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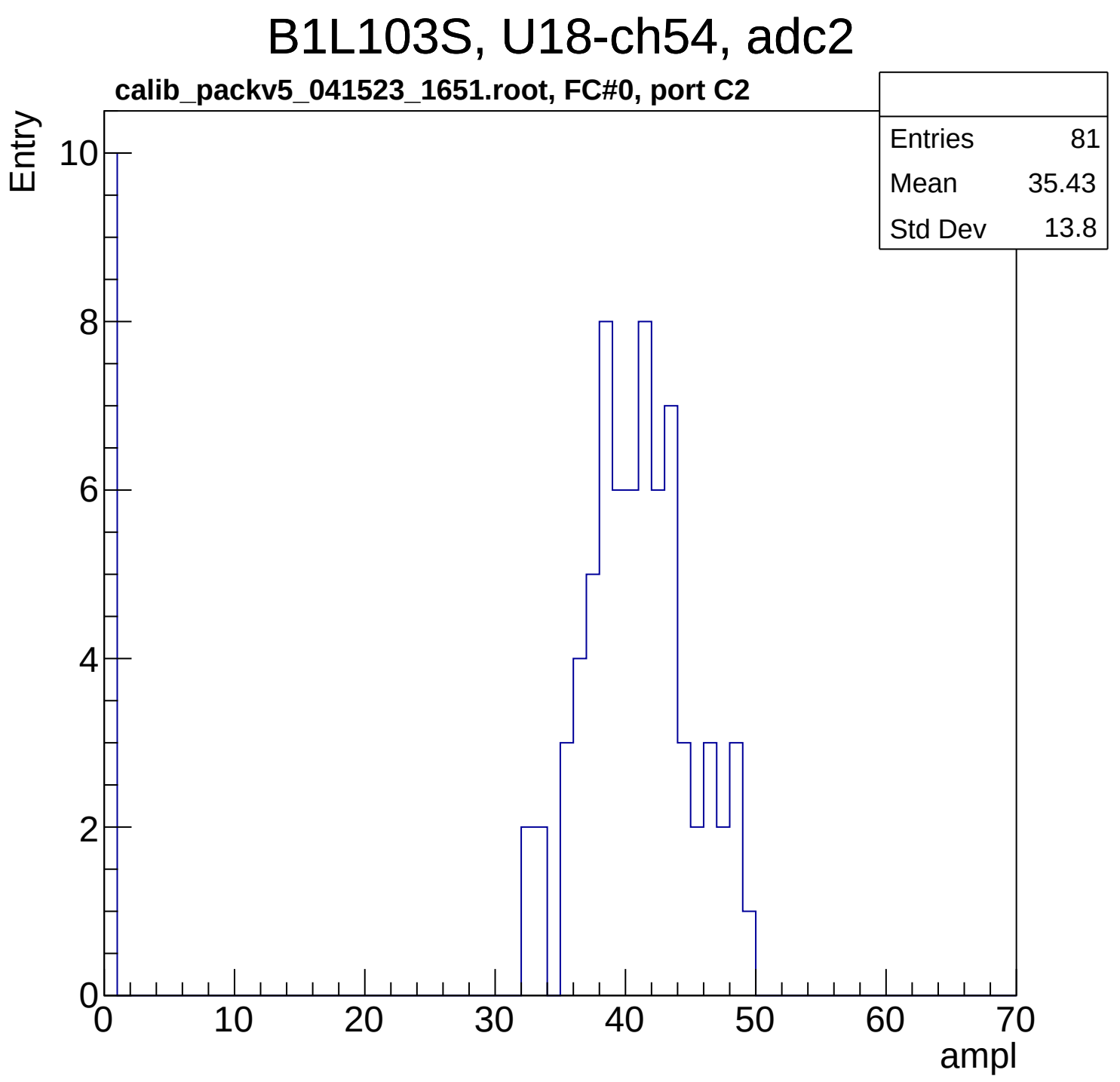
60
70
ampl


B1L103S, U18-ch54, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 35.43
Std Dev 13.8
Entry
ampl
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2
4
6
8
10
0
10
20
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40
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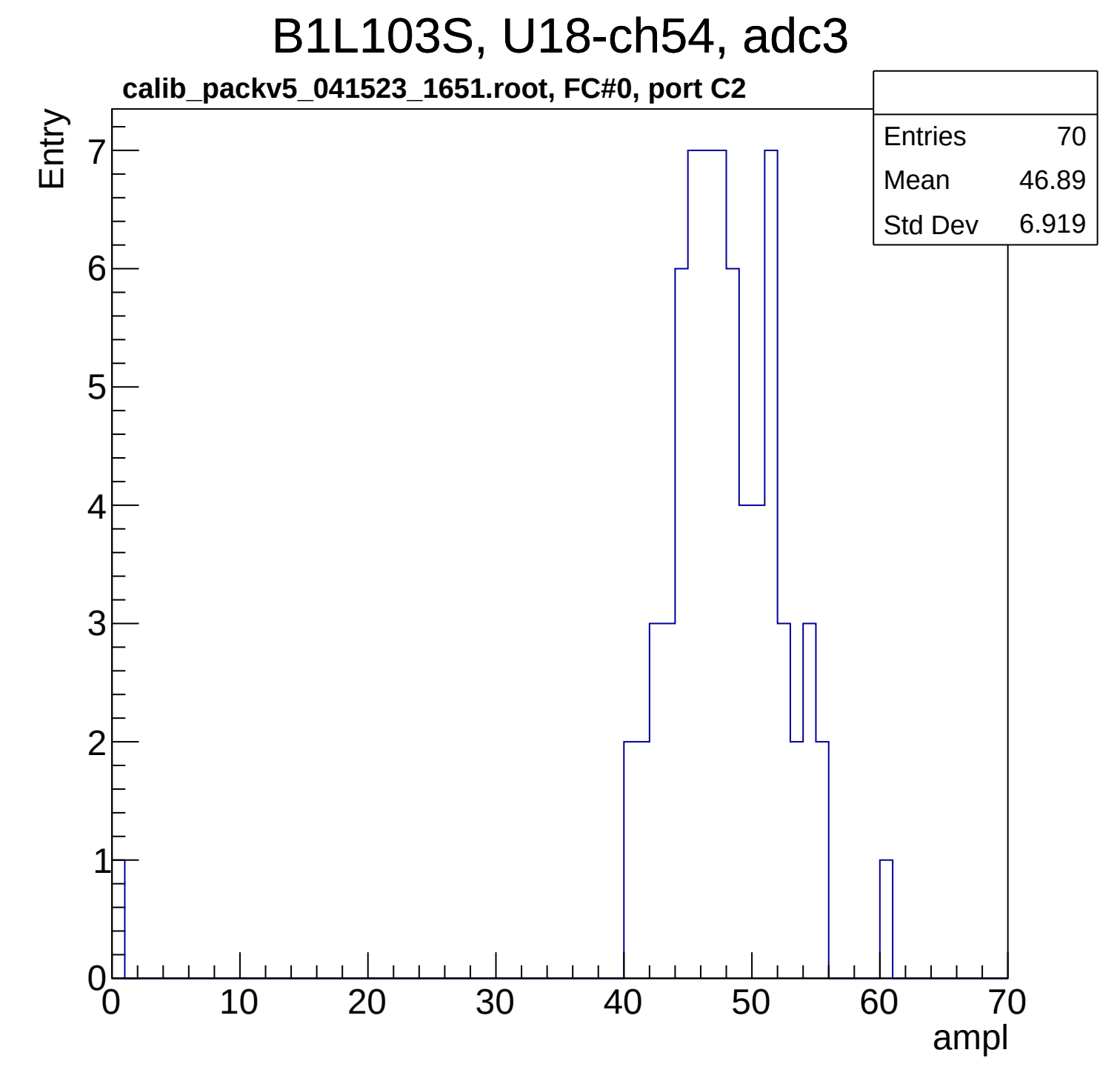
60
70


B1L103S, U18-ch54, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 46.89
Std Dev 6.919
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
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40
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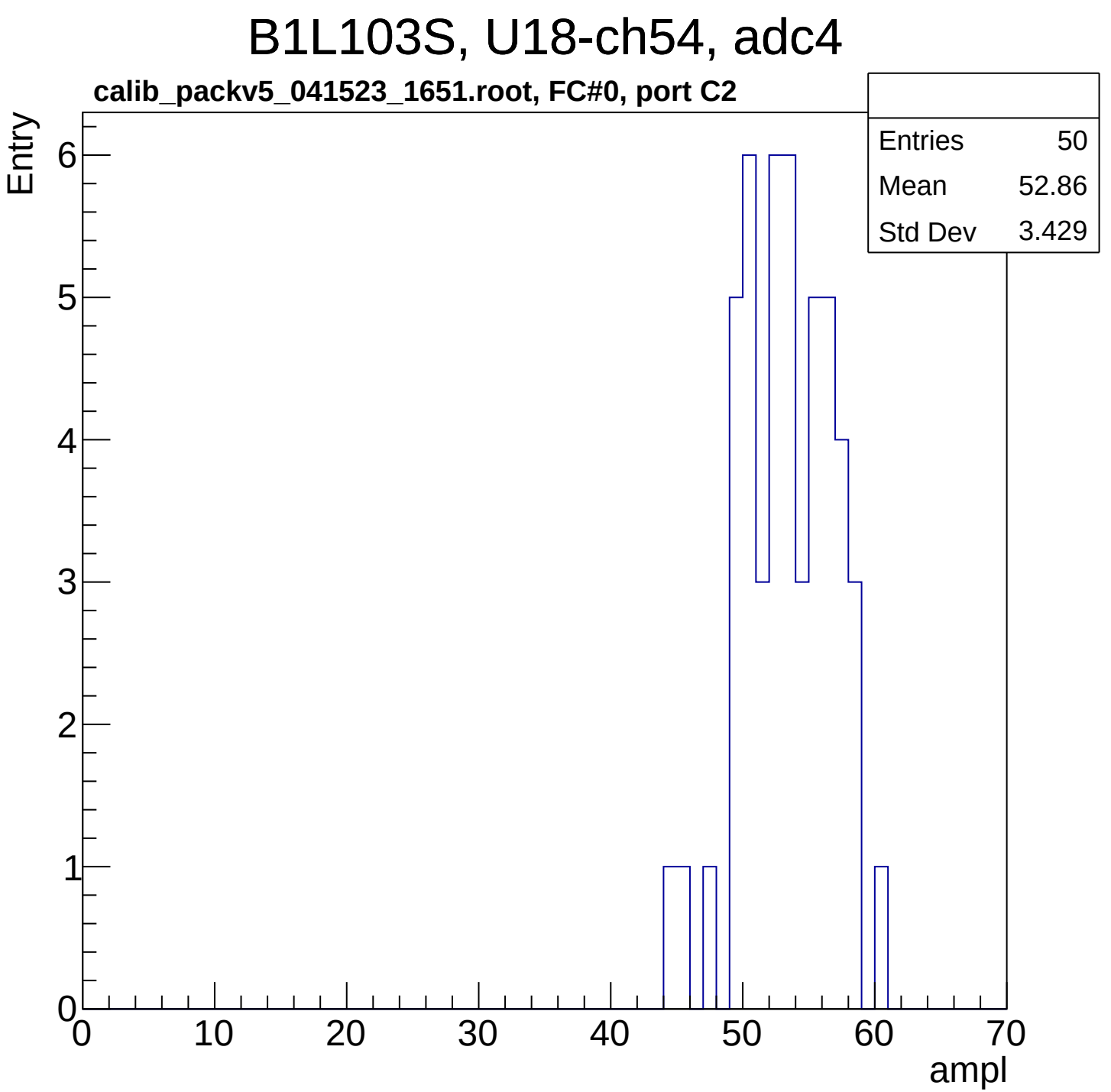
60
70


B1L103S, U18-ch54, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 52.86
Std Dev 3.429
Entry
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1
2
3
4
5
6
0
10
20
30
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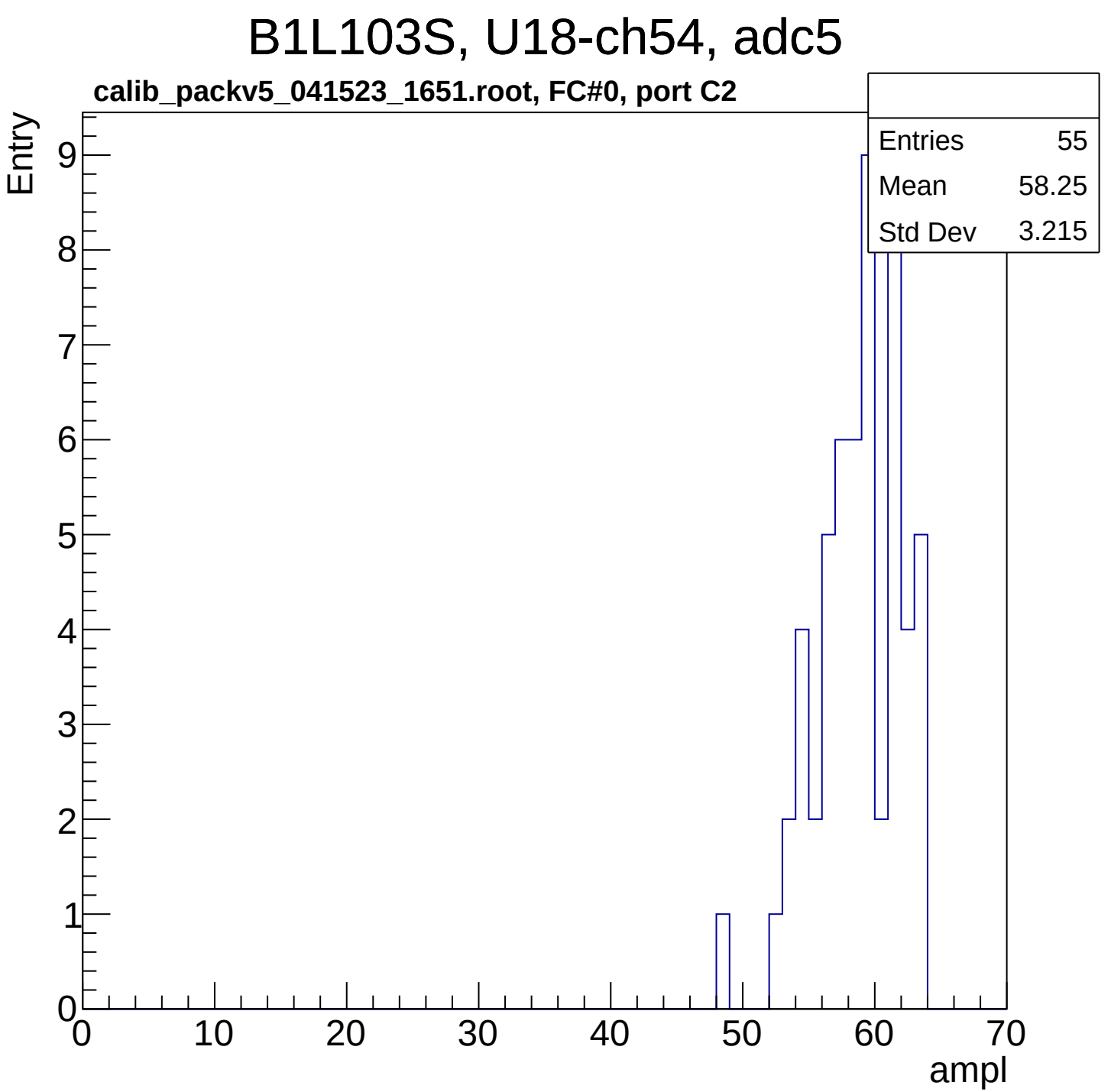
50
60
70
ampl


B1L103S, U18-ch54, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 58.25
Std Dev 3.215
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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60
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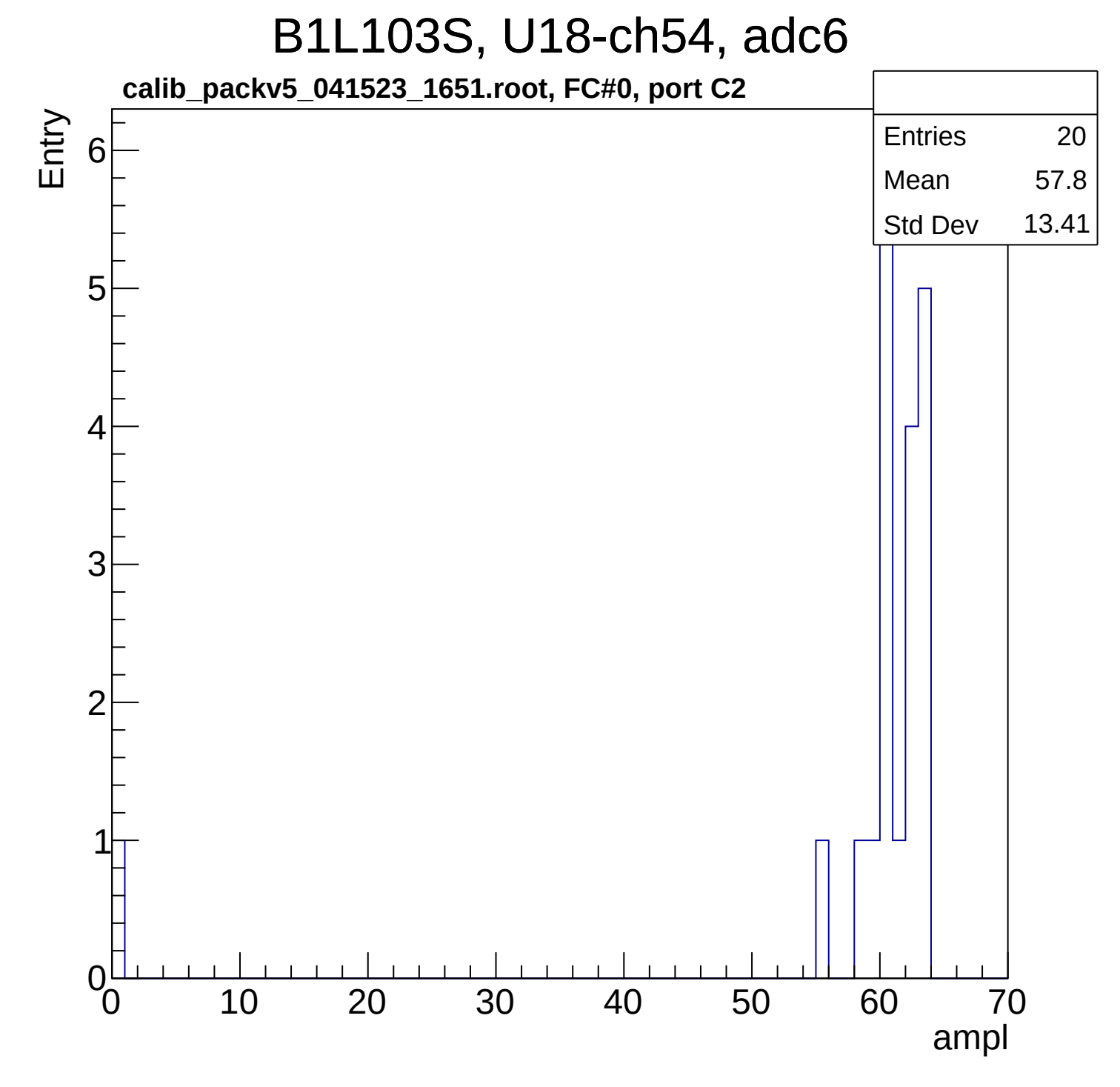
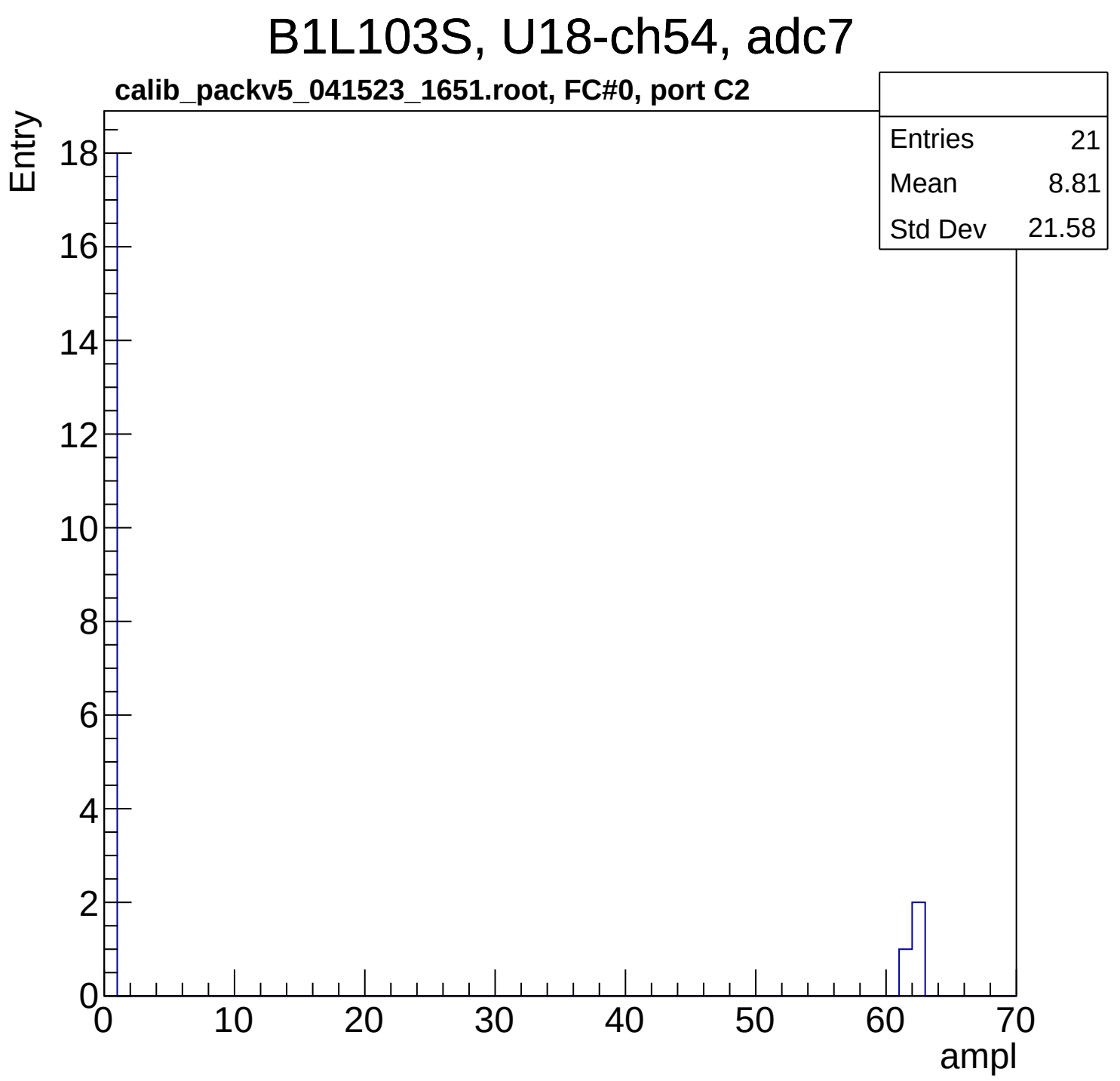
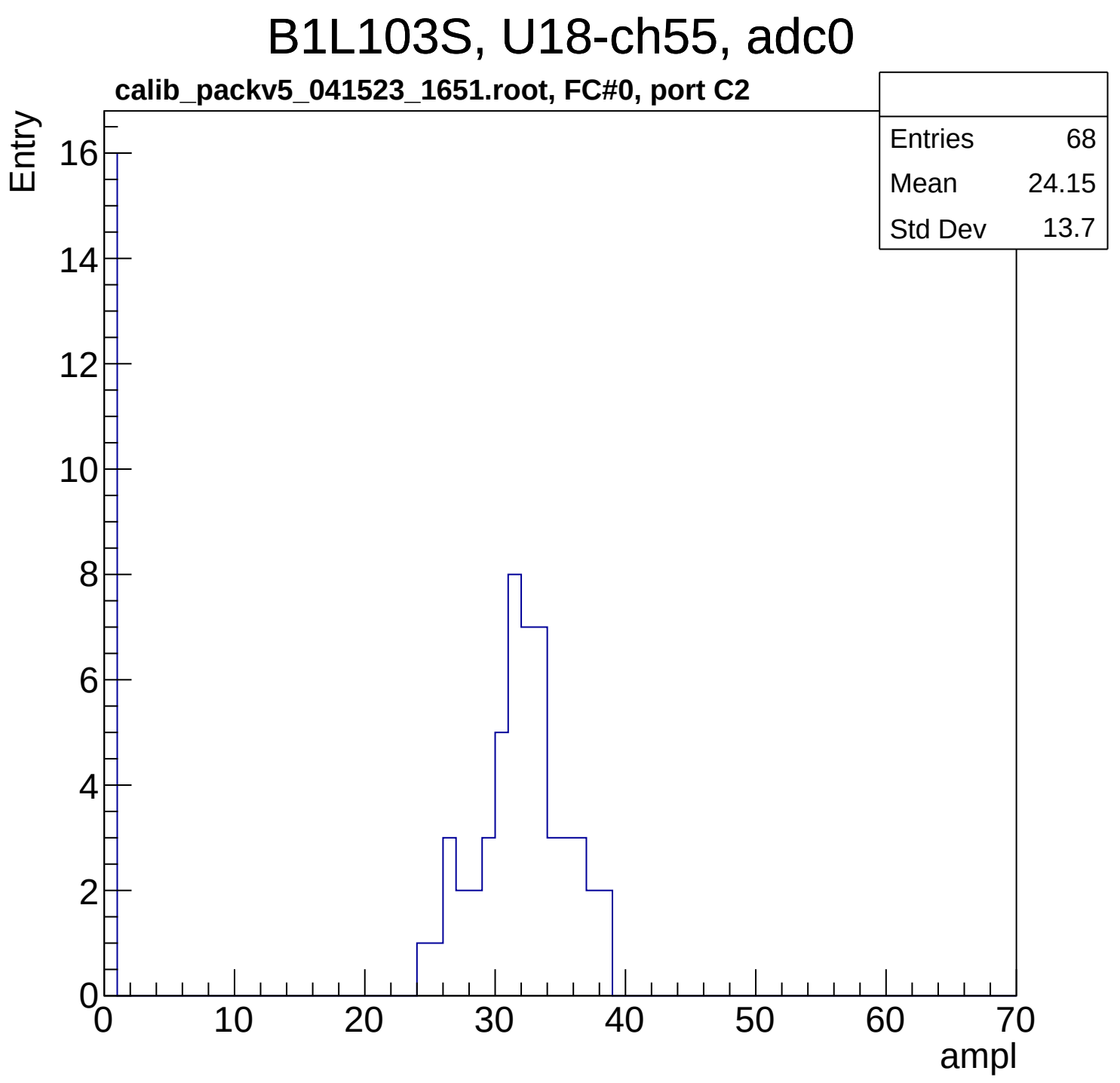

B1L103S, U18-ch54, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 57.8
Std Dev 13.41
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U18-ch54, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 8.81
Std Dev 21.58
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch55, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 24.15
Std Dev 13.7
Entry
ampl
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2
4
6
8
10
12
14
16
0
10
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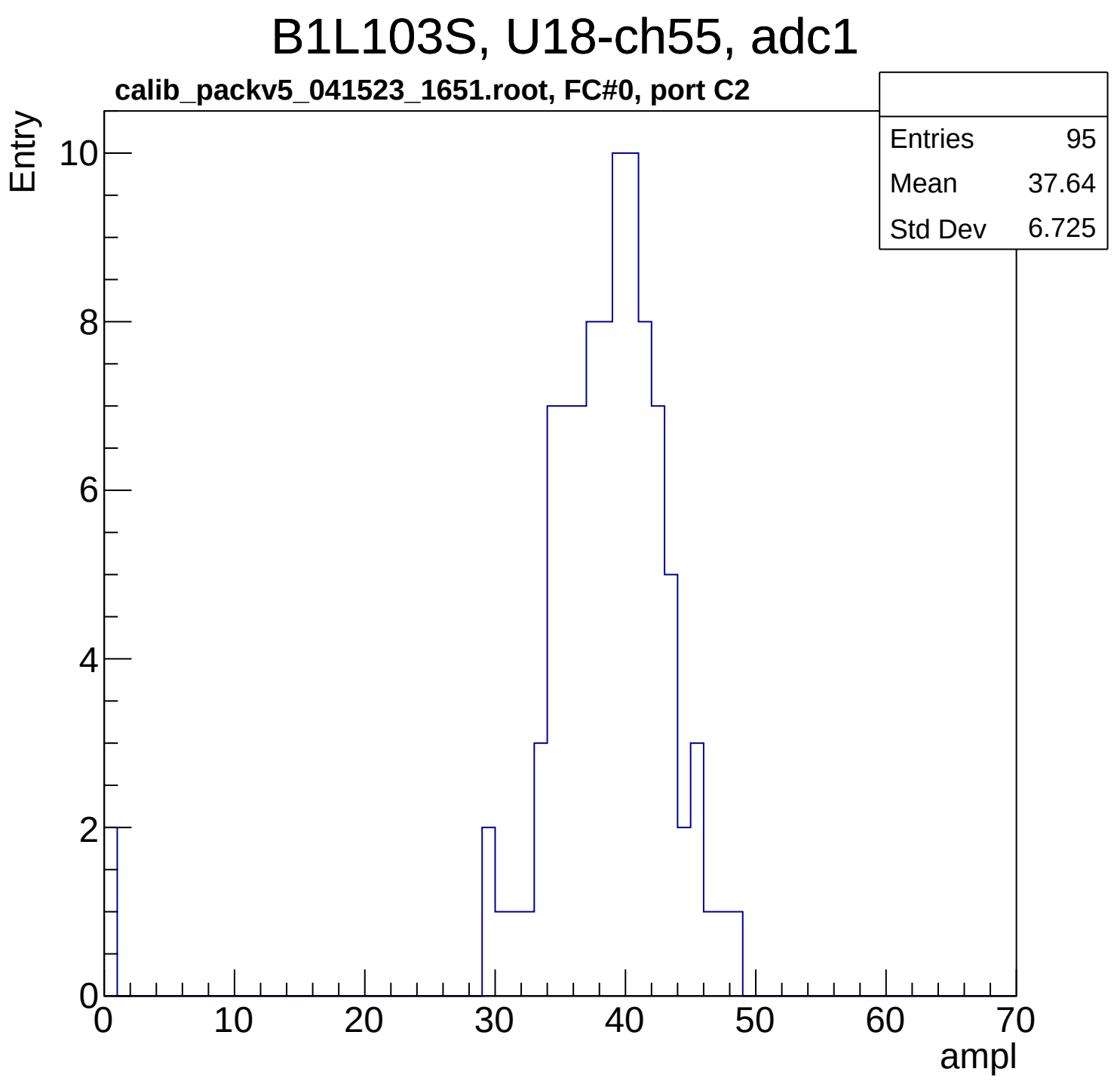
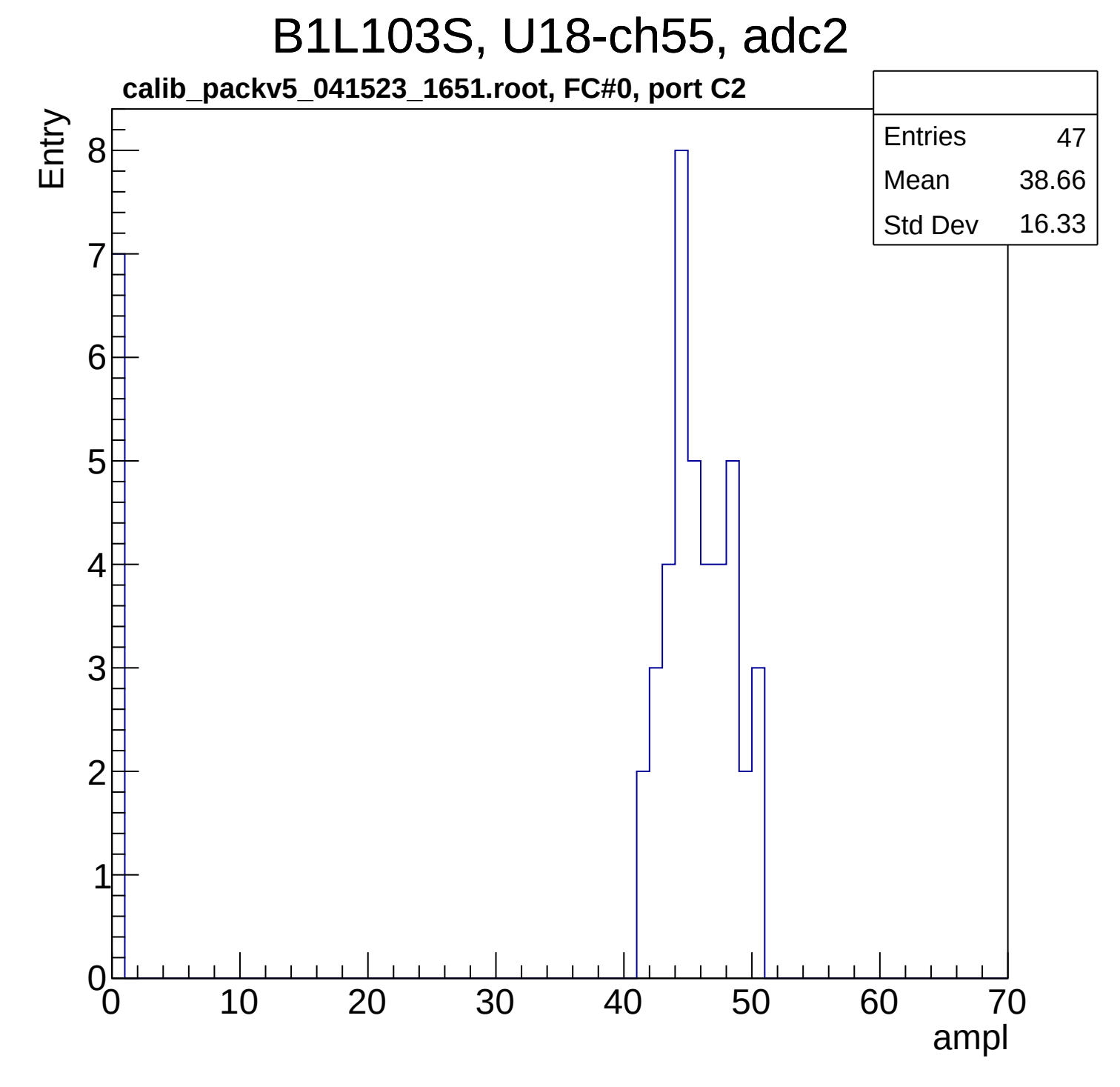

B1L103S, U18-ch55, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 95
Mean 37.64
Std Dev 6.725
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U18-ch55, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 38.66
Std Dev 16.33
Entry
ampl
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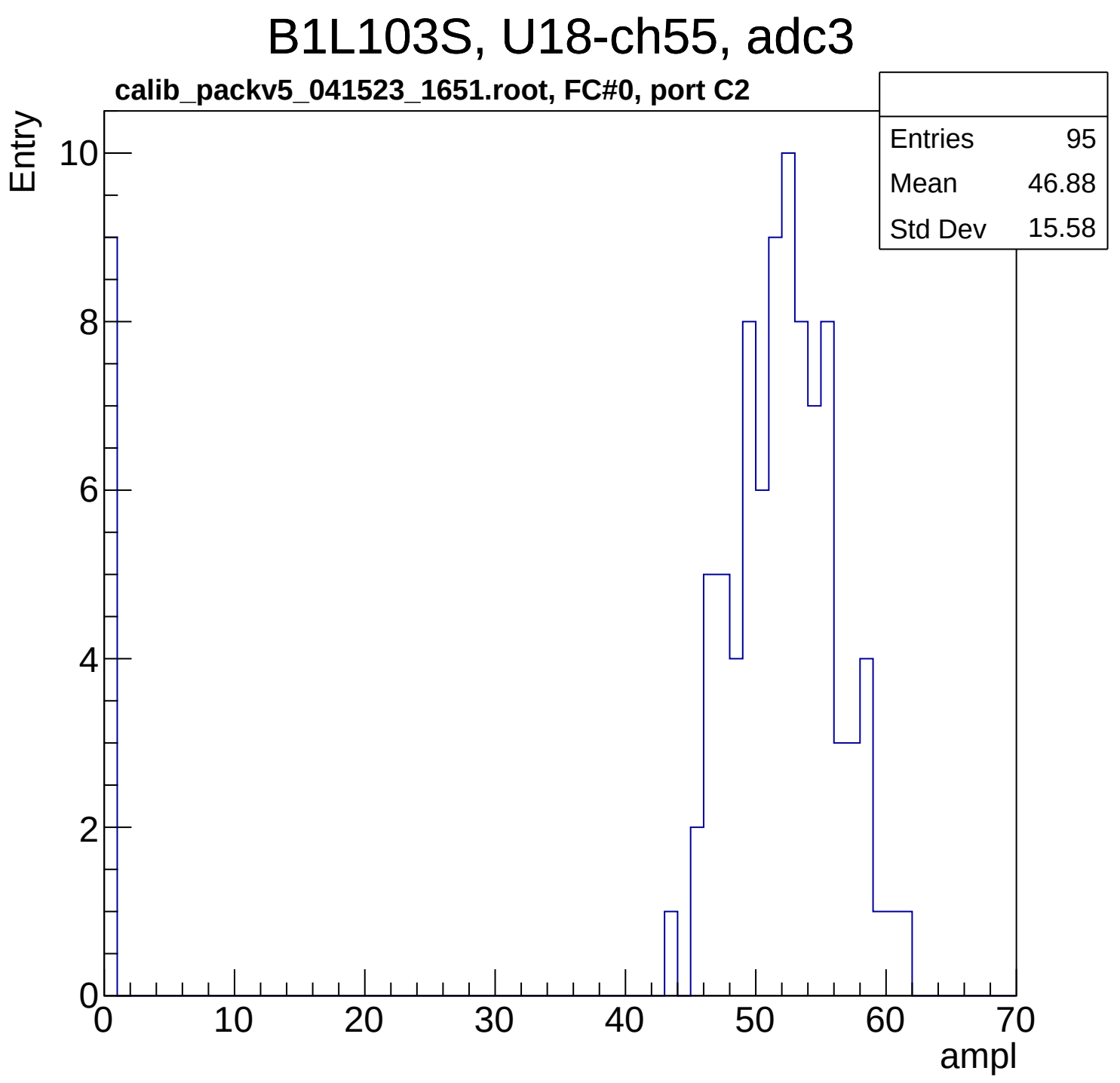
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch55, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 95
Mean 46.88
Std Dev 15.58
Entry
ampl
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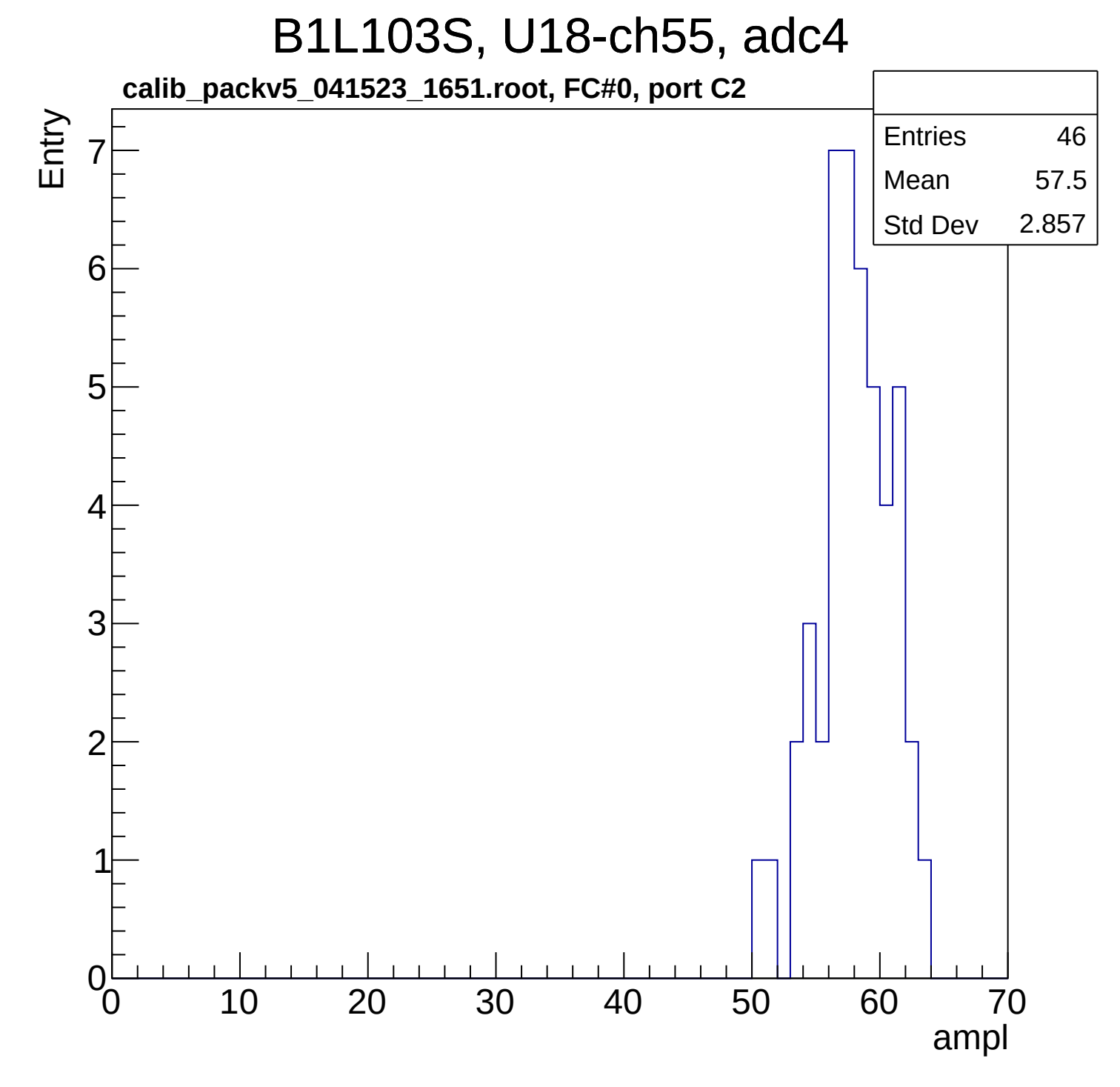
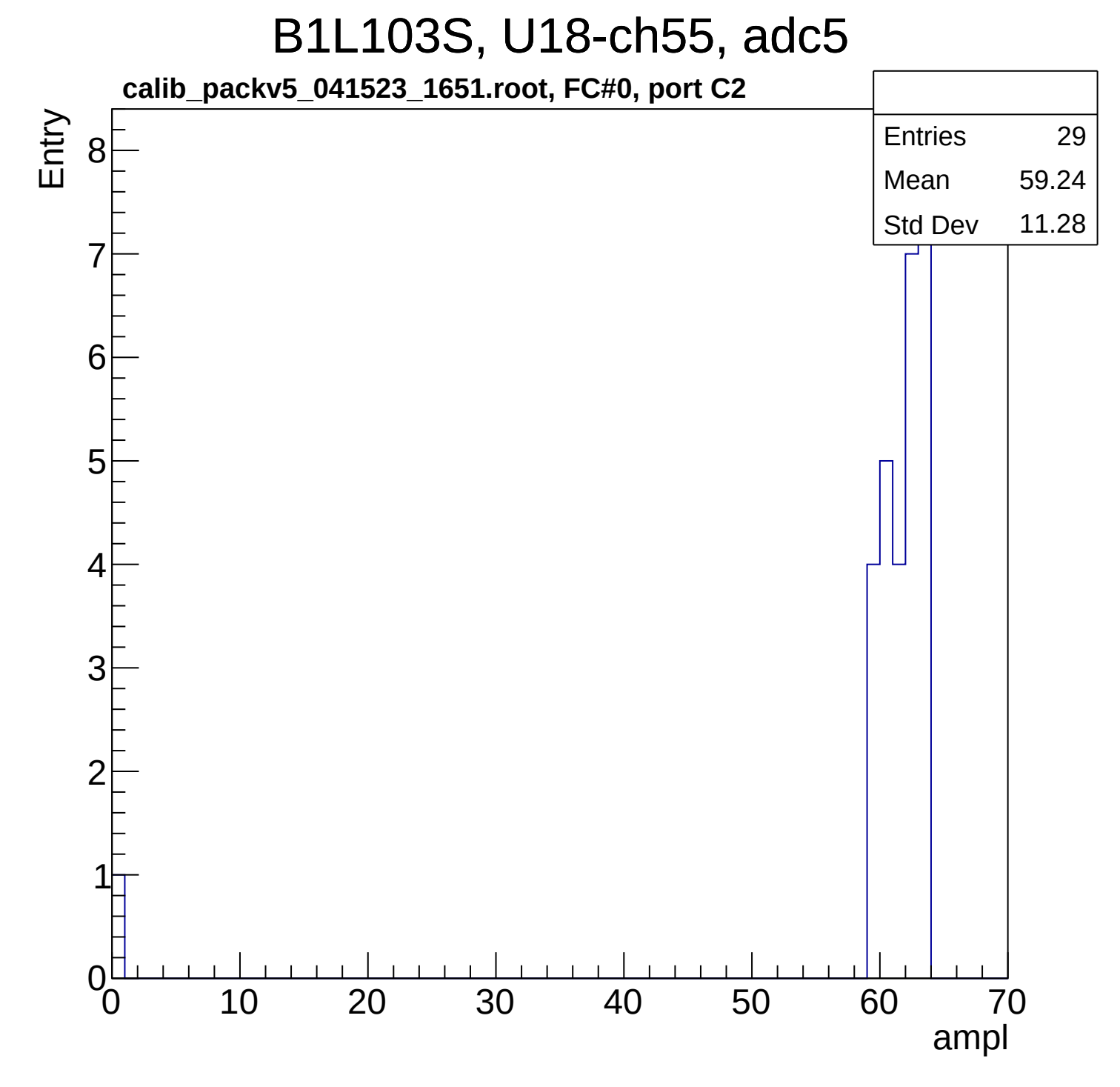
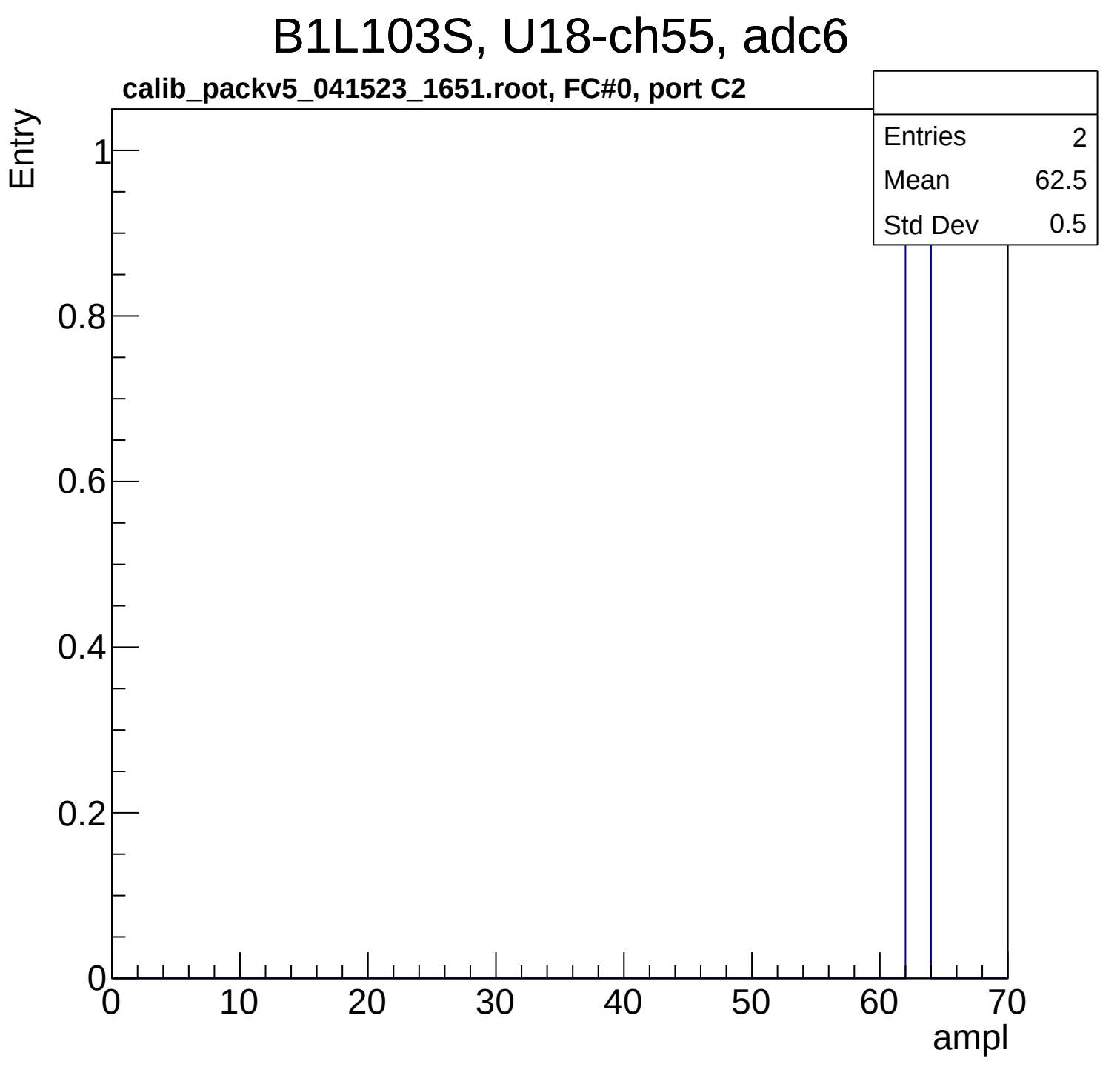
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U18-ch55, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 57.5
Std Dev 2.857
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U18-ch55, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 29
Mean 59.24
Std Dev 11.28
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch55, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 2
Mean 62.5
Std Dev 0.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
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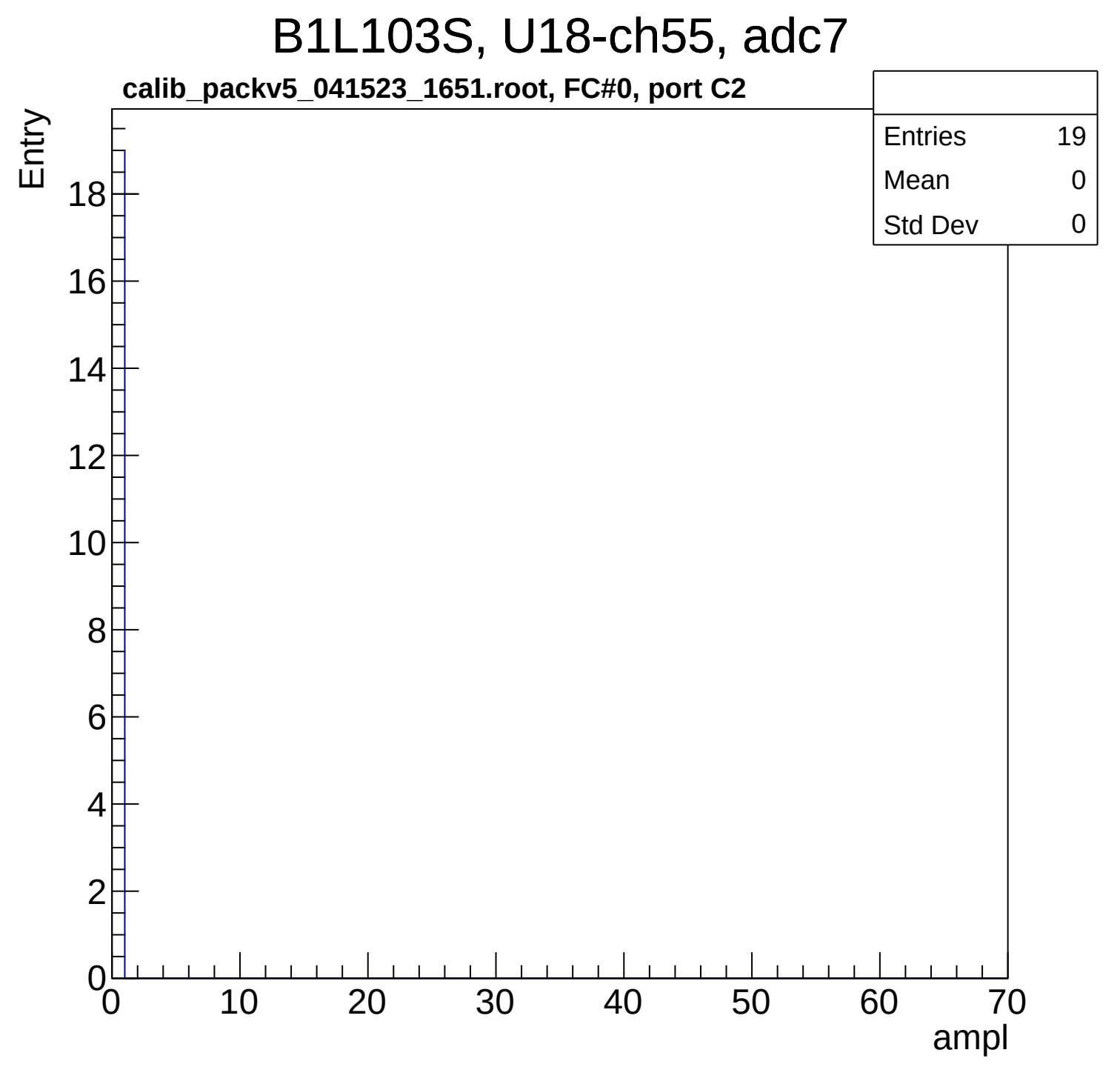
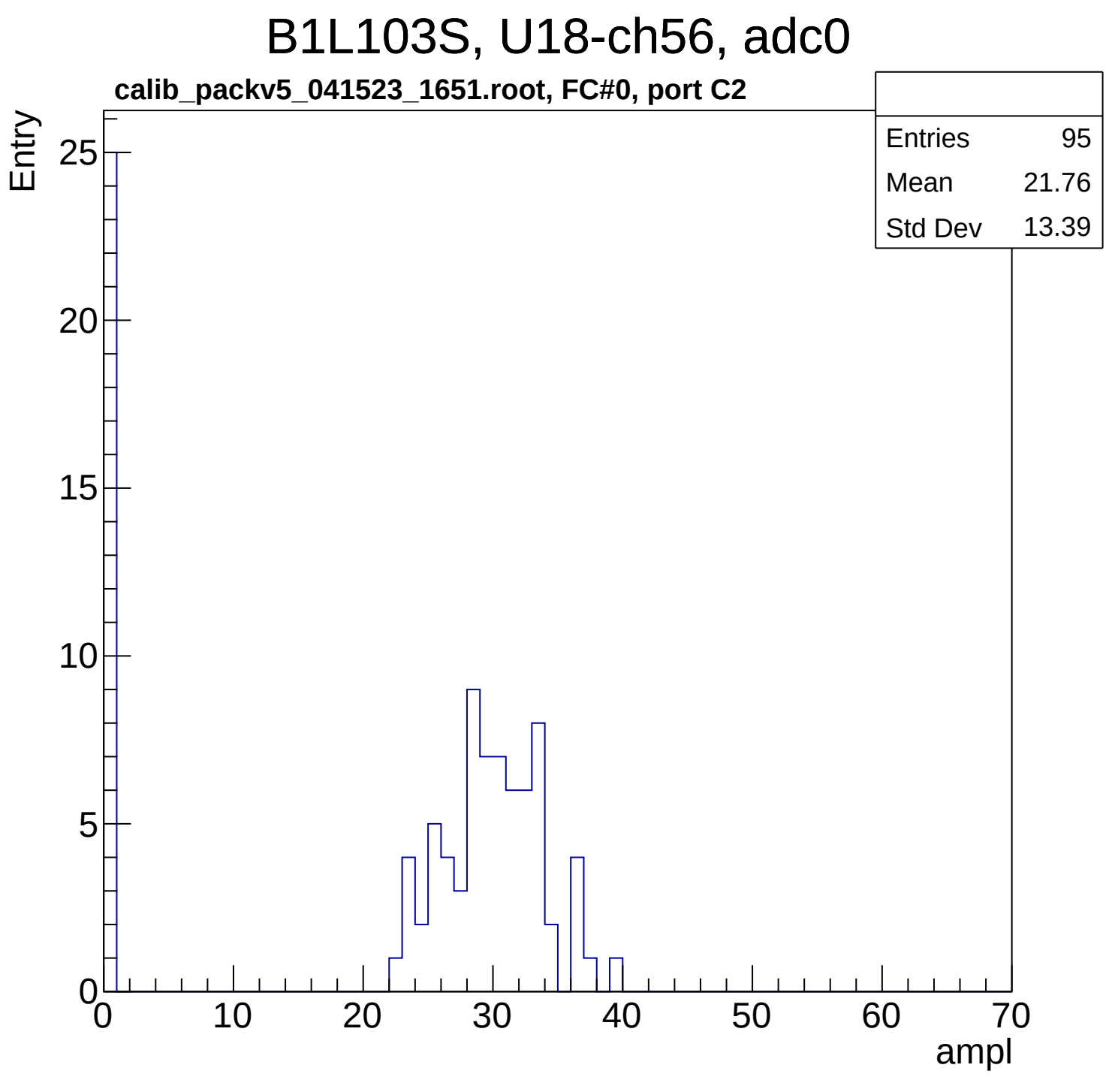
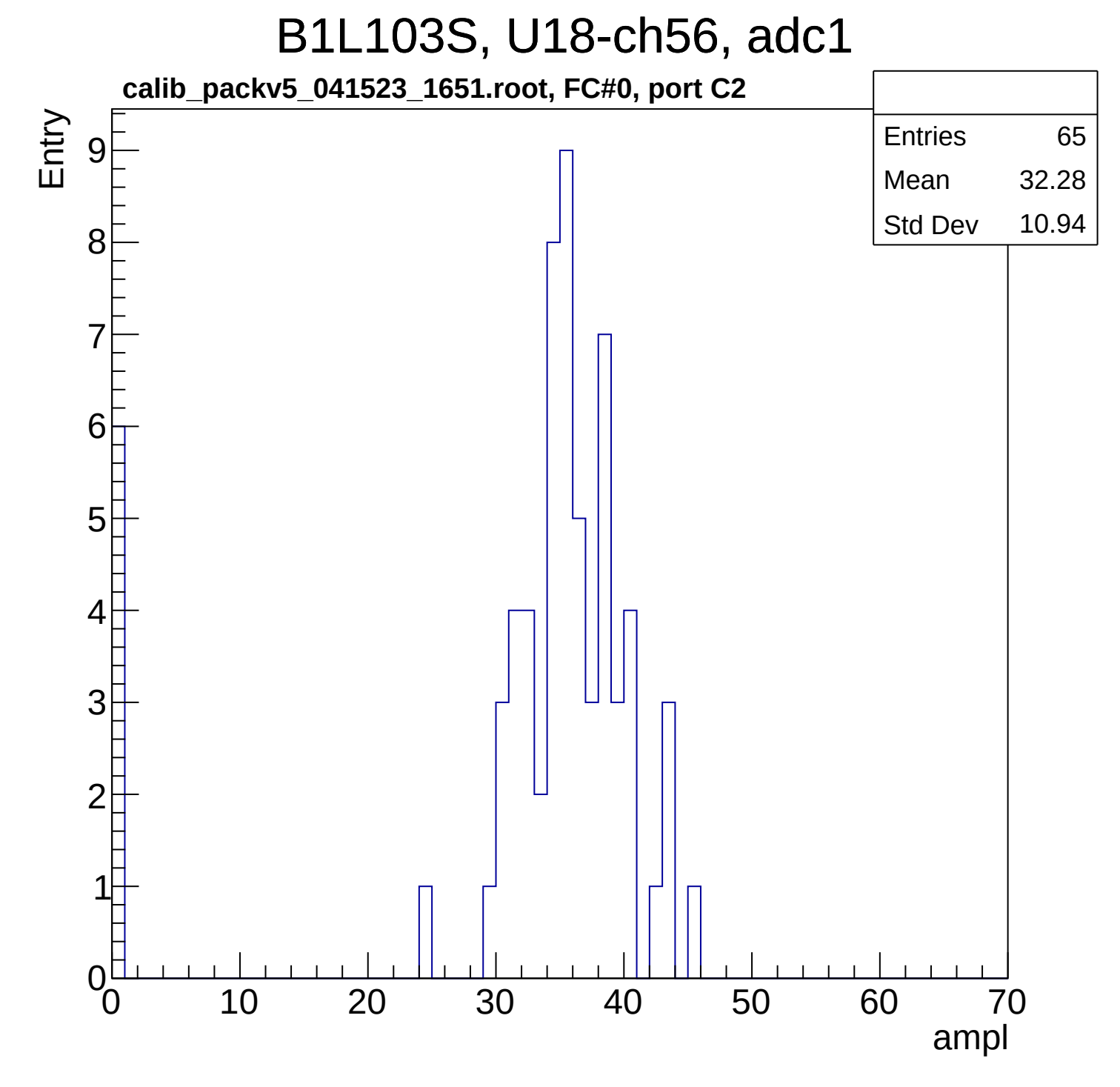
50
60
70
ampl


B1L103S, U18-ch55, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch56, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 95
Mean 21.76
Std Dev 13.39
Entry
0
5
10
15
20
25
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch56, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 32.28
Std Dev 10.94
Entry
ampl
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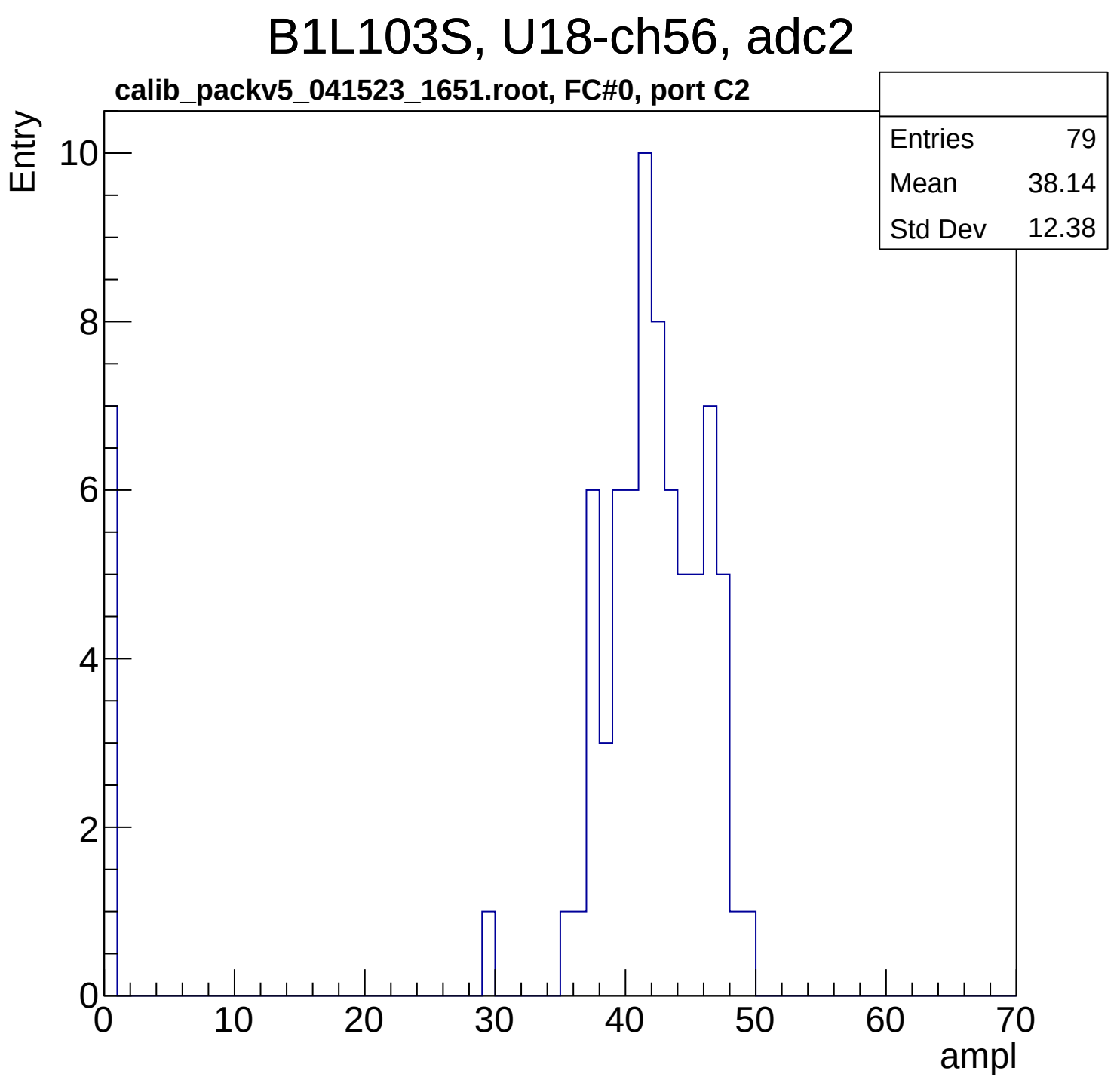
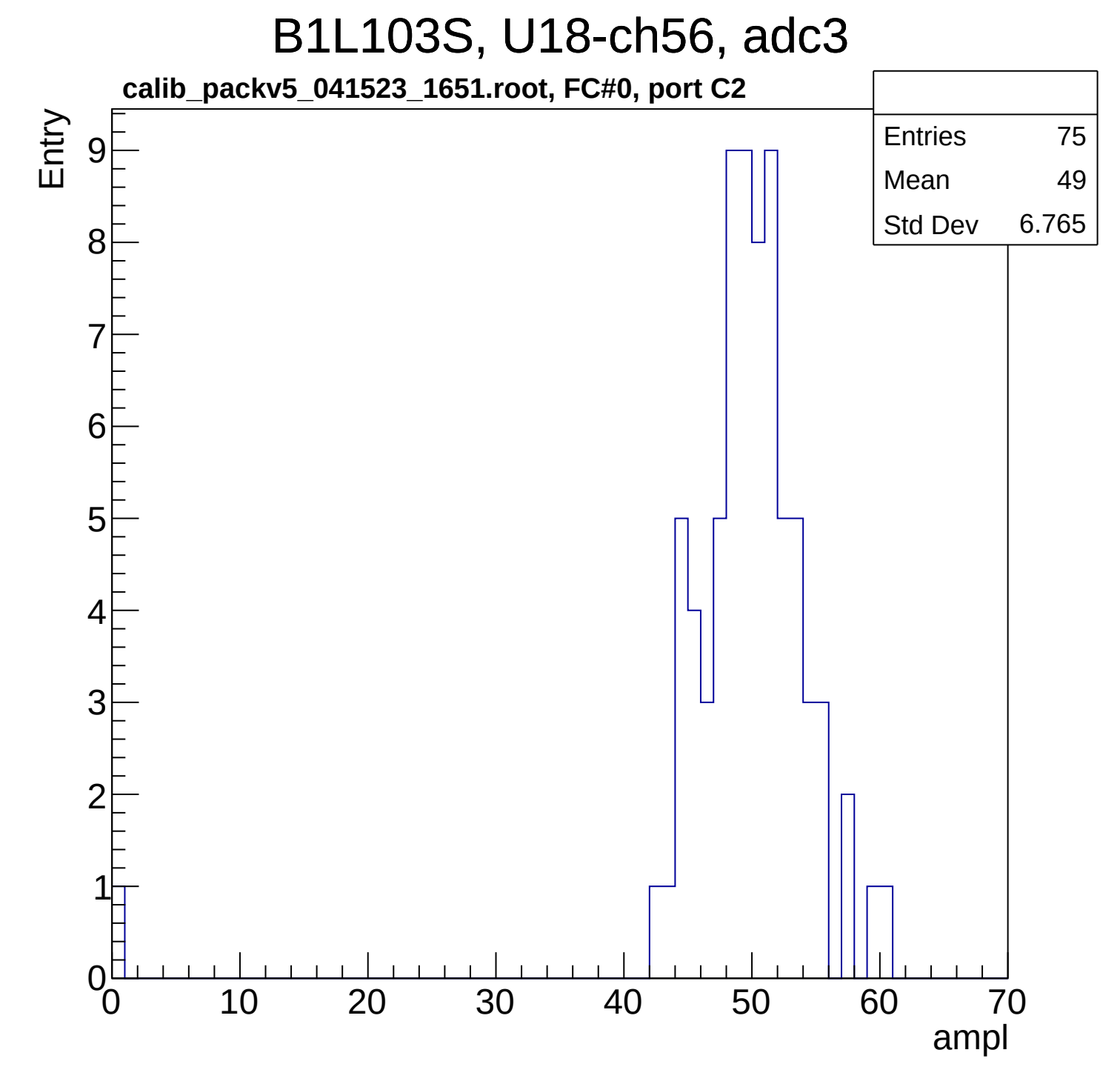
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U18-ch56, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 38.14
Std Dev 12.38
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U18-ch56, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 49
Std Dev 6.765
Entry
ampl
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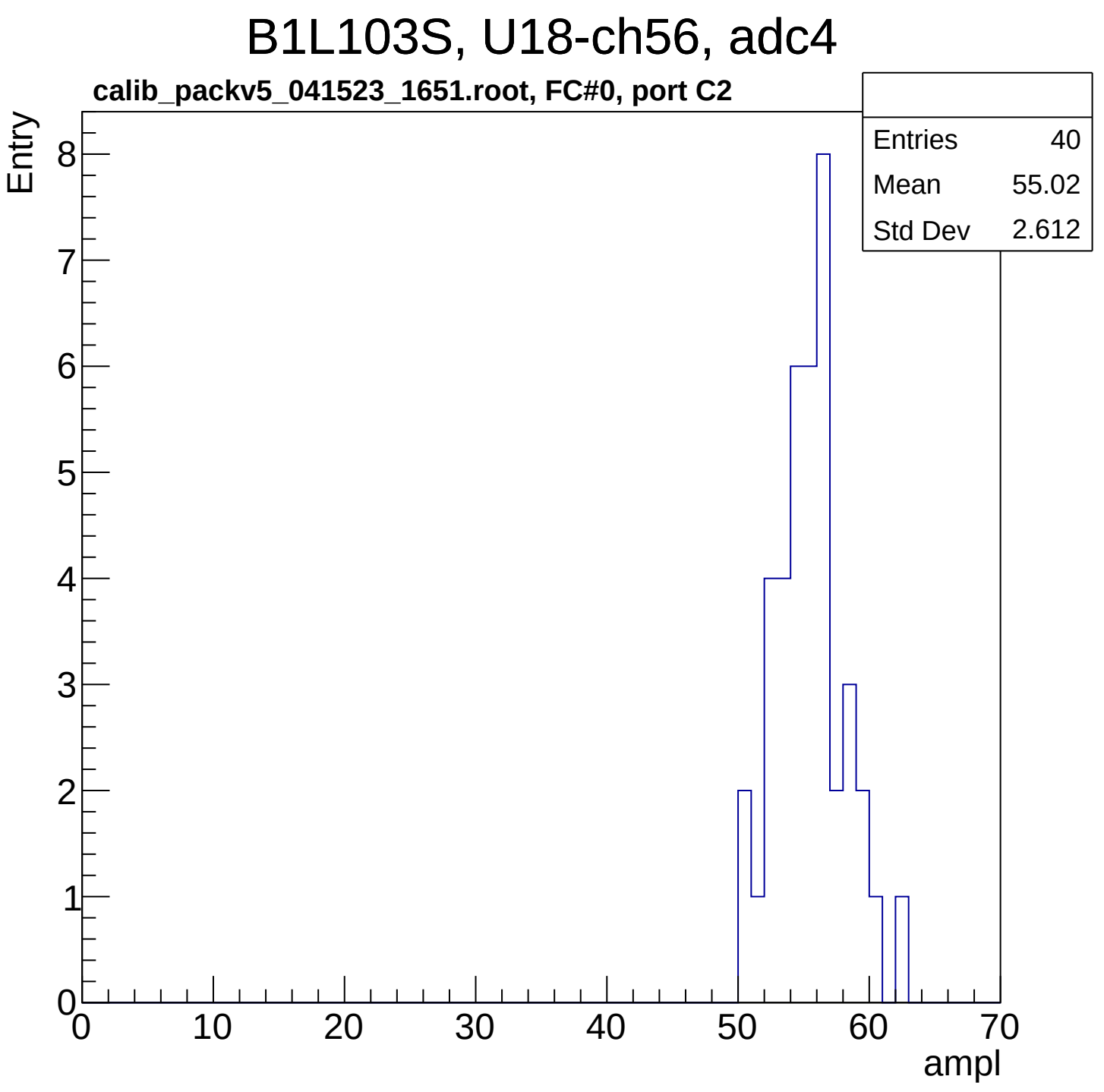
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U18-ch56, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 40
Mean 55.02
Std Dev 2.612
Entry
ampl
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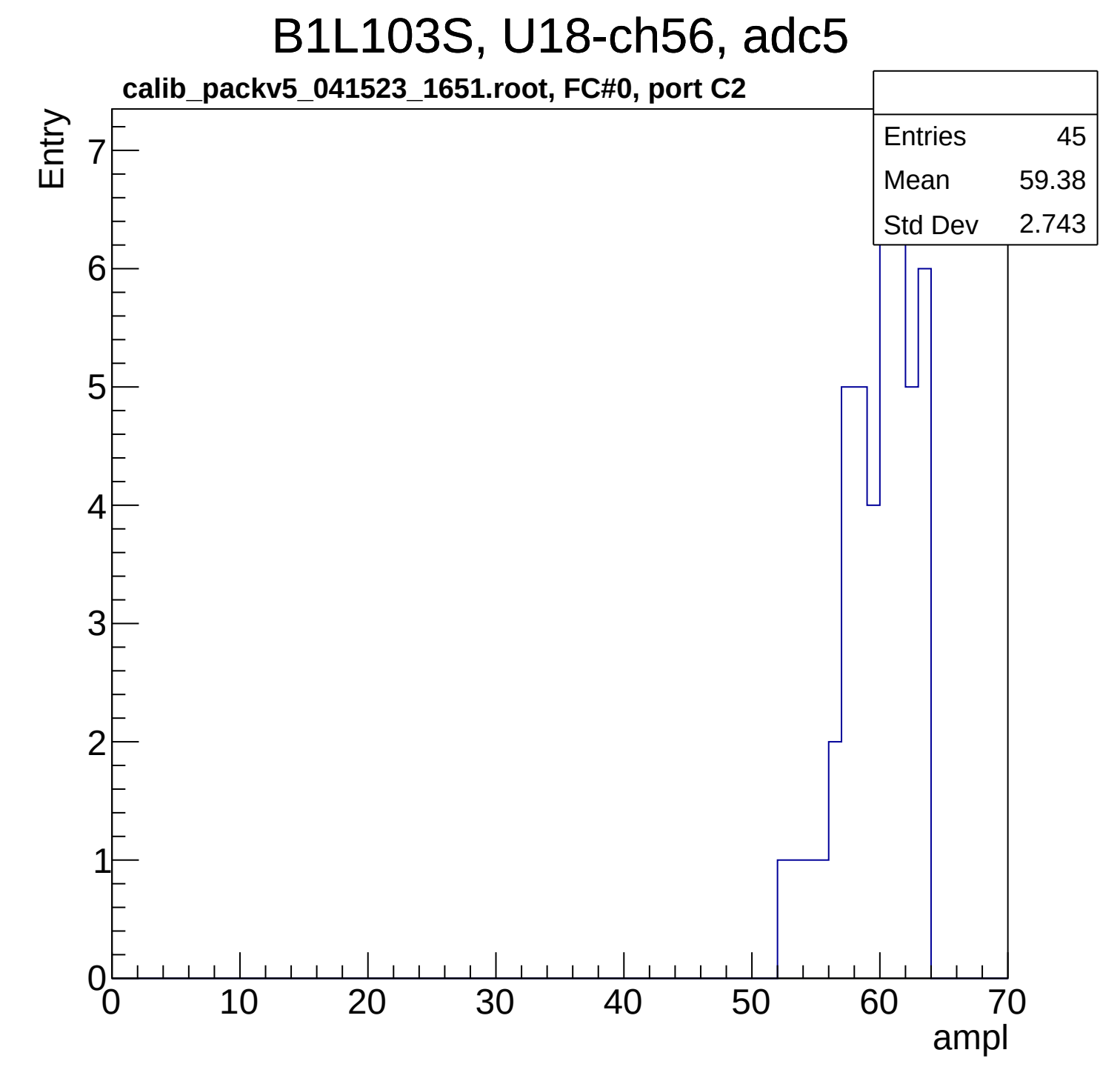
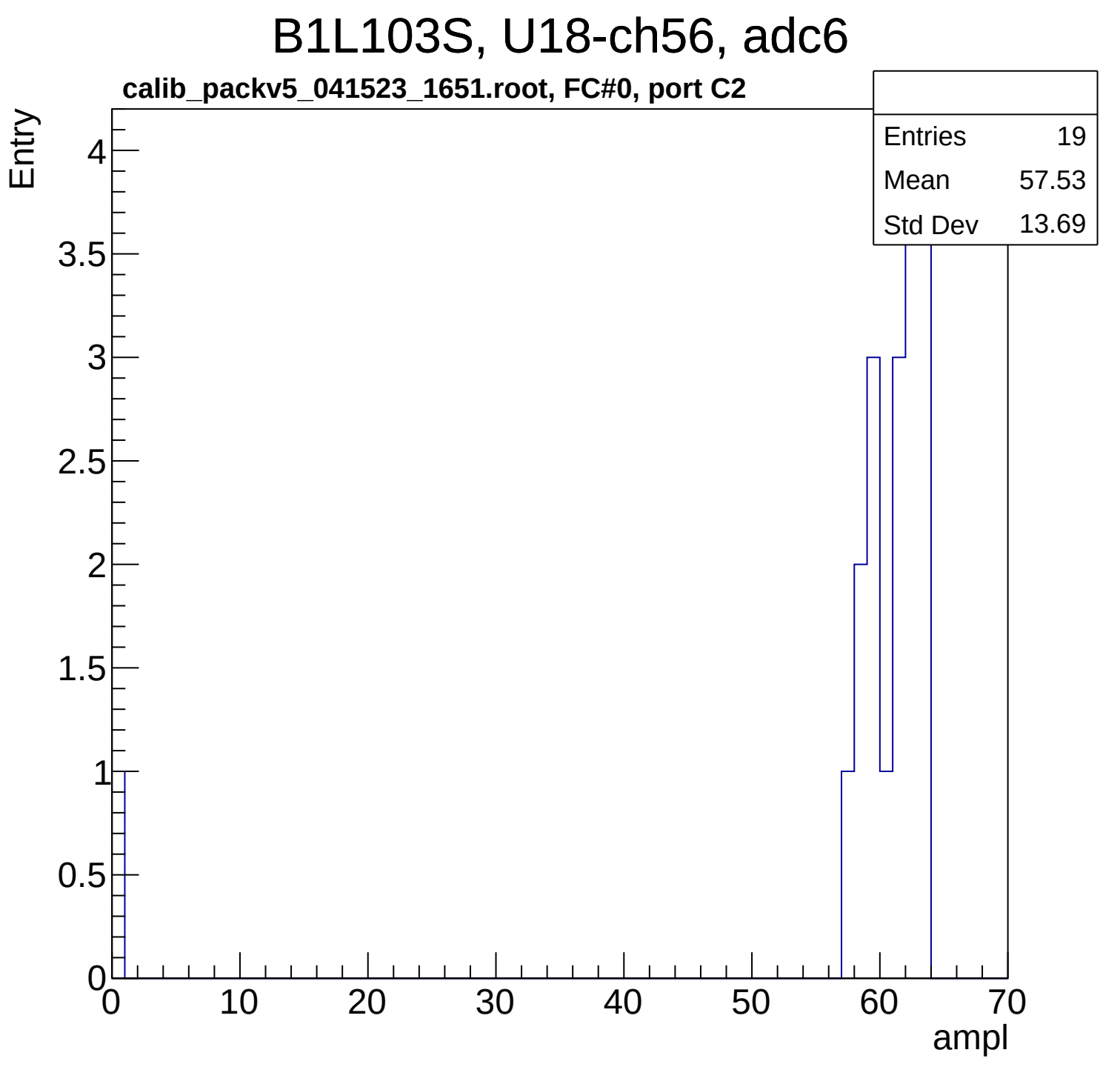
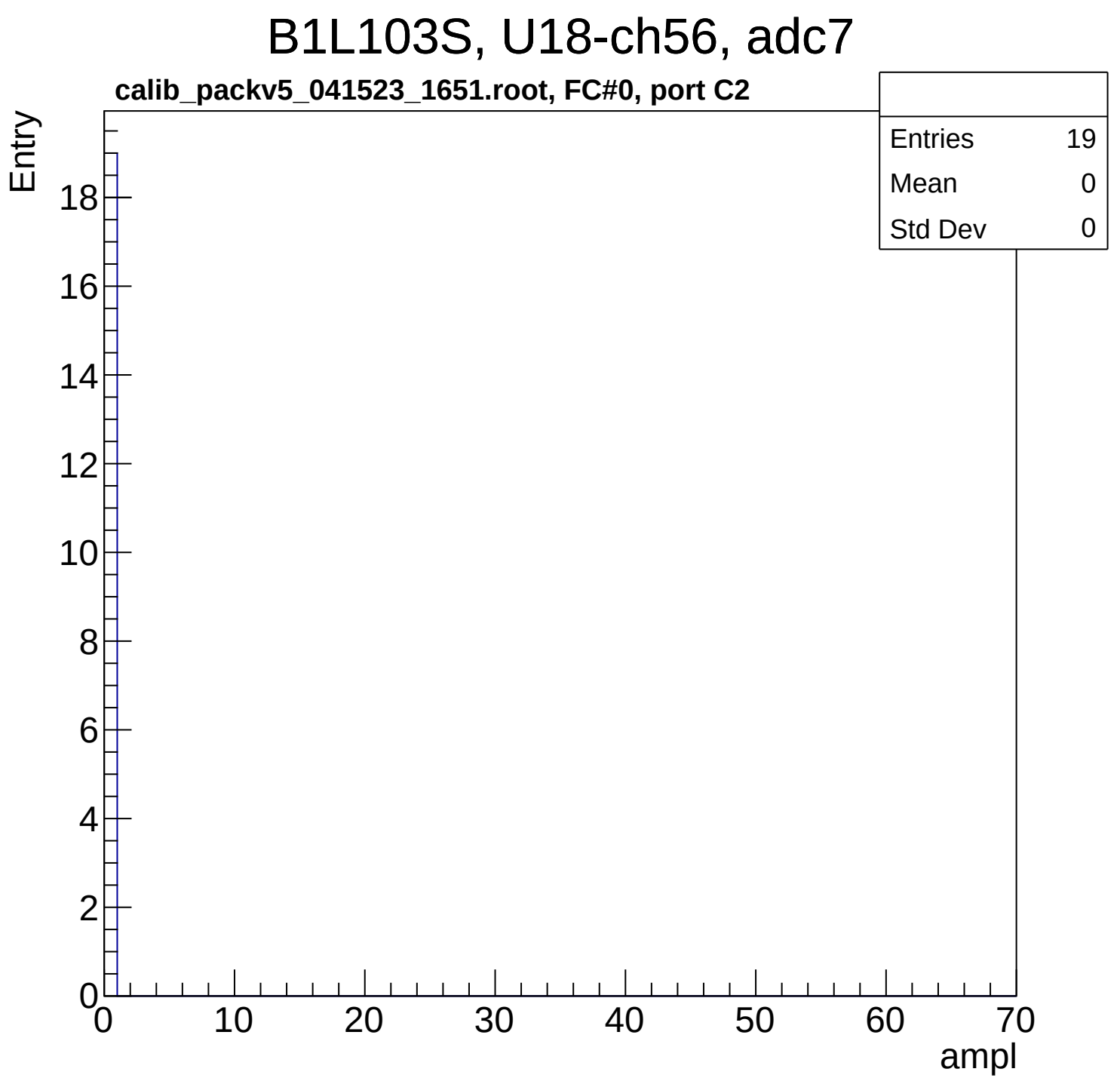
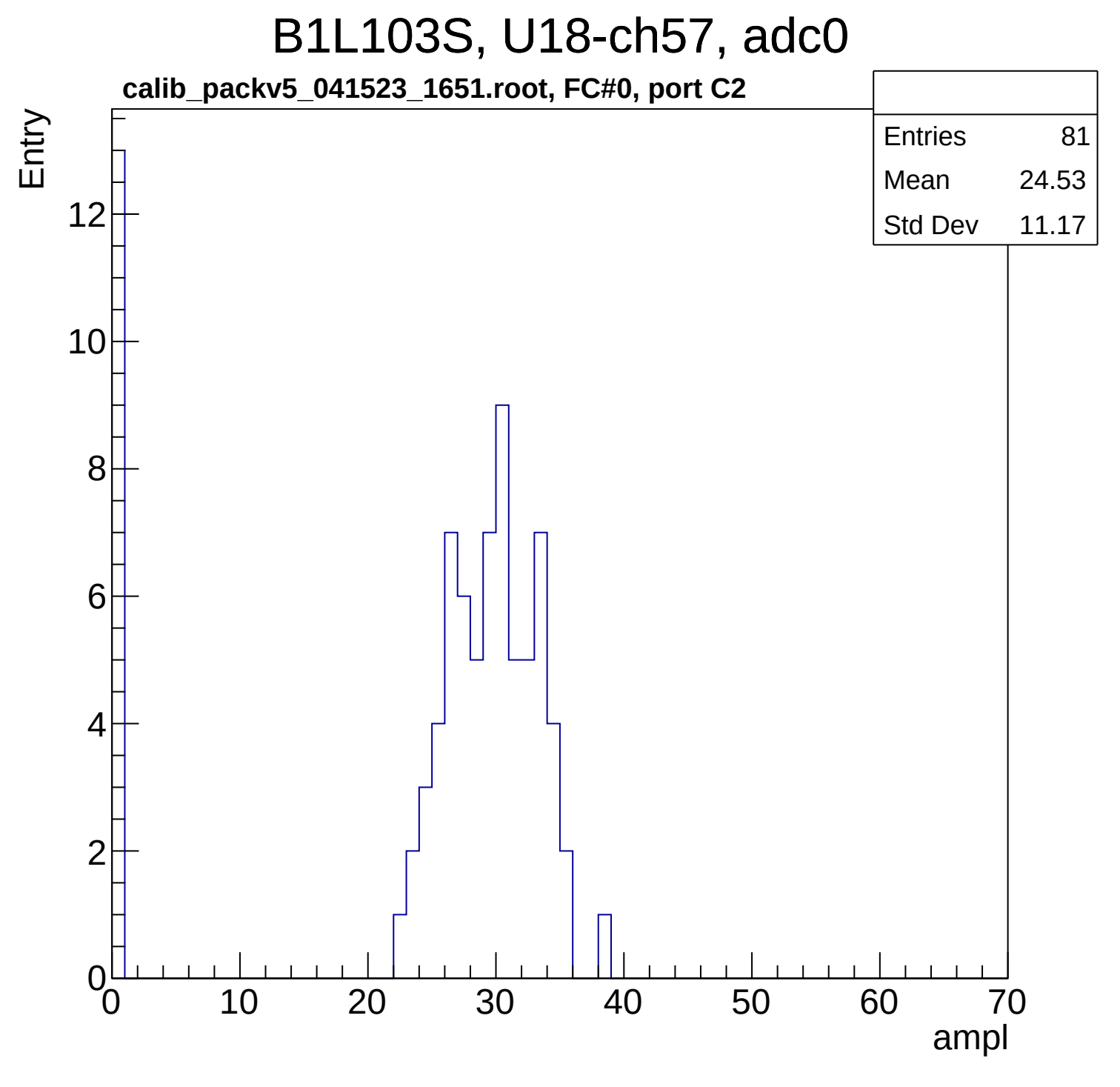
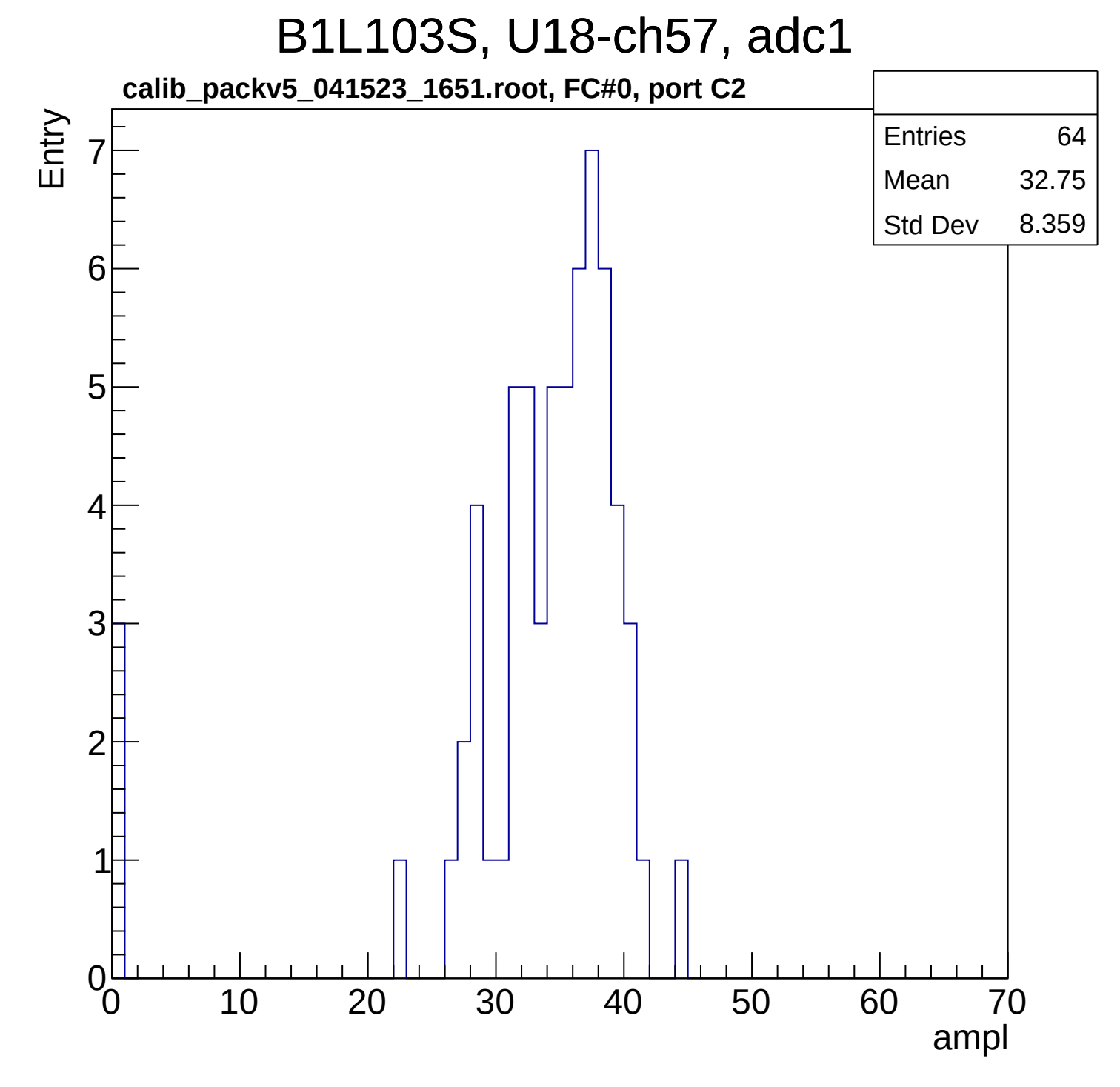
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch56, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 59.38
Std Dev 2.743
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U18-ch56, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 57.53
Std Dev 13.69
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U18-ch56, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch57, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 24.53
Std Dev 11.17
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch57, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 32.75
Std Dev 8.359
Entry
ampl
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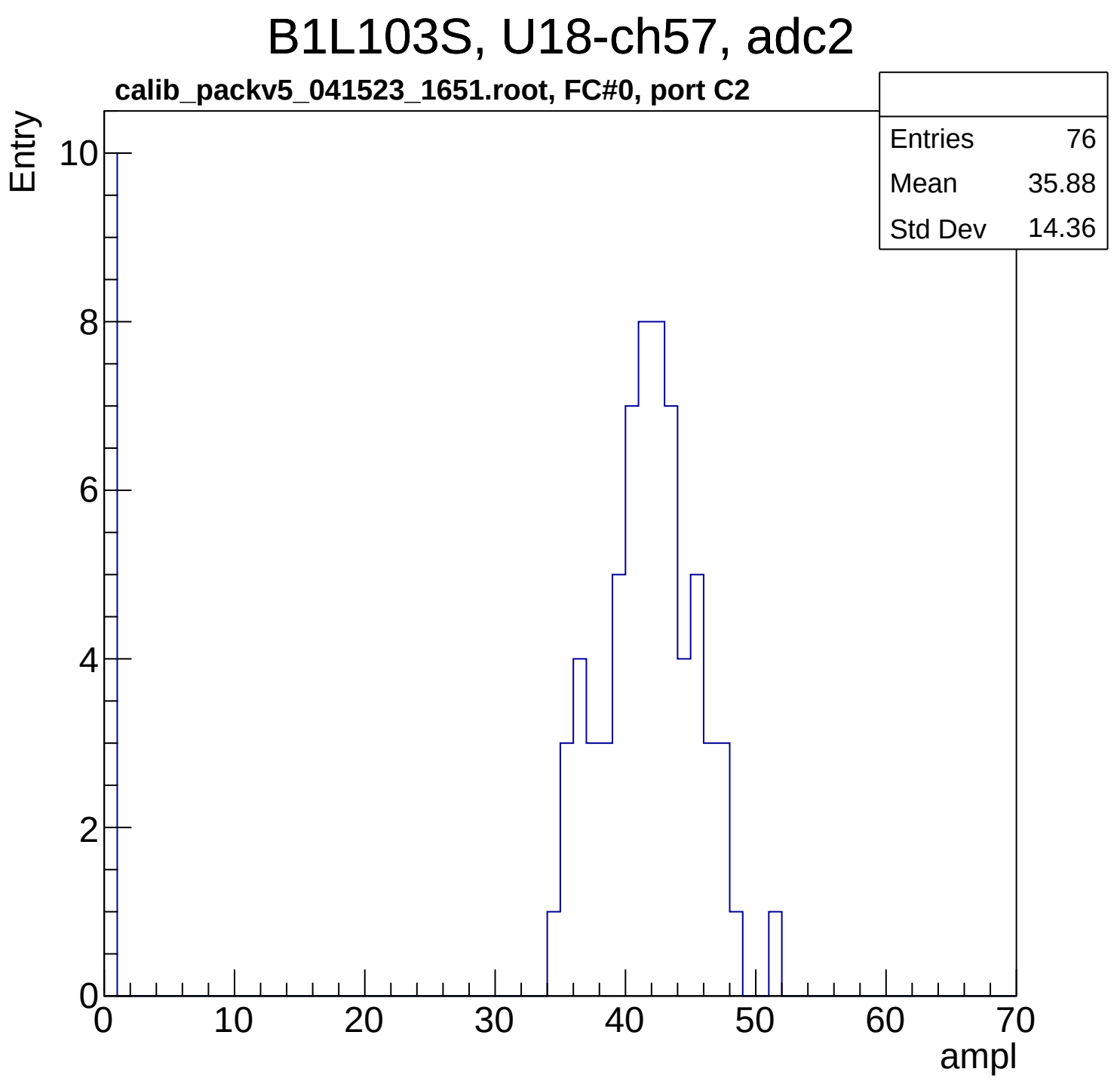
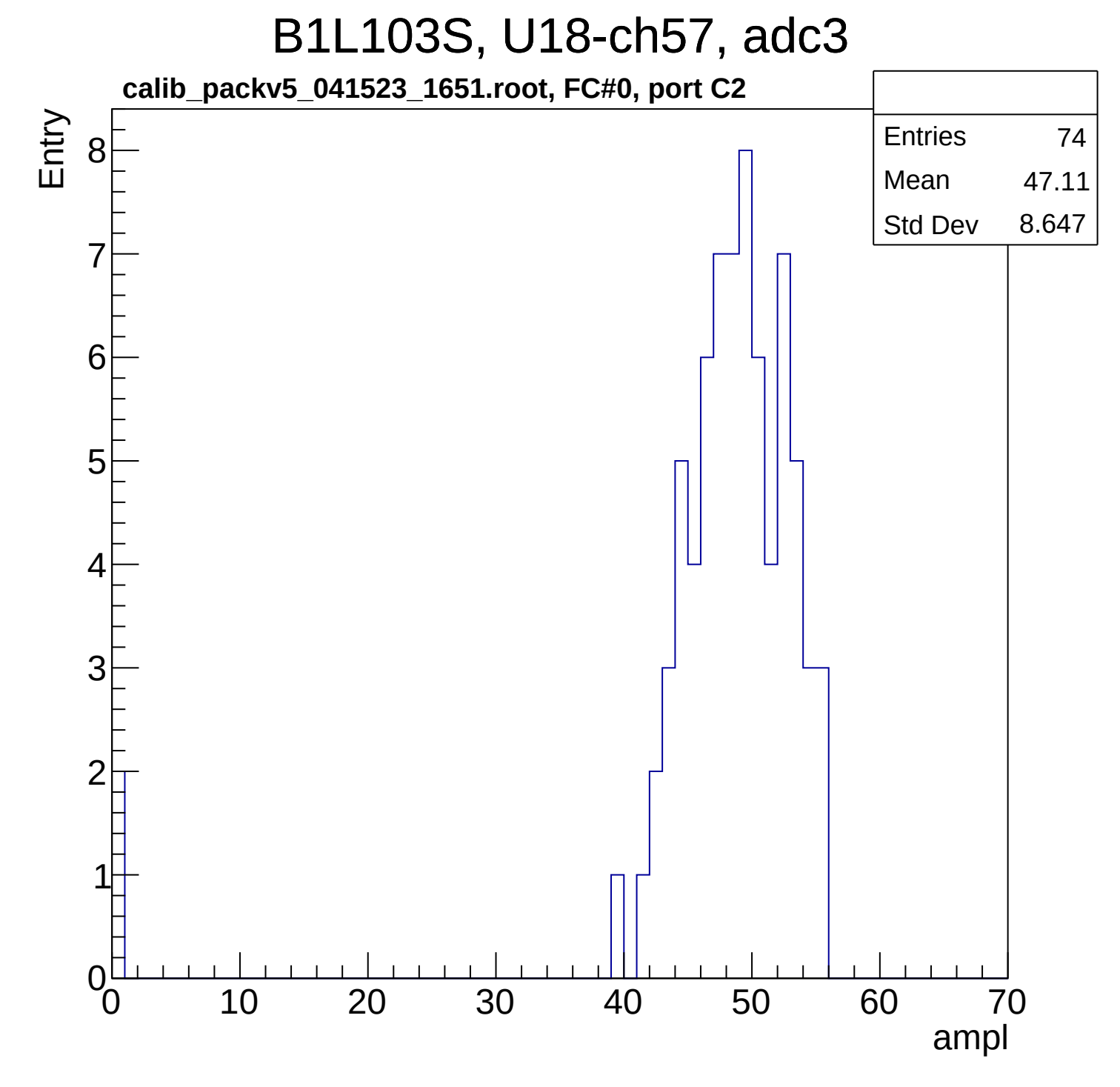
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U18-ch57, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 35.88
Std Dev 14.36
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U18-ch57, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 47.11
Std Dev 8.647
Entry
ampl
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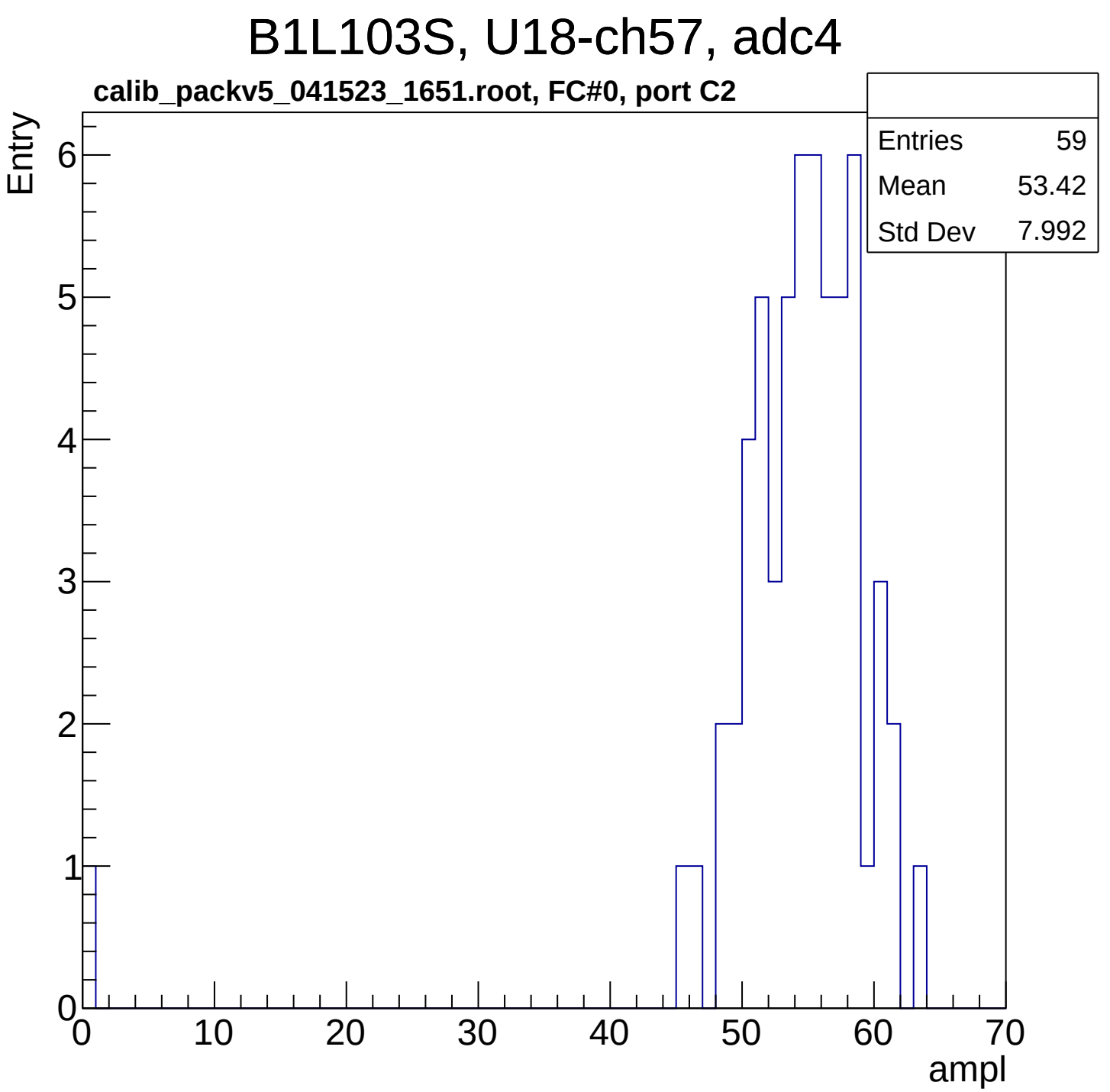
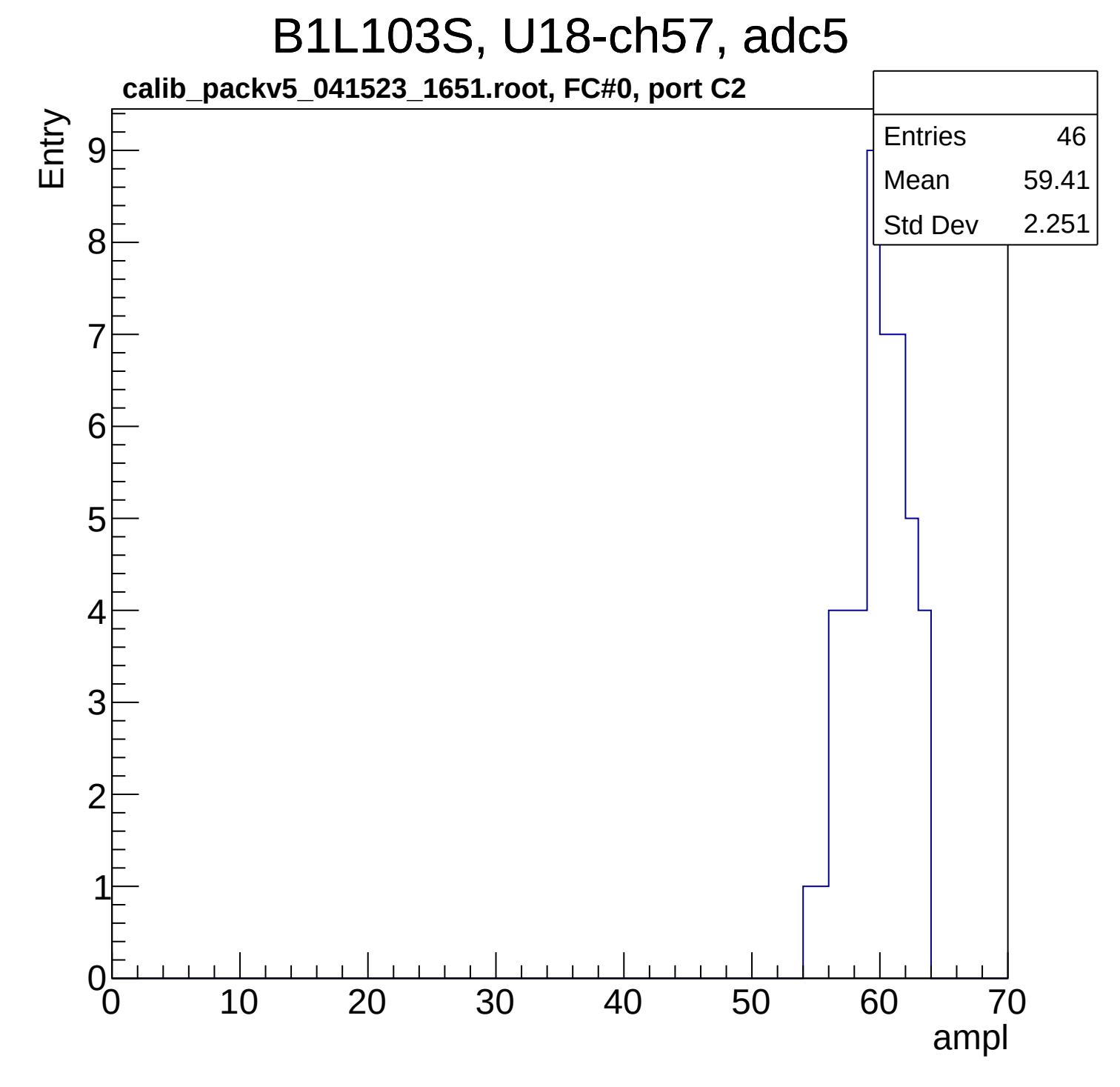
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch57, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 53.42
Std Dev 7.992
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U18-ch57, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 59.41
Std Dev 2.251
Entry
ampl
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2
3
4
5
6
7
8
9
0
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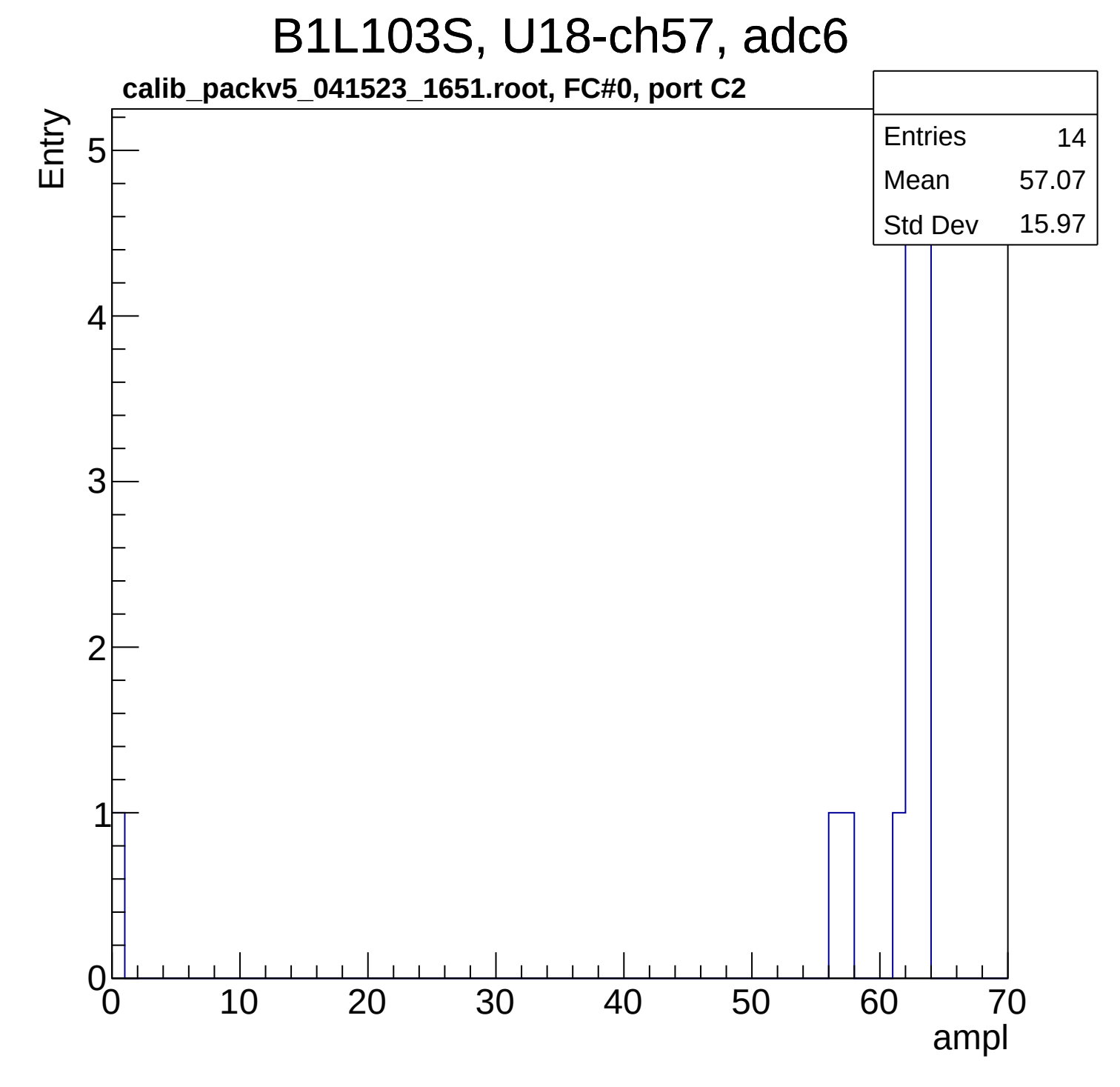
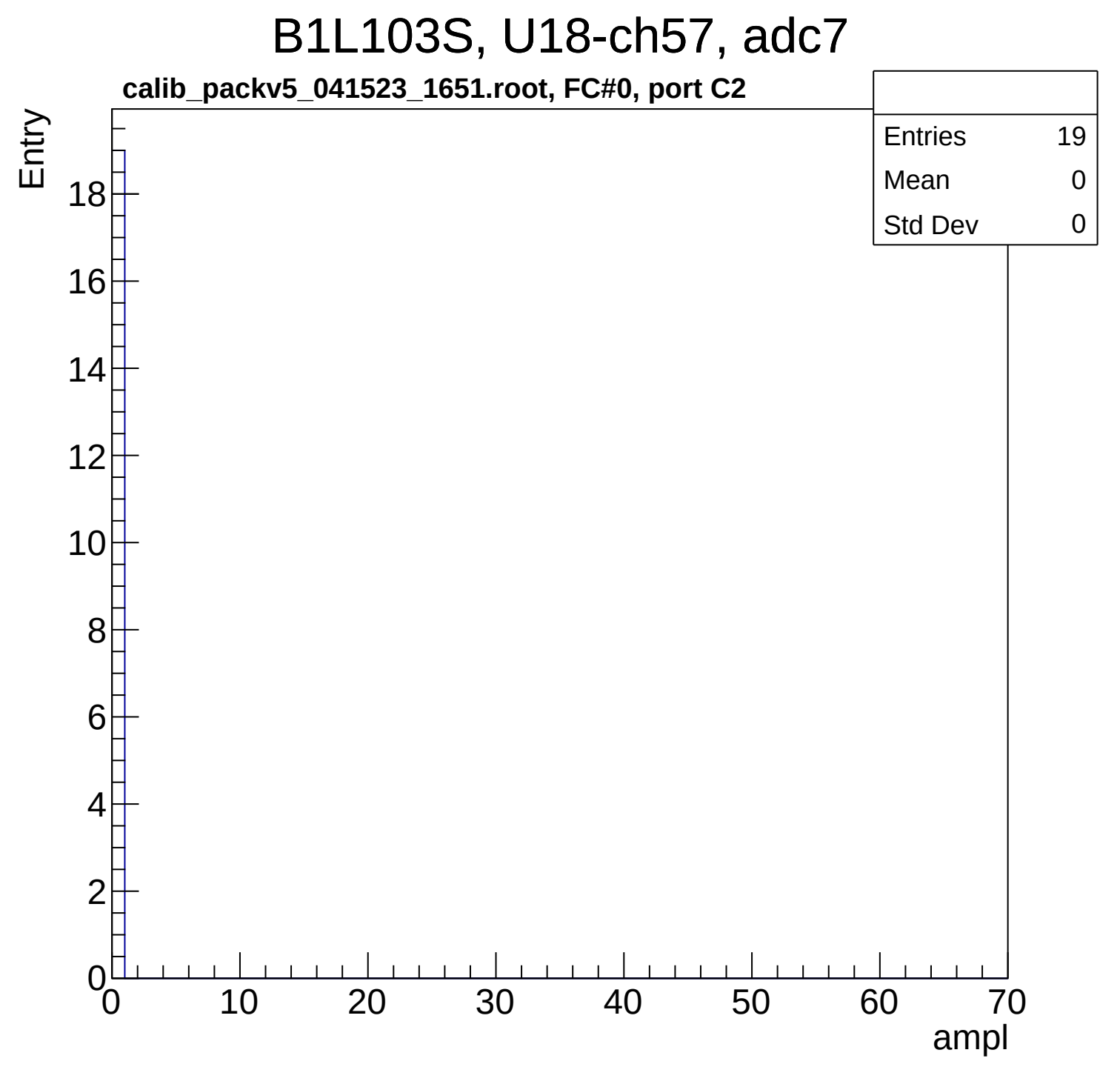
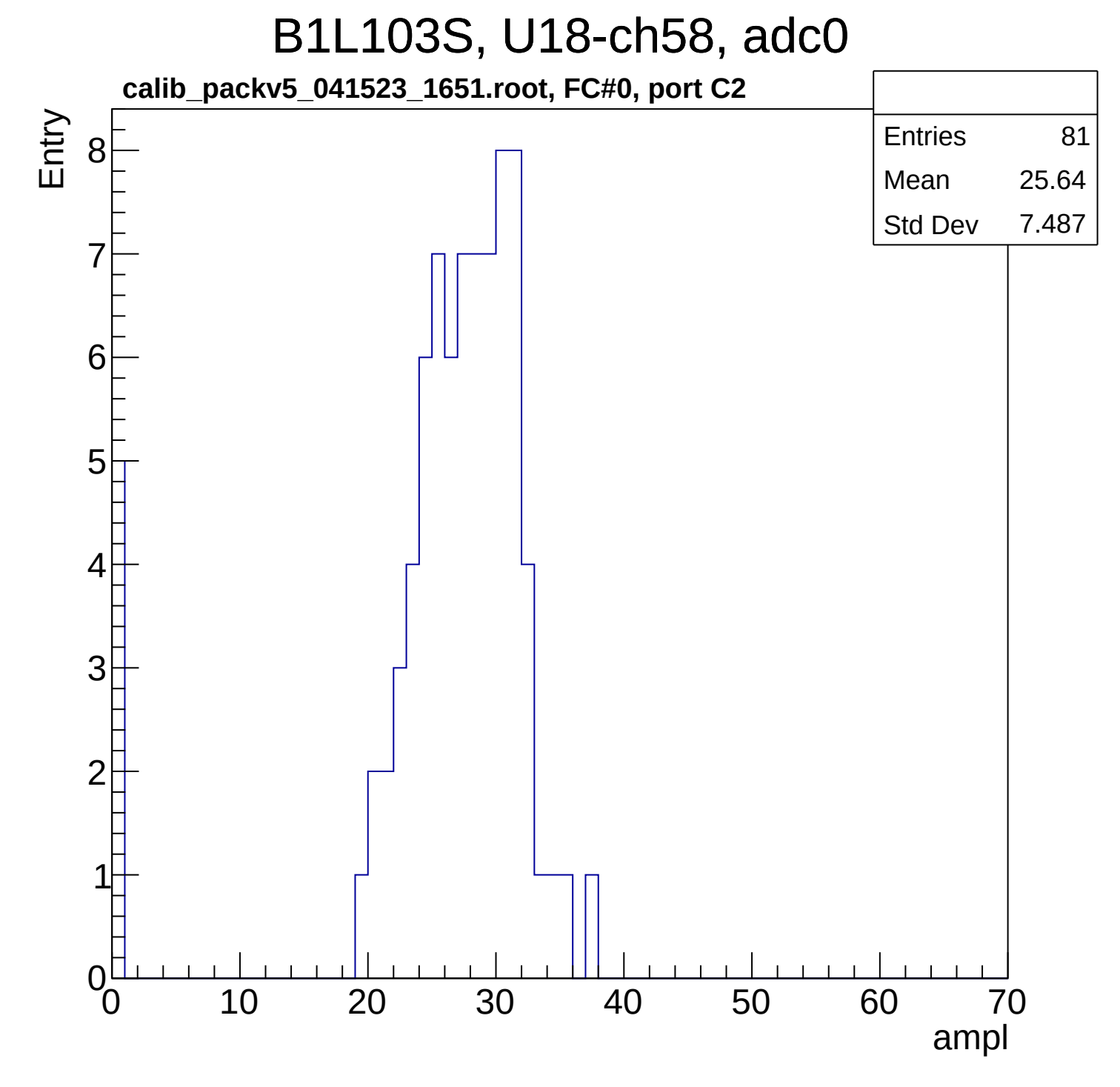
30
40
50
60
70


B1L103S, U18-ch57, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 14
Mean 57.07
Std Dev 15.97
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U18-ch57, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch58, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 25.64
Std Dev 7.487
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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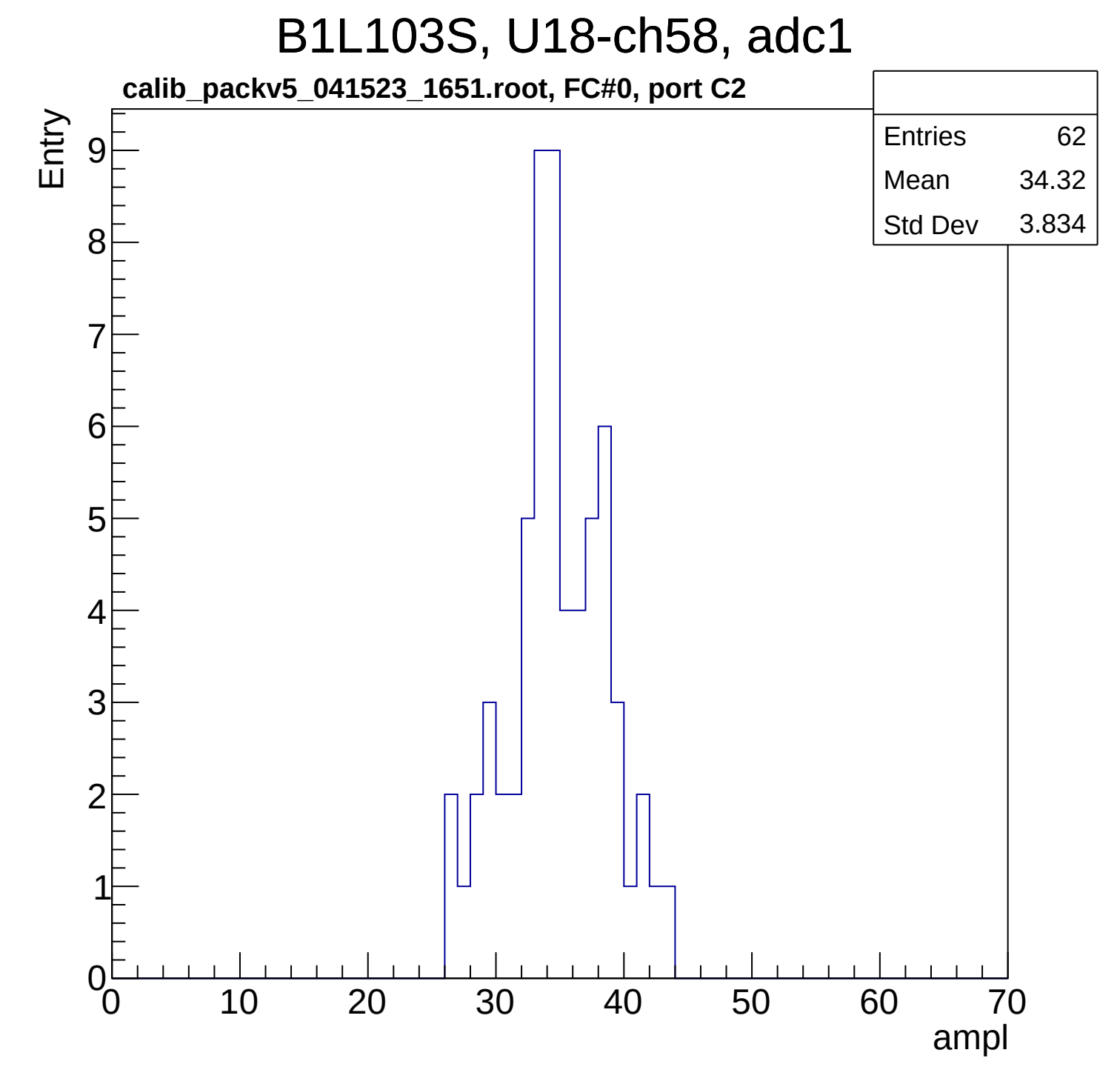
40
50
60
70


B1L103S, U18-ch58, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 34.32
Std Dev 3.834
Entry
ampl
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2
3
4
5
6
7
8
9
0
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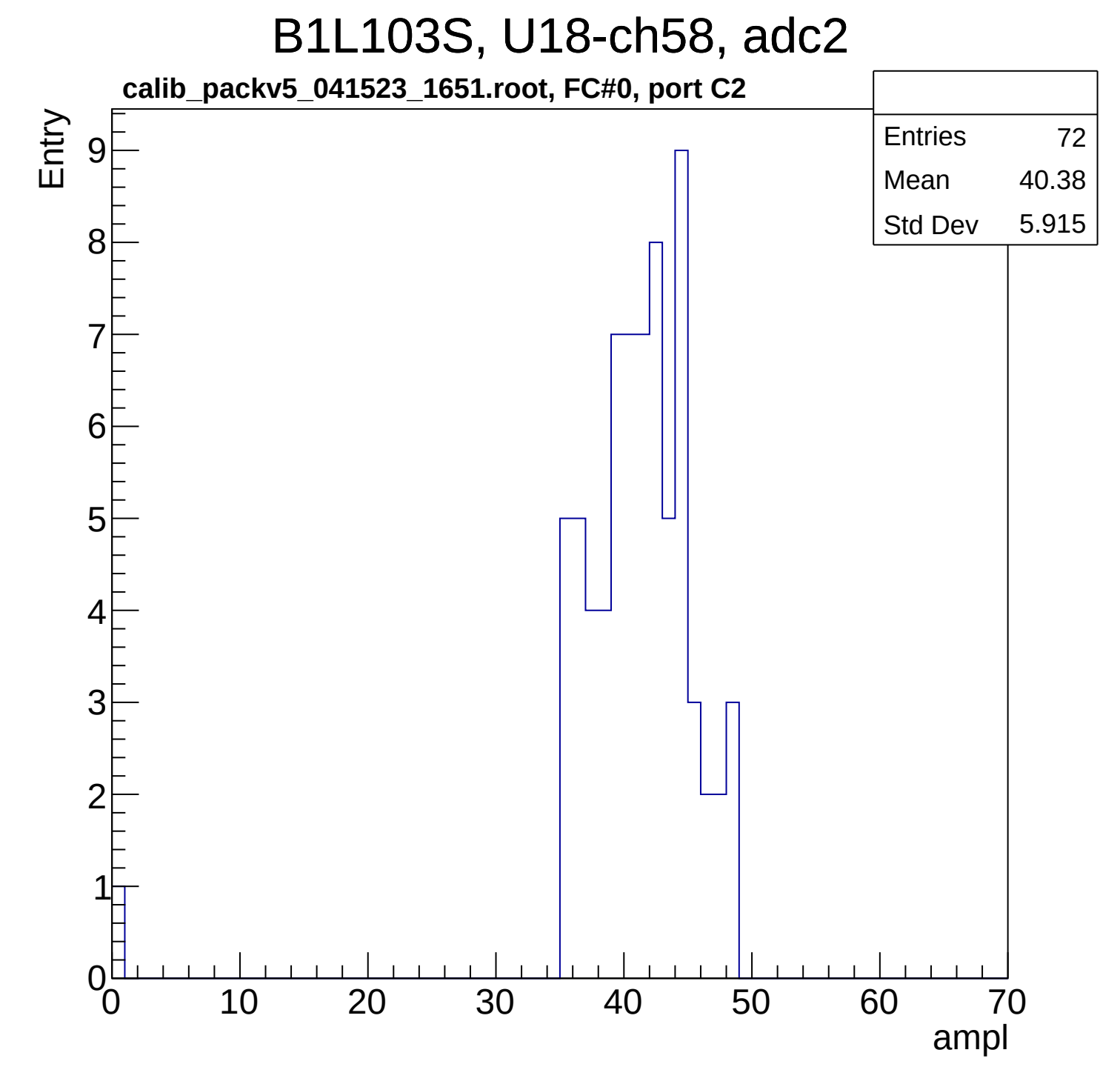
20
30
40
50
60
70


B1L103S, U18-ch58, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 40.38
Std Dev 5.915
Entry
ampl
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2
3
4
5
6
7
8
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0
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20
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40
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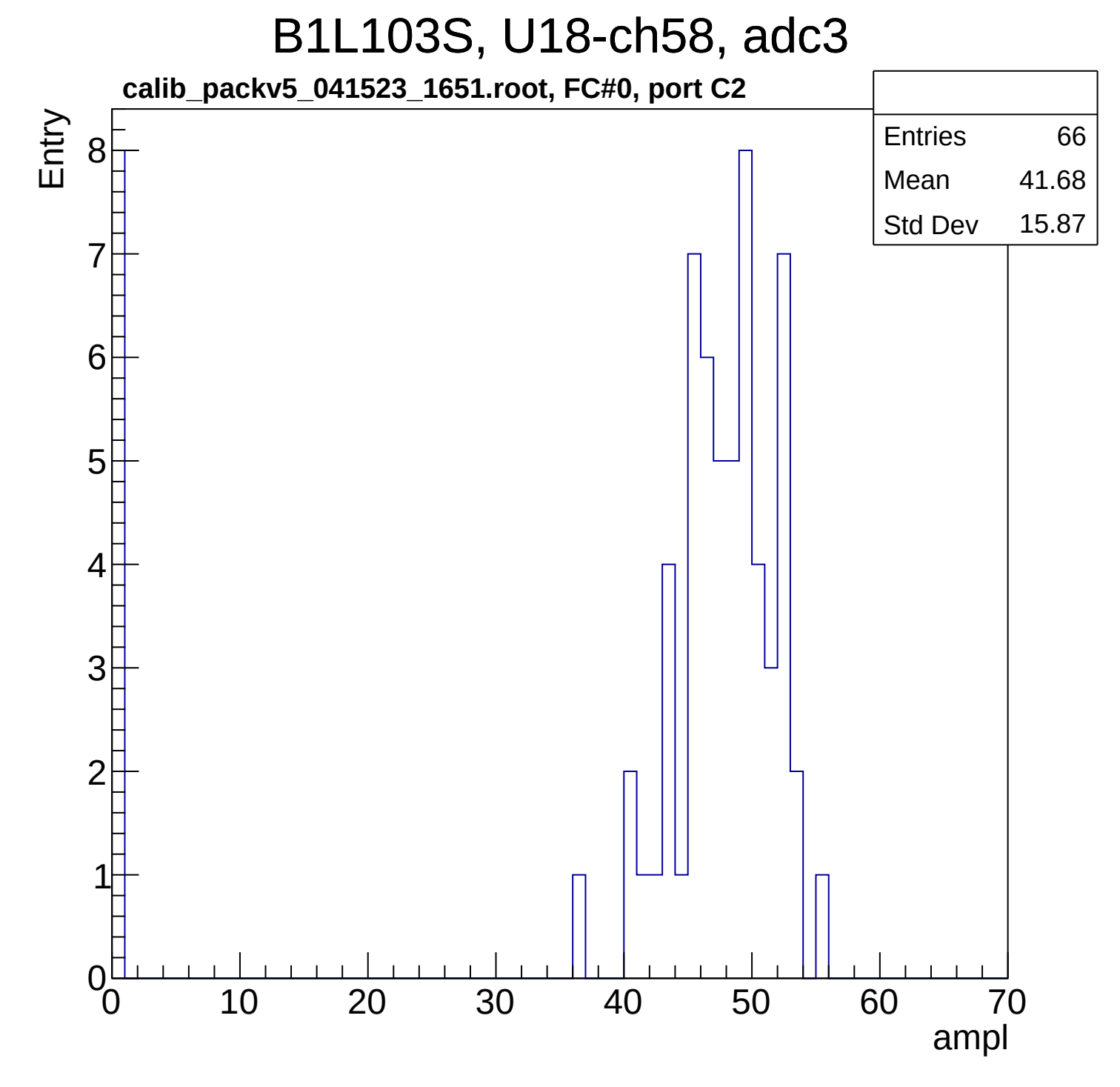
60
70


B1L103S, U18-ch58, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 41.68
Std Dev 15.87
Entry
ampl
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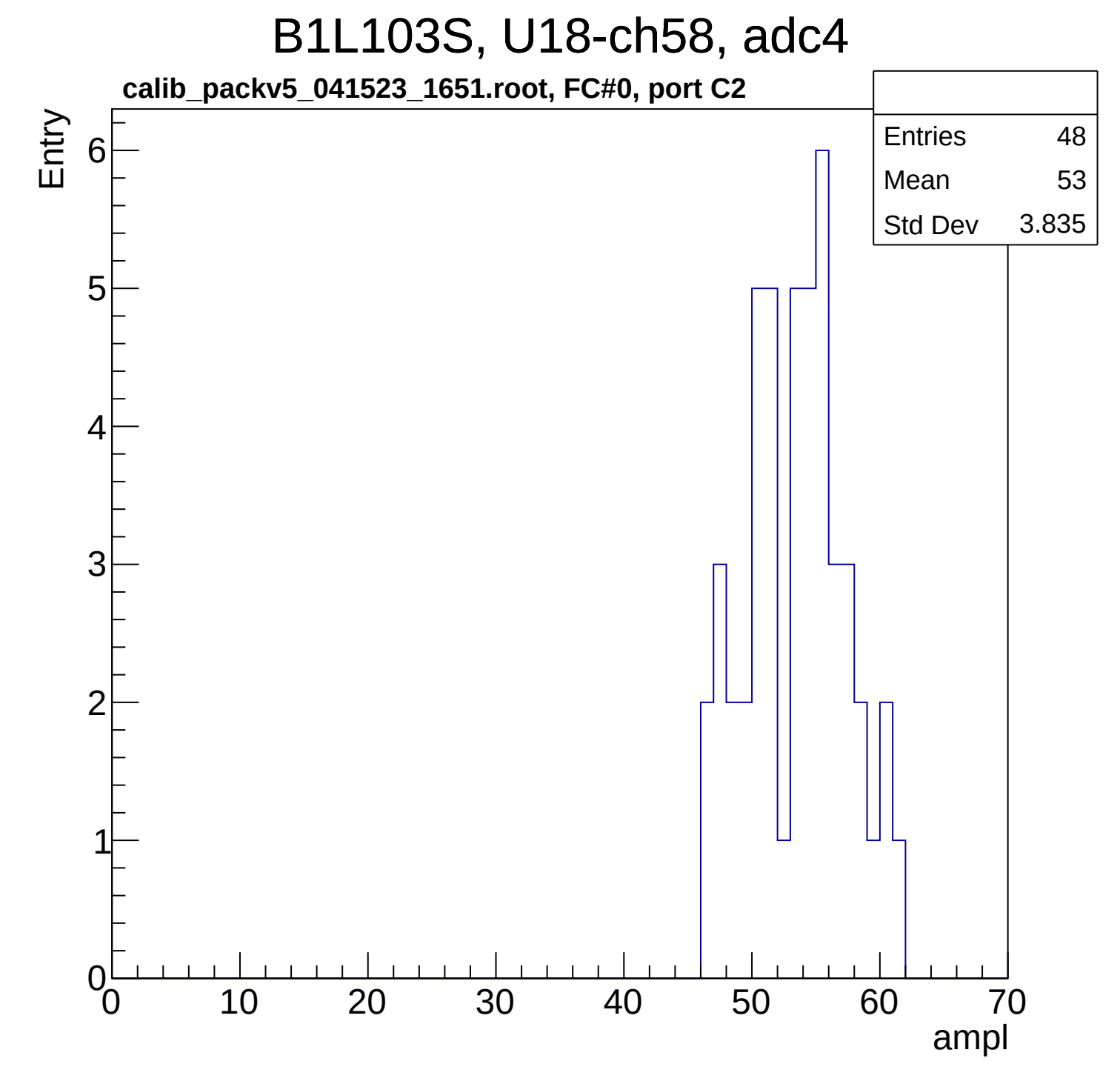
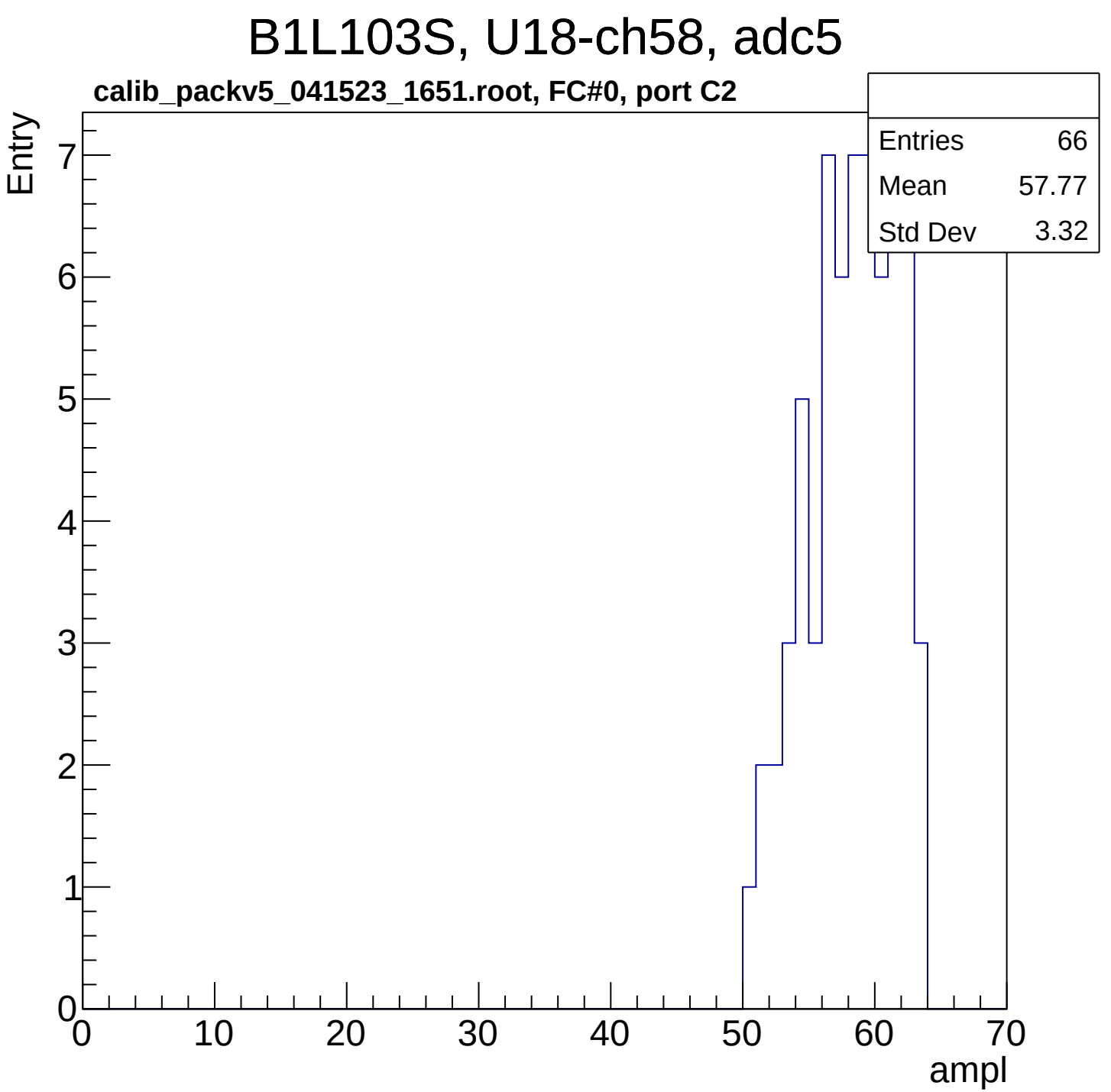
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch58, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 53
Std Dev 3.835
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U18-ch58, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 57.77
Std Dev 3.32
Entry
ampl
0
1
2
3
4
5
6
7
0
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20
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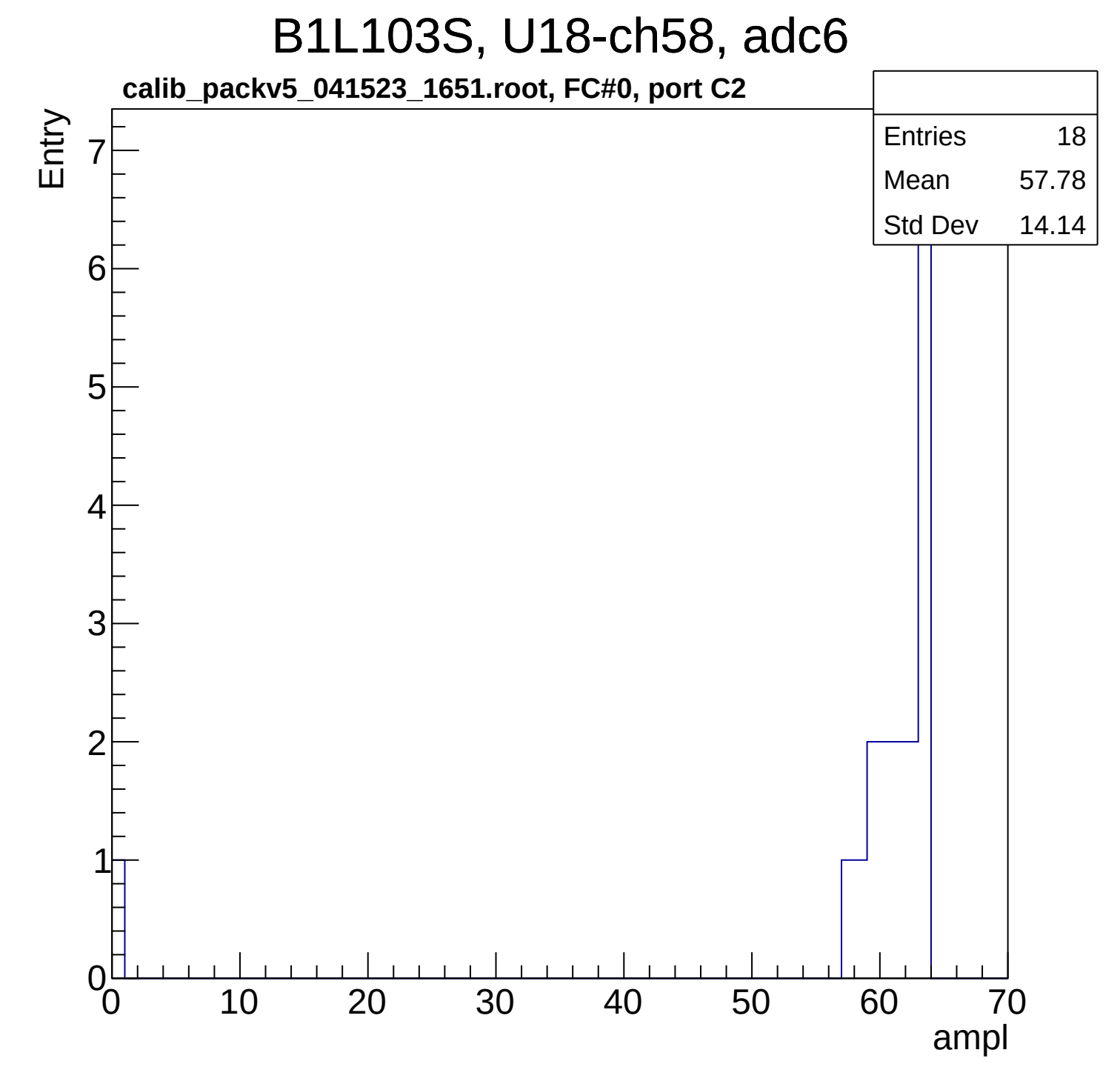
40
50
60
70


B1L103S, U18-ch58, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 57.78
Std Dev 14.14
Entry
ampl
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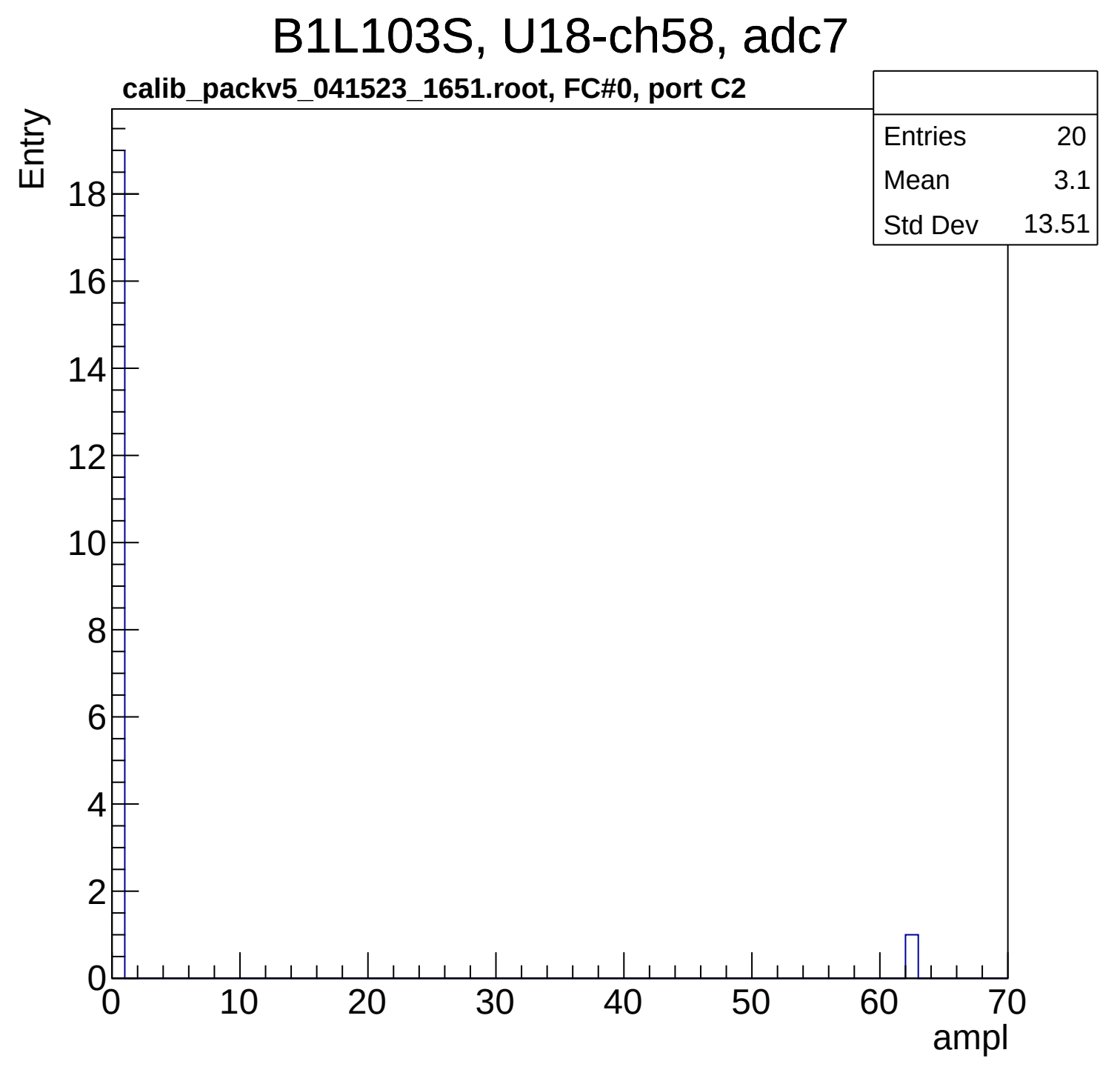
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U18-ch58, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.1
Std Dev 13.51
Entry
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4
6
8
10
12
14
16
18
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10
20
30
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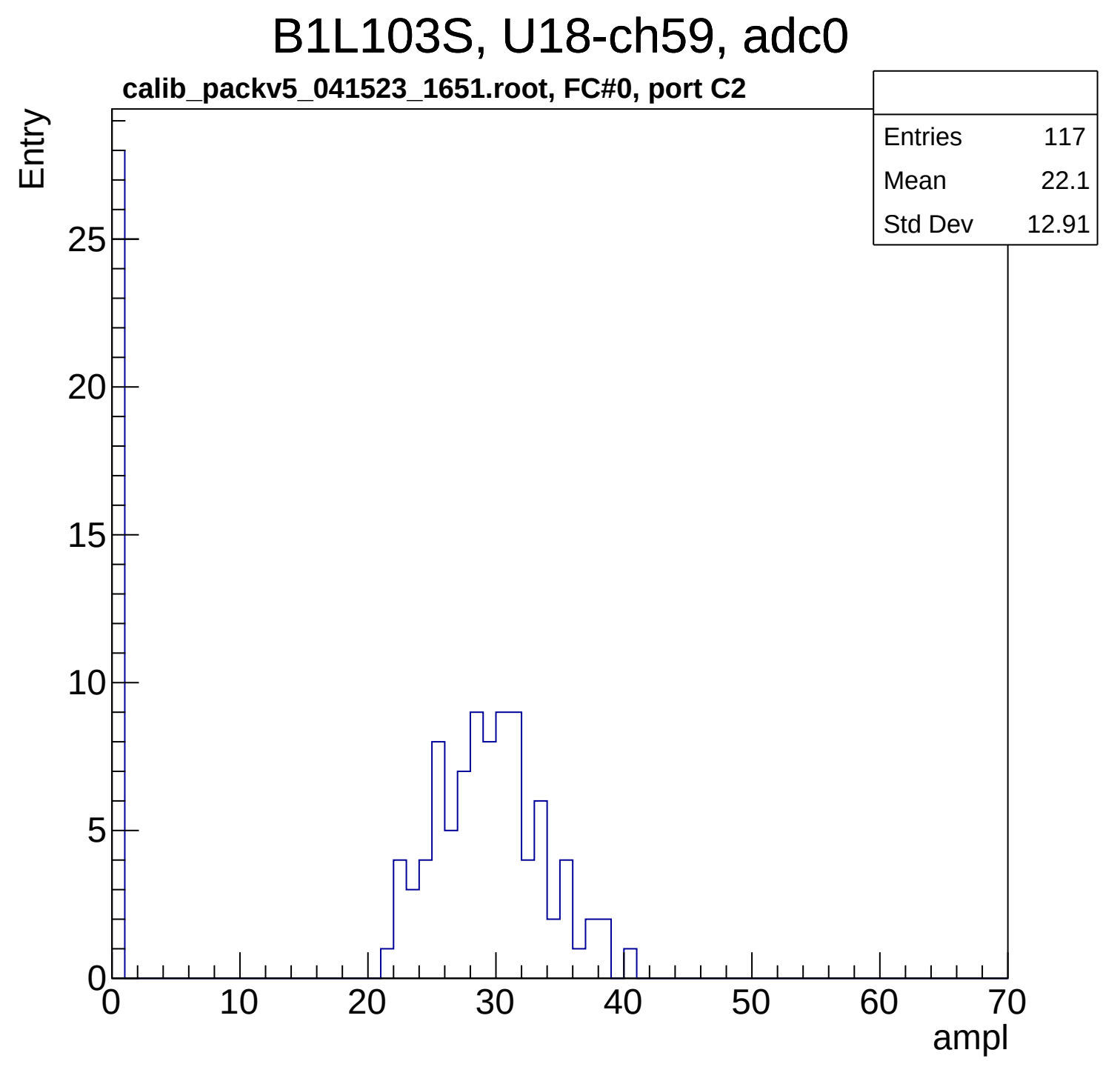
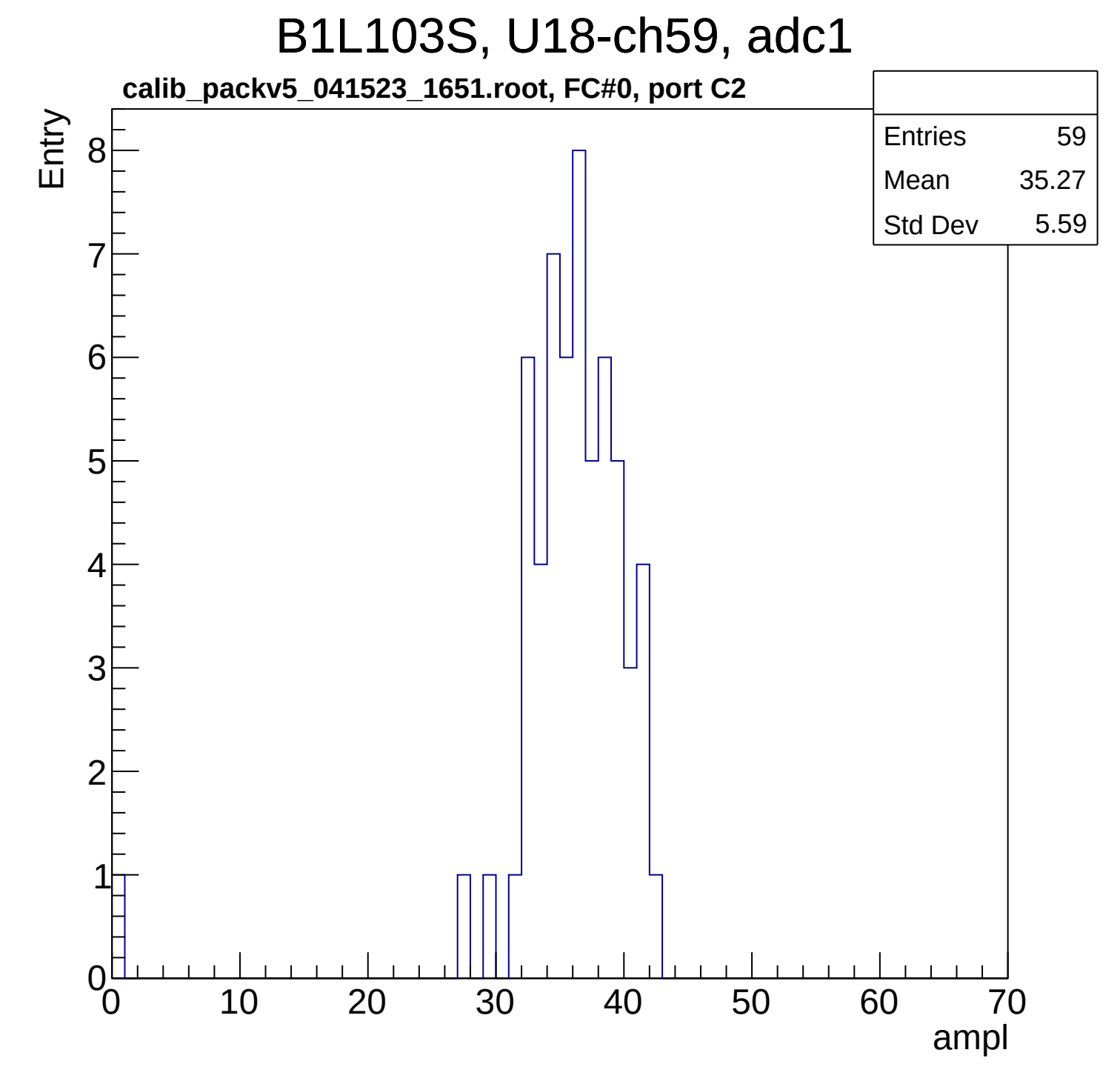
50
60
70
ampl


B1L103S, U18-ch59, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 117
Mean 22.1
Std Dev 12.91
Entry
0
5
10
15
20
25
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch59, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 35.27
Std Dev 5.59
Entry
ampl
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2
3
4
5
6
7
8
0
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40
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60
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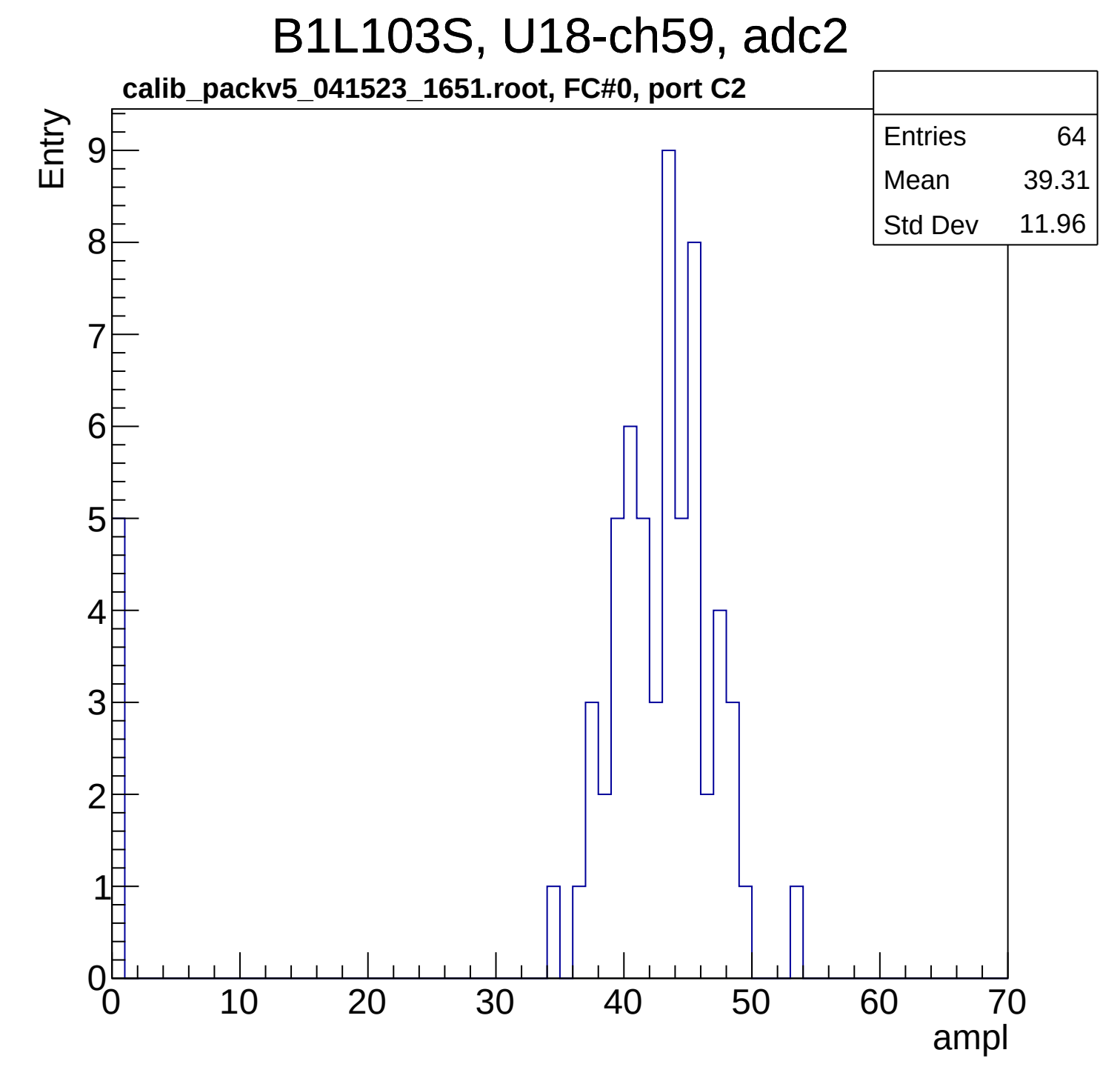
B1L103S, U18-ch59, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 39.31
Std Dev 11.96
Entry
ampl
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2
3
4
5
6
7
8
9
0
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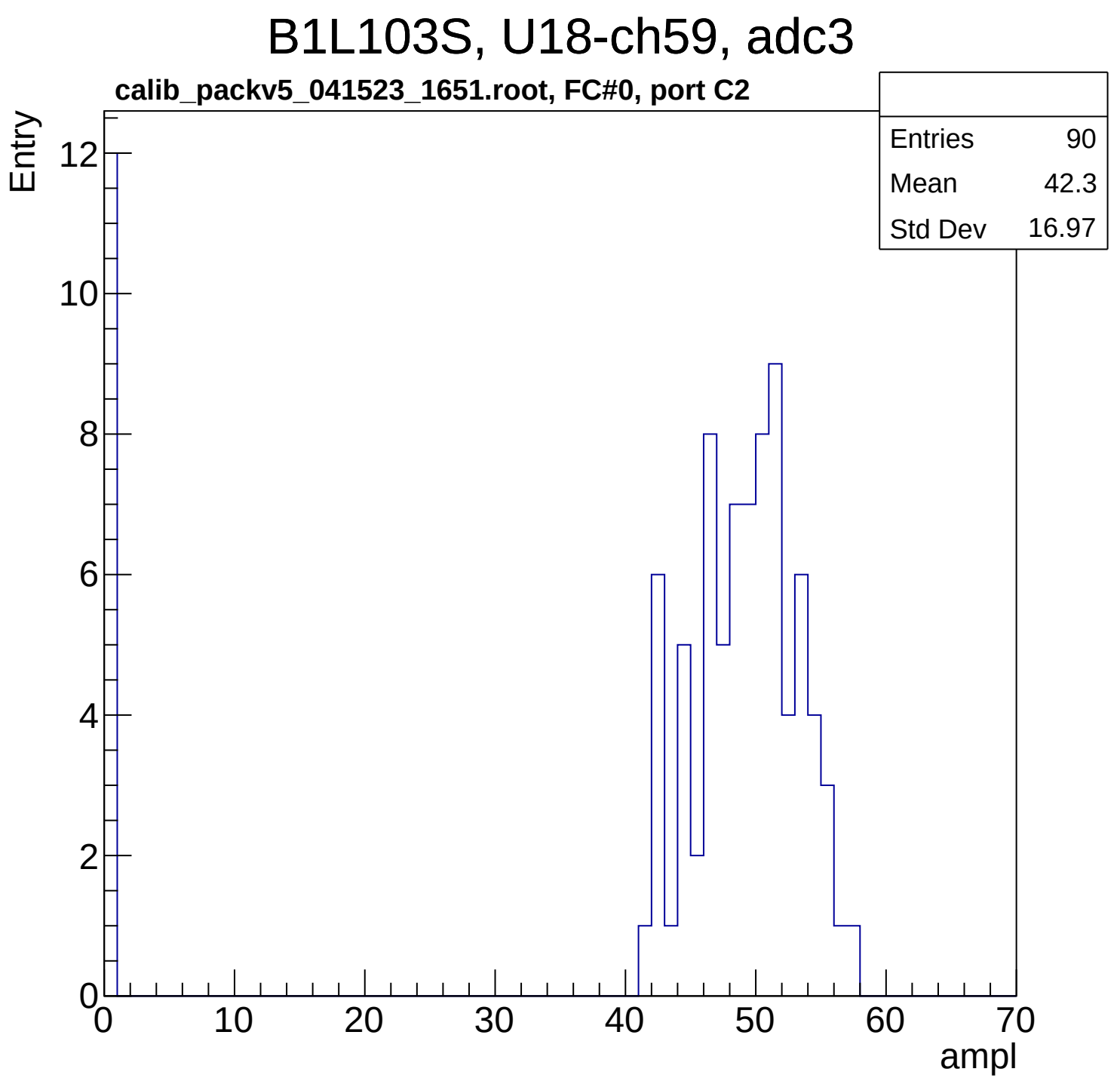
50
60
70


B1L103S, U18-ch59, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 90
Mean 42.3
Std Dev 16.97
Entry
0
2
4
6
8
10
12
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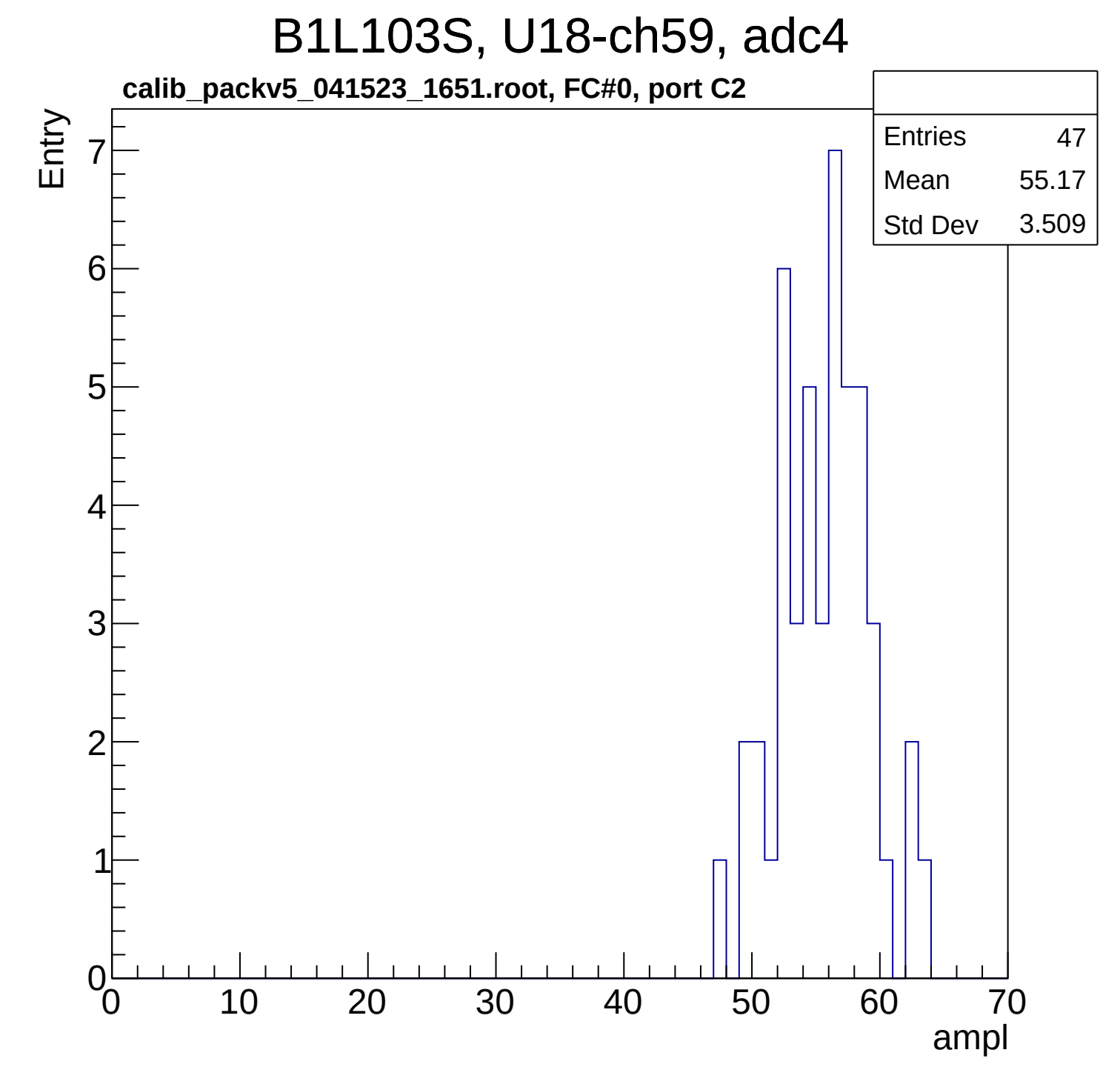
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch59, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 55.17
Std Dev 3.509
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
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40
50
60
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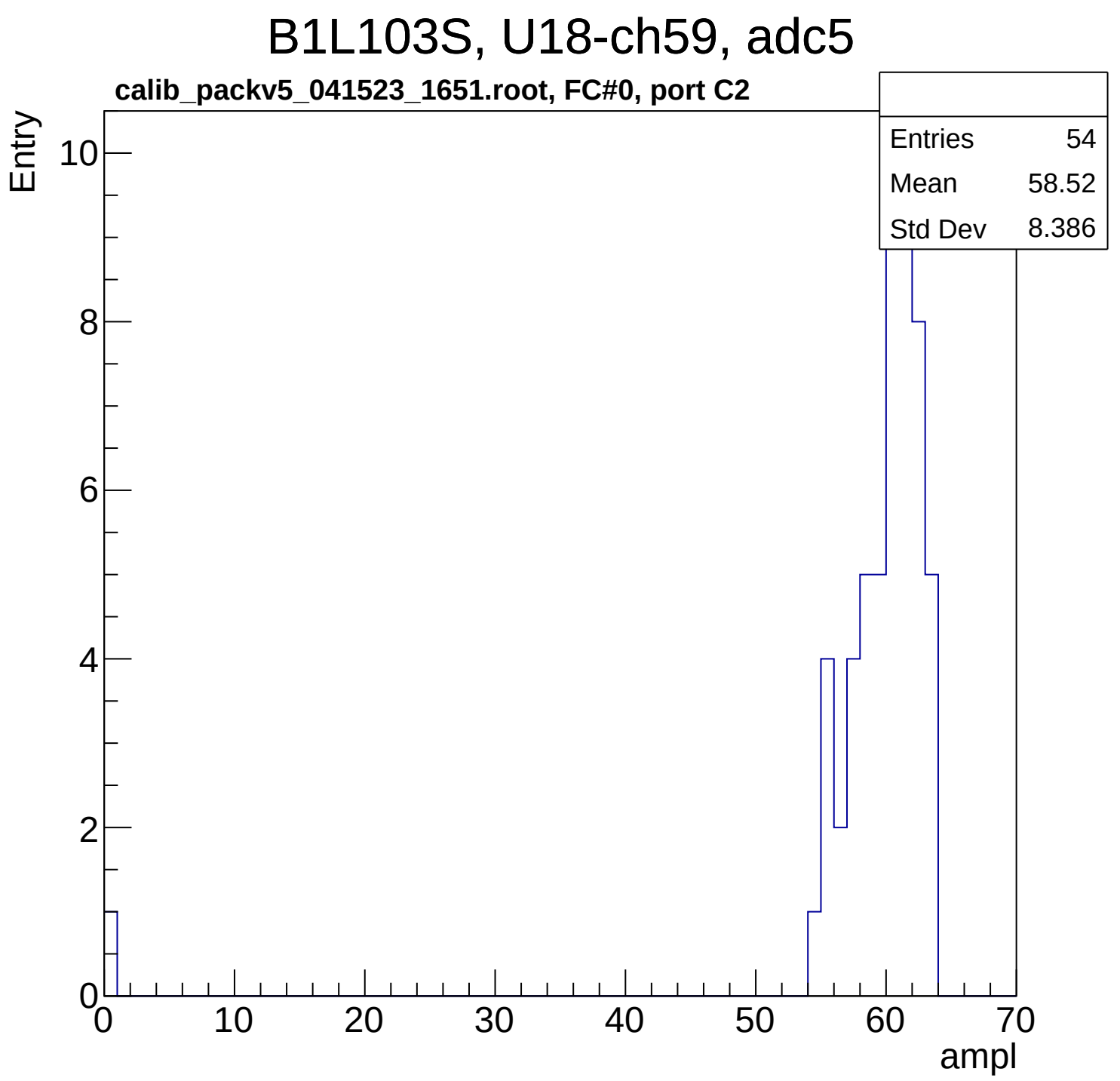
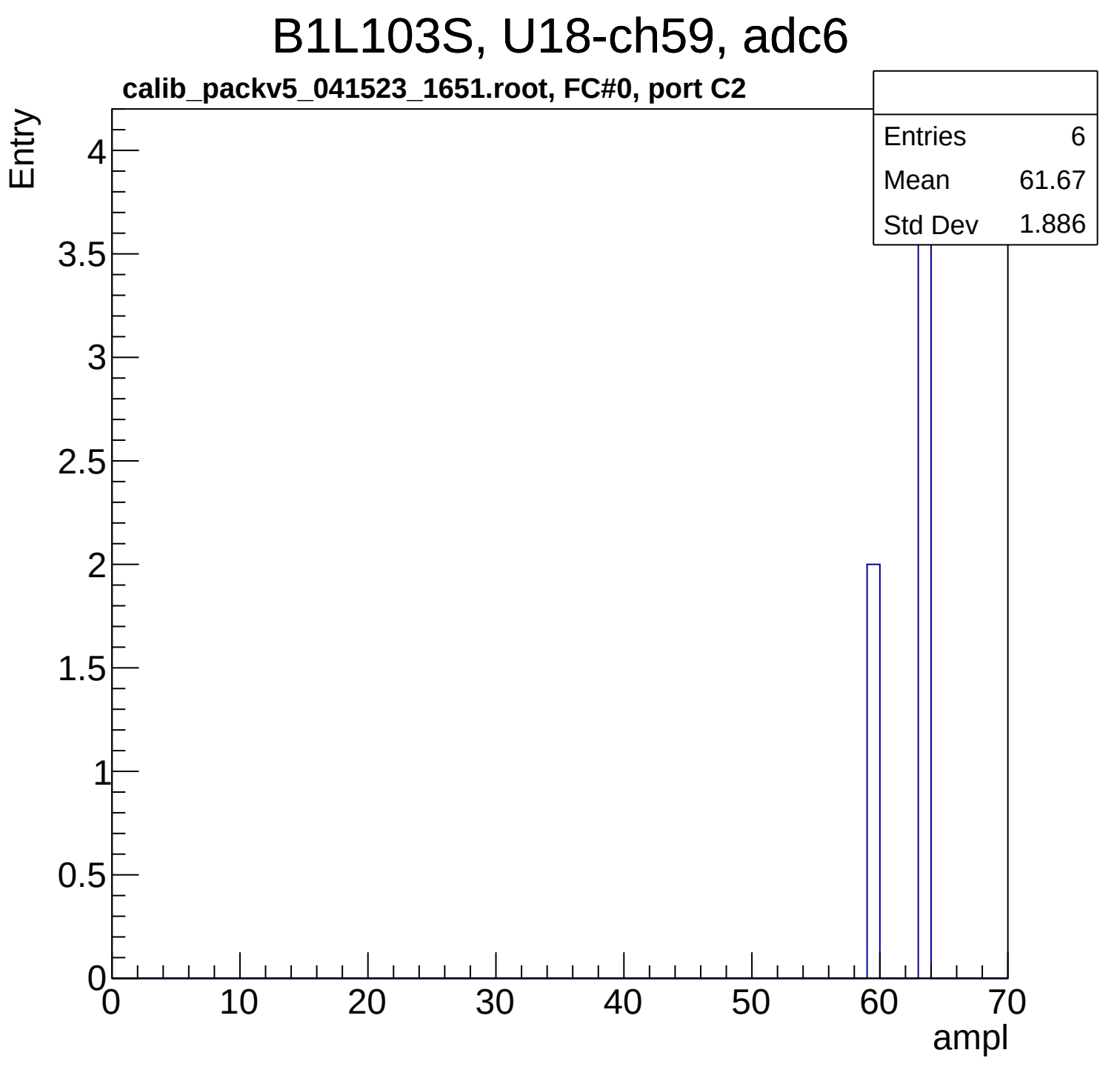

B1L103S, U18-ch59, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 58.52
Std Dev 8.386
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch59, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 61.67
Std Dev 1.886
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
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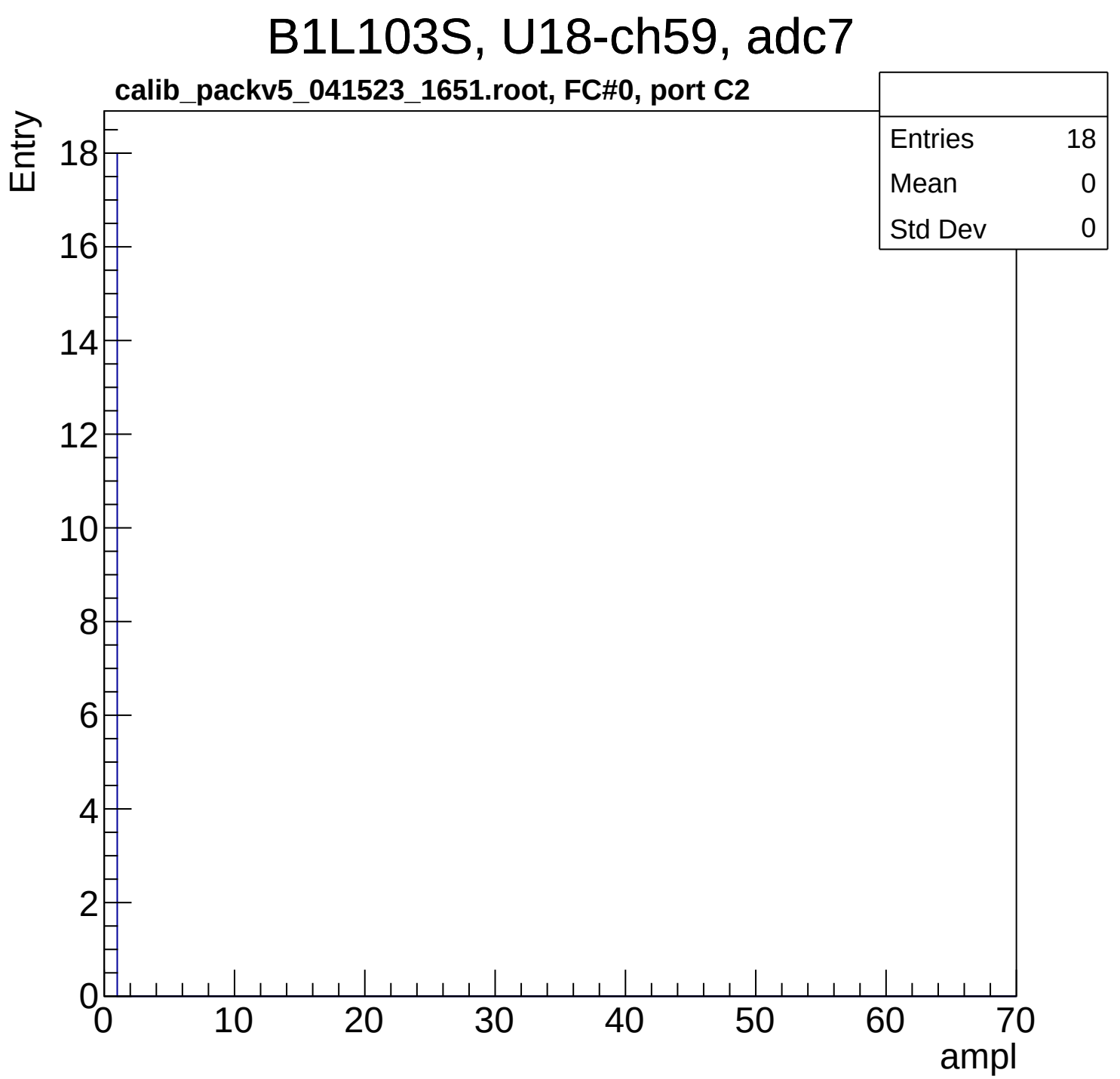
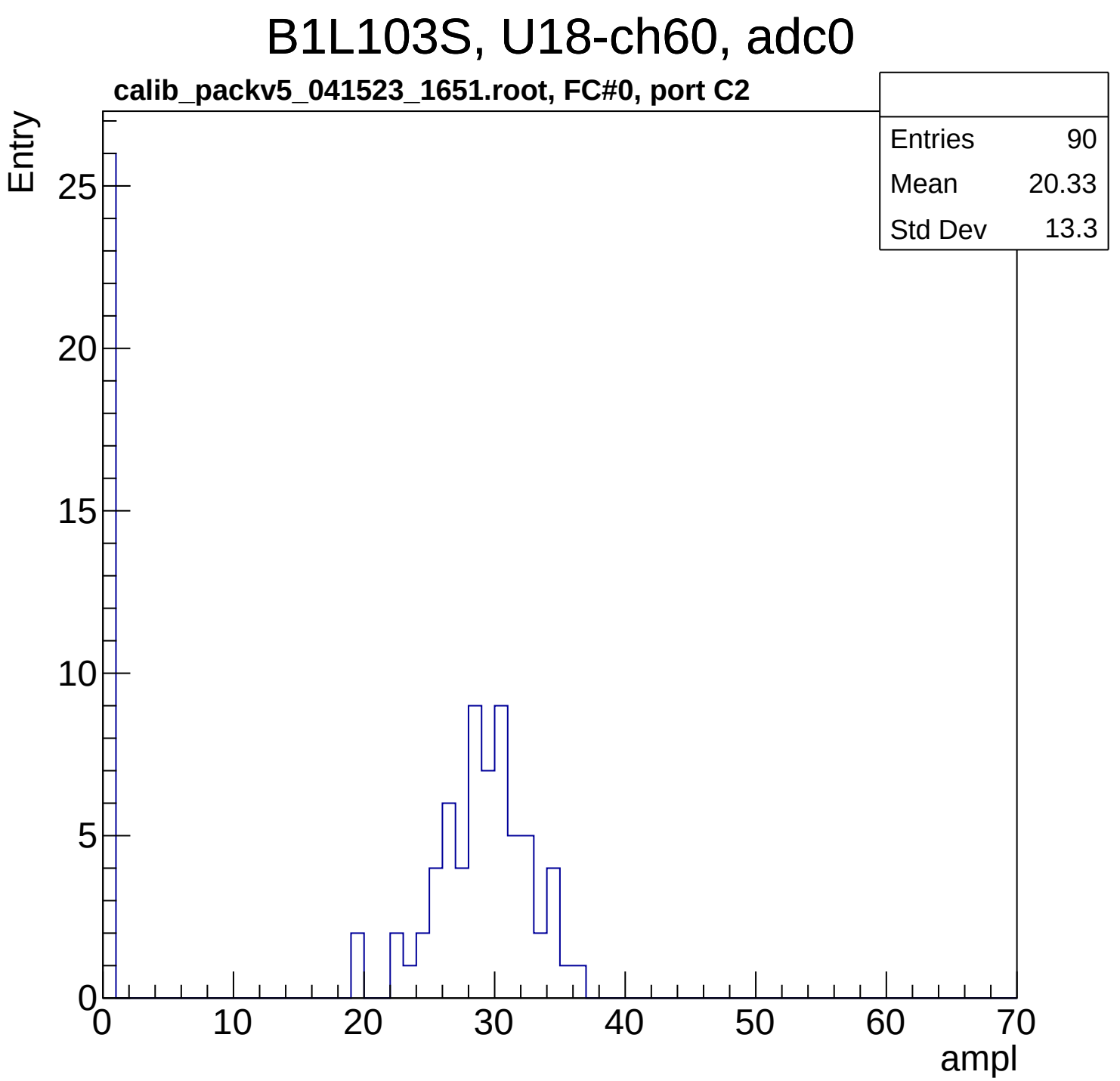
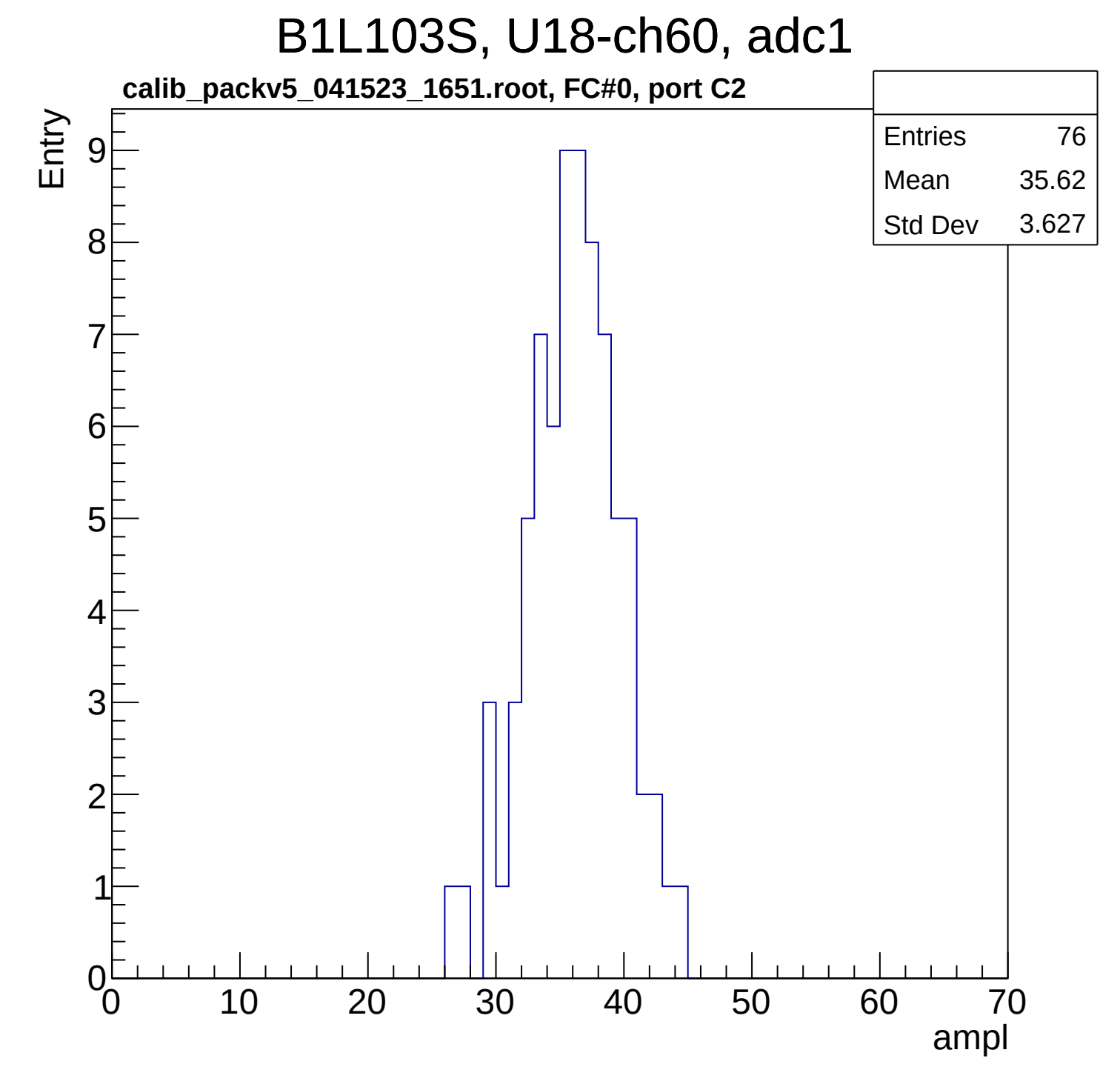

B1L103S, U18-ch59, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch60, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 90
Mean 20.33
Std Dev 13.3
Entry
0
5
10
15
20
25
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch60, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 35.62
Std Dev 3.627
Entry
ampl
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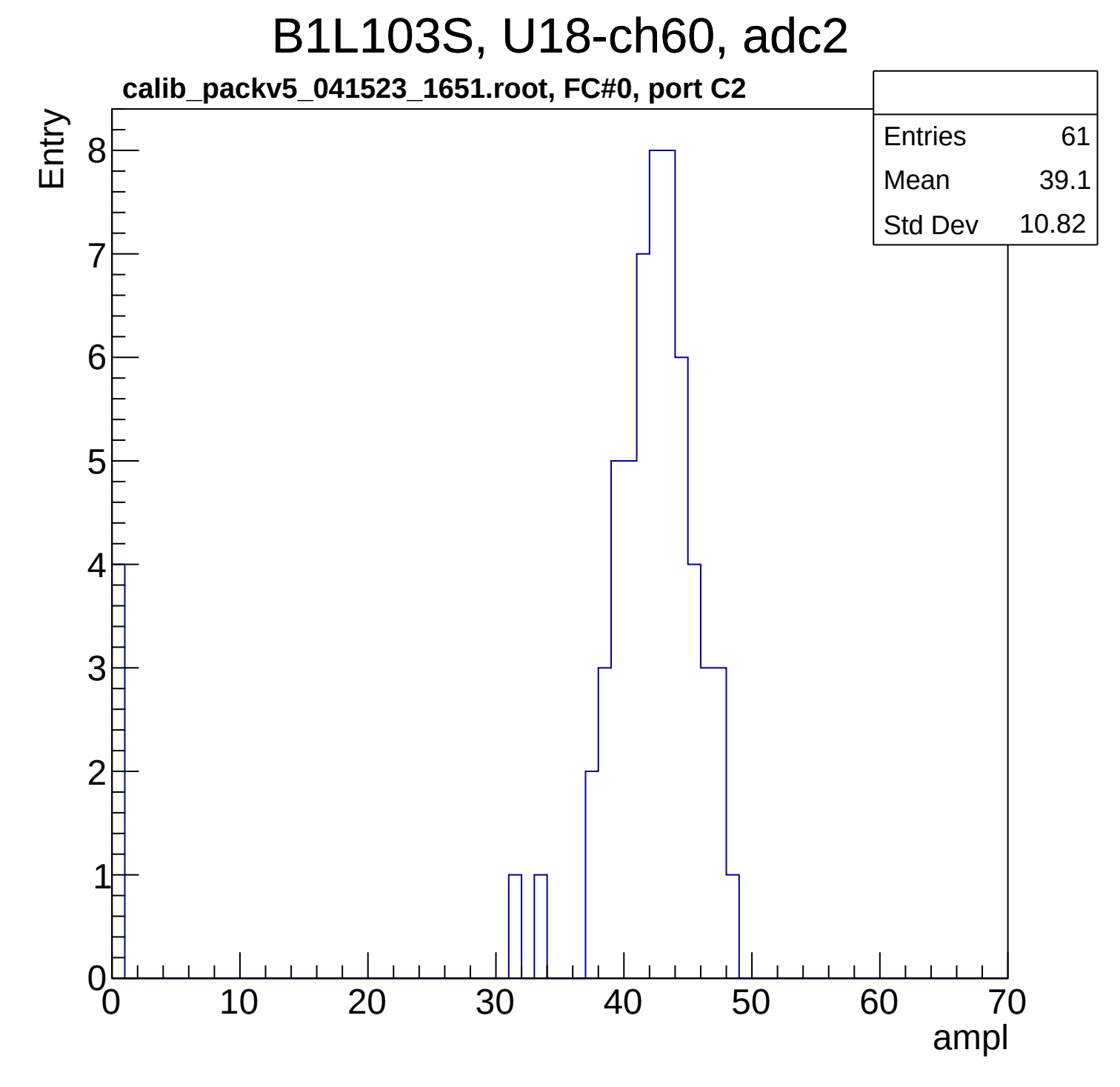
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U18-ch60, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 39.1
Std Dev 10.82
Entry
ampl
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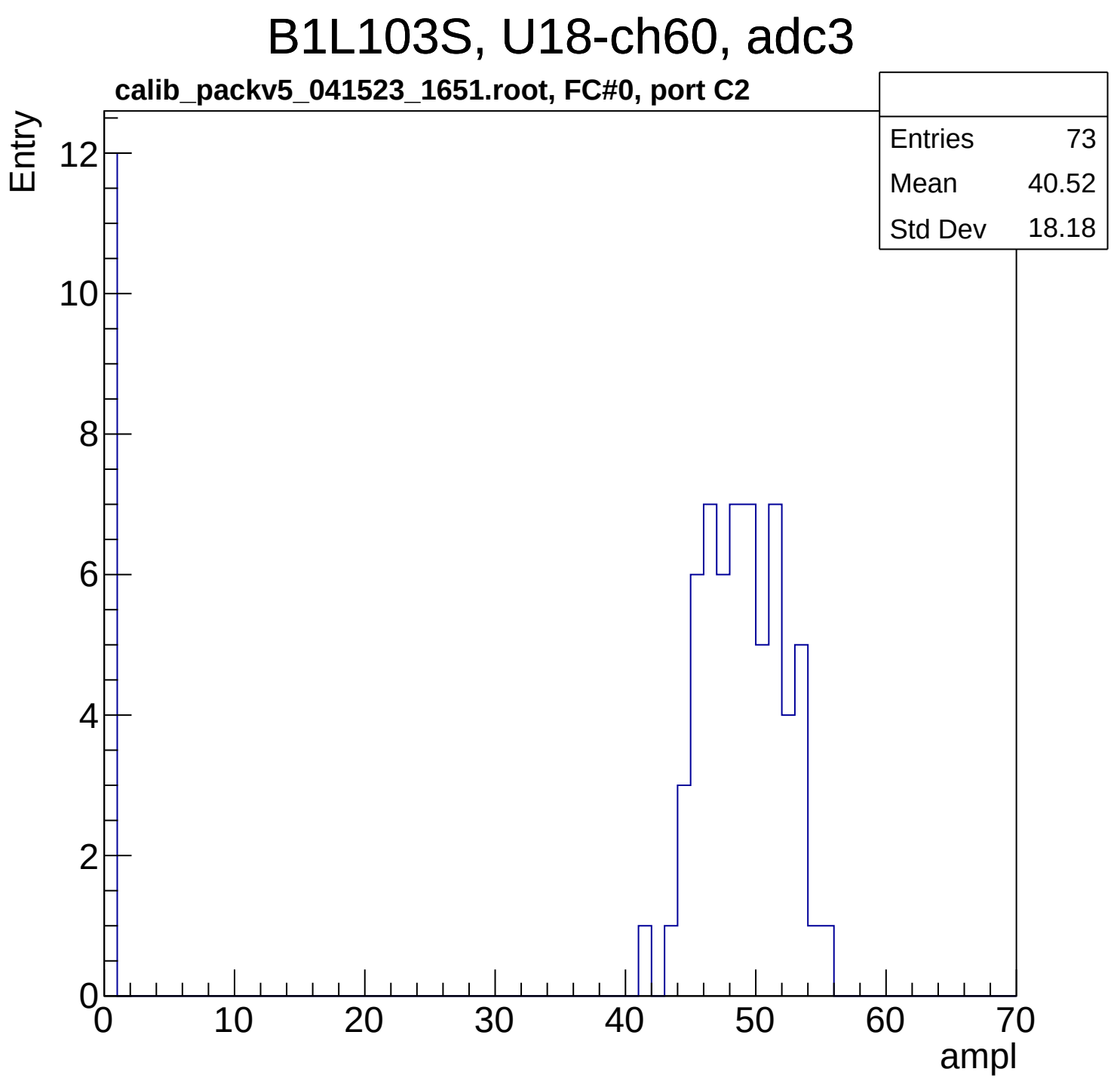
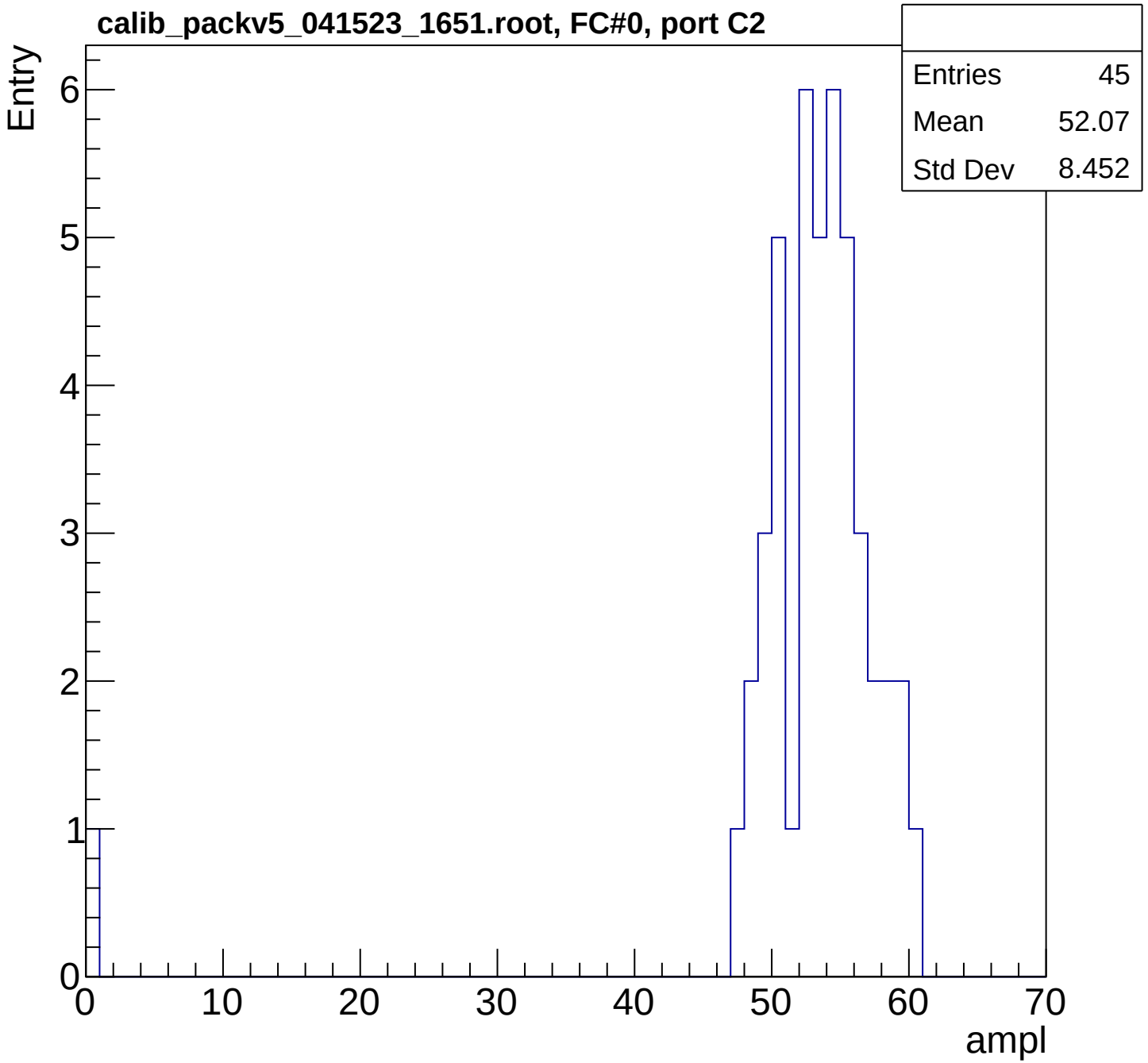
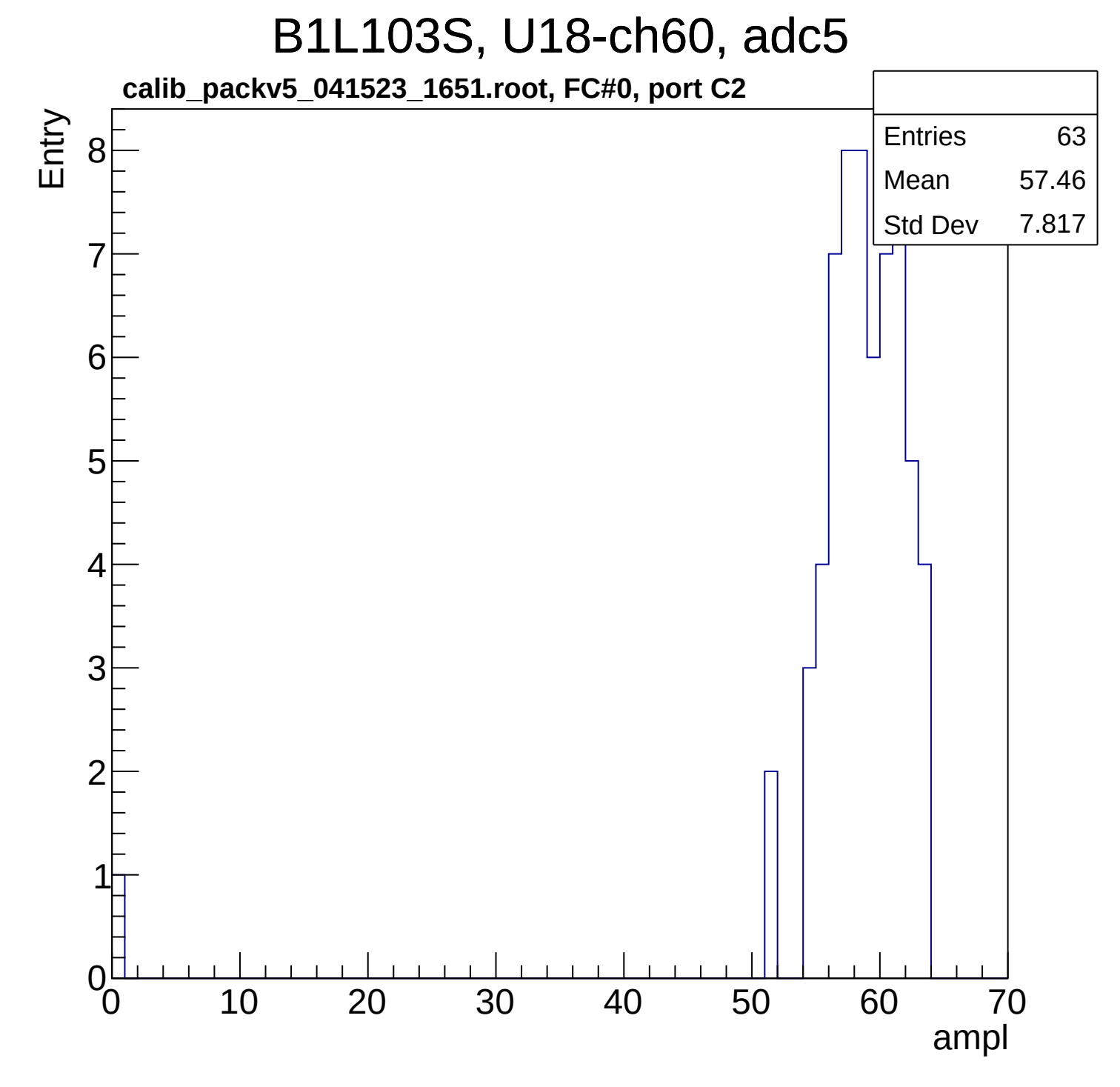
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch60, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 40.52
Std Dev 18.18
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch60, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 52.07
Std Dev 8.452
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U18-ch60, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 57.46
Std Dev 7.817
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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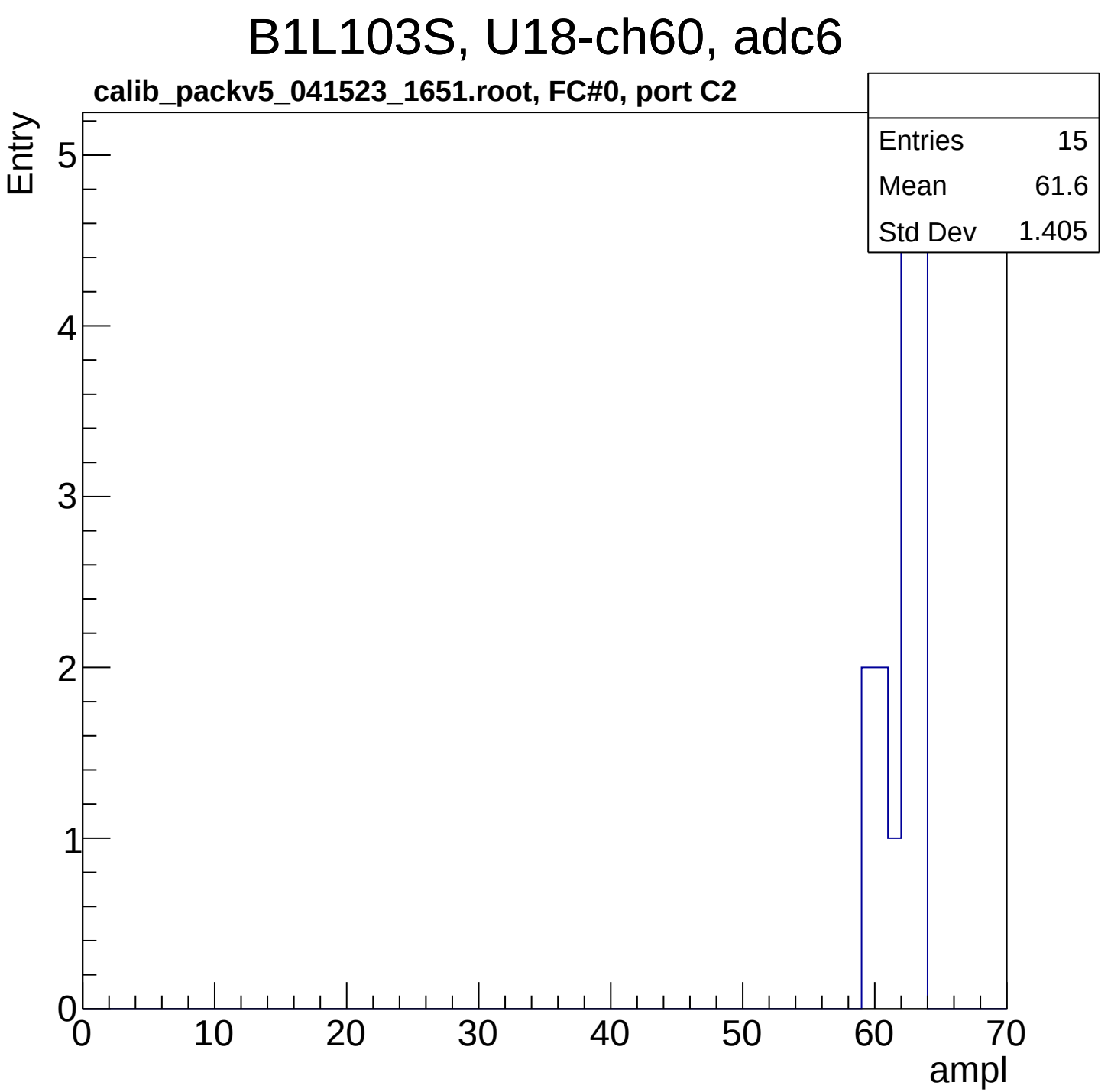
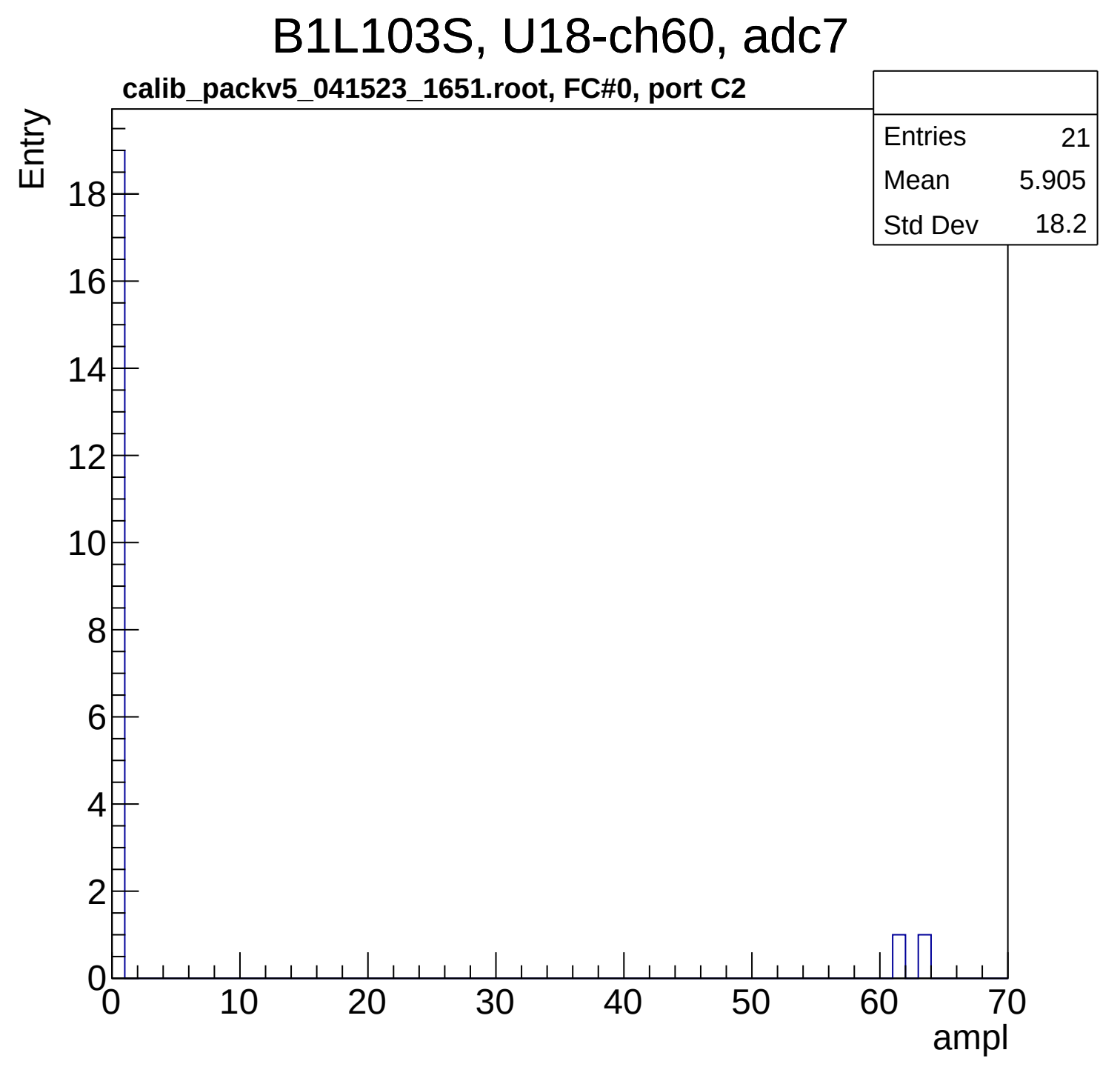
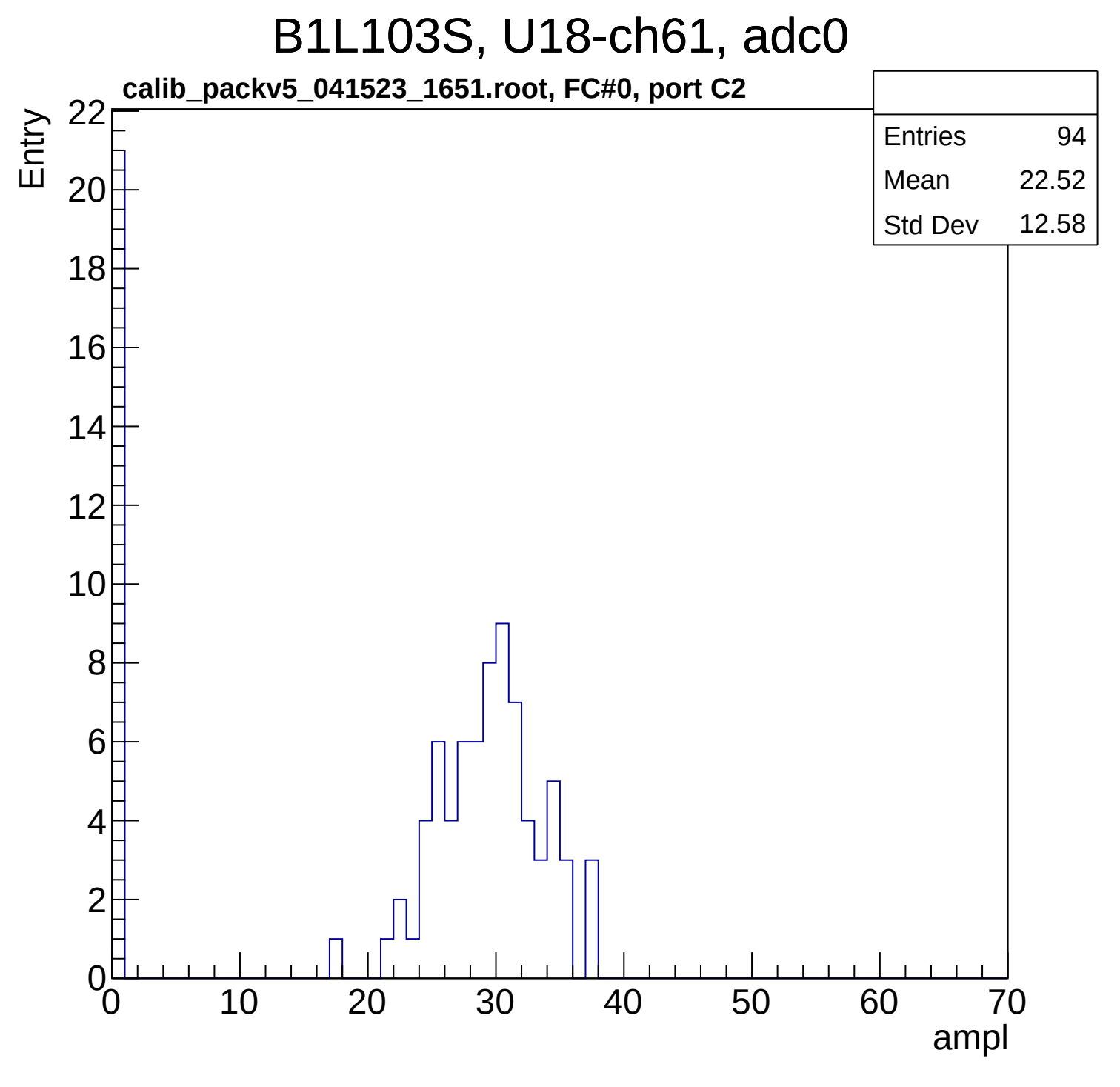

B1L103S, U18-ch60, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 15
Mean 61.6
Std Dev 1.405
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch60, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 5.905
Std Dev 18.2
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch61, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 94
Mean 22.52
Std Dev 12.58
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
22
0
10
20
30
40
50
60
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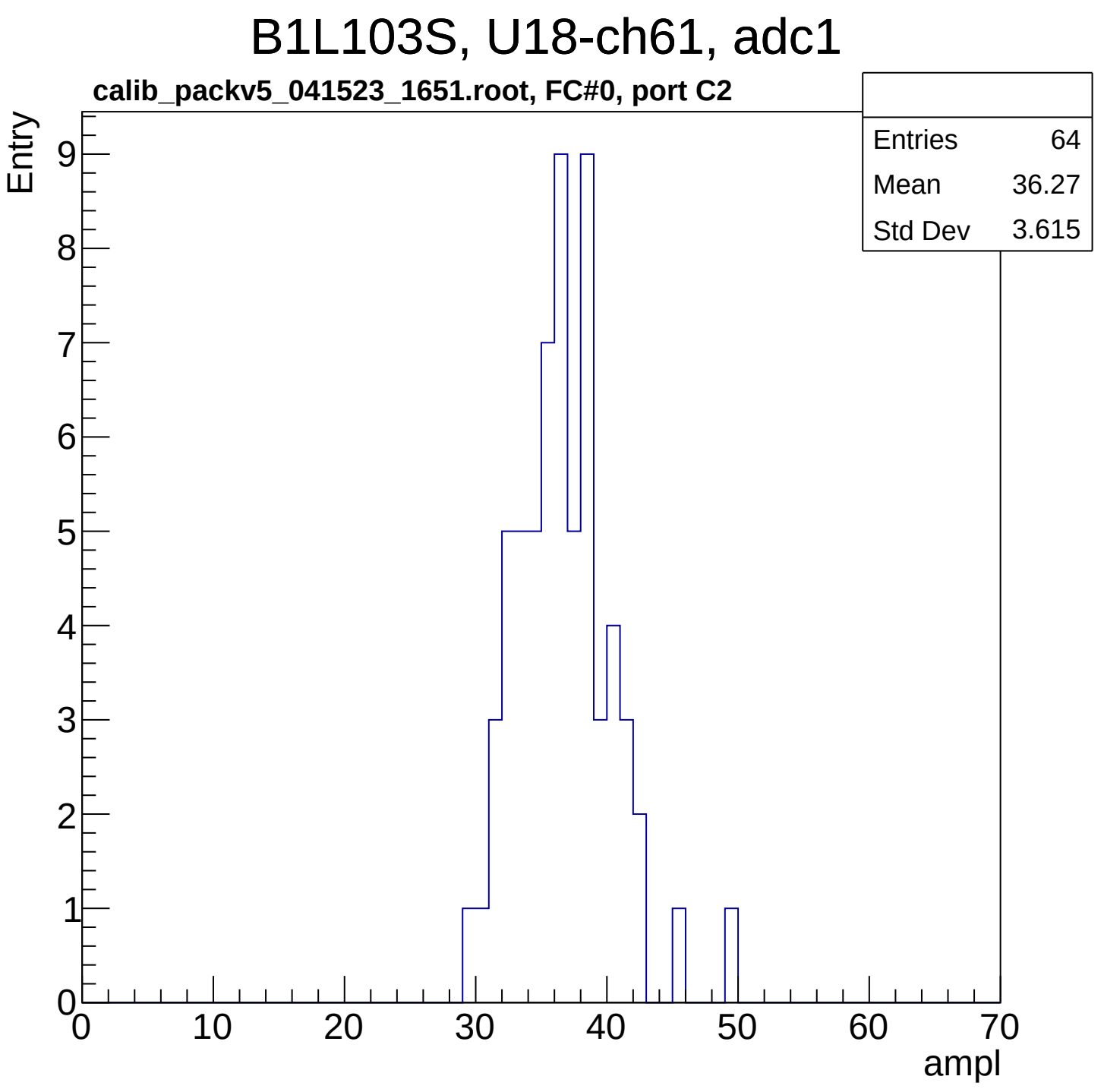
B1L103S, U18-ch61, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 36.27
Std Dev 3.615
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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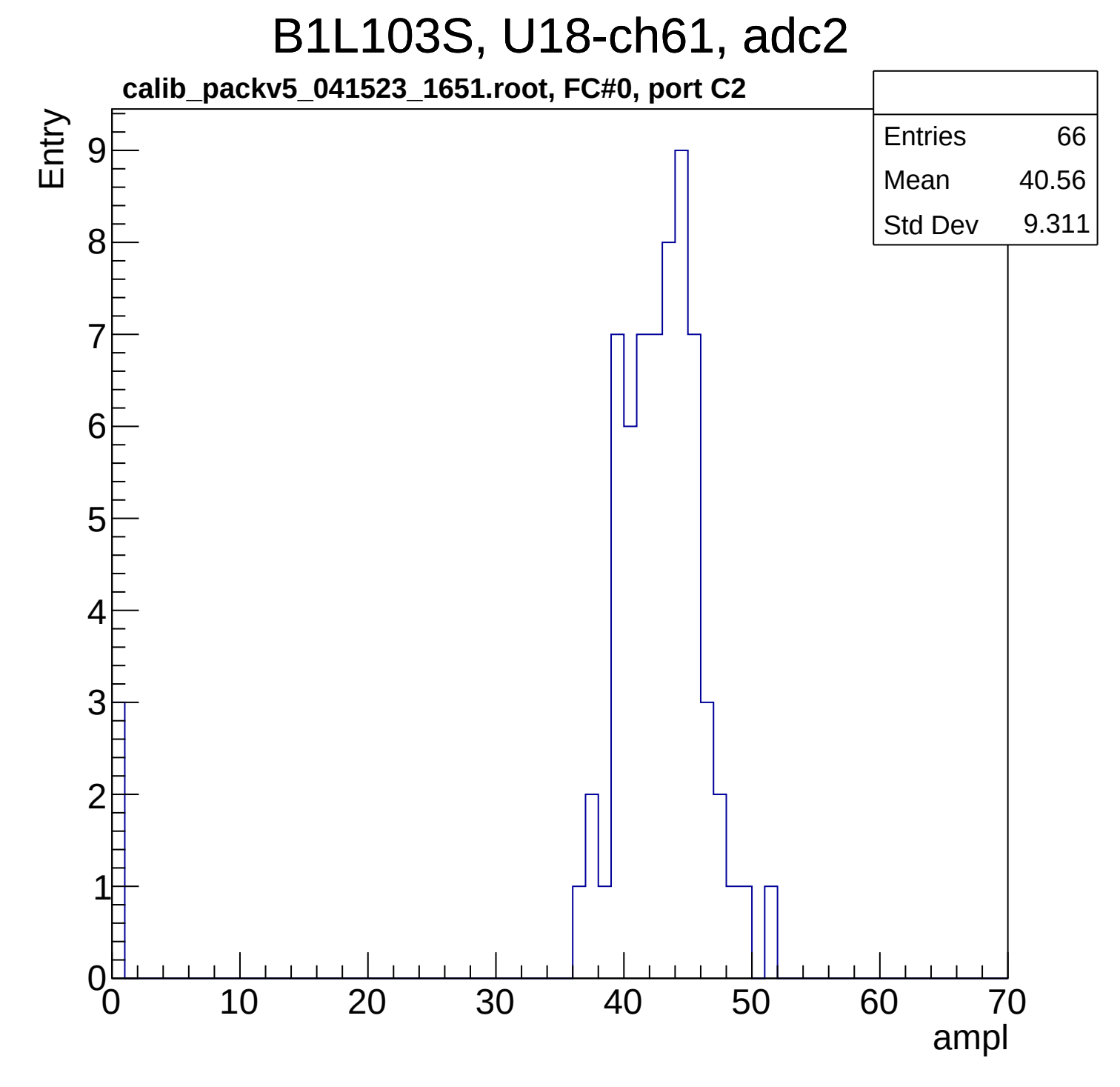
B1L103S, U18-ch61, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 40.56
Std Dev 9.311
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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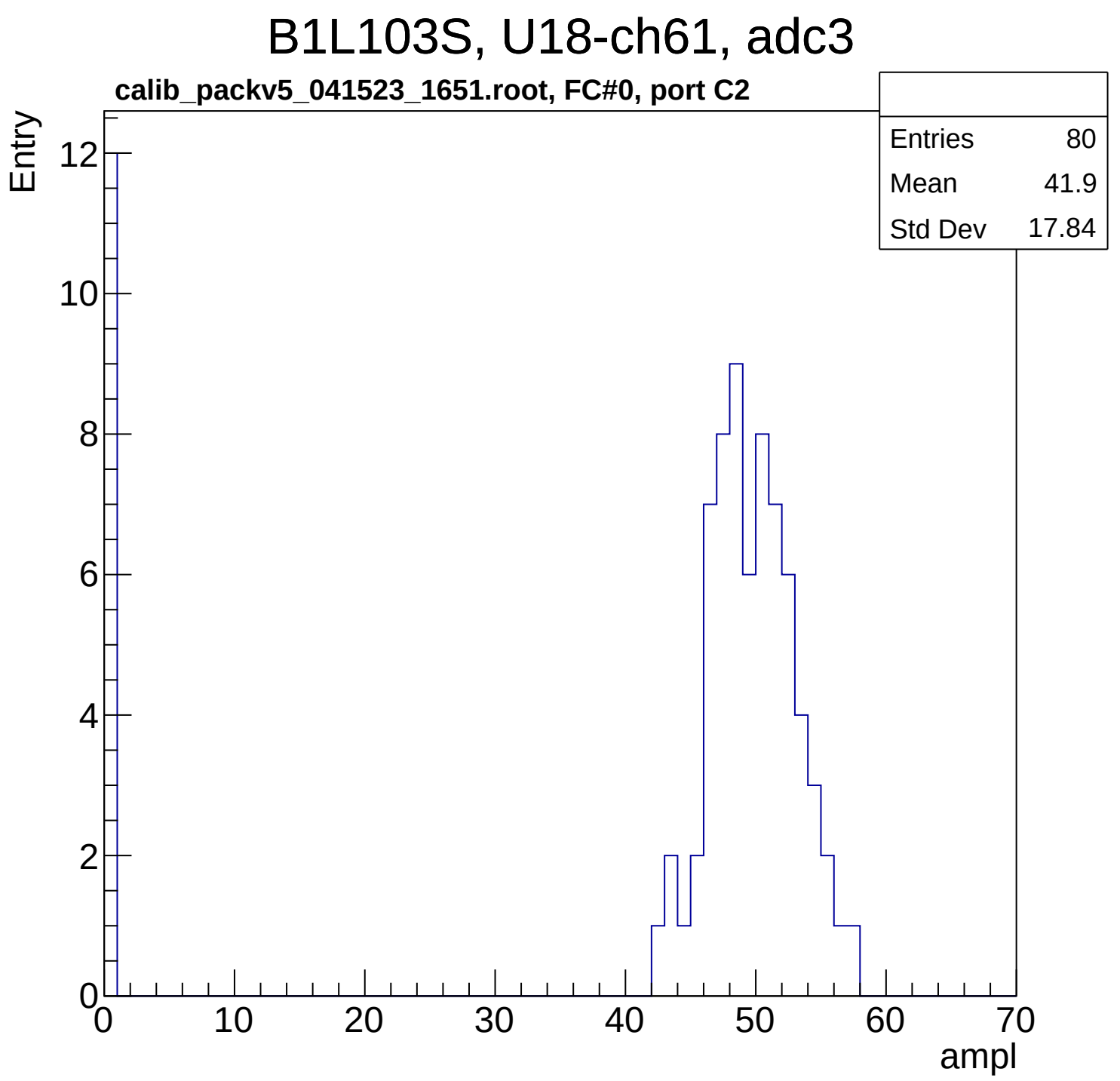
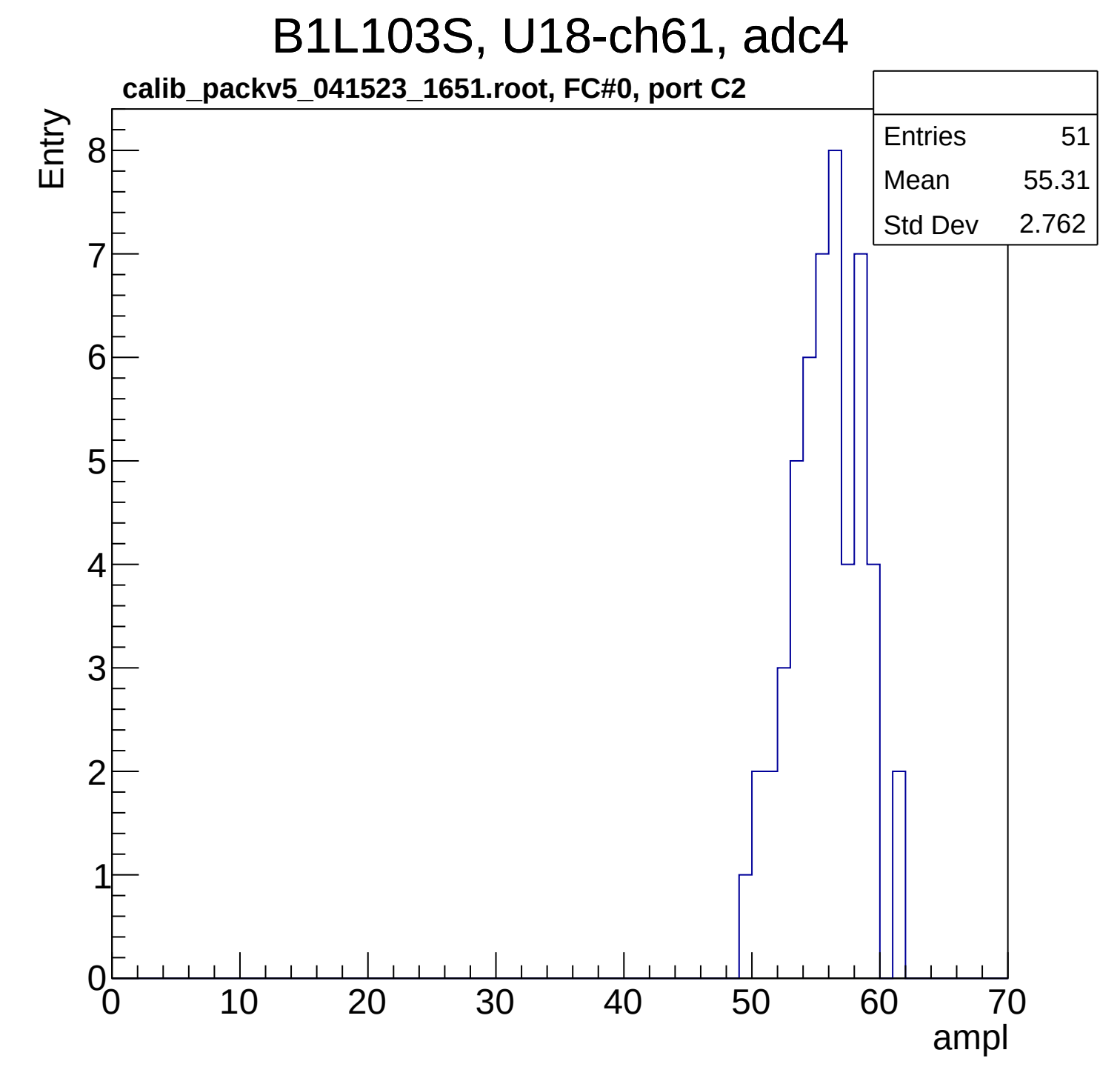

B1L103S, U18-ch61, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 41.9
Std Dev 17.84
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch61, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 55.31
Std Dev 2.762
Entry
ampl
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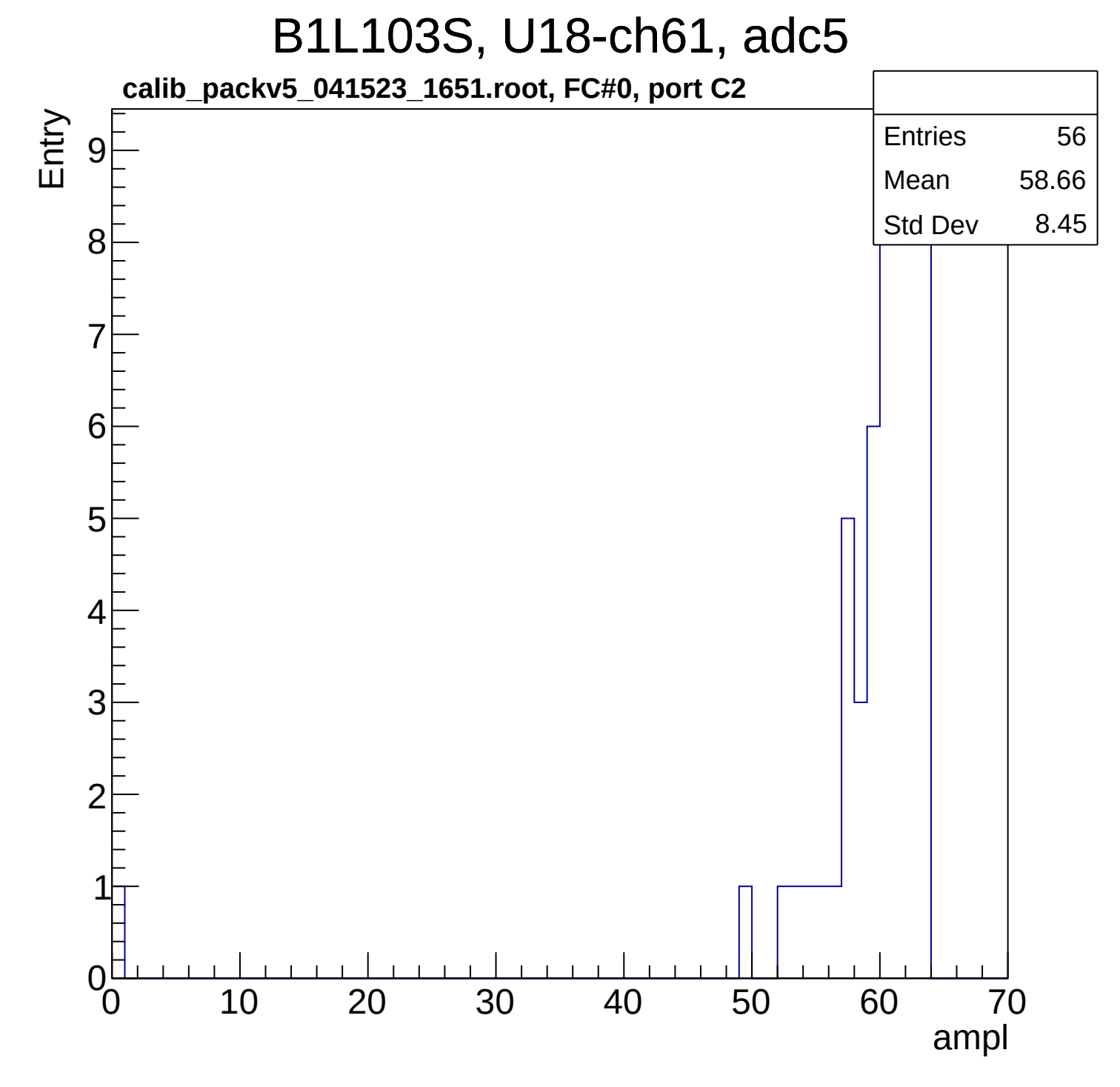
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch61, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 58.66
Std Dev 8.45
Entry
ampl
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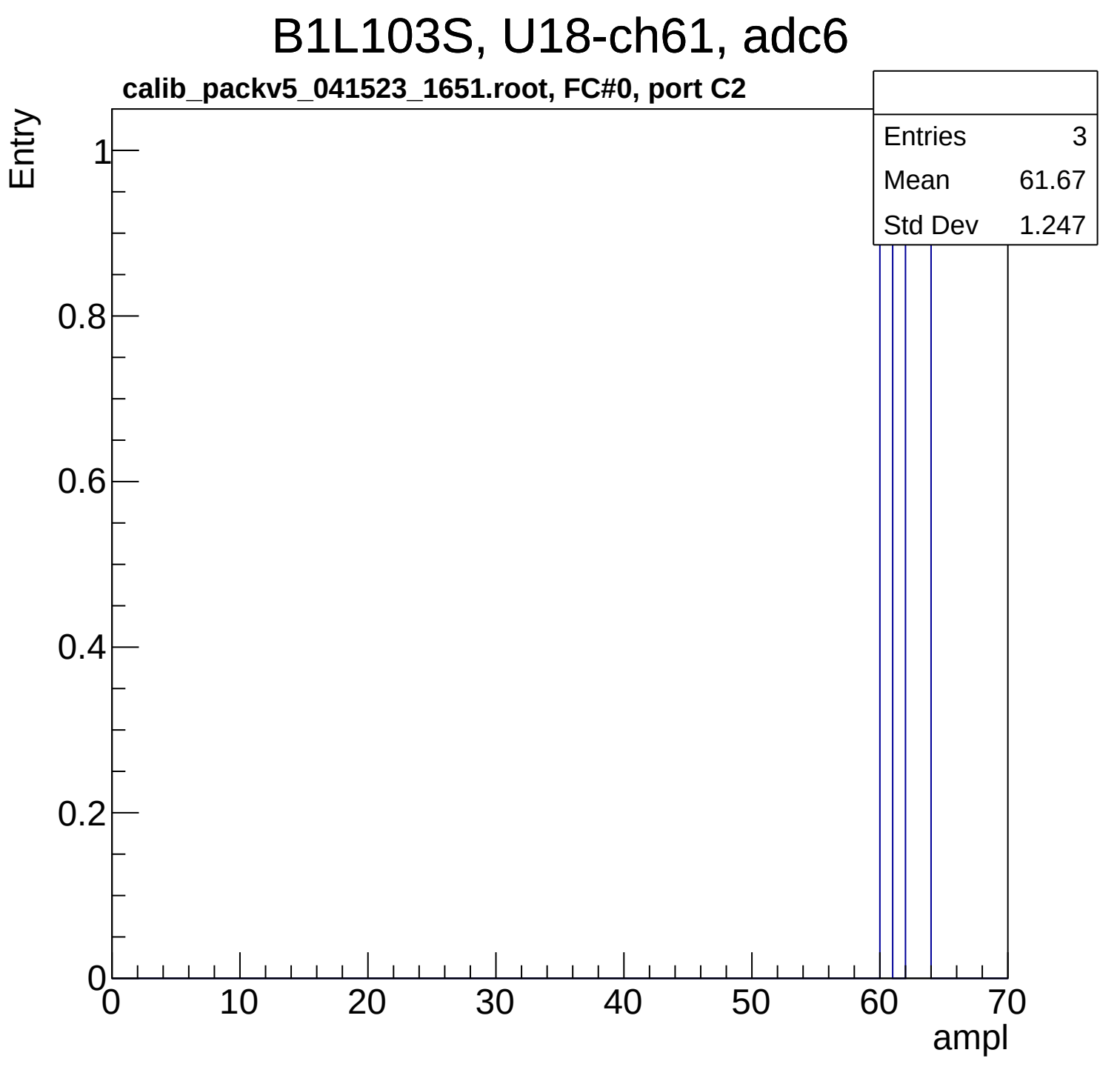
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U18-ch61, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 3
Mean 61.67
Std Dev 1.247
Entry
ampl
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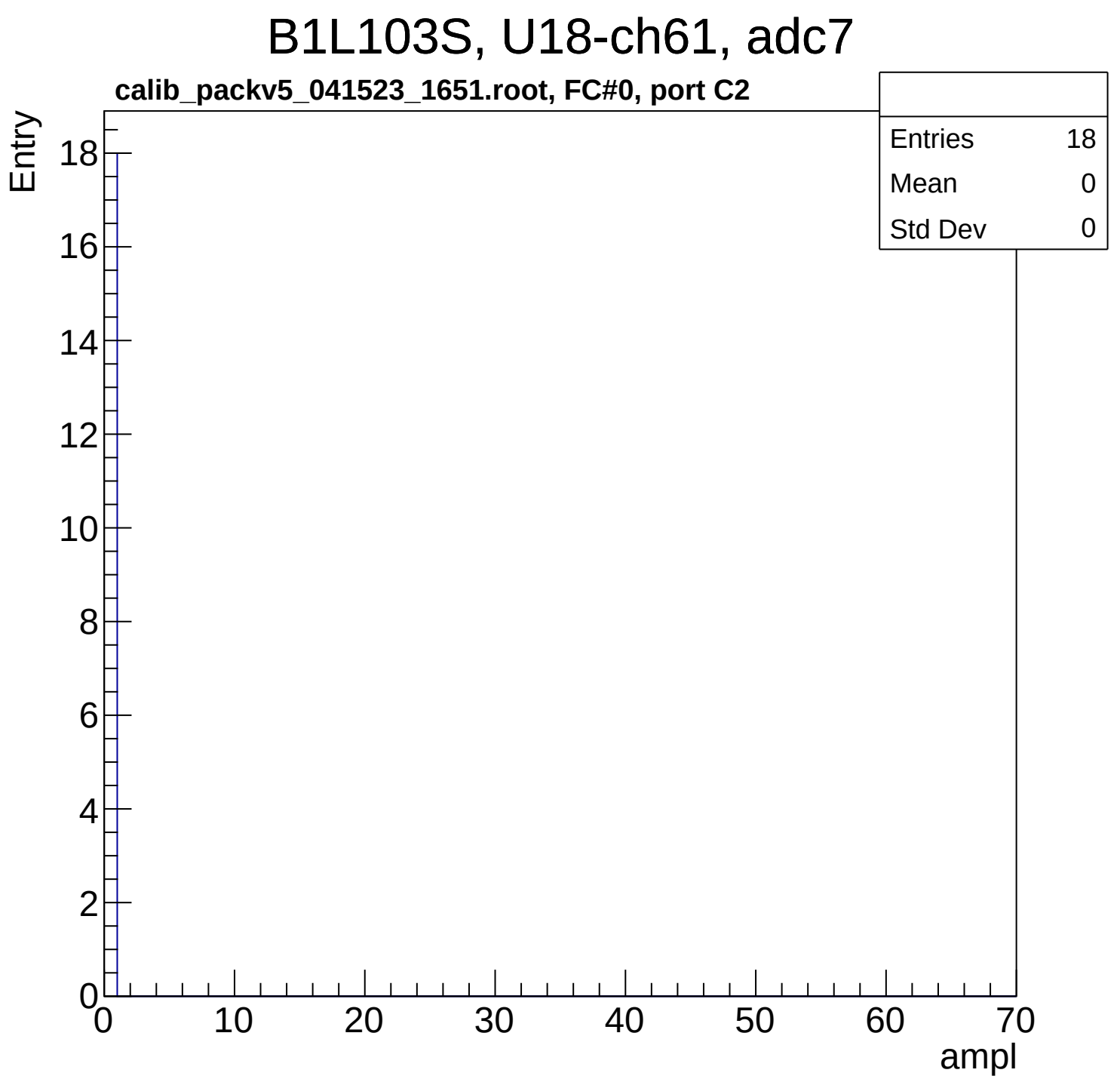
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70


B1L103S, U18-ch61, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
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2
4
6
8
10
12
14
16
18
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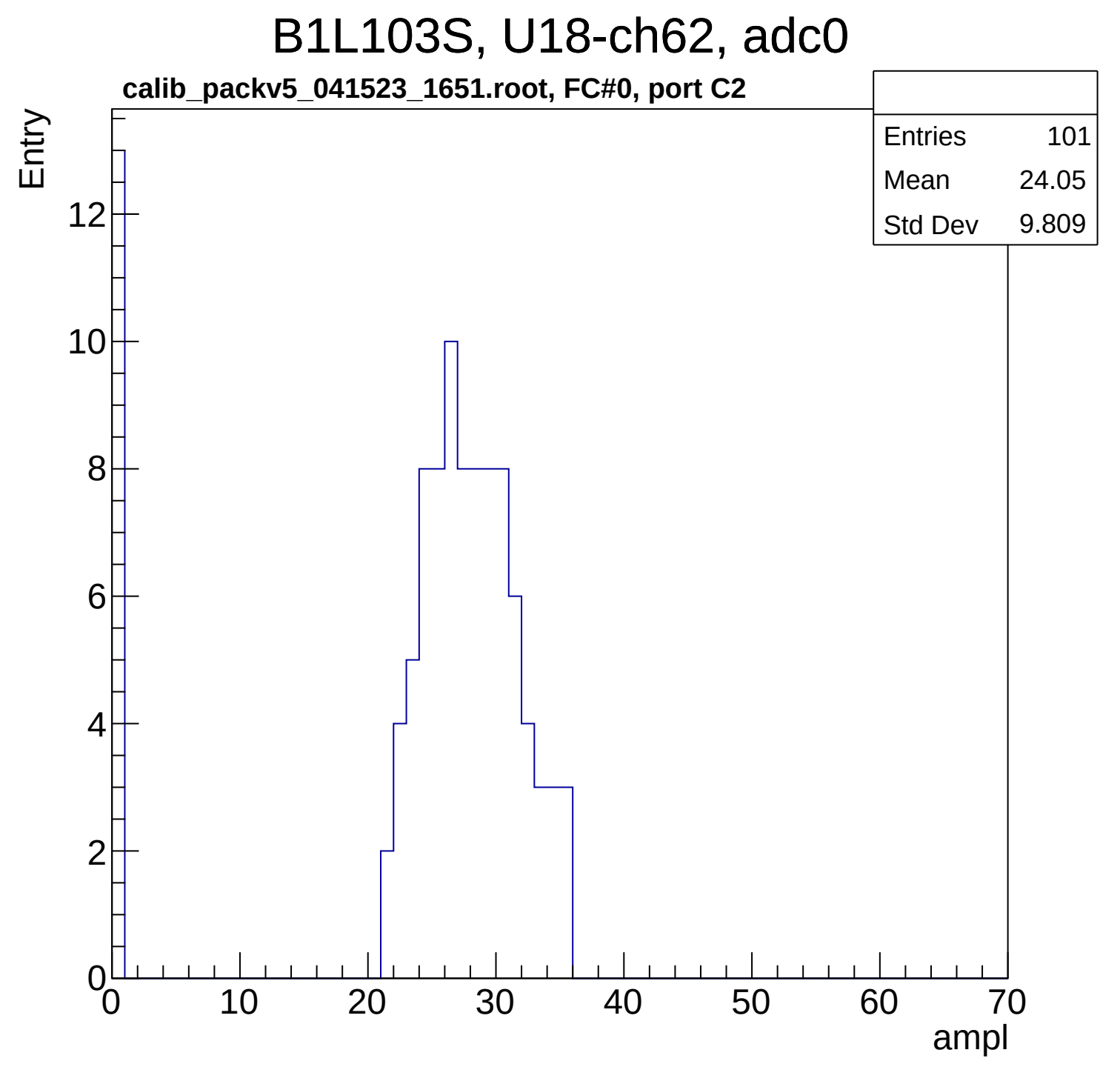
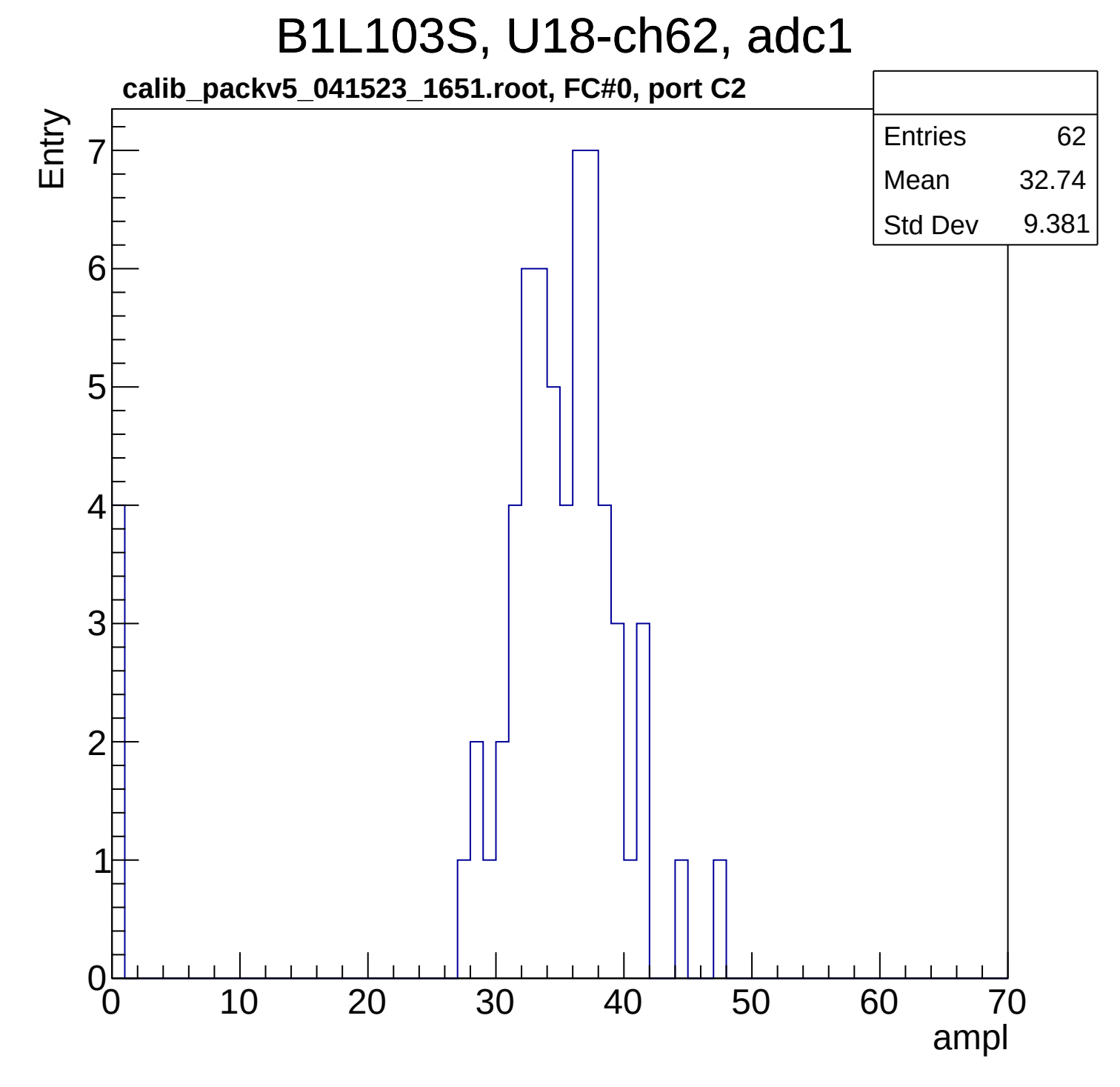
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch62, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 101
Mean 24.05
Std Dev 9.809
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch62, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 32.74
Std Dev 9.381
Entry
ampl
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1
2
3
4
5
6
7
0
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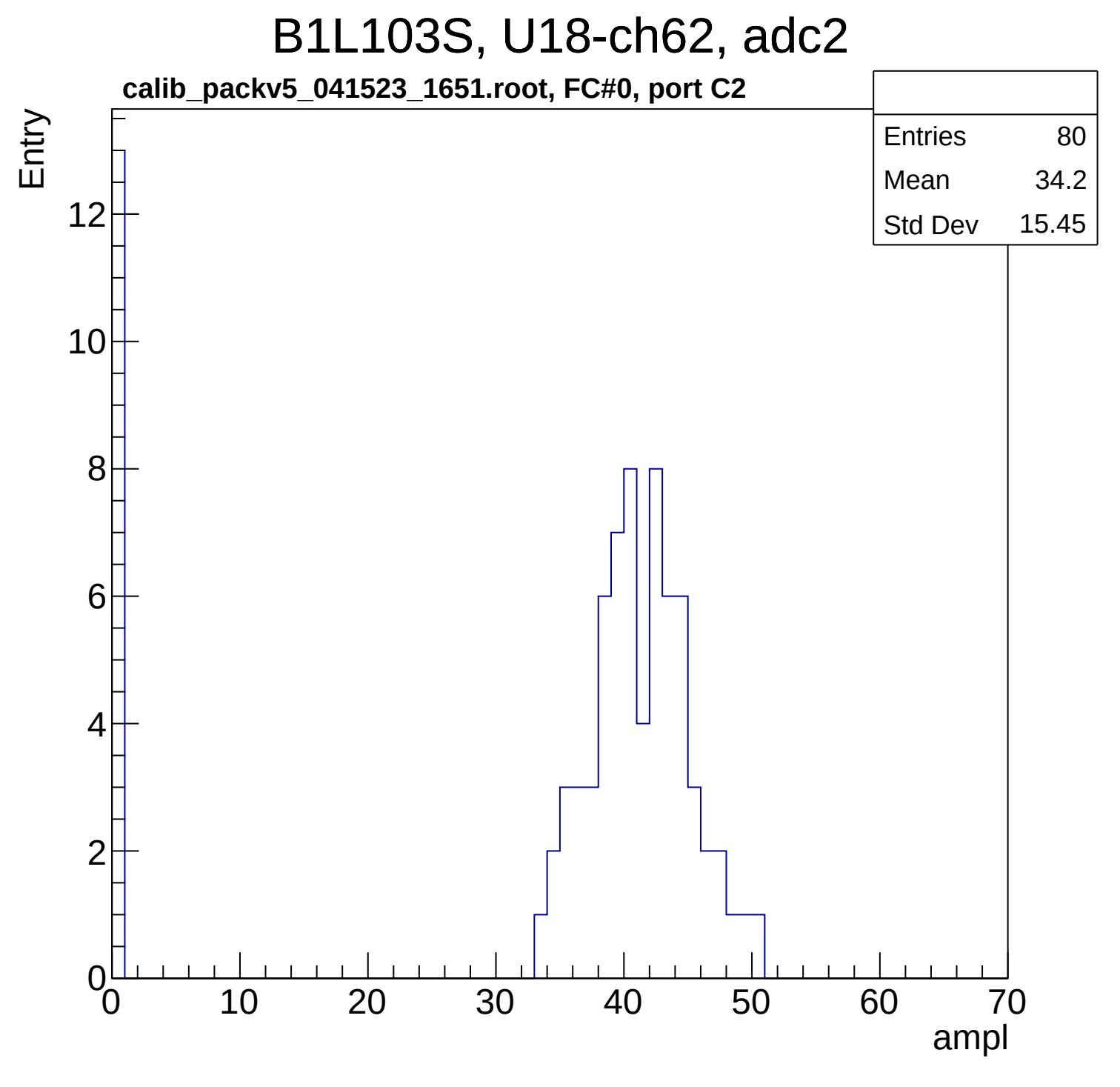
20
30
40
50
60
70


B1L103S, U18-ch62, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 34.2
Std Dev 15.45
Entry
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2
4
6
8
10
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10
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30
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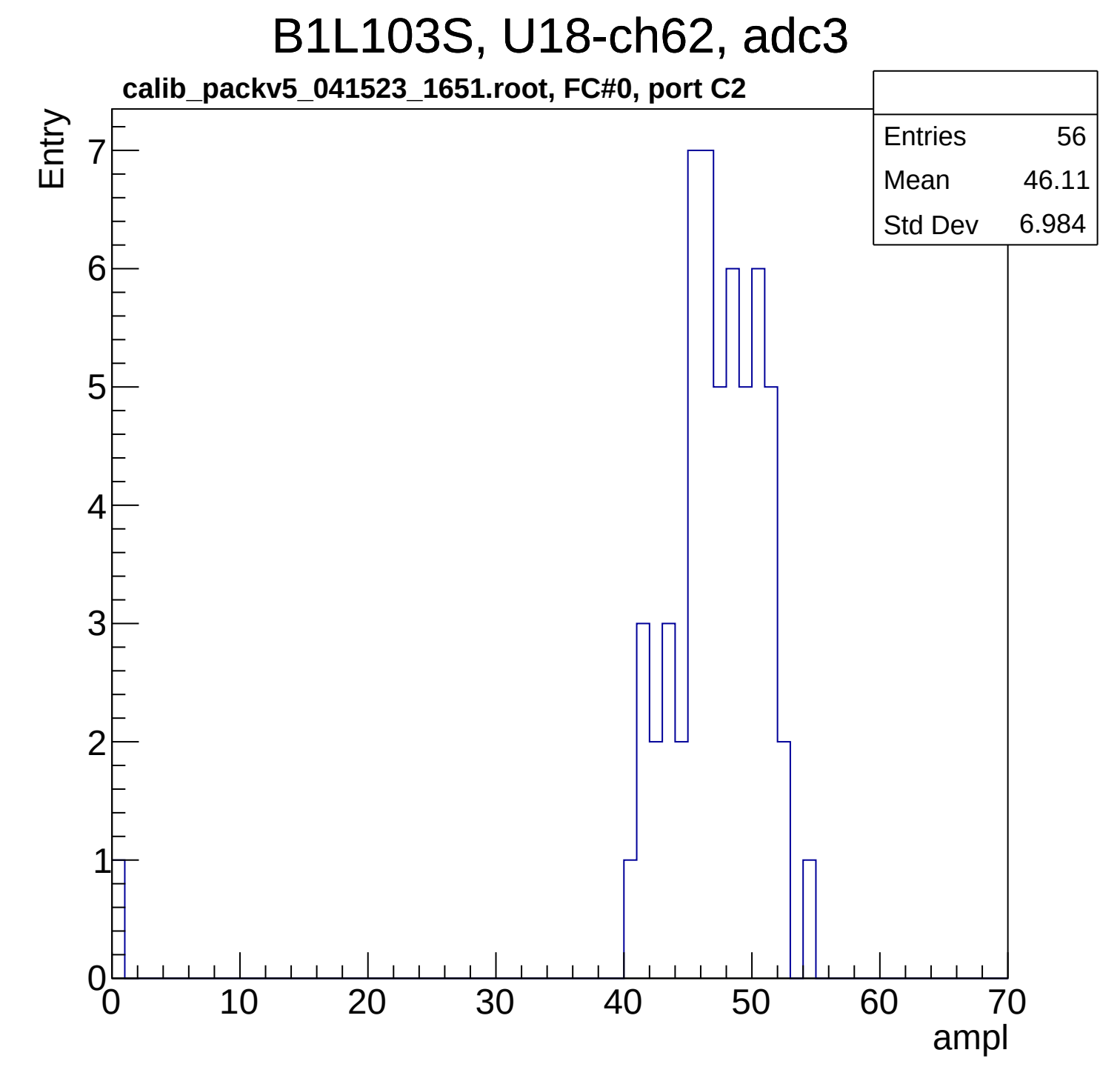
50
60
70
ampl


B1L103S, U18-ch62, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 46.11
Std Dev 6.984
Entry
ampl
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1
2
3
4
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6
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0
10
20
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40
50
60
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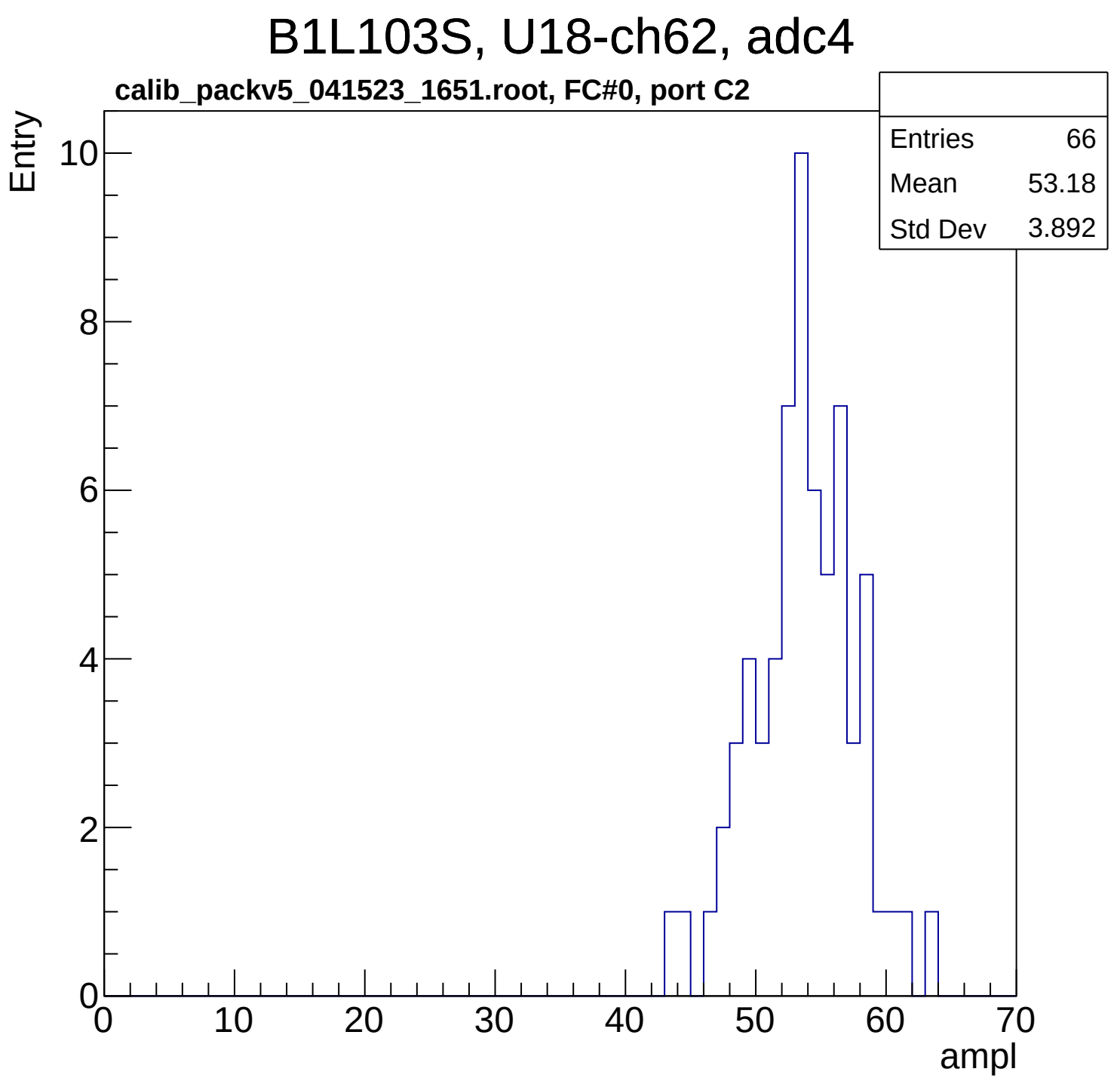
B1L103S, U18-ch62, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 53.18
Std Dev 3.892
Entry
ampl
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2
4
6
8
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0
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20
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40
50
60
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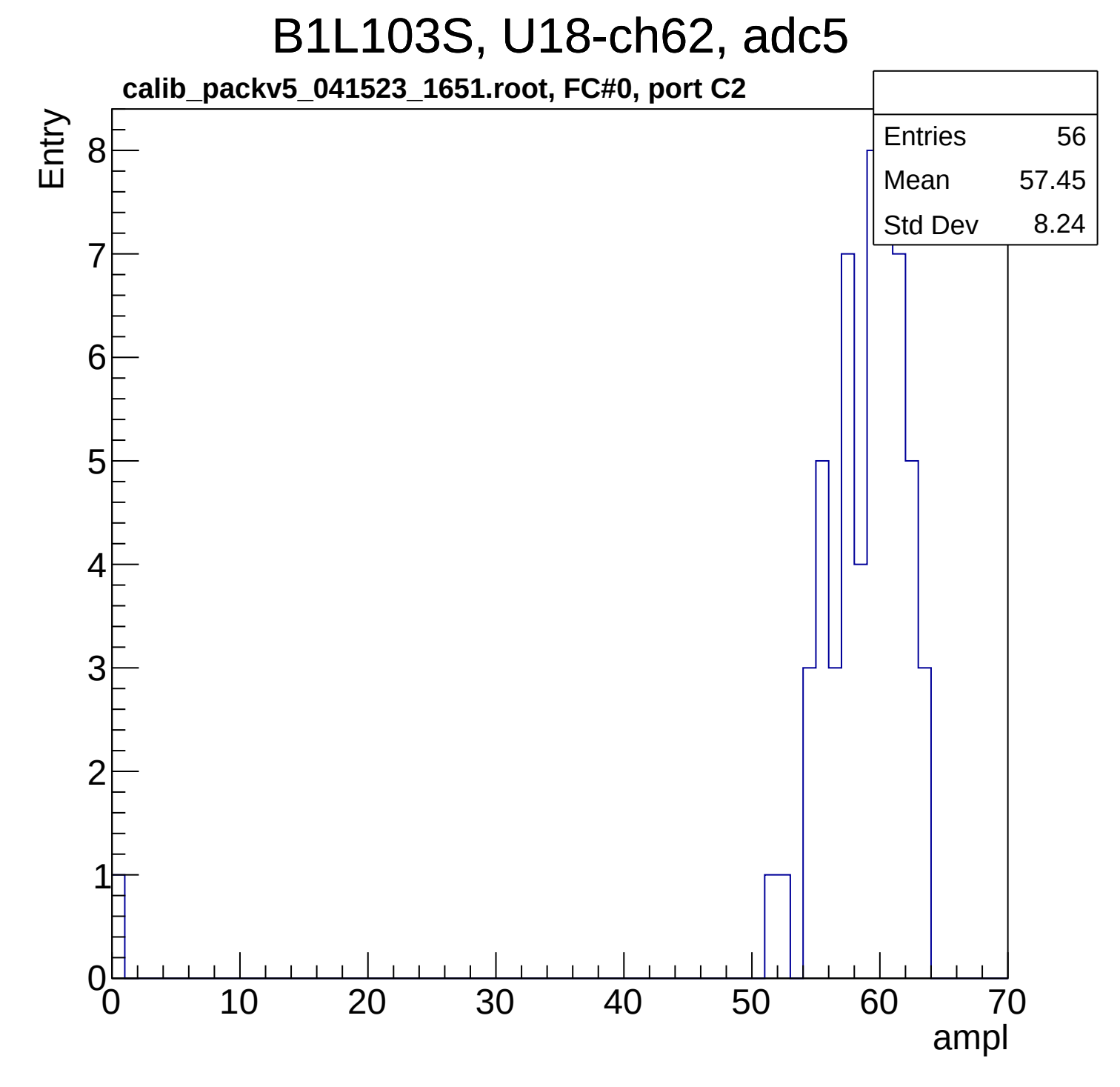
B1L103S, U18-ch62, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 57.45
Std Dev 8.24
Entry
ampl
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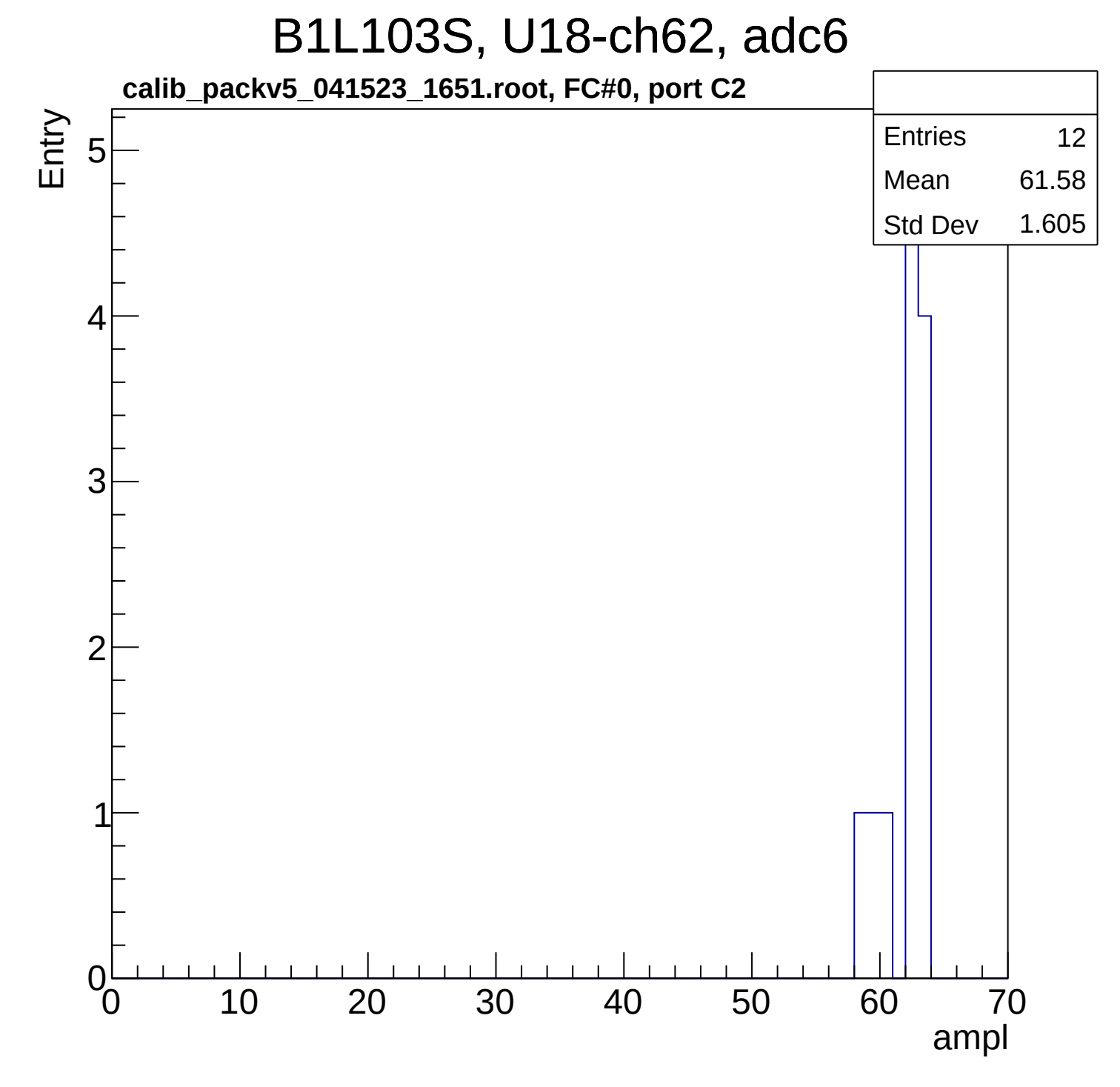
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch62, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 61.58
Std Dev 1.605
Entry
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2
3
4
5
0
10
20
30
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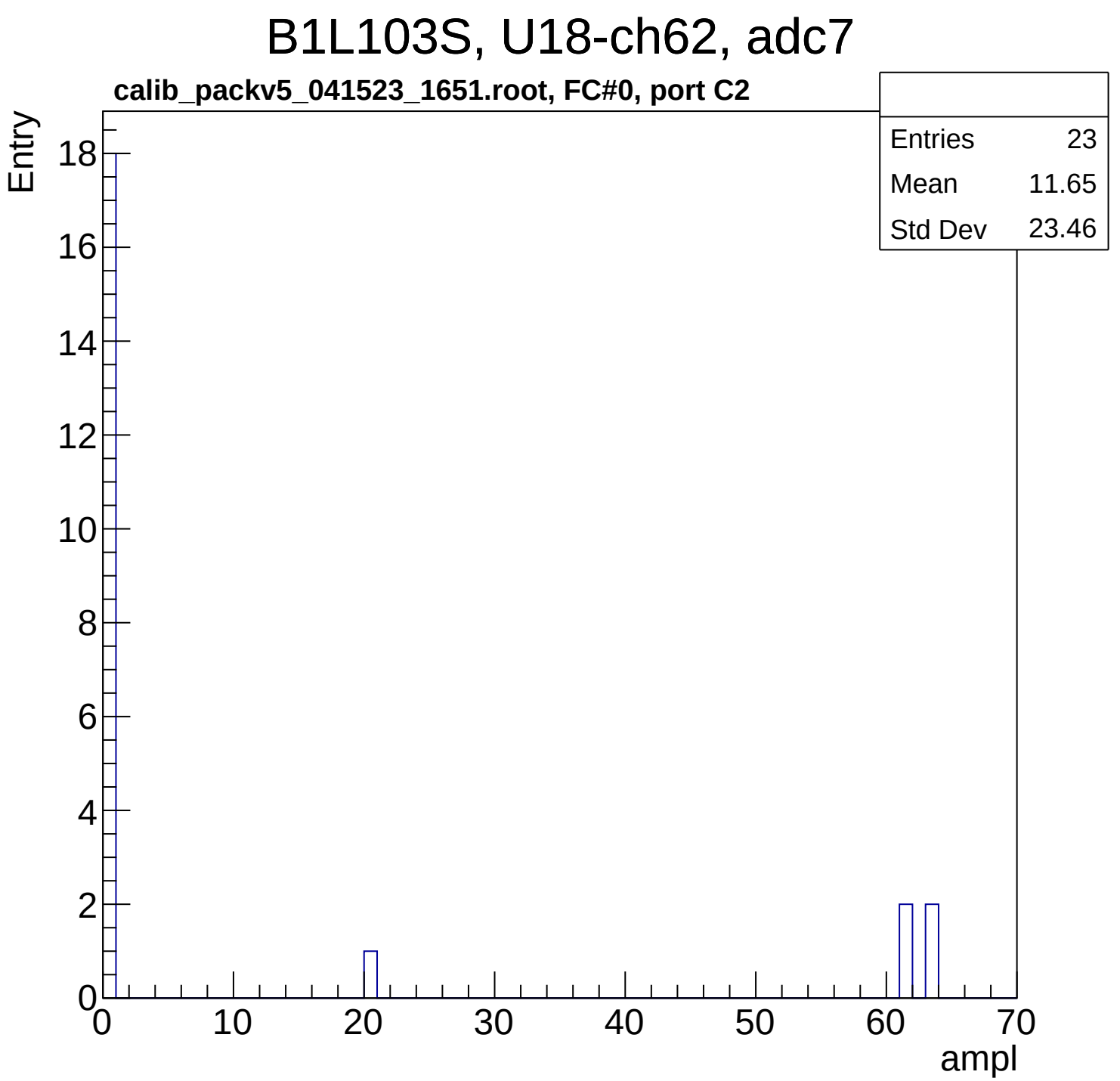
50
60
70
ampl


B1L103S, U18-ch62, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 23
Mean 11.65
Std Dev 23.46
Entry
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6
8
10
12
14
16
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10
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30
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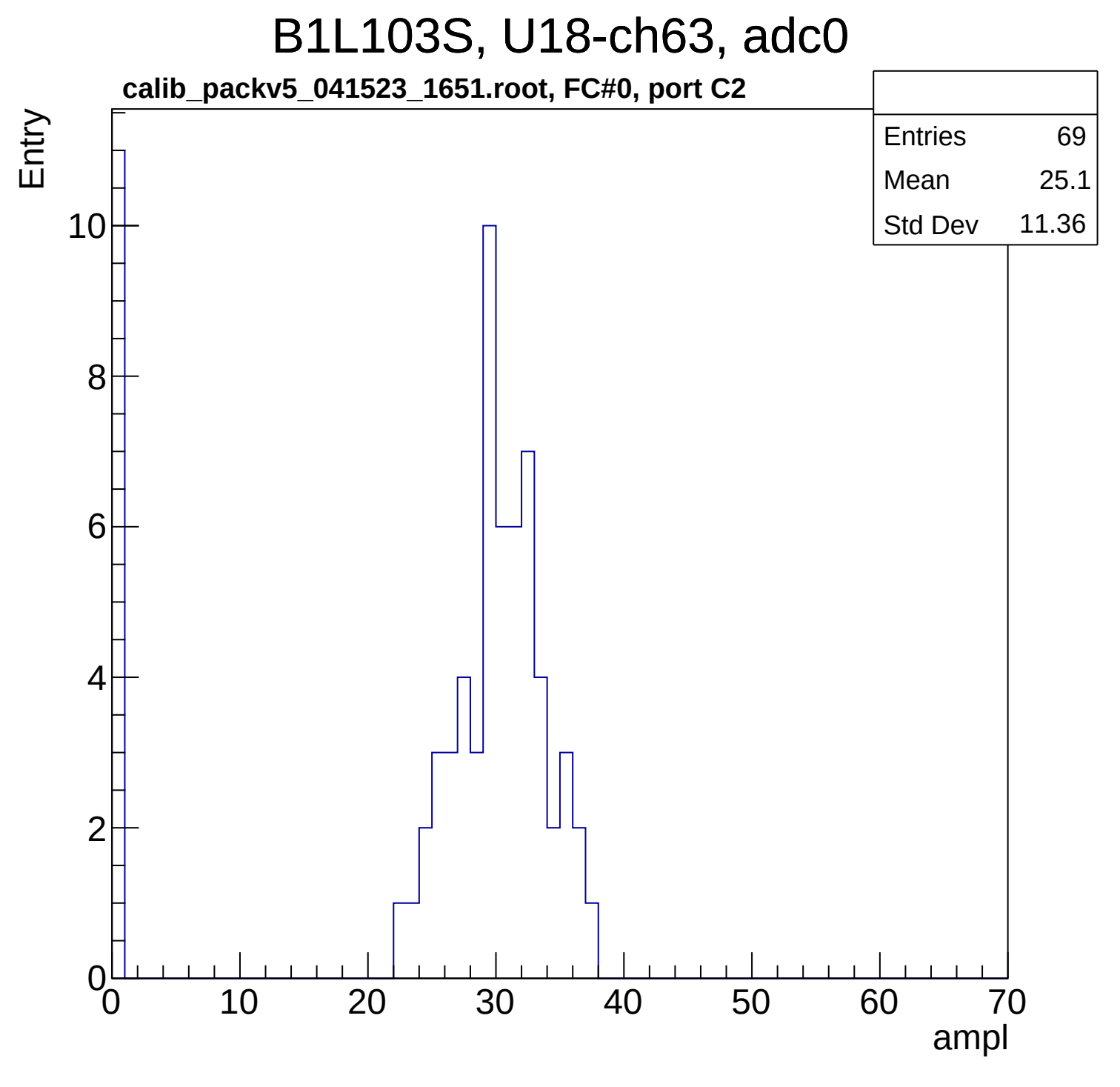
70
ampl


B1L103S, U18-ch63, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 25.1
Std Dev 11.36
Entry
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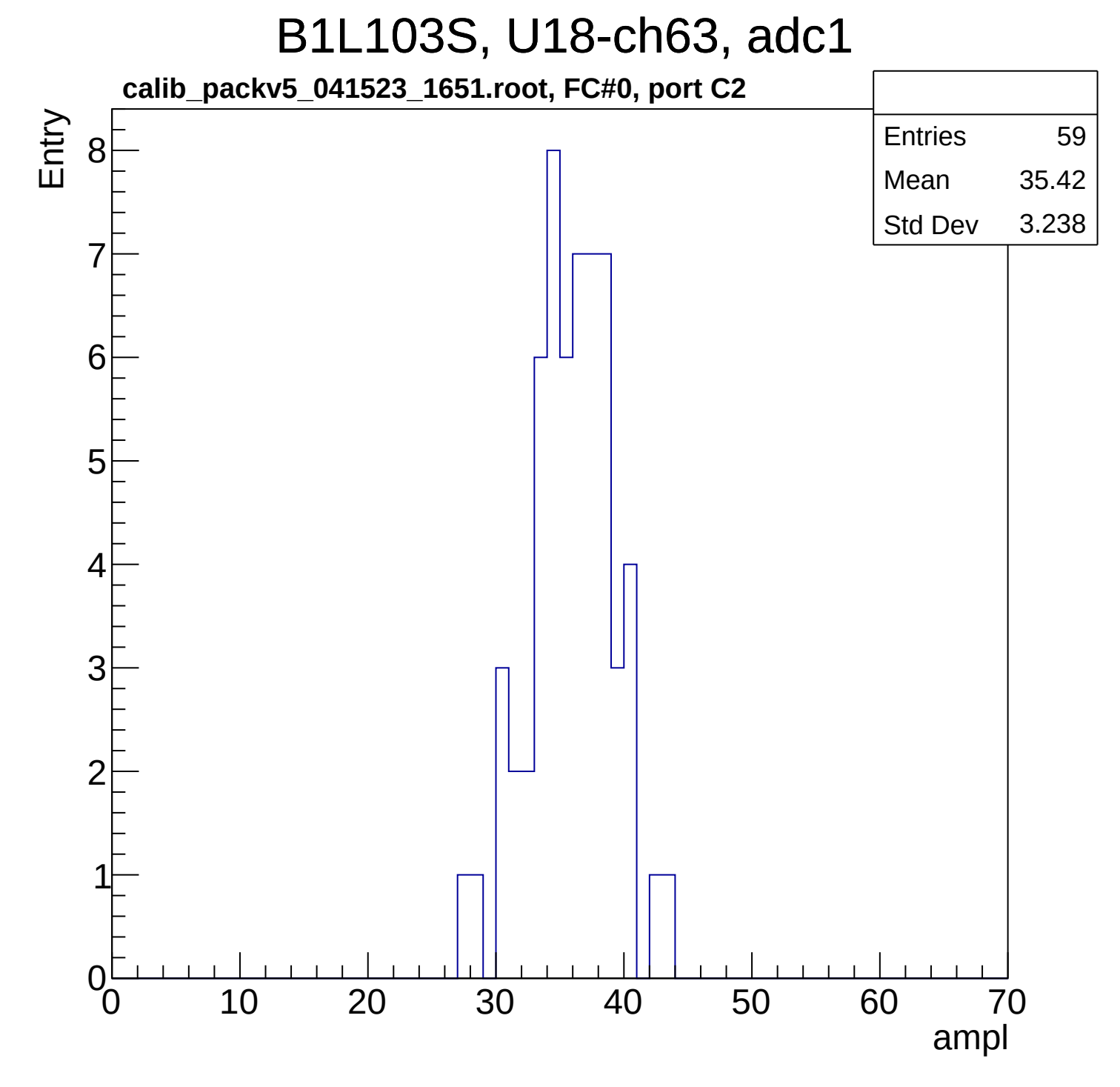
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch63, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 35.42
Std Dev 3.238
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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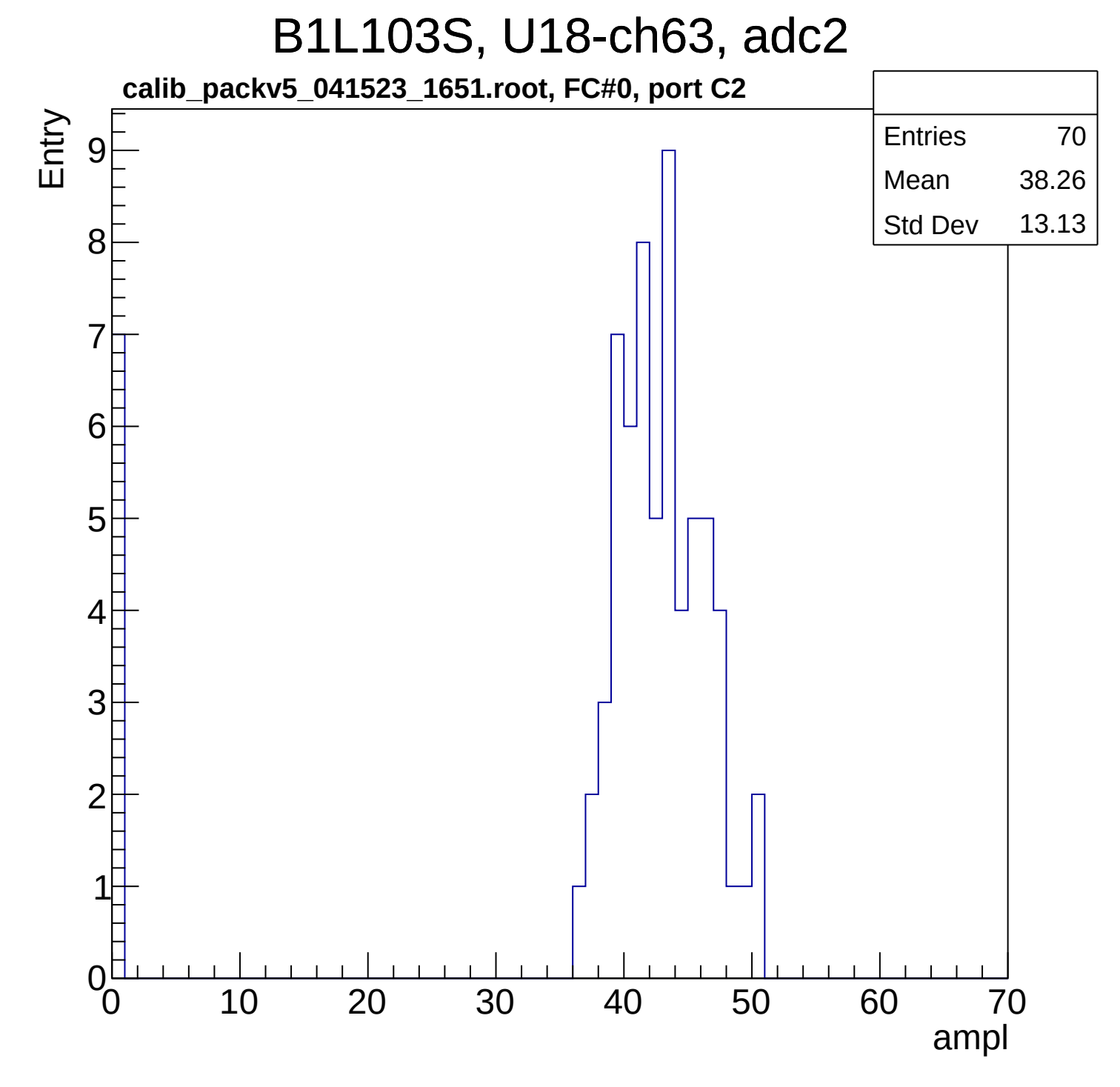
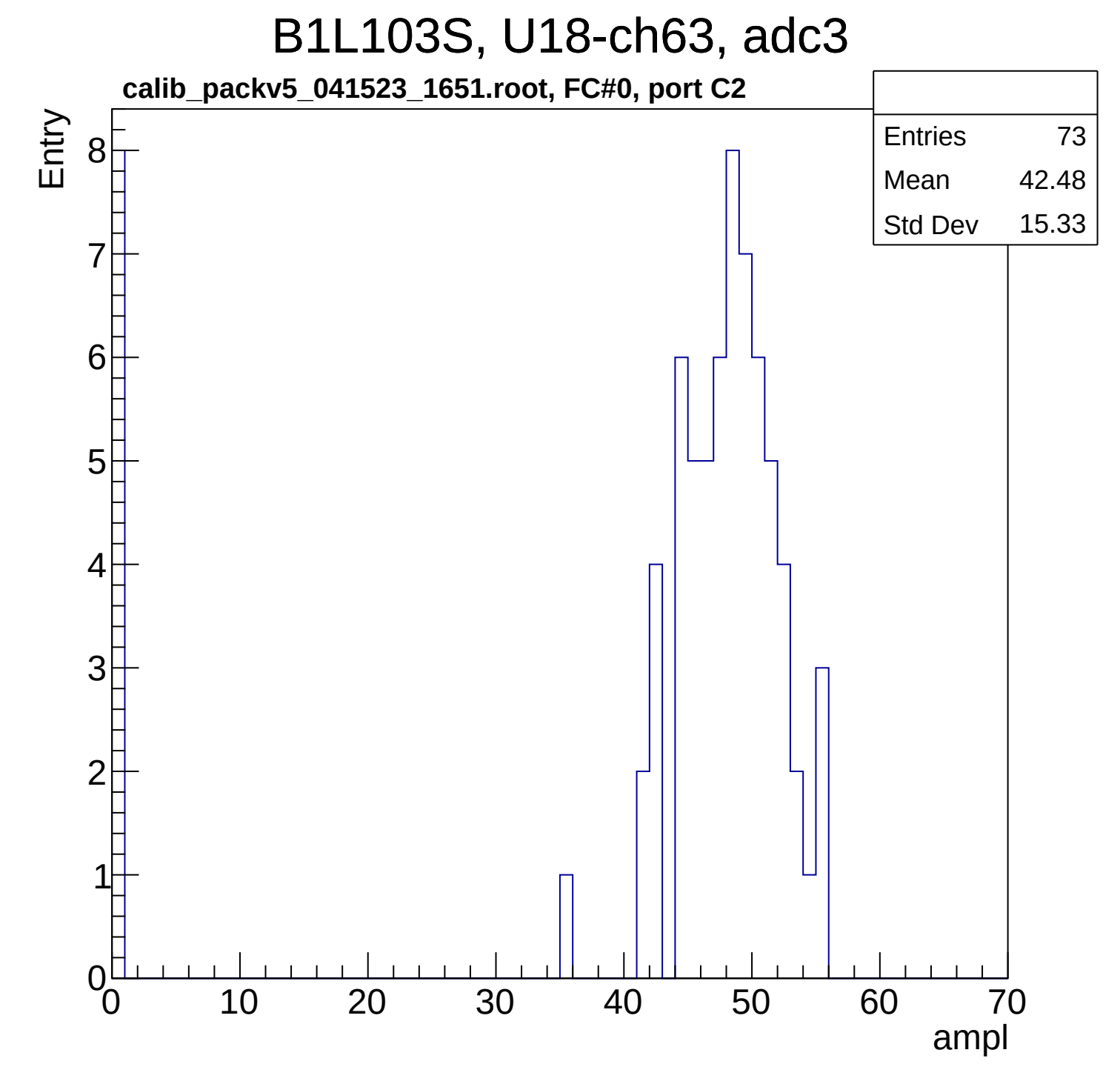
40
50
60
70


B1L103S, U18-ch63, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 38.26
Std Dev 13.13
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U18-ch63, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 42.48
Std Dev 15.33
Entry
ampl
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1
2
3
4
5
6
7
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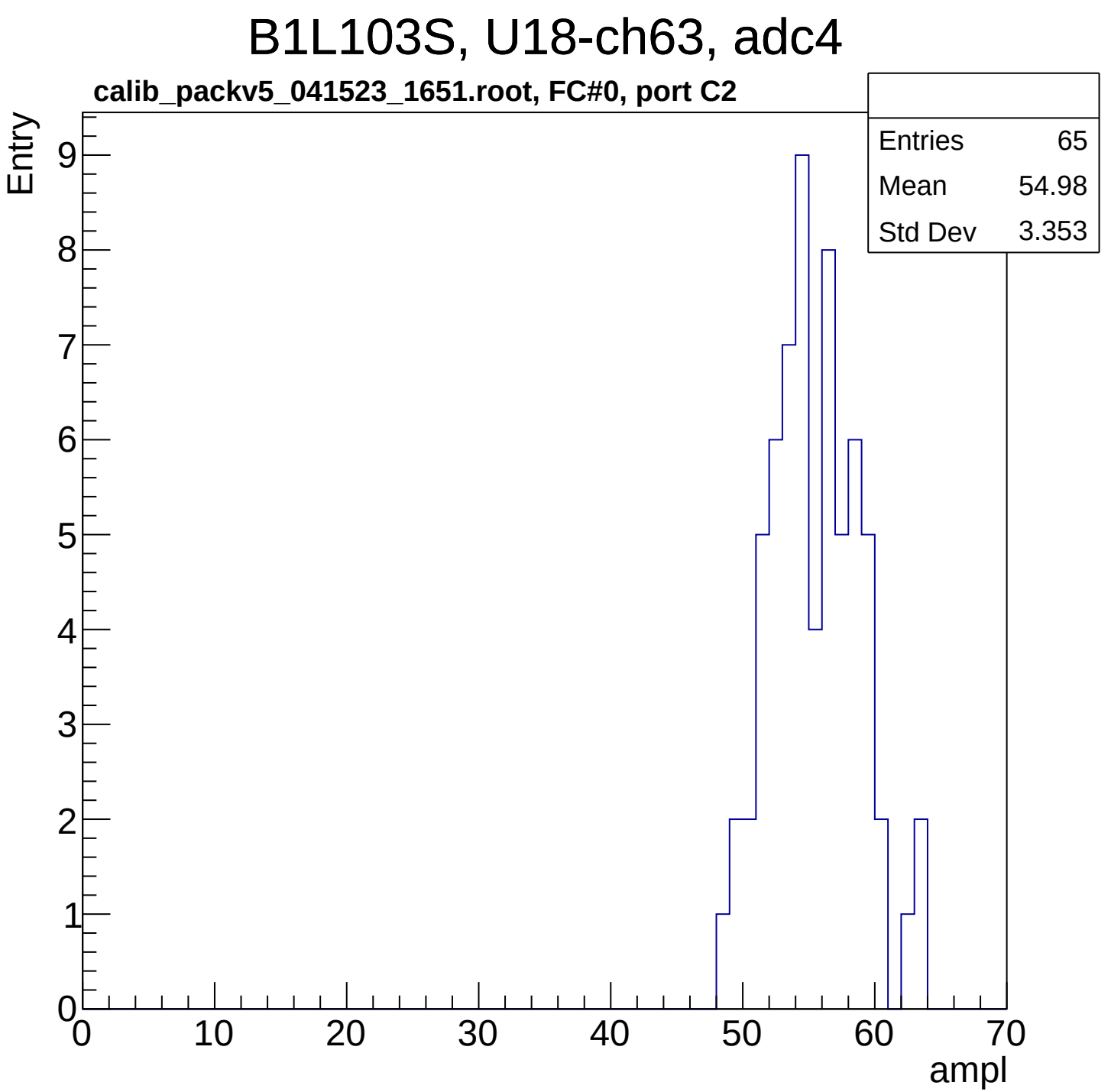
B1L103S, U18-ch63, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 54.98
Std Dev 3.353
Entry
ampl
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2
3
4
5
6
7
8
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0
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40
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60
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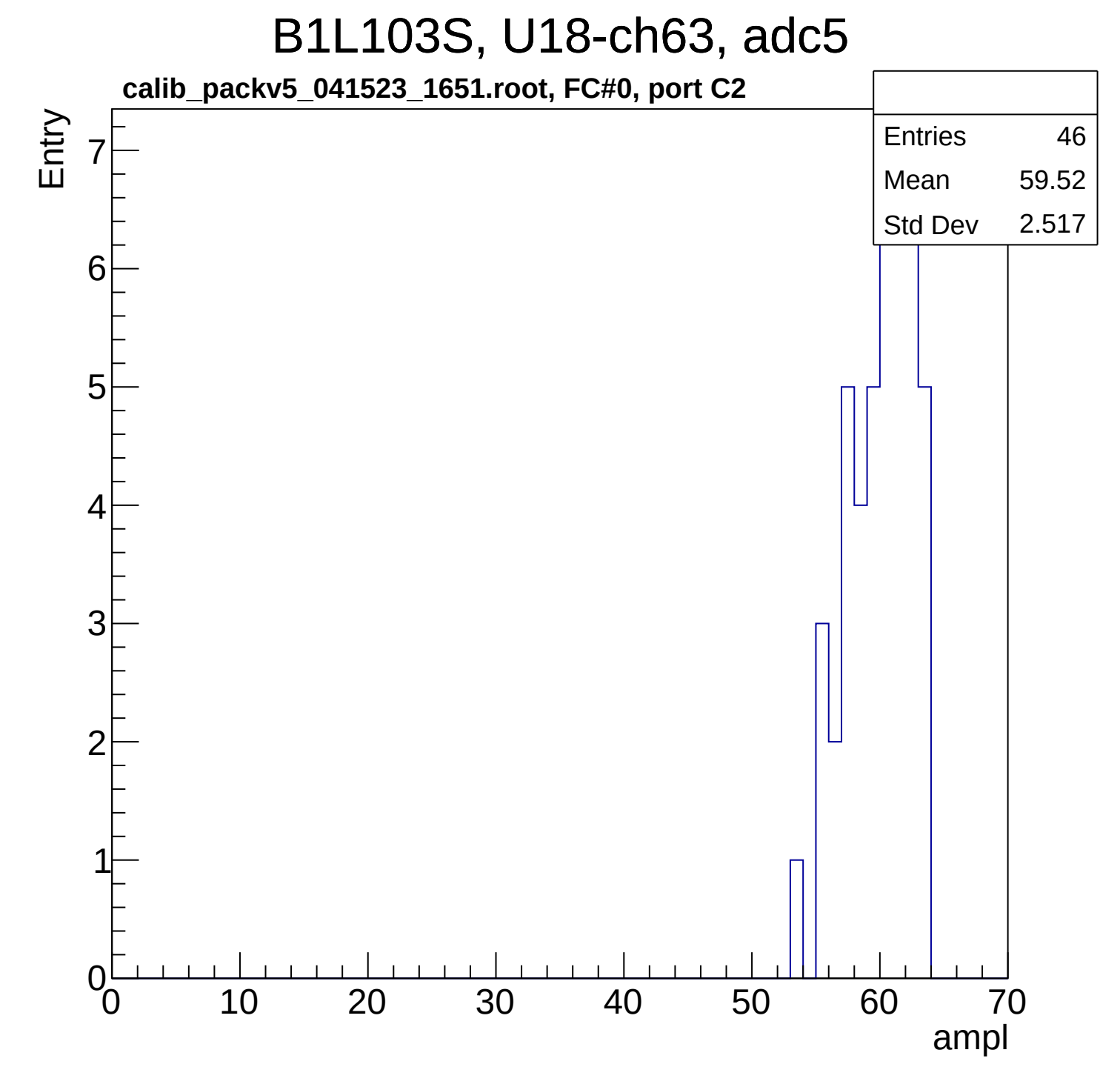
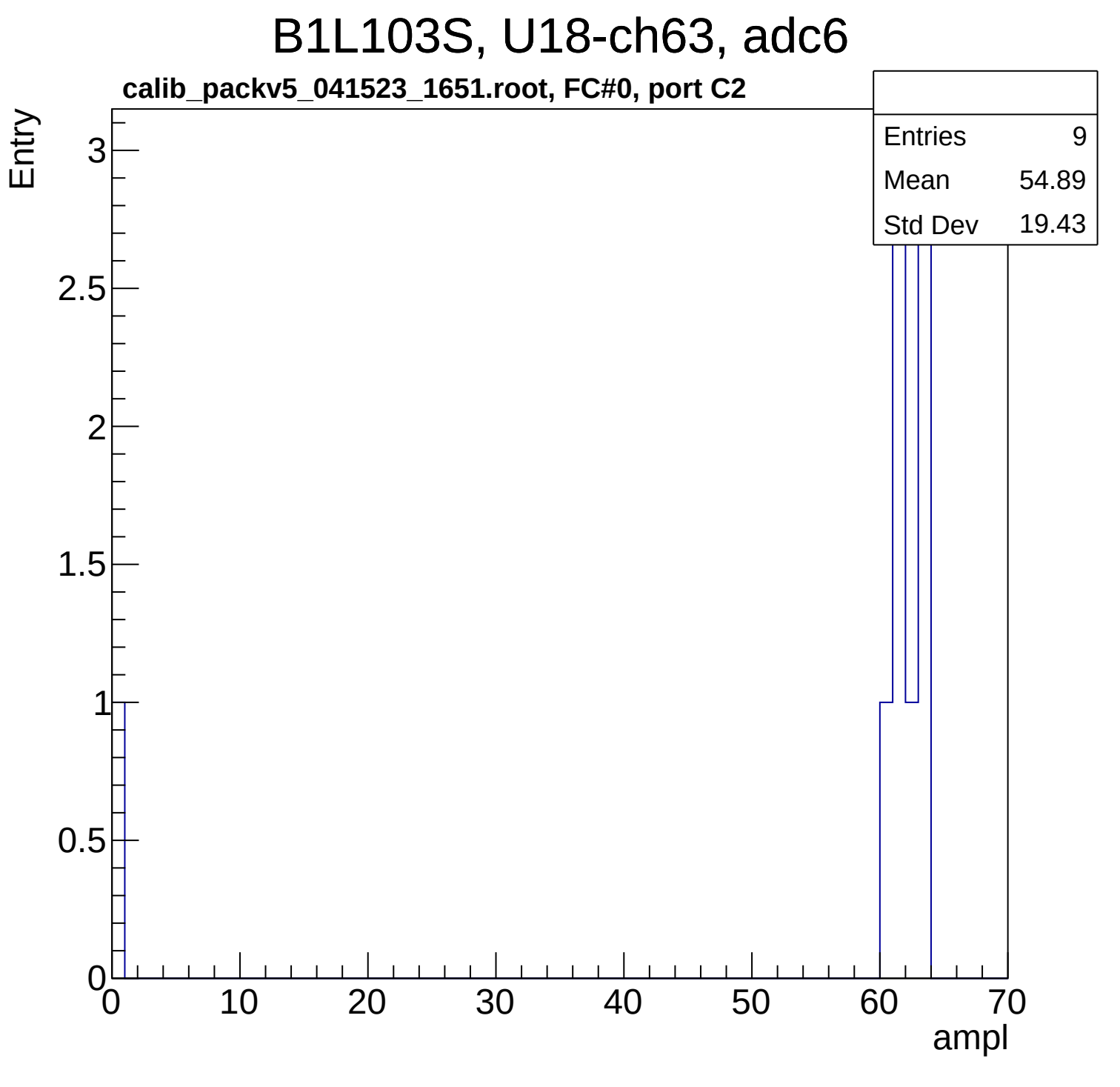

B1L103S, U18-ch63, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 59.52
Std Dev 2.517
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U18-ch63, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 9
Mean 54.89
Std Dev 19.43
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
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20
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40
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60
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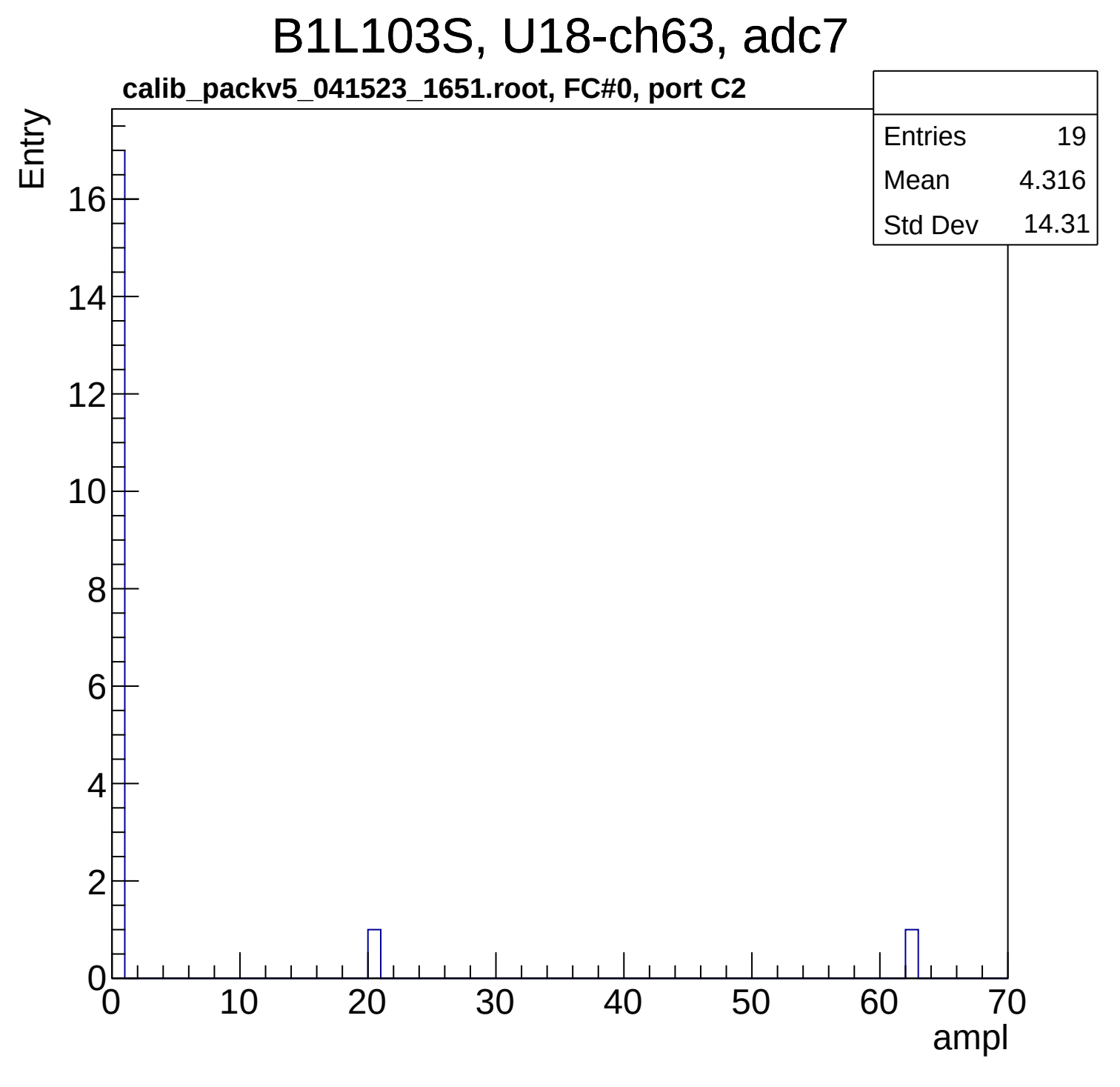
B1L103S, U18-ch63, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 4.316
Std Dev 14.31
Entry
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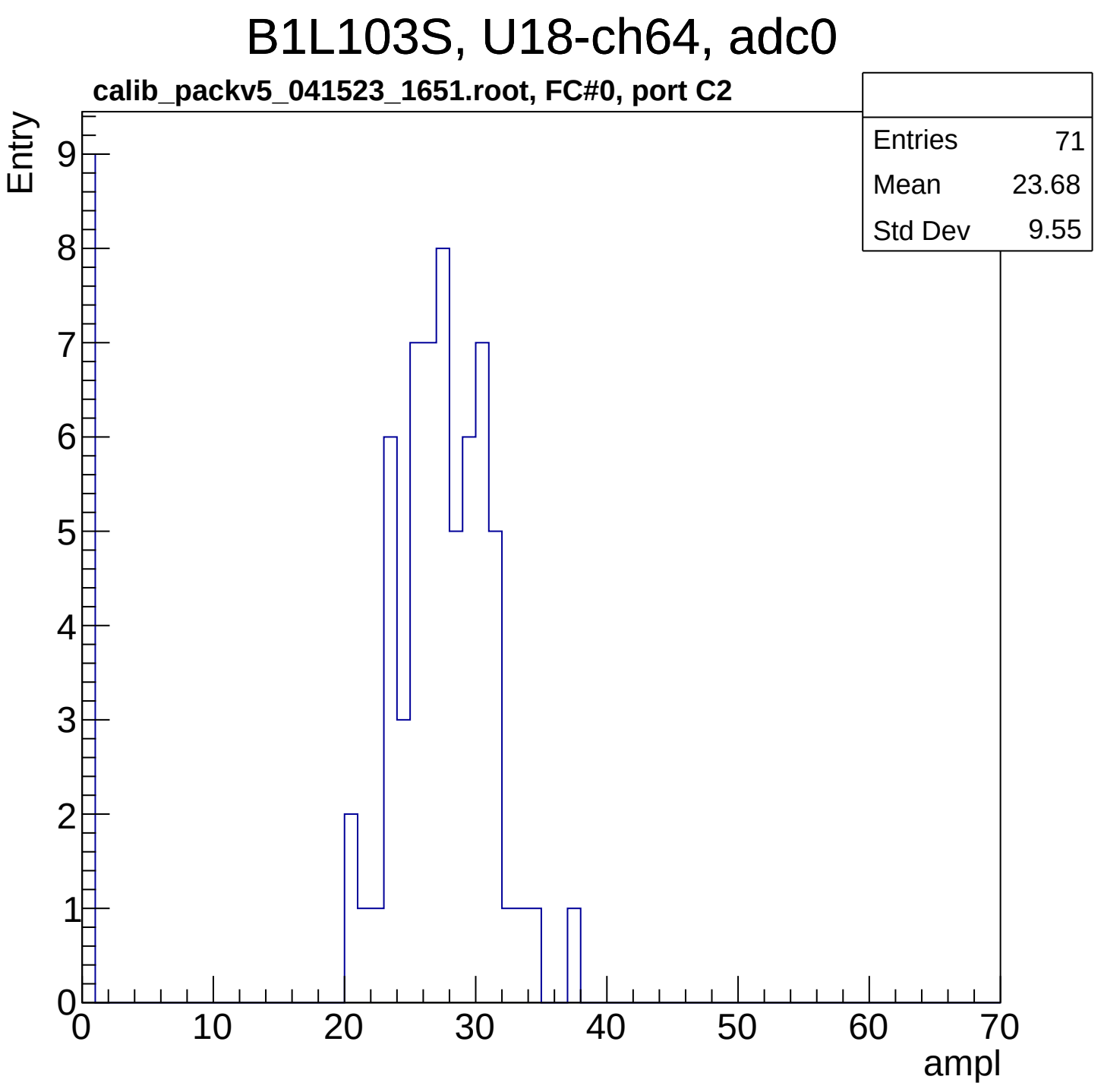
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch64, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 23.68
Std Dev 9.55
Entry
ampl
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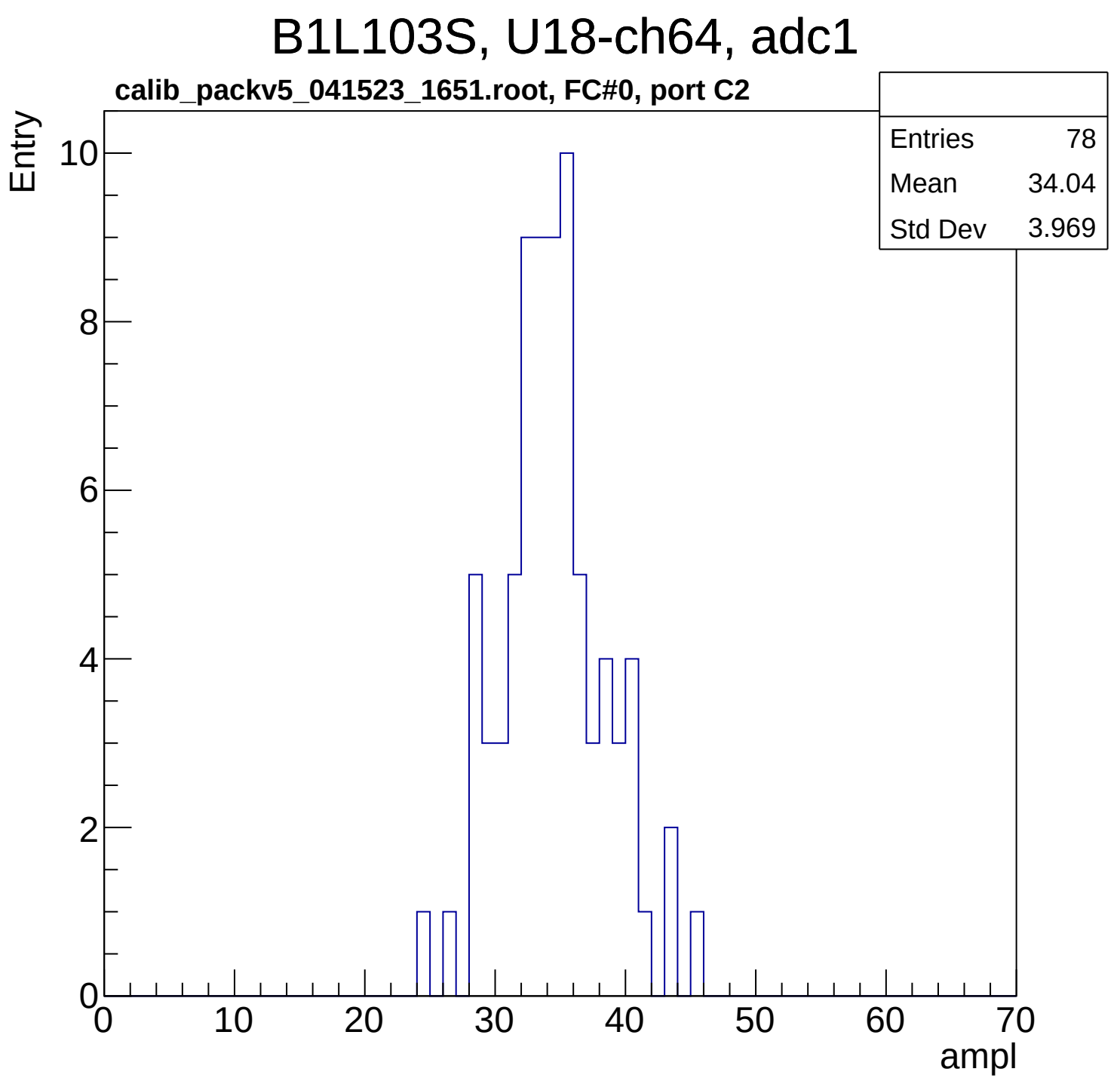
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U18-ch64, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 34.04
Std Dev 3.969
Entry
ampl
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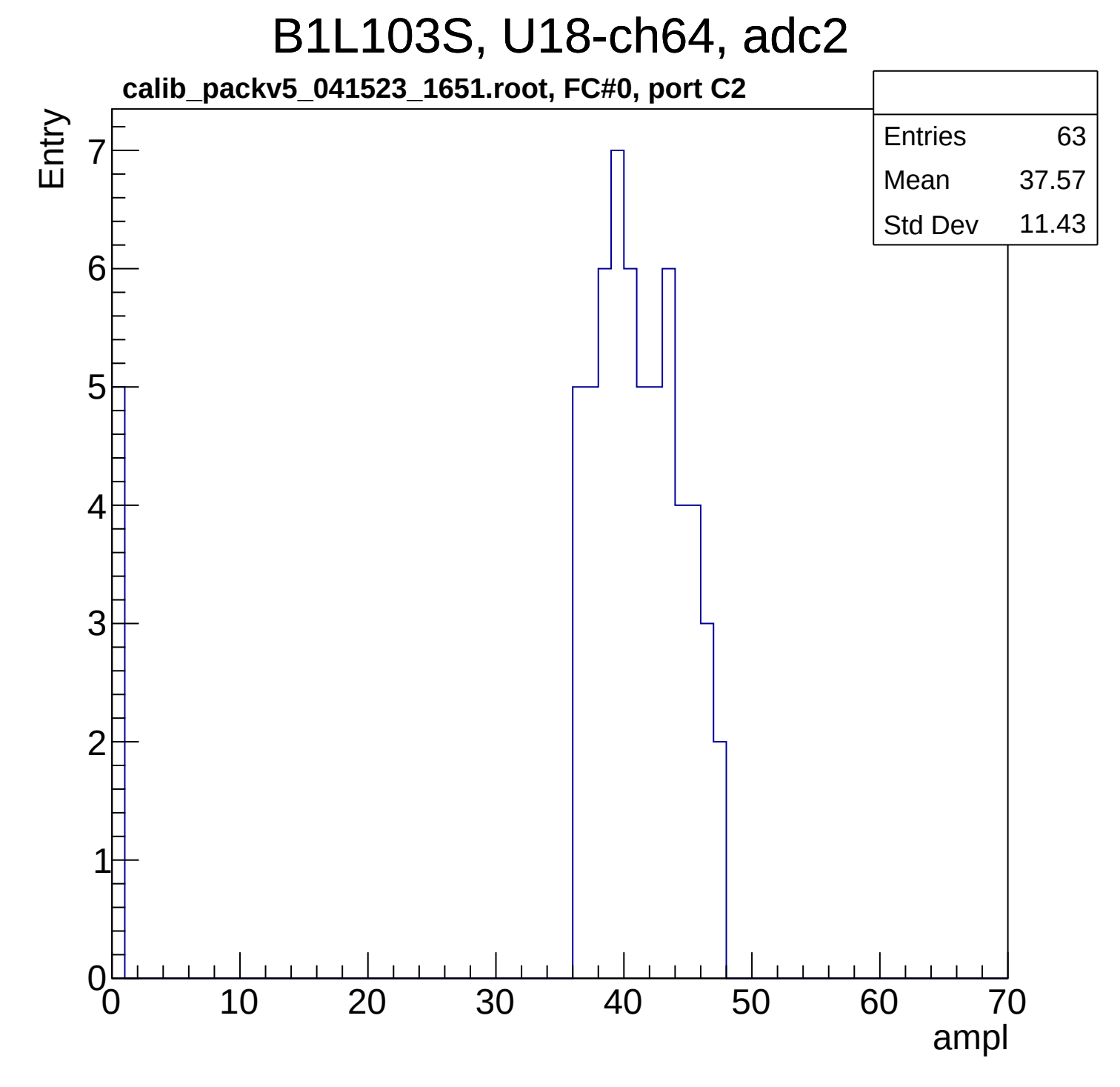
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U18-ch64, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 37.57
Std Dev 11.43
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
30
40
50
60
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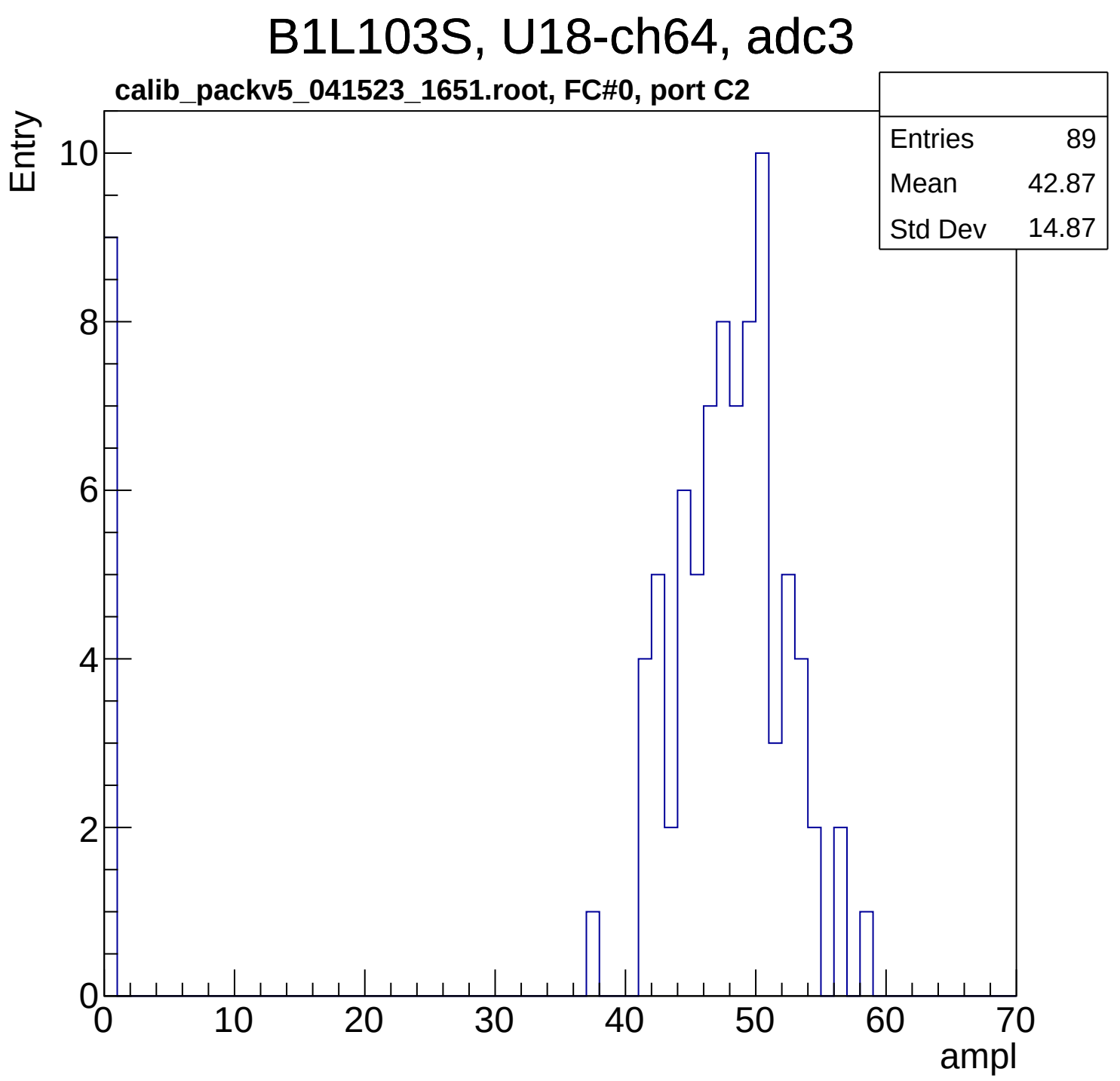
B1L103S, U18-ch64, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 89
Mean 42.87
Std Dev 14.87
Entry
ampl
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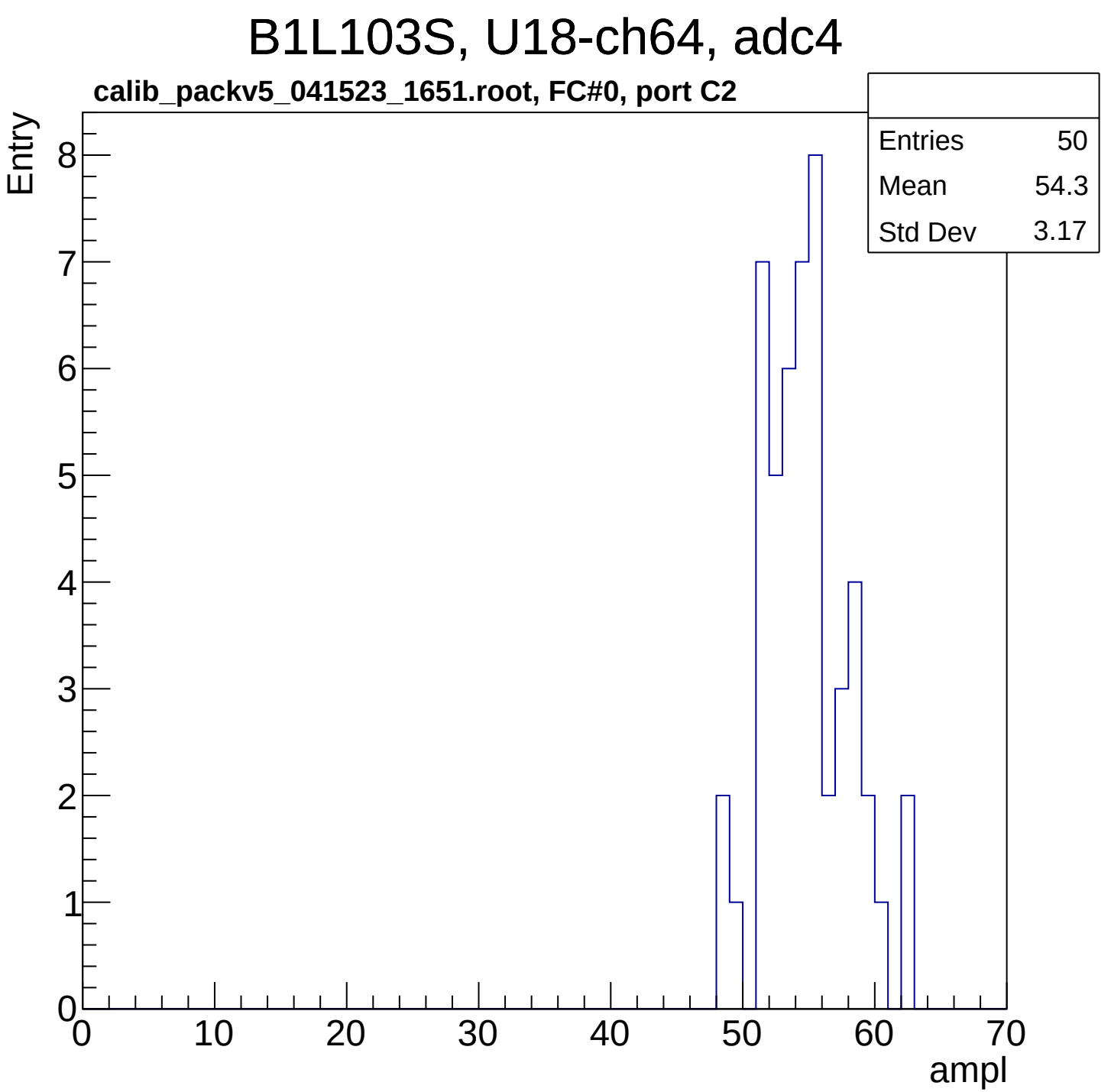
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U18-ch64, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 54.3
Std Dev 3.17
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
30
40
50
60
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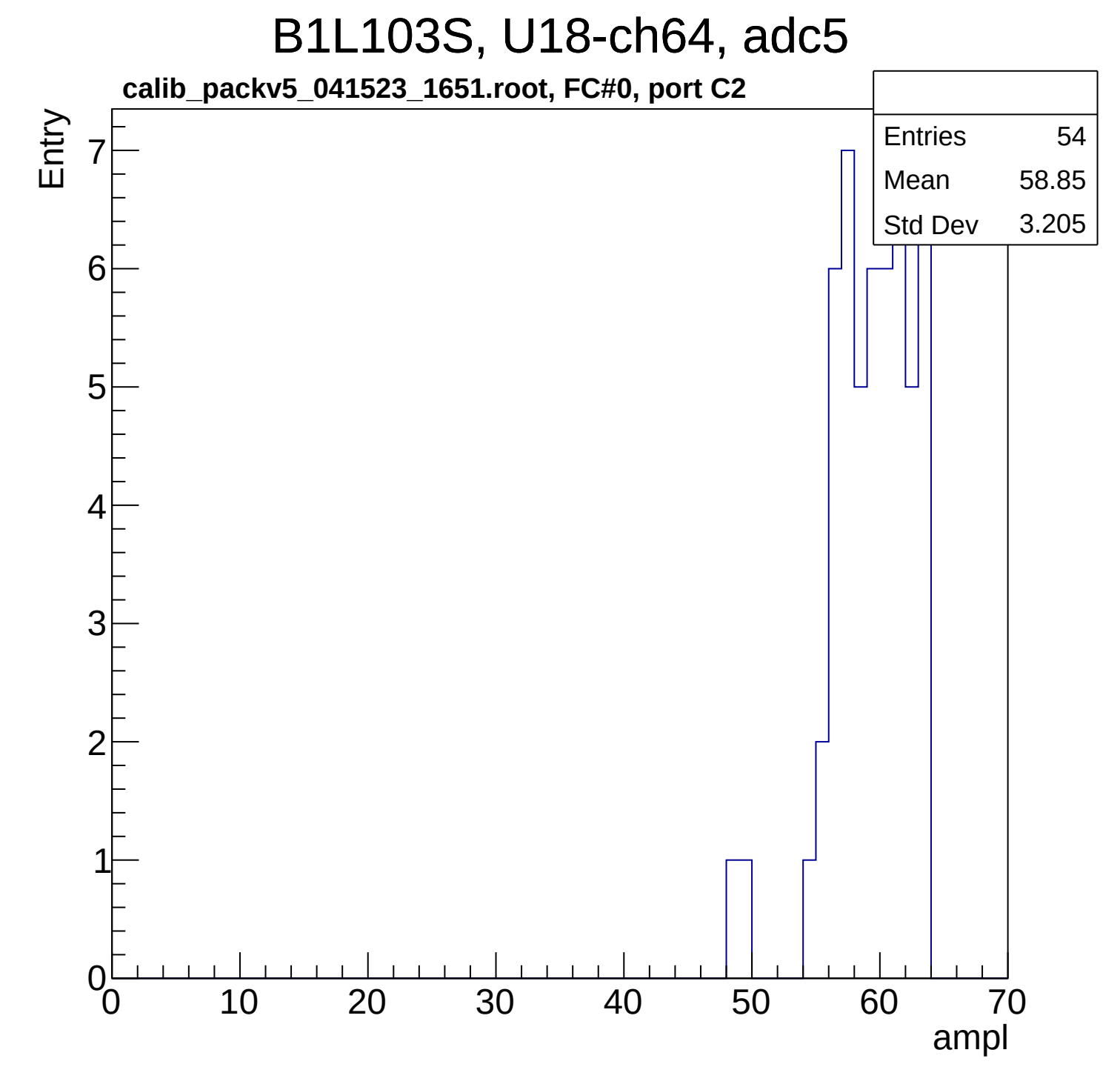
B1L103S, U18-ch64, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 58.85
Std Dev 3.205
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
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40
50
60
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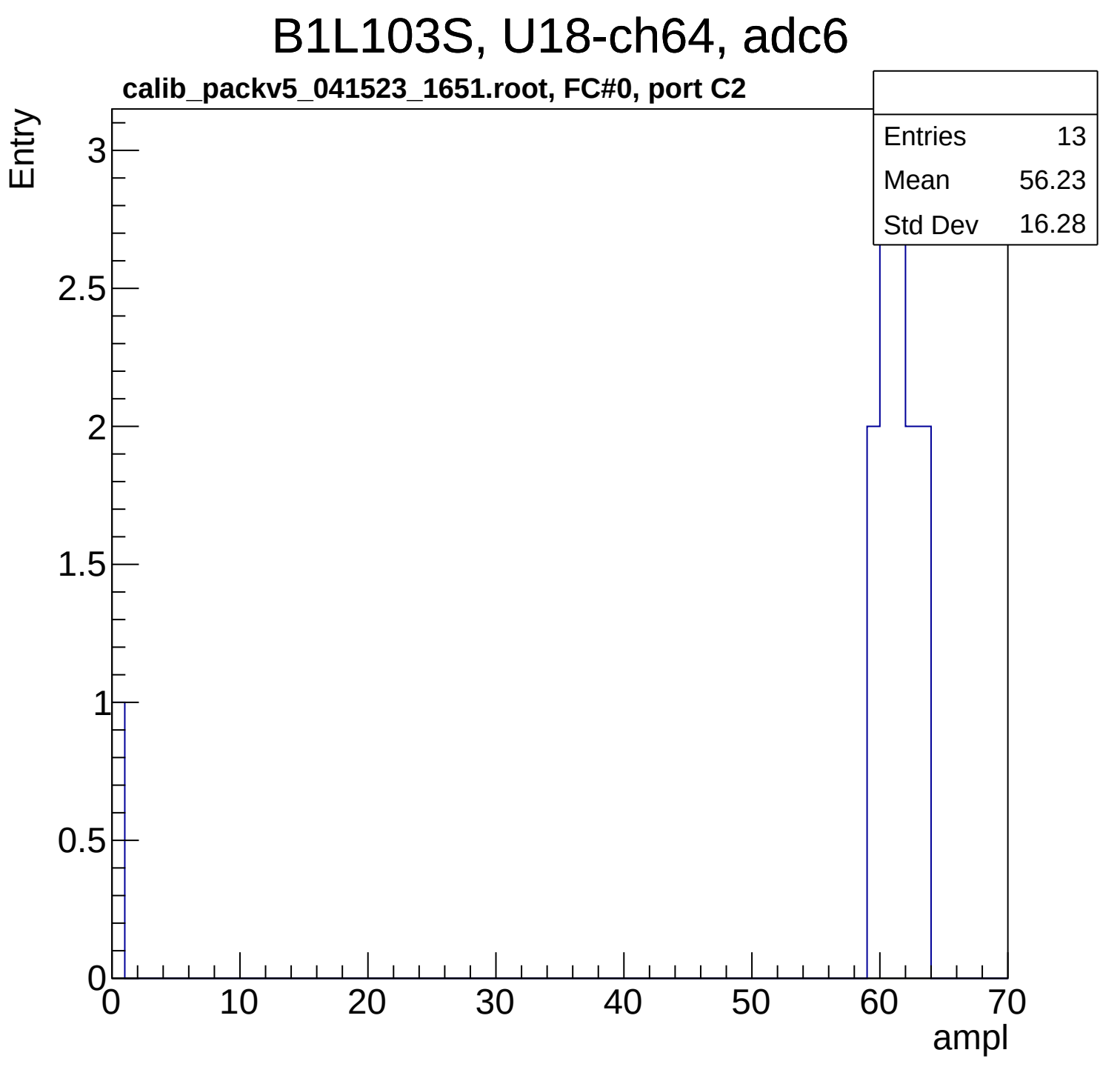
B1L103S, U18-ch64, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 13
Mean 56.23
Std Dev 16.28
Entry
ampl
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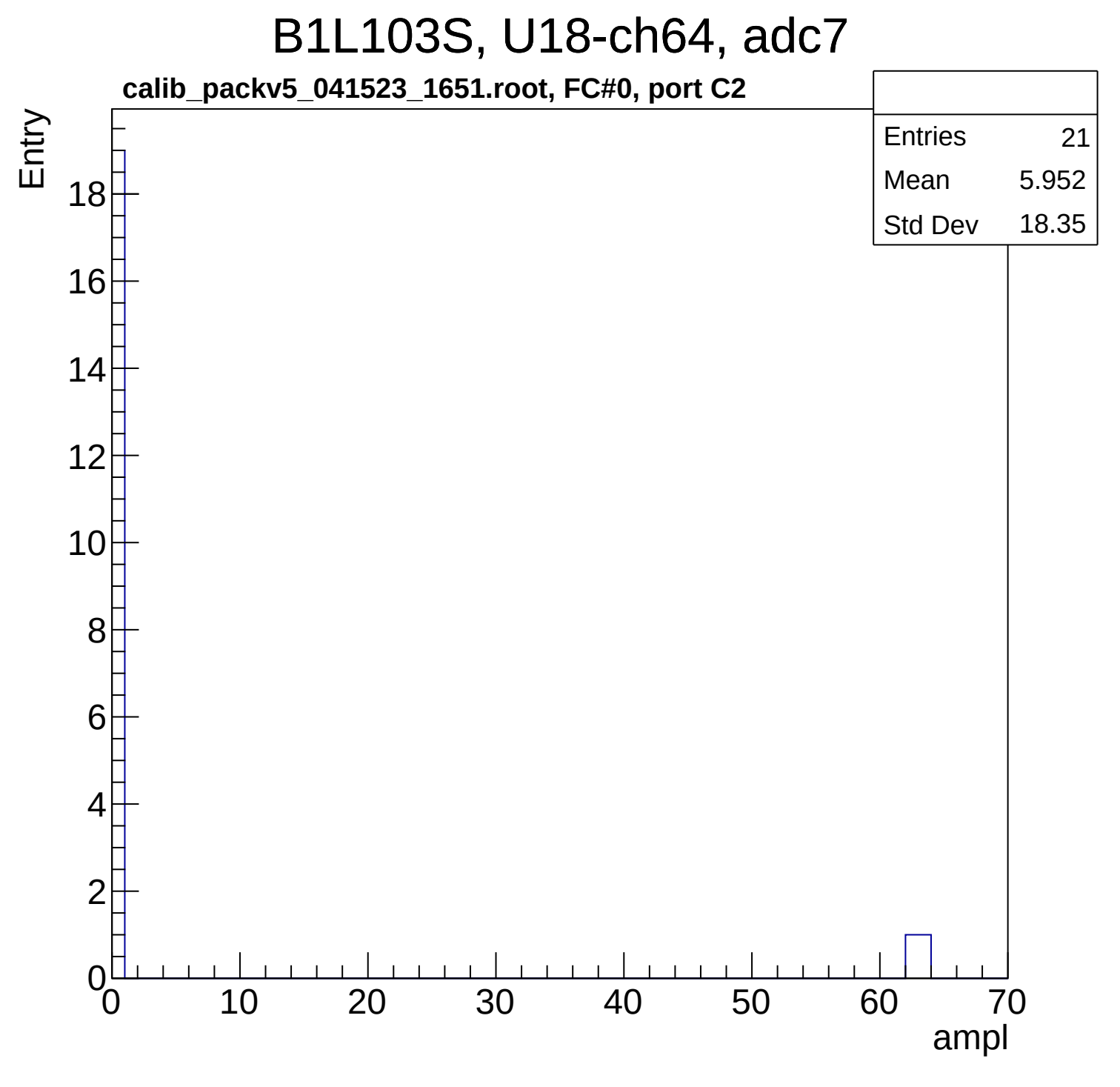
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U18-ch64, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 5.952
Std Dev 18.35
Entry
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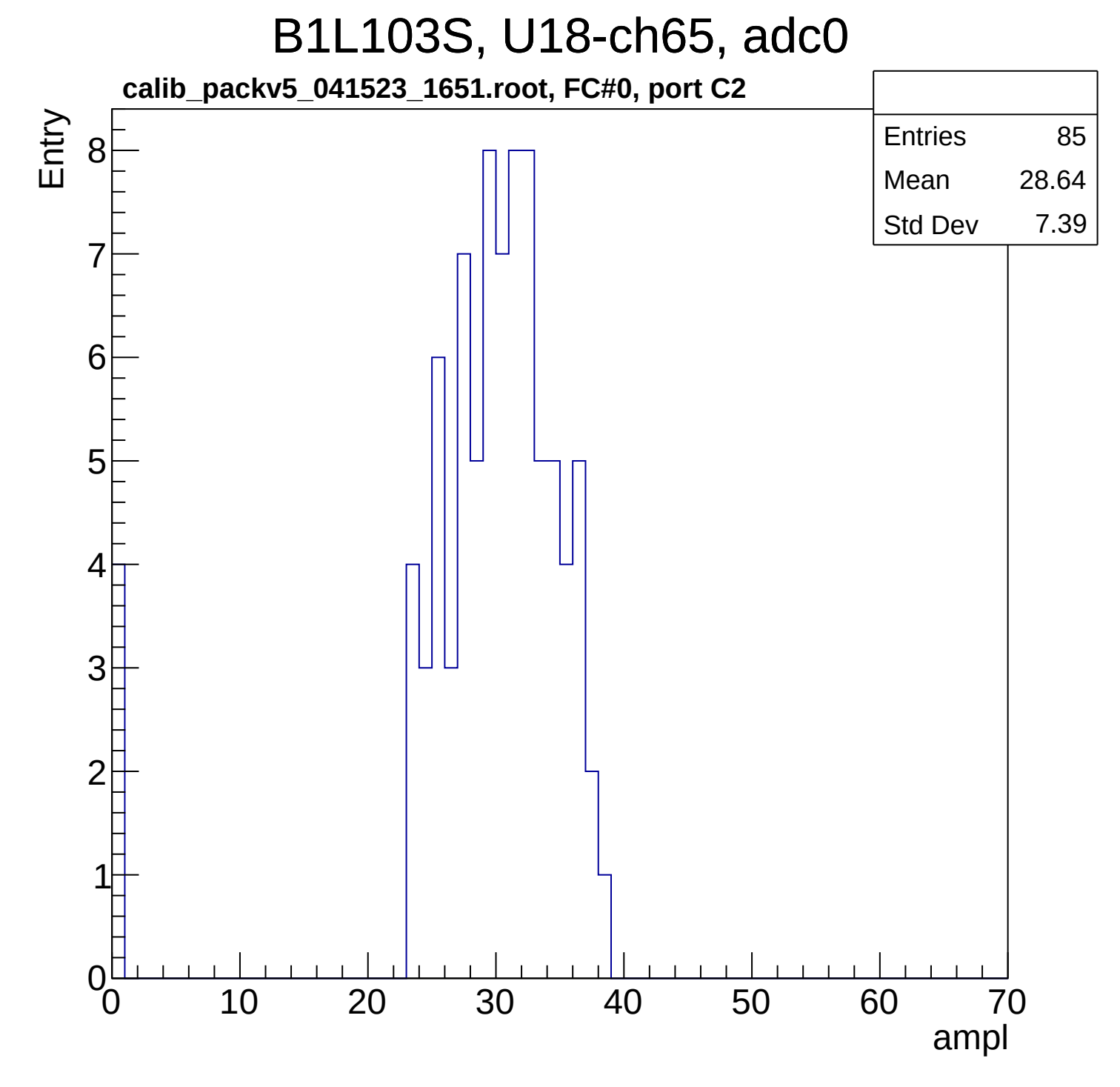
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch65, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 28.64
Std Dev 7.39
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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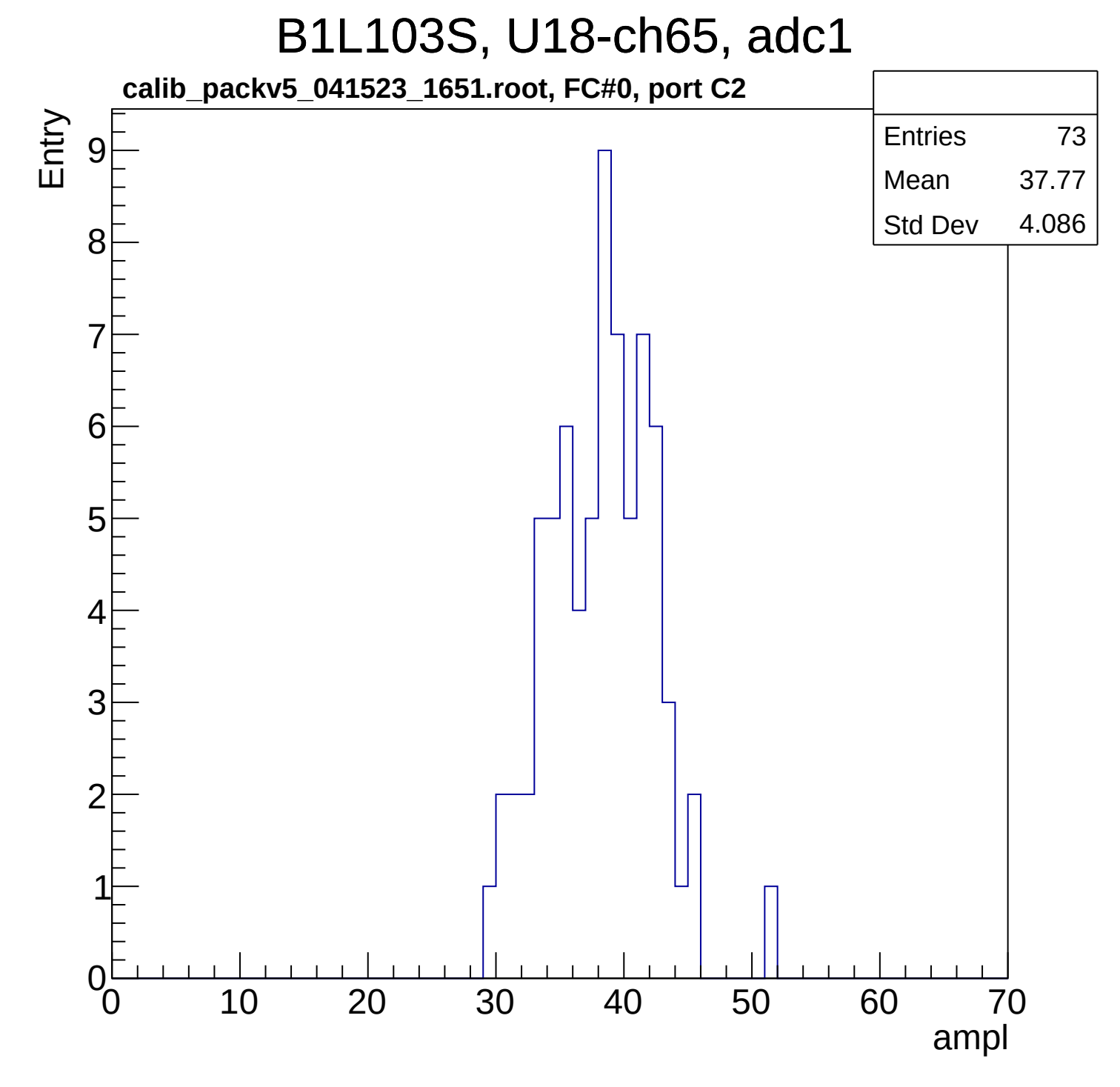
B1L103S, U18-ch65, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 37.77
Std Dev 4.086
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
30
40
50
60
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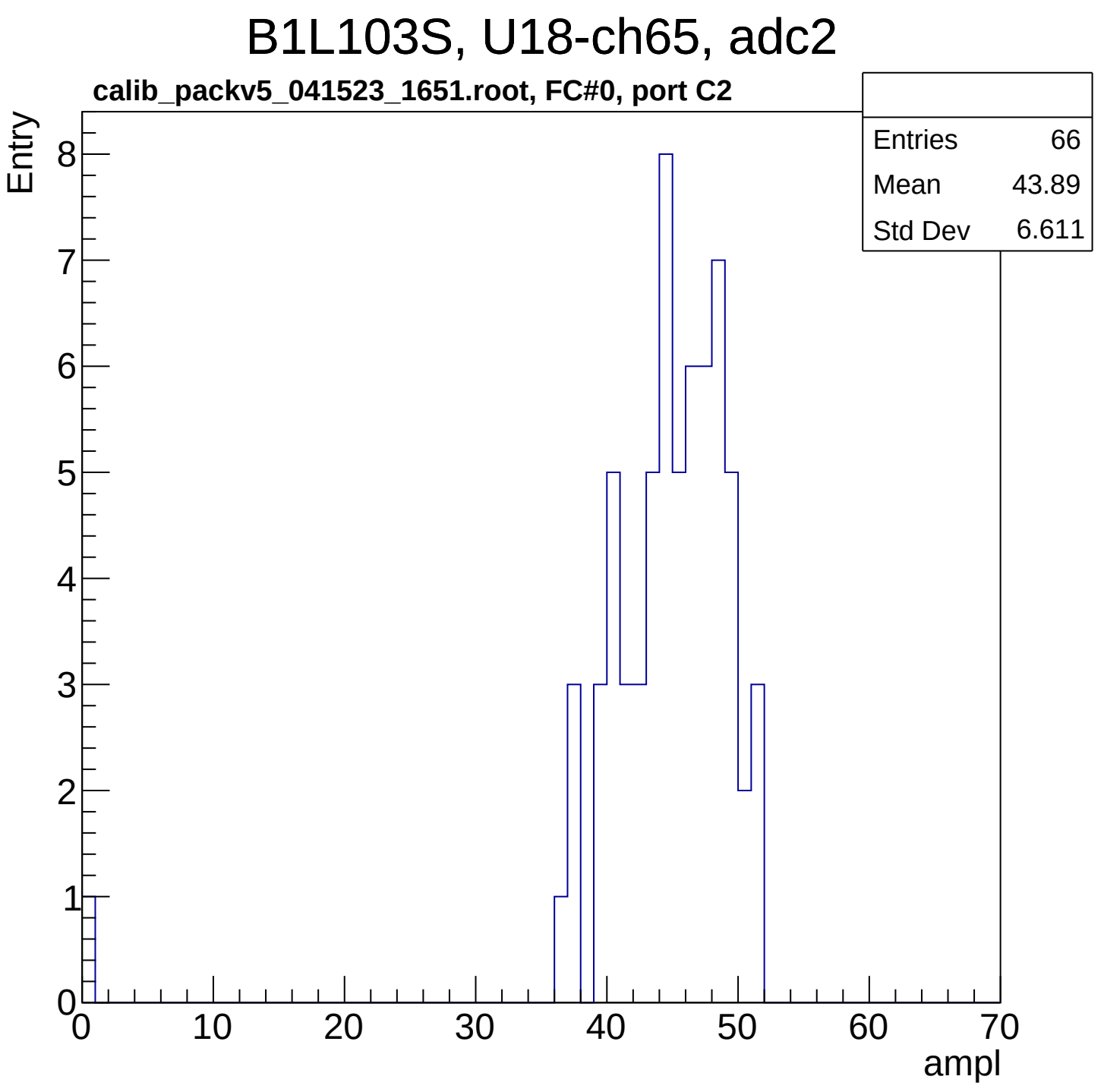
B1L103S, U18-ch65, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 43.89
Std Dev 6.611
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
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60
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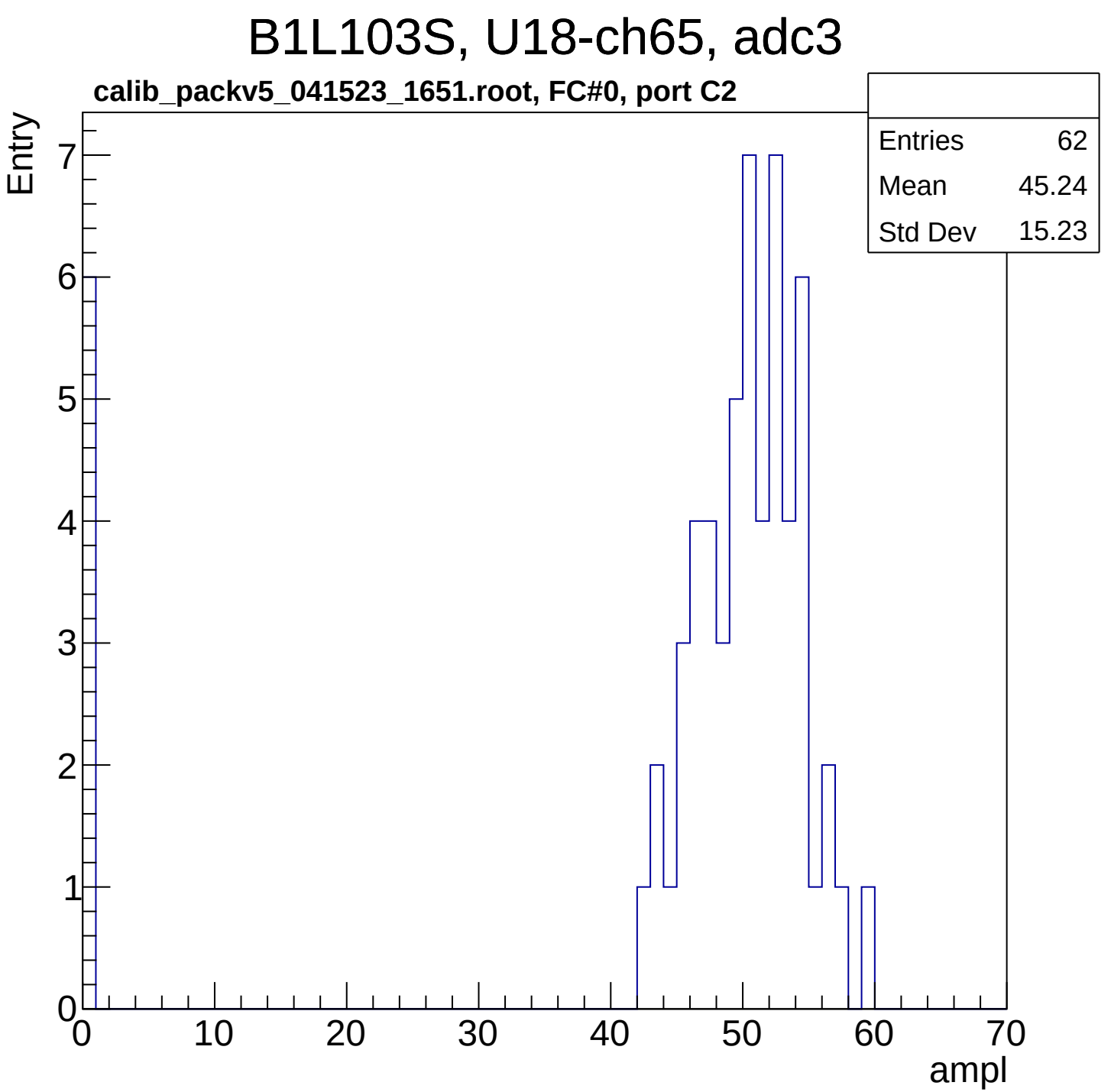
B1L103S, U18-ch65, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 45.24
Std Dev 15.23
Entry
ampl
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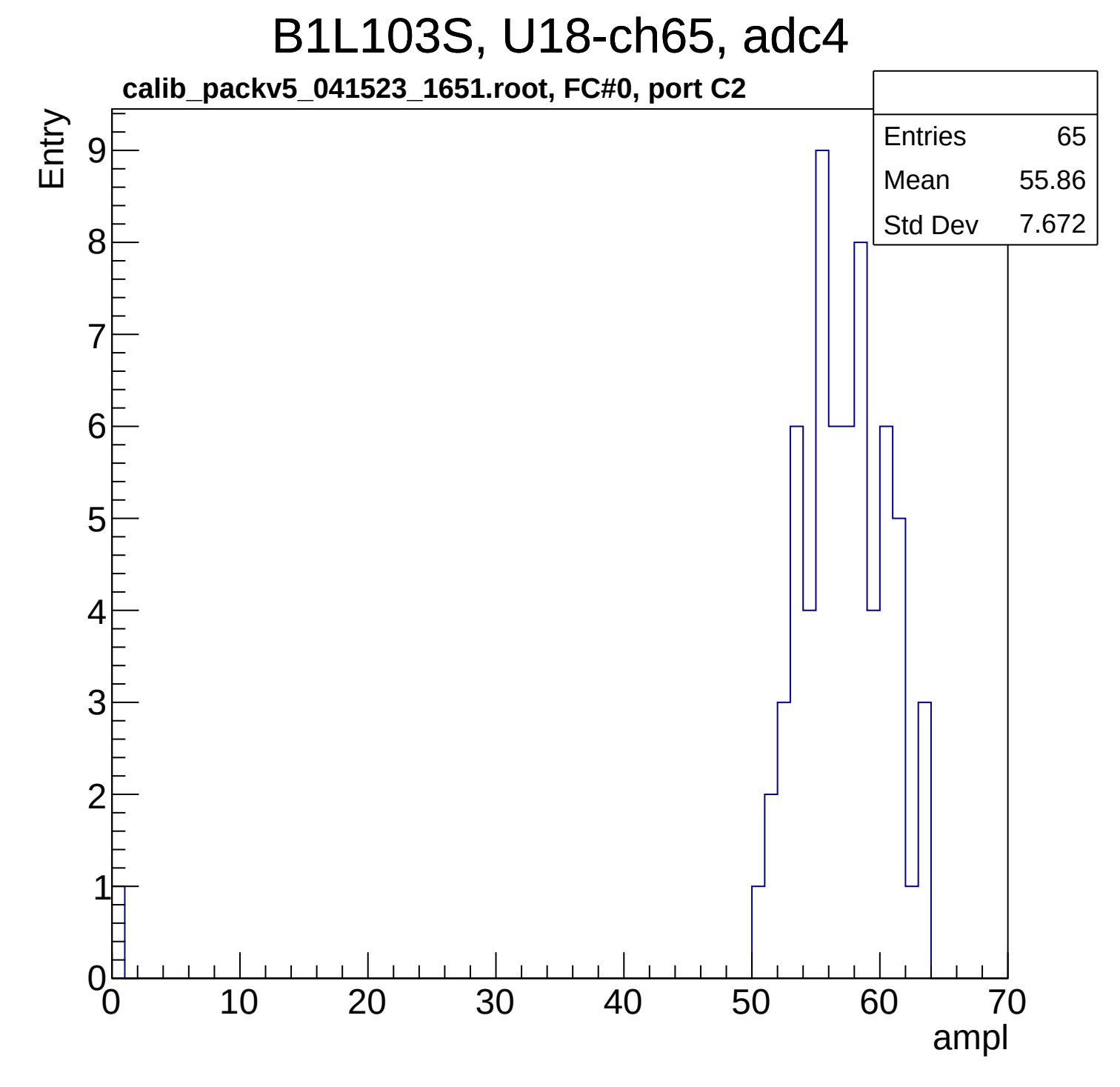
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U18-ch65, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 55.86
Std Dev 7.672
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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40
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60
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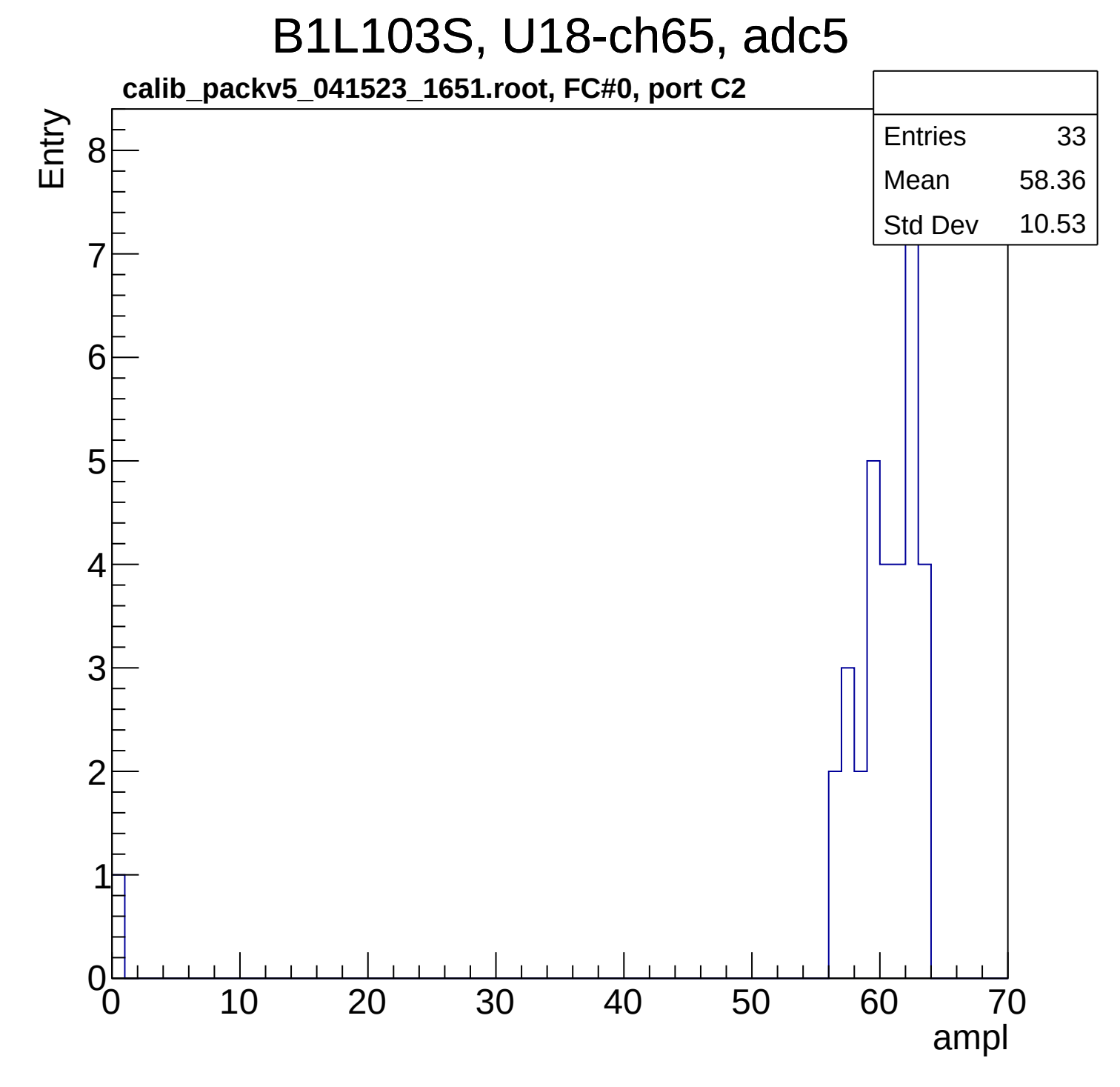
B1L103S, U18-ch65, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 33
Mean 58.36
Std Dev 10.53
Entry
ampl
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2
3
4
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6
7
8
0
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20
30
40
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60
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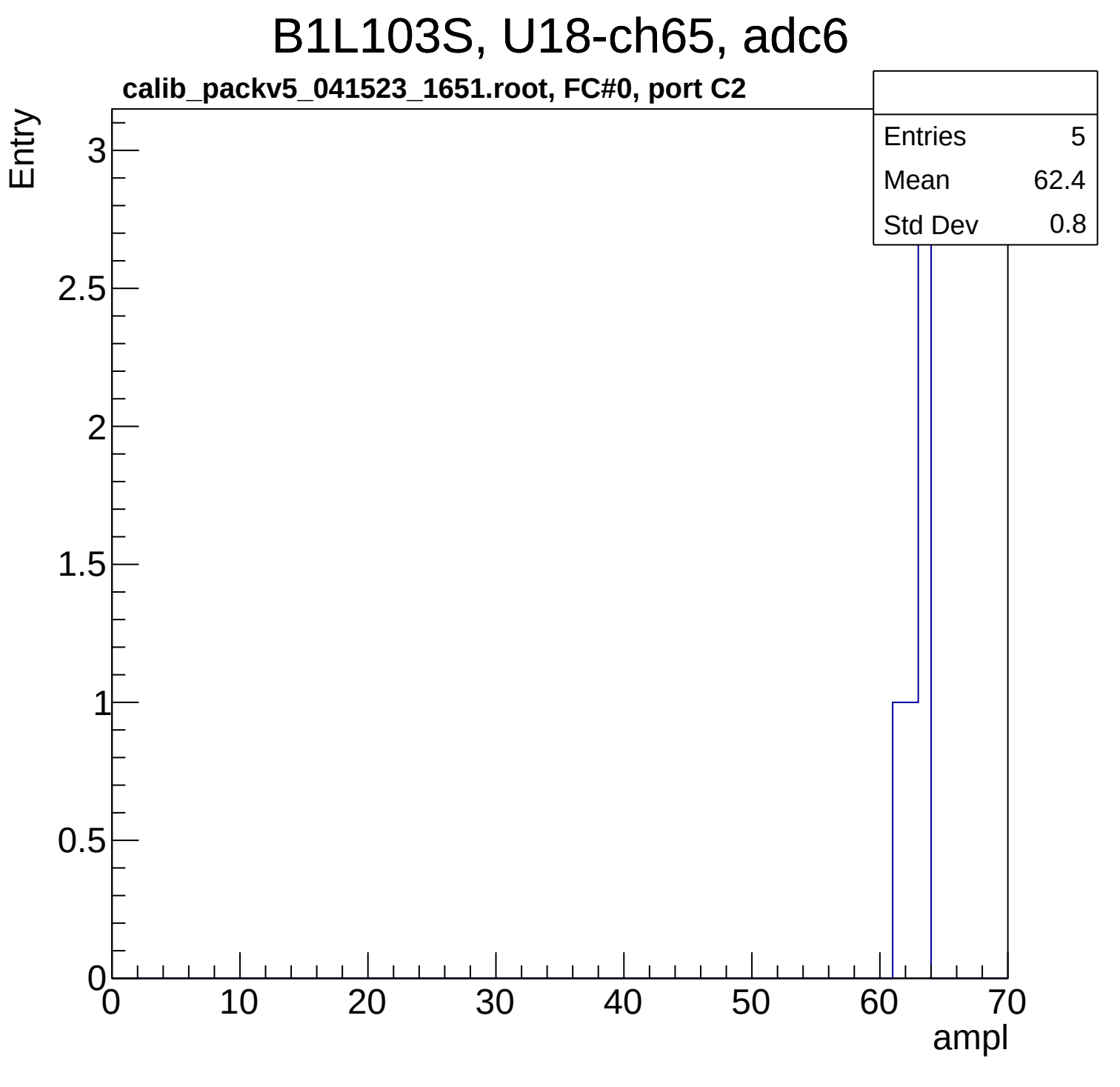
B1L103S, U18-ch65, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 5
Mean 62.4
Std Dev 0.8
Entry
ampl
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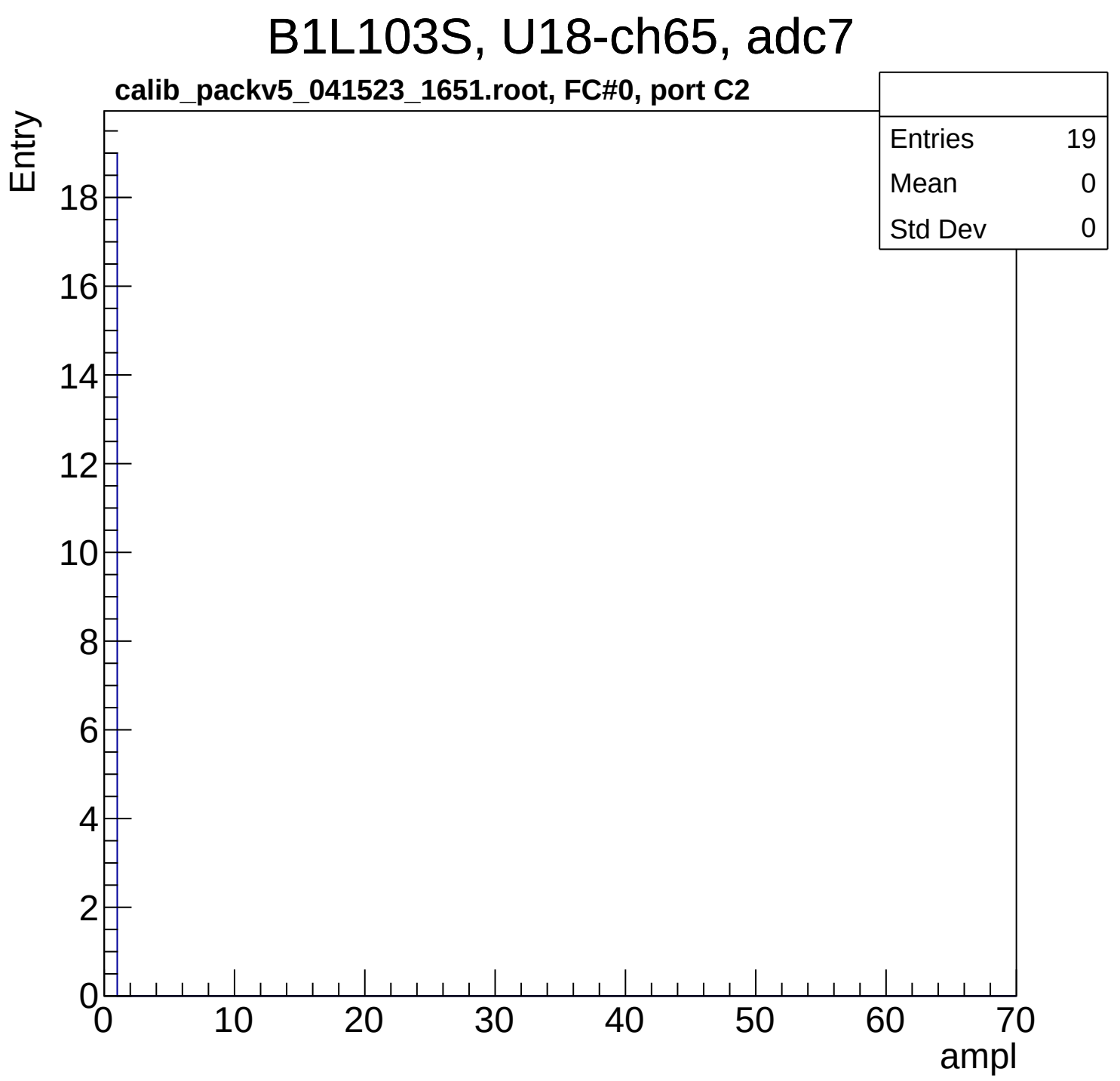
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U18-ch65, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
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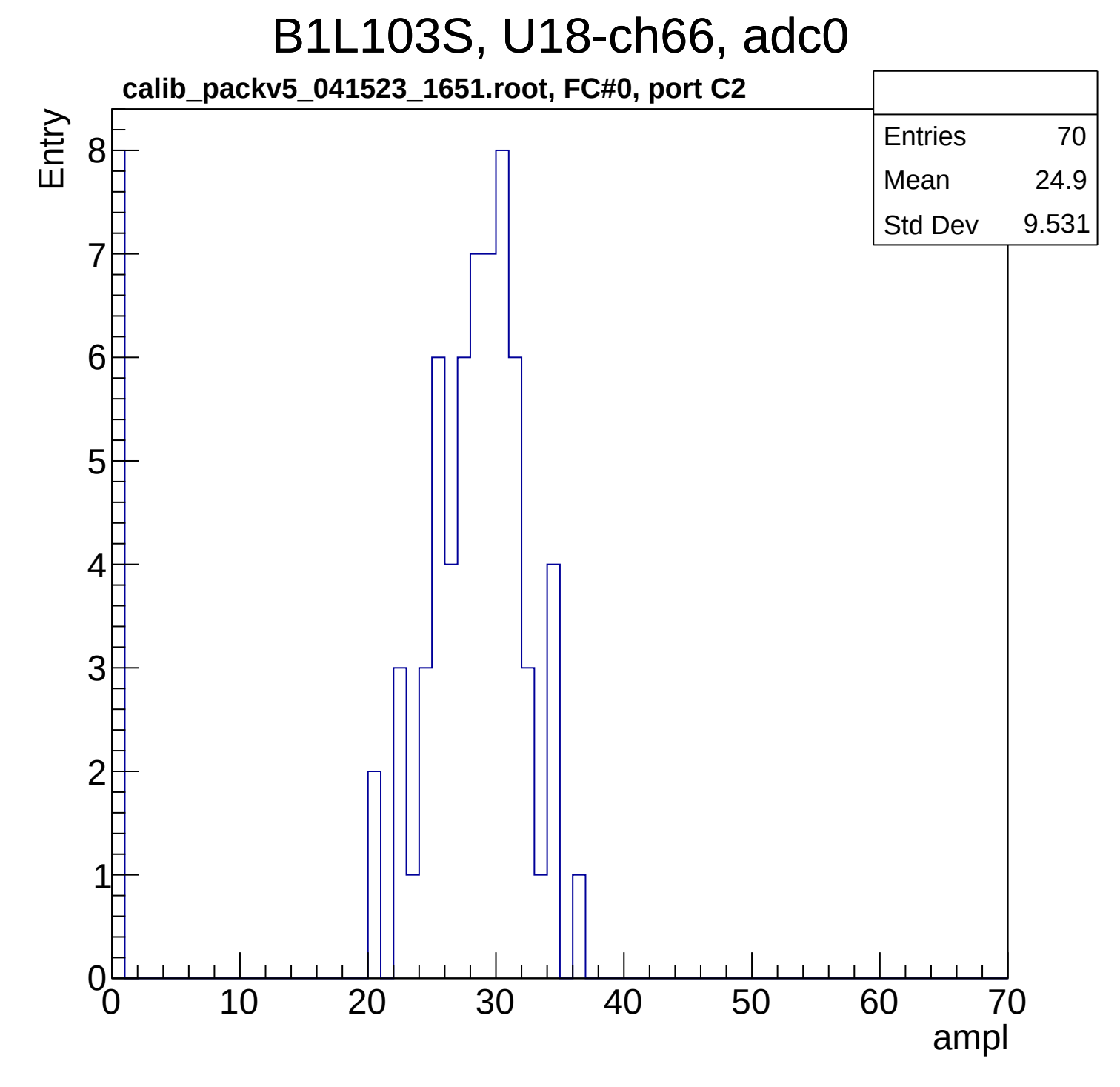
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch66, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 24.9
Std Dev 9.531
Entry
ampl
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4
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0
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20
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40
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60
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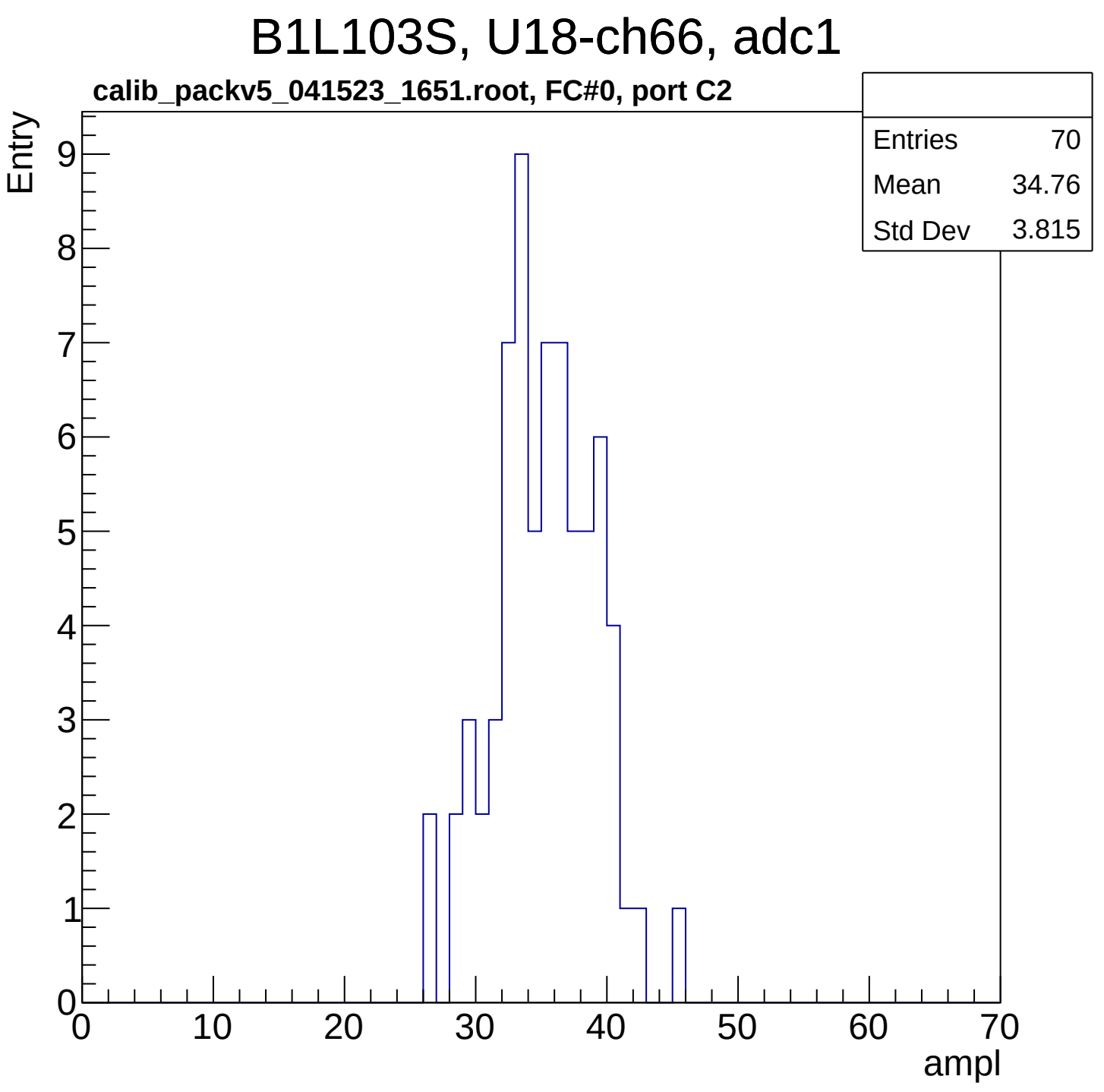
B1L103S, U18-ch66, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 34.76
Std Dev 3.815
Entry
ampl
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4
5
6
7
8
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0
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20
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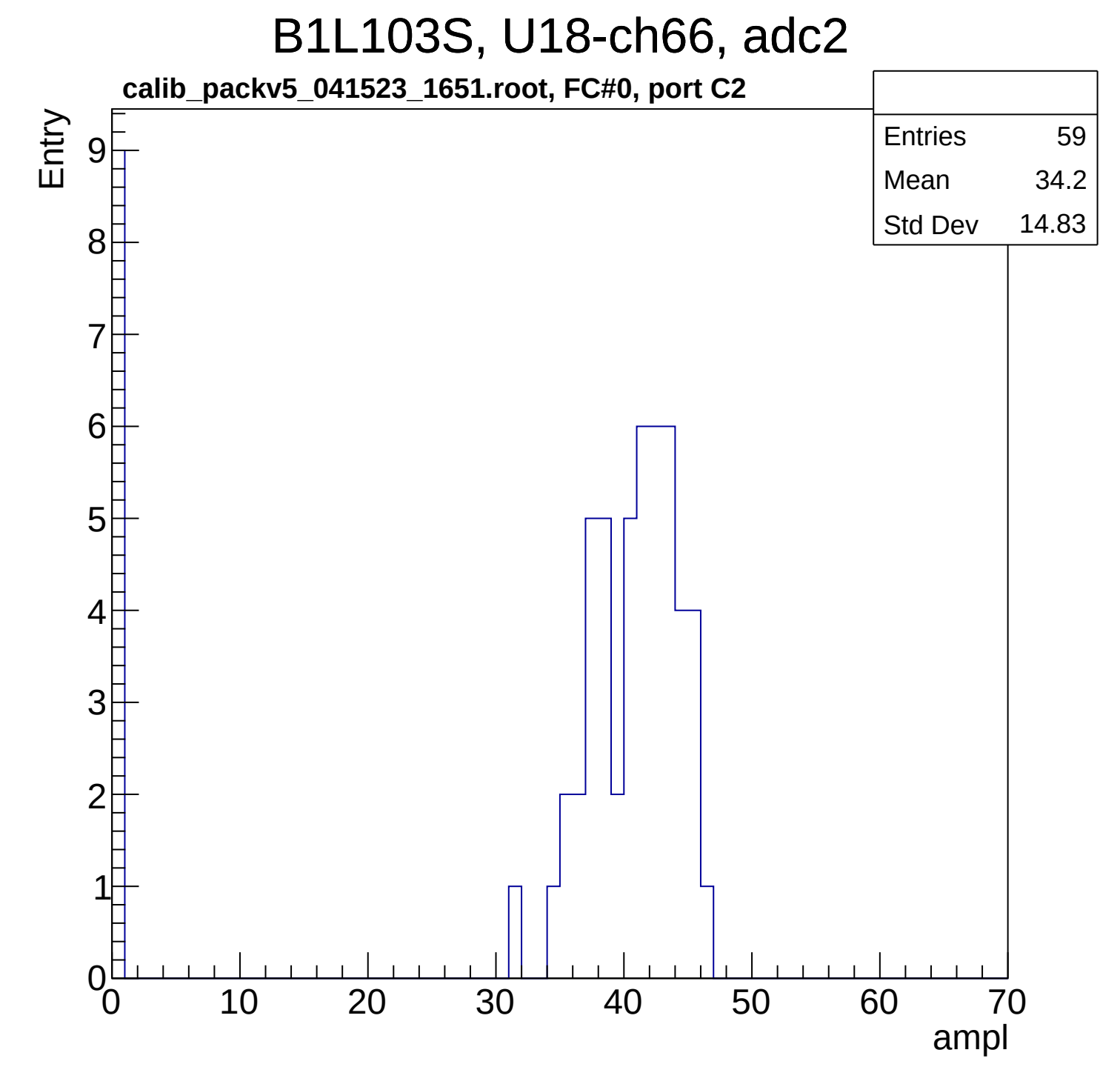
B1L103S, U18-ch66, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 34.2
Std Dev 14.83
Entry
ampl
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3
4
5
6
7
8
9
0
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50
60
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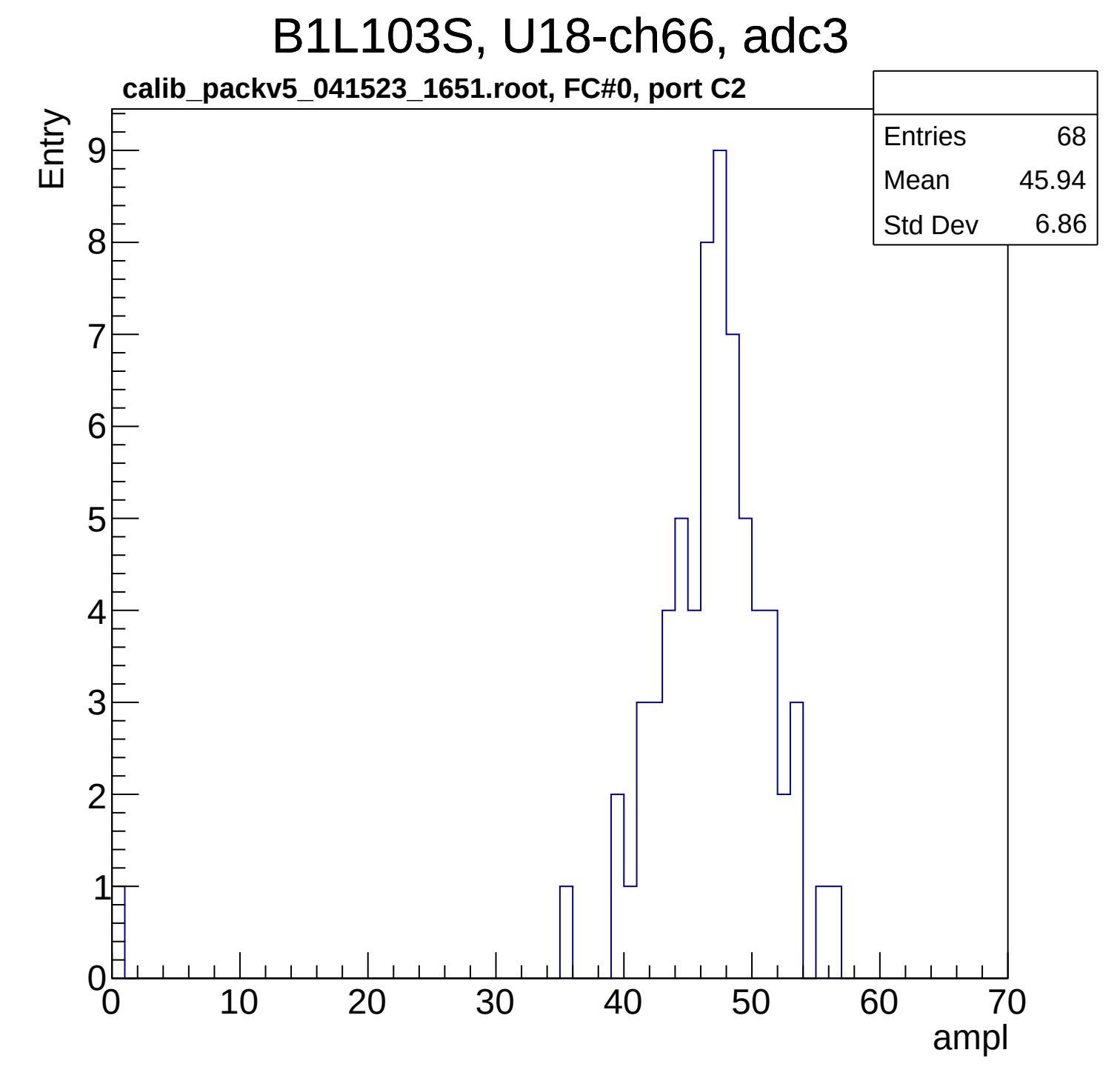
B1L103S, U18-ch66, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 45.94
Std Dev 6.86
Entry
ampl
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2
3
4
5
6
7
8
9
0
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60
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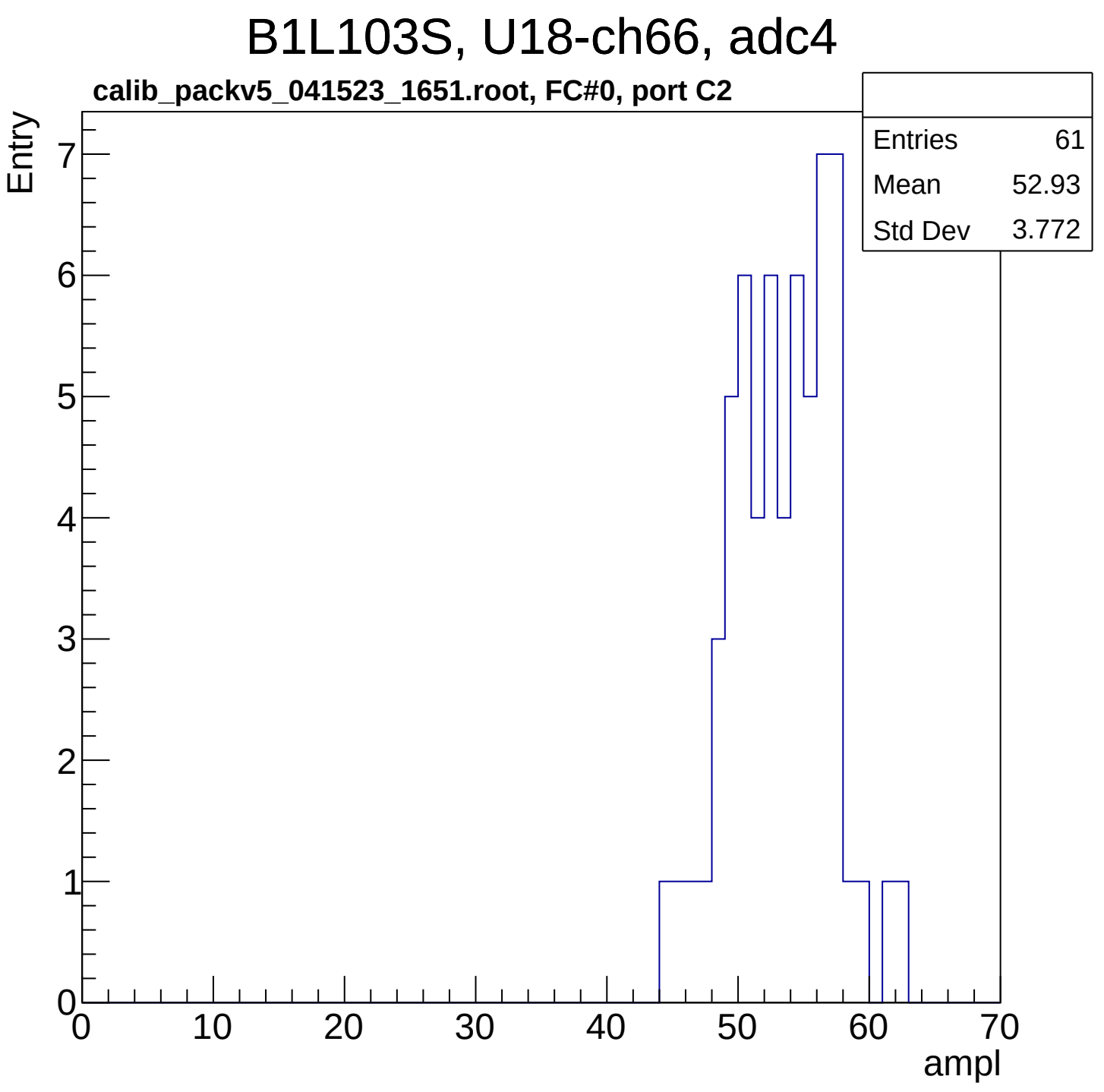
B1L103S, U18-ch66, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 52.93
Std Dev 3.772
Entry
ampl
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4
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6
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0
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20
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40
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60
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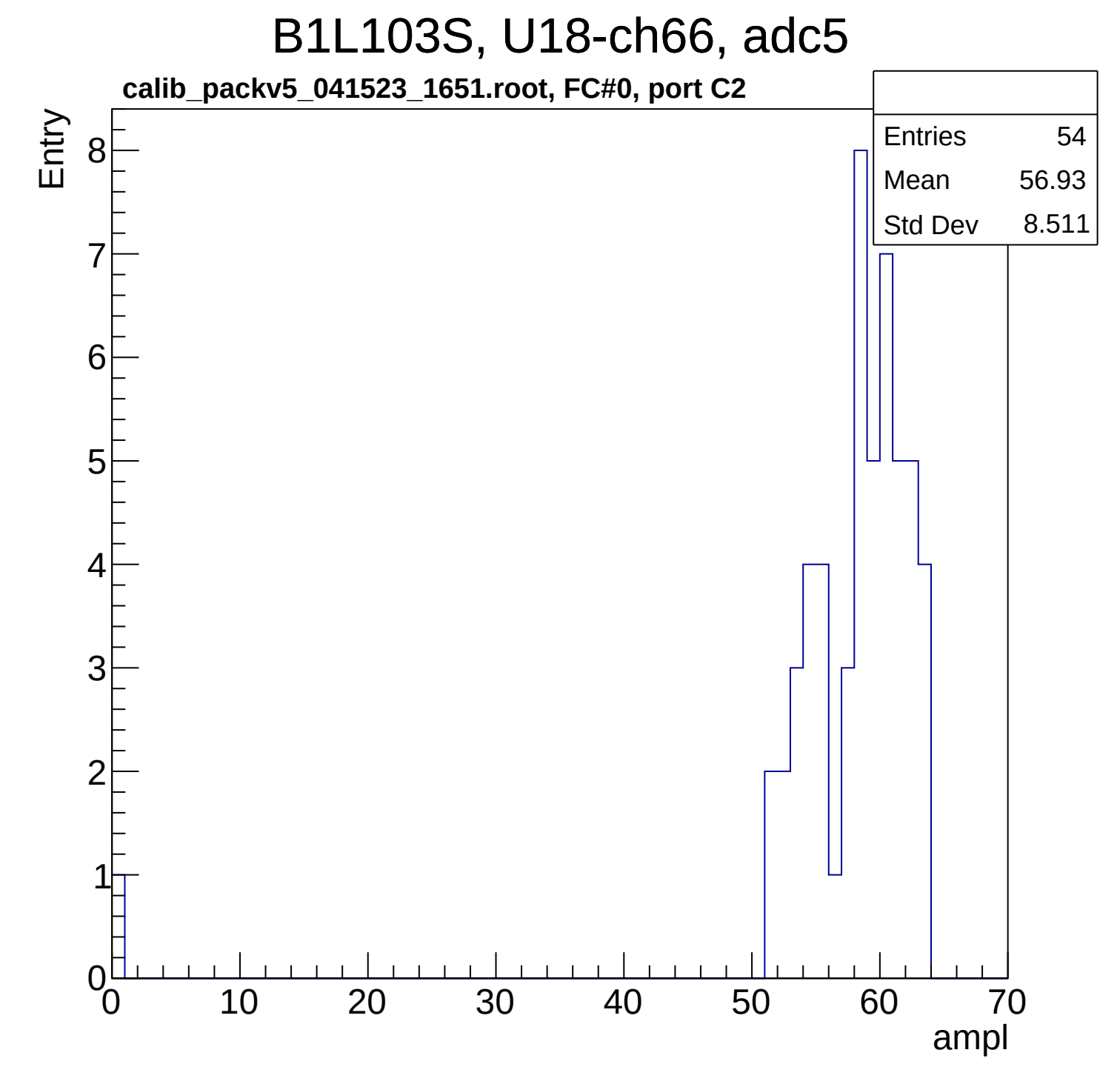
B1L103S, U18-ch66, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 56.93
Std Dev 8.511
Entry
ampl
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2
3
4
5
6
7
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0
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50
60
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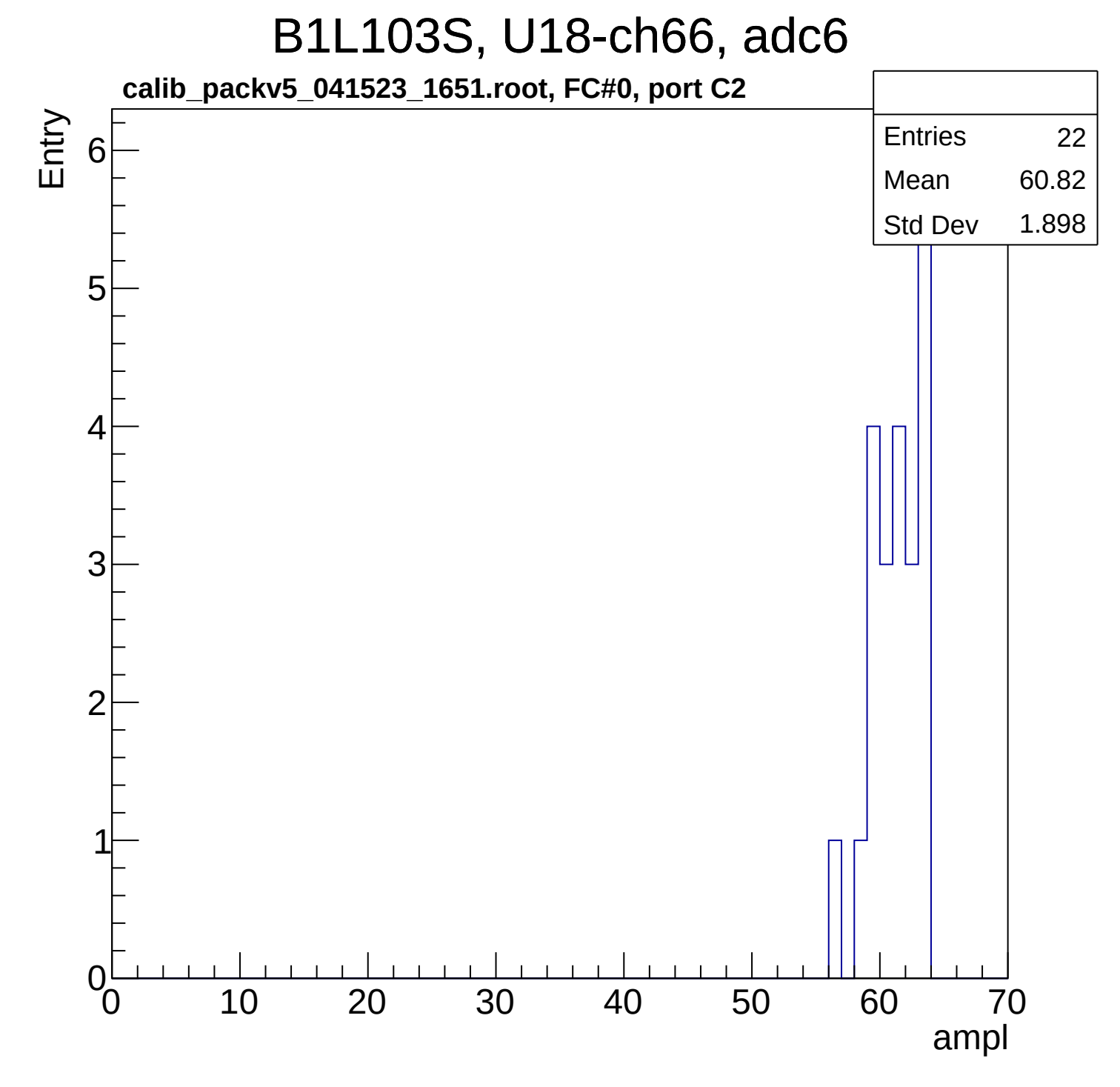
B1L103S, U18-ch66, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 60.82
Std Dev 1.898
Entry
ampl
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3
4
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0
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20
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40
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60
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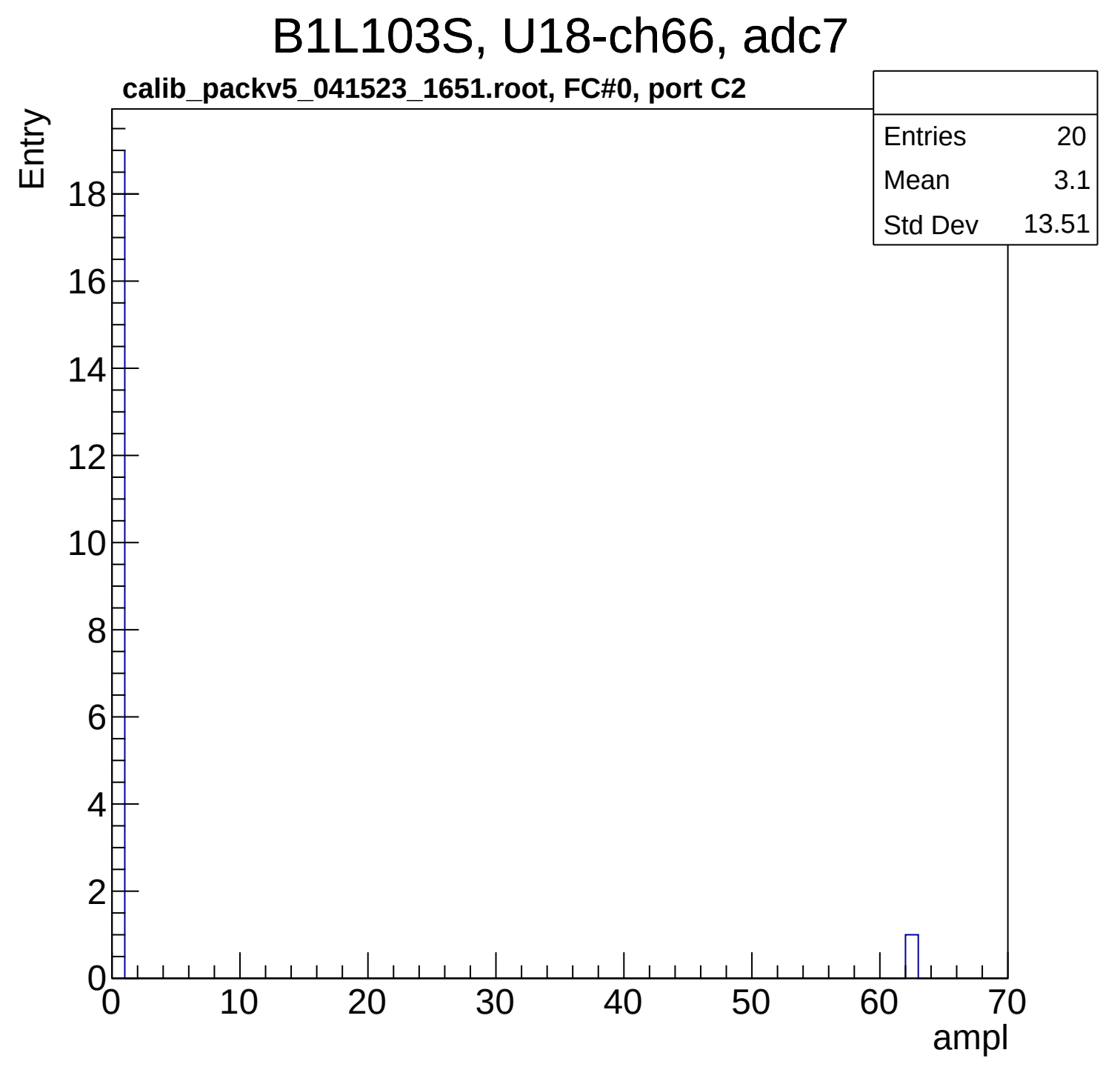
B1L103S, U18-ch66, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.1
Std Dev 13.51
Entry
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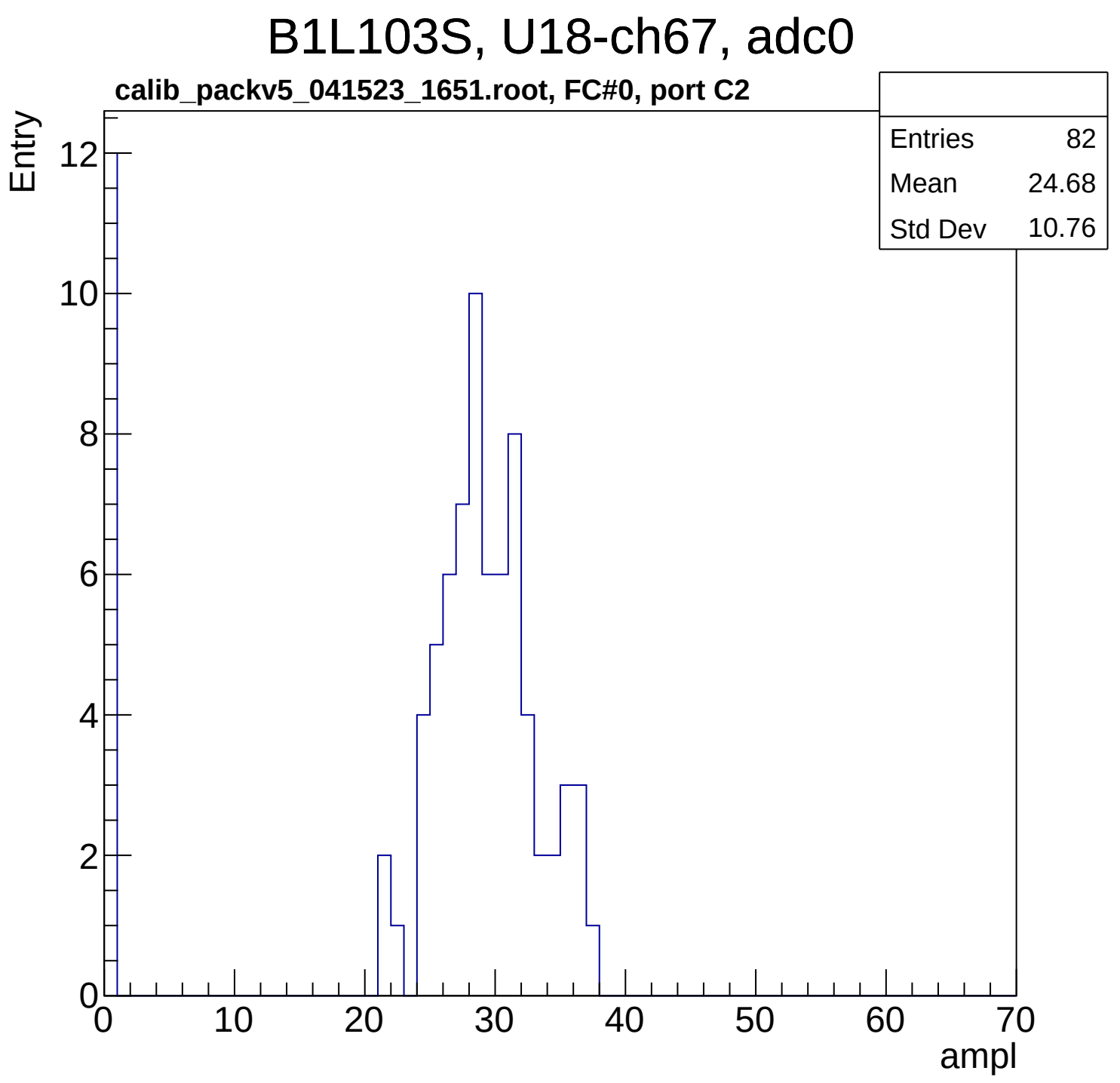
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch67, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 24.68
Std Dev 10.76
Entry
ampl
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6
8
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0
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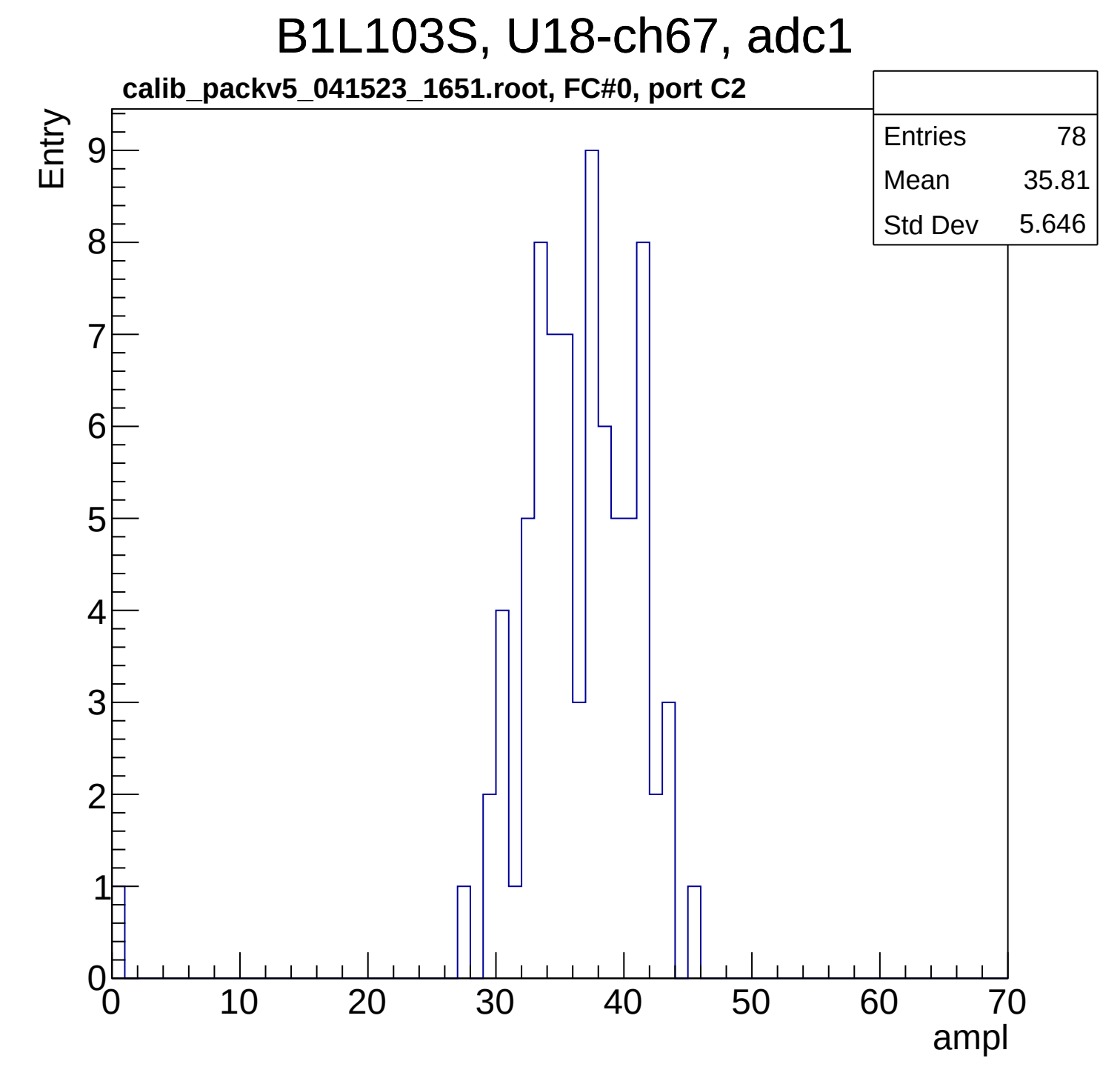
B1L103S, U18-ch67, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 35.81
Std Dev 5.646
Entry
ampl
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3
4
5
6
7
8
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0
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60
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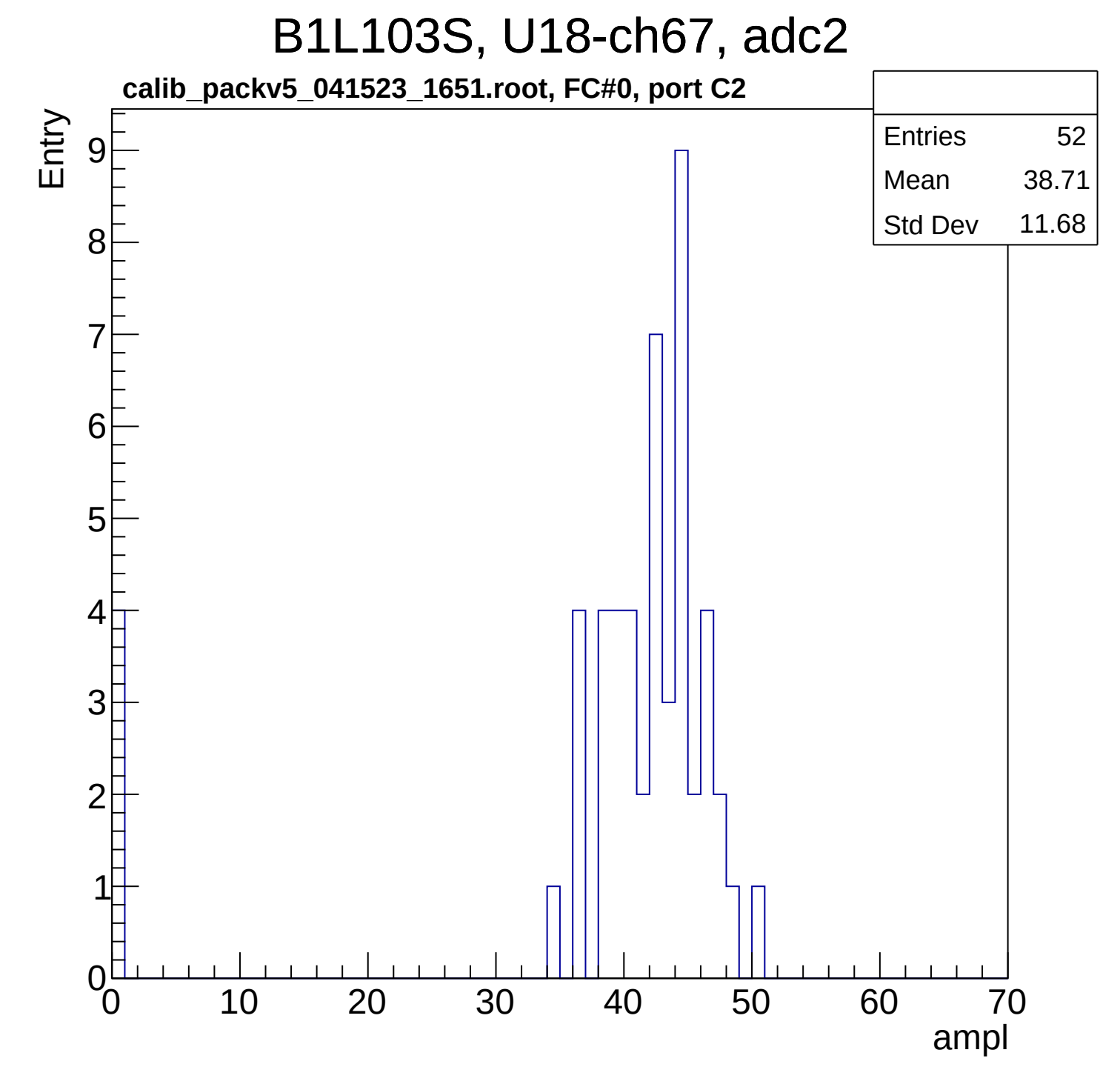
B1L103S, U18-ch67, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 38.71
Std Dev 11.68
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
50
60
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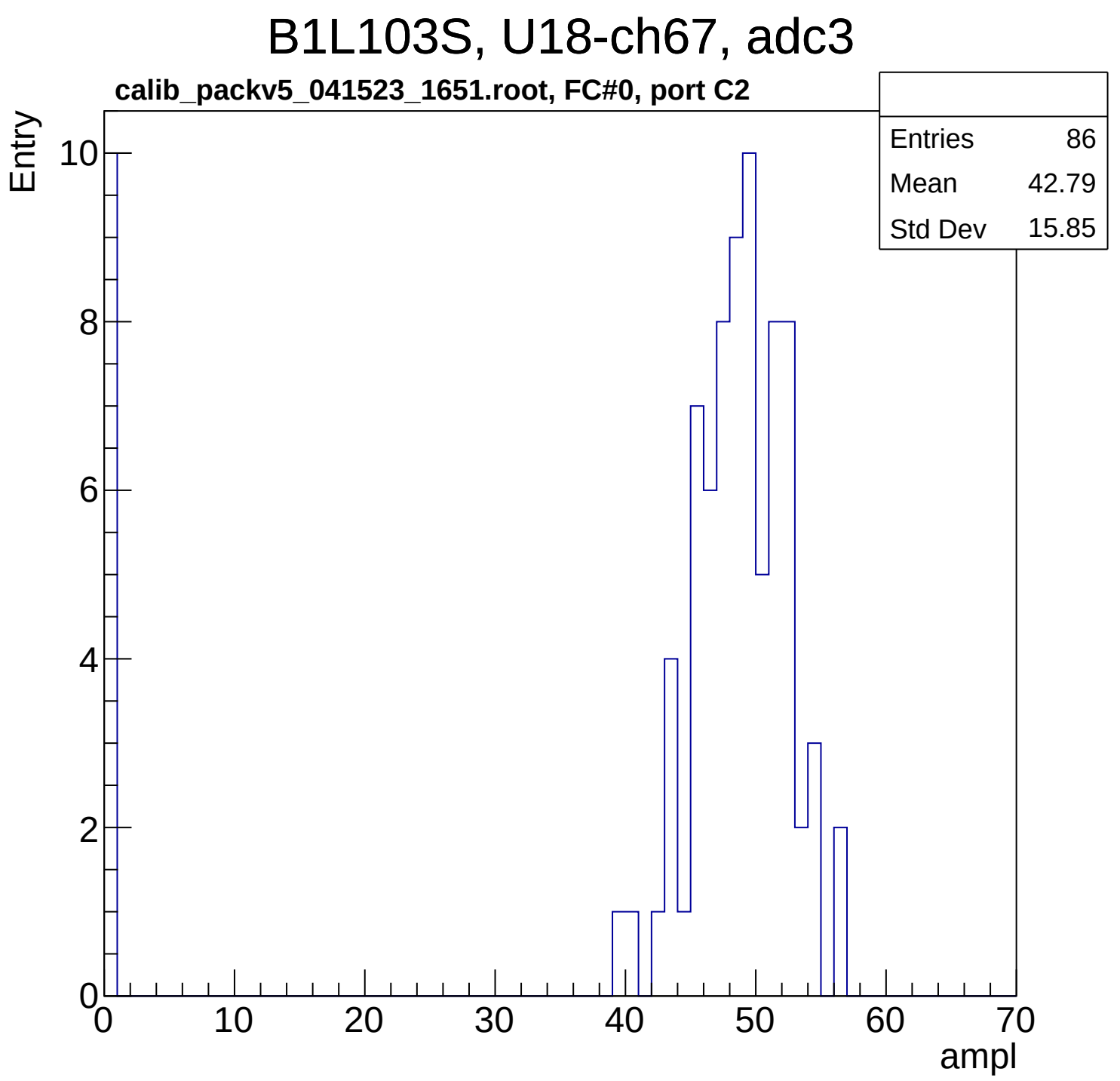
B1L103S, U18-ch67, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 42.79
Std Dev 15.85
Entry
ampl
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40
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60
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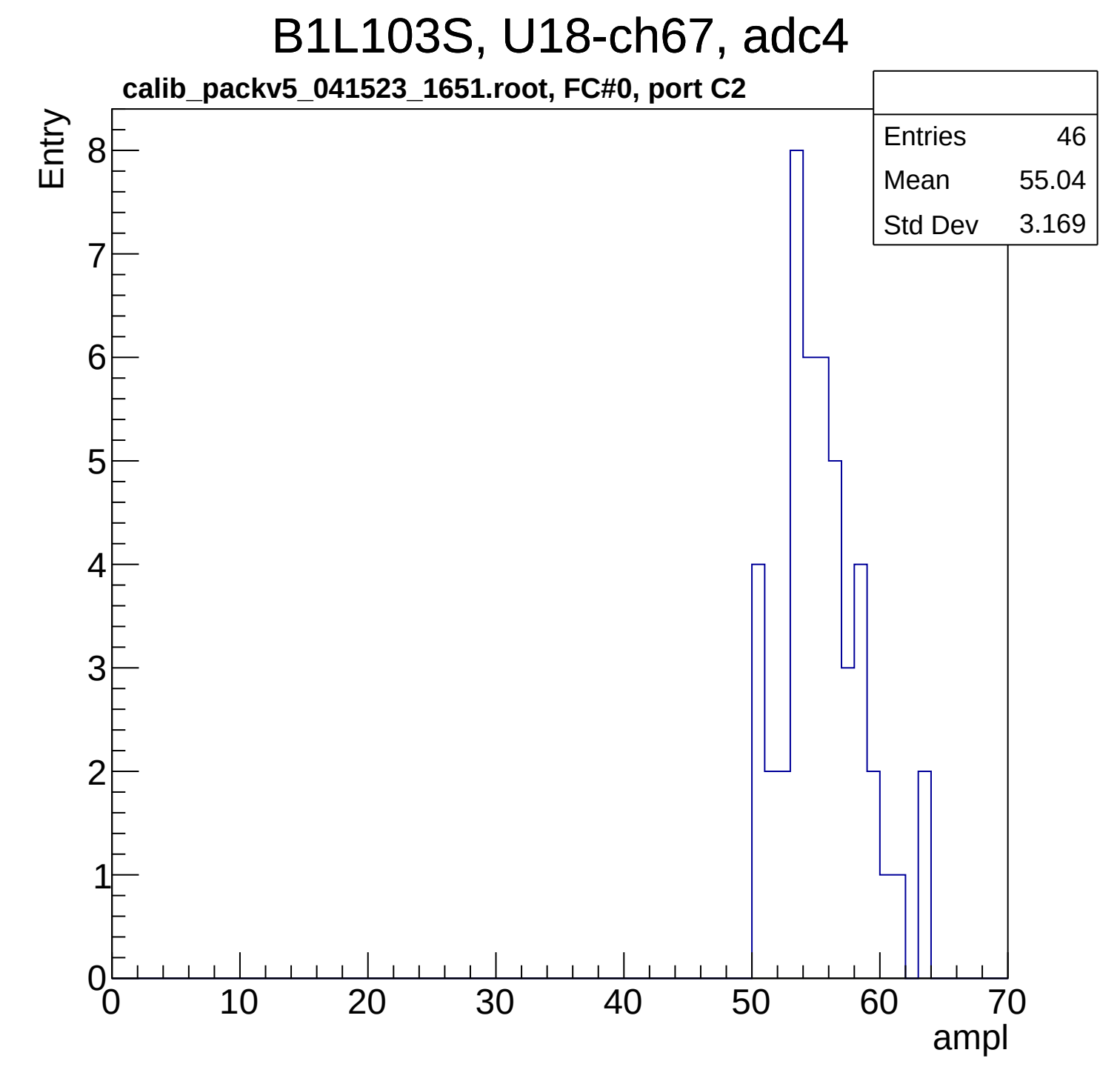
B1L103S, U18-ch67, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 55.04
Std Dev 3.169
Entry
ampl
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5
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7
8
0
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40
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60
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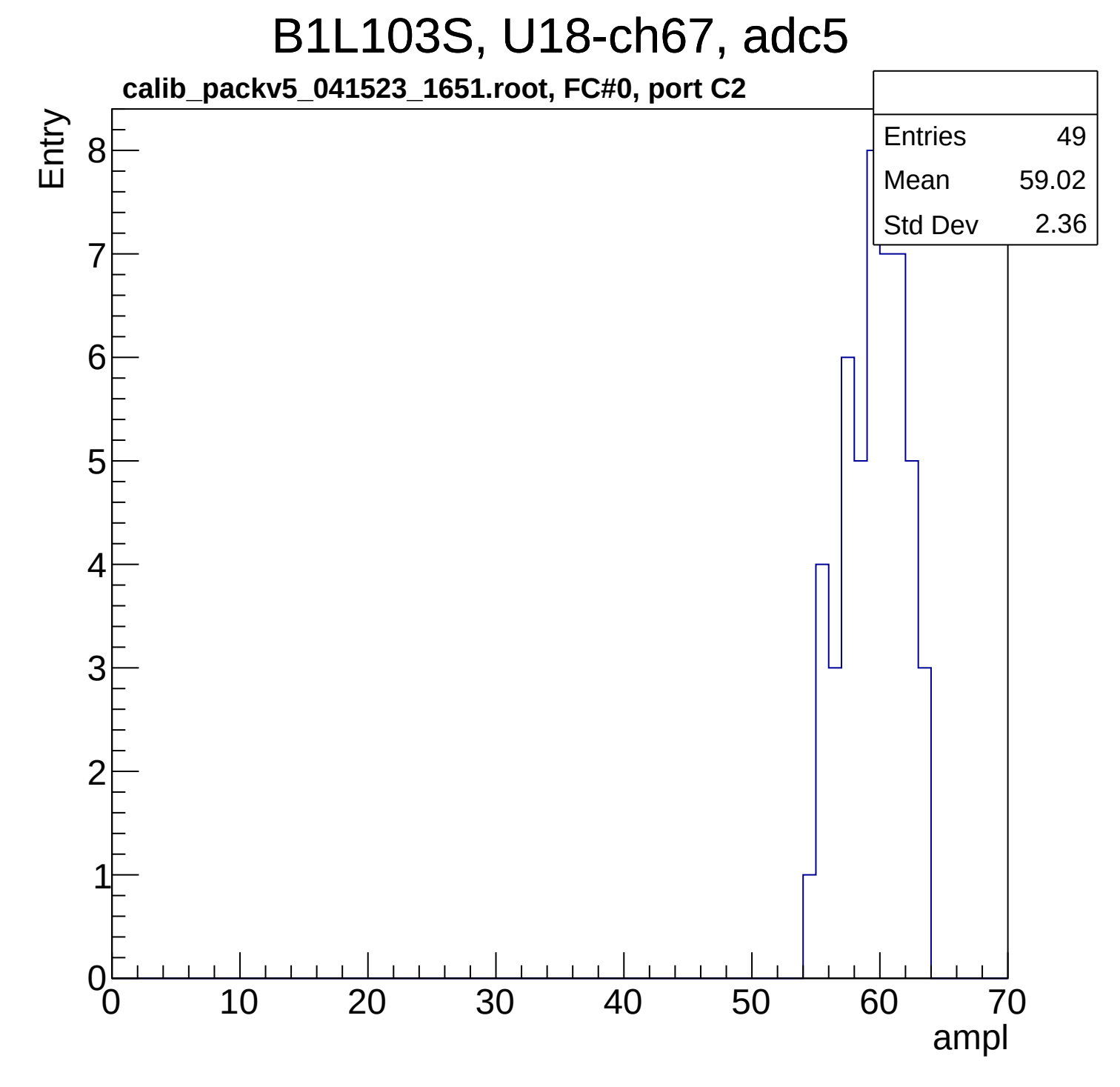
B1L103S, U18-ch67, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 59.02
Std Dev 2.36
Entry
ampl
0
1
2
3
4
5
6
7
8
0
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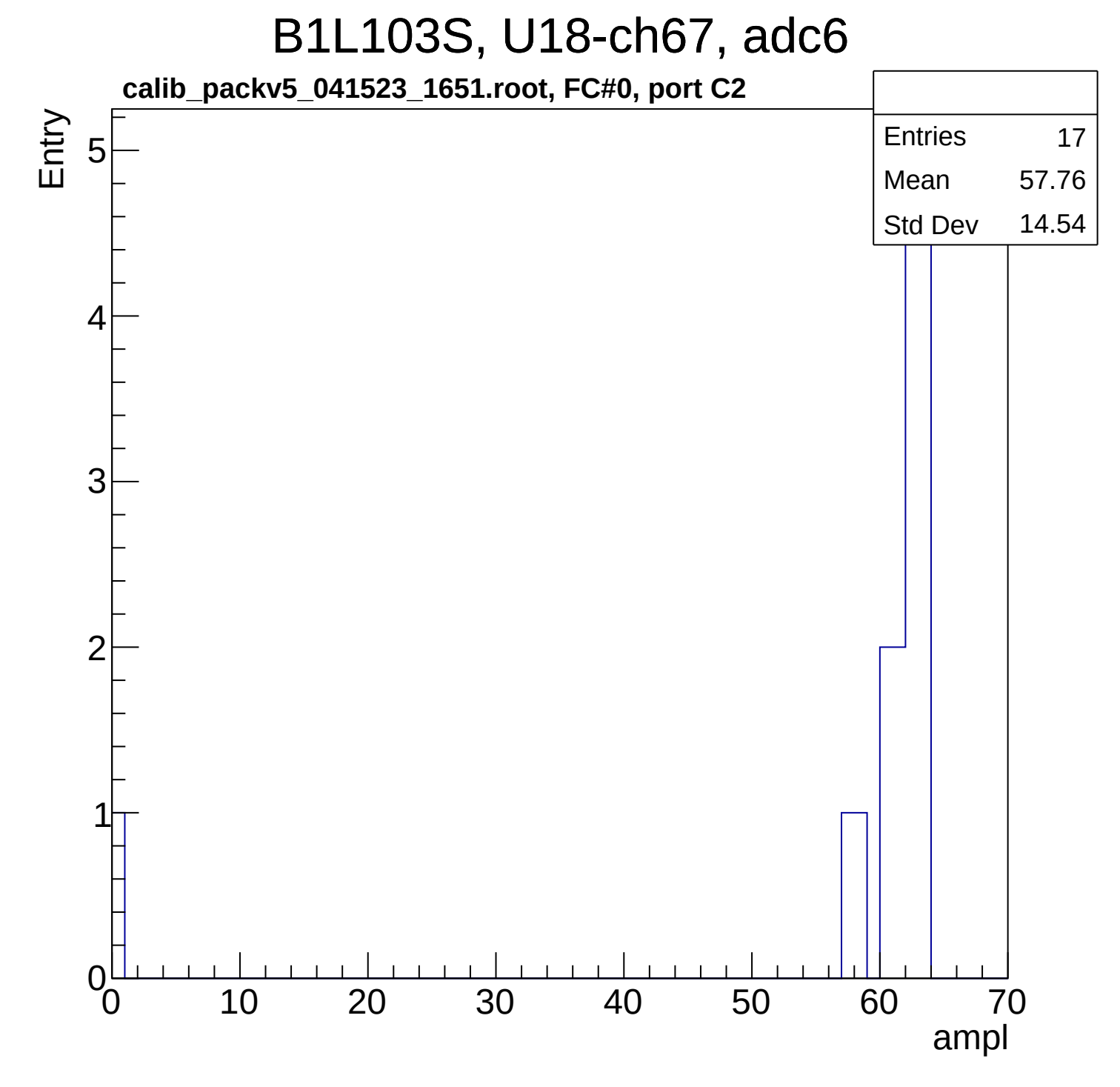
60
70


B1L103S, U18-ch67, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 17
Mean 57.76
Std Dev 14.54
Entry
ampl
0
1
2
3
4
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0
10
20
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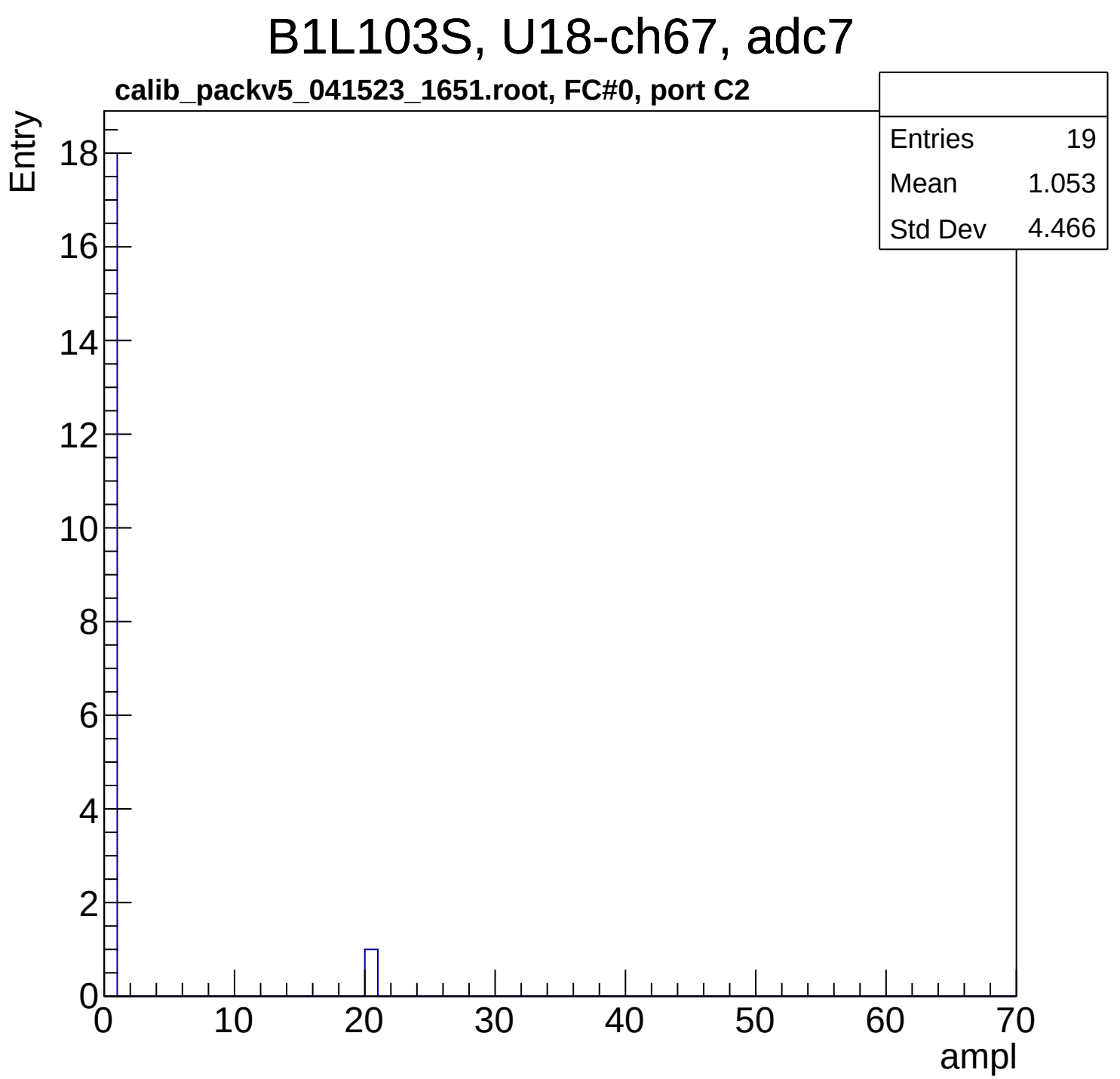
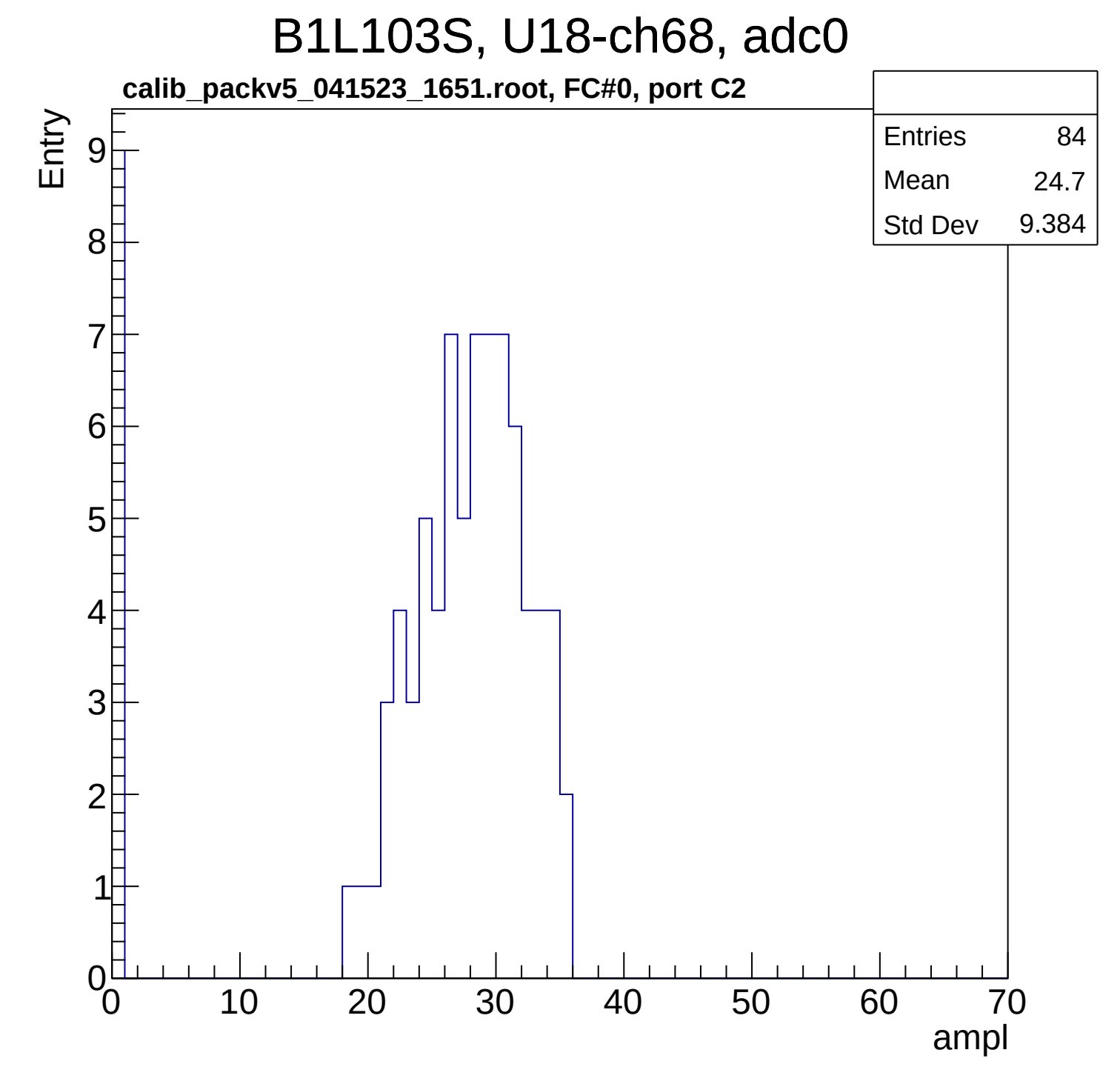
40
50
60
70


B1L103S, U18-ch67, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.053
Std Dev 4.466
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch68, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 24.7
Std Dev 9.384
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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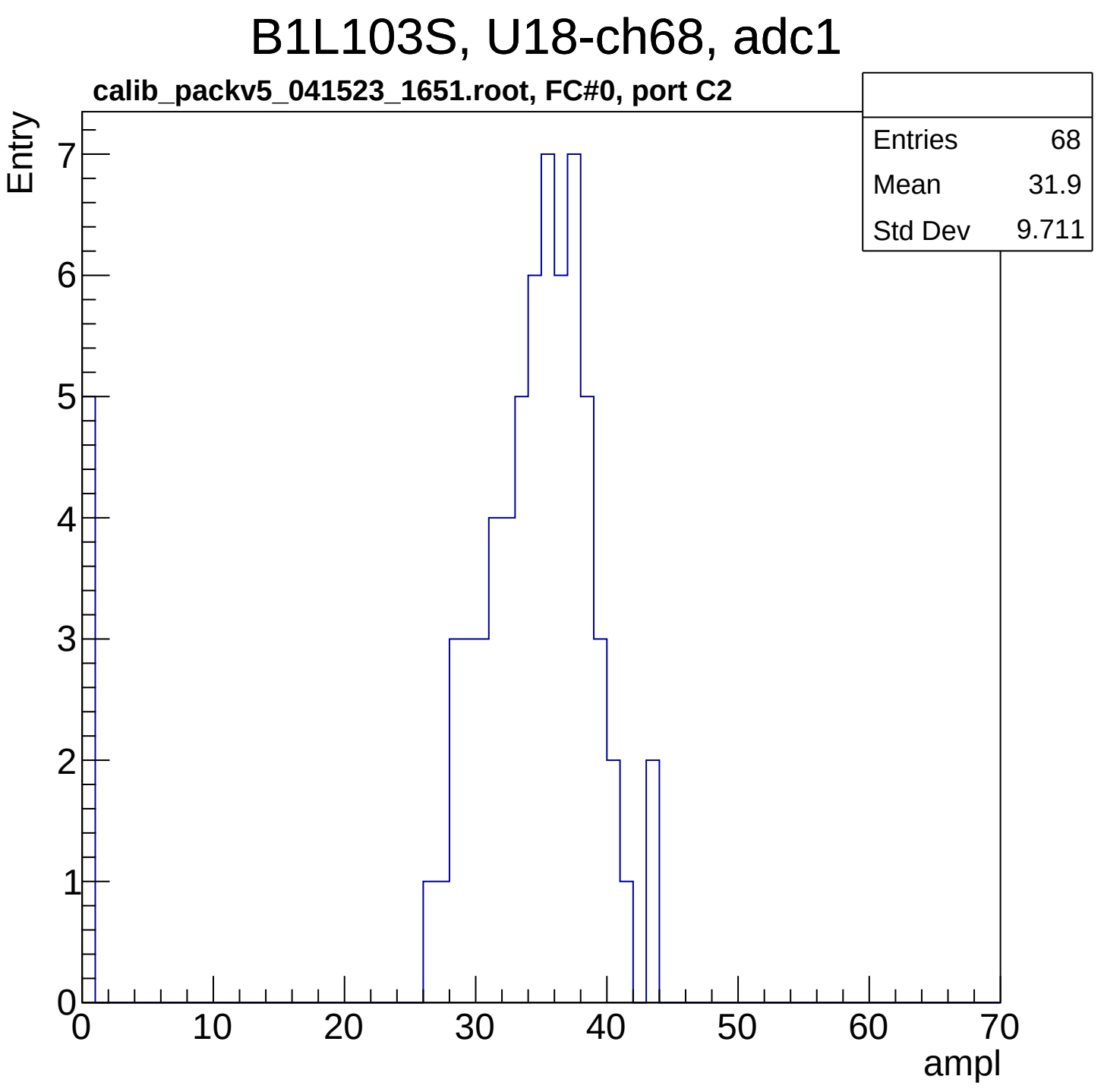
B1L103S, U18-ch68, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 31.9
Std Dev 9.711
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
30
40
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60
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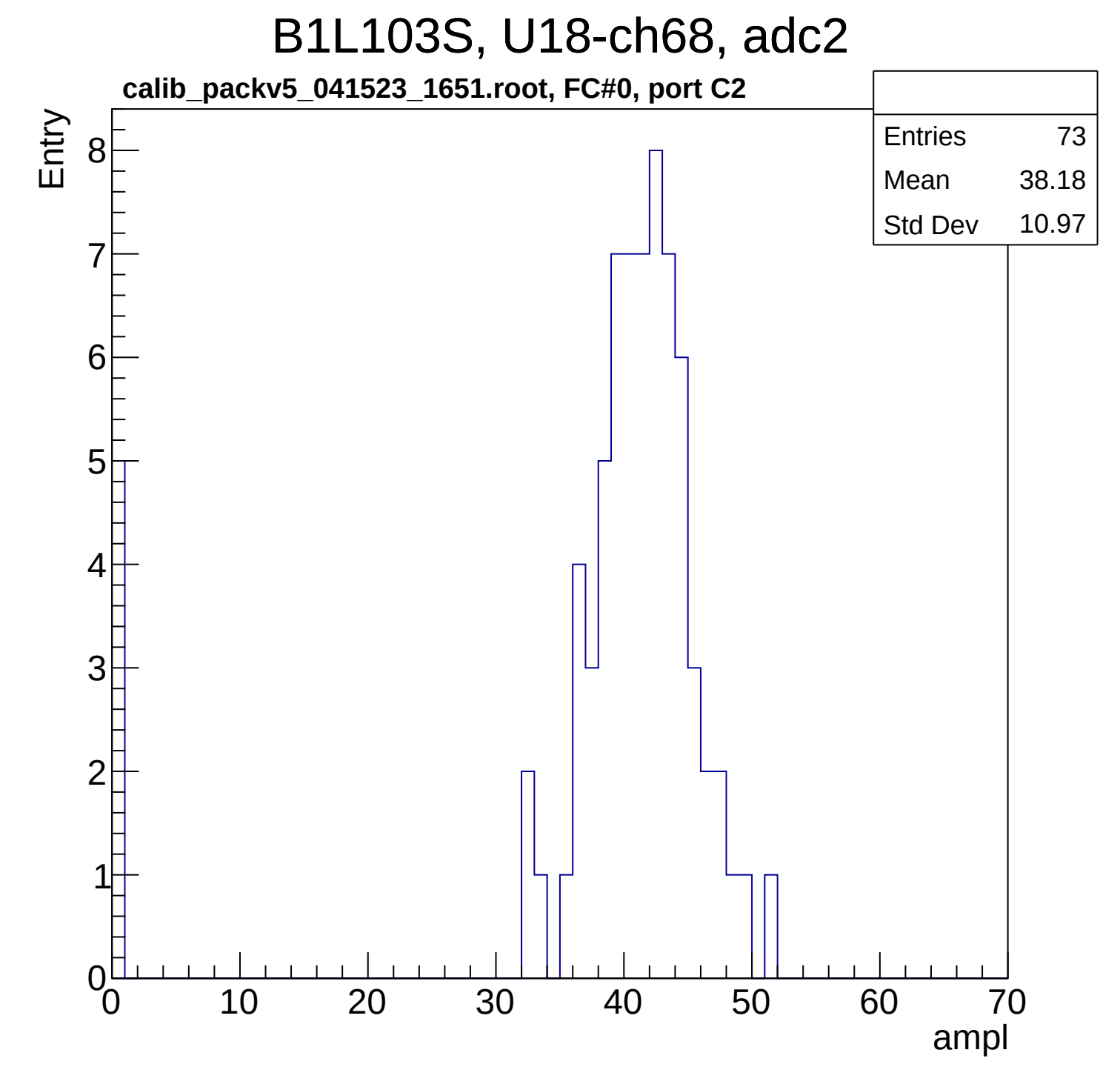
B1L103S, U18-ch68, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 38.18
Std Dev 10.97
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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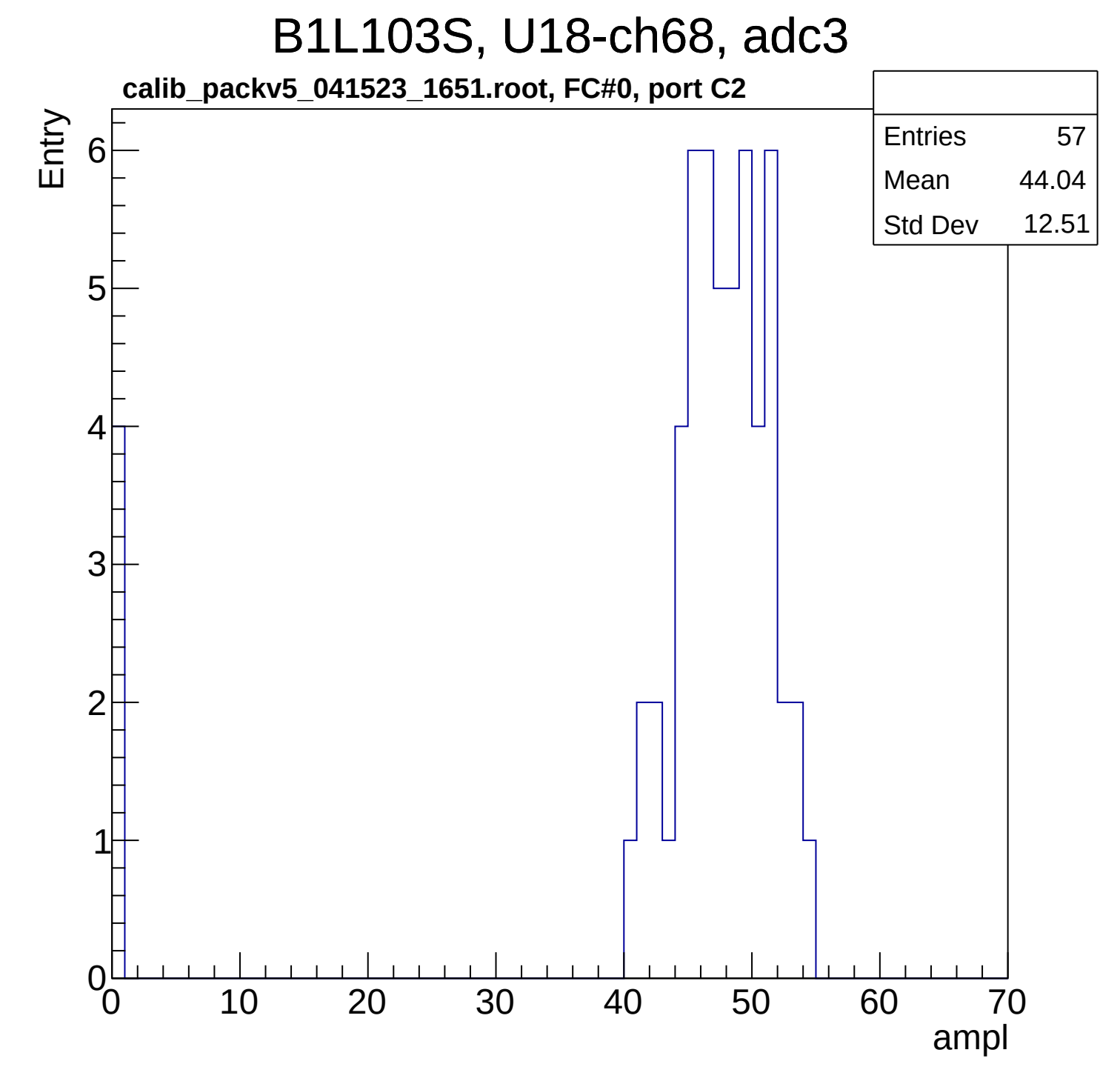
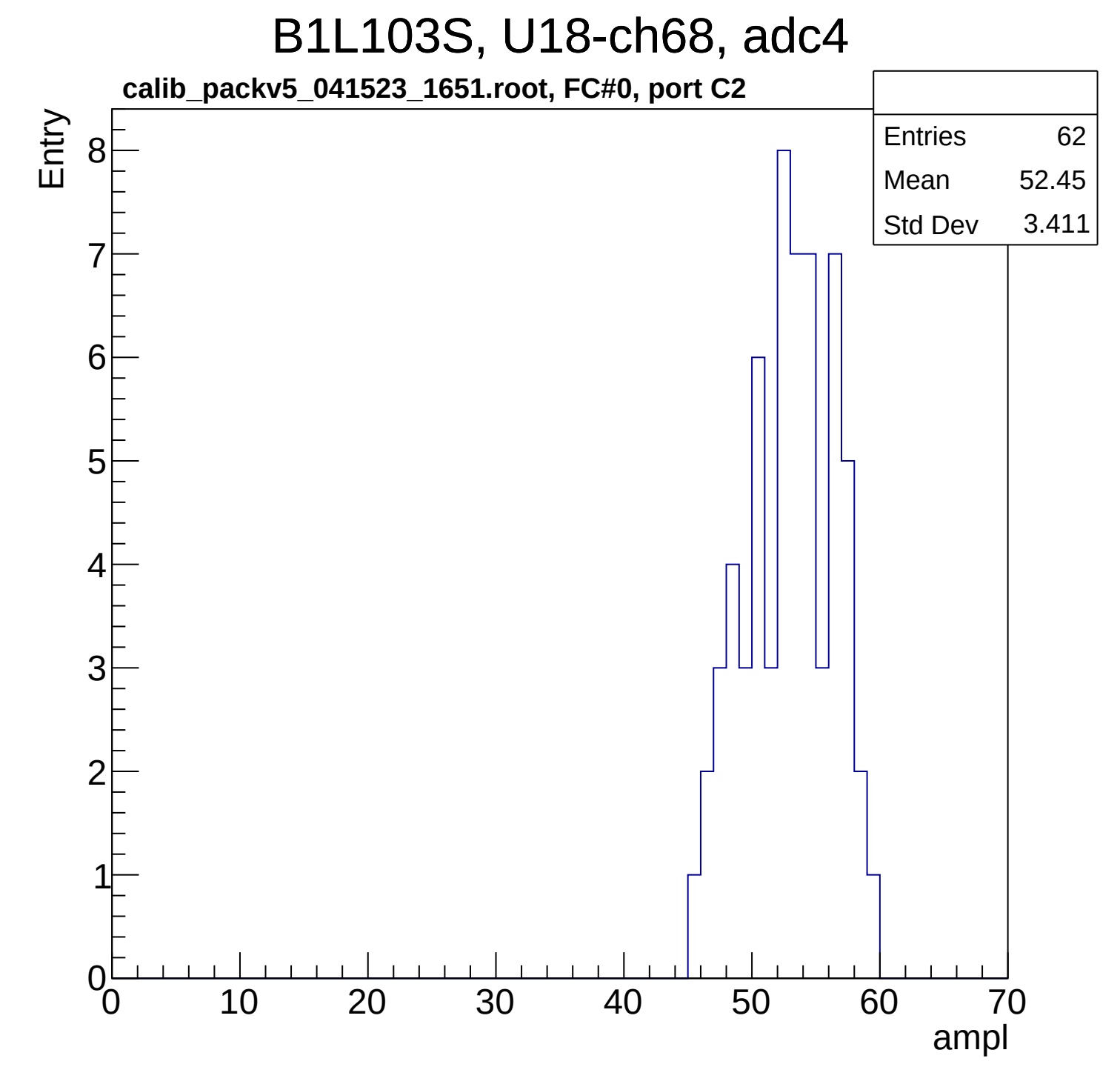

B1L103S, U18-ch68, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 44.04
Std Dev 12.51
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch68, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 52.45
Std Dev 3.411
Entry
ampl
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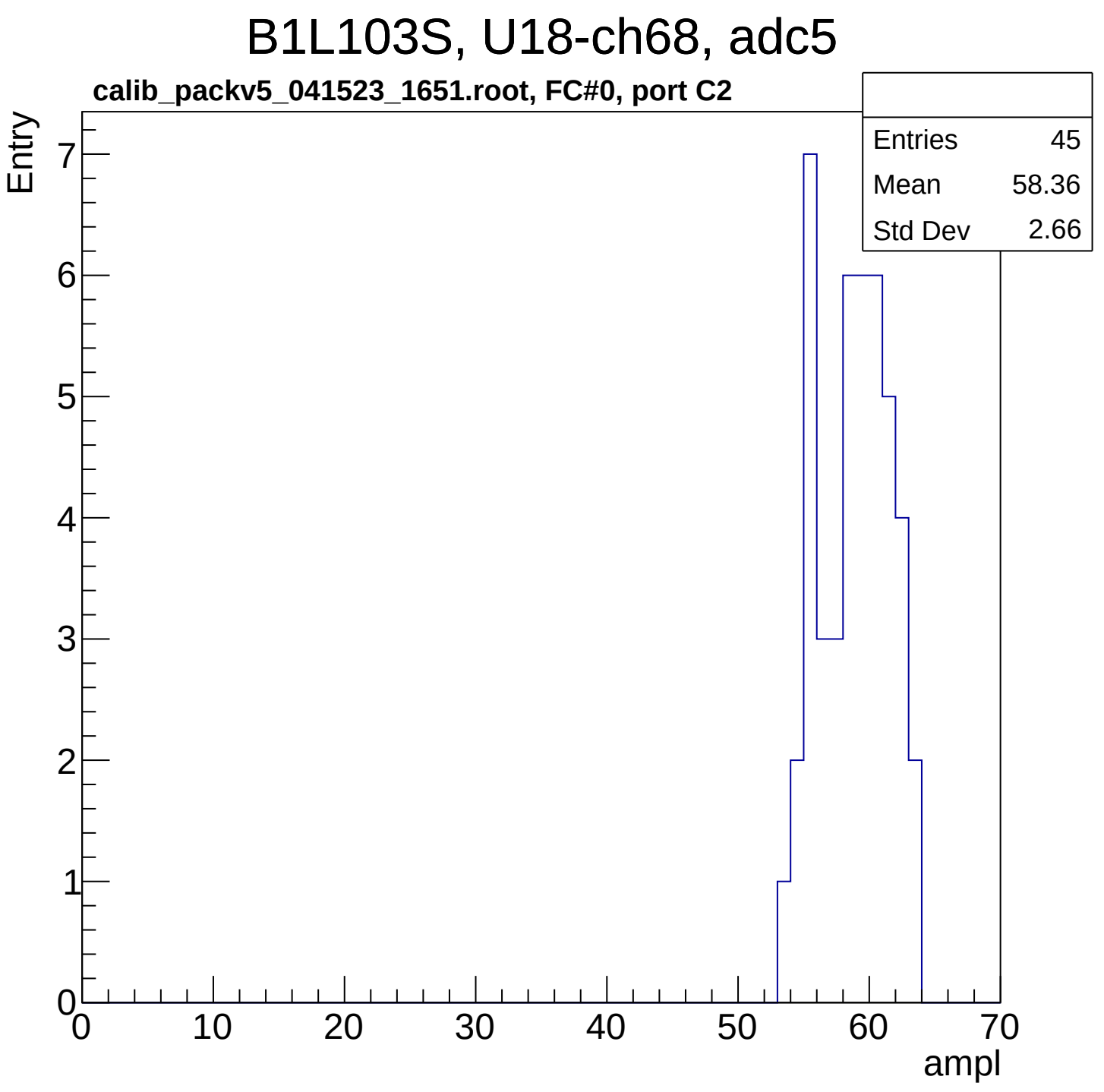
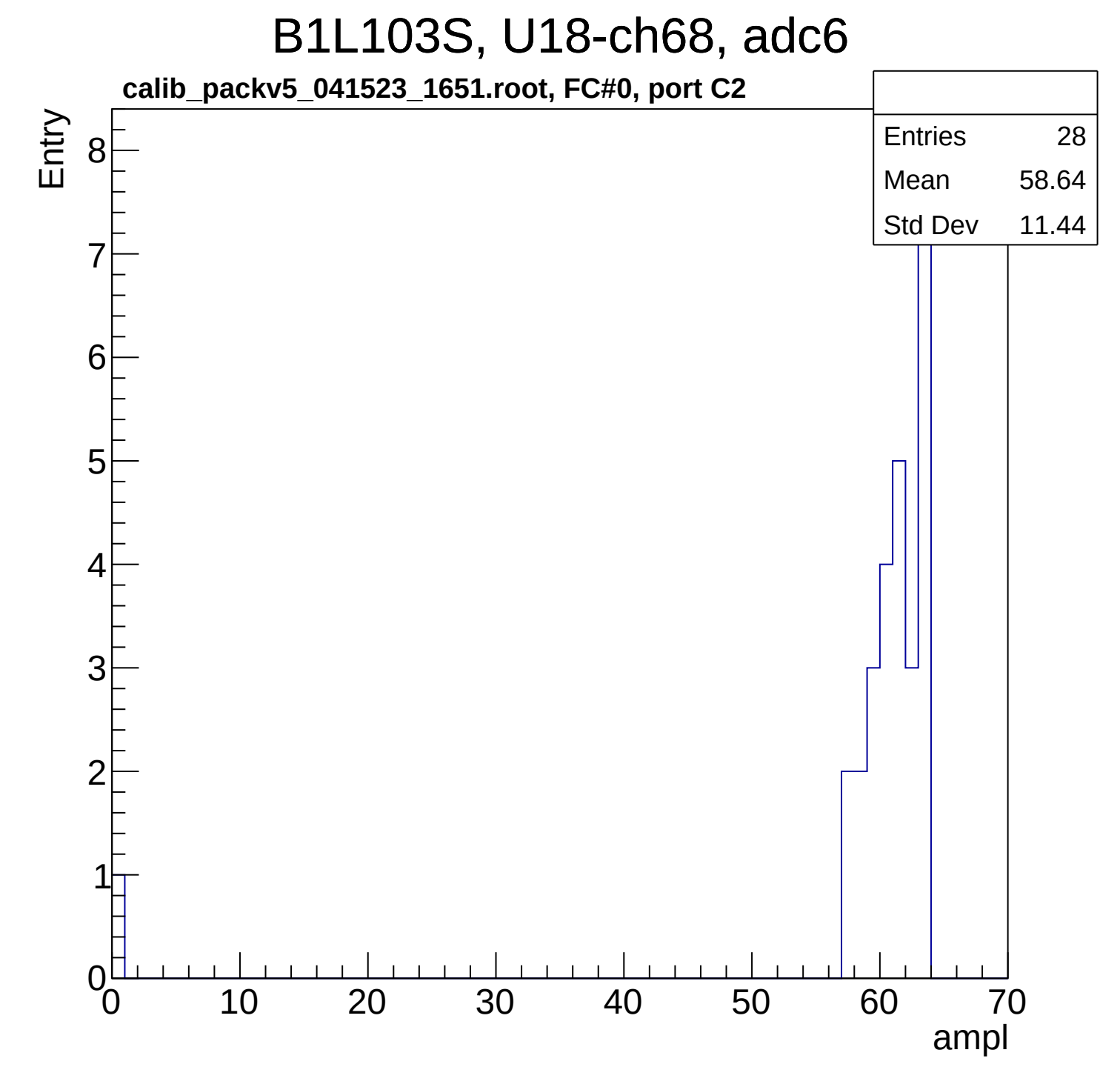
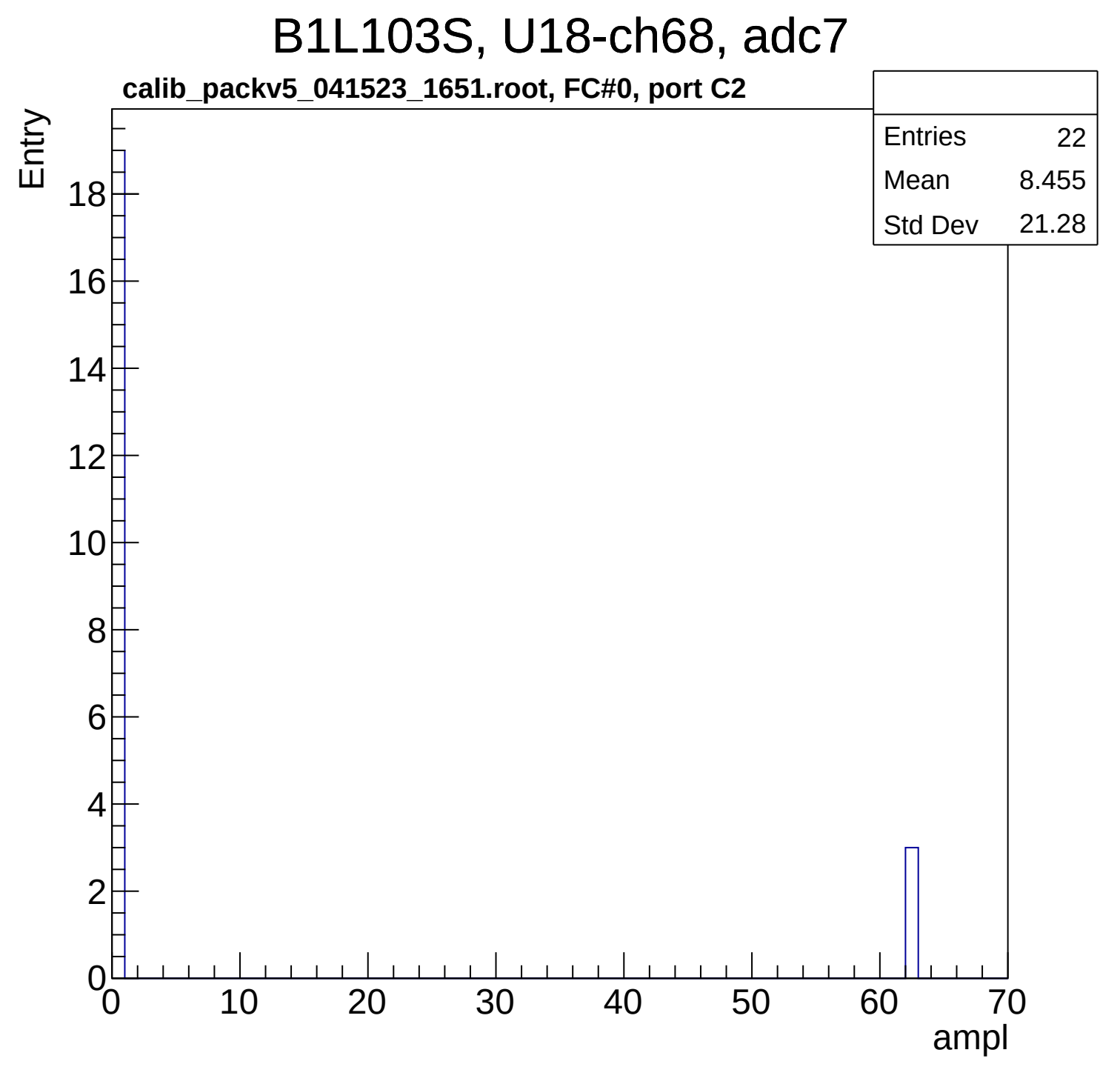
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch68, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 58.36
Std Dev 2.66
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U18-ch68, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 28
Mean 58.64
Std Dev 11.44
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch68, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 8.455
Std Dev 21.28
Entry
ampl
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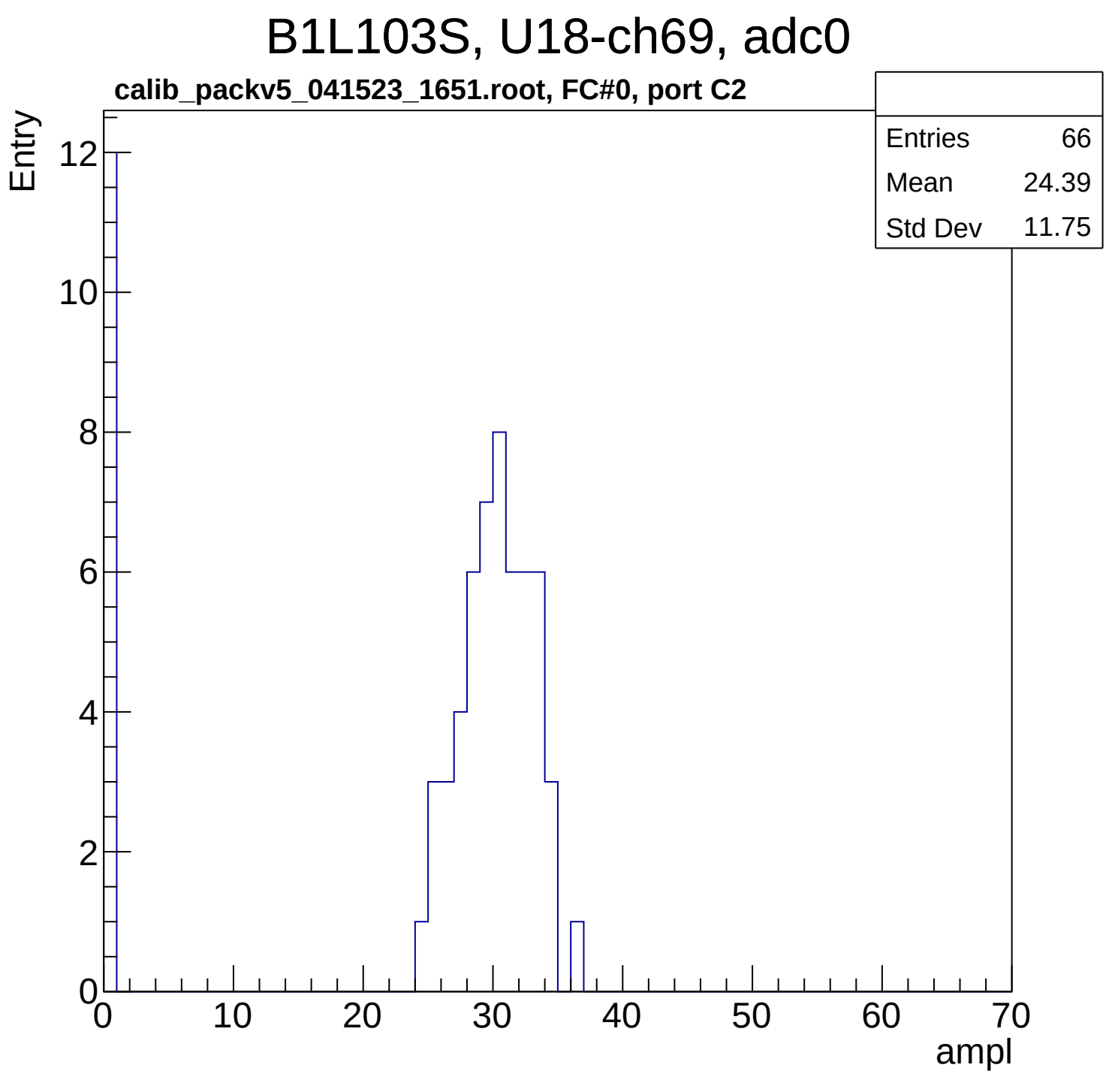
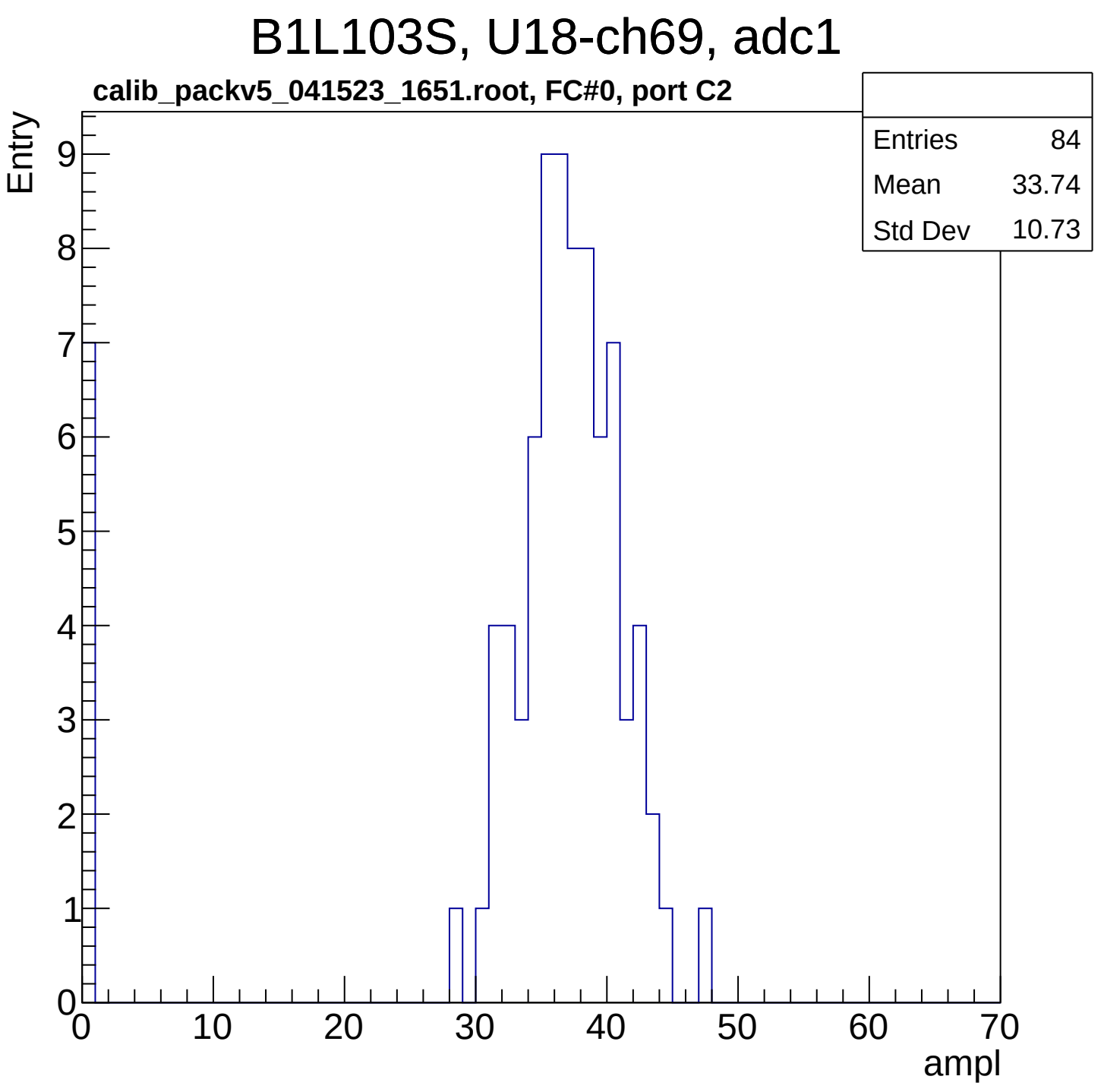
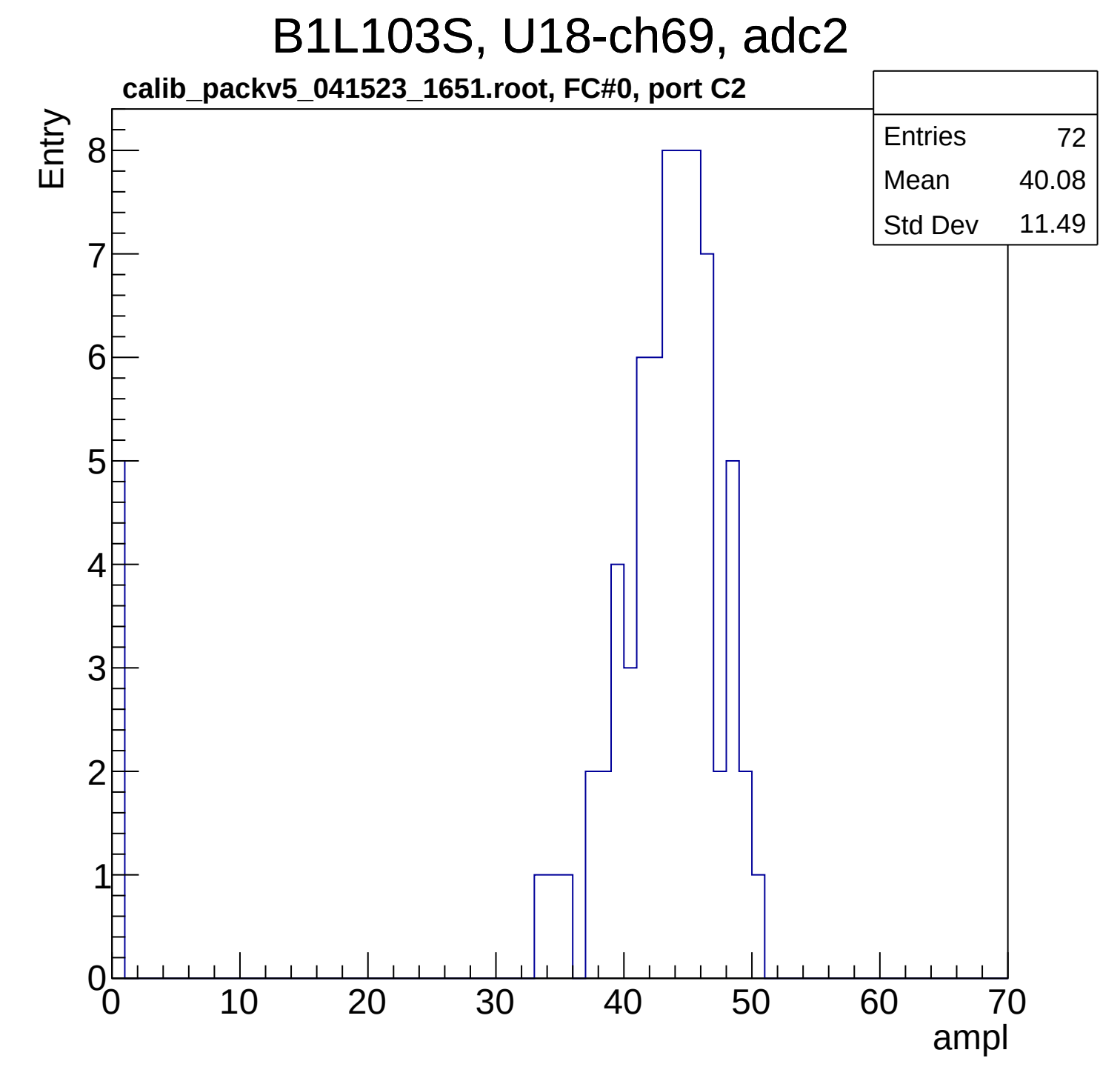
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70


B1L103S, U18-ch69, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 24.39
Std Dev 11.75
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch69, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 33.74
Std Dev 10.73
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U18-ch69, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 40.08
Std Dev 11.49
Entry
ampl
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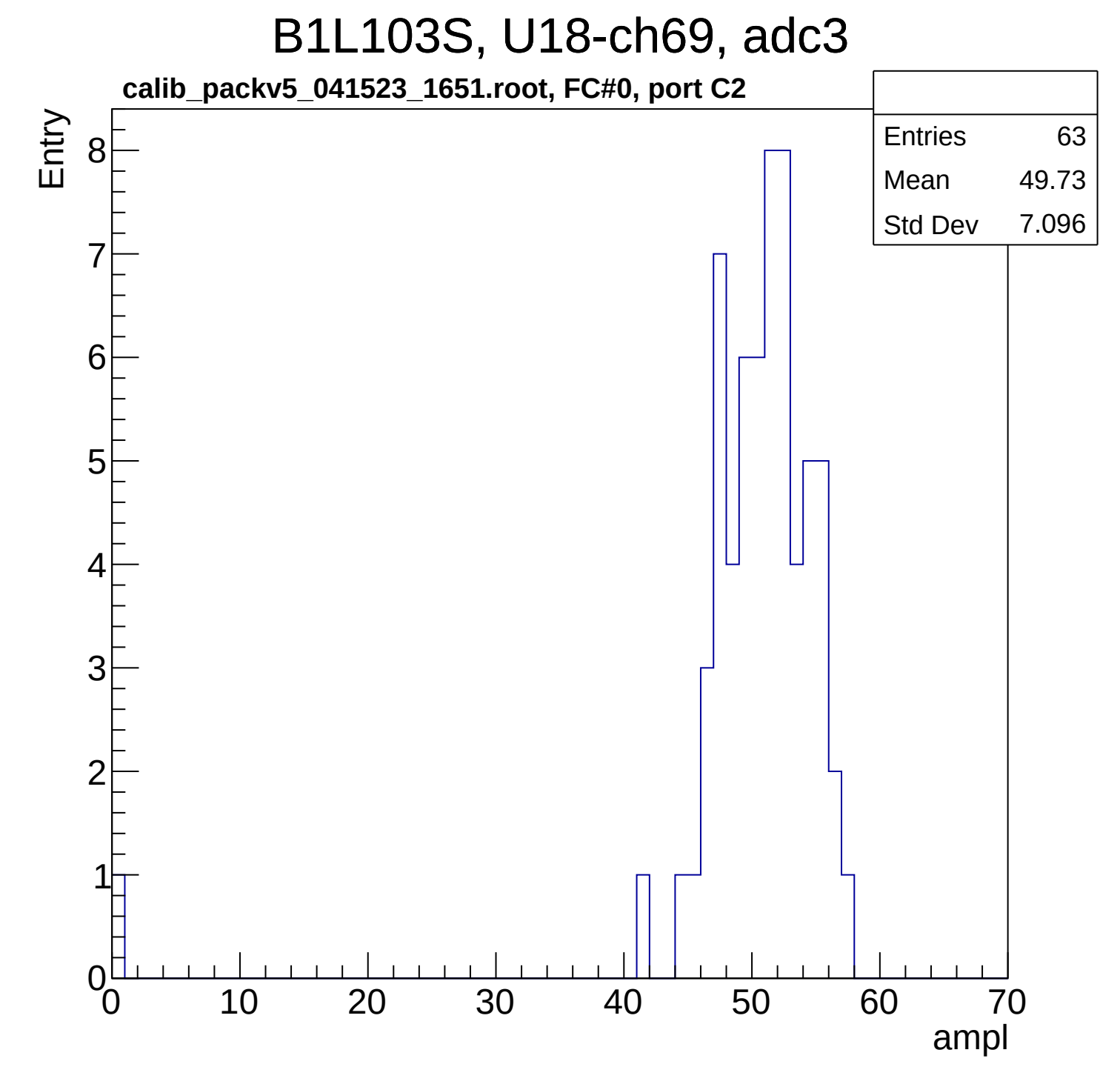
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch69, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 49.73
Std Dev 7.096
Entry
ampl
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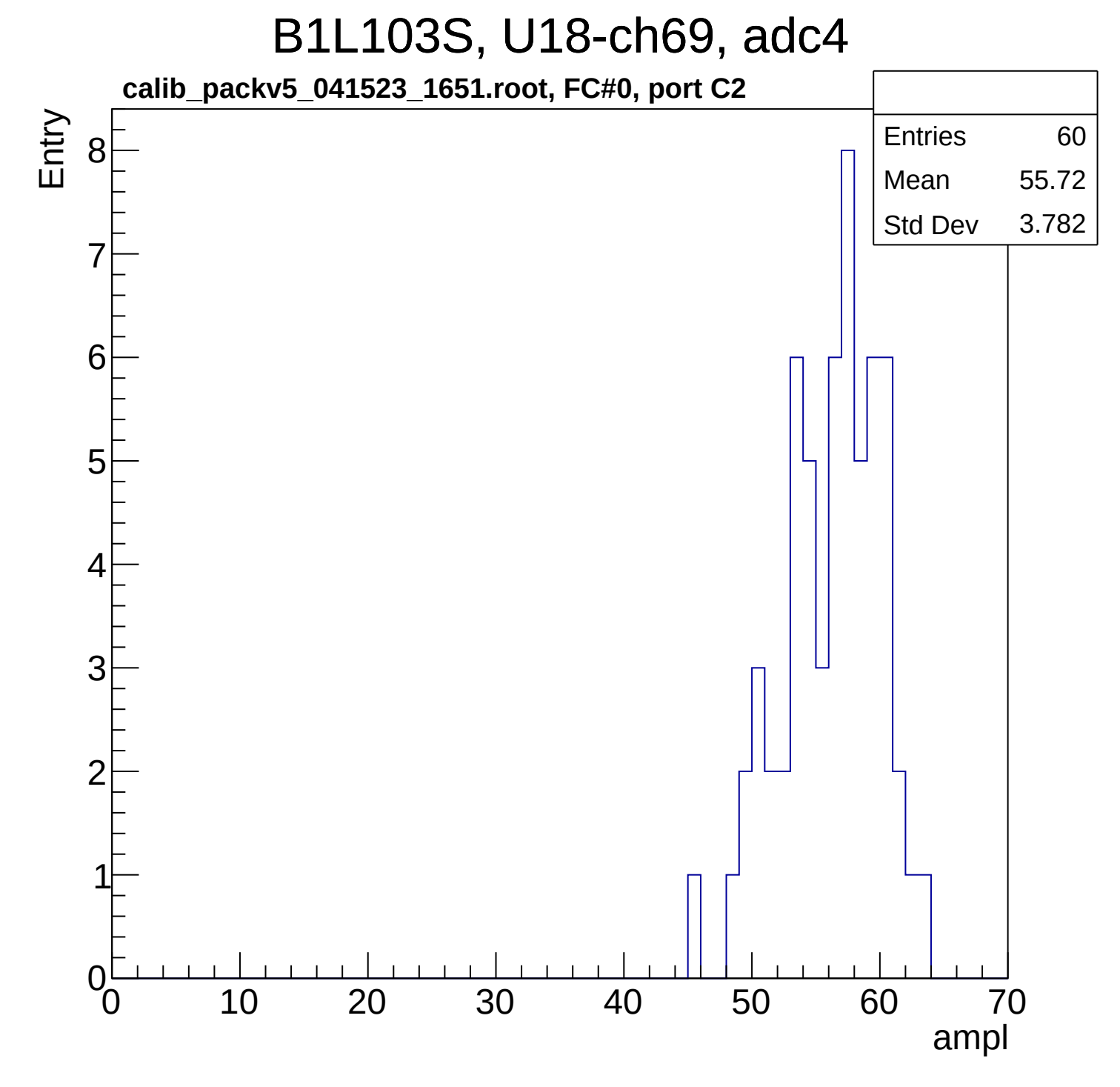
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch69, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 55.72
Std Dev 3.782
Entry
ampl
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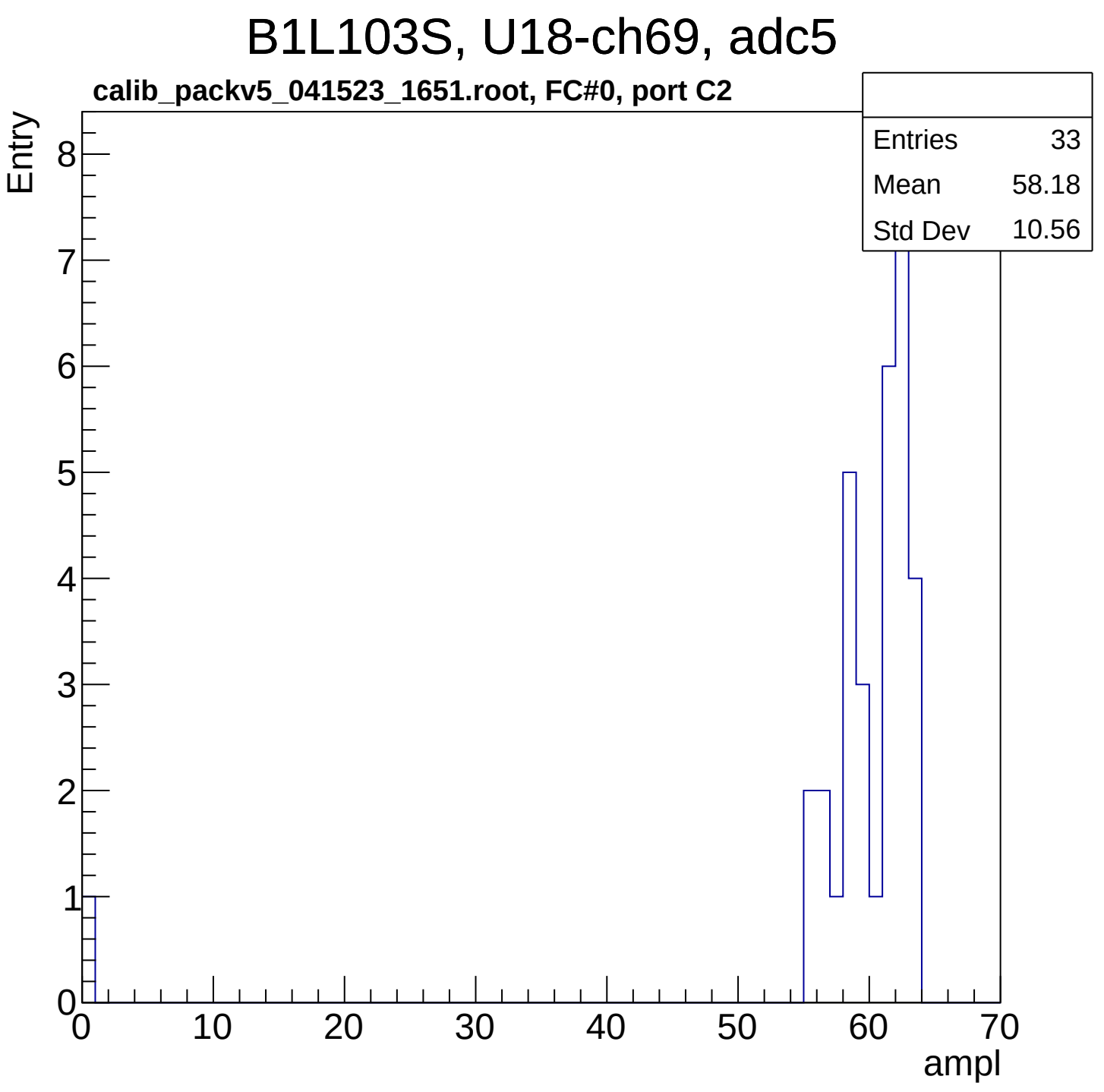
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch69, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 33
Mean 58.18
Std Dev 10.56
Entry
ampl
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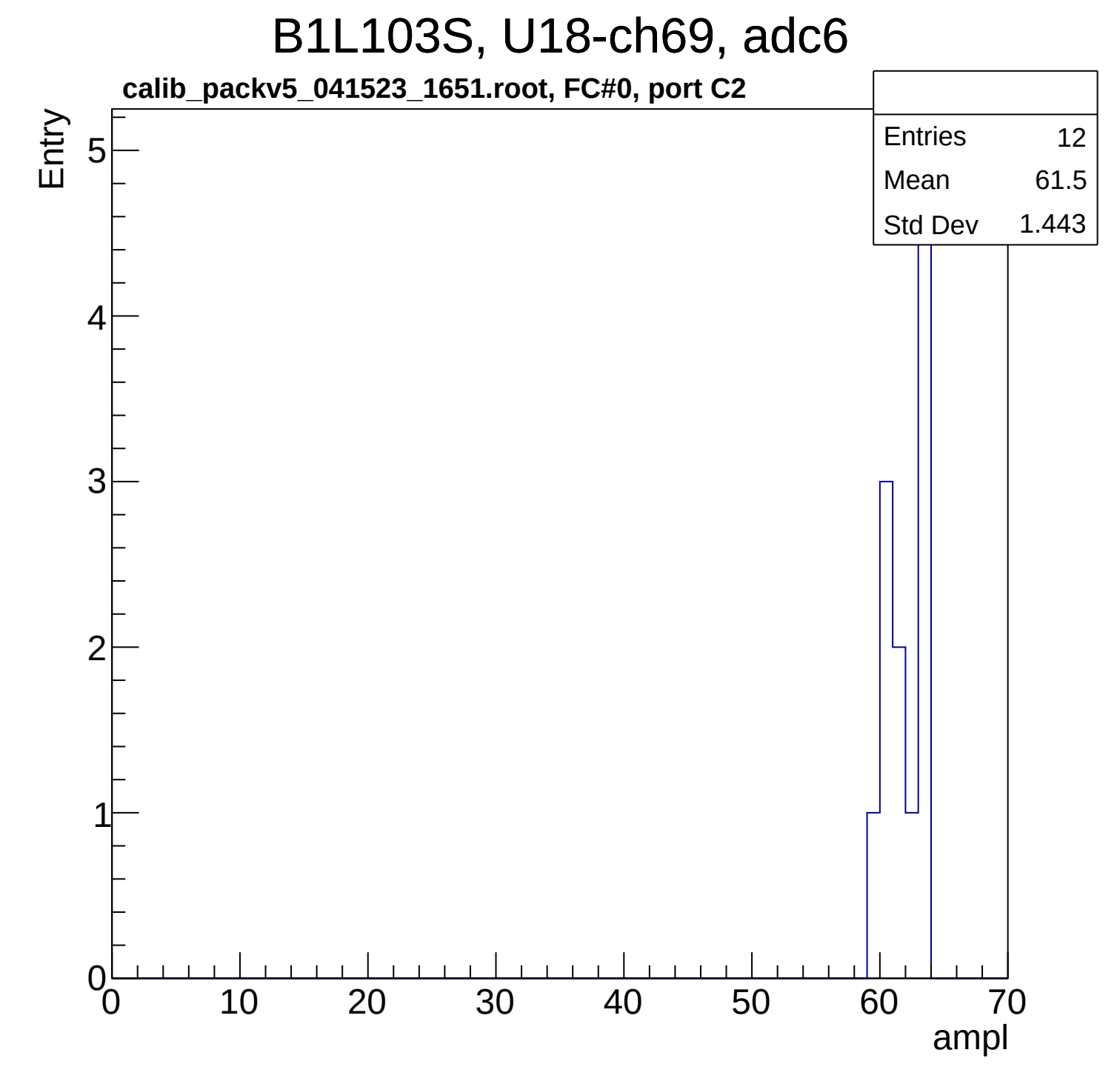
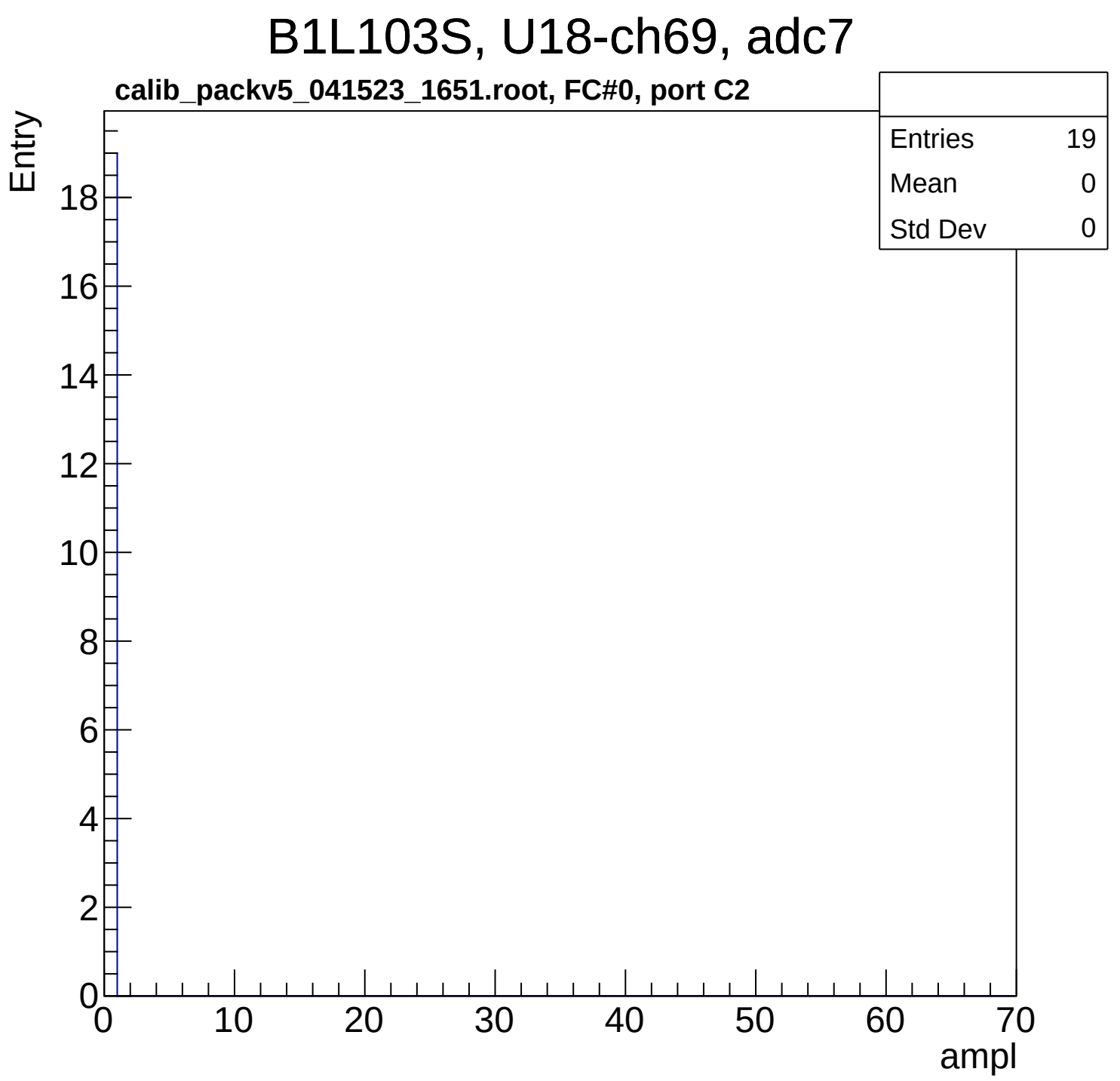
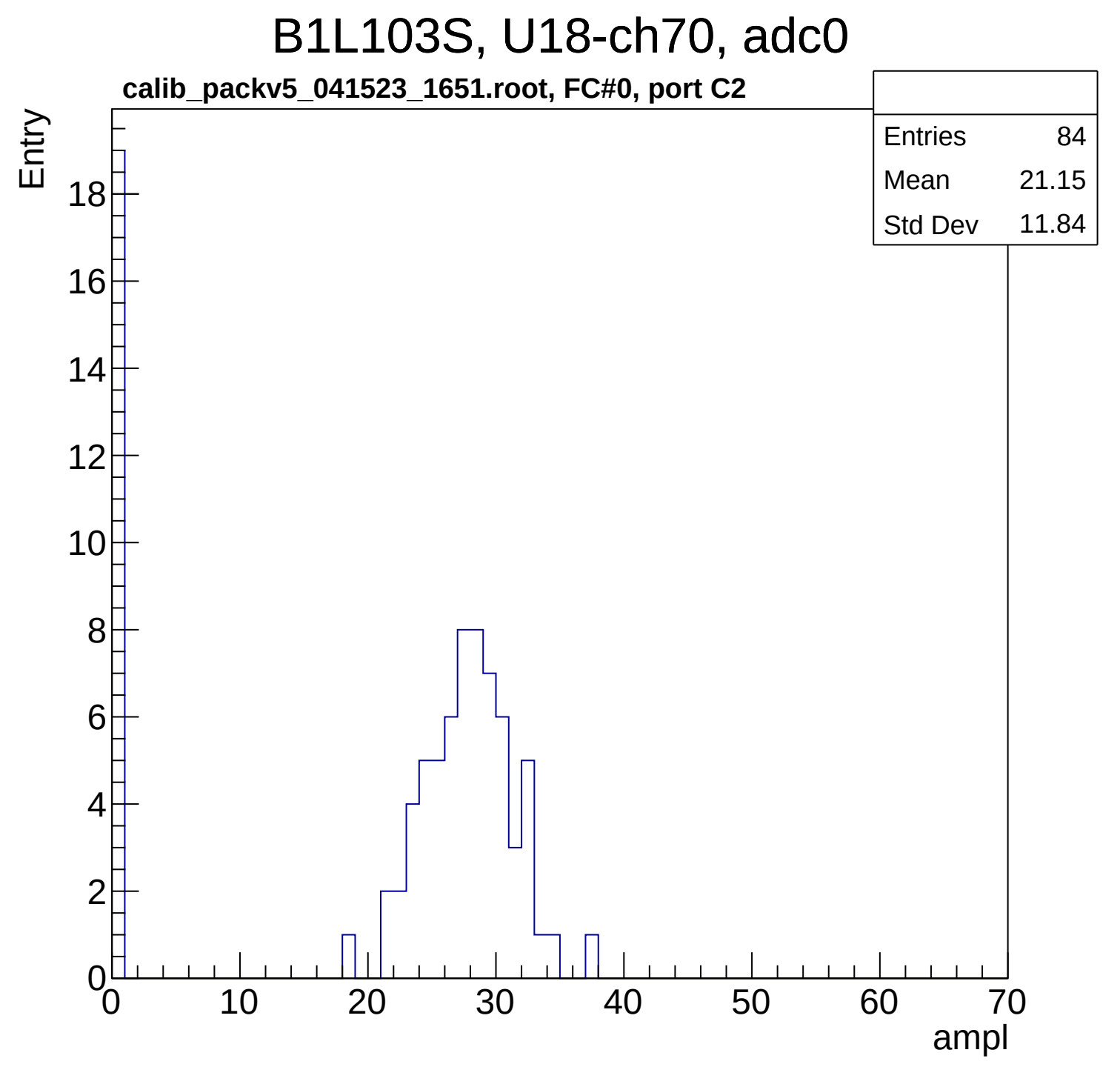
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch69, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 61.5
Std Dev 1.443
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U18-ch69, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch70, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 21.15
Std Dev 11.84
Entry
ampl
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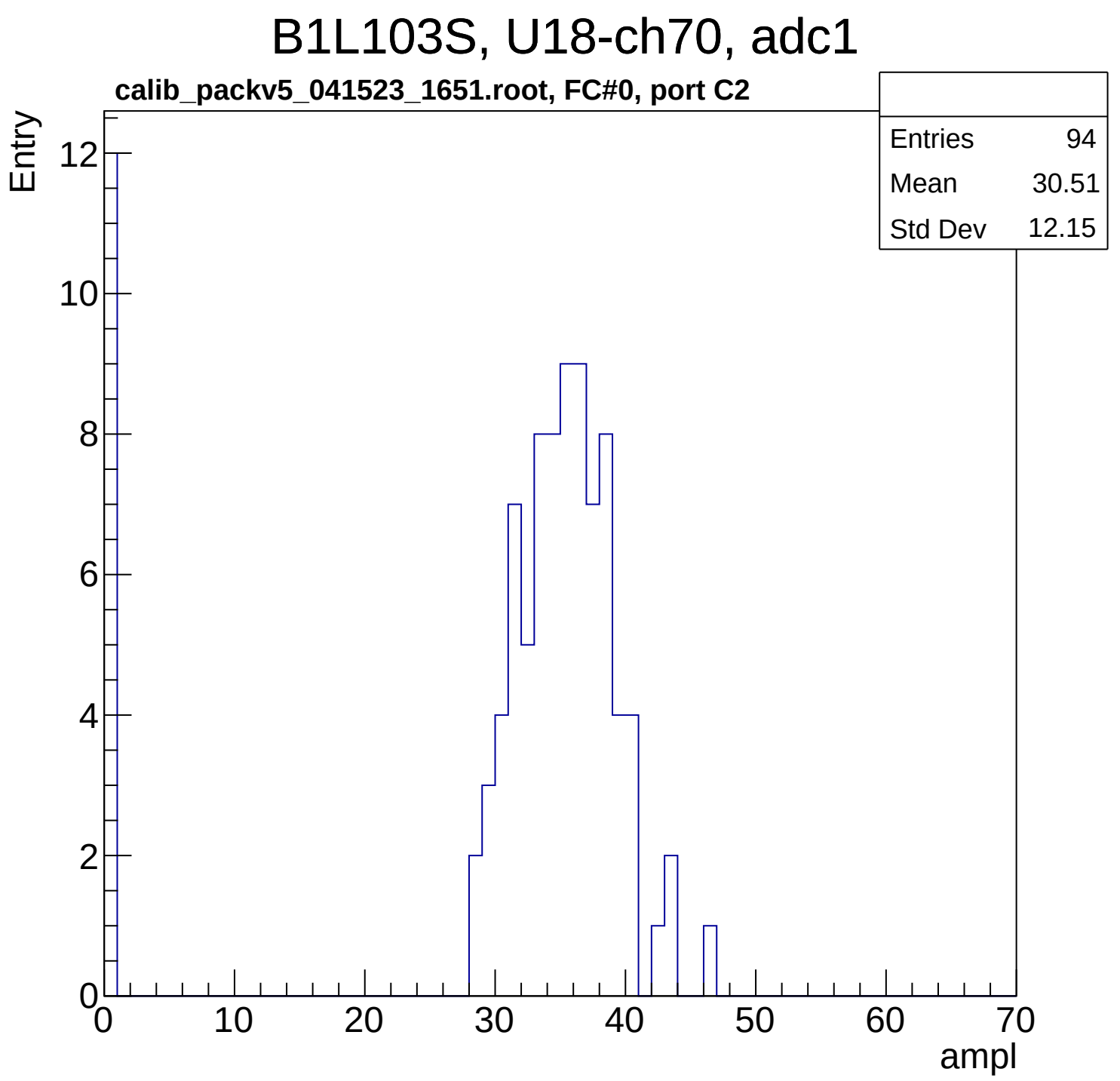
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70


B1L103S, U18-ch70, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 94
Mean 30.51
Std Dev 12.15
Entry
ampl
0
2
4
6
8
10
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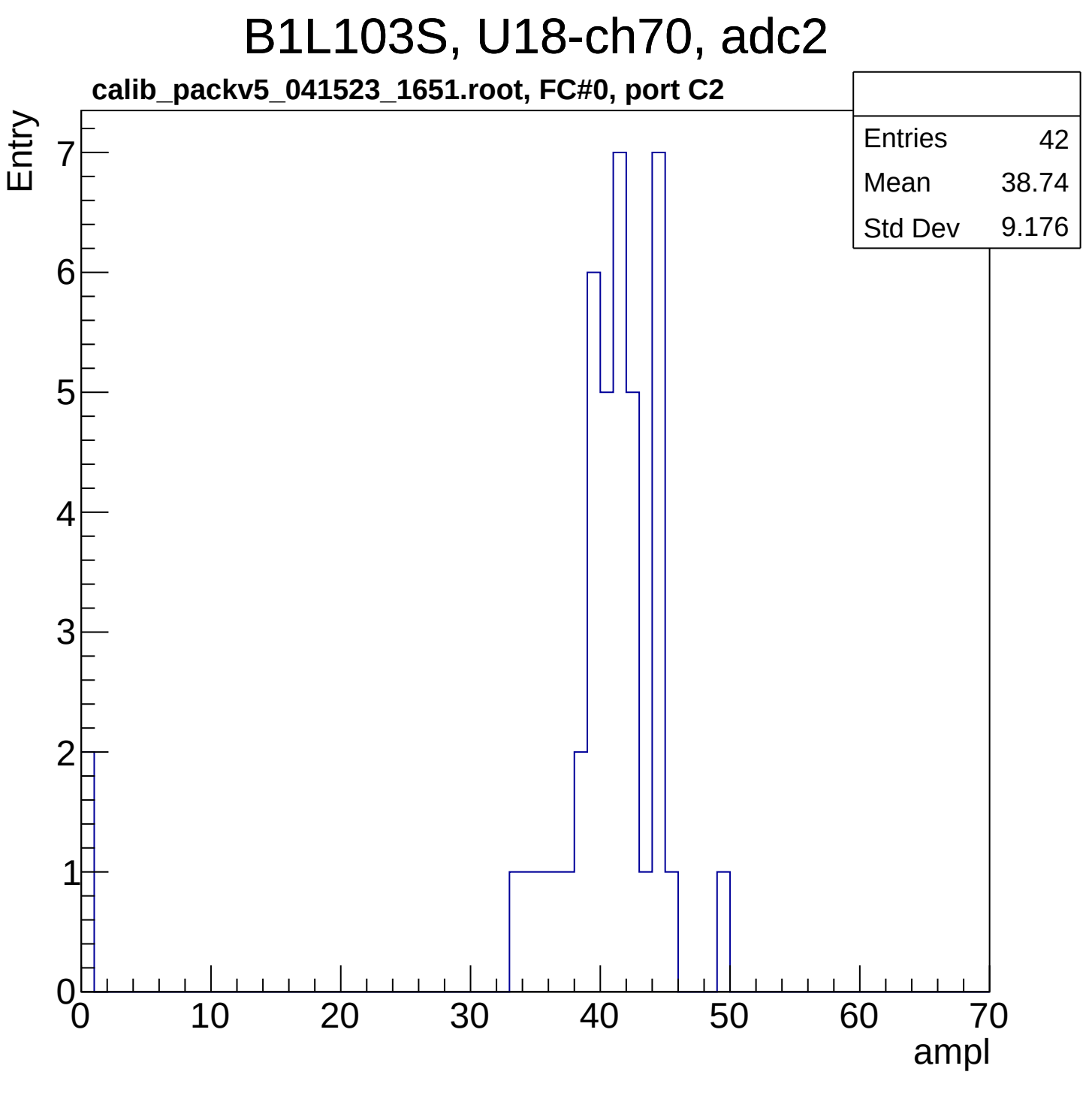
0
10
20
30
40
50
60
70


B1L103S, U18-ch70, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 42
Mean 38.74
Std Dev 9.176
Entry
ampl
0
1
2
3
4
5
6
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0
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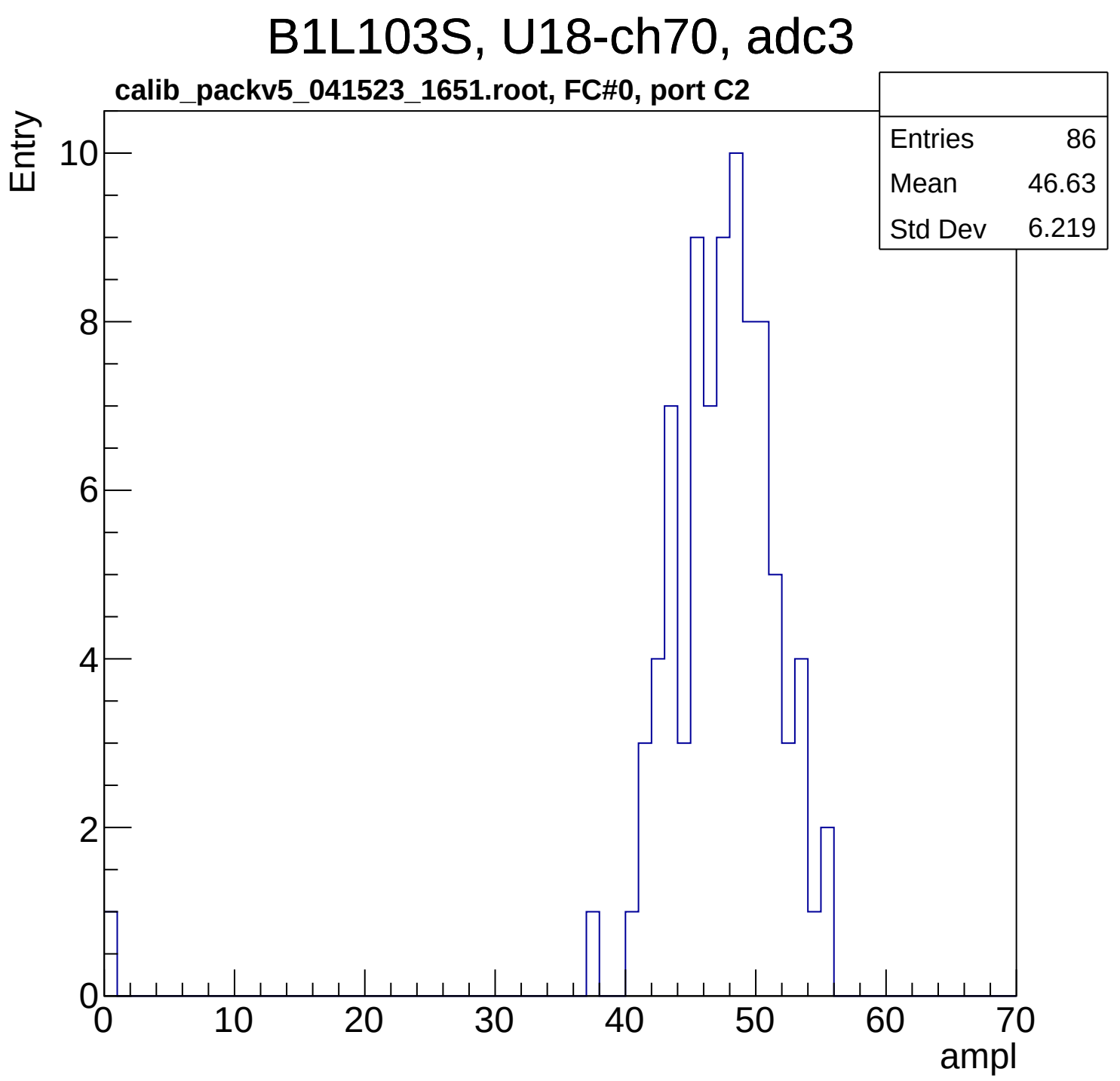
20
30
40
50
60
70


B1L103S, U18-ch70, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 46.63
Std Dev 6.219
Entry
0
2
4
6
8
10
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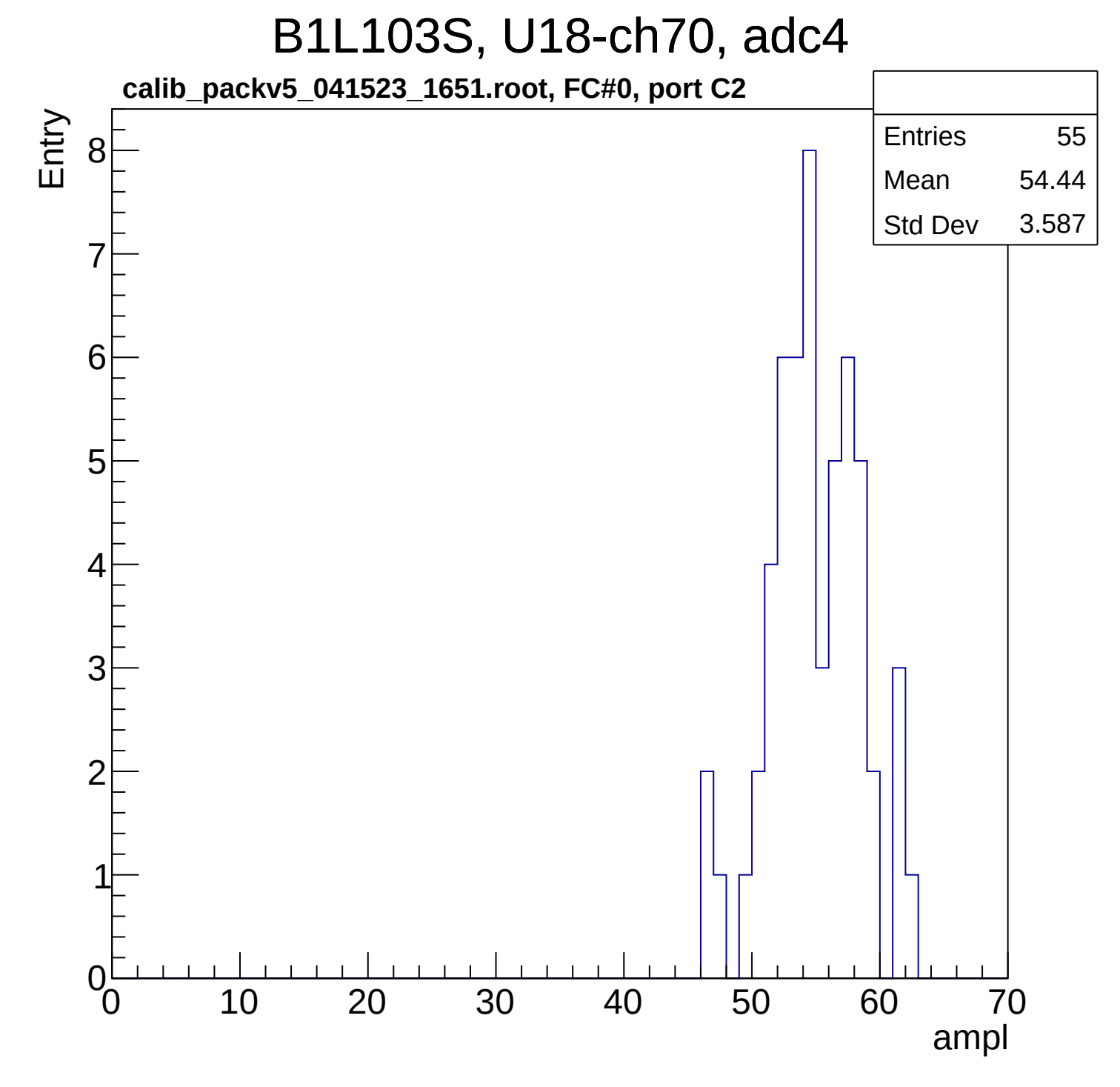
50
60
70
ampl


B1L103S, U18-ch70, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 54.44
Std Dev 3.587
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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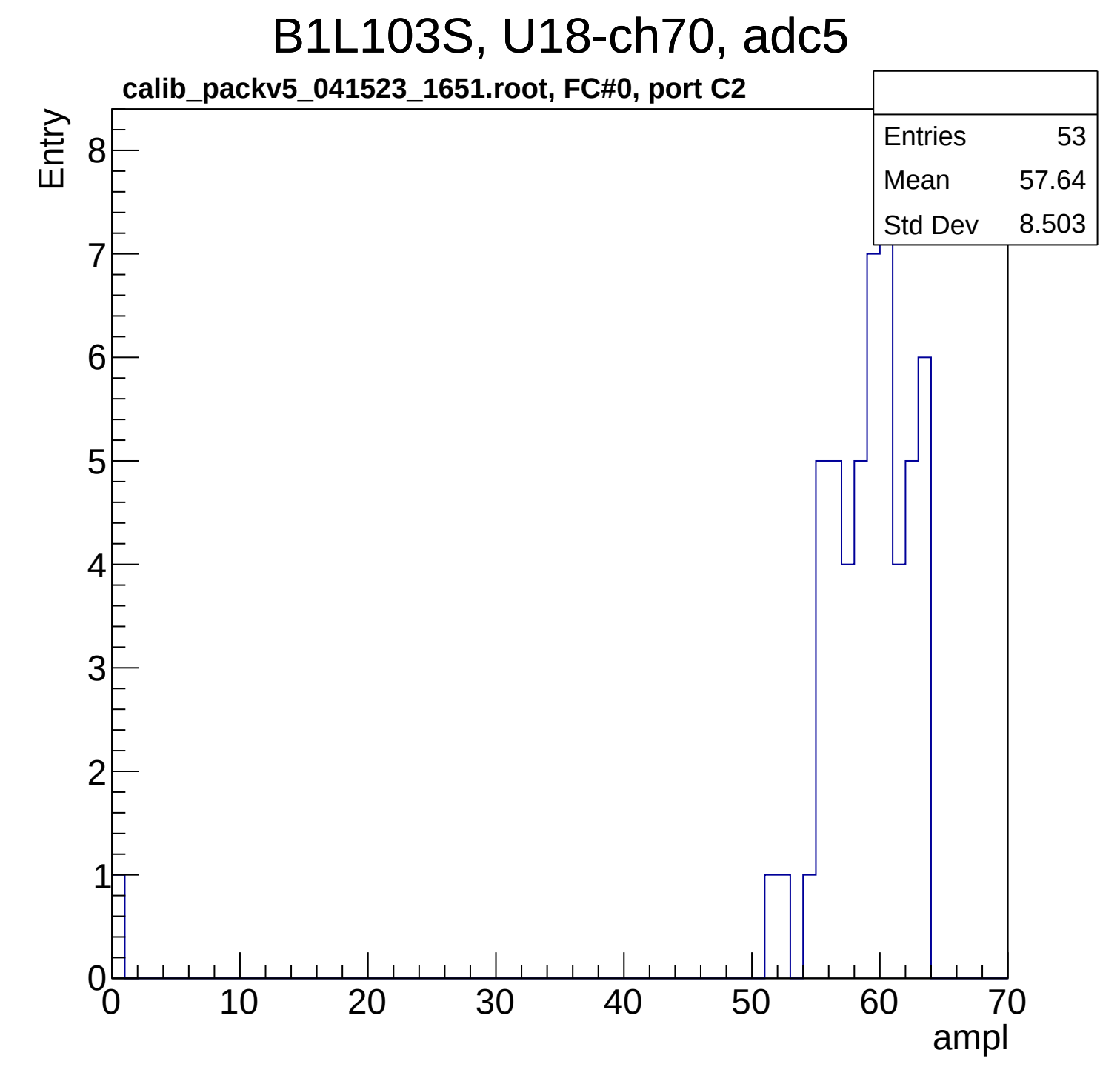
40
50
60
70


B1L103S, U18-ch70, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 57.64
Std Dev 8.503
Entry
ampl
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1
2
3
4
5
6
7
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0
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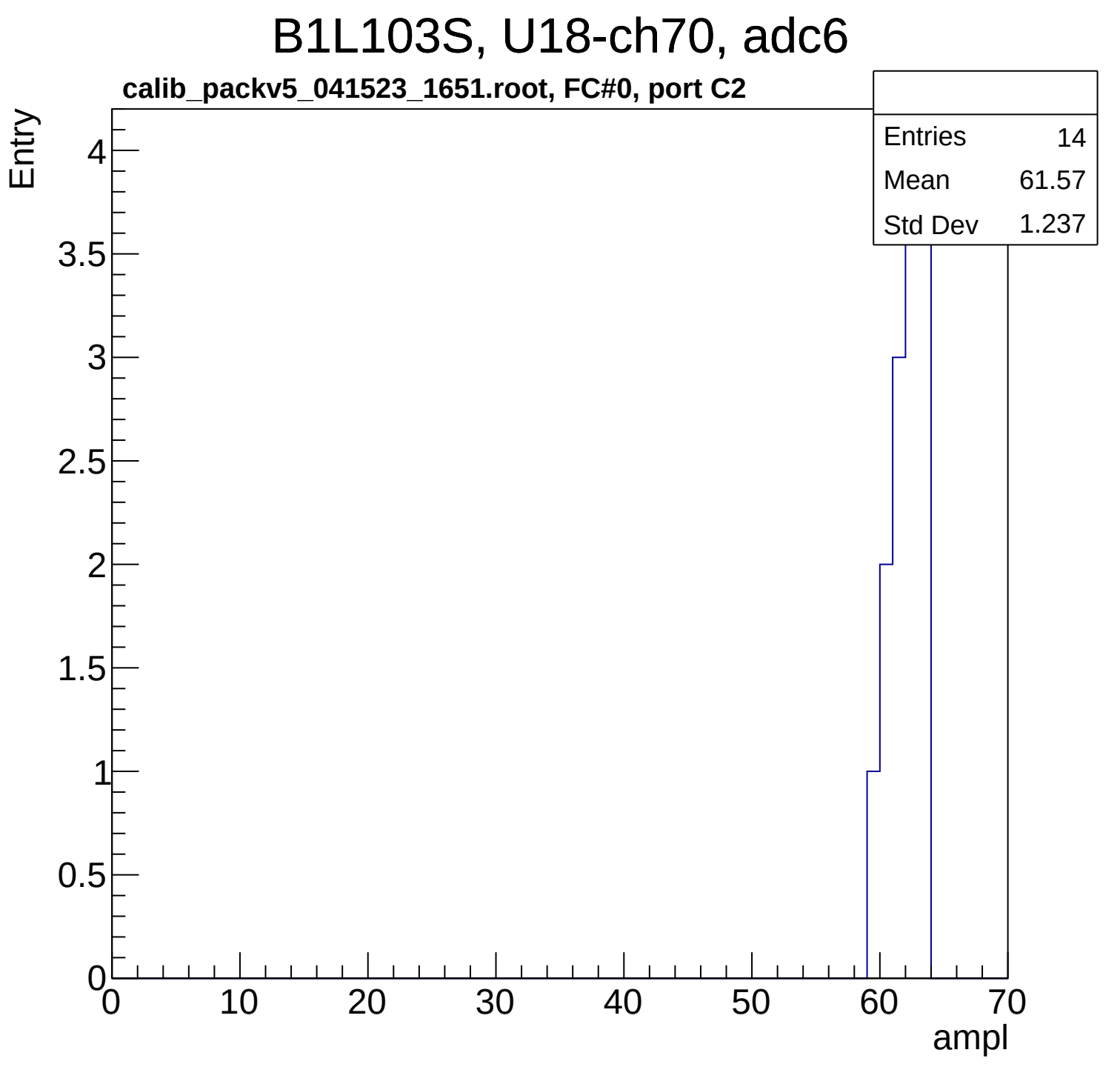
40
50
60
70


B1L103S, U18-ch70, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 14
Mean 61.57
Std Dev 1.237
Entry
ampl
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0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
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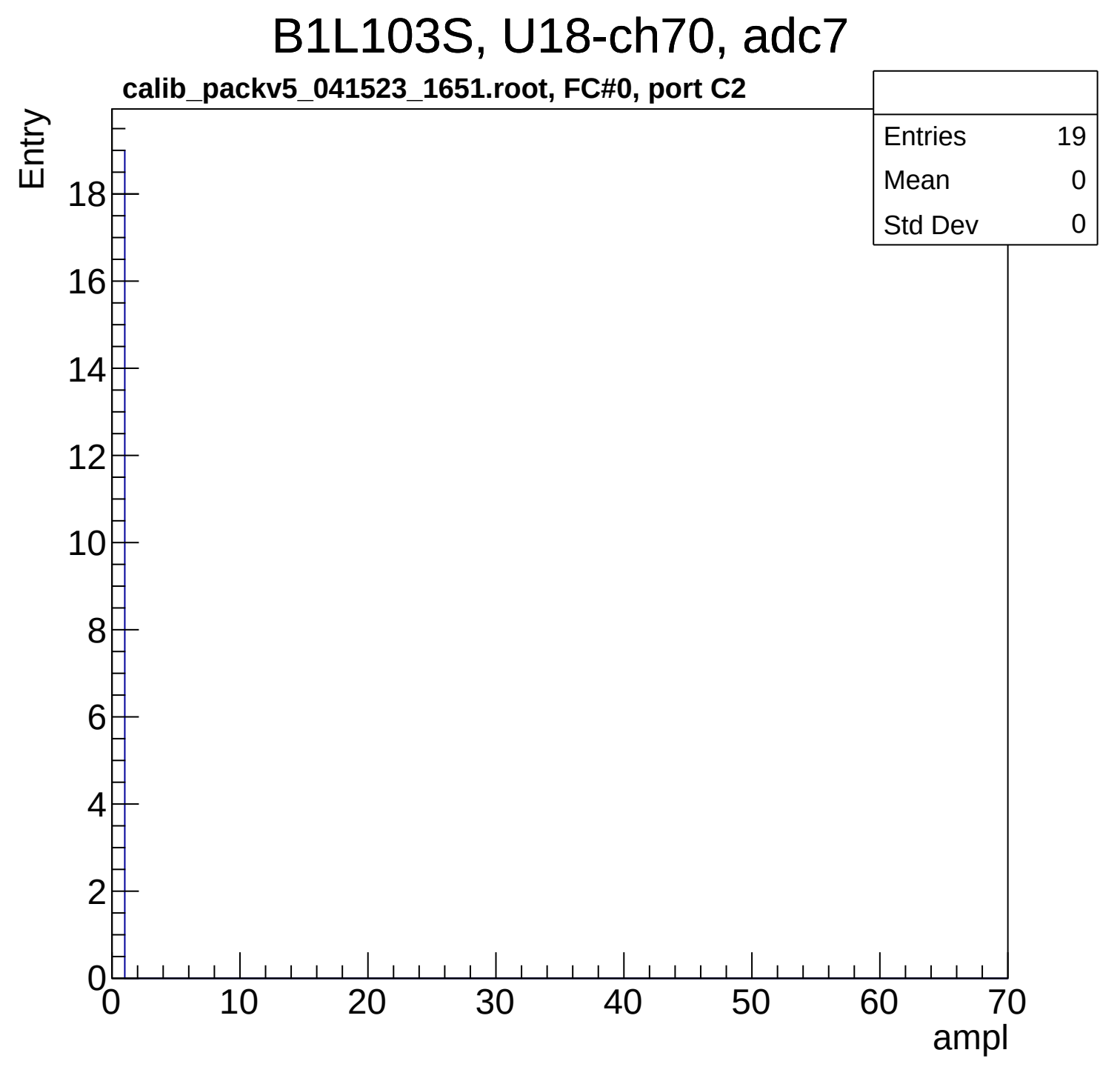
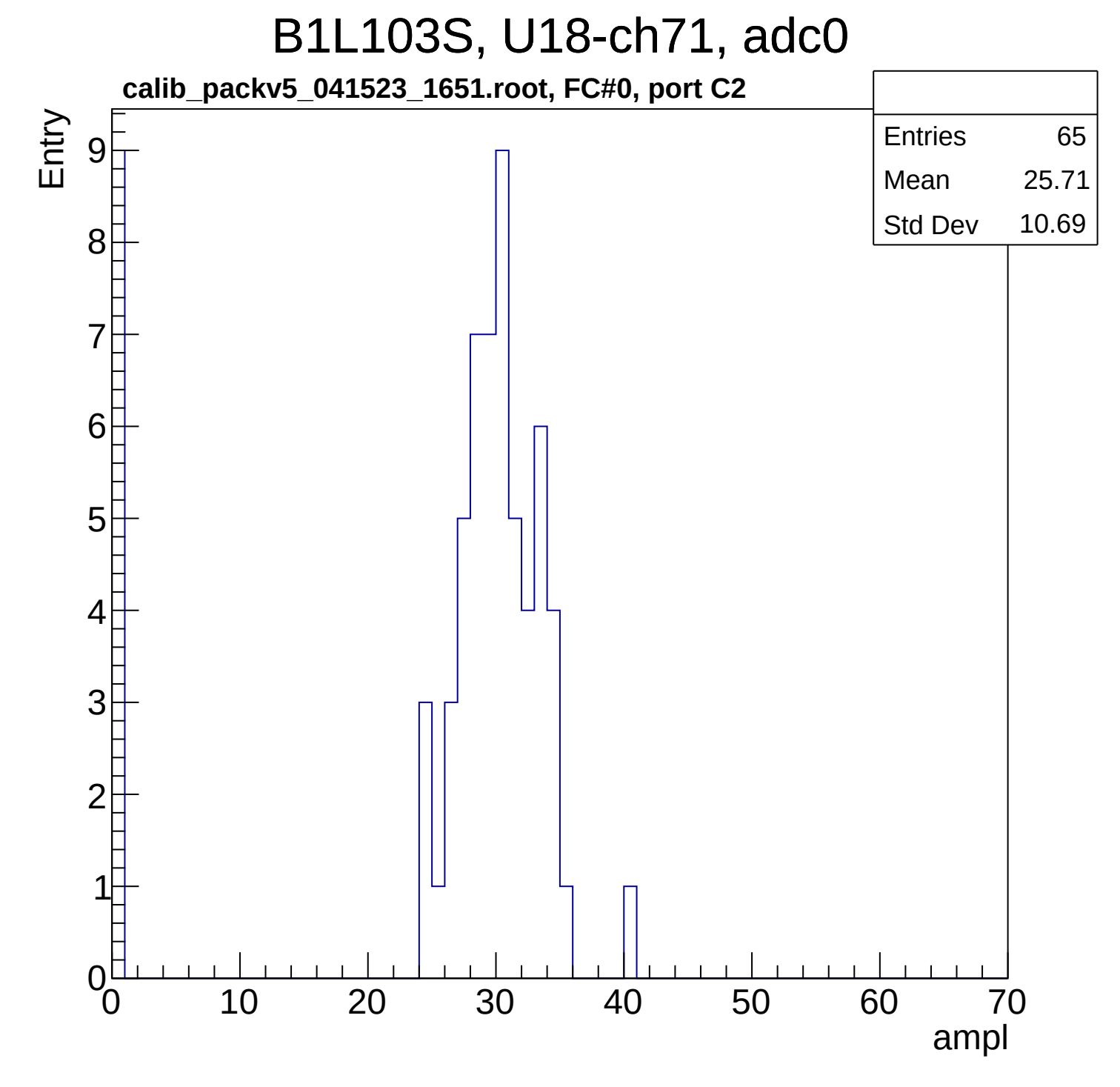
40
50
60
70


B1L103S, U18-ch70, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch71, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 25.71
Std Dev 10.69
Entry
ampl
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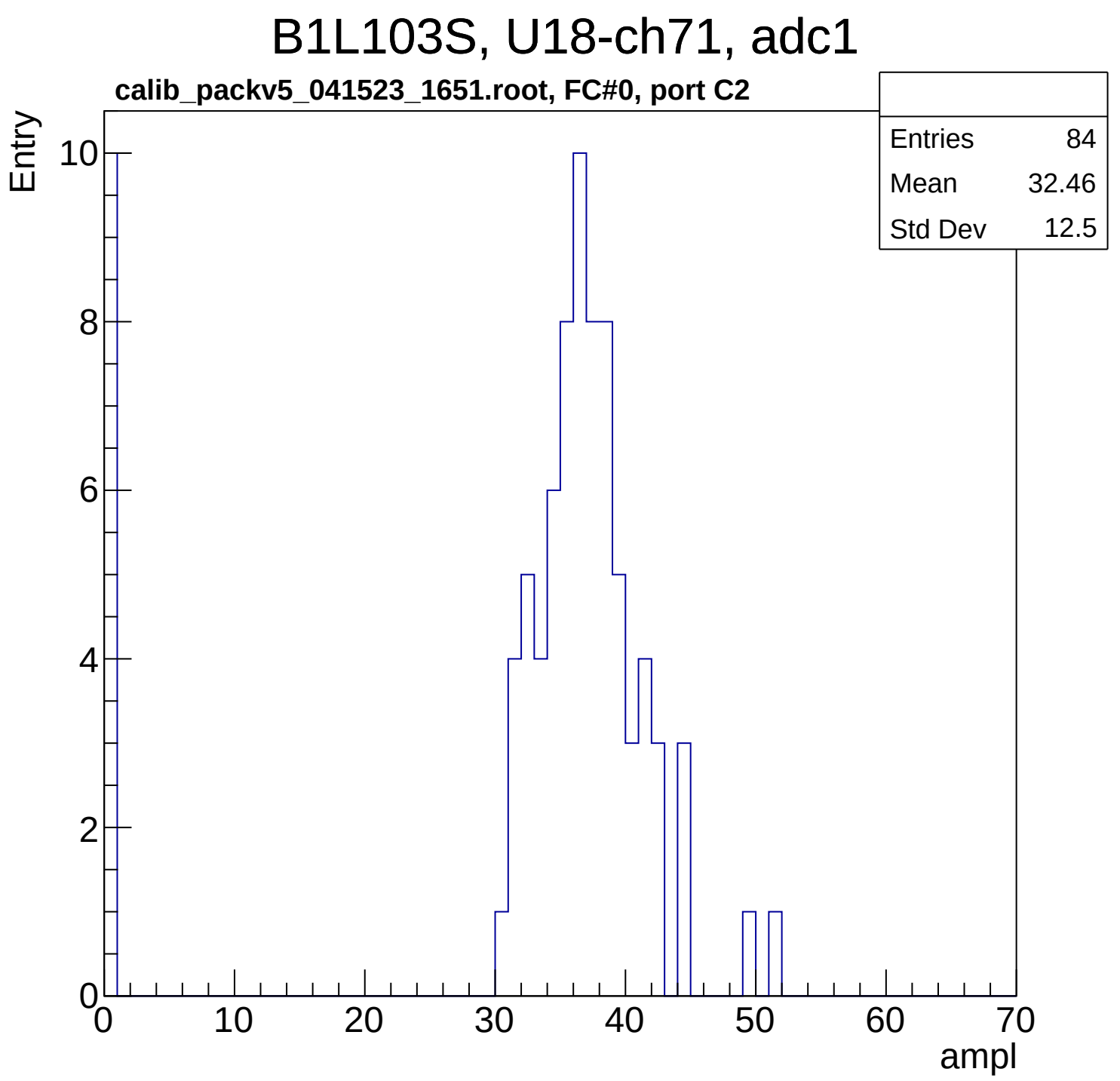
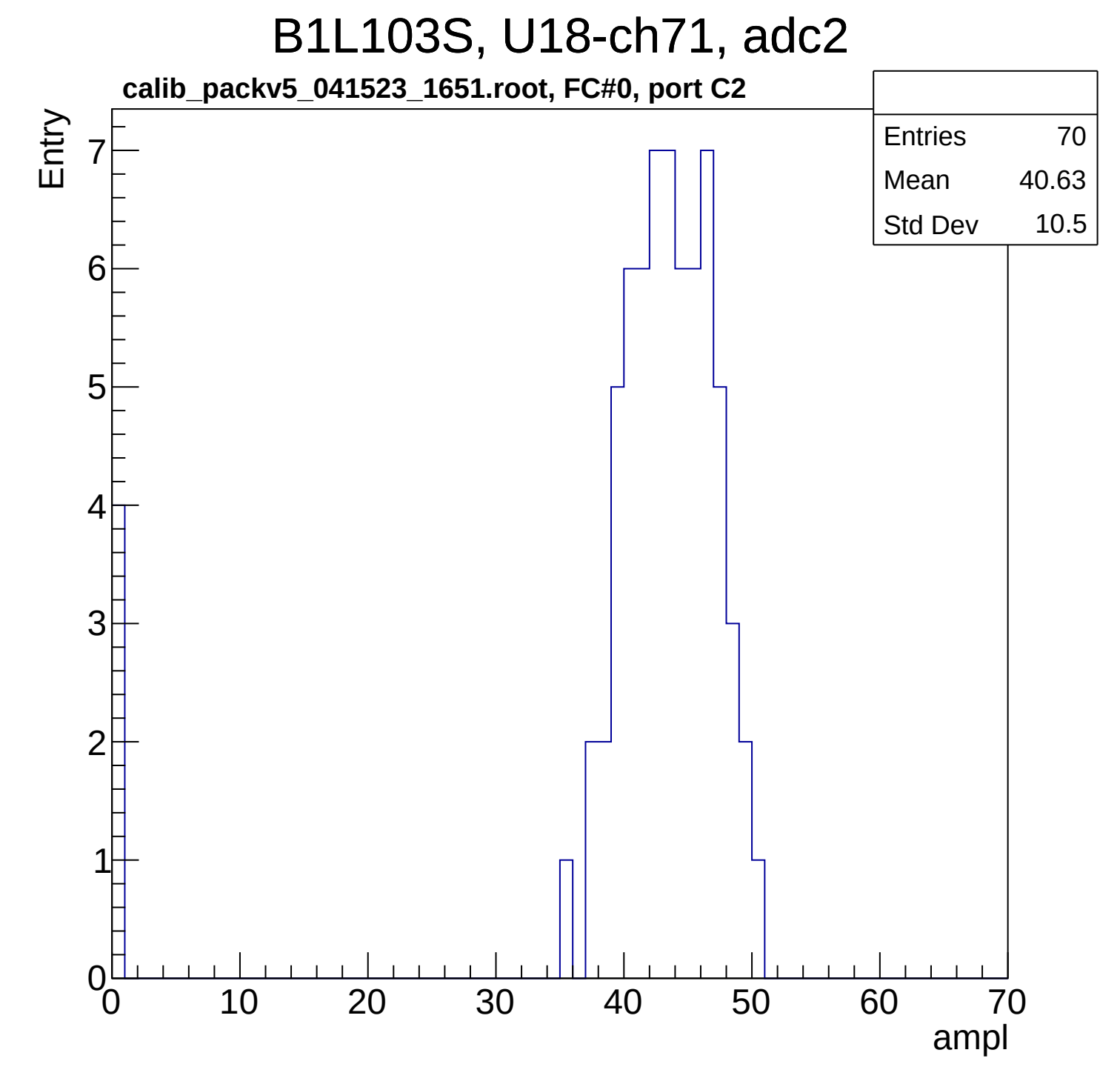
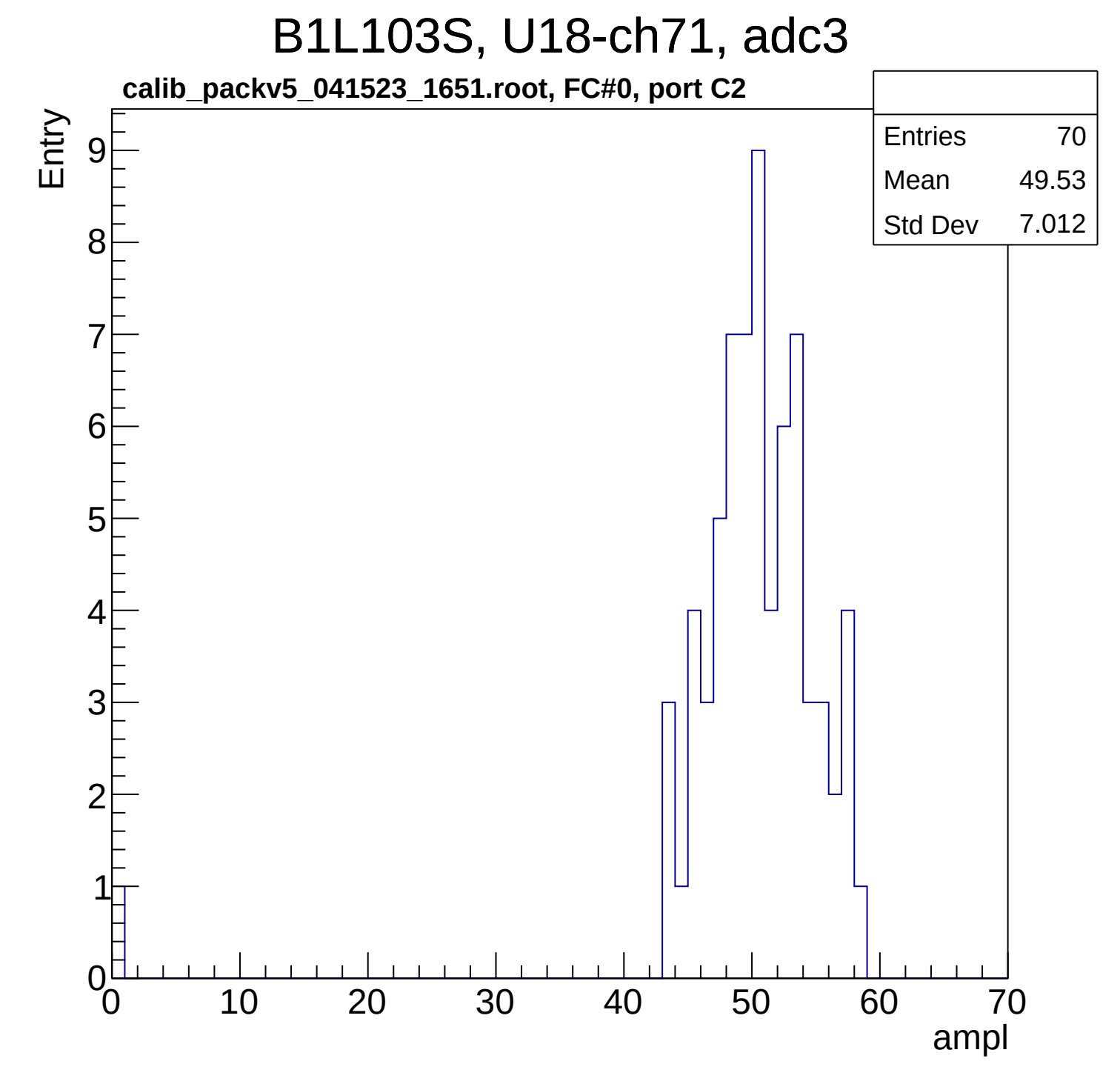
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U18-ch71, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 32.46
Std Dev 12.5
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch71, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 40.63
Std Dev 10.5
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U18-ch71, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 49.53
Std Dev 7.012
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
50
60
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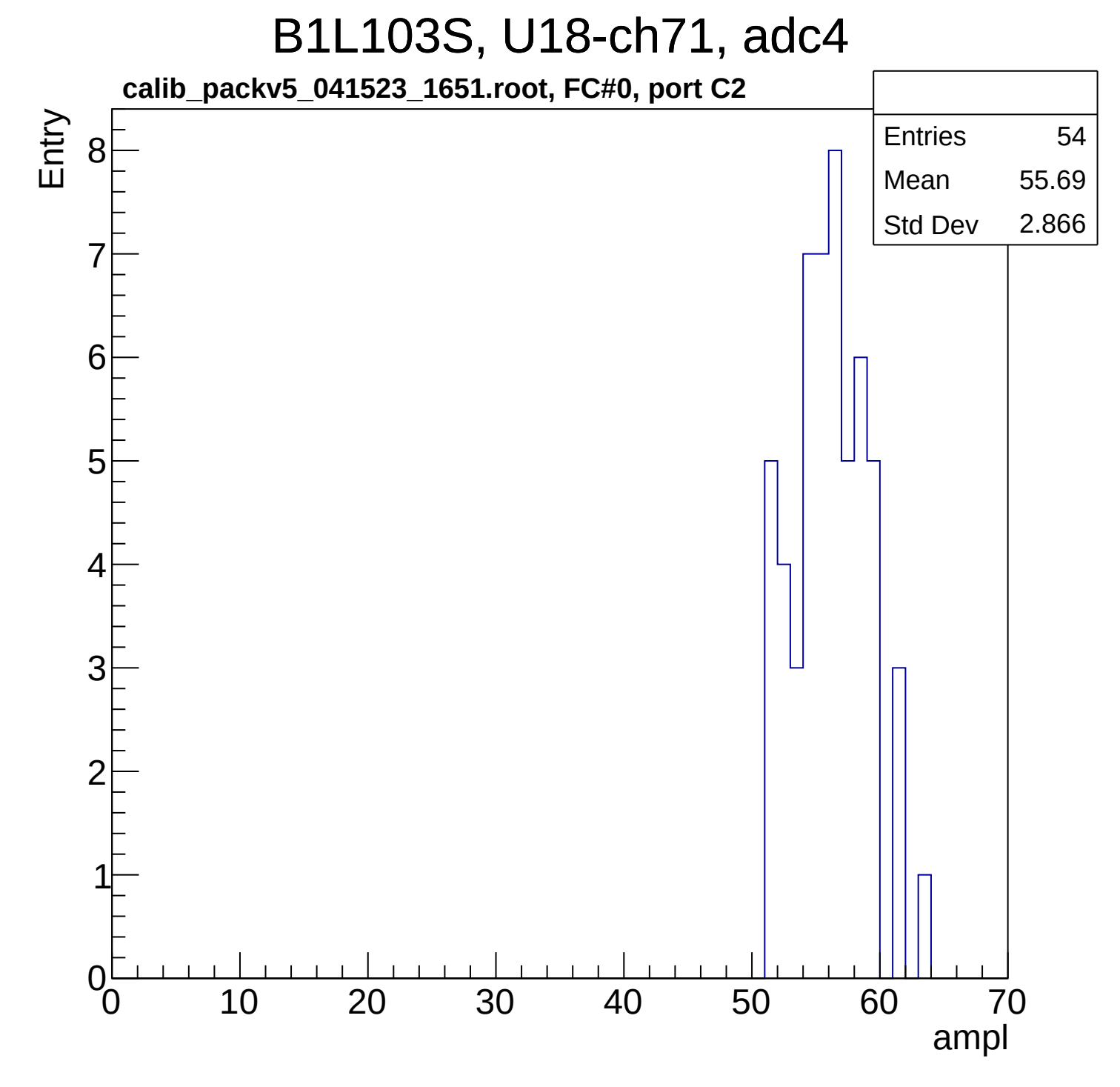
B1L103S, U18-ch71, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 55.69
Std Dev 2.866
Entry
ampl
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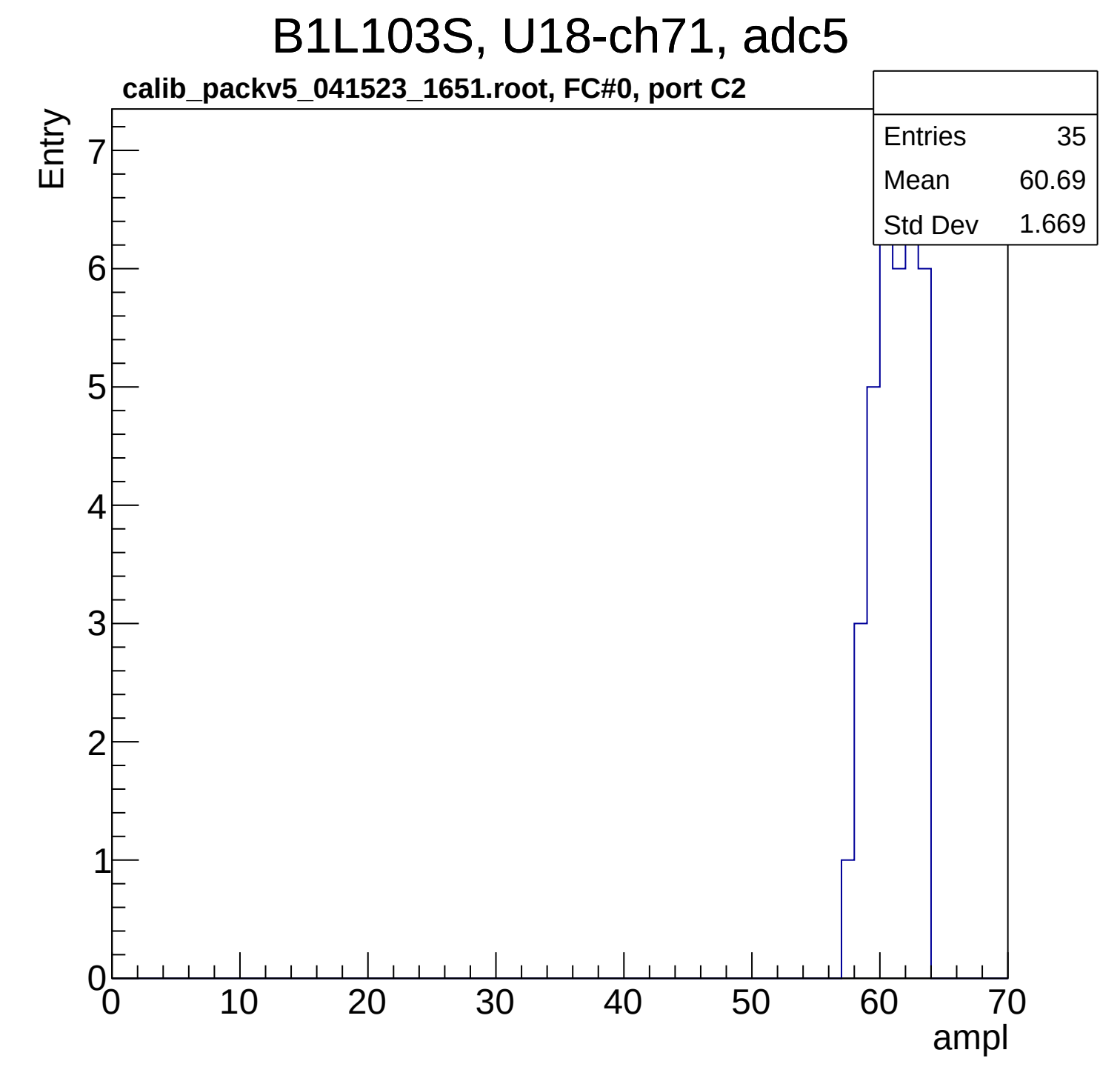
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch71, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 35
Mean 60.69
Std Dev 1.669
Entry
ampl
0
1
2
3
4
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0
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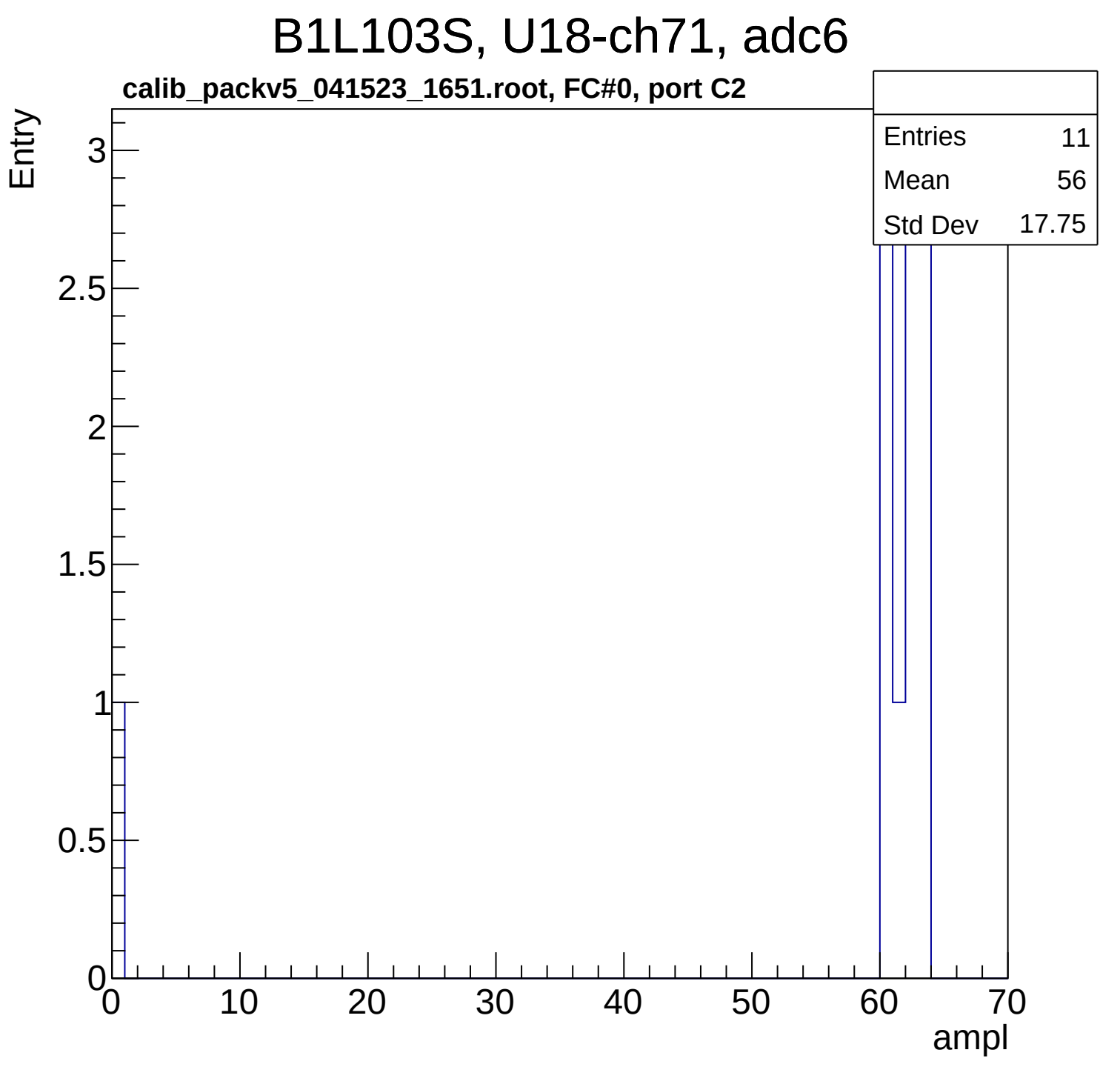
60
70


B1L103S, U18-ch71, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 56
Std Dev 17.75
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
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40
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60
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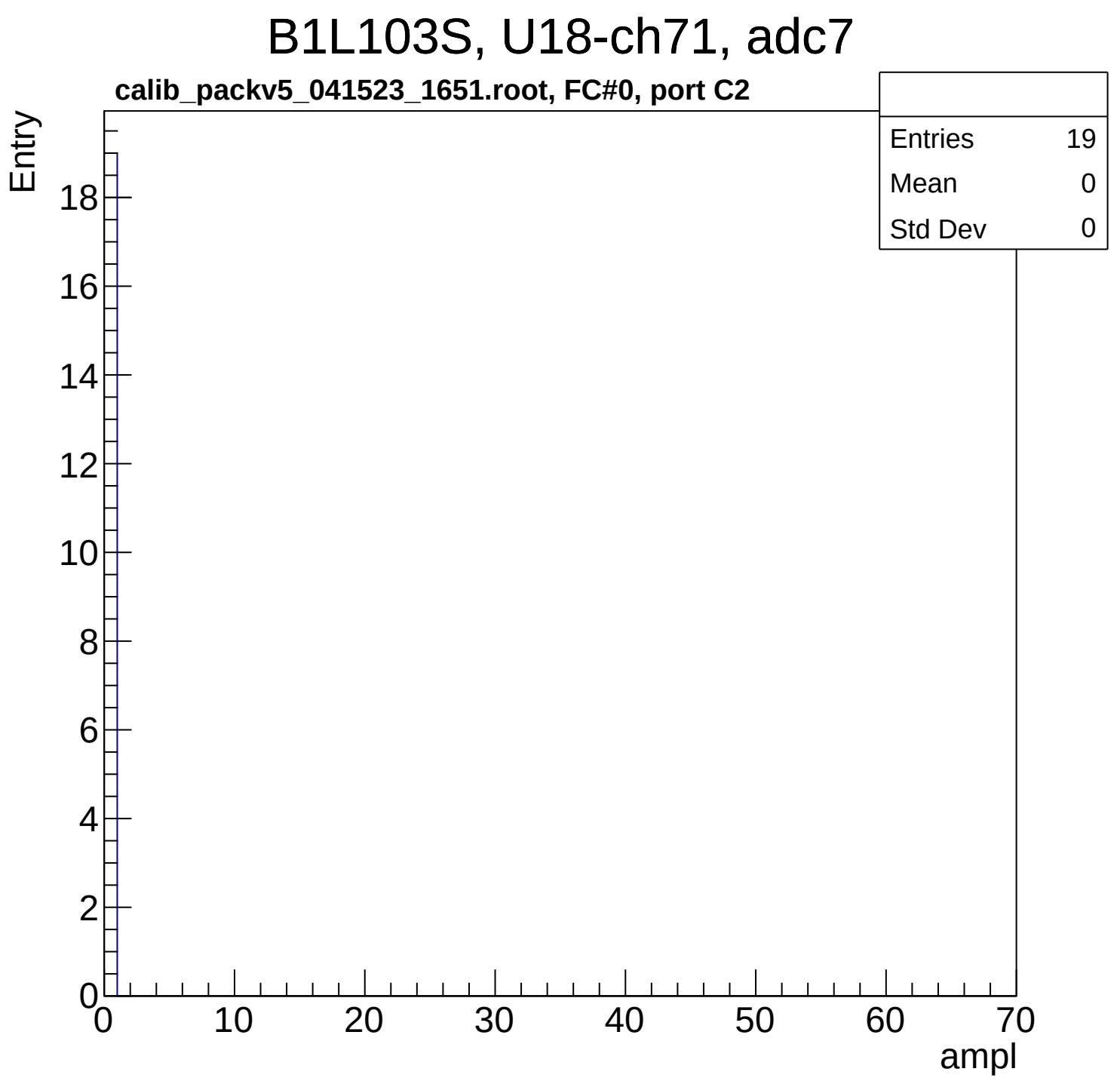
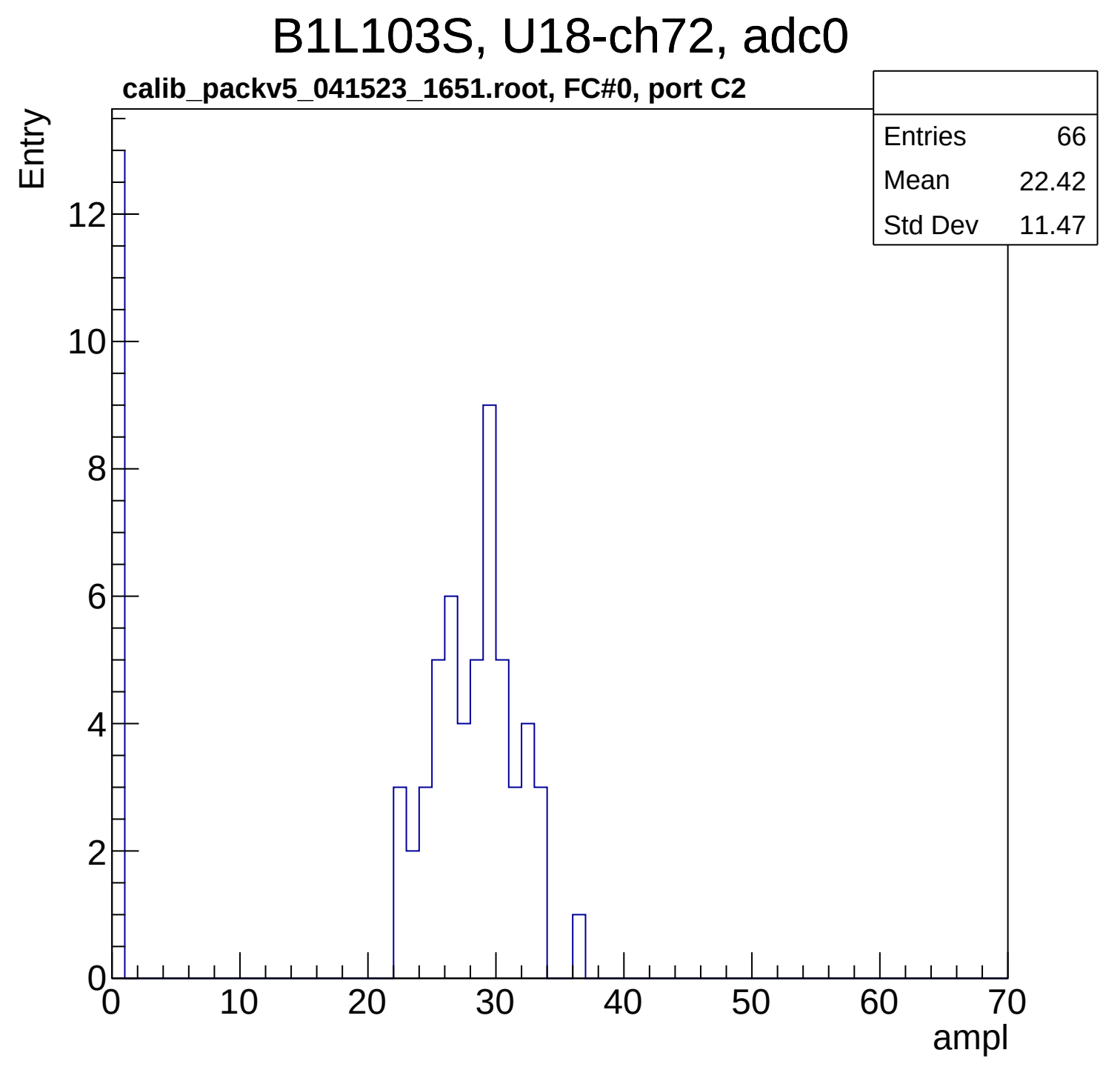
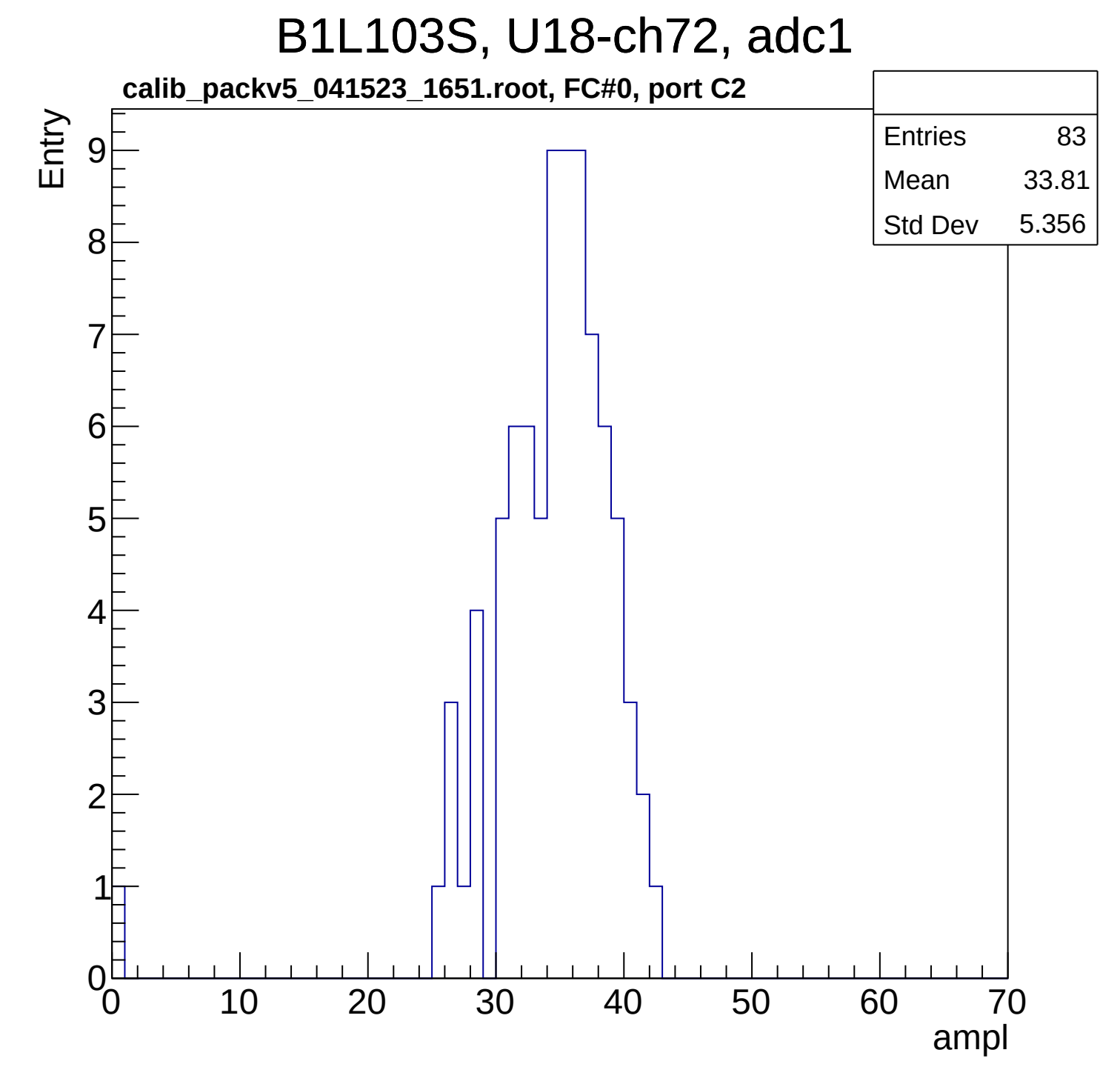

B1L103S, U18-ch71, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch72, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 22.42
Std Dev 11.47
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch72, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 33.81
Std Dev 5.356
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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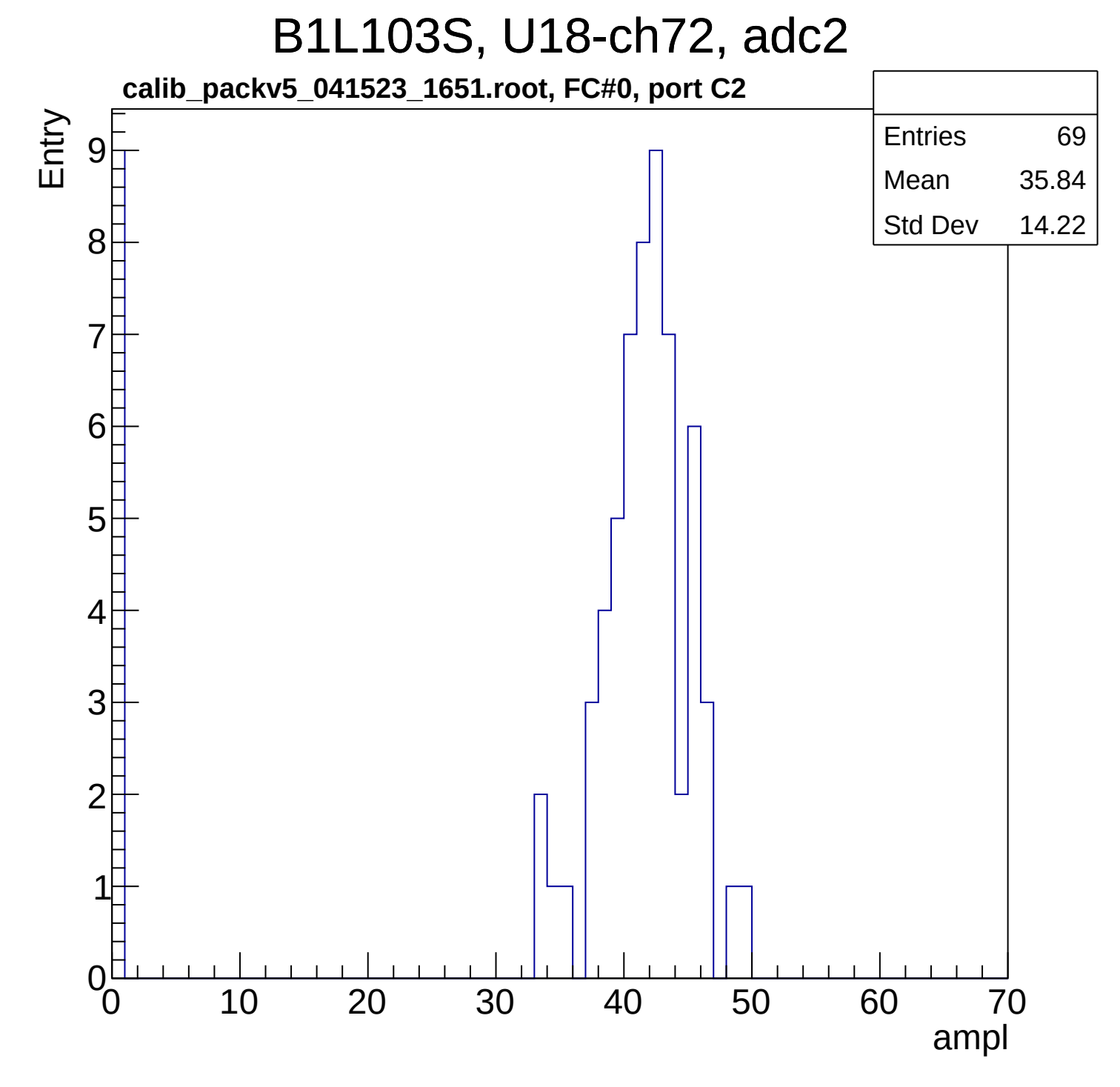
B1L103S, U18-ch72, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 35.84
Std Dev 14.22
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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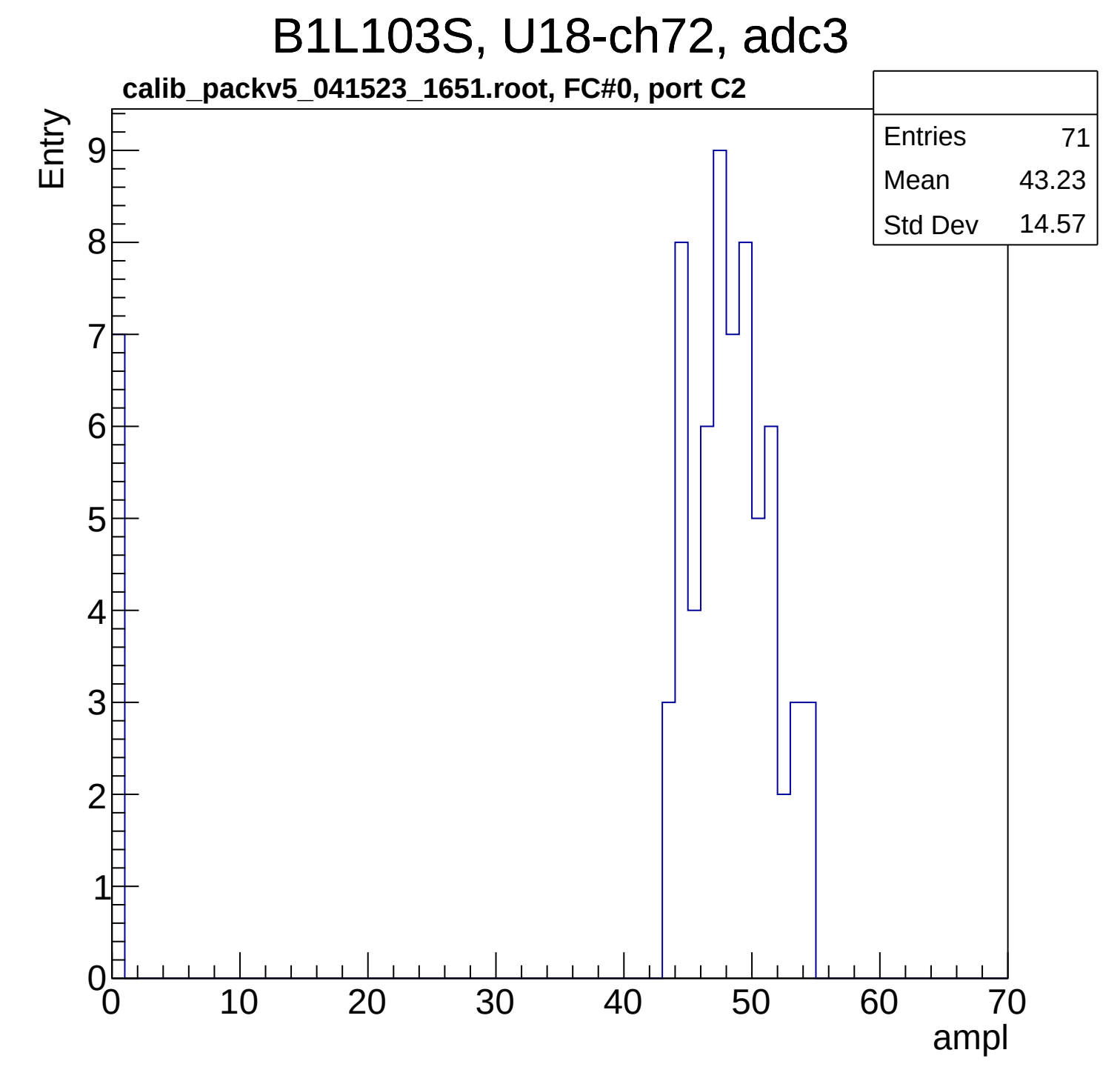
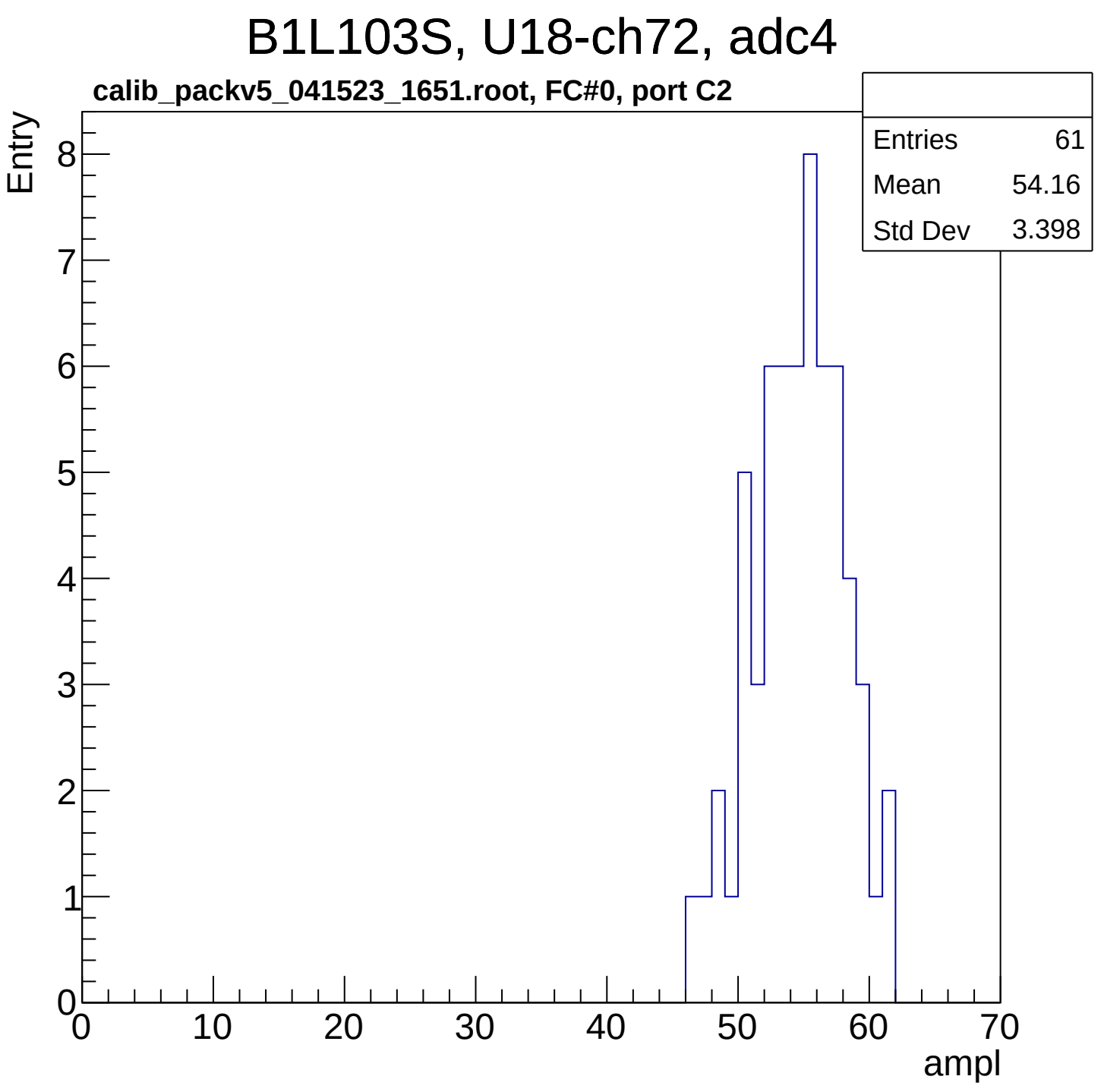

B1L103S, U18-ch72, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 43.23
Std Dev 14.57
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U18-ch72, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 54.16
Std Dev 3.398
Entry
ampl
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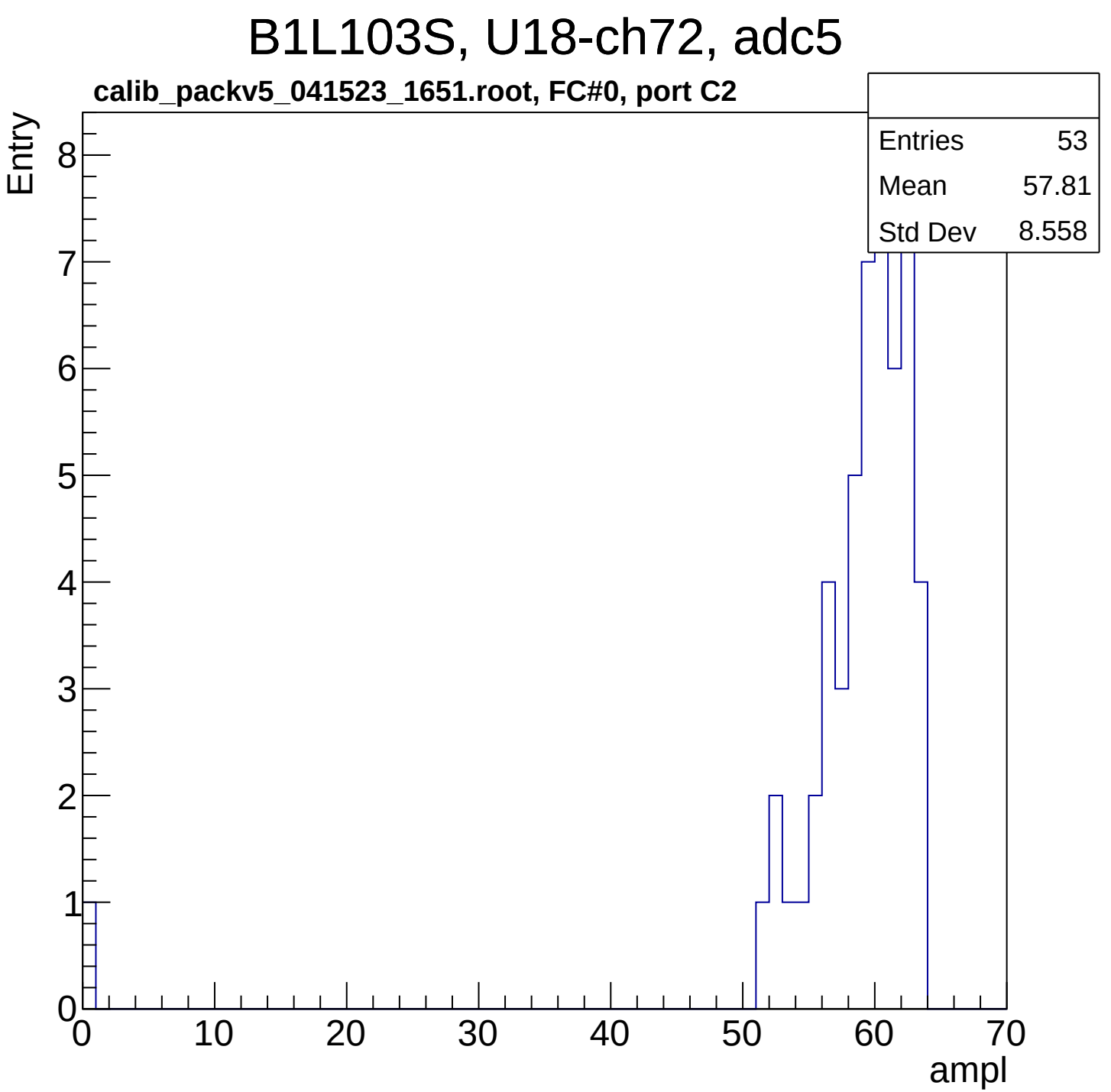
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch72, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 57.81
Std Dev 8.558
Entry
ampl
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1
2
3
4
5
6
7
8
0
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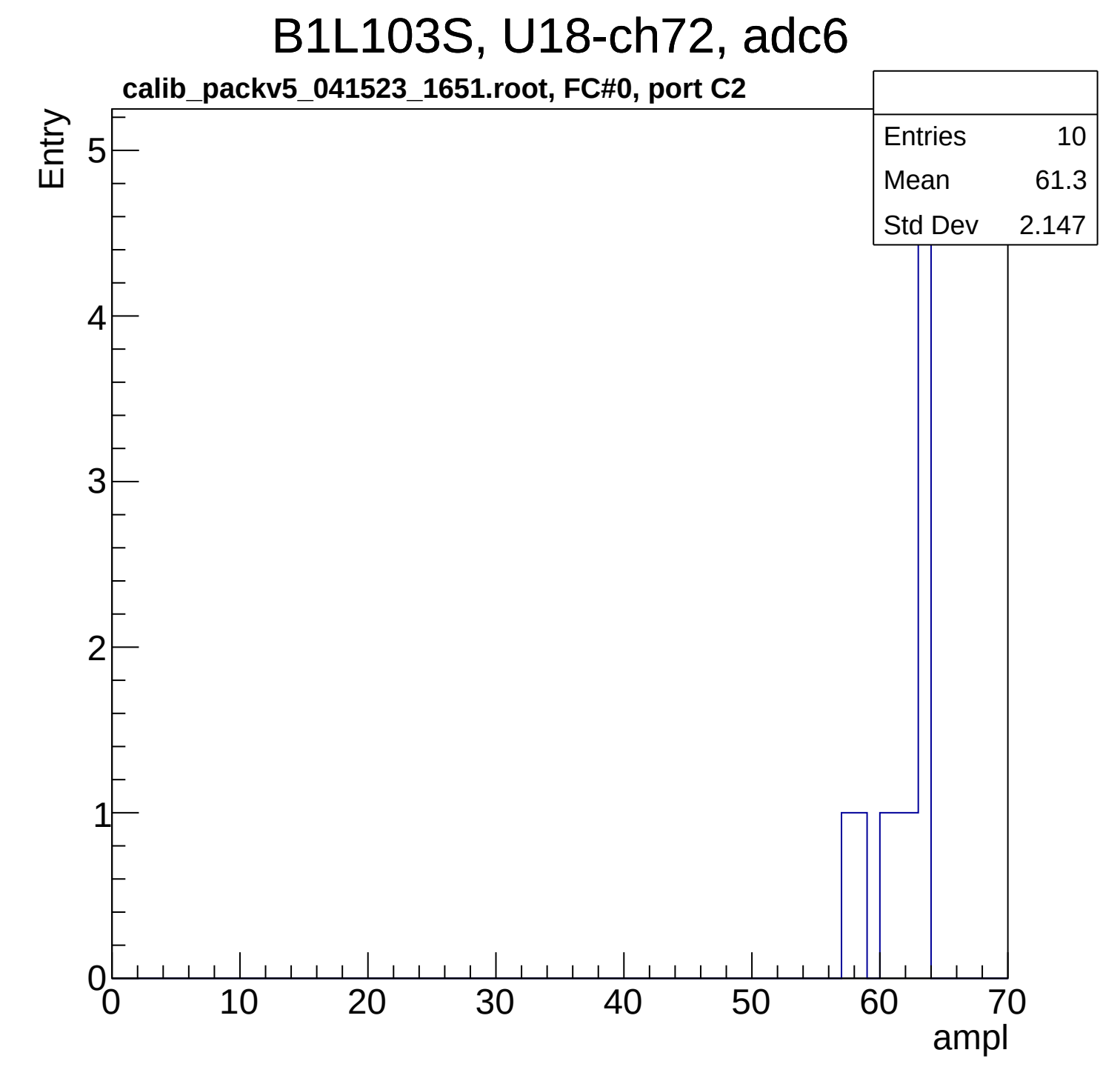
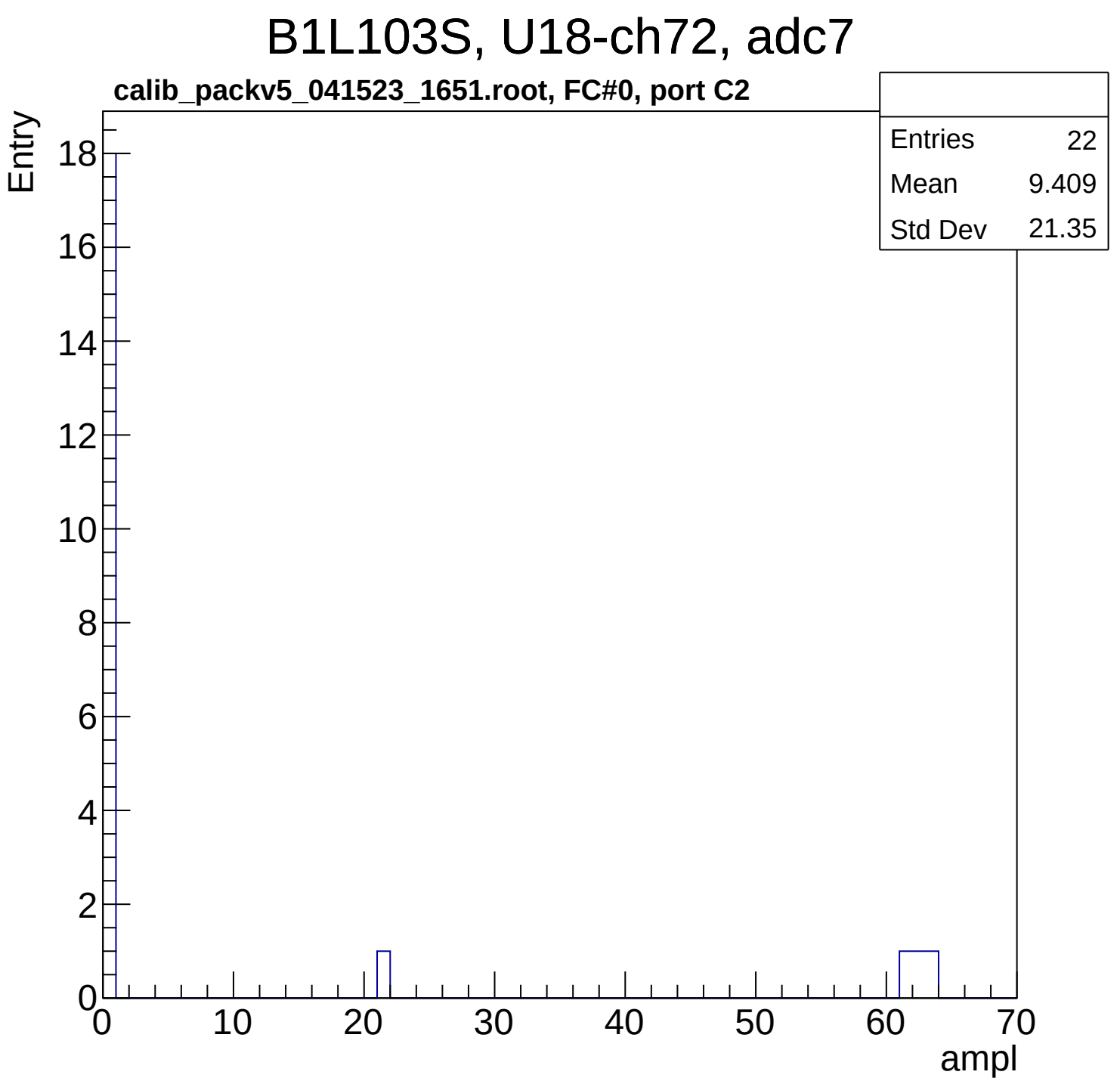
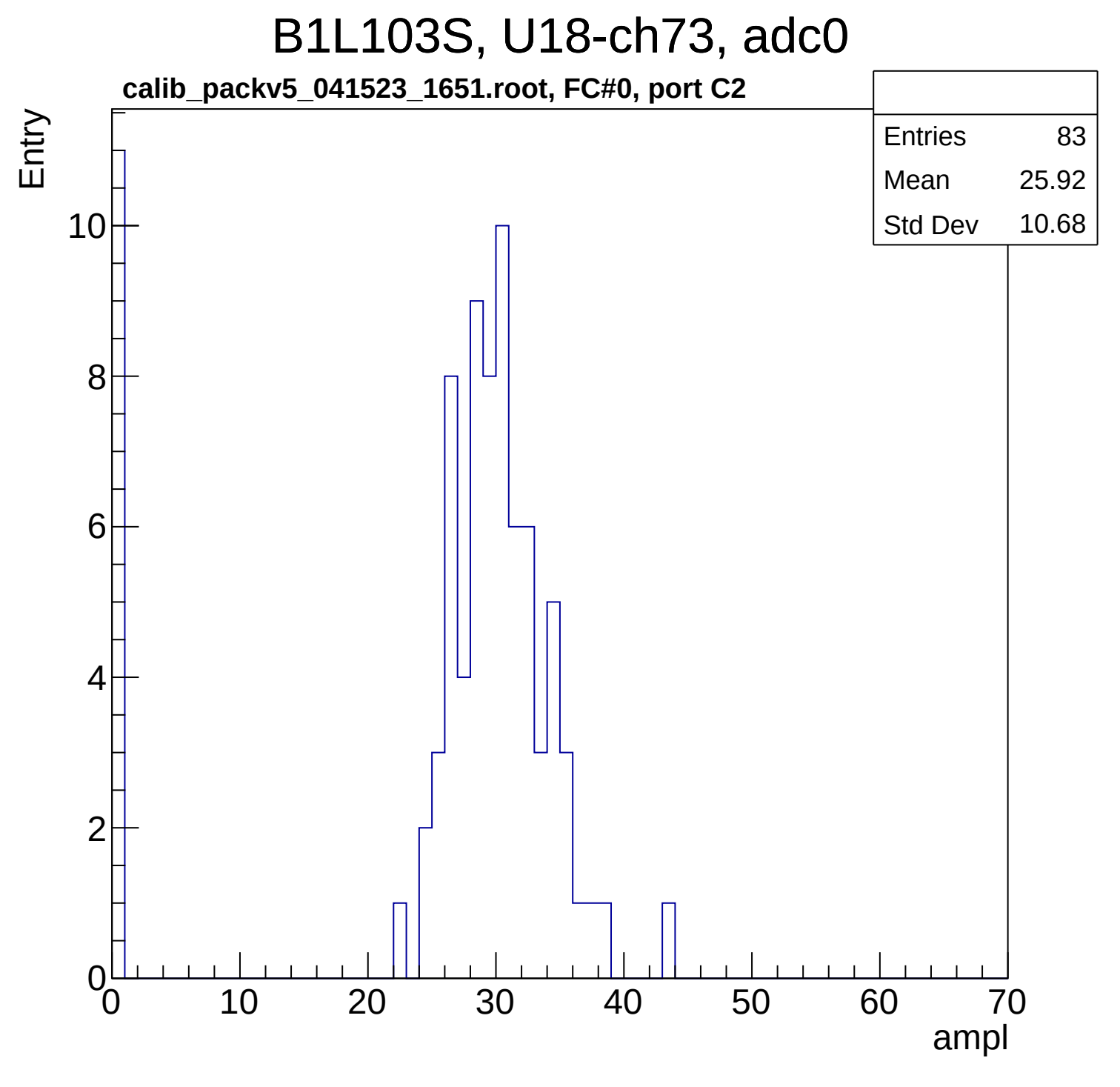
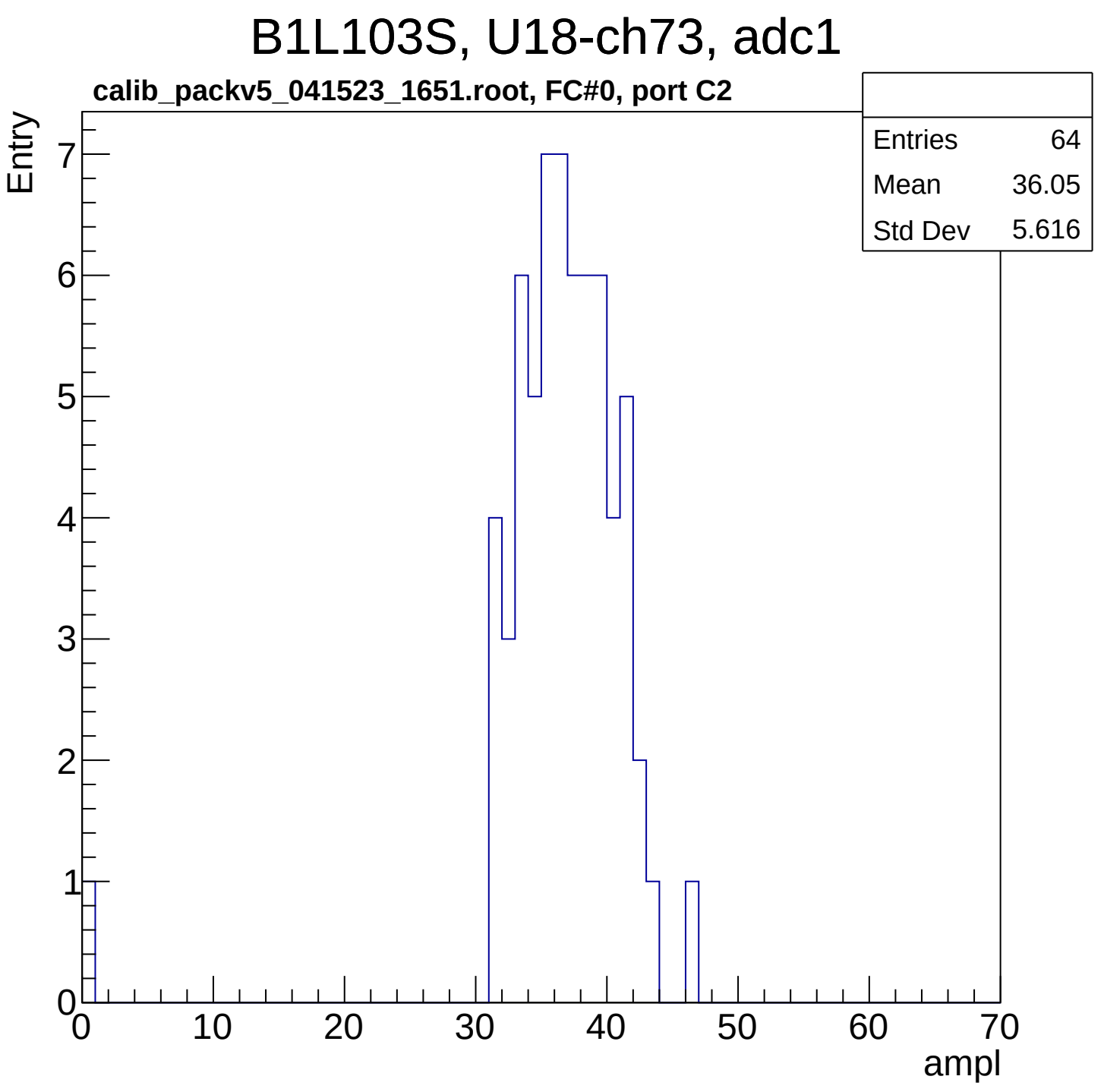
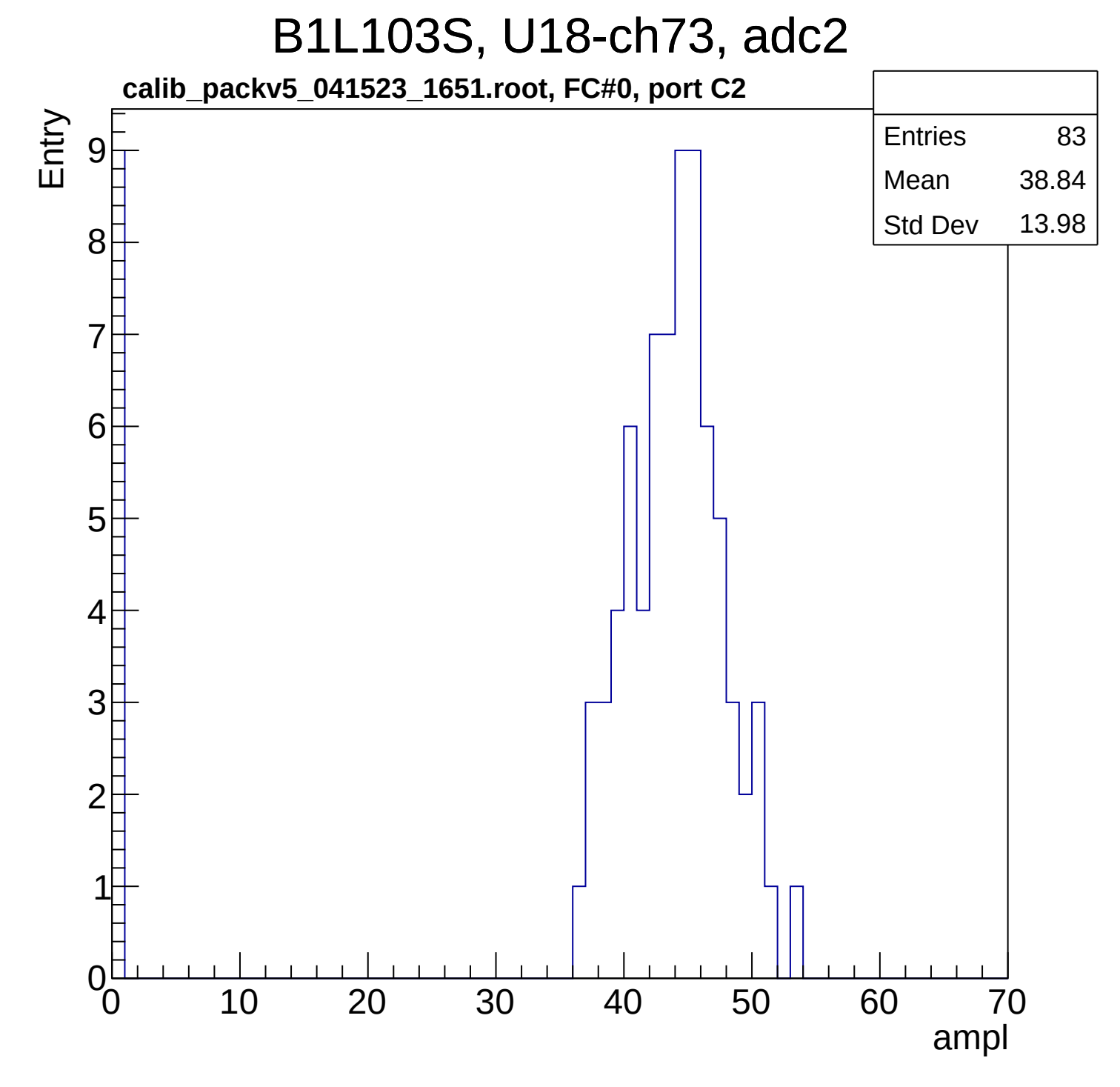
20
30
40
50
60
70

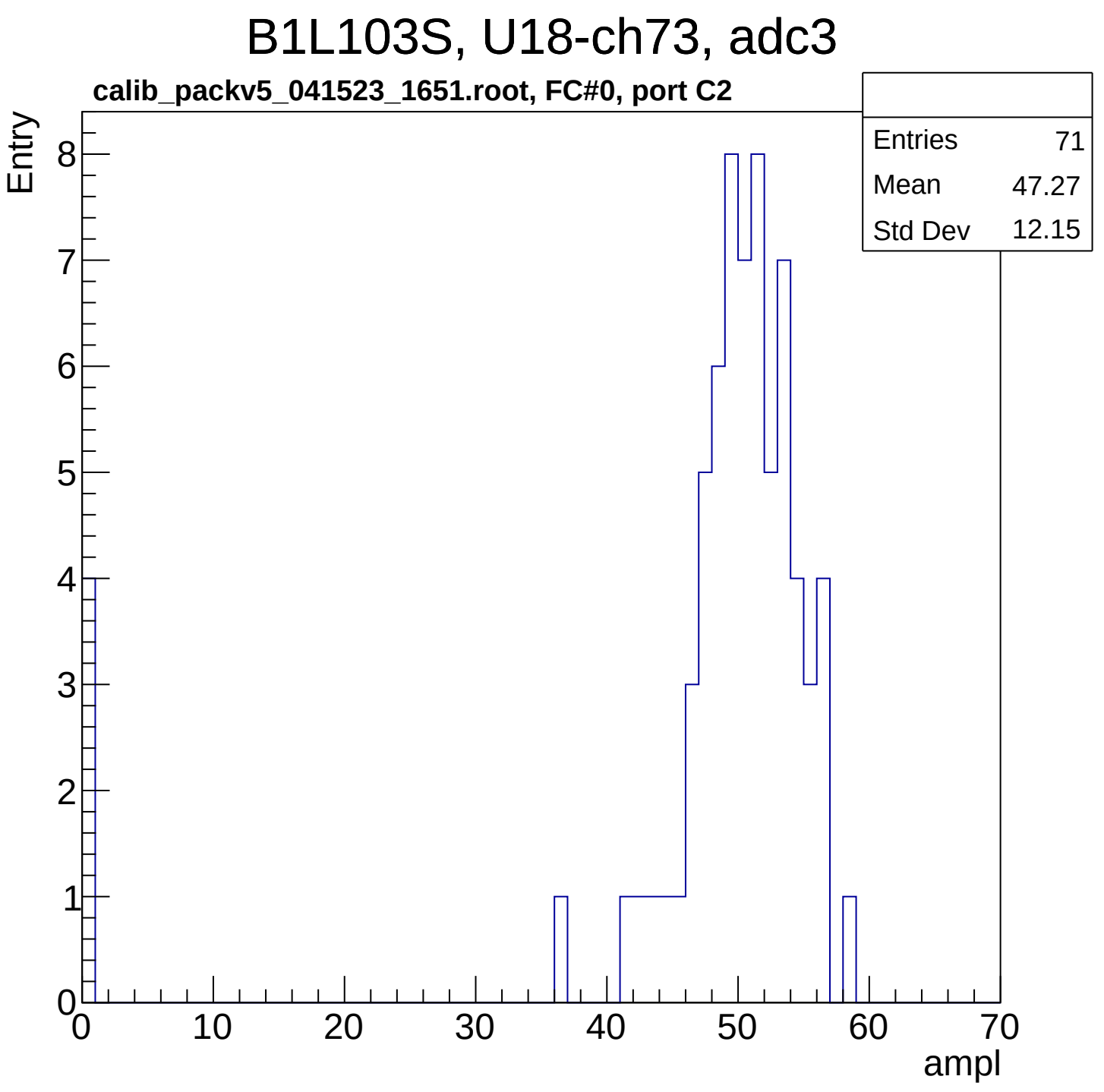

B1L103S, U18-ch72, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 61.3
Std Dev 2.147
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U18-ch72, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 9.409
Std Dev 21.35
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch73, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 25.92
Std Dev 10.68
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch73, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 36.05
Std Dev 5.616
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U18-ch73, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 38.84
Std Dev 13.98
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U18-ch73, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 47.27
Std Dev 12.15
Entry
ampl
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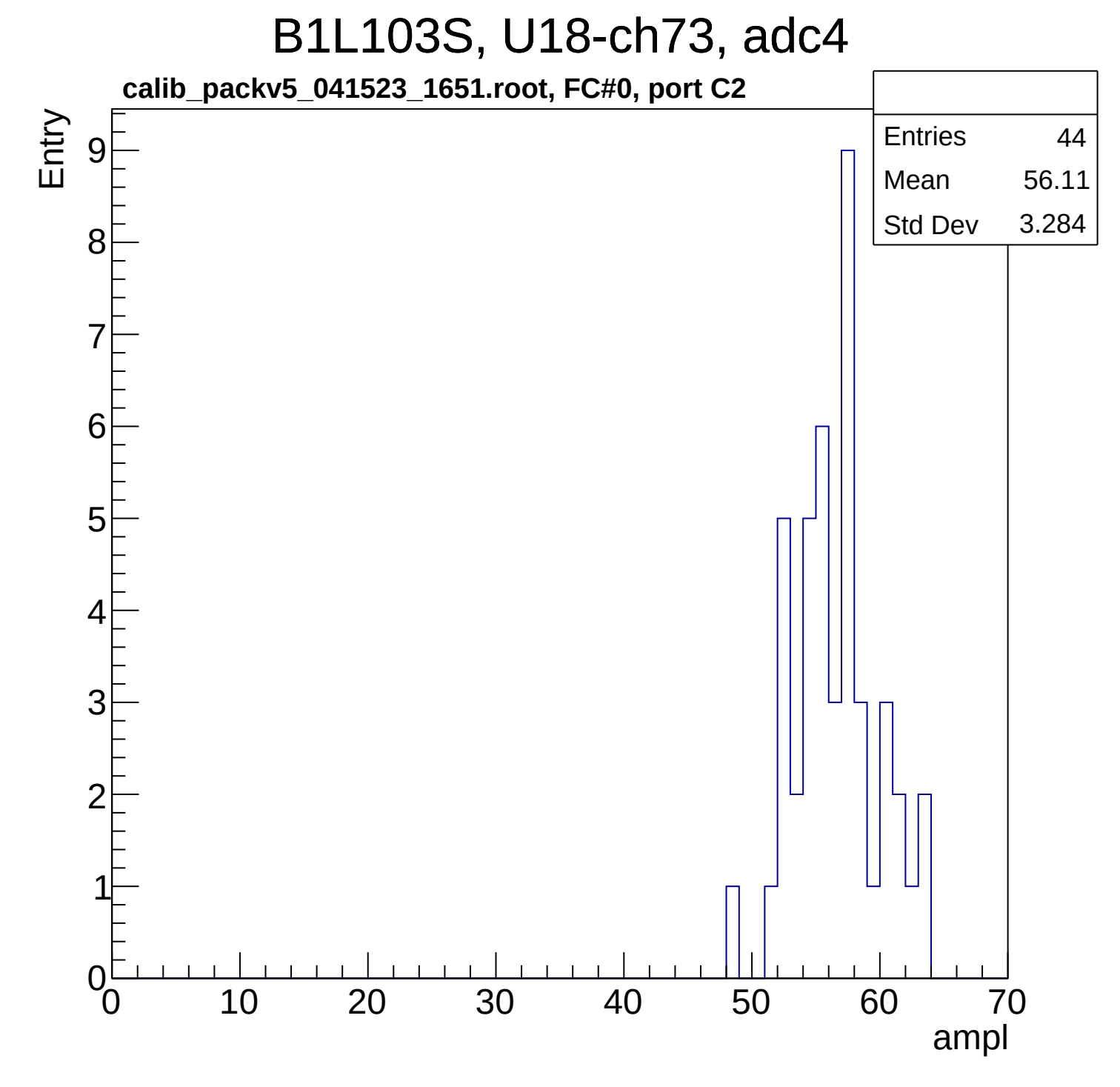
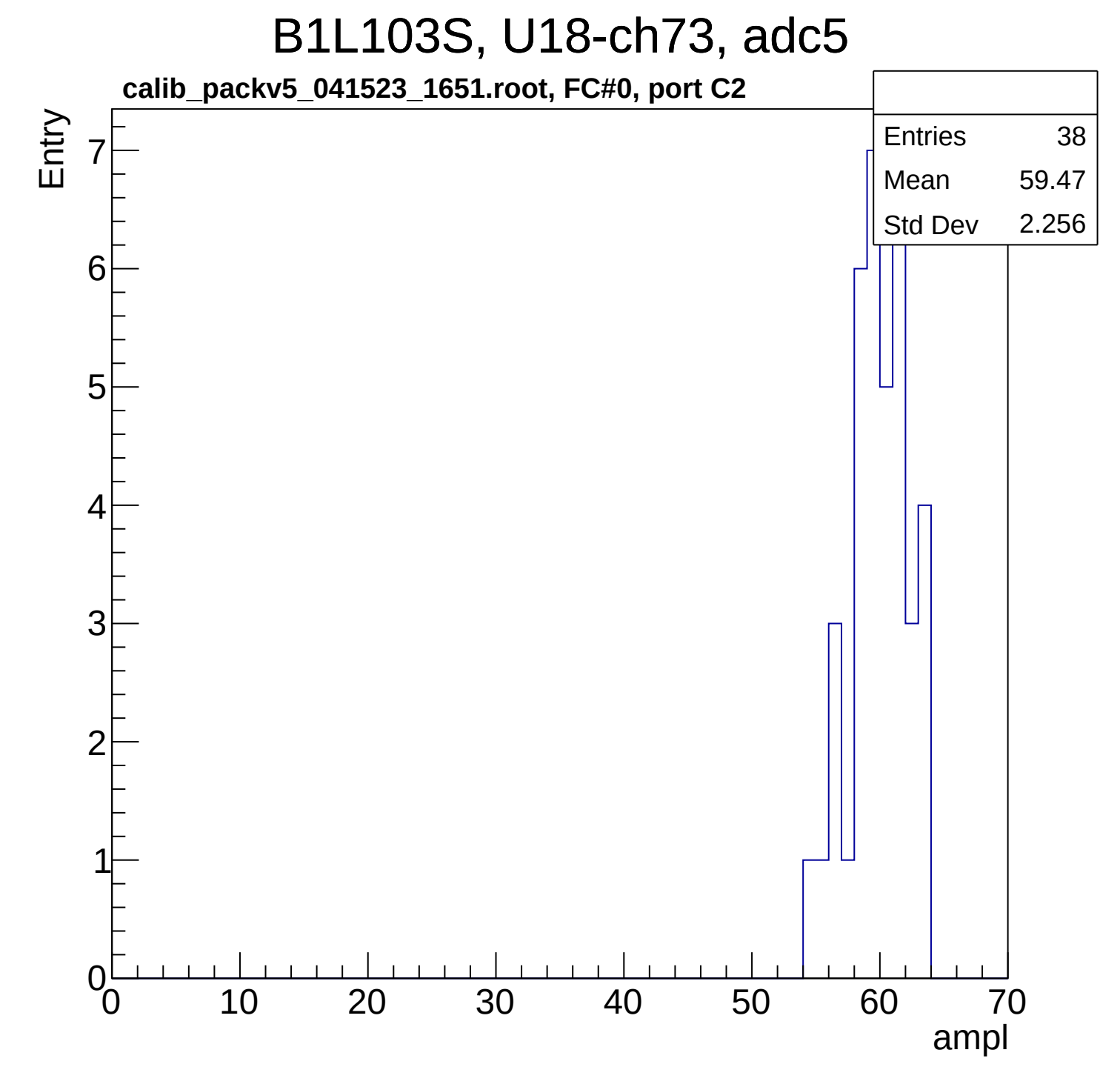
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch73, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 56.11
Std Dev 3.284
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U18-ch73, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 38
Mean 59.47
Std Dev 2.256
Entry
ampl
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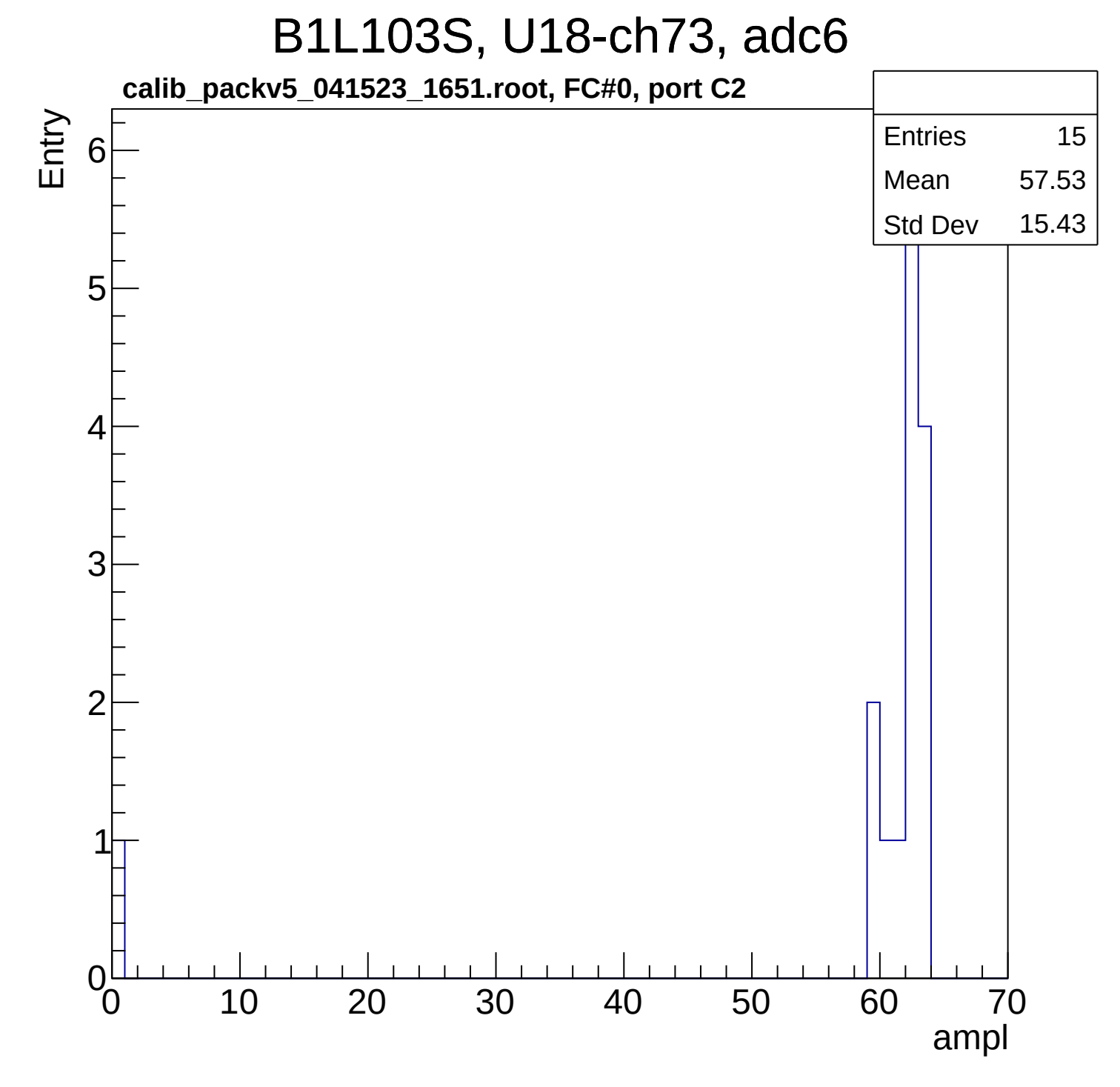
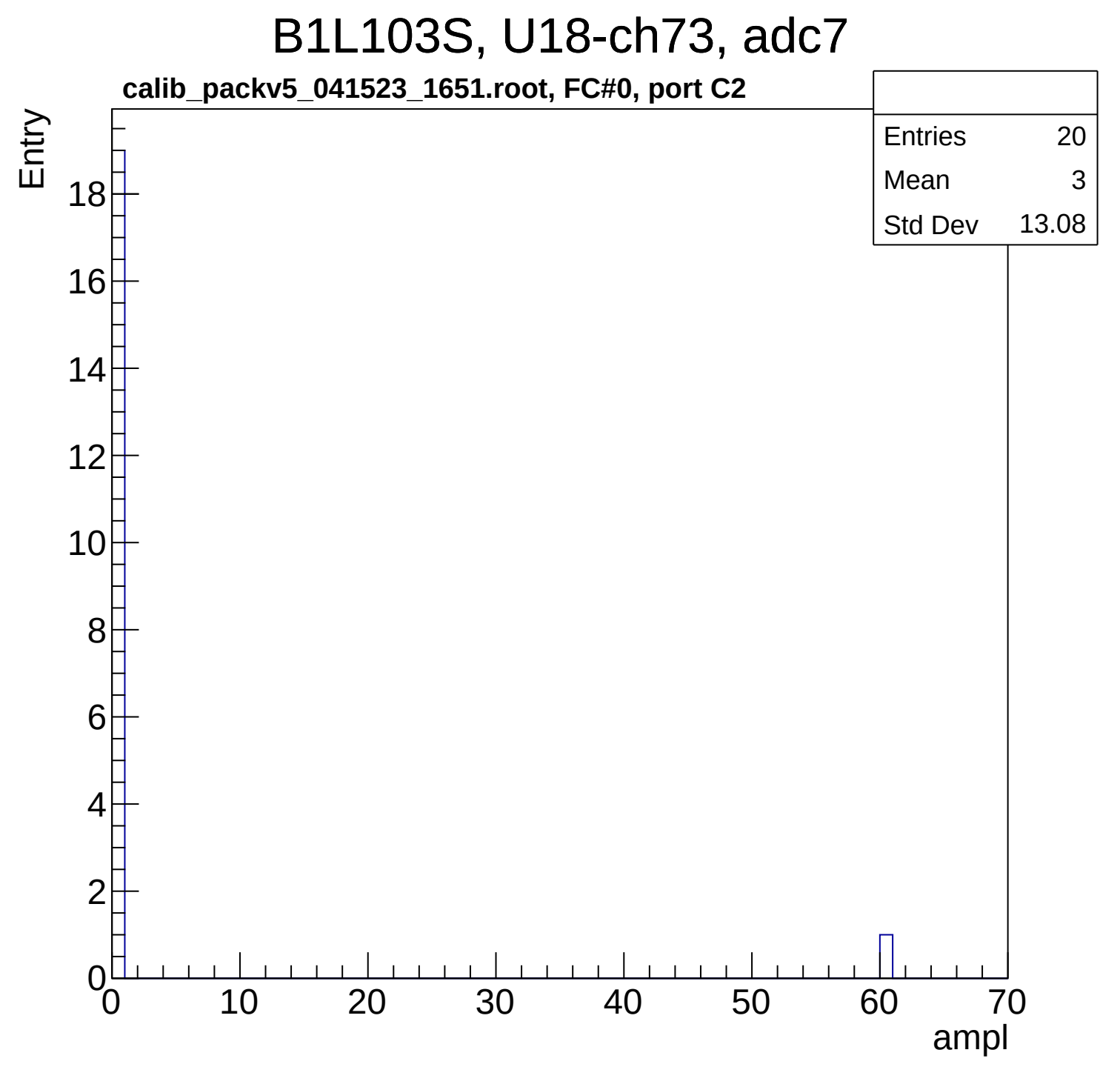
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U18-ch73, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 15
Mean 57.53
Std Dev 15.43
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U18-ch73, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3
Std Dev 13.08
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
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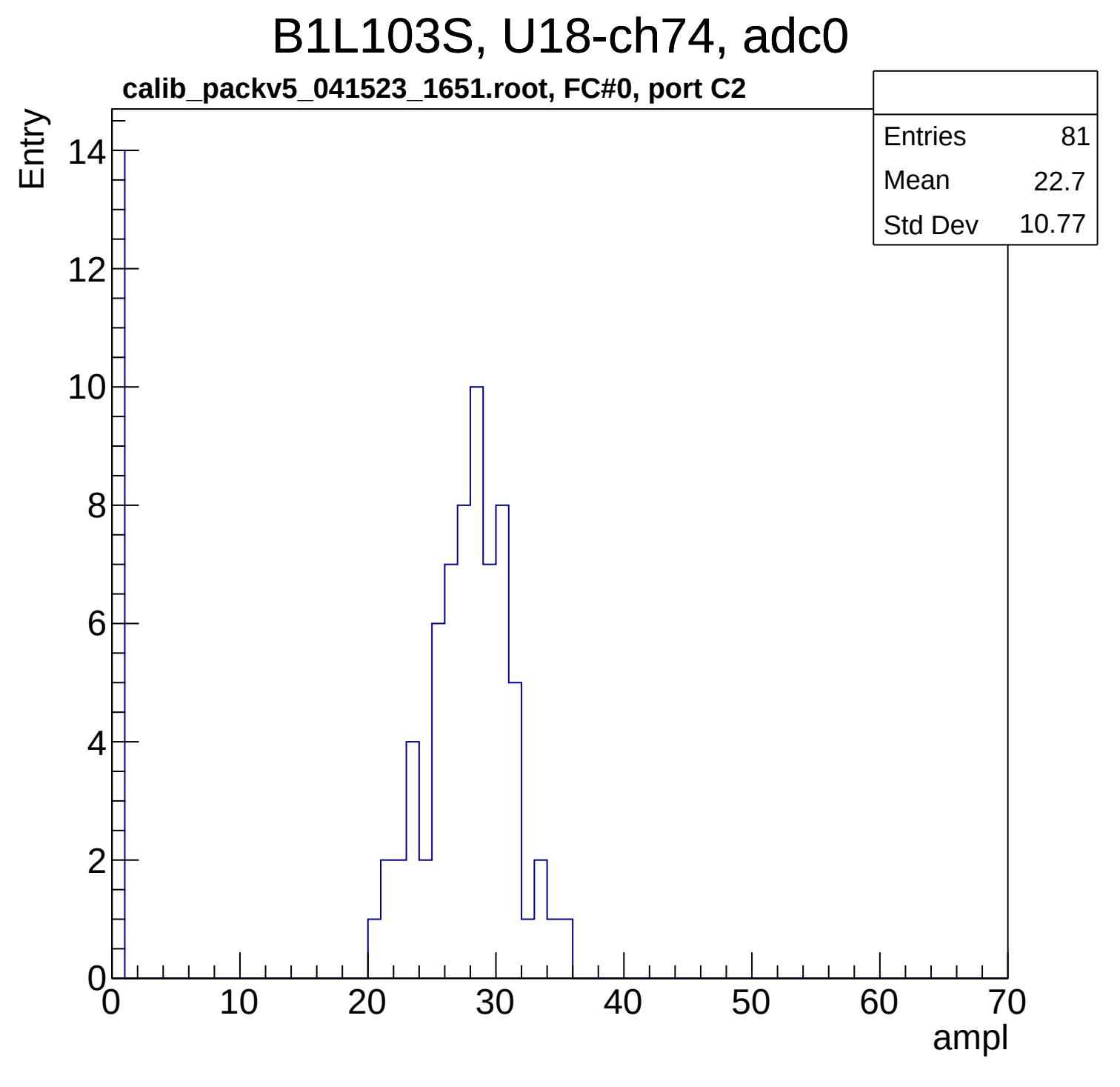
50
60
70
ampl


B1L103S, U18-ch74, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 22.7
Std Dev 10.77
Entry
ampl
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2
4
6
8
10
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0
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40
50
60
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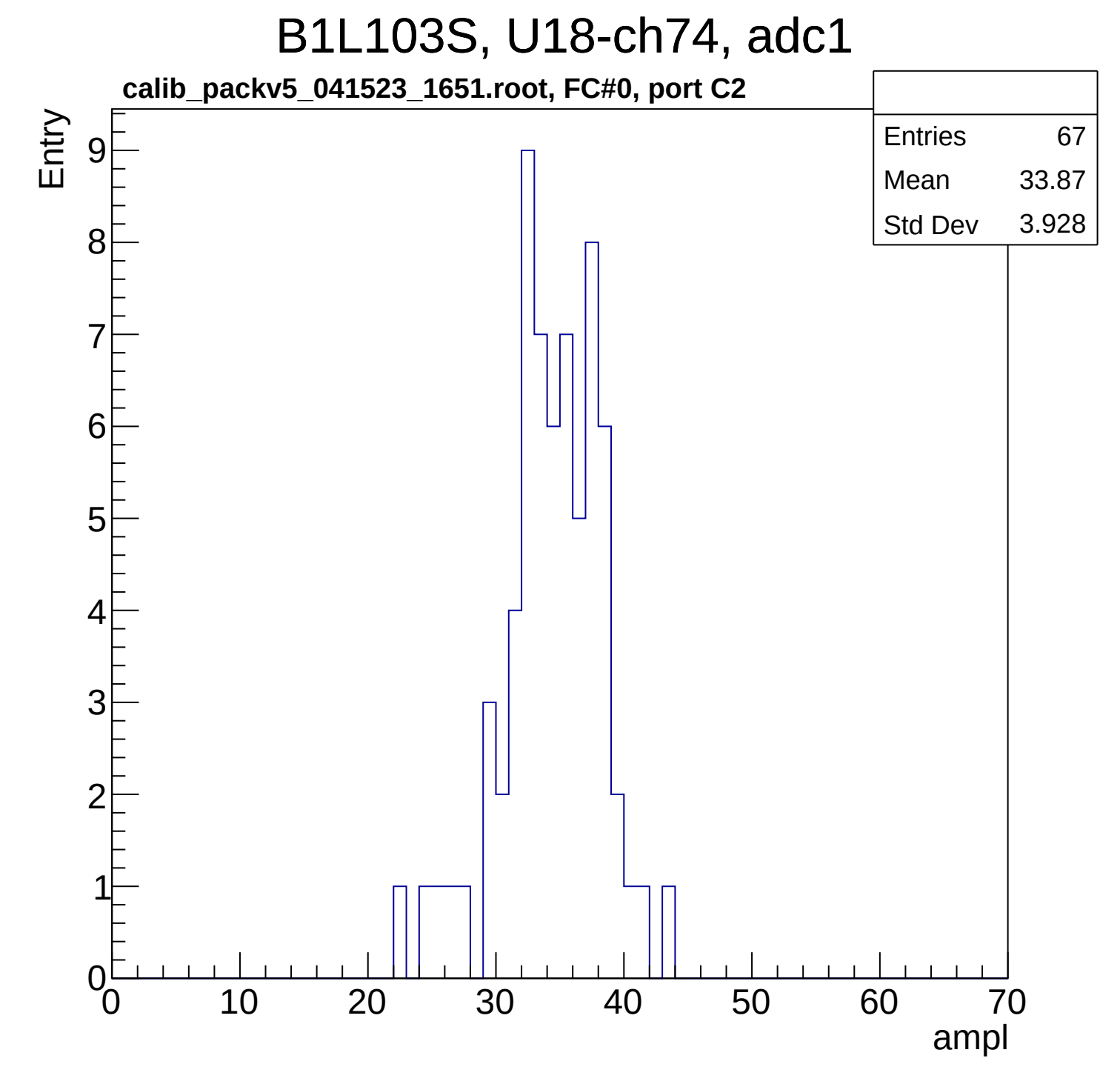
B1L103S, U18-ch74, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 33.87
Std Dev 3.928
Entry
ampl
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2
3
4
5
6
7
8
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0
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20
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60
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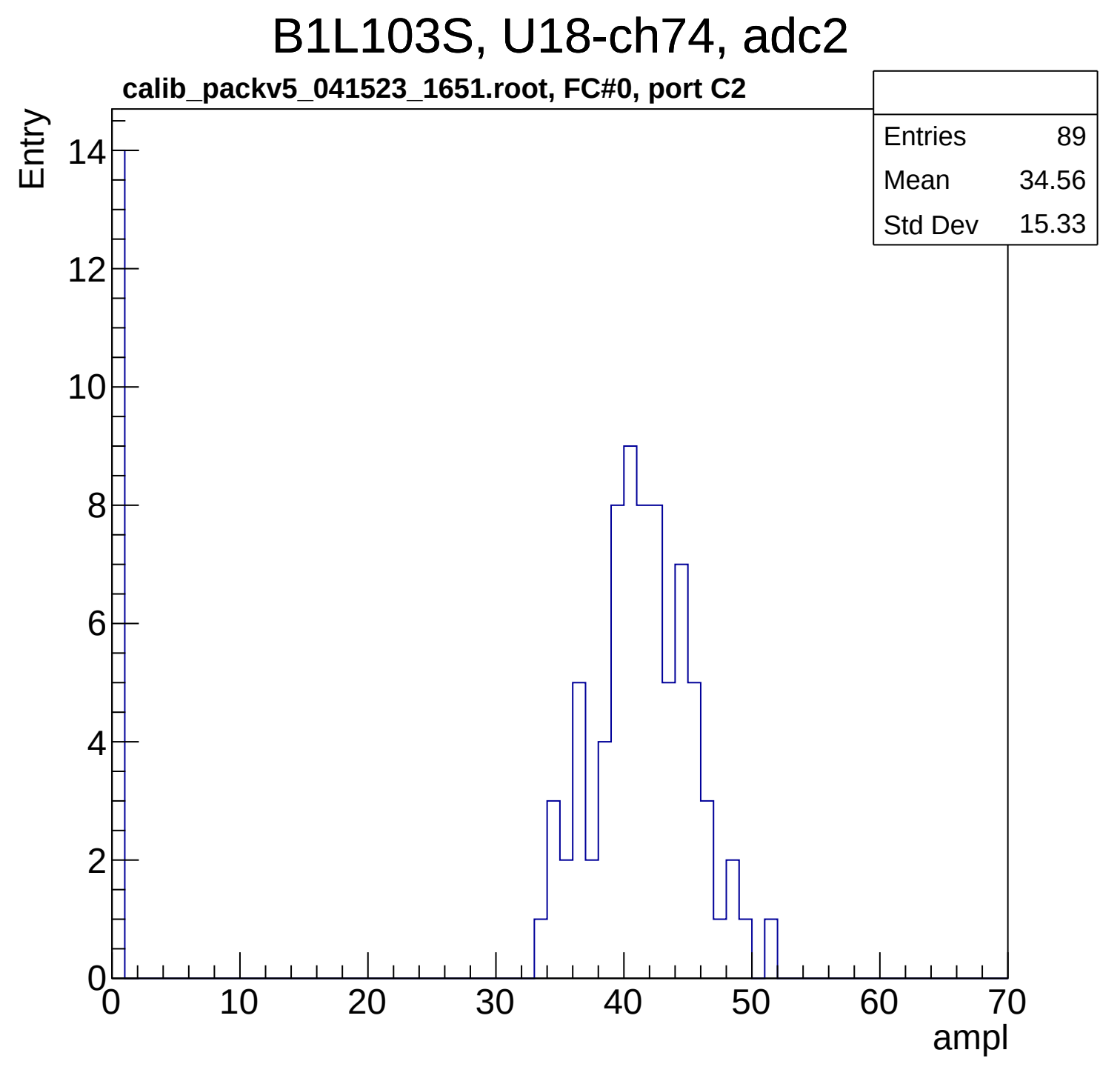
B1L103S, U18-ch74, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 89
Mean 34.56
Std Dev 15.33
Entry
ampl
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2
4
6
8
10
12
14
0
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20
30
40
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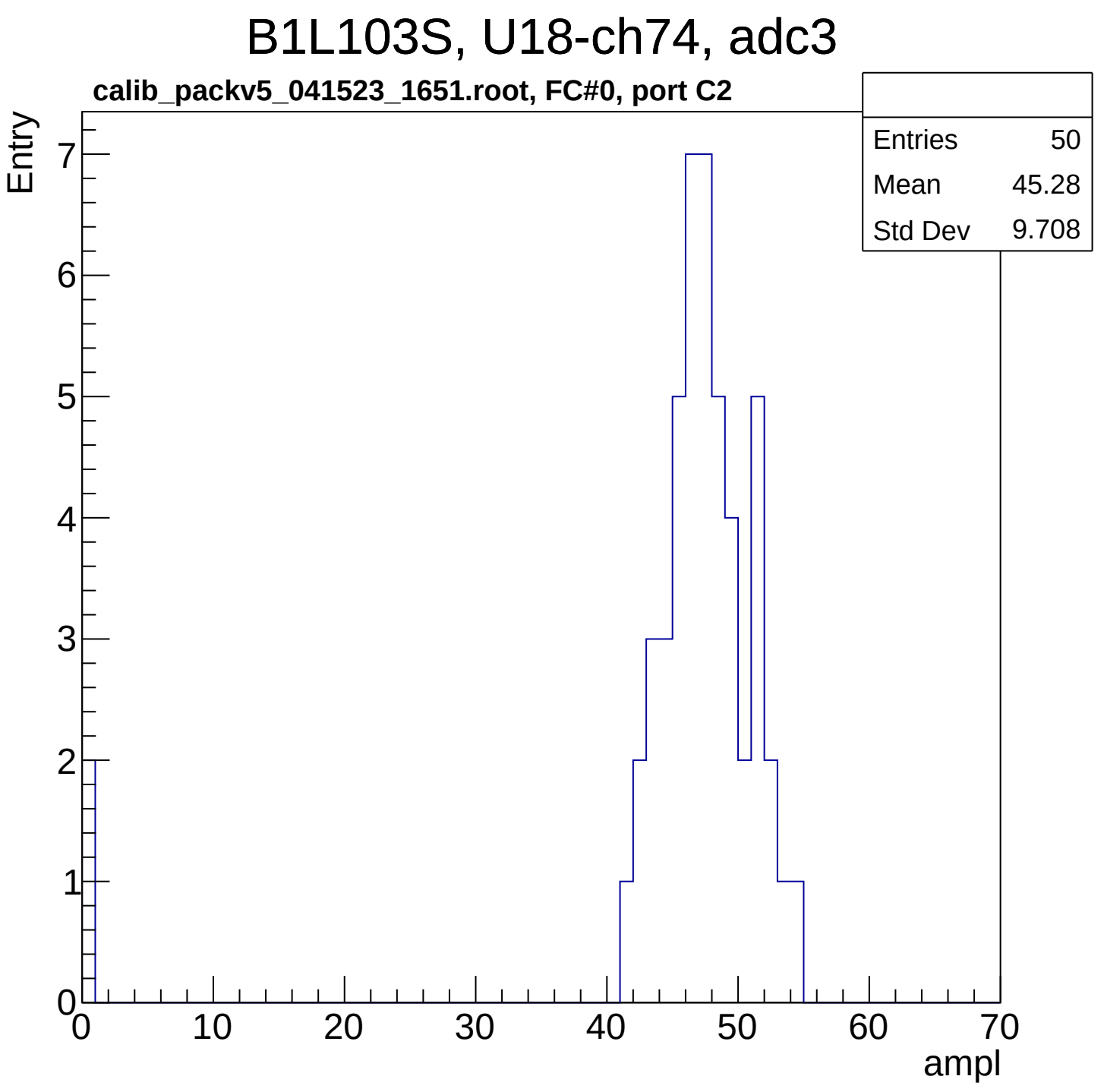
60
70


B1L103S, U18-ch74, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 45.28
Std Dev 9.708
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
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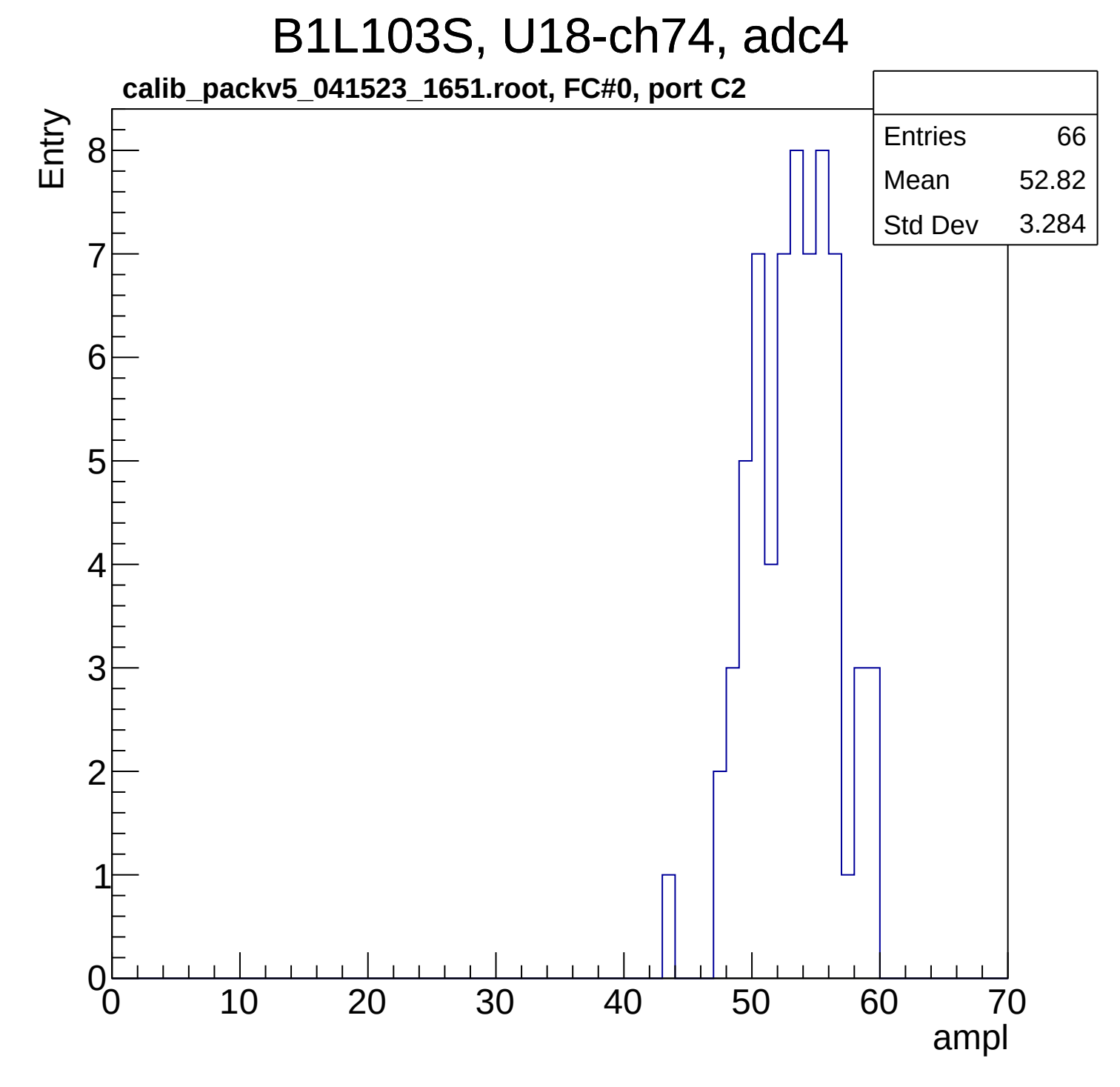
40
50
60
70


B1L103S, U18-ch74, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 52.82
Std Dev 3.284
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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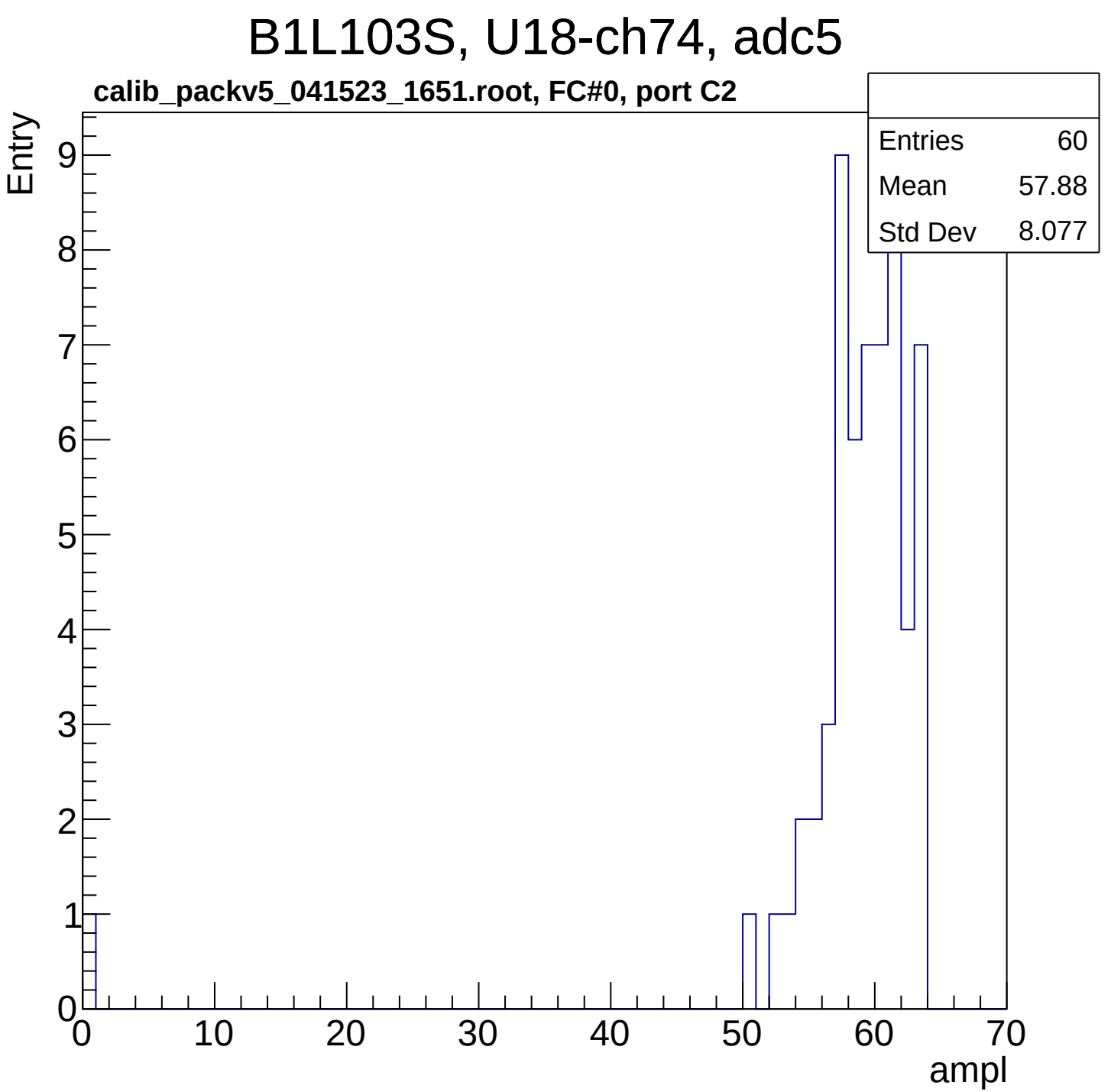
50
60
70


B1L103S, U18-ch74, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 57.88
Std Dev 8.077
Entry
ampl
0
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2
3
4
5
6
7
8
9
0
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20
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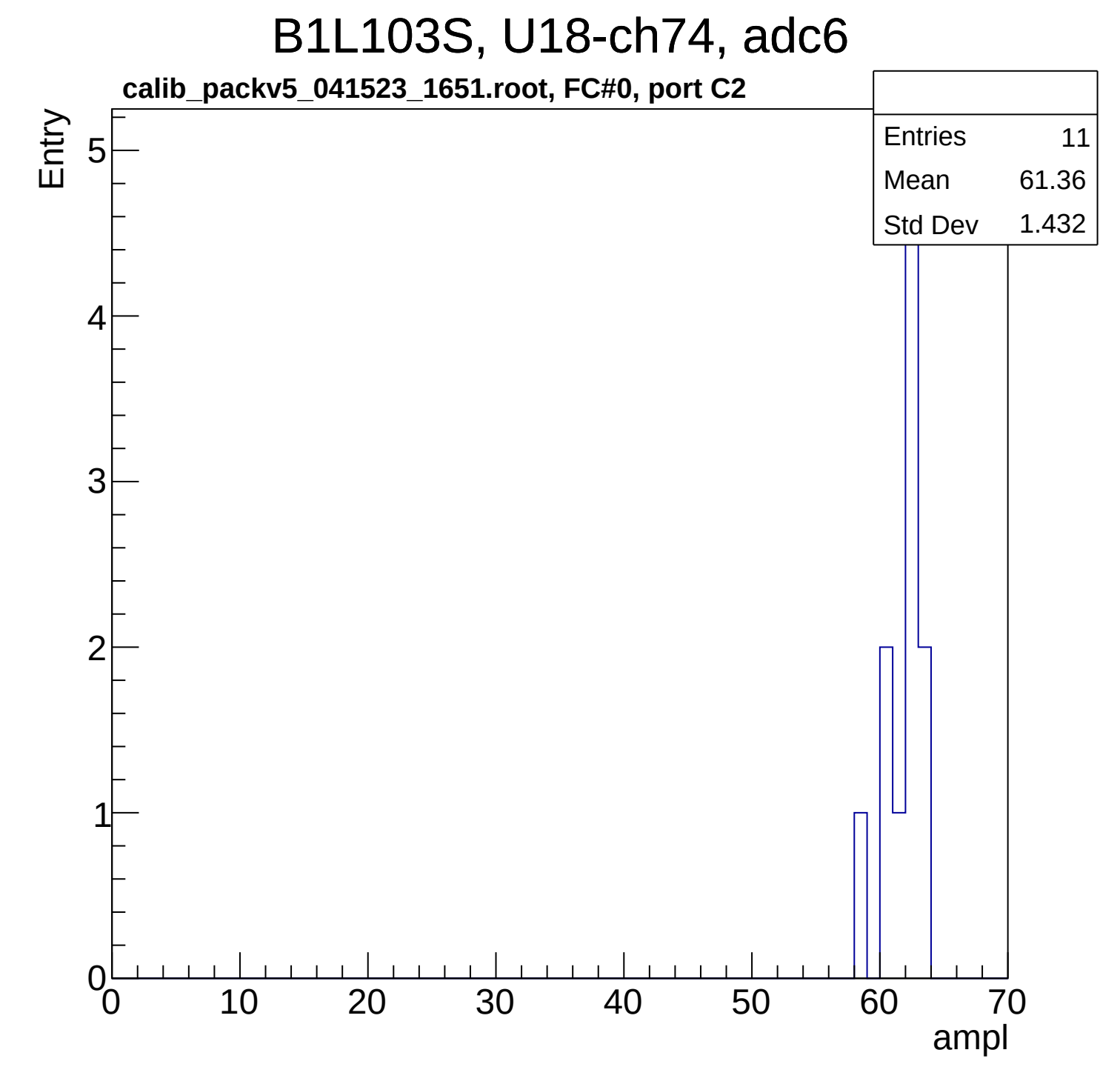
40
50
60
70


B1L103S, U18-ch74, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 61.36
Std Dev 1.432
Entry
ampl
0
1
2
3
4
5
0
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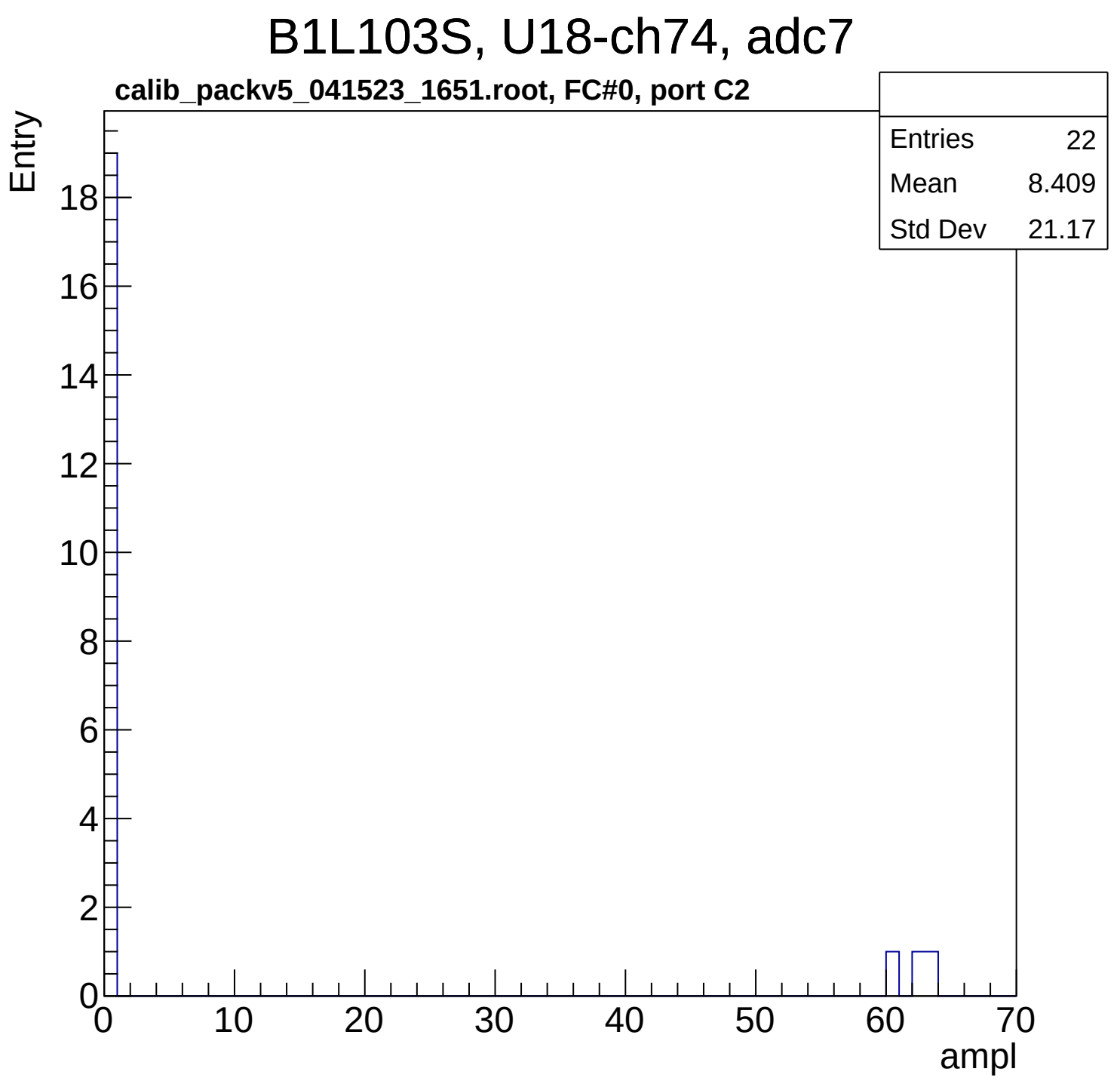
20
30
40
50
60
70


B1L103S, U18-ch74, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 8.409
Std Dev 21.17
Entry
0
2
4
6
8
10
12
14
16
18
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10
20
30
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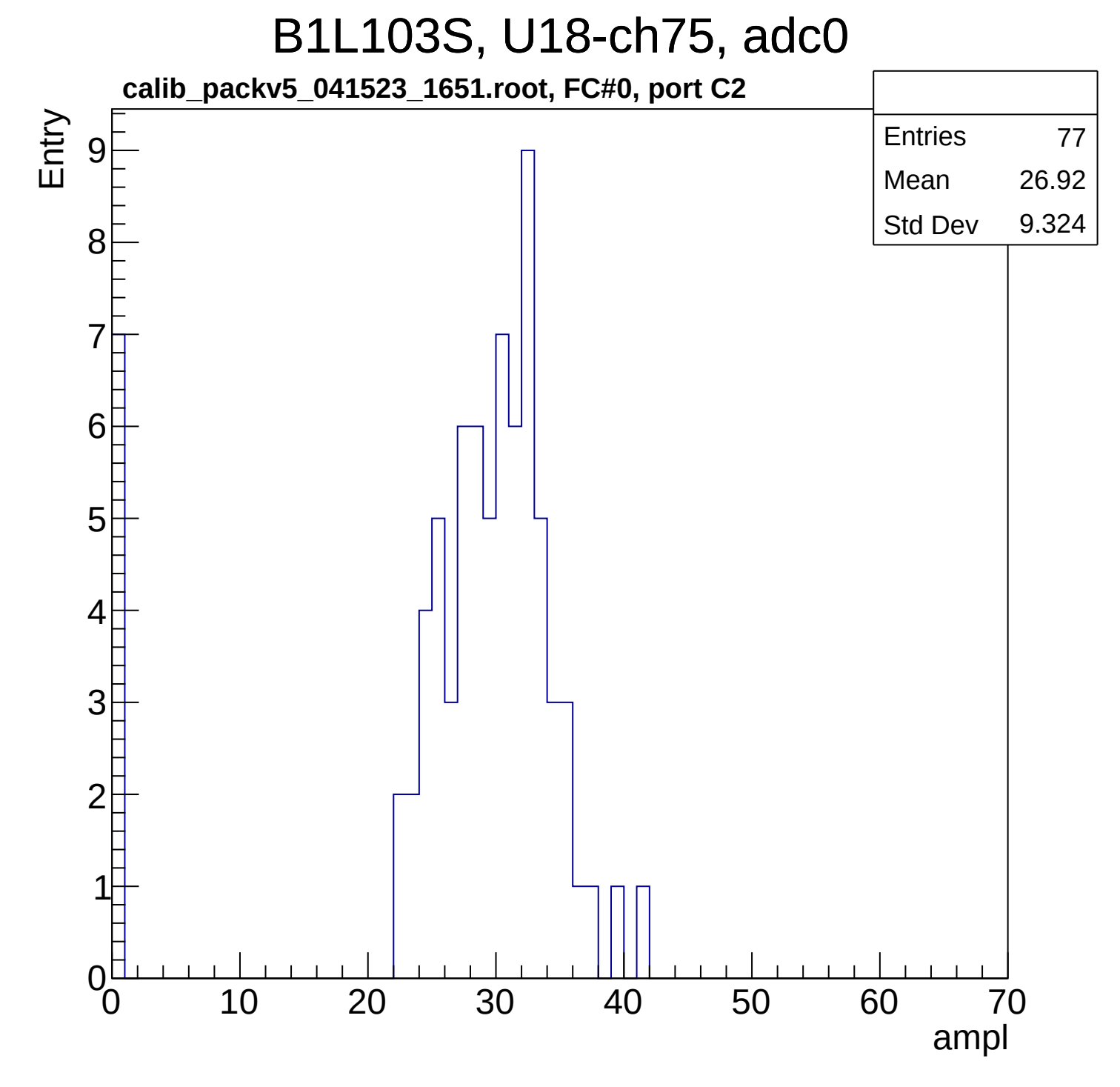
50
60
70
ampl


B1L103S, U18-ch75, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 26.92
Std Dev 9.324
Entry
ampl
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2
3
4
5
6
7
8
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0
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40
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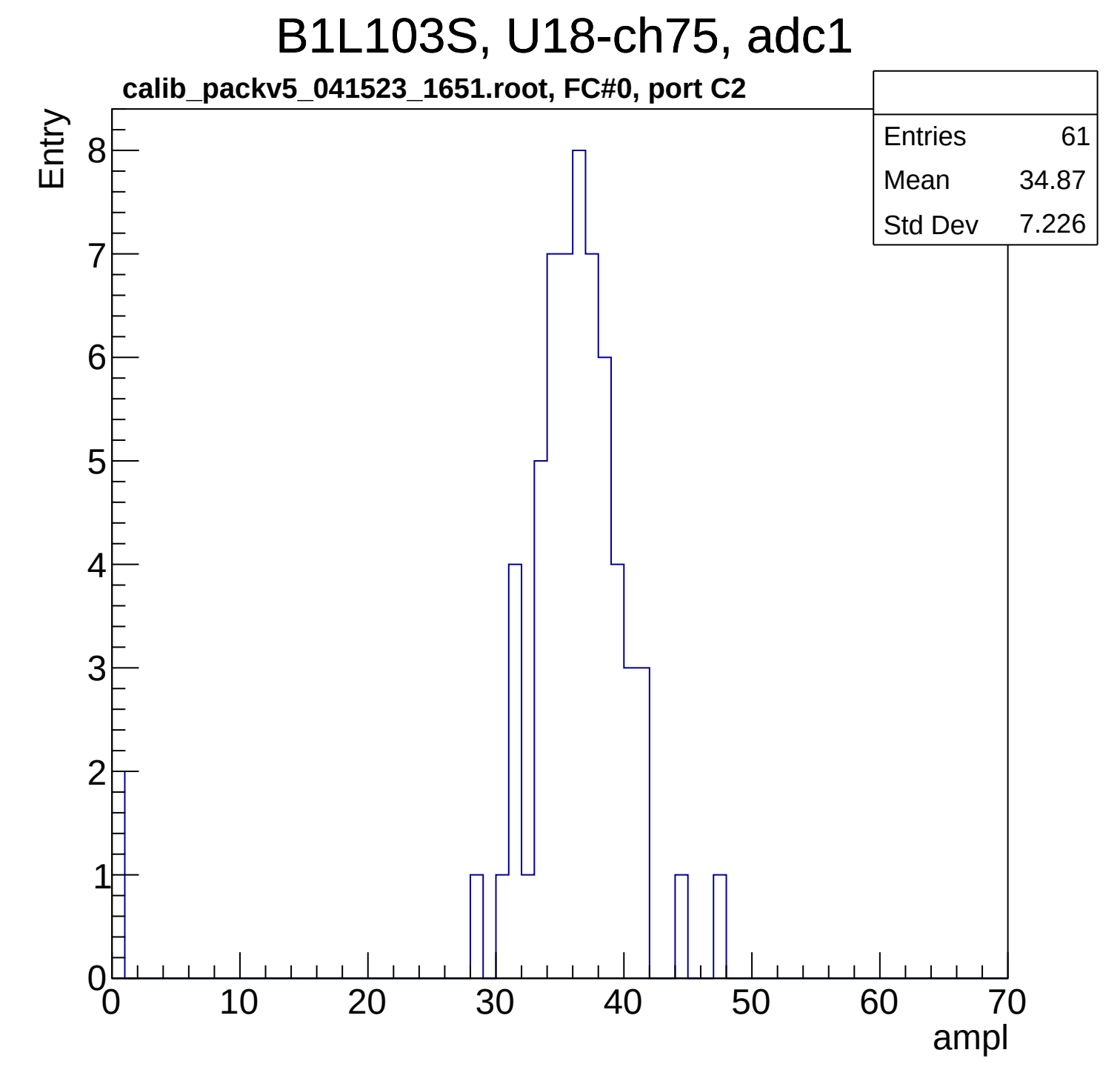
60
70


B1L103S, U18-ch75, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 34.87
Std Dev 7.226
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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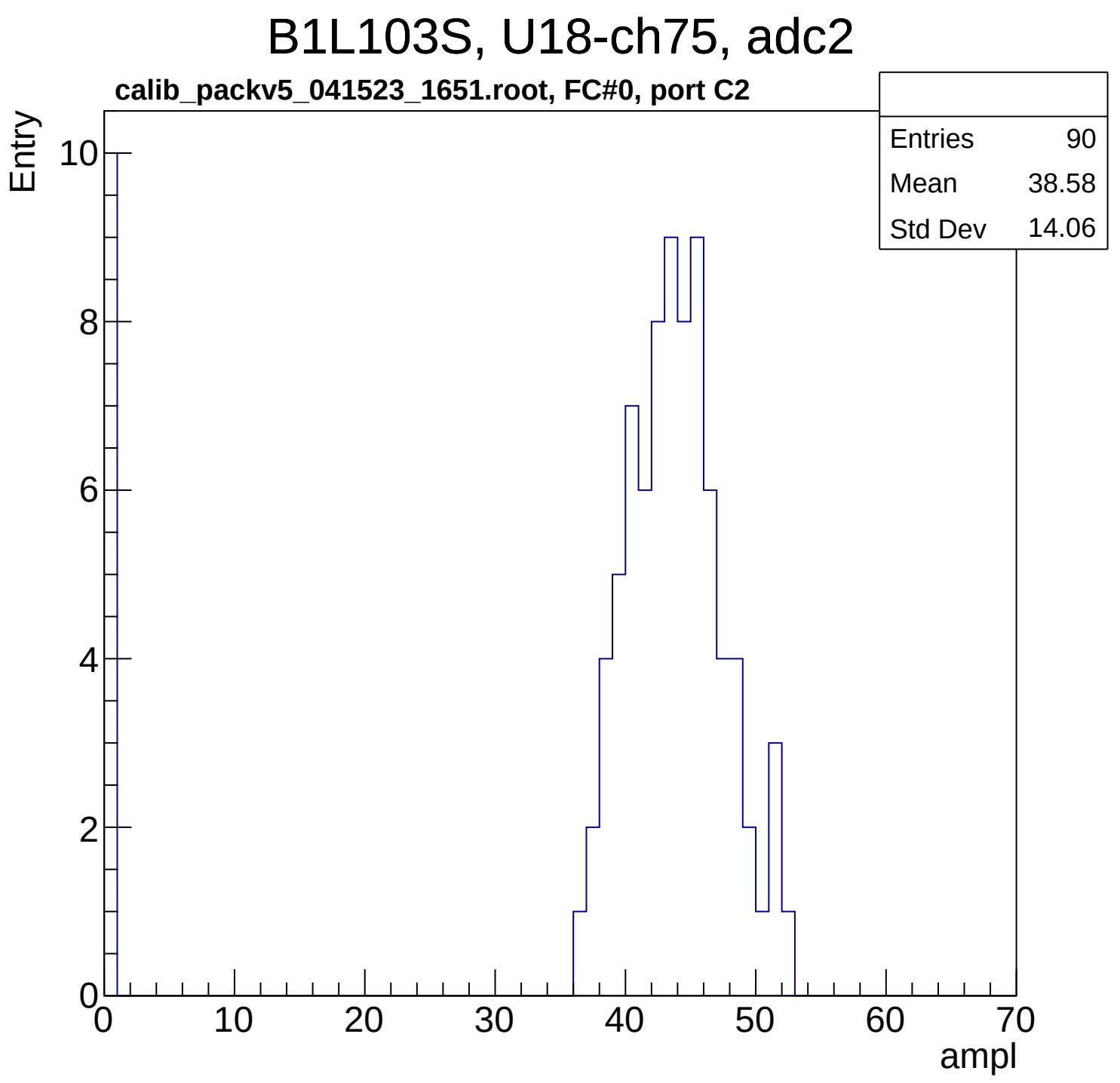
40
50
60
70


B1L103S, U18-ch75, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 90
Mean 38.58
Std Dev 14.06
Entry
ampl
0
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4
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8
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40
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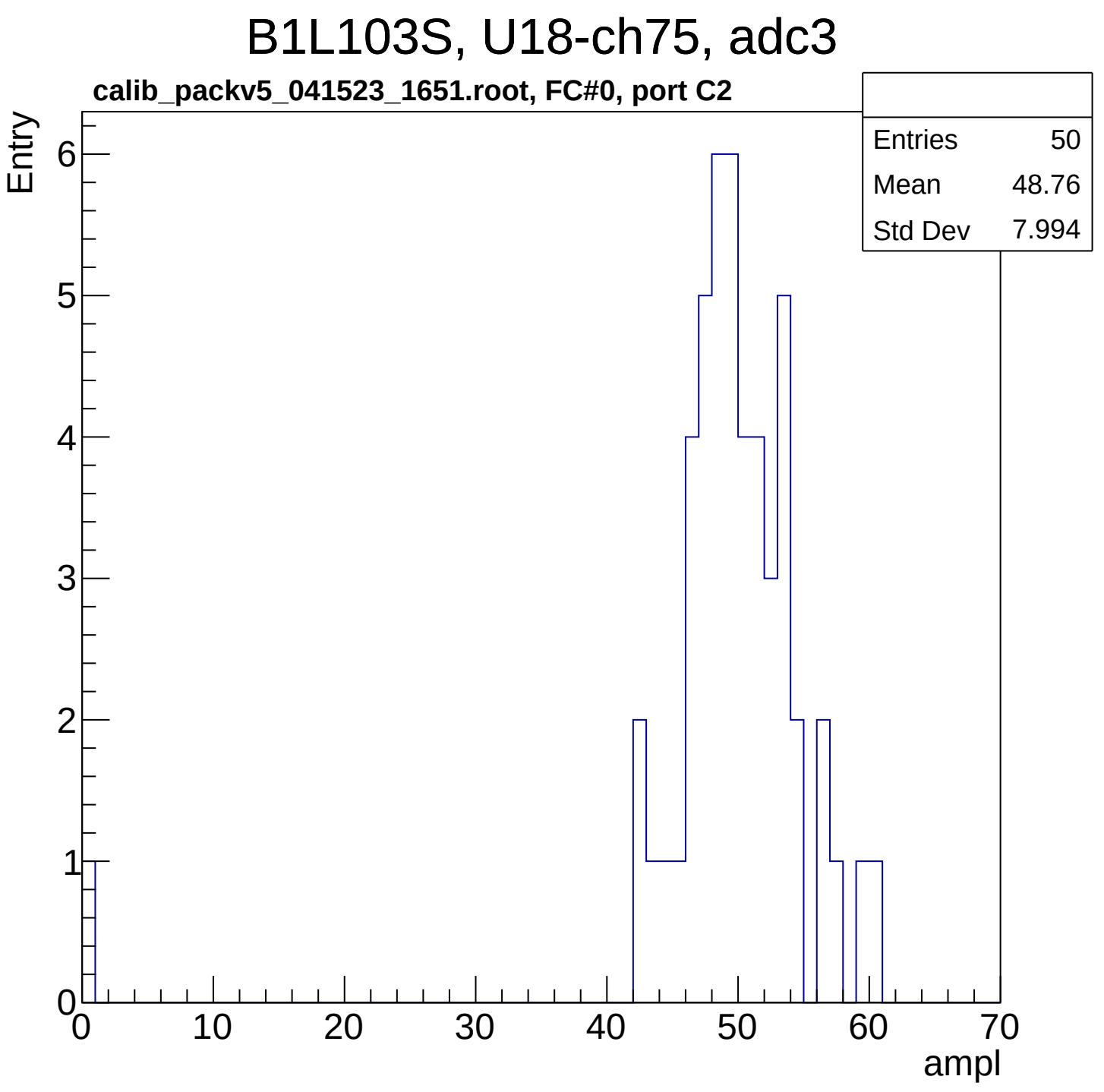
60
70


B1L103S, U18-ch75, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 48.76
Std Dev 7.994
Entry
ampl
0
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2
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4
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60
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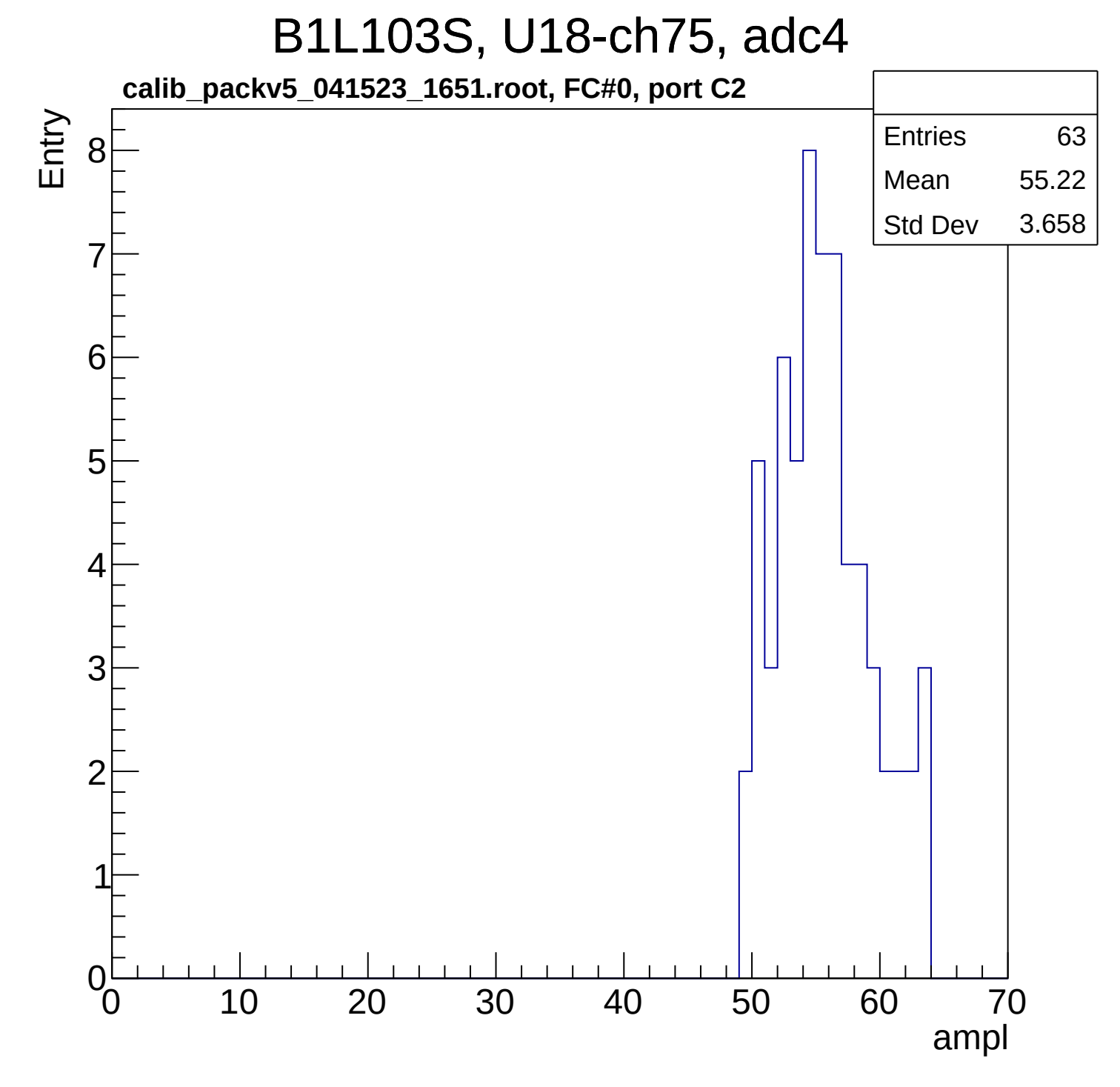
B1L103S, U18-ch75, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 55.22
Std Dev 3.658
Entry
ampl
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1
2
3
4
5
6
7
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0
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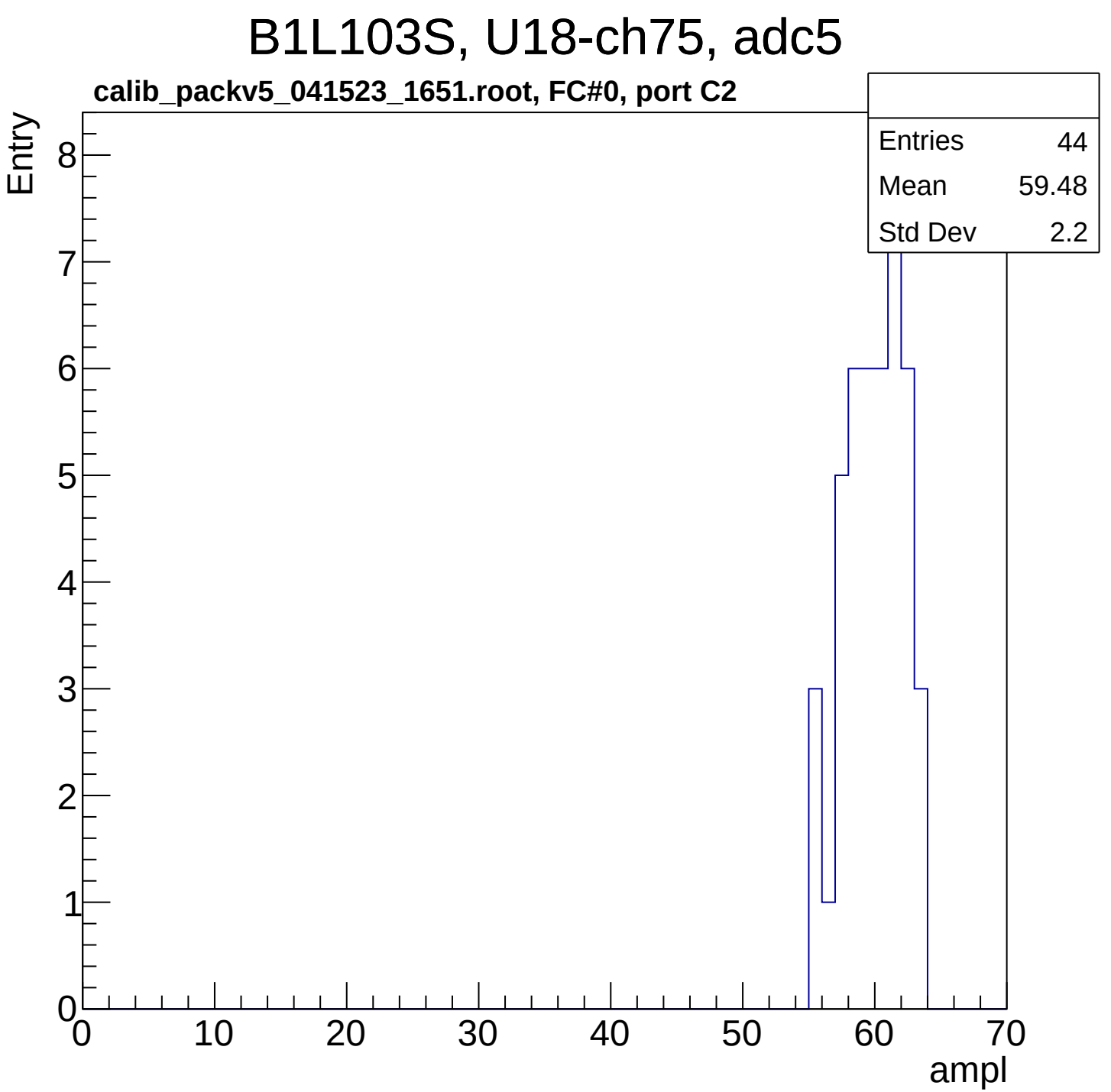
60
70


B1L103S, U18-ch75, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 59.48
Std Dev 2.2
Entry
ampl
0
1
2
3
4
5
6
7
8
0
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40
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60
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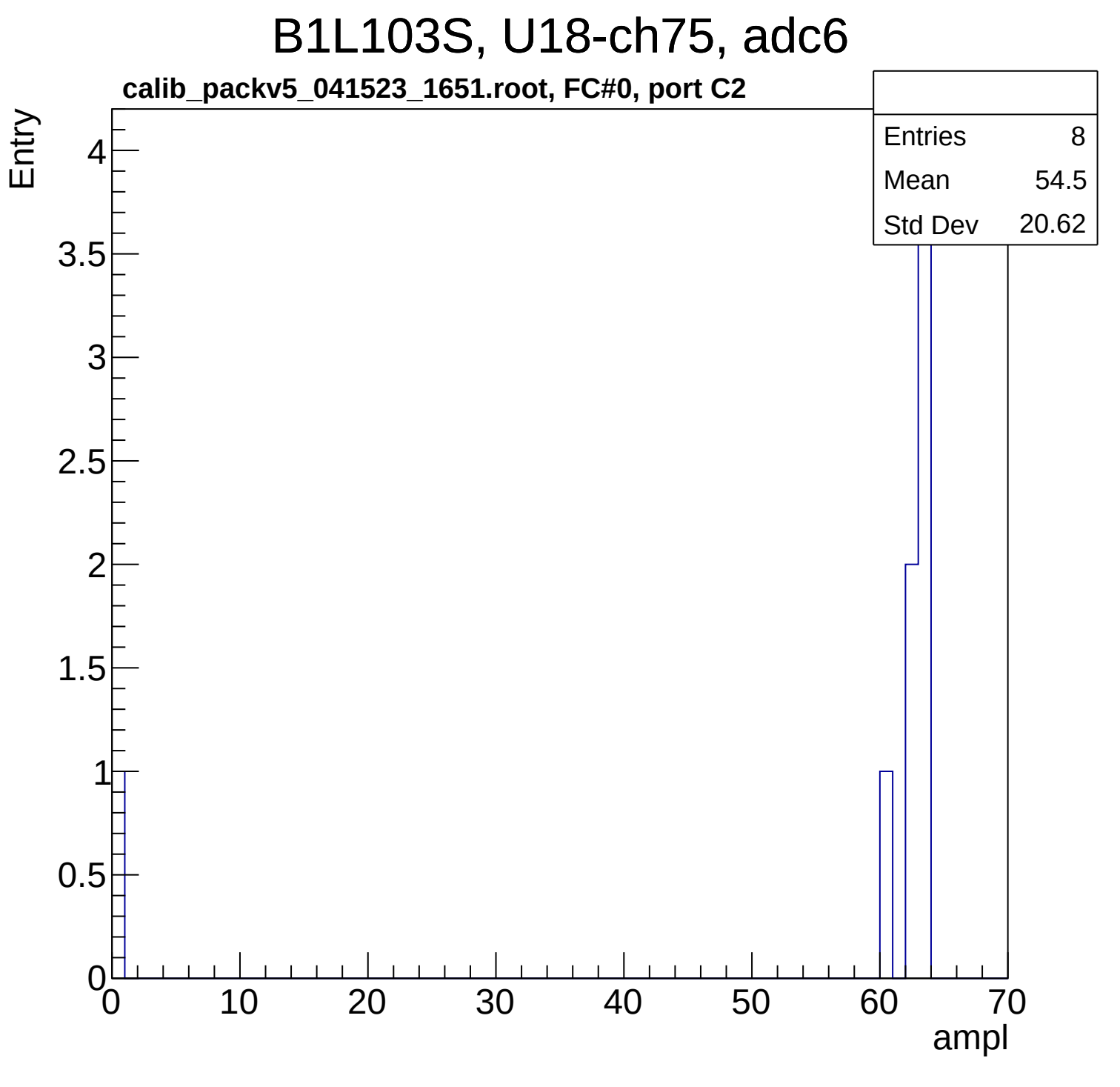
B1L103S, U18-ch75, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 54.5
Std Dev 20.62
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
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20
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40
50
60
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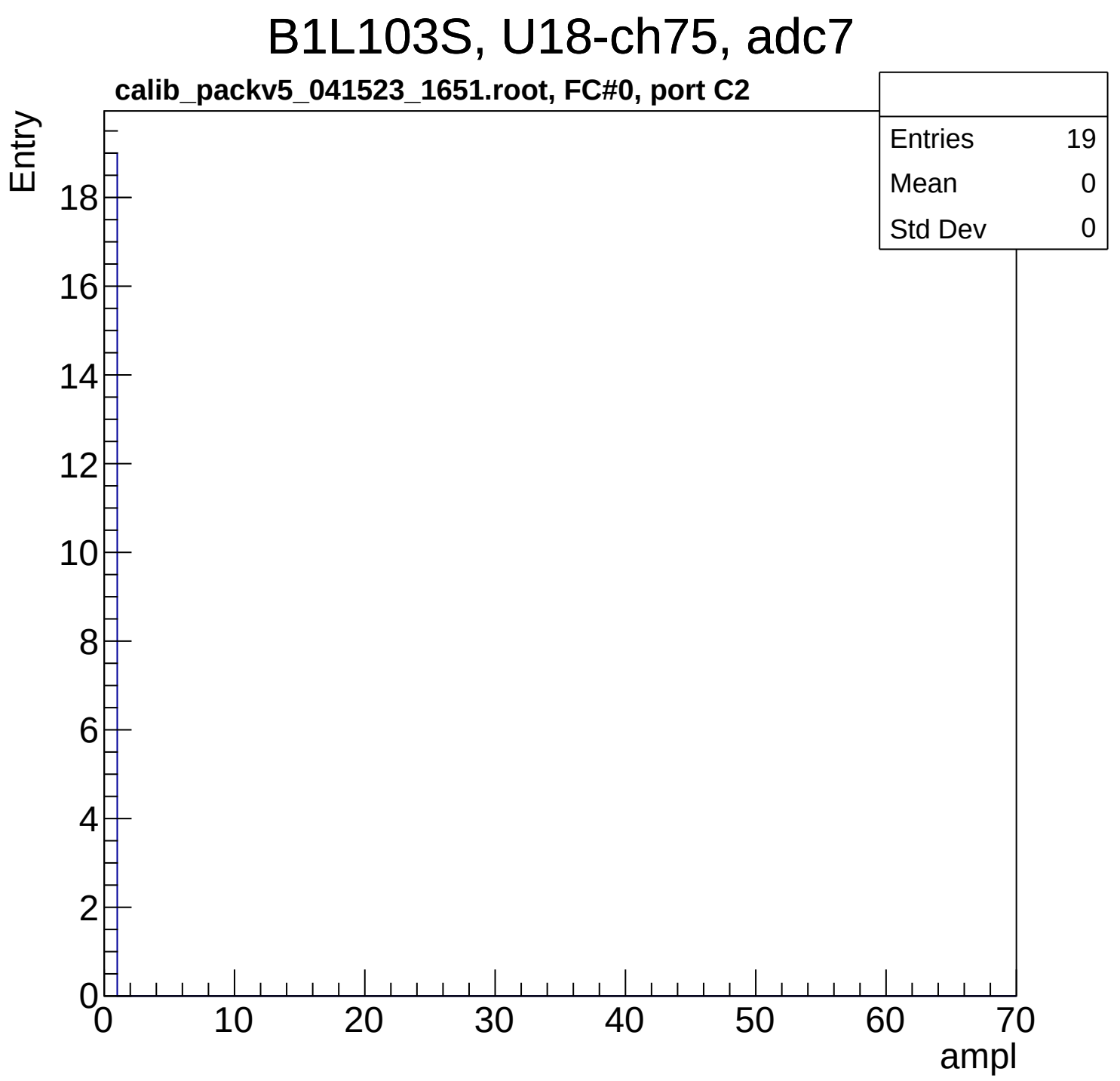
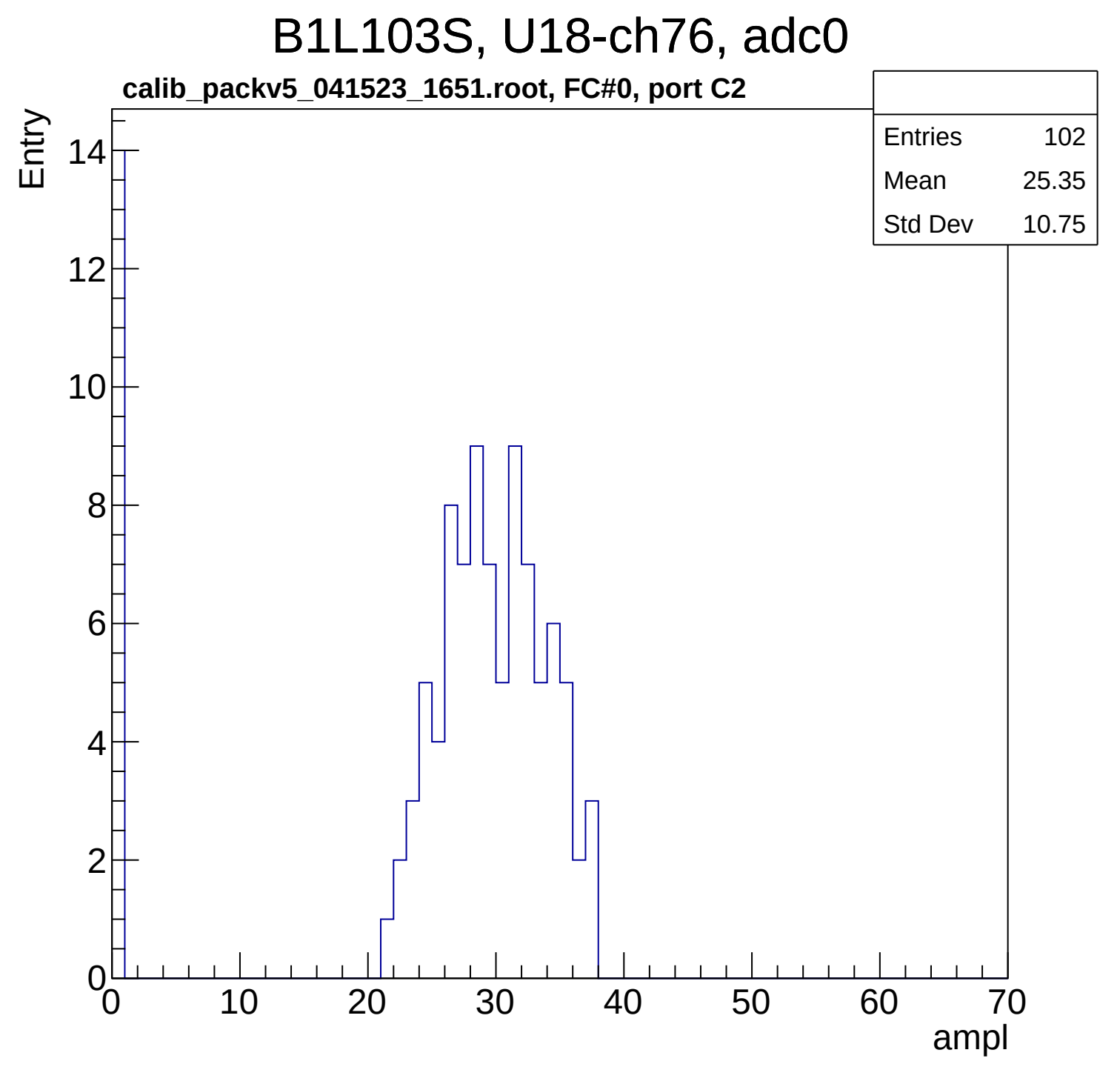

B1L103S, U18-ch75, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch76, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 102
Mean 25.35
Std Dev 10.75
Entry
ampl
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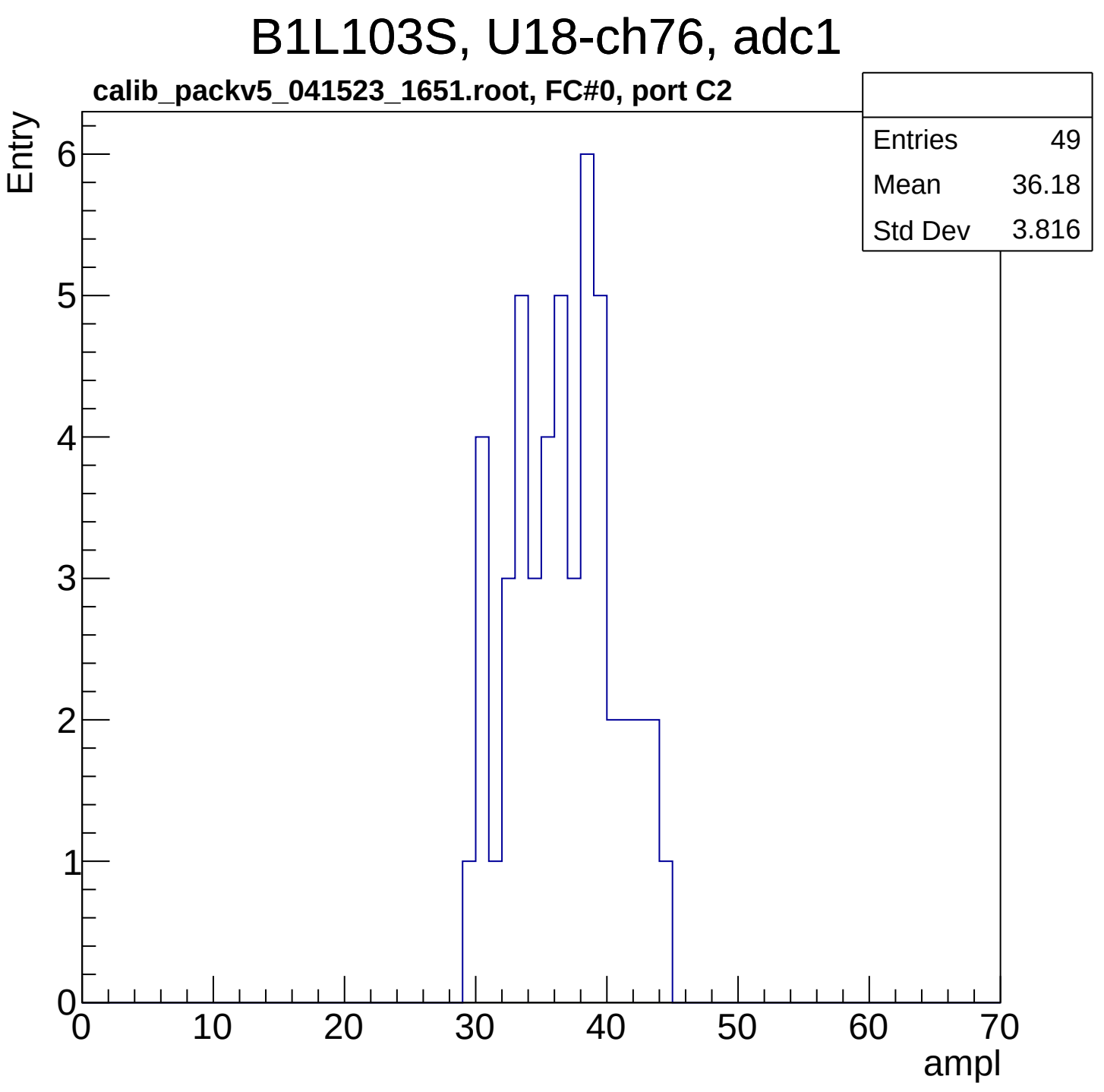
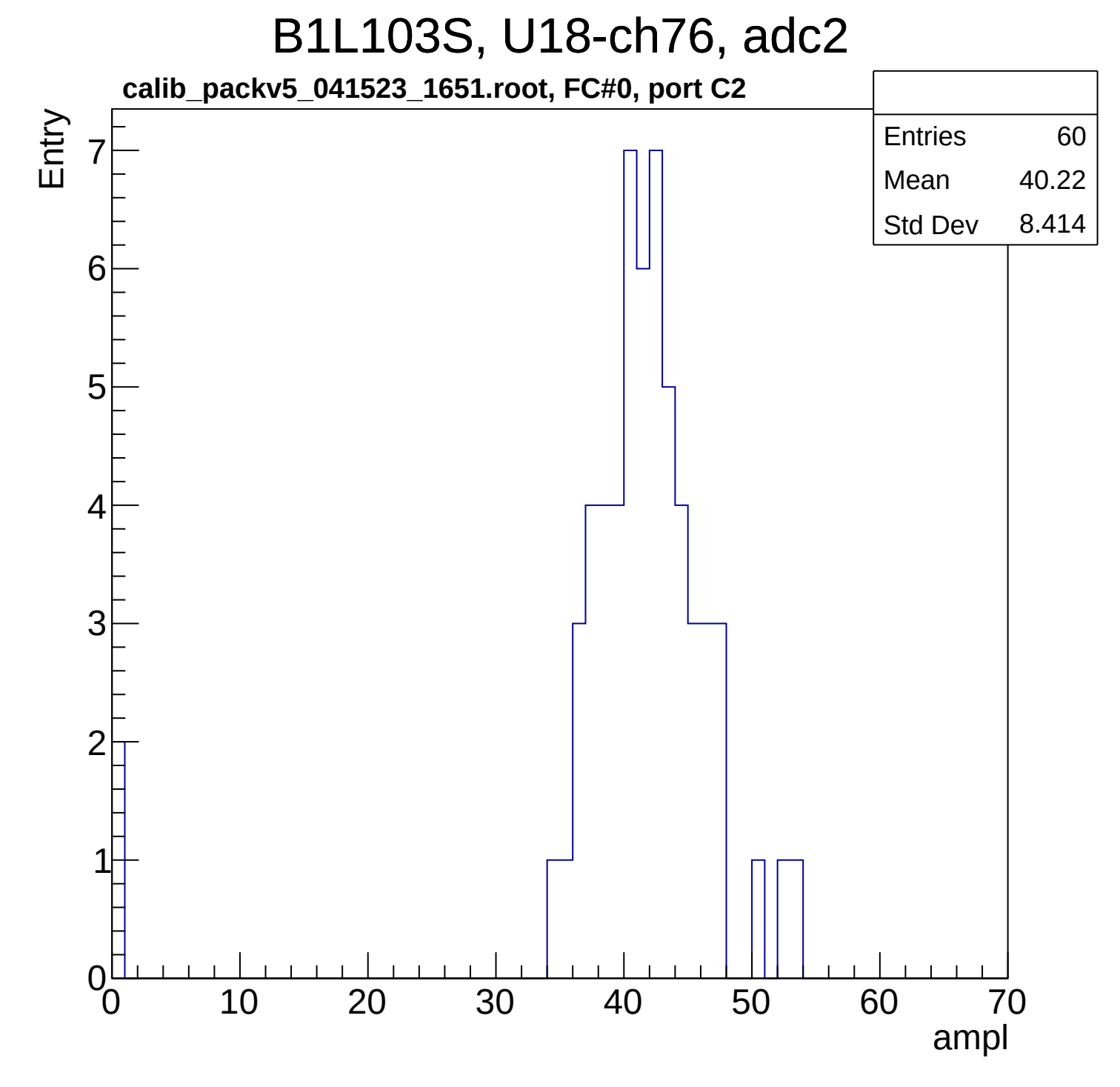
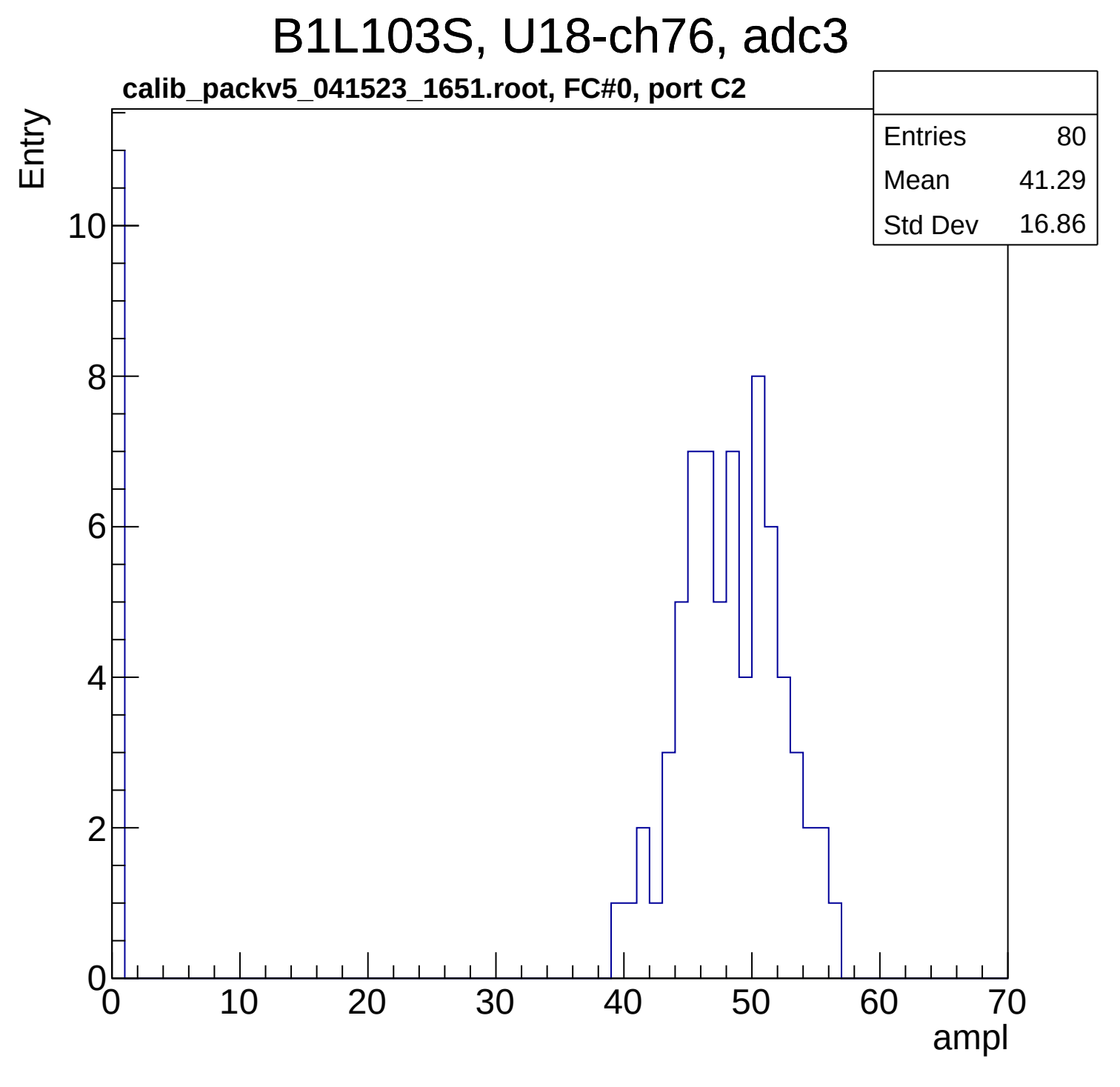
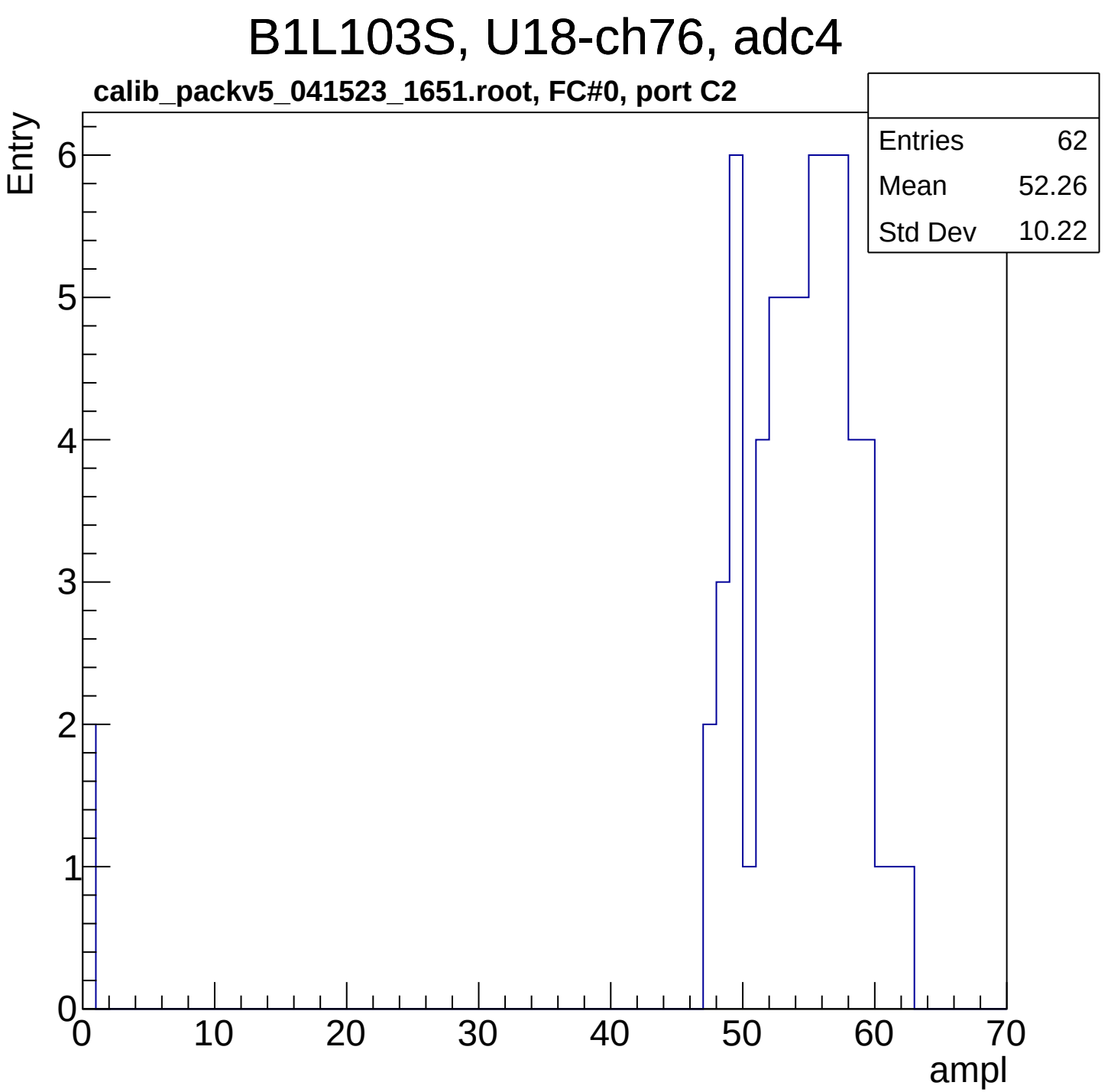
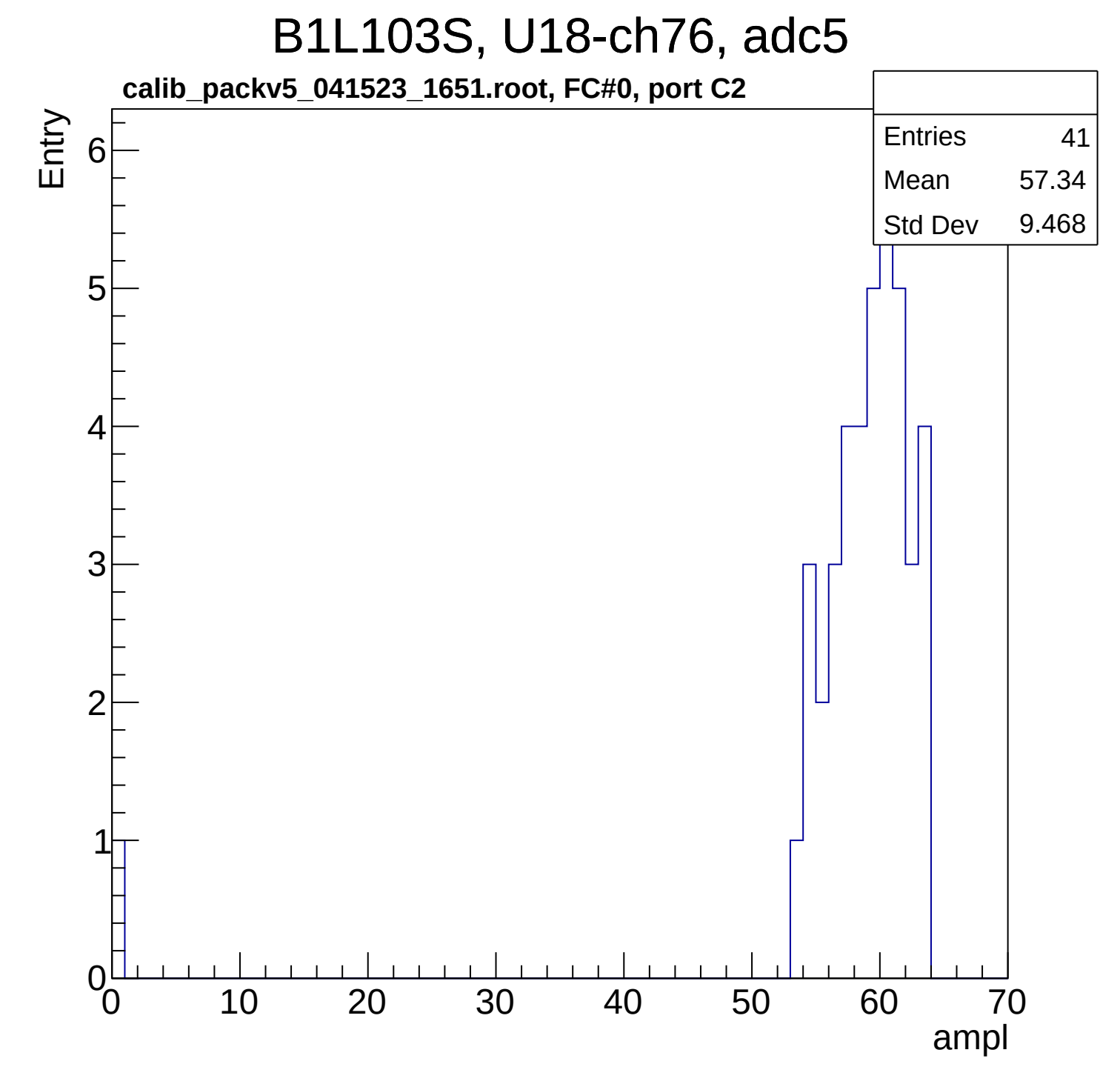
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

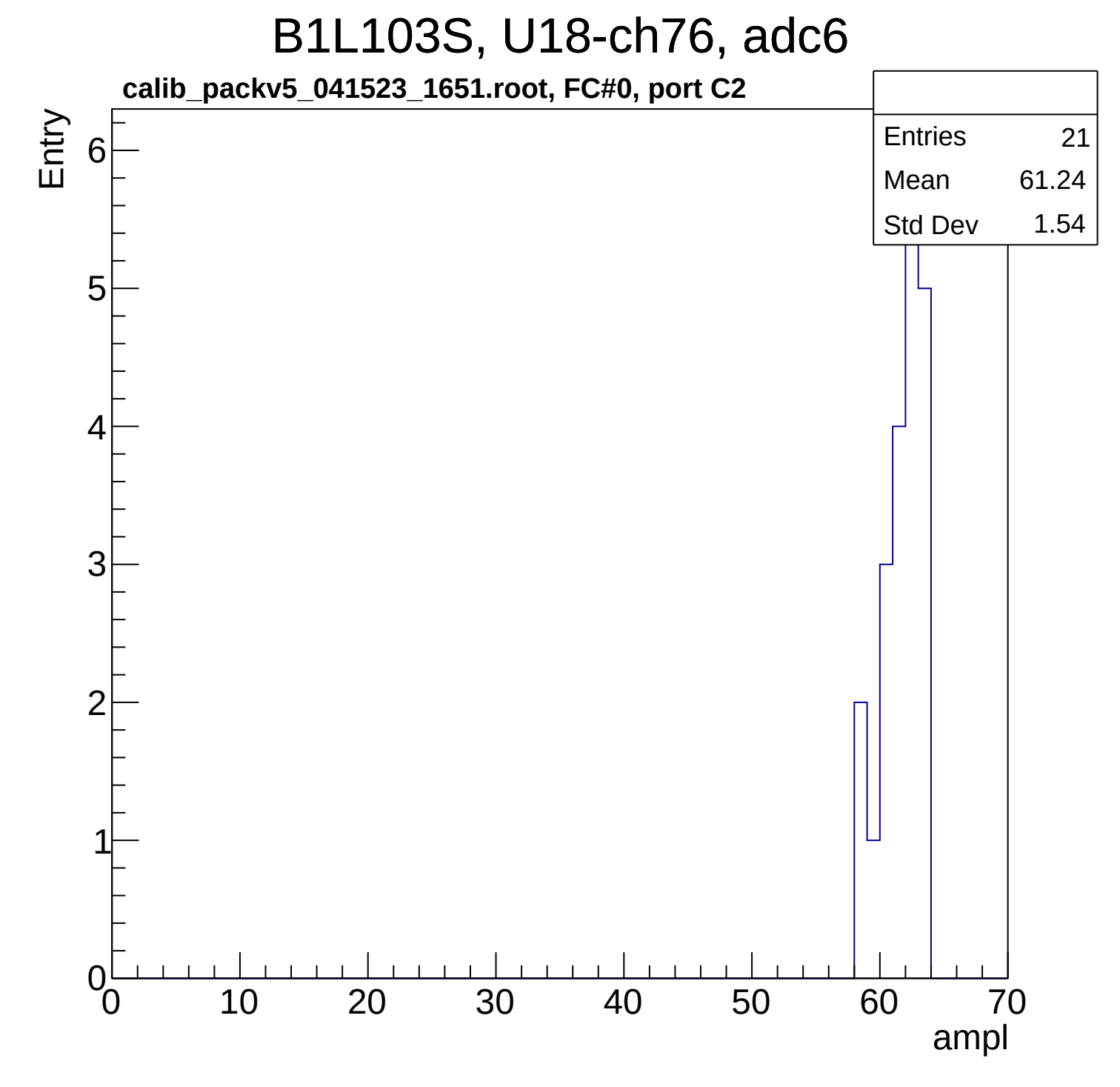

B1L103S, U18-ch76, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 36.18
Std Dev 3.816
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl

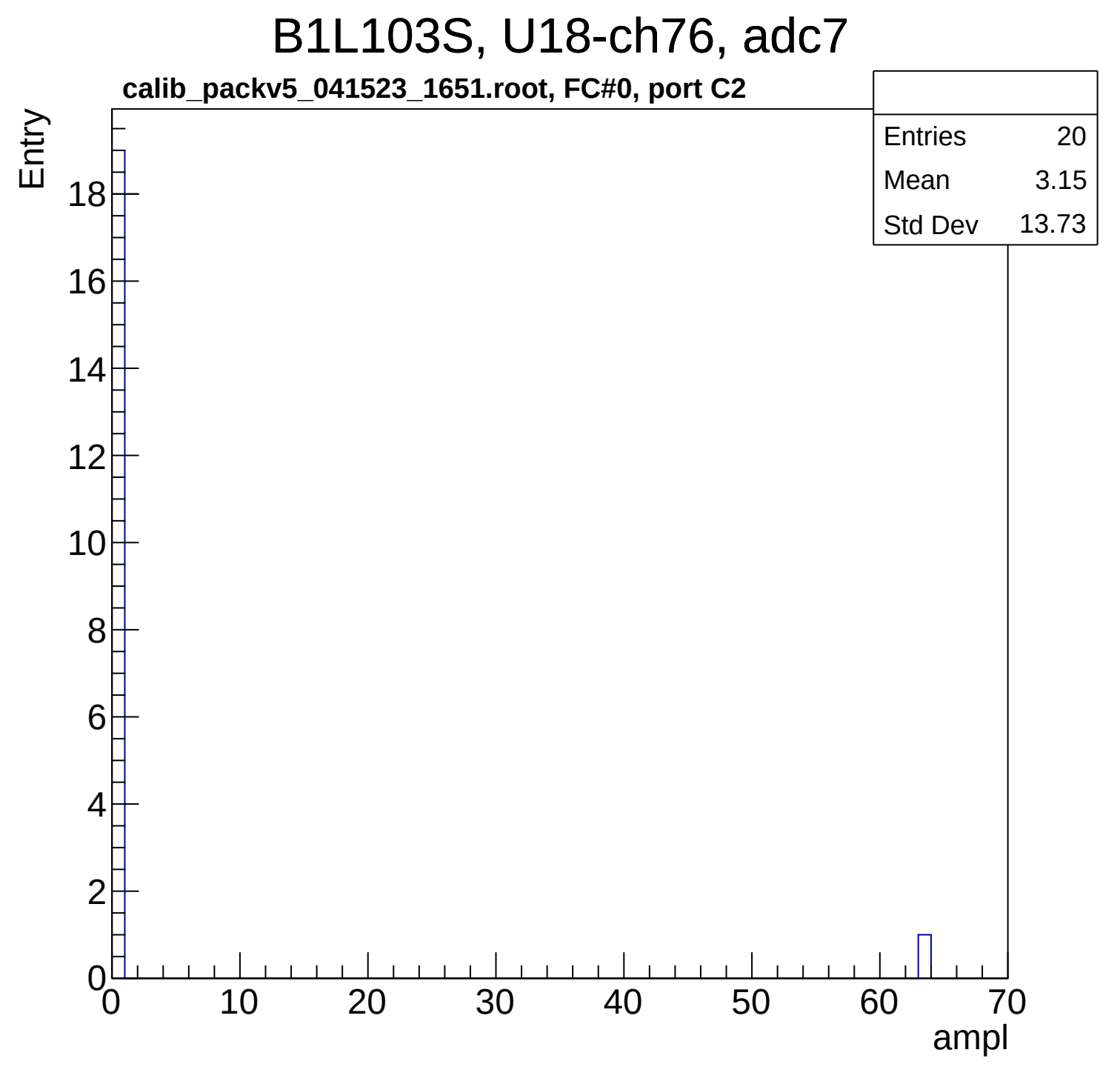

B1L103S, U18-ch76, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 40.22
Std Dev 8.414
Entry
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70
ampl

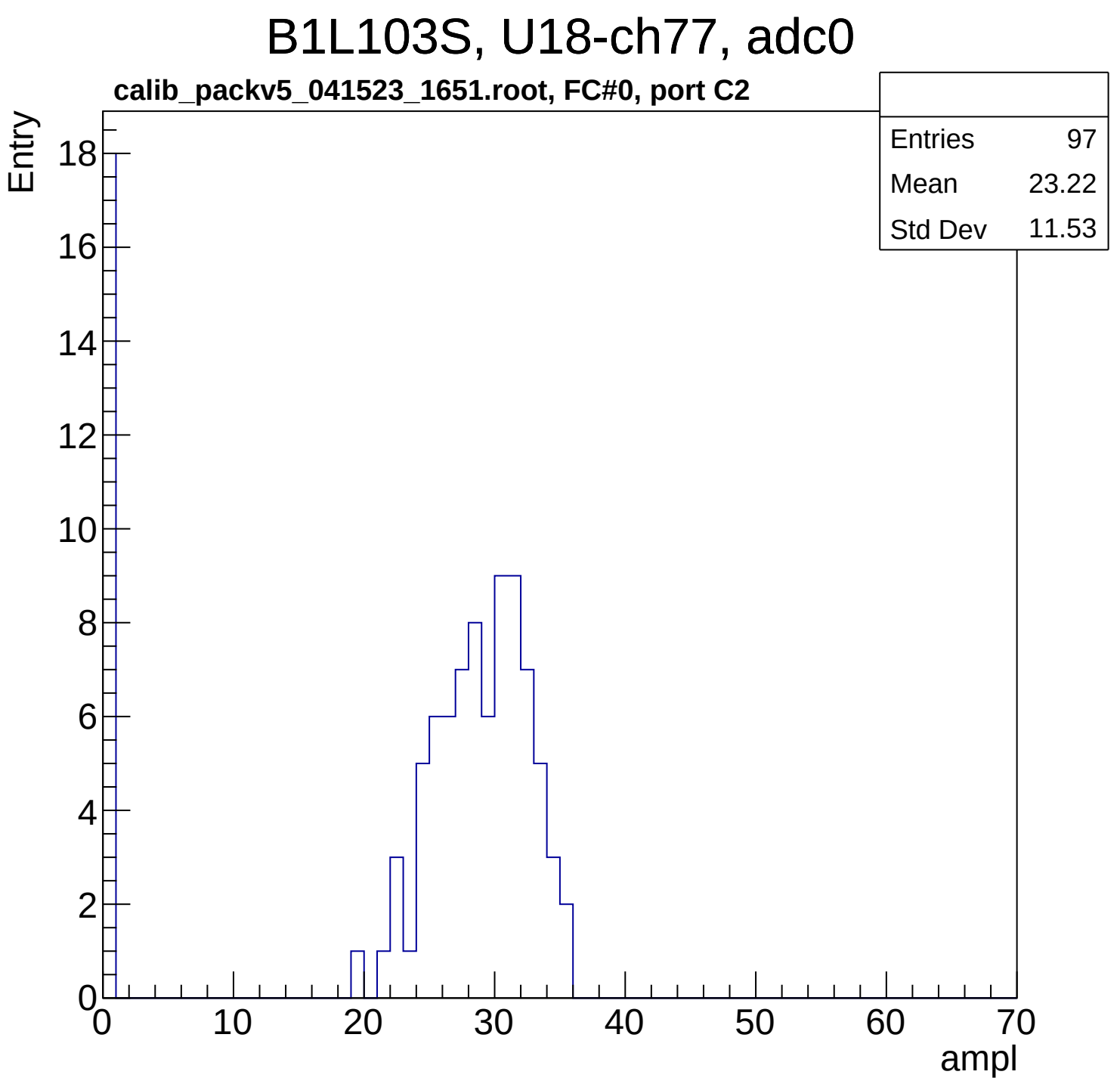

B1L103S, U18-ch76, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 41.29
Std Dev 16.86
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch76, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 52.26
Std Dev 10.22
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U18-ch76, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 41
Mean 57.34
Std Dev 9.468
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U18-ch76, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 61.24
Std Dev 1.54
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch76, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch77, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 97
Mean 23.22
Std Dev 11.53
Entry
ampl
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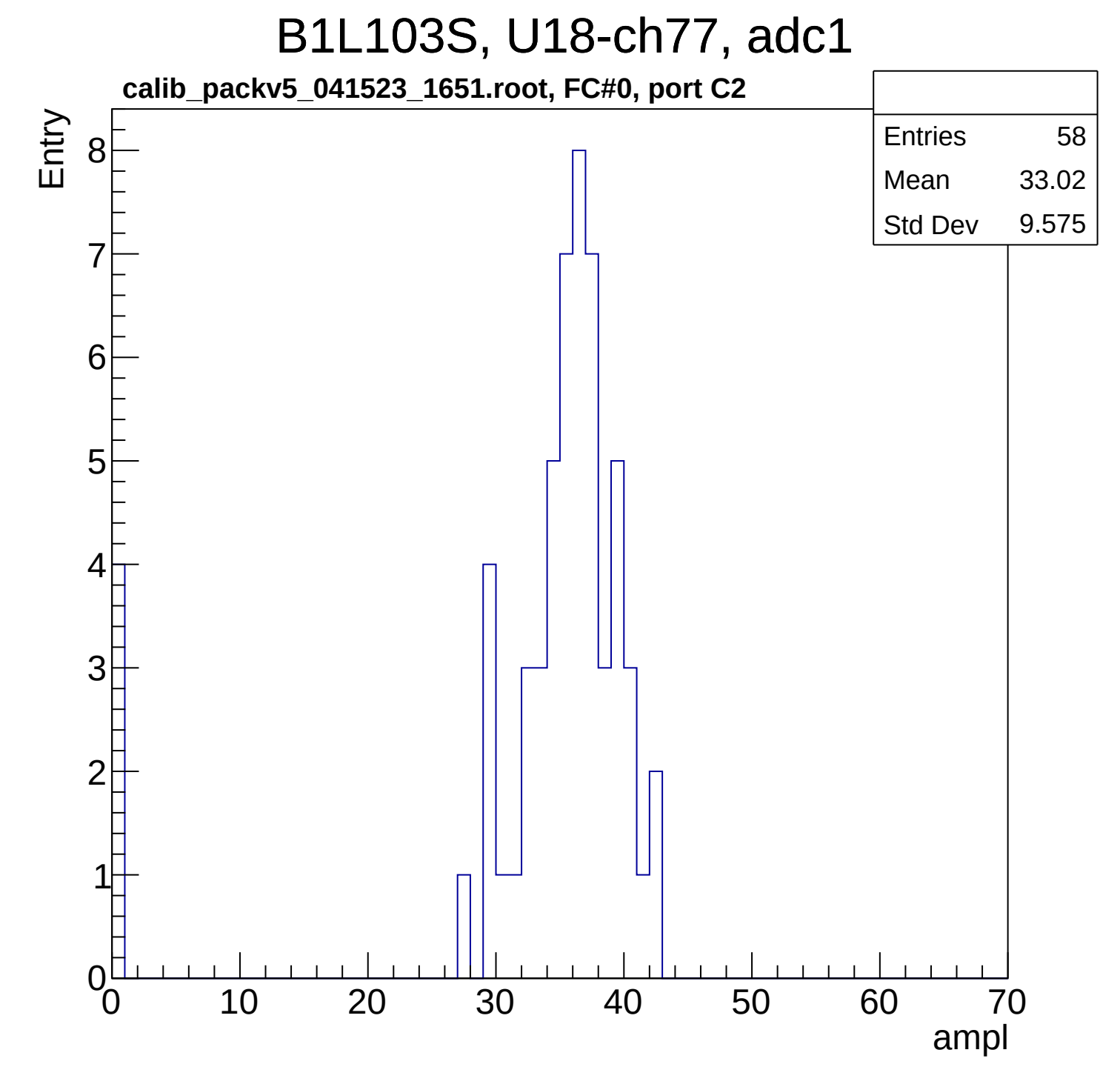
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70


B1L103S, U18-ch77, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 33.02
Std Dev 9.575
Entry
ampl
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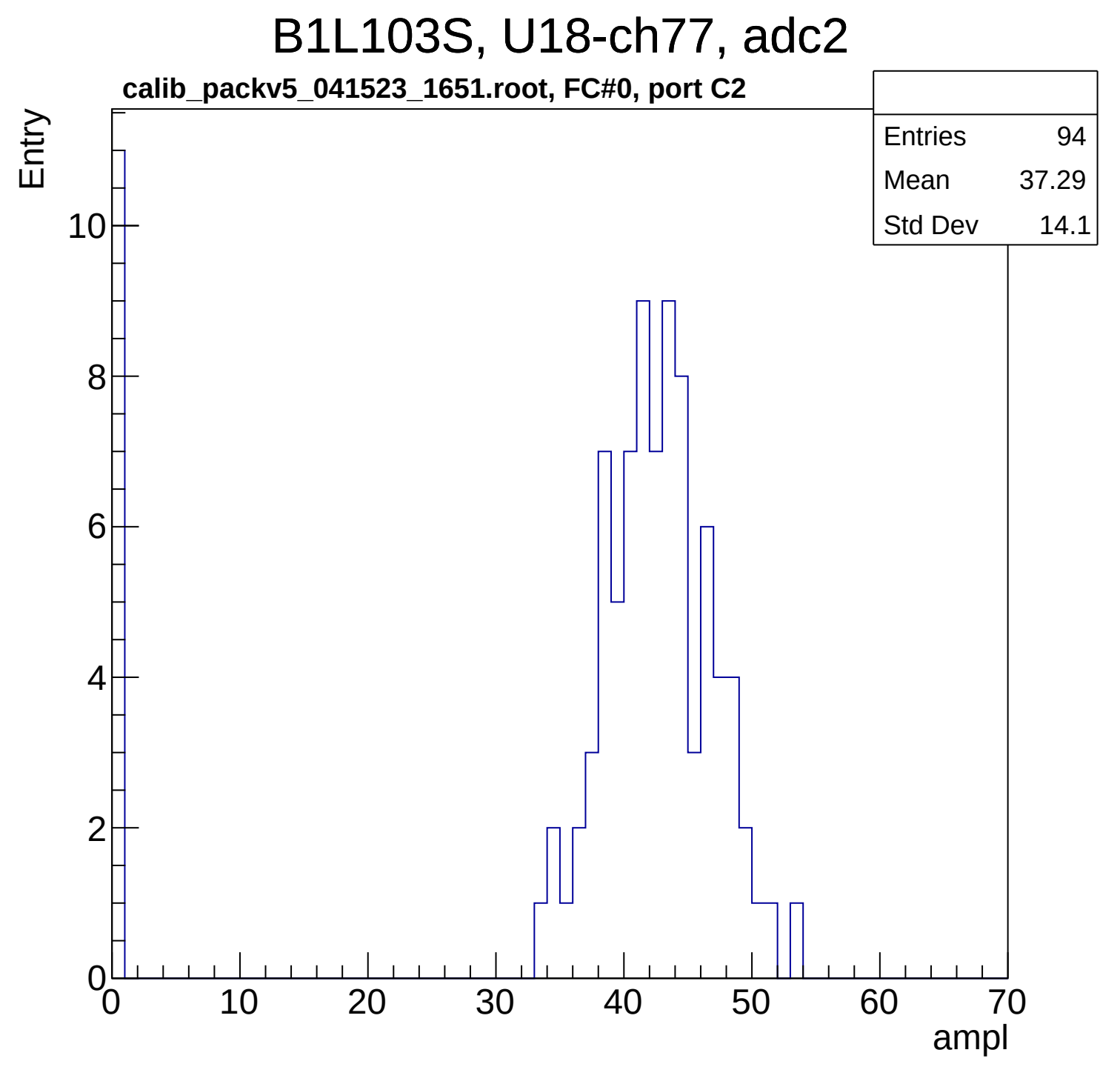
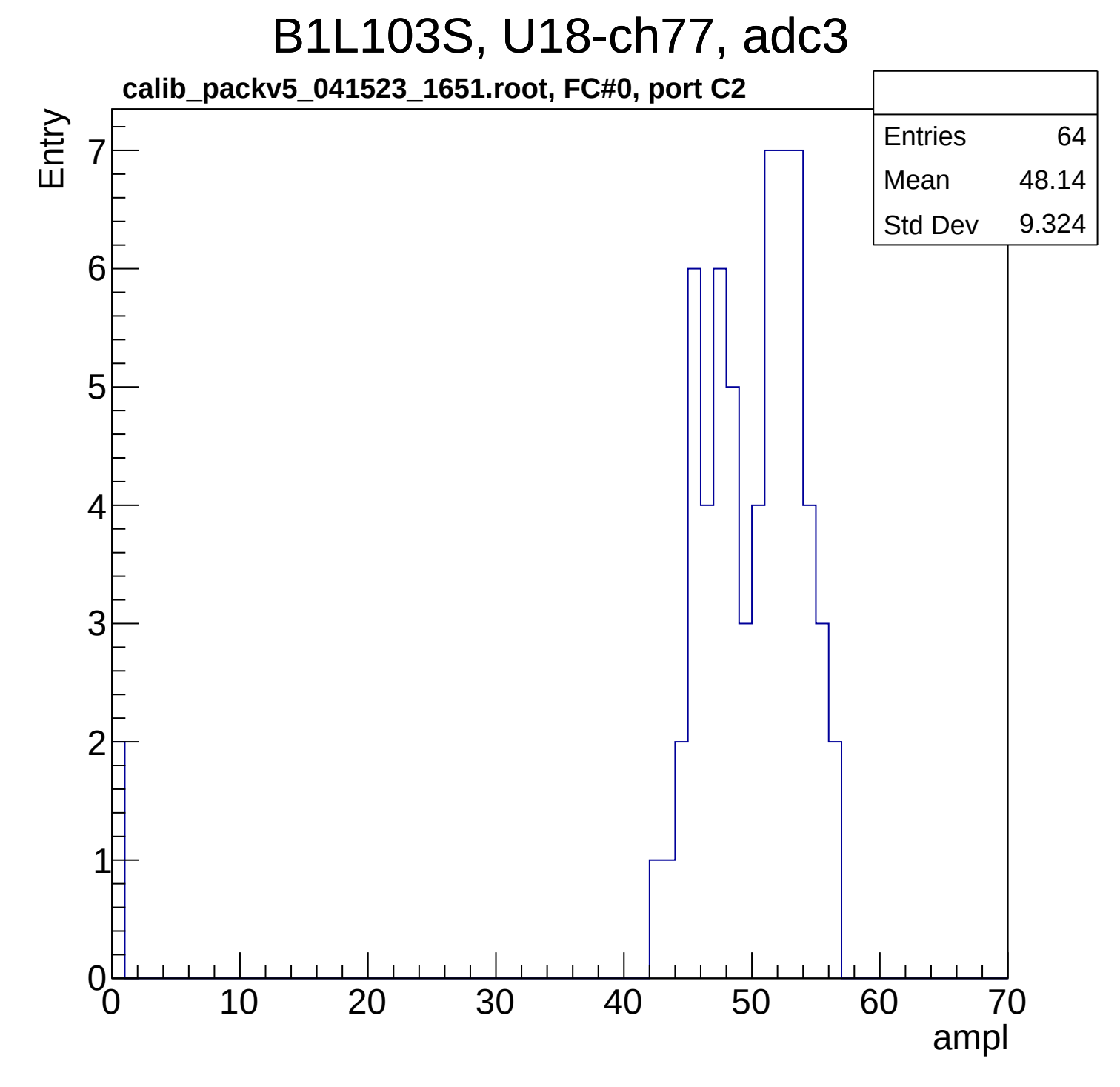
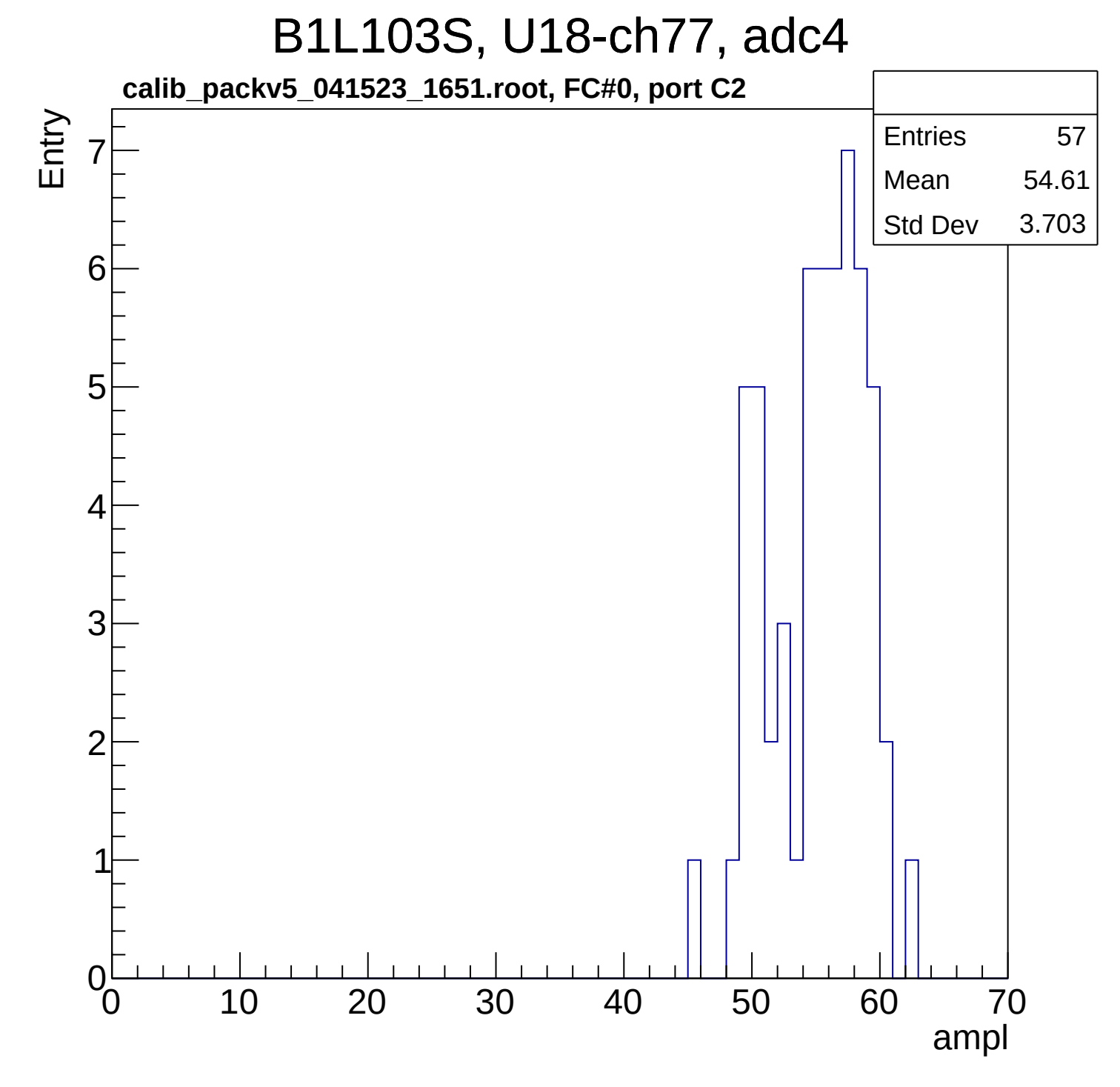
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch77, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 94
Mean 37.29
Std Dev 14.1
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch77, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 48.14
Std Dev 9.324
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U18-ch77, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 54.61
Std Dev 3.703
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
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40
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60
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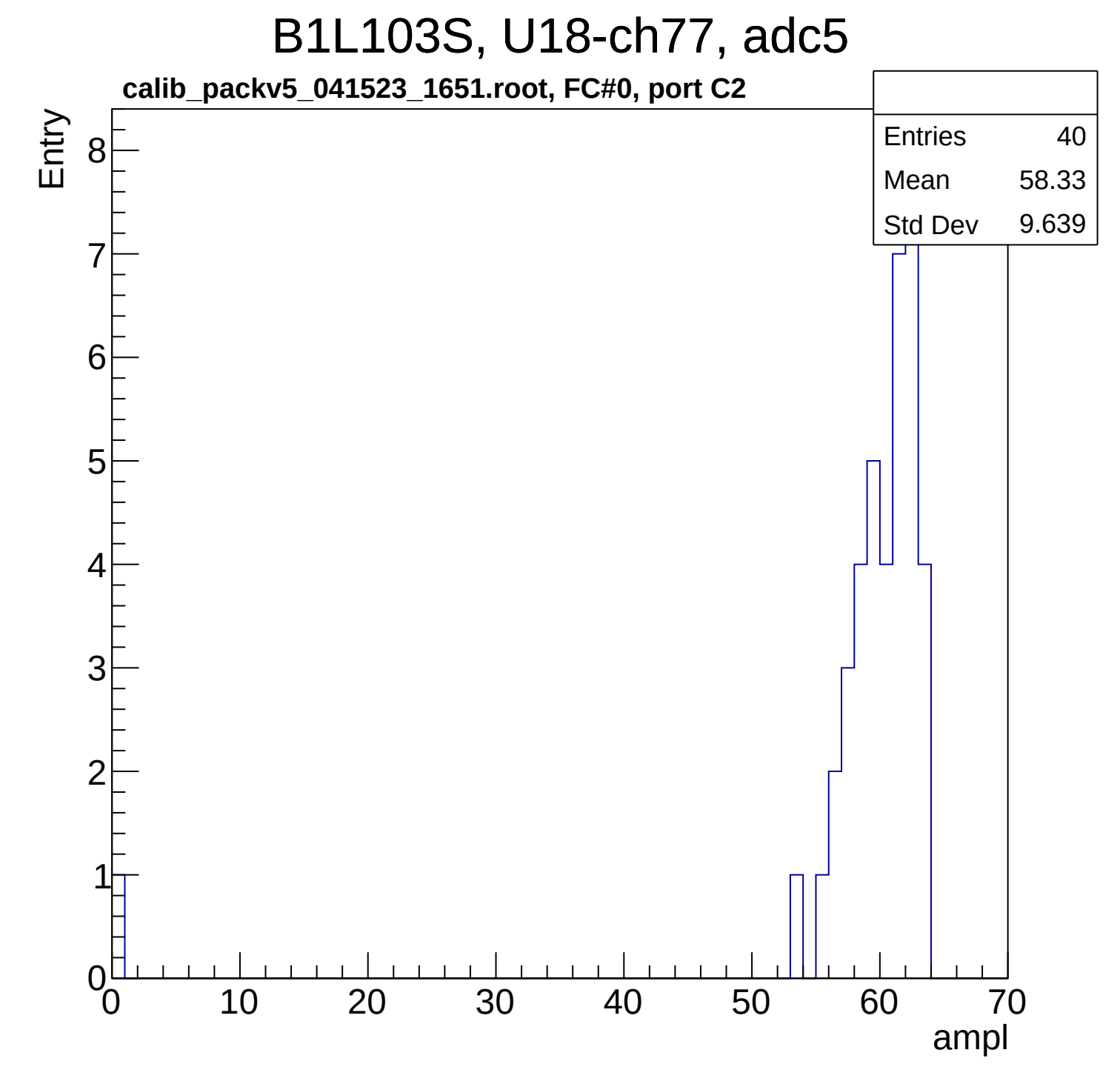
B1L103S, U18-ch77, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 40
Mean 58.33
Std Dev 9.639
Entry
ampl
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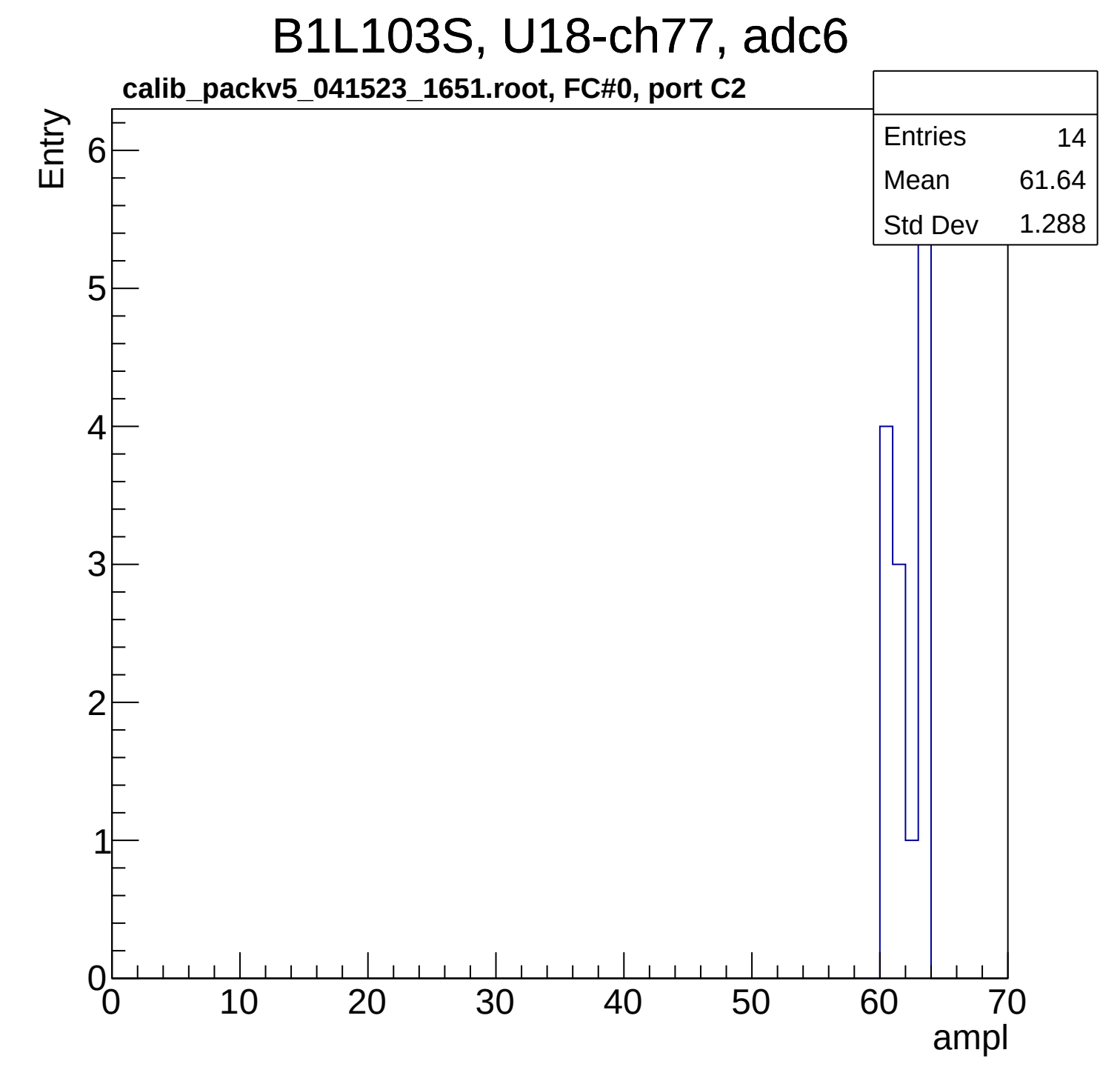
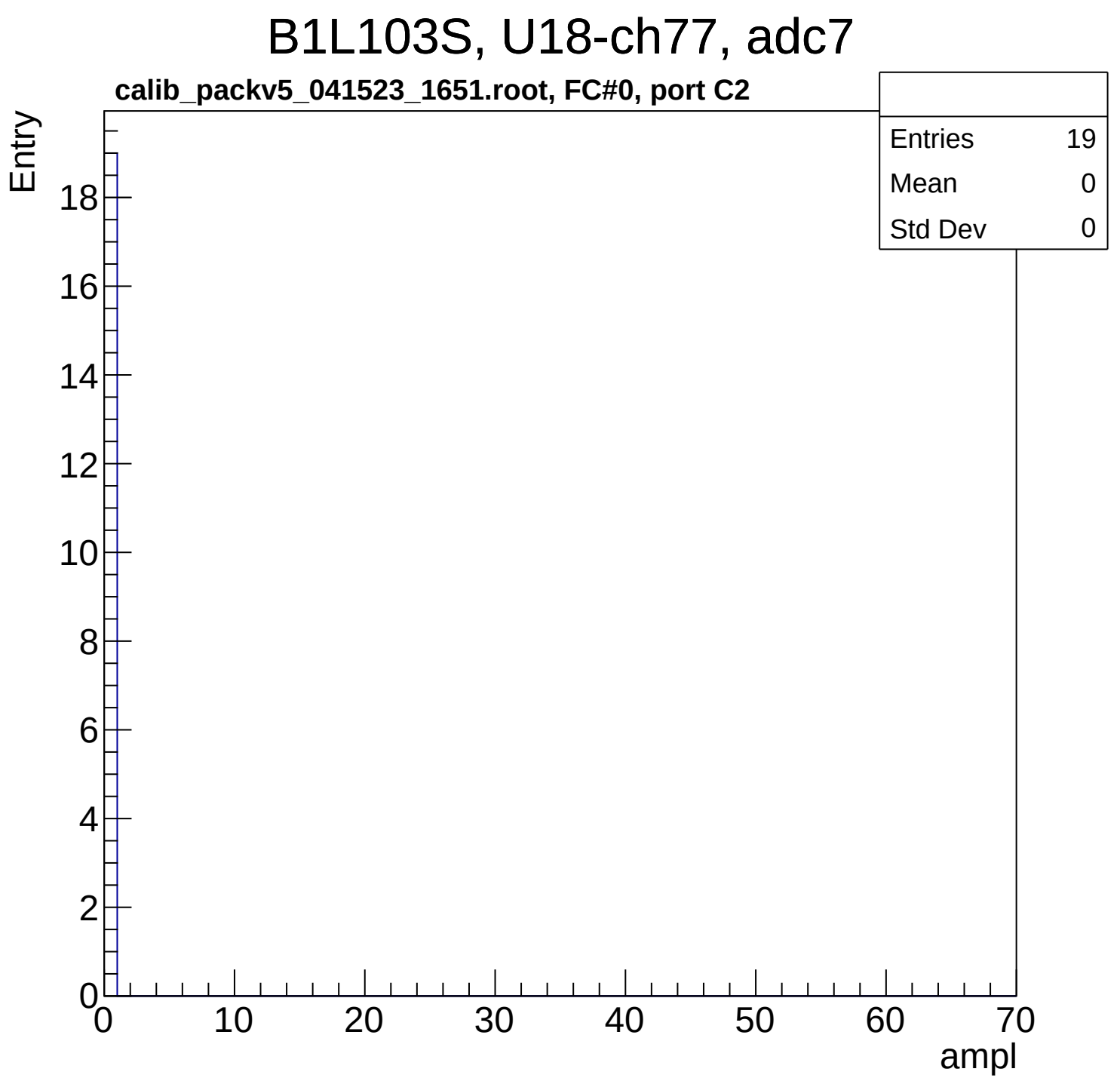
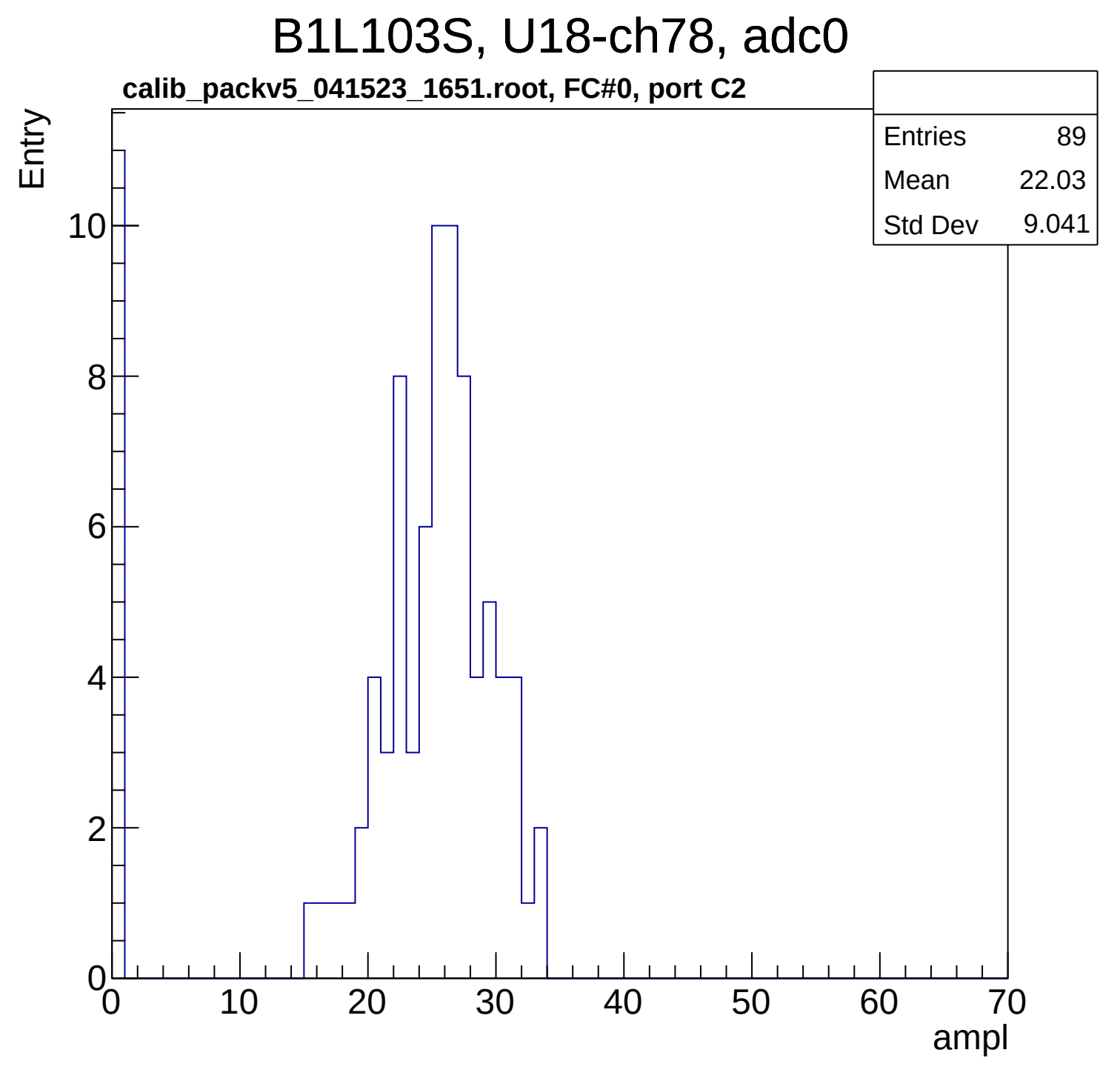
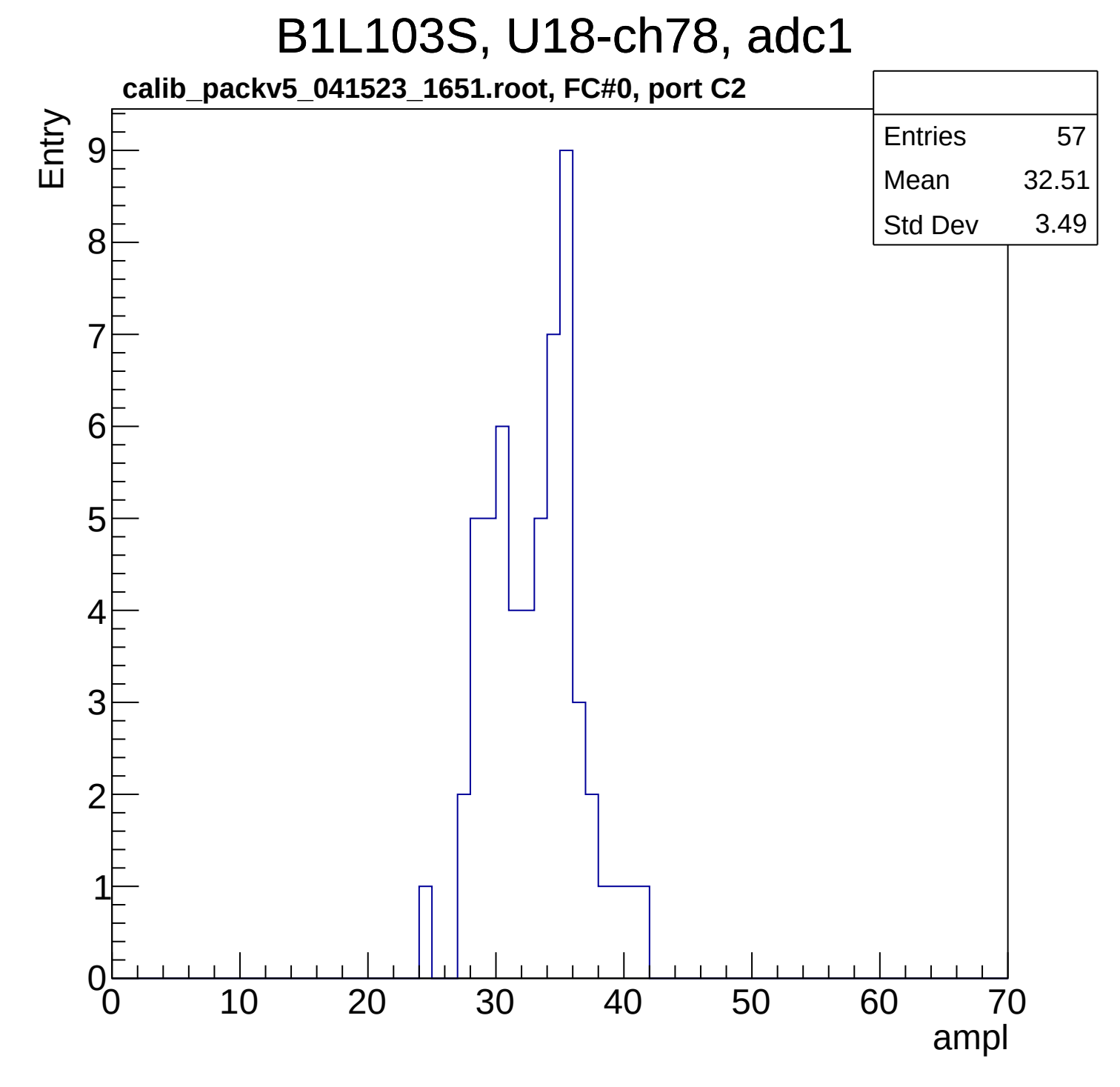
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch77, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 14
Mean 61.64
Std Dev 1.288
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch77, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch78, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 89
Mean 22.03
Std Dev 9.041
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U18-ch78, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 32.51
Std Dev 3.49
Entry
ampl
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3
4
5
6
7
8
9
0
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20
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60
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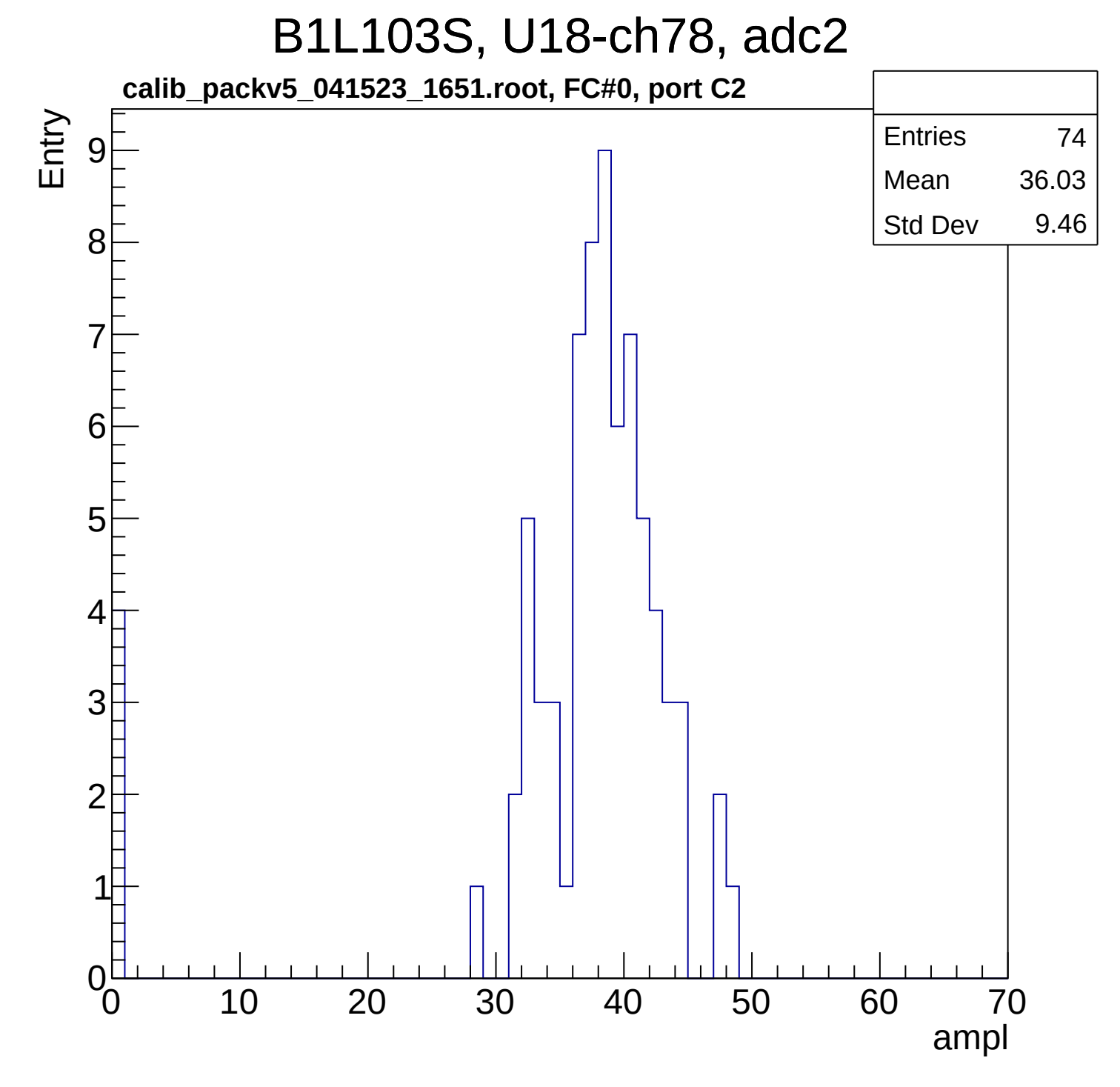
B1L103S, U18-ch78, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 36.03
Std Dev 9.46
Entry
ampl
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3
4
5
6
7
8
9
0
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60
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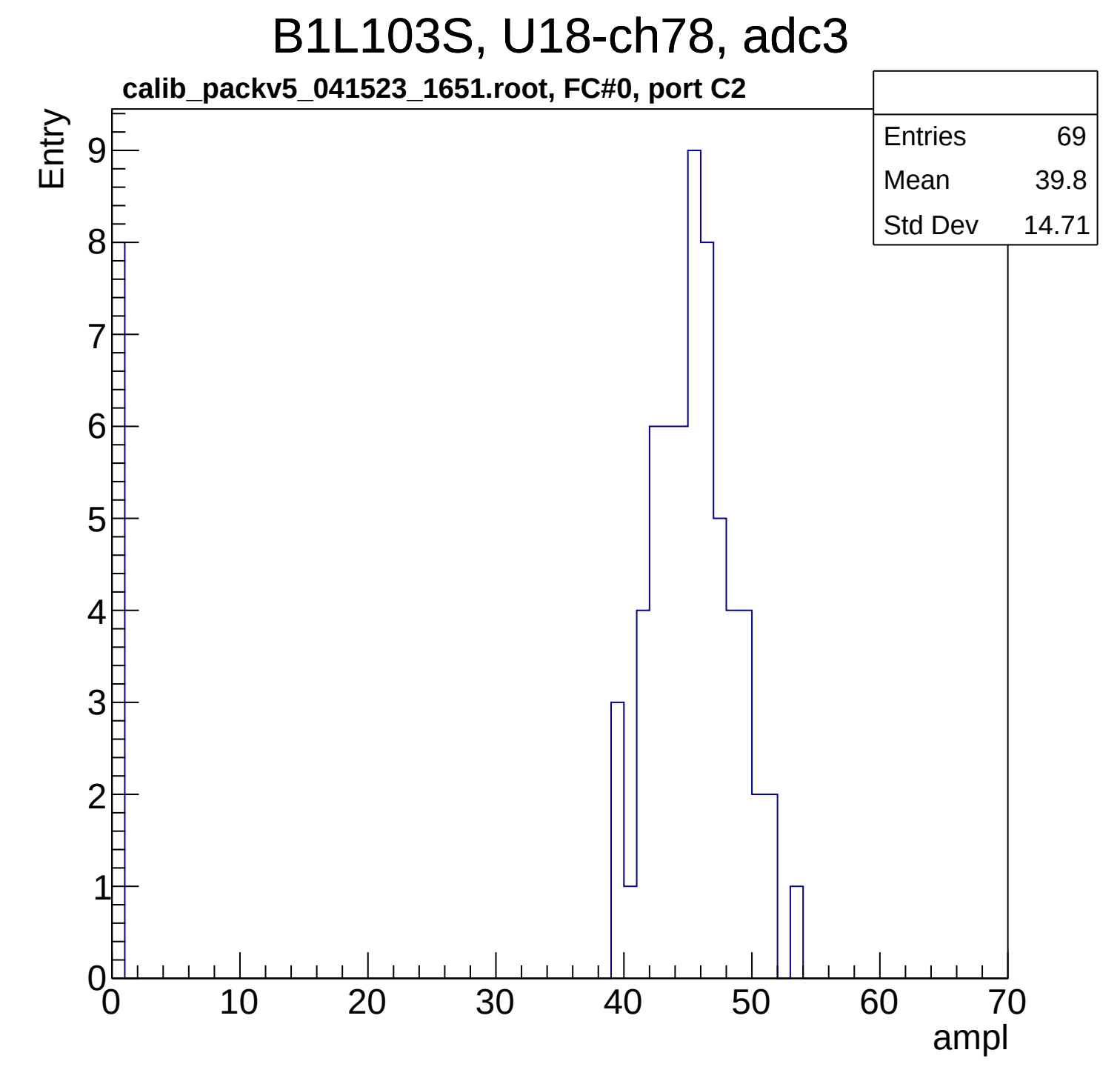
B1L103S, U18-ch78, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 39.8
Std Dev 14.71
Entry
ampl
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2
3
4
5
6
7
8
9
0
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60
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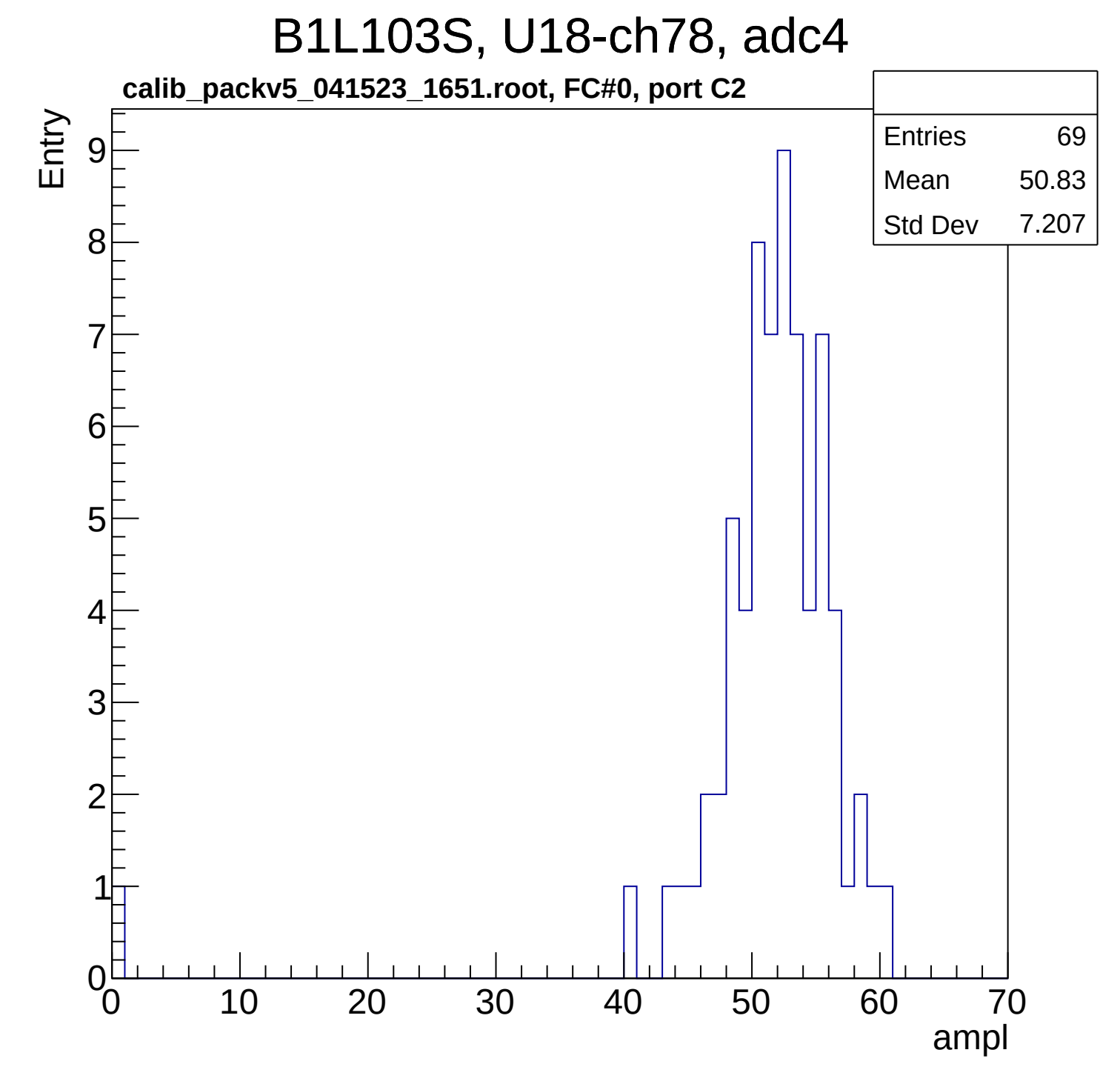
B1L103S, U18-ch78, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 50.83
Std Dev 7.207
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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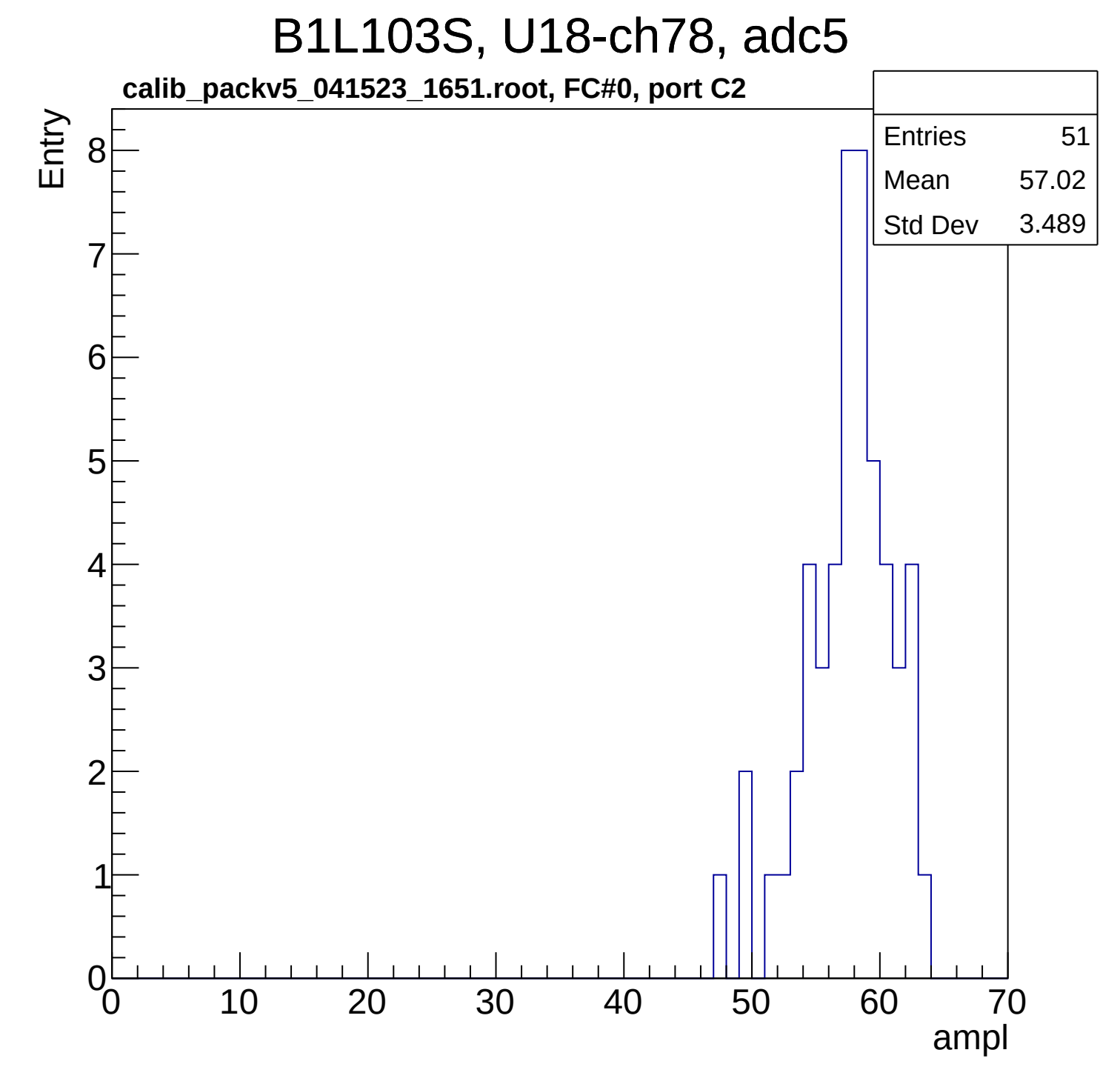
40
50
60
70


B1L103S, U18-ch78, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 57.02
Std Dev 3.489
Entry
ampl
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2
3
4
5
6
7
8
0
10
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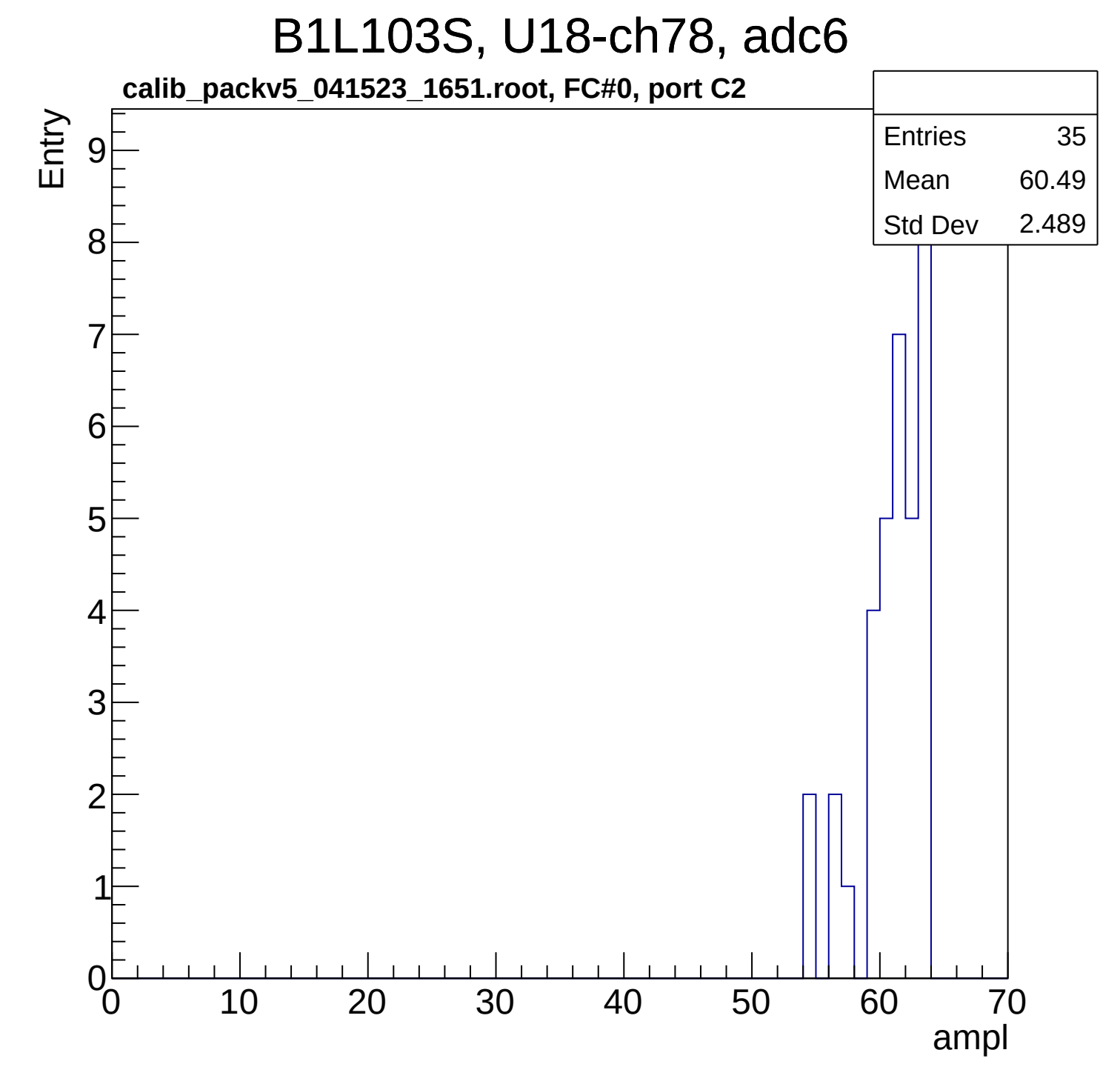
50
60
70


B1L103S, U18-ch78, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 35
Mean 60.49
Std Dev 2.489
Entry
ampl
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2
3
4
5
6
7
8
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0
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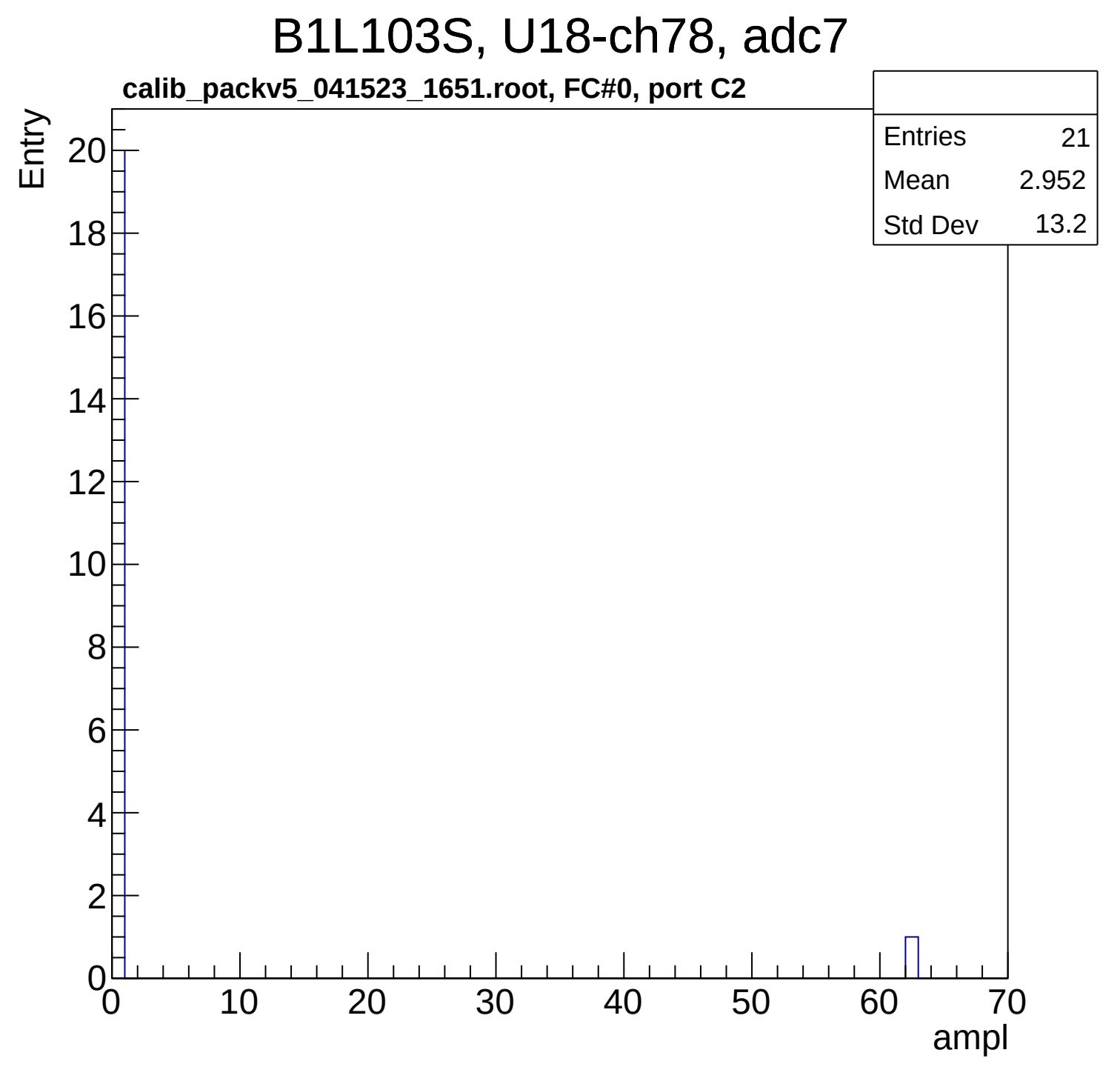
50
60
70


B1L103S, U18-ch78, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 2.952
Std Dev 13.2
Entry
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10
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16
18
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10
20
30
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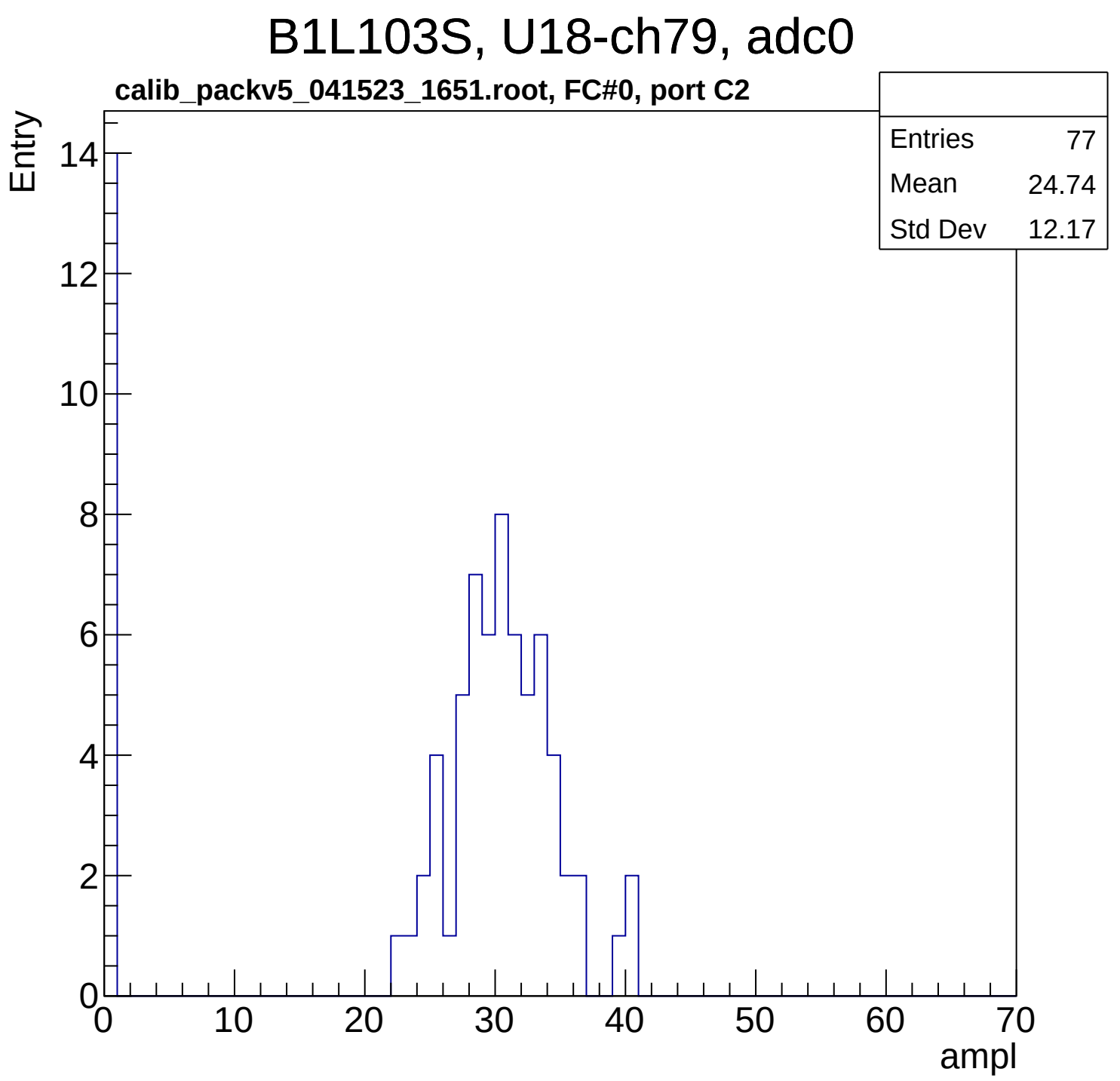
50
60
70
ampl


B1L103S, U18-ch79, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 24.74
Std Dev 12.17
Entry
ampl
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2
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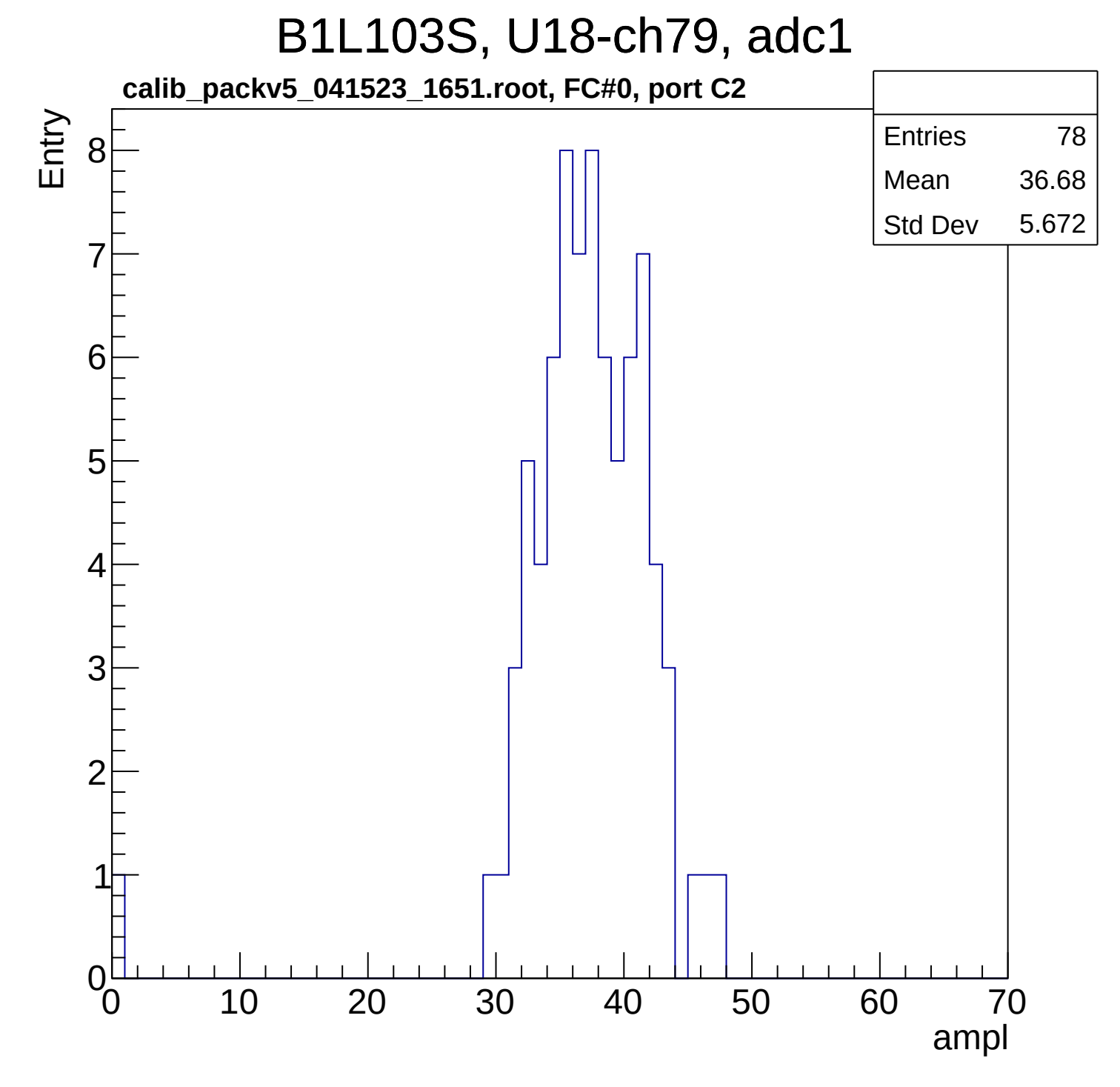
8
10
12
14
0
10
20
30
40
50
60
70


B1L103S, U18-ch79, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 36.68
Std Dev 5.672
Entry
ampl
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2
3
4
5
6
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0
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20
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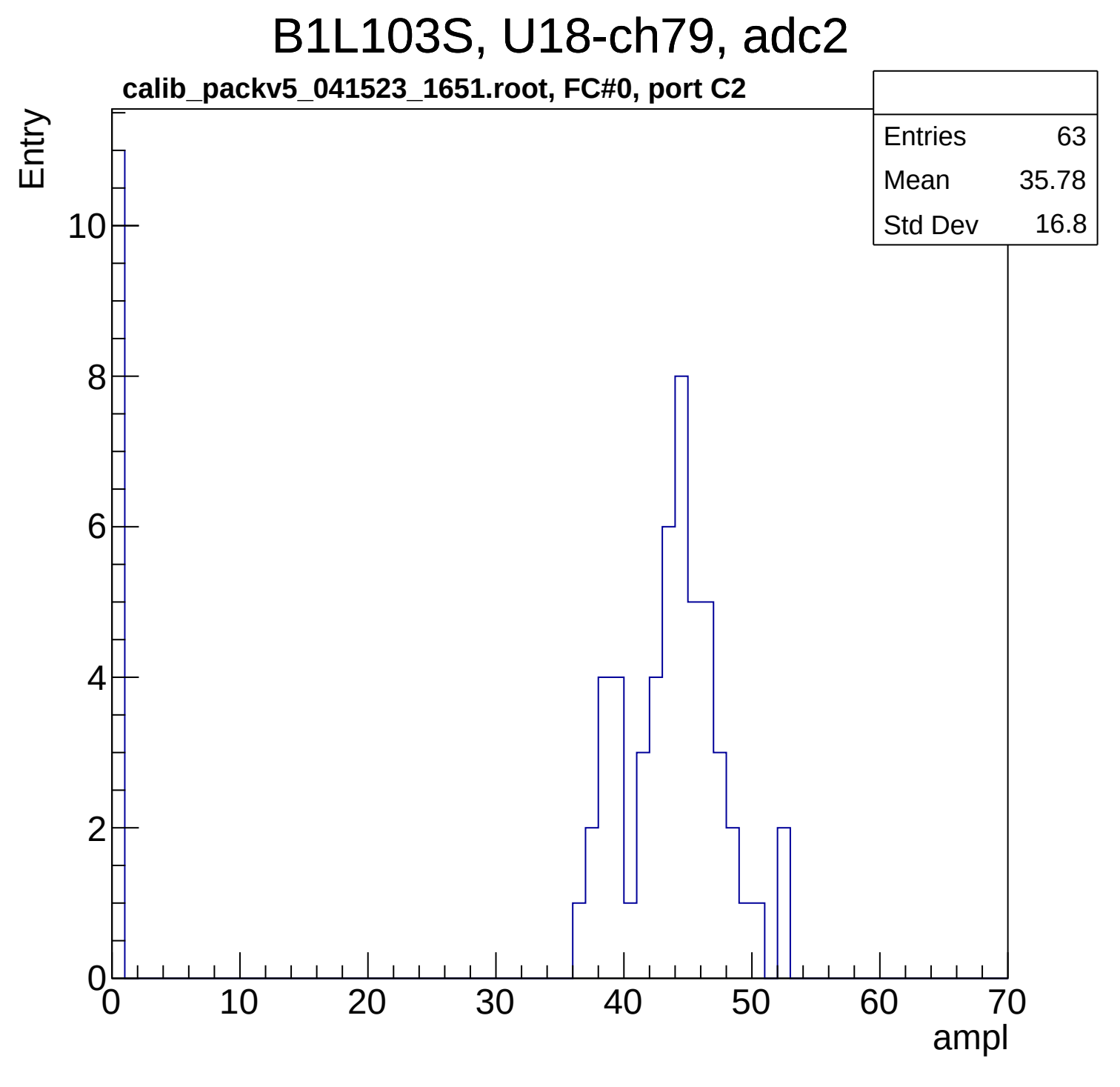
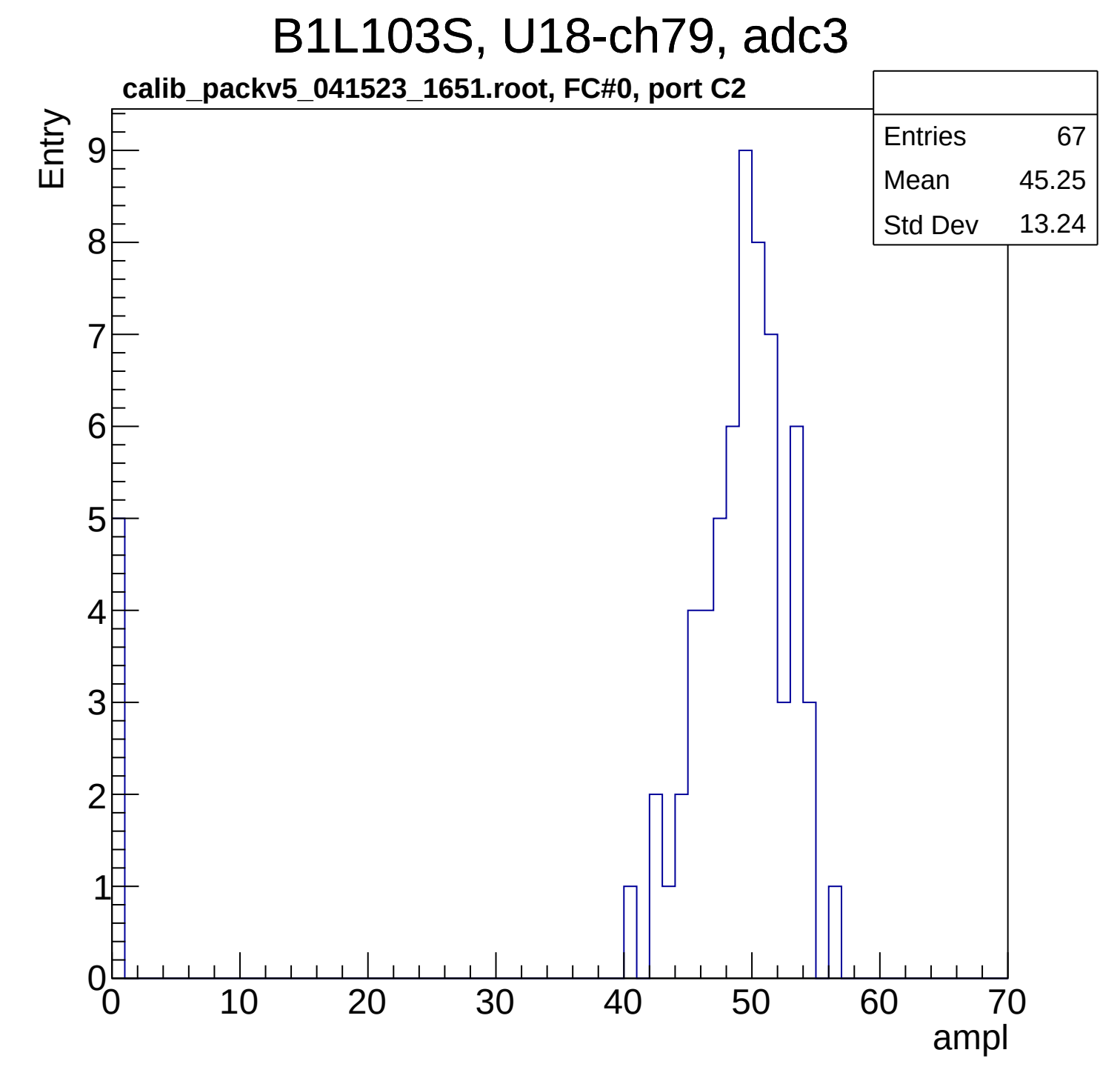

B1L103S, U18-ch79, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 35.78
Std Dev 16.8
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch79, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 45.25
Std Dev 13.24
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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60
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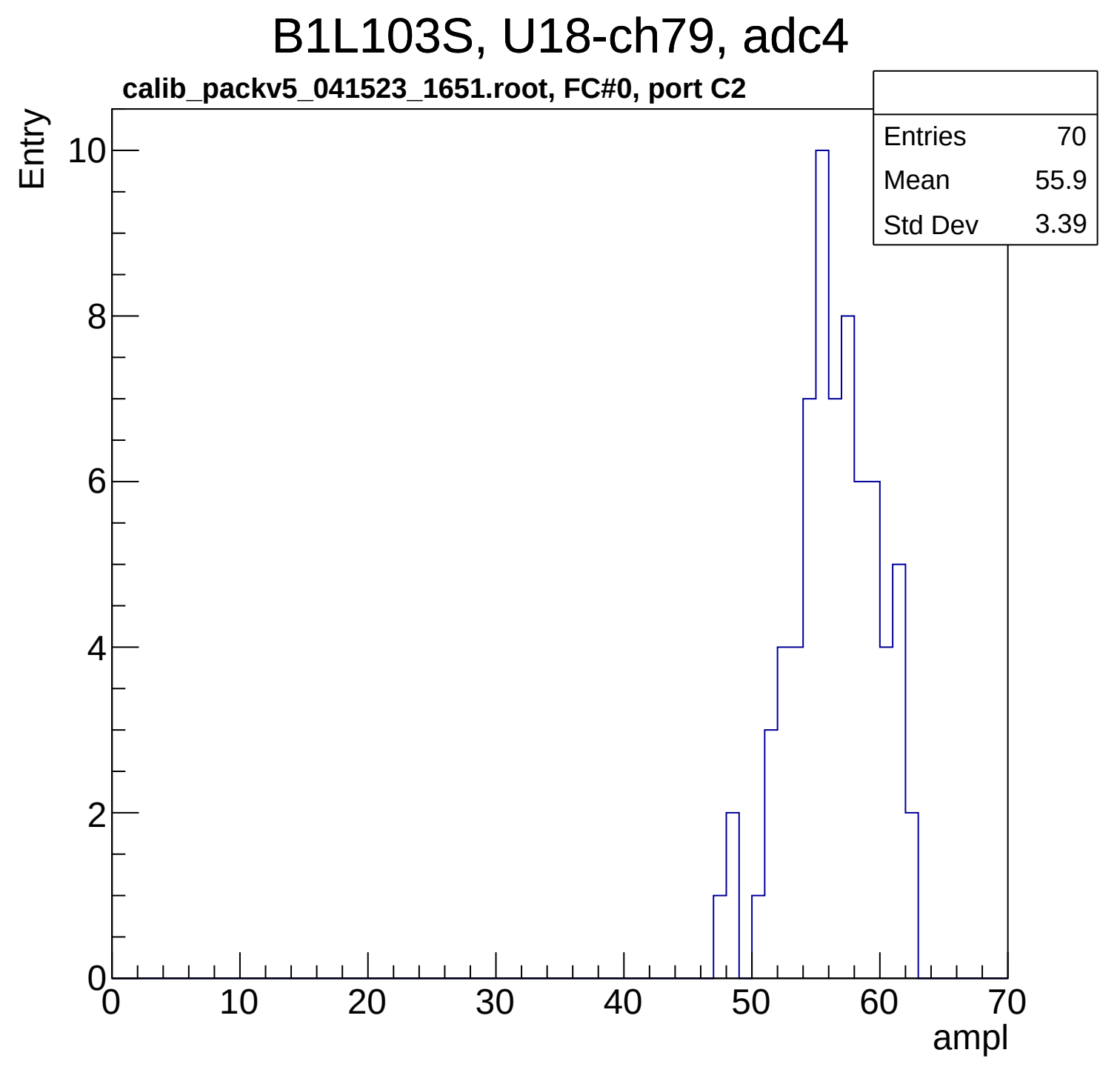
B1L103S, U18-ch79, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 55.9
Std Dev 3.39
Entry
0
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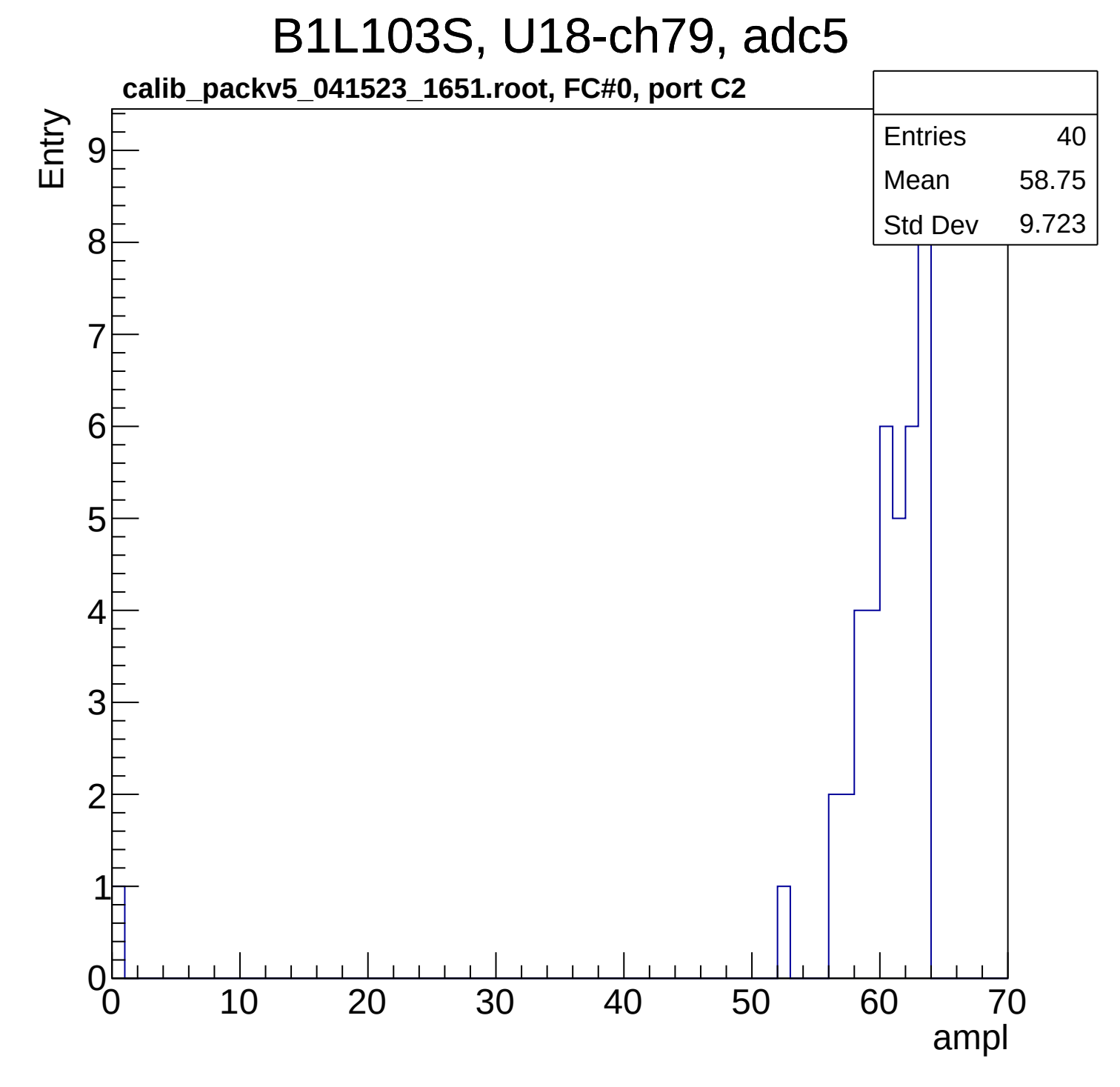
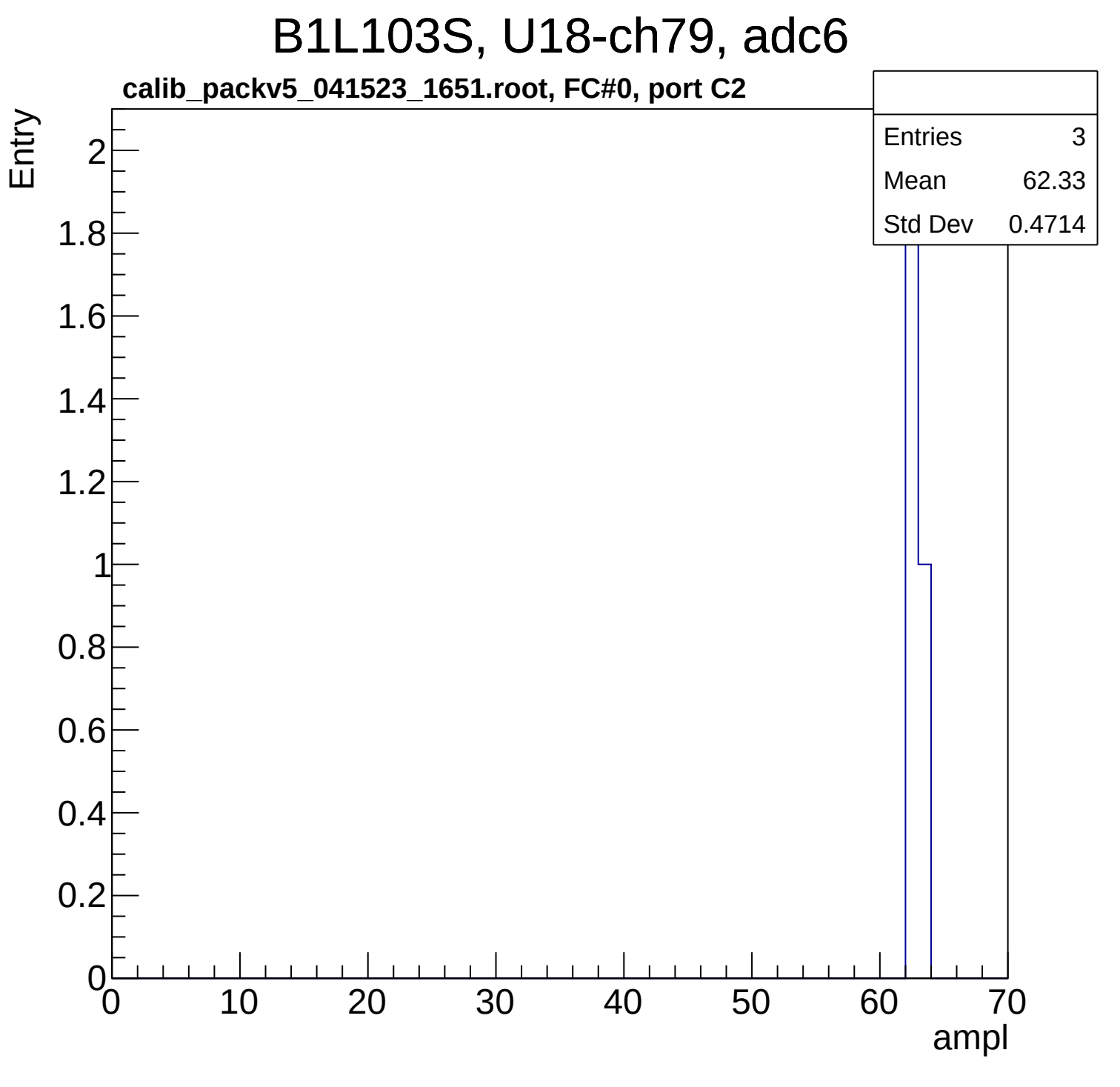
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch79, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 40
Mean 58.75
Std Dev 9.723
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U18-ch79, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 3
Mean 62.33
Std Dev 0.4714
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
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40
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60
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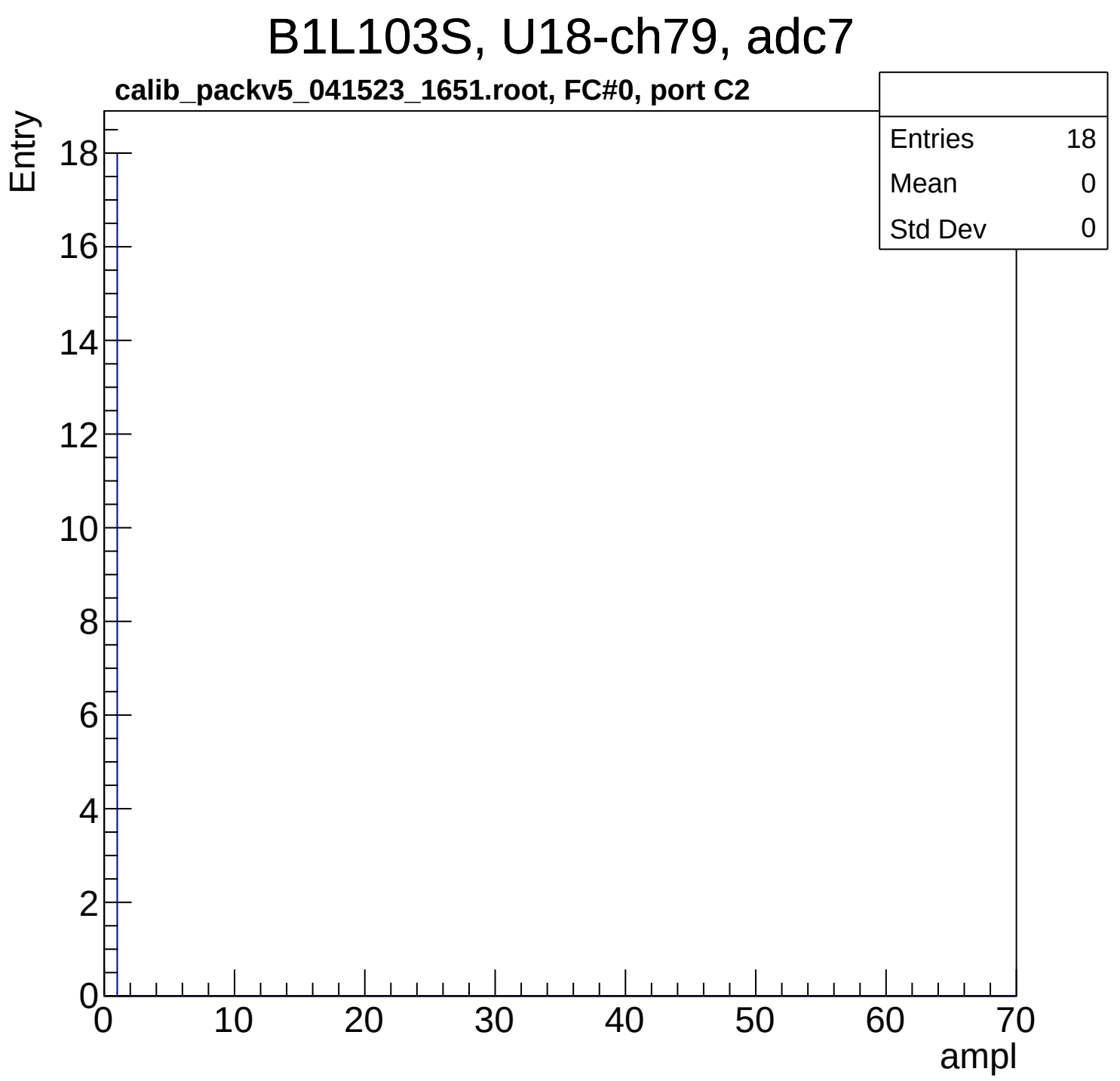
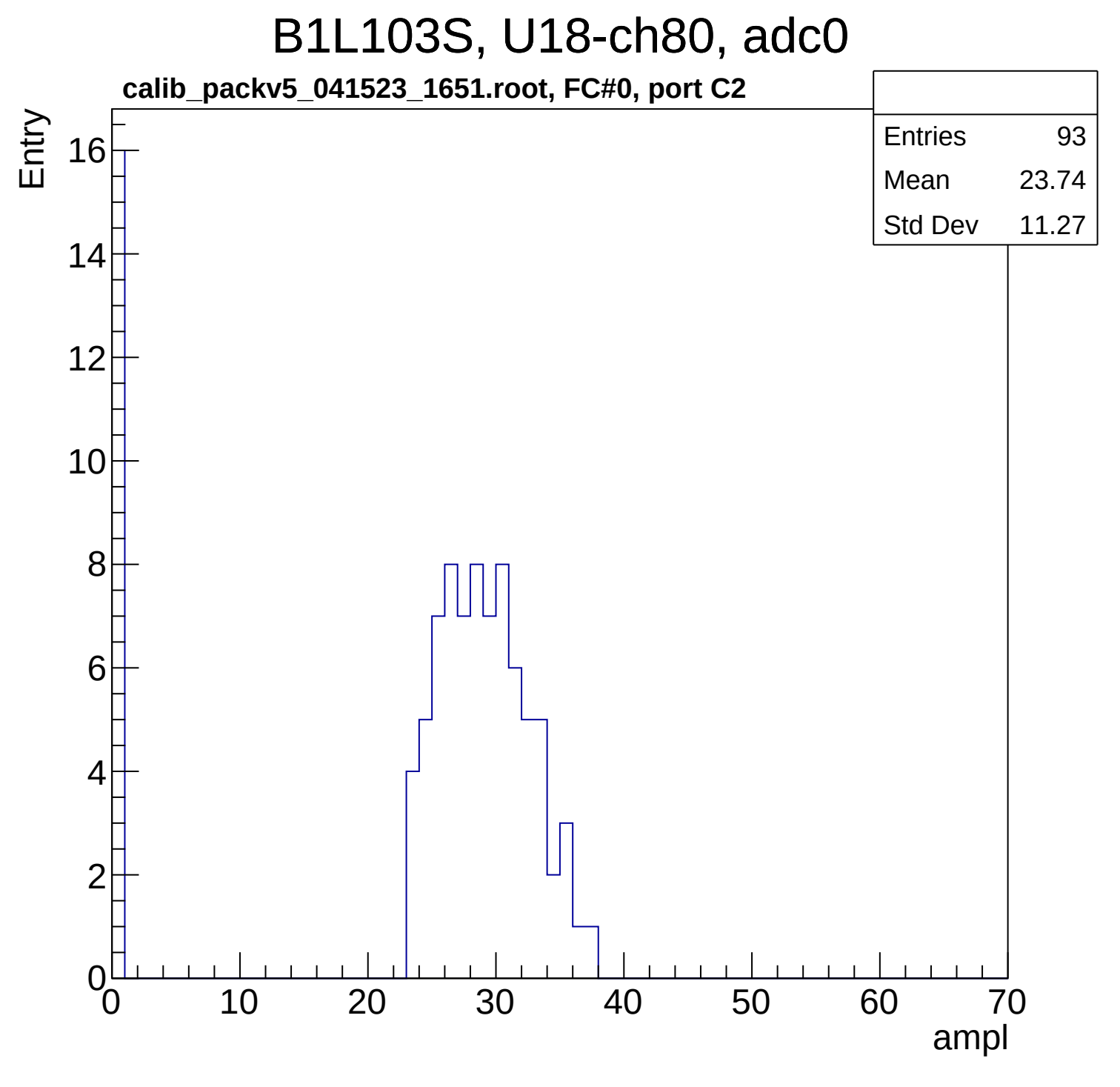

B1L103S, U18-ch79, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch80, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 93
Mean 23.74
Std Dev 11.27
Entry
ampl
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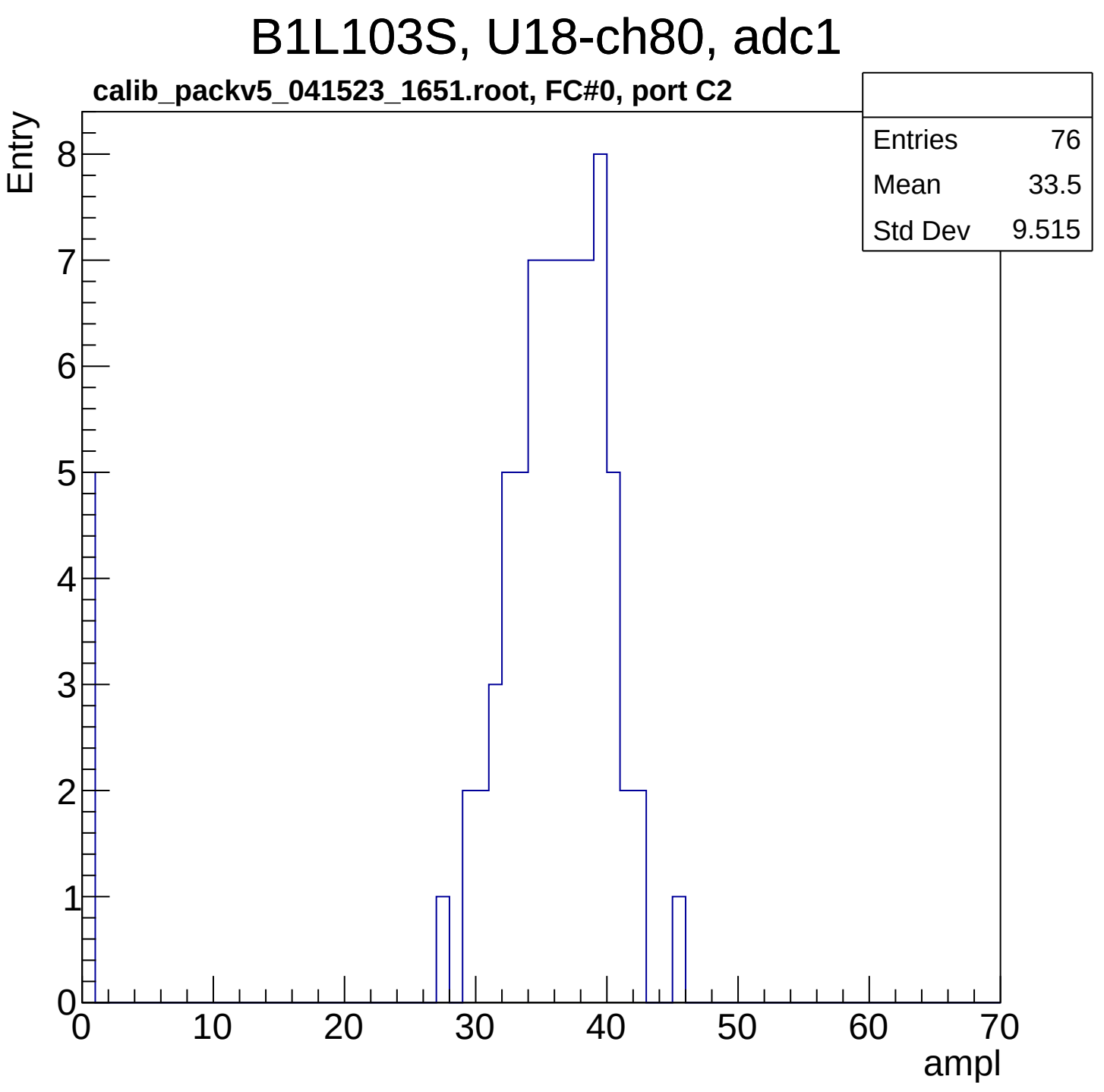
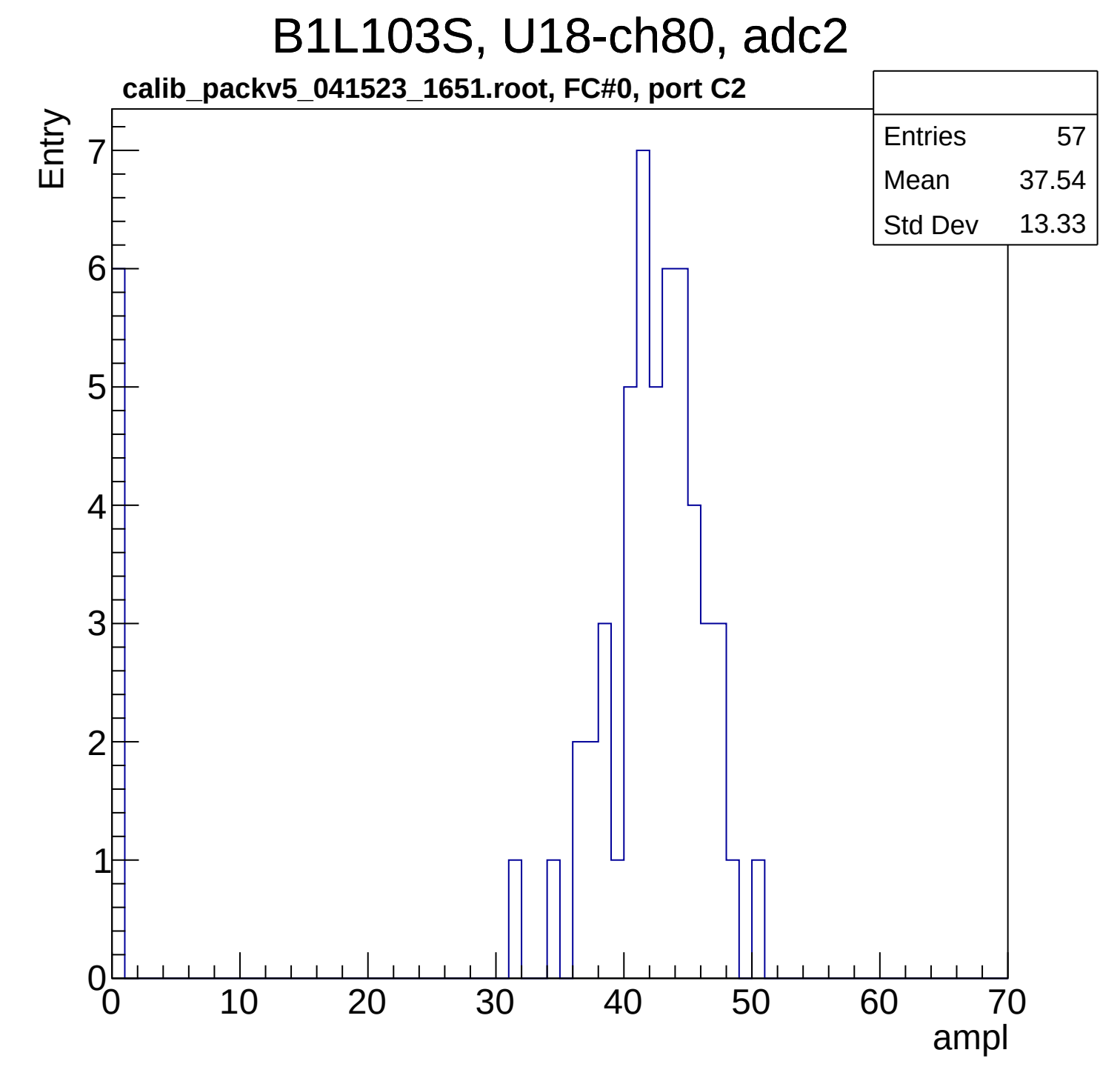
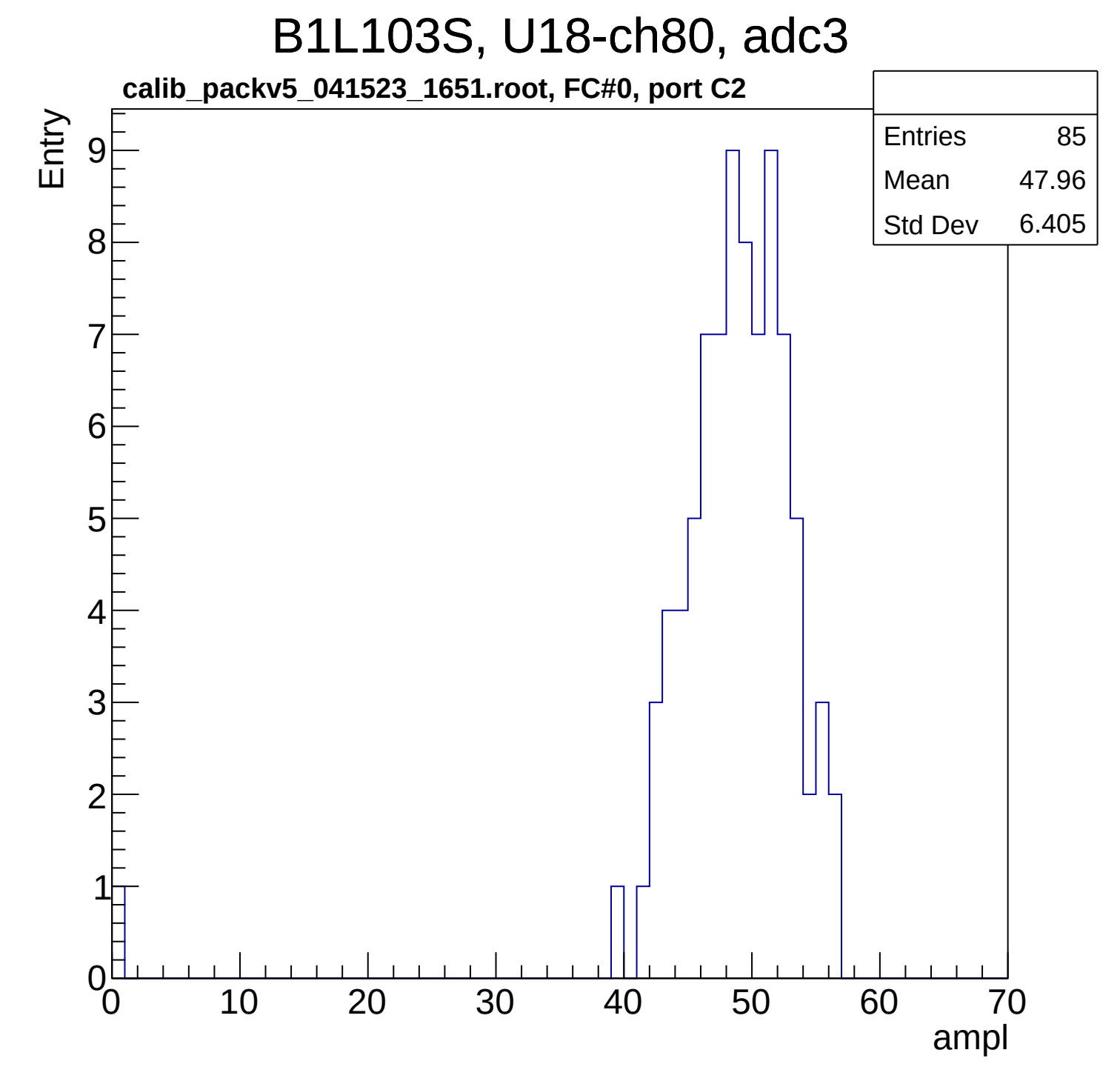
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70


B1L103S, U18-ch80, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 33.5
Std Dev 9.515
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch80, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 37.54
Std Dev 13.33
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U18-ch80, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 47.96
Std Dev 6.405
Entry
ampl
0
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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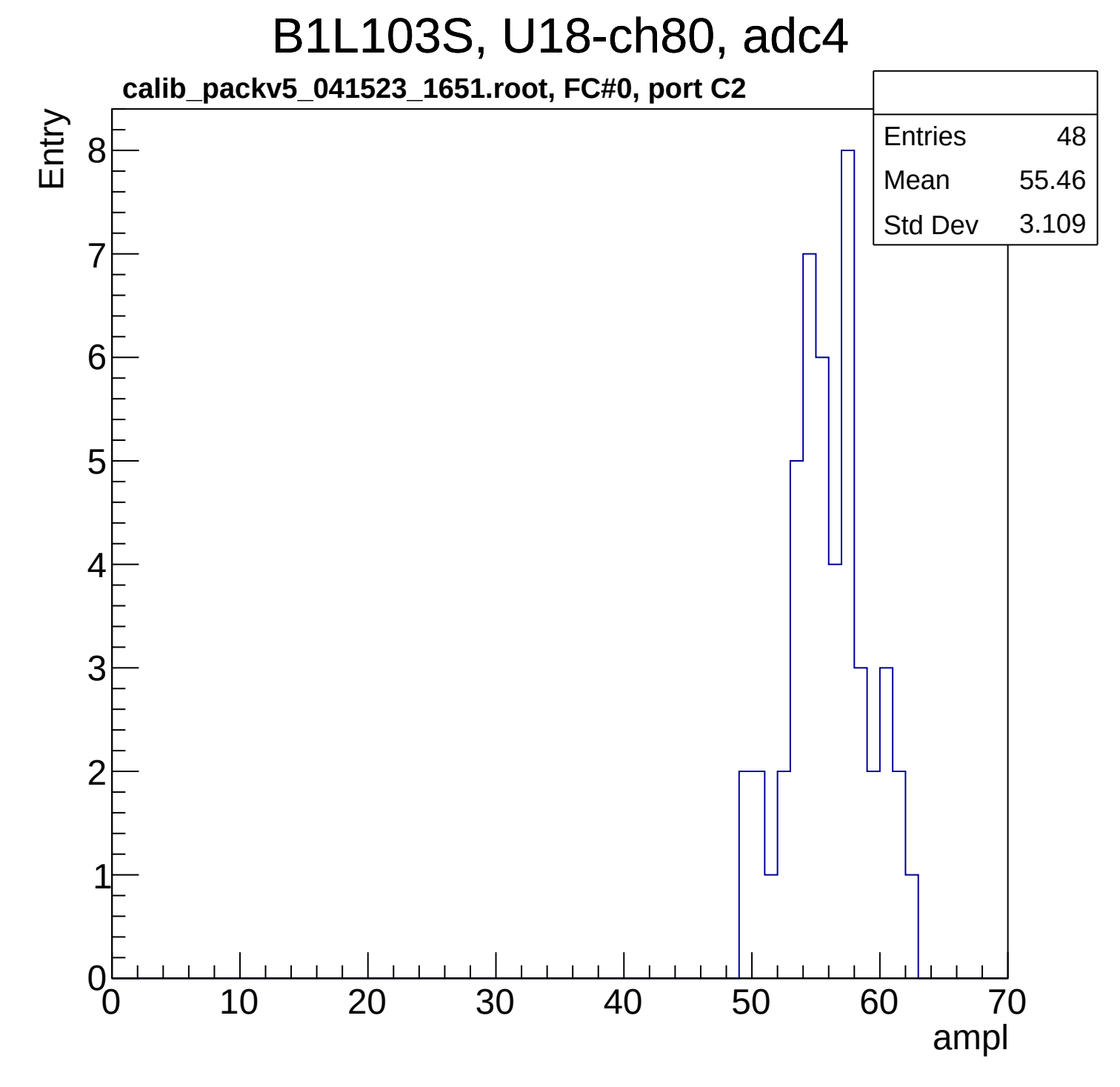
B1L103S, U18-ch80, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 55.46
Std Dev 3.109
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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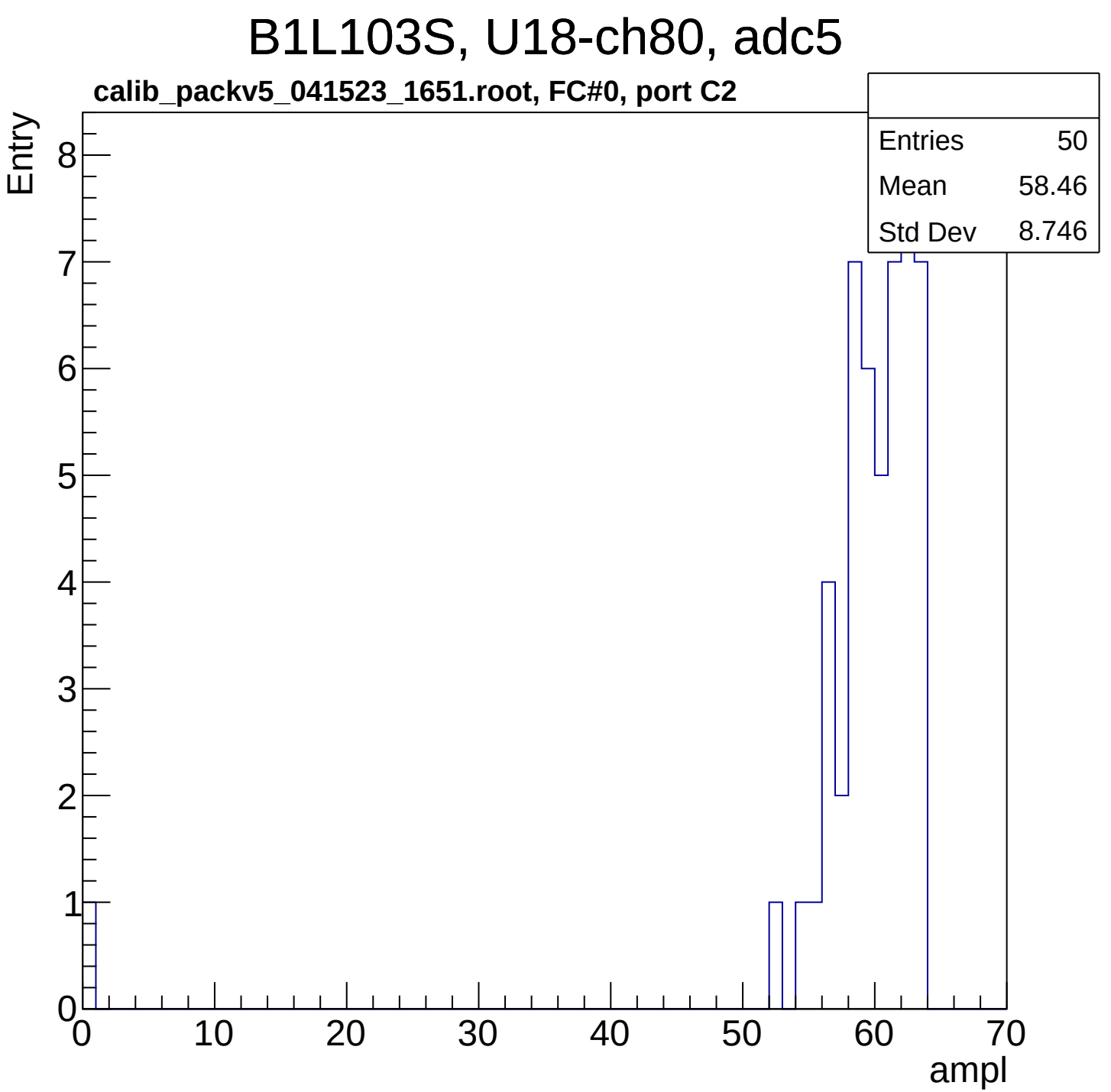
B1L103S, U18-ch80, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 58.46
Std Dev 8.746
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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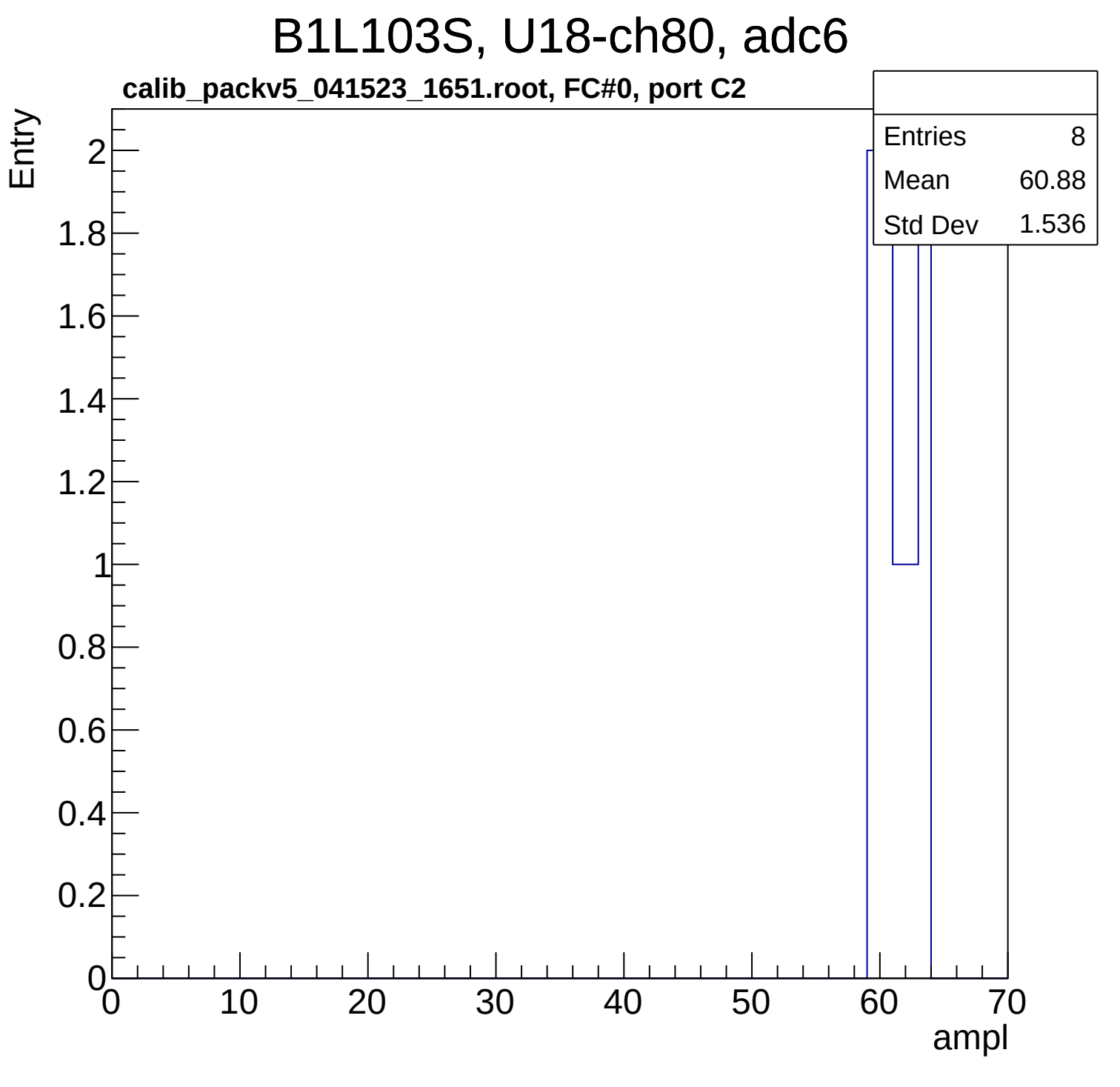
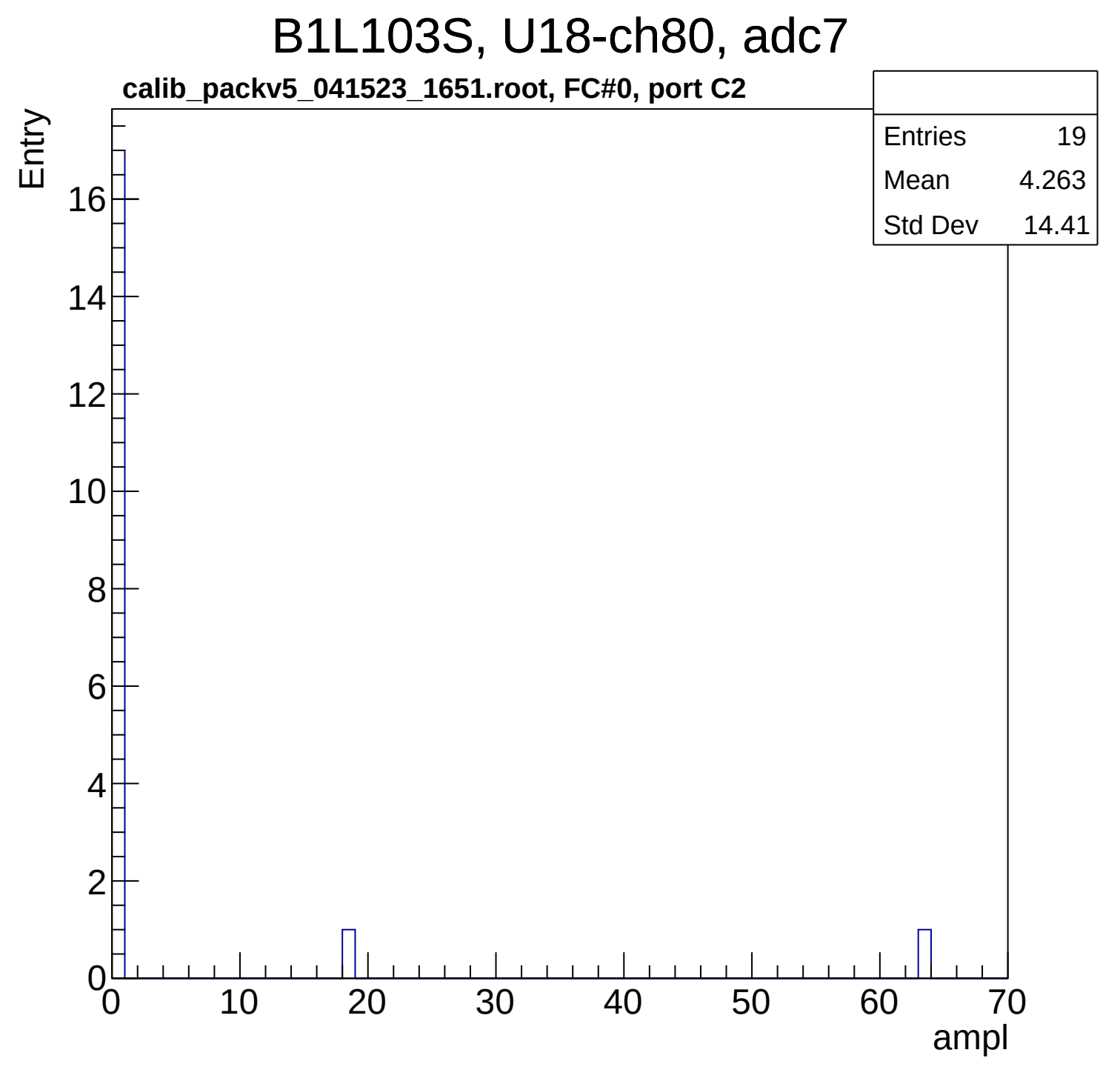
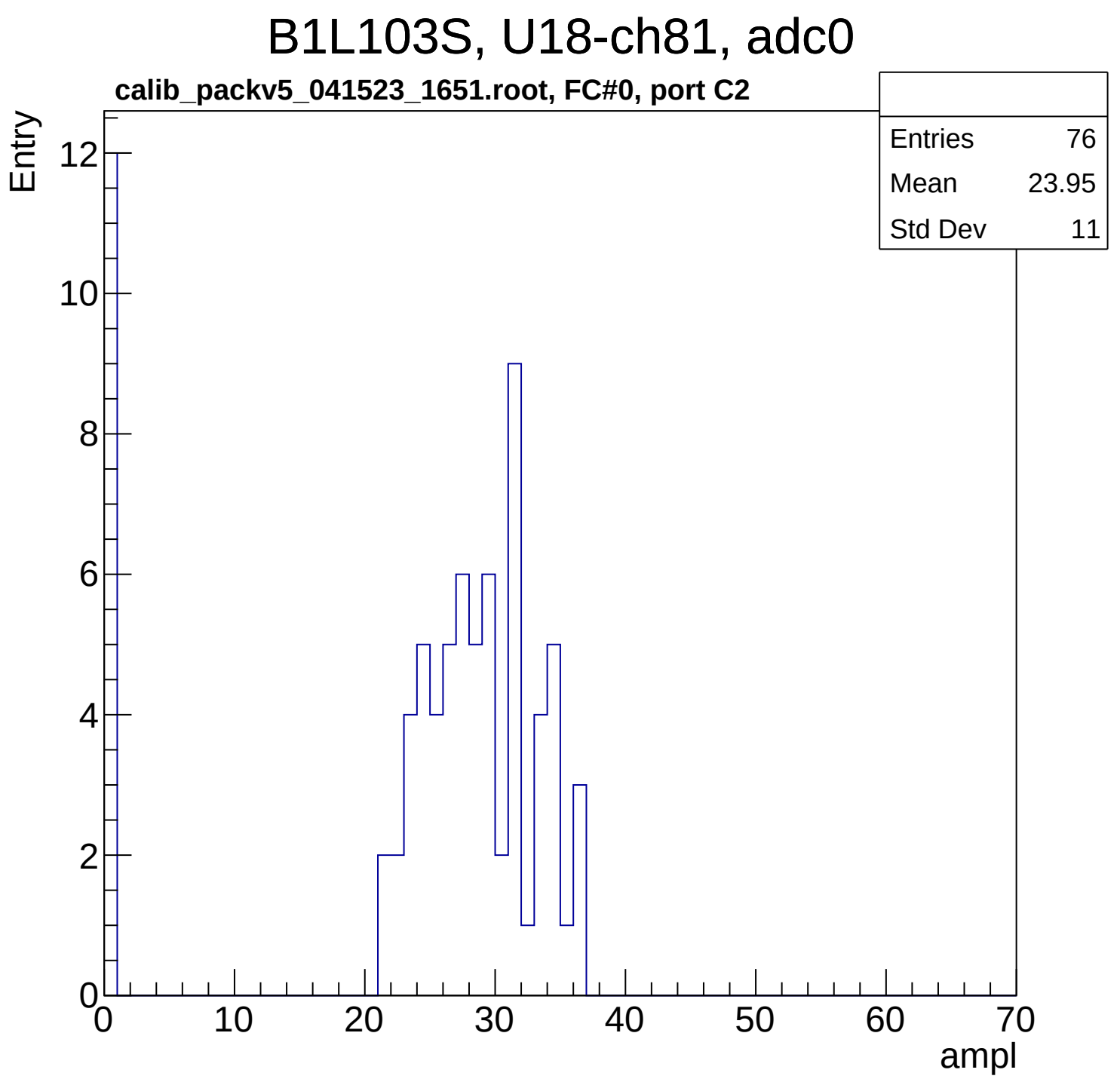
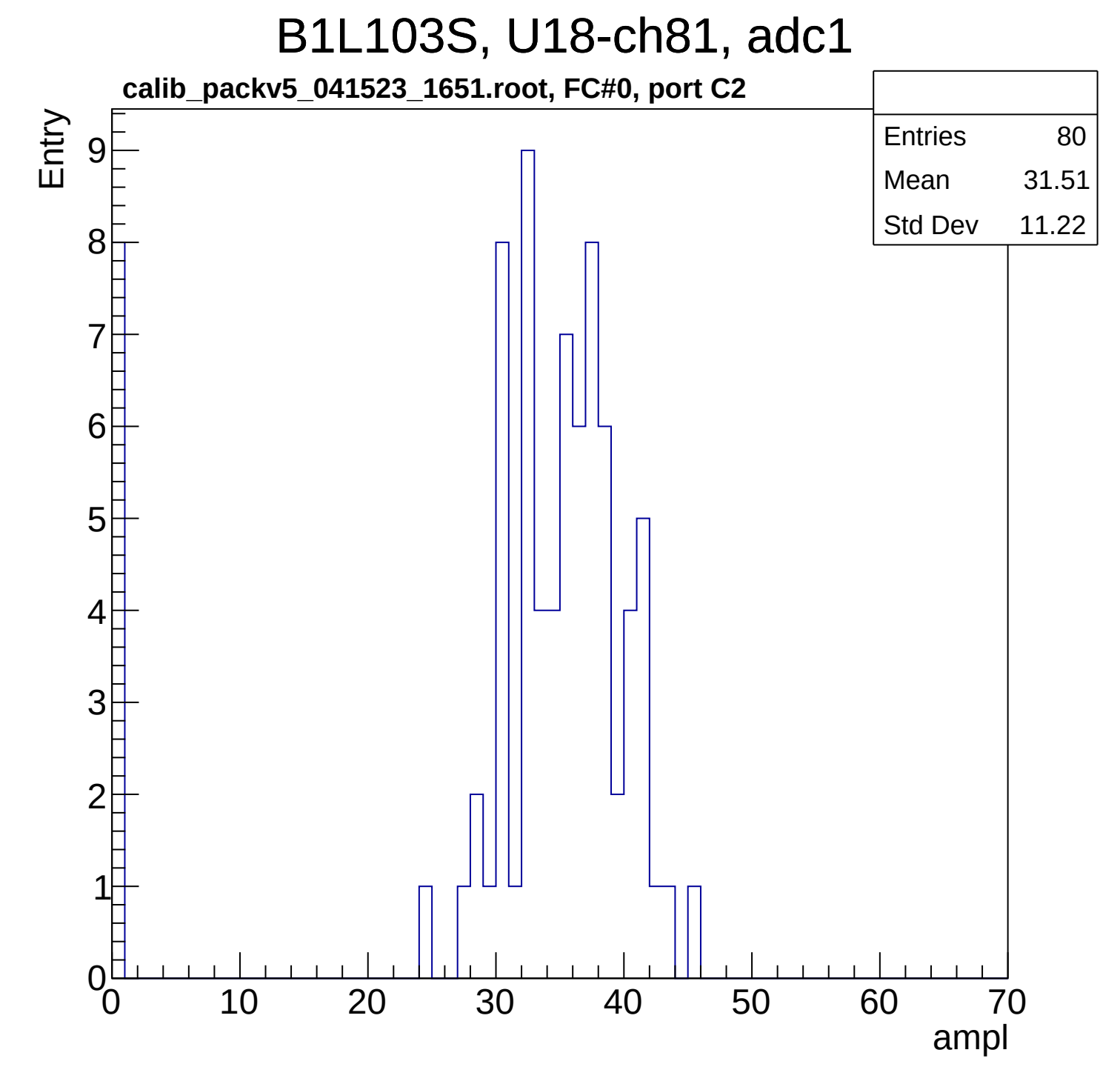

B1L103S, U18-ch80, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 60.88
Std Dev 1.536
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U18-ch80, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 4.263
Std Dev 14.41
Entry
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch81, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 23.95
Std Dev 11
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch81, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 31.51
Std Dev 11.22
Entry
ampl
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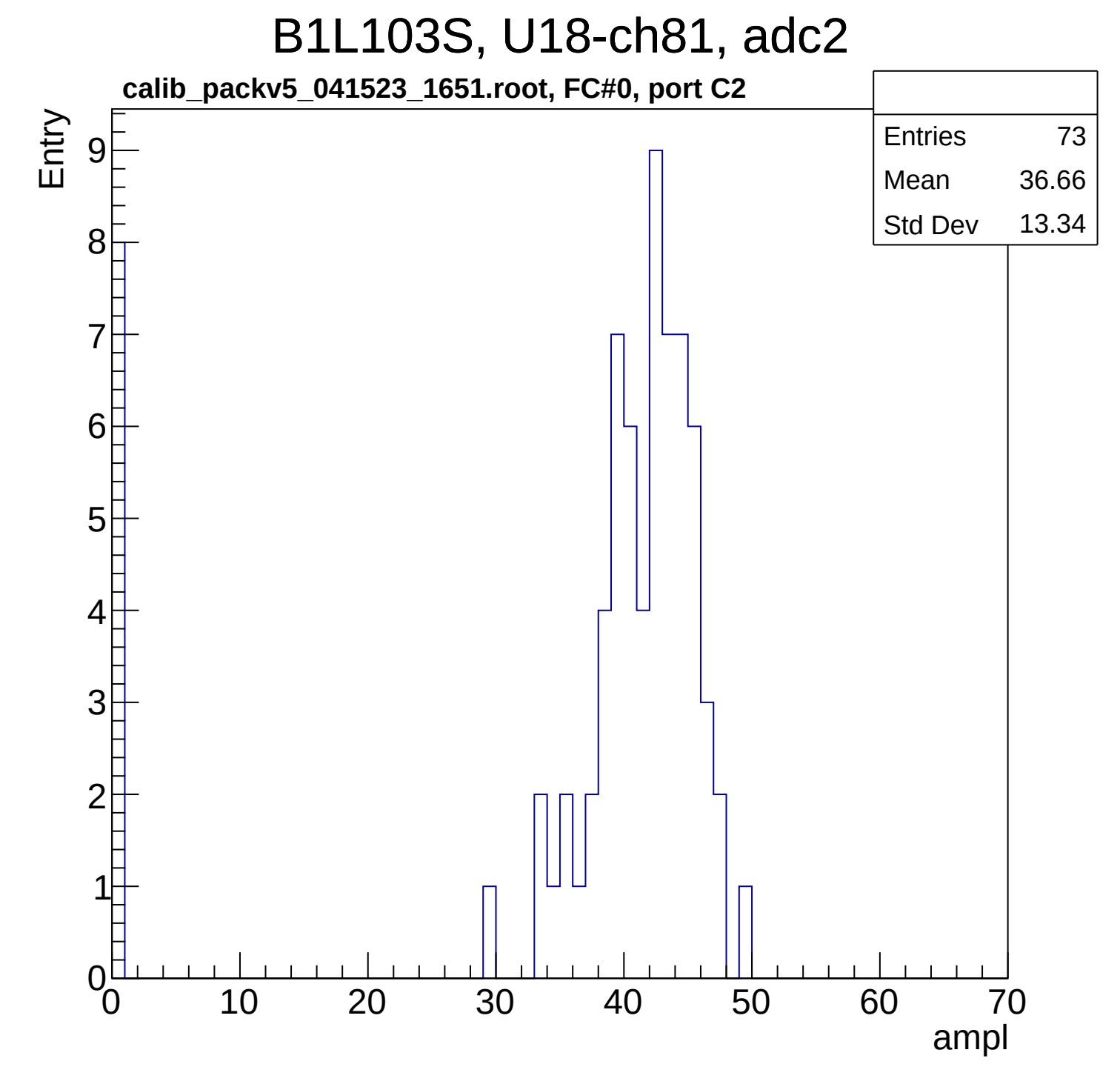
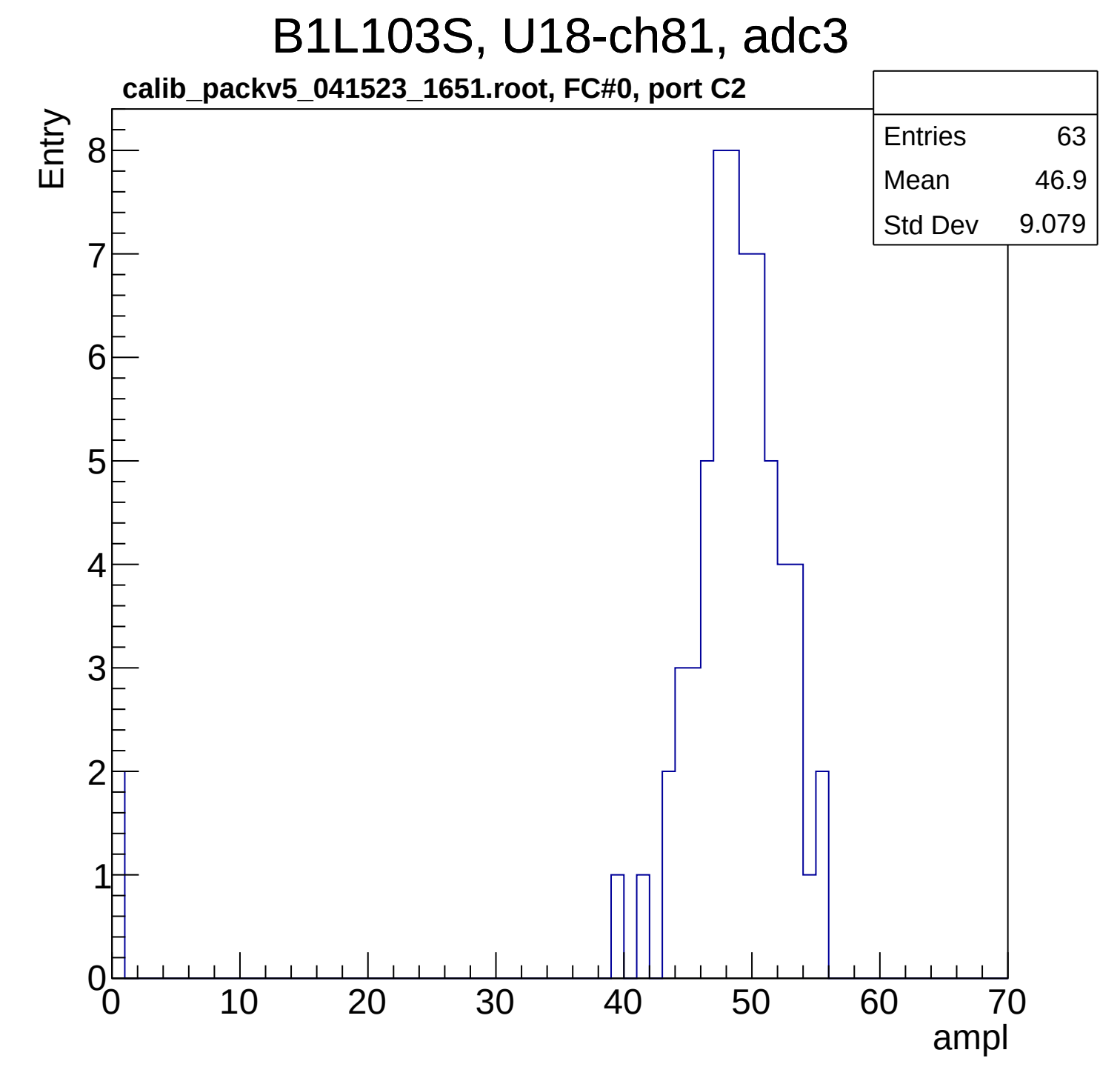
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U18-ch81, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 36.66
Std Dev 13.34
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U18-ch81, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 46.9
Std Dev 9.079
Entry
ampl
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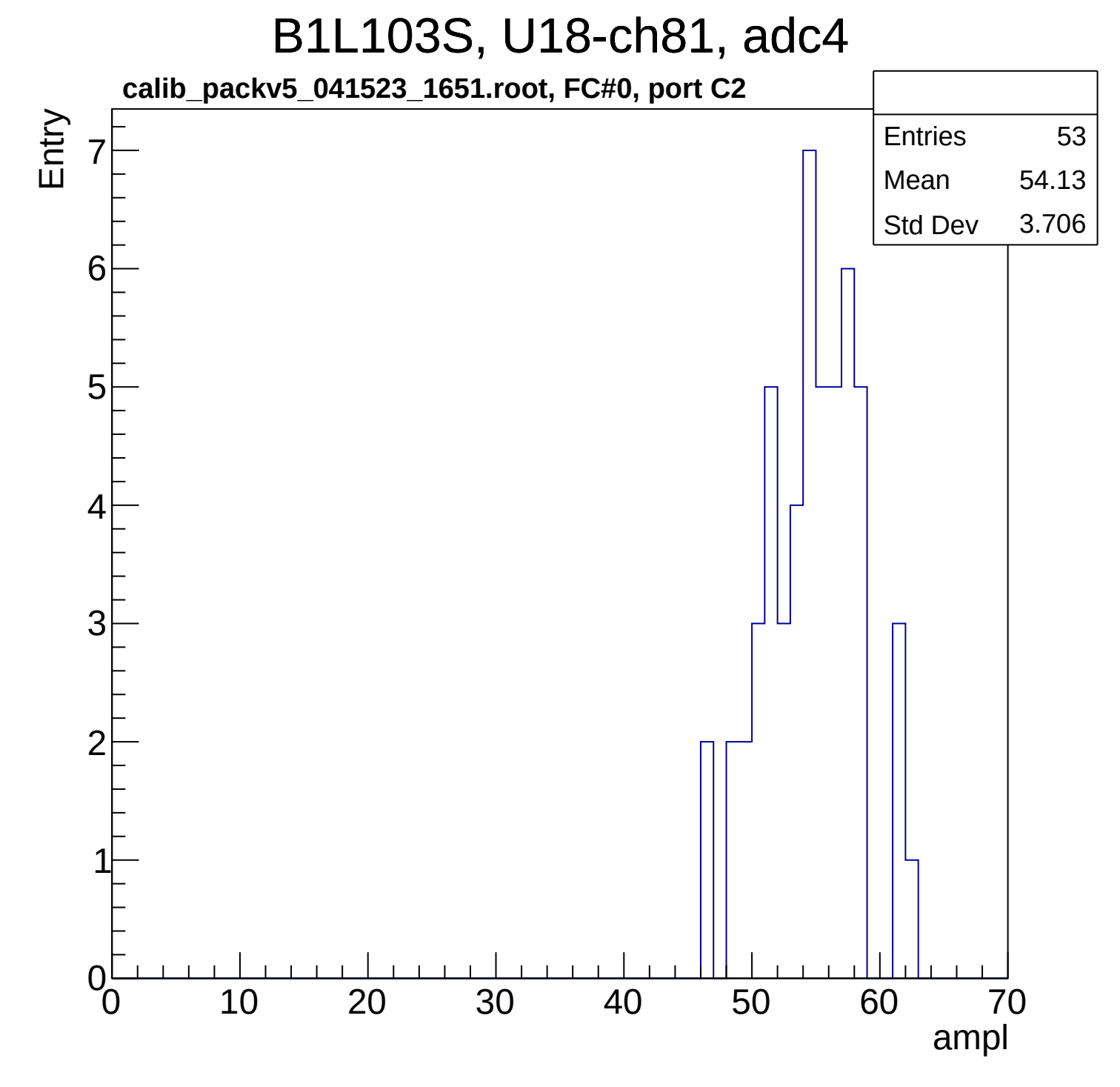
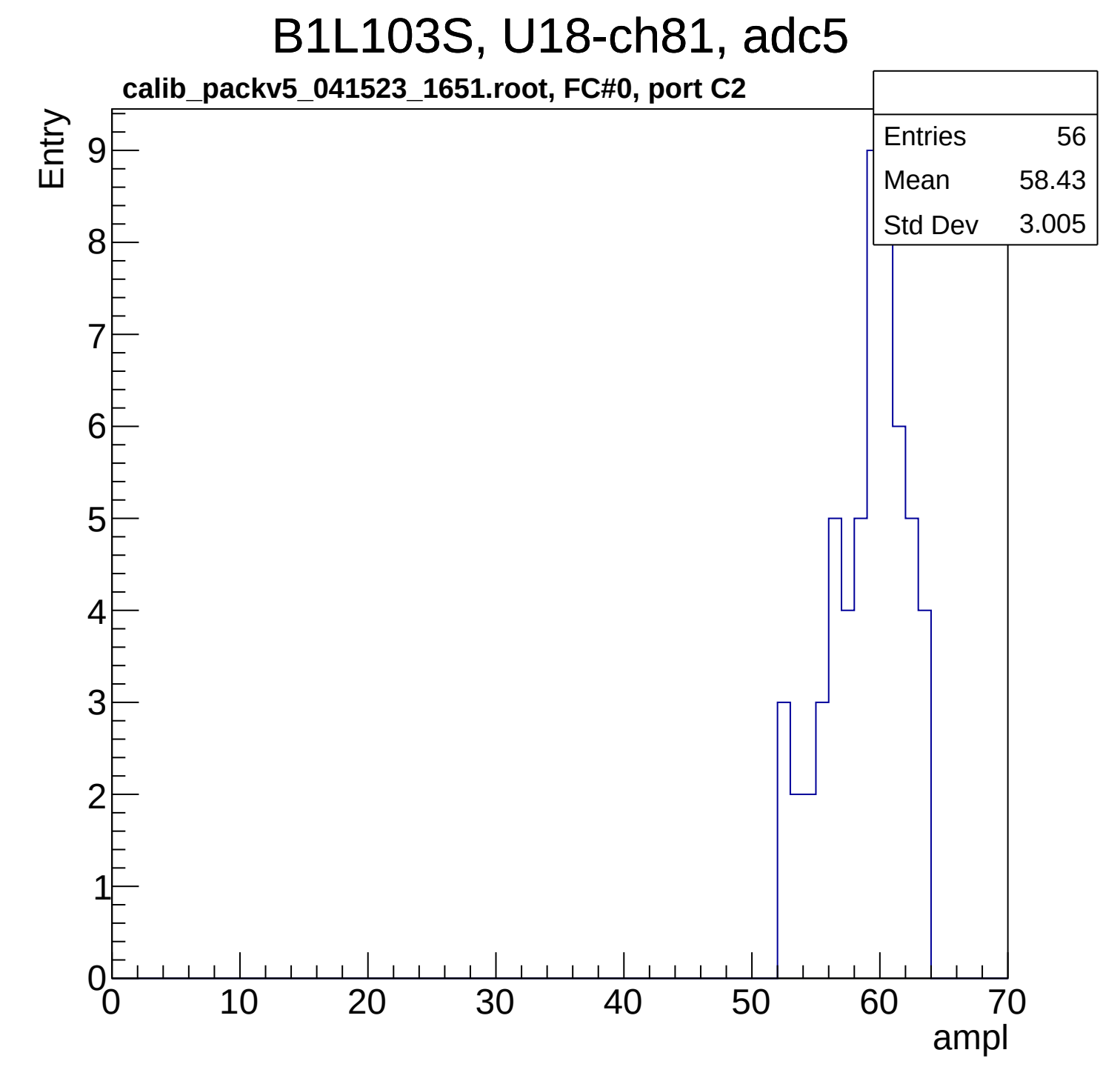
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch81, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 54.13
Std Dev 3.706
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U18-ch81, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 58.43
Std Dev 3.005
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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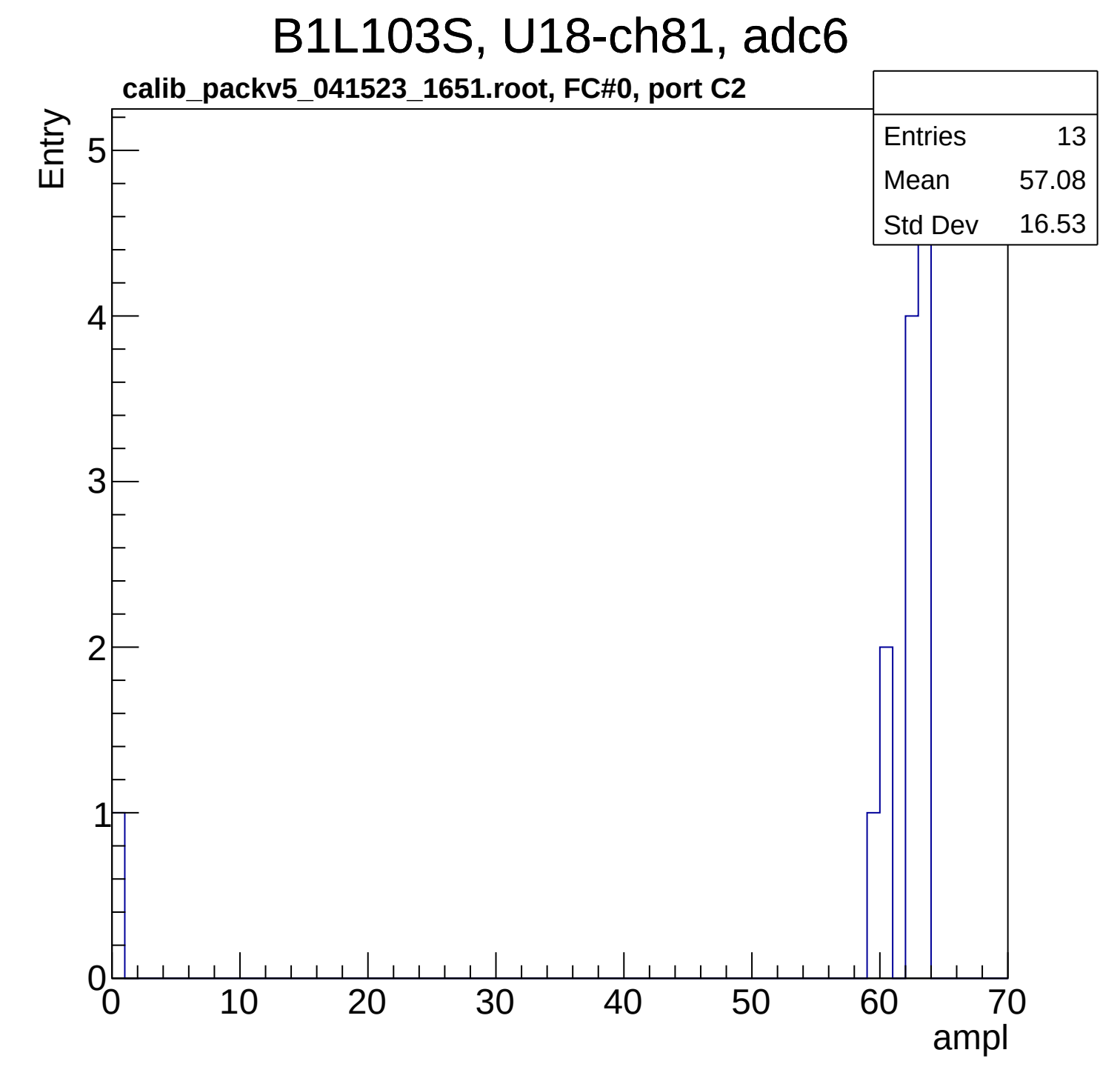
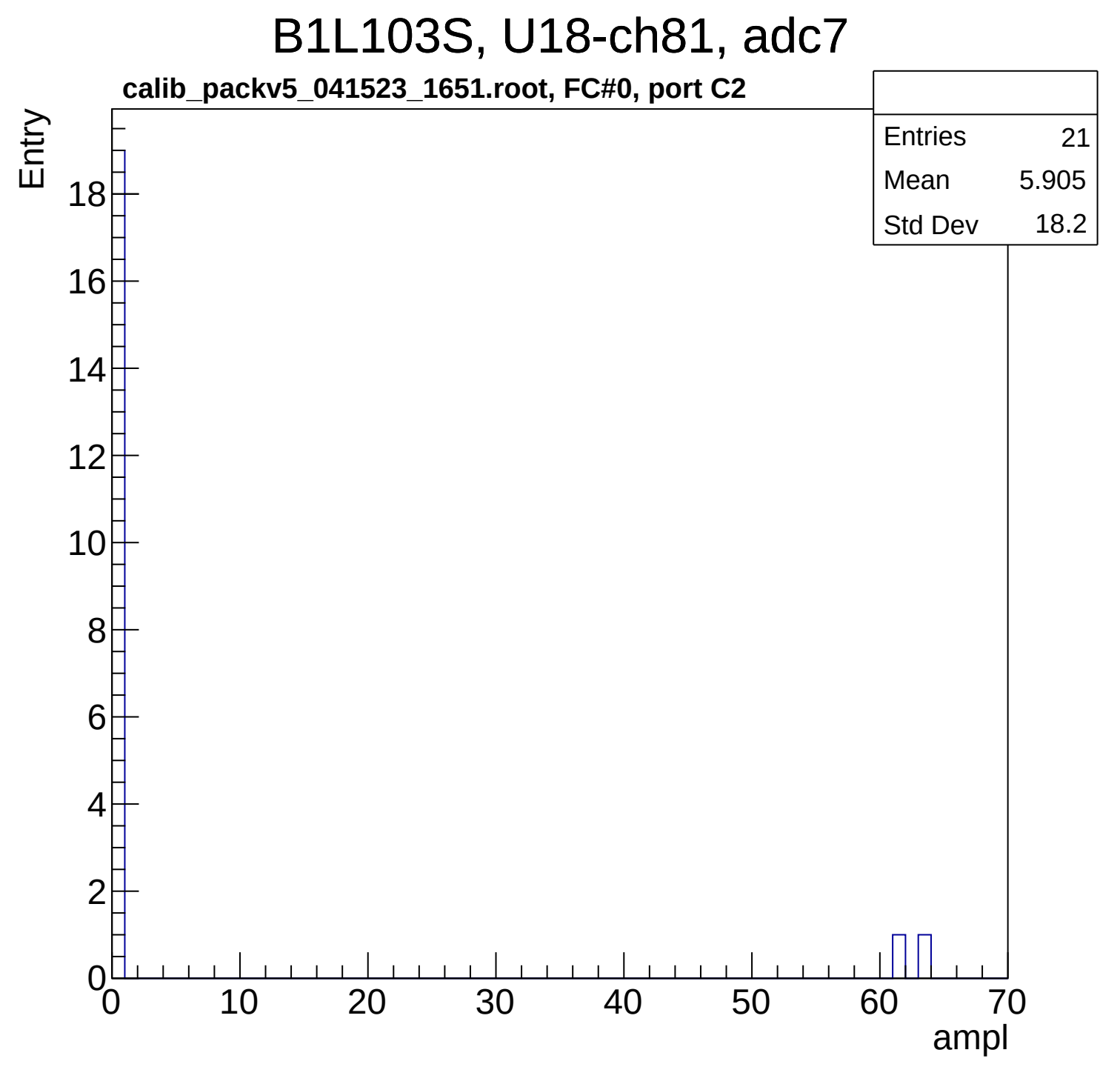
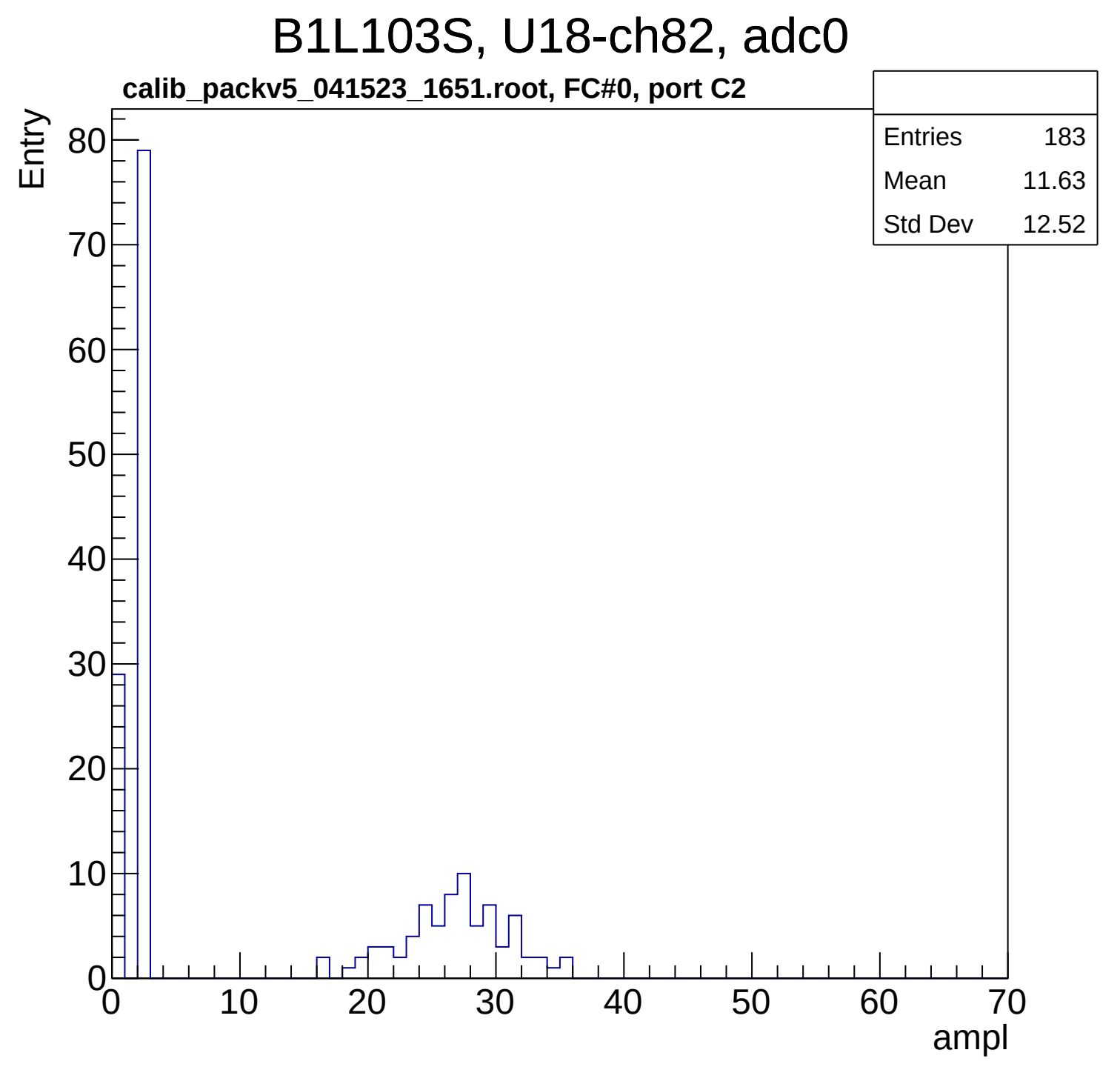

B1L103S, U18-ch81, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 13
Mean 57.08
Std Dev 16.53
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U18-ch81, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 5.905
Std Dev 18.2
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch82, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 183
Mean 11.63
Std Dev 12.52
Entry
ampl
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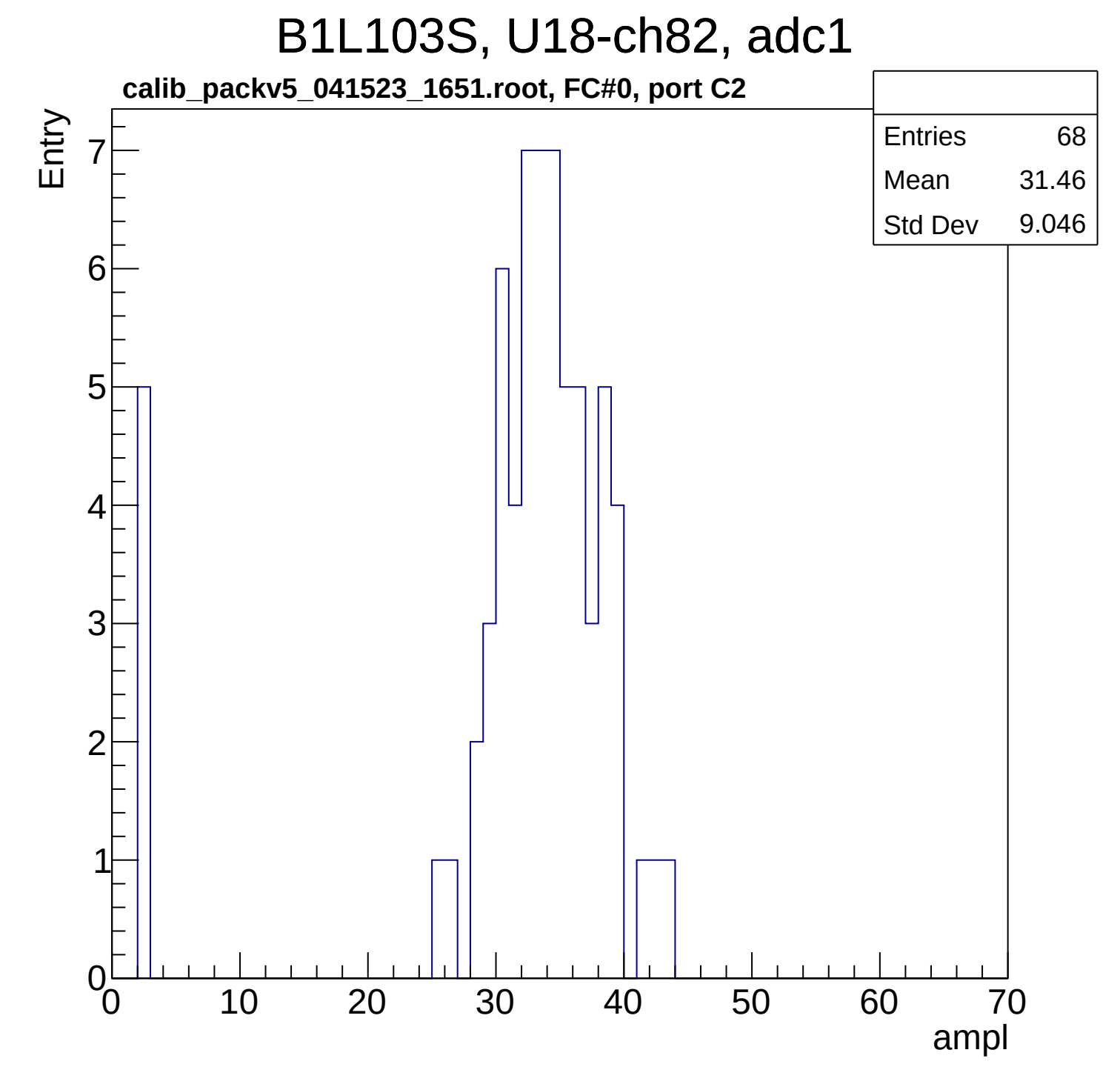
10
20
30
40
50
60
70
80


B1L103S, U18-ch82, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 31.46
Std Dev 9.046
Entry
ampl
0
1
2
3
4
5
6
7
0
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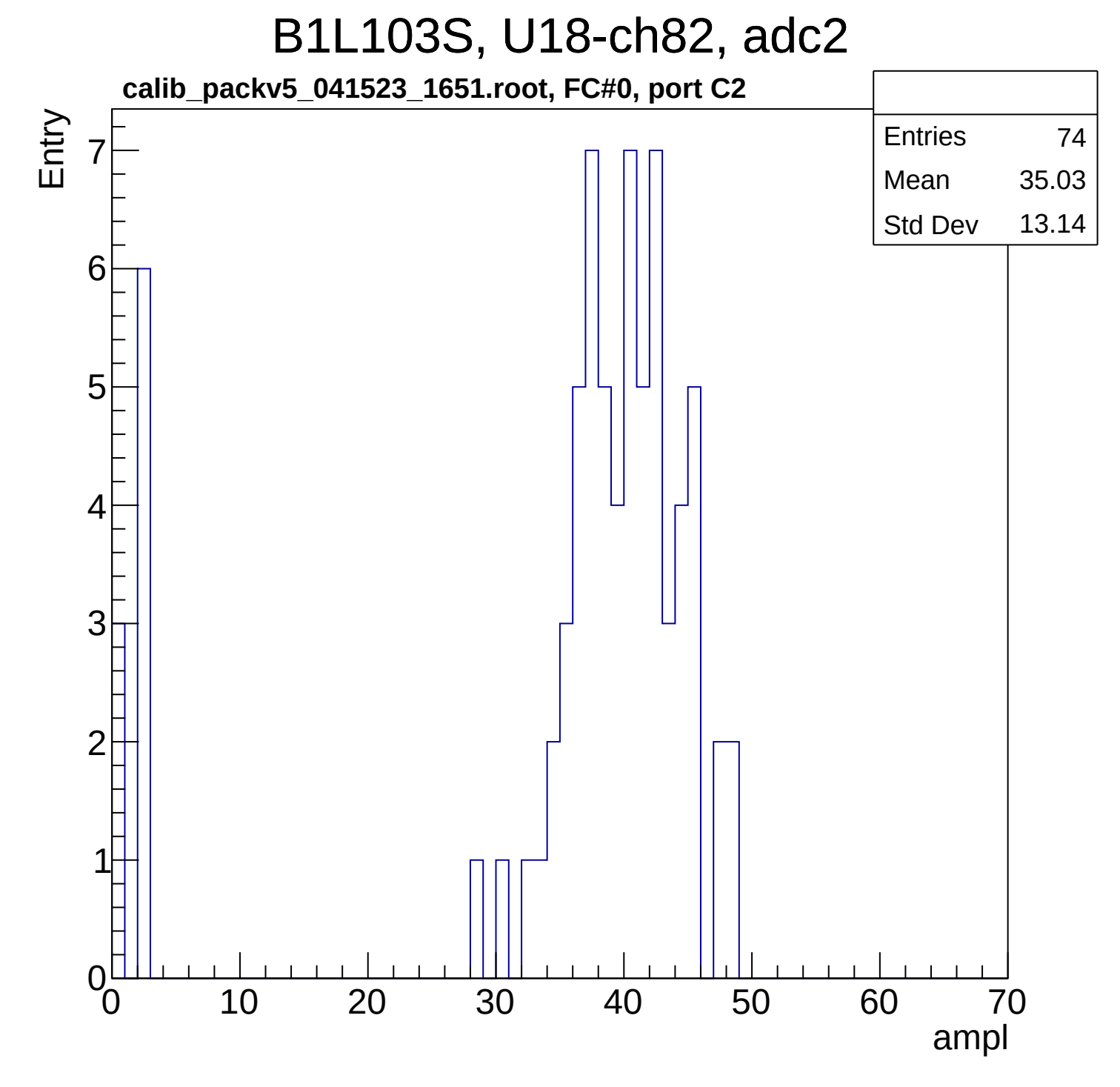
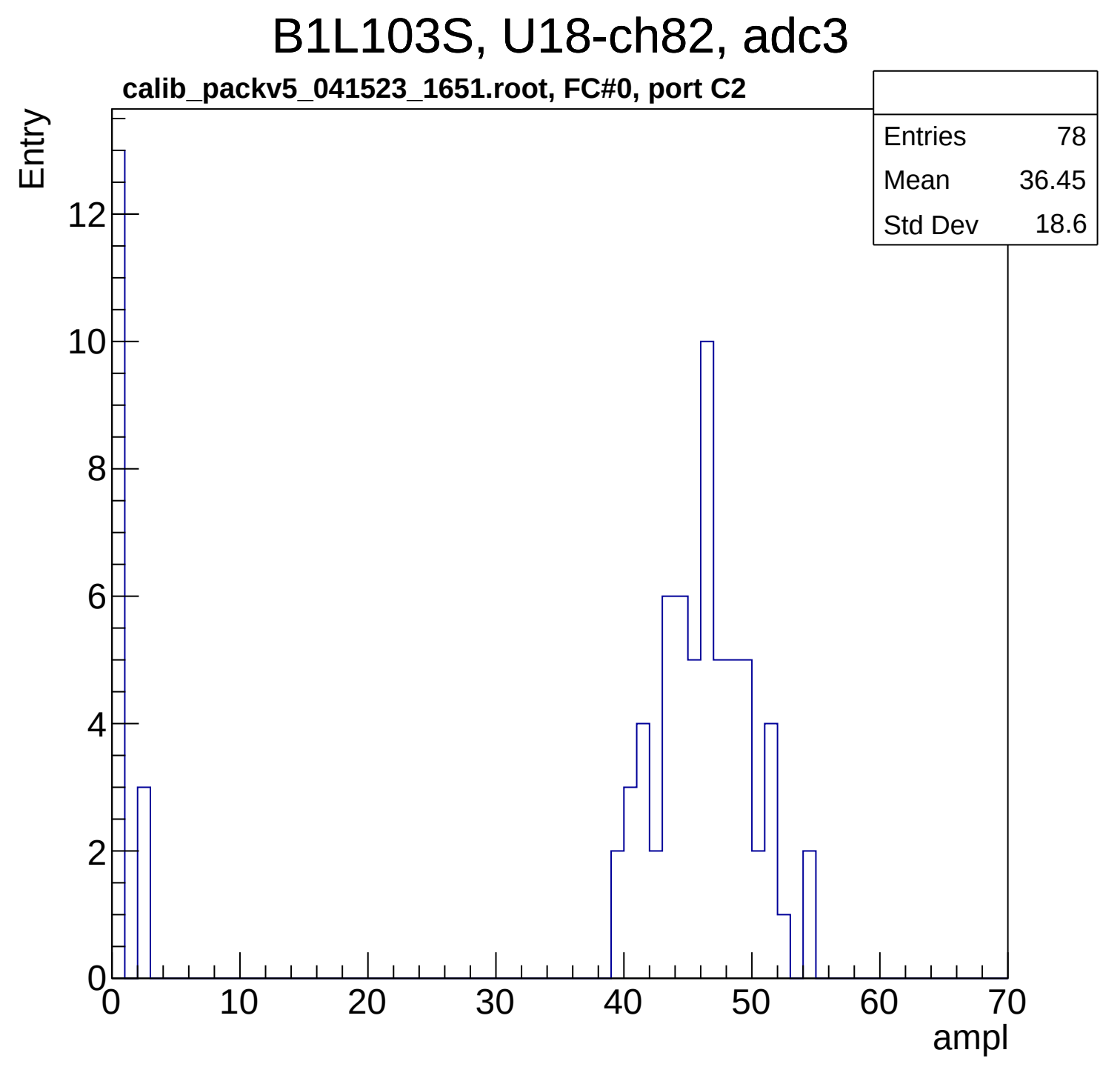
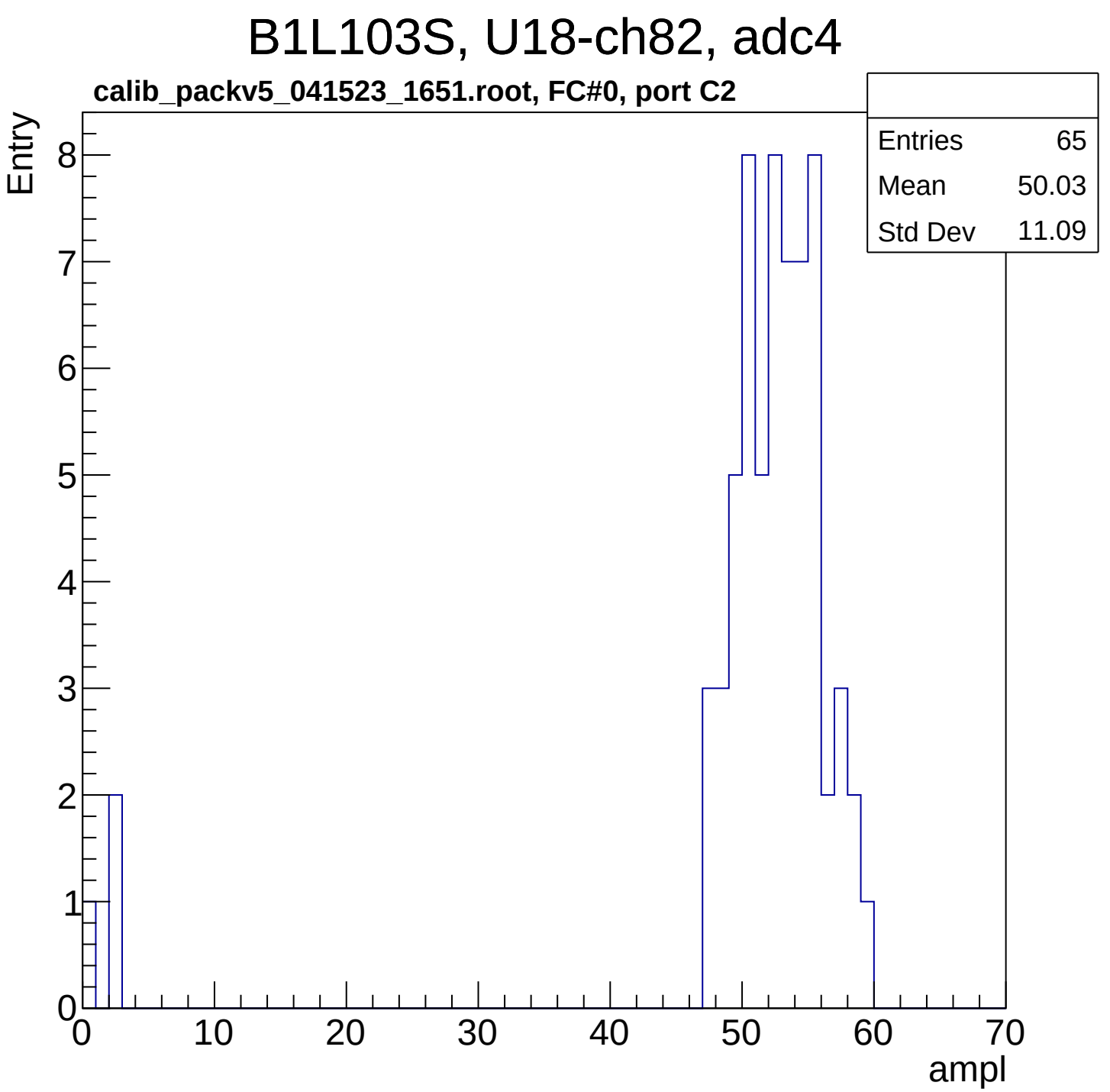
20
30
40
50
60
70


B1L103S, U18-ch82, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 35.03
Std Dev 13.14
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U18-ch82, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 36.45
Std Dev 18.6
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70


B1L103S, U18-ch82, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 50.03
Std Dev 11.09
Entry
ampl
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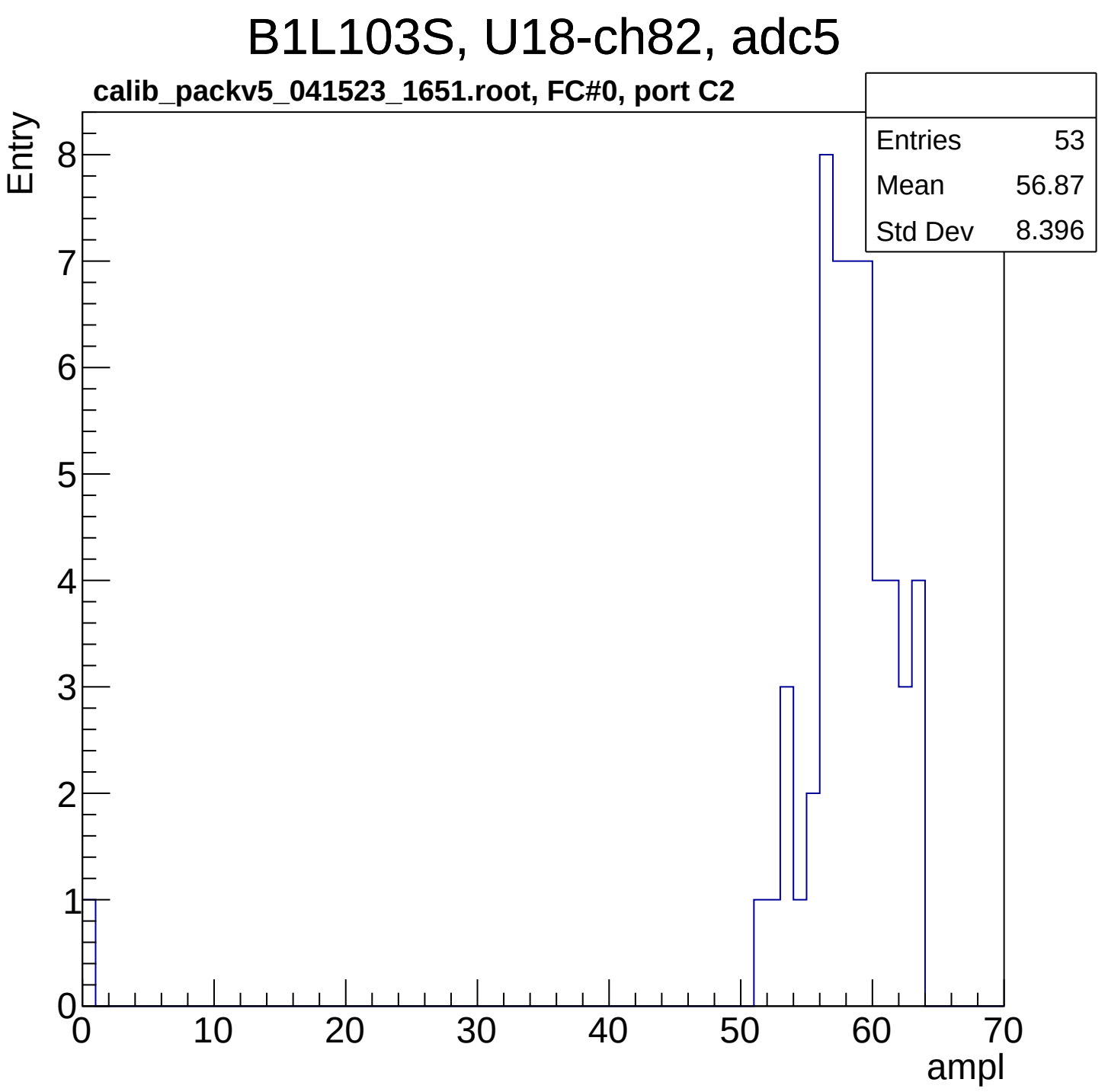
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch82, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 56.87
Std Dev 8.396
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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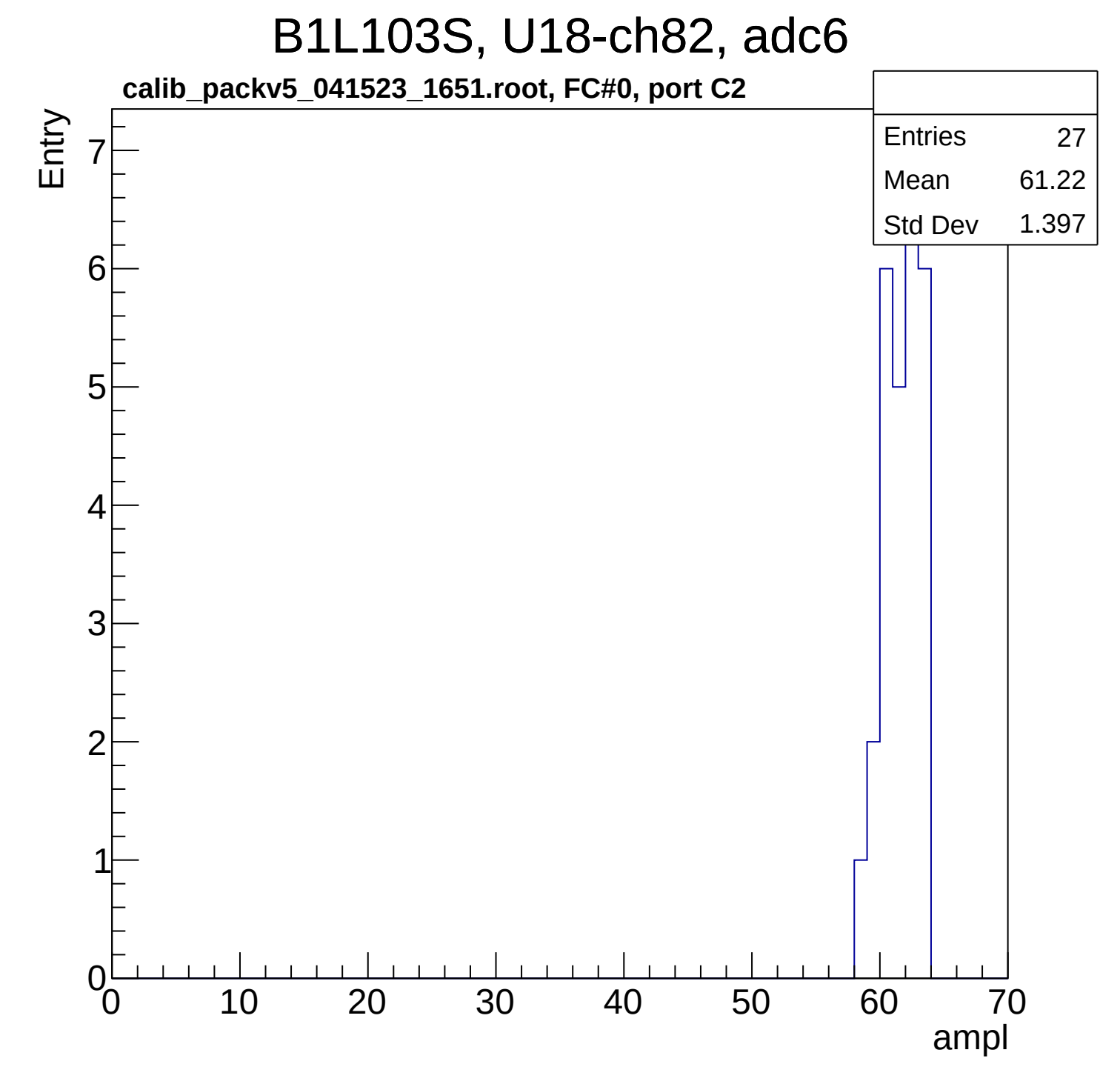
B1L103S, U18-ch82, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 27
Mean 61.22
Std Dev 1.397
Entry
ampl
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1
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6
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0
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20
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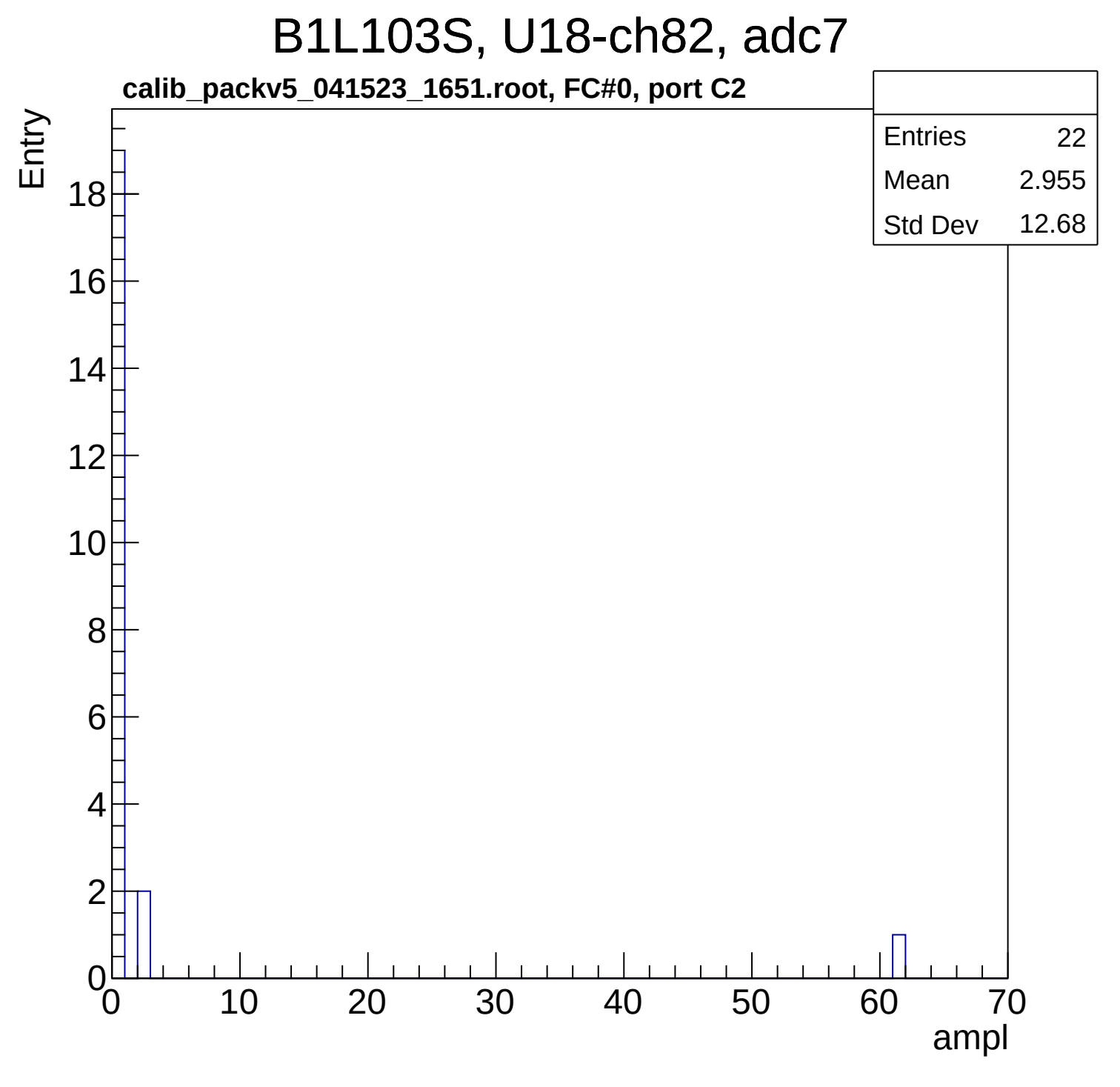
40
50
60
70


B1L103S, U18-ch82, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 2.955
Std Dev 12.68
Entry
ampl
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4
6
8
10
12
14
16
18
0
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40
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60
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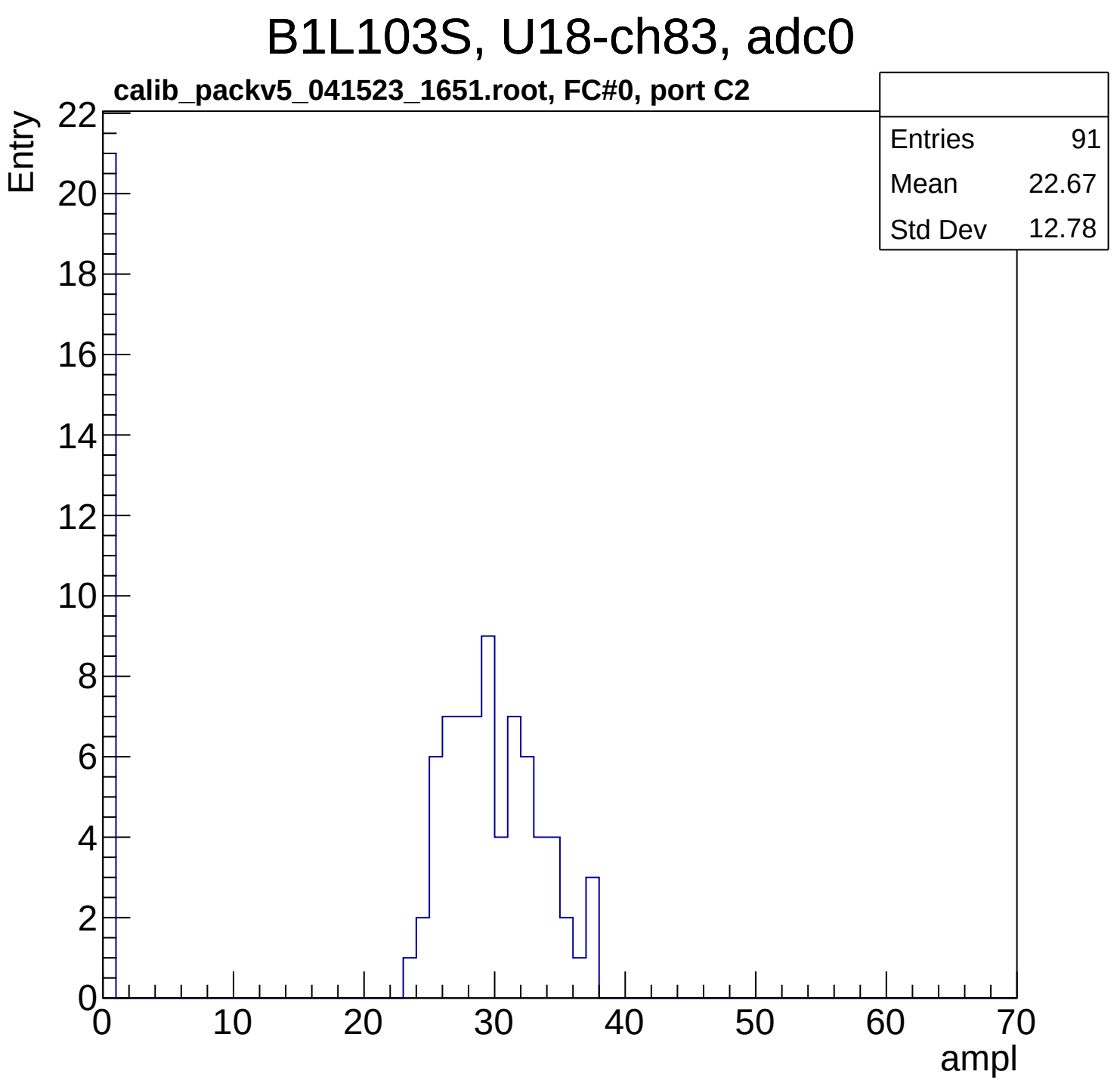
B1L103S, U18-ch83, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 91
Mean 22.67
Std Dev 12.78
Entry
ampl
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8
10
12
14
16
18
20
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0
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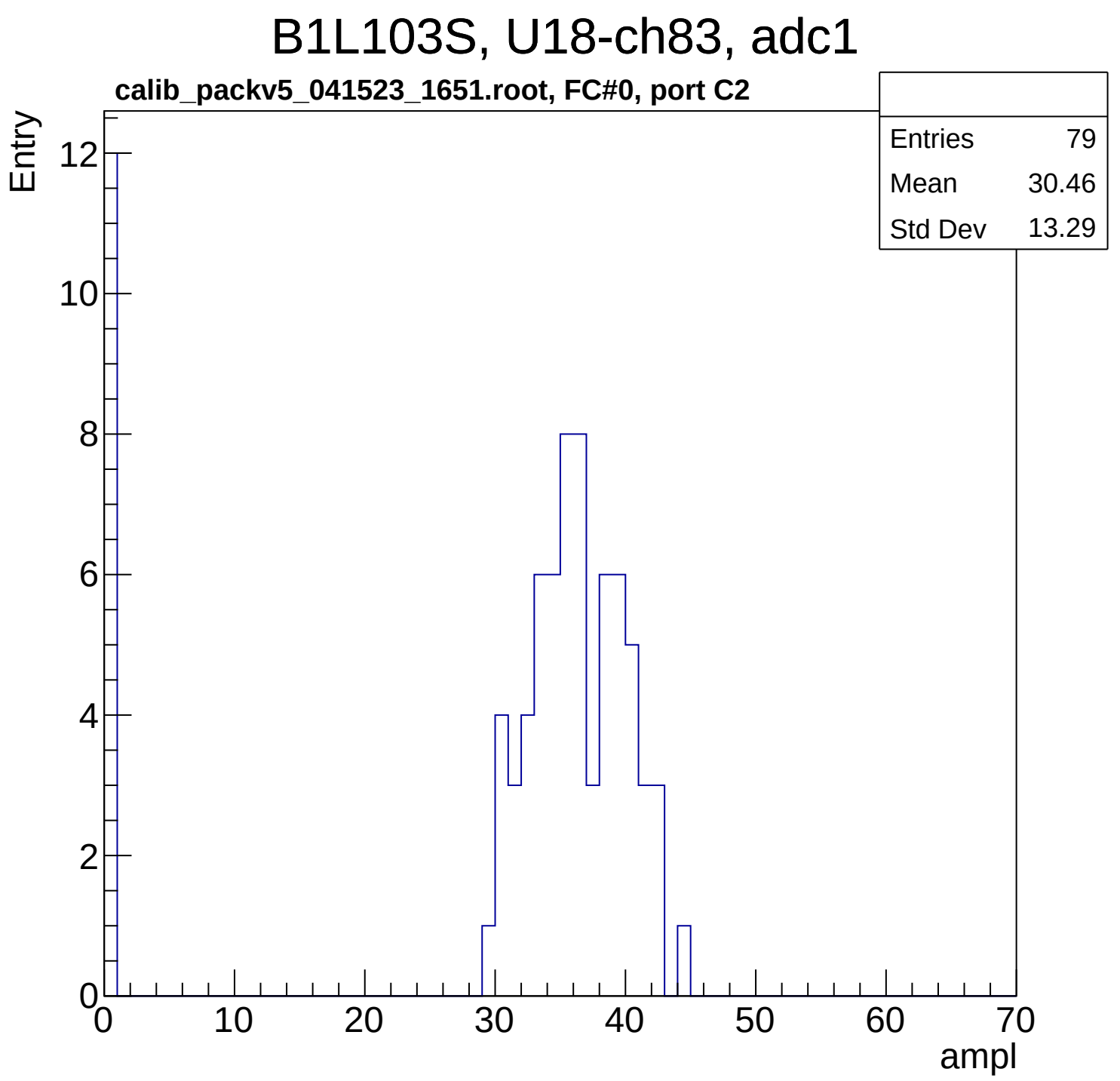
40
50
60
70


B1L103S, U18-ch83, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 30.46
Std Dev 13.29
Entry
0
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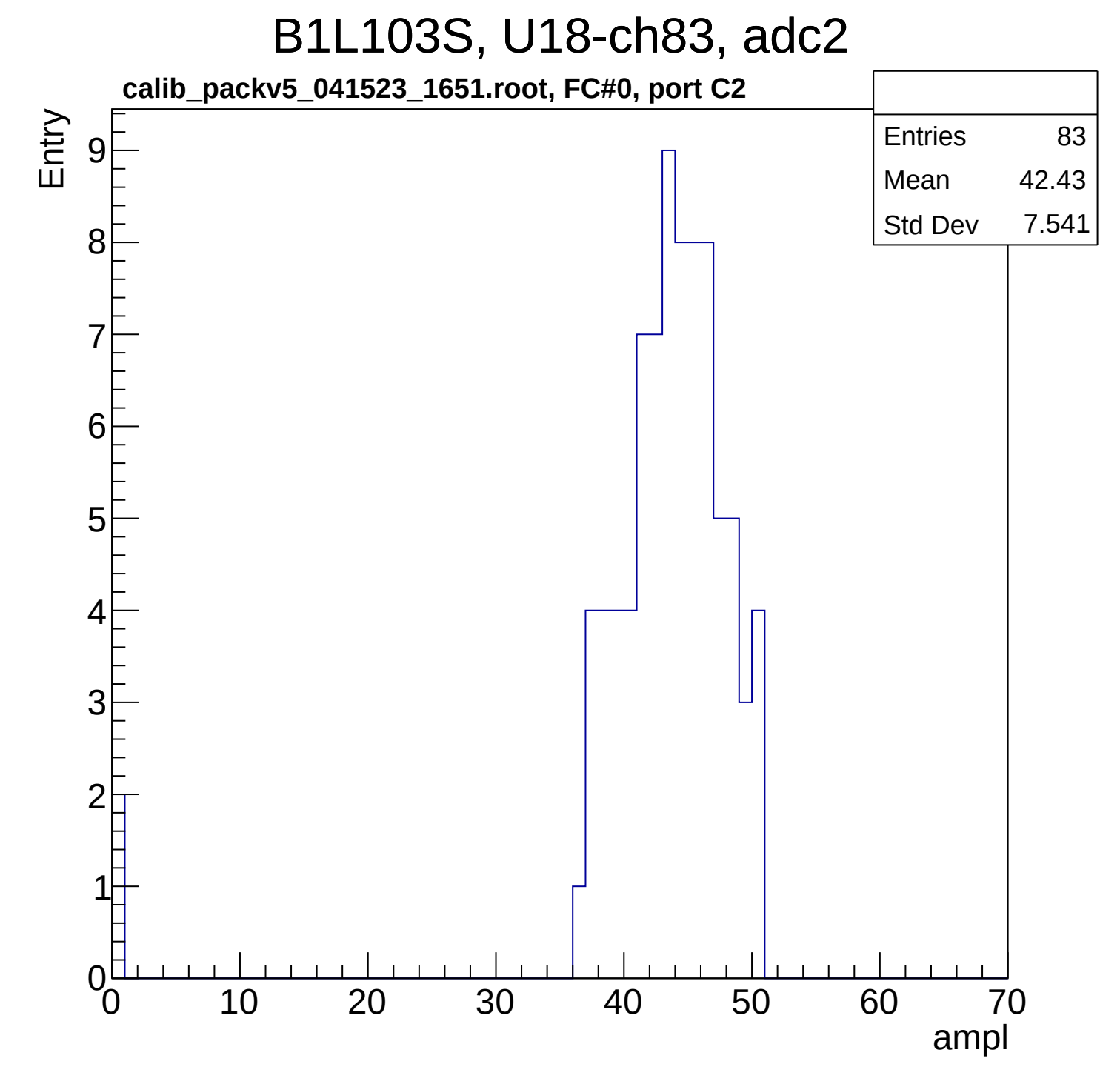
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch83, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 42.43
Std Dev 7.541
Entry
ampl
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20
30
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50
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2
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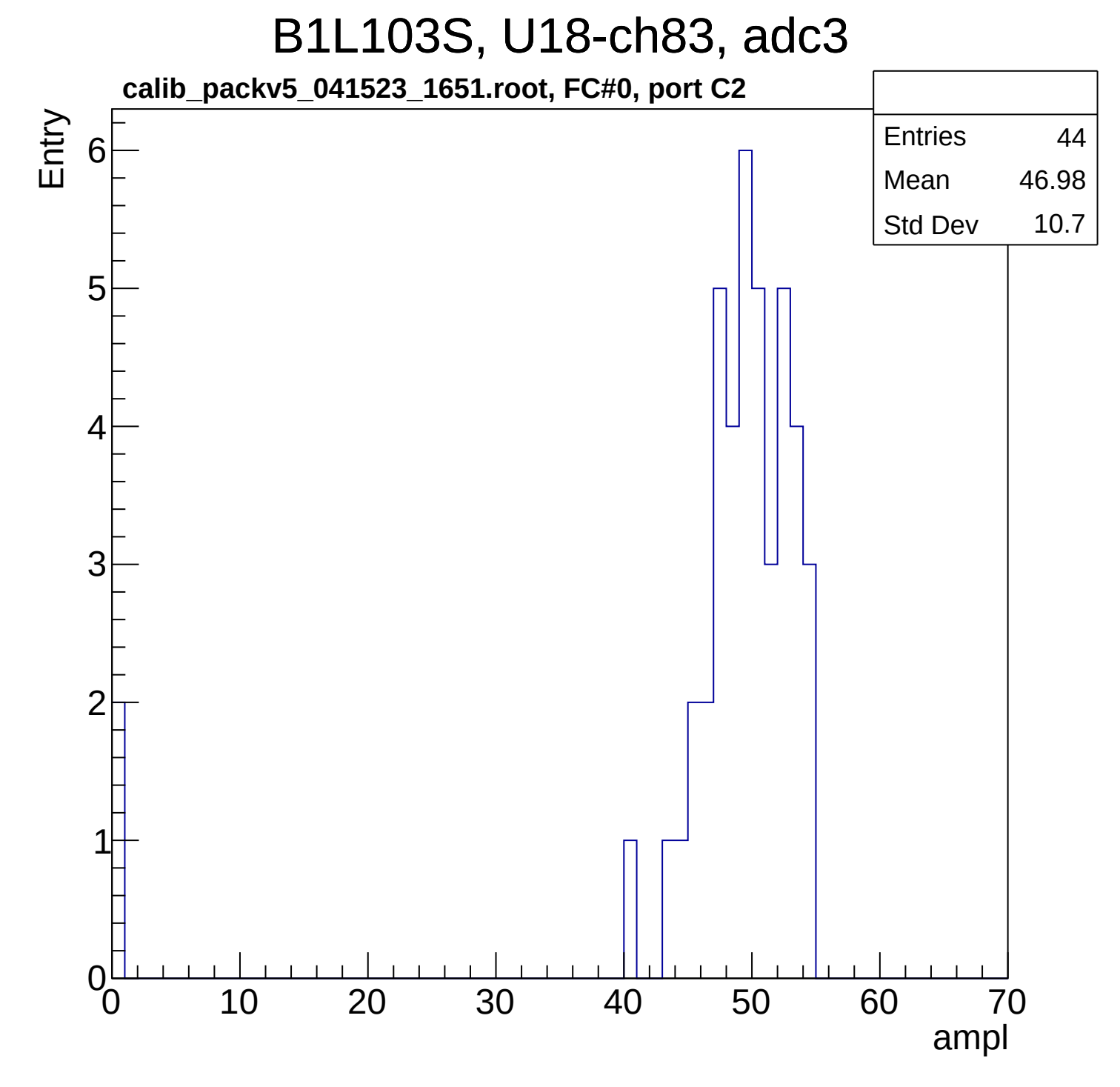
6
7
8
9


B1L103S, U18-ch83, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 46.98
Std Dev 10.7
Entry
ampl
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1
2
3
4
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6
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10
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30
40
50
60
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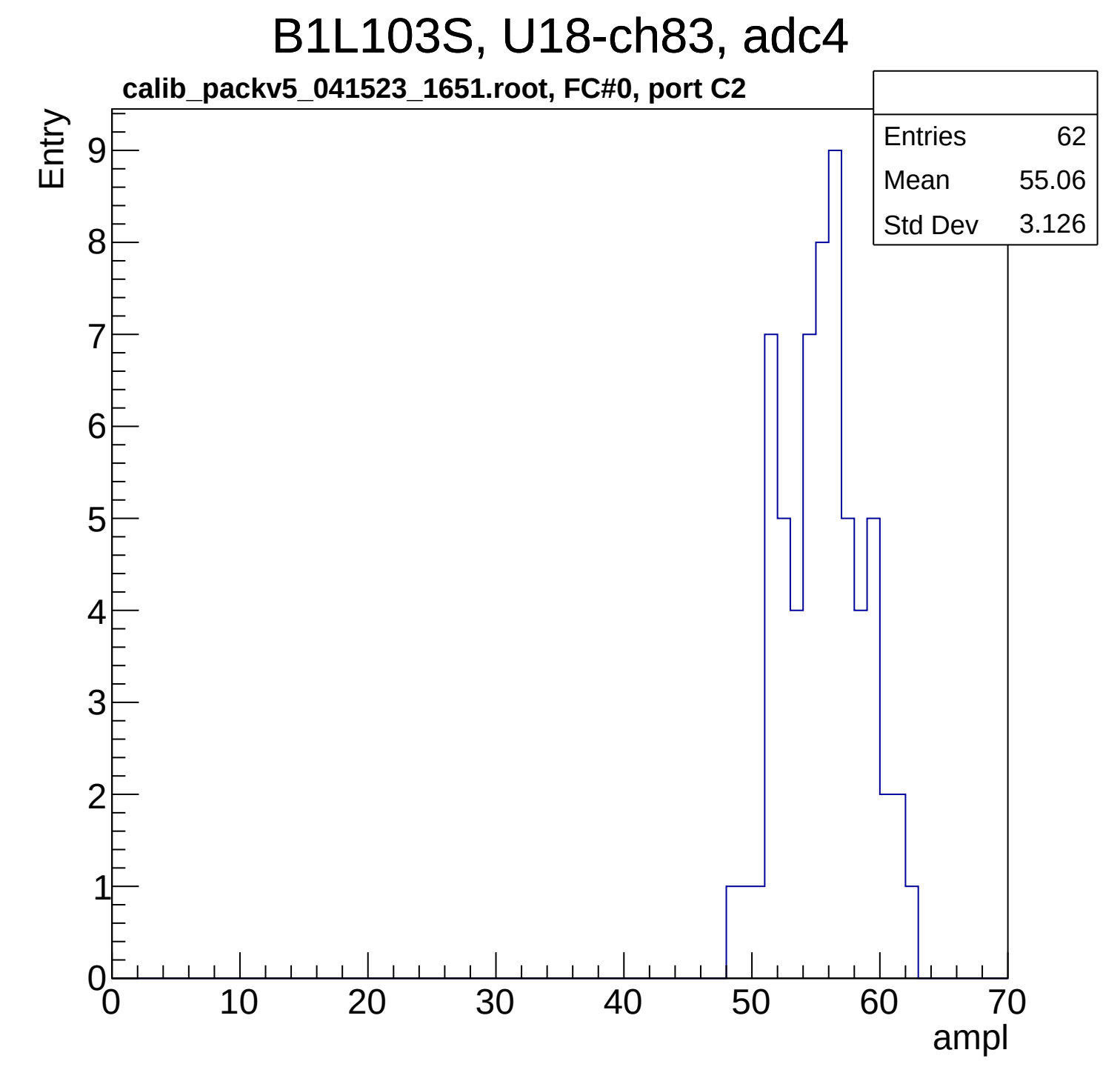
B1L103S, U18-ch83, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 55.06
Std Dev 3.126
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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40
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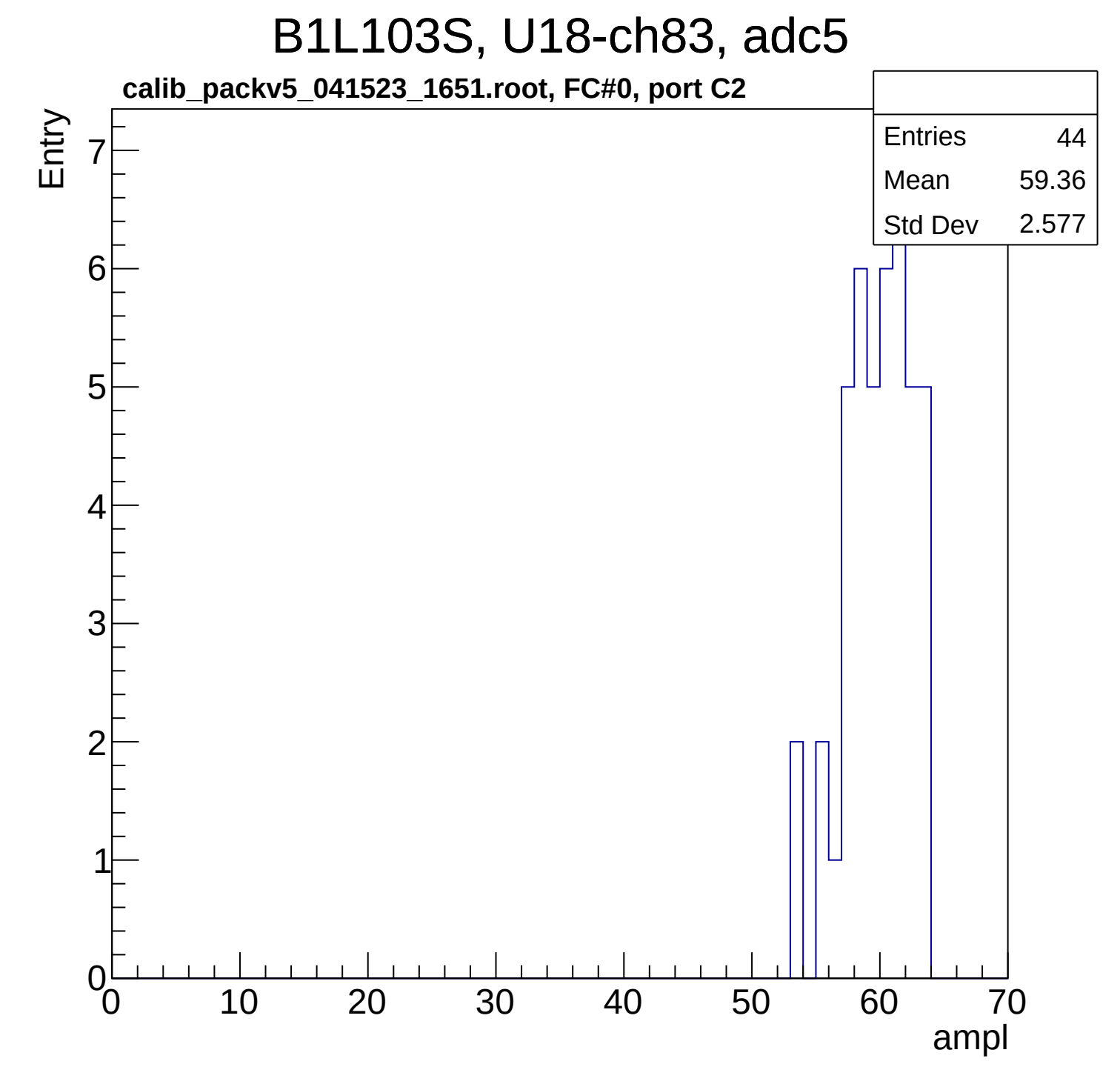
B1L103S, U18-ch83, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 59.36
Std Dev 2.577
Entry
ampl
0
1
2
3
4
5
6
7
0
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20
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40
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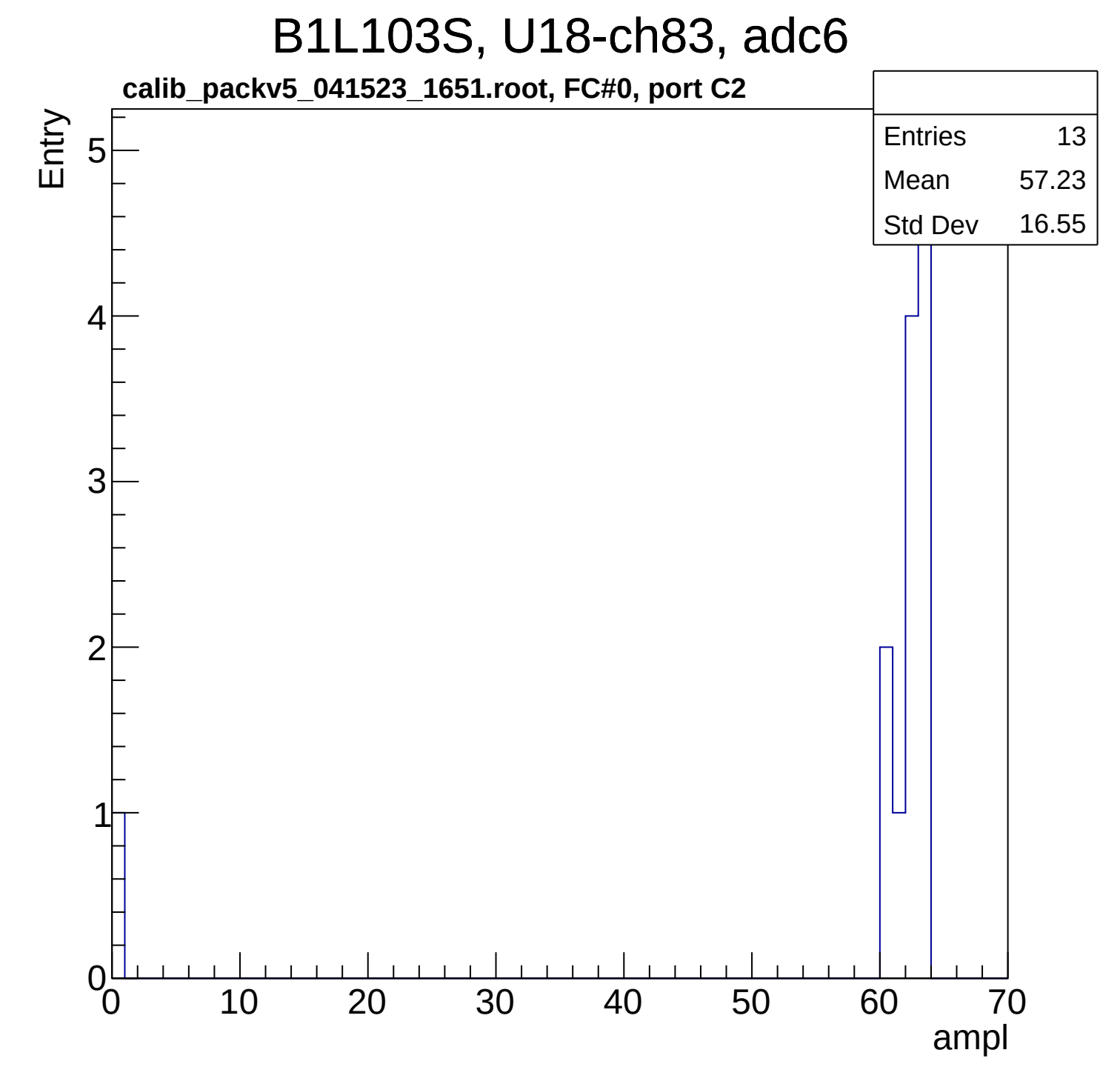
60
70


B1L103S, U18-ch83, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 13
Mean 57.23
Std Dev 16.55
Entry
ampl
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1
2
3
4
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60
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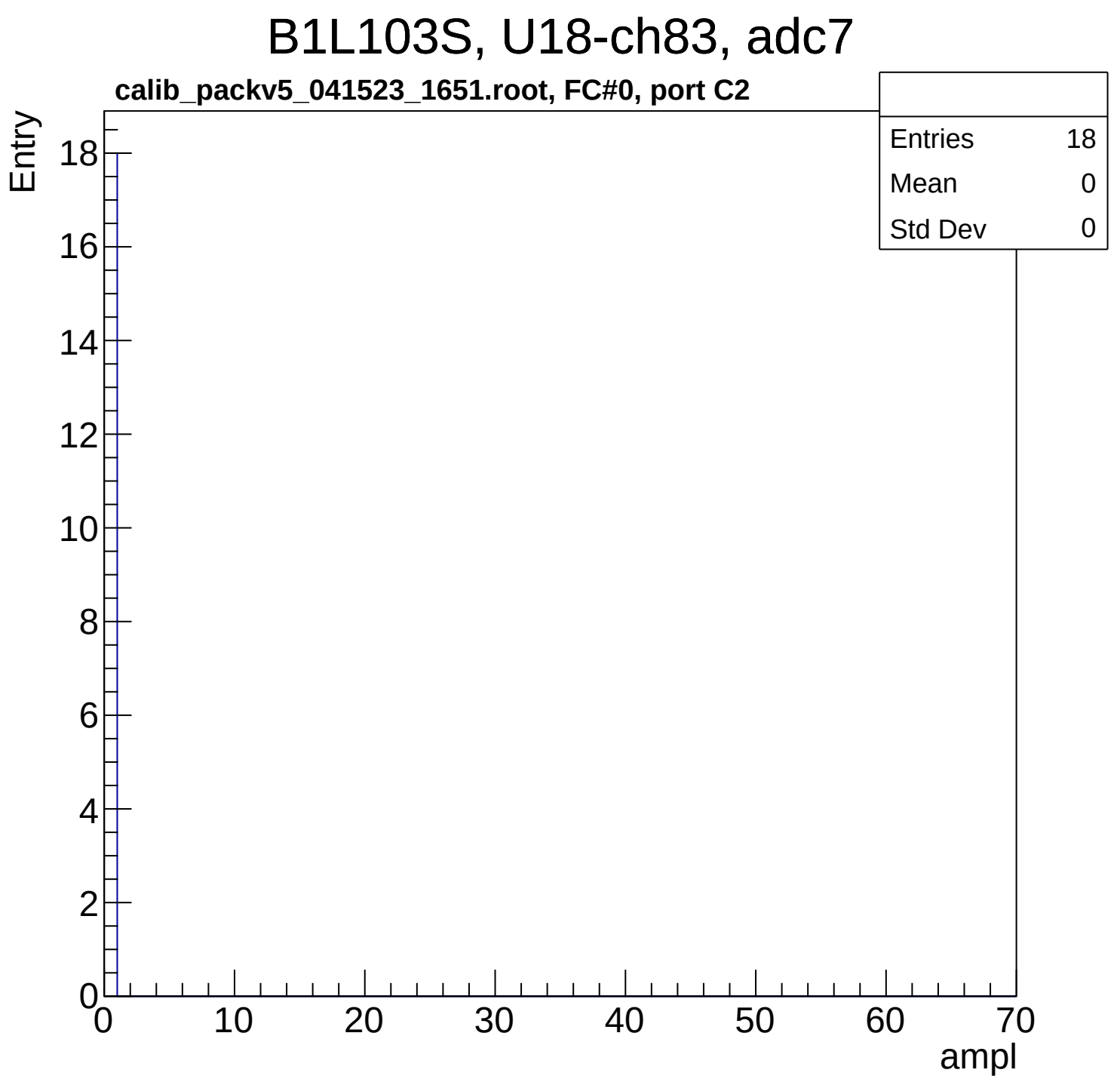
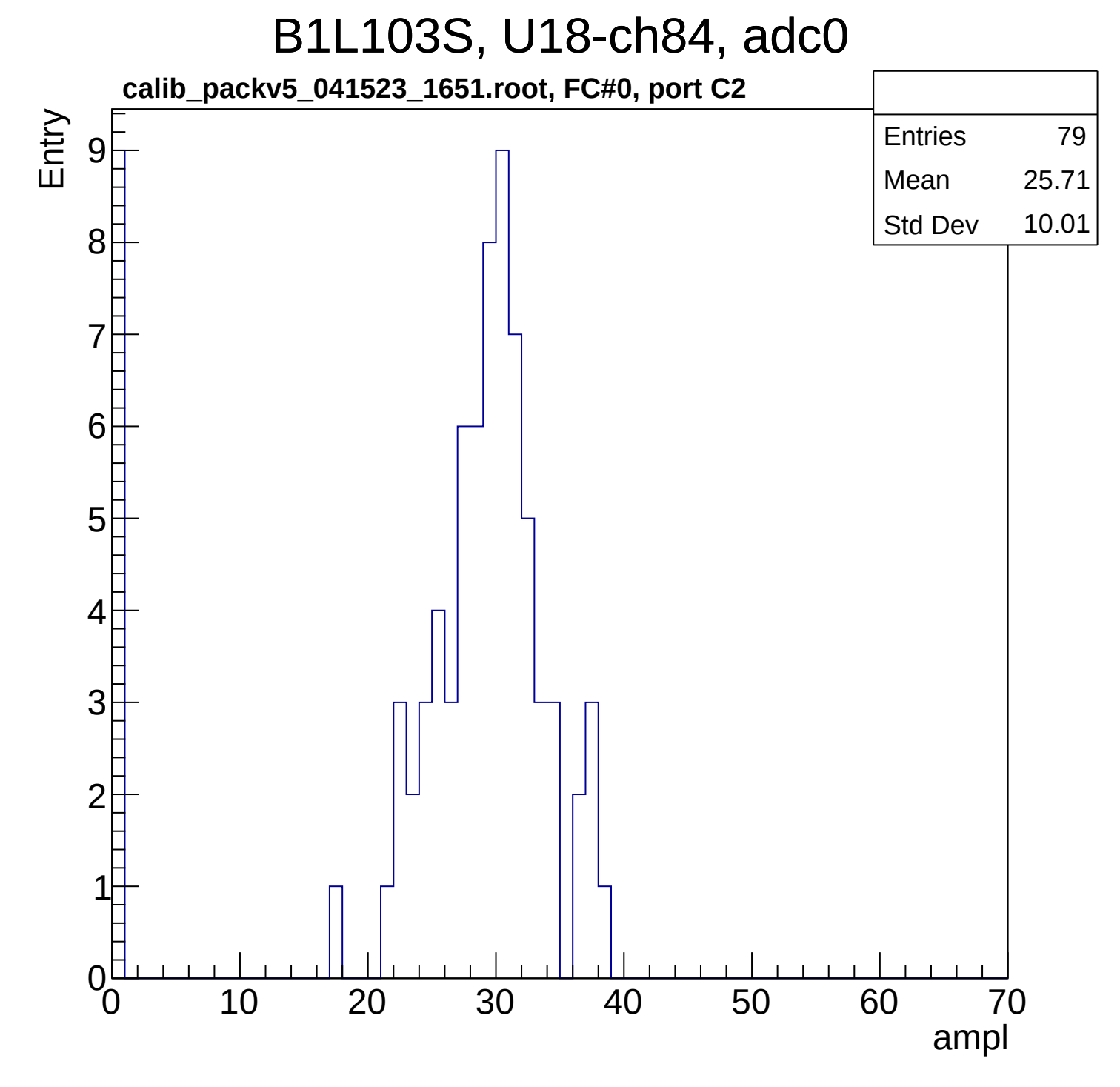

B1L103S, U18-ch83, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch84, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 25.71
Std Dev 10.01
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
50
60
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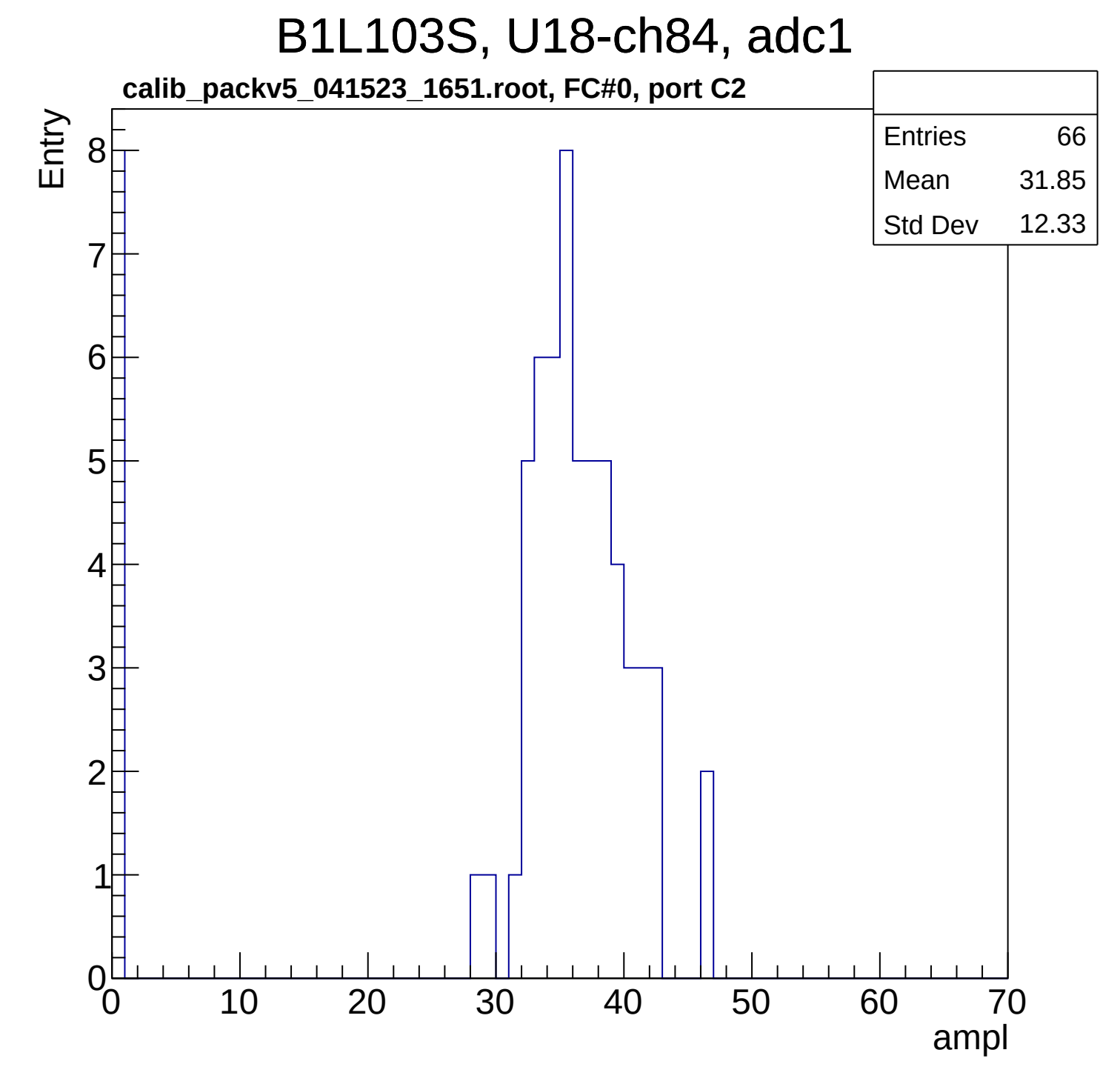
B1L103S, U18-ch84, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 31.85
Std Dev 12.33
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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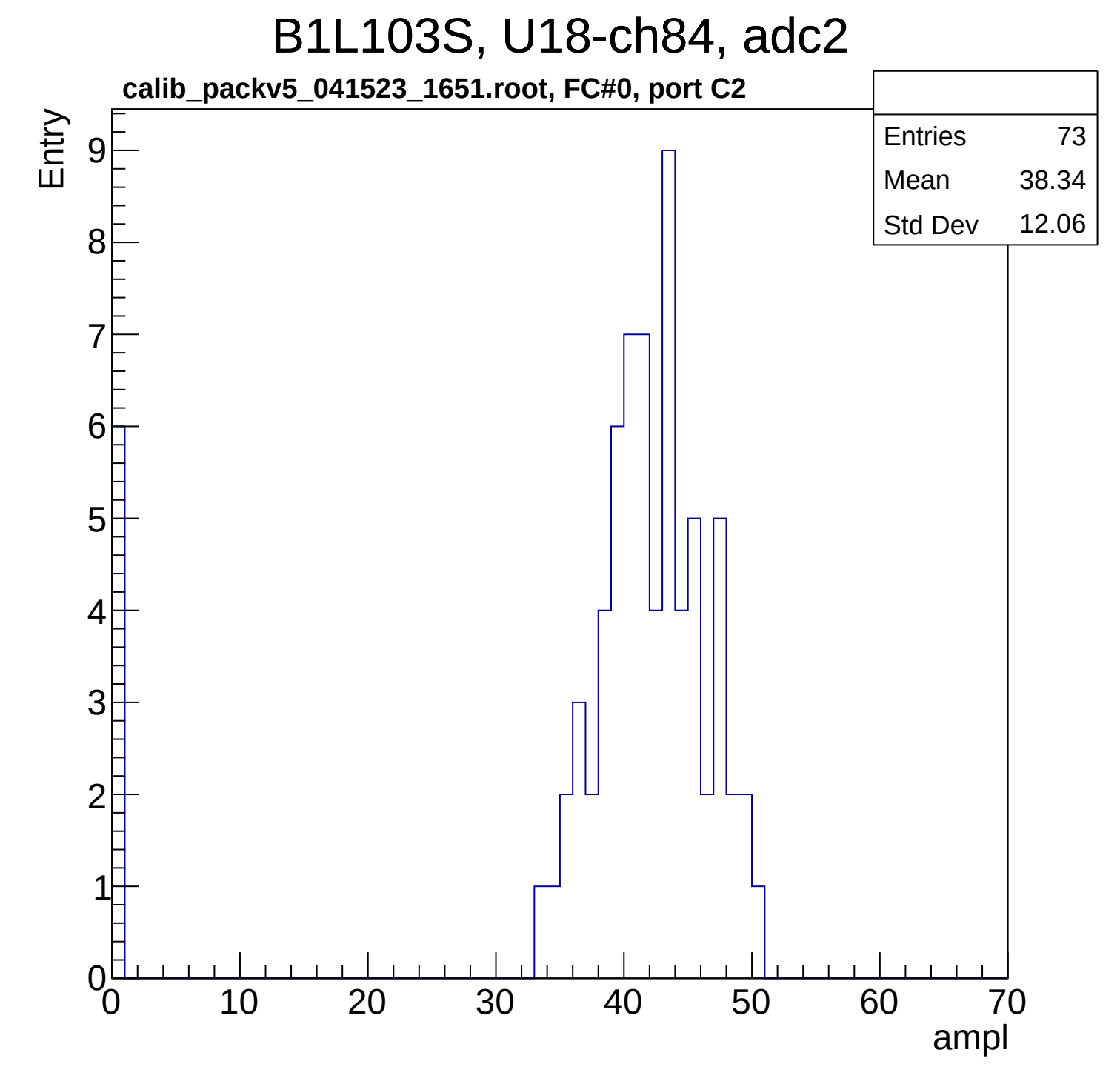
B1L103S, U18-ch84, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 38.34
Std Dev 12.06
Entry
ampl
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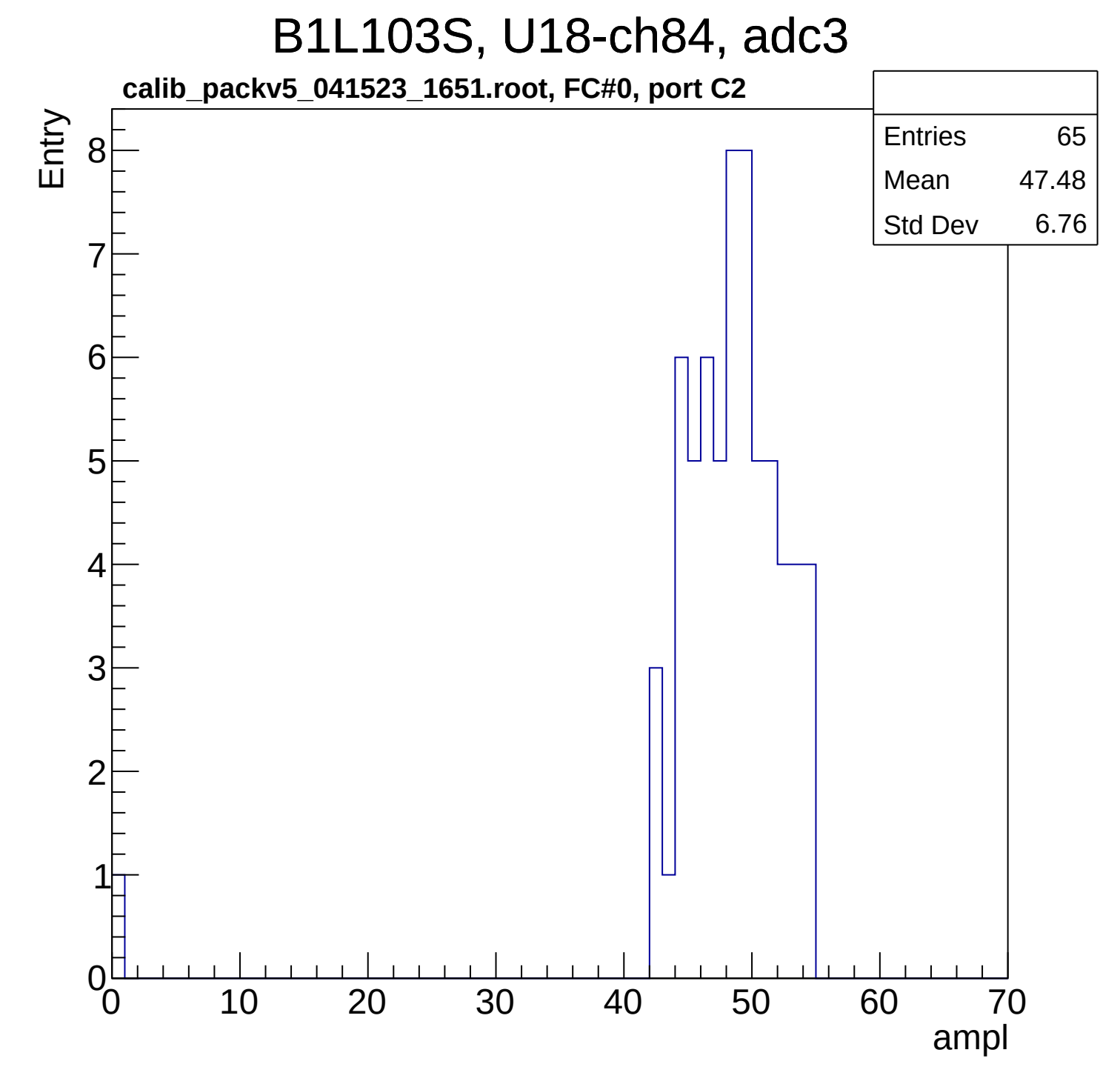
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U18-ch84, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 47.48
Std Dev 6.76
Entry
ampl
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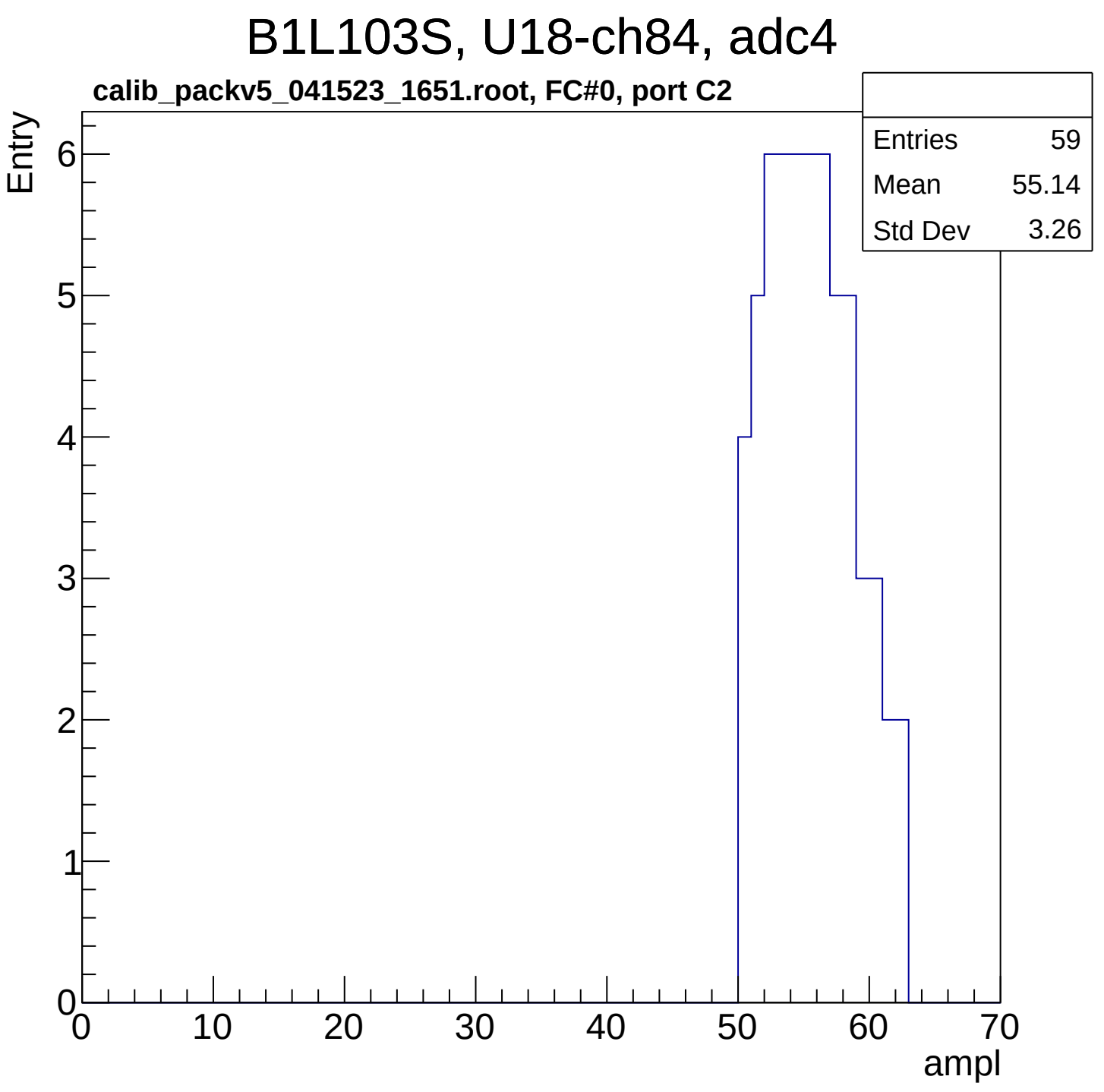
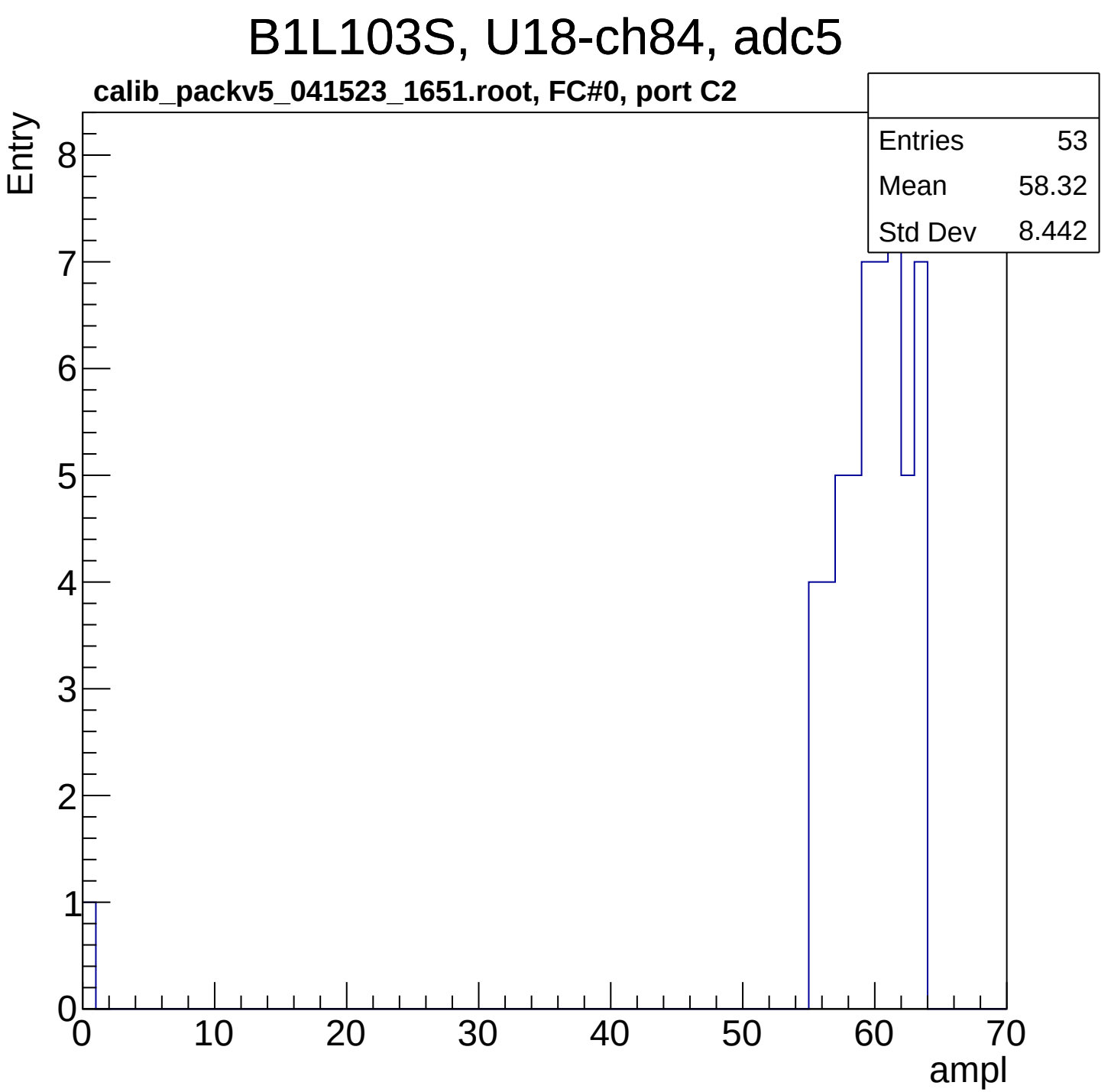
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch84, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 55.14
Std Dev 3.26
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch84, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 58.32
Std Dev 8.442
Entry
ampl
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2
3
4
5
6
7
8
0
10
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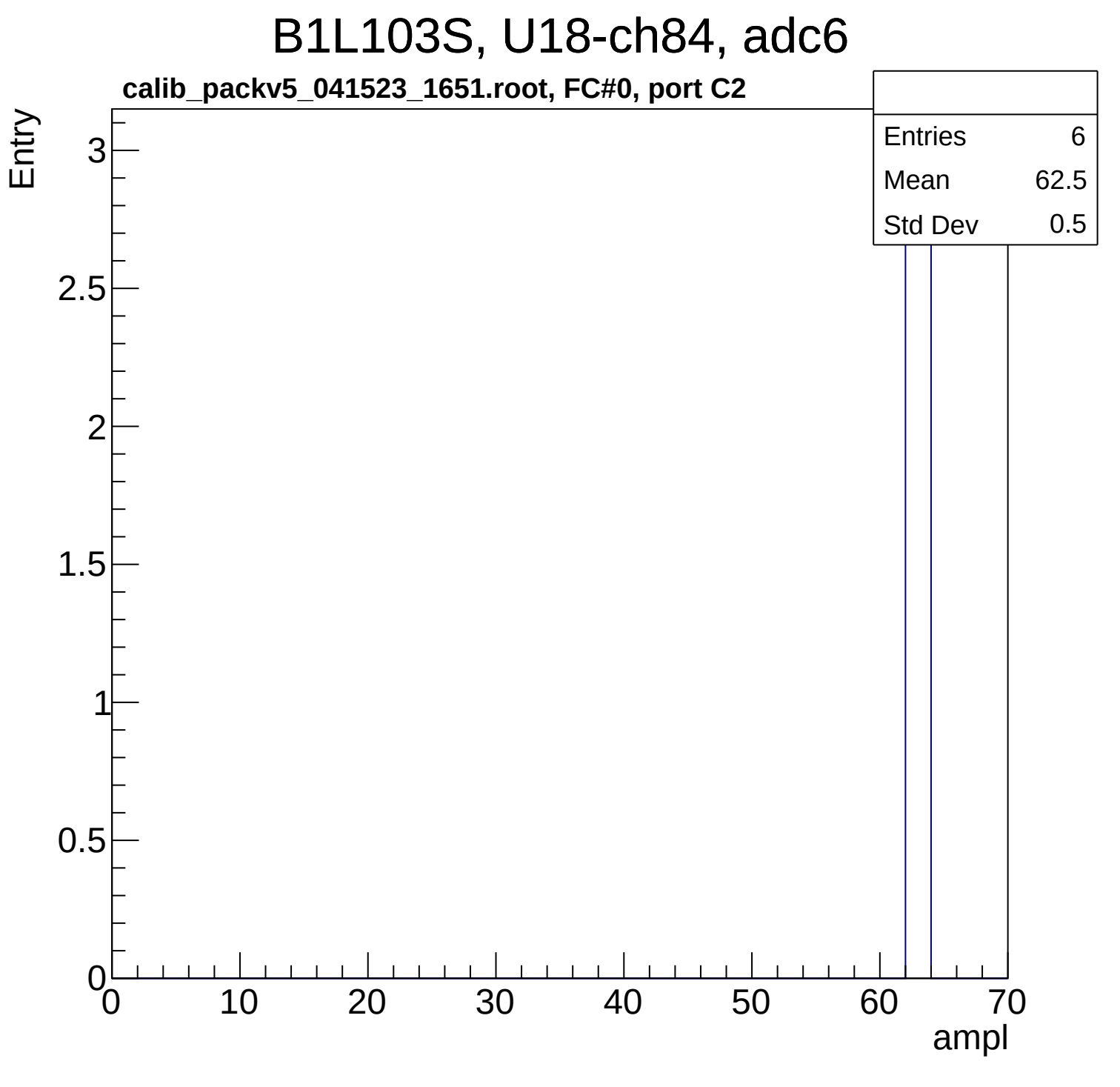
40
50
60
70


B1L103S, U18-ch84, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 62.5
Std Dev 0.5
Entry
ampl
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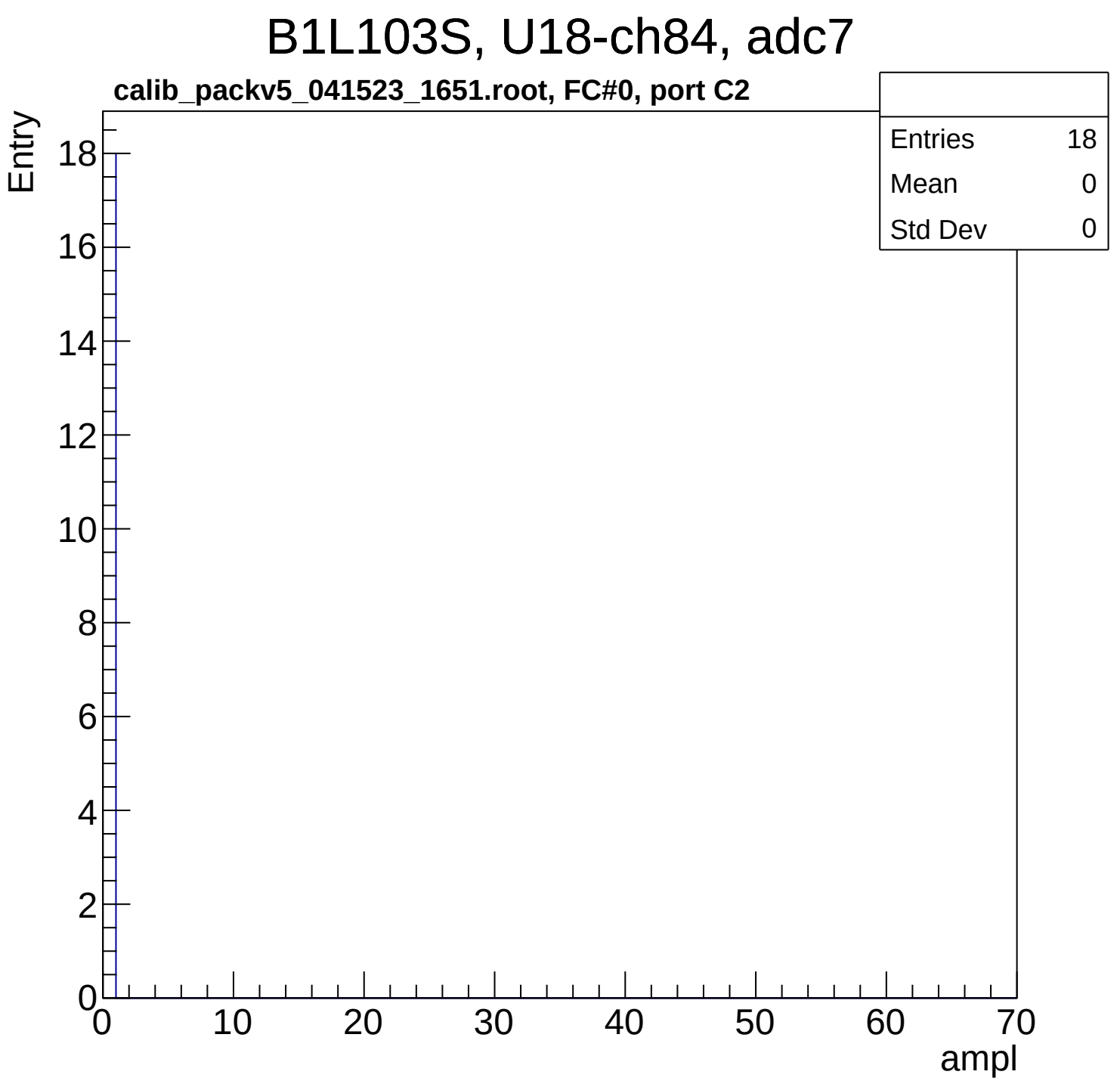
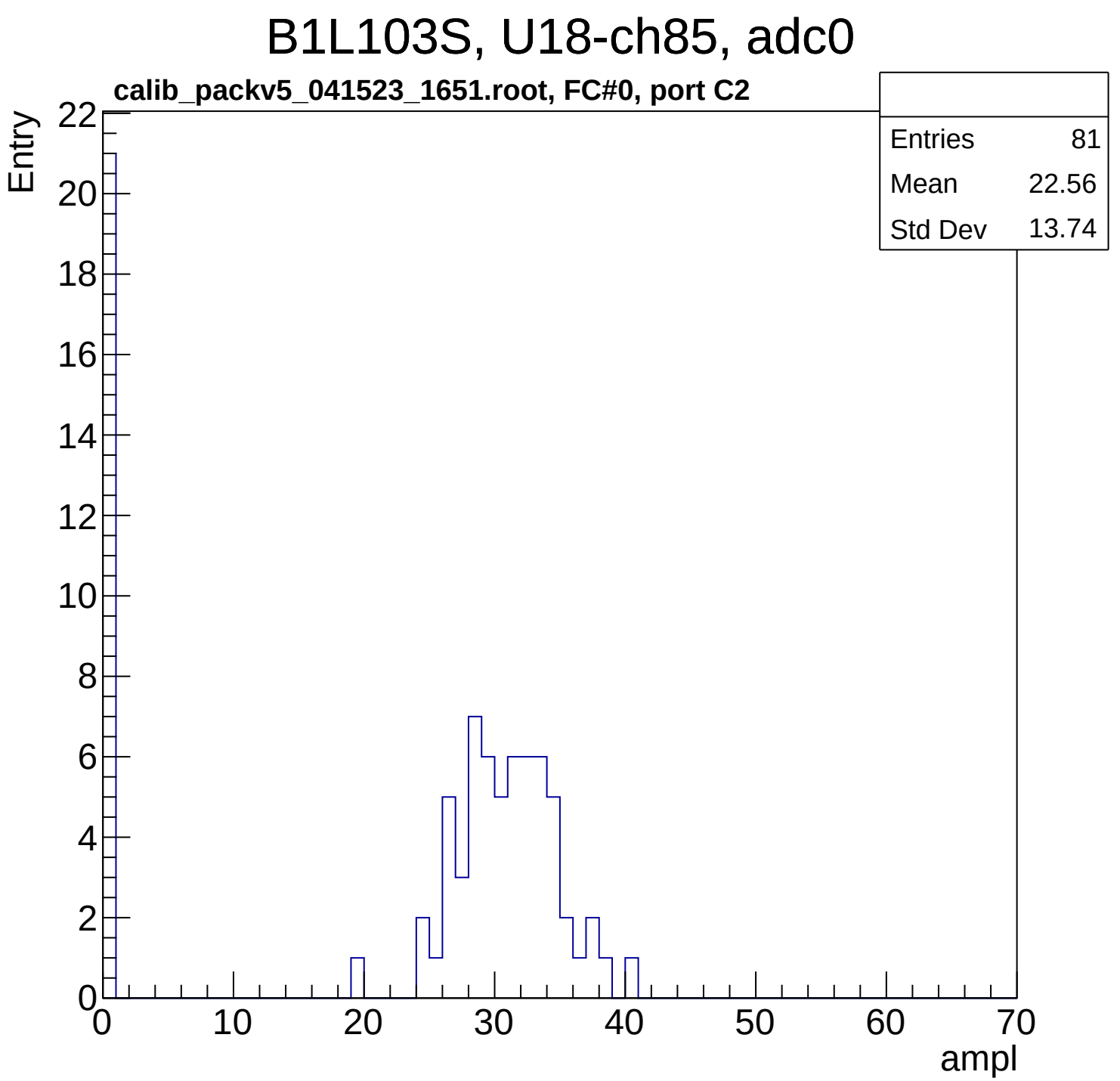
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U18-ch84, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch85, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 22.56
Std Dev 13.74
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
22
0
10
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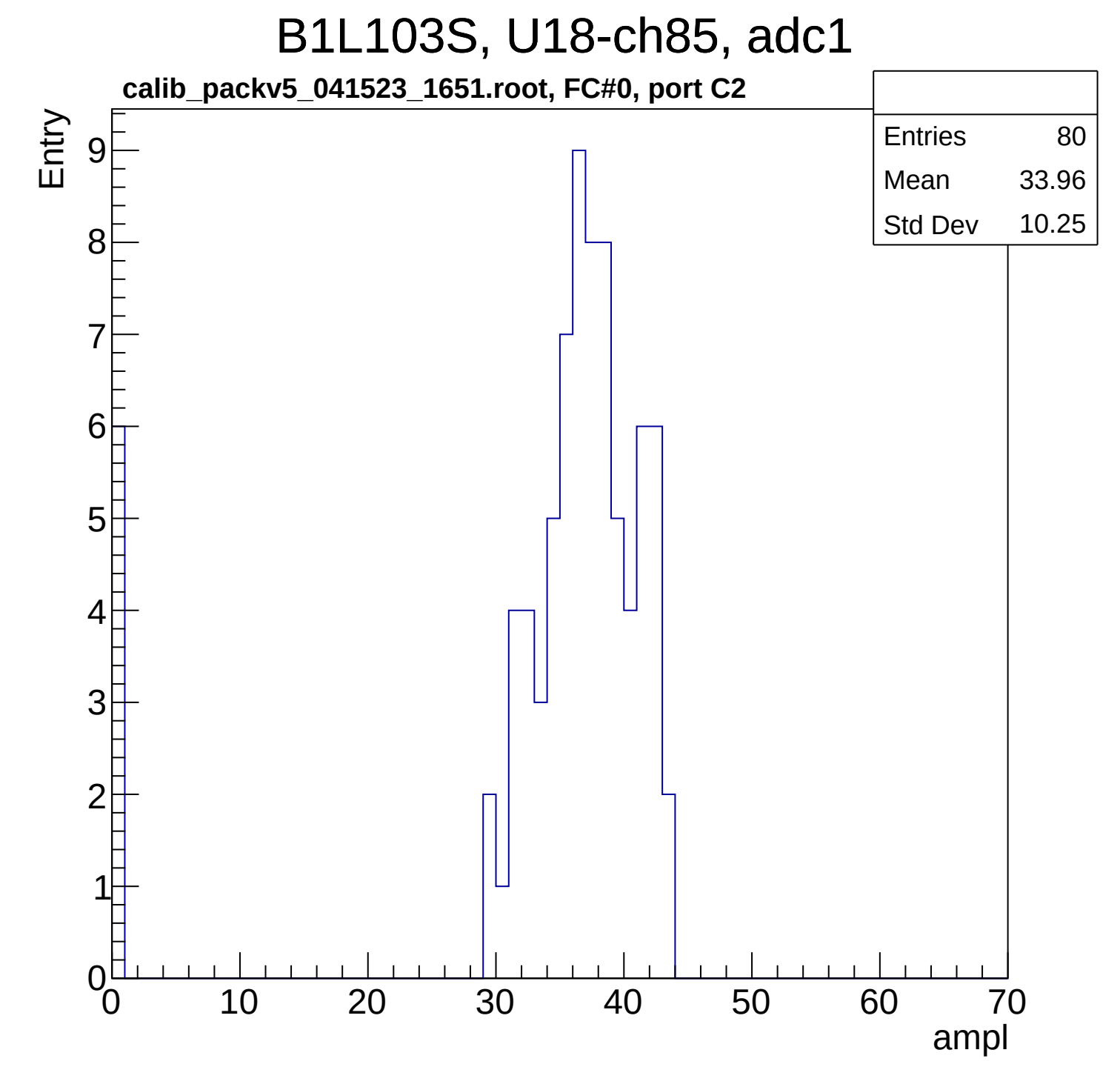
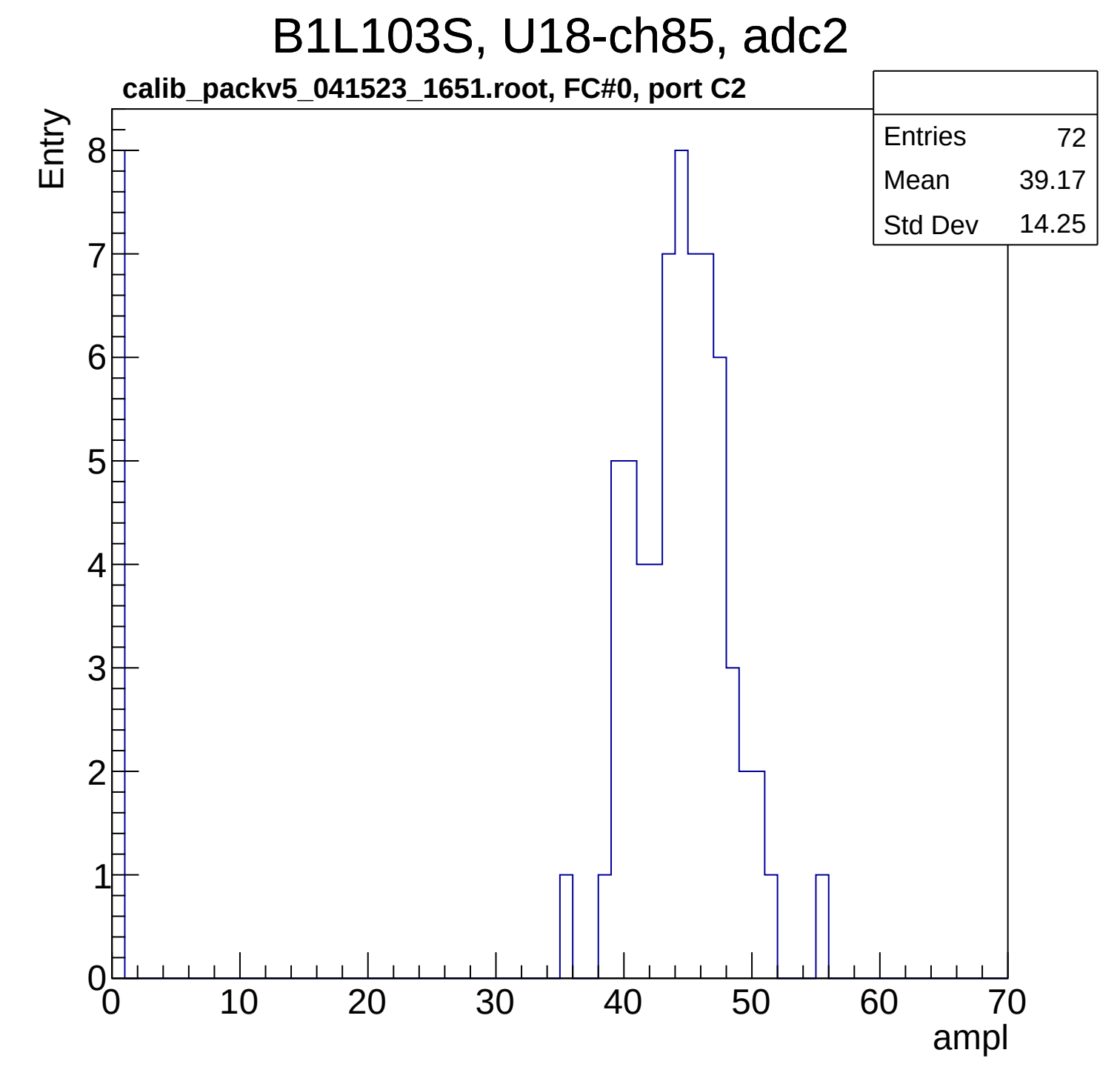
30
40
50
60
70


B1L103S, U18-ch85, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 33.96
Std Dev 10.25
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U18-ch85, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 39.17
Std Dev 14.25
Entry
ampl
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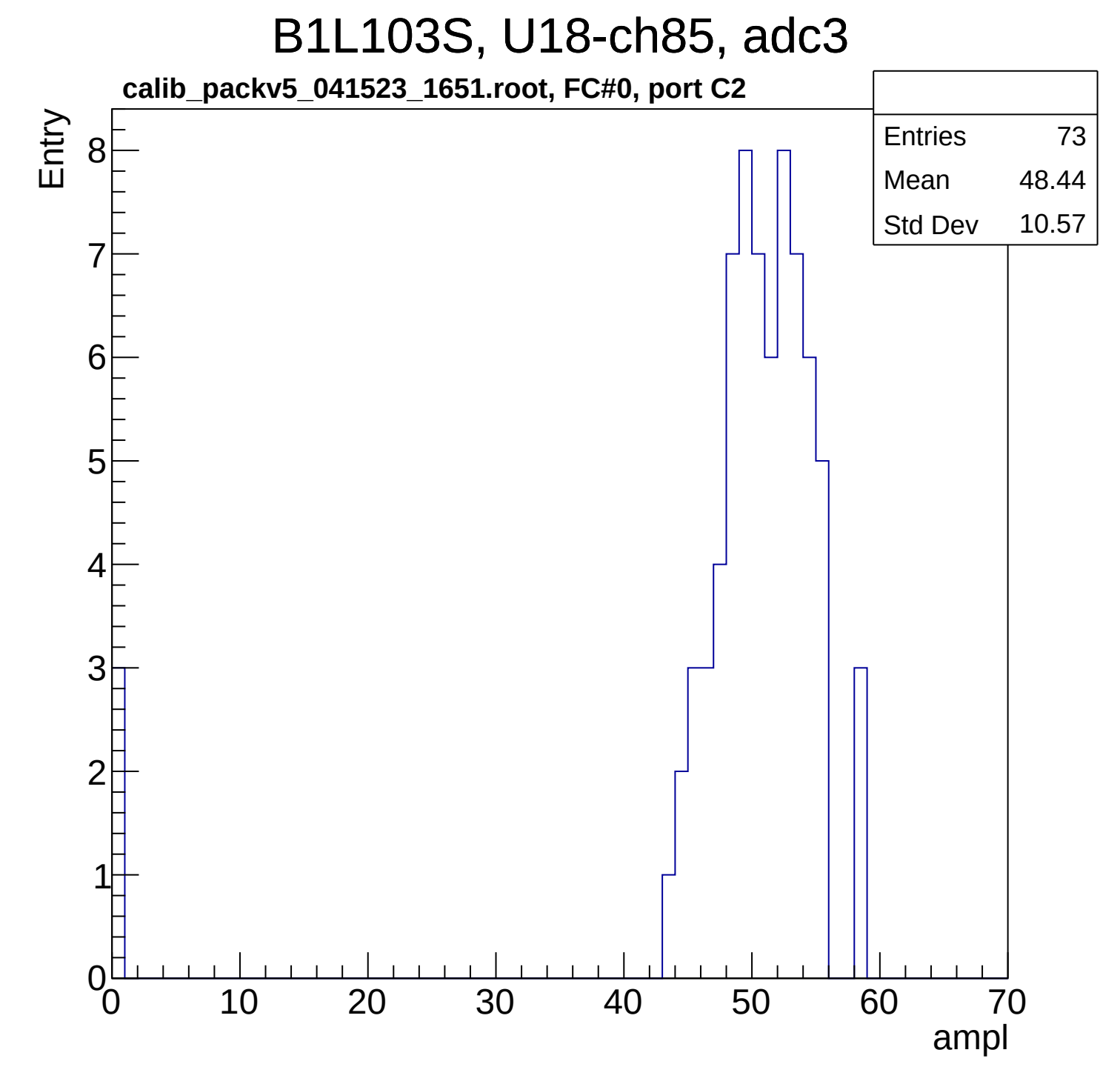
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch85, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 48.44
Std Dev 10.57
Entry
ampl
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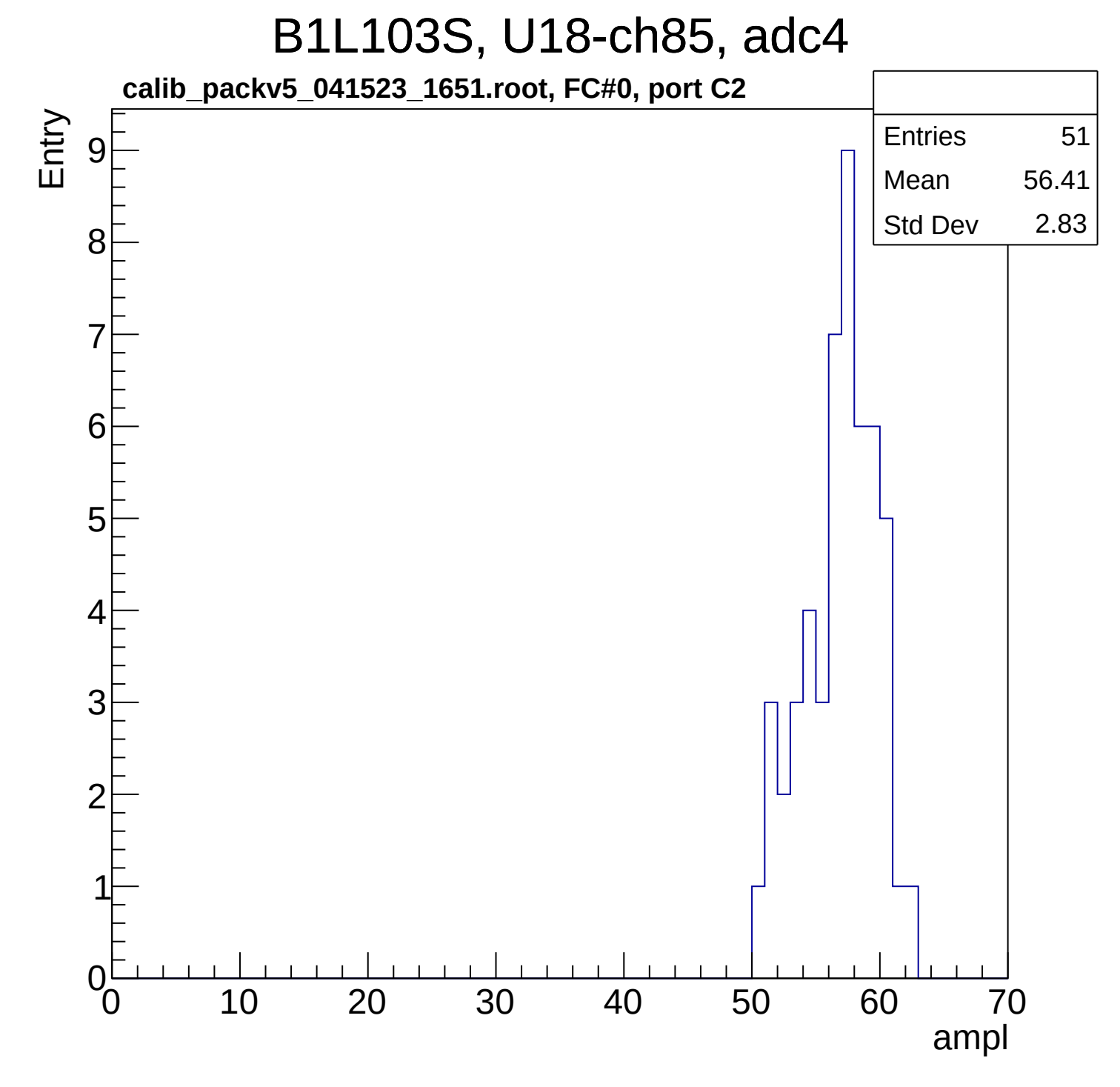
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch85, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 56.41
Std Dev 2.83
Entry
ampl
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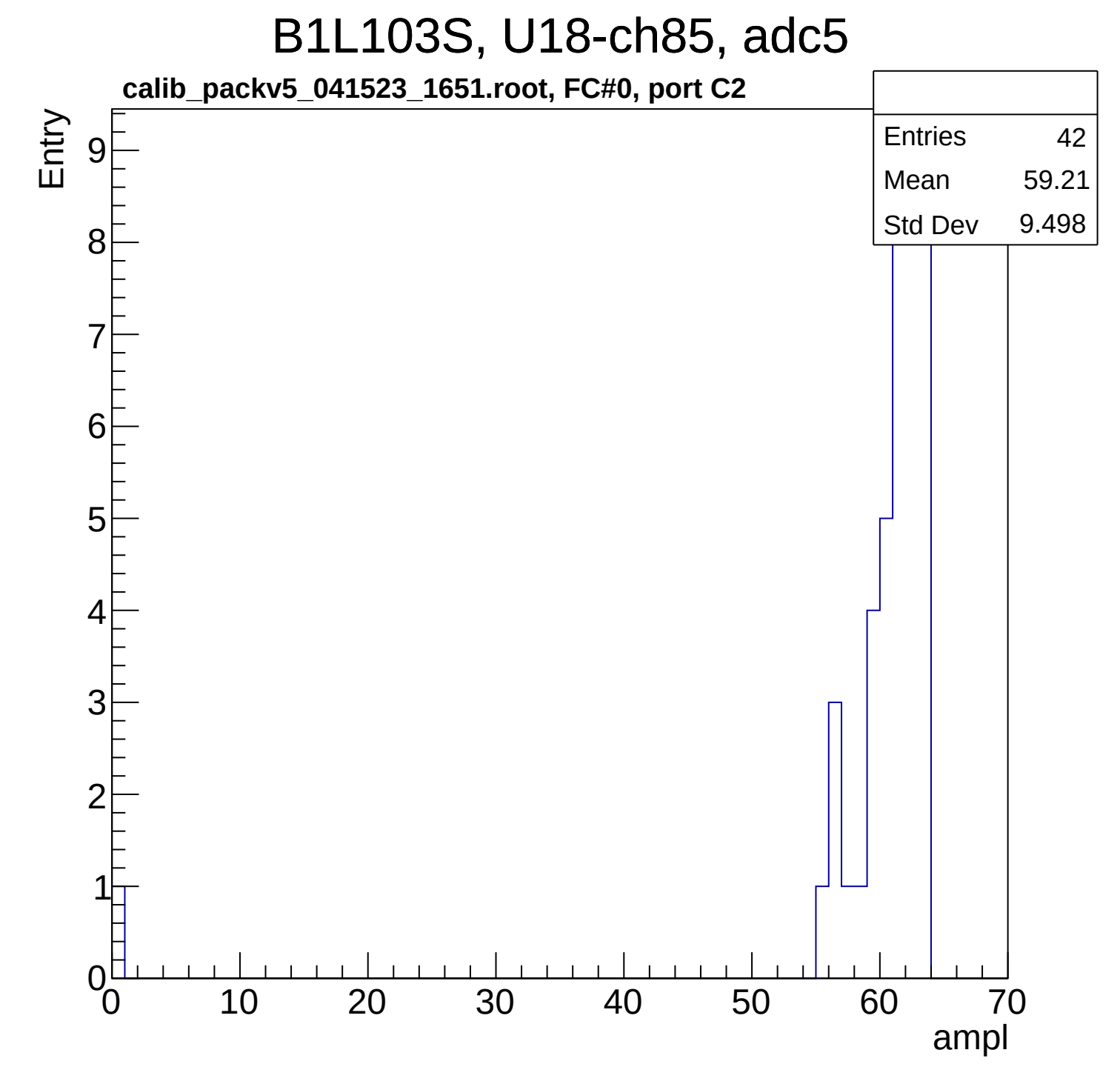
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U18-ch85, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 42
Mean 59.21
Std Dev 9.498
Entry
ampl
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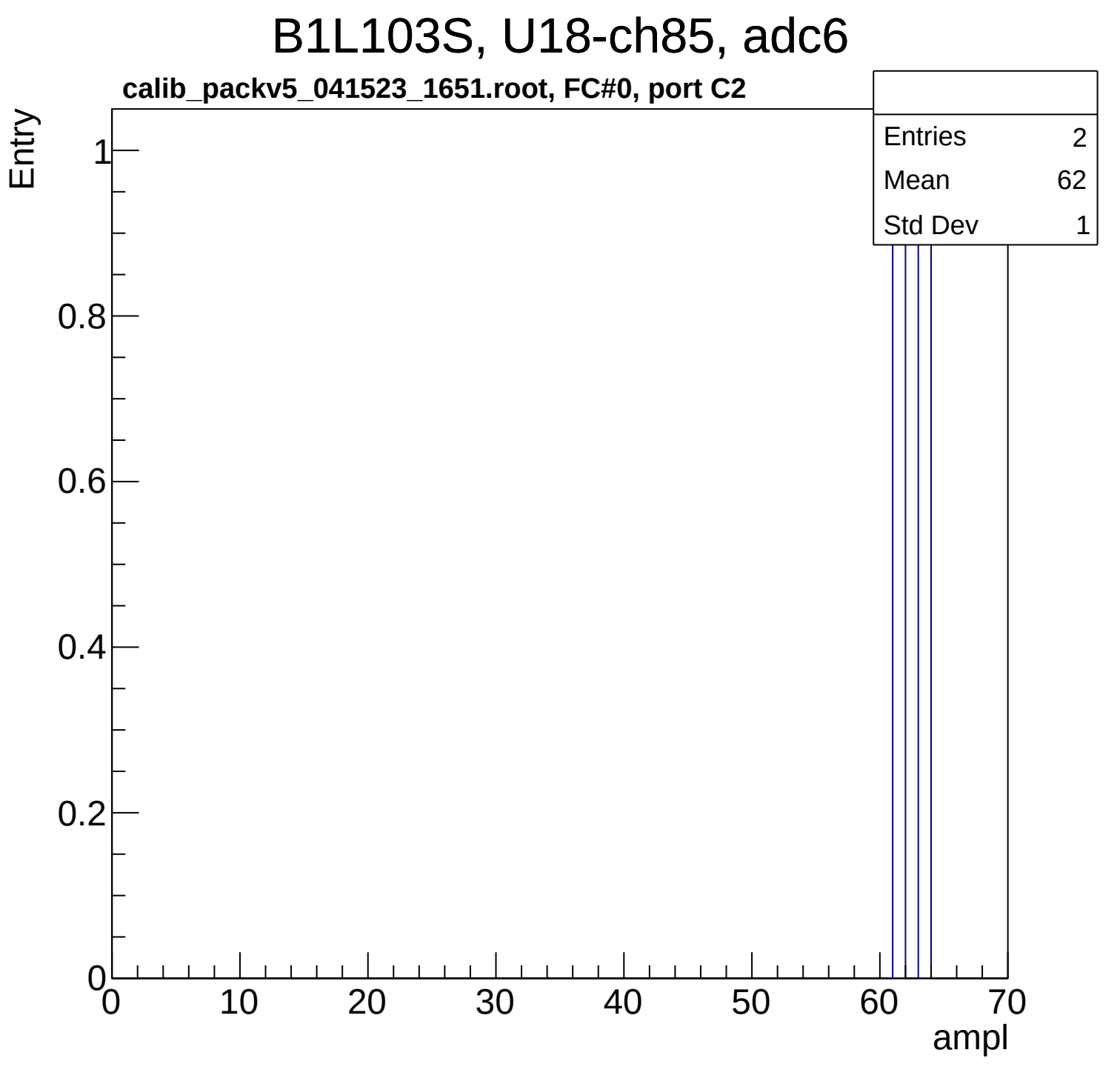
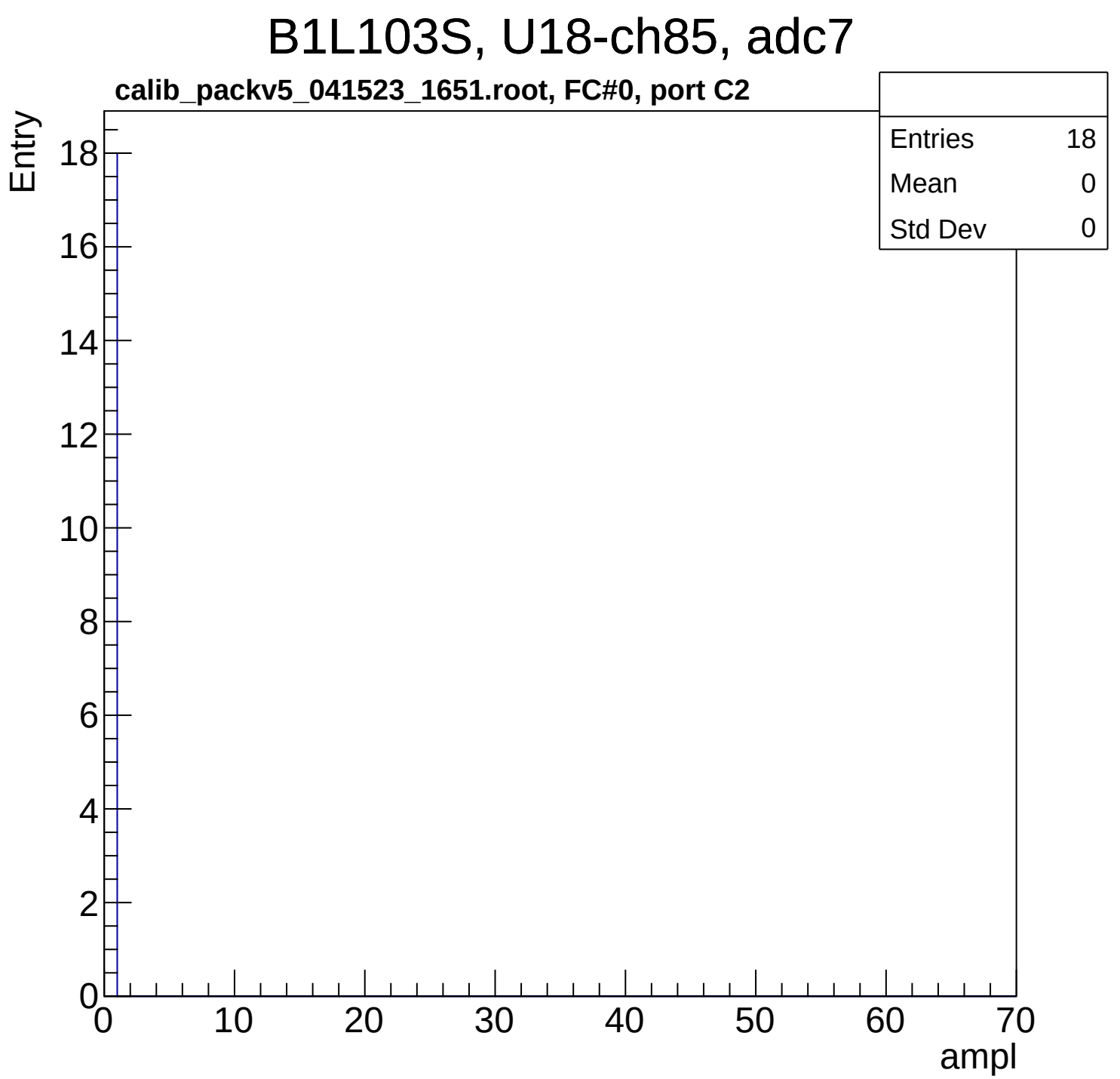
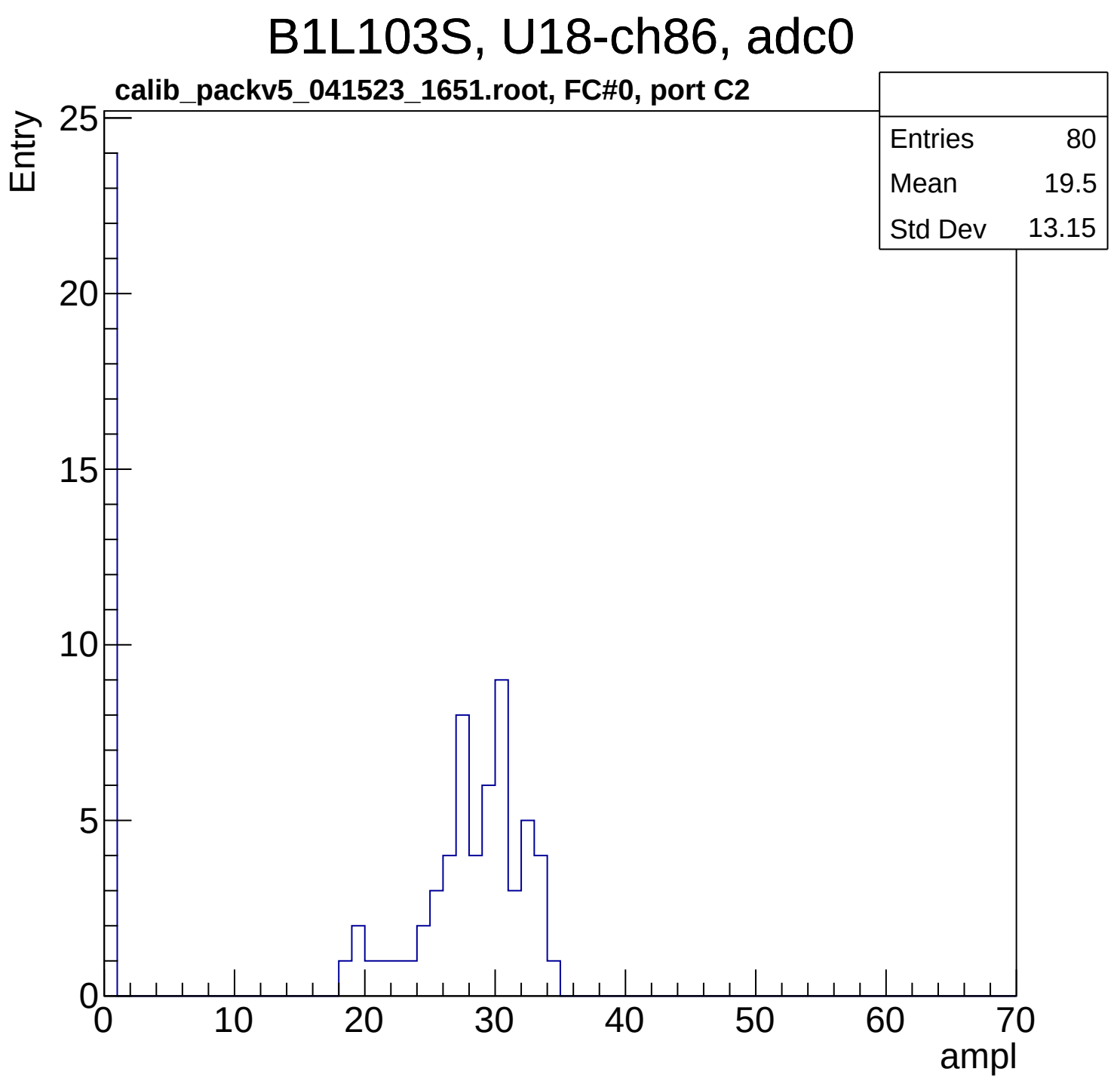
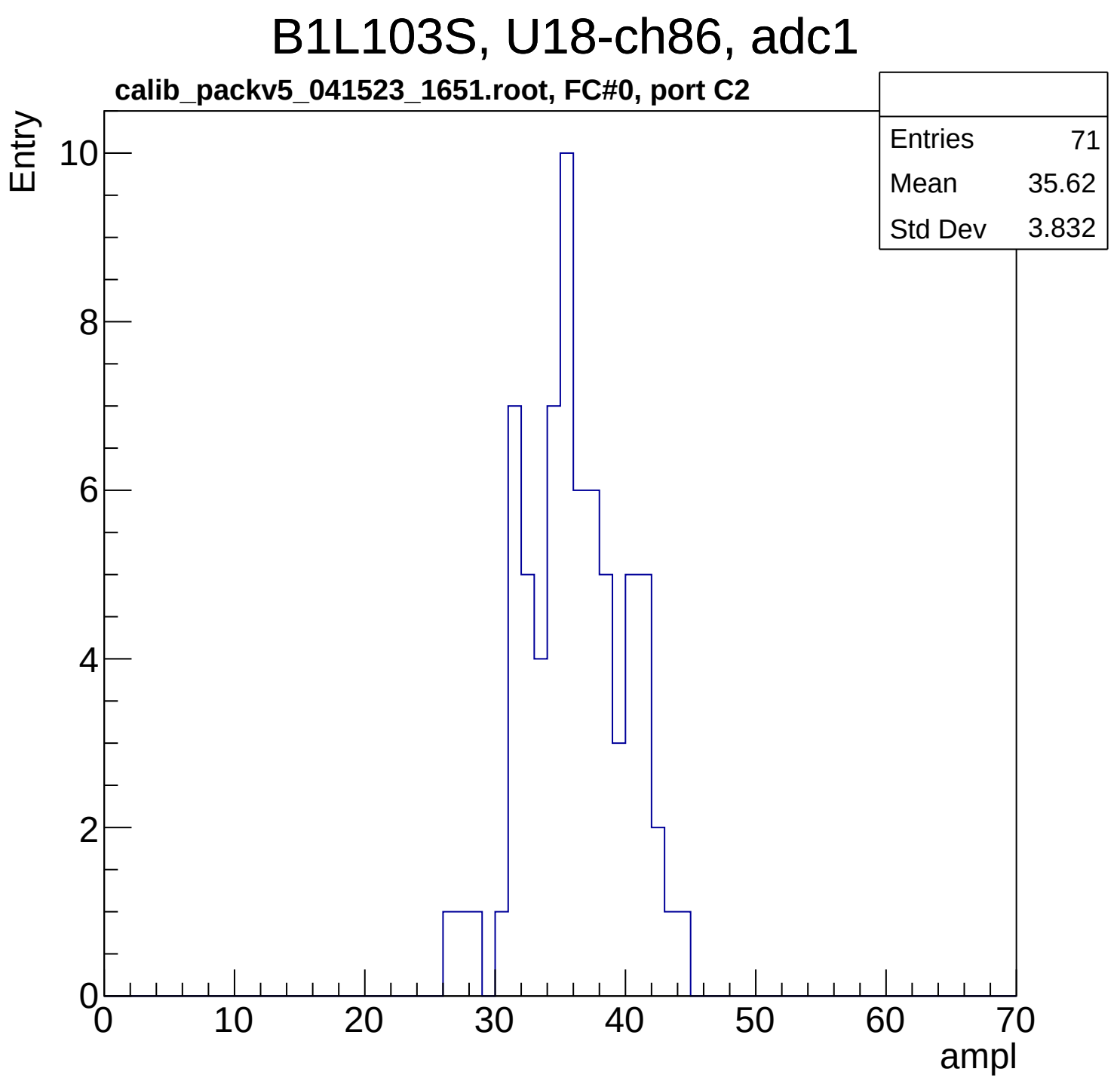
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U18-ch85, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 2
Mean 62
Std Dev 1
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch85, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch86, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 19.5
Std Dev 13.15
Entry
ampl
0
5
10
15
20
25
0
10
20
30
40
50
60
70


B1L103S, U18-ch86, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 35.62
Std Dev 3.832
Entry
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2
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6
8
10
0
10
20
30
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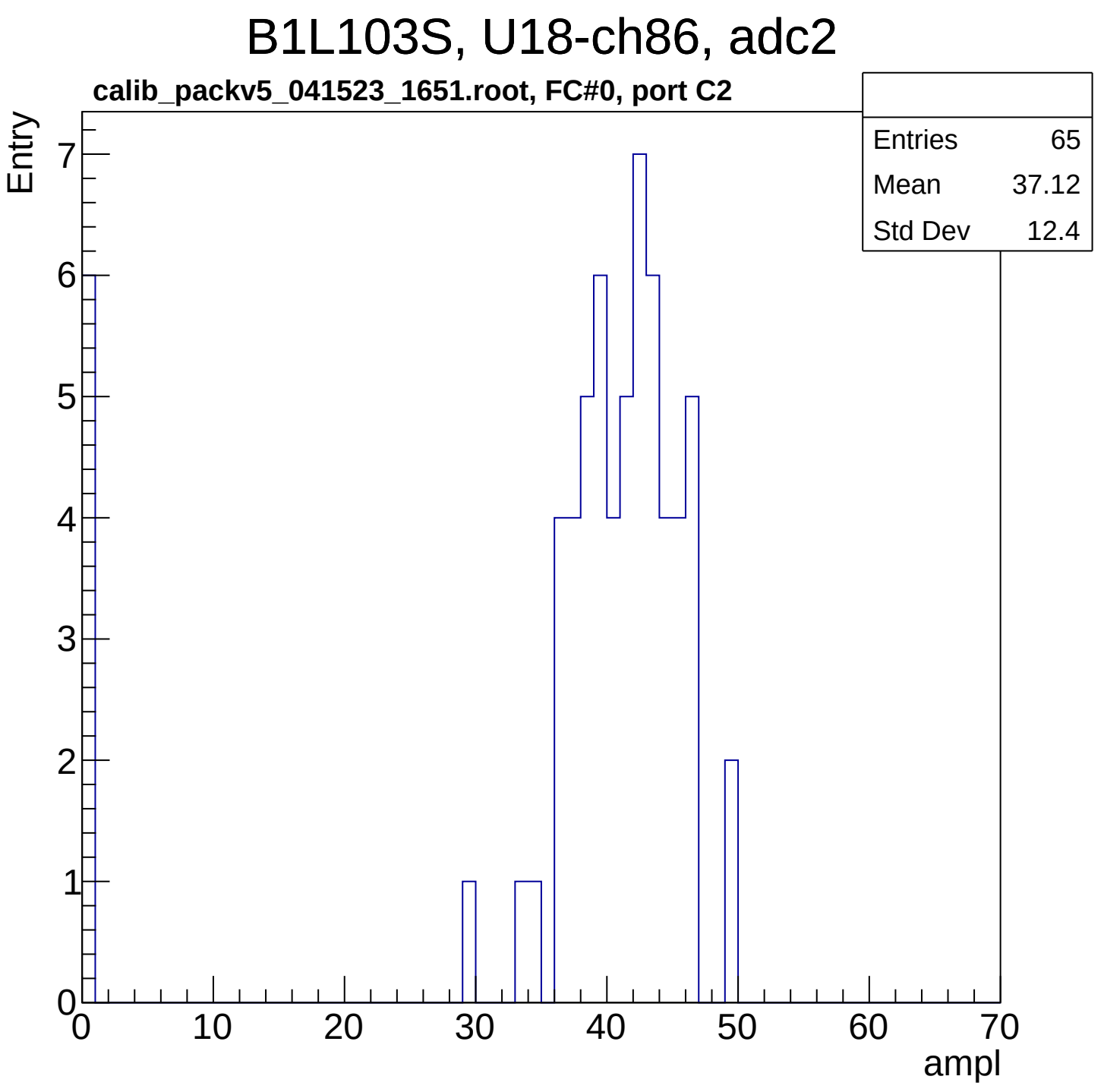
50
60
70
ampl


B1L103S, U18-ch86, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 37.12
Std Dev 12.4
Entry
ampl
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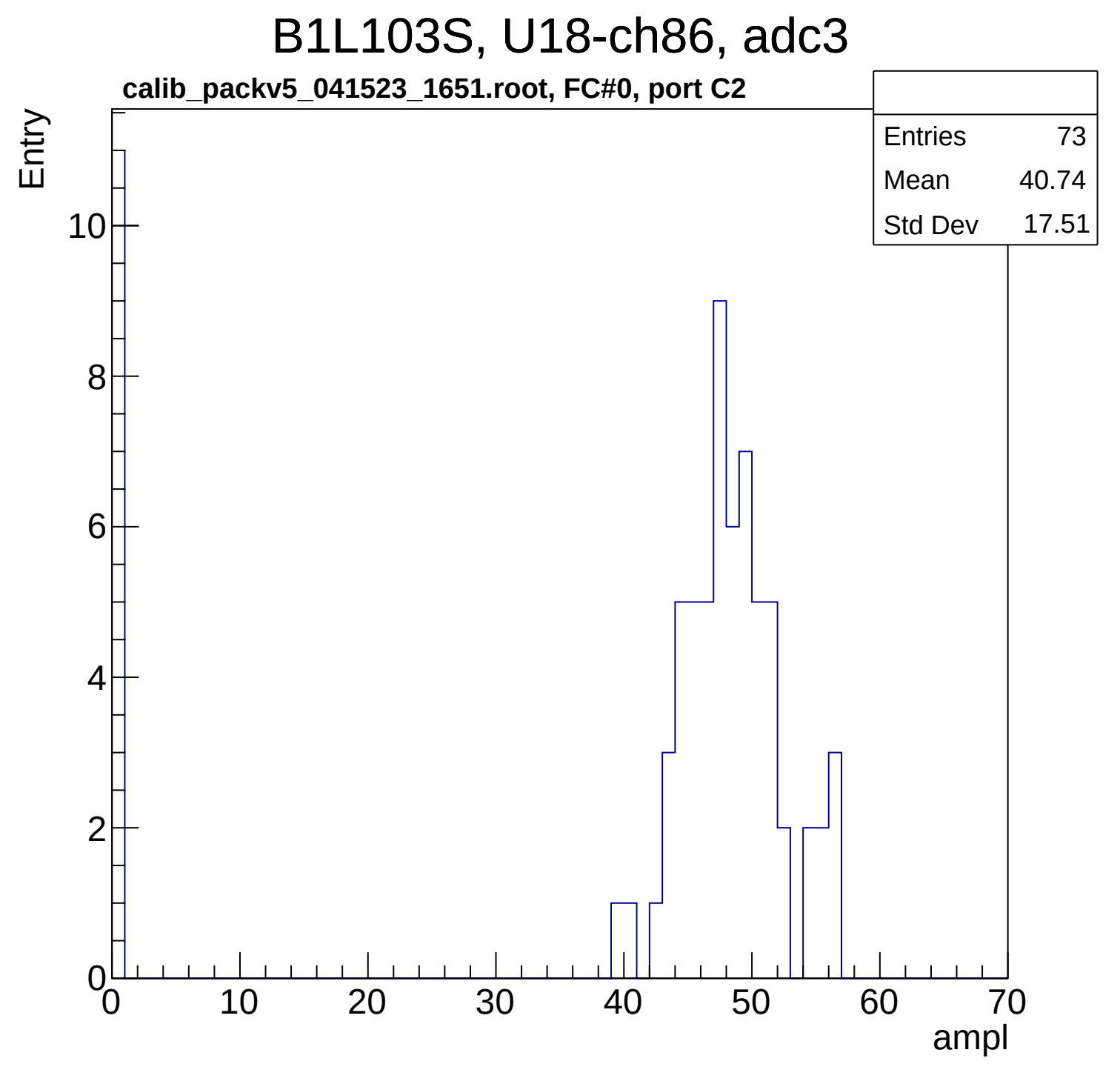
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U18-ch86, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 40.74
Std Dev 17.51
Entry
0
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6
8
10
0
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30
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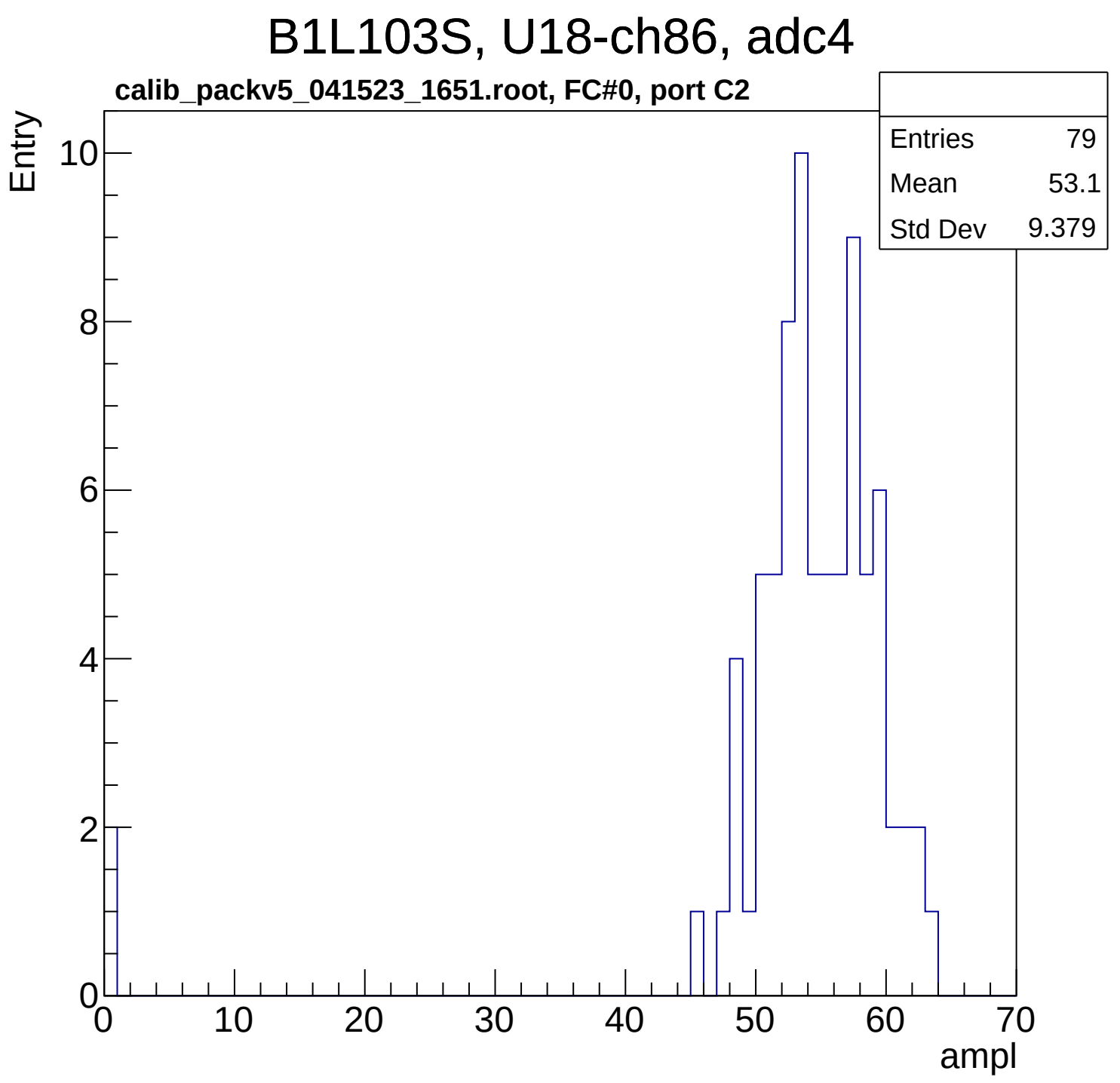
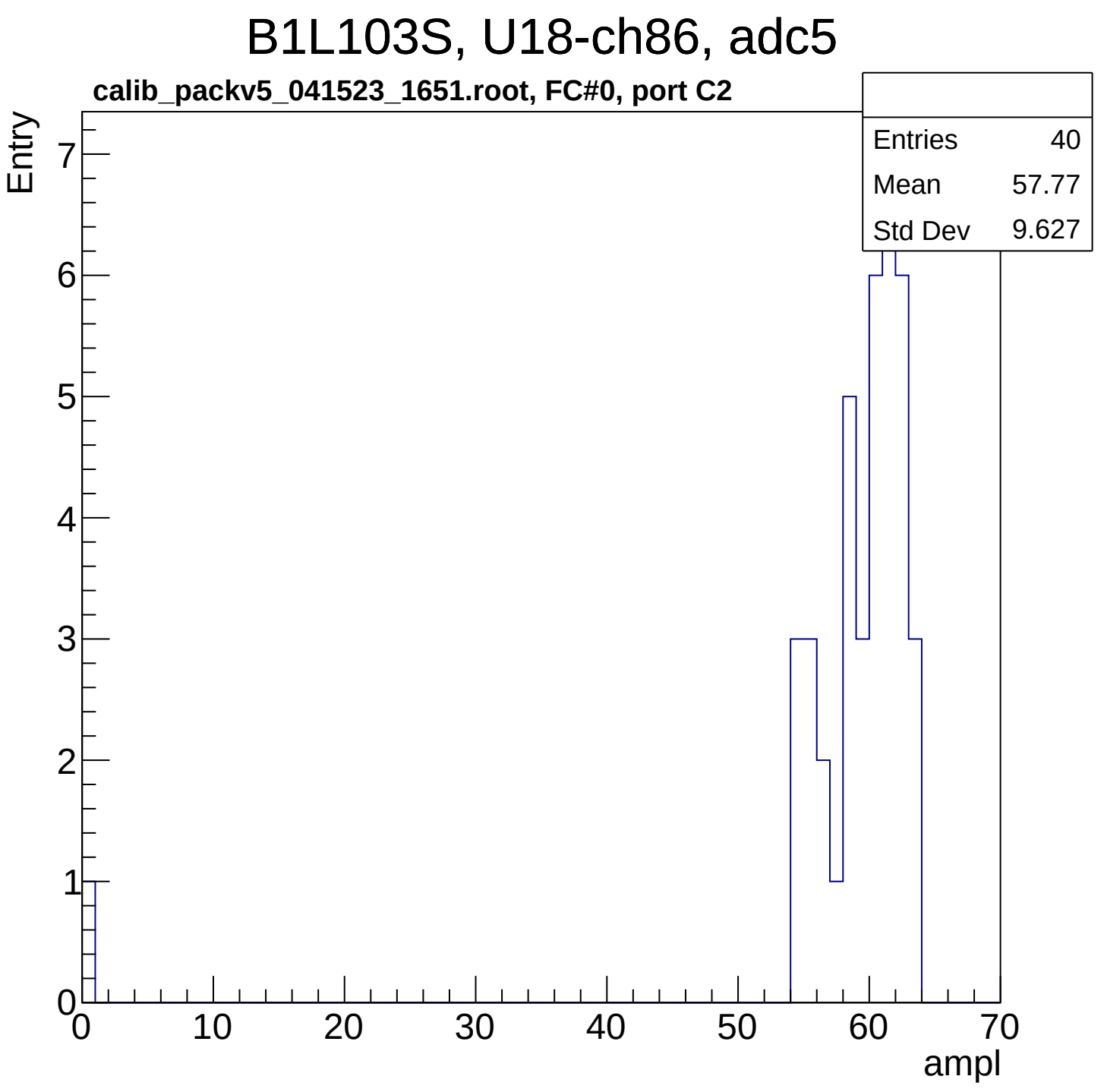
50
60
70
ampl


B1L103S, U18-ch86, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 53.1
Std Dev 9.379
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch86, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 40
Mean 57.77
Std Dev 9.627
Entry
ampl
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1
2
3
4
5
6
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0
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20
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40
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60
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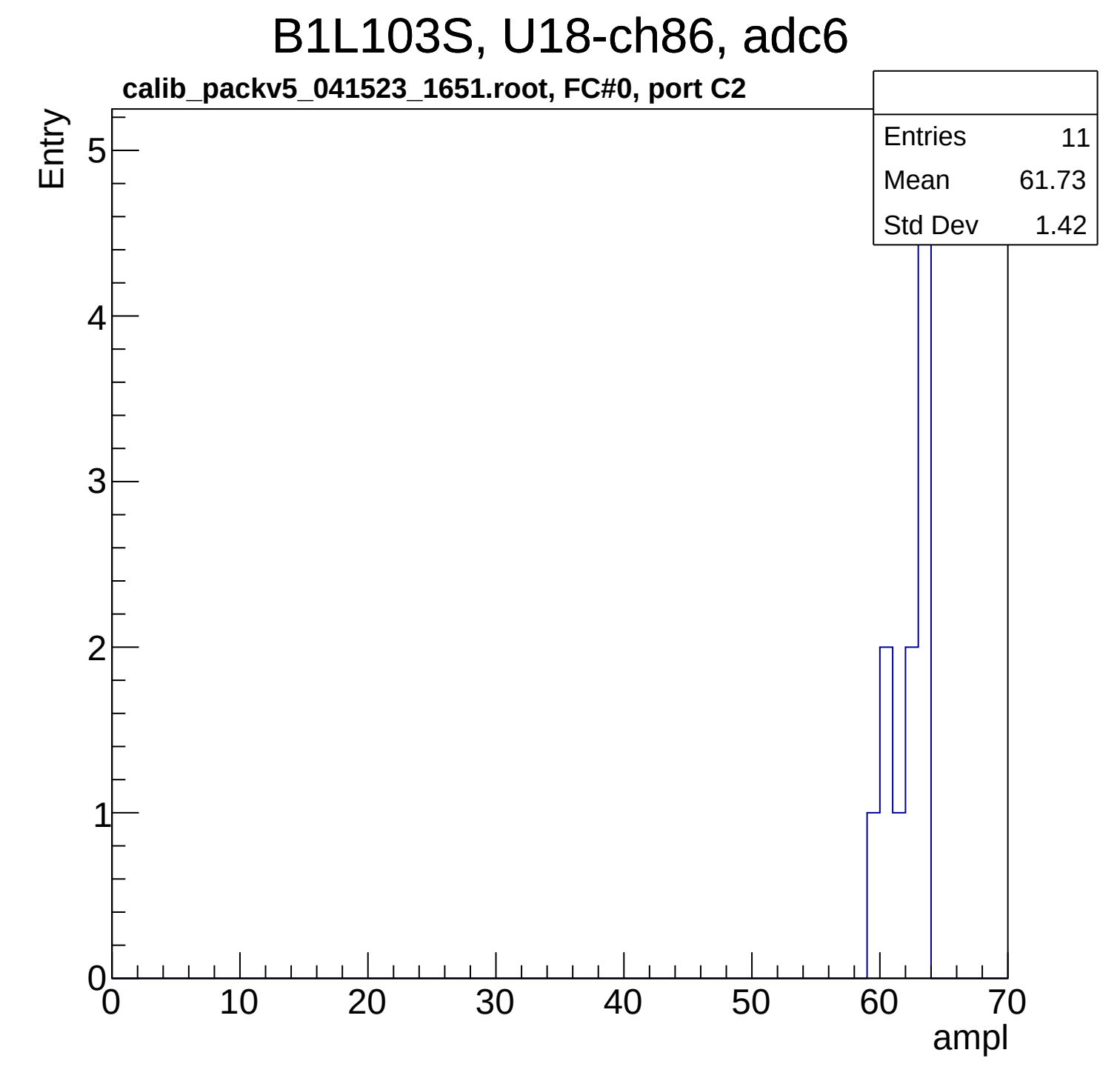
B1L103S, U18-ch86, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 61.73
Std Dev 1.42
Entry
ampl
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2
3
4
5
0
10
20
30
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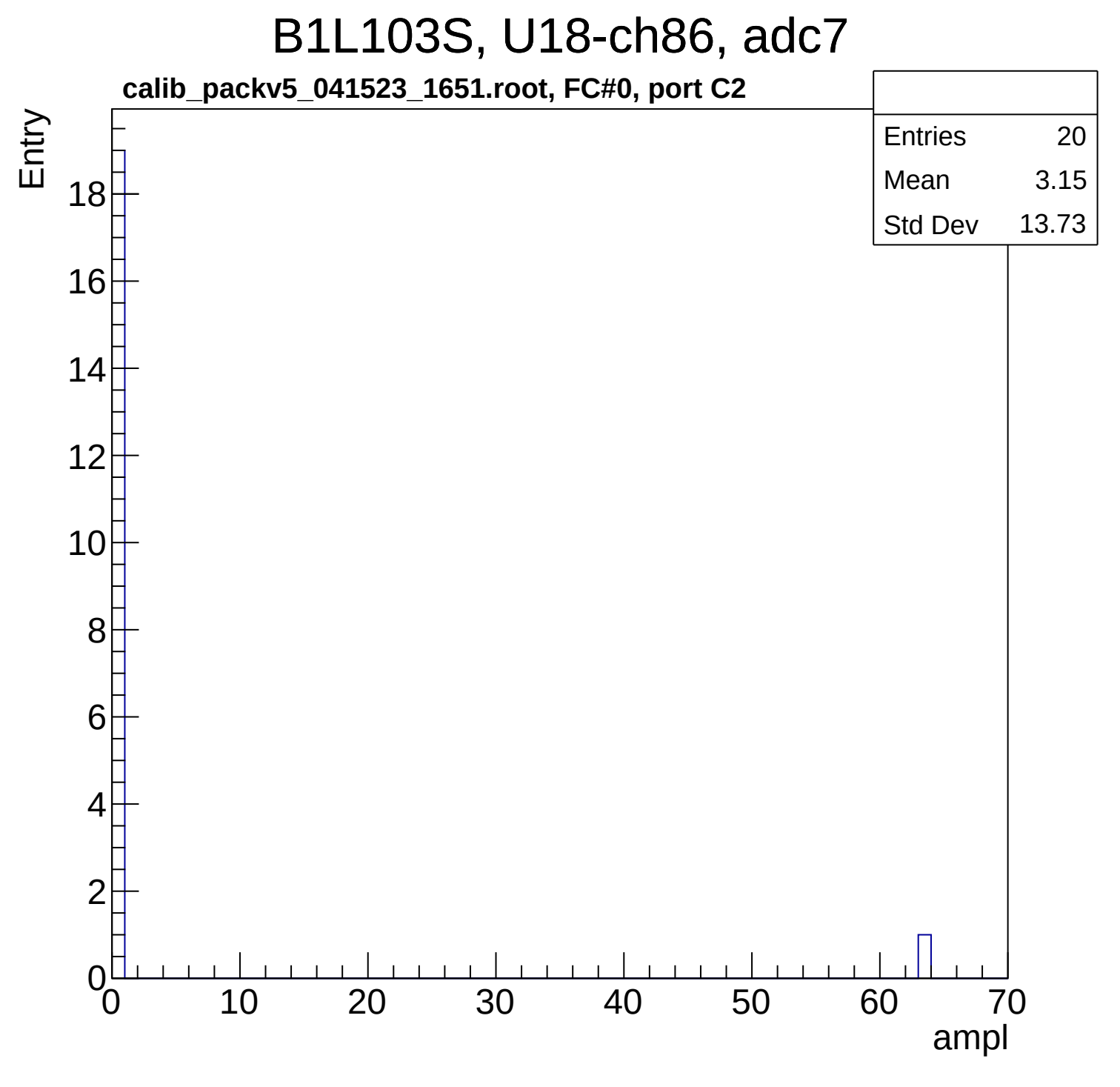
50
60
70


B1L103S, U18-ch86, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
0
2
4
6
8
10
12
14
16
18
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10
20
30
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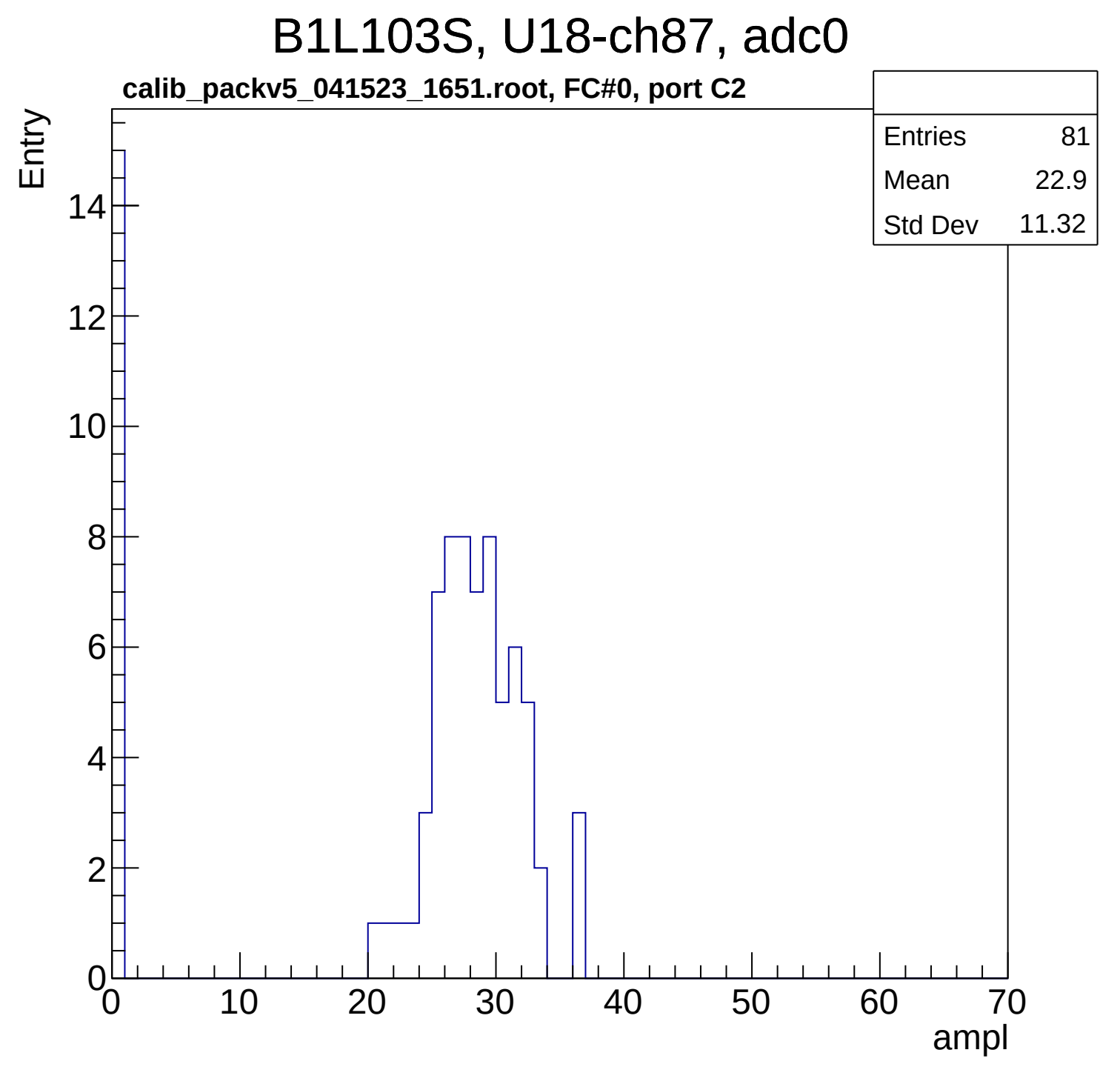
50
60
70
ampl


B1L103S, U18-ch87, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 22.9
Std Dev 11.32
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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40
50
60
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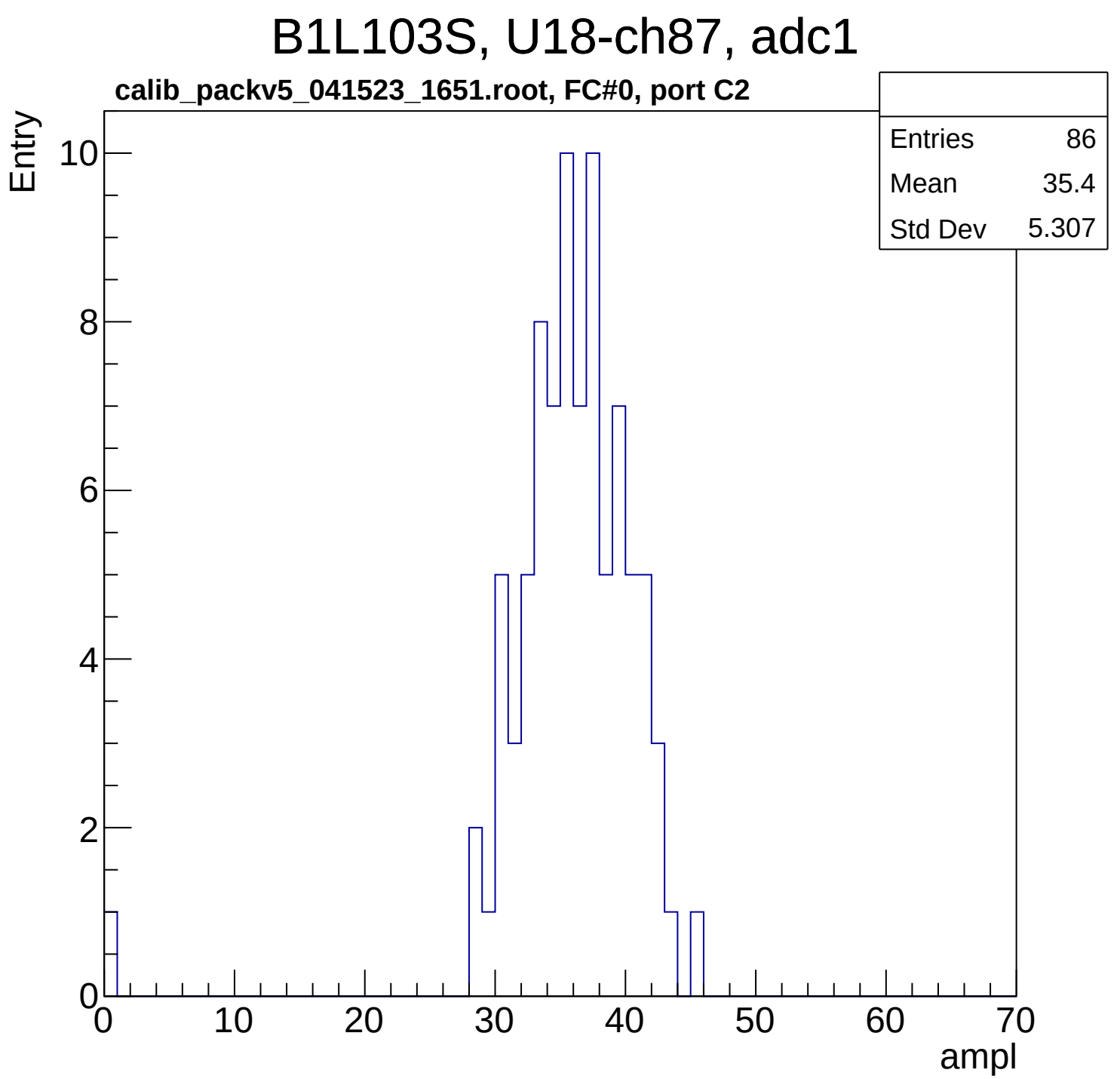
B1L103S, U18-ch87, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 35.4
Std Dev 5.307
Entry
ampl
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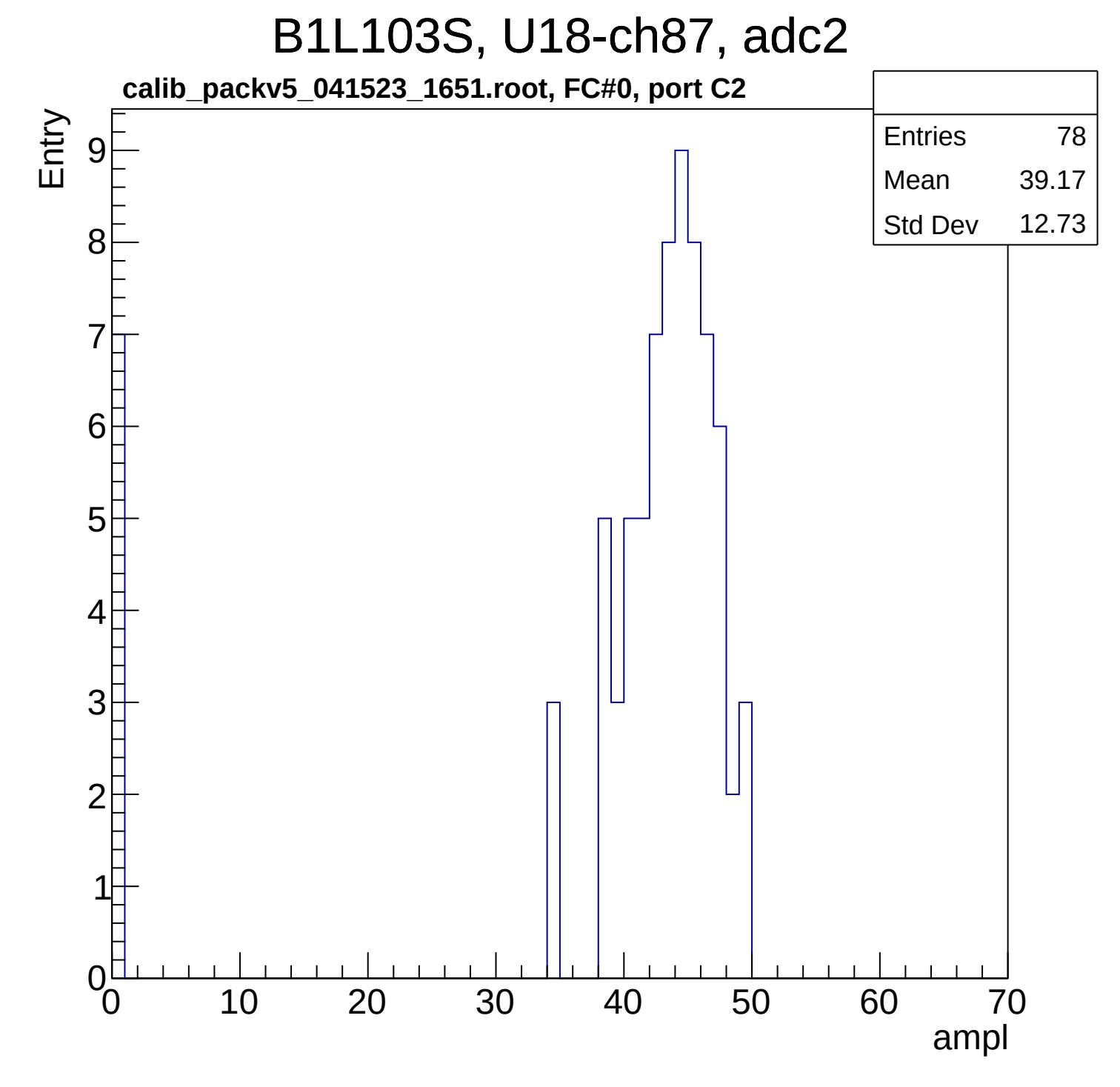
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U18-ch87, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 39.17
Std Dev 12.73
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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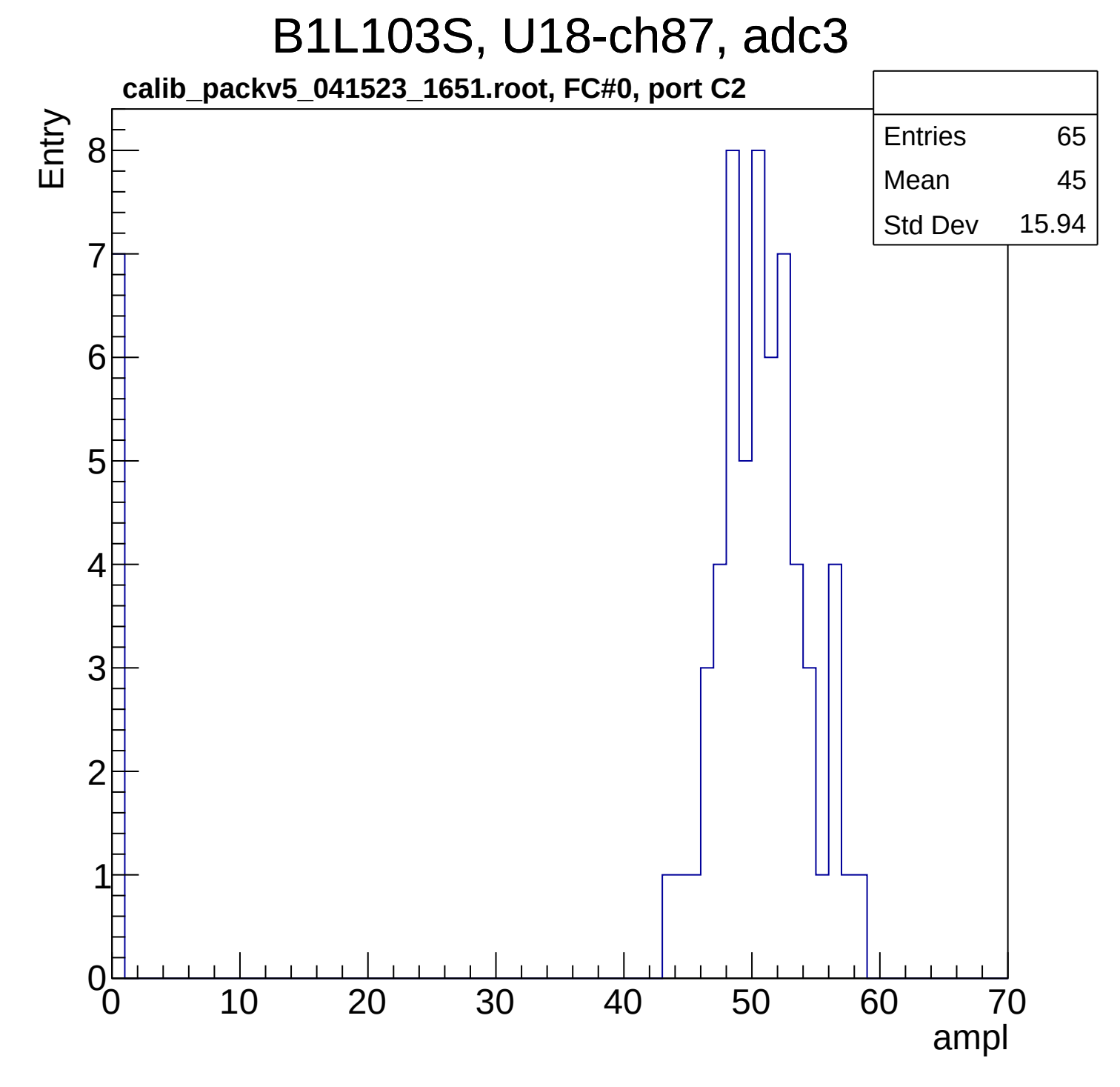
B1L103S, U18-ch87, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 45
Std Dev 15.94
Entry
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4
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6
7
8
0
10
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30
40
50
60
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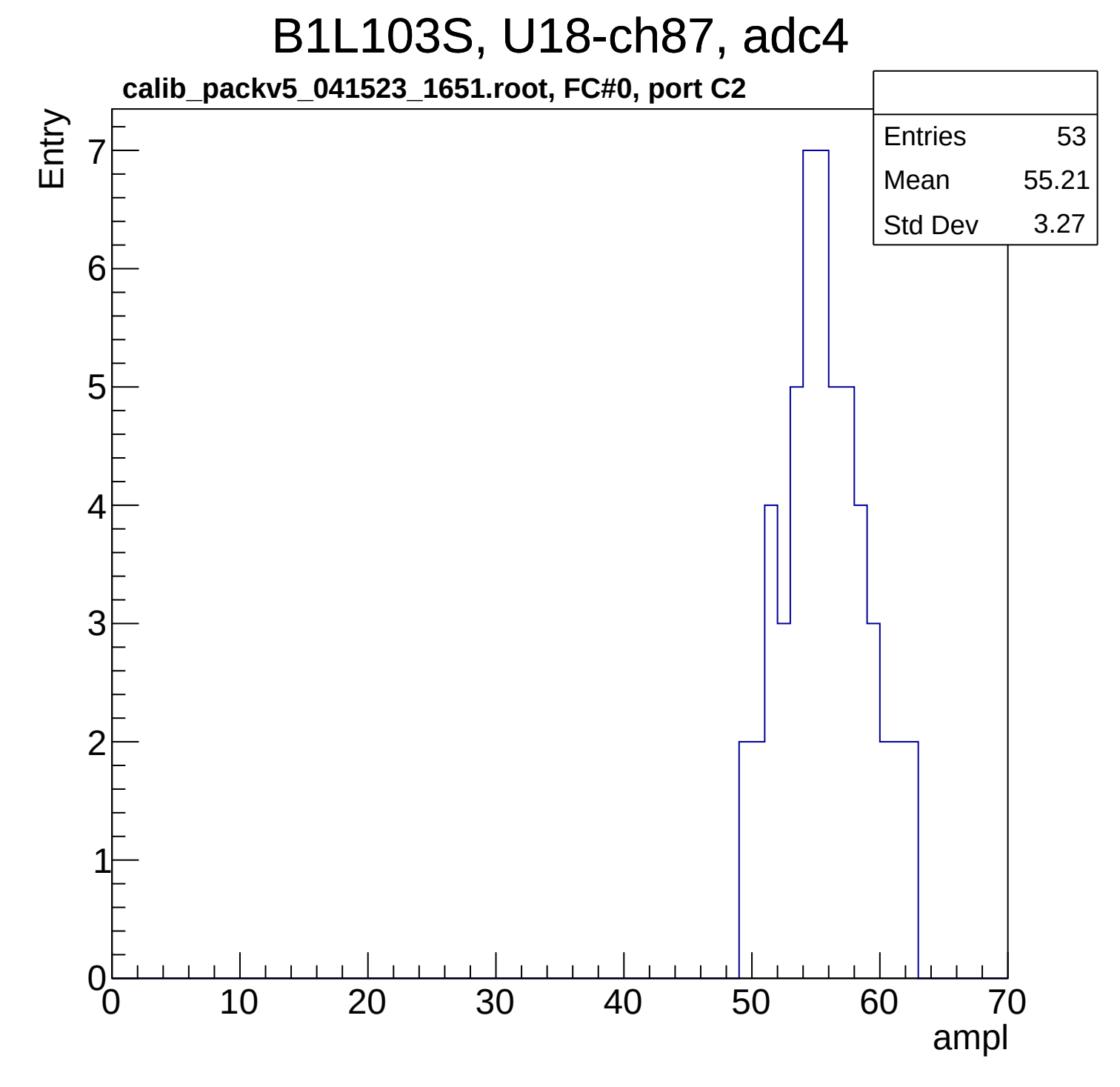
B1L103S, U18-ch87, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 55.21
Std Dev 3.27
Entry
ampl
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4
5
6
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0
10
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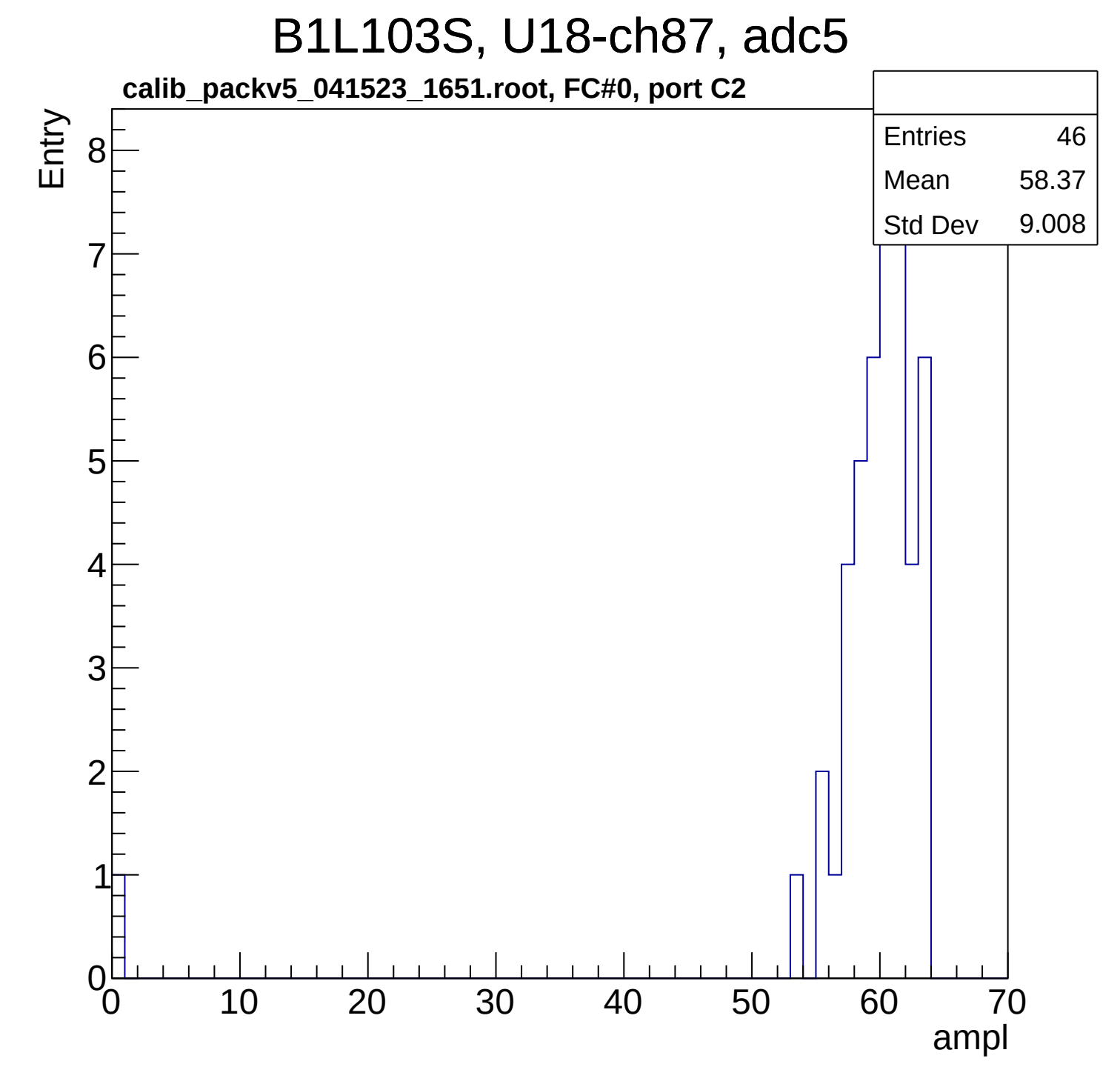
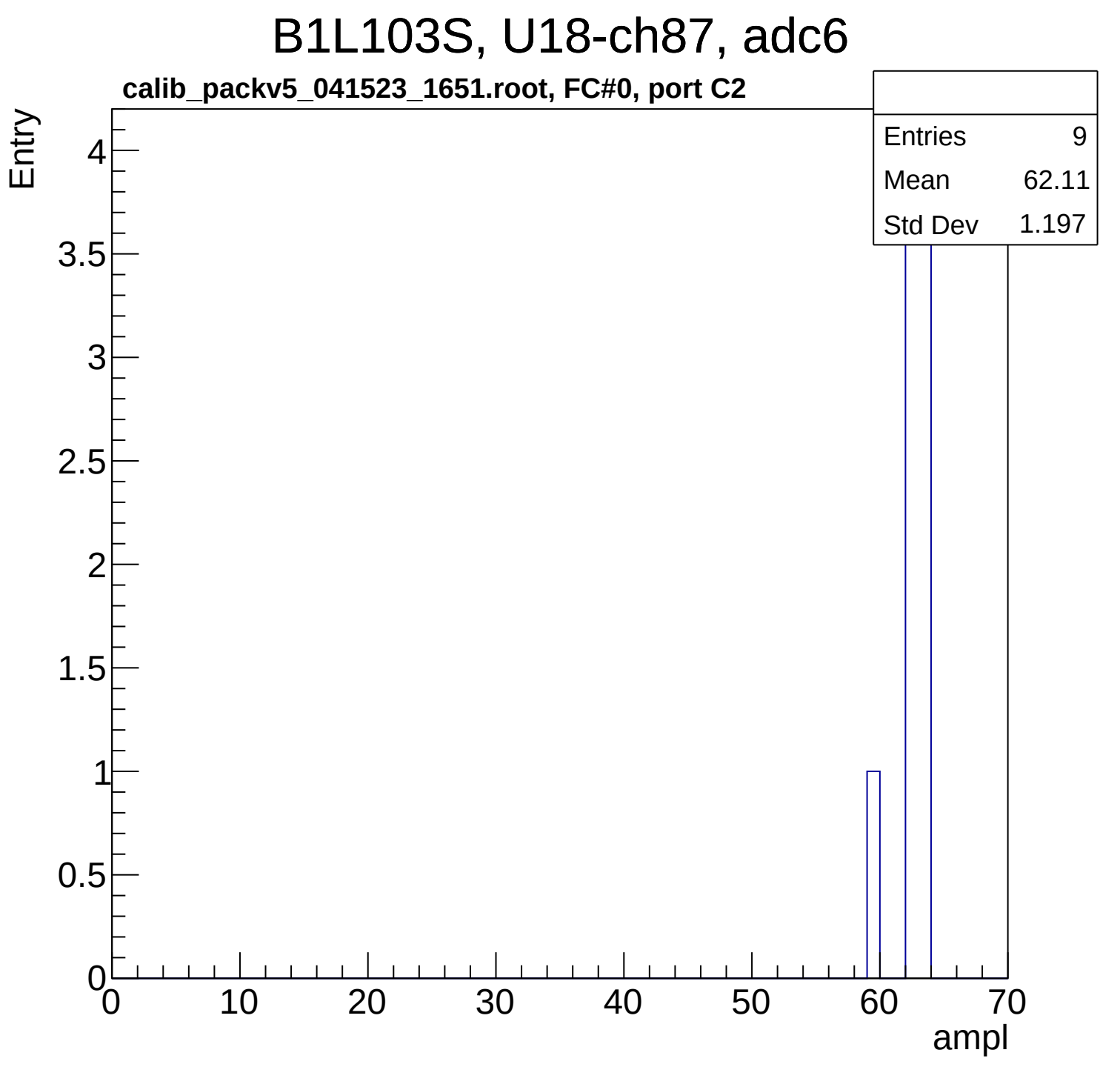
30
40
50
60
70


B1L103S, U18-ch87, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 58.37
Std Dev 9.008
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch87, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 9
Mean 62.11
Std Dev 1.197
Entry
ampl
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0.5
1
1.5
2
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3
3.5
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0
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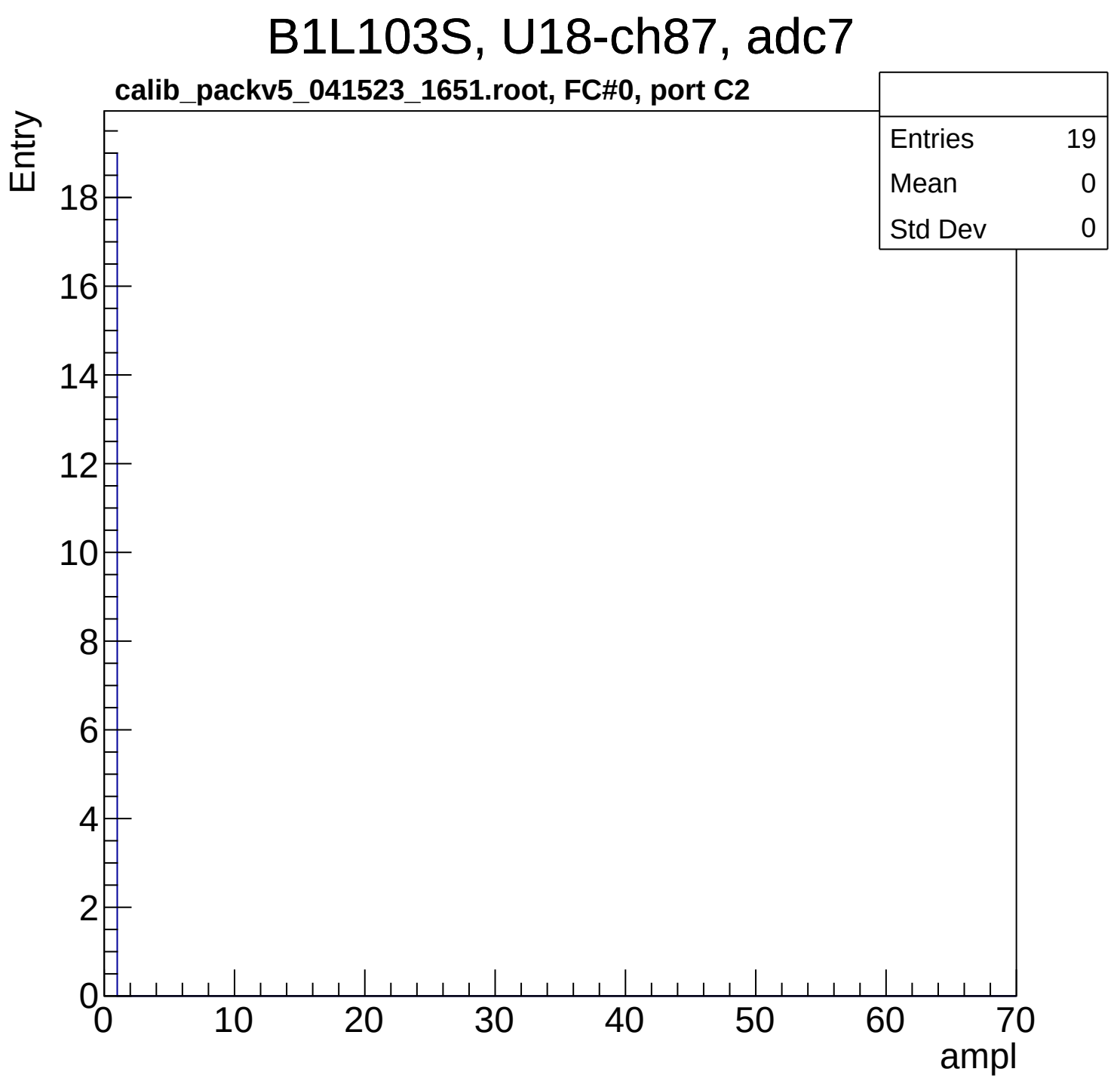
B1L103S, U18-ch87, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
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6
8
10
12
14
16
18
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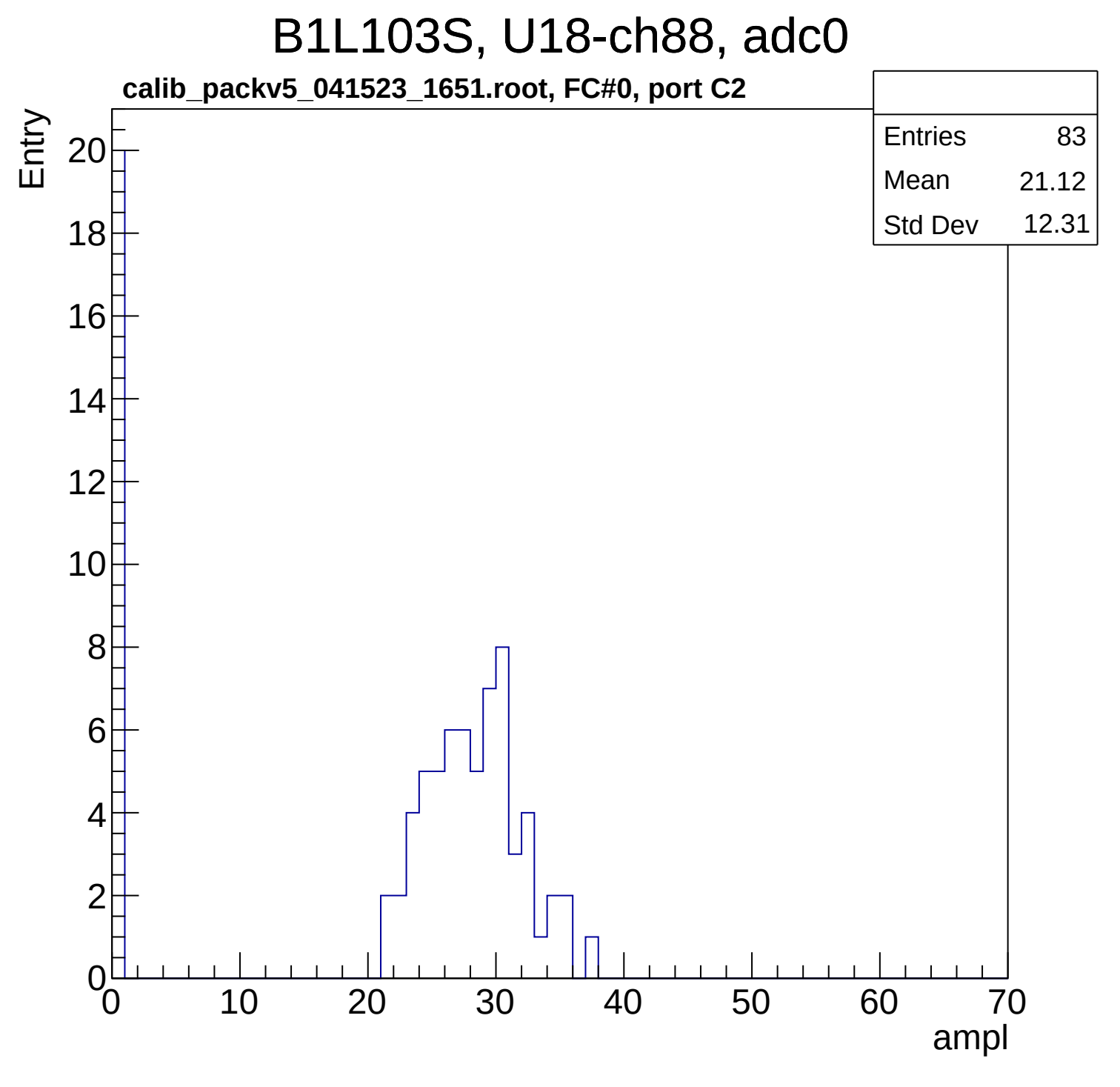
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch88, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 21.12
Std Dev 12.31
Entry
ampl
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0
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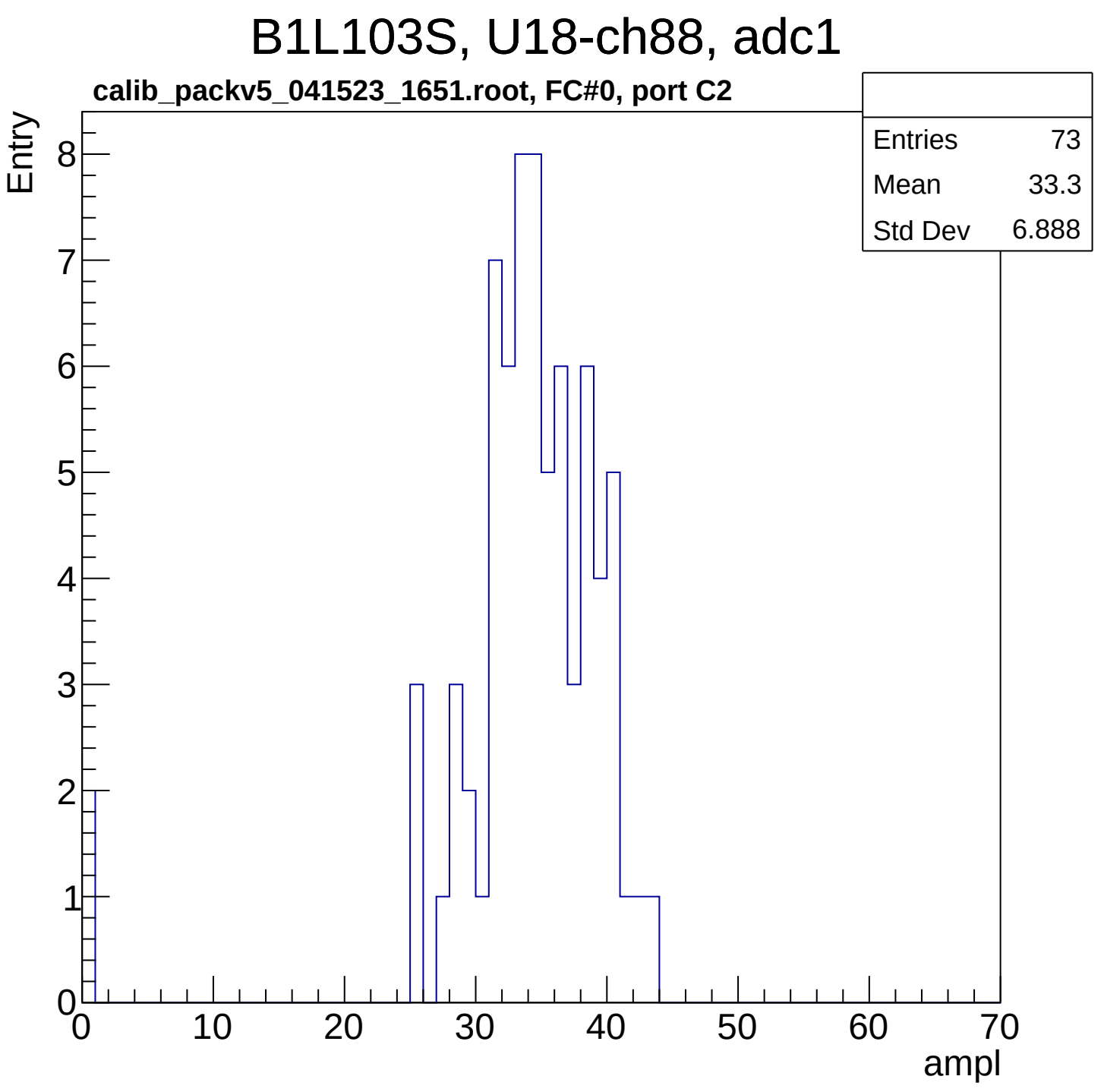
B1L103S, U18-ch88, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 33.3
Std Dev 6.888
Entry
ampl
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2
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4
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0
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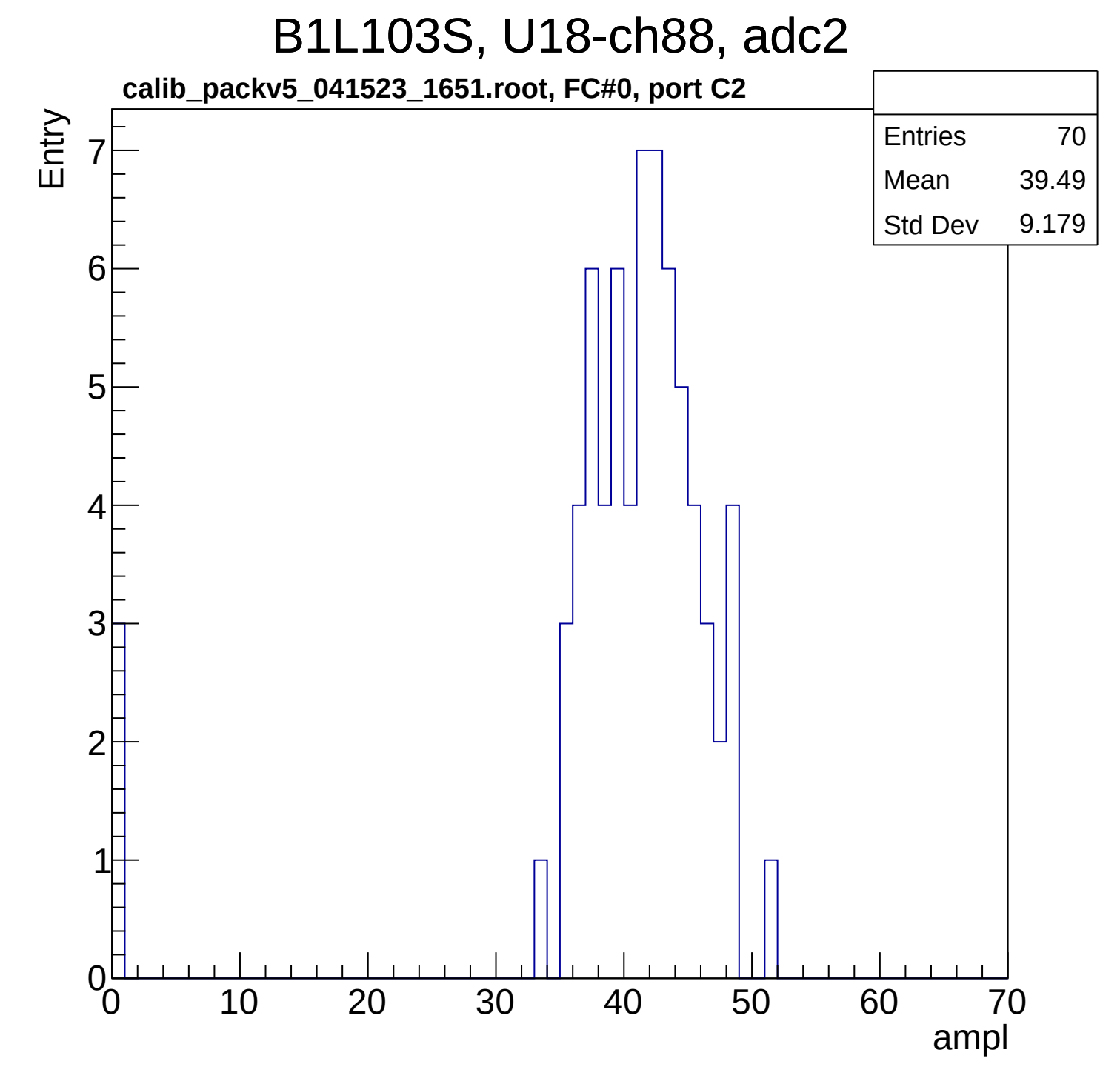
B1L103S, U18-ch88, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 39.49
Std Dev 9.179
Entry
ampl
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1
2
3
4
5
6
7
0
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20
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40
50
60
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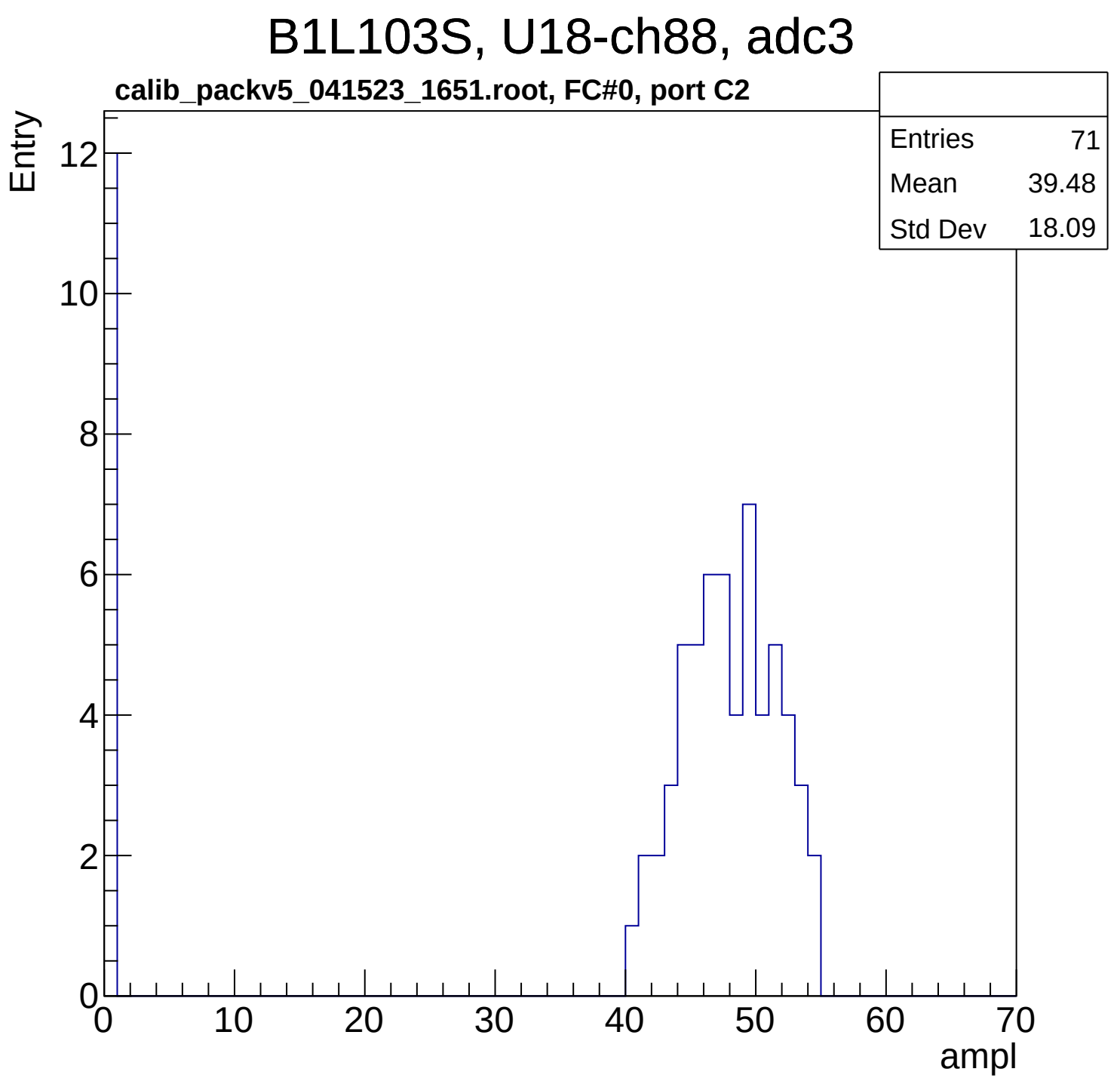
B1L103S, U18-ch88, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 39.48
Std Dev 18.09
Entry
0
2
4
6
8
10
12
0
10
20
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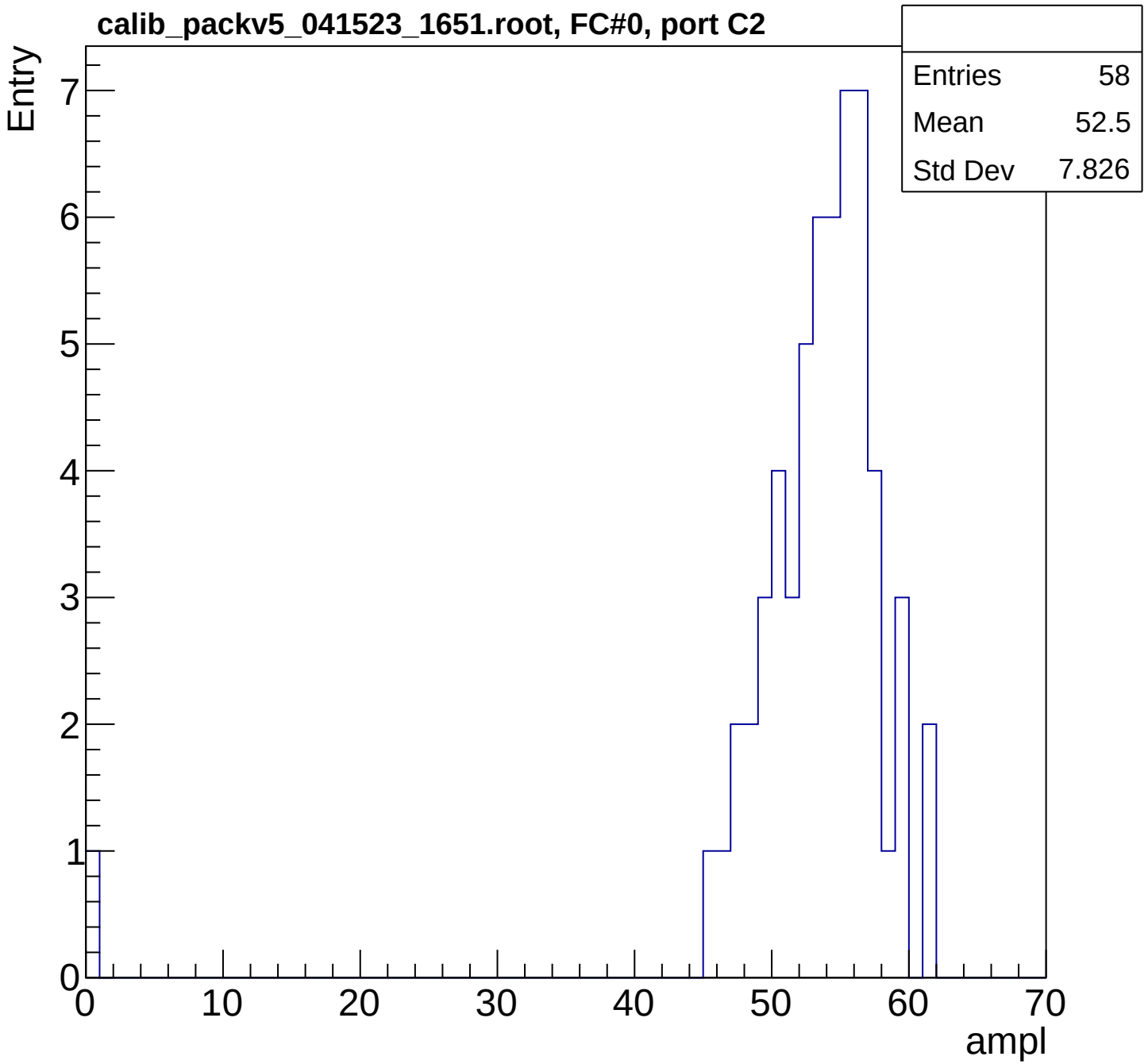
40
50
60
70
ampl


B1L103S, U18-ch88, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 52.5
Std Dev 7.826
Entry
ampl
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1
2
3
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6
7
0
10
20
30
40
50
60
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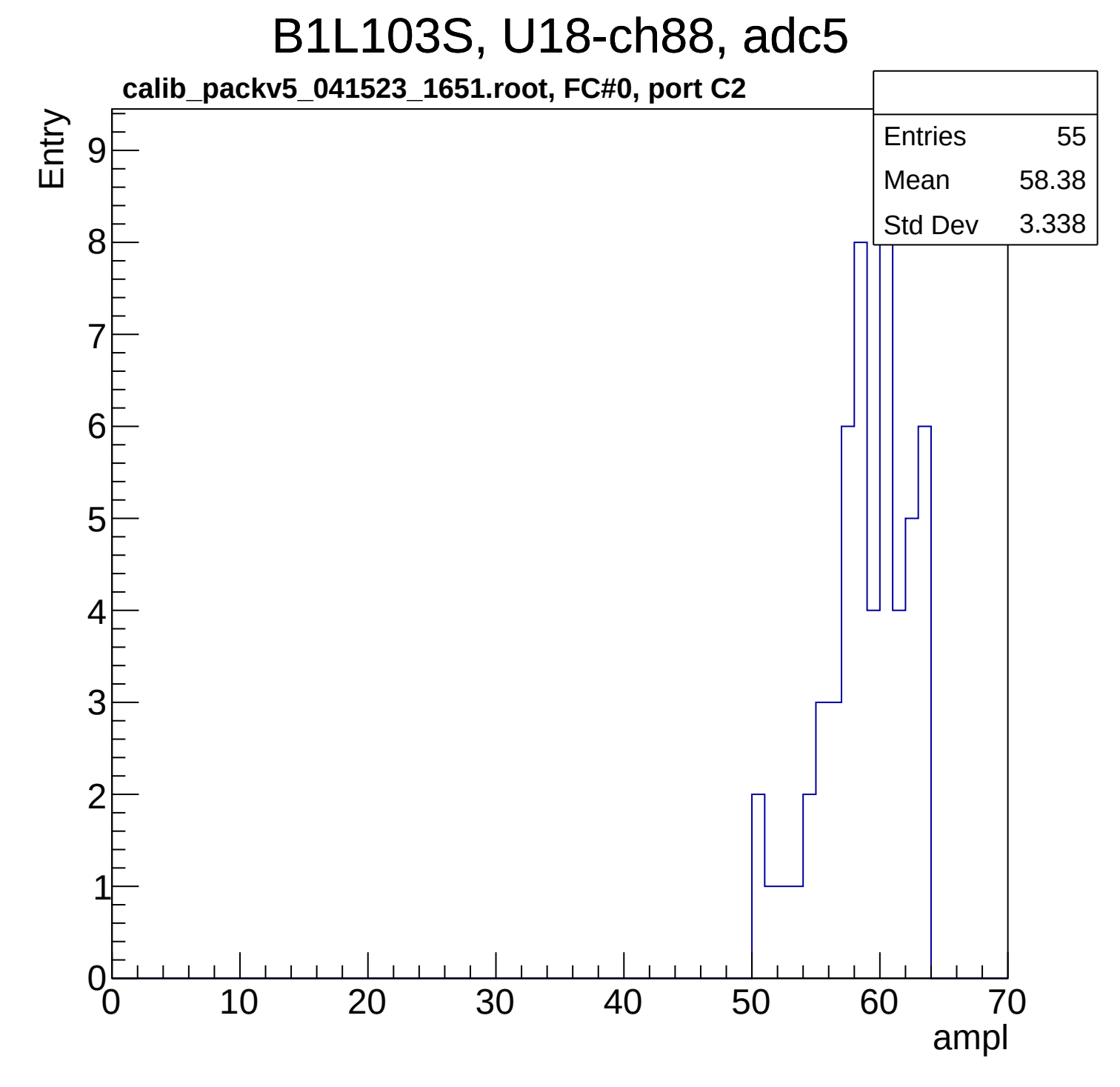
B1L103S, U18-ch88, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 58.38
Std Dev 3.338
Entry
ampl
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40
50
60
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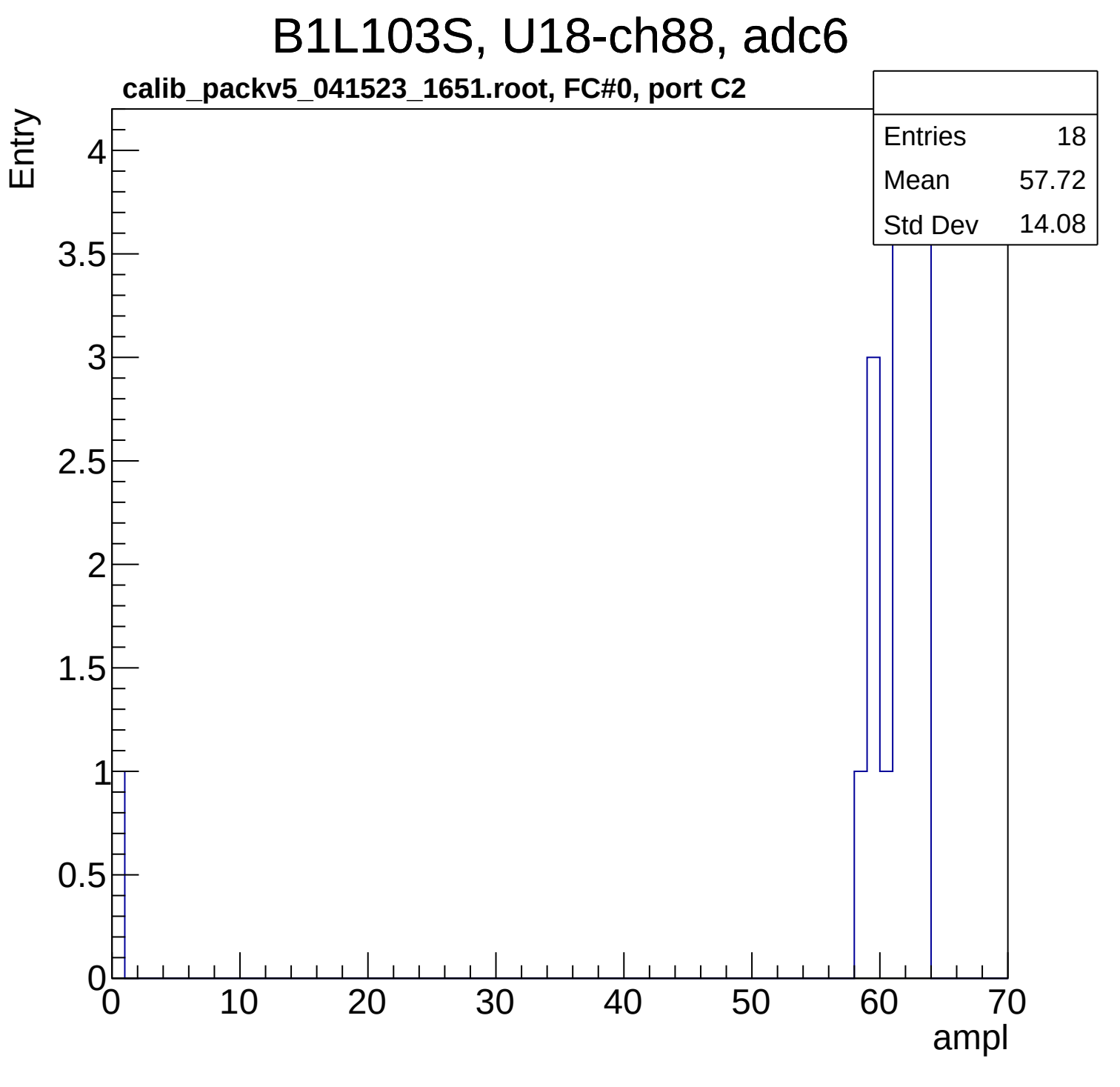
B1L103S, U18-ch88, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 57.72
Std Dev 14.08
Entry
ampl
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0.5
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1.5
2
2.5
3
3.5
4
0
10
20
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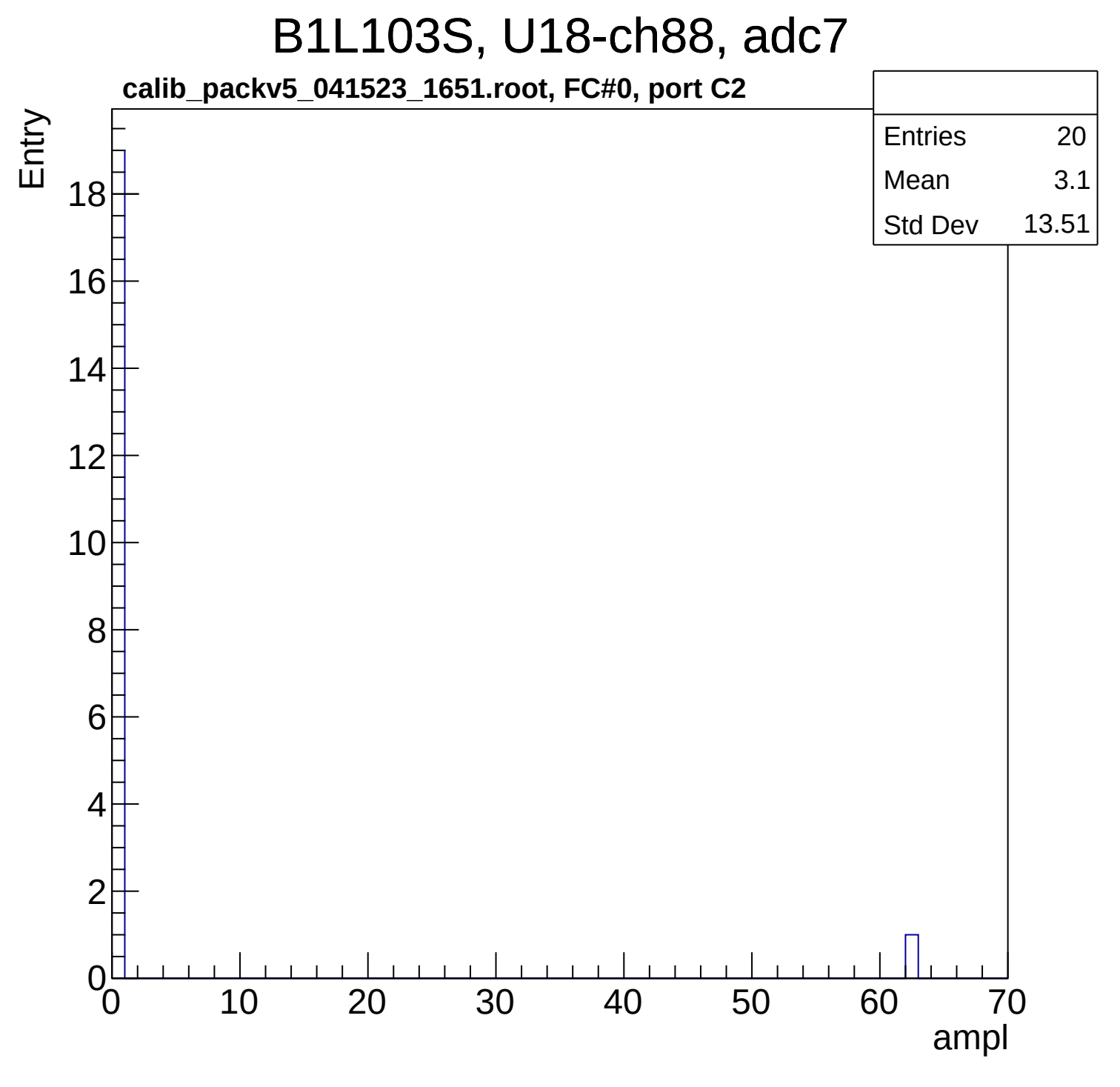
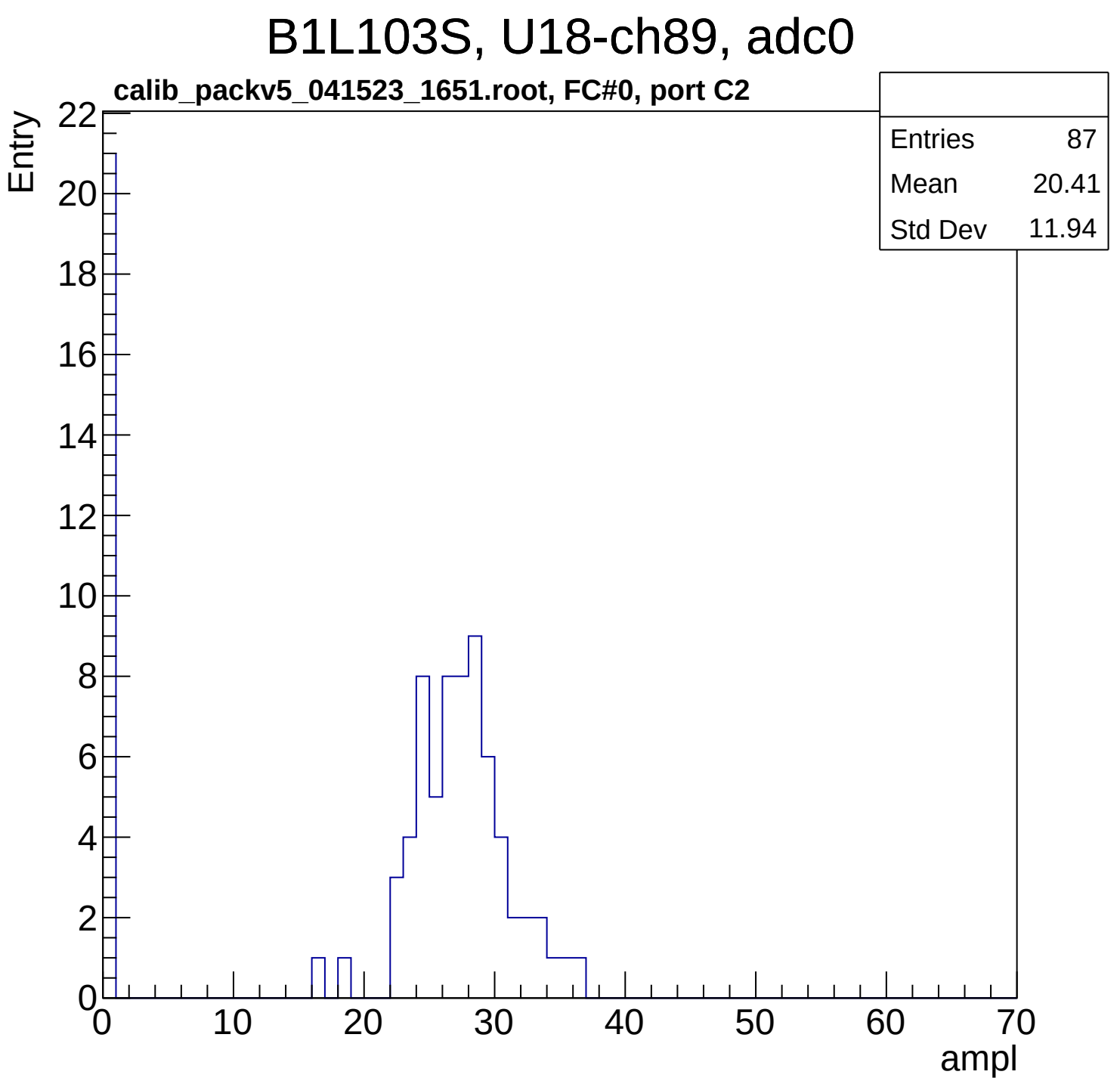
40
50
60
70


B1L103S, U18-ch88, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.1
Std Dev 13.51
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch89, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 87
Mean 20.41
Std Dev 11.94
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
22
0
10
20
30
40
50
60
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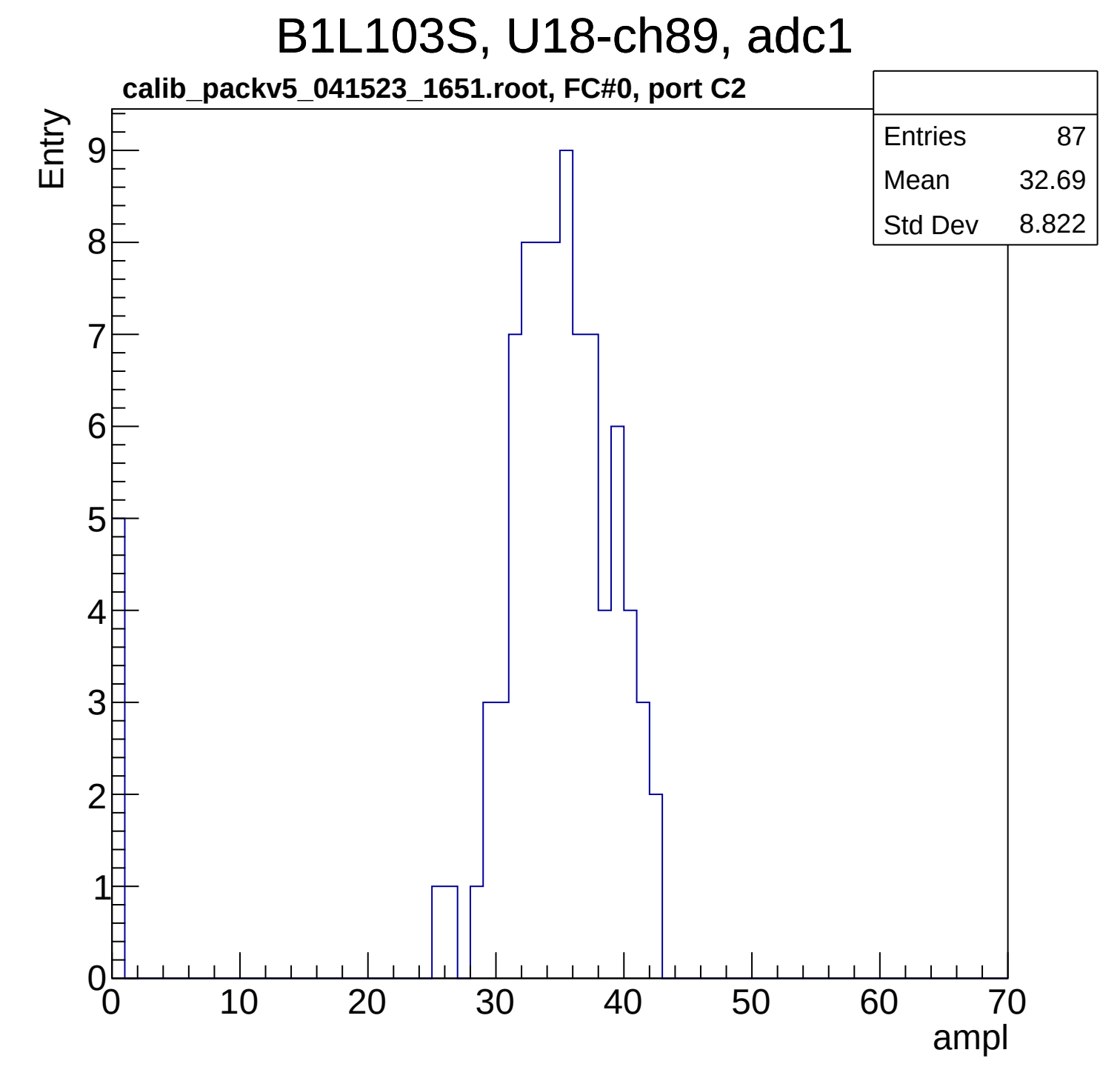
B1L103S, U18-ch89, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 87
Mean 32.69
Std Dev 8.822
Entry
ampl
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3
4
5
6
7
8
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0
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60
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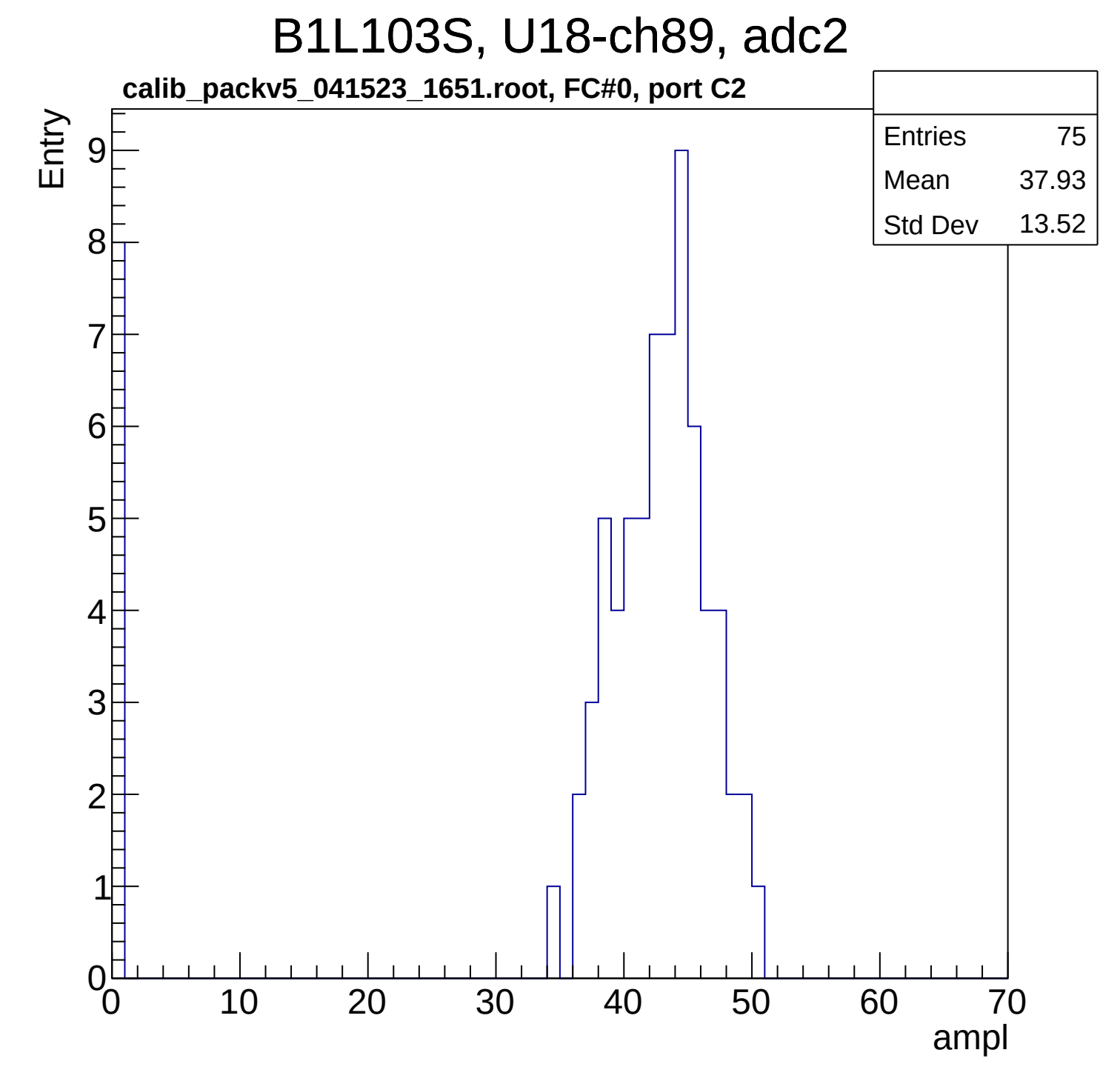
B1L103S, U18-ch89, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 37.93
Std Dev 13.52
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
50
60
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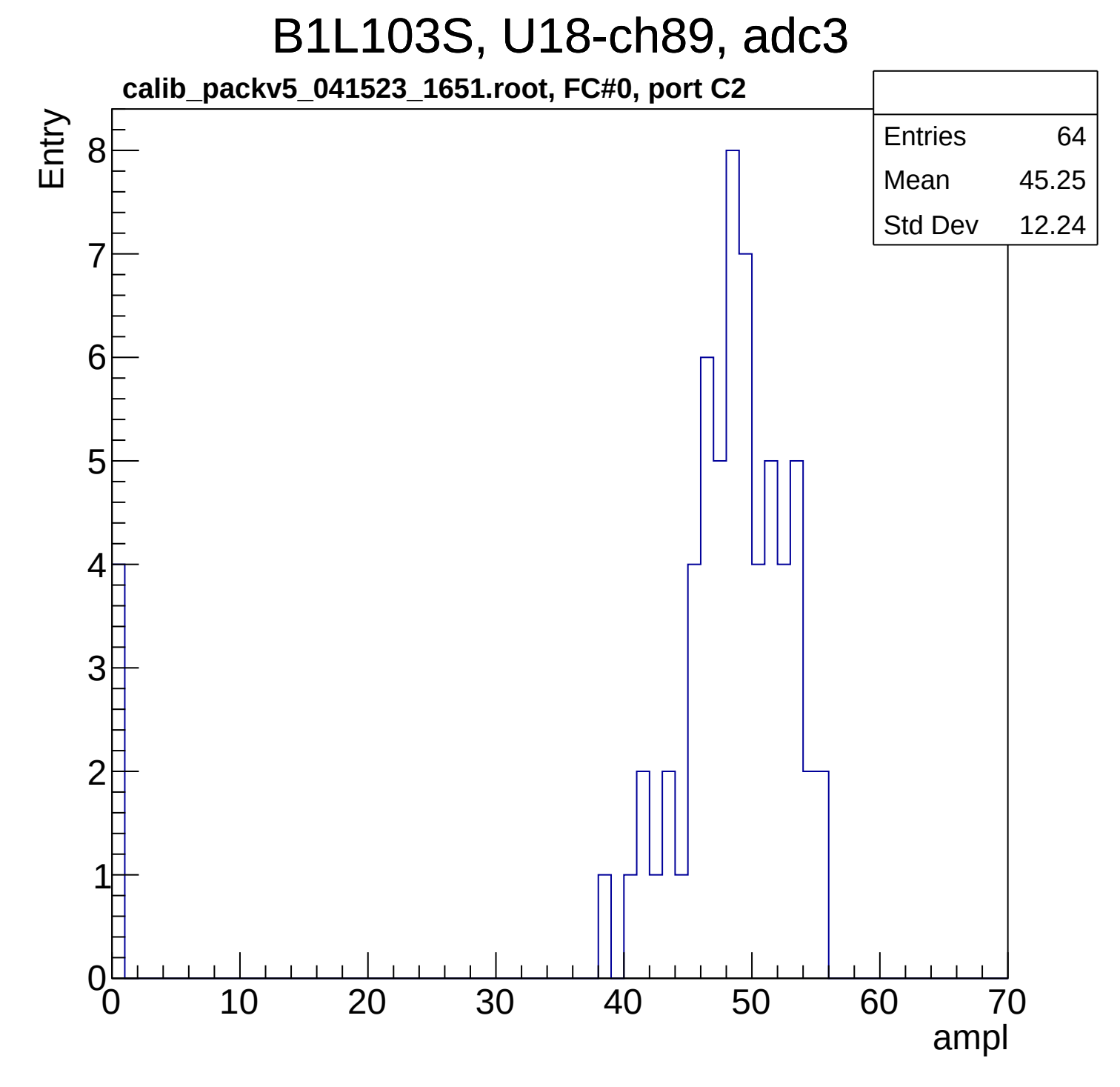
B1L103S, U18-ch89, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 45.25
Std Dev 12.24
Entry
ampl
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2
3
4
5
6
7
8
0
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20
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40
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60
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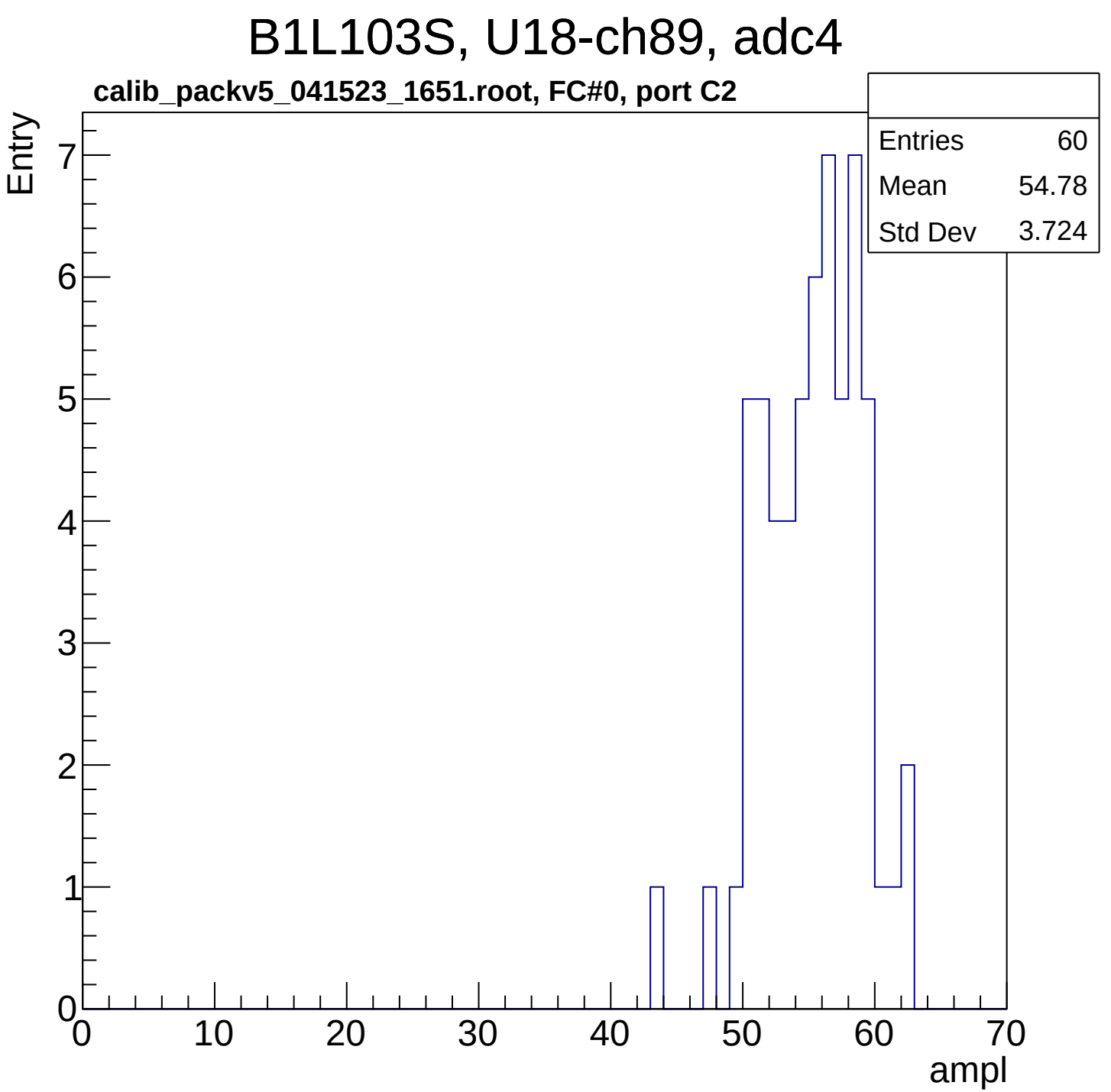
B1L103S, U18-ch89, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 54.78
Std Dev 3.724
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
30
40
50
60
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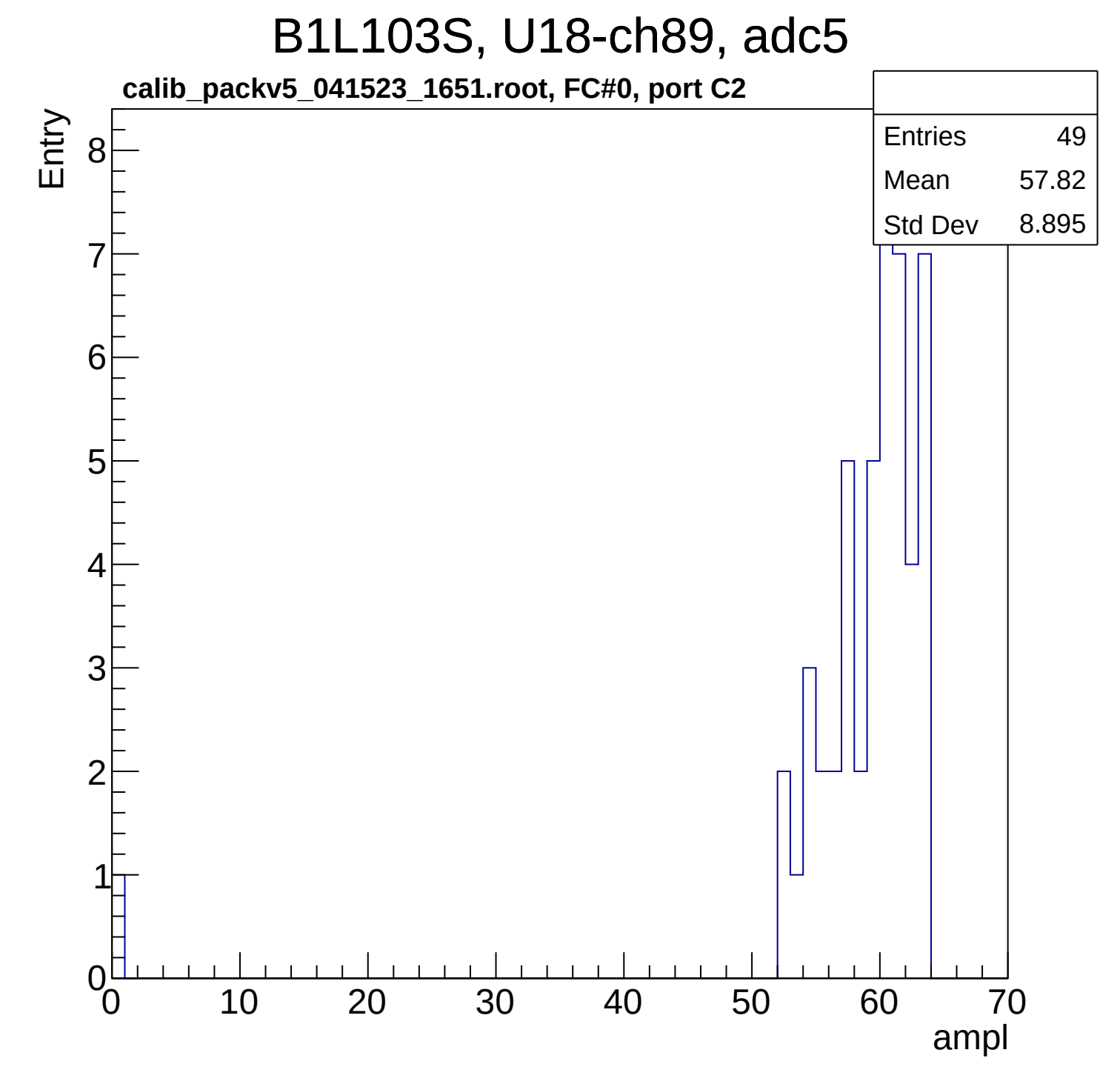
B1L103S, U18-ch89, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 57.82
Std Dev 8.895
Entry
ampl
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6
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0
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60
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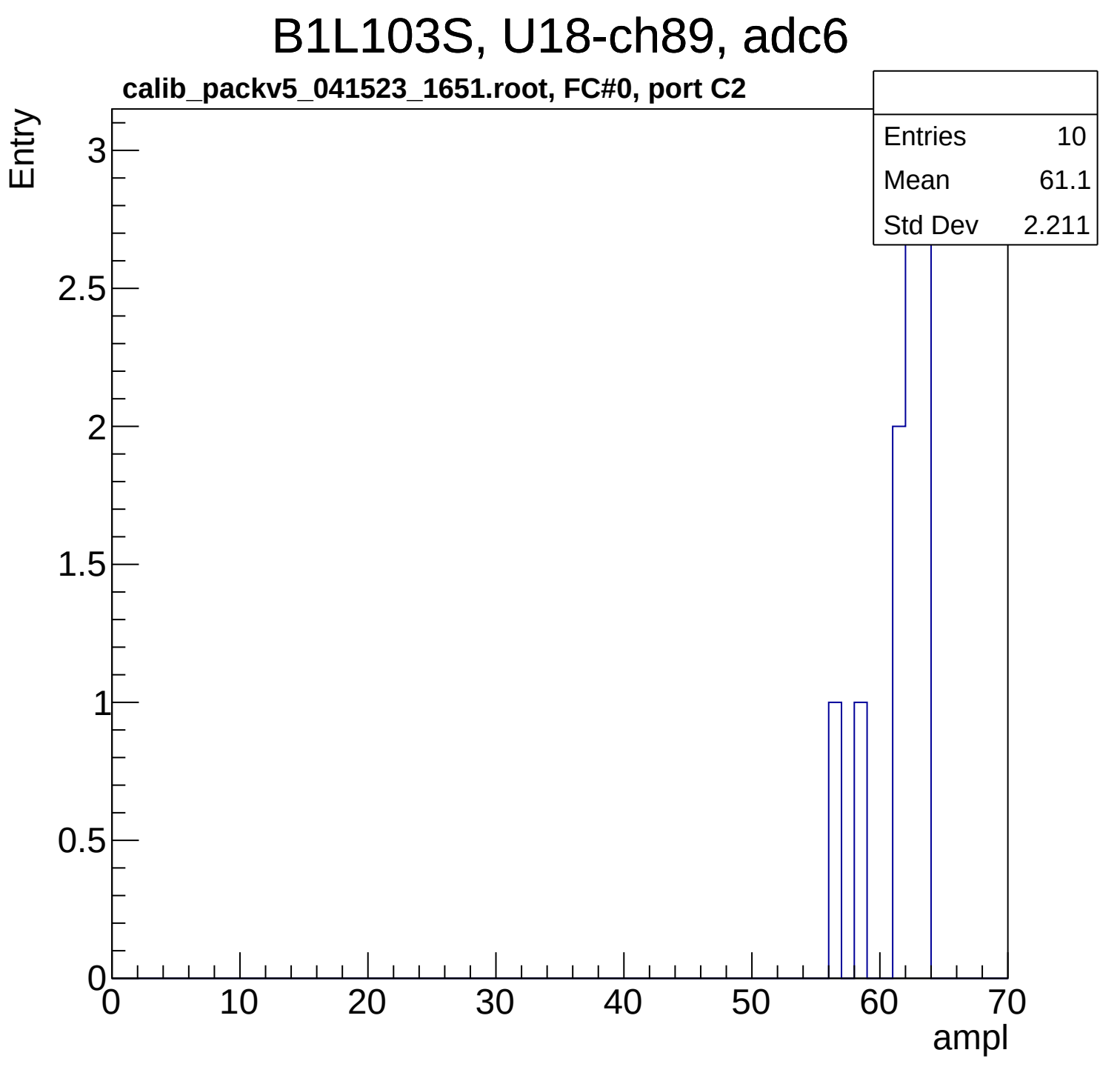
B1L103S, U18-ch89, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 61.1
Std Dev 2.211
Entry
ampl
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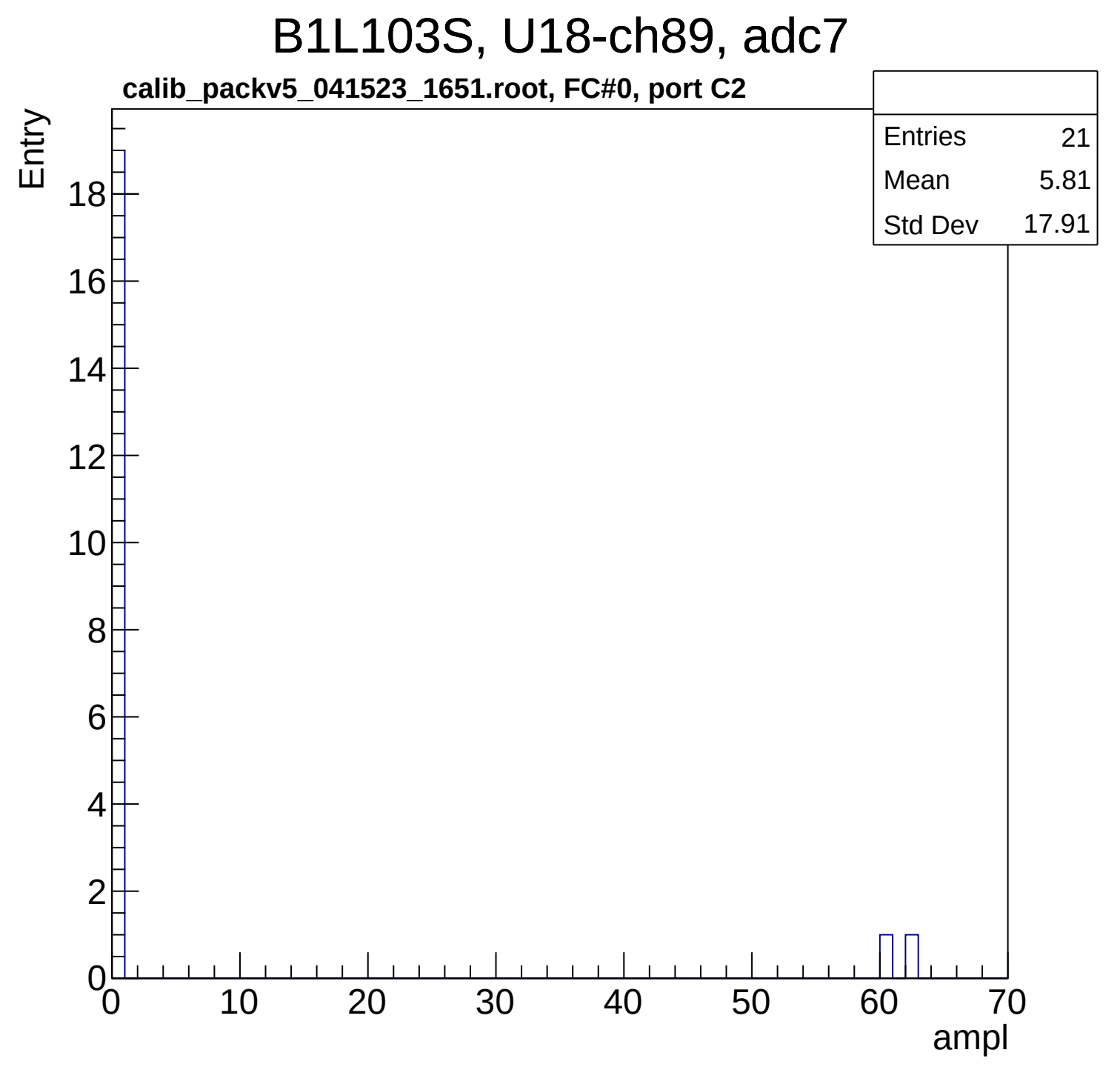
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U18-ch89, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 5.81
Std Dev 17.91
Entry
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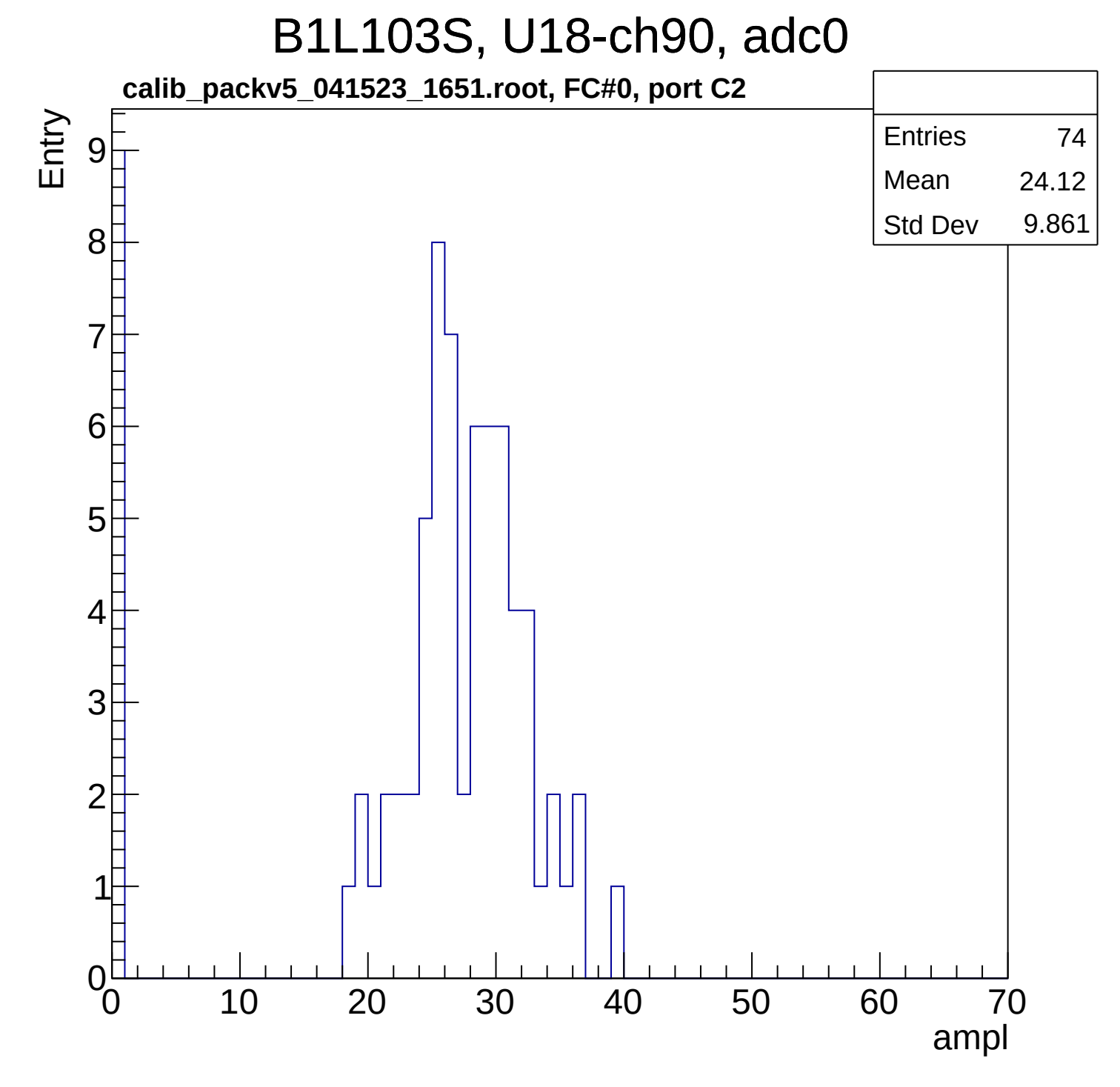
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch90, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 24.12
Std Dev 9.861
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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40
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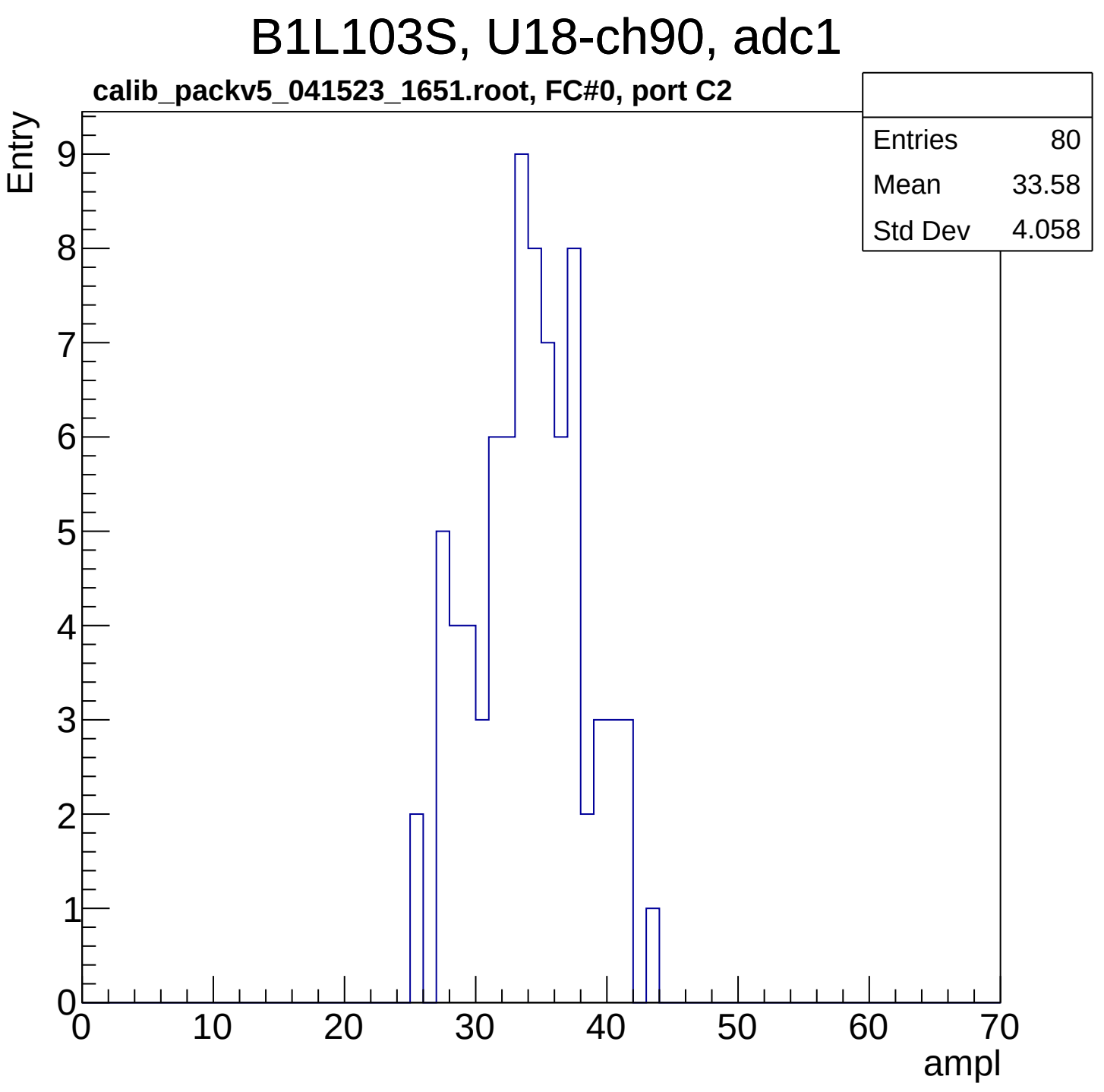
B1L103S, U18-ch90, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 33.58
Std Dev 4.058
Entry
ampl
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6
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8
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0
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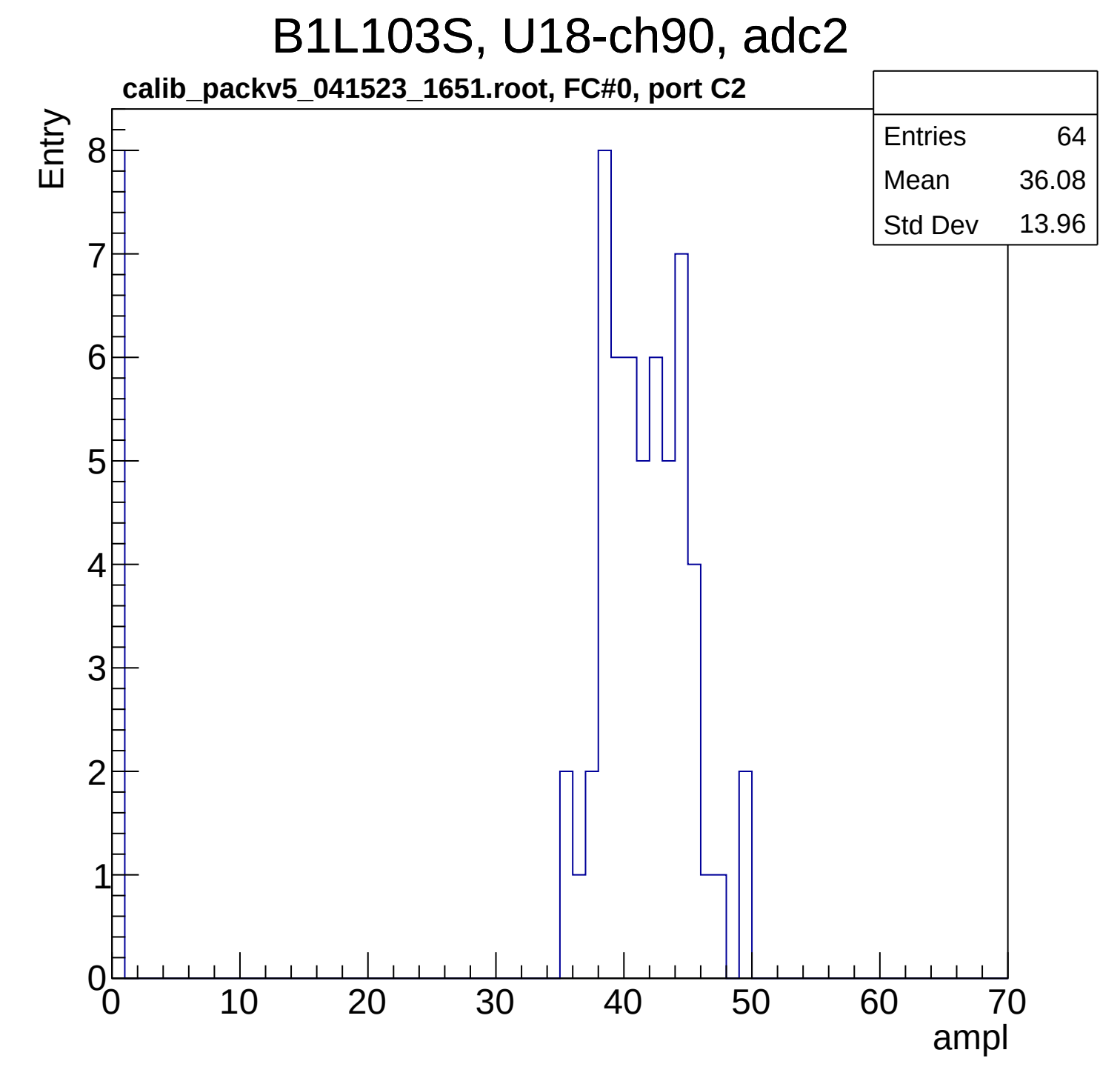
B1L103S, U18-ch90, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 36.08
Std Dev 13.96
Entry
ampl
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2
3
4
5
6
7
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0
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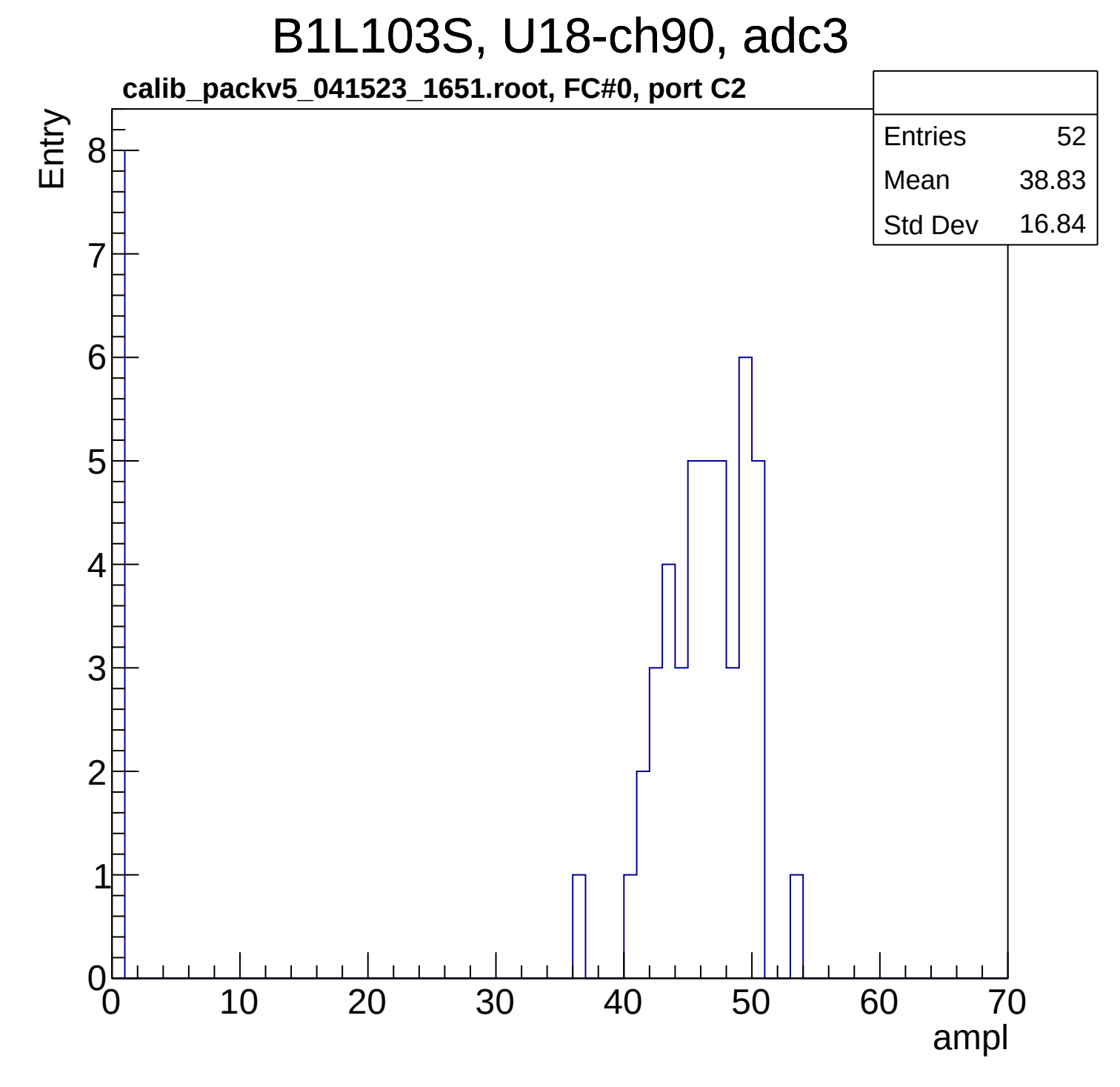
B1L103S, U18-ch90, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 38.83
Std Dev 16.84
Entry
ampl
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4
5
6
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60
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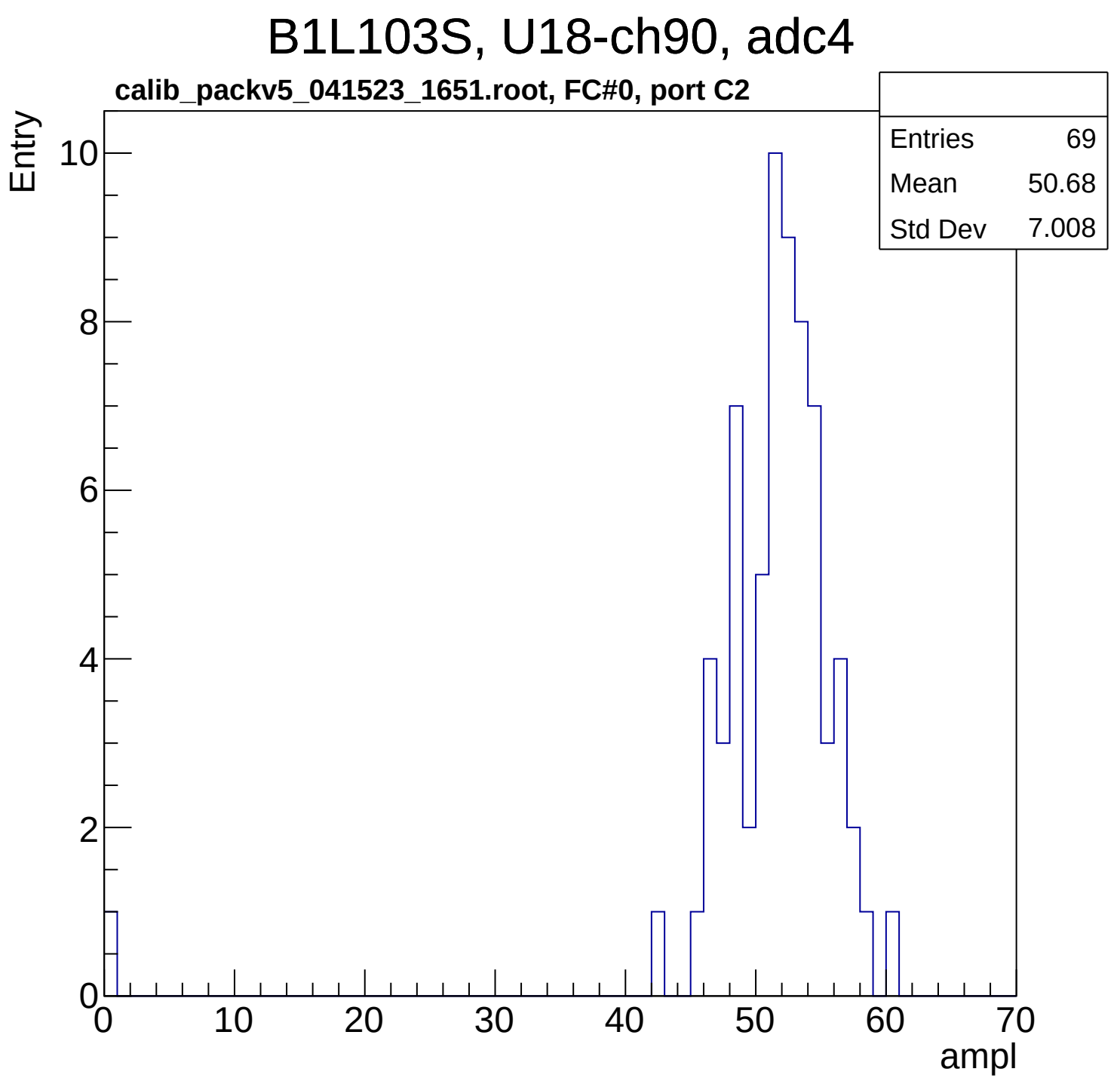
B1L103S, U18-ch90, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 50.68
Std Dev 7.008
Entry
ampl
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4
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0
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40
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60
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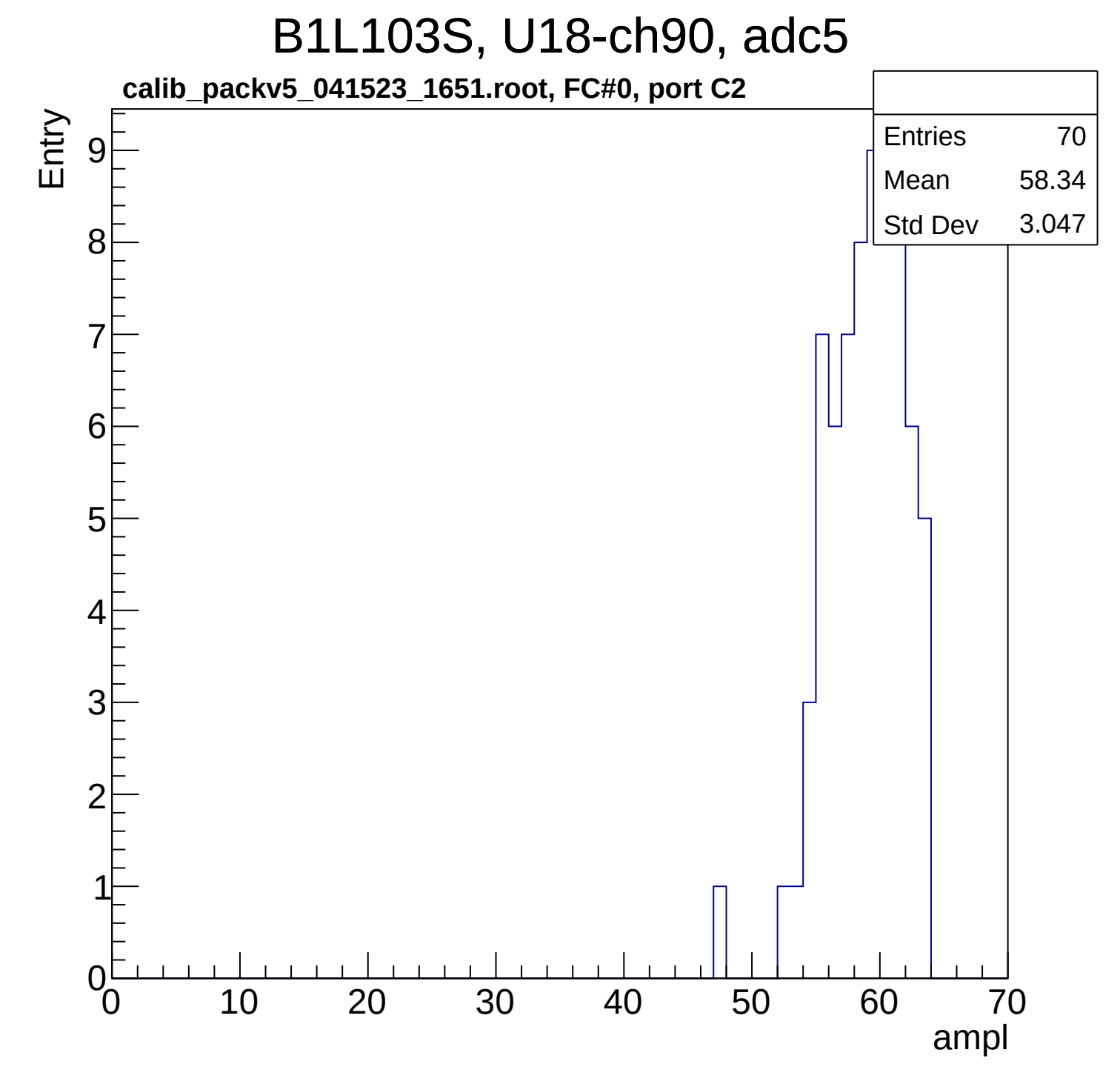
B1L103S, U18-ch90, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 58.34
Std Dev 3.047
Entry
ampl
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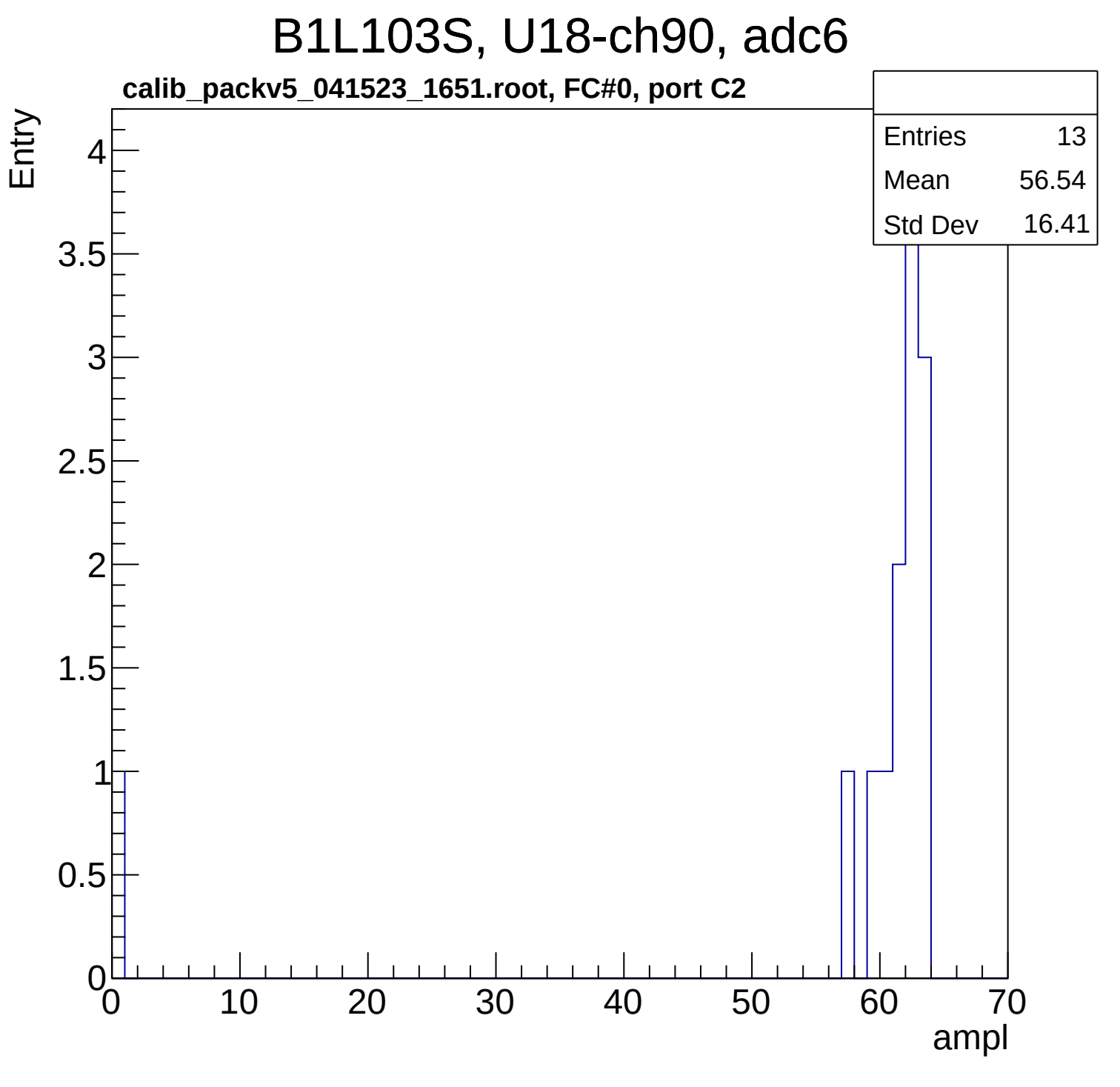
B1L103S, U18-ch90, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 13
Mean 56.54
Std Dev 16.41
Entry
ampl
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1.5
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3.5
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0
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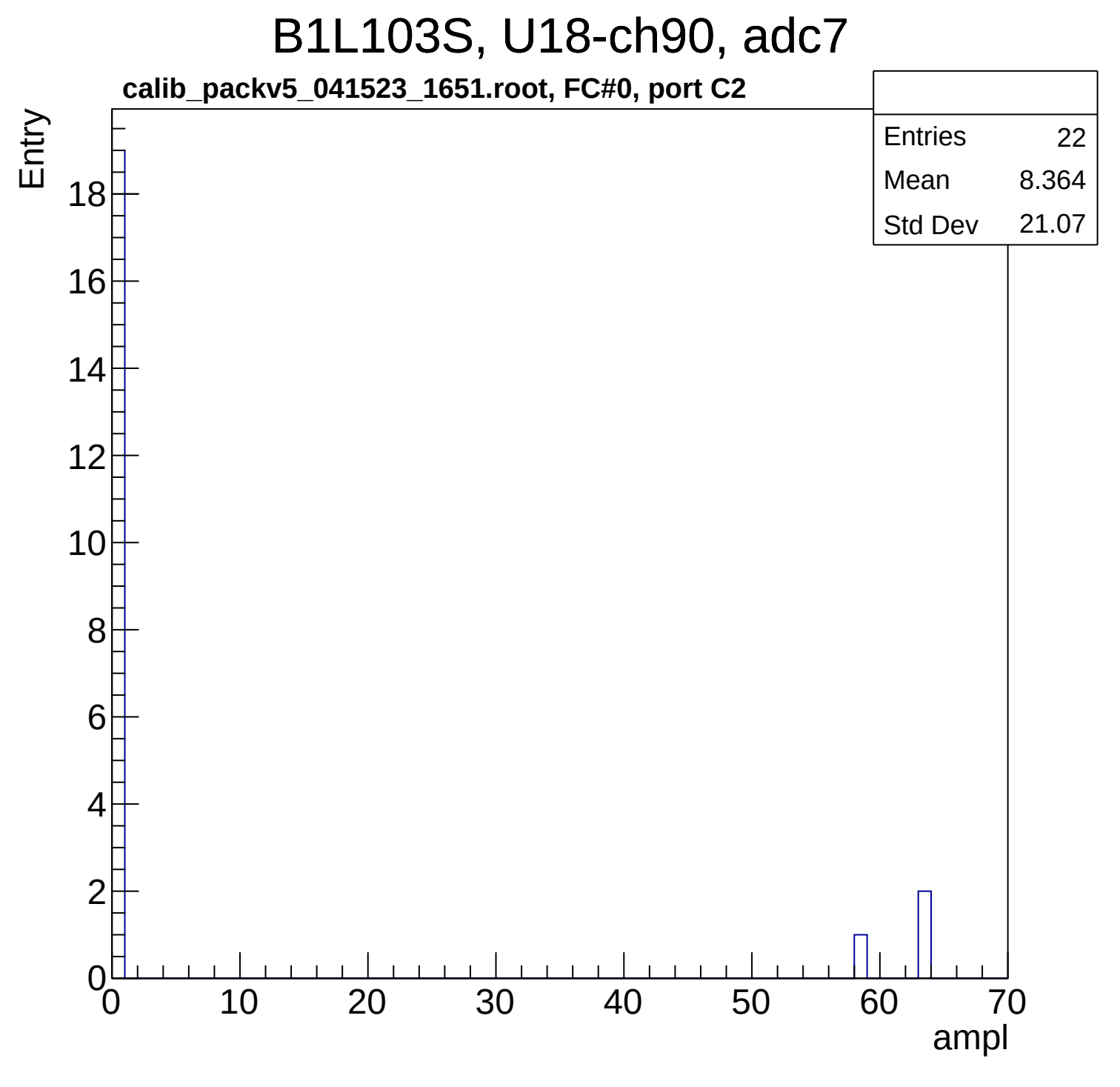
B1L103S, U18-ch90, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 8.364
Std Dev 21.07
Entry
ampl
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6
8
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12
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16
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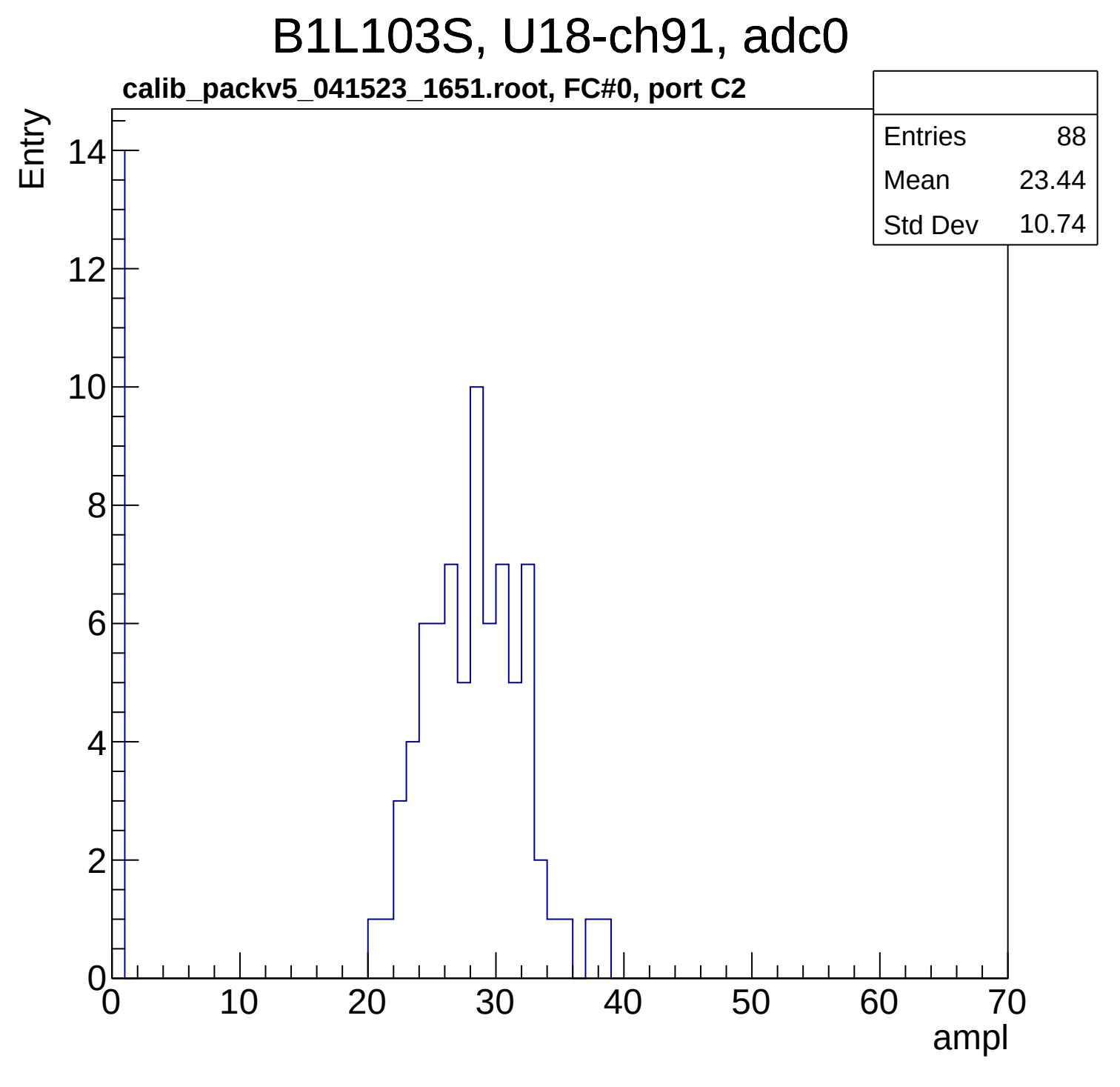
B1L103S, U18-ch91, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 88
Mean 23.44
Std Dev 10.74
Entry
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8
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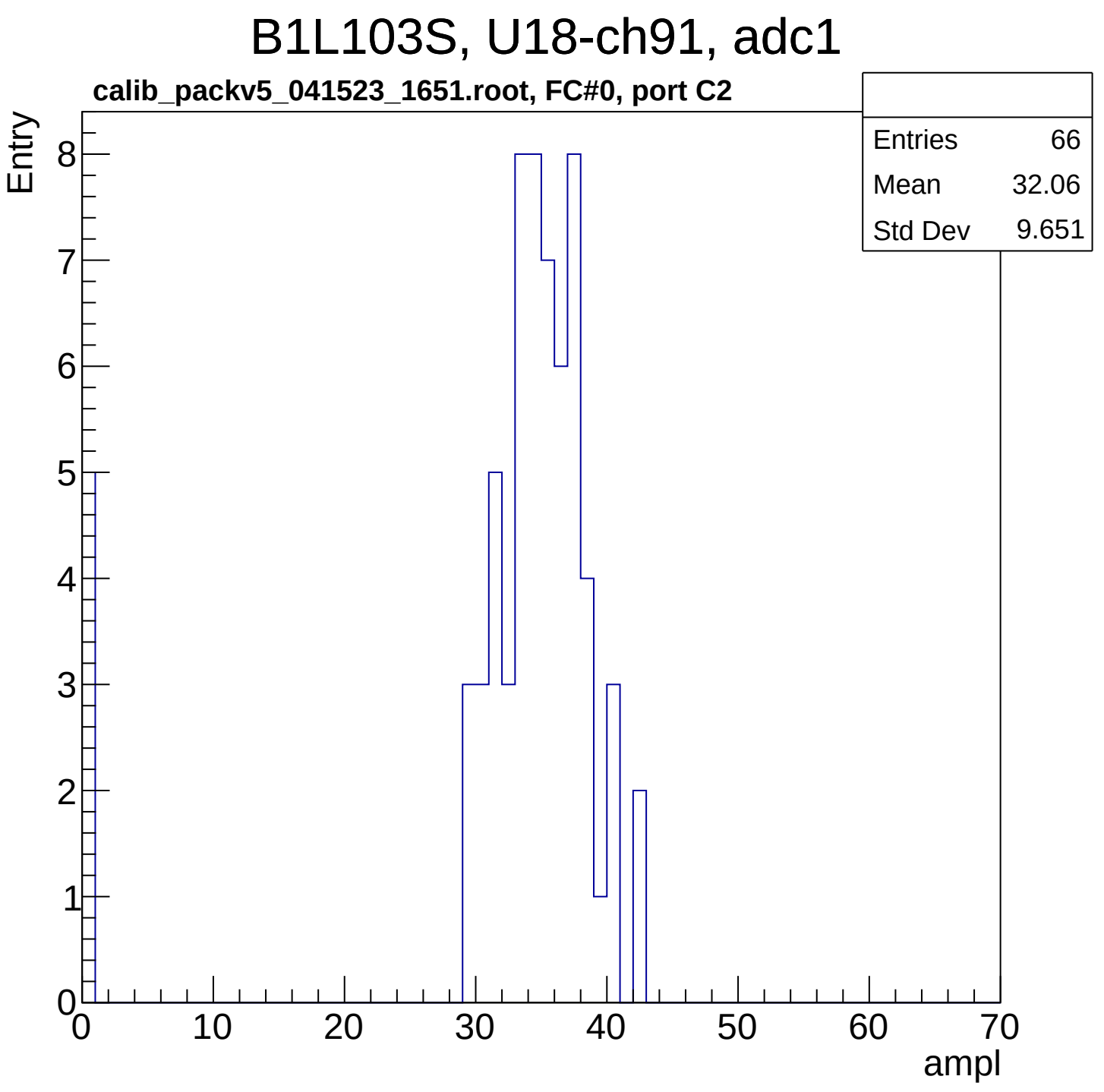
B1L103S, U18-ch91, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 32.06
Std Dev 9.651
Entry
ampl
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4
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7
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0
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20
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40
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60
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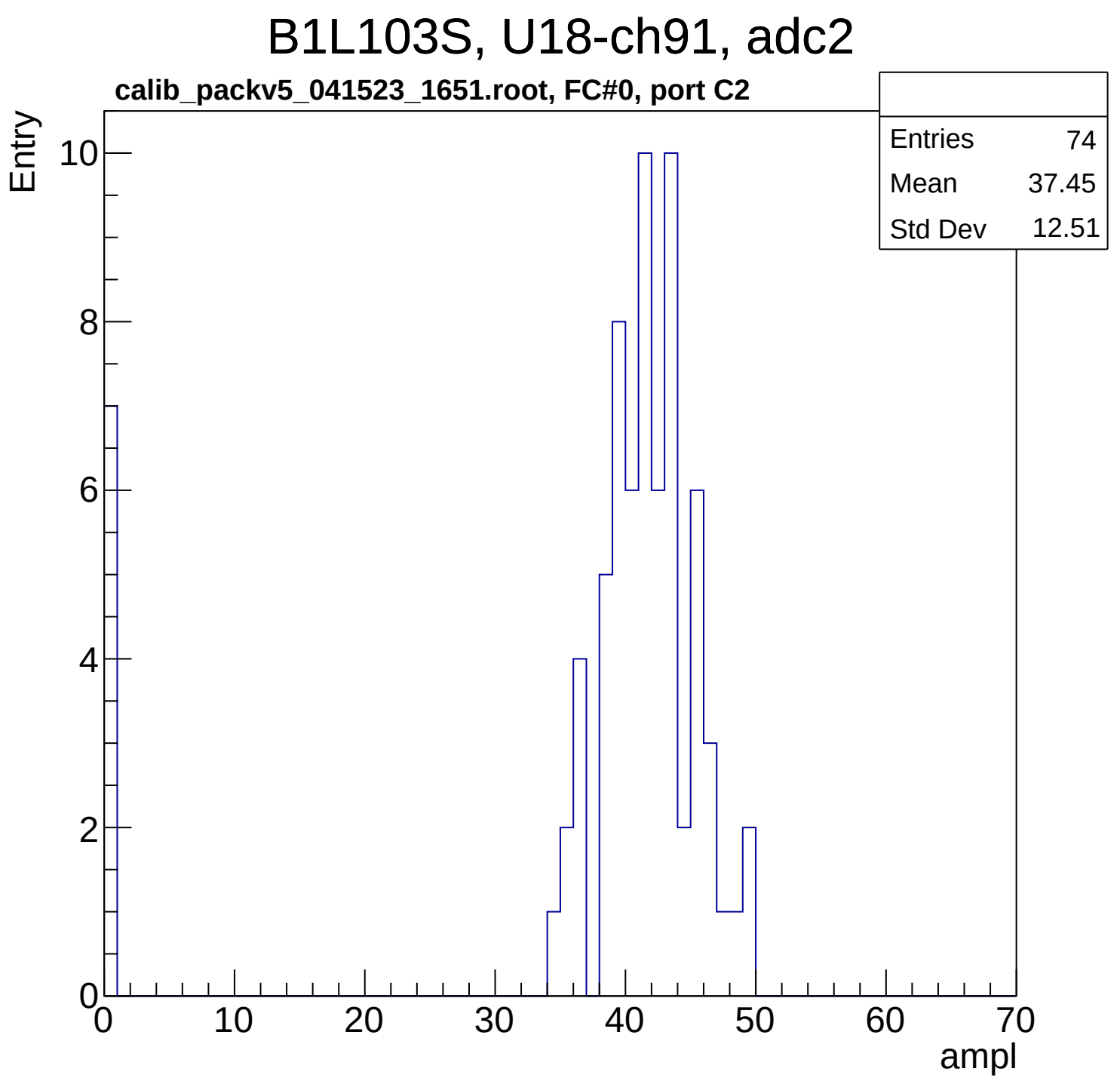
B1L103S, U18-ch91, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 37.45
Std Dev 12.51
Entry
ampl
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20
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40
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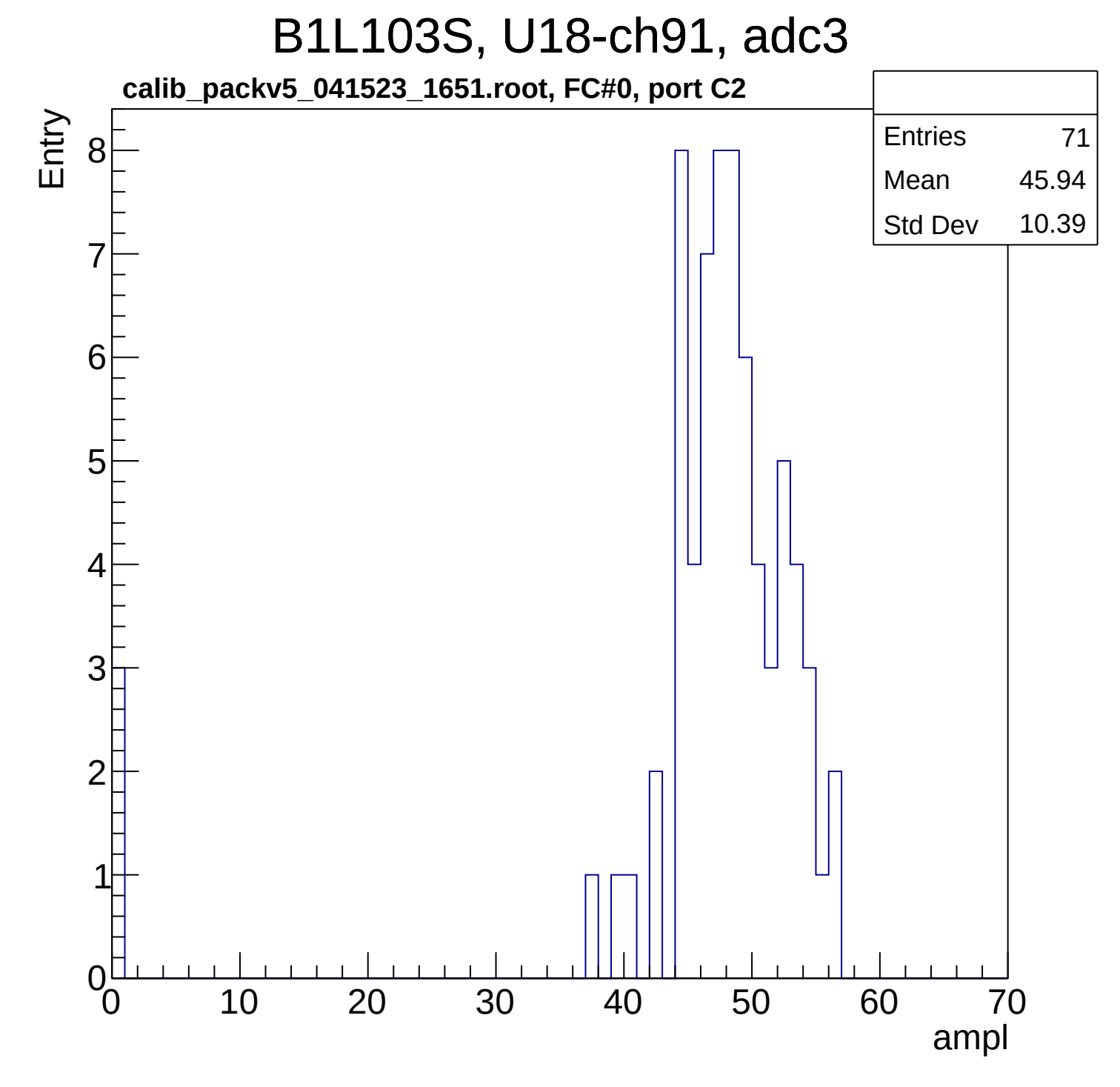
B1L103S, U18-ch91, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 45.94
Std Dev 10.39
Entry
ampl
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2
3
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5
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10
20
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60
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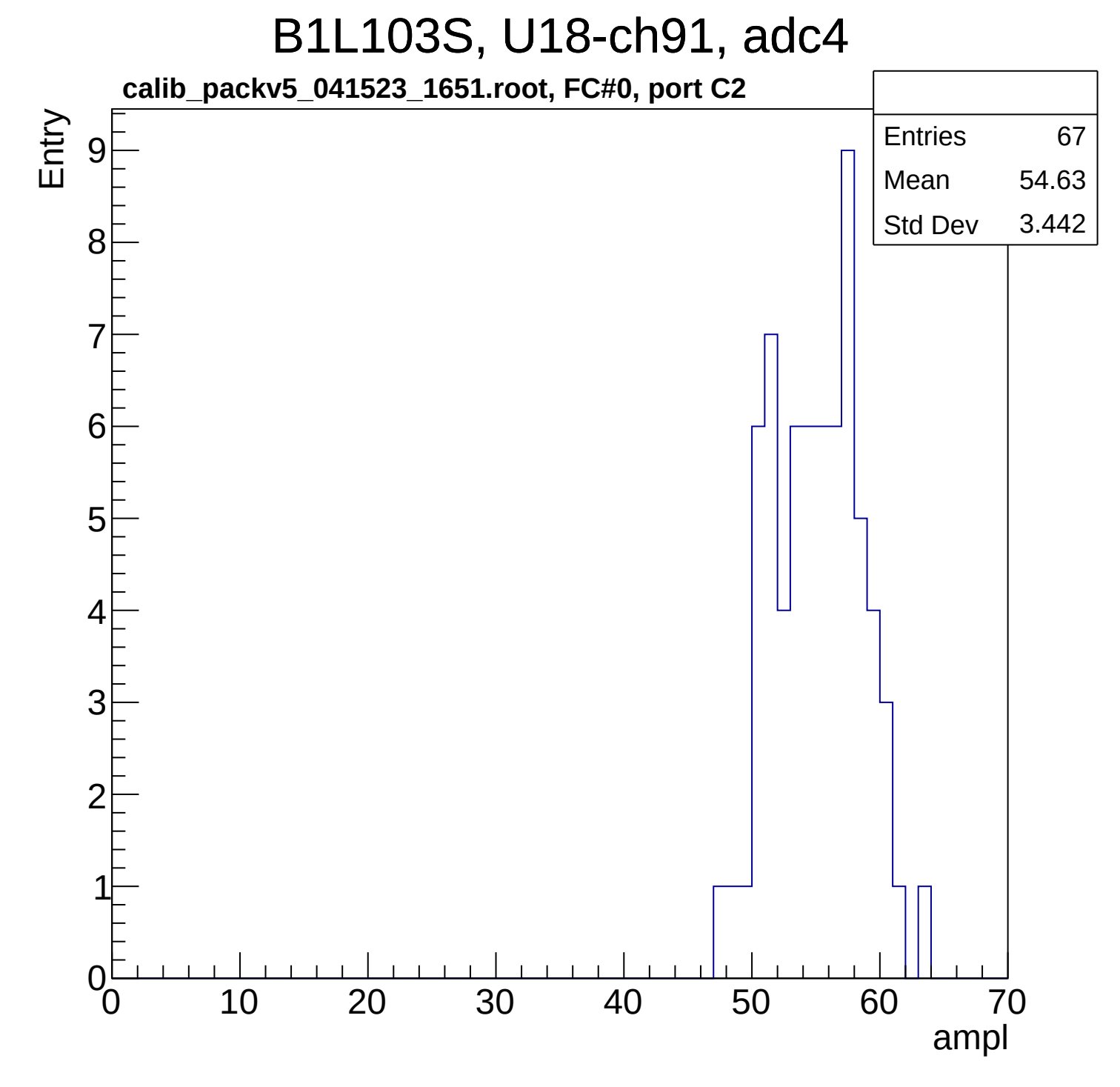
B1L103S, U18-ch91, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 54.63
Std Dev 3.442
Entry
ampl
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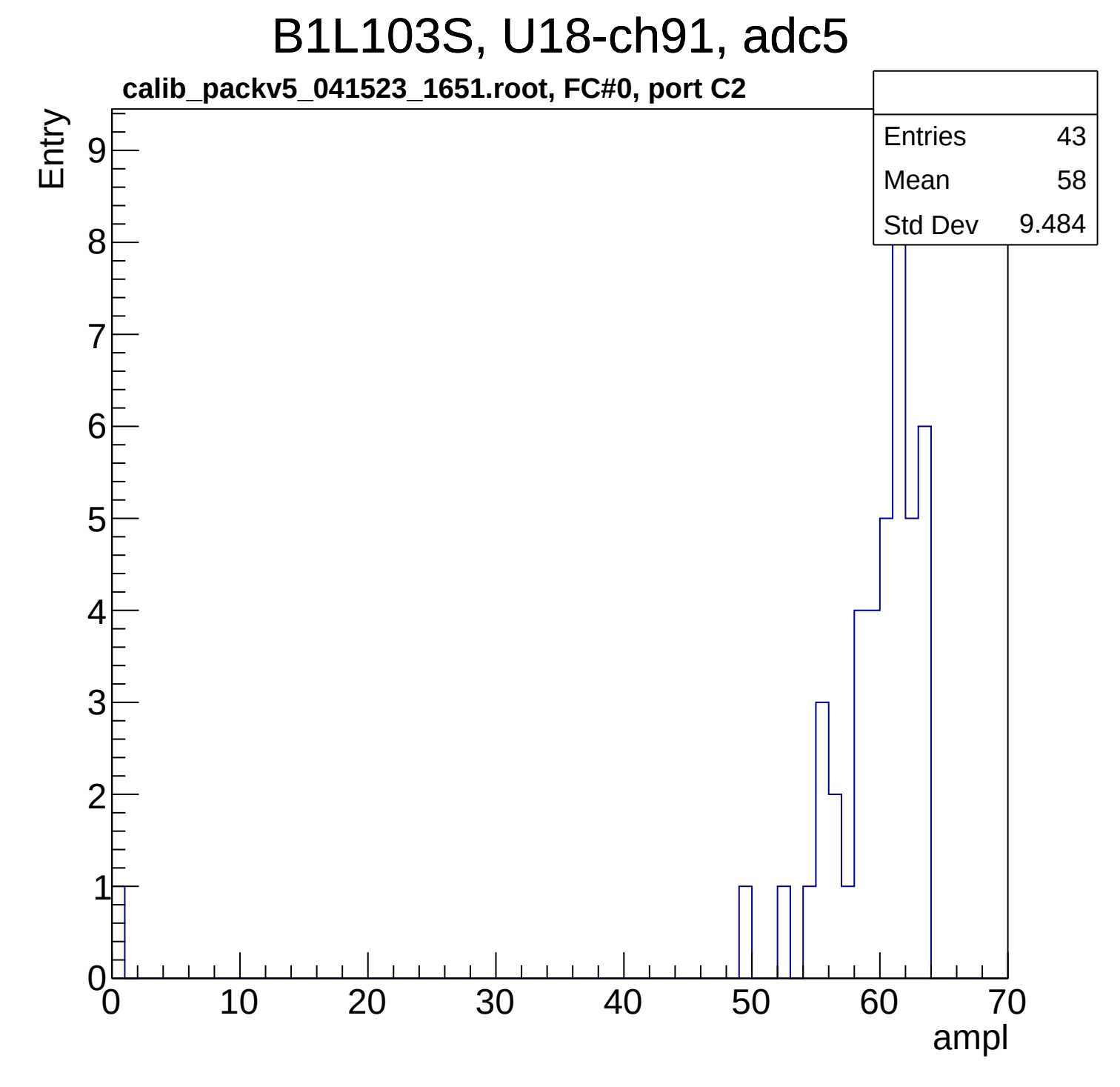
B1L103S, U18-ch91, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 43
Mean 58
Std Dev 9.484
Entry
ampl
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2
3
4
5
6
7
8
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0
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20
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60
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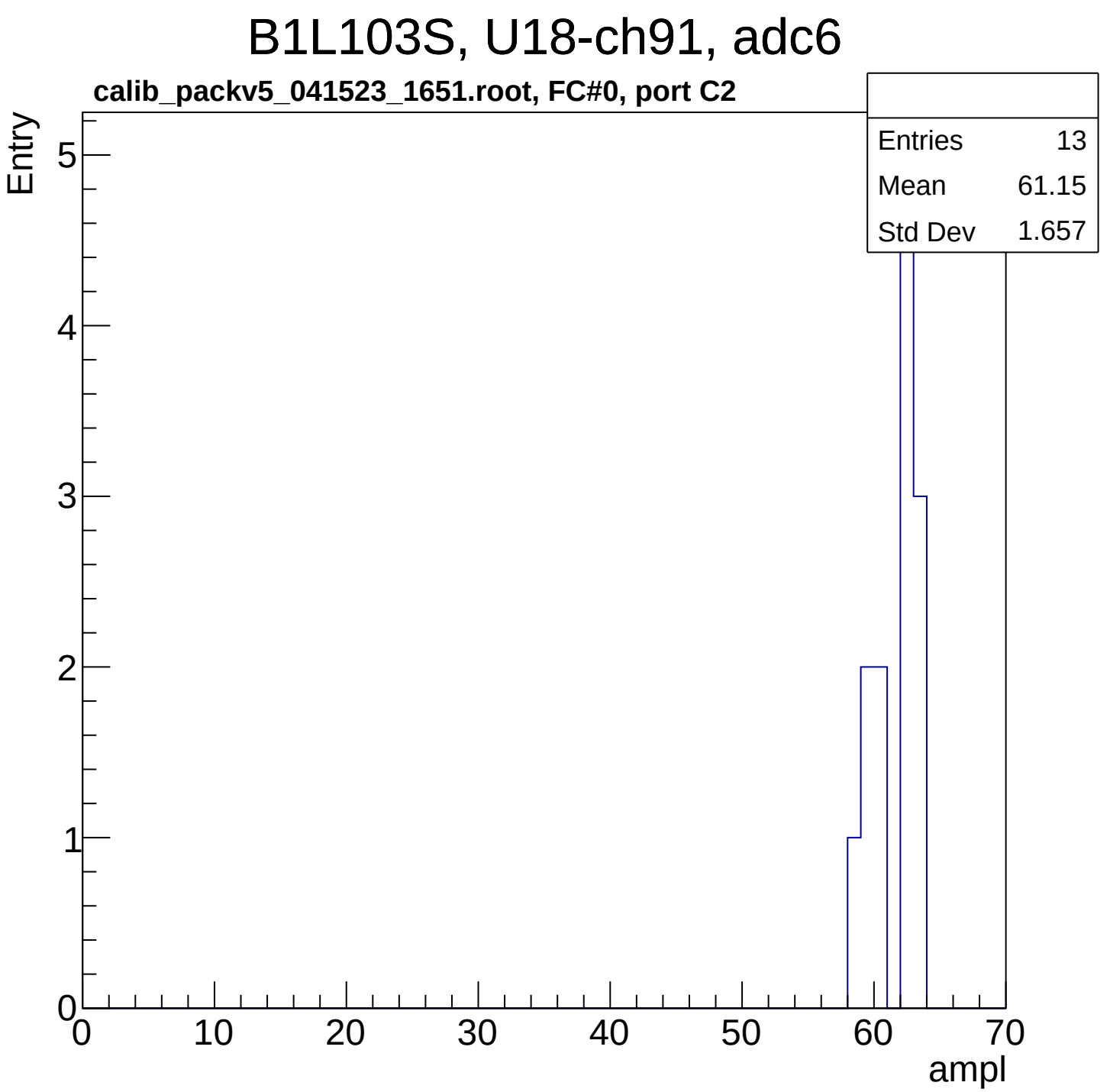
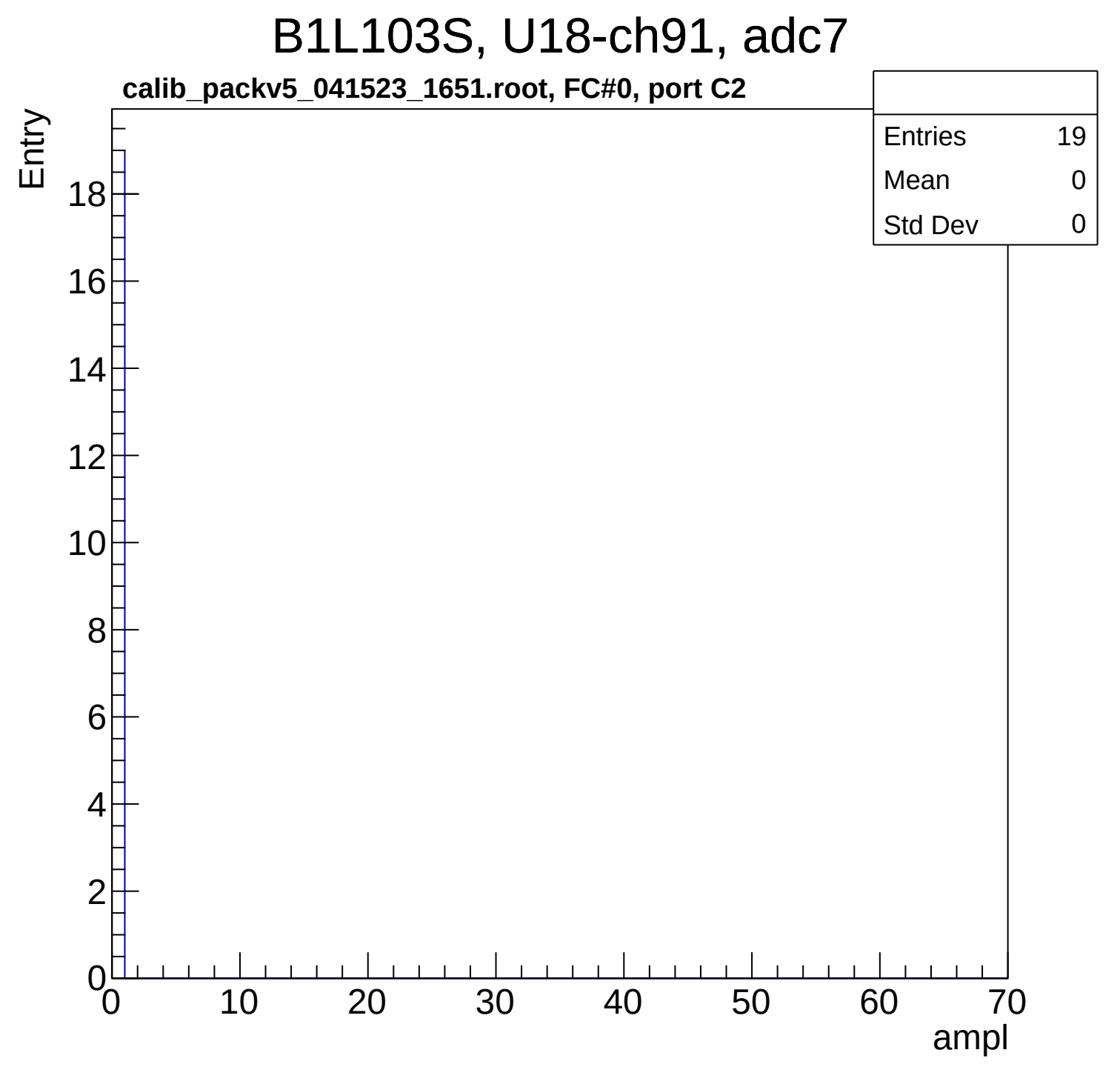

B1L103S, U18-ch91, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 13
Mean 61.15
Std Dev 1.657
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch91, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
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6
8
10
12
14
16
18
0
10
20
30
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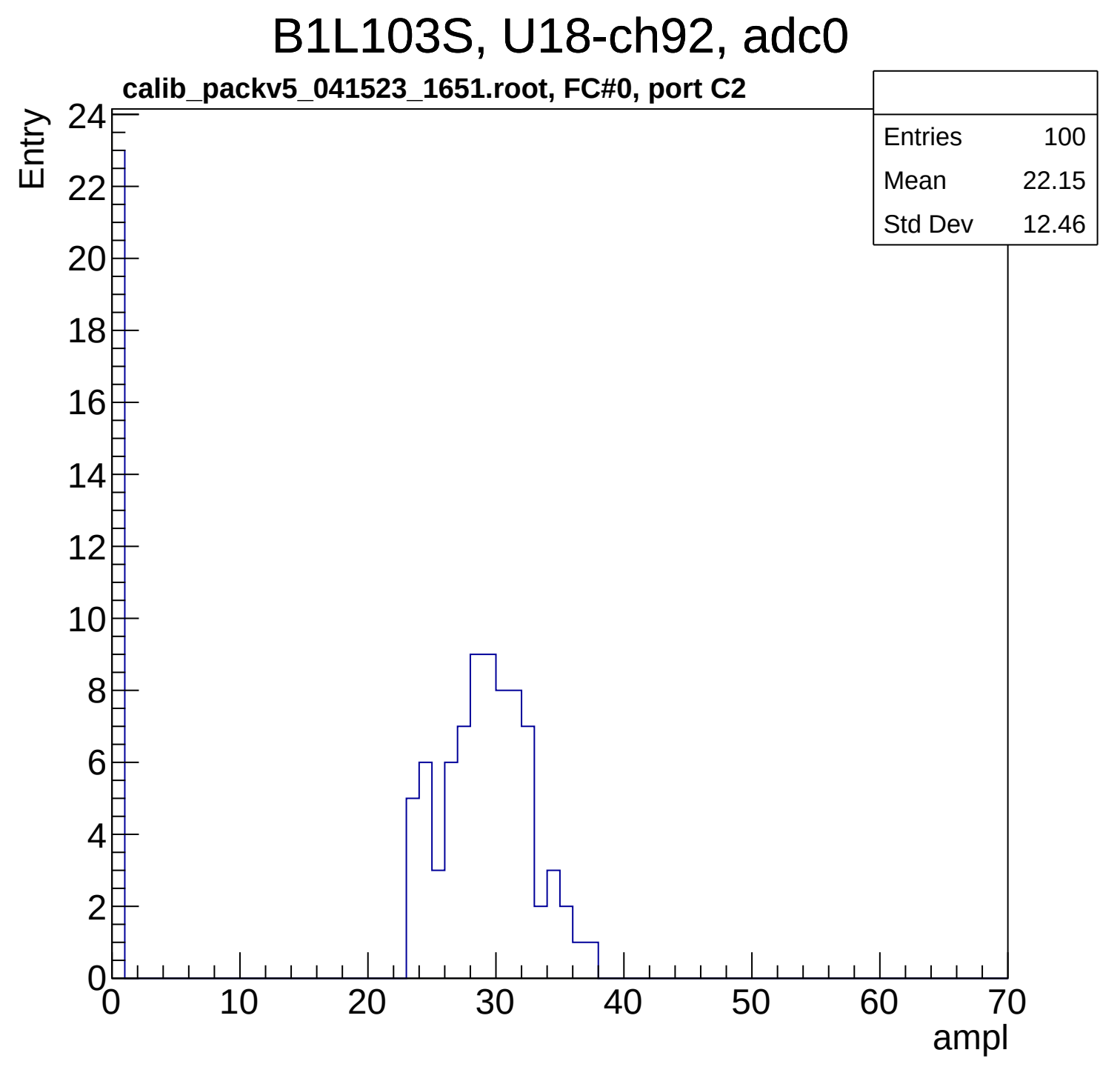
50
60
70
ampl


B1L103S, U18-ch92, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 100
Mean 22.15
Std Dev 12.46
Entry
ampl
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10
12
14
16
18
20
22
24
0
10
20
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40
50
60
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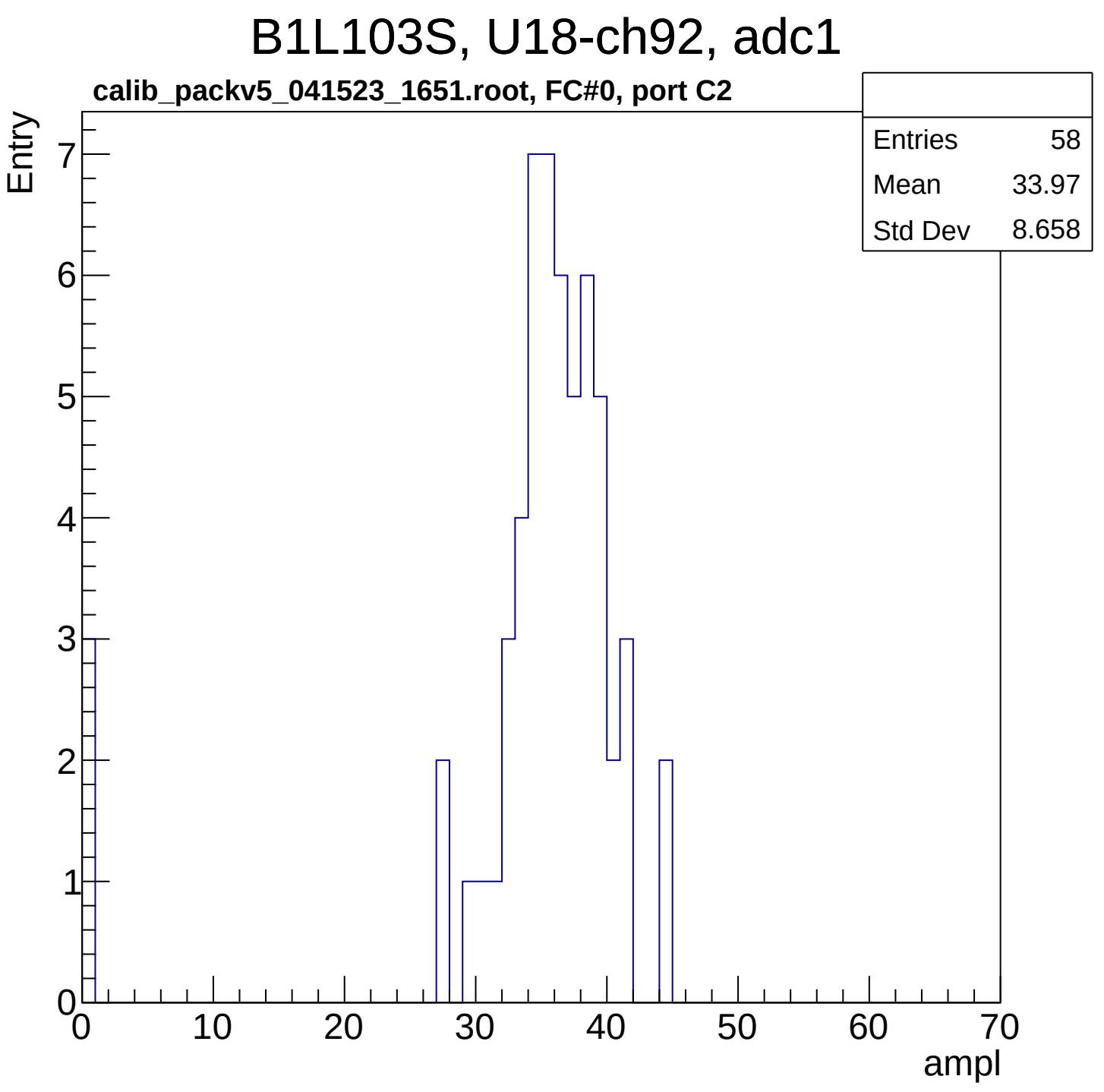
B1L103S, U18-ch92, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 33.97
Std Dev 8.658
Entry
ampl
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4
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6
7
0
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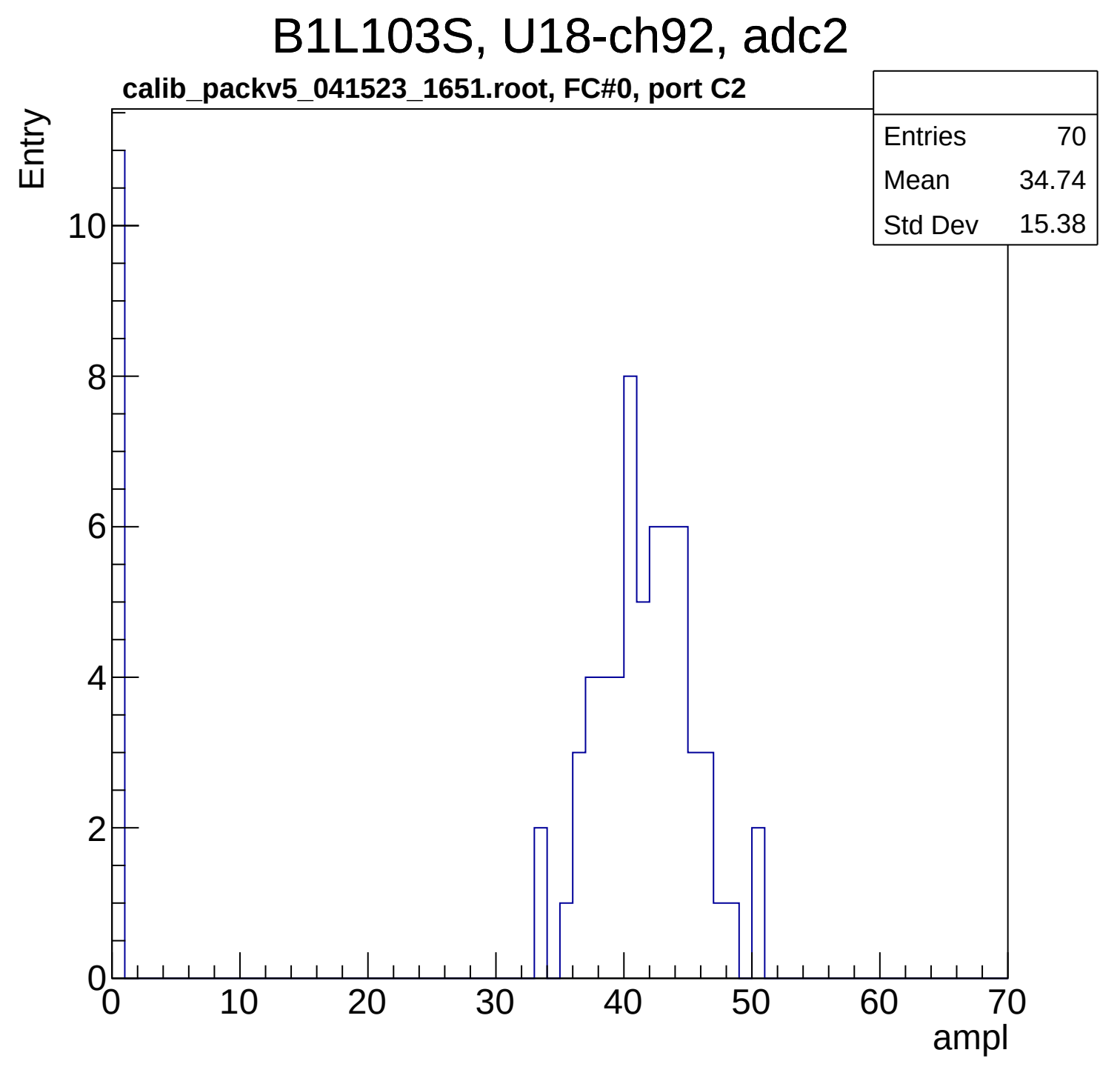
20
30
40
50
60
70


B1L103S, U18-ch92, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 34.74
Std Dev 15.38
Entry
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6
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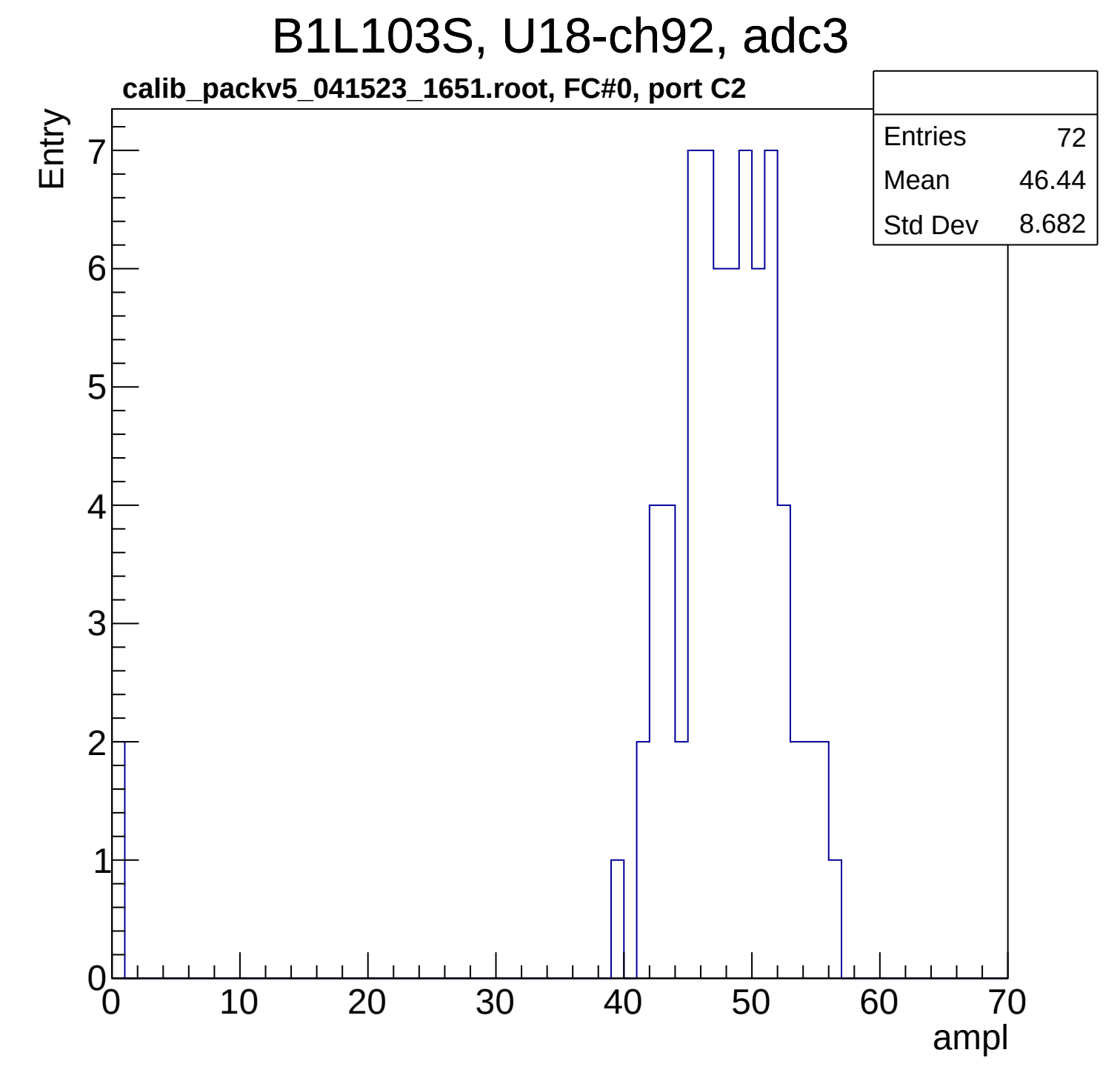
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch92, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 46.44
Std Dev 8.682
Entry
ampl
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3
4
5
6
7
0
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20
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40
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60
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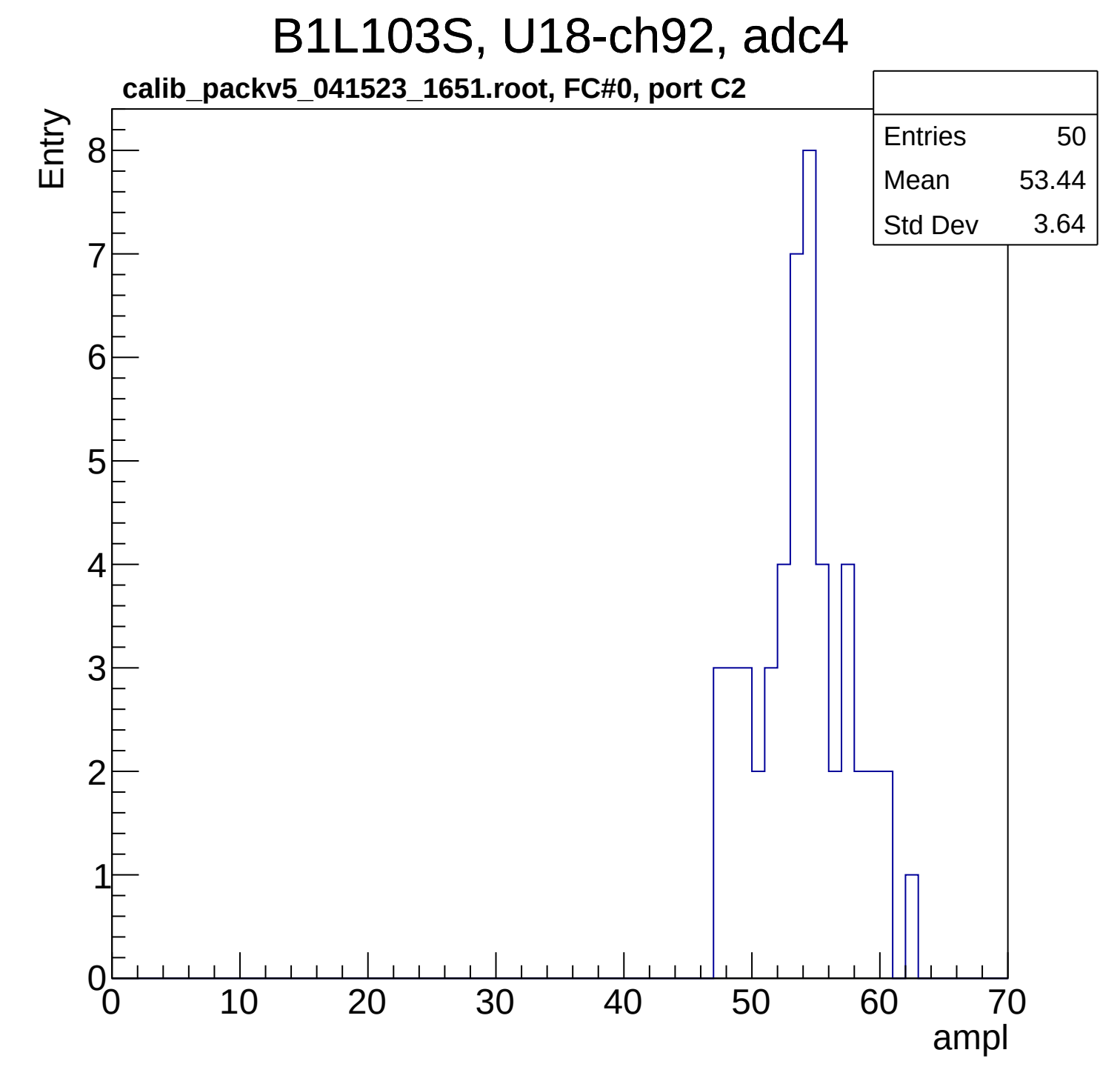
B1L103S, U18-ch92, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 53.44
Std Dev 3.64
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
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40
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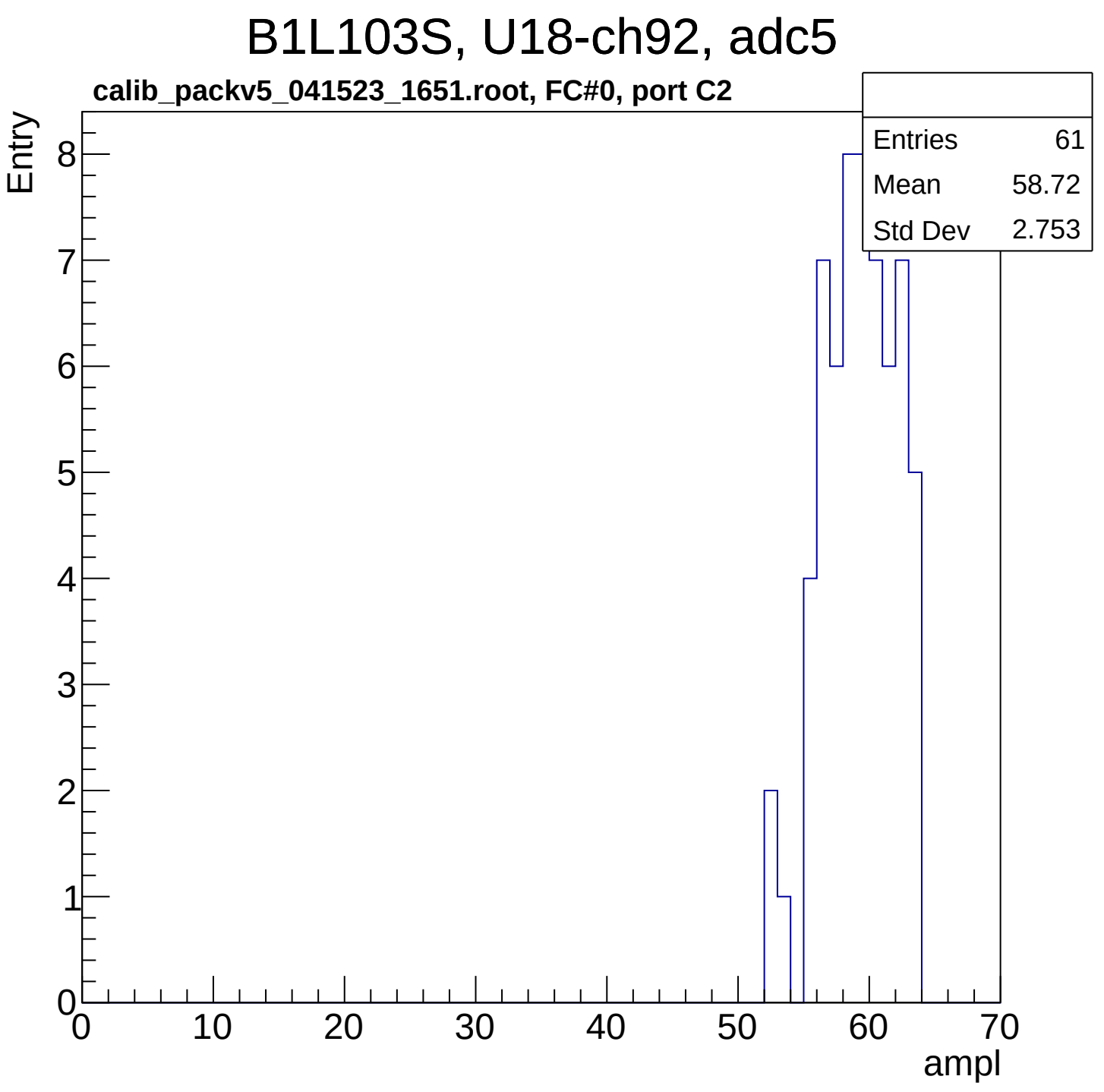
60
70


B1L103S, U18-ch92, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 58.72
Std Dev 2.753
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
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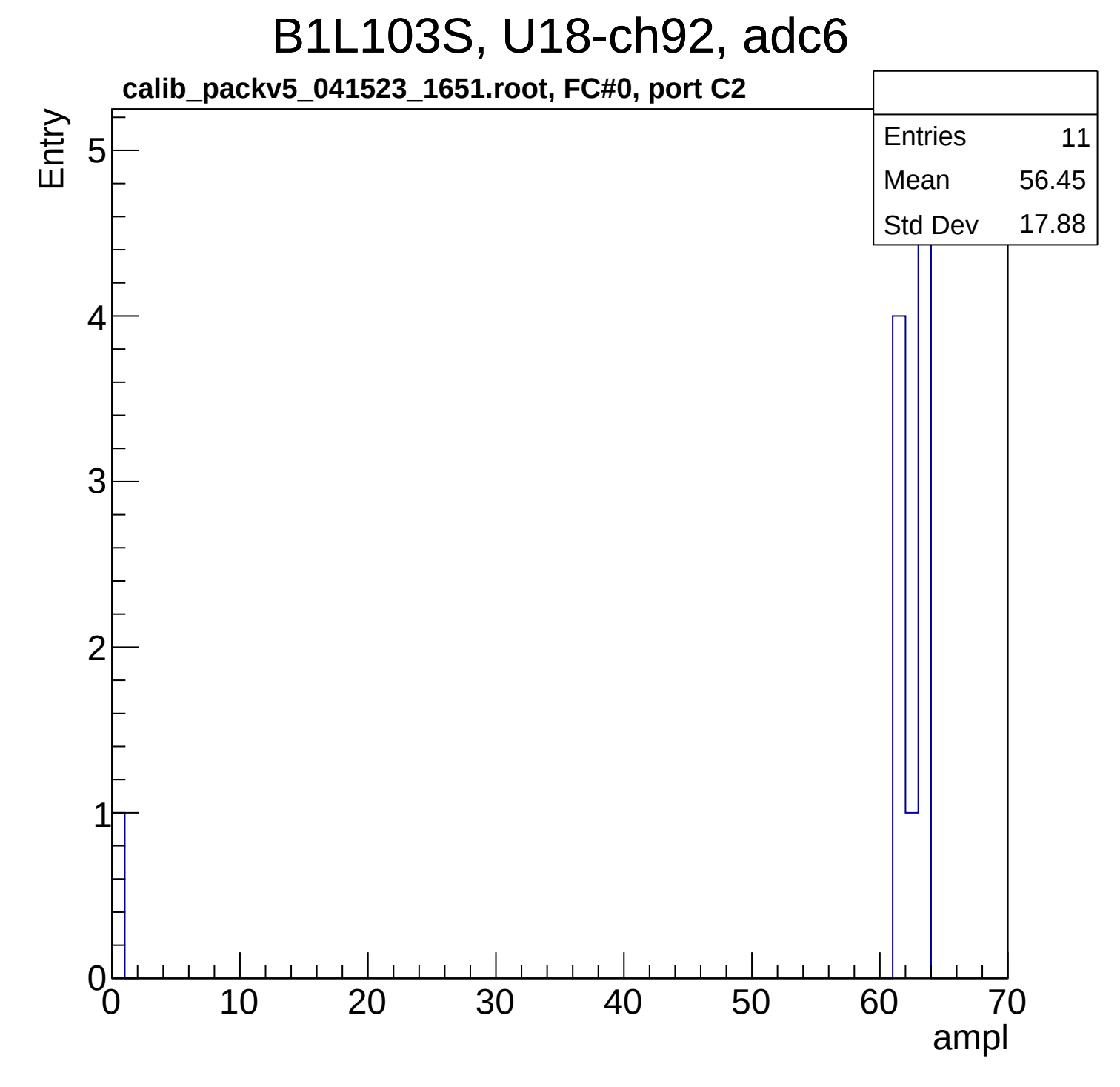
40
50
60
70


B1L103S, U18-ch92, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 56.45
Std Dev 17.88
Entry
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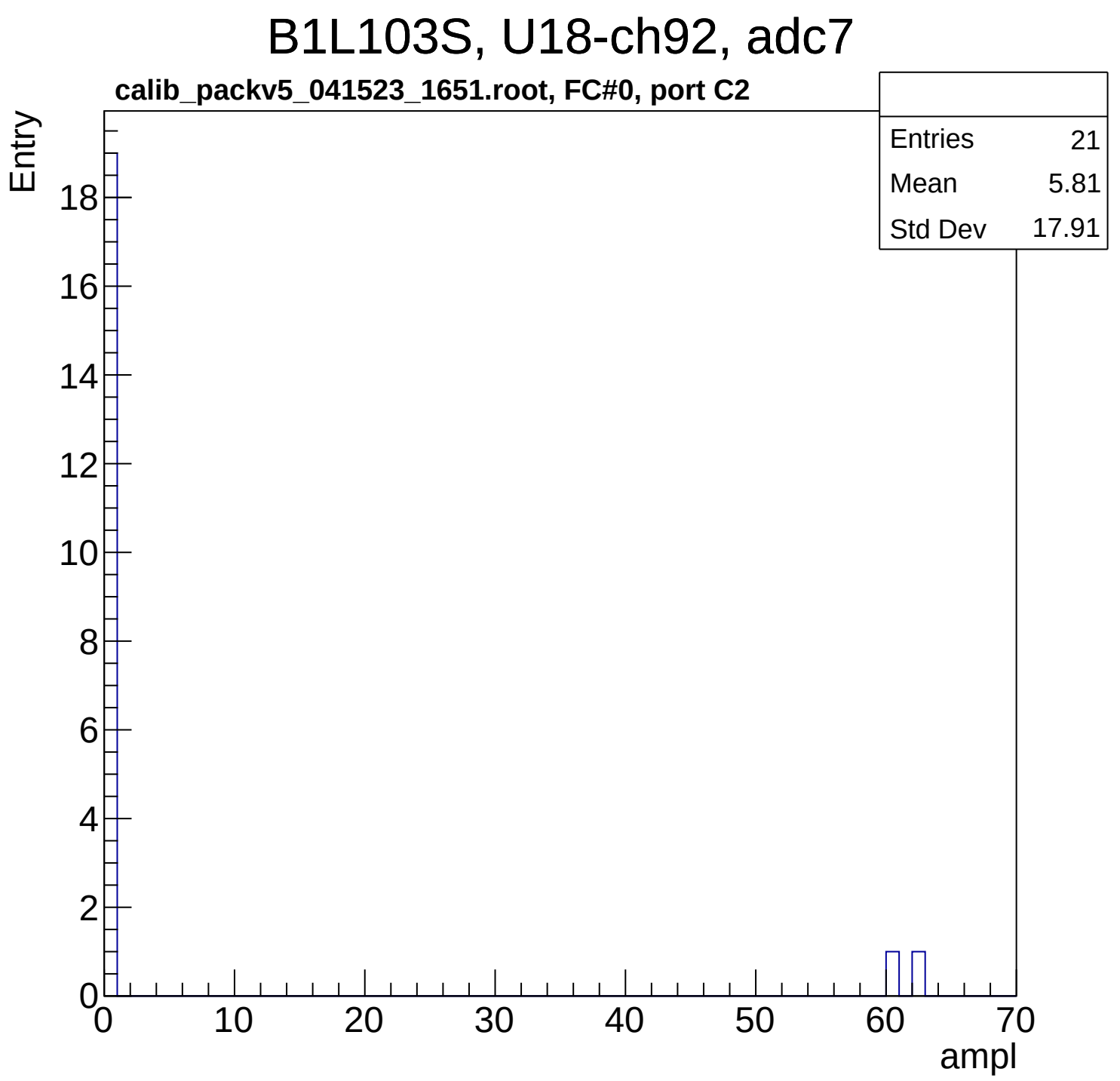
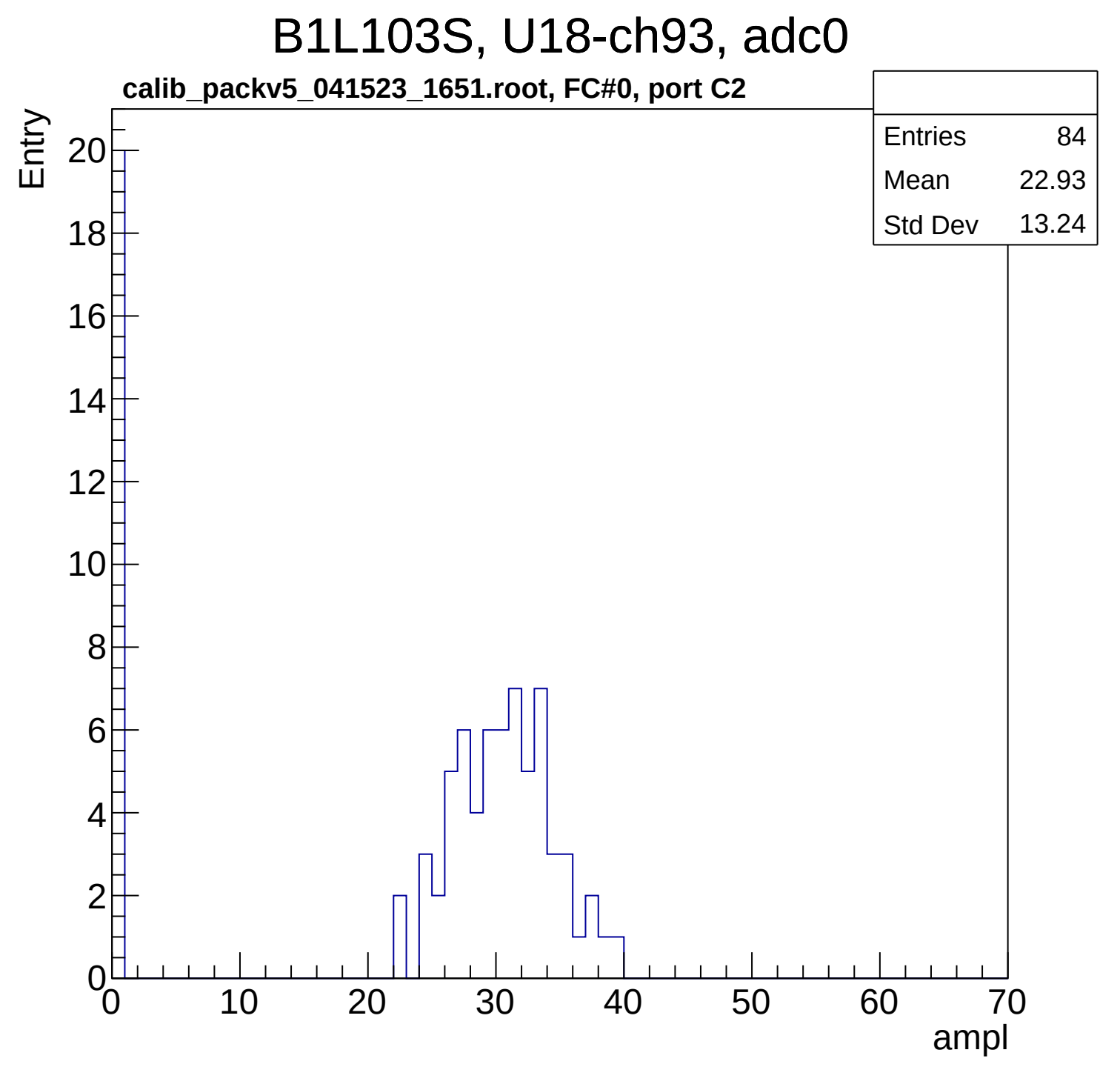
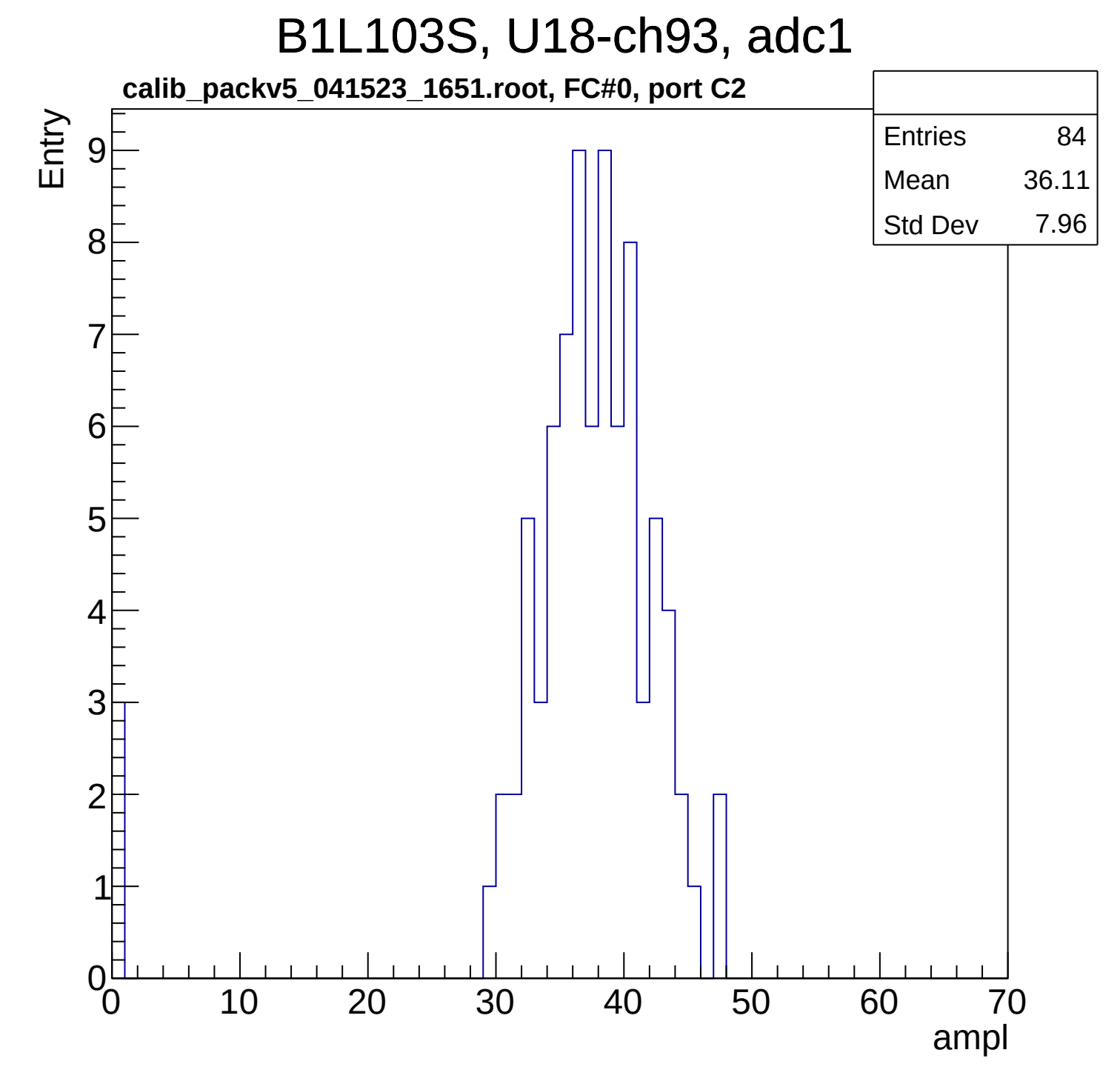
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch92, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 5.81
Std Dev 17.91
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch93, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 22.93
Std Dev 13.24
Entry
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch93, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 36.11
Std Dev 7.96
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
50
60
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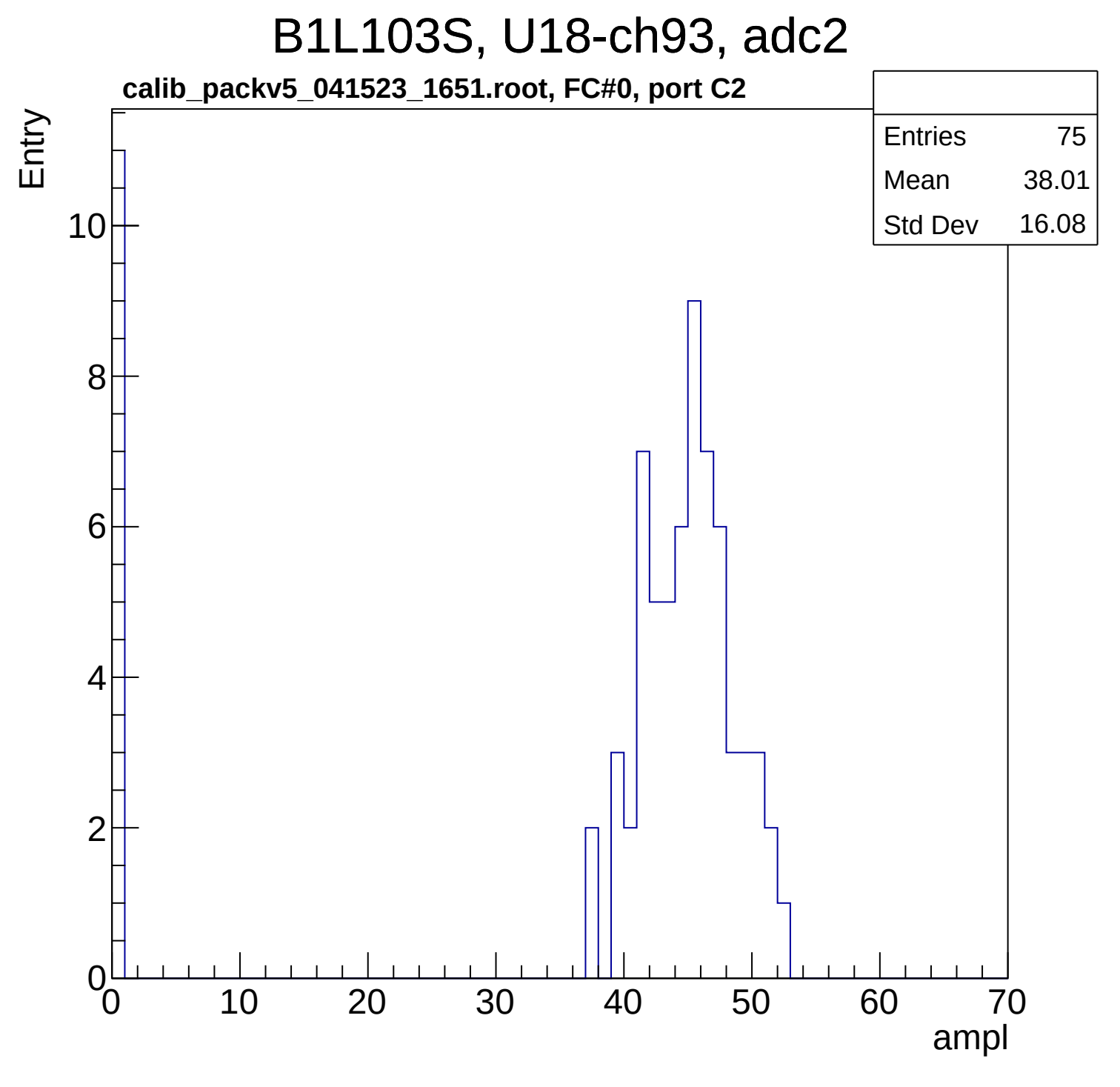
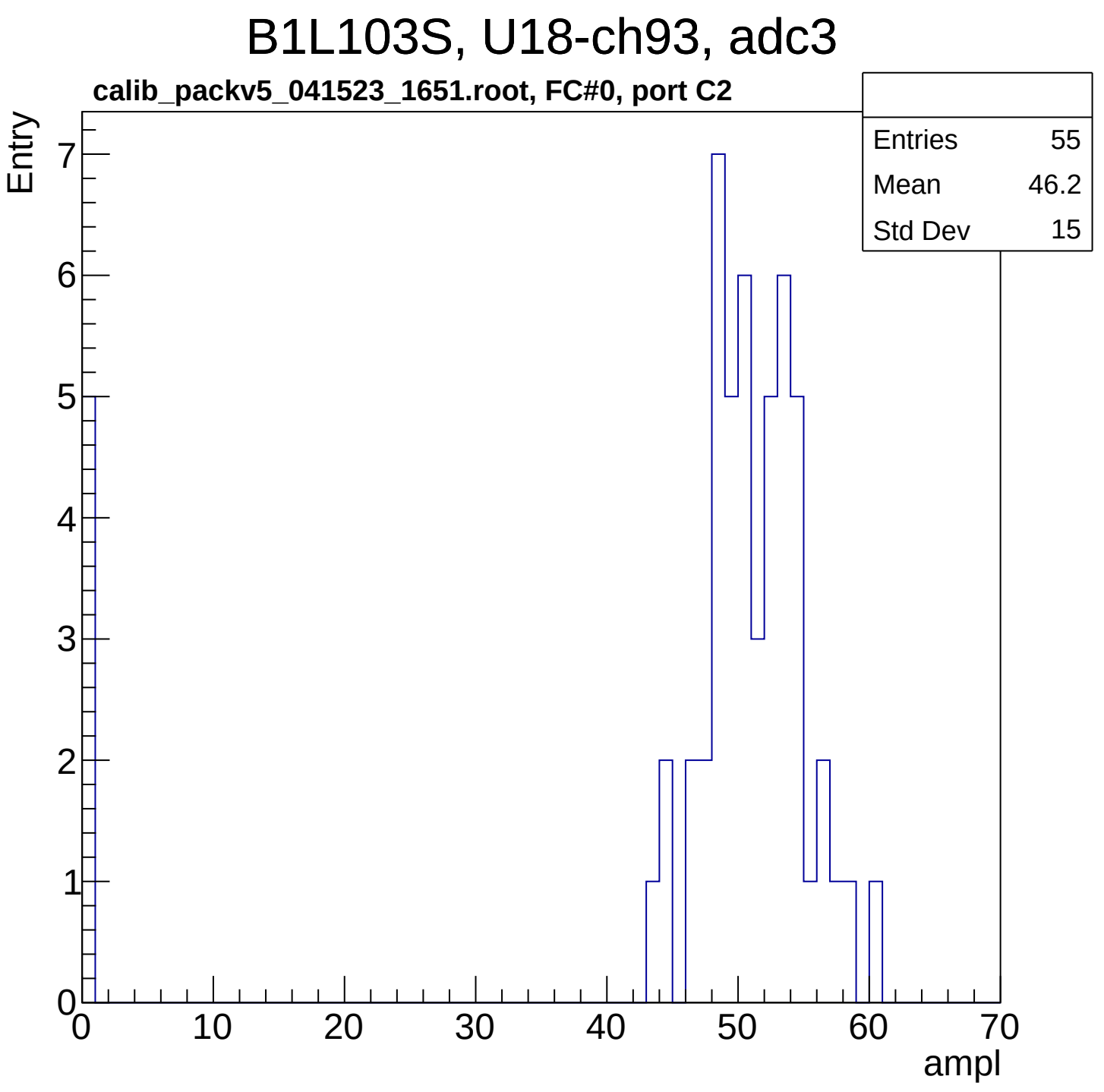

B1L103S, U18-ch93, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 38.01
Std Dev 16.08
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch93, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 46.2
Std Dev 15
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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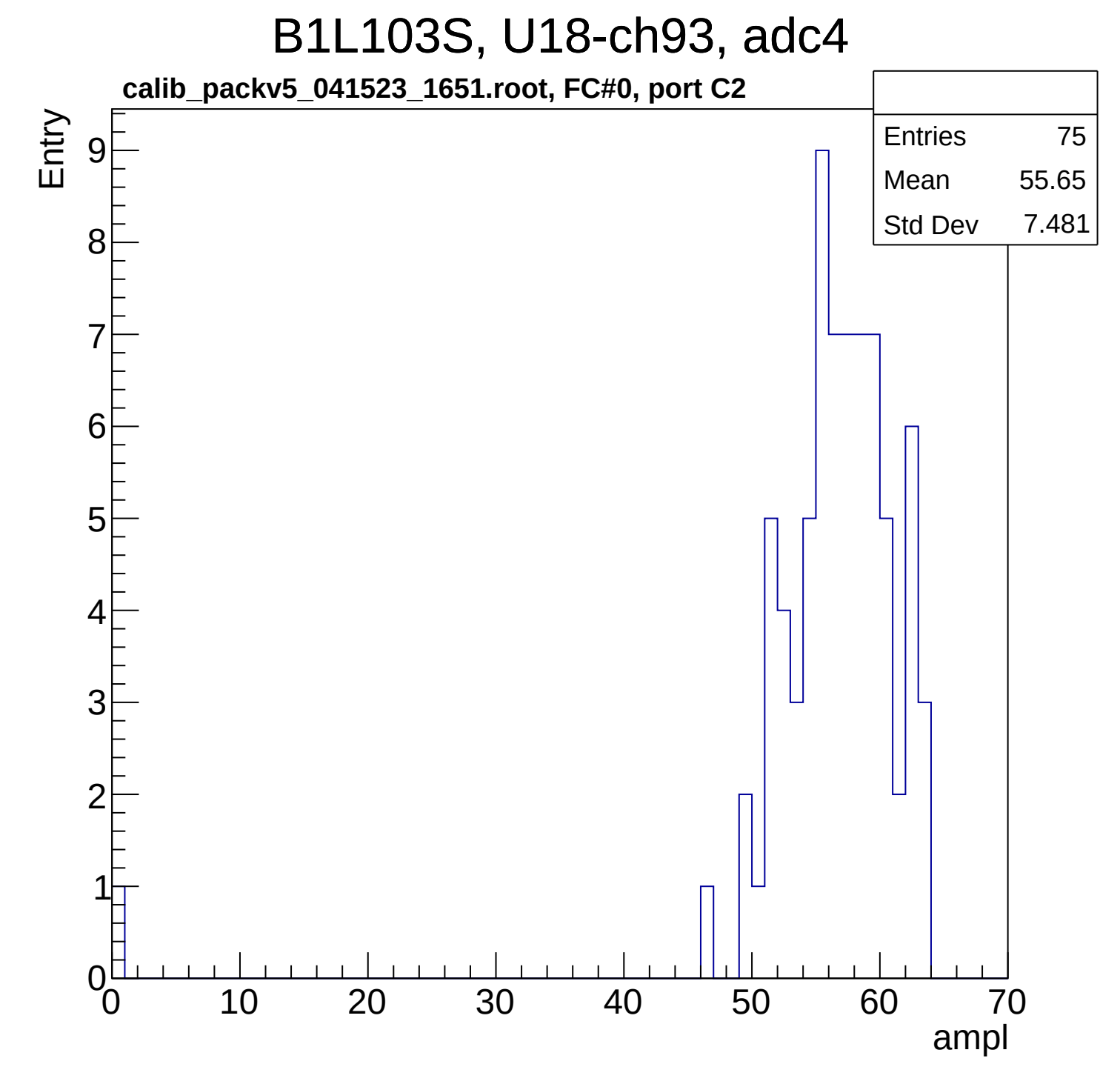
B1L103S, U18-ch93, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 55.65
Std Dev 7.481
Entry
ampl
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2
3
4
5
6
7
8
9
0
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40
50
60
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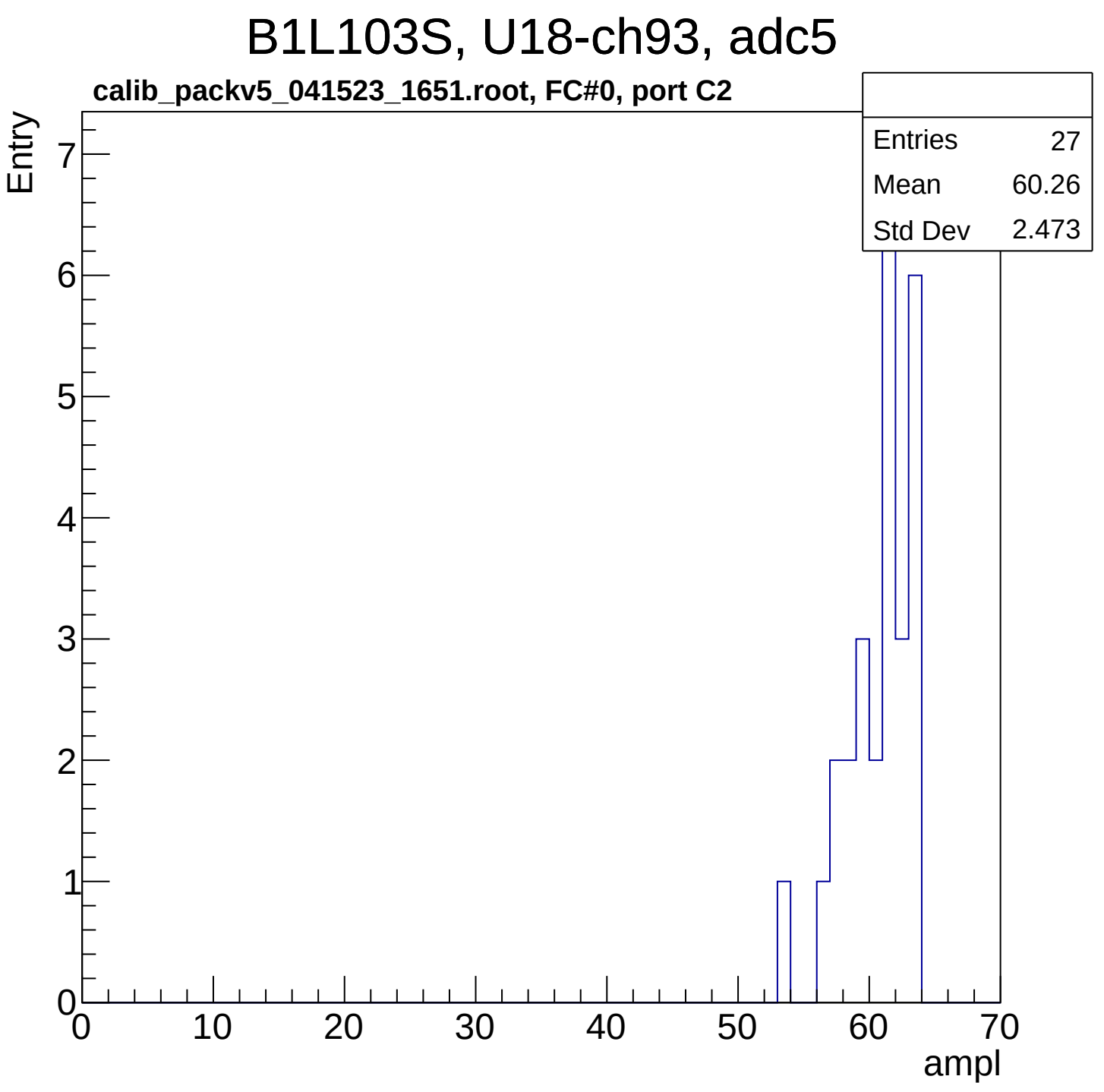
B1L103S, U18-ch93, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 27
Mean 60.26
Std Dev 2.473
Entry
ampl
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2
3
4
5
6
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0
10
20
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40
50
60
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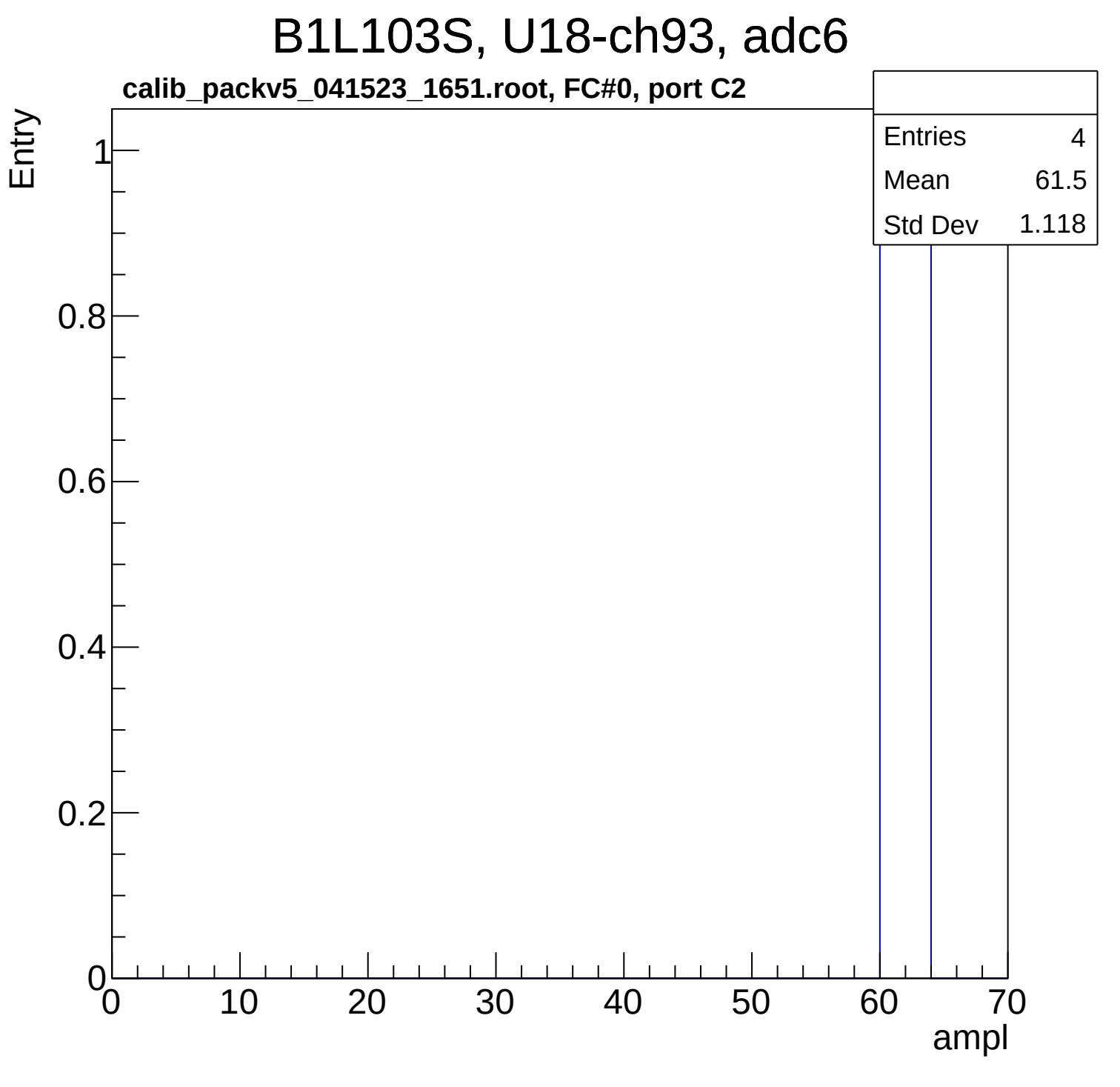
B1L103S, U18-ch93, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 4
Mean 61.5
Std Dev 1.118
Entry
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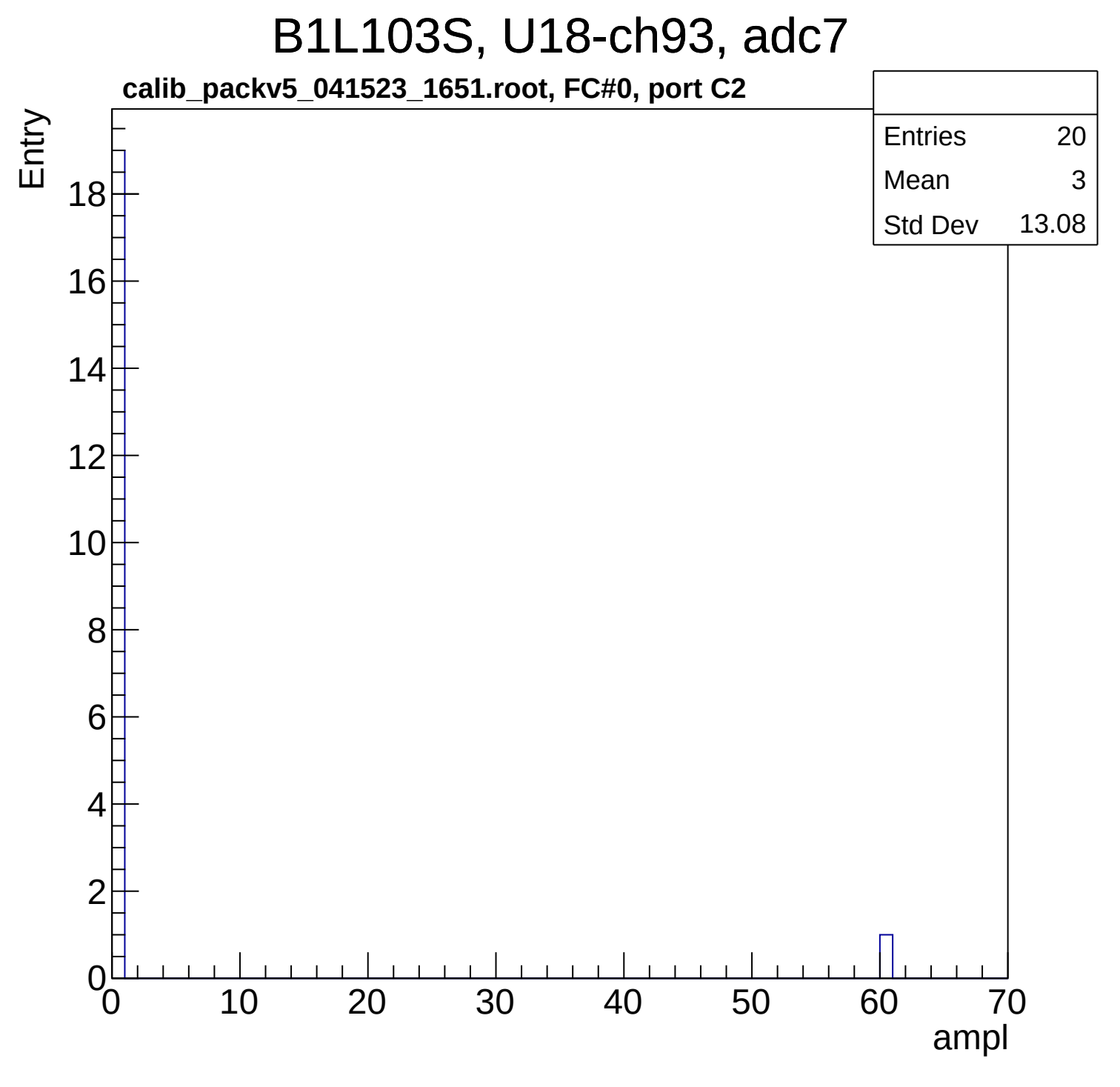
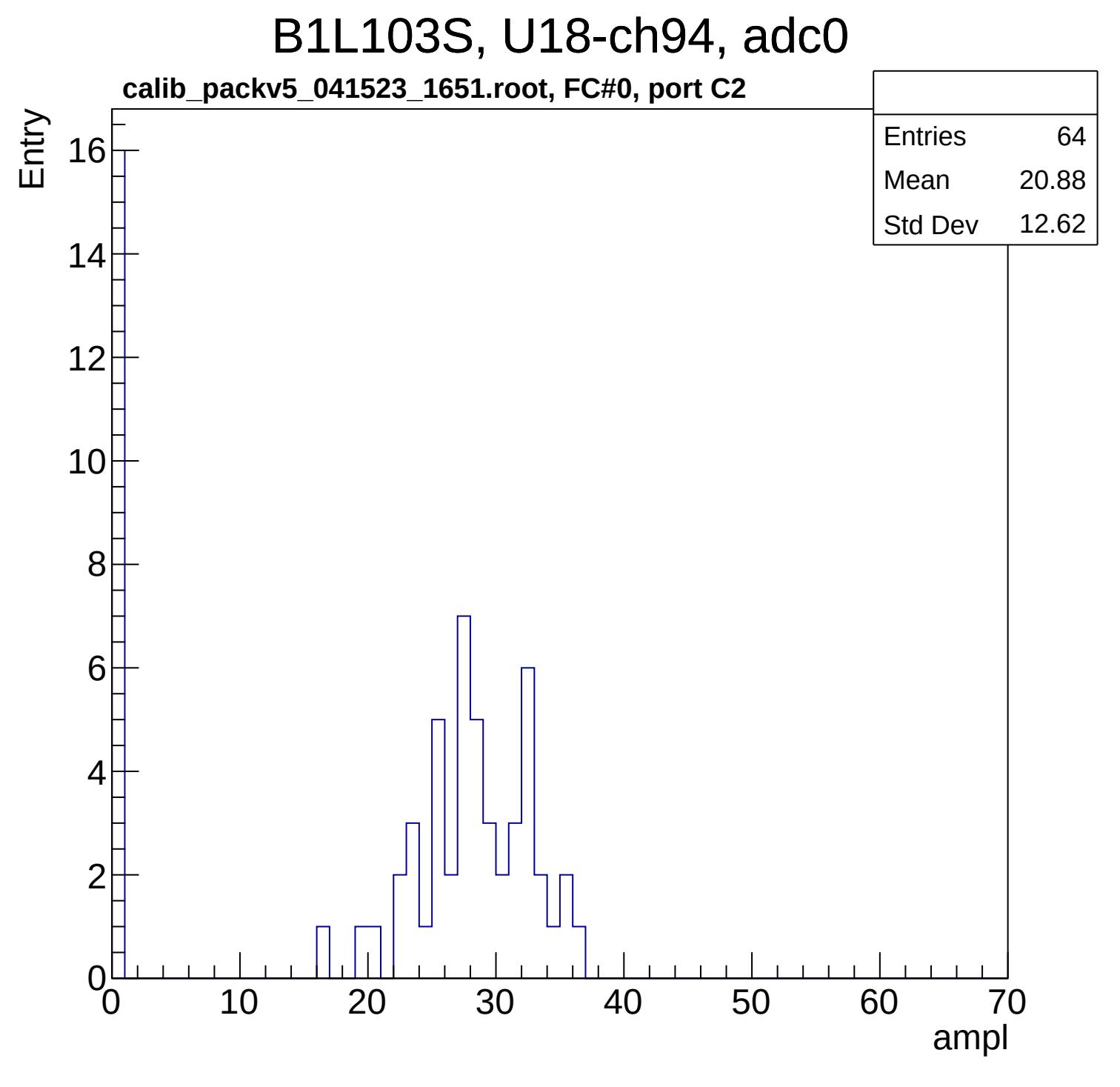
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch93, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3
Std Dev 13.08
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch94, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 20.88
Std Dev 12.62
Entry
ampl
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4
6
8
10
12
14
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0
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20
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40
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60
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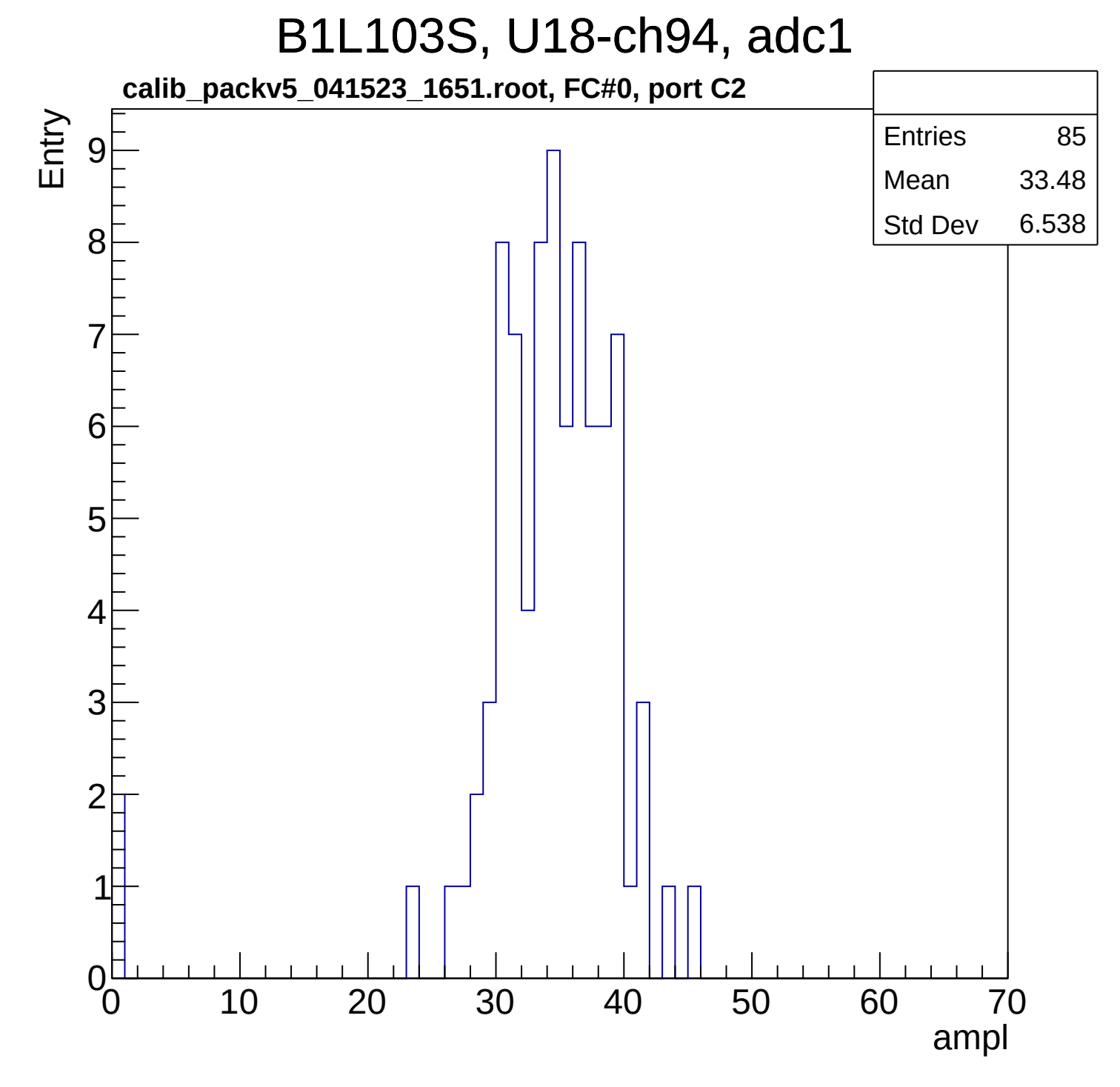
B1L103S, U18-ch94, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 33.48
Std Dev 6.538
Entry
ampl
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3
4
5
6
7
8
9
0
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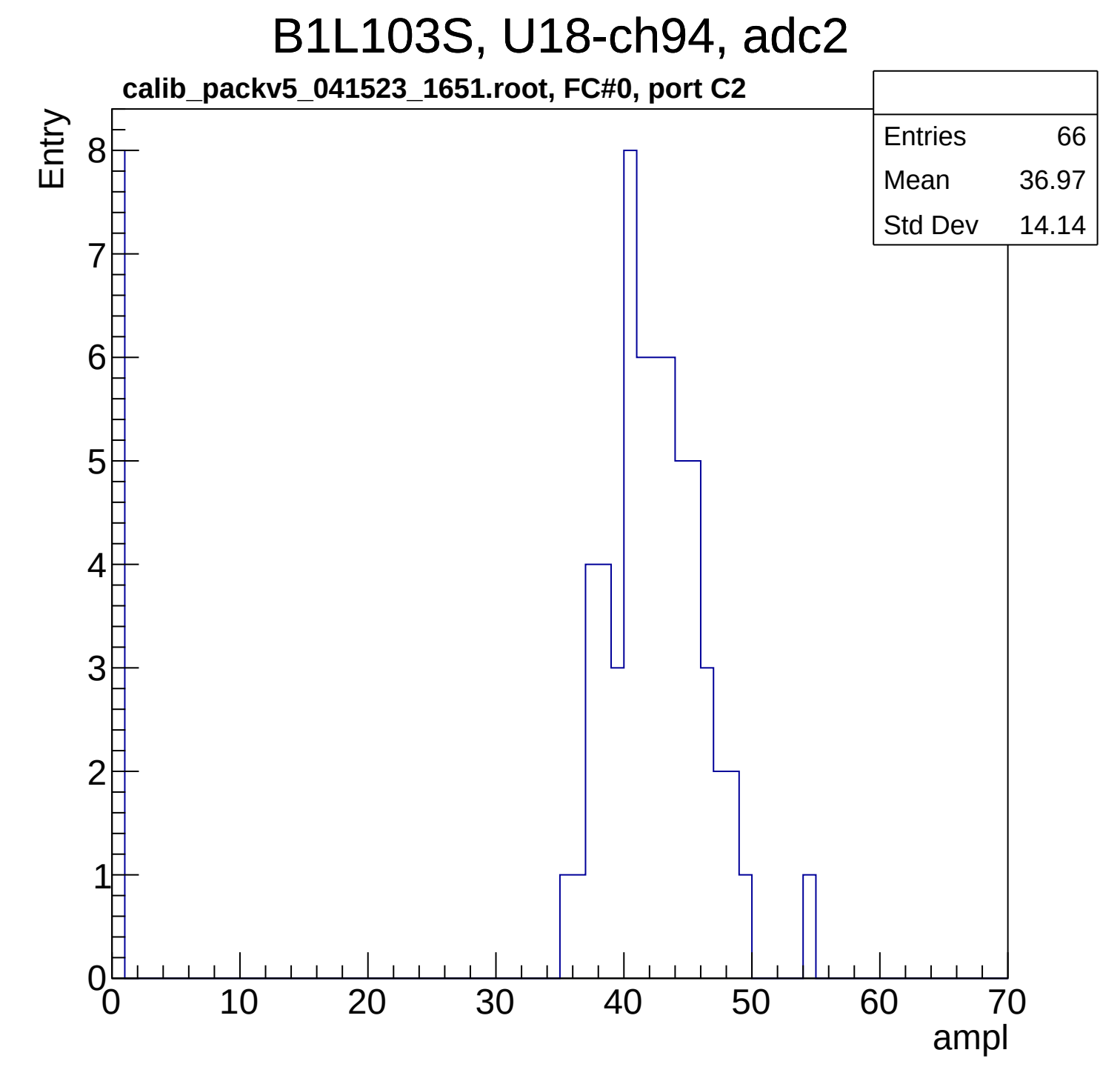
B1L103S, U18-ch94, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 36.97
Std Dev 14.14
Entry
ampl
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2
3
4
5
6
7
8
0
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20
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60
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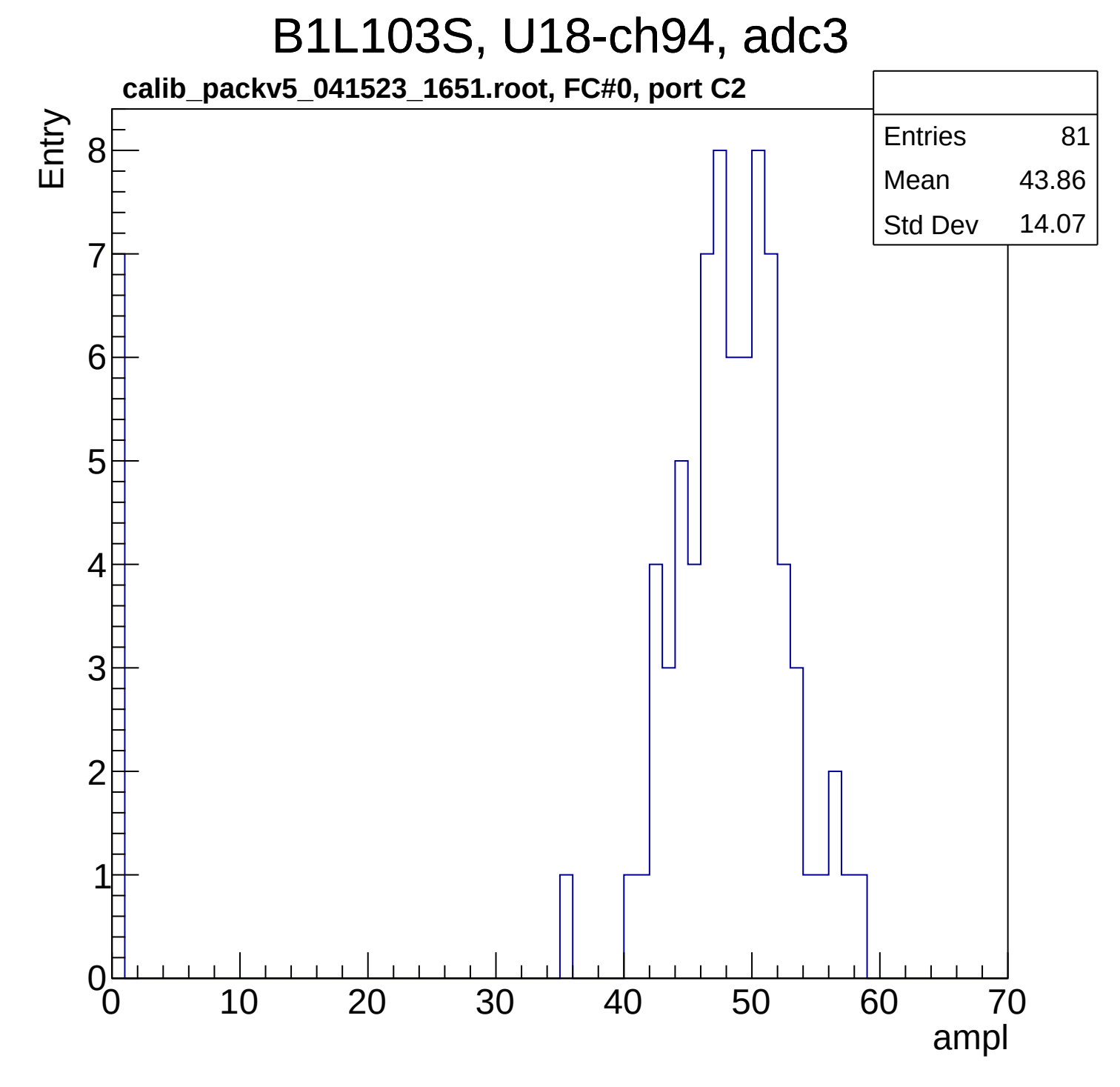
B1L103S, U18-ch94, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 43.86
Std Dev 14.07
Entry
ampl
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2
3
4
5
6
7
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0
10
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60
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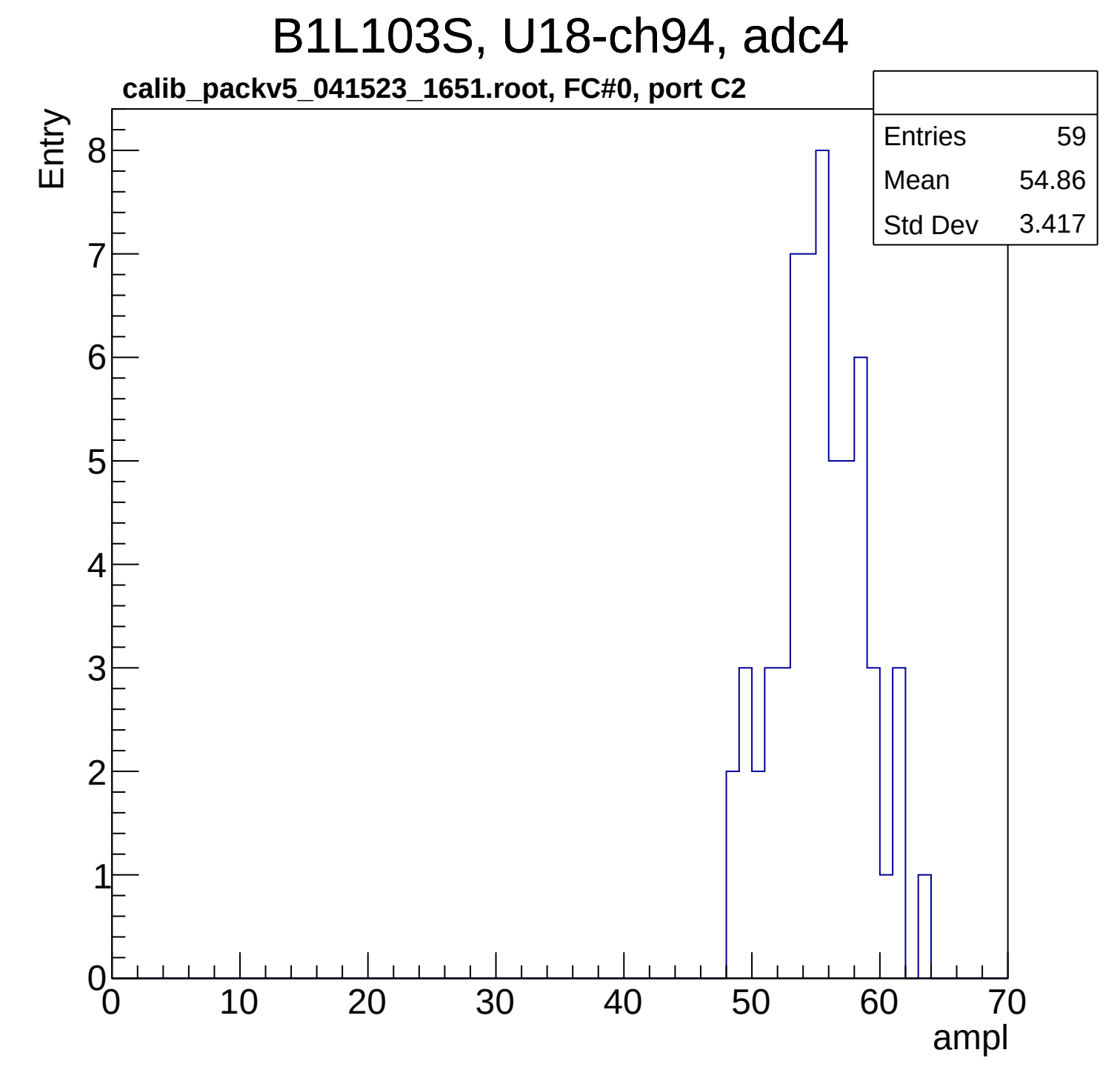
B1L103S, U18-ch94, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 54.86
Std Dev 3.417
Entry
ampl
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4
5
6
7
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0
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60
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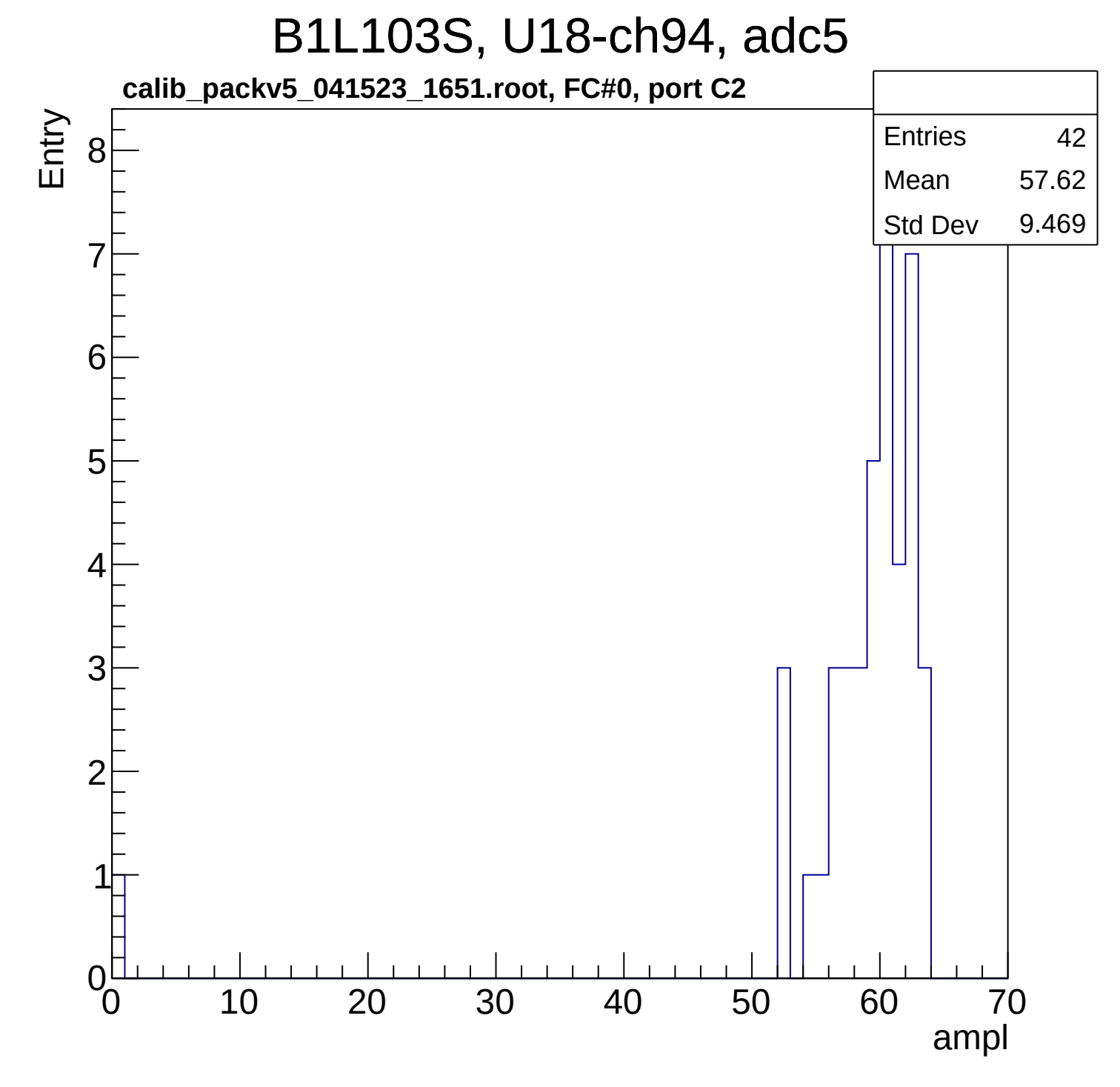
B1L103S, U18-ch94, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 42
Mean 57.62
Std Dev 9.469
Entry
ampl
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2
3
4
5
6
7
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0
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20
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60
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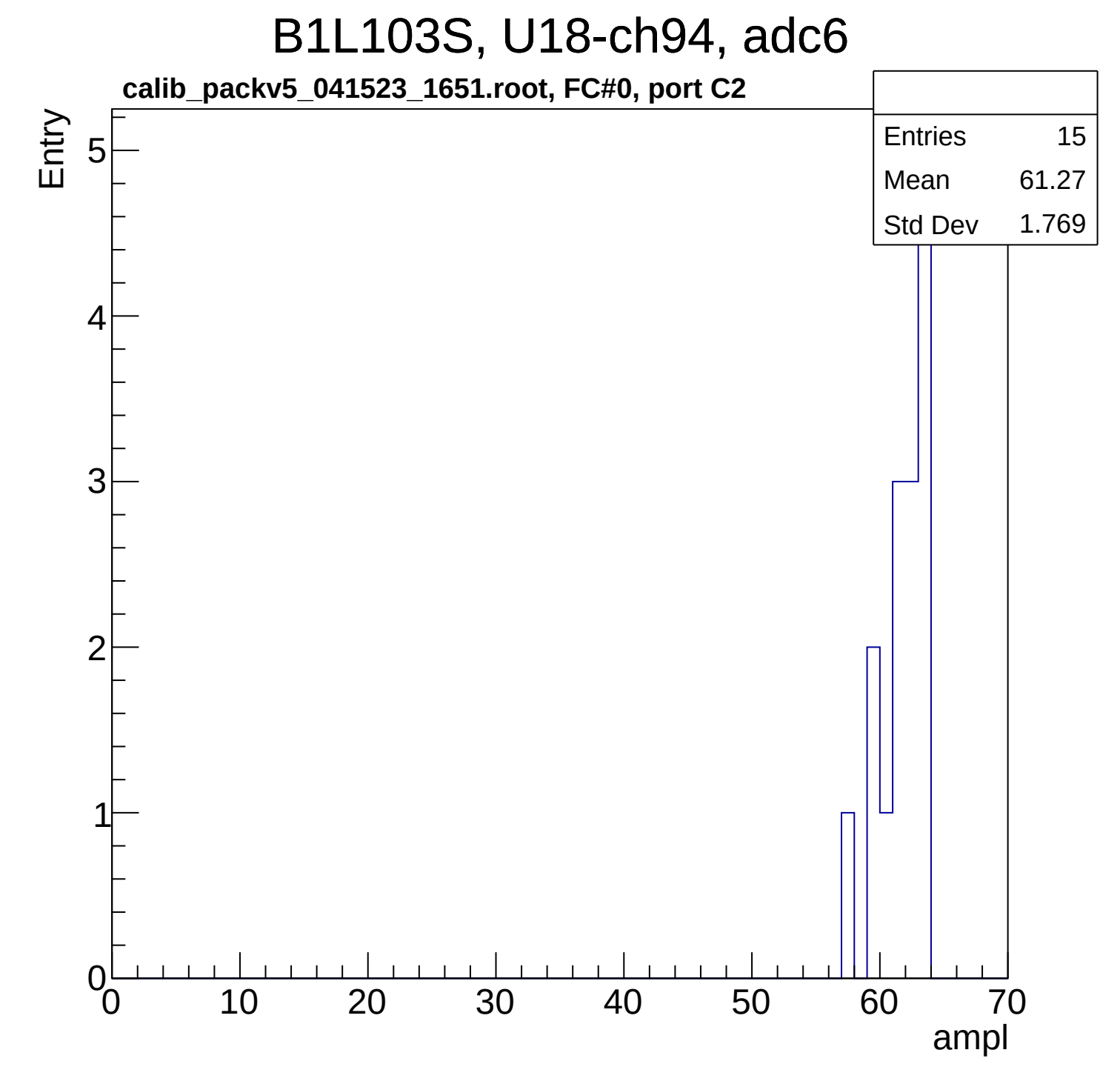
B1L103S, U18-ch94, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 15
Mean 61.27
Std Dev 1.769
Entry
ampl
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1
2
3
4
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0
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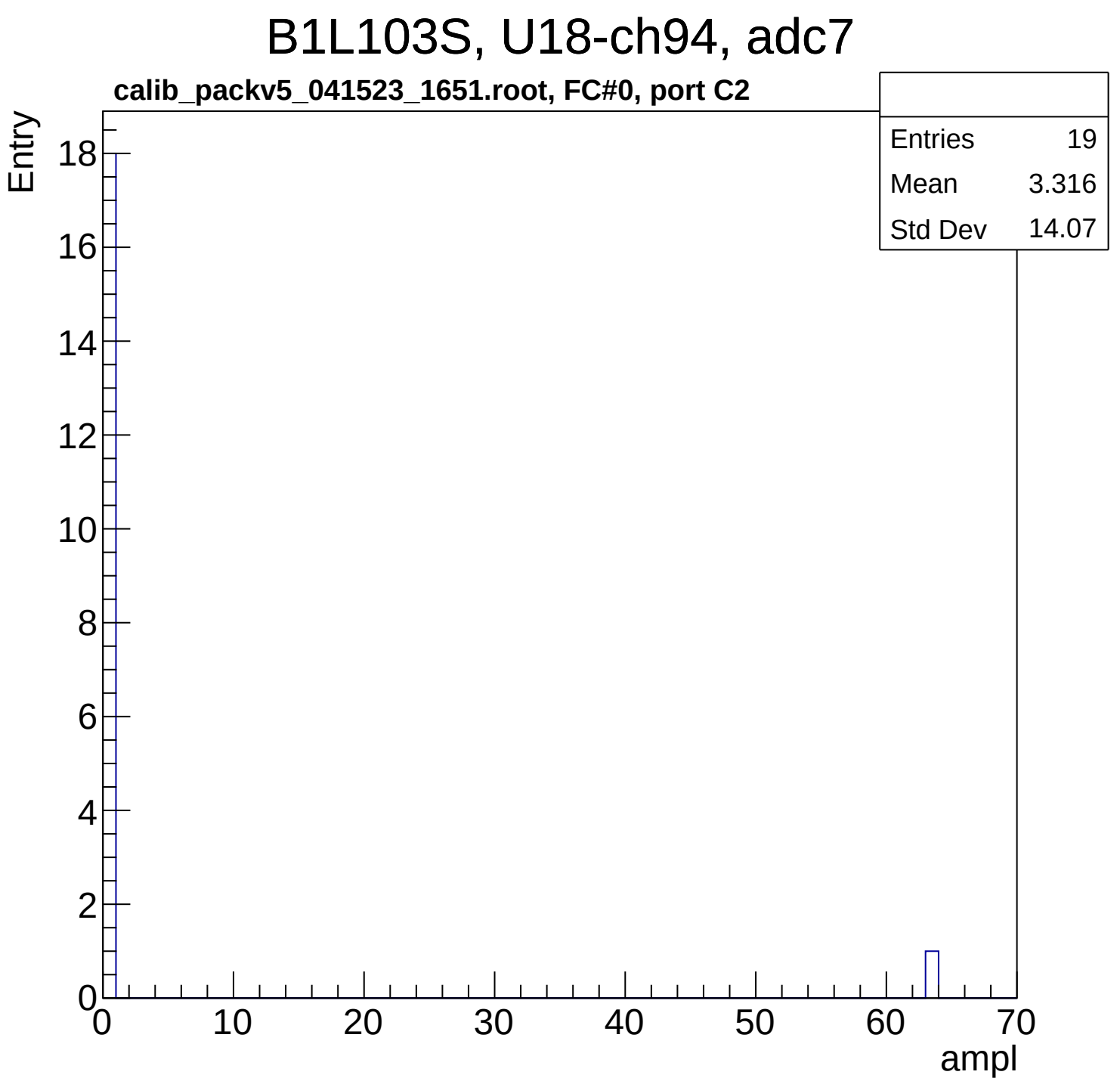
40
50
60
70


B1L103S, U18-ch94, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 3.316
Std Dev 14.07
Entry
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6
8
10
12
14
16
18
0
10
20
30
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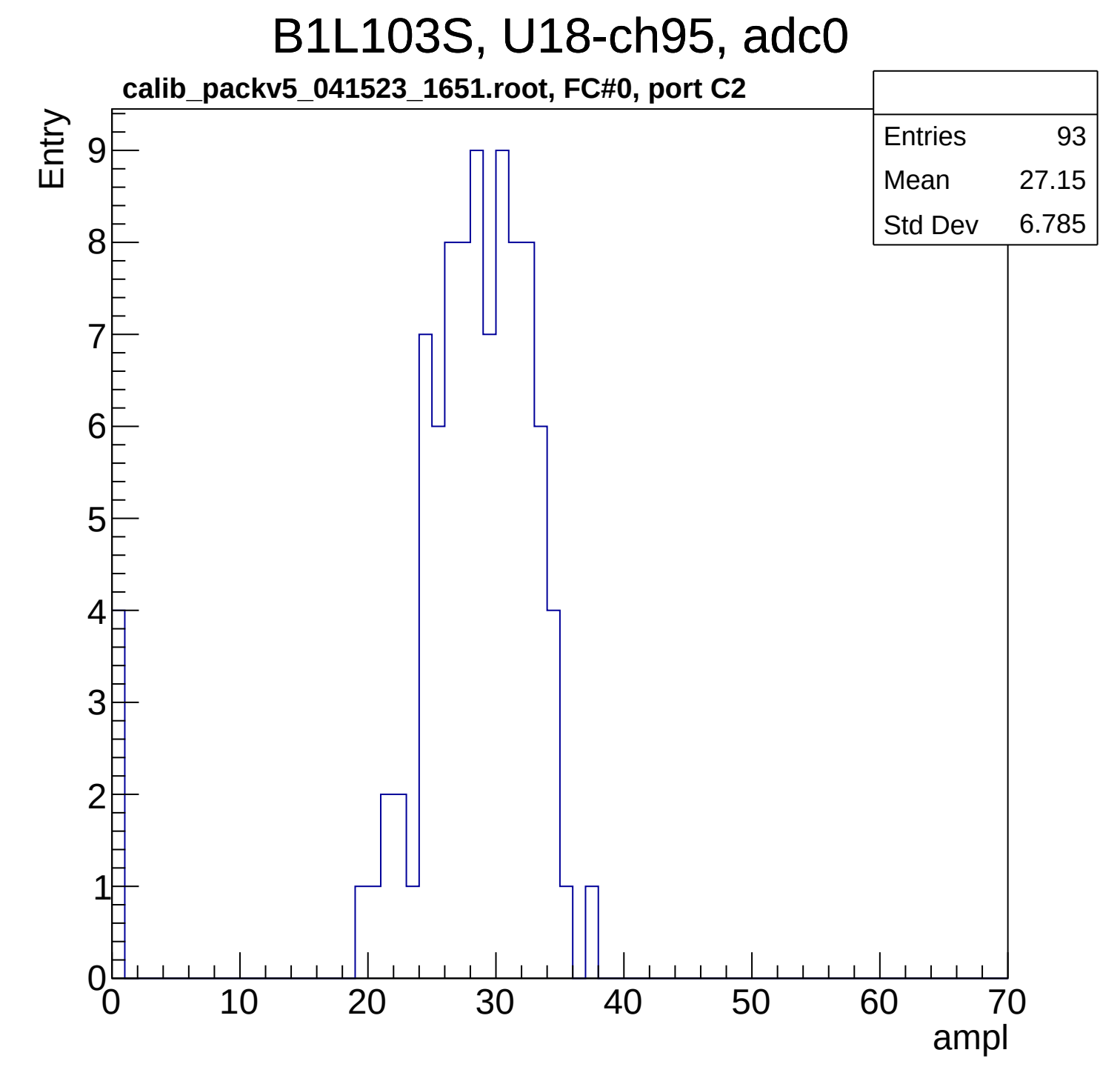
50
60
70
ampl


B1L103S, U18-ch95, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 93
Mean 27.15
Std Dev 6.785
Entry
ampl
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3
4
5
6
7
8
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0
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60
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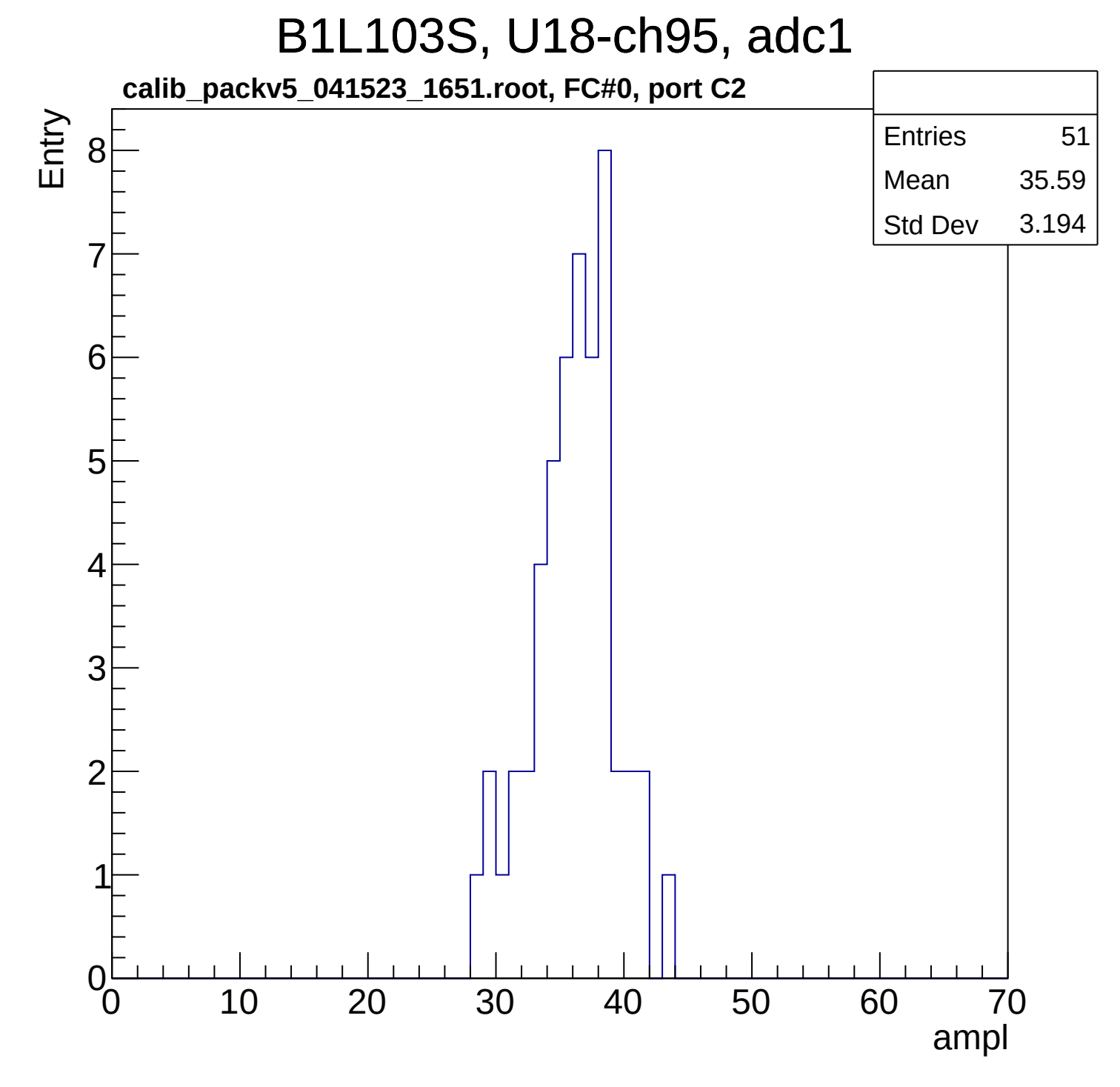
B1L103S, U18-ch95, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 35.59
Std Dev 3.194
Entry
ampl
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4
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6
7
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0
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60
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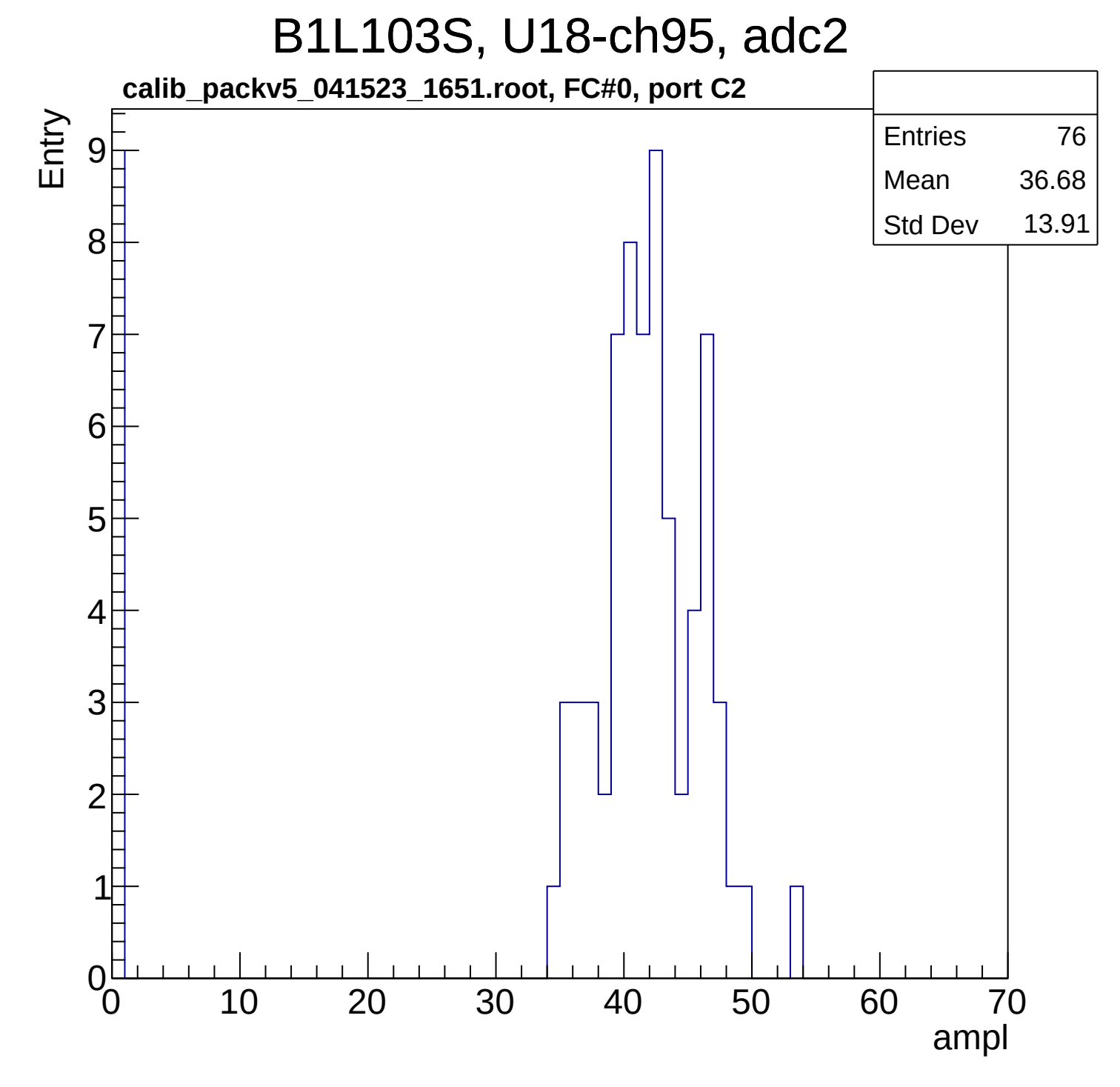
B1L103S, U18-ch95, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 36.68
Std Dev 13.91
Entry
ampl
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3
4
5
6
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0
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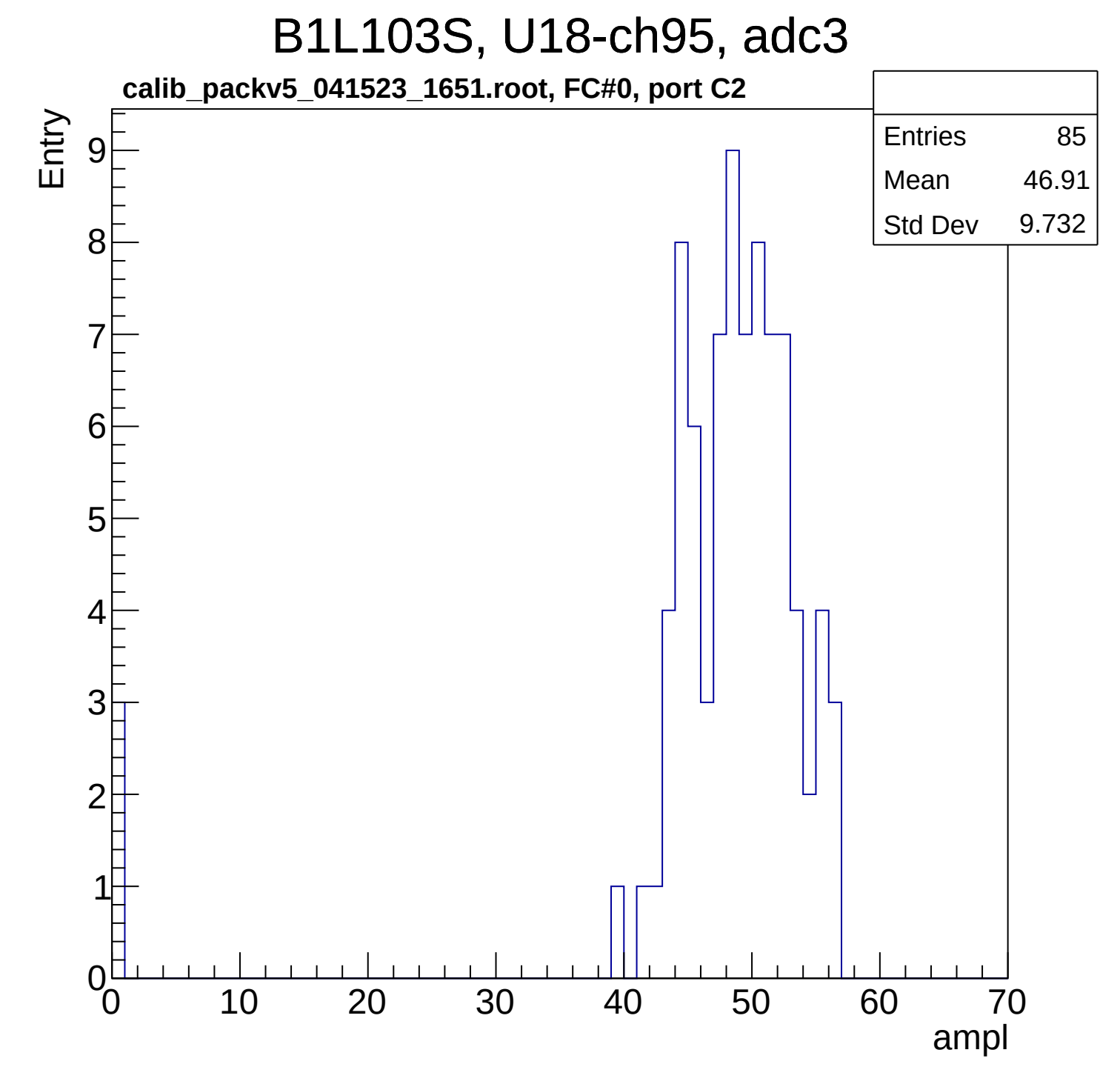
B1L103S, U18-ch95, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 46.91
Std Dev 9.732
Entry
ampl
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3
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5
6
7
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0
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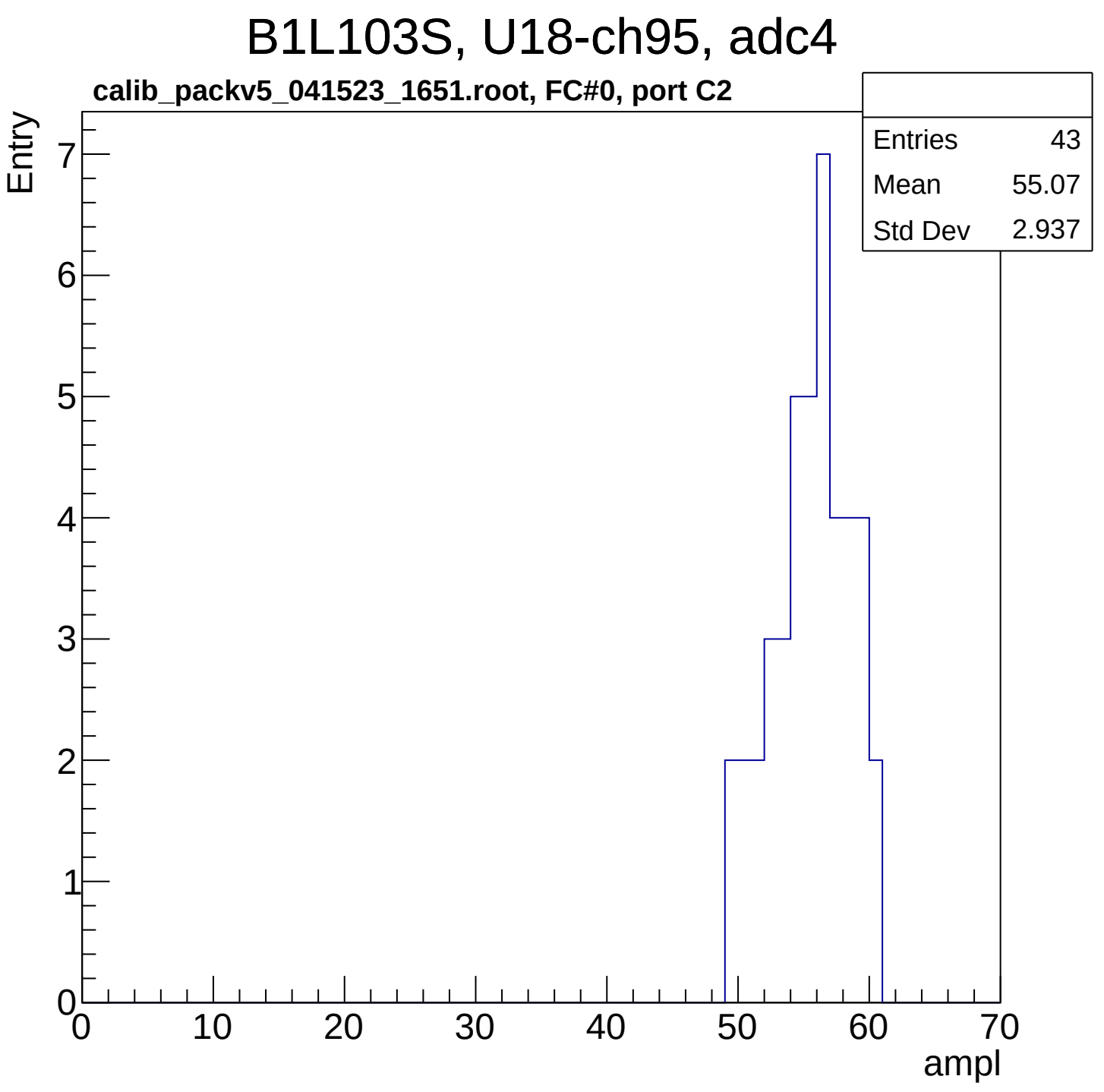
B1L103S, U18-ch95, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 43
Mean 55.07
Std Dev 2.937
Entry
ampl
0
1
2
3
4
5
6
7
0
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60
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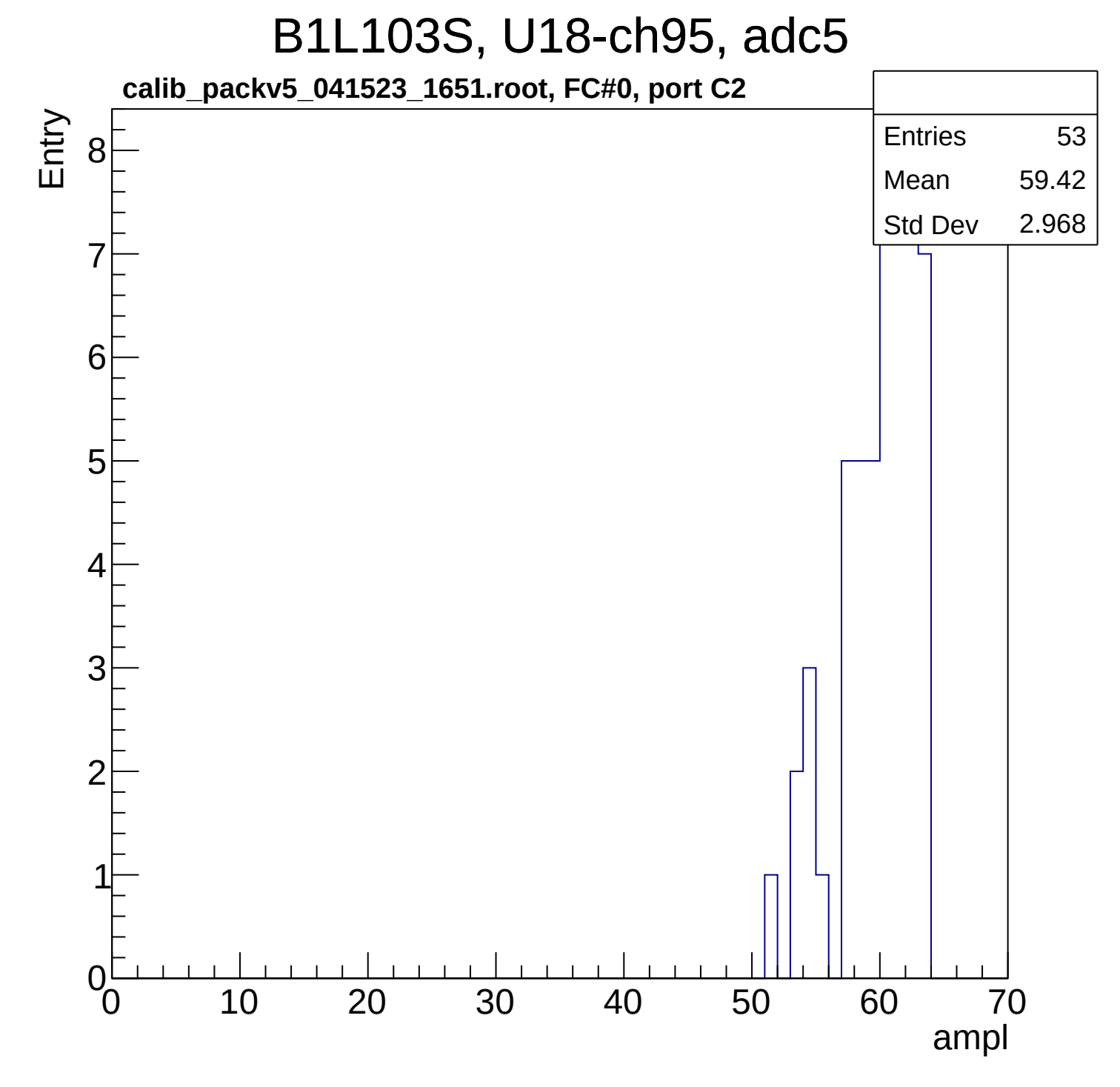
B1L103S, U18-ch95, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 59.42
Std Dev 2.968
Entry
ampl
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1
2
3
4
5
6
7
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0
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40
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60
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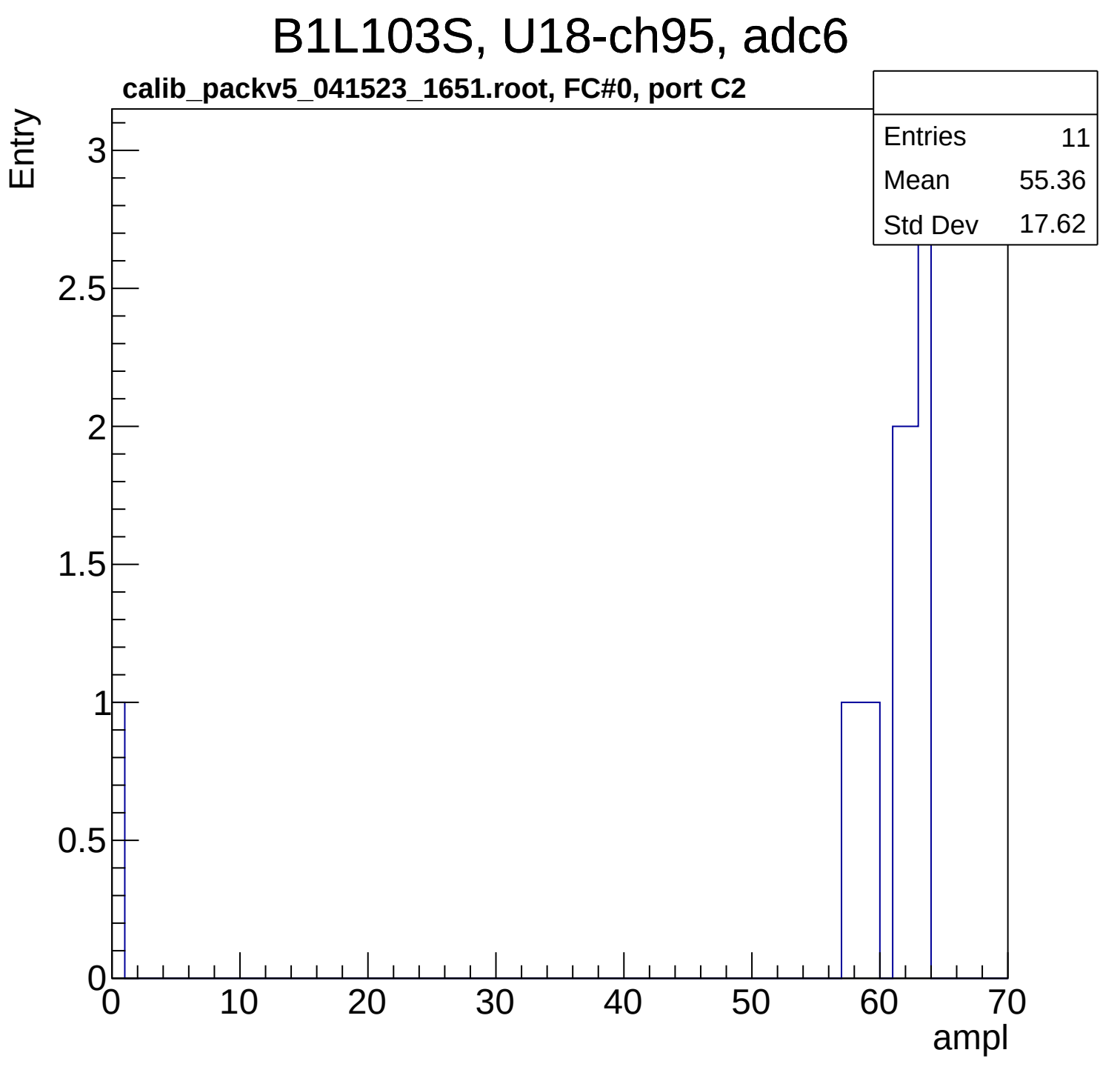
B1L103S, U18-ch95, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 55.36
Std Dev 17.62
Entry
ampl
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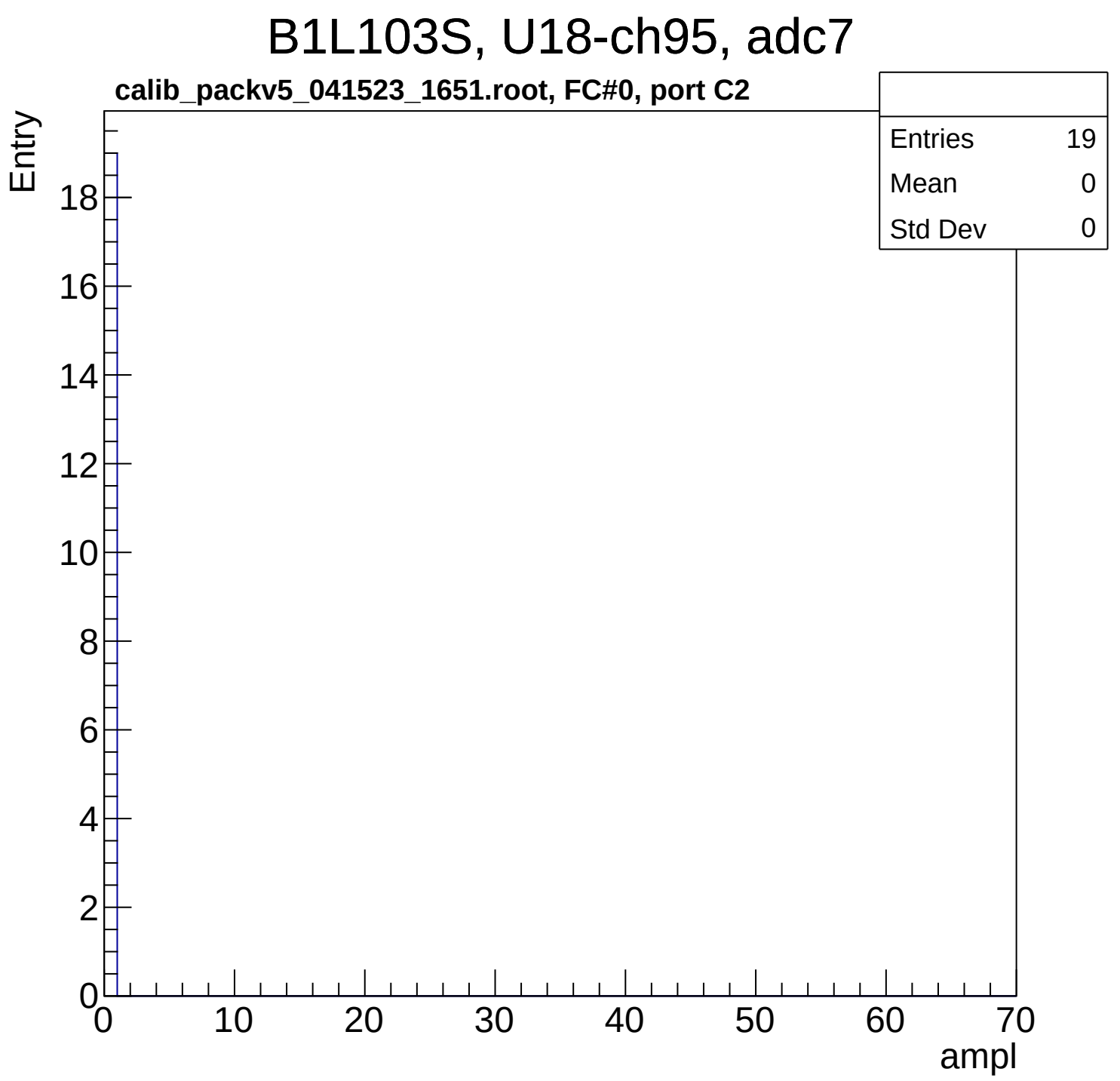
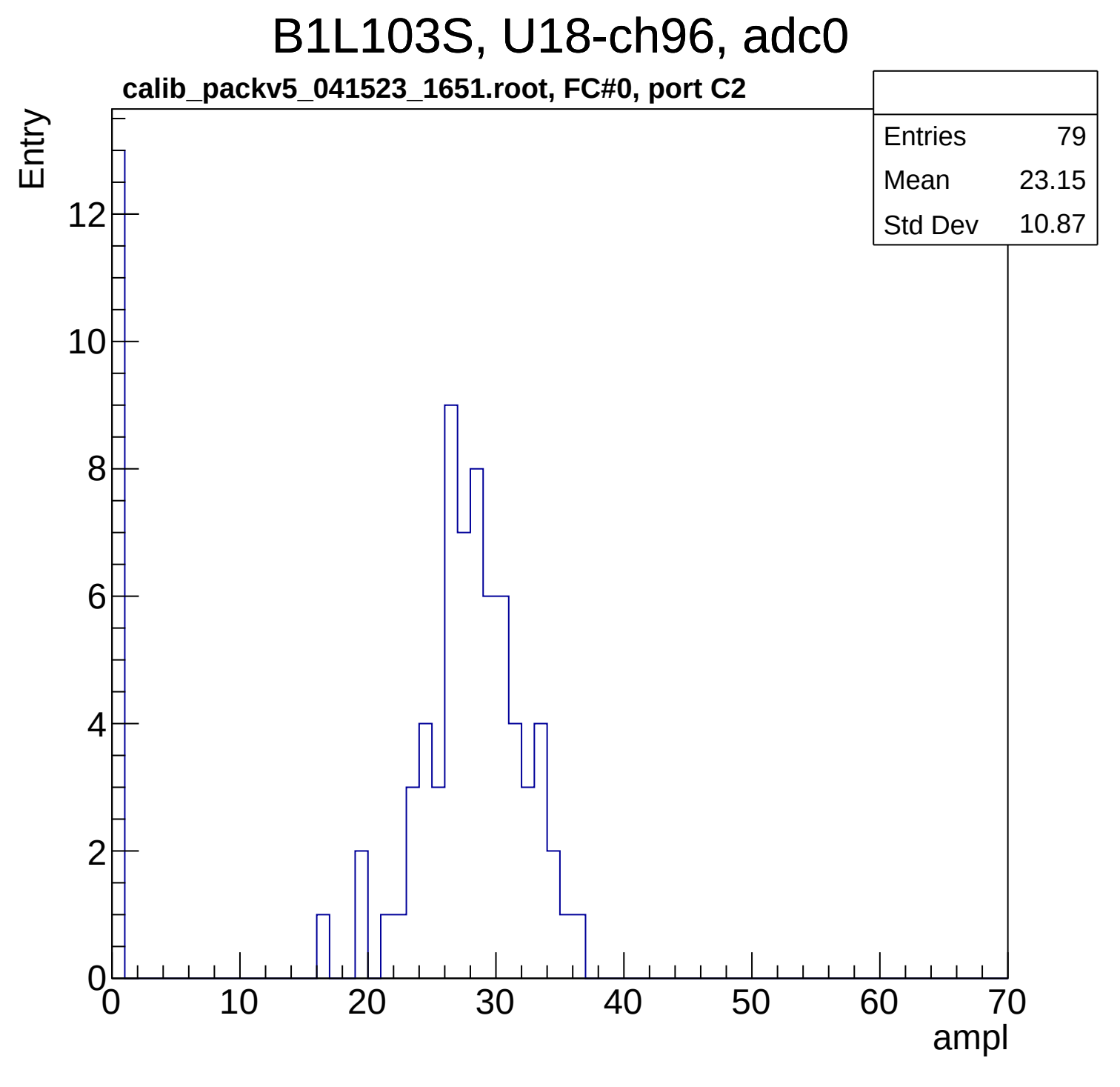
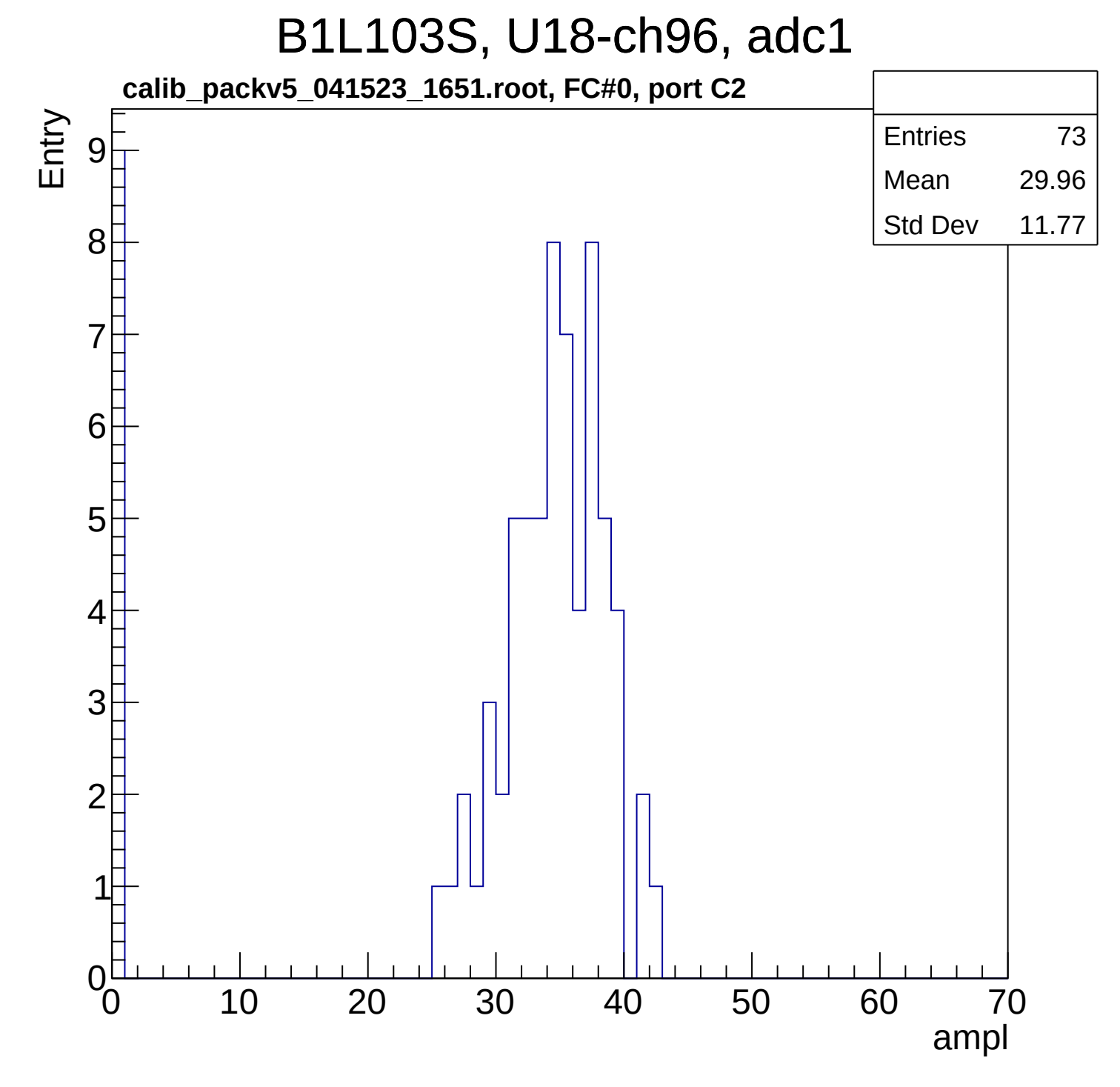
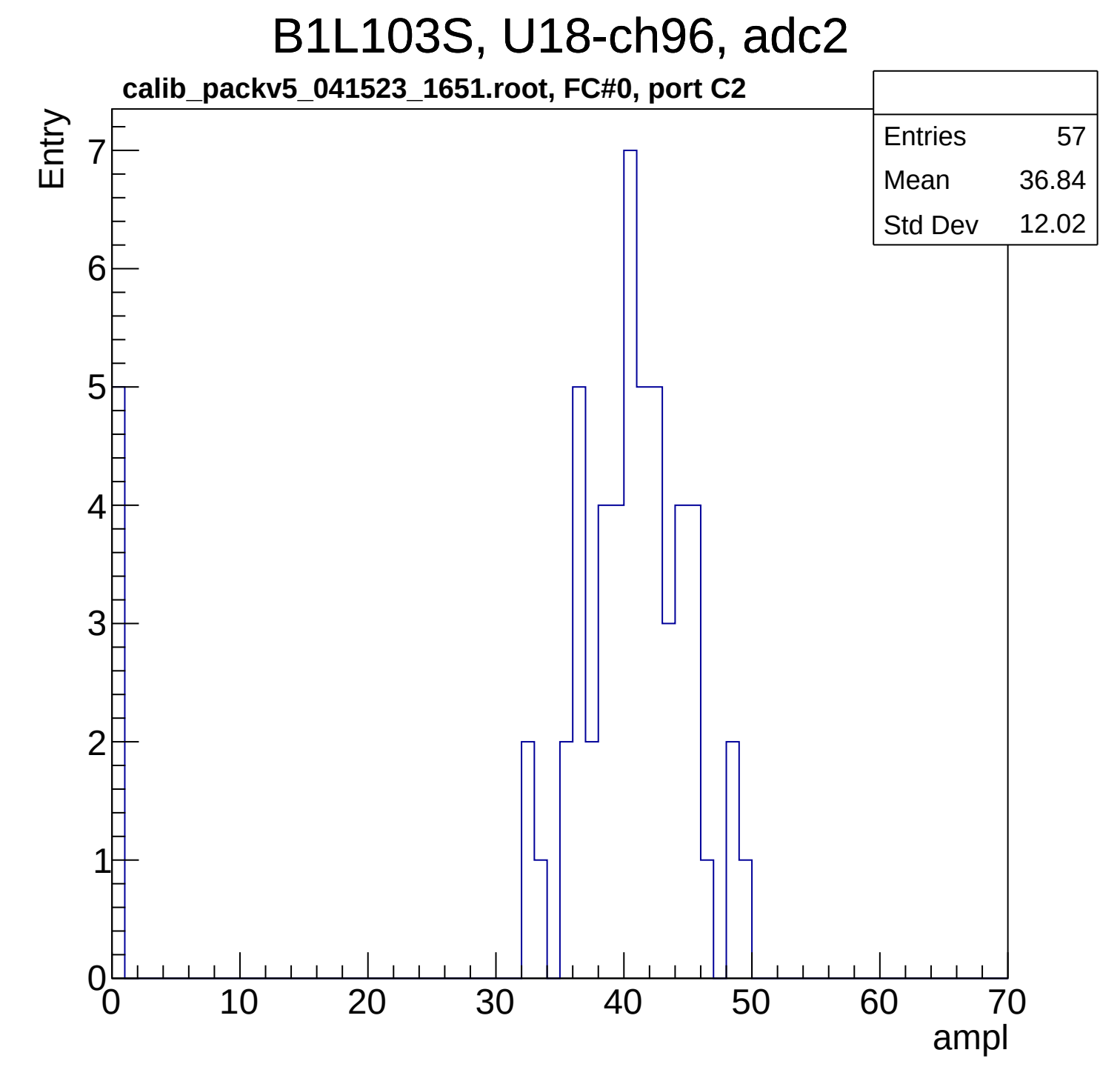
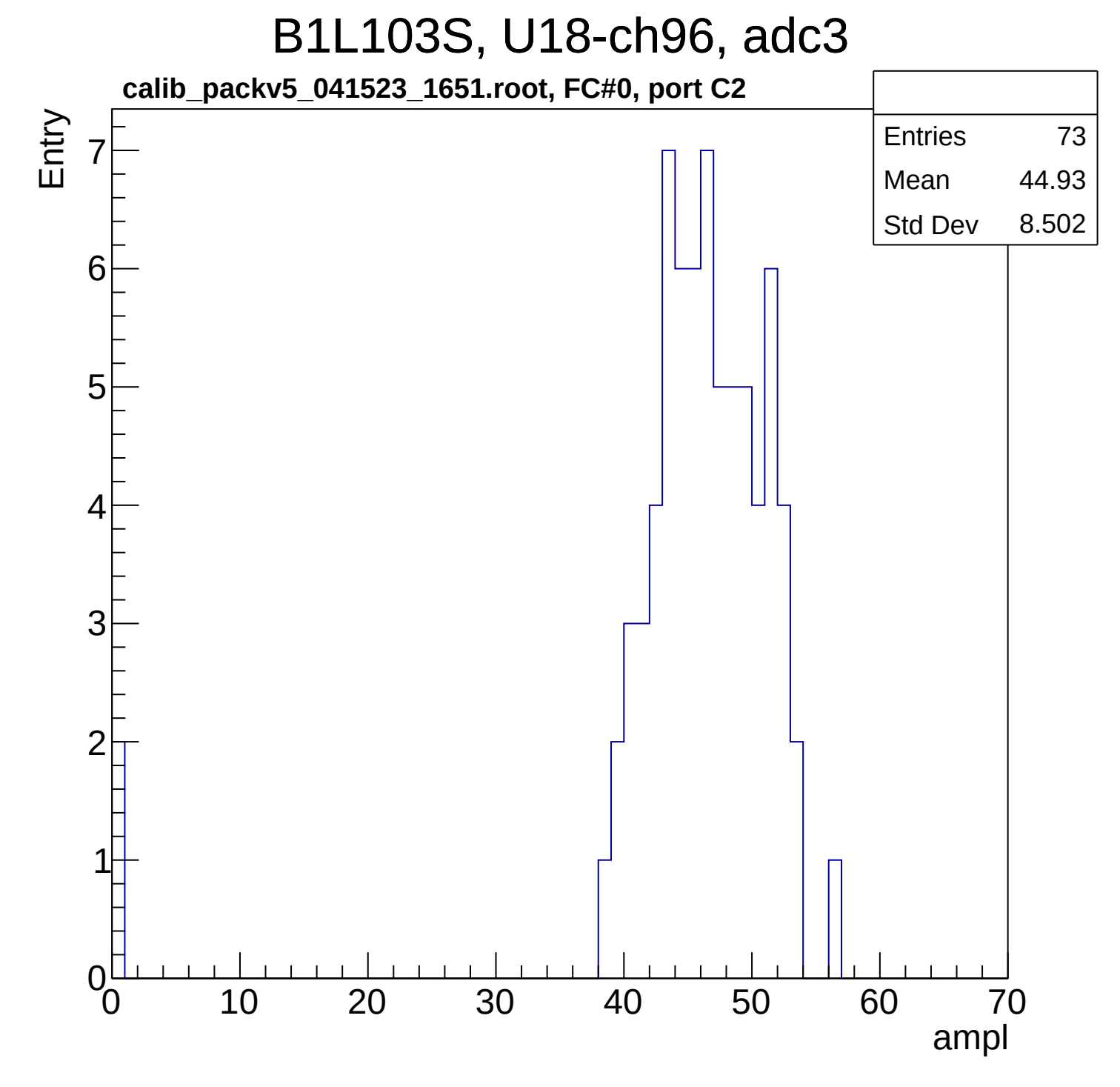
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

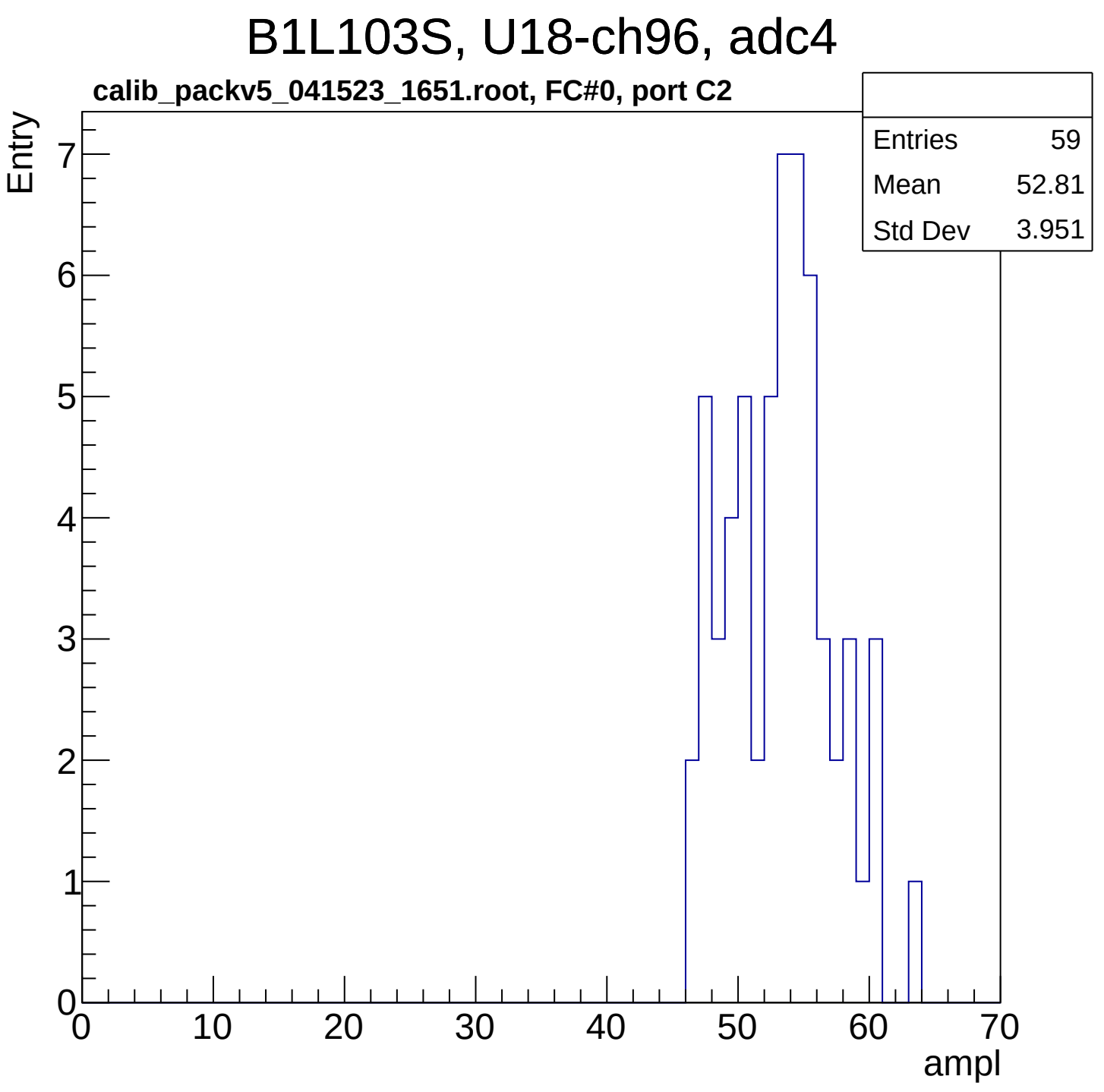

B1L103S, U18-ch95, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

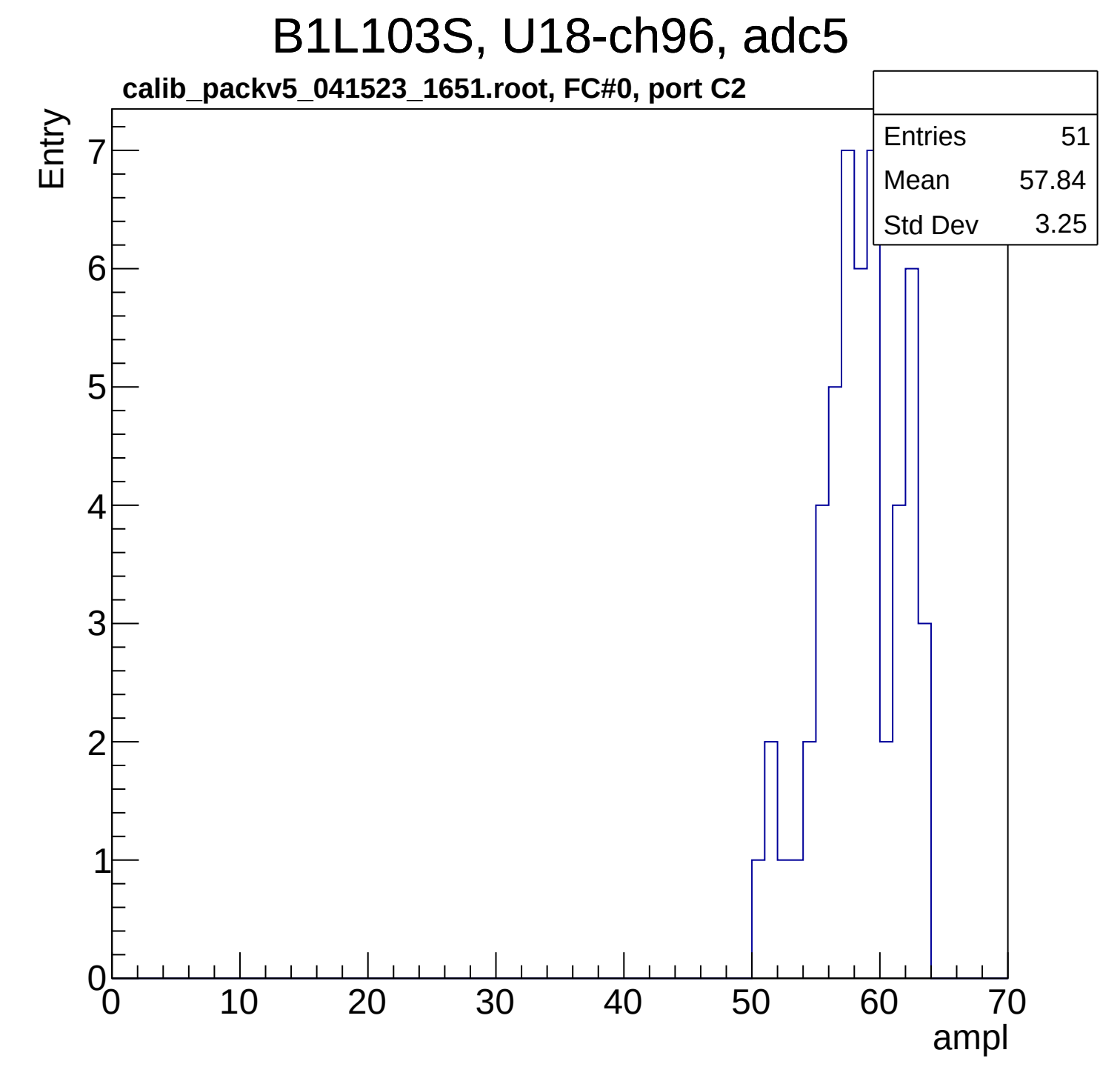

B1L103S, U18-ch96, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 23.15
Std Dev 10.87
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70

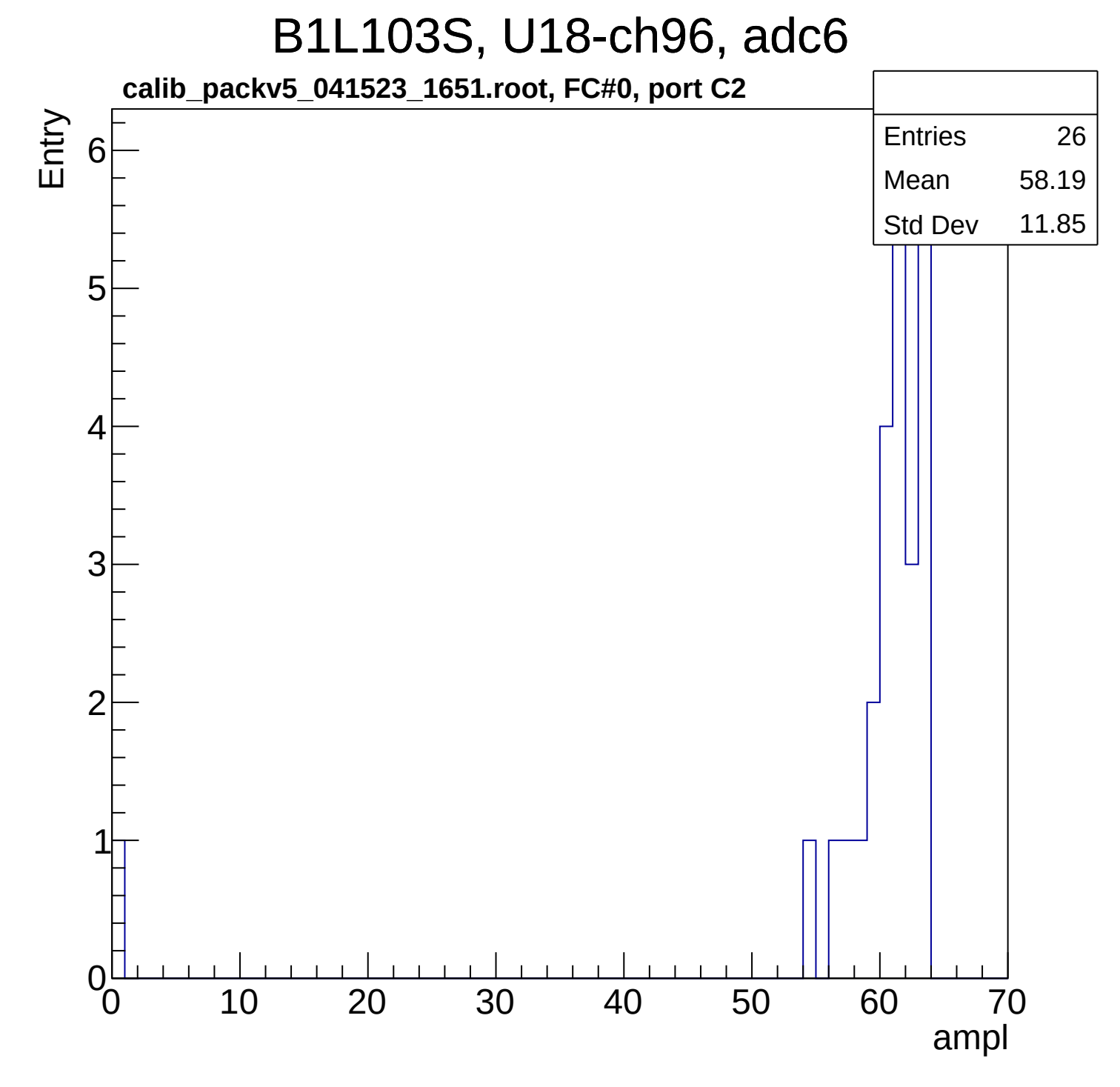

B1L103S, U18-ch96, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 29.96
Std Dev 11.77
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

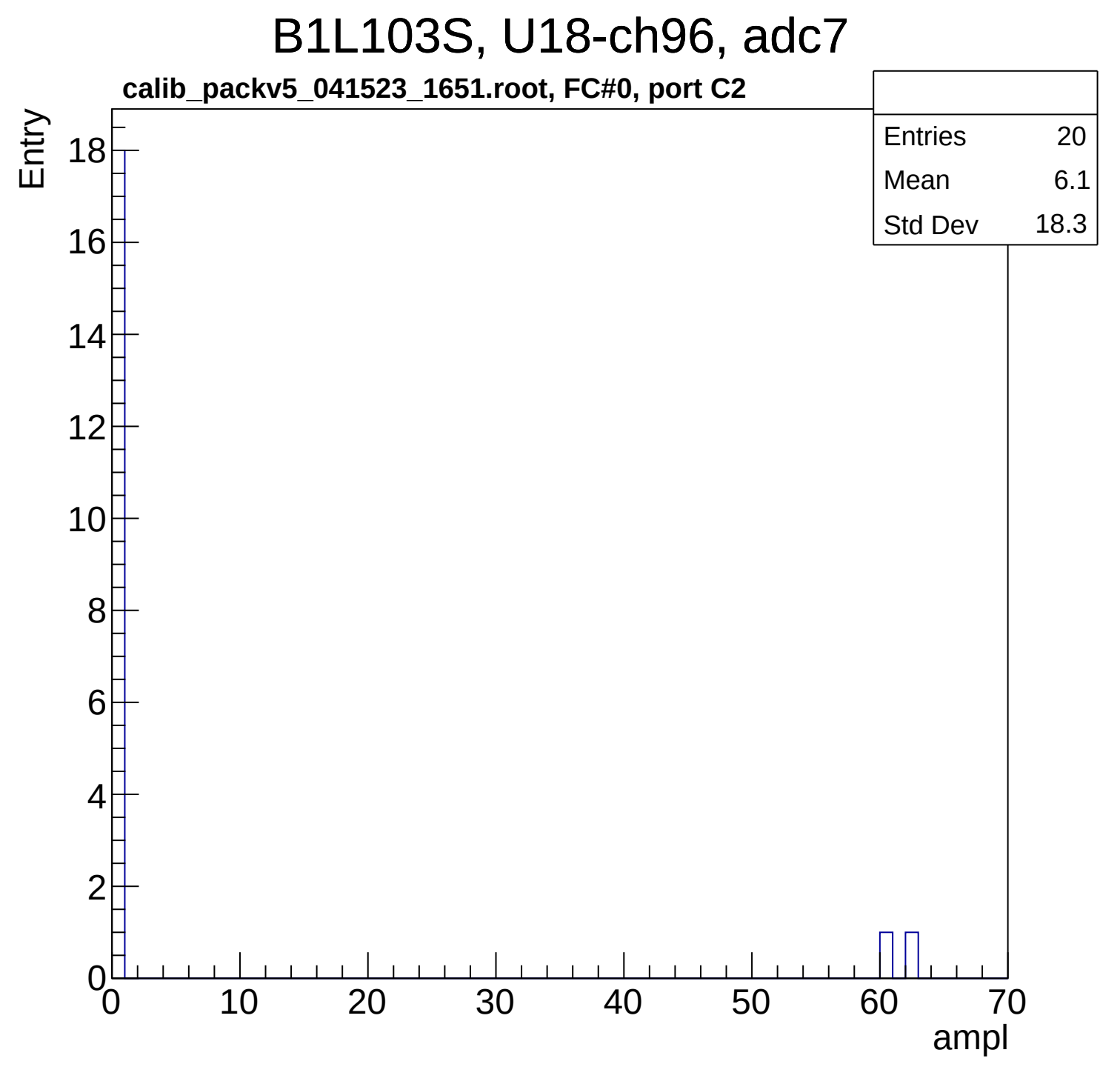

B1L103S, U18-ch96, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 36.84
Std Dev 12.02
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

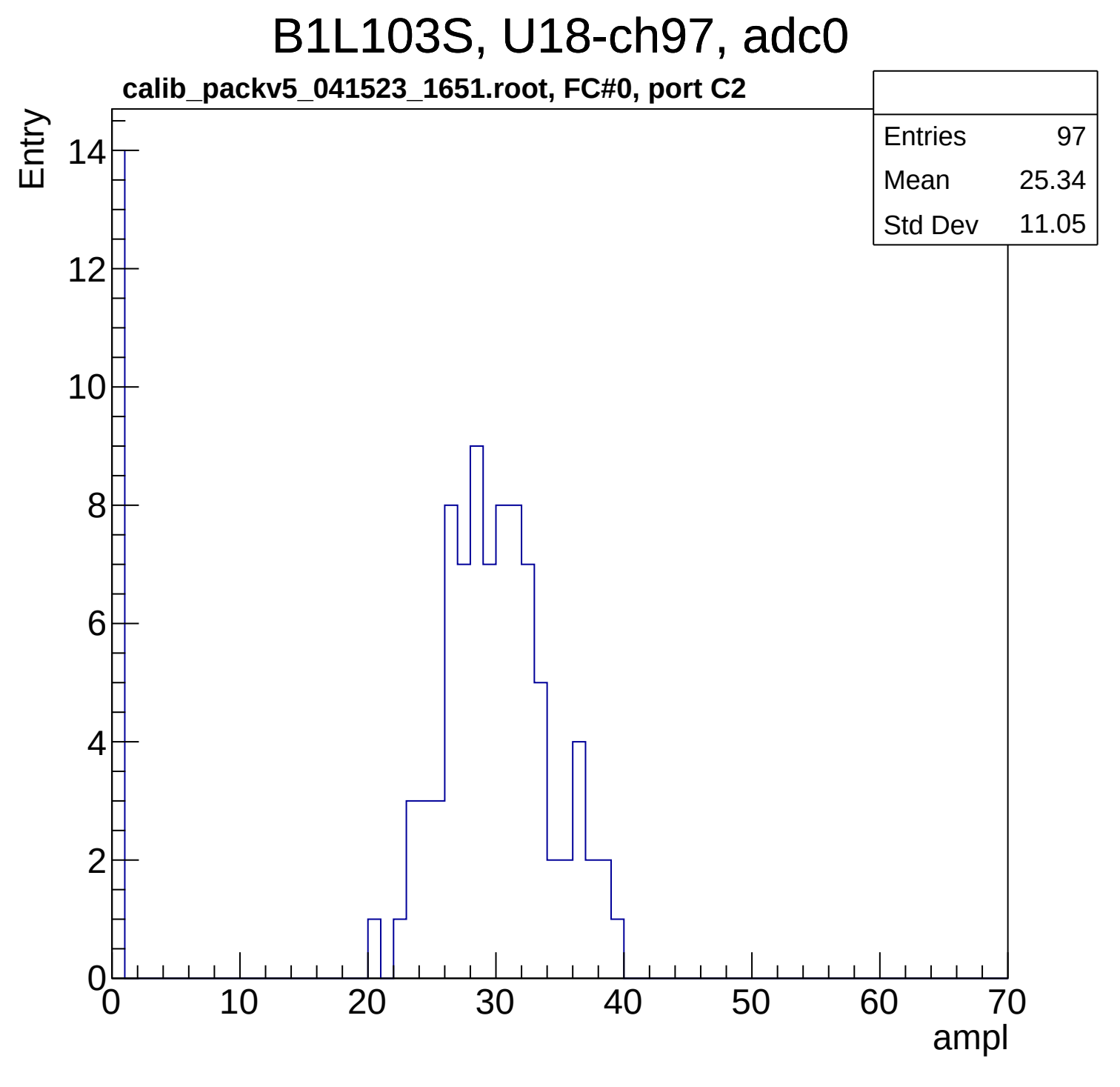

B1L103S, U18-ch96, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 44.93
Std Dev 8.502
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

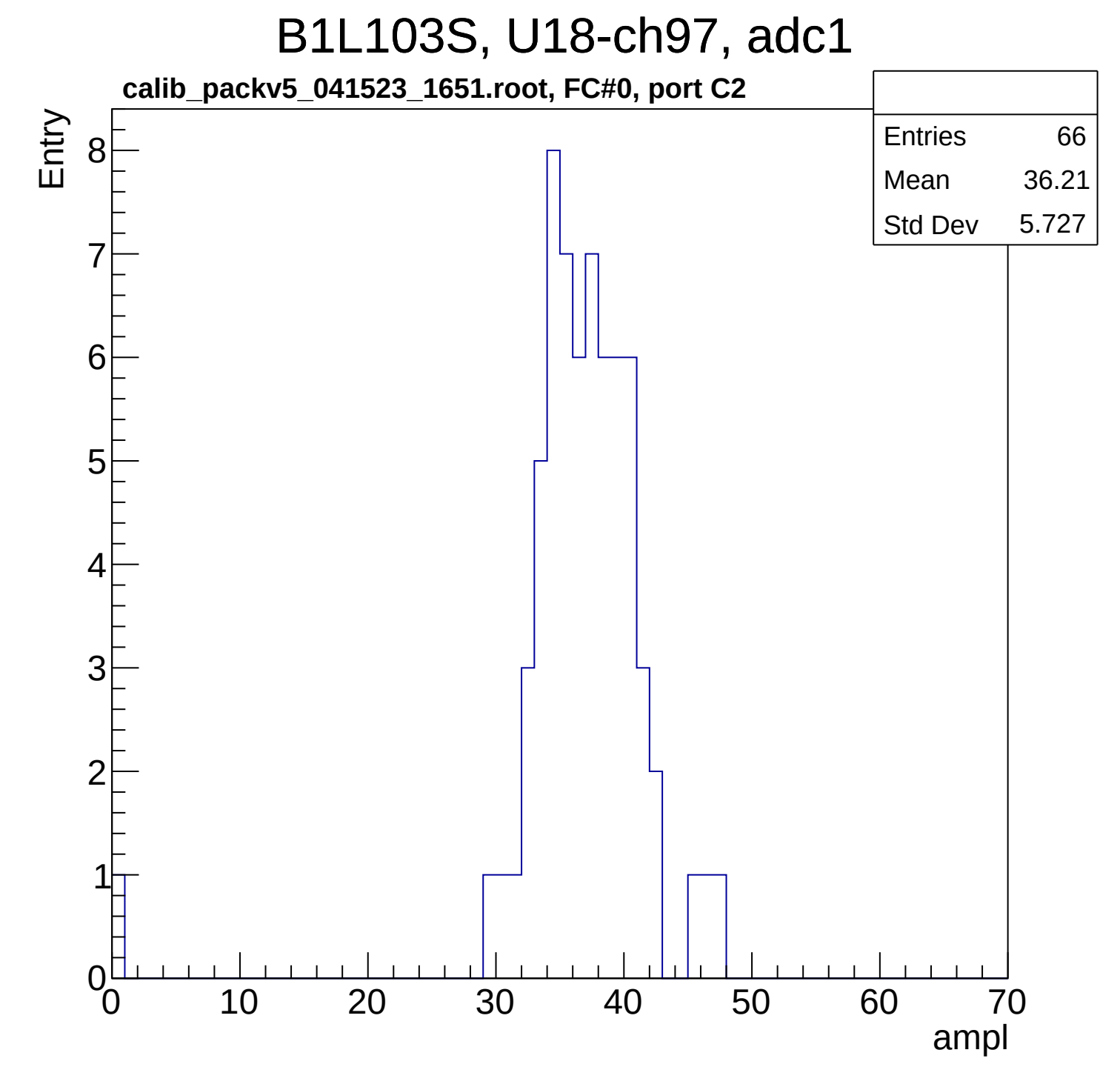

B1L103S, U18-ch96, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 52.81
Std Dev 3.951
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U18-ch96, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 57.84
Std Dev 3.25
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U18-ch96, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 26
Mean 58.19
Std Dev 11.85
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U18-ch96, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 6.1
Std Dev 18.3
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch97, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 97
Mean 25.34
Std Dev 11.05
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L103S, U18-ch97, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 36.21
Std Dev 5.727
Entry
ampl
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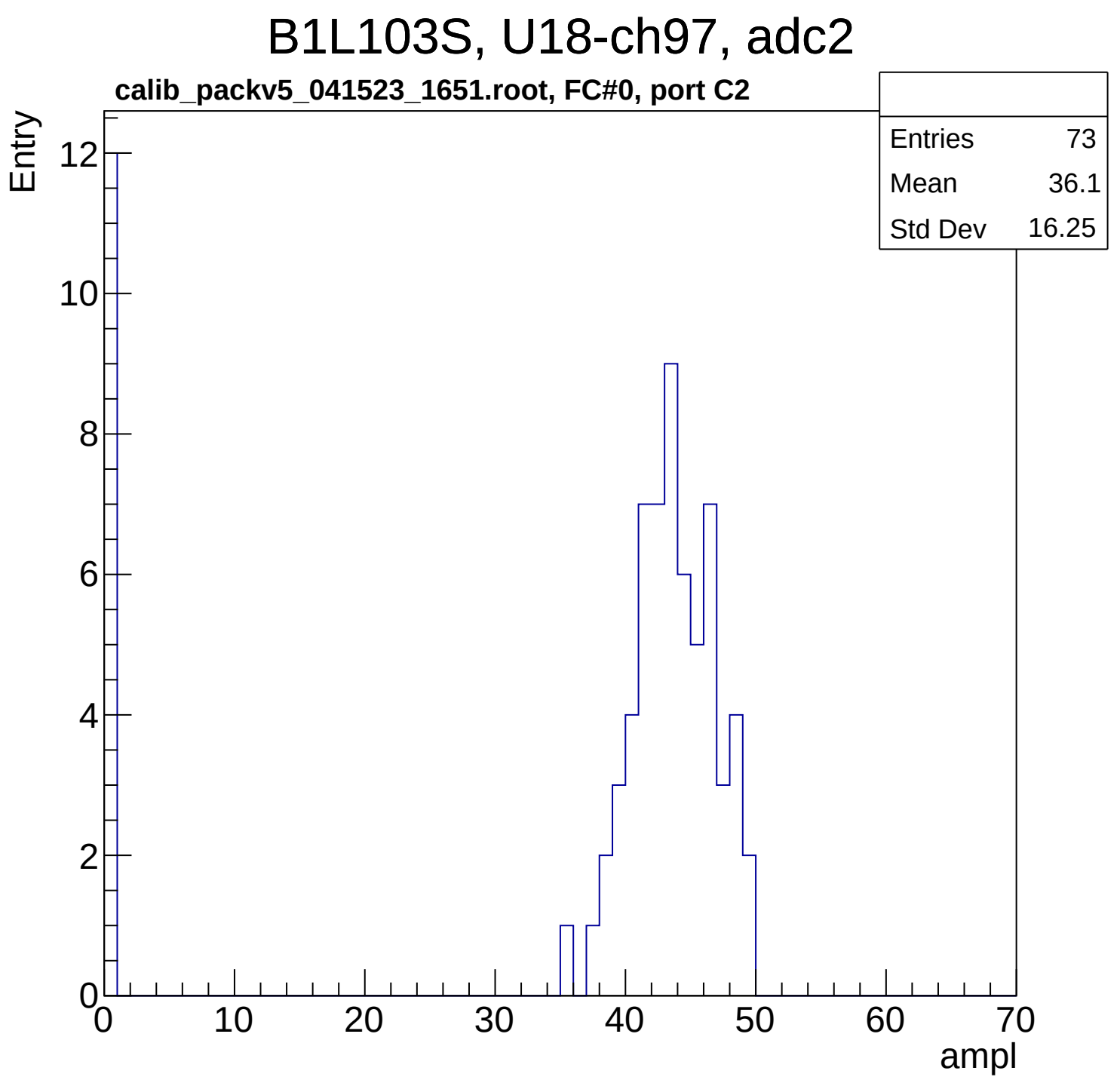
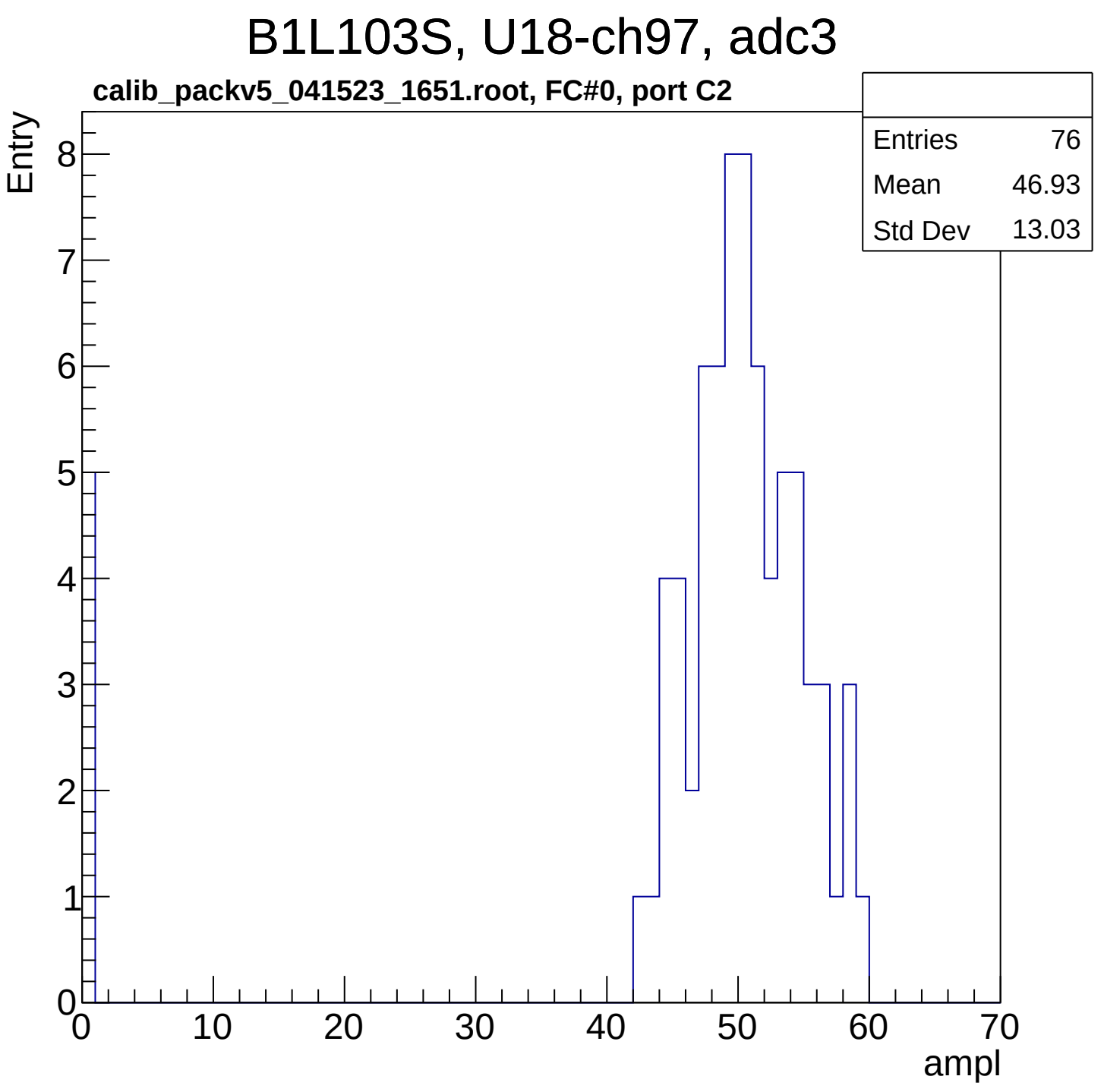
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch97, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 36.1
Std Dev 16.25
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch97, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 46.93
Std Dev 13.03
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
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60
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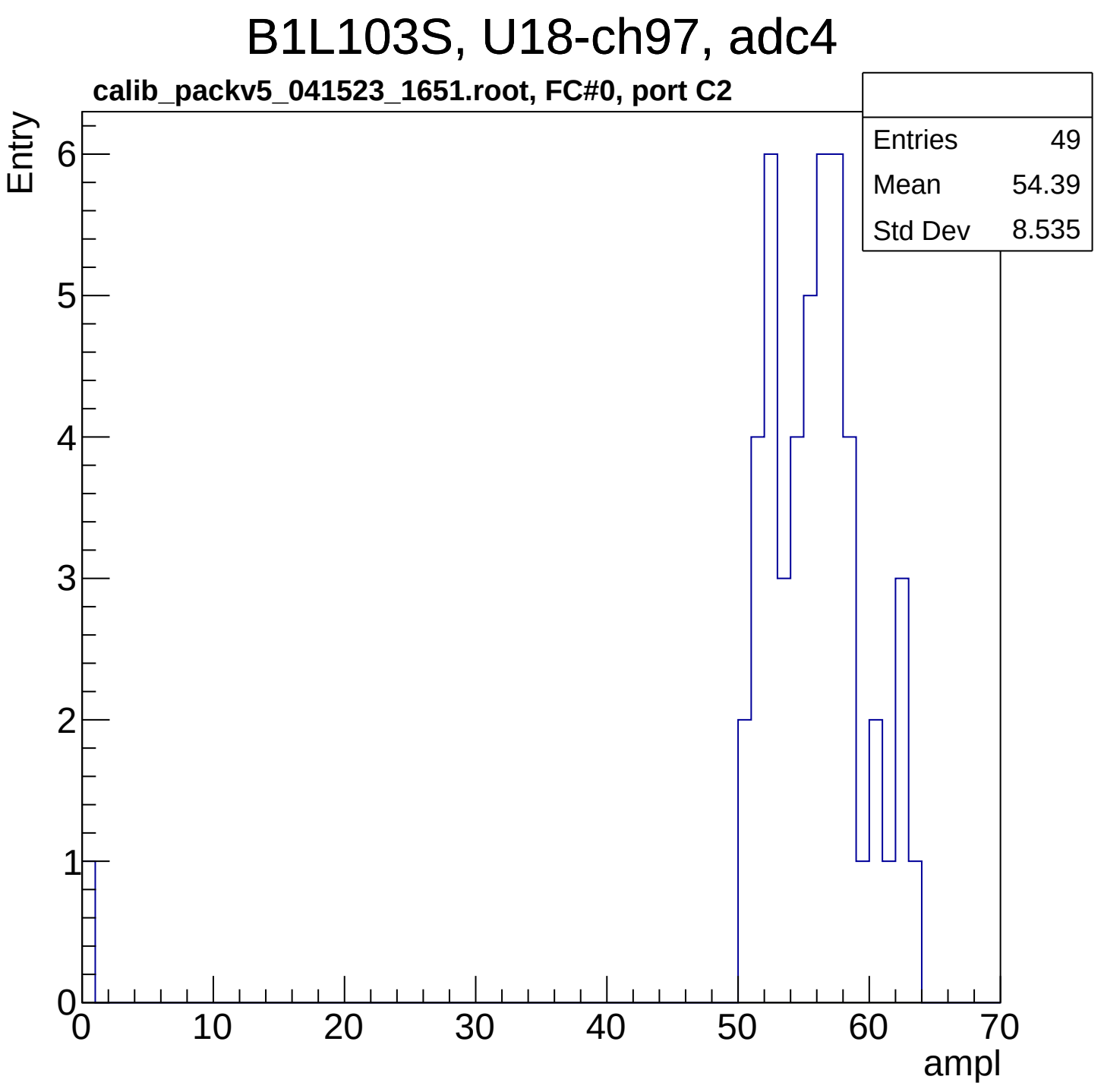
B1L103S, U18-ch97, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 54.39
Std Dev 8.535
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
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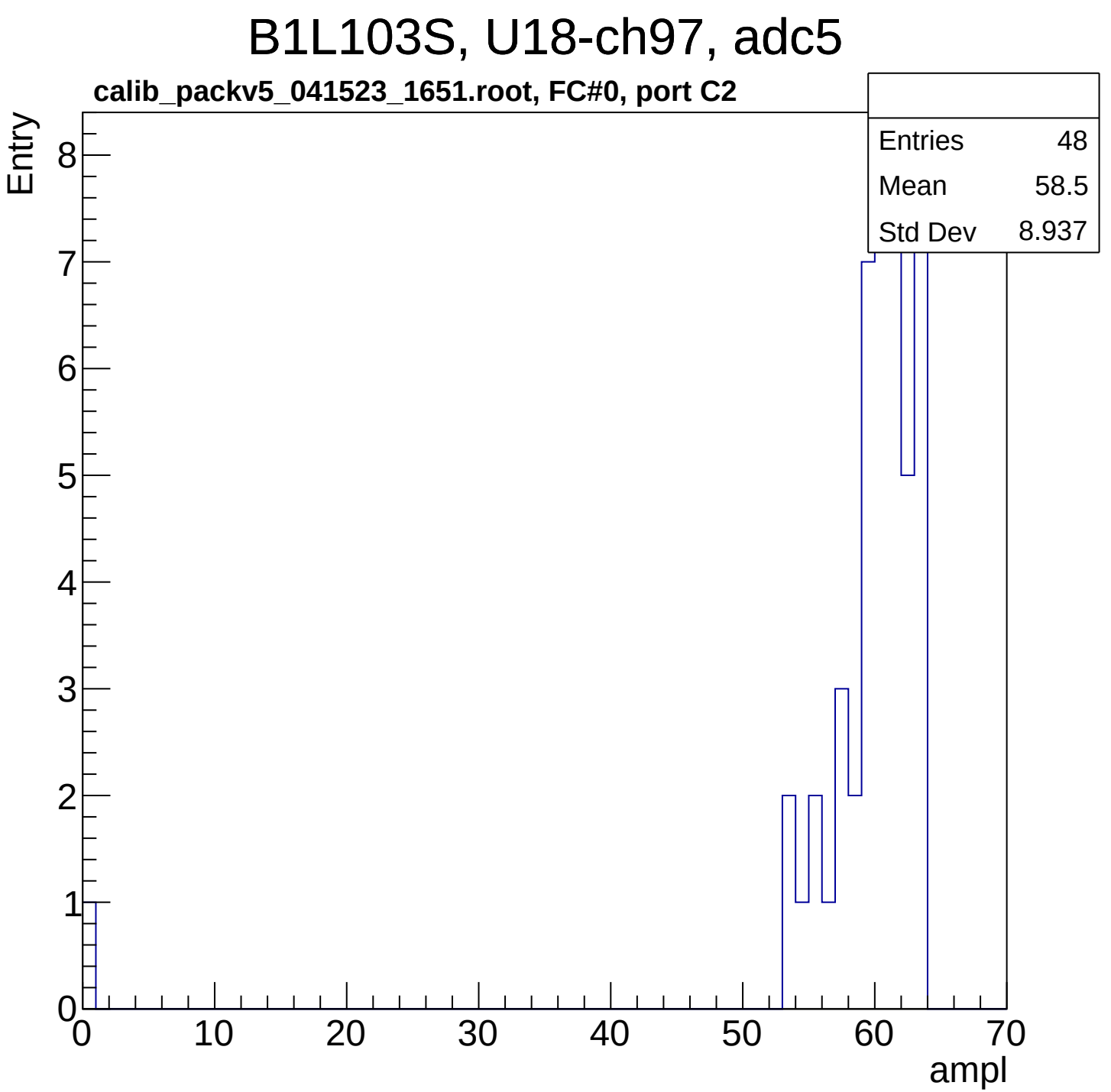
B1L103S, U18-ch97, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 58.5
Std Dev 8.937
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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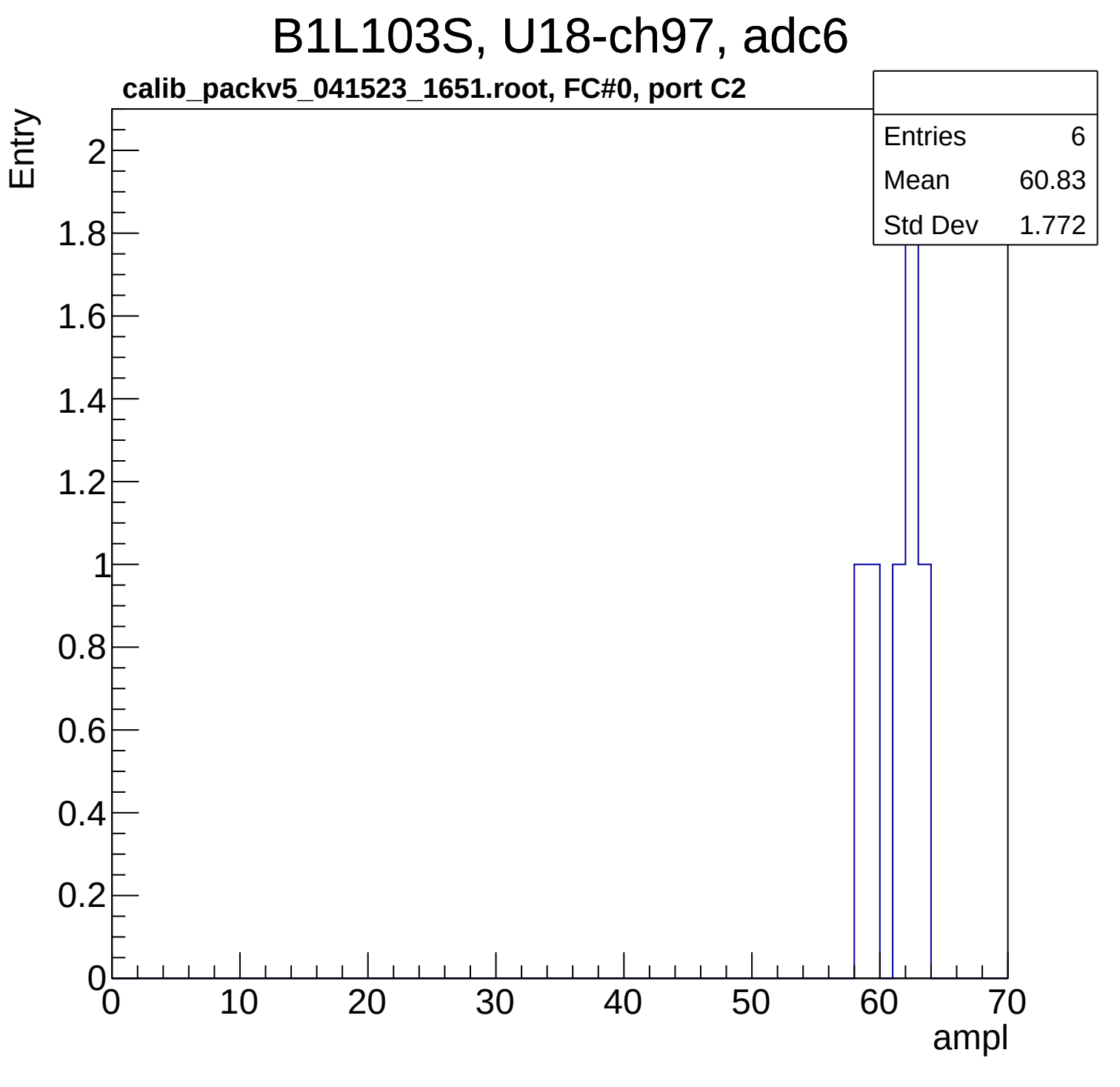
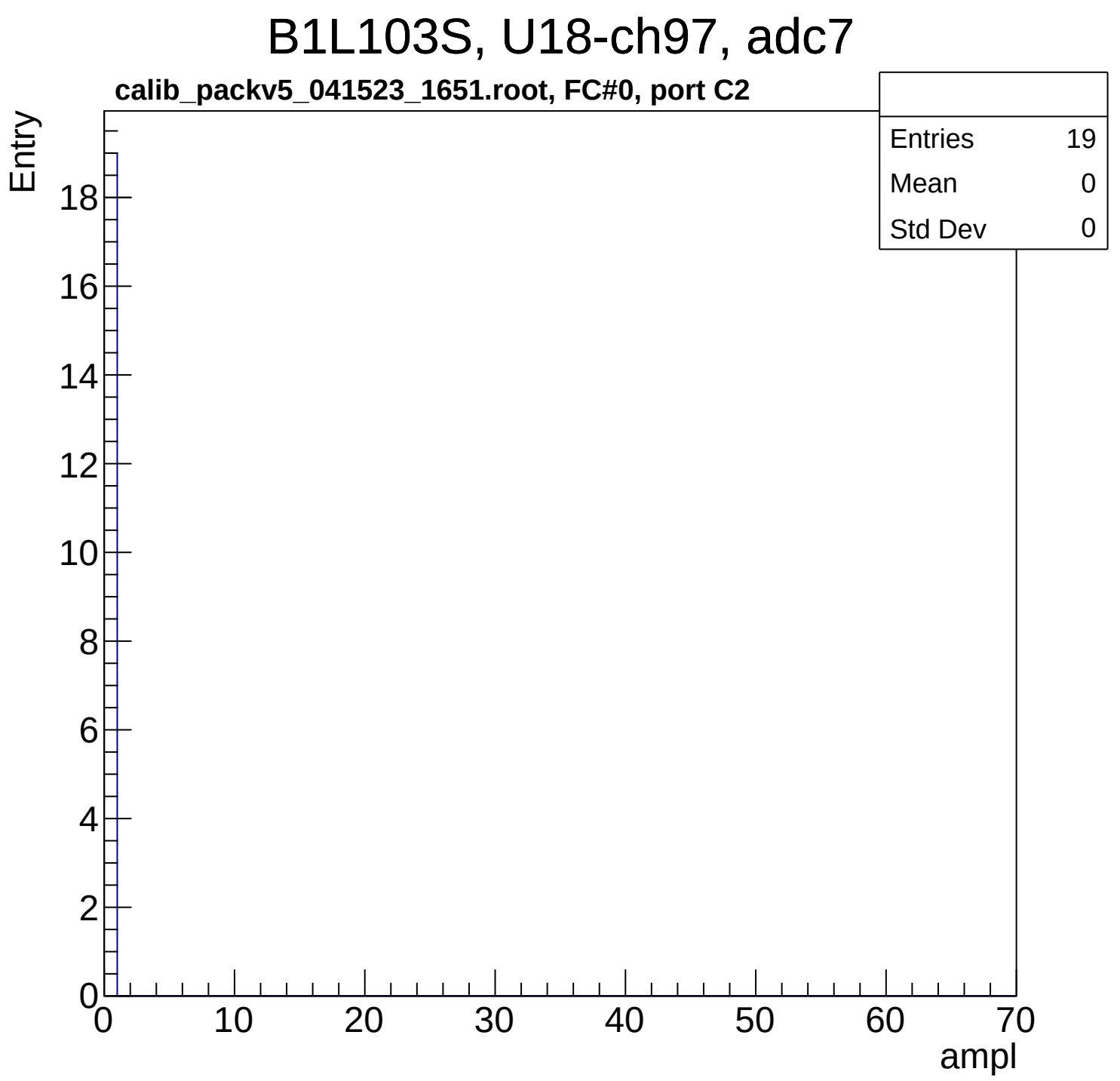
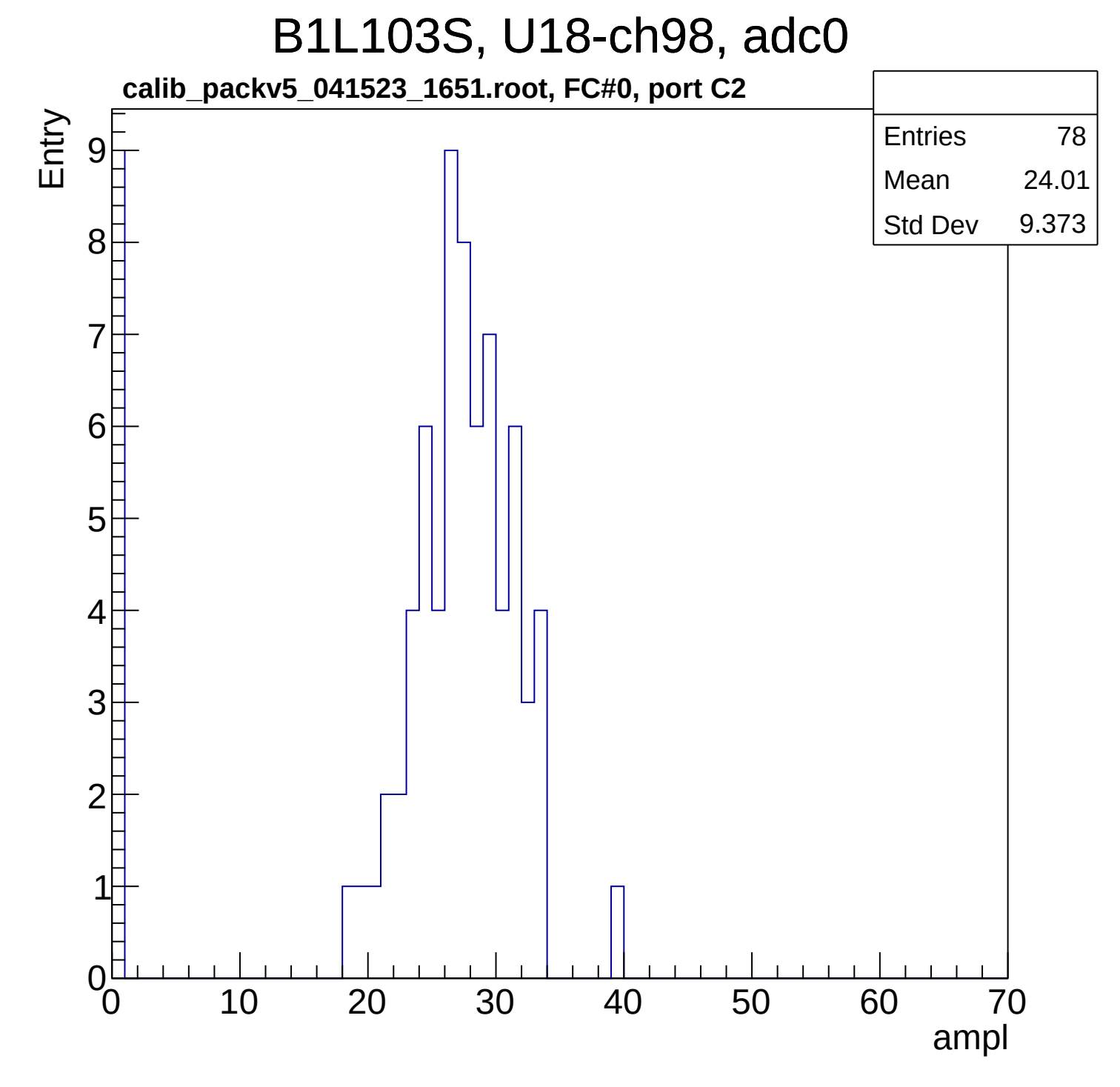

B1L103S, U18-ch97, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 60.83
Std Dev 1.772
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U18-ch97, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch98, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 24.01
Std Dev 9.373
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
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20
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40
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60
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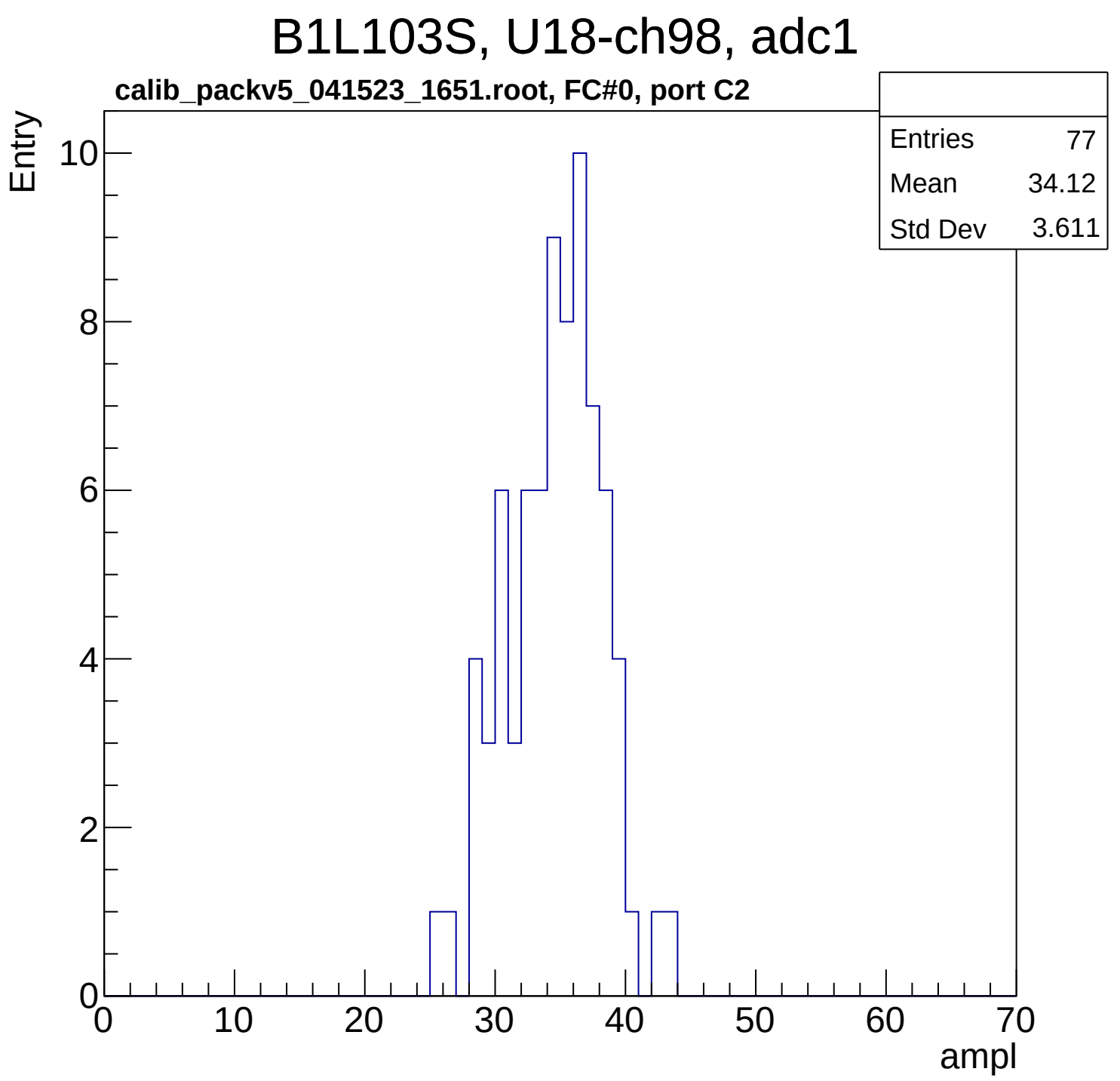
B1L103S, U18-ch98, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 34.12
Std Dev 3.611
Entry
0
2
4
6
8
10
0
10
20
30
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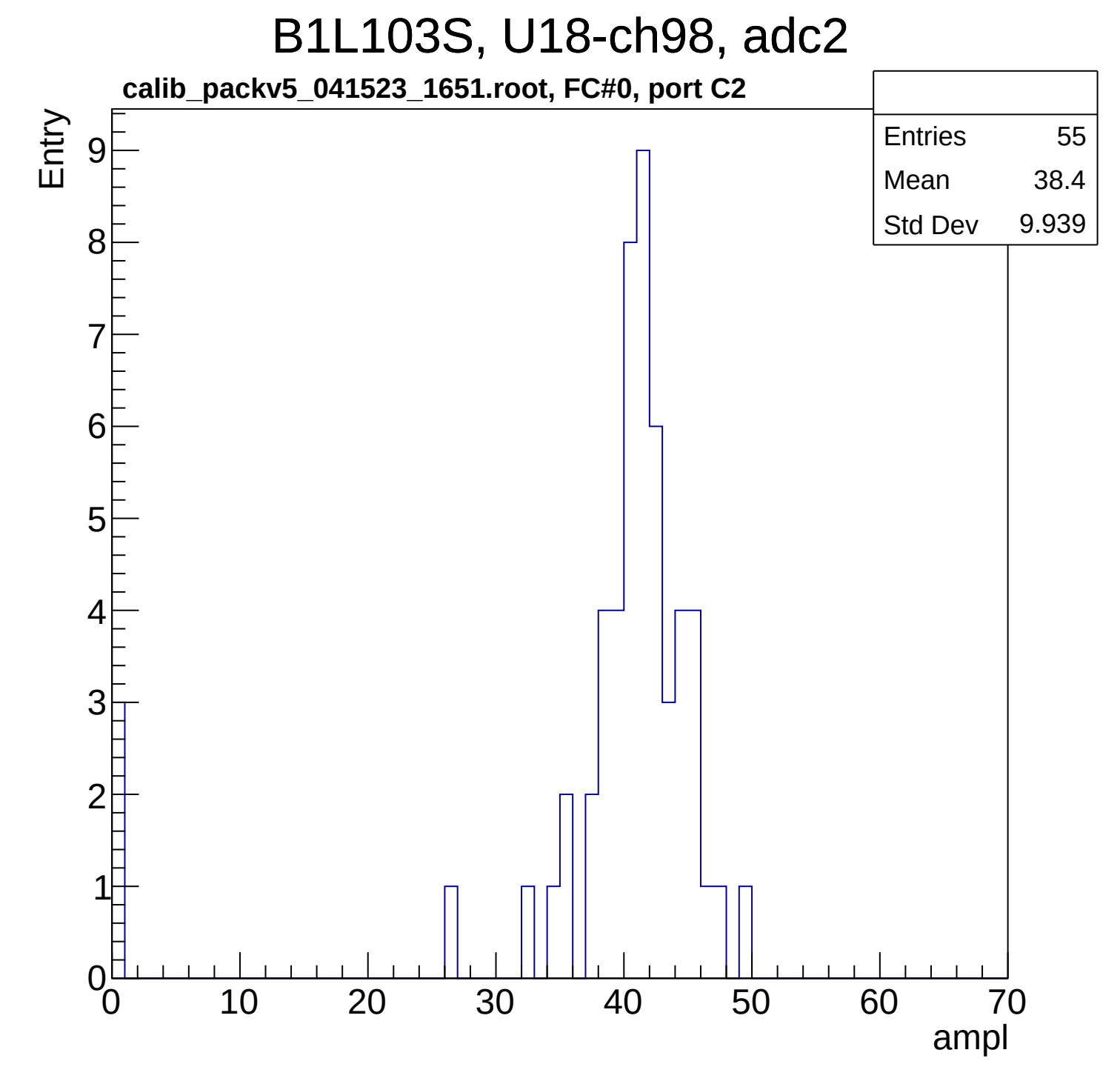
50
60
70
ampl


B1L103S, U18-ch98, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 38.4
Std Dev 9.939
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
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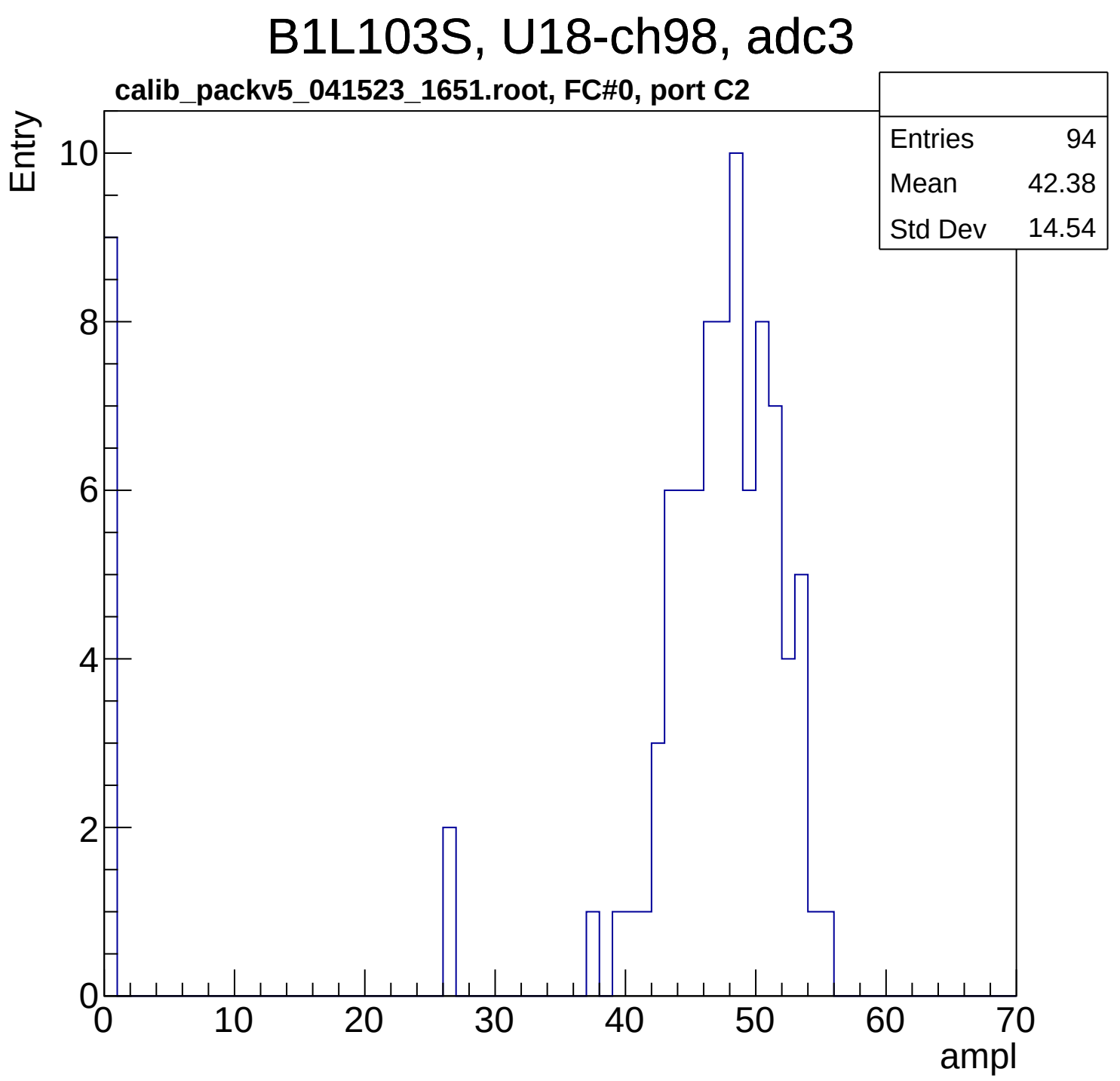
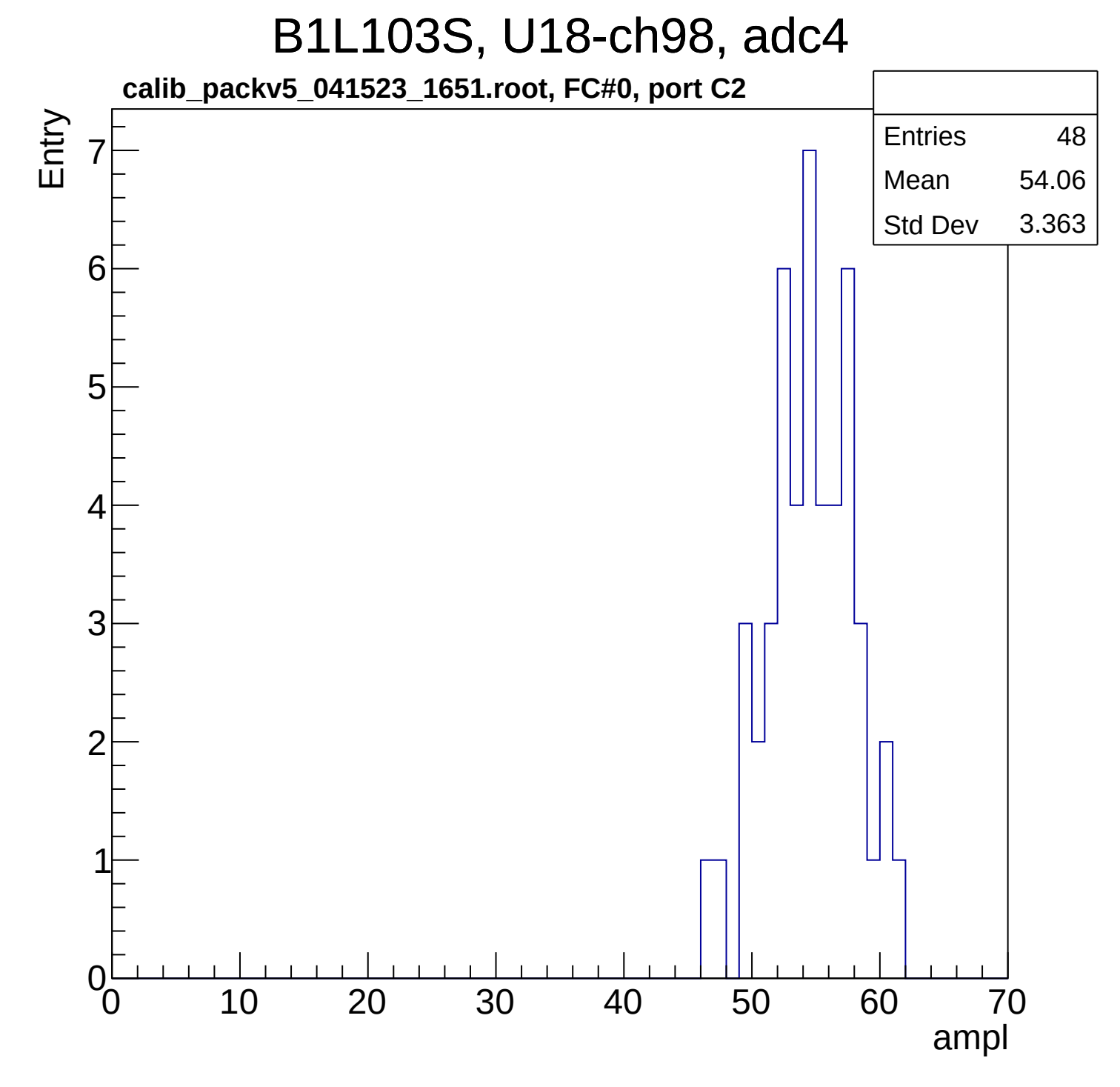
40
50
60
70


B1L103S, U18-ch98, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 94
Mean 42.38
Std Dev 14.54
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U18-ch98, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 54.06
Std Dev 3.363
Entry
ampl
0
1
2
3
4
5
6
7
0
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40
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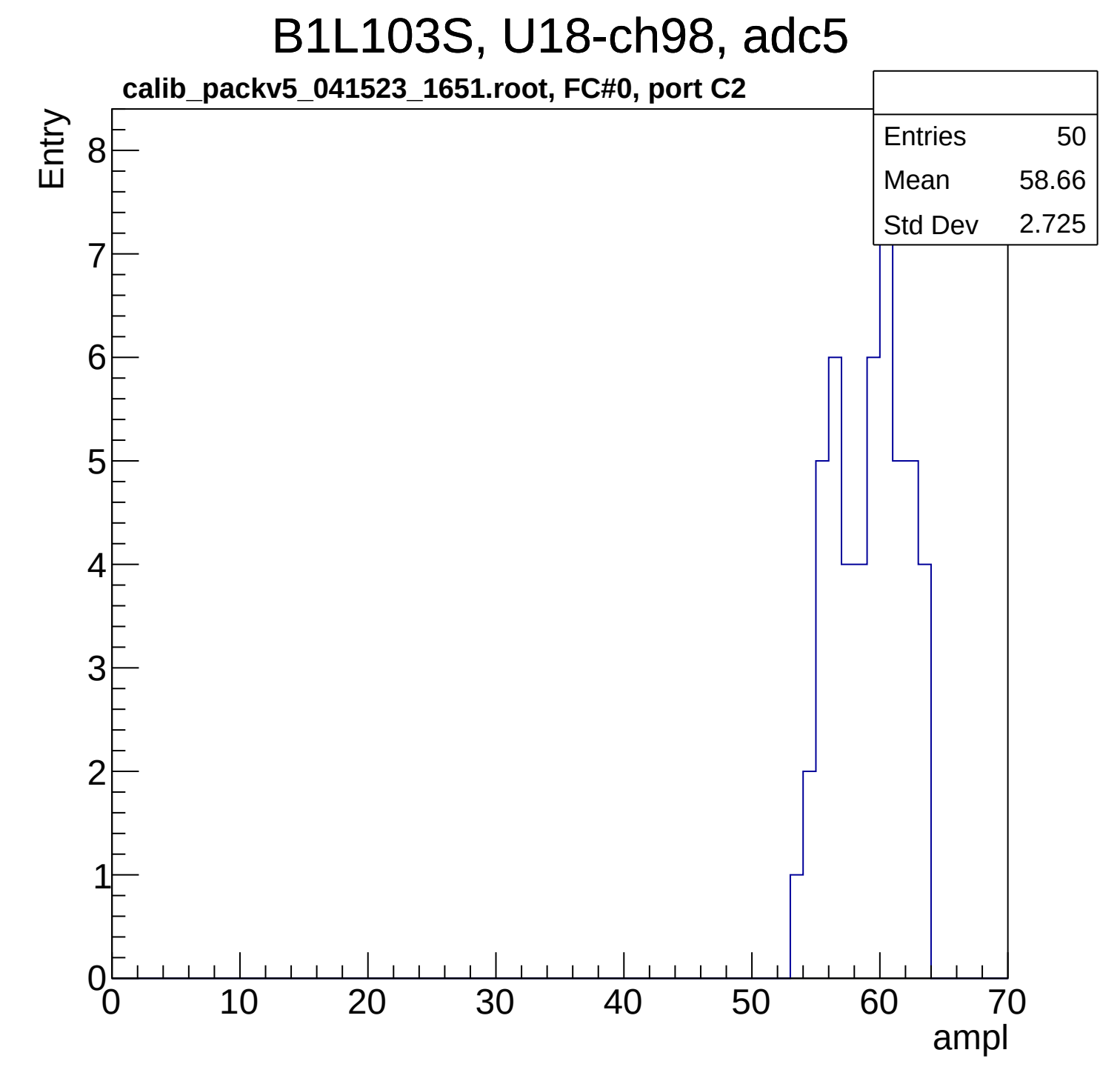
60
70


B1L103S, U18-ch98, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 58.66
Std Dev 2.725
Entry
ampl
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1
2
3
4
5
6
7
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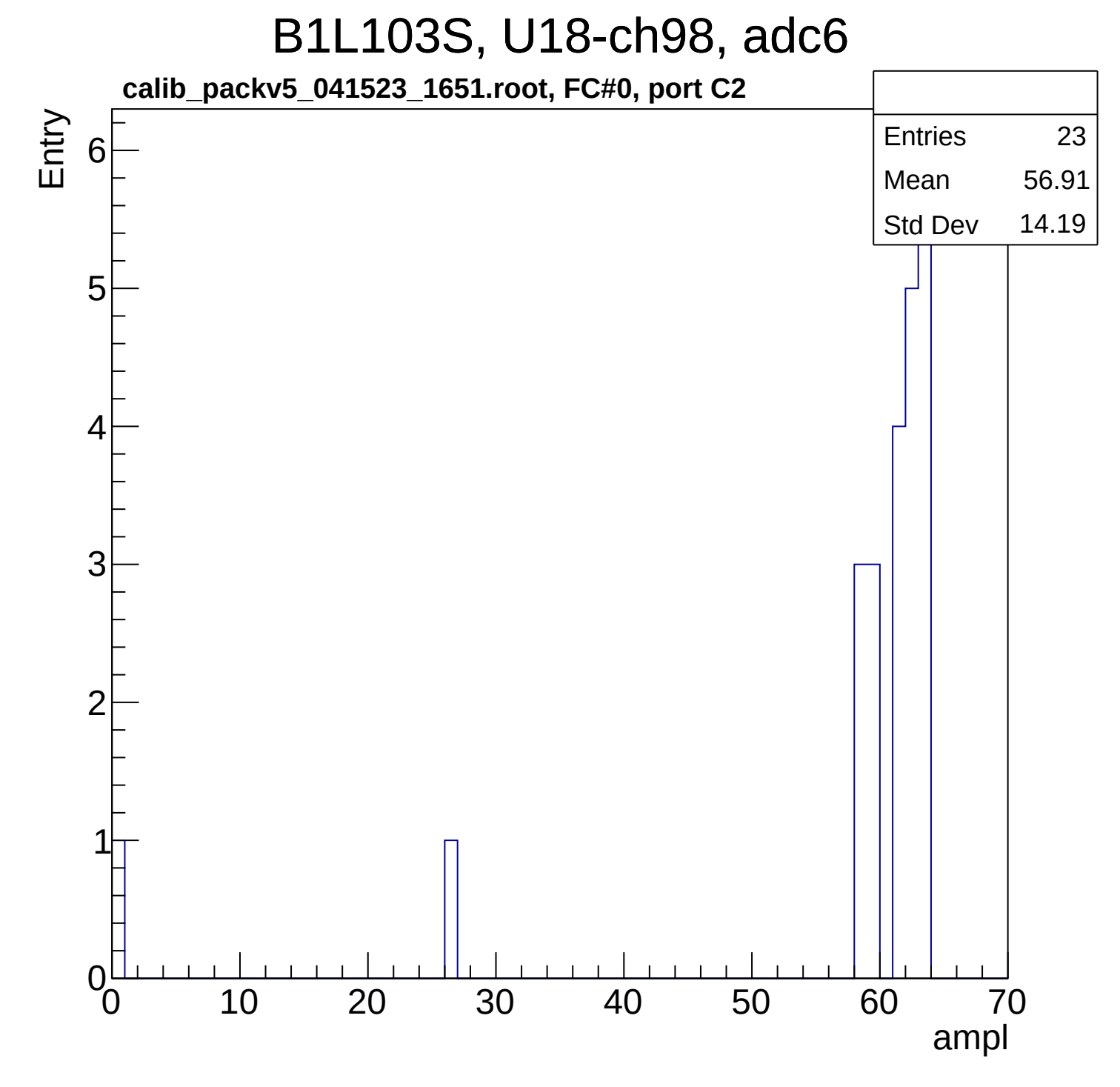
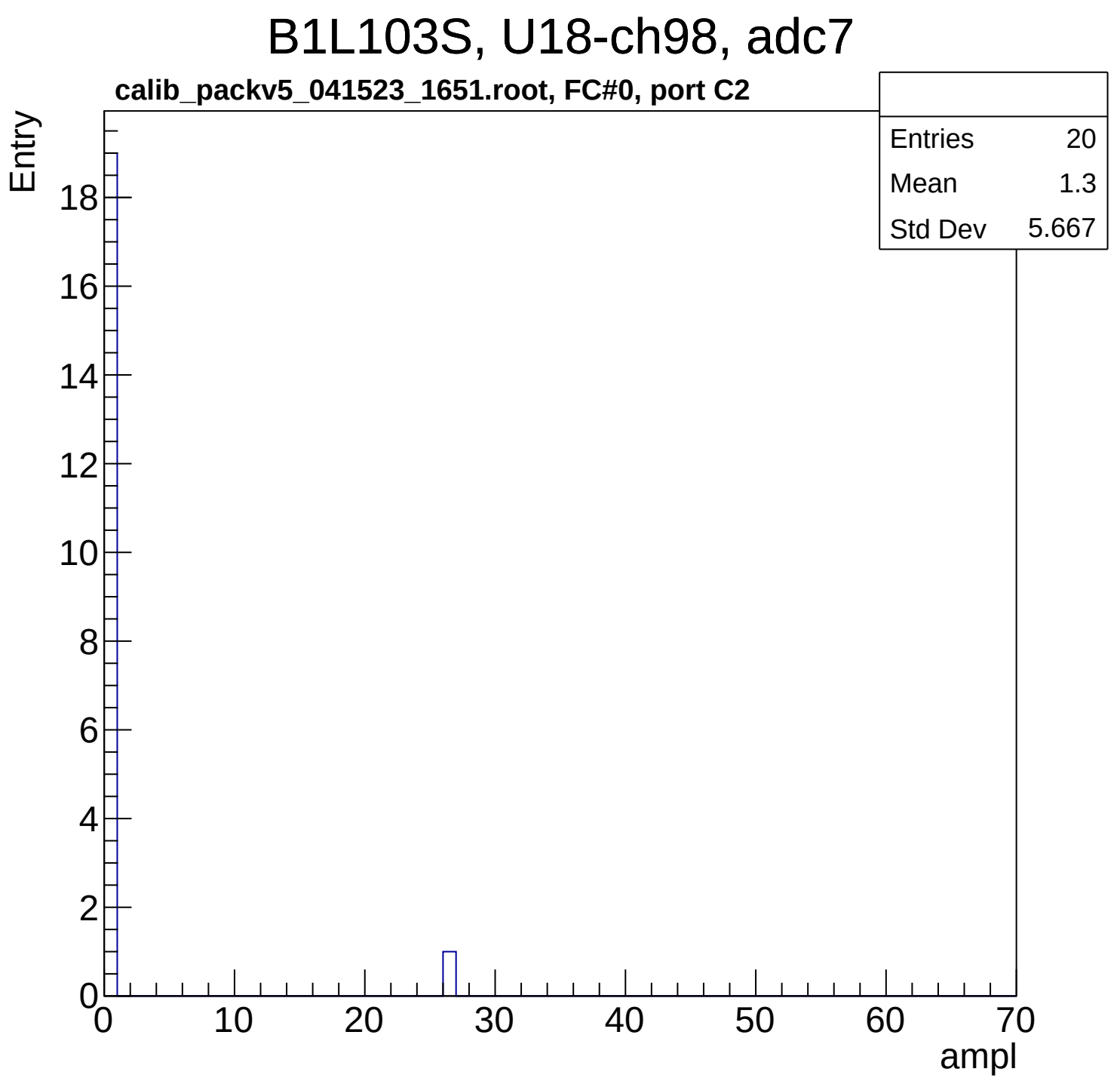
0
10
20
30
40
50
60
70


B1L103S, U18-ch98, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 23
Mean 56.91
Std Dev 14.19
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U18-ch98, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 1.3
Std Dev 5.667
Entry
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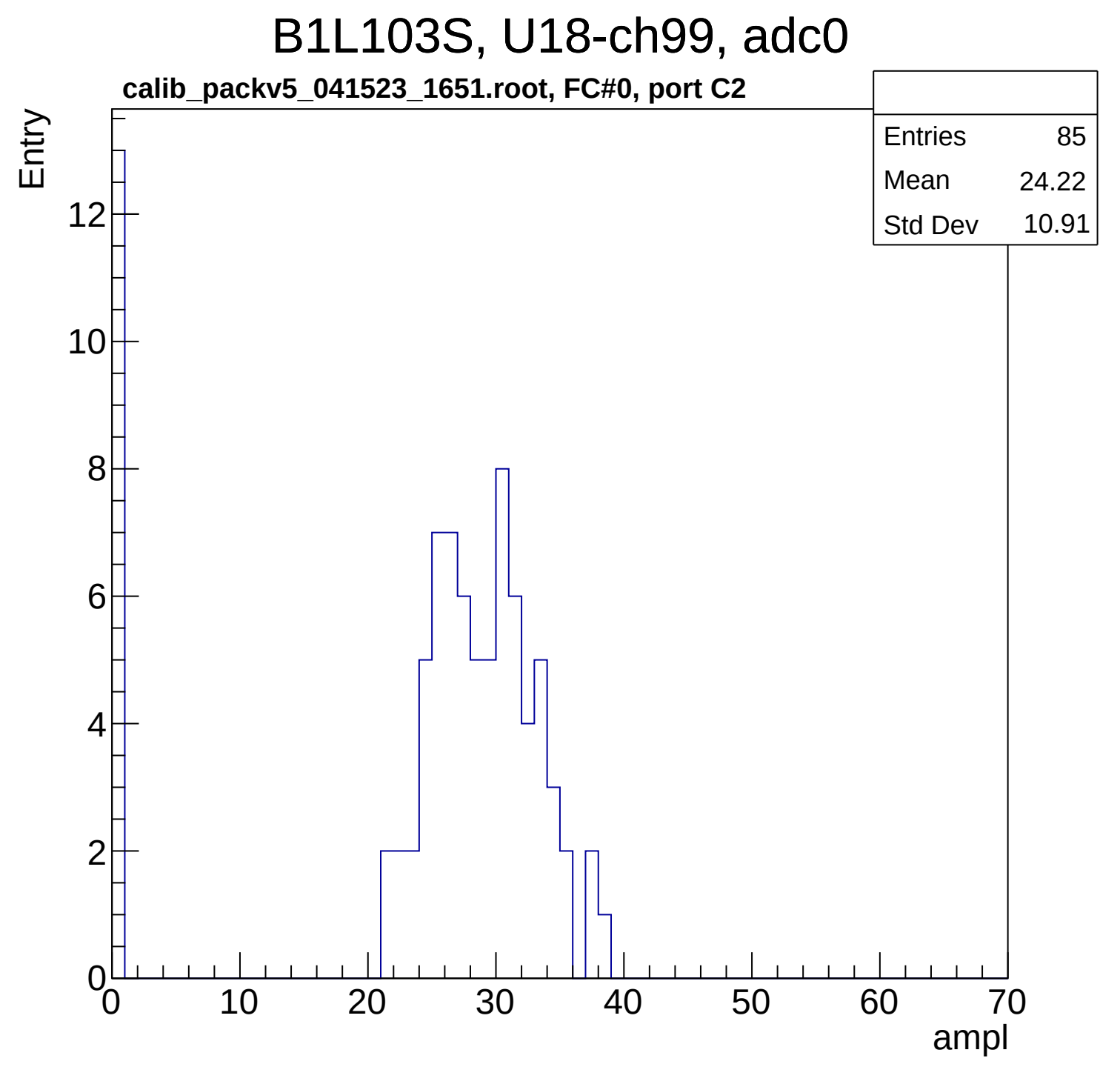
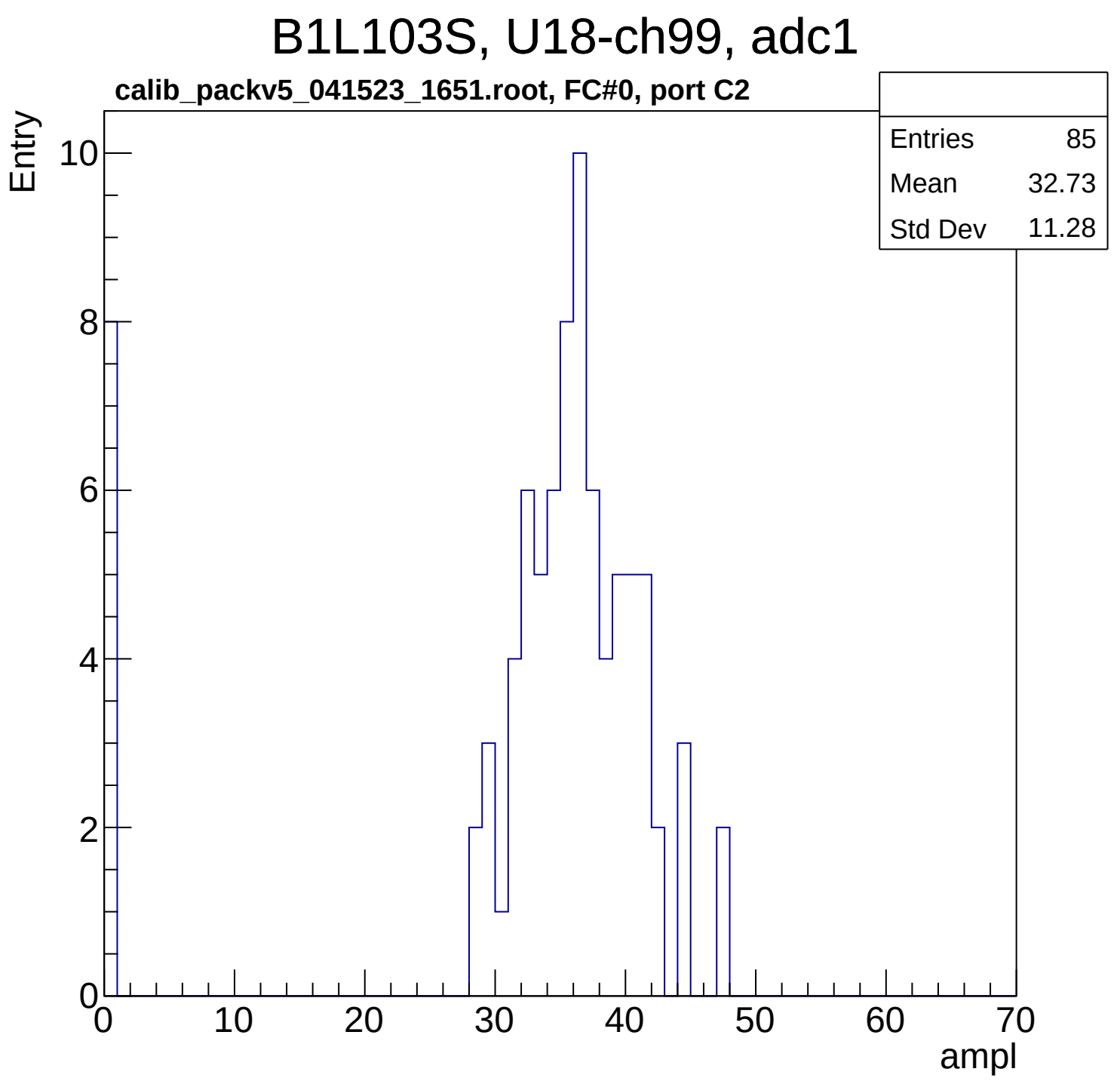
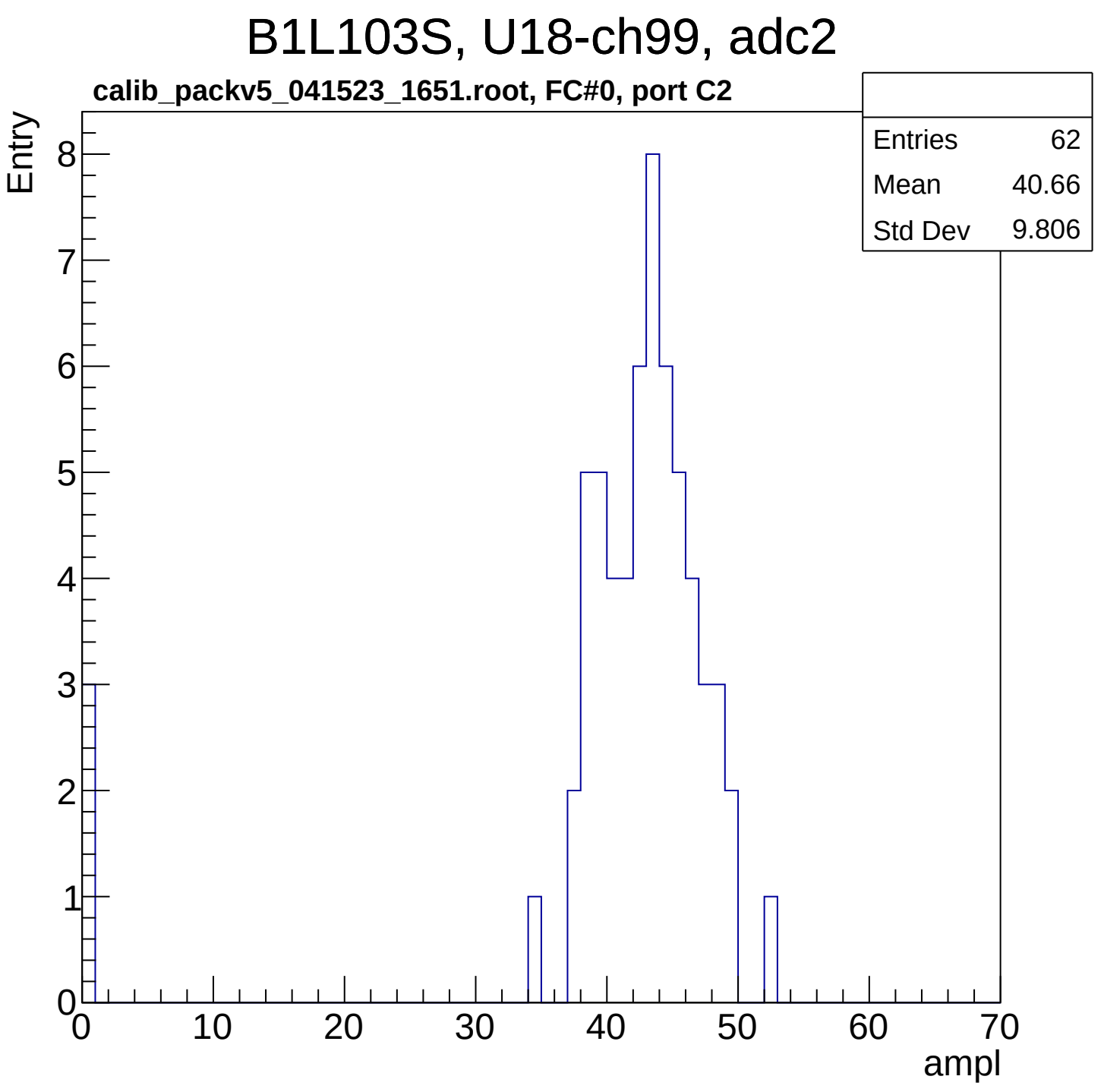
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch99, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 24.22
Std Dev 10.91
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch99, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 32.73
Std Dev 11.28
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U18-ch99, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 40.66
Std Dev 9.806
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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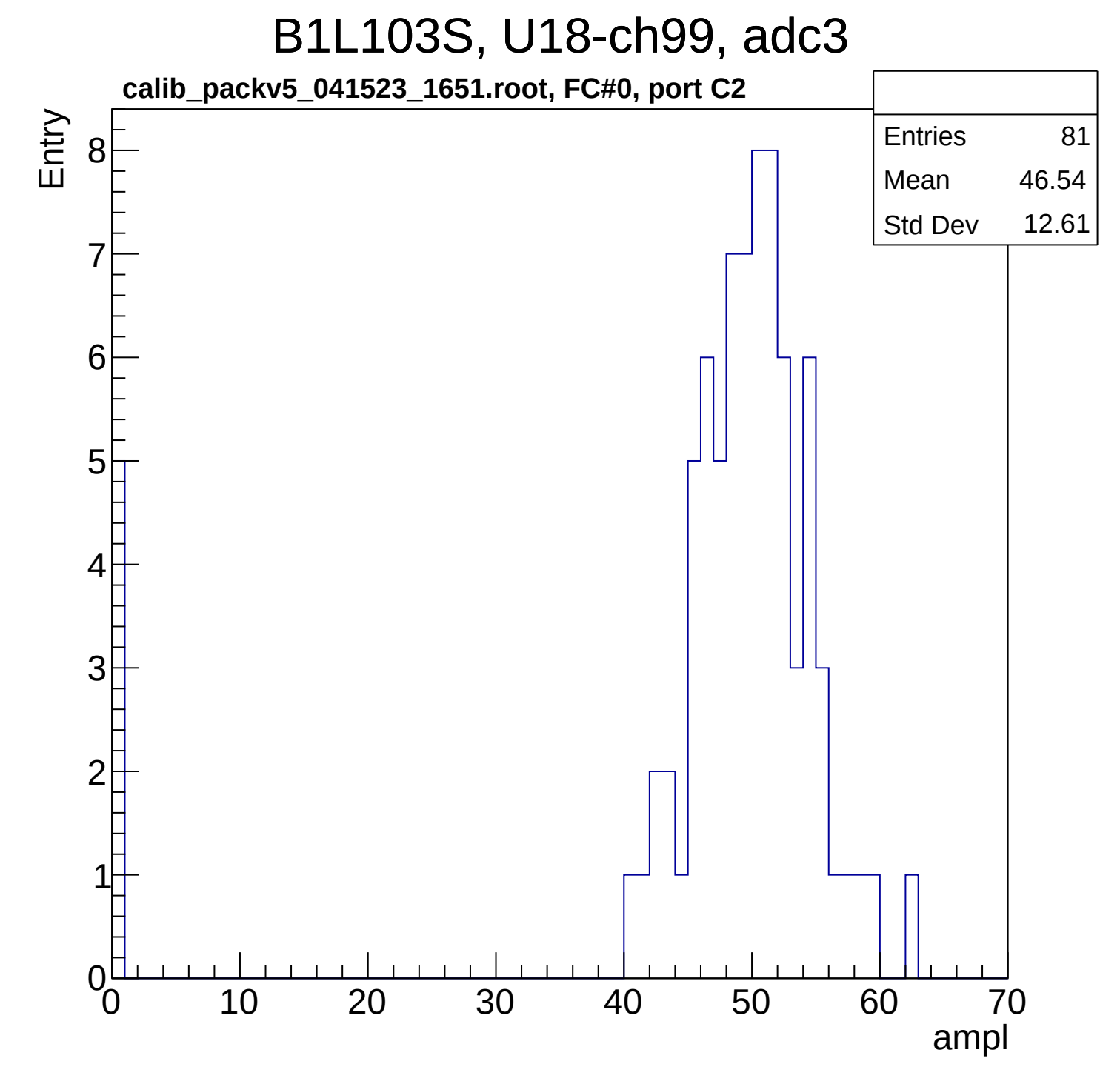
B1L103S, U18-ch99, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 46.54
Std Dev 12.61
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
30
40
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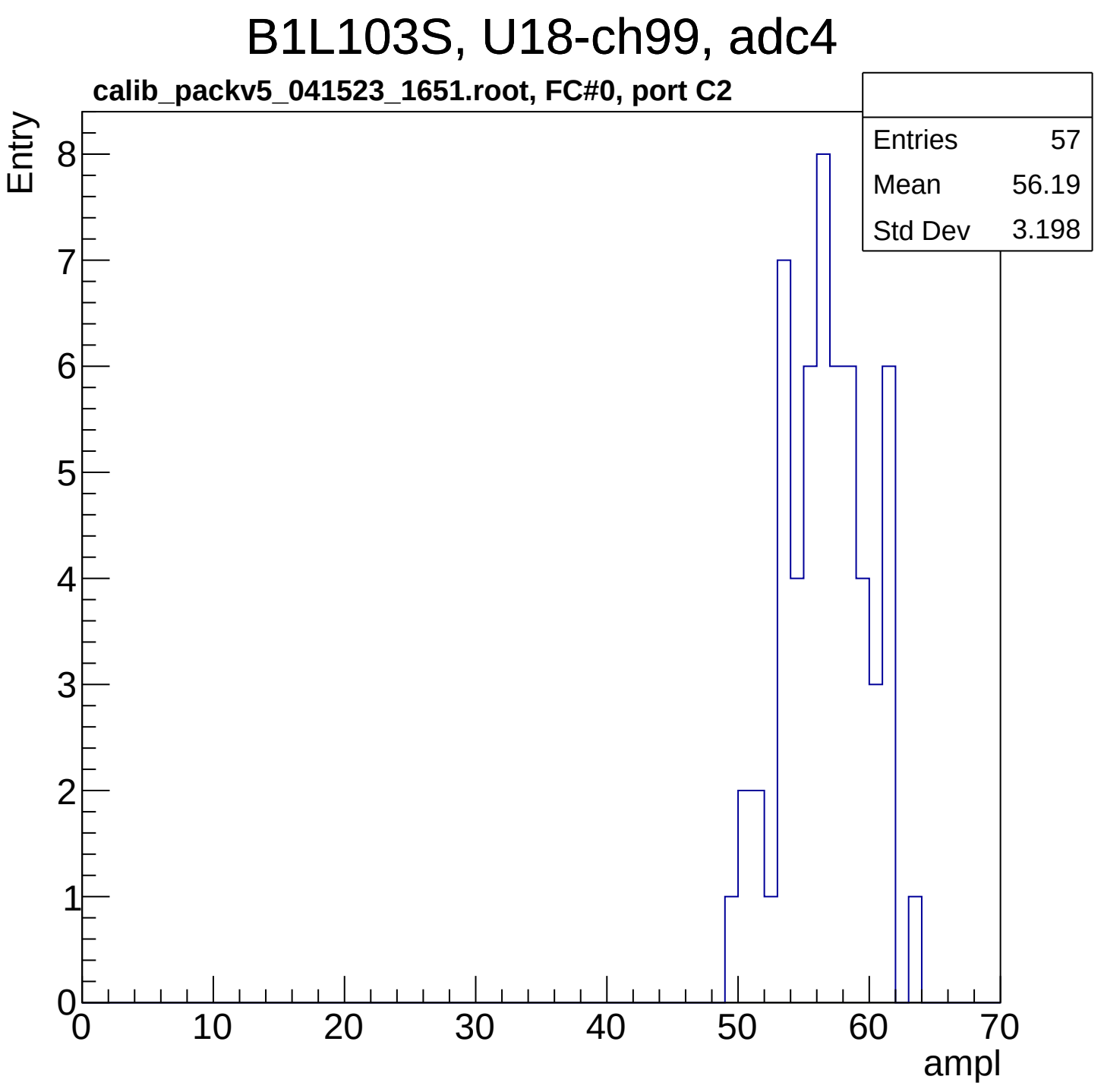
60
70


B1L103S, U18-ch99, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 56.19
Std Dev 3.198
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
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60
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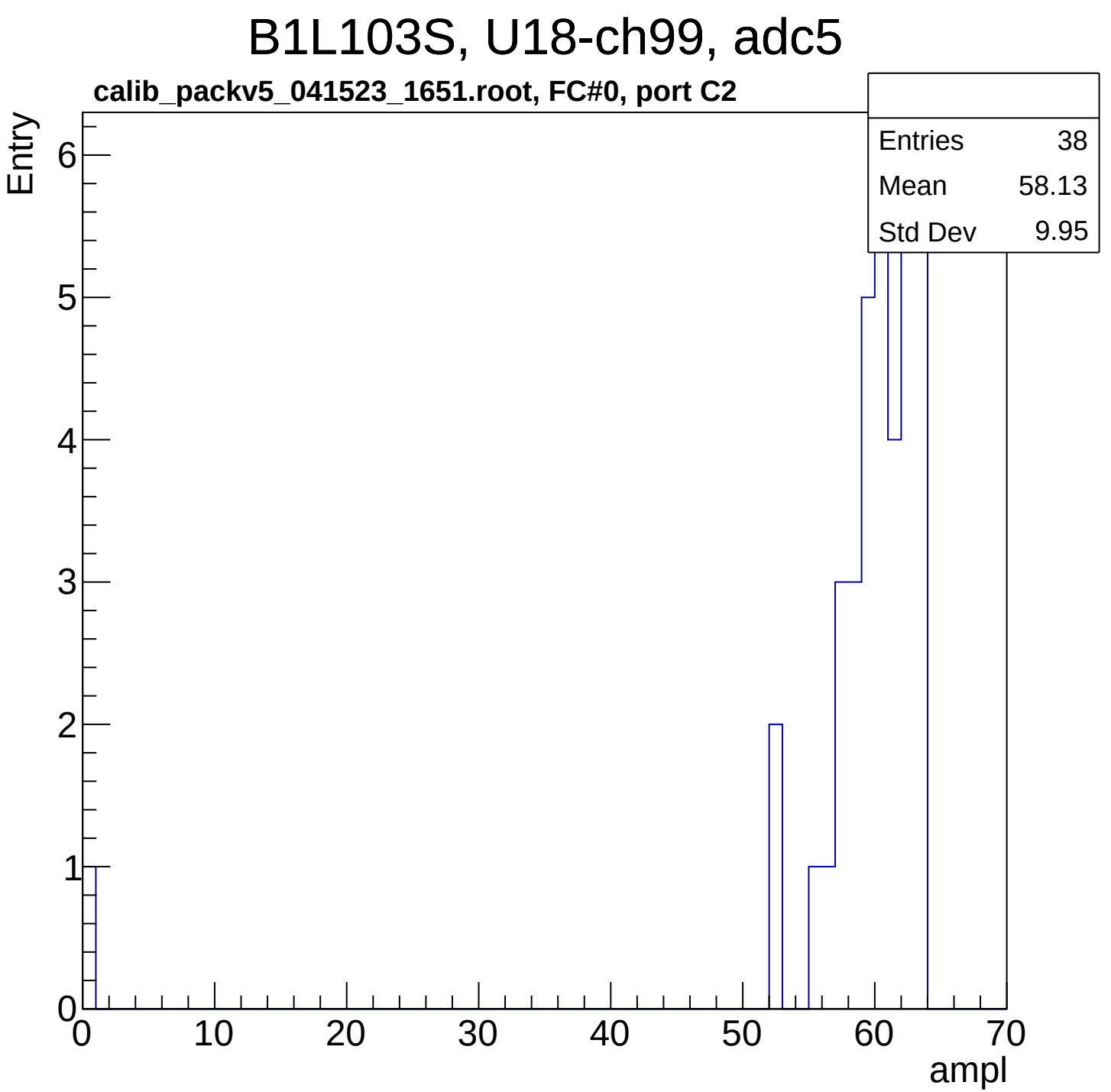
B1L103S, U18-ch99, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 38
Mean 58.13
Std Dev 9.95
Entry
ampl
0
1
2
3
4
5
6
0
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20
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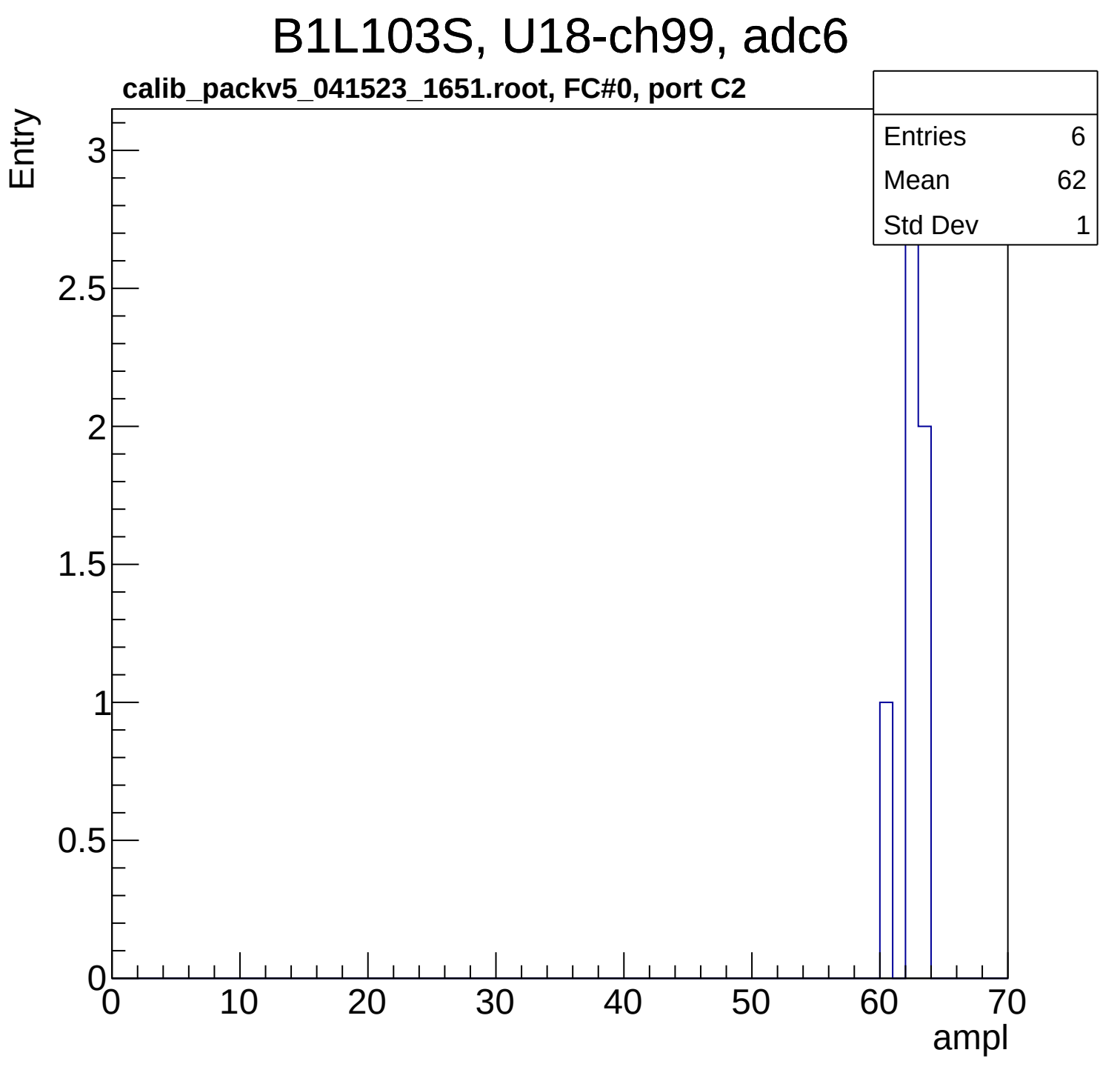
40
50
60
70


B1L103S, U18-ch99, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 62
Std Dev 1
Entry
ampl
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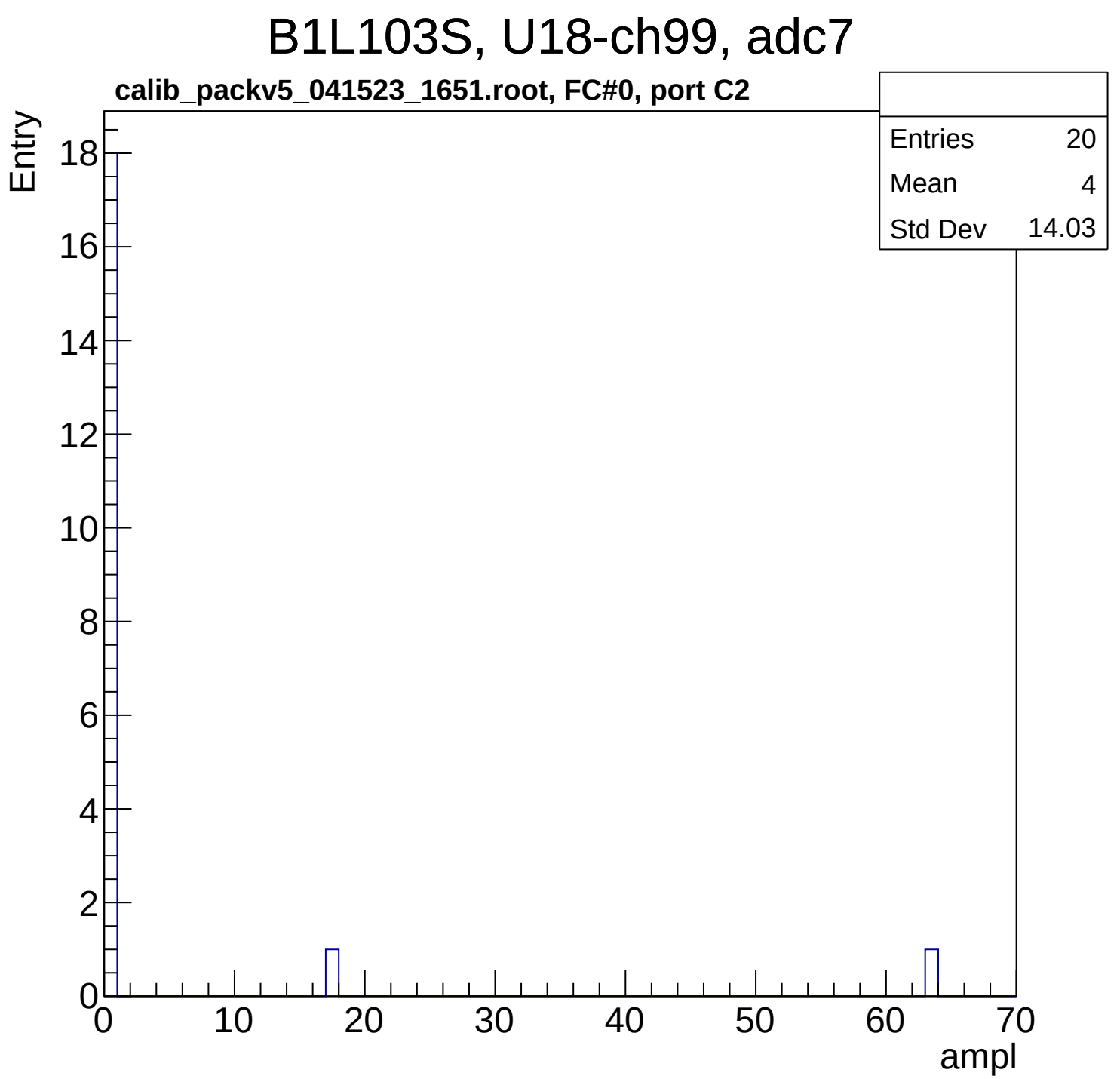
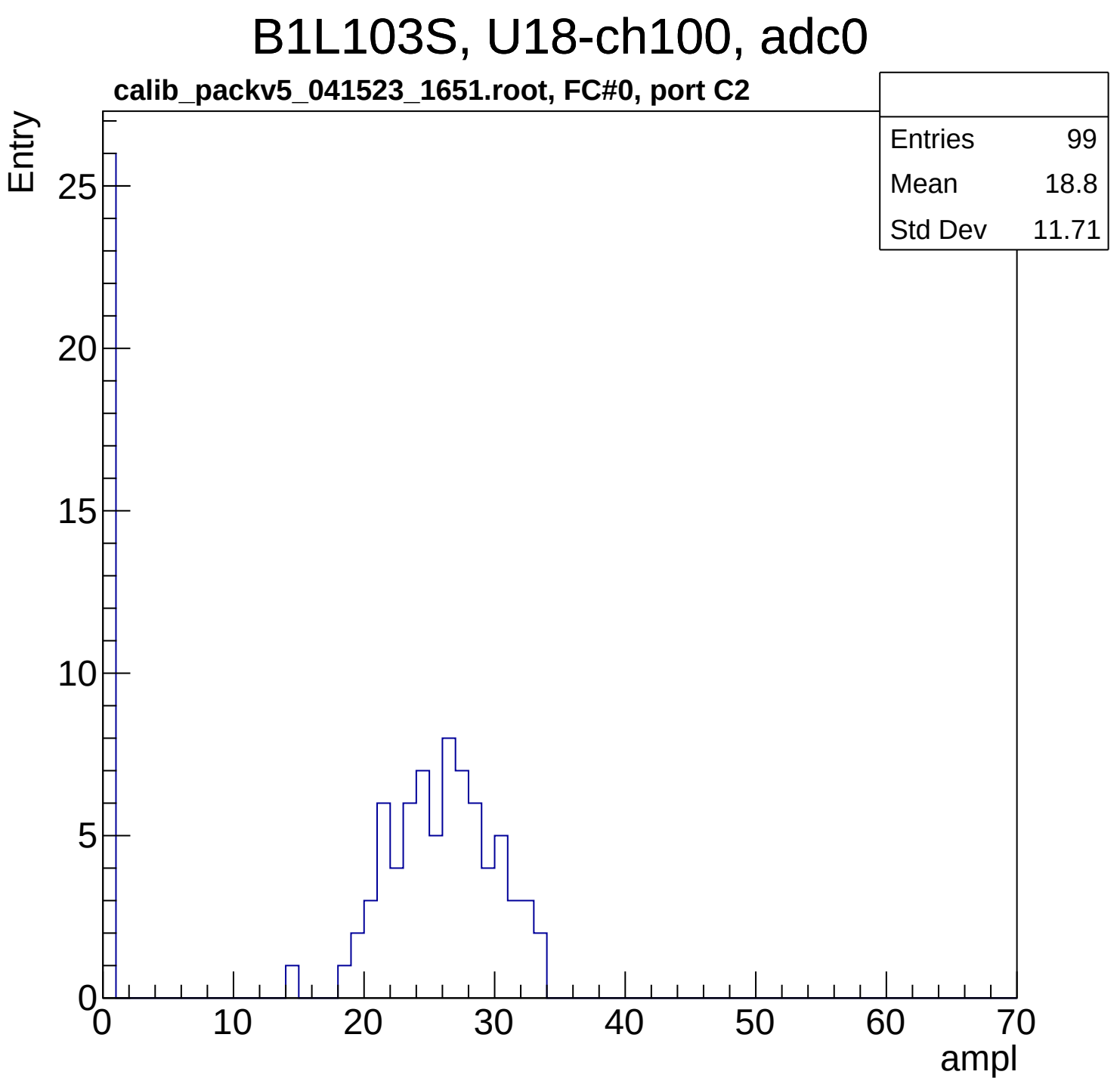
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U18-ch99, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 4
Std Dev 14.03
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch100, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 99
Mean 18.8
Std Dev 11.71
Entry
0
5
10
15
20
25
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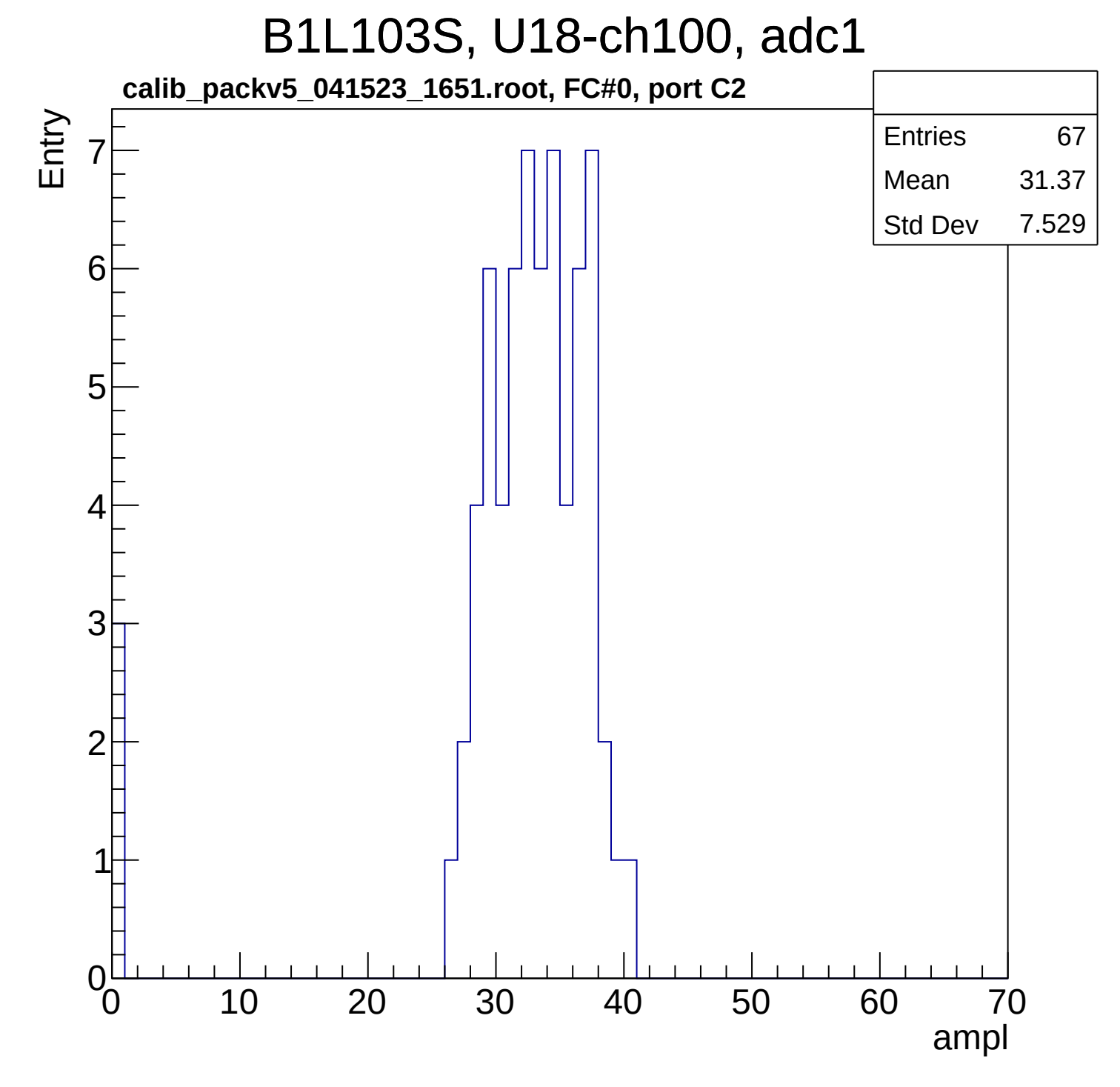
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch100, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 31.37
Std Dev 7.529
Entry
ampl
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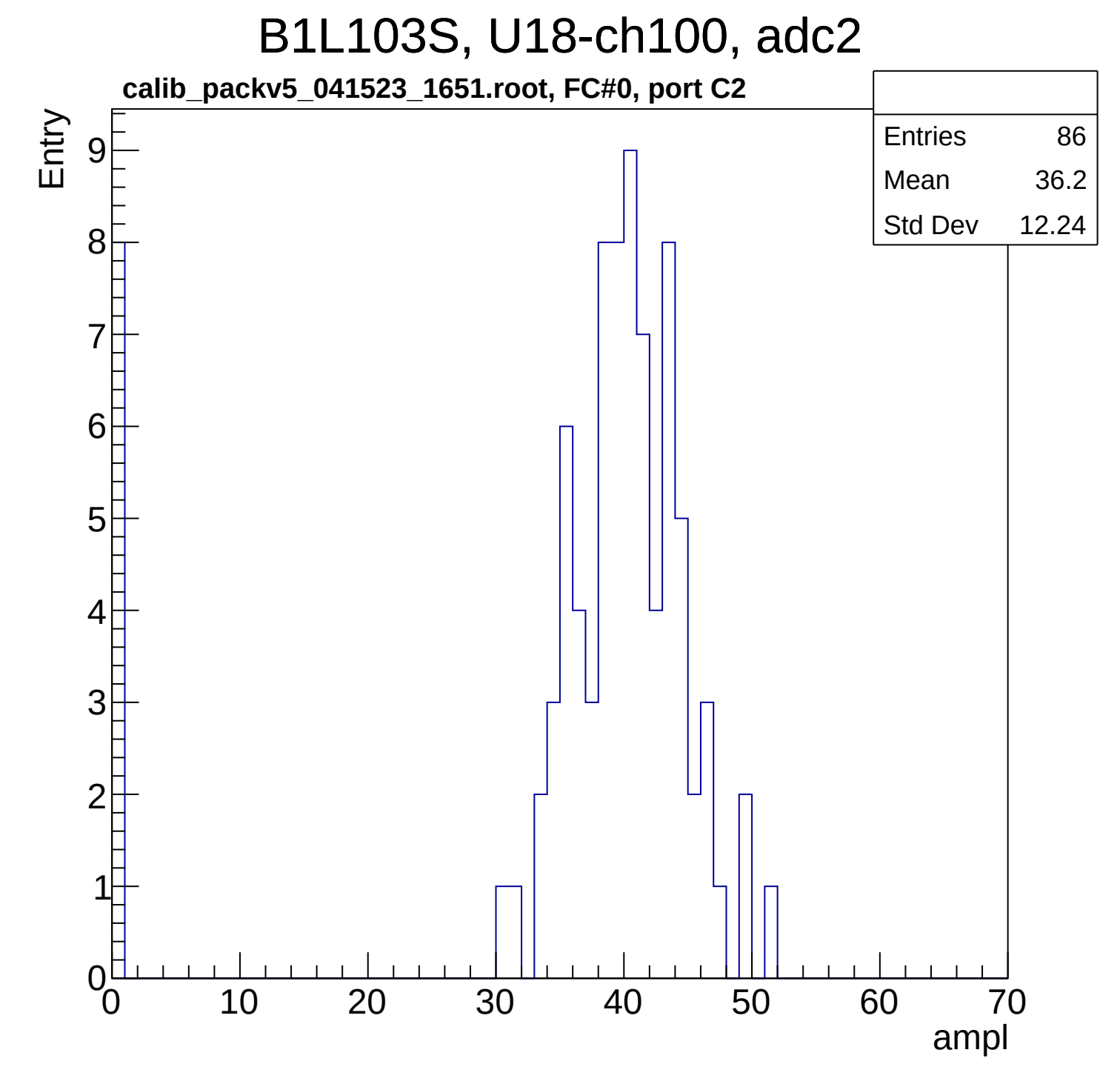
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U18-ch100, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 36.2
Std Dev 12.24
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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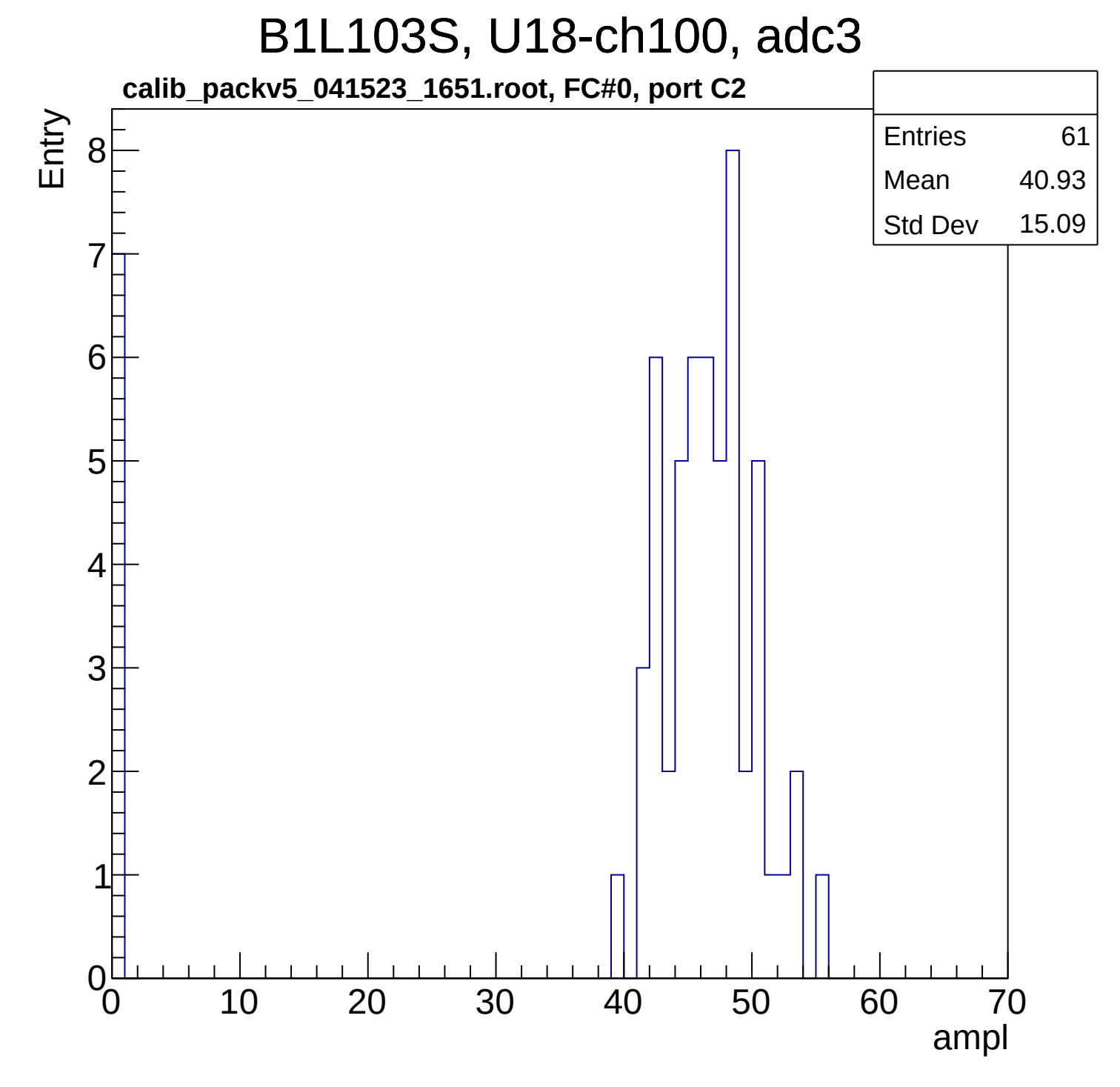
B1L103S, U18-ch100, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 40.93
Std Dev 15.09
Entry
ampl
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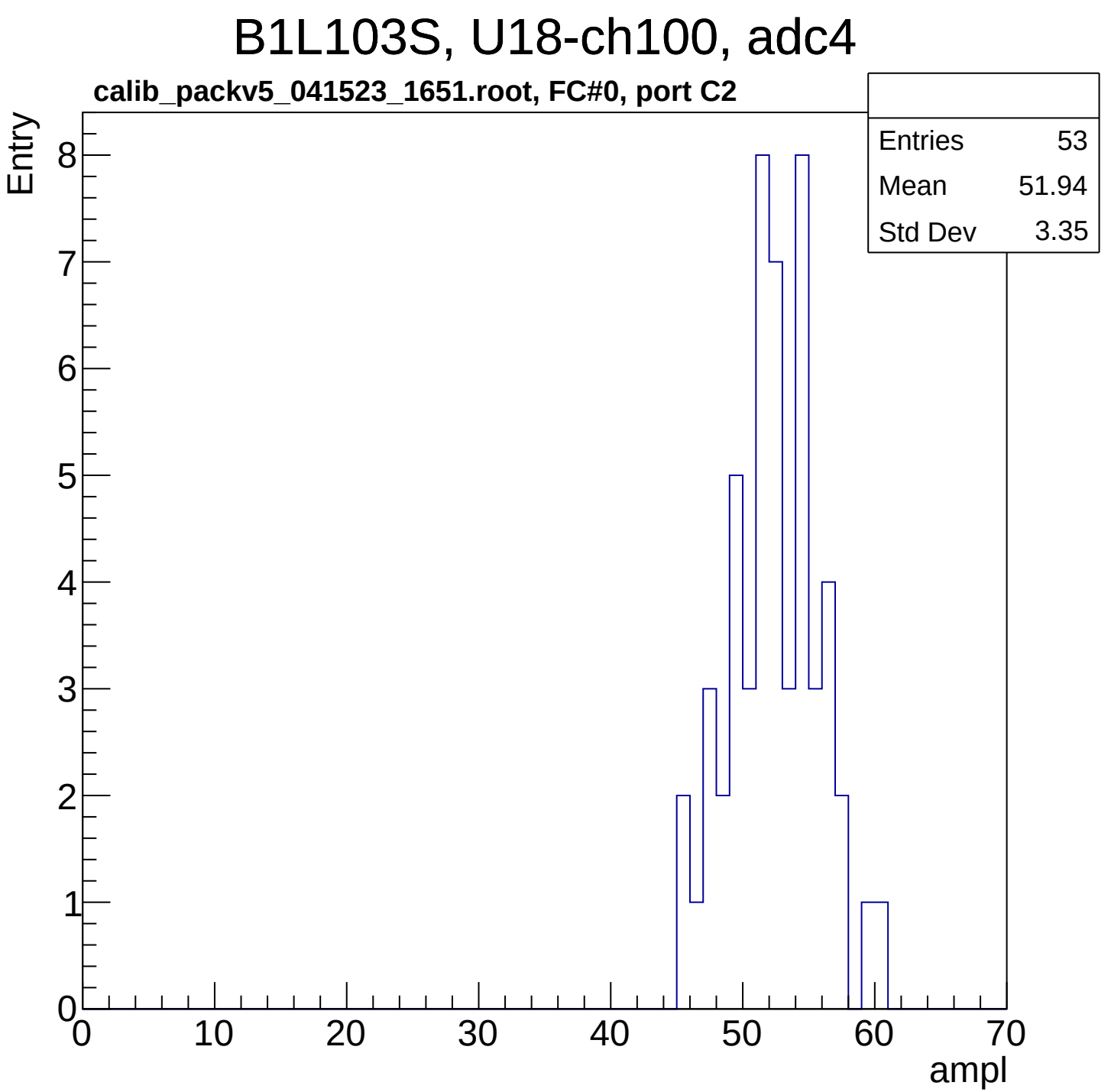
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch100, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 51.94
Std Dev 3.35
Entry
ampl
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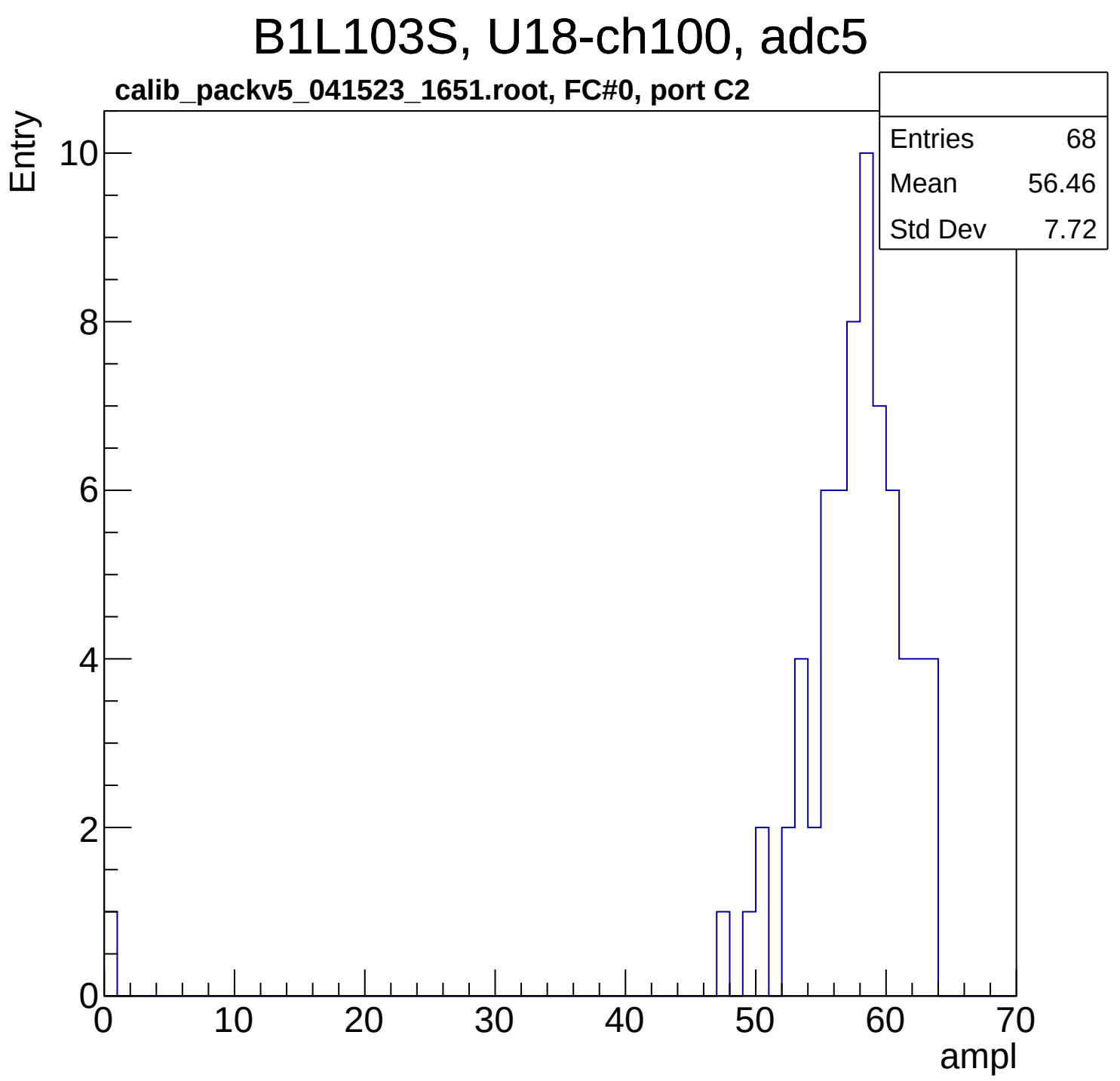
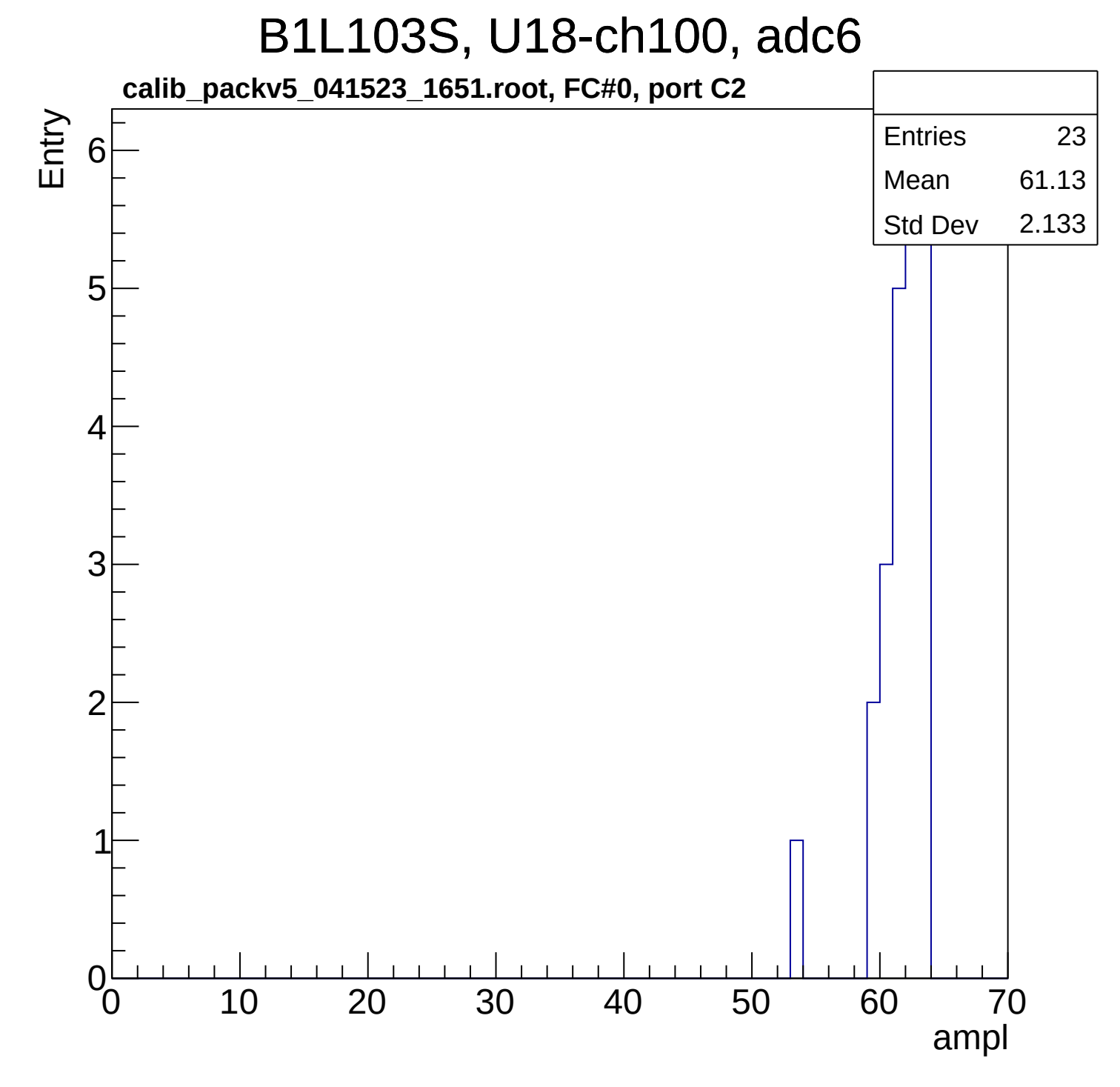
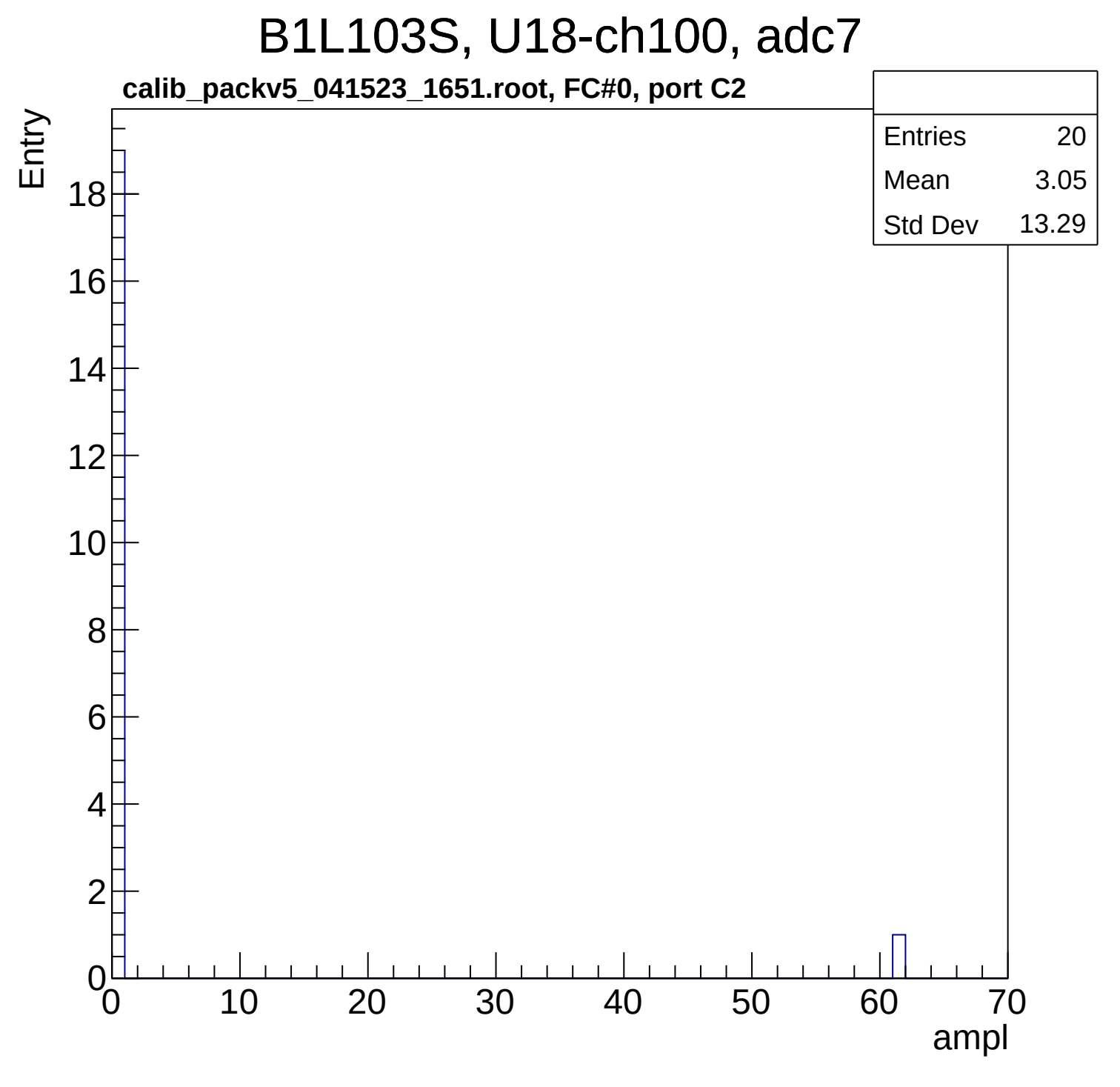
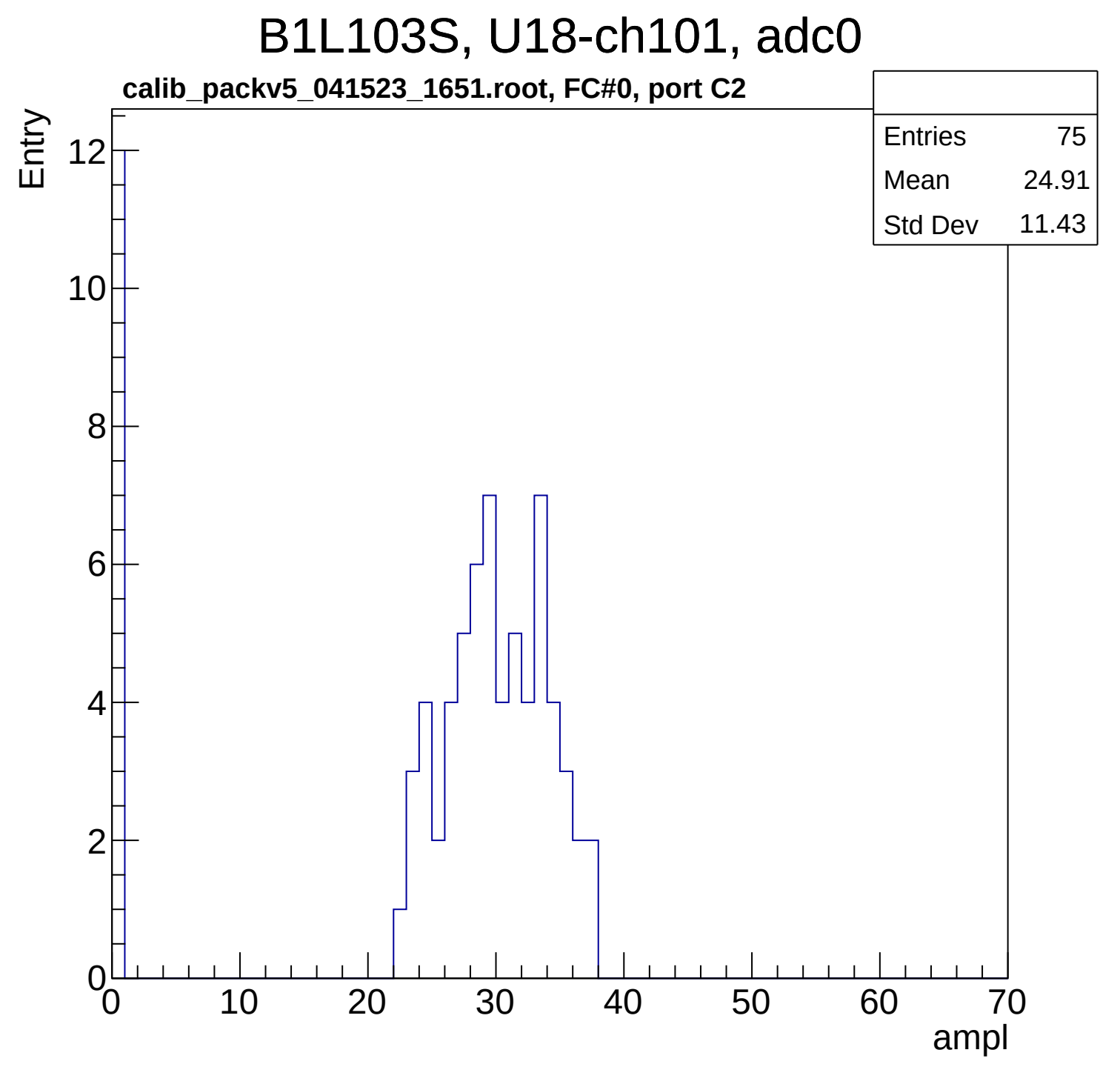
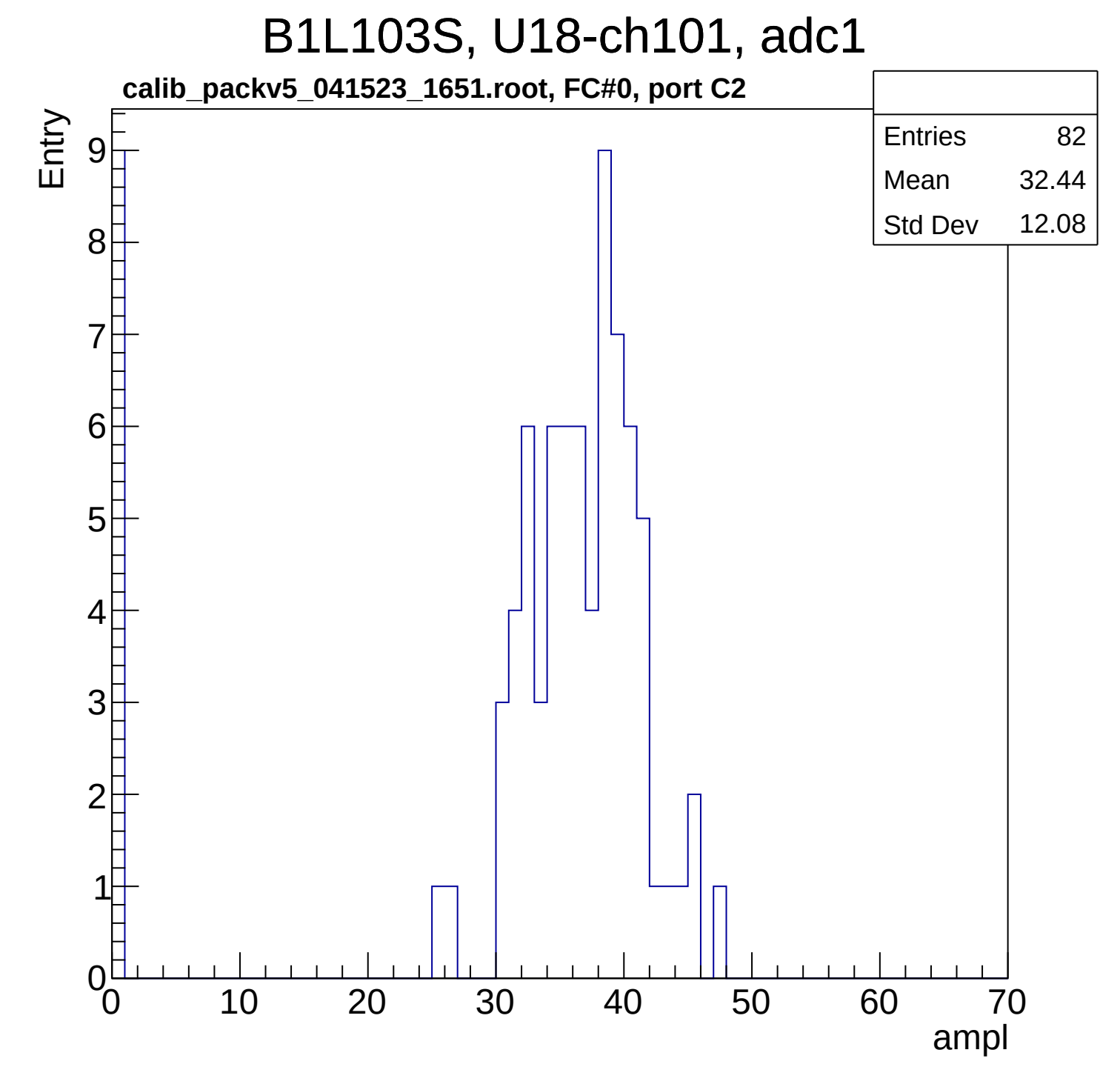
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

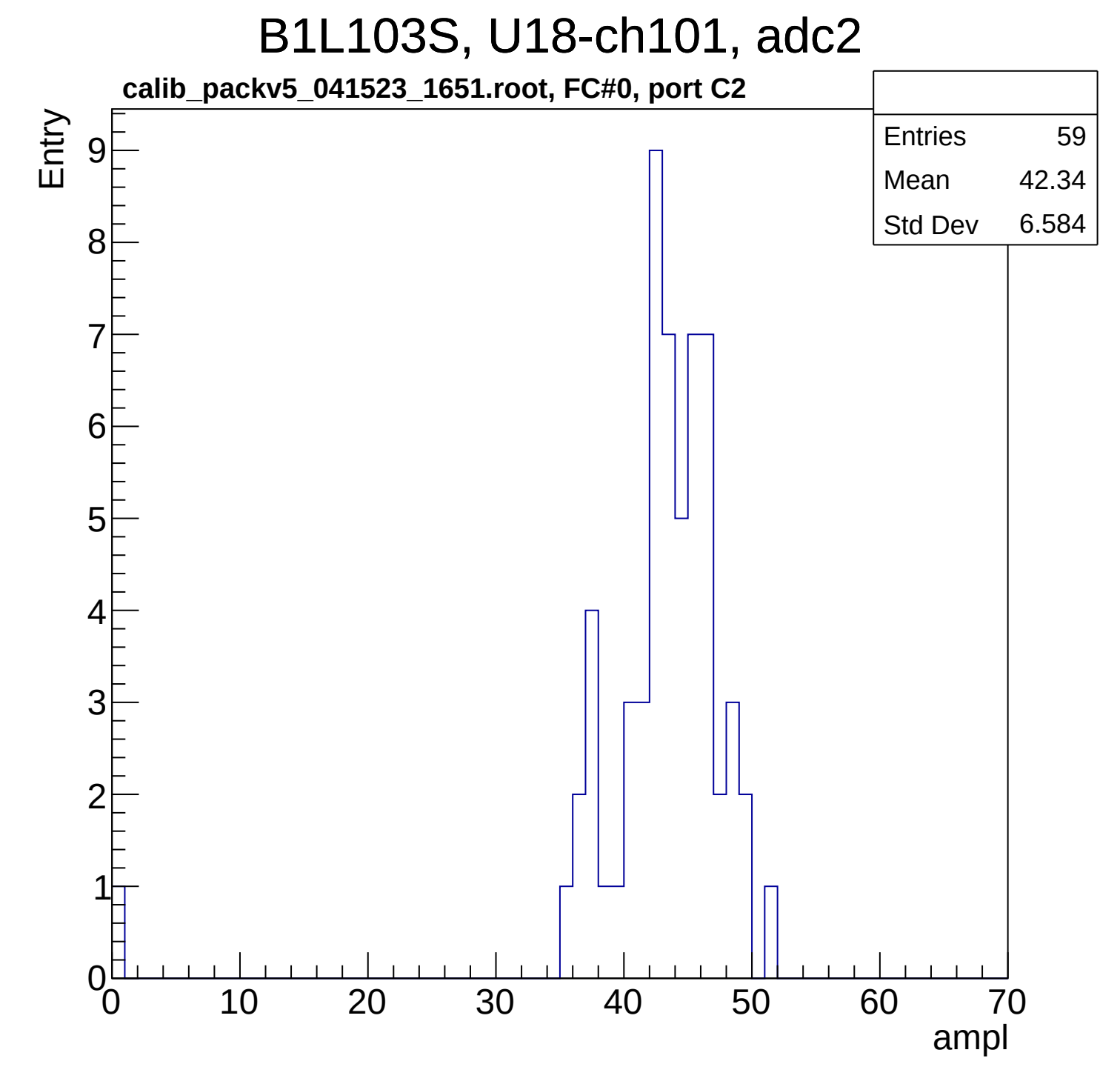

B1L103S, U18-ch100, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 56.46
Std Dev 7.72
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

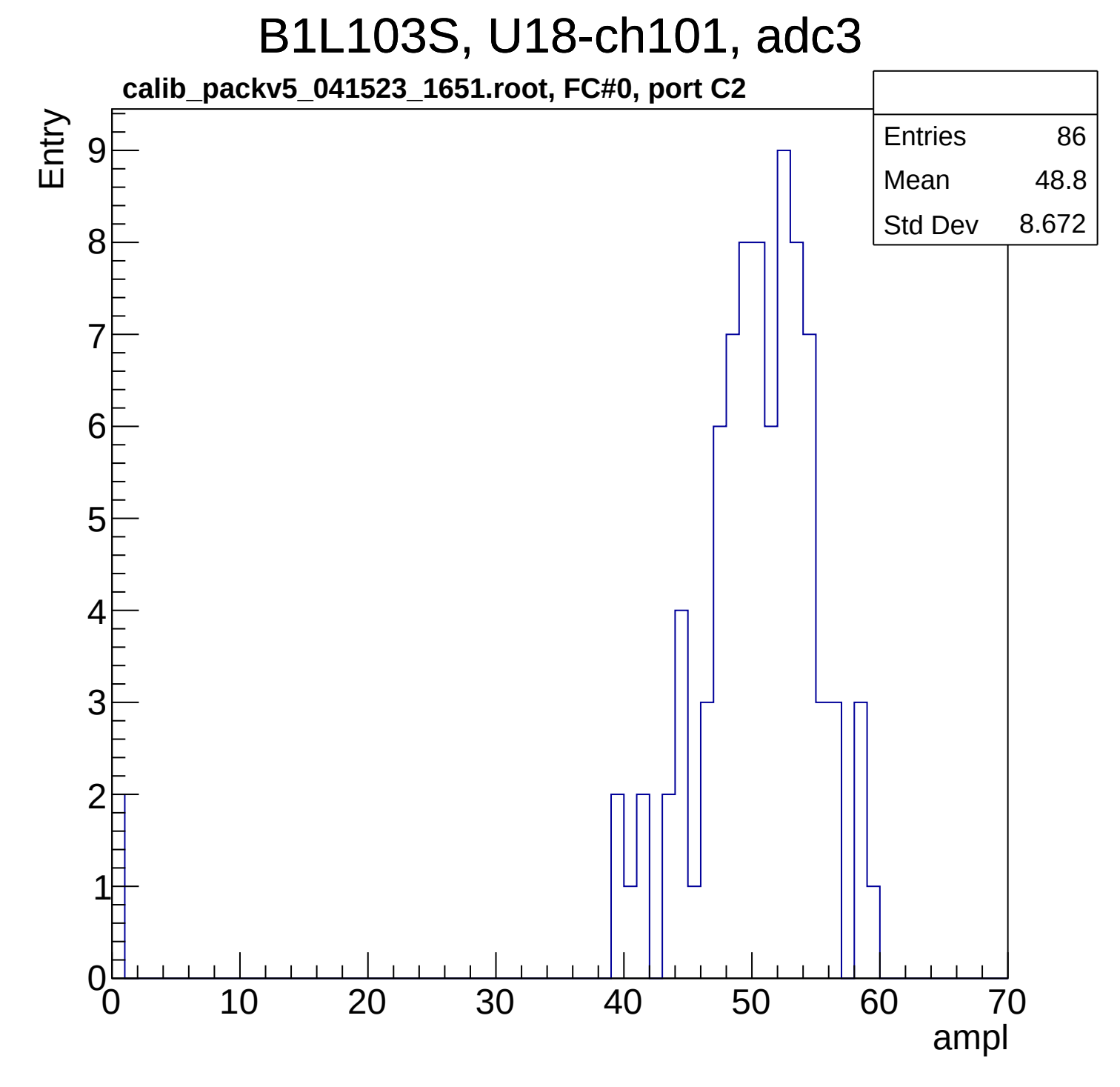

B1L103S, U18-ch100, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 23
Mean 61.13
Std Dev 2.133
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

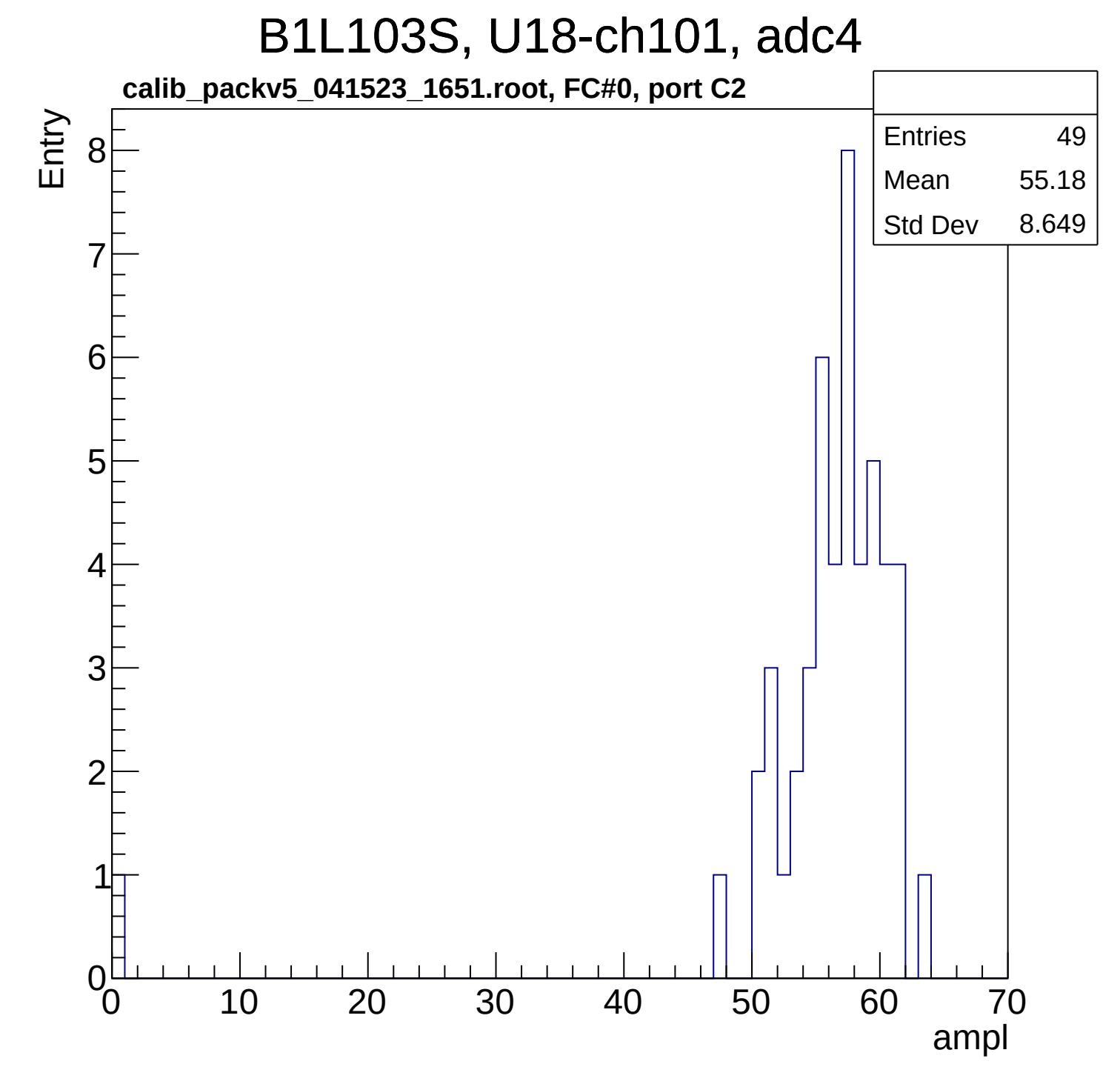

B1L103S, U18-ch100, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.05
Std Dev 13.29
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch101, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 24.91
Std Dev 11.43
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70


B1L103S, U18-ch101, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 32.44
Std Dev 12.08
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U18-ch101, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 42.34
Std Dev 6.584
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U18-ch101, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 48.8
Std Dev 8.672
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U18-ch101, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 55.18
Std Dev 8.649
Entry
ampl
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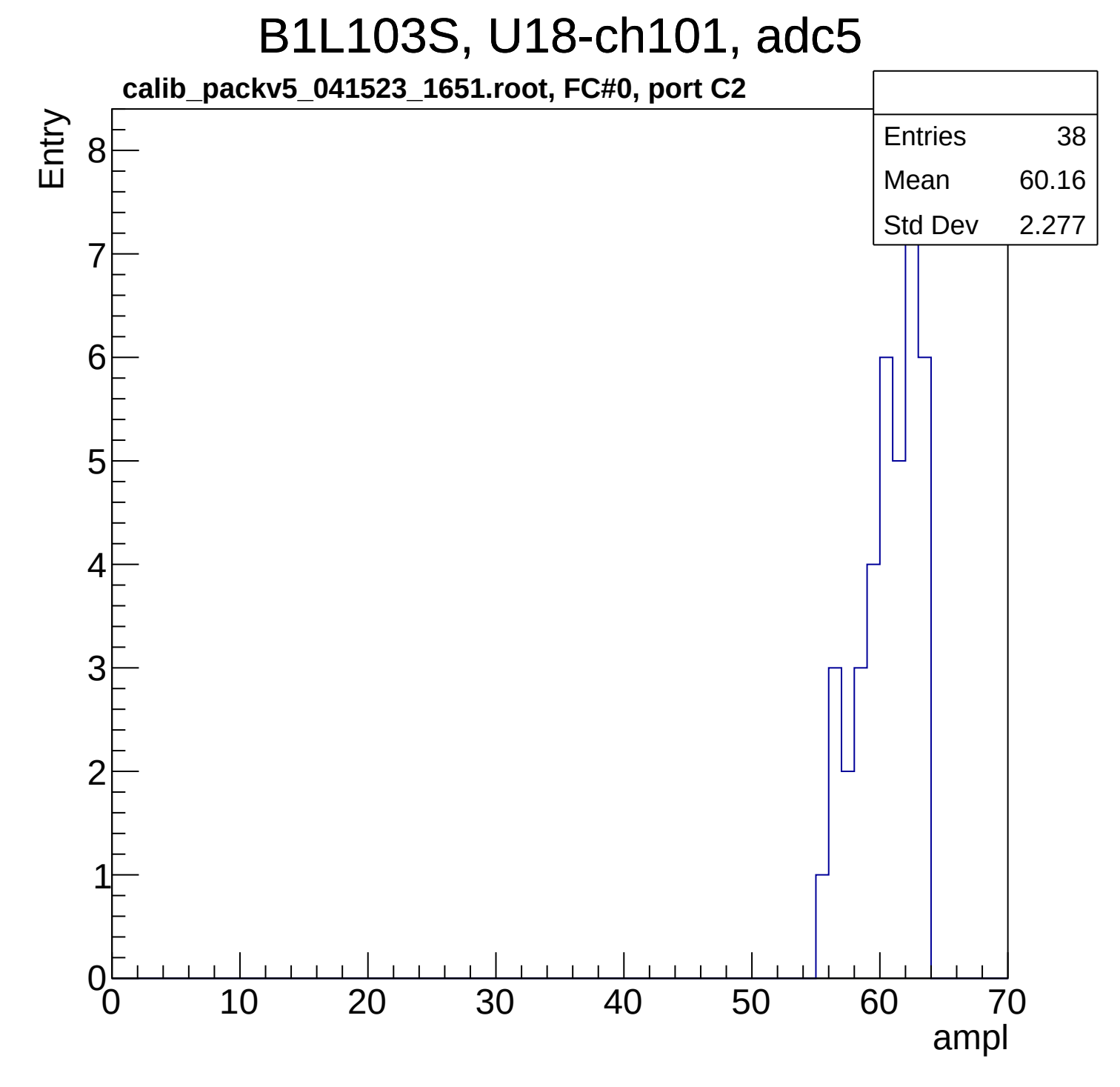
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch101, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 38
Mean 60.16
Std Dev 2.277
Entry
ampl
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1
2
3
4
5
6
7
8
0
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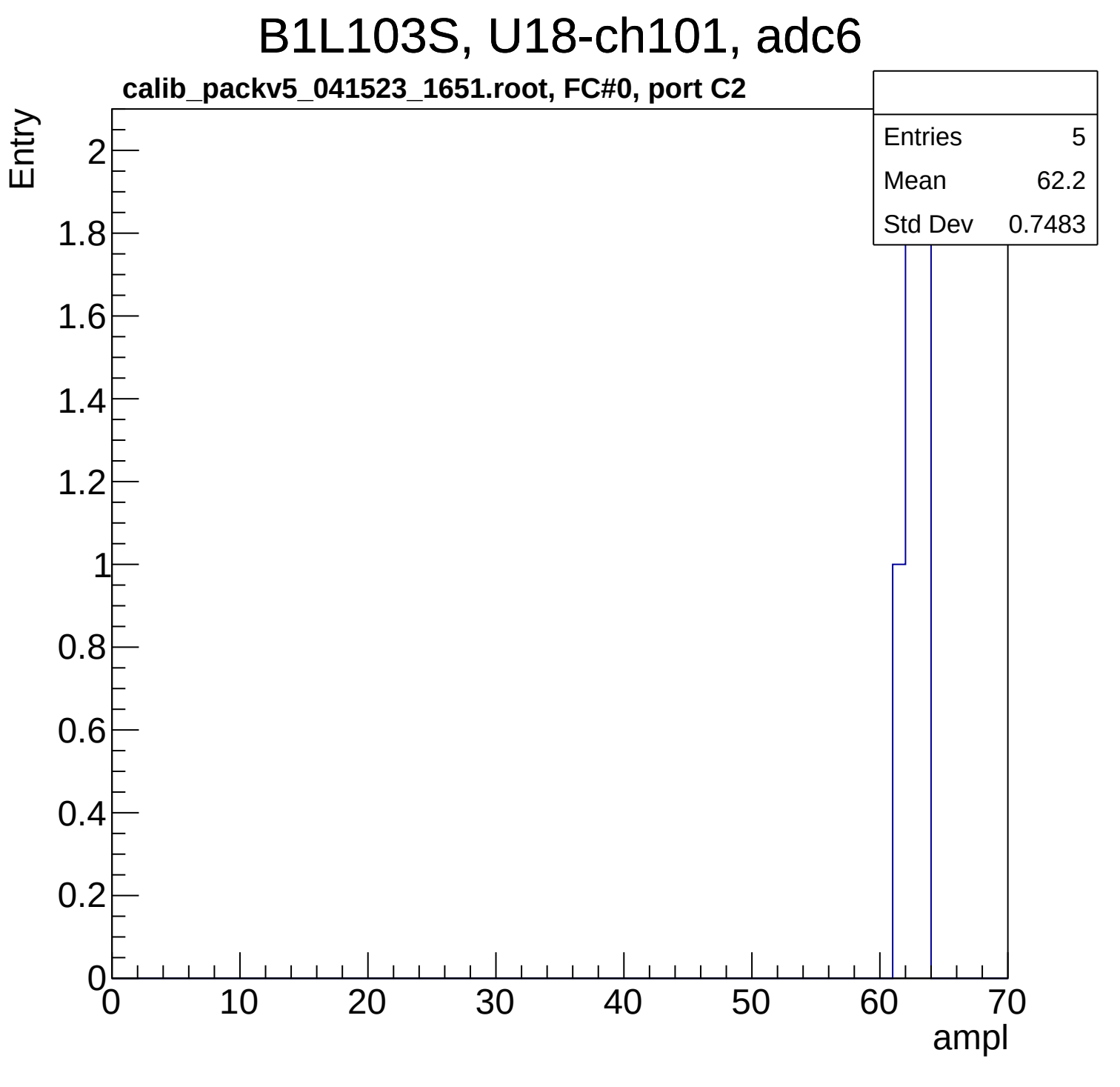
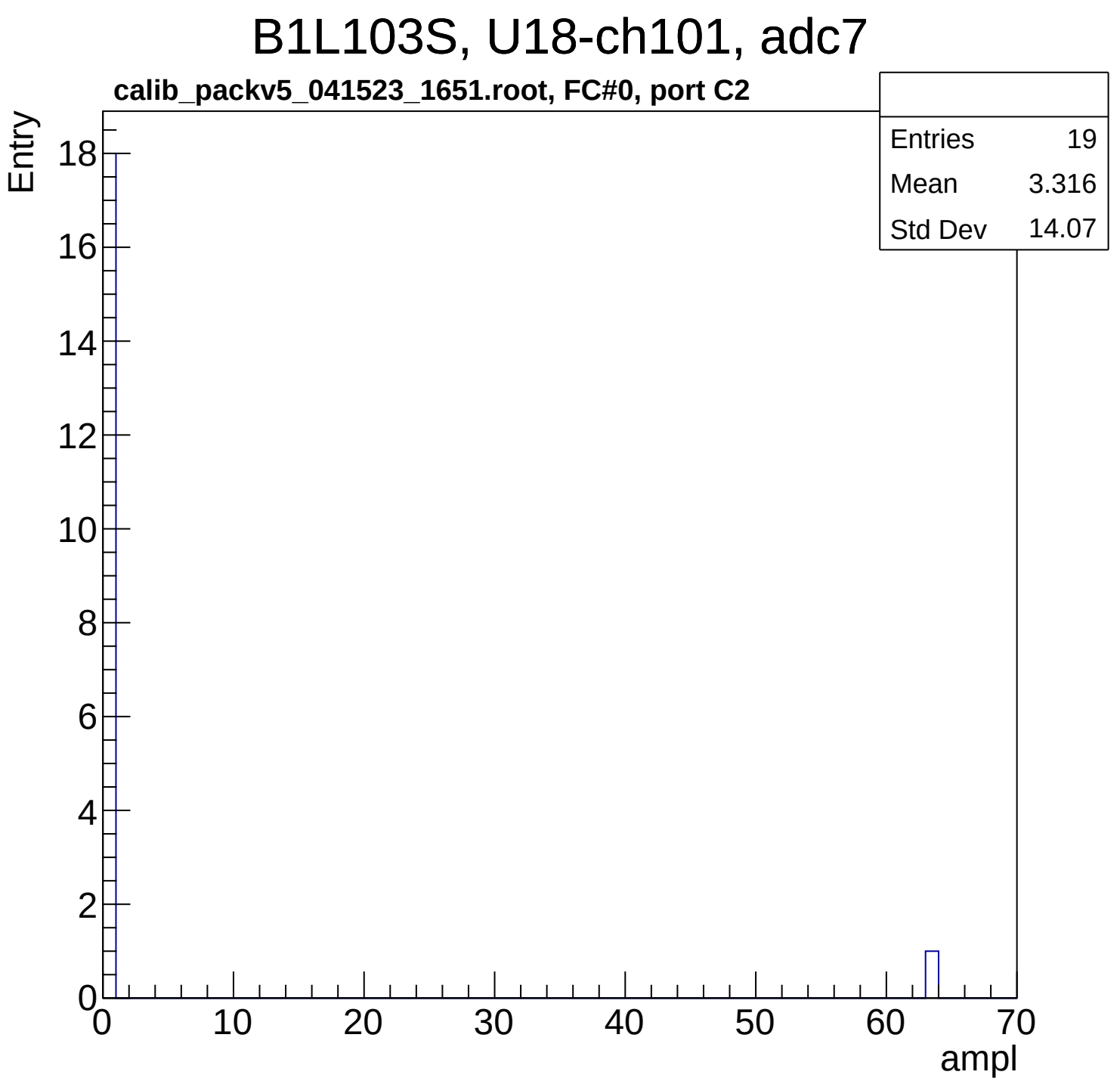
20
30
40
50
60
70


B1L103S, U18-ch101, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 5
Mean 62.2
Std Dev 0.7483
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U18-ch101, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 3.316
Std Dev 14.07
Entry
0
2
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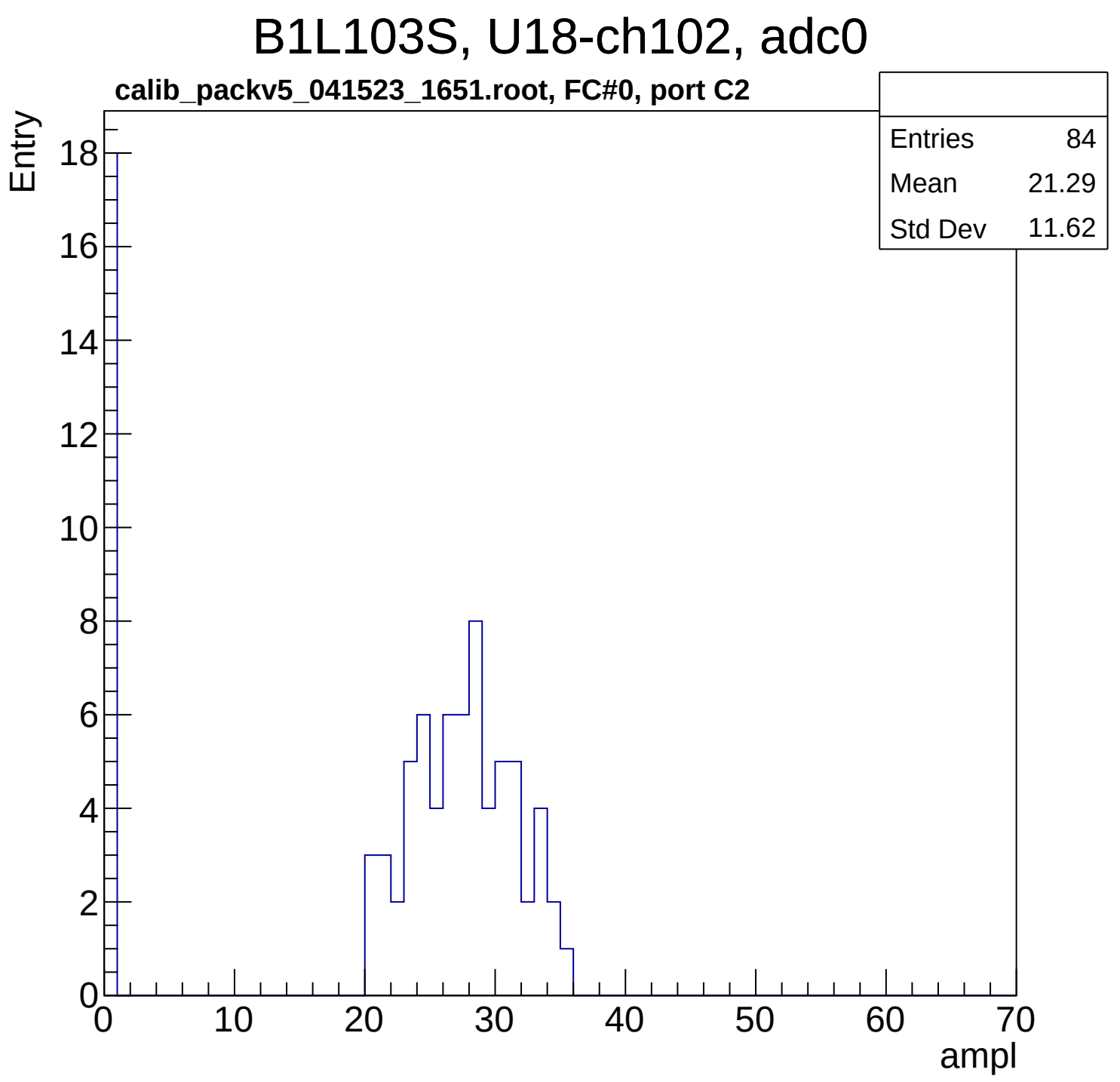
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch102, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 21.29
Std Dev 11.62
Entry
0
2
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6
8
10
12
14
16
18
0
10
20
30
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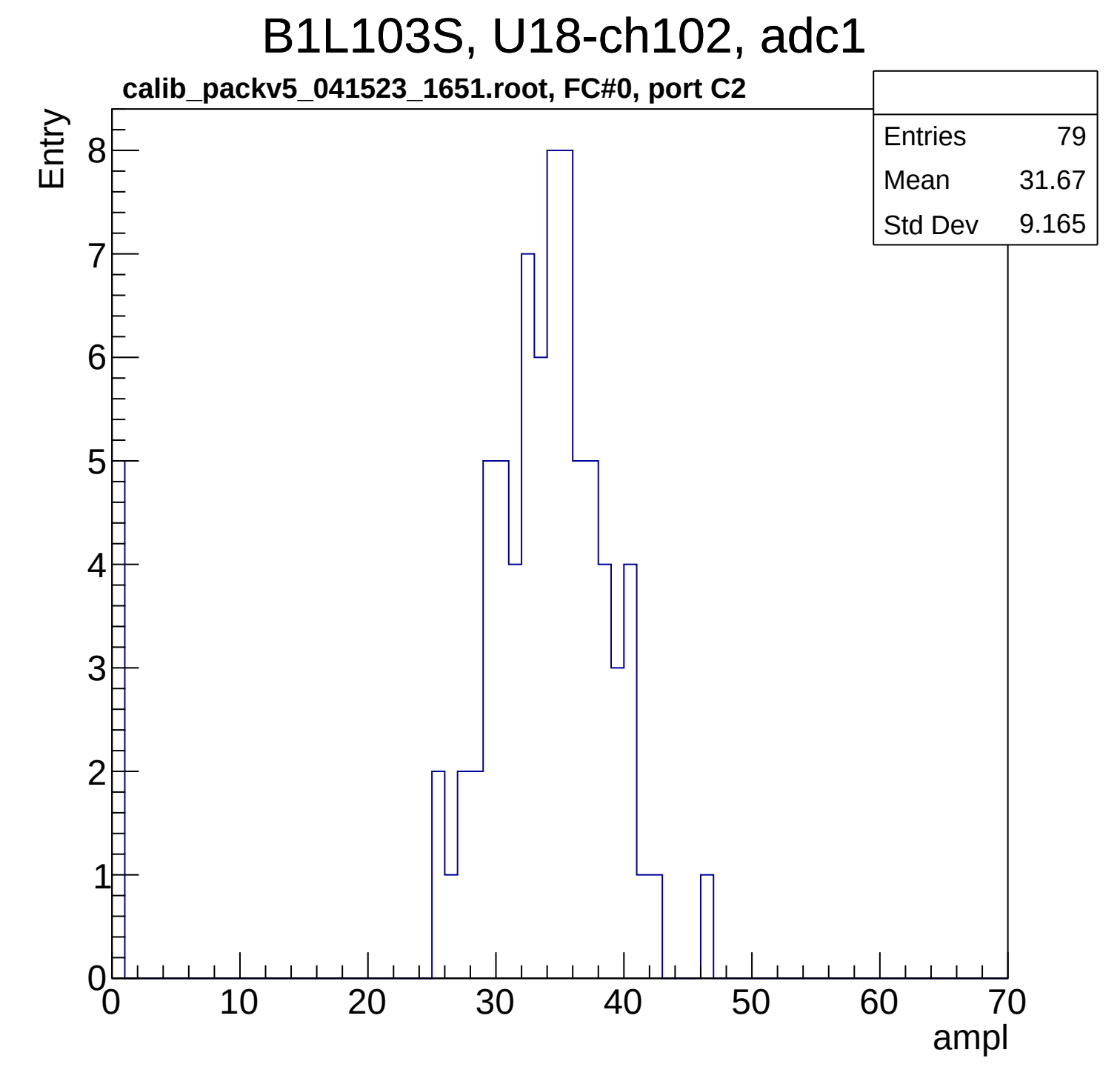
50
60
70
ampl


B1L103S, U18-ch102, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 31.67
Std Dev 9.165
Entry
ampl
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1
2
3
4
5
6
7
8
0
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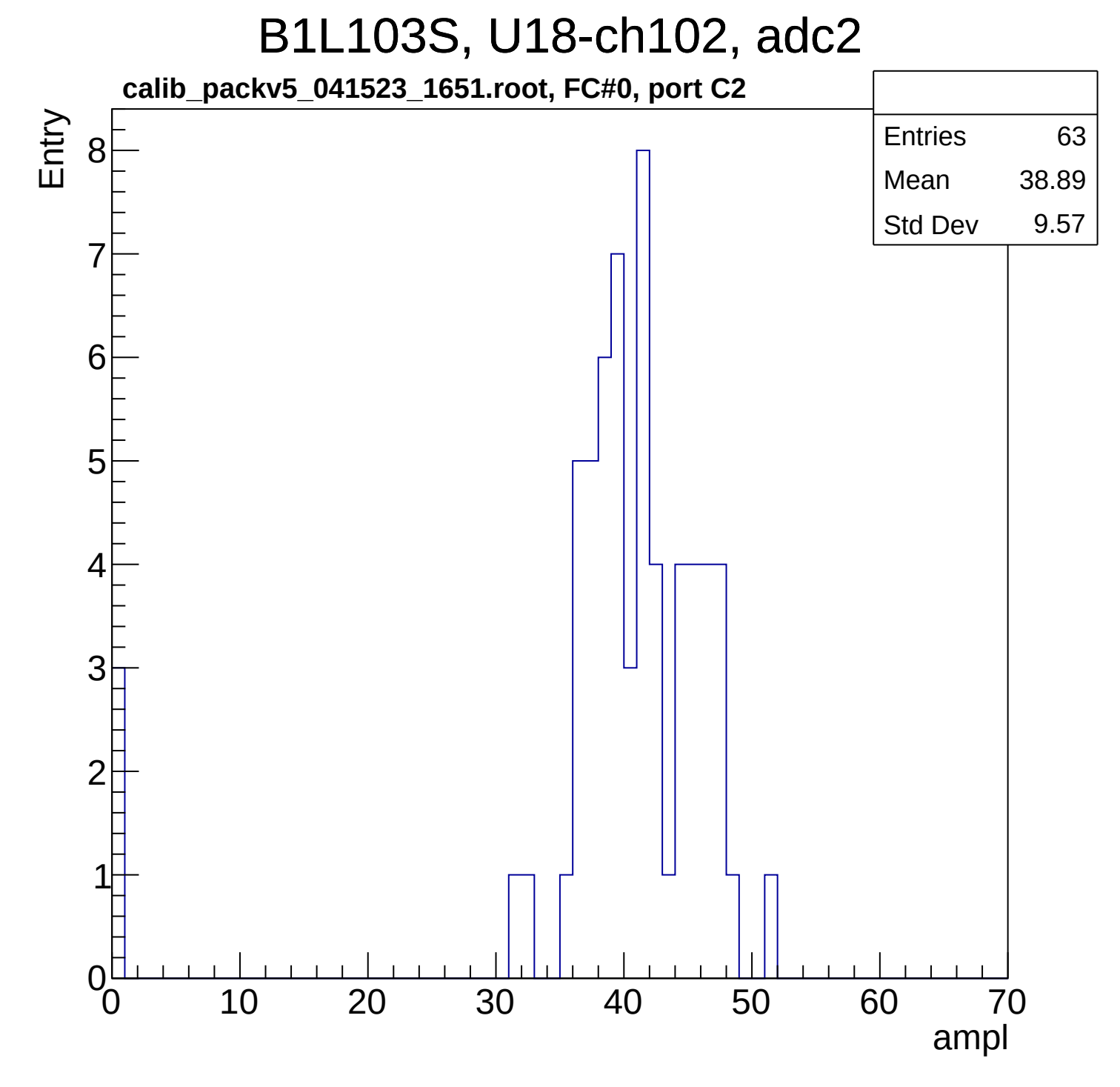
20
30
40
50
60
70


B1L103S, U18-ch102, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 38.89
Std Dev 9.57
Entry
ampl
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1
2
3
4
5
6
7
8
0
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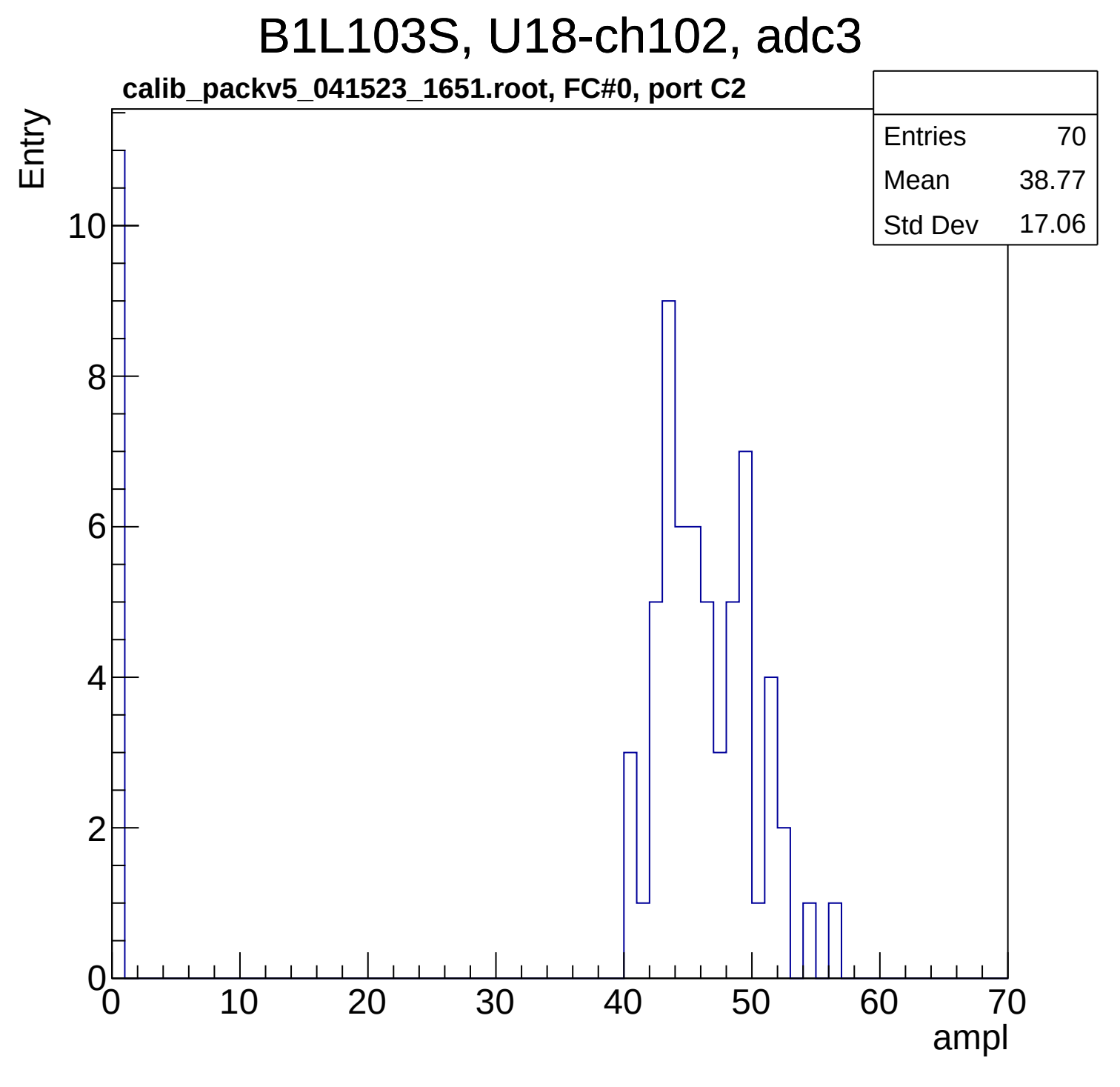
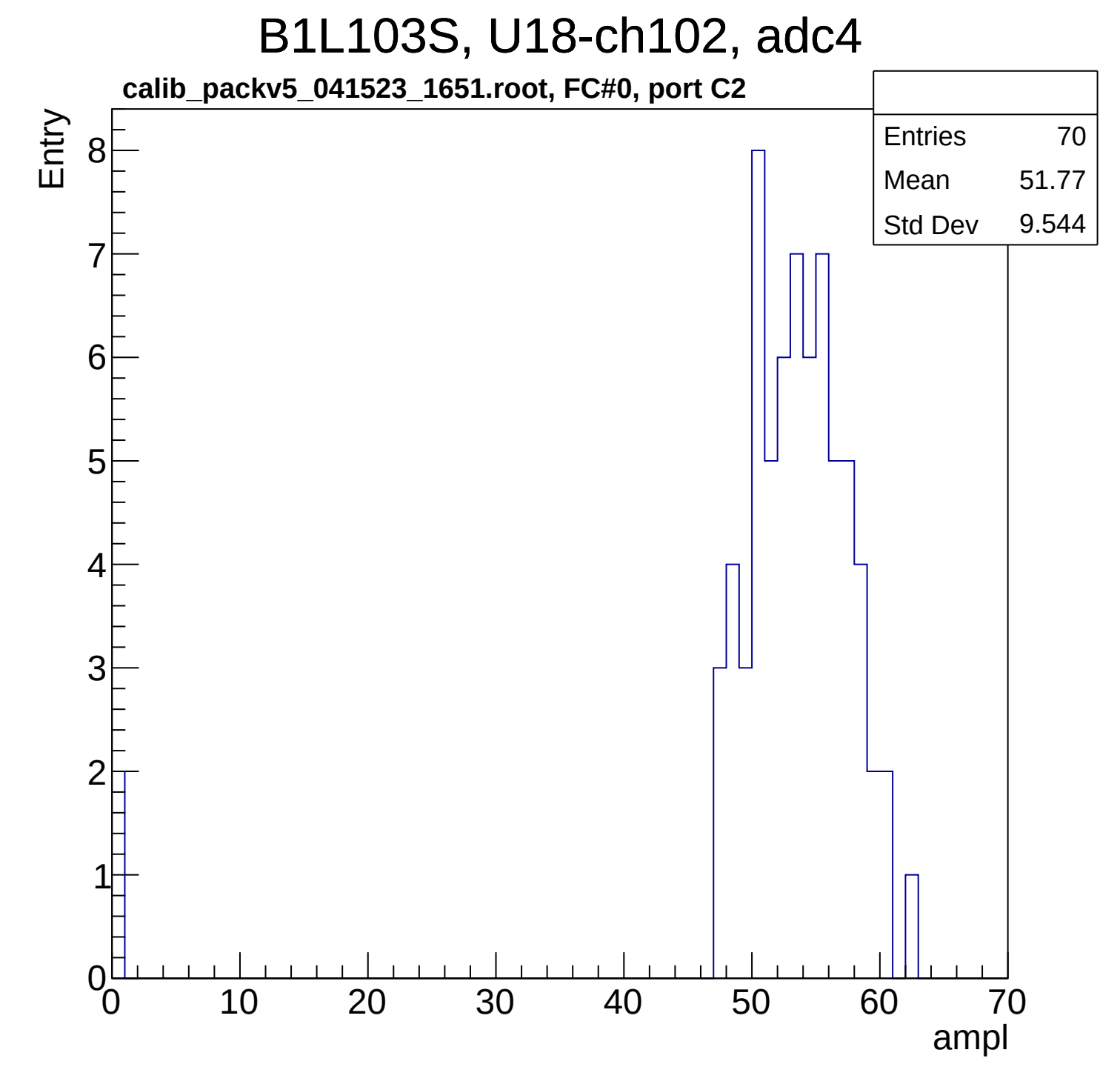
20
30
40
50
60
70


B1L103S, U18-ch102, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 38.77
Std Dev 17.06
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch102, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 51.77
Std Dev 9.544
Entry
ampl
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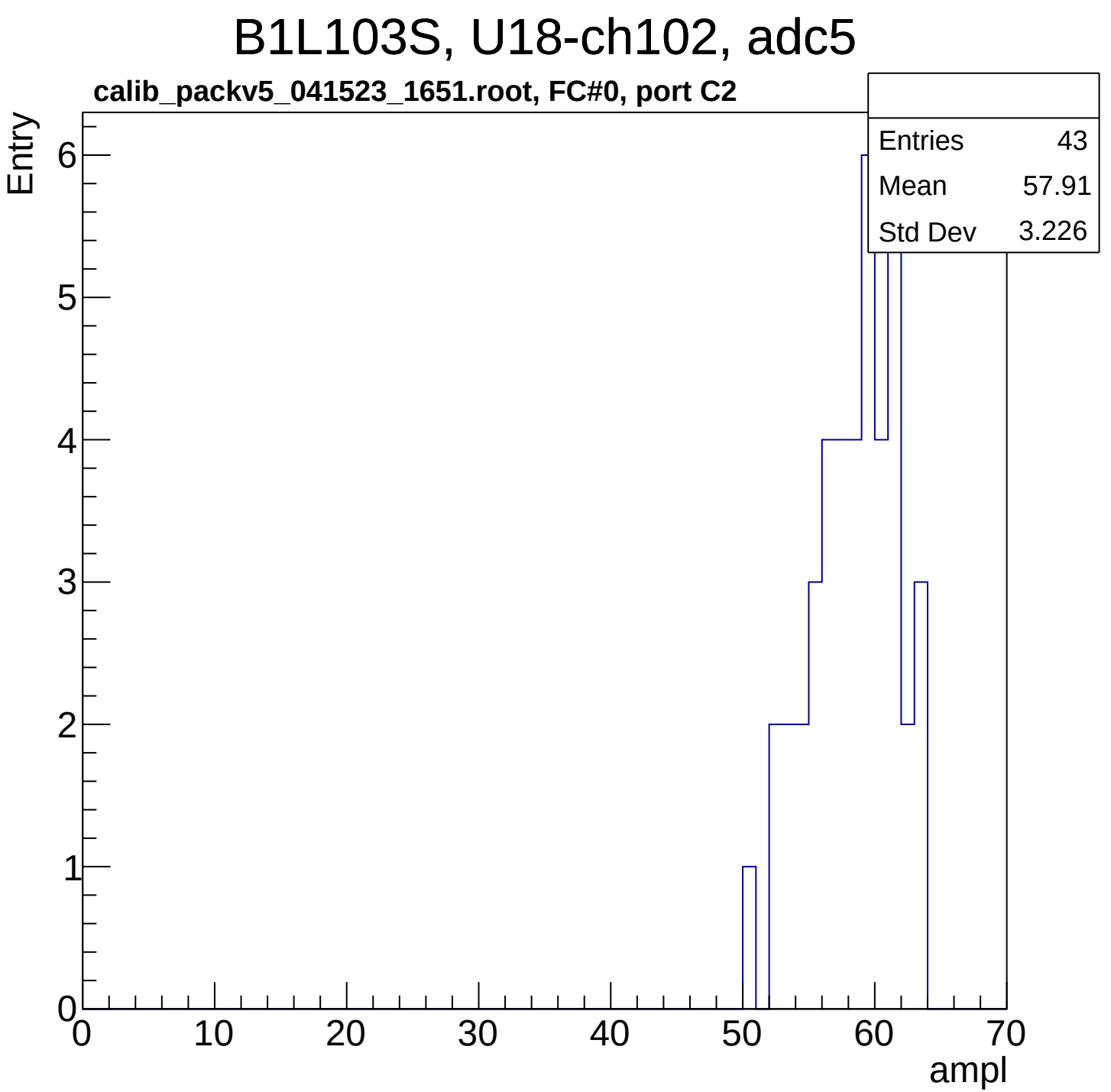
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch102, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 43
Mean 57.91
Std Dev 3.226
Entry
ampl
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1
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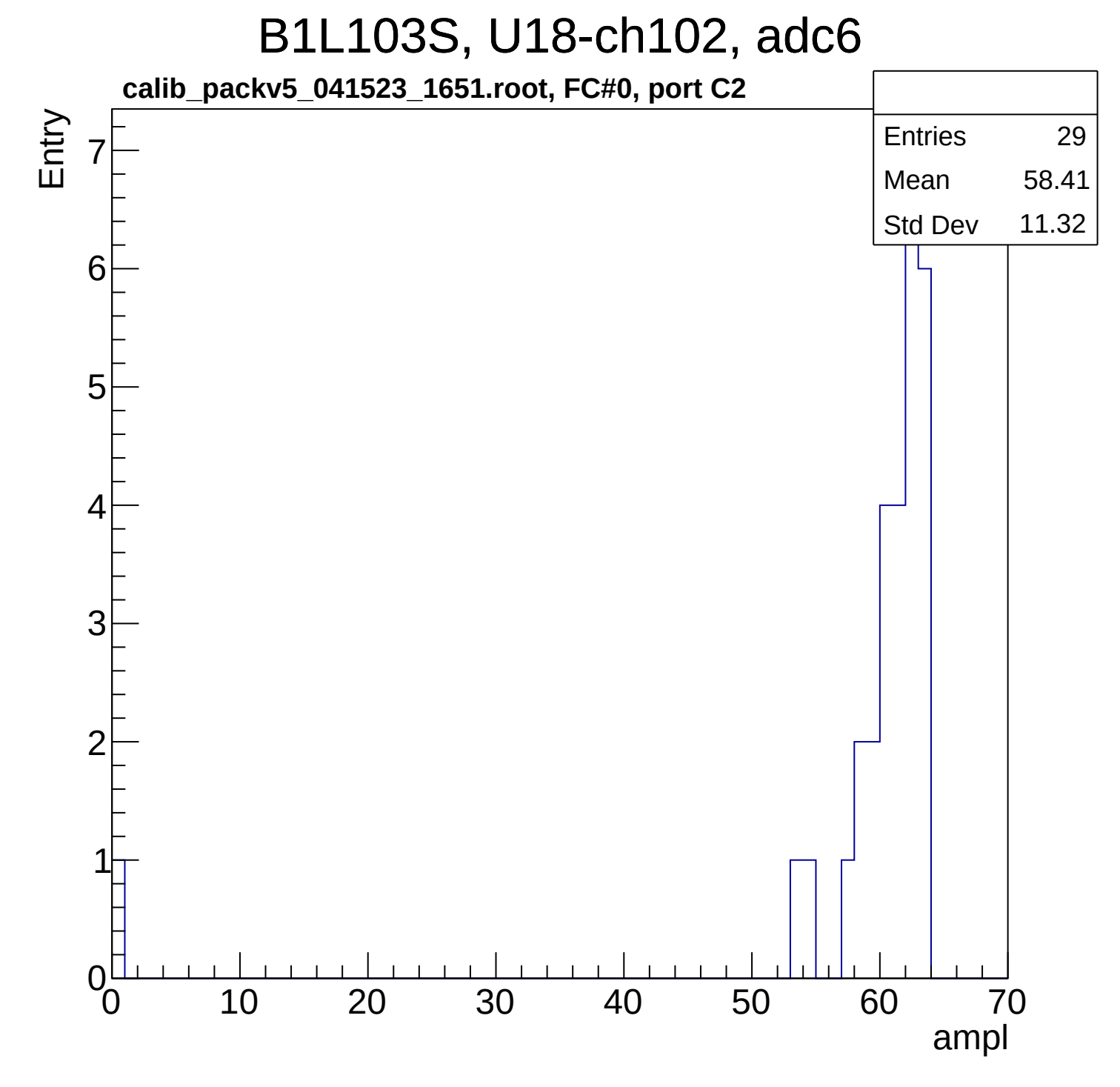
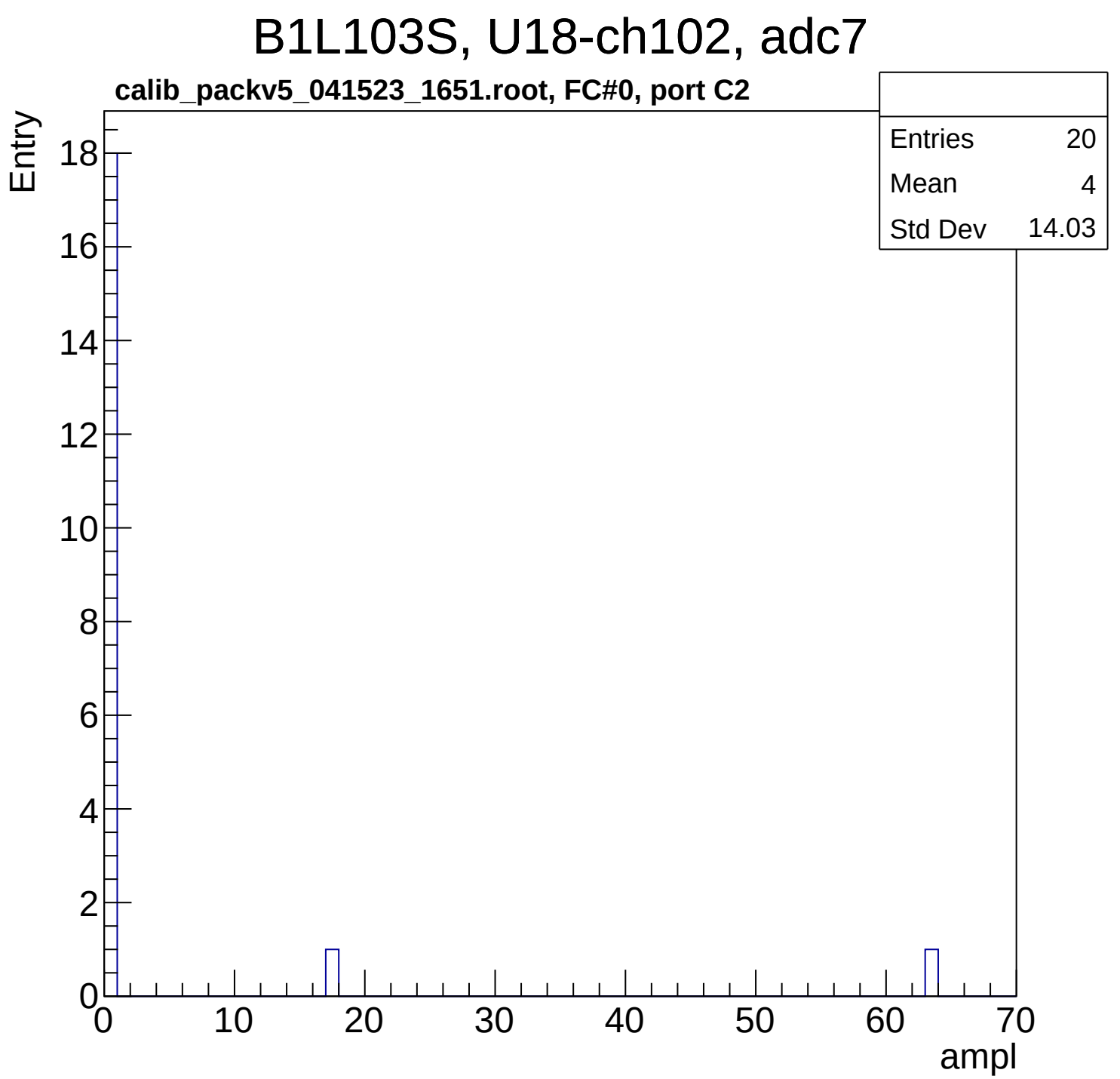
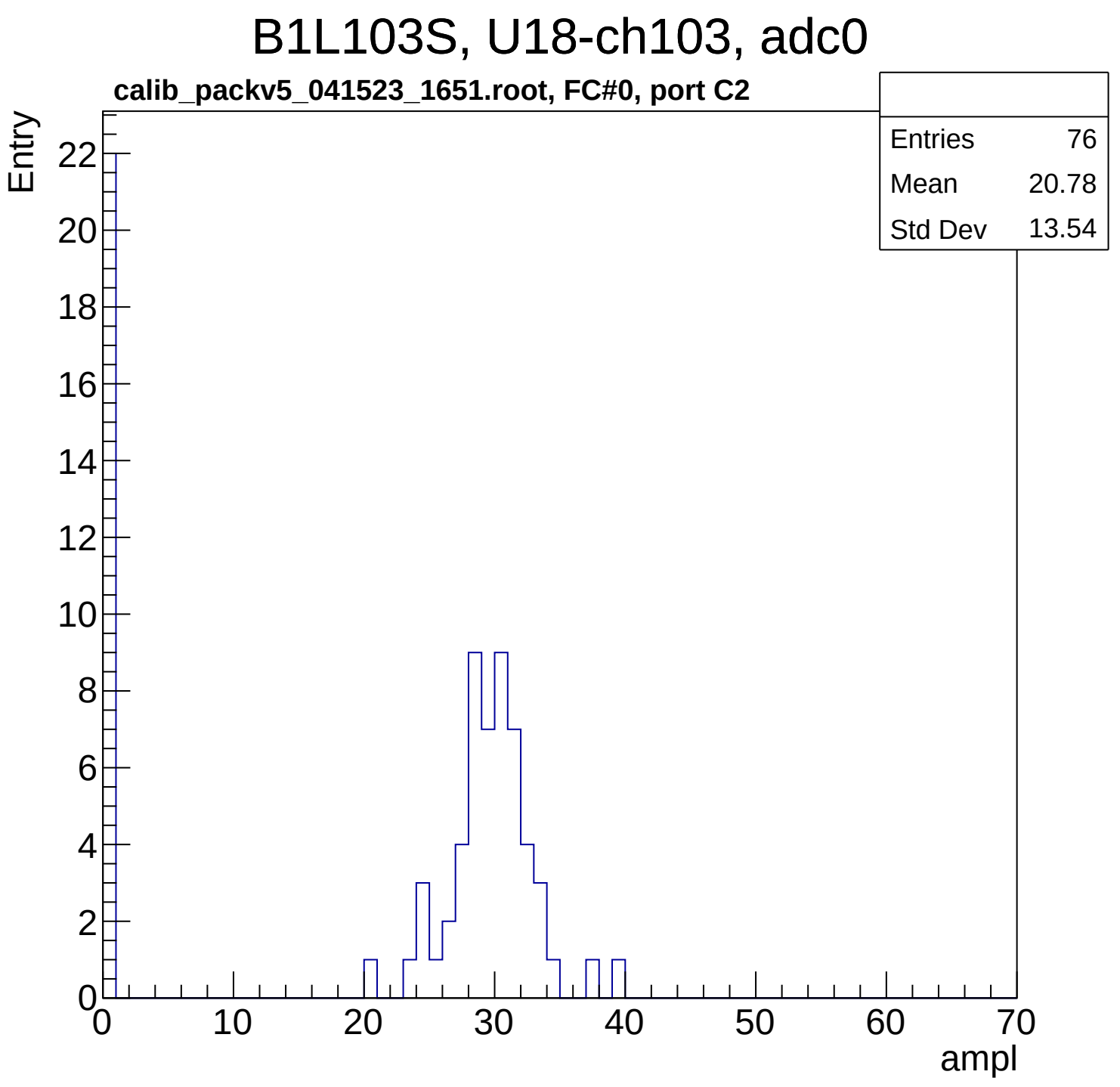
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U18-ch102, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 29
Mean 58.41
Std Dev 11.32
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U18-ch102, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 4
Std Dev 14.03
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch103, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 20.78
Std Dev 13.54
Entry
ampl
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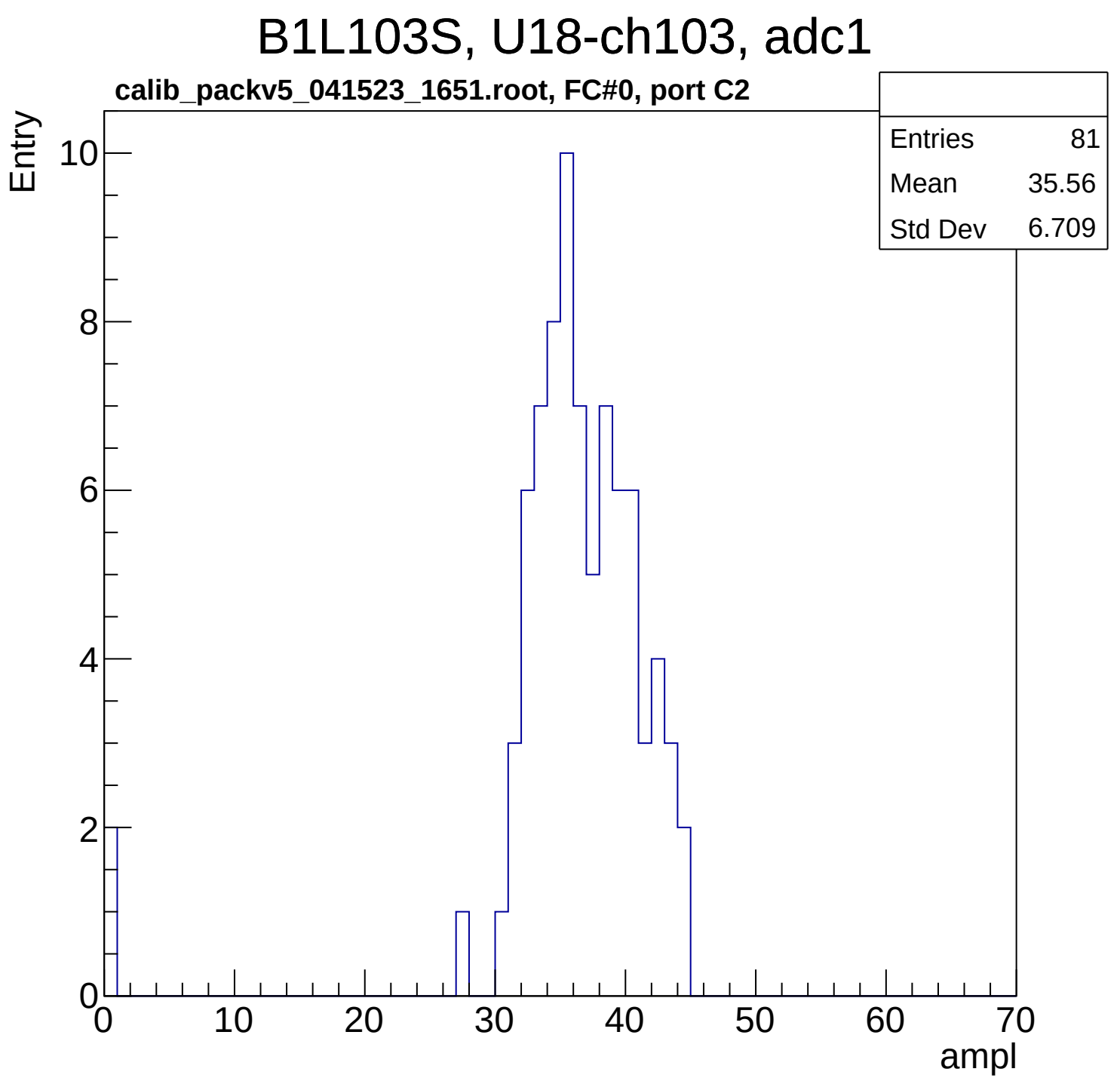
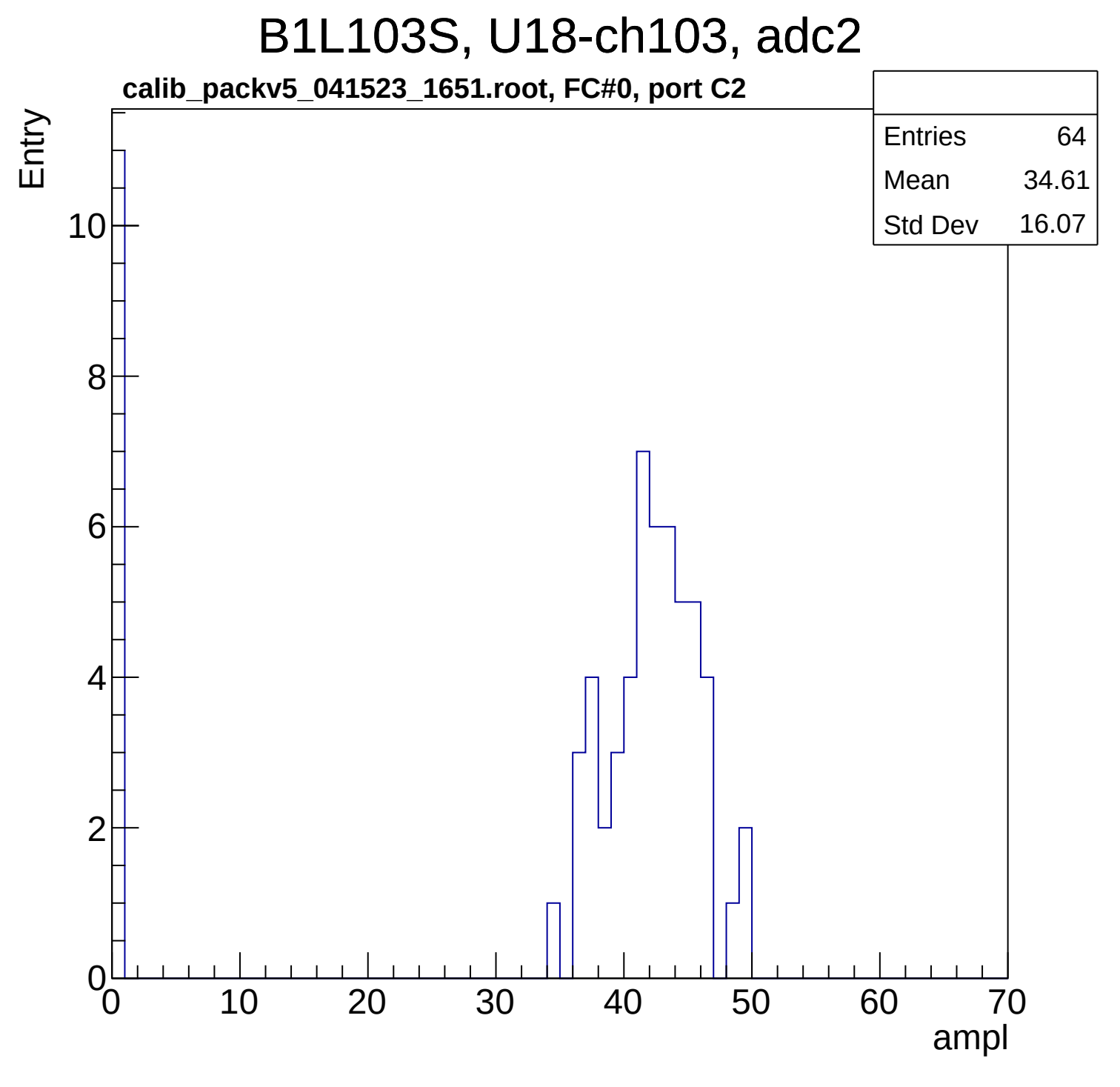
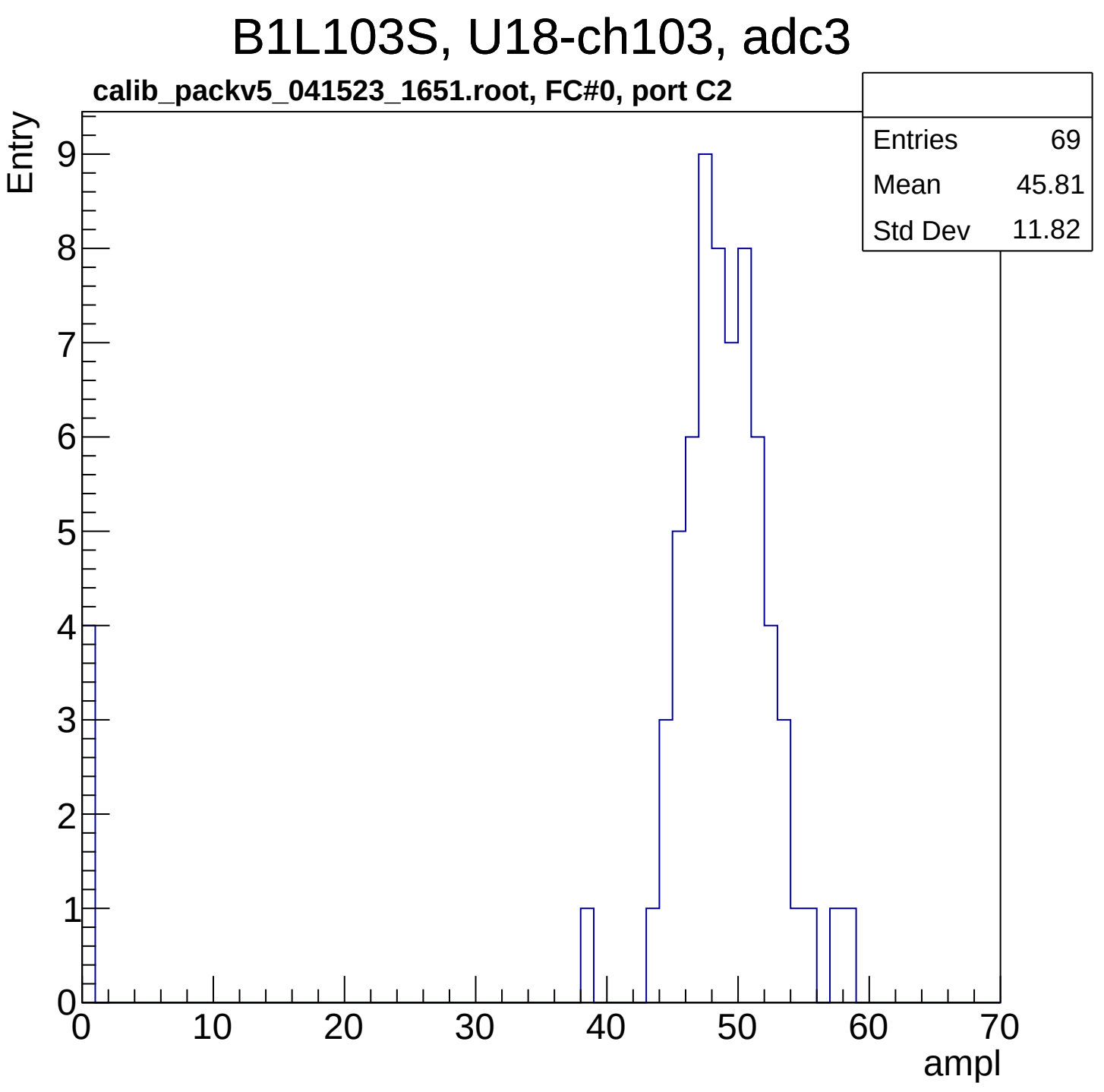
6
8
10
12
14
16
18
20
22
0
10
20
30
40
50
60
70


B1L103S, U18-ch103, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 35.56
Std Dev 6.709
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U18-ch103, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 34.61
Std Dev 16.07
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U18-ch103, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 45.81
Std Dev 11.82
Entry
ampl
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3
4
5
6
7
8
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0
10
20
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40
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60
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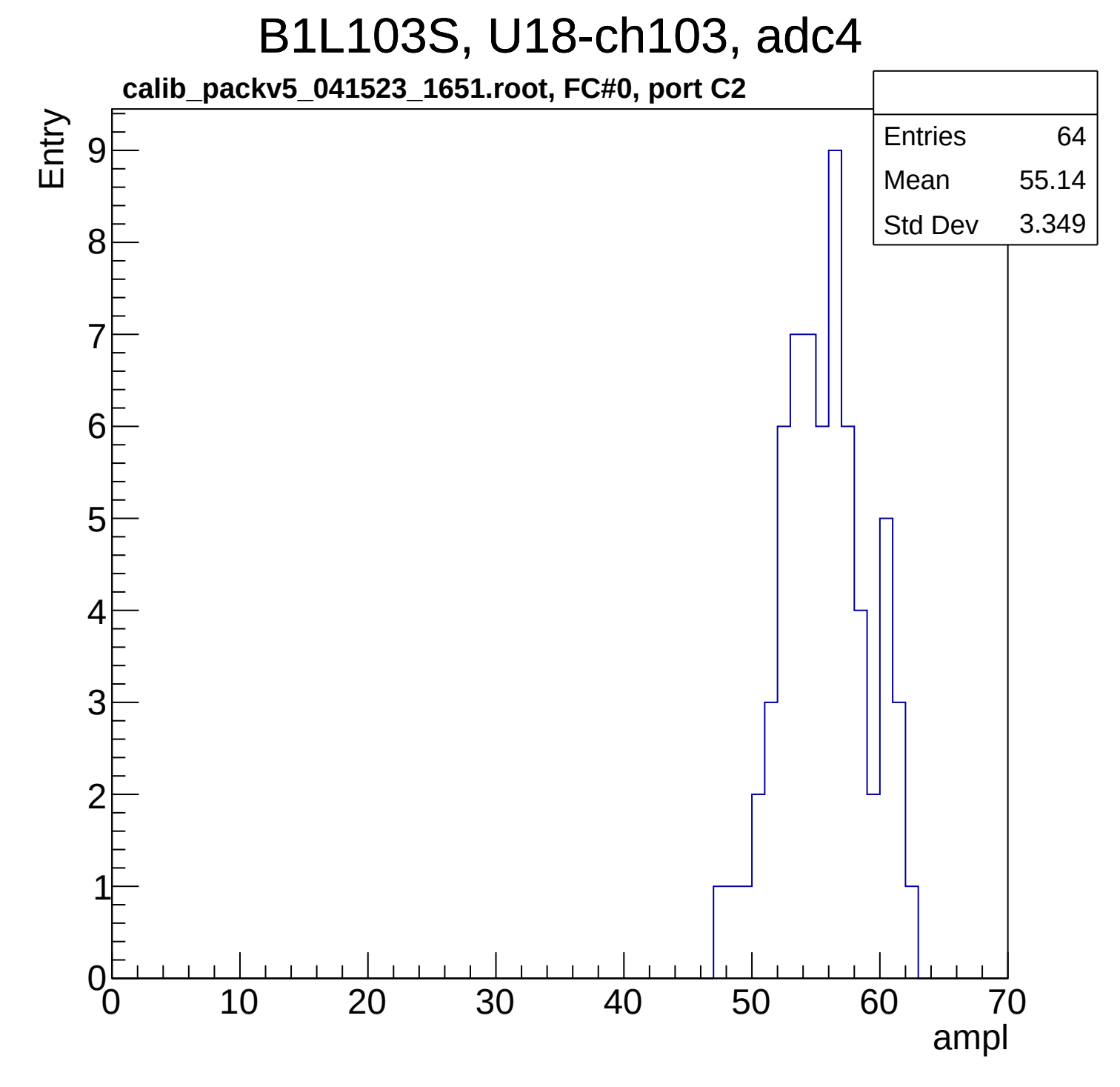
B1L103S, U18-ch103, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 55.14
Std Dev 3.349
Entry
ampl
0
1
2
3
4
5
6
7
8
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0
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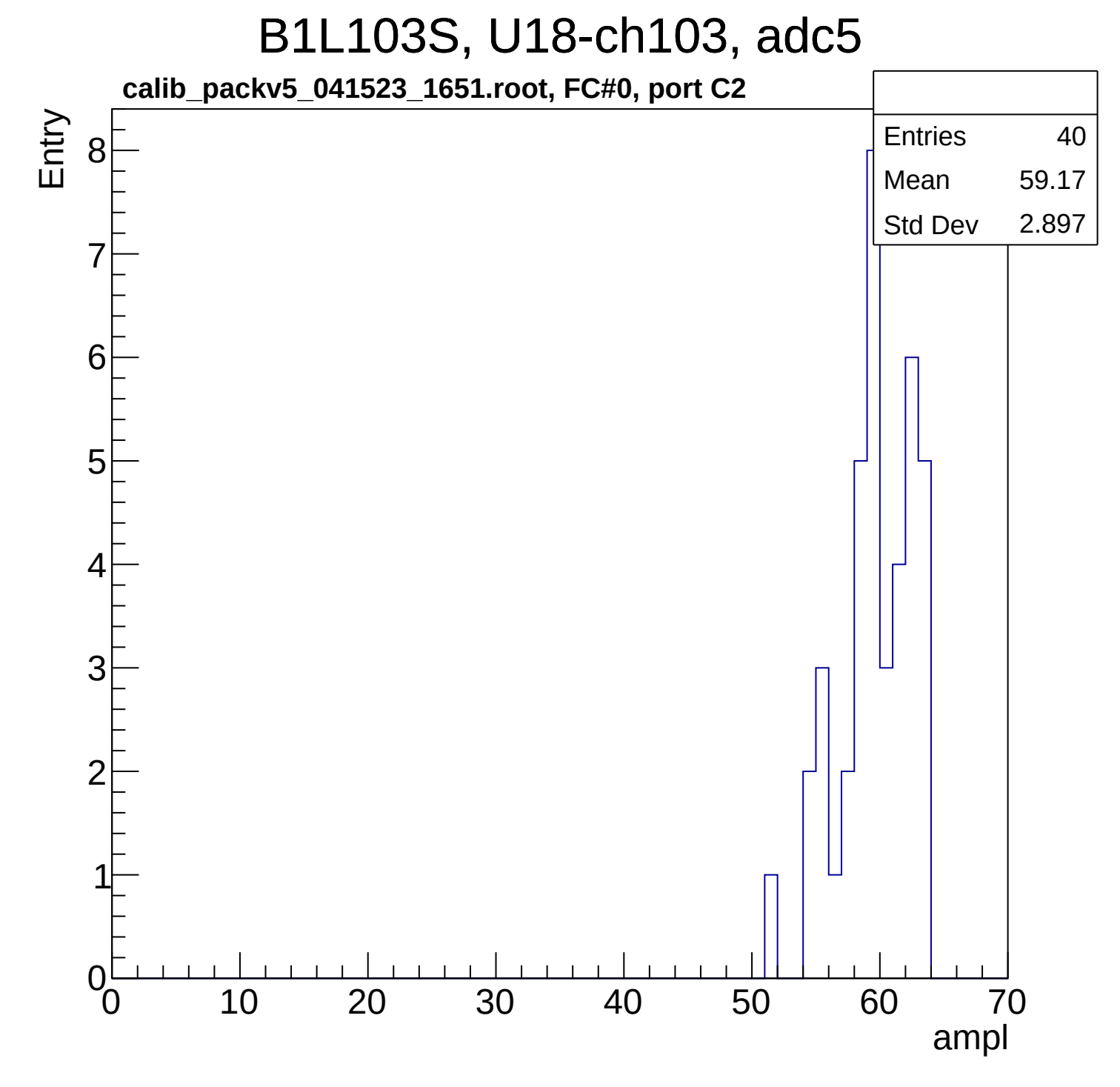
60
70


B1L103S, U18-ch103, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 40
Mean 59.17
Std Dev 2.897
Entry
ampl
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2
3
4
5
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7
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0
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60
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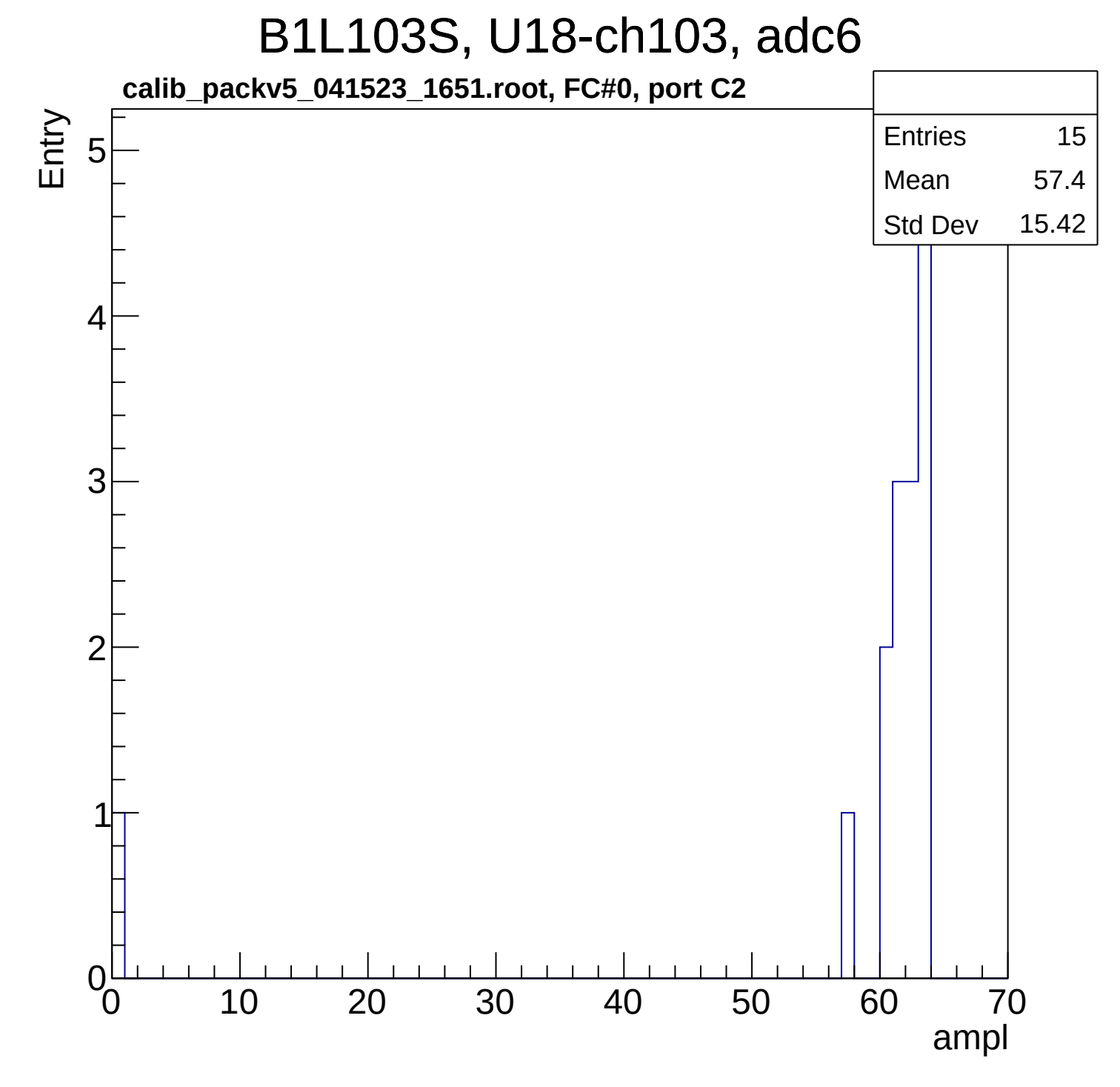
B1L103S, U18-ch103, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 15
Mean 57.4
Std Dev 15.42
Entry
ampl
0
1
2
3
4
5
0
10
20
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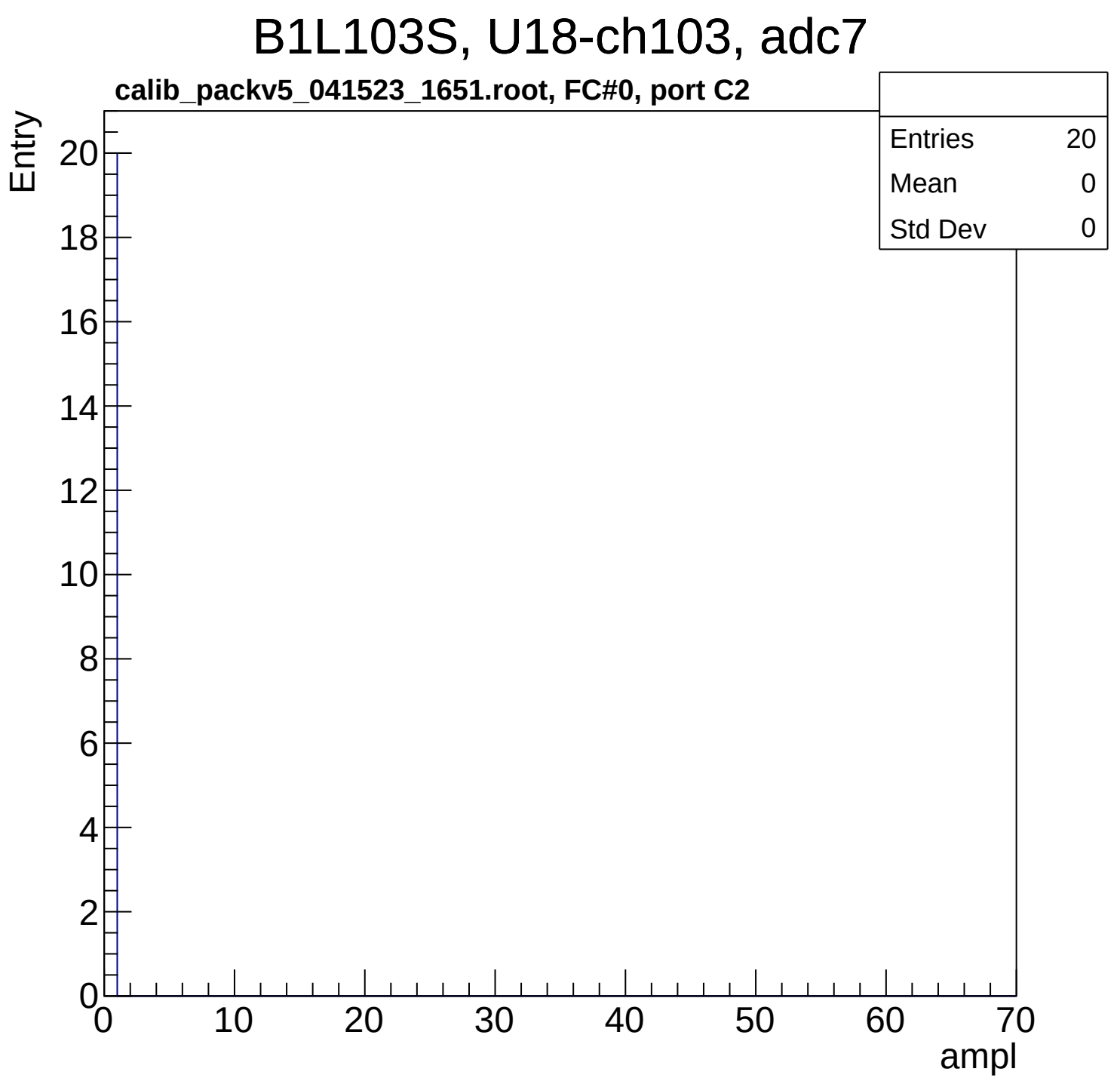
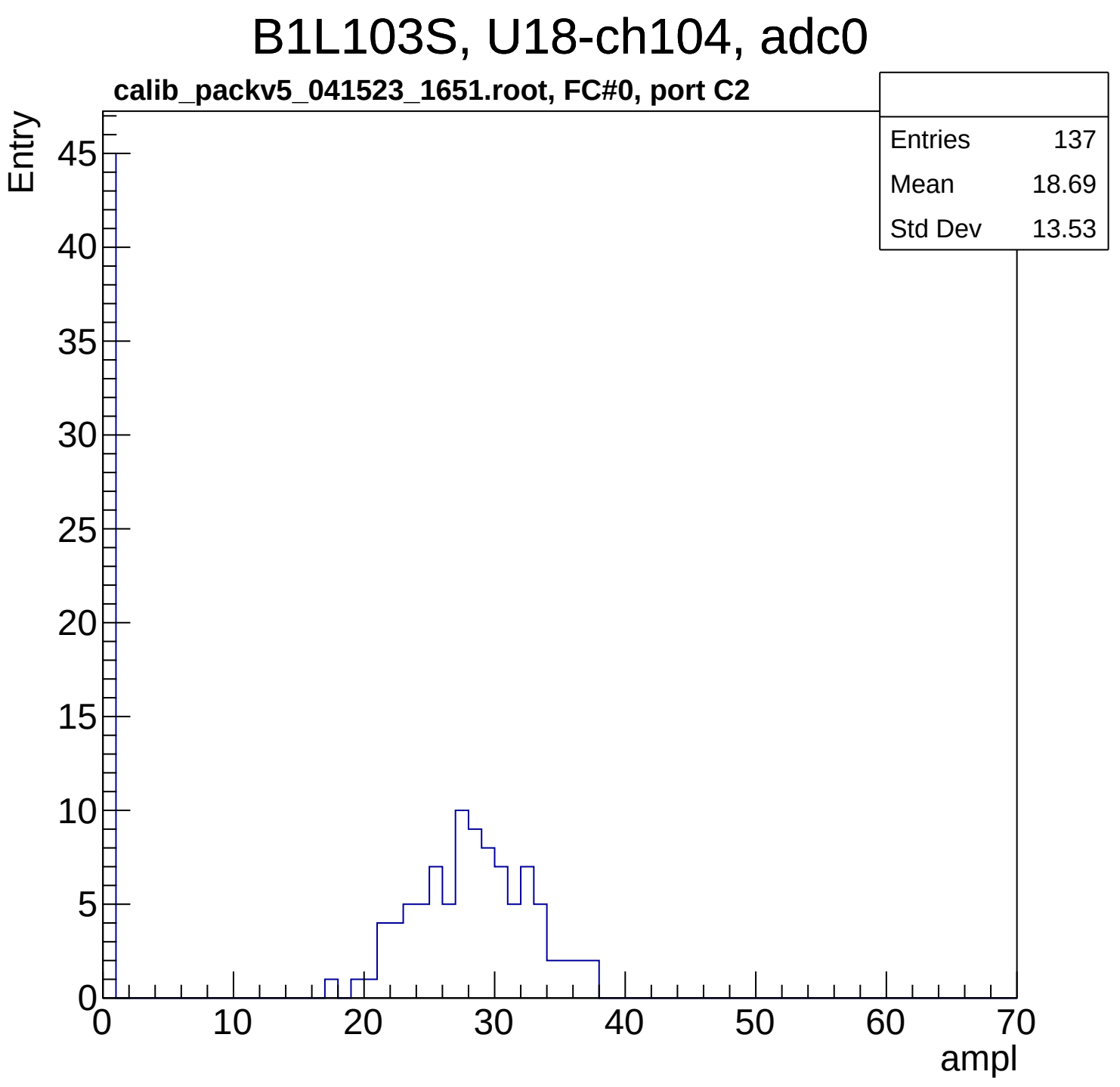
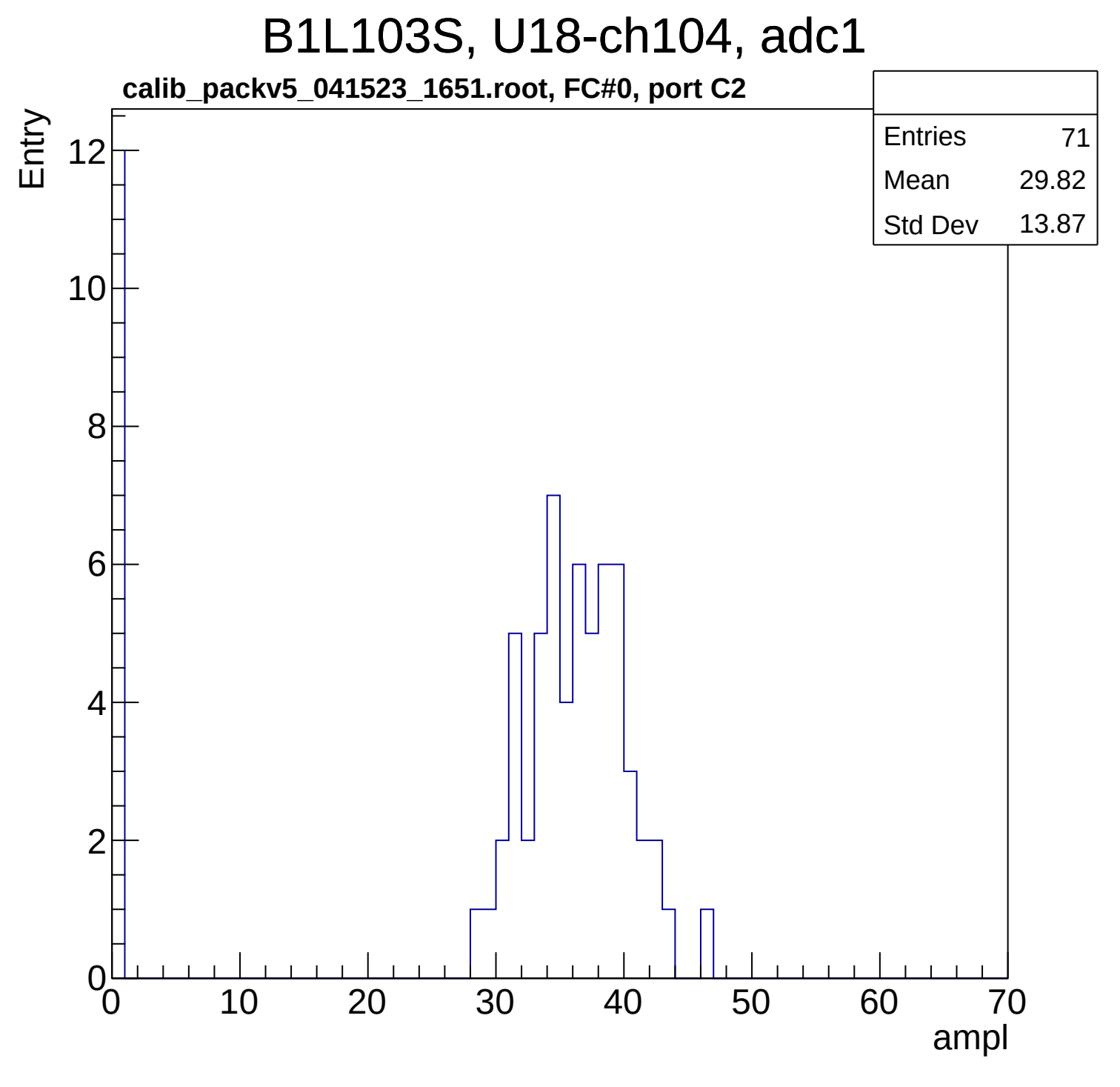
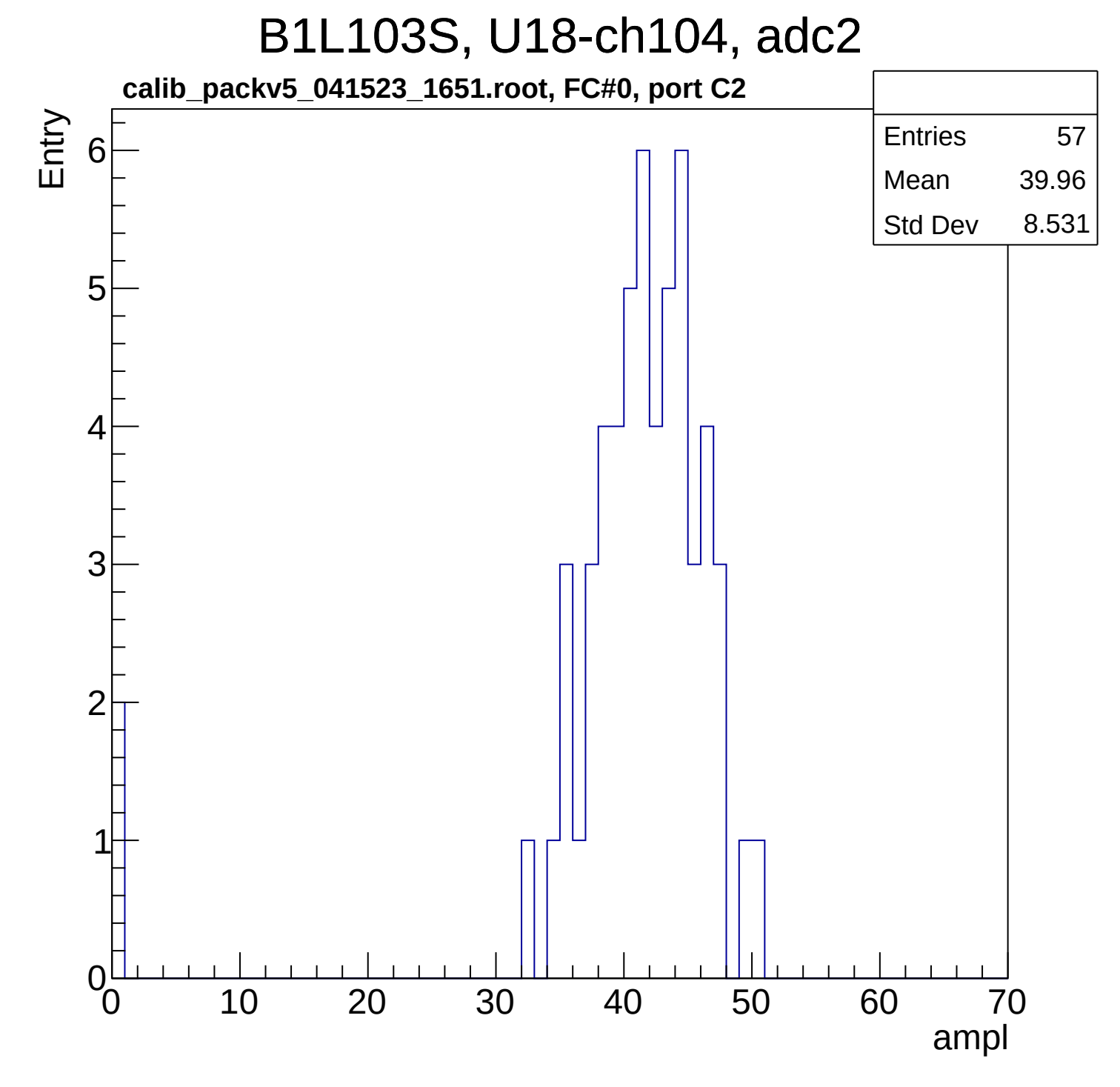
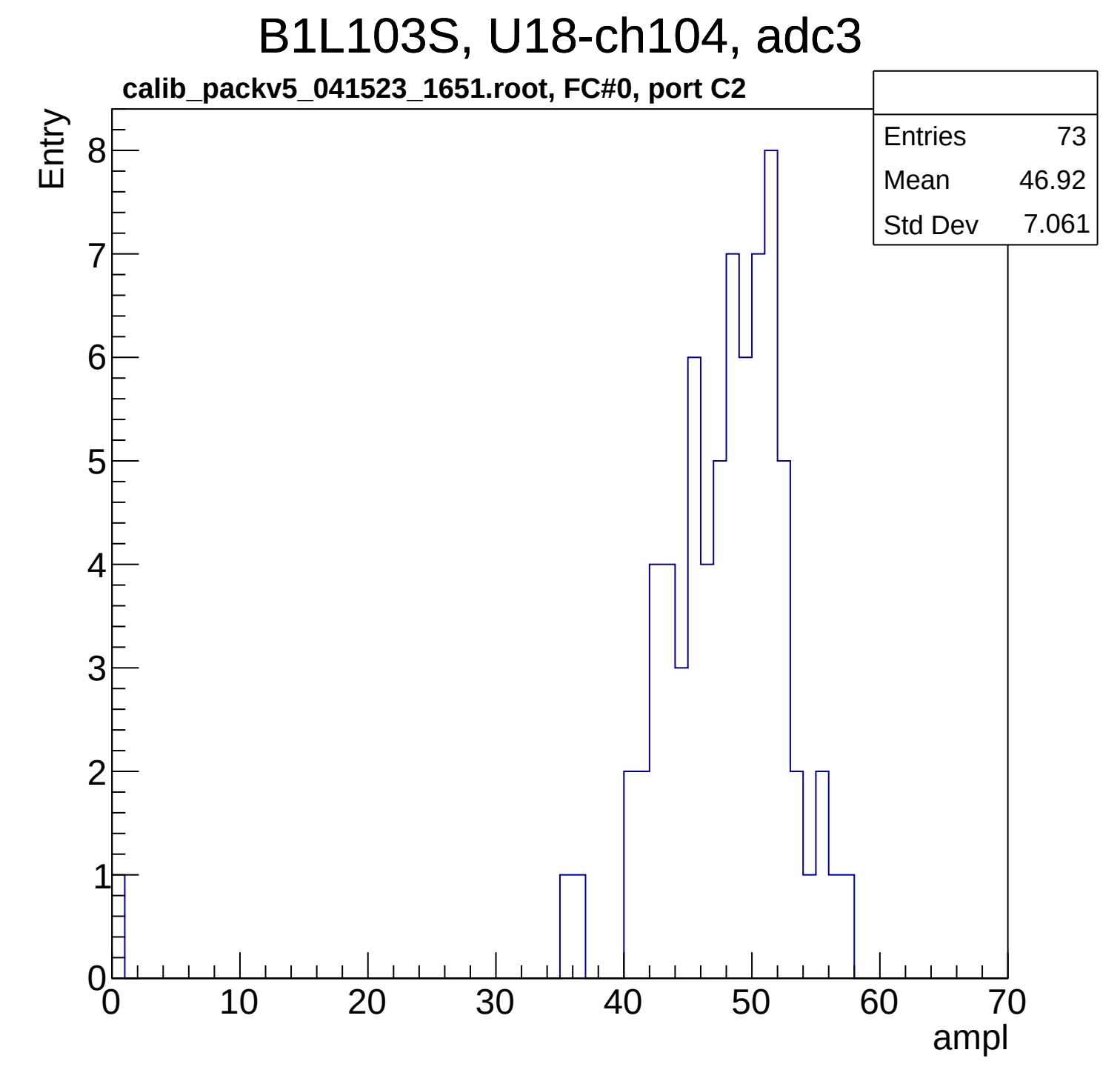
40
50
60
70


B1L103S, U18-ch103, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch104, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 137
Mean 18.69
Std Dev 13.53
Entry
0
5
10
15
20
25
30
35
40
45
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch104, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 29.82
Std Dev 13.87
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch104, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 39.96
Std Dev 8.531
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U18-ch104, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 46.92
Std Dev 7.061
Entry
ampl
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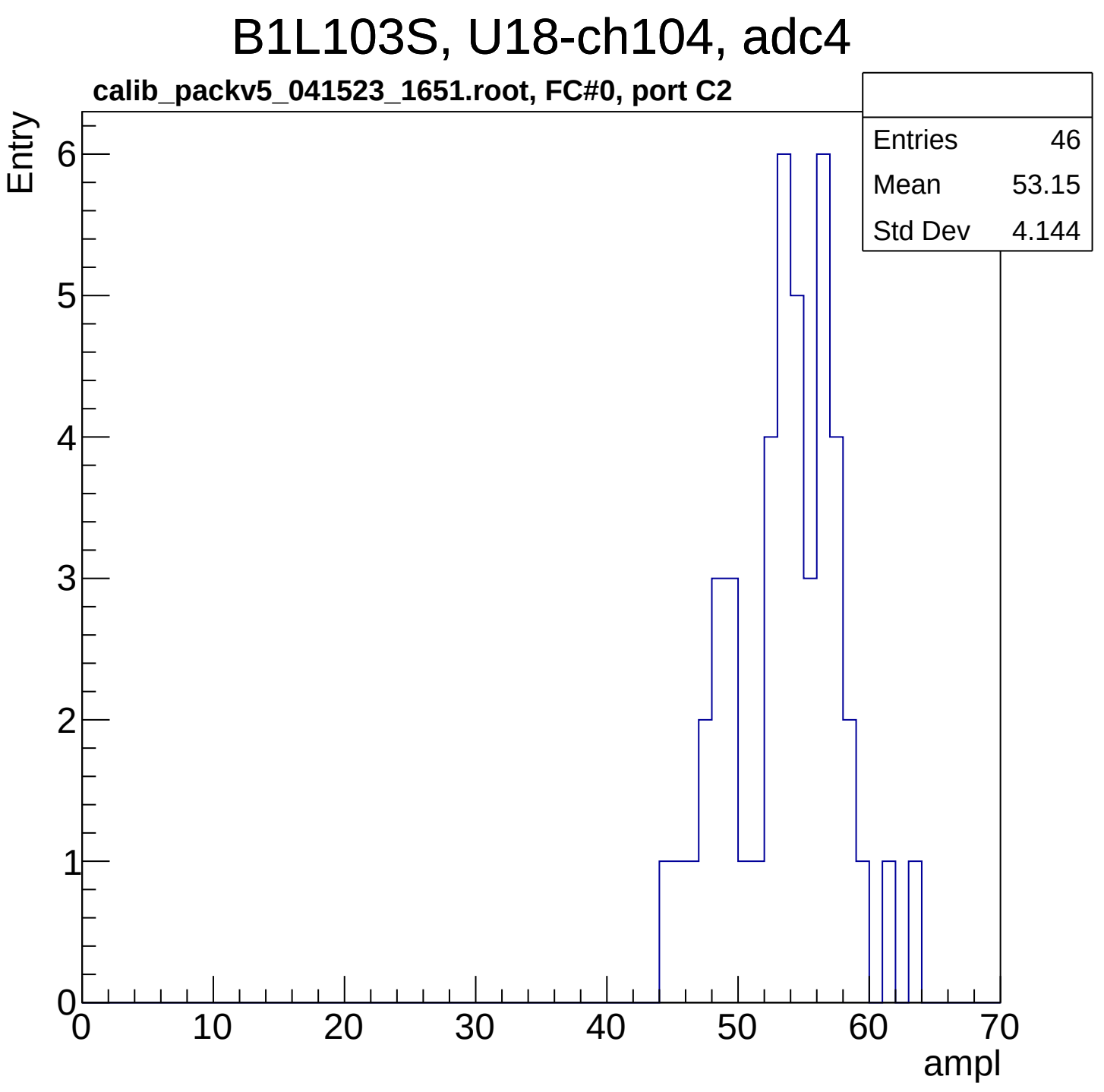
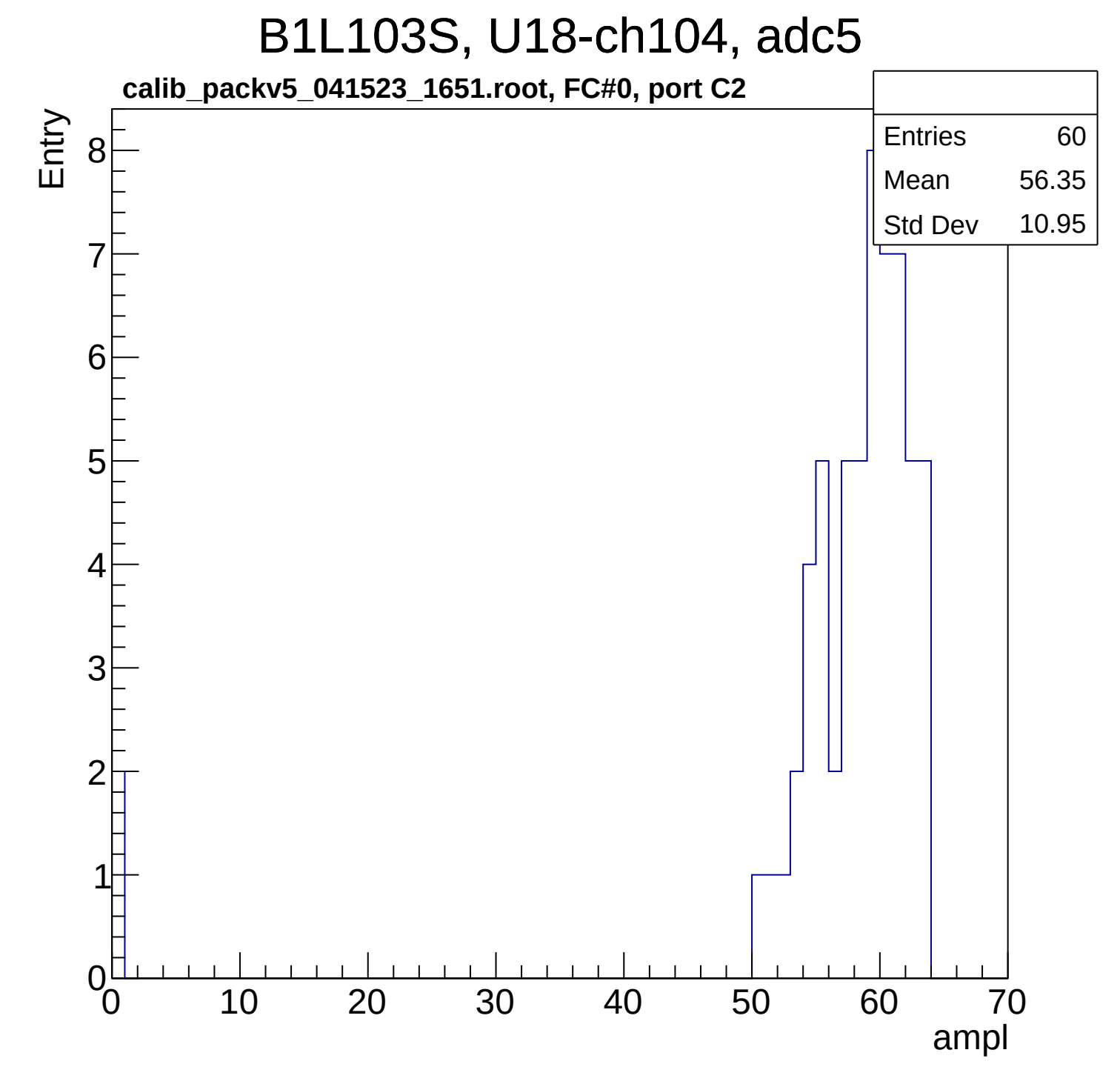
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch104, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 53.15
Std Dev 4.144
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U18-ch104, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 56.35
Std Dev 10.95
Entry
ampl
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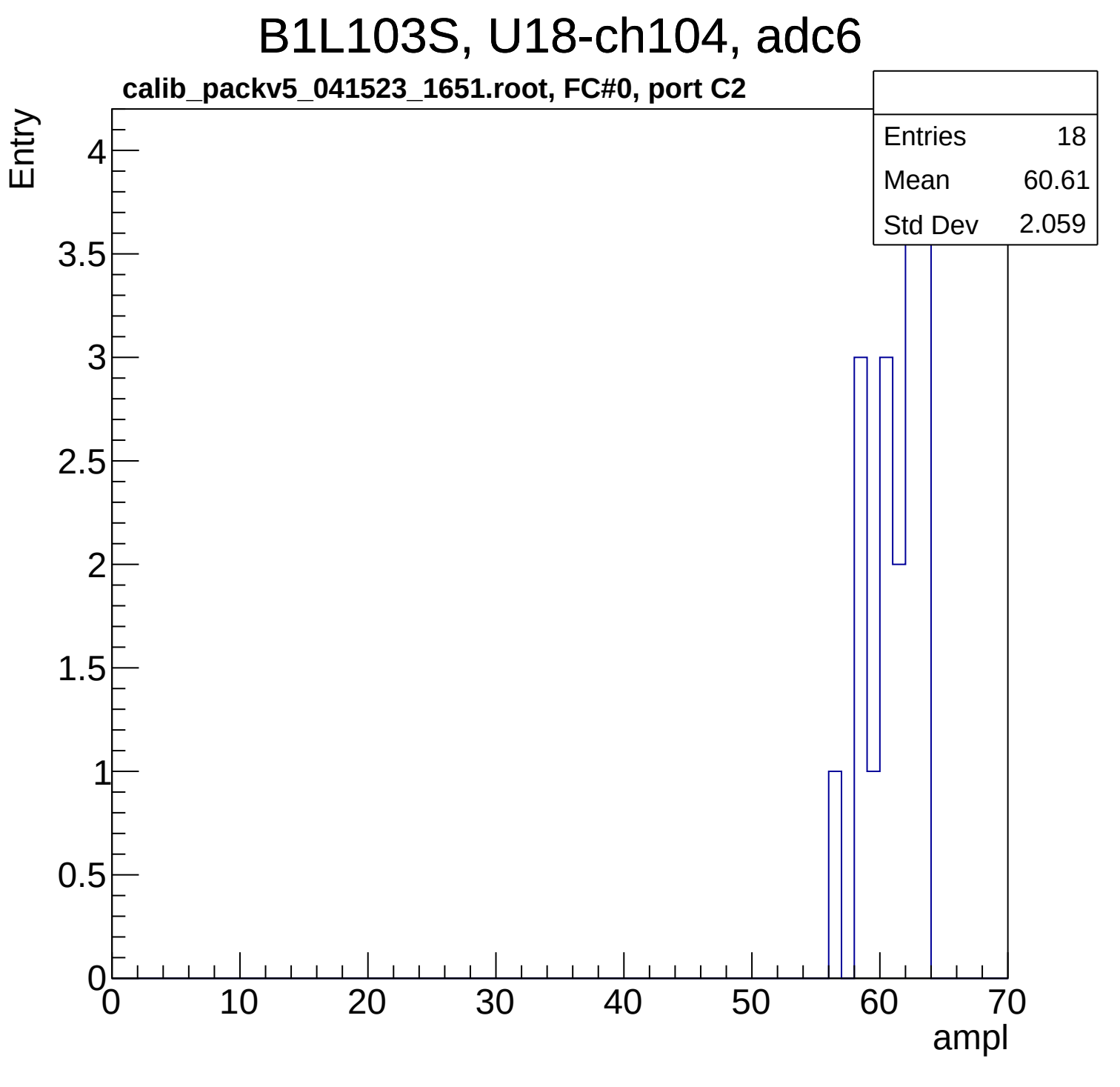
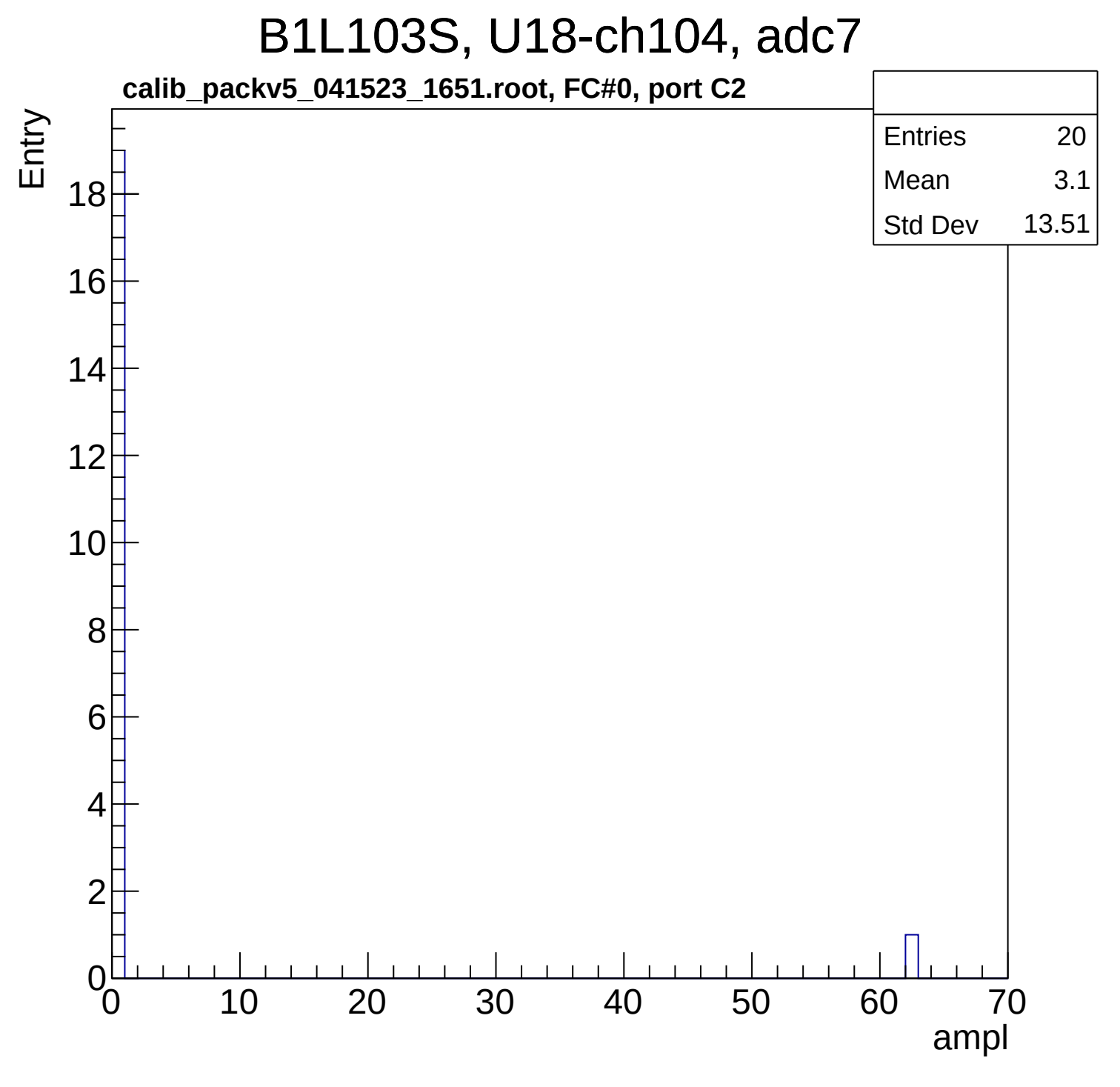
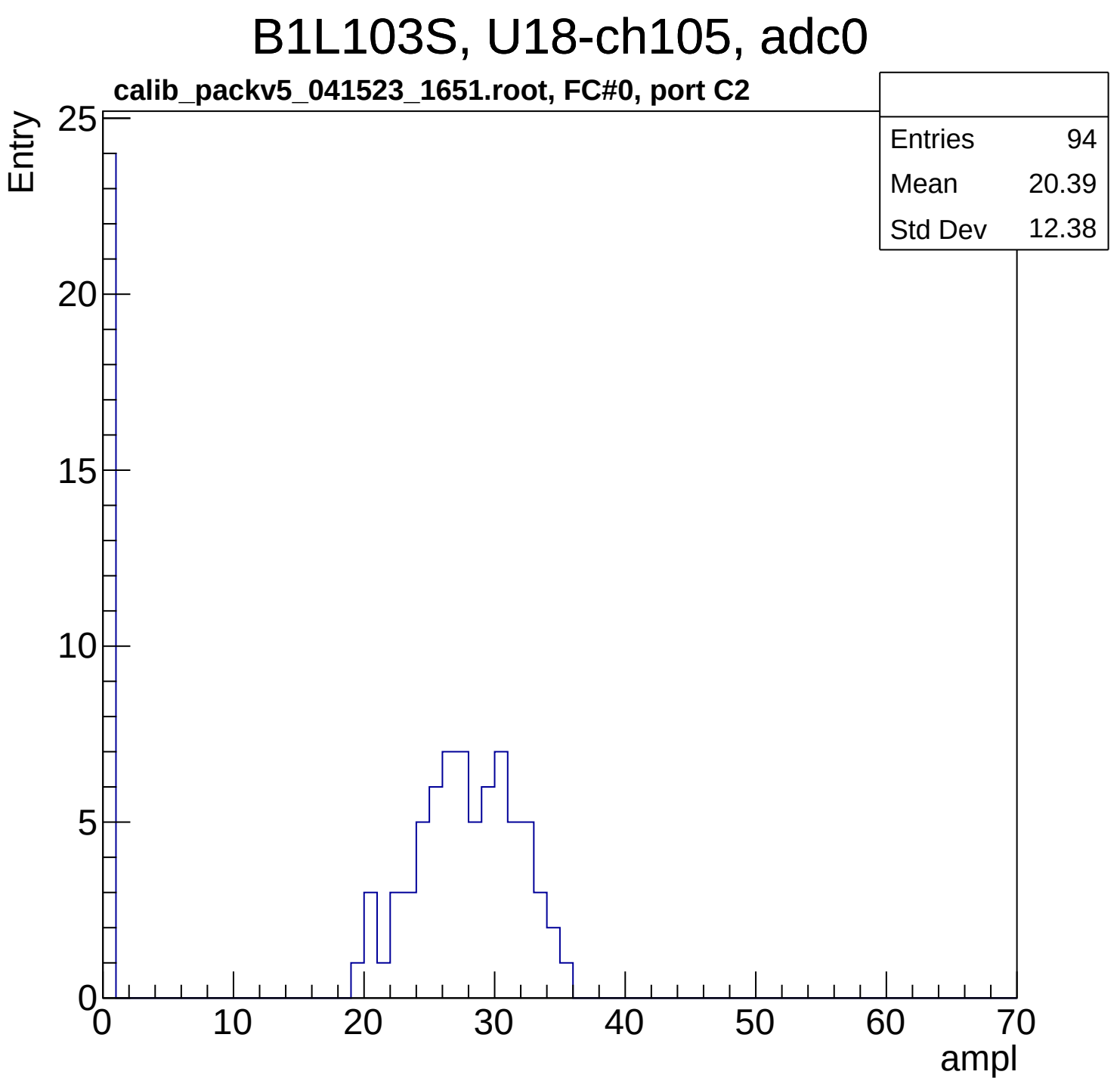
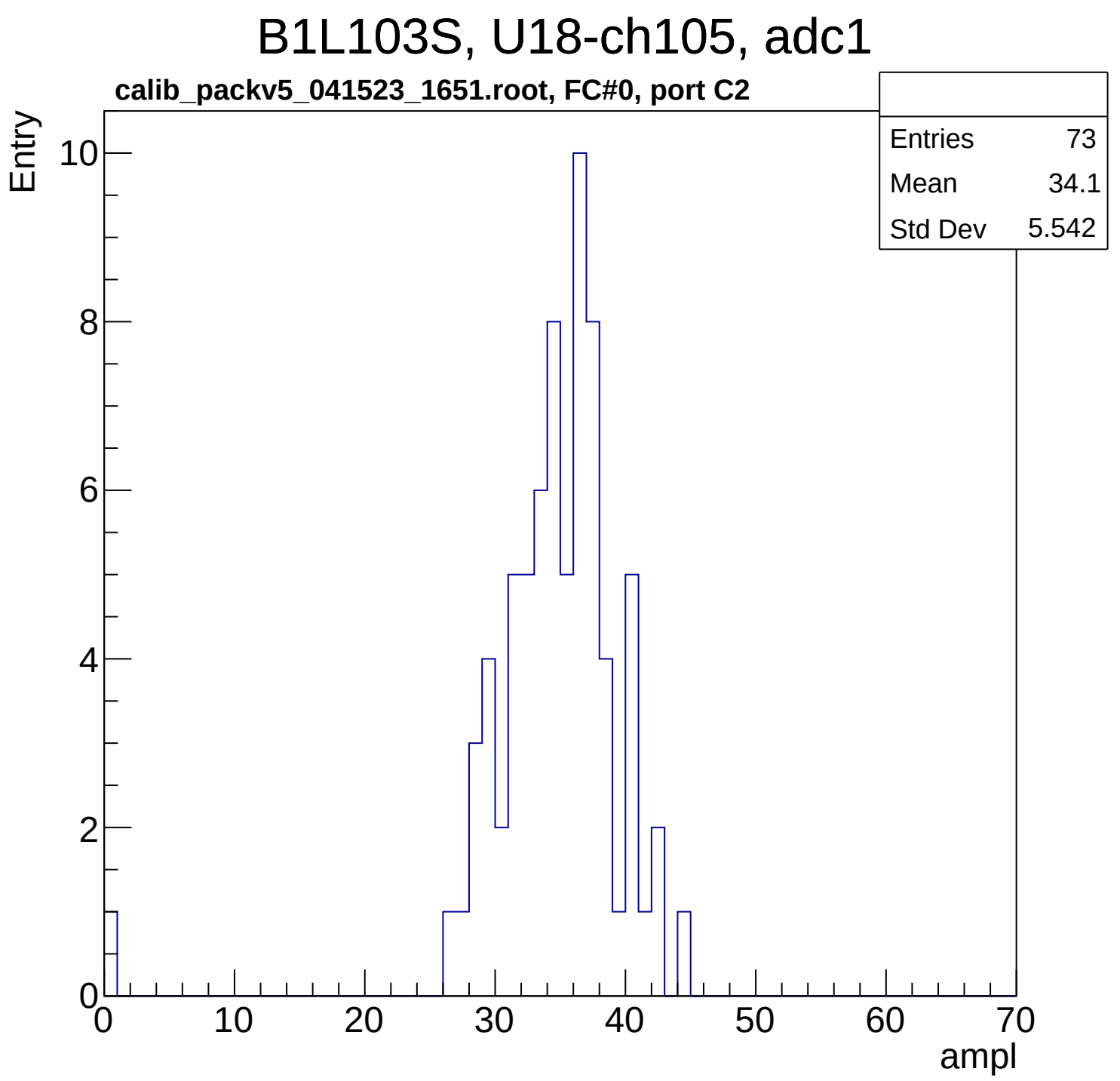
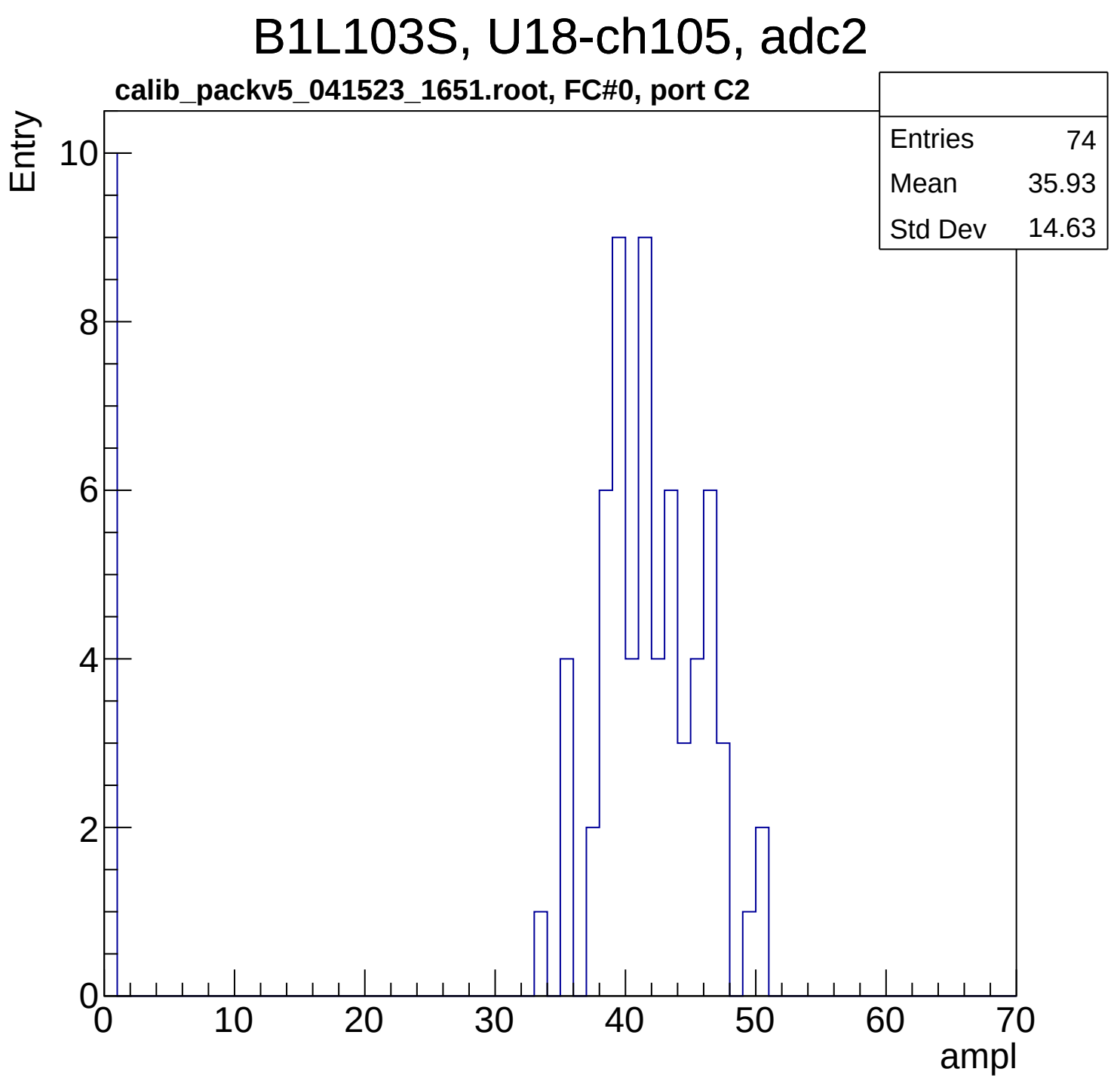
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

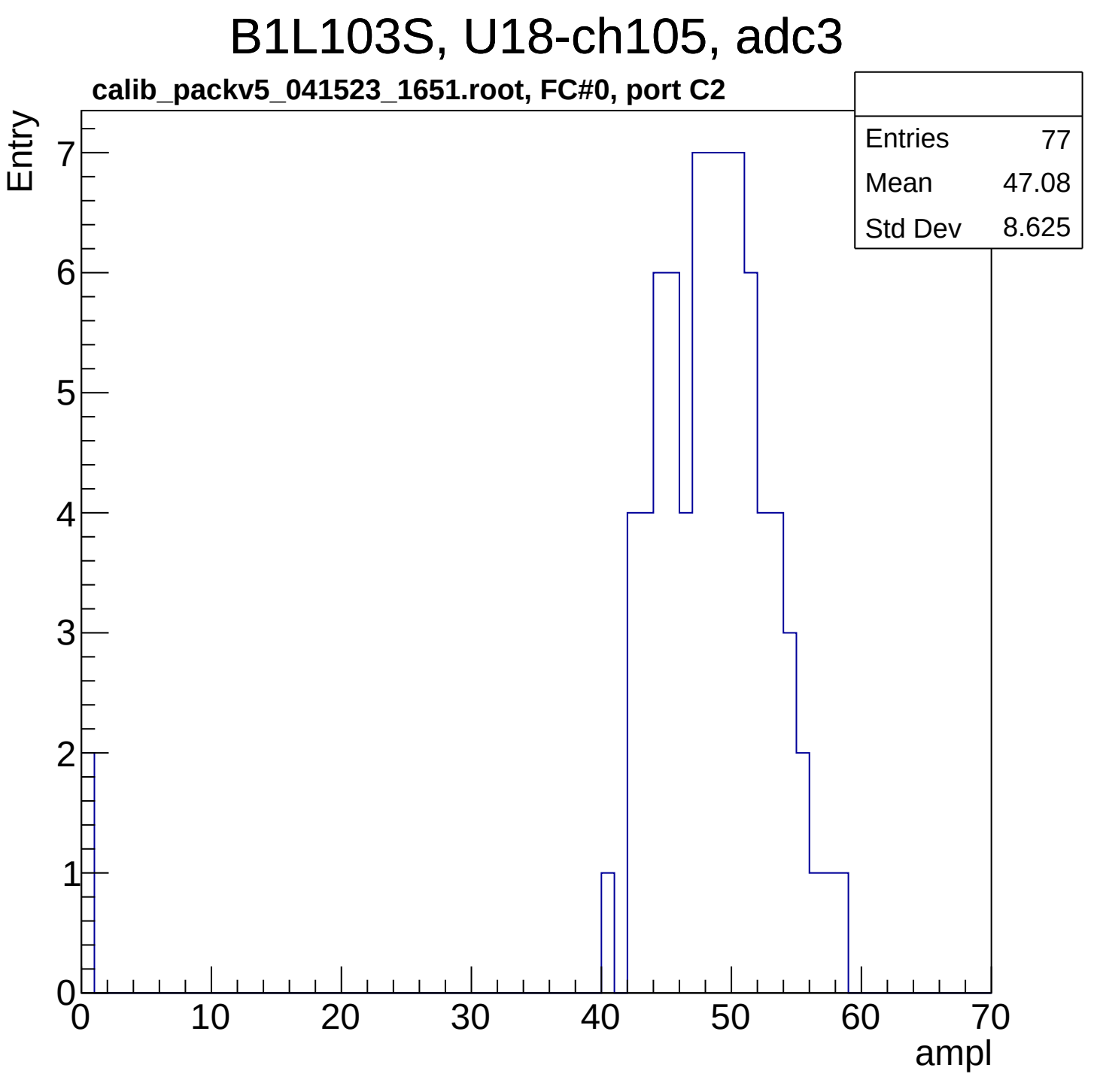

B1L103S, U18-ch104, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 60.61
Std Dev 2.059
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U18-ch104, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.1
Std Dev 13.51
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch105, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 94
Mean 20.39
Std Dev 12.38
Entry
ampl
0
5
10
15
20
25
0
10
20
30
40
50
60
70


B1L103S, U18-ch105, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 34.1
Std Dev 5.542
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch105, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 35.93
Std Dev 14.63
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U18-ch105, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 47.08
Std Dev 8.625
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
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60
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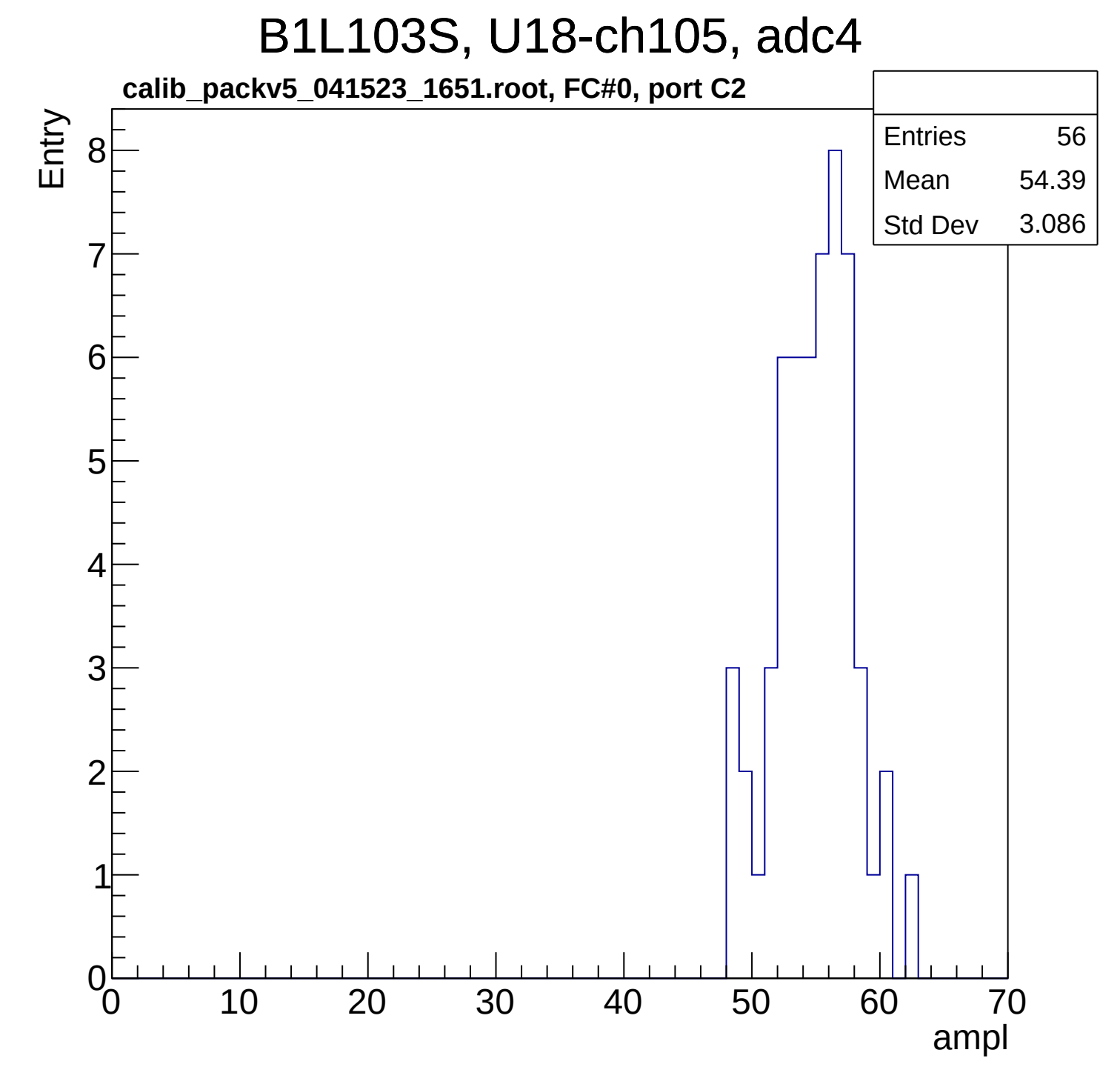
B1L103S, U18-ch105, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 54.39
Std Dev 3.086
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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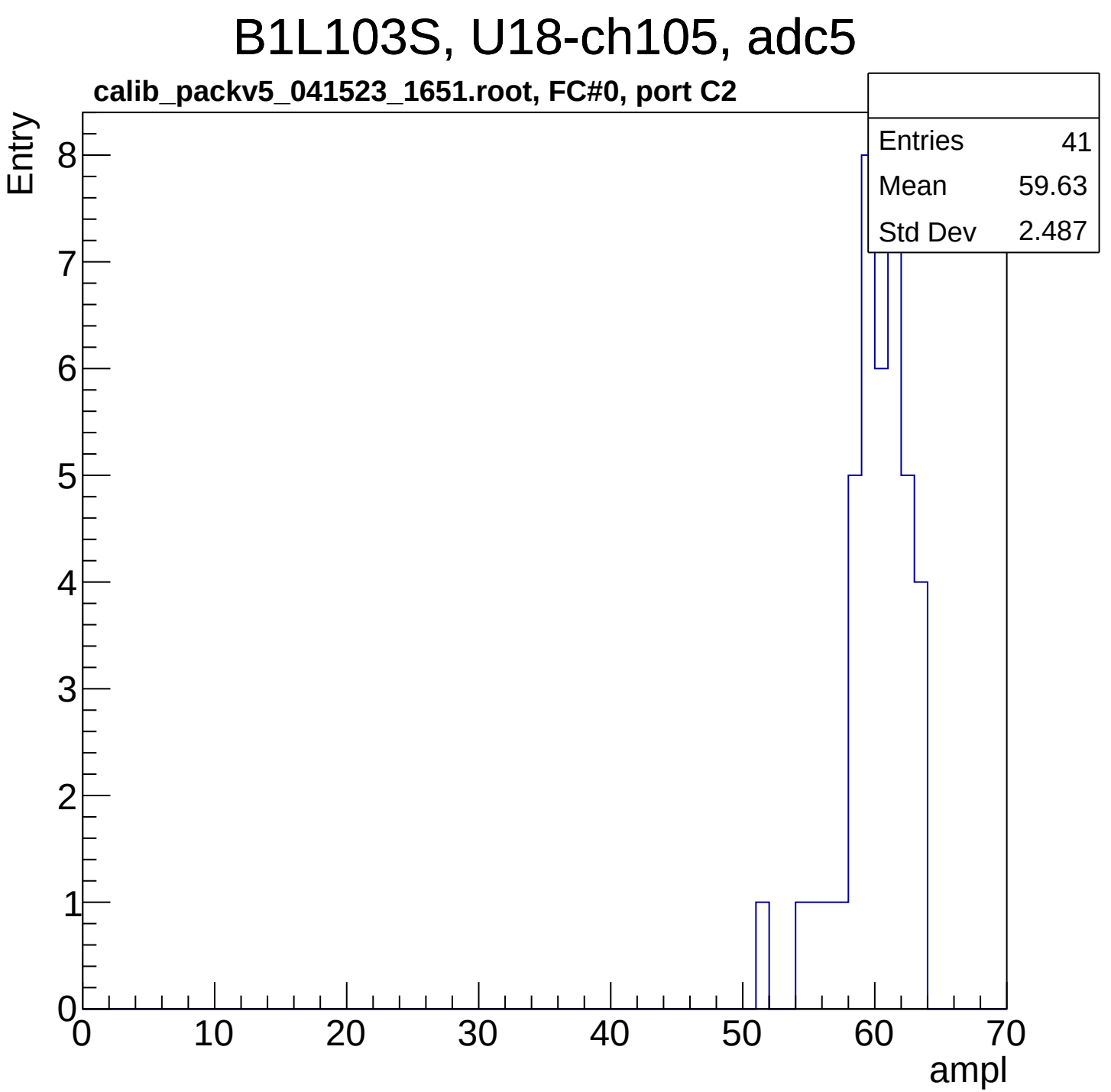
B1L103S, U18-ch105, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 41
Mean 59.63
Std Dev 2.487
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
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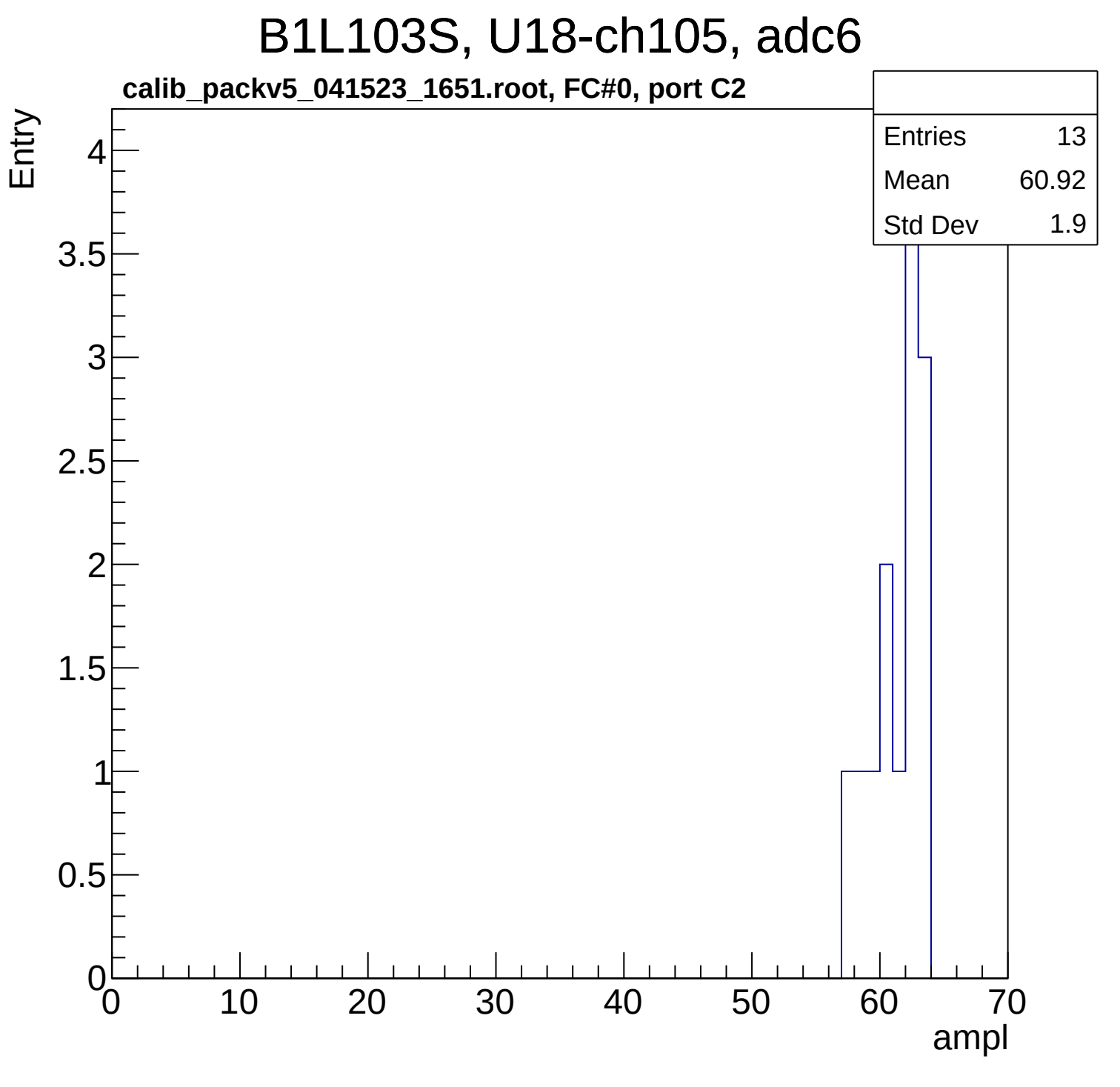
60
70


B1L103S, U18-ch105, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 13
Mean 60.92
Std Dev 1.9
Entry
ampl
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0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
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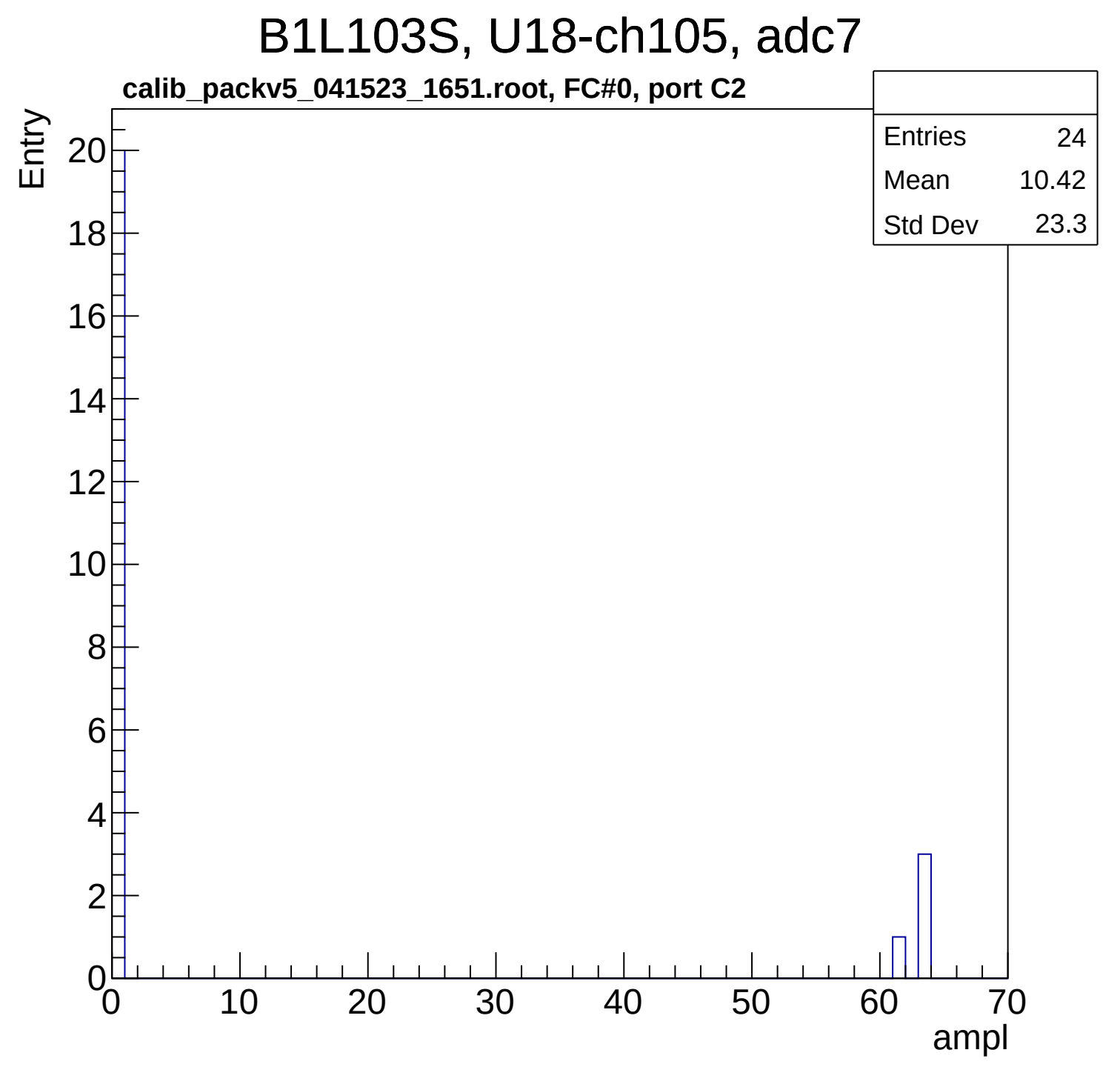
40
50
60
70


B1L103S, U18-ch105, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 24
Mean 10.42
Std Dev 23.3
Entry
ampl
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4
6
8
10
12
14
16
18
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0
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20
30
40
50
60
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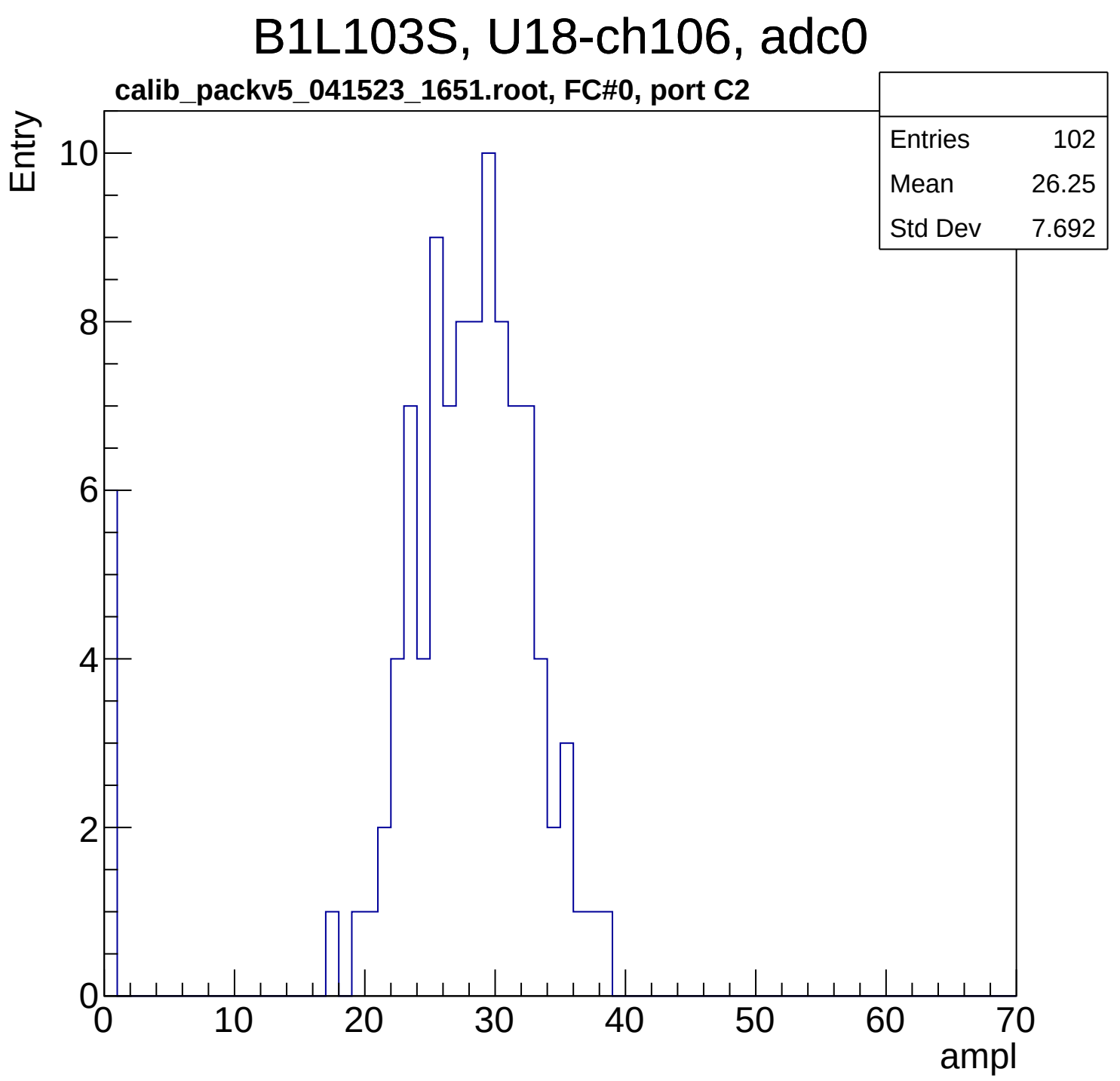
B1L103S, U18-ch106, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 102
Mean 26.25
Std Dev 7.692
Entry
ampl
0
2
4
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8
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0
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20
30
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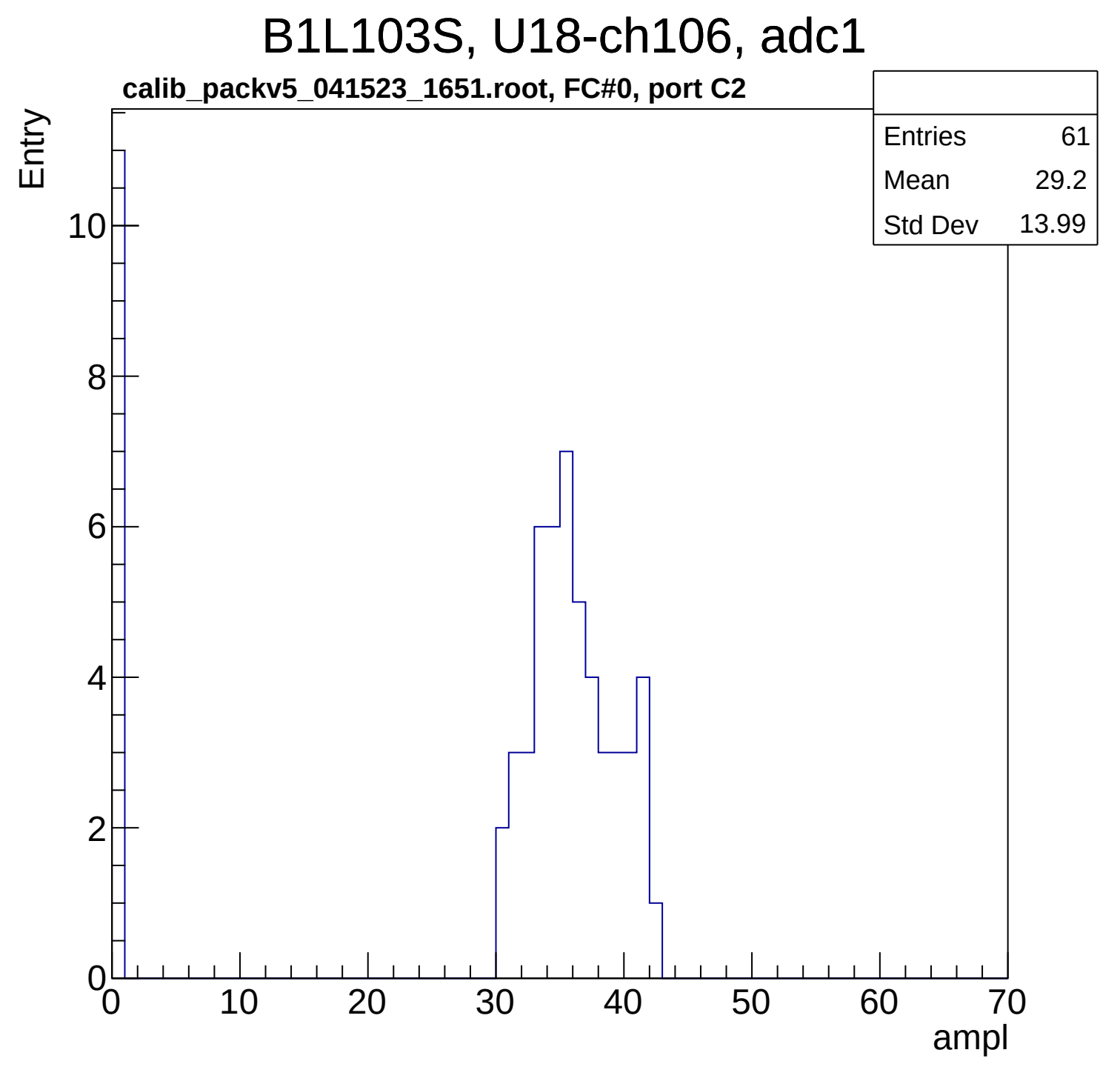
60
70


B1L103S, U18-ch106, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 29.2
Std Dev 13.99
Entry
0
2
4
6
8
10
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10
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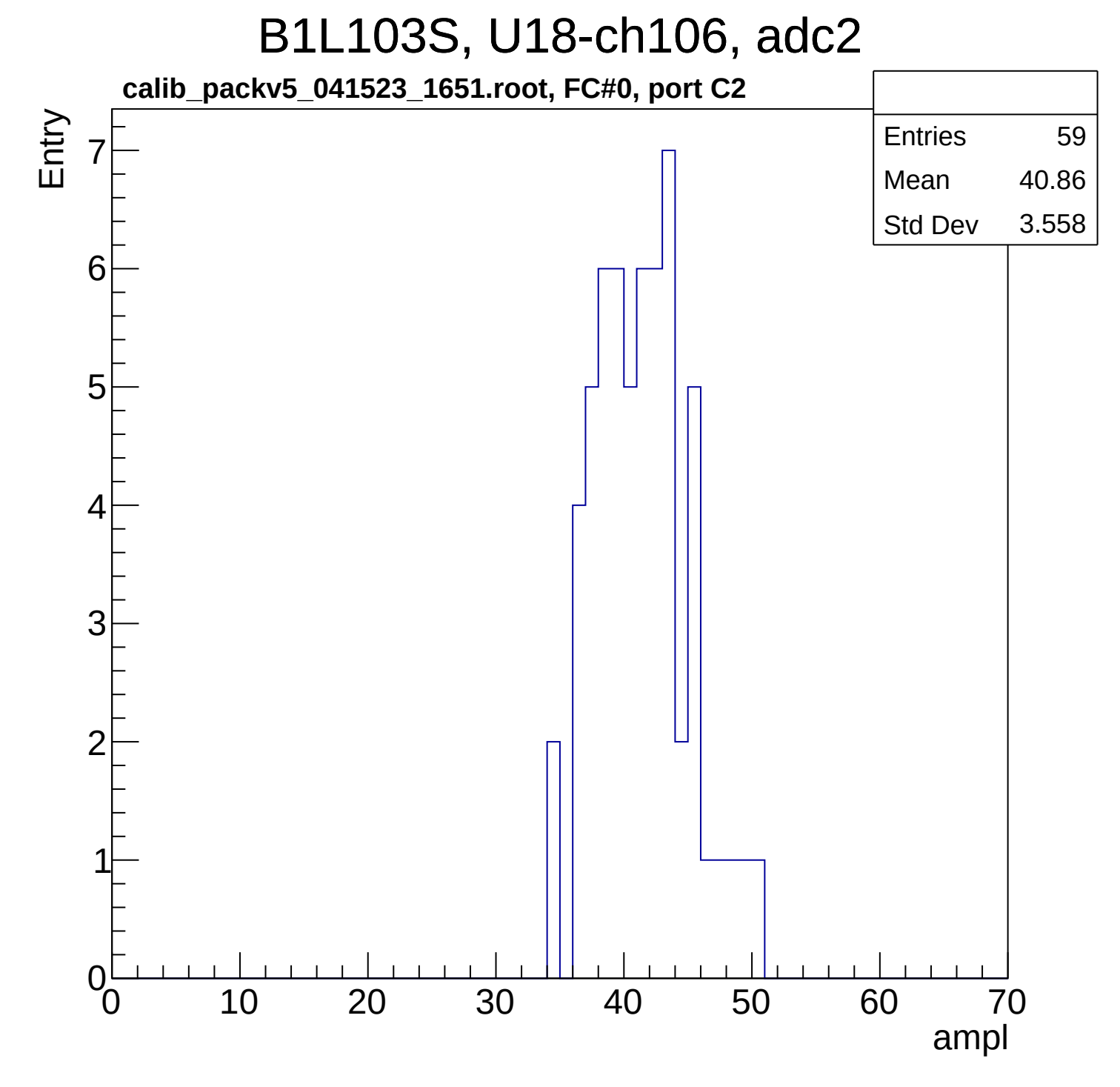
30
40
50
60
70
ampl


B1L103S, U18-ch106, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 40.86
Std Dev 3.558
Entry
ampl
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2
3
4
5
6
7
0
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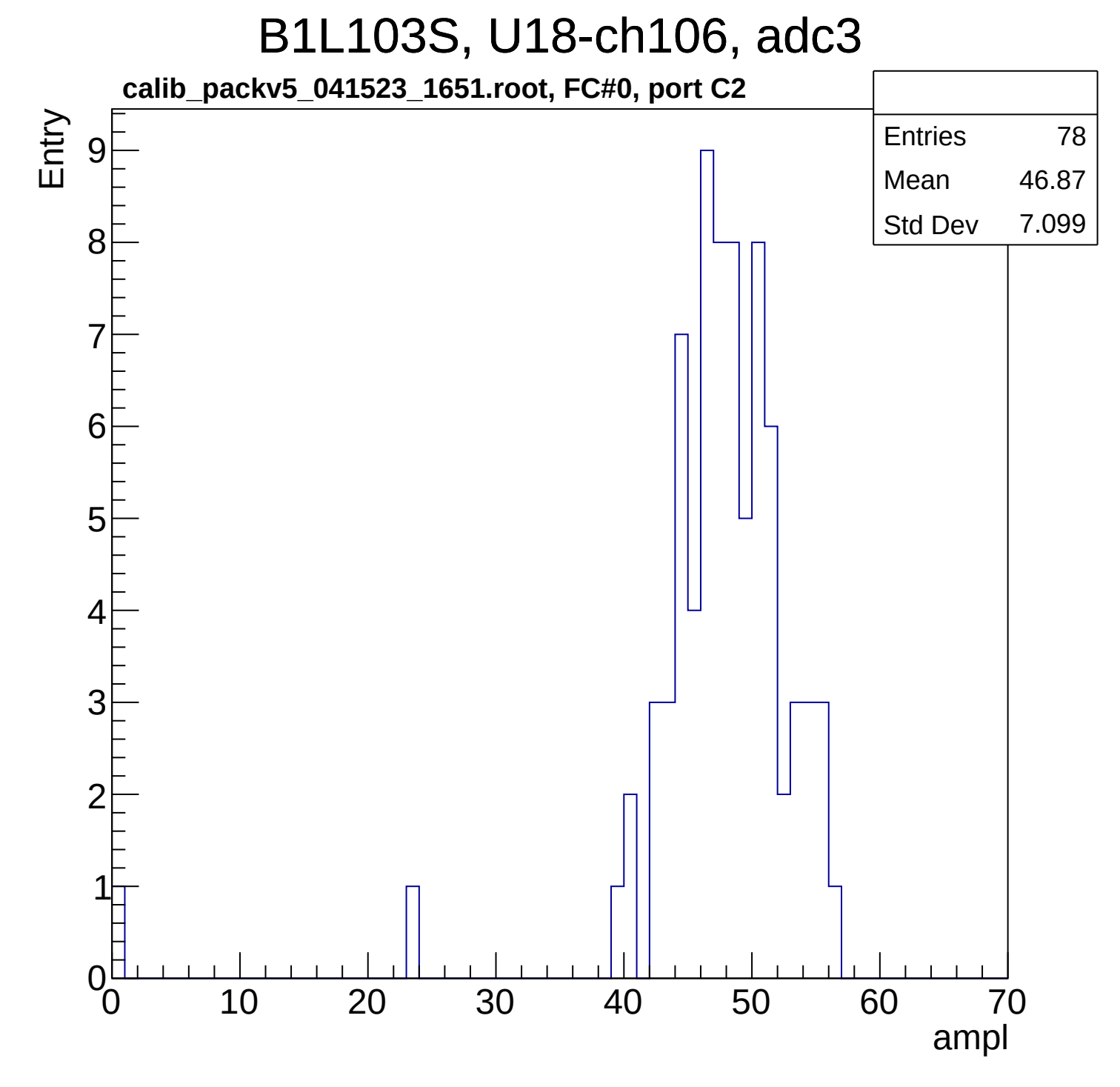
40
50
60
70


B1L103S, U18-ch106, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 46.87
Std Dev 7.099
Entry
ampl
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2
3
4
5
6
7
8
9
0
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40
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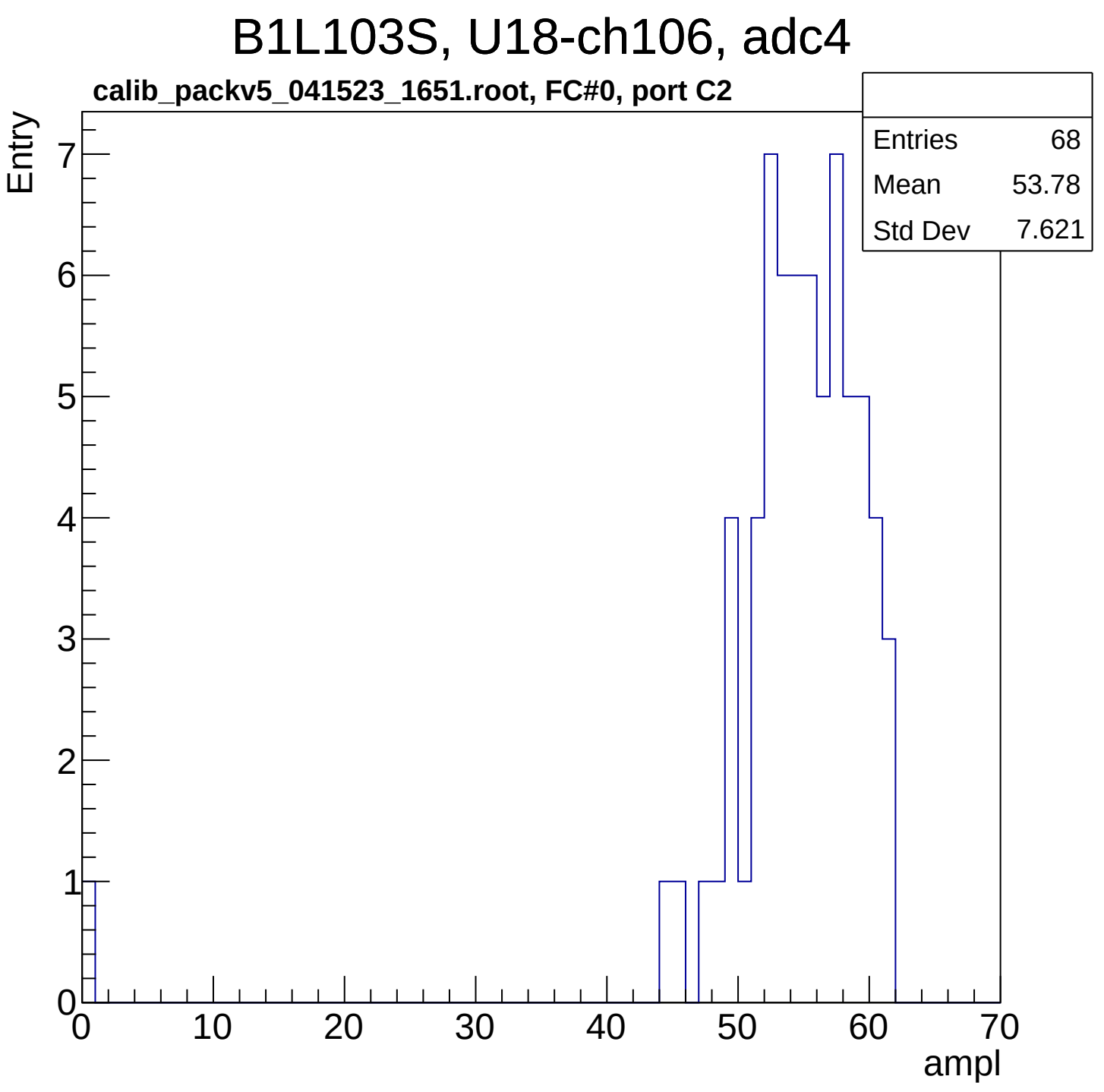
60
70


B1L103S, U18-ch106, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 53.78
Std Dev 7.621
Entry
ampl
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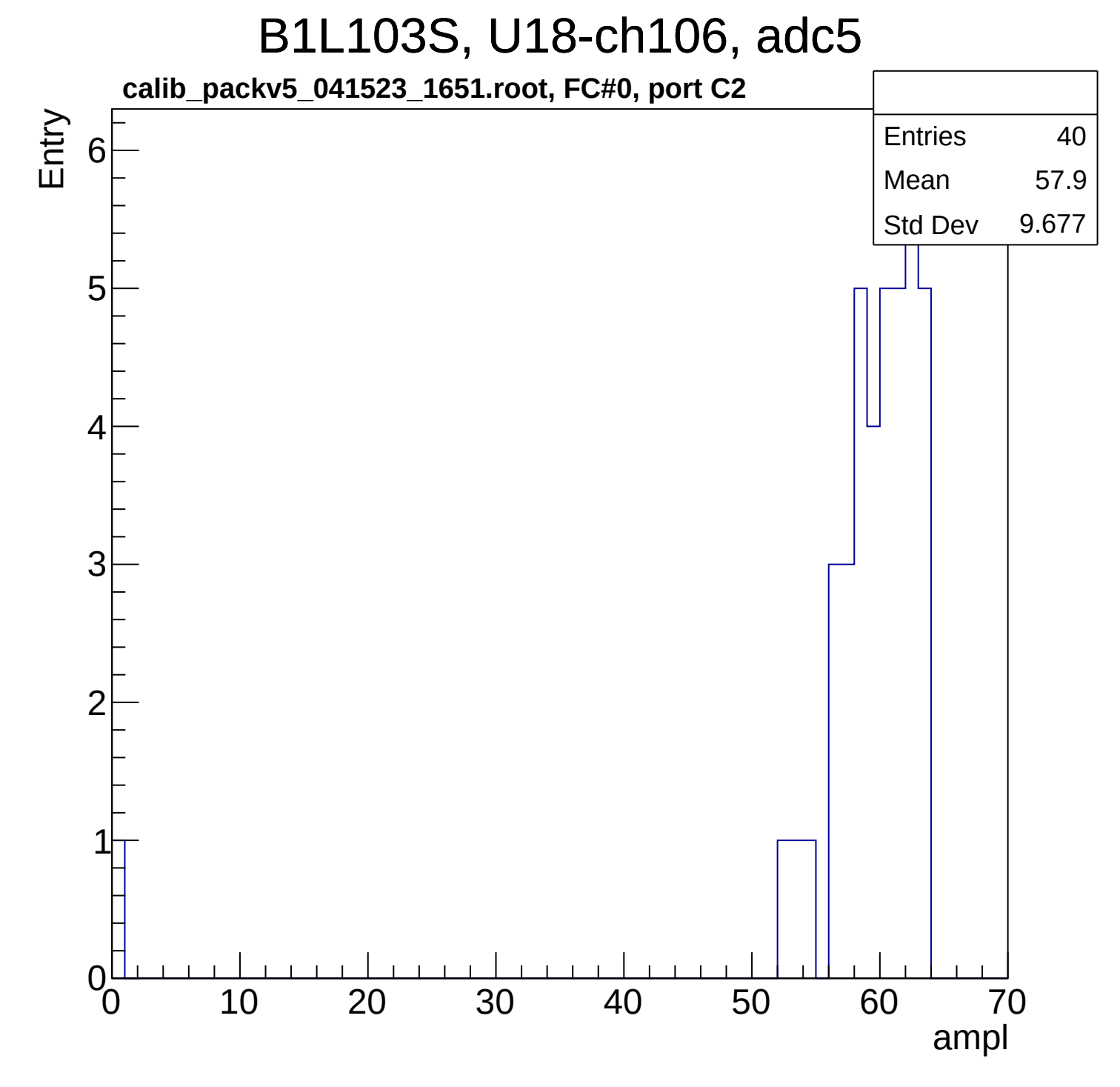
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U18-ch106, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 40
Mean 57.9
Std Dev 9.677
Entry
ampl
0
1
2
3
4
5
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0
10
20
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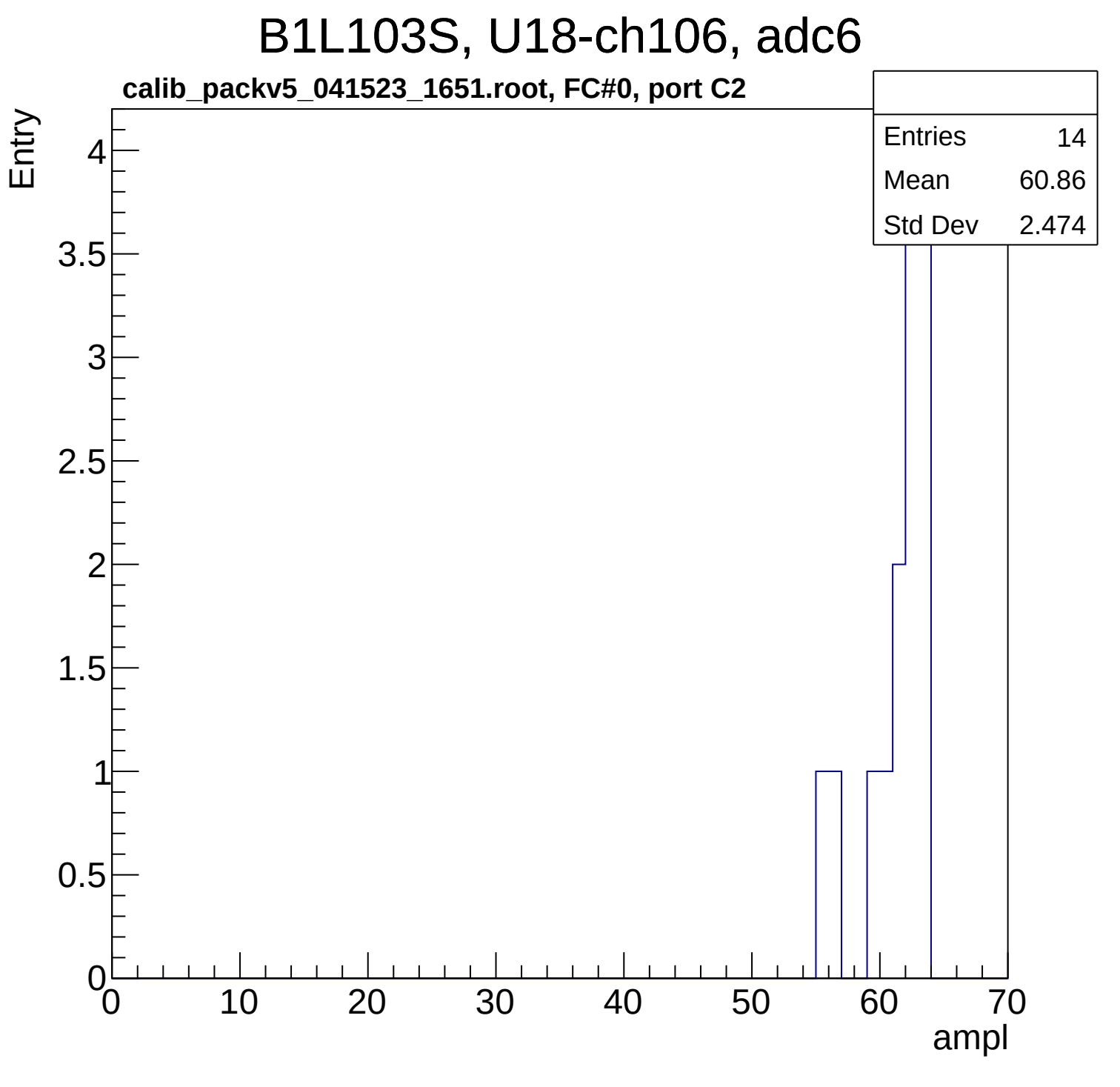
40
50
60
70


B1L103S, U18-ch106, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 14
Mean 60.86
Std Dev 2.474
Entry
ampl
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1.5
2
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3
3.5
4
0
10
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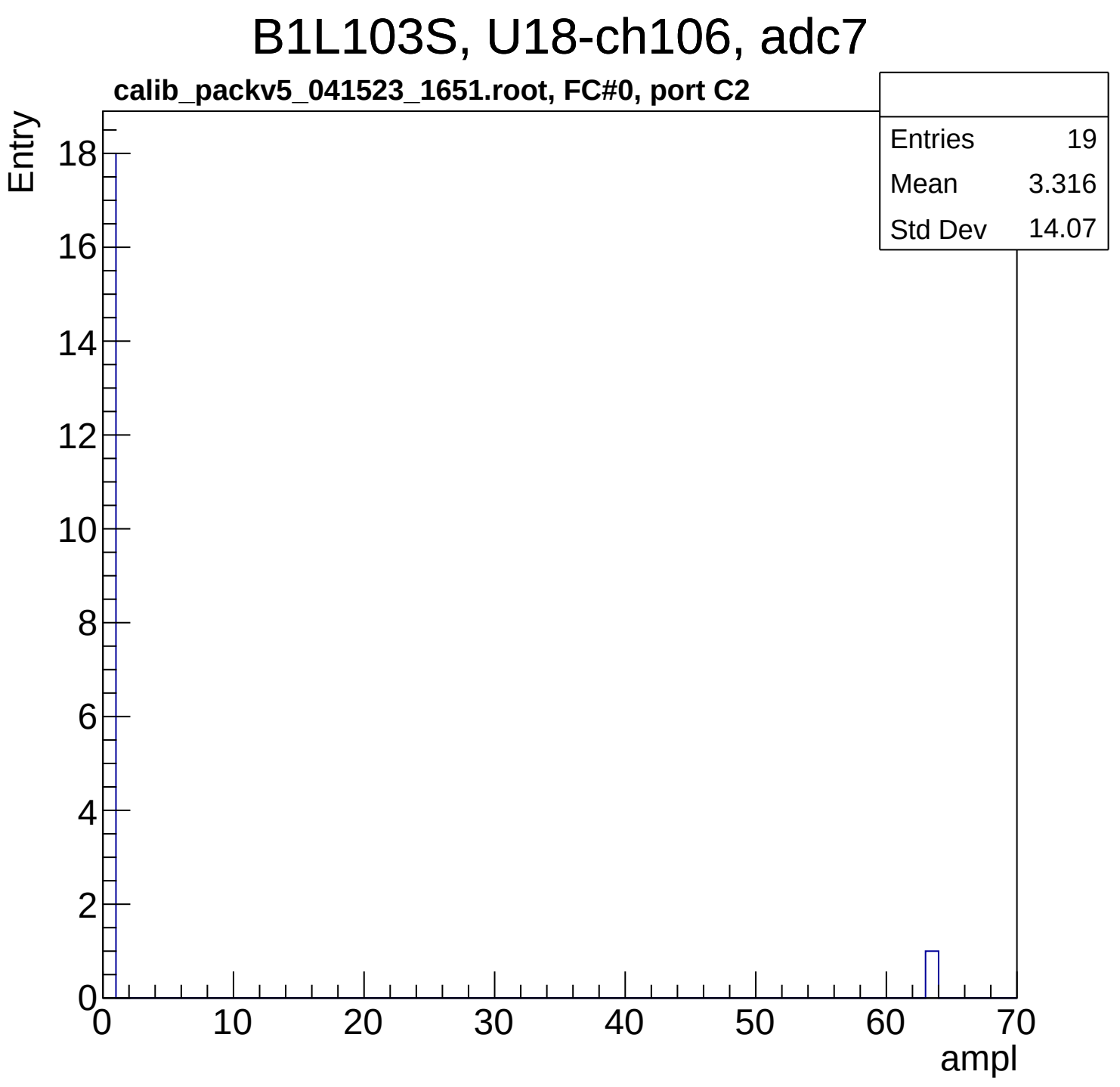
40
50
60
70


B1L103S, U18-ch106, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 3.316
Std Dev 14.07
Entry
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4
6
8
10
12
14
16
18
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10
20
30
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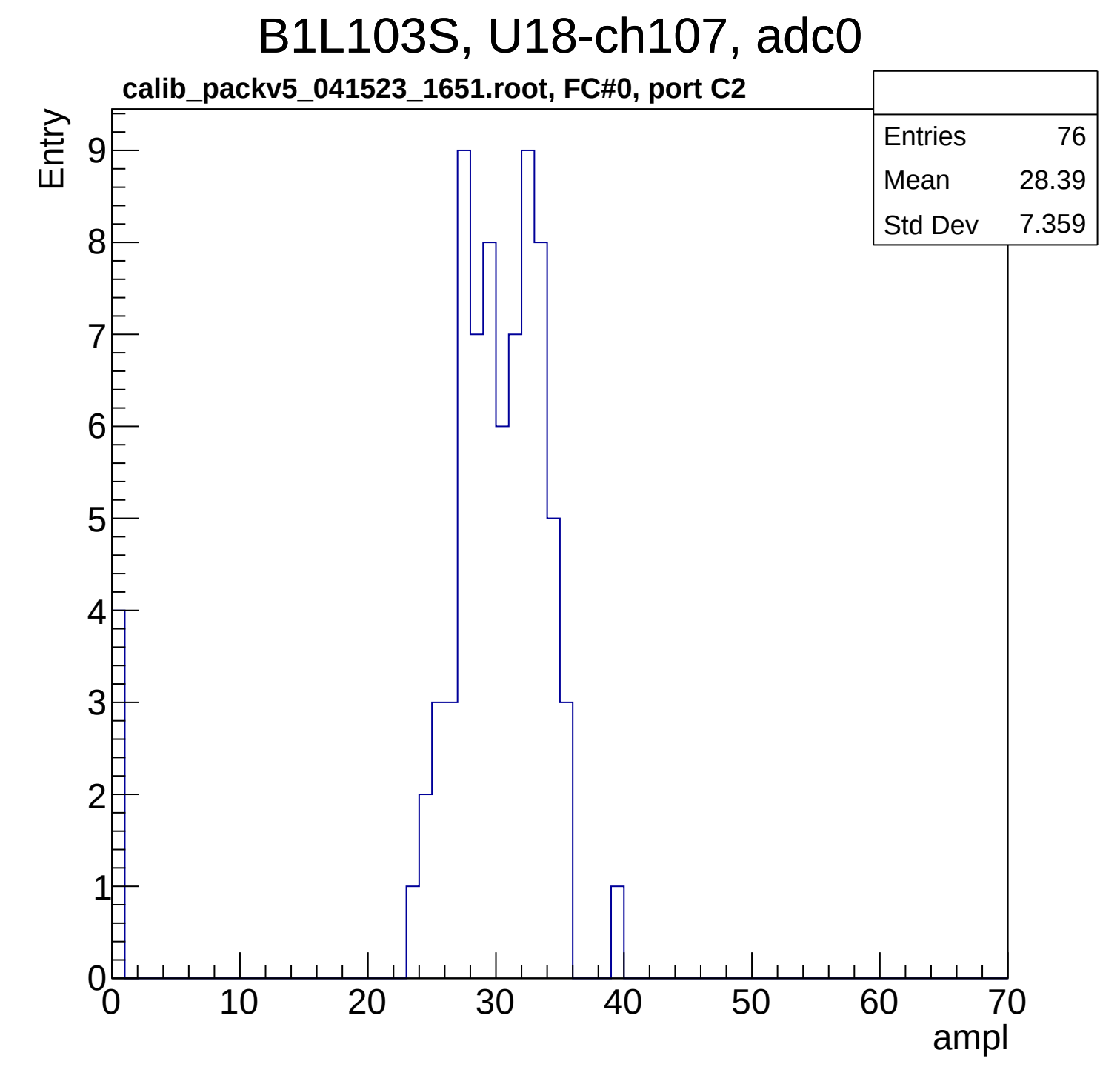
50
60
70
ampl


B1L103S, U18-ch107, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 28.39
Std Dev 7.359
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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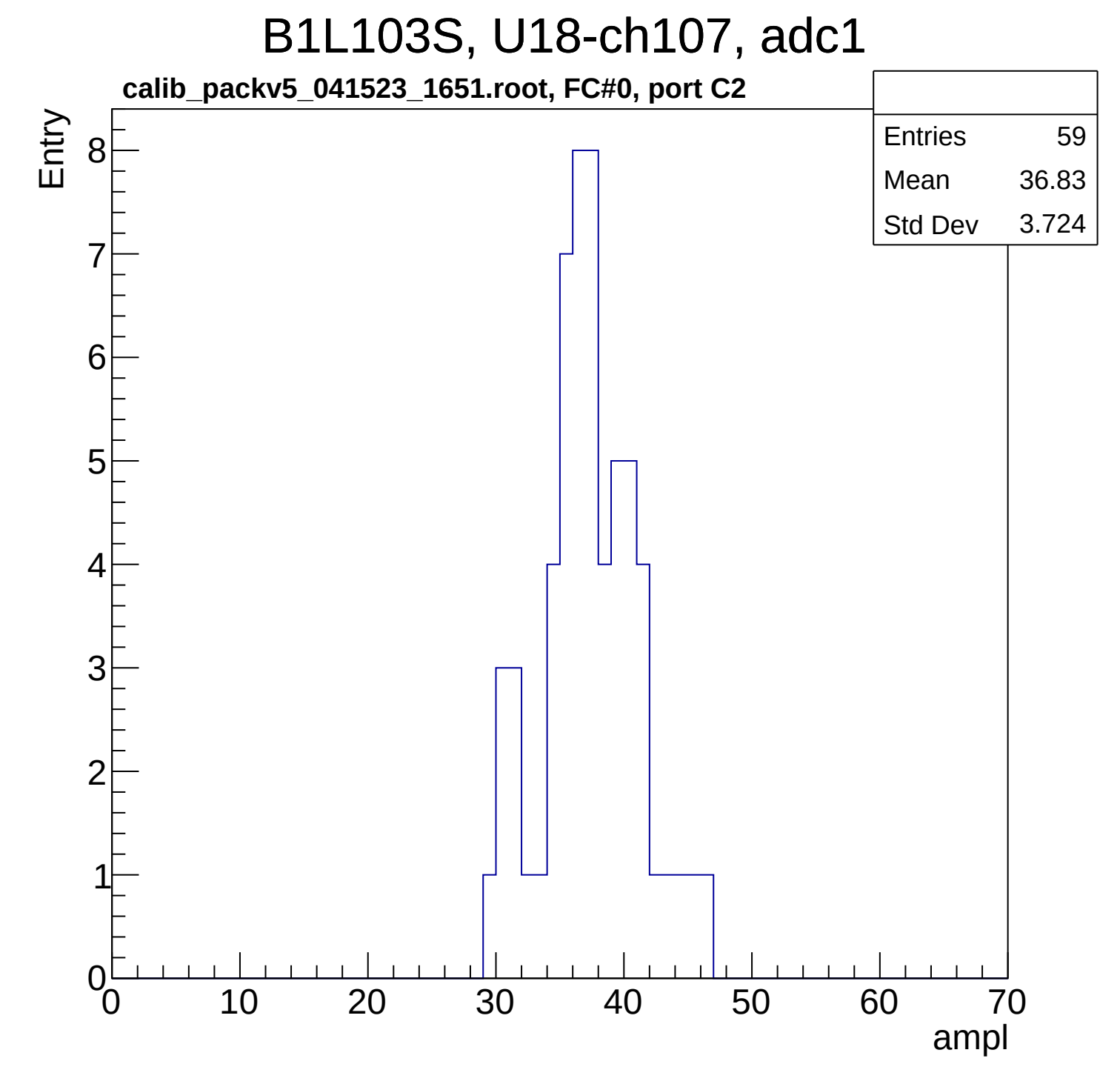
40
50
60
70


B1L103S, U18-ch107, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 36.83
Std Dev 3.724
Entry
ampl
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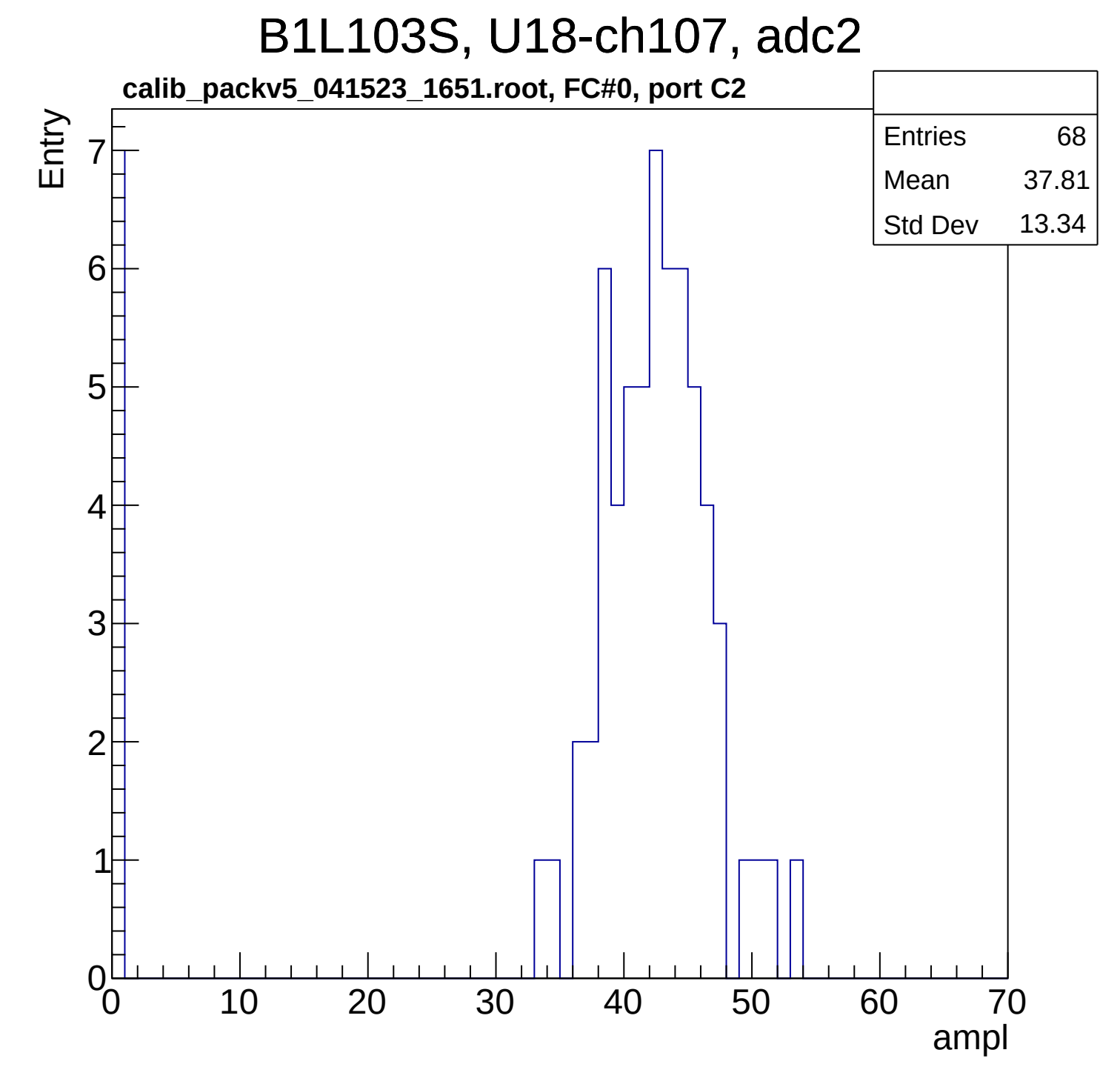
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch107, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 37.81
Std Dev 13.34
Entry
ampl
0
1
2
3
4
5
6
7
0
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20
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40
50
60
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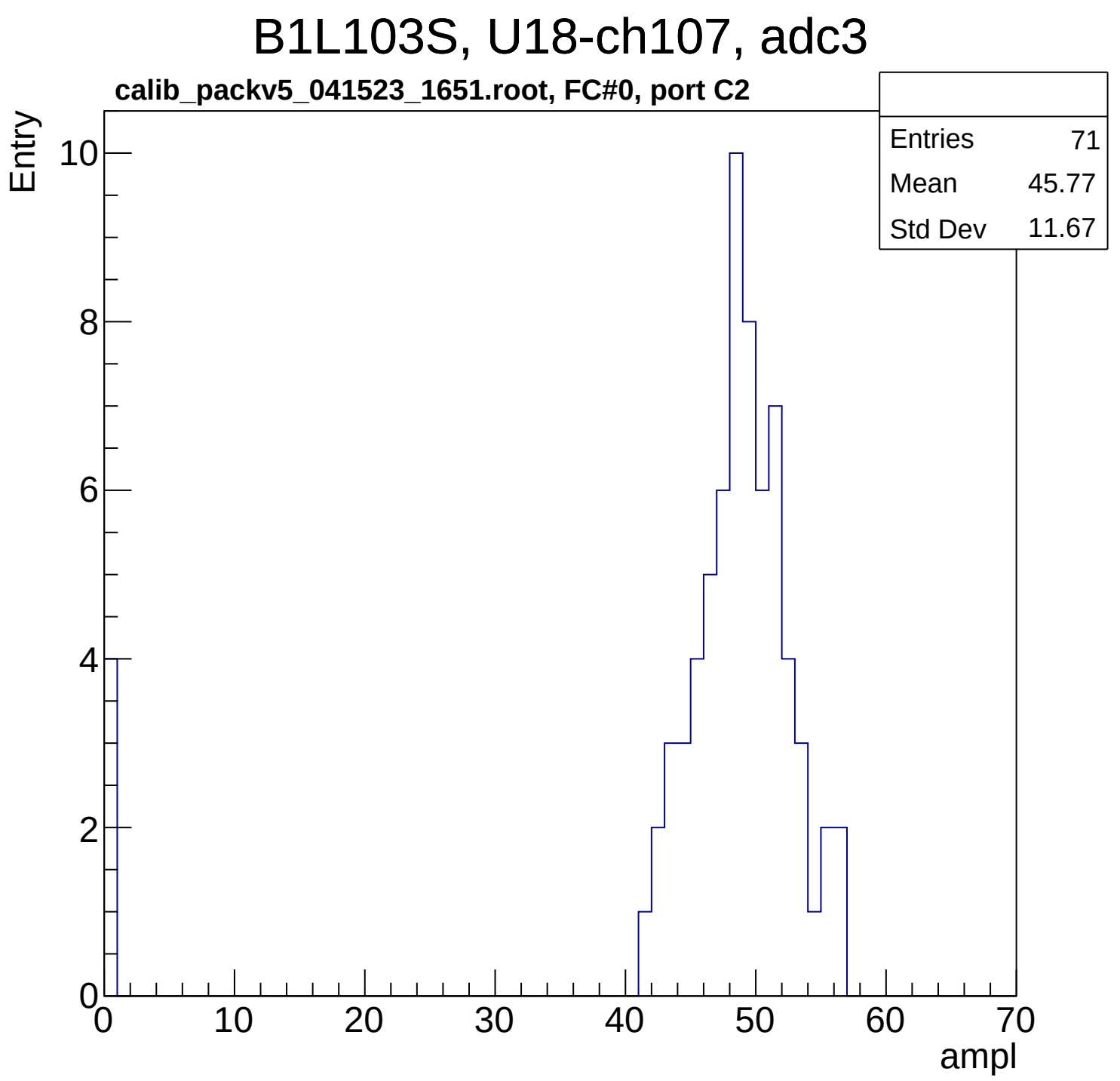
B1L103S, U18-ch107, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 45.77
Std Dev 11.67
Entry
ampl
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4
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0
10
20
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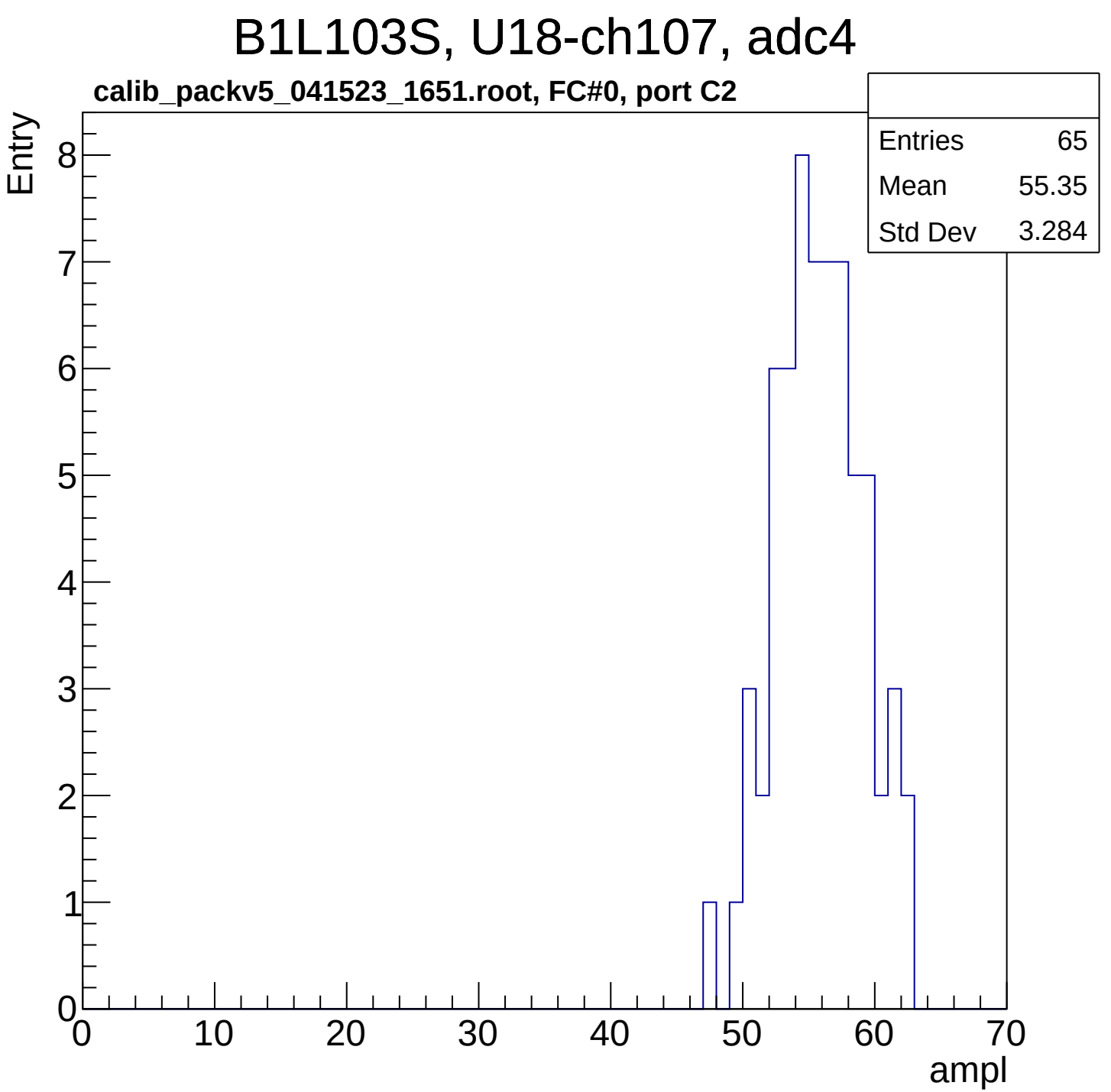
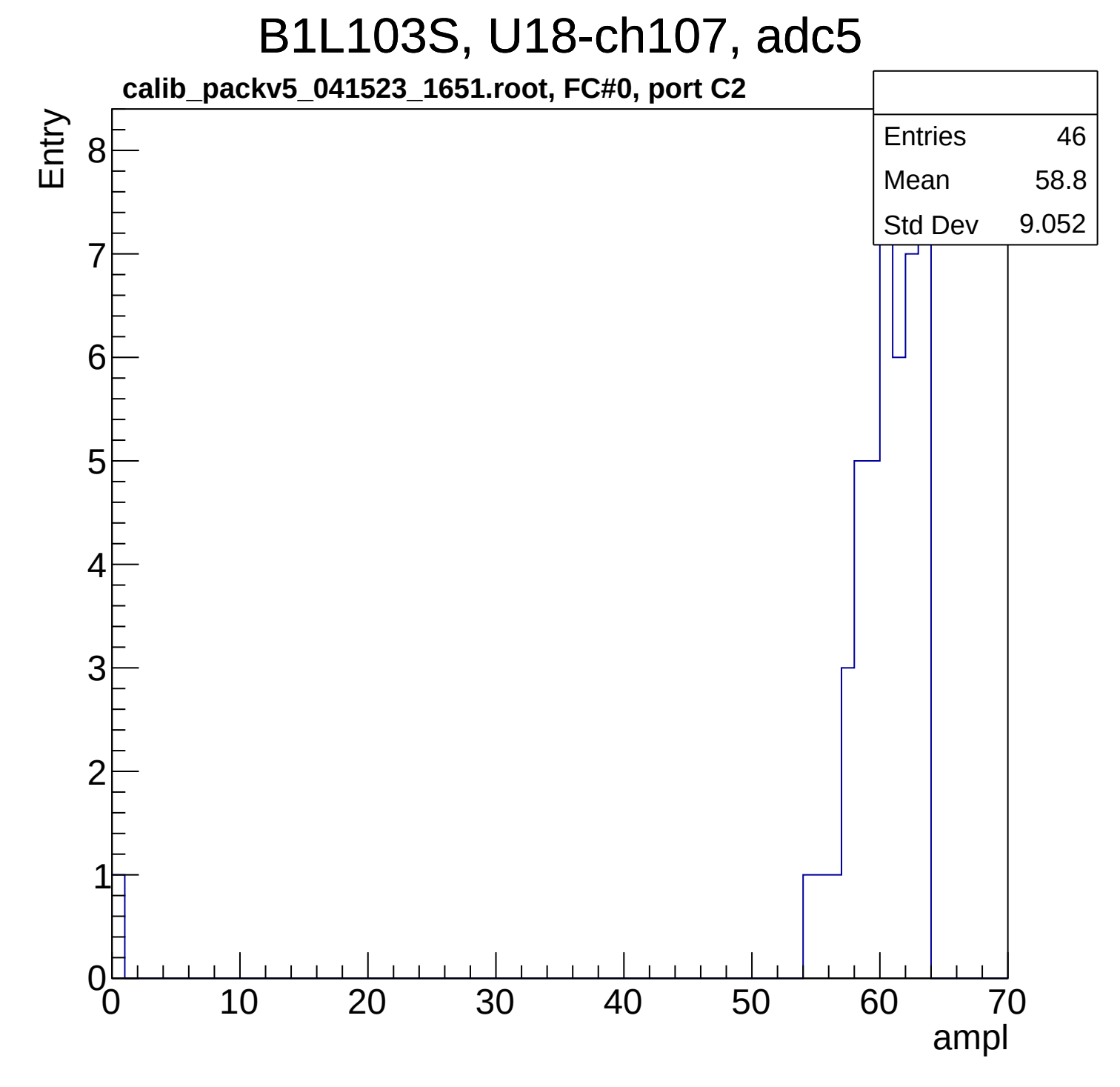
40
50
60
70


B1L103S, U18-ch107, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 55.35
Std Dev 3.284
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch107, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 58.8
Std Dev 9.052
Entry
ampl
0
1
2
3
4
5
6
7
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0
10
20
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40
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60
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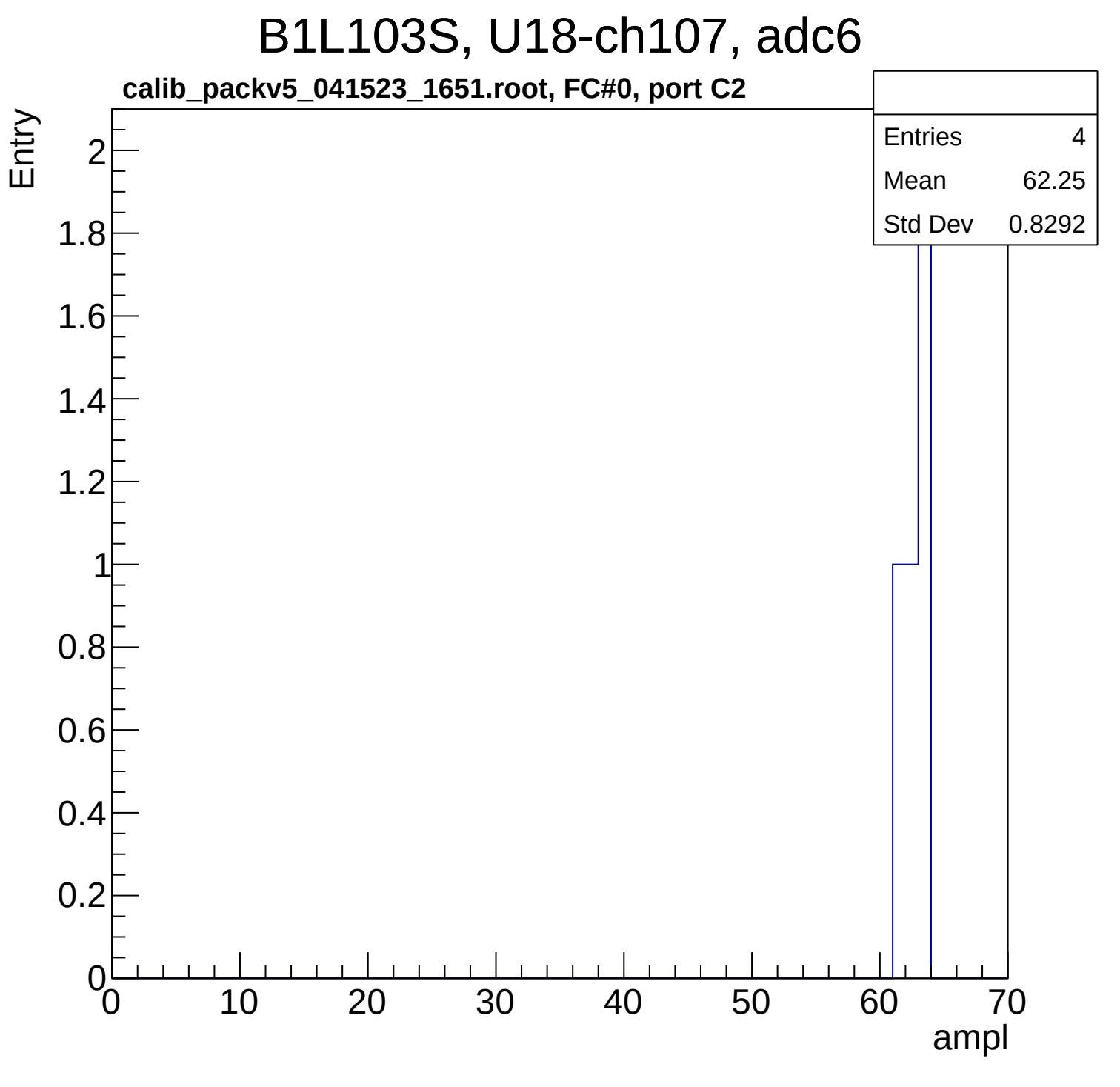
B1L103S, U18-ch107, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 4
Mean 62.25
Std Dev 0.8292
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
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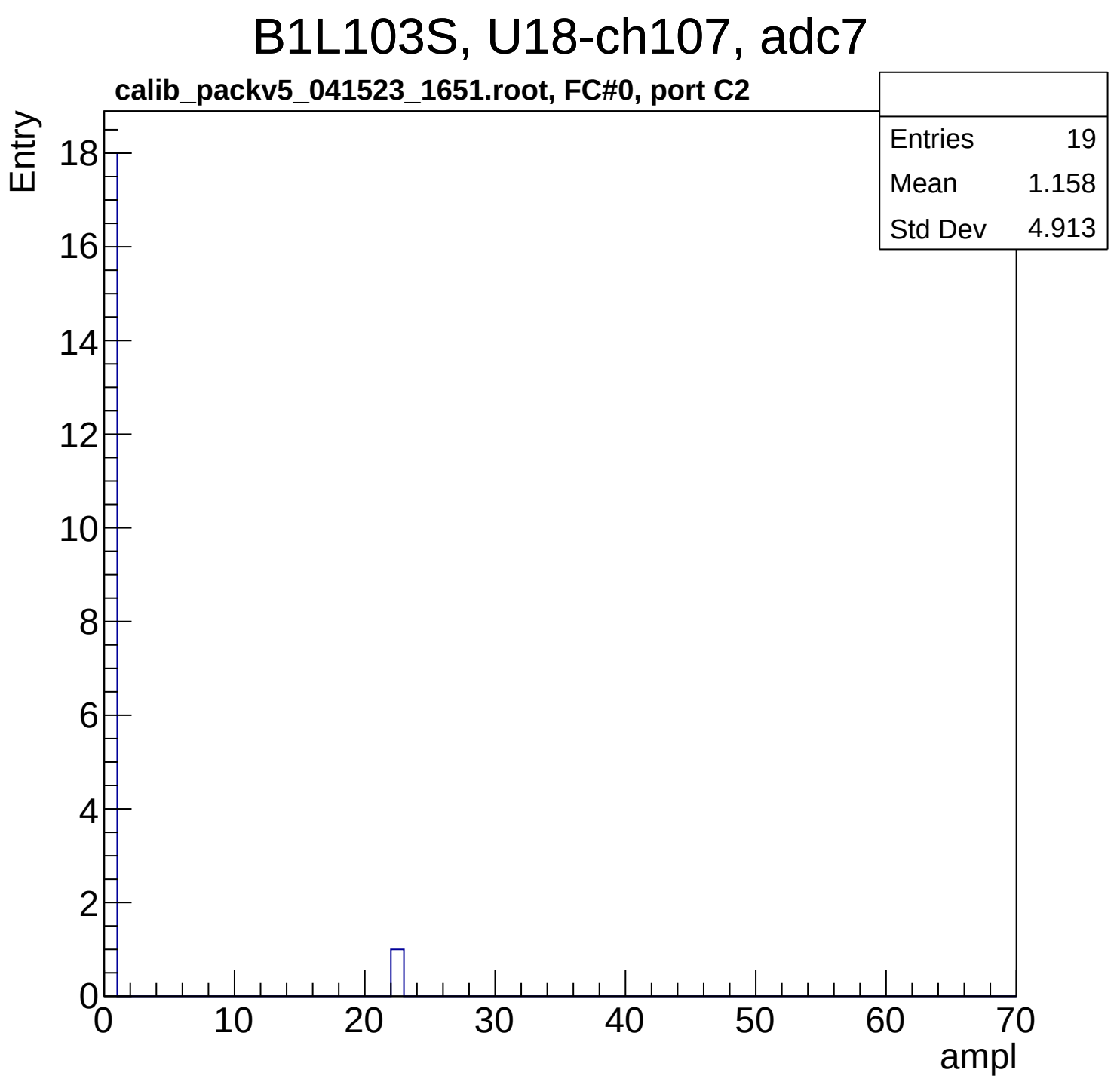
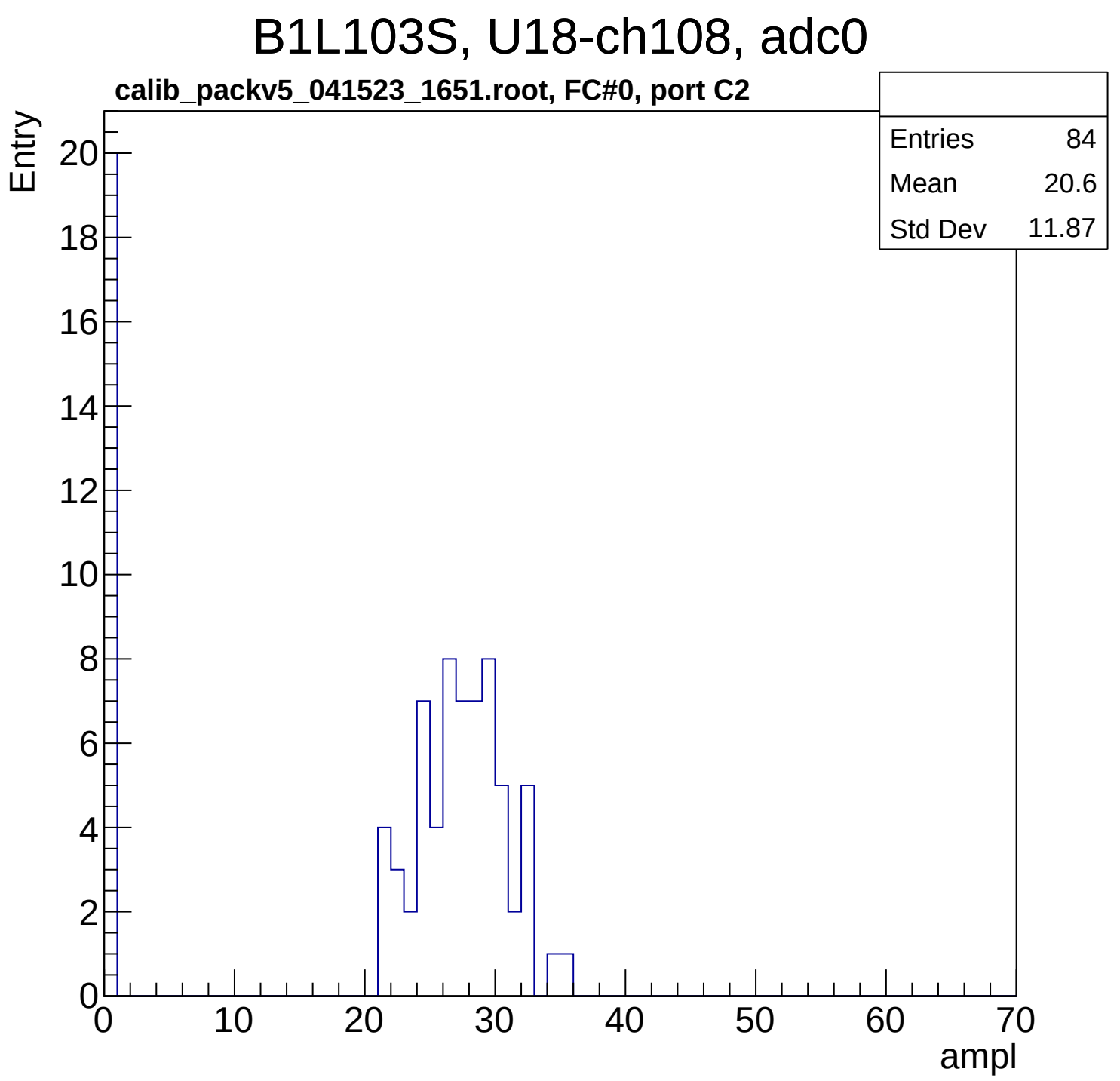

B1L103S, U18-ch107, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.158
Std Dev 4.913
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch108, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 20.6
Std Dev 11.87
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
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40
50
60
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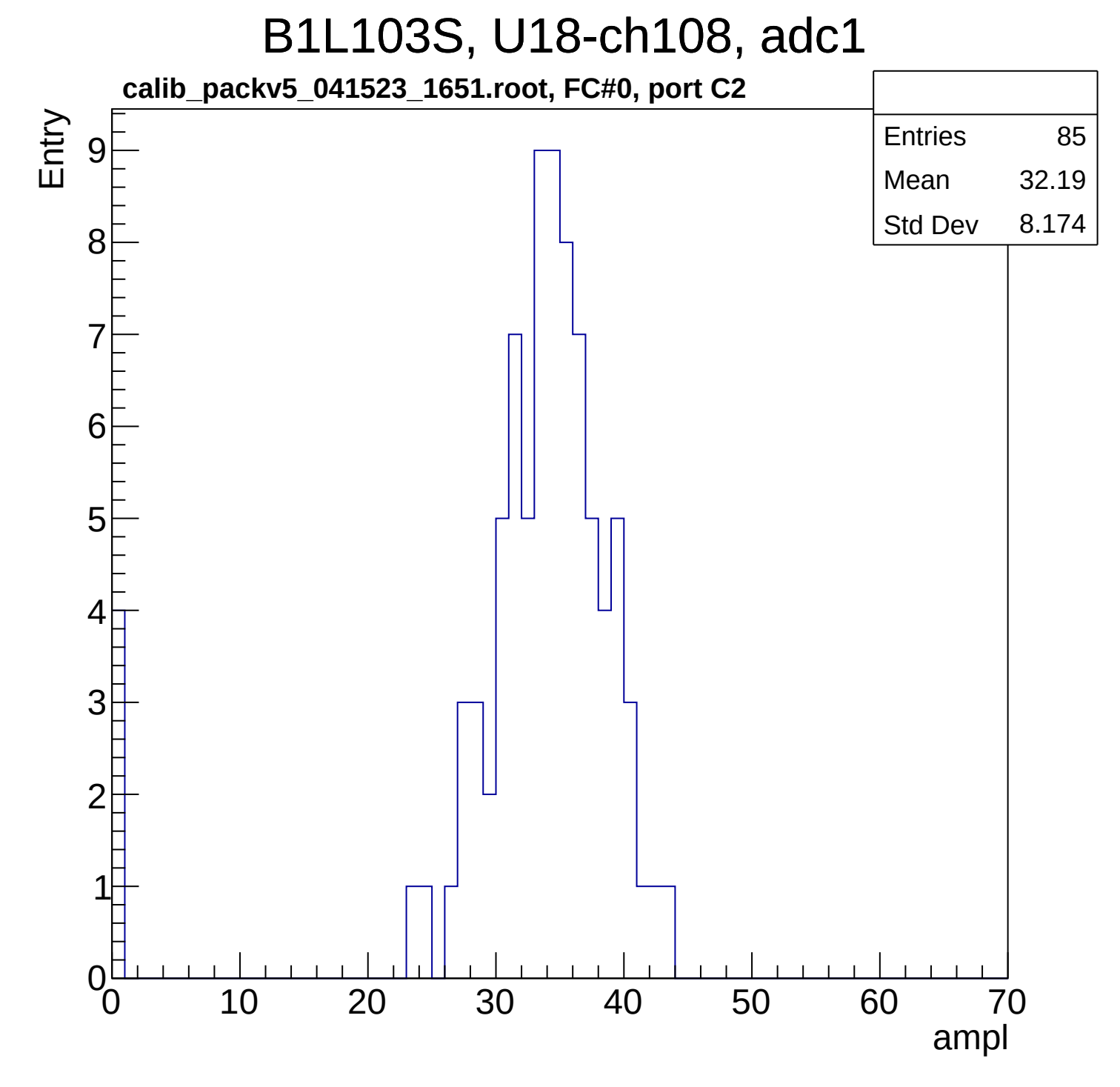
B1L103S, U18-ch108, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 32.19
Std Dev 8.174
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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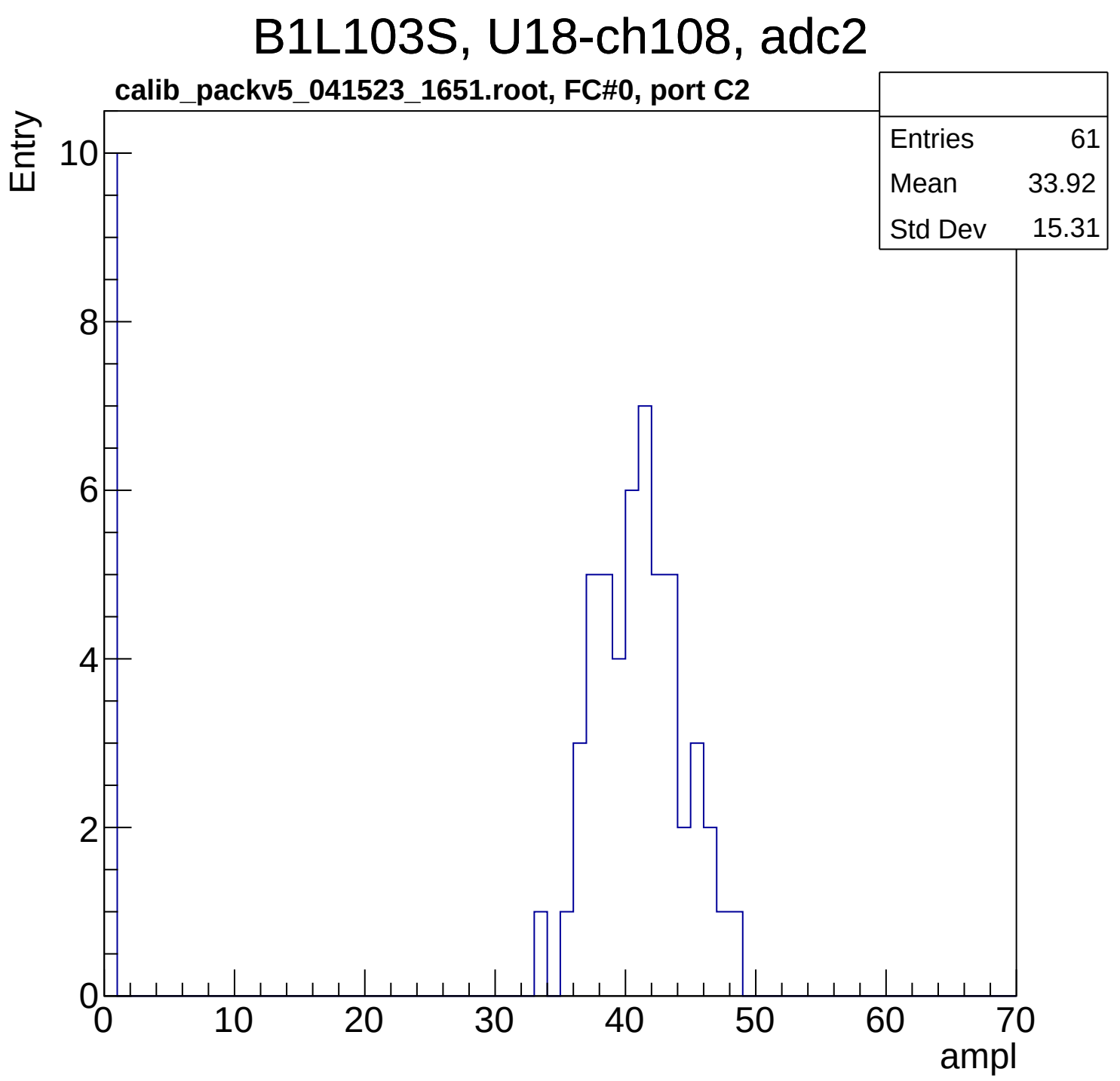
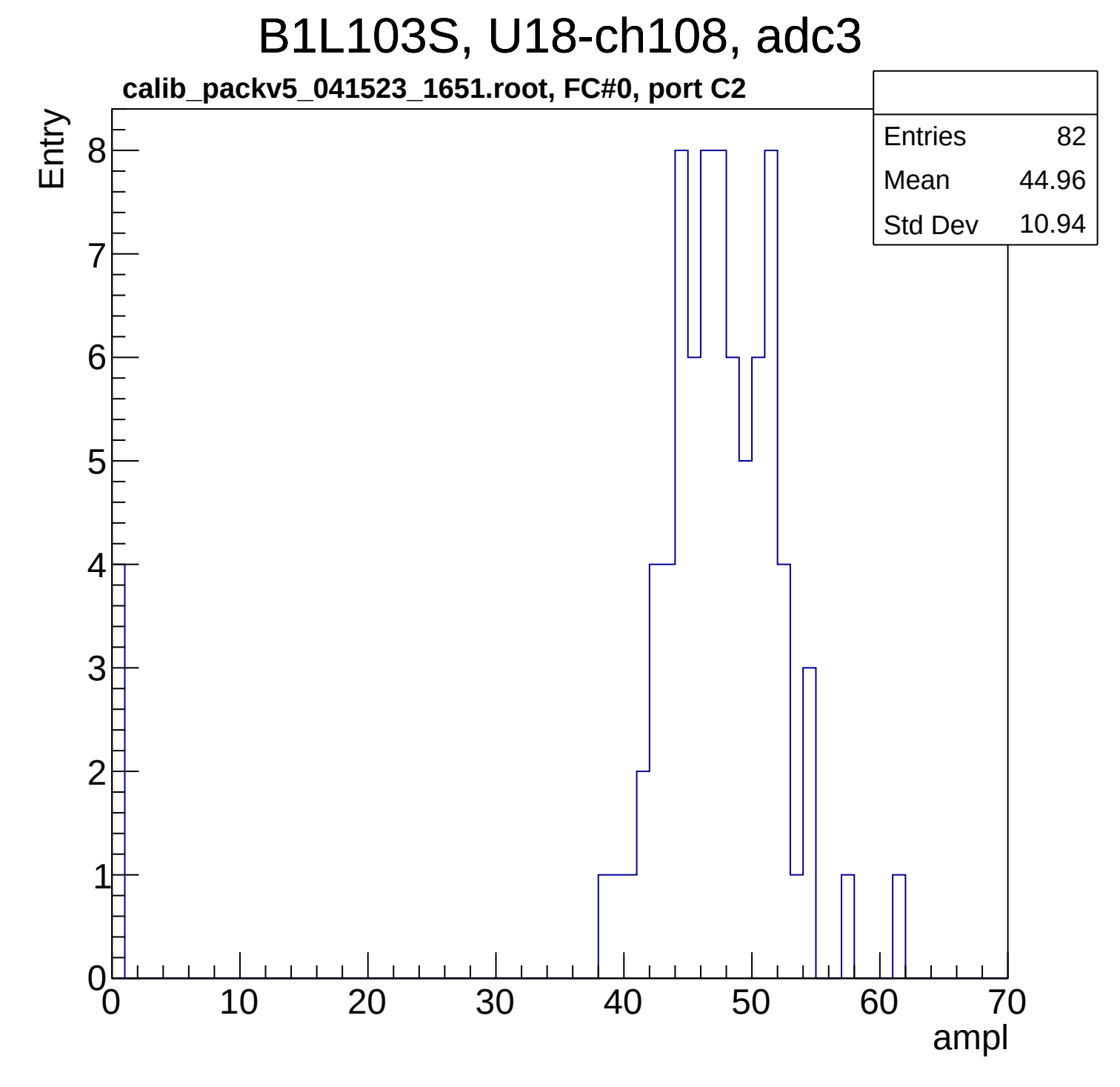

B1L103S, U18-ch108, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 33.92
Std Dev 15.31
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U18-ch108, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 44.96
Std Dev 10.94
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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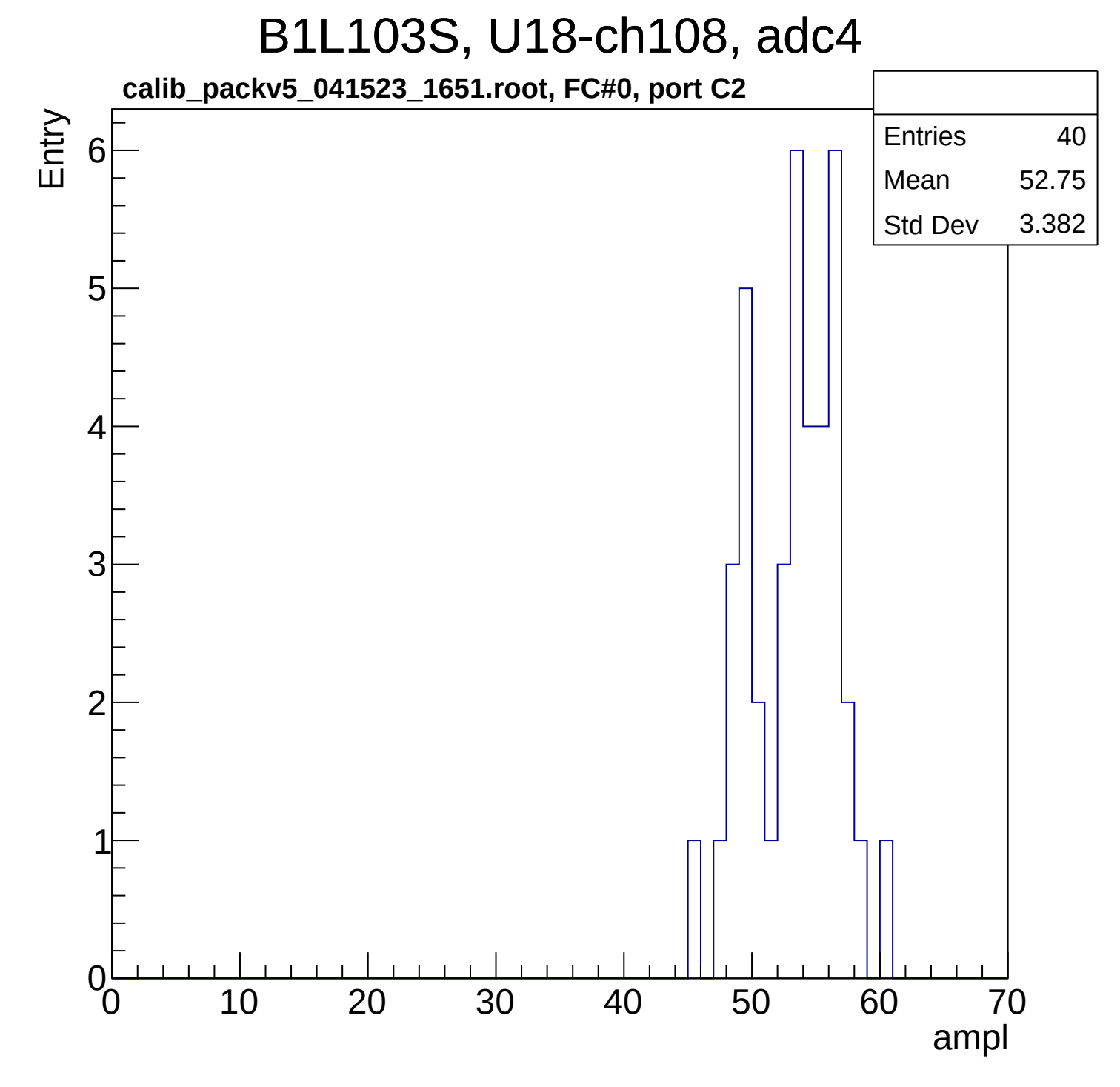
B1L103S, U18-ch108, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 40
Mean 52.75
Std Dev 3.382
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
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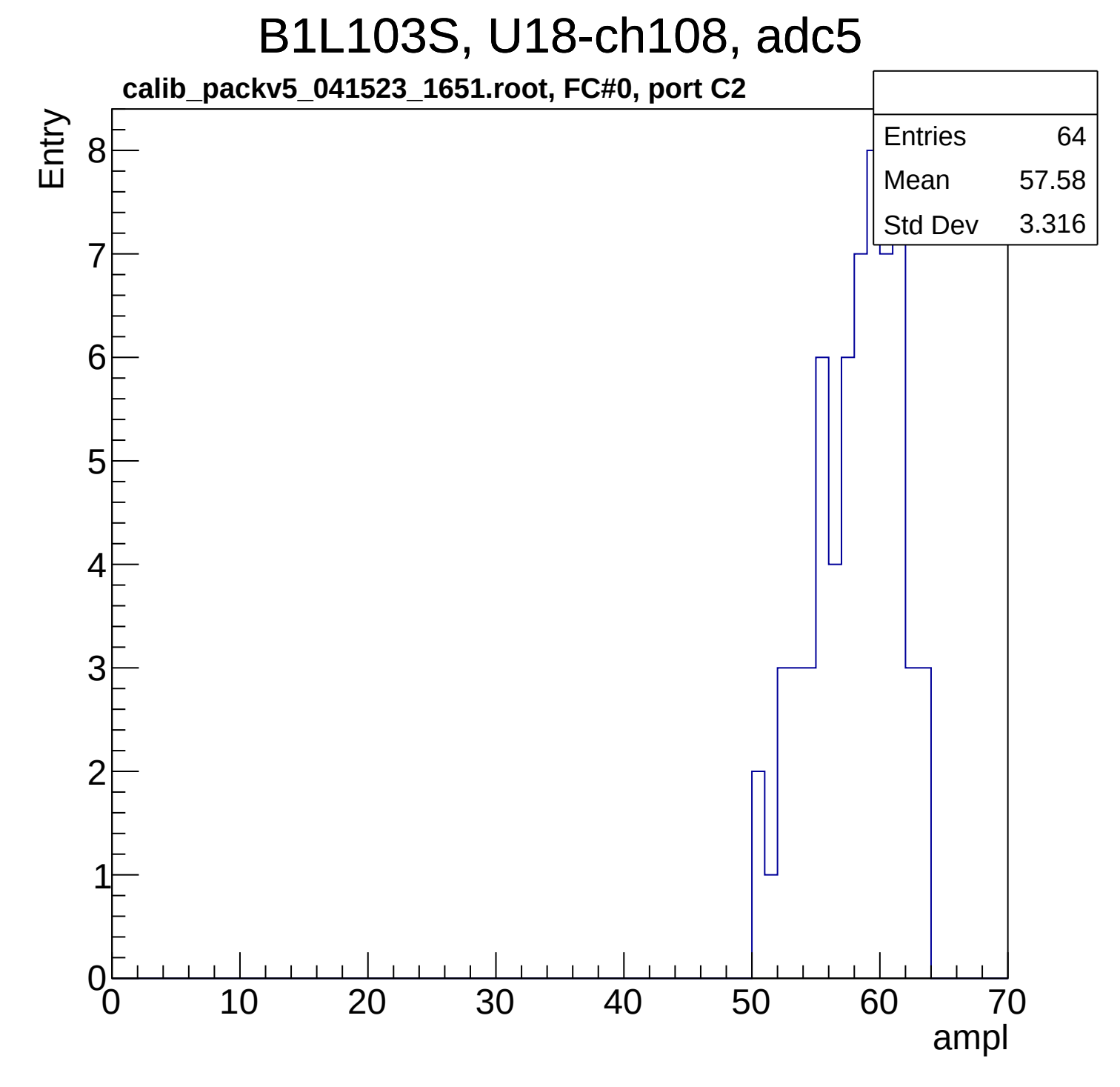
B1L103S, U18-ch108, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 57.58
Std Dev 3.316
Entry
ampl
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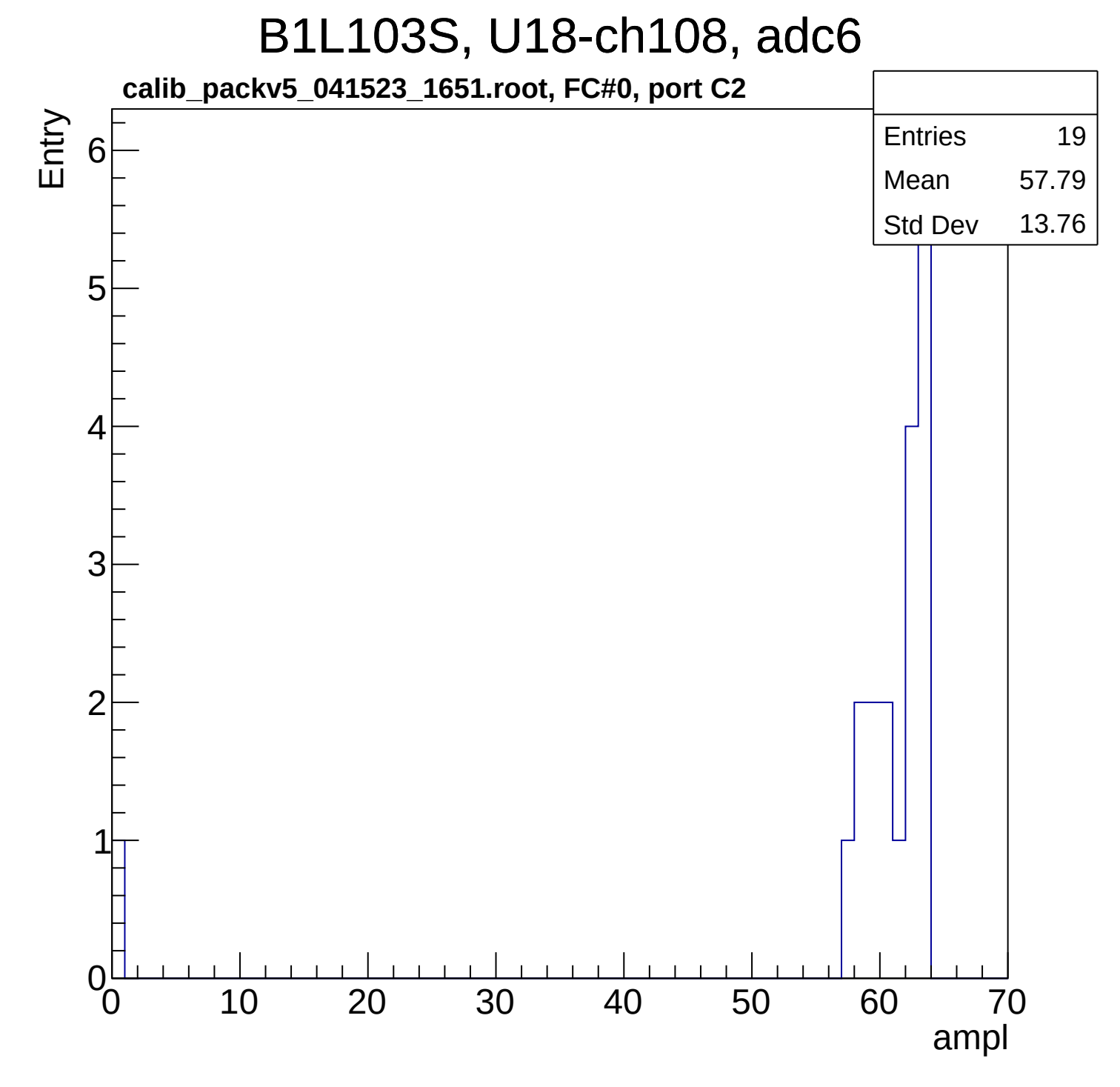
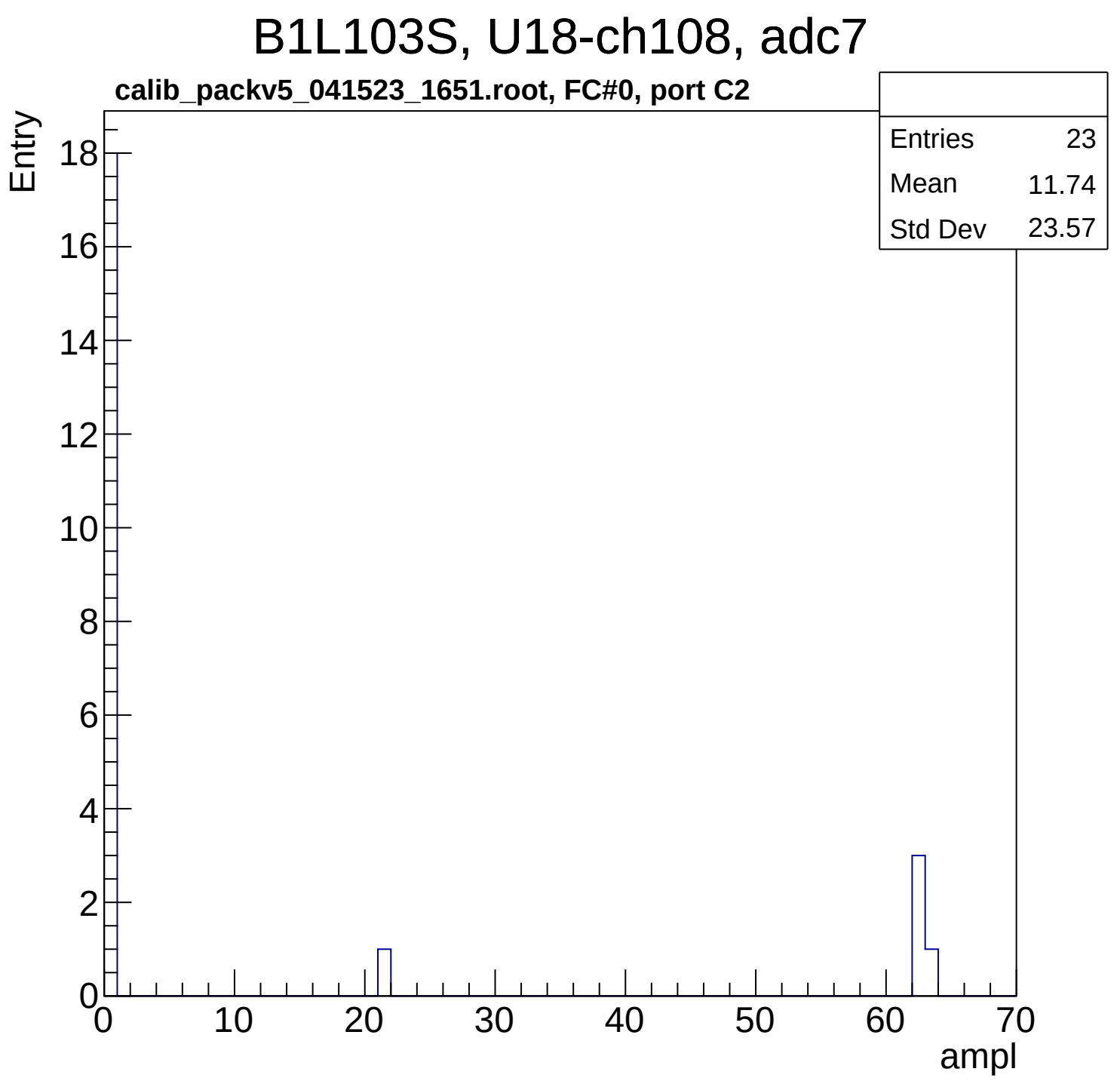
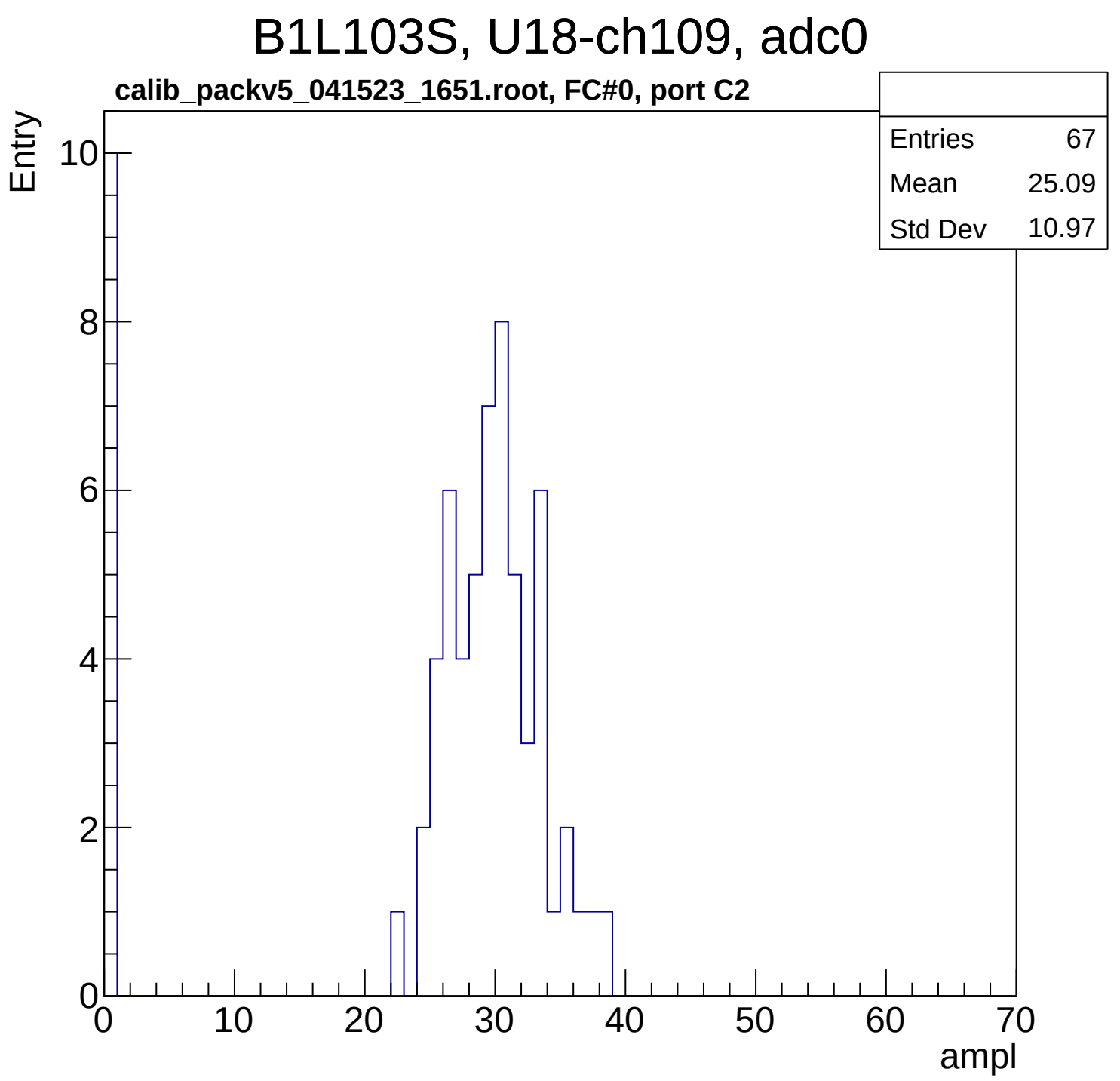
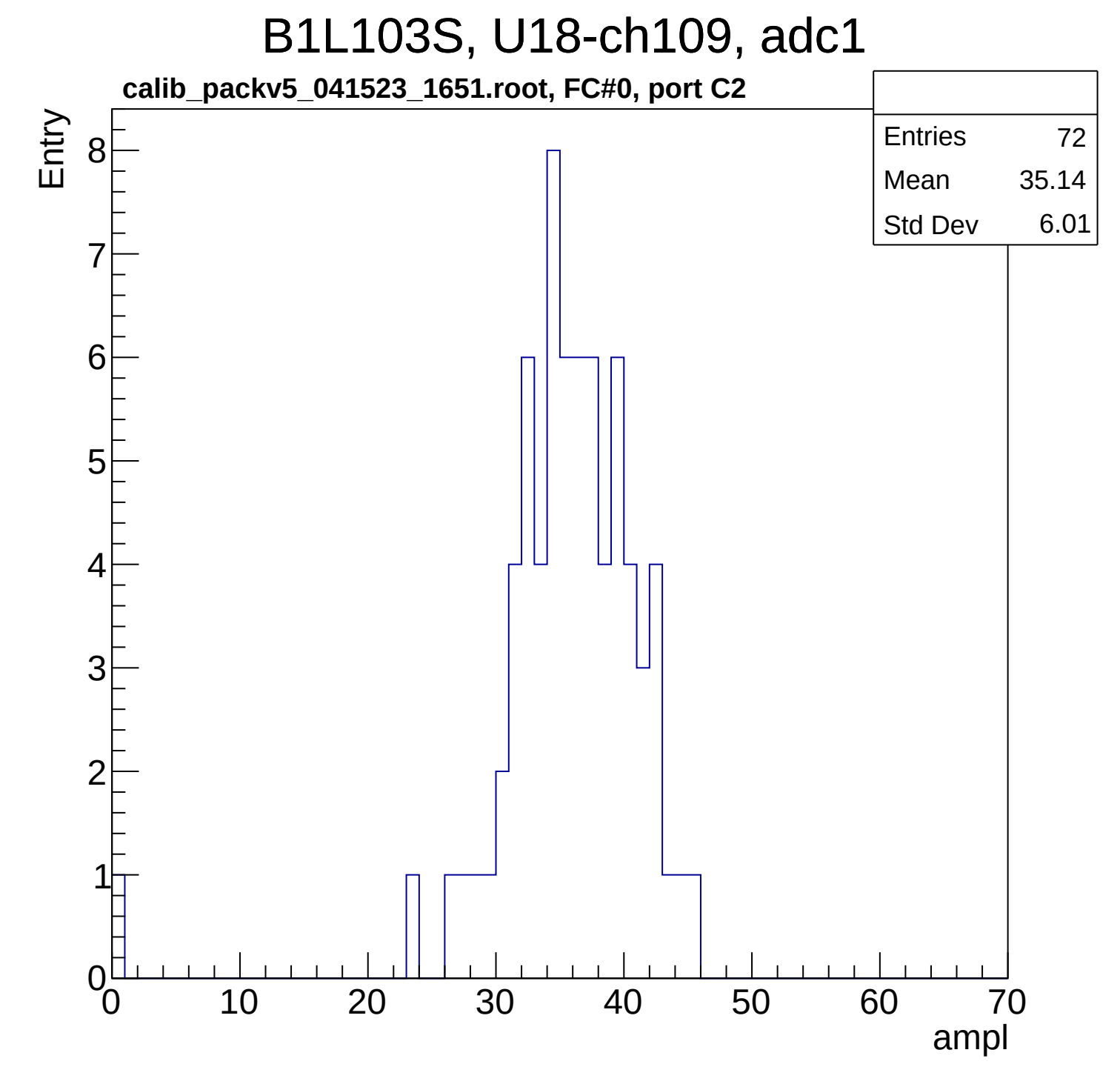
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch108, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 57.79
Std Dev 13.76
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U18-ch108, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 23
Mean 11.74
Std Dev 23.57
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch109, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 25.09
Std Dev 10.97
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch109, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 35.14
Std Dev 6.01
Entry
ampl
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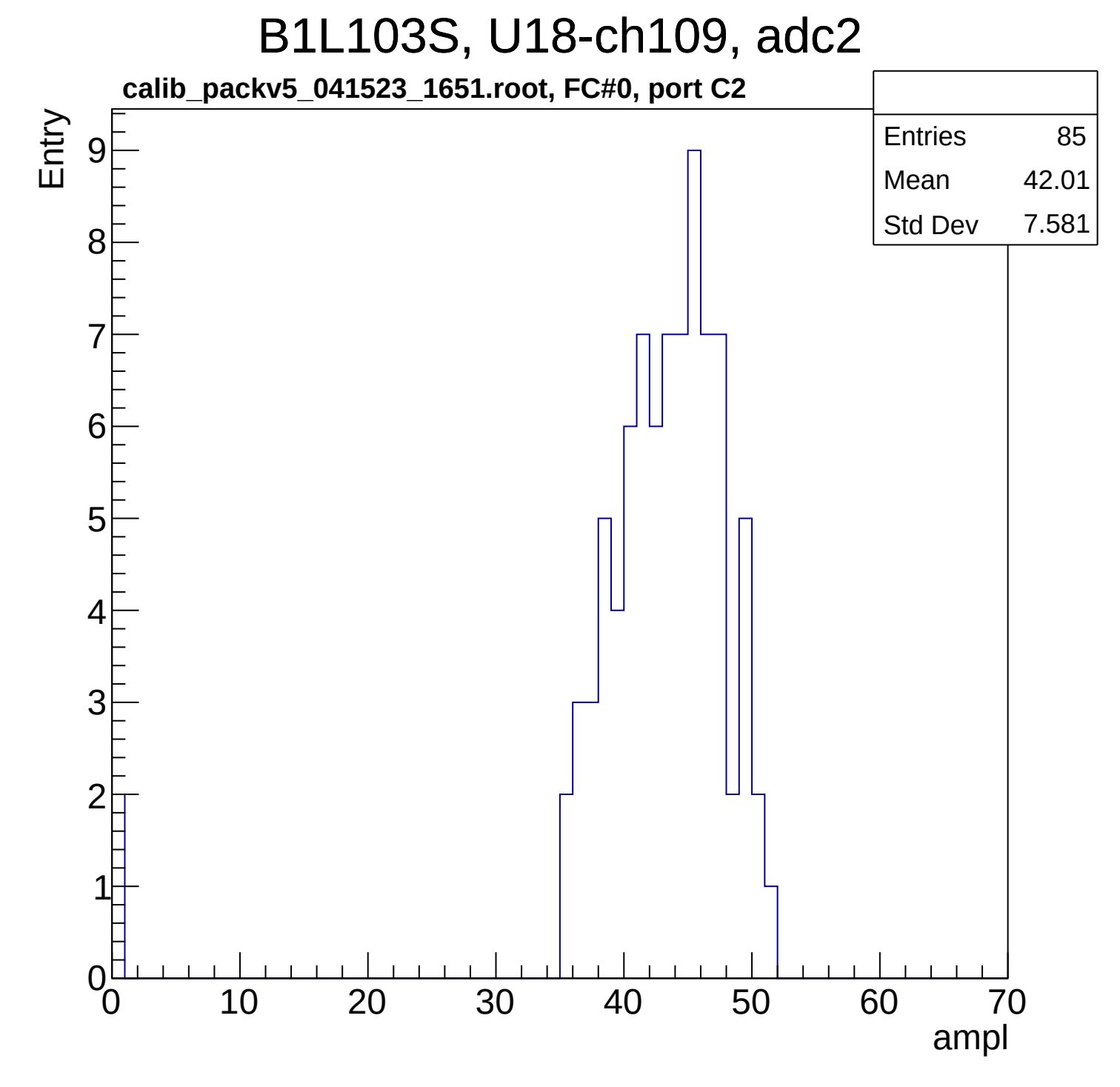
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch109, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 42.01
Std Dev 7.581
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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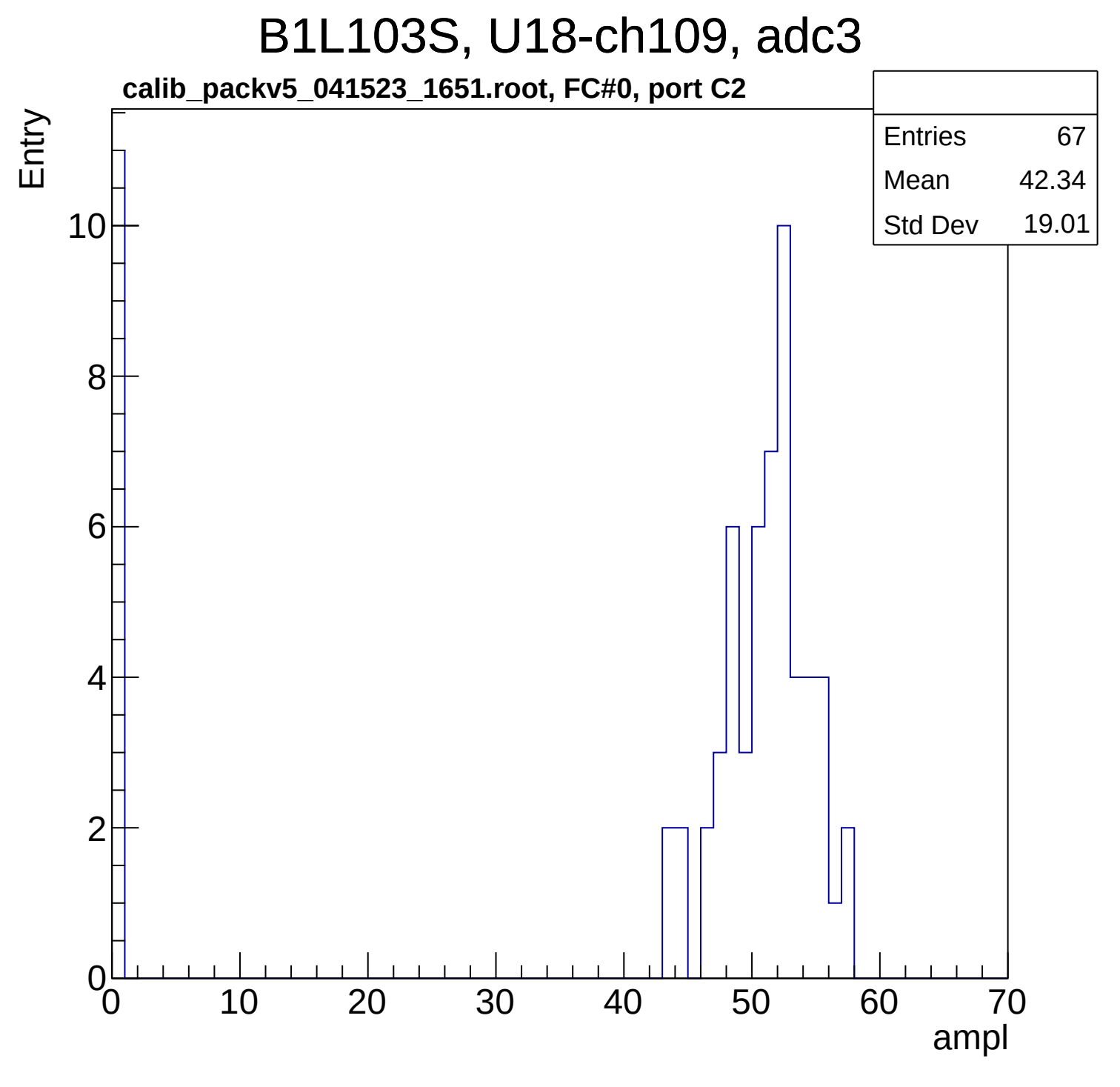
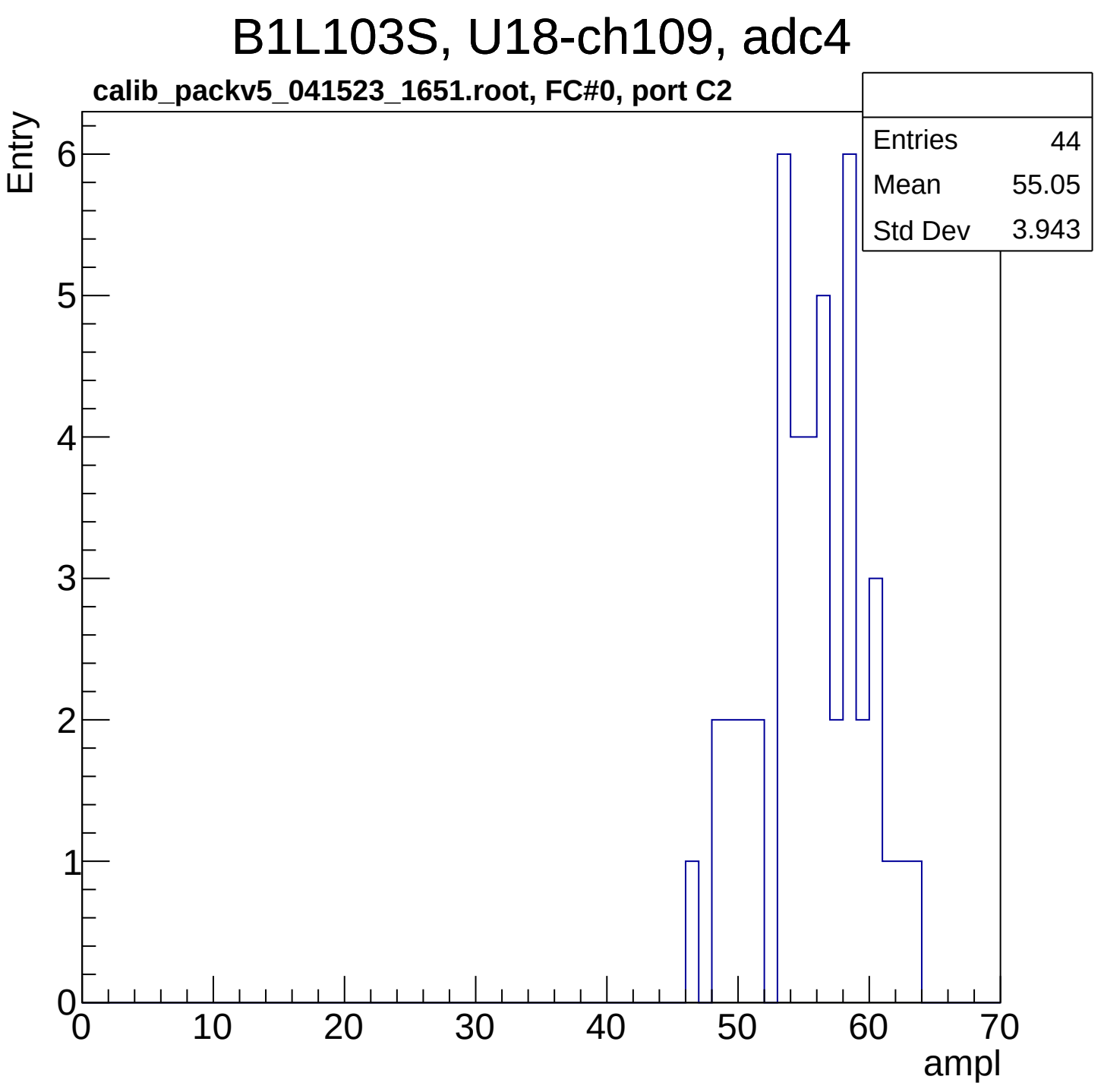

B1L103S, U18-ch109, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 42.34
Std Dev 19.01
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U18-ch109, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 55.05
Std Dev 3.943
Entry
ampl
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1
2
3
4
5
6
0
10
20
30
40
50
60
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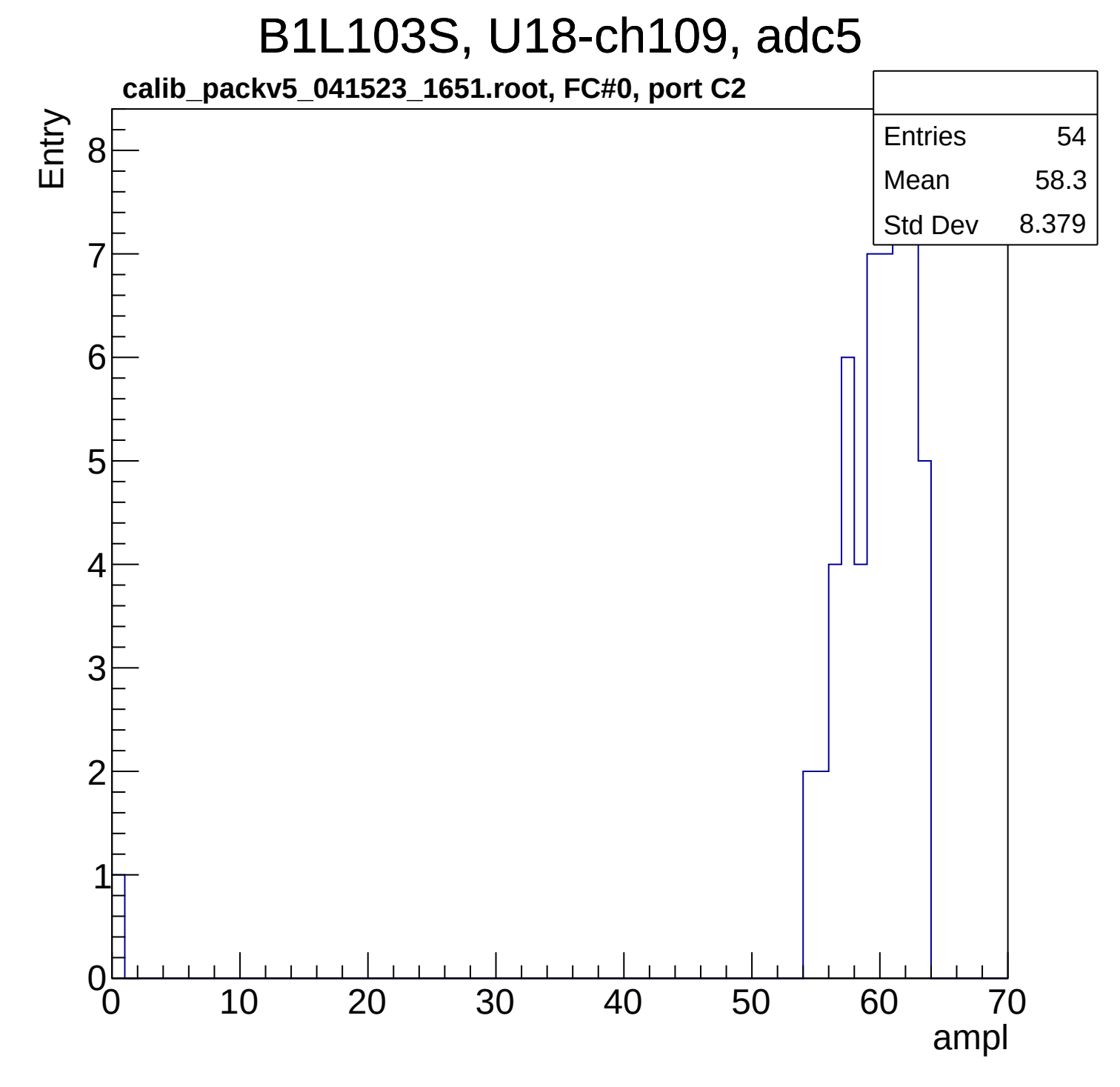
B1L103S, U18-ch109, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 58.3
Std Dev 8.379
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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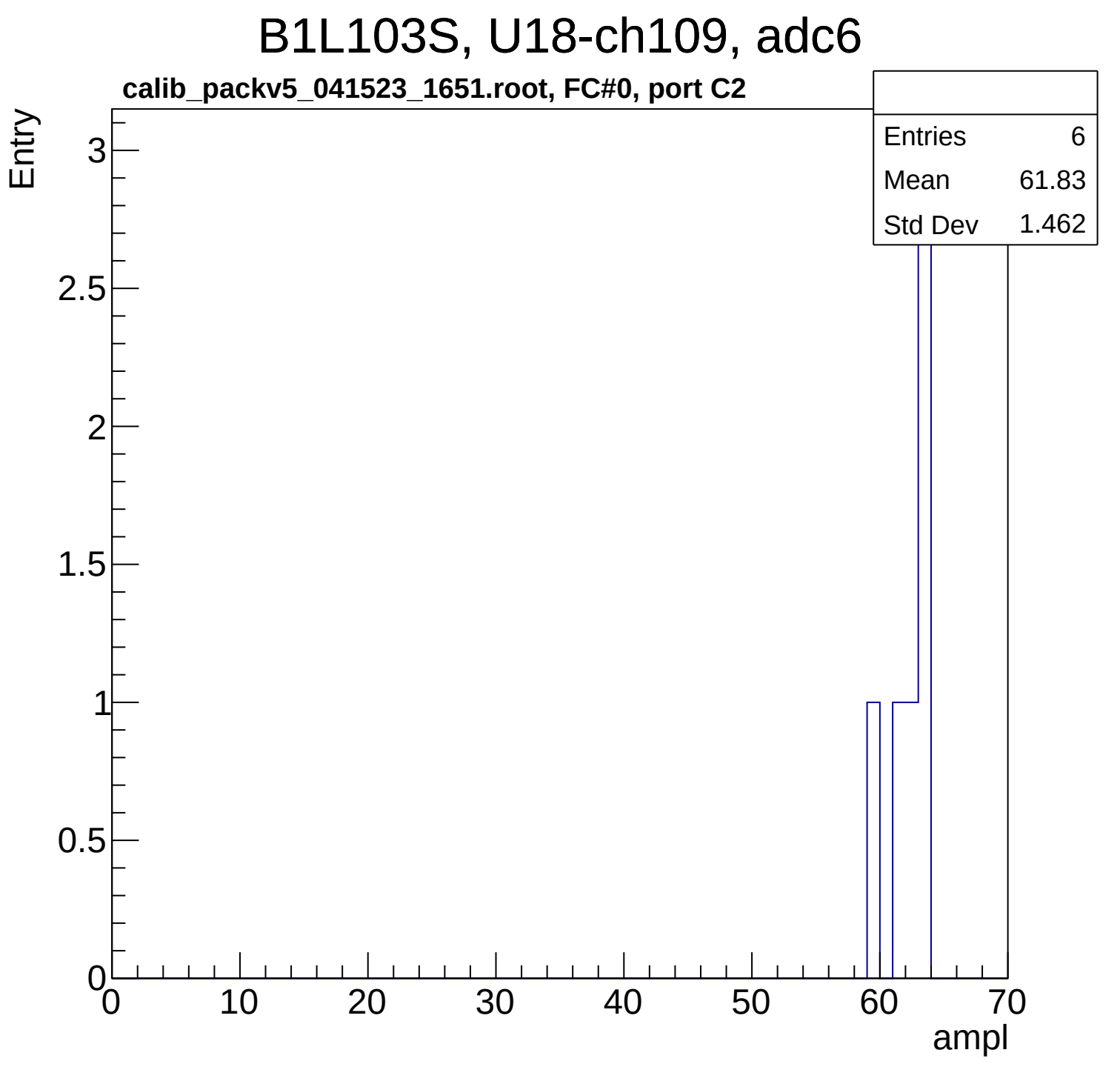
B1L103S, U18-ch109, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 61.83
Std Dev 1.462
Entry
ampl
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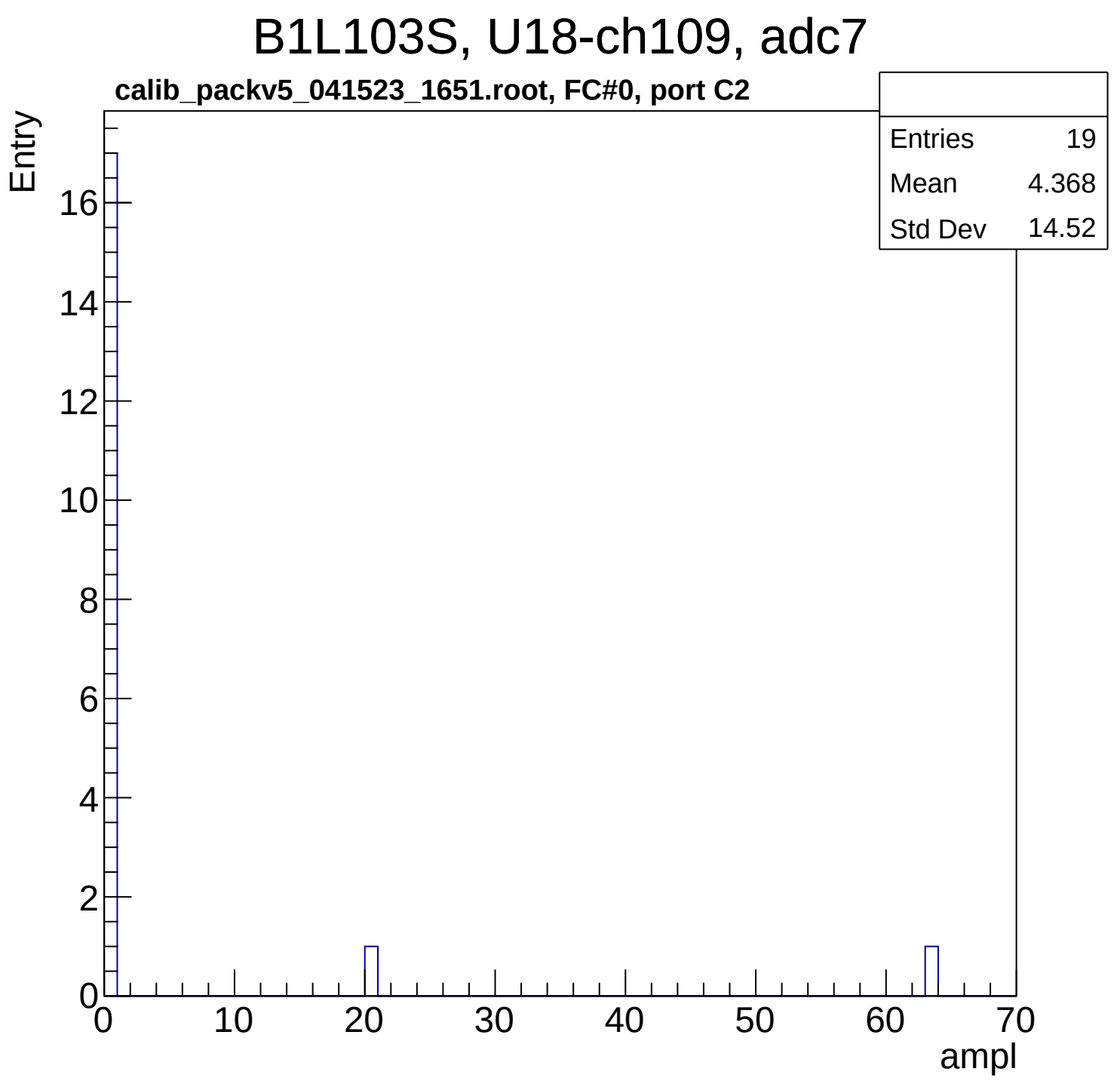
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U18-ch109, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 4.368
Std Dev 14.52
Entry
0
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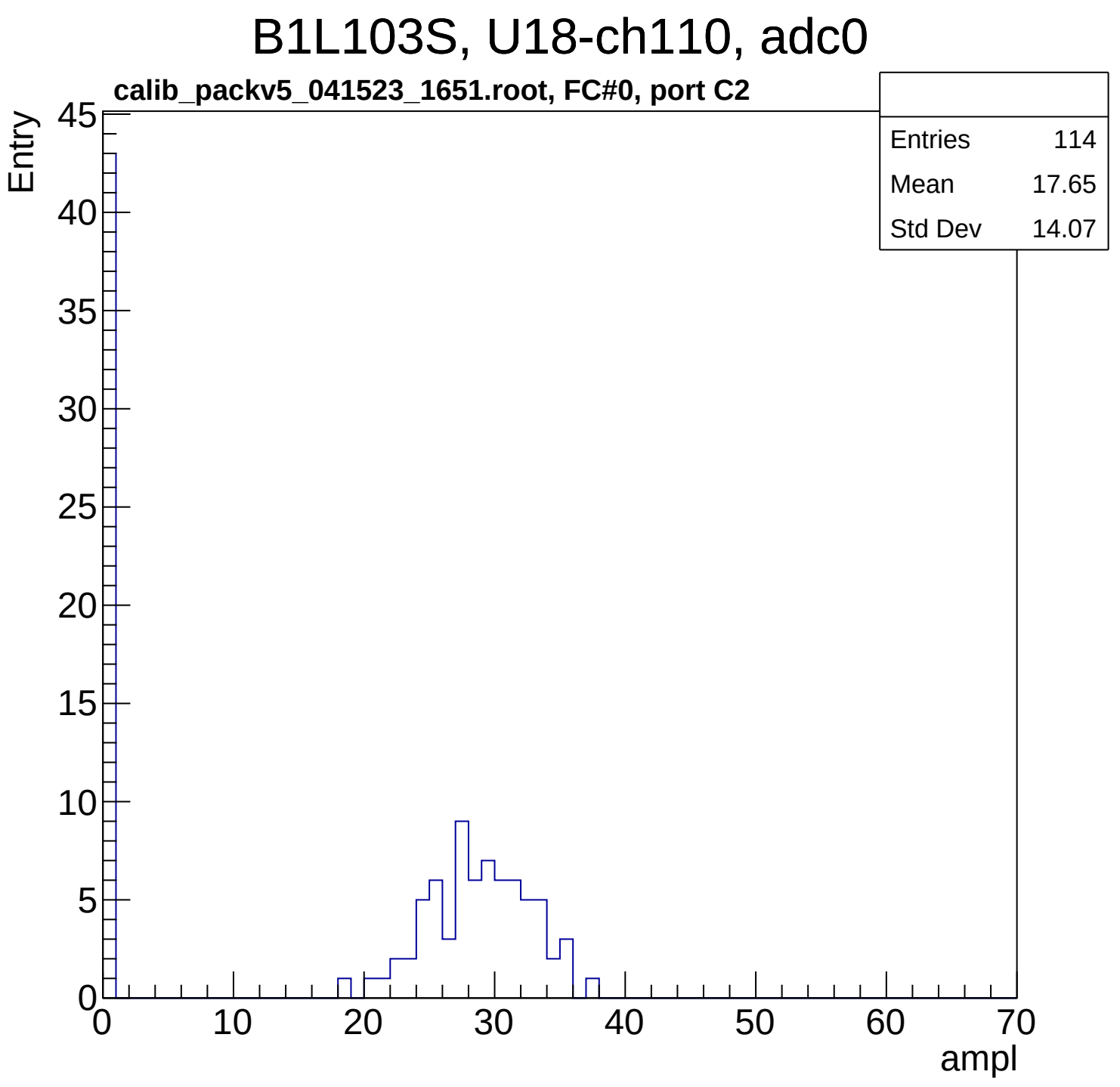
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch110, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 114
Mean 17.65
Std Dev 14.07
Entry
ampl
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10
15
20
25
30
35
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45
0
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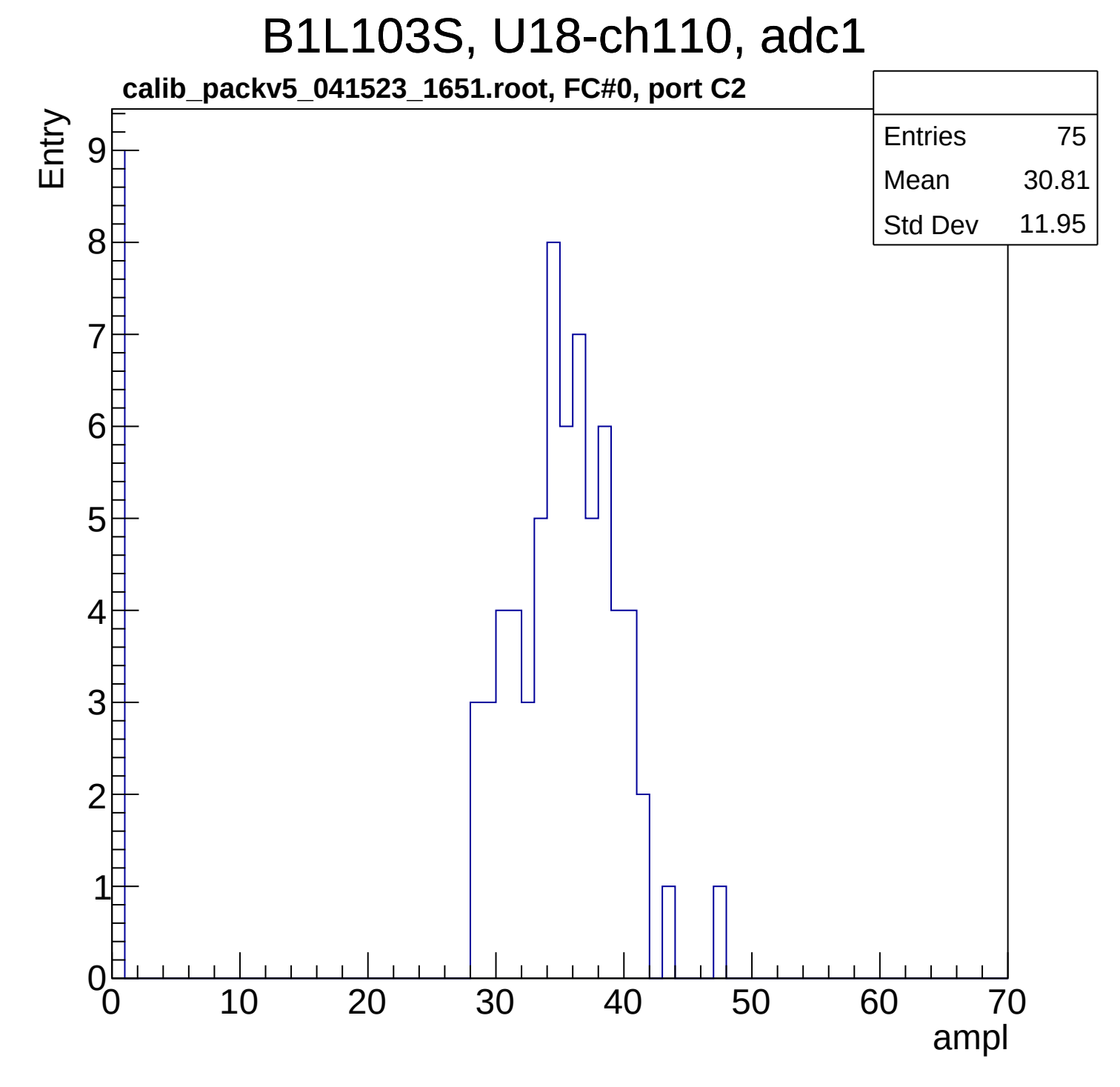
20
30
40
50
60
70


B1L103S, U18-ch110, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 30.81
Std Dev 11.95
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
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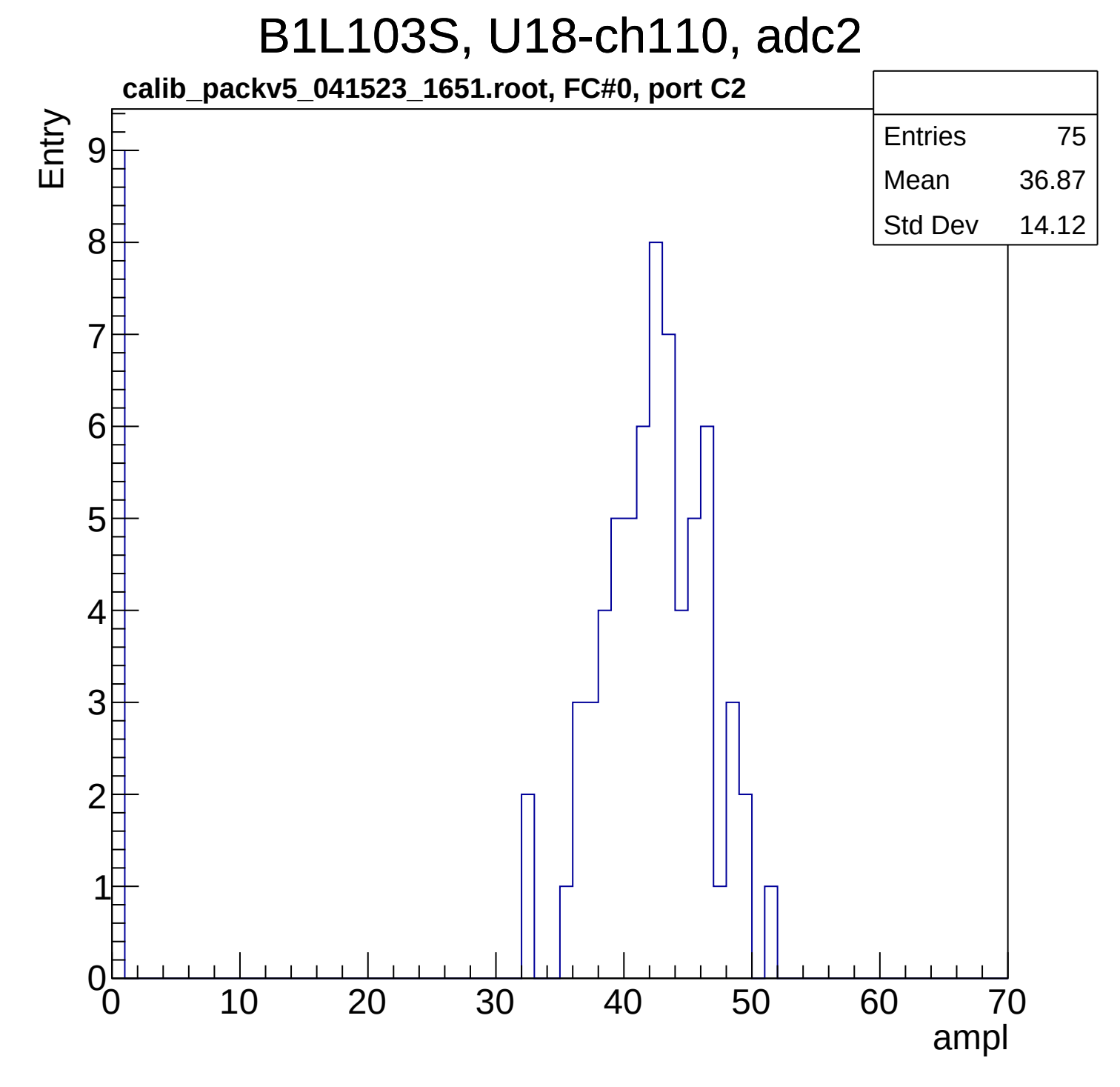
60
70


B1L103S, U18-ch110, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 36.87
Std Dev 14.12
Entry
ampl
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2
3
4
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6
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0
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60
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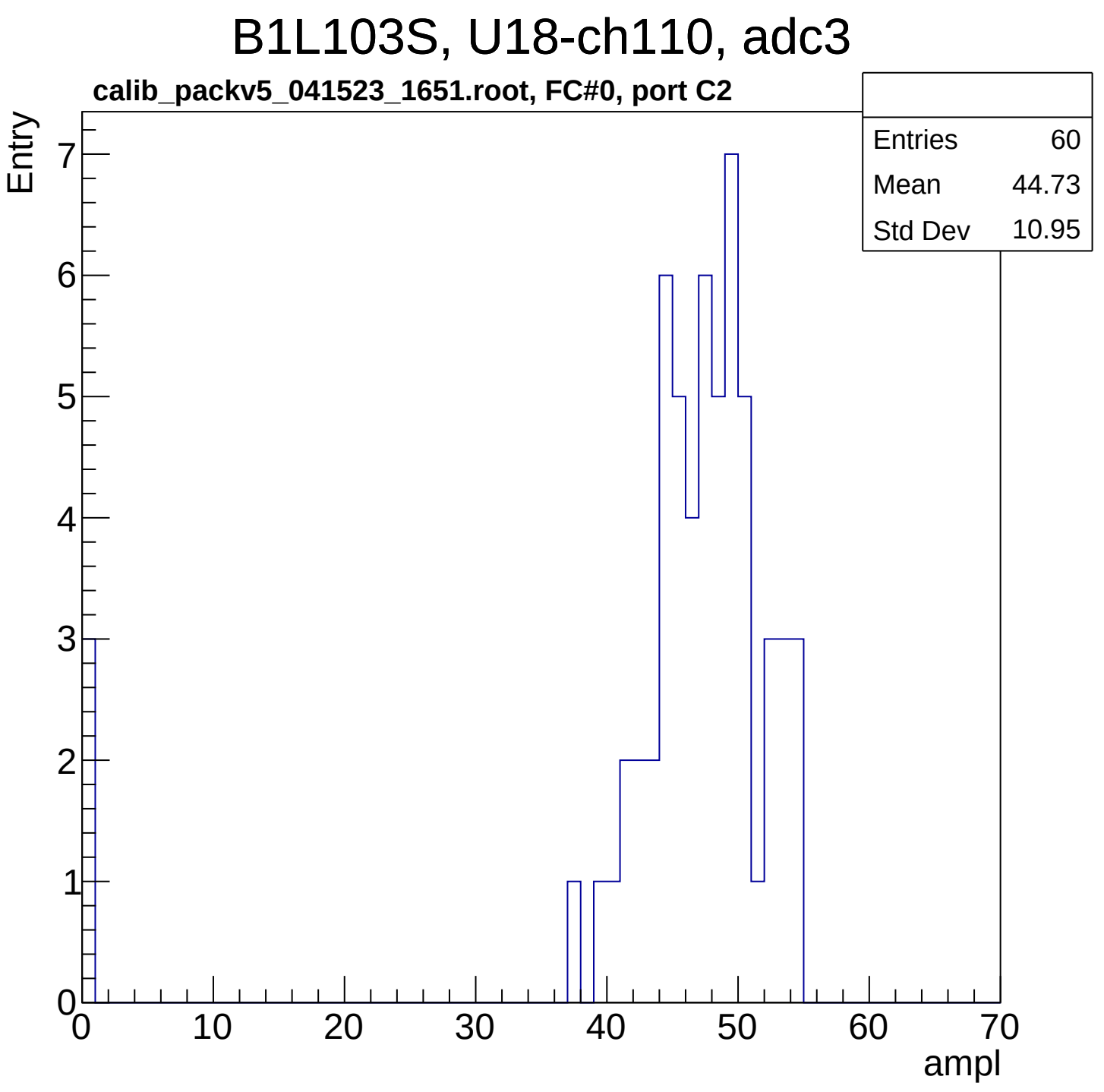
B1L103S, U18-ch110, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 44.73
Std Dev 10.95
Entry
ampl
0
1
2
3
4
5
6
7
0
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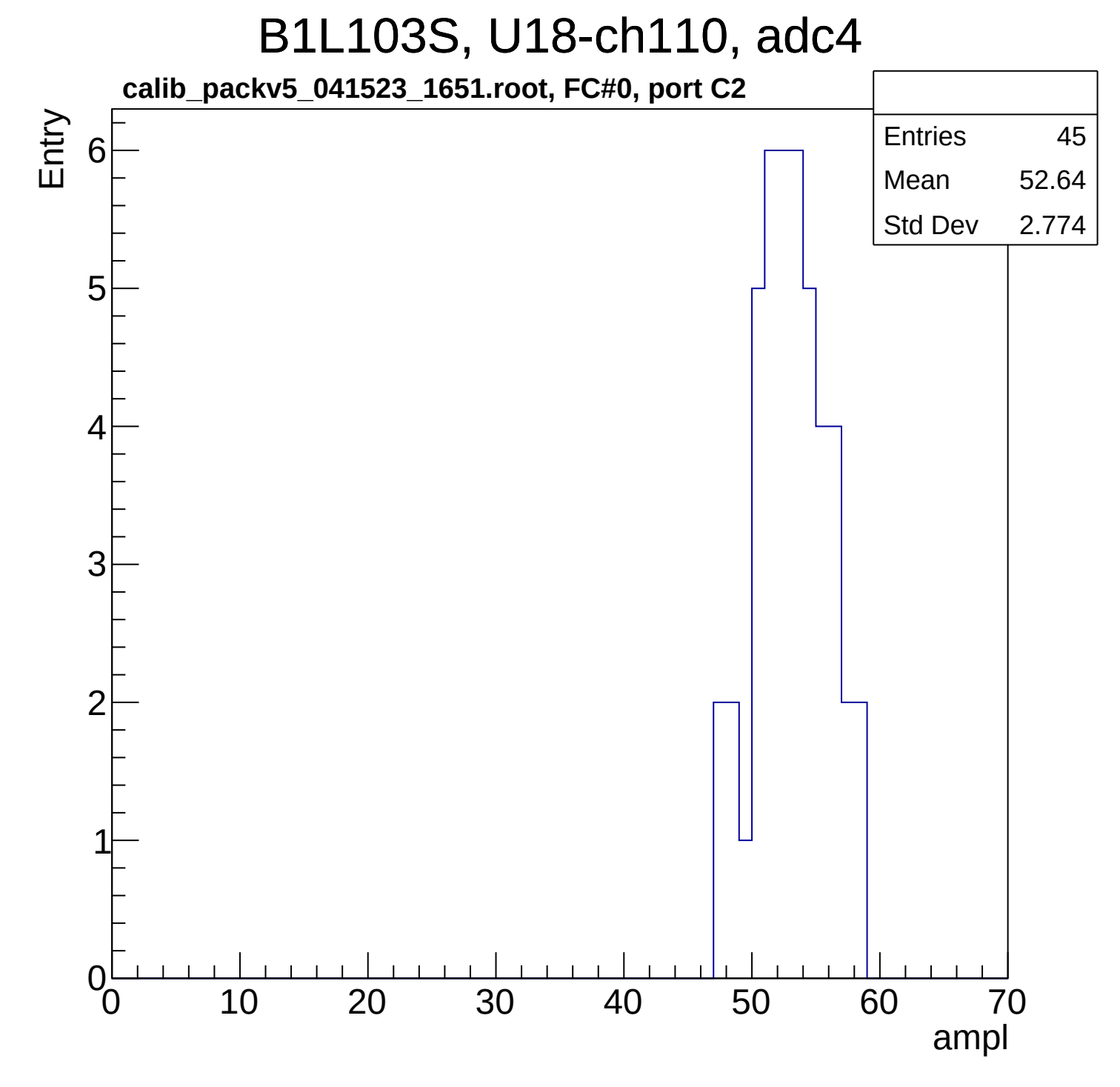
20
30
40
50
60
70


B1L103S, U18-ch110, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 52.64
Std Dev 2.774
Entry
ampl
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4
5
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0
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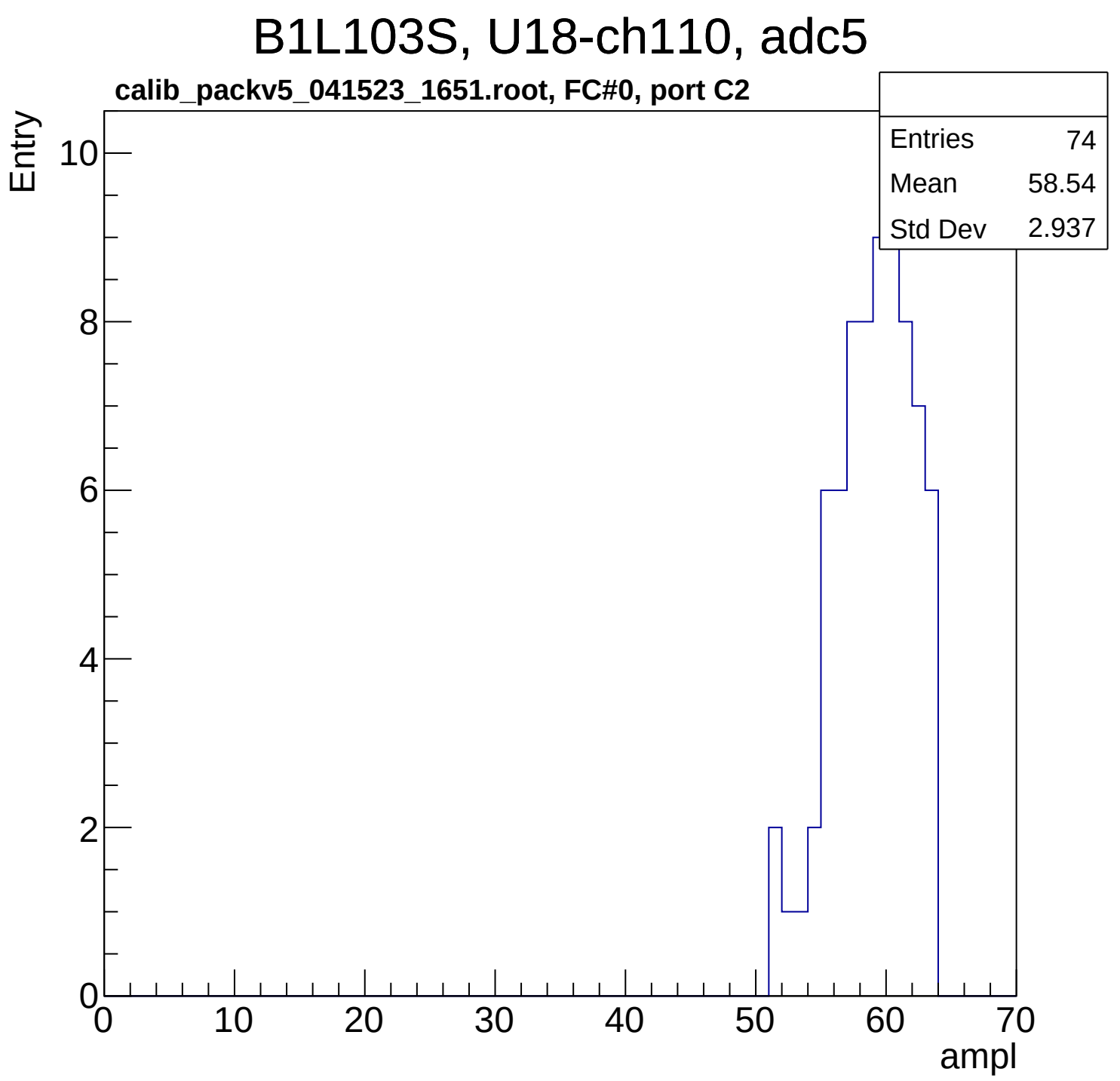
20
30
40
50
60
70


B1L103S, U18-ch110, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 58.54
Std Dev 2.937
Entry
ampl
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2
4
6
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0
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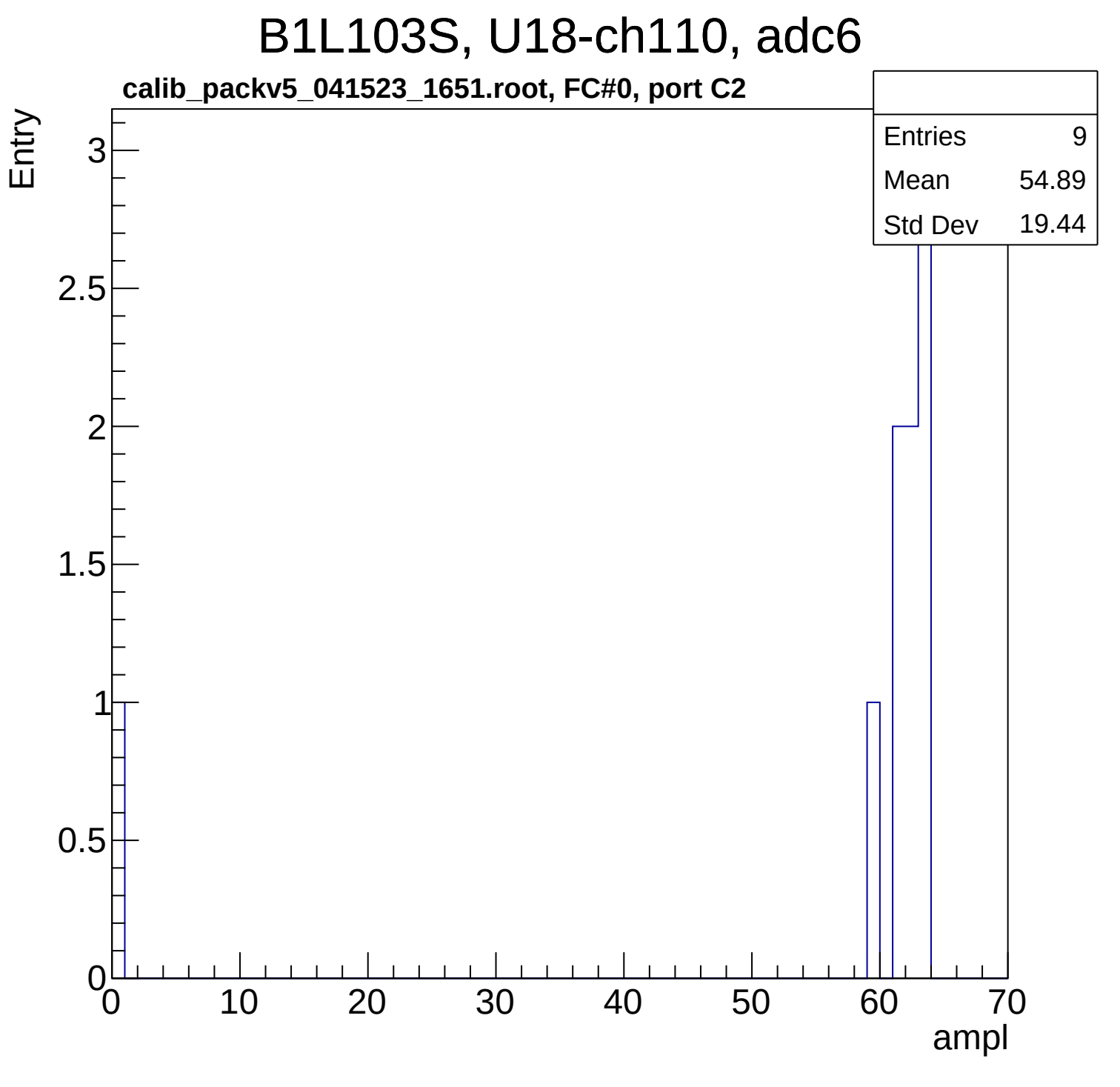
40
50
60
70


B1L103S, U18-ch110, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 9
Mean 54.89
Std Dev 19.44
Entry
ampl
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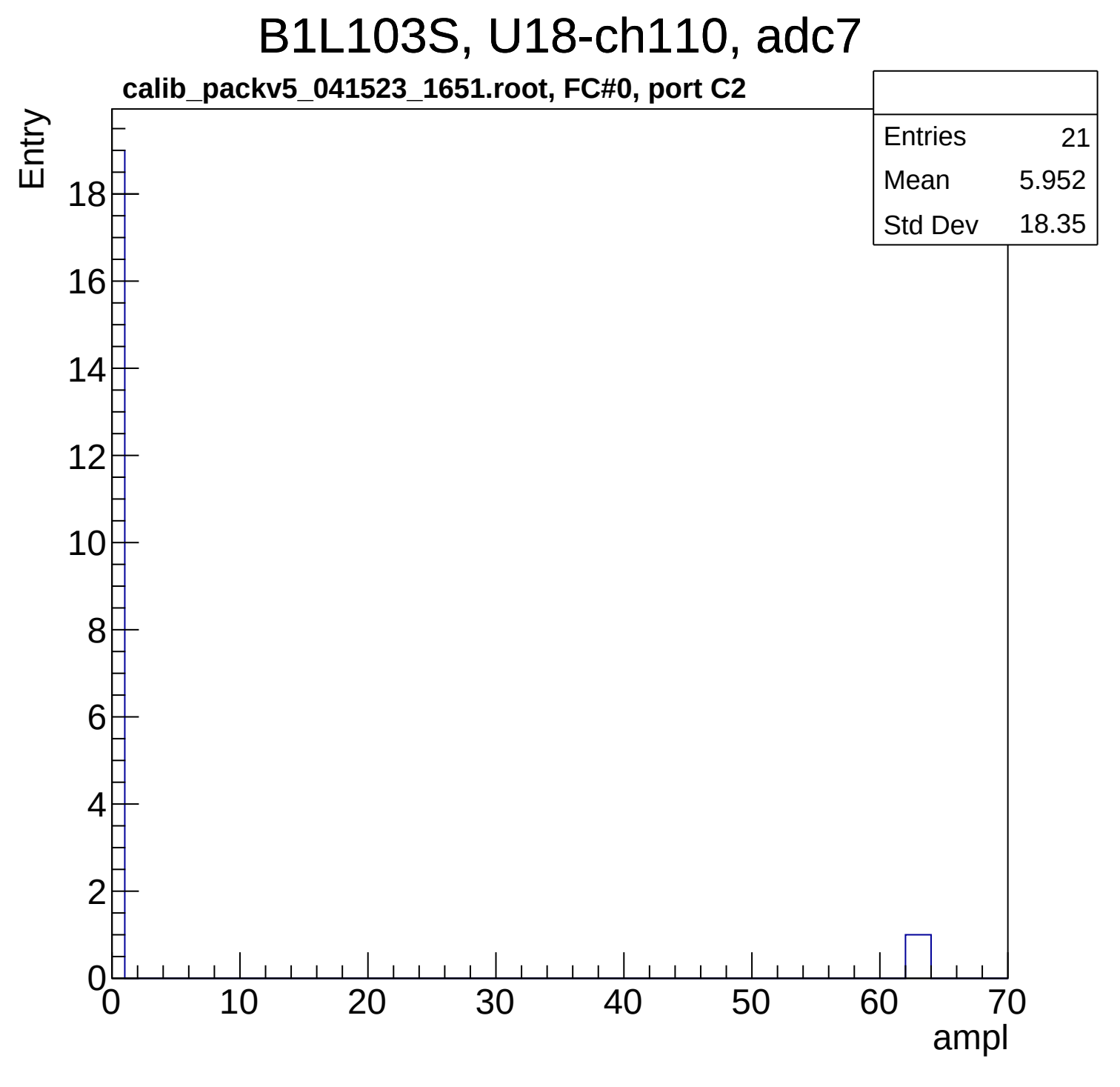
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U18-ch110, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 5.952
Std Dev 18.35
Entry
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6
8
10
12
14
16
18
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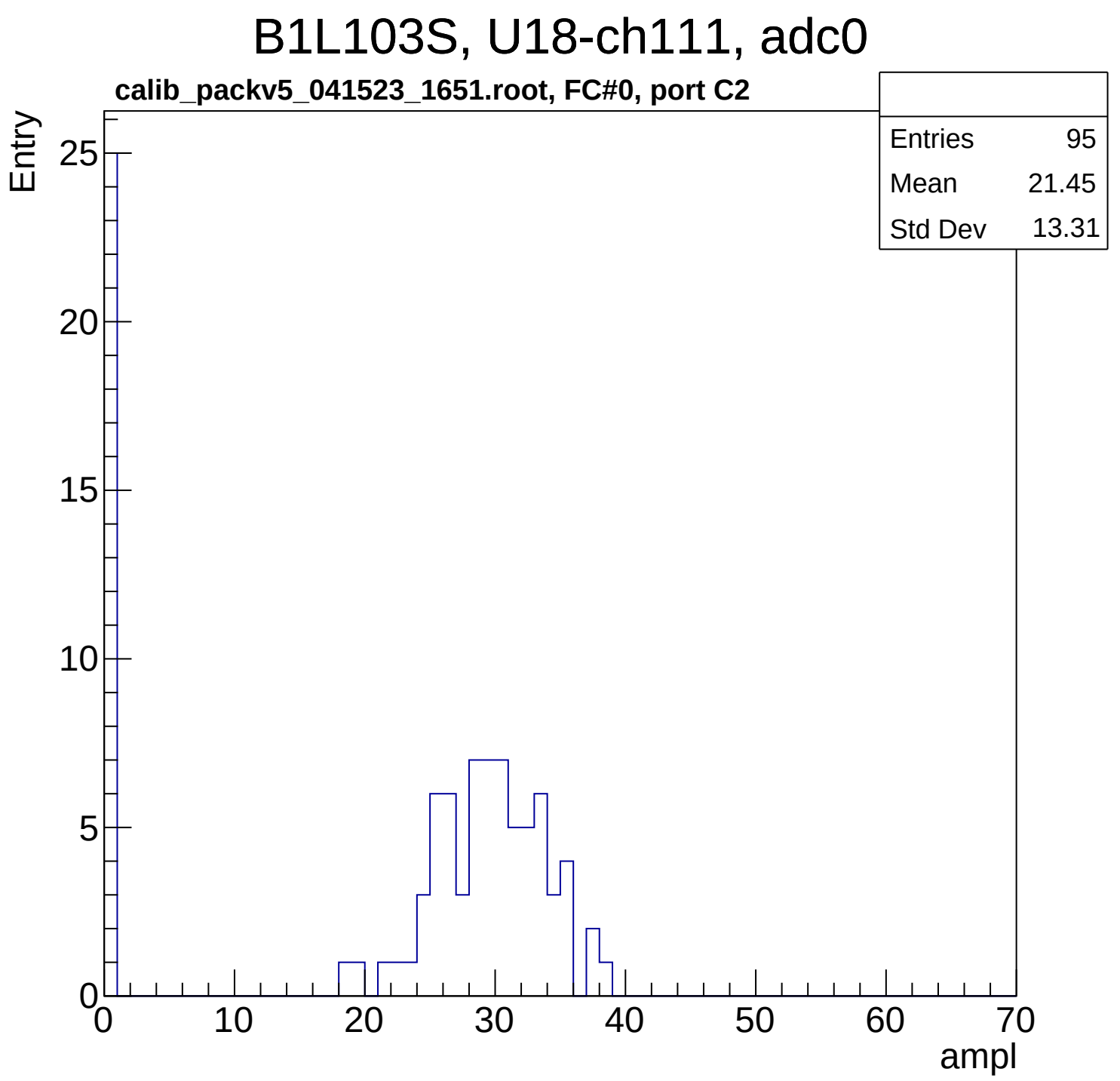
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch111, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 95
Mean 21.45
Std Dev 13.31
Entry
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5
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15
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25
0
10
20
30
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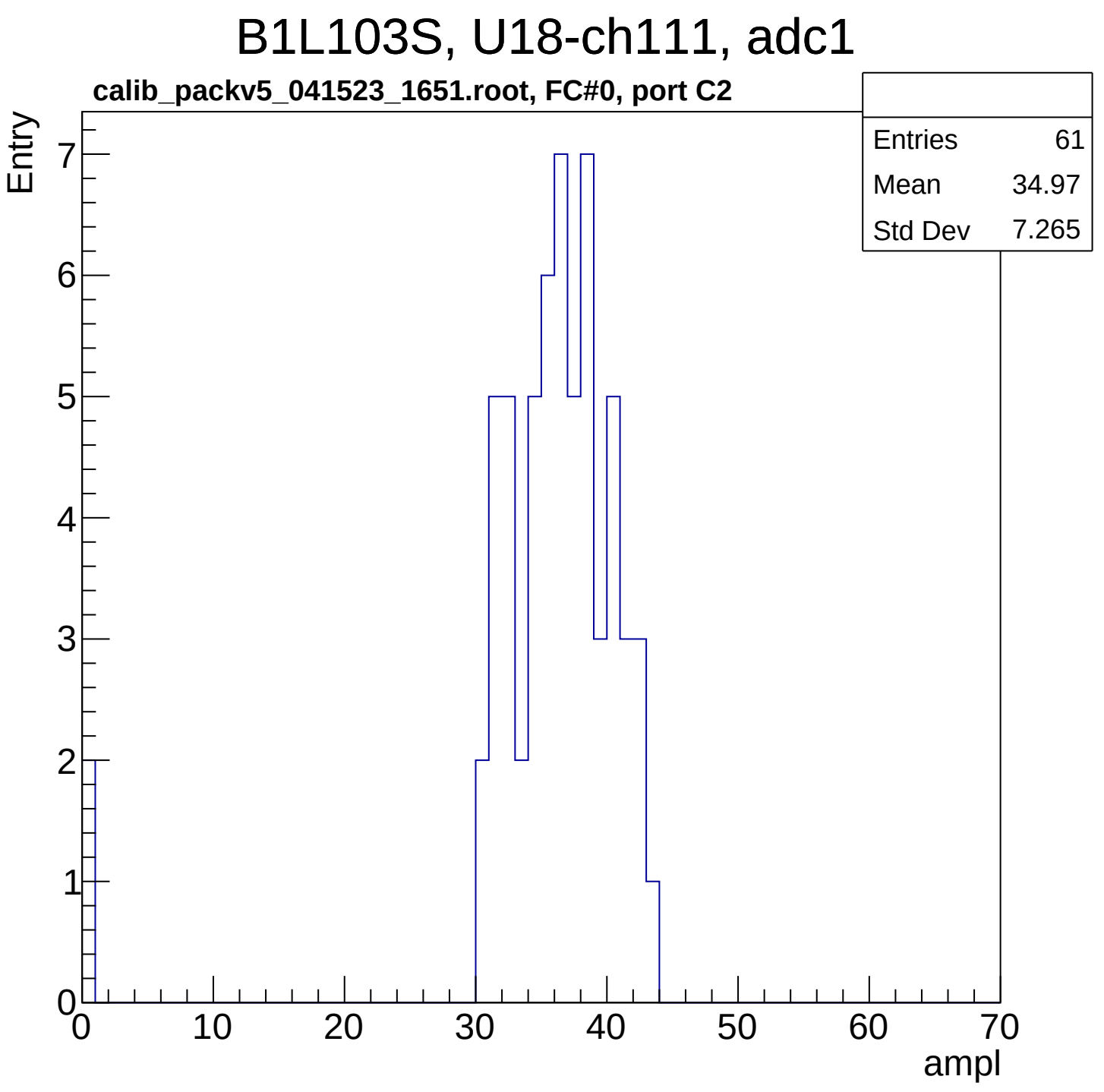
50
60
70
ampl


B1L103S, U18-ch111, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 34.97
Std Dev 7.265
Entry
ampl
0
1
2
3
4
5
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7
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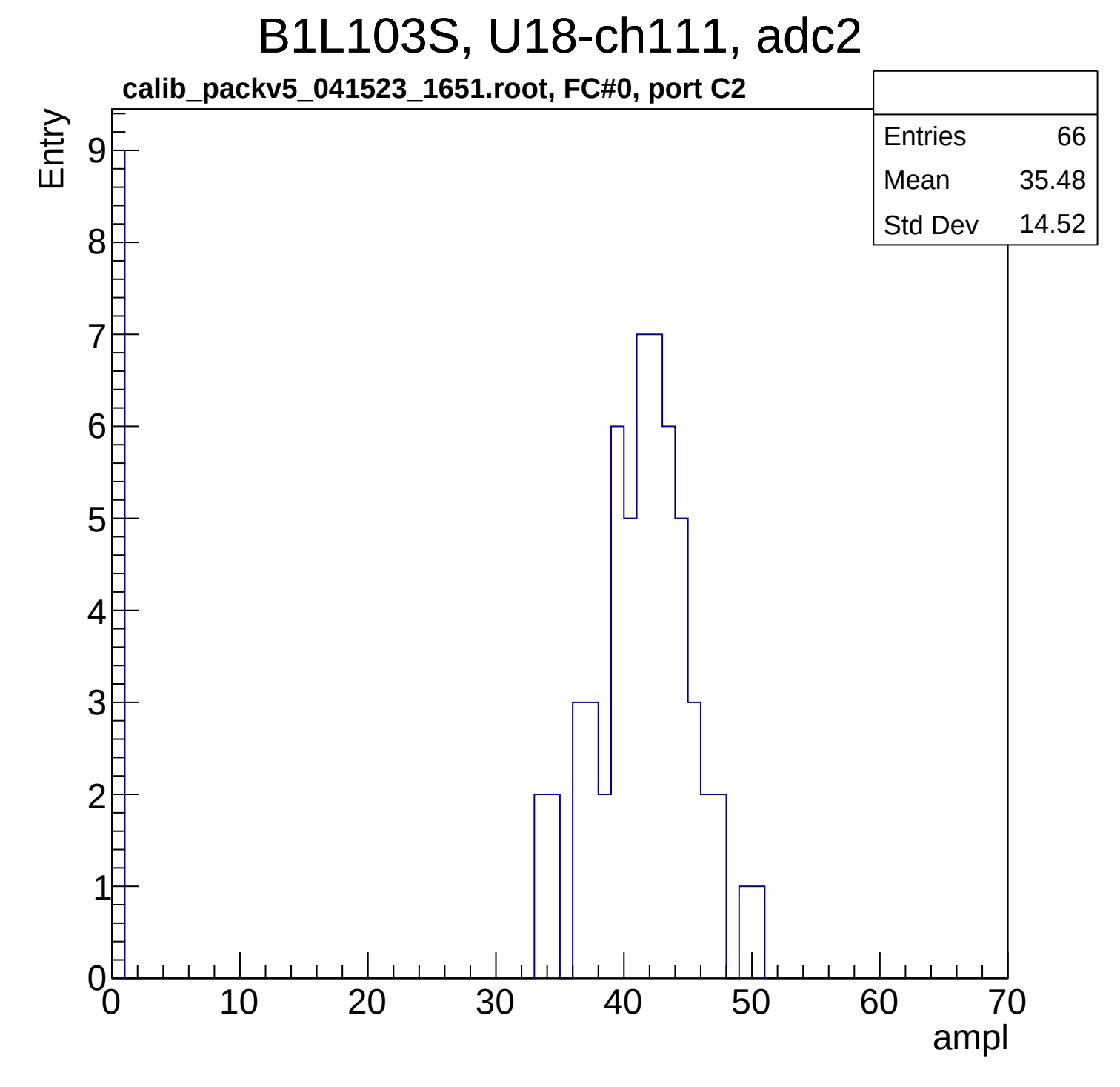
40
50
60
70


B1L103S, U18-ch111, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 35.48
Std Dev 14.52
Entry
ampl
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2
3
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7
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60
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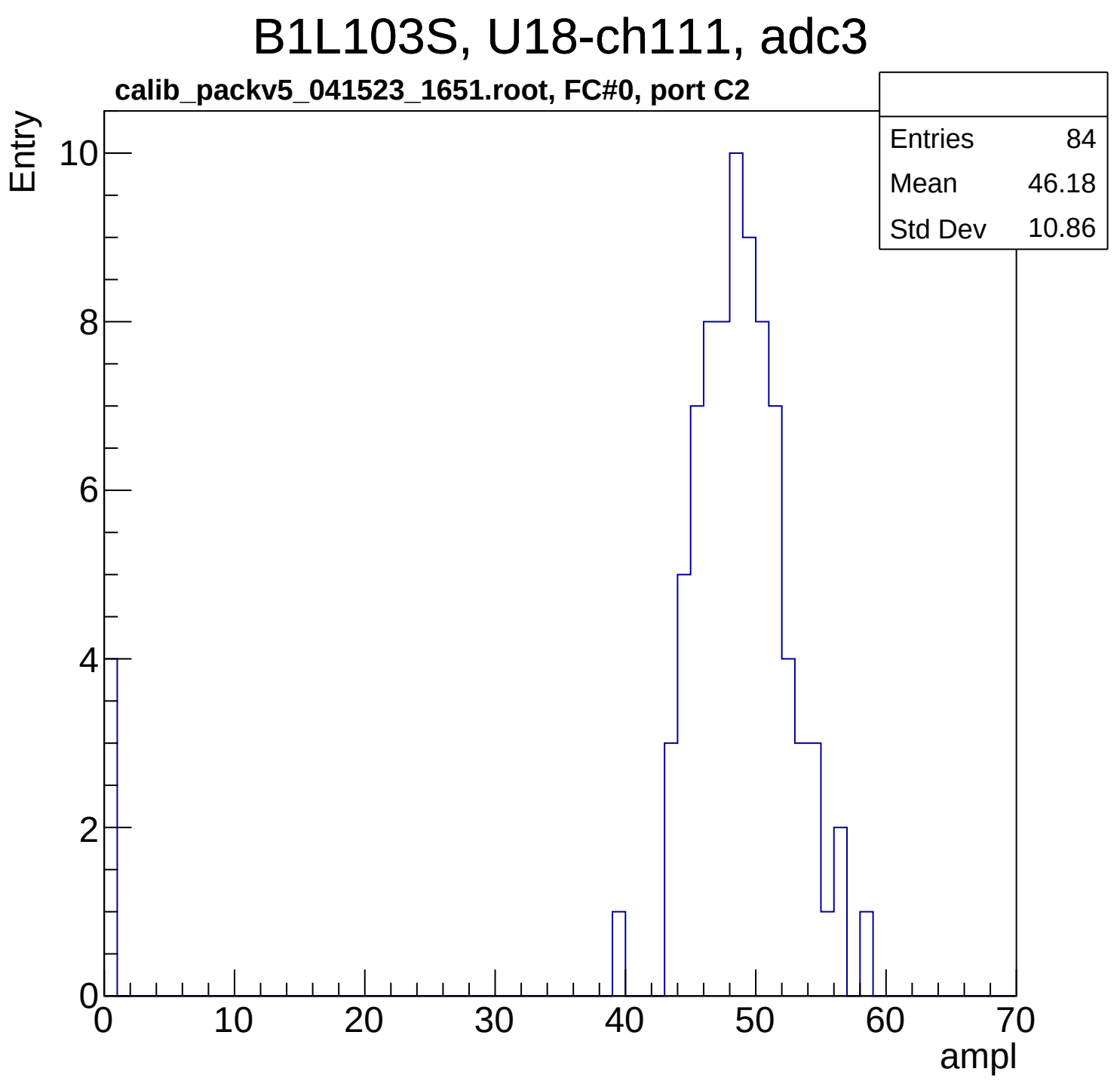
B1L103S, U18-ch111, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 46.18
Std Dev 10.86
Entry
ampl
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4
6
8
10
0
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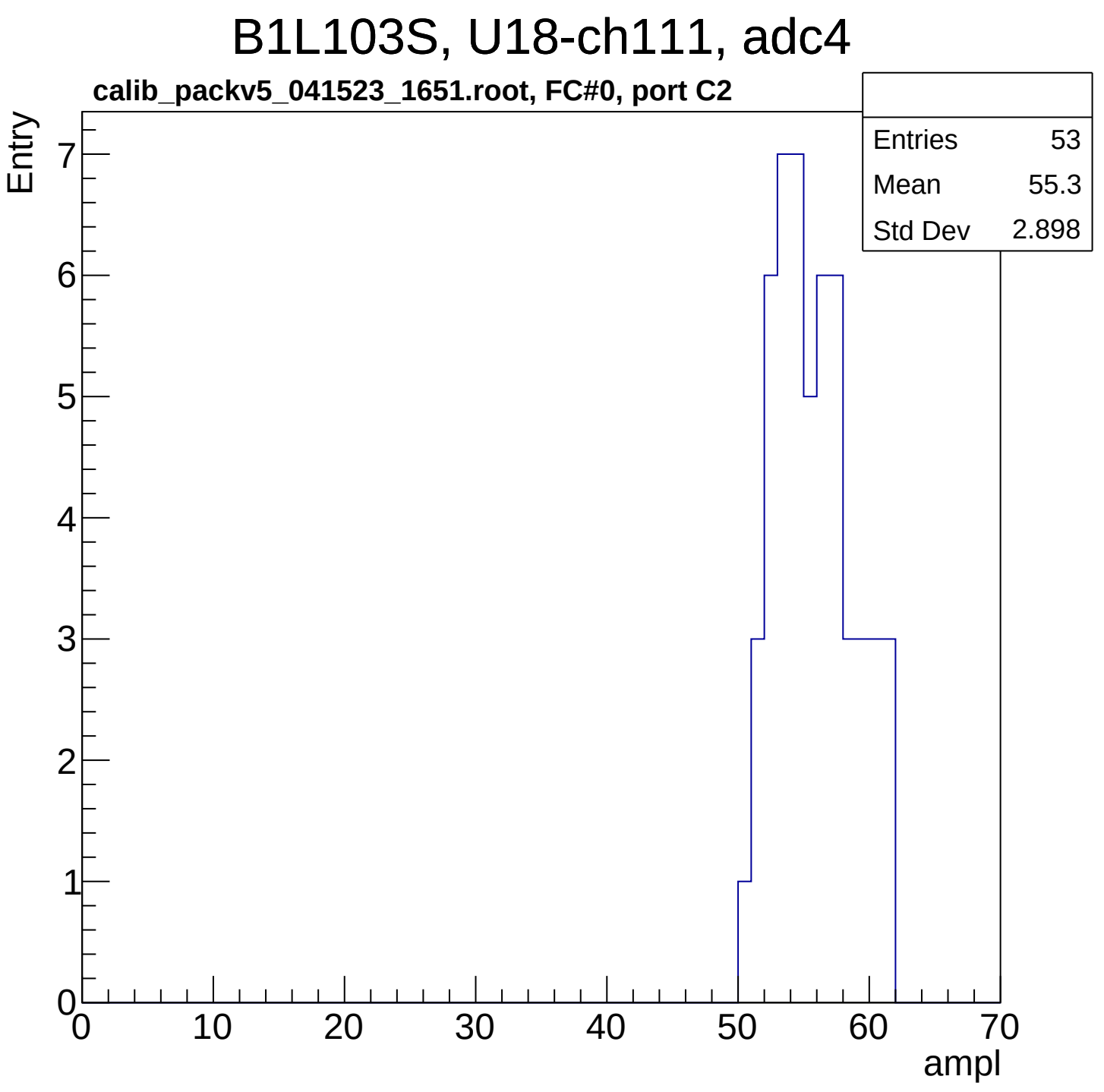
20
30
40
50
60
70


B1L103S, U18-ch111, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 55.3
Std Dev 2.898
Entry
ampl
0
1
2
3
4
5
6
7
0
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20
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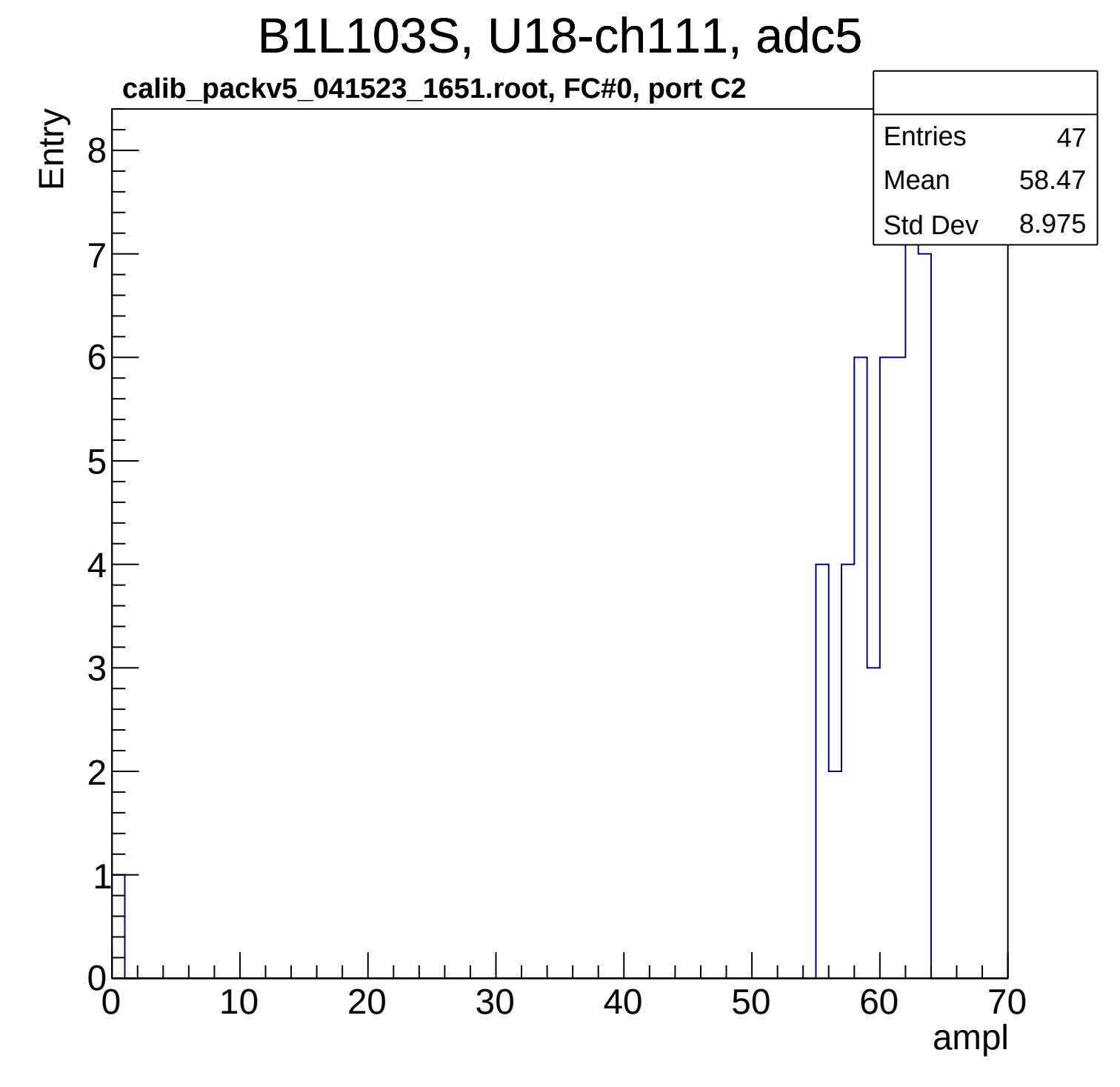
60
70


B1L103S, U18-ch111, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 58.47
Std Dev 8.975
Entry
ampl
0
1
2
3
4
5
6
7
8
0
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20
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40
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60
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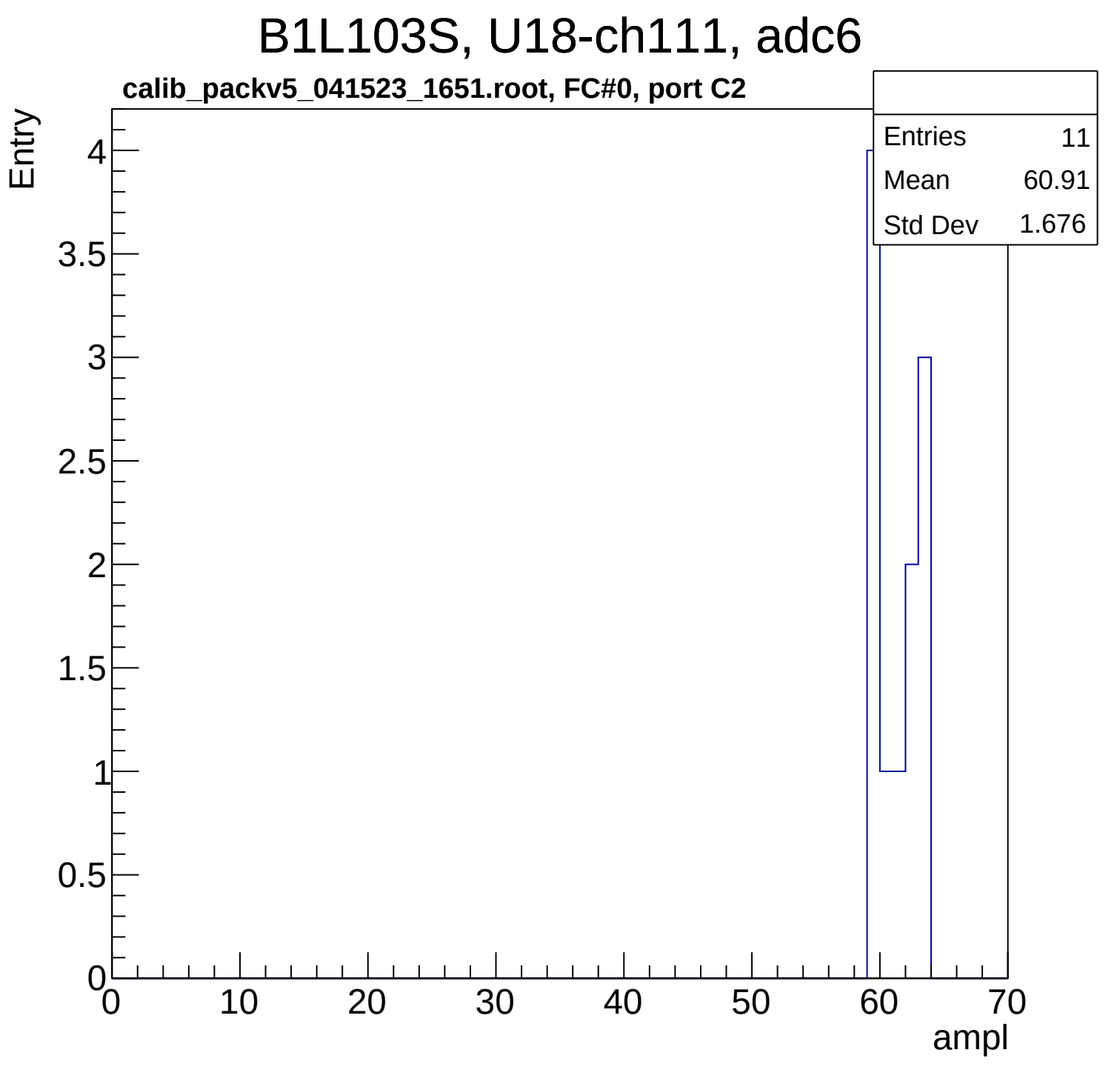
B1L103S, U18-ch111, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 60.91
Std Dev 1.676
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
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40
50
60
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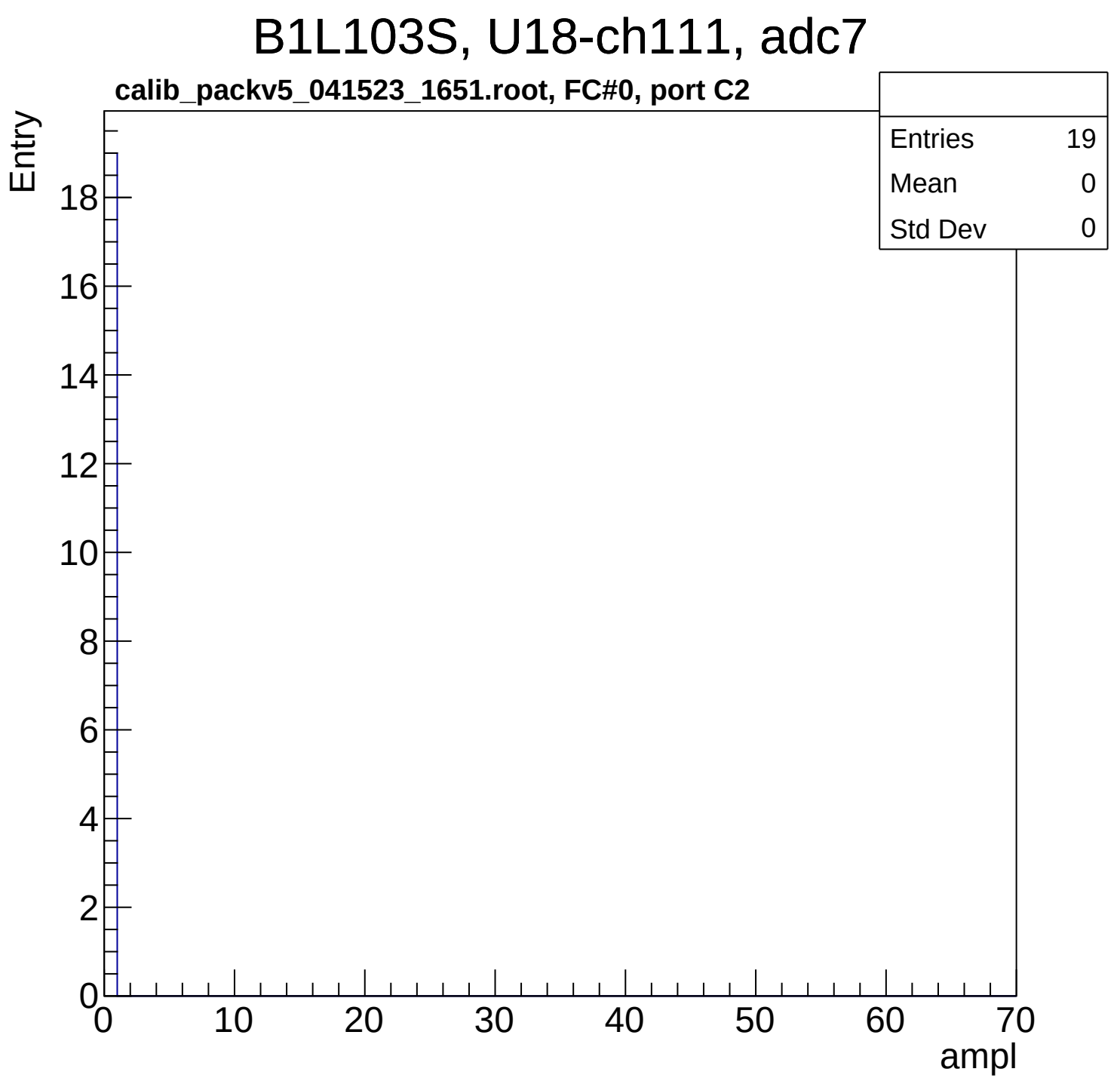
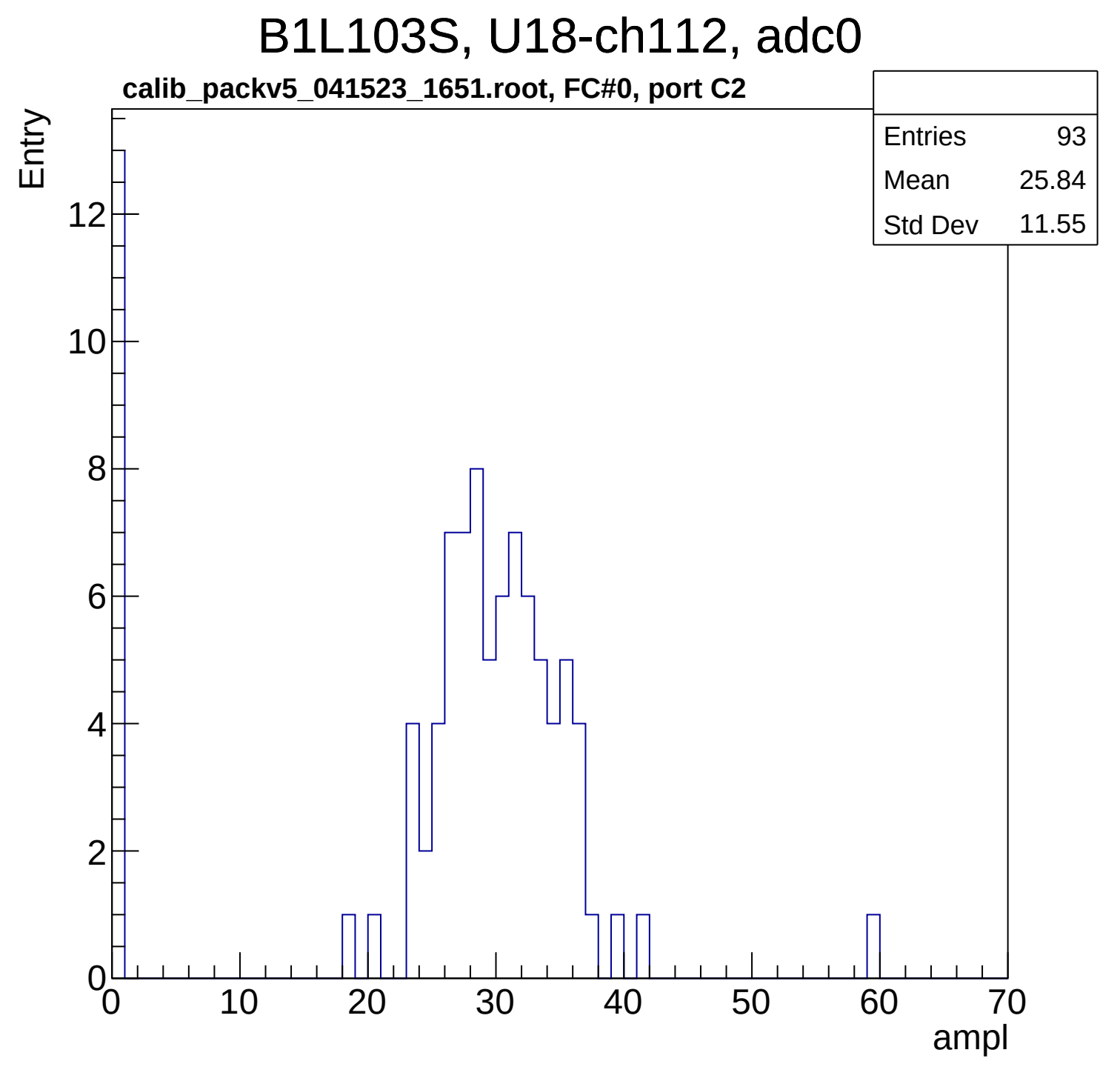
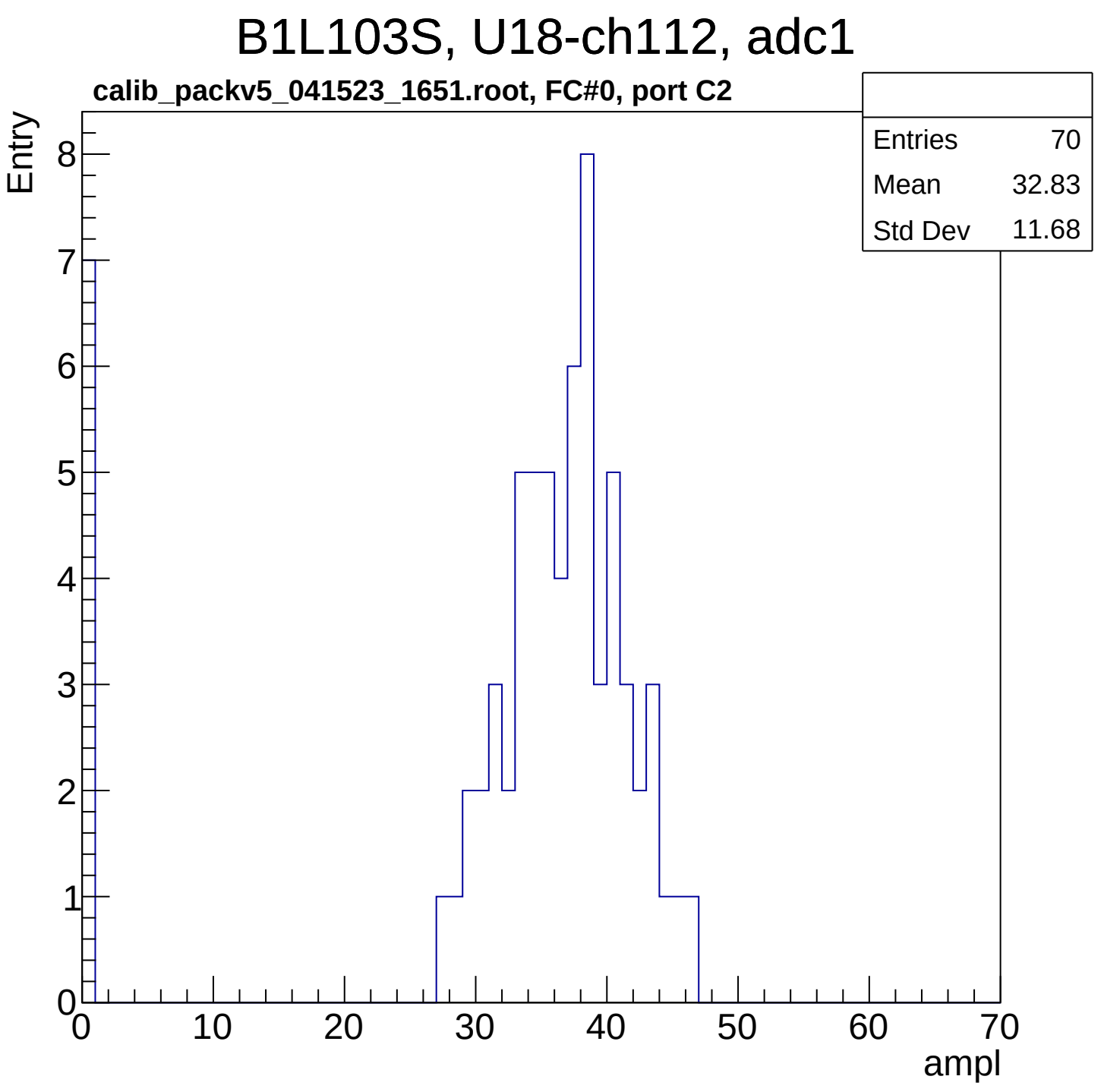

B1L103S, U18-ch111, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch112, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 93
Mean 25.84
Std Dev 11.55
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch112, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 32.83
Std Dev 11.68
Entry
ampl
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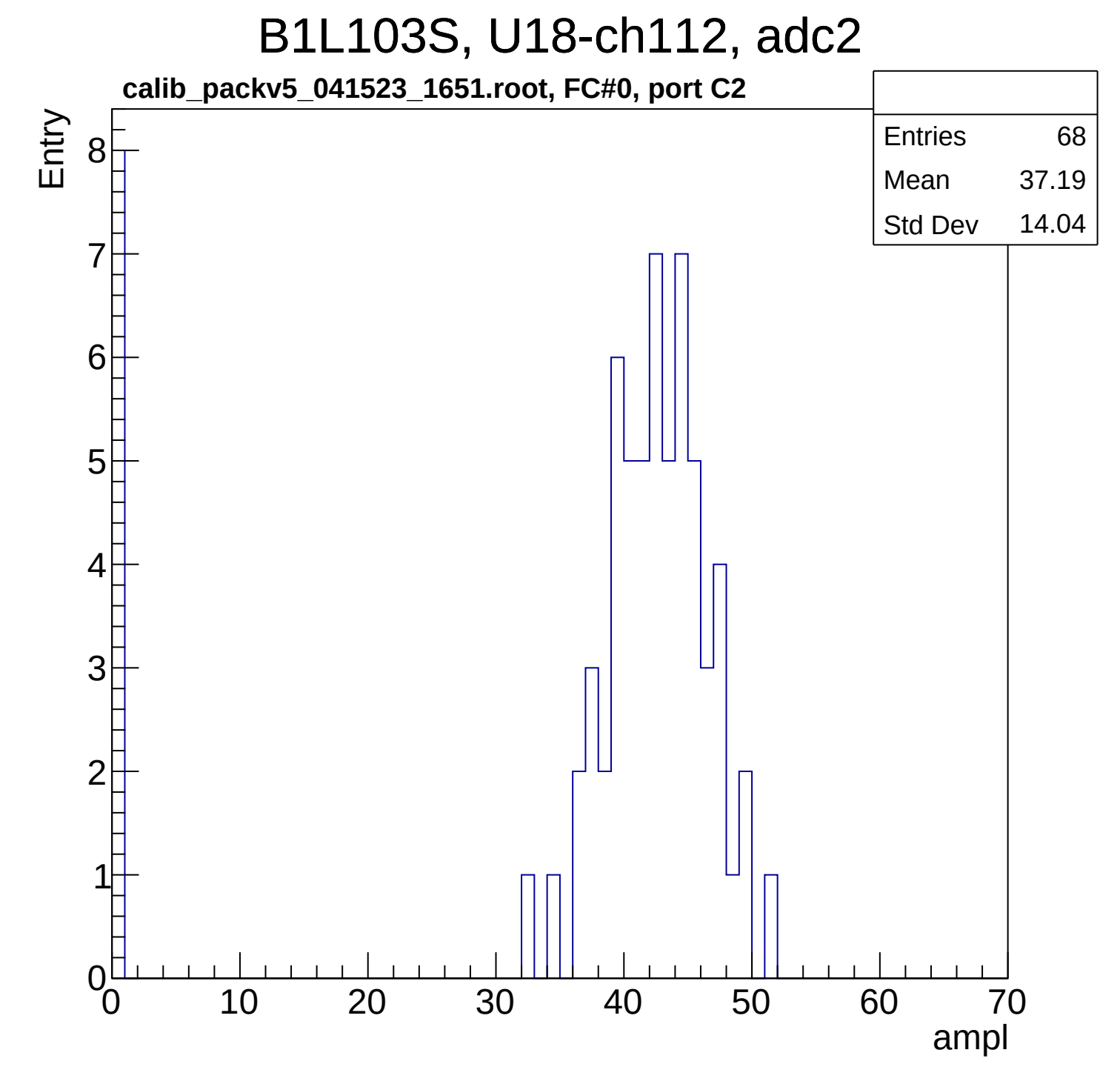
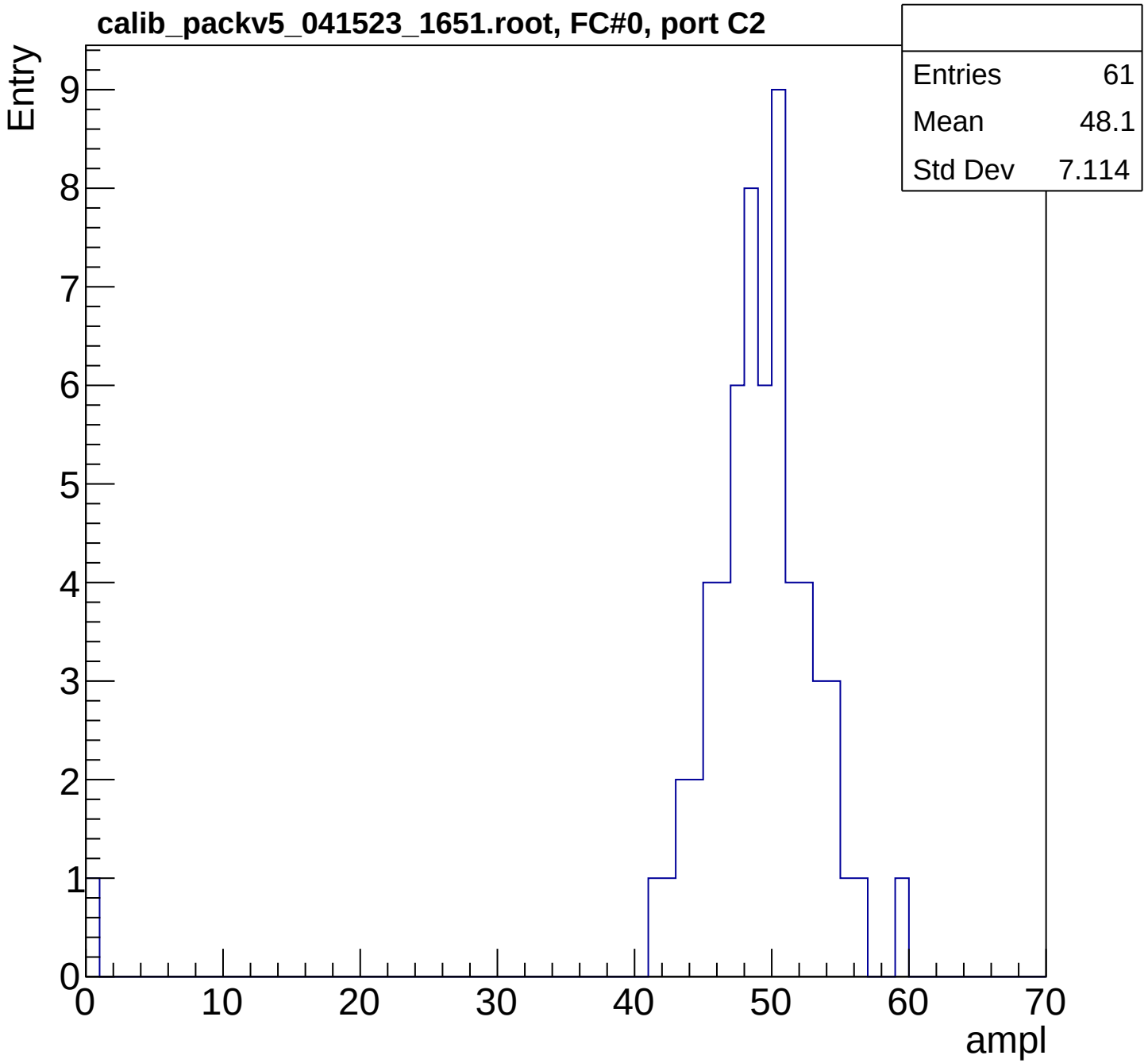
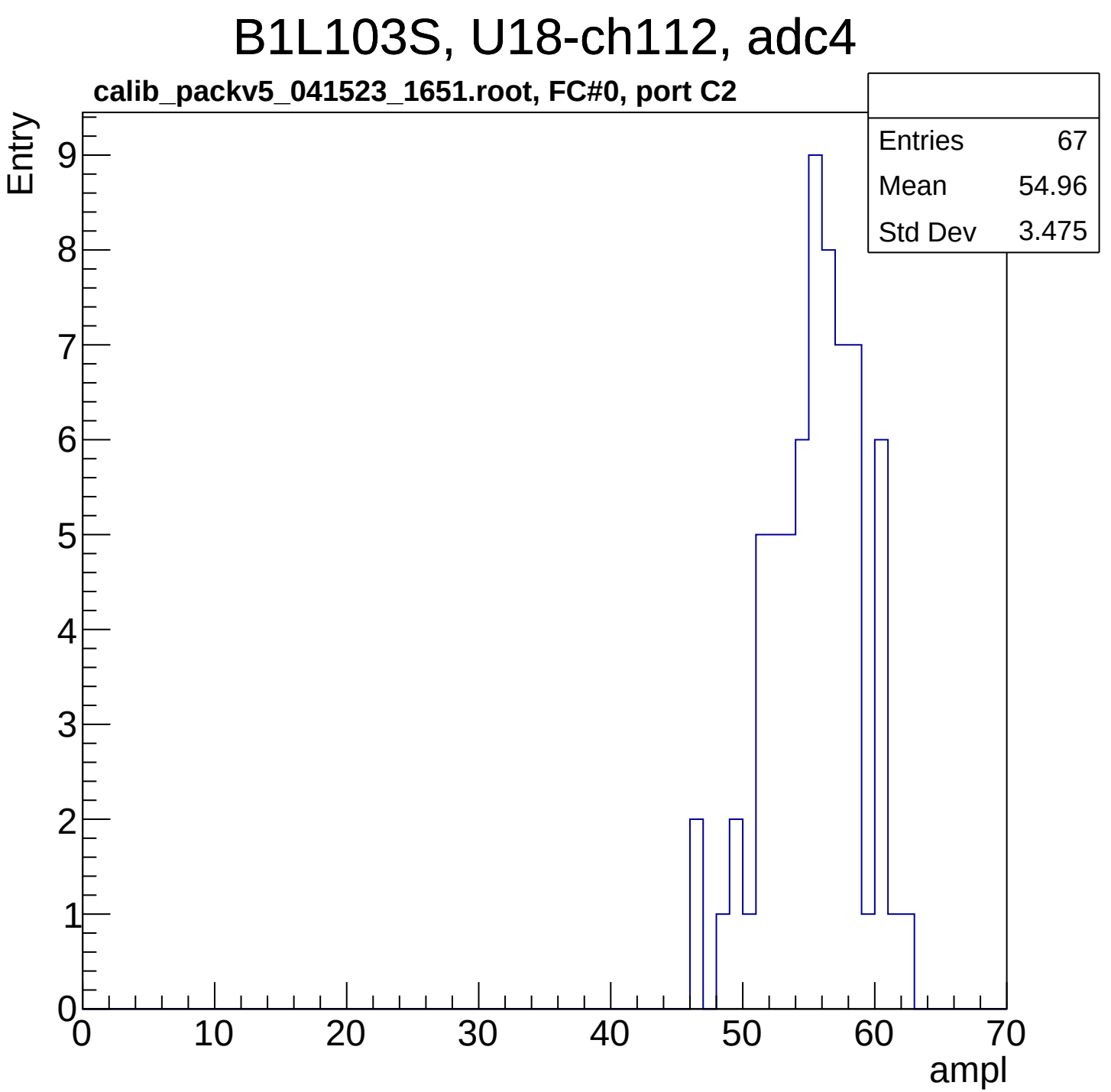
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch112, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 37.19
Std Dev 14.04
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch112, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 48.1
Std Dev 7.114
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U18-ch112, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 54.96
Std Dev 3.475
Entry
ampl
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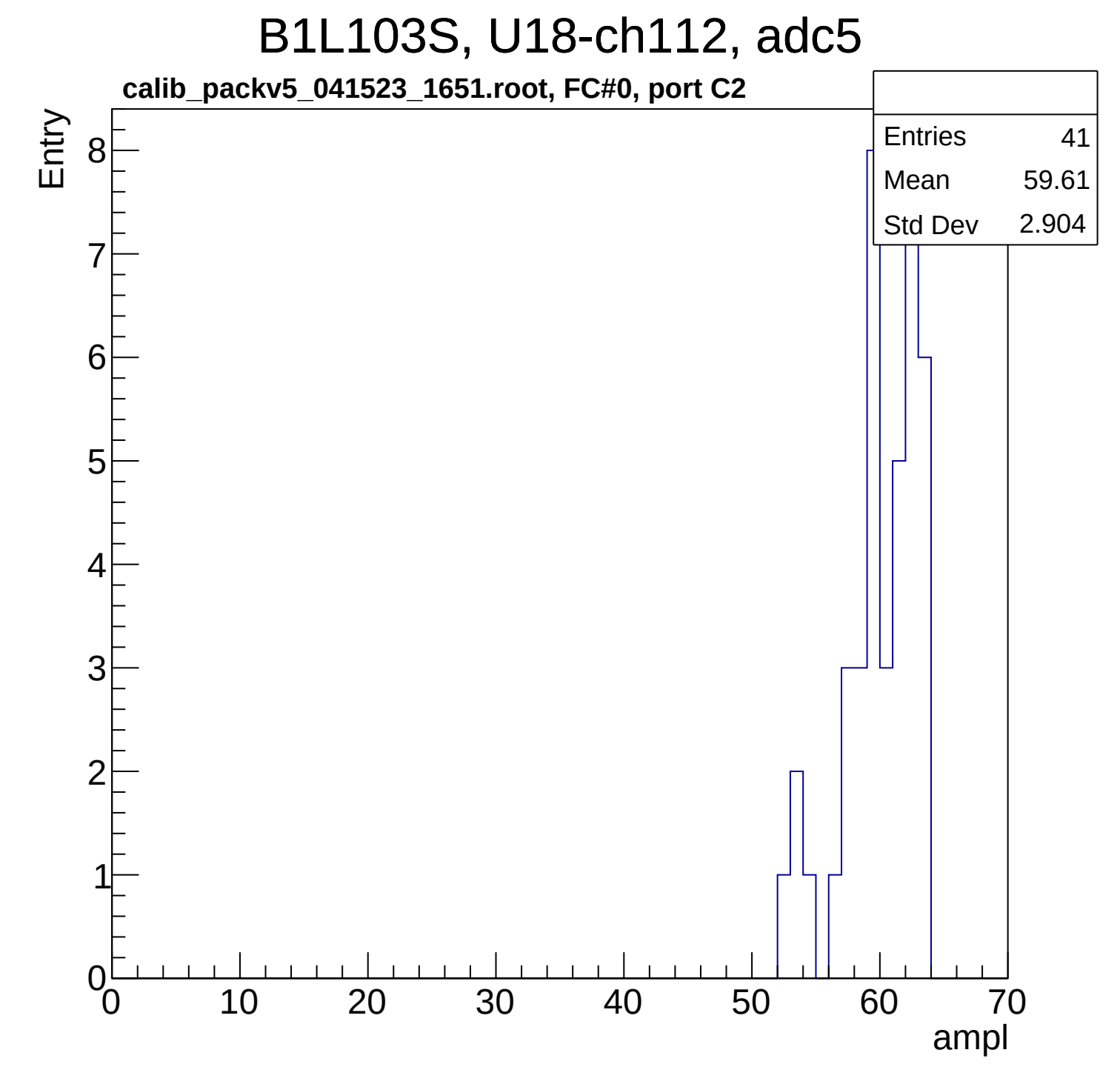
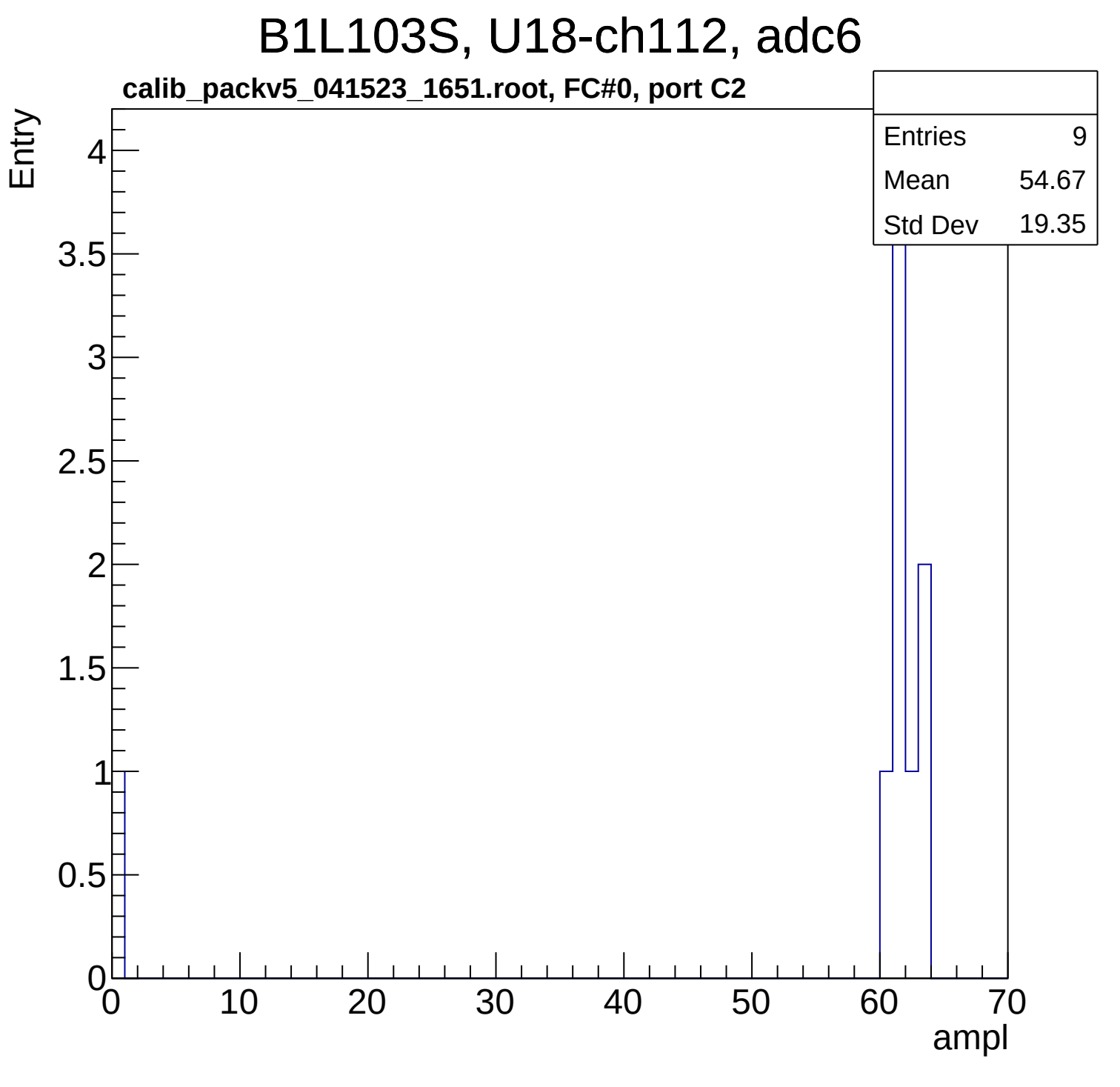
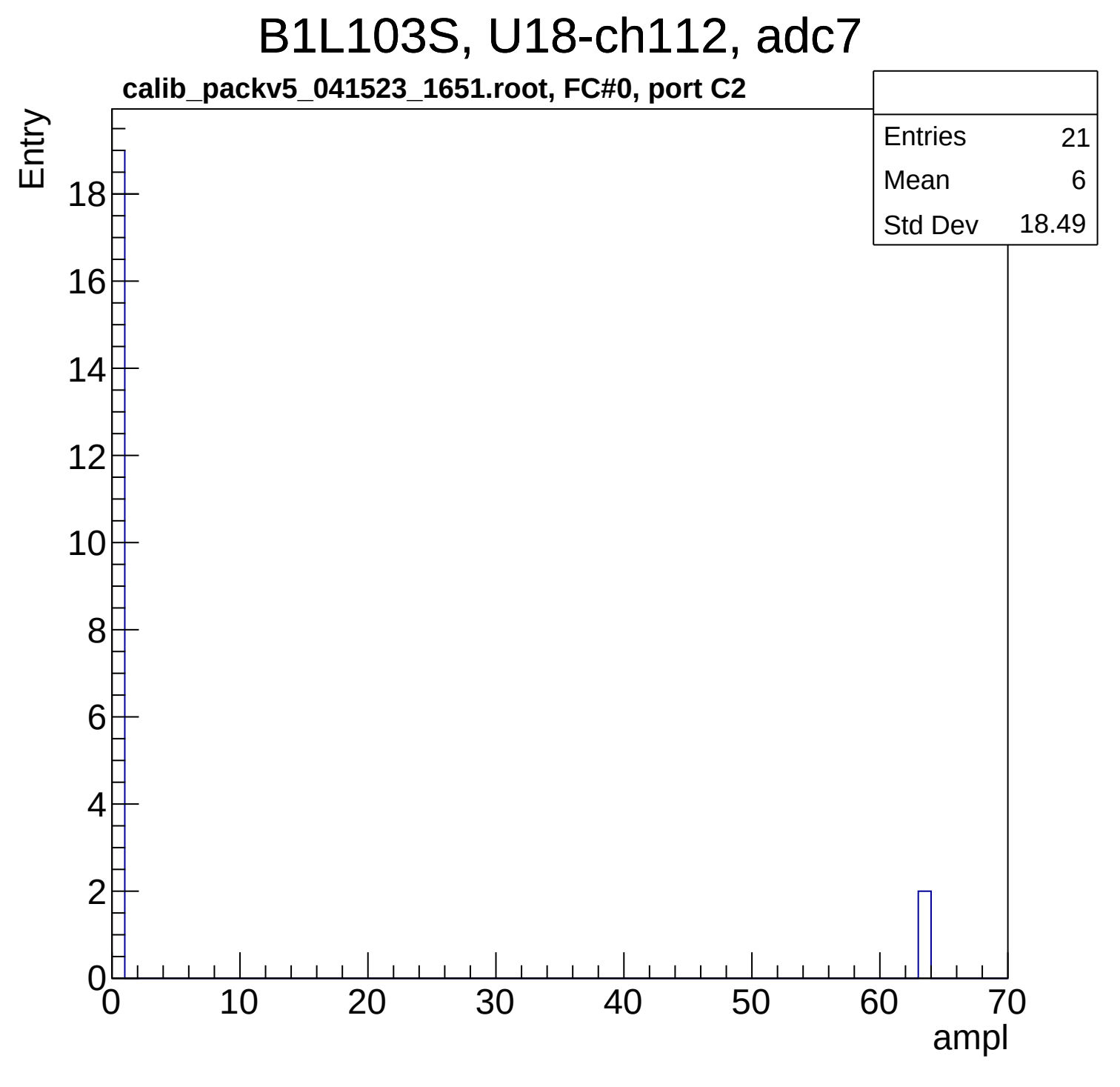
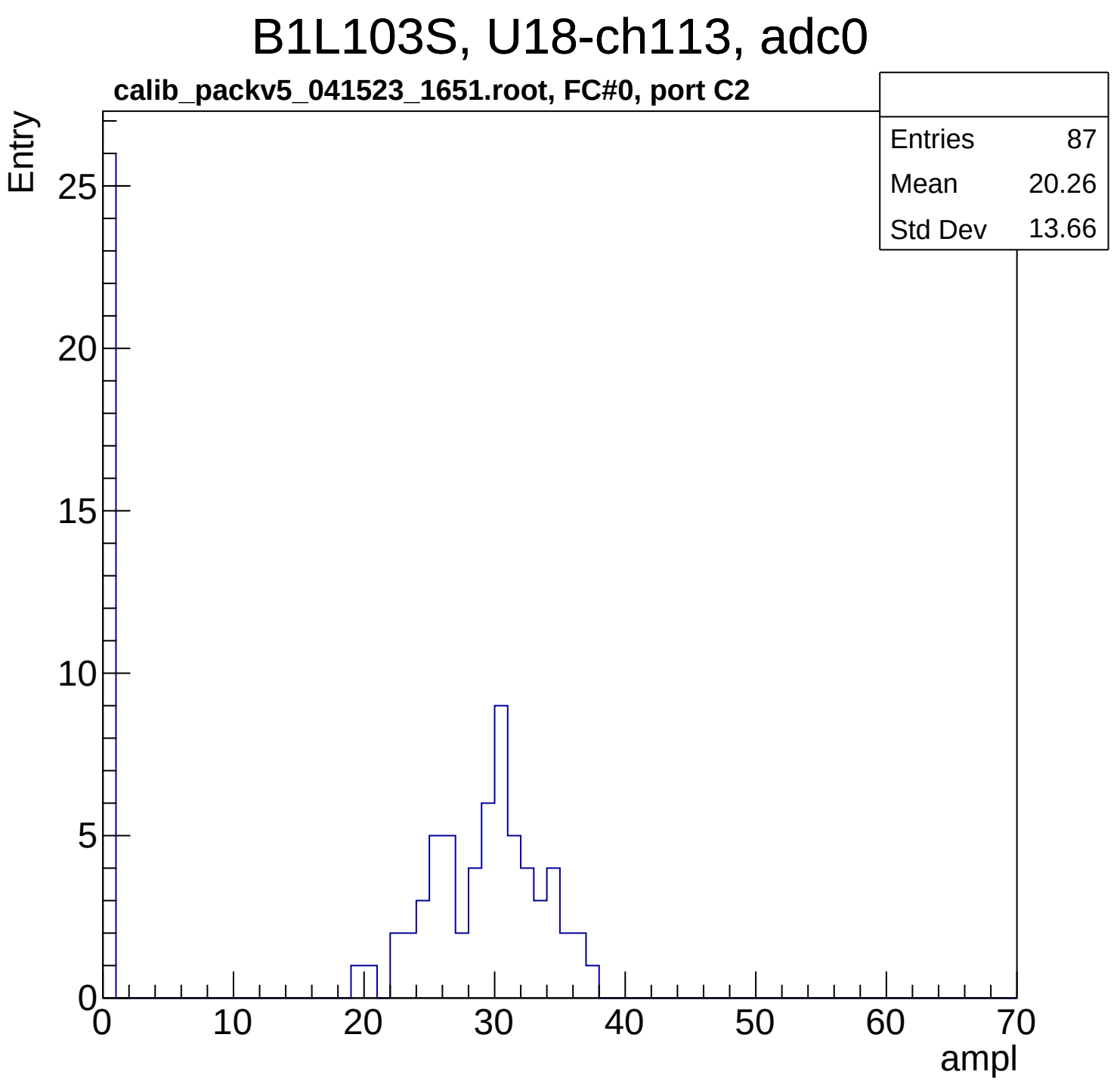
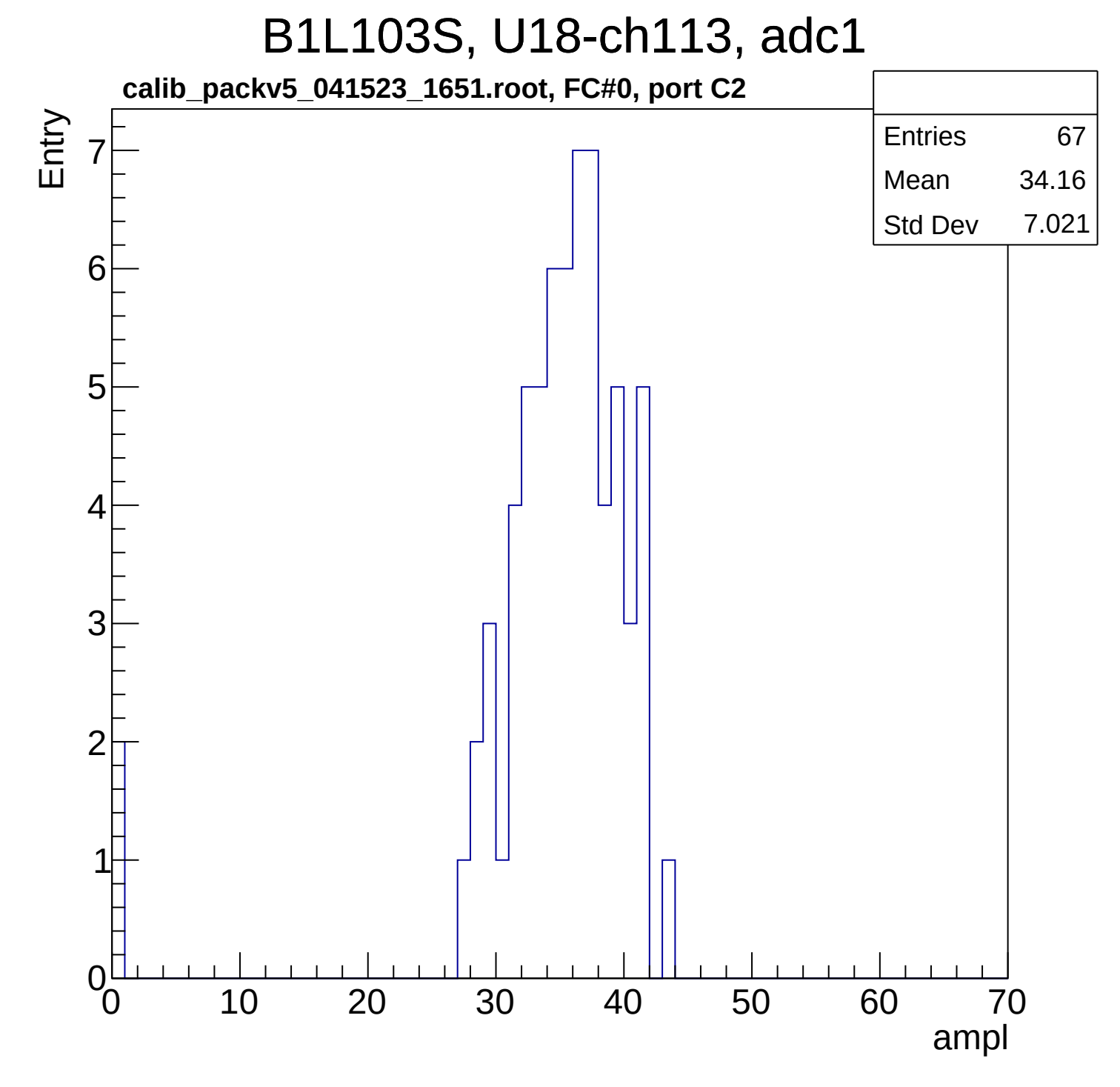
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

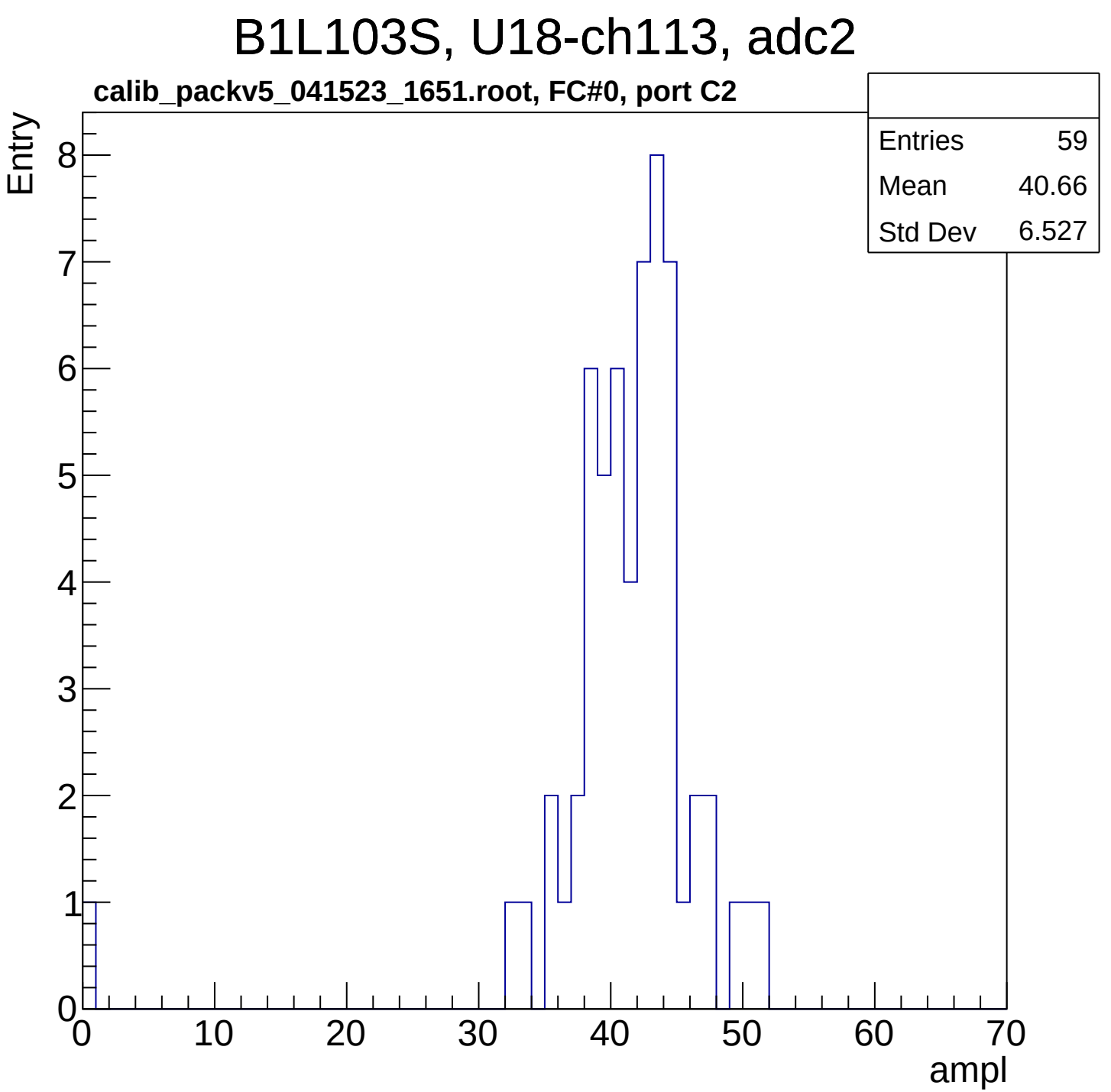

B1L103S, U18-ch112, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 41
Mean 59.61
Std Dev 2.904
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

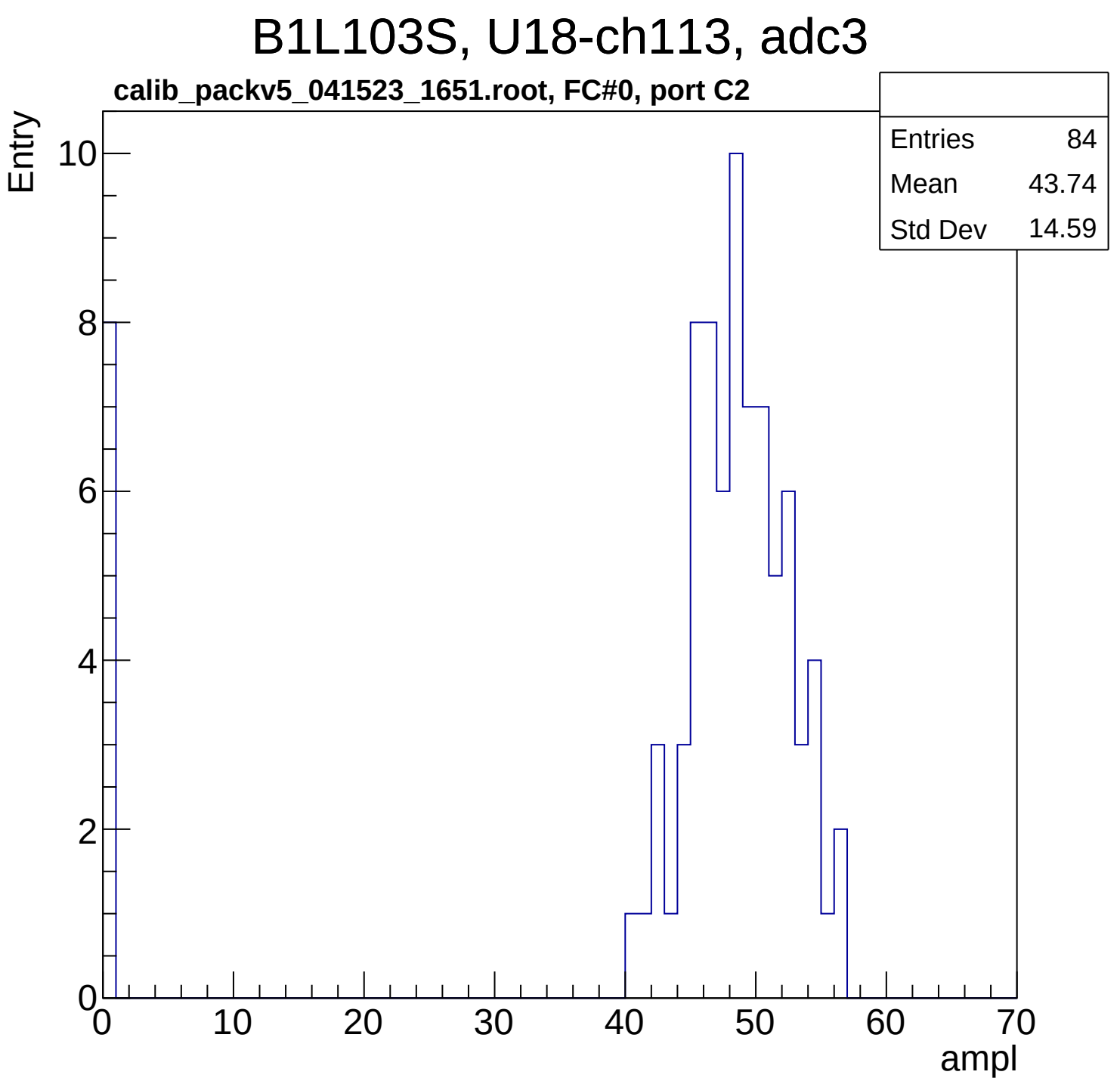

B1L103S, U18-ch112, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 9
Mean 54.67
Std Dev 19.35
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

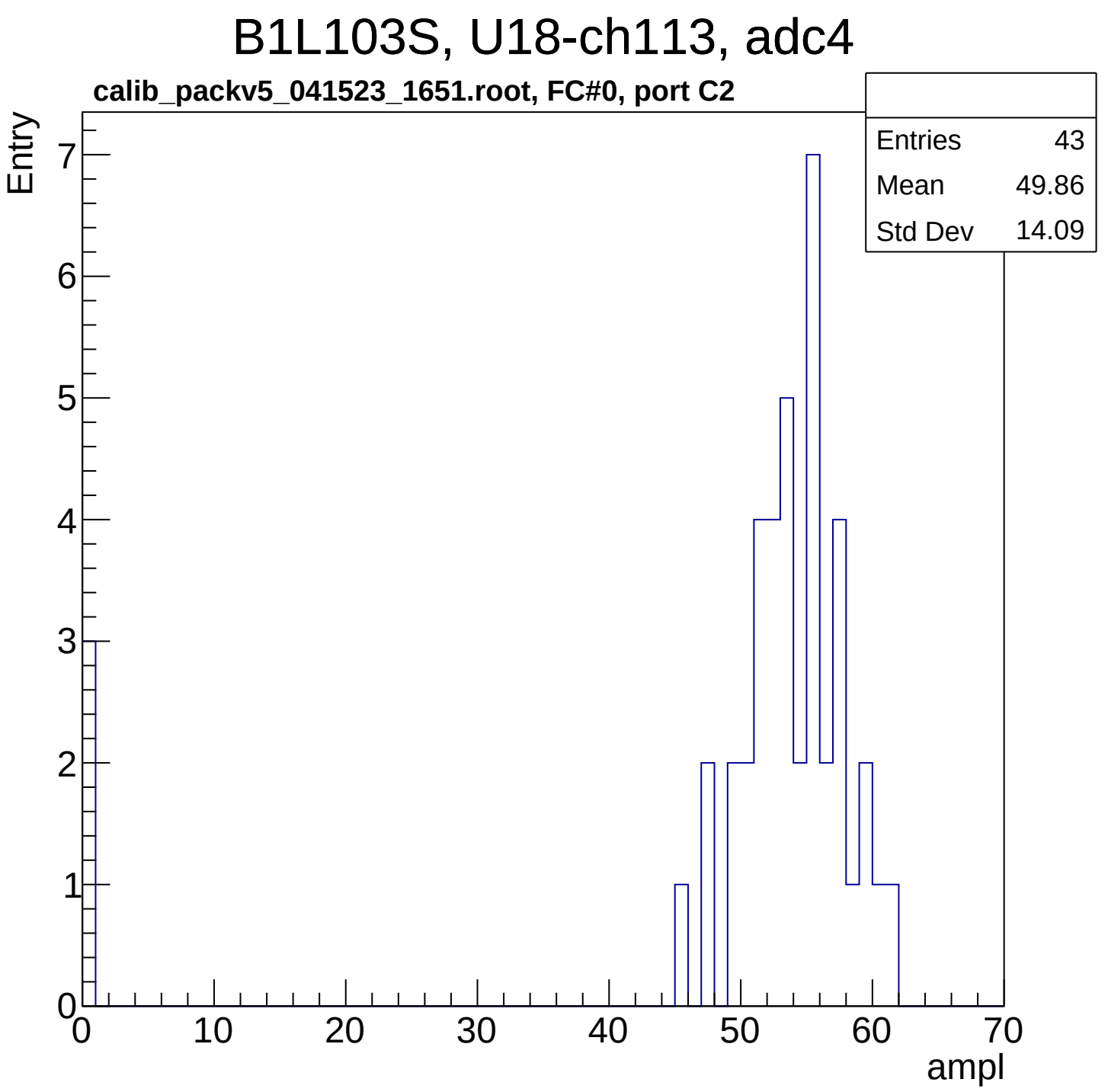

B1L103S, U18-ch112, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 6
Std Dev 18.49
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

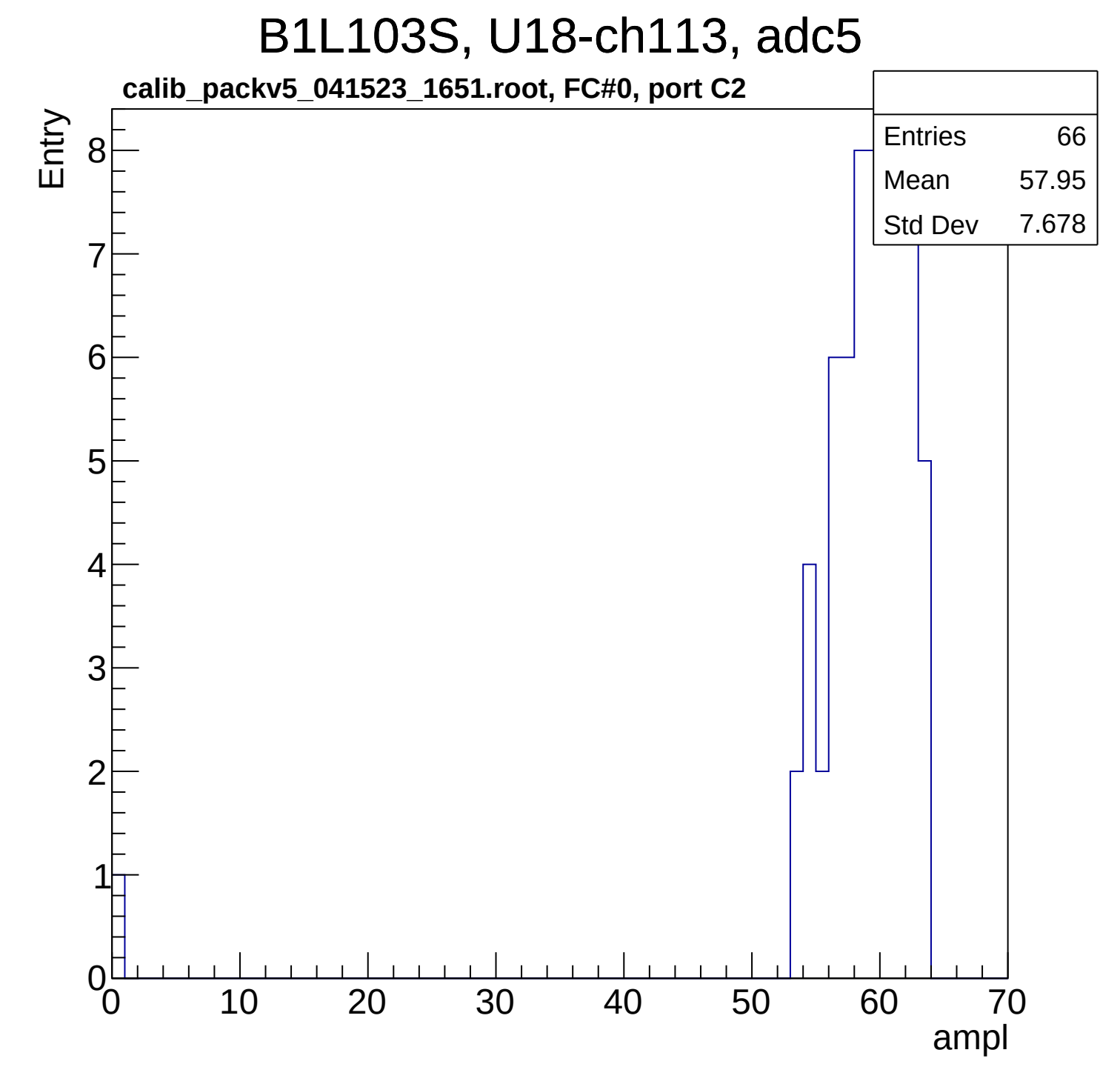

B1L103S, U18-ch113, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 87
Mean 20.26
Std Dev 13.66
Entry
0
5
10
15
20
25
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch113, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 34.16
Std Dev 7.021
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U18-ch113, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 40.66
Std Dev 6.527
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch113, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 43.74
Std Dev 14.59
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch113, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 43
Mean 49.86
Std Dev 14.09
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U18-ch113, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 57.95
Std Dev 7.678
Entry
ampl
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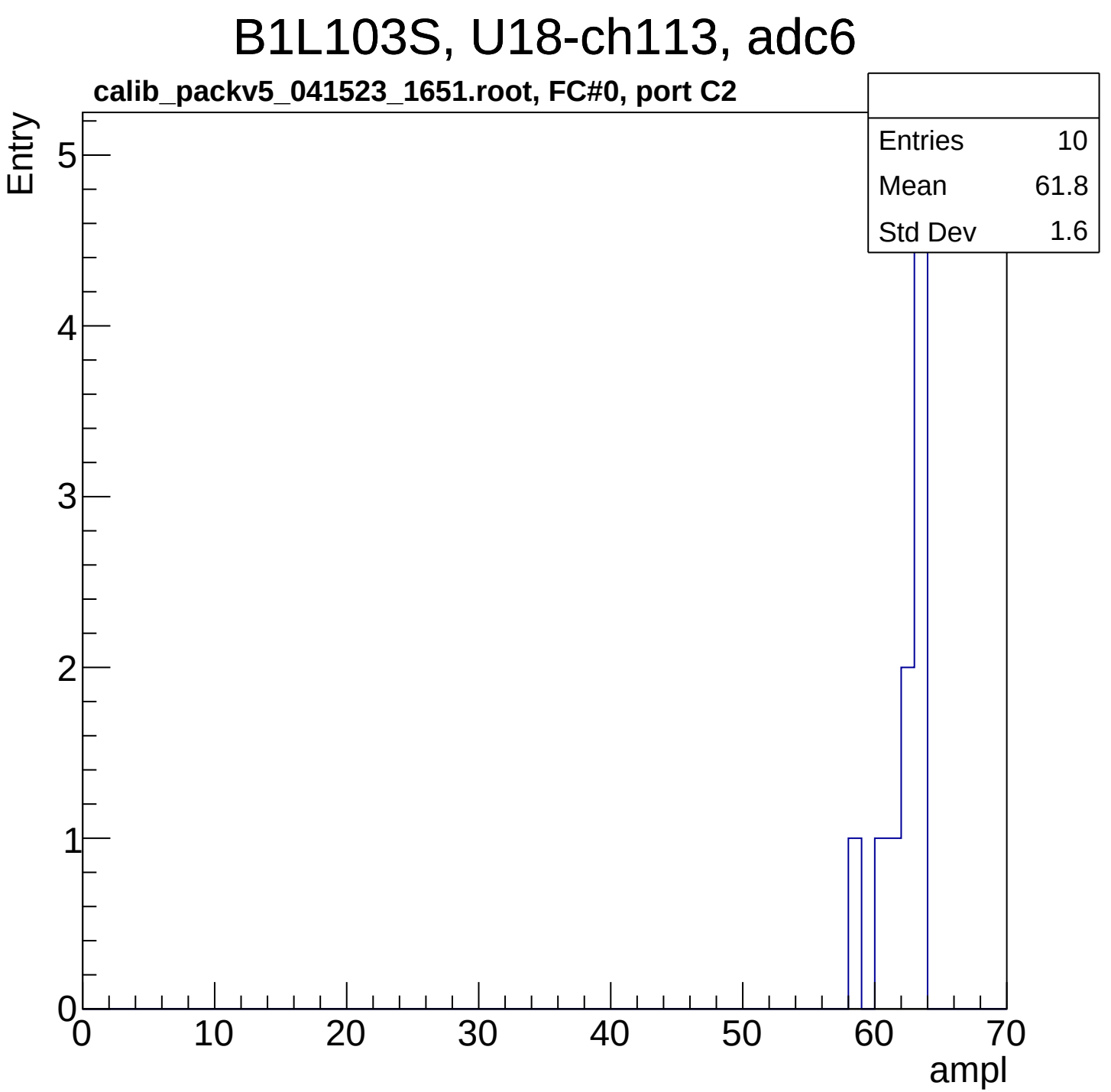
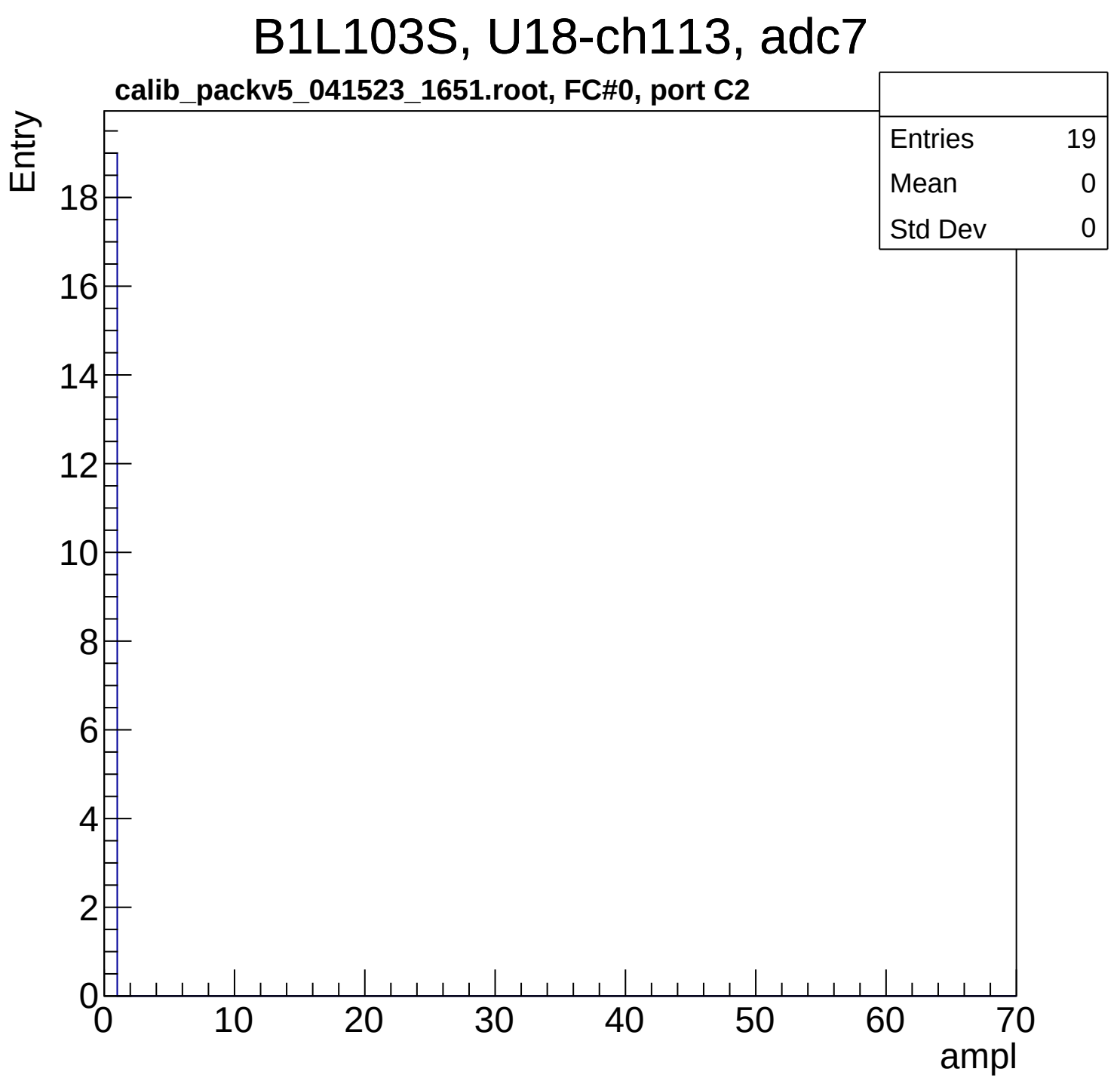
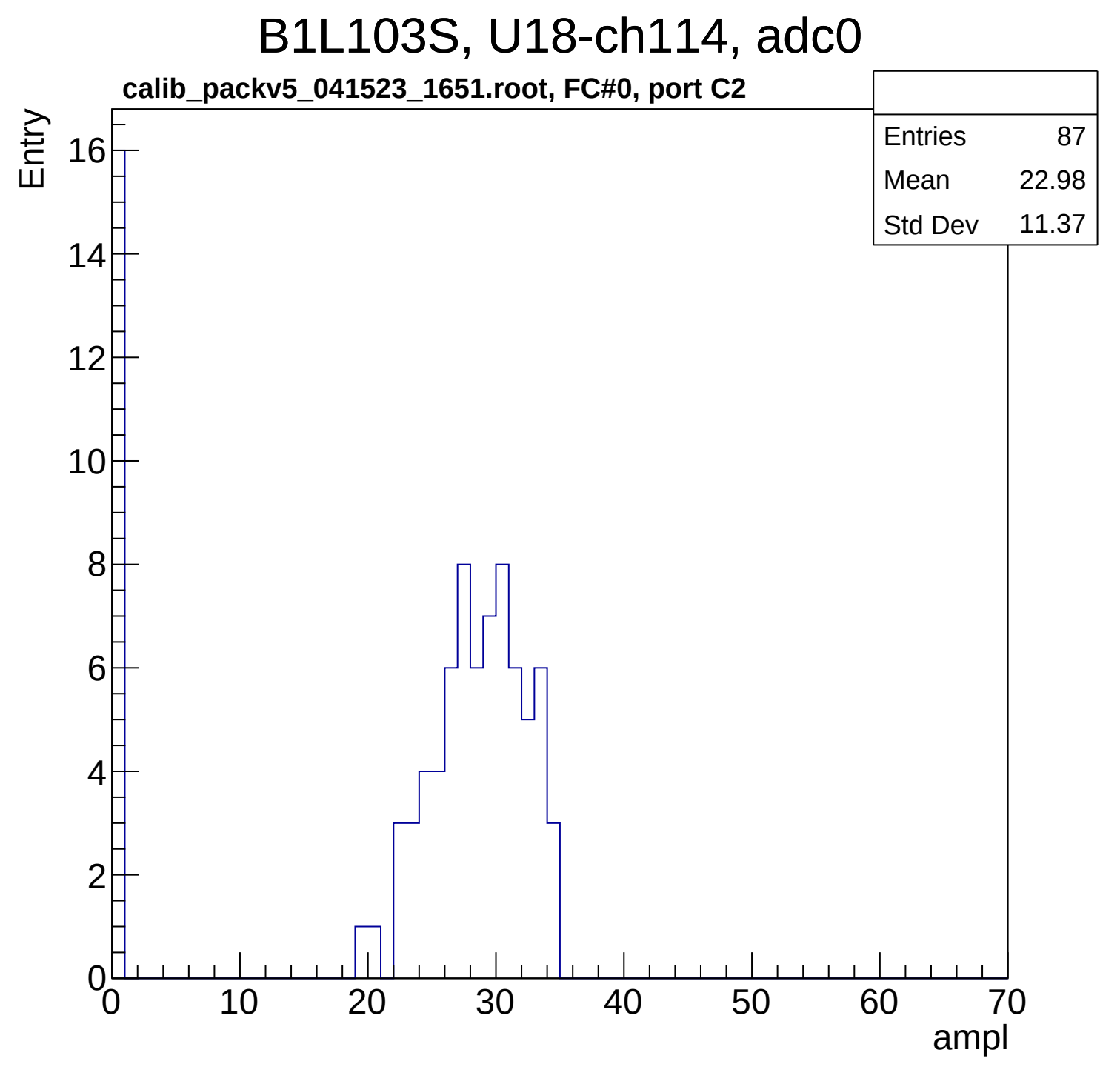
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch113, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 61.8
Std Dev 1.6
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch113, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch114, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 87
Mean 22.98
Std Dev 11.37
Entry
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4
6
8
10
12
14
16
0
10
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30
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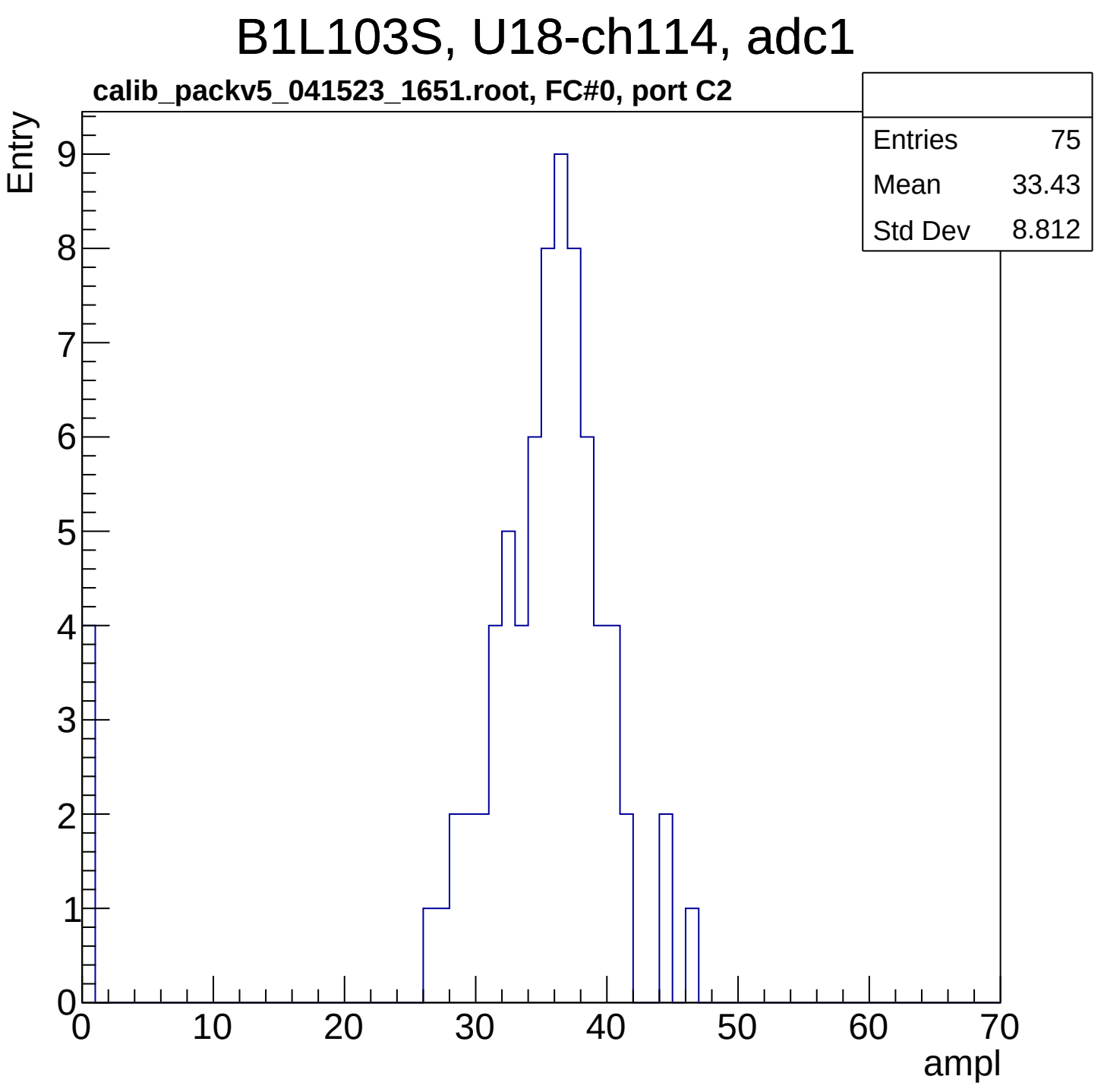
50
60
70
ampl


B1L103S, U18-ch114, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 33.43
Std Dev 8.812
Entry
ampl
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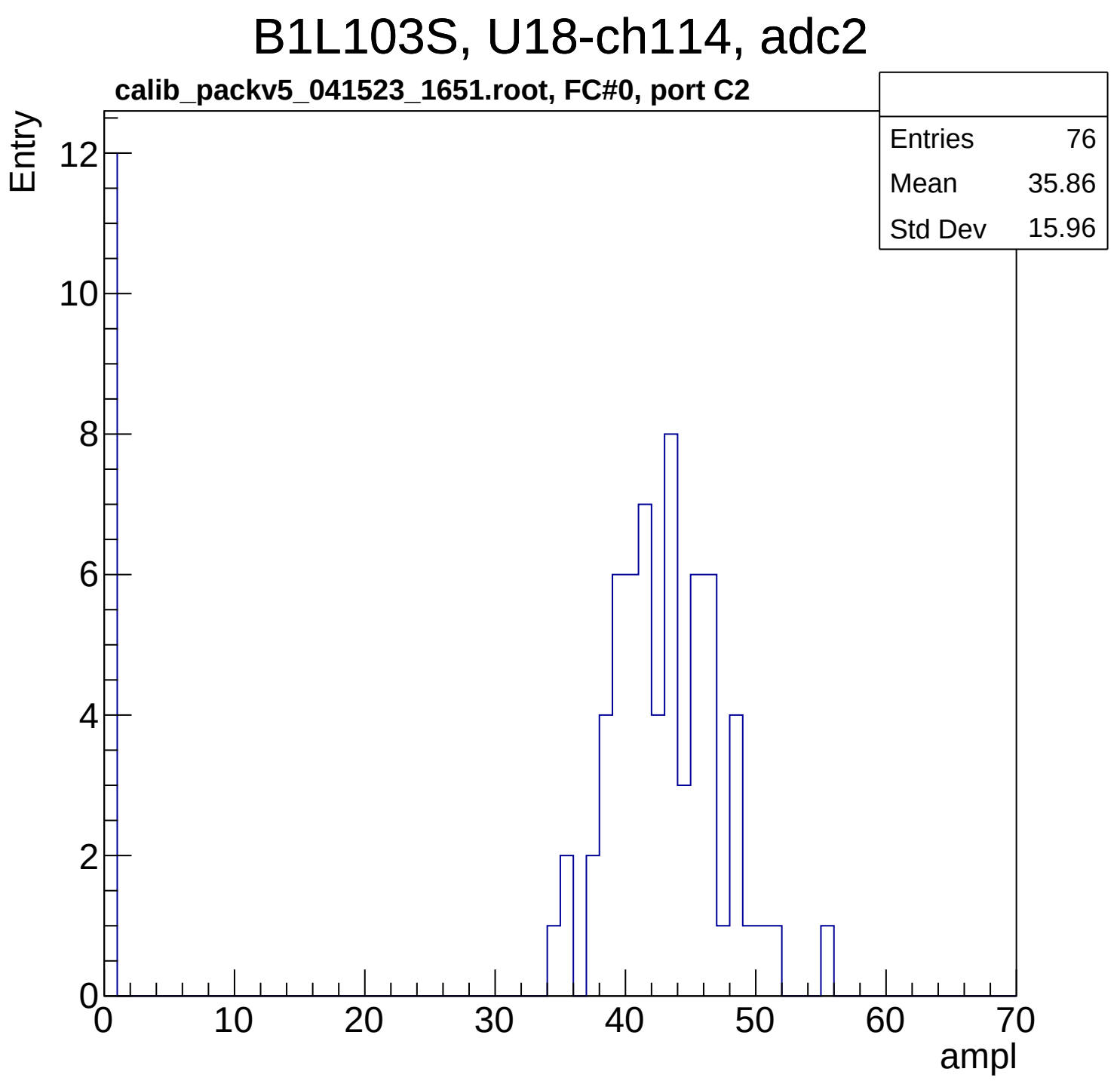
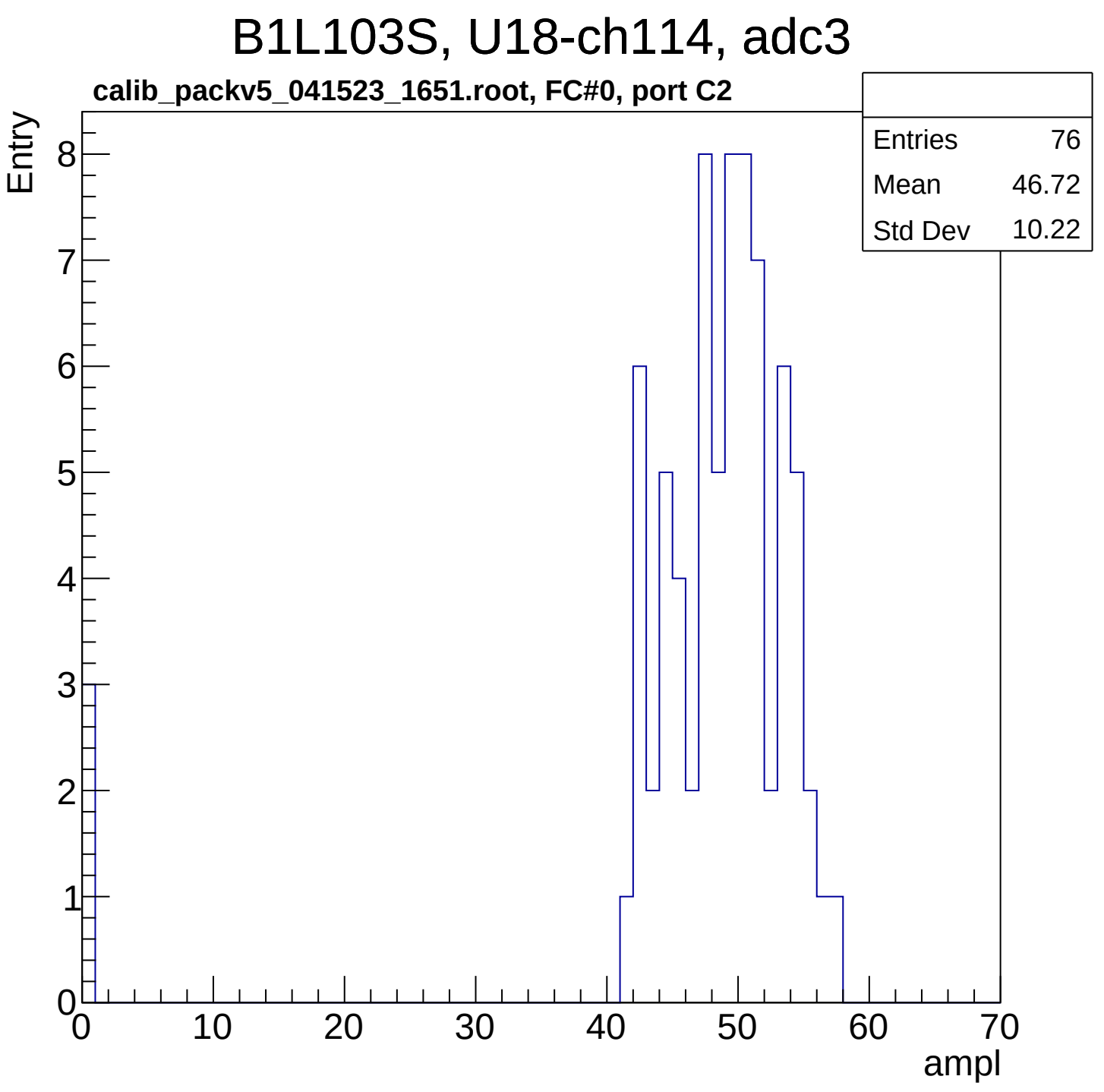
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U18-ch114, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 35.86
Std Dev 15.96
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70


B1L103S, U18-ch114, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 46.72
Std Dev 10.22
Entry
ampl
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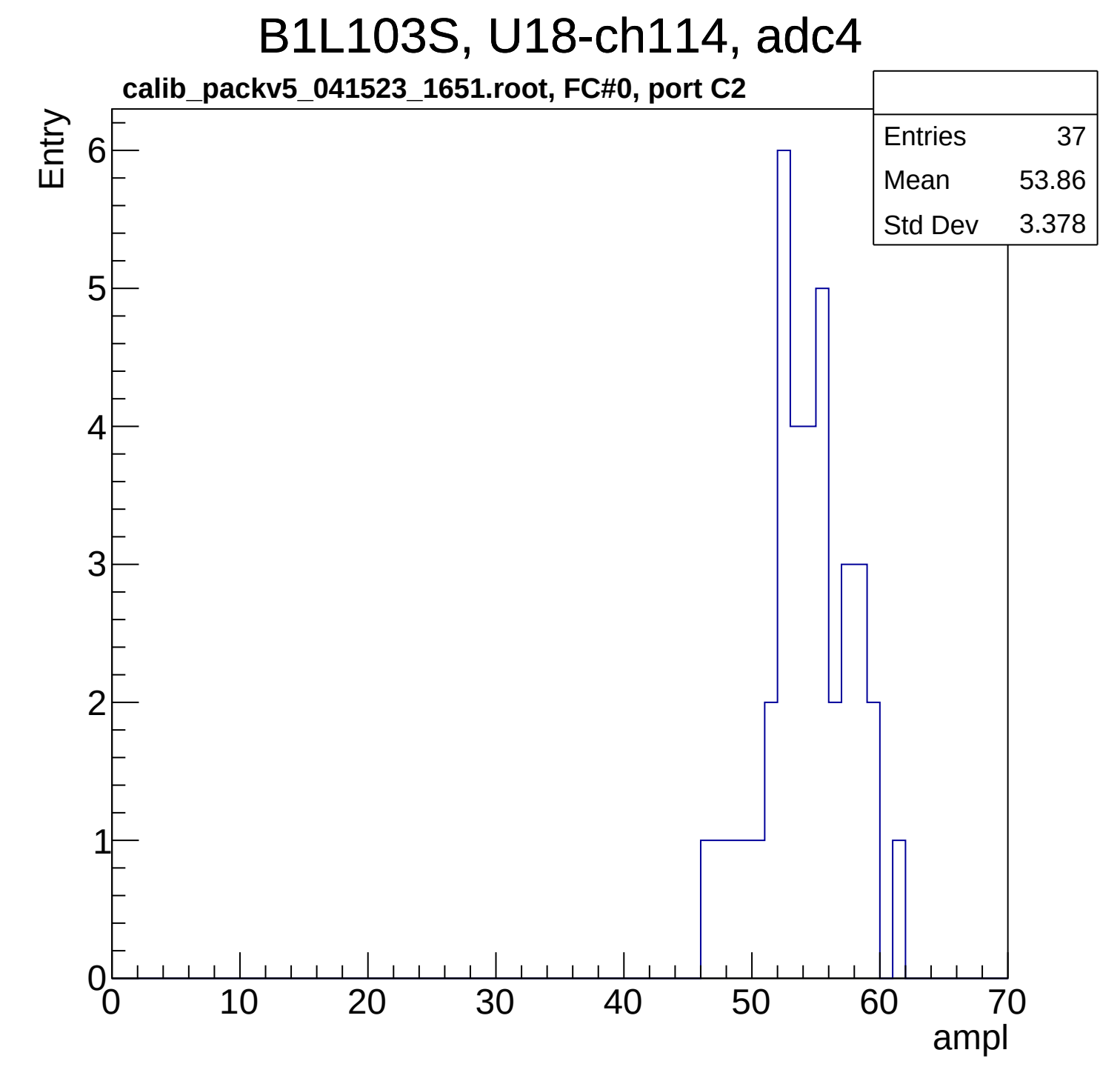
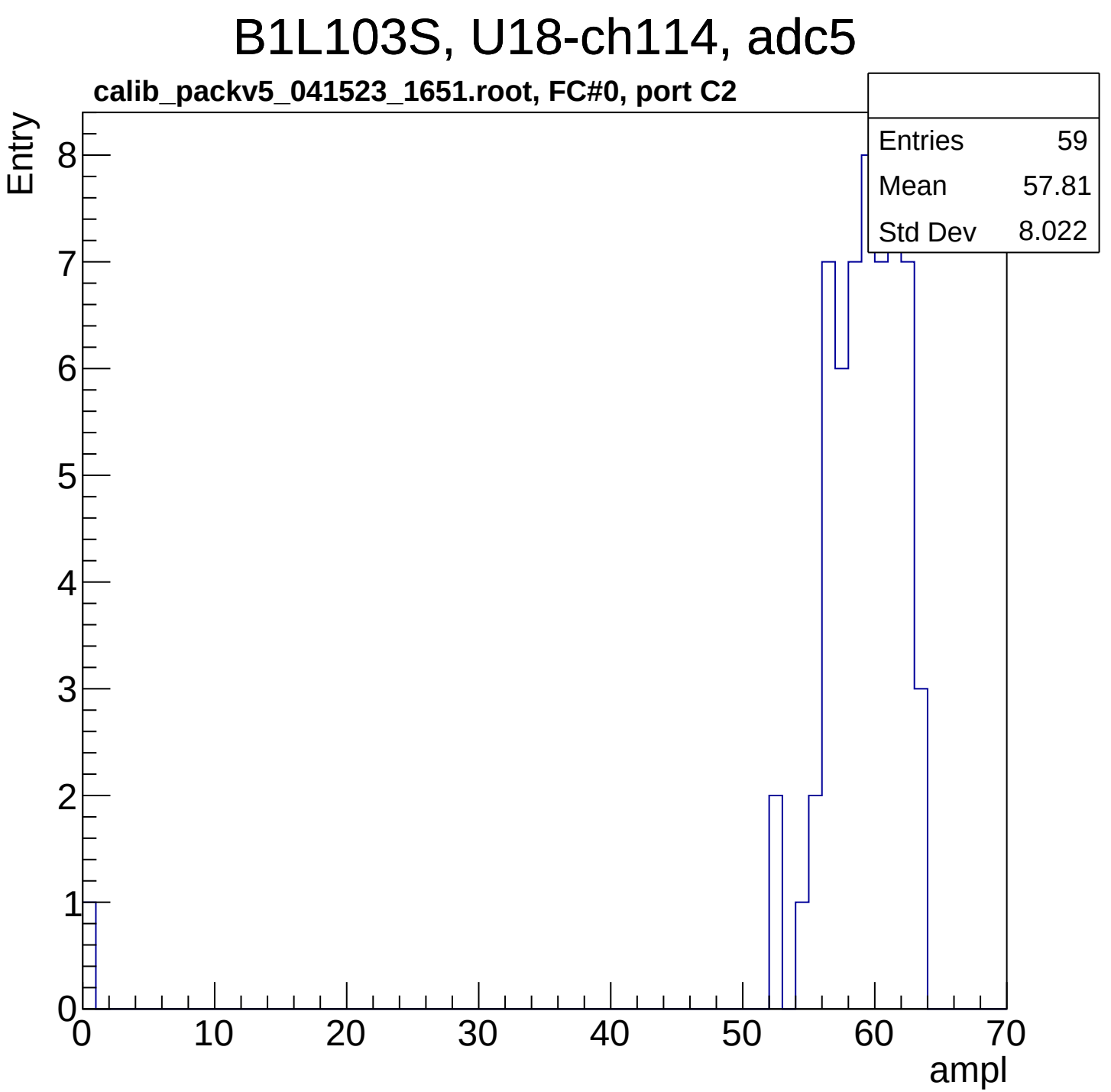
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch114, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 37
Mean 53.86
Std Dev 3.378
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U18-ch114, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 57.81
Std Dev 8.022
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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60
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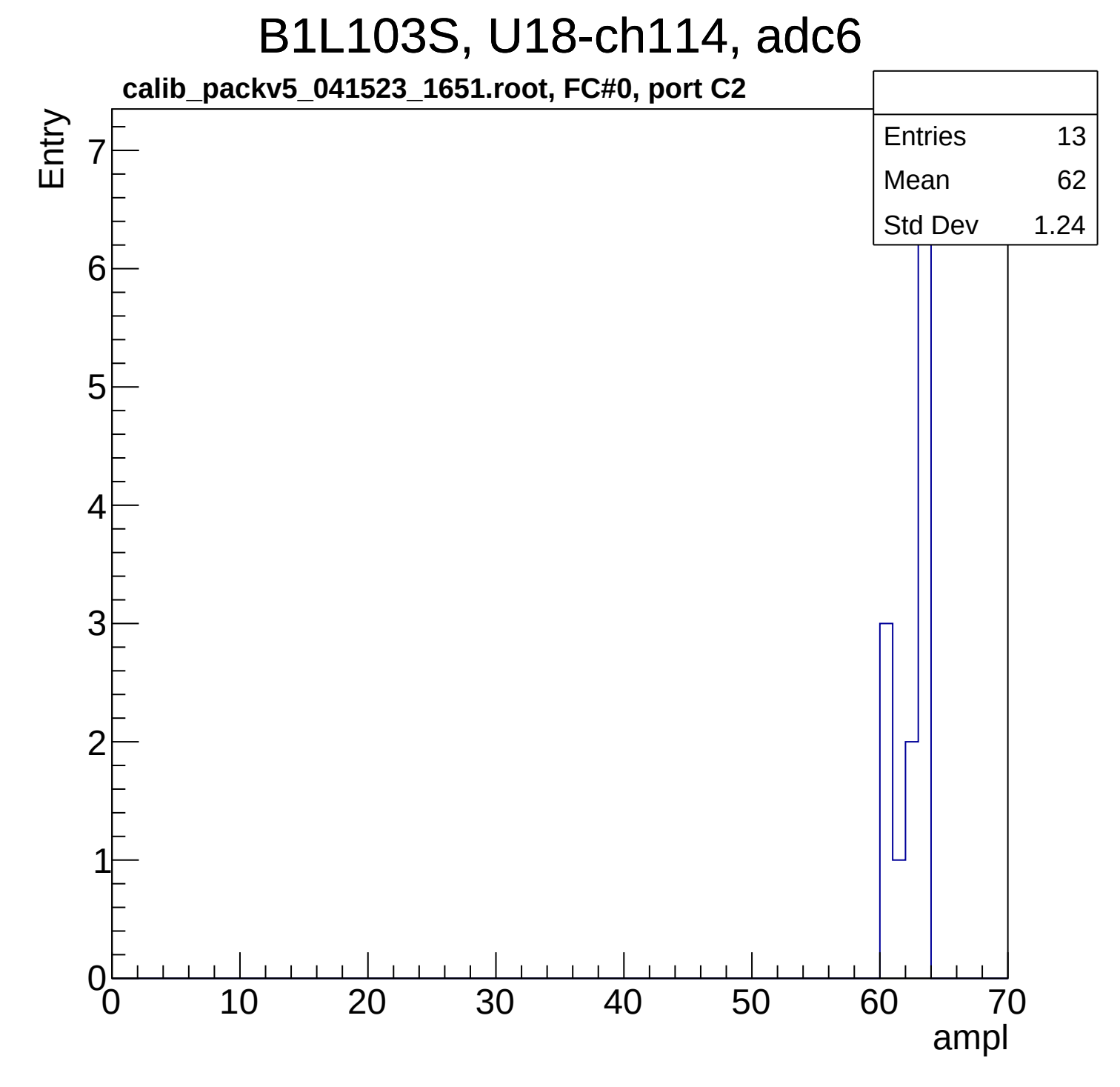
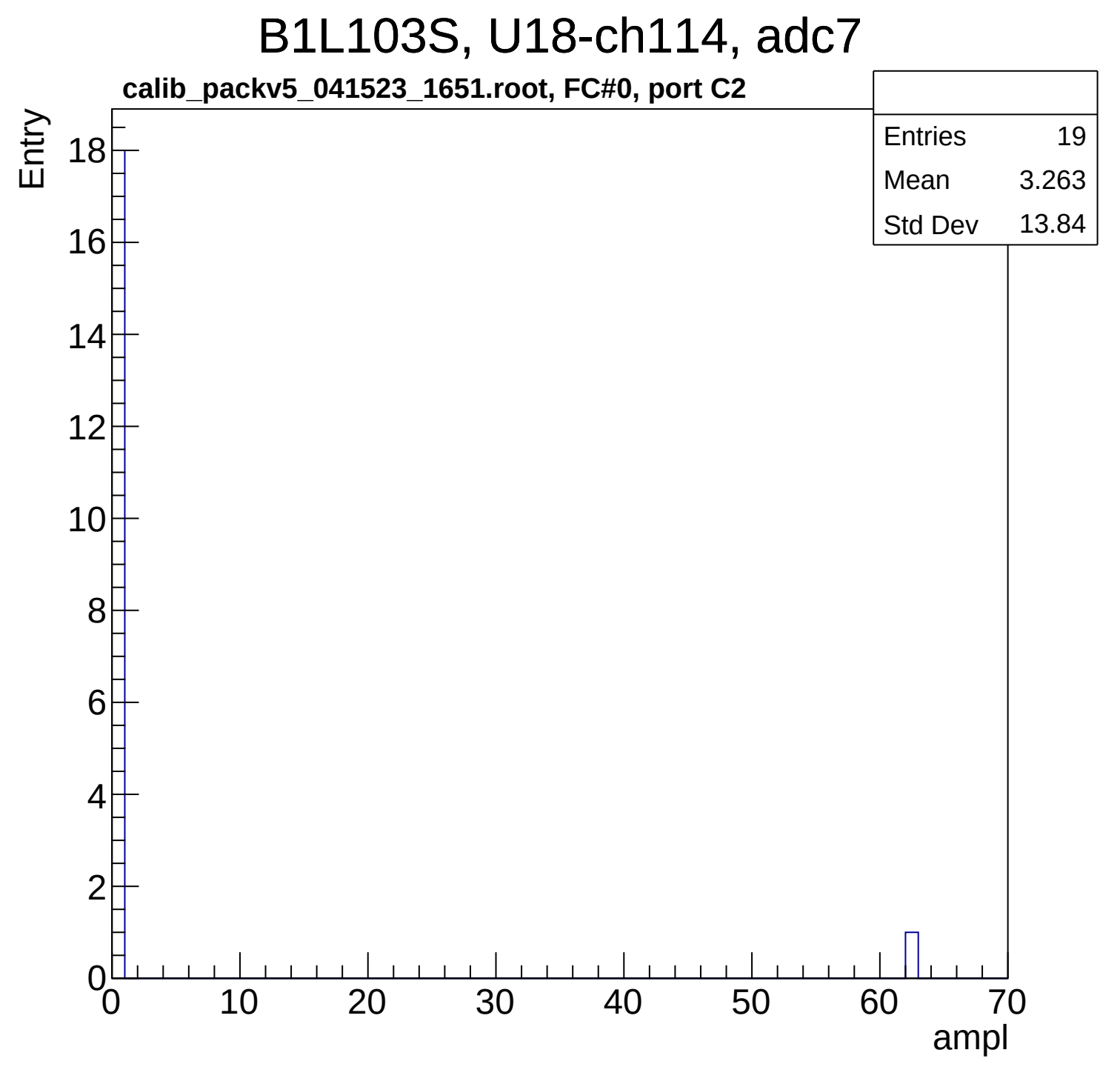

B1L103S, U18-ch114, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 13
Mean 62
Std Dev 1.24
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U18-ch114, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 3.263
Std Dev 13.84
Entry
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6
8
10
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14
16
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0
10
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30
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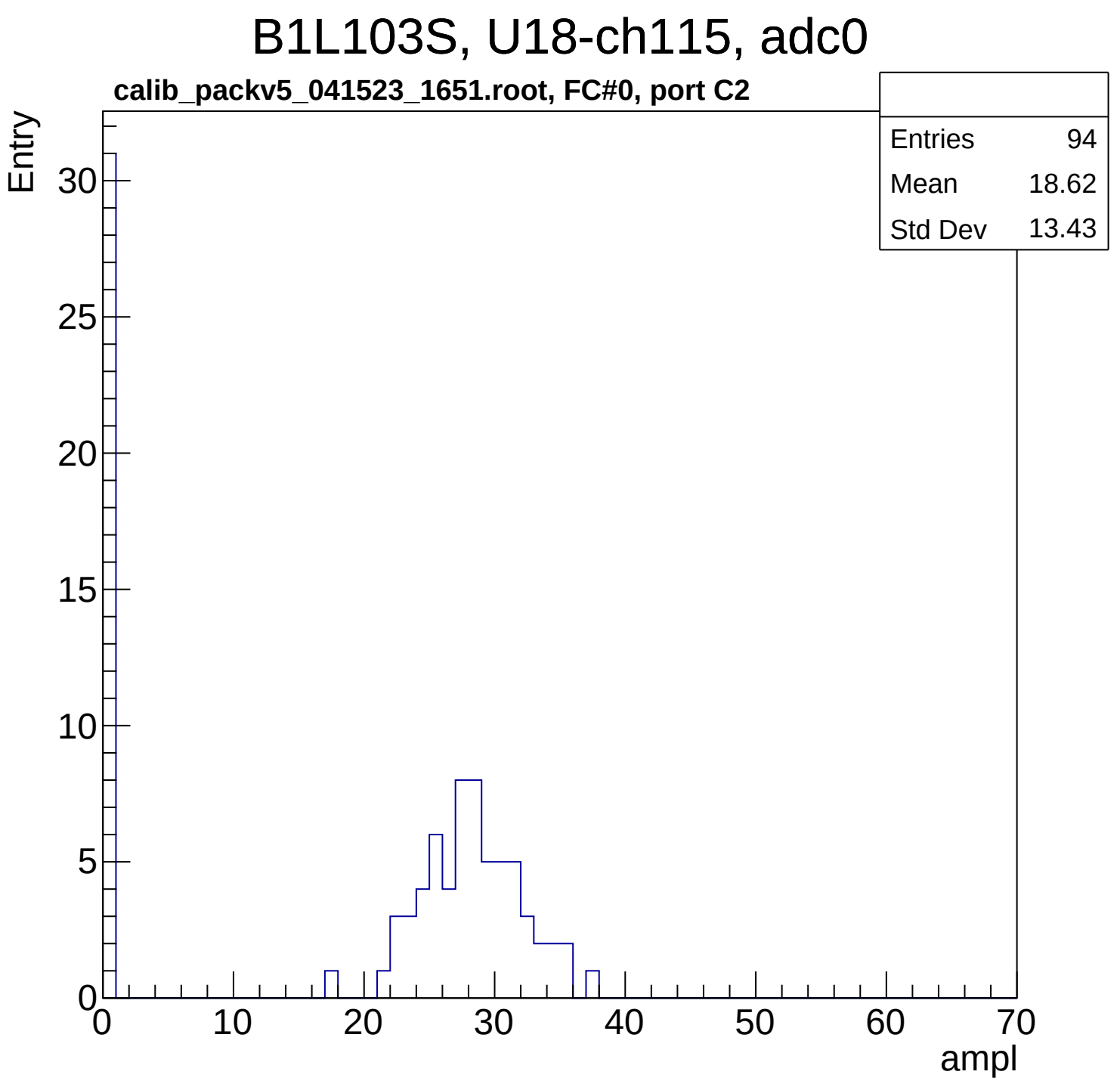
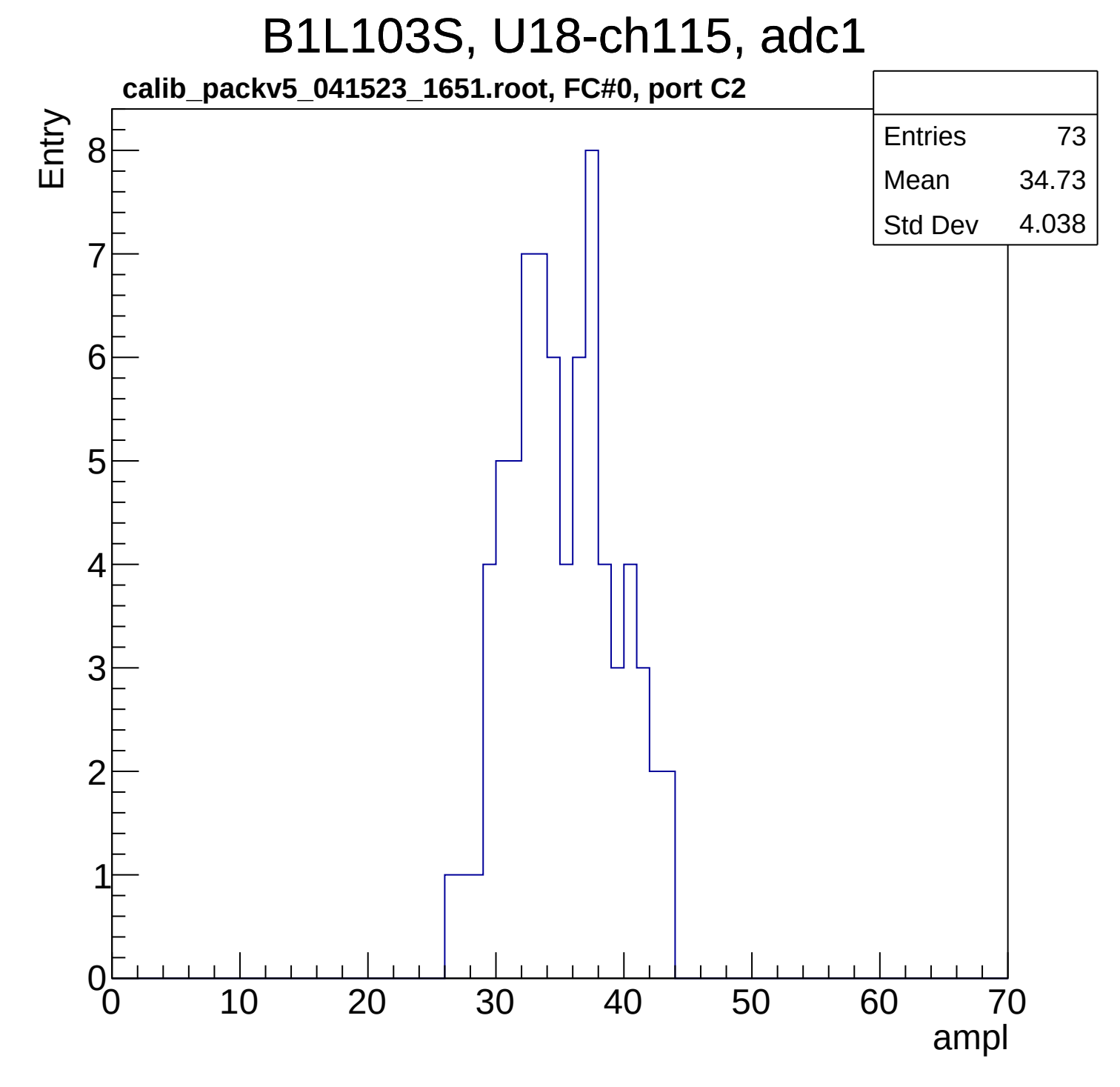
70
ampl


B1L103S, U18-ch115, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 94
Mean 18.62
Std Dev 13.43
Entry
0
5
10
15
20
25
30
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch115, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 34.73
Std Dev 4.038
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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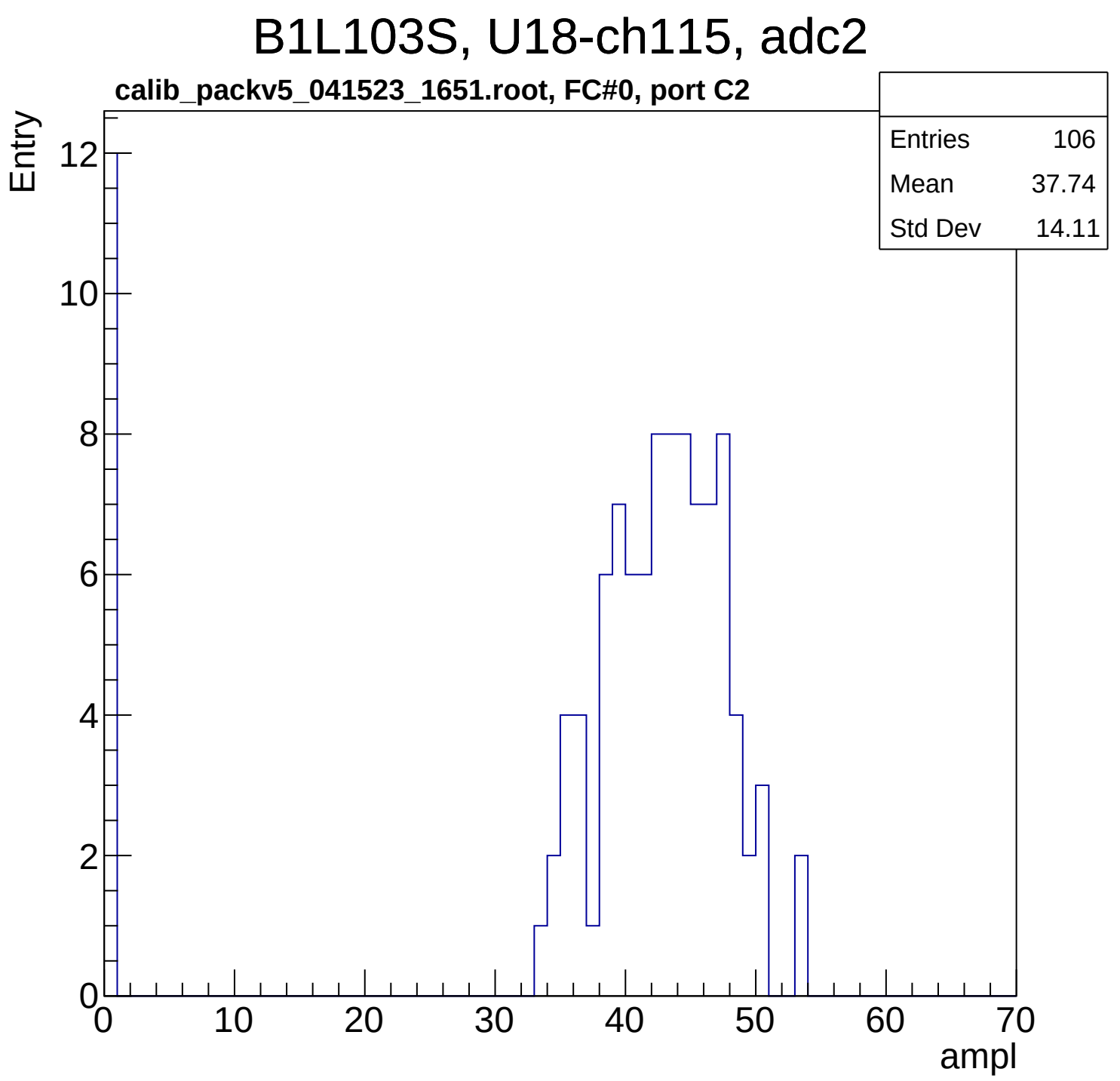
40
50
60
70


B1L103S, U18-ch115, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 106
Mean 37.74
Std Dev 14.11
Entry
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2
4
6
8
10
12
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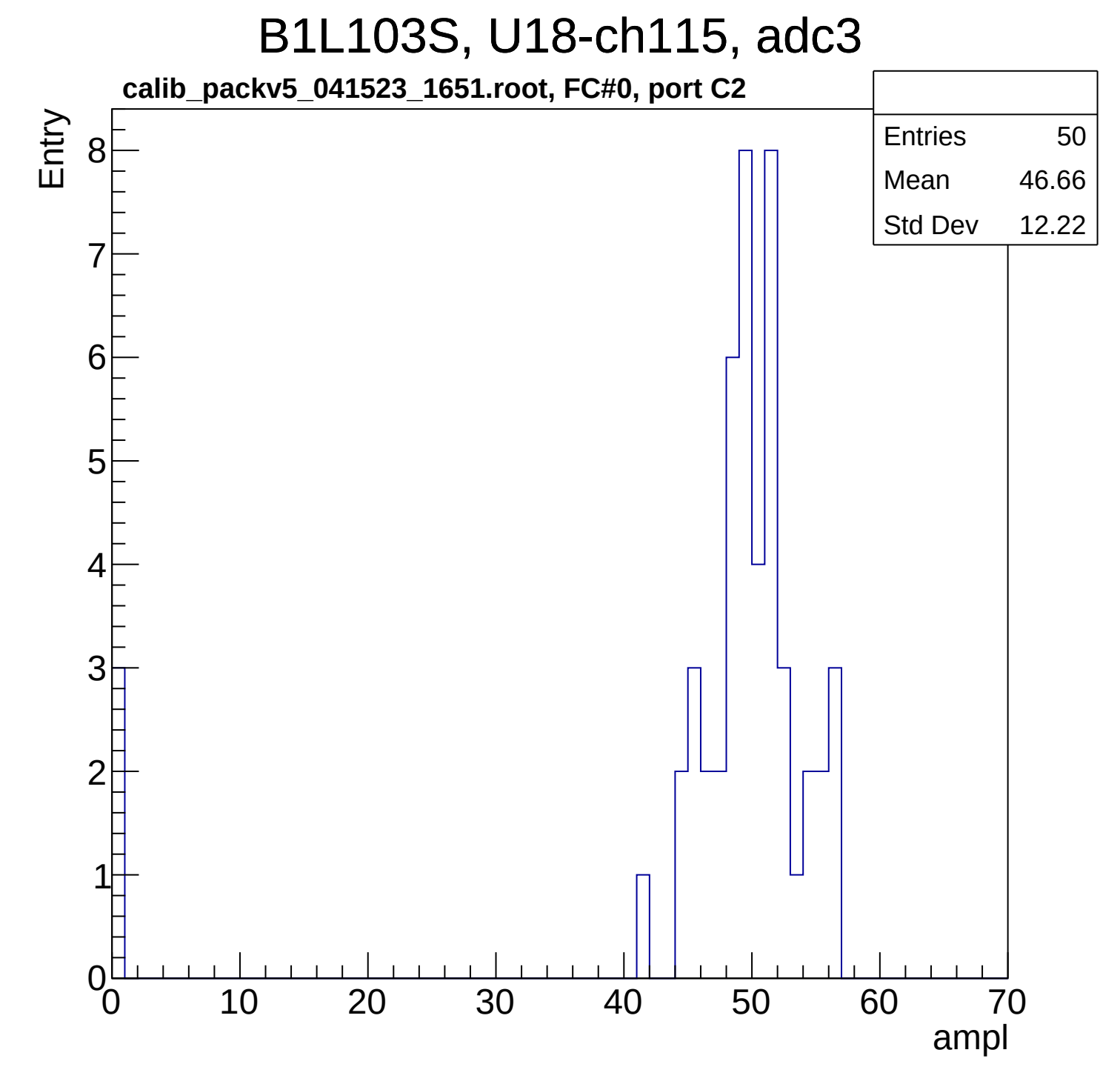
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch115, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 46.66
Std Dev 12.22
Entry
ampl
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1
2
3
4
5
6
7
8
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60
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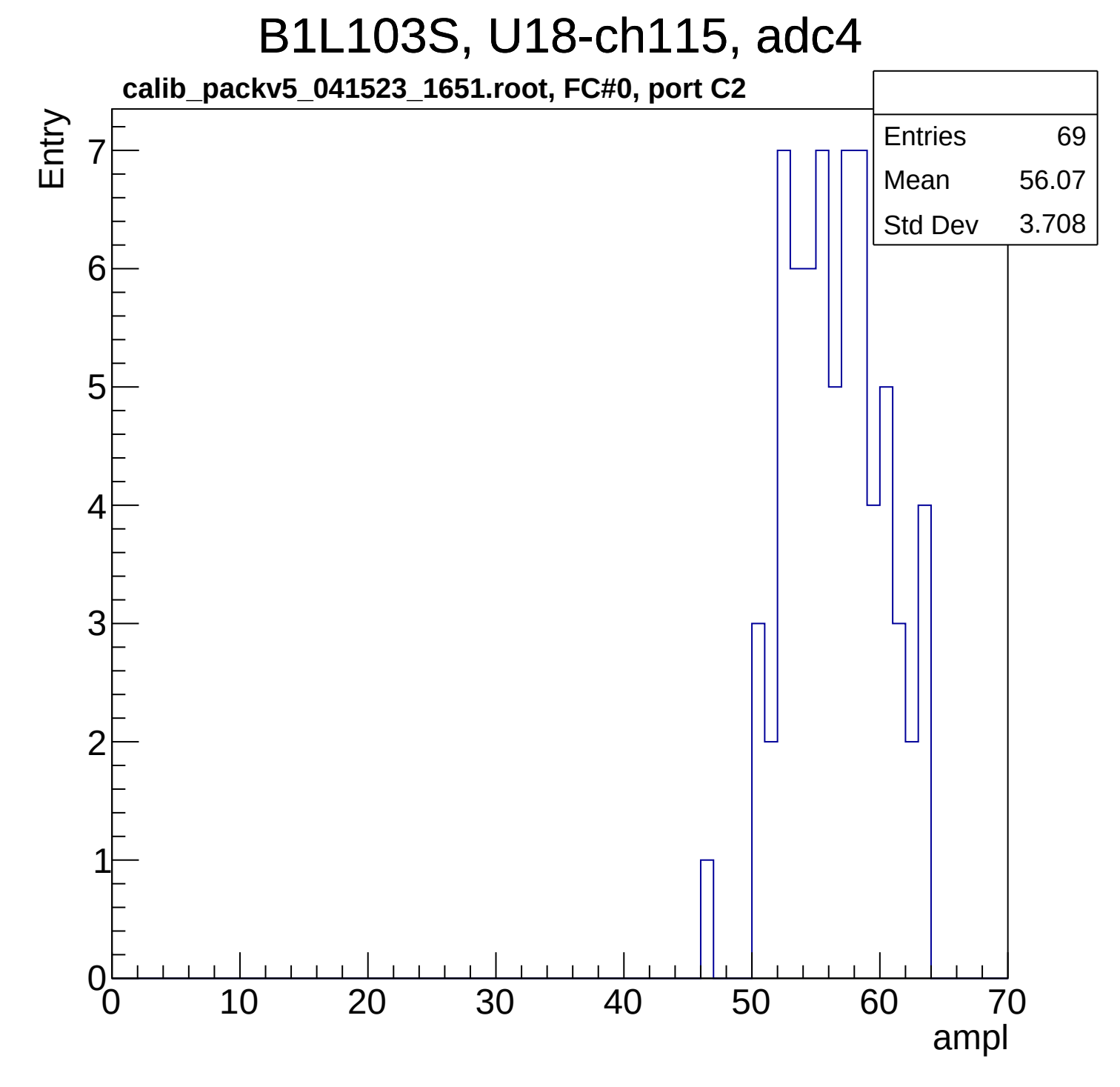
B1L103S, U18-ch115, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 56.07
Std Dev 3.708
Entry
ampl
0
1
2
3
4
5
6
7
0
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60
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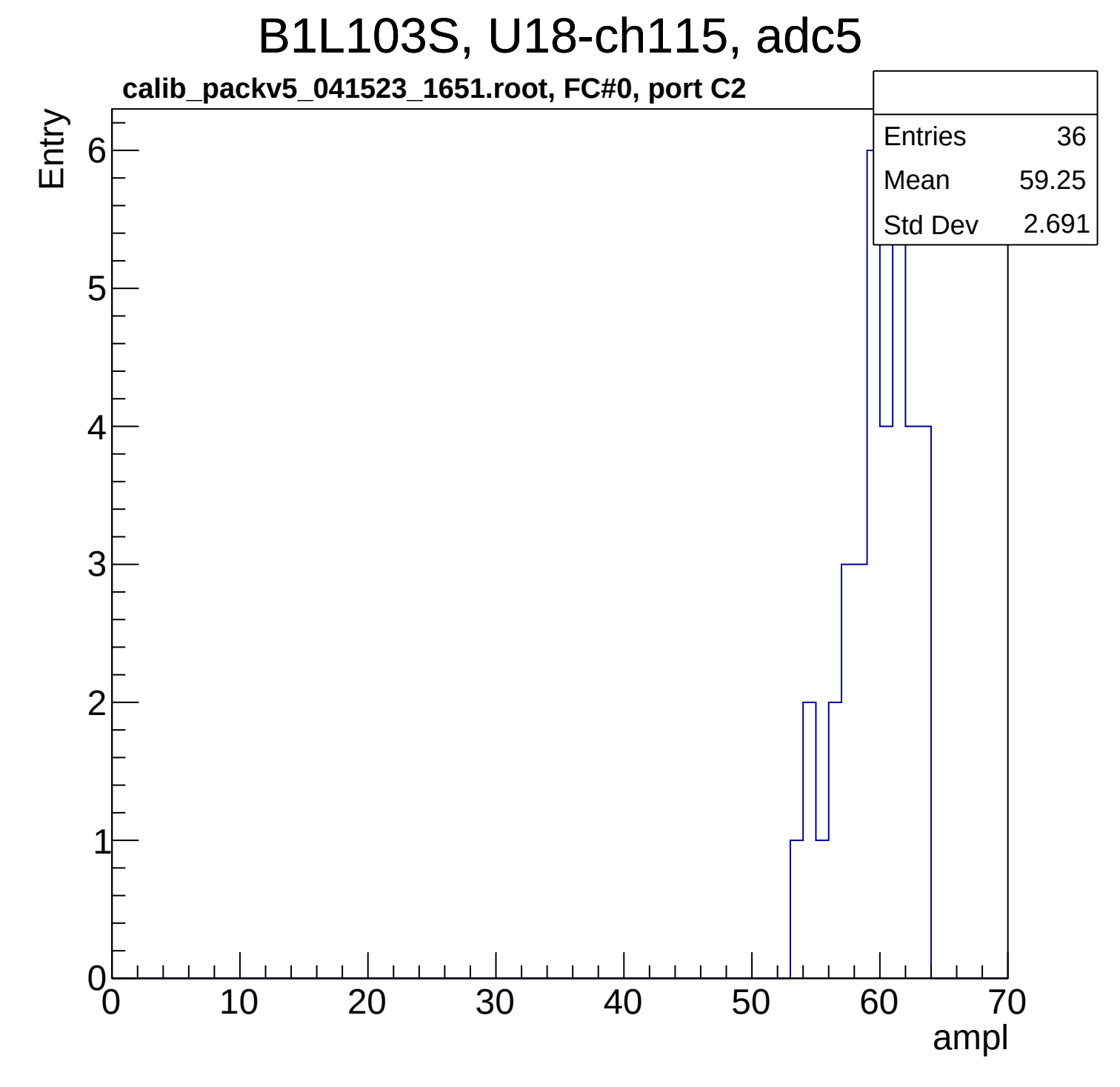
B1L103S, U18-ch115, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 36
Mean 59.25
Std Dev 2.691
Entry
ampl
0
1
2
3
4
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0
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60
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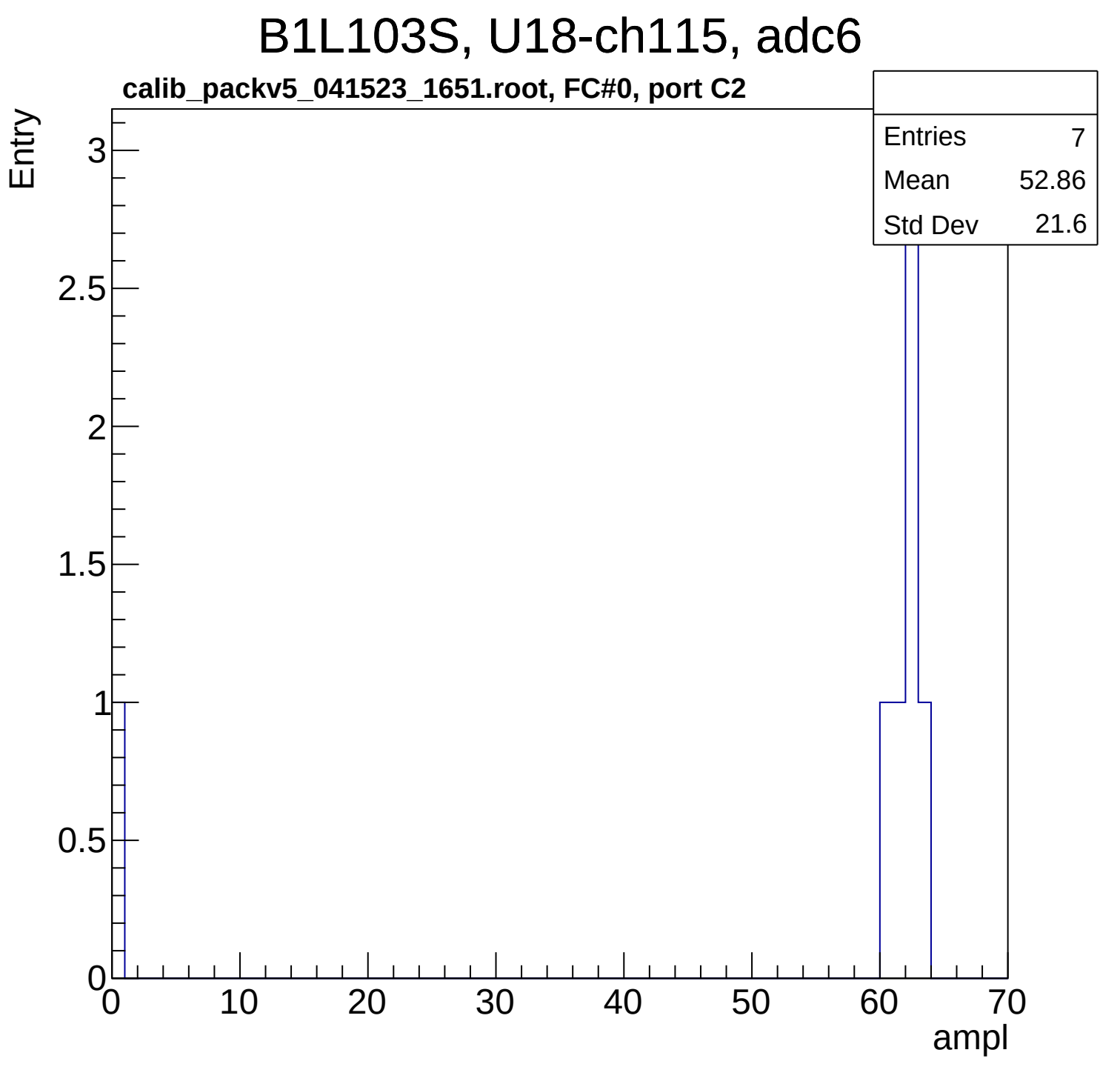
B1L103S, U18-ch115, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 52.86
Std Dev 21.6
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
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20
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40
50
60
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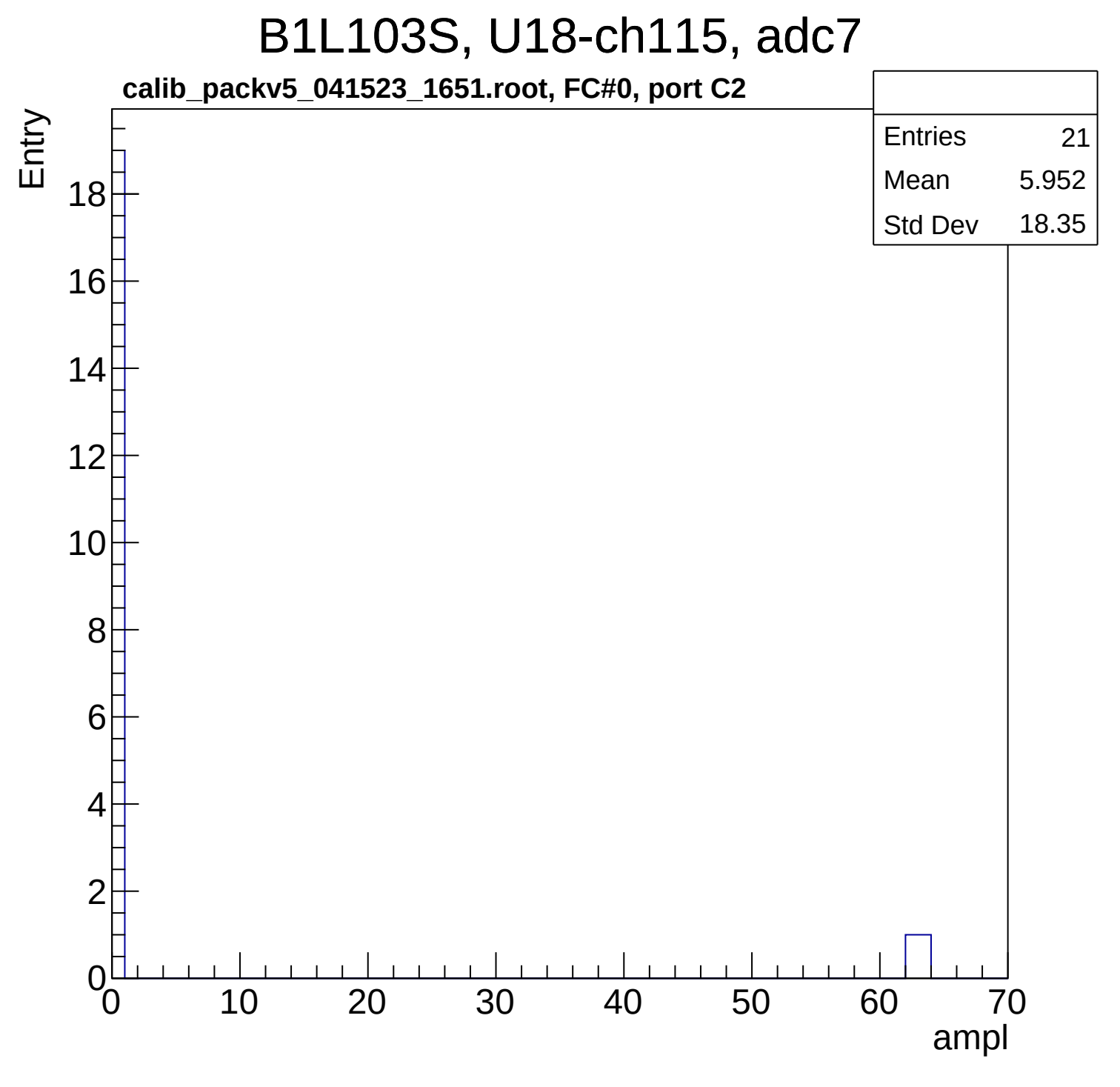
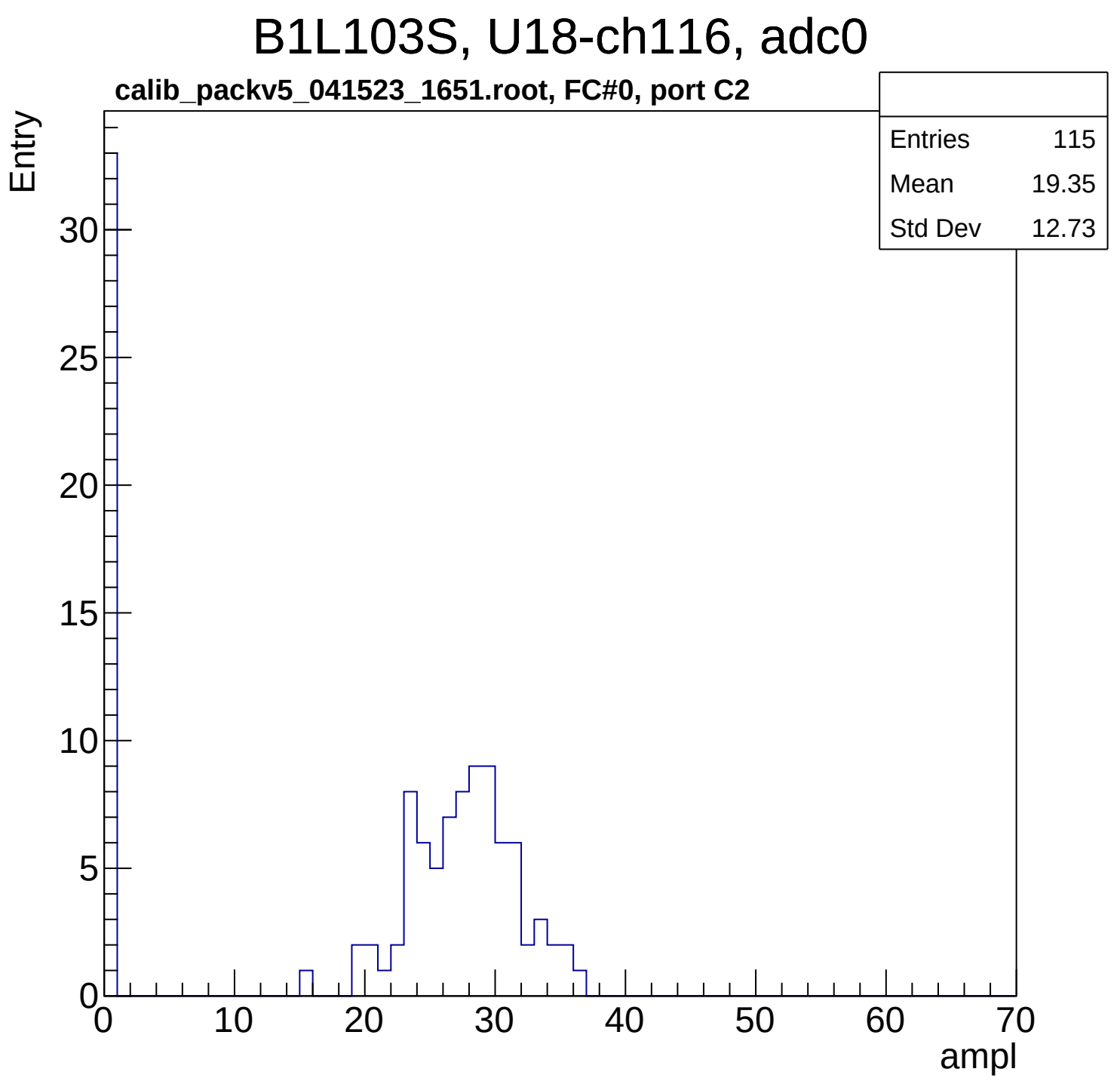
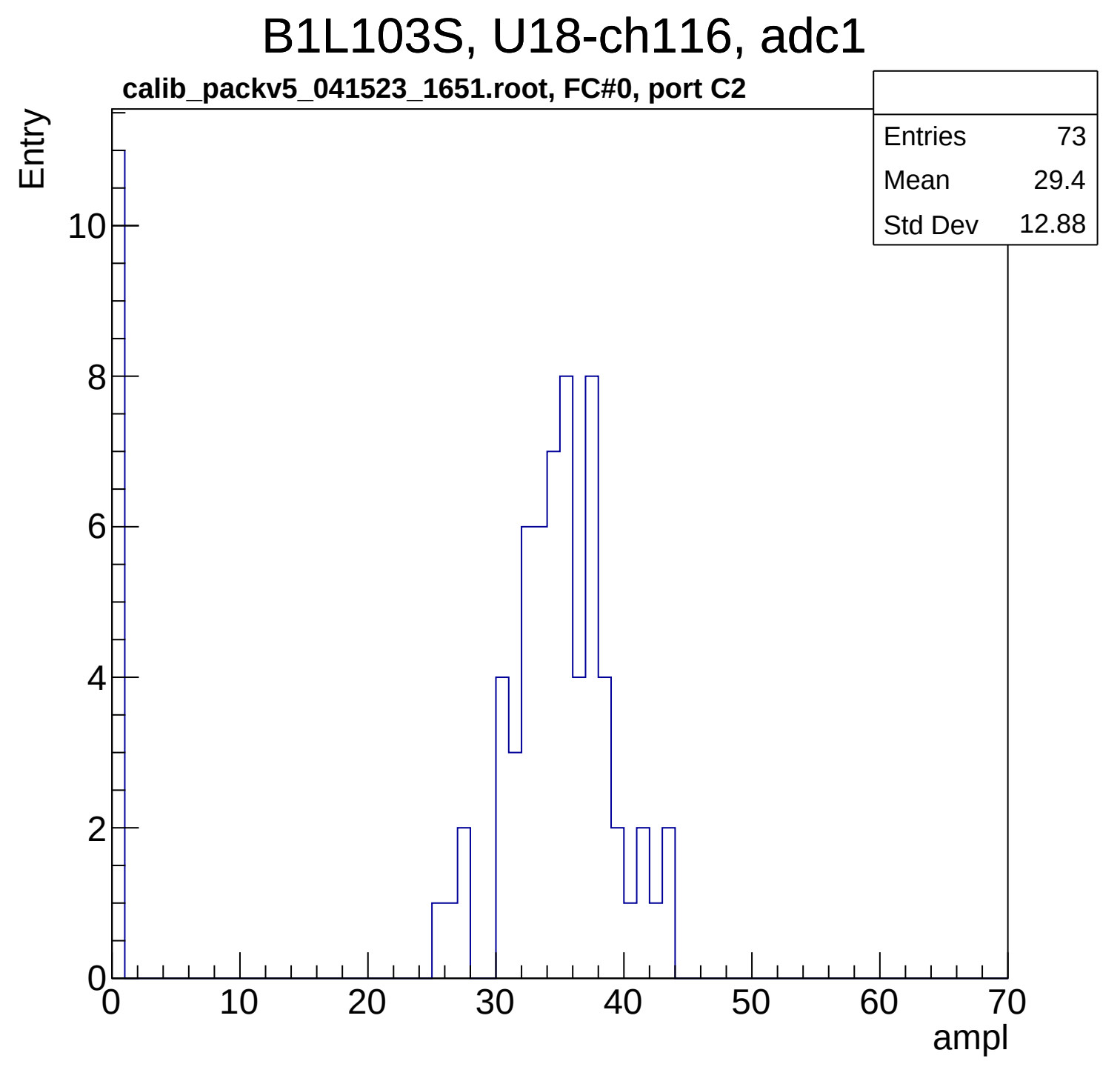
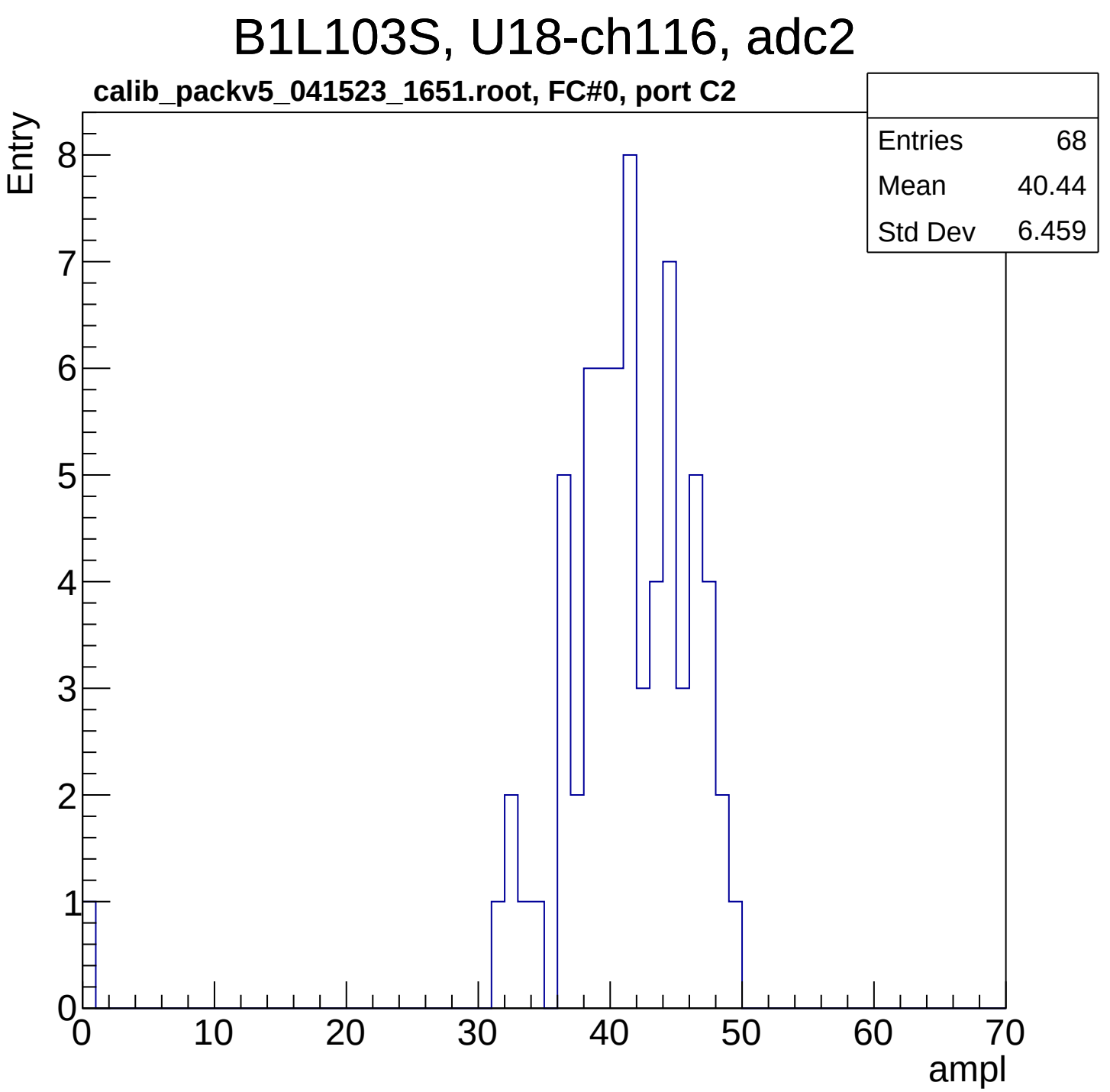

B1L103S, U18-ch115, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 5.952
Std Dev 18.35
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch116, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 115
Mean 19.35
Std Dev 12.73
Entry
0
5
10
15
20
25
30
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch116, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 29.4
Std Dev 12.88
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch116, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 40.44
Std Dev 6.459
Entry
ampl
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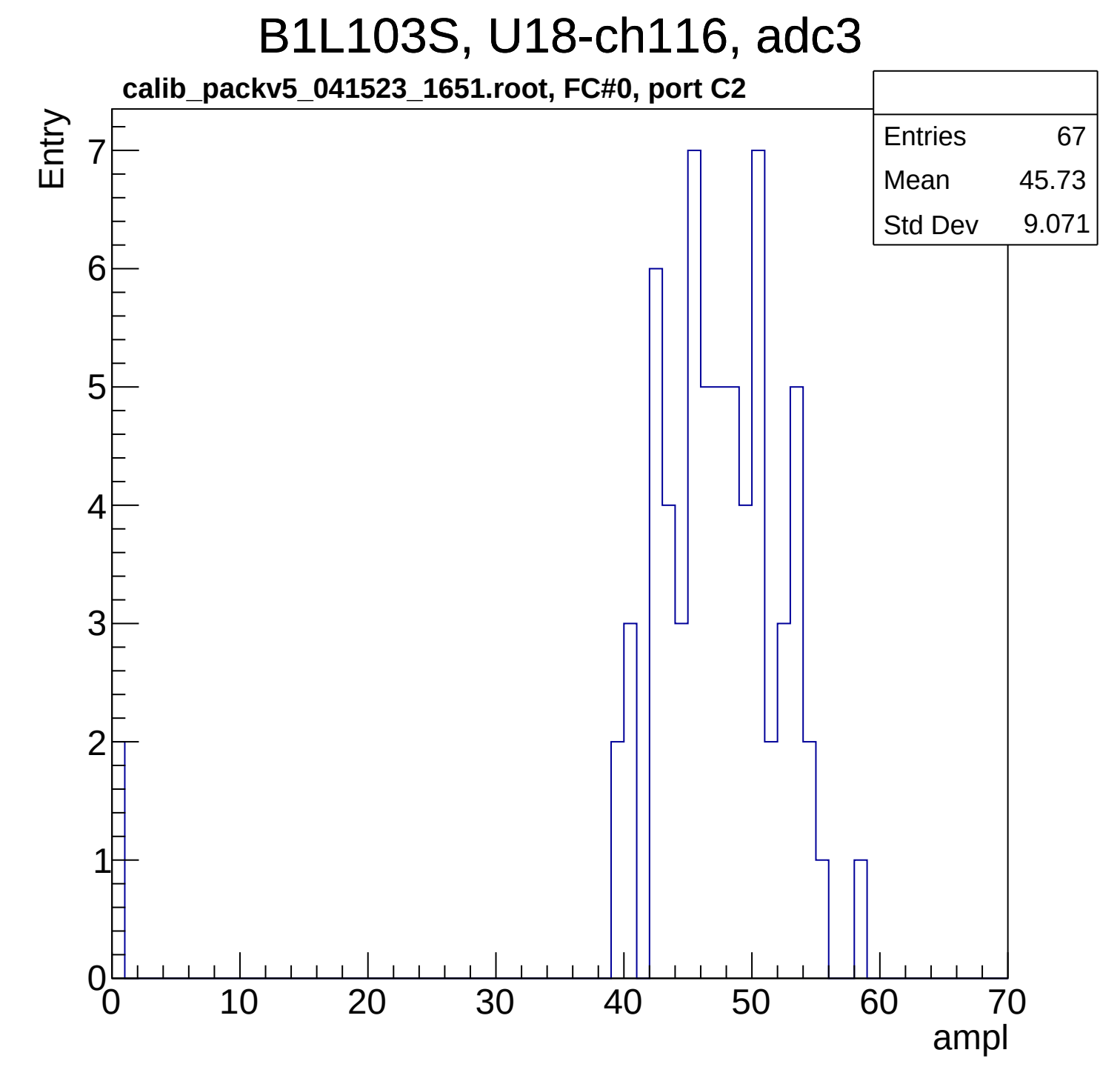
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch116, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 45.73
Std Dev 9.071
Entry
ampl
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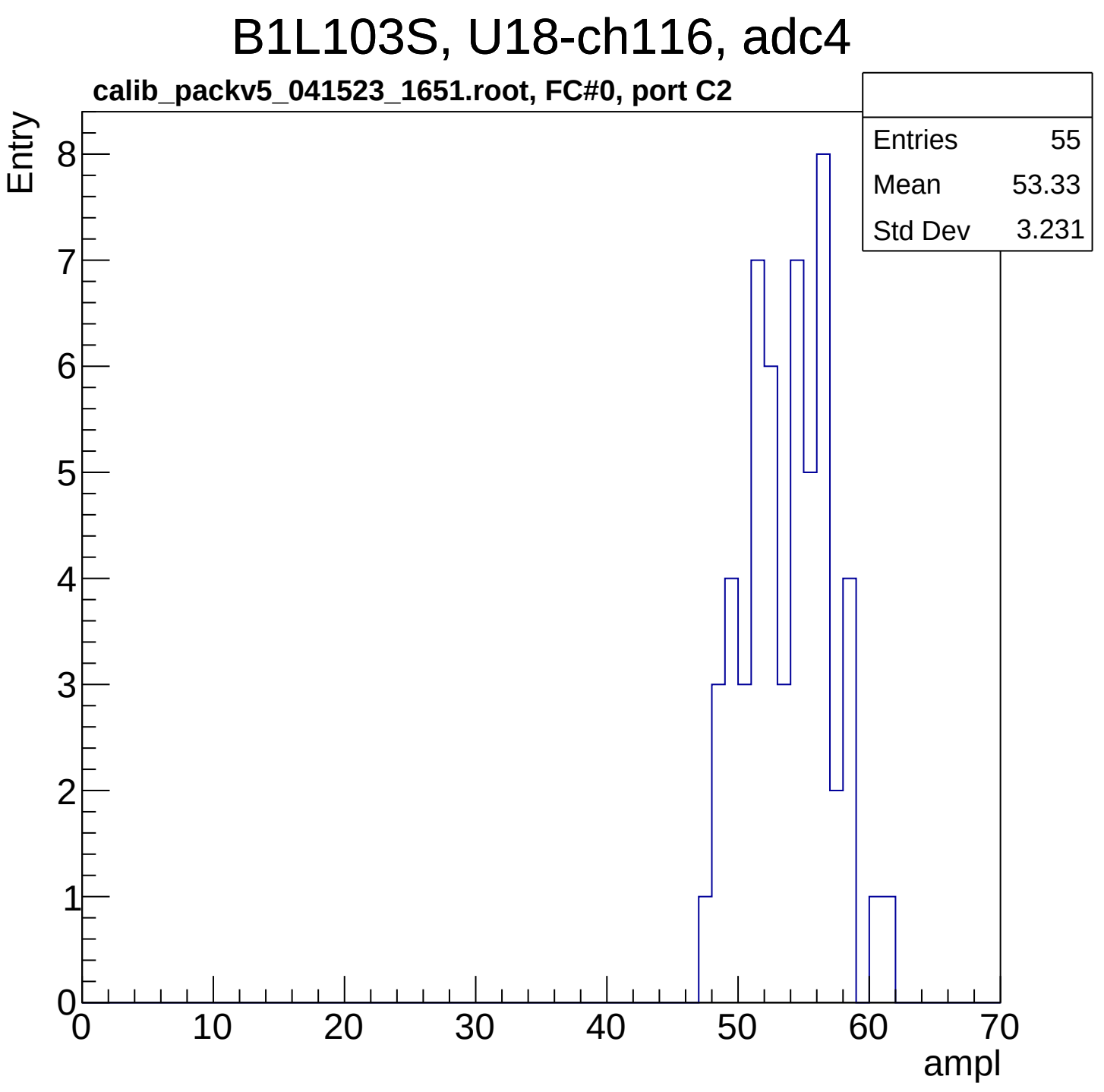
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U18-ch116, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 53.33
Std Dev 3.231
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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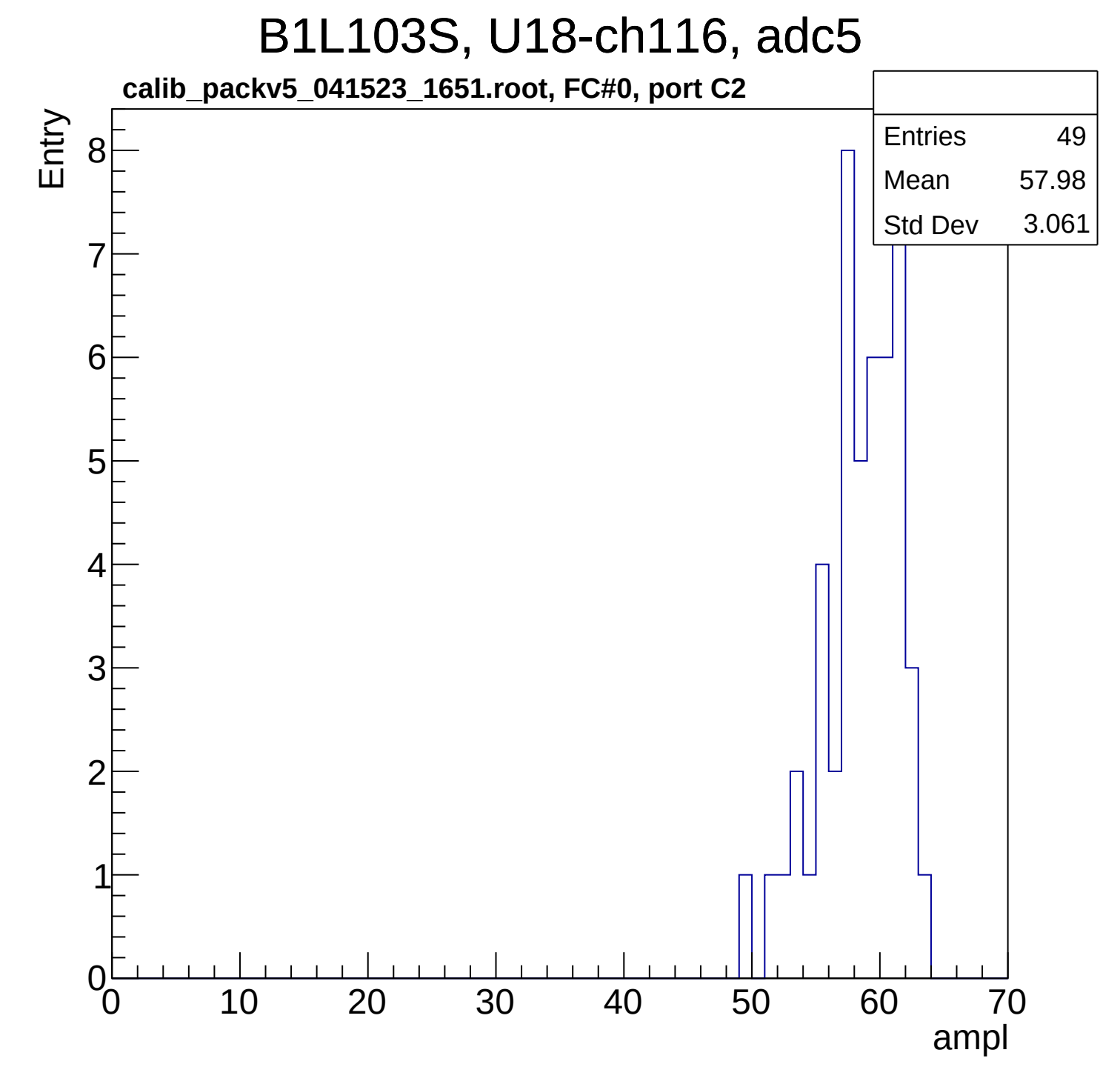
B1L103S, U18-ch116, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 57.98
Std Dev 3.061
Entry
ampl
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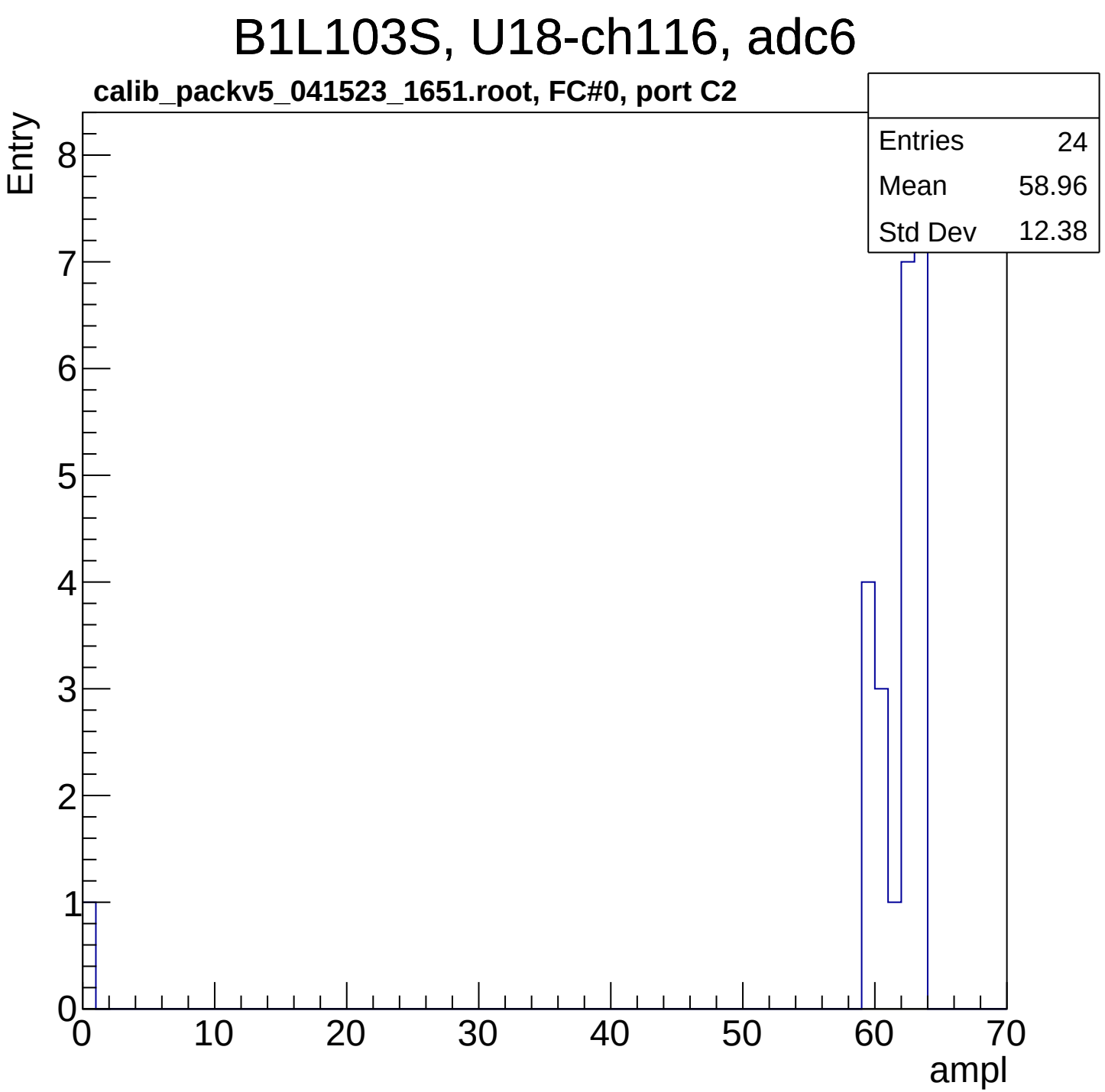
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch116, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 24
Mean 58.96
Std Dev 12.38
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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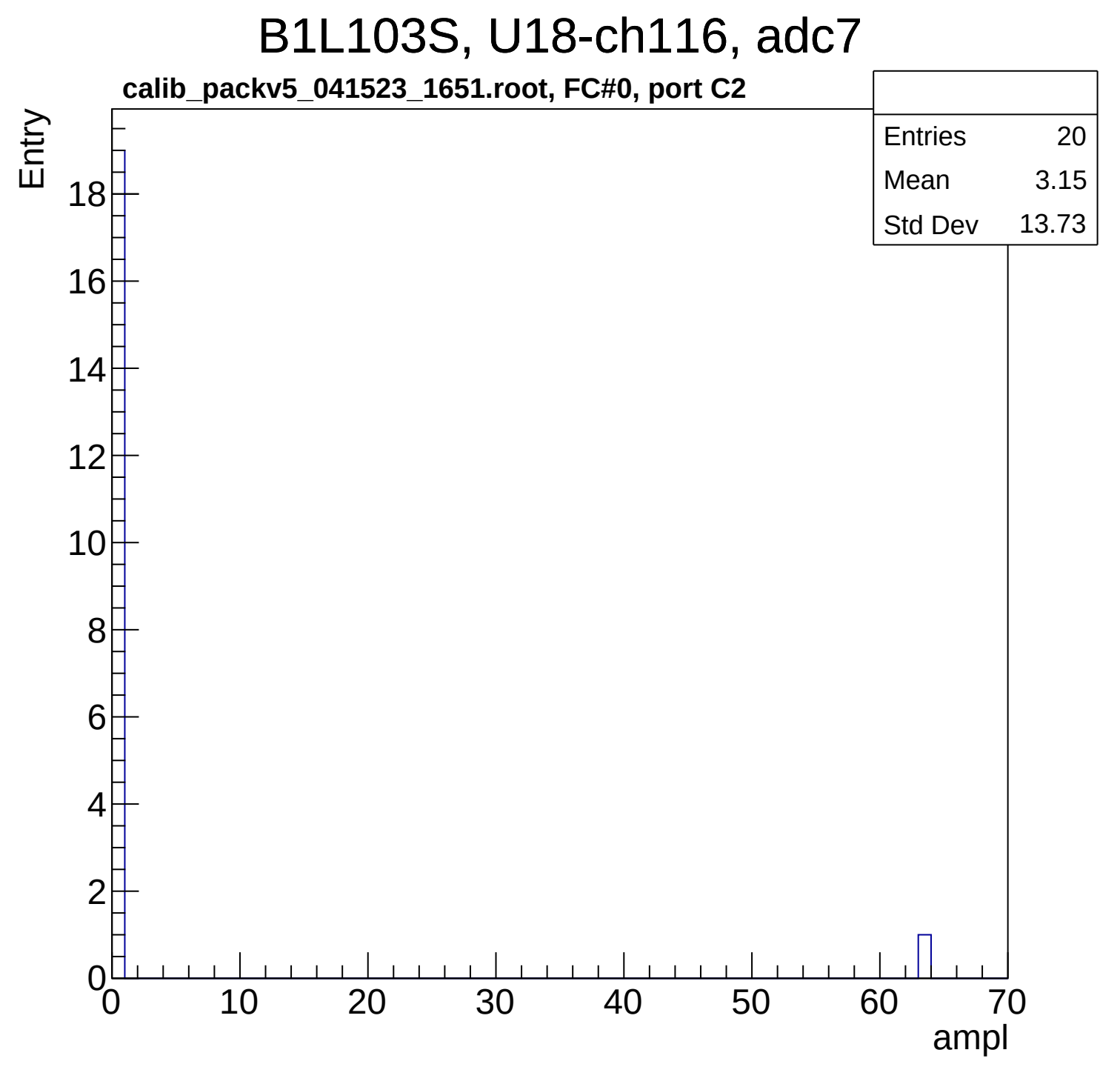
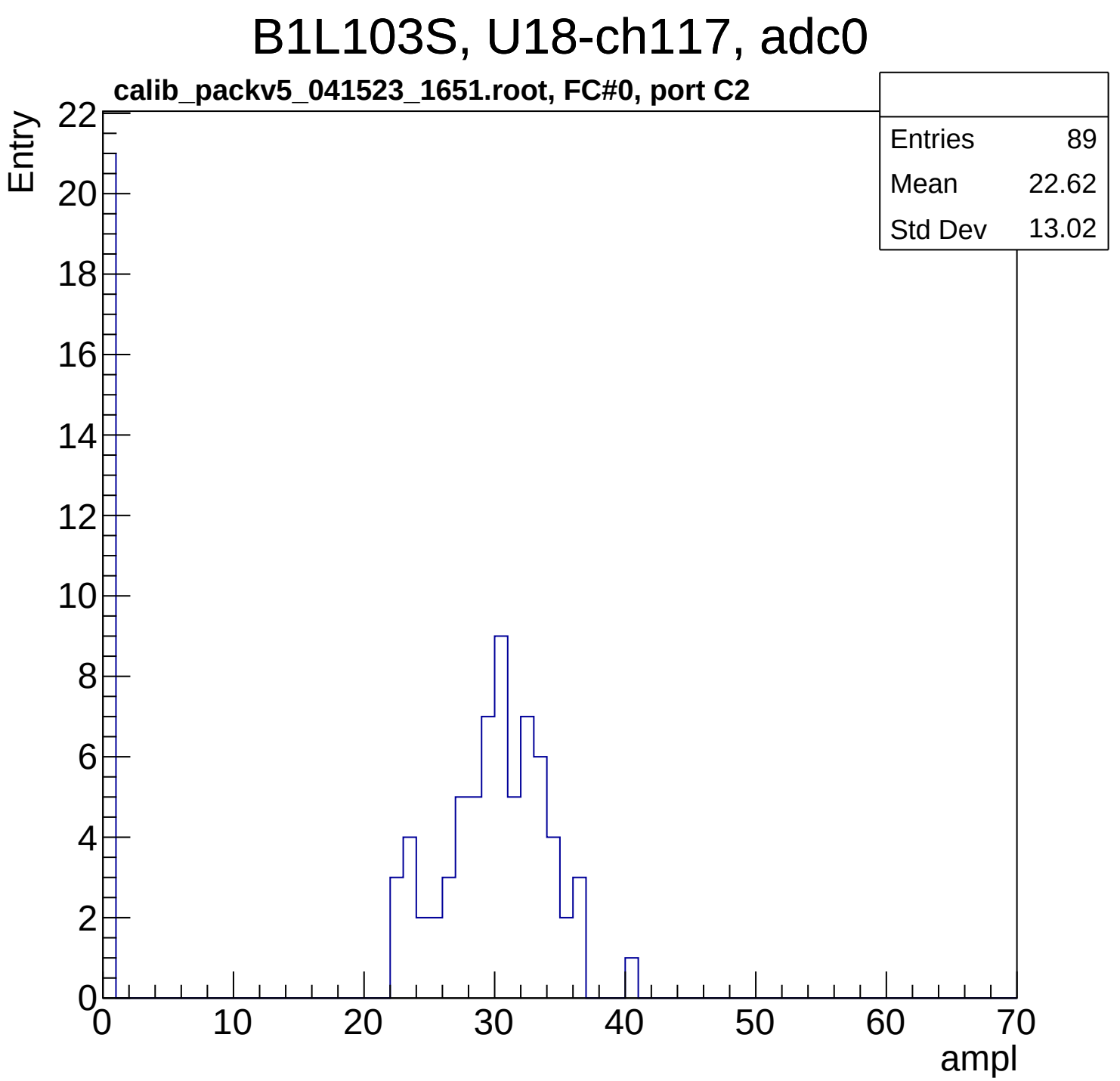

B1L103S, U18-ch116, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch117, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 89
Mean 22.62
Std Dev 13.02
Entry
ampl
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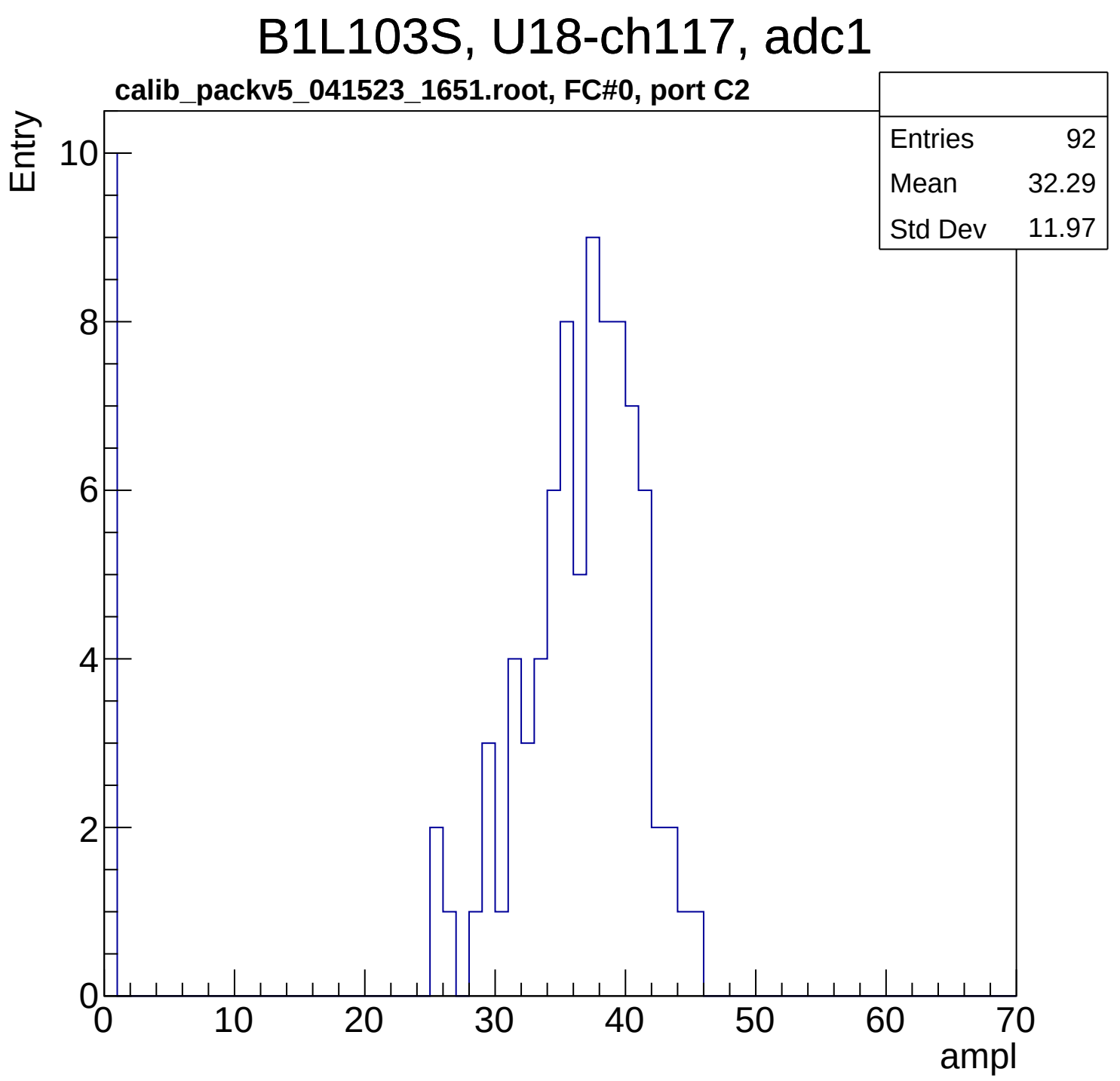
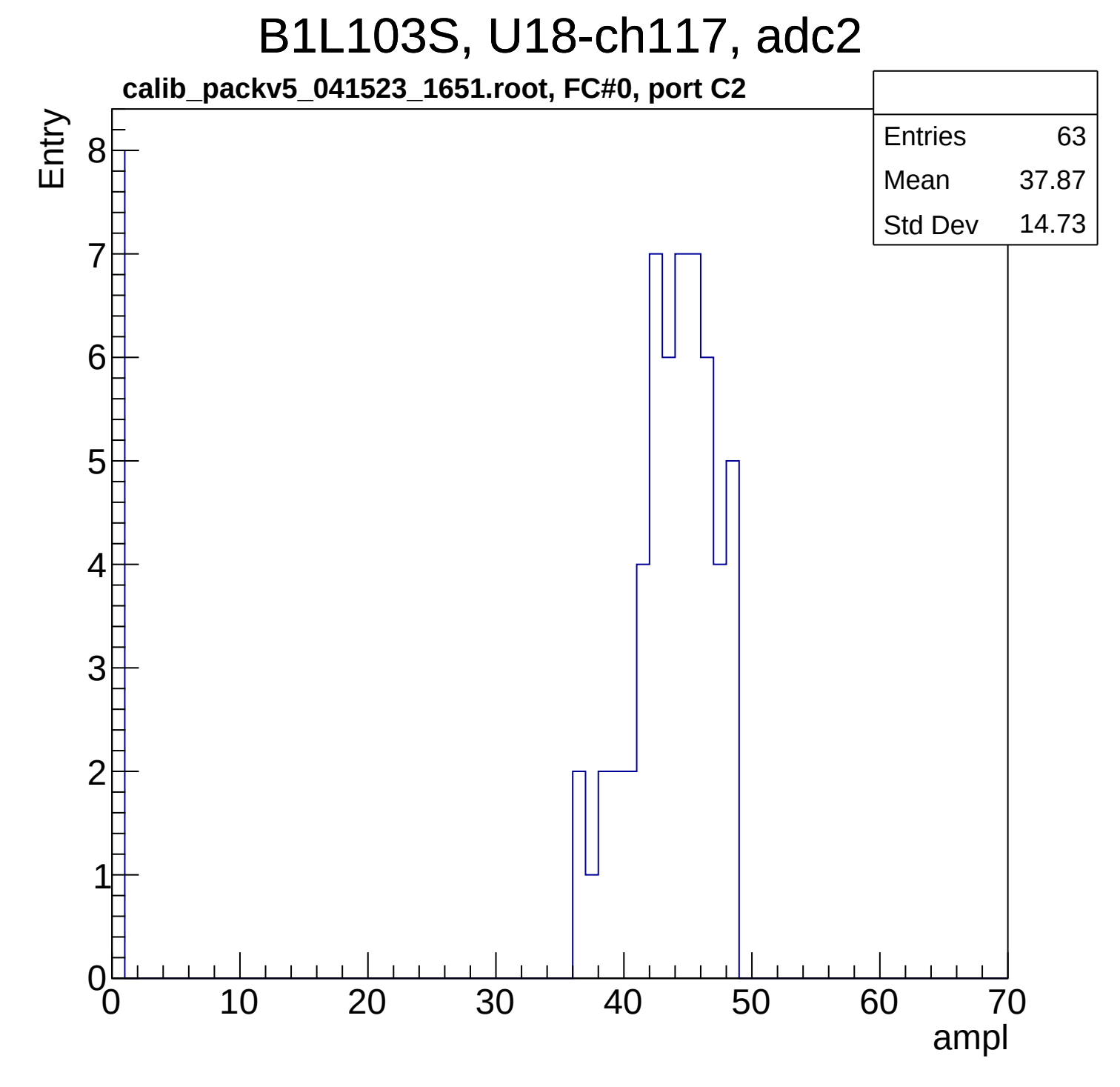
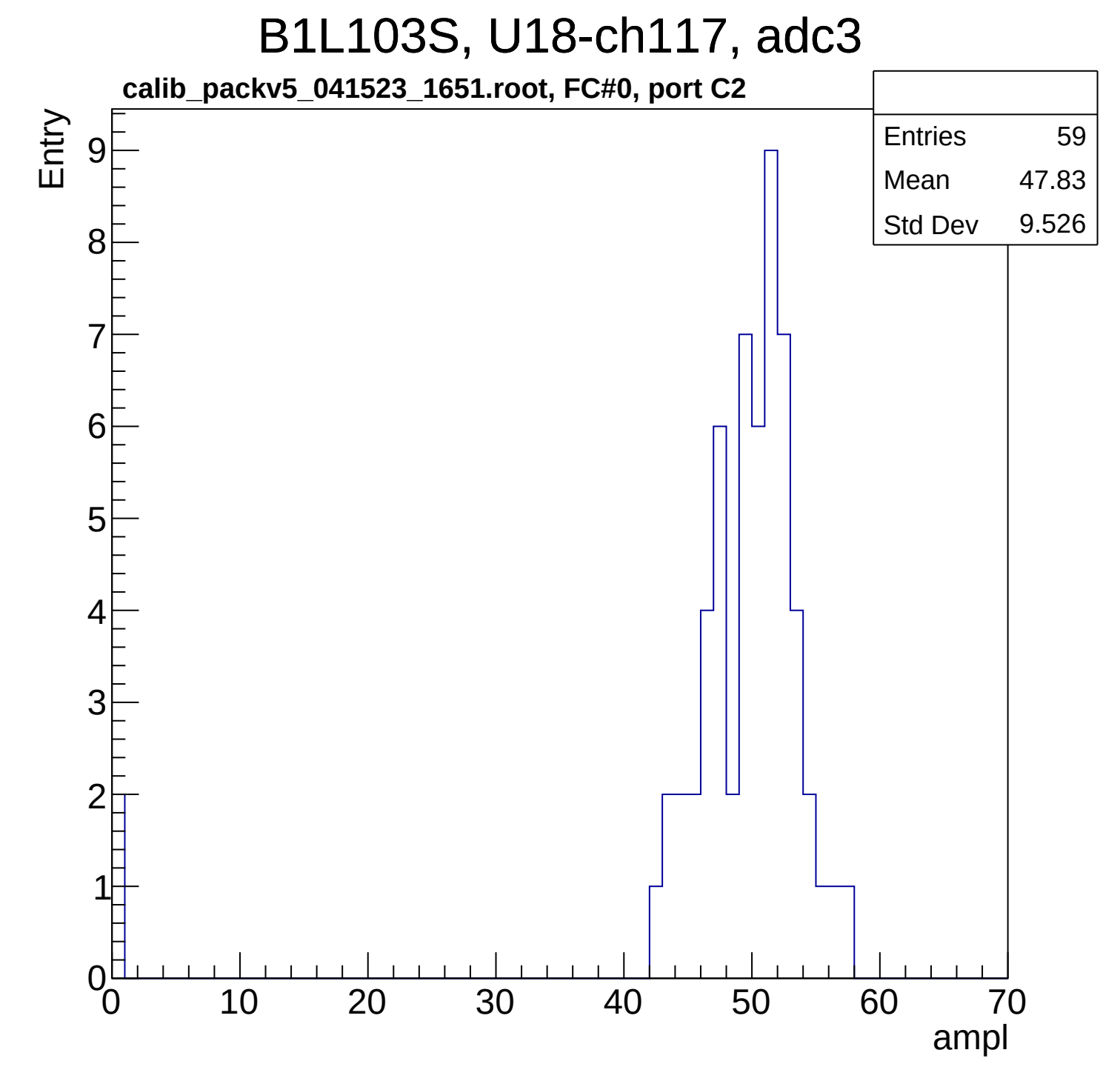
2
4
6
8
10
12
14
16
18
20
22
0
10
20
30
40
50
60
70


B1L103S, U18-ch117, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 92
Mean 32.29
Std Dev 11.97
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U18-ch117, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 37.87
Std Dev 14.73
Entry
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch117, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 47.83
Std Dev 9.526
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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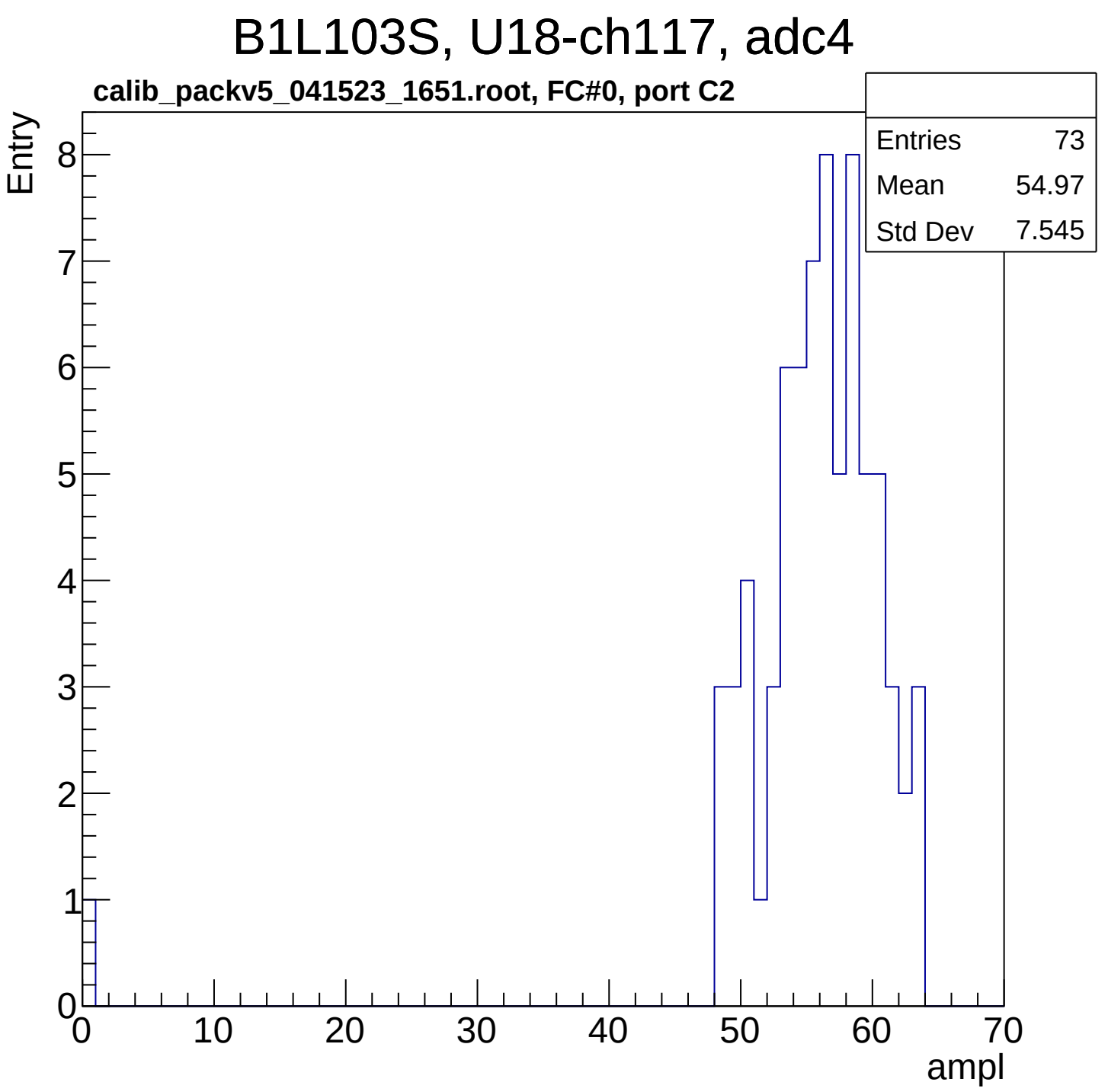
40
50
60
70


B1L103S, U18-ch117, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 54.97
Std Dev 7.545
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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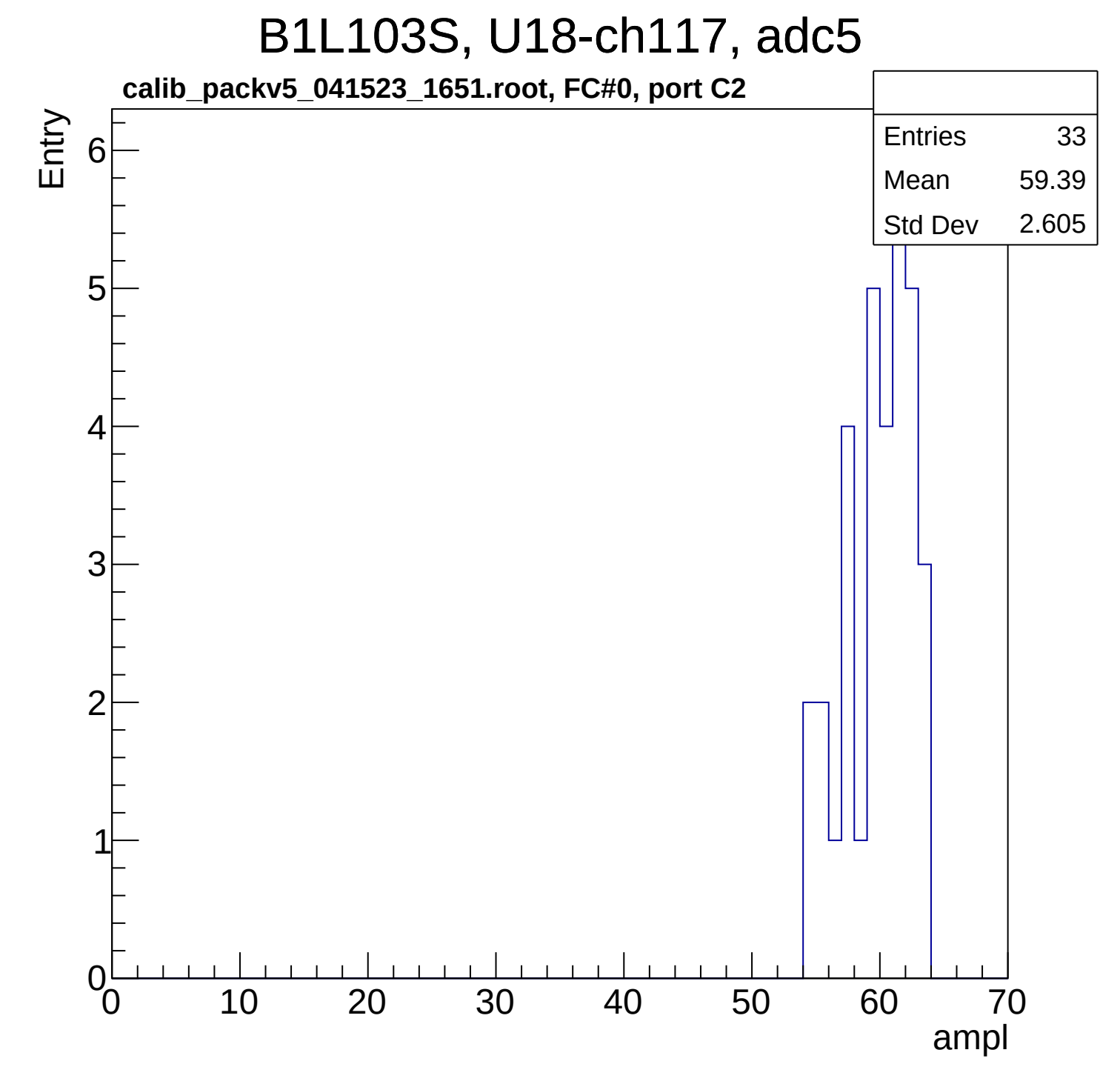
40
50
60
70


B1L103S, U18-ch117, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 33
Mean 59.39
Std Dev 2.605
Entry
ampl
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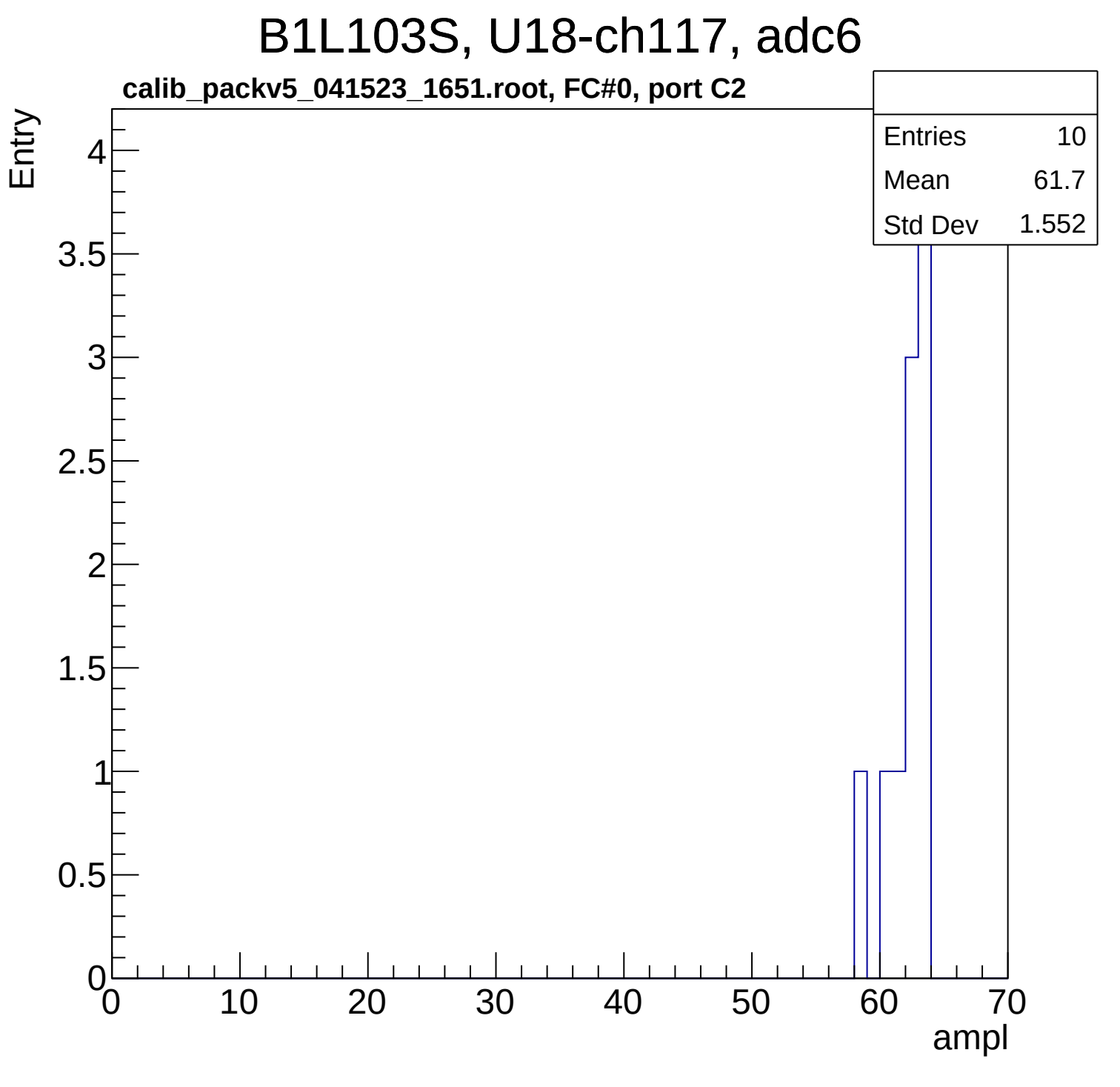
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U18-ch117, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 61.7
Std Dev 1.552
Entry
ampl
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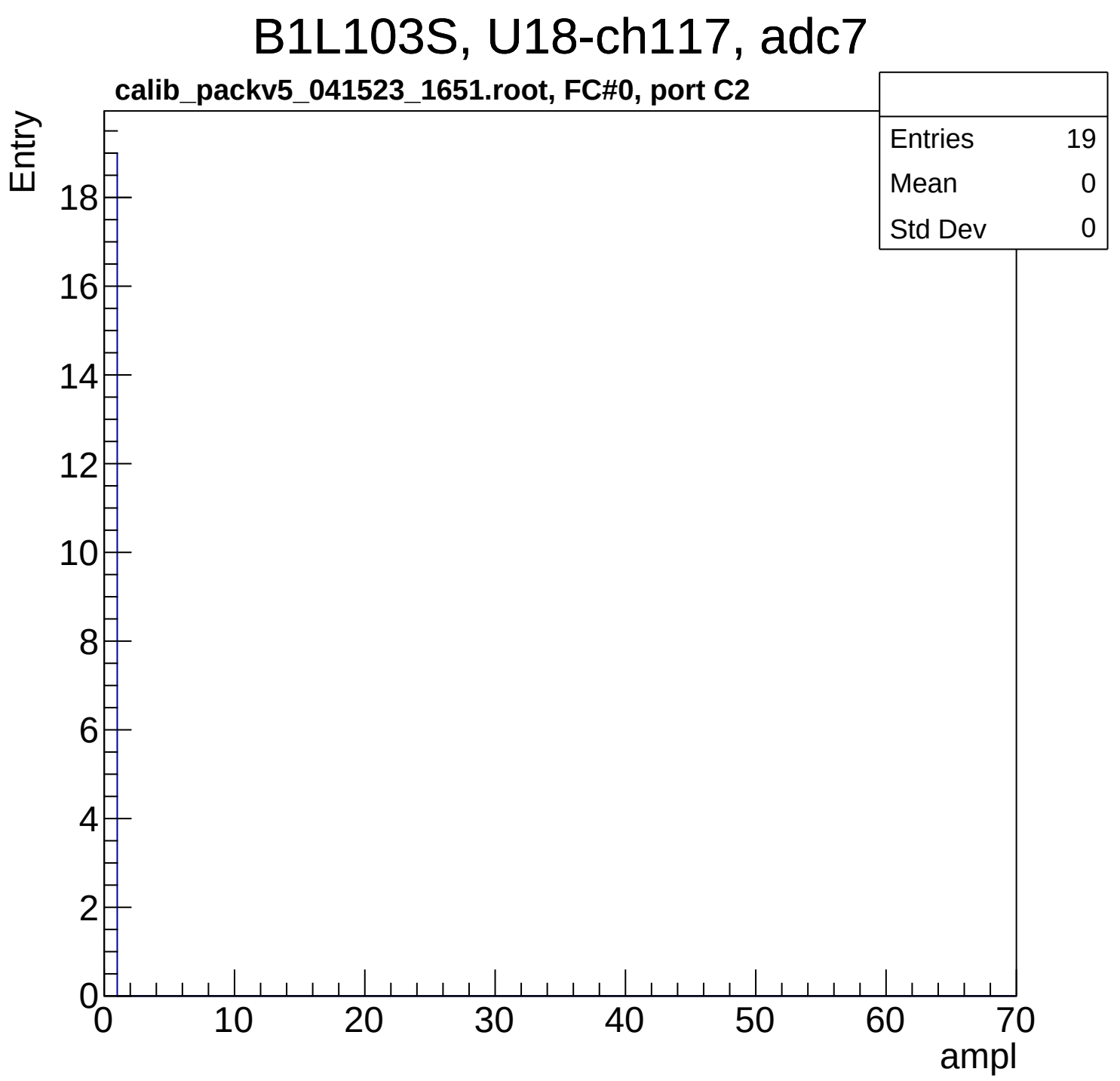
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U18-ch117, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
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2
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6
8
10
12
14
16
18
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10
20
30
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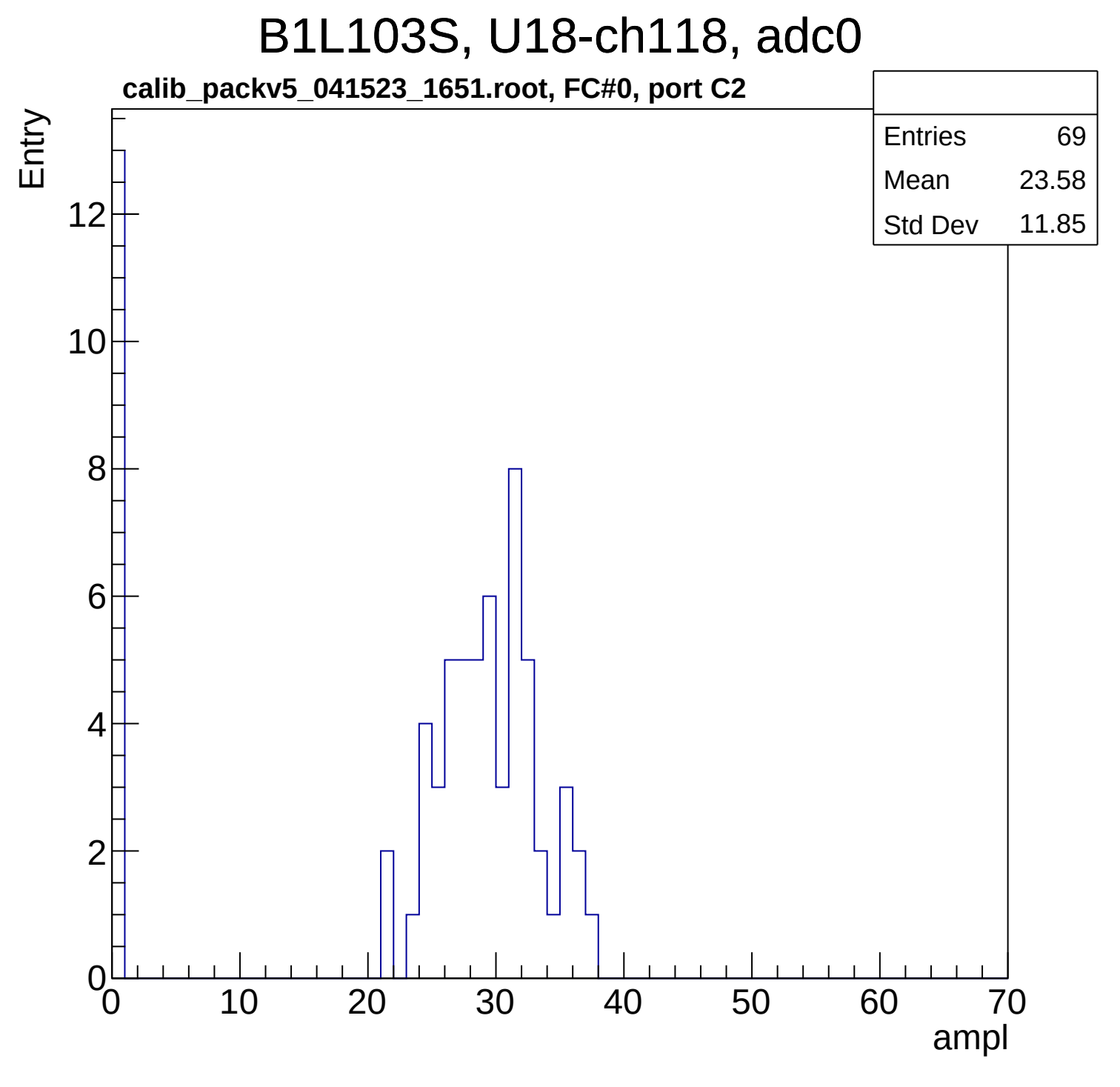
50
60
70
ampl


B1L103S, U18-ch118, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 23.58
Std Dev 11.85
Entry
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4
6
8
10
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10
20
30
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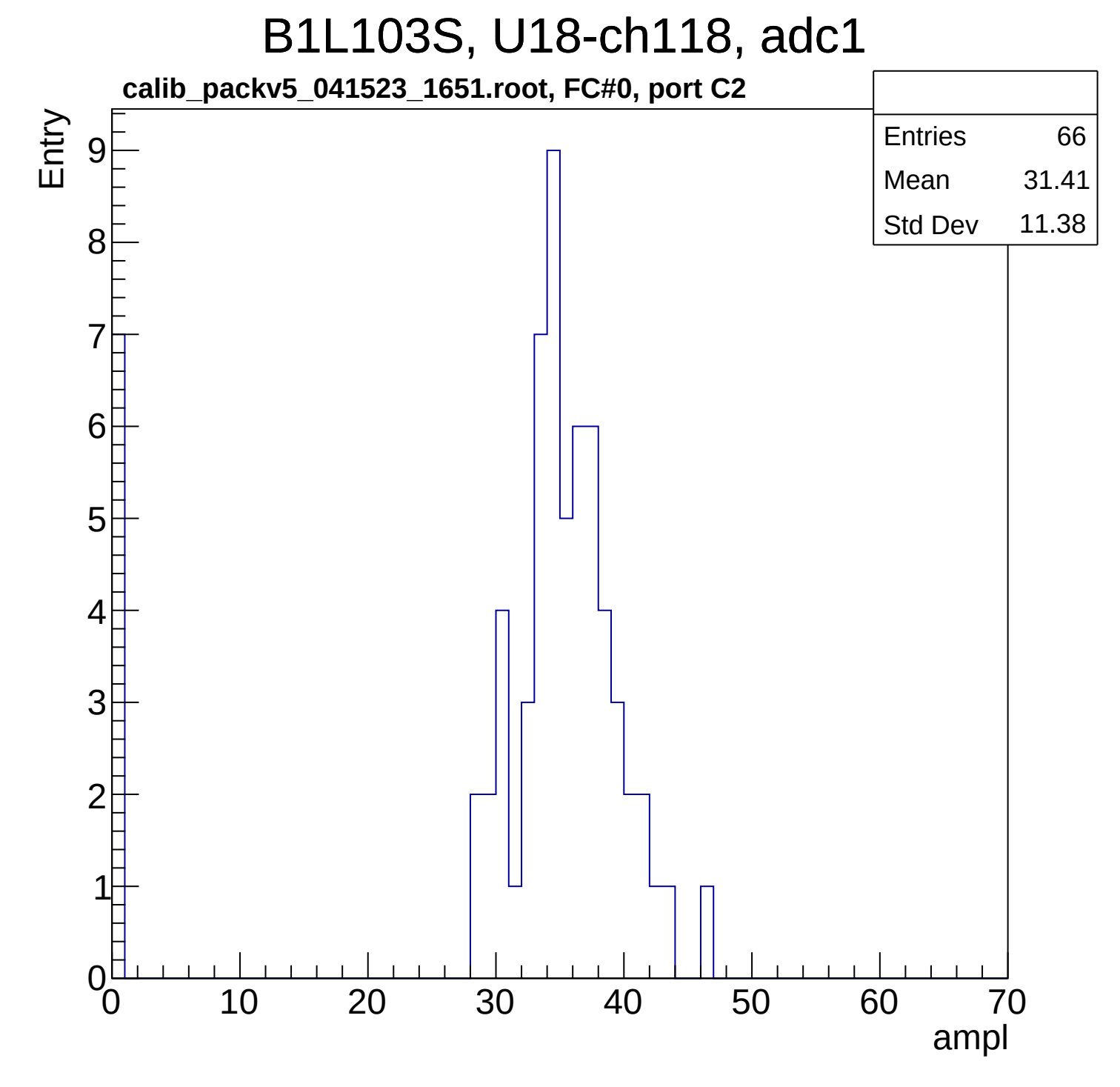
50
60
70
ampl


B1L103S, U18-ch118, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 31.41
Std Dev 11.38
Entry
ampl
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2
3
4
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6
7
8
9
0
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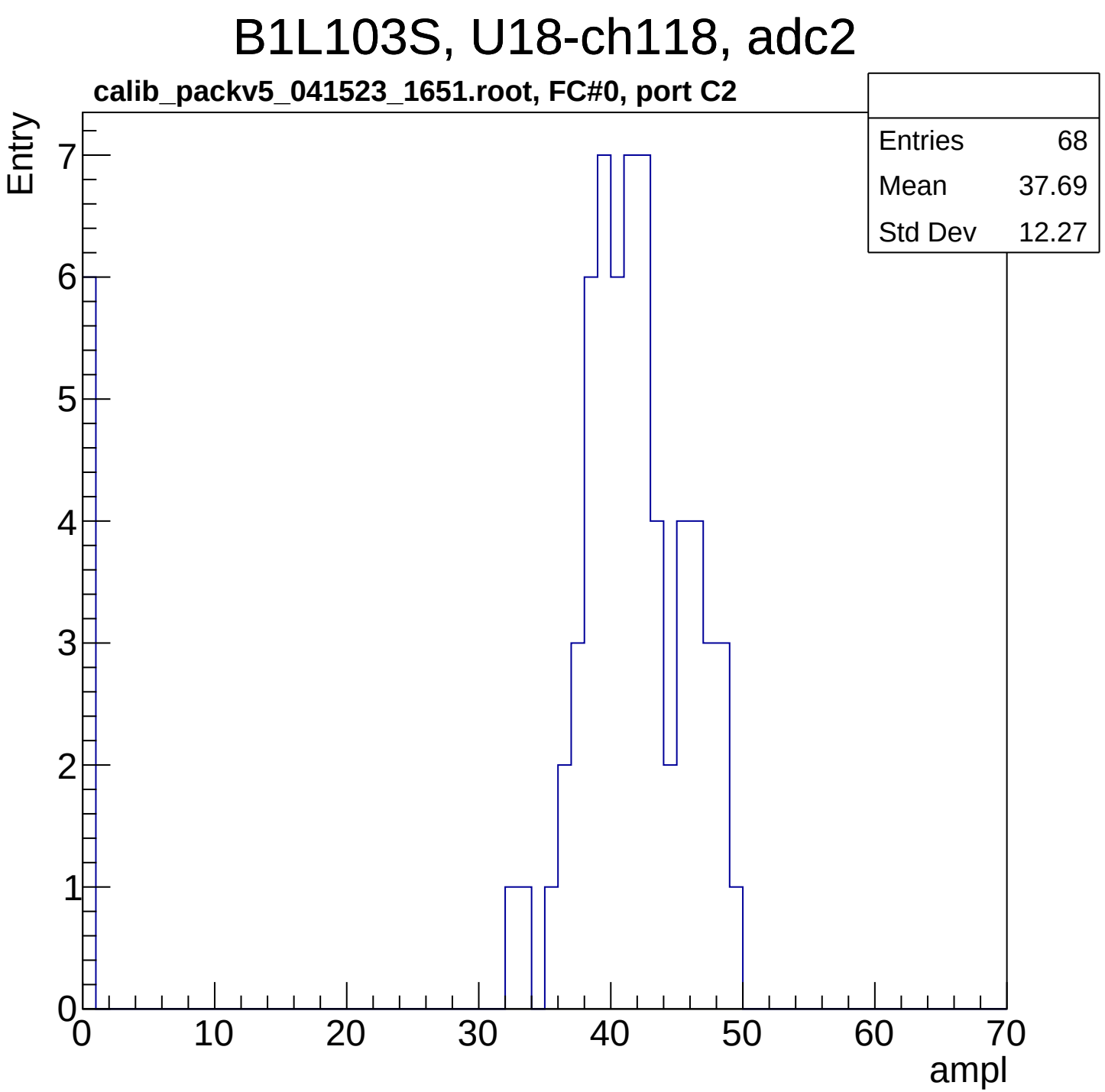
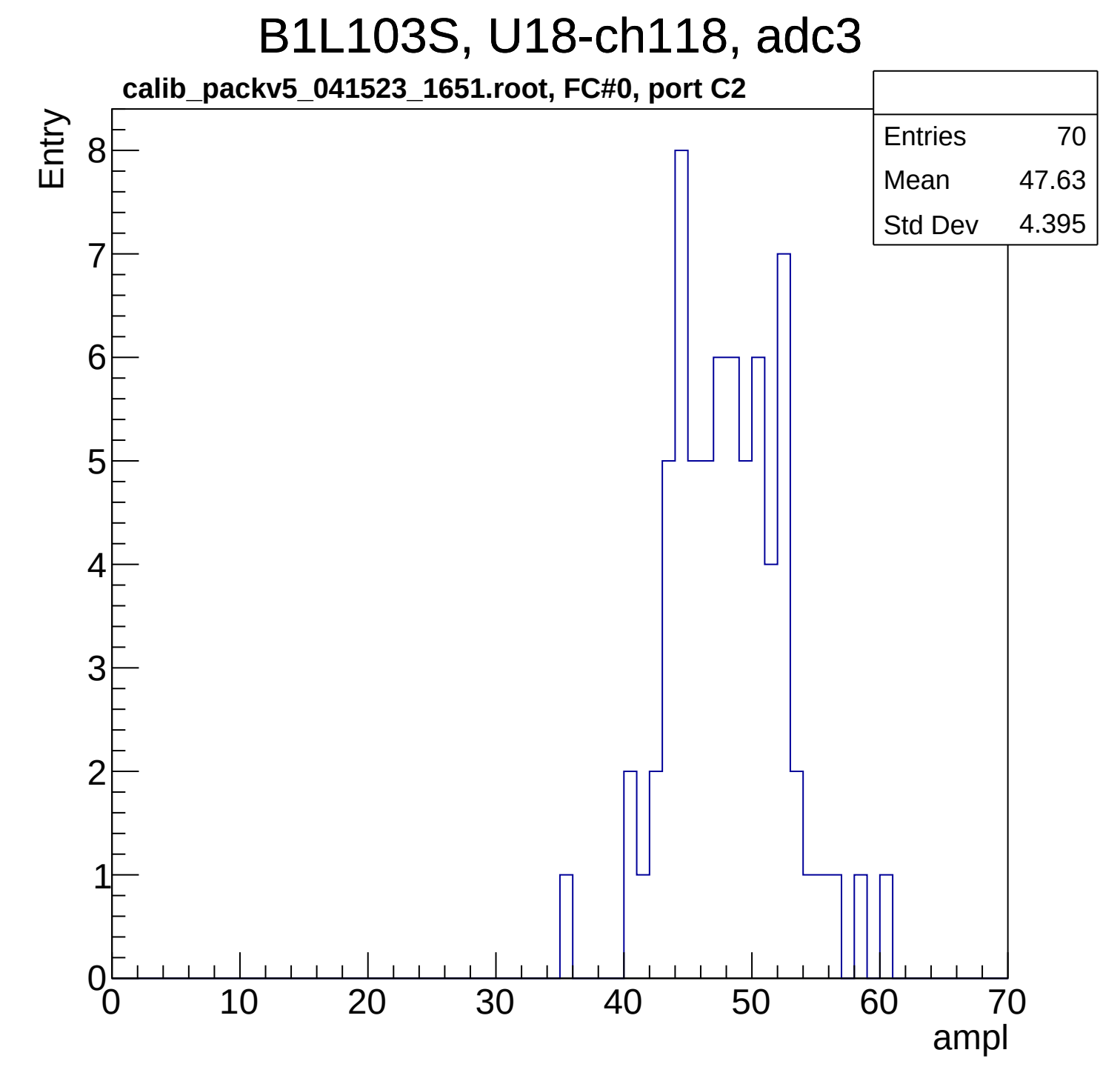
20
30
40
50
60
70


B1L103S, U18-ch118, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 37.69
Std Dev 12.27
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U18-ch118, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 47.63
Std Dev 4.395
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
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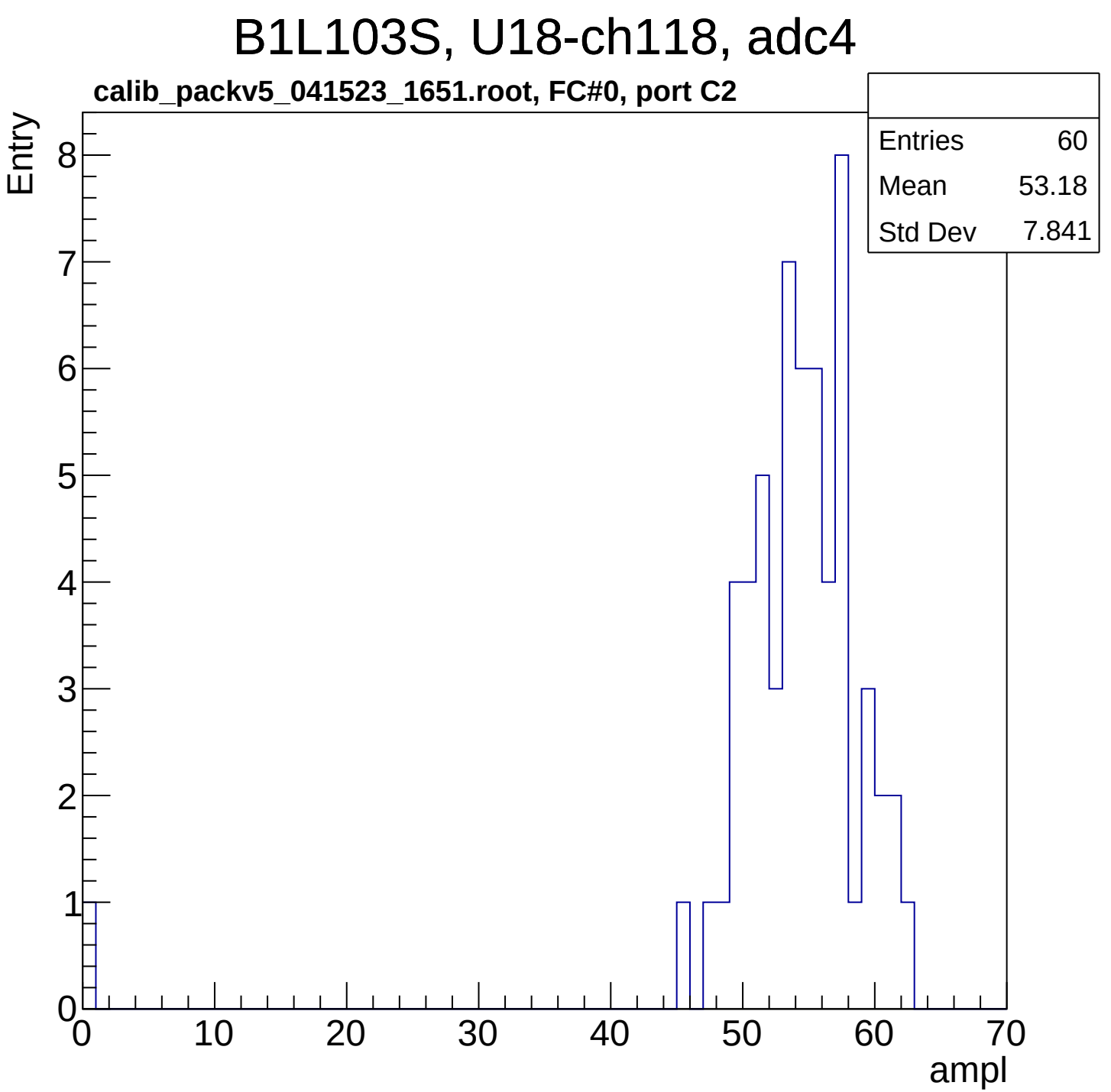
40
50
60
70


B1L103S, U18-ch118, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 53.18
Std Dev 7.841
Entry
ampl
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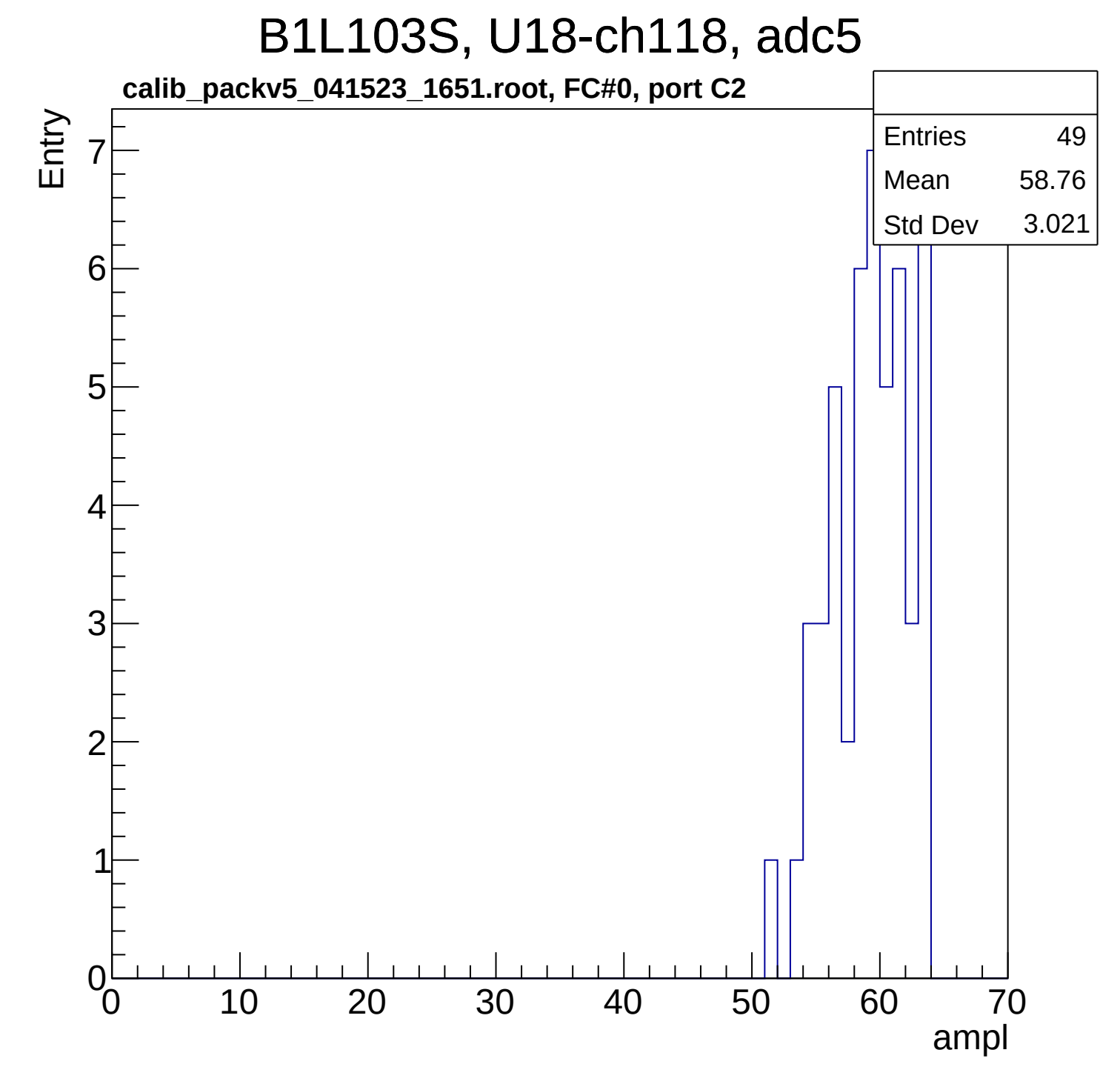
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch118, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 58.76
Std Dev 3.021
Entry
ampl
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2
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4
5
6
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0
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20
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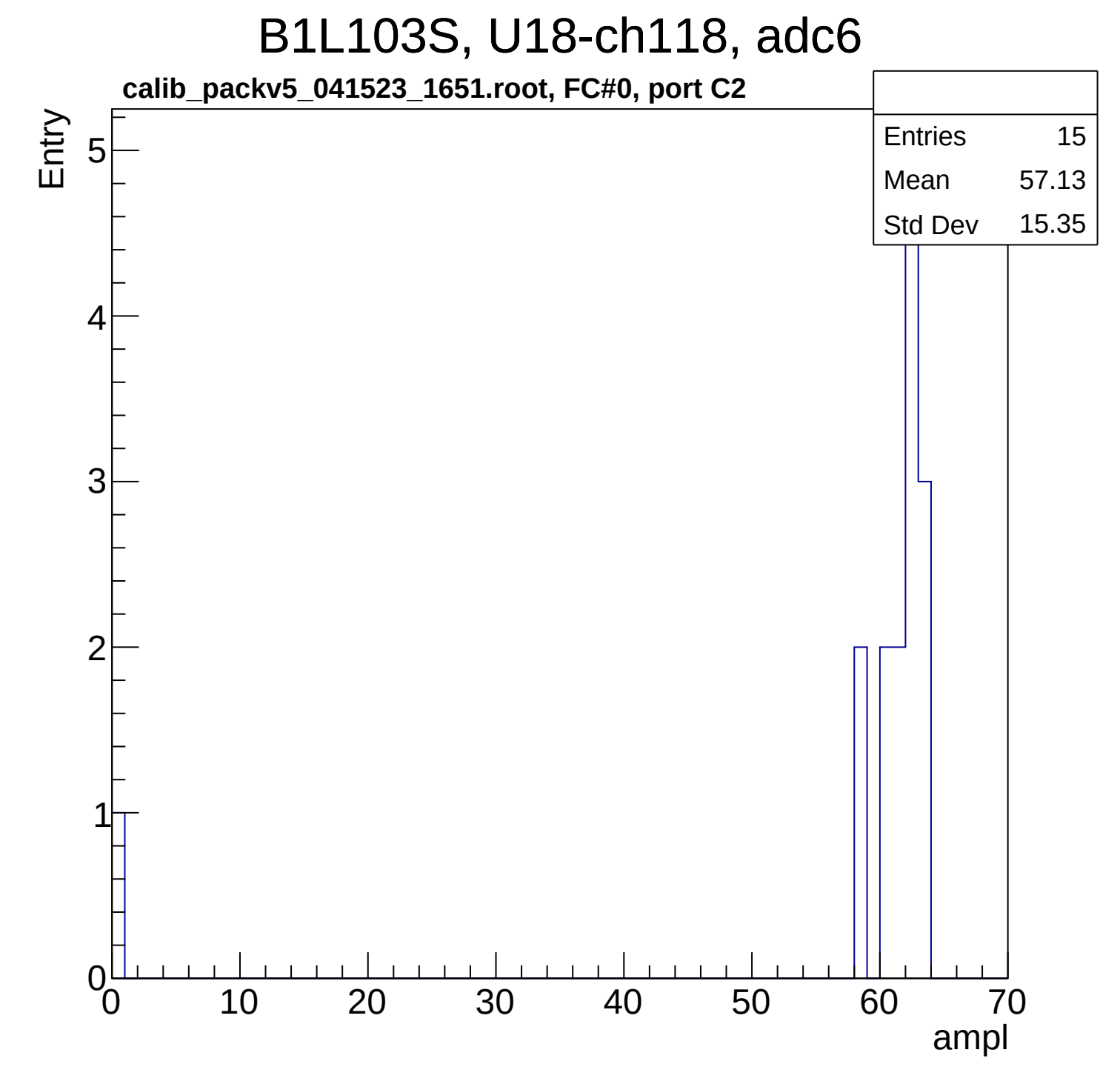
40
50
60
70


B1L103S, U18-ch118, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 15
Mean 57.13
Std Dev 15.35
Entry
ampl
0
1
2
3
4
5
0
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20
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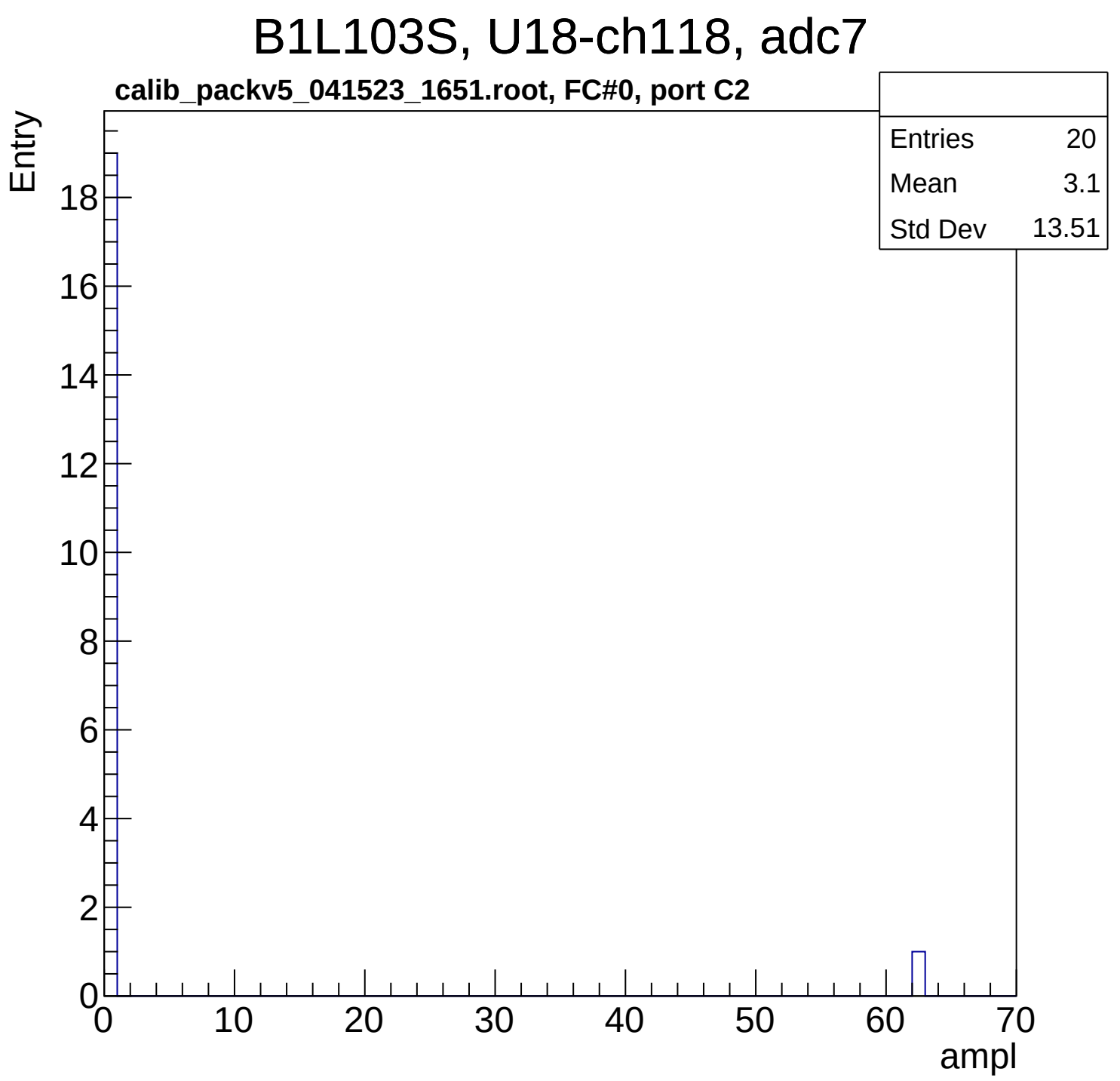
40
50
60
70


B1L103S, U18-ch118, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.1
Std Dev 13.51
Entry
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6
8
10
12
14
16
18
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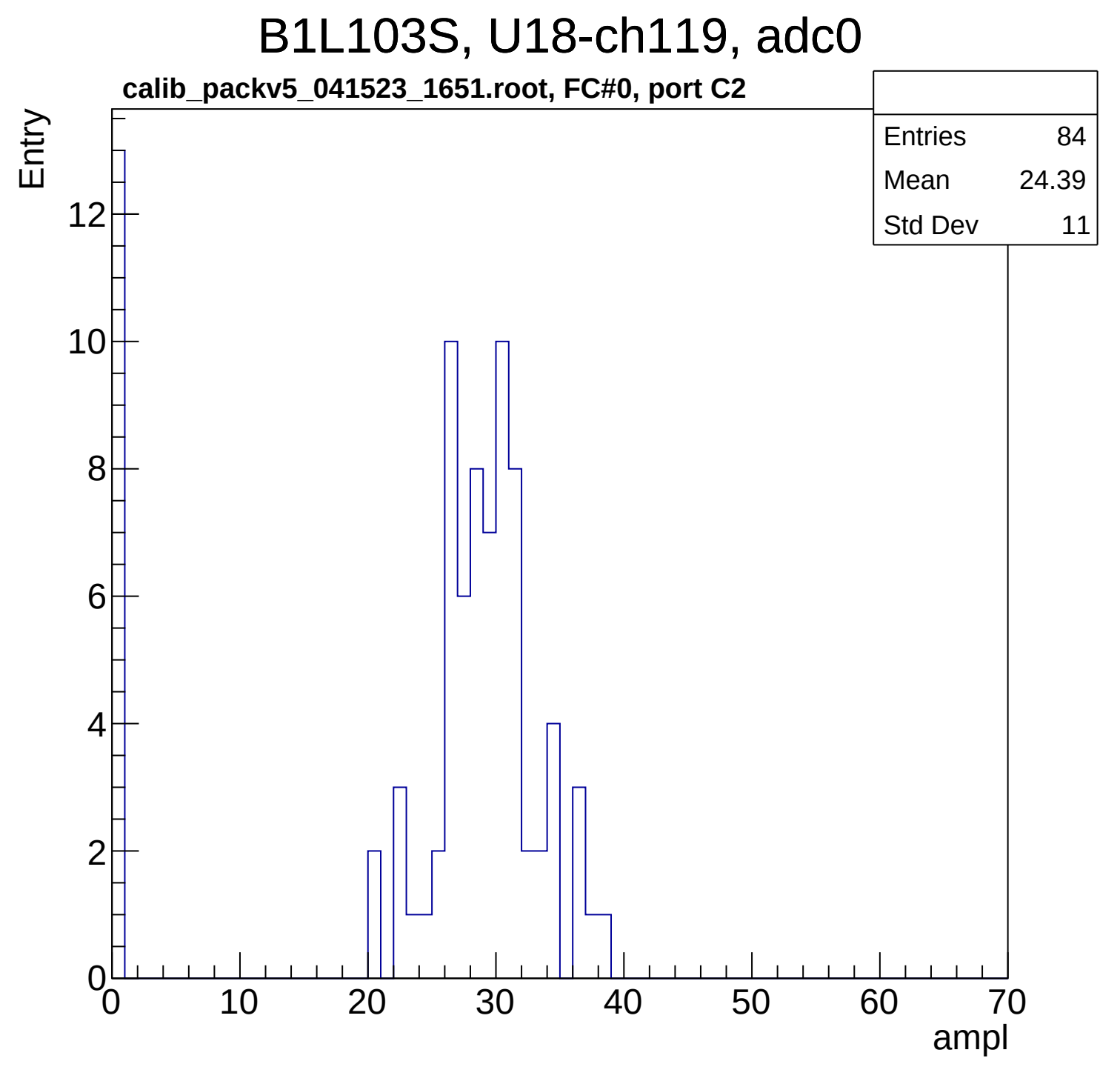
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch119, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 24.39
Std Dev 11
Entry
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2
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6
8
10
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10
20
30
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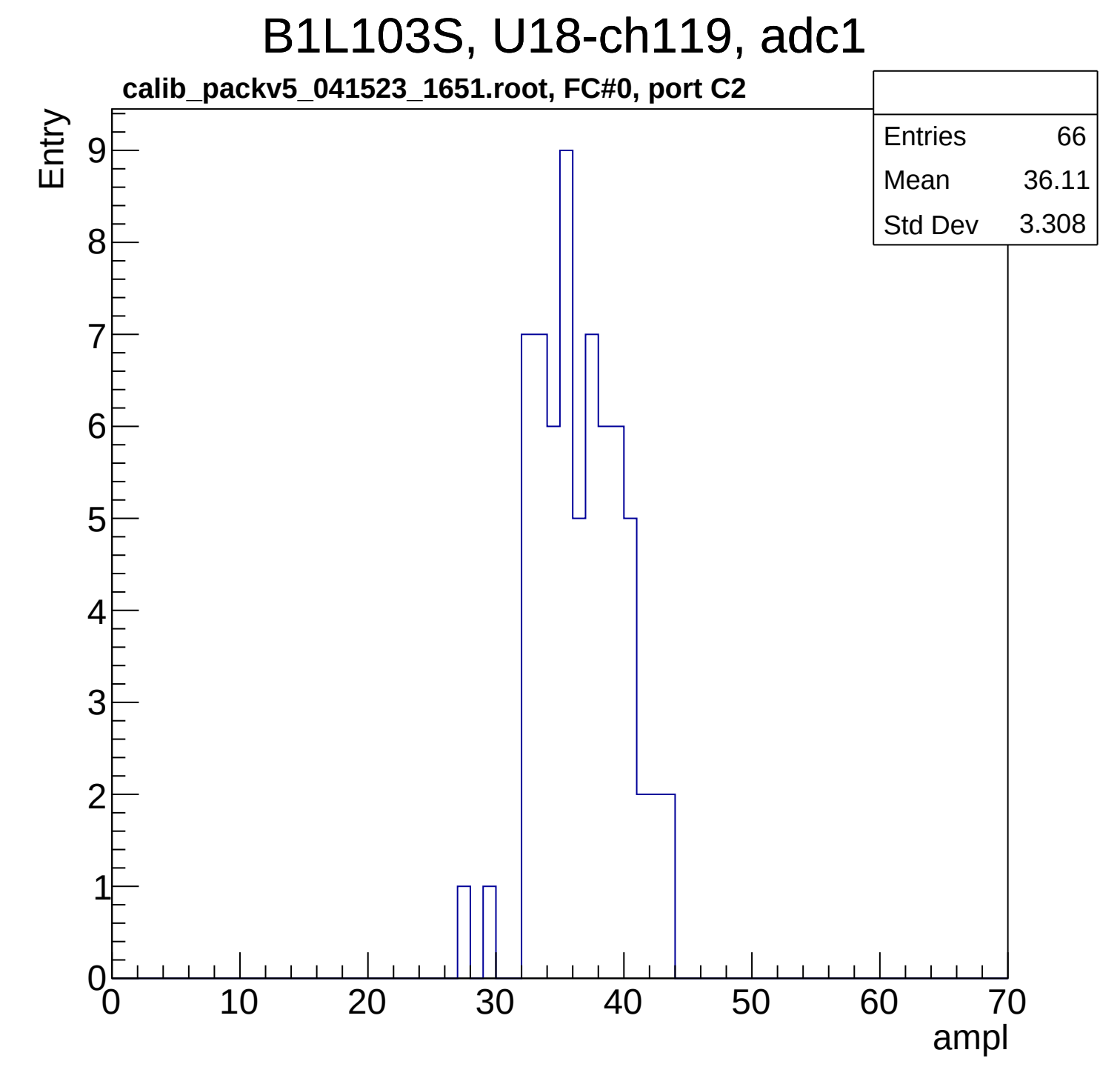
50
60
70
ampl


B1L103S, U18-ch119, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 36.11
Std Dev 3.308
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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60
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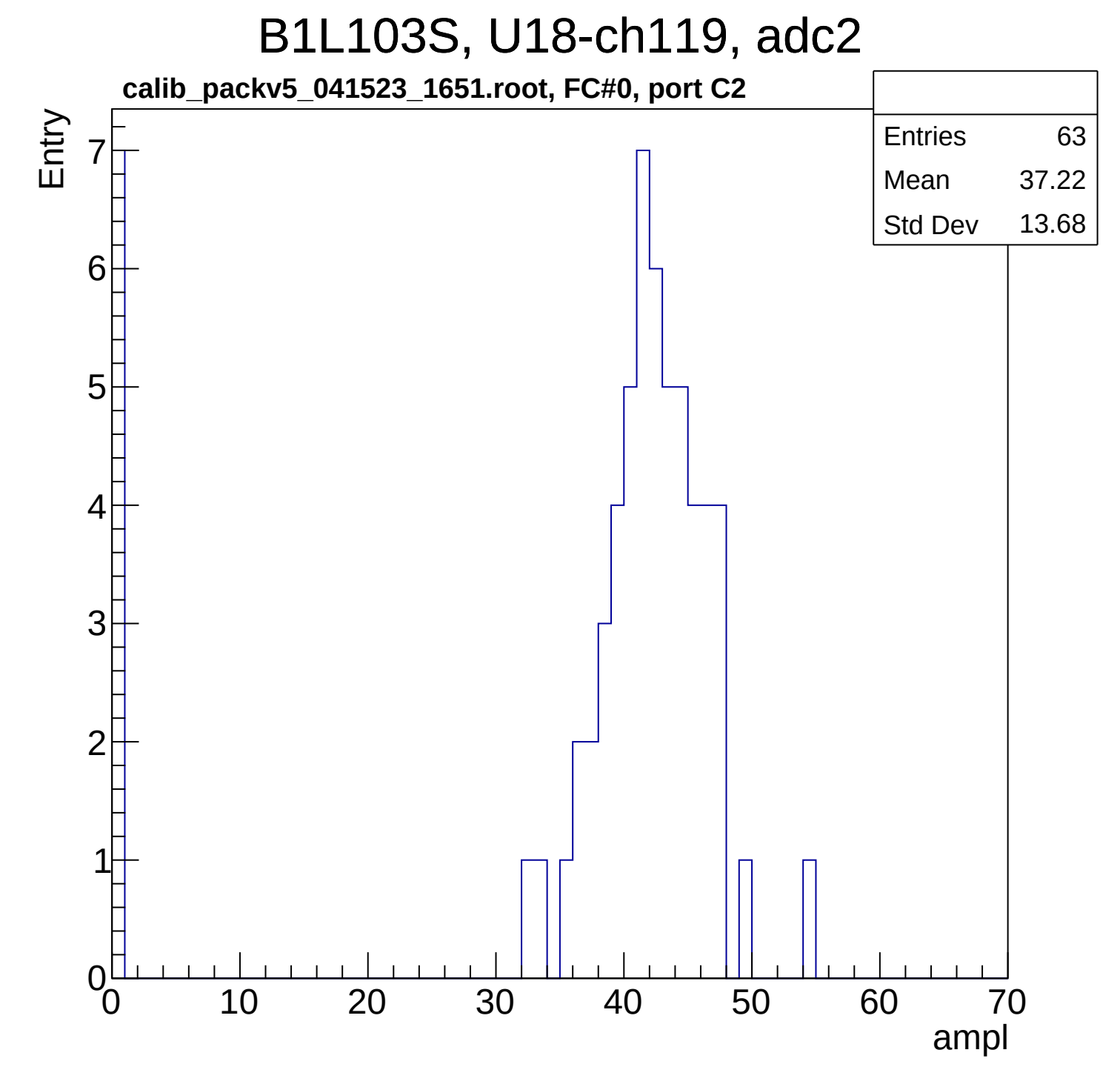
B1L103S, U18-ch119, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 37.22
Std Dev 13.68
Entry
ampl
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1
2
3
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0
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40
50
60
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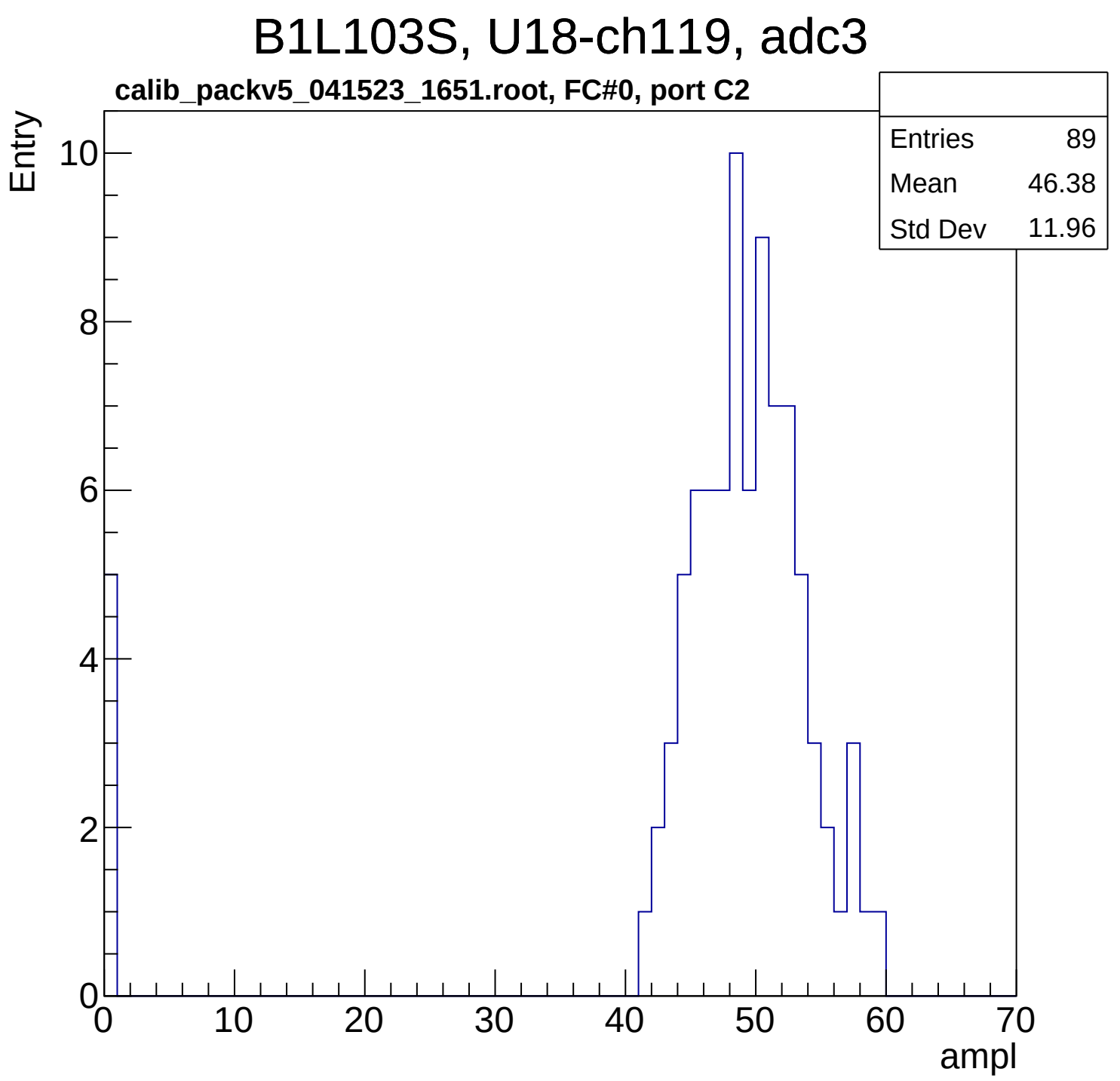
B1L103S, U18-ch119, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 89
Mean 46.38
Std Dev 11.96
Entry
ampl
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6
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40
50
60
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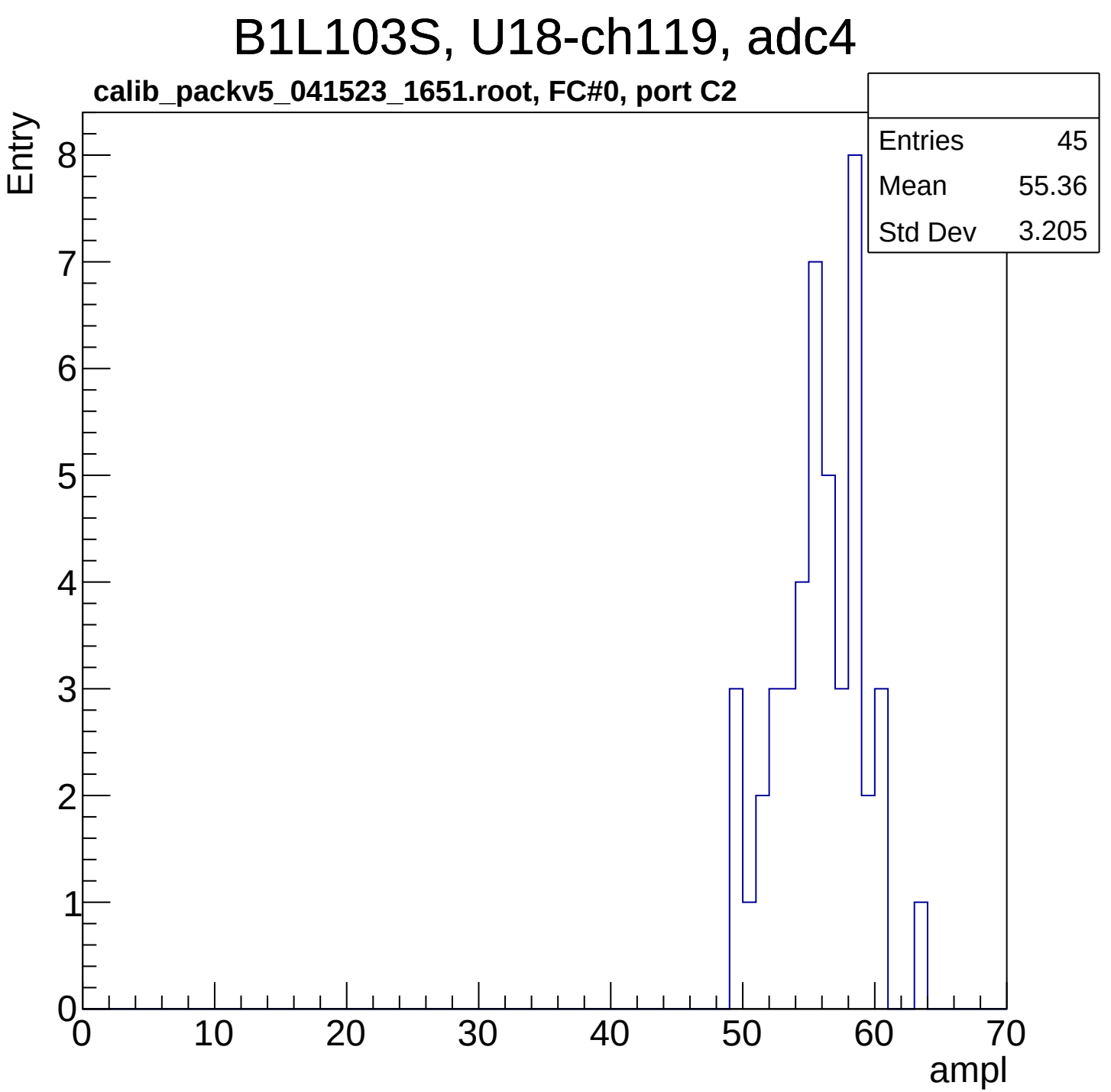
B1L103S, U18-ch119, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 55.36
Std Dev 3.205
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
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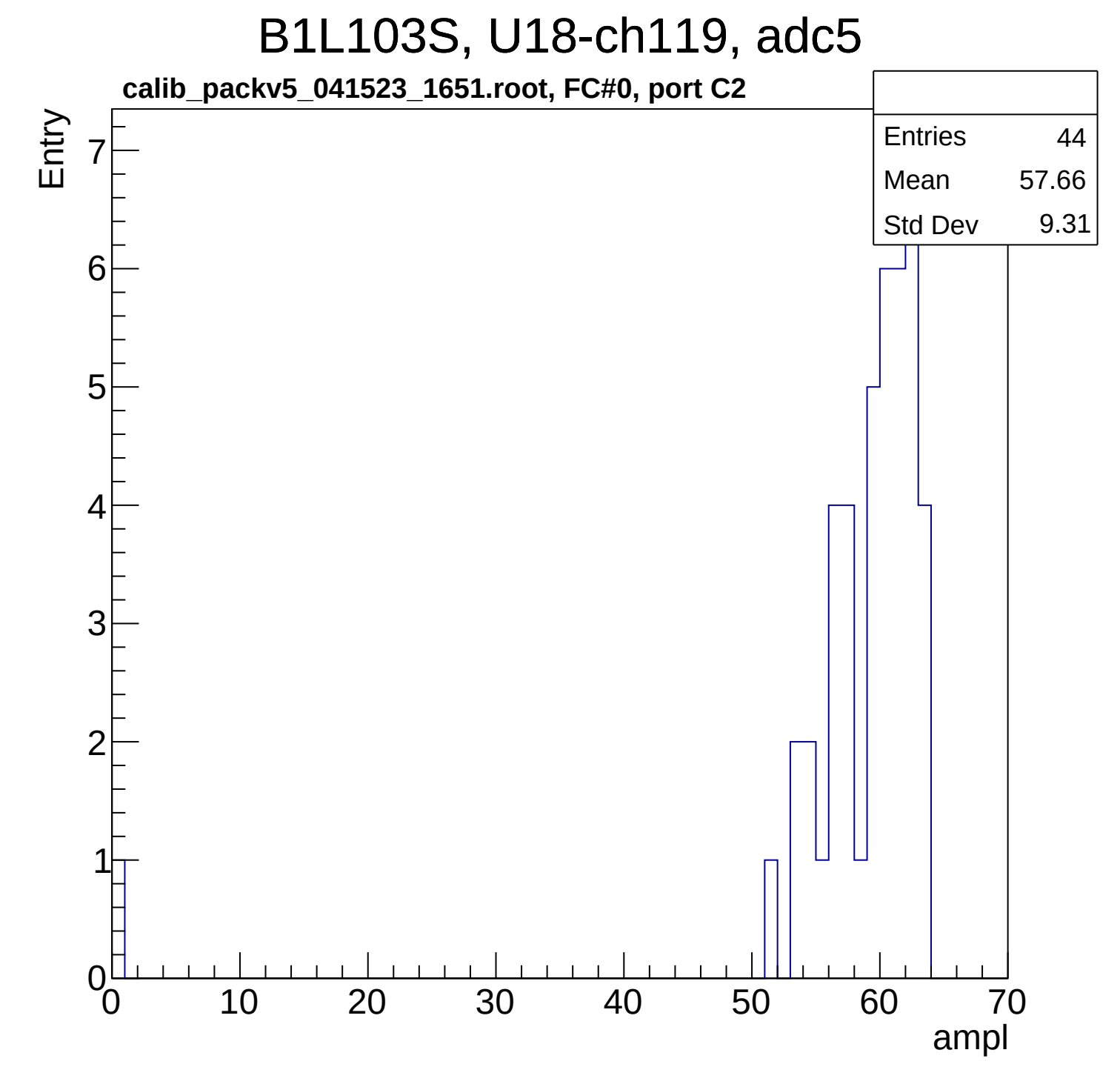
B1L103S, U18-ch119, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 57.66
Std Dev 9.31
Entry
ampl
0
1
2
3
4
5
6
7
0
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20
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40
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60
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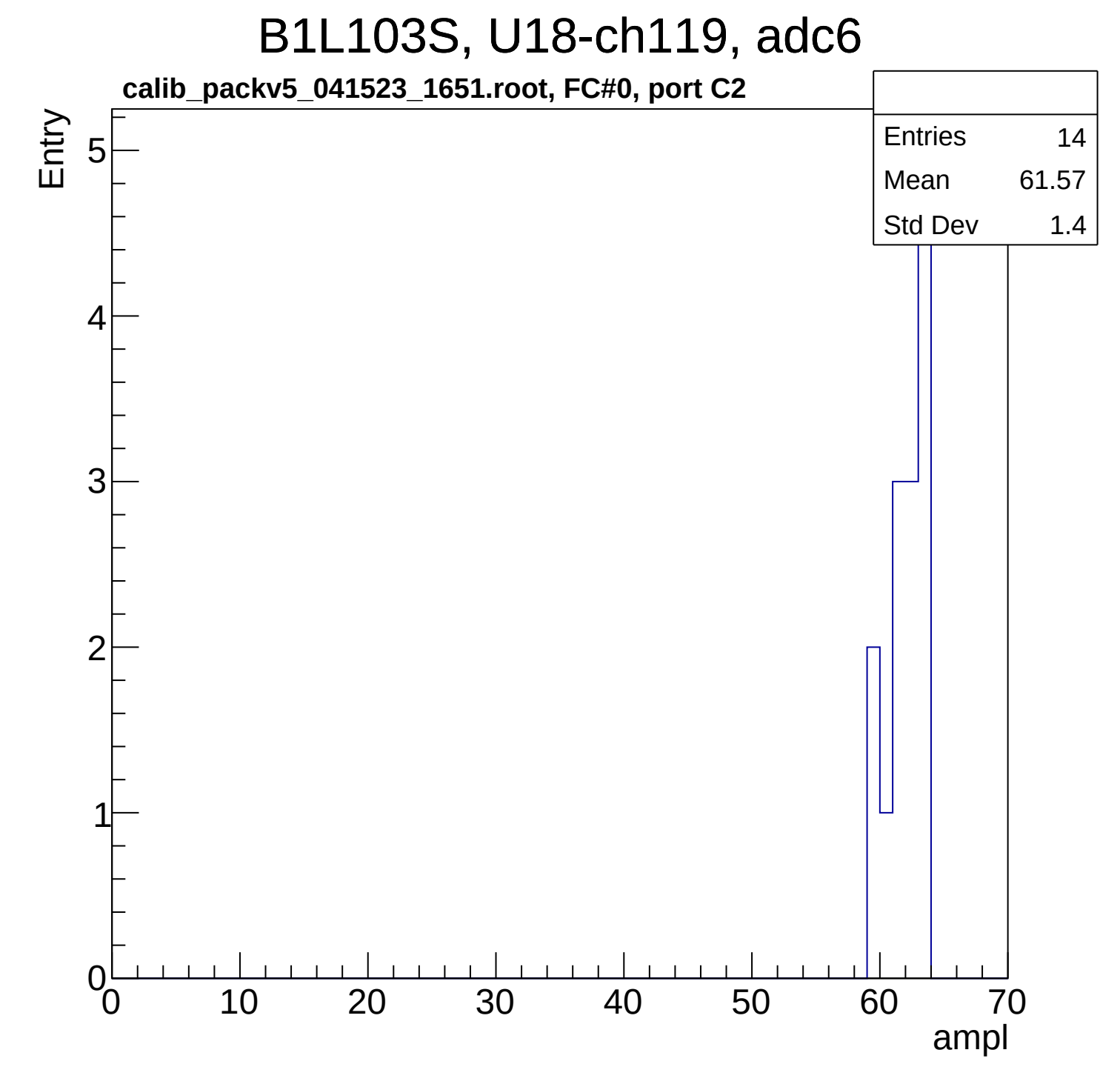
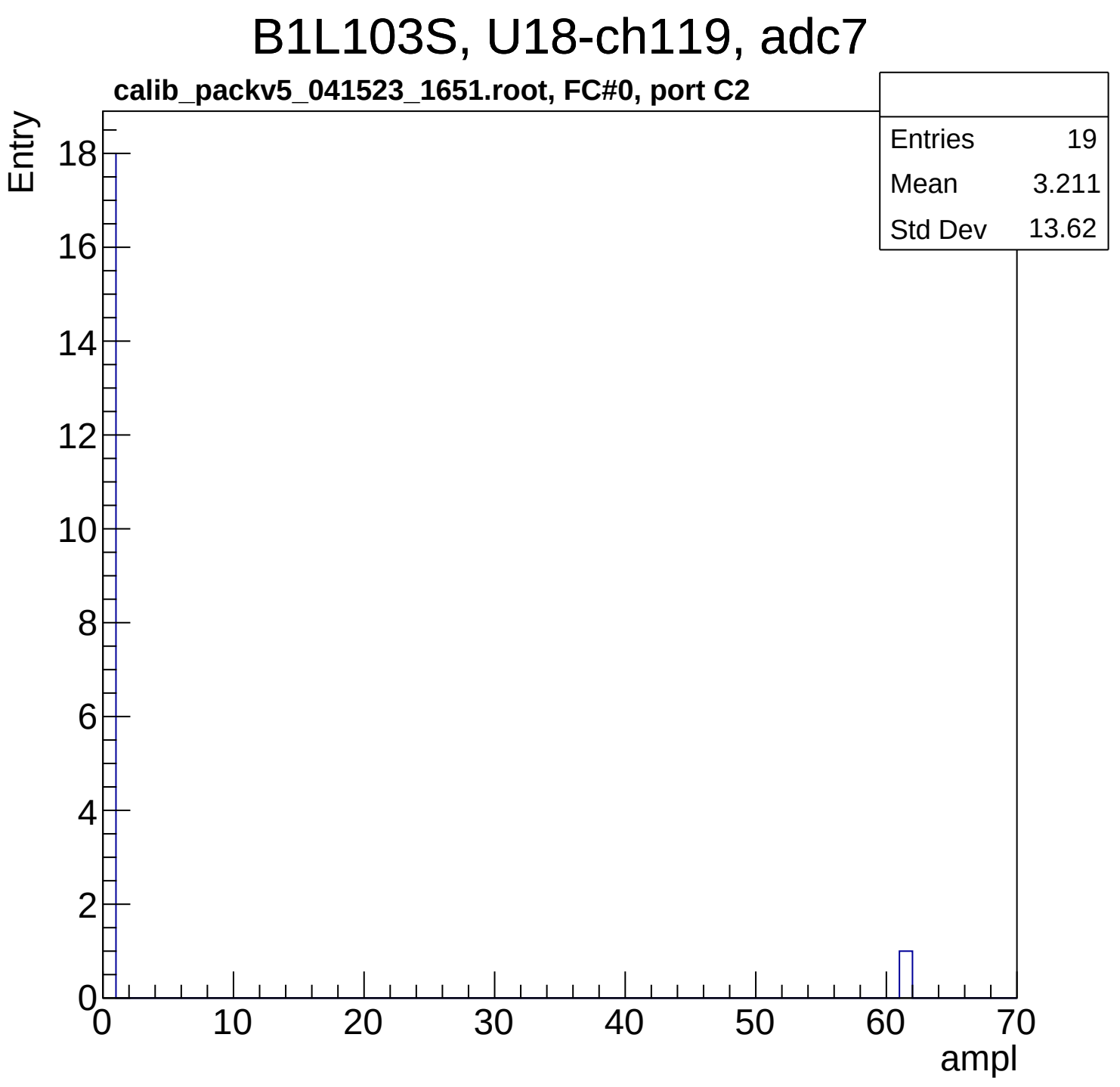

B1L103S, U18-ch119, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 14
Mean 61.57
Std Dev 1.4
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U18-ch119, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 3.211
Std Dev 13.62
Entry
ampl
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2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
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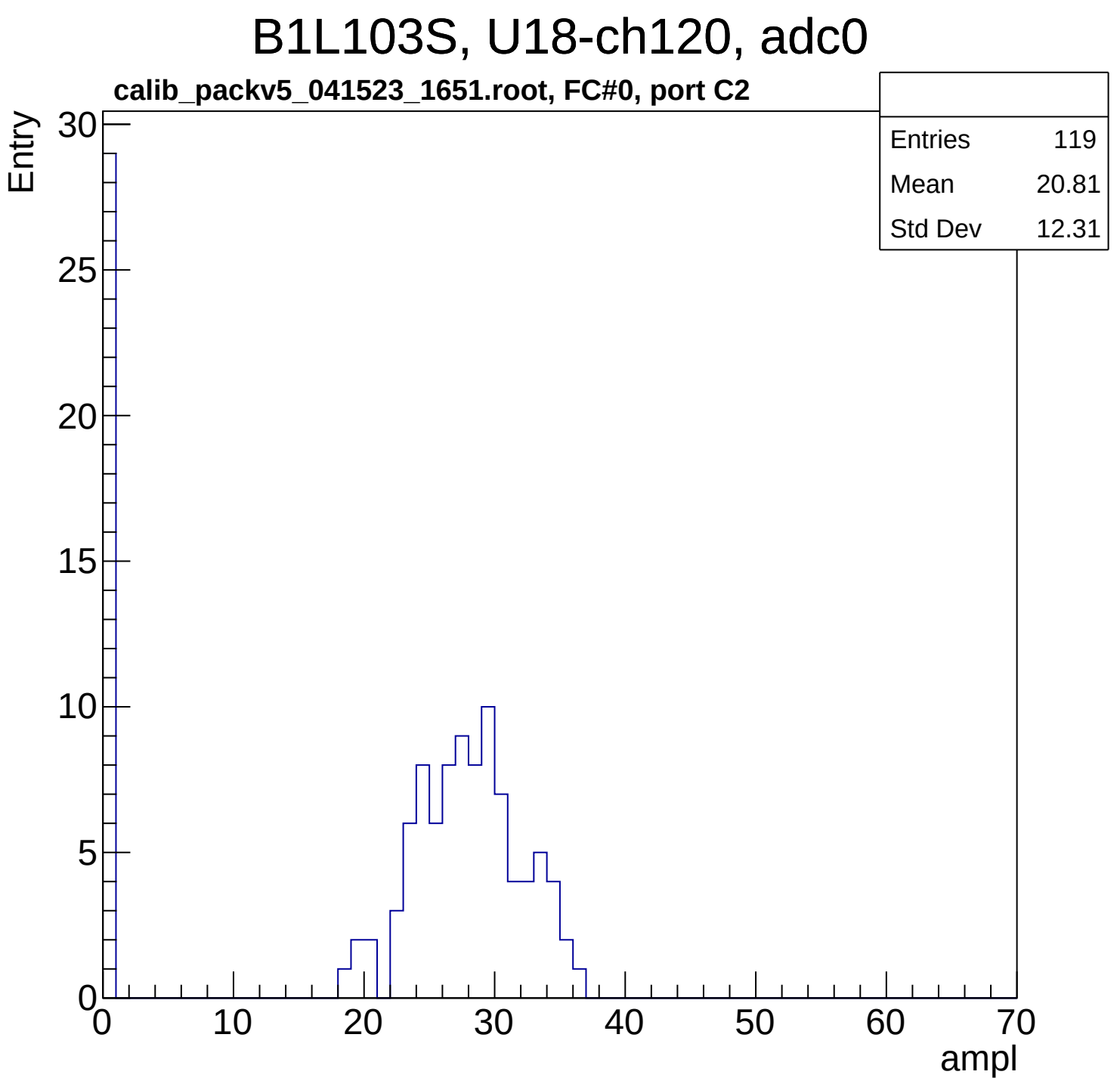
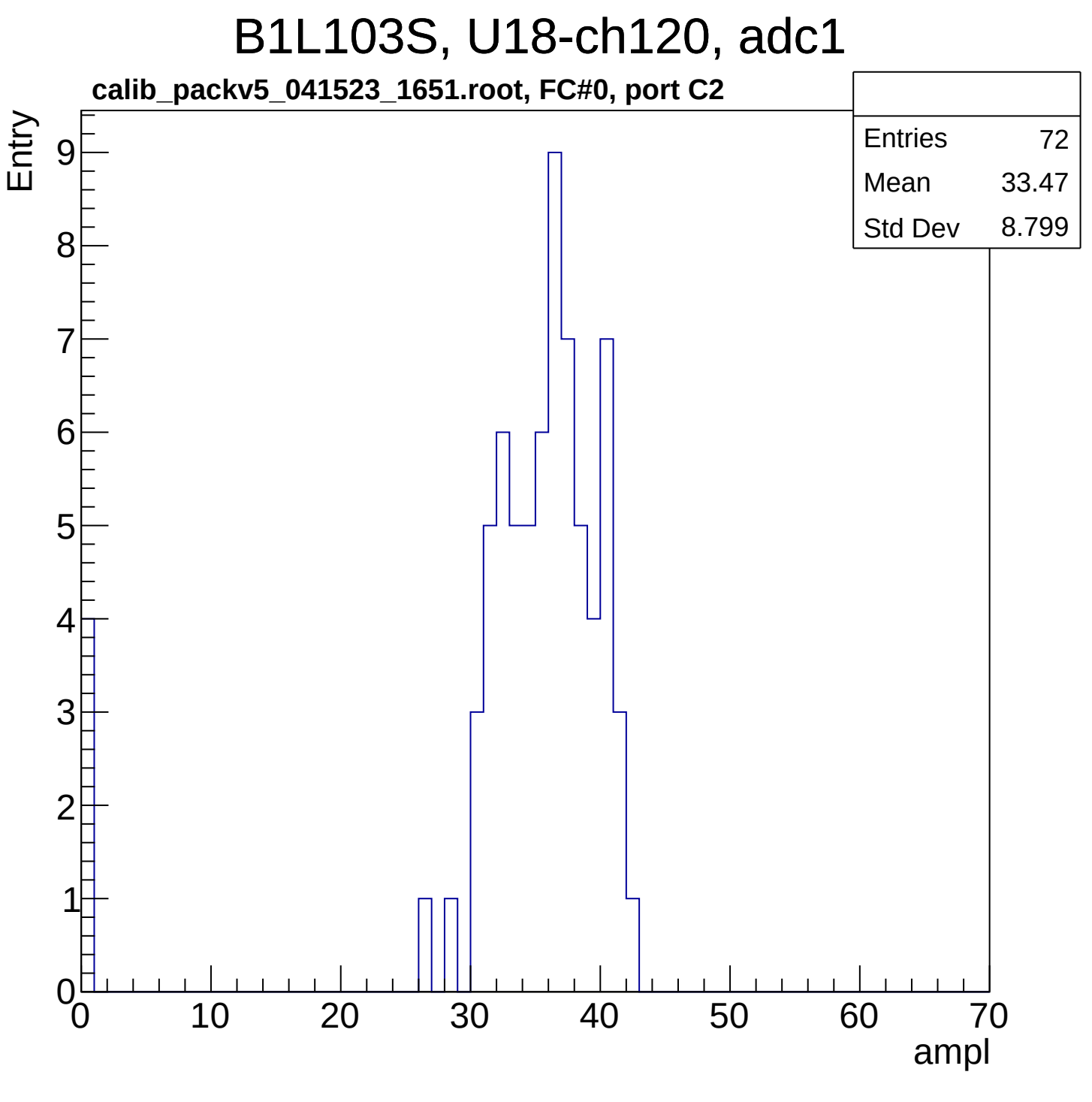

B1L103S, U18-ch120, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 119
Mean 20.81
Std Dev 12.31
Entry
ampl
0
5
10
15
20
25
30
0
10
20
30
40
50
60
70


B1L103S, U18-ch120, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 33.47
Std Dev 8.799
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
50
60
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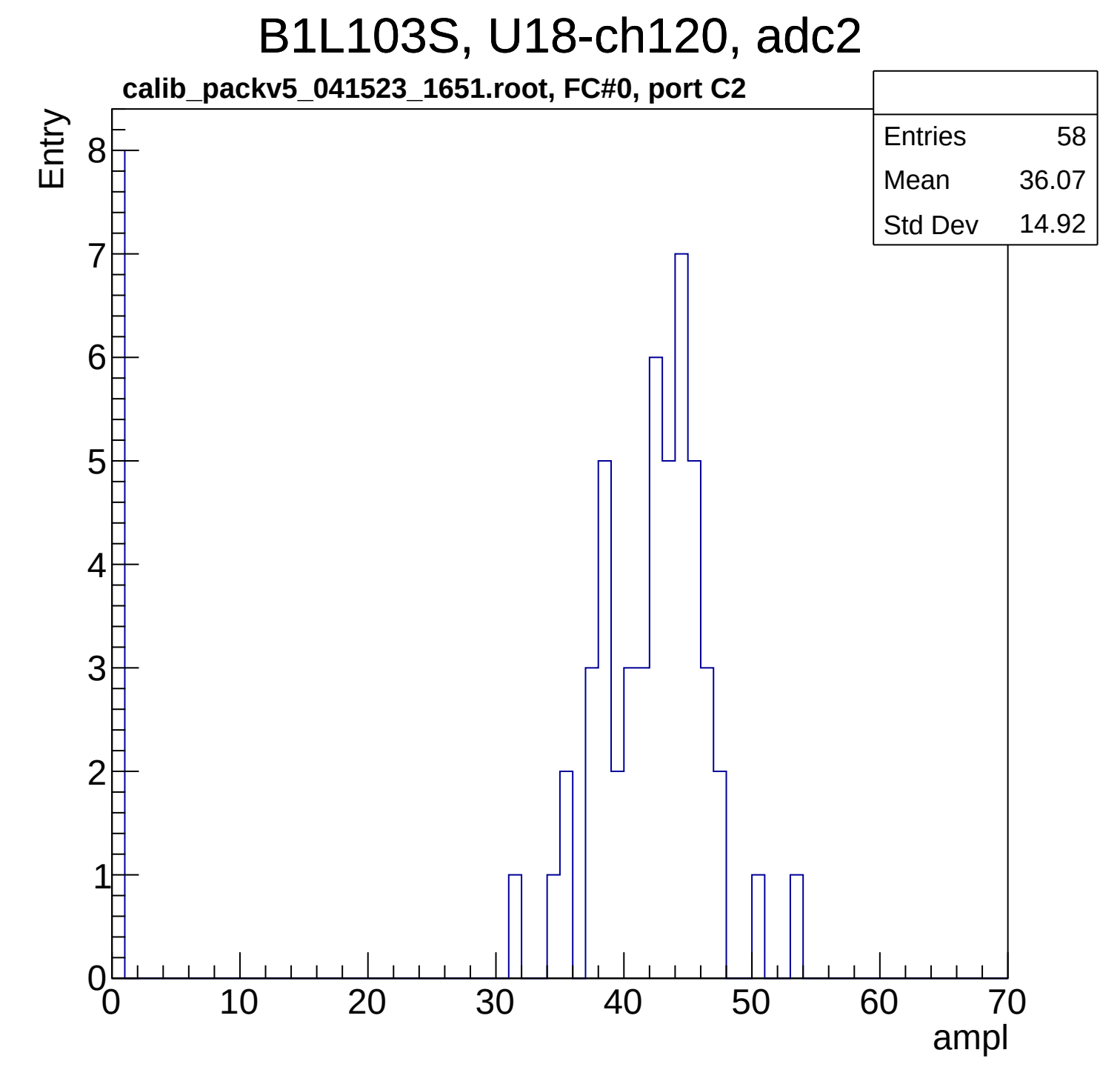
B1L103S, U18-ch120, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 36.07
Std Dev 14.92
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
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40
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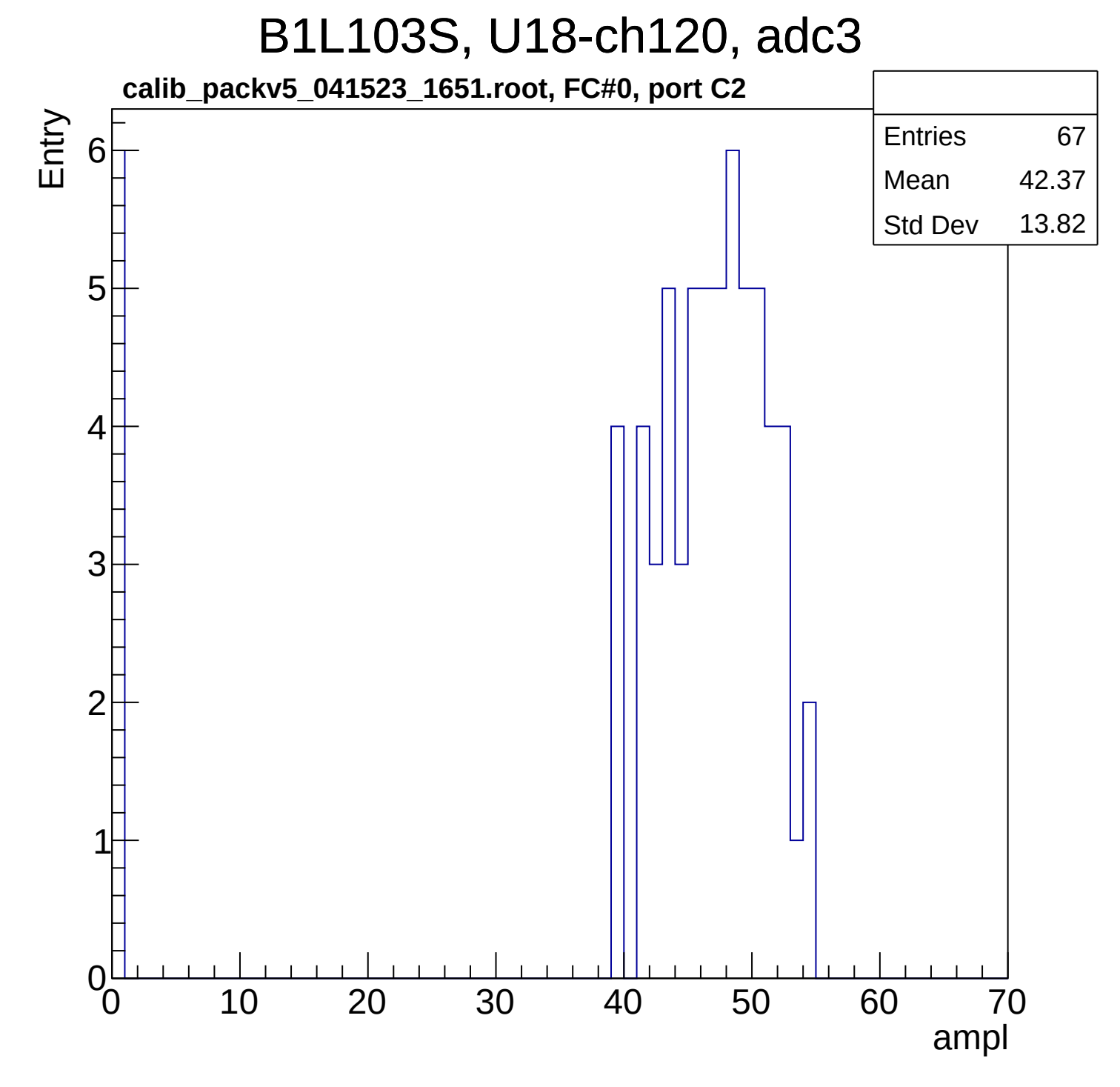
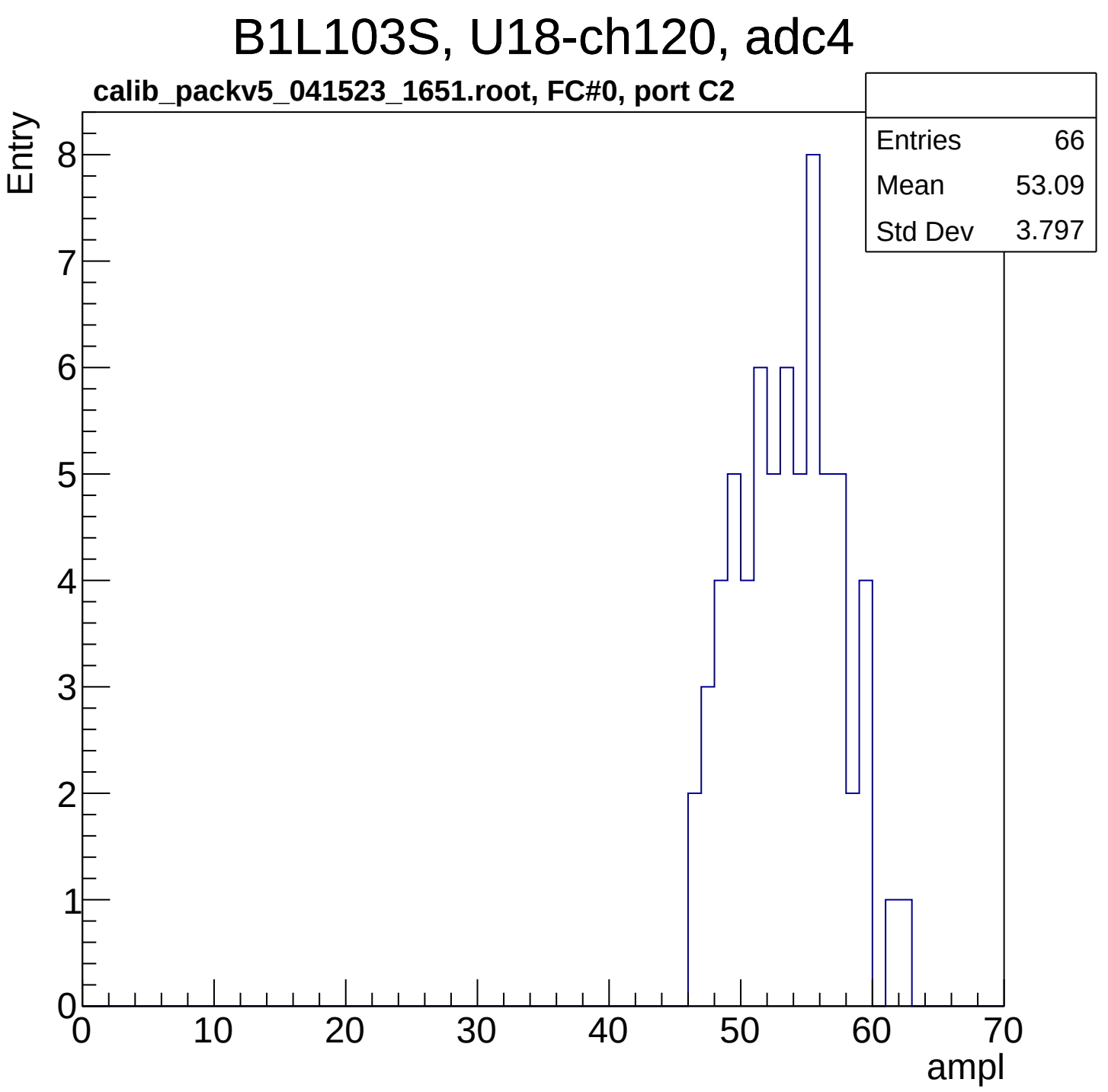
60
70


B1L103S, U18-ch120, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 42.37
Std Dev 13.82
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U18-ch120, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 53.09
Std Dev 3.797
Entry
ampl
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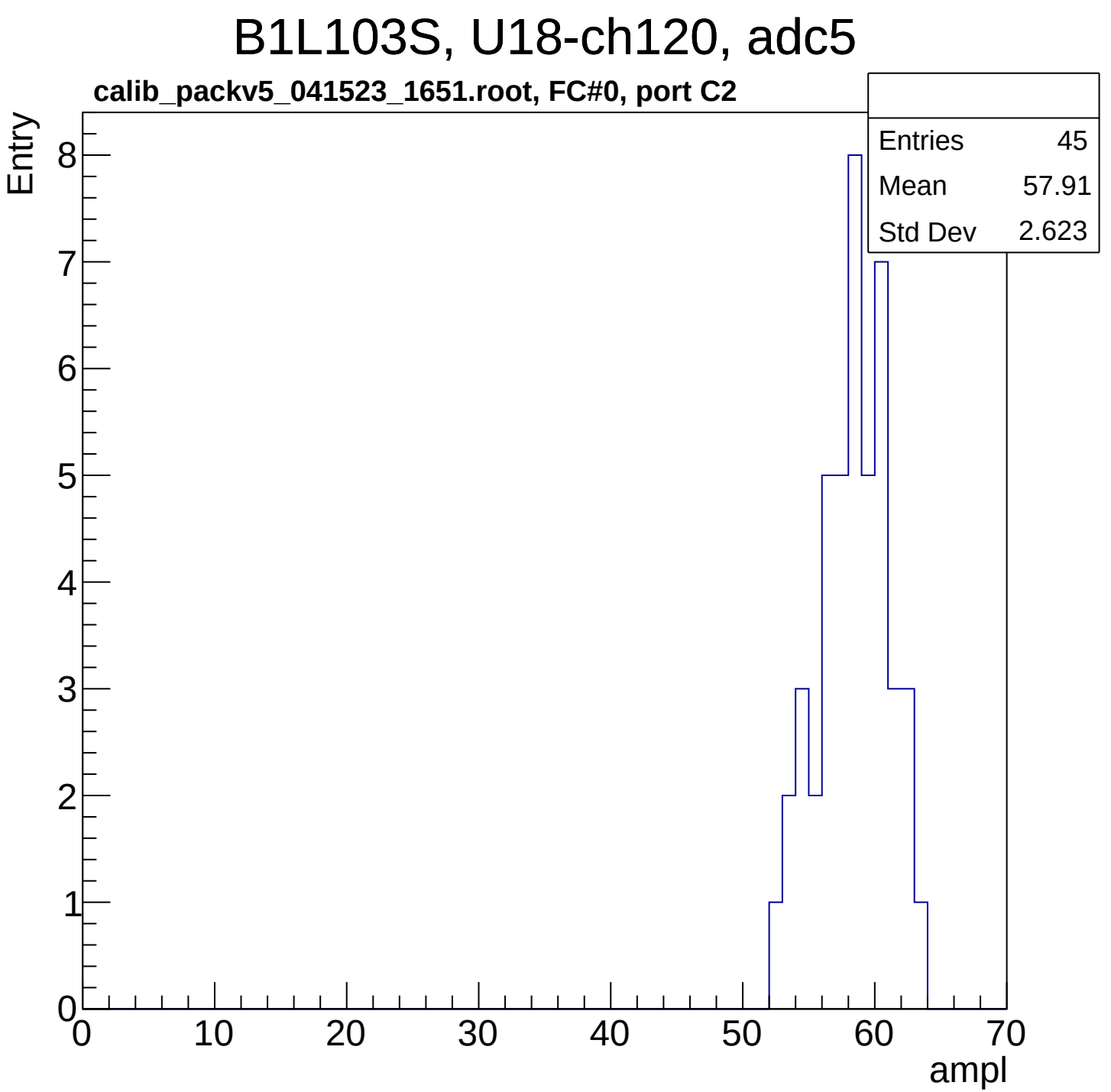
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch120, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 57.91
Std Dev 2.623
Entry
ampl
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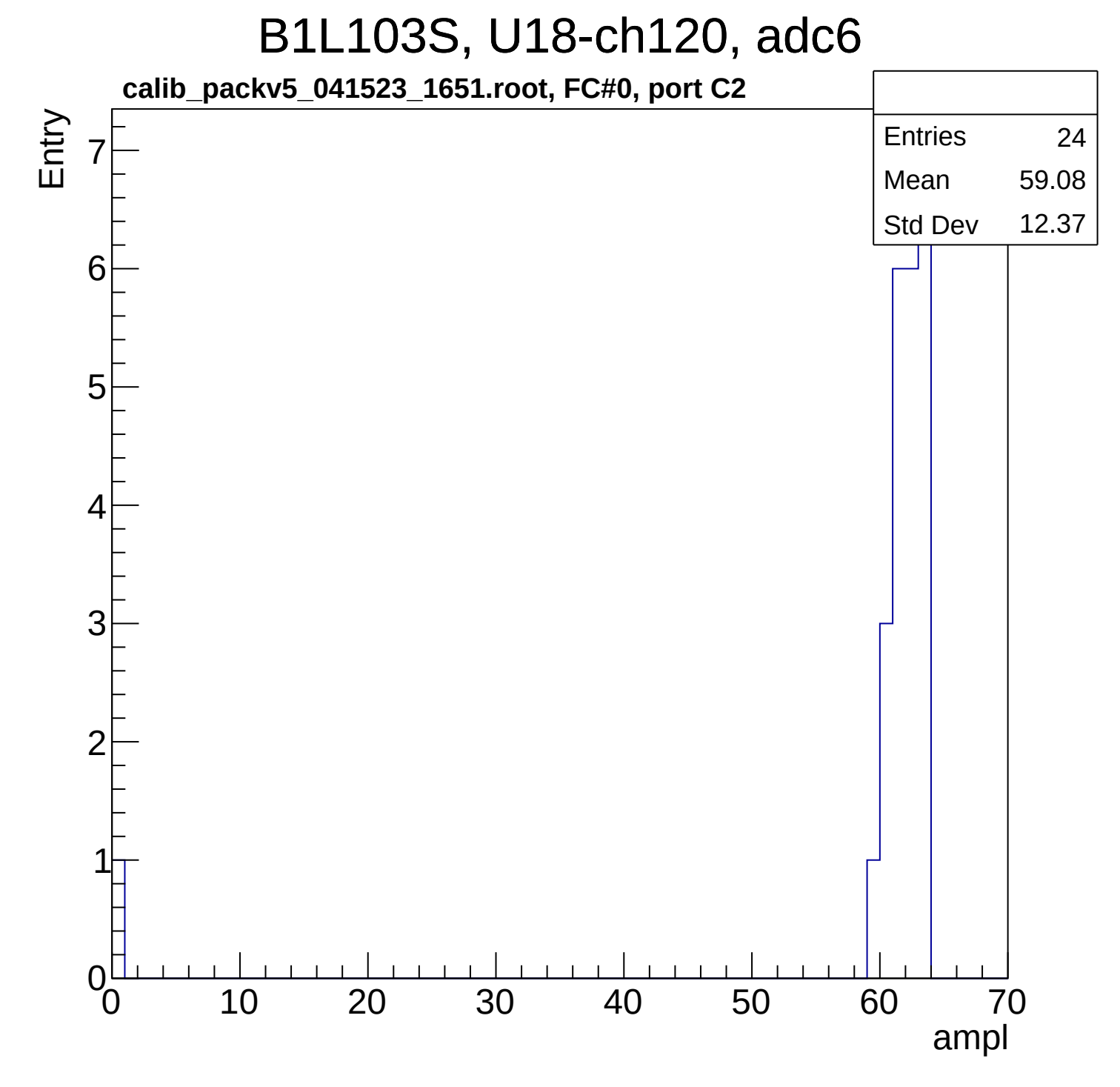
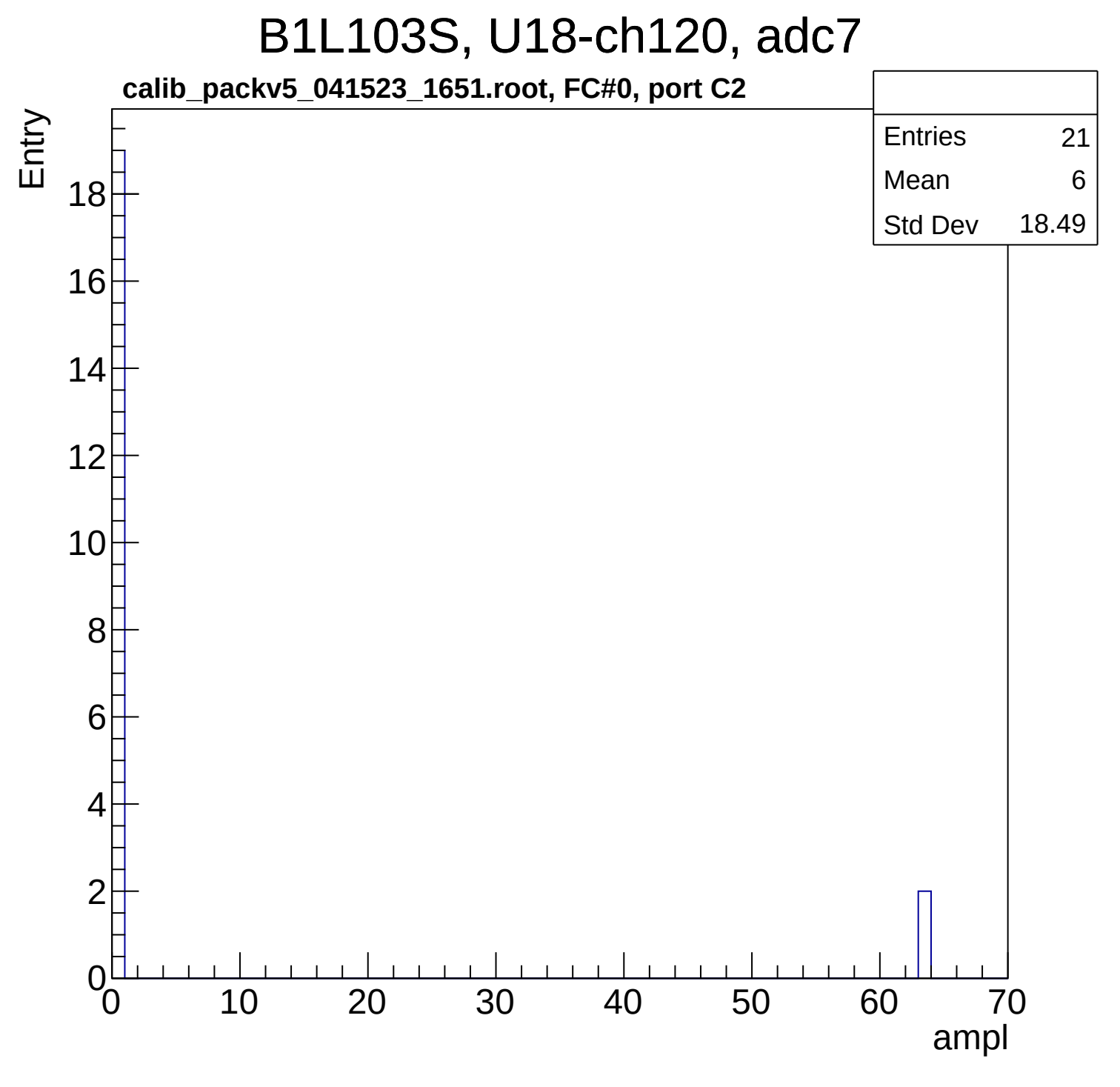
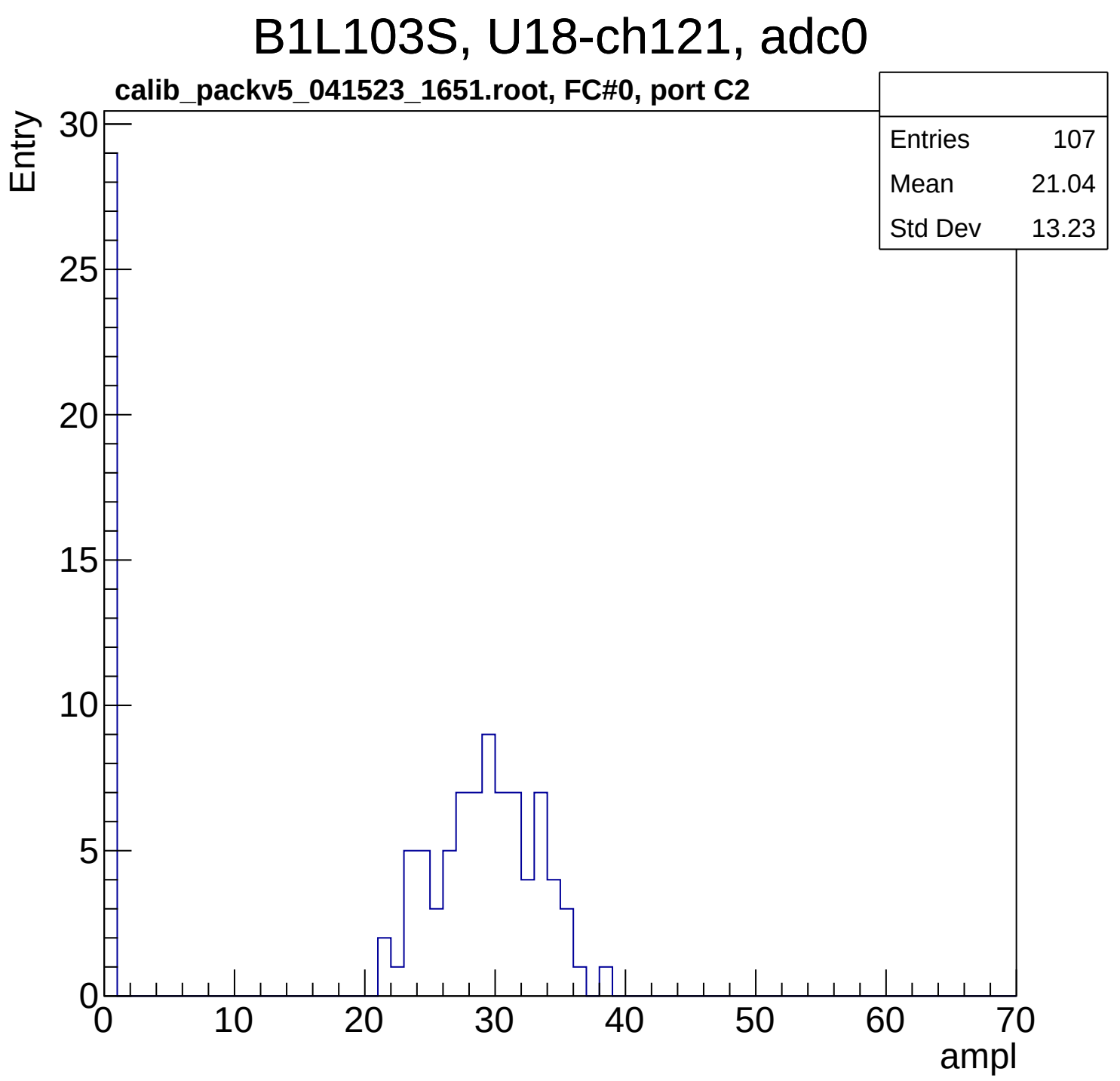
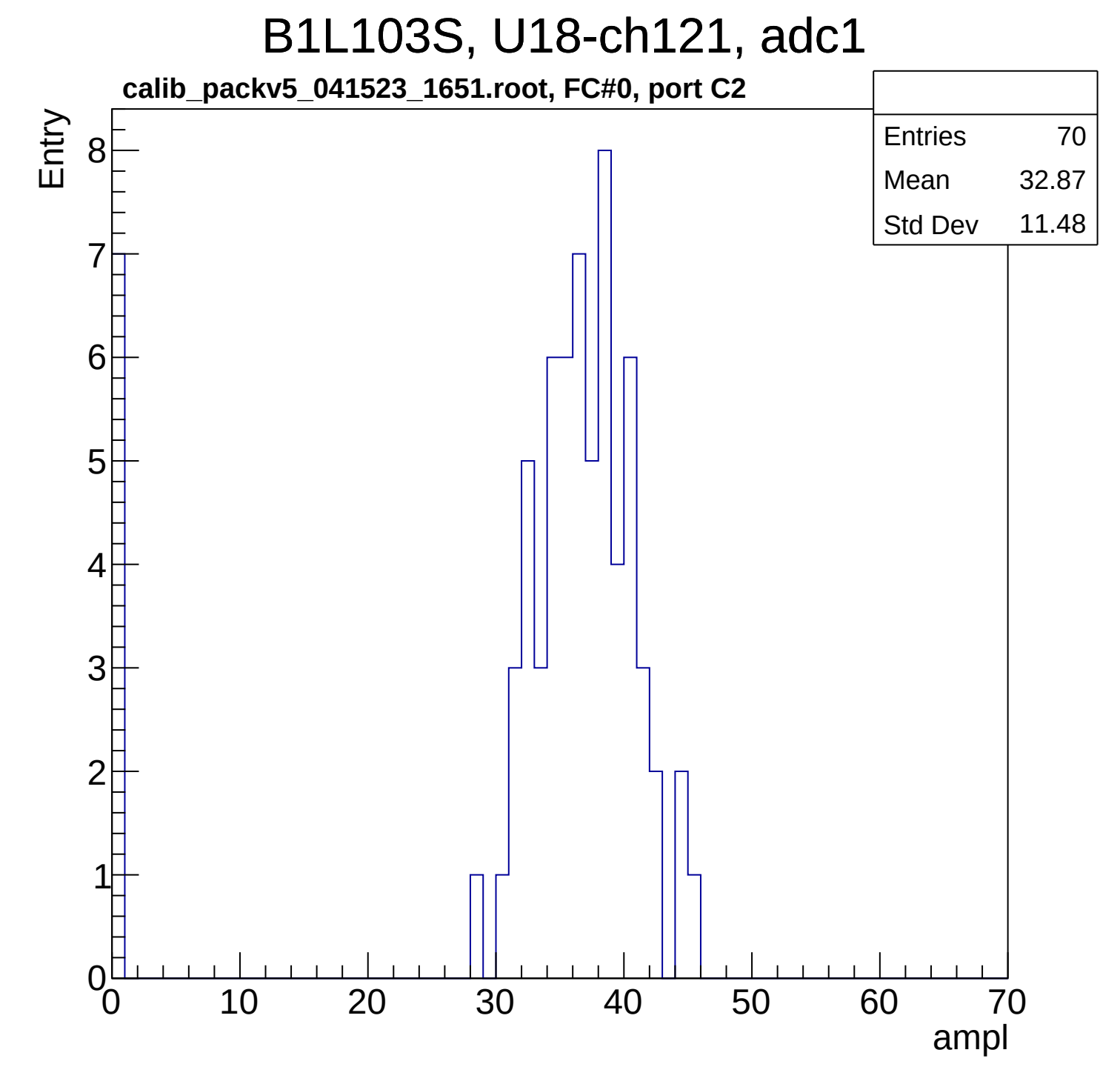
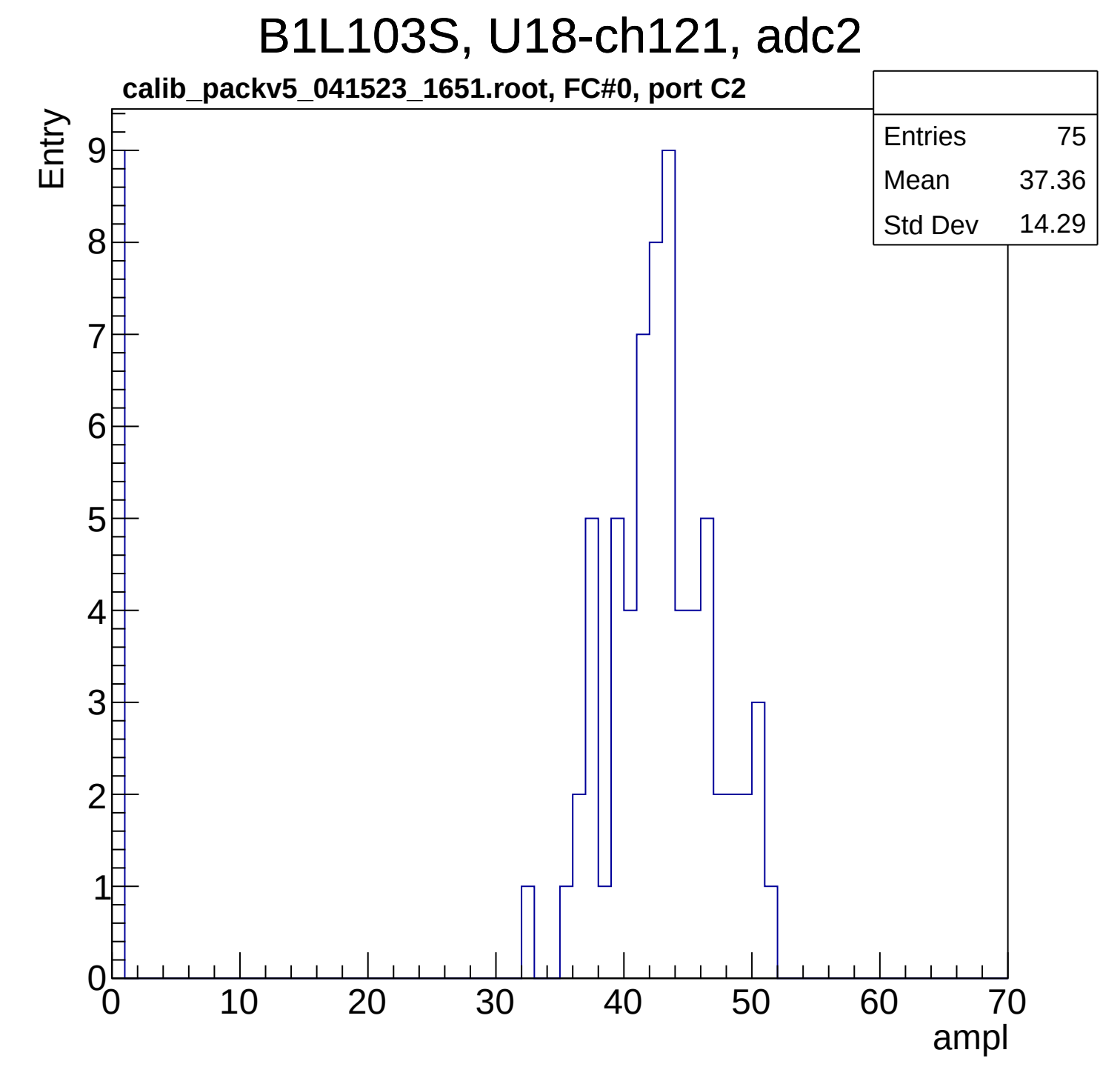
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

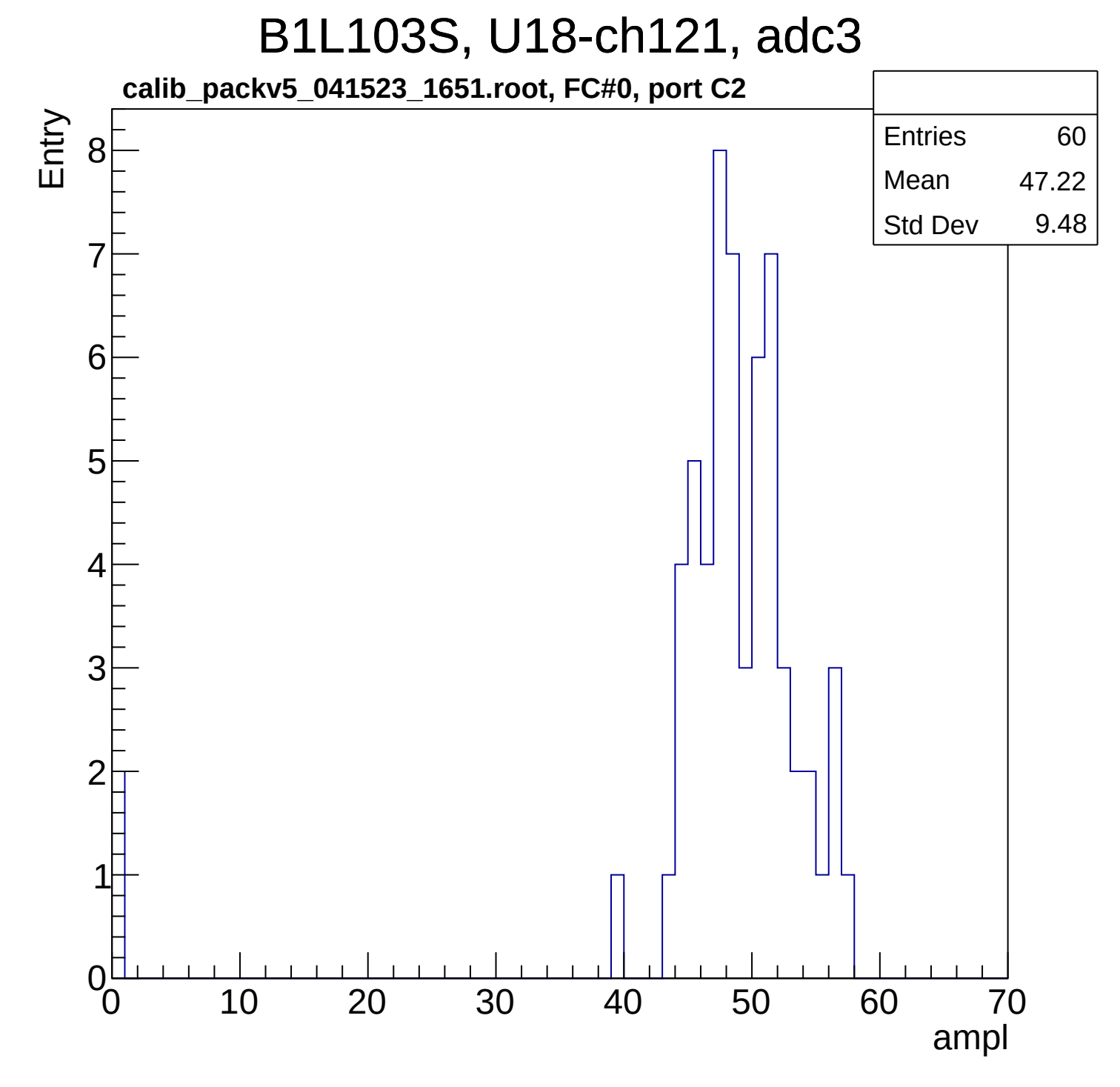

B1L103S, U18-ch120, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 24
Mean 59.08
Std Dev 12.37
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U18-ch120, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 6
Std Dev 18.49
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch121, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 107
Mean 21.04
Std Dev 13.23
Entry
ampl
0
5
10
15
20
25
30
0
10
20
30
40
50
60
70


B1L103S, U18-ch121, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 32.87
Std Dev 11.48
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch121, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 37.36
Std Dev 14.29
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U18-ch121, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 47.22
Std Dev 9.48
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
30
40
50
60
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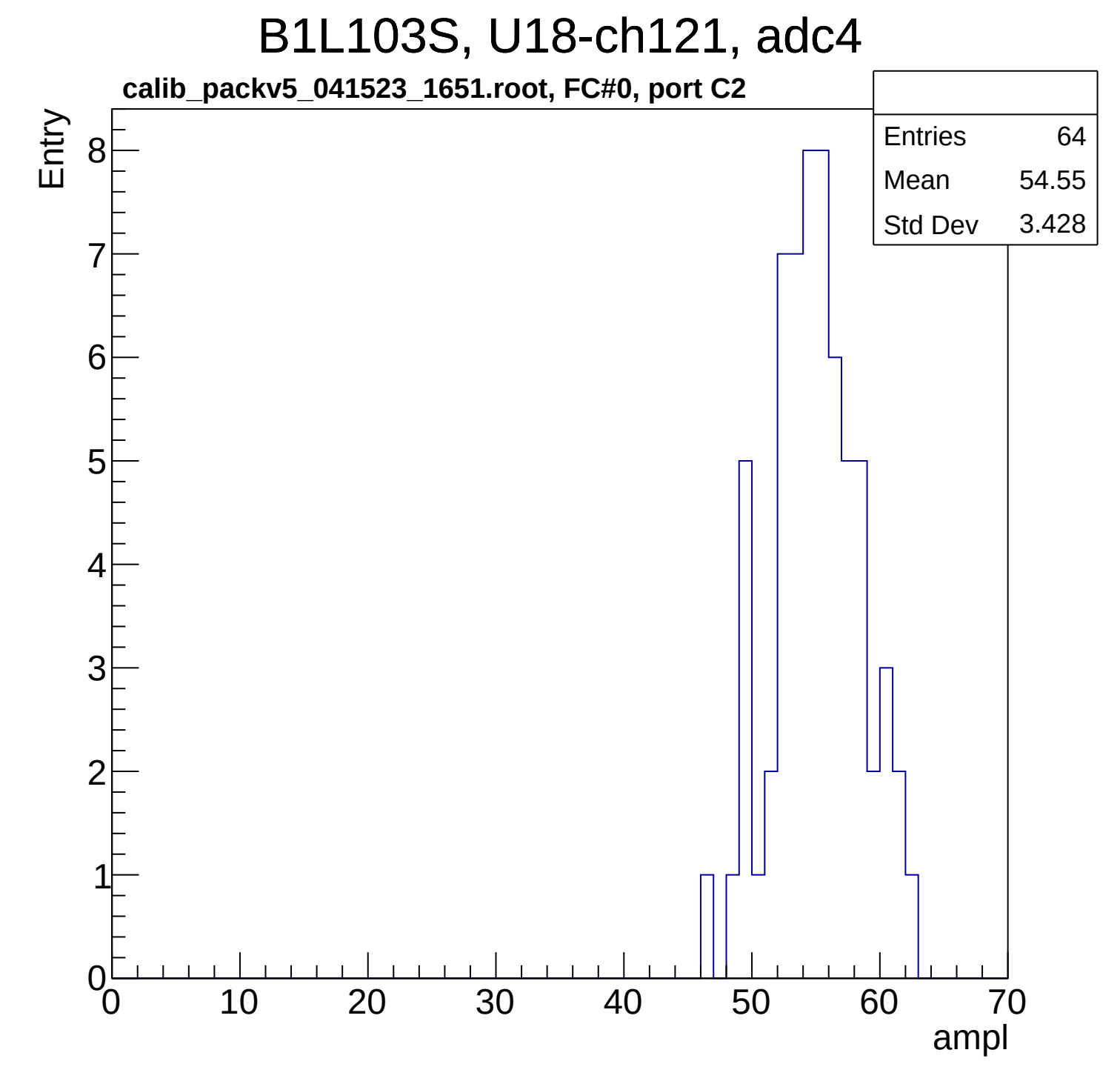
B1L103S, U18-ch121, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 54.55
Std Dev 3.428
Entry
ampl
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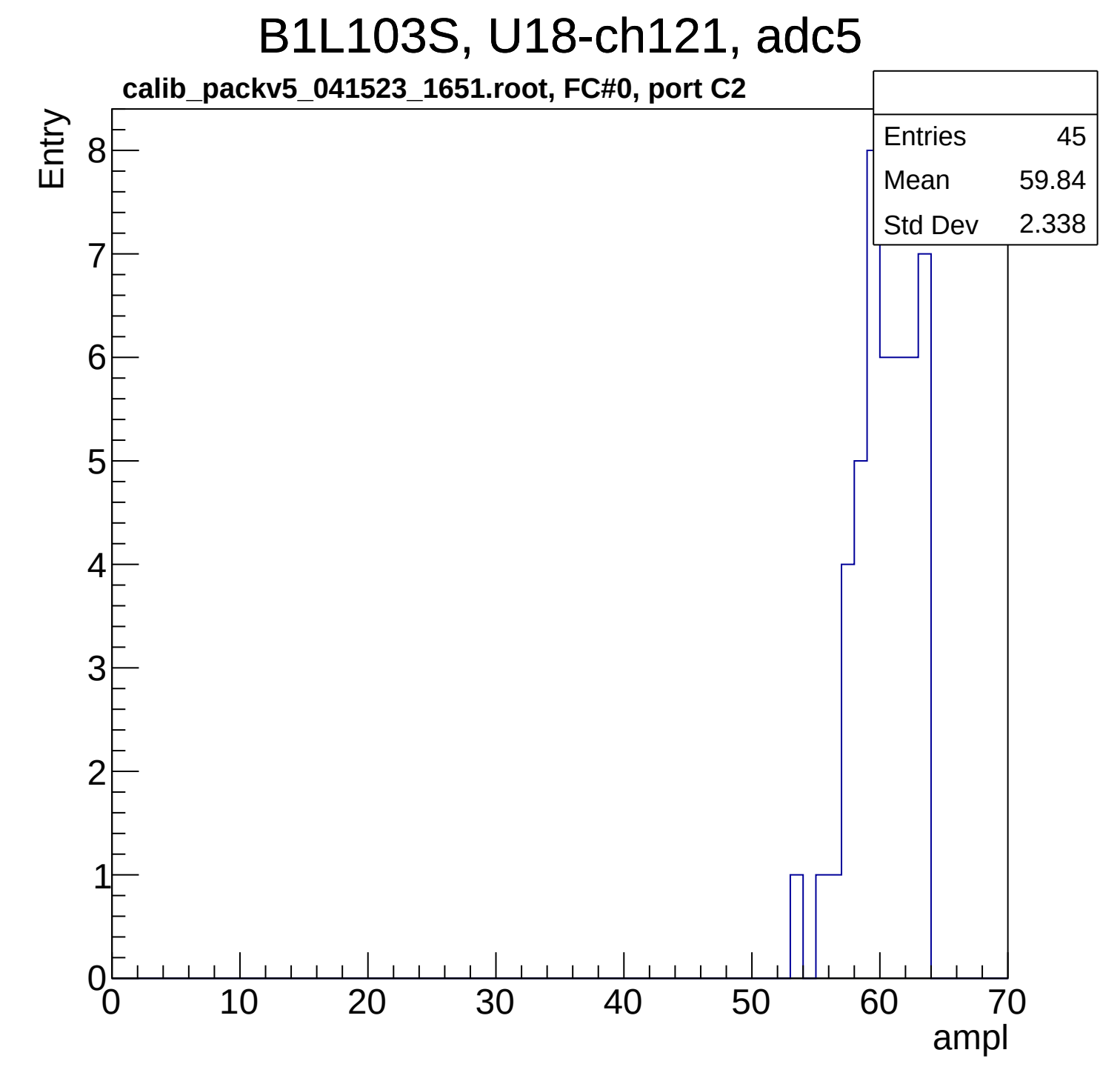
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch121, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 59.84
Std Dev 2.338
Entry
ampl
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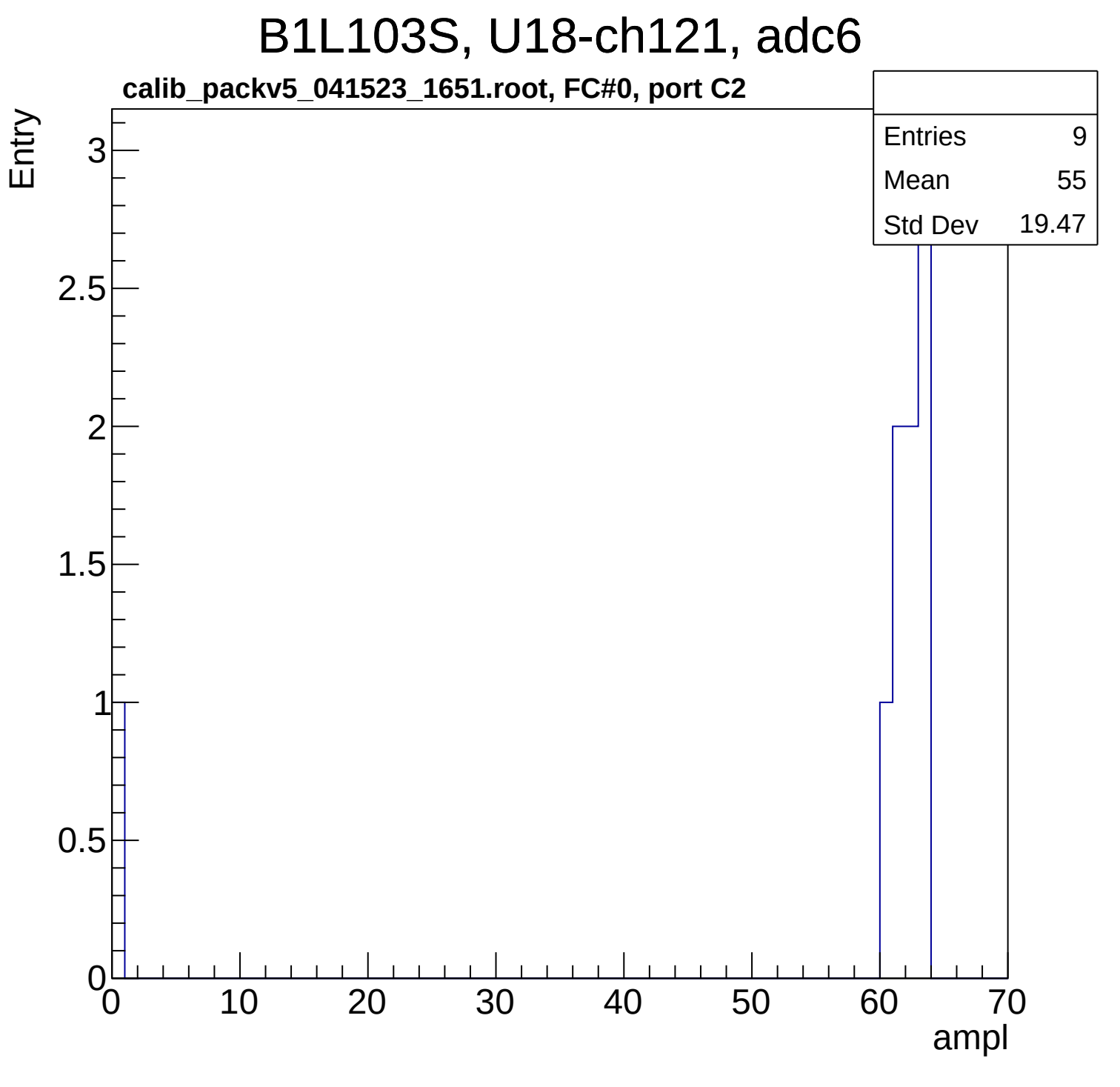
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch121, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 9
Mean 55
Std Dev 19.47
Entry
ampl
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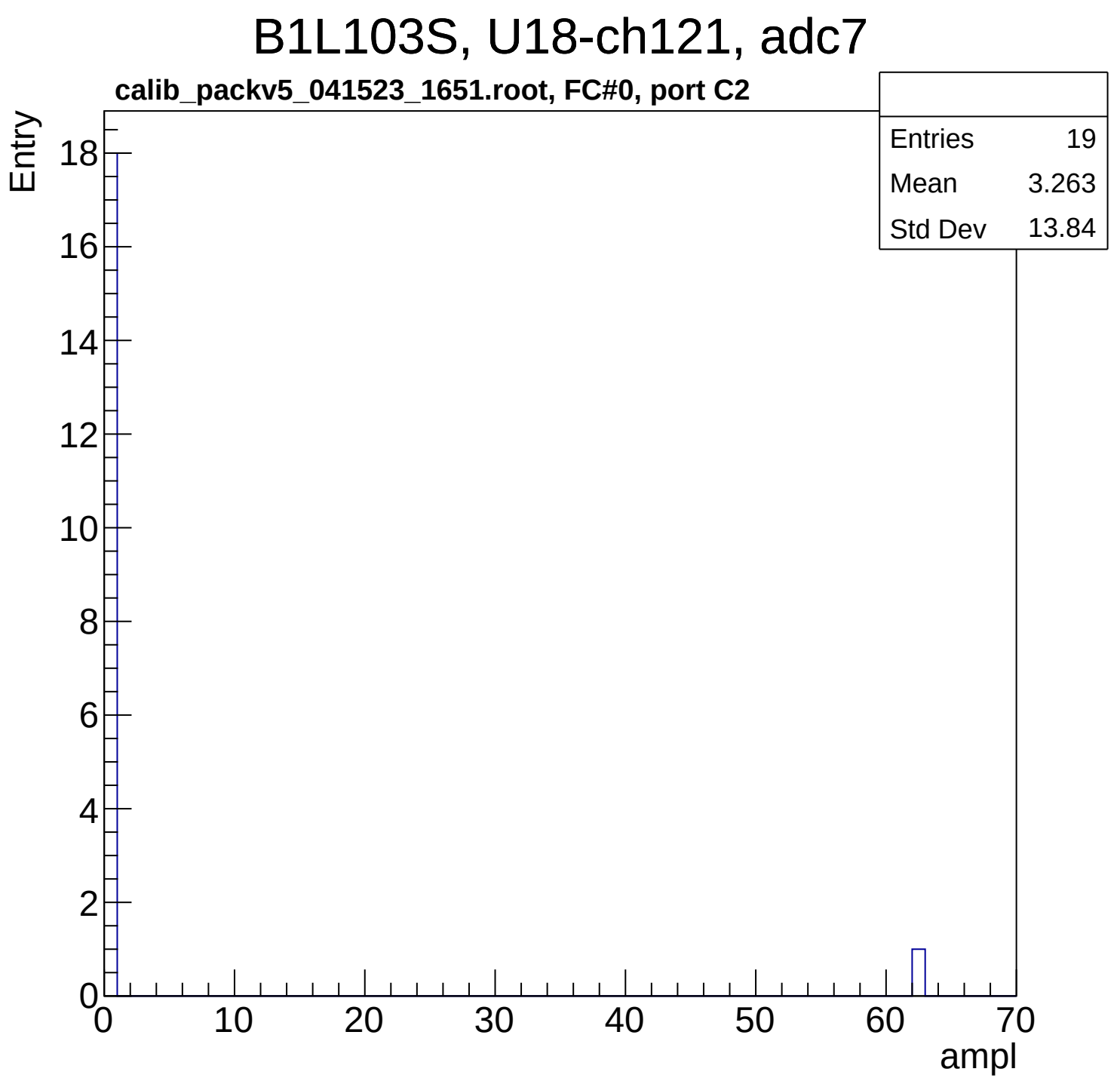
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U18-ch121, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 3.263
Std Dev 13.84
Entry
0
2
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6
8
10
12
14
16
18
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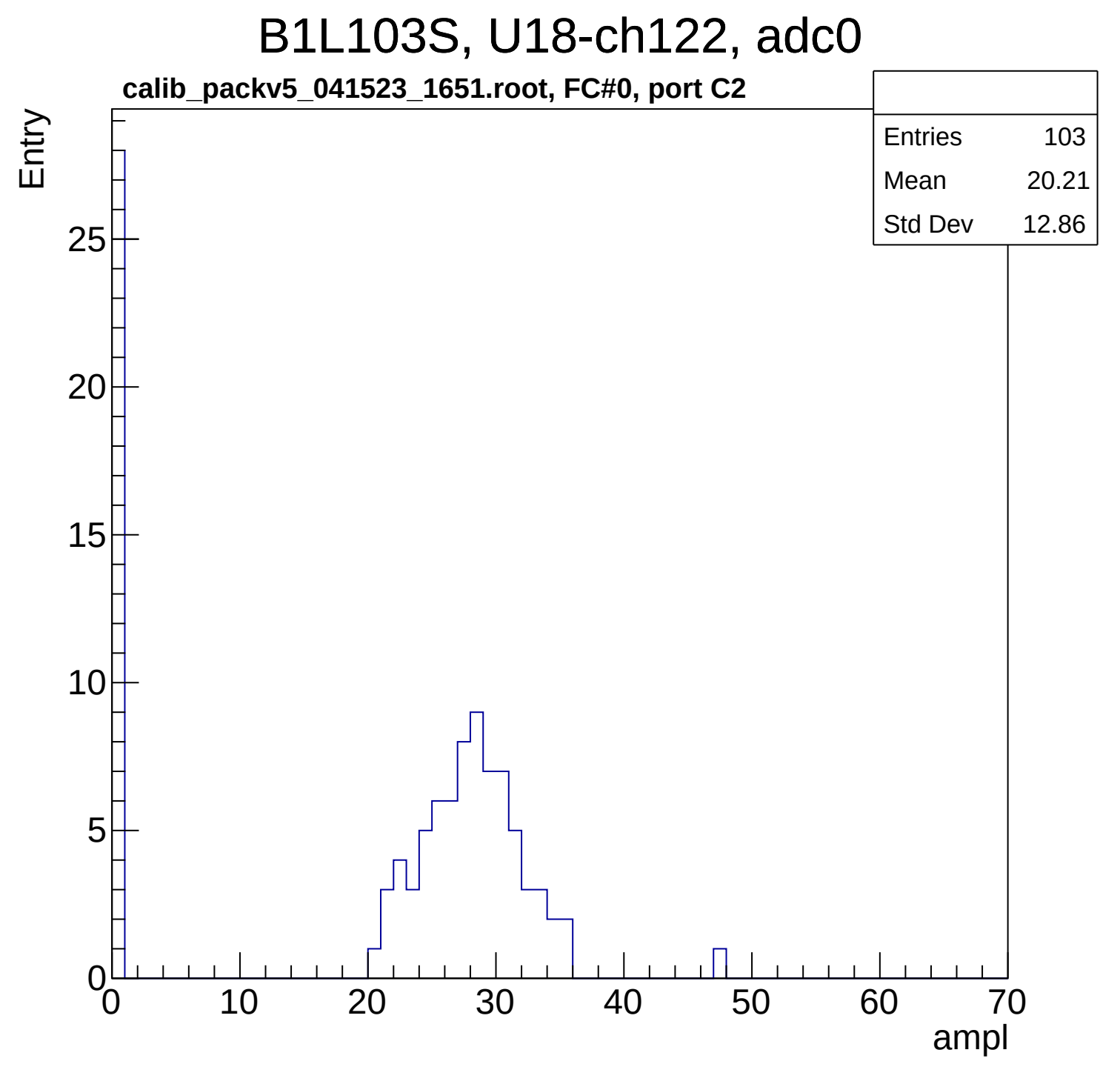
20
30
40
50
60
70
ampl


B1L103S, U18-ch122, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 103
Mean 20.21
Std Dev 12.86
Entry
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10
15
20
25
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30
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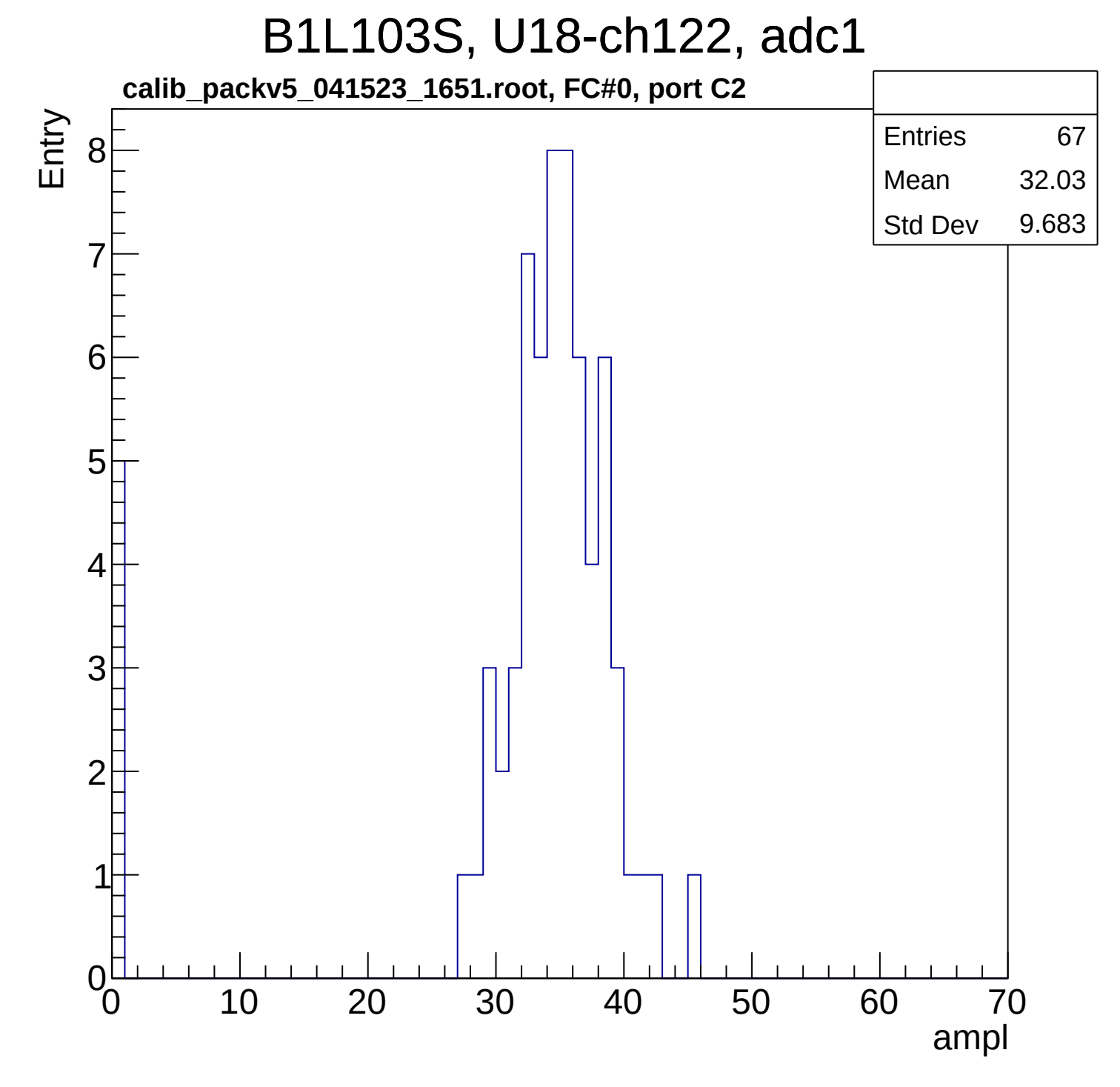
50
60
70
ampl


B1L103S, U18-ch122, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 32.03
Std Dev 9.683
Entry
ampl
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2
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4
5
6
7
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0
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20
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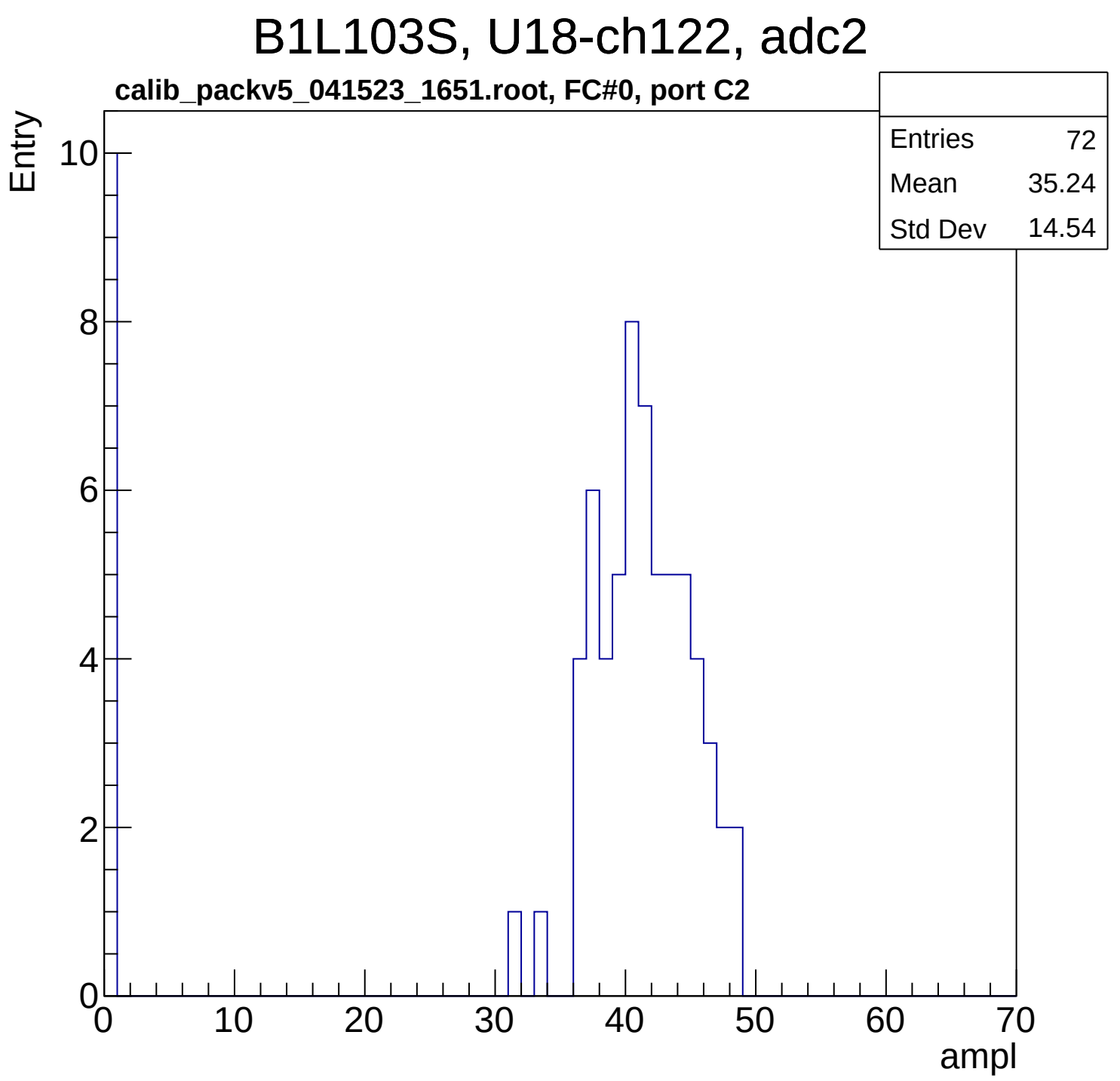
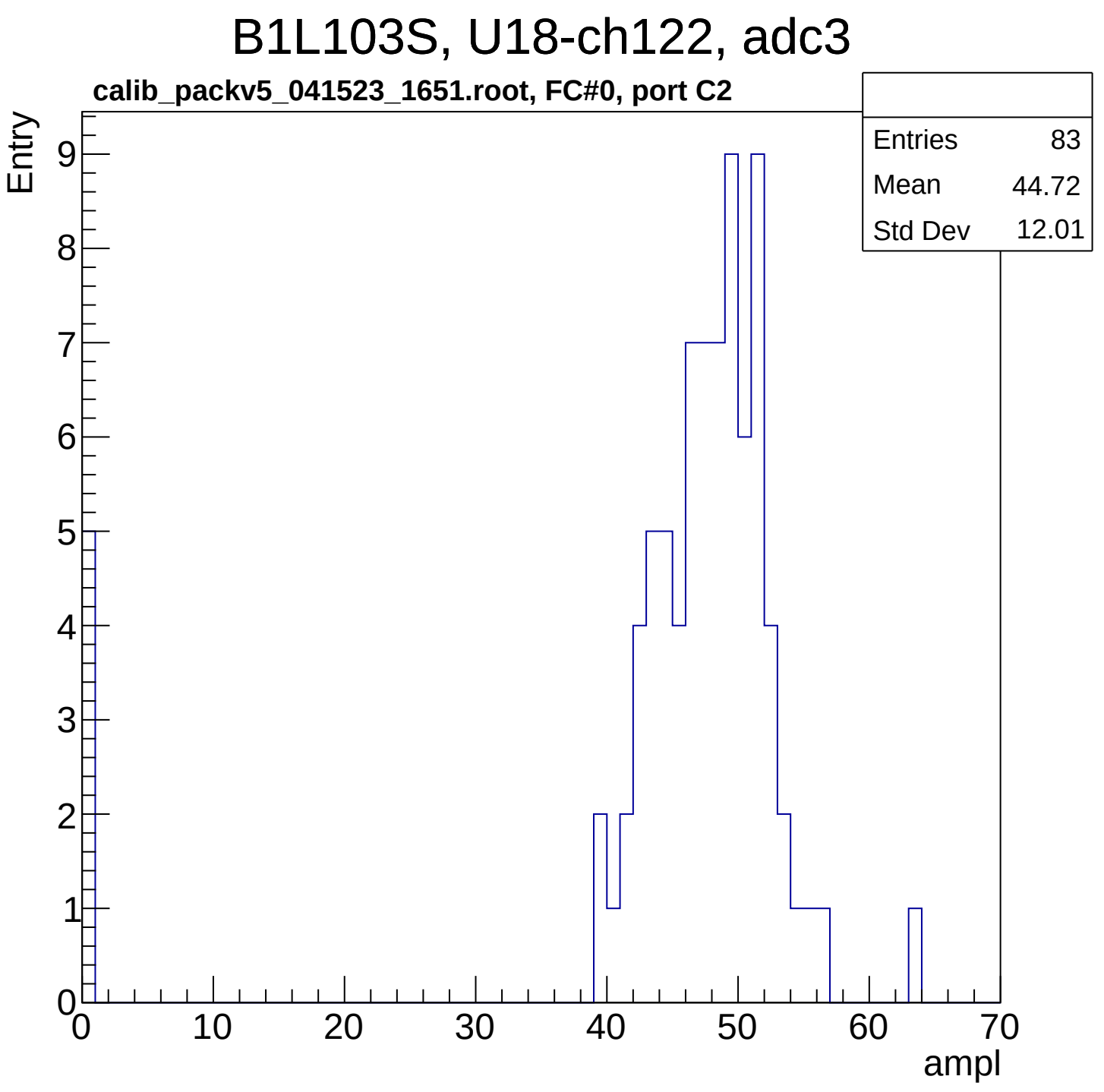
50
60
70


B1L103S, U18-ch122, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 35.24
Std Dev 14.54
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U18-ch122, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 44.72
Std Dev 12.01
Entry
ampl
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2
3
4
5
6
7
8
9
0
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60
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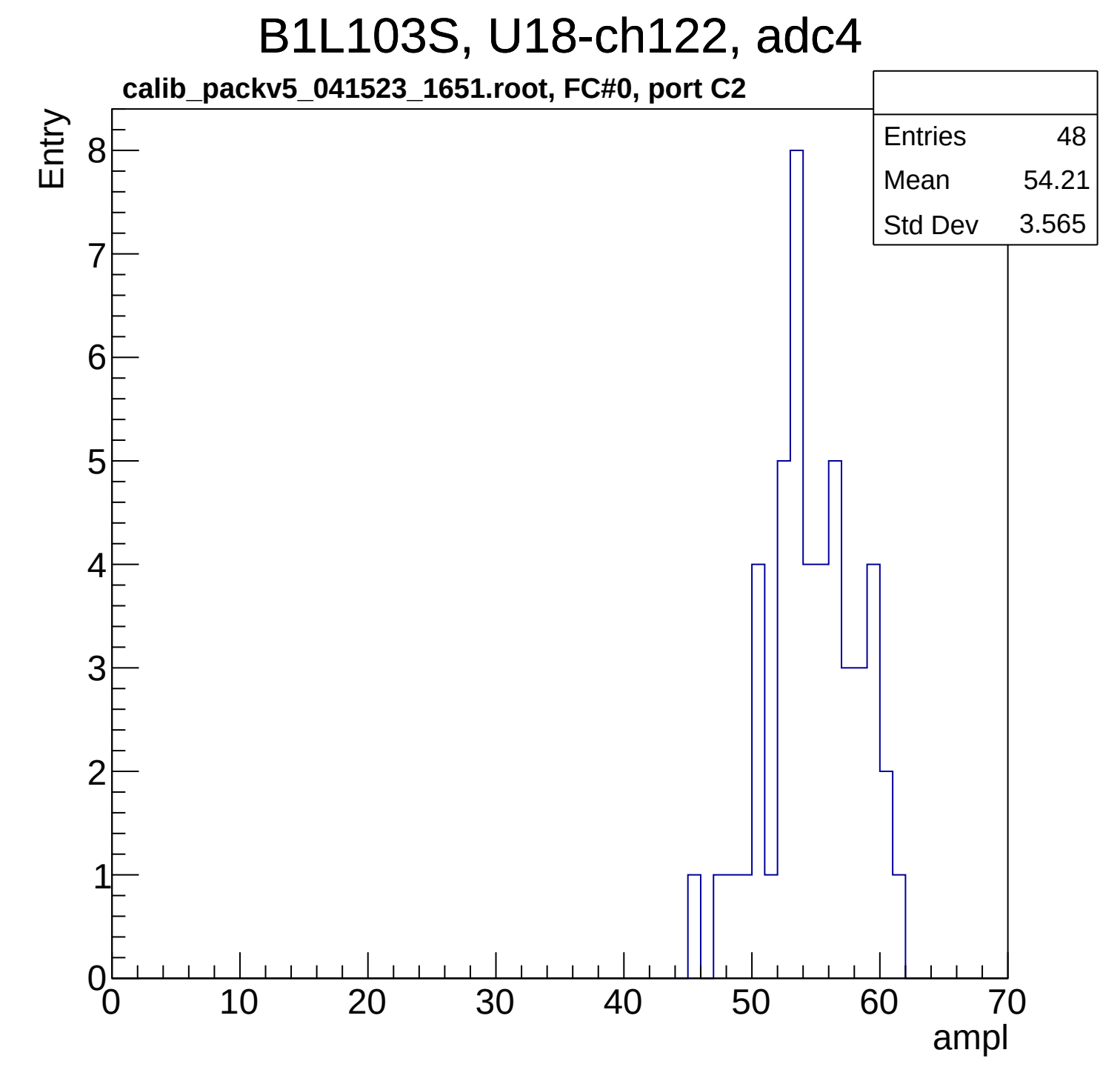
B1L103S, U18-ch122, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 54.21
Std Dev 3.565
Entry
ampl
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2
3
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5
6
7
8
0
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20
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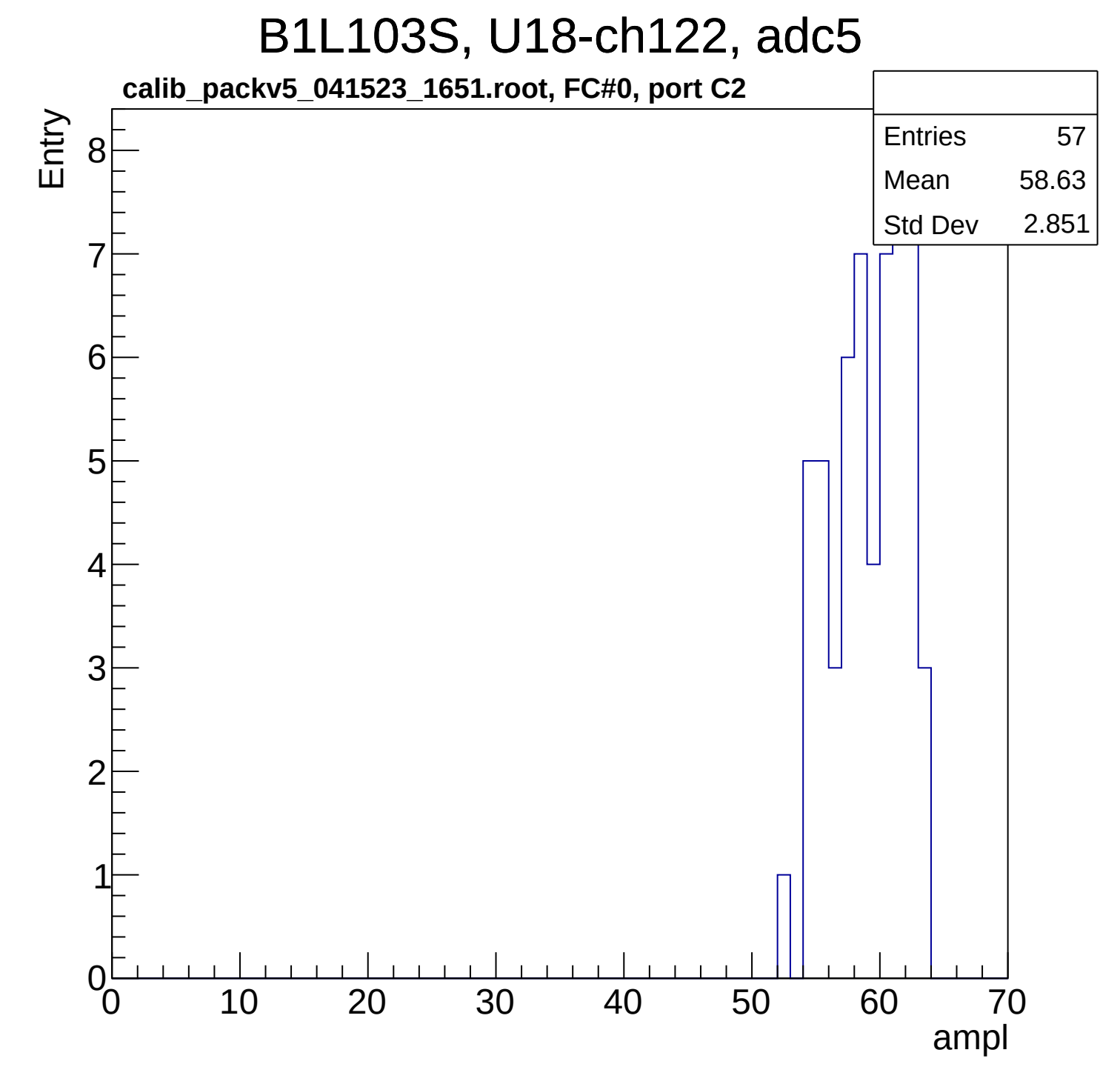
40
50
60
70


B1L103S, U18-ch122, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 58.63
Std Dev 2.851
Entry
ampl
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2
3
4
5
6
7
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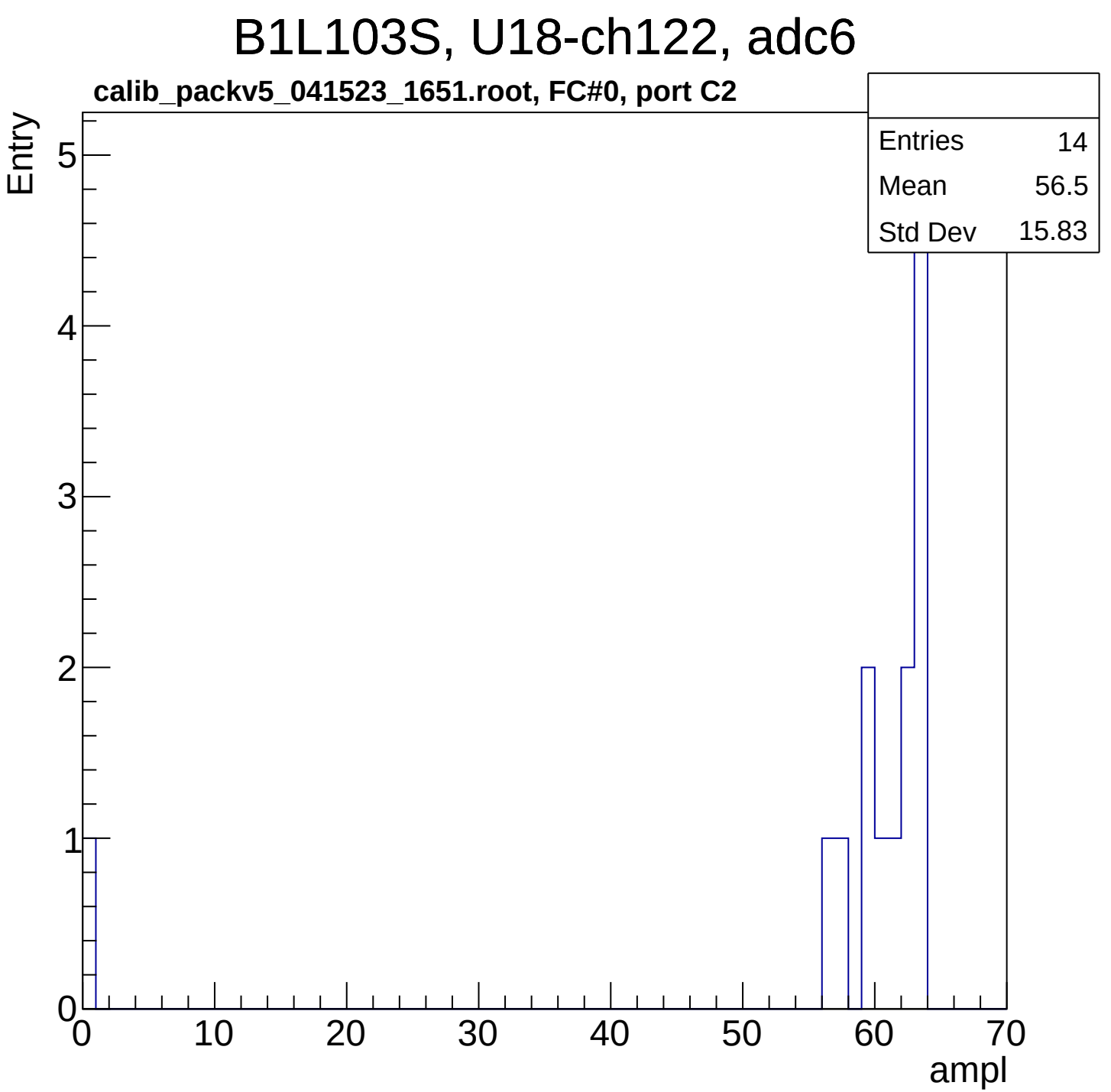
0
10
20
30
40
50
60
70


B1L103S, U18-ch122, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 14
Mean 56.5
Std Dev 15.83
Entry
0
1
2
3
4
5
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10
20
30
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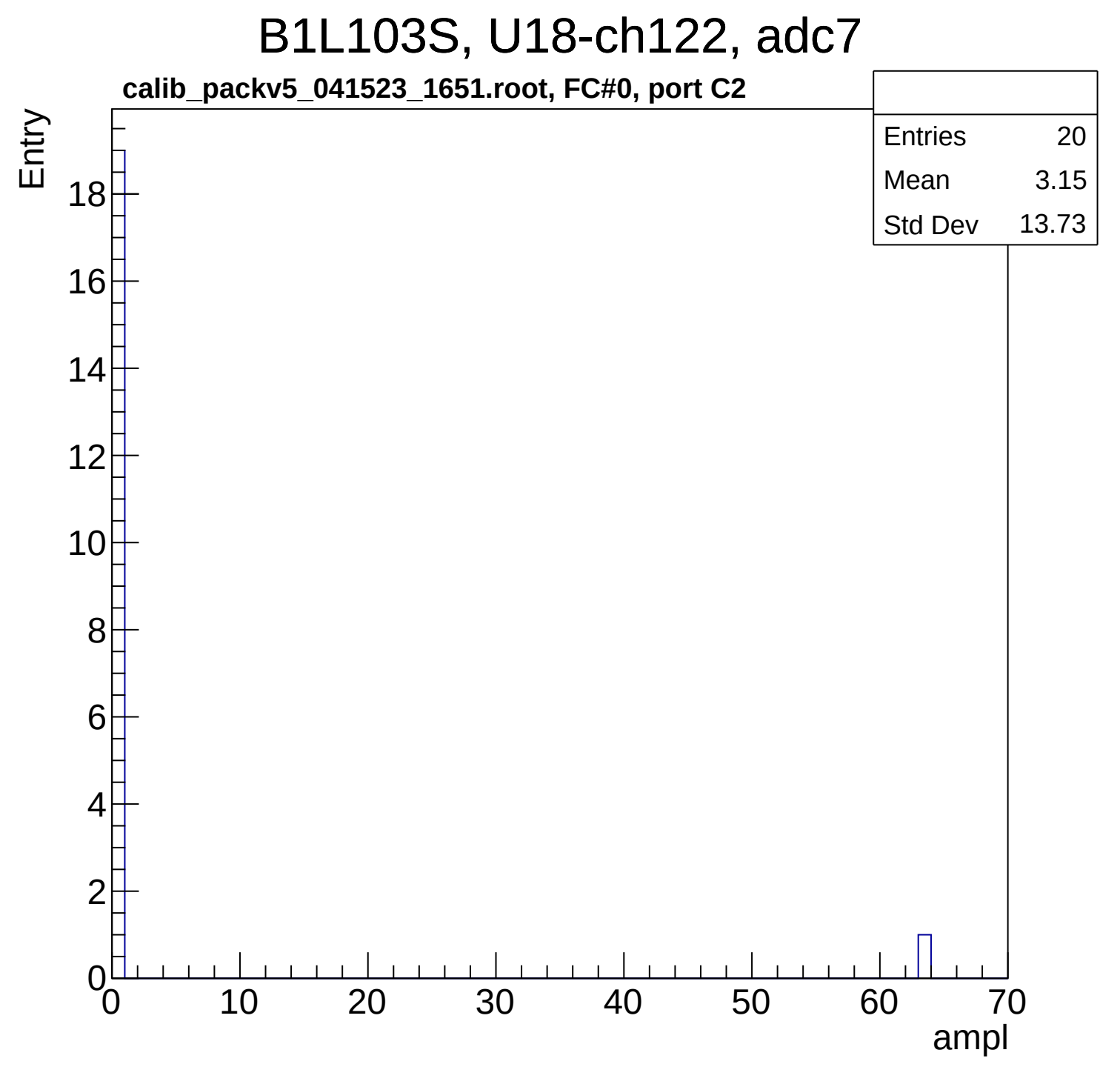
60
70
ampl


B1L103S, U18-ch122, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
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6
8
10
12
14
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18
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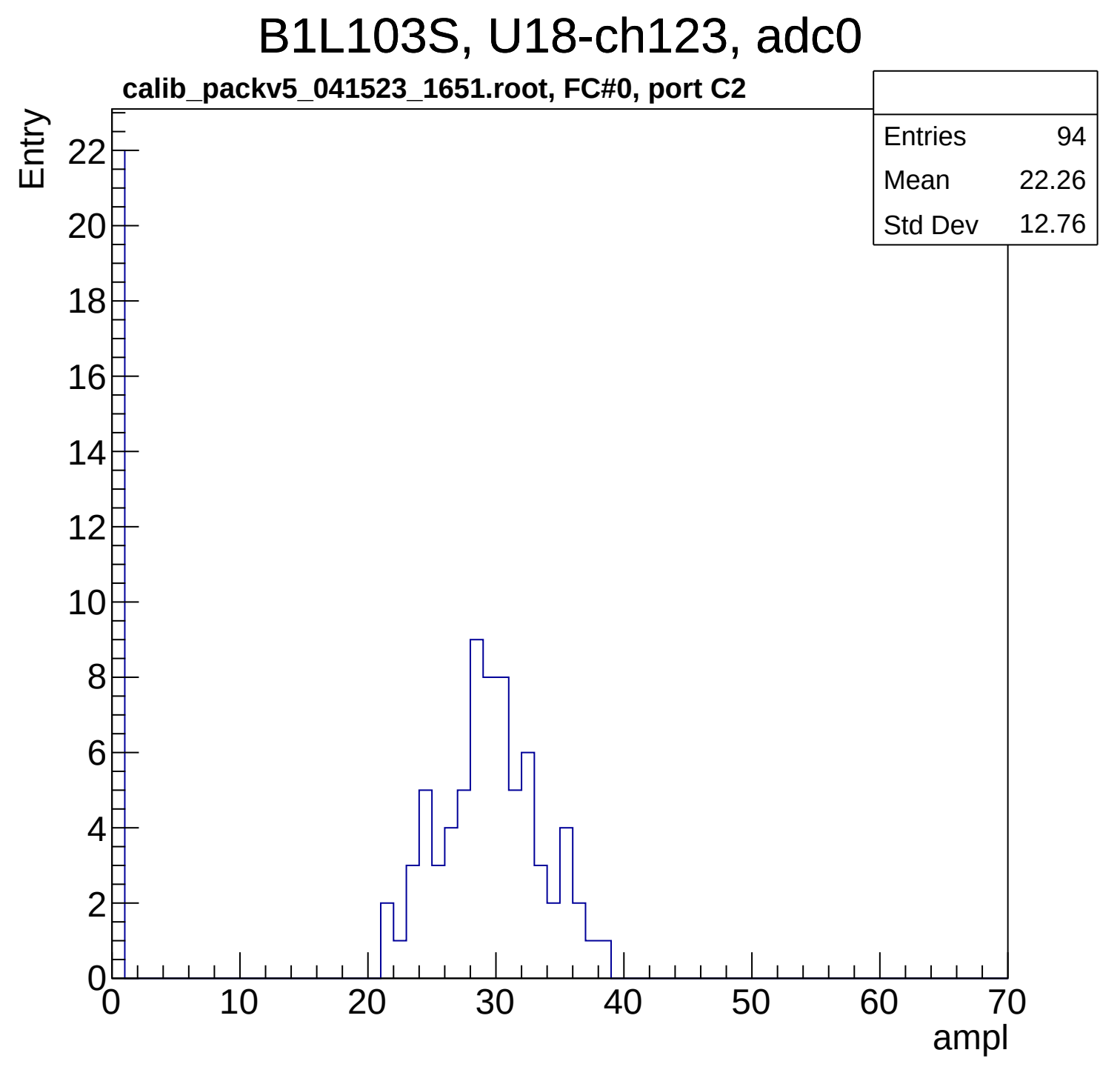
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch123, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 94
Mean 22.26
Std Dev 12.76
Entry
ampl
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2
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8
10
12
14
16
18
20
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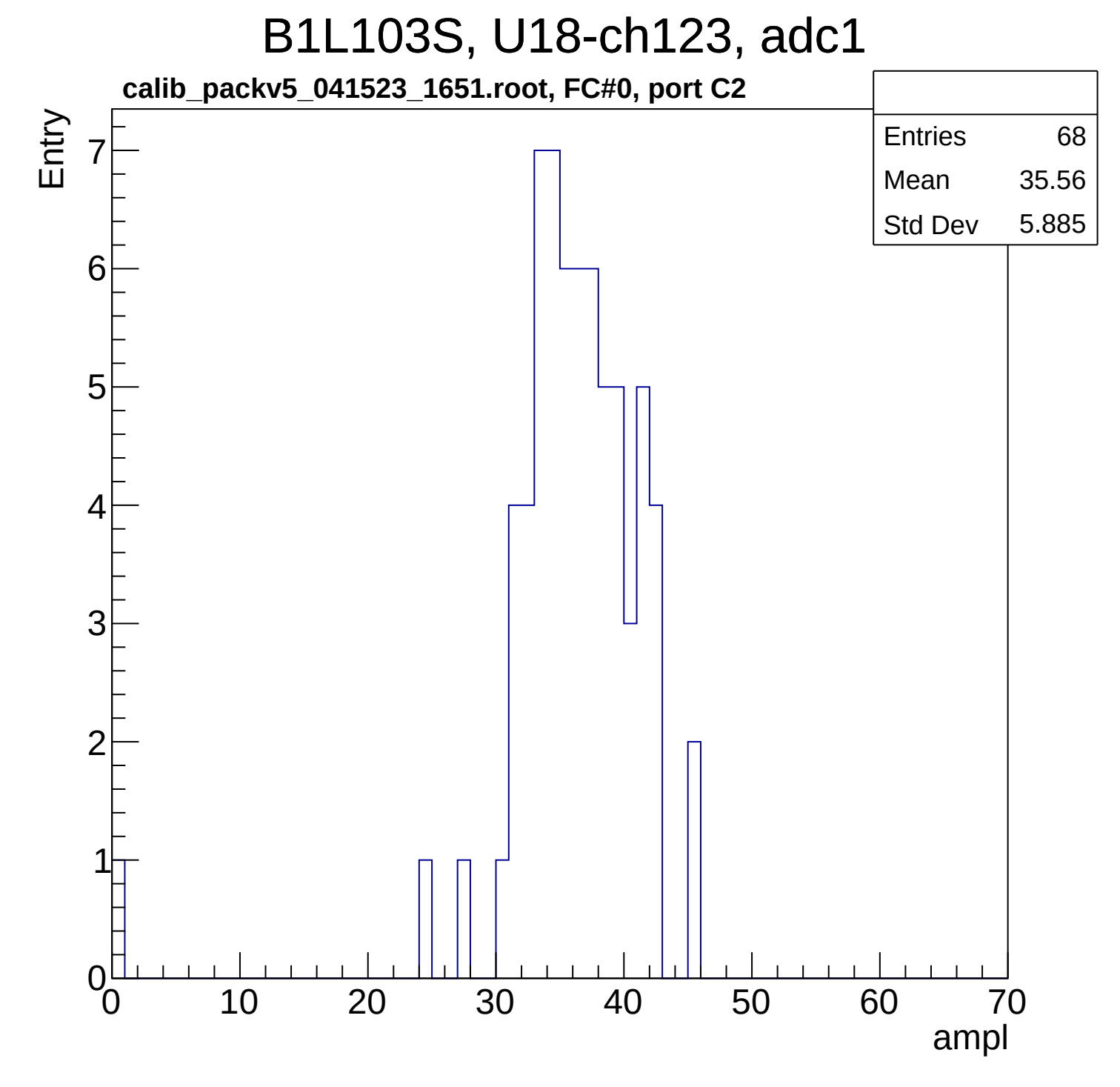
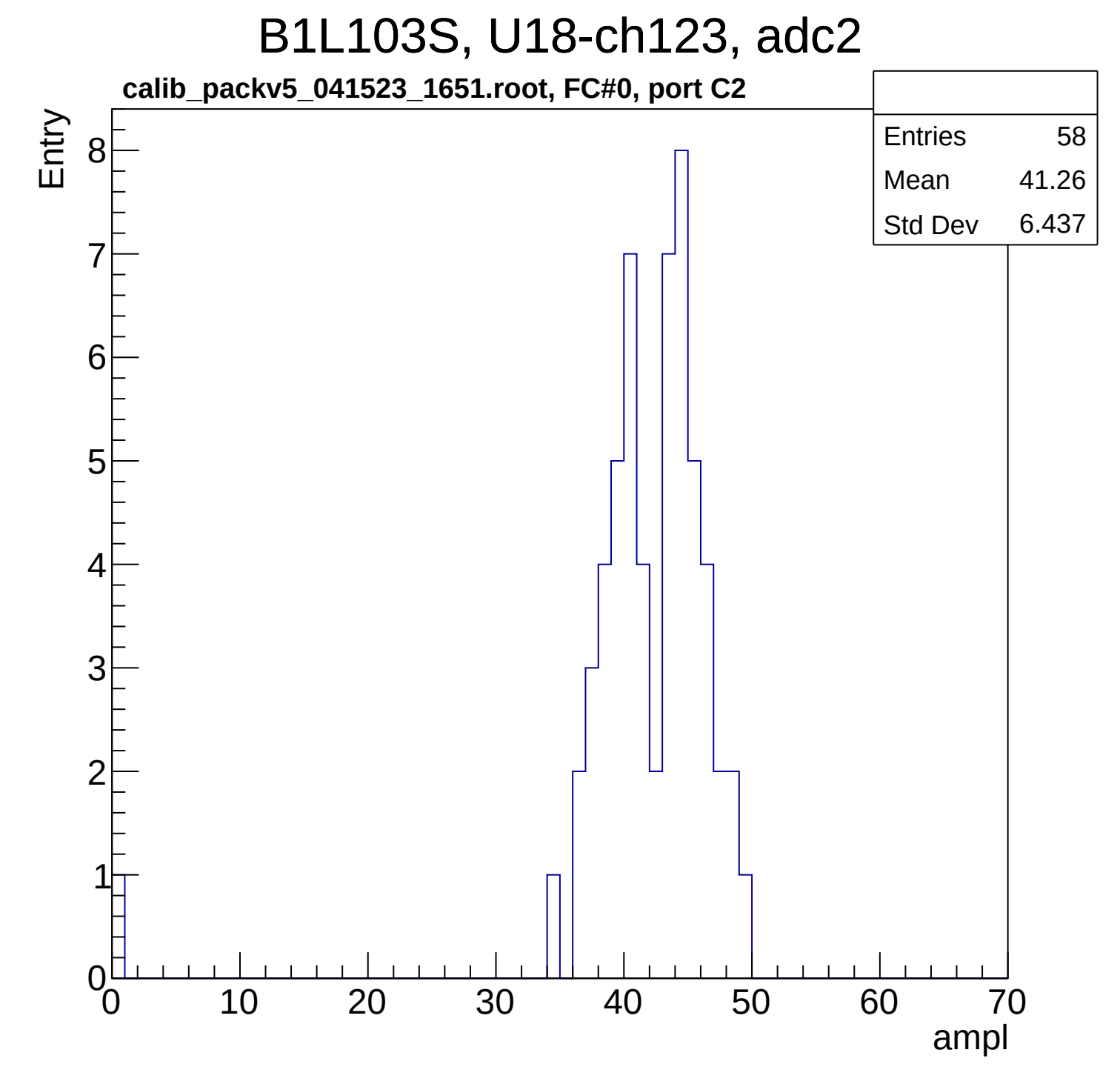
40
50
60
70


B1L103S, U18-ch123, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 35.56
Std Dev 5.885
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U18-ch123, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 41.26
Std Dev 6.437
Entry
ampl
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1
2
3
4
5
6
7
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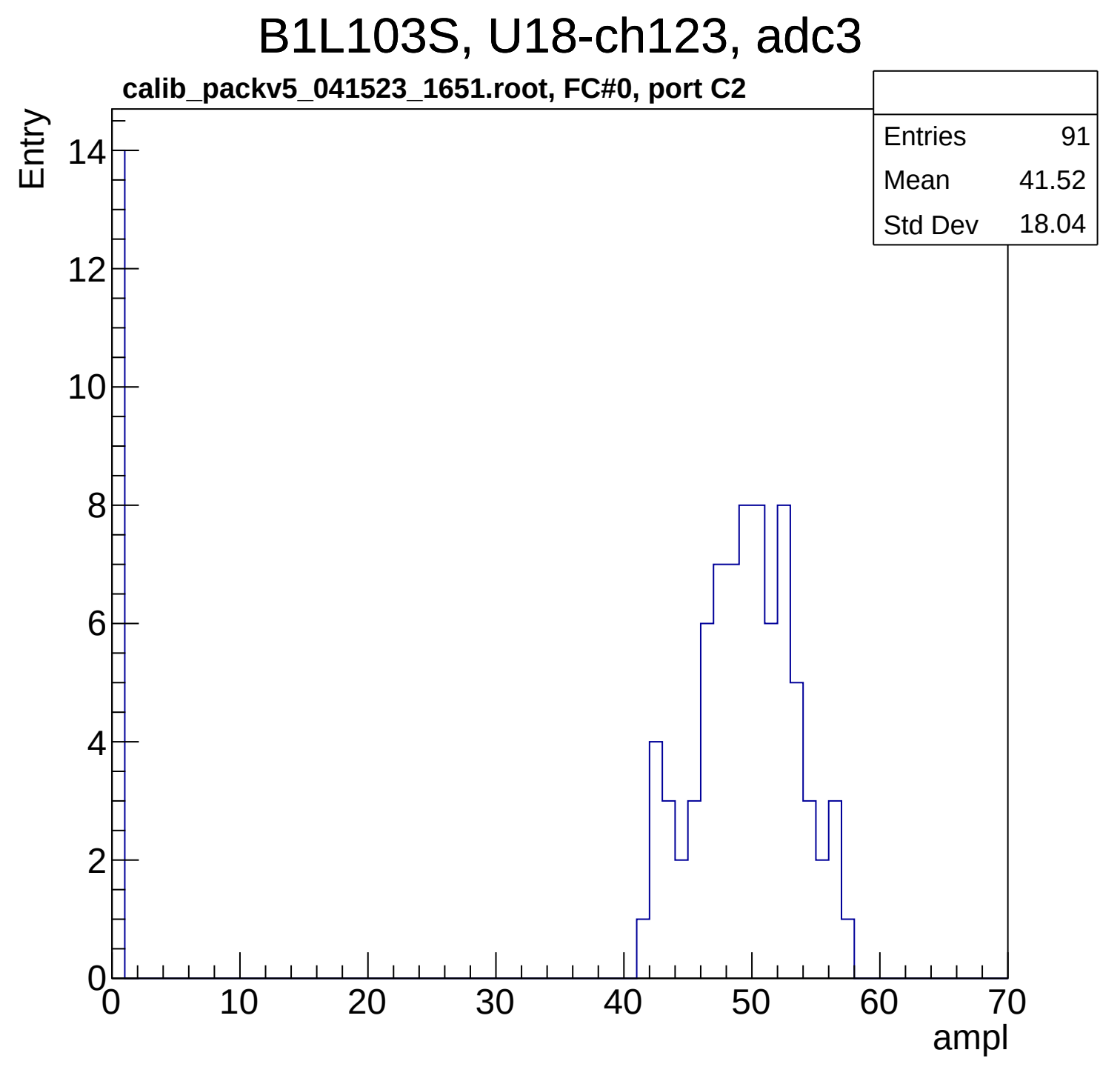
0
10
20
30
40
50
60
70


B1L103S, U18-ch123, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 91
Mean 41.52
Std Dev 18.04
Entry
ampl
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2
4
6
8
10
12
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0
10
20
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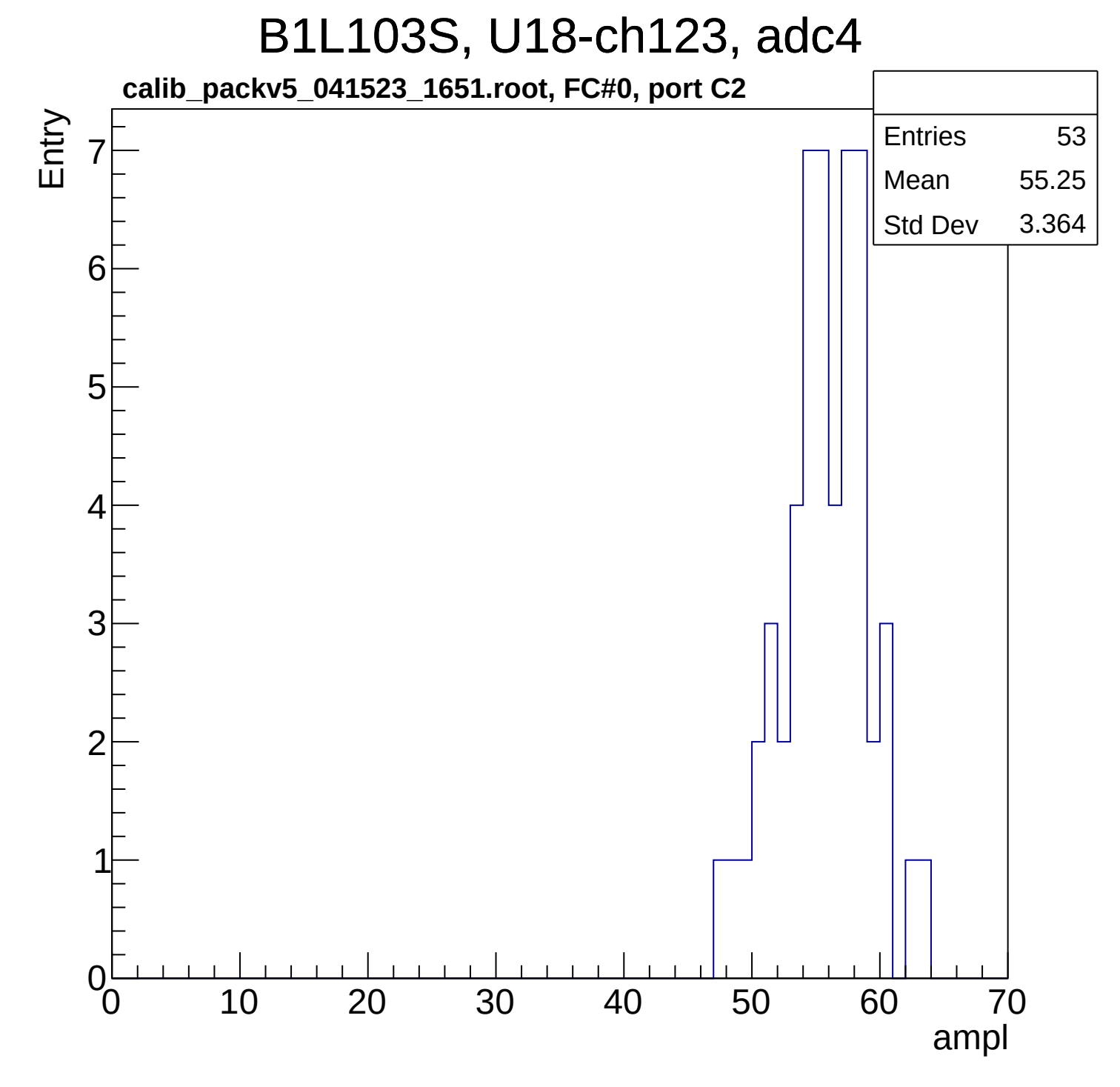
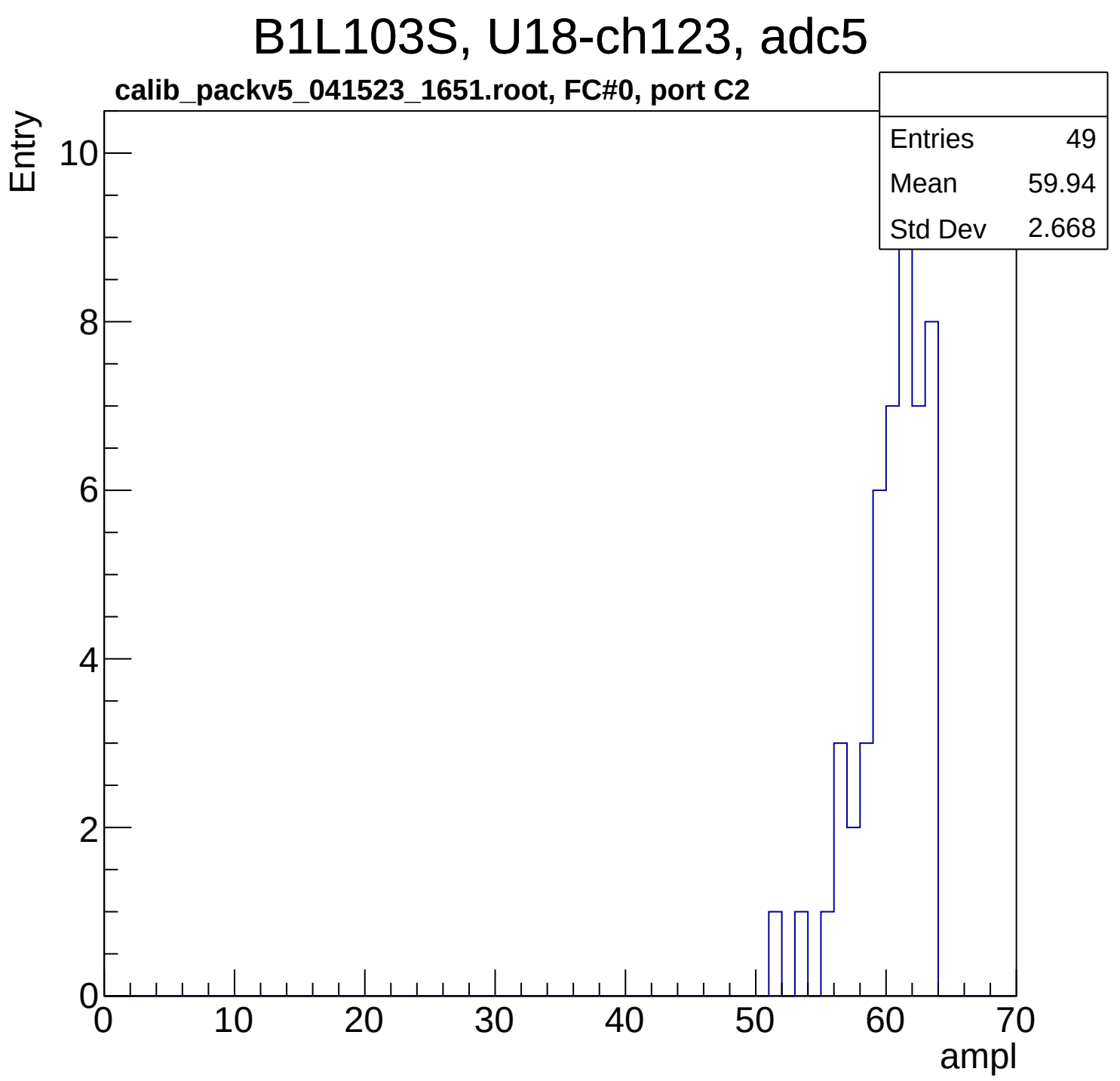
40
50
60
70


B1L103S, U18-ch123, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 55.25
Std Dev 3.364
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U18-ch123, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 59.94
Std Dev 2.668
Entry
ampl
0
2
4
6
8
10
0
10
20
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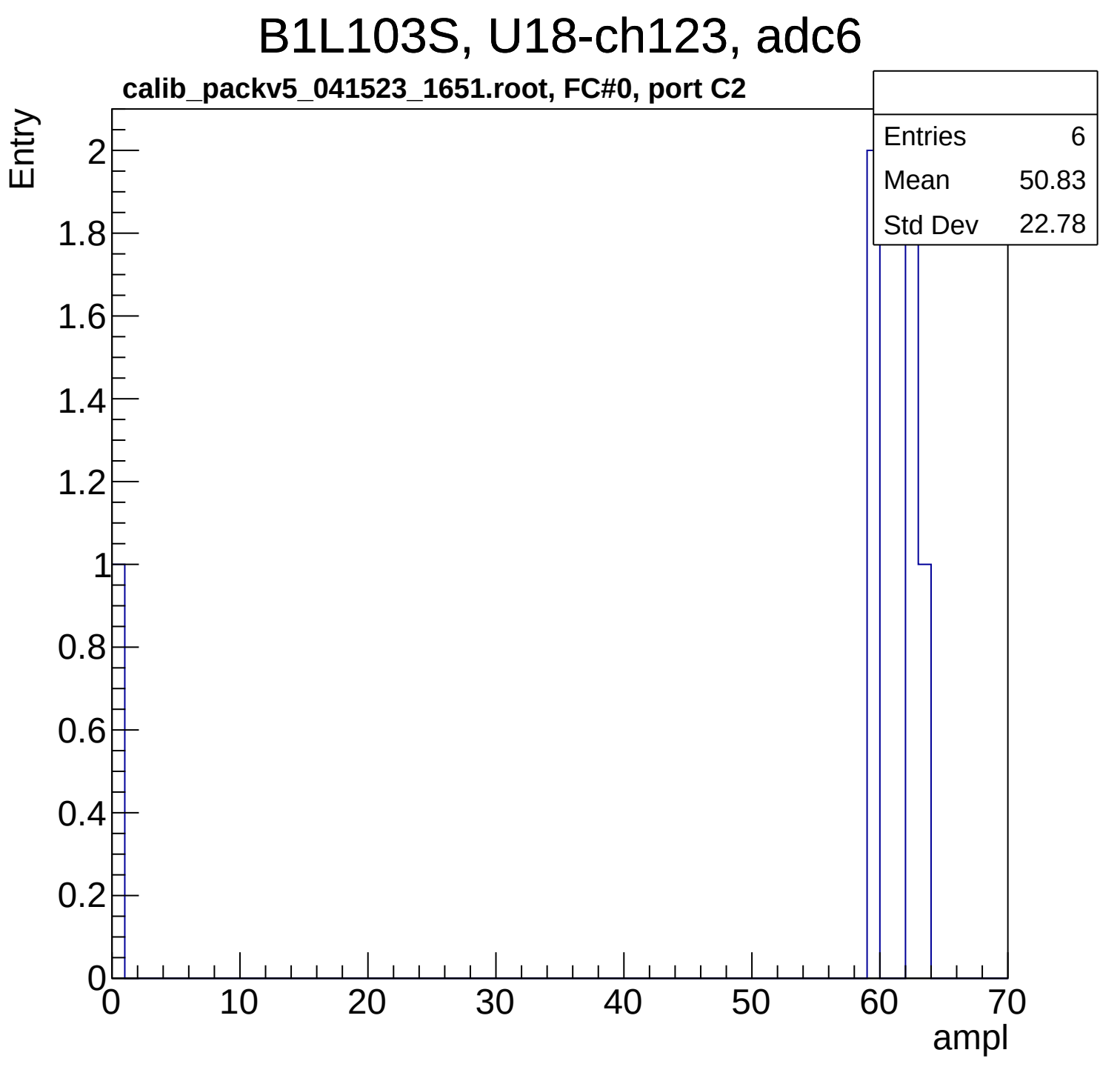
40
50
60
70


B1L103S, U18-ch123, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 50.83
Std Dev 22.78
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
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40
50
60
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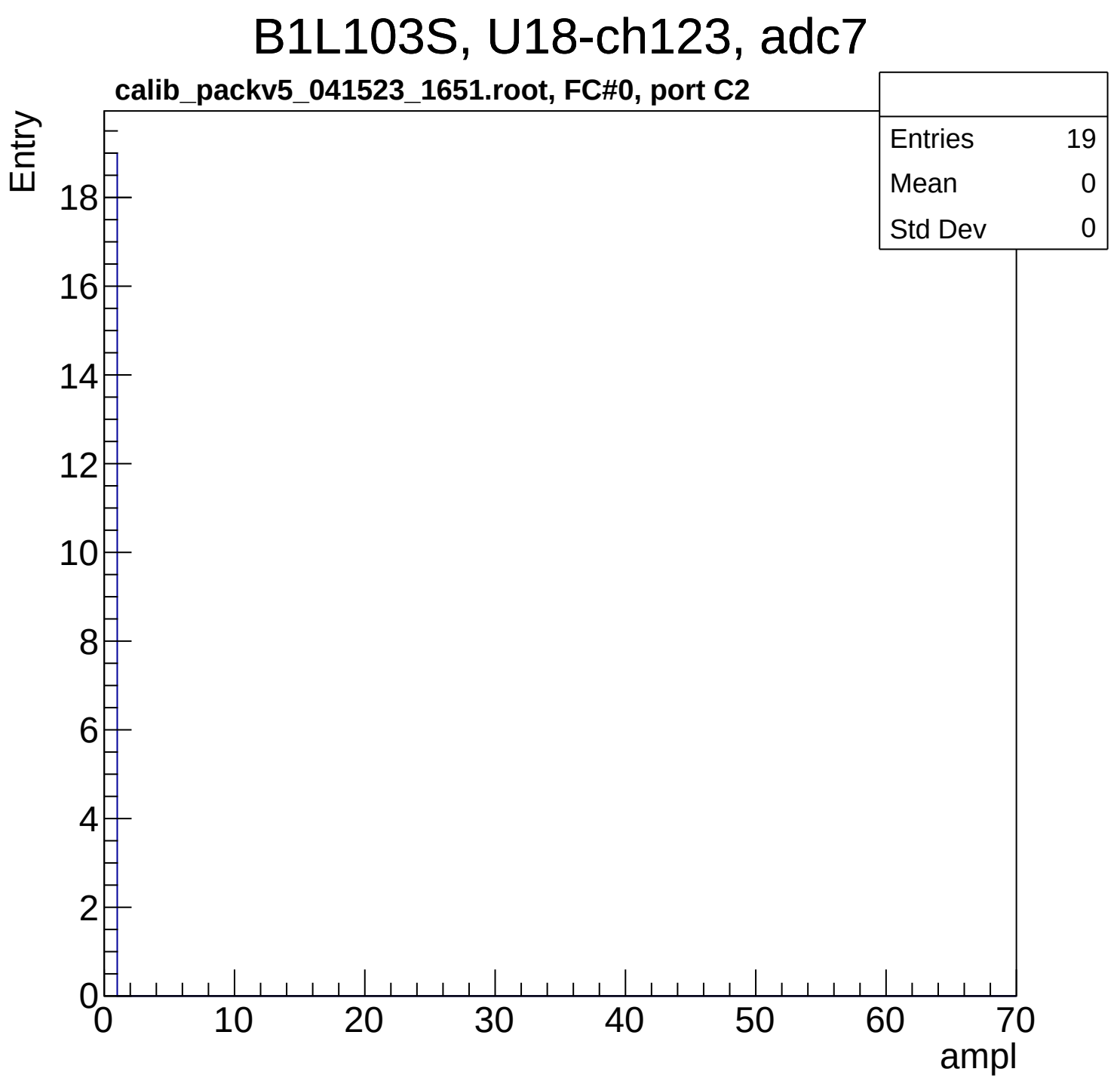
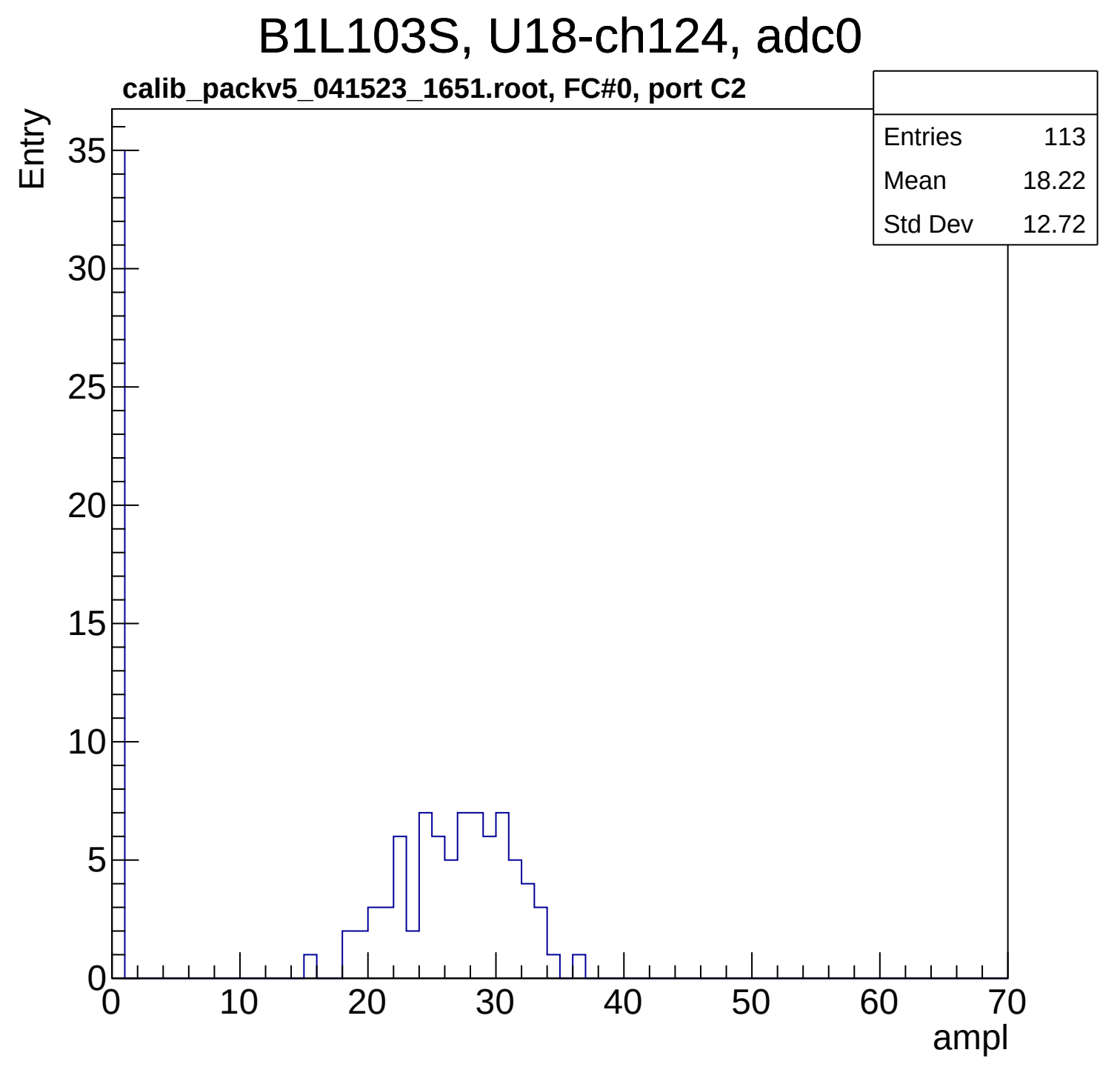
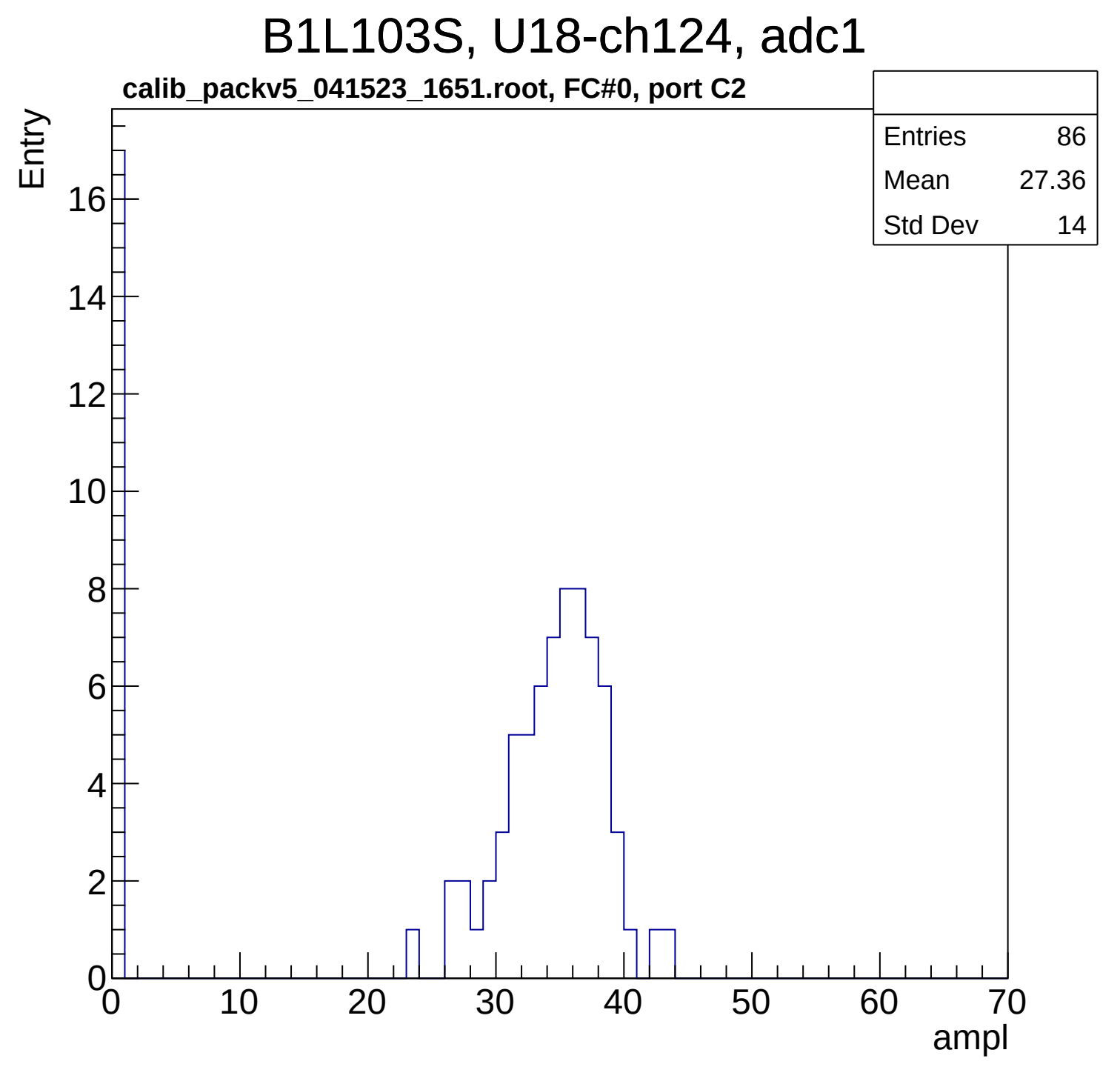

B1L103S, U18-ch123, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch124, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 113
Mean 18.22
Std Dev 12.72
Entry
ampl
0
5
10
15
20
25
30
35
0
10
20
30
40
50
60
70


B1L103S, U18-ch124, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 27.36
Std Dev 14
Entry
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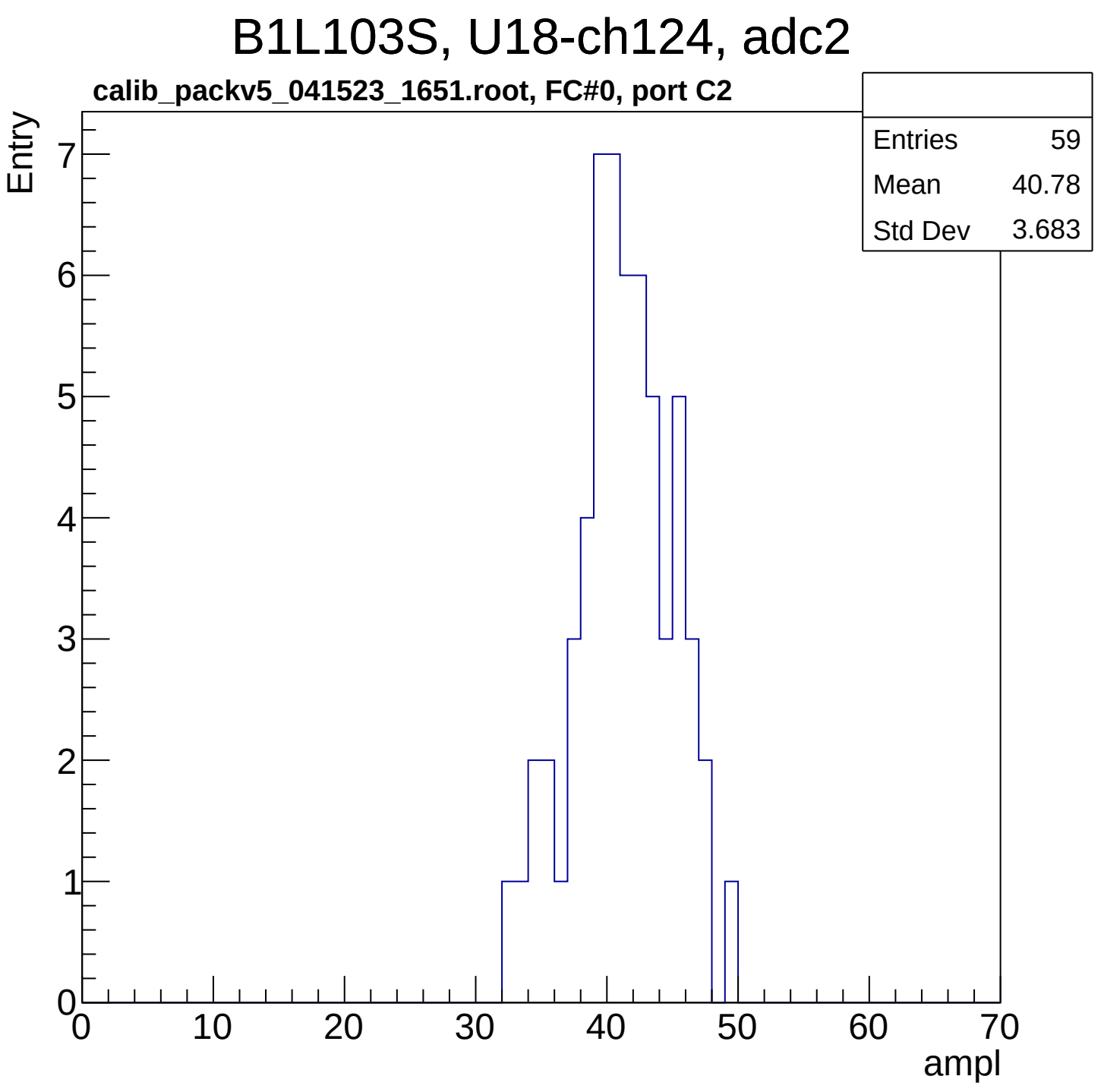
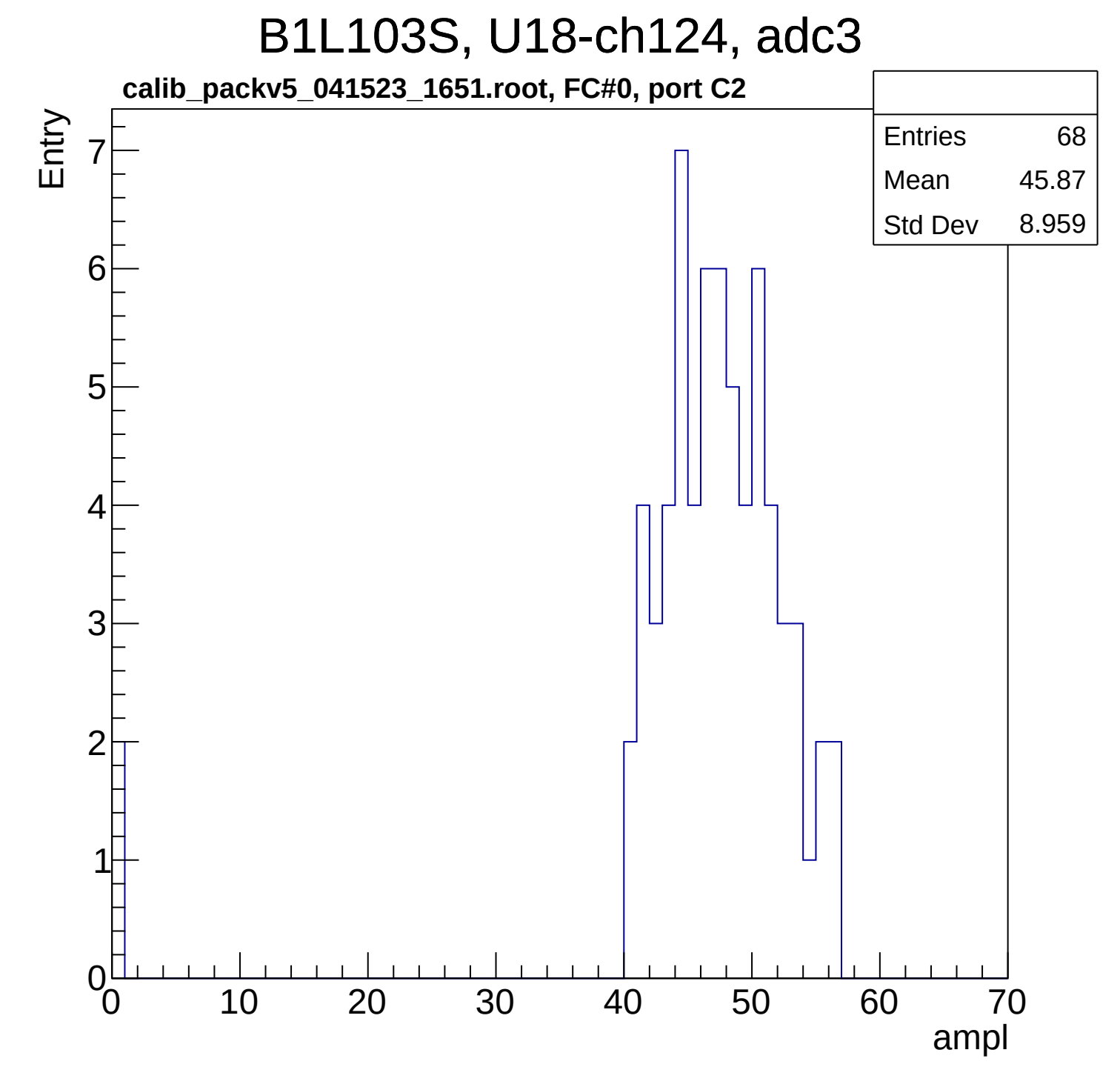
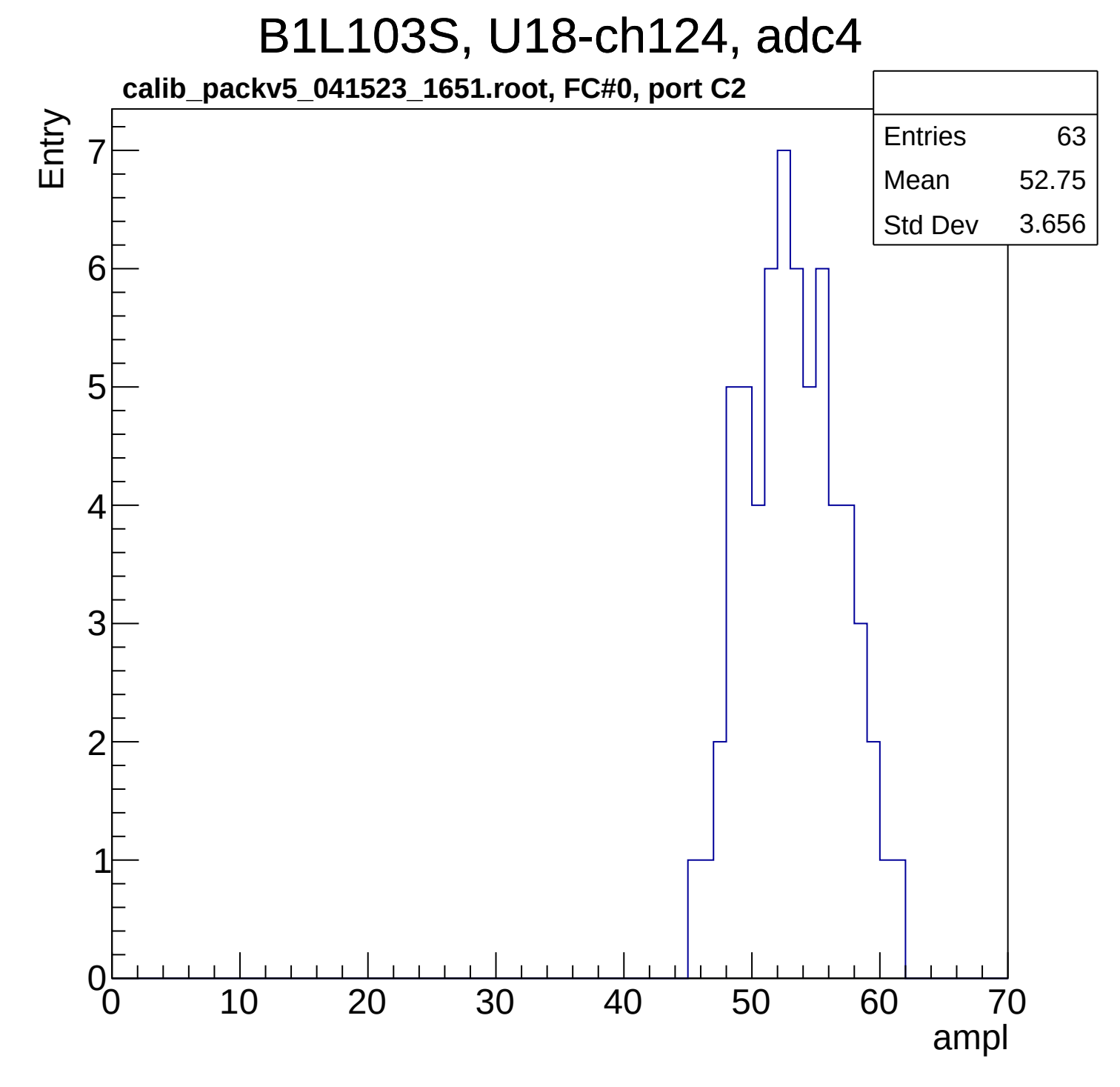
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch124, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 40.78
Std Dev 3.683
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U18-ch124, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 45.87
Std Dev 8.959
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U18-ch124, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 52.75
Std Dev 3.656
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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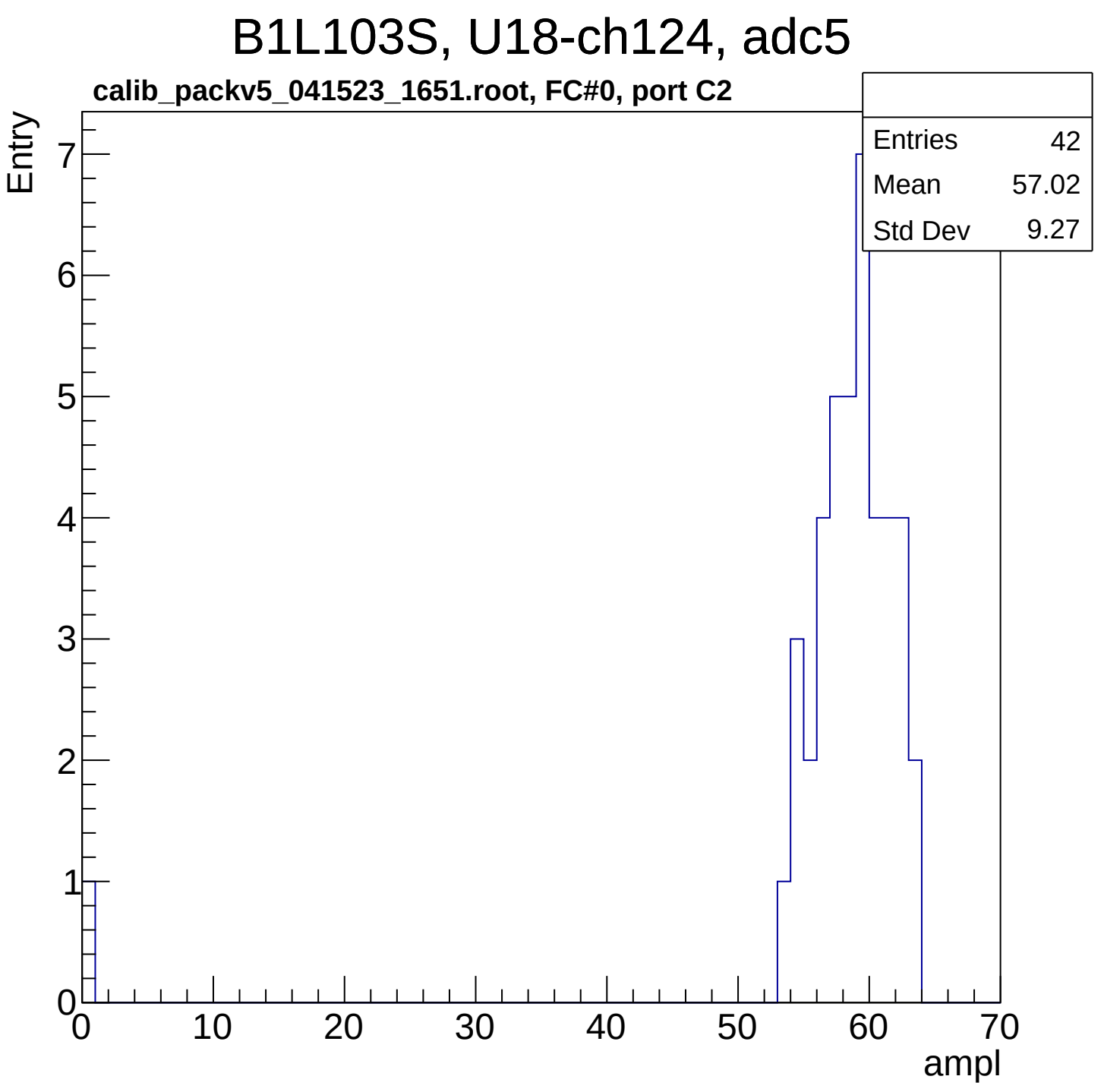
B1L103S, U18-ch124, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 42
Mean 57.02
Std Dev 9.27
Entry
ampl
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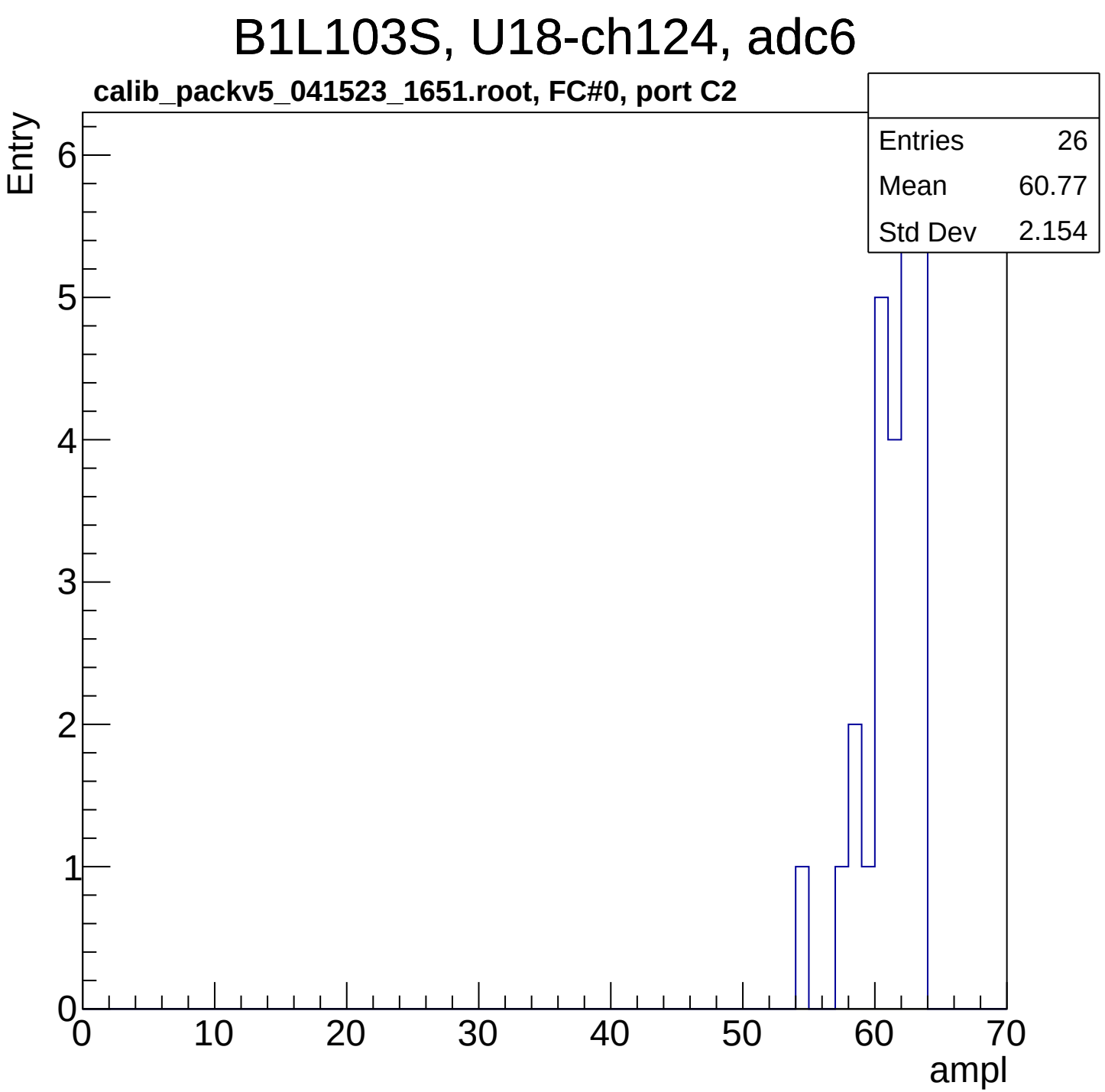
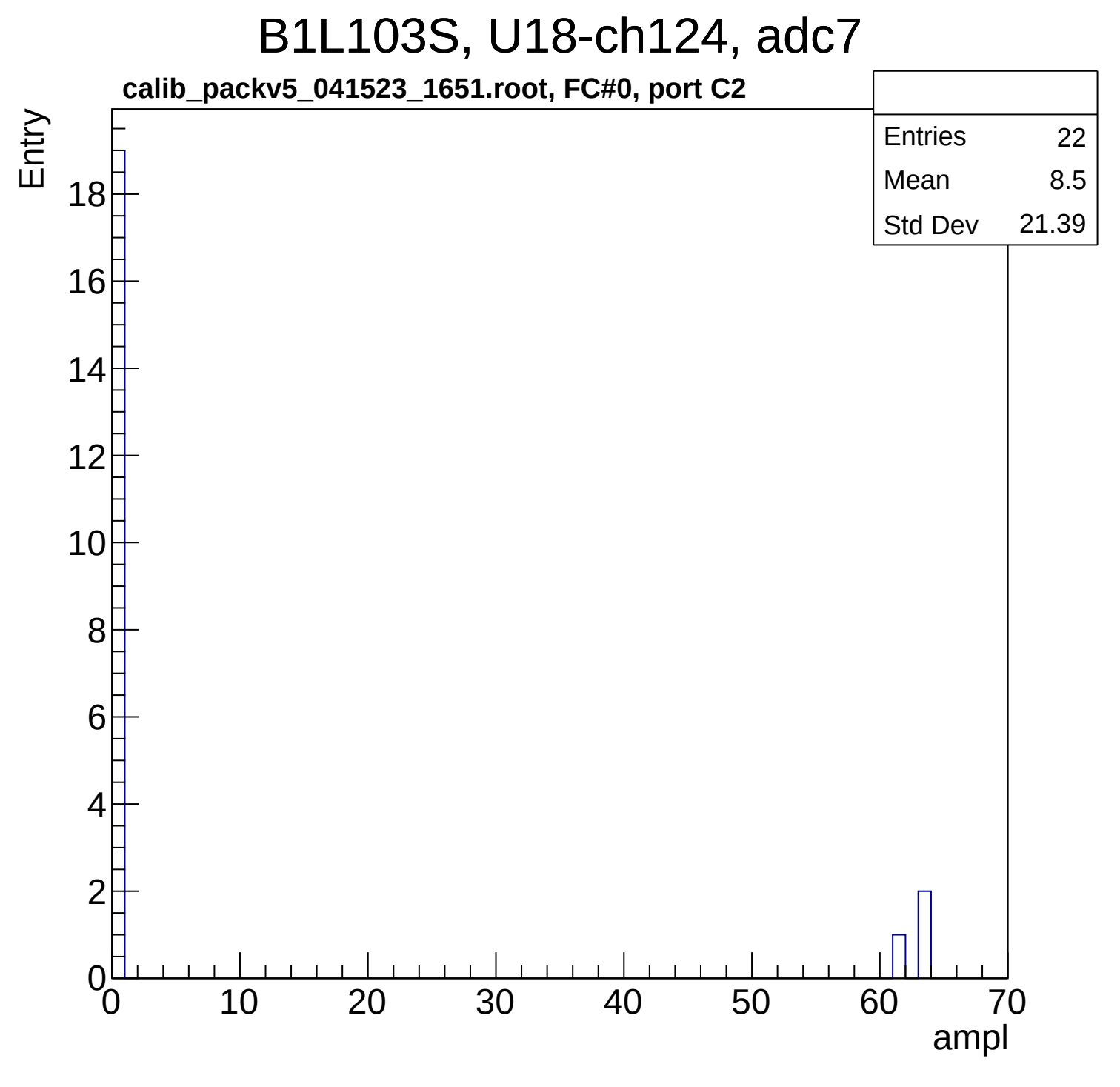
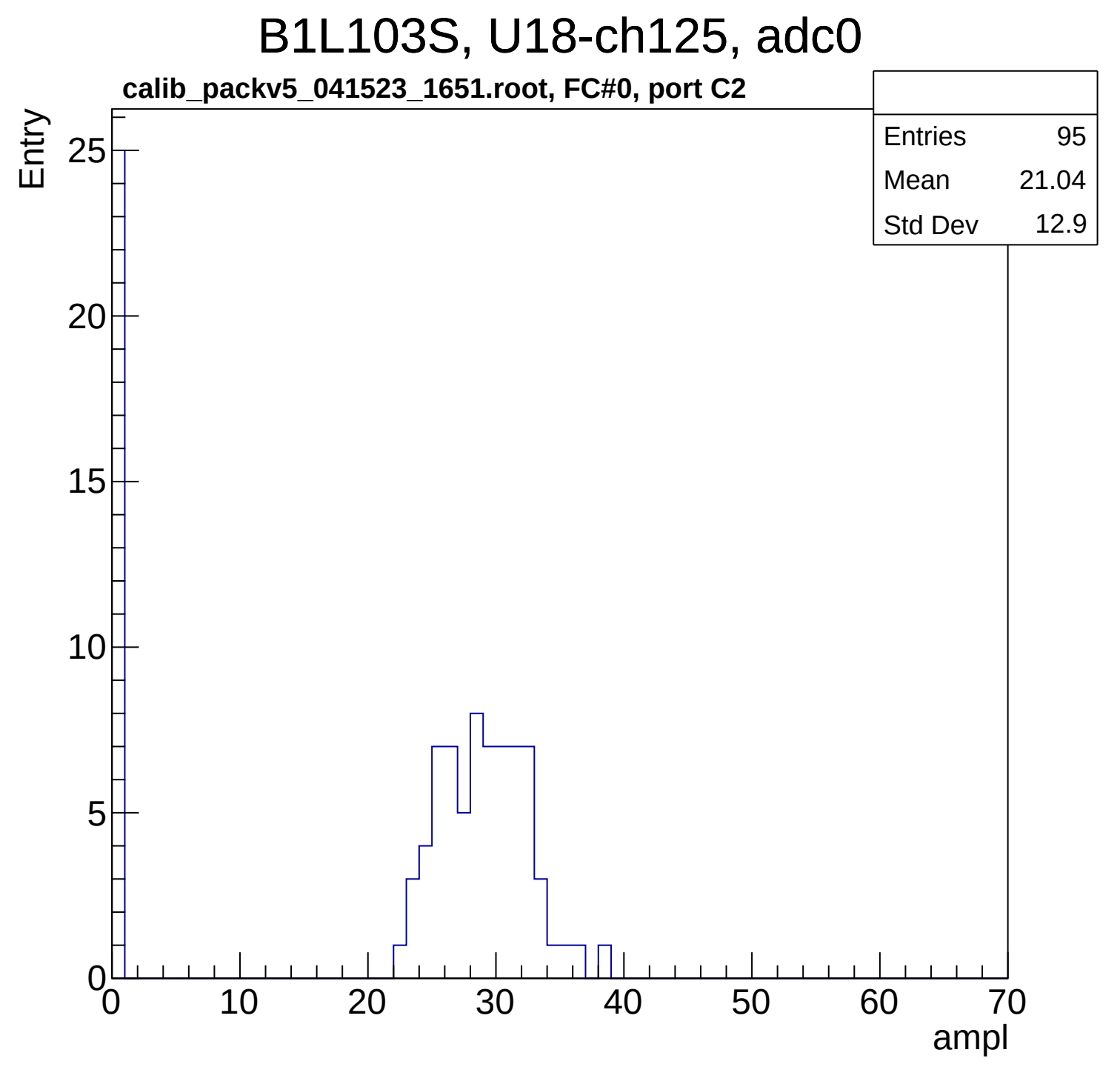
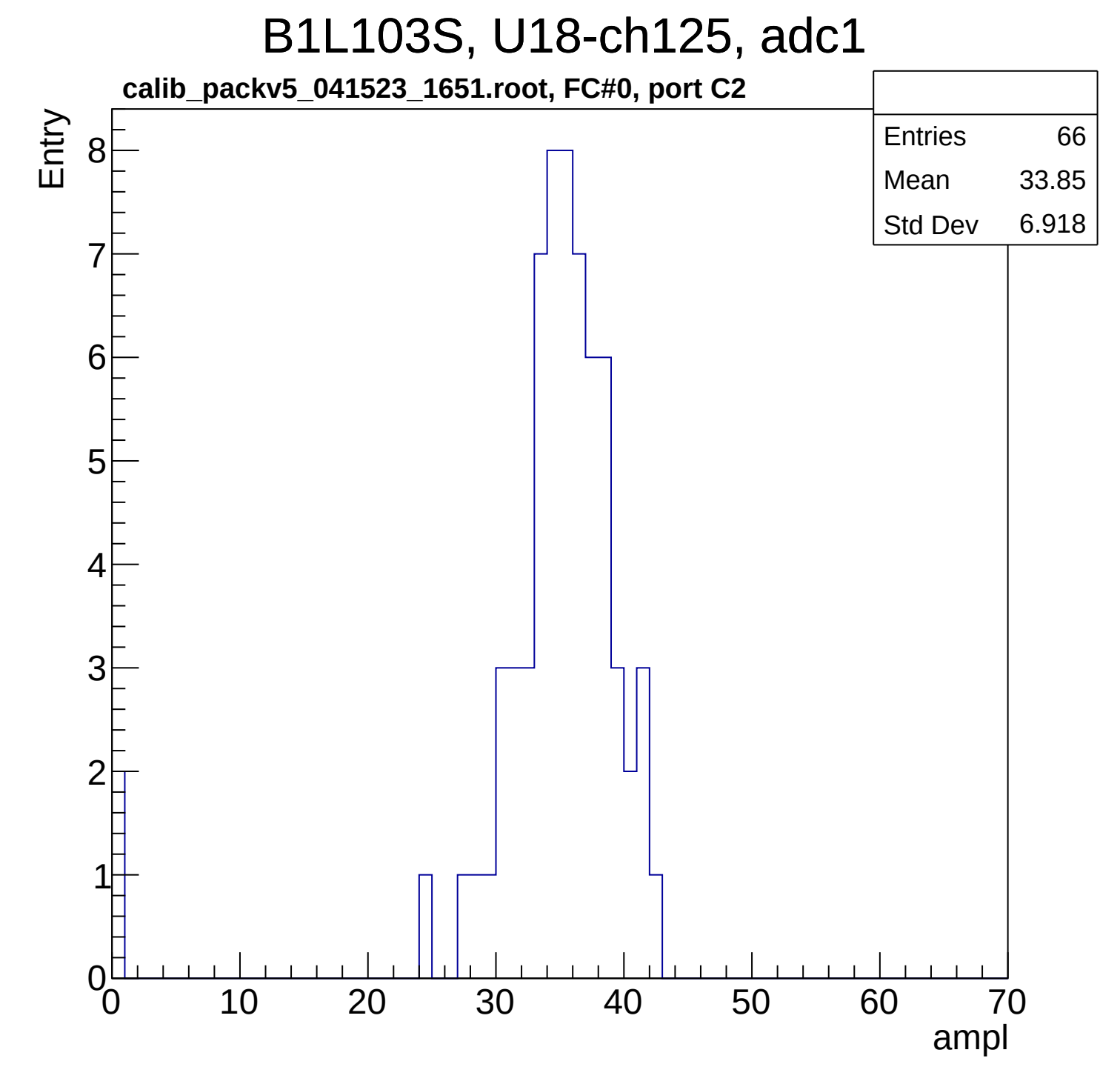
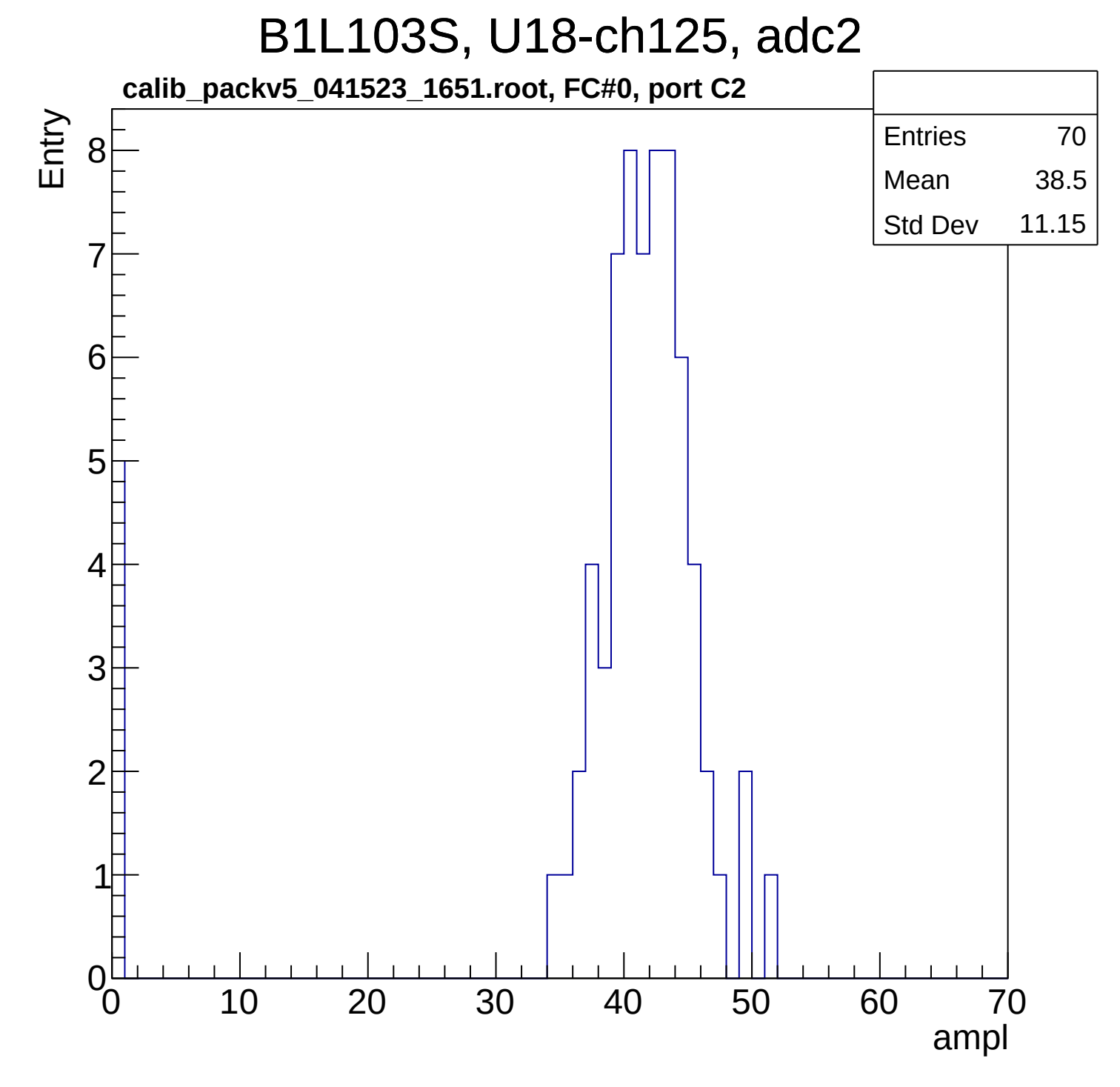
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

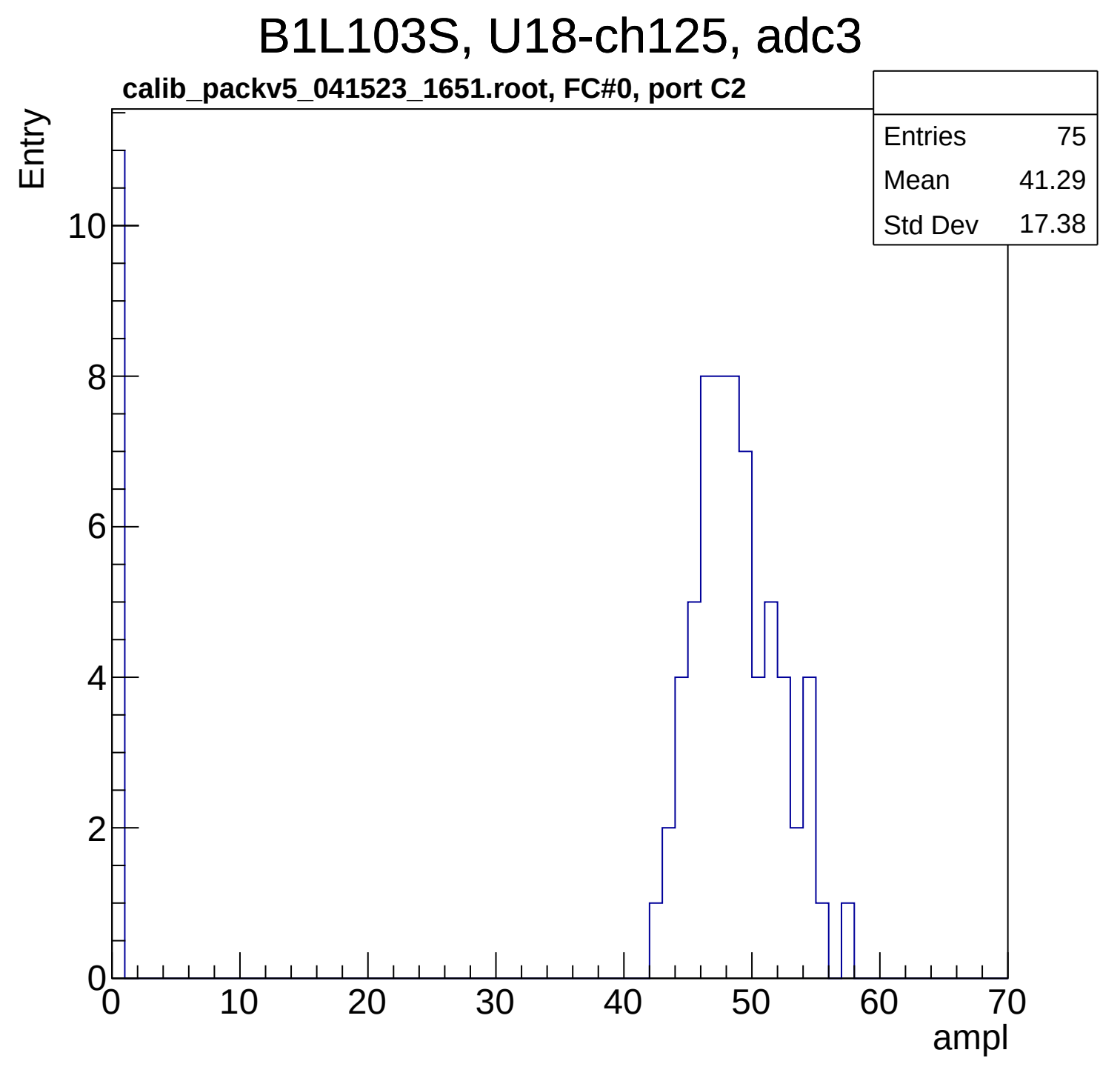

B1L103S, U18-ch124, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 26
Mean 60.77
Std Dev 2.154
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

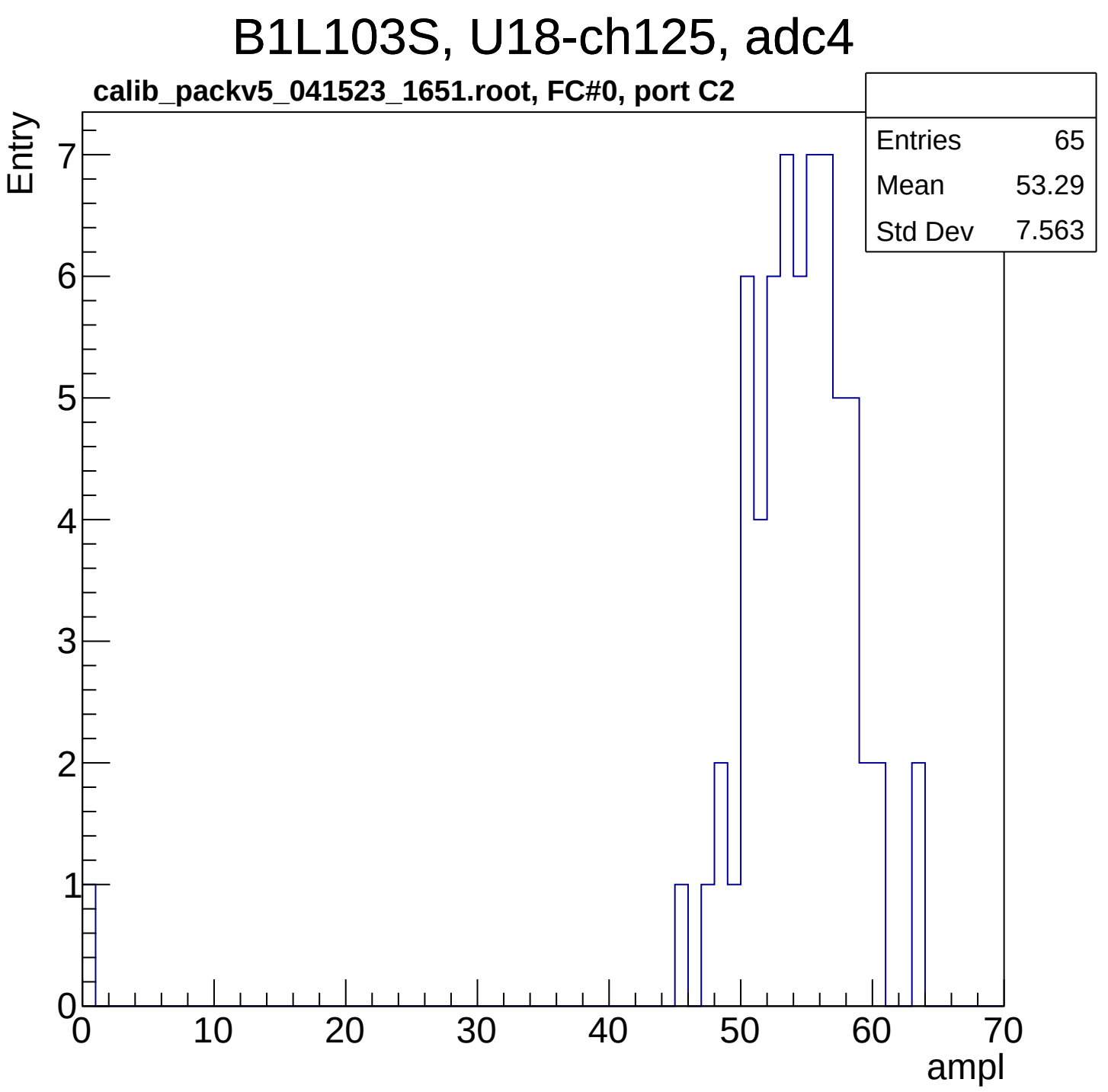

B1L103S, U18-ch124, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 8.5
Std Dev 21.39
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

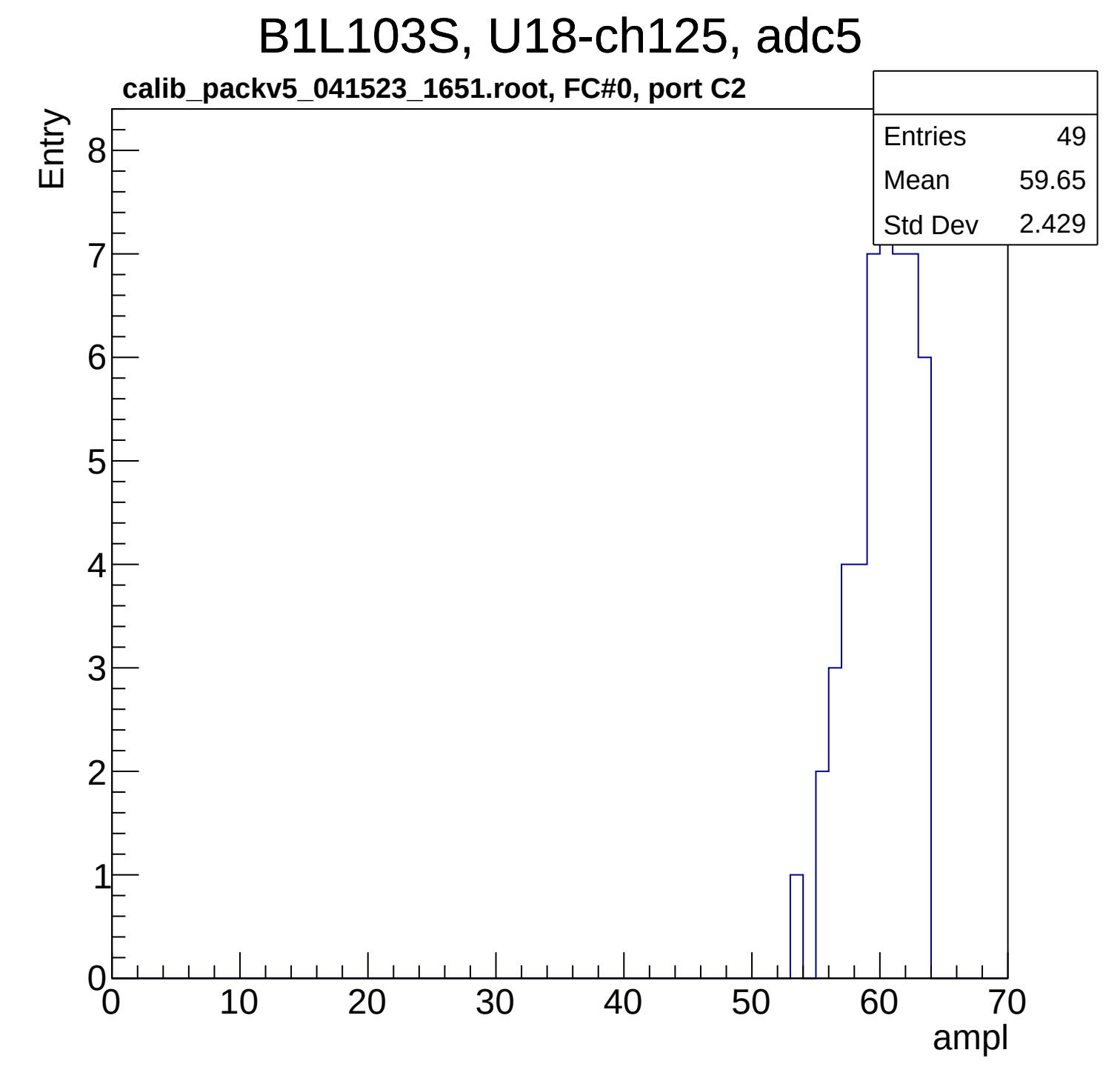

B1L103S, U18-ch125, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 95
Mean 21.04
Std Dev 12.9
Entry
0
5
10
15
20
25
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch125, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 33.85
Std Dev 6.918
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch125, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 38.5
Std Dev 11.15
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch125, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 41.29
Std Dev 17.38
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch125, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 53.29
Std Dev 7.563
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U18-ch125, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 59.65
Std Dev 2.429
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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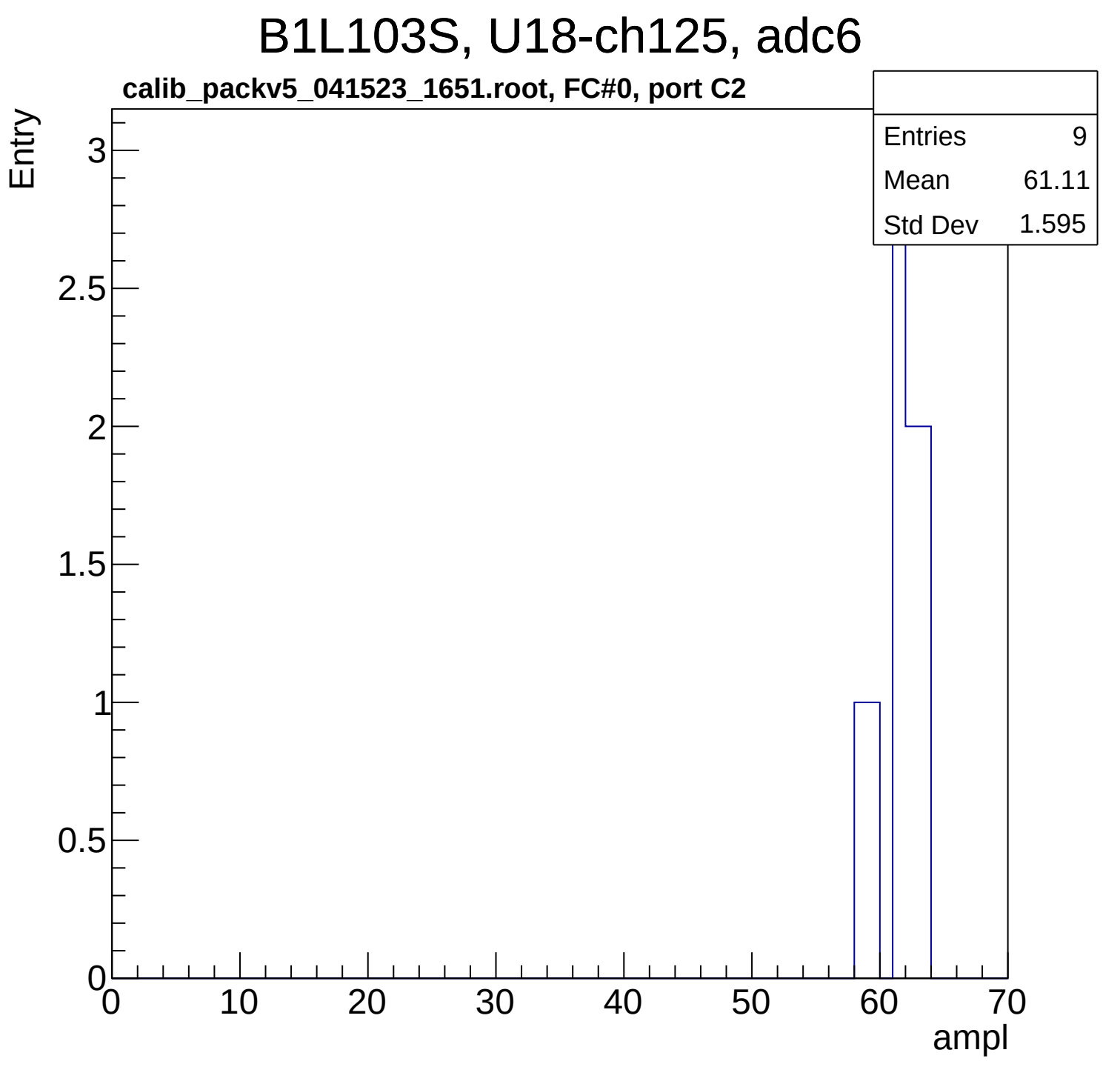
B1L103S, U18-ch125, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 9
Mean 61.11
Std Dev 1.595
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
10
20
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40
50
60
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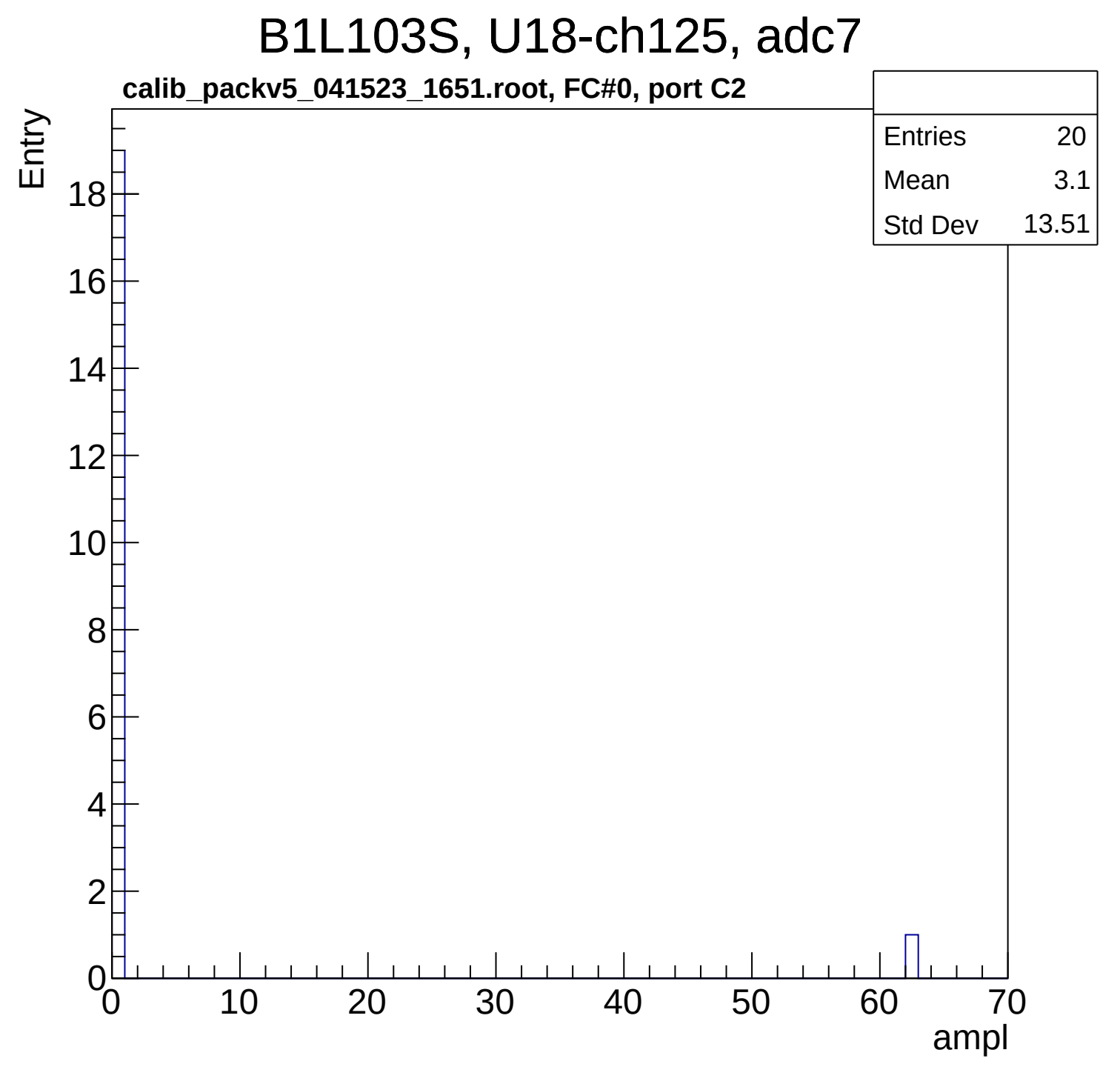
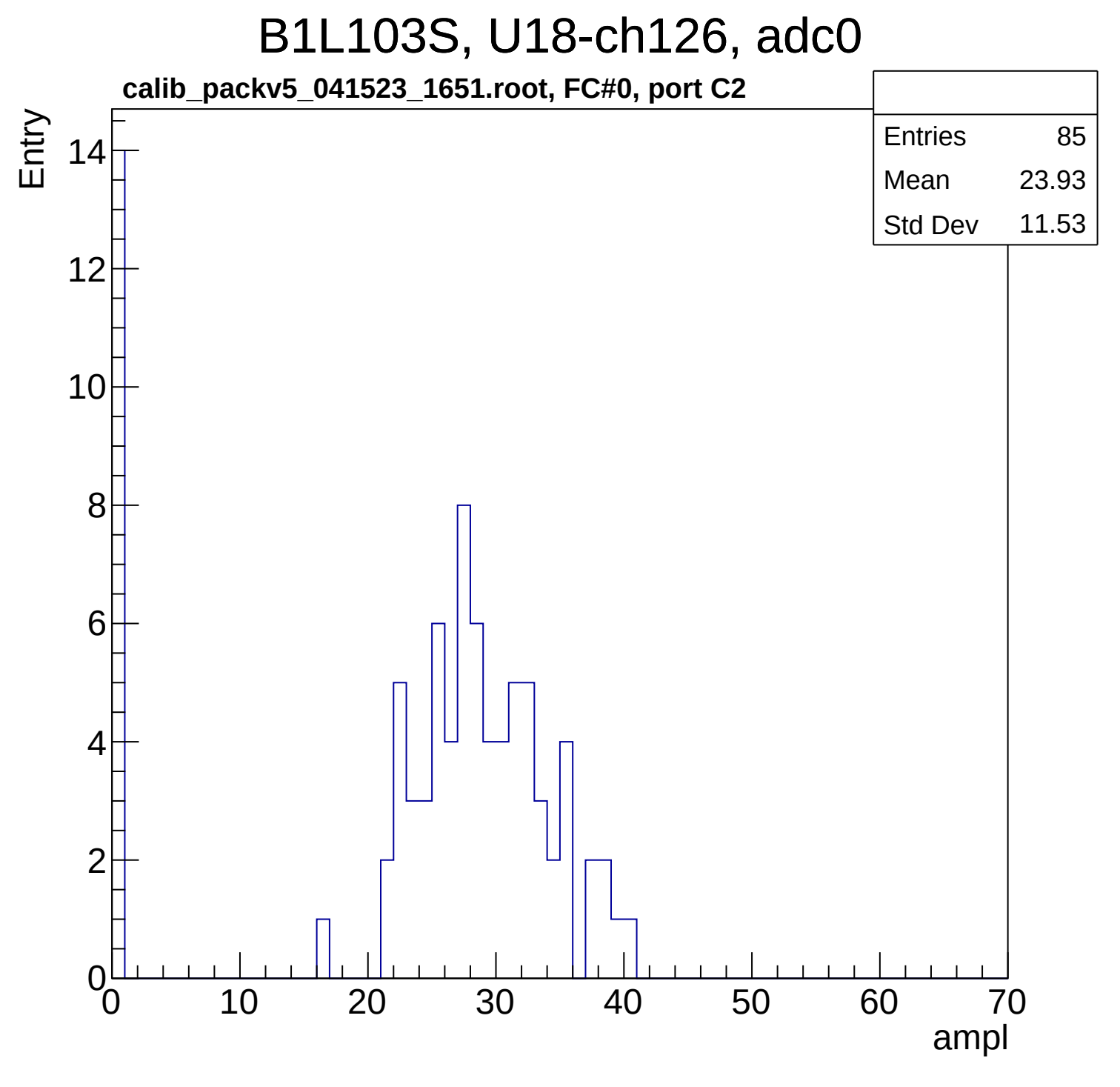

B1L103S, U18-ch125, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.1
Std Dev 13.51
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch126, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 23.93
Std Dev 11.53
Entry
ampl
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2
4
6
8
10
12
14
0
10
20
30
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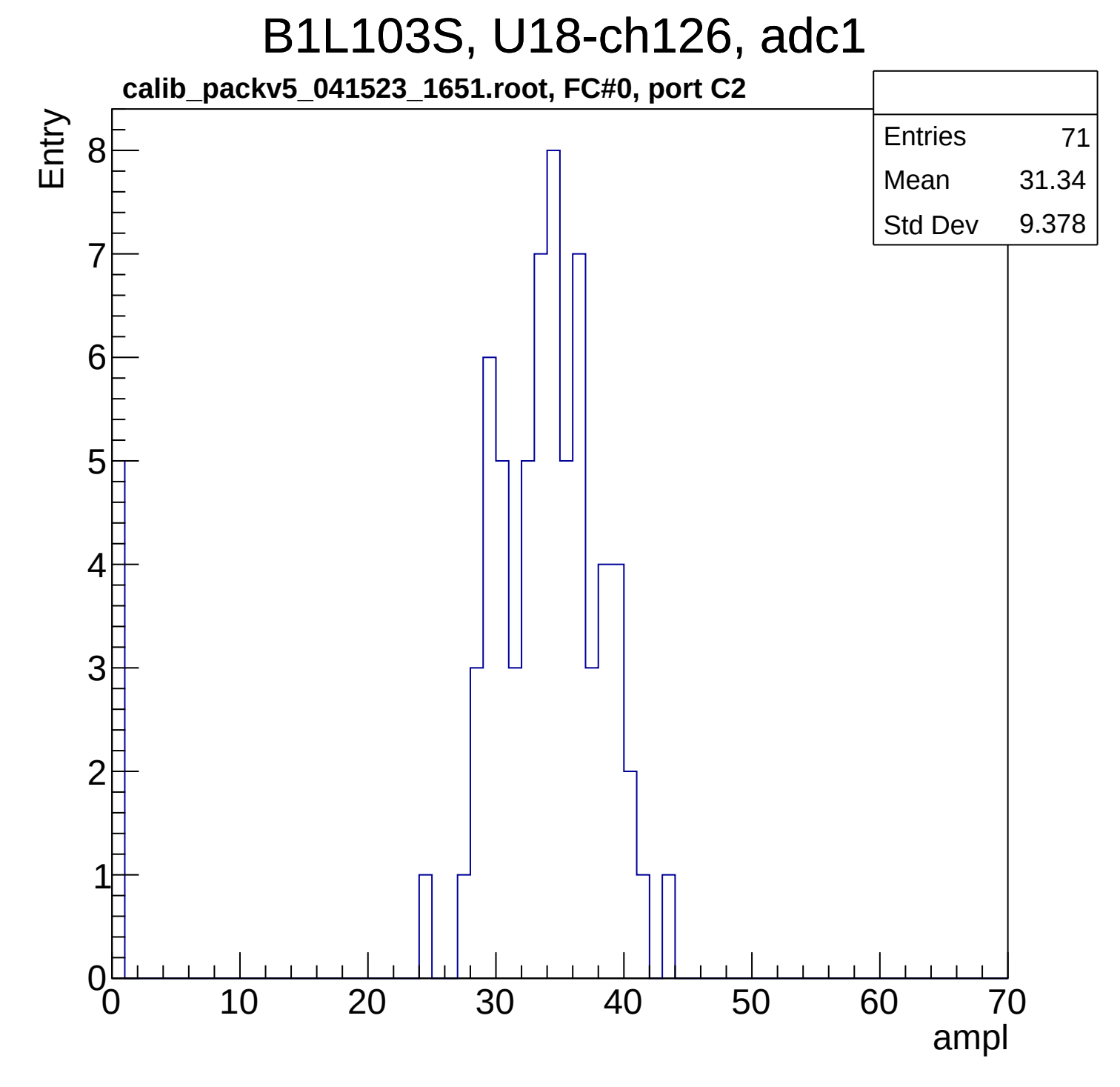
B1L103S, U18-ch126, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 31.34
Std Dev 9.378
Entry
ampl
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2
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4
5
6
7
8
0
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20
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60
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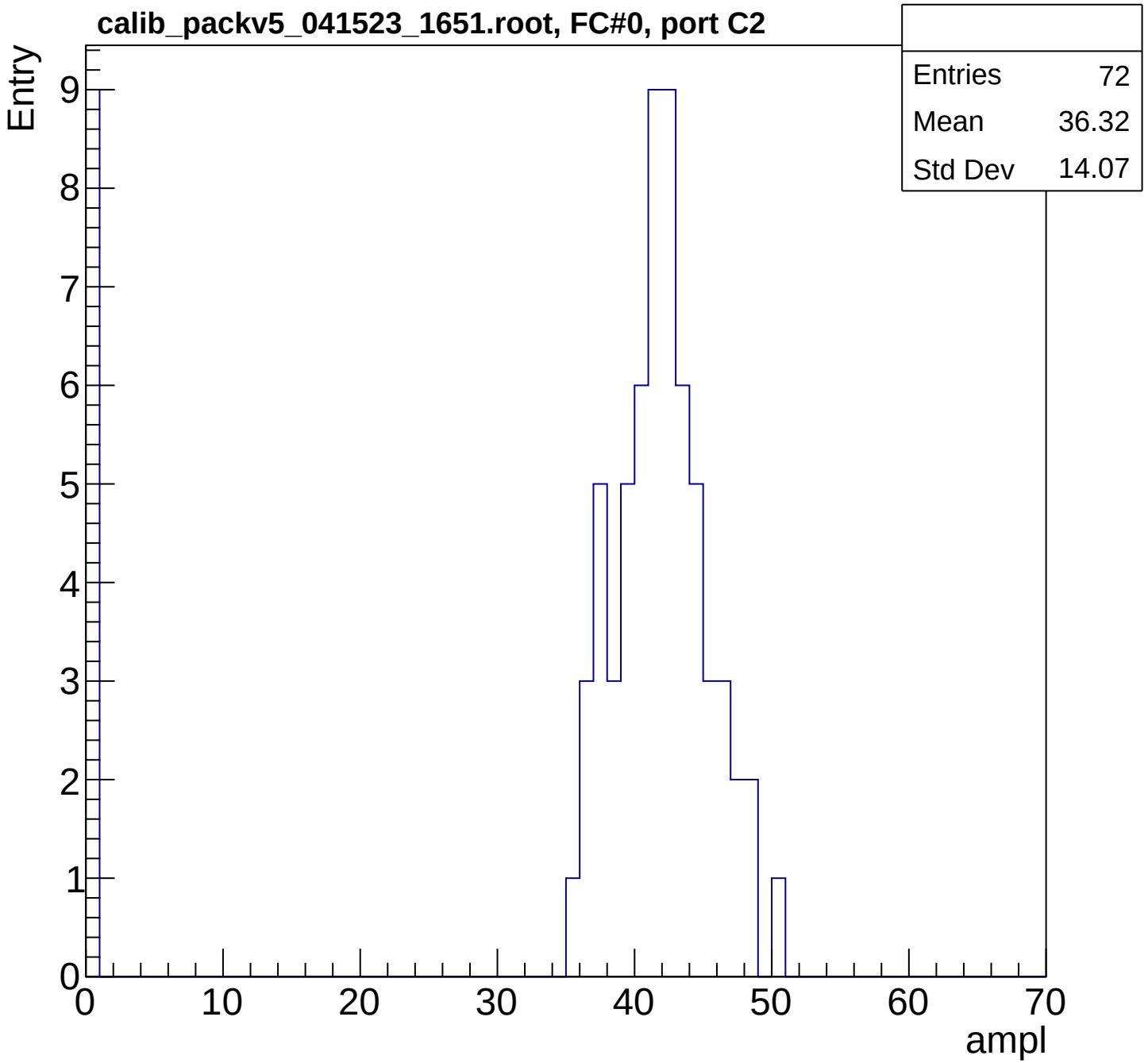
B1L103S, U18-ch126, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 36.32
Std Dev 14.07
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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40
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60
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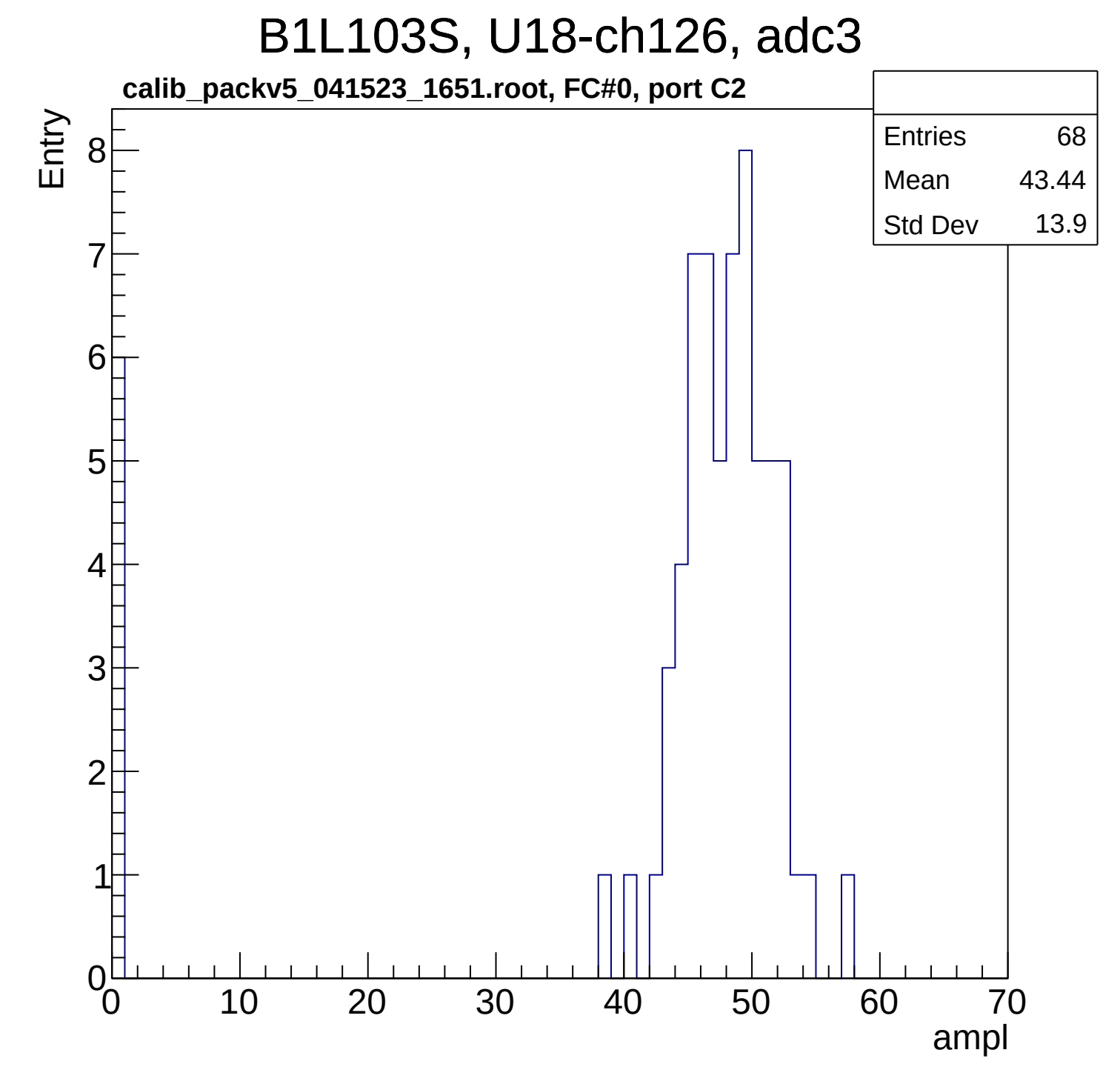
B1L103S, U18-ch126, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 43.44
Std Dev 13.9
Entry
ampl
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2
3
4
5
6
7
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0
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40
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60
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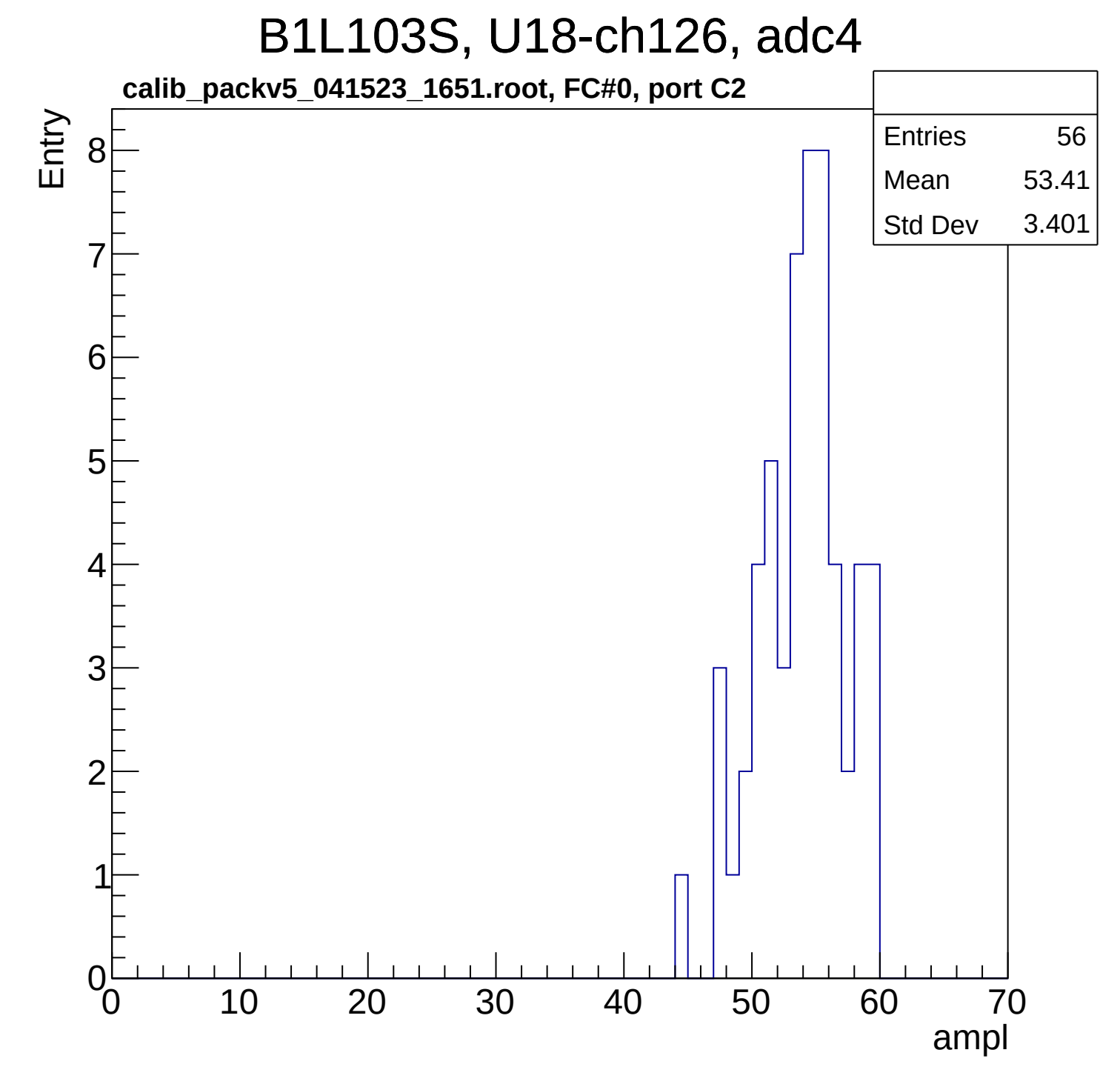
B1L103S, U18-ch126, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 53.41
Std Dev 3.401
Entry
ampl
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2
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5
6
7
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60
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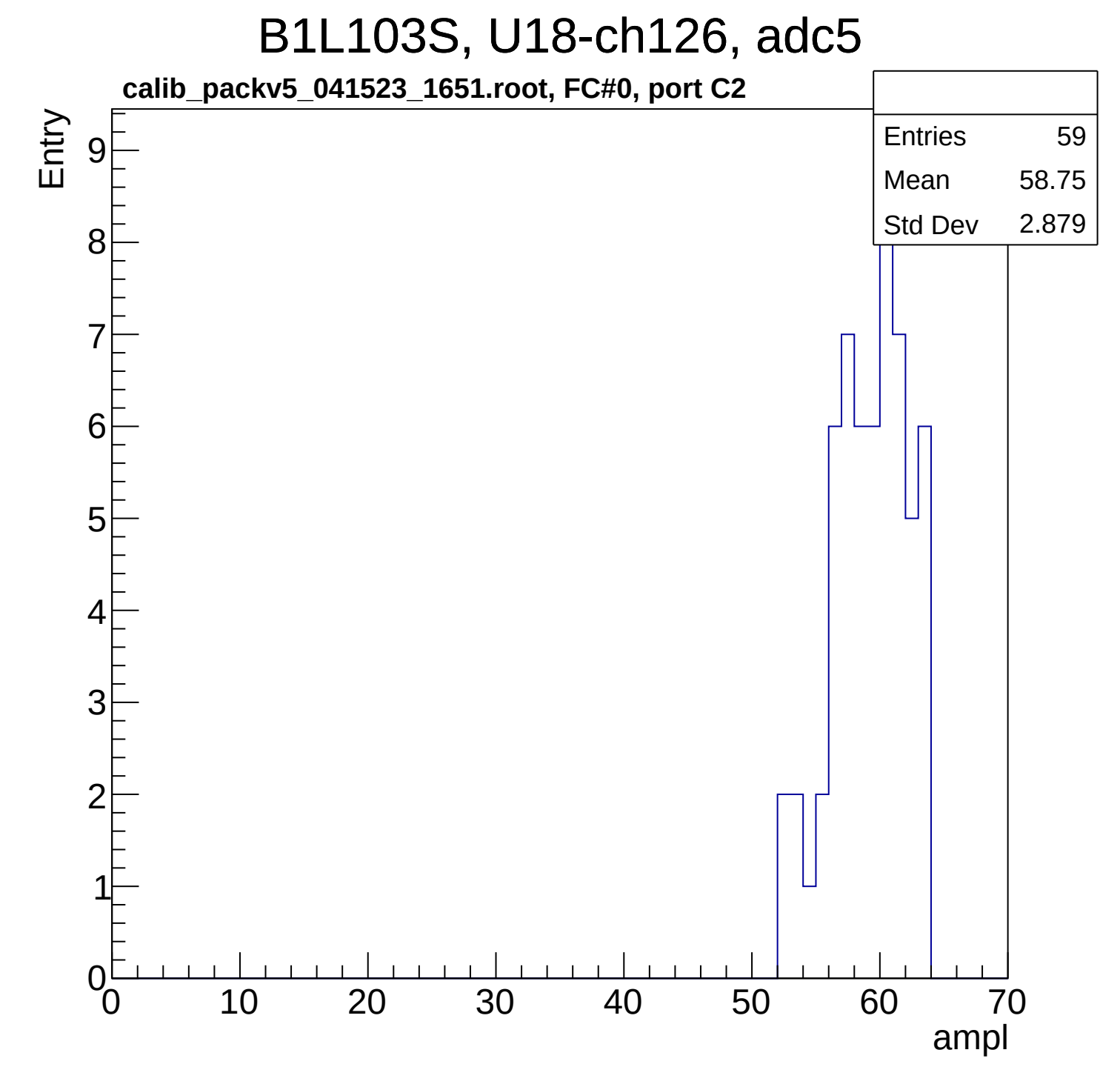
B1L103S, U18-ch126, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 58.75
Std Dev 2.879
Entry
ampl
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2
3
4
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6
7
8
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0
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60
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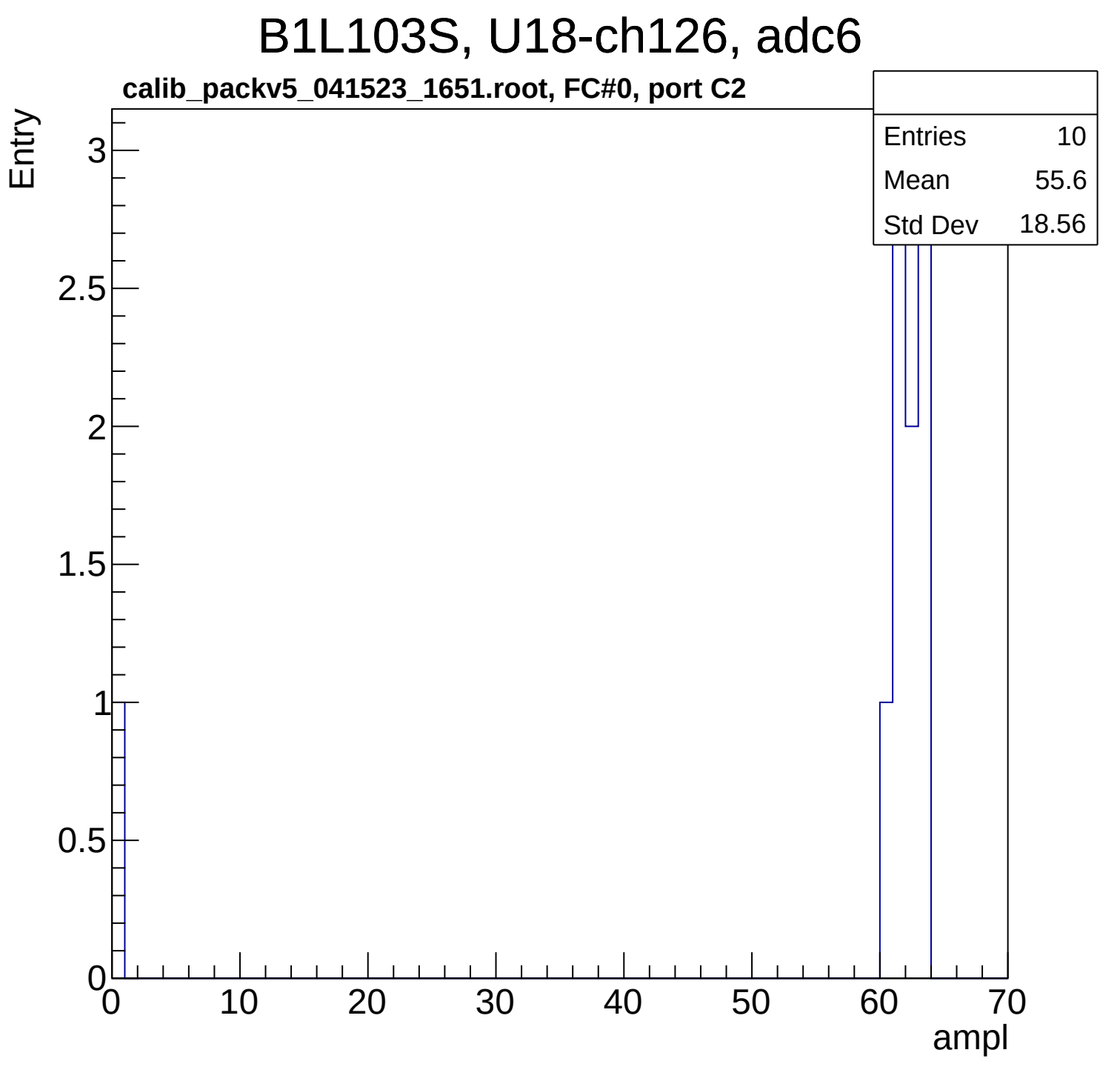
B1L103S, U18-ch126, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 55.6
Std Dev 18.56
Entry
ampl
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0.5
1
1.5
2
2.5
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0
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20
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40
50
60
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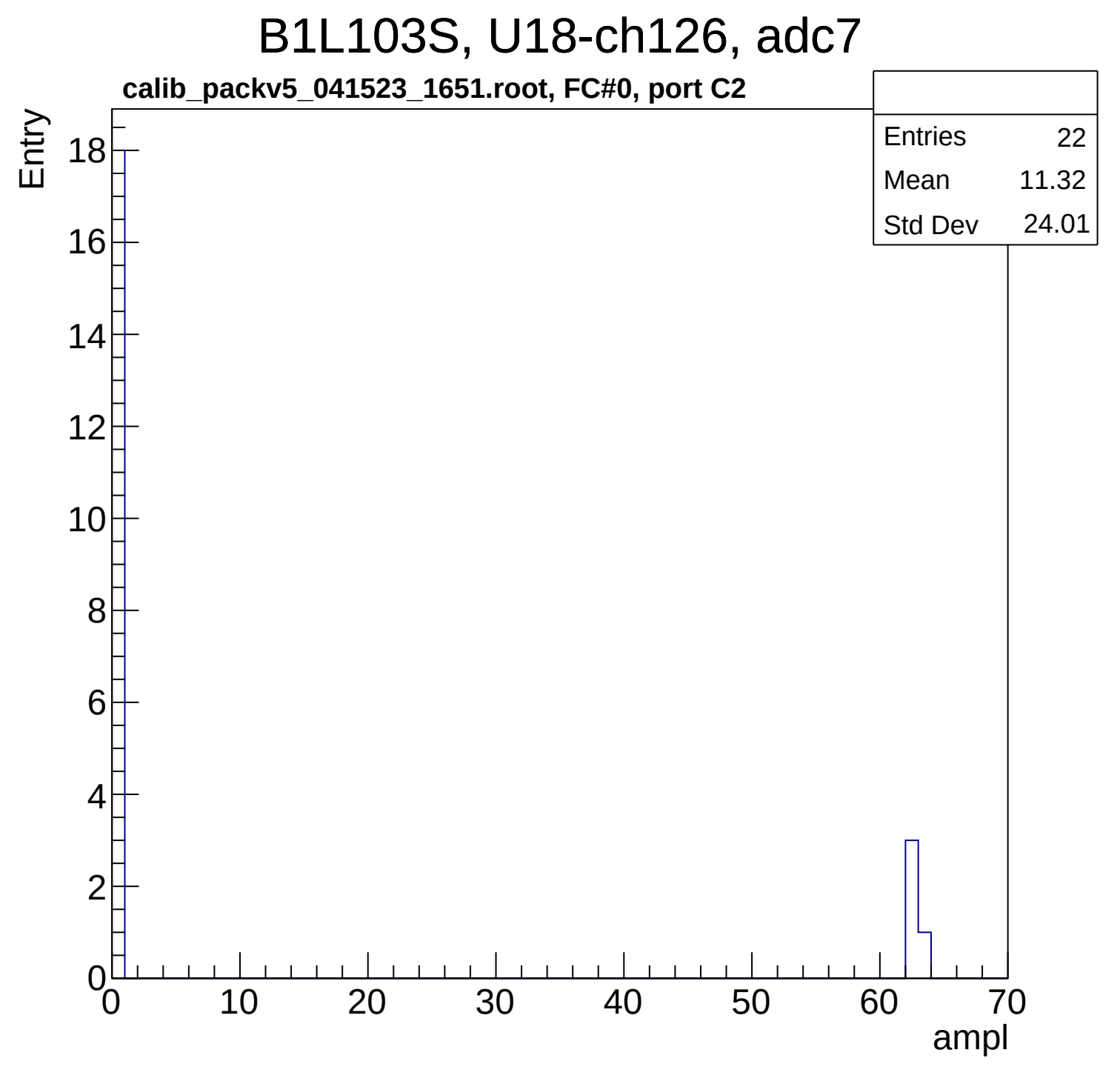
B1L103S, U18-ch126, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 11.32
Std Dev 24.01
Entry
ampl
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4
6
8
10
12
14
16
18
0
10
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30
40
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60
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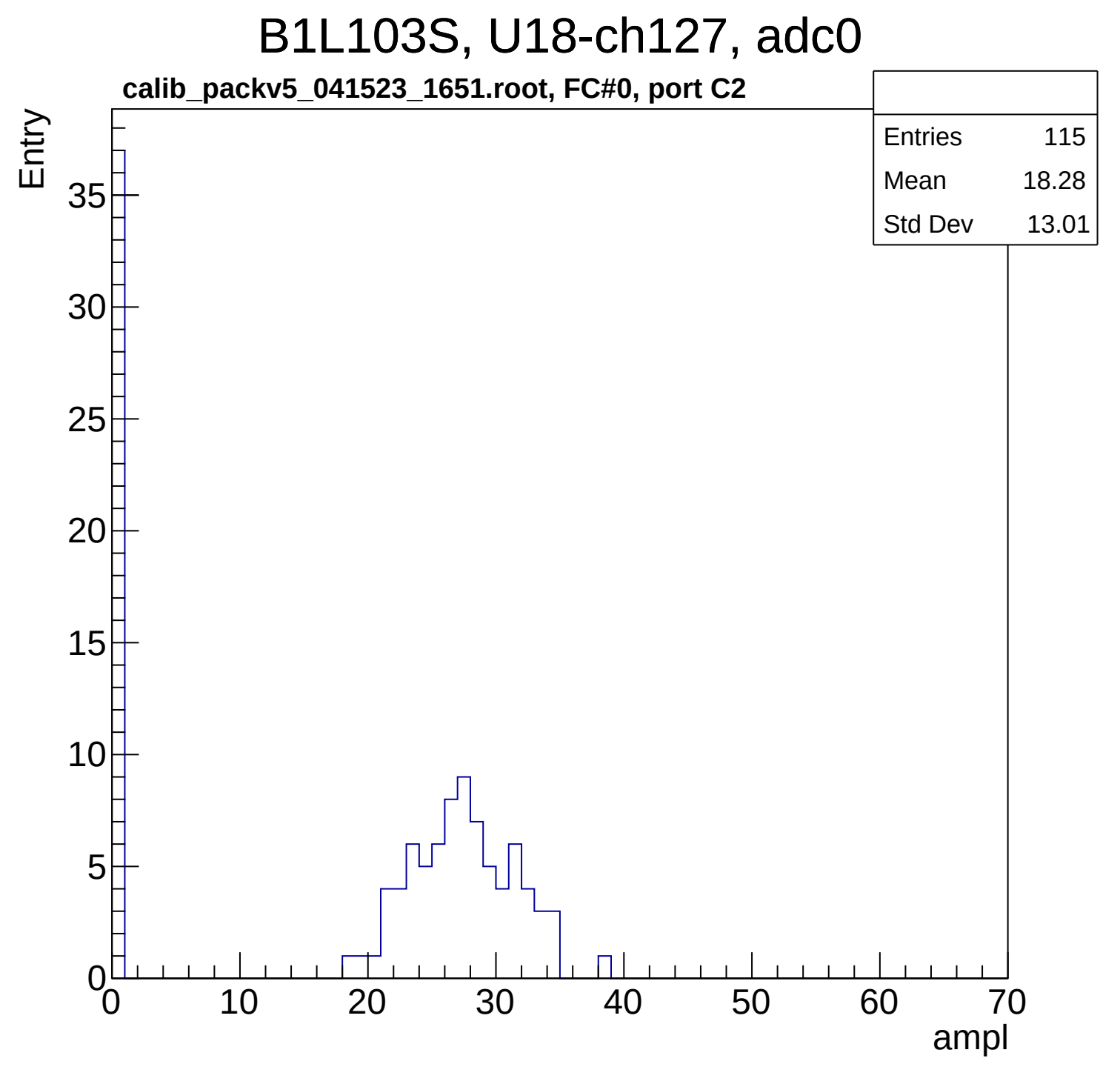
B1L103S, U18-ch127, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 115
Mean 18.28
Std Dev 13.01
Entry
ampl
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5
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0
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40
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60
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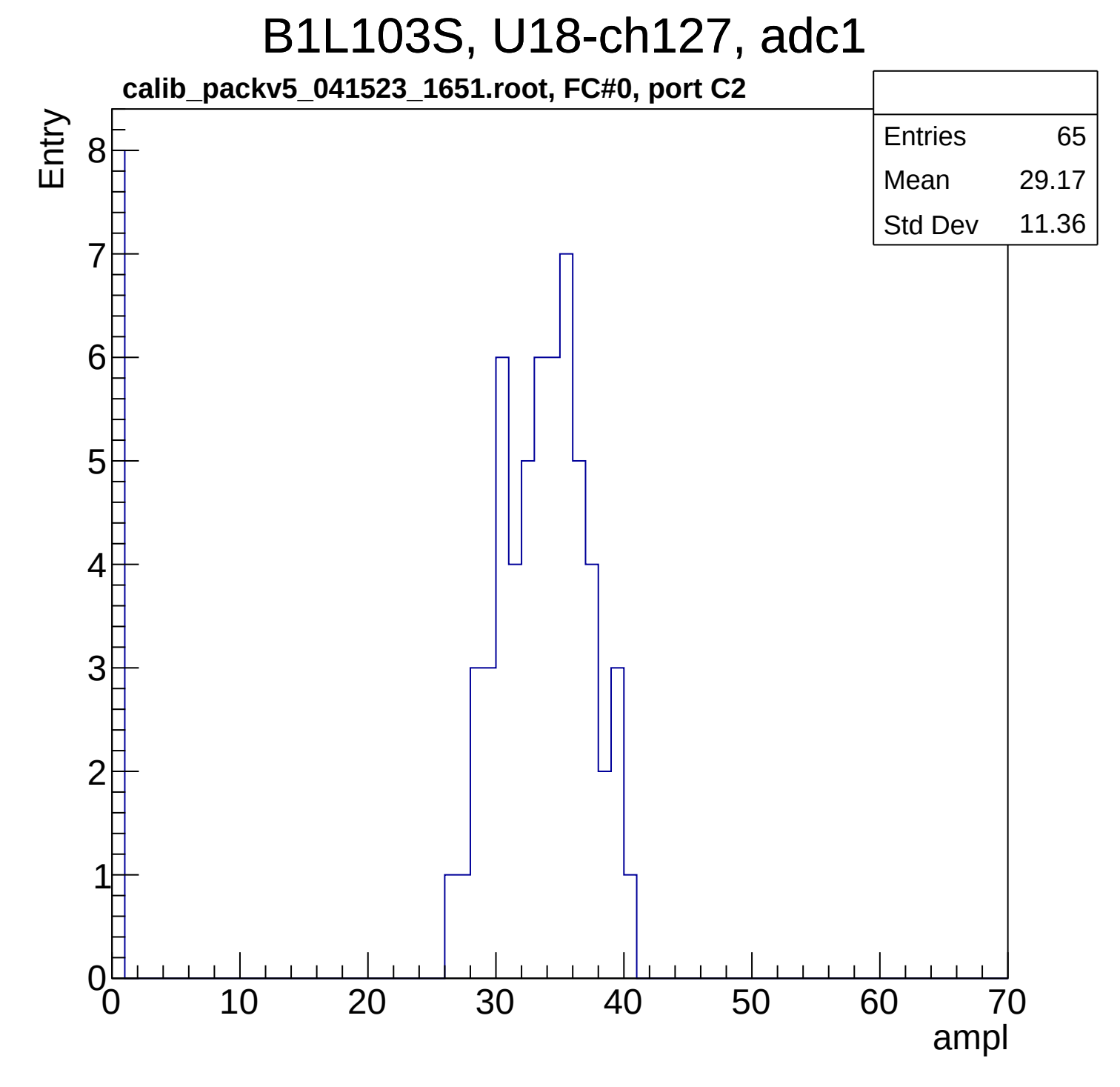
B1L103S, U18-ch127, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 29.17
Std Dev 11.36
Entry
ampl
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1
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3
4
5
6
7
8
0
10
20
30
40
50
60
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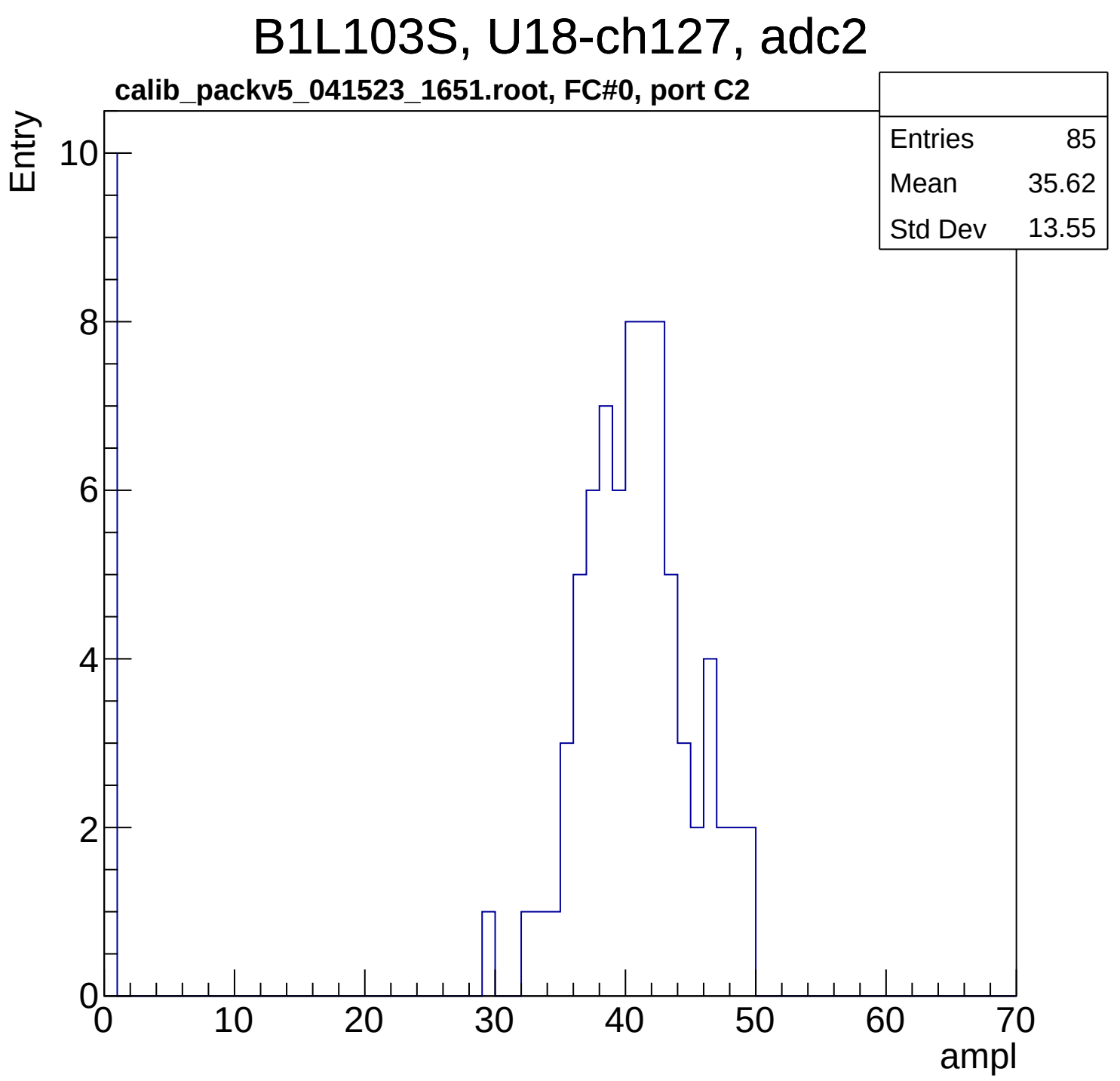
B1L103S, U18-ch127, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 35.62
Std Dev 13.55
Entry
ampl
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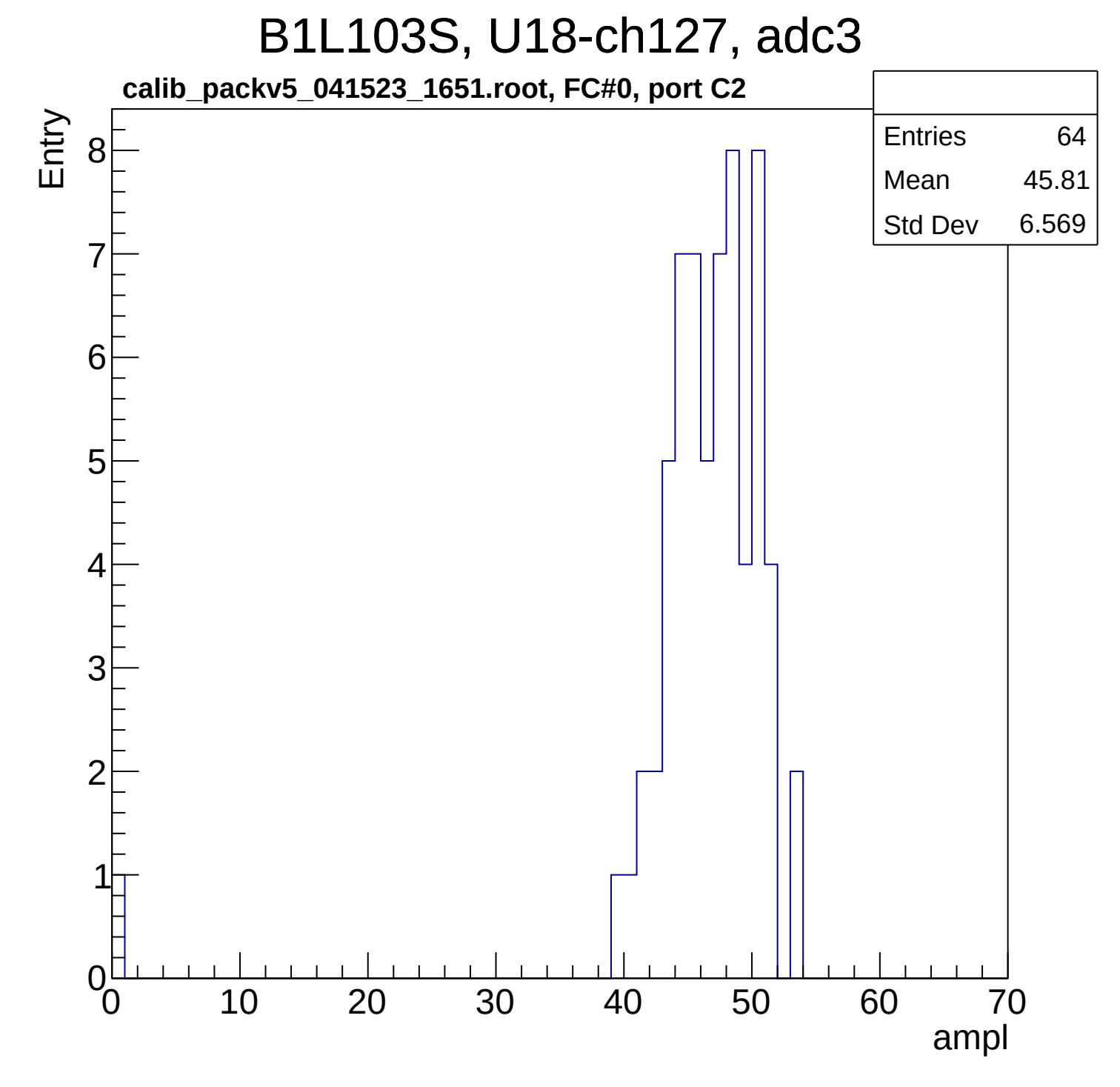
B1L103S, U18-ch127, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 45.81
Std Dev 6.569
Entry
ampl
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3
4
5
6
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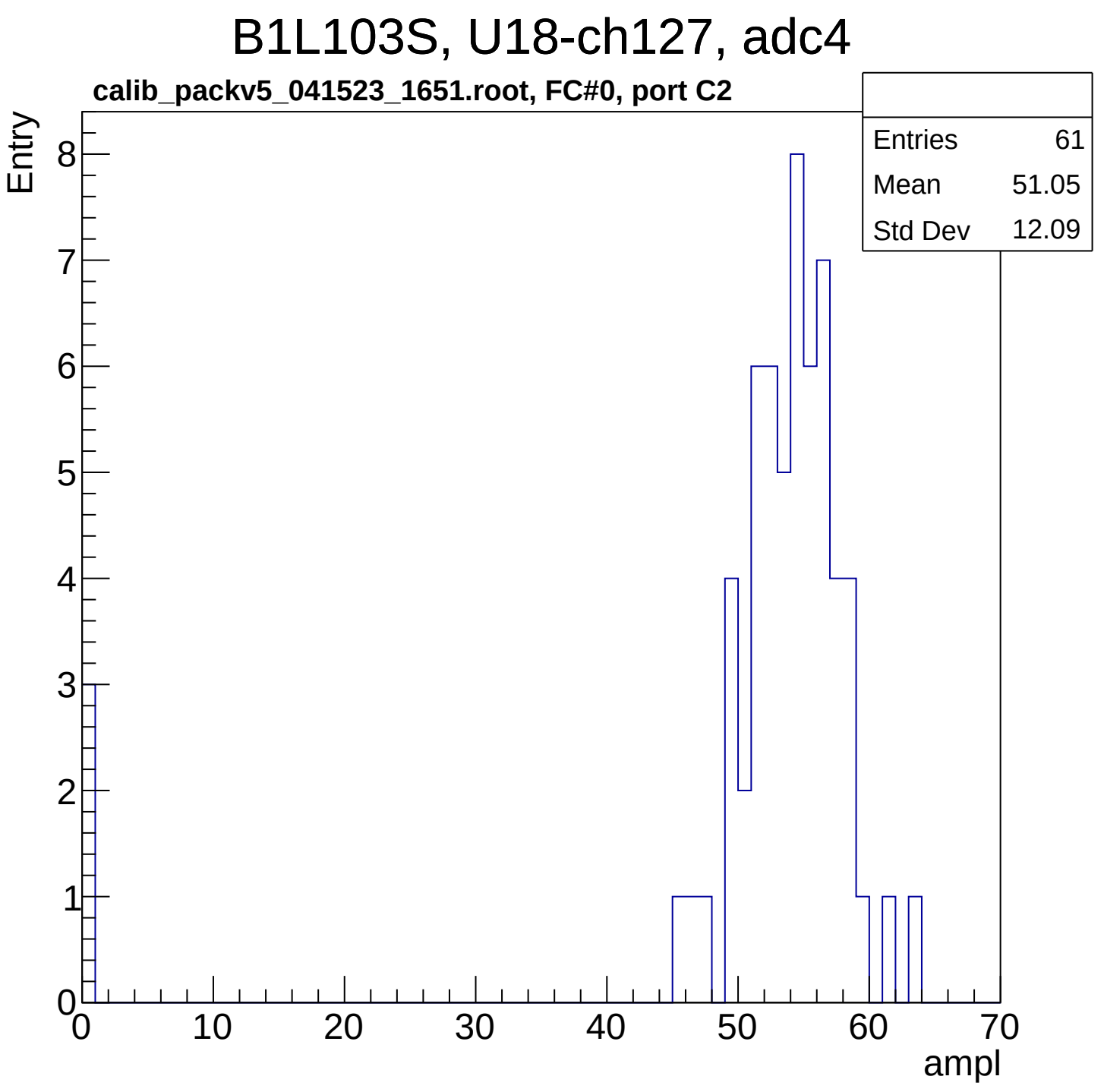
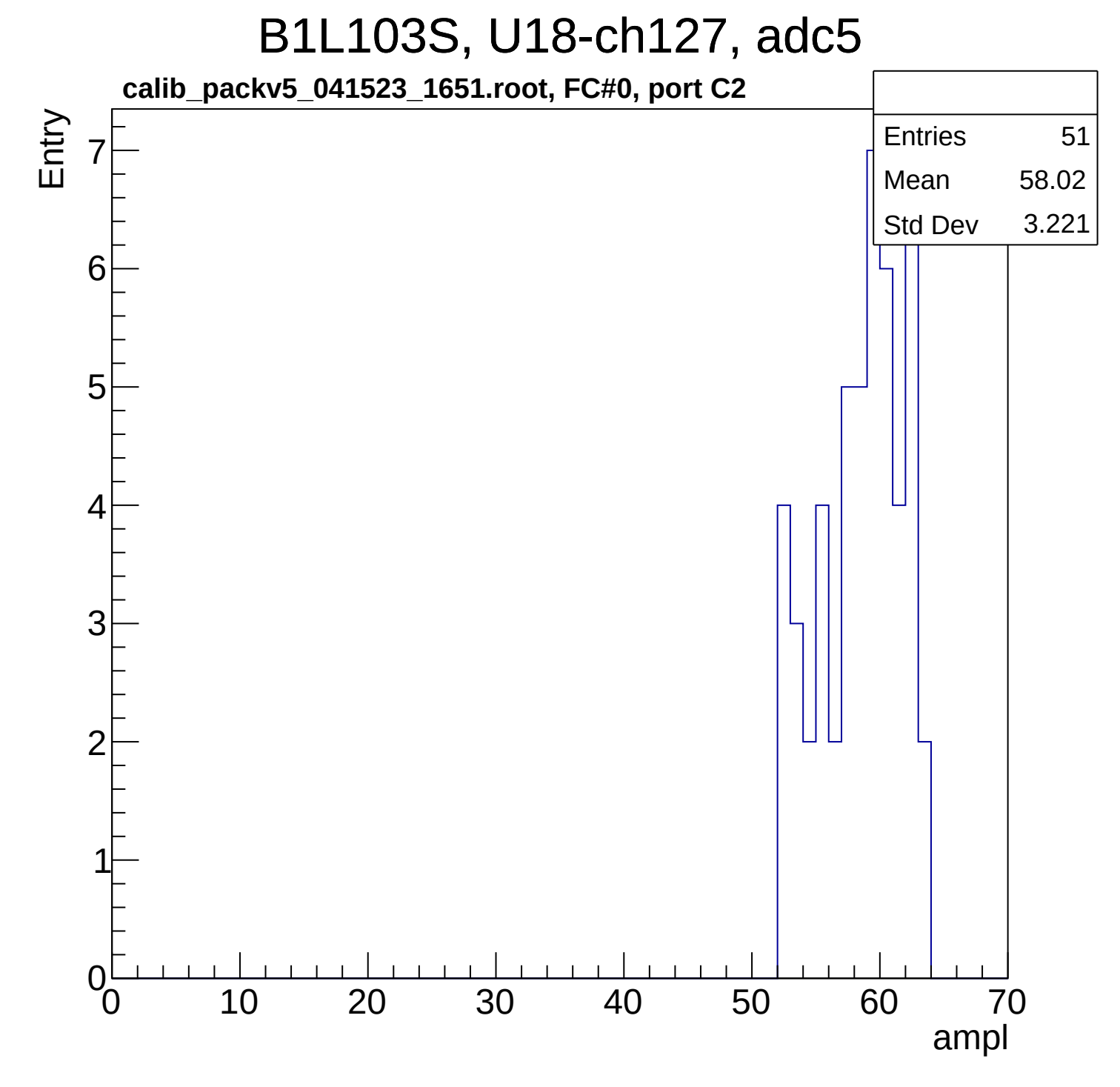
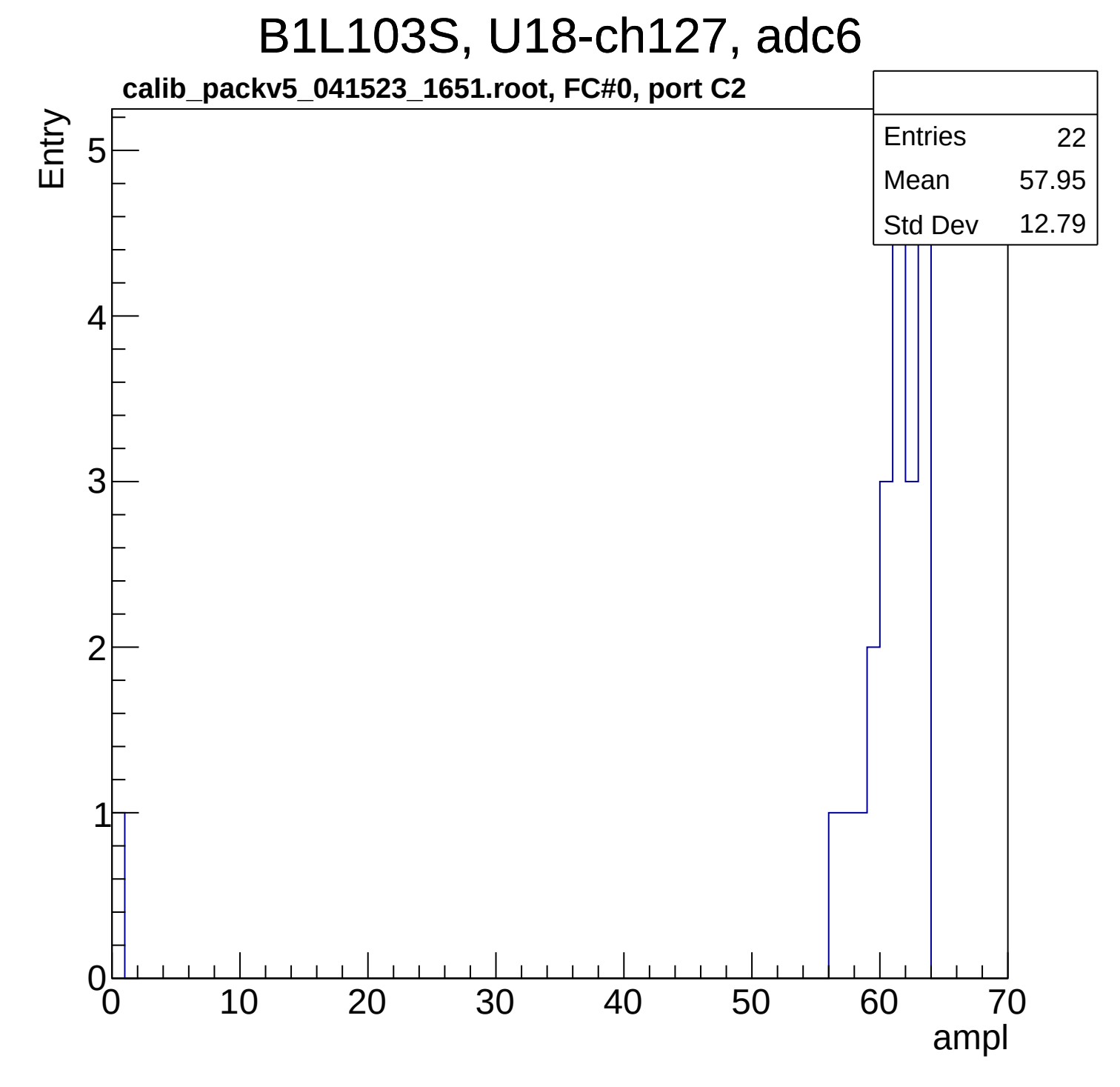
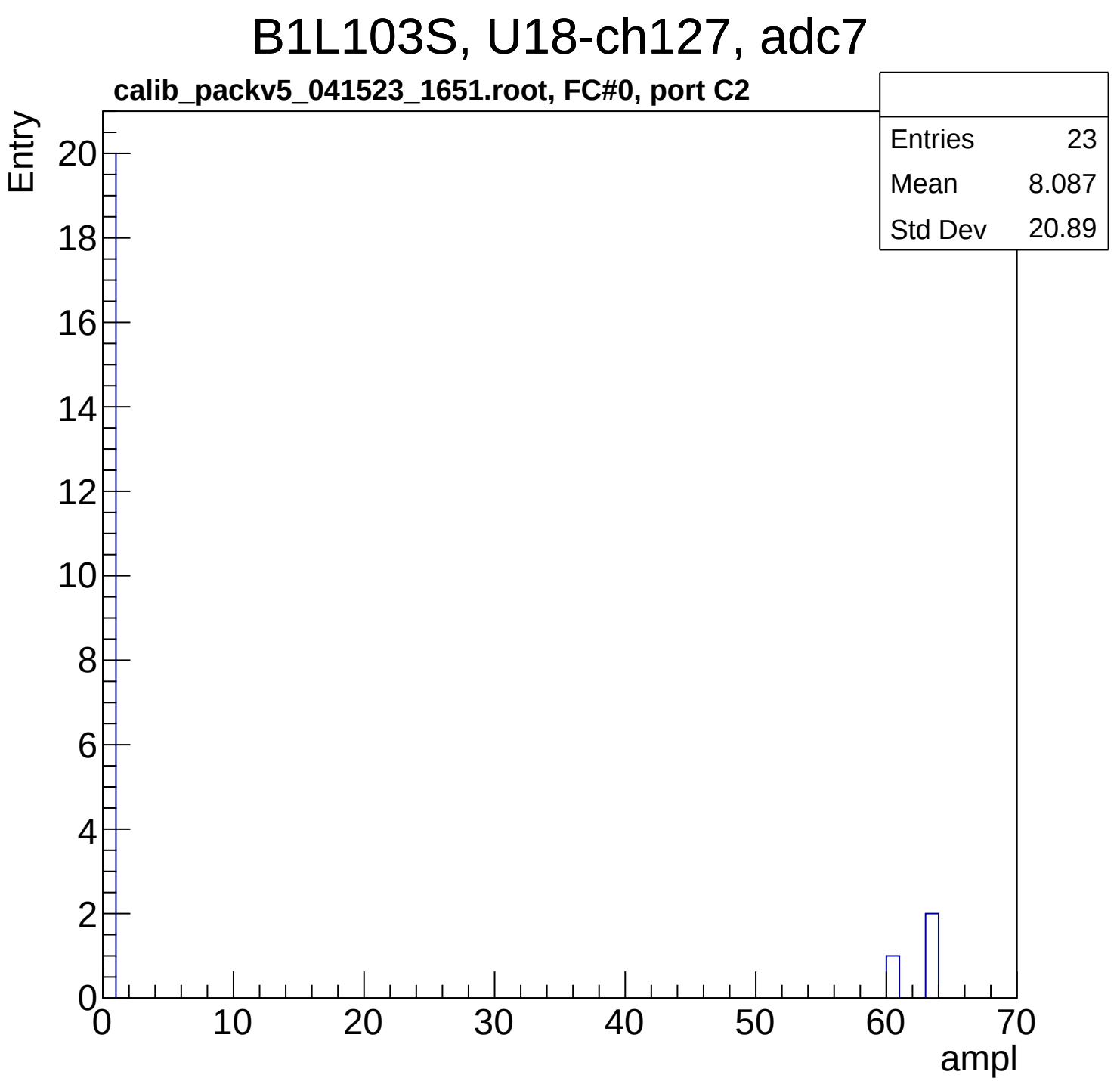
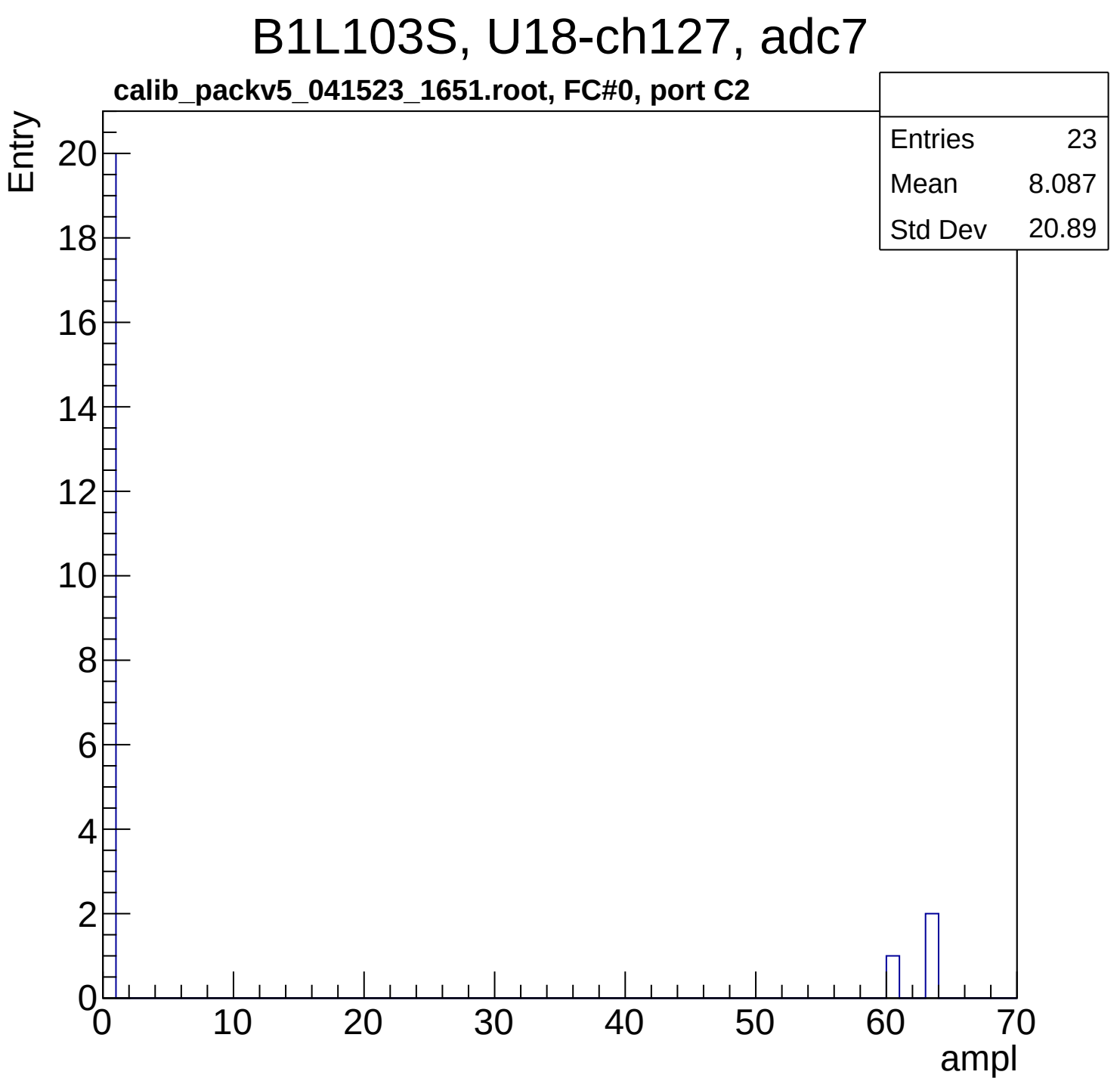

B1L103S, U18-ch127, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 51.05
Std Dev 12.09
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U18-ch127, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 58.02
Std Dev 3.221
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U18-ch127, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 57.95
Std Dev 12.79
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U18-ch127, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 23
Mean 8.087
Std Dev 20.89
Entry
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70
ampl


B1L103S, U18-ch127, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 23
Mean 8.087
Std Dev 20.89
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70