



# B1L100S, U2-ch0, adc0

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	79
Mean	26.2
Std Dev	6.466

**Gaus mean : 27.5542**

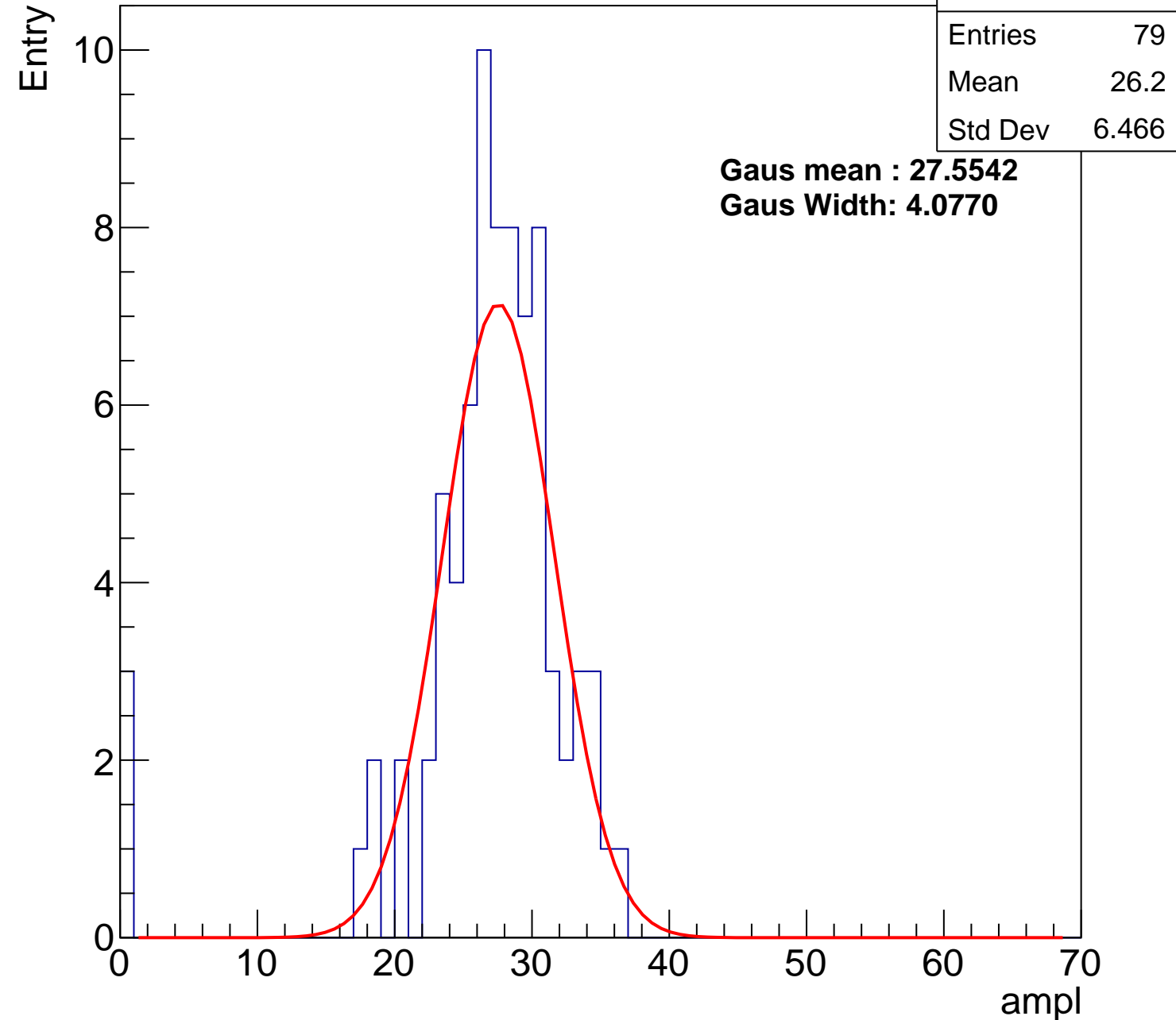
**Gaus Width: 4.0770**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



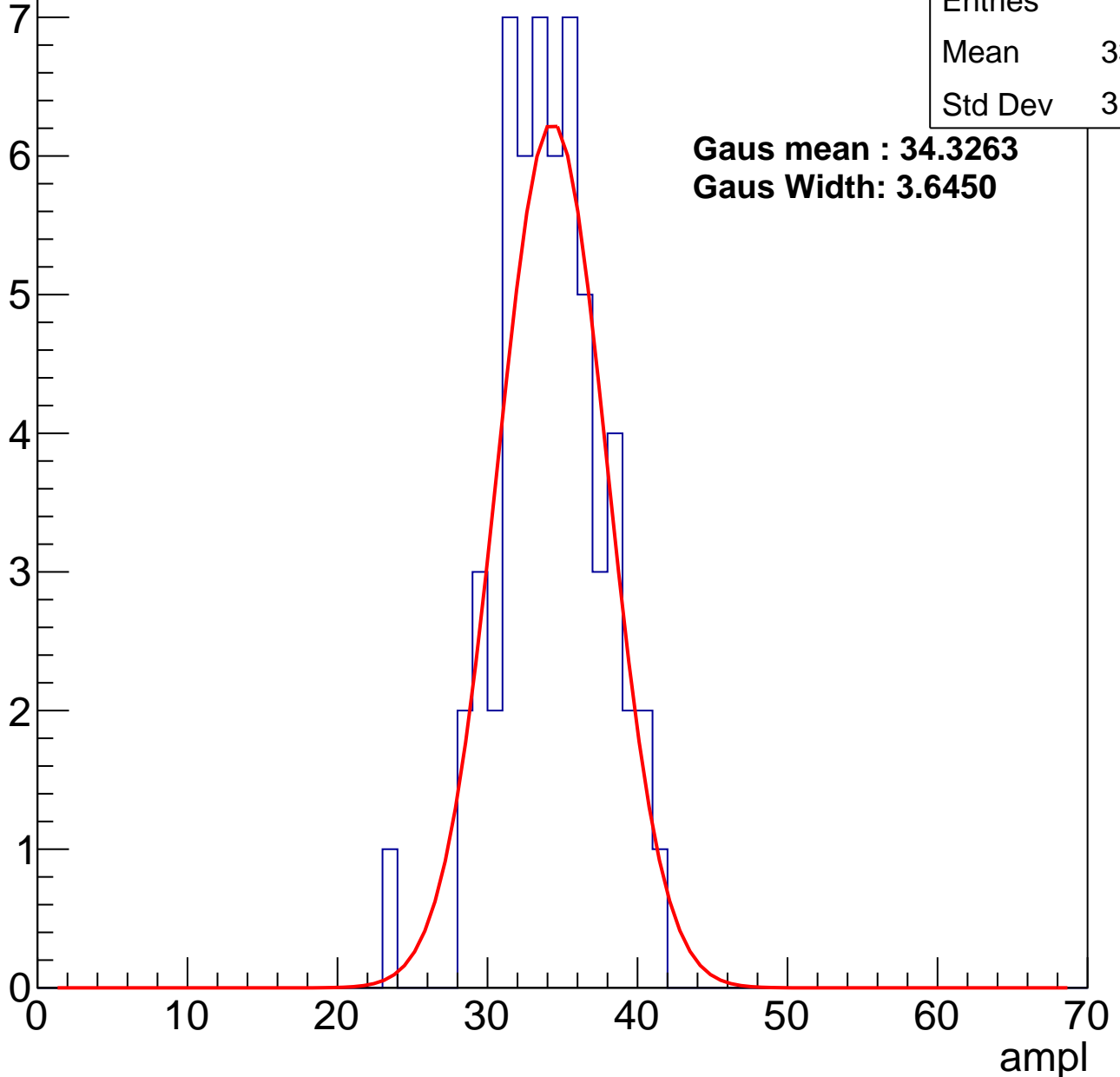
# B1L100S, U2-ch0, adc1

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	58
Mean	33.74
Std Dev	3.422

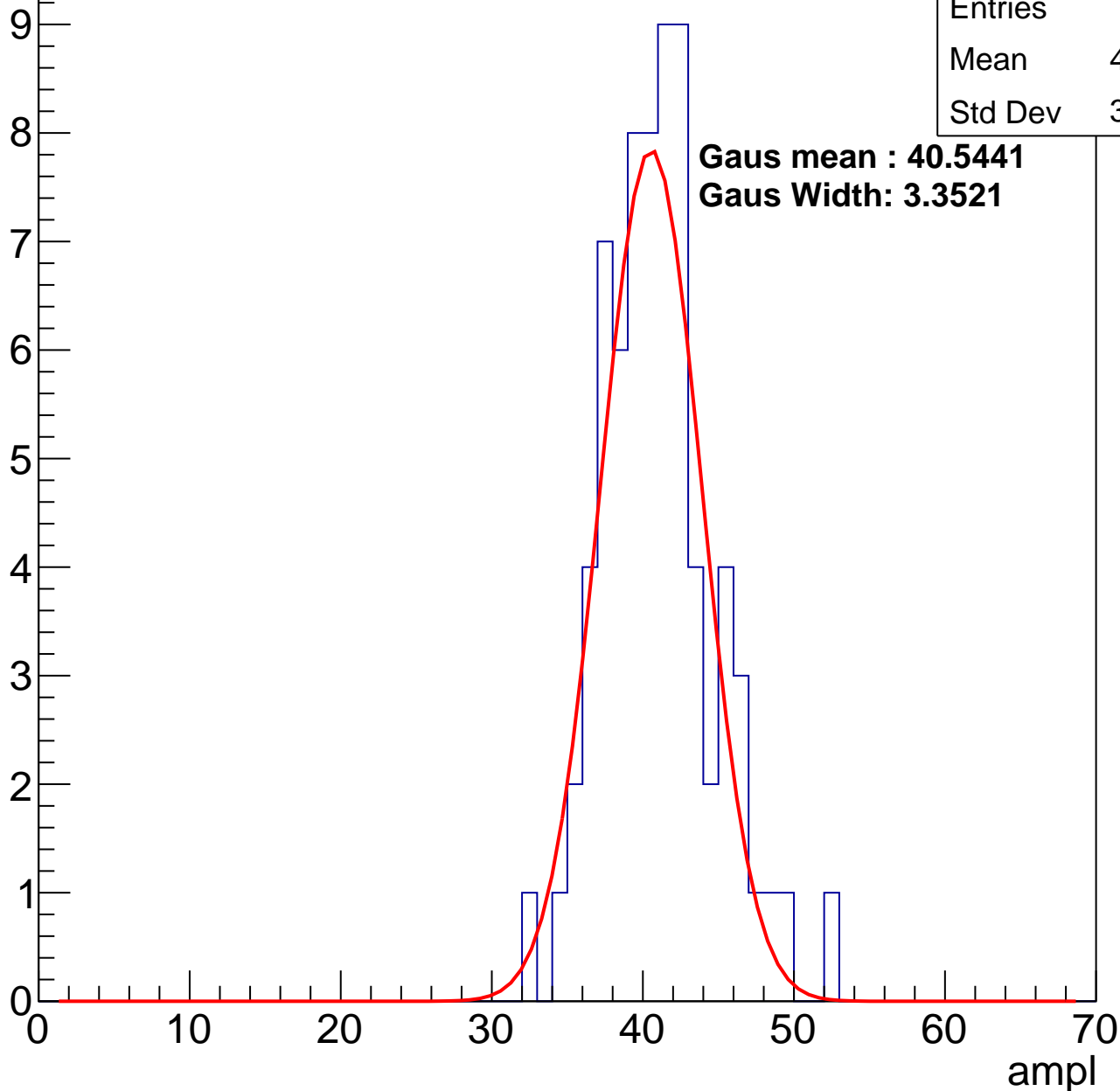
**Gaus mean : 34.3263**  
**Gaus Width: 3.6450**



# B1L100S, U2-ch0, adc2

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

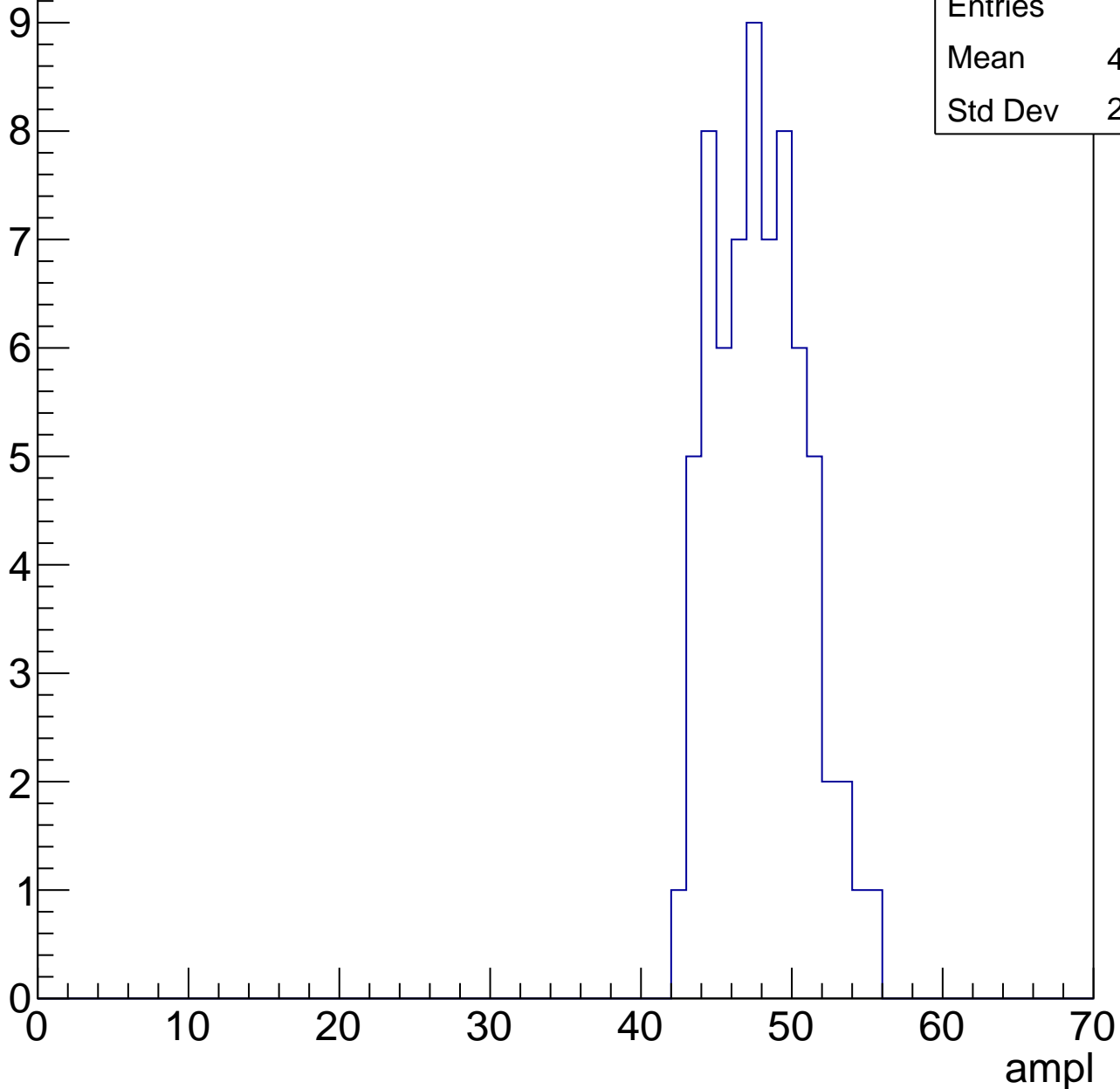


# B1L100S, U2-ch0, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	68
Mean	47.44
Std Dev	2.977

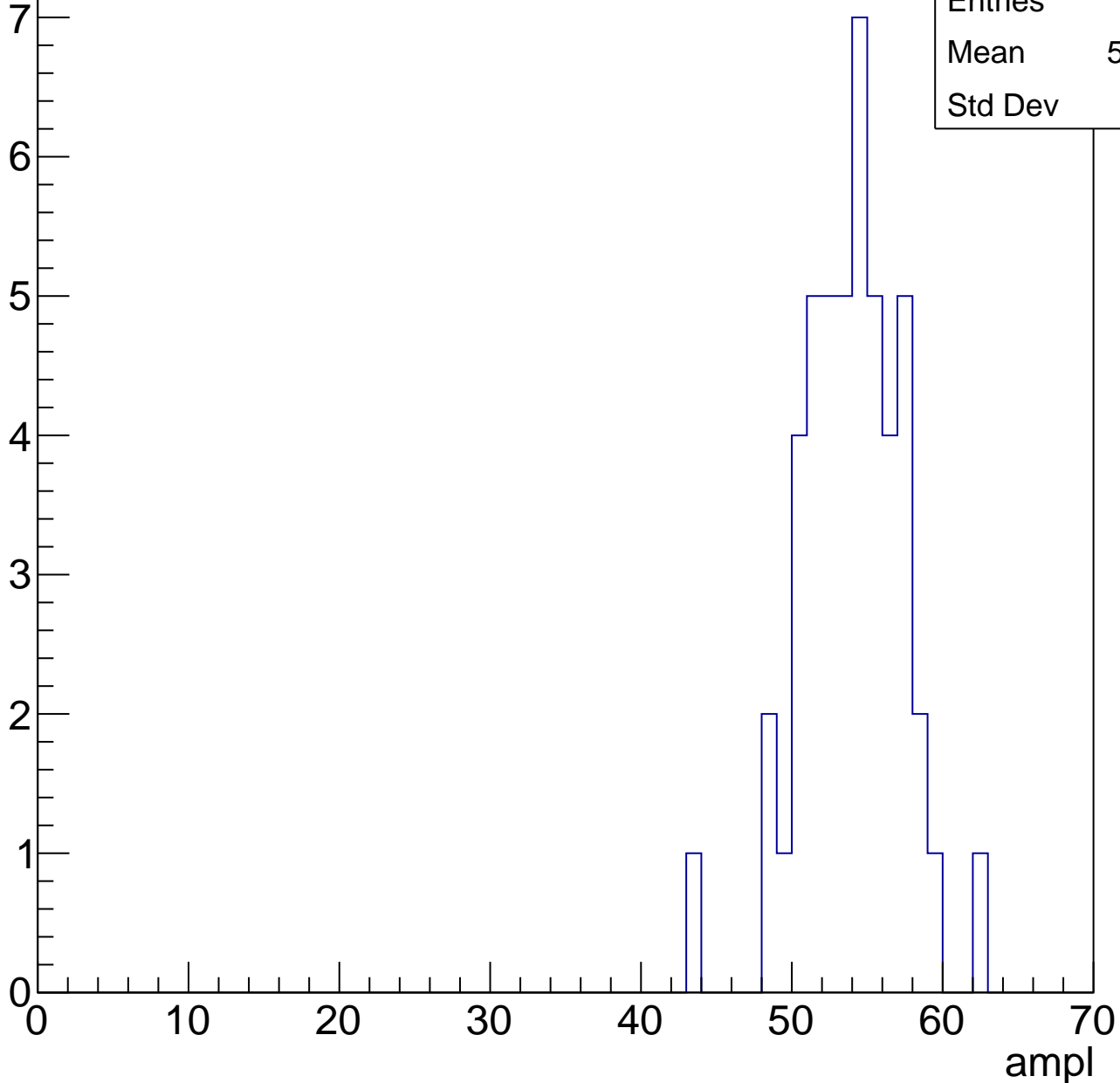


# B1L100S, U2-ch0, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	48
Mean	53.48
Std Dev	3.31



# B1L100S, U2-ch0, adc5

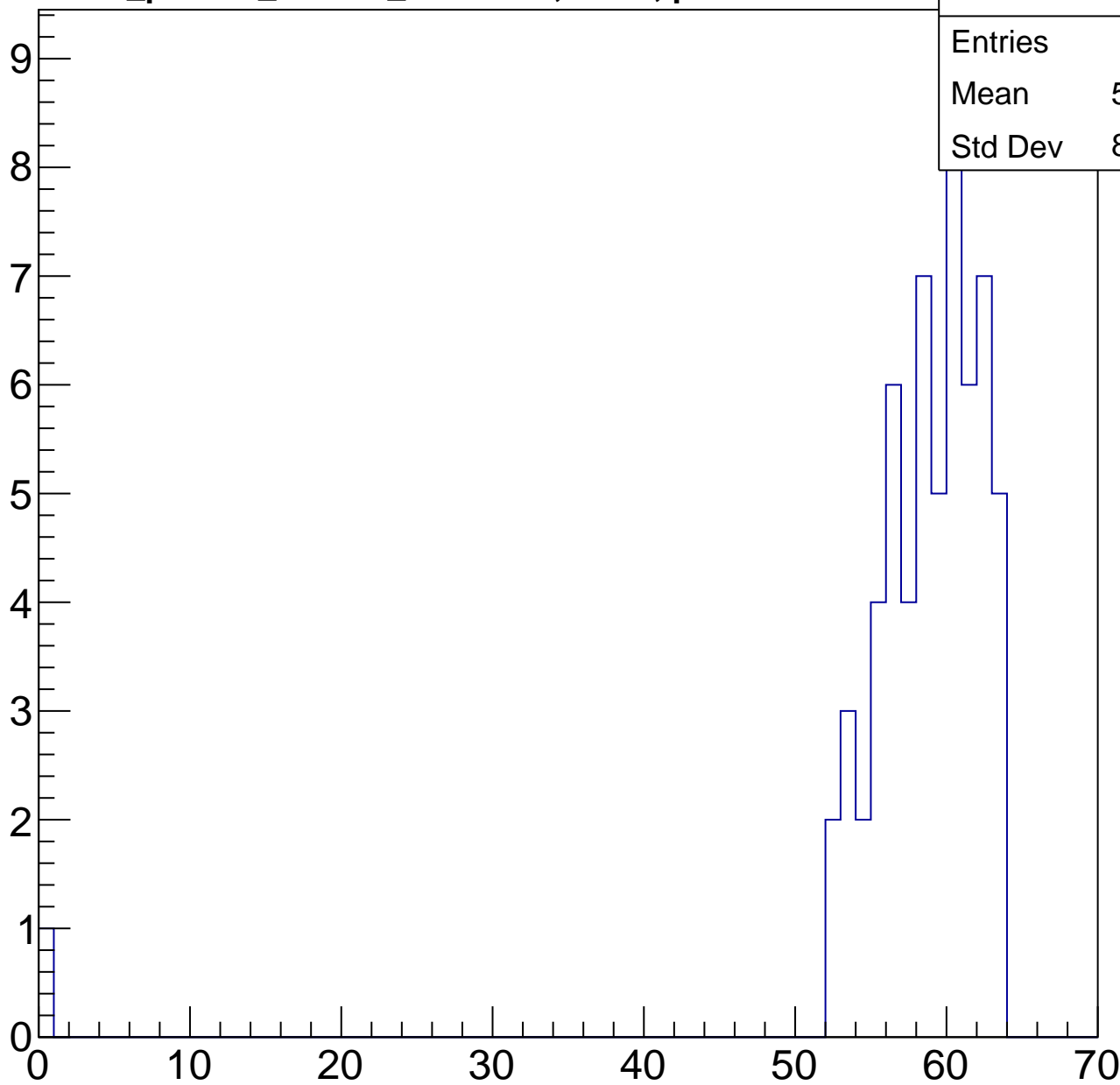
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	61
Mean	57.56
Std Dev	8.024

ampl

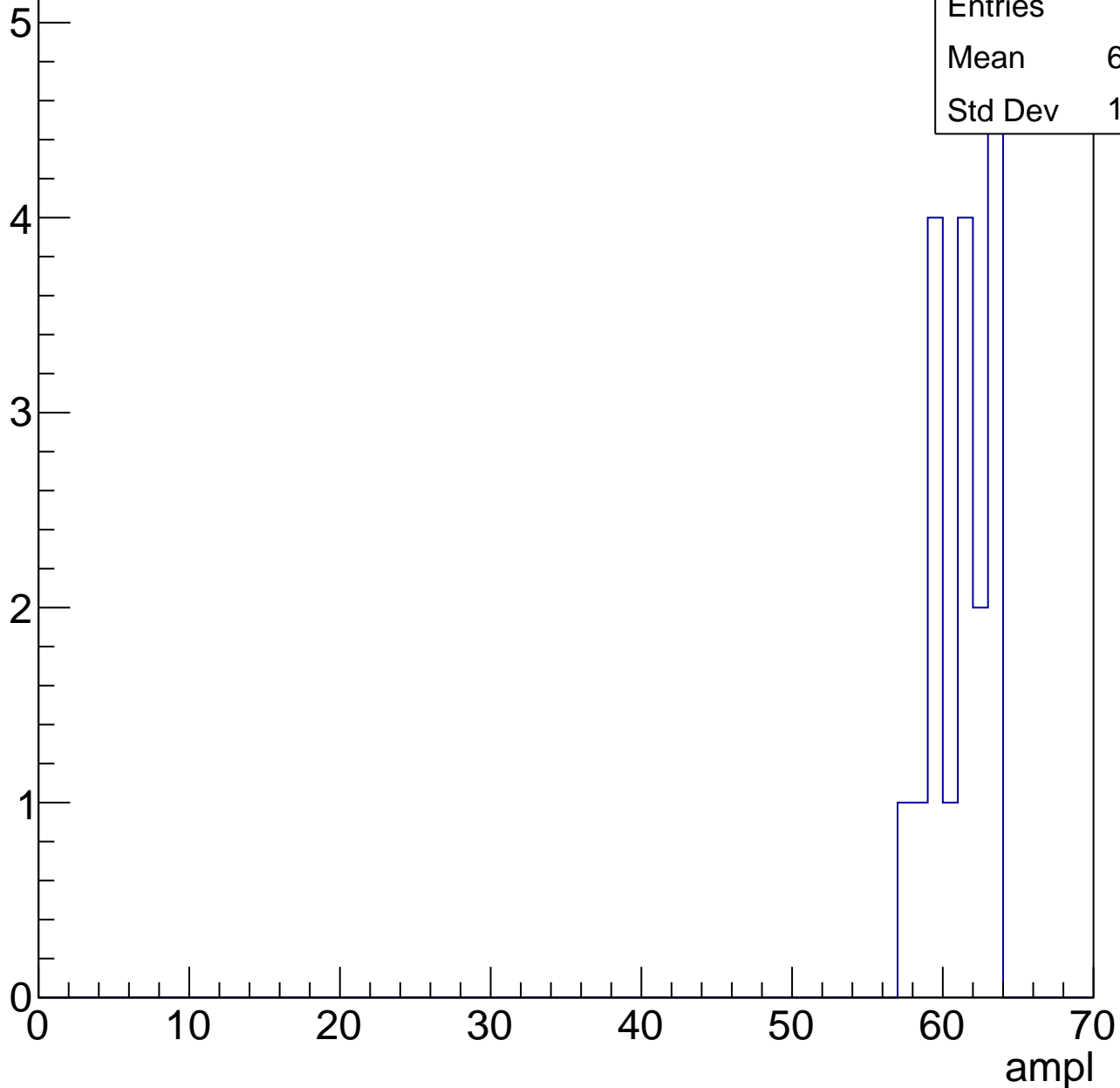


# B1L100S, U2-ch0, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	18
Mean	60.78
Std Dev	1.872





# B1L100S, U2-ch0, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L100S, U2-ch1, adc0

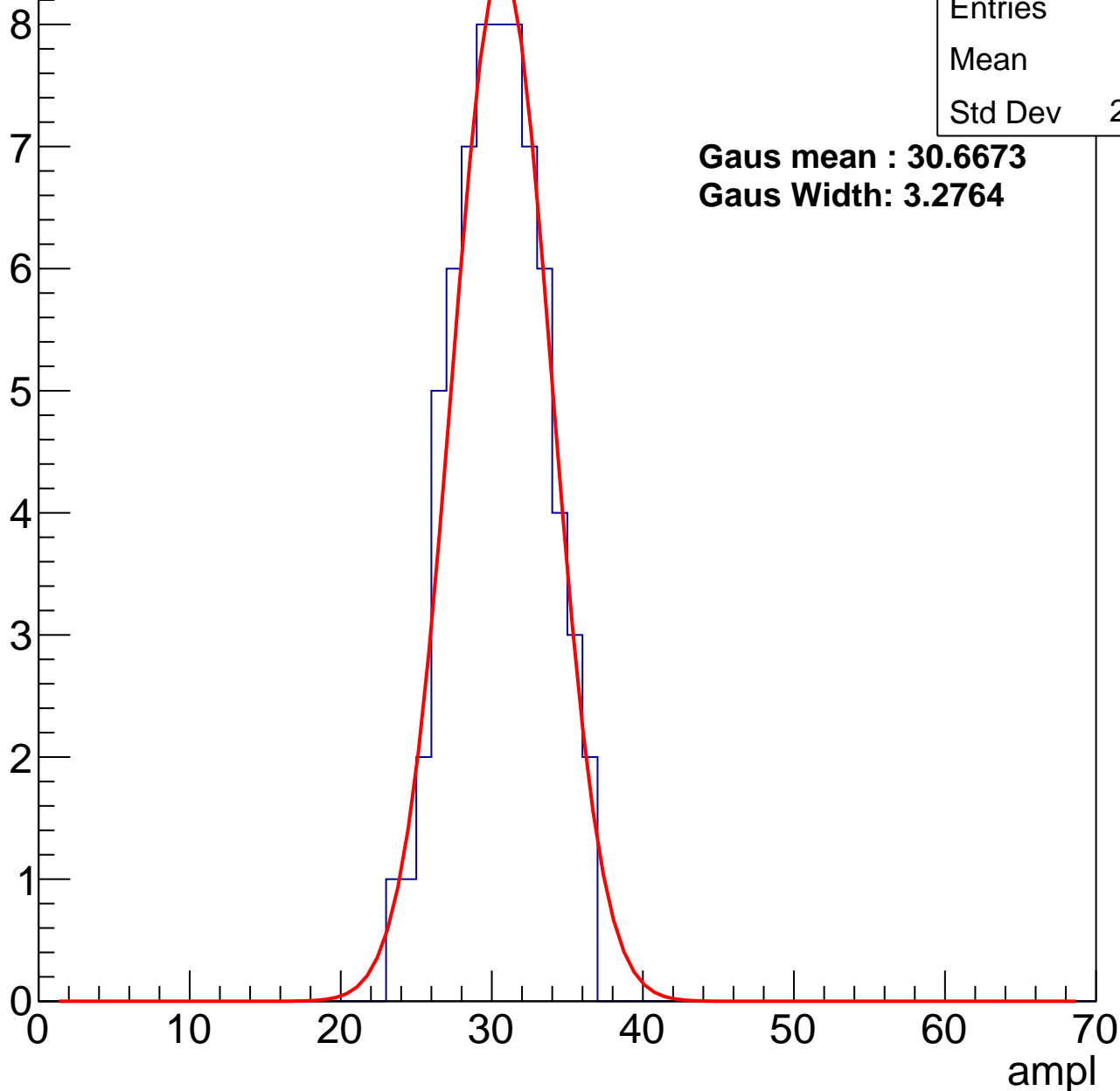
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	68
Mean	30
Std Dev	2.985

**Gaus mean : 30.6673**

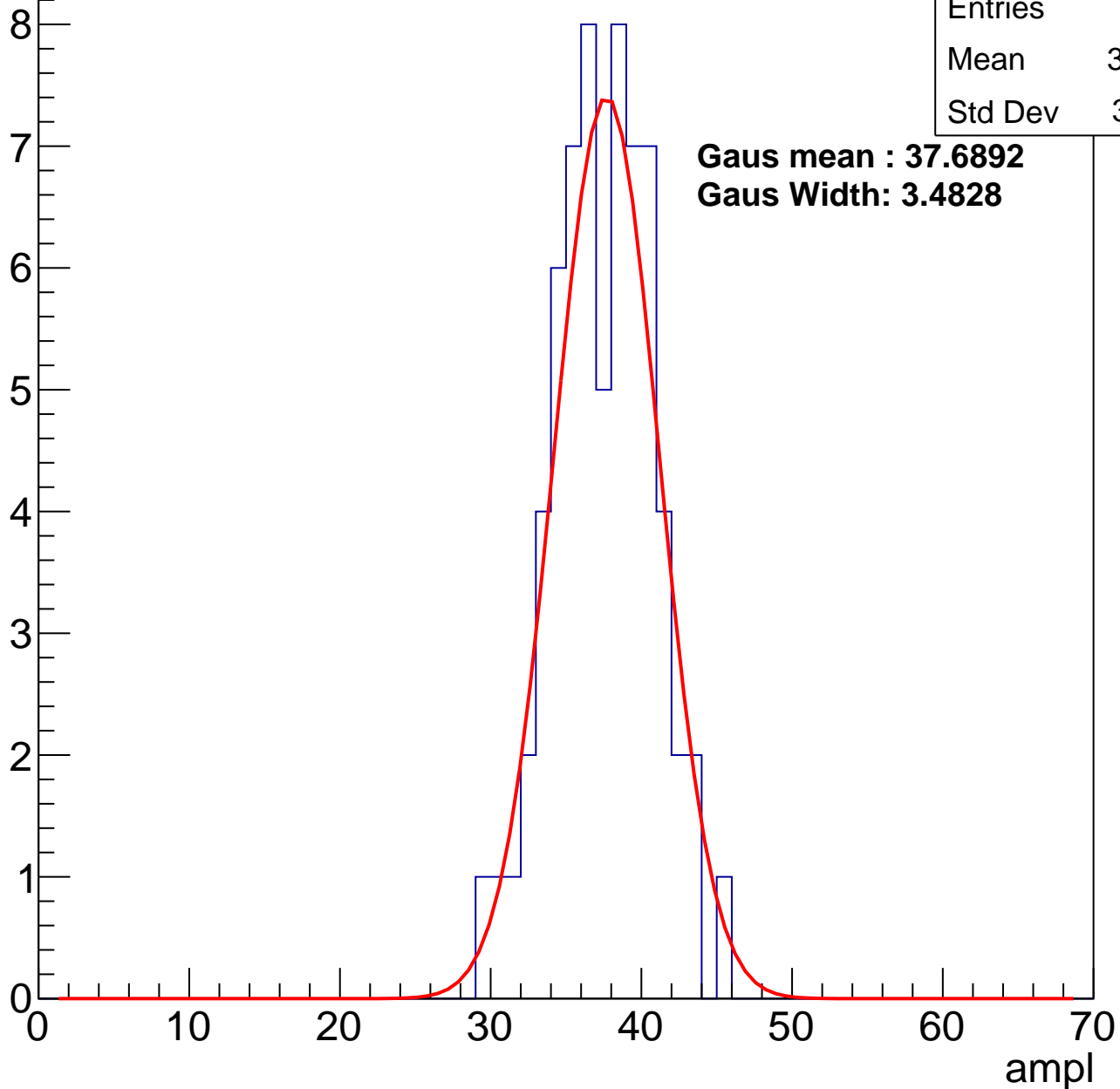
**Gaus Width: 3.2764**



# B1L100S, U2-ch1, adc1

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



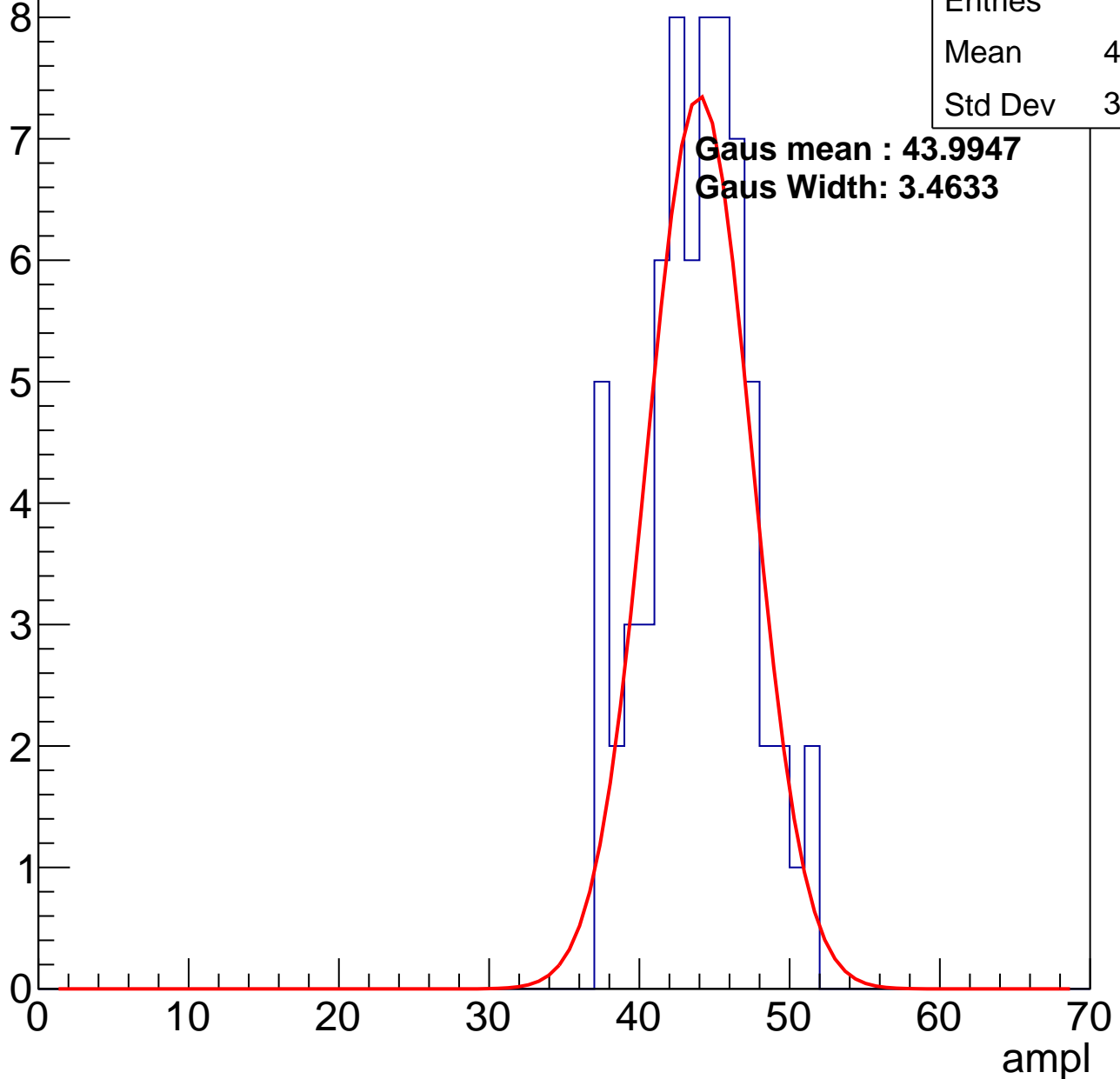
# B1L100S, U2-ch1, adc2

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	68
Mean	43.43
Std Dev	3.444

**Gaus mean : 43.9947**  
**Gaus Width: 3.4633**

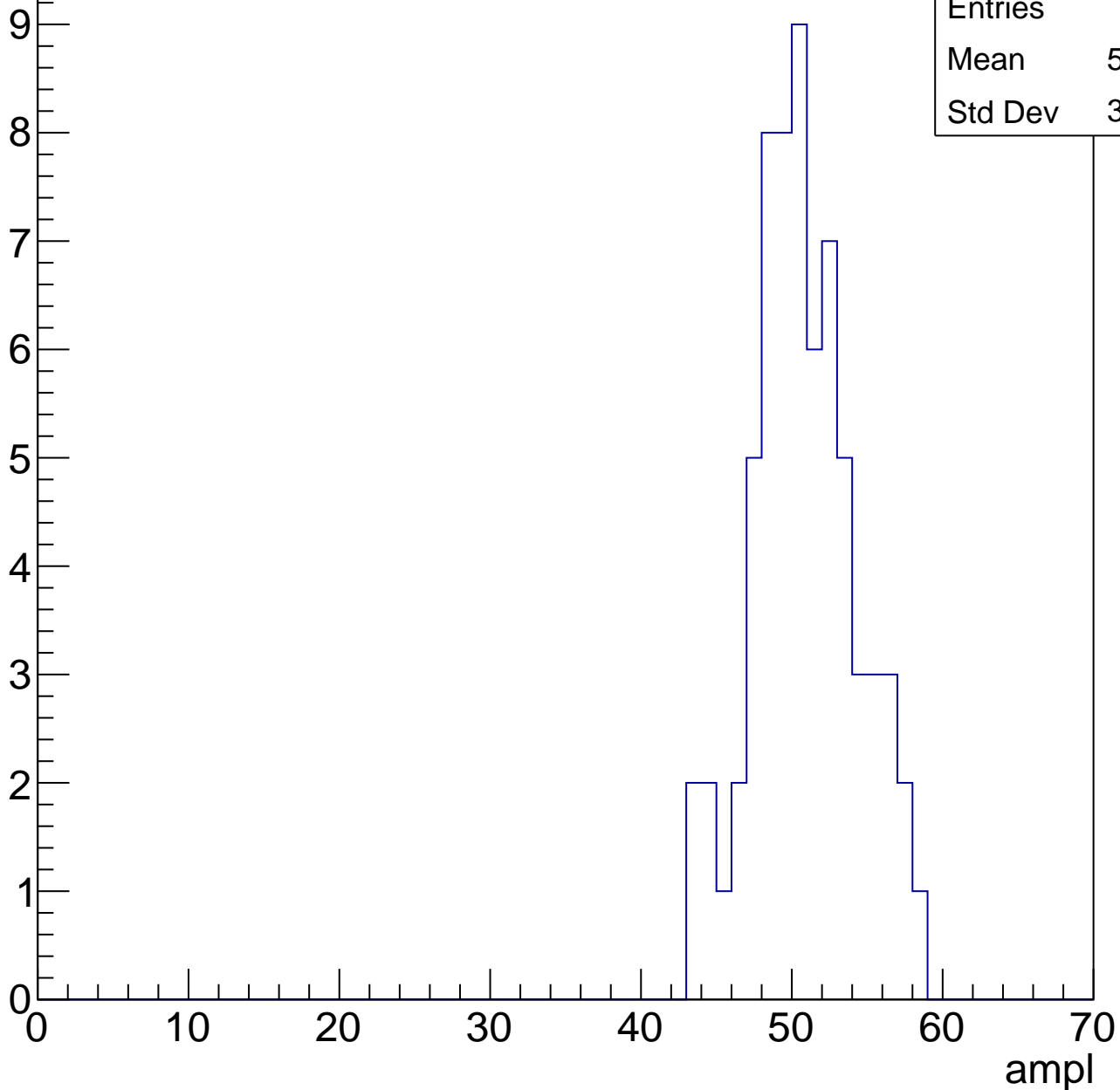


# B1L100S, U2-ch1, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	67
Mean	50.36
Std Dev	3.402

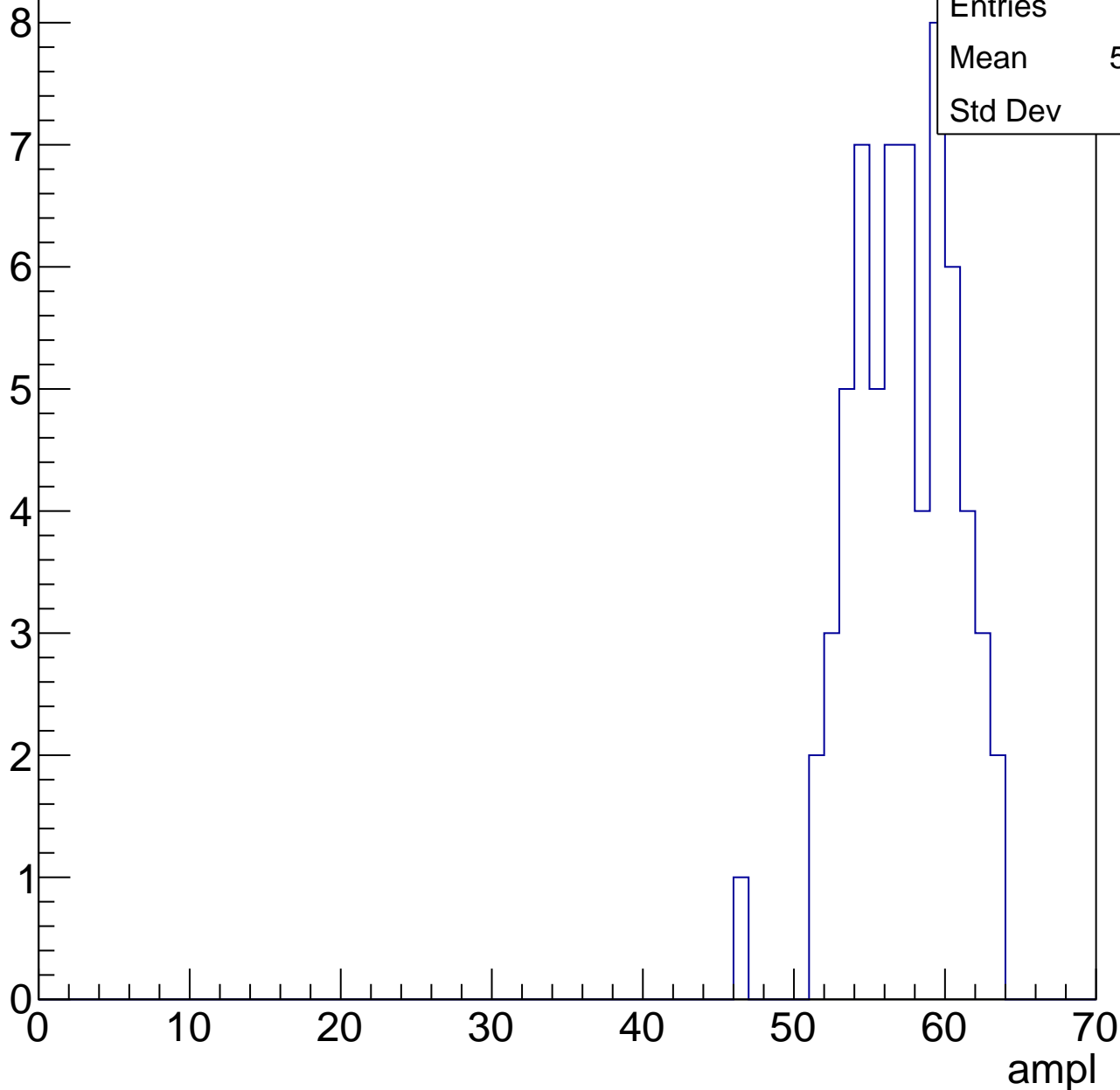


# B1L100S, U2-ch1, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	64
Mean	56.77
Std Dev	3.39

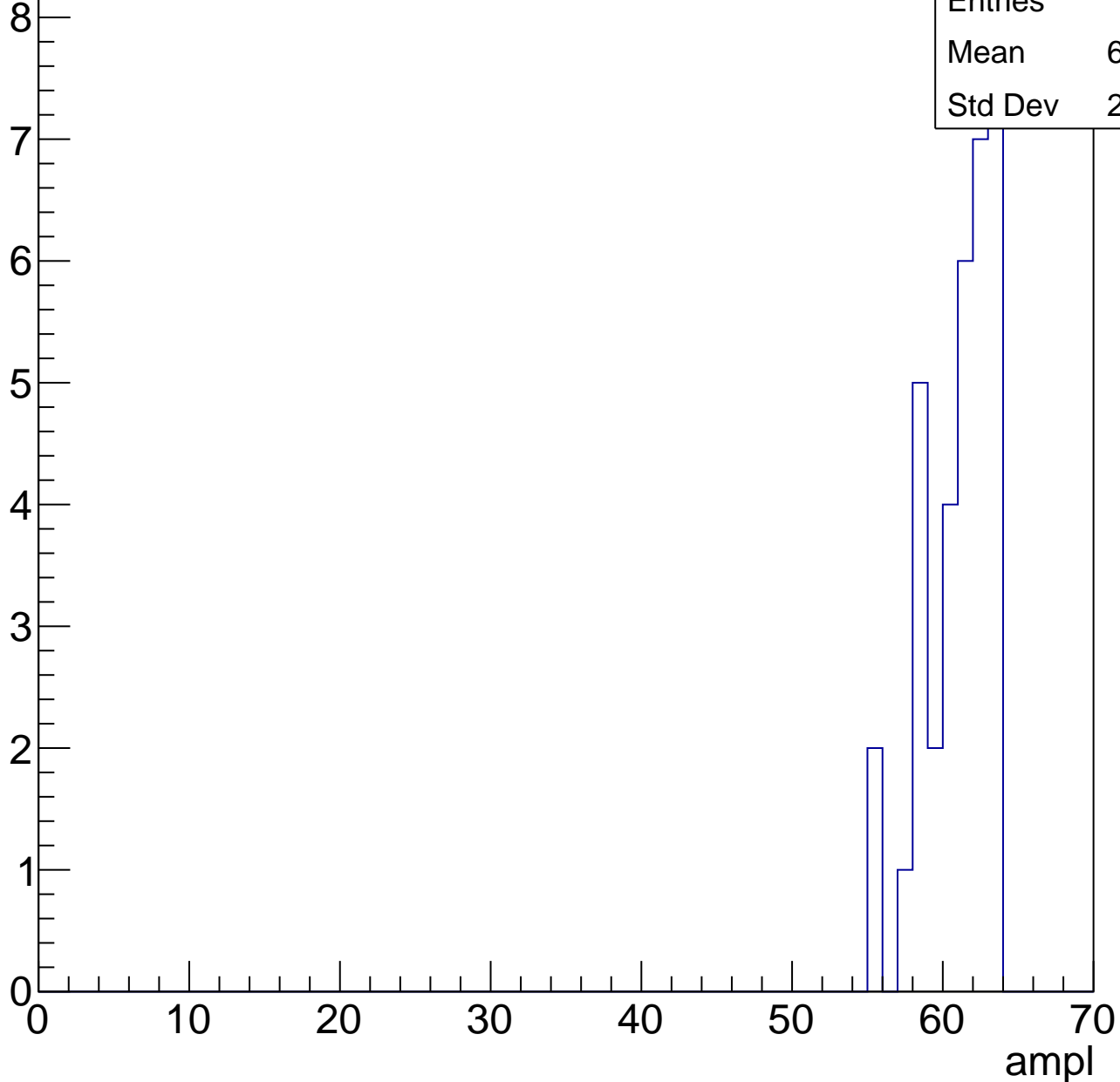


# B1L100S, U2-ch1, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	35
Mean	60.54
Std Dev	2.247



# B1L100S, U2-ch1, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry





# B1L100S, U2-ch1, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



# B1L100S, U2-ch2, adc0

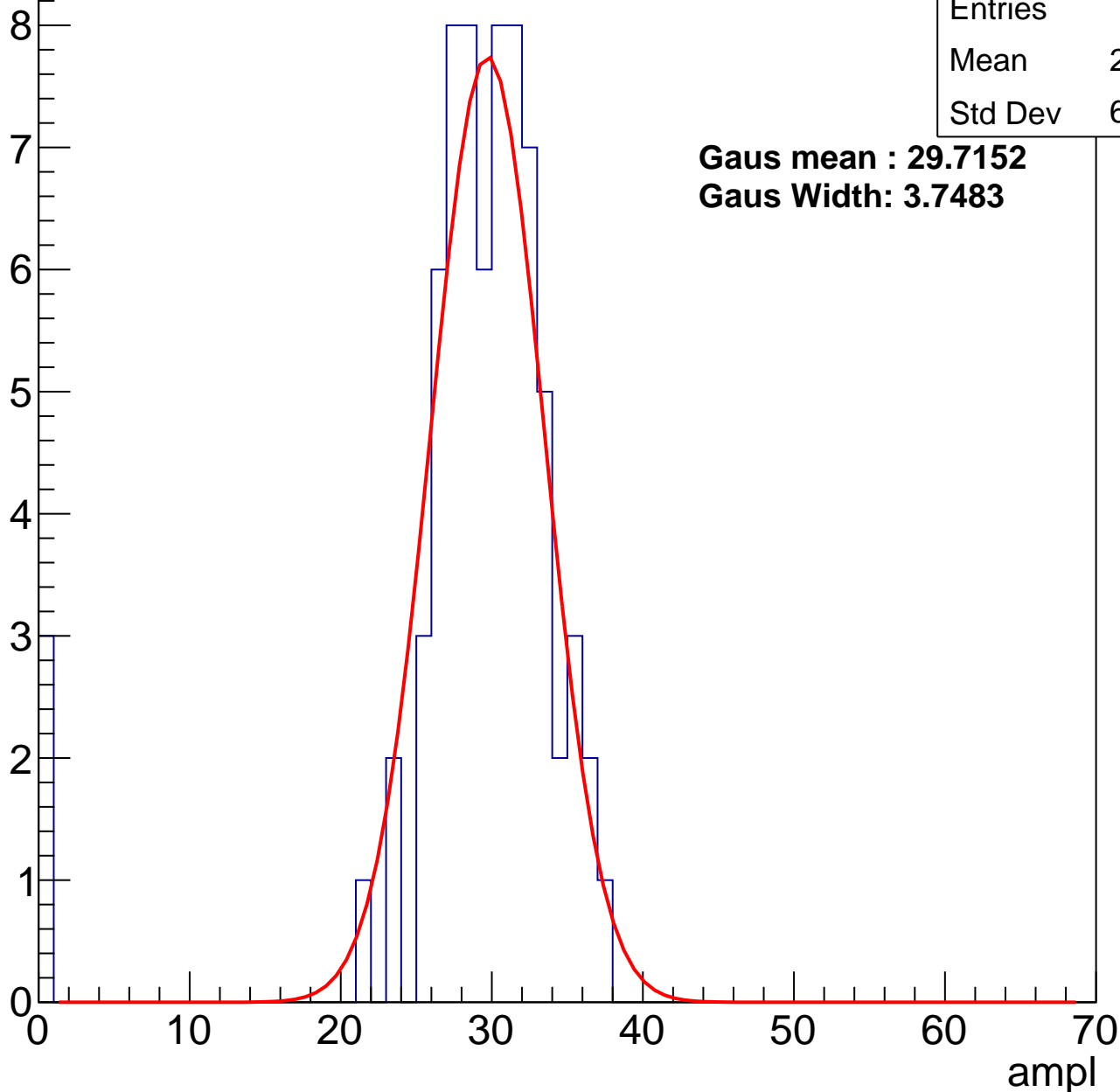
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	73
Mean	28.37
Std Dev	6.698

**Gaus mean : 29.7152**

**Gaus Width: 3.7483**



# B1L100S, U2-ch2, adc1

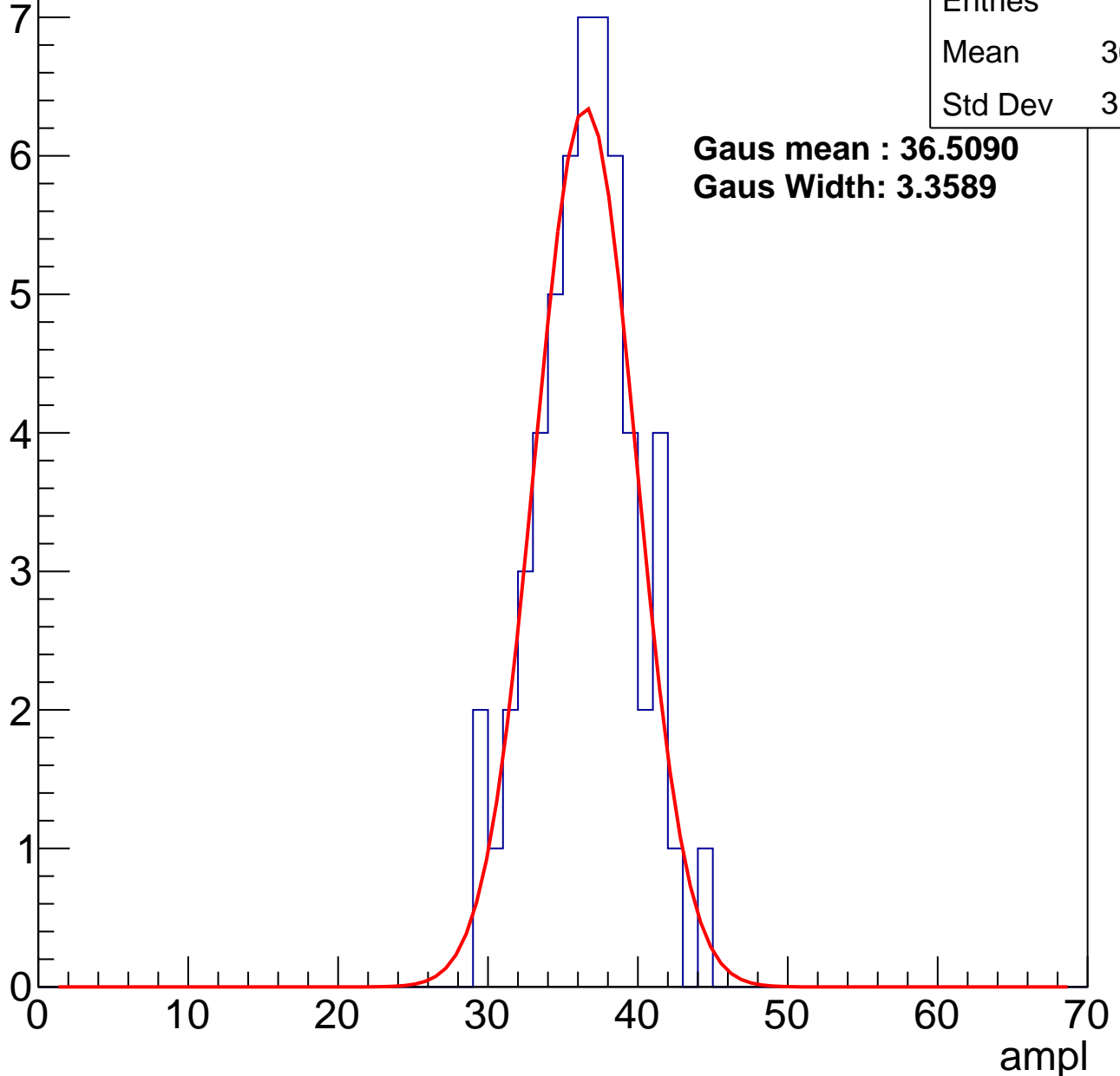
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	55
Mean	36.05
Std Dev	3.283

**Gaus mean : 36.5090**

**Gaus Width: 3.3589**



# B1L100S, U2-ch2, adc2

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	82
Mean	42.41
Std Dev	3.895

**Gaus mean : 43.2270**

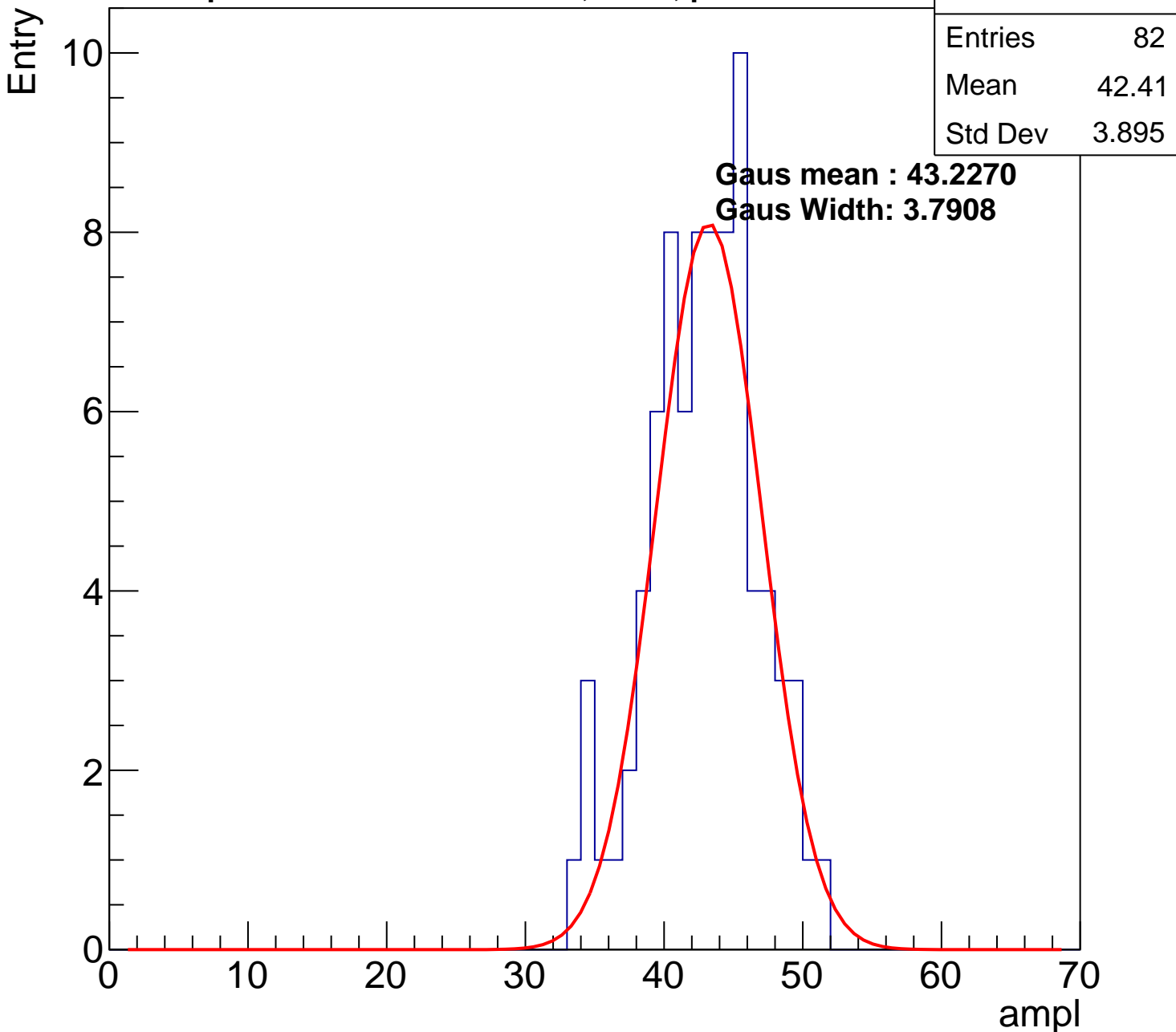
**Gaus Width: 3.7908**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

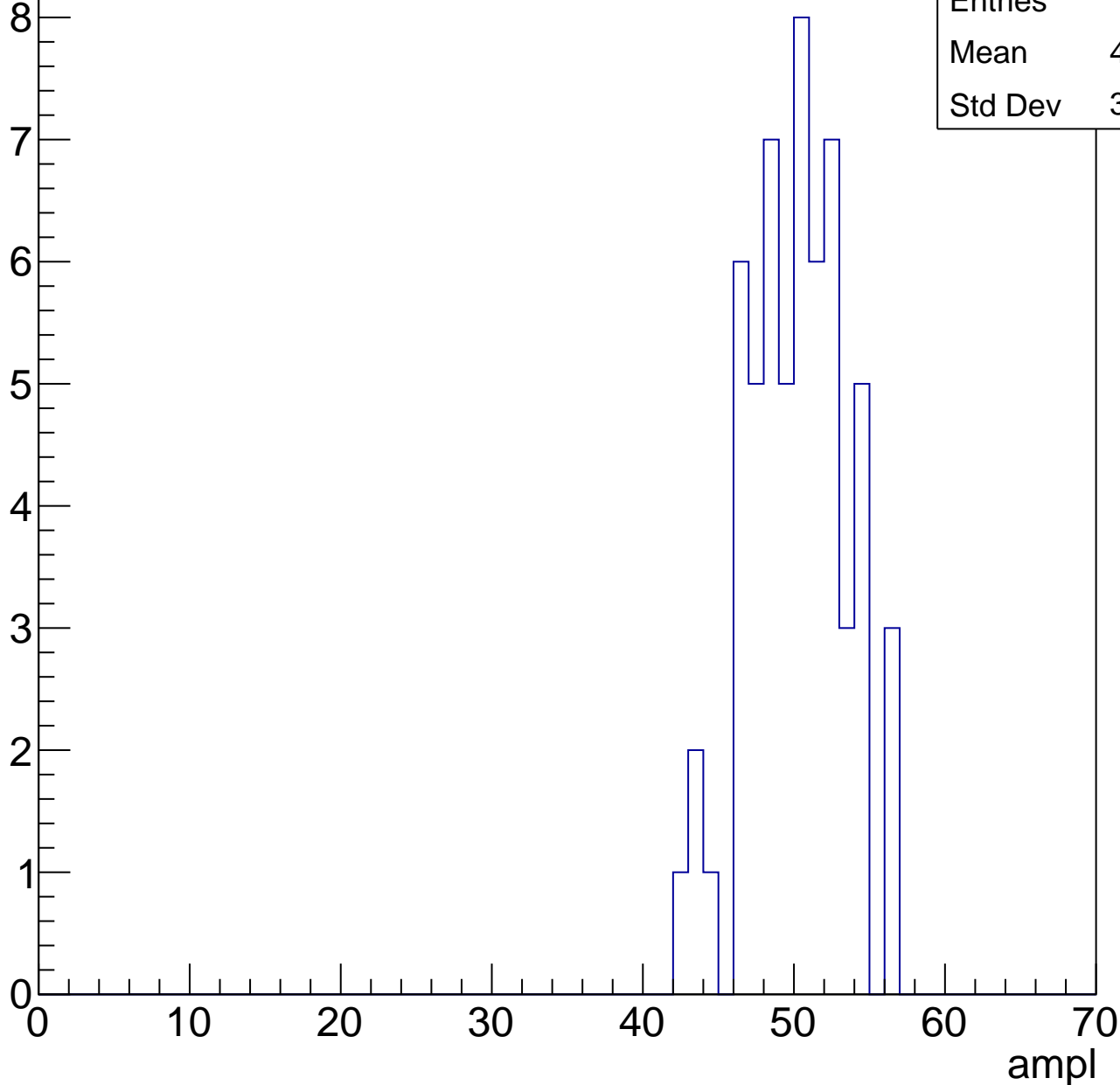


# B1L100S, U2-ch2, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	59
Mean	49.68
Std Dev	3.228

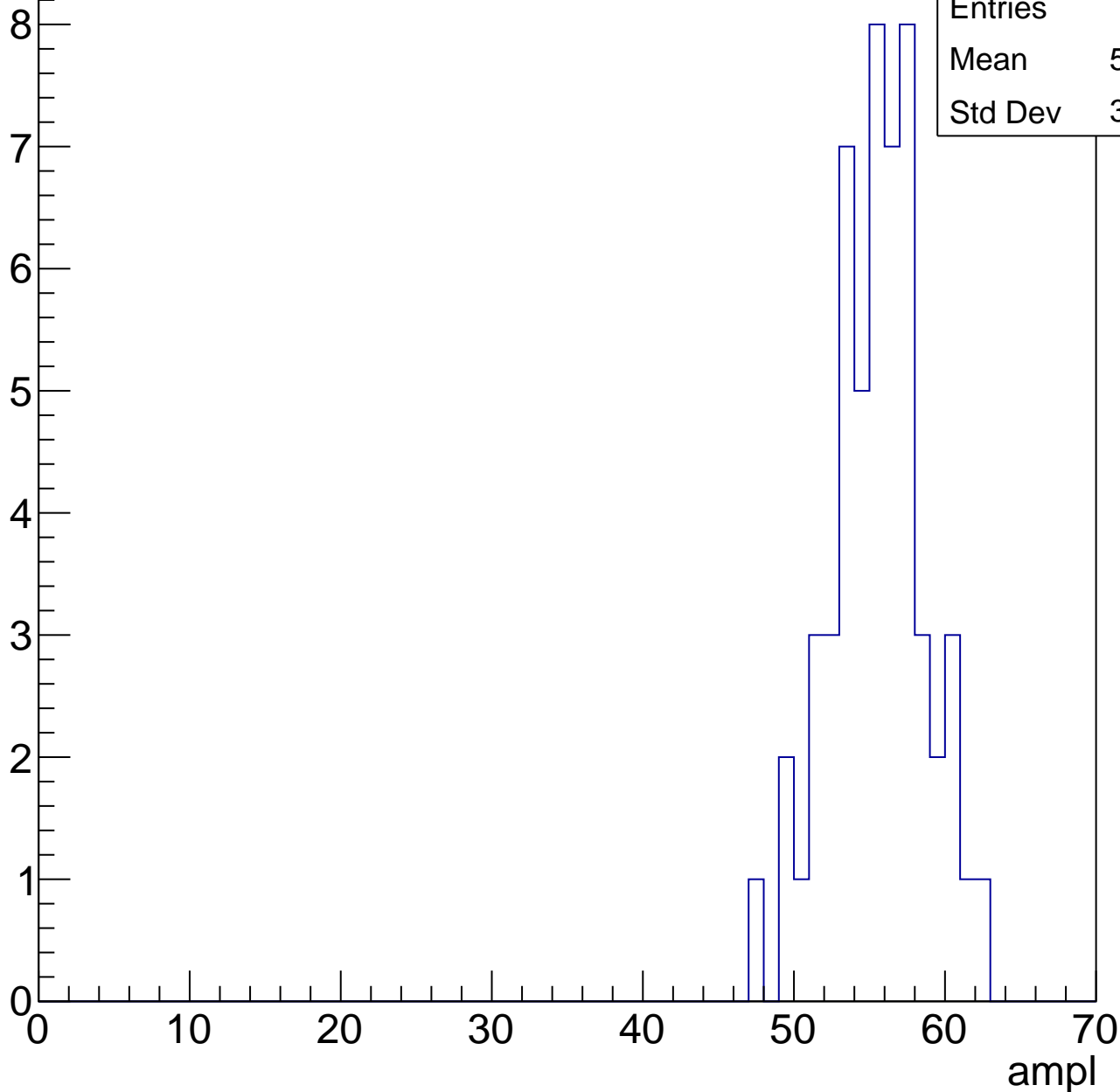


# B1L100S, U2-ch2, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	55
Mean	55.05
Std Dev	3.095

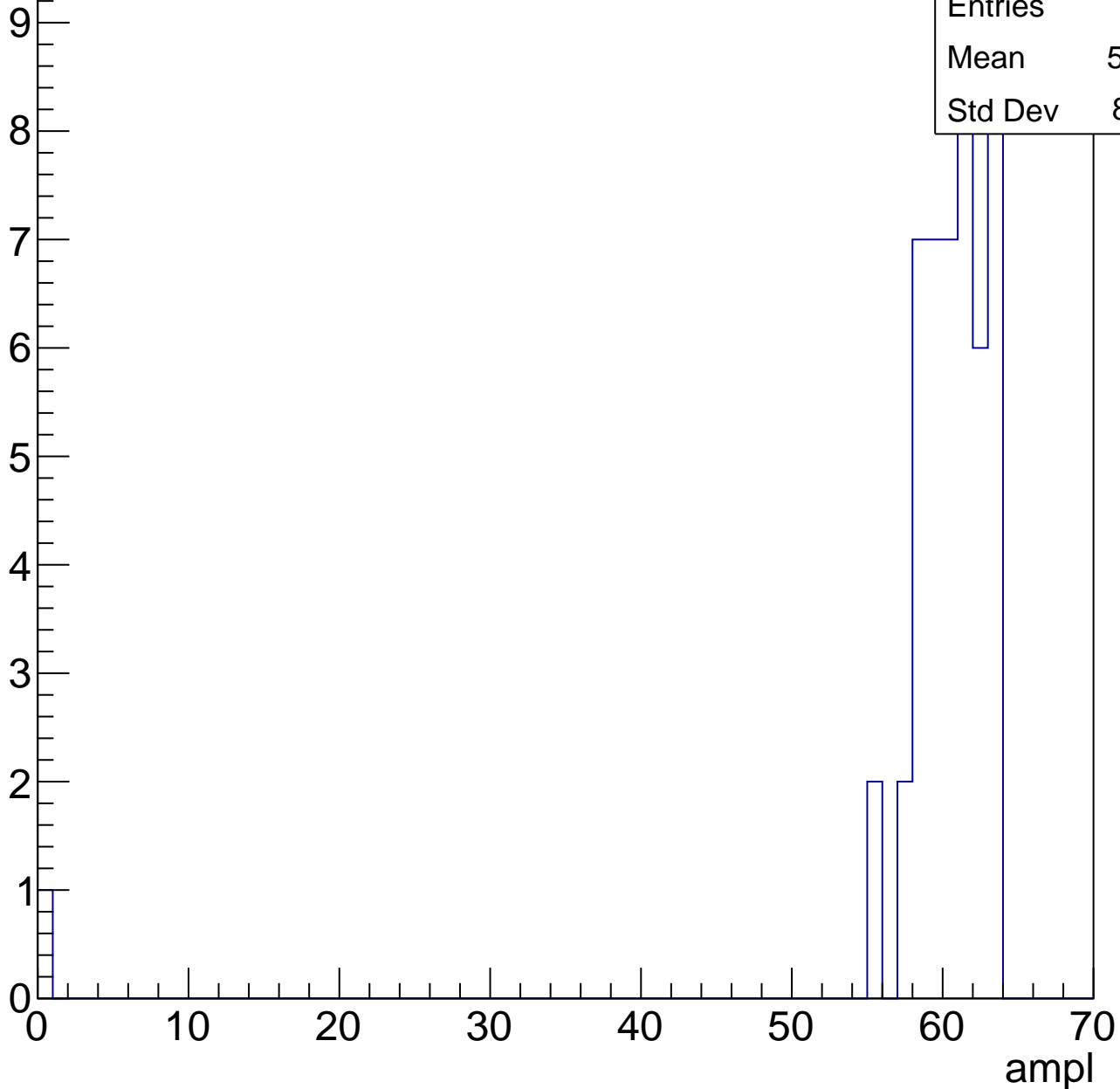


# B1L100S, U2-ch2, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

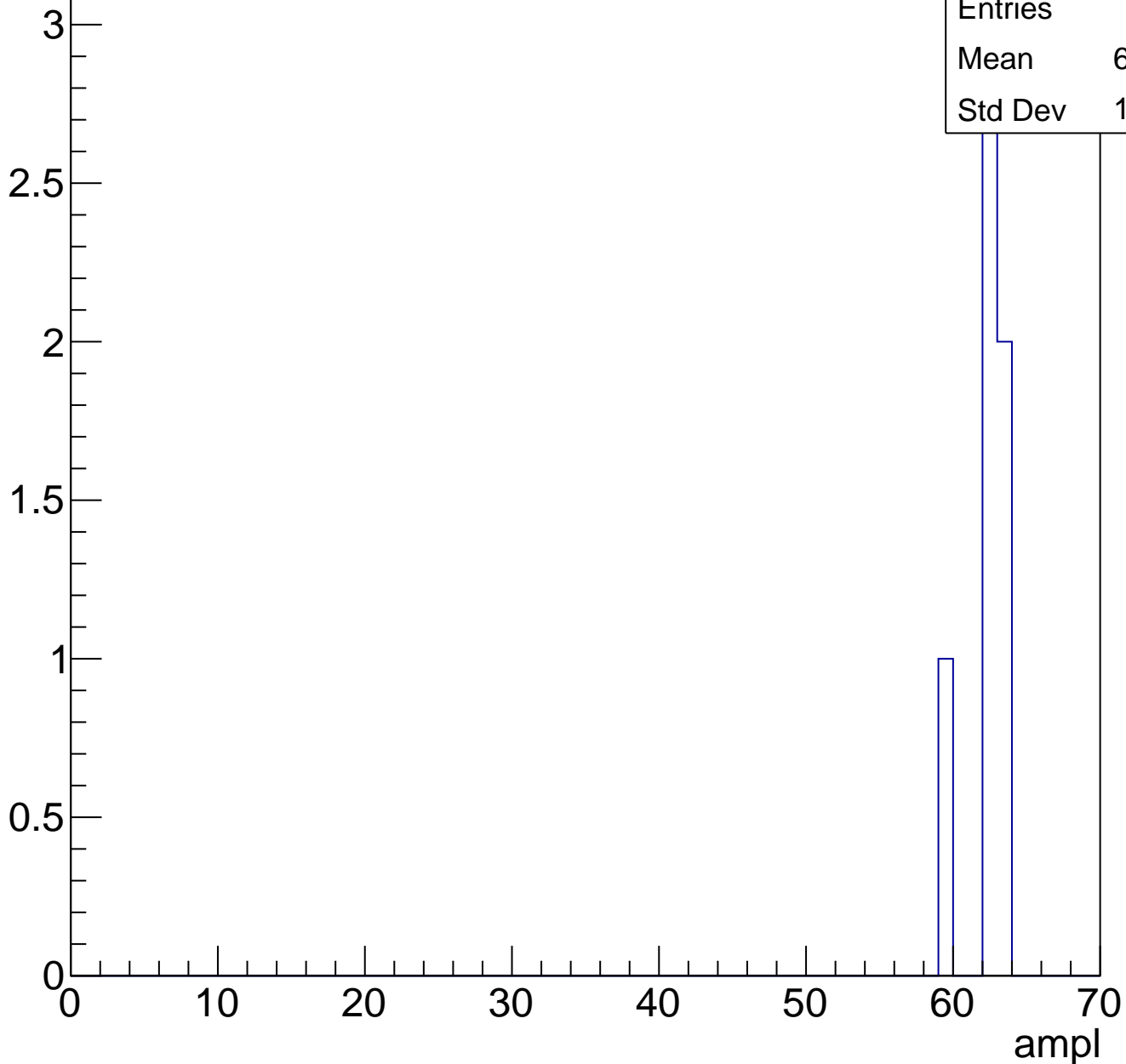
Entries	49
Mean	58.94
Std Dev	8.751



# B1L100S, U2-ch2, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry





# B1L100S, U2-ch2, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



# B1L100S, U2-ch3, adc0

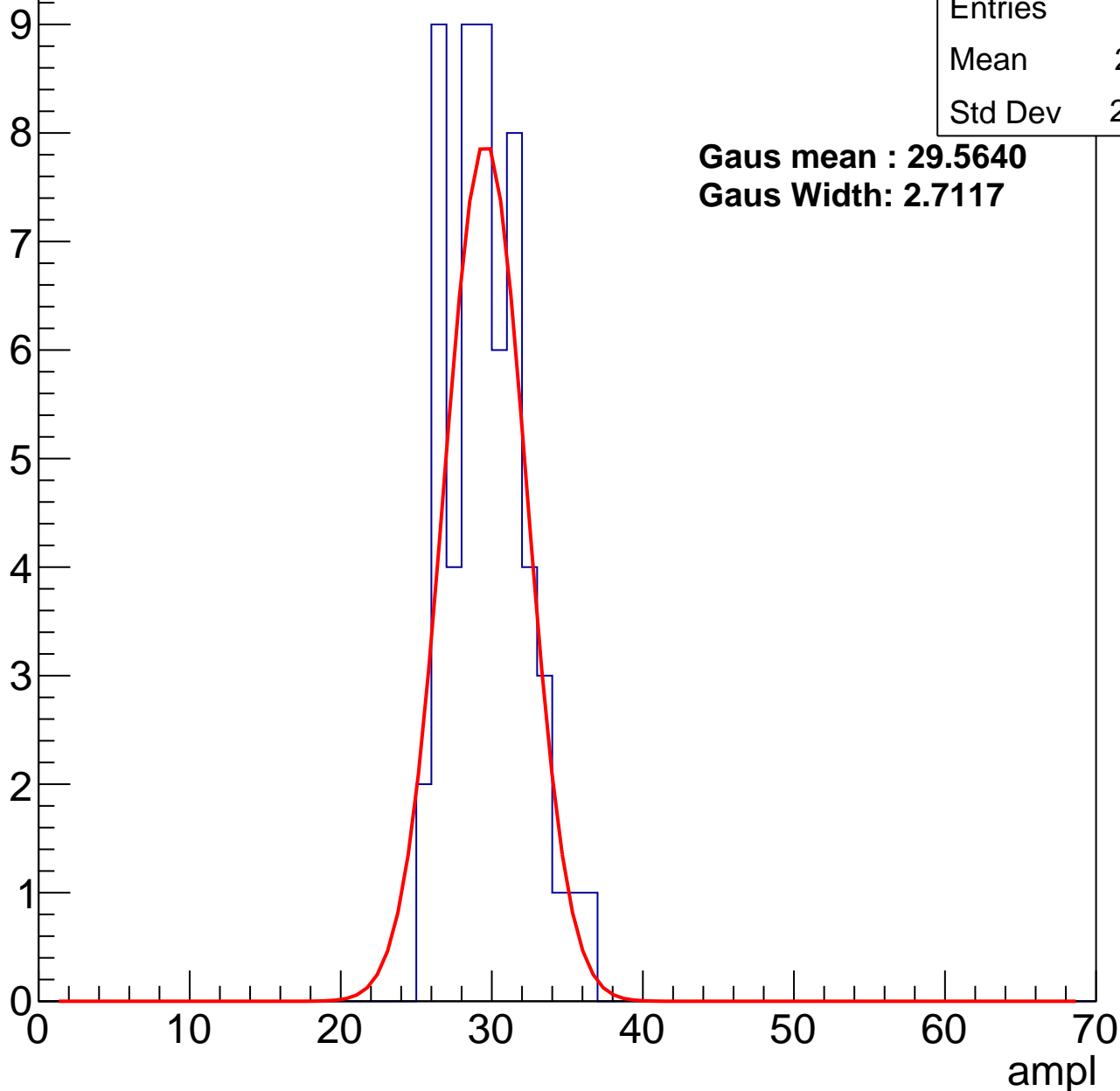
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	57
Mean	29.21
Std Dev	2.539

**Gaus mean : 29.5640**

**Gaus Width: 2.7117**



# B1L100S, U2-ch3, adc1

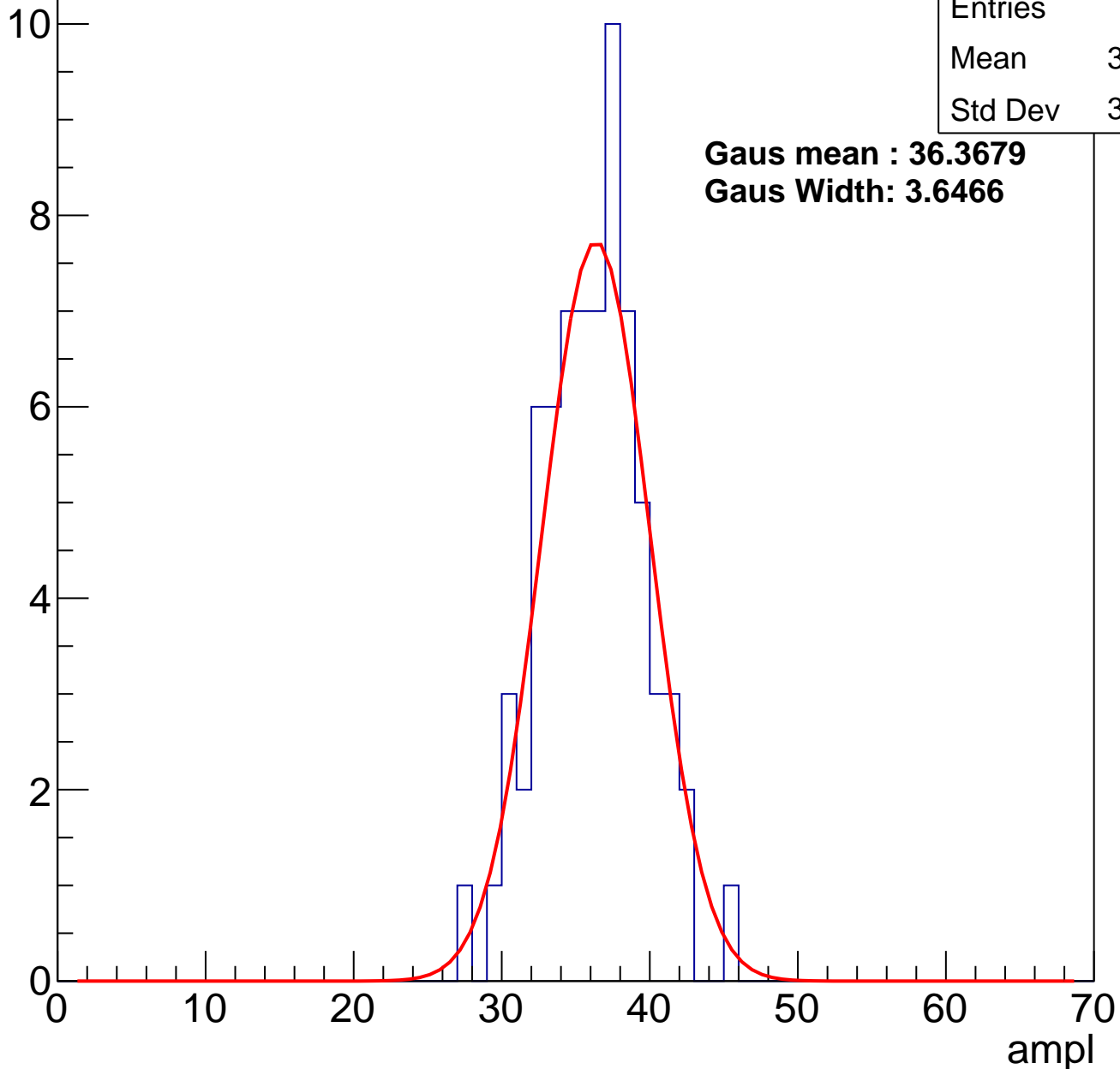
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	71
Mean	35.72
Std Dev	3.412

**Gaus mean : 36.3679**

**Gaus Width: 3.6466**

Entry



# B1L100S, U2-ch3, adc2

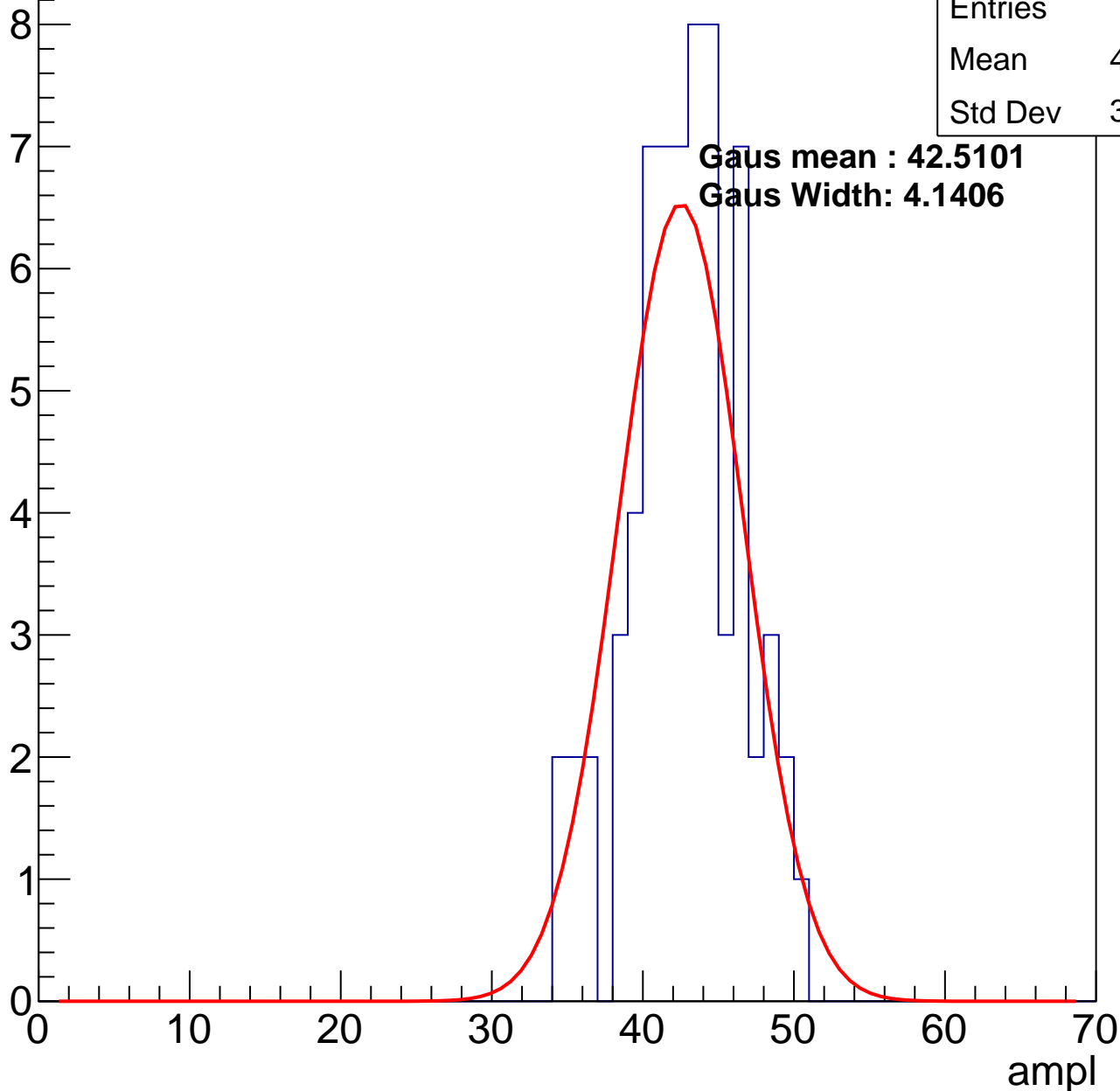
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	68
Mean	42.35
Std Dev	3.653

**Gaus mean : 42.5101**

**Gaus Width: 4.1406**

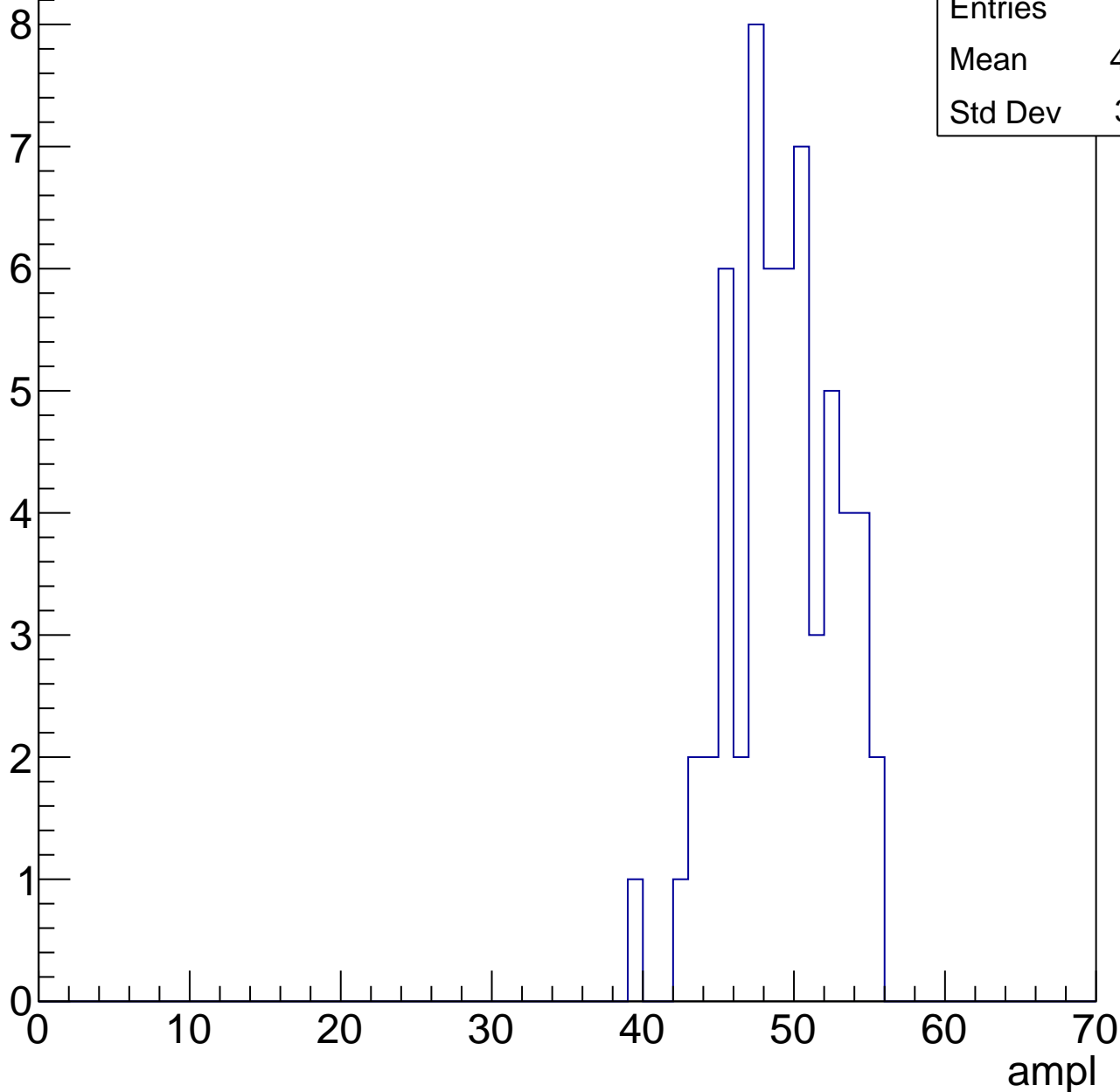


# B1L100S, U2-ch3, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	59
Mean	48.75
Std Dev	3.491

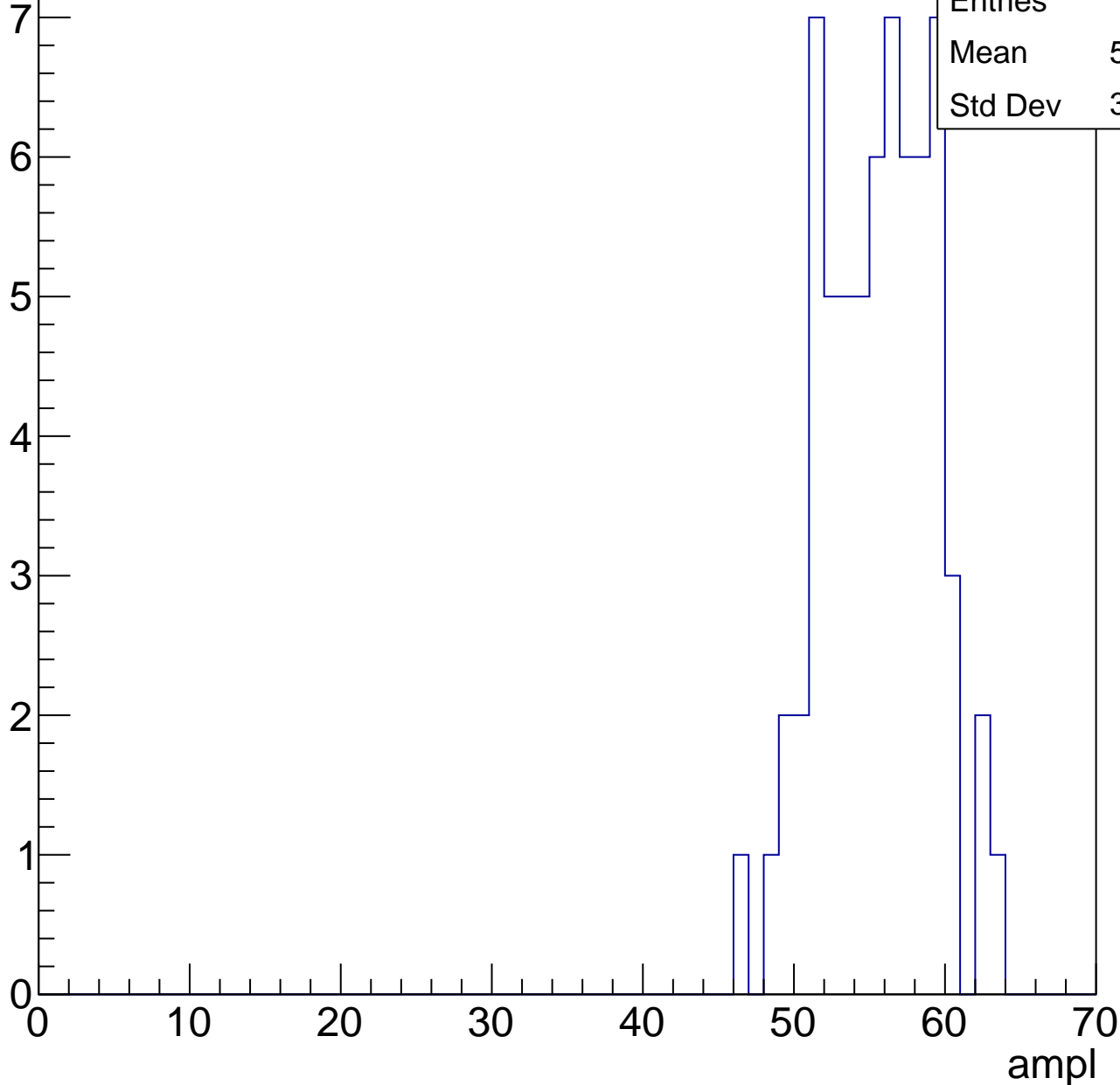


# B1L100S, U2-ch3, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	66
Mean	55.09
Std Dev	3.625

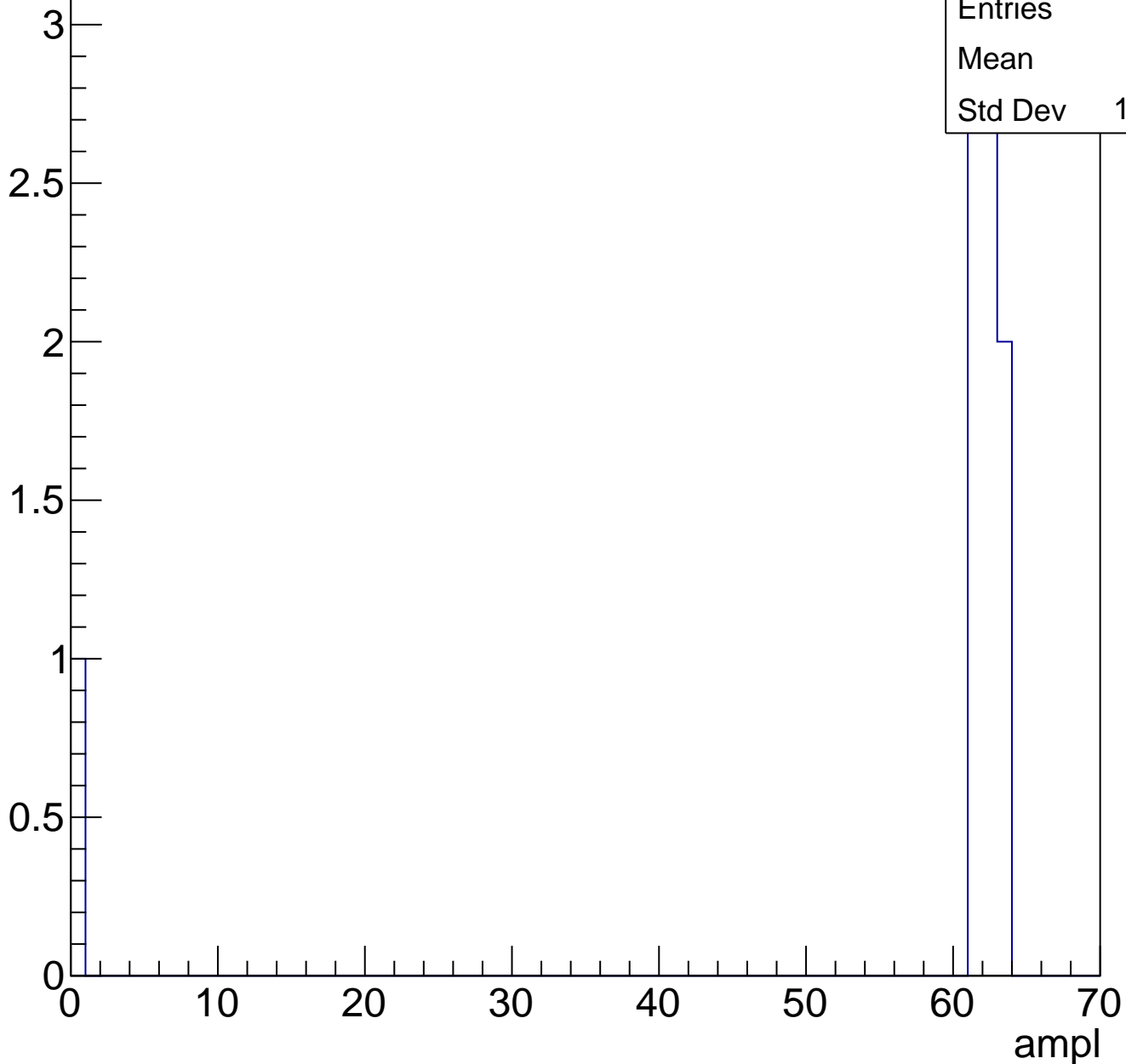




# B1L100S, U2-ch3, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry





# B1L100S, U2-ch3, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



# B1L100S, U2-ch4, adc0

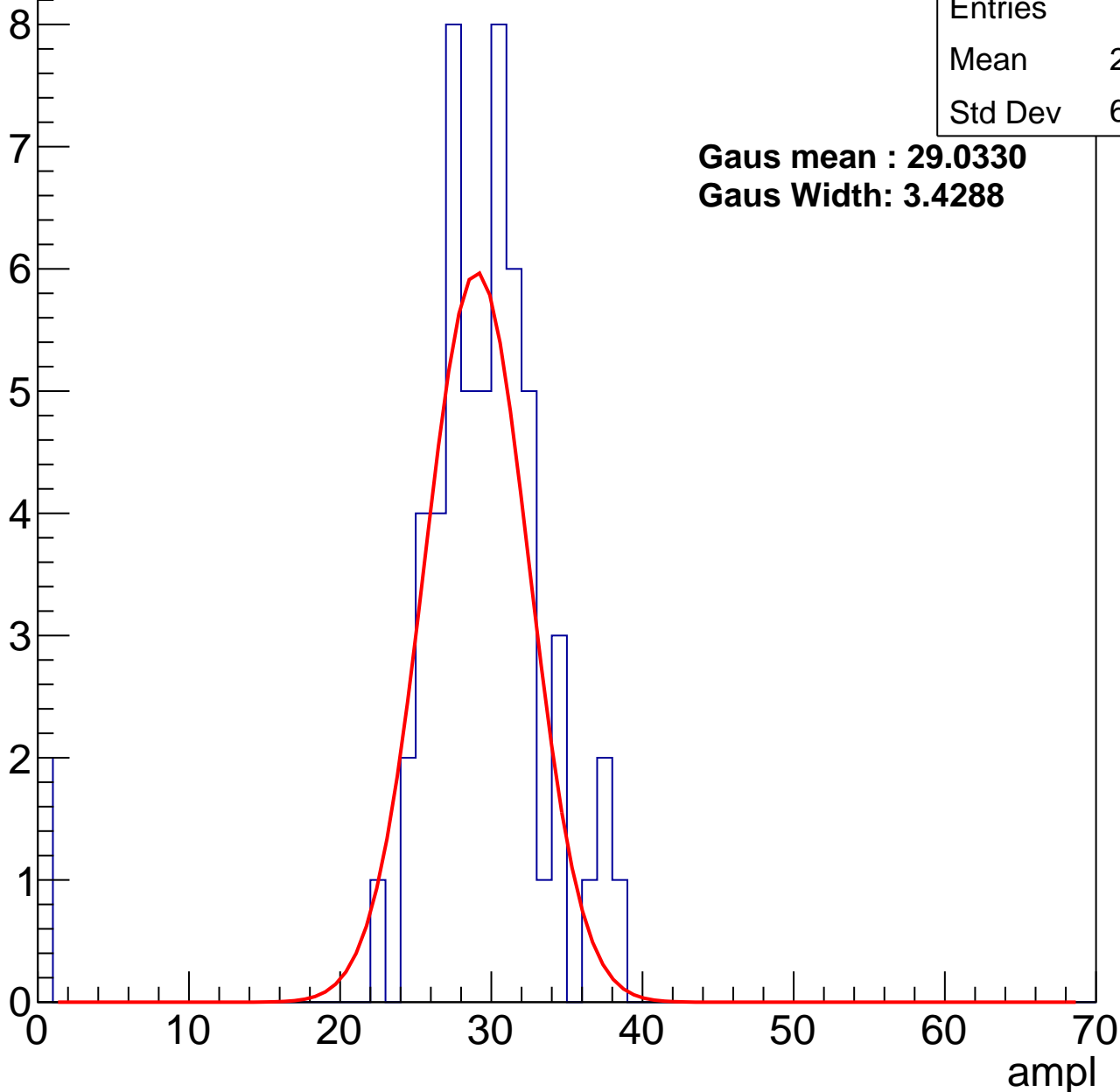
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	58
Mean	28.34
Std Dev	6.323

**Gaus mean : 29.0330**

**Gaus Width: 3.4288**



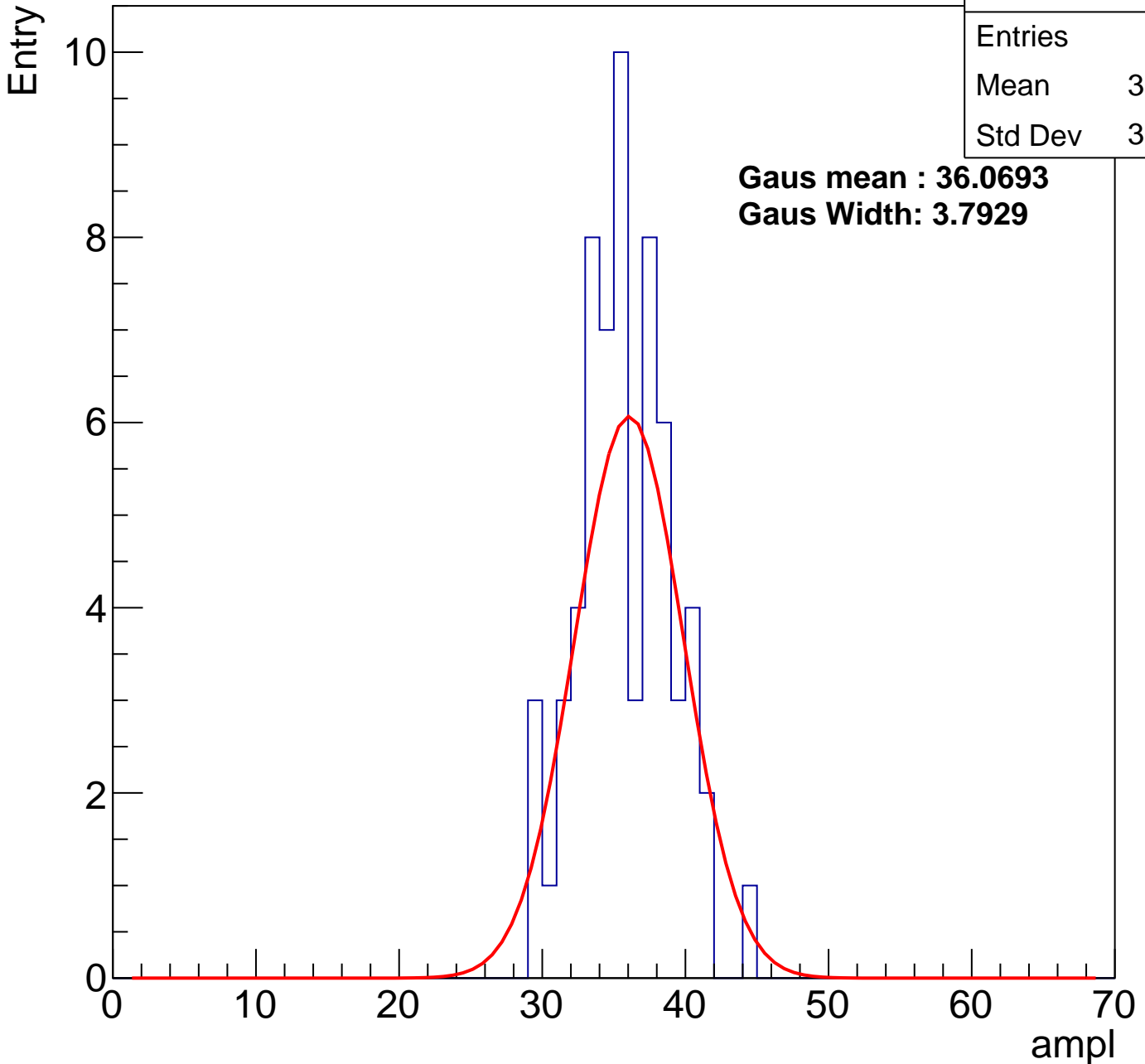
# B1L100S, U2-ch4, adc1

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	63
Mean	35.32
Std Dev	3.186

**Gaus mean : 36.0693**

**Gaus Width: 3.7929**



# B1L100S, U2-ch4, adc2

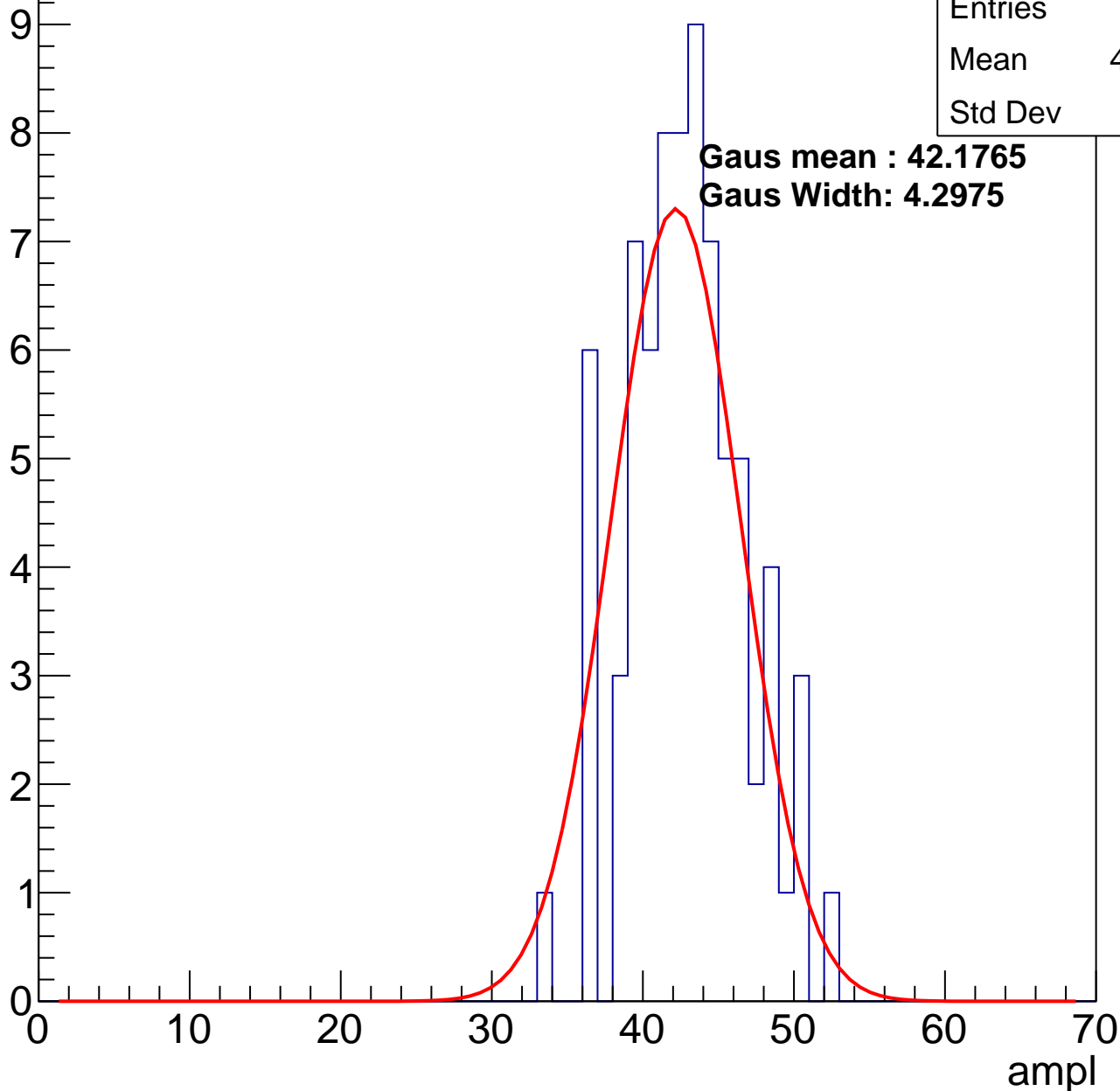
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	76
Mean	42.46
Std Dev	3.84

**Gaus mean : 42.1765**

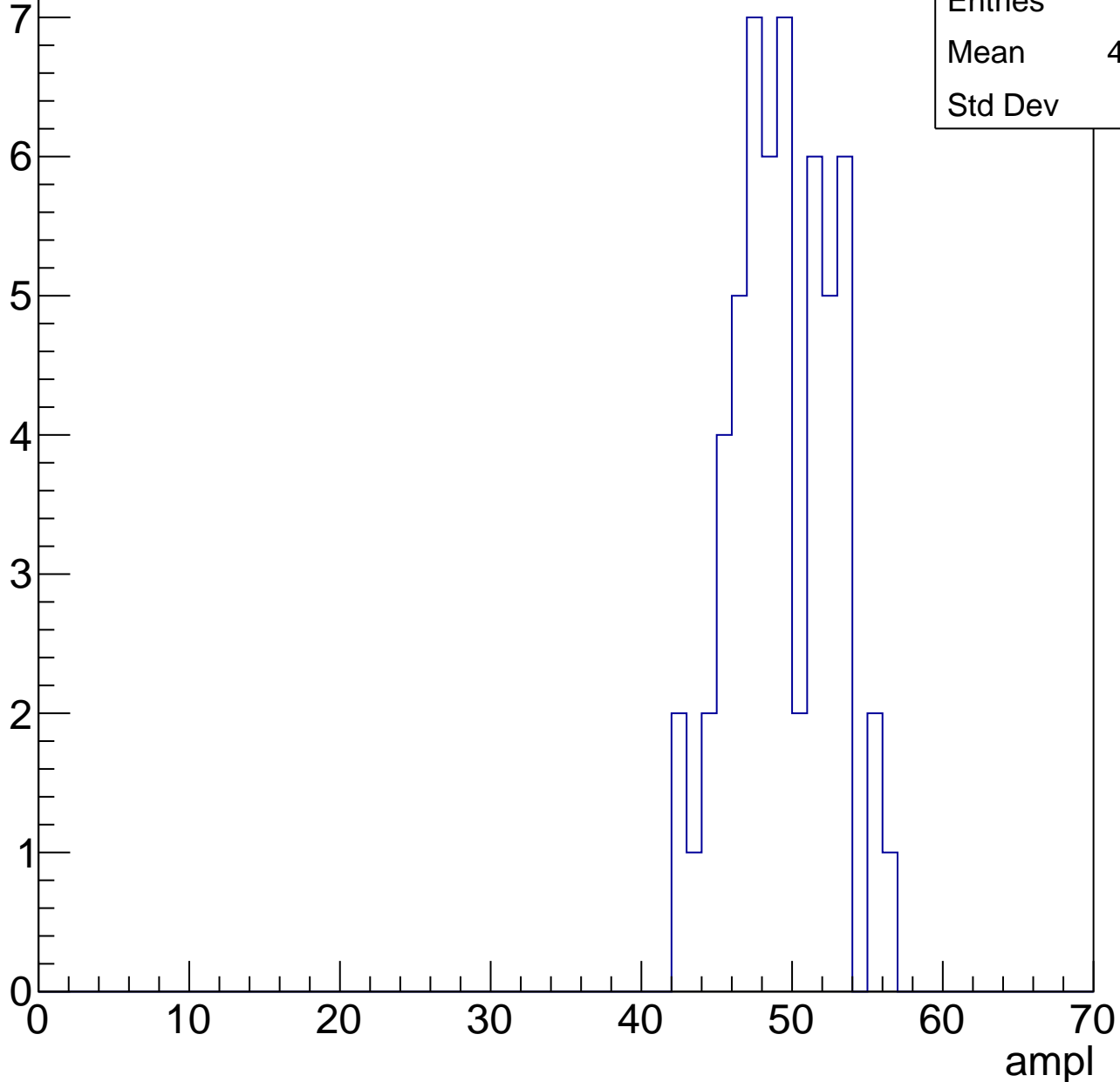
**Gaus Width: 4.2975**



# B1L100S, U2-ch4, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



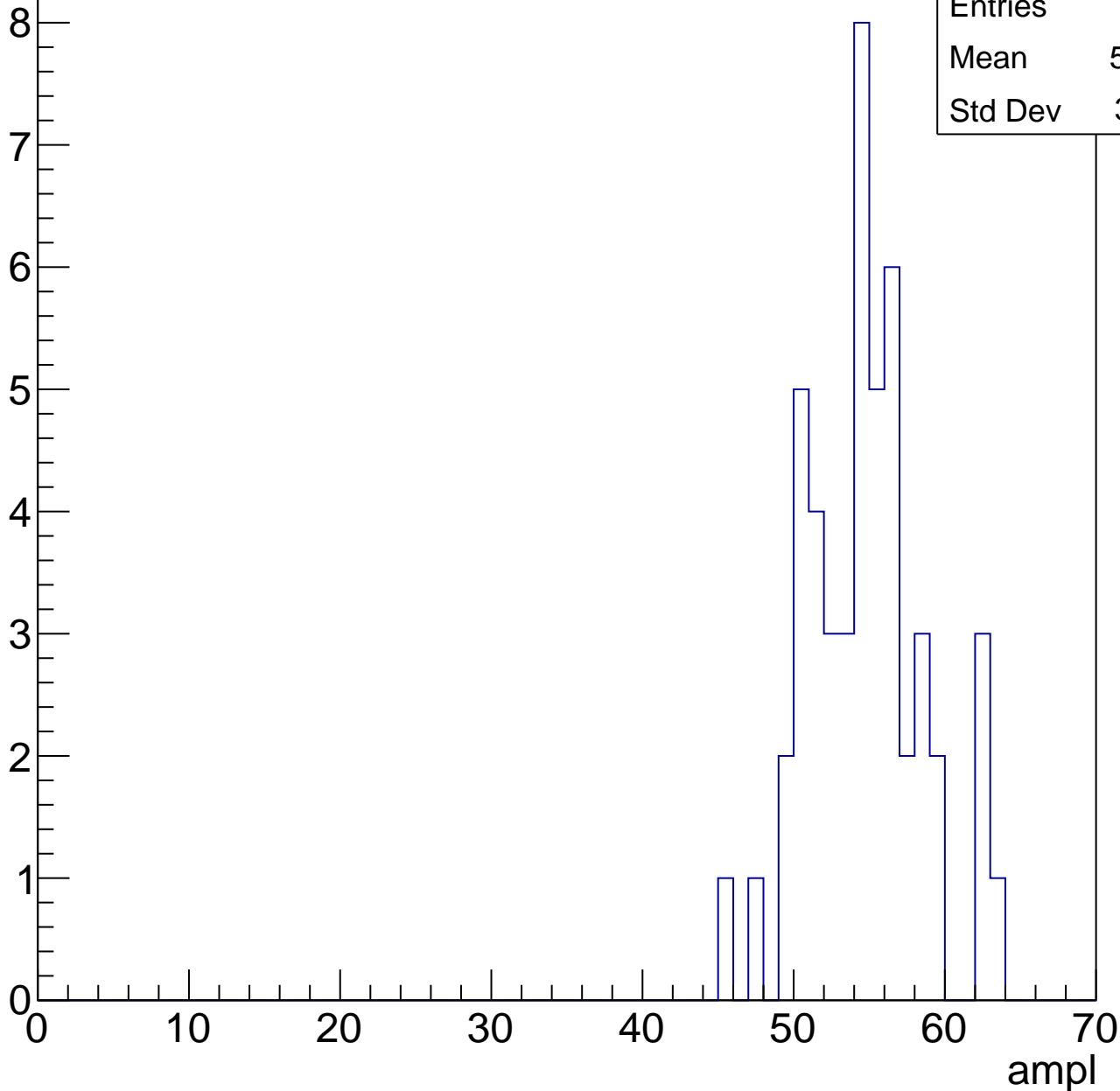
Entries	56
Mean	48.84
Std Dev	3.31

# B1L100S, U2-ch4, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	49
Mean	54.22
Std Dev	3.851



# B1L100S, U2-ch4, adc5

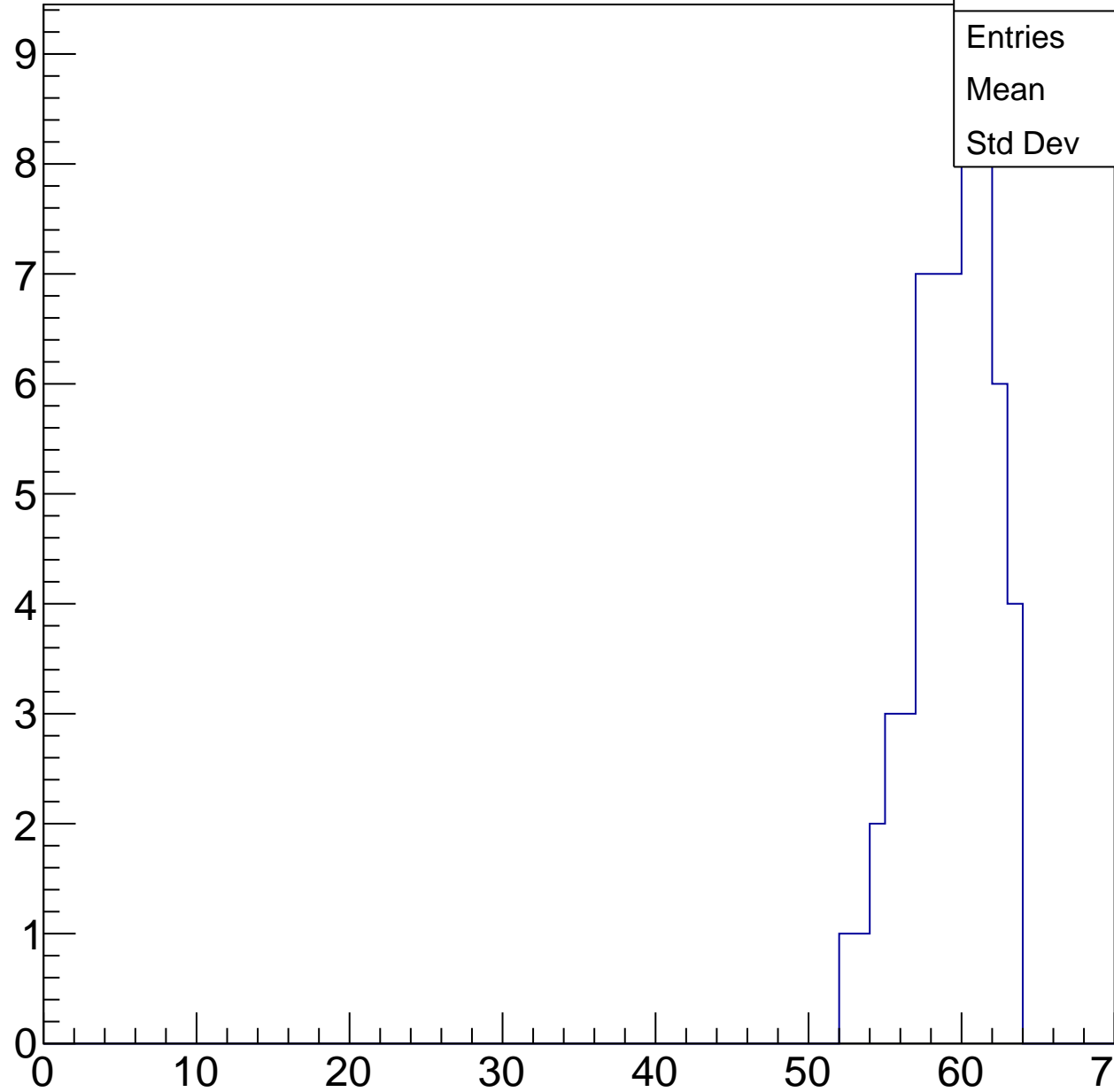
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	58
Mean	58.9
Std Dev	2.637

ampl

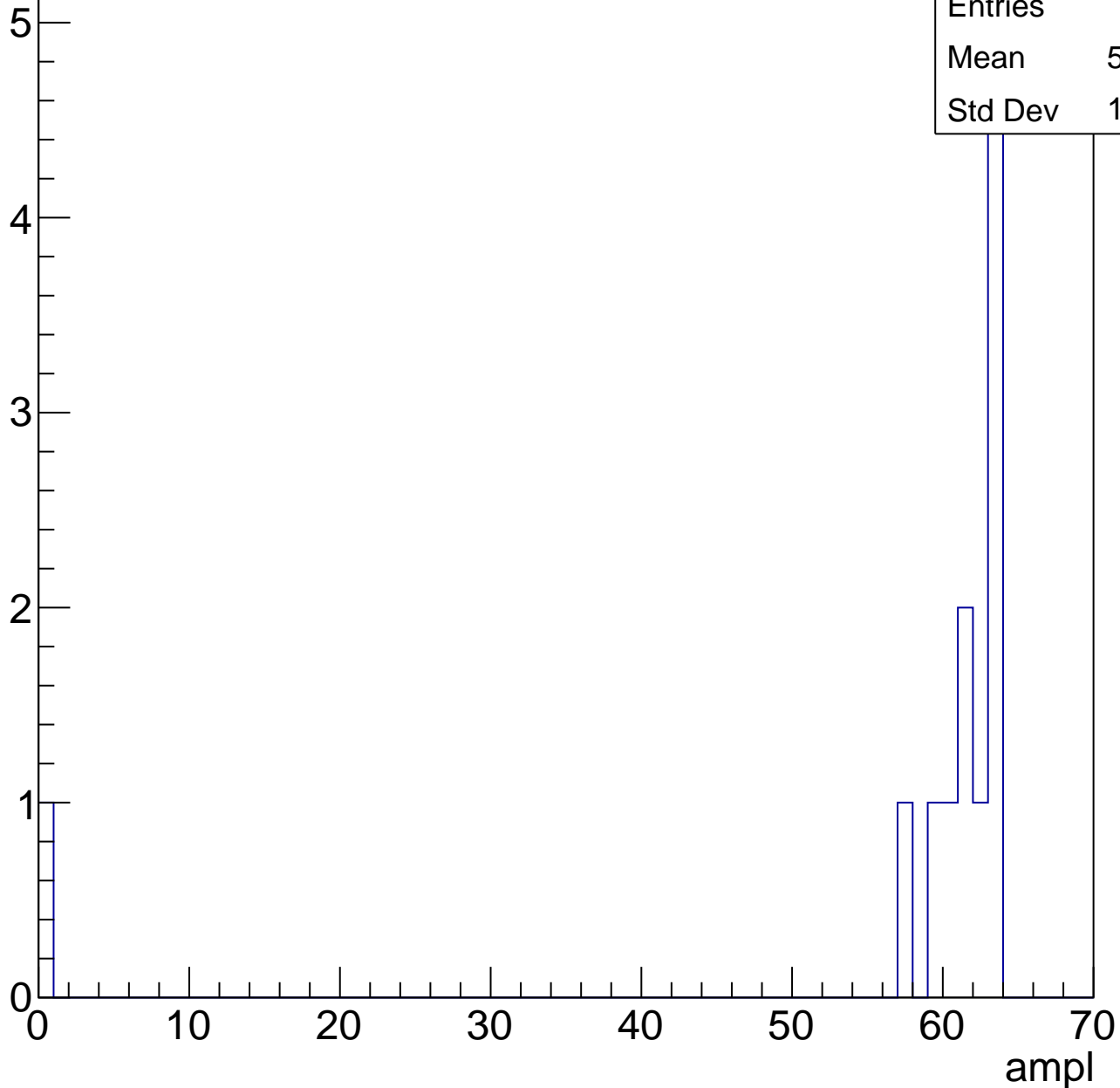


# B1L100S, U2-ch4, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	12
Mean	56.25
Std Dev	17.06





# B1L100S, U2-ch4, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

1  
0.8  
0.6  
0.4  
0.2  
0

Entries	1
Mean	22
Std Dev	0

ampl

# B1L100S, U2-ch5, adc0

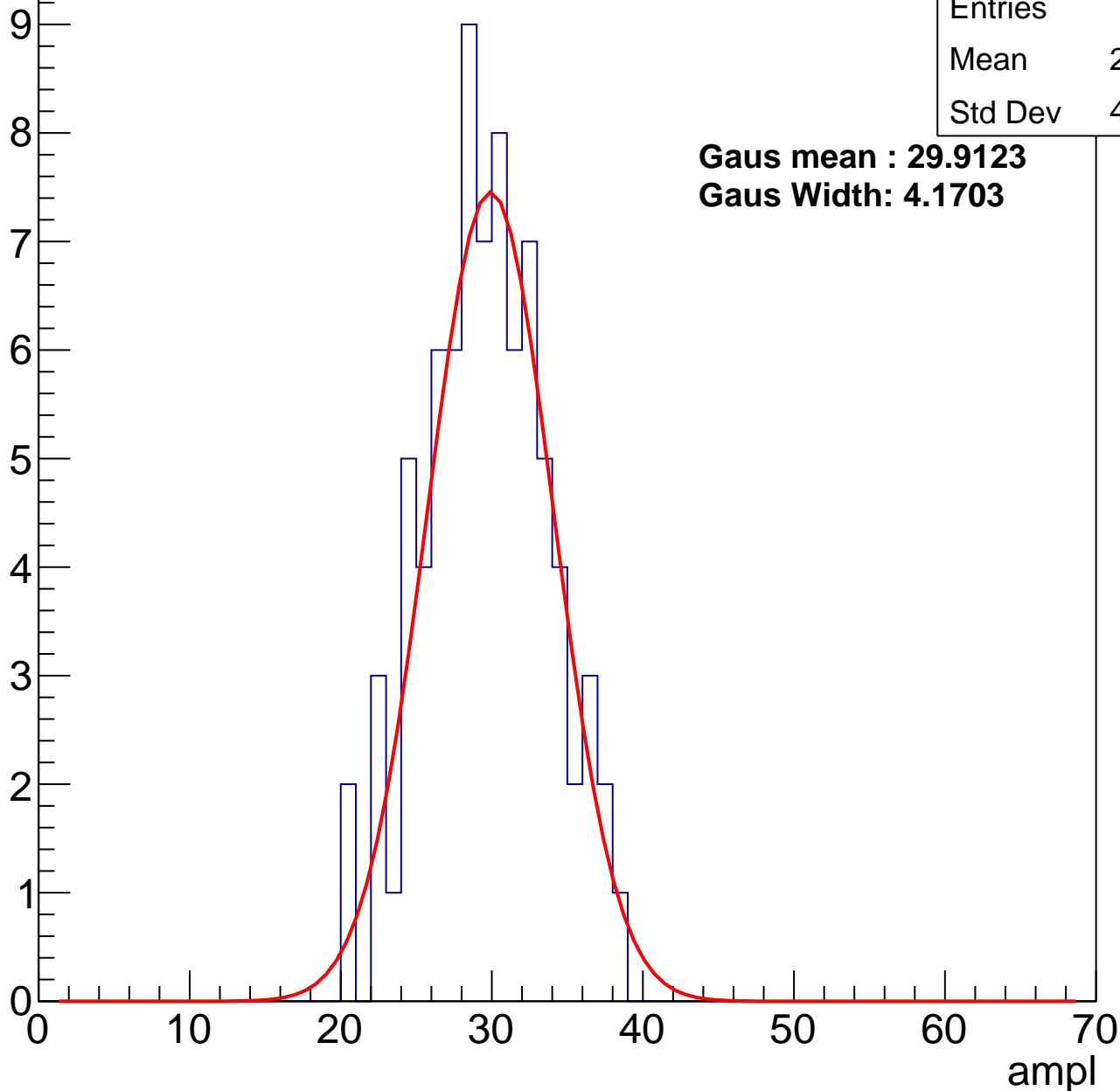
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	81
Mean	29.17
Std Dev	4.039

**Gaus mean : 29.9123**

**Gaus Width: 4.1703**



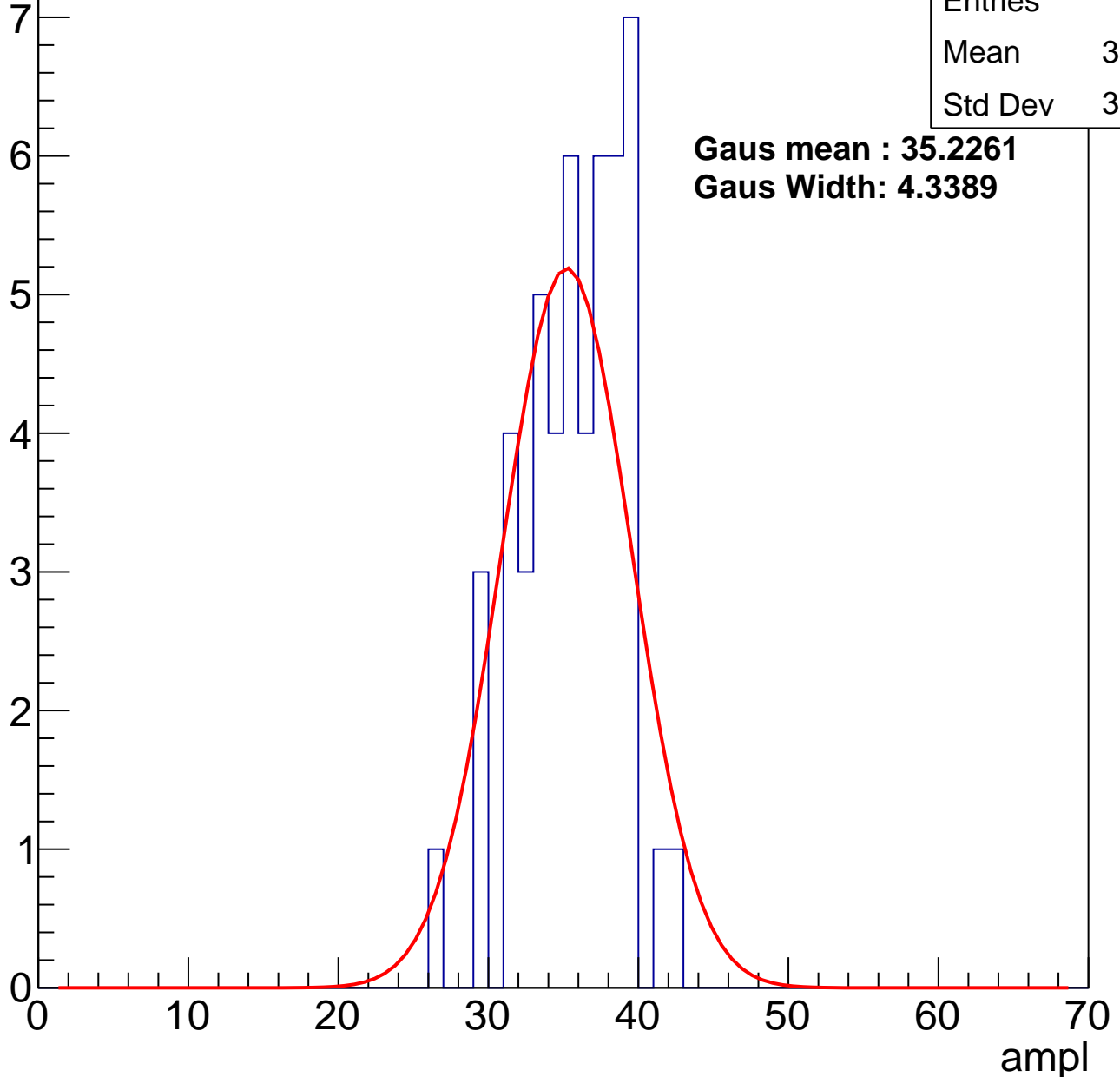
# B1L100S, U2-ch5, adc1

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	51
Mean	35.18
Std Dev	3.376

**Gaus mean : 35.2261**  
**Gaus Width: 4.3389**



# B1L100S, U2-ch5, adc2

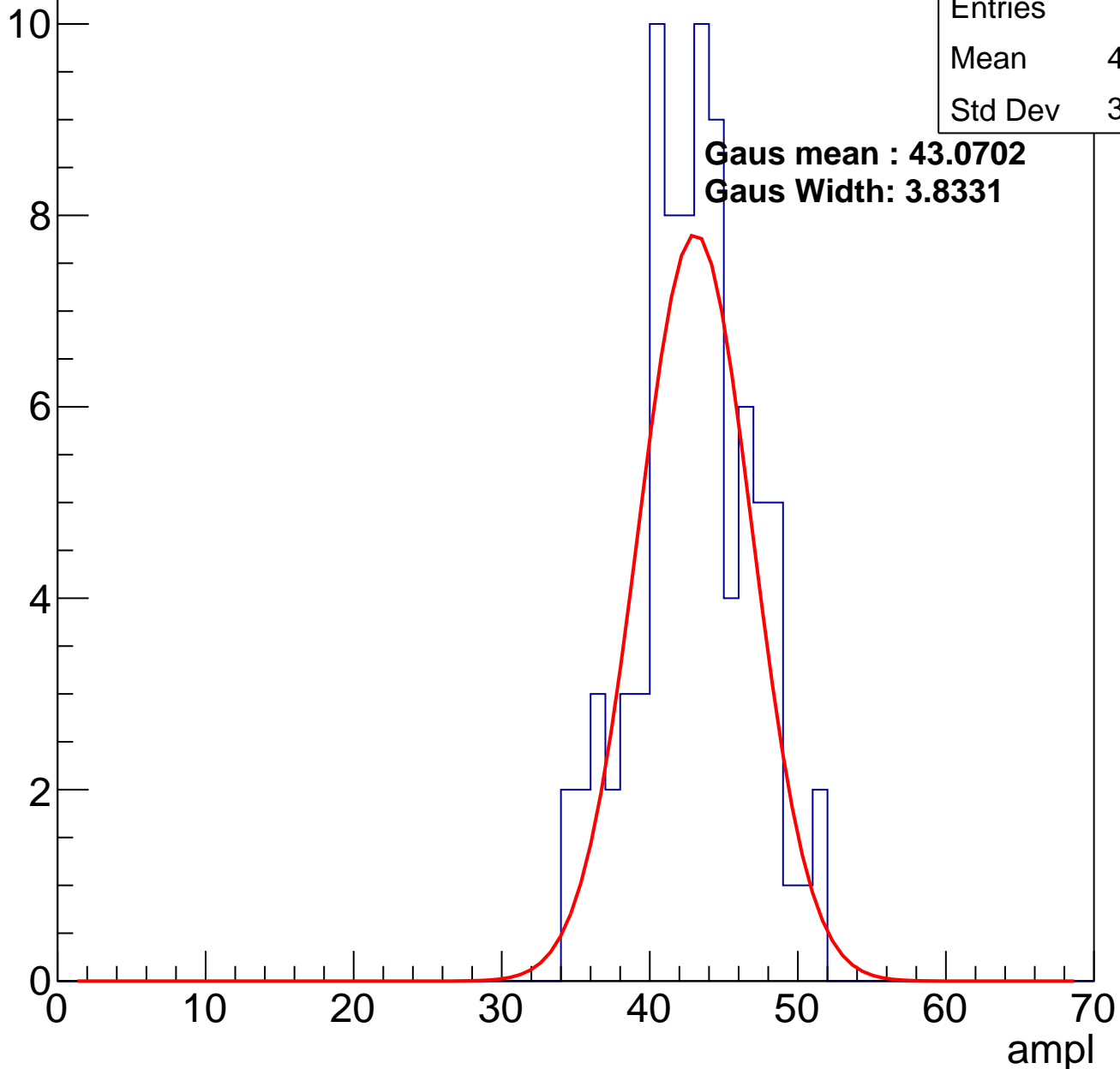
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	84
Mean	42.54
Std Dev	3.844

**Gaus mean : 43.0702**

**Gaus Width: 3.8331**

Entry

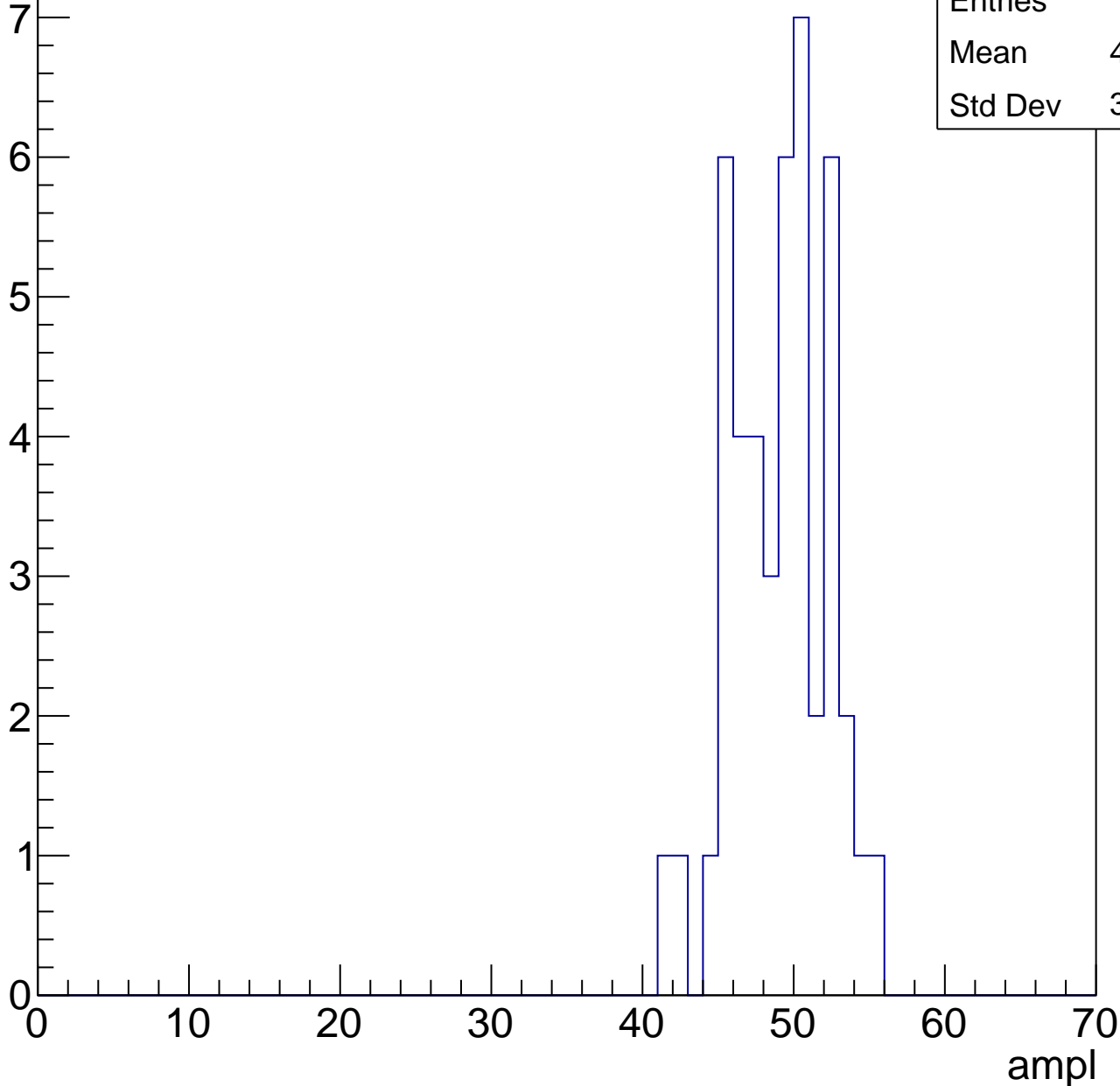


# B1L100S, U2-ch5, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	45
Mean	48.58
Std Dev	3.138

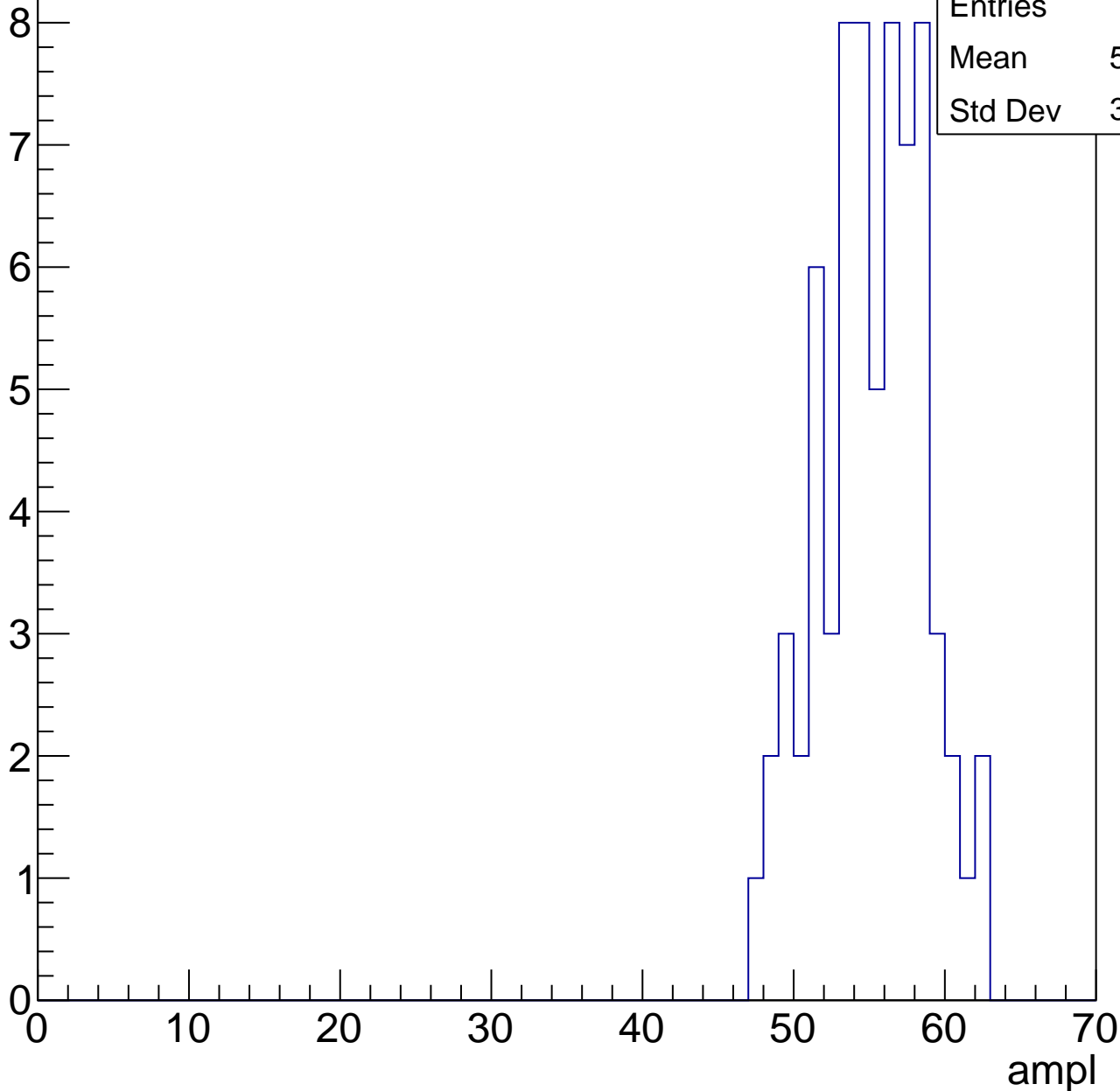


# B1L100S, U2-ch5, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	69
Mean	54.72
Std Dev	3.443

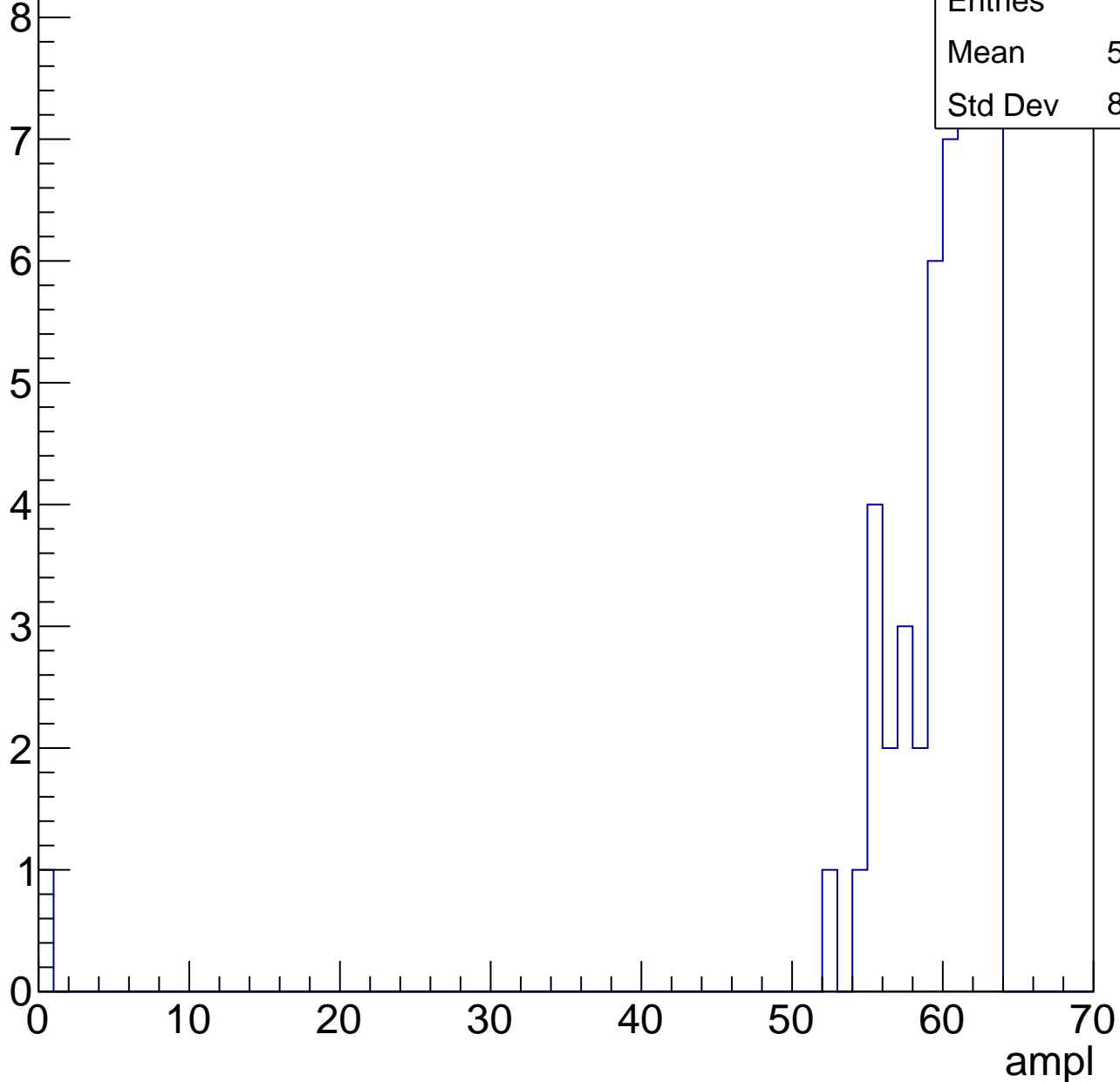


# B1L100S, U2-ch5, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	51
Mean	58.57
Std Dev	8.723



# B1L100S, U2-ch5, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

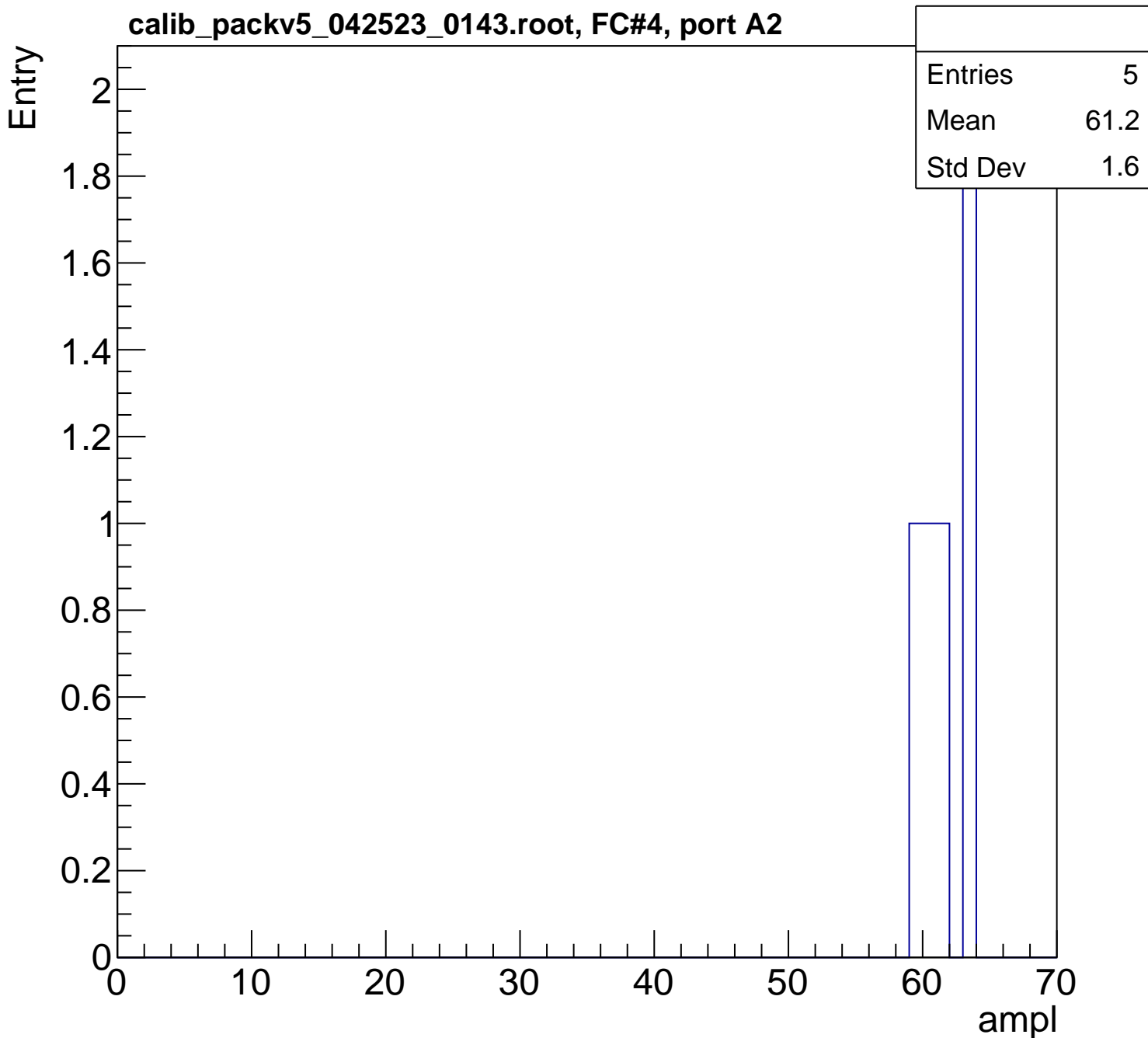
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	5
Mean	61.2
Std Dev	1.6

ampl

0 10 20 30 40 50 60 70





# B1L100S, U2-ch5, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L100S, U2-ch6, adc0

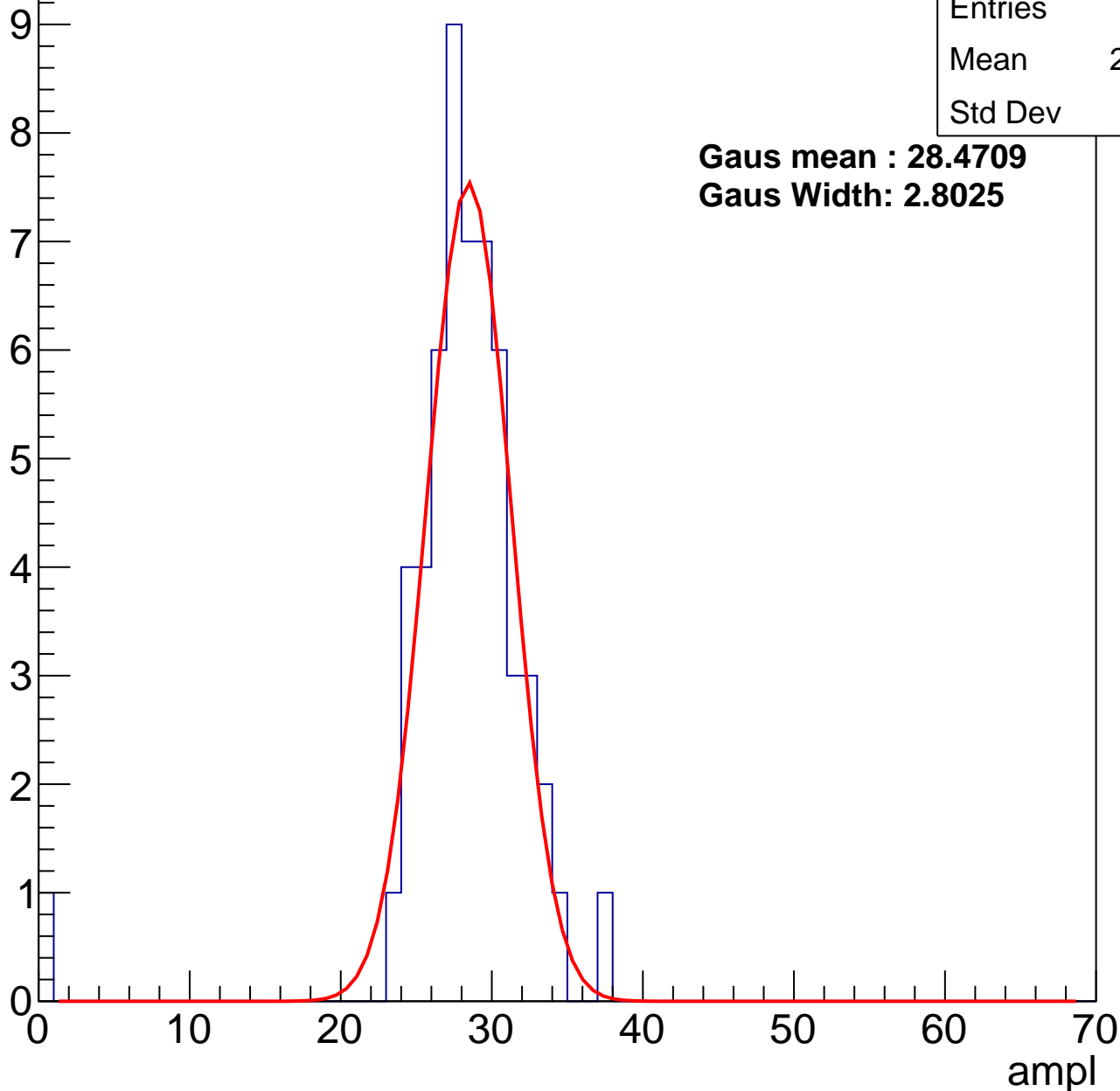
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	55
Mean	27.69
Std Dev	4.69

**Gaus mean : 28.4709**

**Gaus Width: 2.8025**



# B1L100S, U2-ch6, adc1

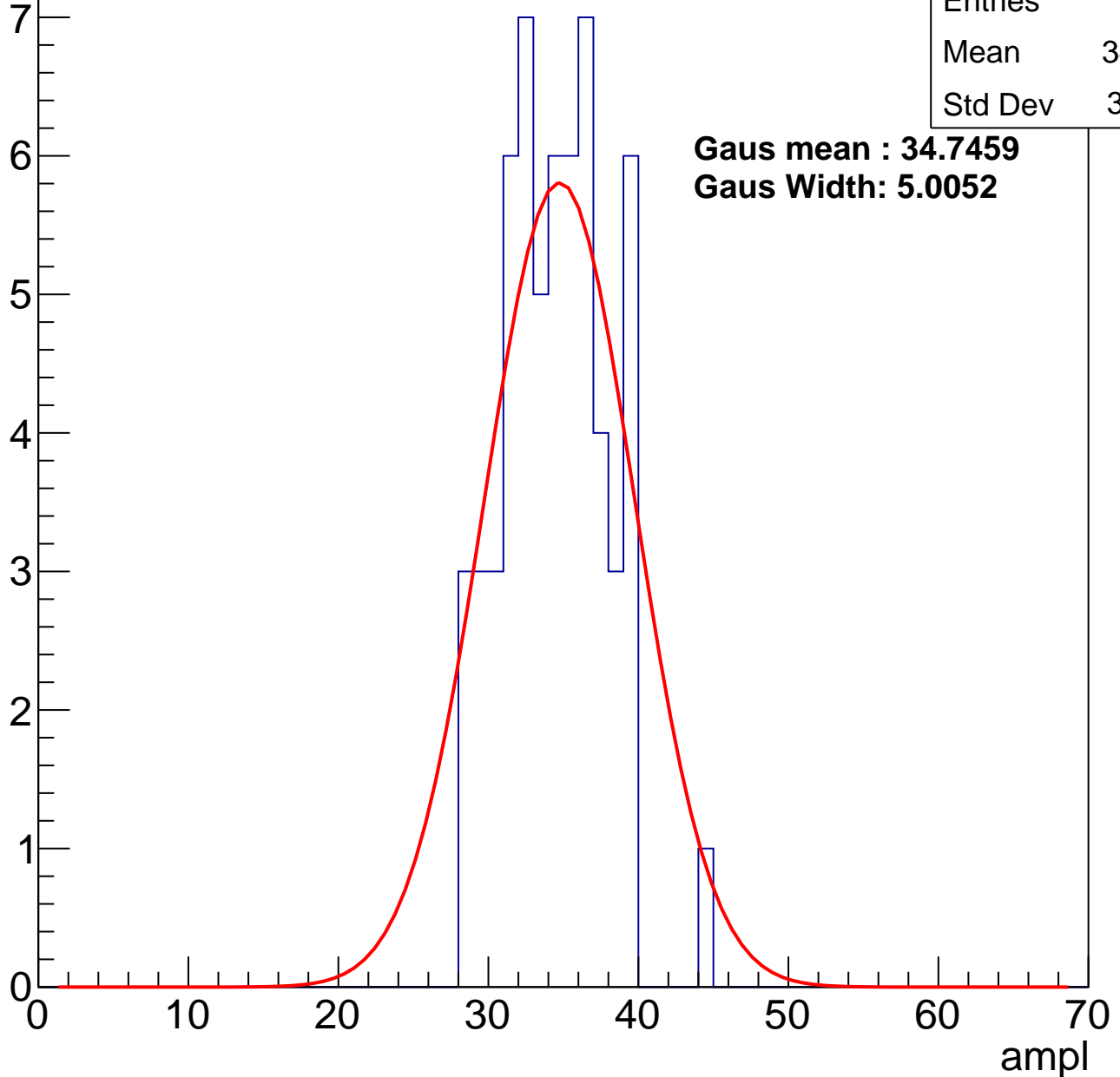
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	60
Mean	34.03
Std Dev	3.381

**Gaus mean : 34.7459**

**Gaus Width: 5.0052**



# B1L100S, U2-ch6, adc2

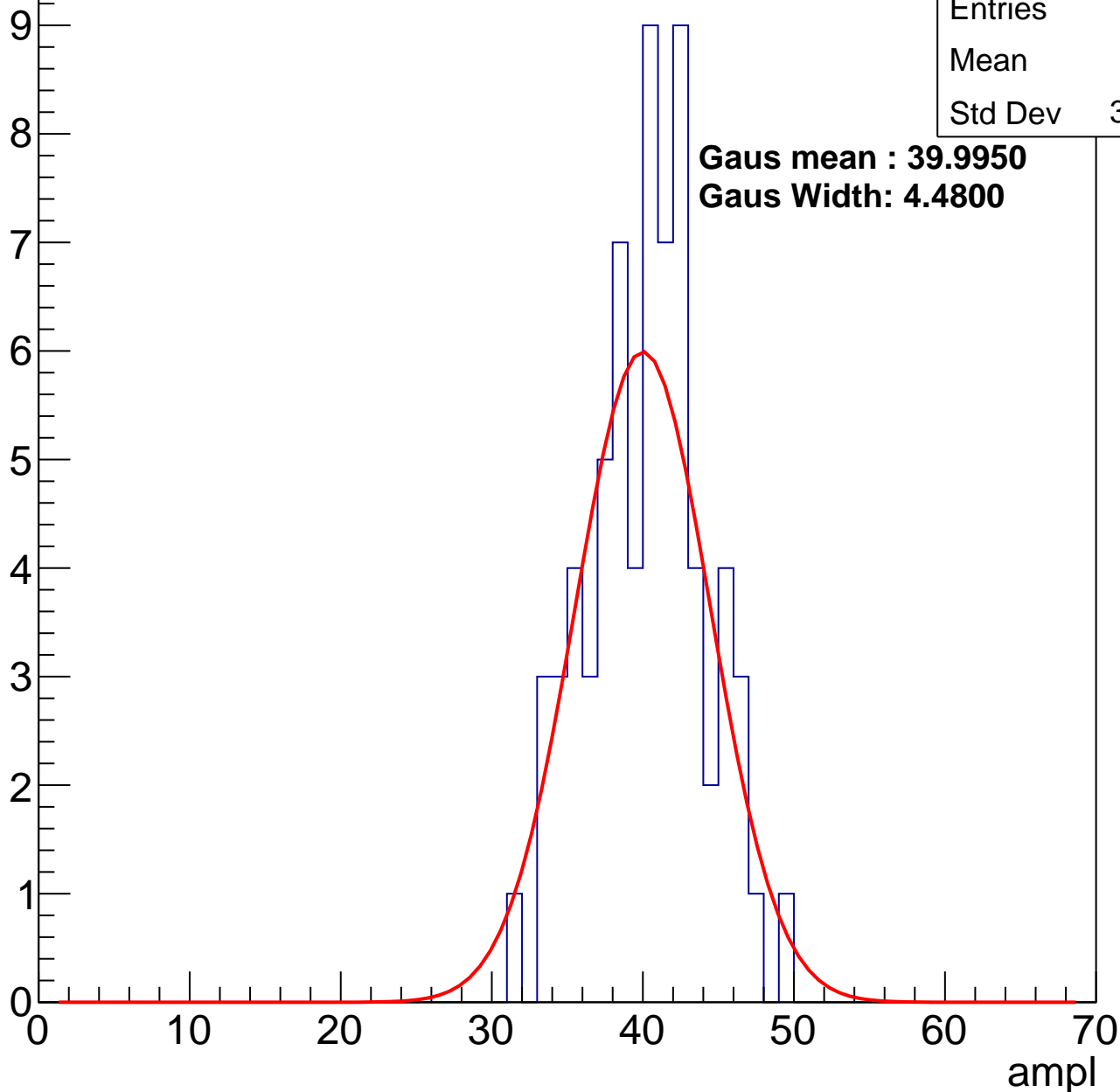
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	70
Mean	39.8
Std Dev	3.793

**Gaus mean : 39.9950**

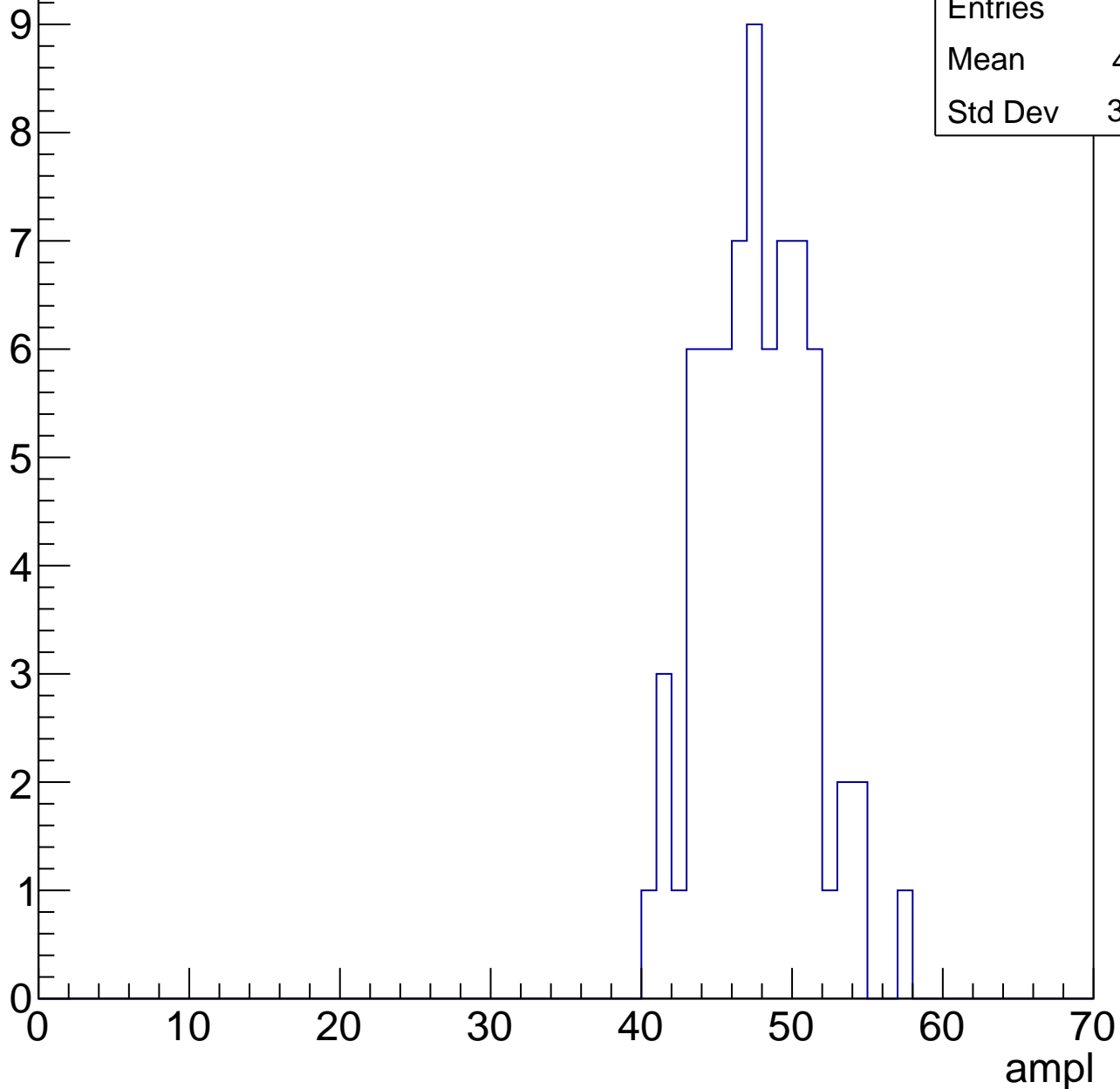
**Gaus Width: 4.4800**



# B1L100S, U2-ch6, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



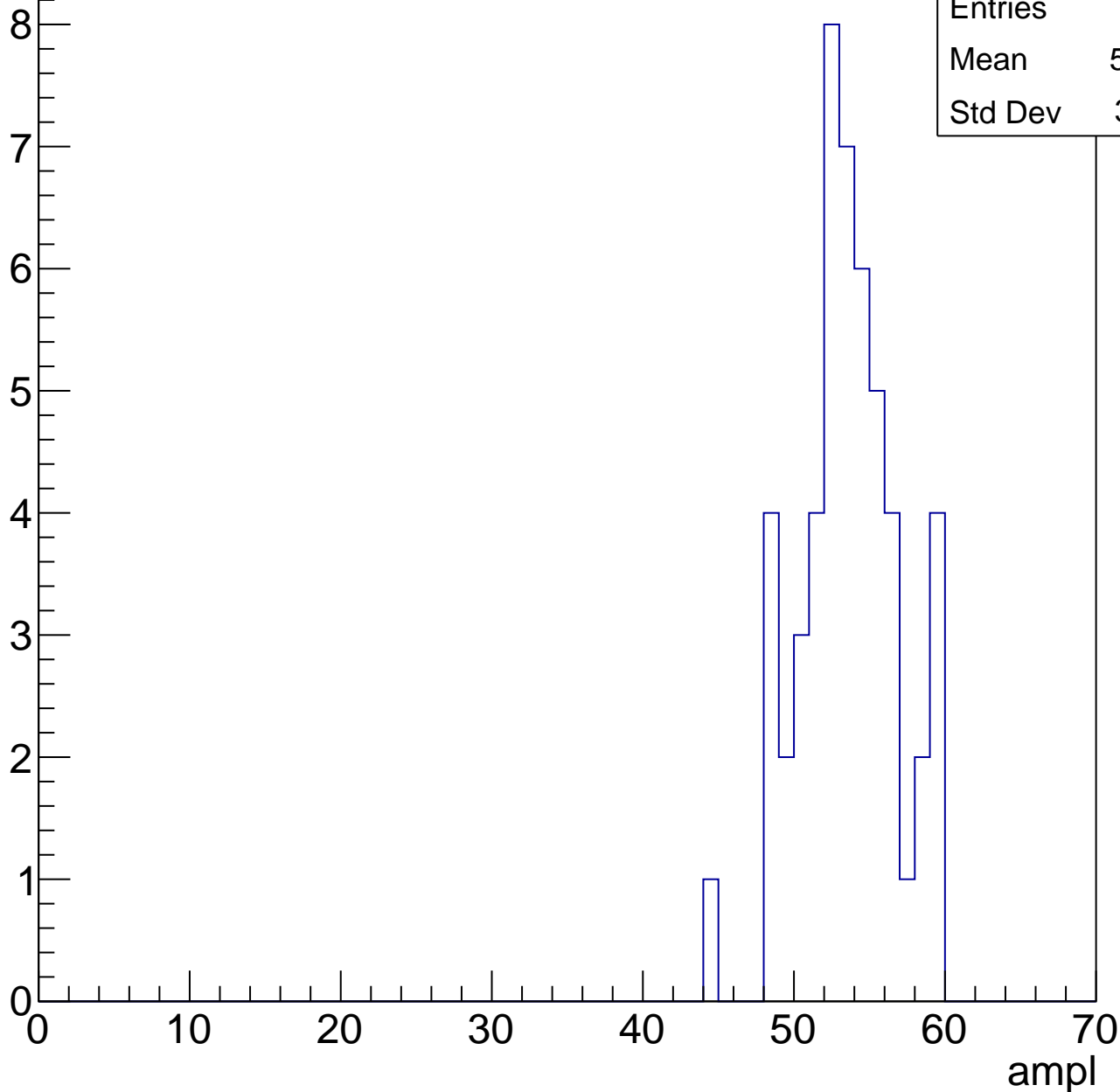
Entries	71
Mean	47.21
Std Dev	3.456

# B1L100S, U2-ch6, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

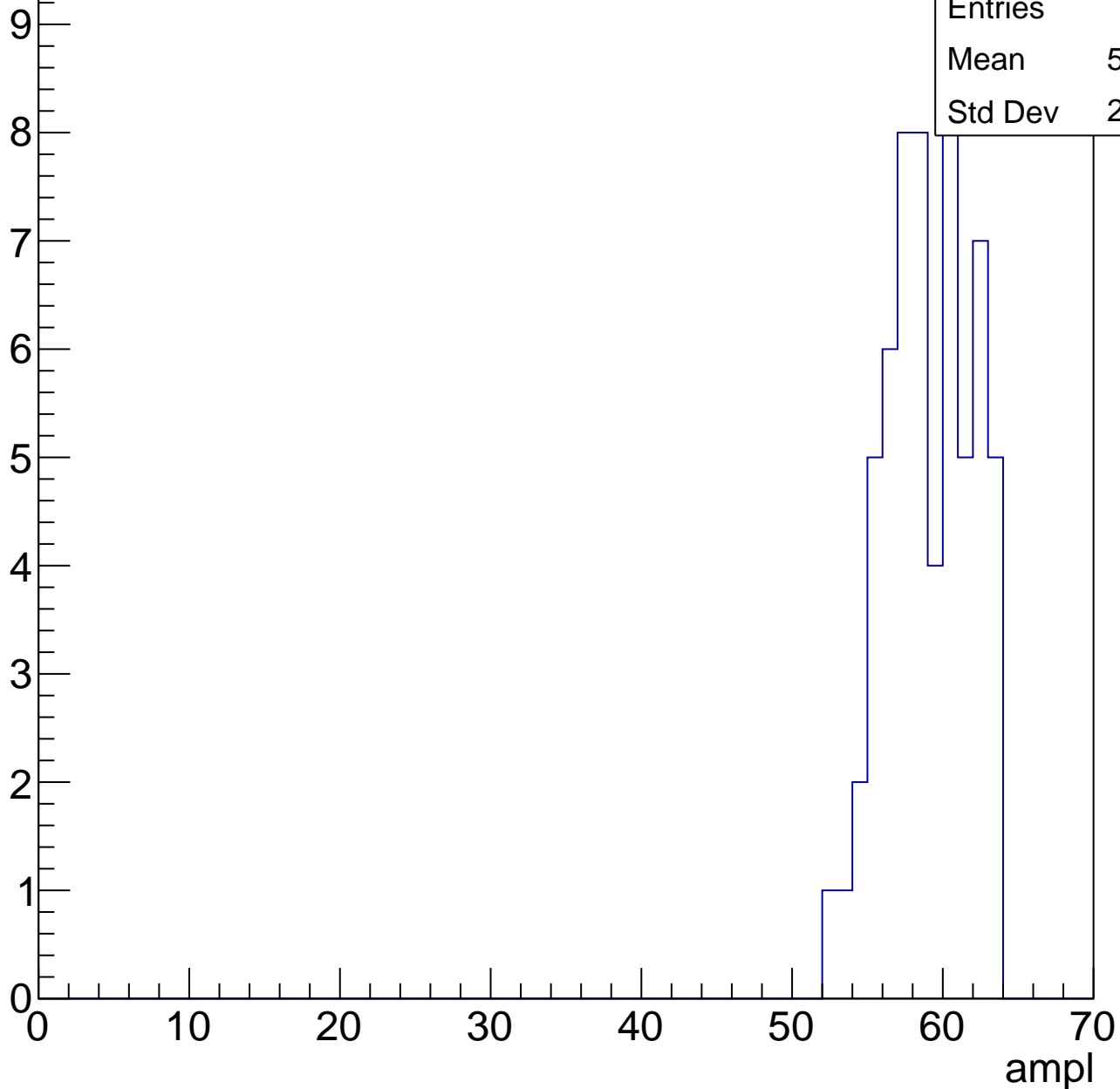
Entries	51
Mean	53.08
Std Dev	3.241



# B1L100S, U2-ch6, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



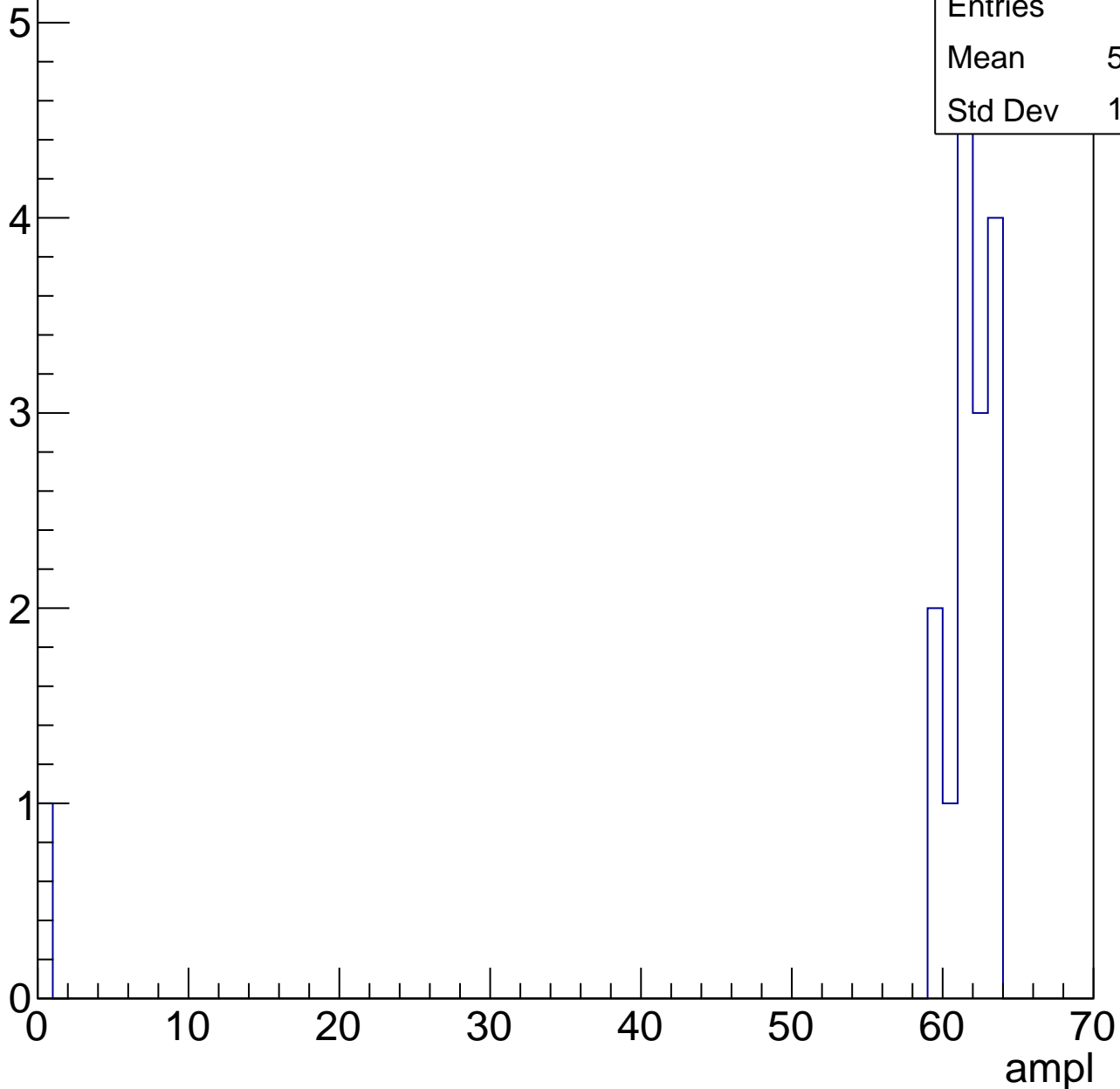
Entries	61
Mean	58.59
Std Dev	2.778

# B1L100S, U2-ch6, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	16
Mean	57.56
Std Dev	14.92





# B1L100S, U2-ch6, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



# B1L100S, U2-ch7, adc0

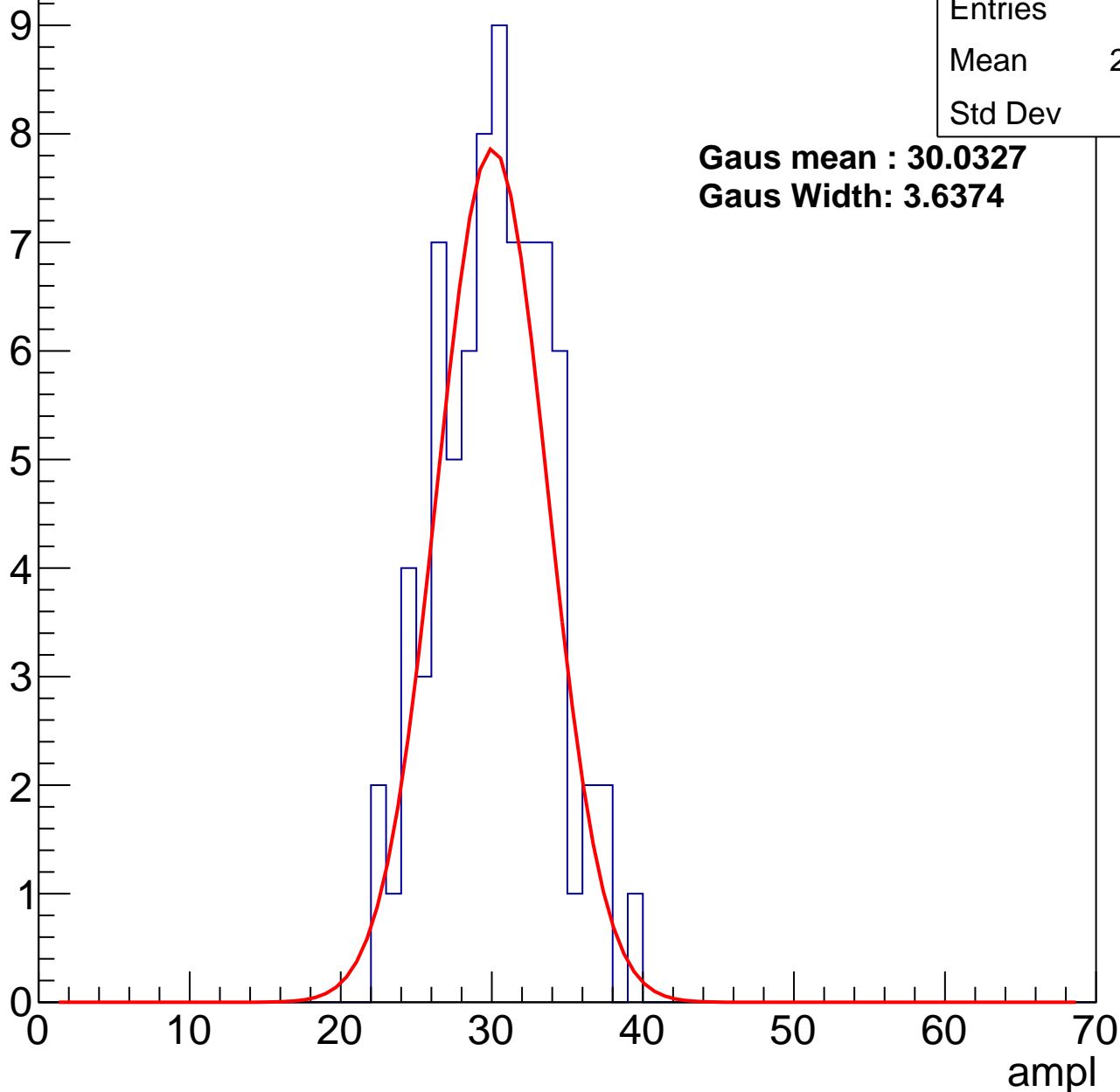
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	78
Mean	29.76
Std Dev	3.67

**Gaus mean : 30.0327**

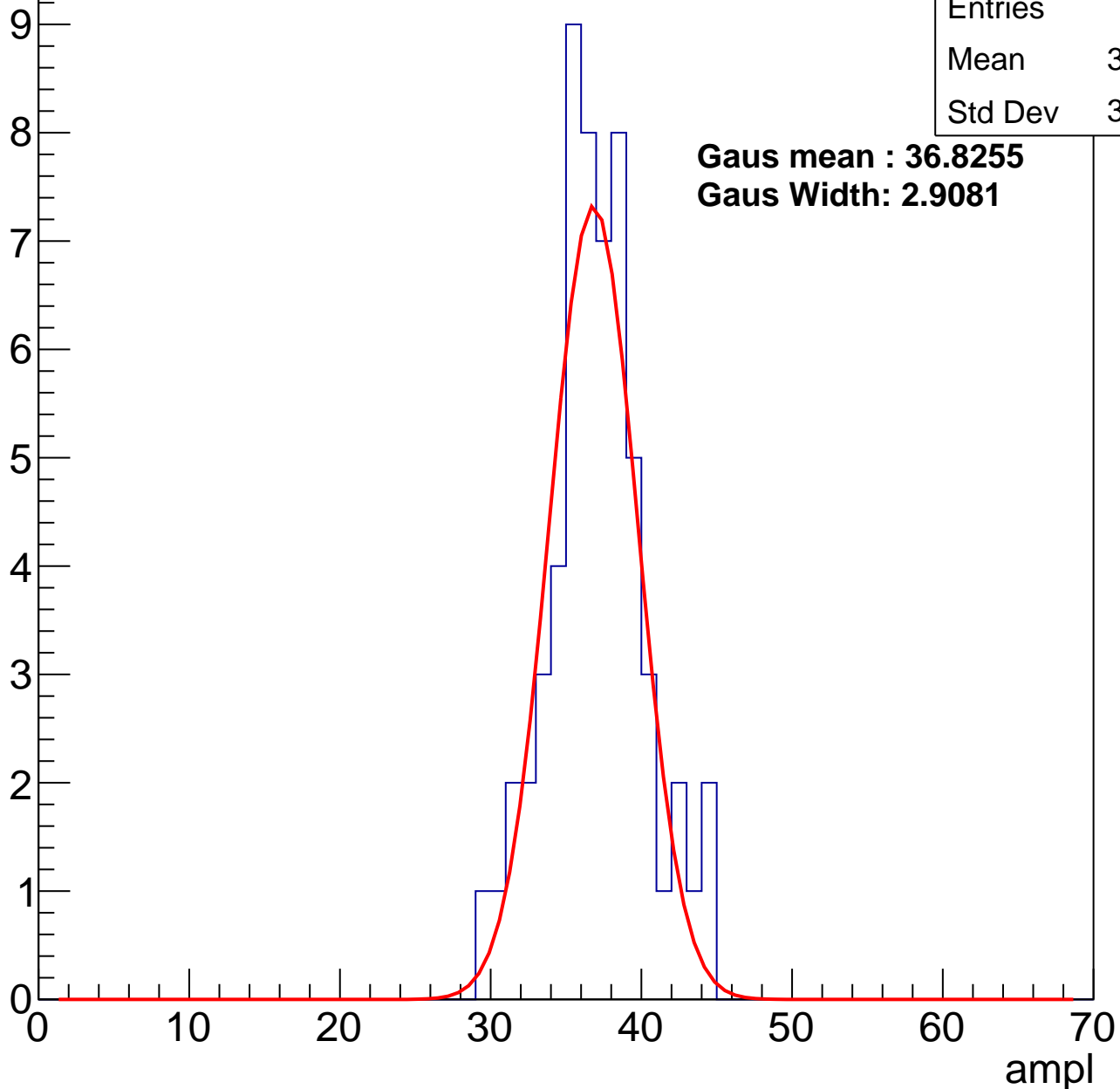
**Gaus Width: 3.6374**



# B1L100S, U2-ch7, adc1

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



# B1L100S, U2-ch7, adc2

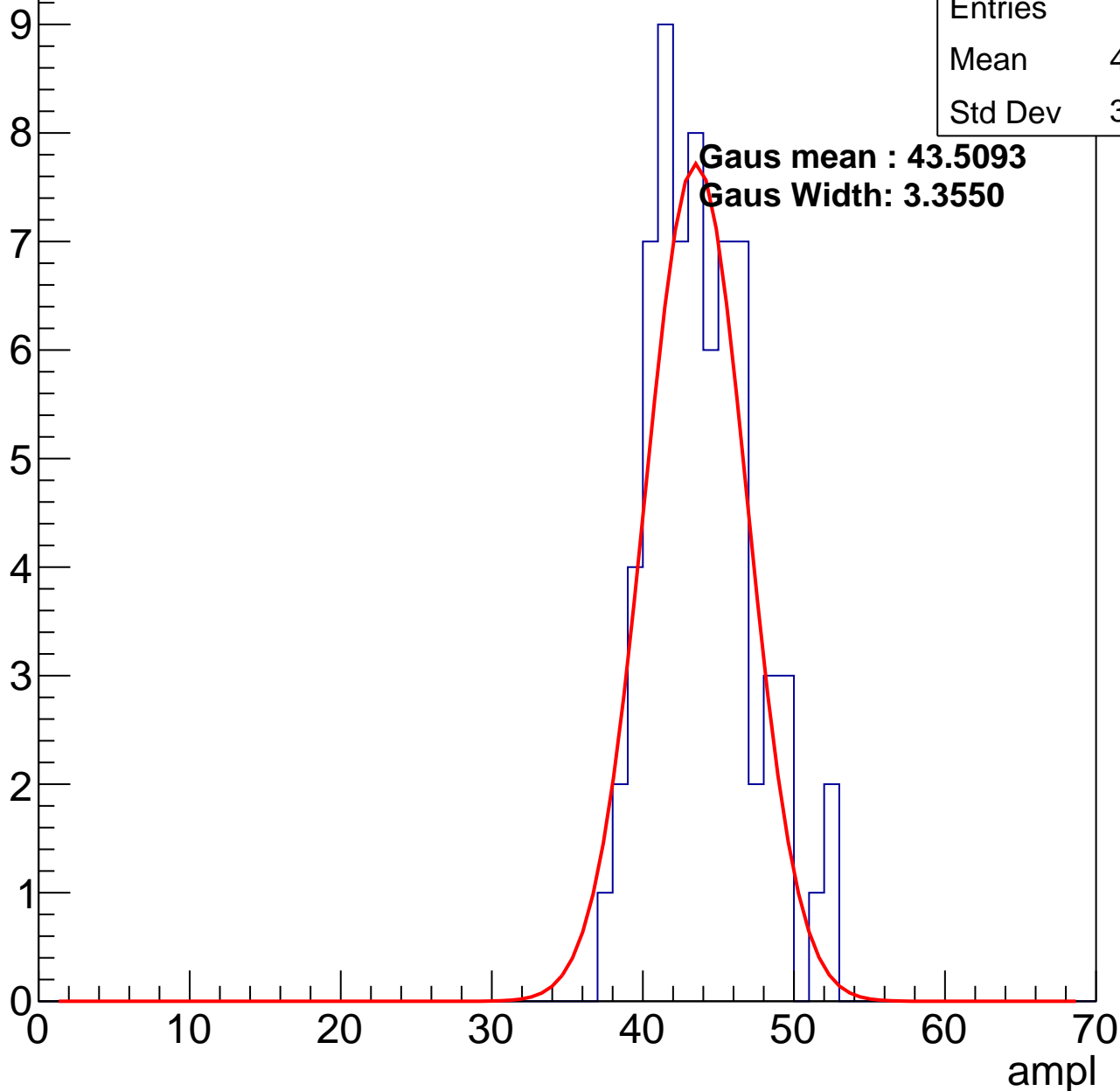
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	69
Mean	43.43
Std Dev	3.364

**Gaus mean : 43.5093**

**Gaus Width: 3.3550**

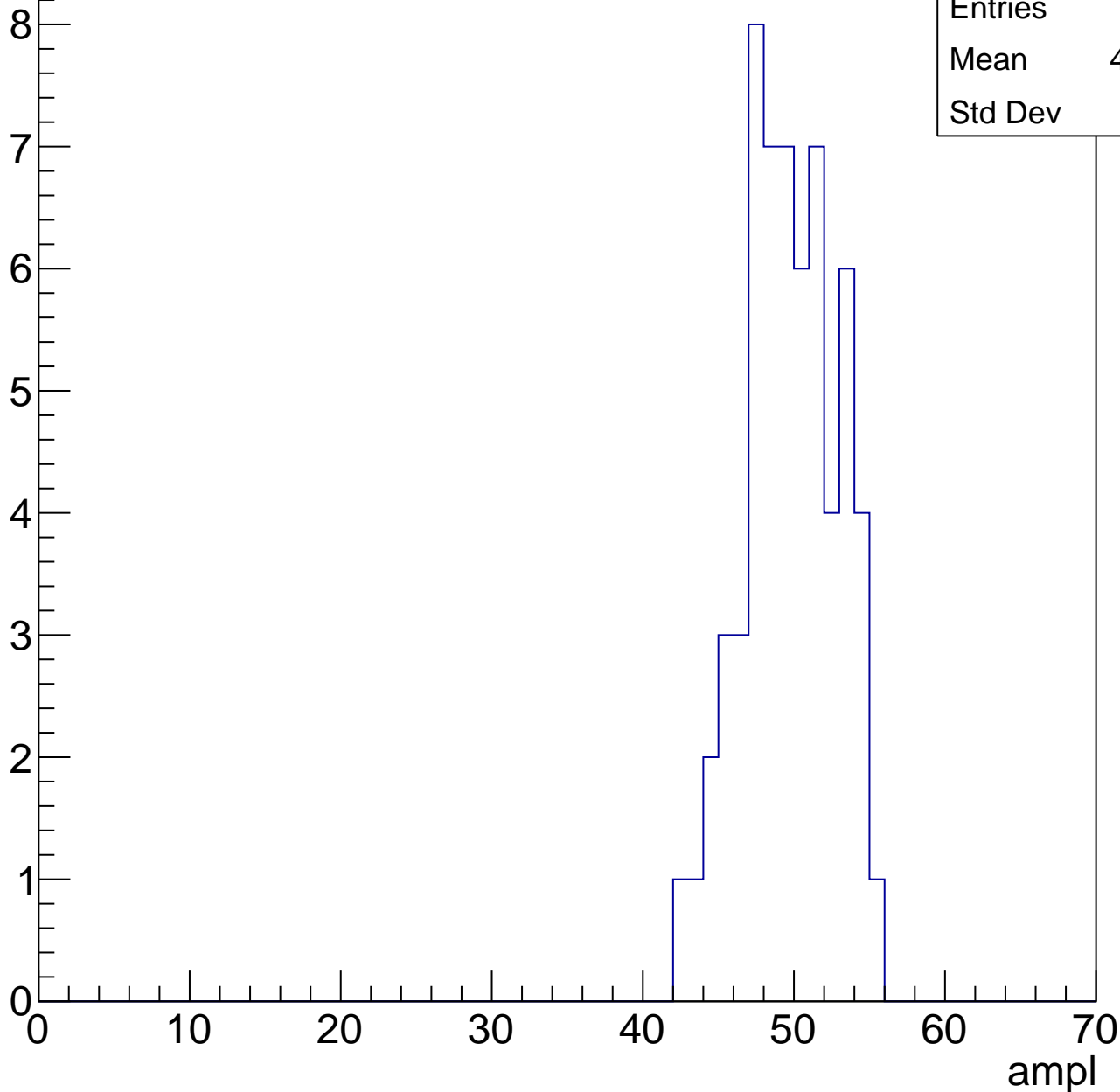


# B1L100S, U2-ch7, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	60
Mean	49.25
Std Dev	3.02



# B1L100S, U2-ch7, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

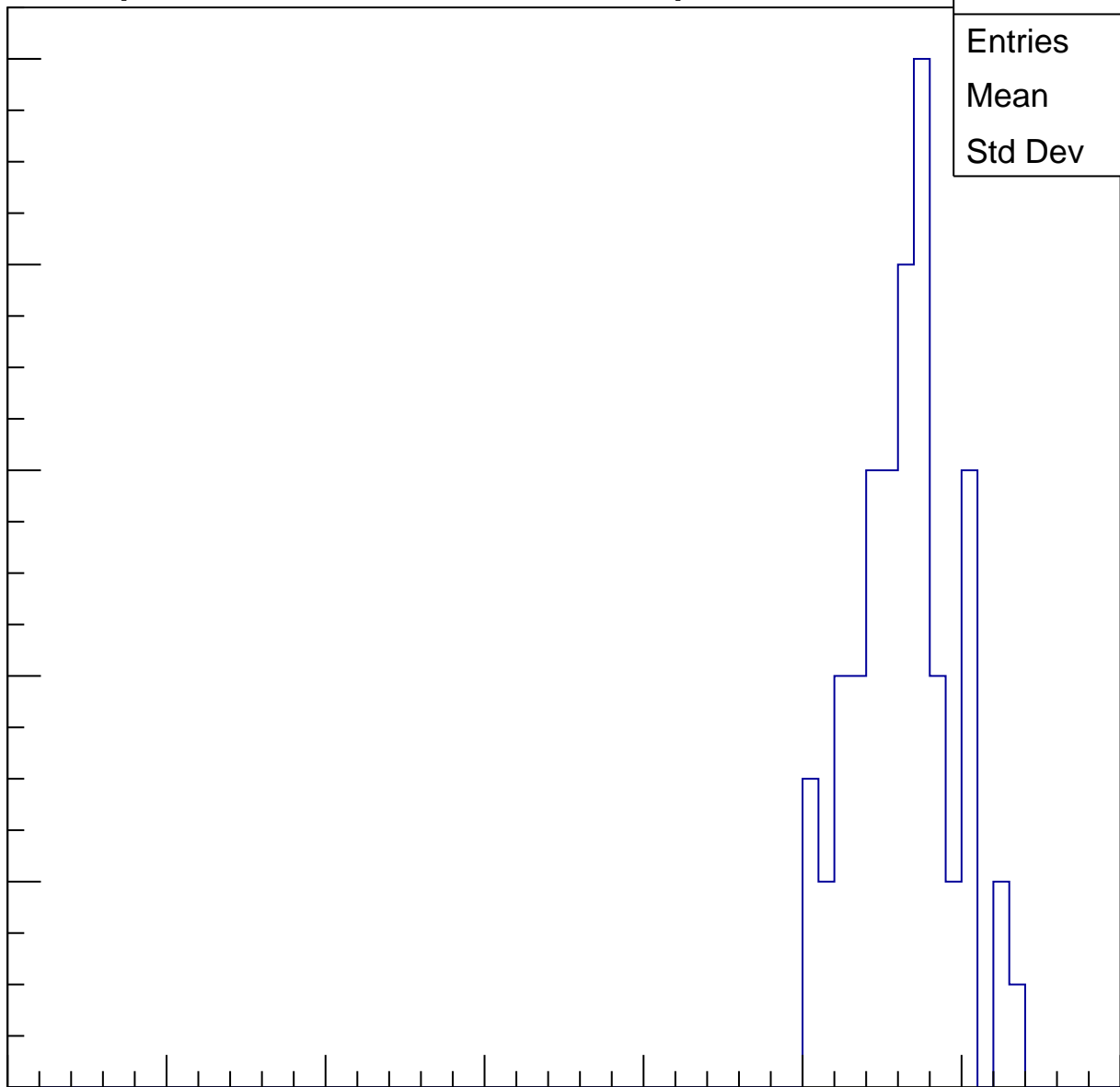
Entries	58
Mean	55.88
Std Dev	3.074

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

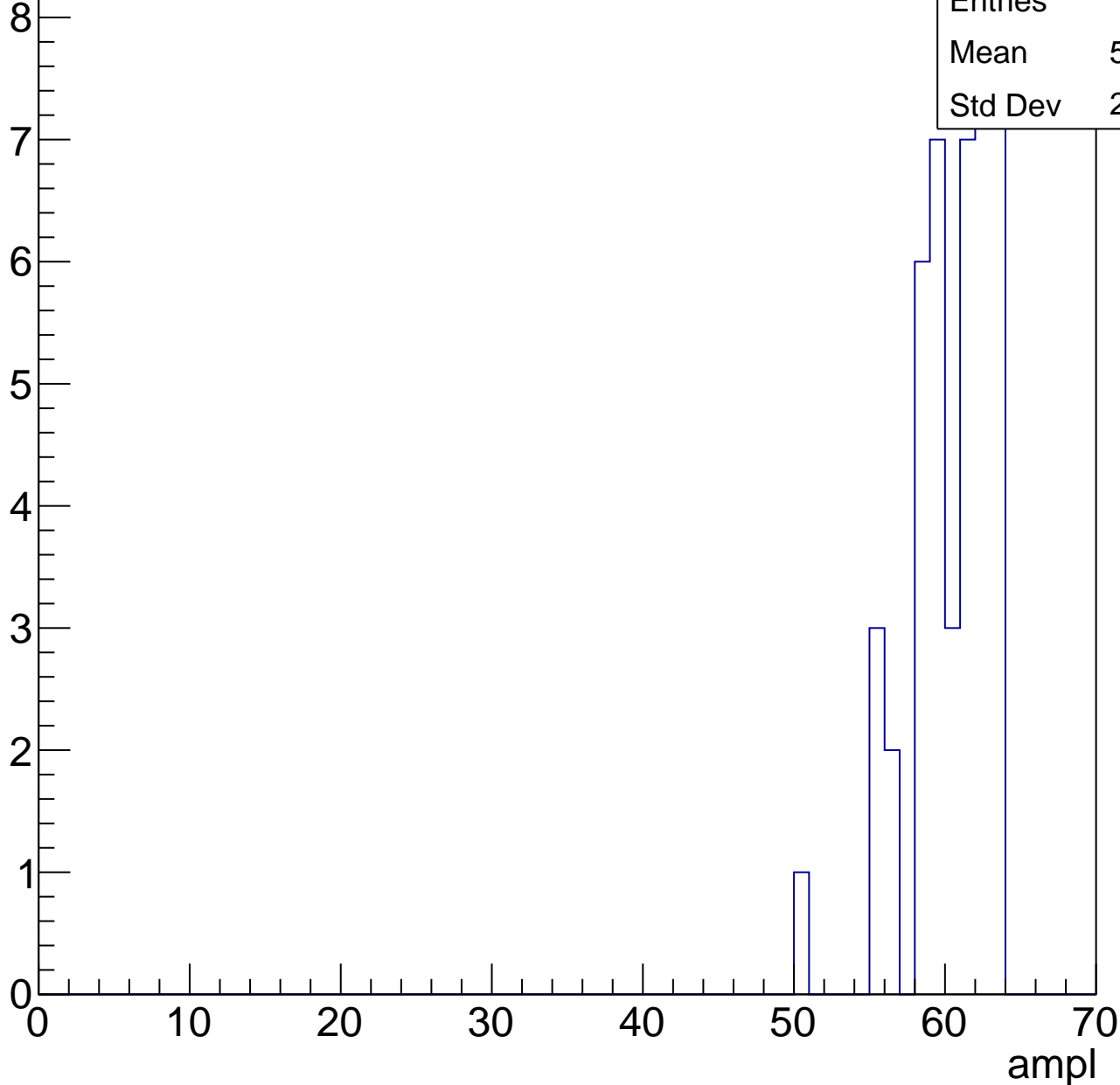


# B1L100S, U2-ch7, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

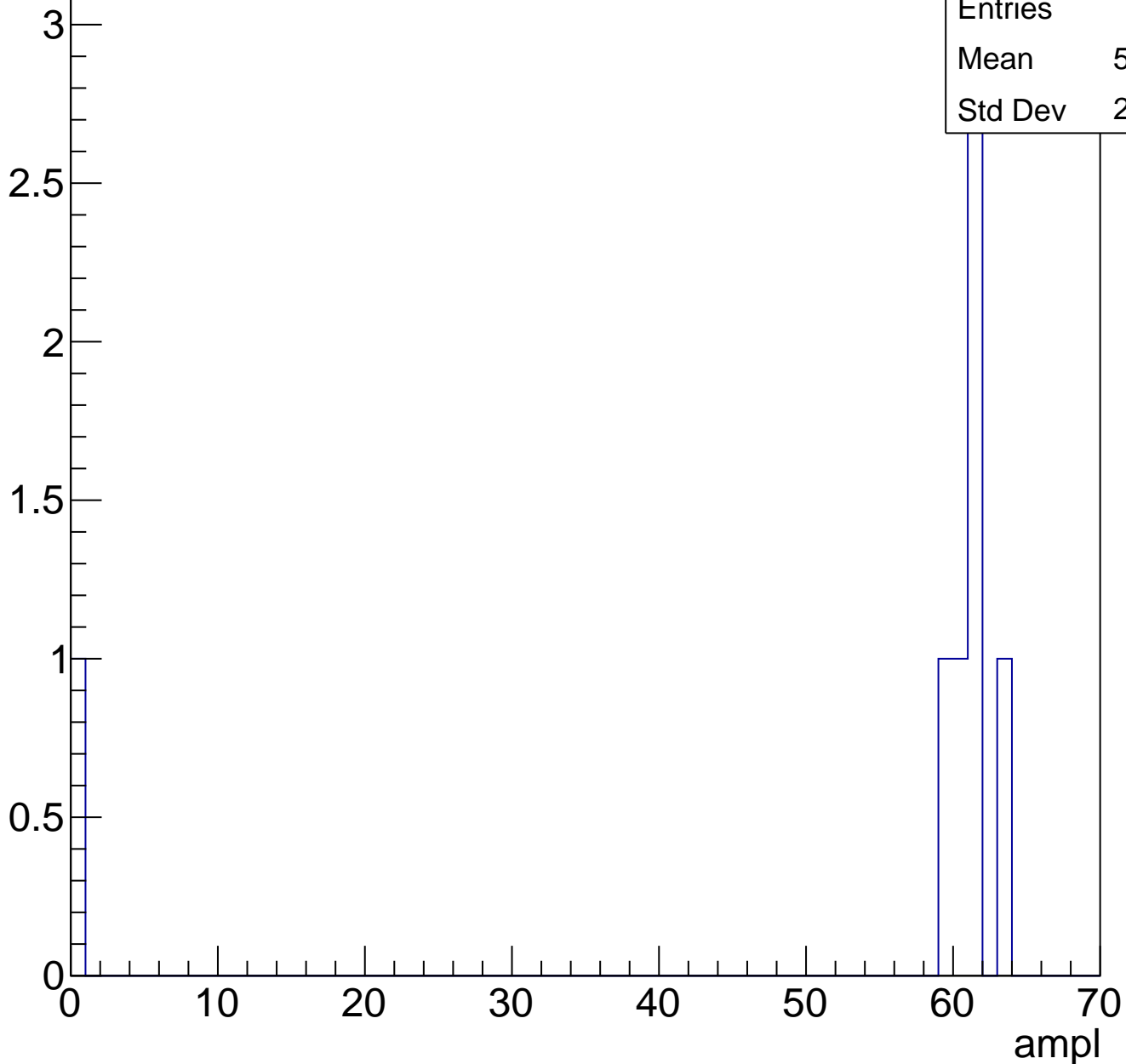
Entries	45
Mean	59.89
Std Dev	2.783



# B1L100S, U2-ch7, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	7
Mean	52.14
Std Dev	21.32



# B1L100S, U2-ch7, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

1  
0.8  
0.6  
0.4  
0.2  
0

Entries	1
Mean	18
Std Dev	0

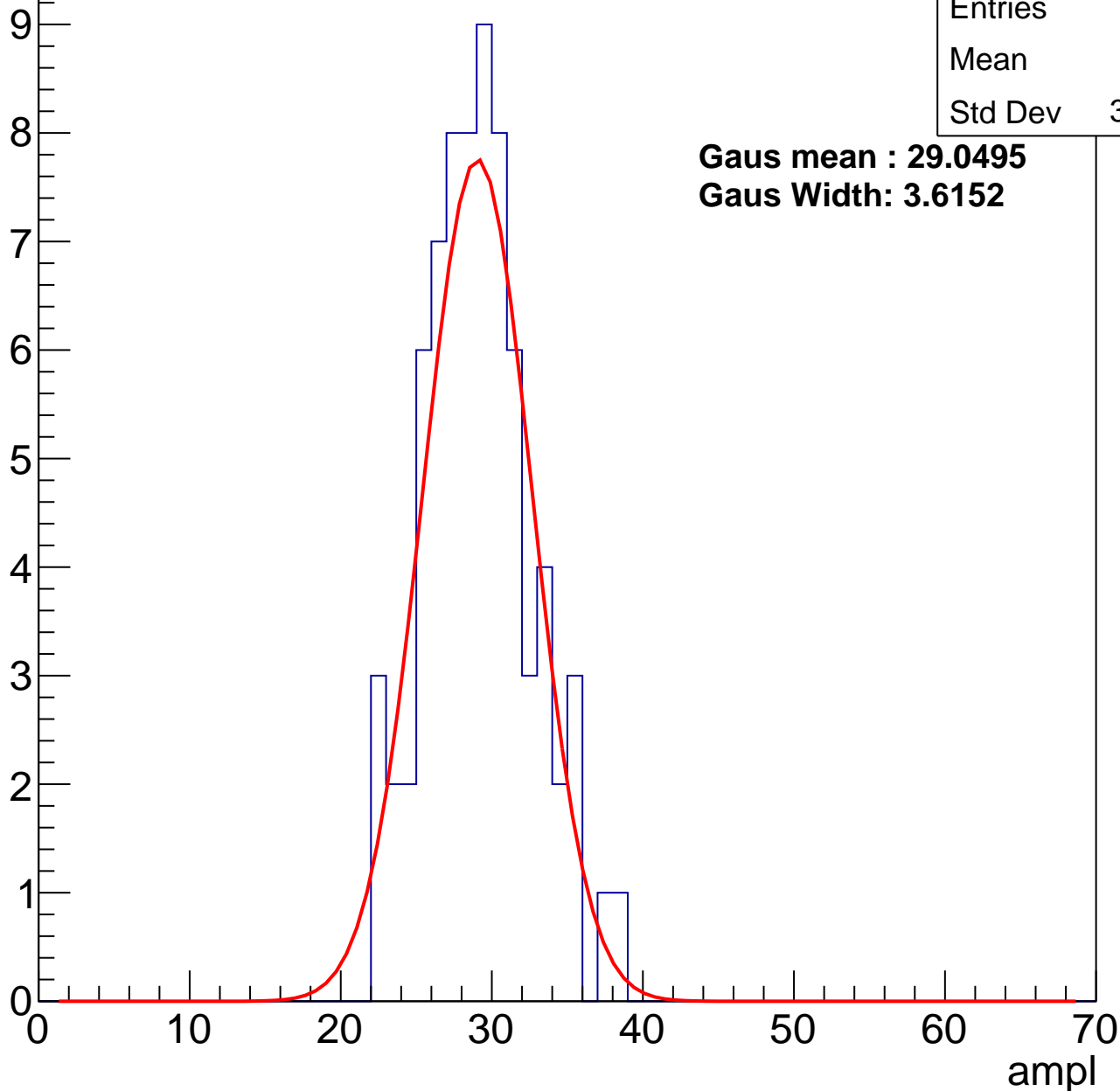
ampl

0 10 20 30 40 50 60 70

# B1L100S, U2-ch8, adc0

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



# B1L100S, U2-ch8, adc1

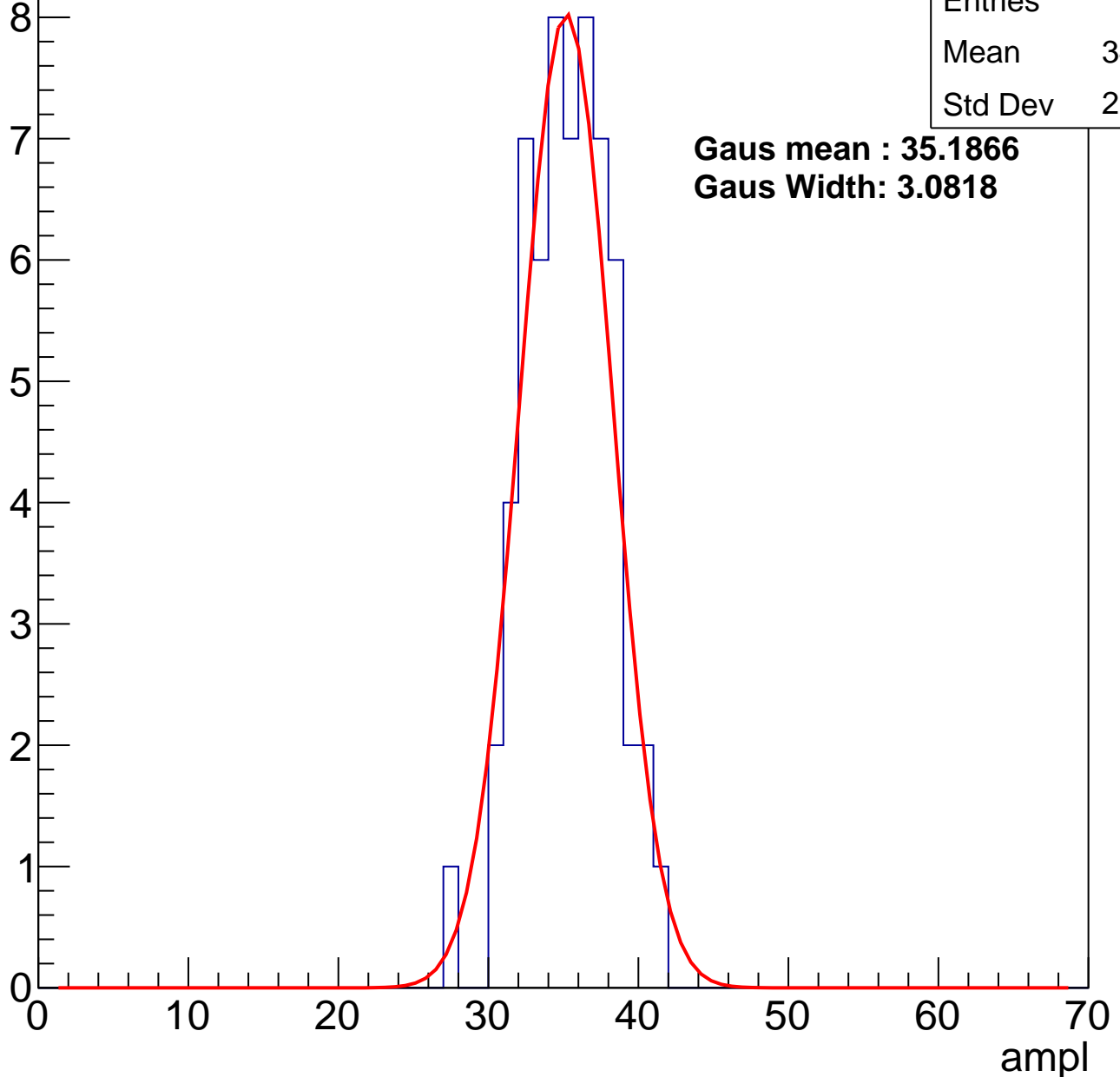
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	61
Mean	34.82
Std Dev	2.802

**Gaus mean : 35.1866**

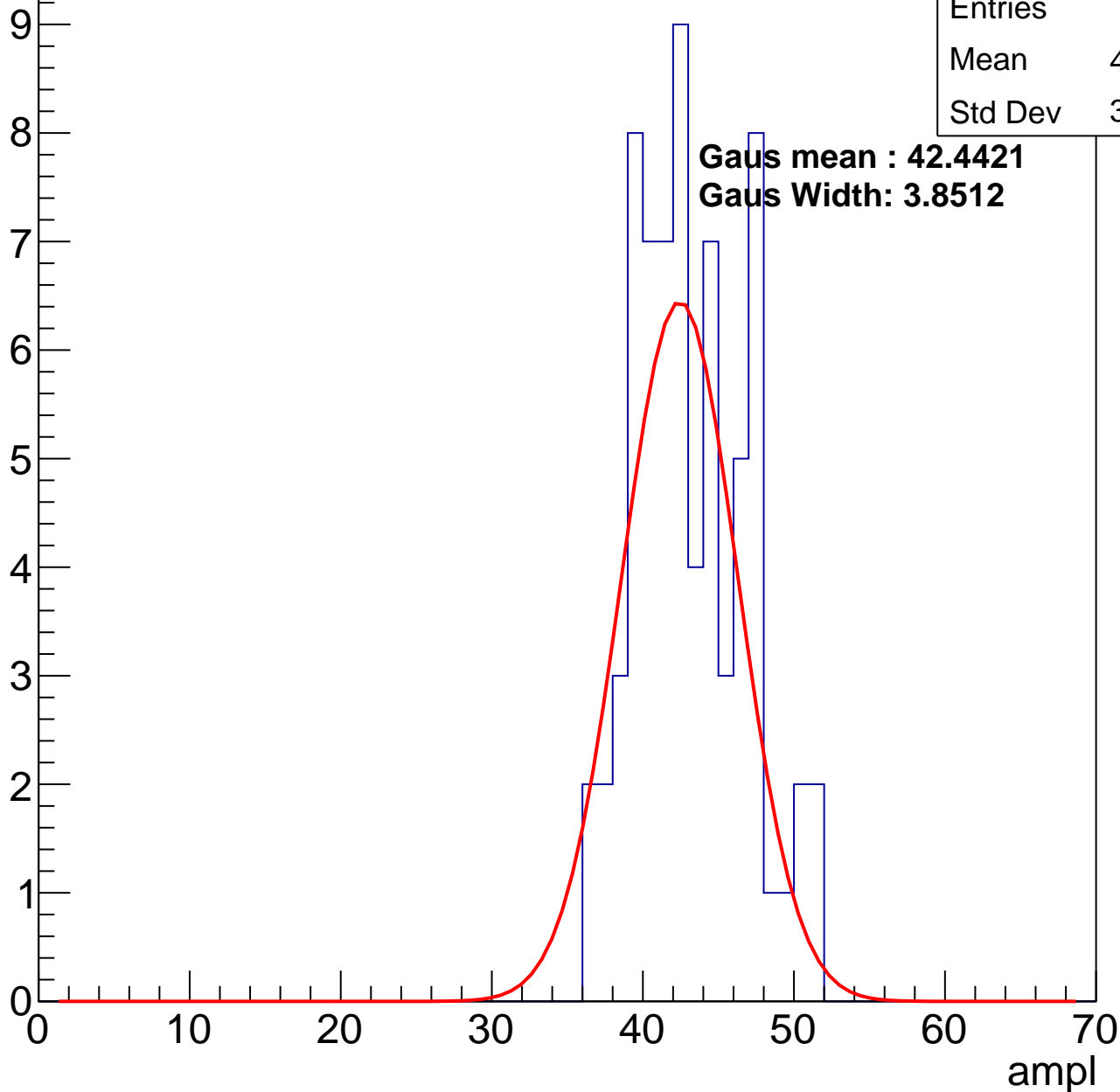
**Gaus Width: 3.0818**



# B1L100S, U2-ch8, adc2

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

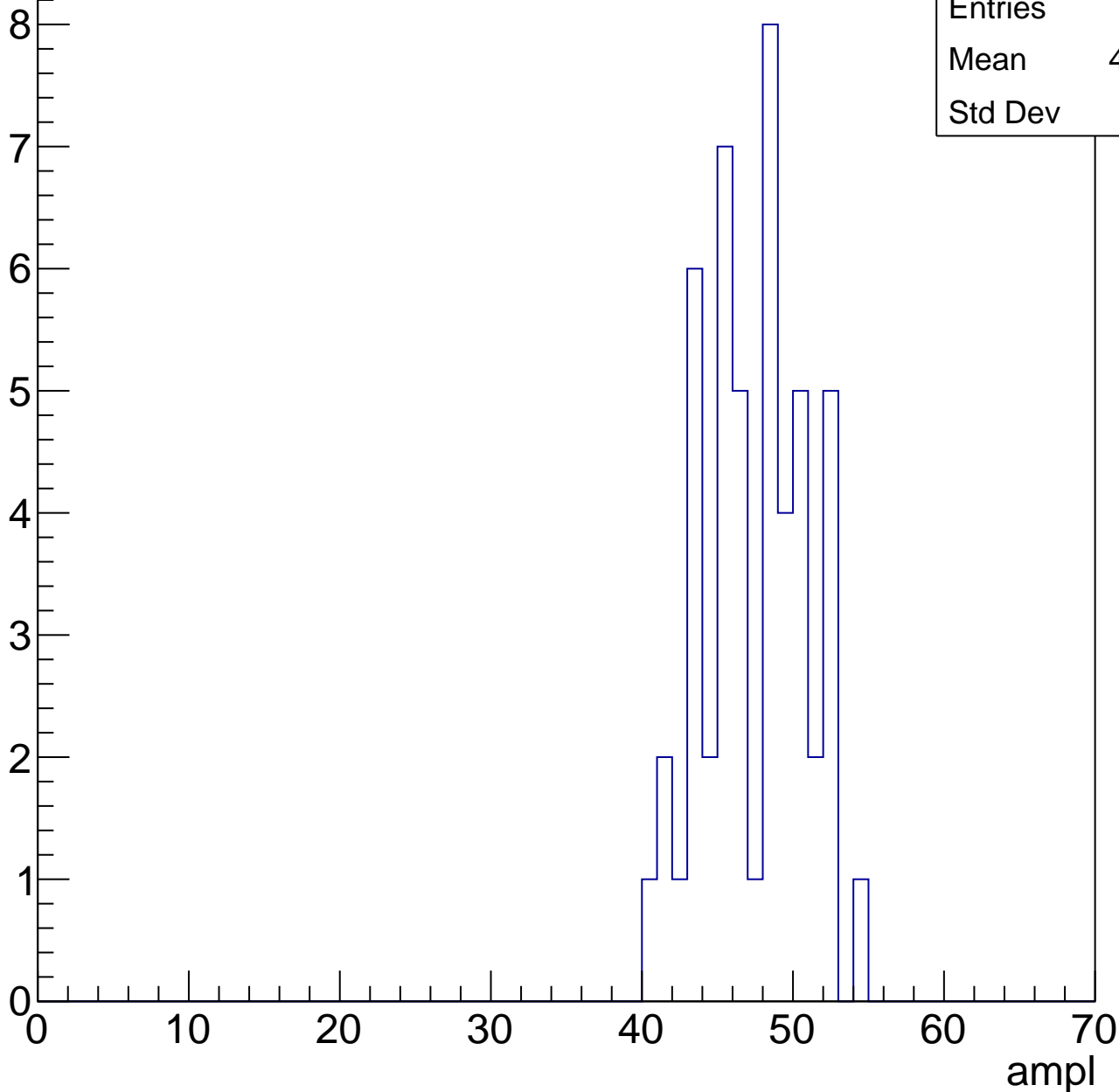


# B1L100S, U2-ch8, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	50
Mean	46.96
Std Dev	3.37

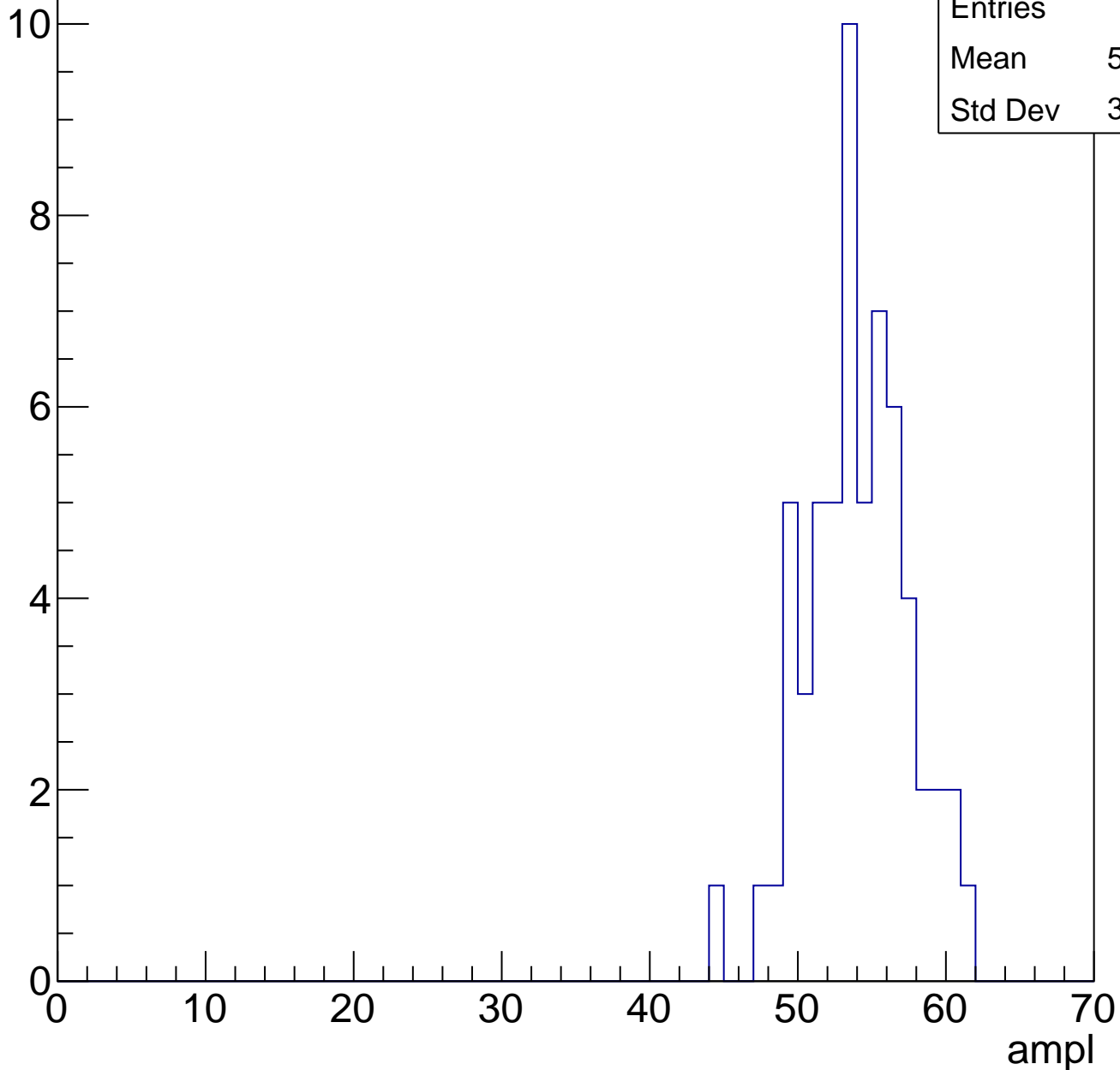


# B1L100S, U2-ch8, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	60
Mean	53.55
Std Dev	3.393

Entry

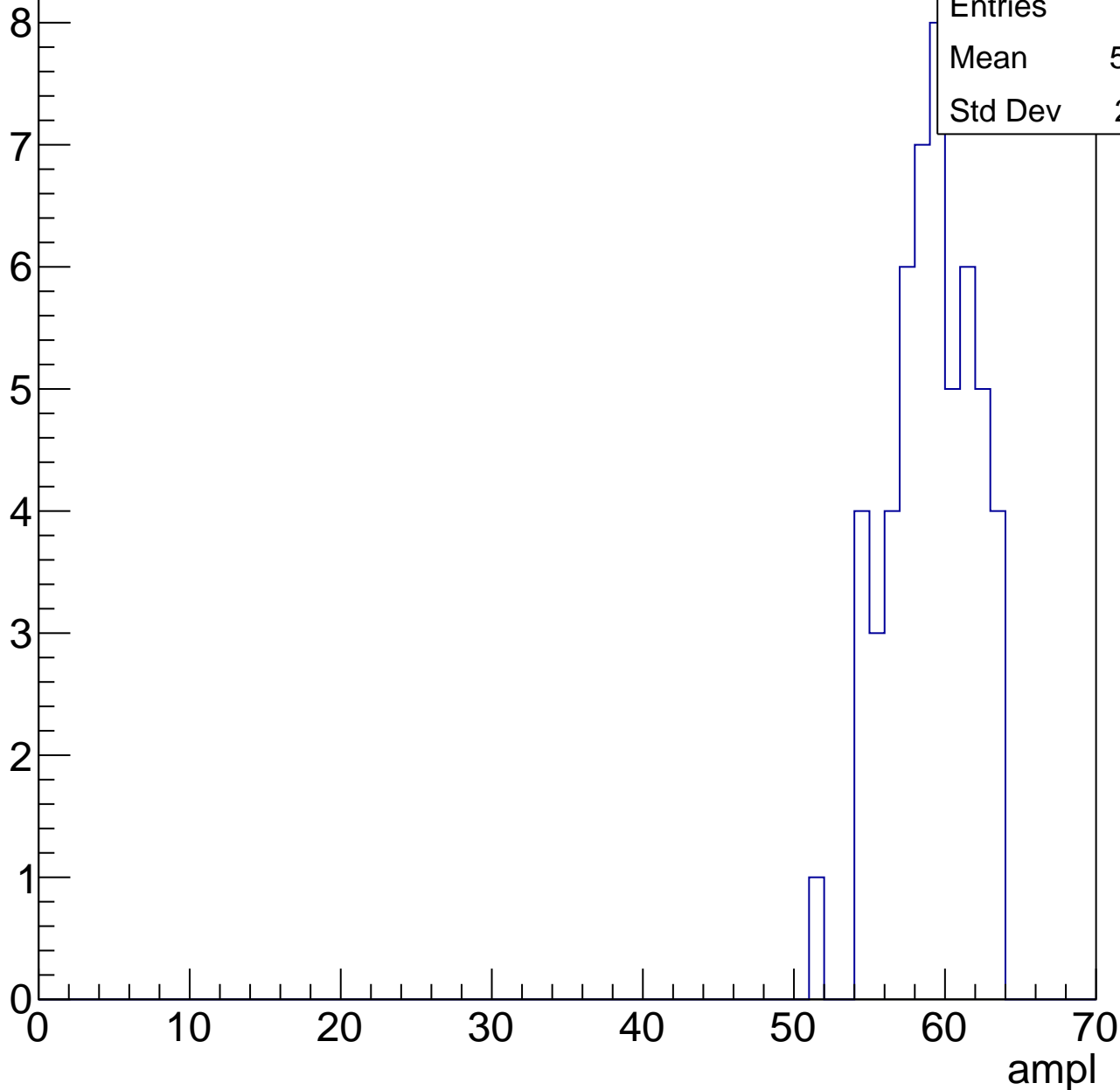


# B1L100S, U2-ch8, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	53
Mean	58.57
Std Dev	2.771

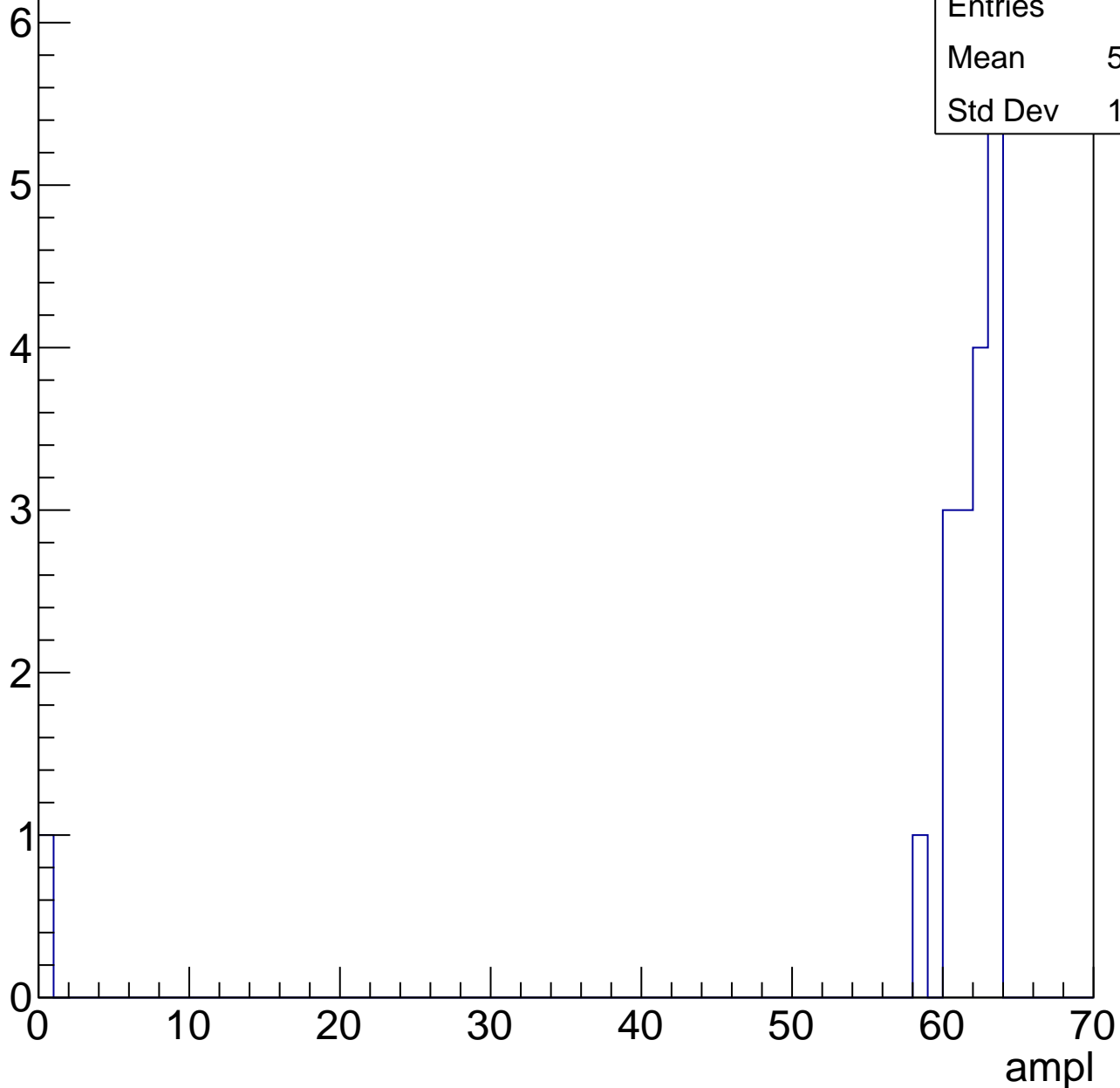


# B1L100S, U2-ch8, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	18
Mean	58.17
Std Dev	14.17

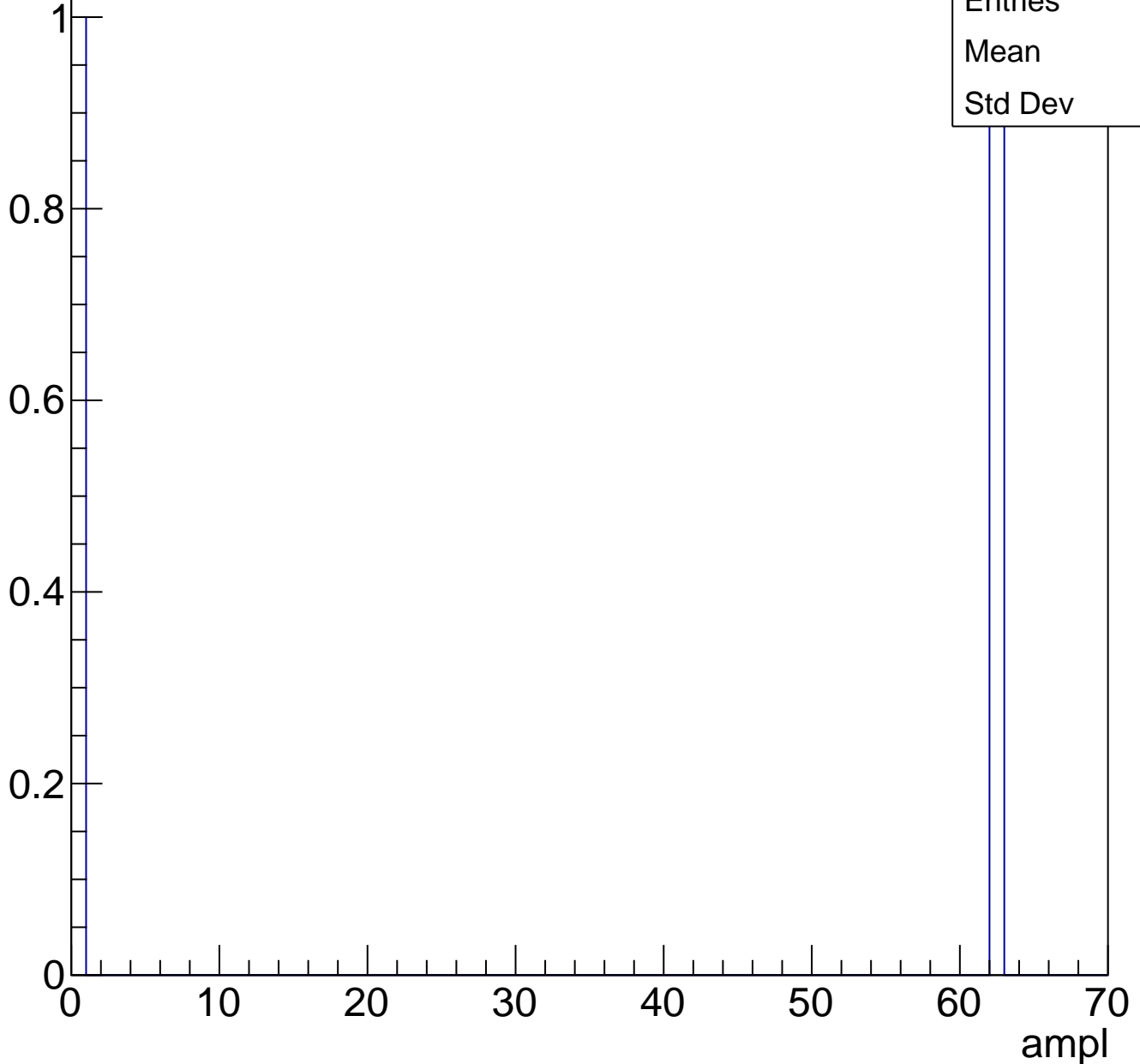




# B1L100S, U2-ch8, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



# B1L100S, U2-ch9, adc0

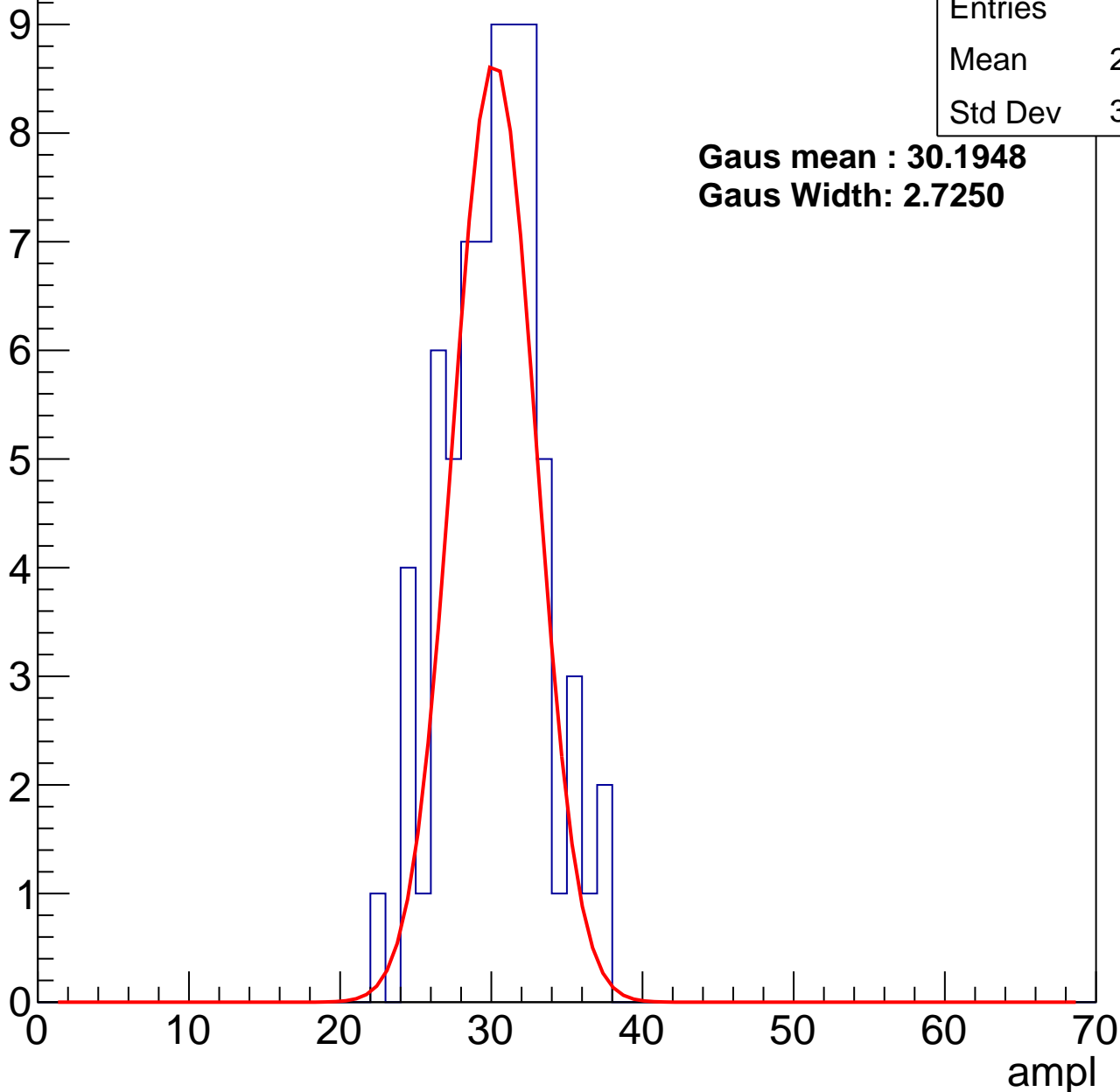
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	70
Mean	29.77
Std Dev	3.208

**Gaus mean : 30.1948**

**Gaus Width: 2.7250**



# B1L100S, U2-ch9, adc1

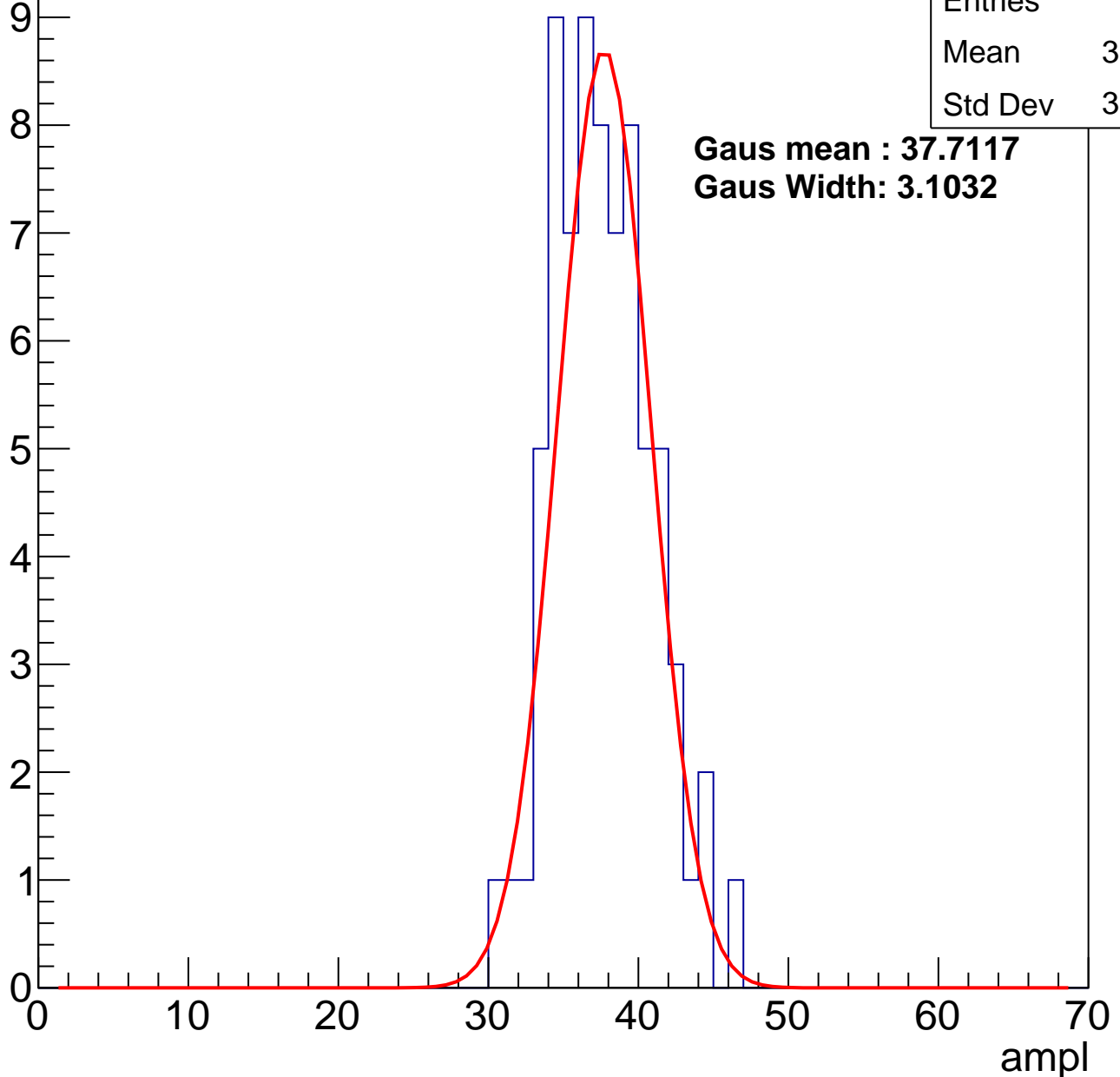
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	73
Mean	37.19
Std Dev	3.225

**Gaus mean : 37.7117**

**Gaus Width: 3.1032**



# B1L100S, U2-ch9, adc2

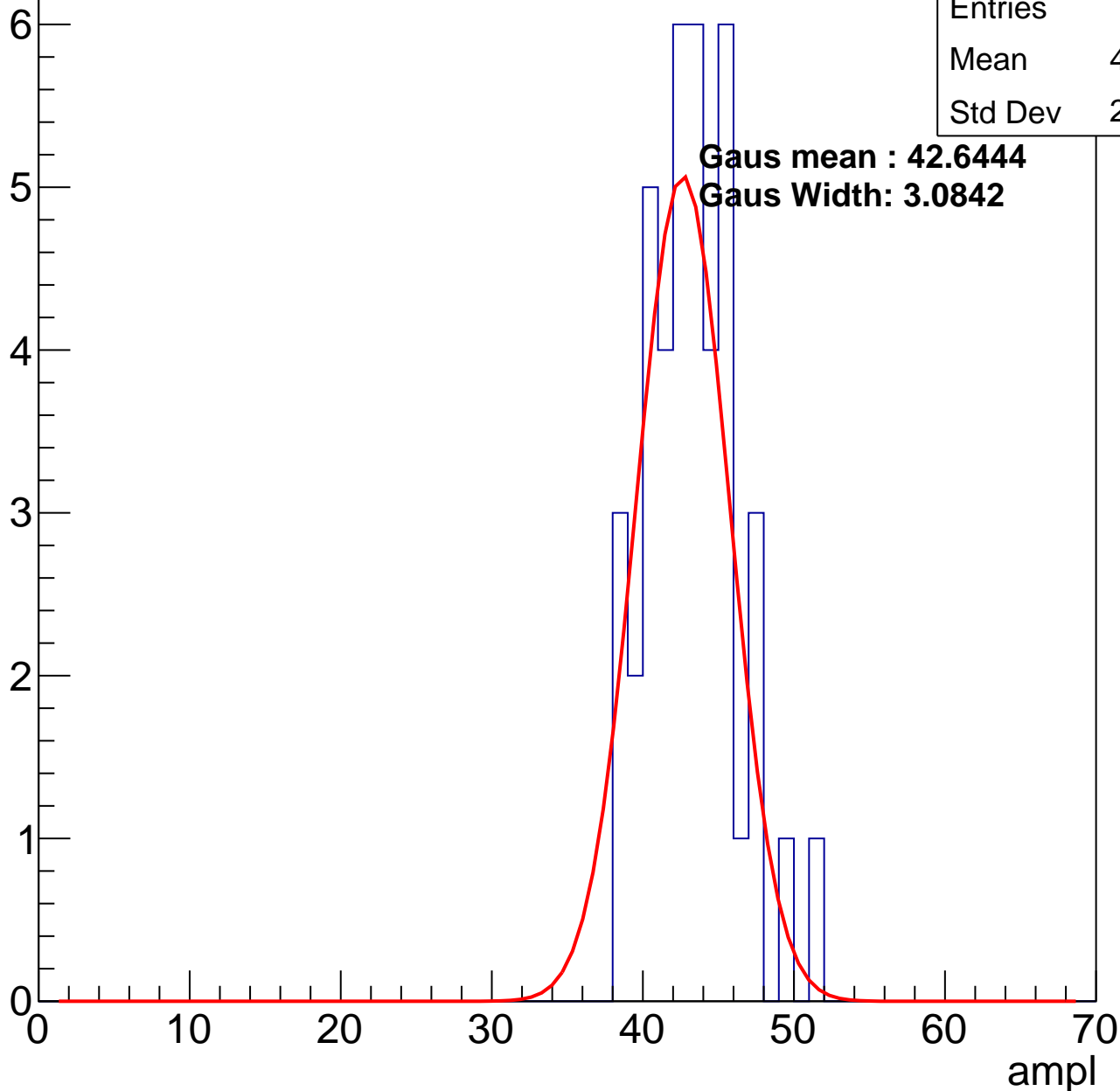
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	42
Mean	42.83
Std Dev	2.919

**Gaus mean : 42.6444**

**Gaus Width: 3.0842**



# B1L100S, U2-ch9, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	81
Mean	49.02
Std Dev	3.58

Entry

10

8

6

4

2

0

0

10

20

30

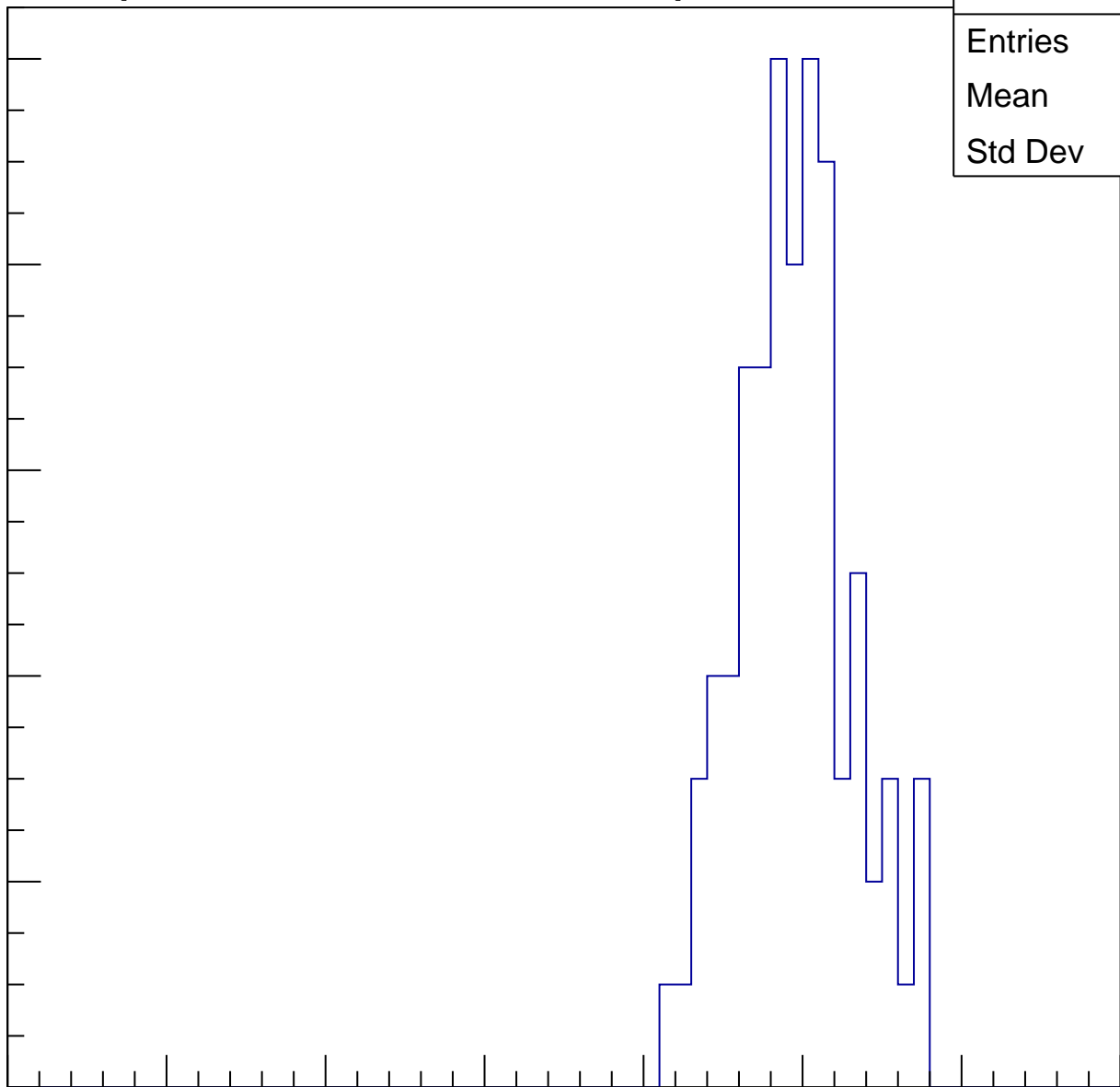
40

50

60

70

ampl

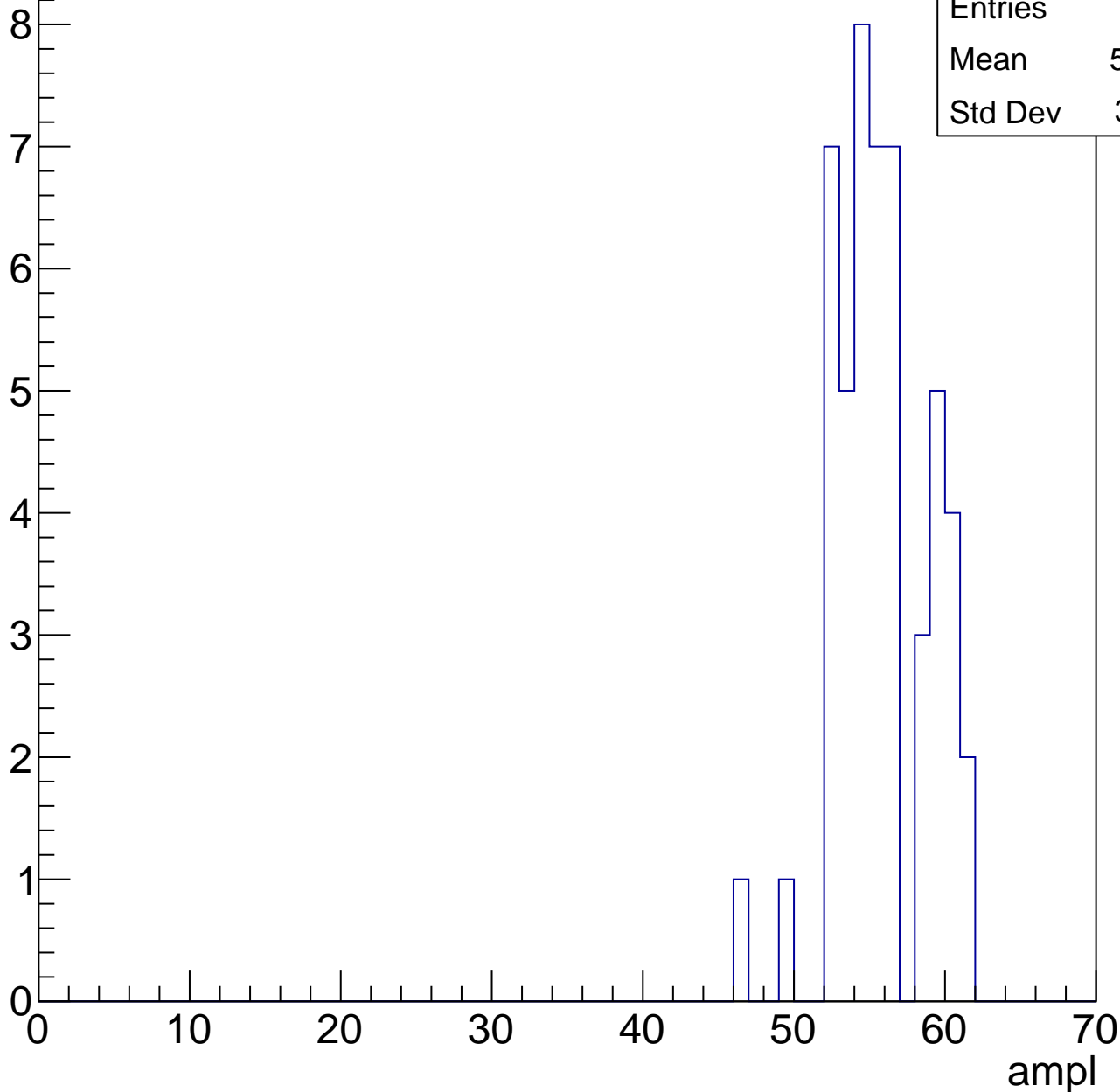


# B1L100S, U2-ch9, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	50
Mean	55.28
Std Dev	3.131



# B1L100S, U2-ch9, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

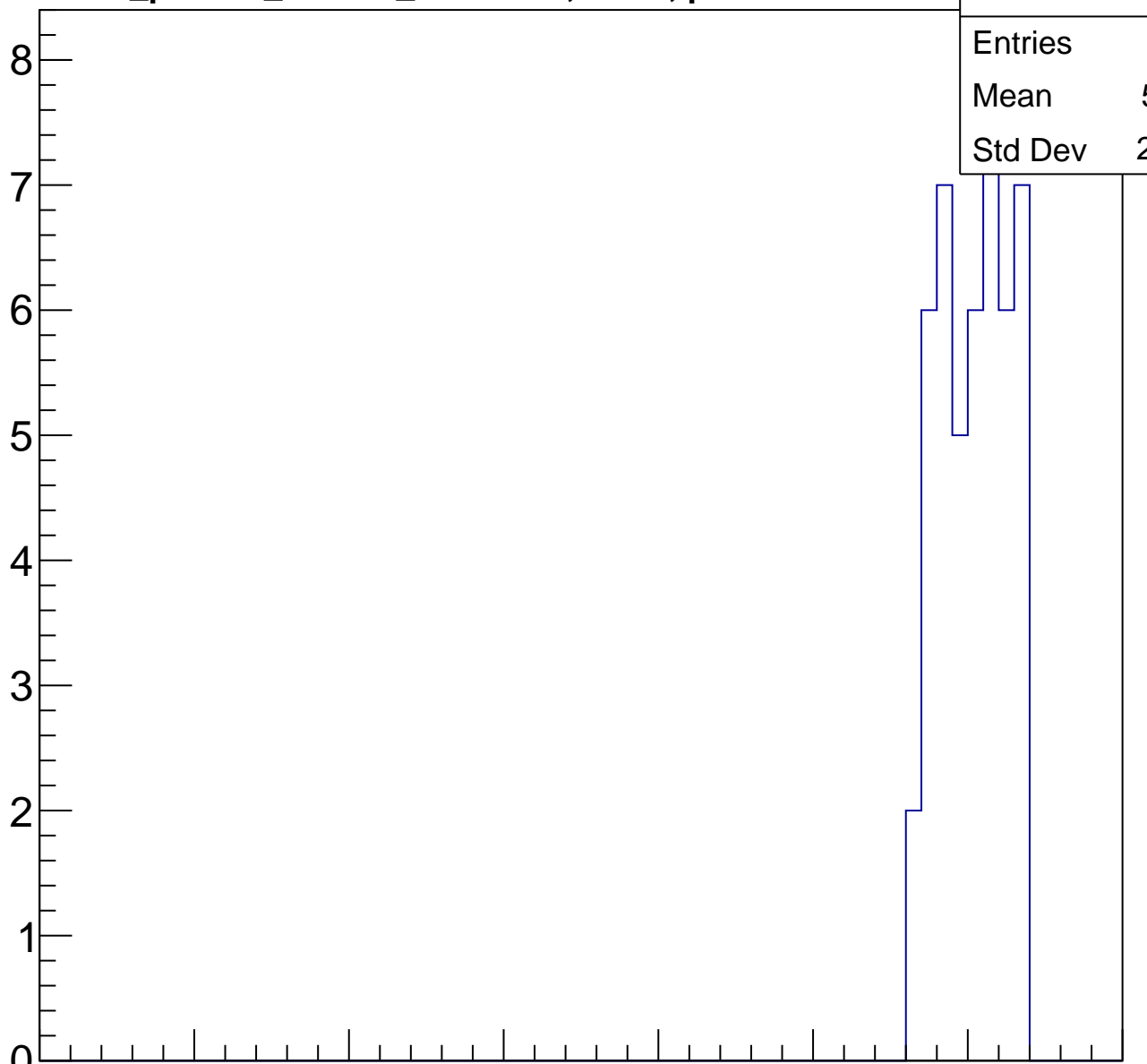
Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	47
Mean	59.91
Std Dev	2.132

ampl

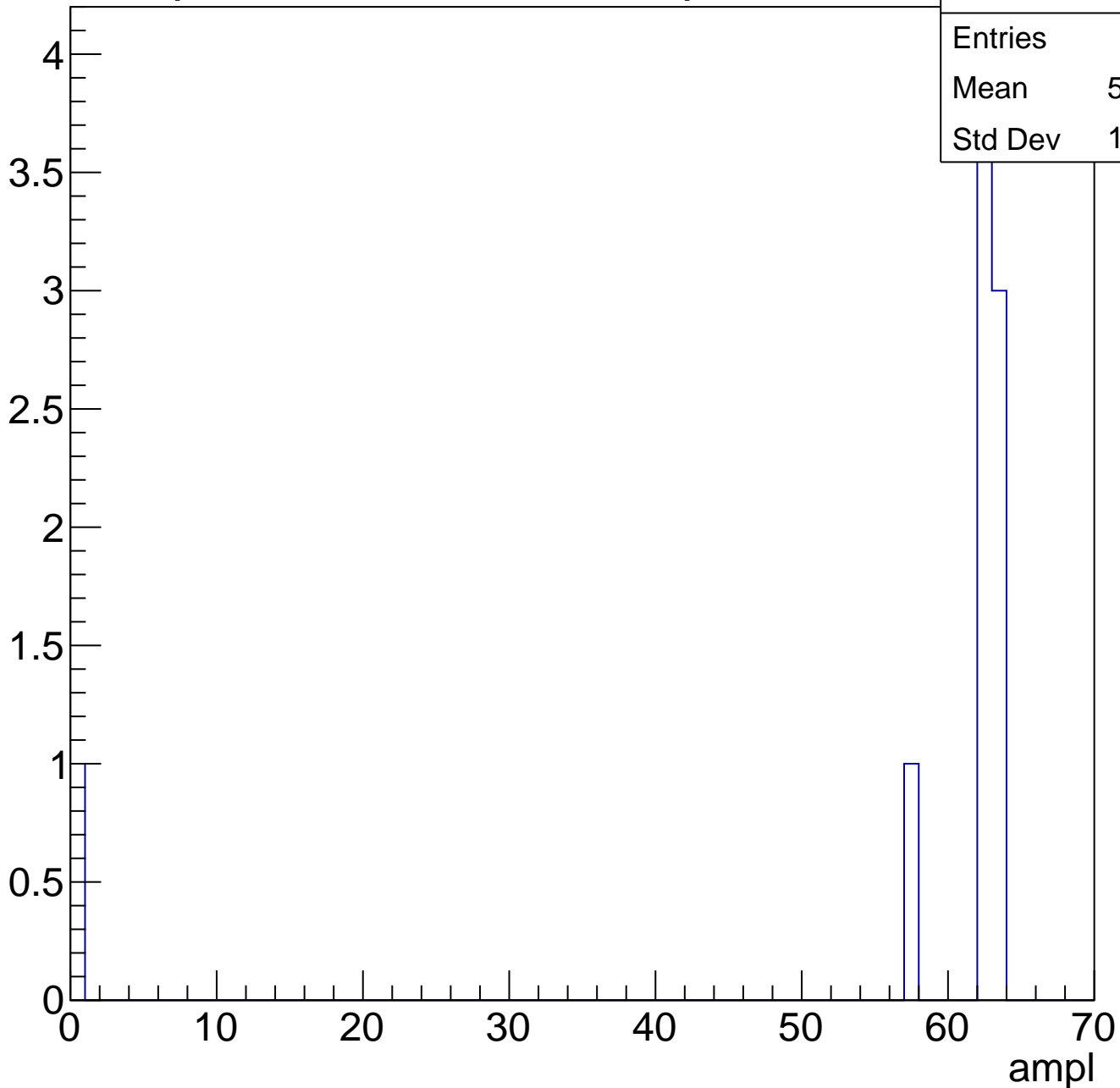
0 10 20 30 40 50 60 70



# B1L100S, U2-ch9, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	9
Mean	54.89
Std Dev	19.48



# B1L100S, U2-ch9, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



# B1L100S, U2-ch10, adc0

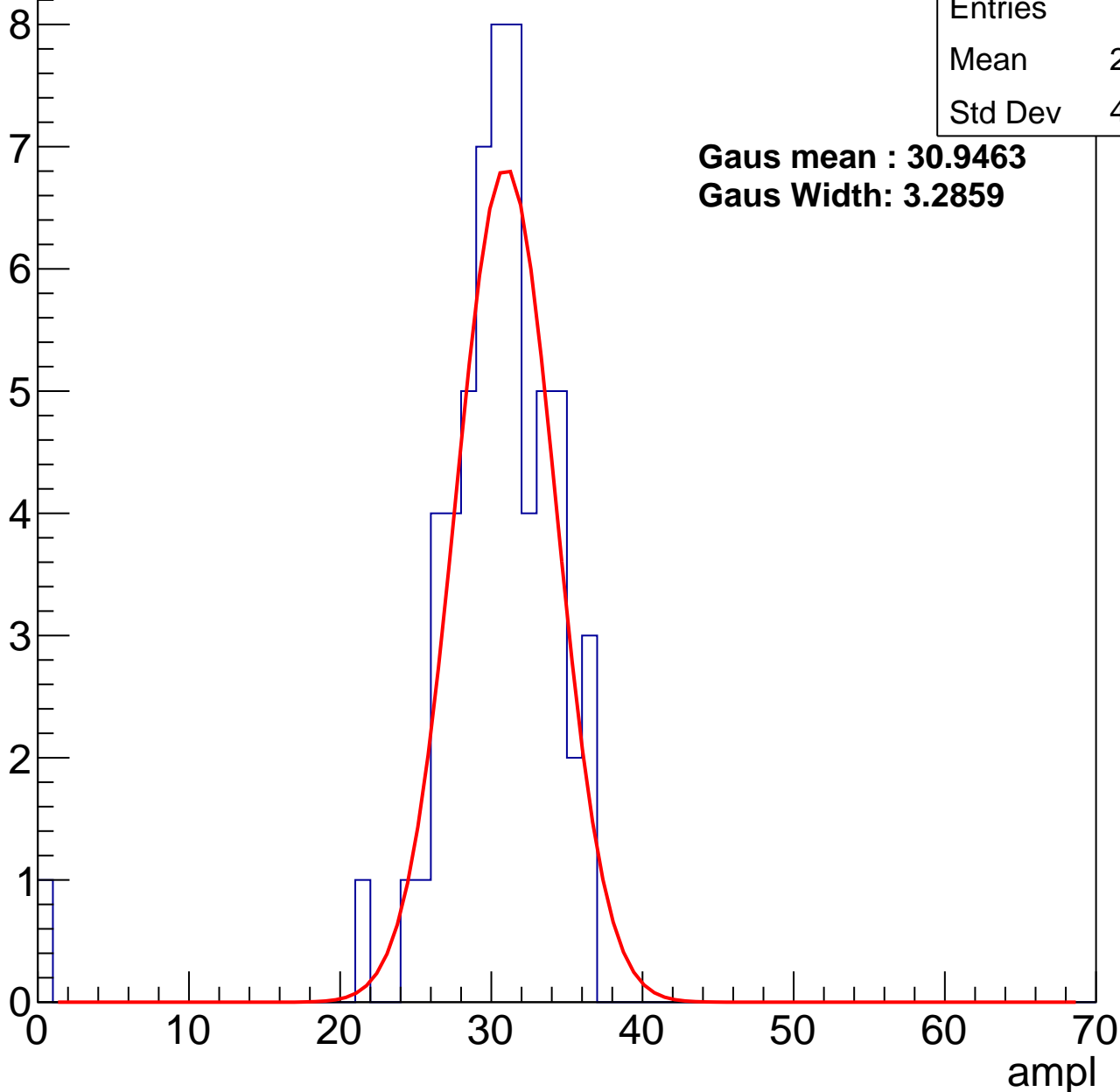
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	59
Mean	29.73
Std Dev	4.994

**Gaus mean : 30.9463**

**Gaus Width: 3.2859**



# B1L100S, U2-ch10, adc1

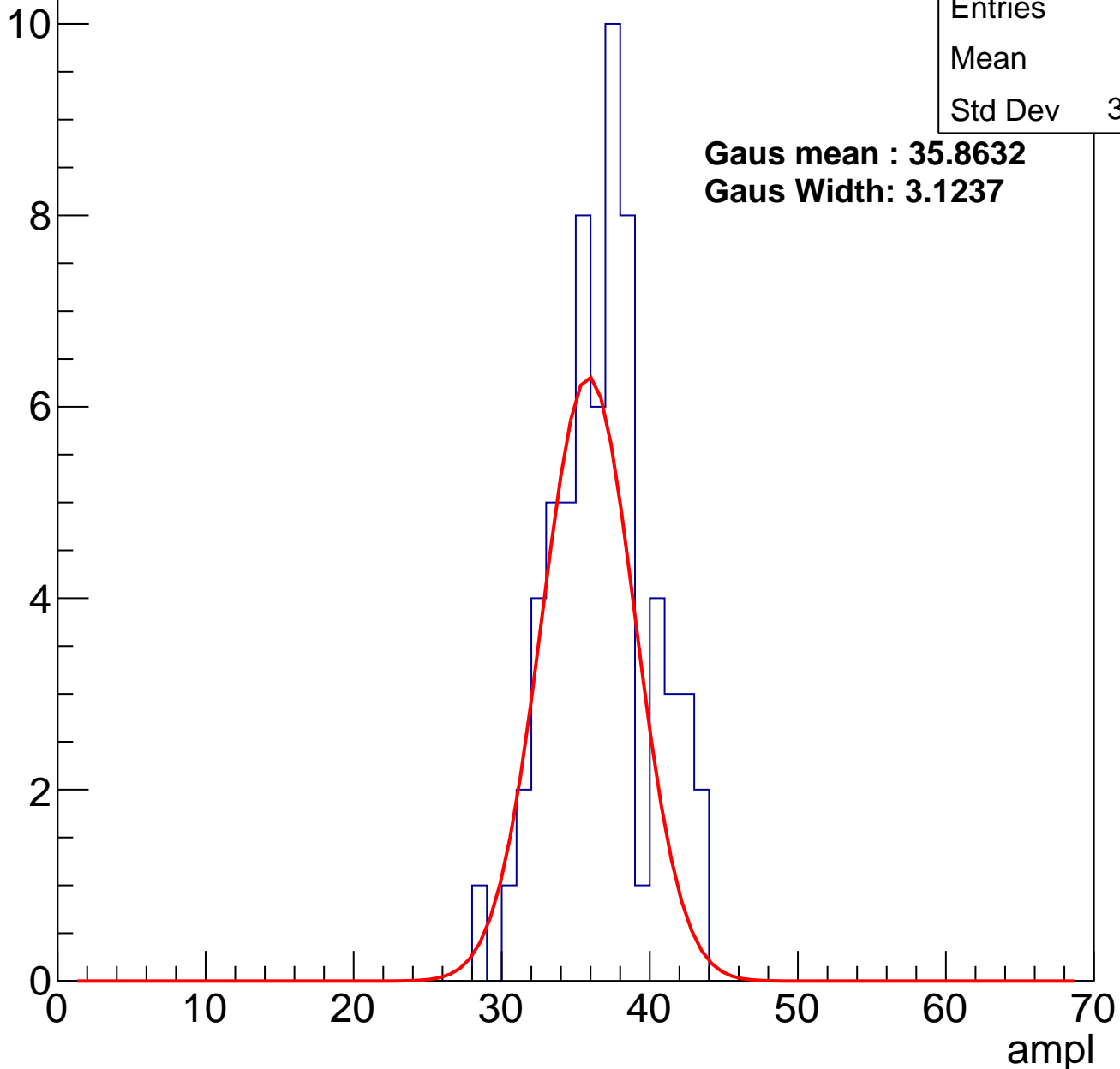
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	63
Mean	36.3
Std Dev	3.279

**Gaus mean : 35.8632**

**Gaus Width: 3.1237**

Entry



# B1L100S, U2-ch10, adc2

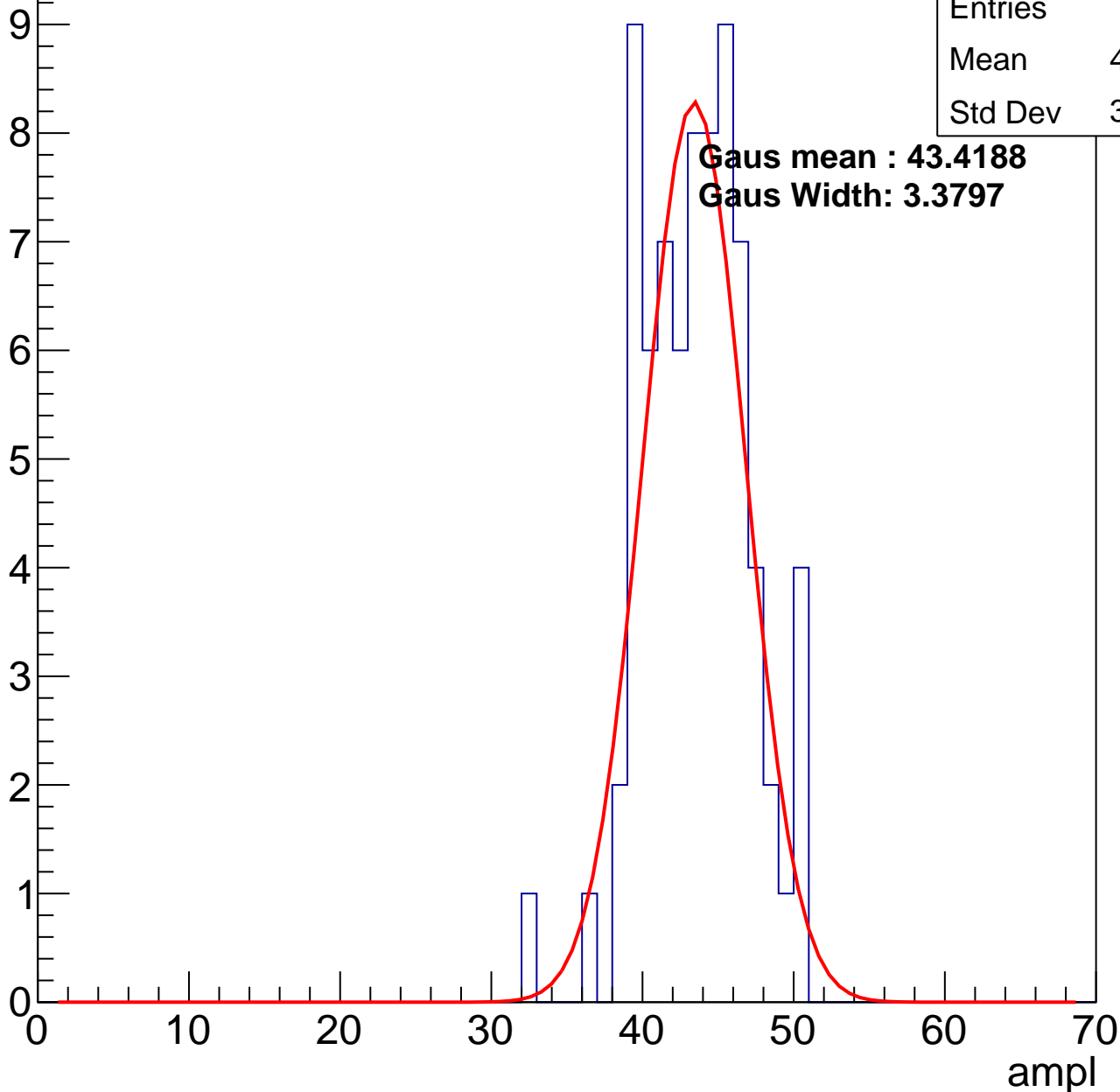
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	75
Mean	43.07
Std Dev	3.473

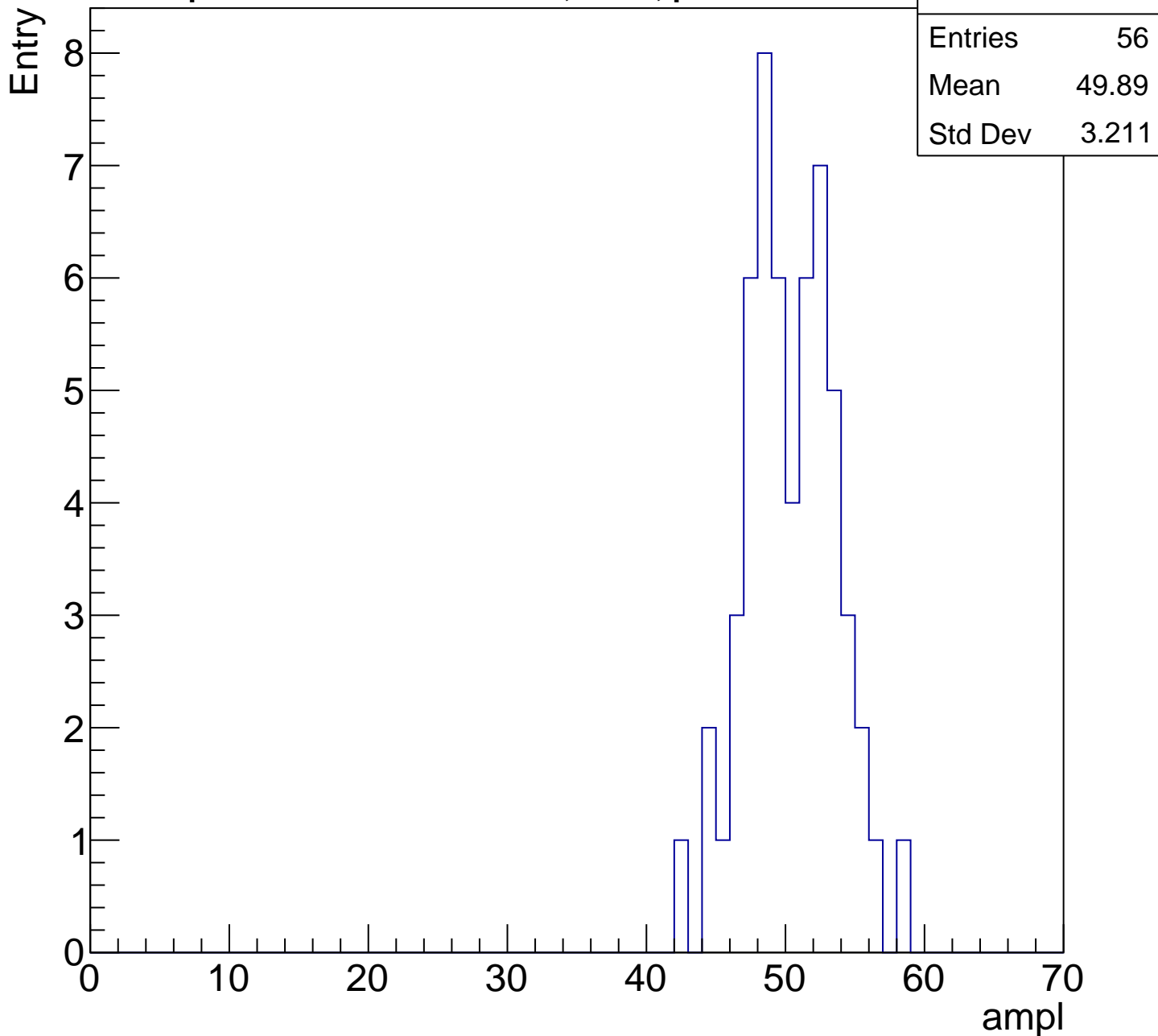
**Gaus mean : 43.4188**

**Gaus Width: 3.3797**



# B1L100S, U2-ch10, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

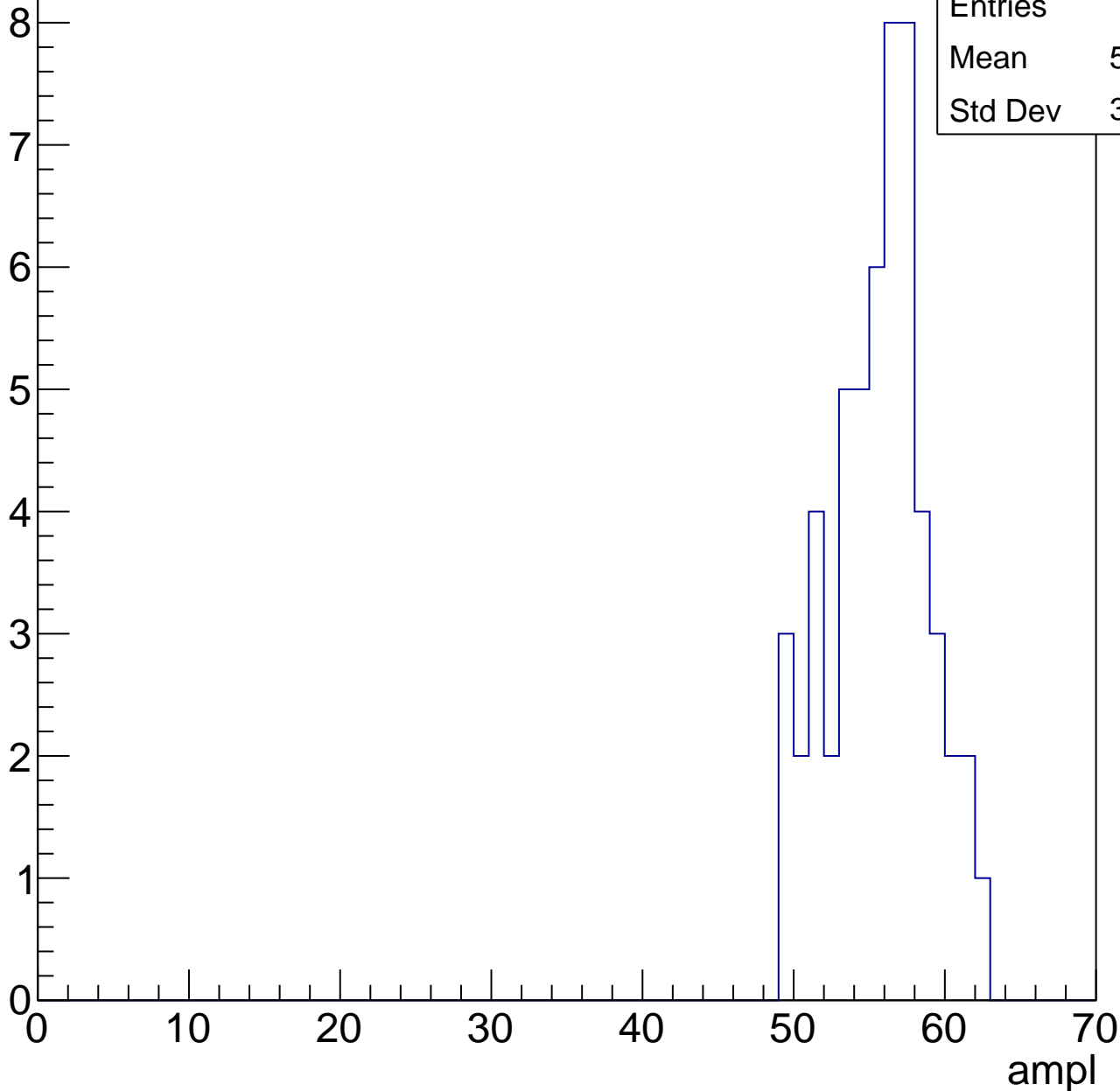


# B1L100S, U2-ch10, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	55
Mean	55.22
Std Dev	3.183



# B1L100S, U2-ch10, adc5

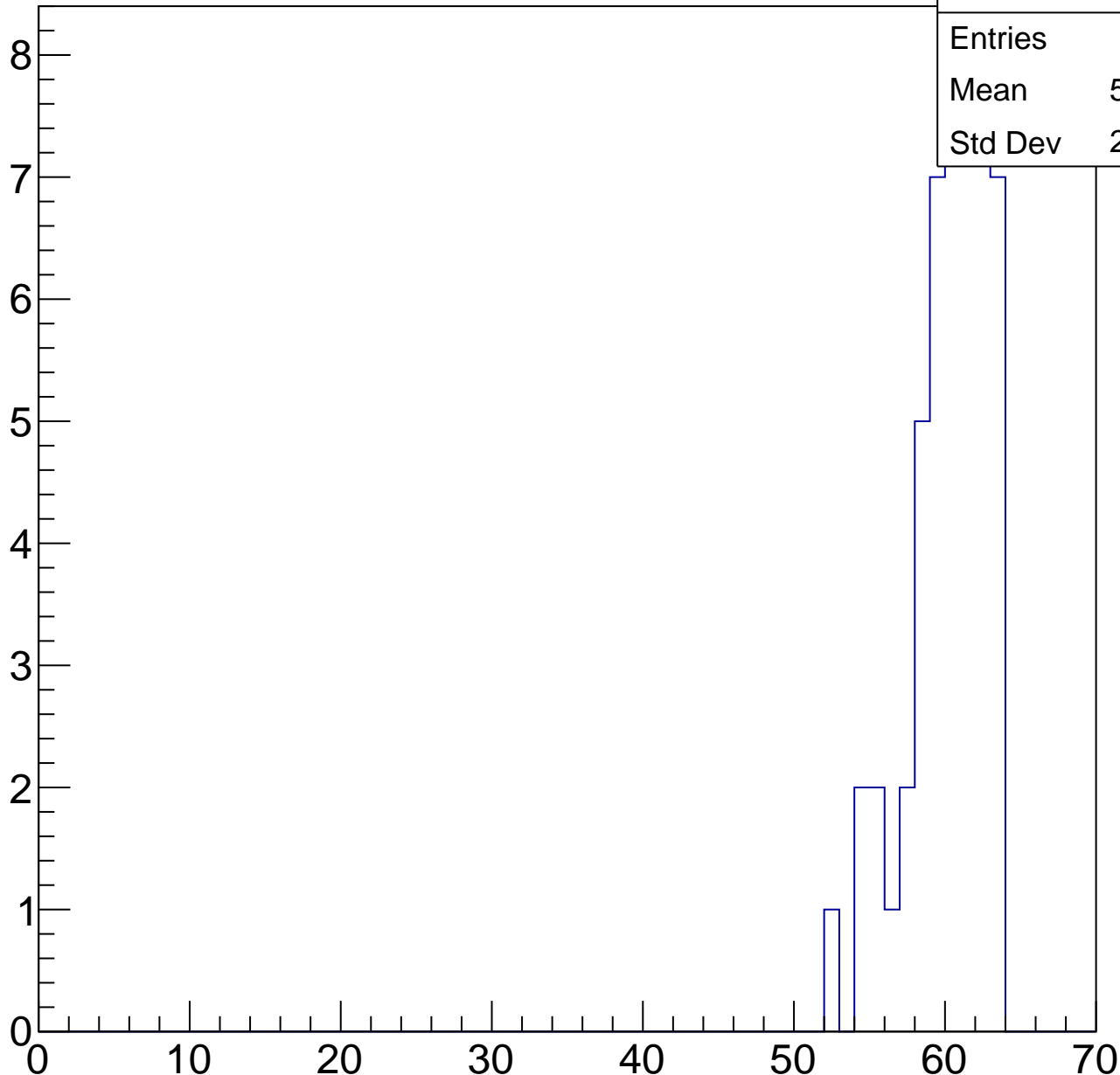
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	51
Mean	59.76
Std Dev	2.609

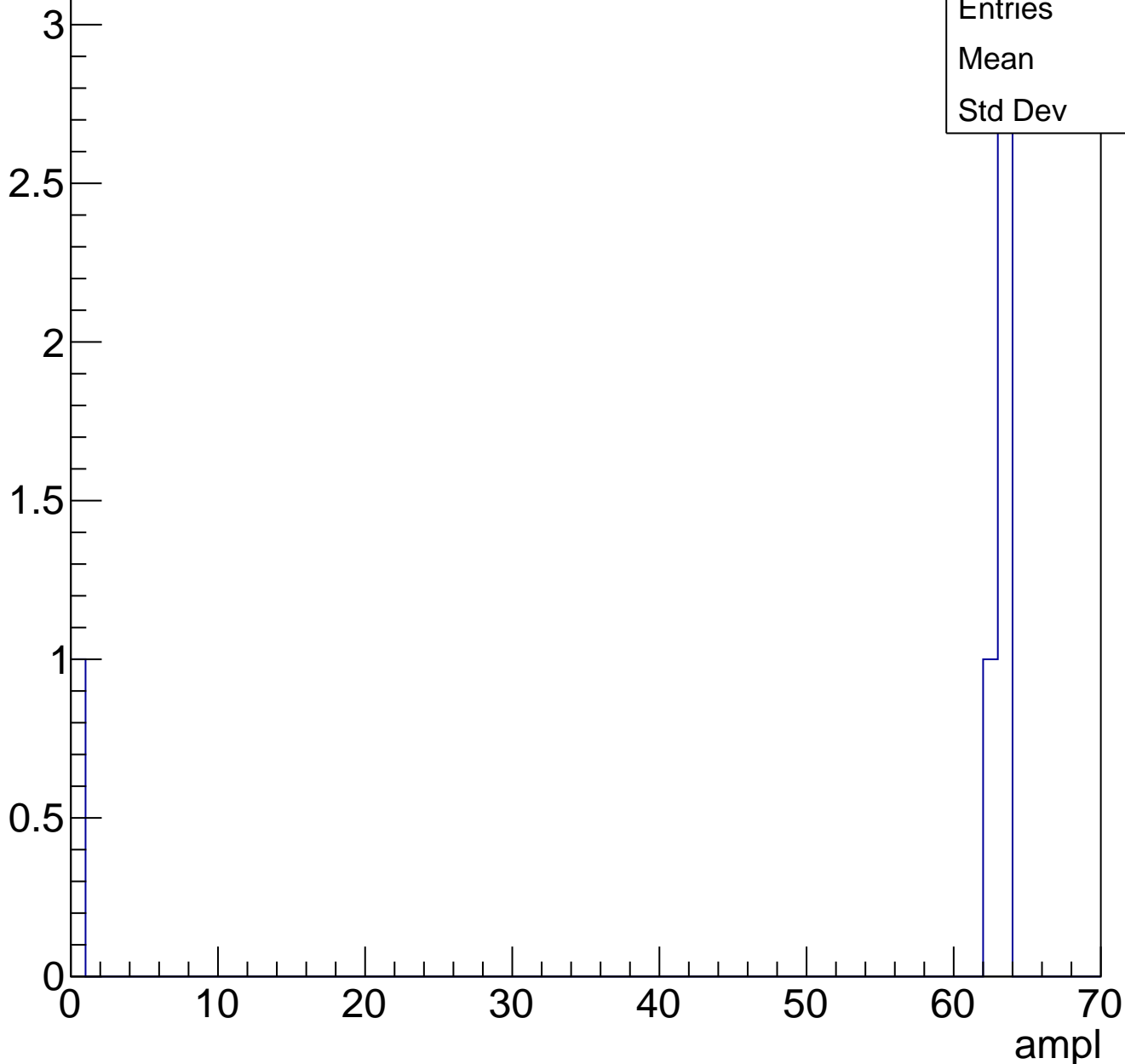
ampl



# B1L100S, U2-ch10, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry





# B1L100S, U2-ch10, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L100S, U2-ch11, adc0

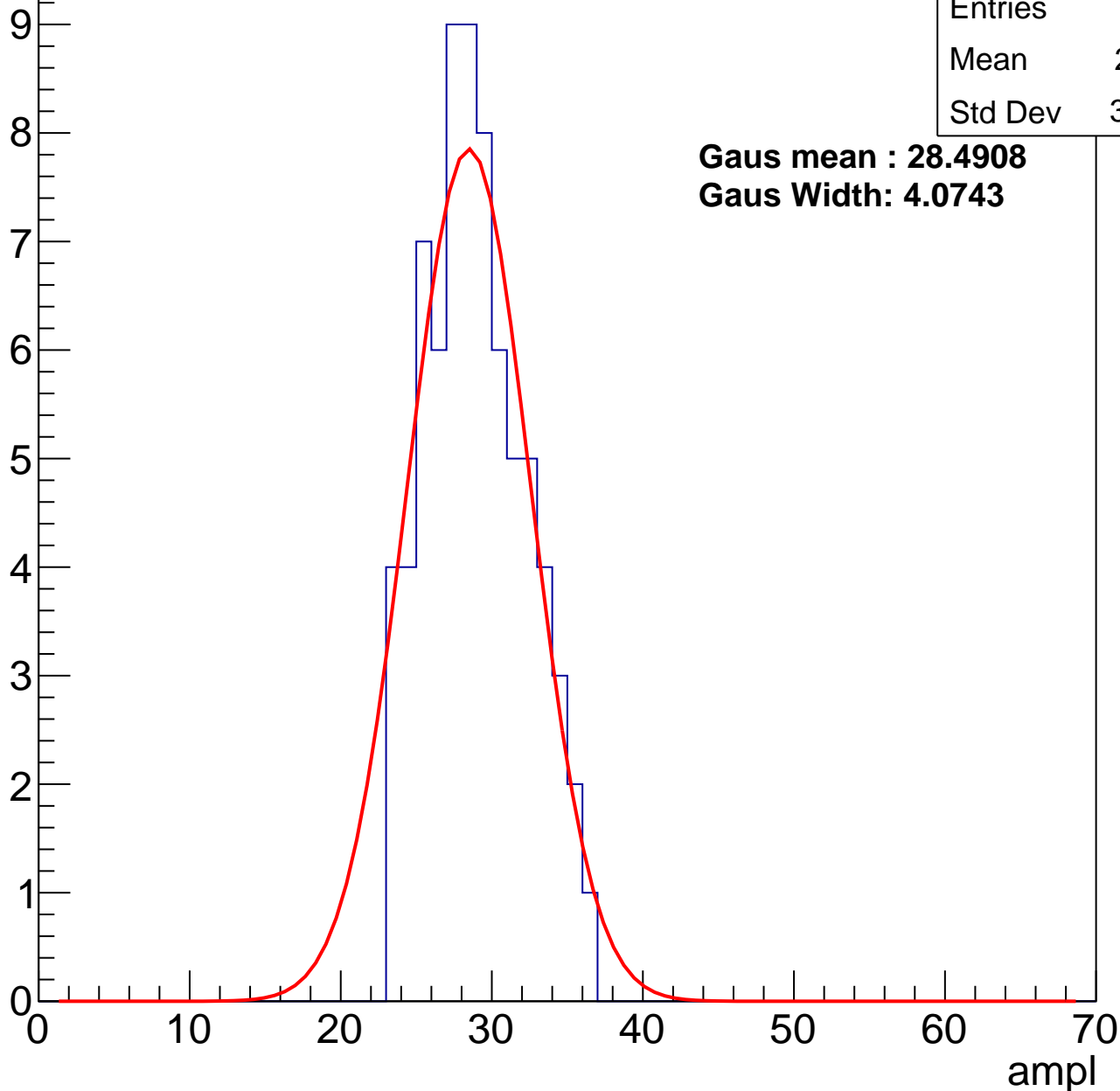
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	73
Mean	28.51
Std Dev	3.244

**Gaus mean : 28.4908**

**Gaus Width: 4.0743**



# B1L100S, U2-ch11, adc1

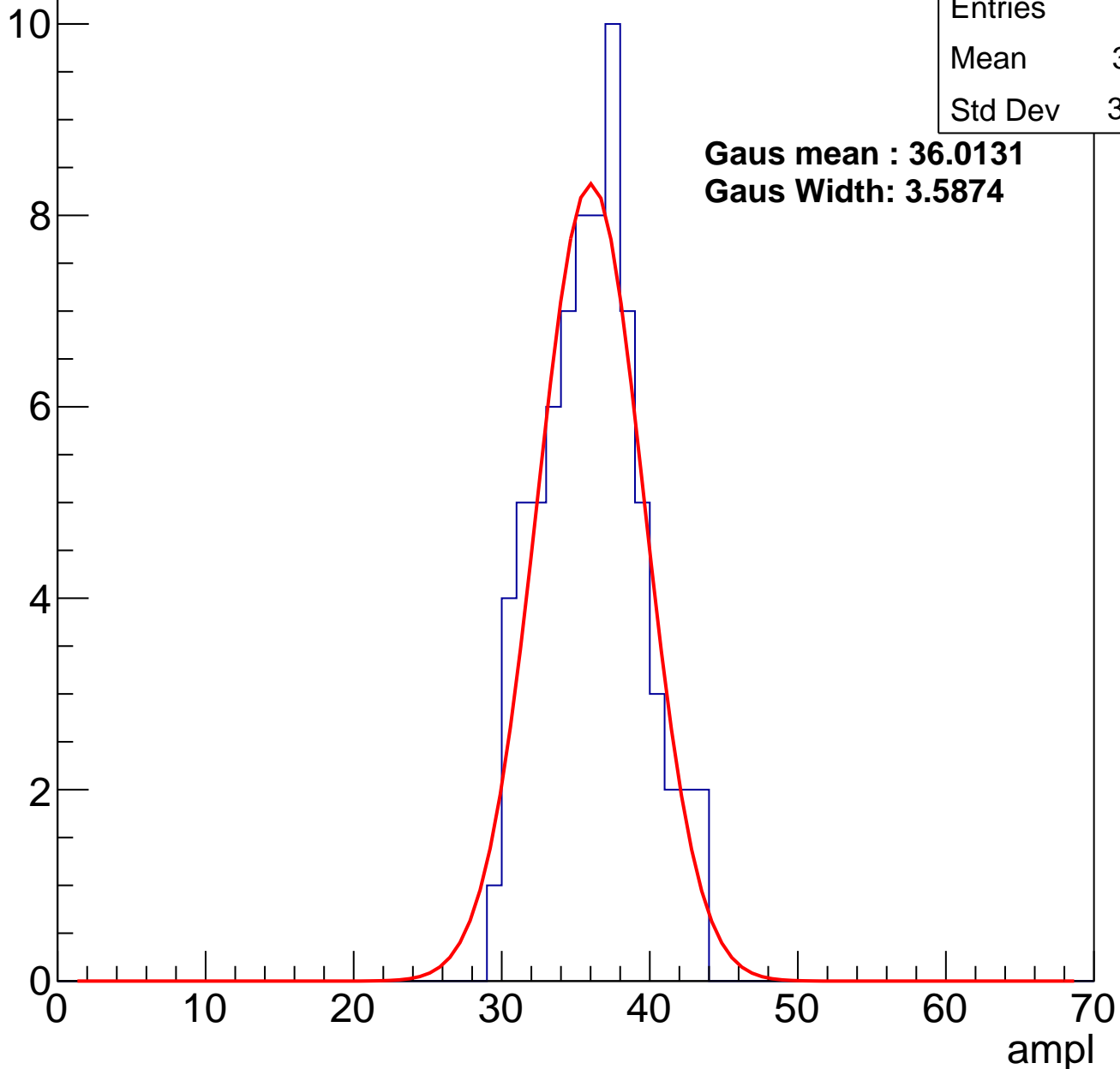
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	75
Mean	35.61
Std Dev	3.322

**Gaus mean : 36.0131**

**Gaus Width: 3.5874**

Entry



# B1L100S, U2-ch11, adc2

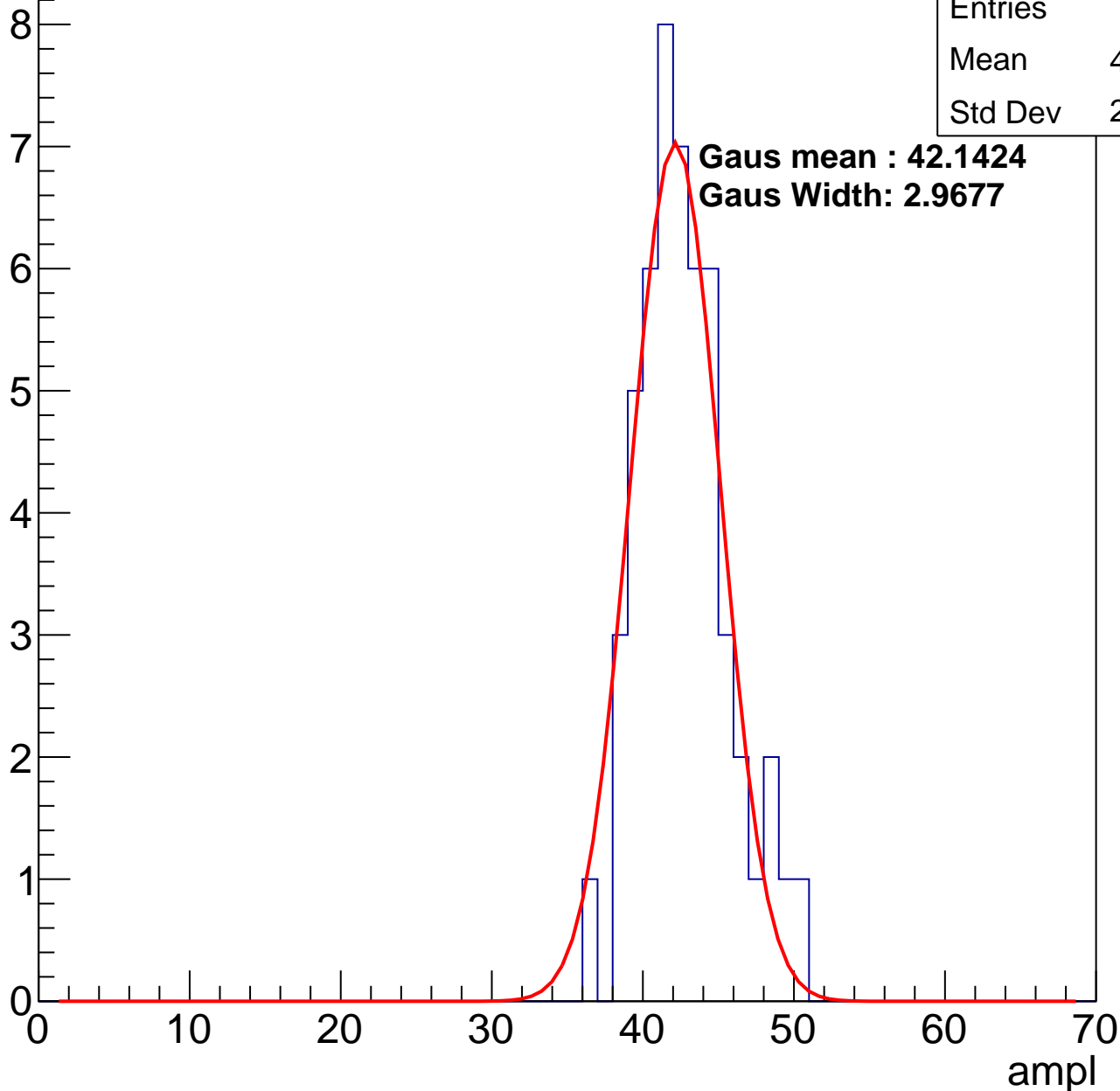
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	52
Mean	42.27
Std Dev	2.962

**Gaus mean : 42.1424**

**Gaus Width: 2.9677**

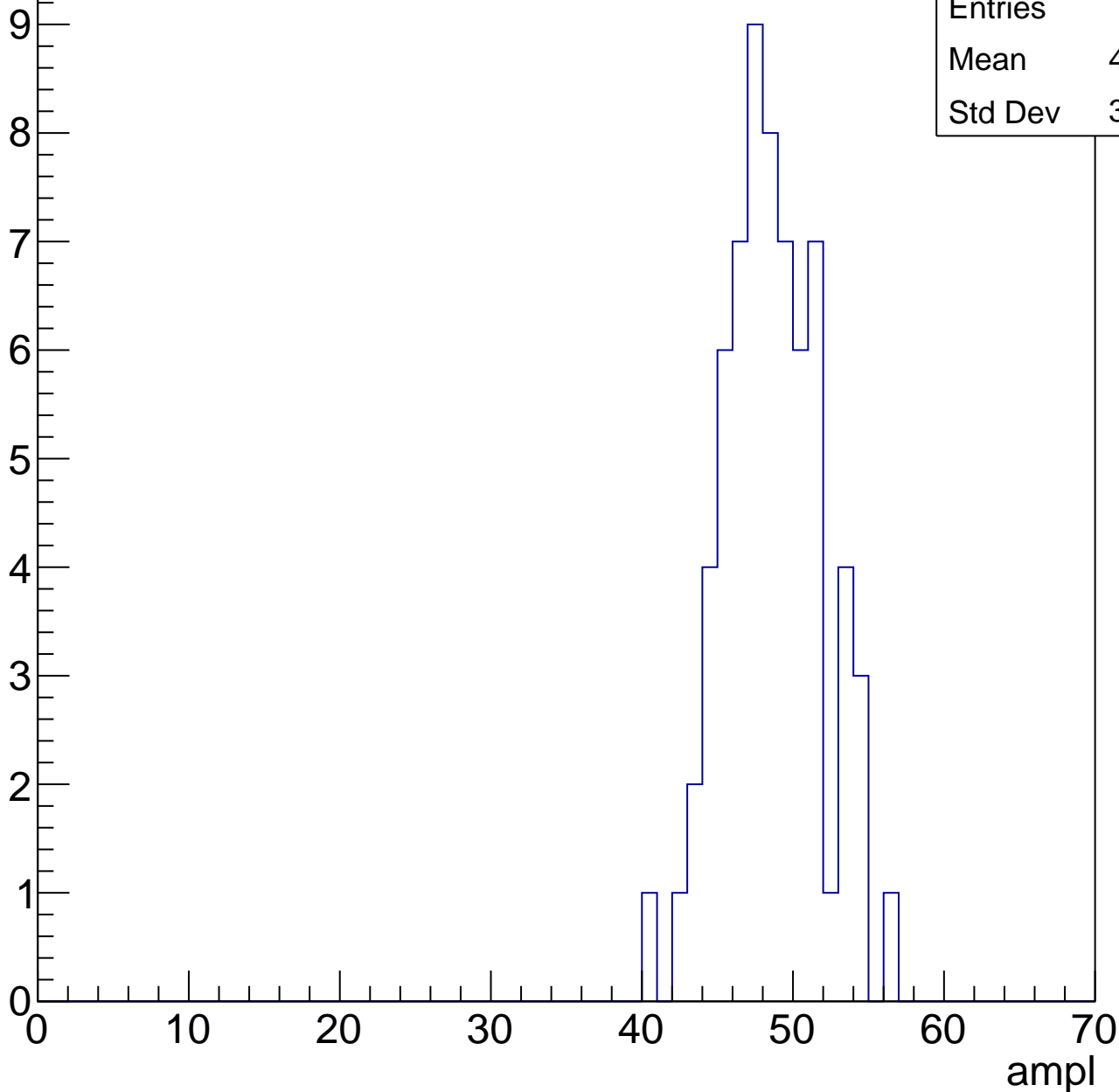


# B1L100S, U2-ch11, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

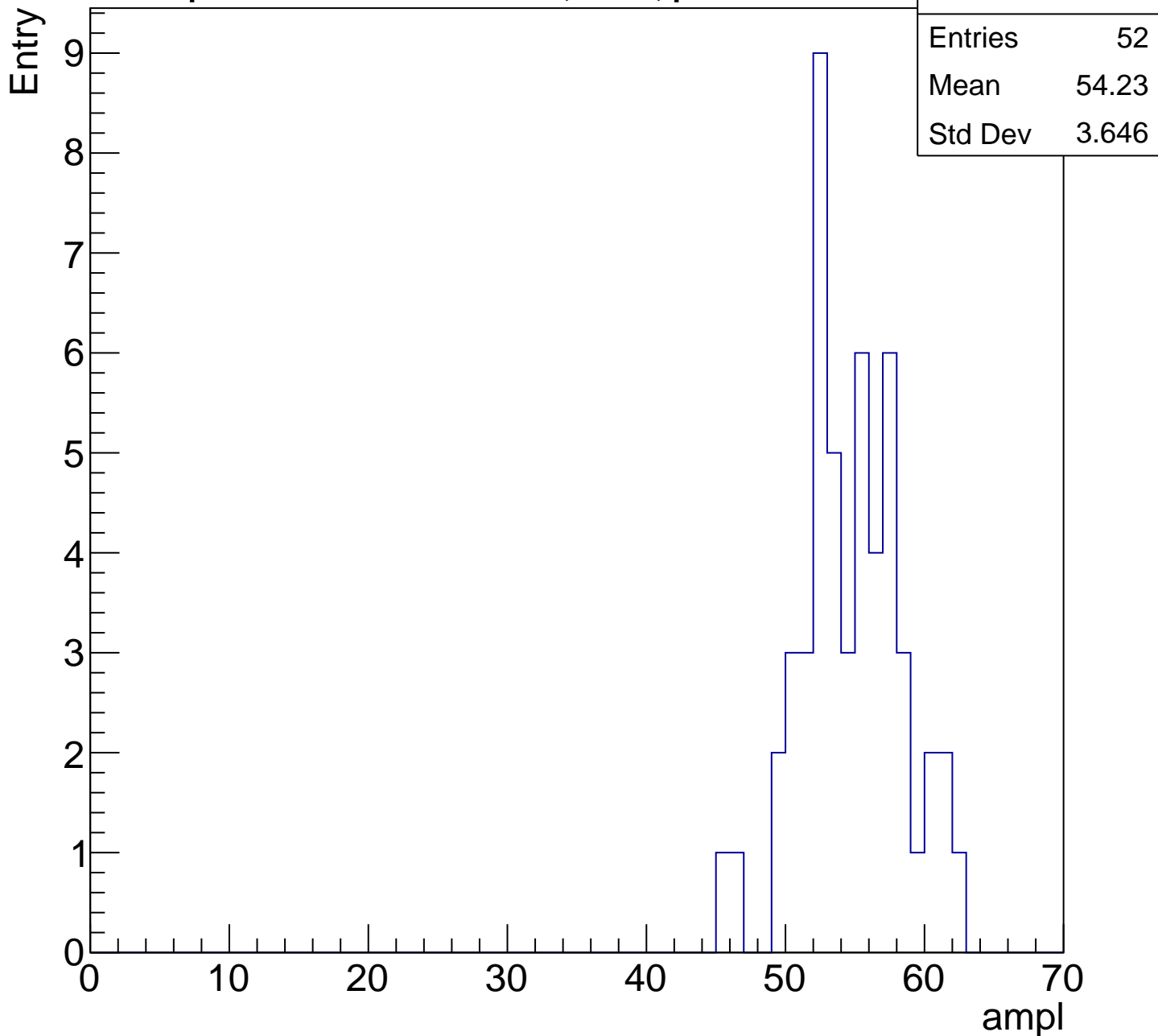
Entry

Entries	67
Mean	48.13
Std Dev	3.199



# B1L100S, U2-ch11, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2



# B1L100S, U2-ch11, adc5

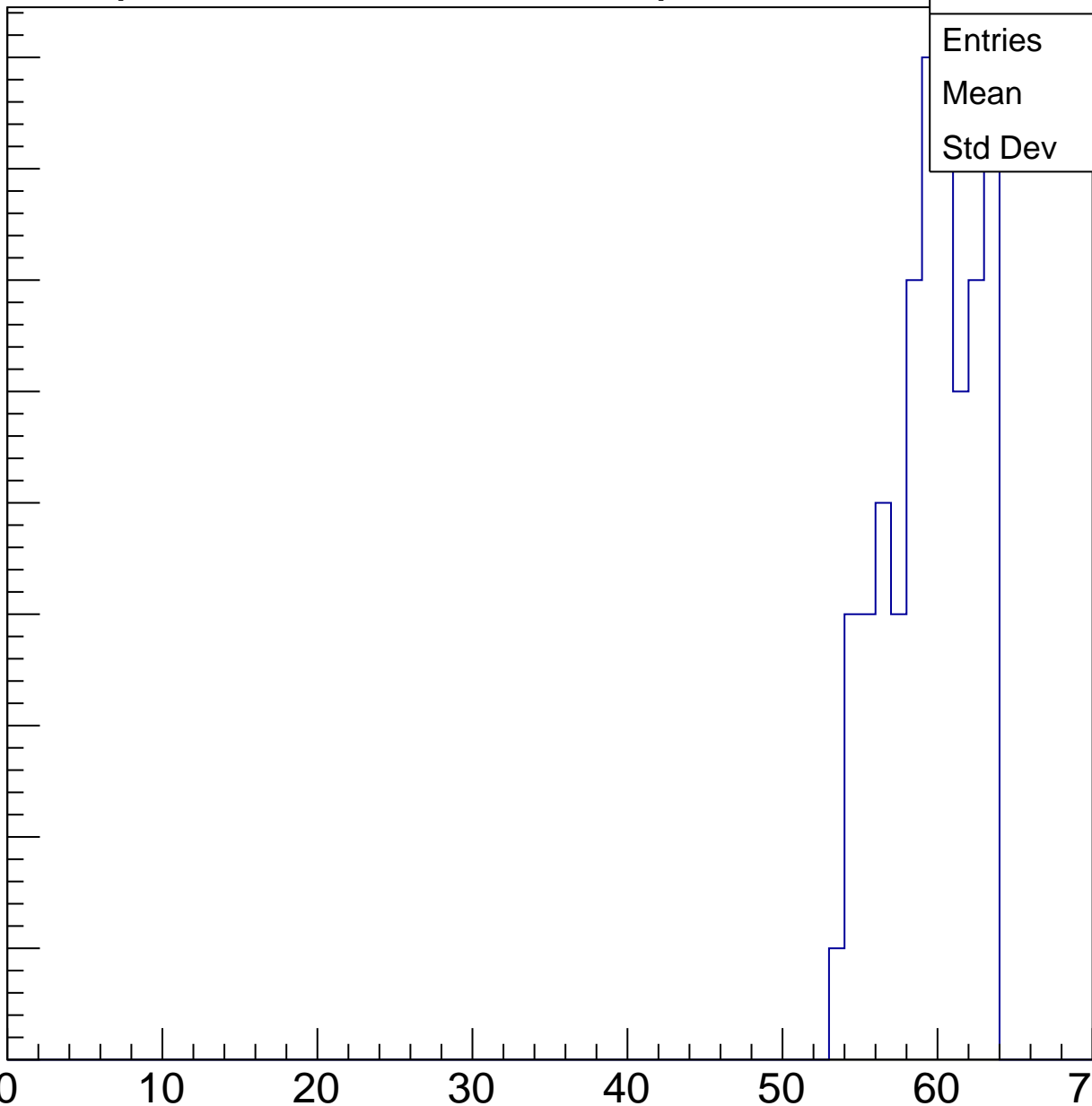
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	64
Mean	59.08
Std Dev	2.813

ampl



# B1L100S, U2-ch11, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

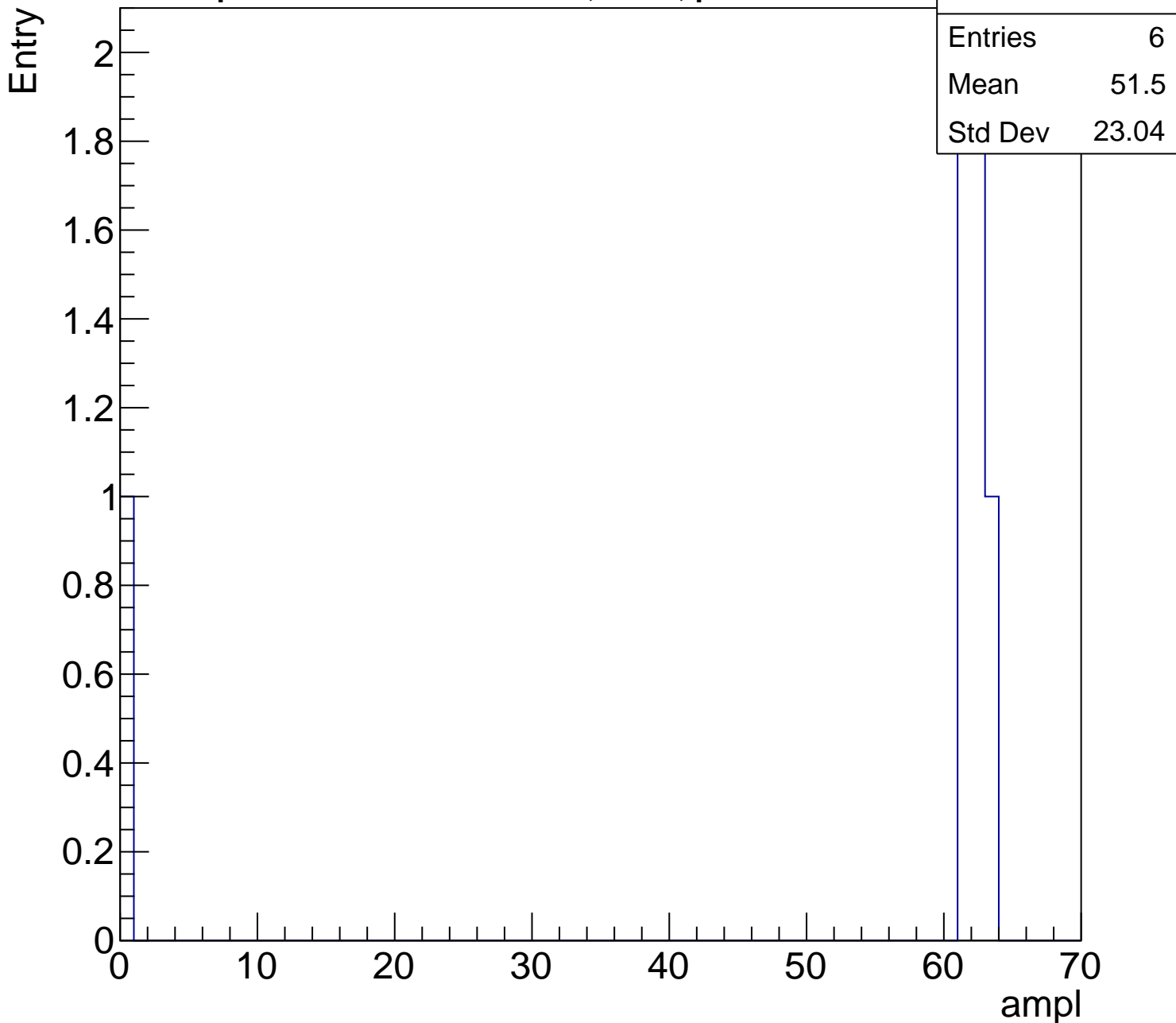
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	6
Mean	51.5
Std Dev	23.04

0 10 20 30 40 50 60 70

ampl





# B1L100S, U2-ch11, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L100S, U2-ch12, adc0

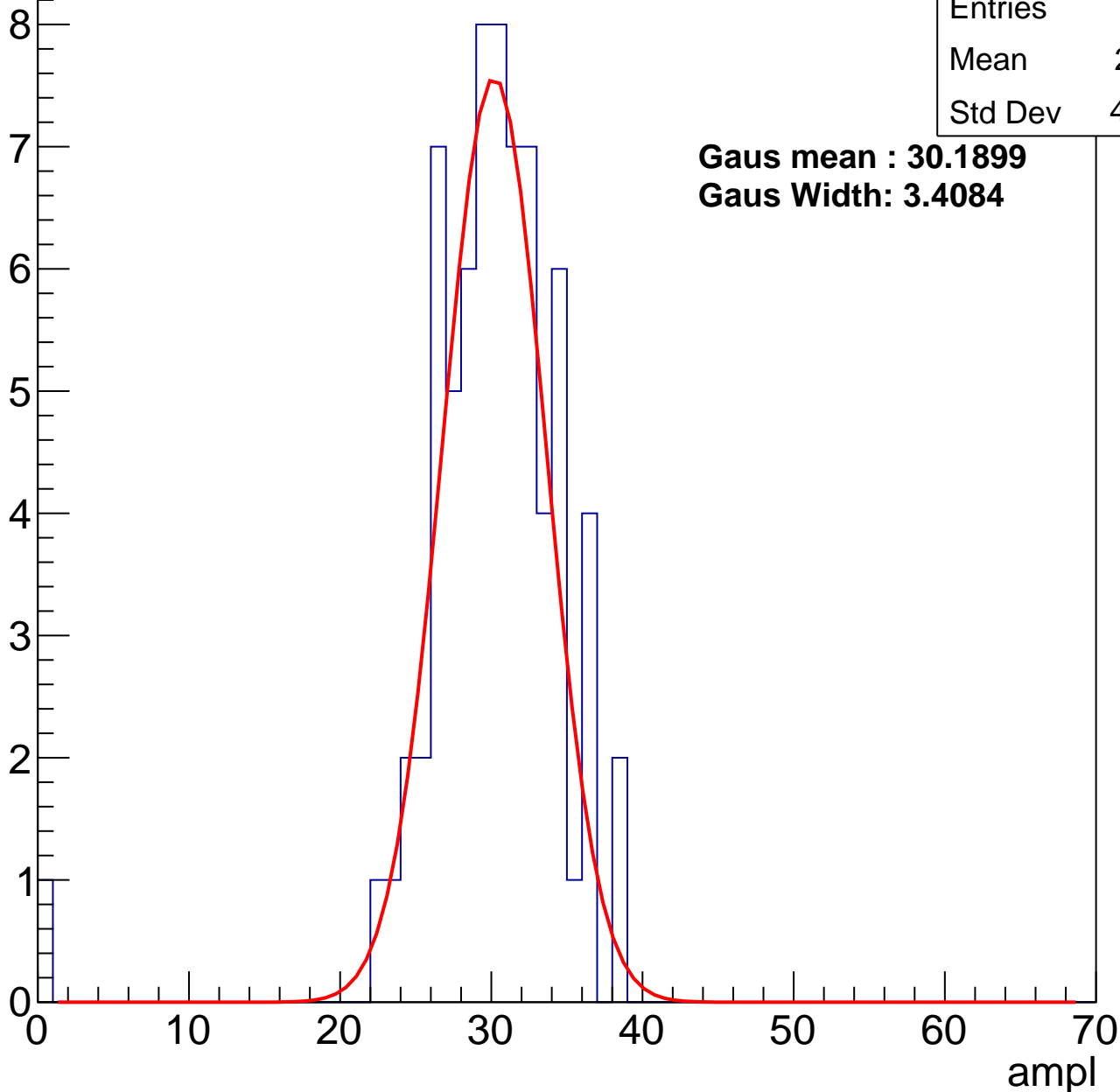
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	72
Mean	29.61
Std Dev	4.968

**Gaus mean : 30.1899**

**Gaus Width: 3.4084**



# B1L100S, U2-ch12, adc1

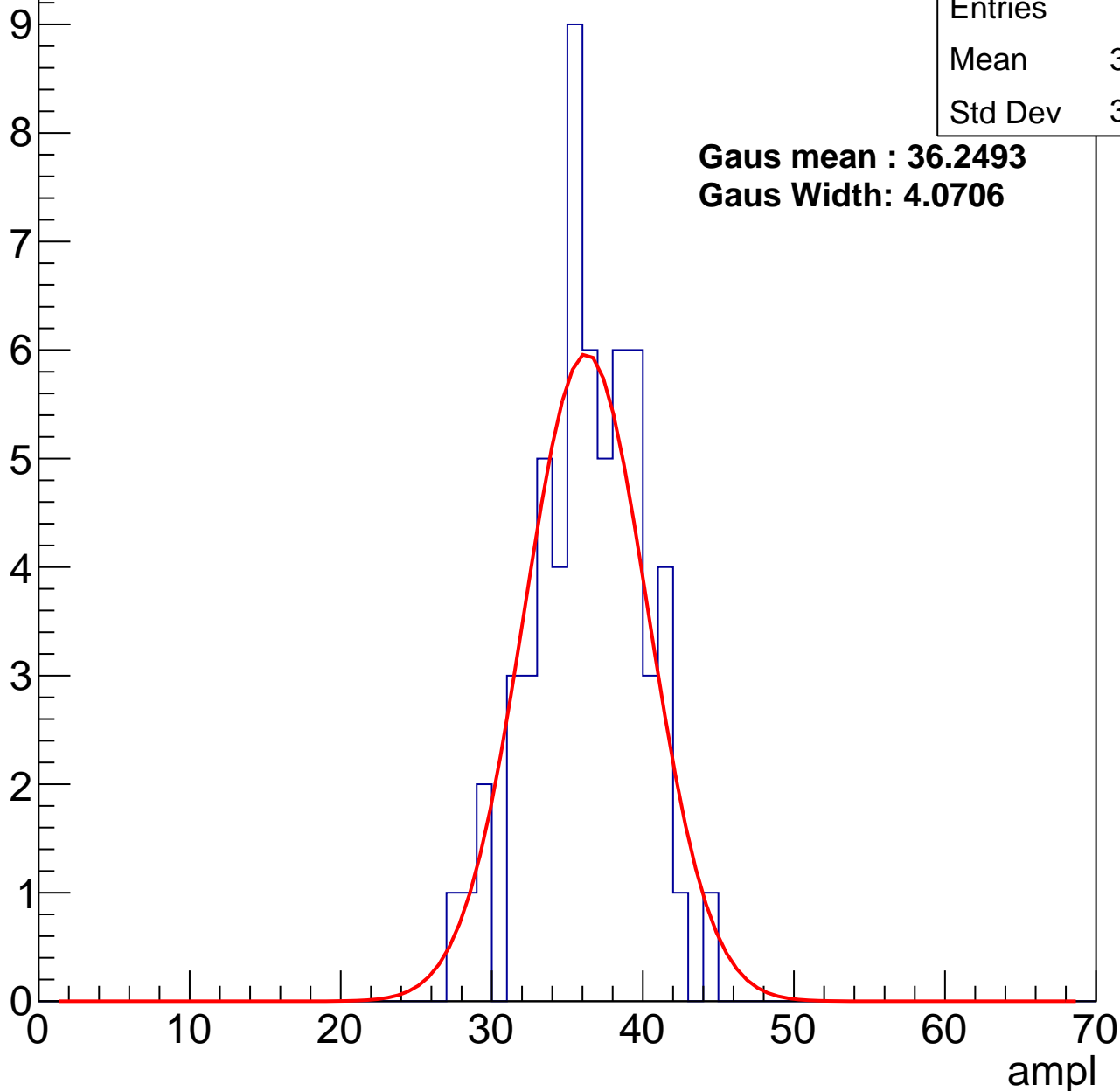
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	60
Mean	35.85
Std Dev	3.572

**Gaus mean : 36.2493**

**Gaus Width: 4.0706**



# B1L100S, U2-ch12, adc2

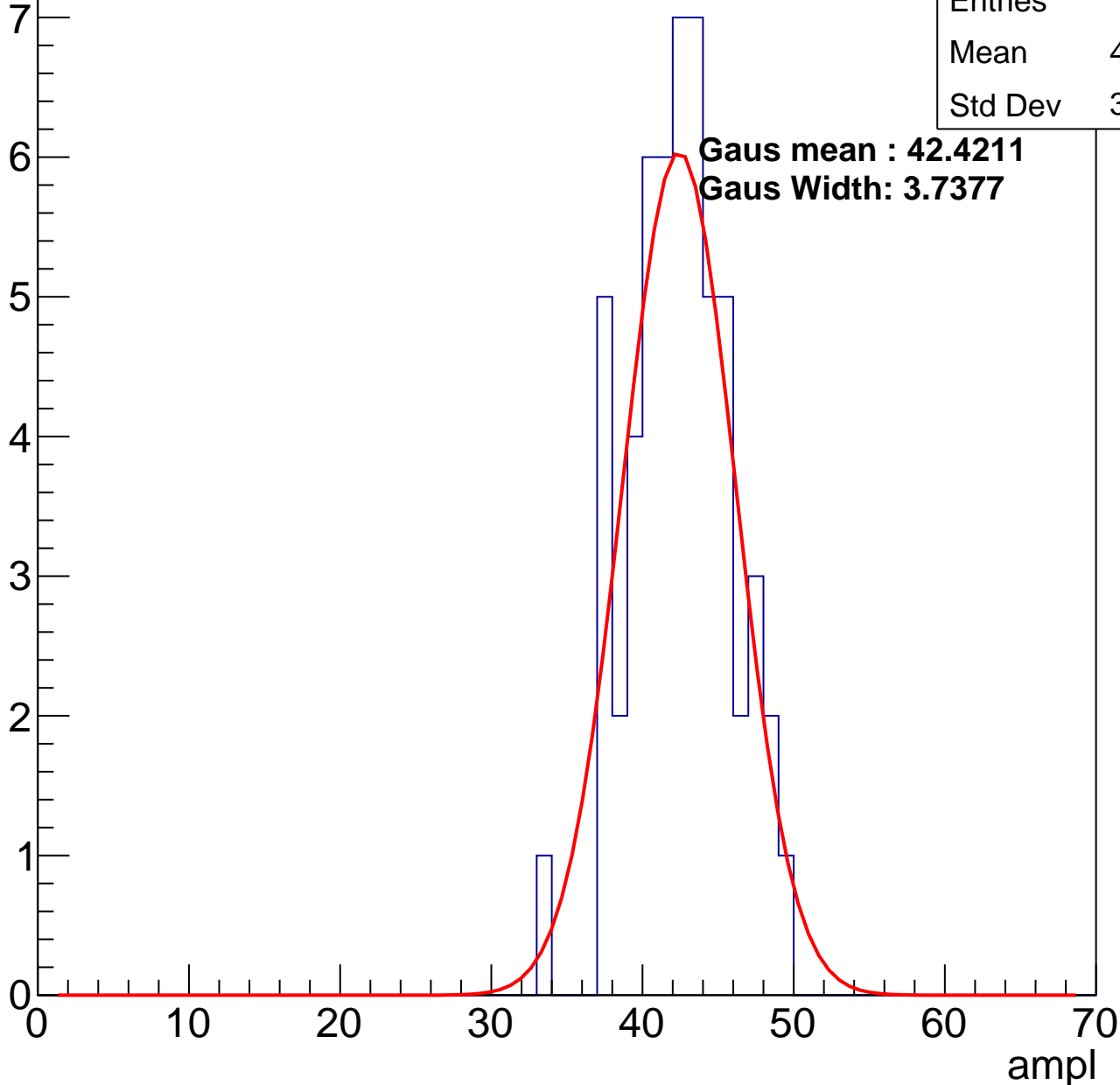
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	56
Mean	42.04
Std Dev	3.284

**Gaus mean : 42.4211**

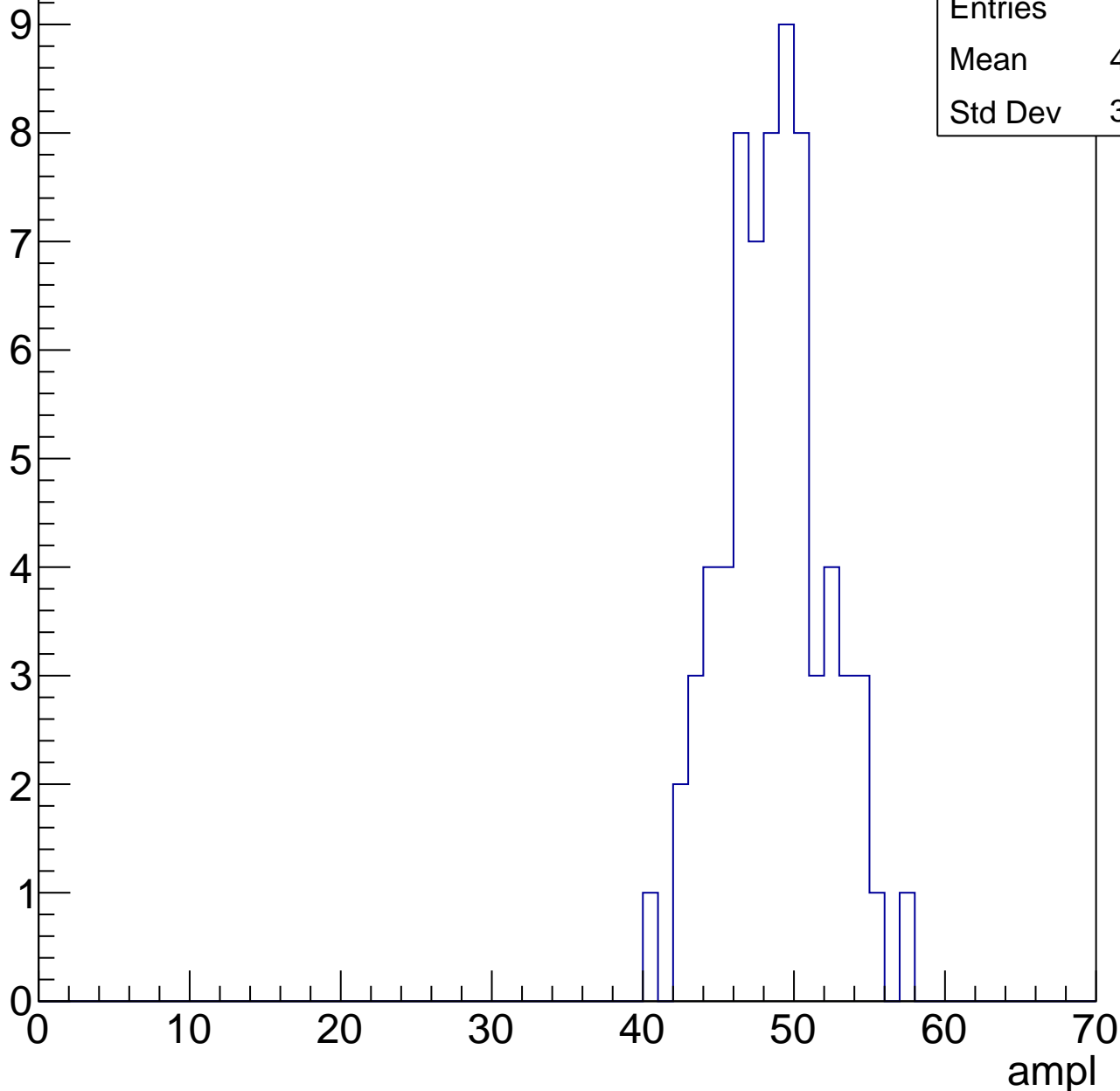
**Gaus Width: 3.7377**



# B1L100S, U2-ch12, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

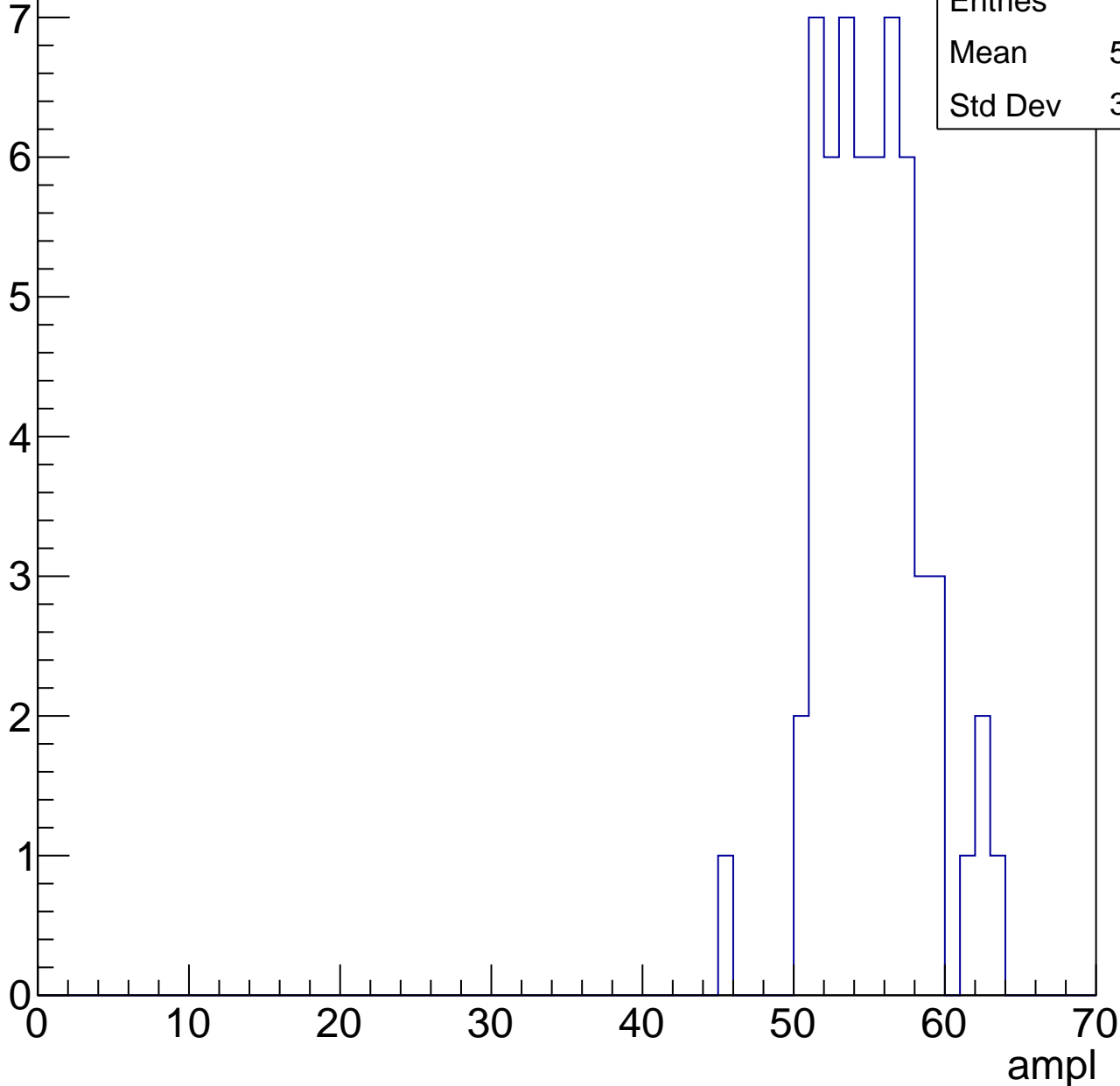


# B1L100S, U2-ch12, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	58
Mean	54.69
Std Dev	3.344



# B1L100S, U2-ch12, adc5

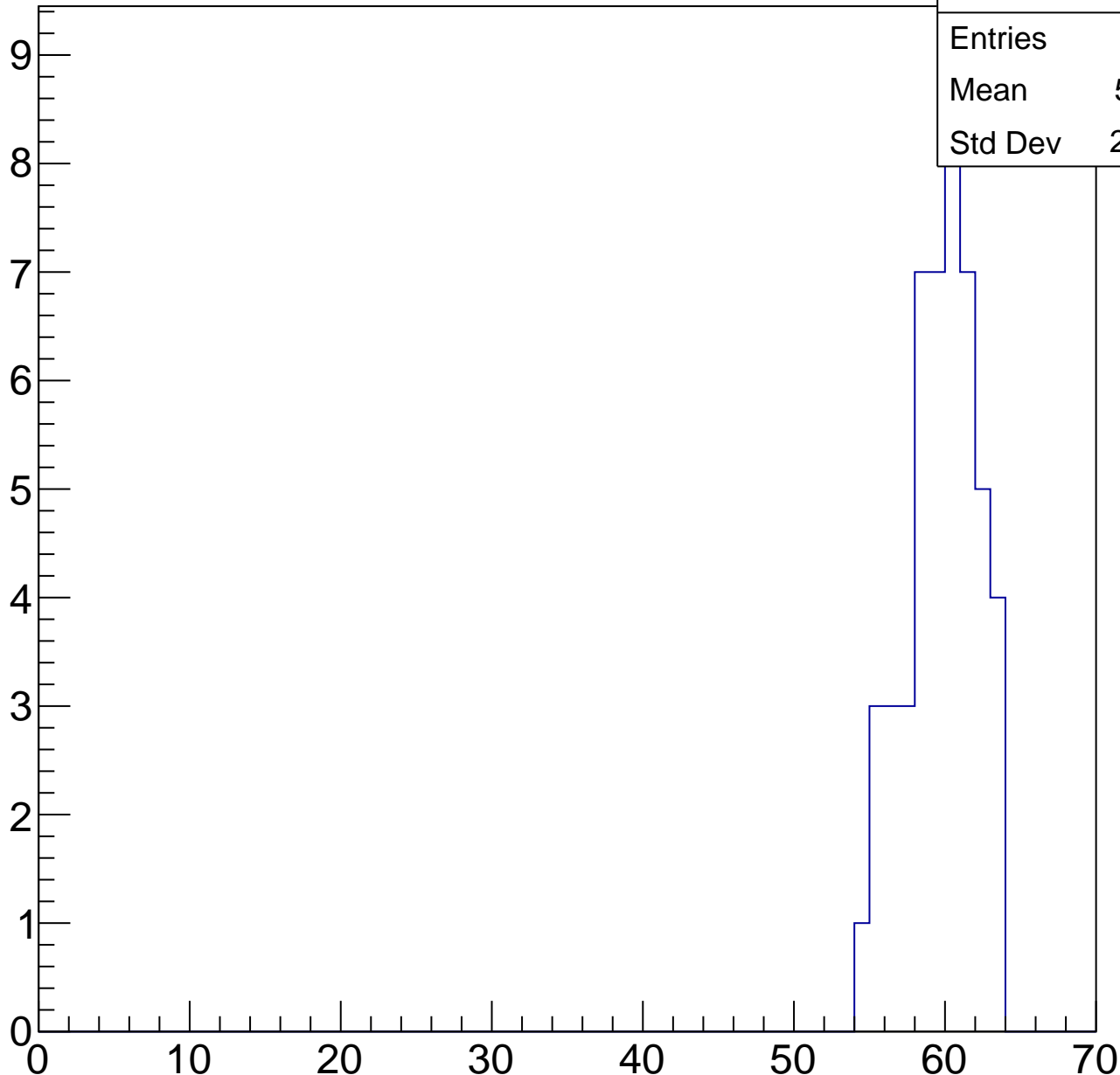
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	49
Mean	59.31
Std Dev	2.305

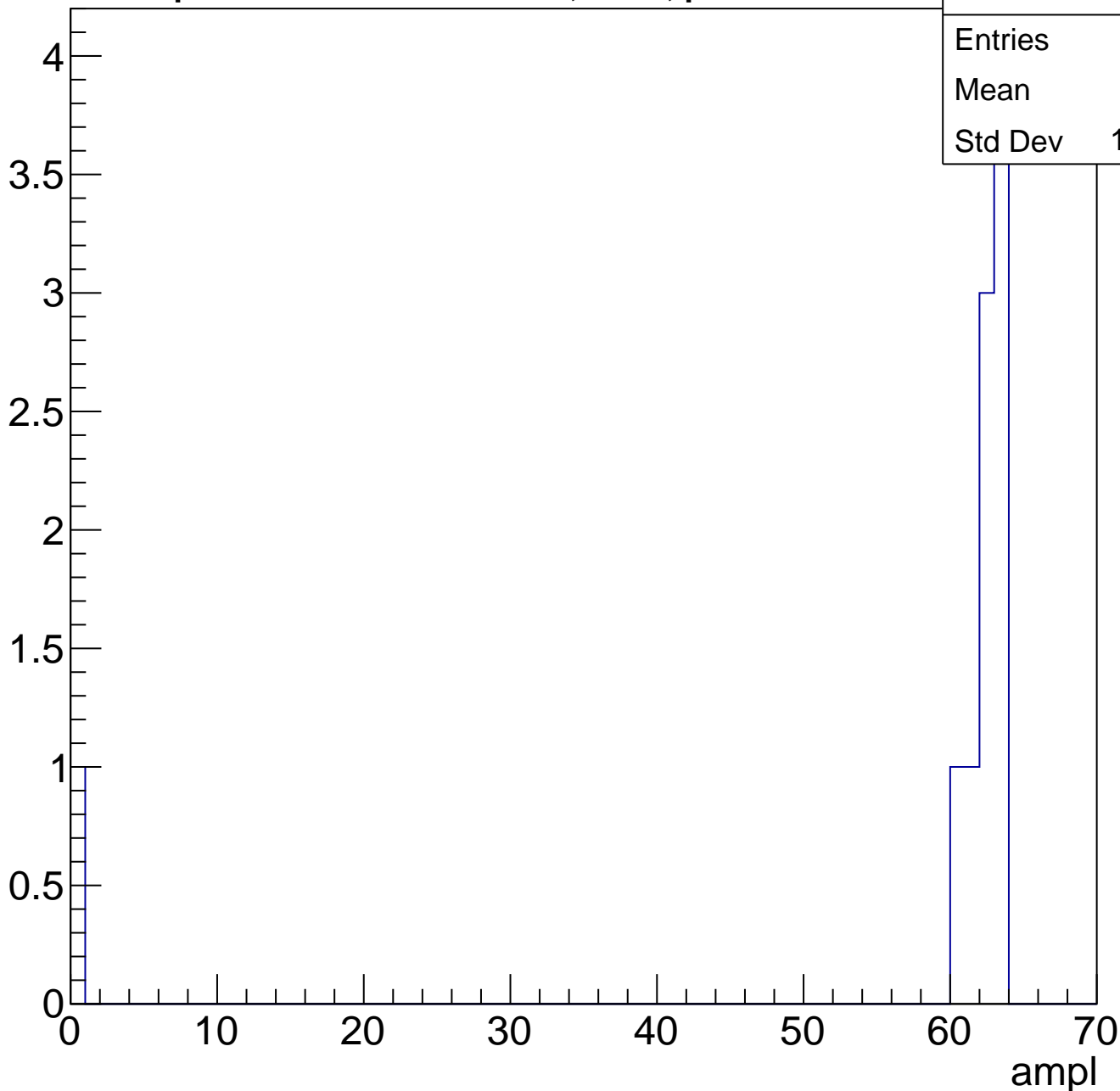
ampl



# B1L100S, U2-ch12, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

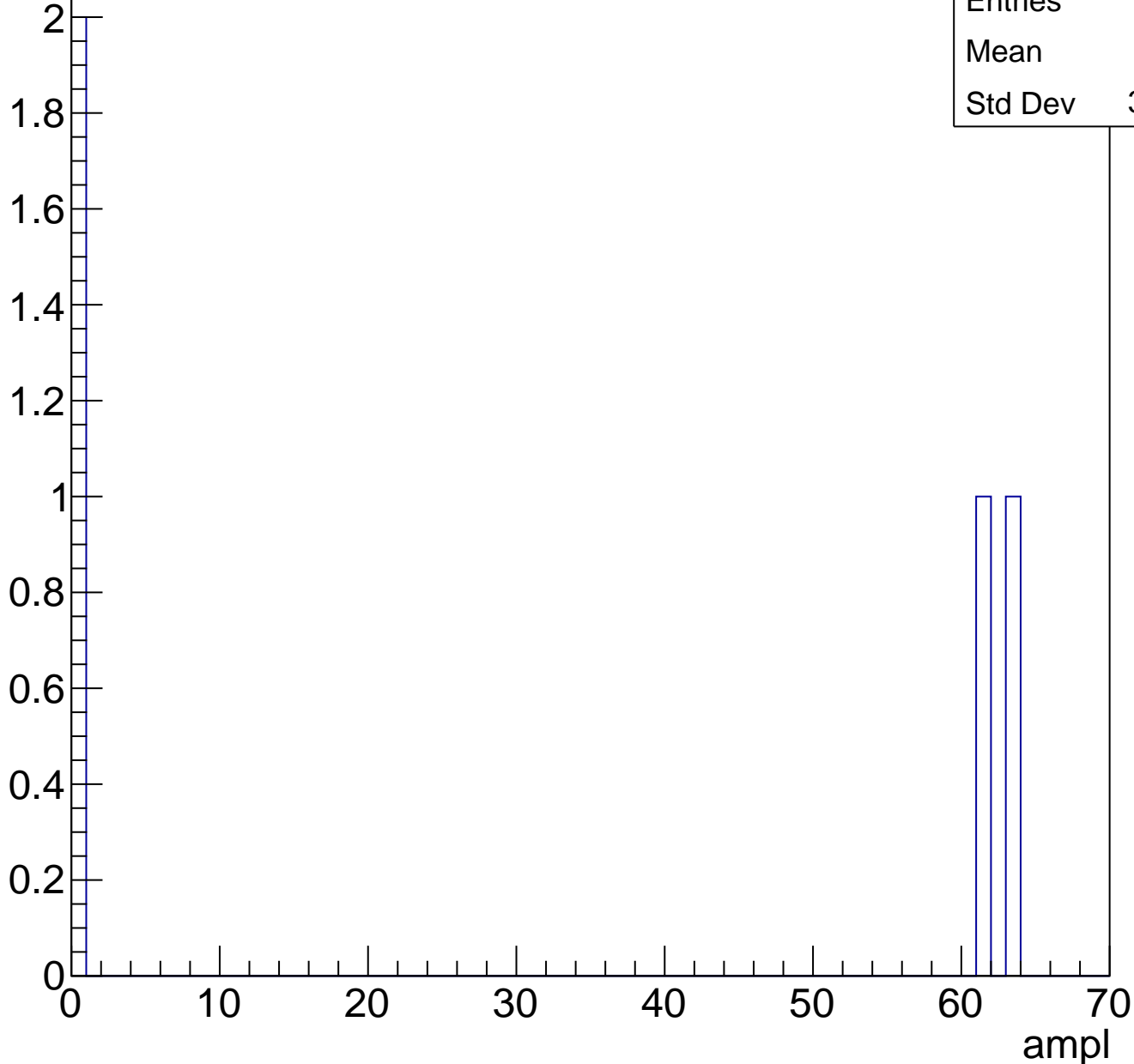




# B1L100S, U2-ch12, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



# B1L100S, U2-ch13, adc0

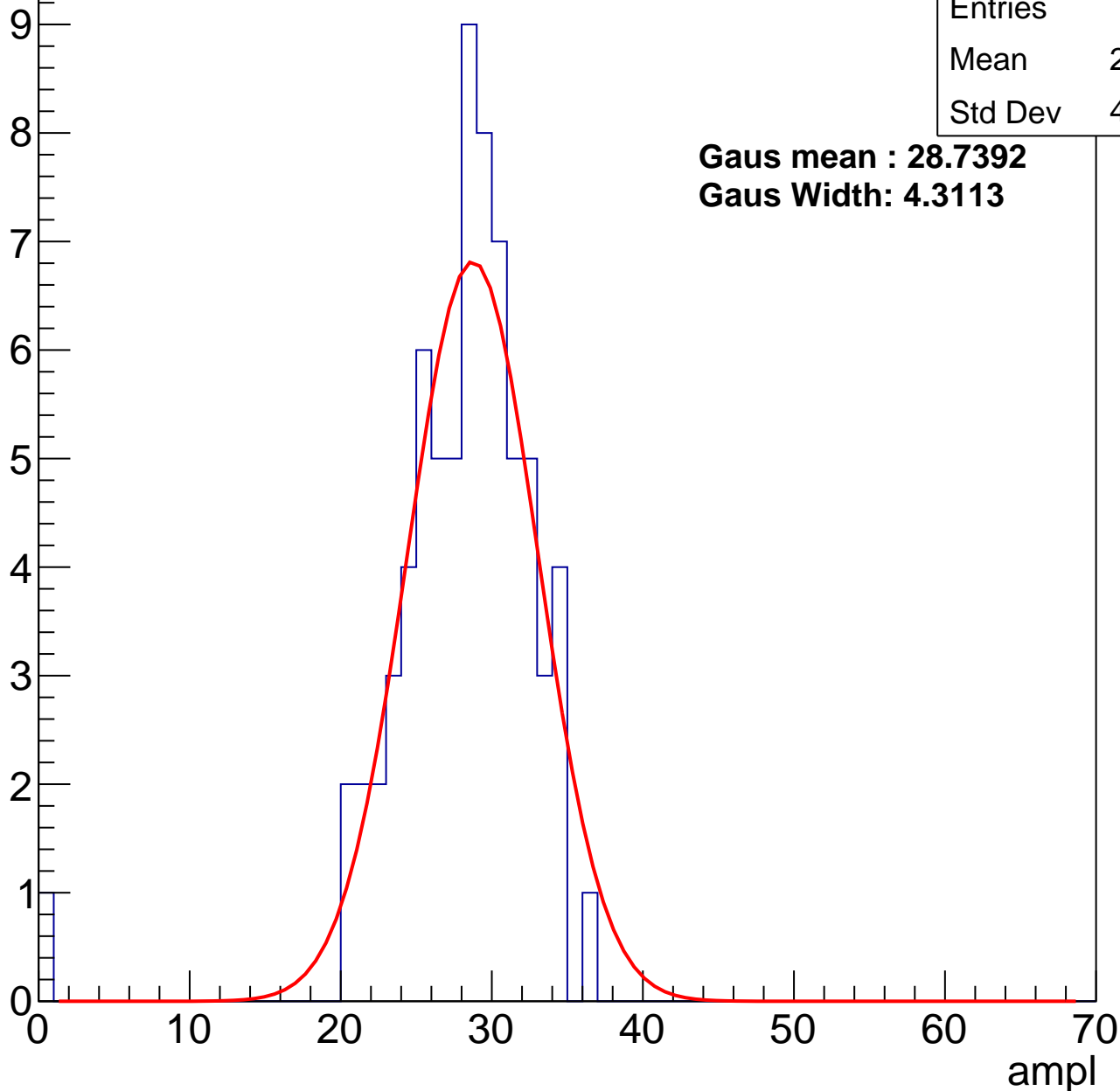
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	72
Mean	27.58
Std Dev	4.904

**Gaus mean : 28.7392**

**Gaus Width: 4.3113**



# B1L100S, U2-ch13, adc1

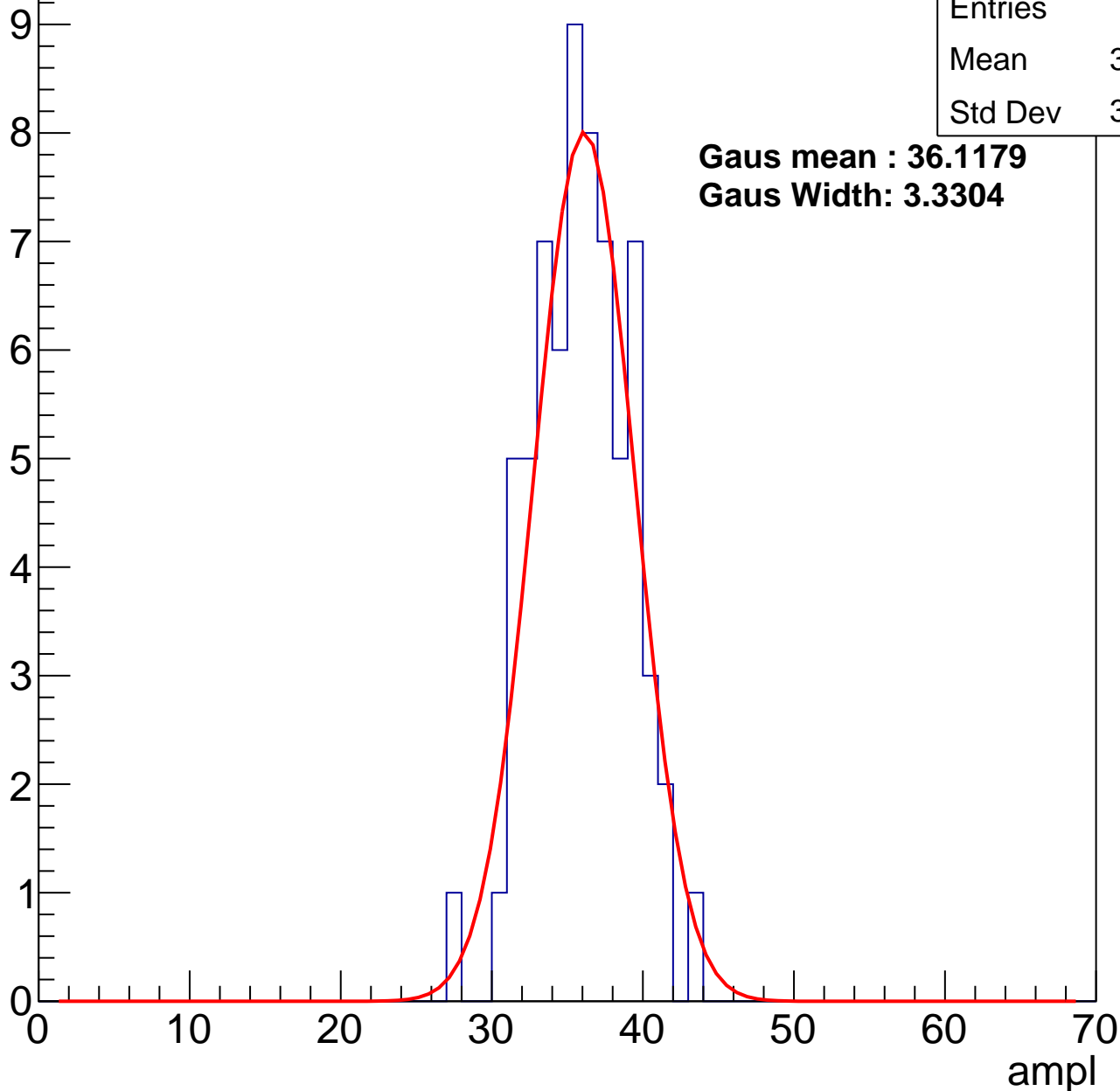
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	67
Mean	35.48
Std Dev	3.083

**Gaus mean : 36.1179**

**Gaus Width: 3.3304**



# B1L100S, U2-ch13, adc2

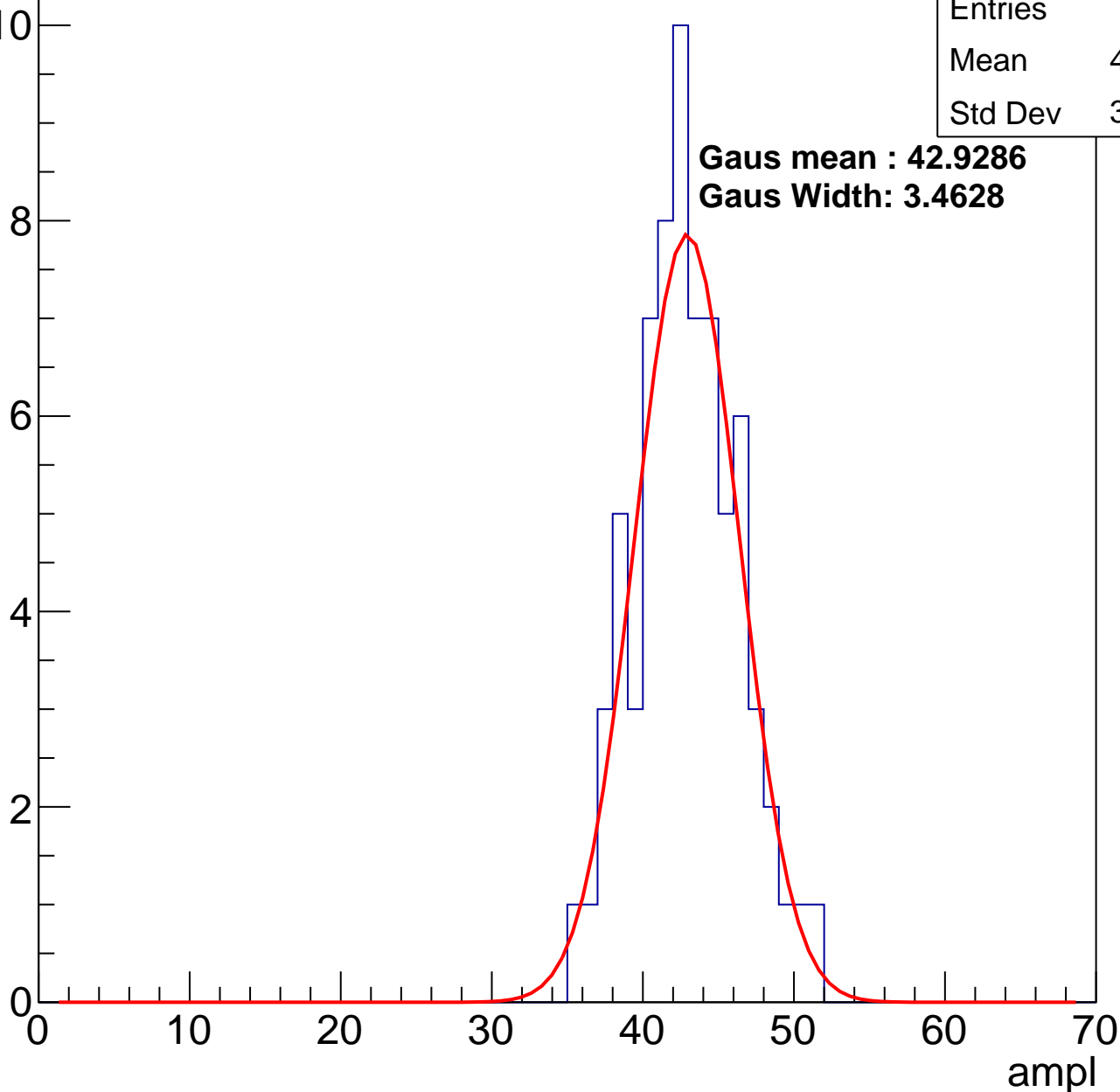
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	71
Mean	42.45
Std Dev	3.368

**Gaus mean : 42.9286**

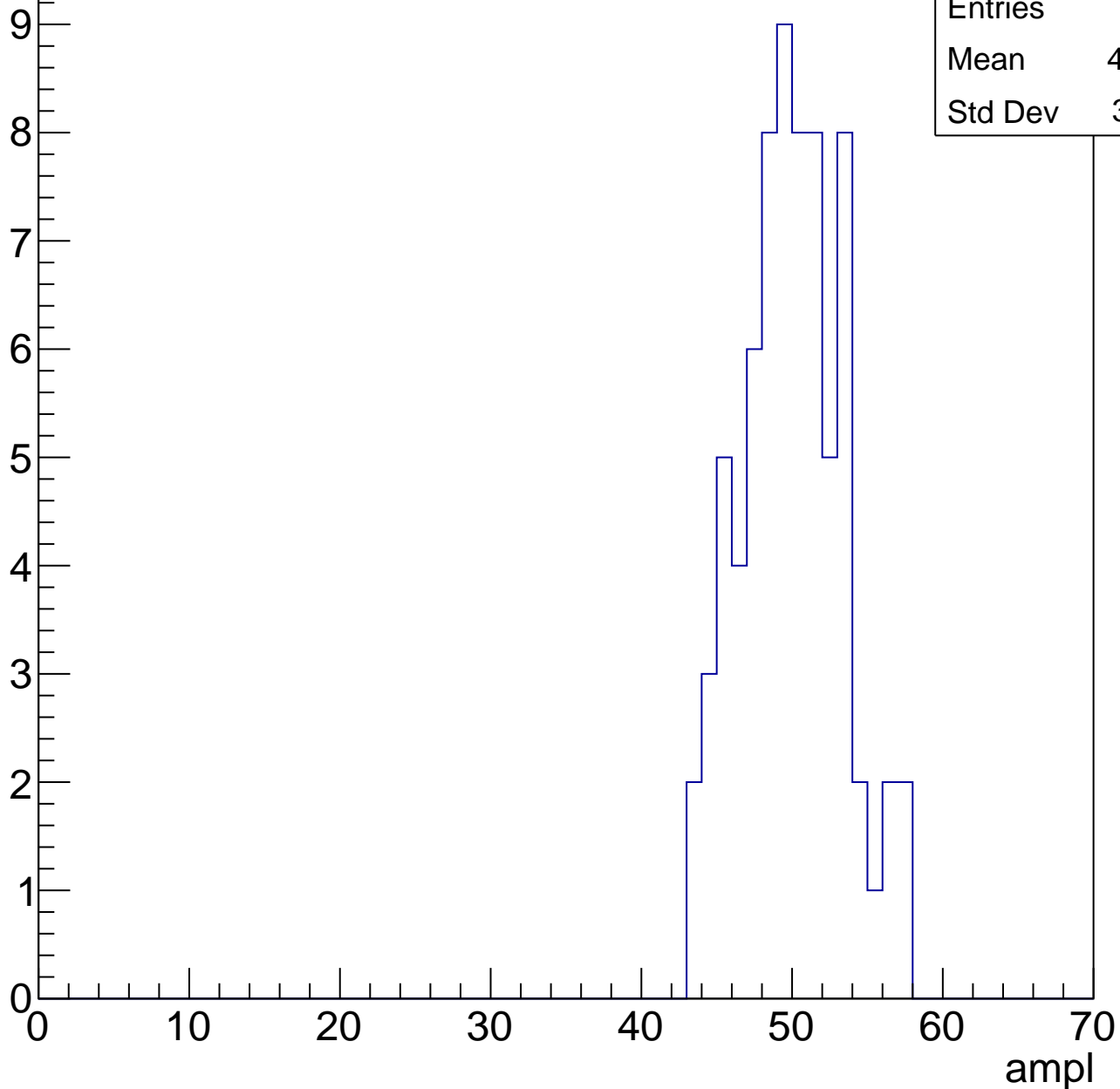
**Gaus Width: 3.4628**



# B1L100S, U2-ch13, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

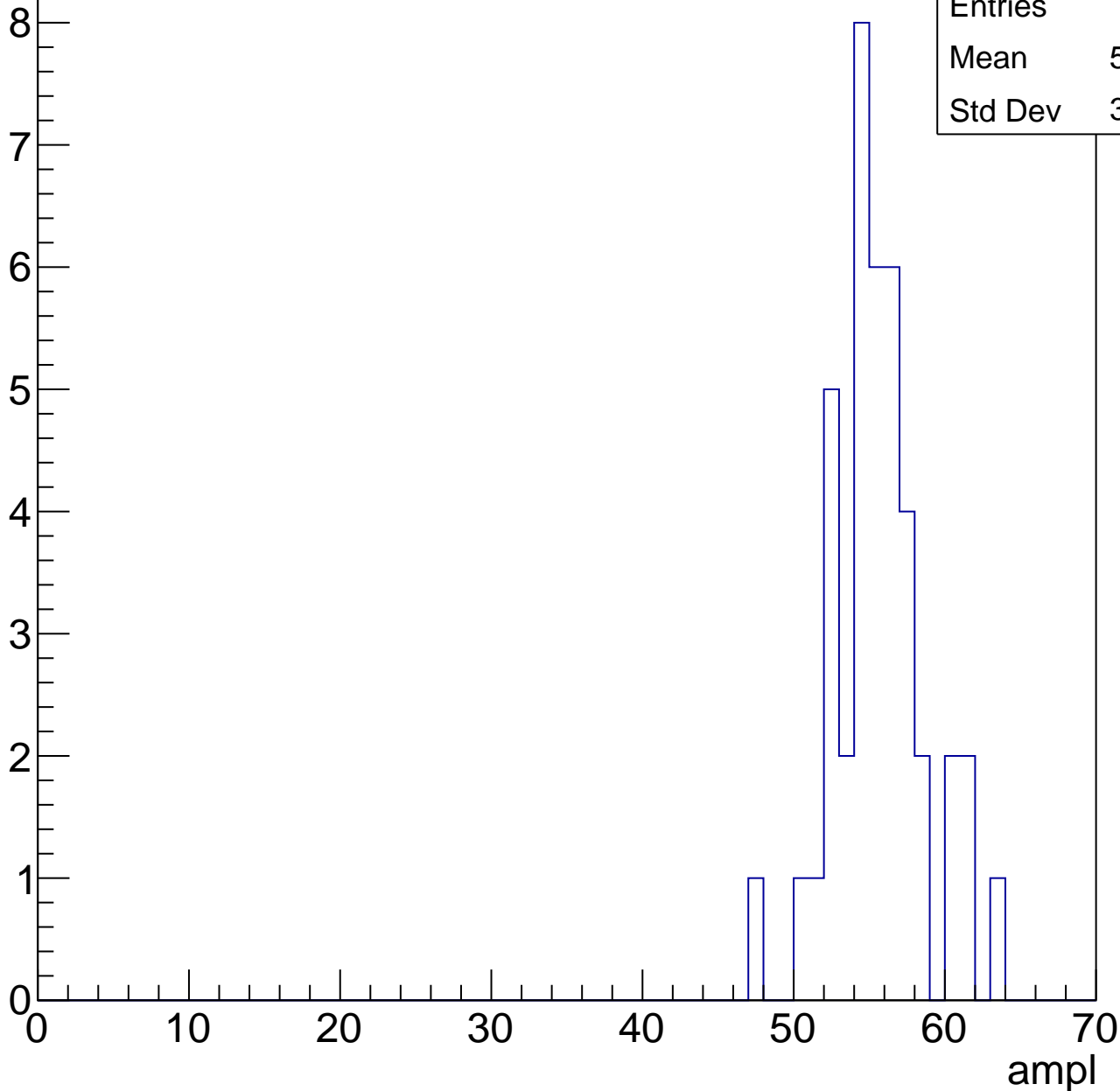


# B1L100S, U2-ch13, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	41
Mean	55.15
Std Dev	3.089



# B1L100S, U2-ch13, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

10

8

6

4

2

0

0

10

20

30

40

50

60

70

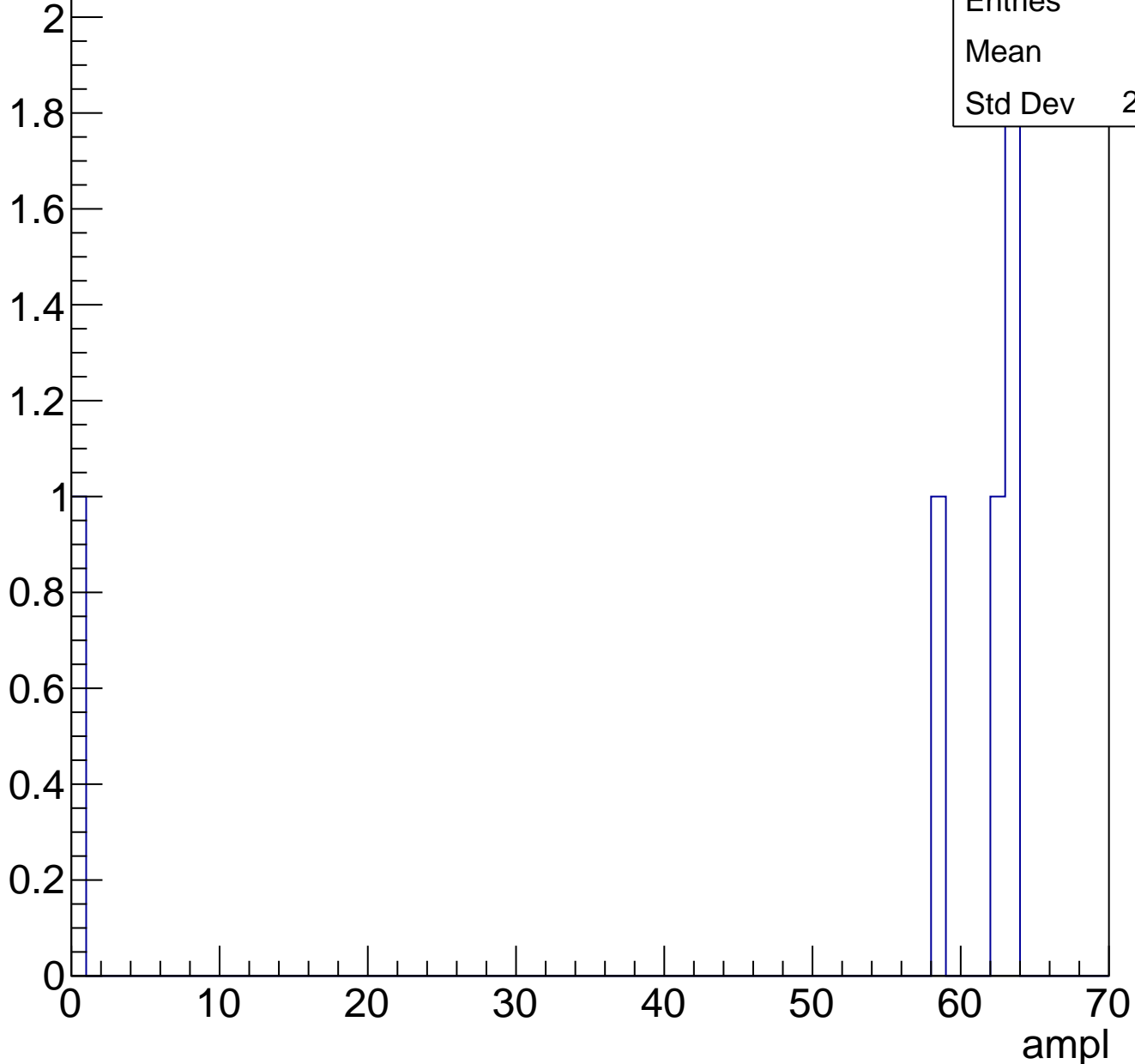
ampl

Entries	58
Mean	59.79
Std Dev	2.219

# B1L100S, U2-ch13, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry





# B1L100S, U2-ch13, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L100S, U2-ch14, adc0

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	69
Mean	28.52
Std Dev	4.811

**Gaus mean : 29.5662**

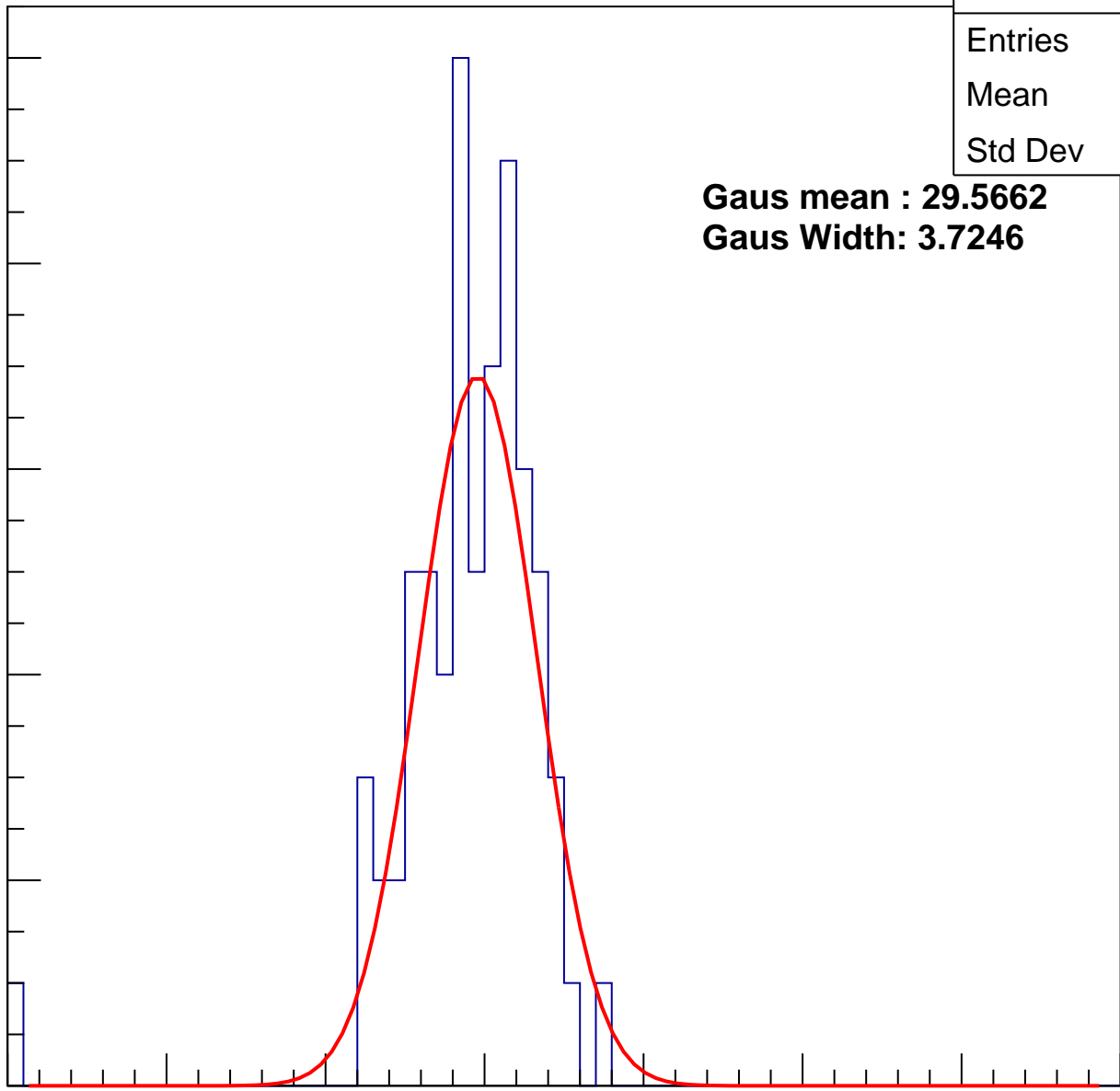
**Gaus Width: 3.7246**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L100S, U2-ch14, adc1

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	79
Mean	35.54
Std Dev	4.087

**Gaus mean : 37.0001**

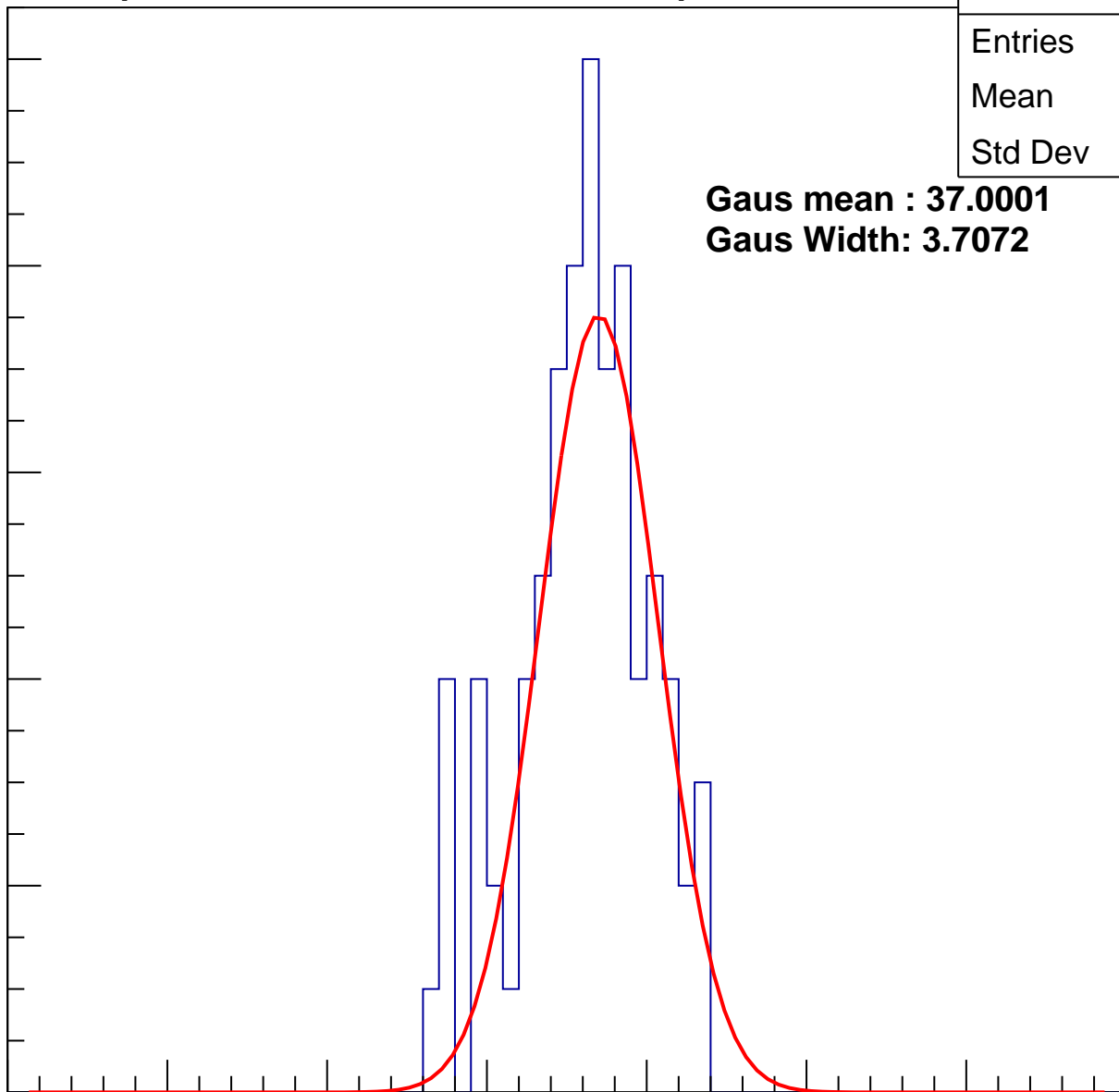
**Gaus Width: 3.7072**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B1L100S, U2-ch14, adc2

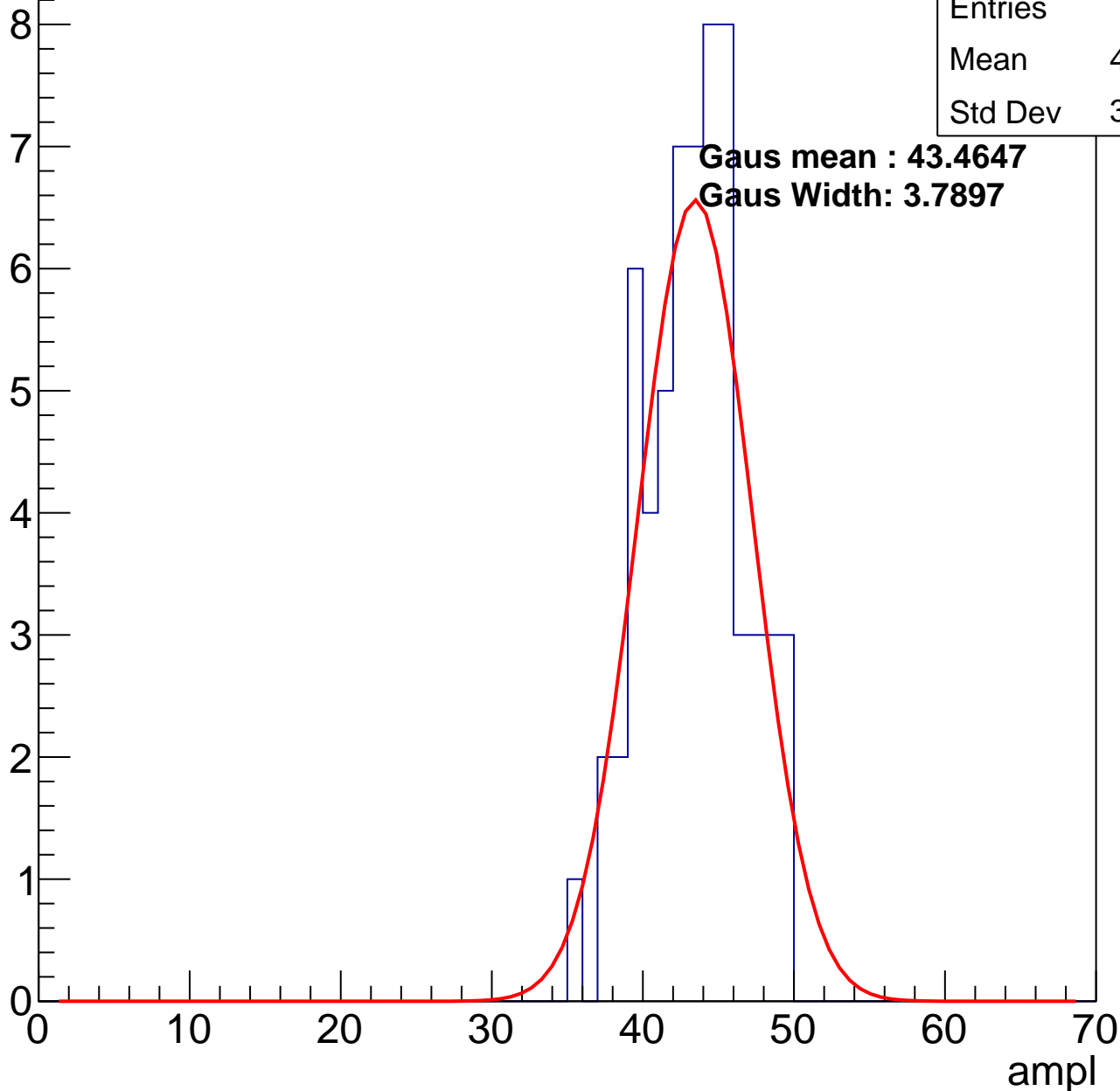
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	62
Mean	42.92
Std Dev	3.219

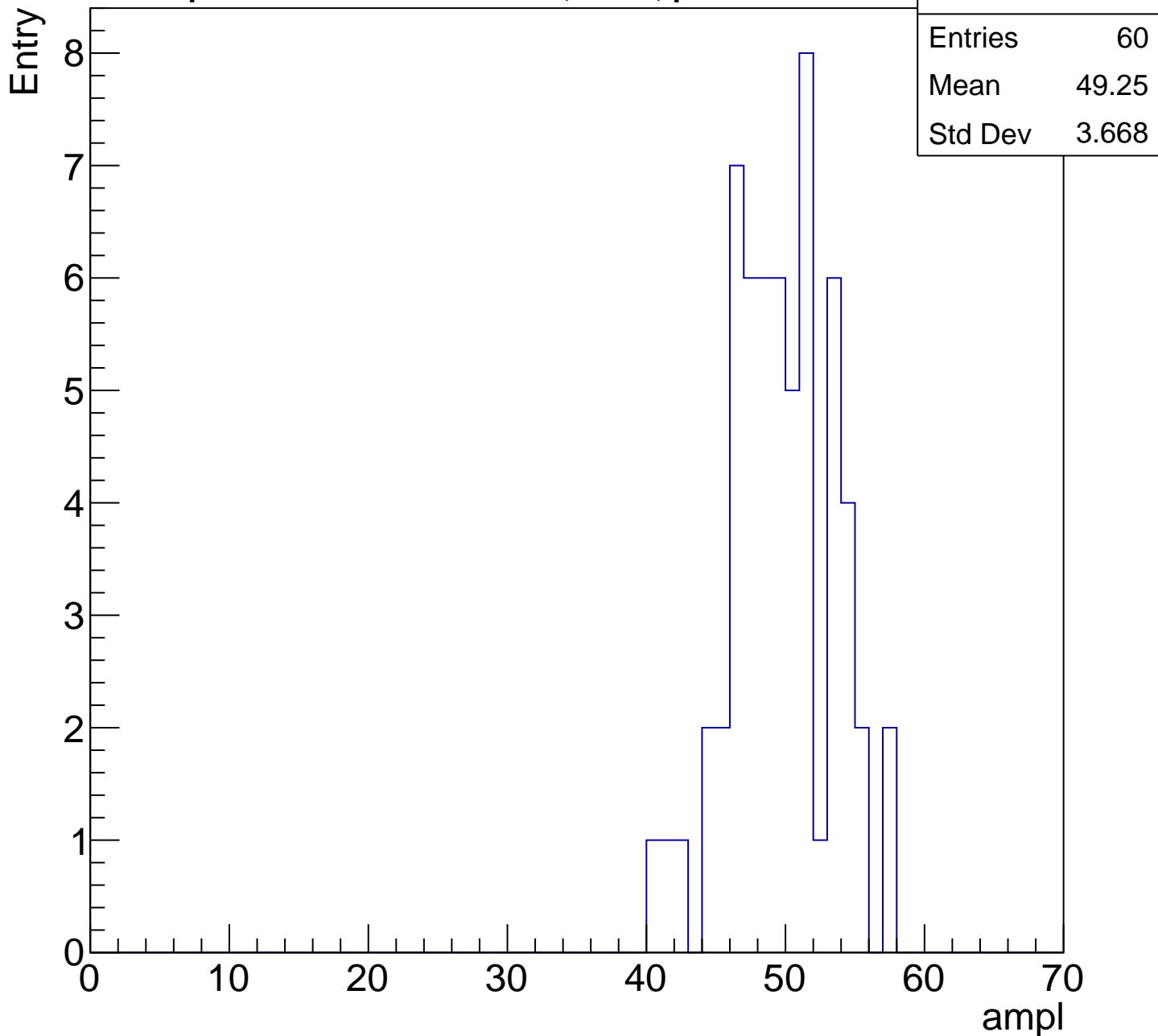
**Gaus mean : 43.4647**

**Gaus Width: 3.7897**



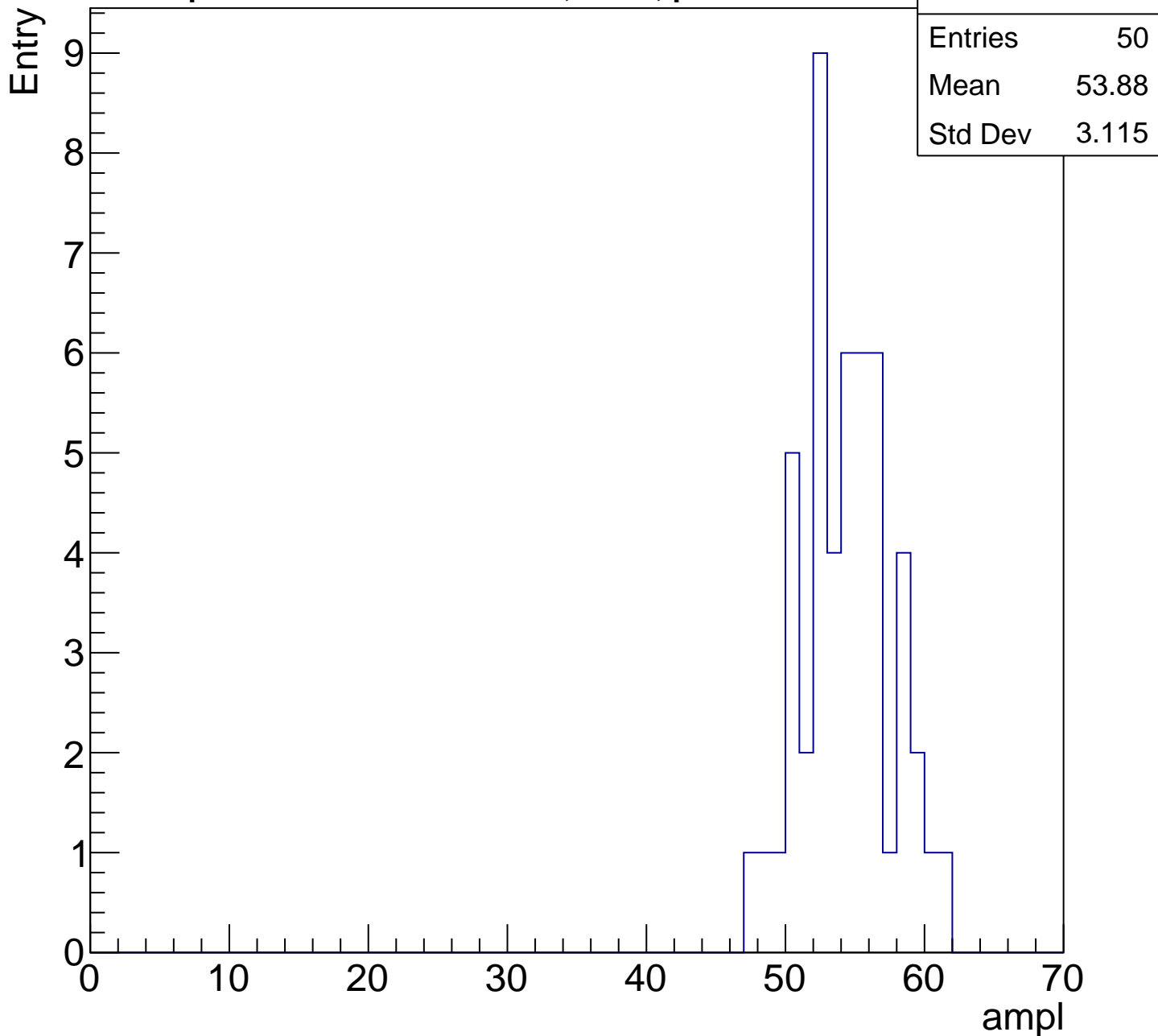
# B1L100S, U2-ch14, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2



# B1L100S, U2-ch14, adc4

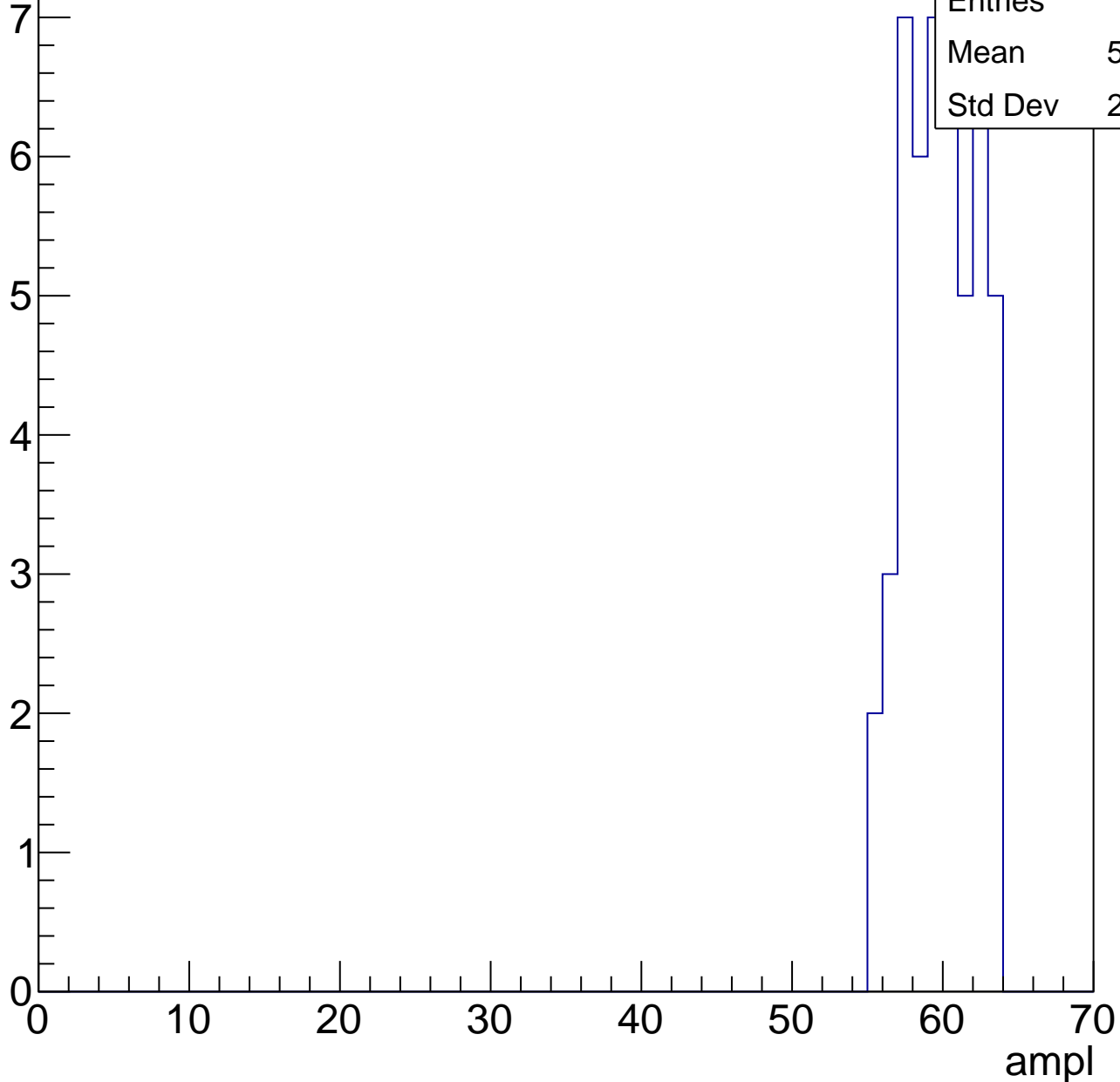
calib\_packv5\_042523\_0143.root, FC#4, port A2



# B1L100S, U2-ch14, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

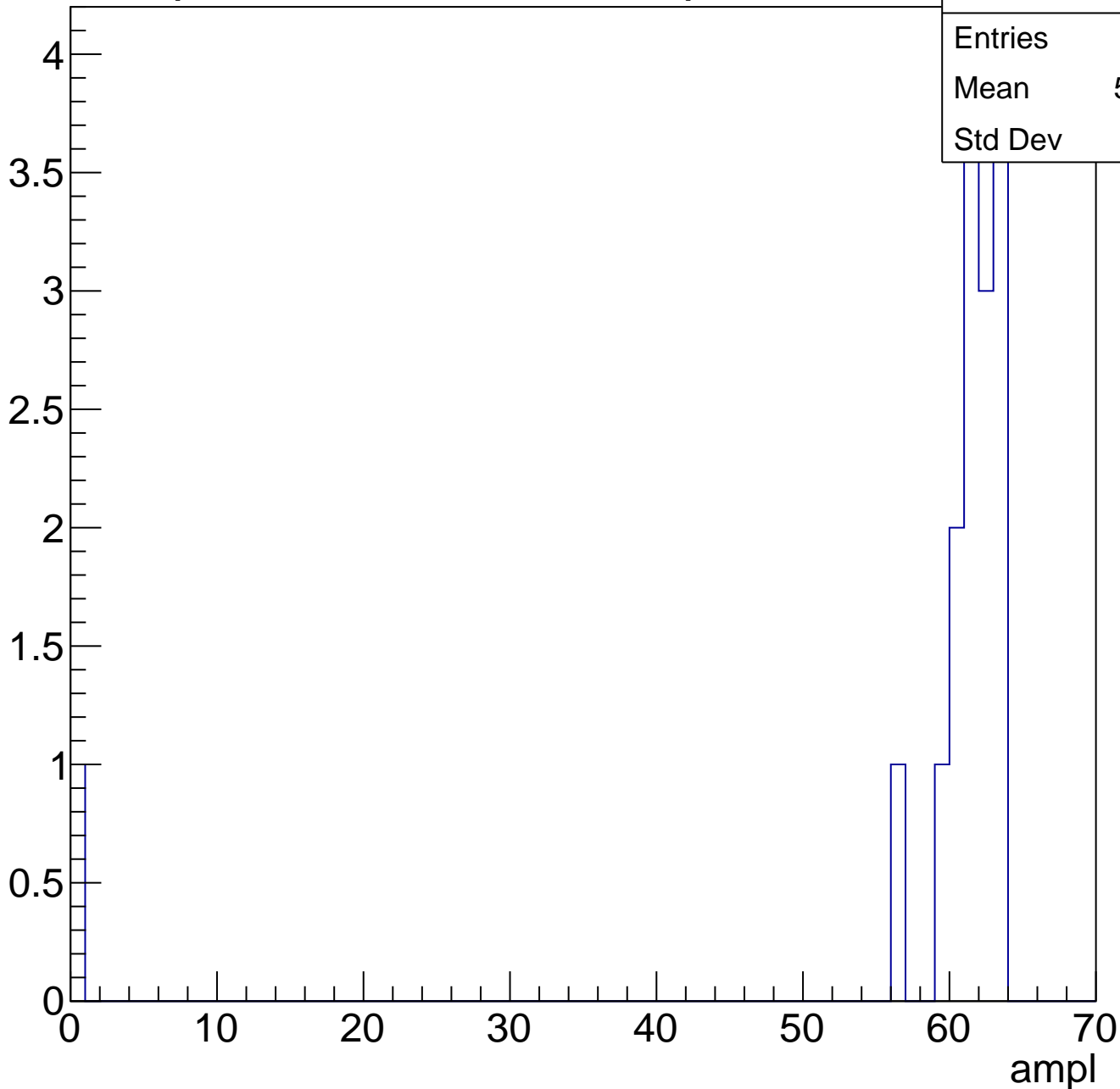


Entries	49
Mean	59.43
Std Dev	2.277

# B1L100S, U2-ch14, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

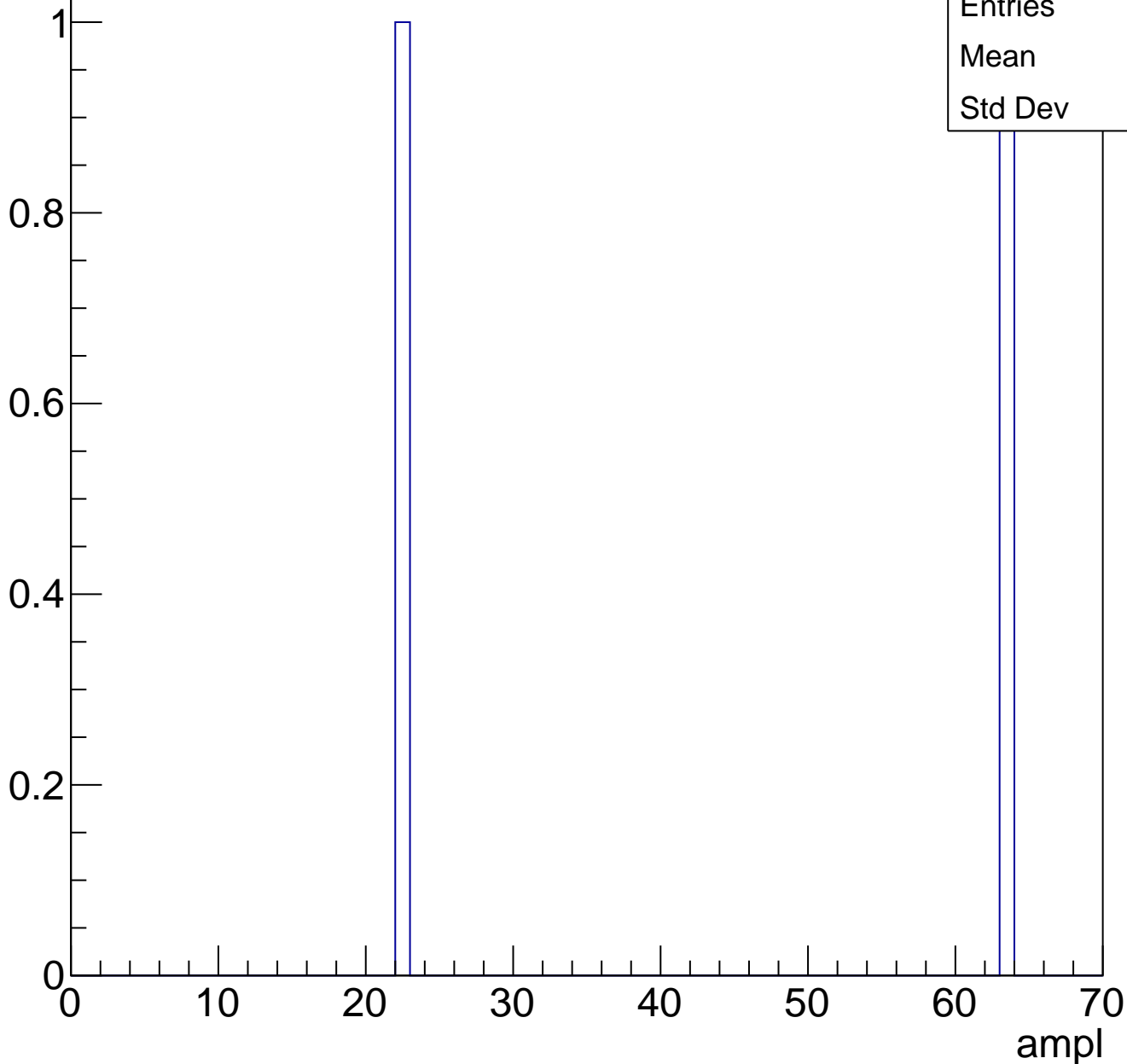




# B1L100S, U2-ch14, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



# B1L100S, U2-ch15, adc0

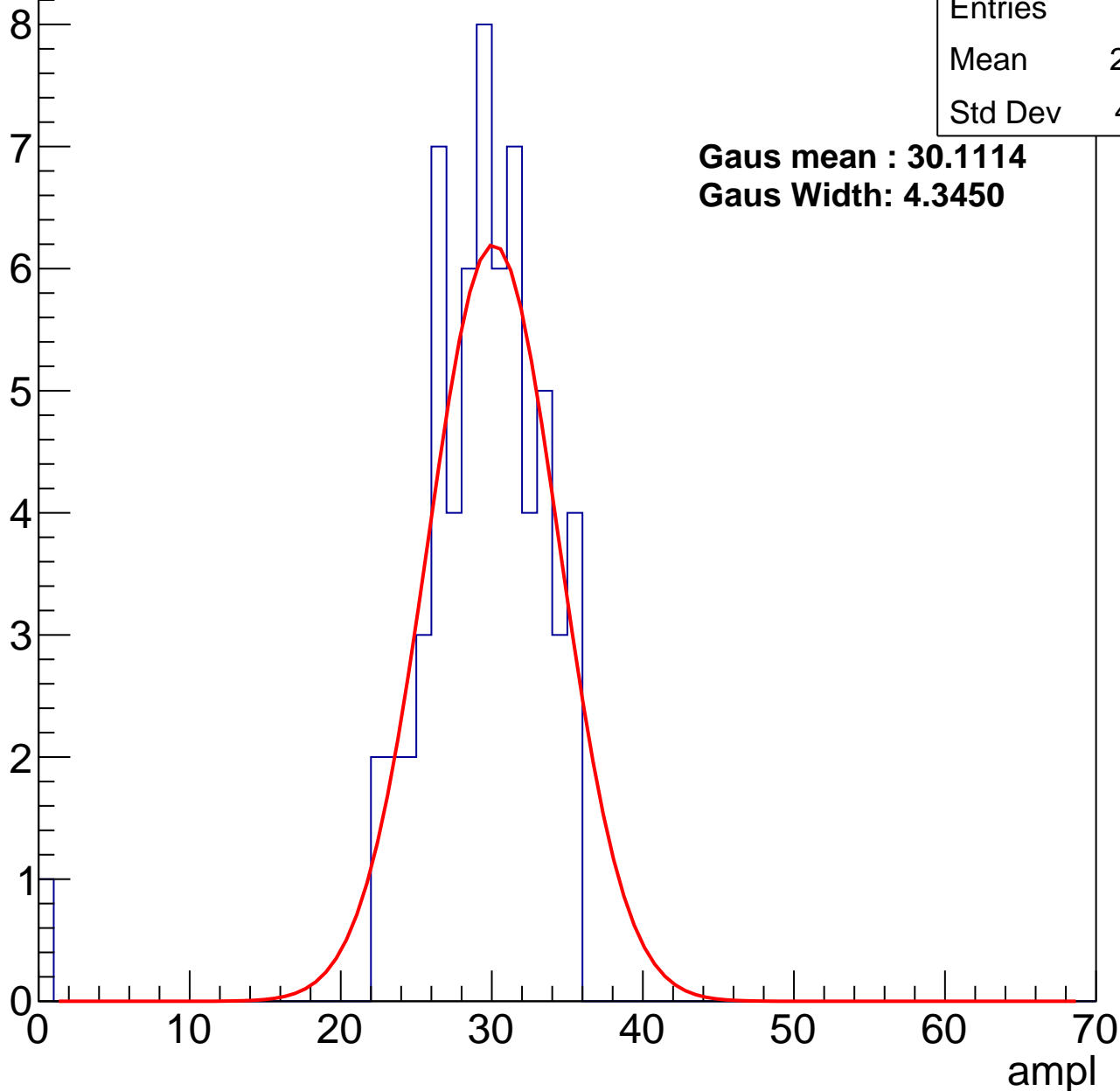
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	64
Mean	28.67
Std Dev	4.931

**Gaus mean : 30.1114**

**Gaus Width: 4.3450**



# B1L100S, U2-ch15, adc1

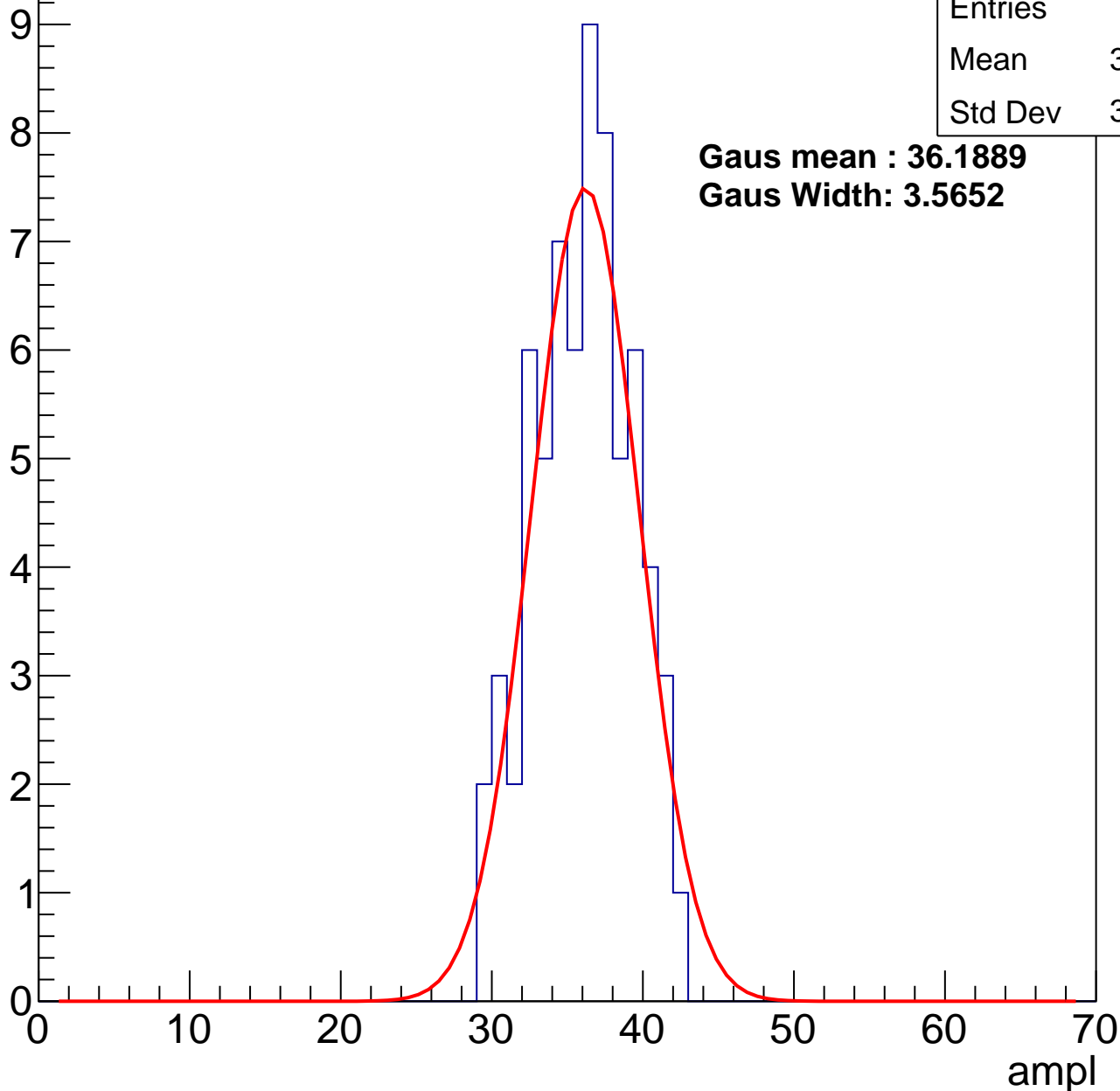
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	67
Mean	35.58
Std Dev	3.177

**Gaus mean : 36.1889**

**Gaus Width: 3.5652**



# B1L100S, U2-ch15, adc2

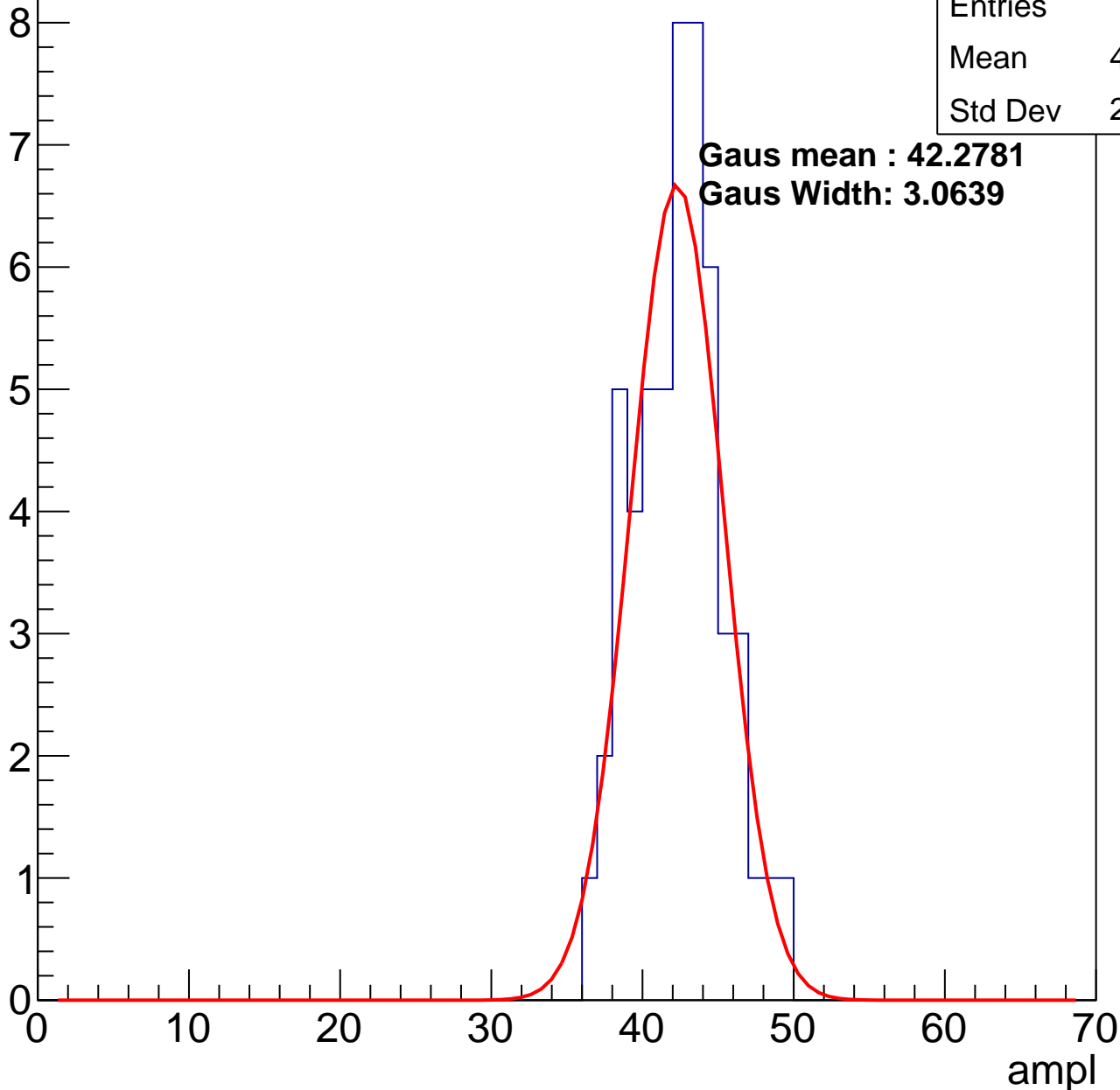
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	53
Mean	41.92
Std Dev	2.893

**Gaus mean : 42.2781**

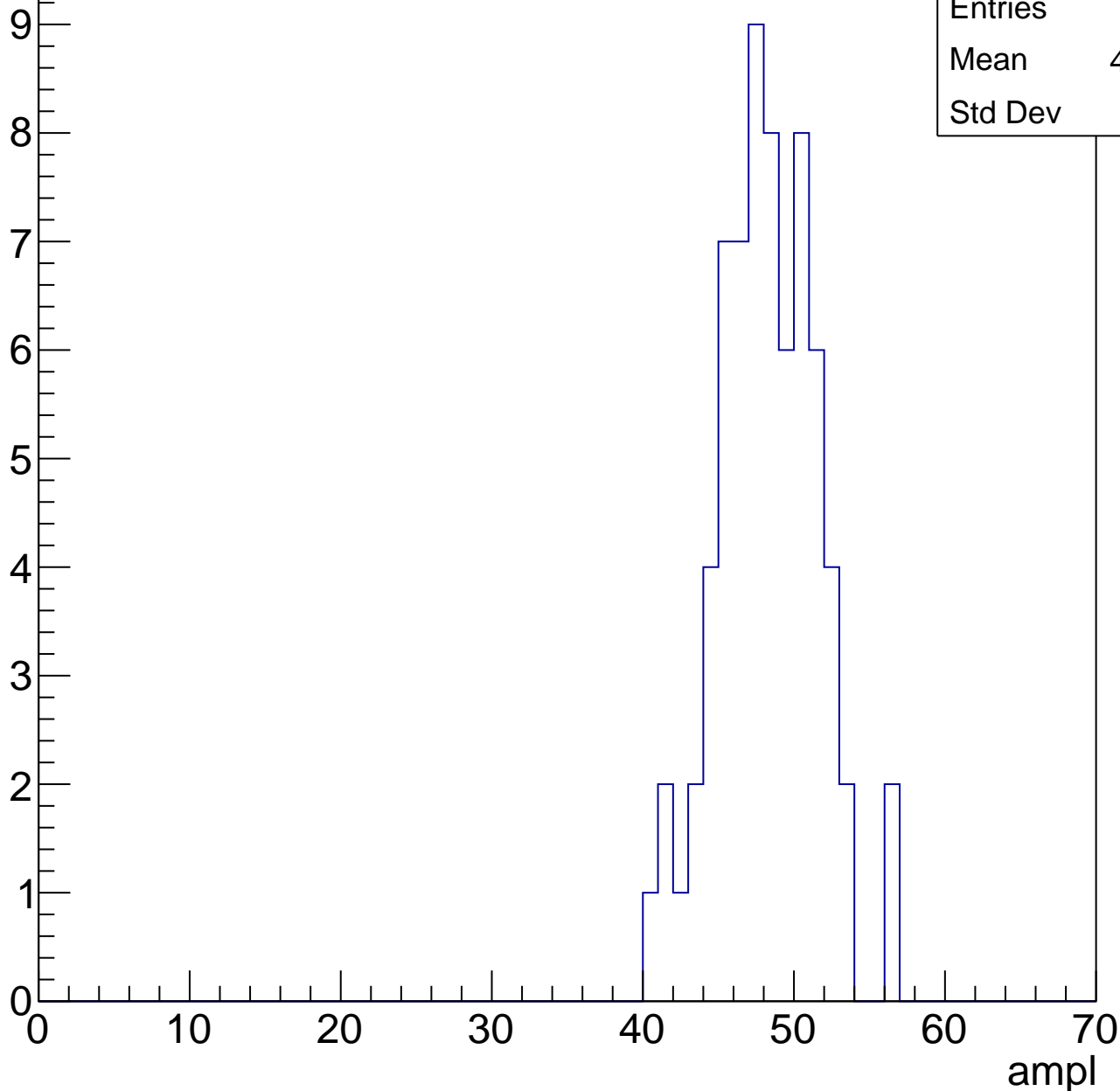
**Gaus Width: 3.0639**



# B1L100S, U2-ch15, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

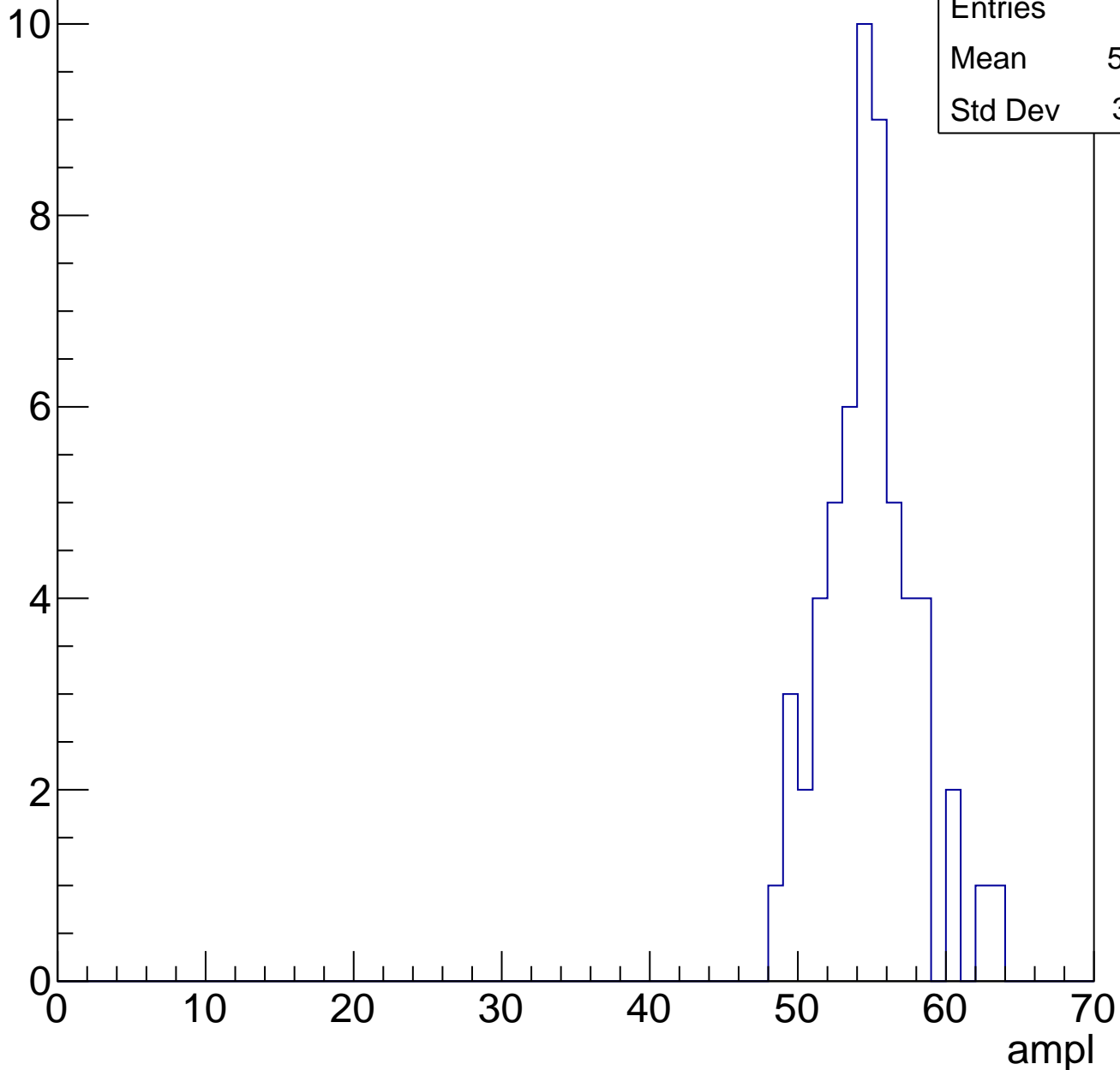


# B1L100S, U2-ch15, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	57
Mean	54.33
Std Dev	3.091

Entry



# B1L100S, U2-ch15, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

10

Entries 54

Mean 59.22

Std Dev 2.565

8

6

4

2

0

0

10

20

30

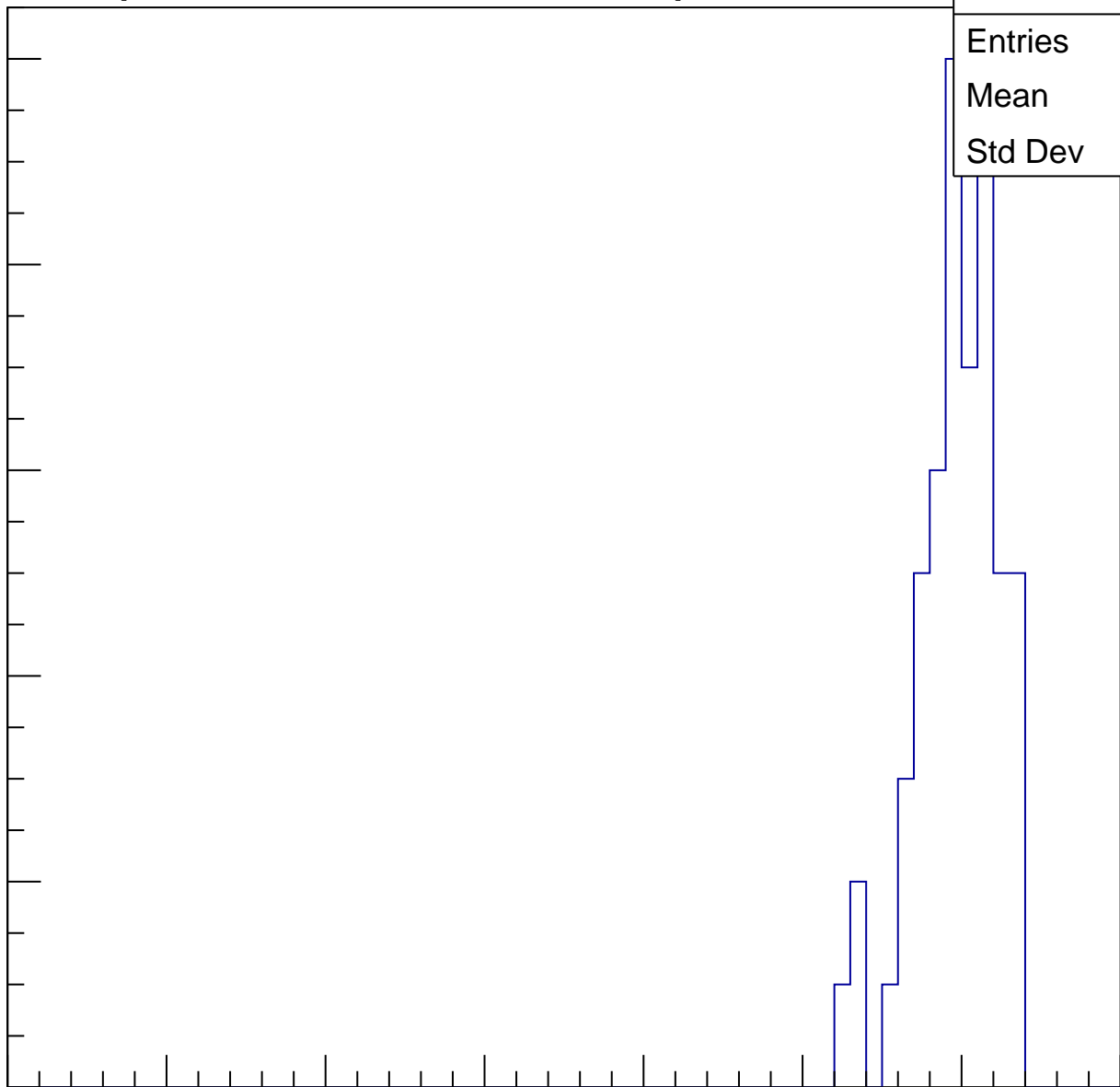
40

50

60

70

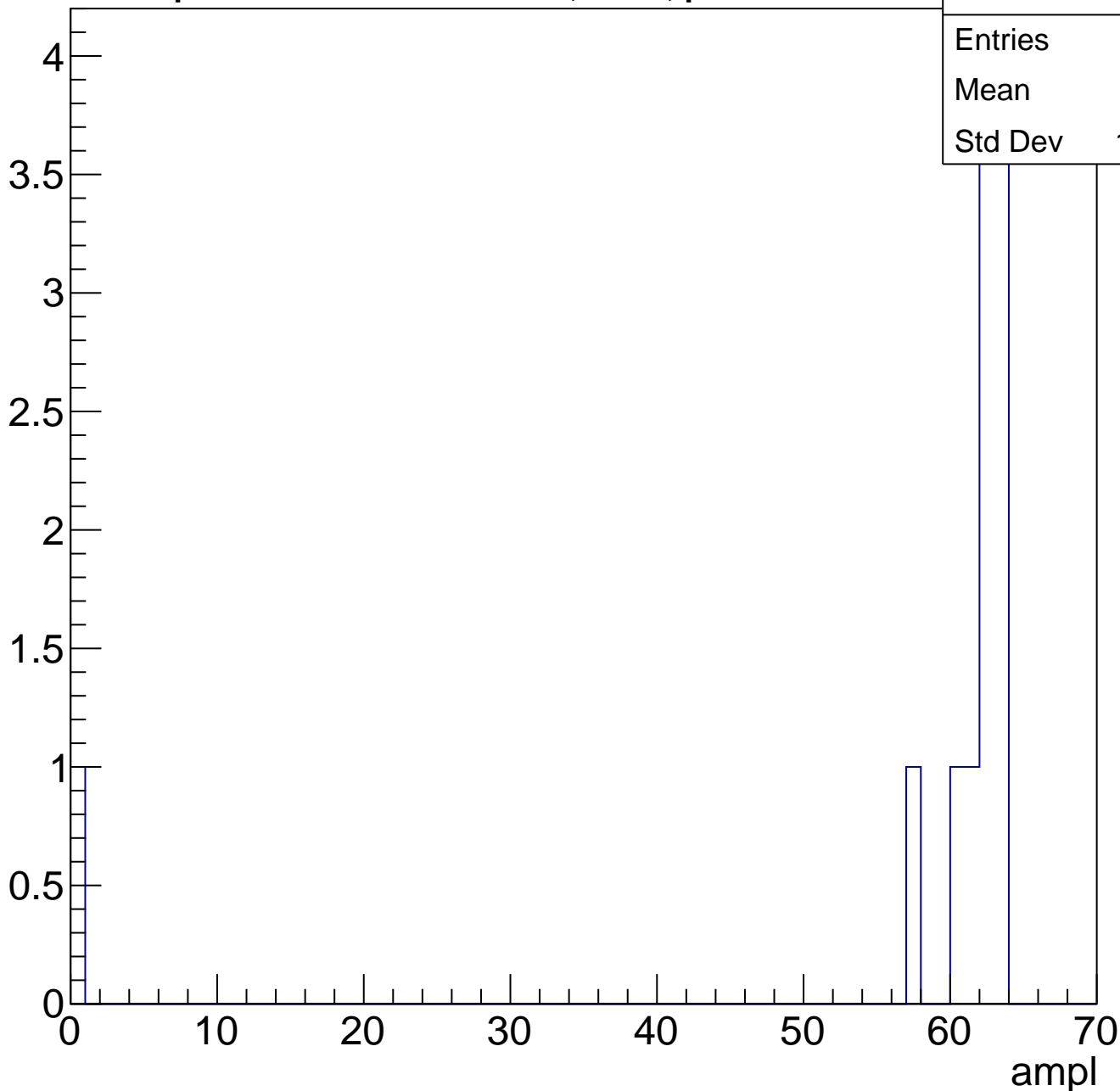
ampl



# B1L100S, U2-ch15, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry





# B1L100S, U2-ch15, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L100S, U2-ch16, adc0

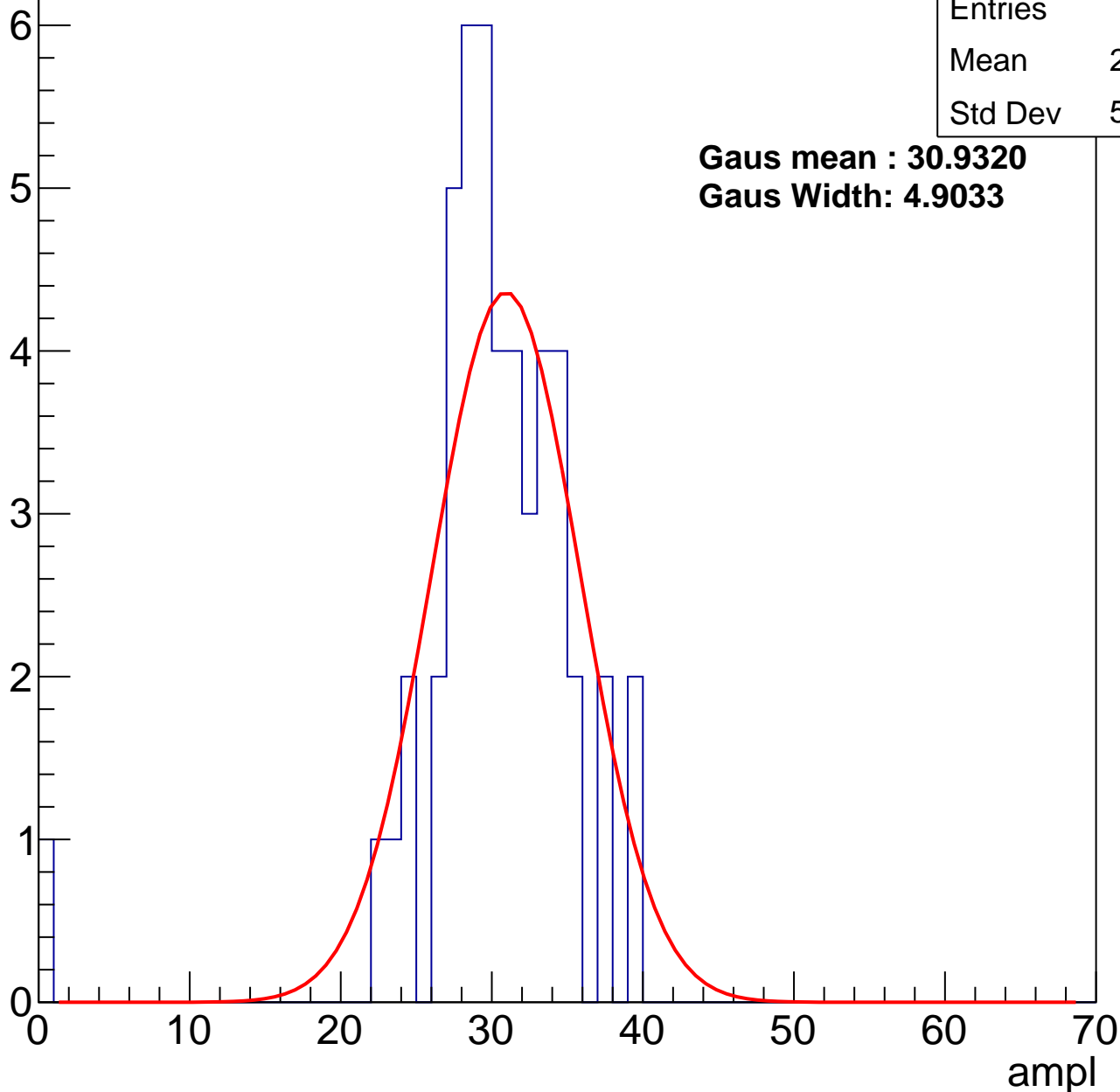
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	49
Mean	29.63
Std Dev	5.735

**Gaus mean : 30.9320**

**Gaus Width: 4.9033**



# B1L100S, U2-ch16, adc1

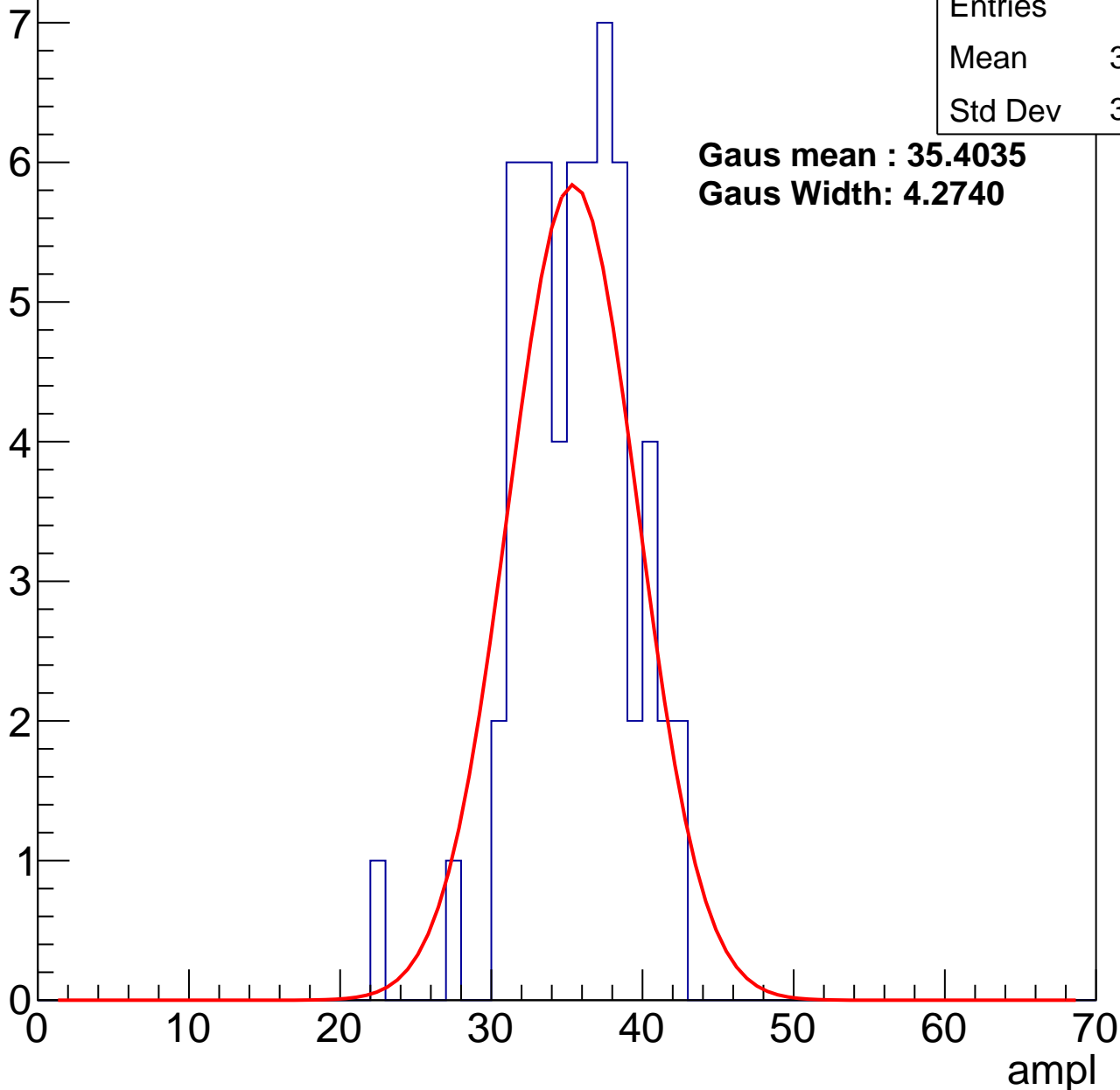
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	61
Mean	35.05
Std Dev	3.735

**Gaus mean : 35.4035**

**Gaus Width: 4.2740**



# B1L100S, U2-ch16, adc2

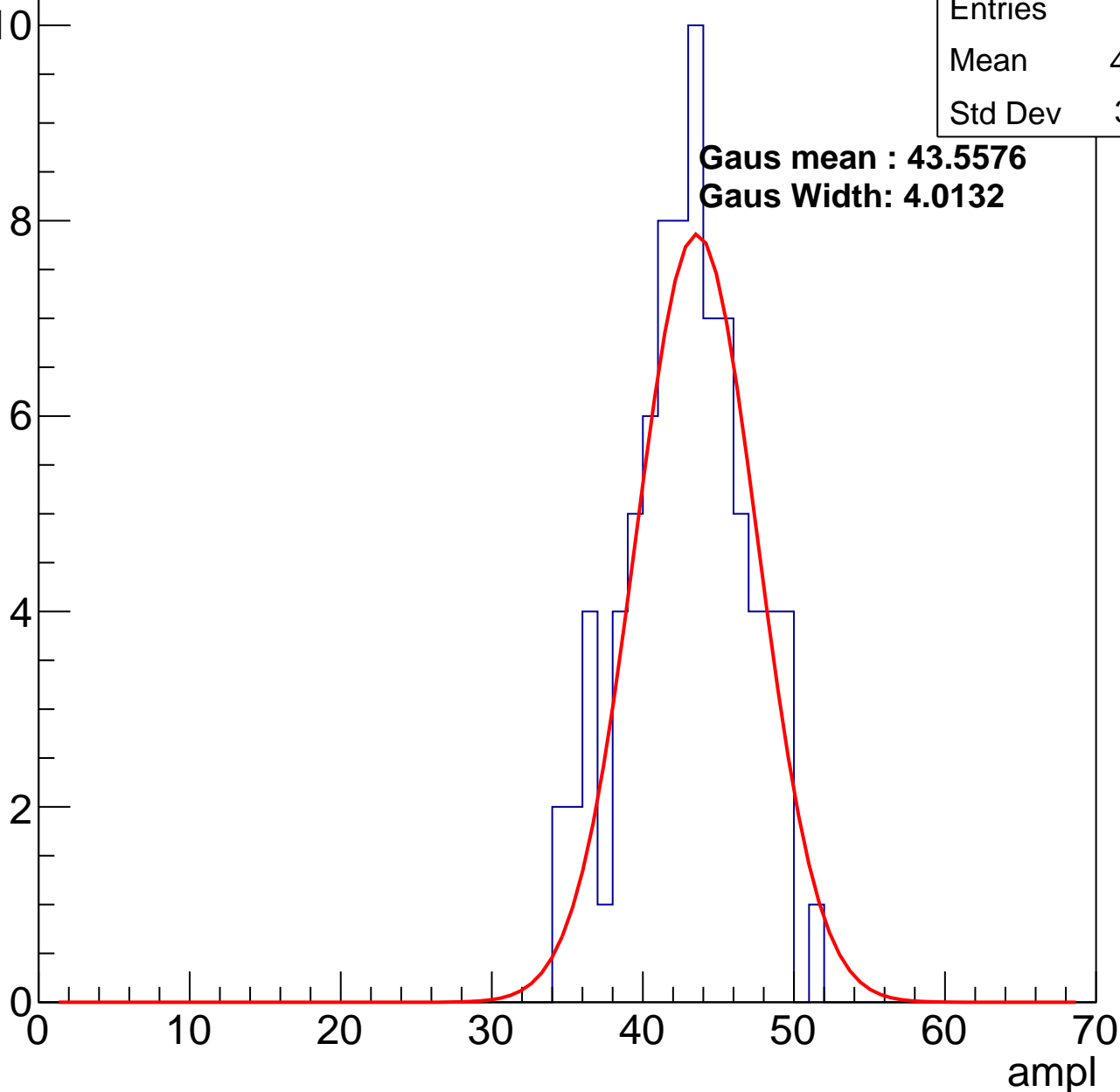
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	82
Mean	42.44
Std Dev	3.861

**Gaus mean : 43.5576**

**Gaus Width: 4.0132**

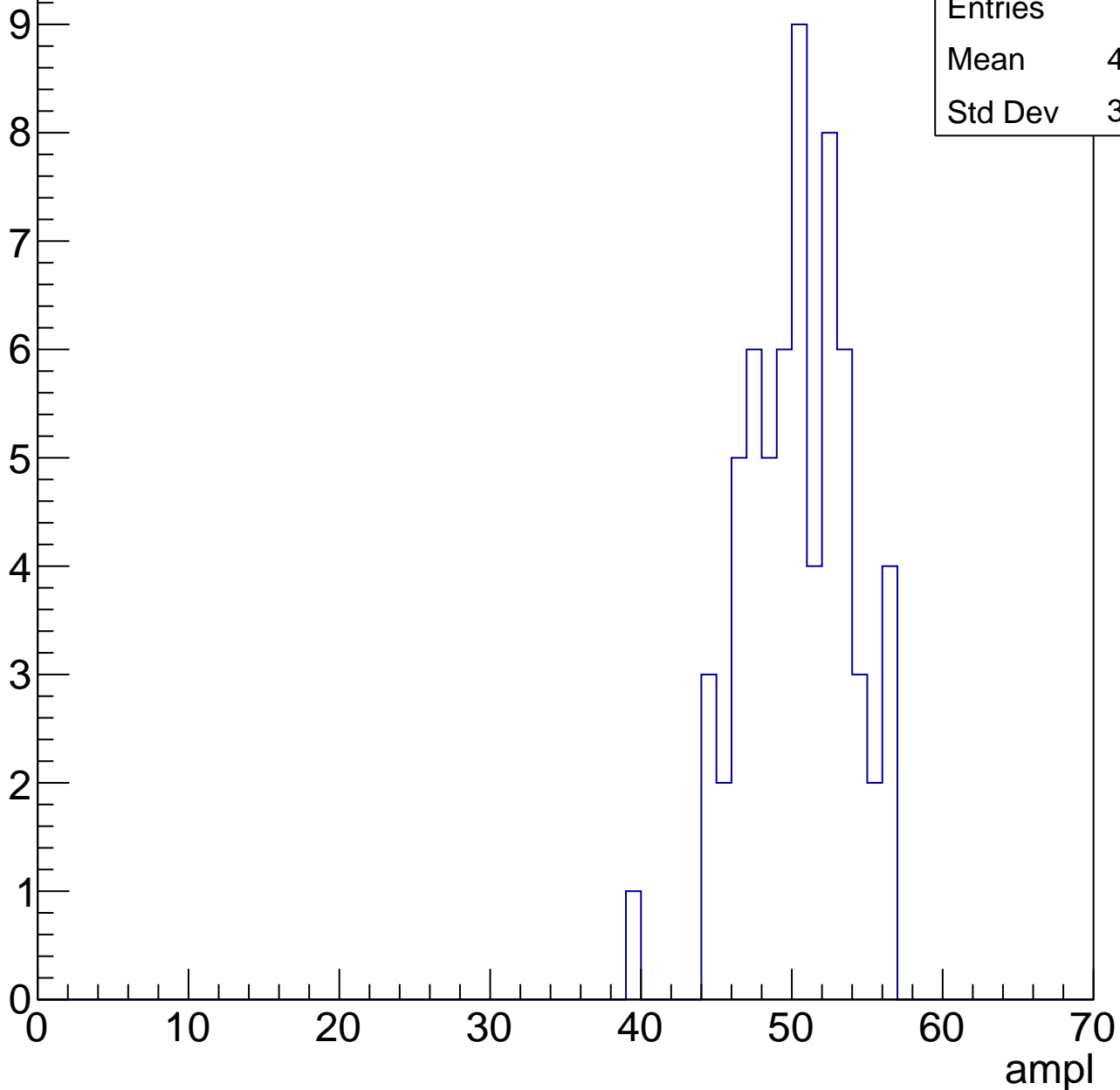


# B1L100S, U2-ch16, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

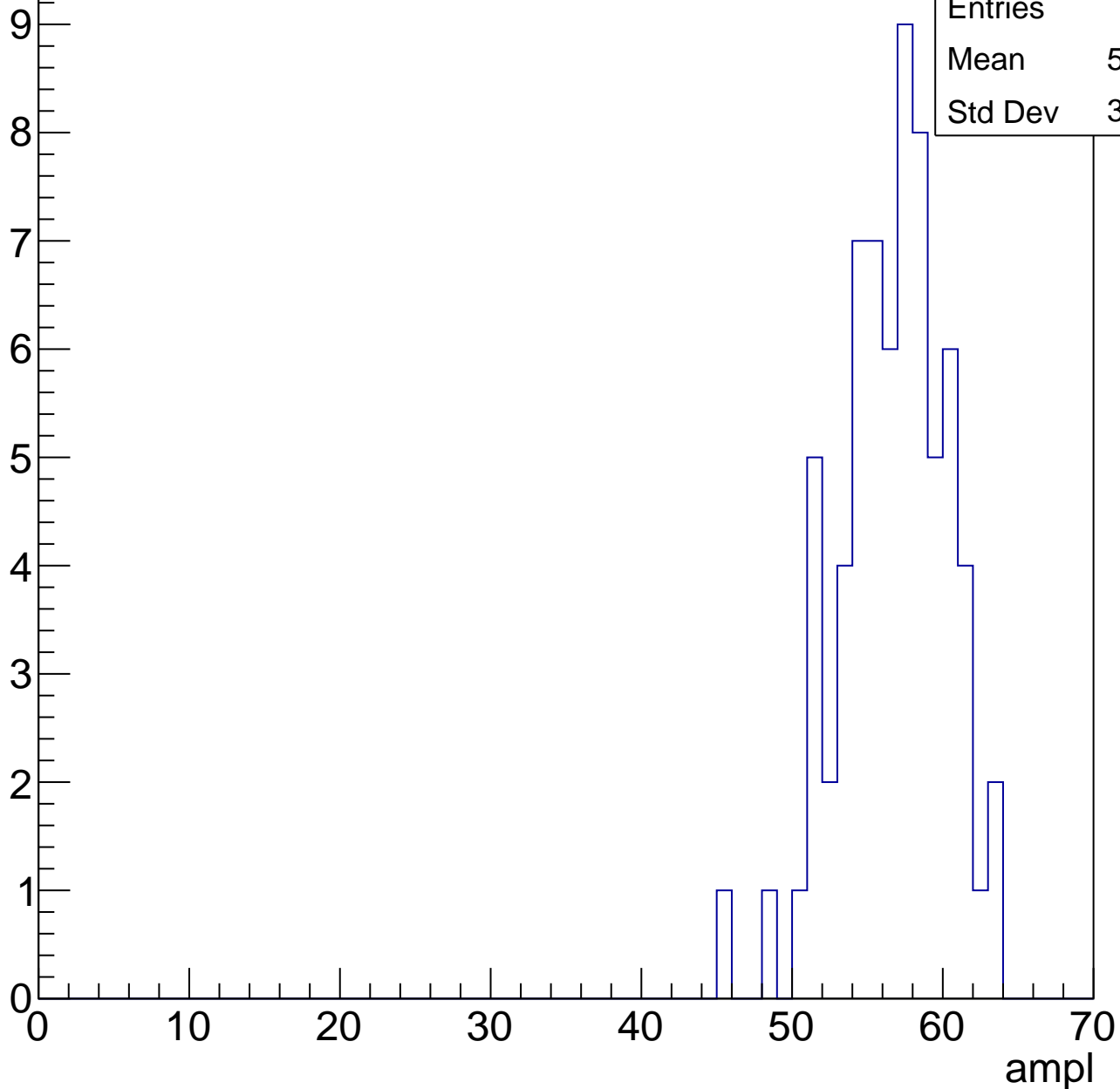
Entries	64
Mean	49.86
Std Dev	3.468



# B1L100S, U2-ch16, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



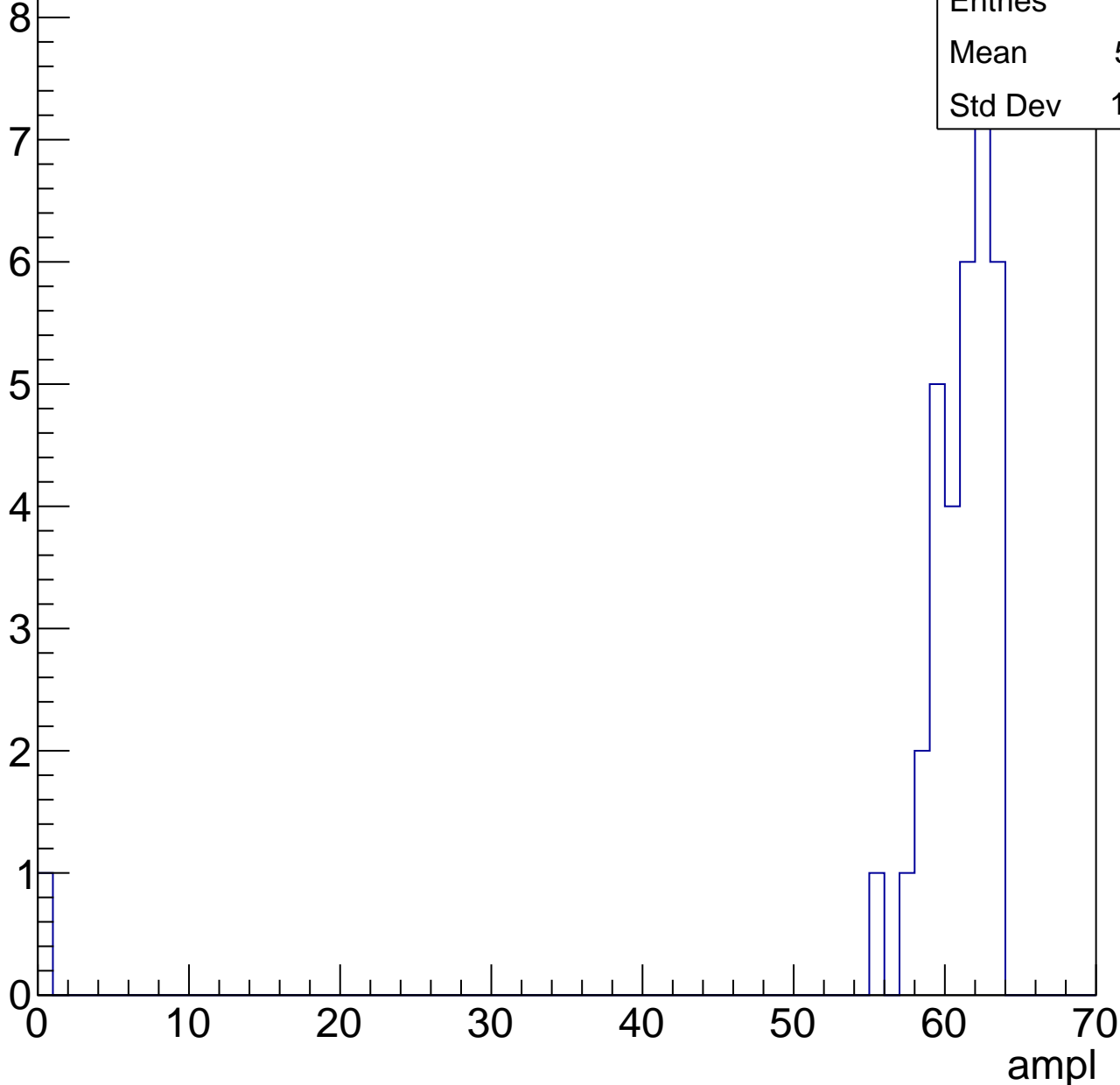
Entries	69
Mean	56.19
Std Dev	3.536

# B1L100S, U2-ch16, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	34
Mean	58.91
Std Dev	10.43



# B1L100S, U2-ch16, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry





# B1L100S, U2-ch16, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L100S, U2-ch17, adc0

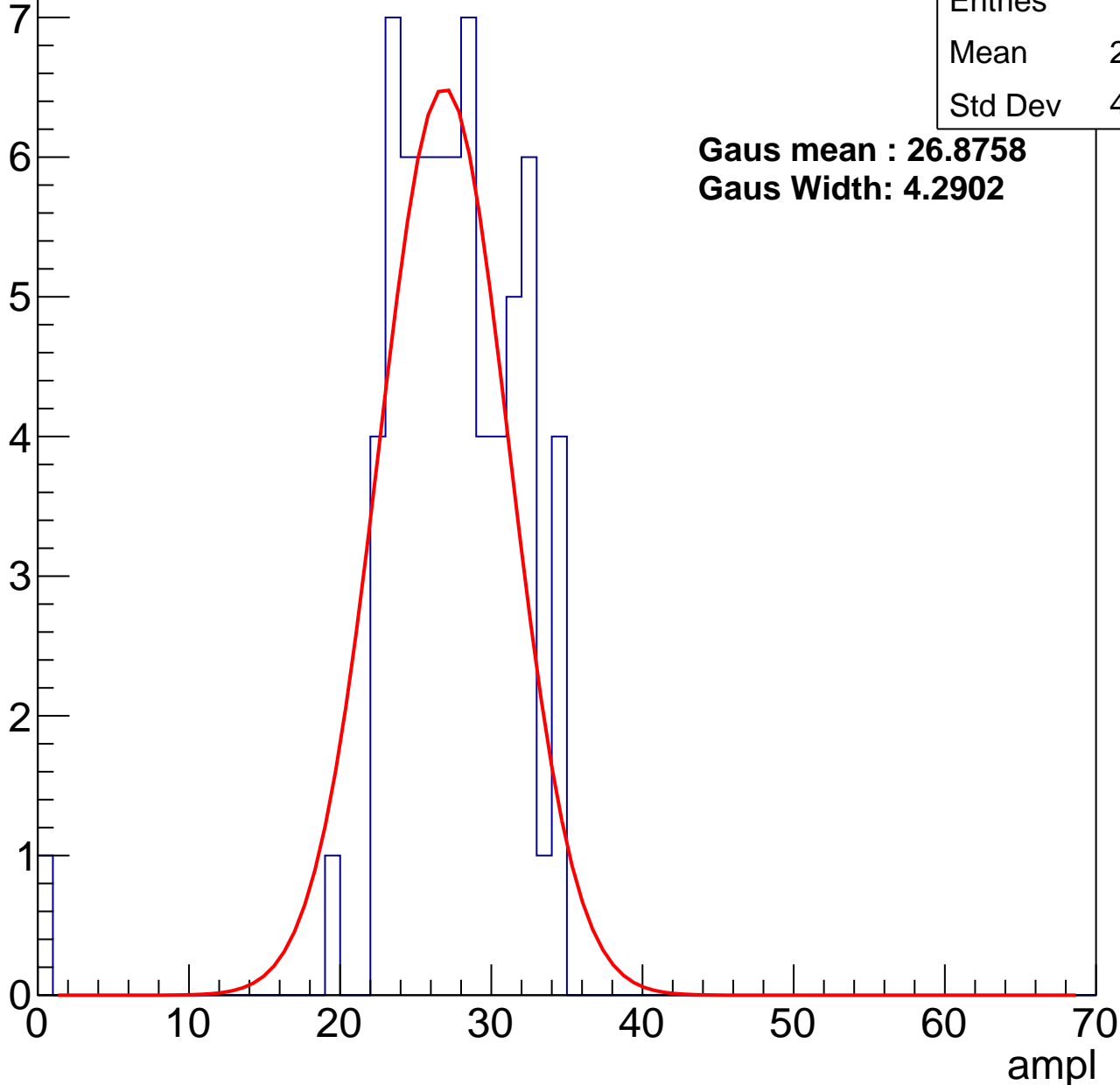
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	68
Mean	26.88
Std Dev	4.864

**Gaus mean : 26.8758**

**Gaus Width: 4.2902**



# B1L100S, U2-ch17, adc1

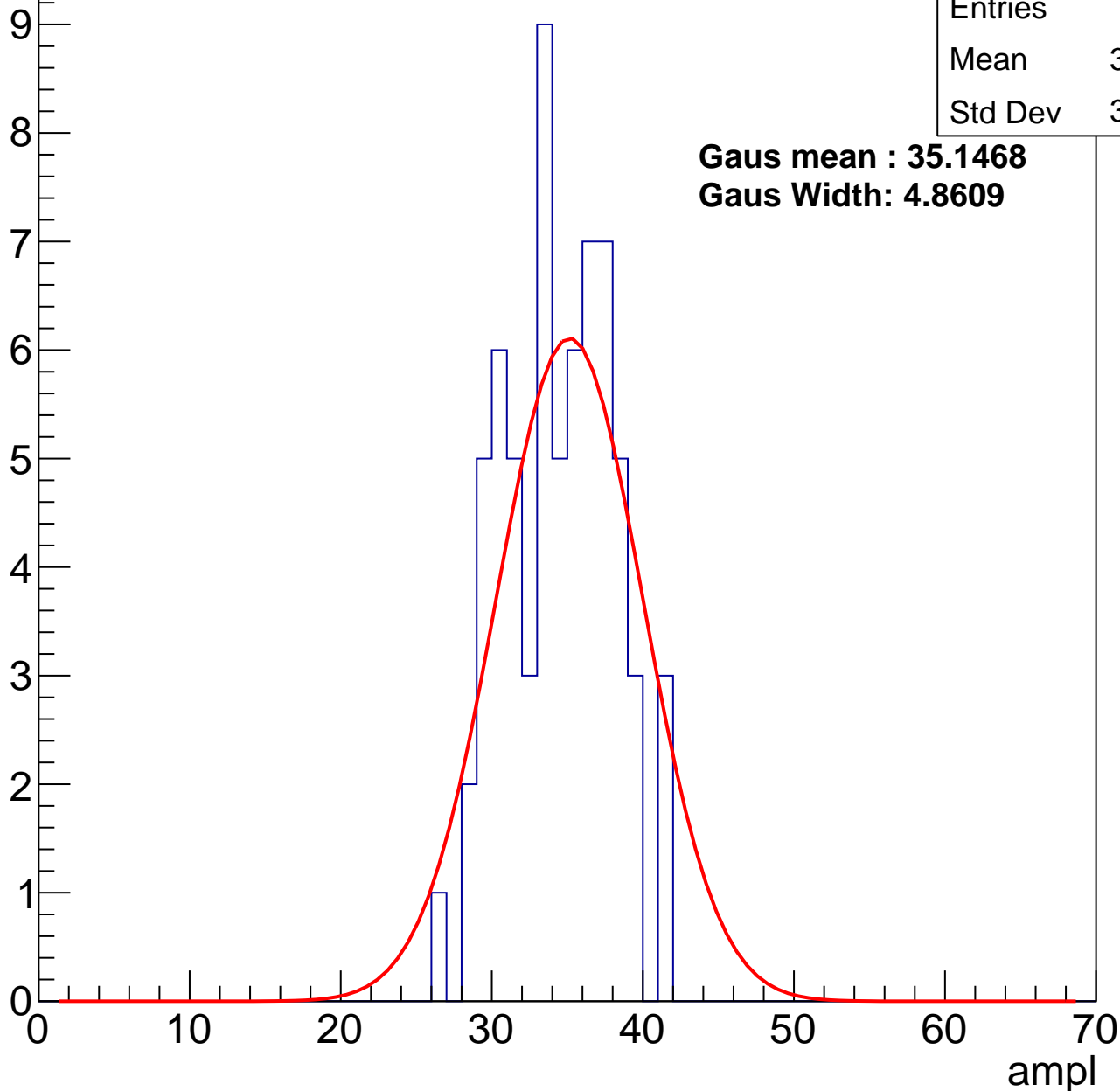
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	67
Mean	33.97
Std Dev	3.503

**Gaus mean : 35.1468**

**Gaus Width: 4.8609**



# B1L100S, U2-ch17, adc2

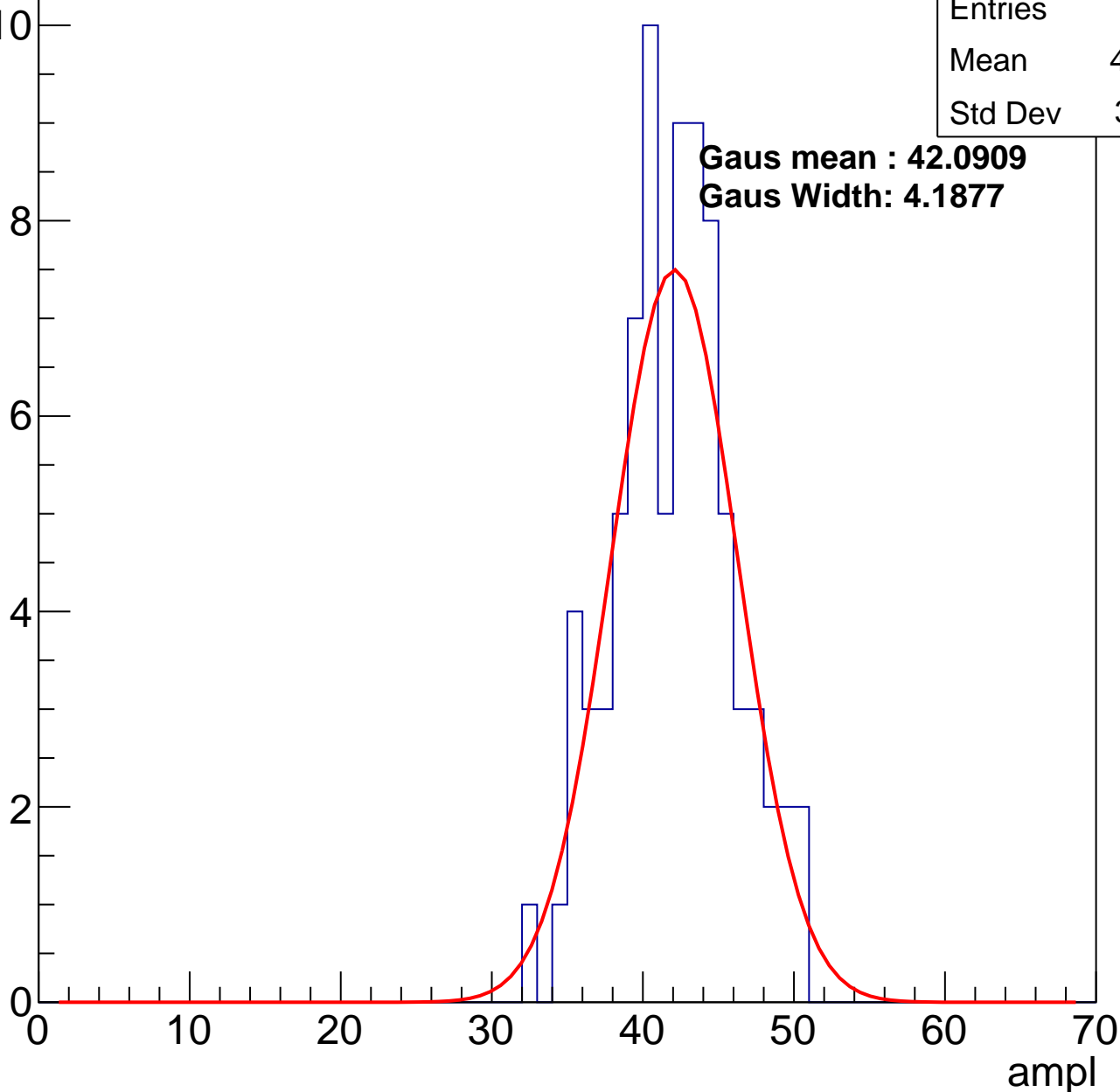
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	82
Mean	41.56
Std Dev	3.861

**Gaus mean : 42.0909**

**Gaus Width: 4.1877**

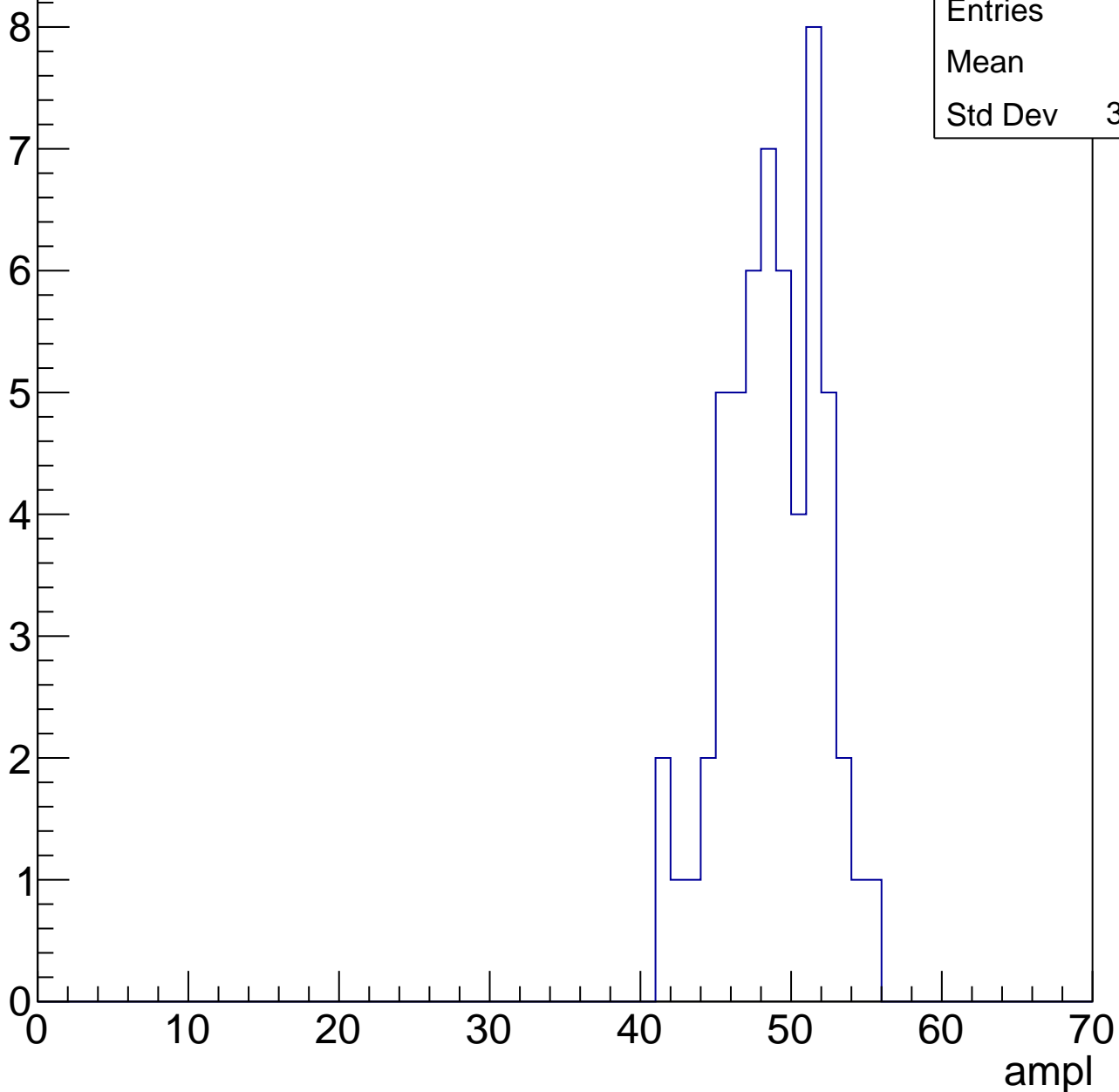


# B1L100S, U2-ch17, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	56
Mean	48.3
Std Dev	3.179

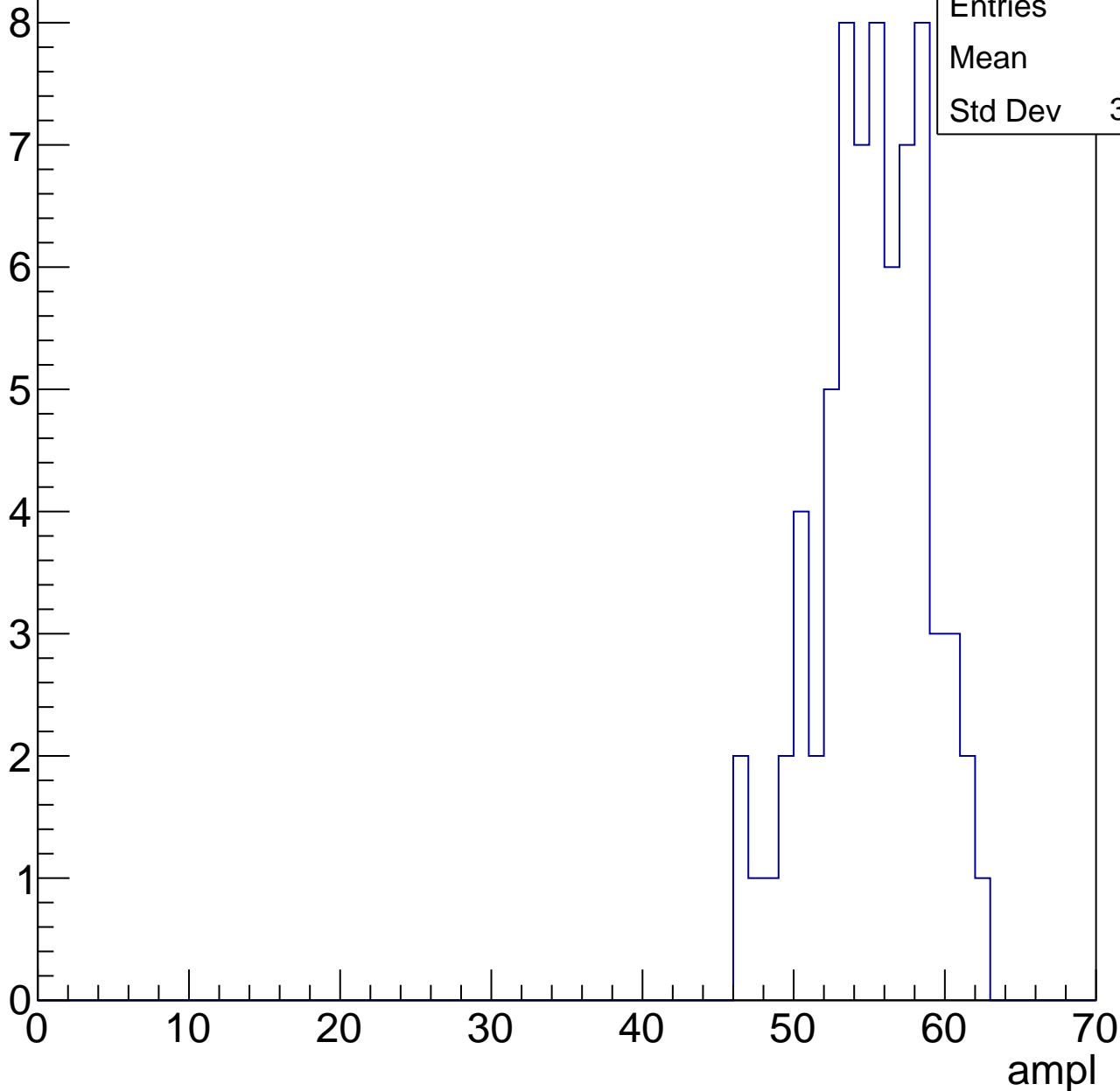


# B1L100S, U2-ch17, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	70
Mean	54.7
Std Dev	3.599



# B1L100S, U2-ch17, adc5

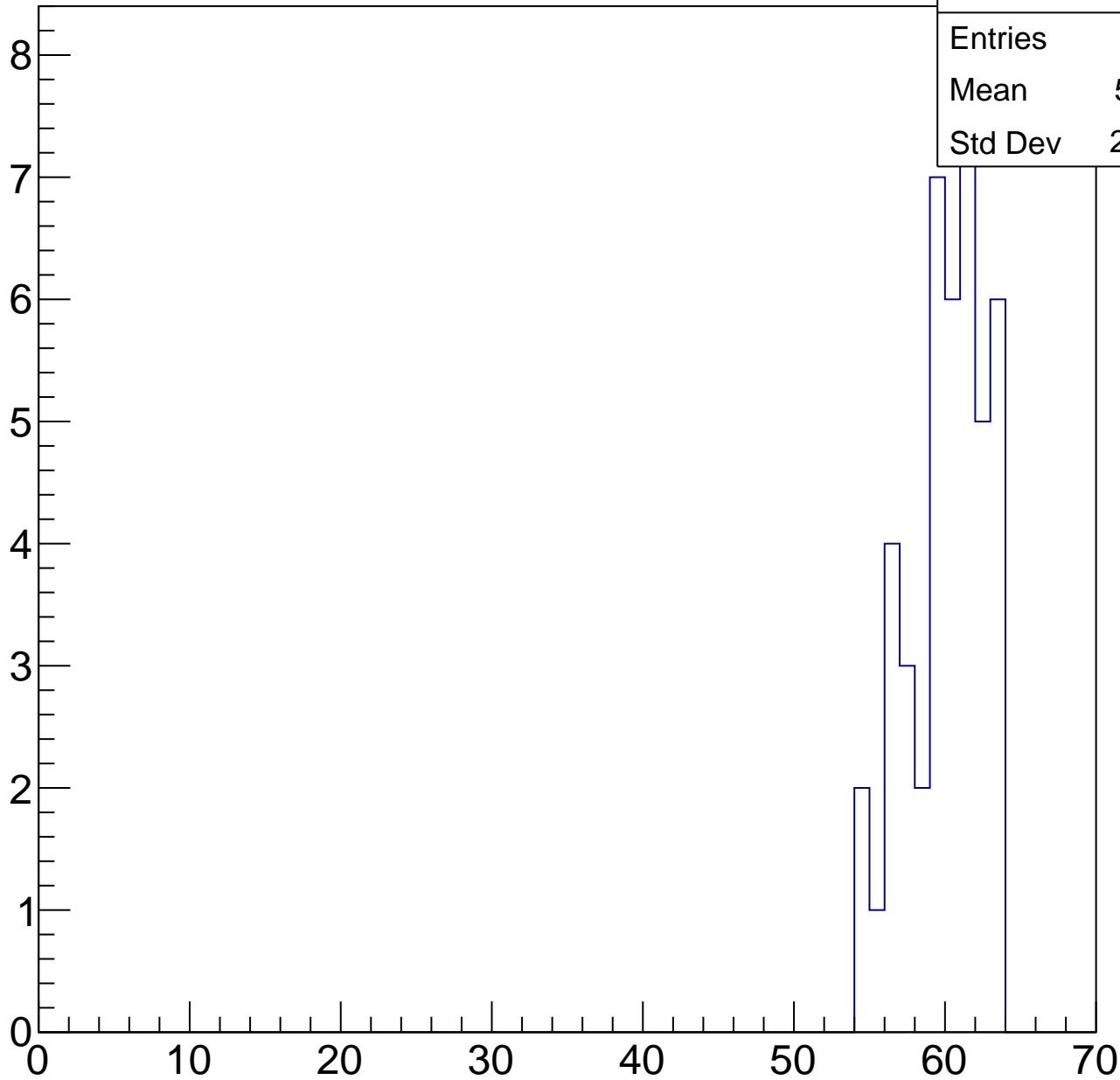
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	44
Mean	59.61
Std Dev	2.516

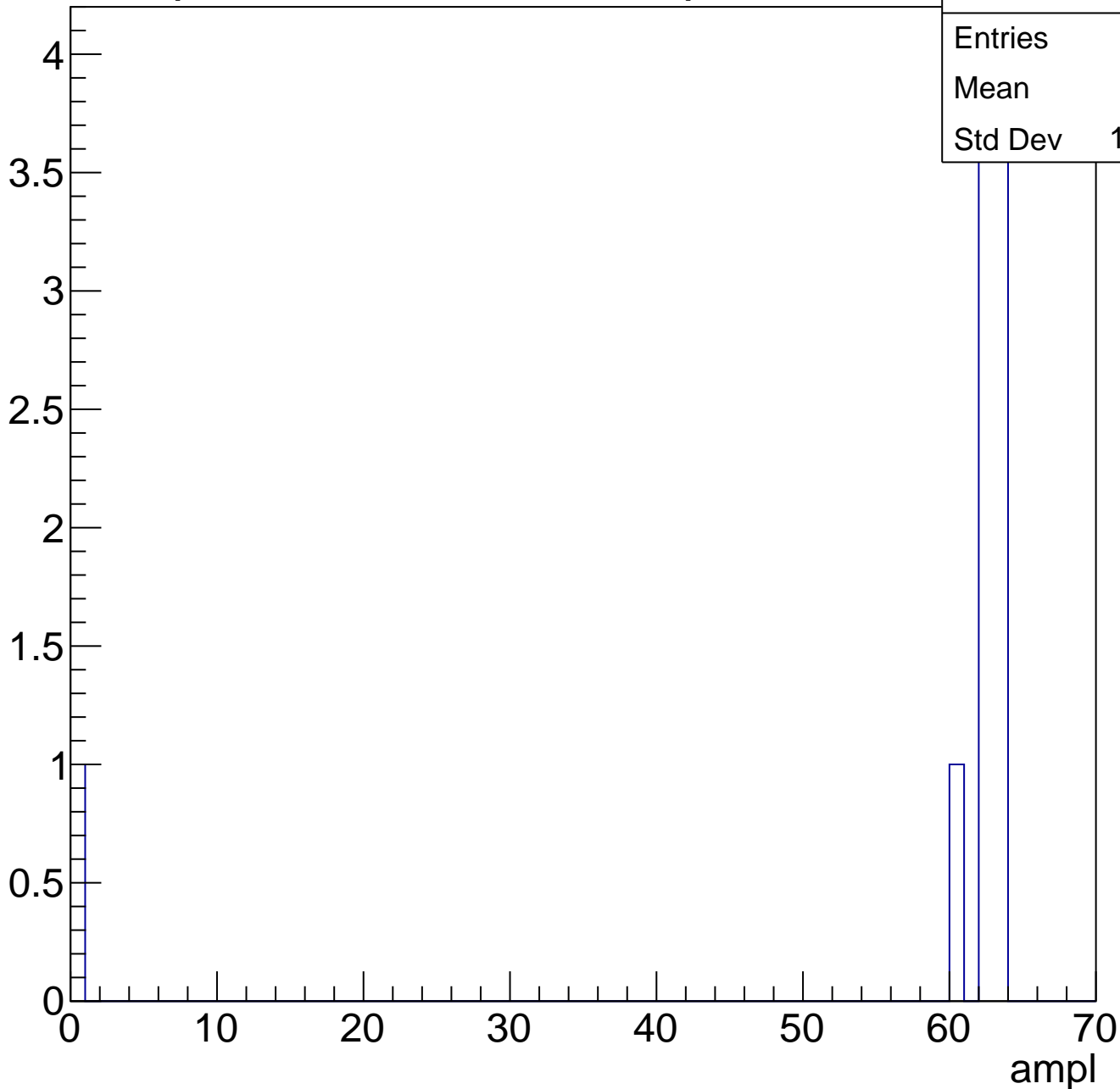
ampl



# B1L100S, U2-ch17, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry





# B1L100S, U2-ch17, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L100S, U2-ch18, adc0

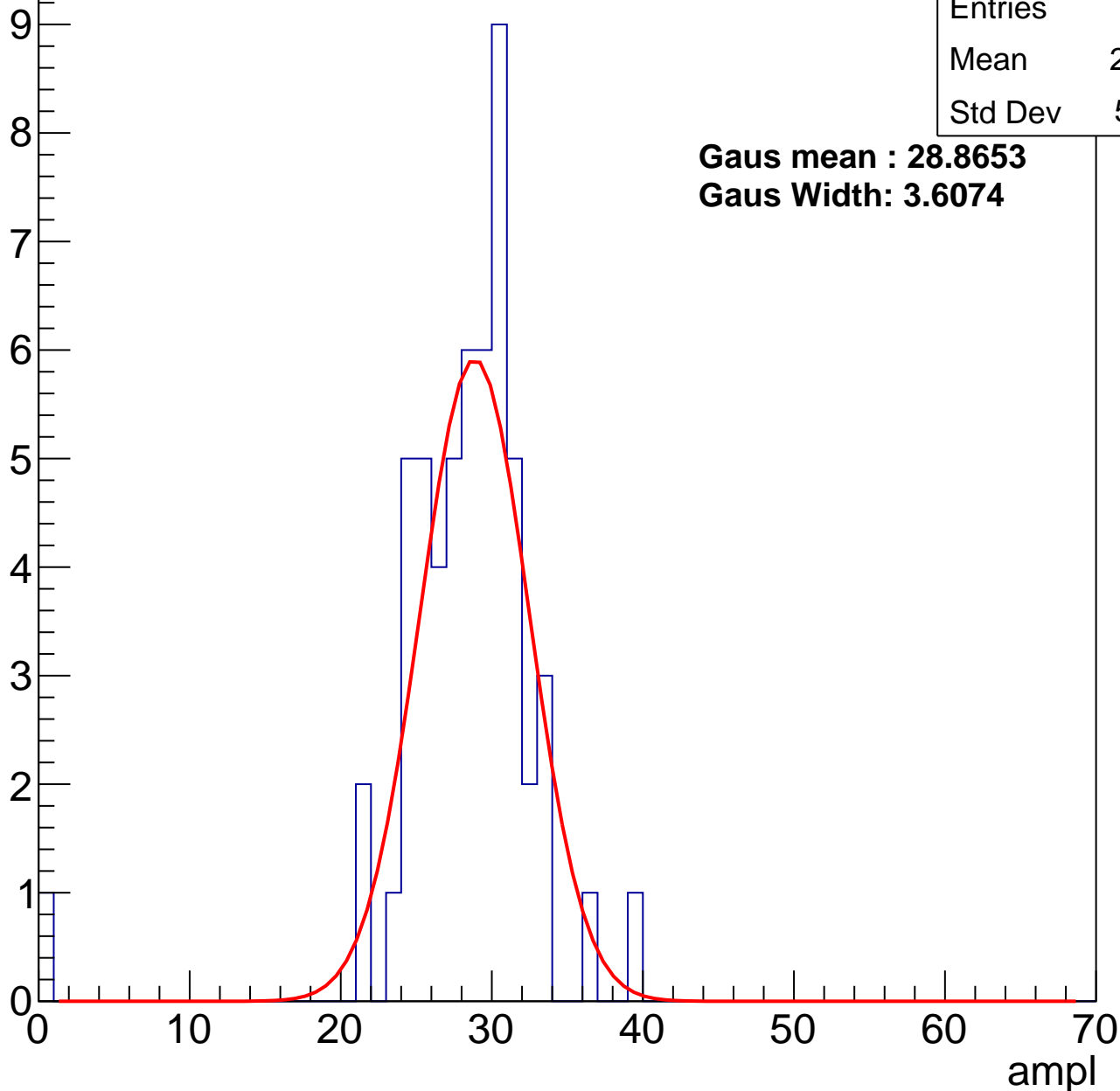
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	56
Mean	27.75
Std Dev	5.051

**Gaus mean : 28.8653**

**Gaus Width: 3.6074**



# B1L100S, U2-ch18, adc1

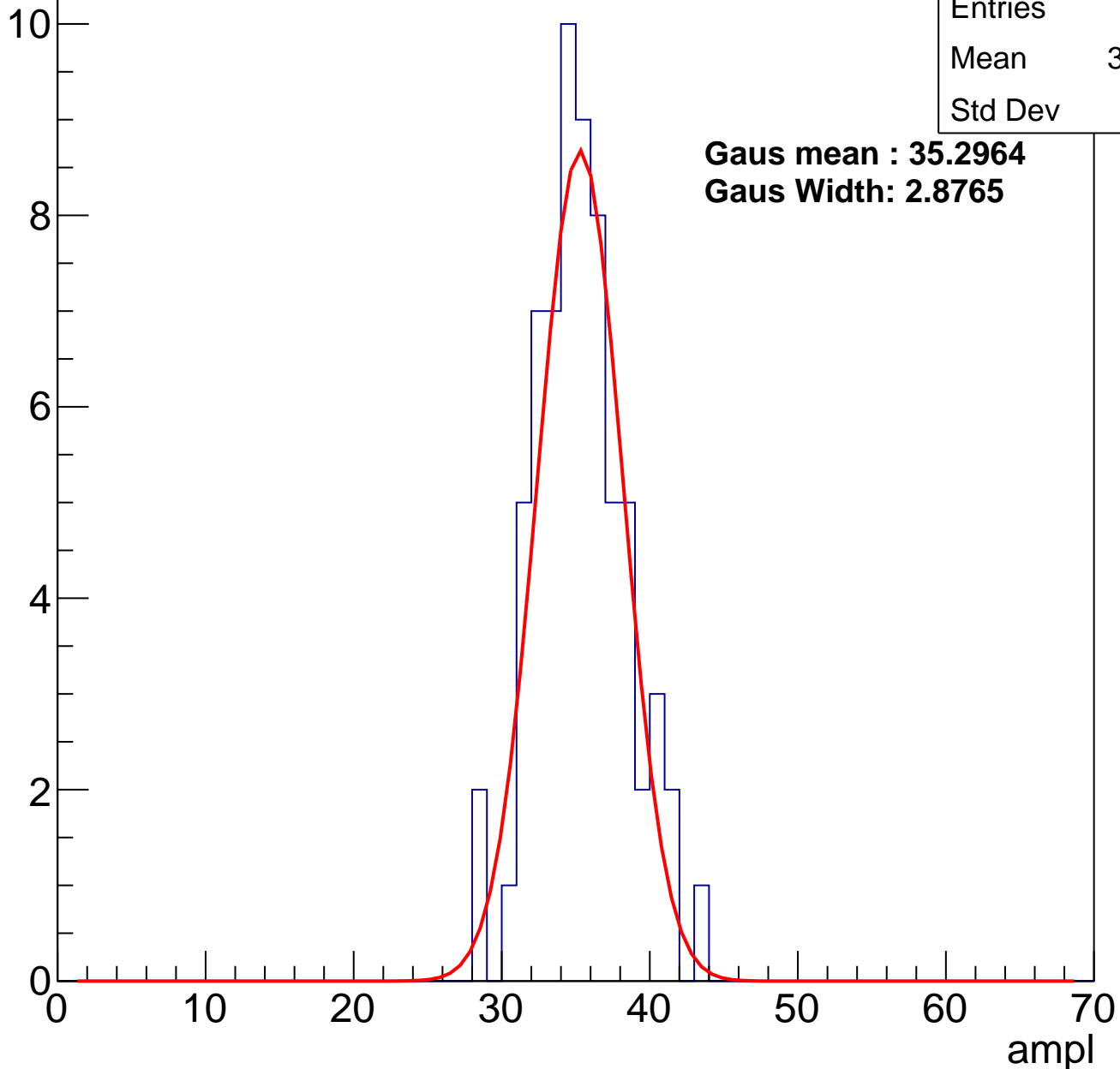
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	67
Mean	34.88
Std Dev	3.04

**Gaus mean : 35.2964**

**Gaus Width: 2.8765**

Entry



# B1L100S, U2-ch18, adc2

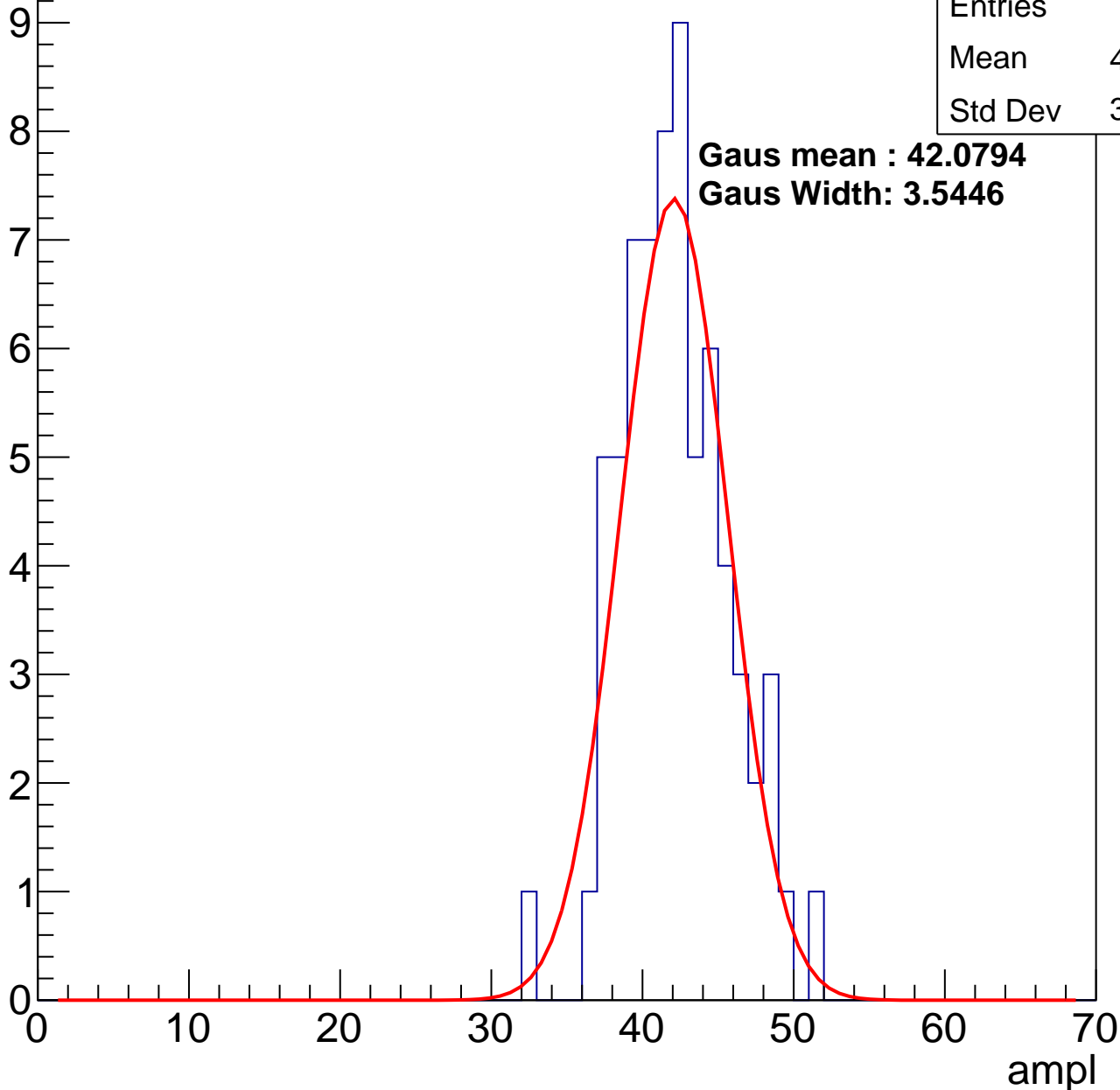
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	68
Mean	41.72
Std Dev	3.506

**Gaus mean : 42.0794**

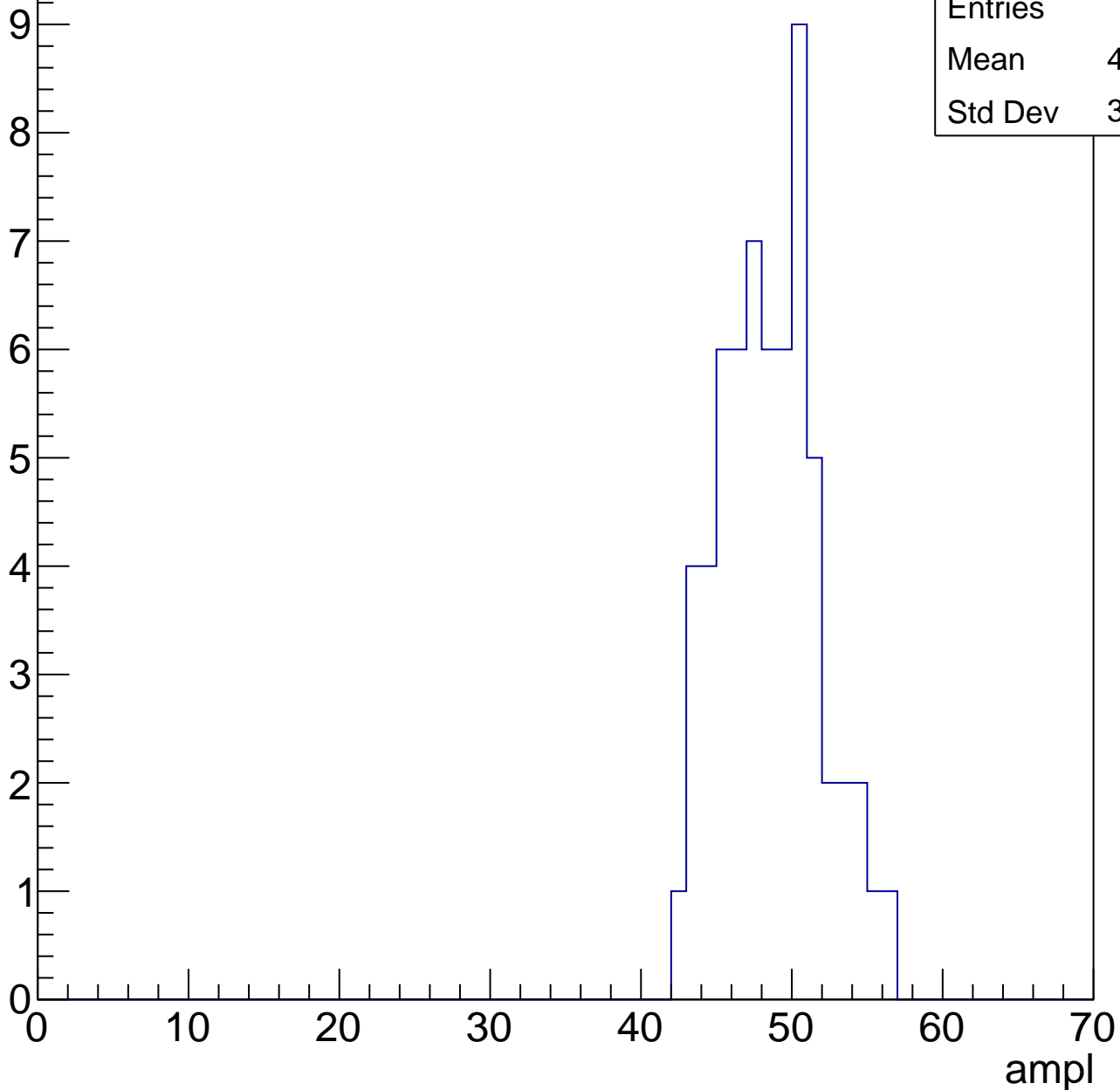
**Gaus Width: 3.5446**



# B1L100S, U2-ch18, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



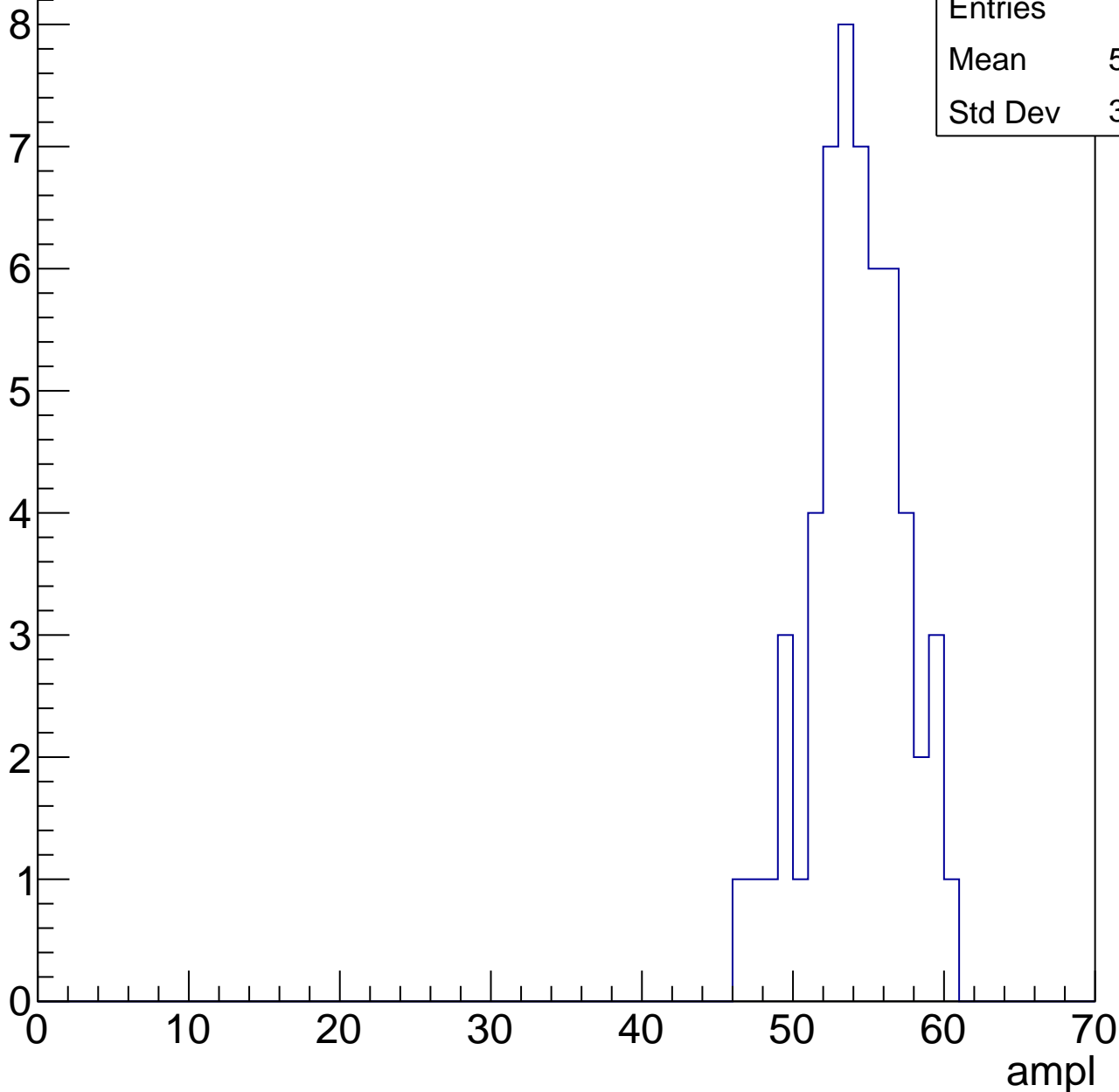
Entries	62
Mean	48.08
Std Dev	3.209

# B1L100S, U2-ch18, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	55
Mean	53.73
Std Dev	3.066



# B1L100S, U2-ch18, adc5

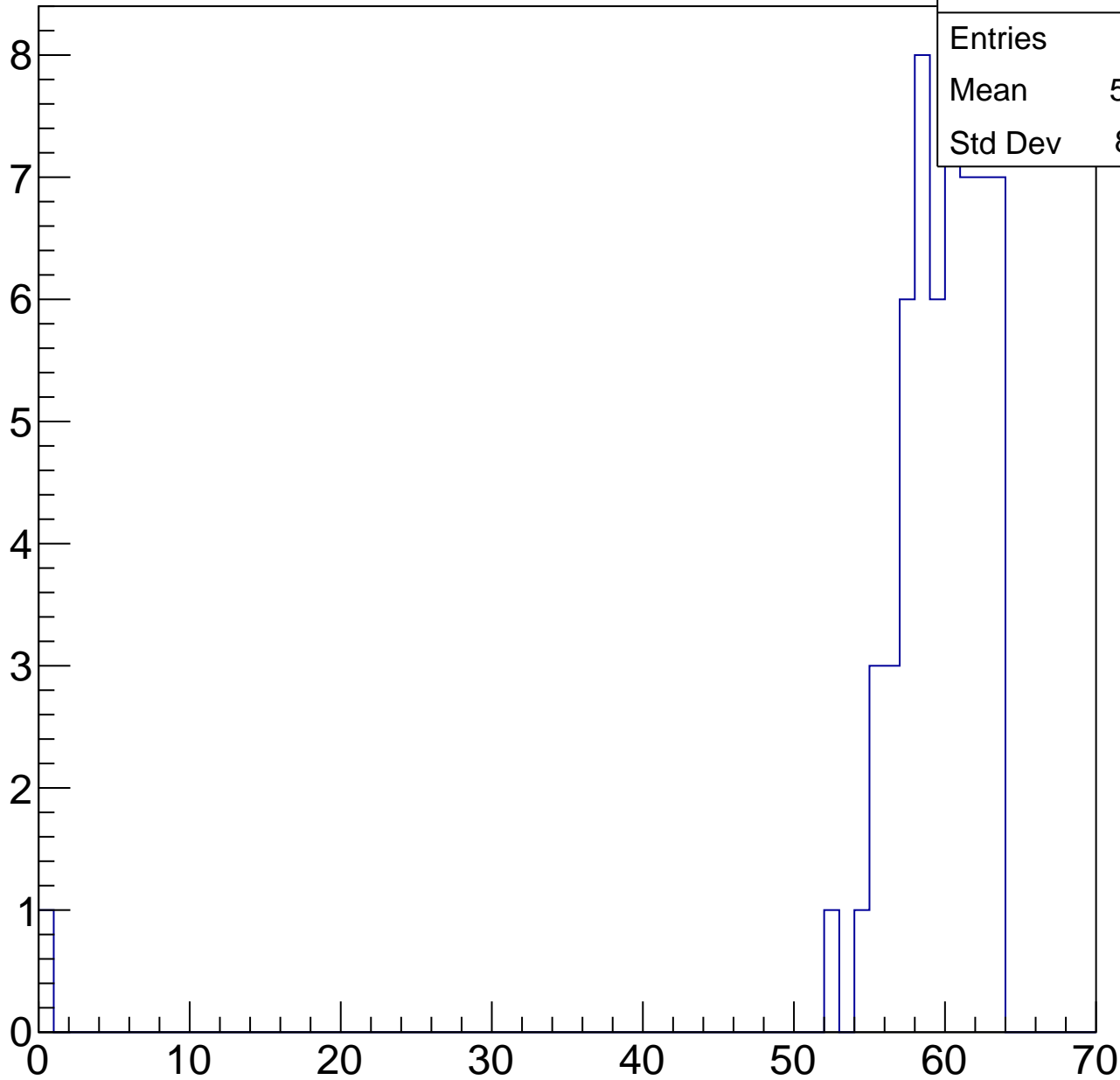
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	58
Mean	58.29
Std Dev	8.141

ampl



# B1L100S, U2-ch18, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

3

2.5

2

1.5

1

0.5

0

0

10

20

30

40

50

60

70

ampl

Entries	11
Mean	61.55
Std Dev	1.233



# B1L100S, U2-ch18, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



# B1L100S, U2-ch19, adc0

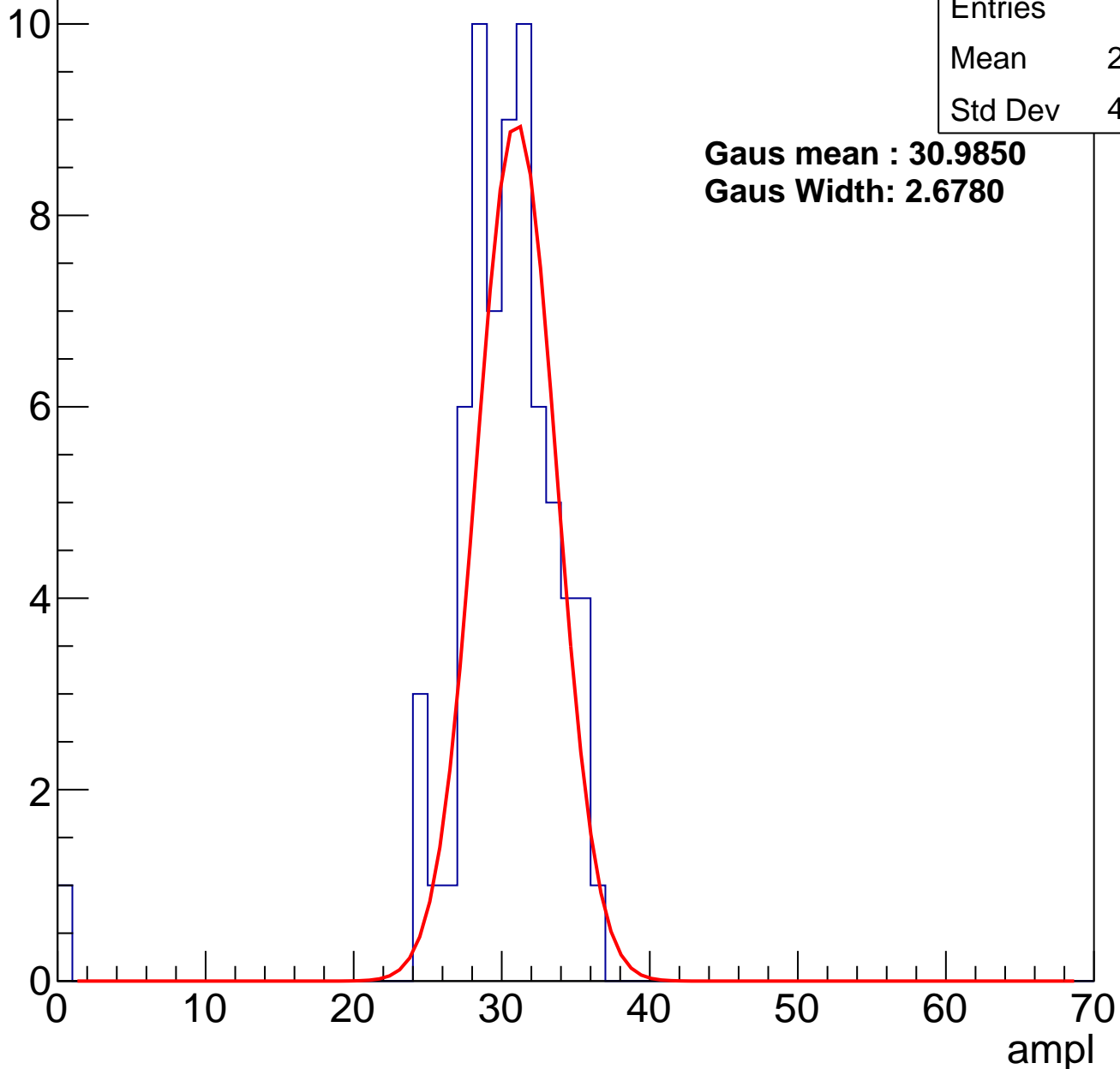
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	68
Mean	29.66
Std Dev	4.572

**Gaus mean : 30.9850**

**Gaus Width: 2.6780**

Entry



# B1L100S, U2-ch19, adc1

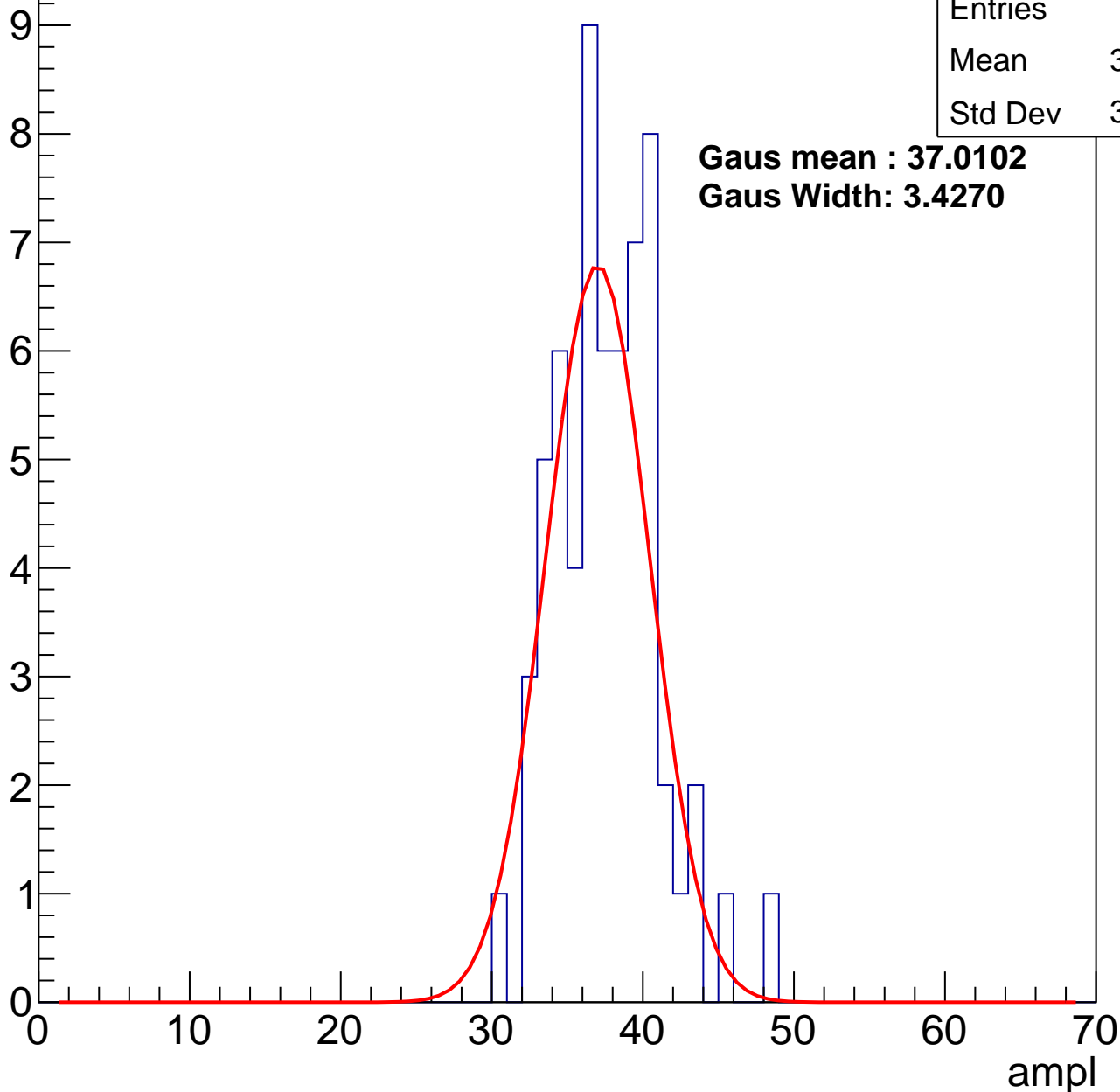
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	62
Mean	37.18
Std Dev	3.363

**Gaus mean : 37.0102**

**Gaus Width: 3.4270**



# B1L100S, U2-ch19, adc2

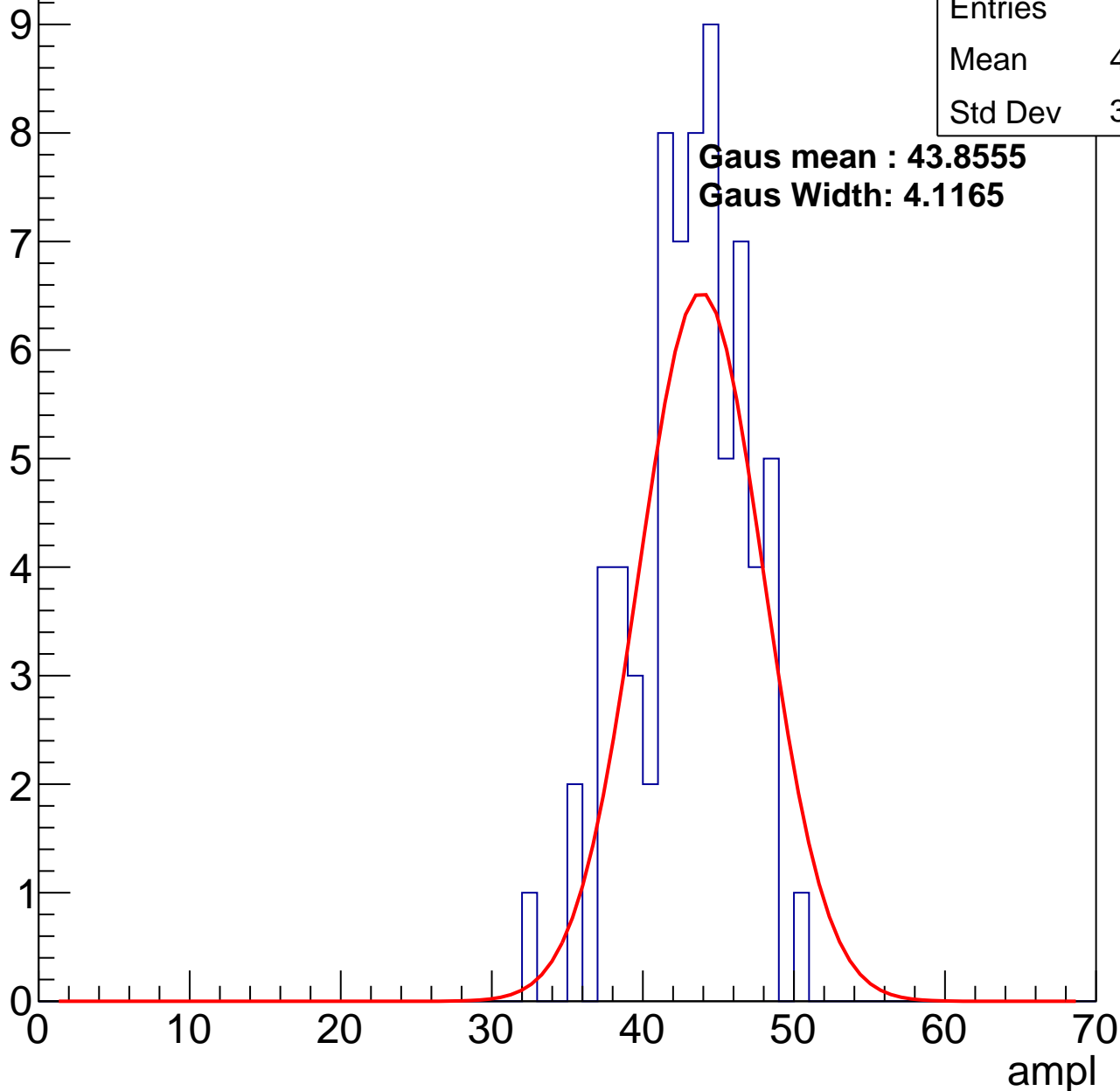
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	70
Mean	42.66
Std Dev	3.625

**Gaus mean : 43.8555**

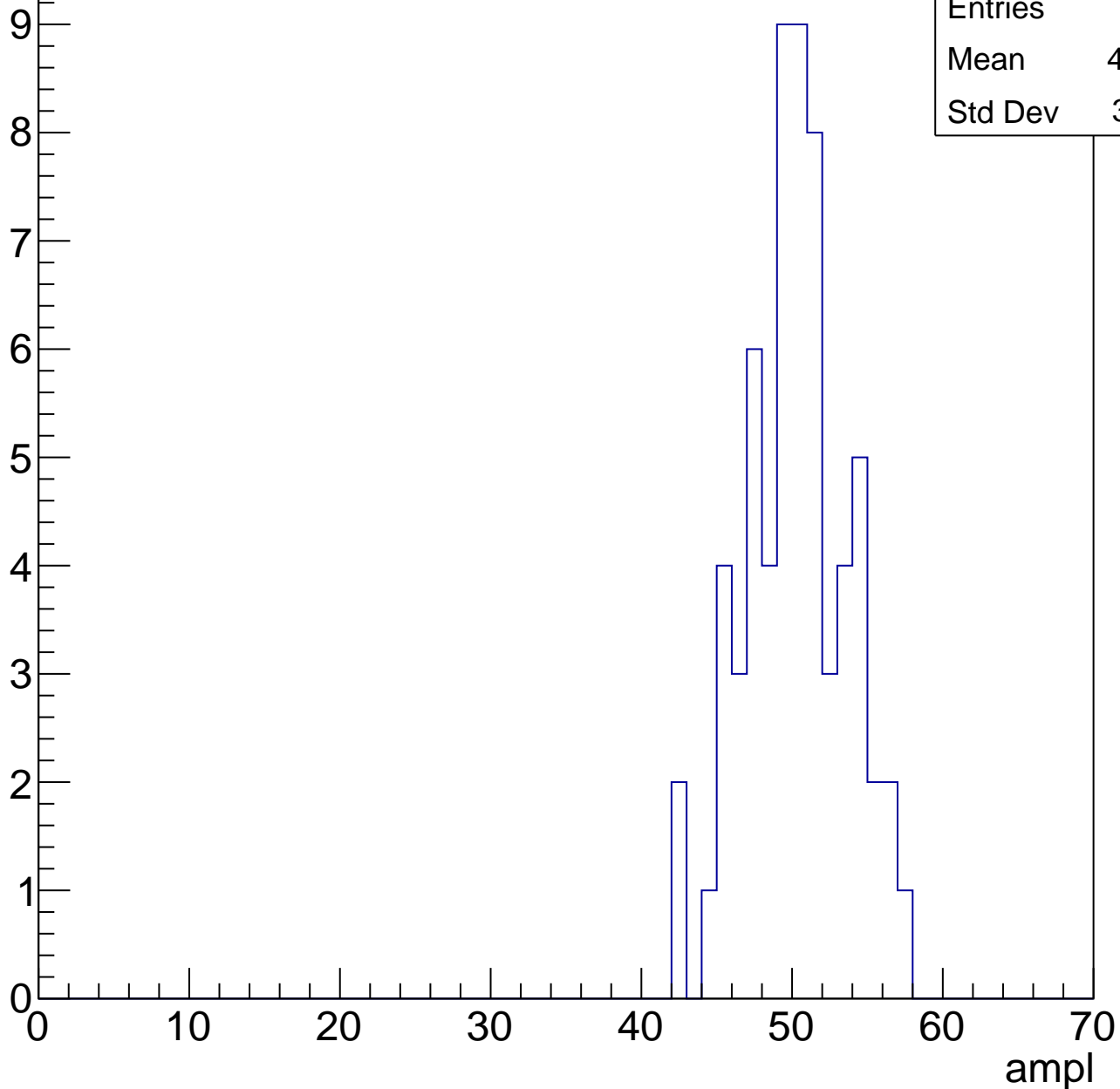
**Gaus Width: 4.1165**



# B1L100S, U2-ch19, adc3

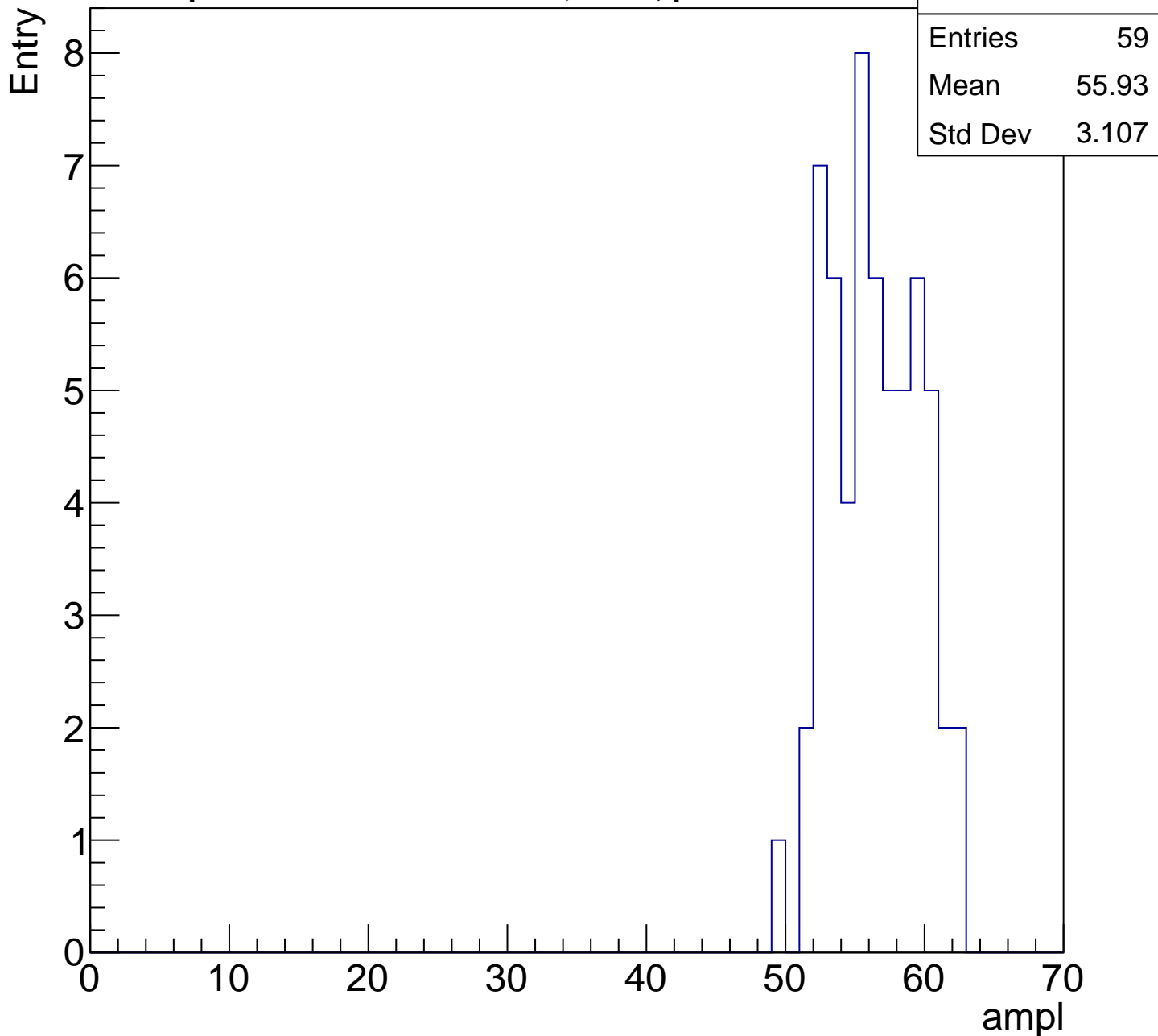
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



# B1L100S, U2-ch19, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

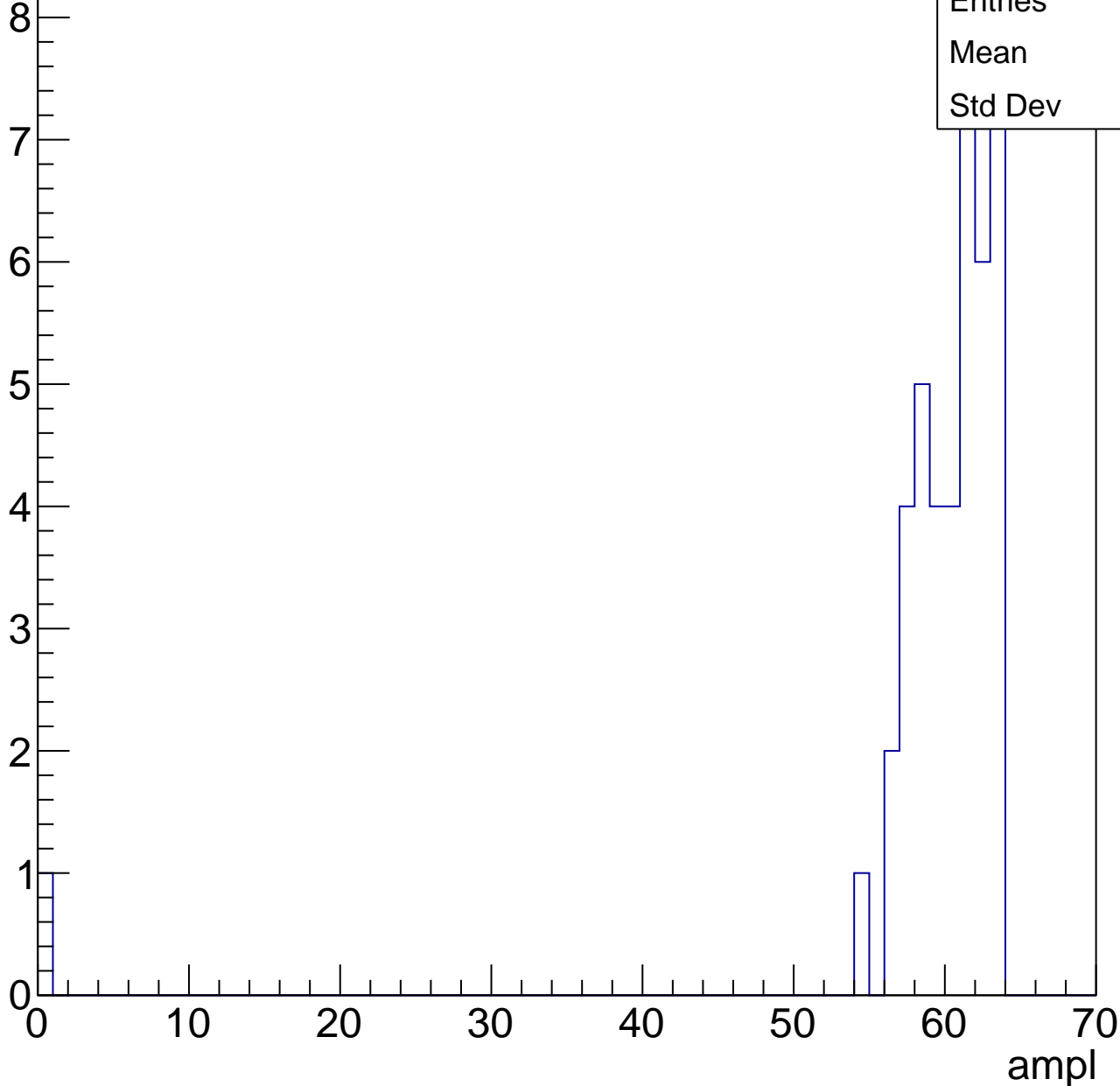


# B1L100S, U2-ch19, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	43
Mean	58.7
Std Dev	9.35



# B1L100S, U2-ch19, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

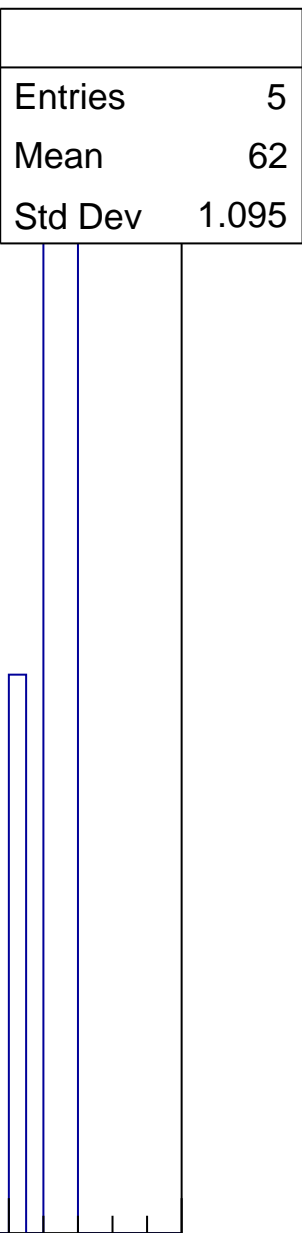
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	5
Mean	62
Std Dev	1.095

0 10 20 30 40 50 60 70

ampl





# B1L100S, U2-ch19, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



# B1L100S, U2-ch20, adc0

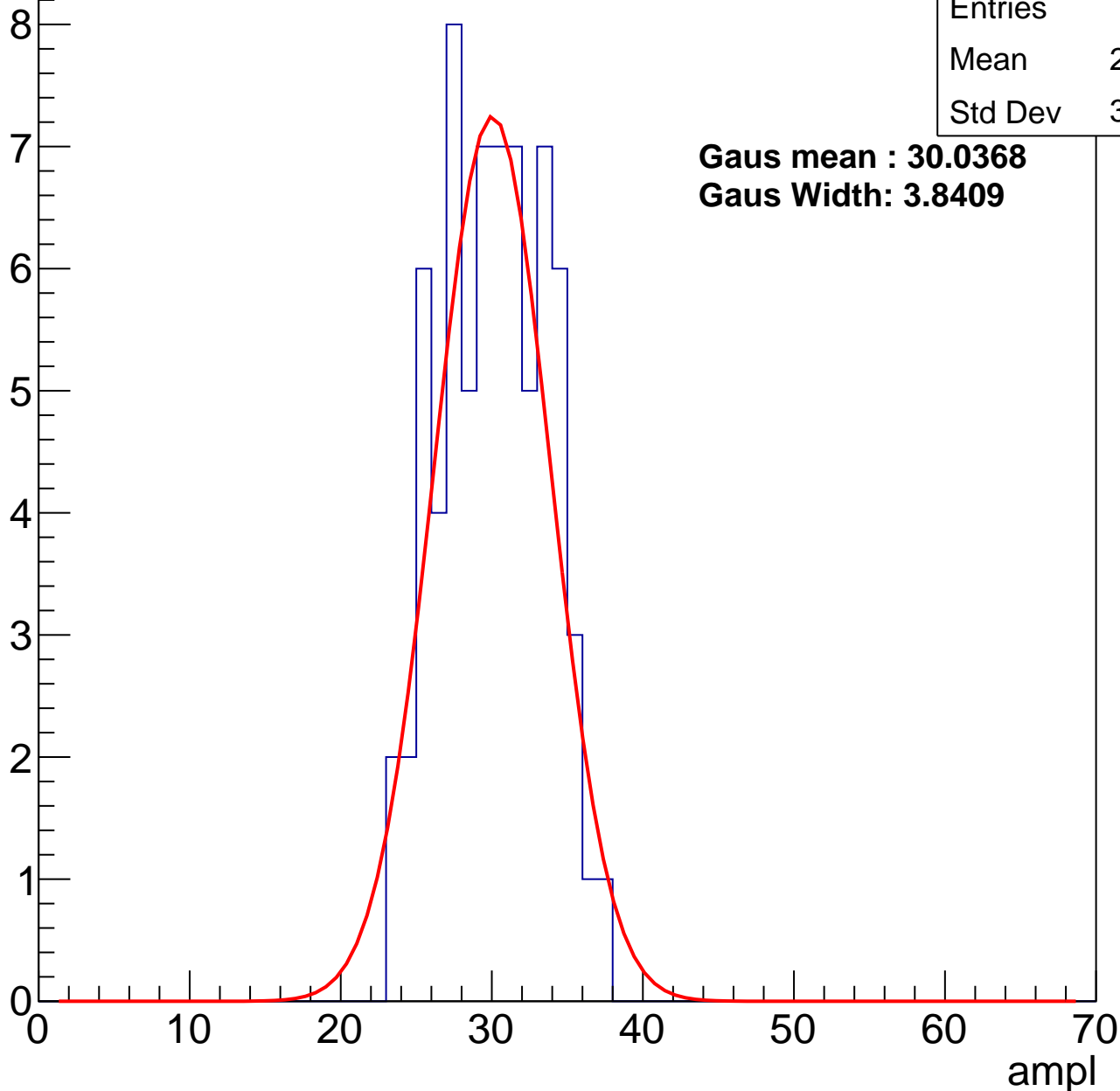
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	71
Mean	29.68
Std Dev	3.402

**Gaus mean : 30.0368**

**Gaus Width: 3.8409**



# B1L100S, U2-ch20, adc1

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	65
Mean	36.34
Std Dev	3.226

**Gaus mean : 36.8262**

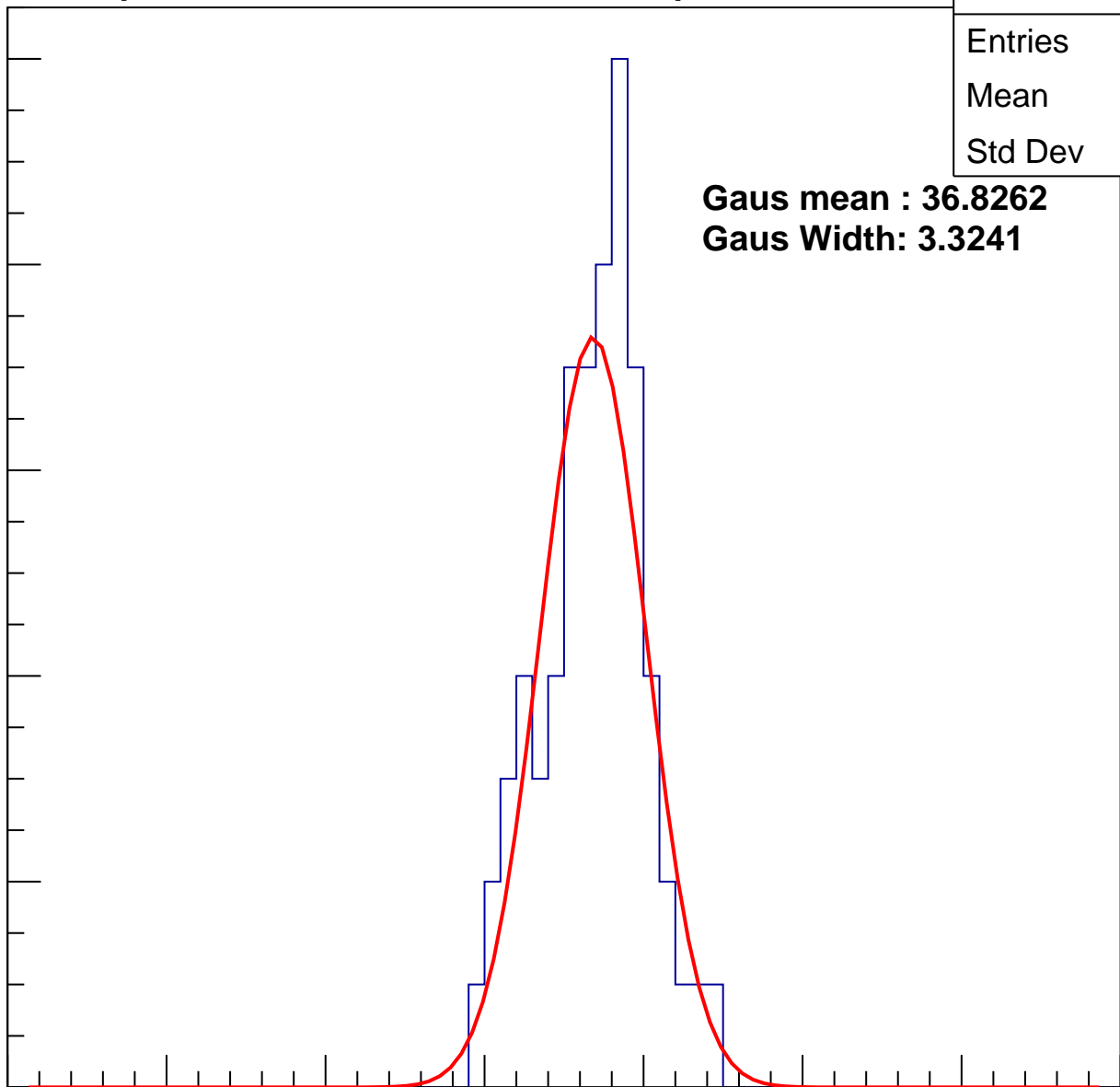
**Gaus Width: 3.3241**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L100S, U2-ch20, adc2

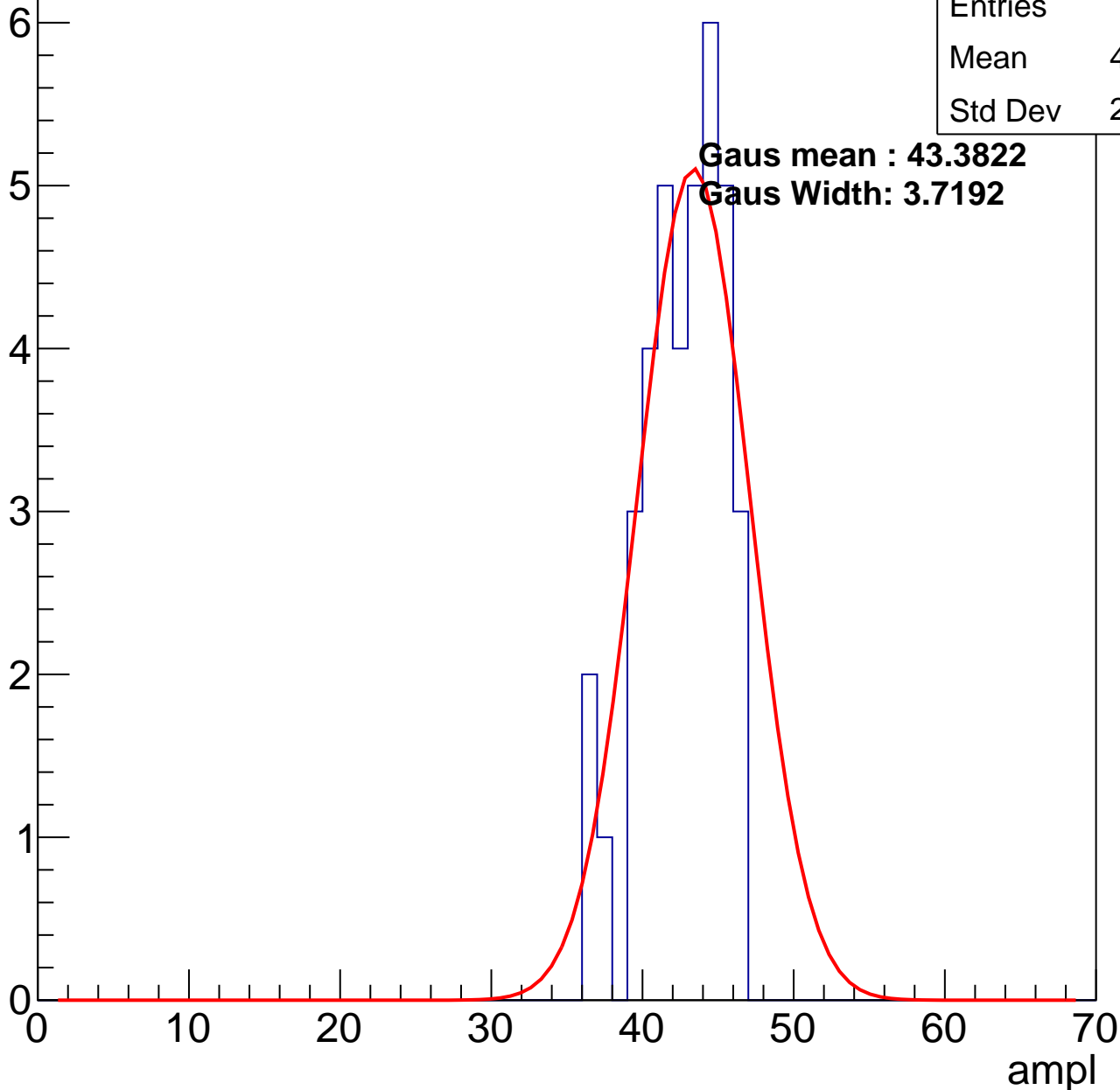
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	38
Mean	42.13
Std Dev	2.647

**Gaus mean : 43.3822**

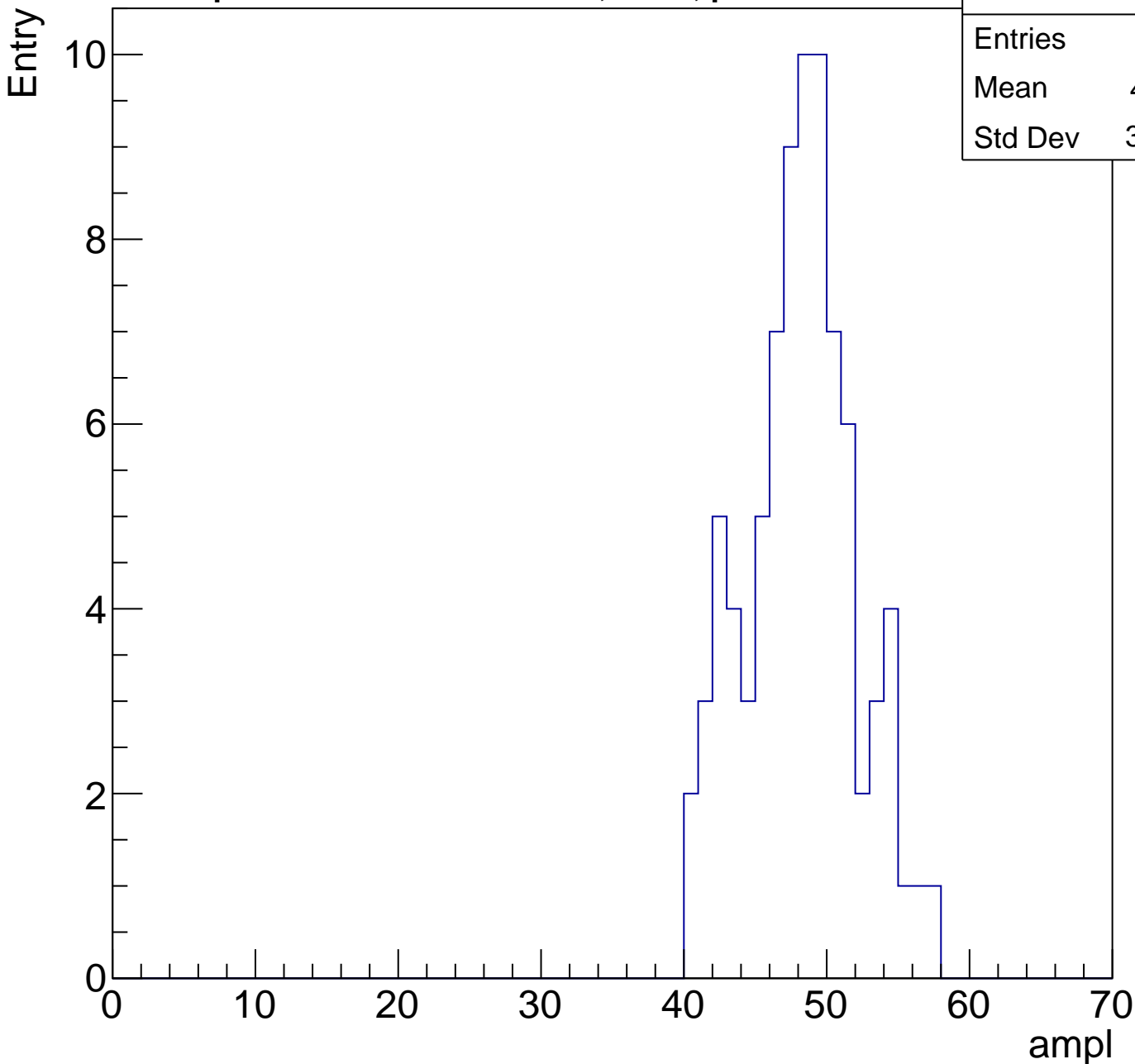
**Gaus Width: 3.7192**



# B1L100S, U2-ch20, adc3

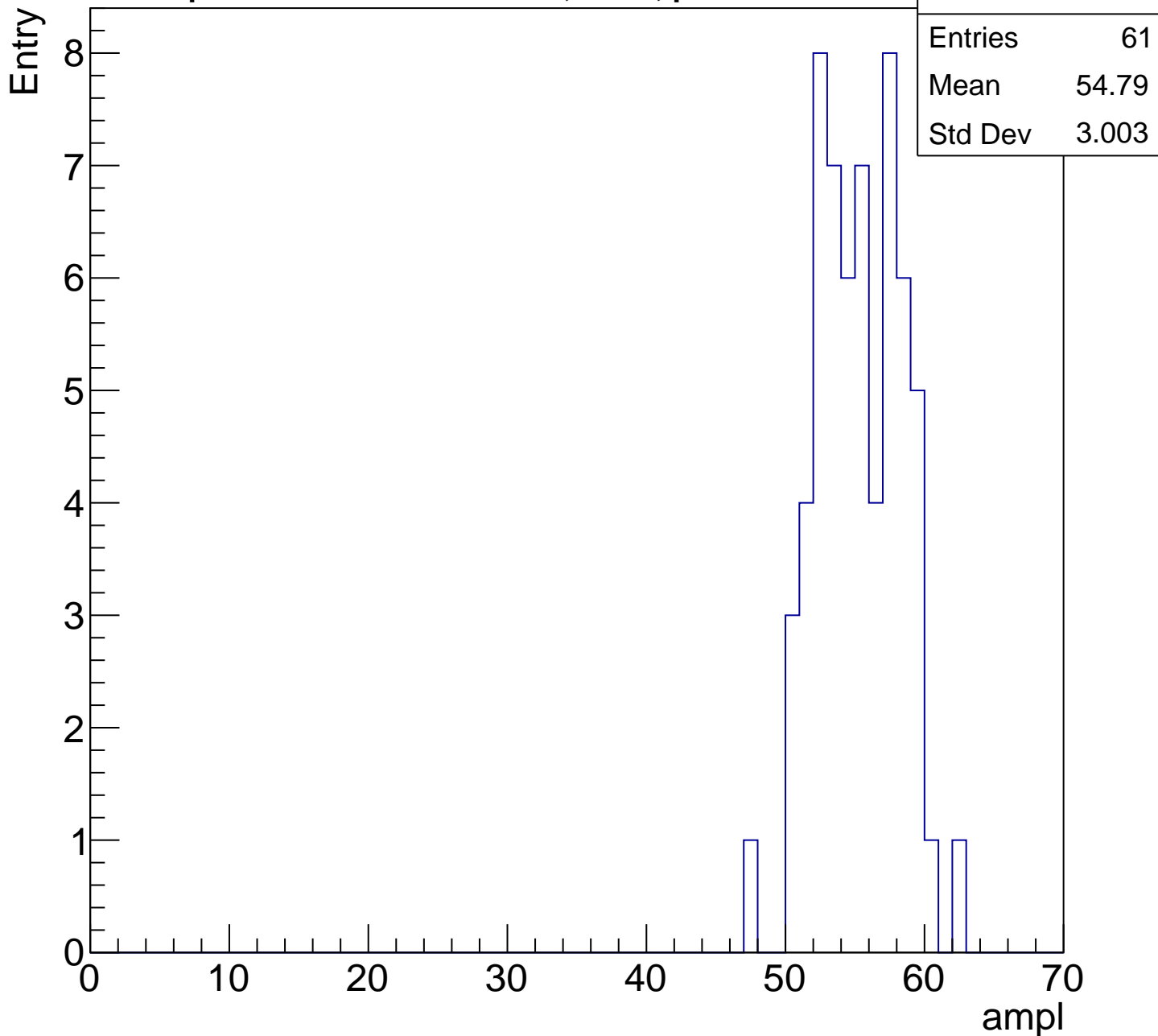
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	83
Mean	47.71
Std Dev	3.826



# B1L100S, U2-ch20, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2



# B1L100S, U2-ch20, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

6

5

4

3

2

1

0

Entries	39
Mean	59.74
Std Dev	2.478

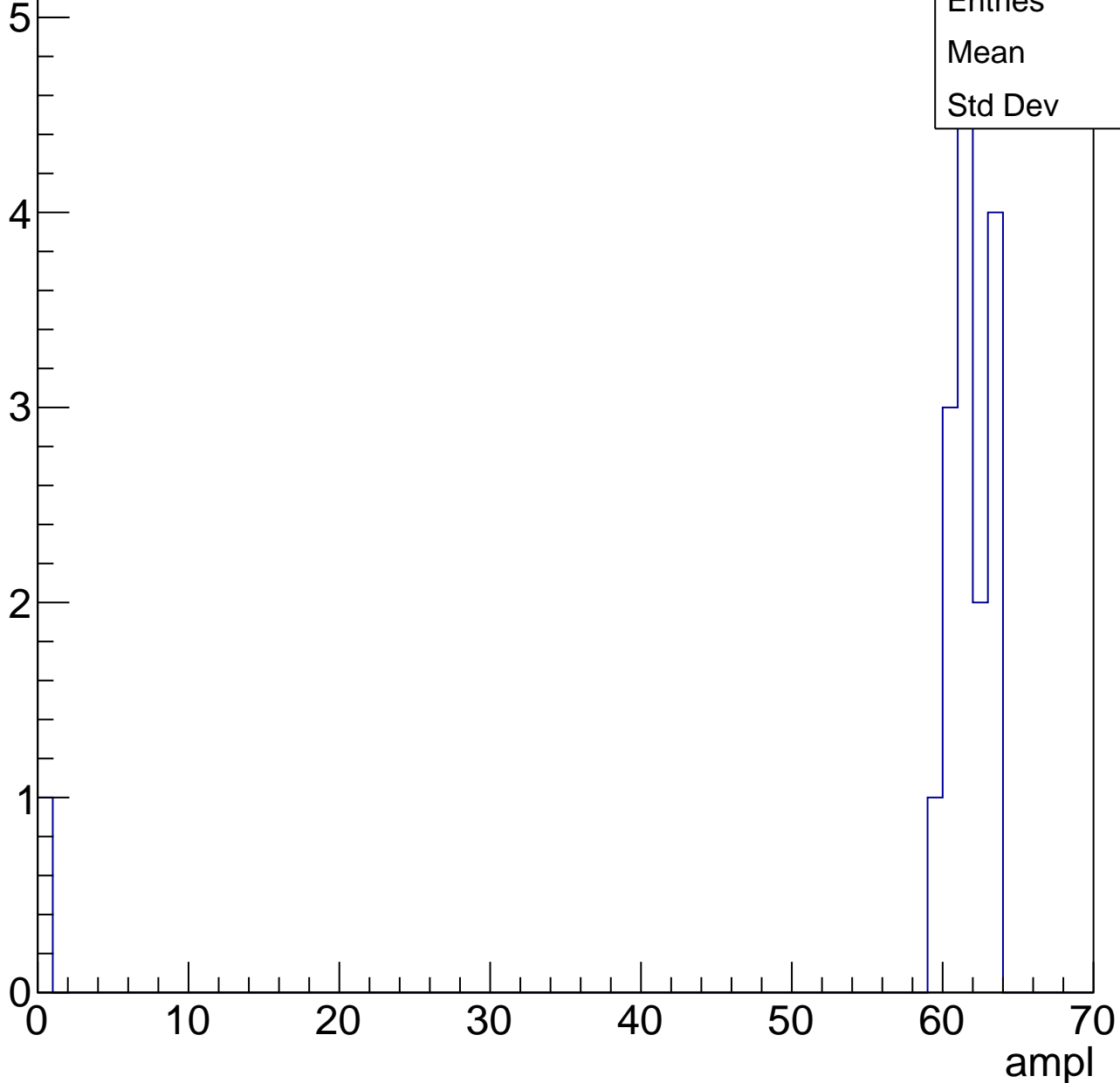
ampl

# B1L100S, U2-ch20, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	16
Mean	57.5
Std Dev	14.9

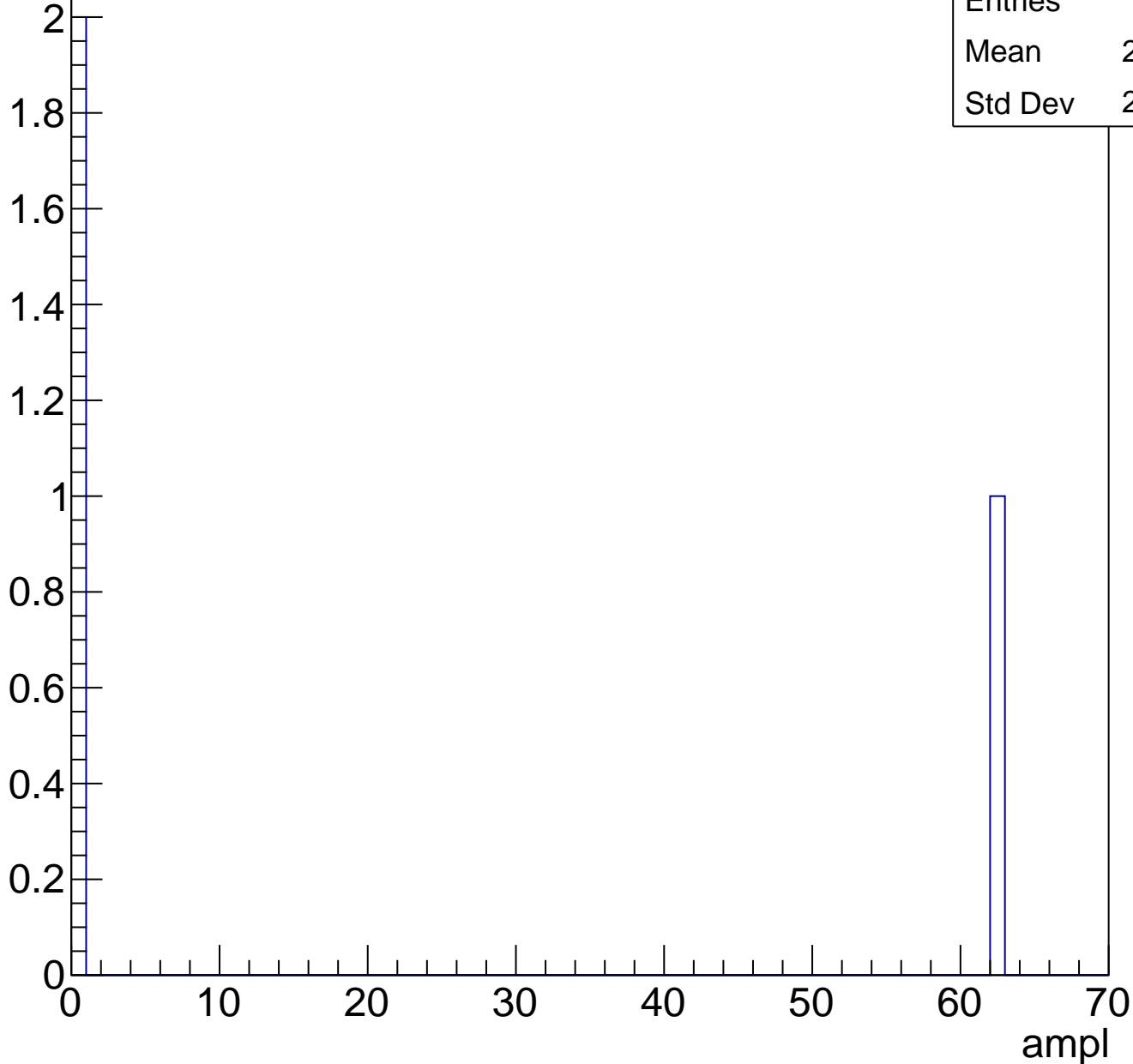




# B1L100S, U2-ch20, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



# B1L100S, U2-ch21, adc0

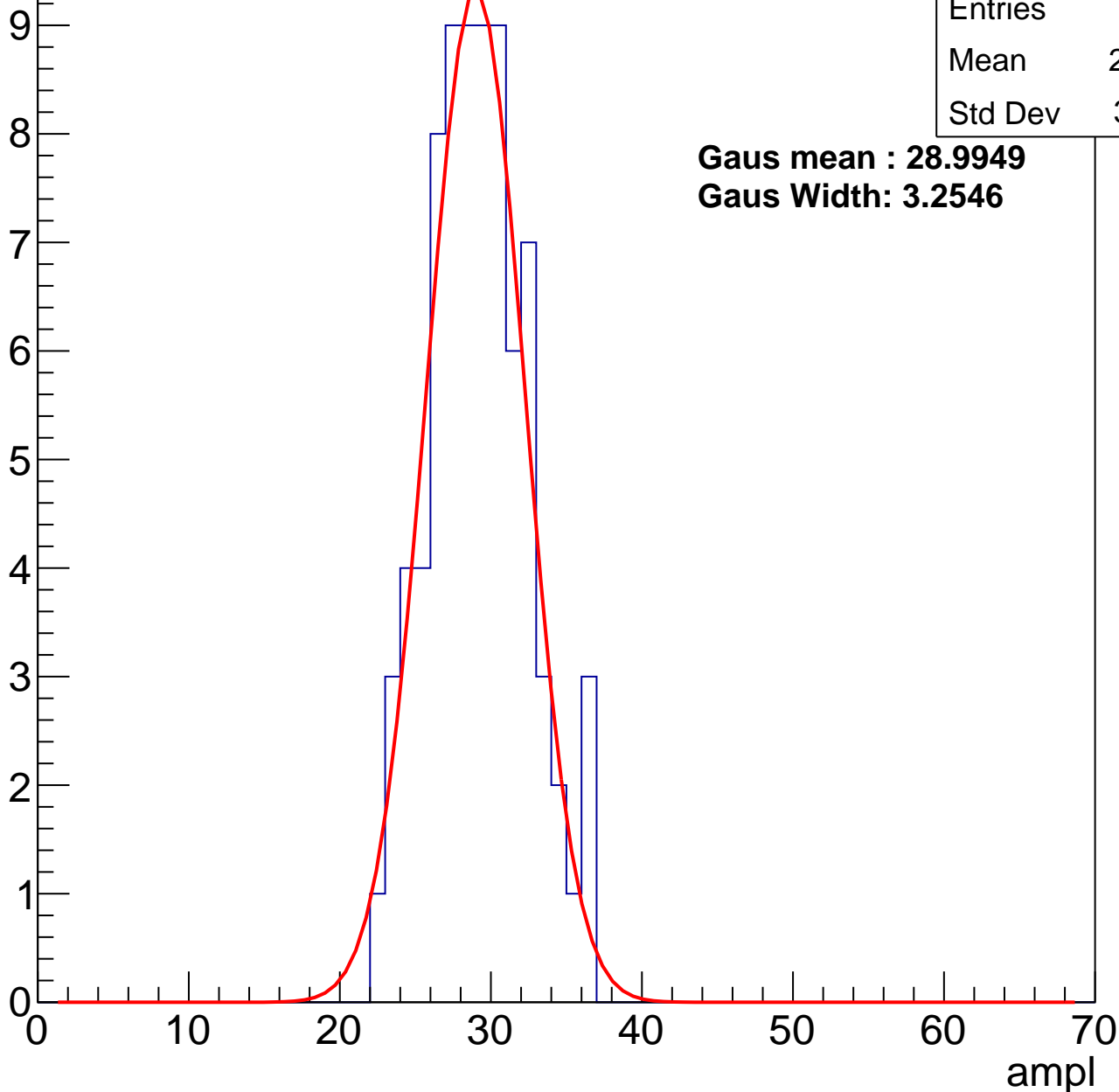
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	78
Mean	28.73
Std Dev	3.221

**Gaus mean : 28.9949**

**Gaus Width: 3.2546**



# B1L100S, U2-ch21, adc1

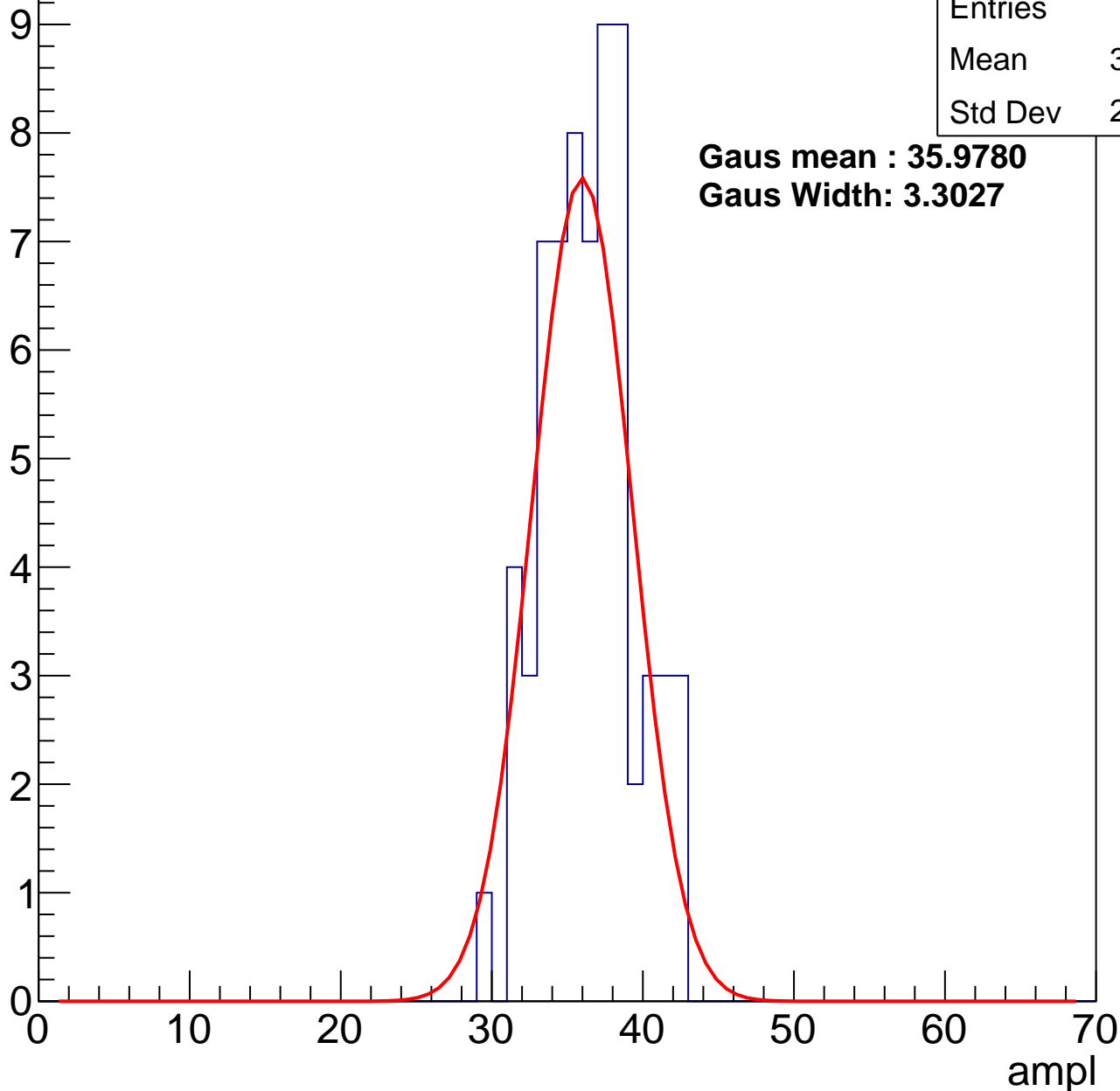
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	66
Mean	35.94
Std Dev	2.989

**Gaus mean : 35.9780**

**Gaus Width: 3.3027**



# B1L100S, U2-ch21, adc2

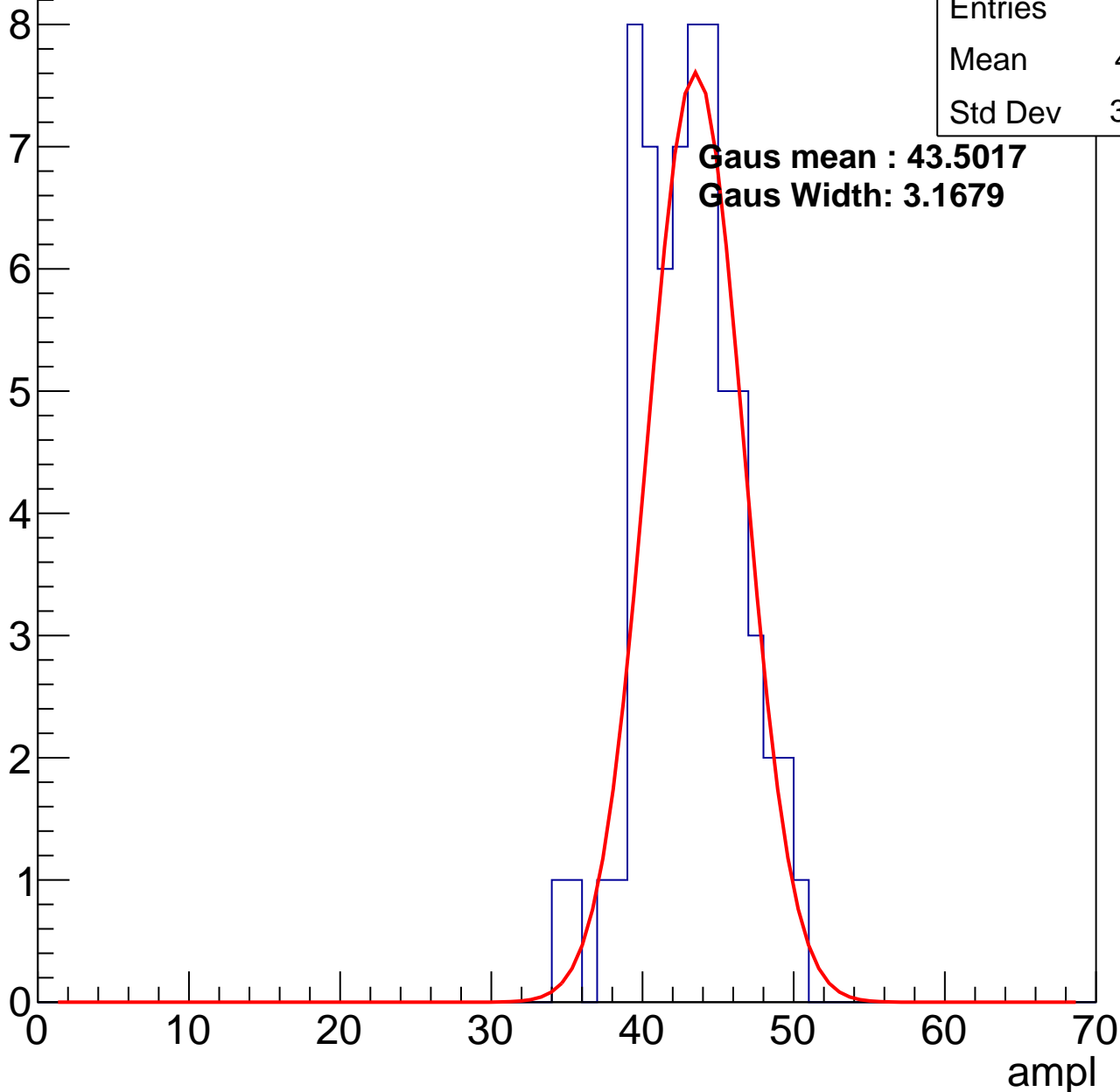
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	66
Mean	42.61
Std Dev	3.279

**Gaus mean : 43.5017**

**Gaus Width: 3.1679**

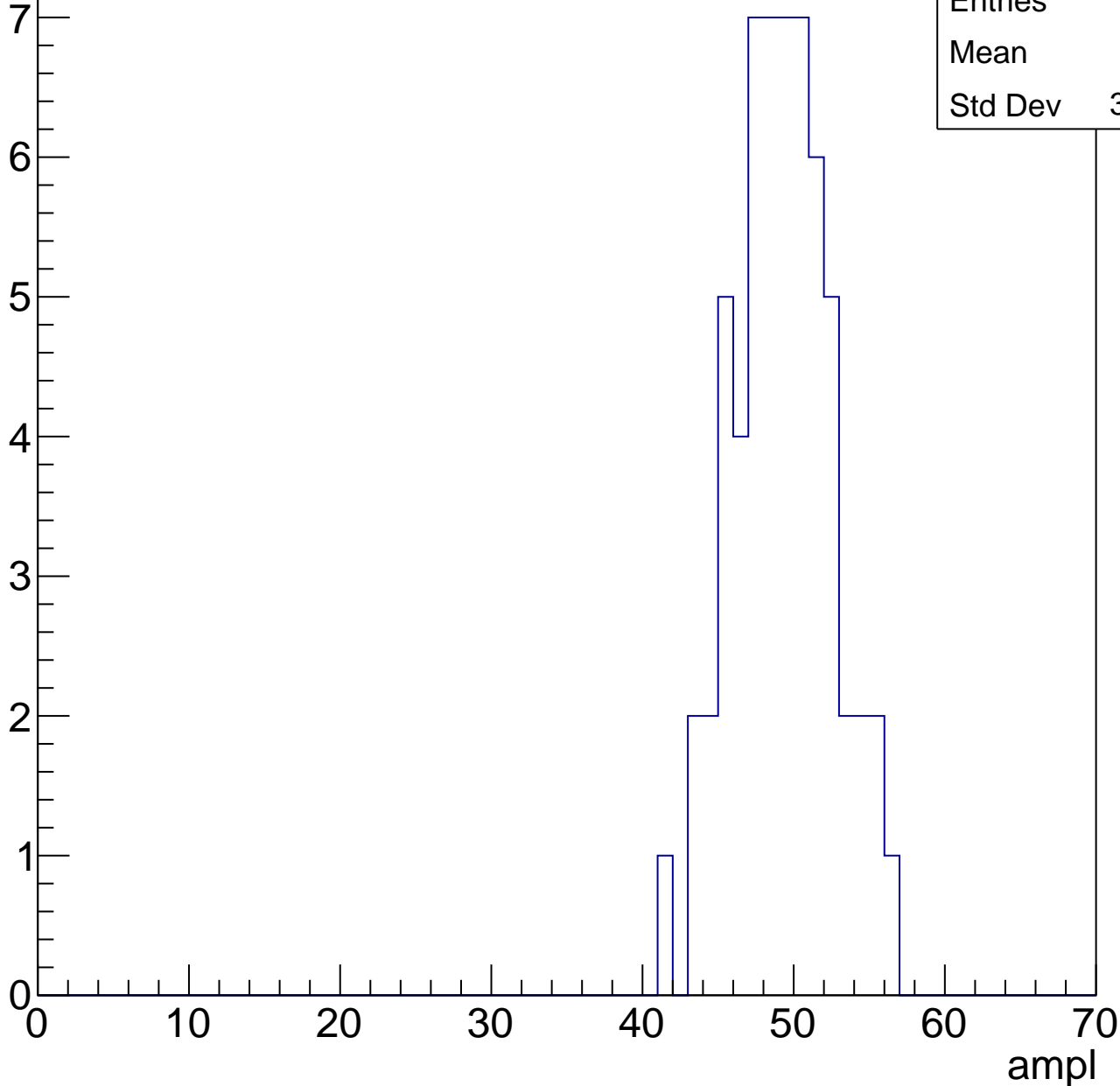


# B1L100S, U2-ch21, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	60
Mean	48.8
Std Dev	3.198

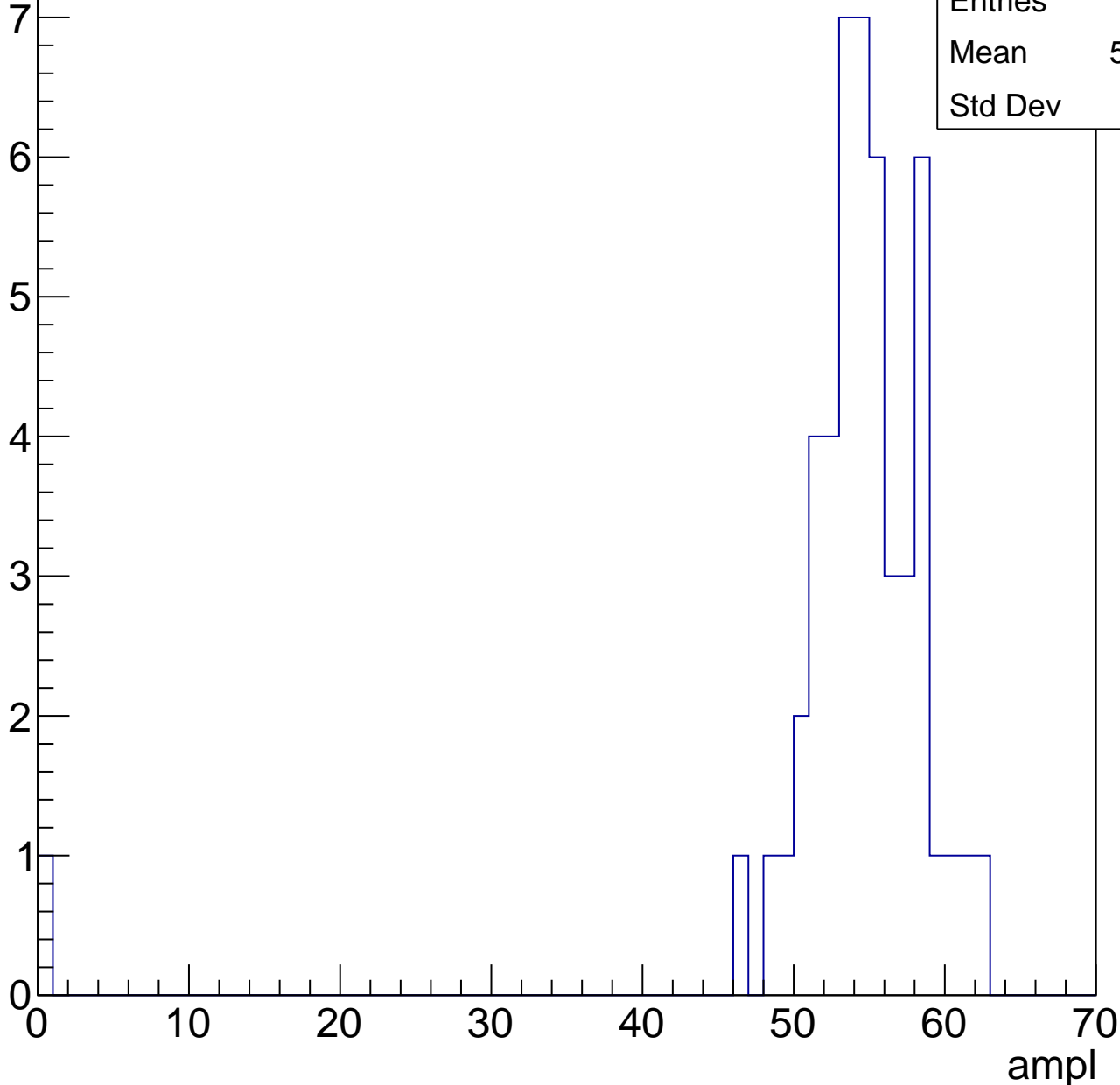


# B1L100S, U2-ch21, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	50
Mean	53.26
Std Dev	8.27



# B1L100S, U2-ch21, adc5

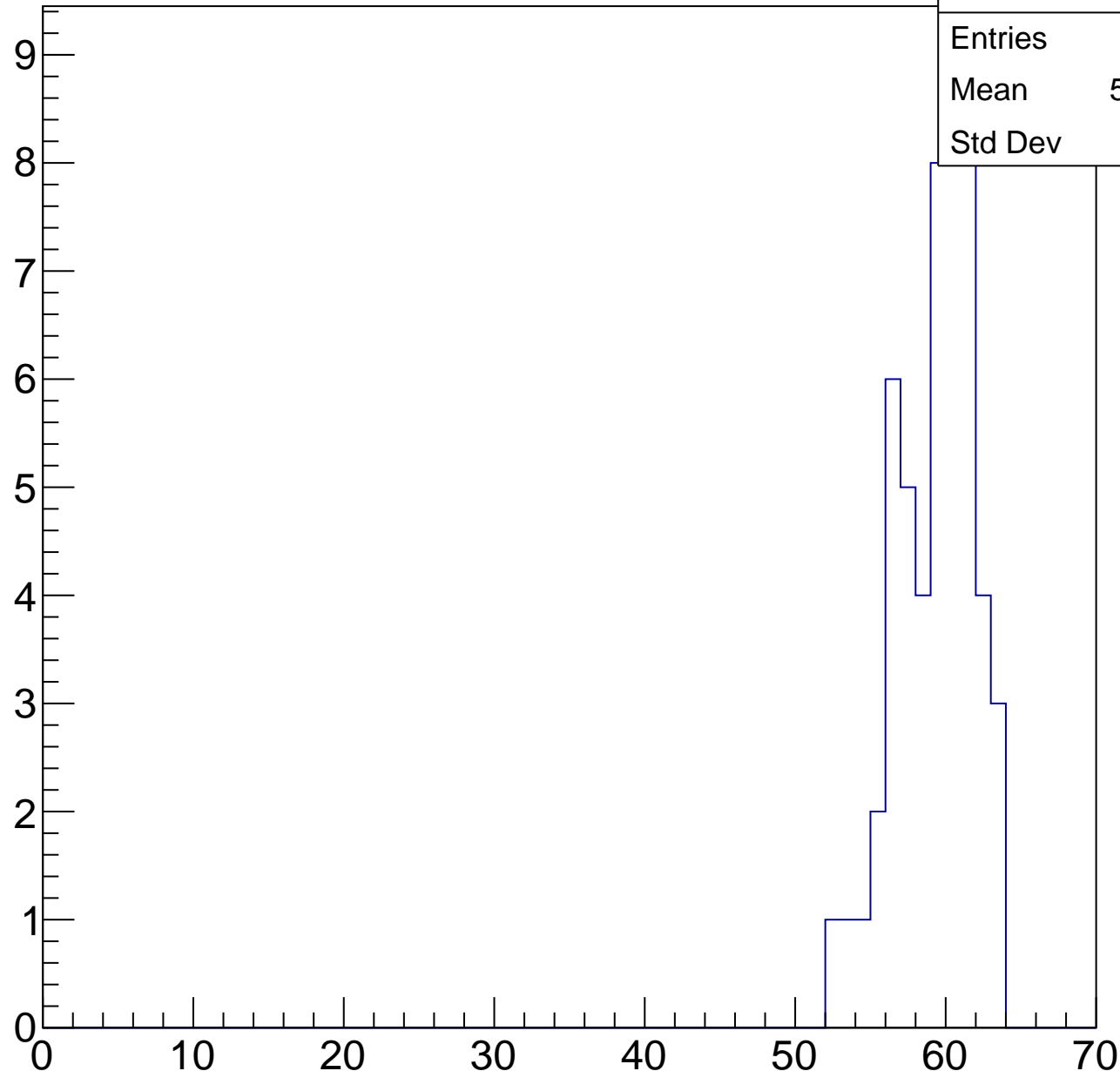
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	52
Mean	58.83
Std Dev	2.57

ampl

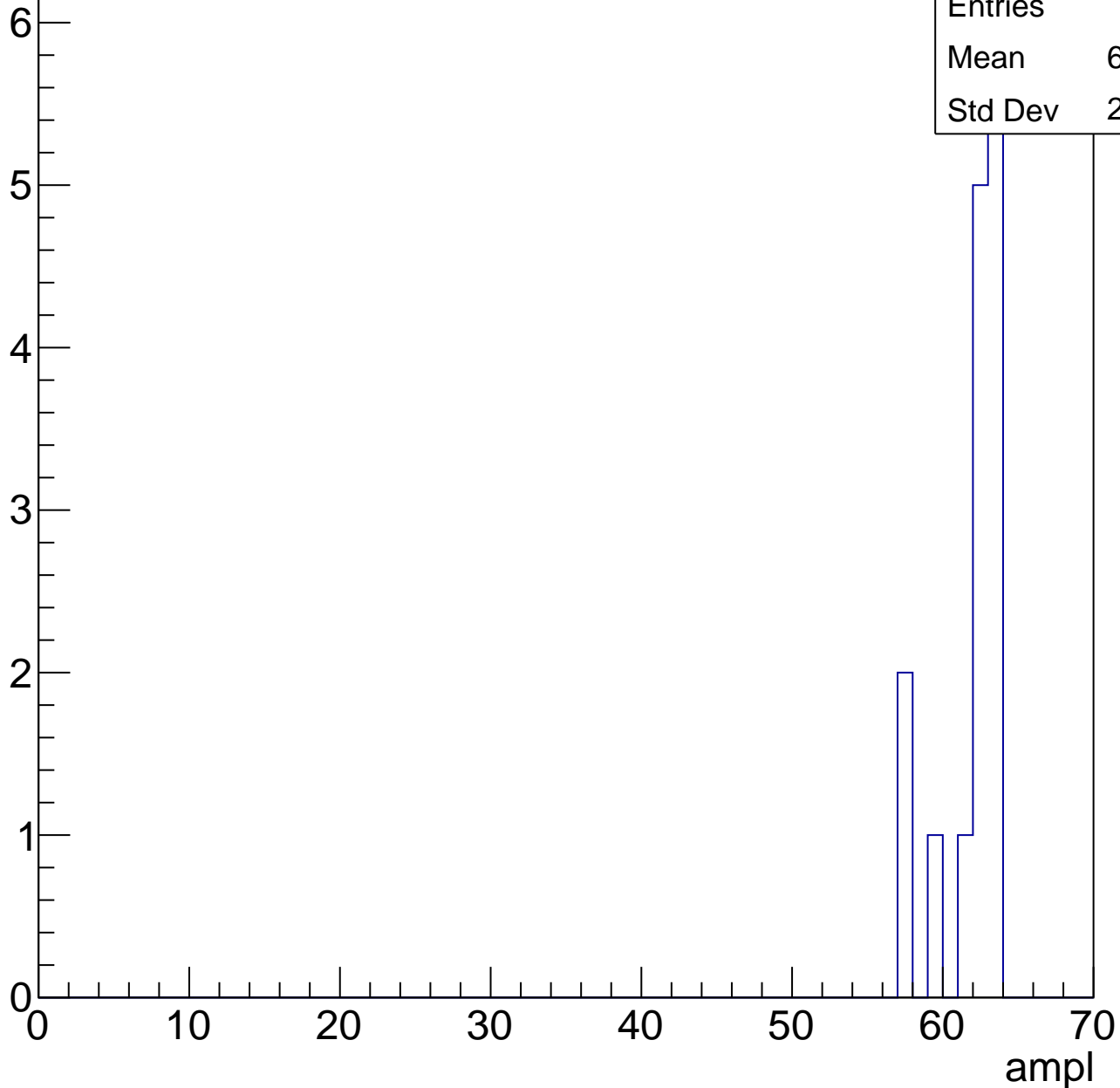


# B1L100S, U2-ch21, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	15
Mean	61.47
Std Dev	2.029





# B1L100S, U2-ch21, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



# B1L100S, U2-ch22, adc0

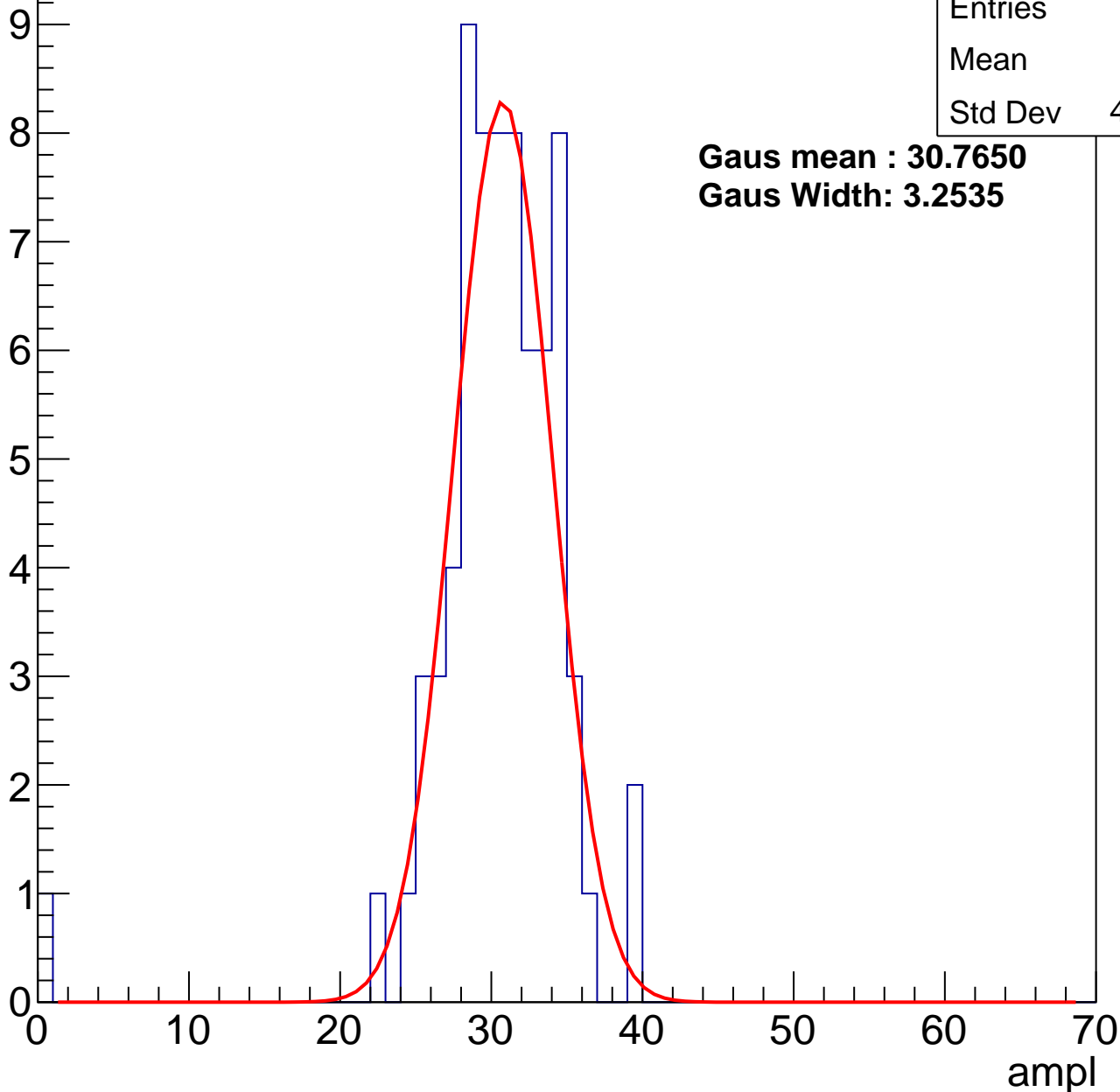
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	72
Mean	30
Std Dev	4.845

**Gaus mean : 30.7650**

**Gaus Width: 3.2535**



# B1L100S, U2-ch22, adc1

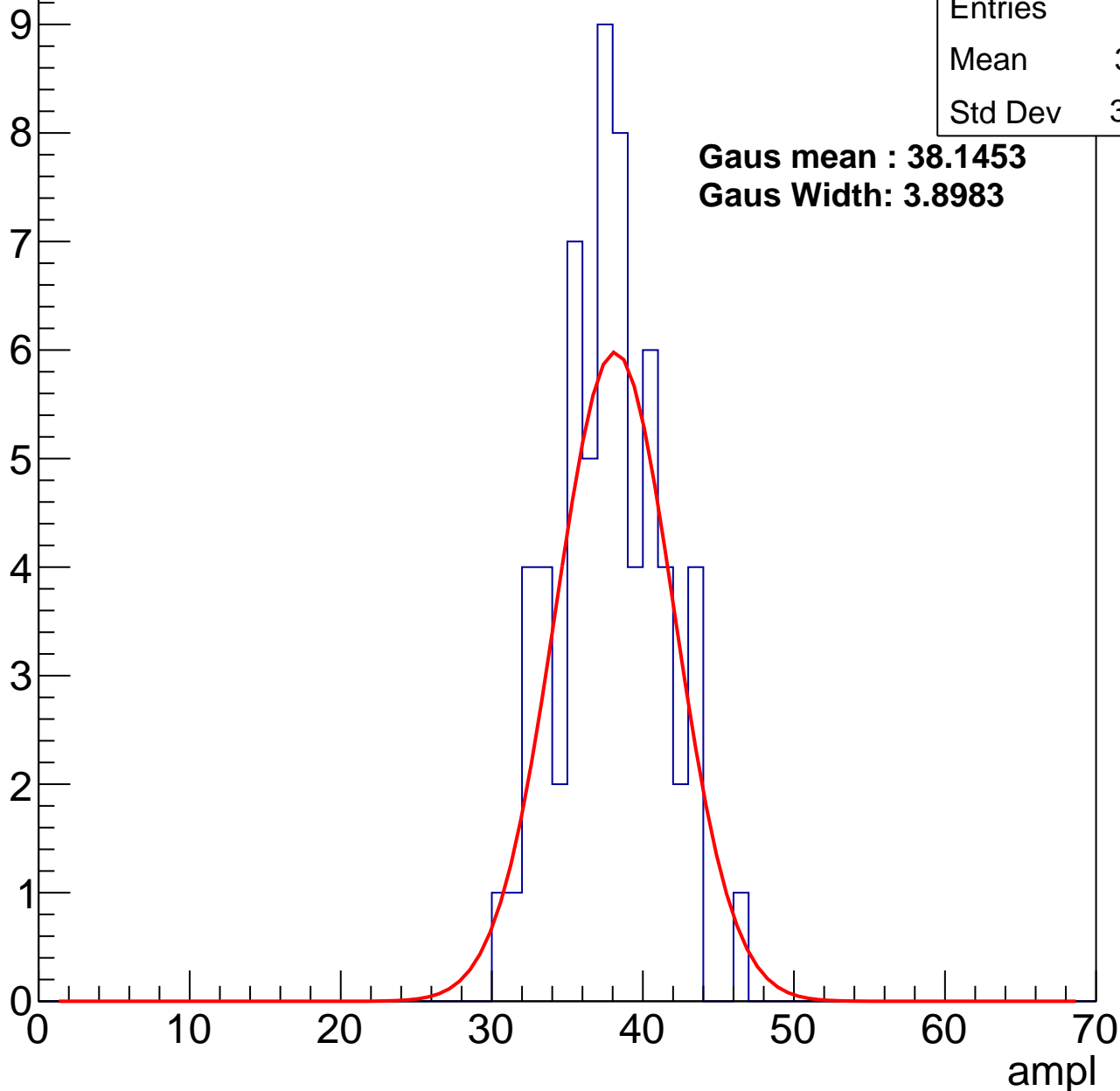
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	62
Mean	37.31
Std Dev	3.387

**Gaus mean : 38.1453**

**Gaus Width: 3.8983**



# B1L100S, U2-ch22, adc2

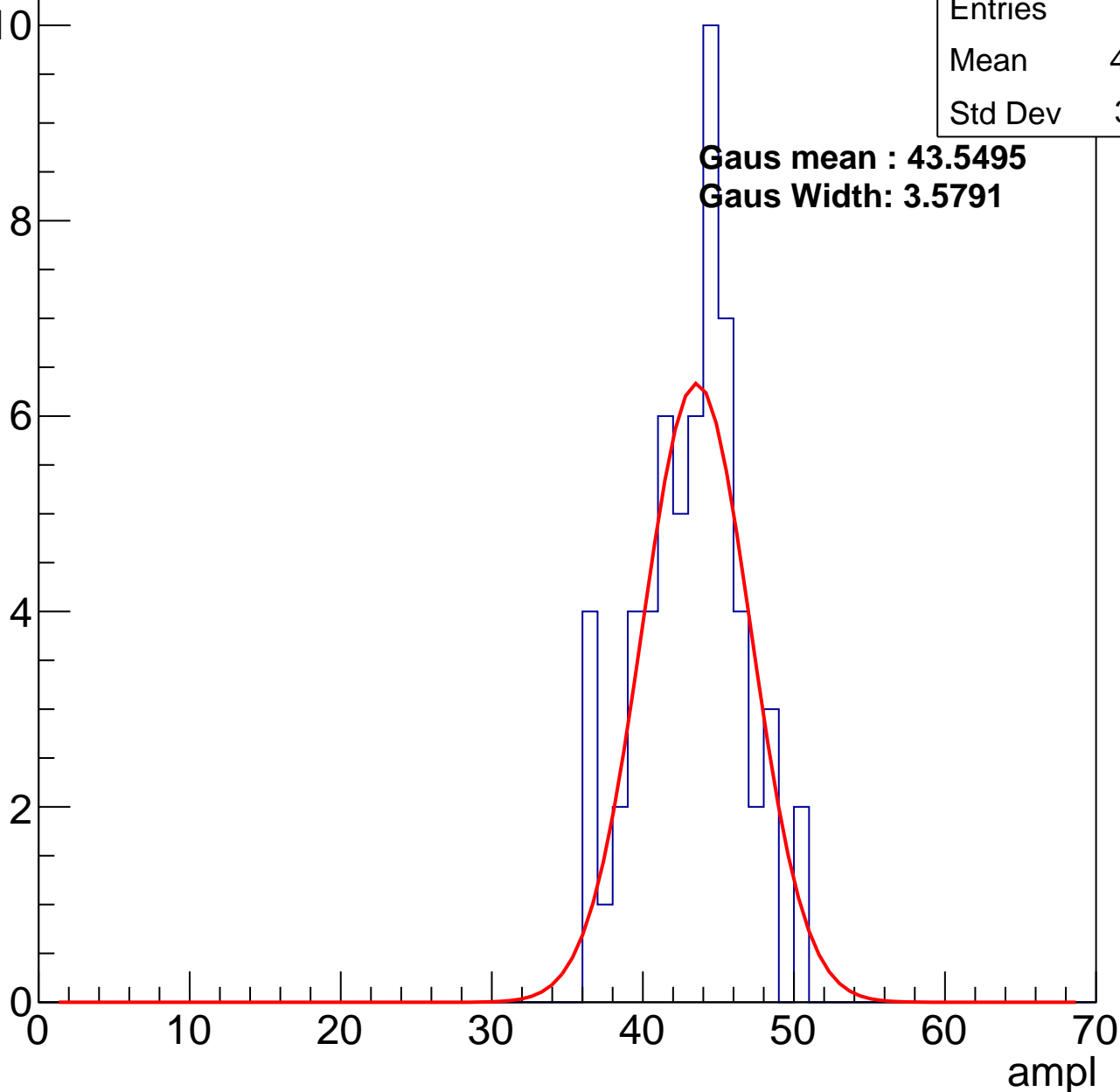
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	60
Mean	42.73
Std Dev	3.381

**Gaus mean : 43.5495**

**Gaus Width: 3.5791**

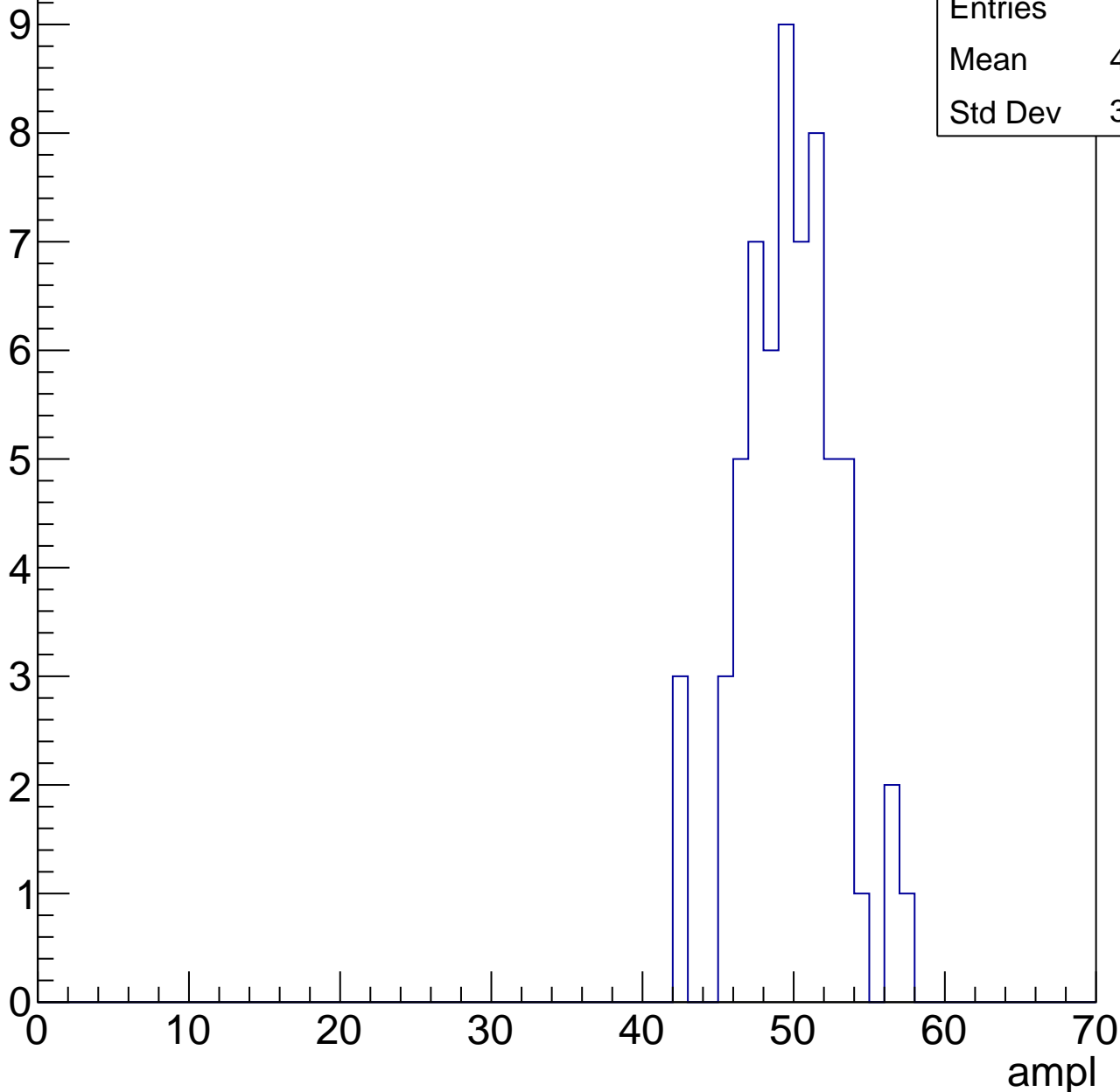


# B1L100S, U2-ch22, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	62
Mean	49.27
Std Dev	3.163

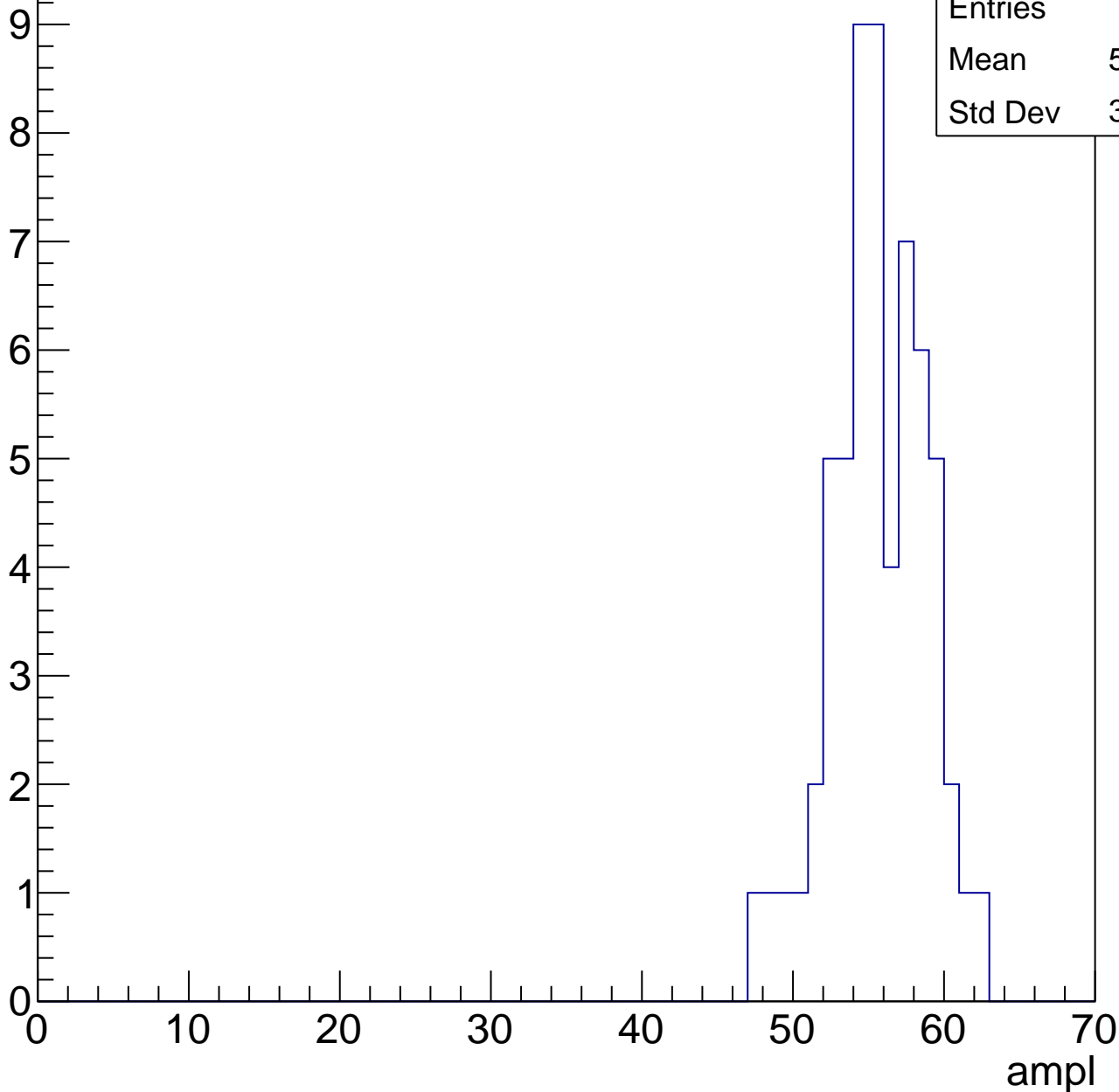


# B1L100S, U2-ch22, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	60
Mean	55.18
Std Dev	3.106



# B1L100S, U2-ch22, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	41
Mean	58.29
Std Dev	9.459

ampl

0

10

20

30

40

50

60

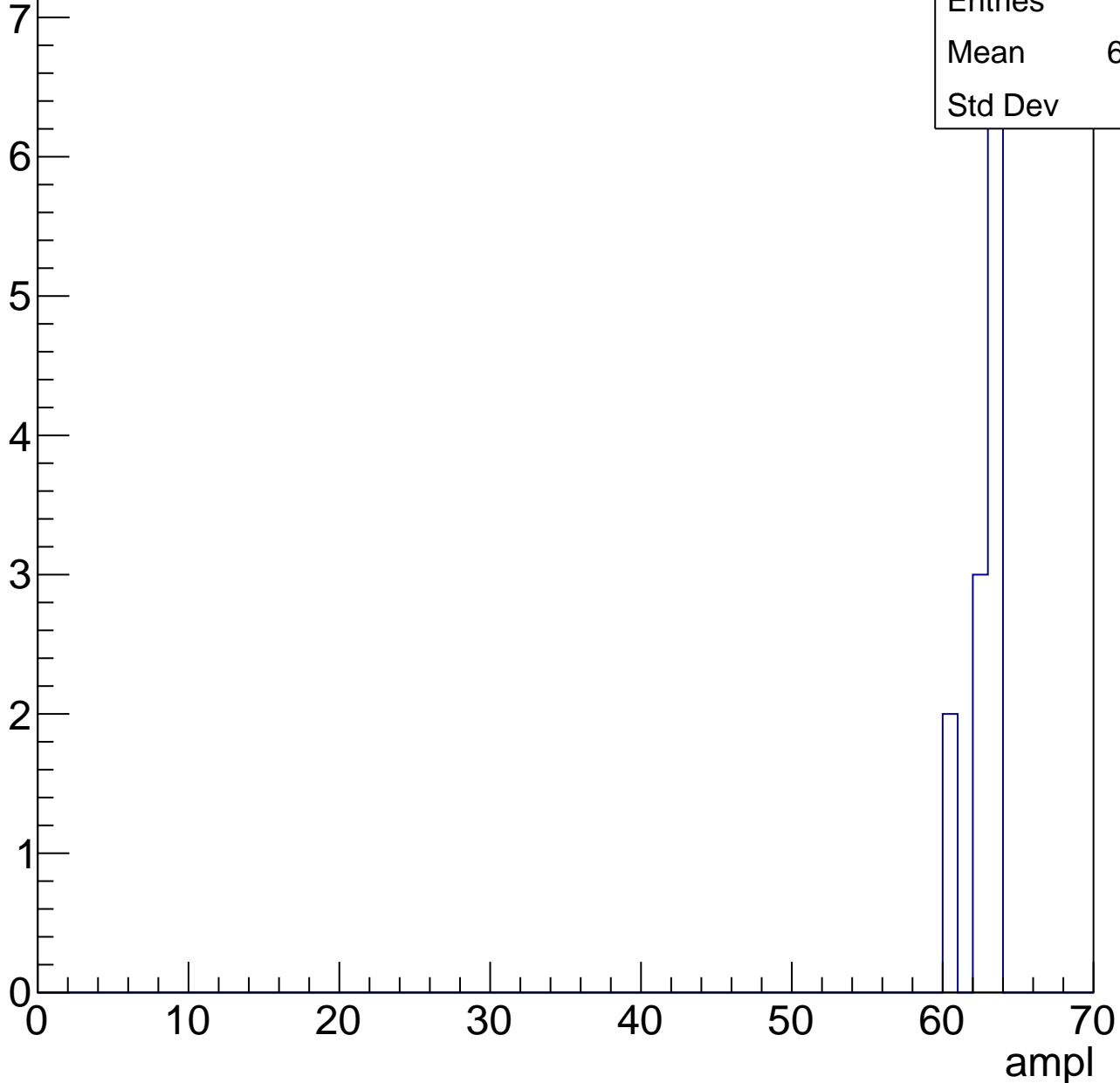
70

# B1L100S, U2-ch22, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	12
Mean	62.25
Std Dev	1.09





# B1L100S, U2-ch22, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L100S, U2-ch23, adc0

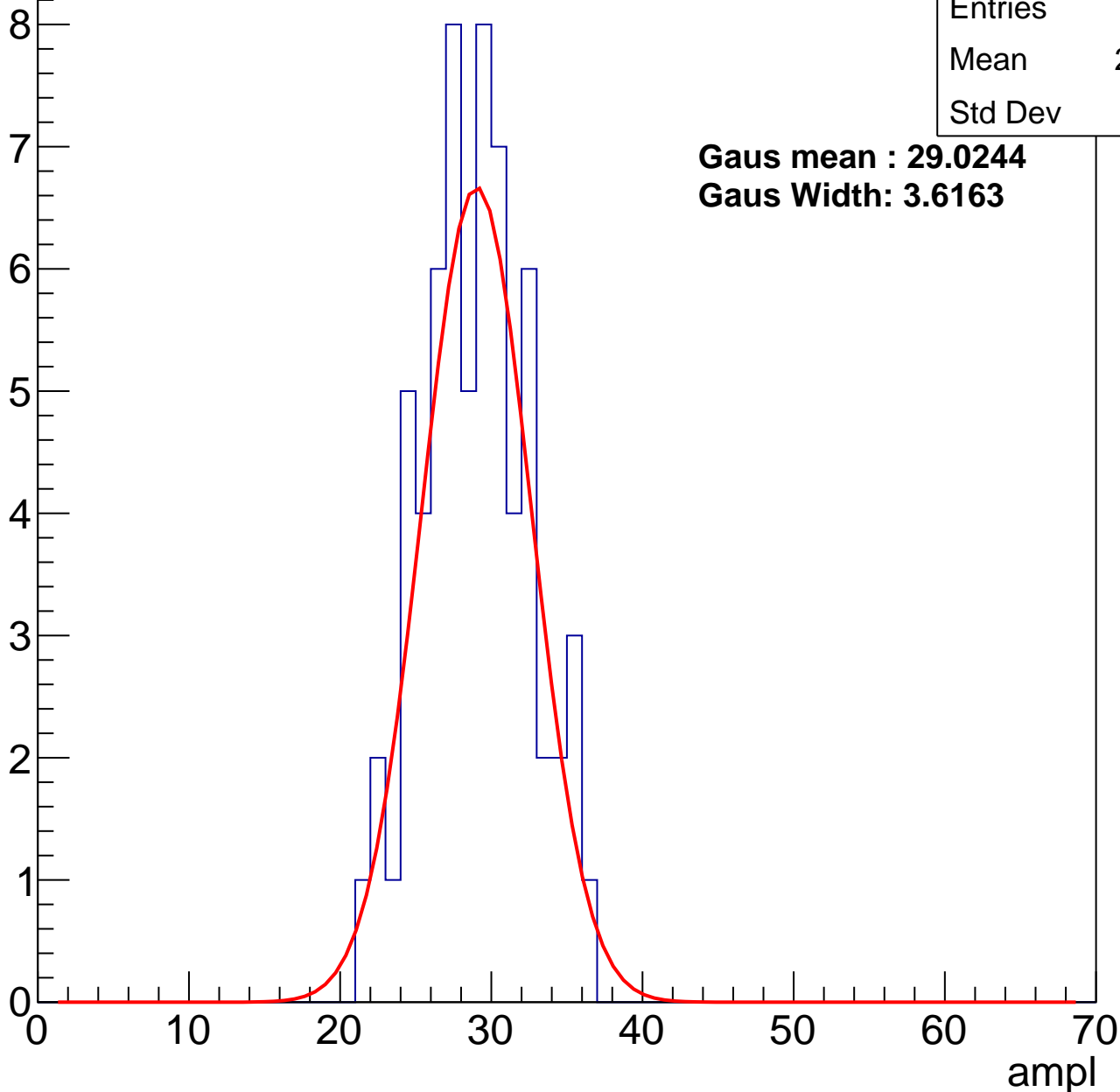
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	65
Mean	28.51
Std Dev	3.46

**Gaus mean : 29.0244**

**Gaus Width: 3.6163**



# B1L100S, U2-ch23, adc1

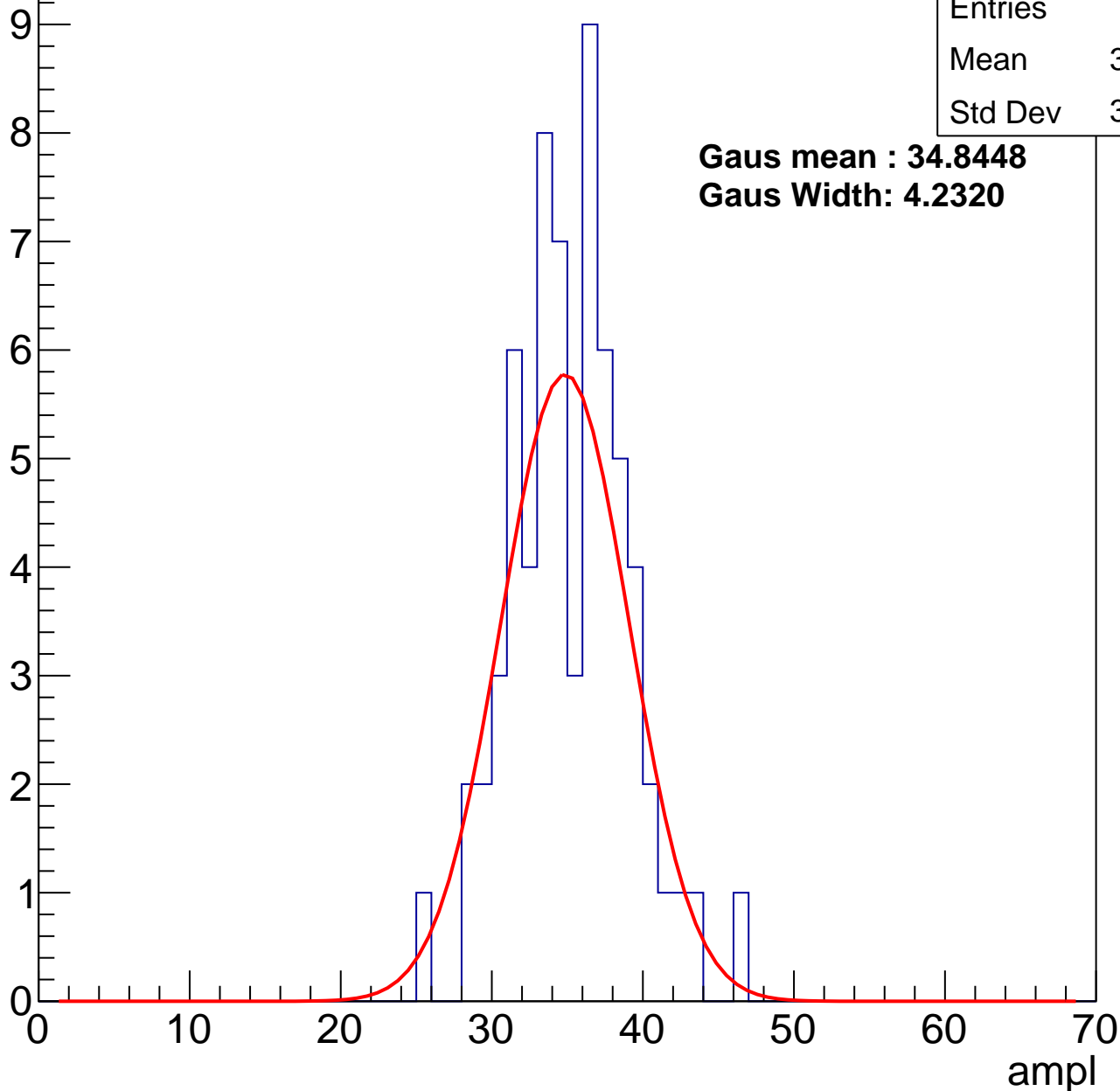
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	66
Mean	34.76
Std Dev	3.842

**Gaus mean : 34.8448**

**Gaus Width: 4.2320**



# B1L100S, U2-ch23, adc2

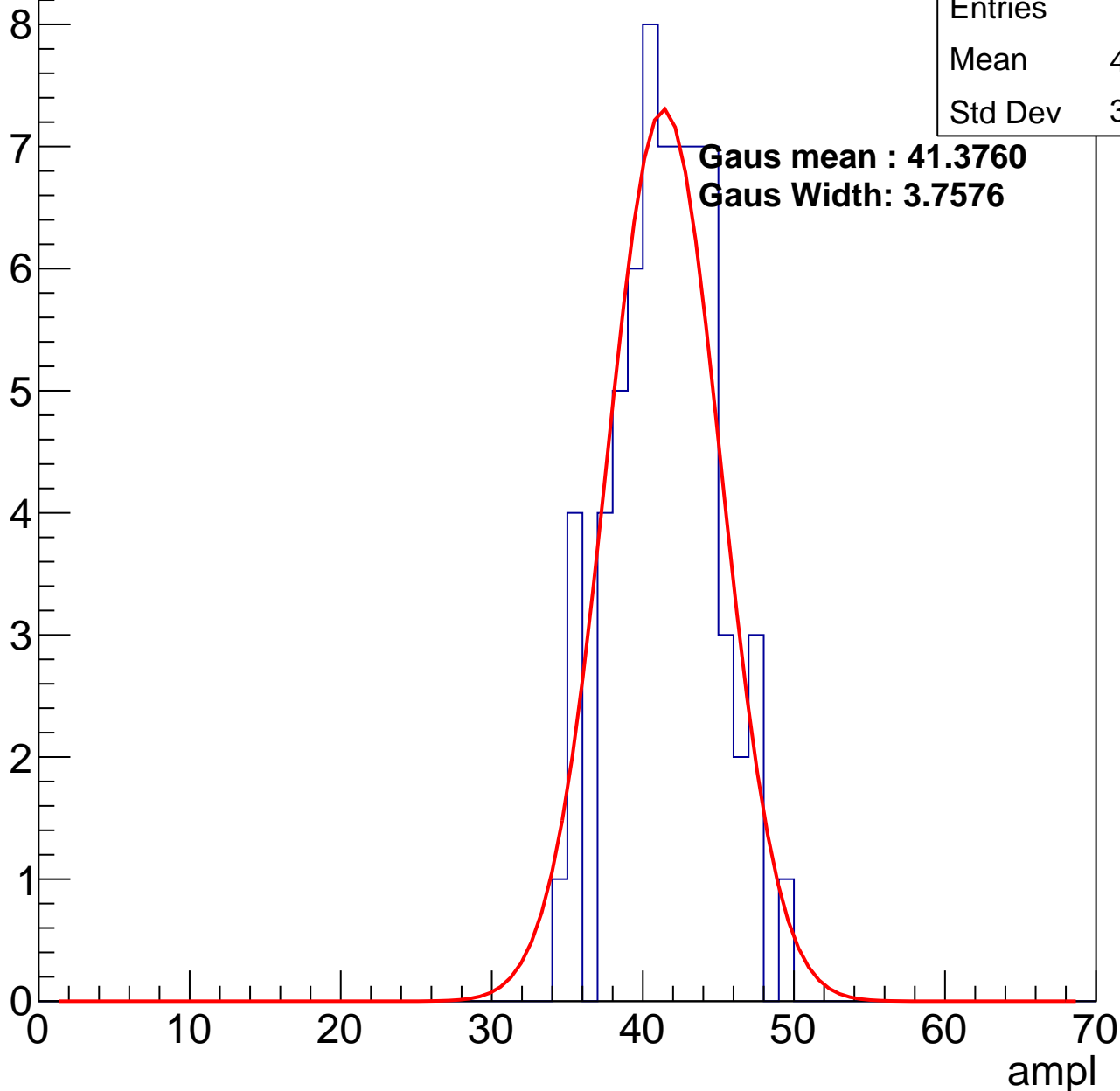
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	65
Mean	41.12
Std Dev	3.284

**Gaus mean : 41.3760**

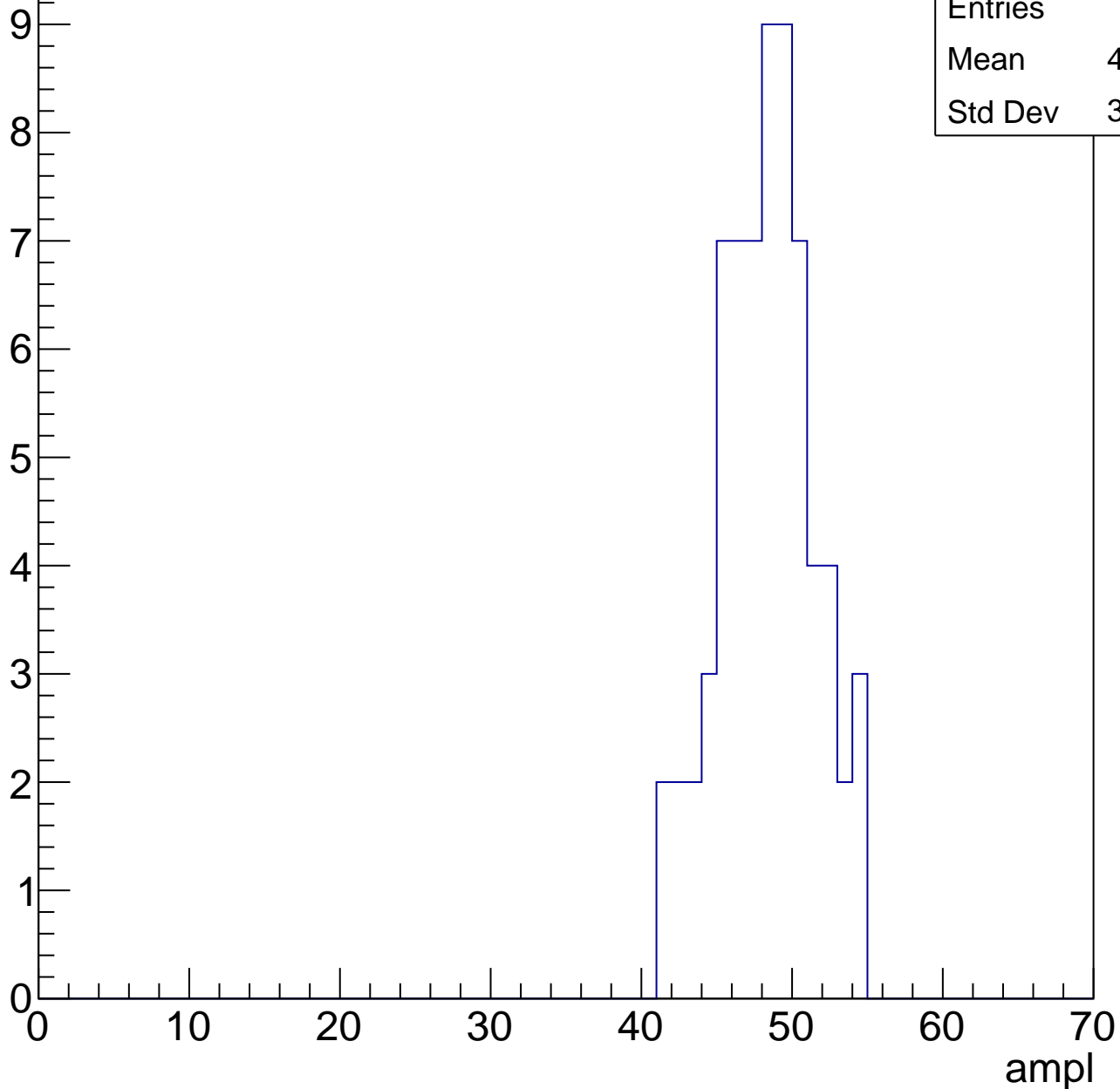
**Gaus Width: 3.7576**



# B1L100S, U2-ch23, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

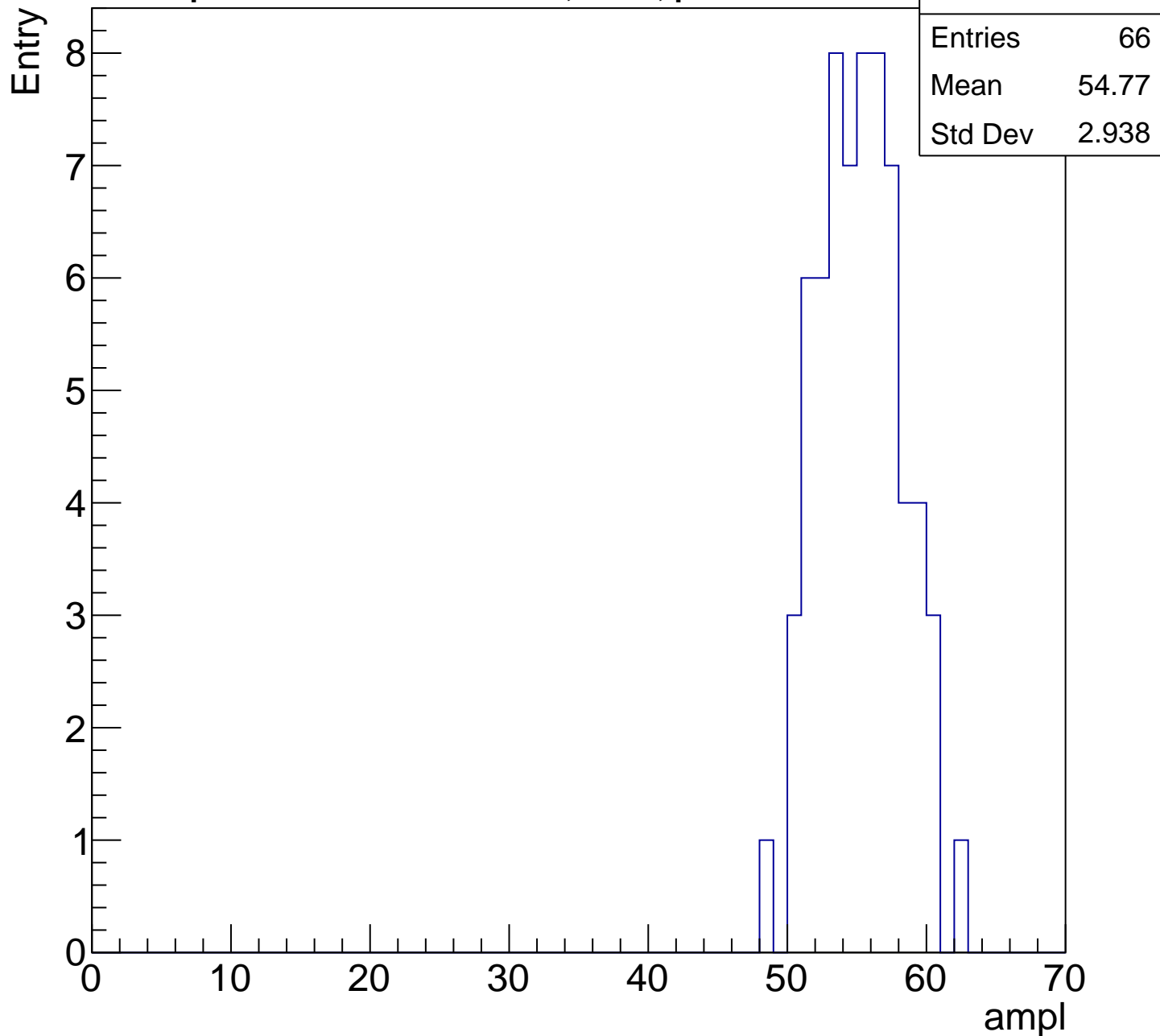
Entry



Entries	68
Mean	47.84
Std Dev	3.114

# B1L100S, U2-ch23, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2



# B1L100S, U2-ch23, adc5

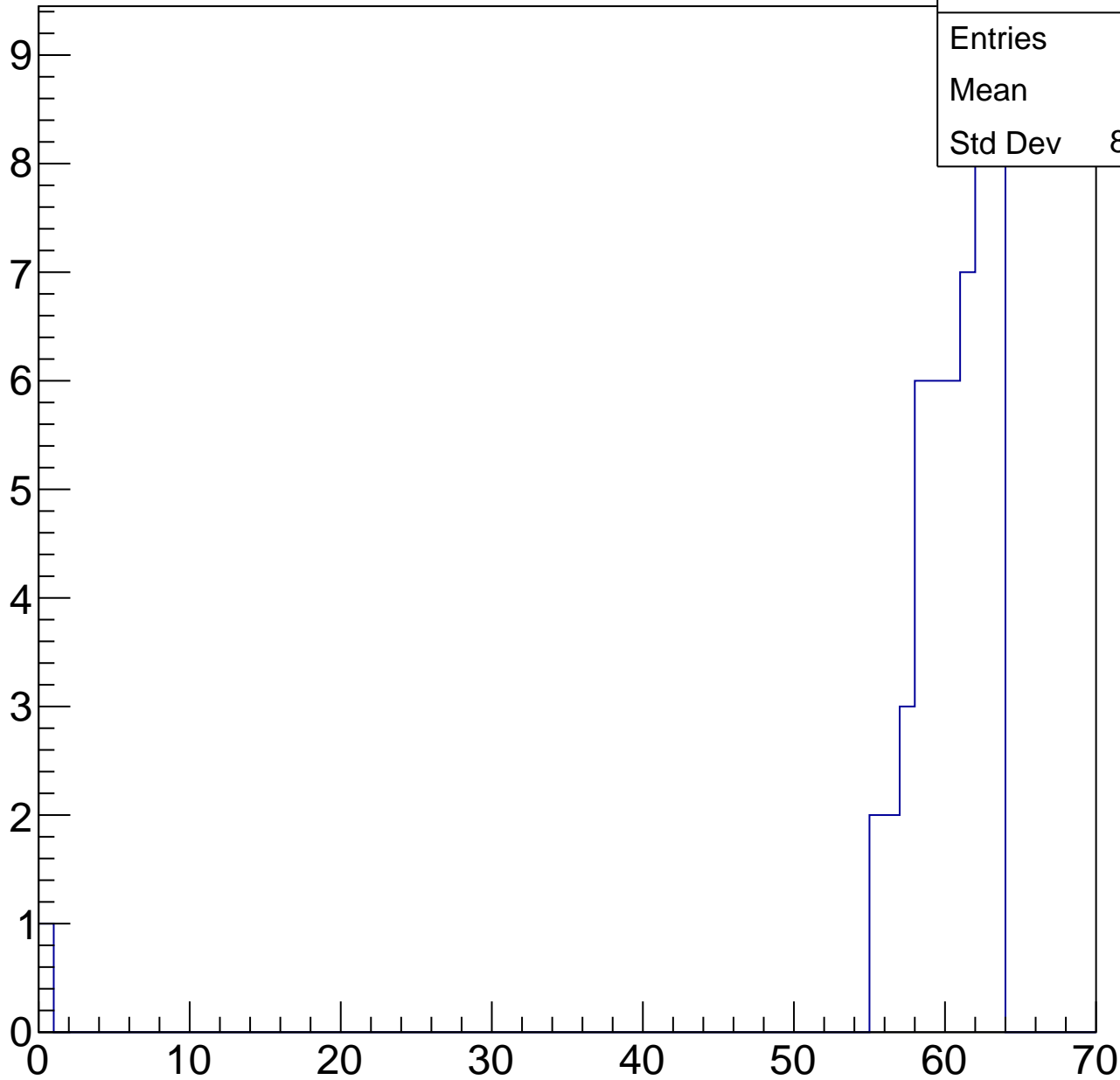
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	50
Mean	58.9
Std Dev	8.716

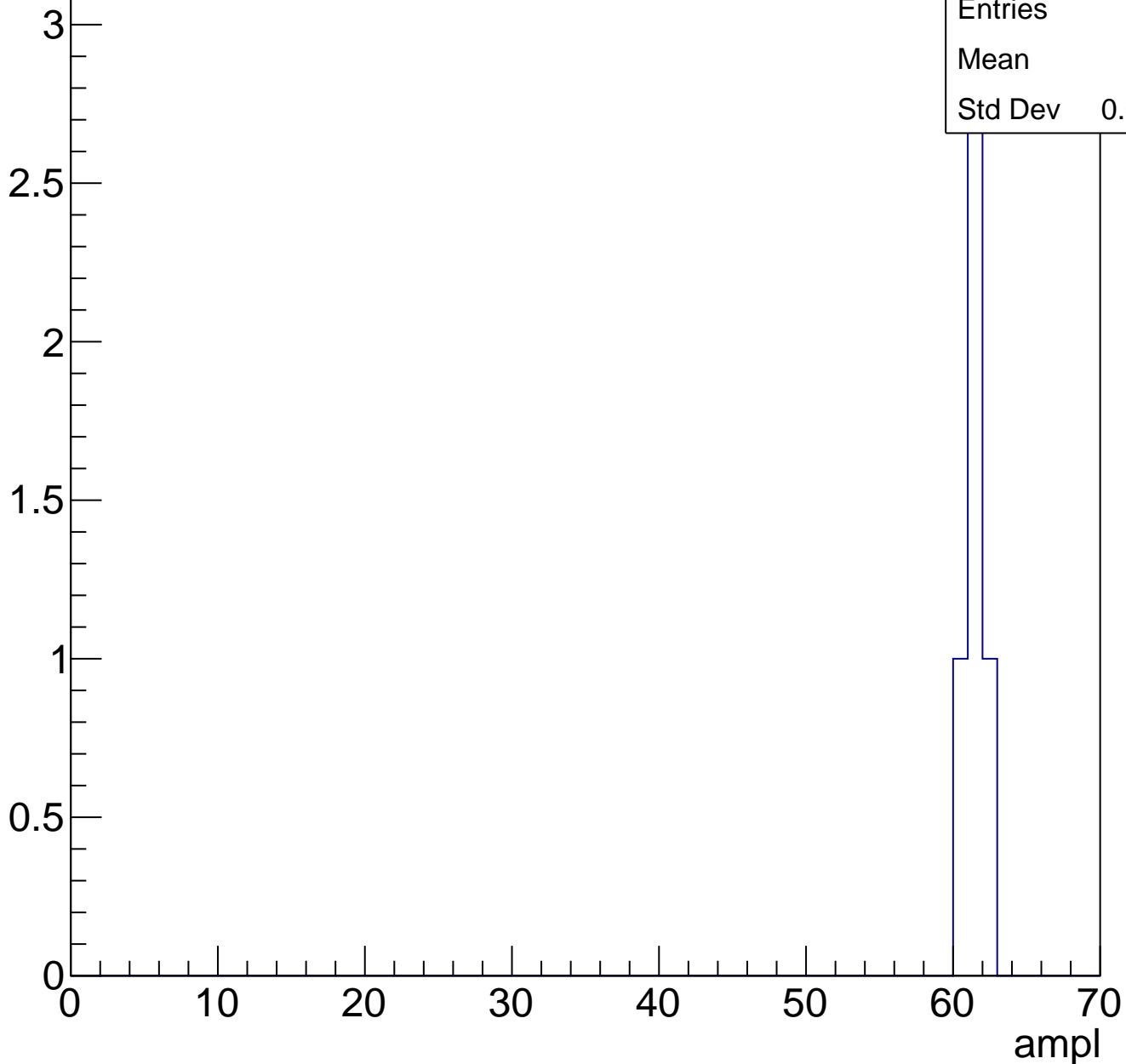
ampl



# B1L100S, U2-ch23, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry





# B1L100S, U2-ch23, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



# B1L100S, U2-ch24, adc0

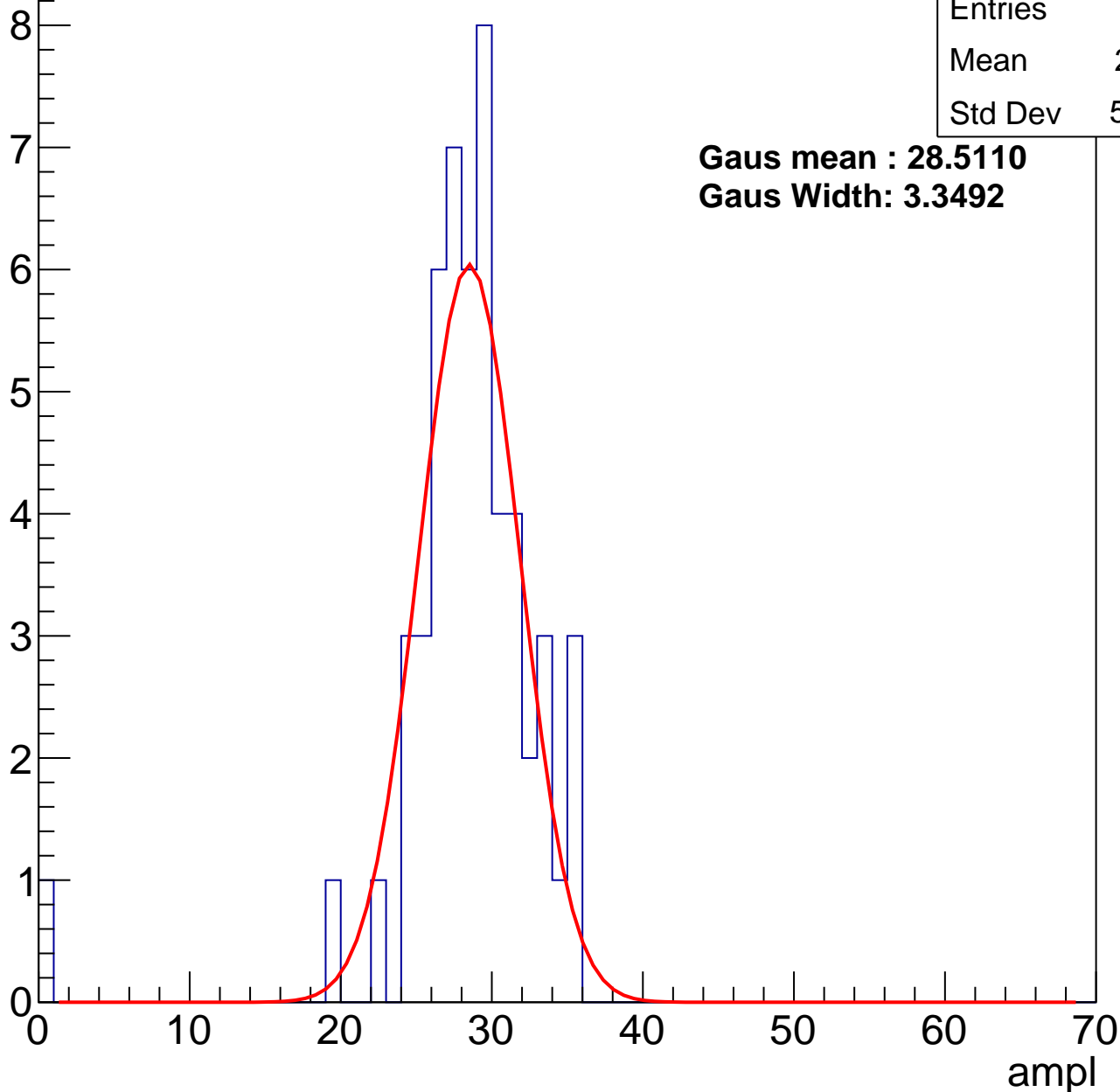
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	53
Mean	27.91
Std Dev	5.059

**Gaus mean : 28.5110**

**Gaus Width: 3.3492**



# B1L100S, U2-ch24, adc1

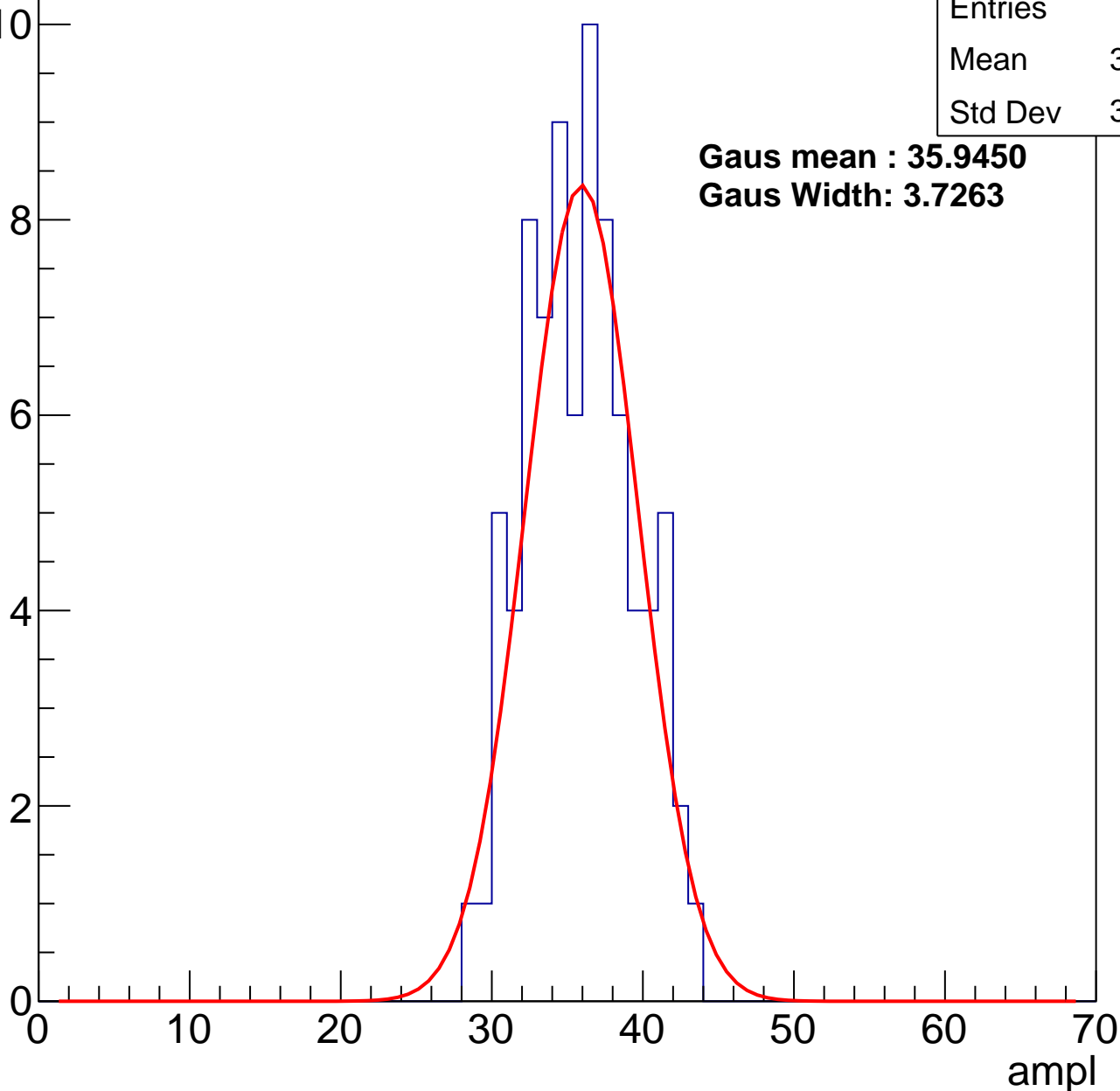
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	81
Mean	35.38
Std Dev	3.466

**Gaus mean : 35.9450**

**Gaus Width: 3.7263**



# B1L100S, U2-ch24, adc2

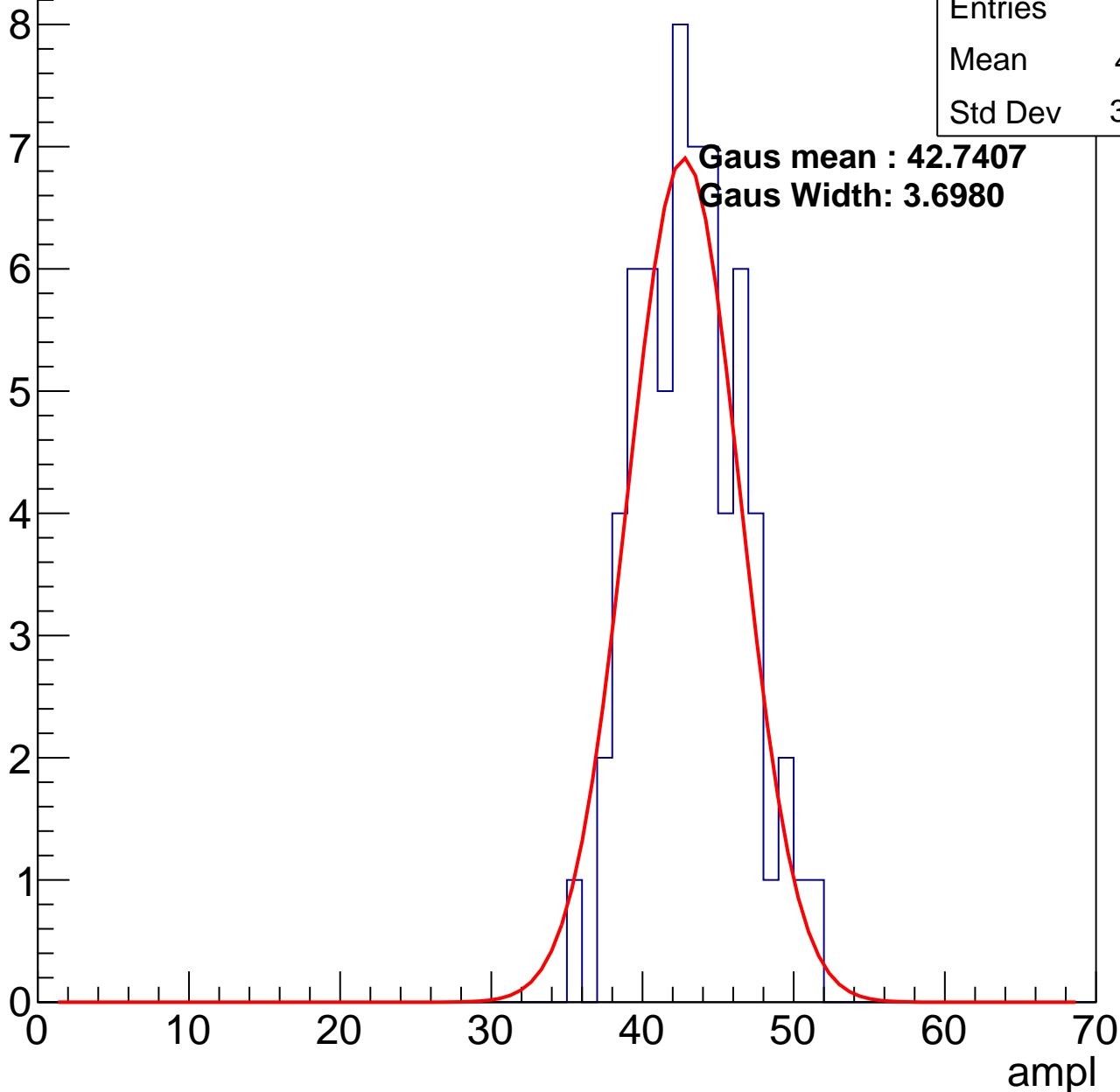
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	65
Mean	42.71
Std Dev	3.418

**Gaus mean : 42.7407**

**Gaus Width: 3.6980**

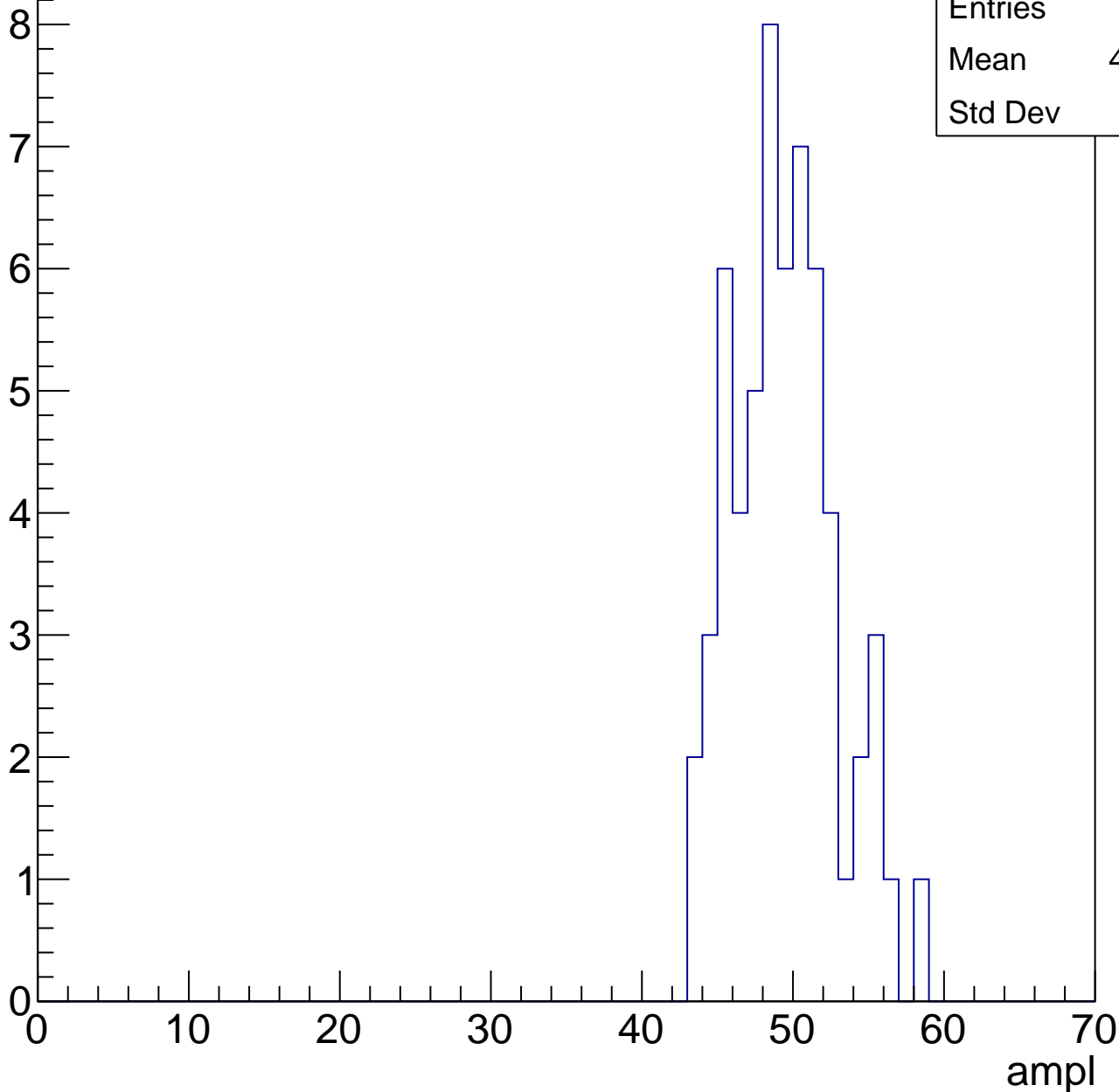


# B1L100S, U2-ch24, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	59
Mean	48.97
Std Dev	3.39

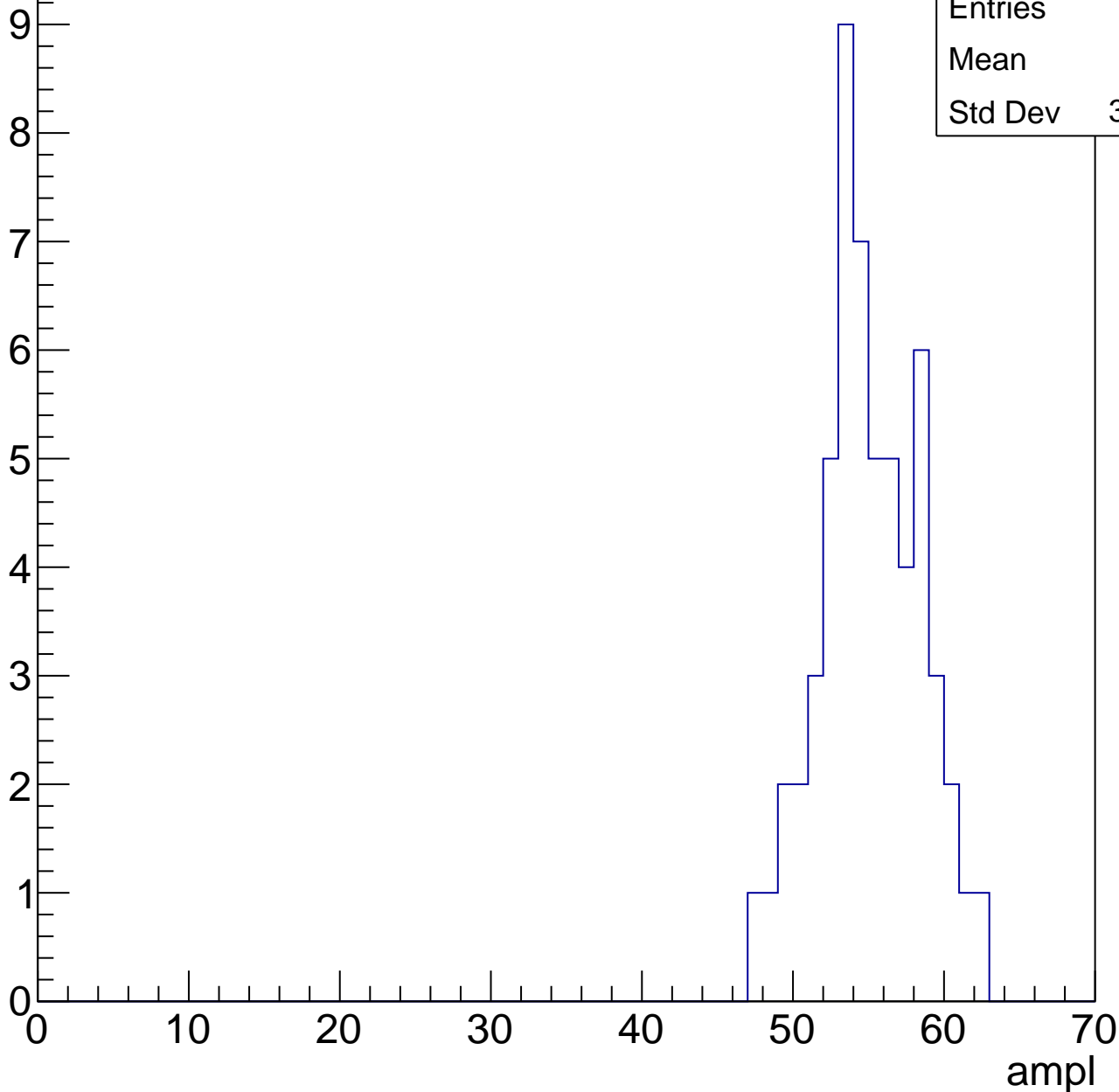


# B1L100S, U2-ch24, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	57
Mean	54.6
Std Dev	3.297



# B1L100S, U2-ch24, adc5

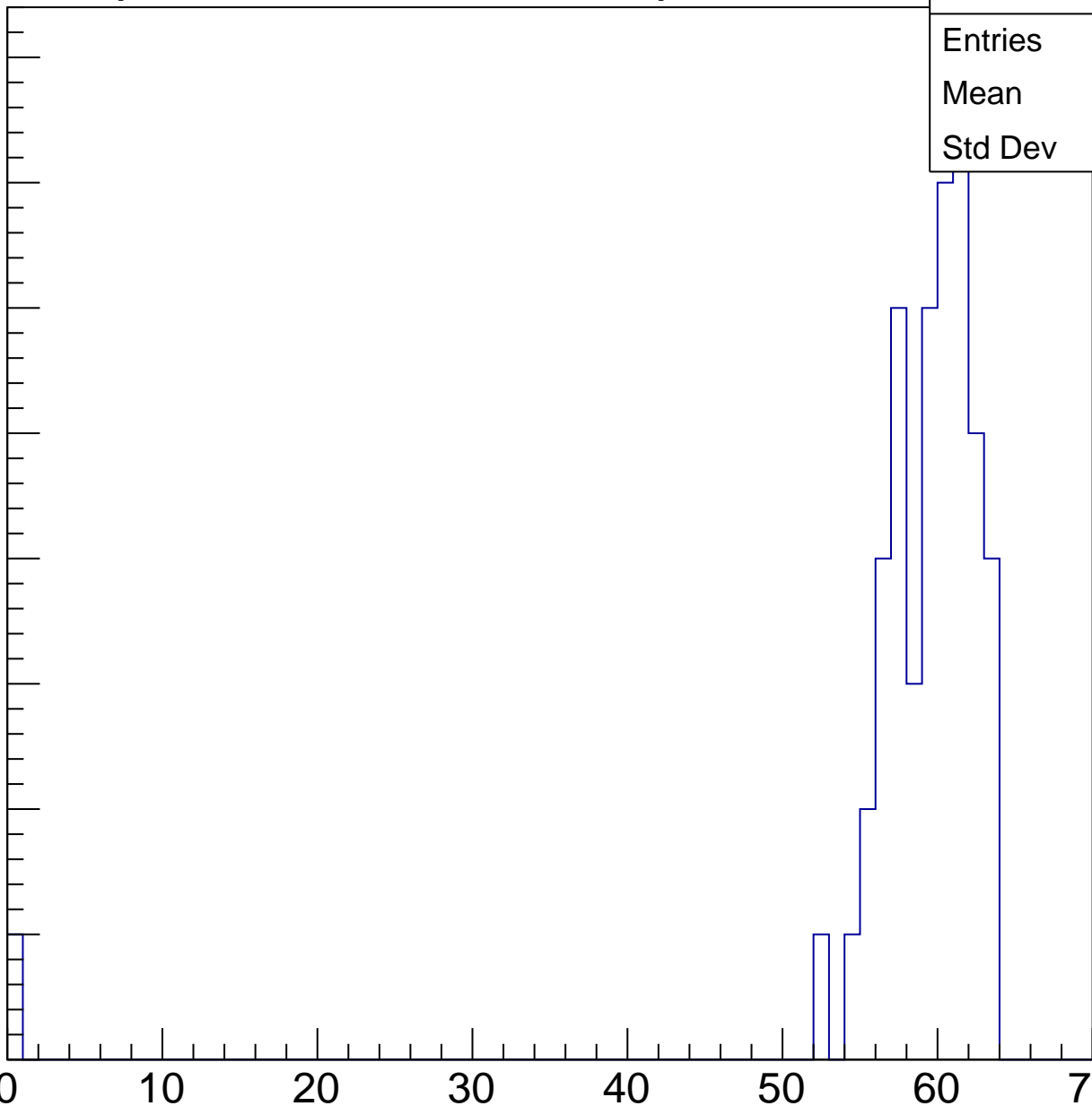
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	48
Mean	57.92
Std Dev	8.829

ampl



# B1L100S, U2-ch24, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

6

5

4

3

2

1

0

0

10

20

30

40

50

60

70

ampl

Entries

13

Mean

62

Std Dev

1.24

0



# B1L100S, U2-ch24, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L100S, U2-ch25, adc0

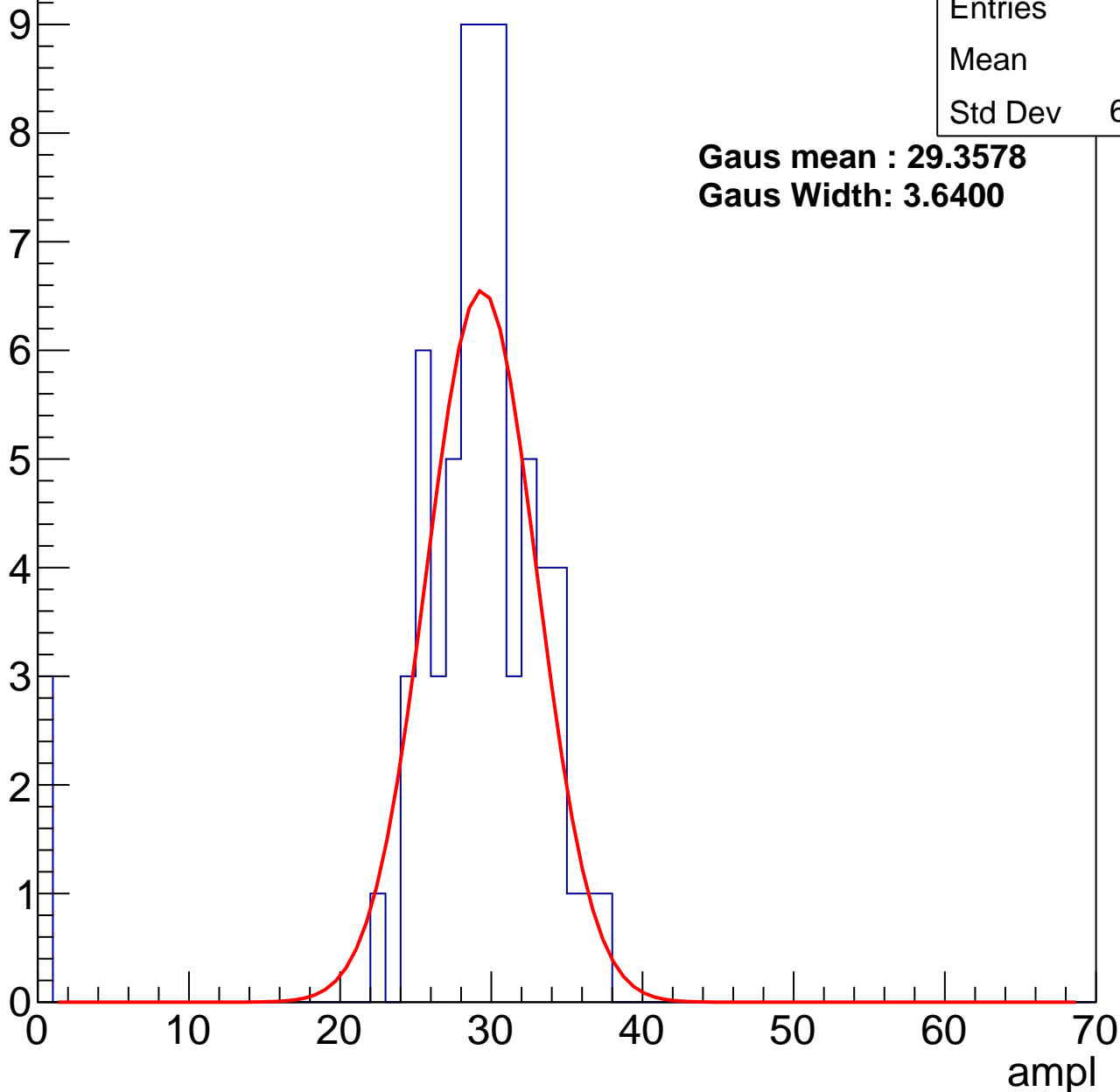
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	67
Mean	27.9
Std Dev	6.798

**Gaus mean : 29.3578**

**Gaus Width: 3.6400**



# B1L100S, U2-ch25, adc1

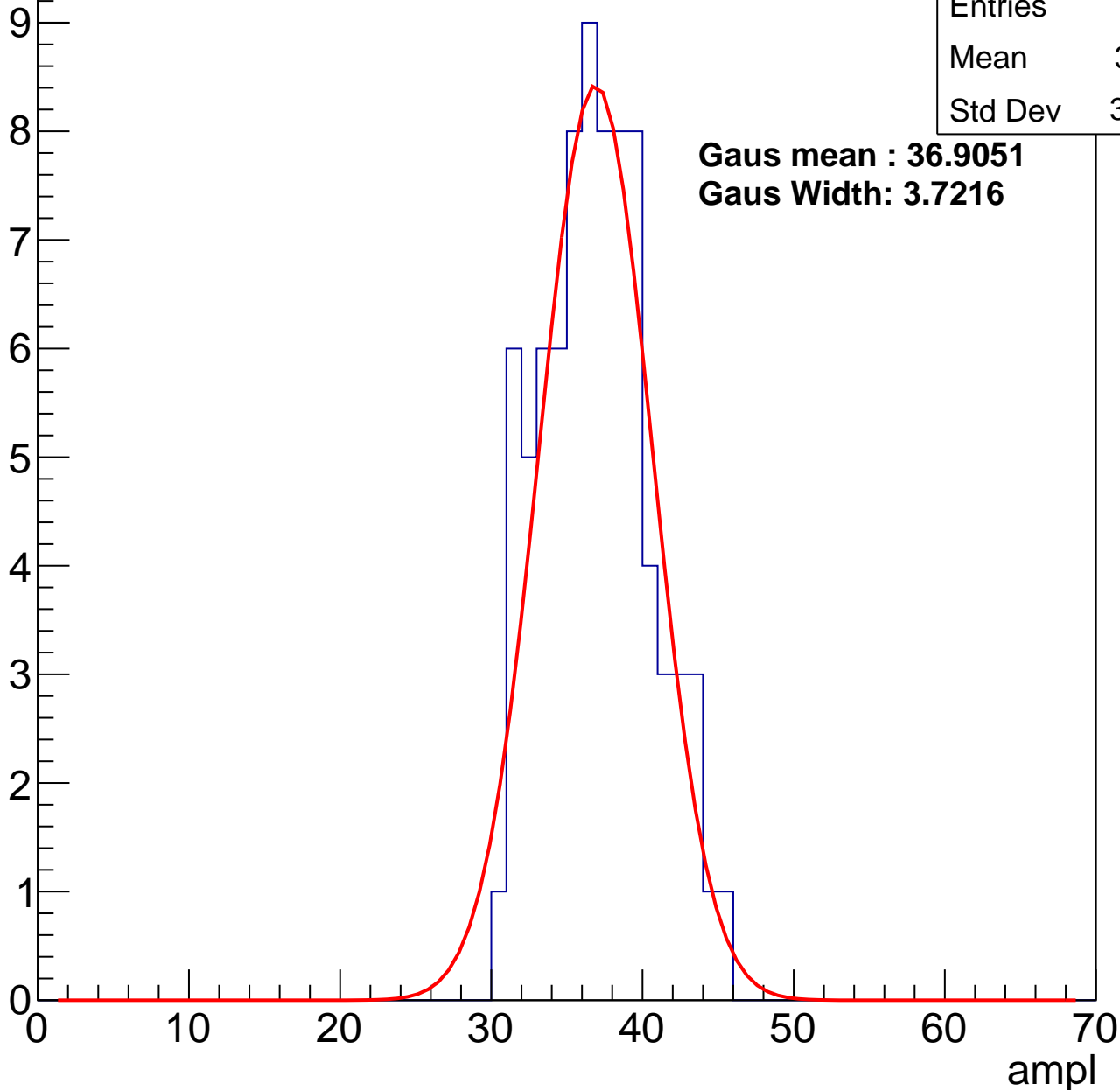
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	80
Mean	36.51
Std Dev	3.504

**Gaus mean : 36.9051**

**Gaus Width: 3.7216**



# B1L100S, U2-ch25, adc2

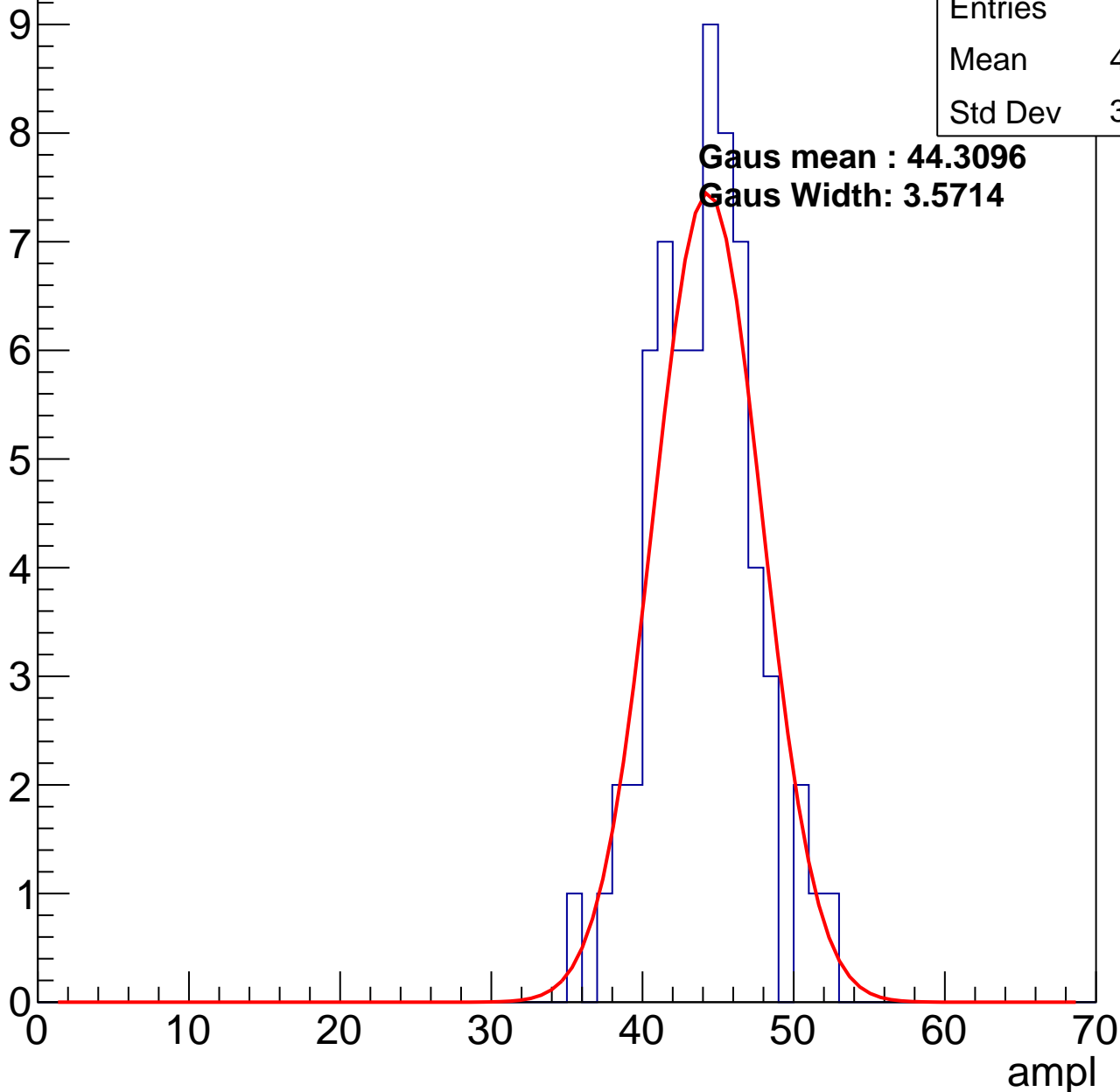
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	66
Mean	43.58
Std Dev	3.335

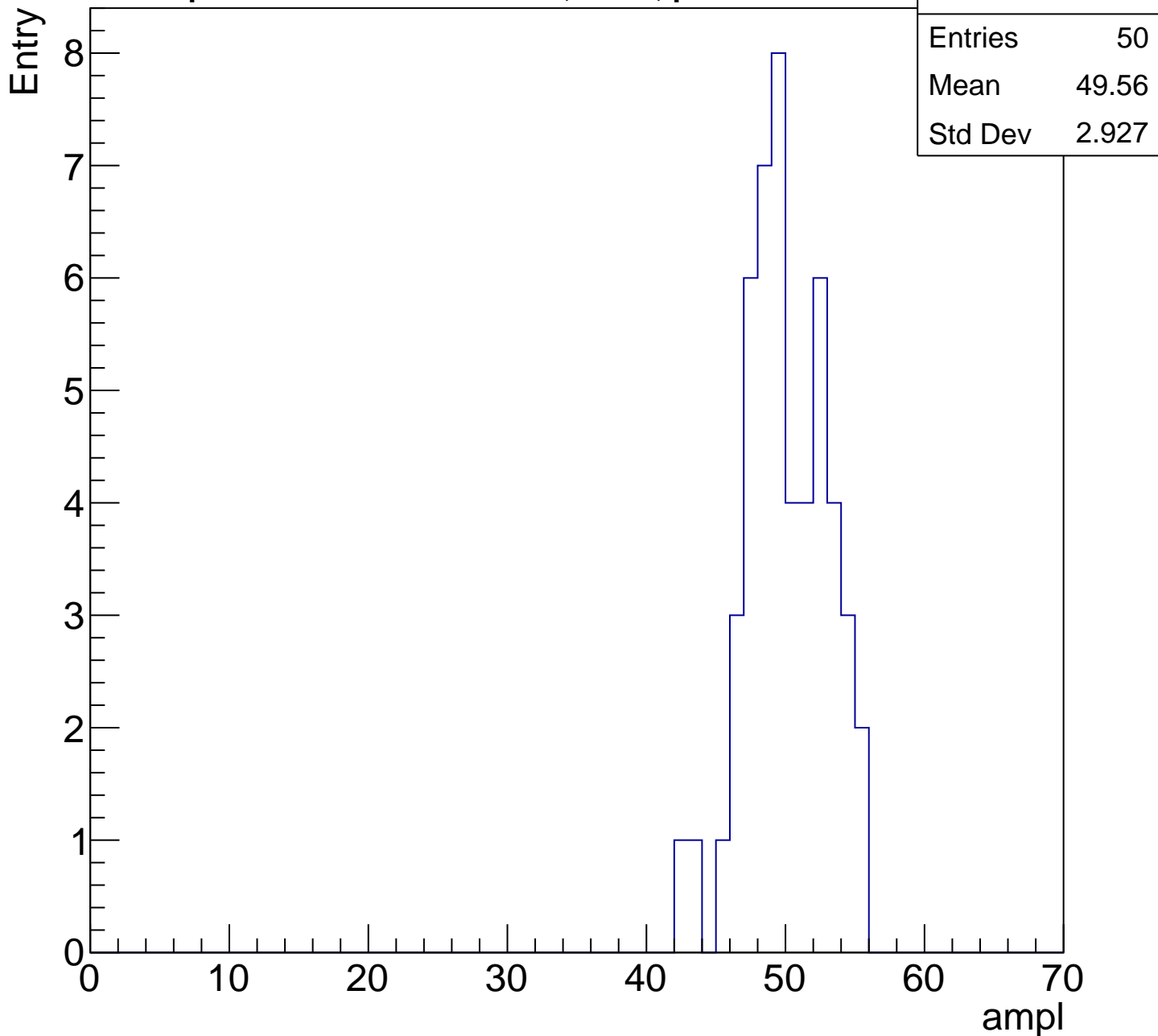
**Gaus mean : 44.3096**

**Gaus Width: 3.5714**



# B1L100S, U2-ch25, adc3

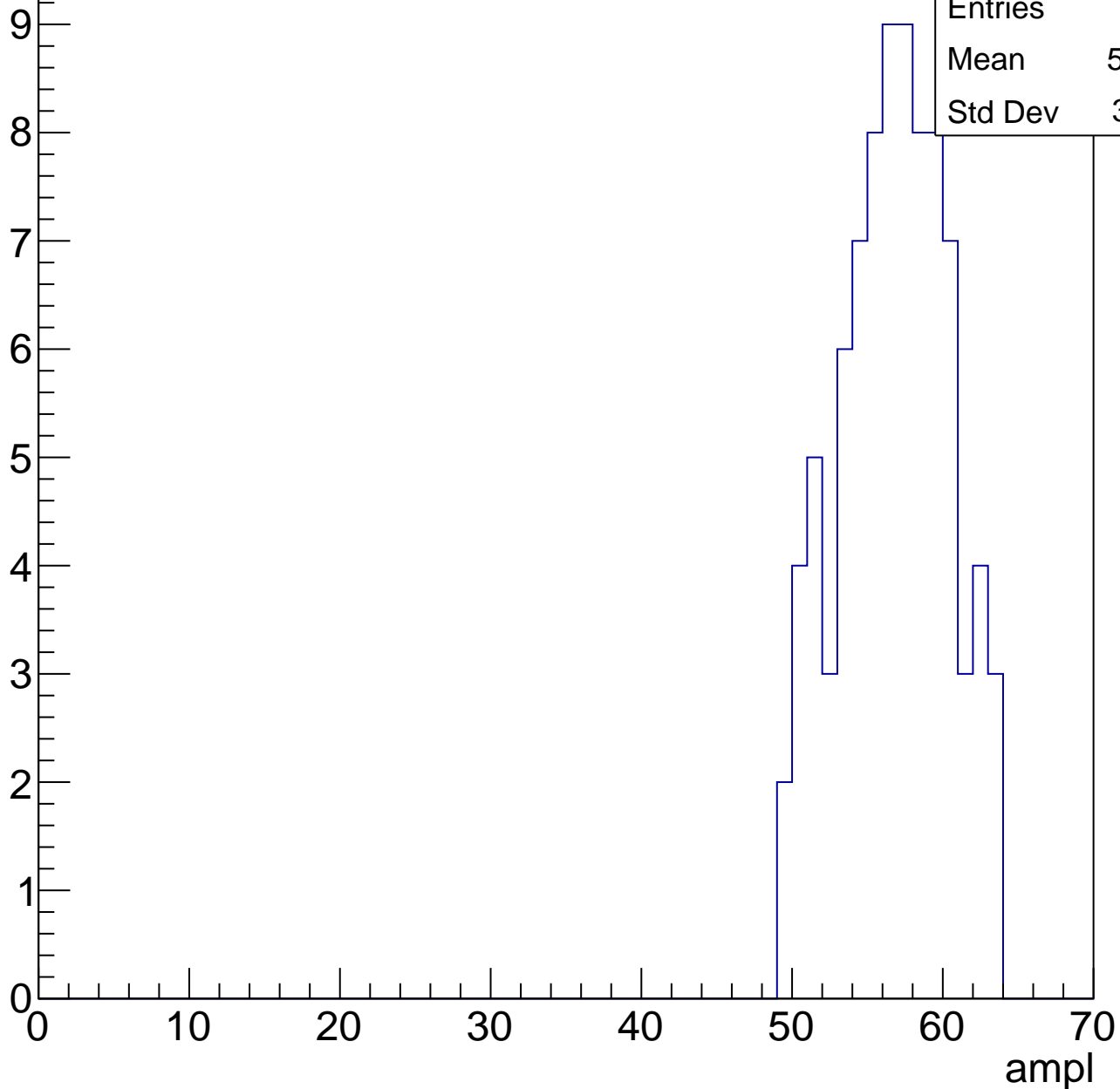
calib\_packv5\_042523\_0143.root, FC#4, port A2



# B1L100S, U2-ch25, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	86
Mean	56.26
Std Dev	3.561

# B1L100S, U2-ch25, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

7

6

5

4

3

2

1

0

Entries	26
Mean	60.81
Std Dev	1.902

ampl

10

20

30

40

50

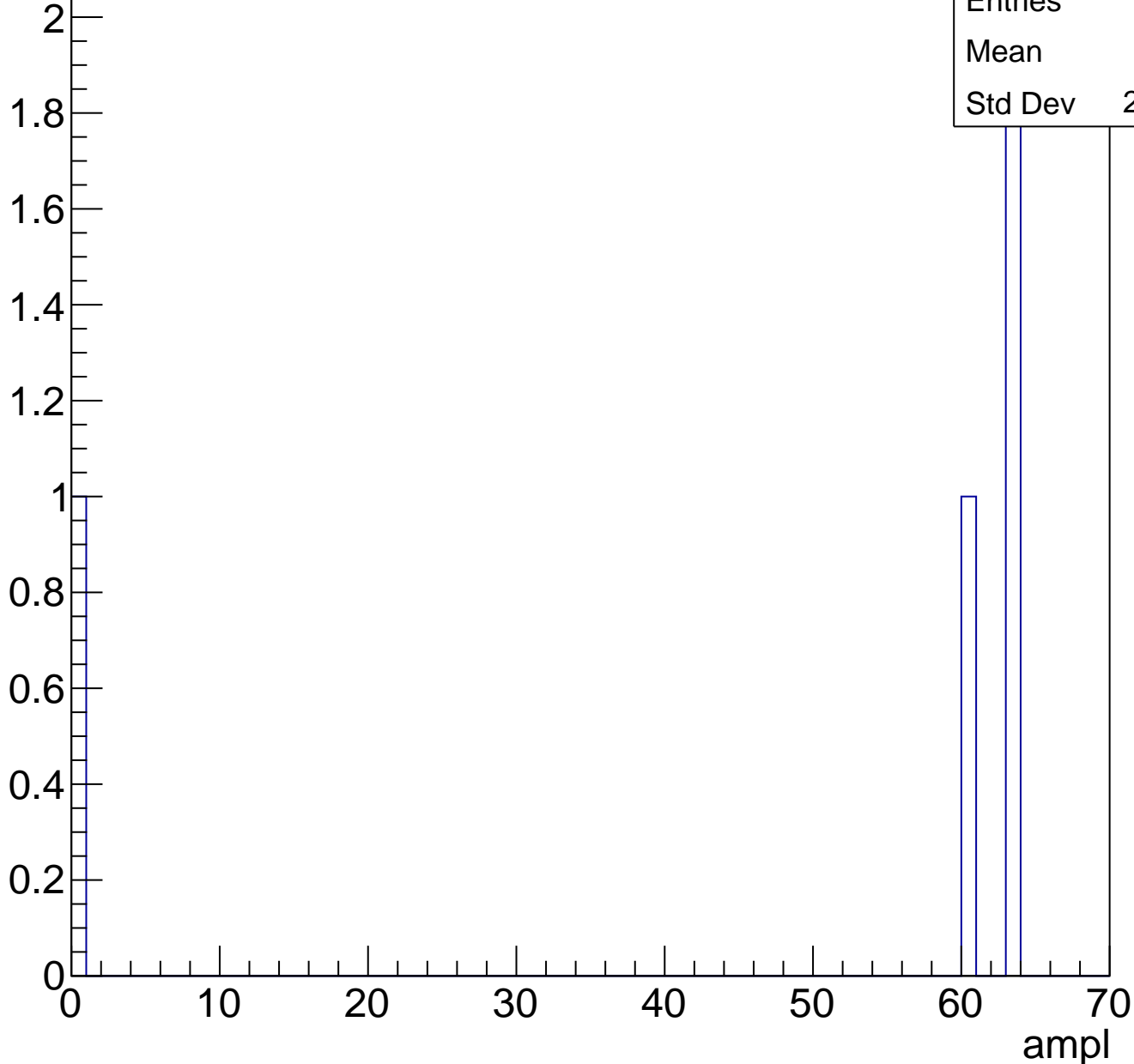
60

70

# B1L100S, U2-ch25, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry





# B1L100S, U2-ch25, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

1

0.8

0.6

0.4

0.2

0

0

10

20

30

40

50

60

70

ampl

Entries

0

Mean

0

Std Dev

0

# B1L100S, U2-ch26, adc0

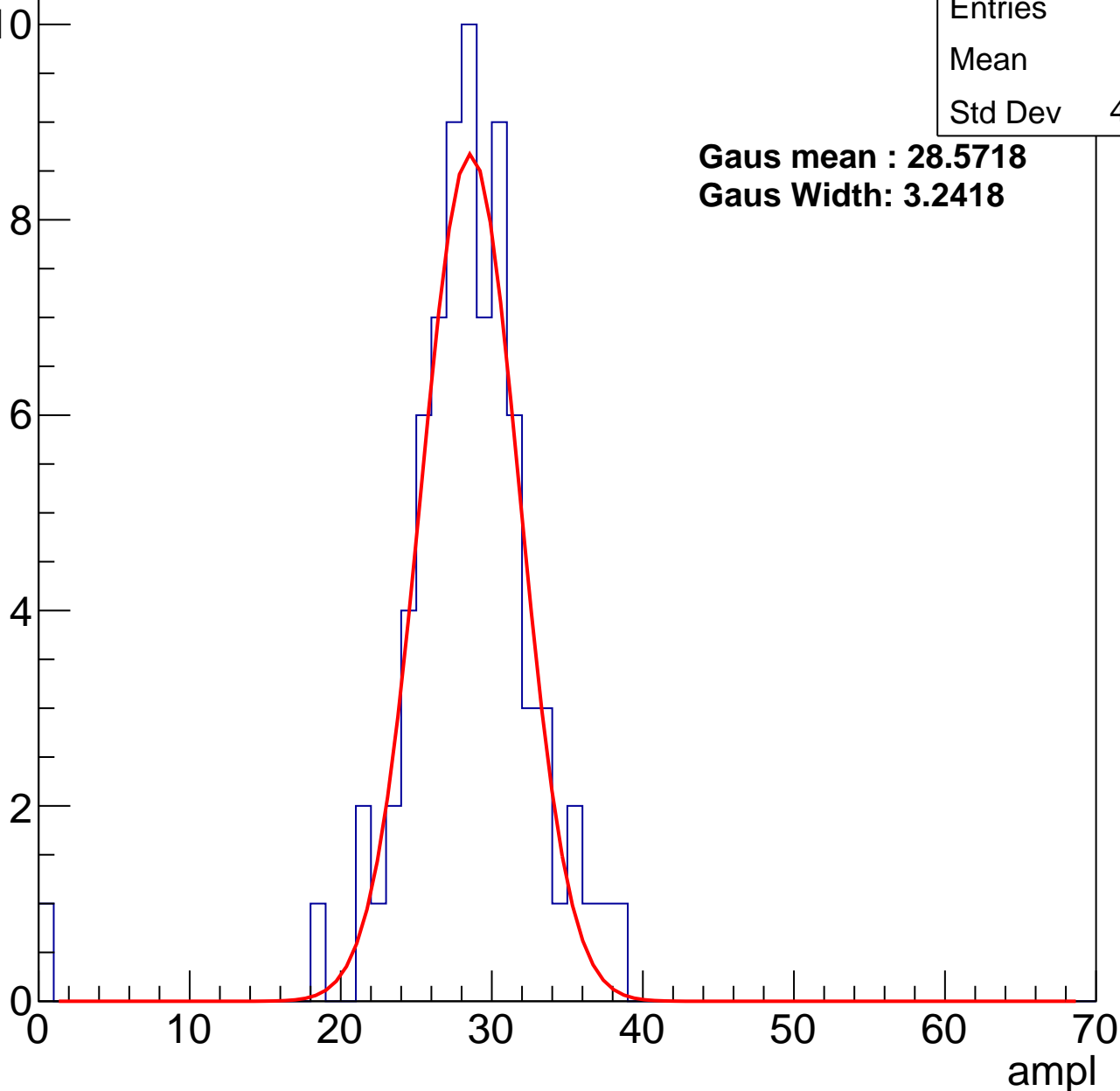
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	77
Mean	27.9
Std Dev	4.863

**Gaus mean : 28.5718**

**Gaus Width: 3.2418**



# B1L100S, U2-ch26, adc1

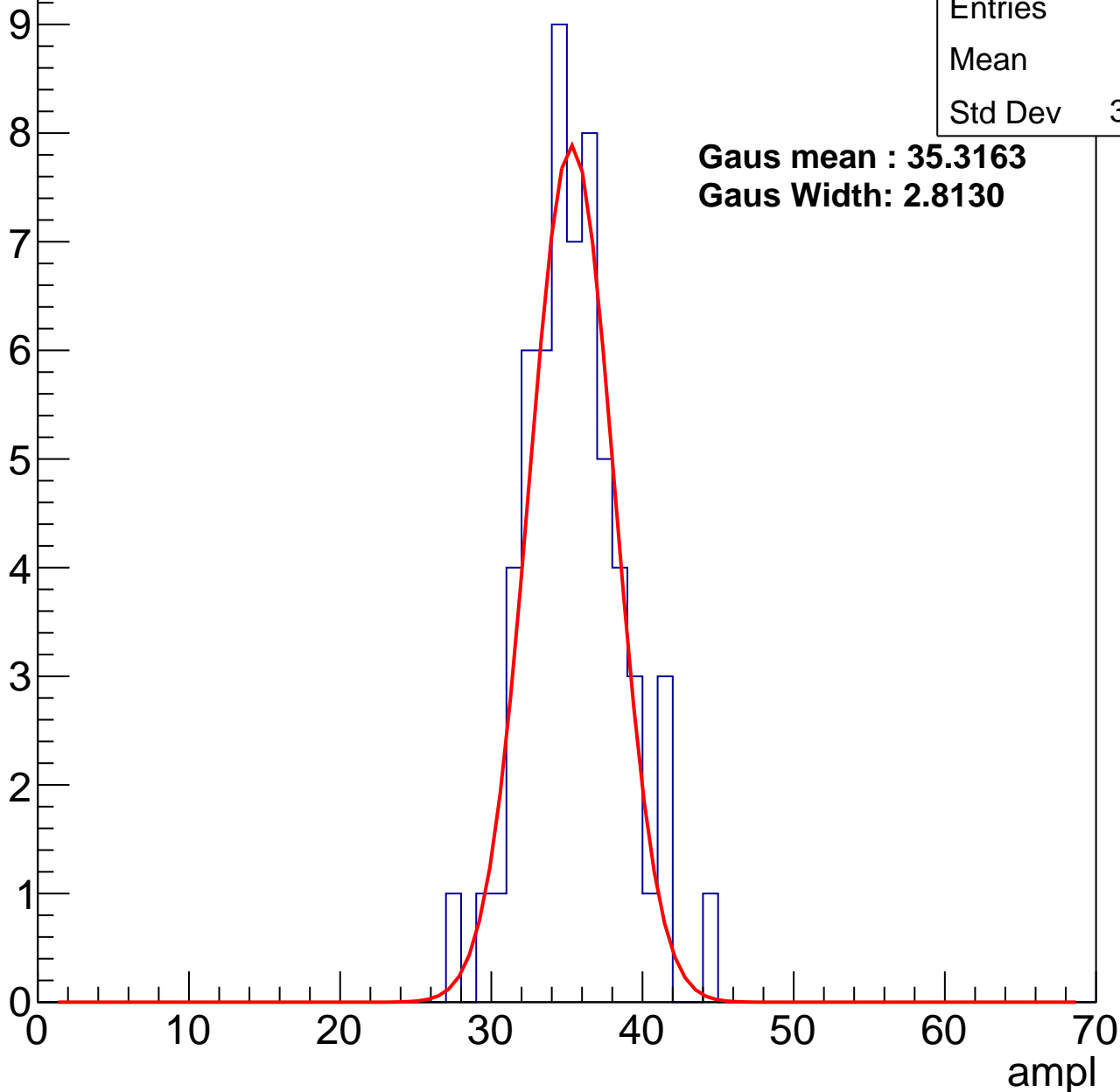
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	60
Mean	35
Std Dev	3.168

**Gaus mean : 35.3163**

**Gaus Width: 2.8130**



# B1L100S, U2-ch26, adc2

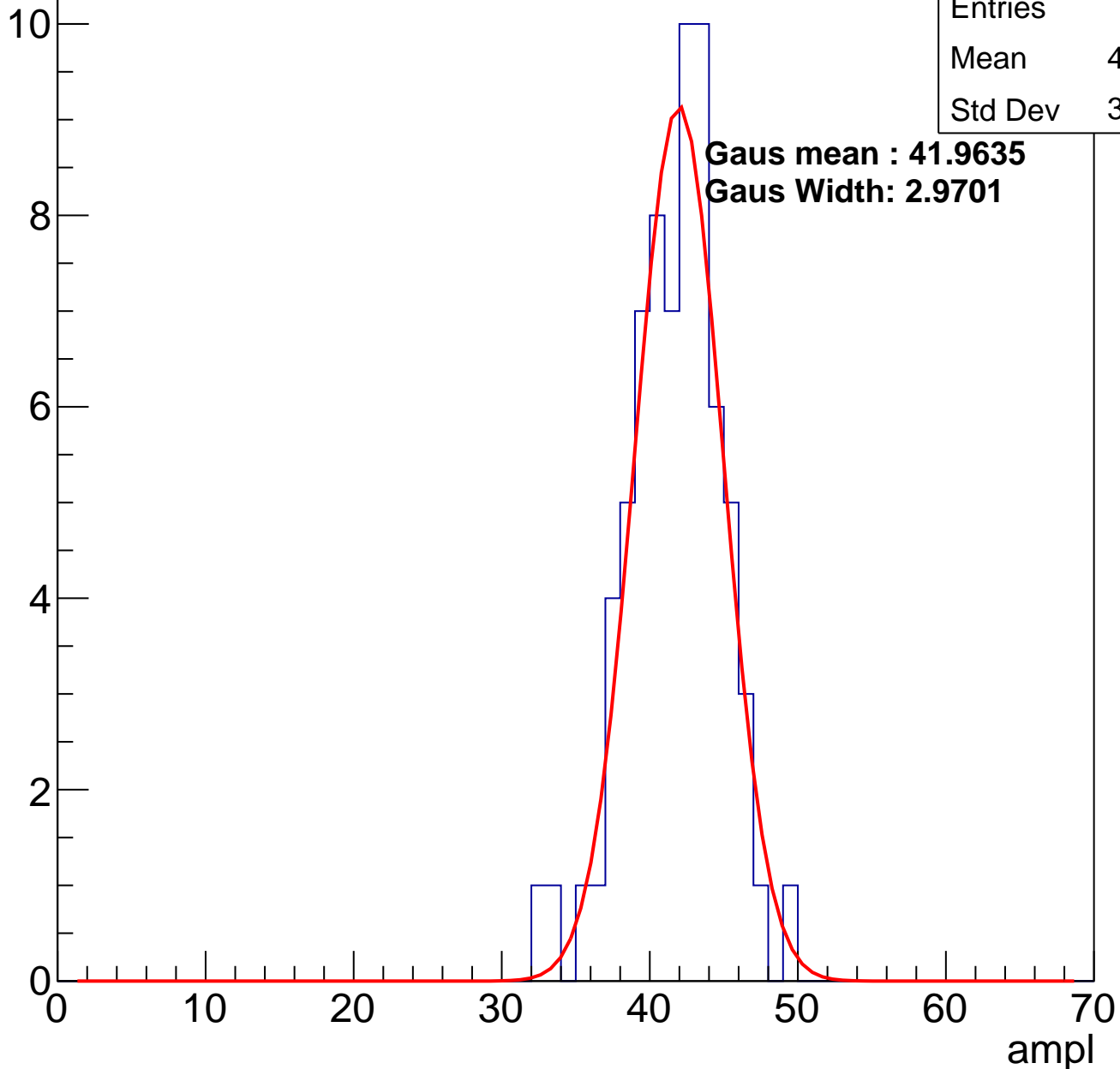
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	71
Mean	41.23
Std Dev	3.154

**Gaus mean : 41.9635**

**Gaus Width: 2.9701**

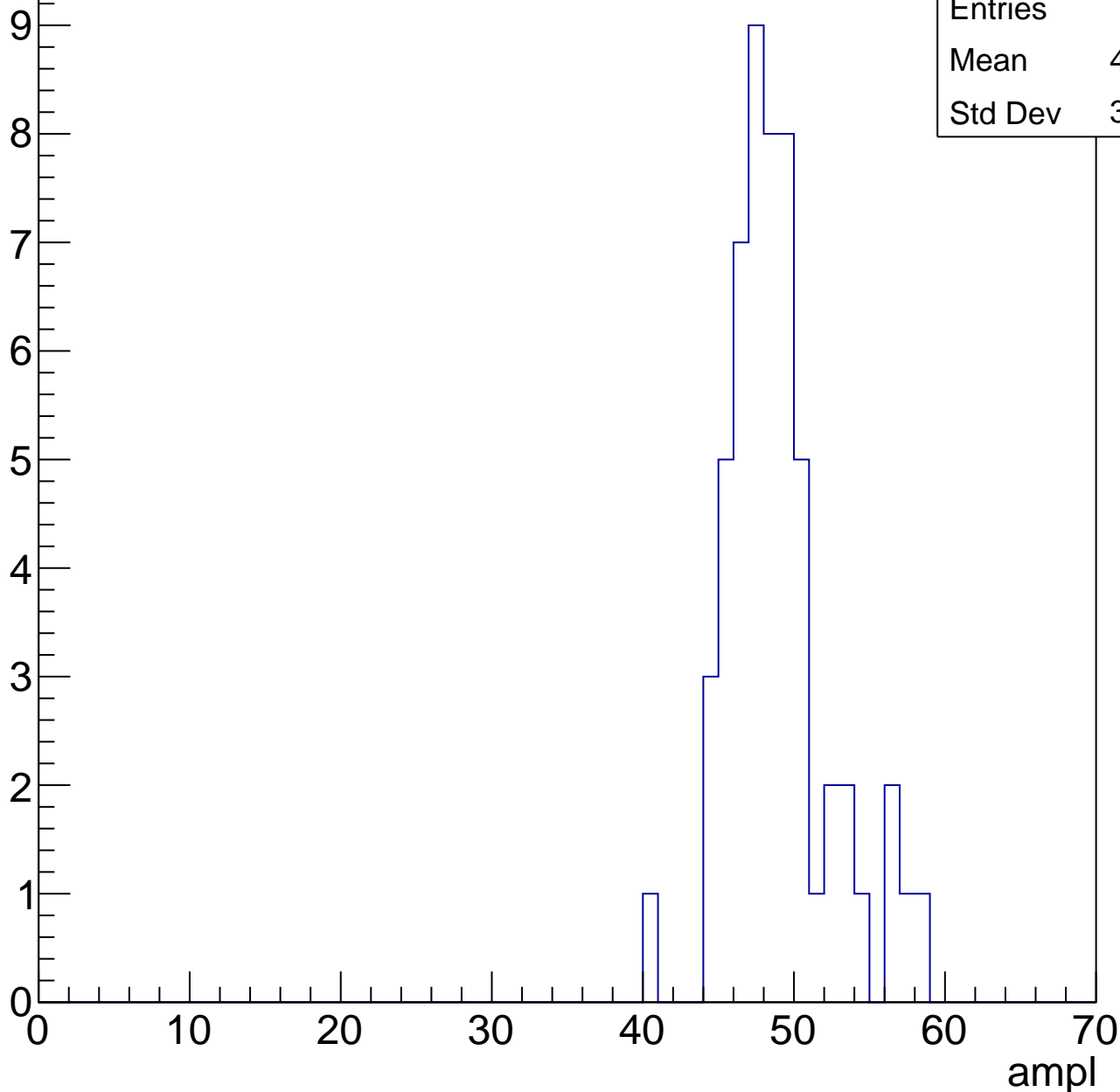
Entry



# B1L100S, U2-ch26, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



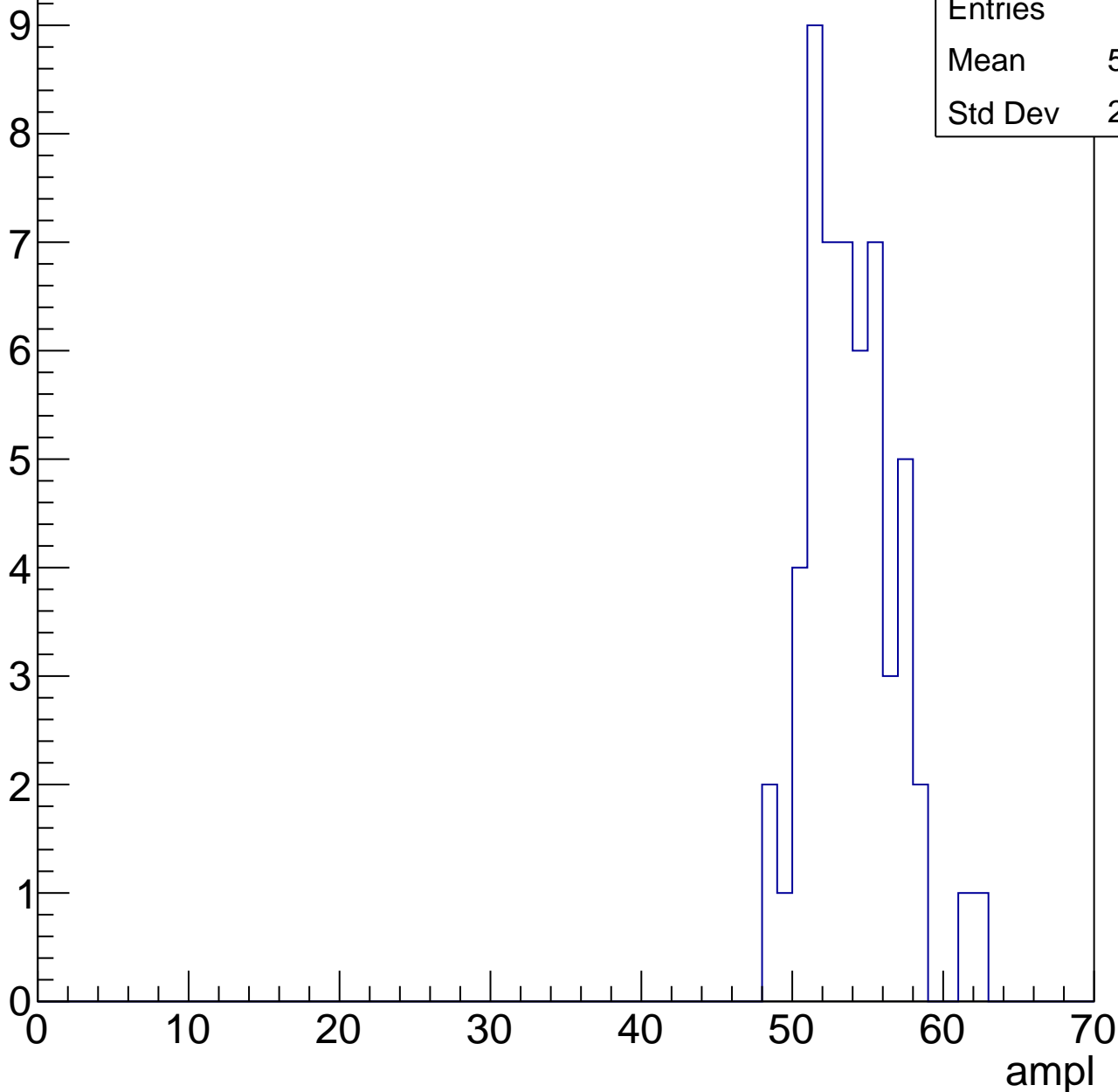
Entries	56
Mean	48.39
Std Dev	3.405

# B1L100S, U2-ch26, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	55
Mean	53.45
Std Dev	2.922

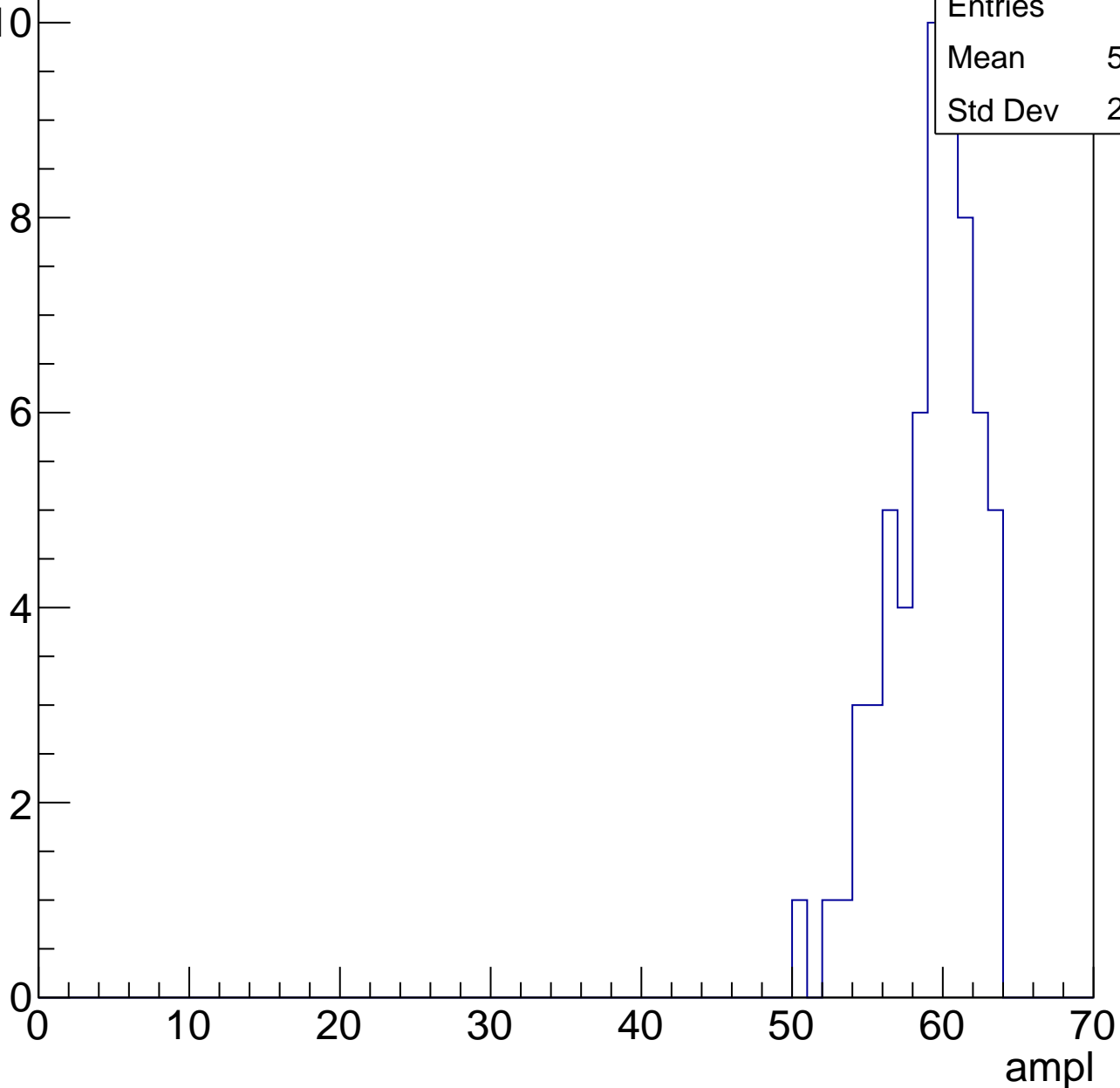


# B1L100S, U2-ch26, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	62
Mean	58.76
Std Dev	2.917



# B1L100S, U2-ch26, adc6

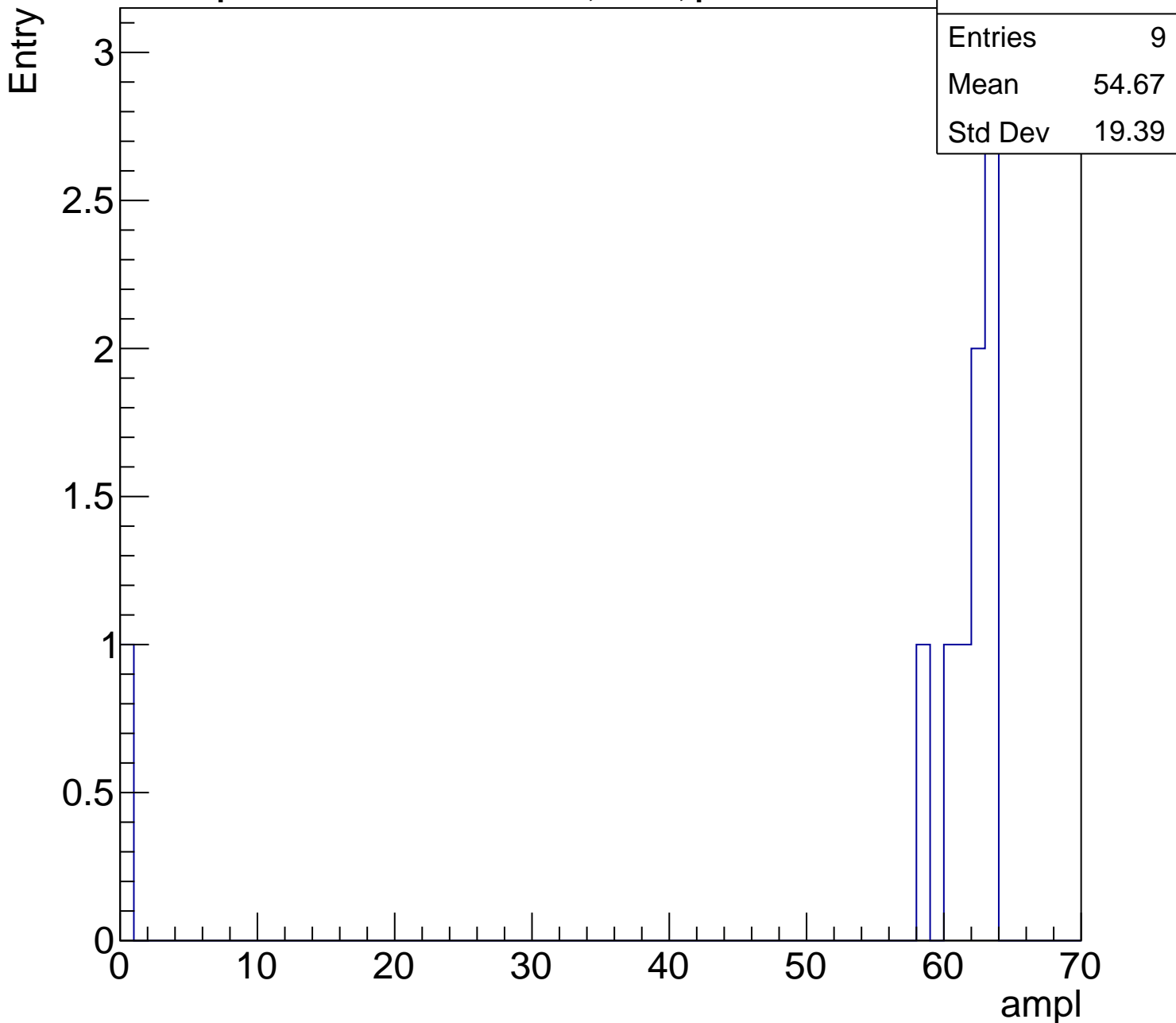
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

3  
2.5  
2  
1.5  
1  
0.5  
0

Entries	9
Mean	54.67
Std Dev	19.39

ampl





# B1L100S, U2-ch26, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



# B1L100S, U2-ch27, adc0

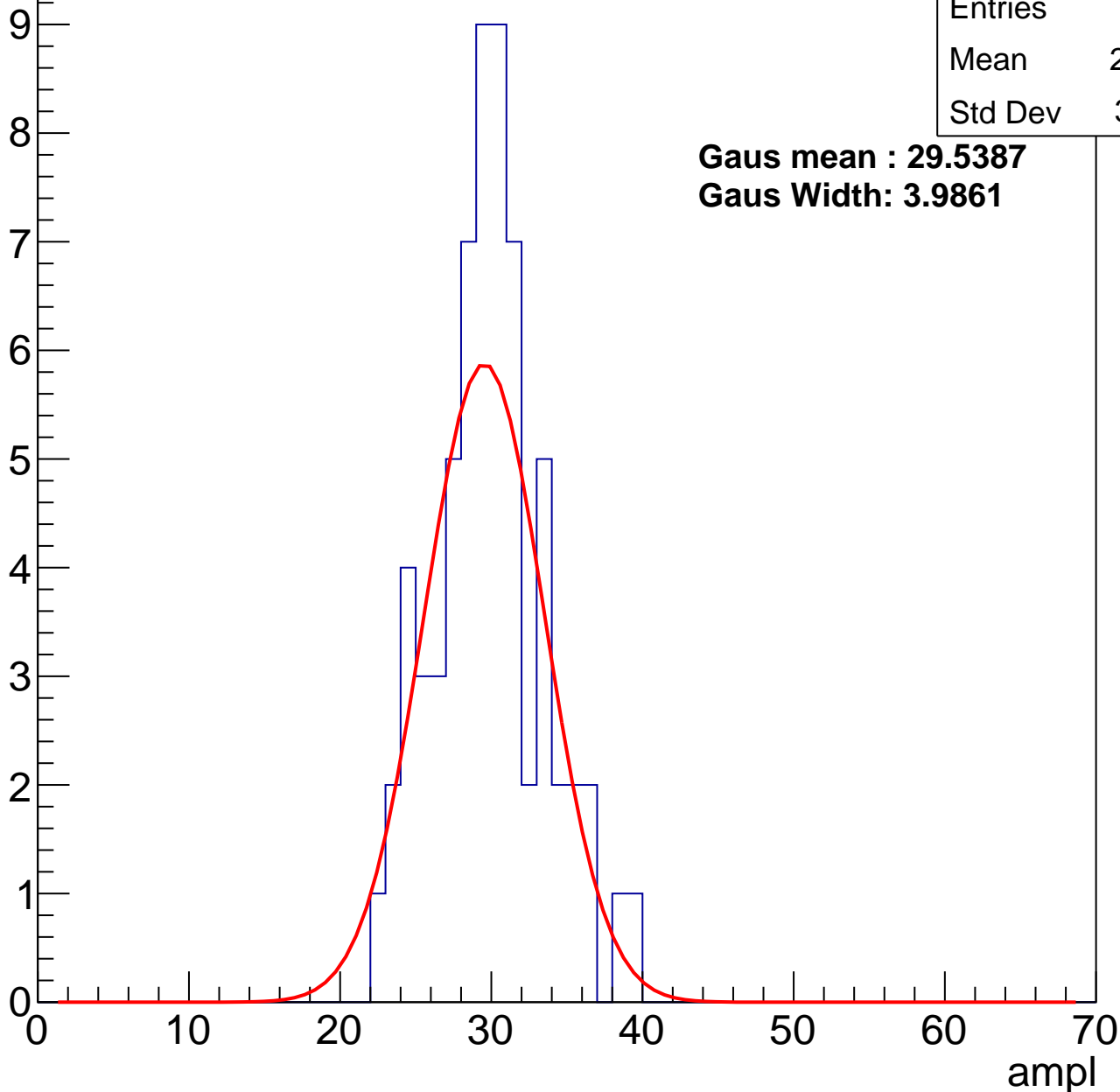
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	65
Mean	29.42
Std Dev	3.611

**Gaus mean : 29.5387**

**Gaus Width: 3.9861**



# B1L100S, U2-ch27, adc1

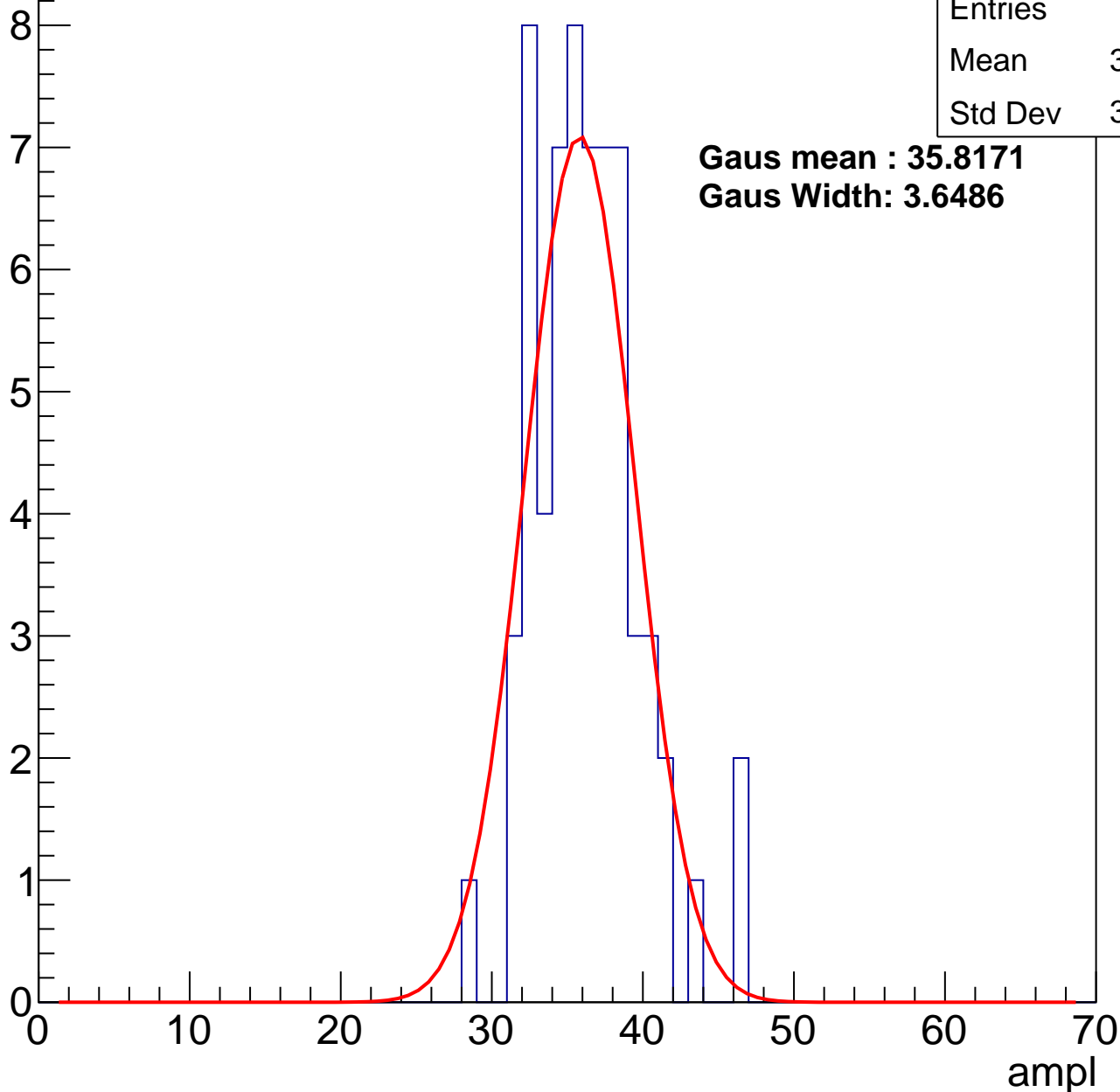
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	63
Mean	35.84
Std Dev	3.442

**Gaus mean : 35.8171**

**Gaus Width: 3.6486**



# B1L100S, U2-ch27, adc2

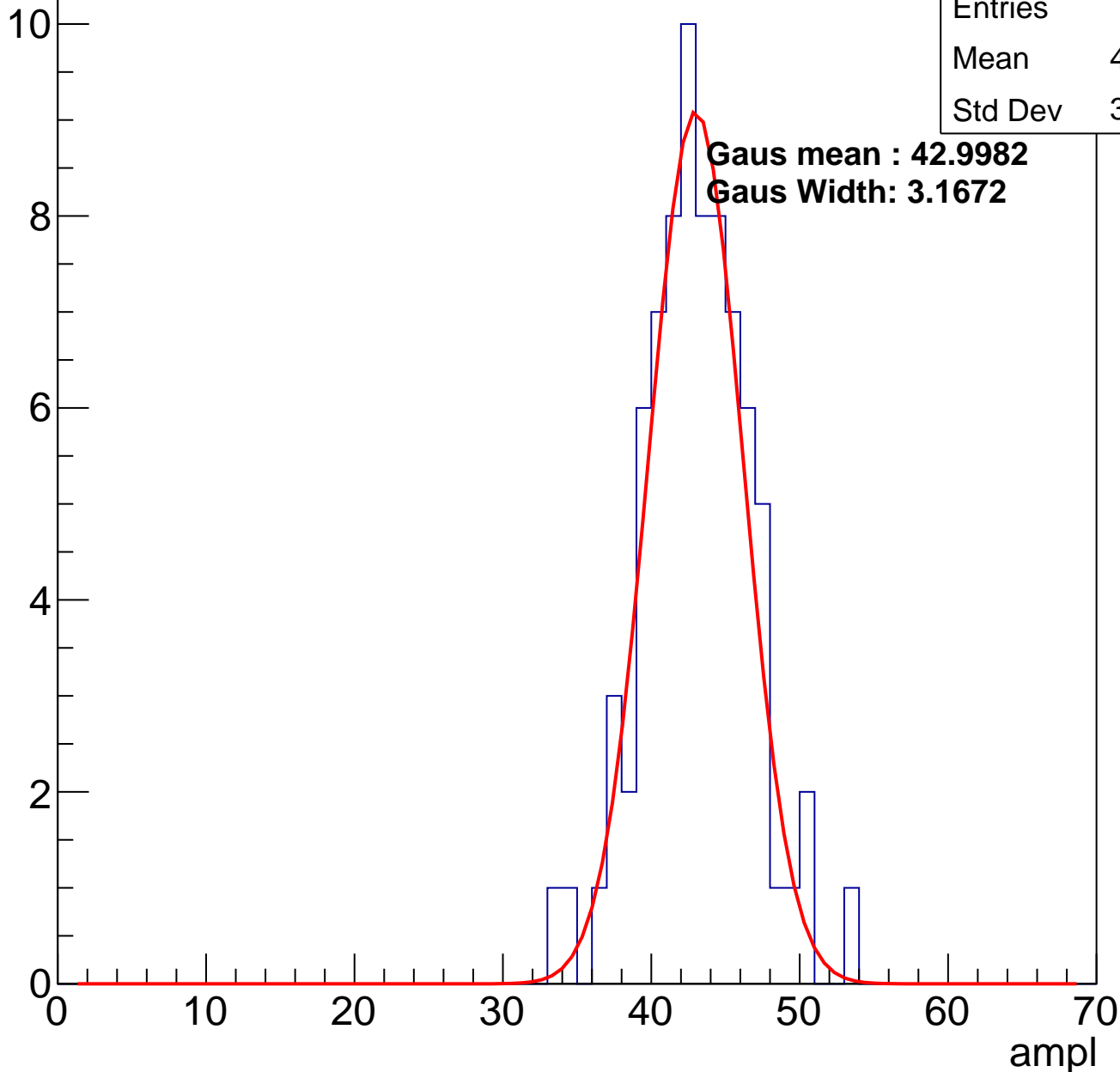
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	78
Mean	42.62
Std Dev	3.592

**Gaus mean : 42.9982**

**Gaus Width: 3.1672**

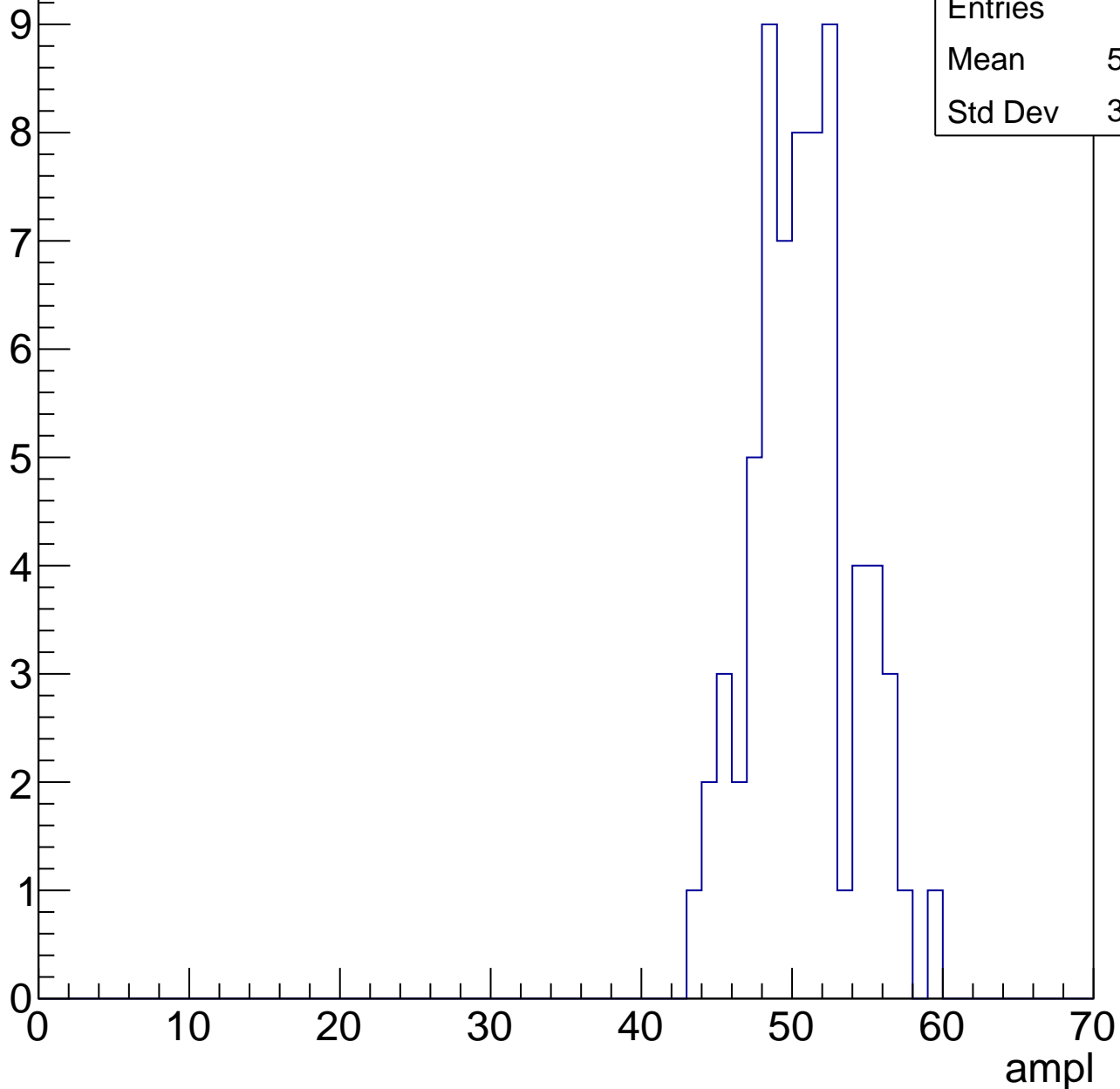
Entry



# B1L100S, U2-ch27, adc3

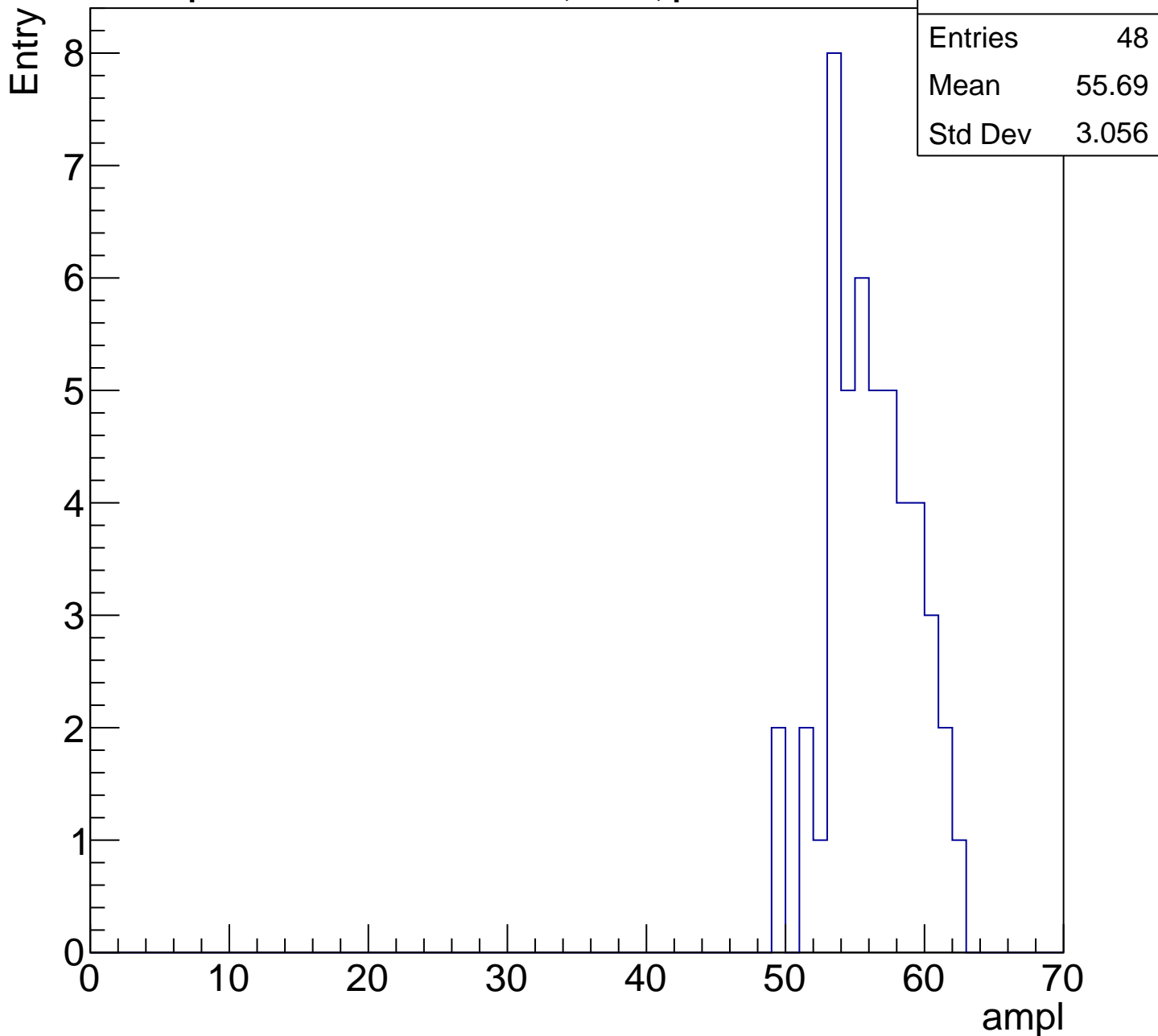
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



# B1L100S, U2-ch27, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

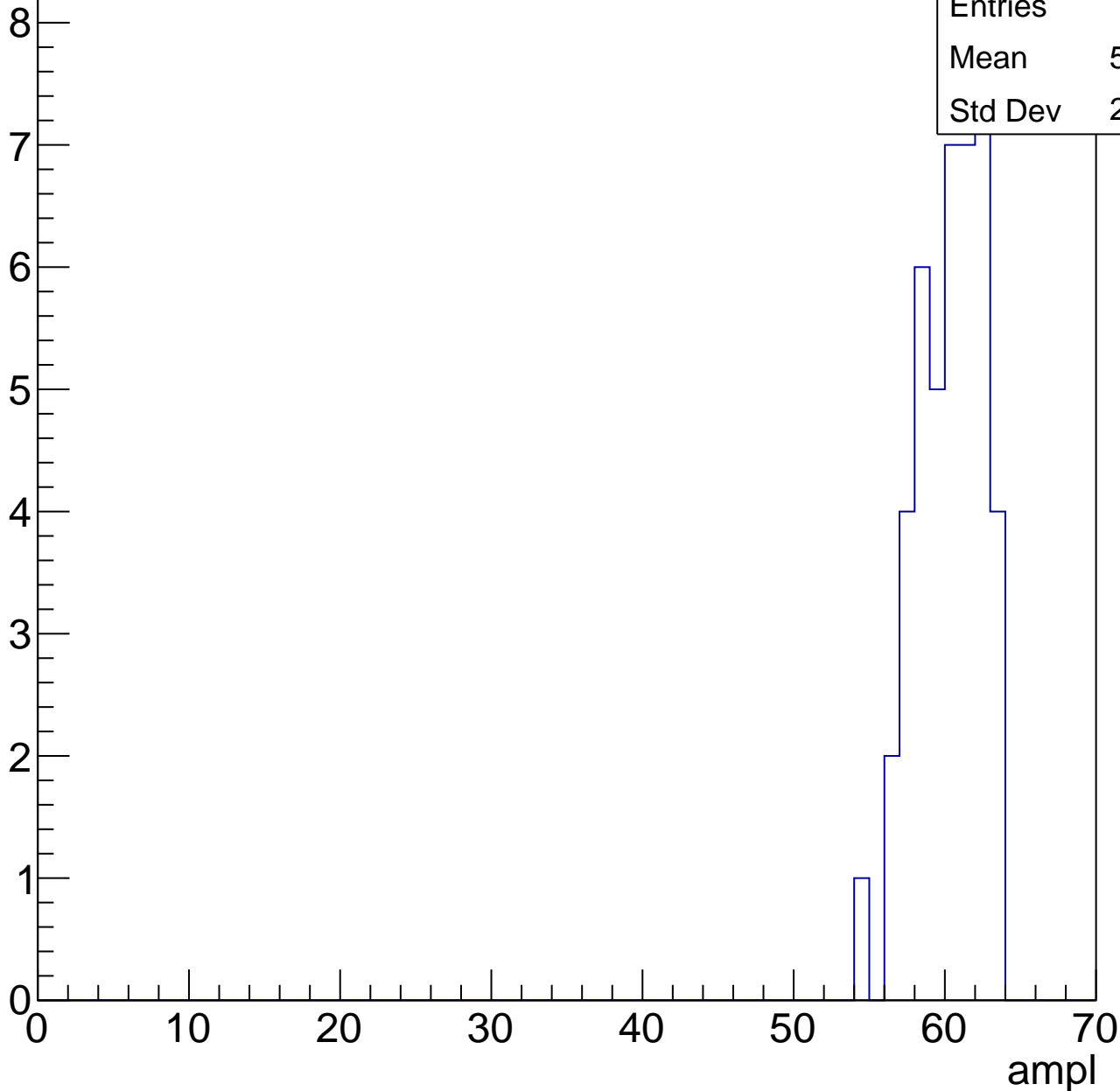


# B1L100S, U2-ch27, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	44
Mean	59.82
Std Dev	2.167

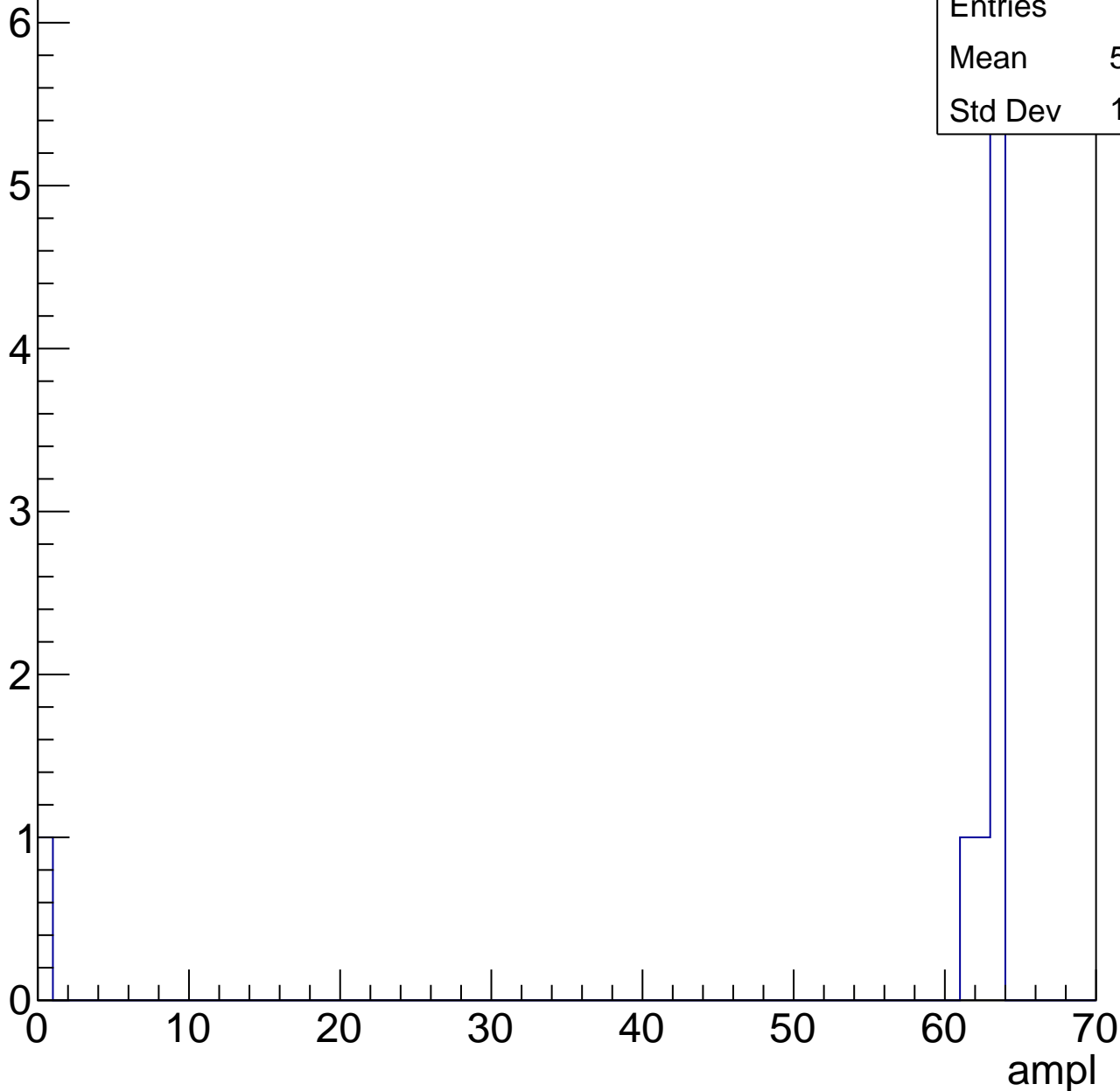


# B1L100S, U2-ch27, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	9
Mean	55.67
Std Dev	19.69





# B1L100S, U2-ch27, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L100S, U2-ch28, adc0

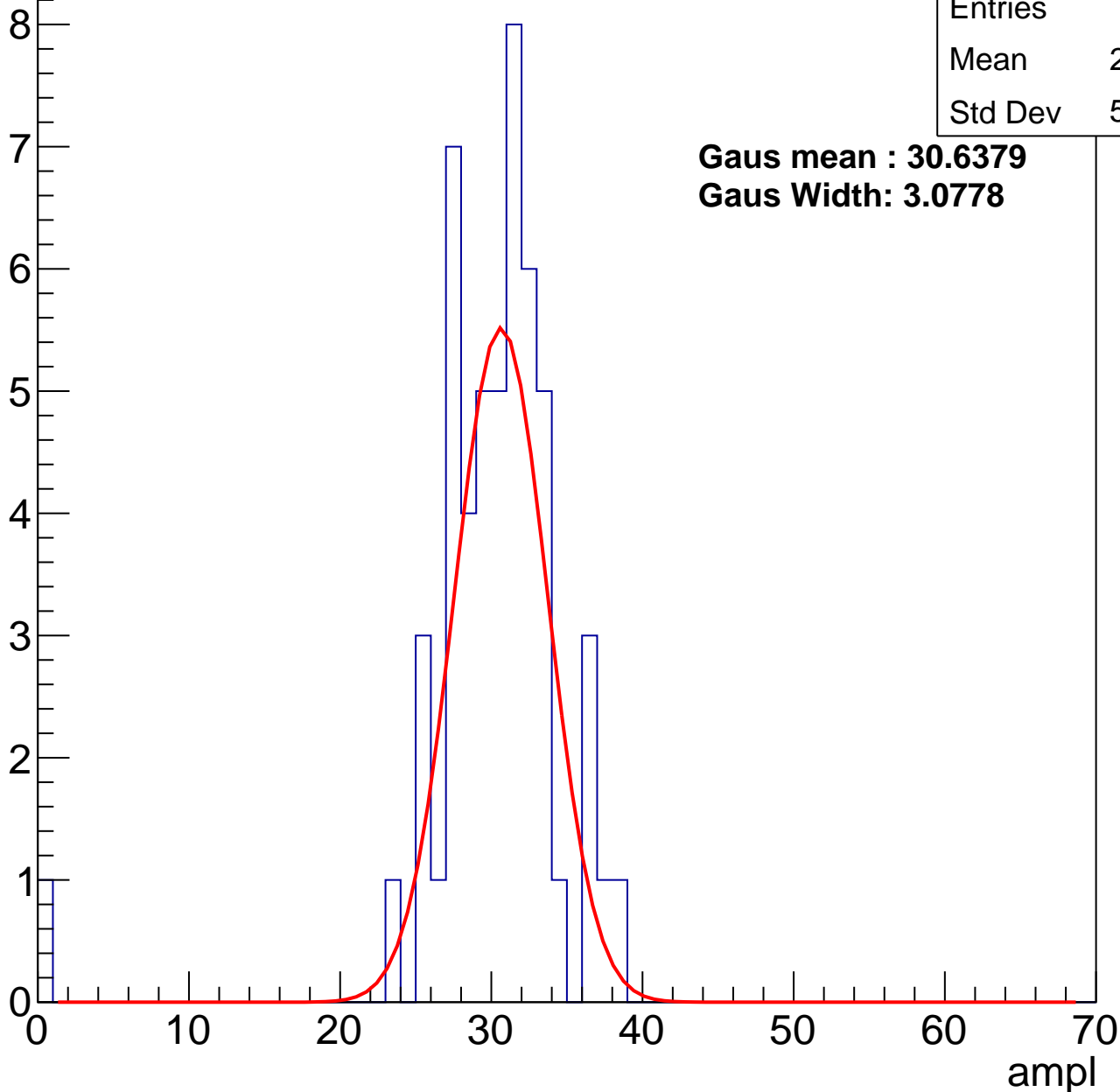
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	52
Mean	29.65
Std Dev	5.247

**Gaus mean : 30.6379**

**Gaus Width: 3.0778**



# B1L100S, U2-ch28, adc1

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	84
Mean	36.88
Std Dev	3.63

**Gaus mean : 37.3126**

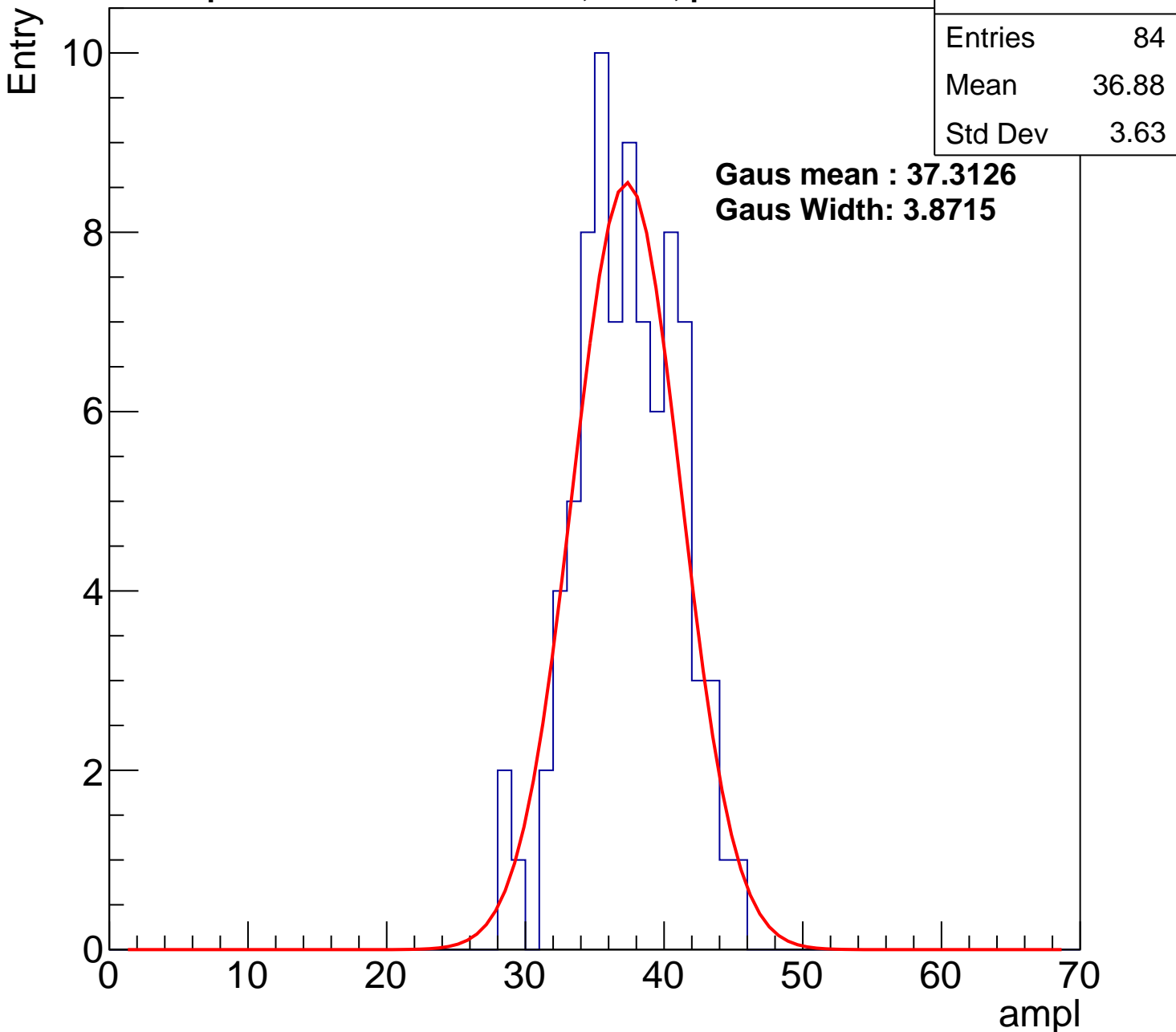
**Gaus Width: 3.8715**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B1L100S, U2-ch28, adc2

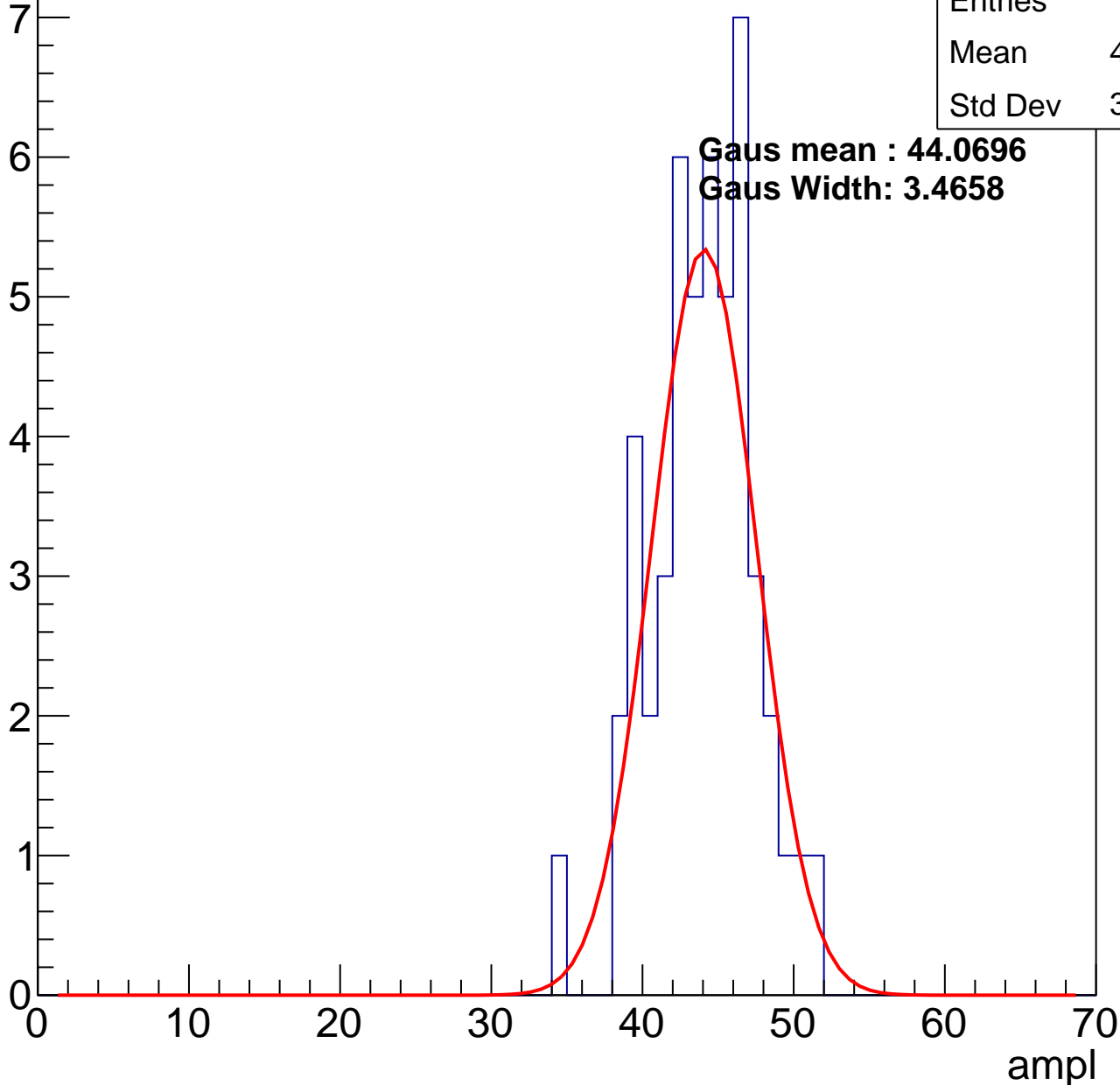
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	49
Mean	43.55
Std Dev	3.357

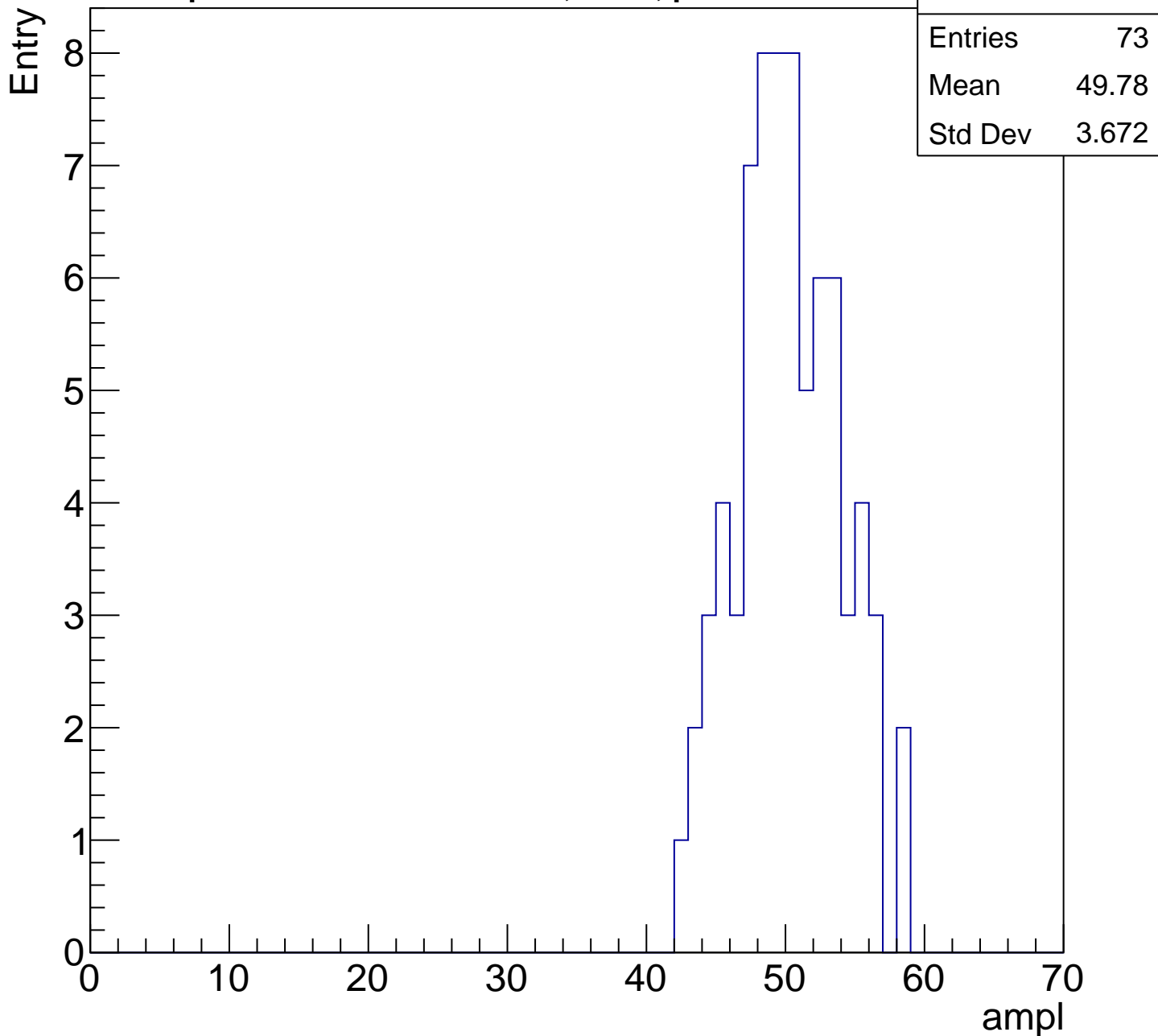
**Gaus mean : 44.0696**

**Gaus Width: 3.4658**



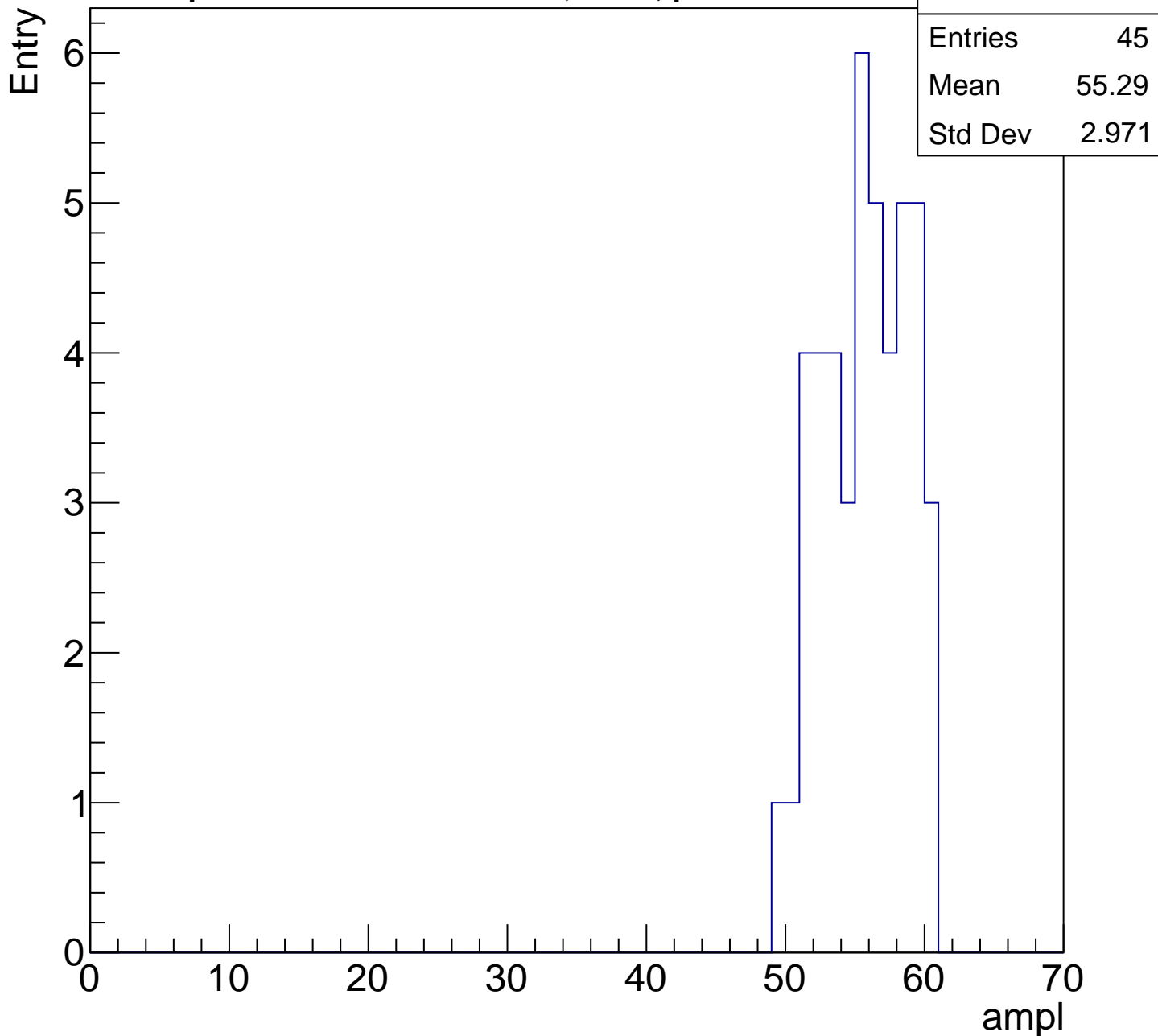
# B1L100S, U2-ch28, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2



# B1L100S, U2-ch28, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

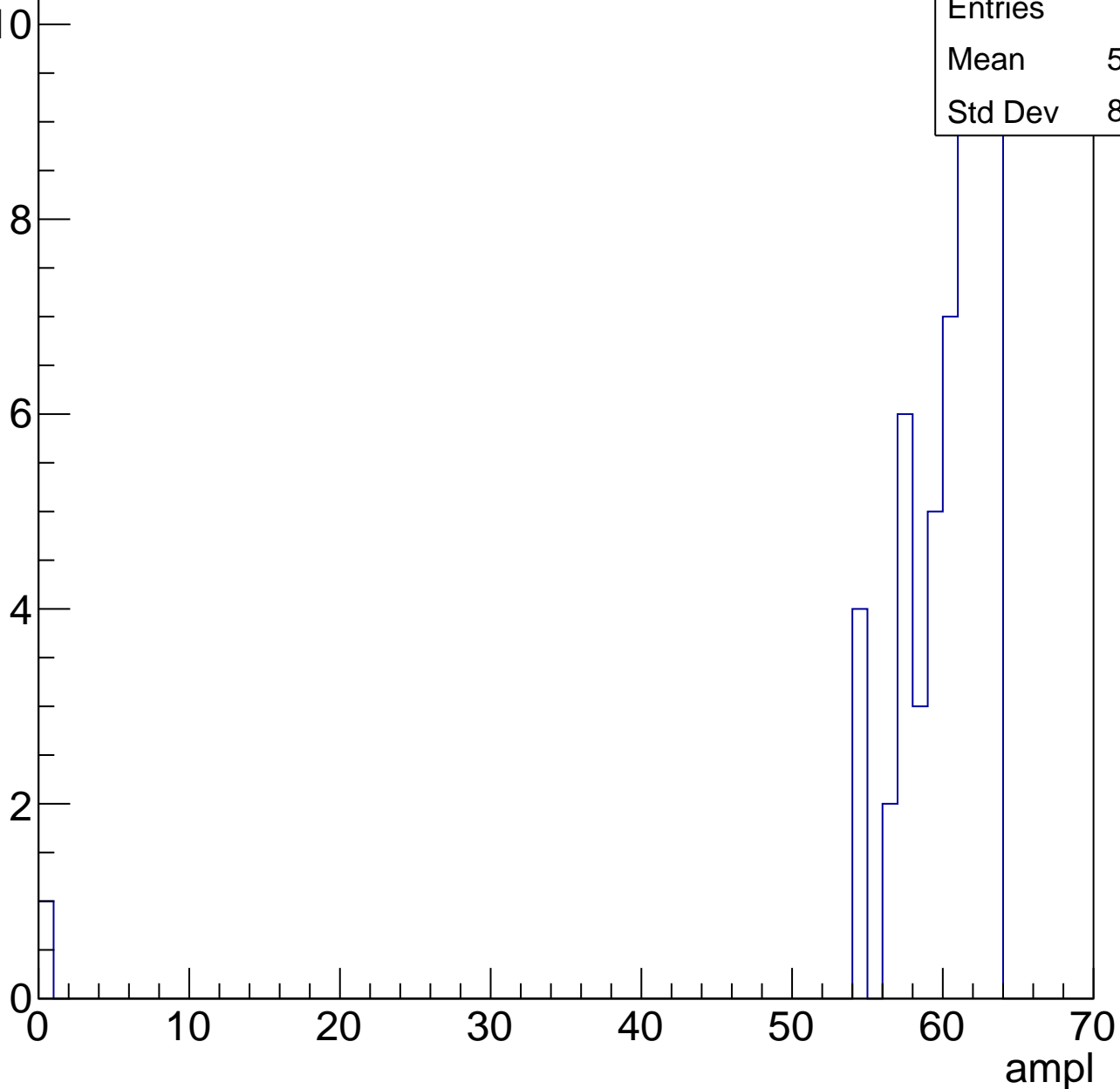


# B1L100S, U2-ch28, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	58
Mean	58.95
Std Dev	8.224



# B1L100S, U2-ch28, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	0
Mean	0
Std Dev	0



# B1L100S, U2-ch28, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

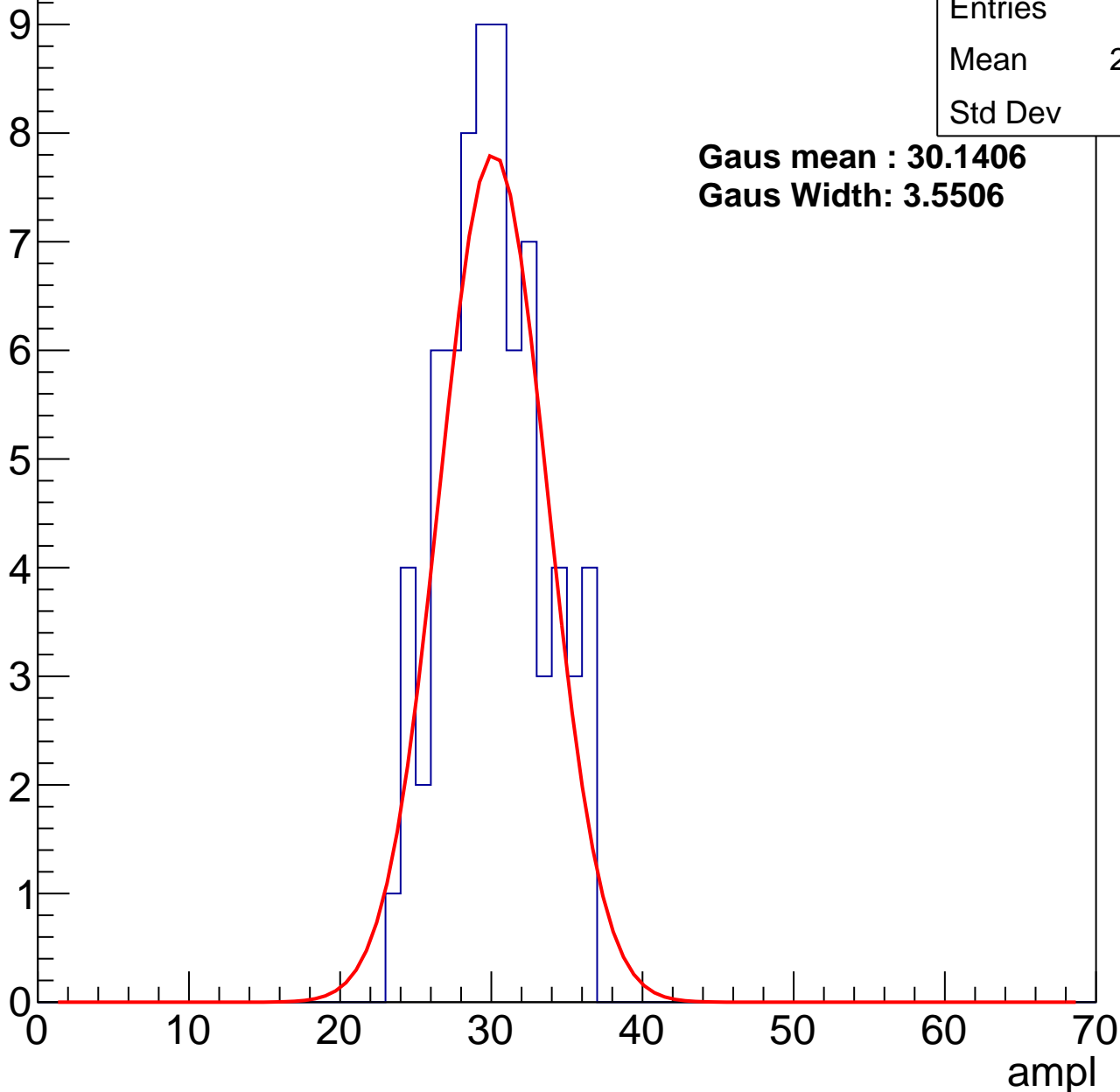


Entries	1
Mean	0
Std Dev	0

# B1L100S, U2-ch29, adc0

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



# B1L100S, U2-ch29, adc1

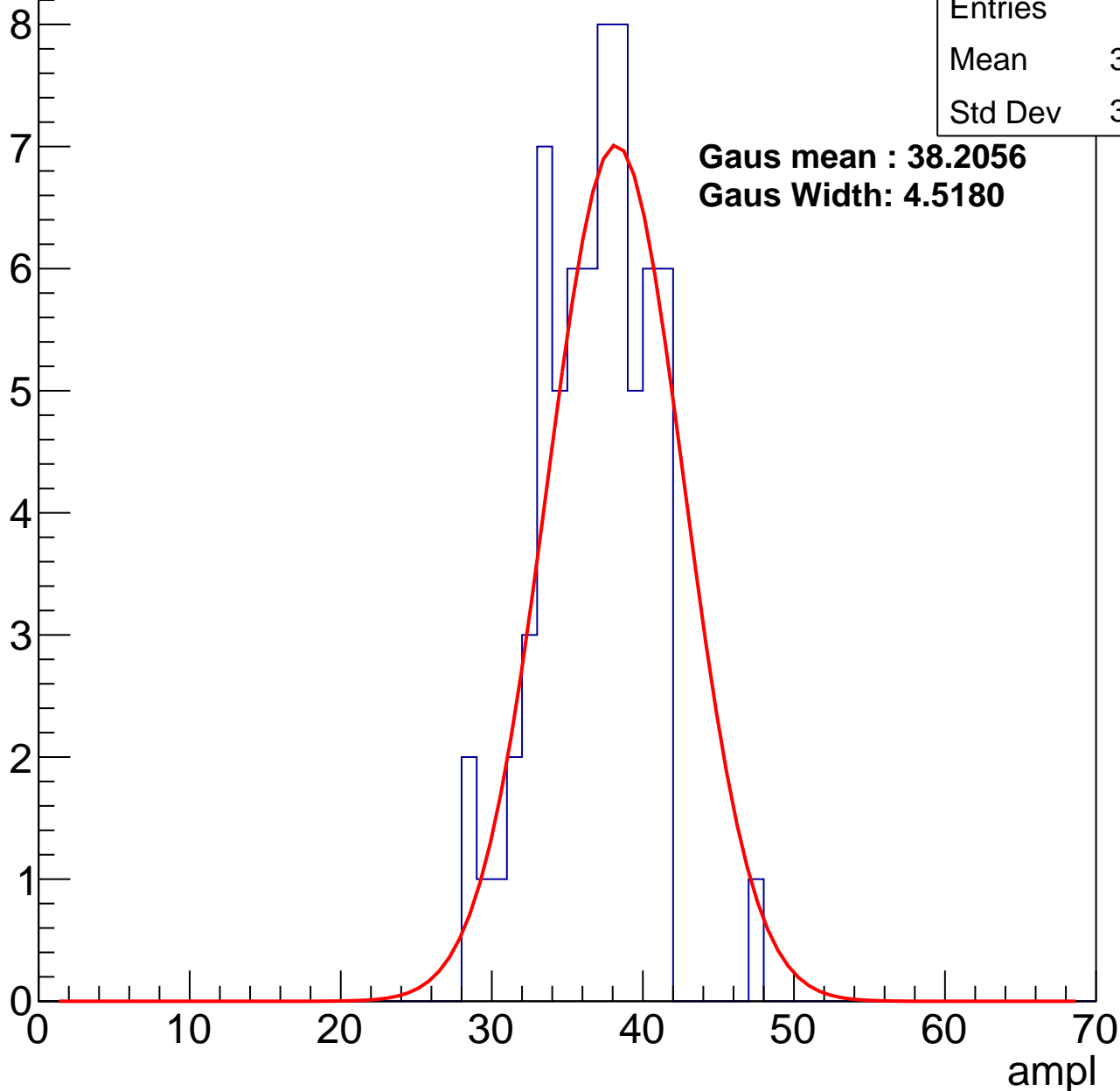
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	67
Mean	36.24
Std Dev	3.558

**Gaus mean : 38.2056**

**Gaus Width: 4.5180**



# B1L100S, U2-ch29, adc2

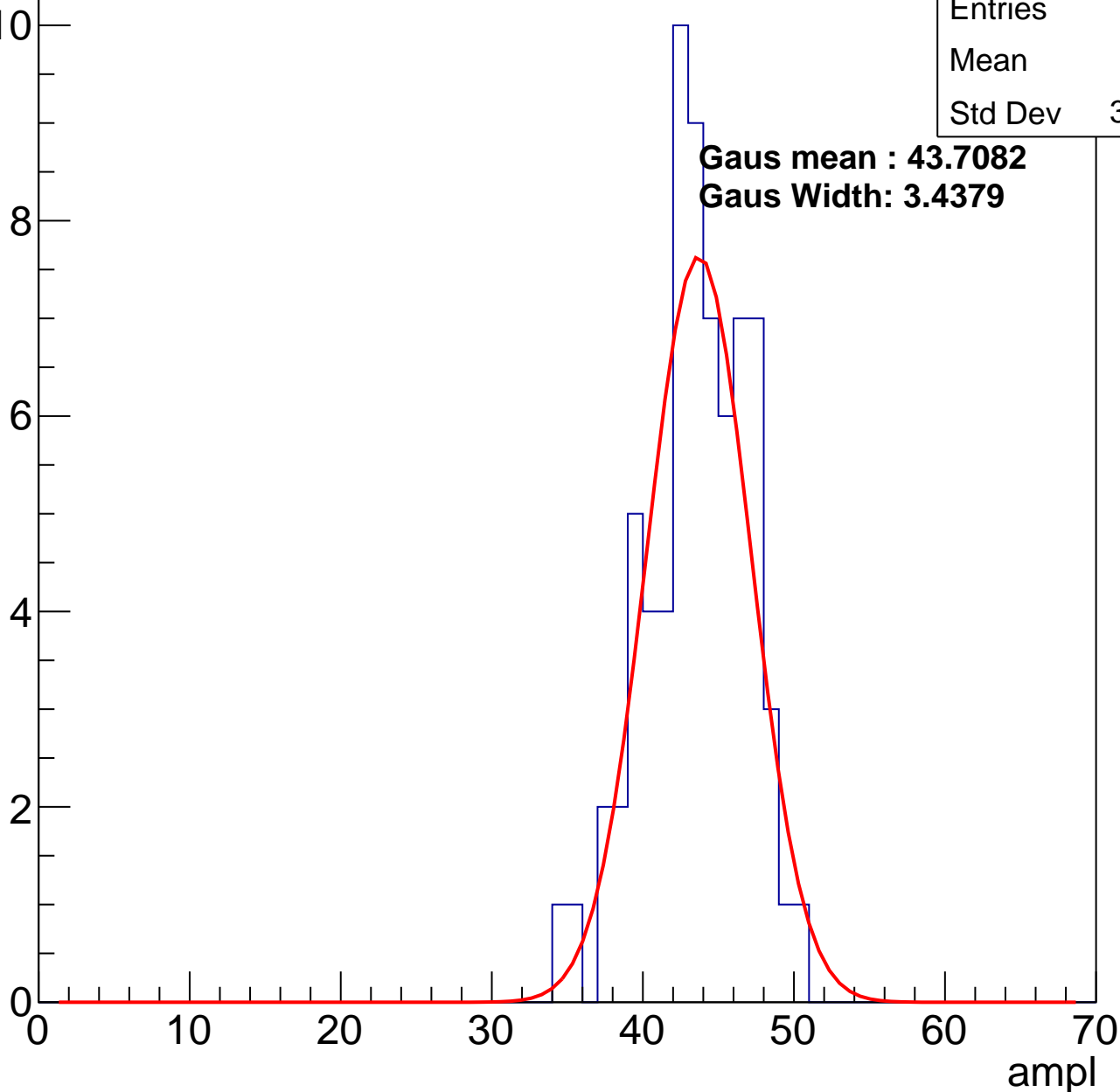
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	70
Mean	43.1
Std Dev	3.326

**Gaus mean : 43.7082**

**Gaus Width: 3.4379**

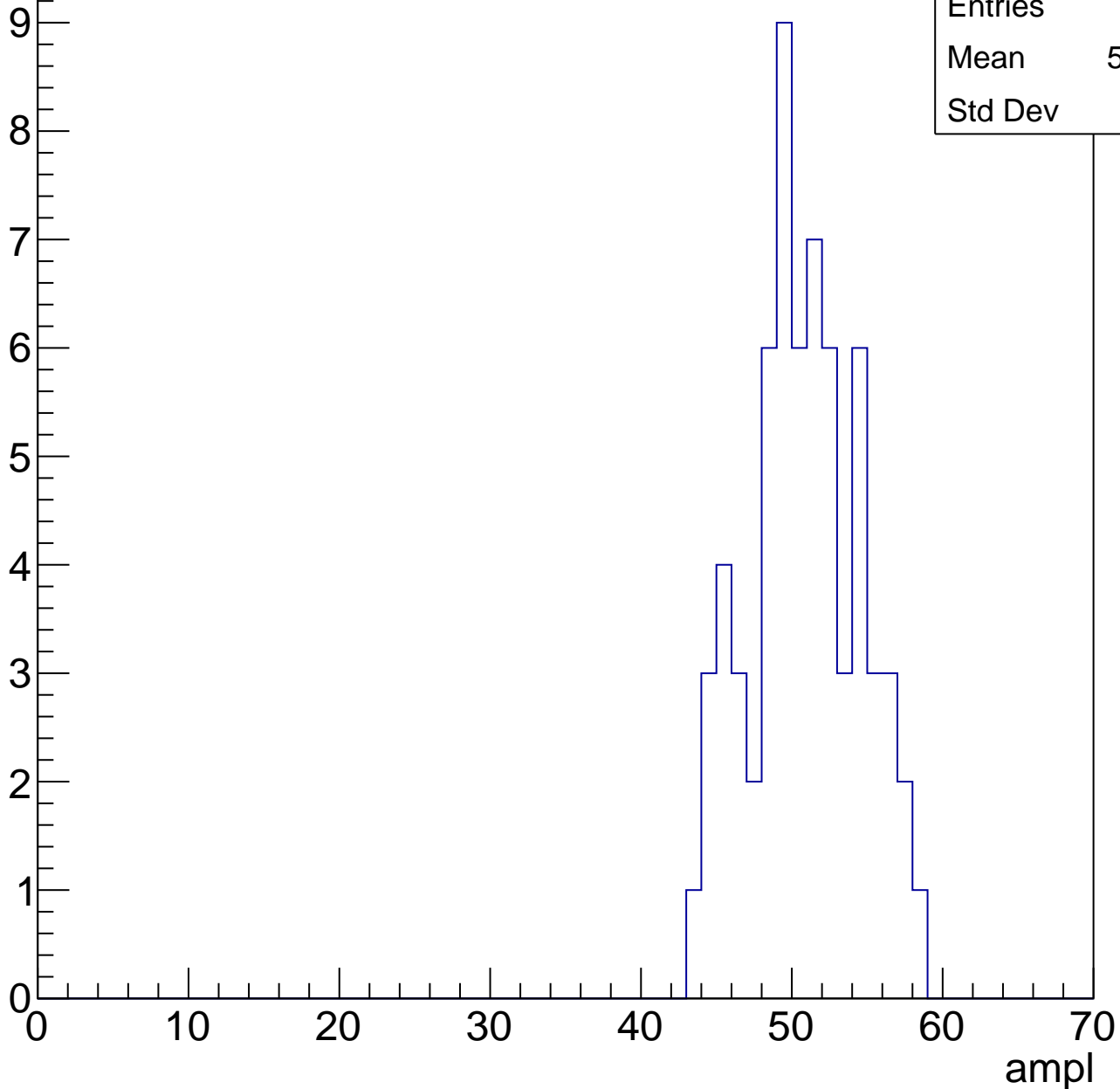


# B1L100S, U2-ch29, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

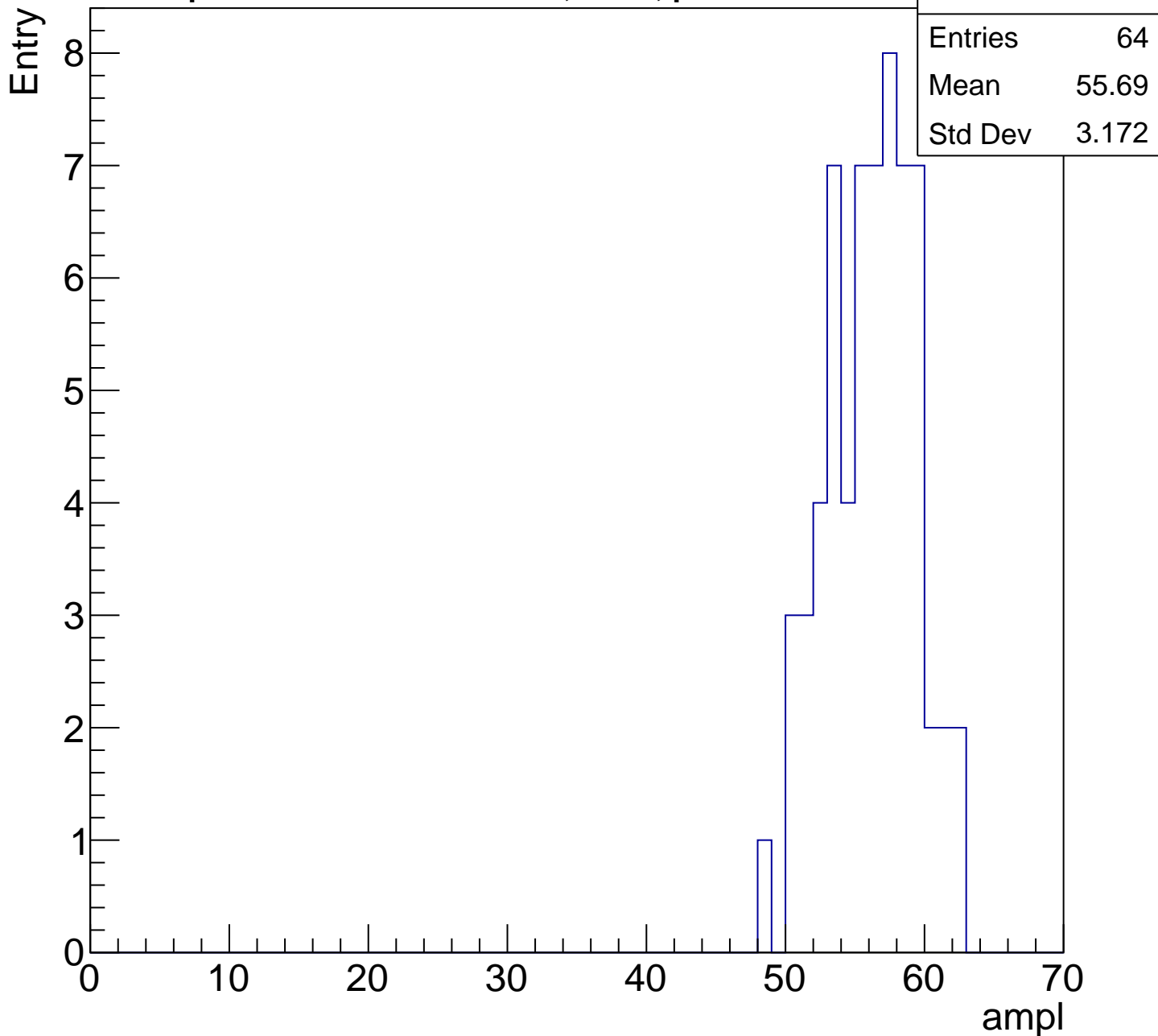
Entry

Entries	65
Mean	50.35
Std Dev	3.61



# B1L100S, U2-ch29, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2



# B1L100S, U2-ch29, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

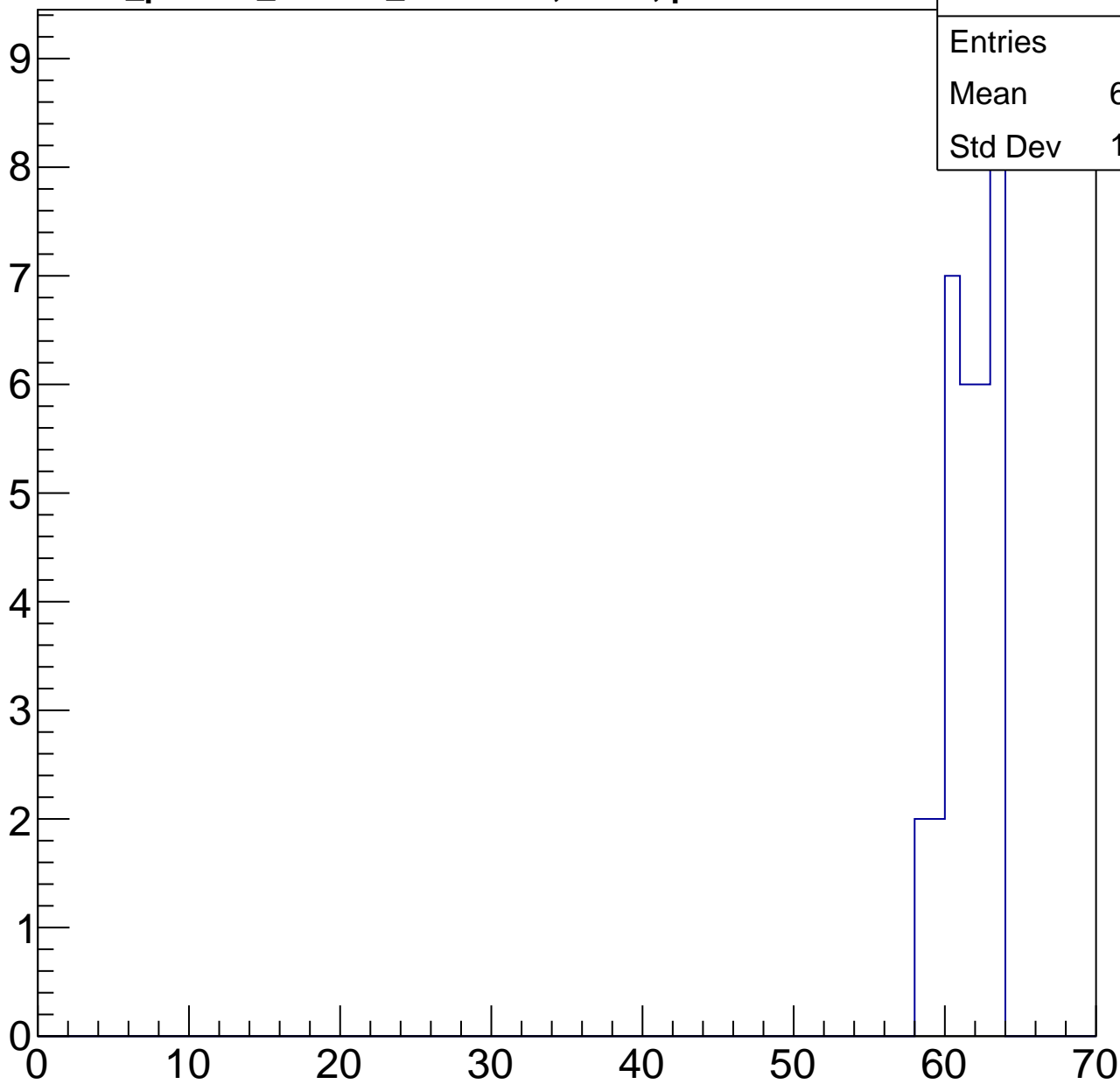
Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	32
Mean	61.22
Std Dev	1.515

ampl

0 10 20 30 40 50 60 70



# B1L100S, U2-ch29, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

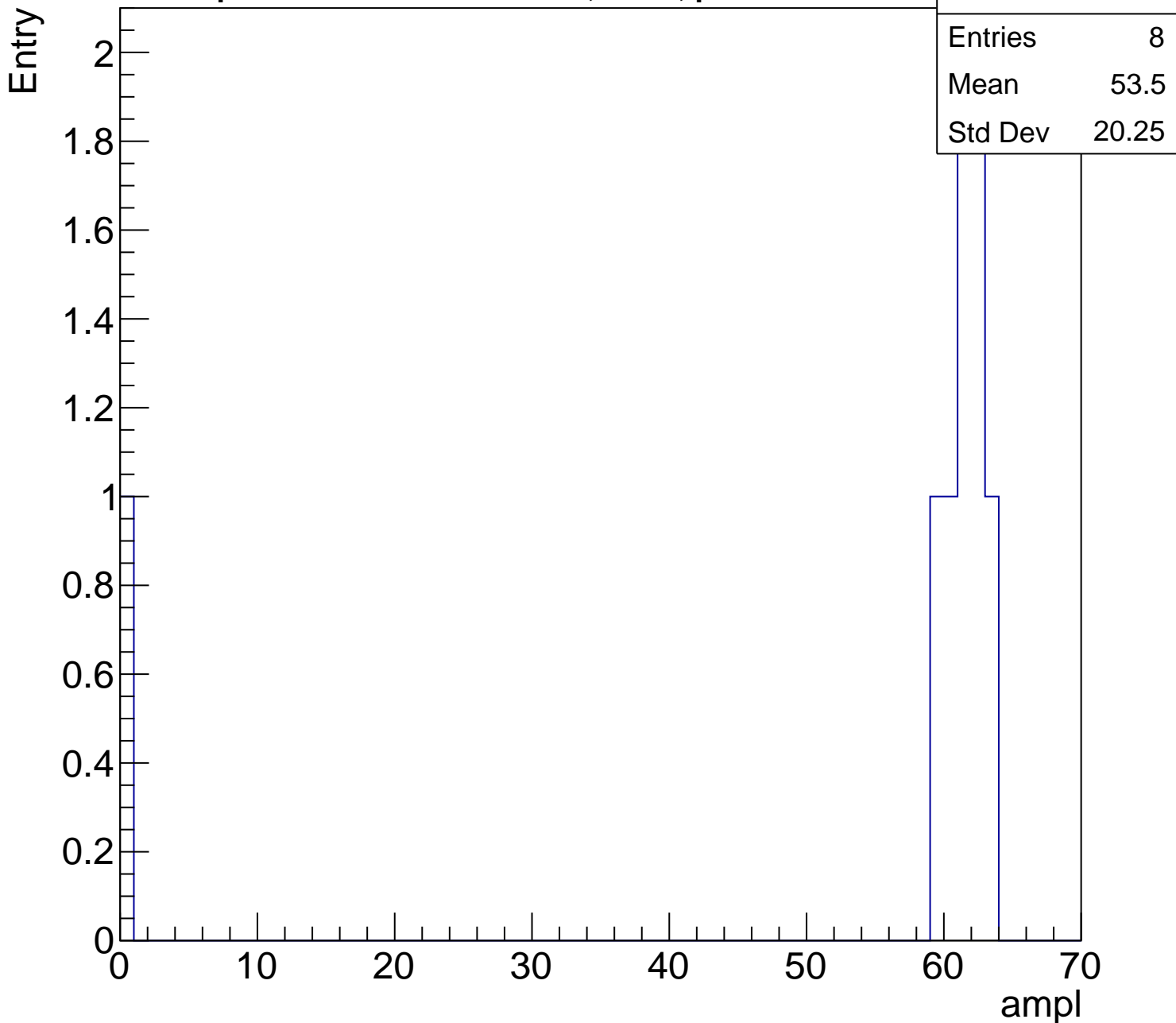
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	8
Mean	53.5
Std Dev	20.25

0 10 20 30 40 50 60 70

ampl





# B1L100S, U2-ch29, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	2
Mean	10
Std Dev	10

# B1L100S, U2-ch30, adc0

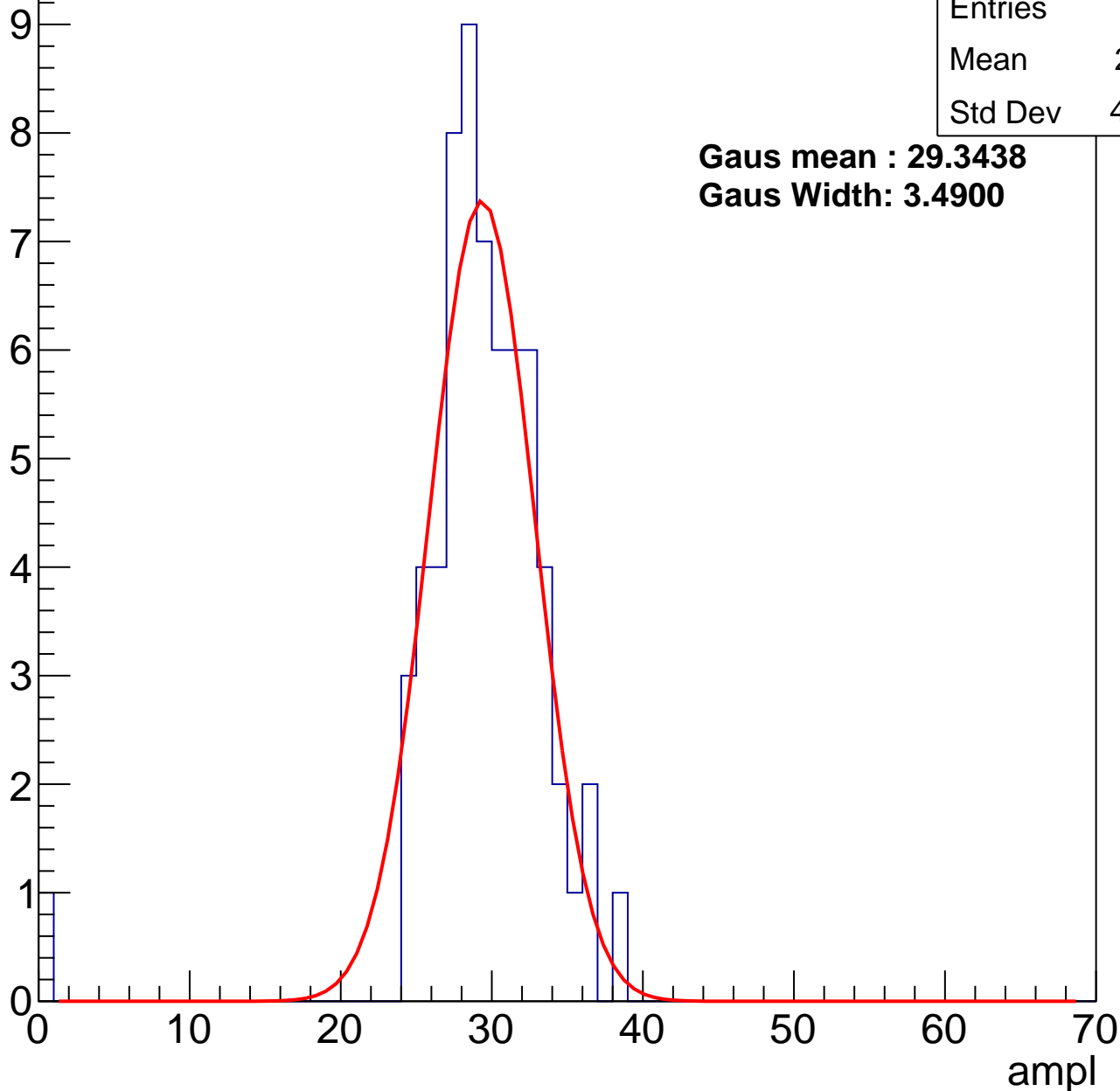
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	64
Mean	28.91
Std Dev	4.792

**Gaus mean : 29.3438**

**Gaus Width: 3.4900**



# B1L100S, U2-ch30, adc1

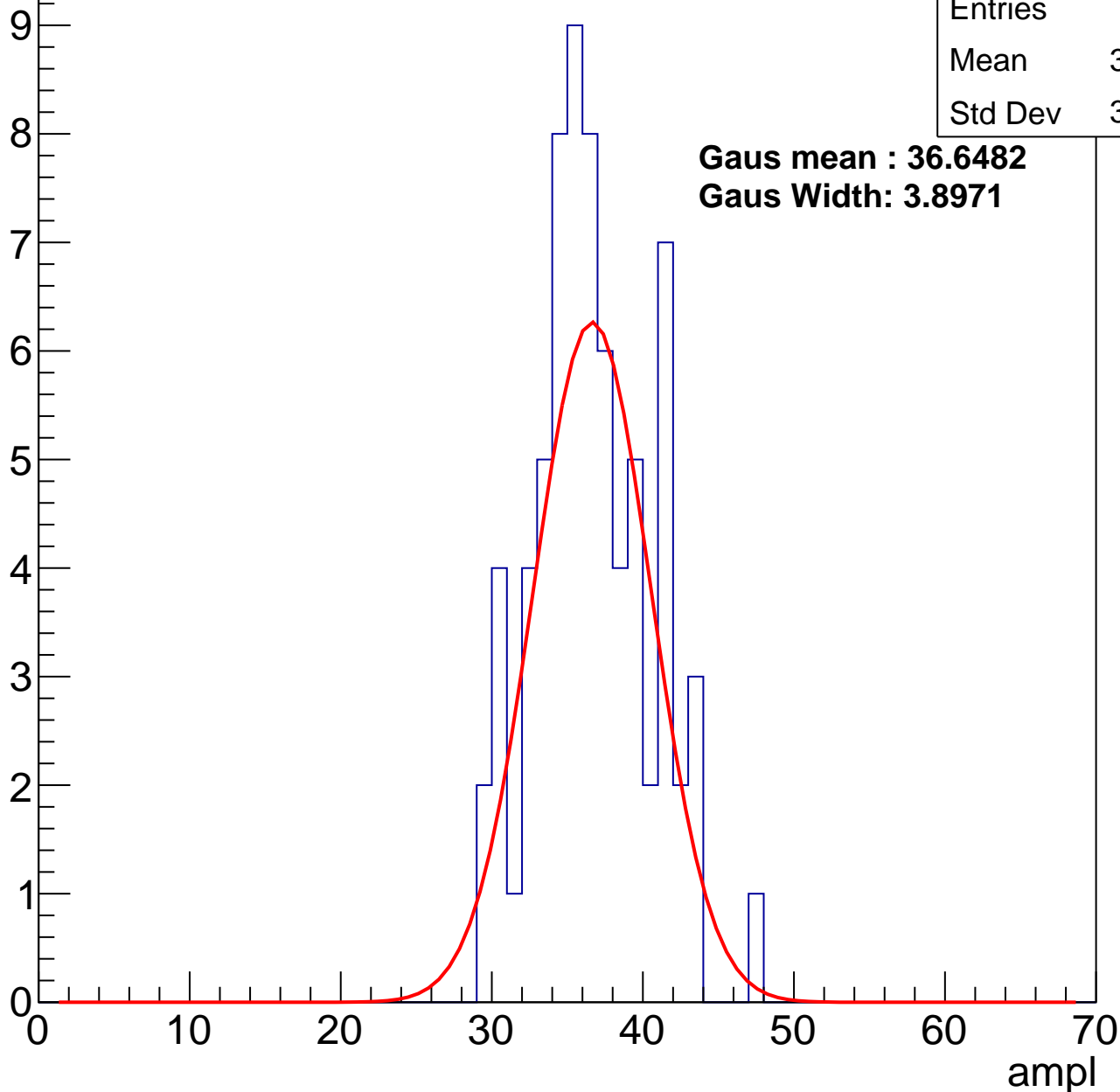
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	71
Mean	36.24
Std Dev	3.803

**Gaus mean : 36.6482**

**Gaus Width: 3.8971**



# B1L100S, U2-ch30, adc2

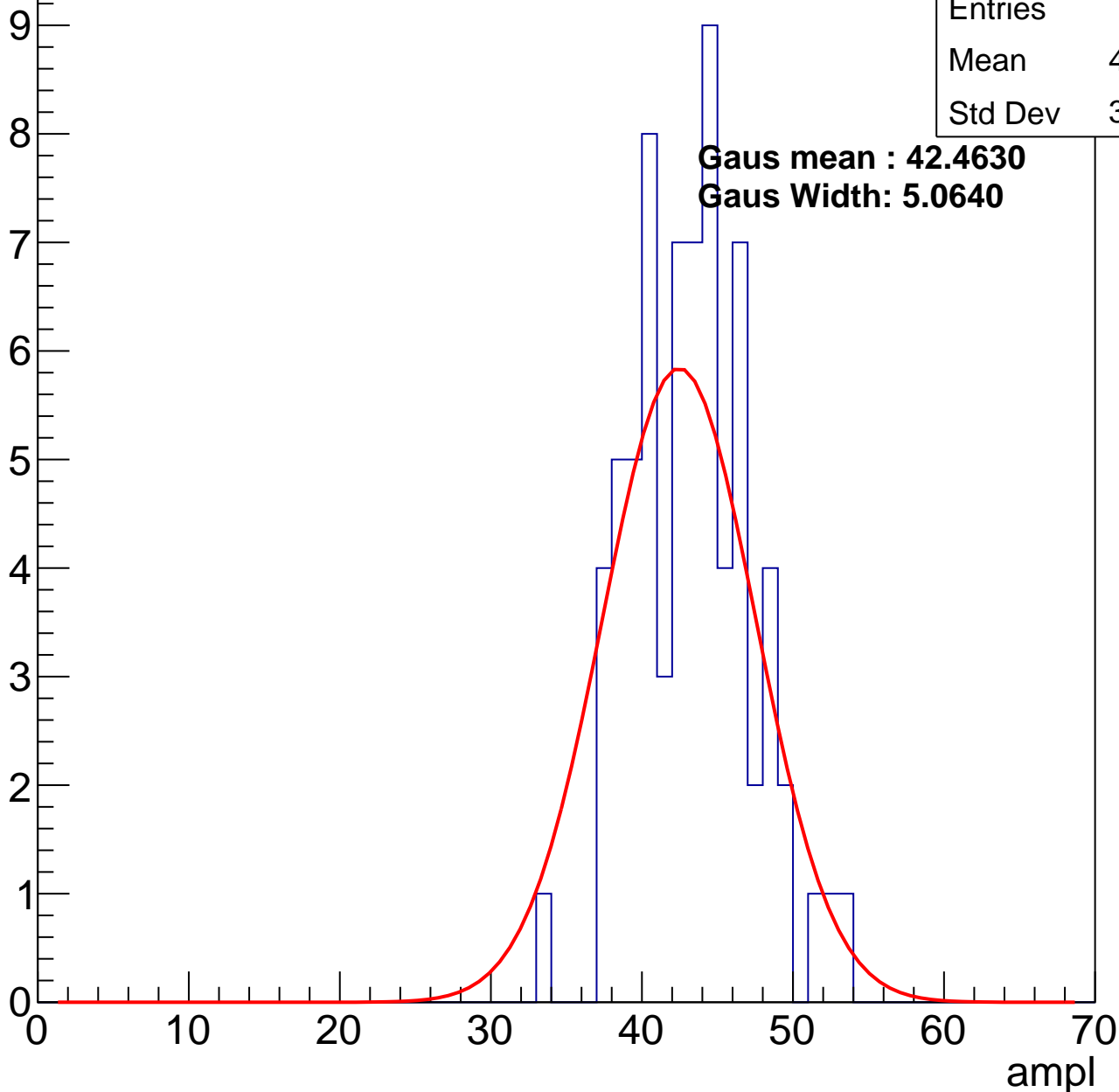
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	71
Mean	42.85
Std Dev	3.892

**Gaus mean : 42.4630**

**Gaus Width: 5.0640**

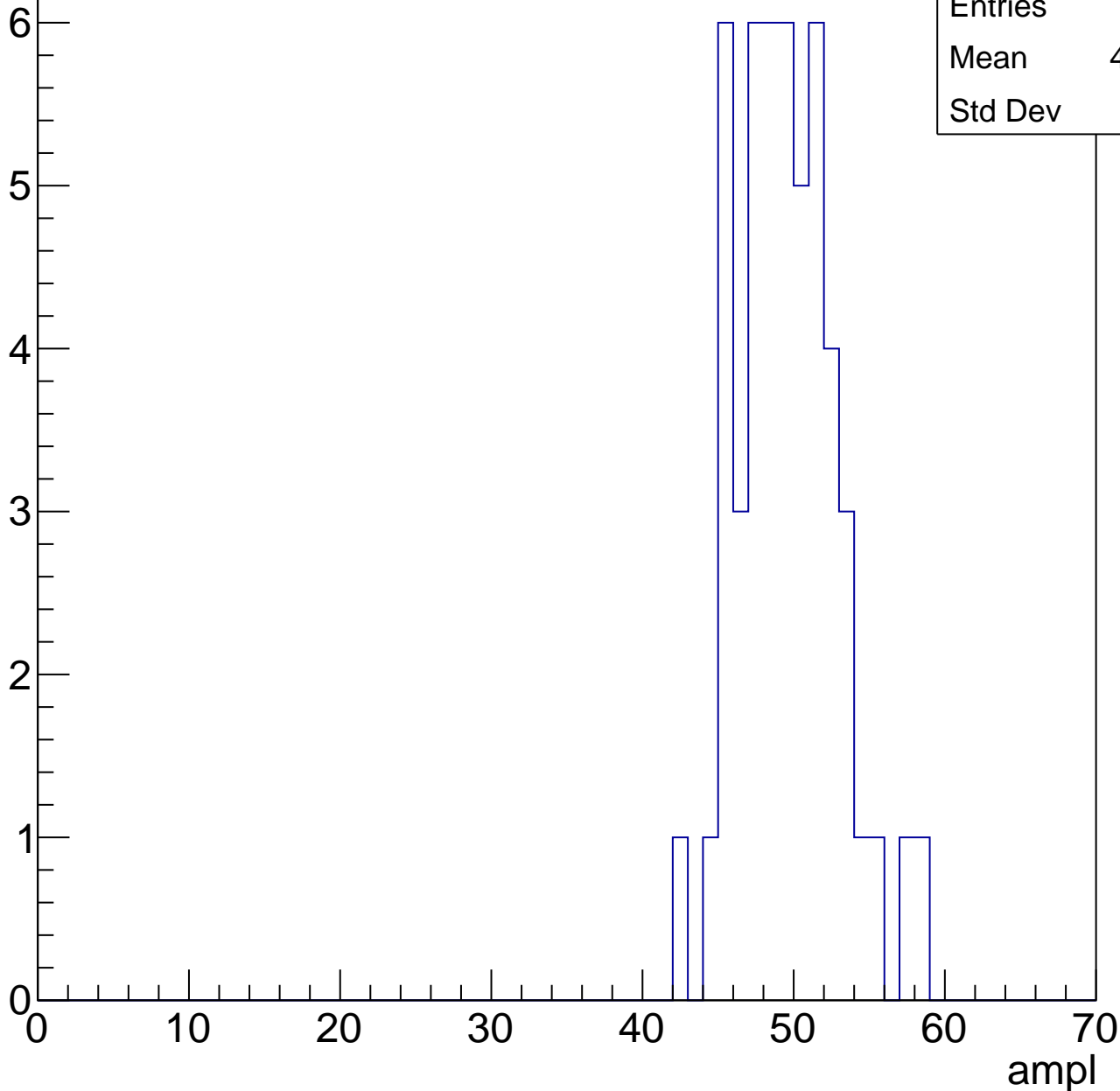


# B1L100S, U2-ch30, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

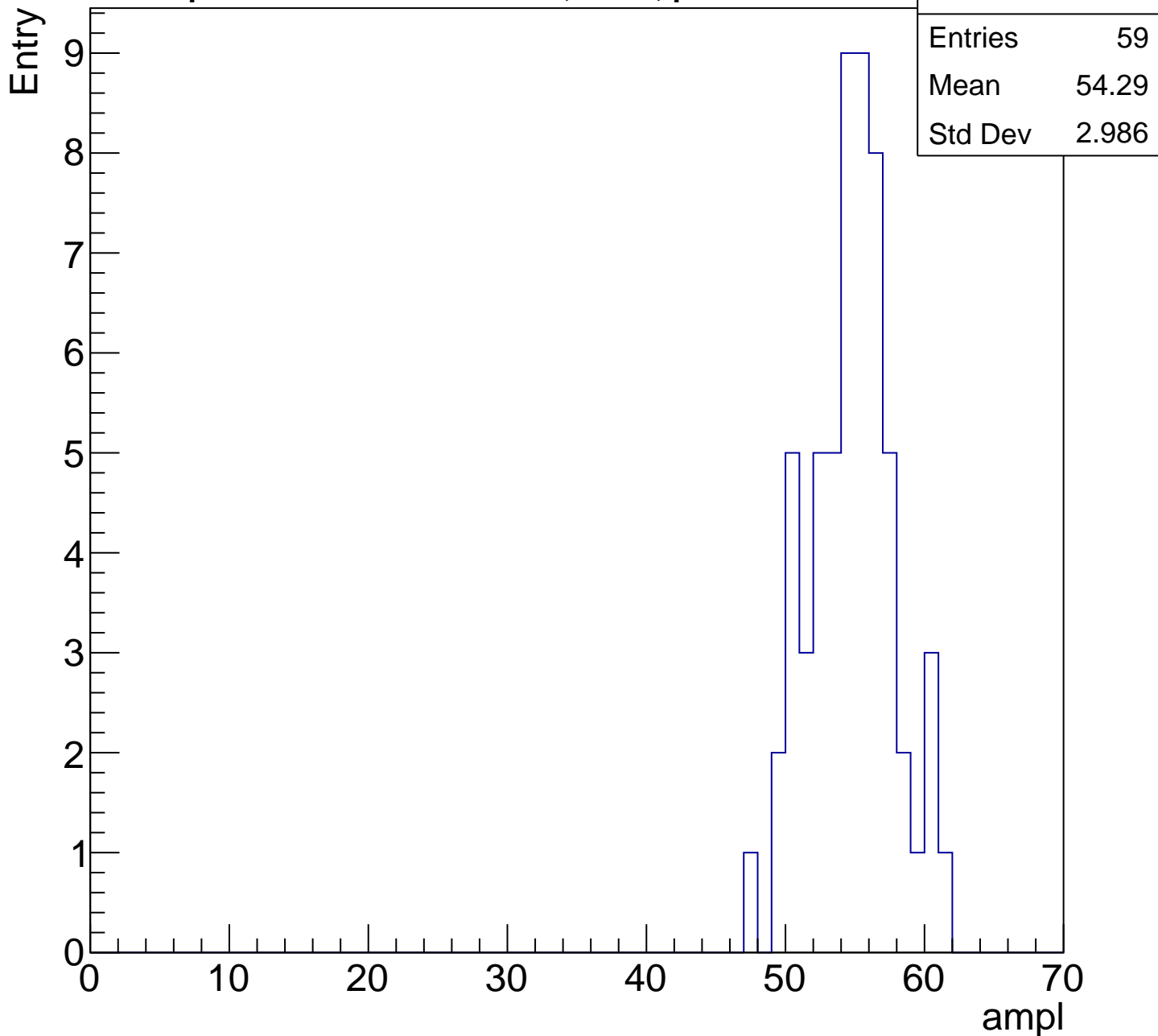
Entry

Entries	51
Mean	49.12
Std Dev	3.27



# B1L100S, U2-ch30, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

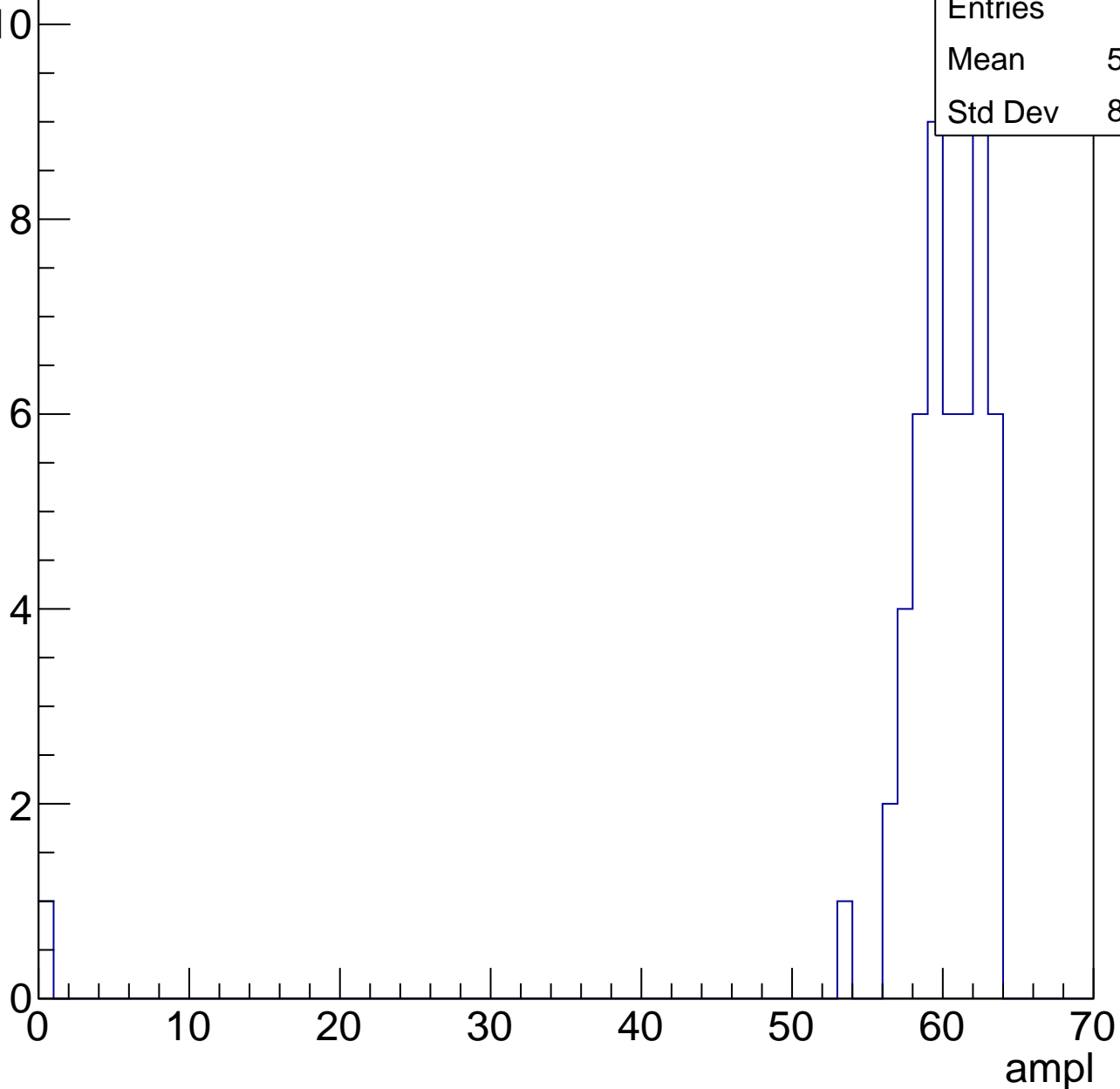


# B1L100S, U2-ch30, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

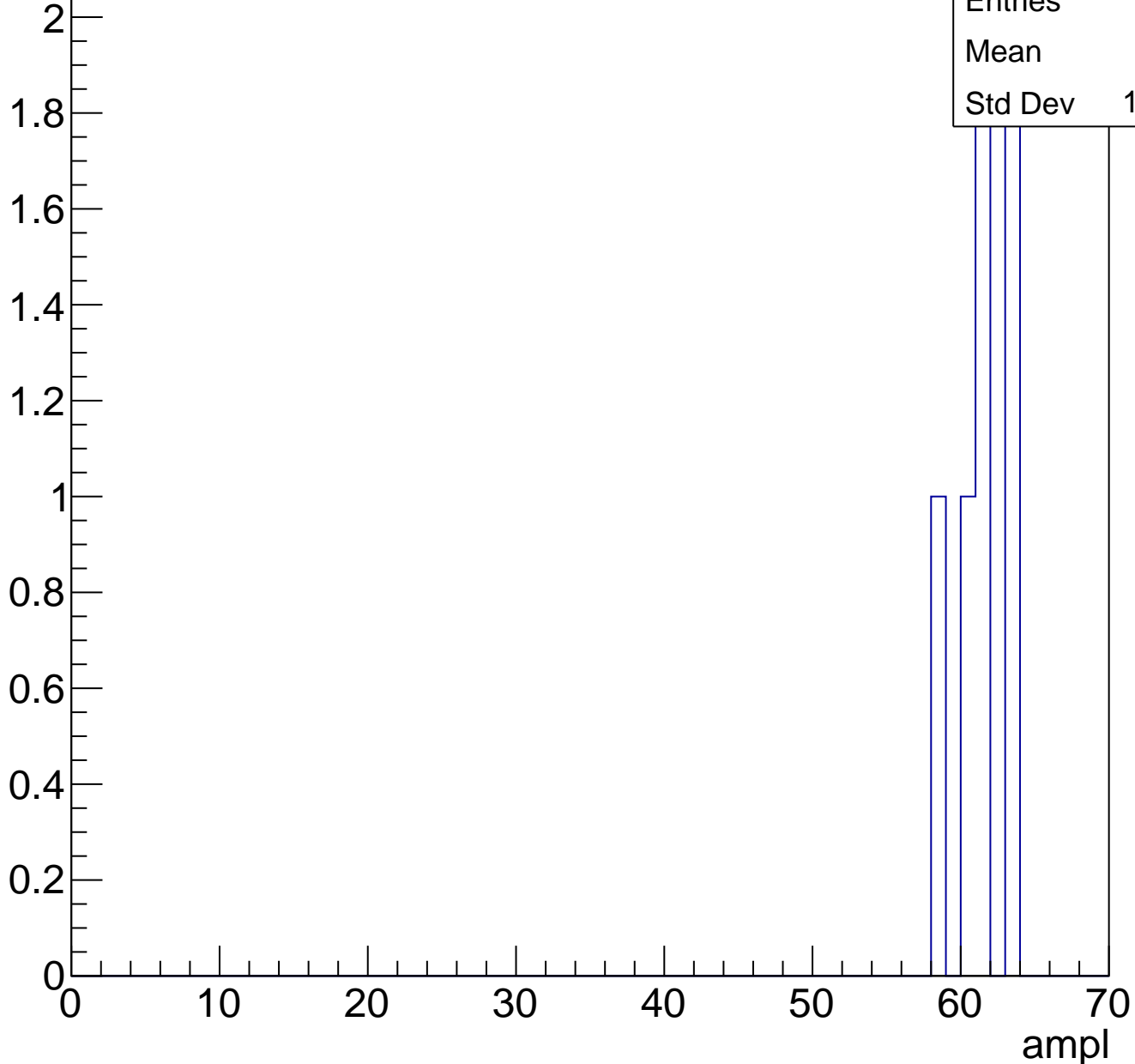
Entries	51
Mean	58.75
Std Dev	8.597



# B1L100S, U2-ch30, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

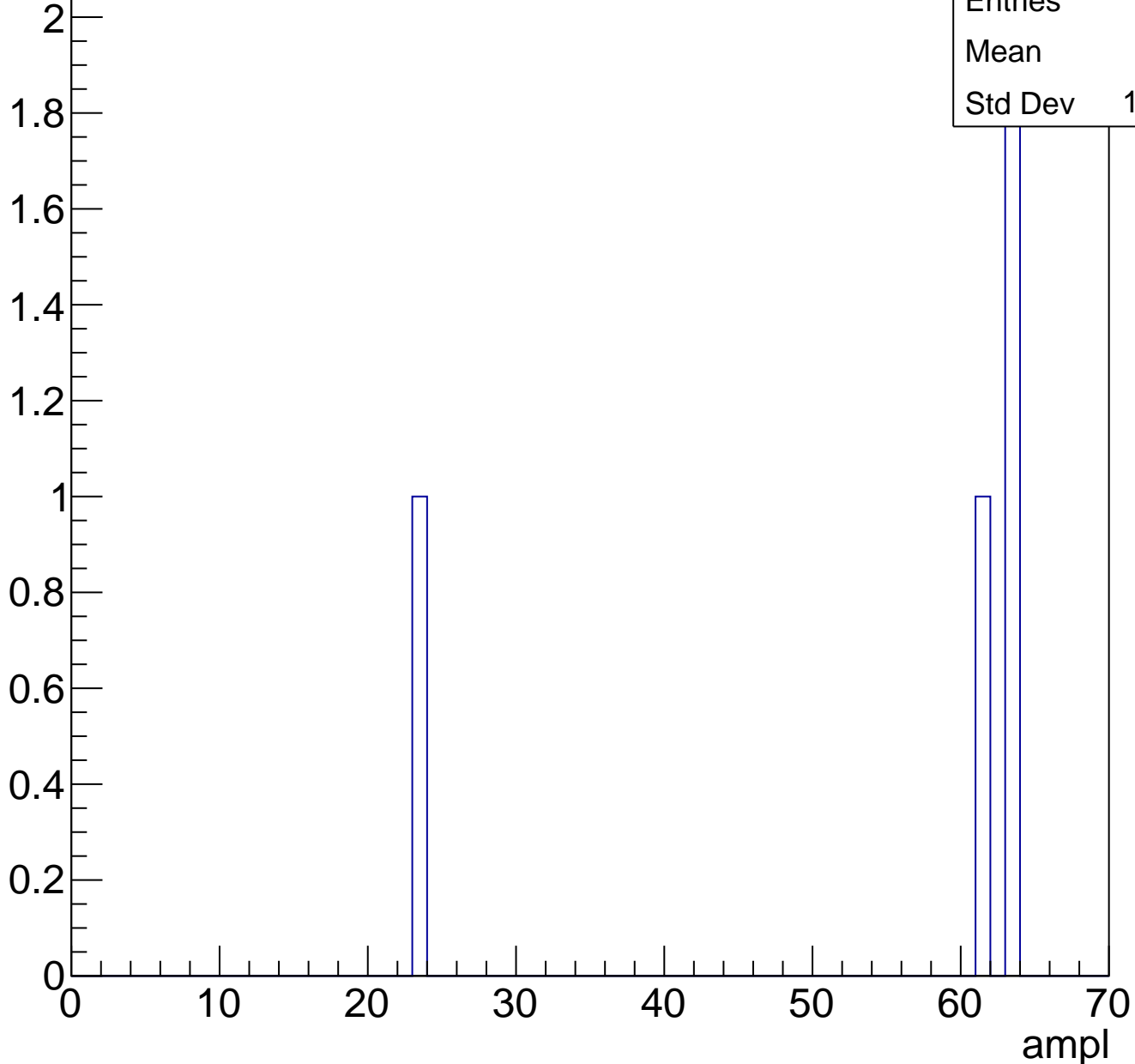




# B1L100S, U2-ch30, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	4
Mean	52.5
Std Dev	17.05

# B1L100S, U2-ch31, adc0

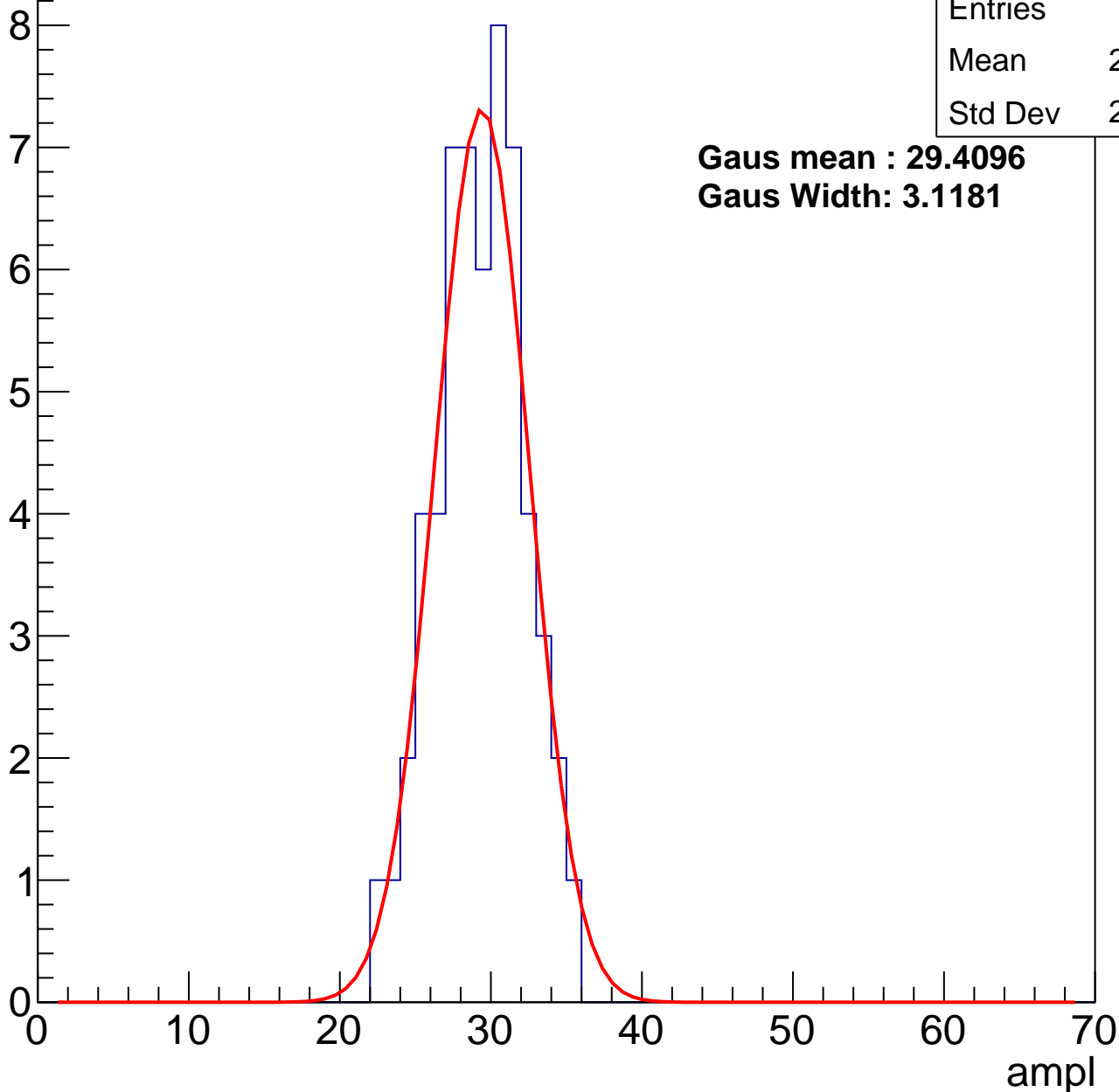
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	57
Mean	28.82
Std Dev	2.884

**Gaus mean : 29.4096**

**Gaus Width: 3.1181**



# B1L100S, U2-ch31, adc1

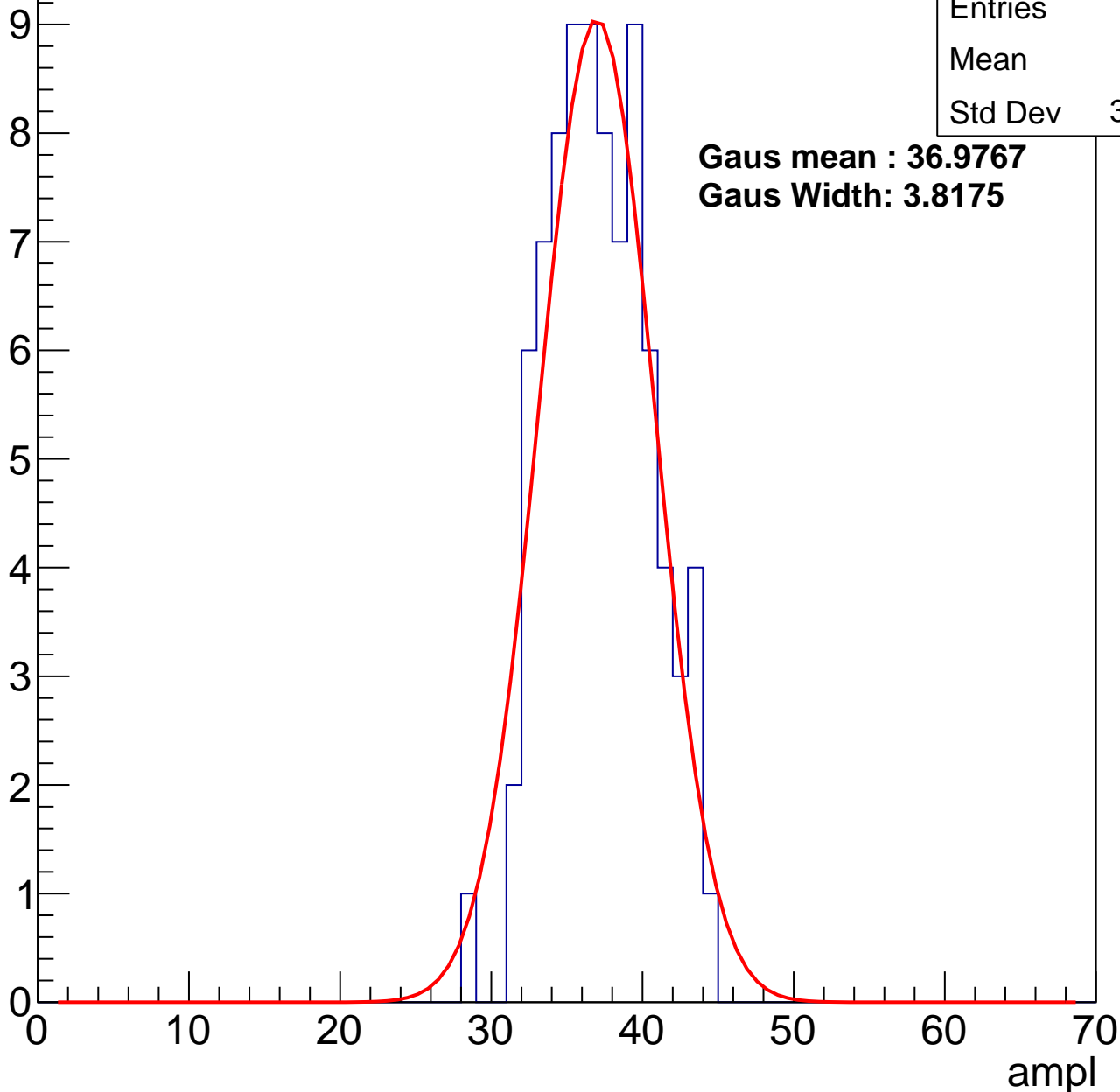
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	84
Mean	36.7
Std Dev	3.369

**Gaus mean : 36.9767**

**Gaus Width: 3.8175**



# B1L100S, U2-ch31, adc2

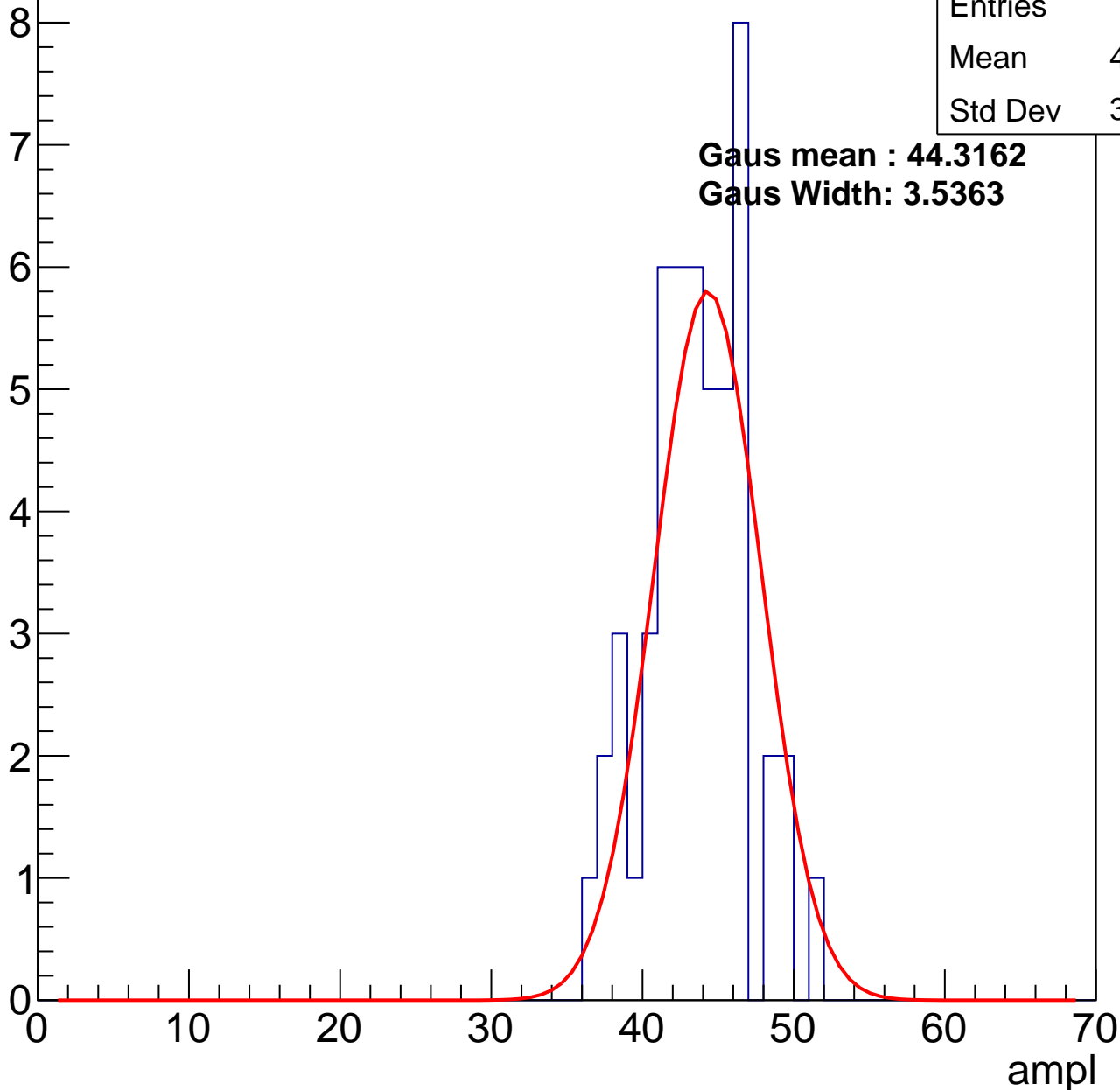
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	51
Mean	43.08
Std Dev	3.289

**Gaus mean : 44.3162**

**Gaus Width: 3.5363**

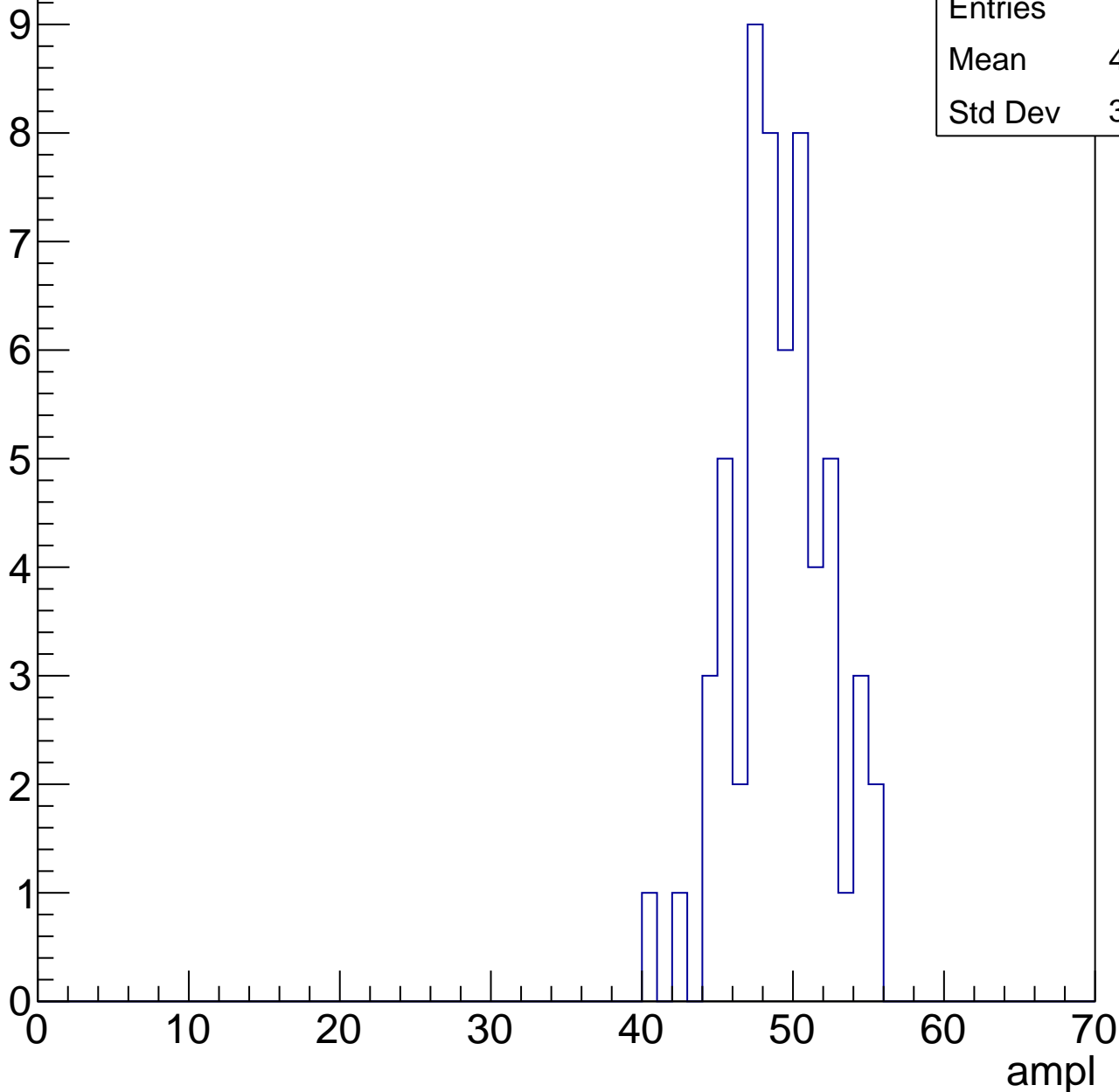


# B1L100S, U2-ch31, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	58
Mean	48.64
Std Dev	3.139

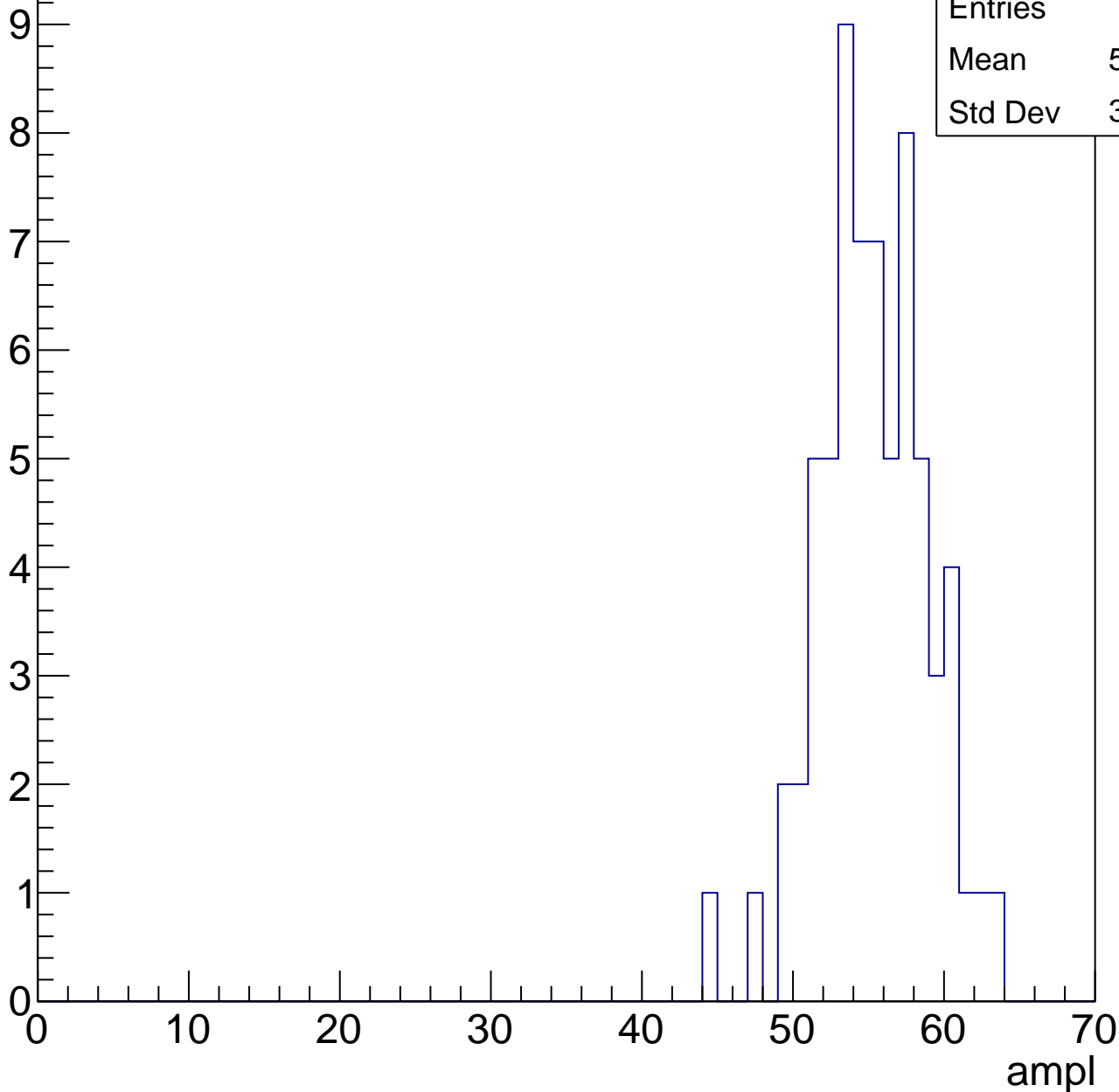


# B1L100S, U2-ch31, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	67
Mean	54.82
Std Dev	3.566



# B1L100S, U2-ch31, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	48
Mean	60.02
Std Dev	2.222

ampl

0 10 20 30 40 50 60 70

0

1

2

3

4

5

6

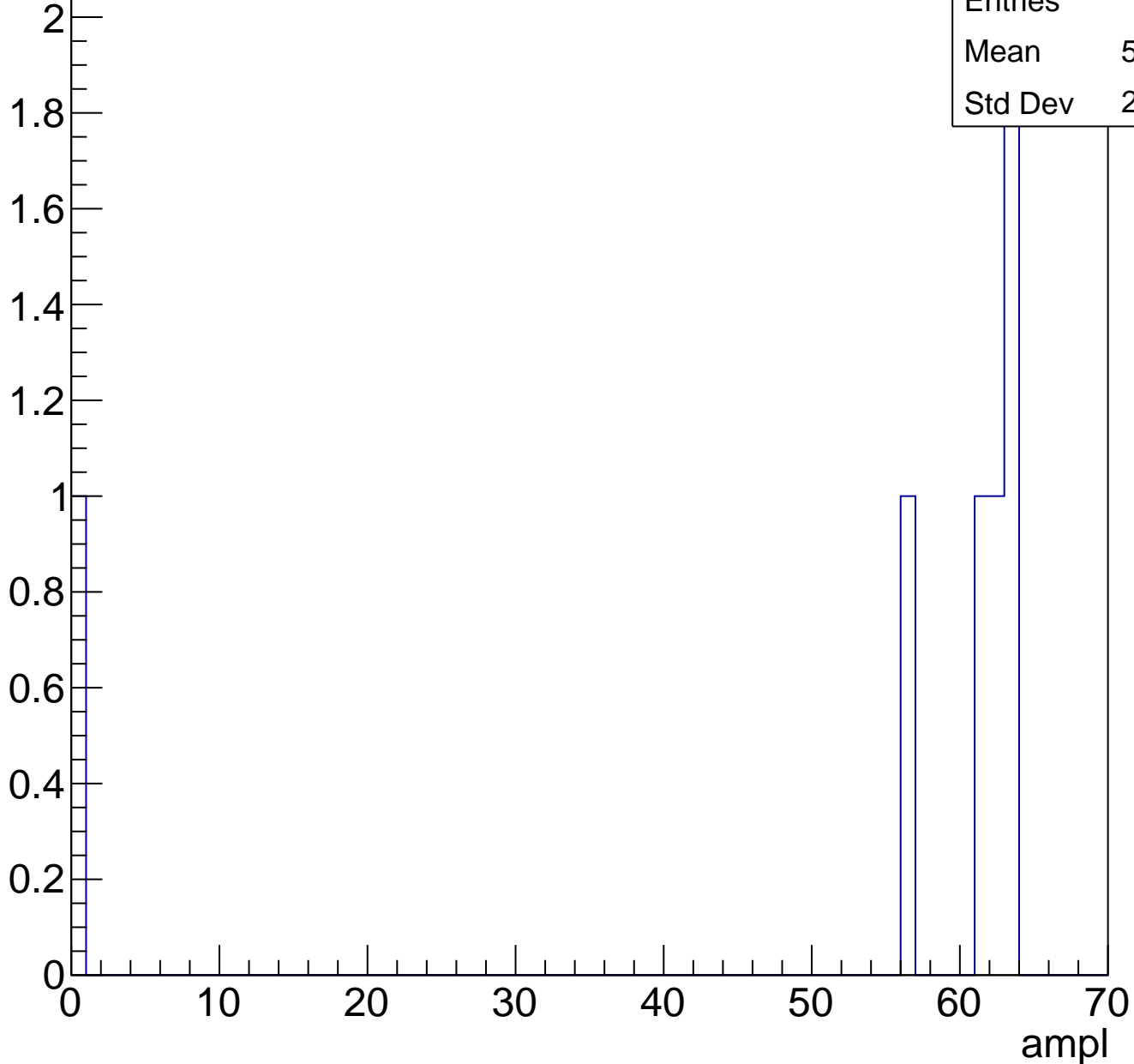
7

8

# B1L100S, U2-ch31, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry





# B1L100S, U2-ch31, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	3
Mean	0
Std Dev	0

# B1L100S, U2-ch32, adc0

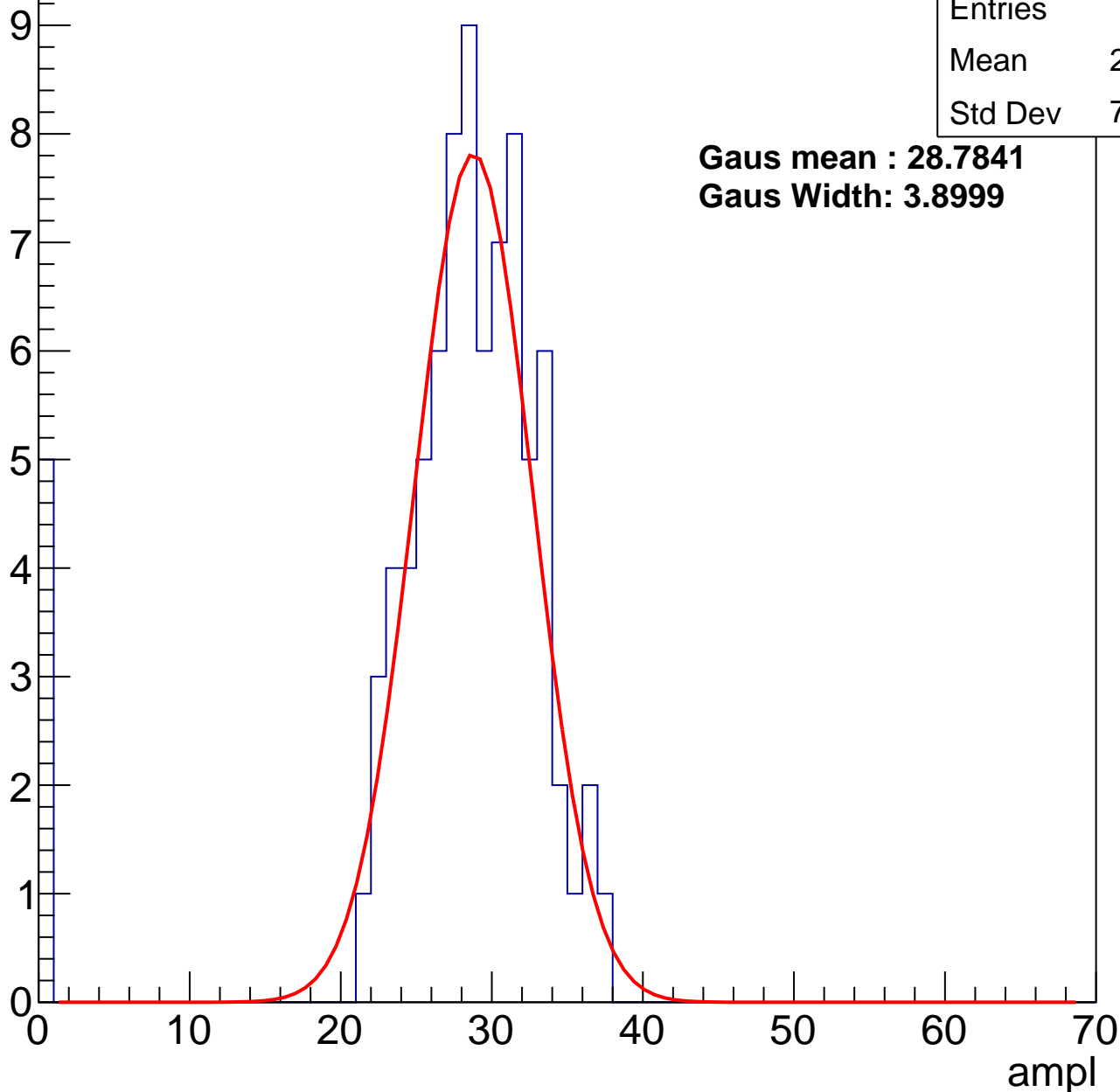
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	83
Mean	26.82
Std Dev	7.659

**Gaus mean : 28.7841**

**Gaus Width: 3.8999**



# B1L100S, U2-ch32, adc1

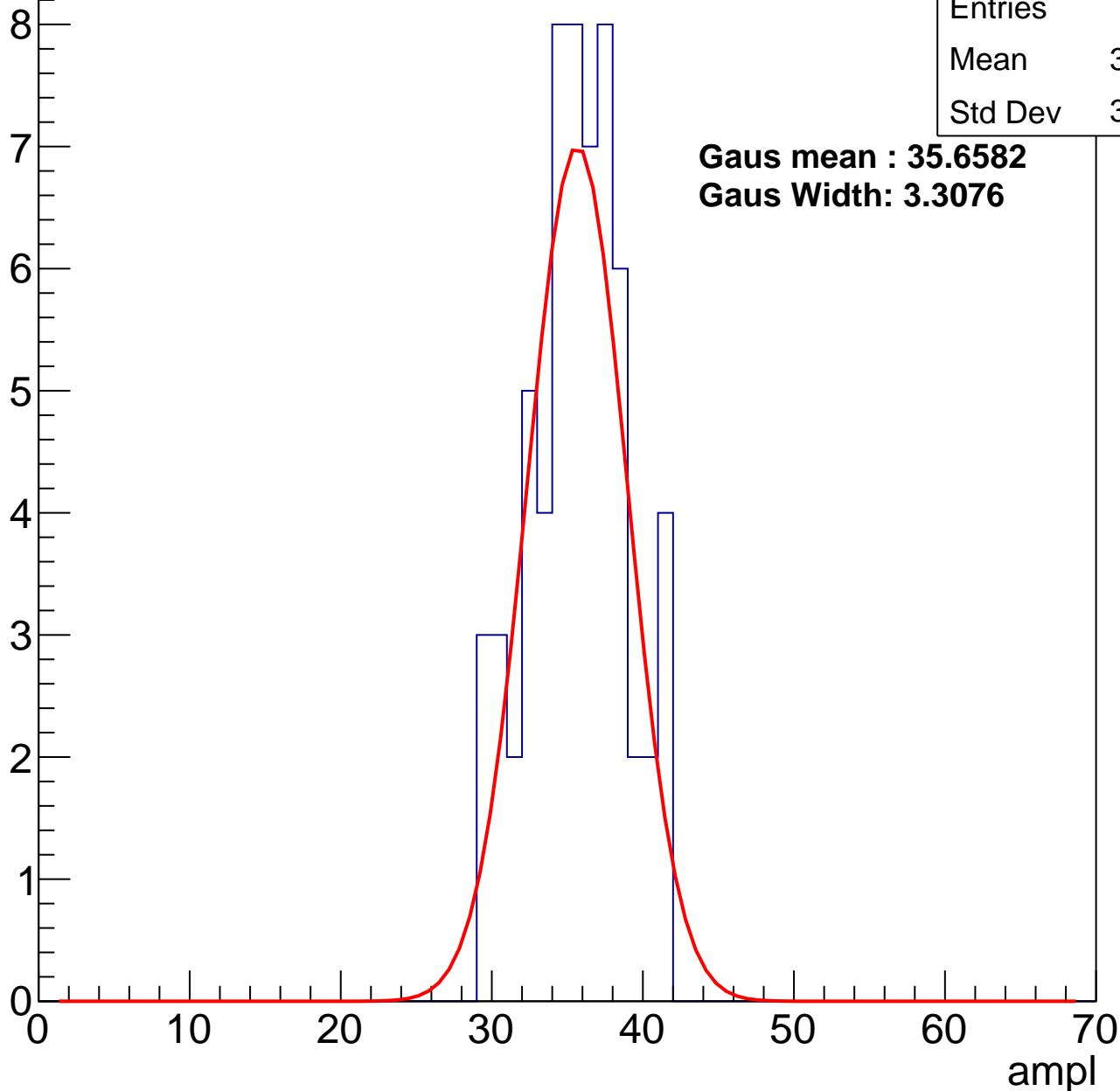
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	62
Mean	35.18
Std Dev	3.114

**Gaus mean : 35.6582**

**Gaus Width: 3.3076**



# B1L100S, U2-ch32, adc2

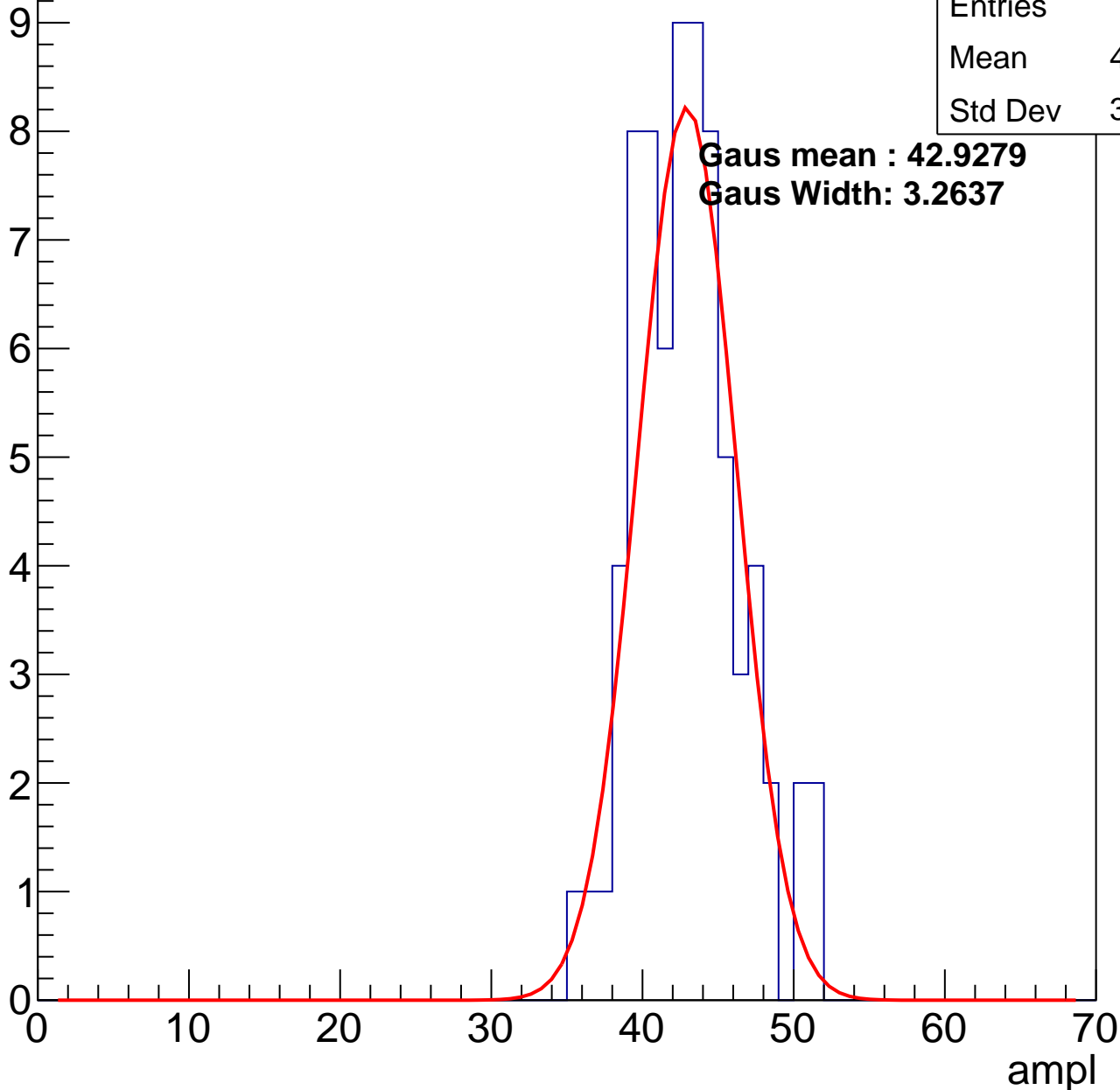
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	73
Mean	42.52
Std Dev	3.433

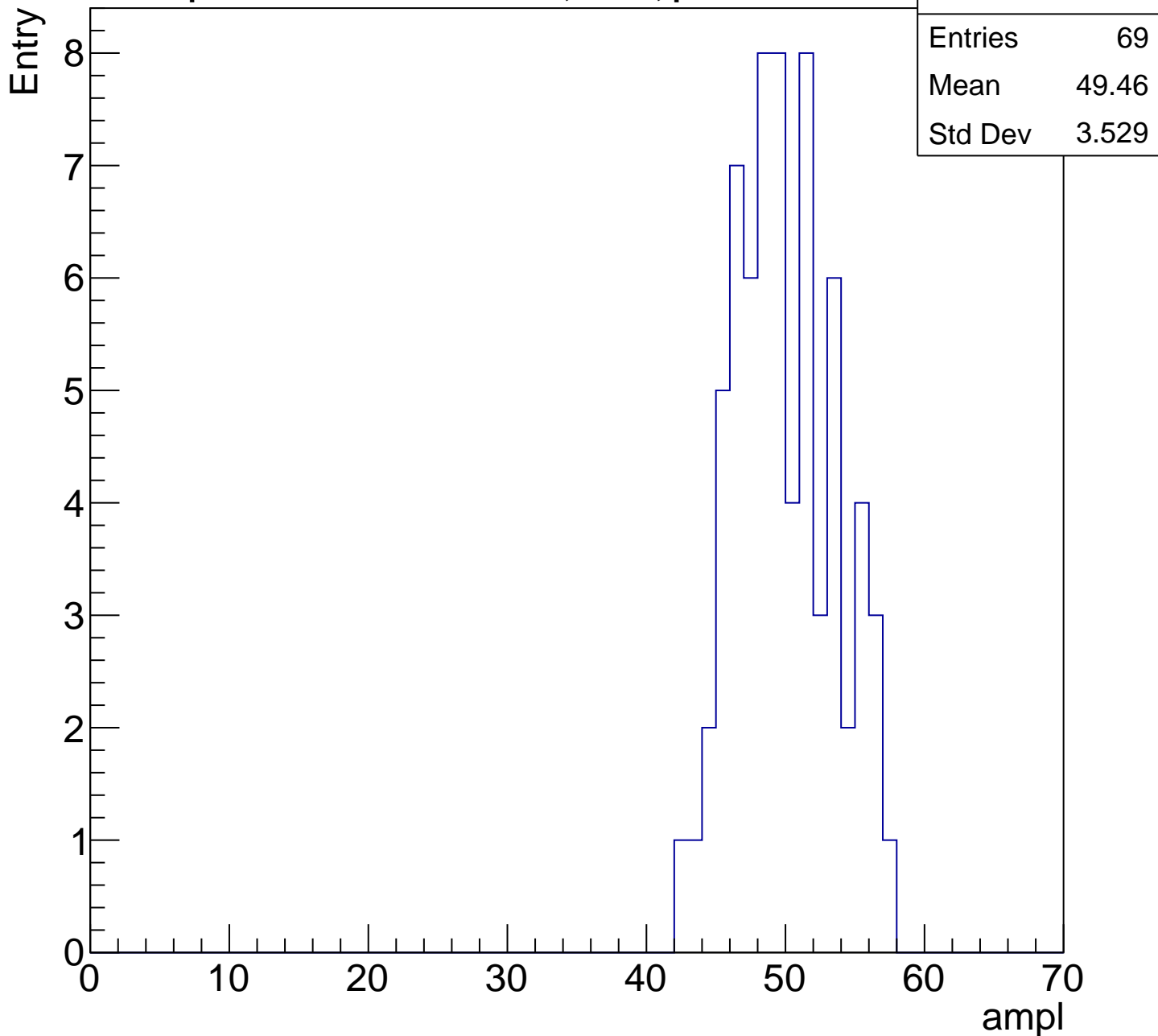
**Gaus mean : 42.9279**

**Gaus Width: 3.2637**



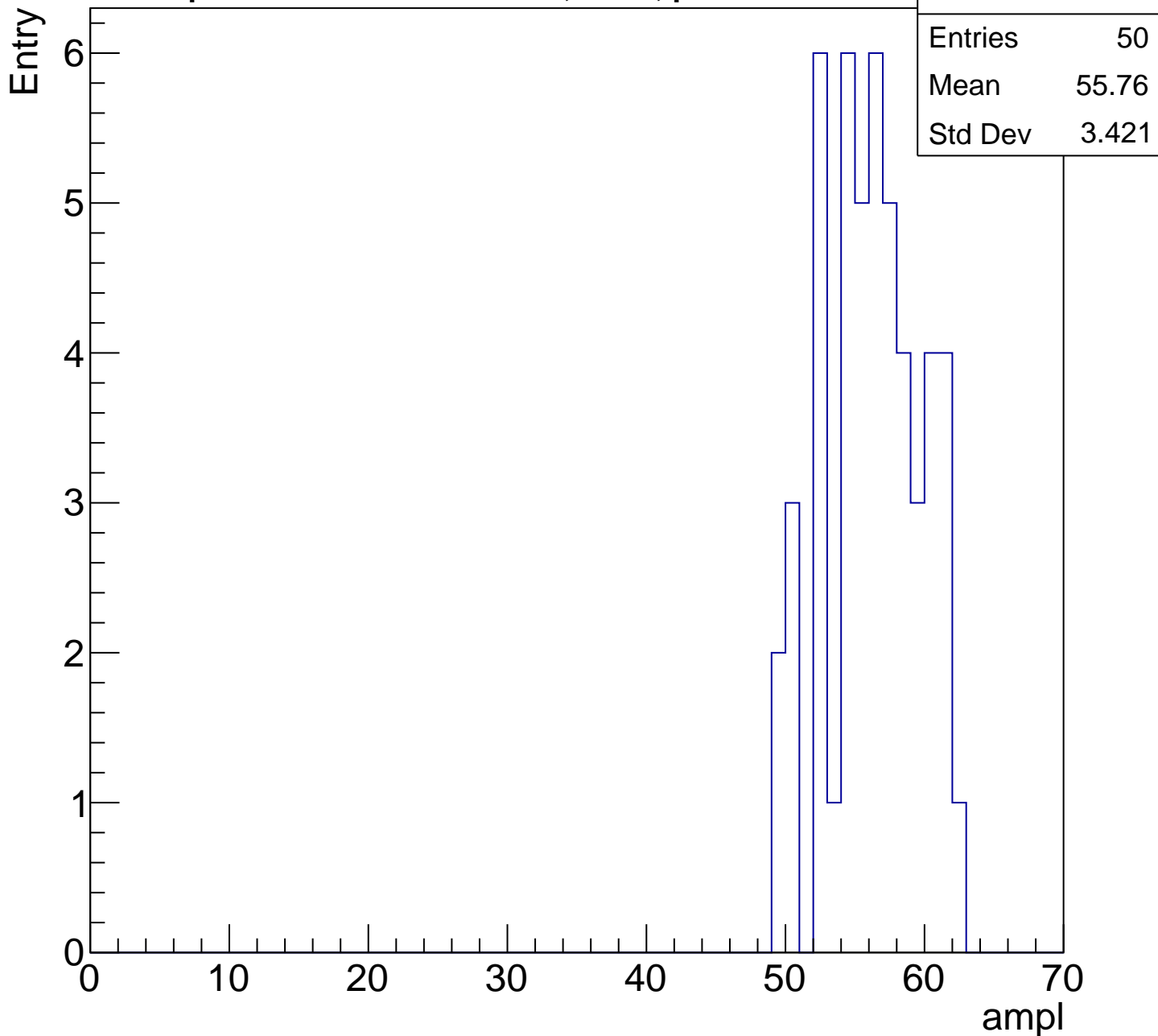
# B1L100S, U2-ch32, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2



# B1L100S, U2-ch32, adc4

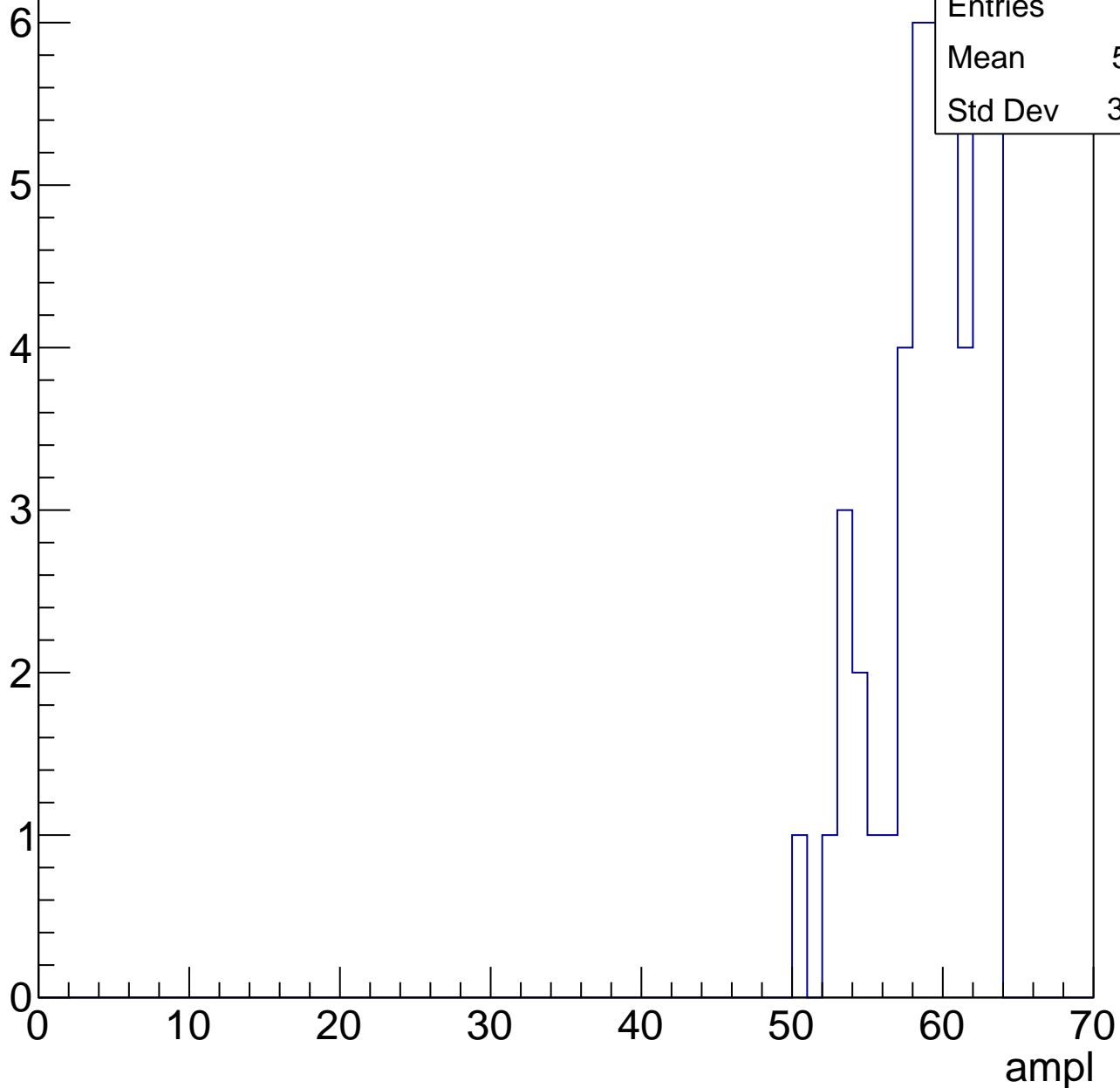
calib\_packv5\_042523\_0143.root, FC#4, port A2



# B1L100S, U2-ch32, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

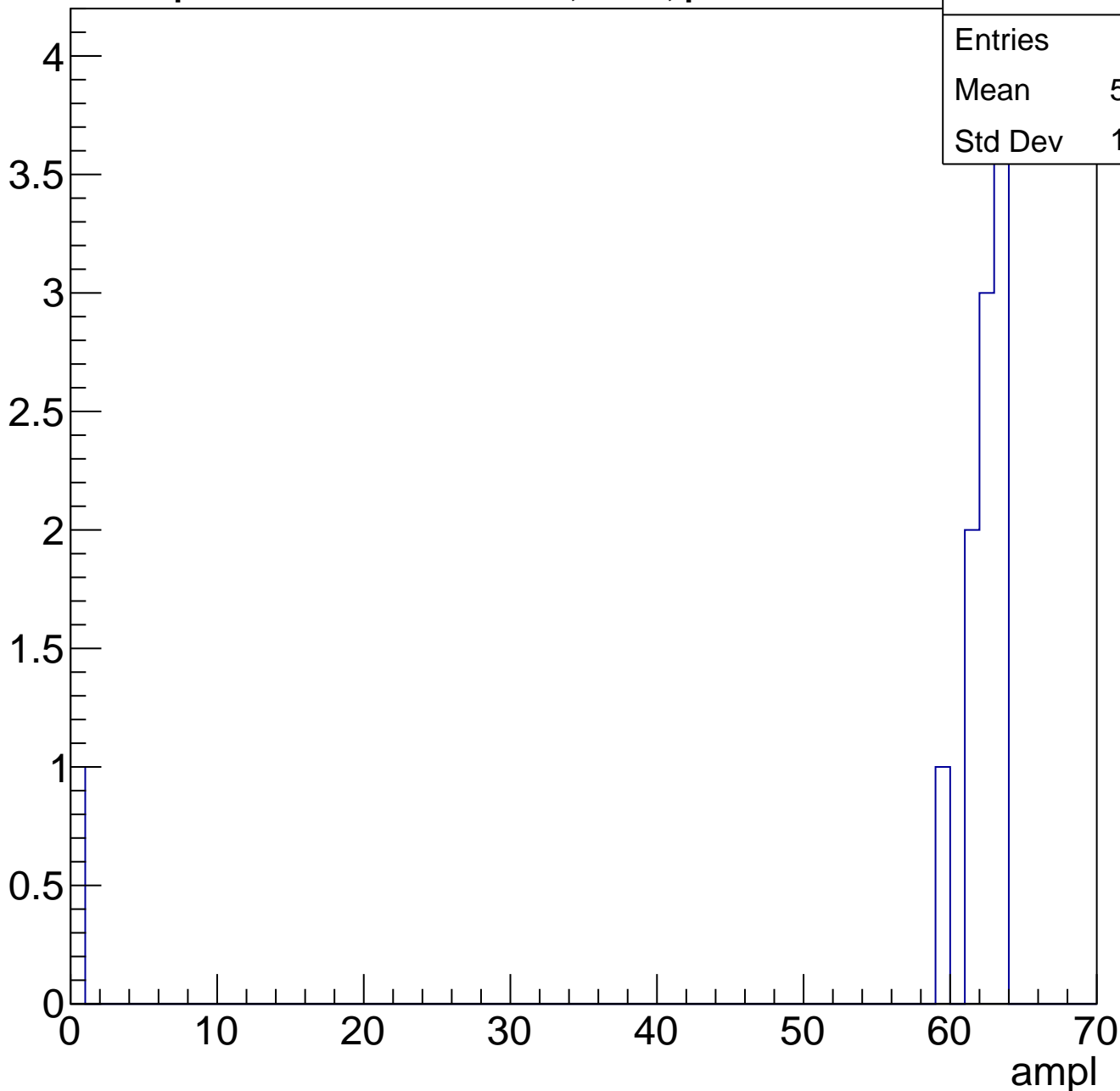
Entry



# B1L100S, U2-ch32, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry





# B1L100S, U2-ch32, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L100S, U2-ch33, adc0

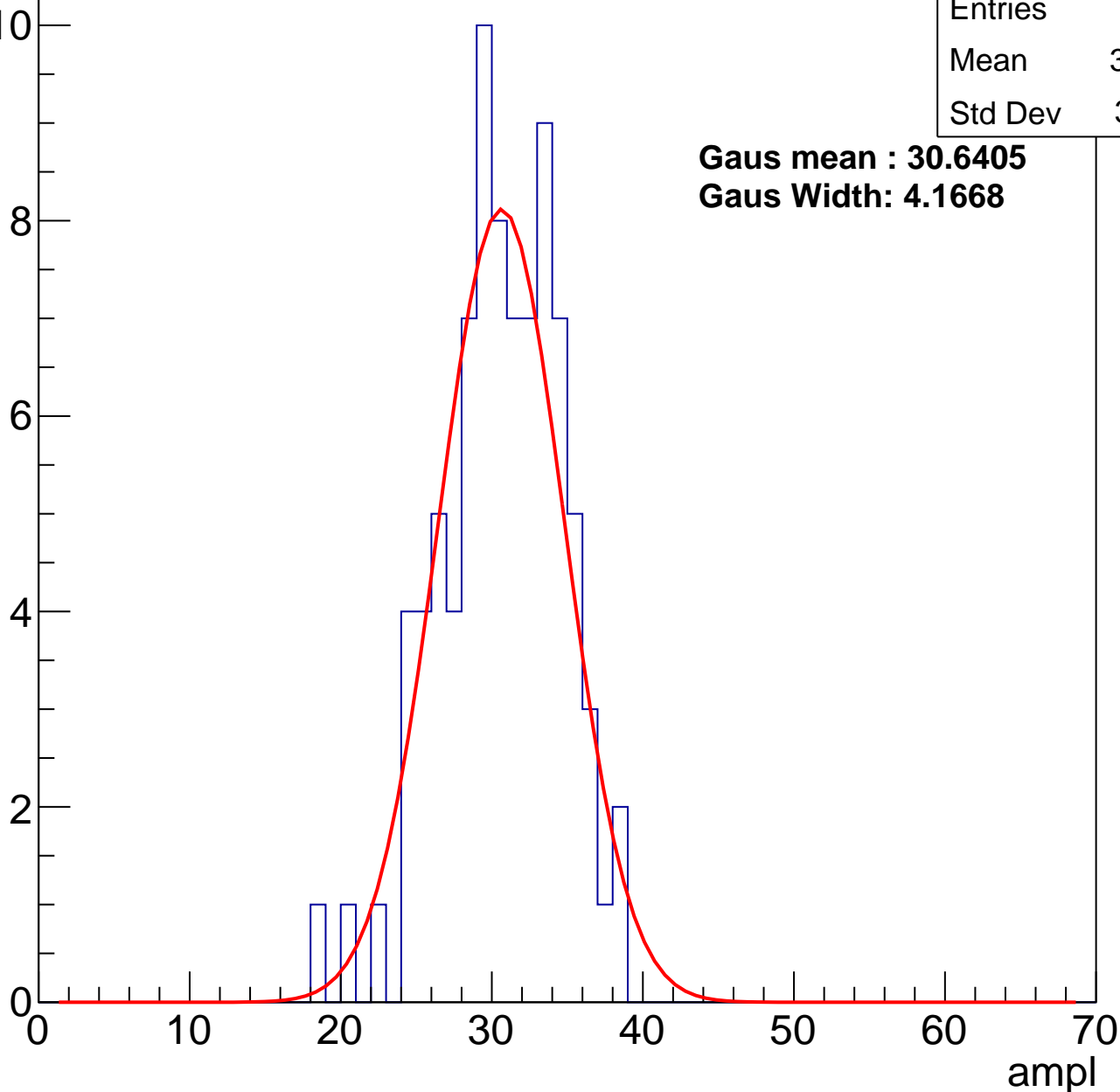
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	86
Mean	30.14
Std Dev	3.951

**Gaus mean : 30.6405**

**Gaus Width: 4.1668**



# B1L100S, U2-ch33, adc1

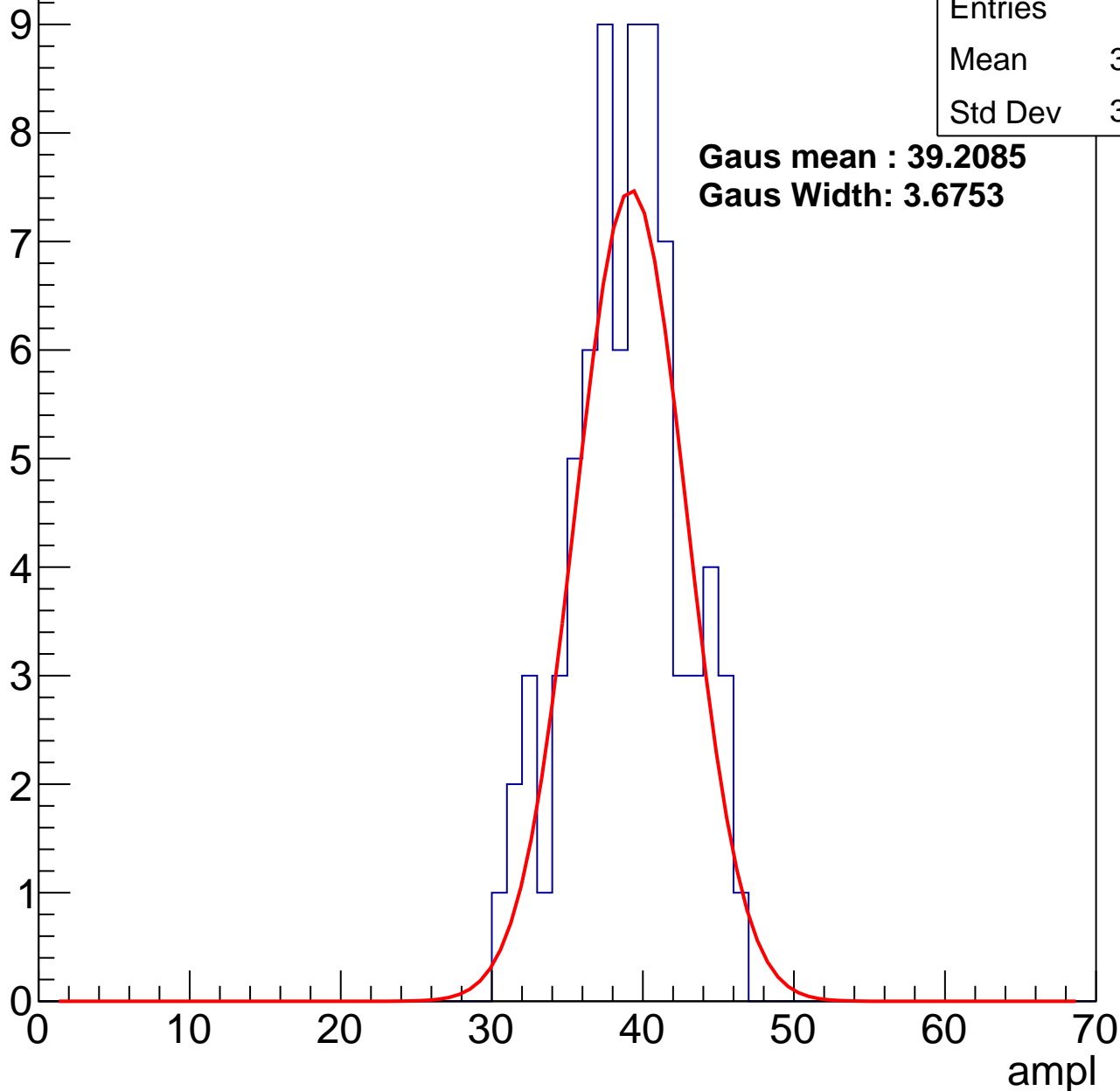
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	75
Mean	38.47
Std Dev	3.634

**Gaus mean : 39.2085**

**Gaus Width: 3.6753**



# B1L100S, U2-ch33, adc2

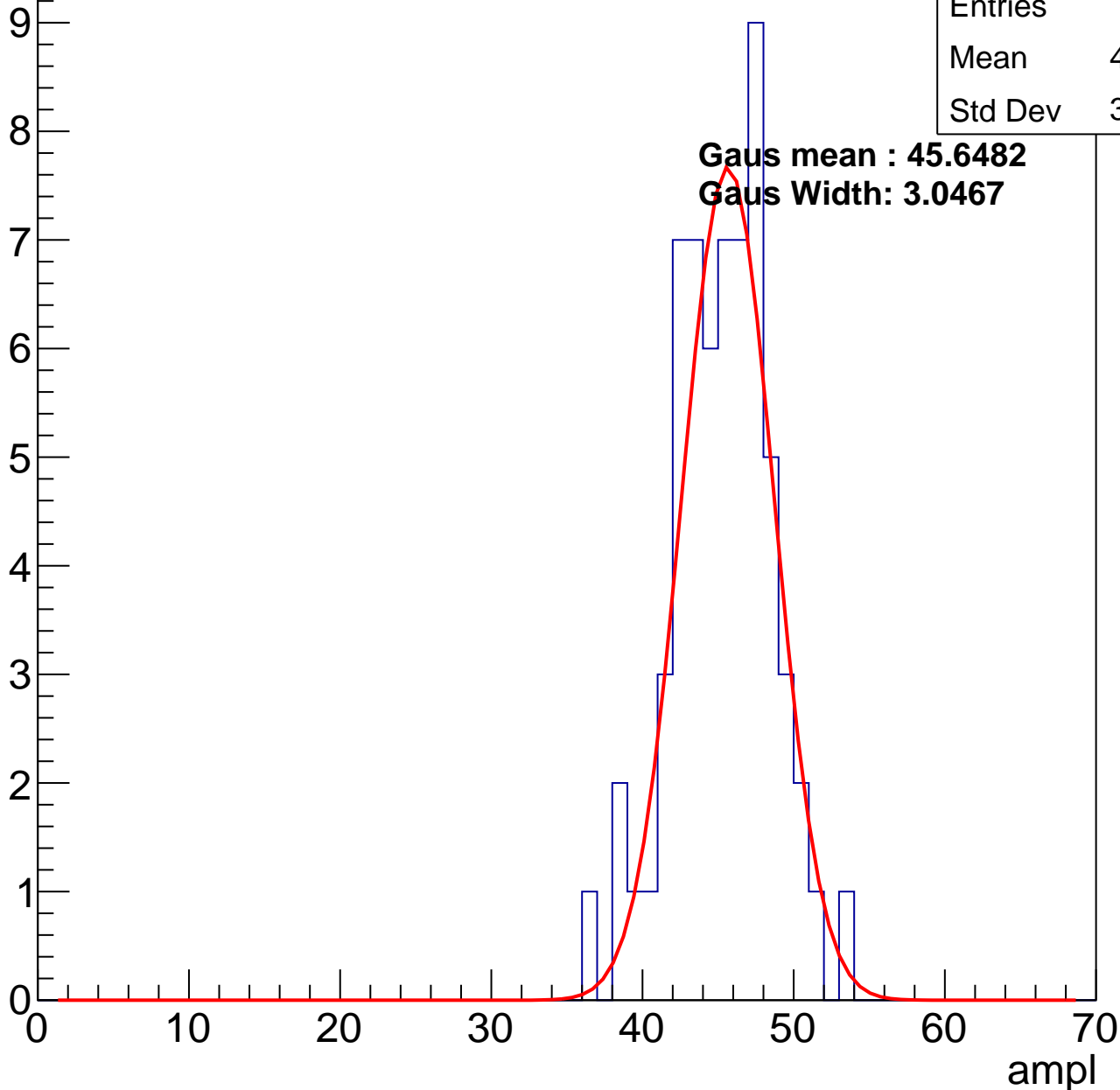
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	63
Mean	44.83
Std Dev	3.259

**Gaus mean : 45.6482**

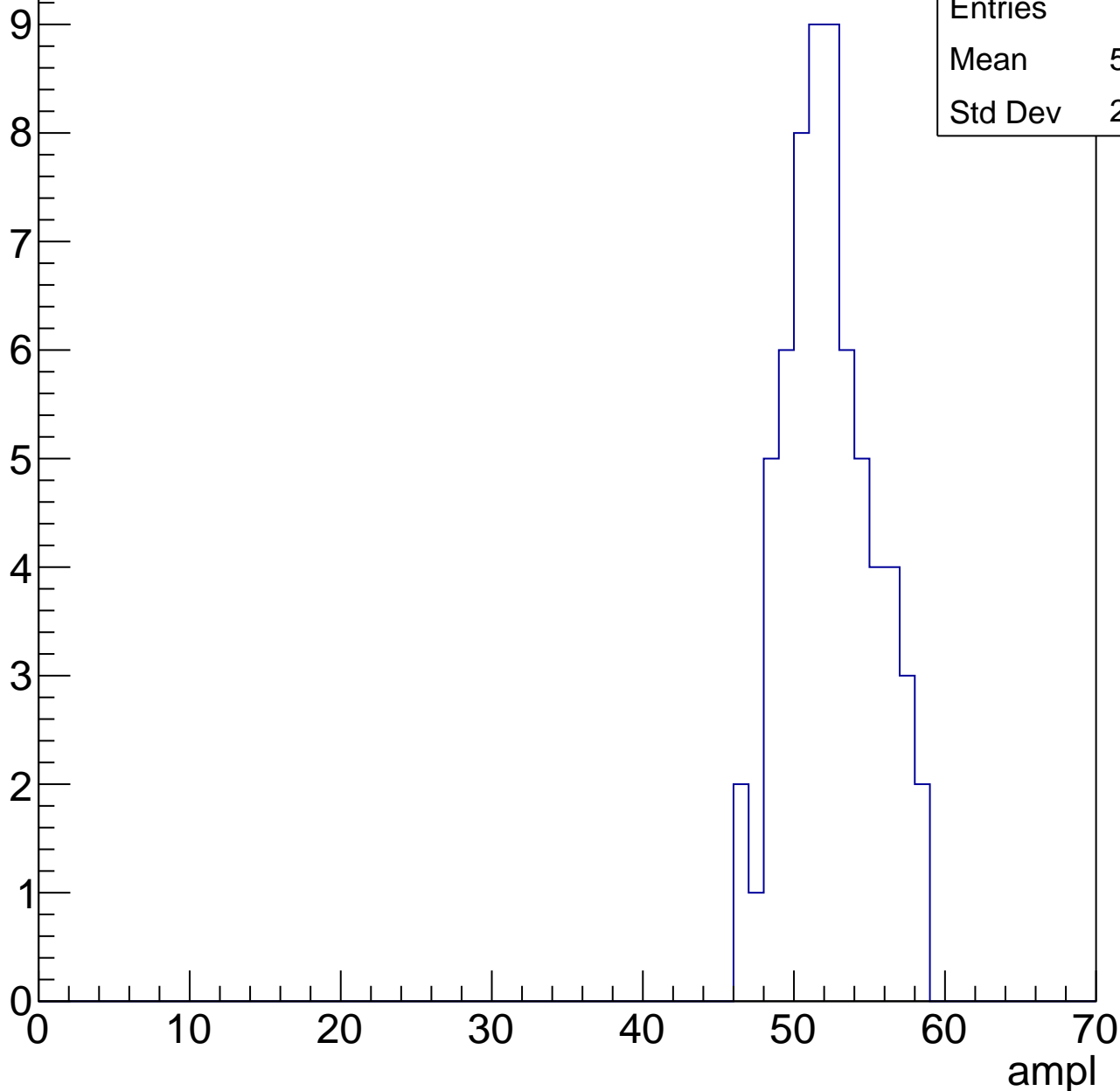
**Gaus Width: 3.0467**



# B1L100S, U2-ch33, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

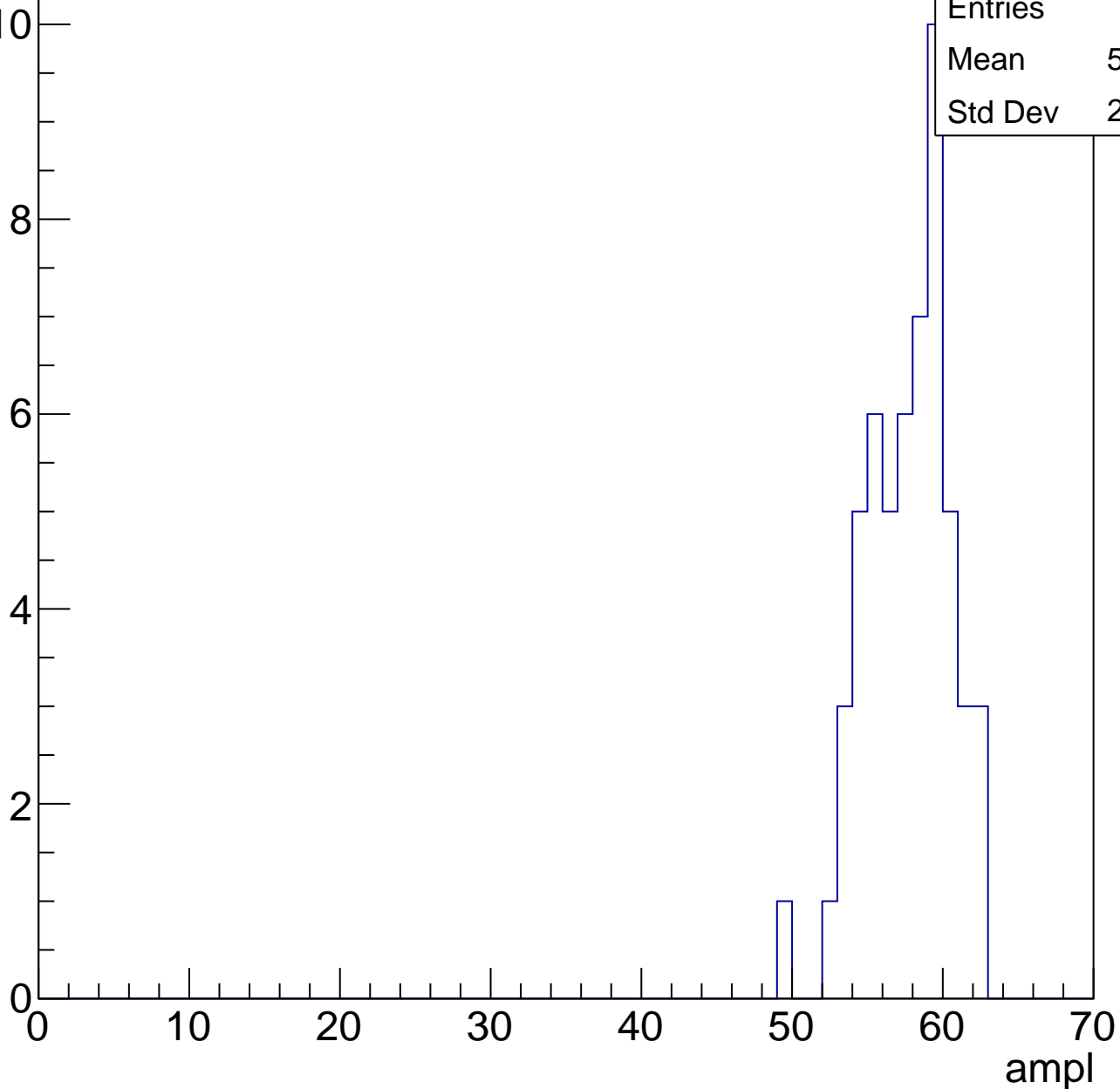


# B1L100S, U2-ch33, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	55
Mean	57.22
Std Dev	2.775

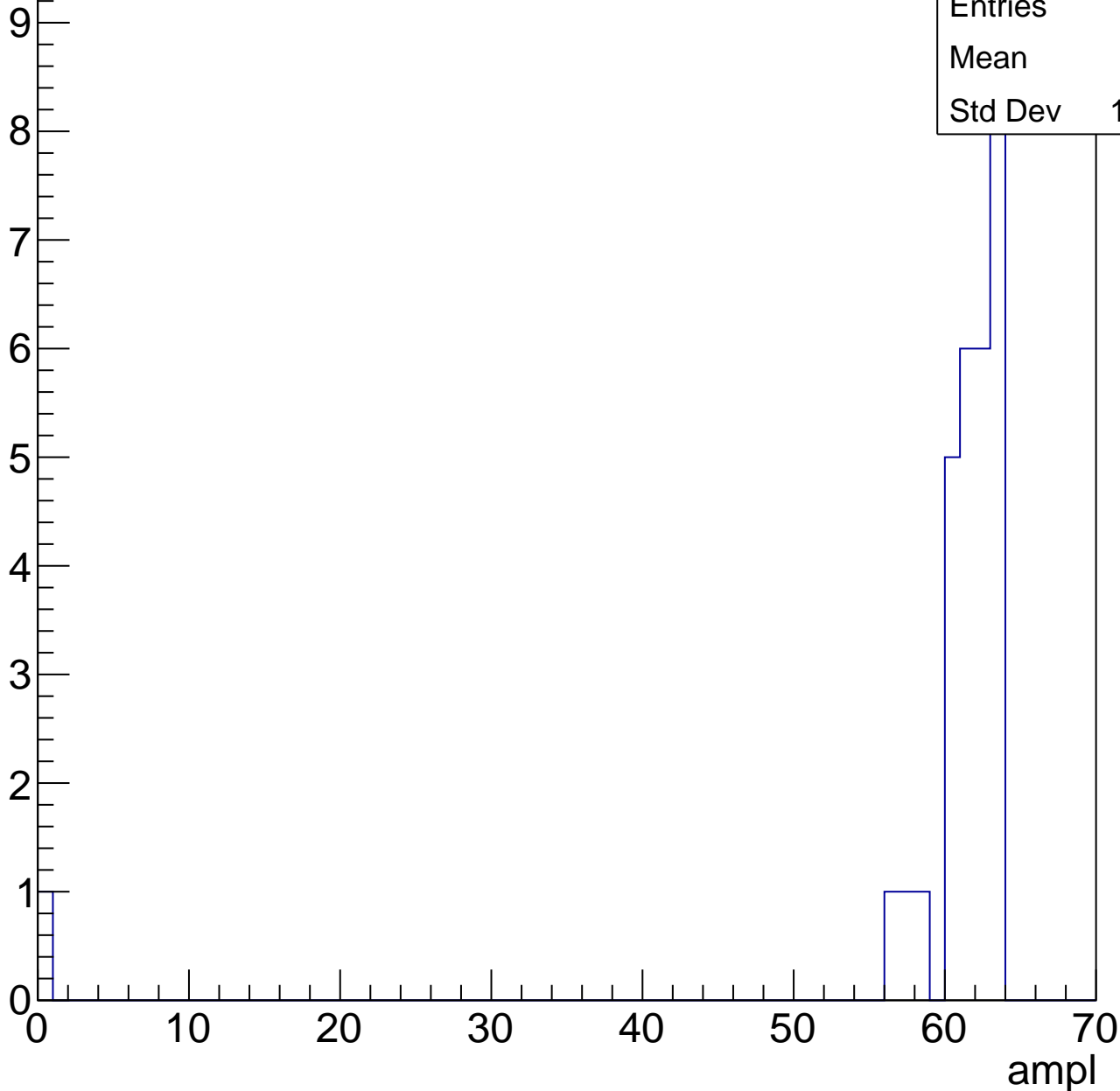


# B1L100S, U2-ch33, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

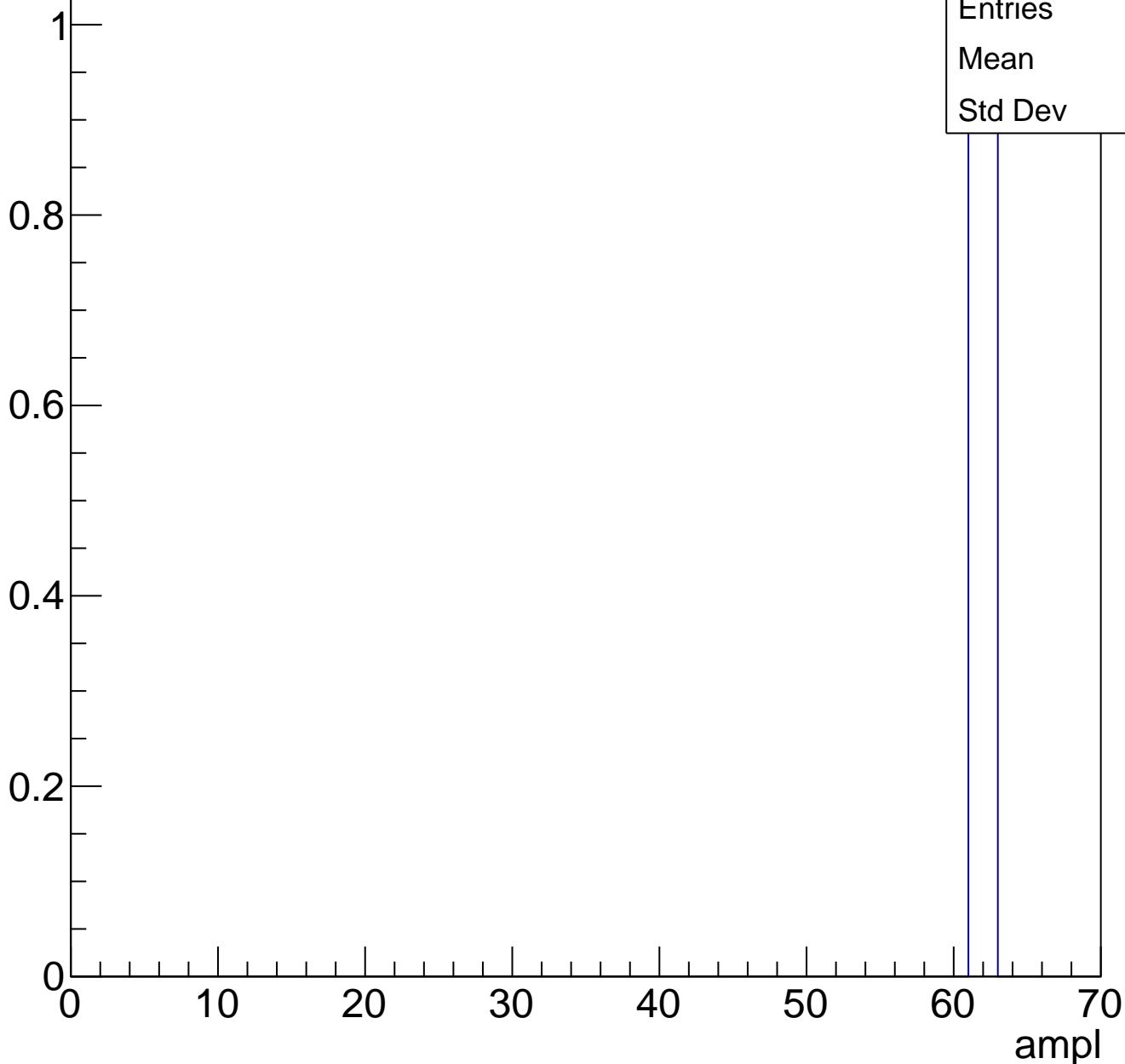
Entries	30
Mean	59.2
Std Dev	11.14



# B1L100S, U2-ch33, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry





# B1L100S, U2-ch33, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

1

0.8

0.6

0.4

0.2

0

0

10

20

30

40

50

60

70

ampl

Entries

1

Mean

63

Std Dev

0

# B1L100S, U2-ch34, adc0

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	78
Mean	29.23
Std Dev	4.959

**Gaus mean : 29.8355**

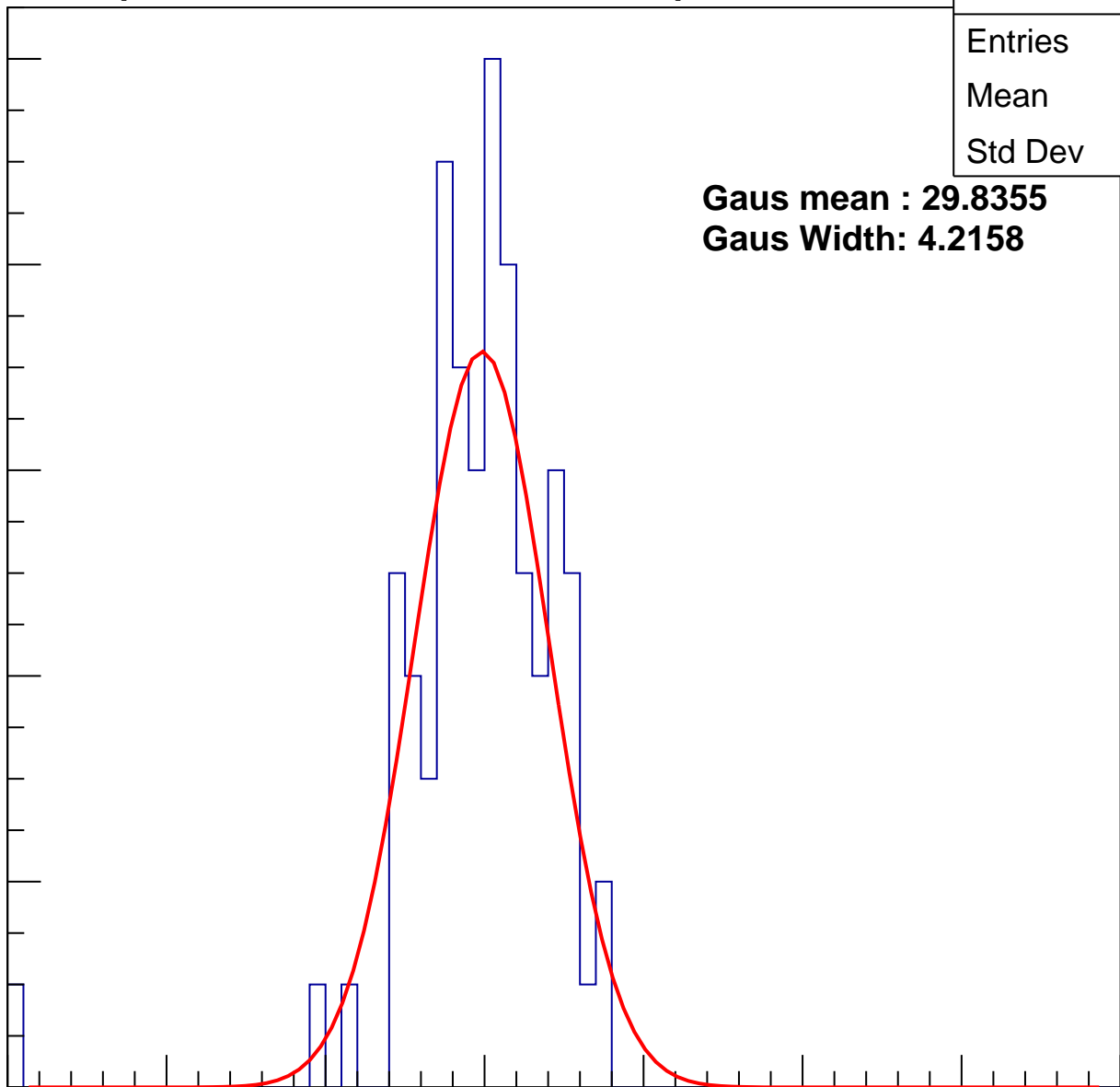
**Gaus Width: 4.2158**

Entry

10  
8  
6  
4  
2  
0

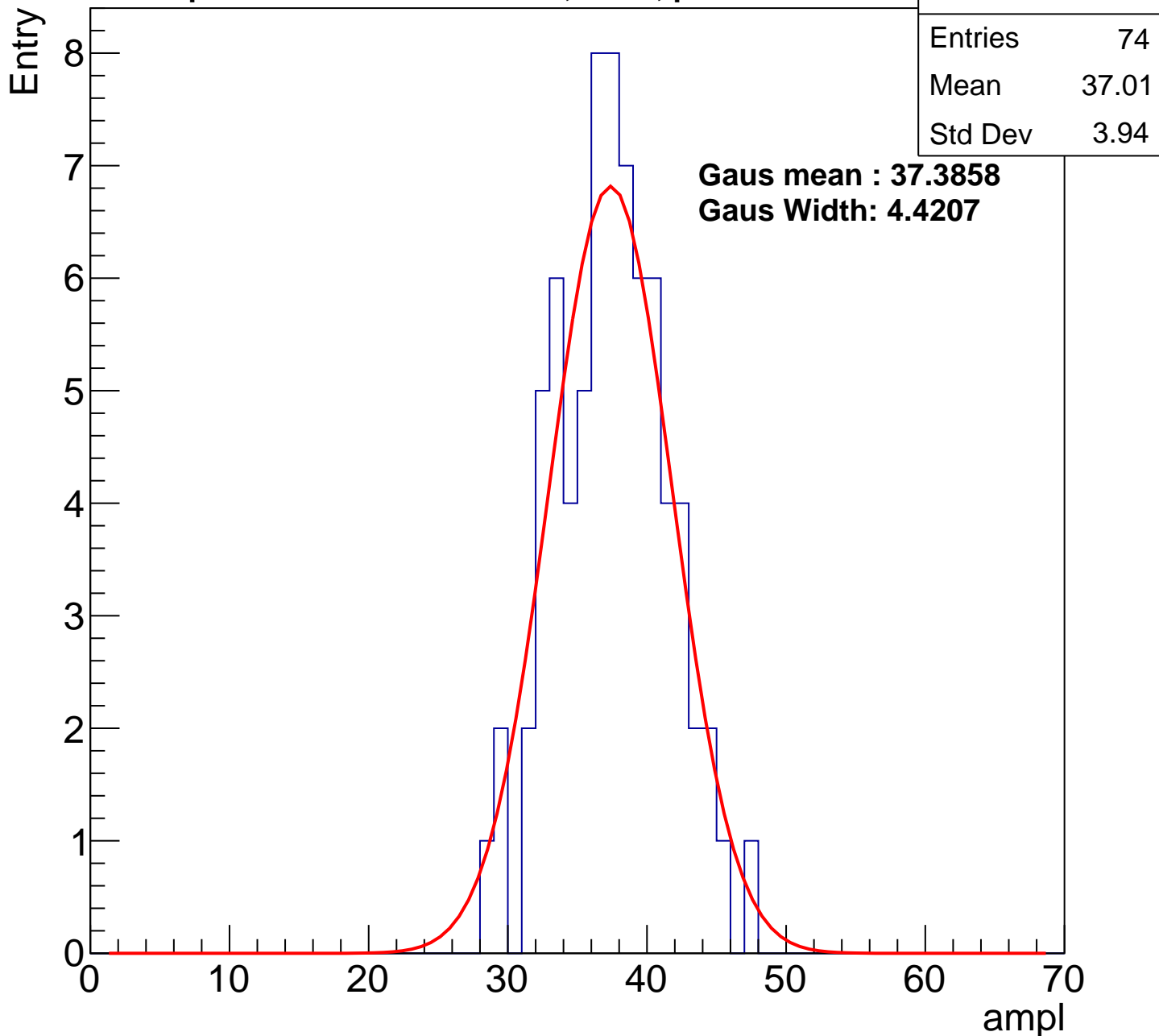
ampl

0 10 20 30 40 50 60 70



# B1L100S, U2-ch34, adc1

calib\_packv5\_042523\_0143.root, FC#4, port A2



# B1L100S, U2-ch34, adc2

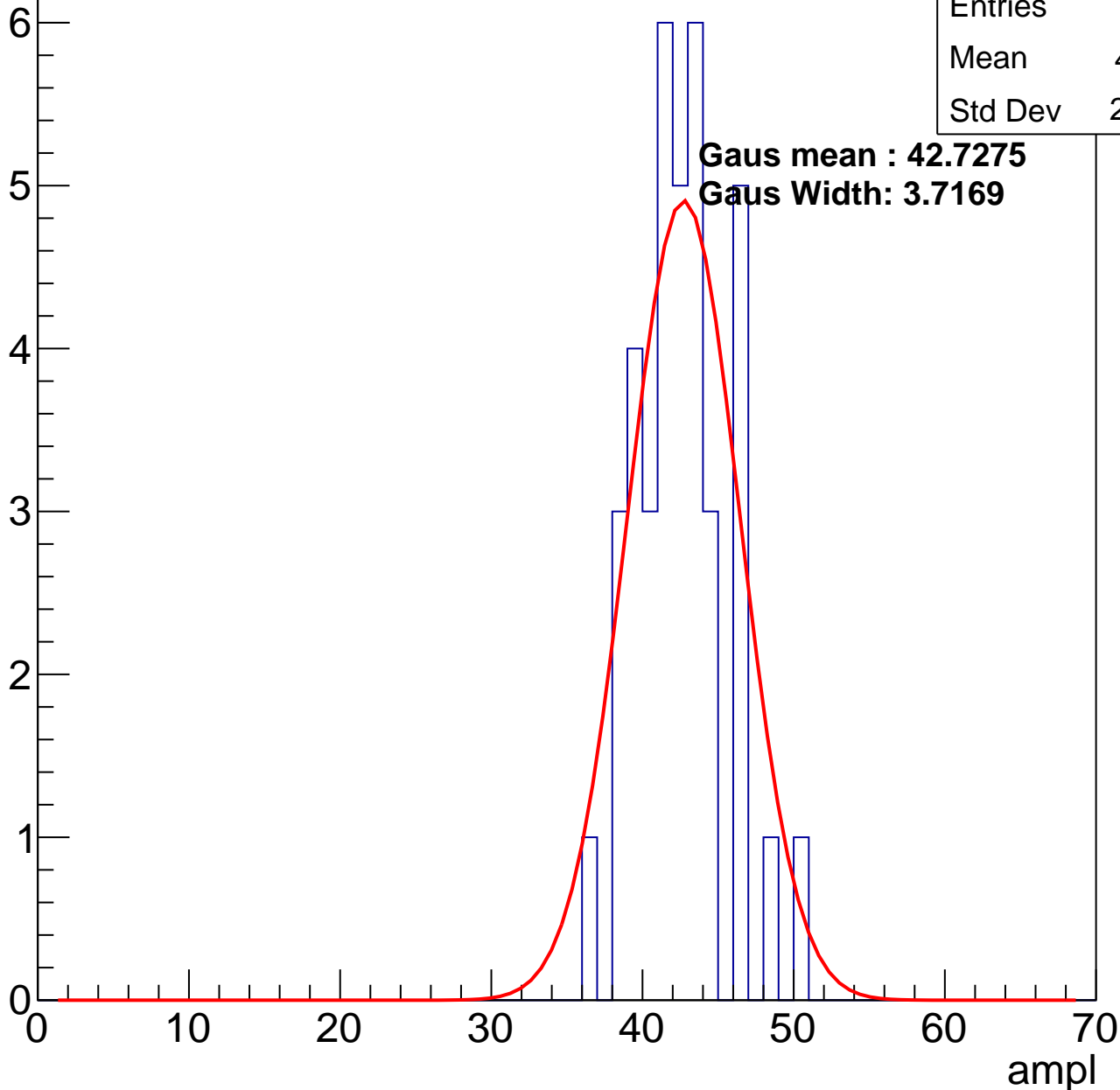
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	38
Mean	42.11
Std Dev	2.972

**Gaus mean : 42.7275**

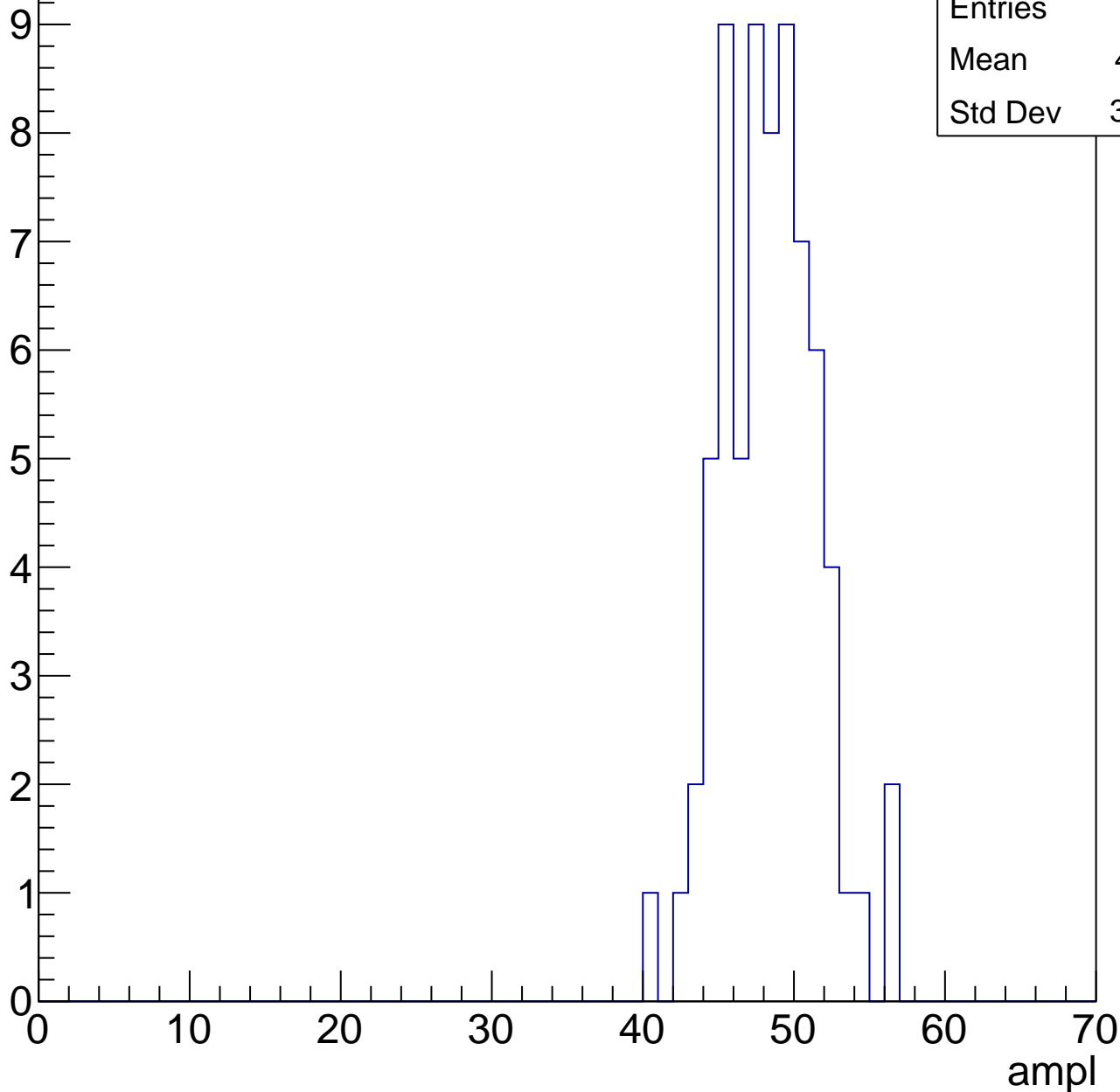
**Gaus Width: 3.7169**



# B1L100S, U2-ch34, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



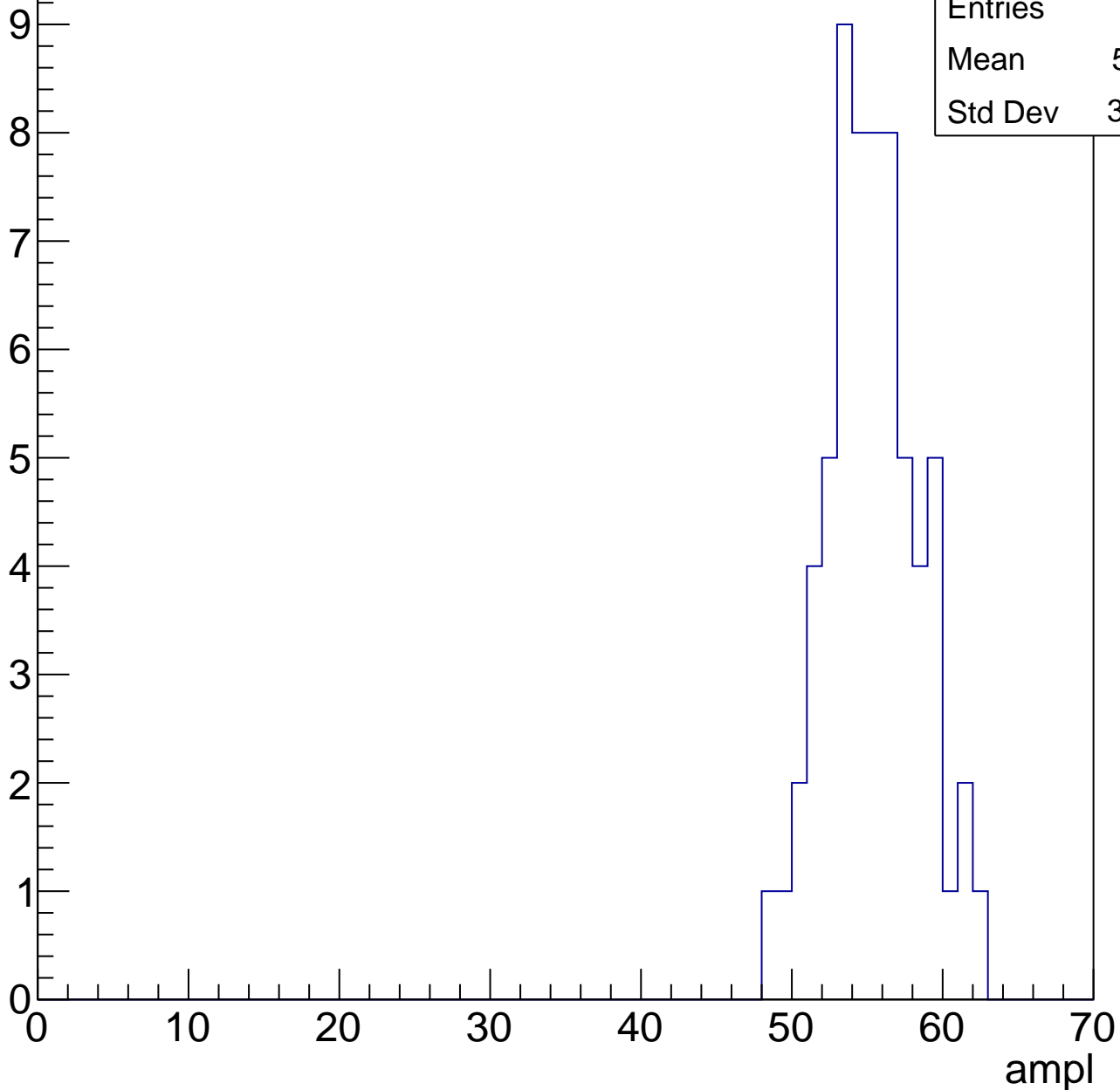
Entries	70
Mean	47.91
Std Dev	3.125

# B1L100S, U2-ch34, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

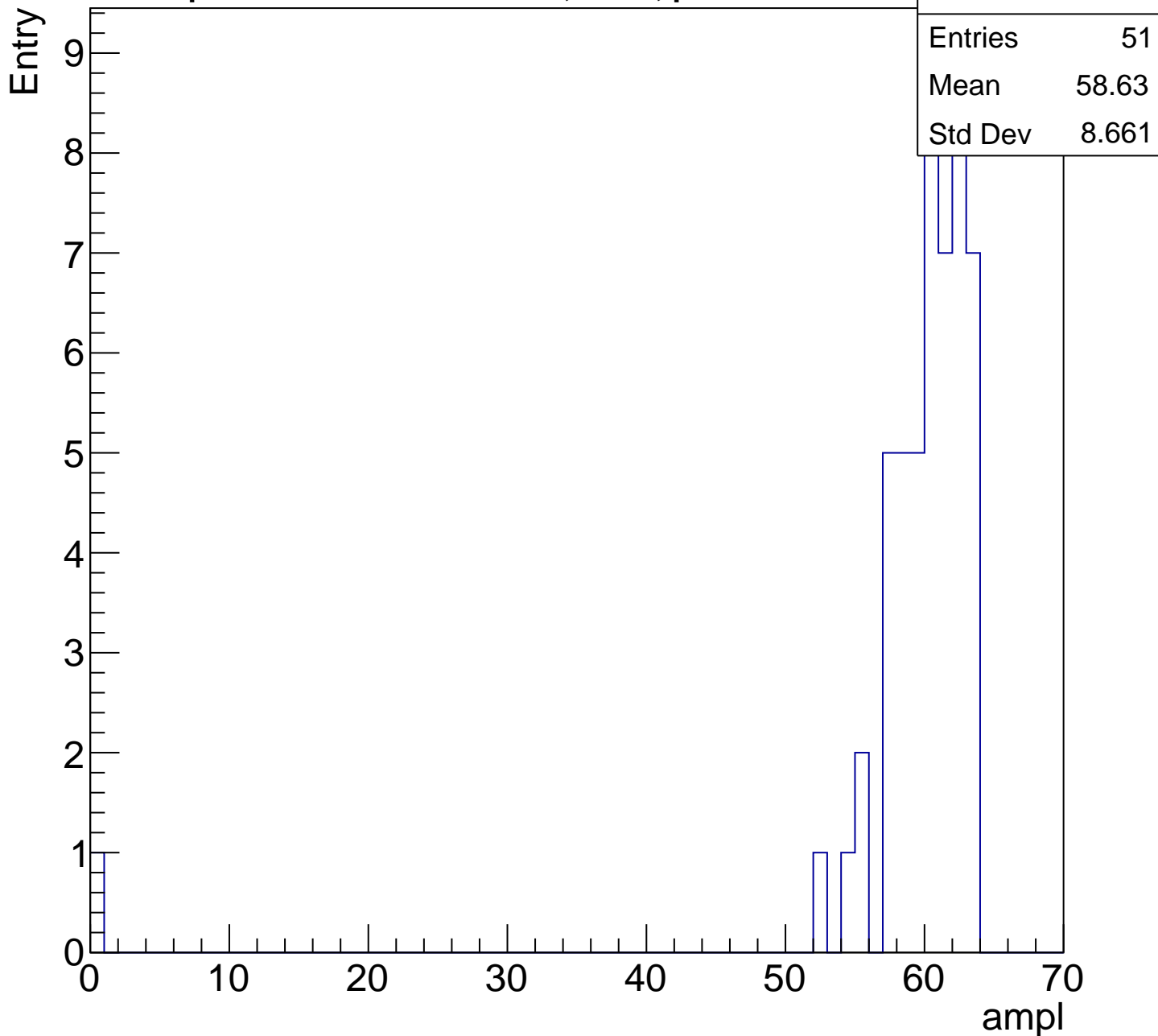
Entry

Entries	64
Mean	54.91
Std Dev	3.004



# B1L100S, U2-ch34, adc5

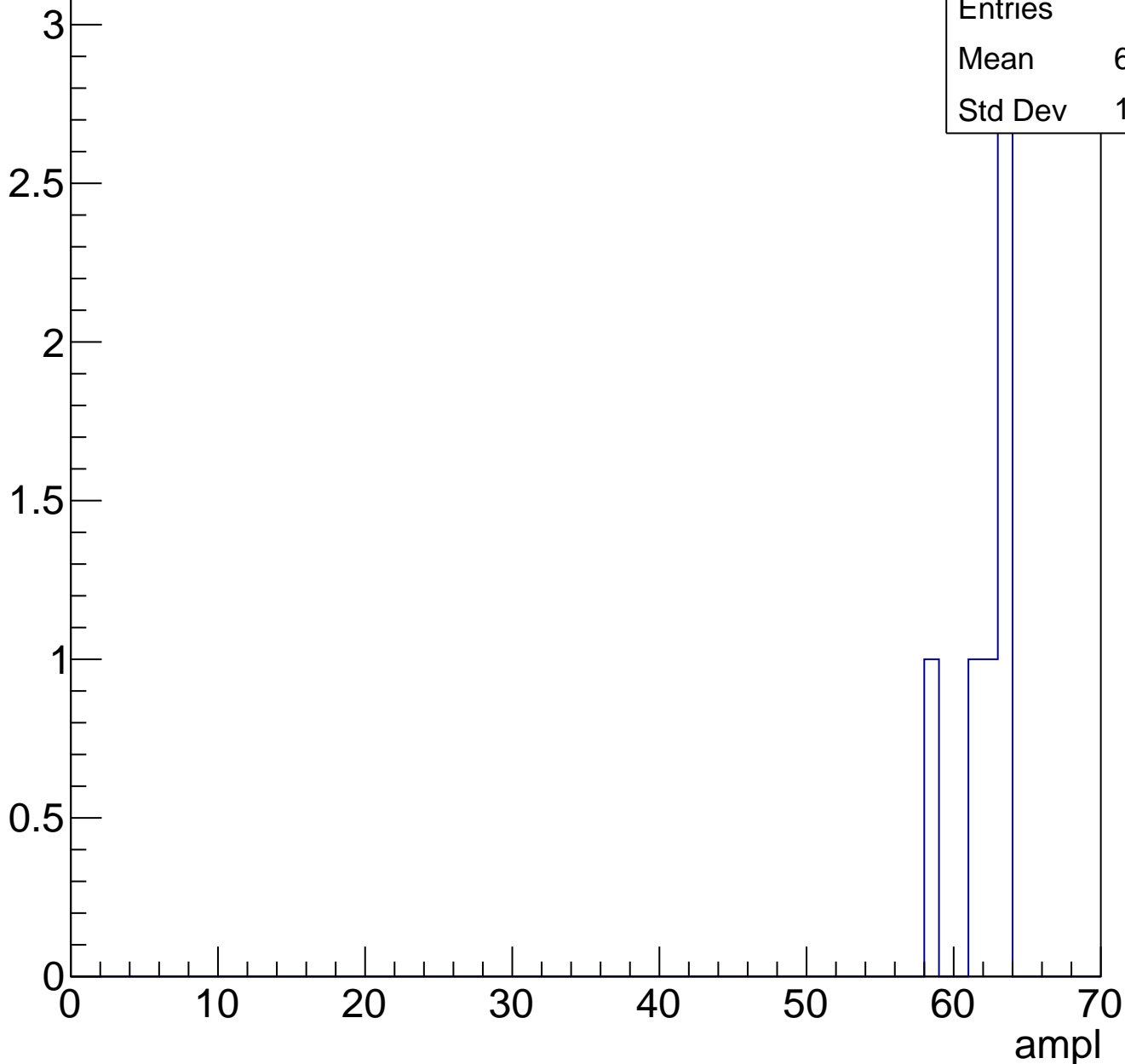
calib\_packv5\_042523\_0143.root, FC#4, port A2



# B1L100S, U2-ch34, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

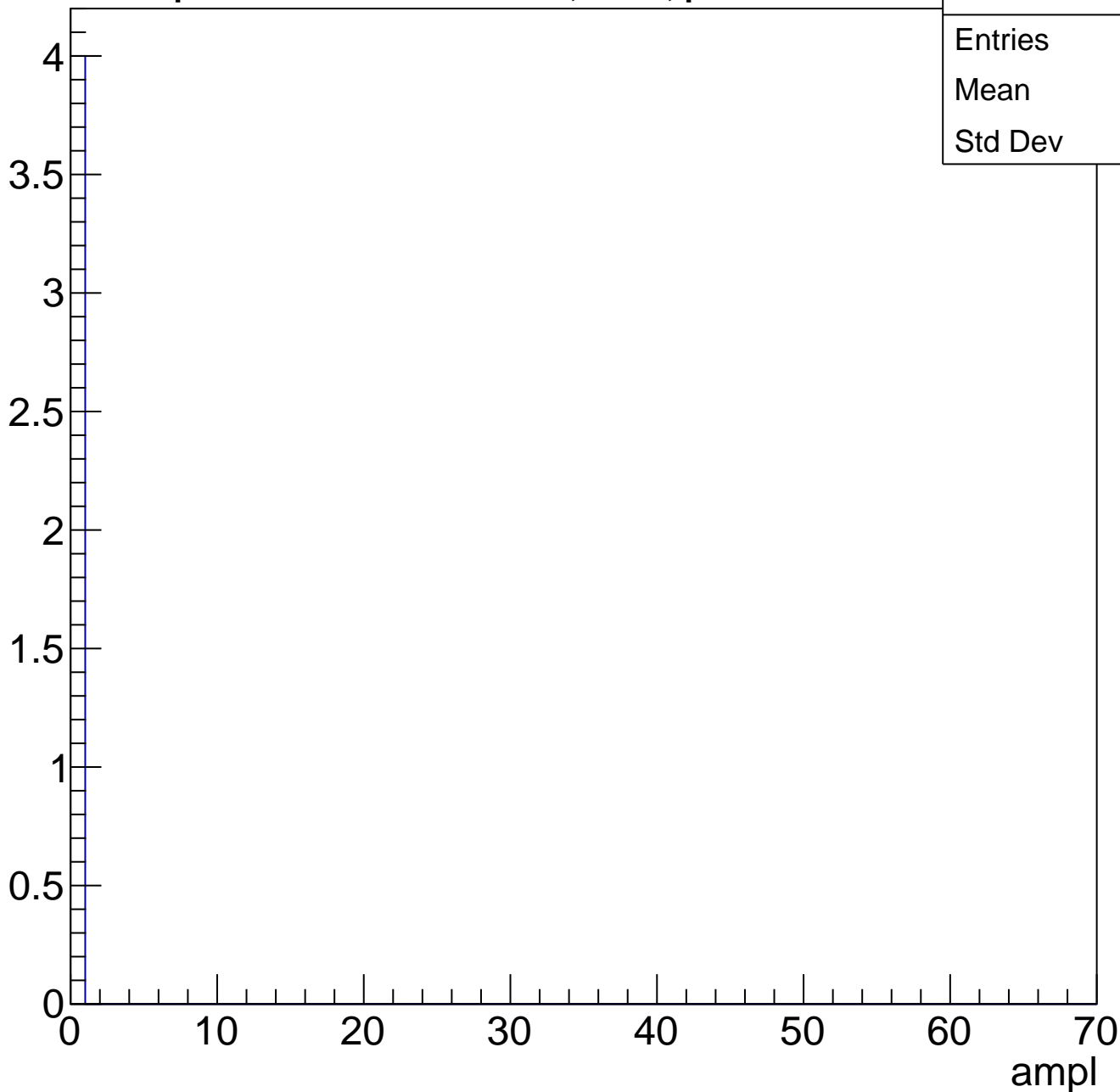




# B1L100S, U2-ch34, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	4
Mean	0
Std Dev	0

# B1L100S, U2-ch35, adc0

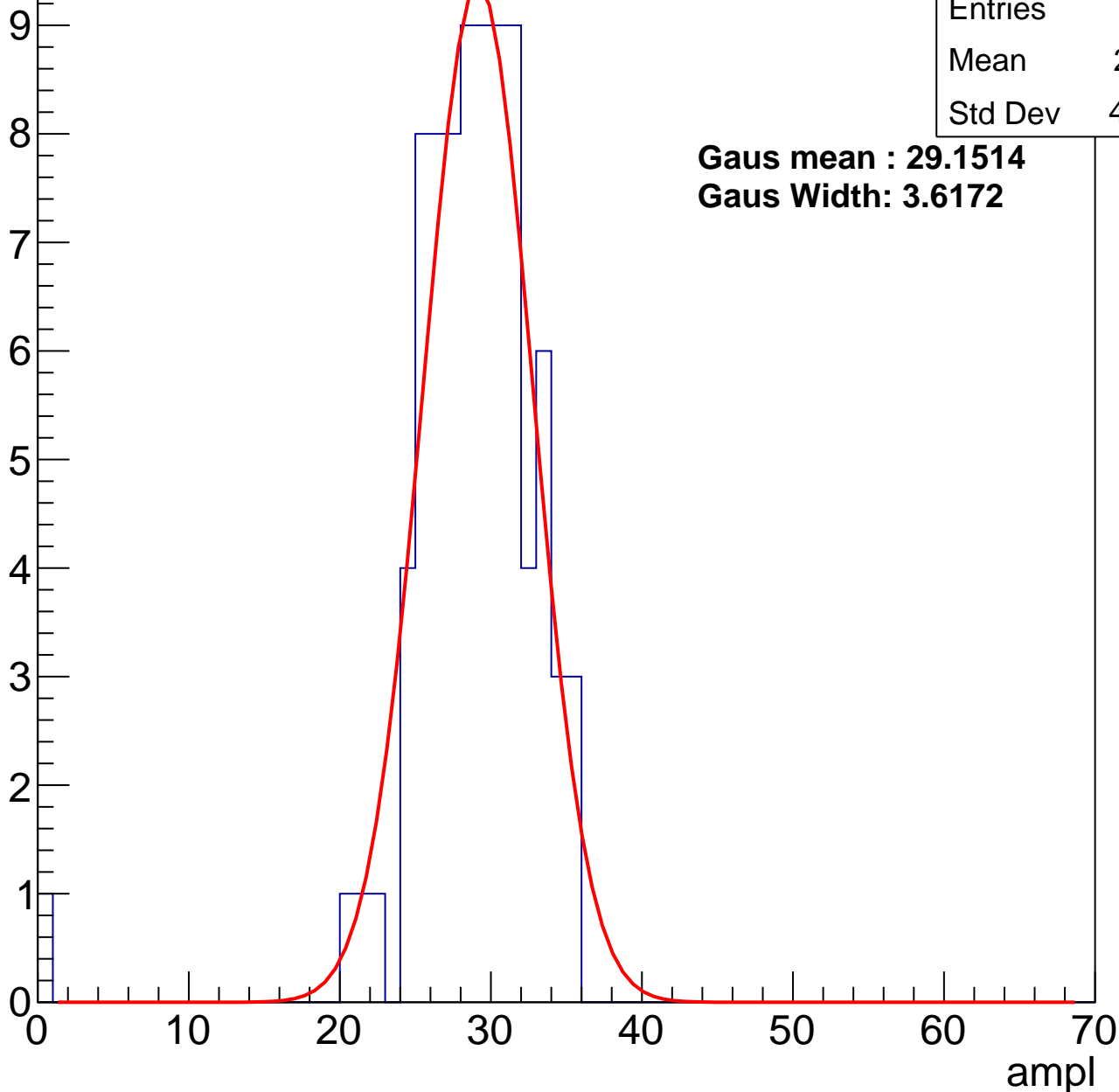
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	84
Mean	28.31
Std Dev	4.493

**Gaus mean : 29.1514**

**Gaus Width: 3.6172**



# B1L100S, U2-ch35, adc1

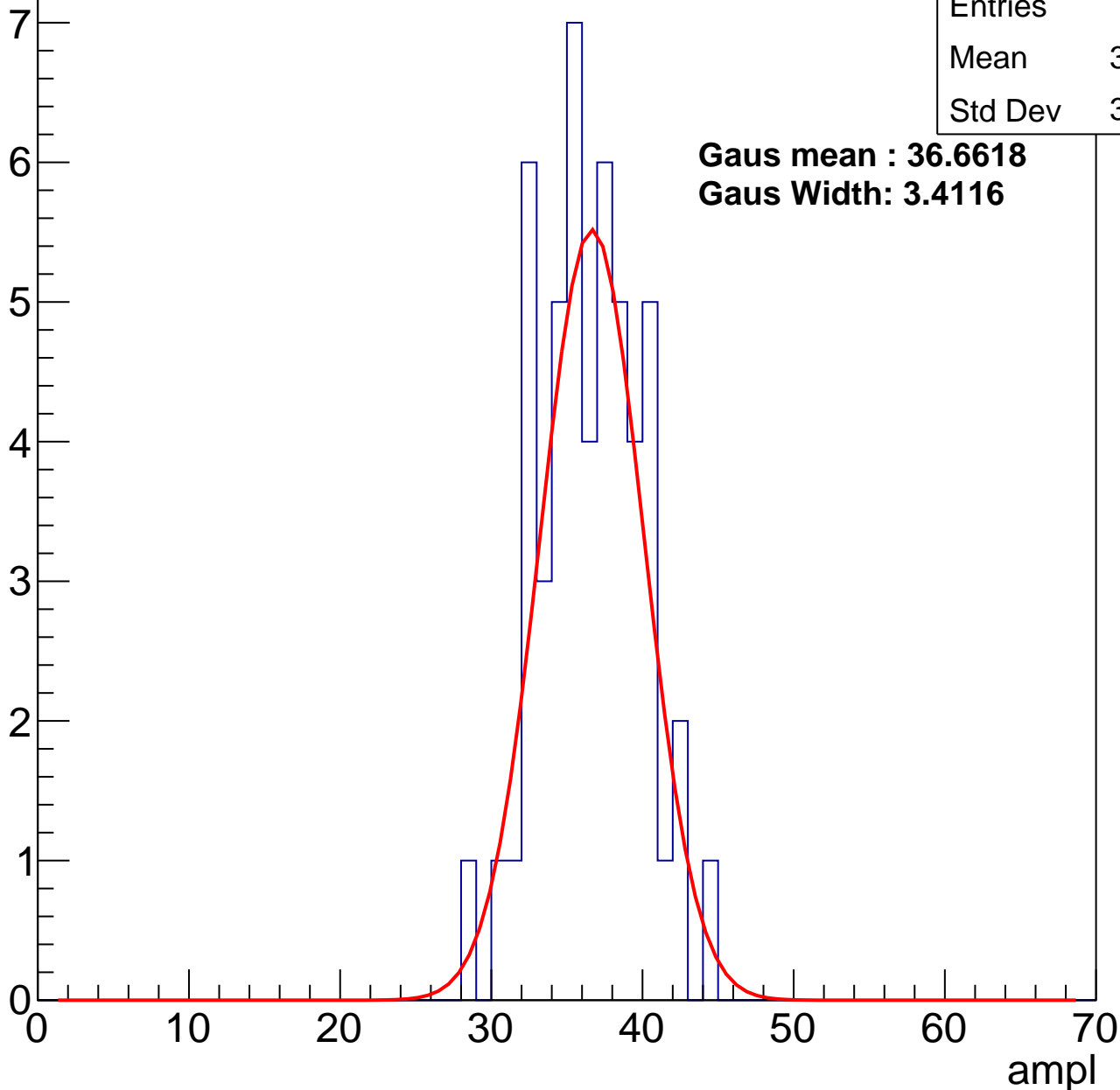
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	52
Mean	36.08
Std Dev	3.333

**Gaus mean : 36.6618**

**Gaus Width: 3.4116**



# B1L100S, U2-ch35, adc2

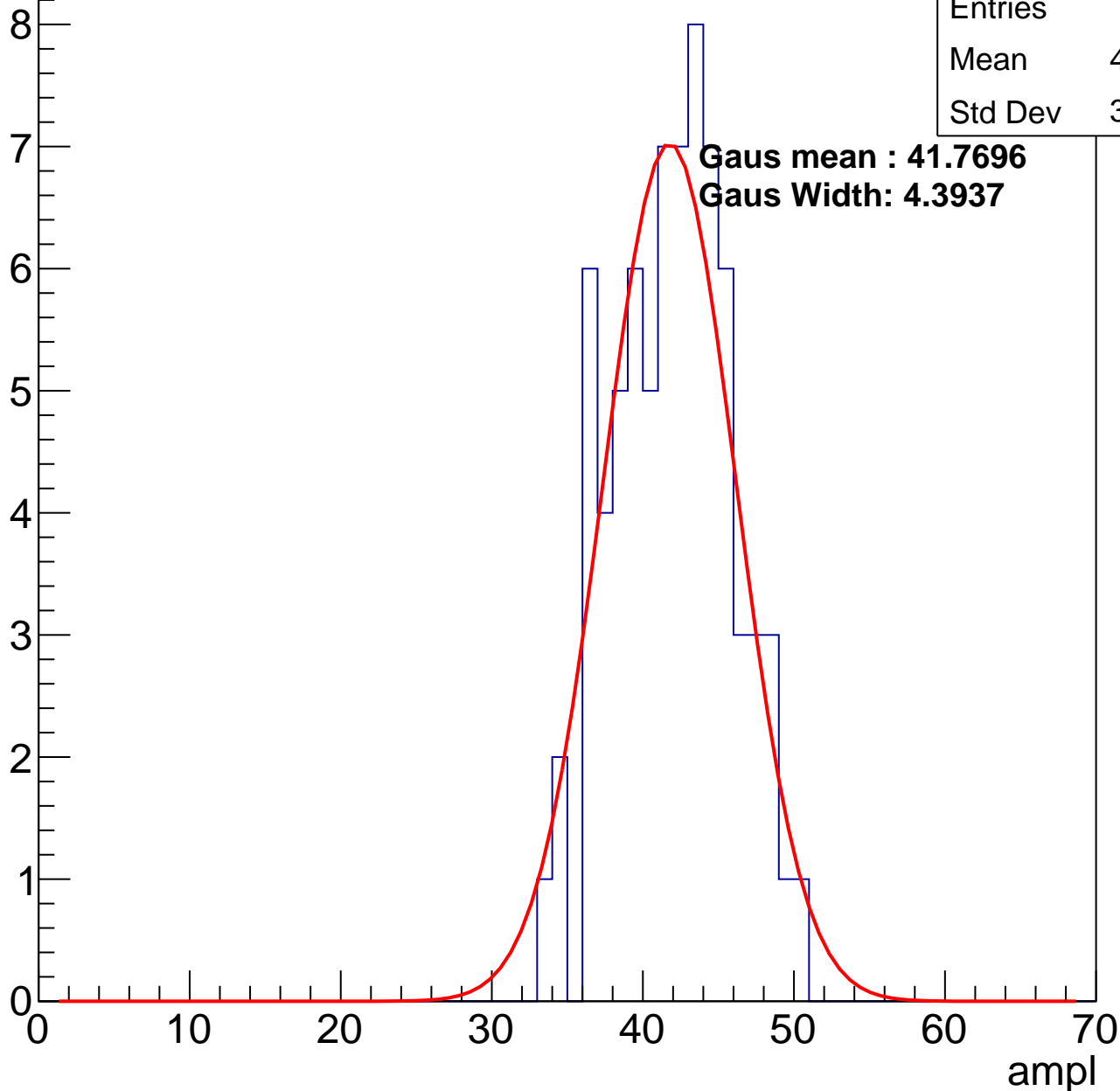
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	75
Mean	41.52
Std Dev	3.834

**Gaus mean : 41.7696**

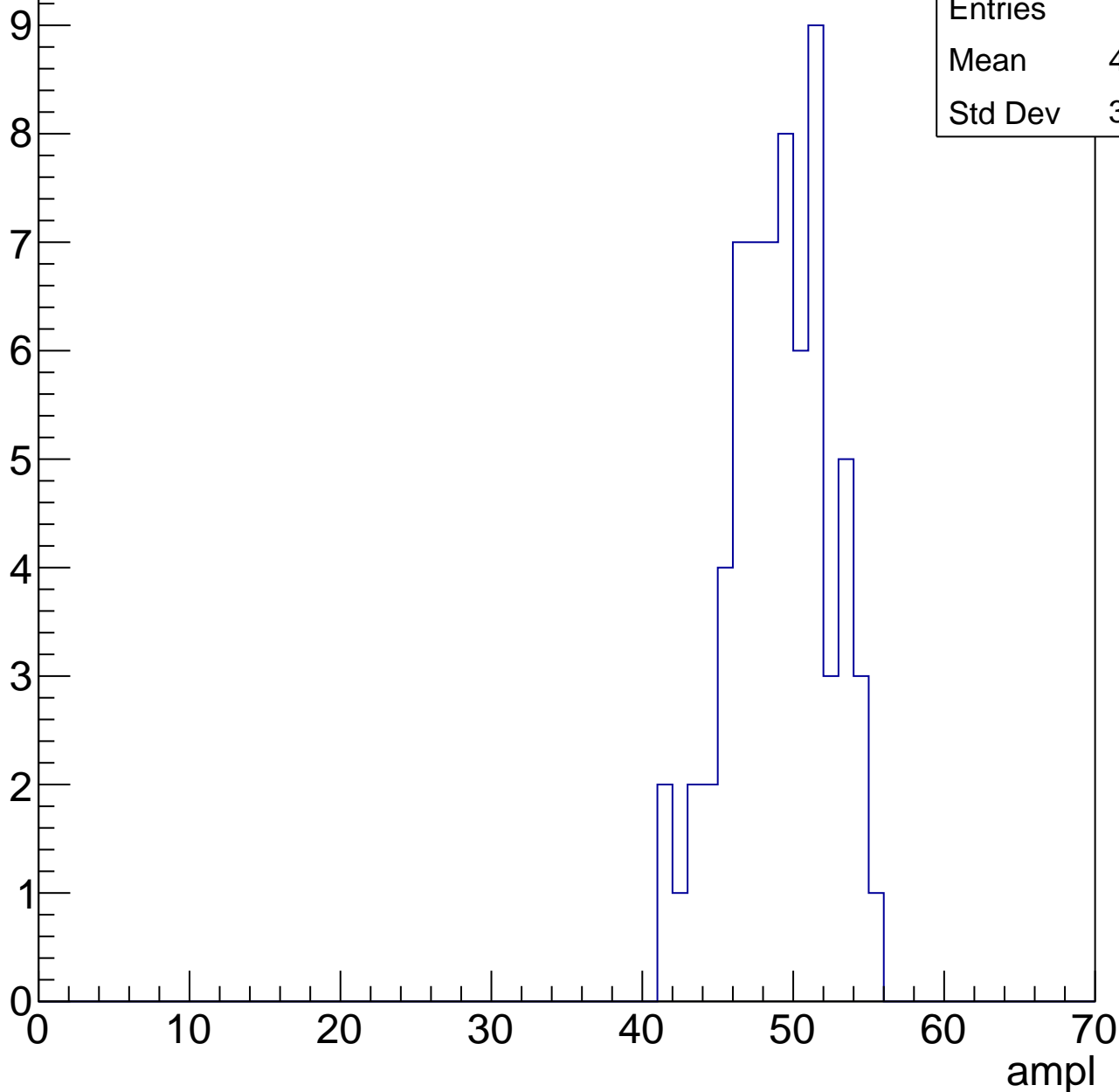
**Gaus Width: 4.3937**



# B1L100S, U2-ch35, adc3

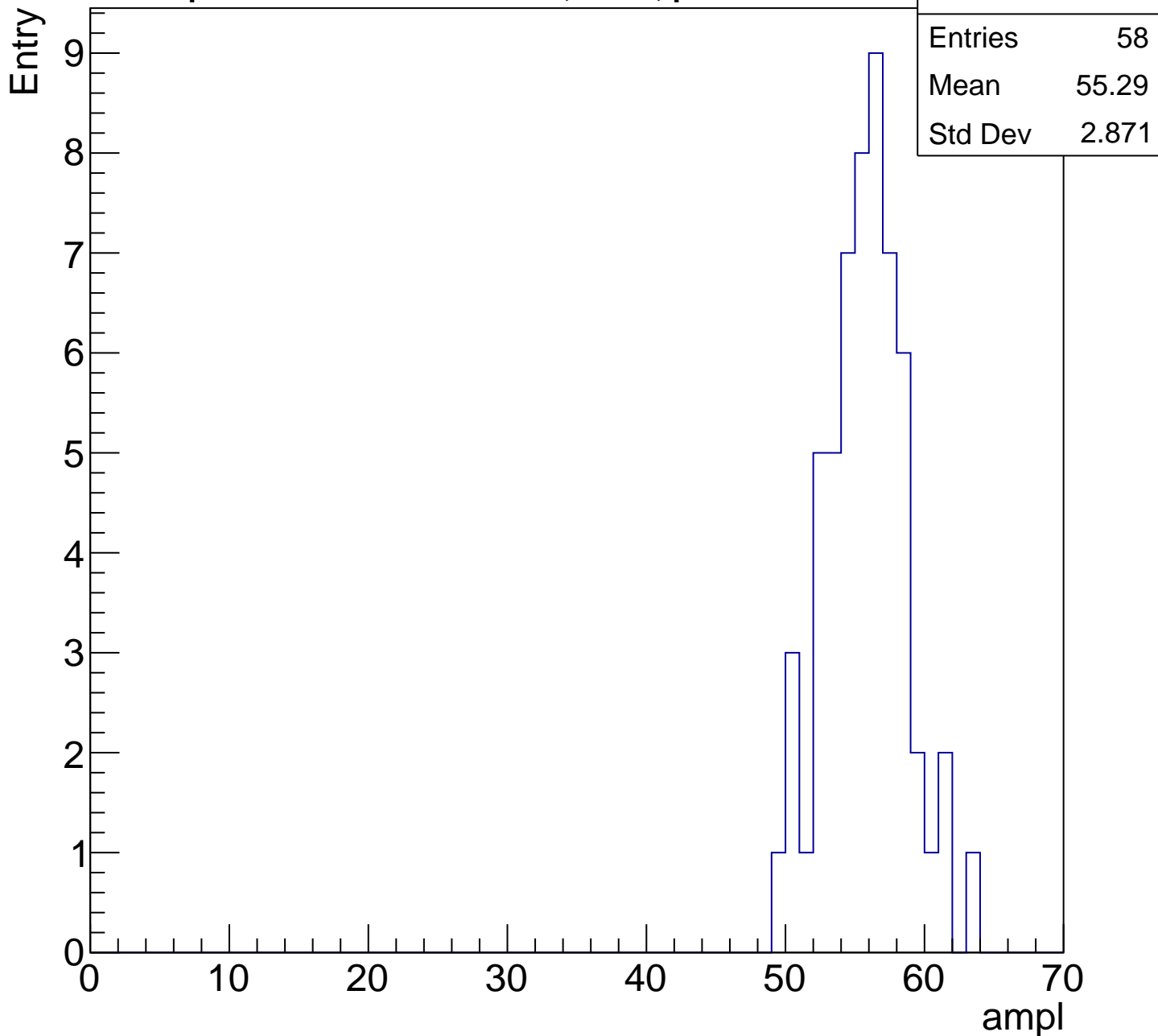
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



# B1L100S, U2-ch35, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2



# B1L100S, U2-ch35, adc5

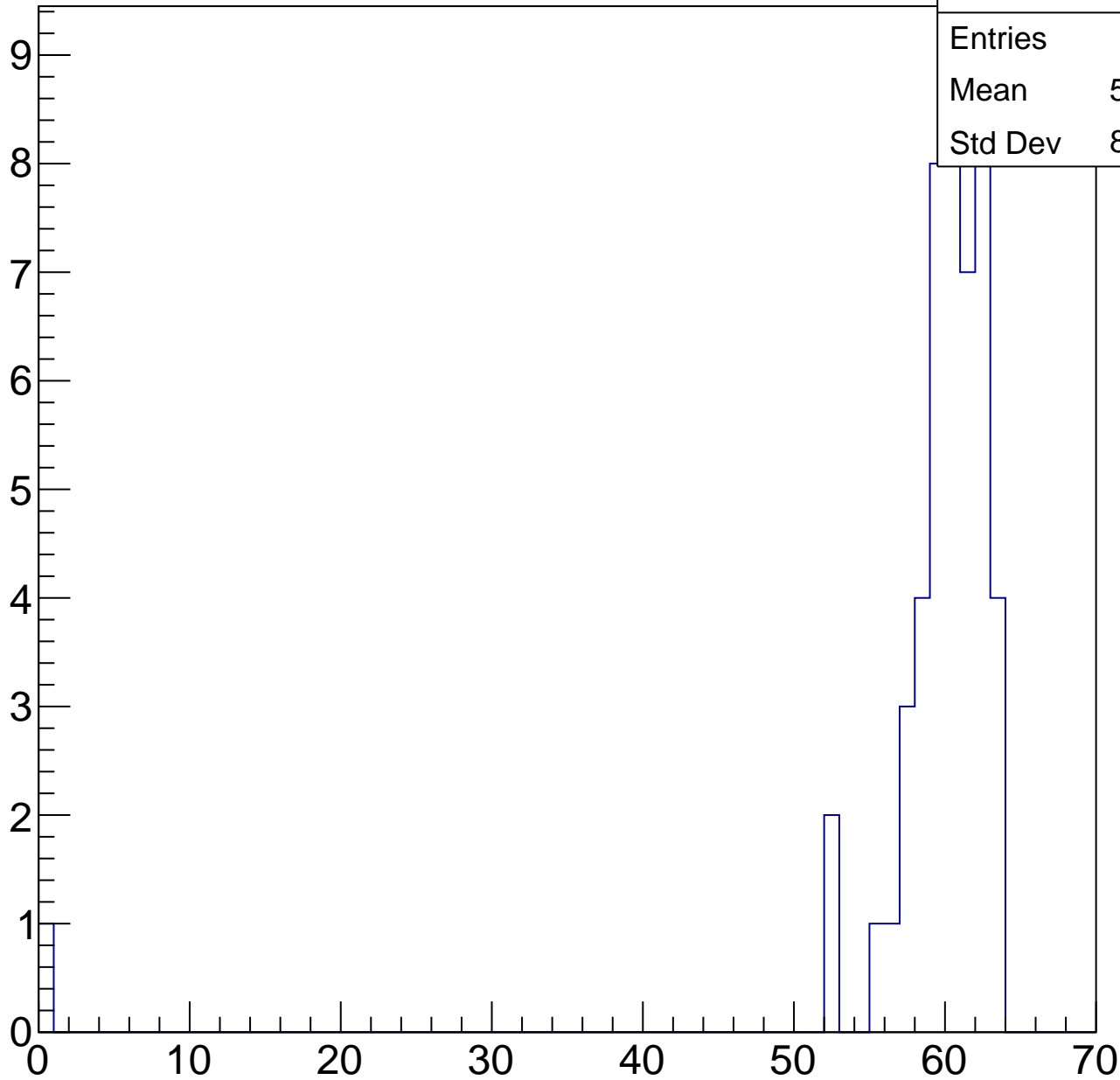
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	48
Mean	58.44
Std Dev	8.872

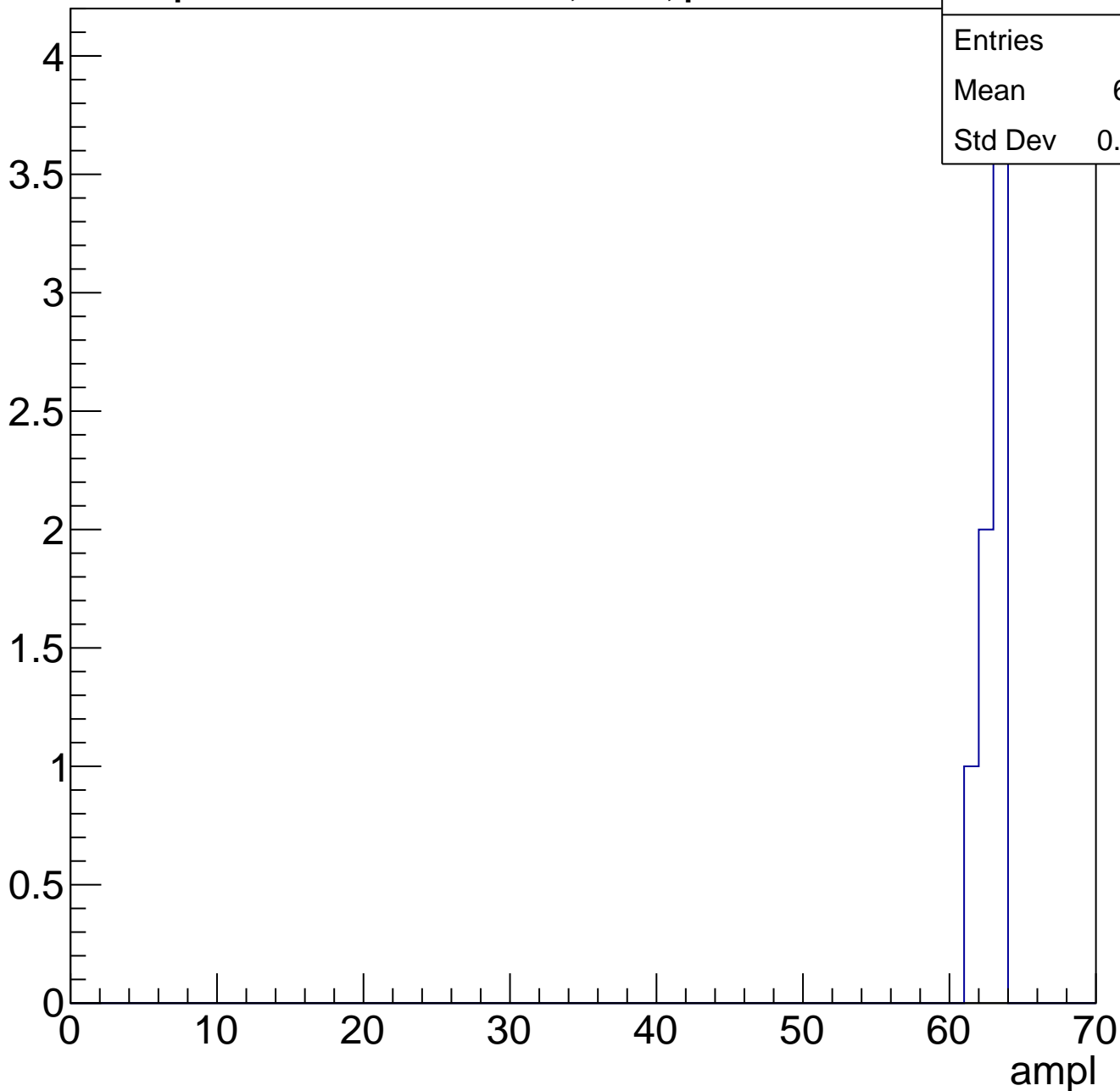
ampl



# B1L100S, U2-ch35, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry





# B1L100S, U2-ch35, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



# B1L100S, U2-ch36, adc0

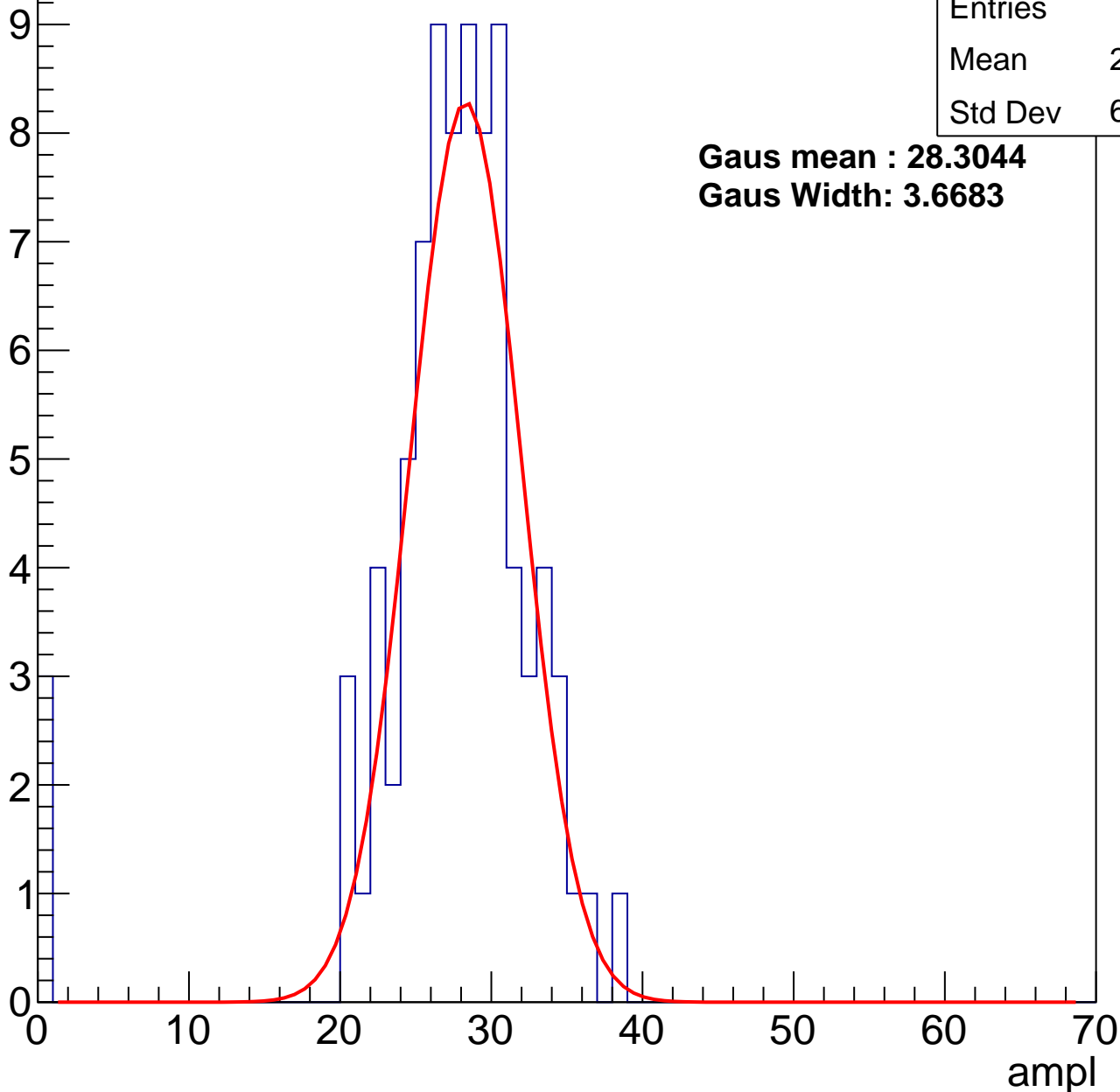
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	85
Mean	26.79
Std Dev	6.323

**Gaus mean : 28.3044**

**Gaus Width: 3.6683**



# B1L100S, U2-ch36, adc1

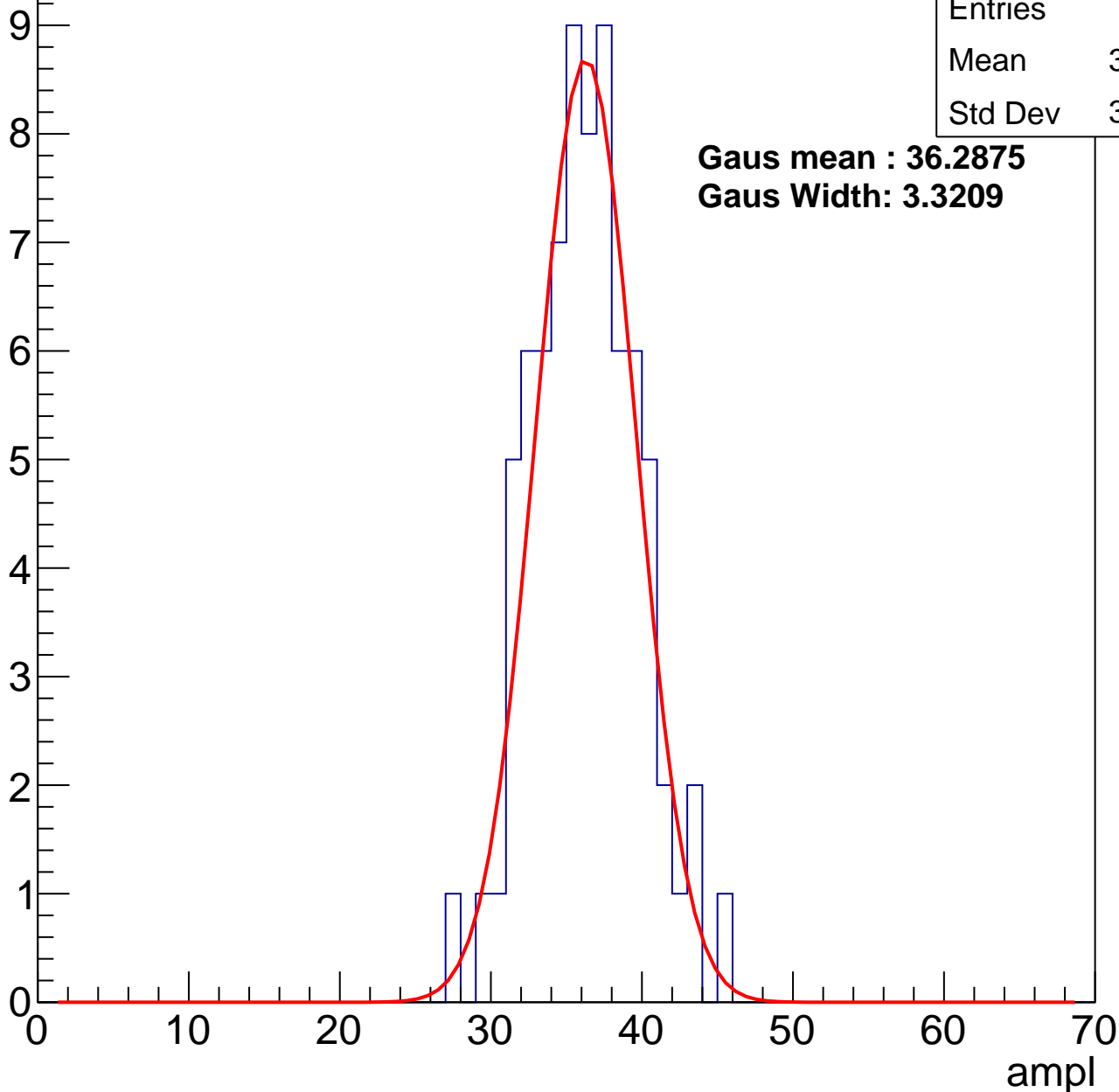
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	76
Mean	35.82
Std Dev	3.455

**Gaus mean : 36.2875**

**Gaus Width: 3.3209**



# B1L100S, U2-ch36, adc2

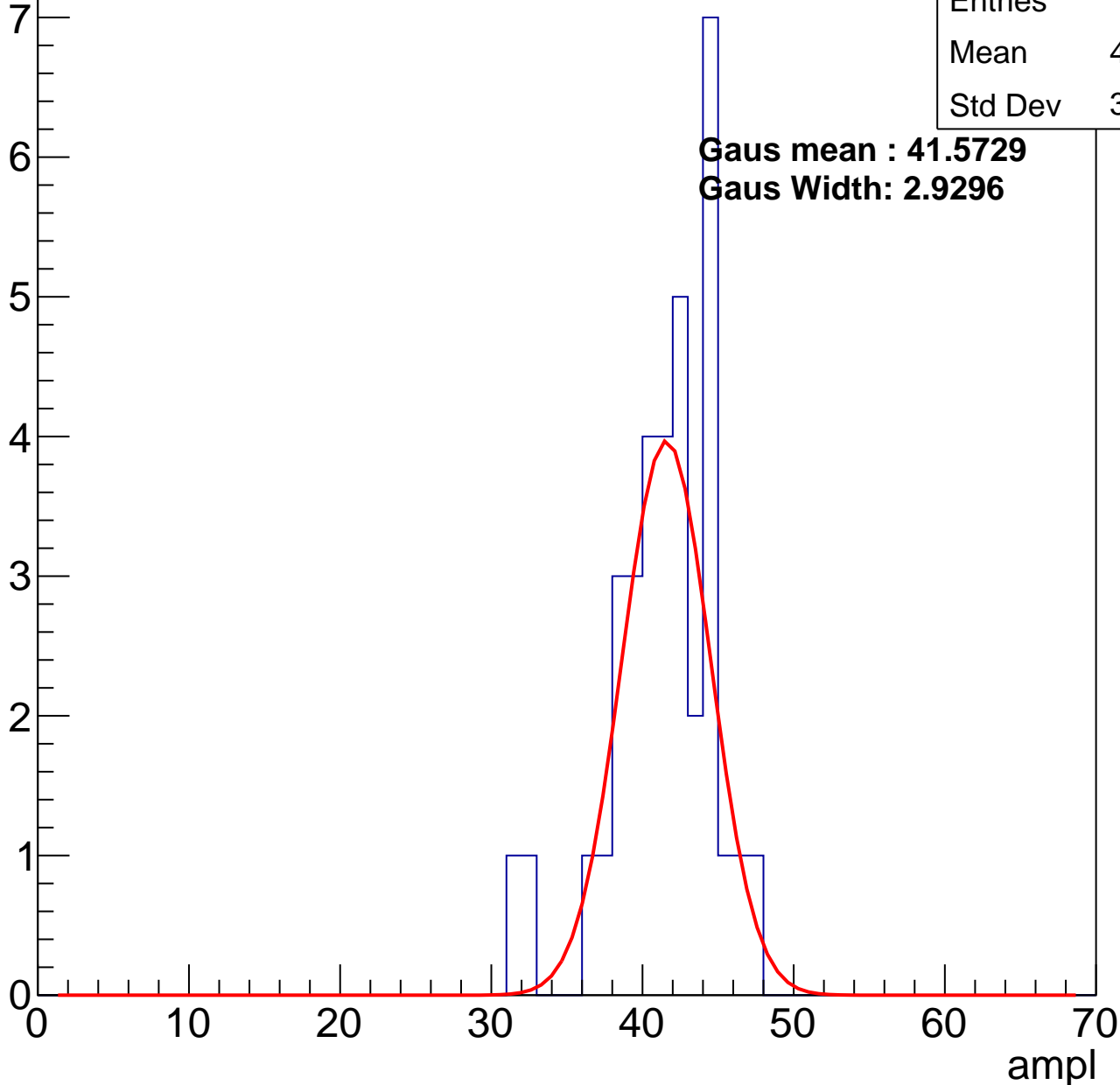
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	35
Mean	40.94
Std Dev	3.455

**Gaus mean : 41.5729**

**Gaus Width: 2.9296**



# B1L100S, U2-ch36, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

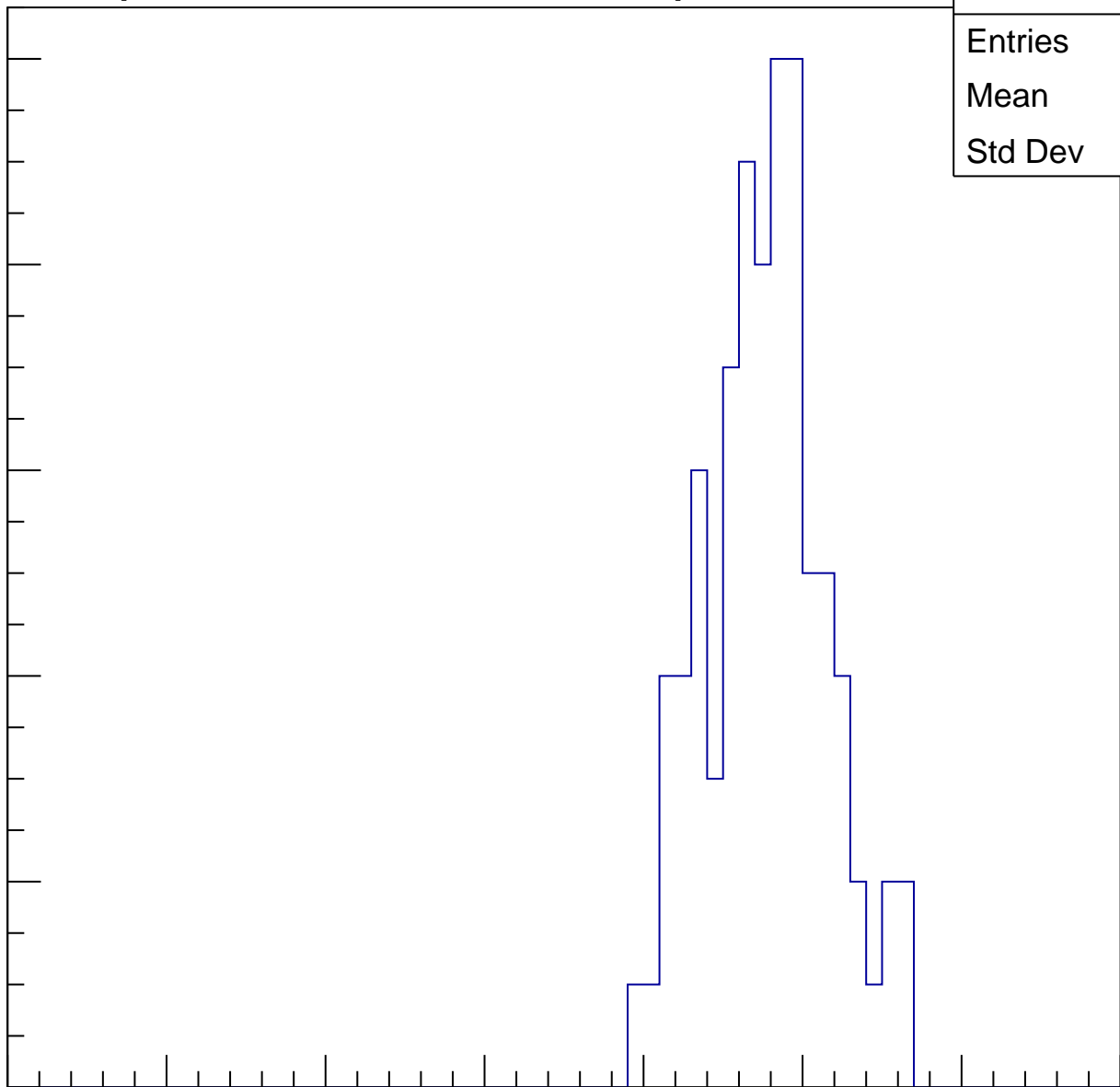
Entries	84
Mean	47.27
Std Dev	3.774

Entry

10  
8  
6  
4  
2  
0

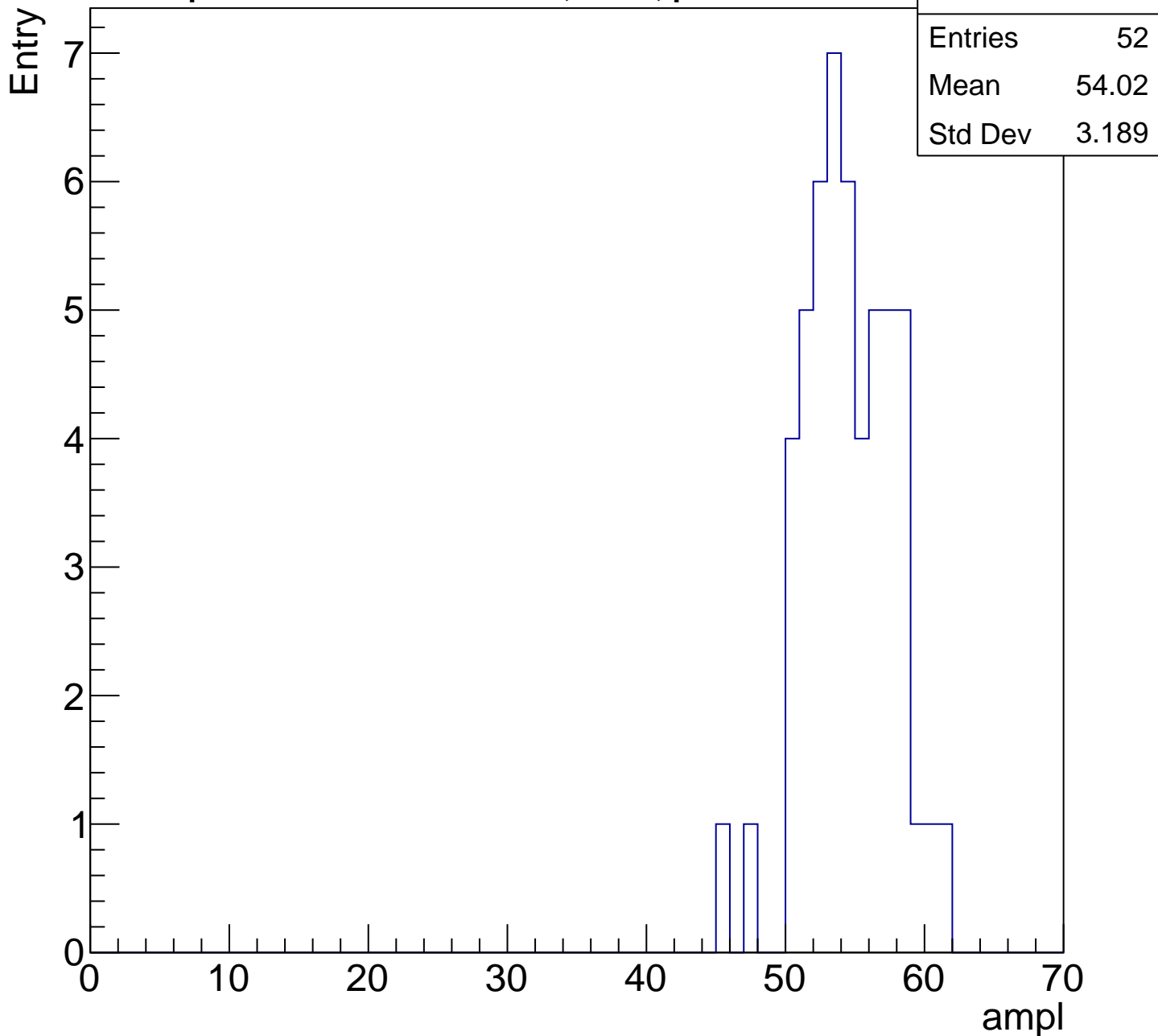
0 10 20 30 40 50 60 70

ampl



# B1L100S, U2-ch36, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2



# B1L100S, U2-ch36, adc5

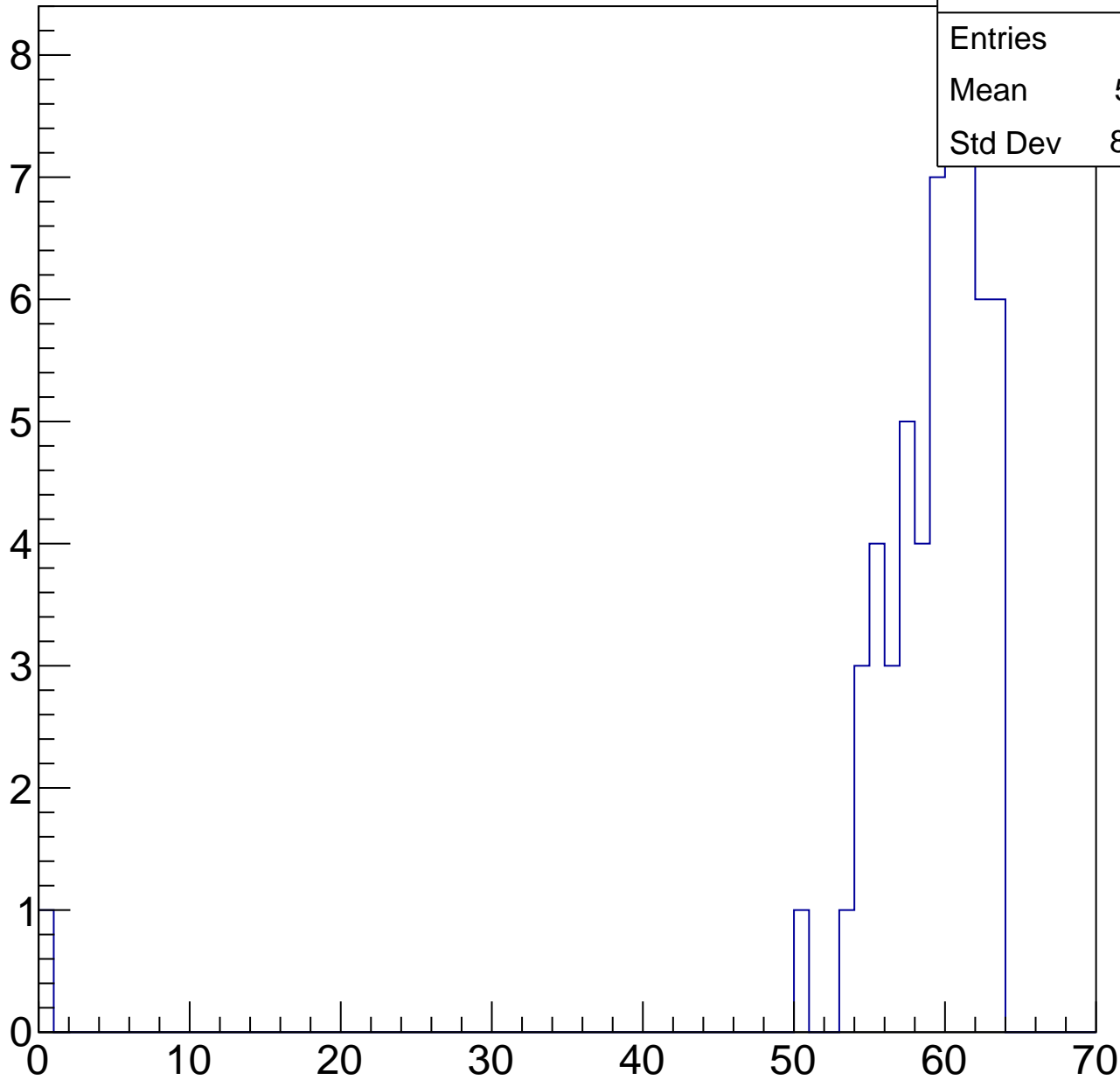
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	57
Mean	57.91
Std Dev	8.283

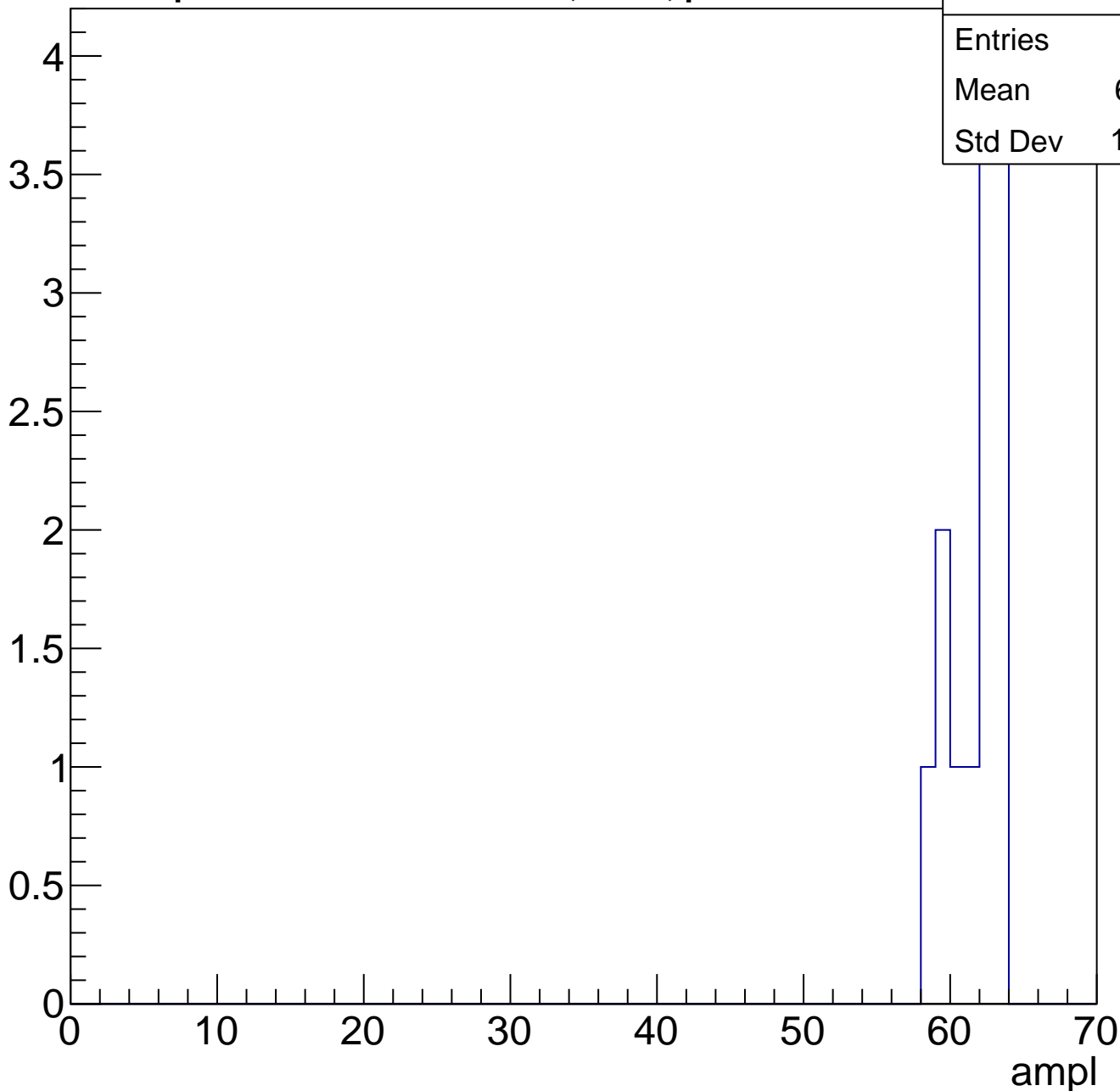
ampl



# B1L100S, U2-ch36, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry





# B1L100S, U2-ch36, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L100S, U2-ch37, adc0

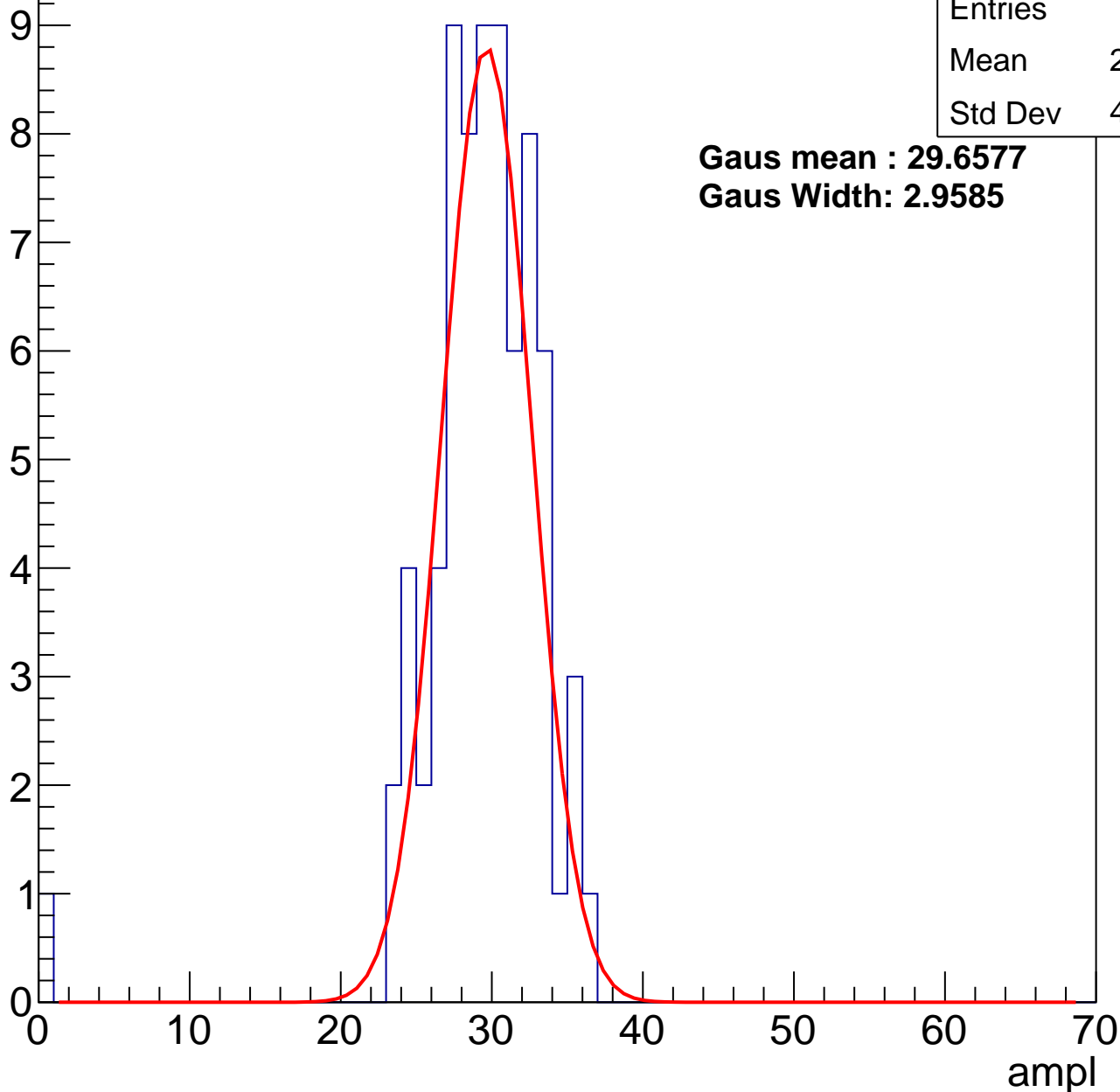
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	73
Mean	28.89
Std Dev	4.544

**Gaus mean : 29.6577**

**Gaus Width: 2.9585**



# B1L100S, U2-ch37, adc1

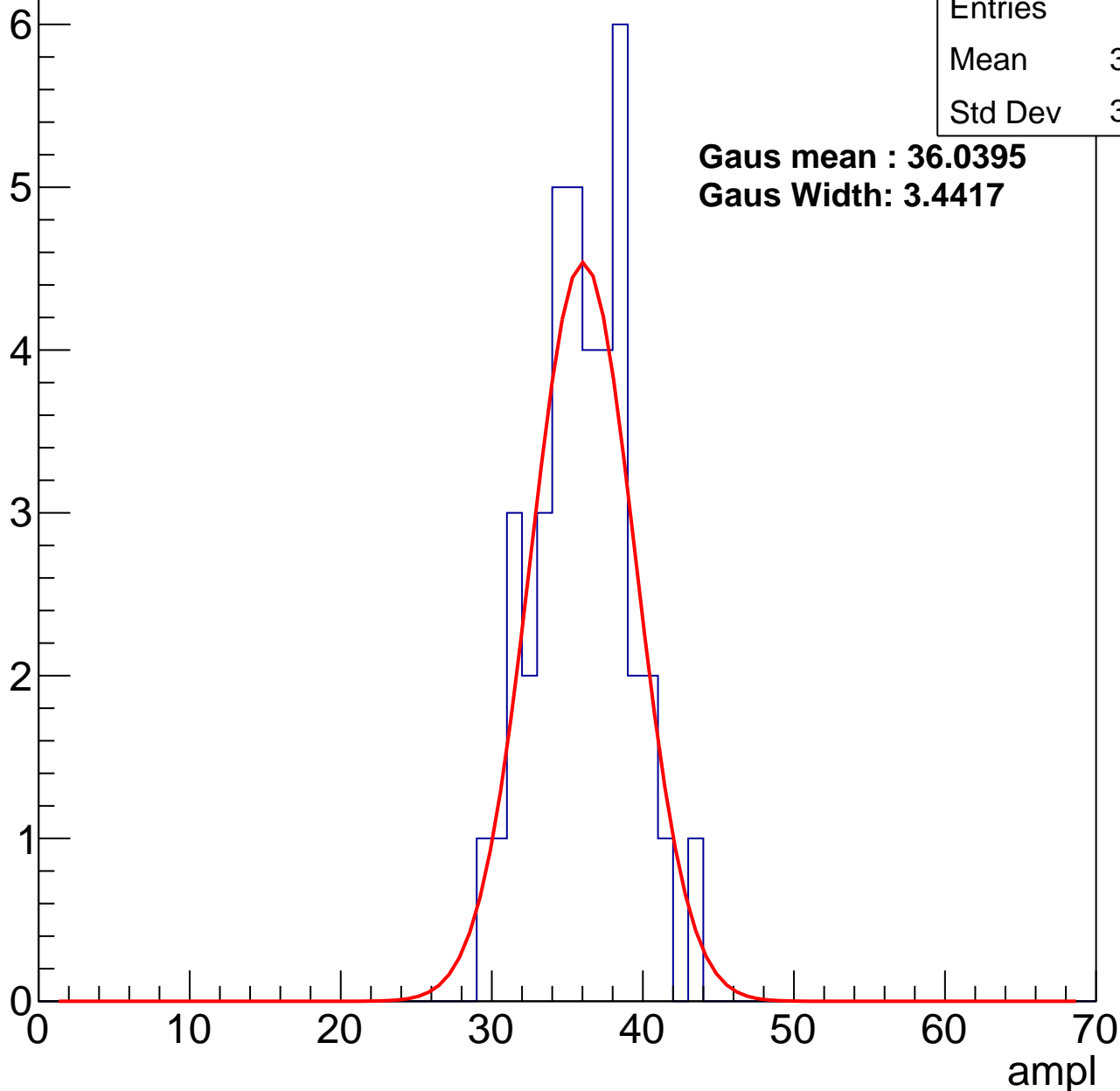
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	40
Mean	35.55
Std Dev	3.114

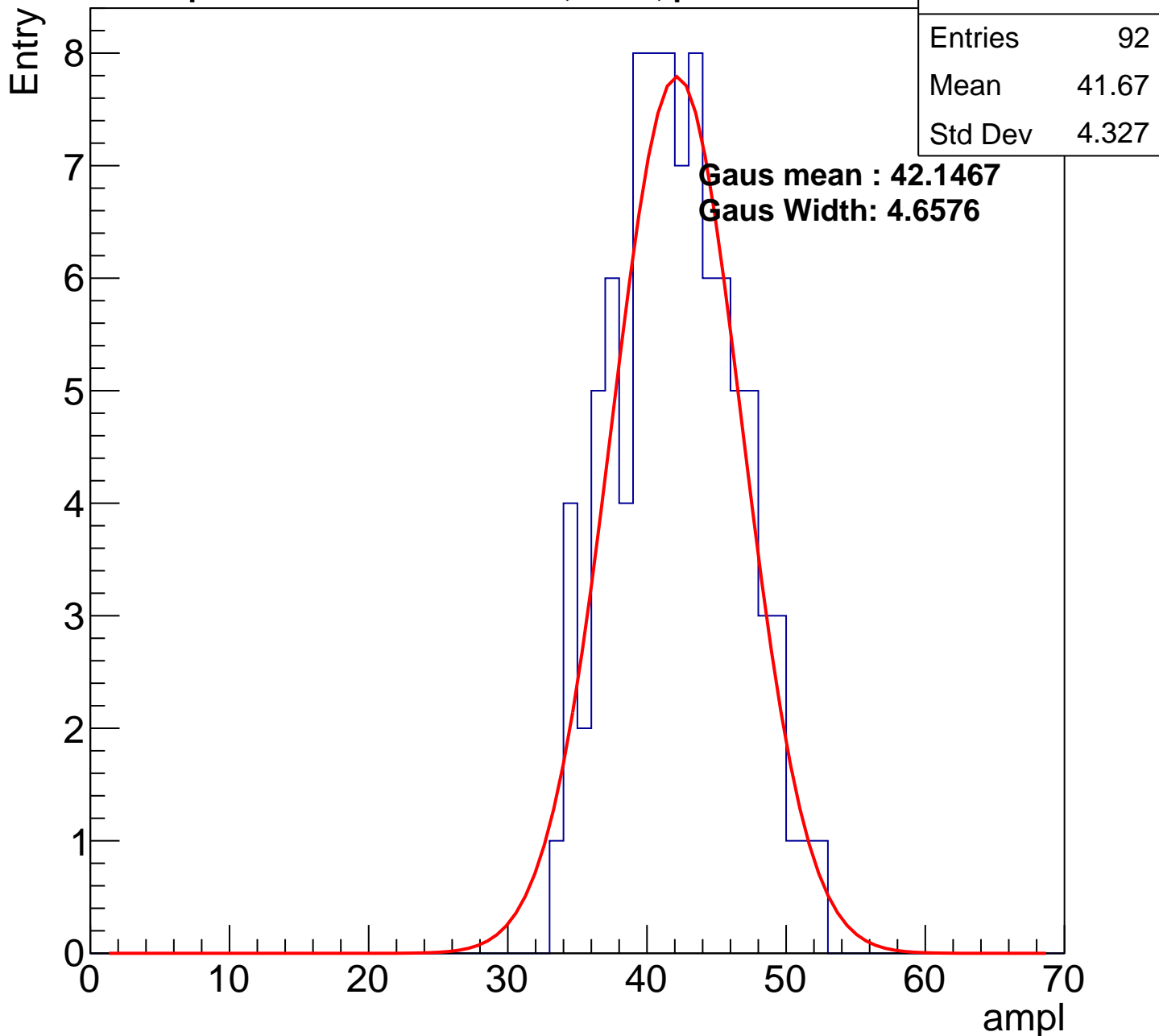
**Gaus mean : 36.0395**

**Gaus Width: 3.4417**



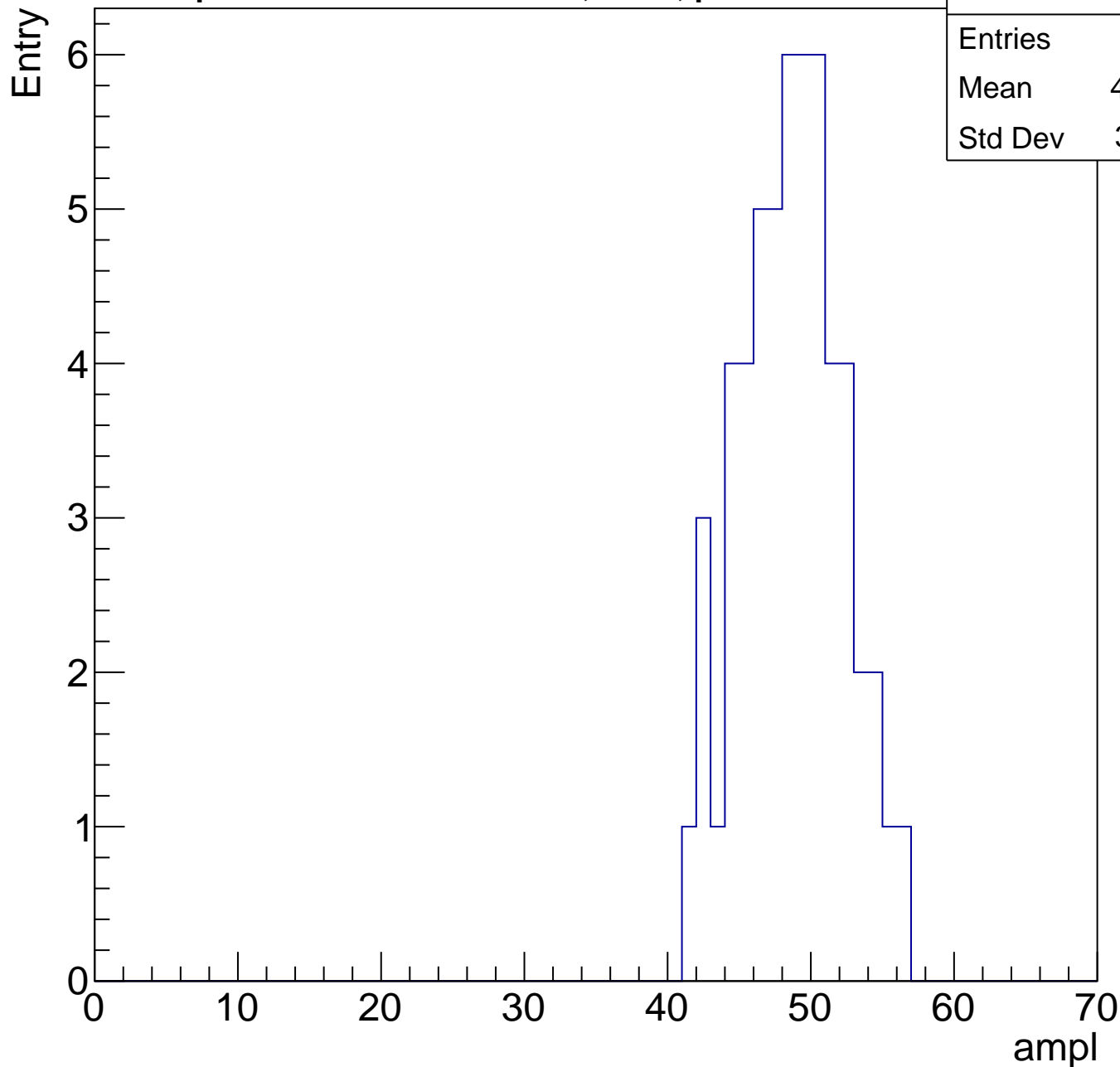
# B1L100S, U2-ch37, adc2

calib\_packv5\_042523\_0143.root, FC#4, port A2



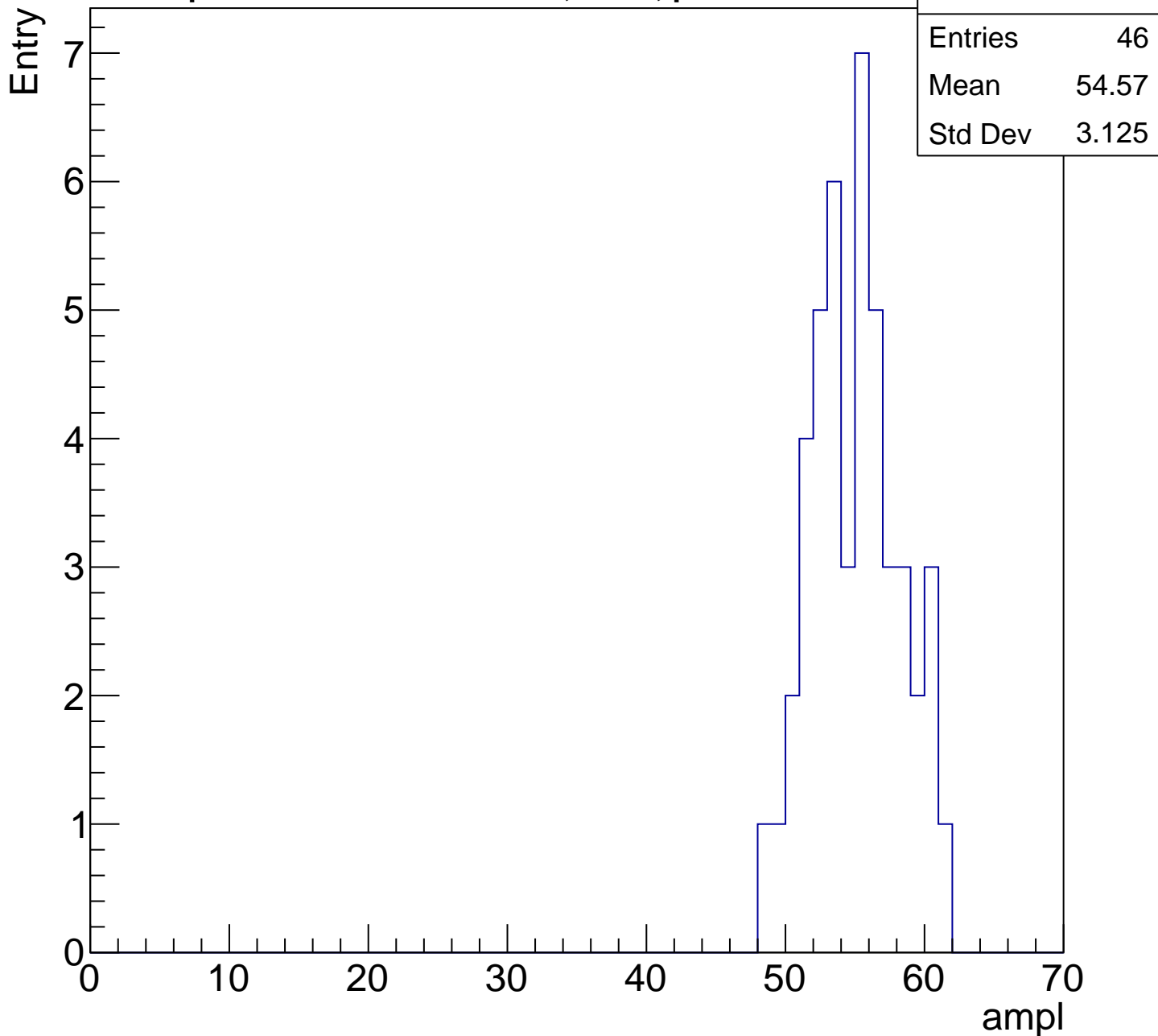
# B1L100S, U2-ch37, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2



# B1L100S, U2-ch37, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

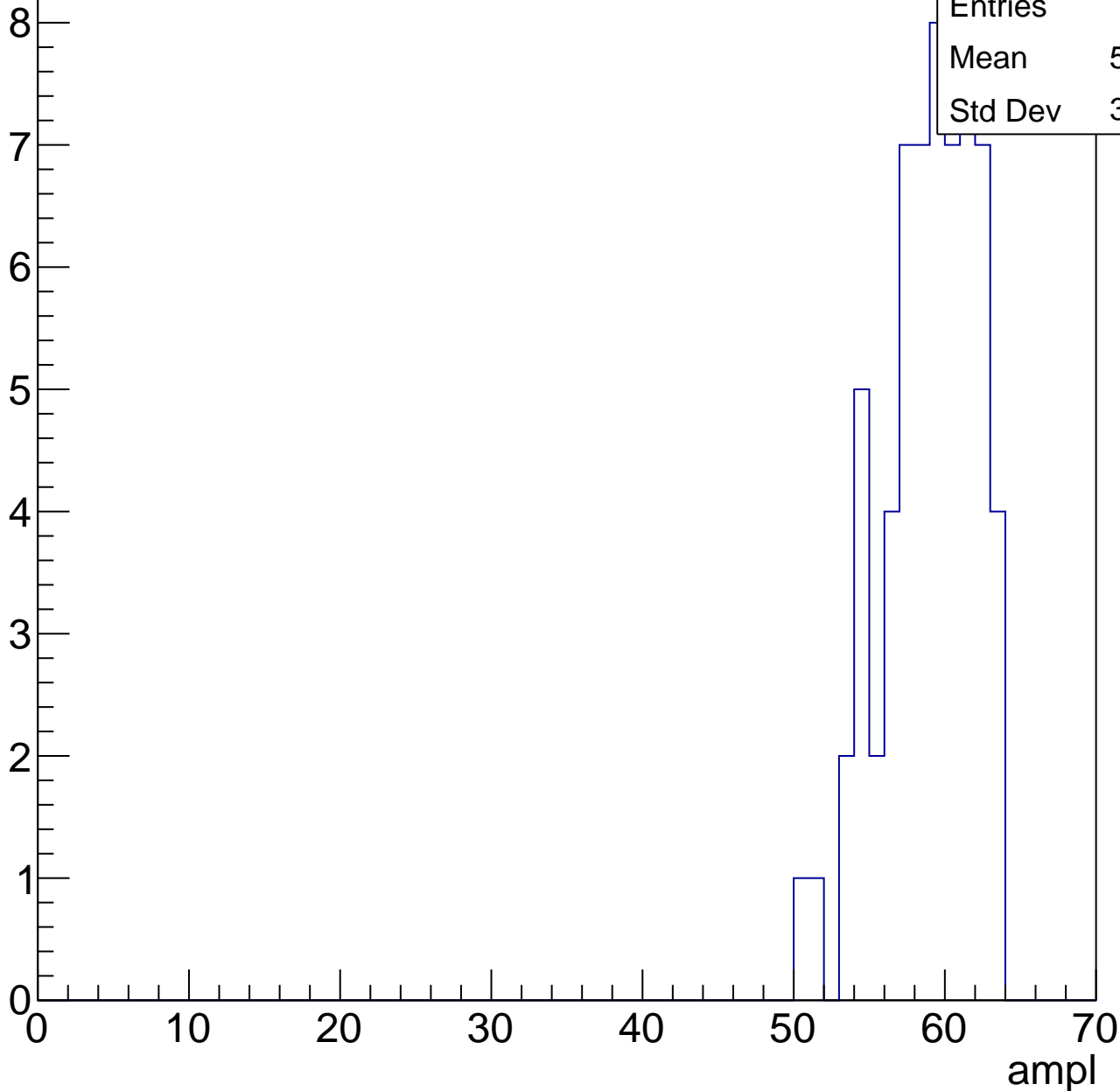


# B1L100S, U2-ch37, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	63
Mean	58.44
Std Dev	3.064

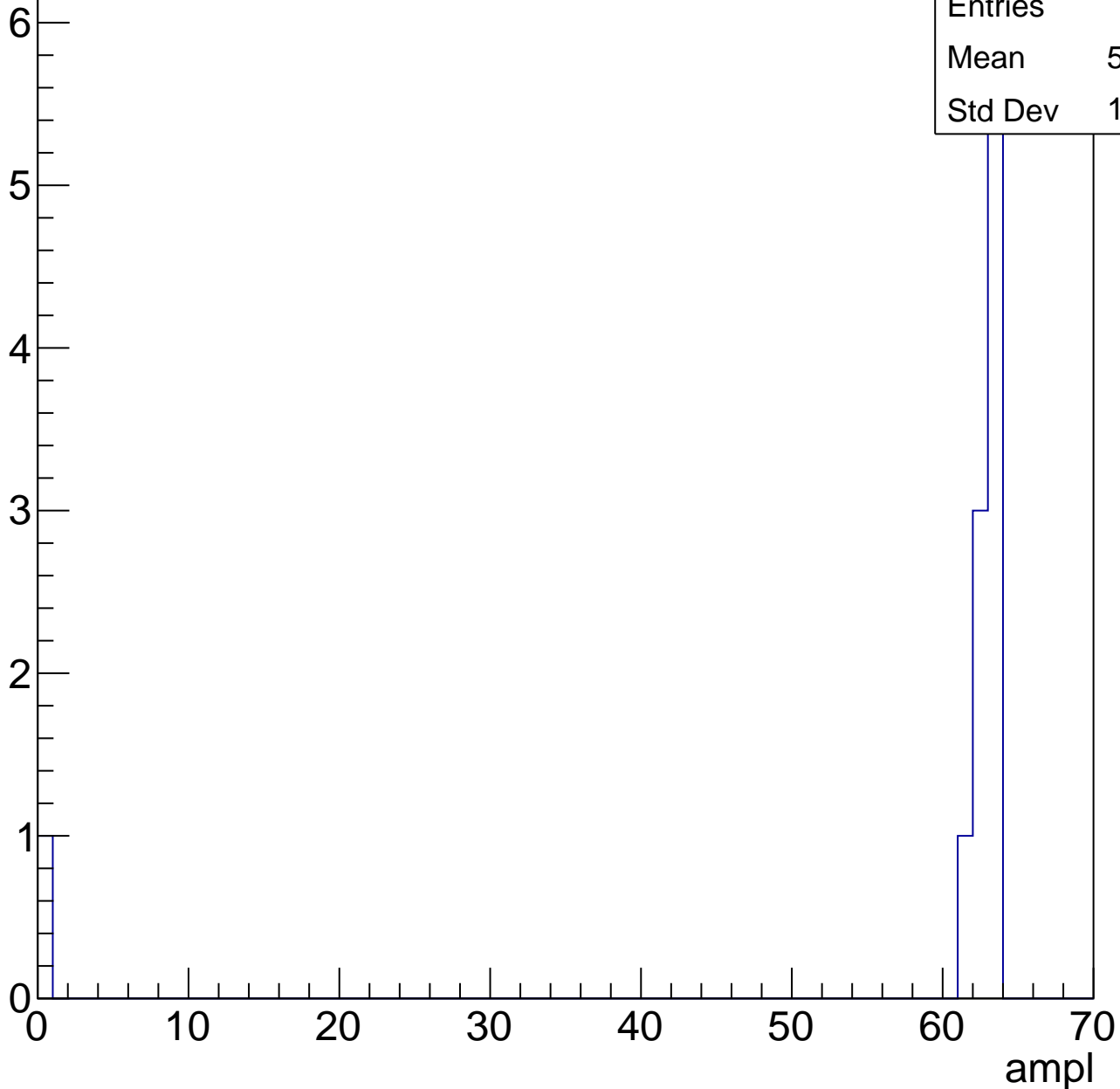


# B1L100S, U2-ch37, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	11
Mean	56.82
Std Dev	17.98





# B1L100S, U2-ch37, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L100S, U2-ch38, adc0

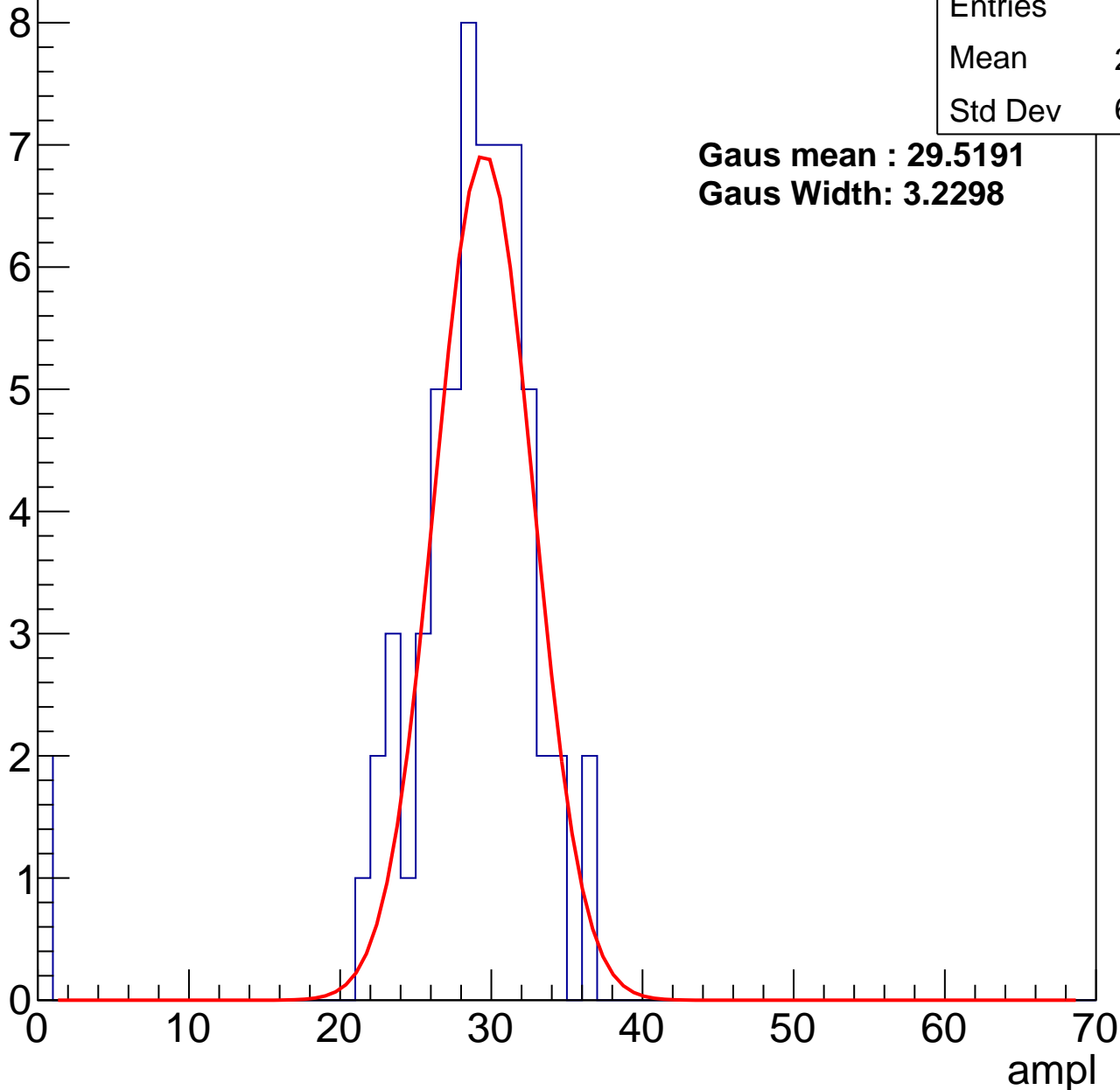
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	62
Mean	27.71
Std Dev	6.031

**Gaus mean : 29.5191**

**Gaus Width: 3.2298**



# B1L100S, U2-ch38, adc1

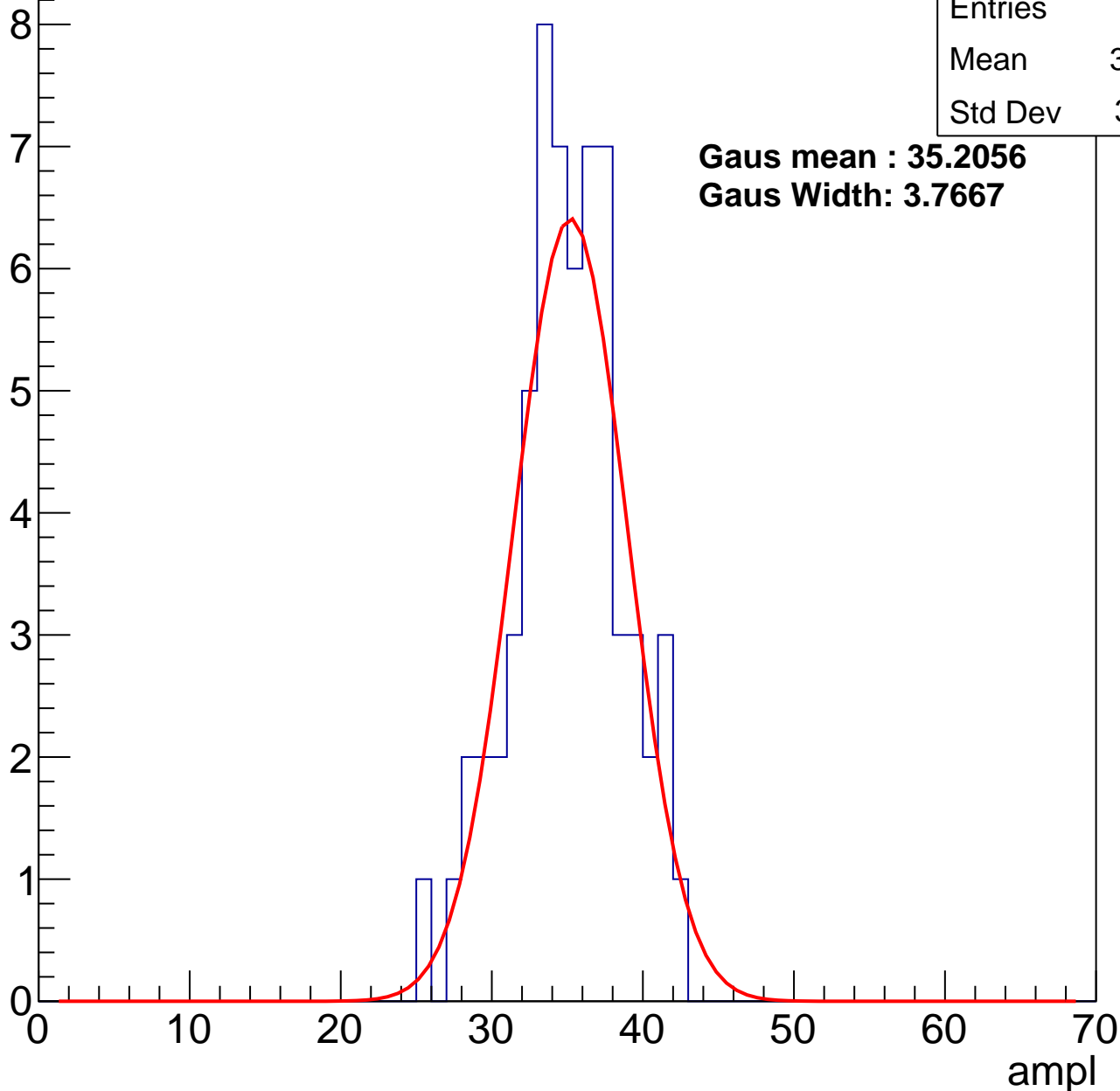
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	63
Mean	34.57
Std Dev	3.611

**Gaus mean : 35.2056**

**Gaus Width: 3.7667**



# B1L100S, U2-ch38, adc2

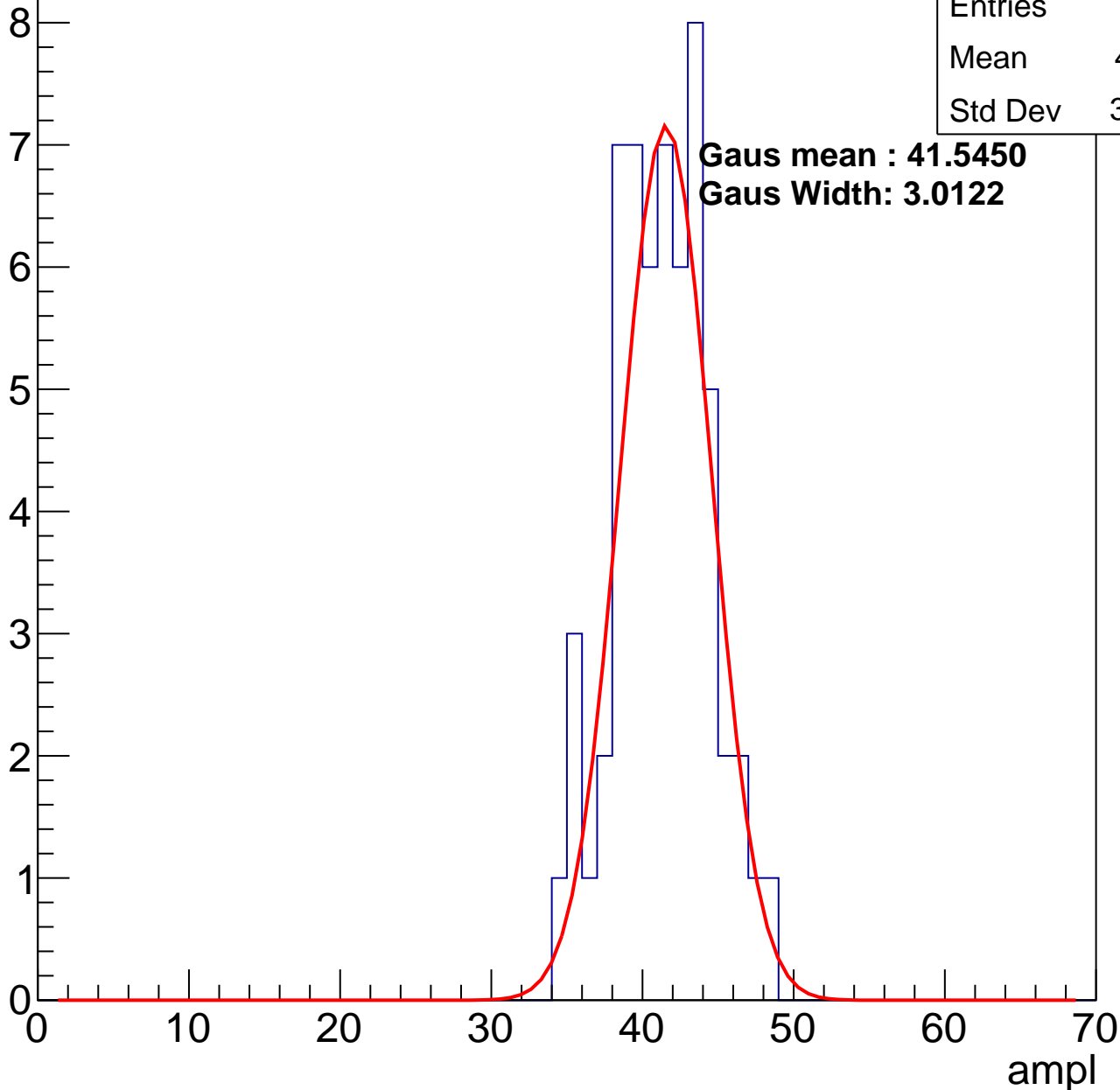
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	59
Mean	40.81
Std Dev	3.078

**Gaus mean : 41.5450**

**Gaus Width: 3.0122**

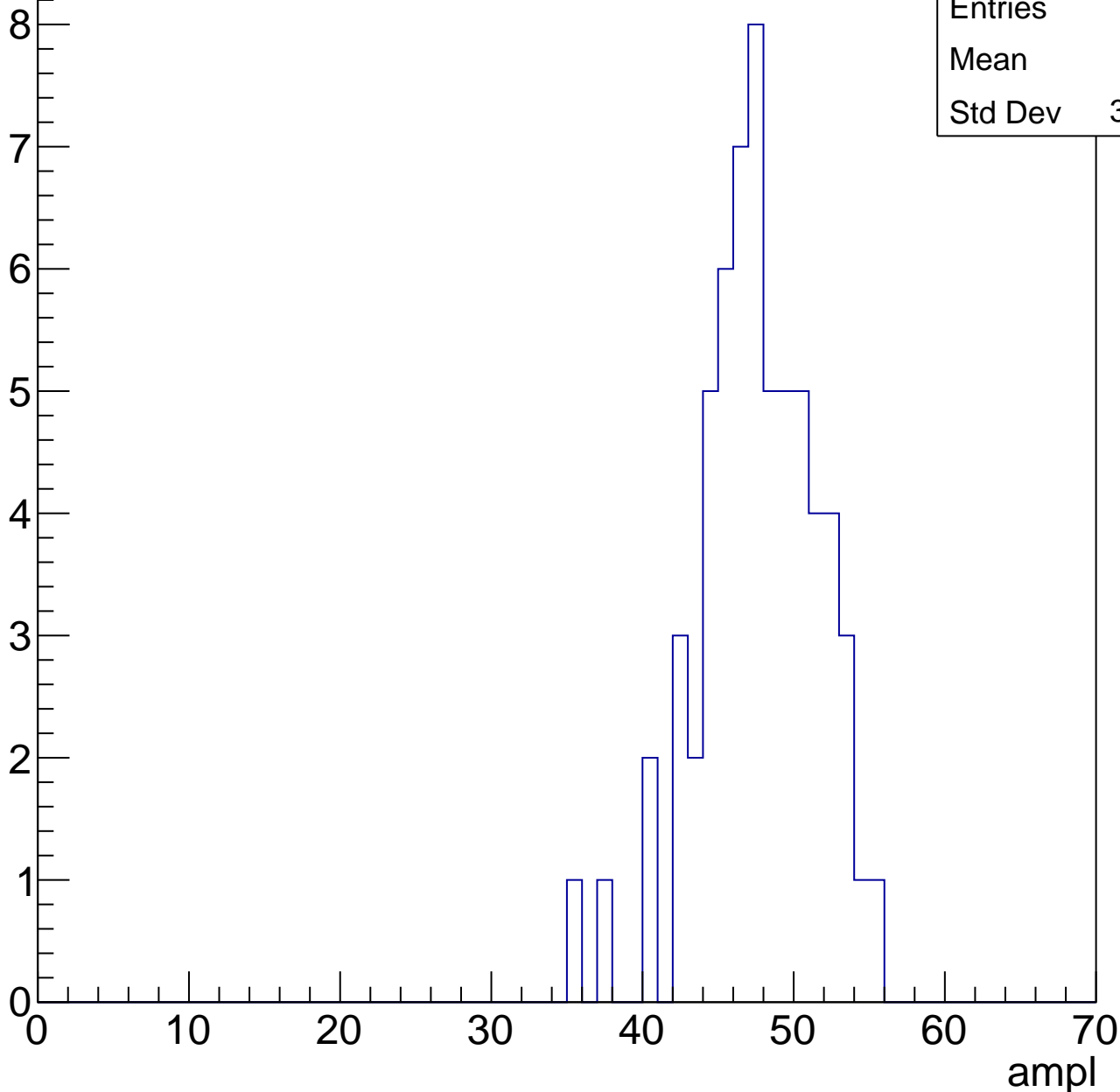


# B1L100S, U2-ch38, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	63
Mean	47.1
Std Dev	3.943

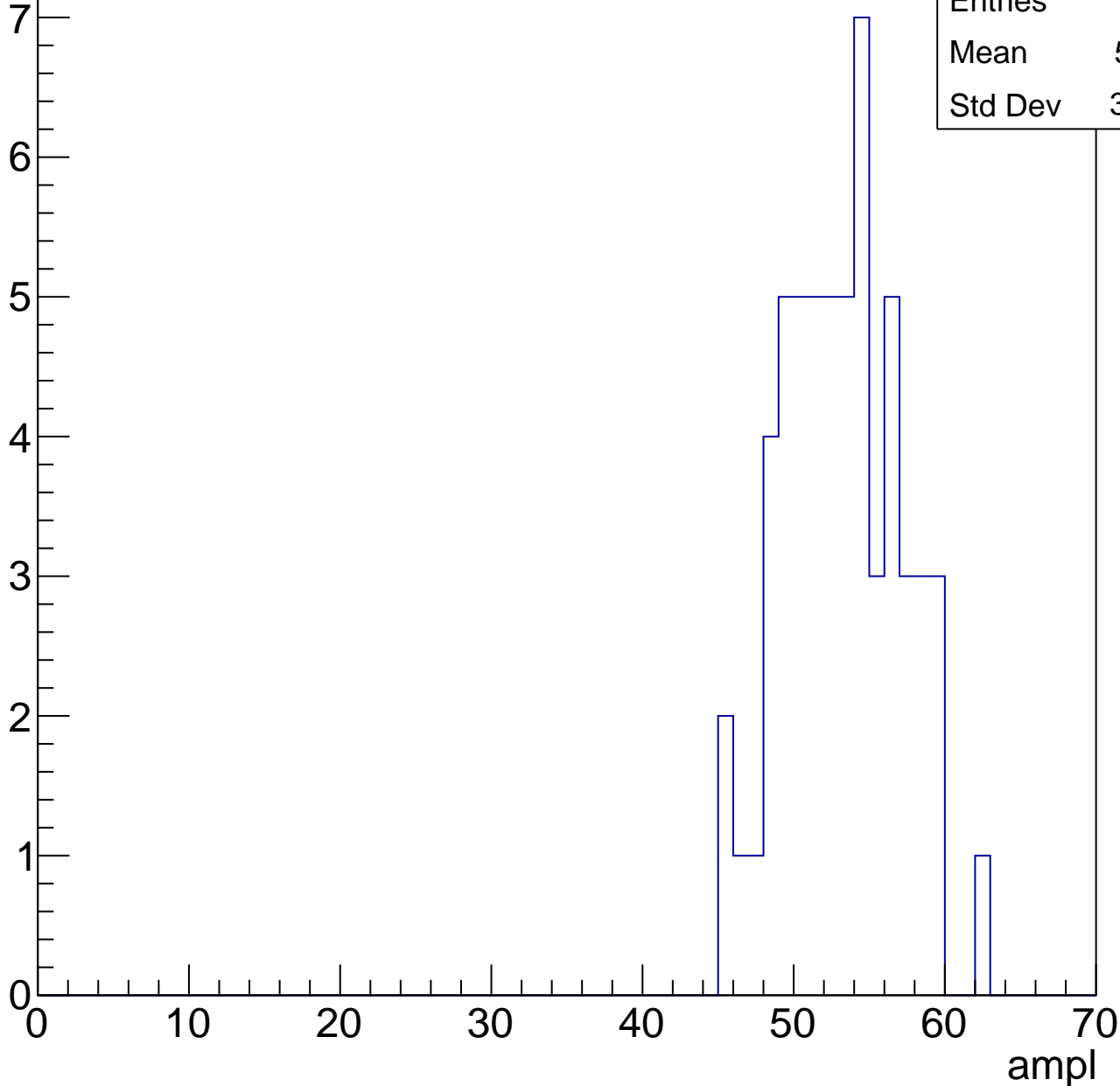


# B1L100S, U2-ch38, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

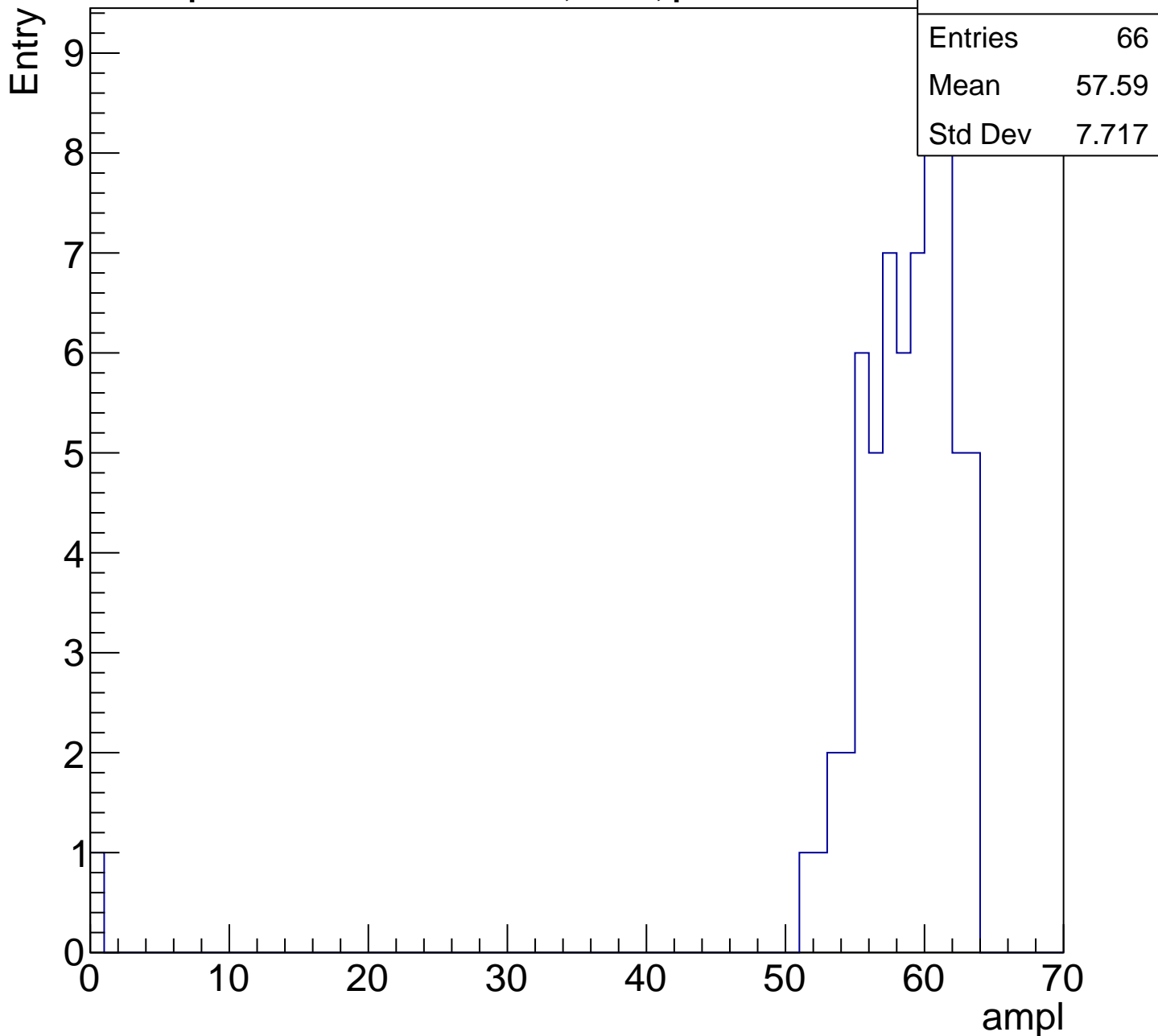
Entry

Entries	58
Mean	52.71
Std Dev	3.792



# B1L100S, U2-ch38, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

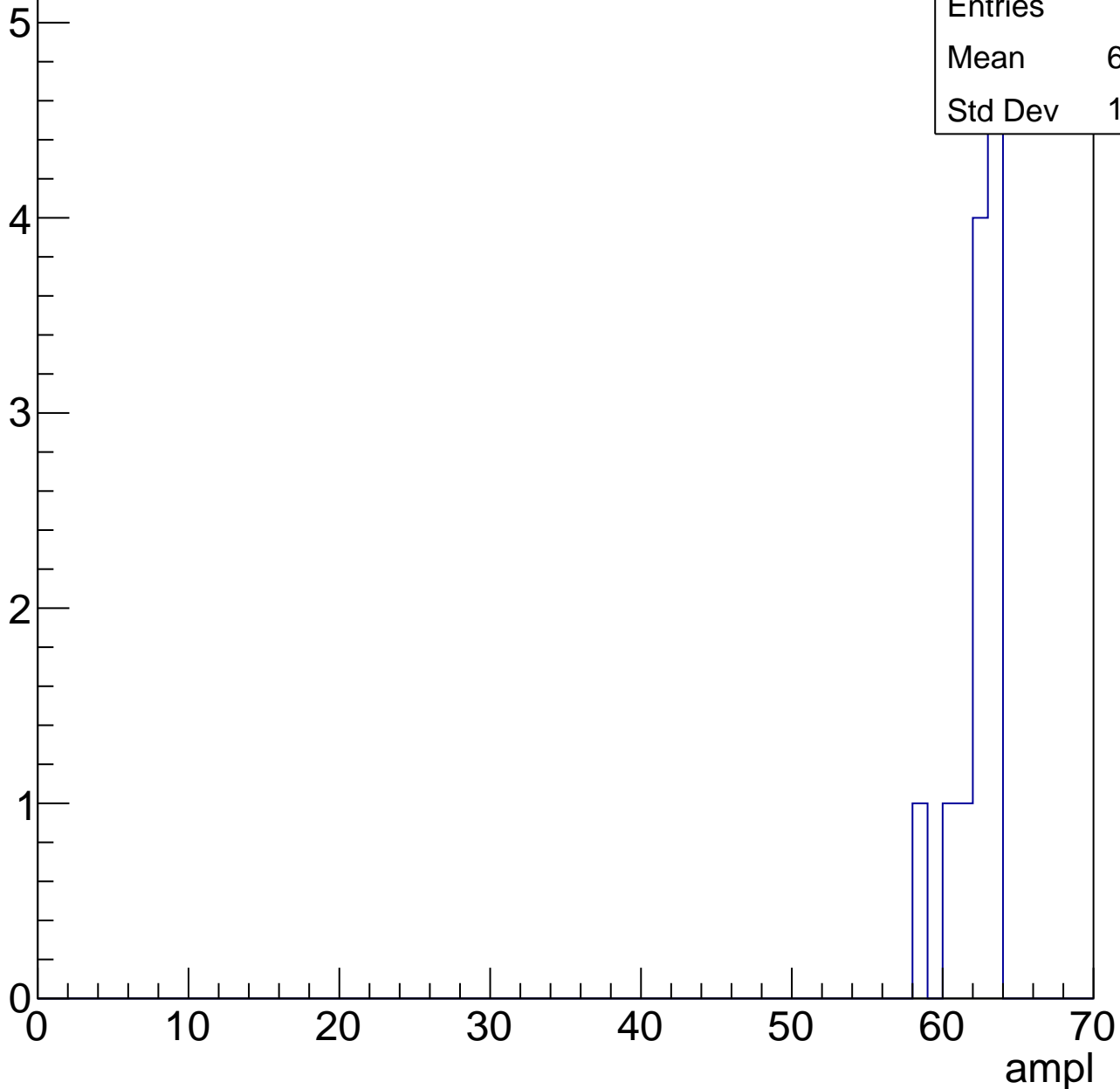


# B1L100S, U2-ch38, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	12
Mean	61.83
Std Dev	1.462





# B1L100S, U2-ch38, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



# B1L100S, U2-ch39, adc0

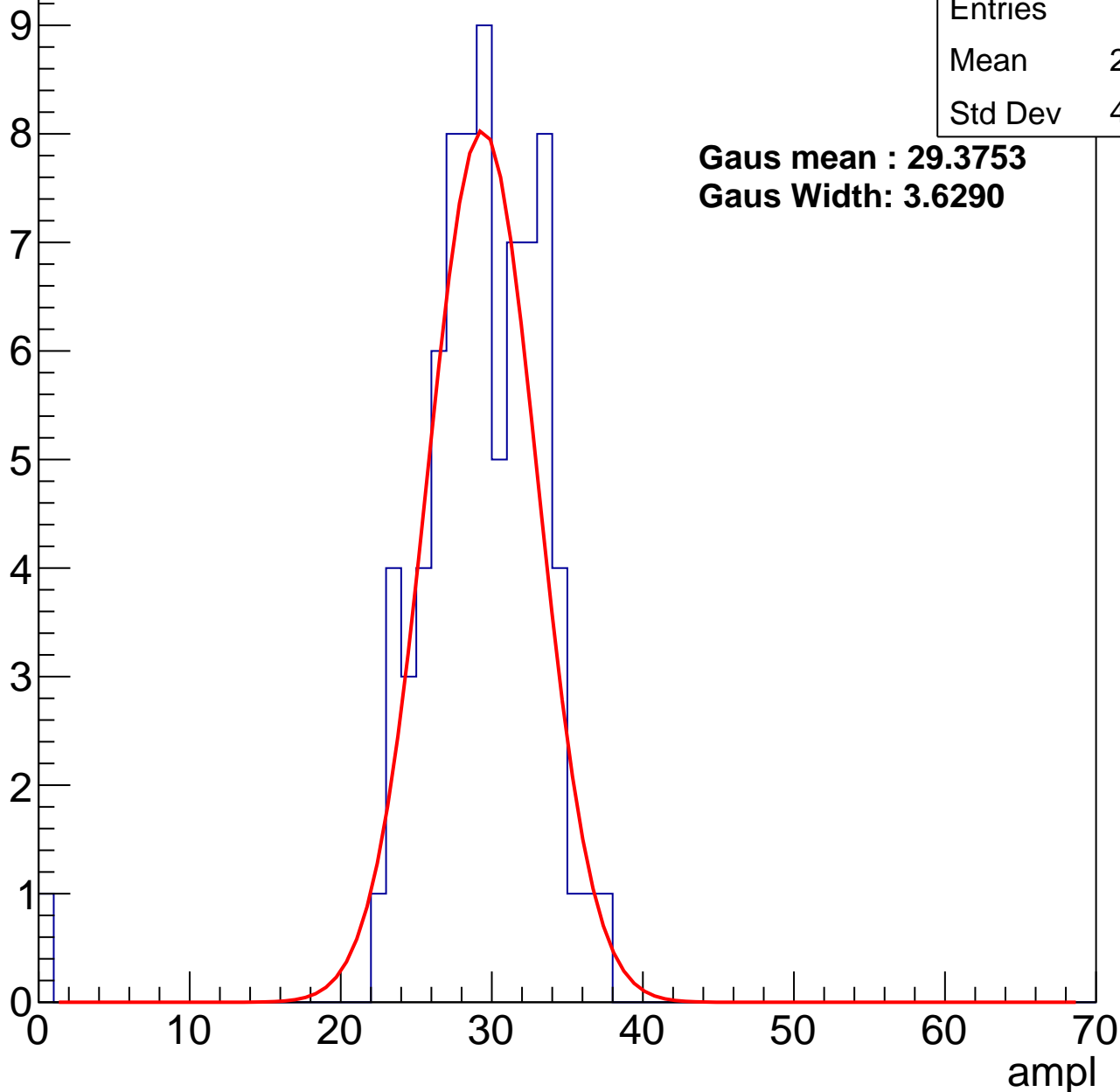
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	78
Mean	28.74
Std Dev	4.716

**Gaus mean : 29.3753**

**Gaus Width: 3.6290**



# B1L100S, U2-ch39, adc1

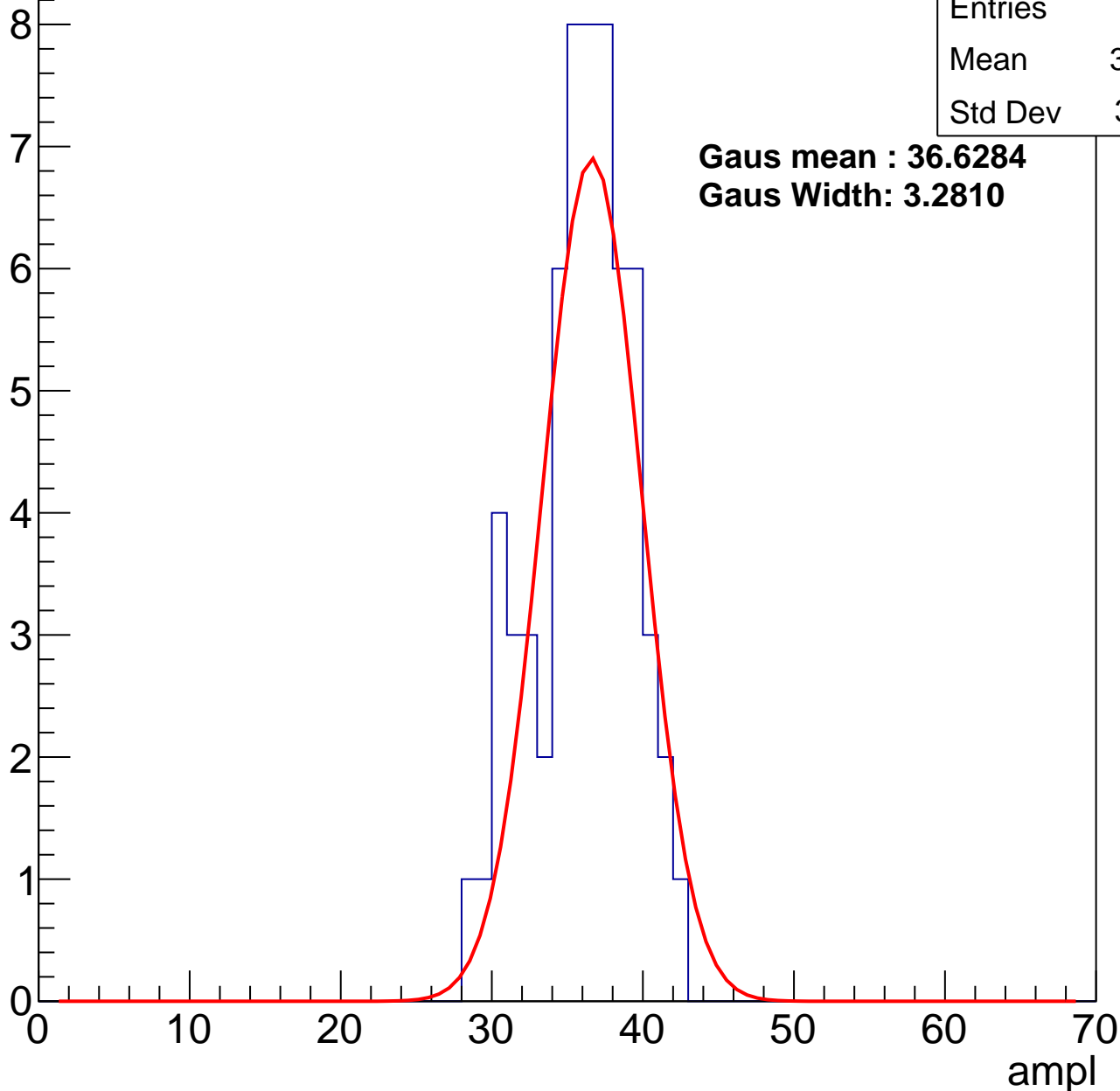
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	62
Mean	35.58
Std Dev	3.211

**Gaus mean : 36.6284**

**Gaus Width: 3.2810**



# B1L100S, U2-ch39, adc2

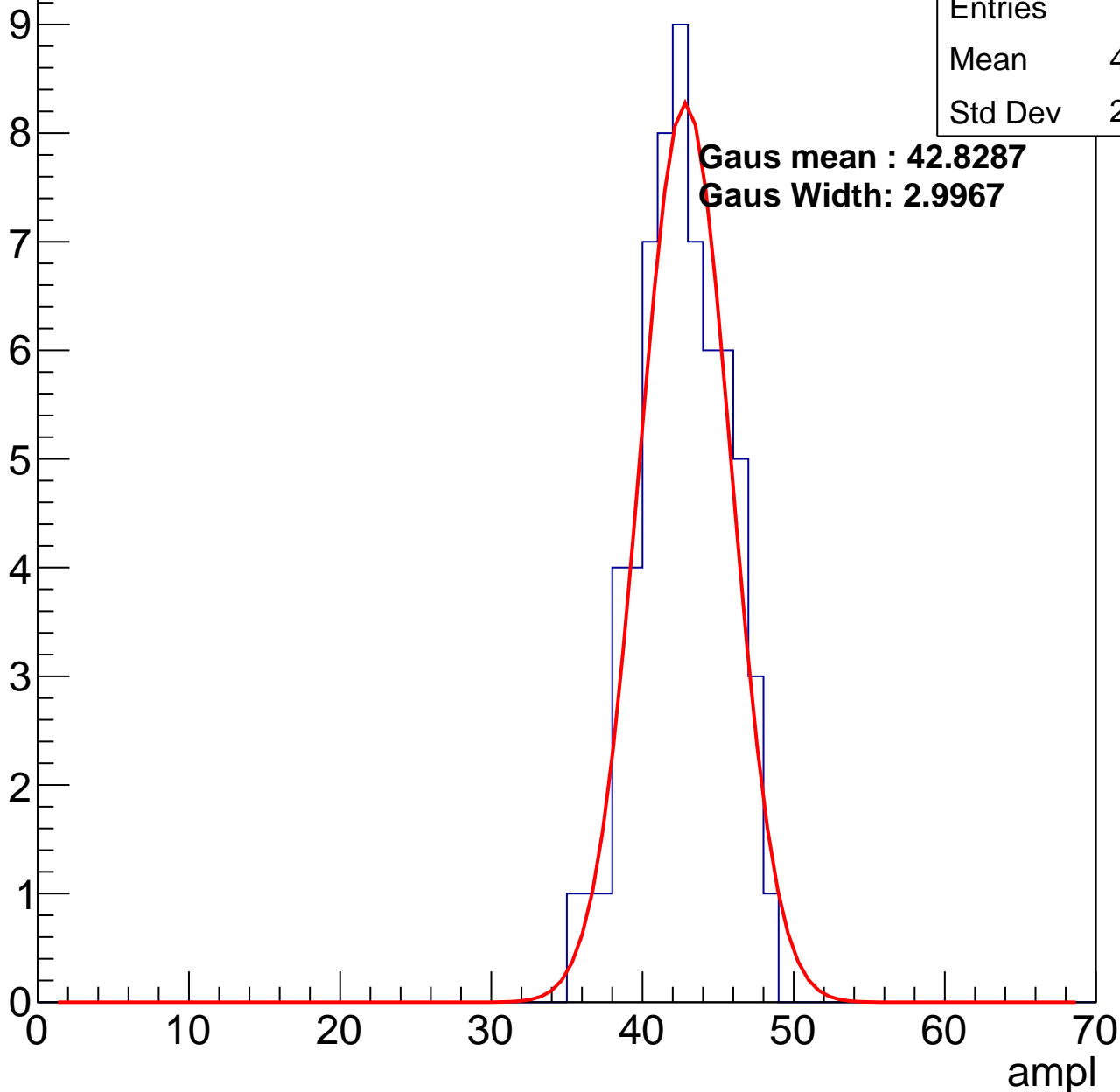
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	63
Mean	42.16
Std Dev	2.874

**Gaus mean : 42.8287**

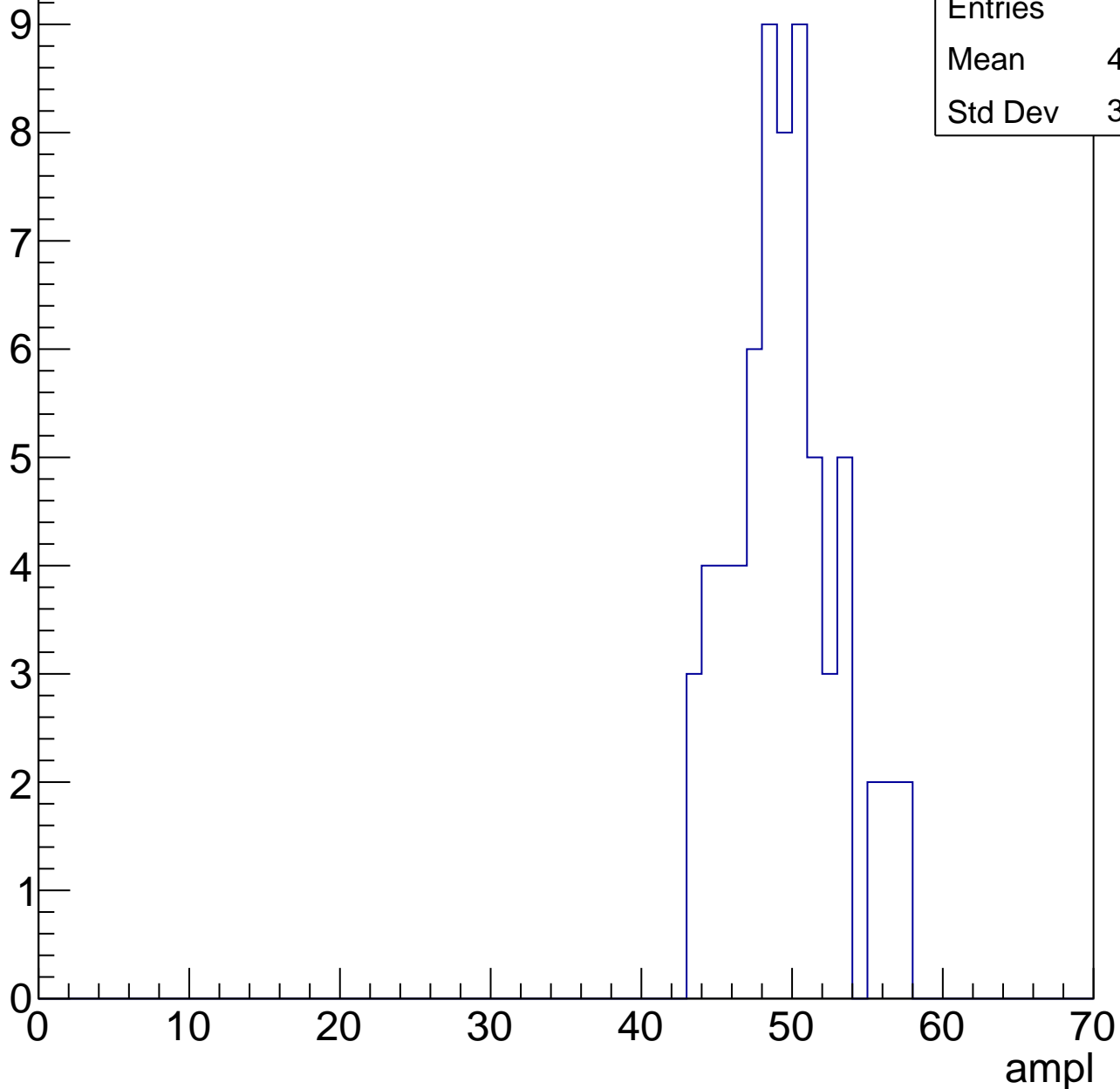
**Gaus Width: 2.9967**



# B1L100S, U2-ch39, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

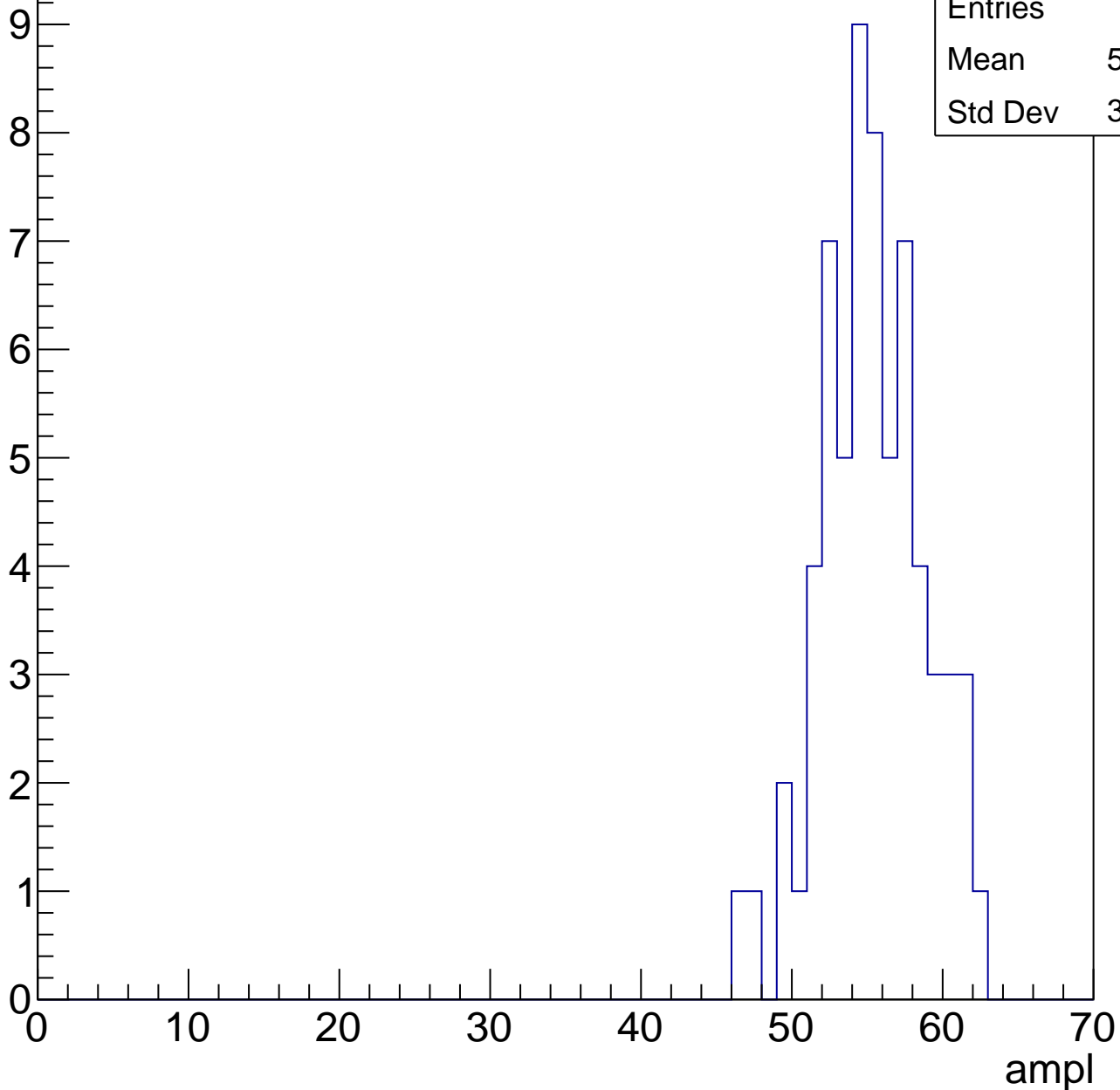


# B1L100S, U2-ch39, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	64
Mean	54.89
Std Dev	3.415



# B1L100S, U2-ch39, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

7

6

5

4

3

2

1

0

Entries	43
Mean	59.84
Std Dev	2.587

10

20

30

40

50

60

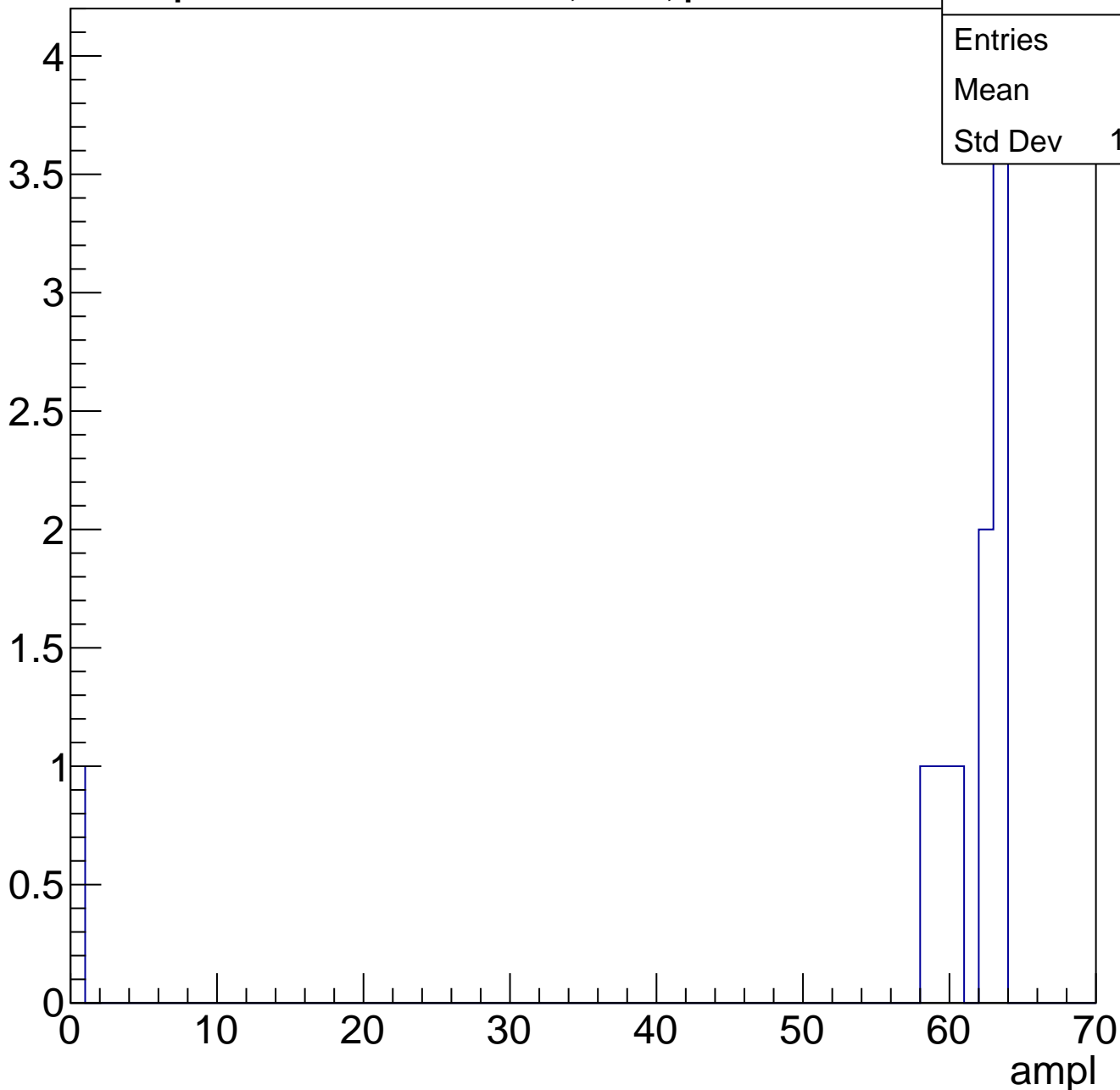
70

ampl

# B1L100S, U2-ch39, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry





# B1L100S, U2-ch39, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L100S, U2-ch40, adc0

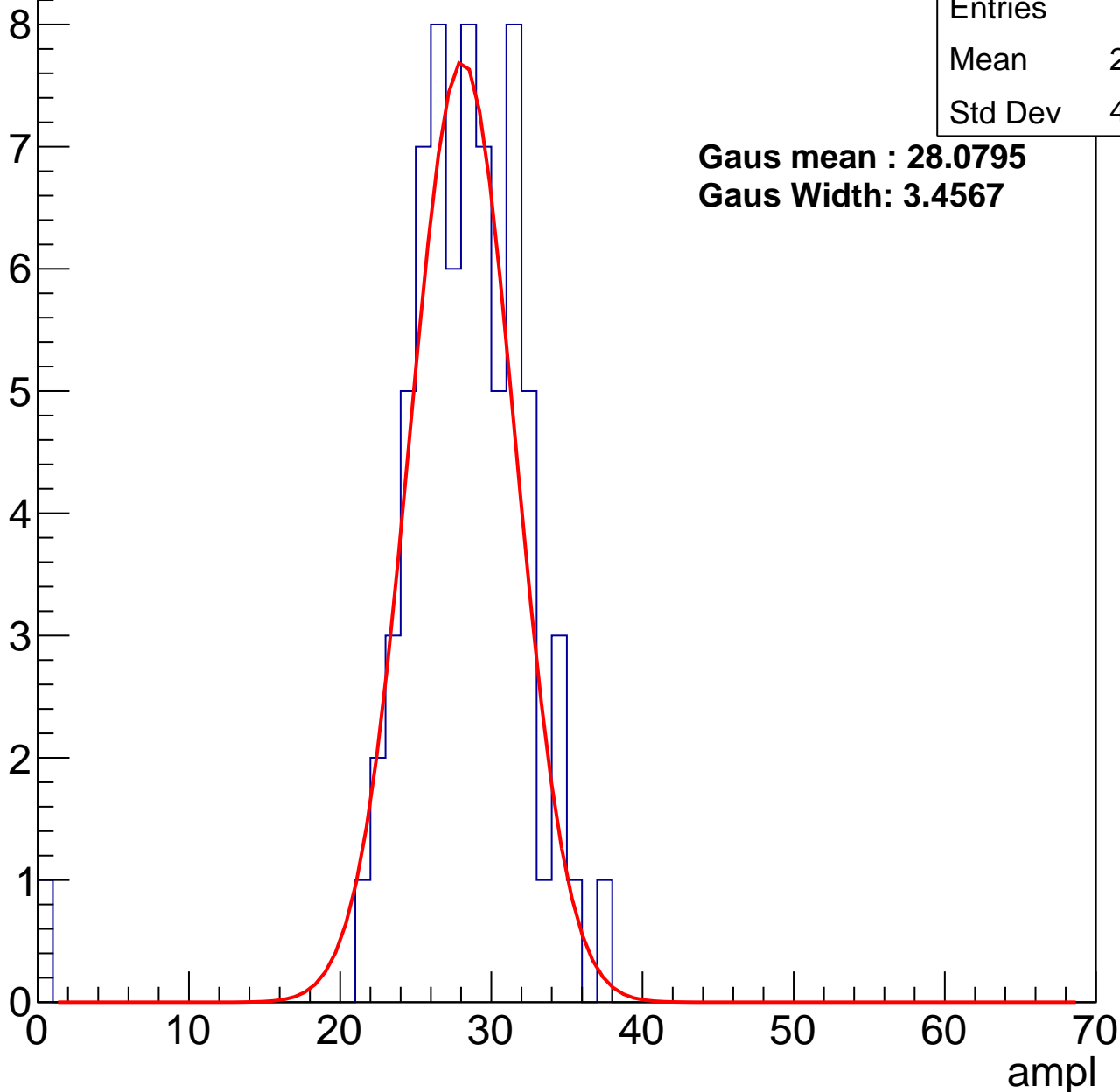
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	72
Mean	27.65
Std Dev	4.706

**Gaus mean : 28.0795**

**Gaus Width: 3.4567**



# B1L100S, U2-ch40, adc1

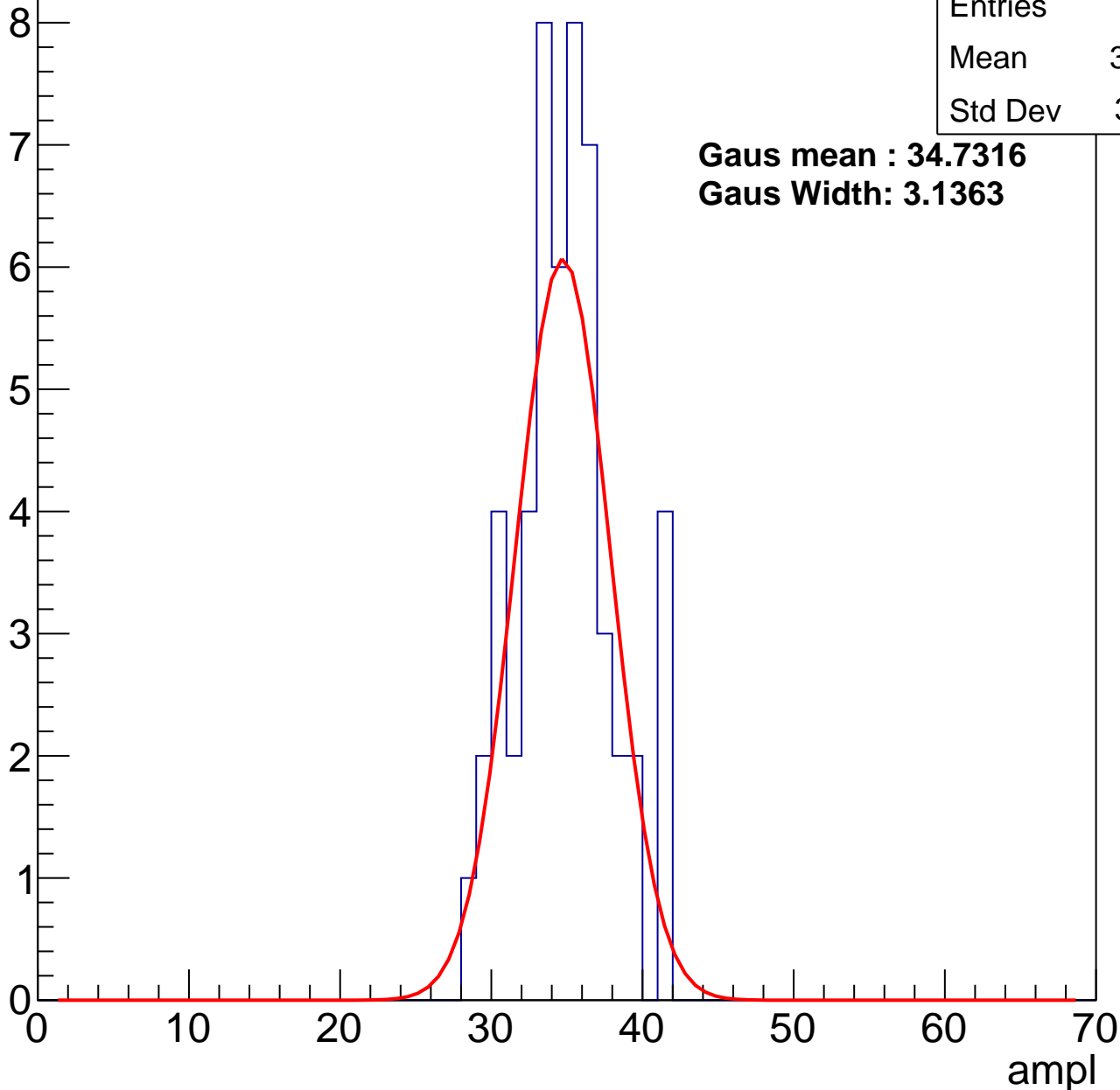
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	53
Mean	34.43
Std Dev	3.141

**Gaus mean : 34.7316**

**Gaus Width: 3.1363**



# B1L100S, U2-ch40, adc2

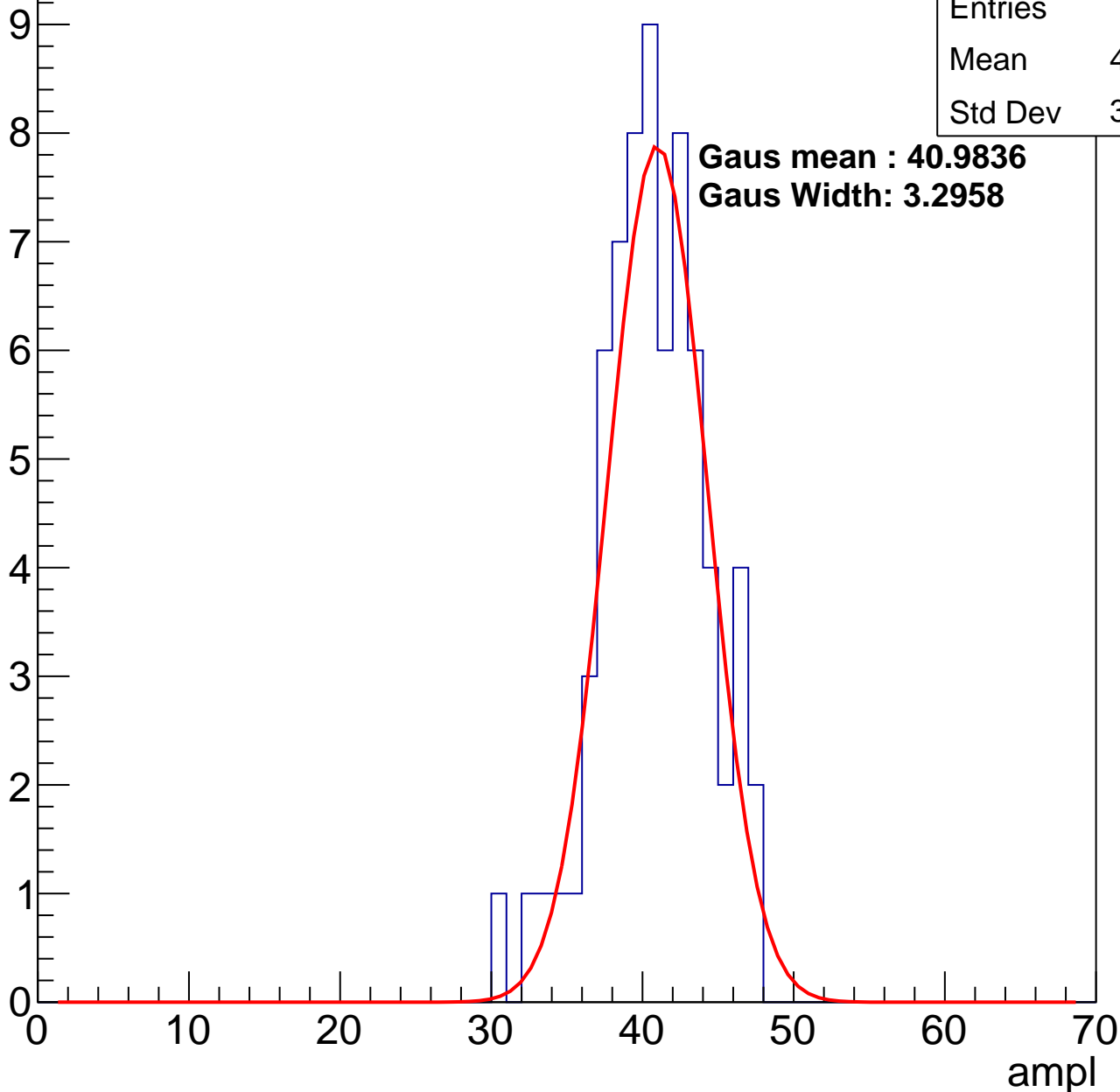
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	70
Mean	40.23
Std Dev	3.498

**Gaus mean : 40.9836**

**Gaus Width: 3.2958**



# B1L100S, U2-ch40, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	75
Mean	47.53
Std Dev	3.312

Entry

10

8

6

4

2

0

0

10

20

30

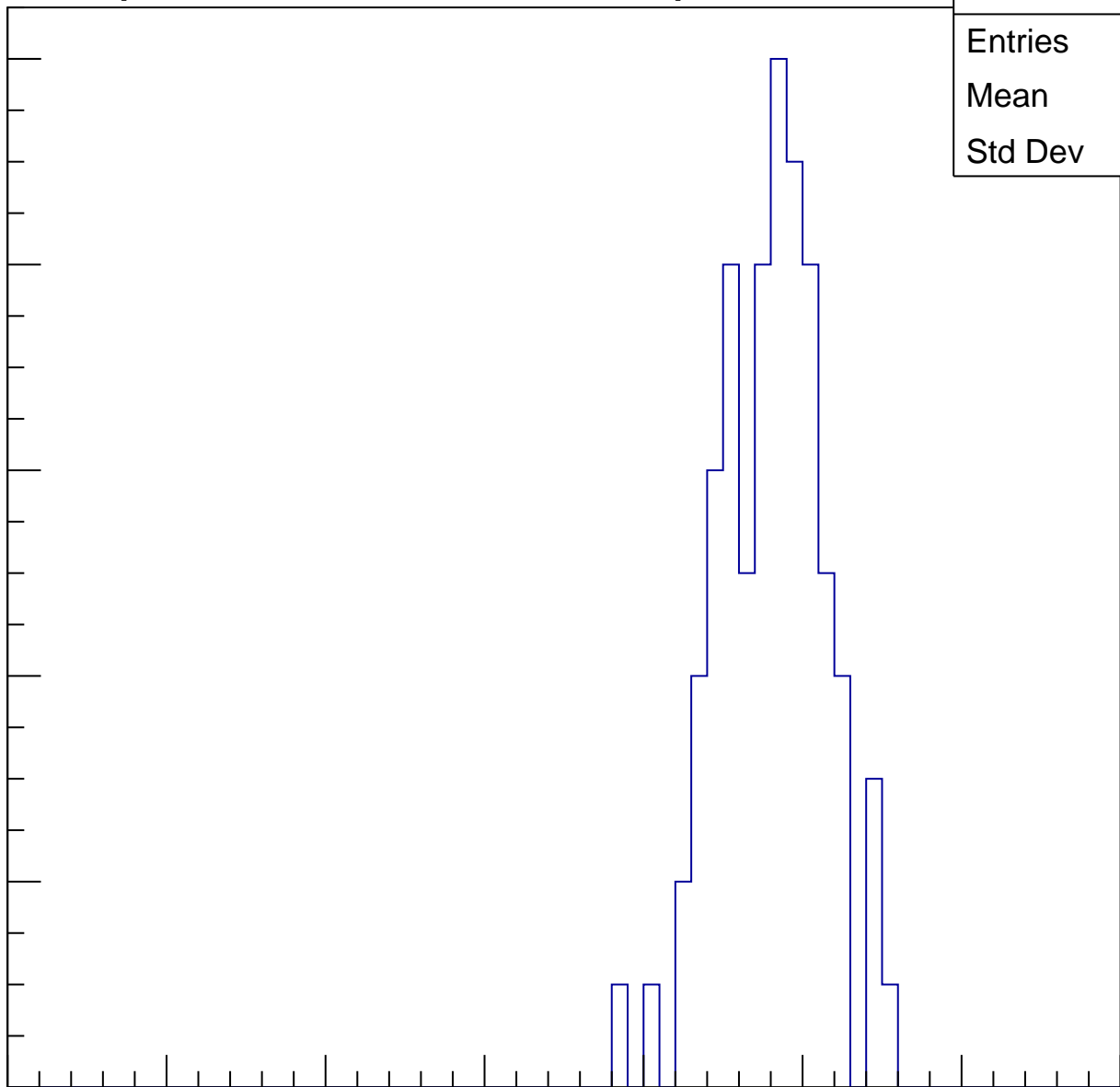
40

50

60

70

ampl

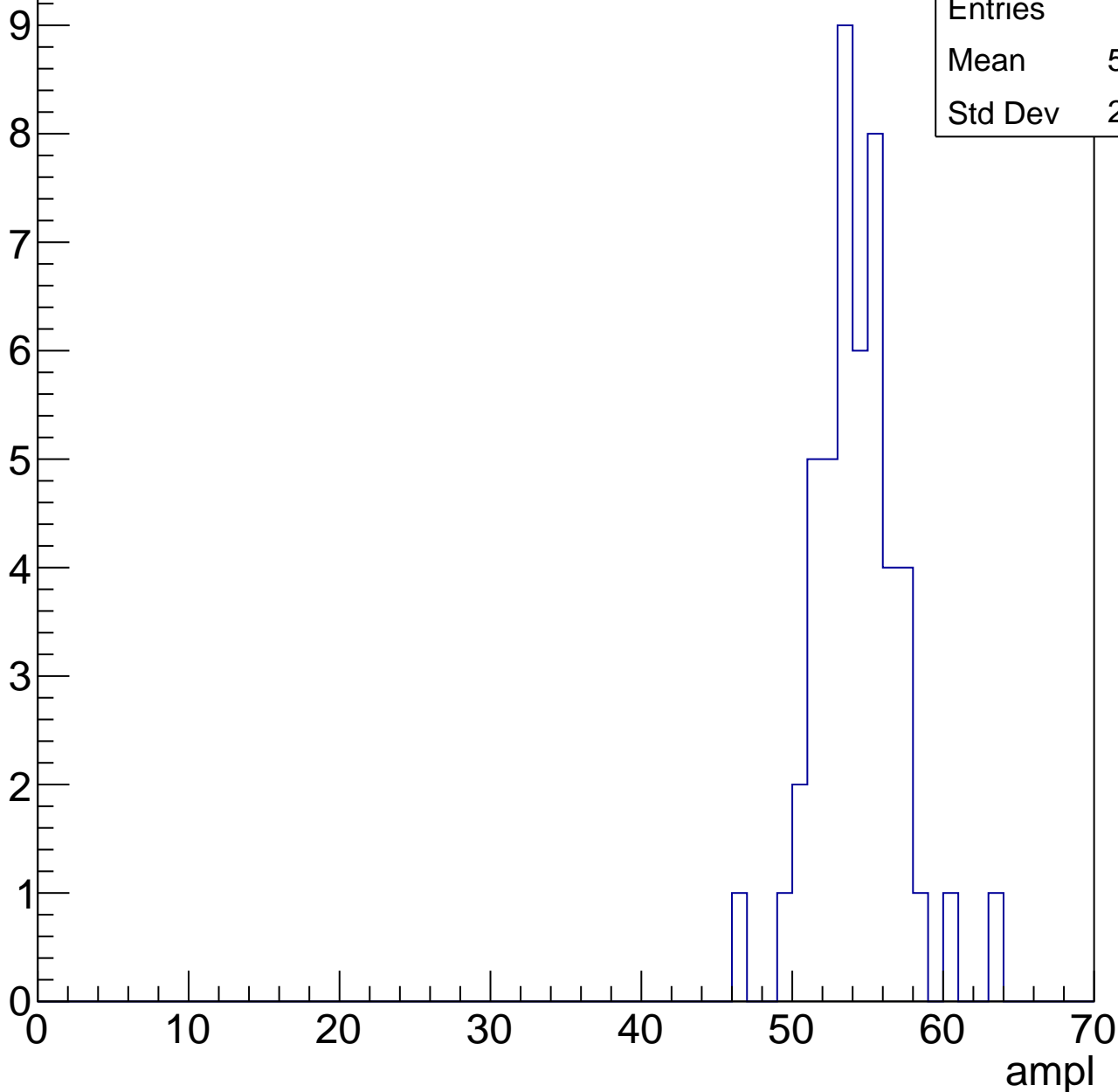


# B1L100S, U2-ch40, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	48
Mean	53.83
Std Dev	2.838



# B1L100S, U2-ch40, adc5

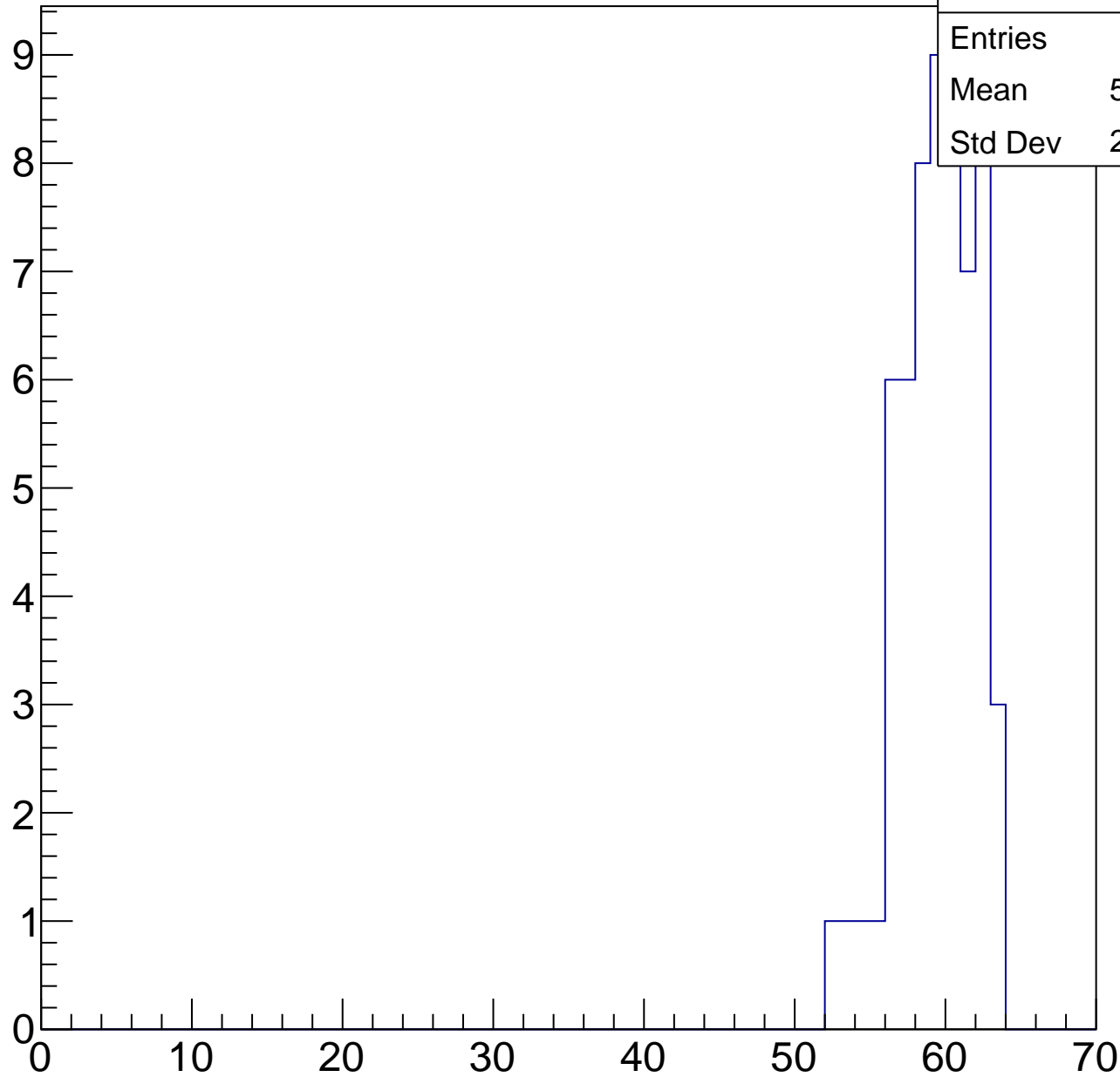
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	59
Mean	58.97
Std Dev	2.497

ampl

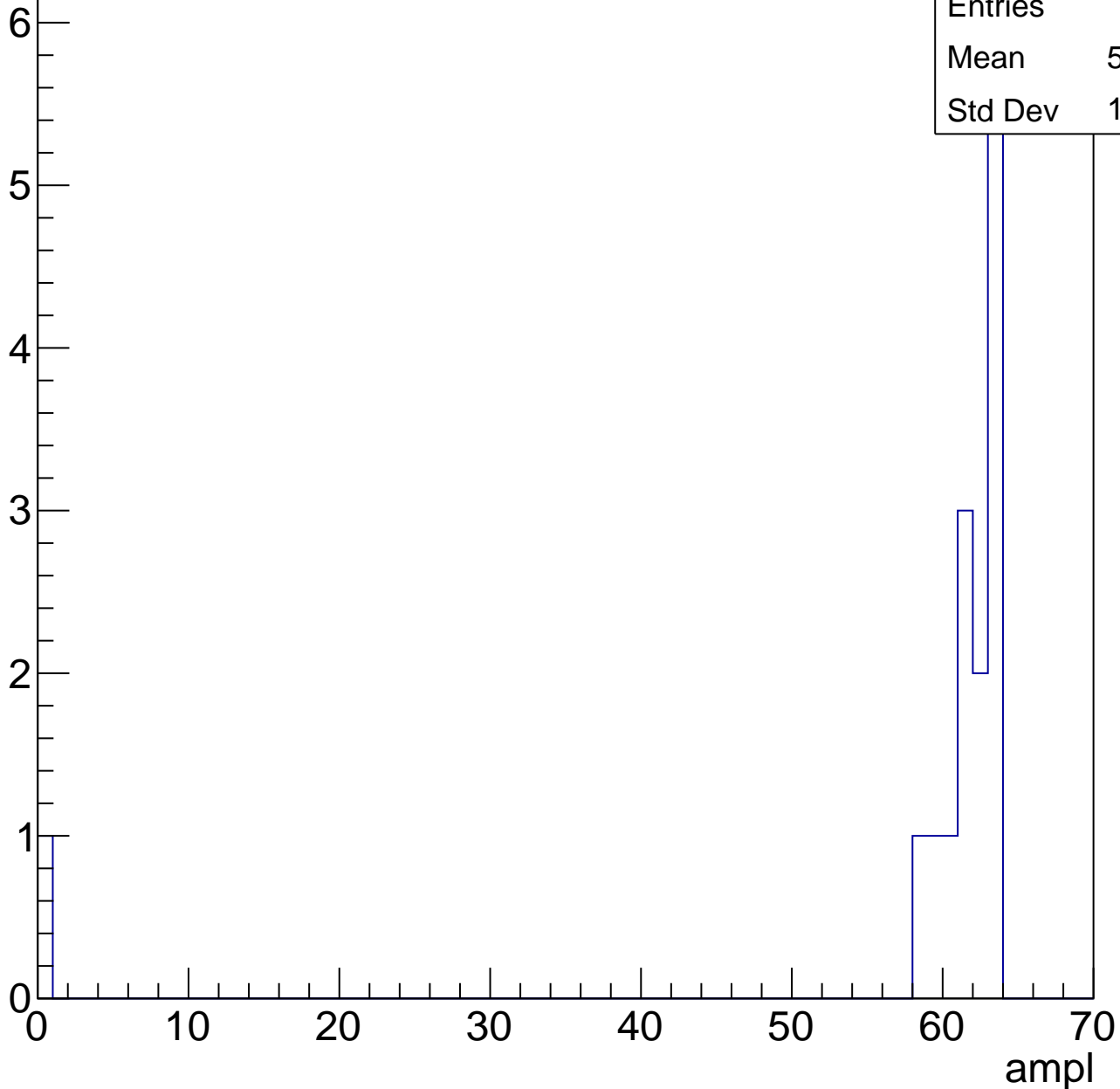


# B1L100S, U2-ch40, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	15
Mean	57.47
Std Dev	15.44





# B1L100S, U2-ch40, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

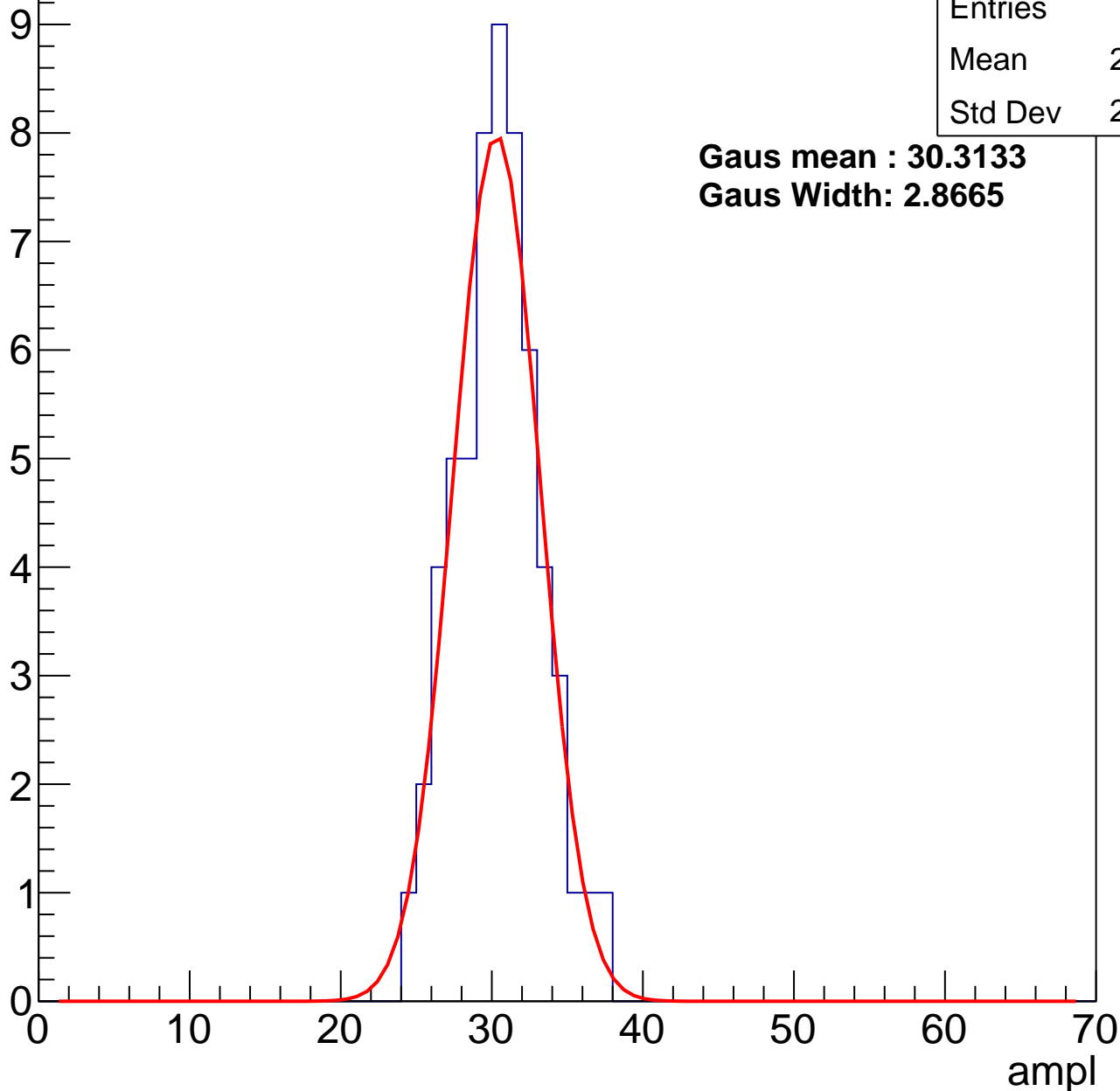


Entries	0
Mean	0
Std Dev	0

# B1L100S, U2-ch41, adc0

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	58
Mean	29.95
Std Dev	2.782

# B1L100S, U2-ch41, adc1

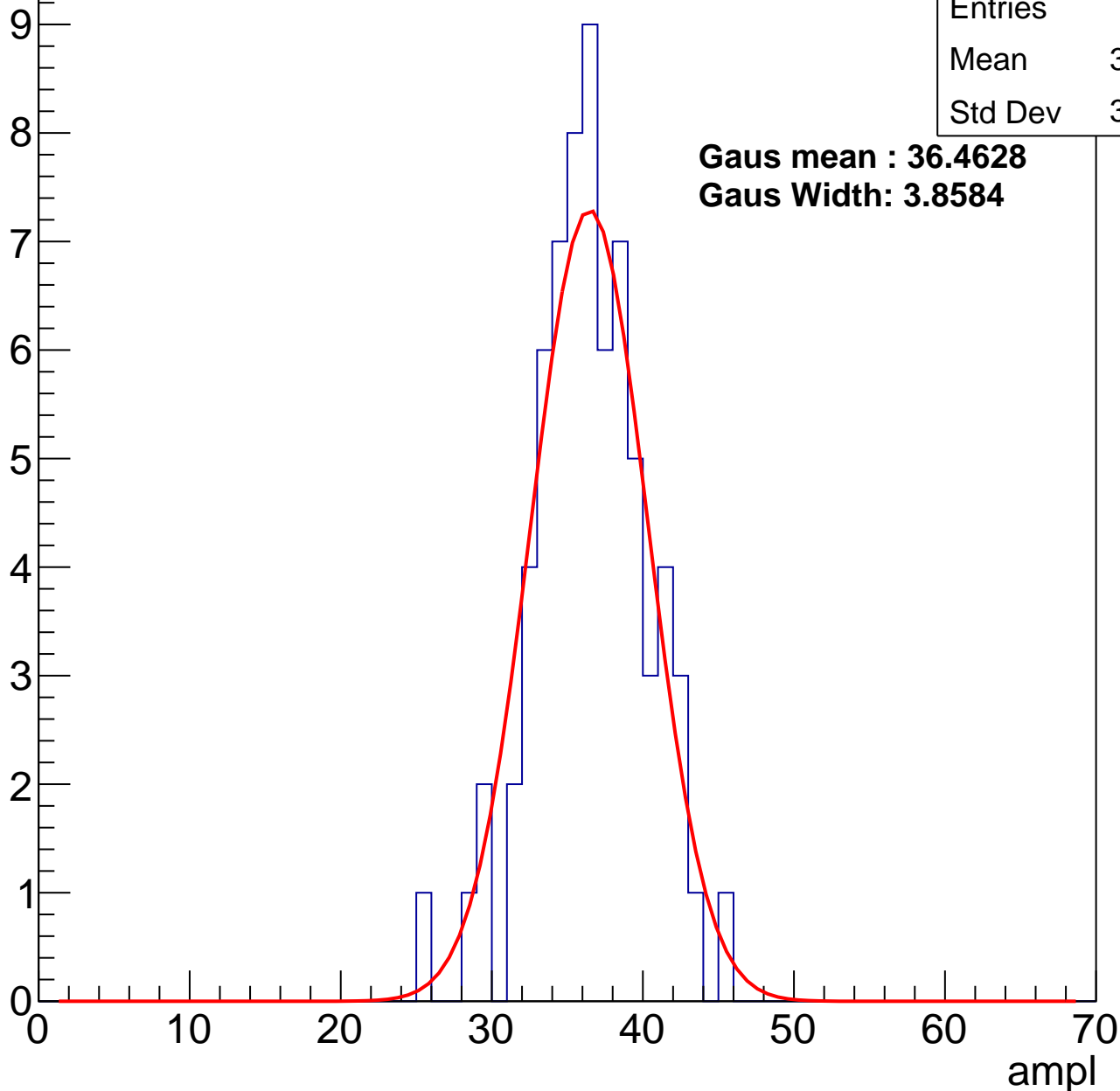
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	70
Mean	36.03
Std Dev	3.688

**Gaus mean : 36.4628**

**Gaus Width: 3.8584**



# B1L100S, U2-ch41, adc2

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	82
Mean	43.44
Std Dev	3.538

**Gaus mean : 43.7904**

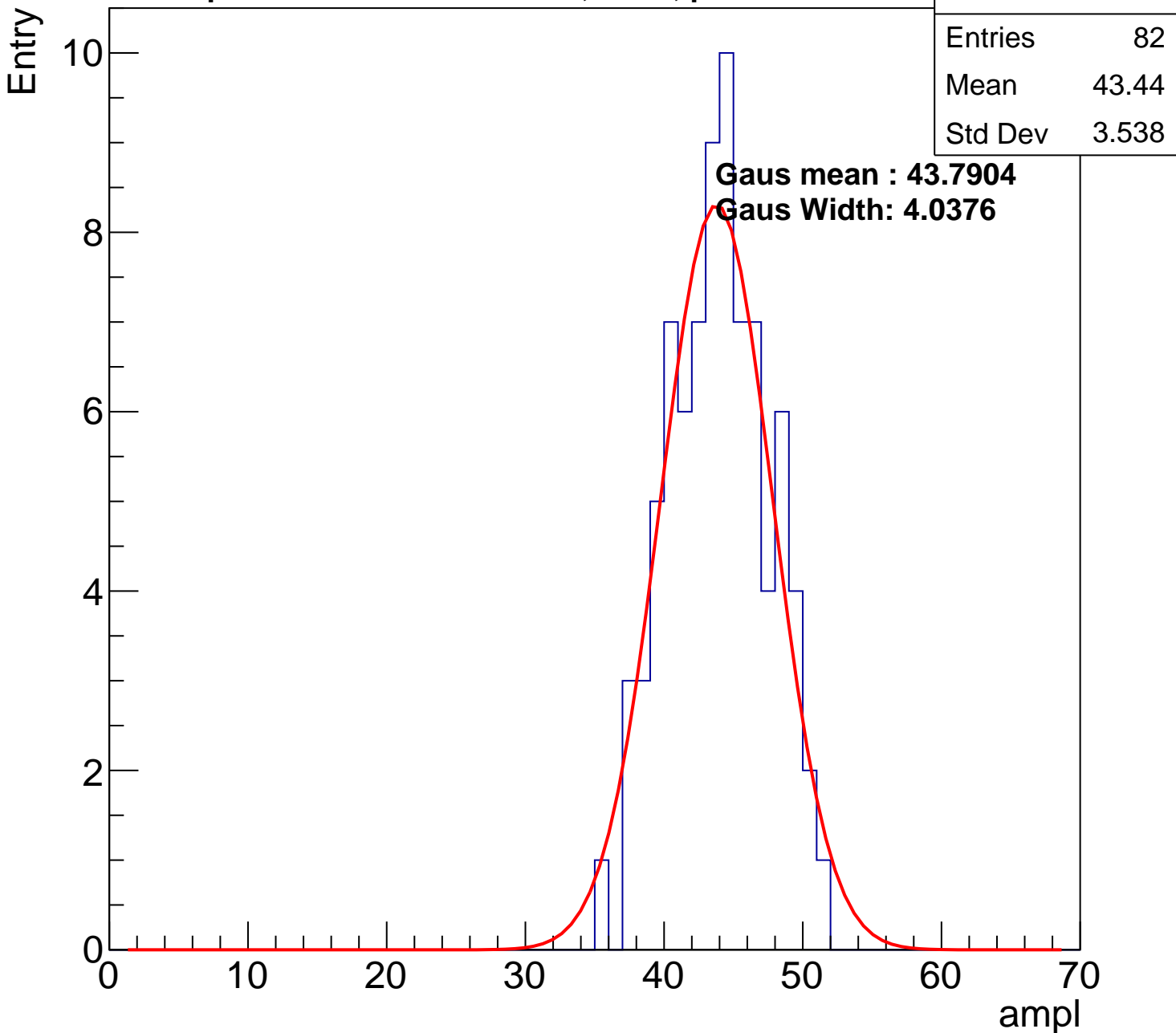
**Gaus Width: 4.0376**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

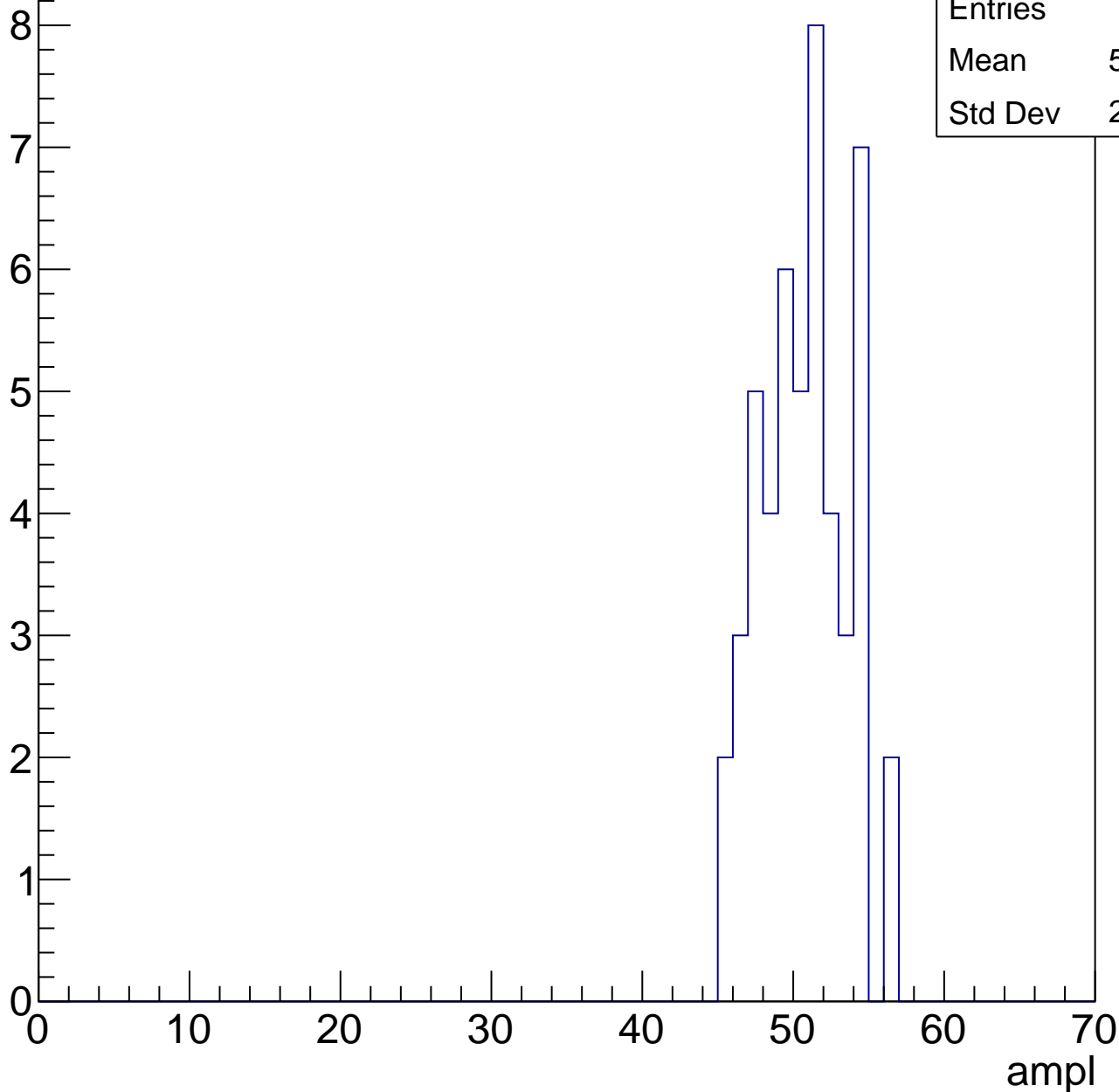


# B1L100S, U2-ch41, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

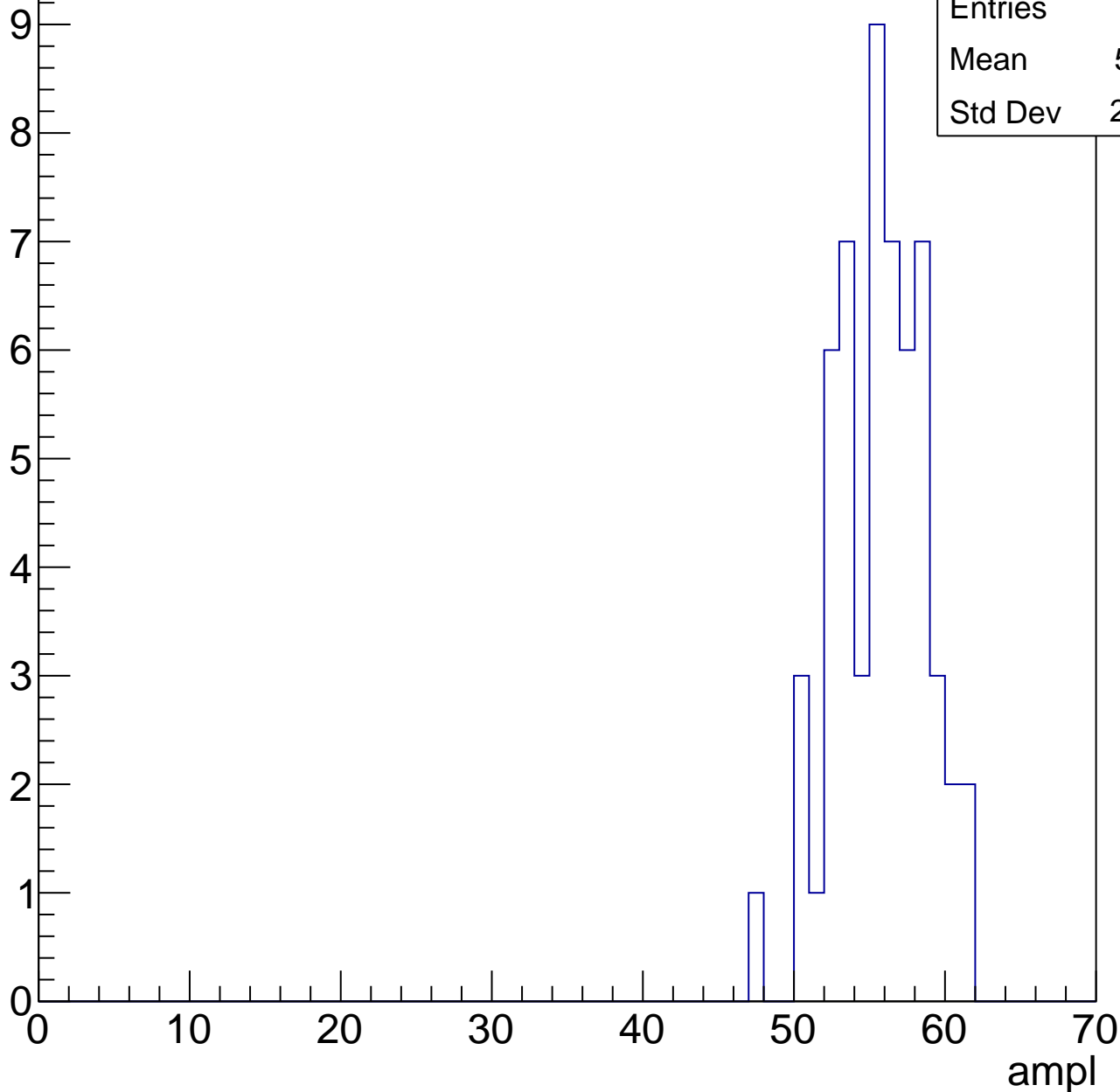
Entries	49
Mean	50.29
Std Dev	2.843



# B1L100S, U2-ch41, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



# B1L100S, U2-ch41, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	49
Mean	59.08
Std Dev	8.771

ampl

0 10 20 30 40 50 60 70

0

1

2

3

4

5

6

7

8

9

# B1L100S, U2-ch41, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry





# B1L100S, U2-ch41, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L100S, U2-ch42, adc0

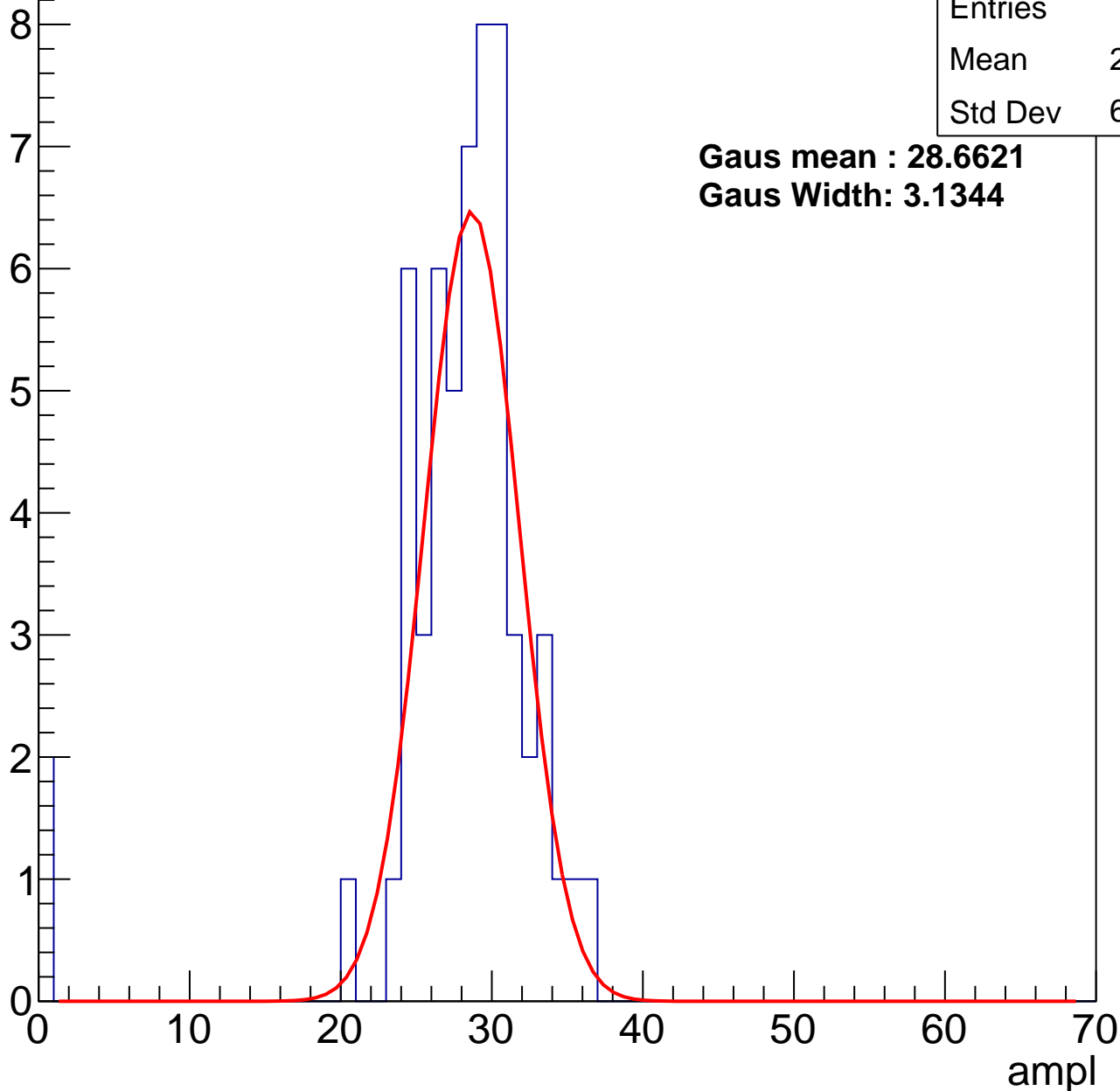
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	58
Mean	27.28
Std Dev	6.019

**Gaus mean : 28.6621**

**Gaus Width: 3.1344**



# B1L100S, U2-ch42, adc1

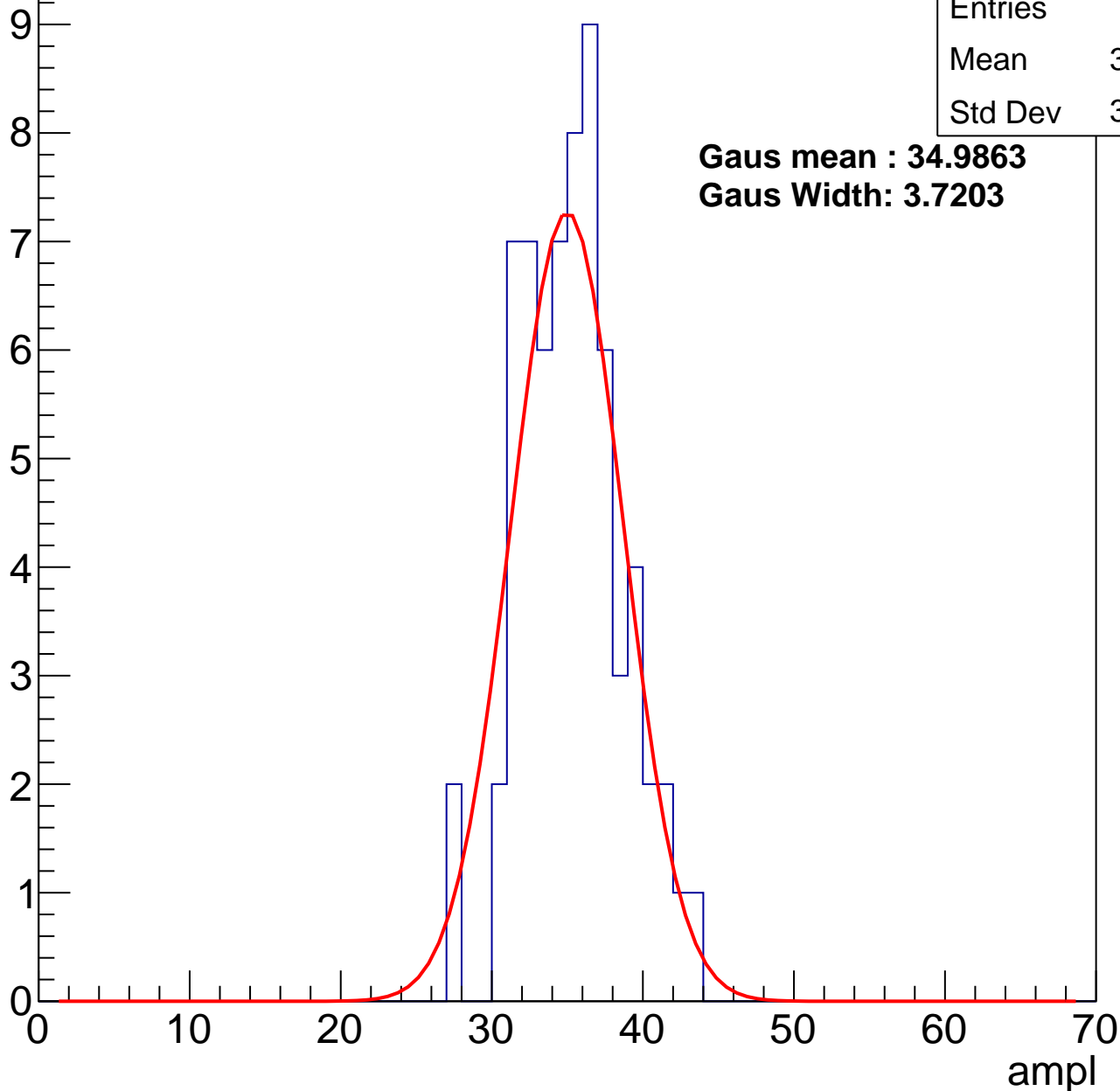
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	67
Mean	34.84
Std Dev	3.326

**Gaus mean : 34.9863**

**Gaus Width: 3.7203**



# B1L100S, U2-ch42, adc2

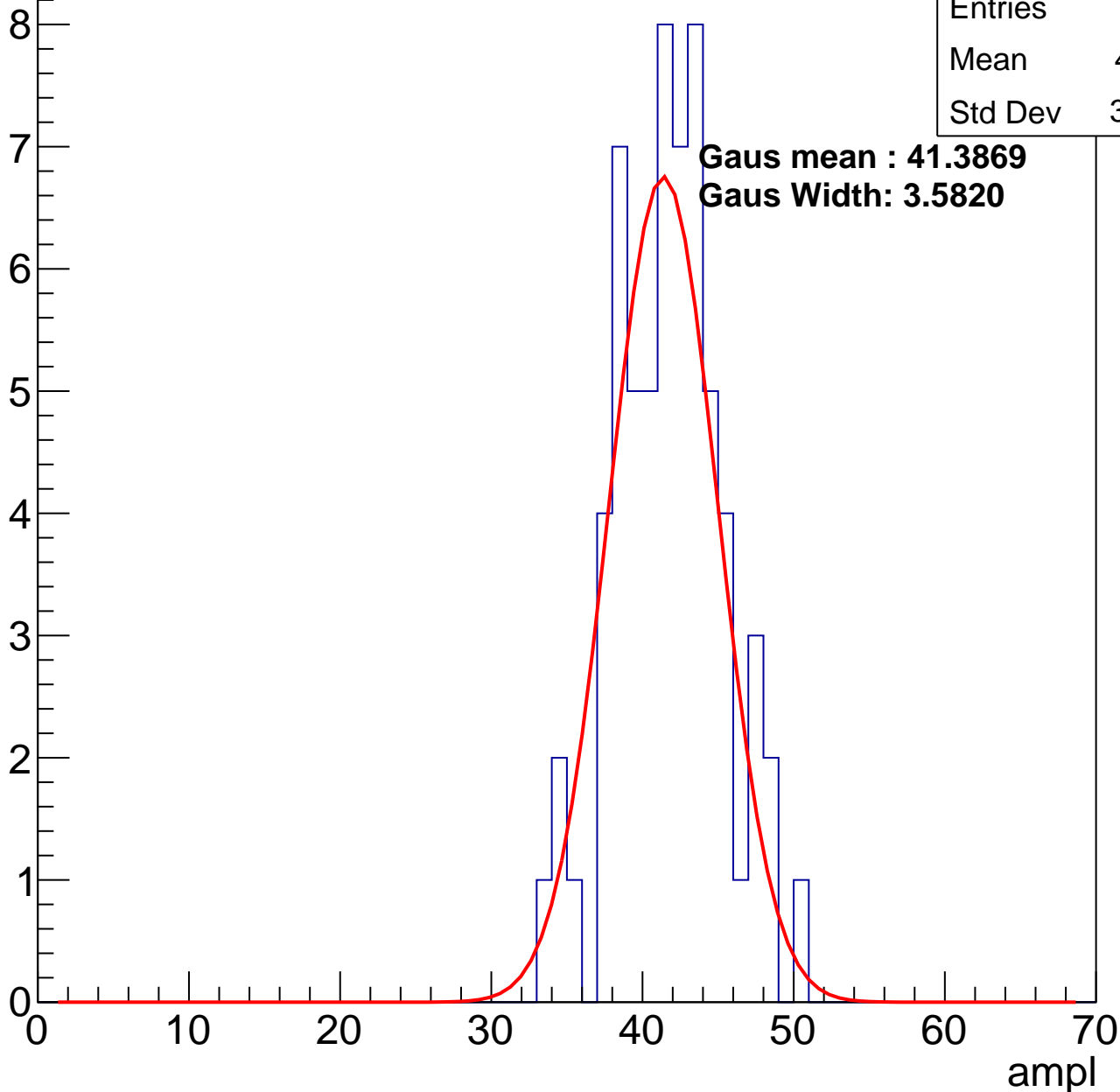
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	64
Mean	41.31
Std Dev	3.544

**Gaus mean : 41.3869**

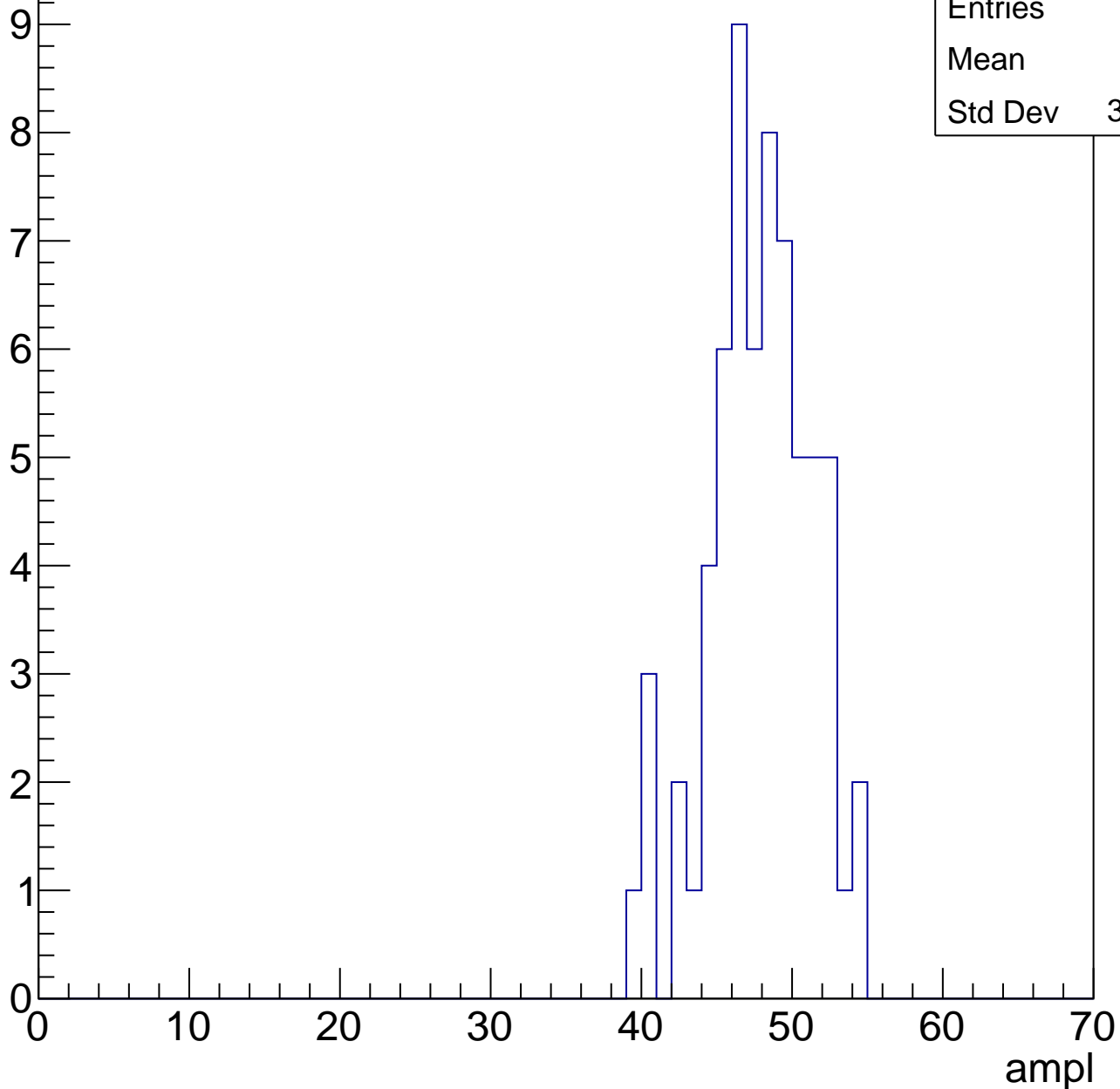
**Gaus Width: 3.5820**



# B1L100S, U2-ch42, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



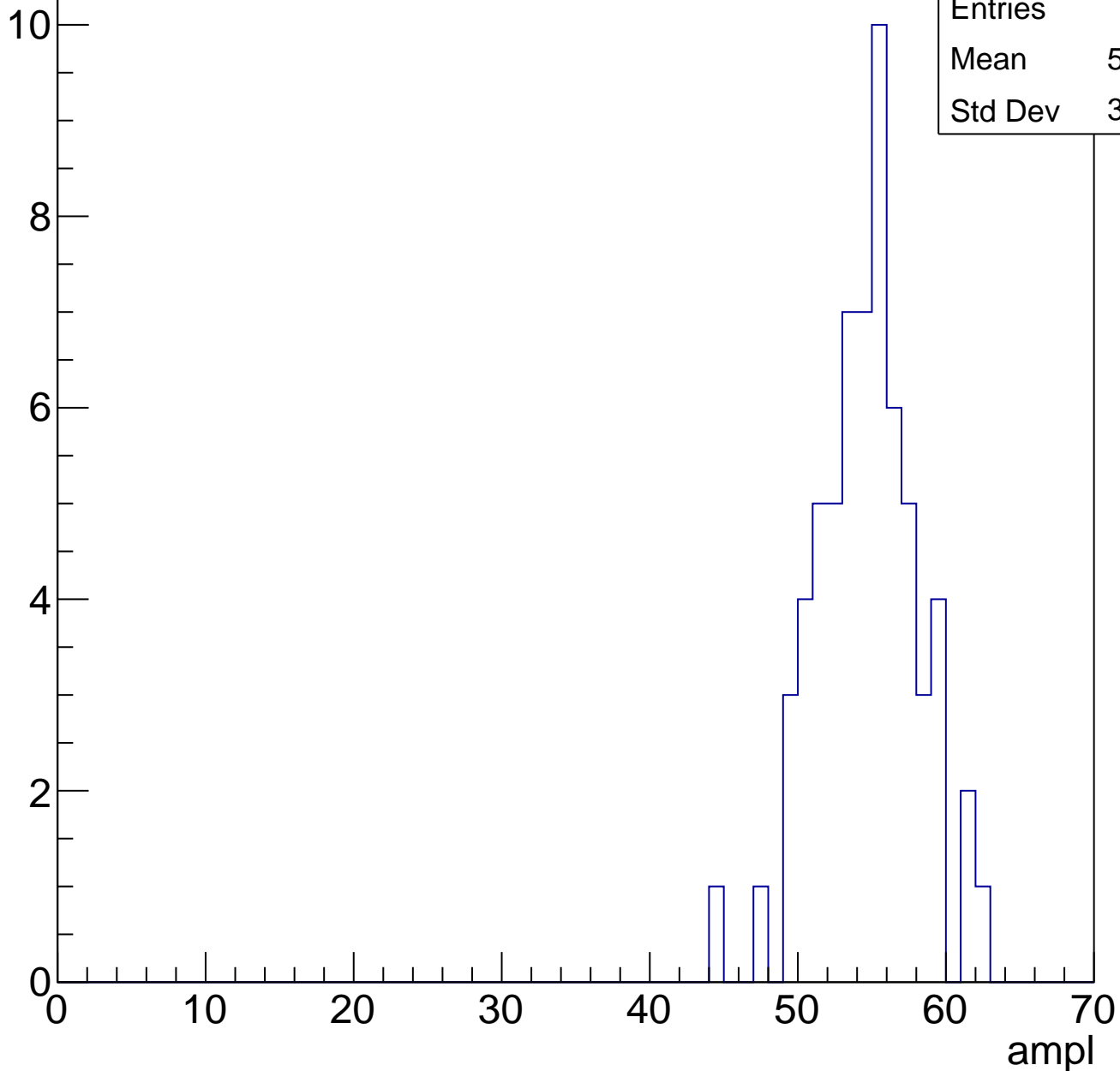
Entries	65
Mean	47.4
Std Dev	3.409

# B1L100S, U2-ch42, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	64
Mean	54.17
Std Dev	3.417

Entry



# B1L100S, U2-ch42, adc5

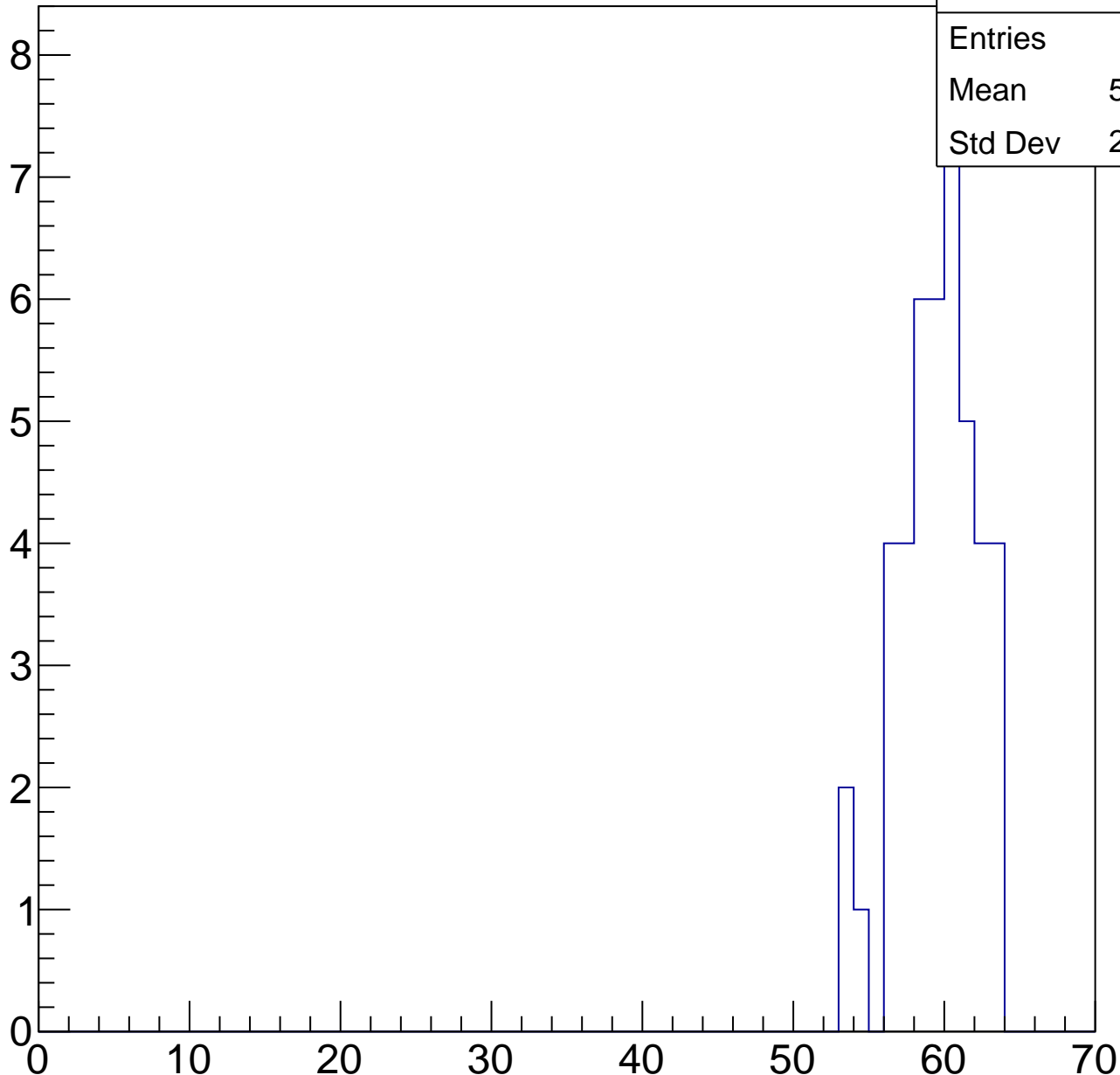
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	44
Mean	59.07
Std Dev	2.535

ampl

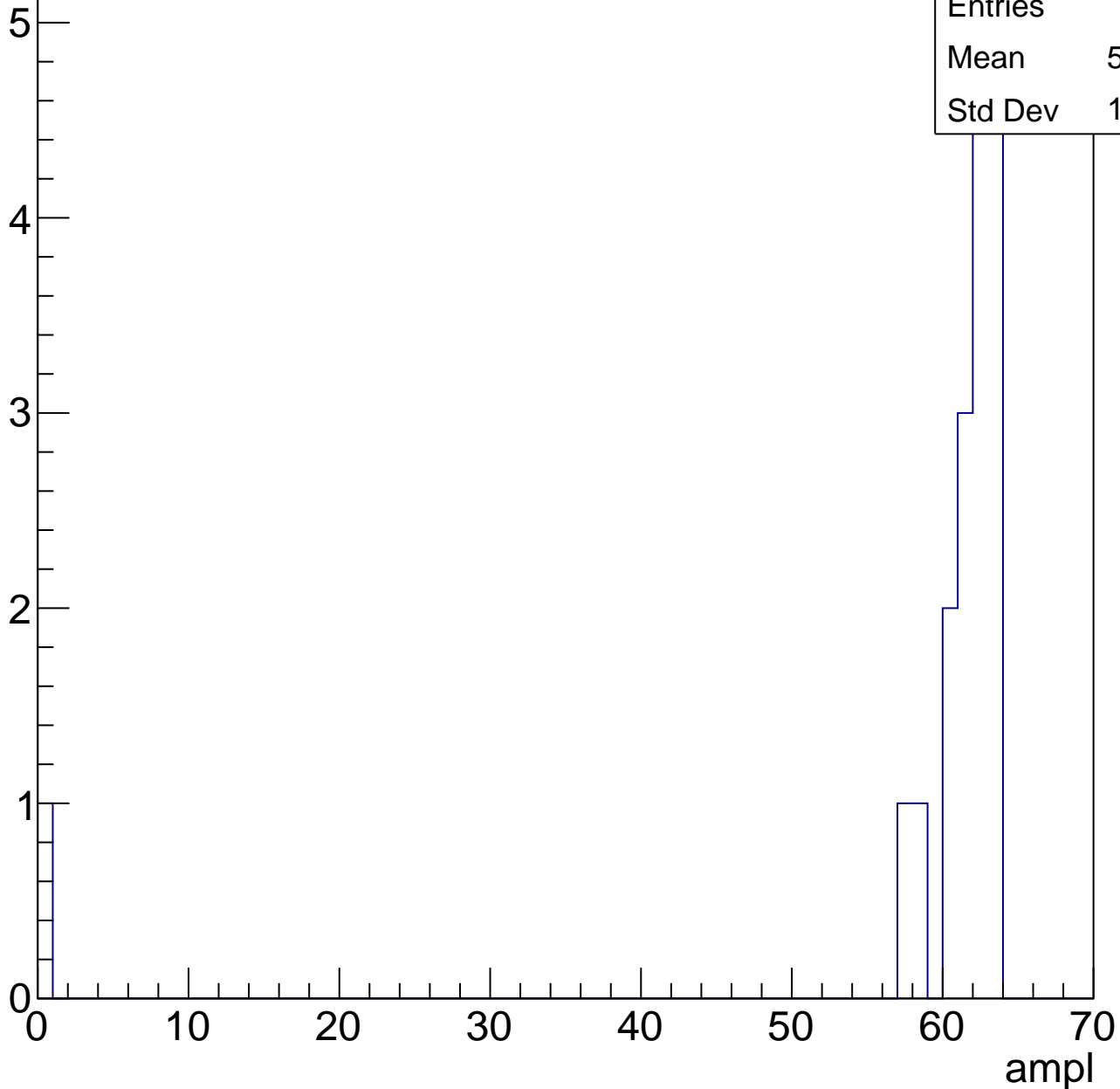


# B1L100S, U2-ch42, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	18
Mean	57.94
Std Dev	14.15





# B1L100S, U2-ch42, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



# B1L100S, U2-ch43, adc0

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	78
Mean	30.63
Std Dev	4.117

**Gaus mean : 31.1246**

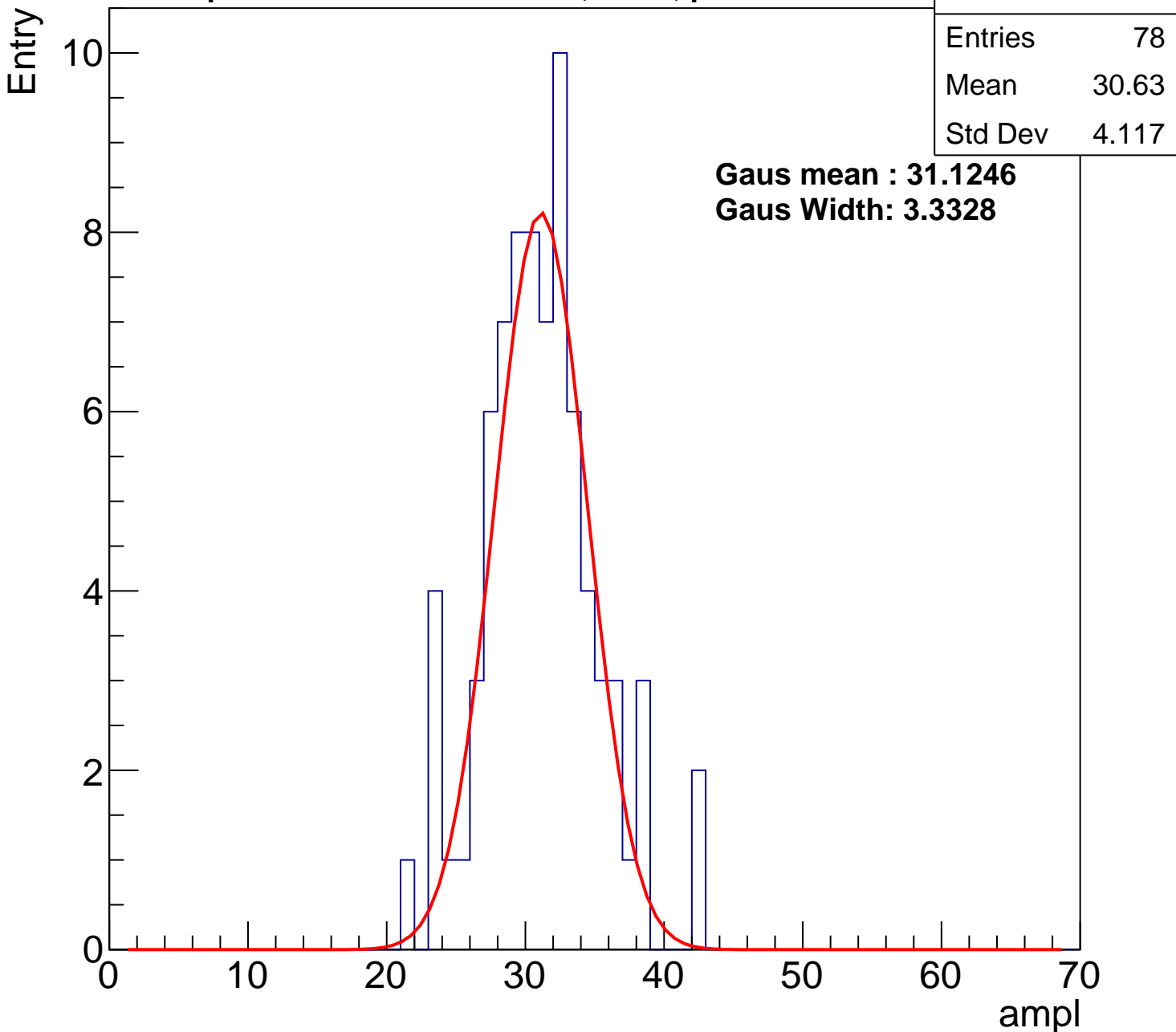
**Gaus Width: 3.3328**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L100S, U2-ch43, adc1

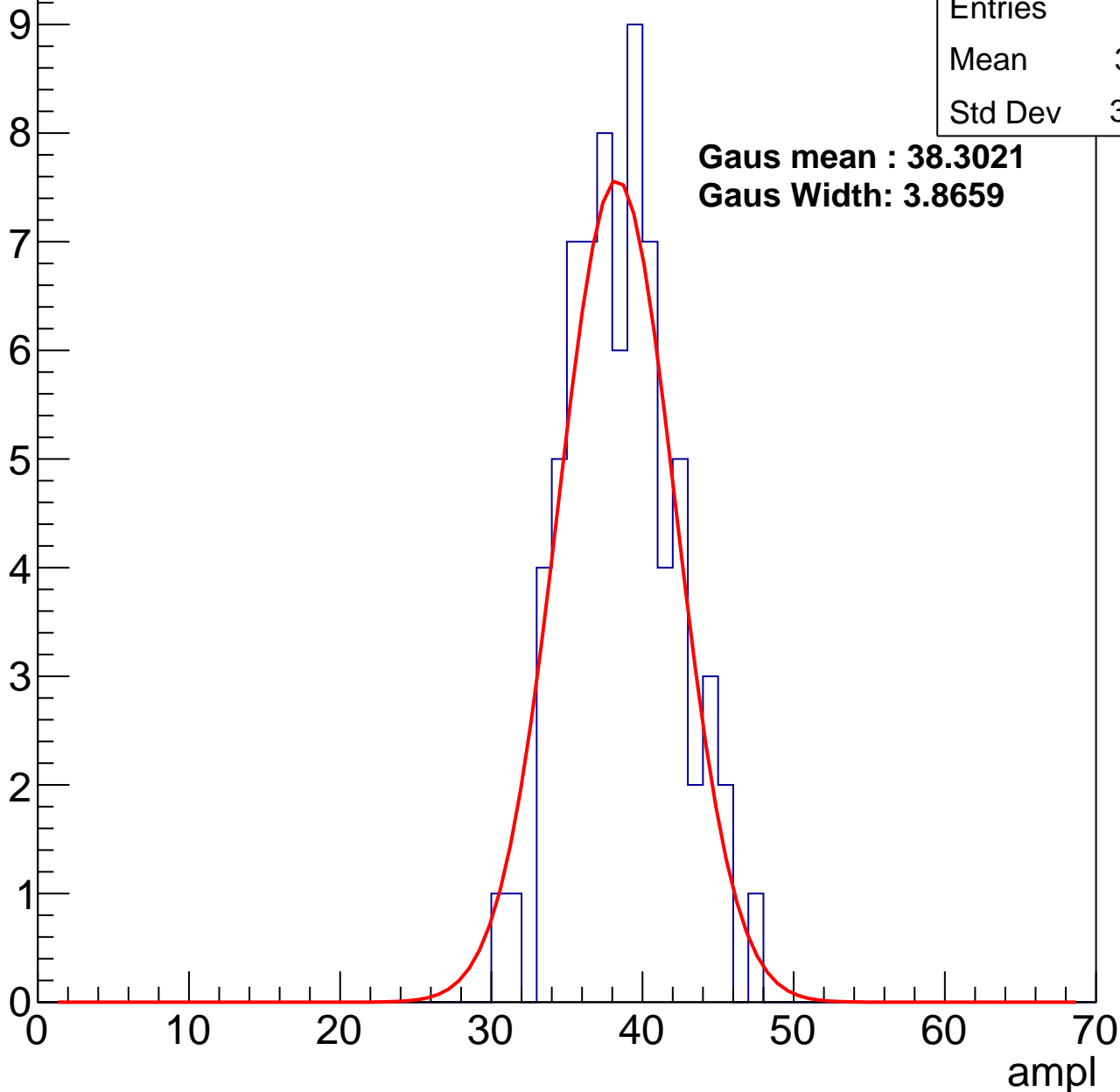
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	72
Mean	38.11
Std Dev	3.498

**Gaus mean : 38.3021**

**Gaus Width: 3.8659**



# B1L100S, U2-ch43, adc2

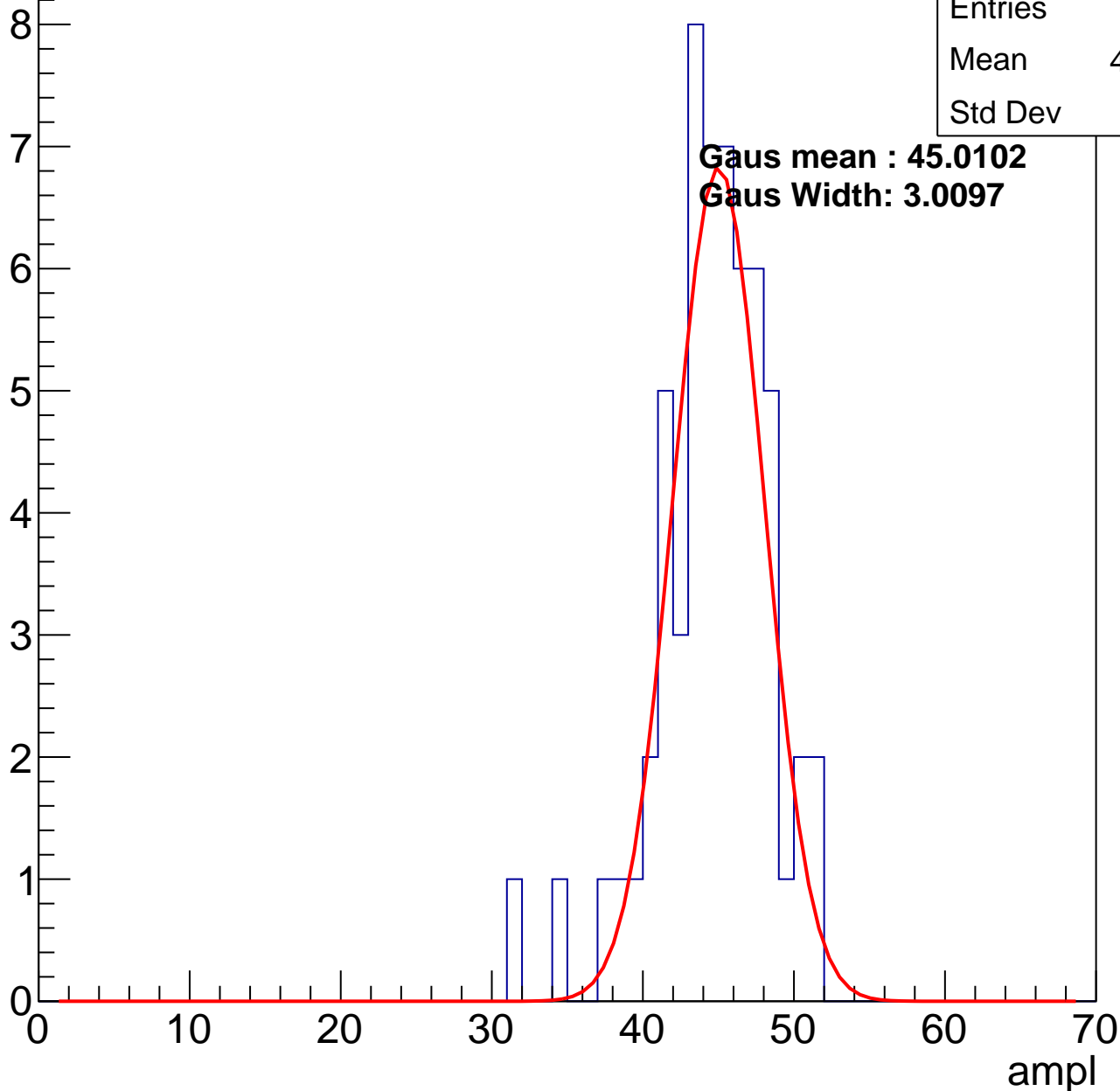
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	59
Mean	44.17
Std Dev	3.76

Gaus mean : 45.0102

Gaus Width: 3.0097

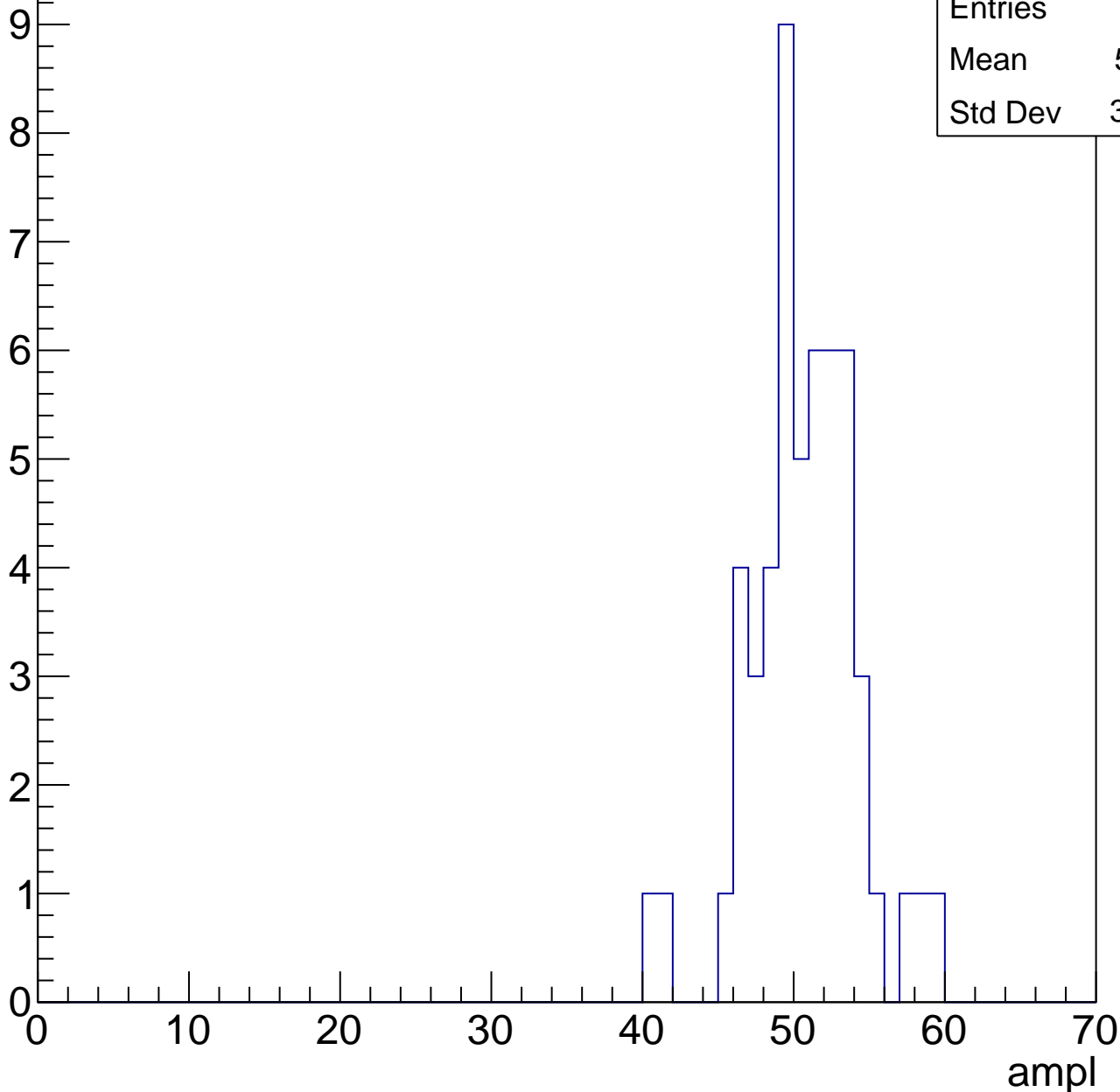


# B1L100S, U2-ch43, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

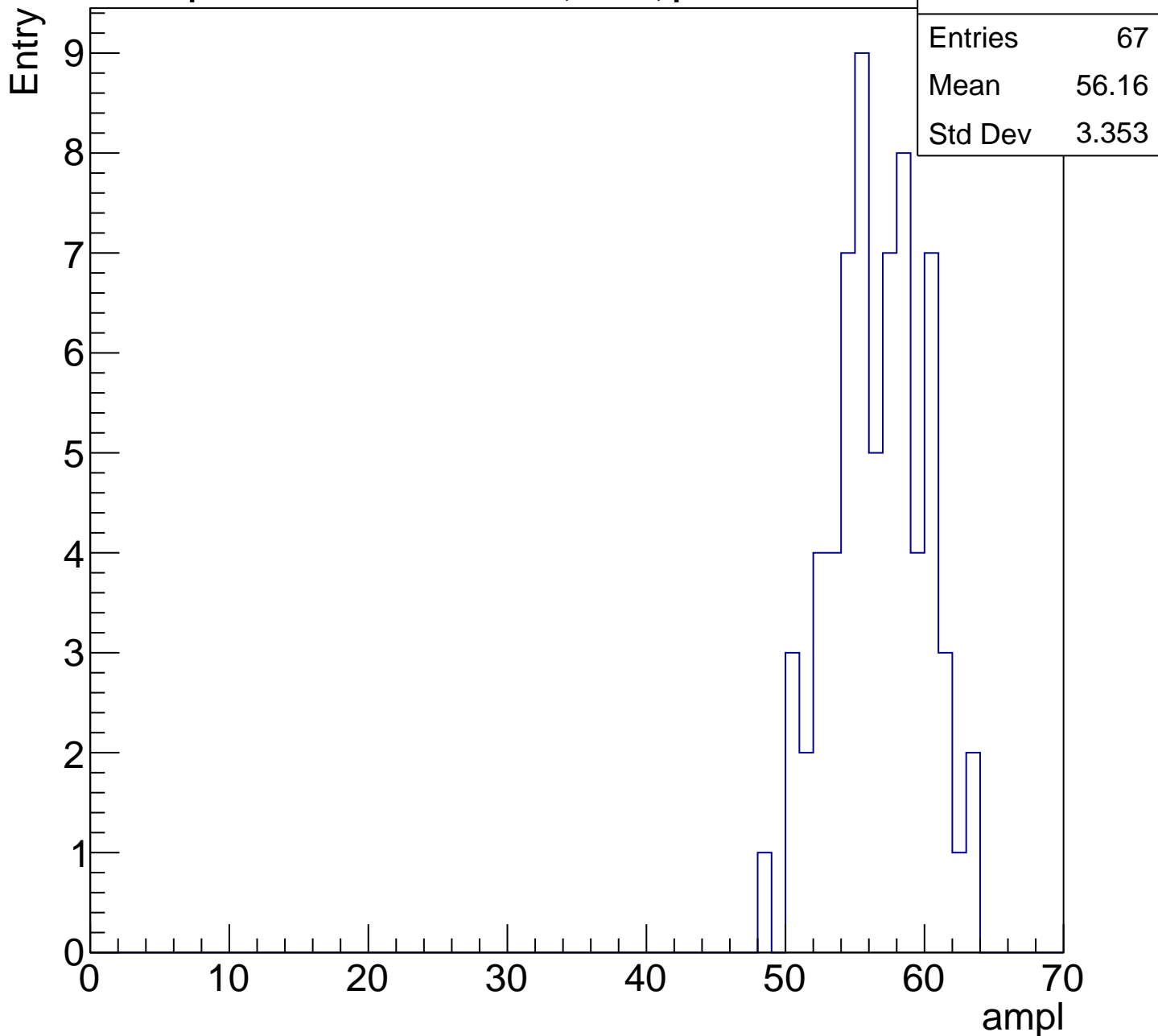
Entry

Entries	53
Mean	50.21
Std Dev	3.557



# B1L100S, U2-ch43, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

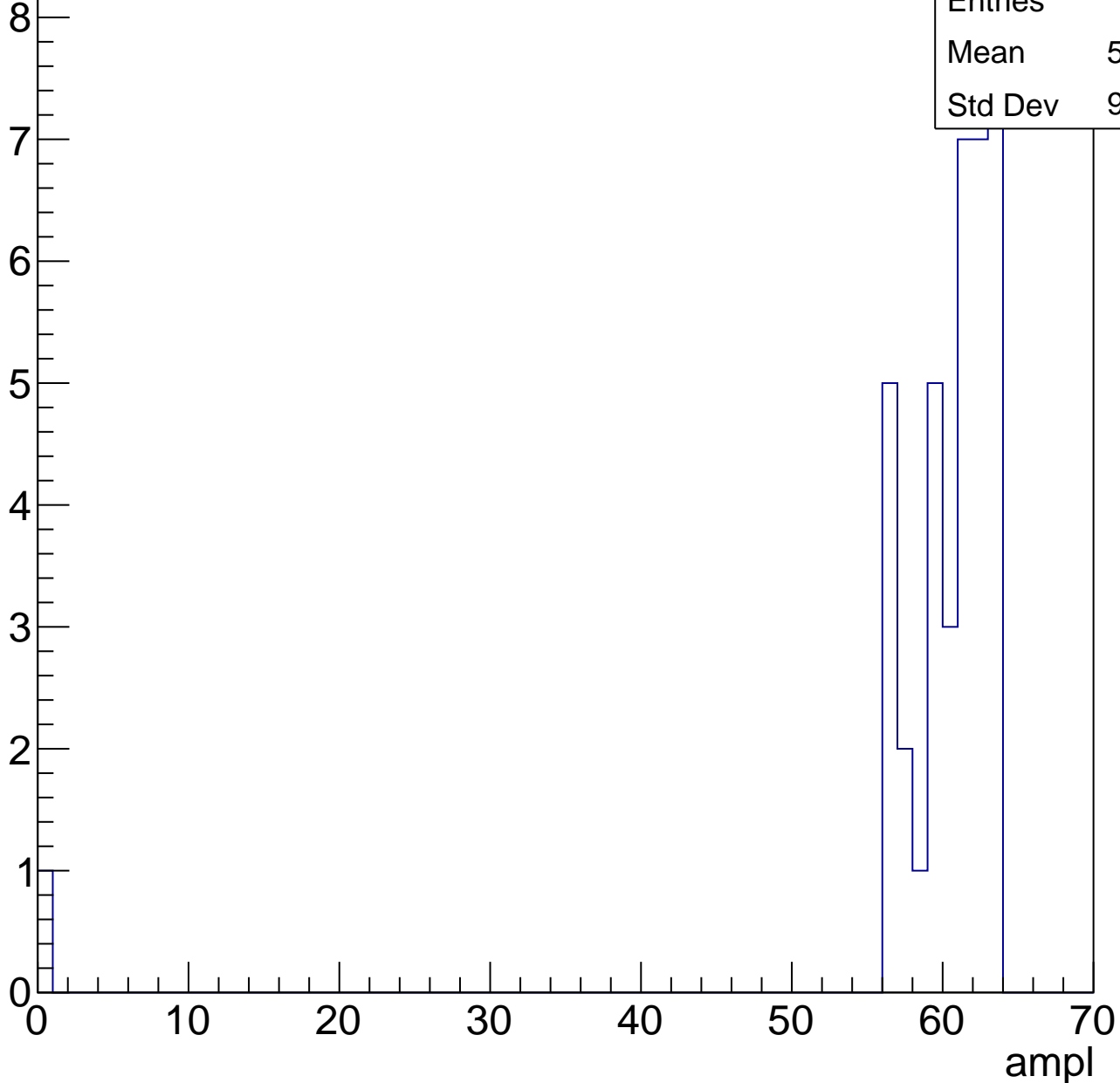


# B1L100S, U2-ch43, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	39
Mean	58.77
Std Dev	9.812



# B1L100S, U2-ch43, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry





# B1L100S, U2-ch43, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L100S, U2-ch44, adc0

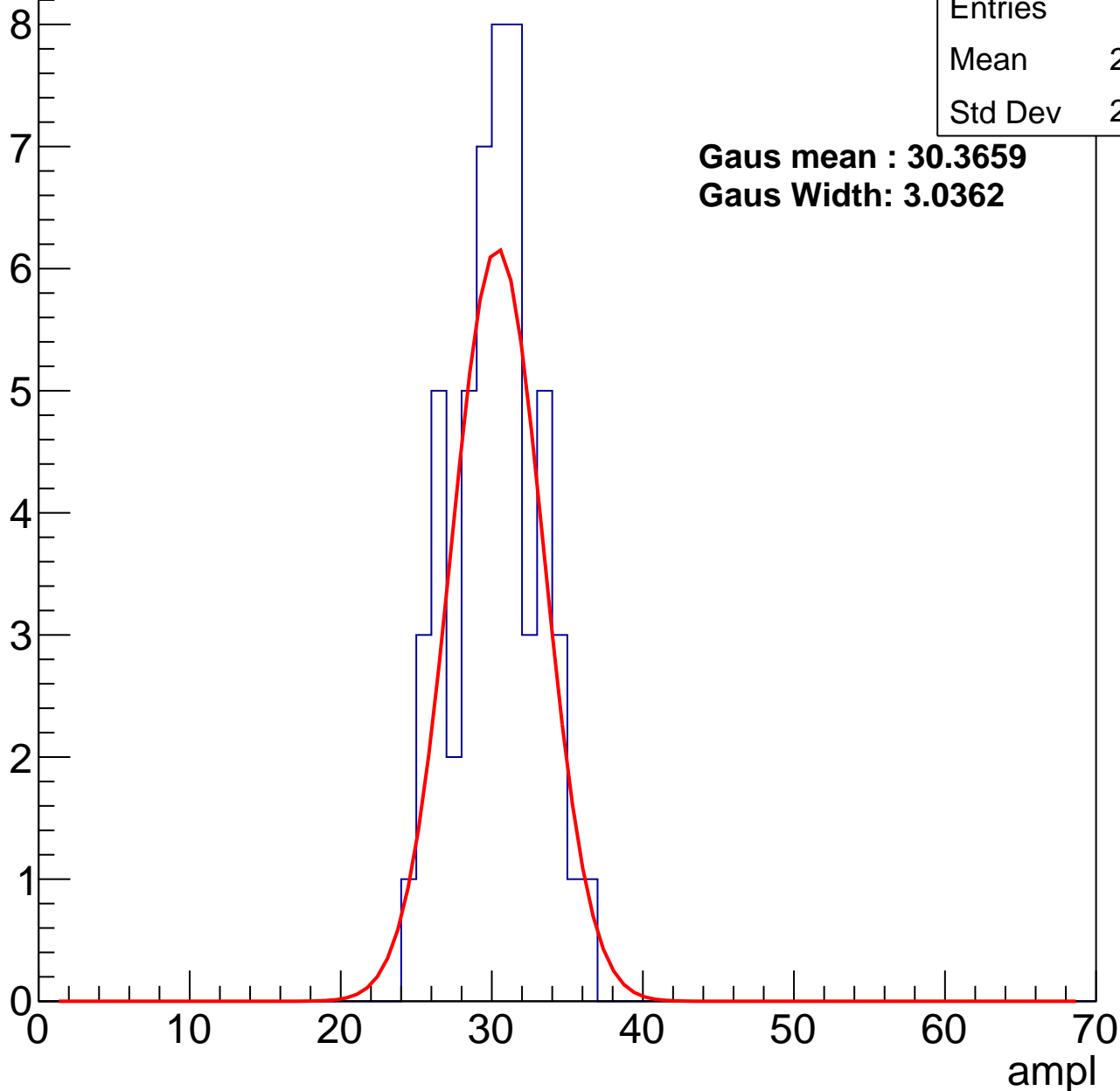
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	52
Mean	29.77
Std Dev	2.798

**Gaus mean : 30.3659**

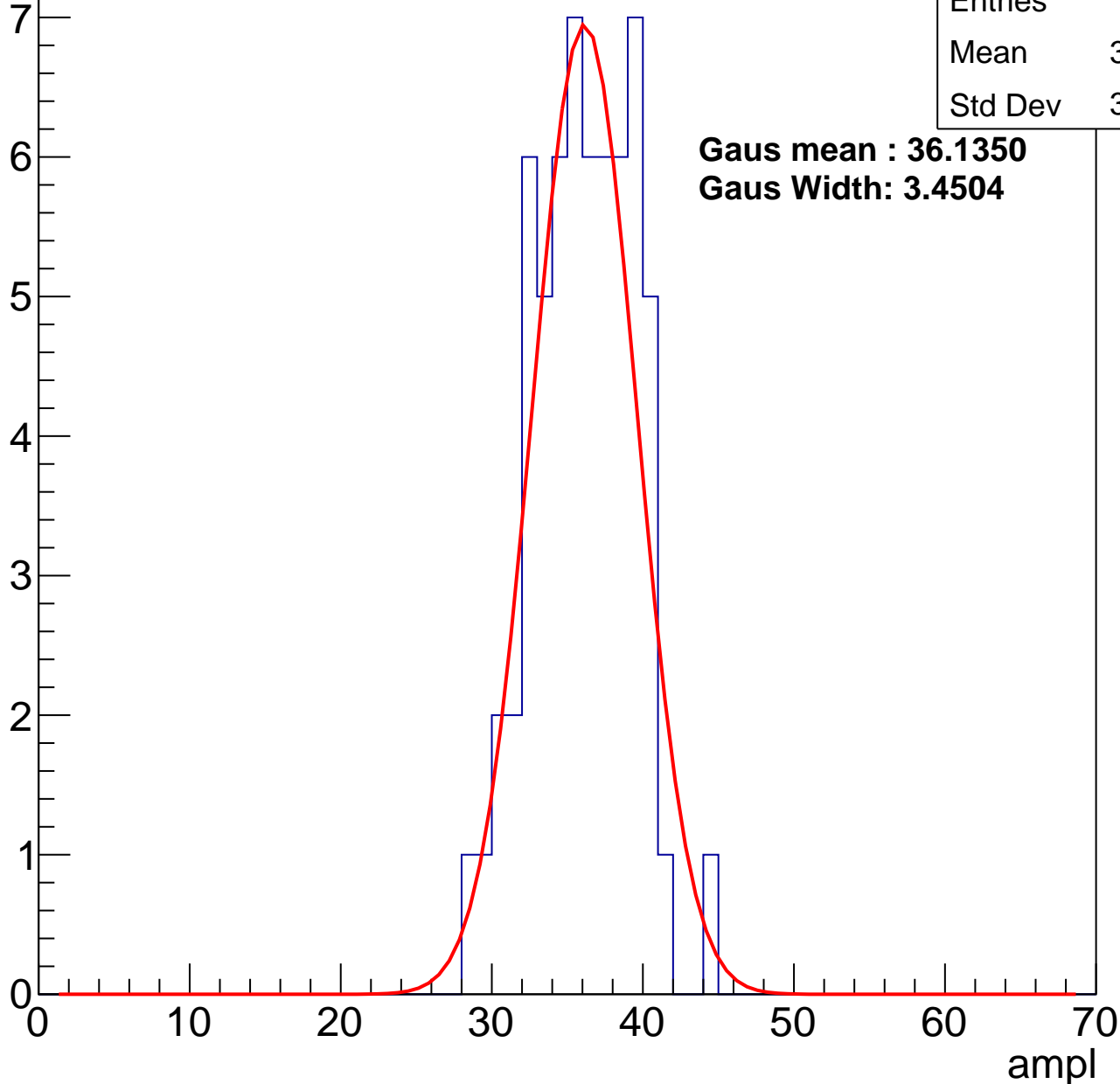
**Gaus Width: 3.0362**



# B1L100S, U2-ch44, adc1

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



# B1L100S, U2-ch44, adc2

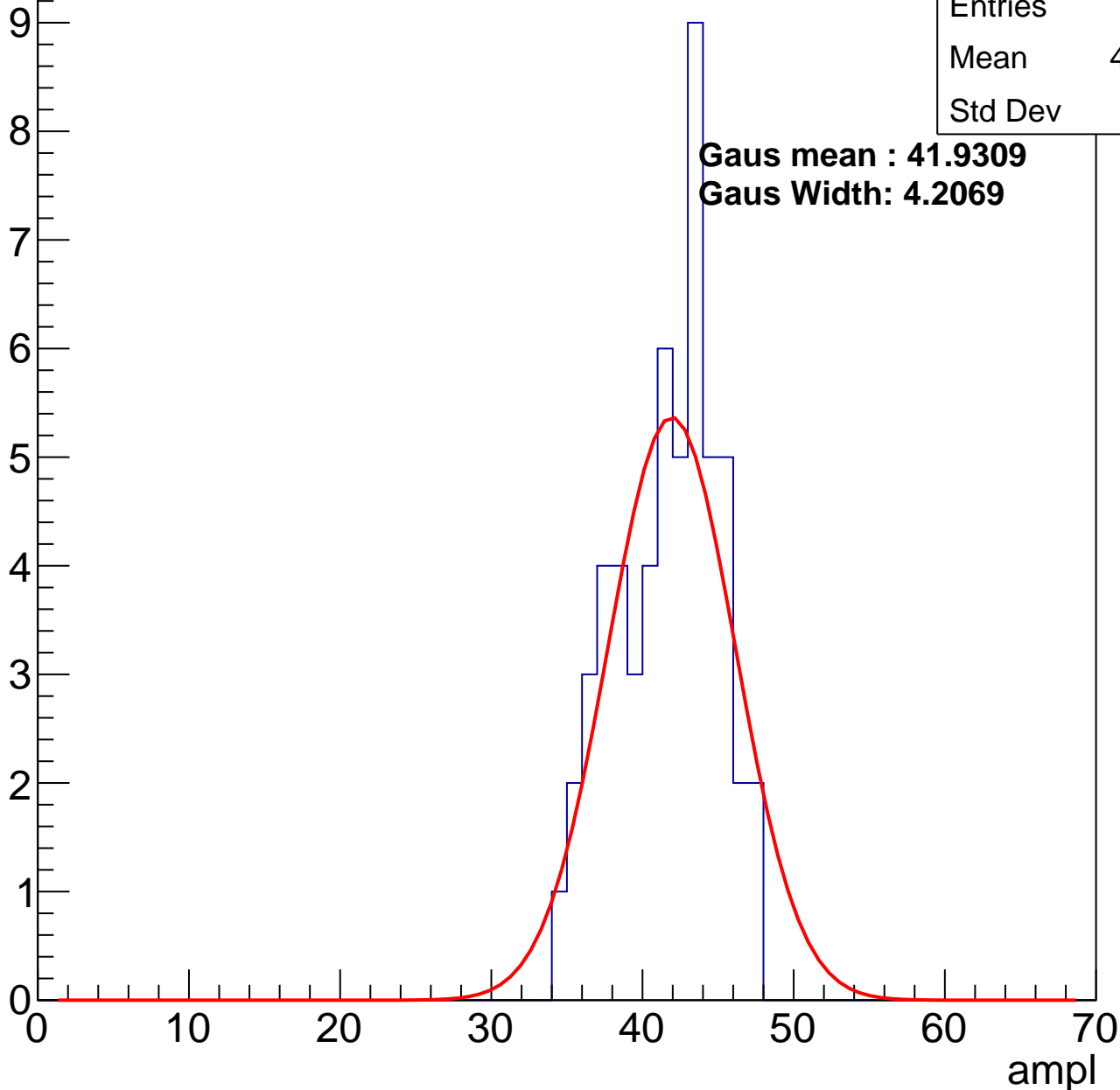
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	55
Mean	41.15
Std Dev	3.3

**Gaus mean : 41.9309**

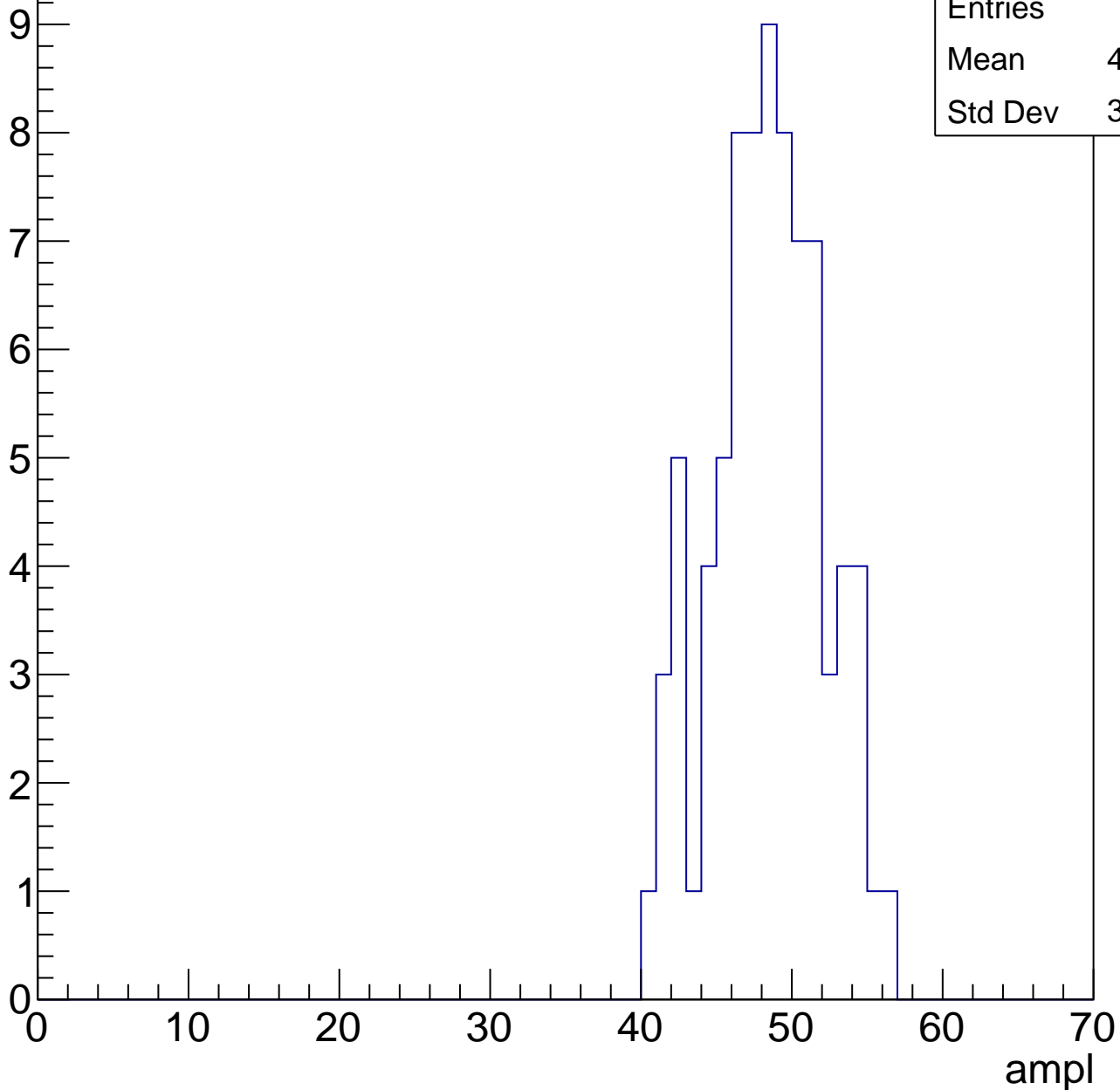
**Gaus Width: 4.2069**



# B1L100S, U2-ch44, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

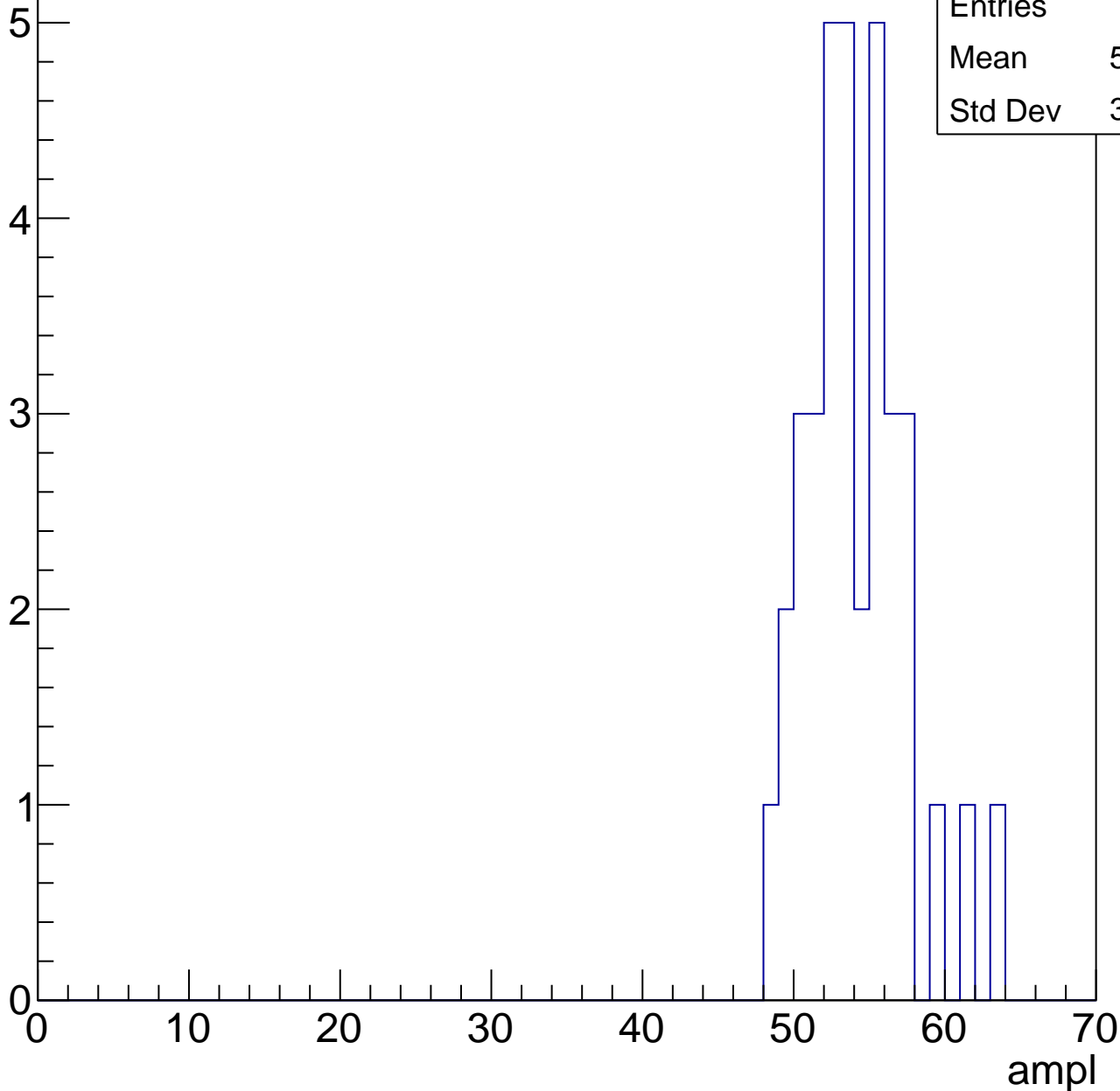


# B1L100S, U2-ch44, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	35
Mean	53.69
Std Dev	3.302

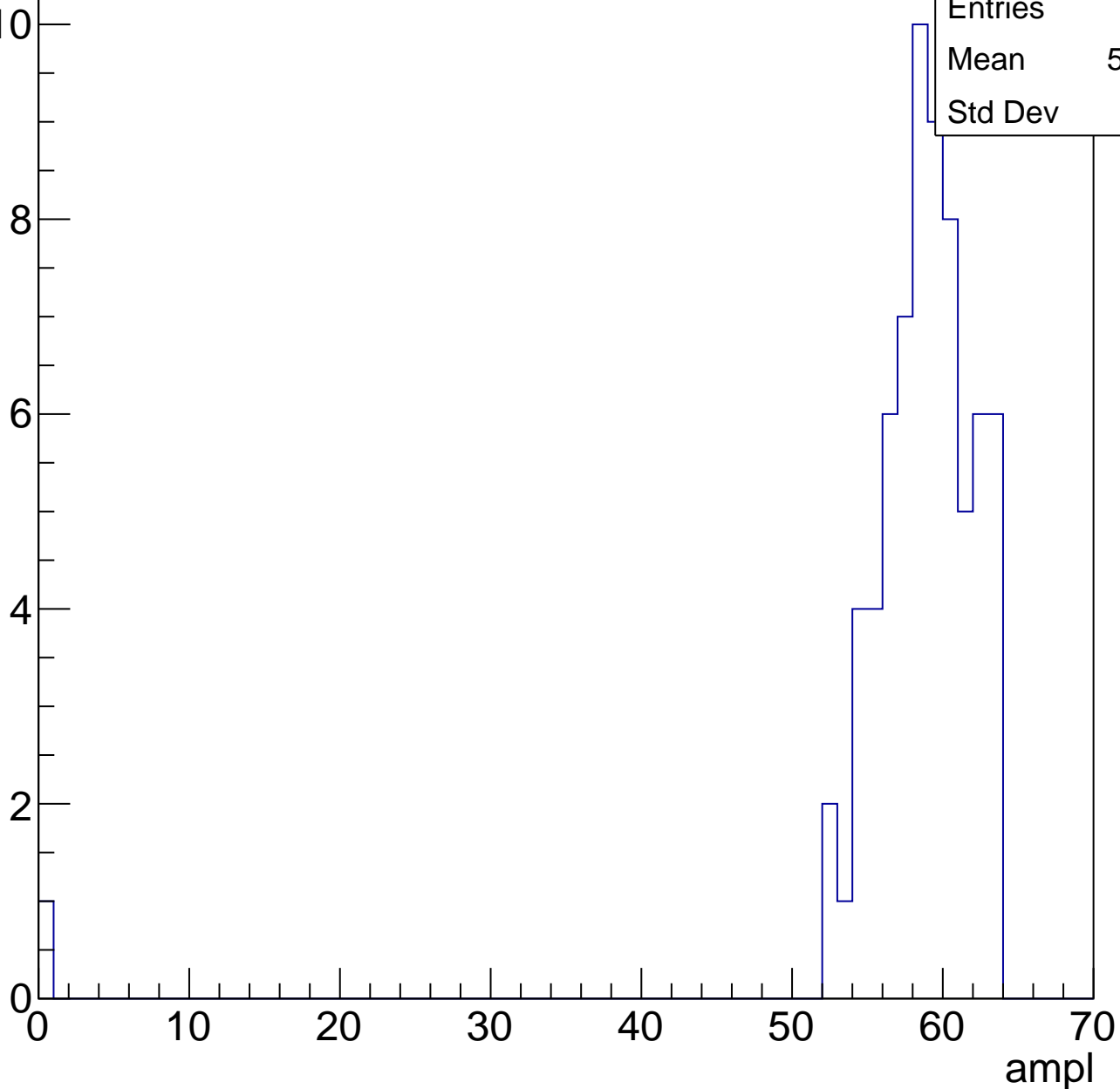


# B1L100S, U2-ch44, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

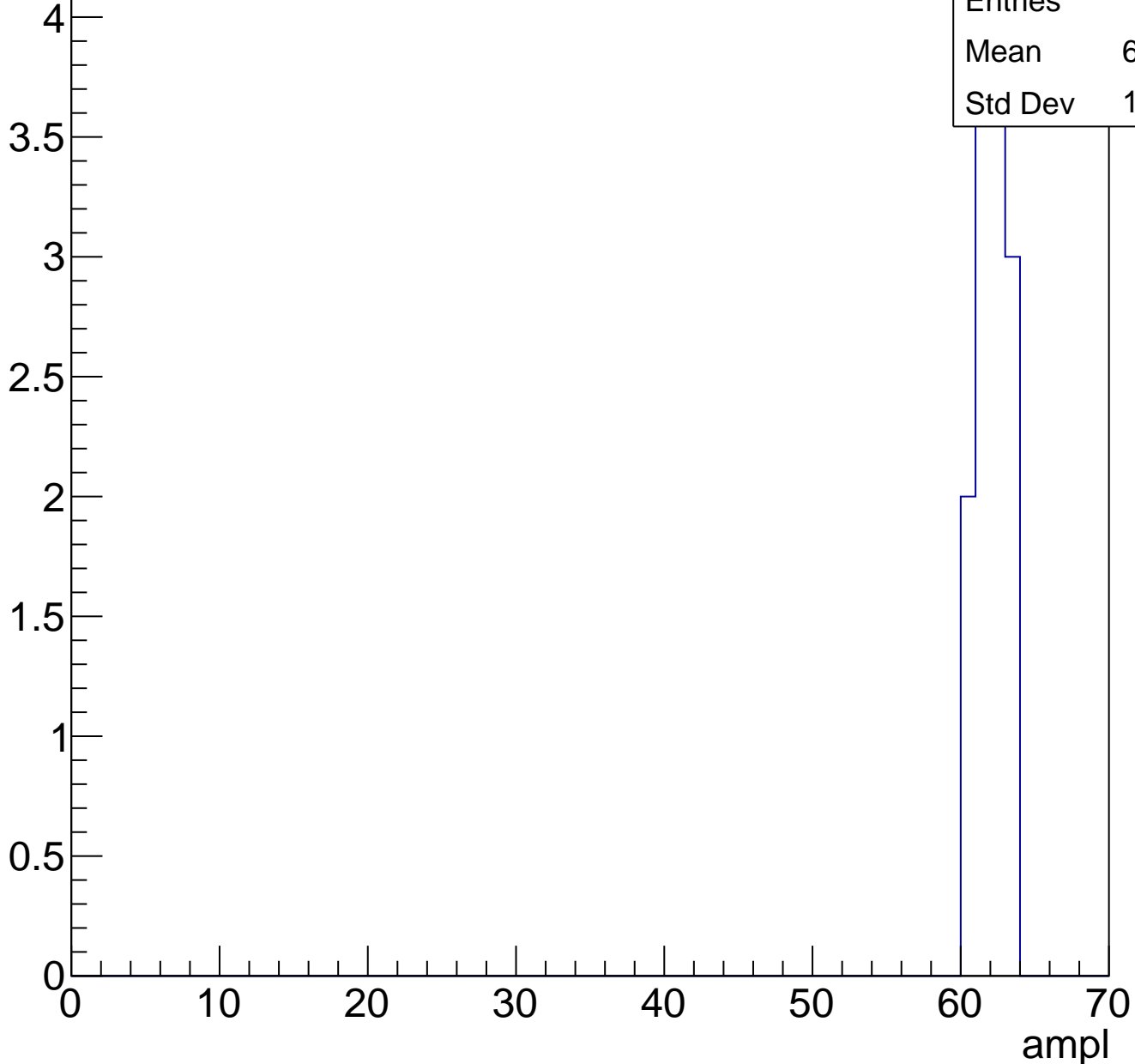
Entries	69
Mean	57.59
Std Dev	7.53



# B1L100S, U2-ch44, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	13
Mean	61.62
Std Dev	1.003



# B1L100S, U2-ch44, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L100S, U2-ch45, adc0

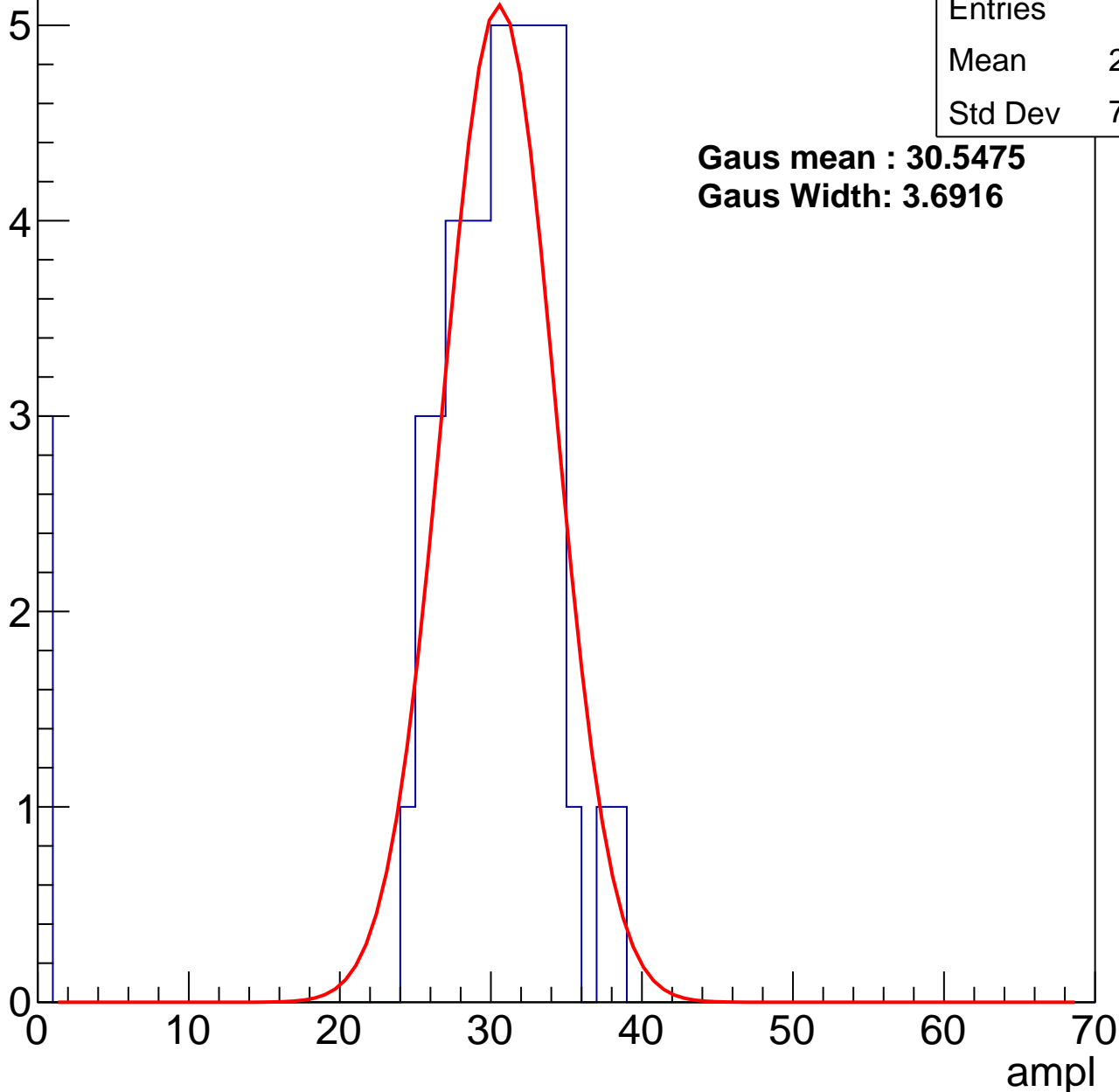
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	50
Mean	28.46
Std Dev	7.854

**Gaus mean : 30.5475**

**Gaus Width: 3.6916**



# B1L100S, U2-ch45, adc1

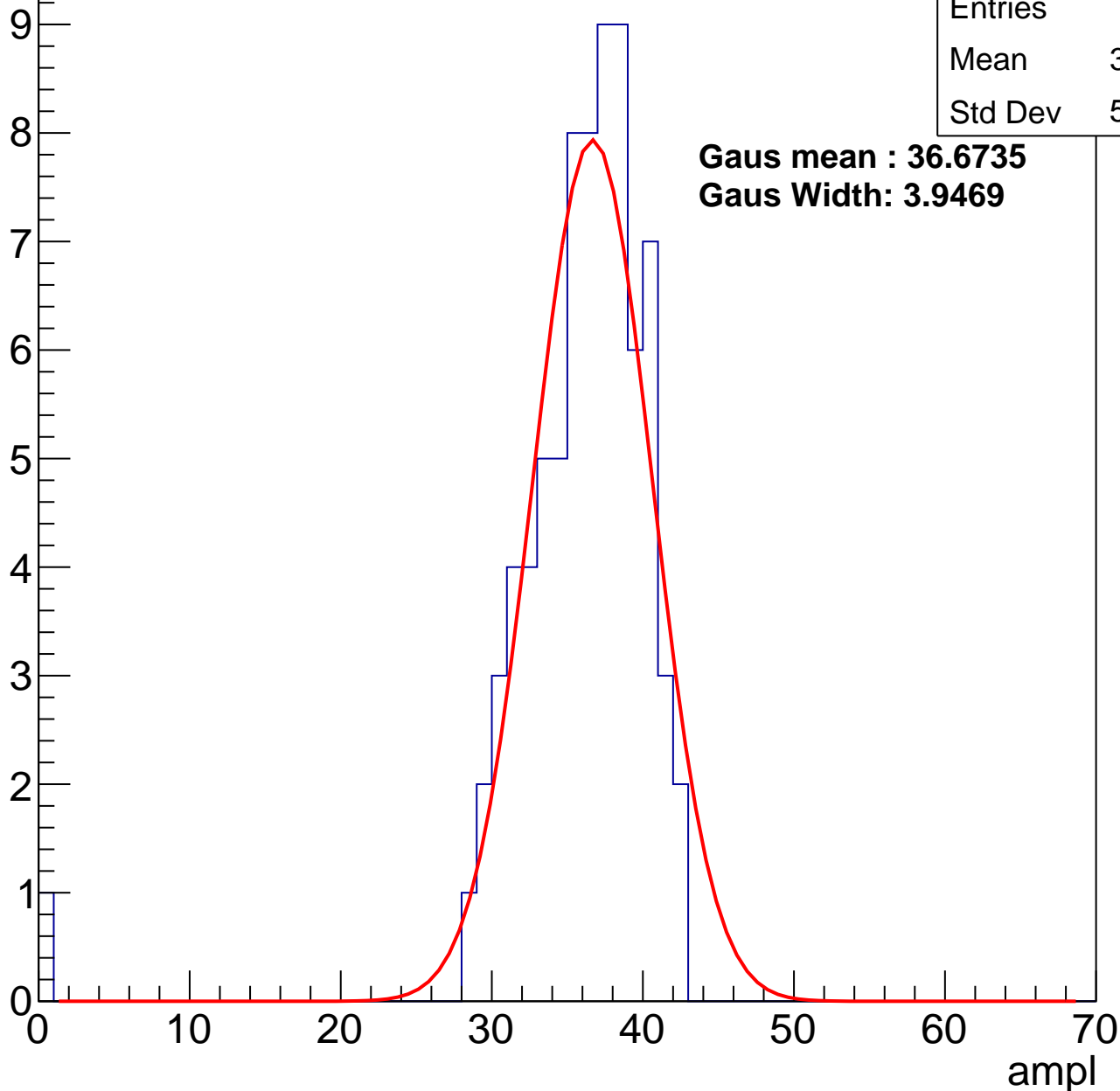
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	77
Mean	35.42
Std Dev	5.265

**Gaus mean : 36.6735**

**Gaus Width: 3.9469**



# B1L100S, U2-ch45, adc2

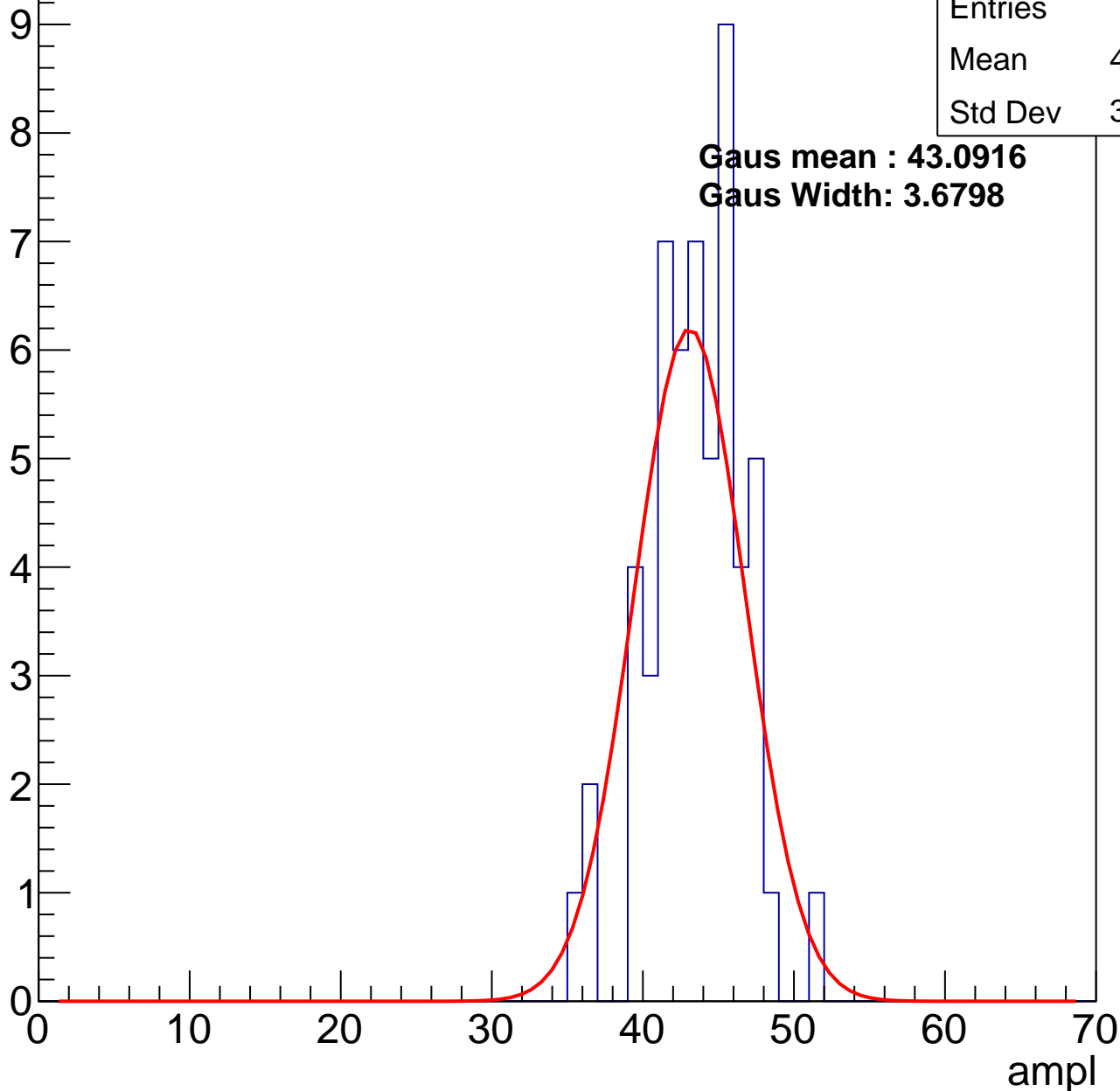
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	55
Mean	43.02
Std Dev	3.113

**Gaus mean : 43.0916**

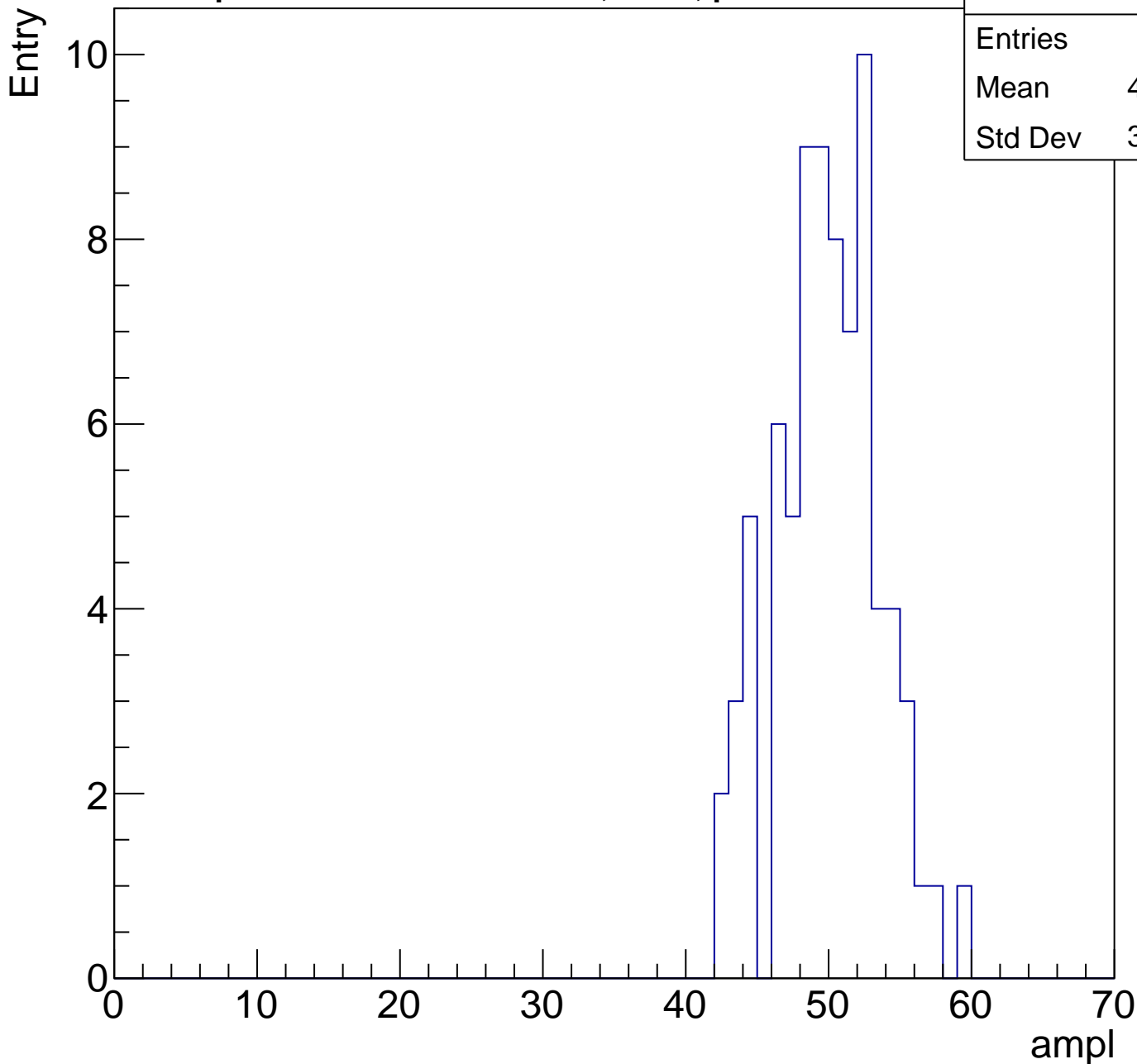
**Gaus Width: 3.6798**



# B1L100S, U2-ch45, adc3

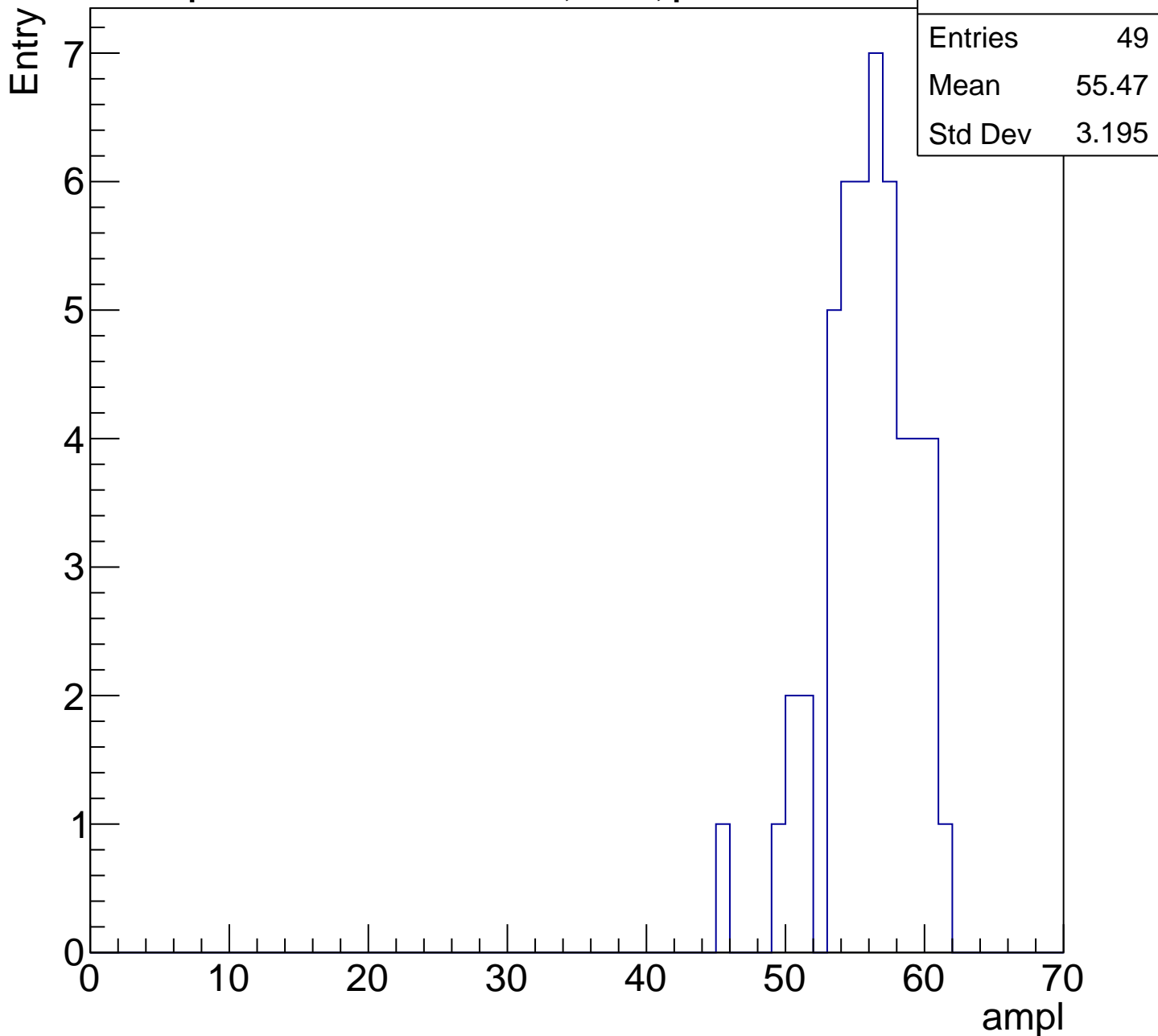
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	78
Mean	49.47
Std Dev	3.594



# B1L100S, U2-ch45, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

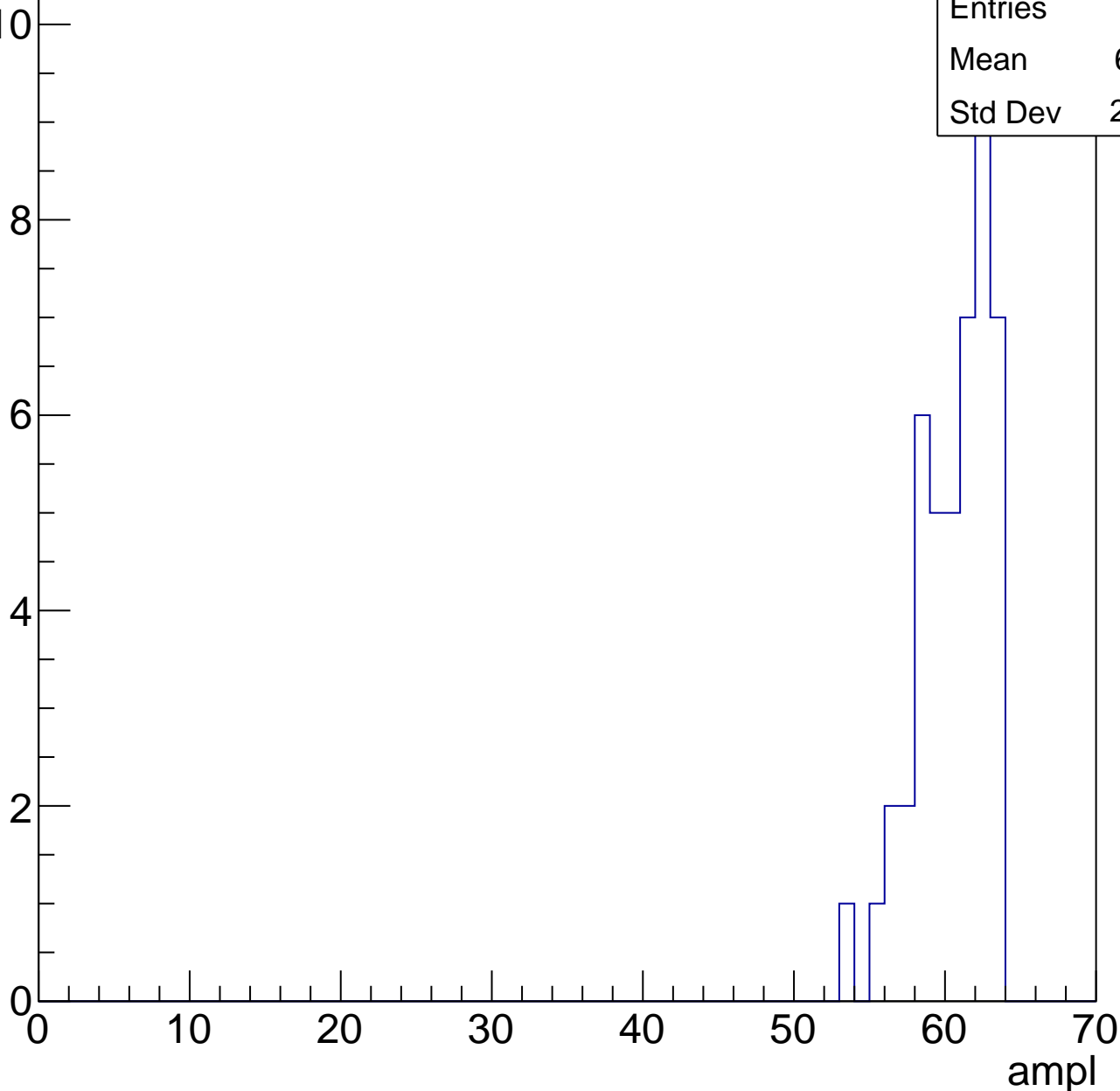


# B1L100S, U2-ch45, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

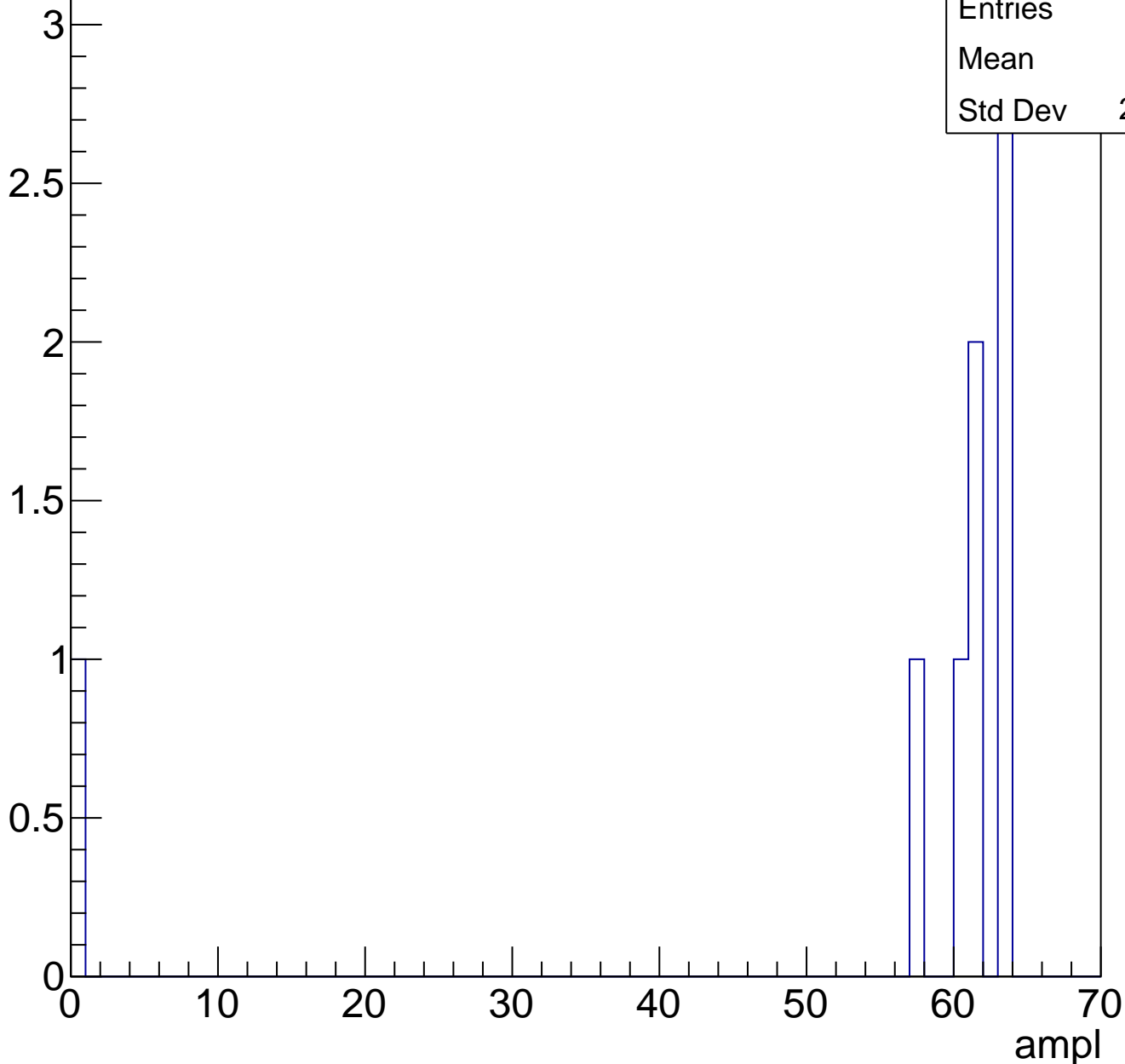
Entries	46
Mean	60.11
Std Dev	2.389



# B1L100S, U2-ch45, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry





# B1L100S, U2-ch45, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L100S, U2-ch46, adc0

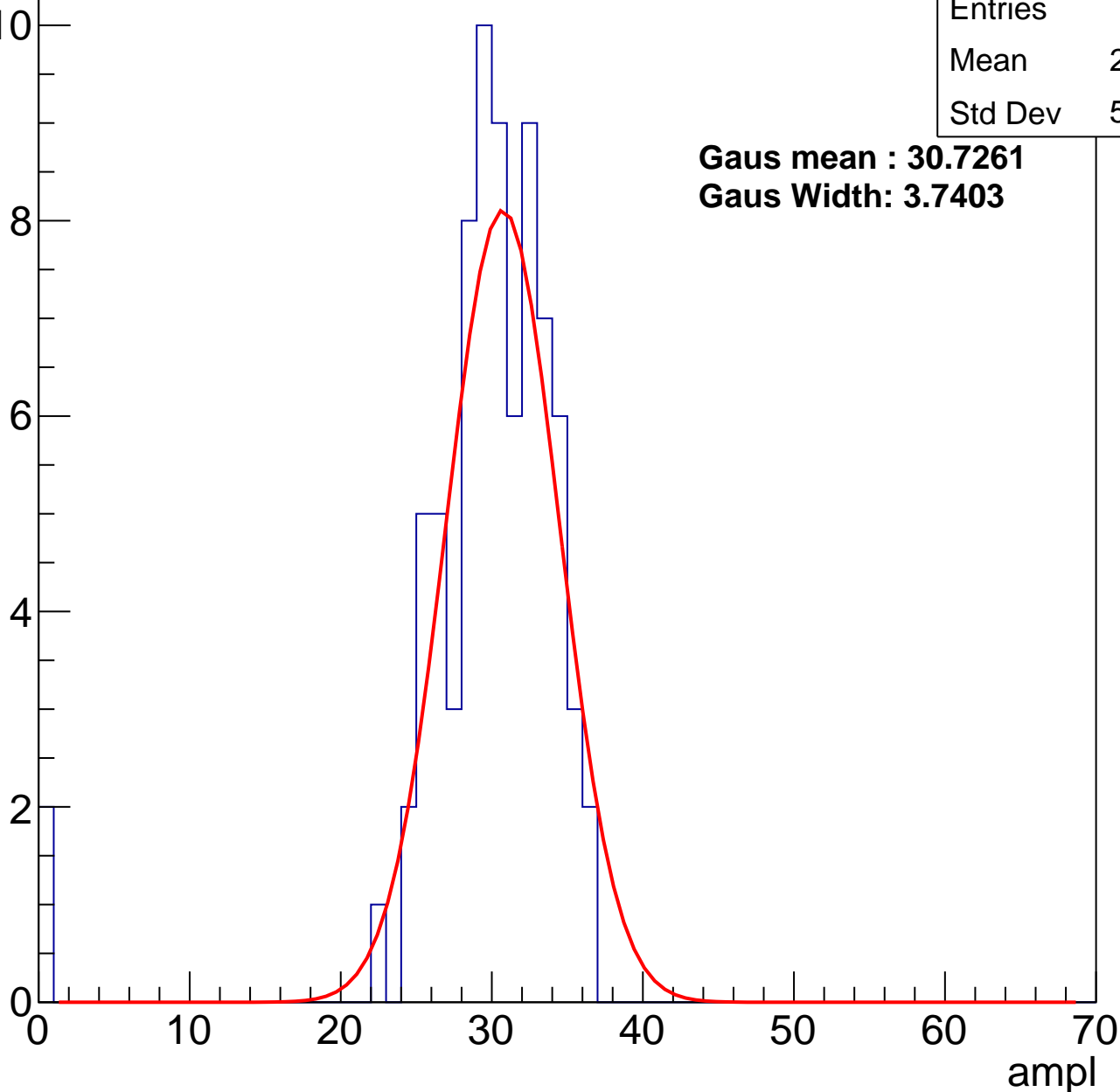
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	78
Mean	29.18
Std Dev	5.668

**Gaus mean : 30.7261**

**Gaus Width: 3.7403**



# B1L100S, U2-ch46, adc1

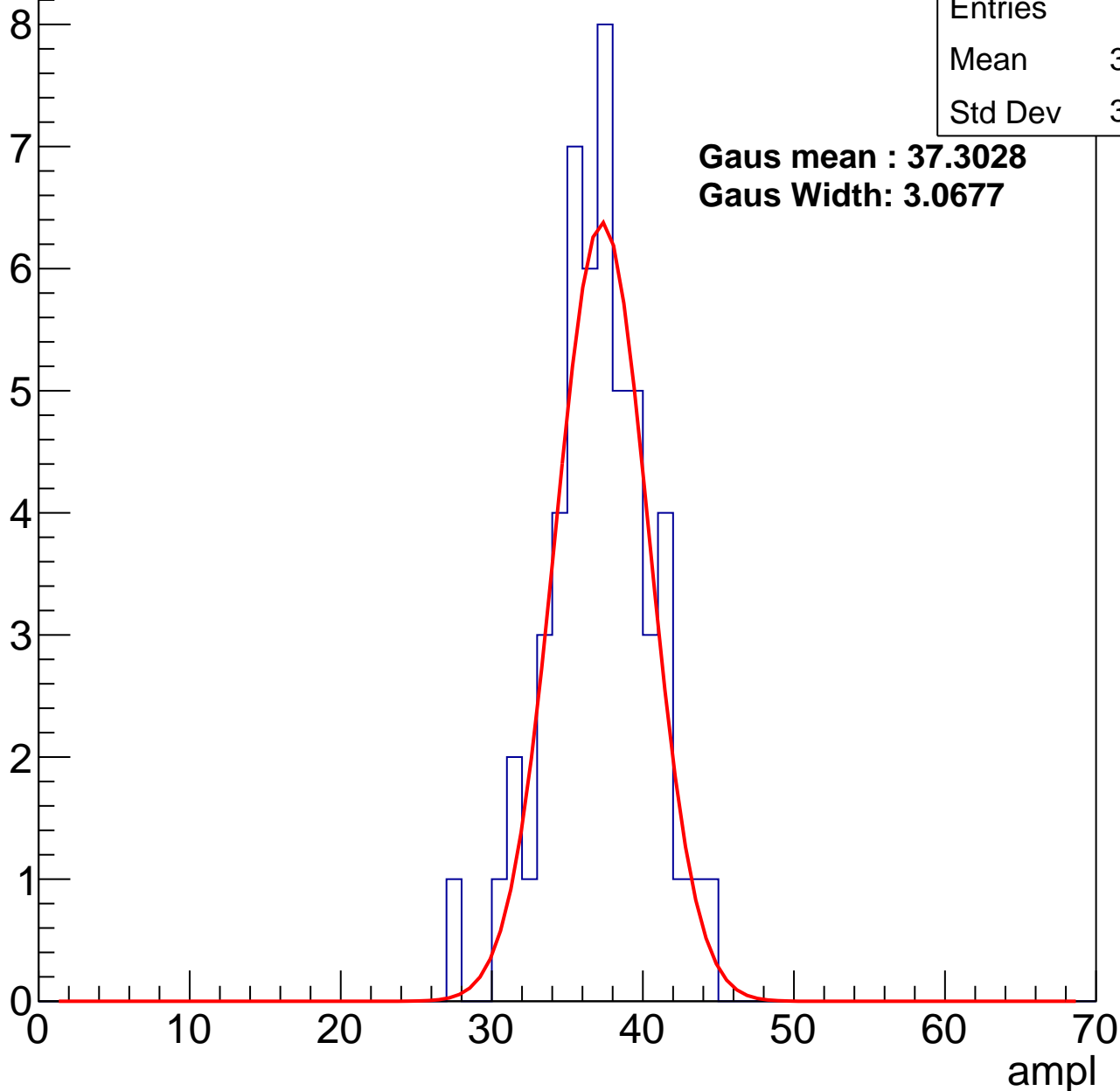
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	53
Mean	36.62
Std Dev	3.315

**Gaus mean : 37.3028**

**Gaus Width: 3.0677**



# B1L100S, U2-ch46, adc2

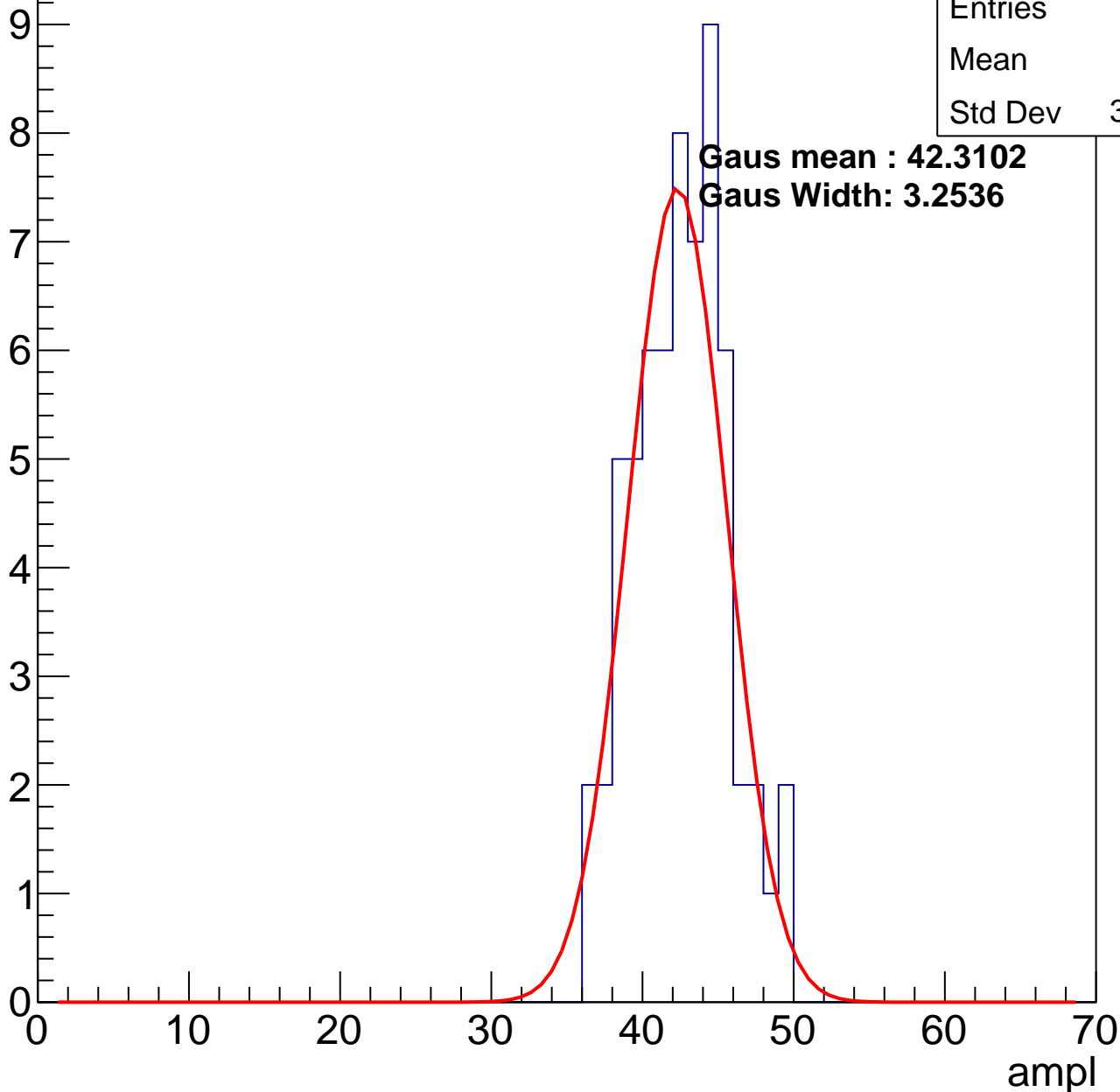
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	63
Mean	42.1
Std Dev	3.059

**Gaus mean : 42.3102**

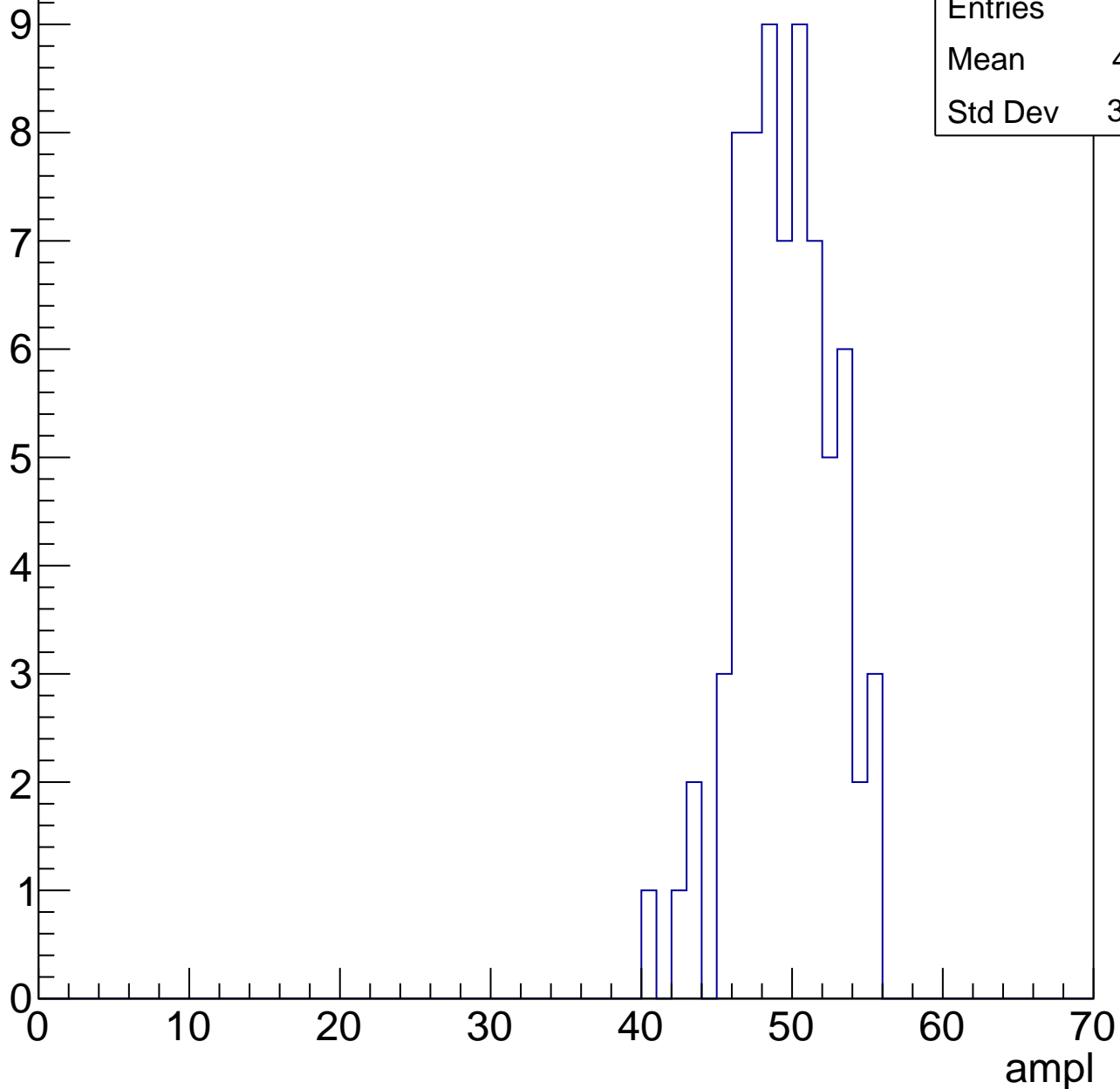
**Gaus Width: 3.2536**



# B1L100S, U2-ch46, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

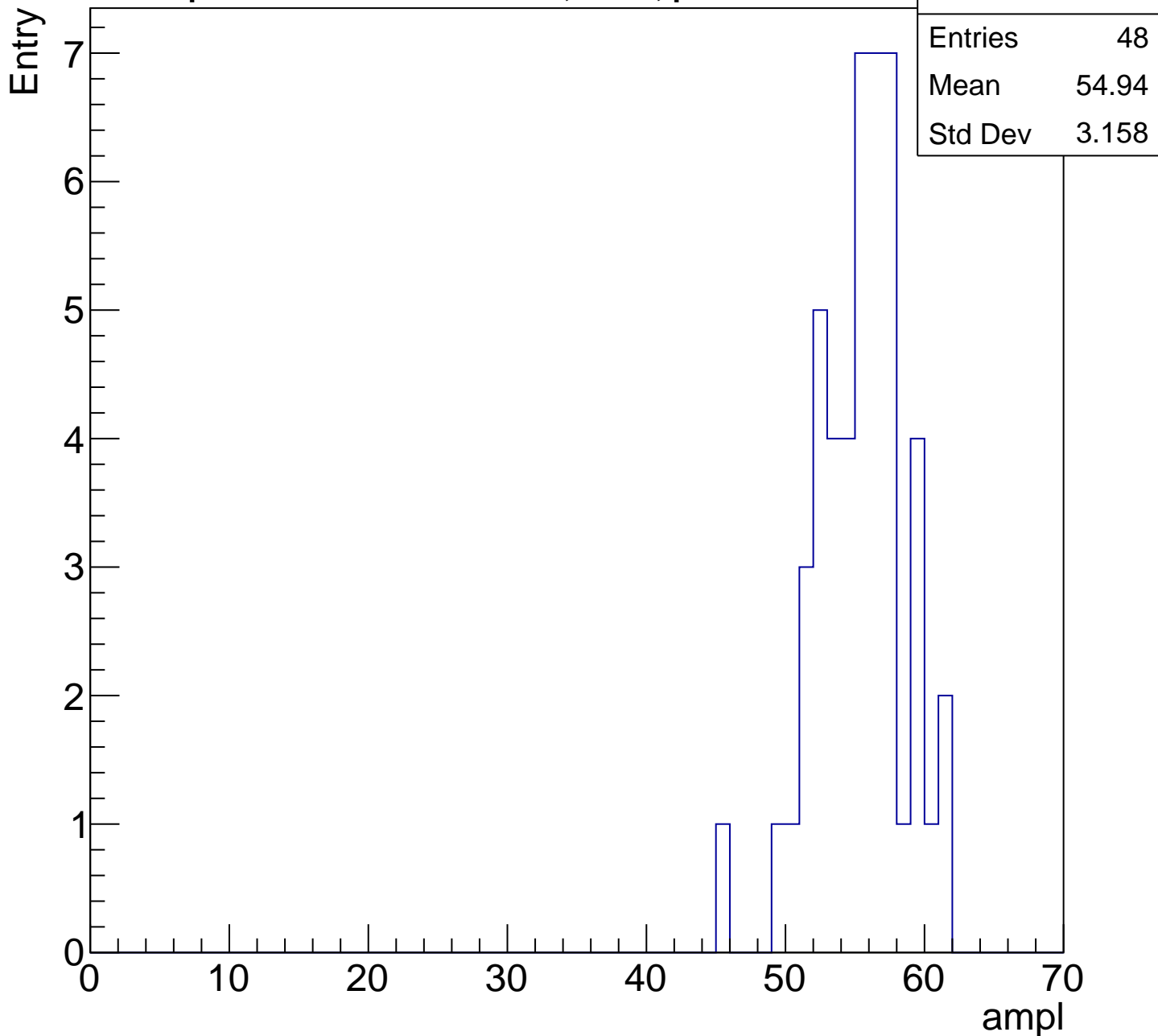
Entry



Entries	71
Mean	49.01
Std Dev	3.138

# B1L100S, U2-ch46, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

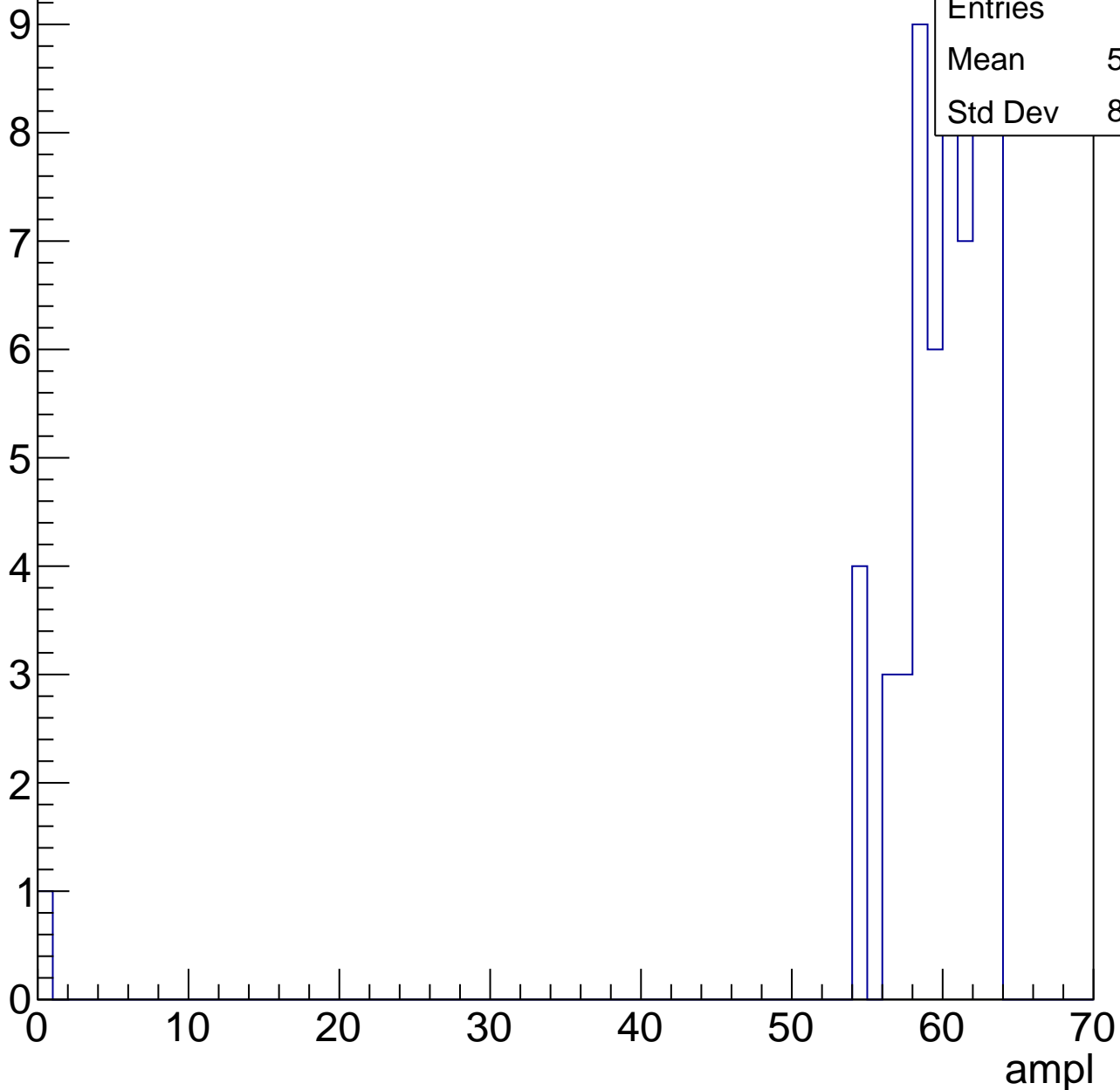


# B1L100S, U2-ch46, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	59
Mean	58.64
Std Dev	8.096



# B1L100S, U2-ch46, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry





# B1L100S, U2-ch46, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L100S, U2-ch47, adc0

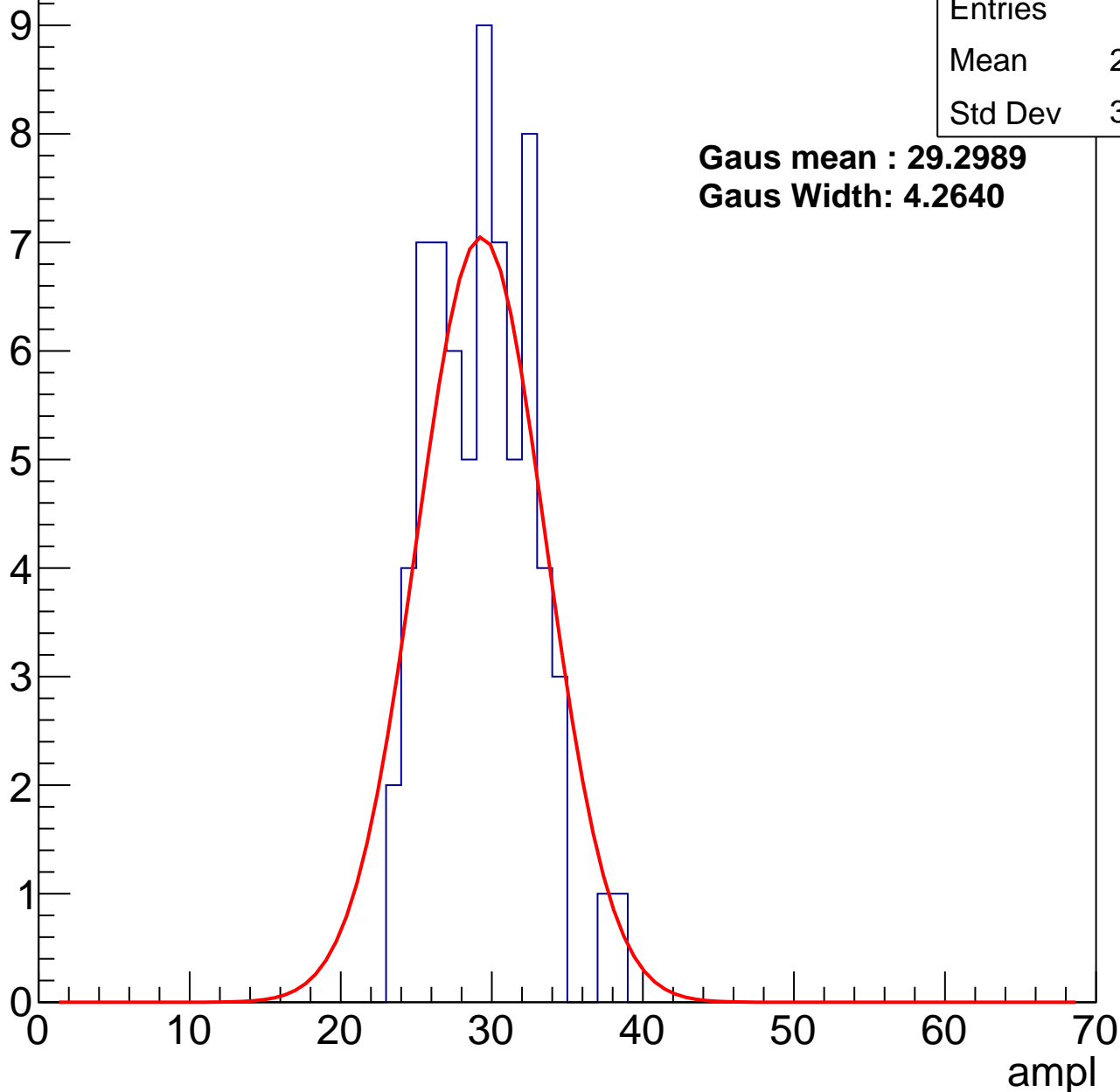
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	69
Mean	28.87
Std Dev	3.314

**Gaus mean : 29.2989**

**Gaus Width: 4.2640**



# B1L100S, U2-ch47, adc1

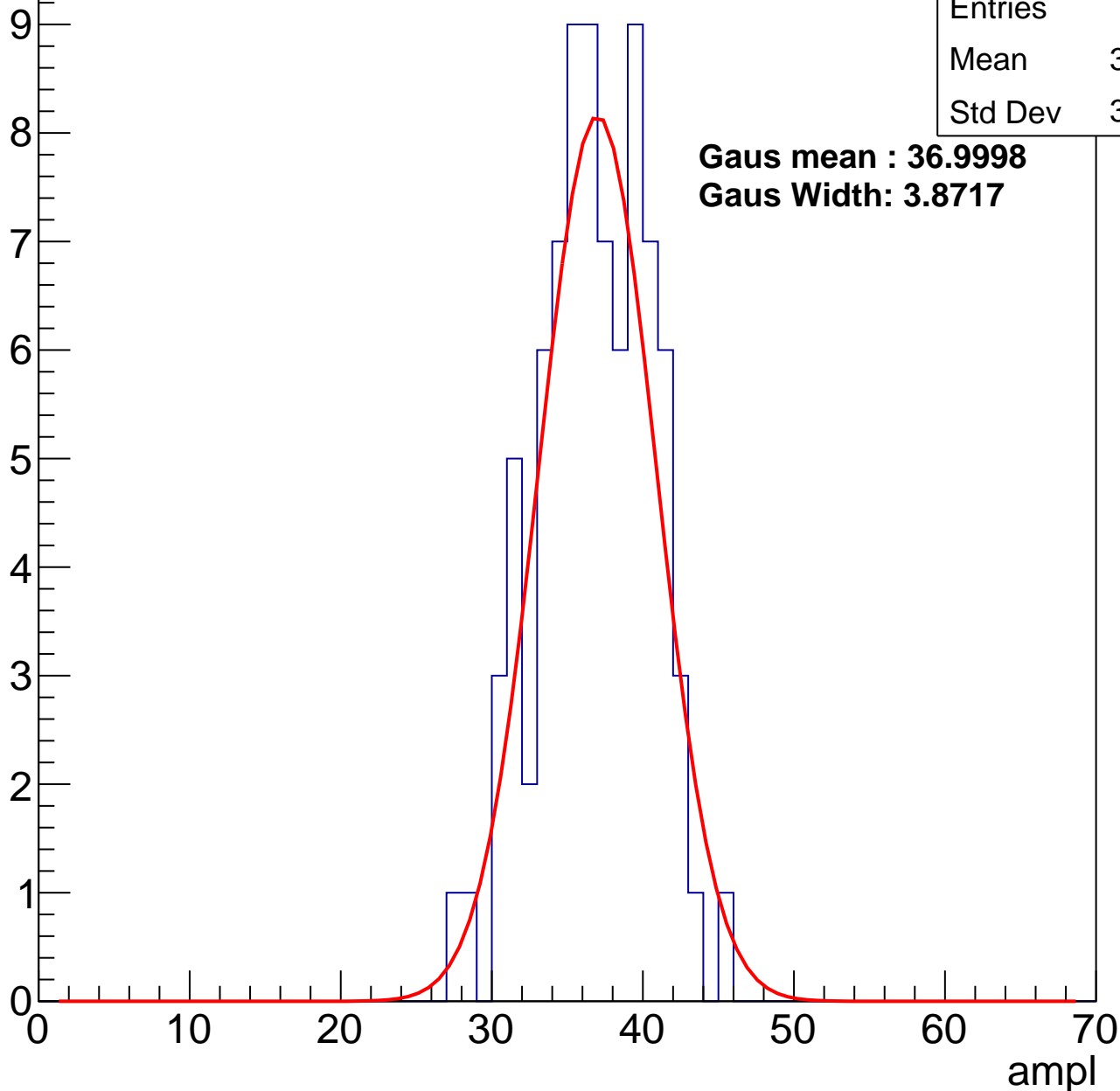
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	83
Mean	36.35
Std Dev	3.645

**Gaus mean : 36.9998**

**Gaus Width: 3.8717**



# B1L100S, U2-ch47, adc2

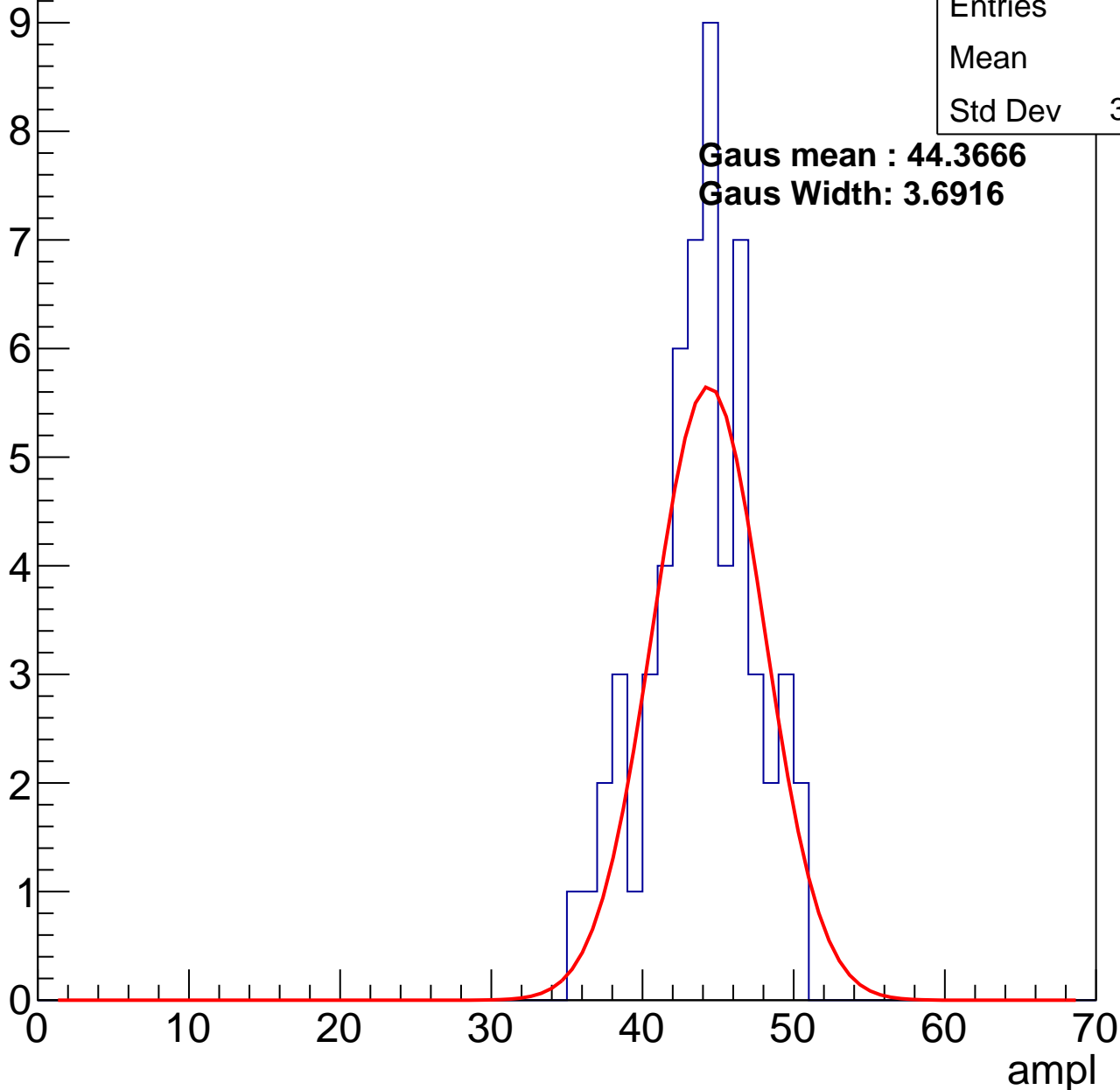
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	58
Mean	43.4
Std Dev	3.494

**Gaus mean : 44.3666**

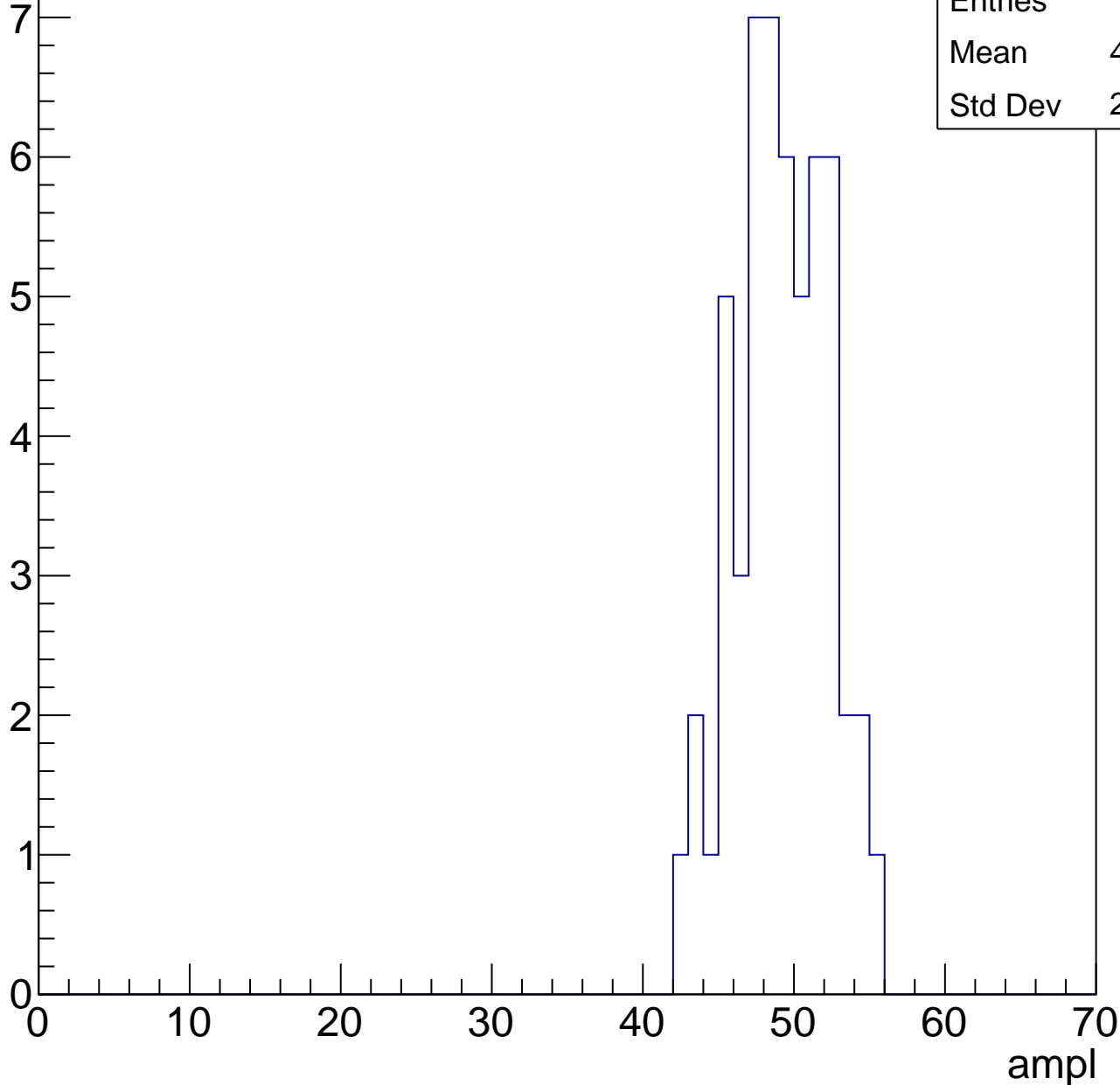
**Gaus Width: 3.6916**



# B1L100S, U2-ch47, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

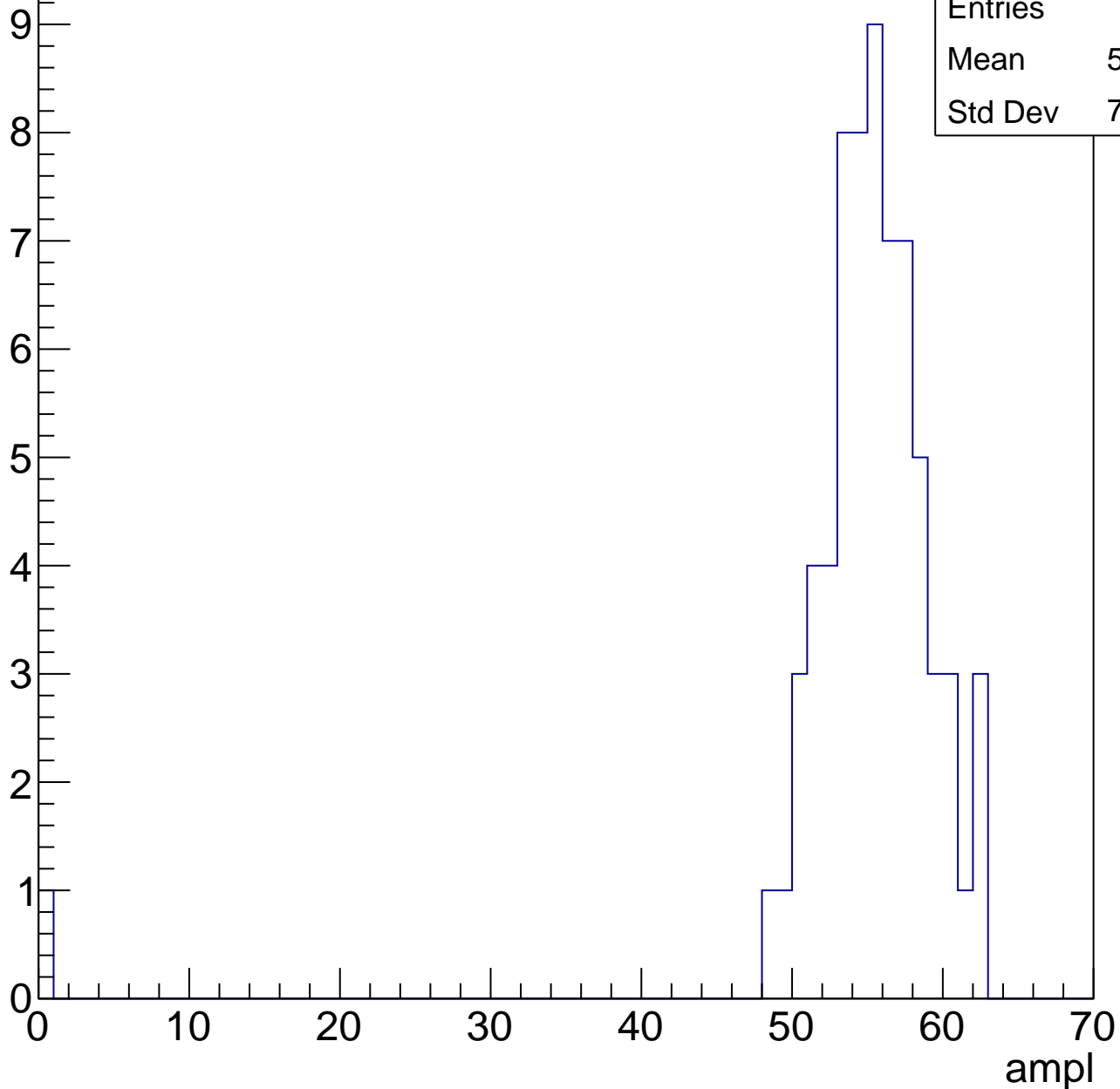


Entries	54
Mean	48.72
Std Dev	2.996

# B1L100S, U2-ch47, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

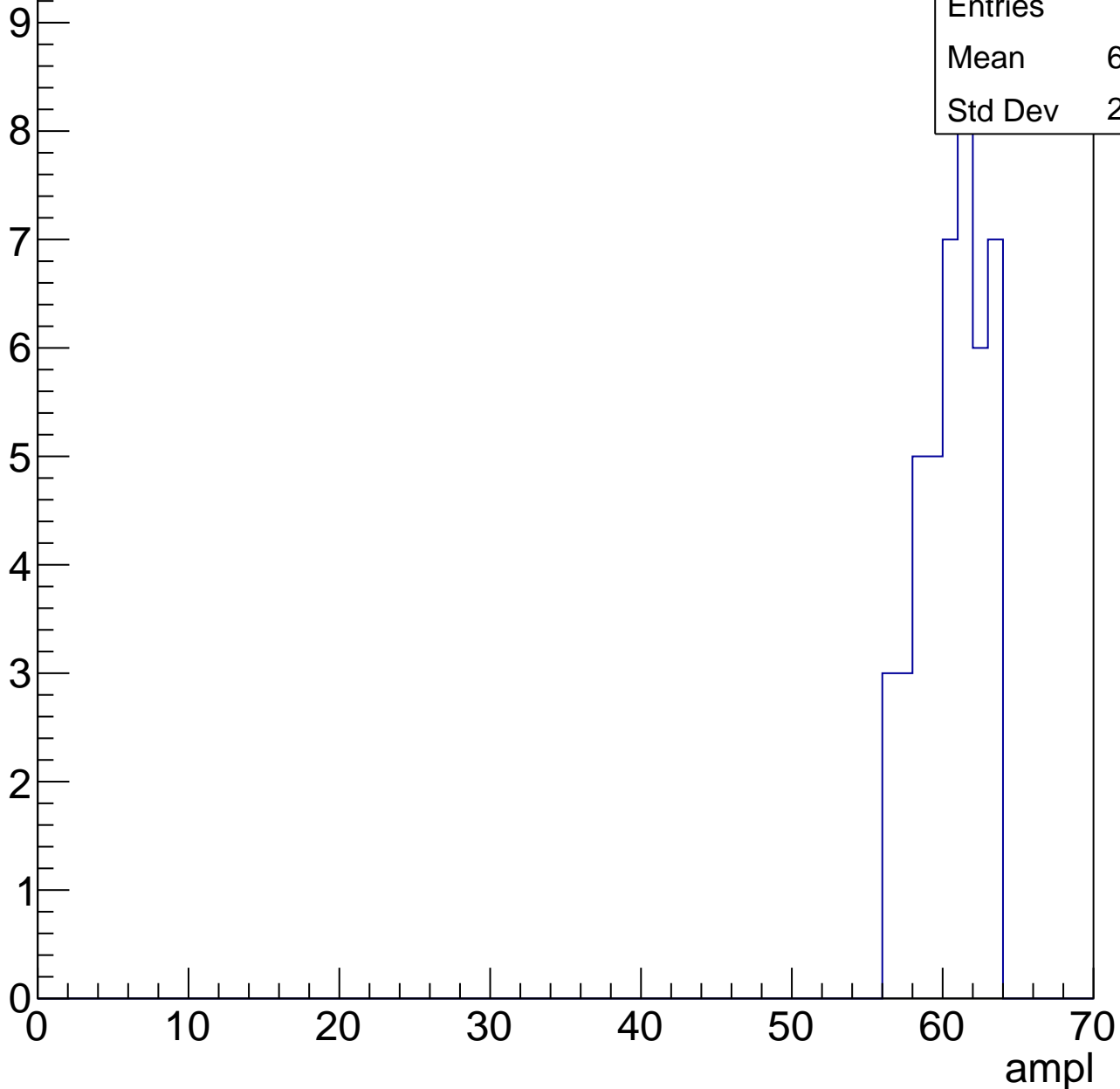


Entries	68
Mean	54.34
Std Dev	7.358

# B1L100S, U2-ch47, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

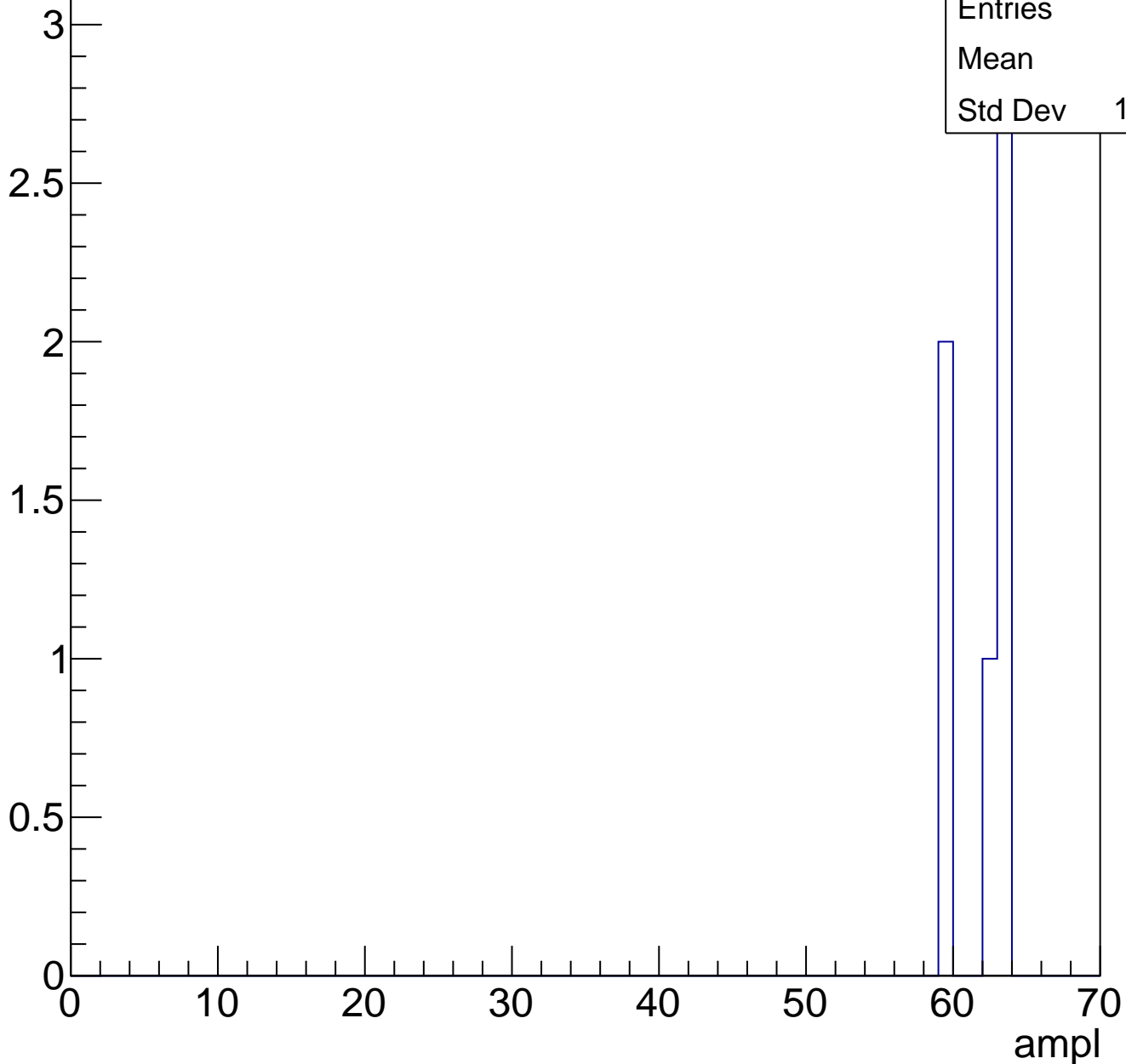
Entry



# B1L100S, U2-ch47, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

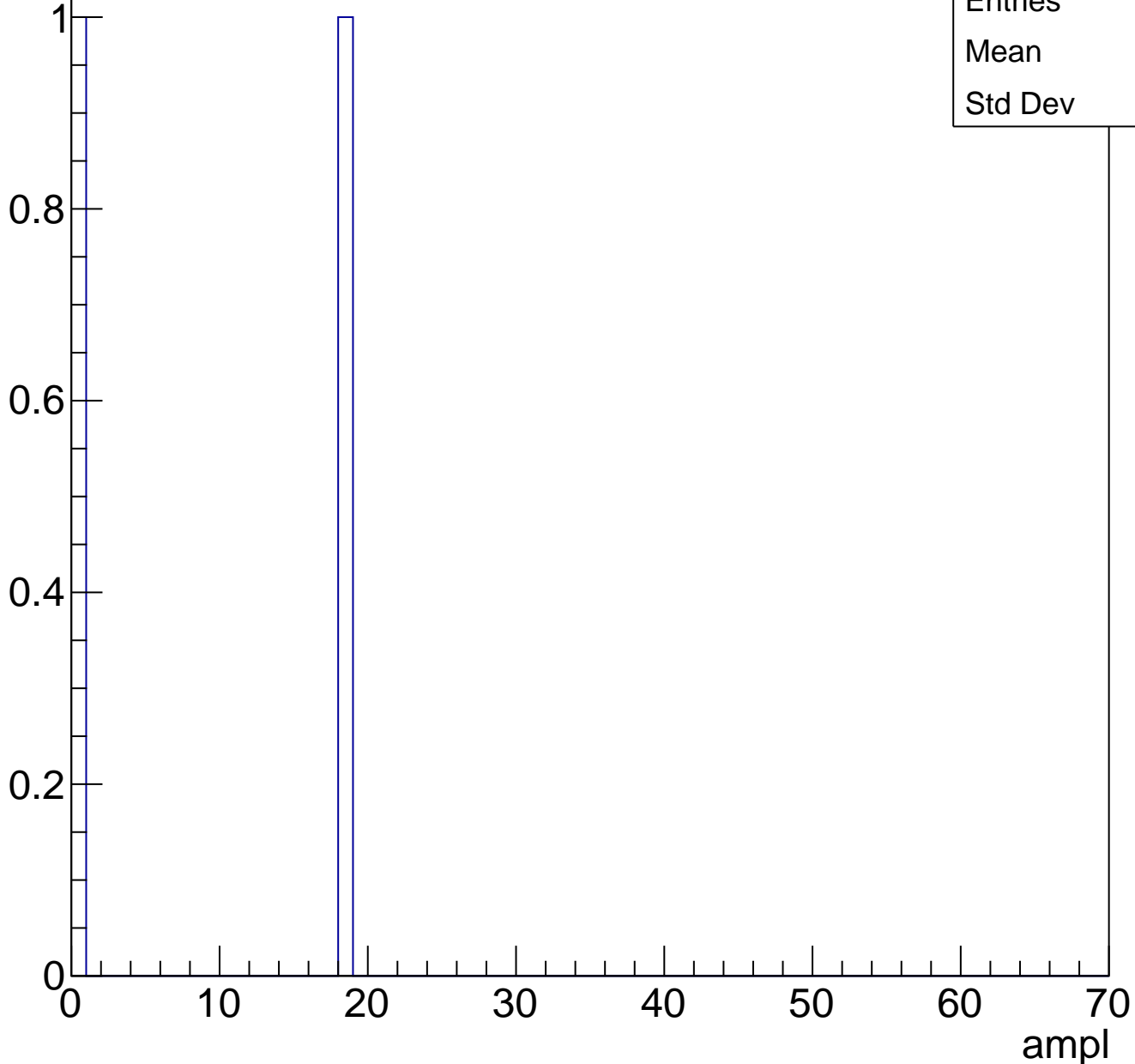




# B1L100S, U2-ch47, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	2
Mean	9
Std Dev	9

# B1L100S, U2-ch48, adc0

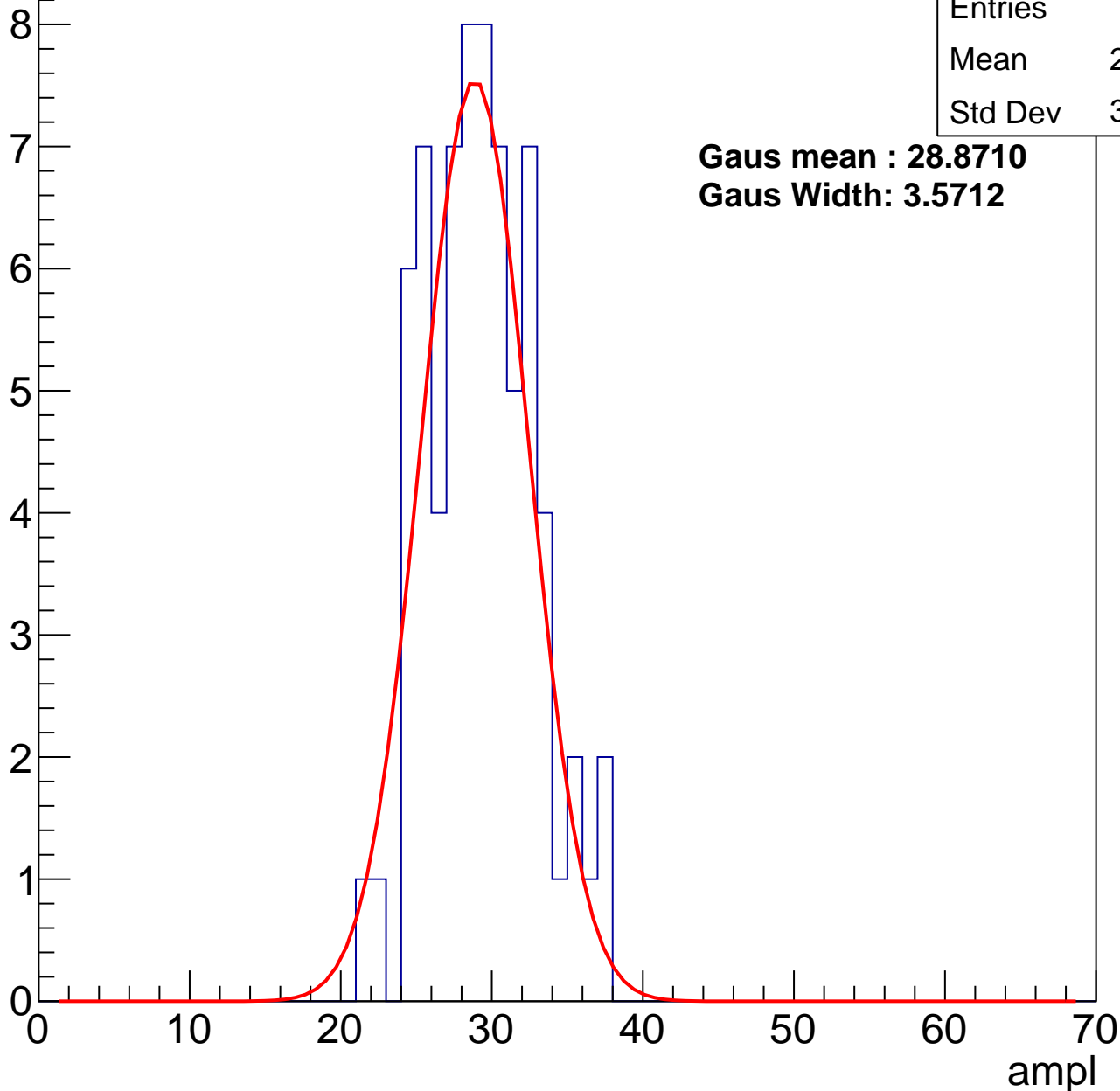
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	71
Mean	28.82
Std Dev	3.506

**Gaus mean : 28.8710**

**Gaus Width: 3.5712**



# B1L100S, U2-ch48, adc1

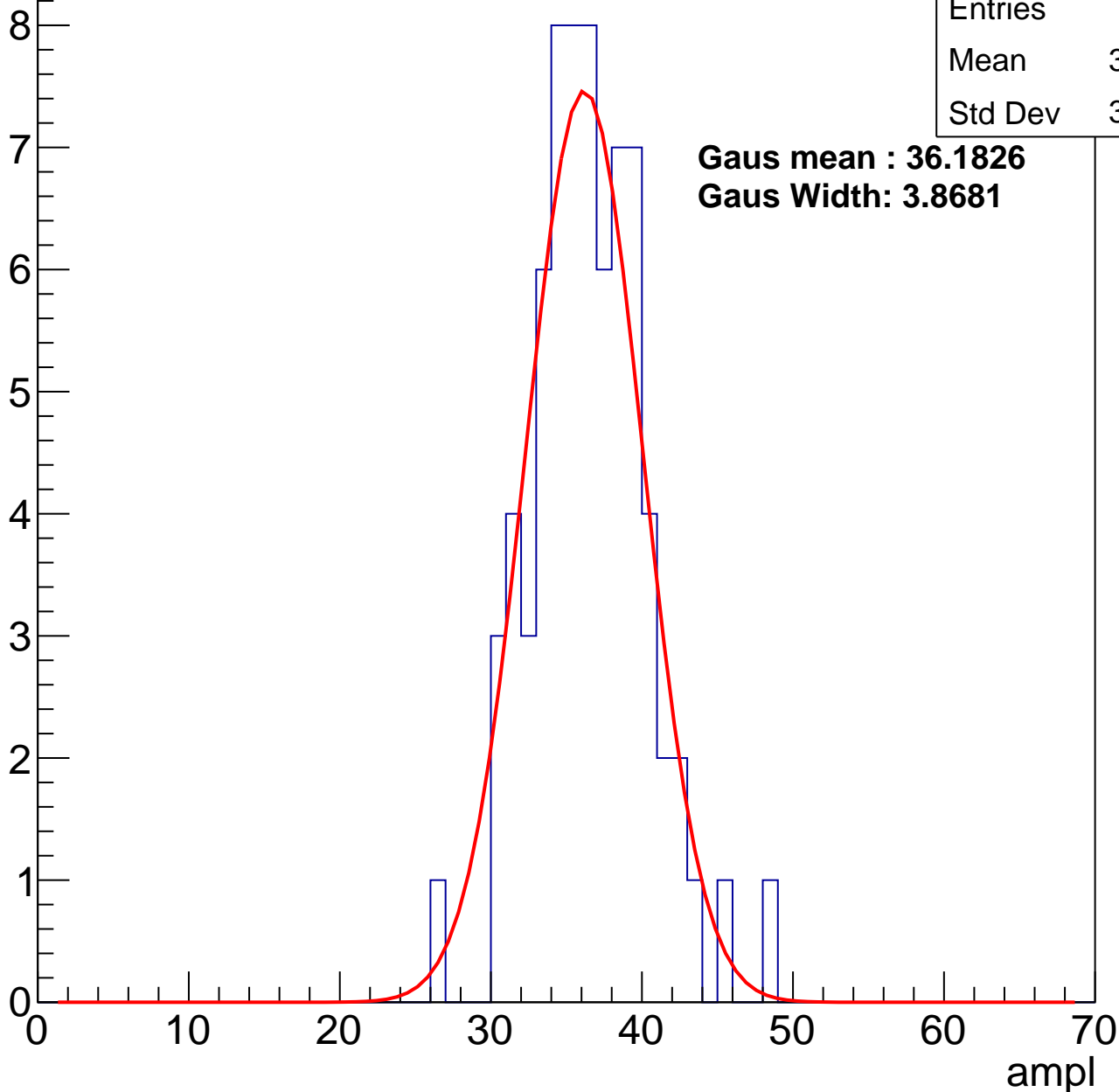
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	72
Mean	36.07
Std Dev	3.739

**Gaus mean : 36.1826**

**Gaus Width: 3.8681**

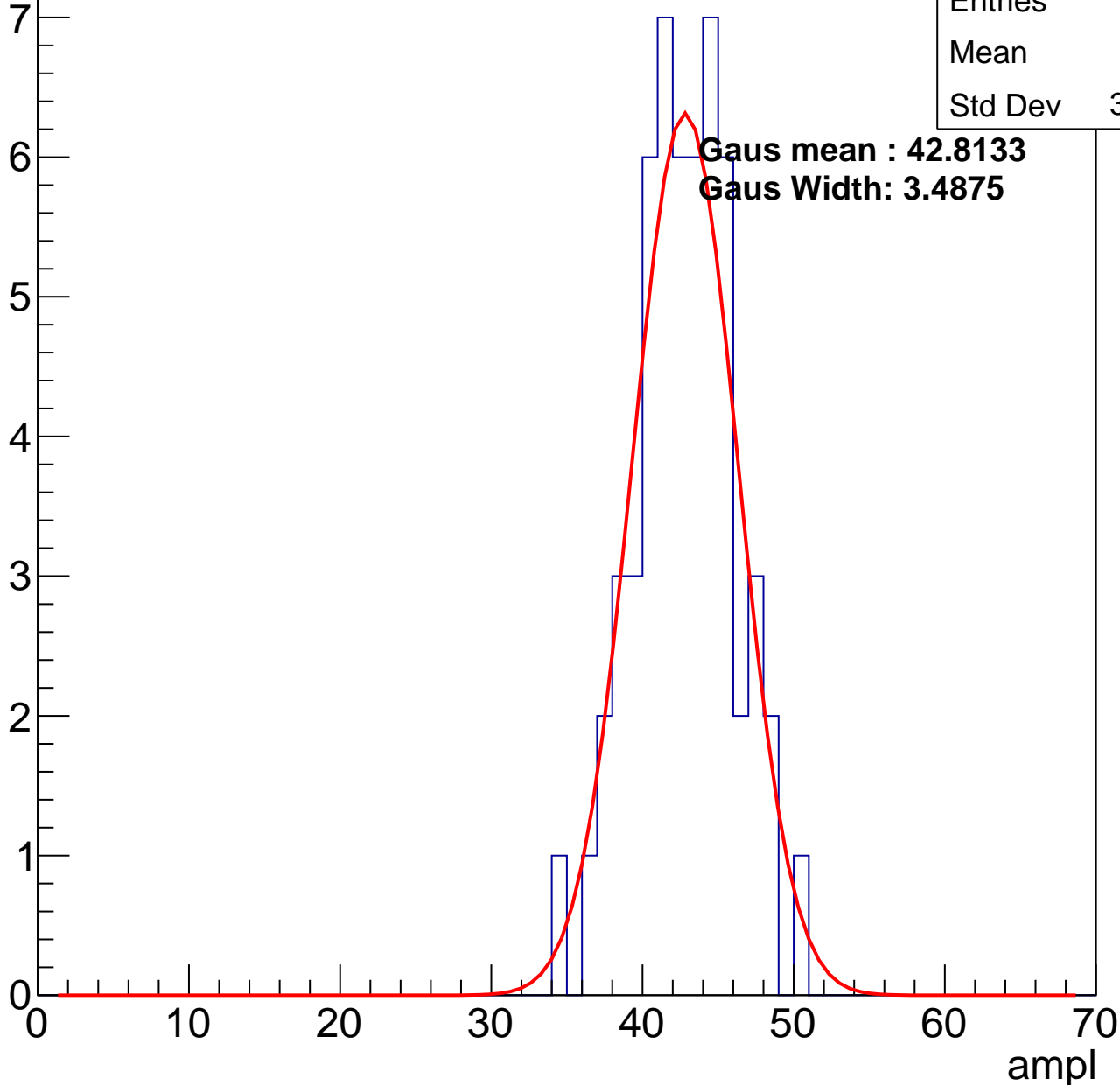


# B1L100S, U2-ch48, adc2

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	56
Mean	42.3
Std Dev	3.223

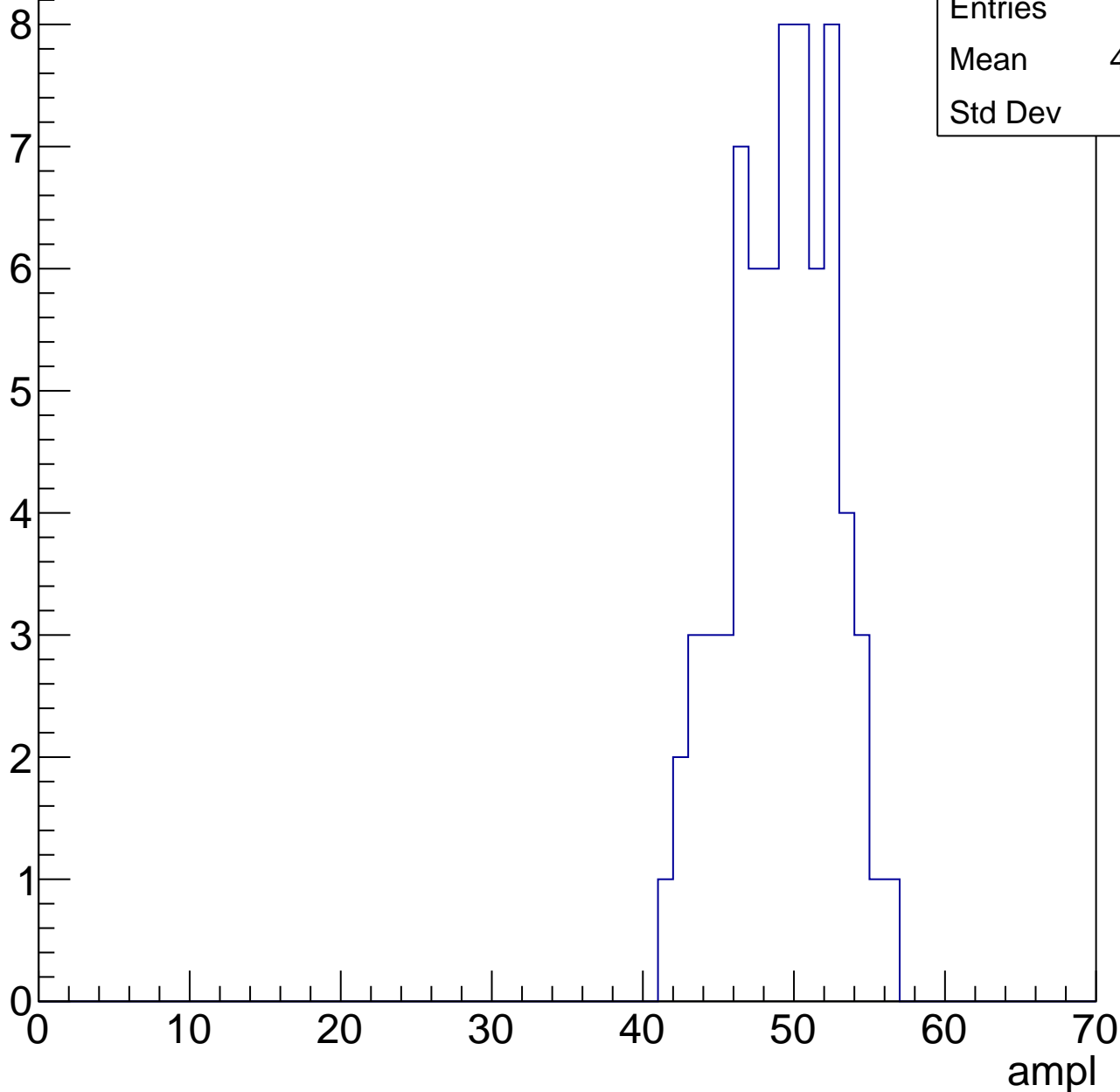


# B1L100S, U2-ch48, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	70
Mean	48.74
Std Dev	3.4



# B1L100S, U2-ch48, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

6

5

4

3

2

1

0

Entries 51

Mean 54.94

Std Dev 3.589

0

10

20

30

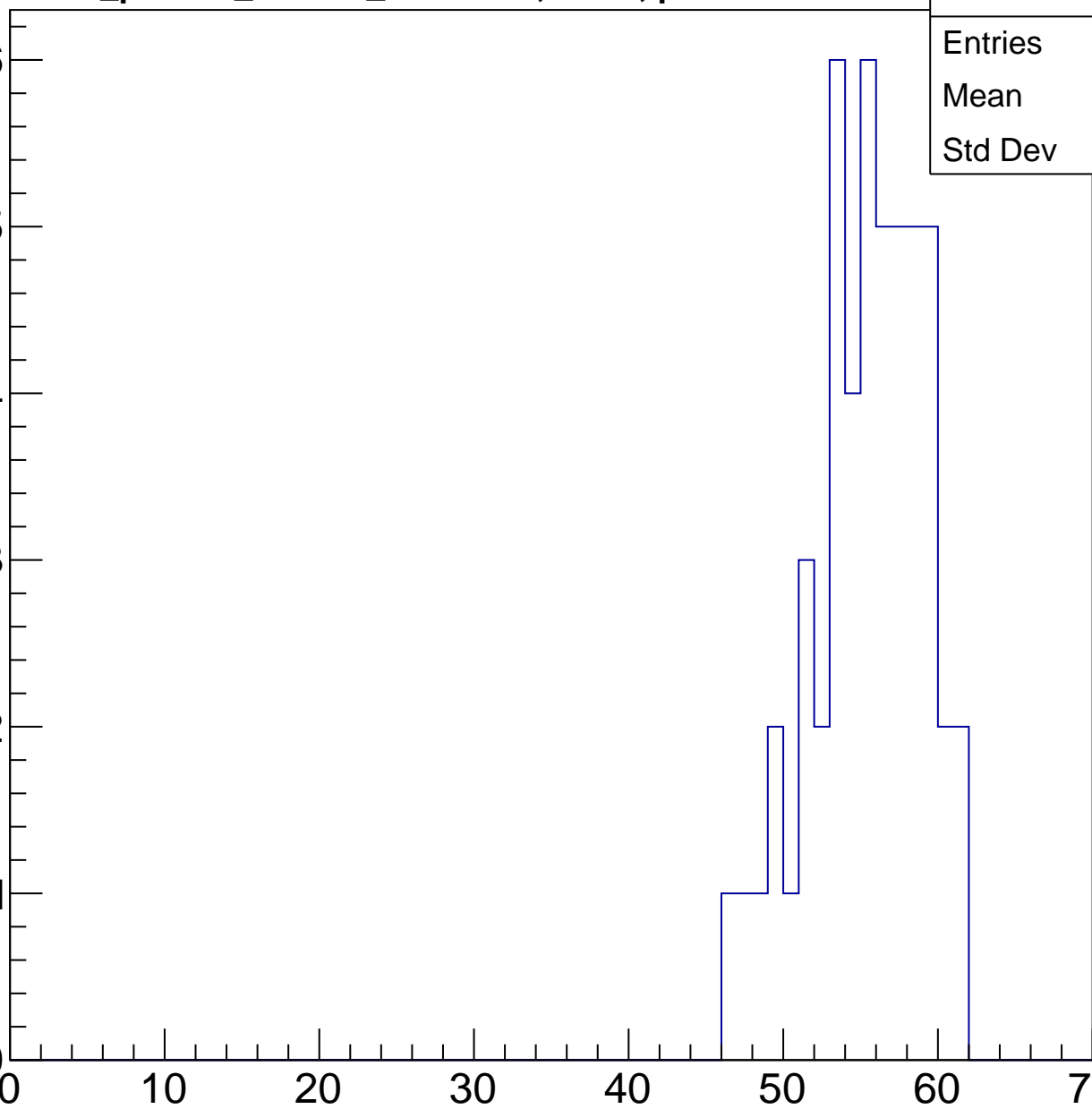
40

50

60

70

ampl

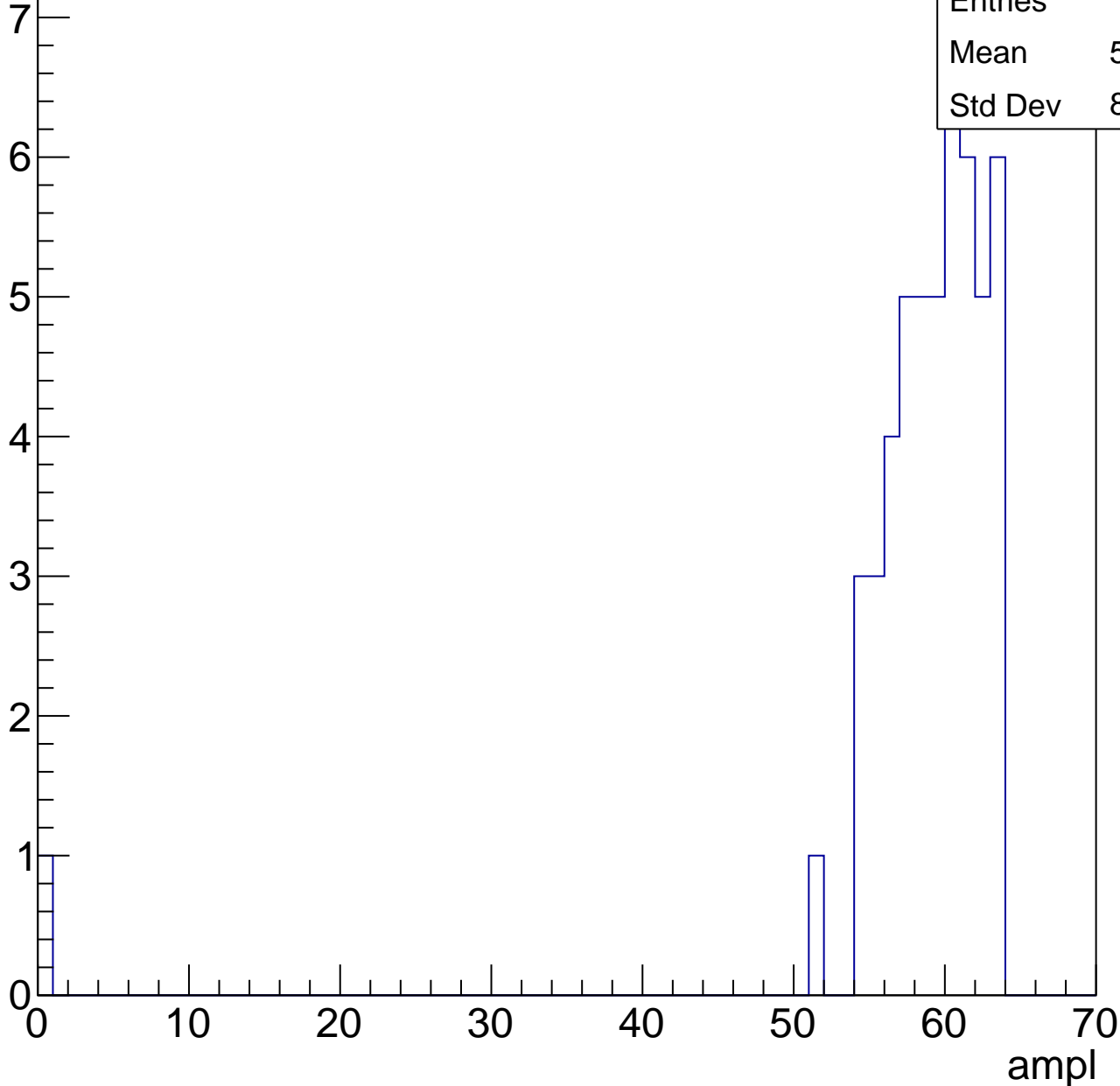


# B1L100S, U2-ch48, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	51
Mean	57.76
Std Dev	8.658

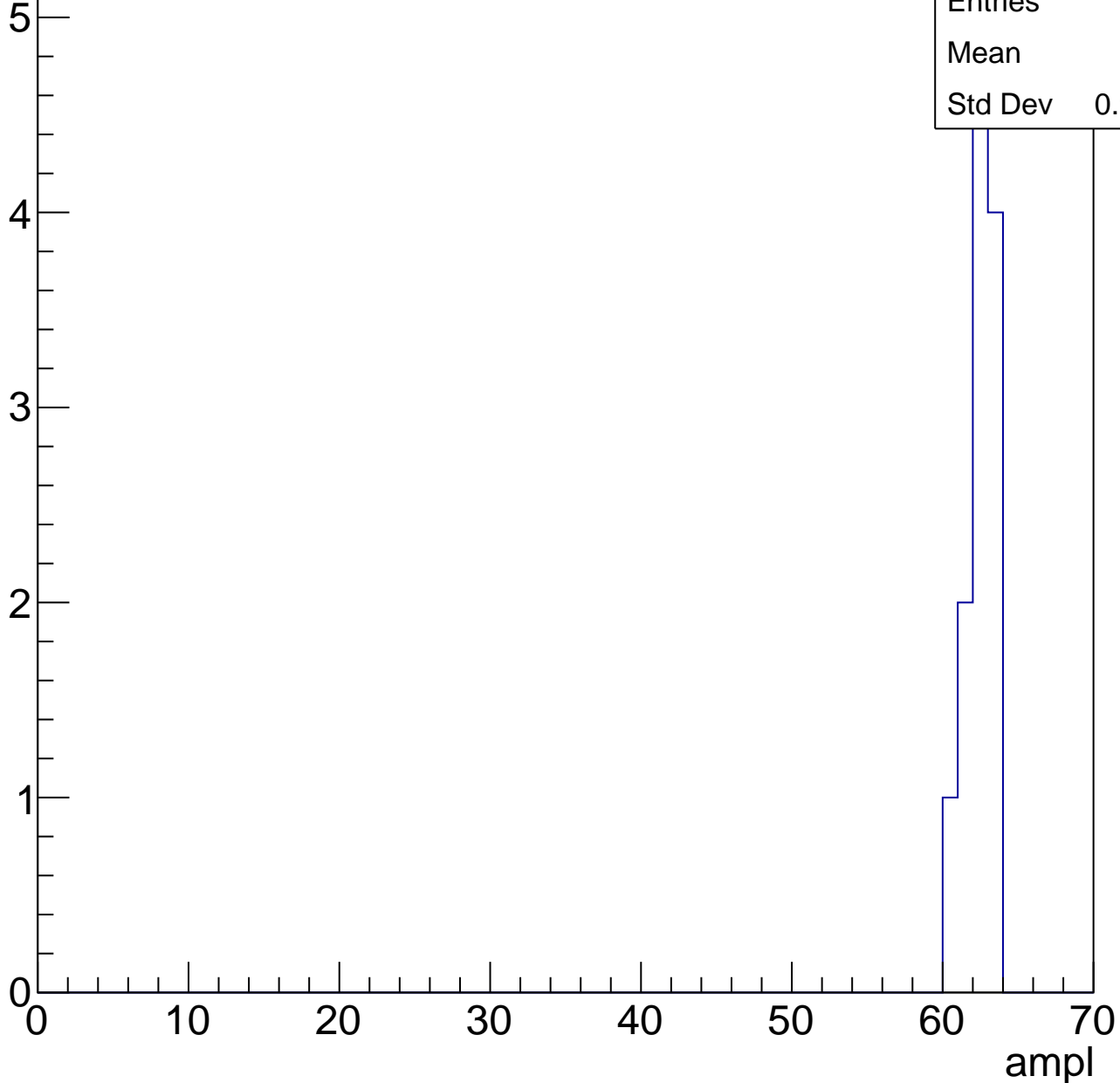


# B1L100S, U2-ch48, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	12
Mean	62
Std Dev	0.9129





# B1L100S, U2-ch48, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



# B1L100S, U2-ch49, adc0

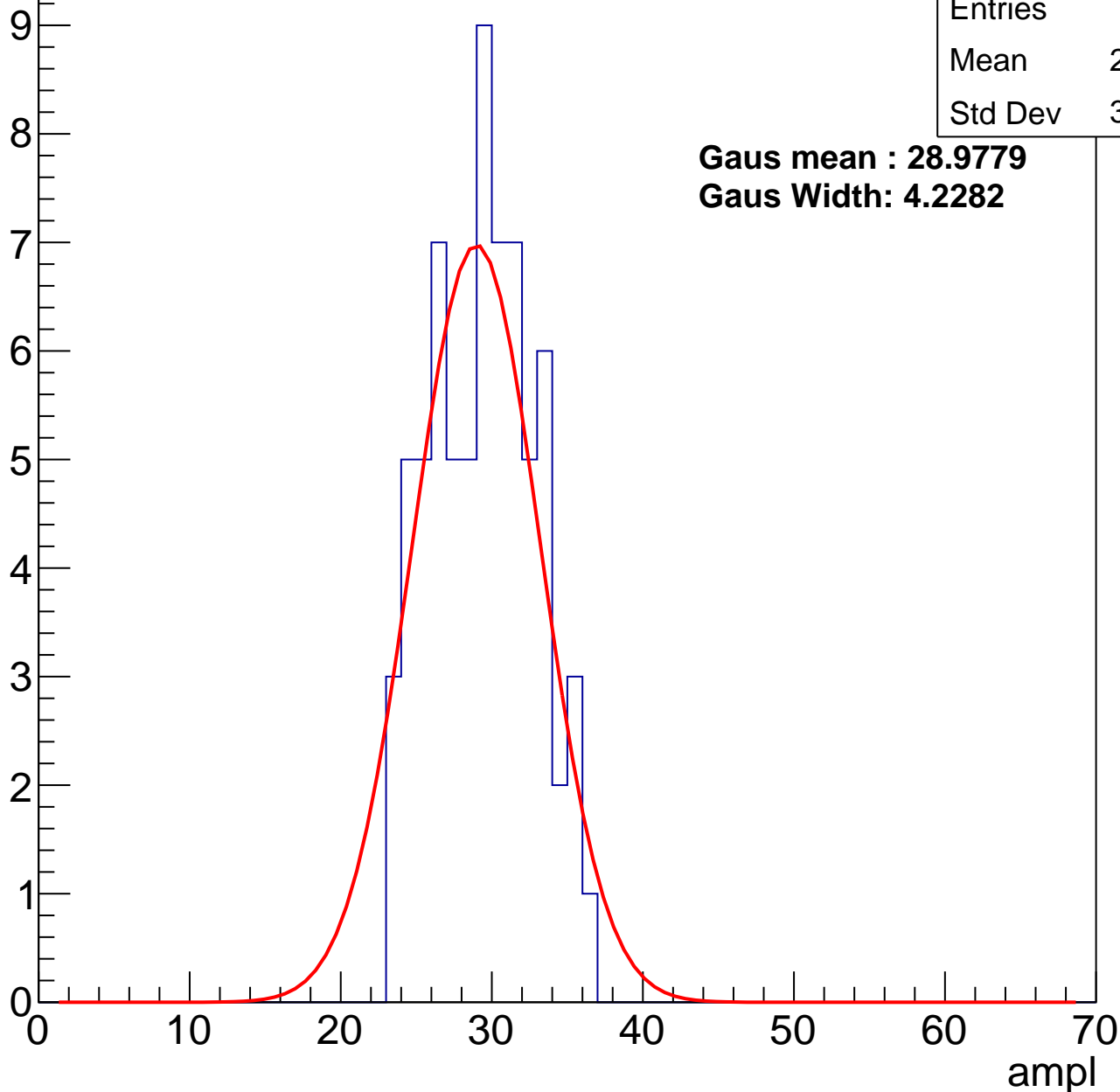
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	70
Mean	28.94
Std Dev	3.346

**Gaus mean : 28.9779**

**Gaus Width: 4.2282**



# B1L100S, U2-ch49, adc1

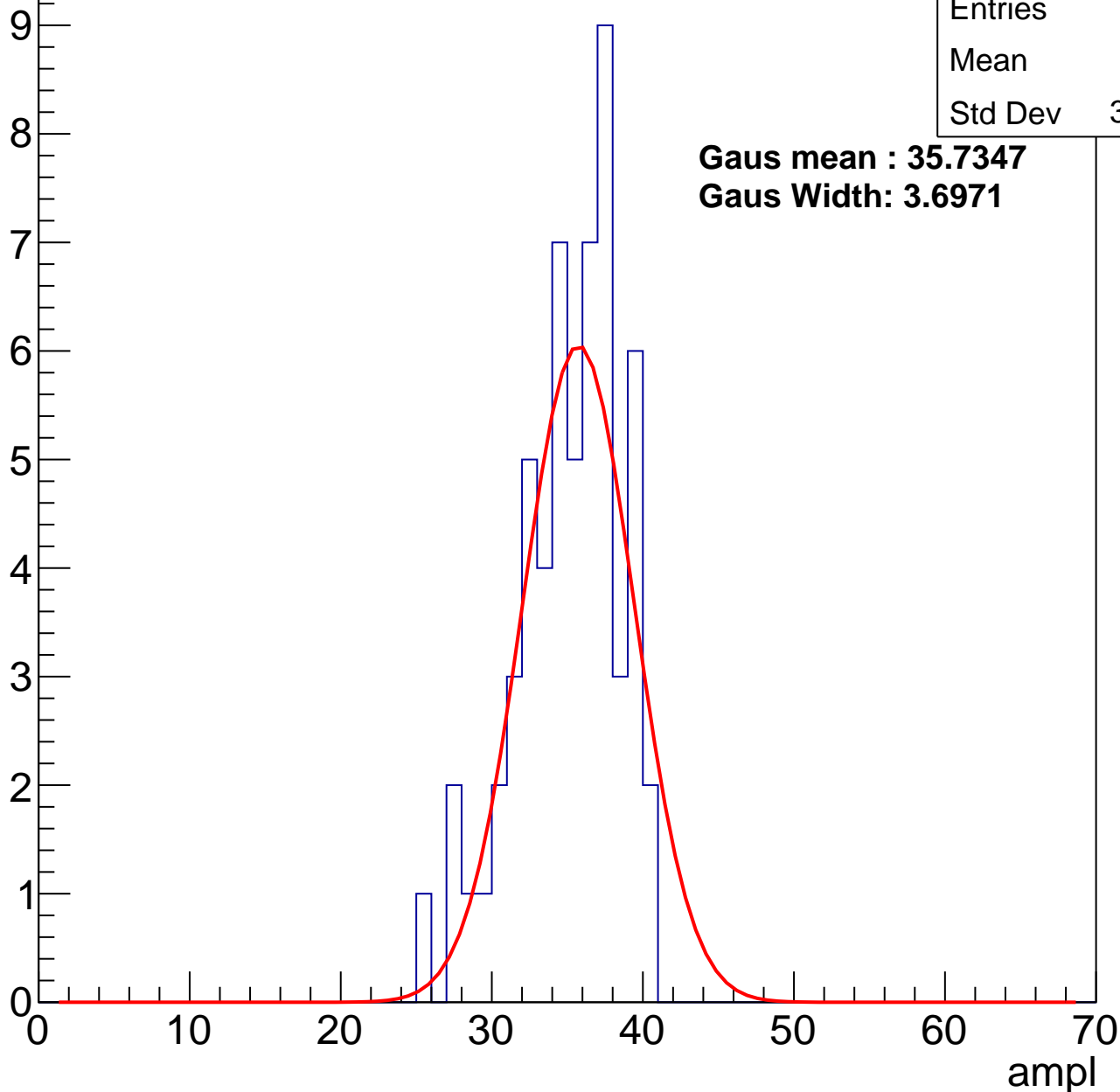
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	58
Mean	34.6
Std Dev	3.439

**Gaus mean : 35.7347**

**Gaus Width: 3.6971**



# B1L100S, U2-ch49, adc2

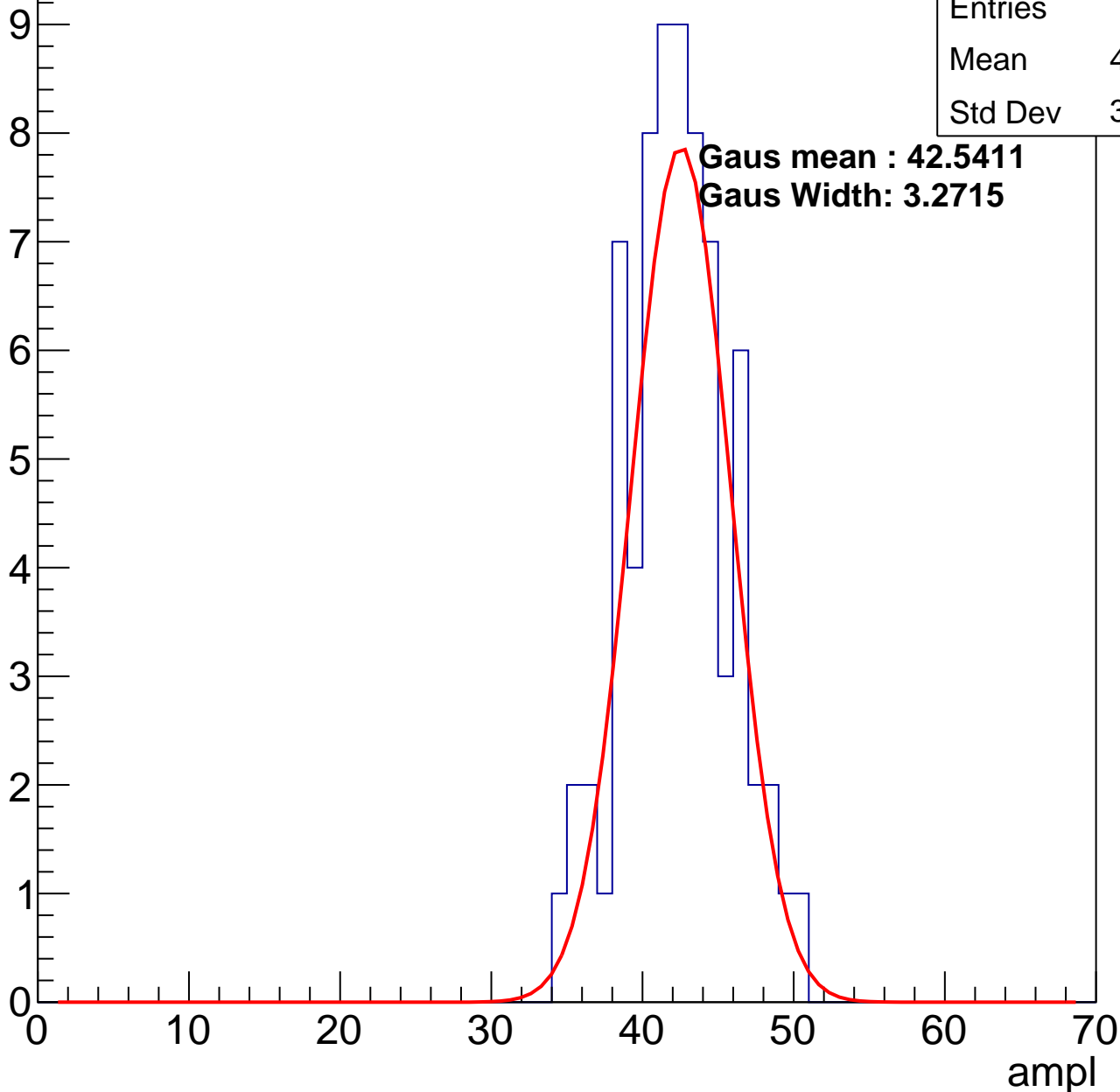
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	73
Mean	41.84
Std Dev	3.392

**Gaus mean : 42.5411**

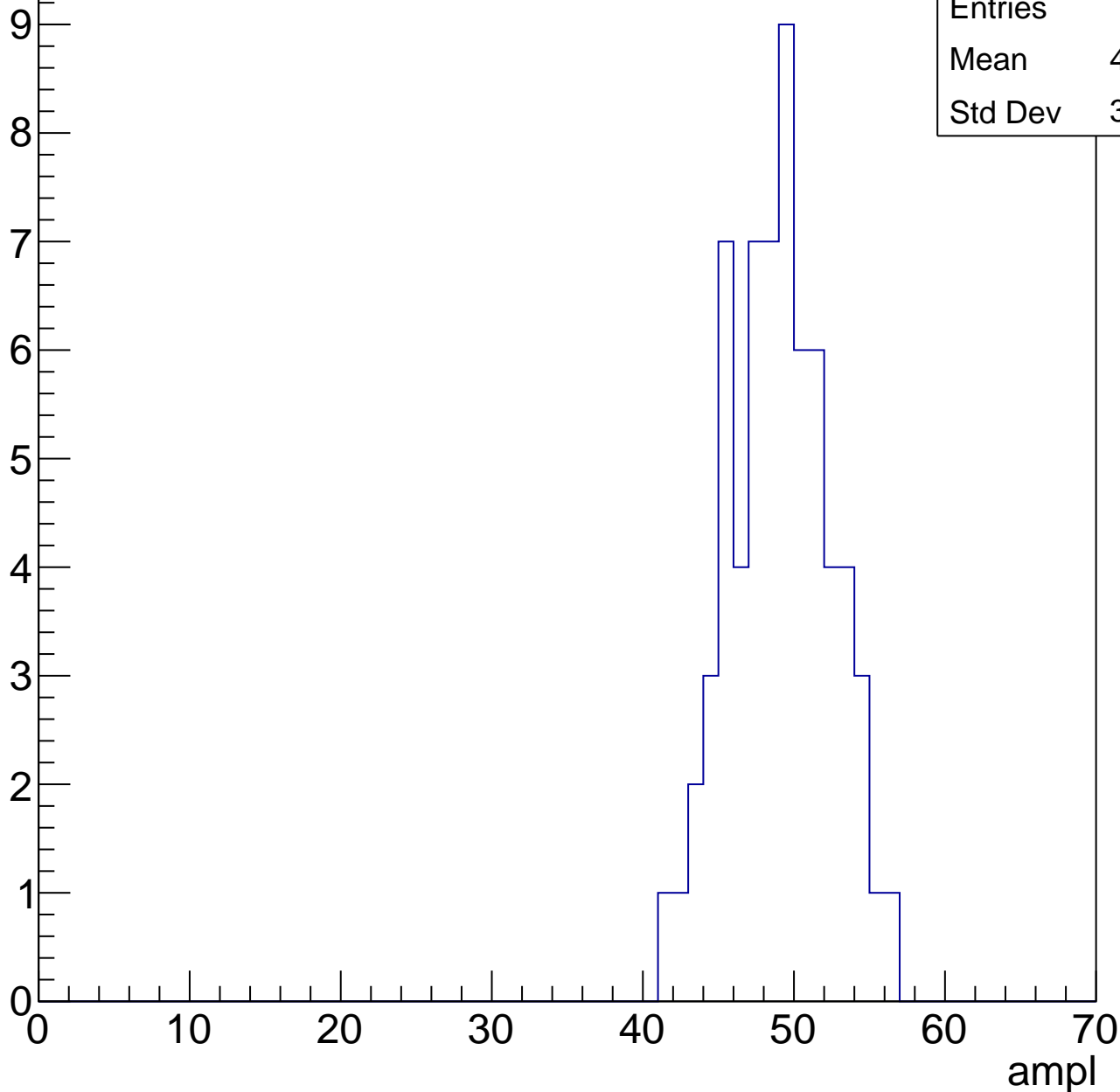
**Gaus Width: 3.2715**



# B1L100S, U2-ch49, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

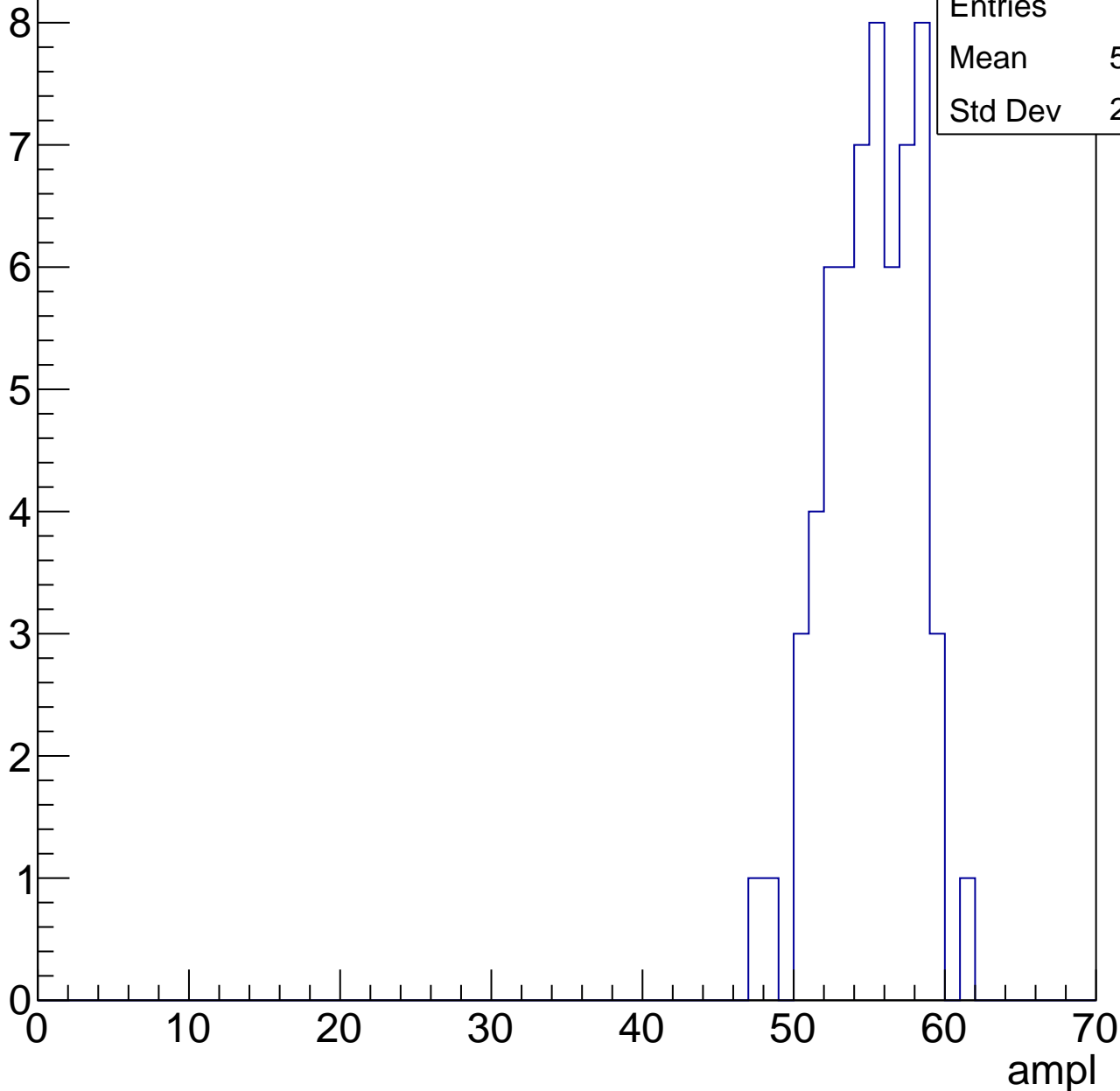


# B1L100S, U2-ch49, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

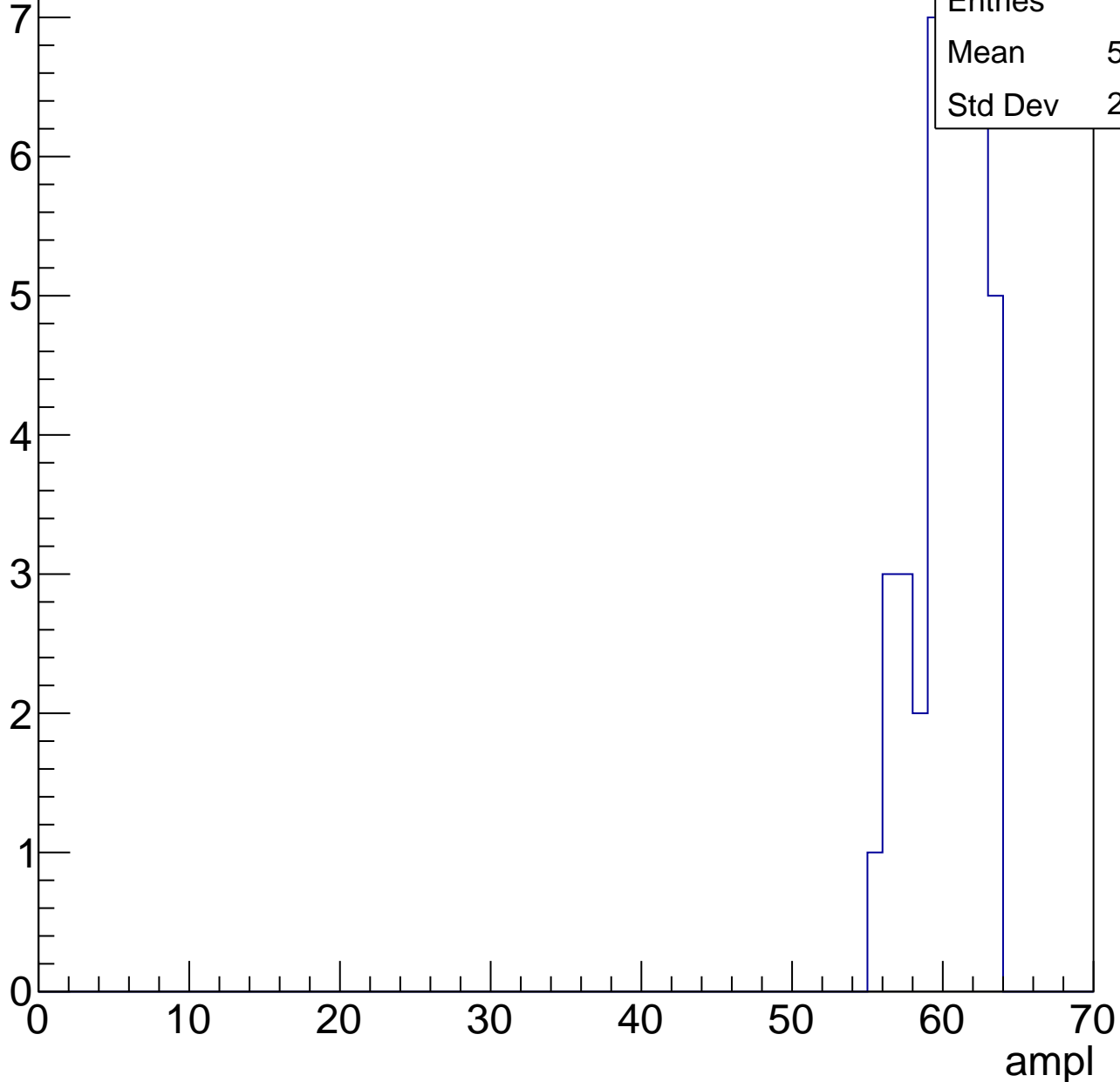
Entries	61
Mean	54.66
Std Dev	2.919



# B1L100S, U2-ch49, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

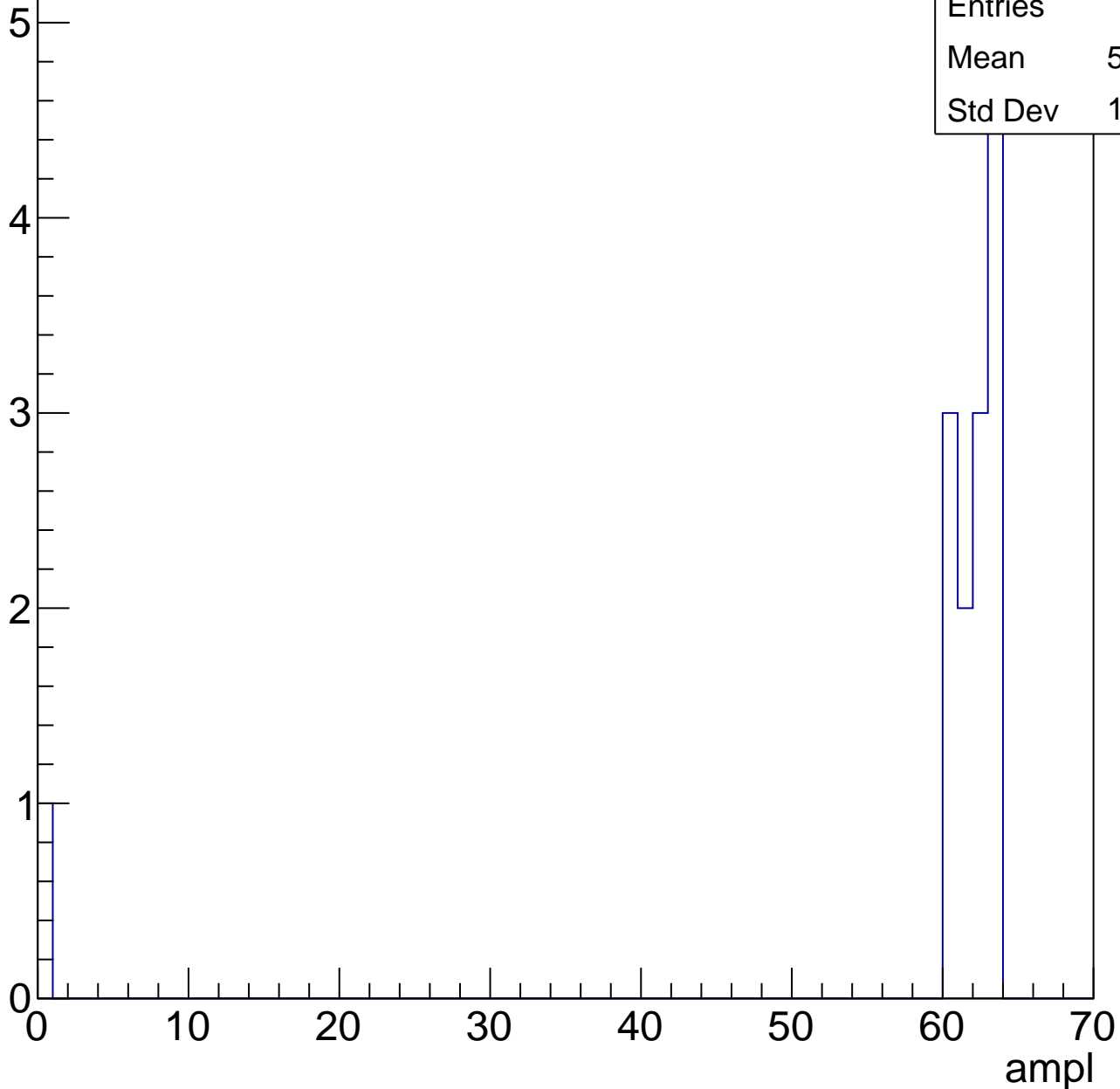


# B1L100S, U2-ch49, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	14
Mean	57.36
Std Dev	15.95





# B1L100S, U2-ch49, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L100S, U2-ch50, adc0

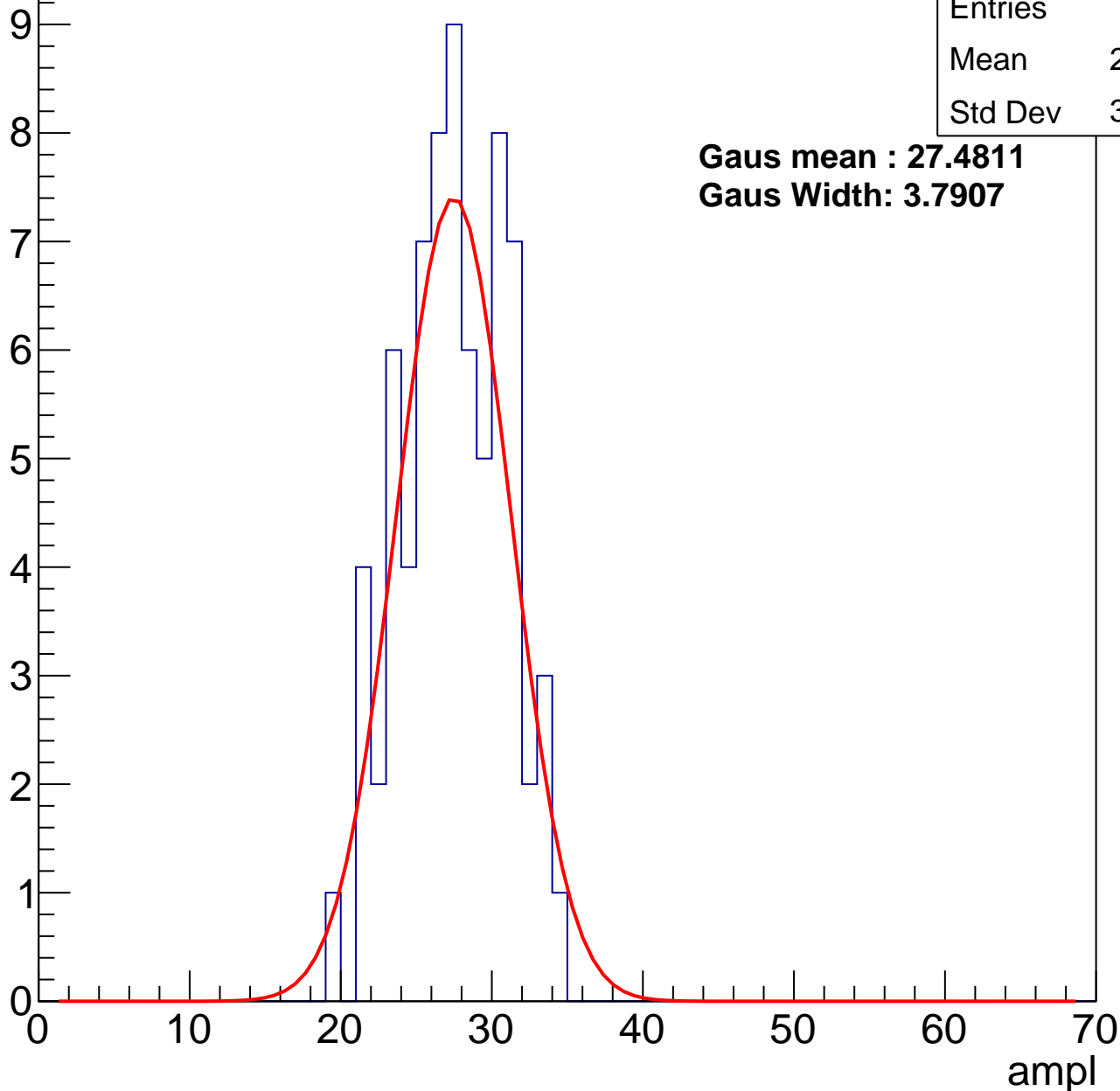
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	73
Mean	27.04
Std Dev	3.398

**Gaus mean : 27.4811**

**Gaus Width: 3.7907**



# B1L100S, U2-ch50, adc1

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	88
Mean	34.83
Std Dev	4.325

**Gaus mean : 35.7194**

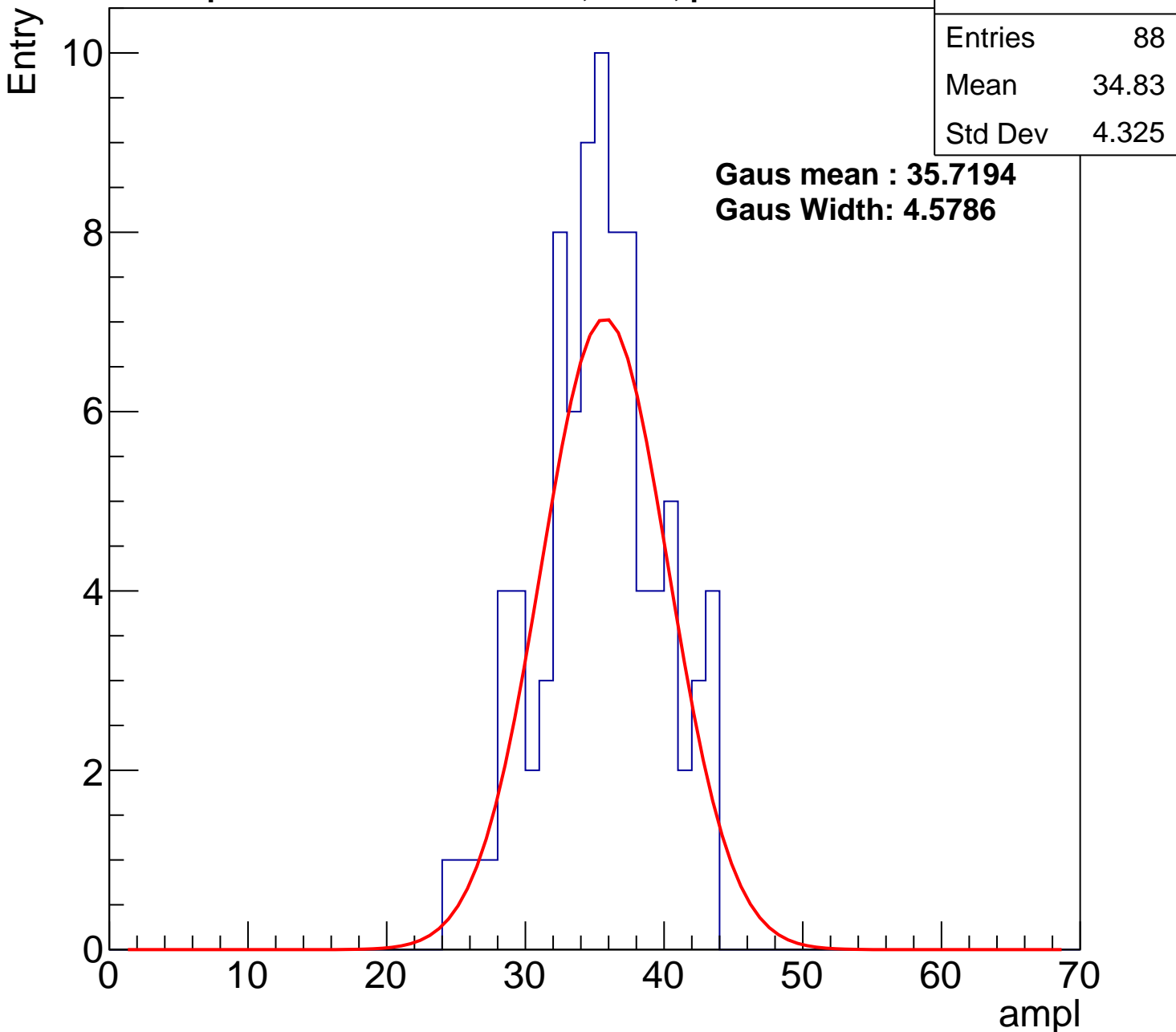
**Gaus Width: 4.5786**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L100S, U2-ch50, adc2

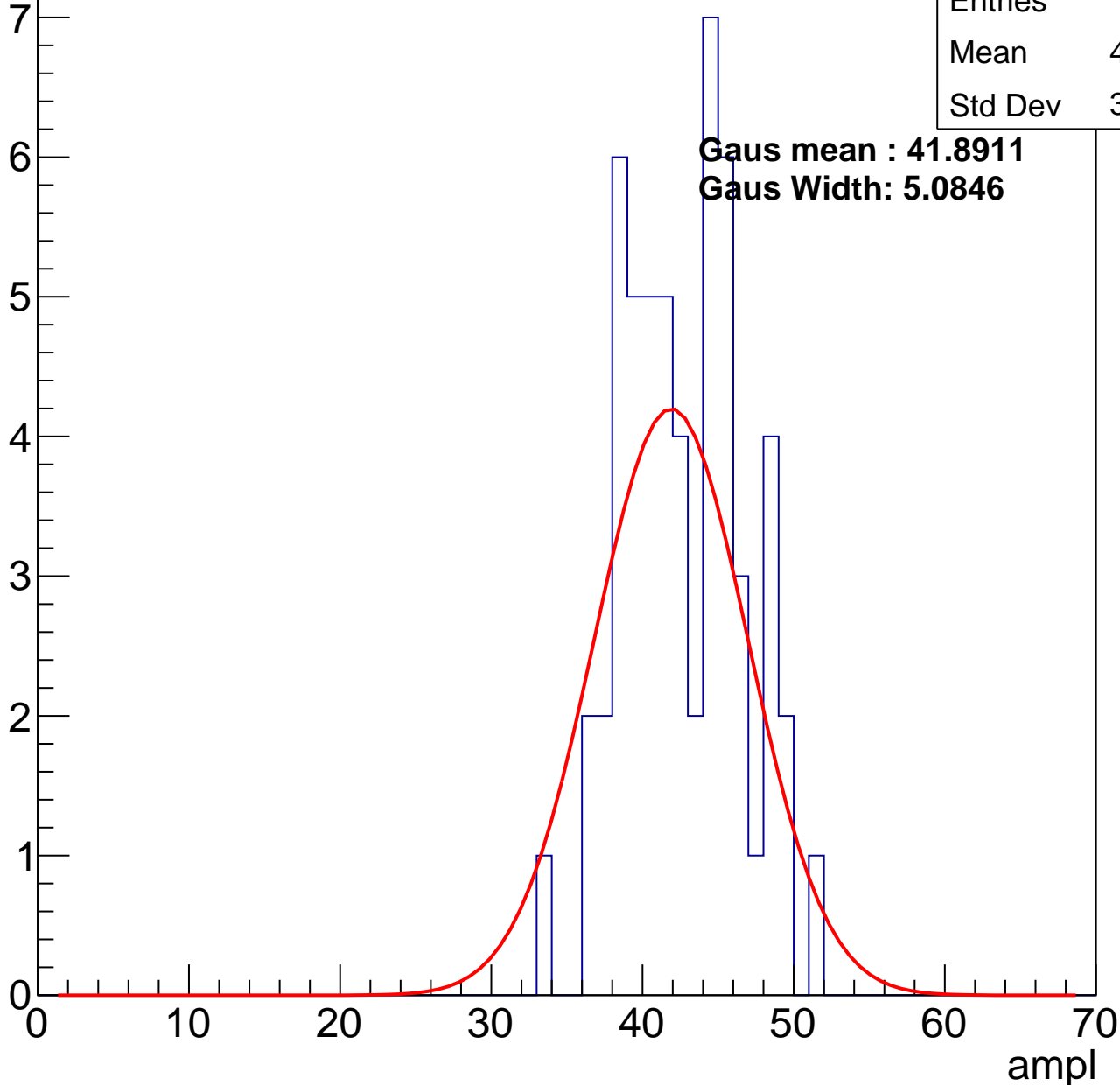
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	56
Mean	42.23
Std Dev	3.887

**Gaus mean : 41.8911**

**Gaus Width: 5.0846**

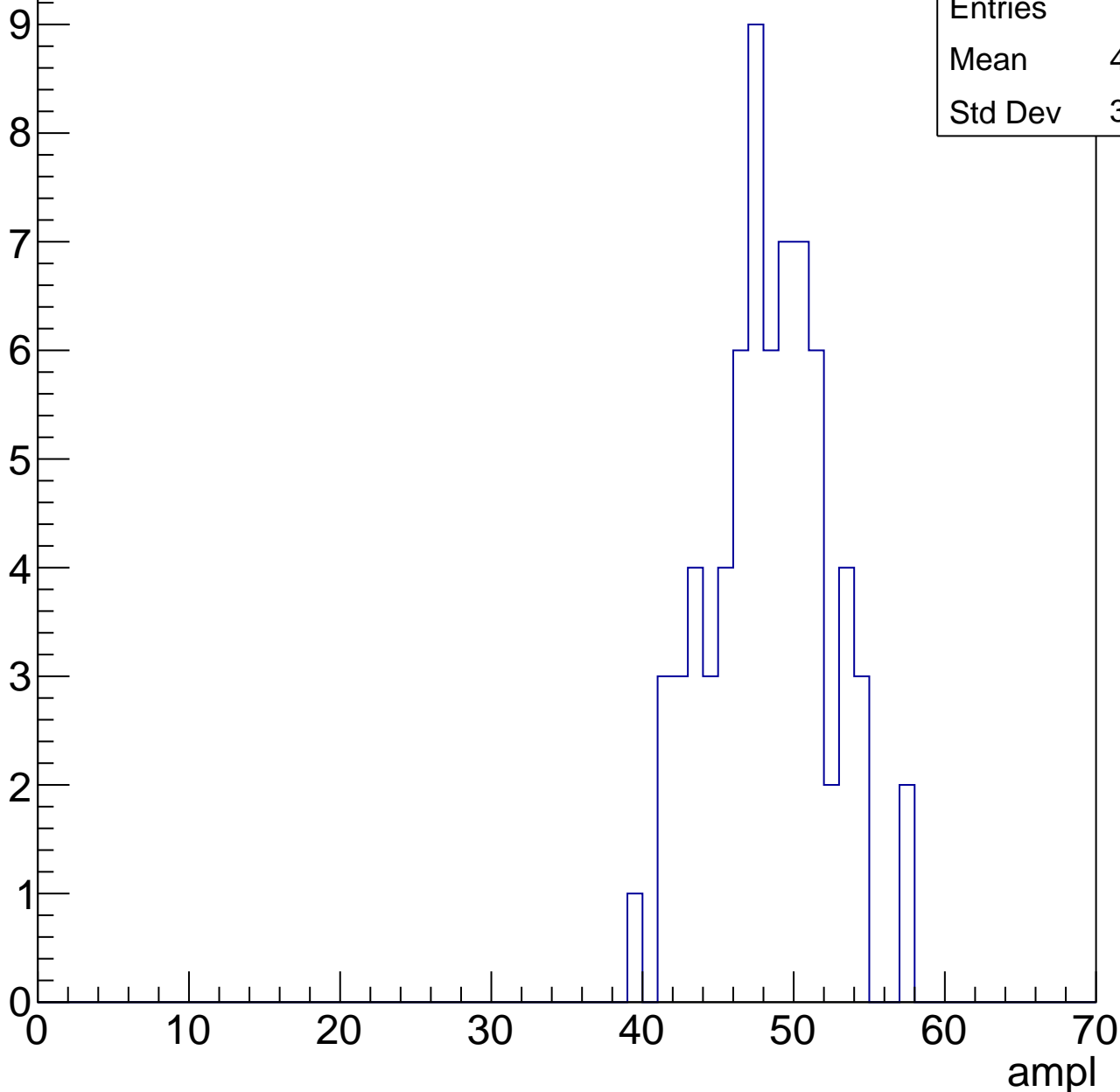


# B1L100S, U2-ch50, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	70
Mean	47.86
Std Dev	3.859

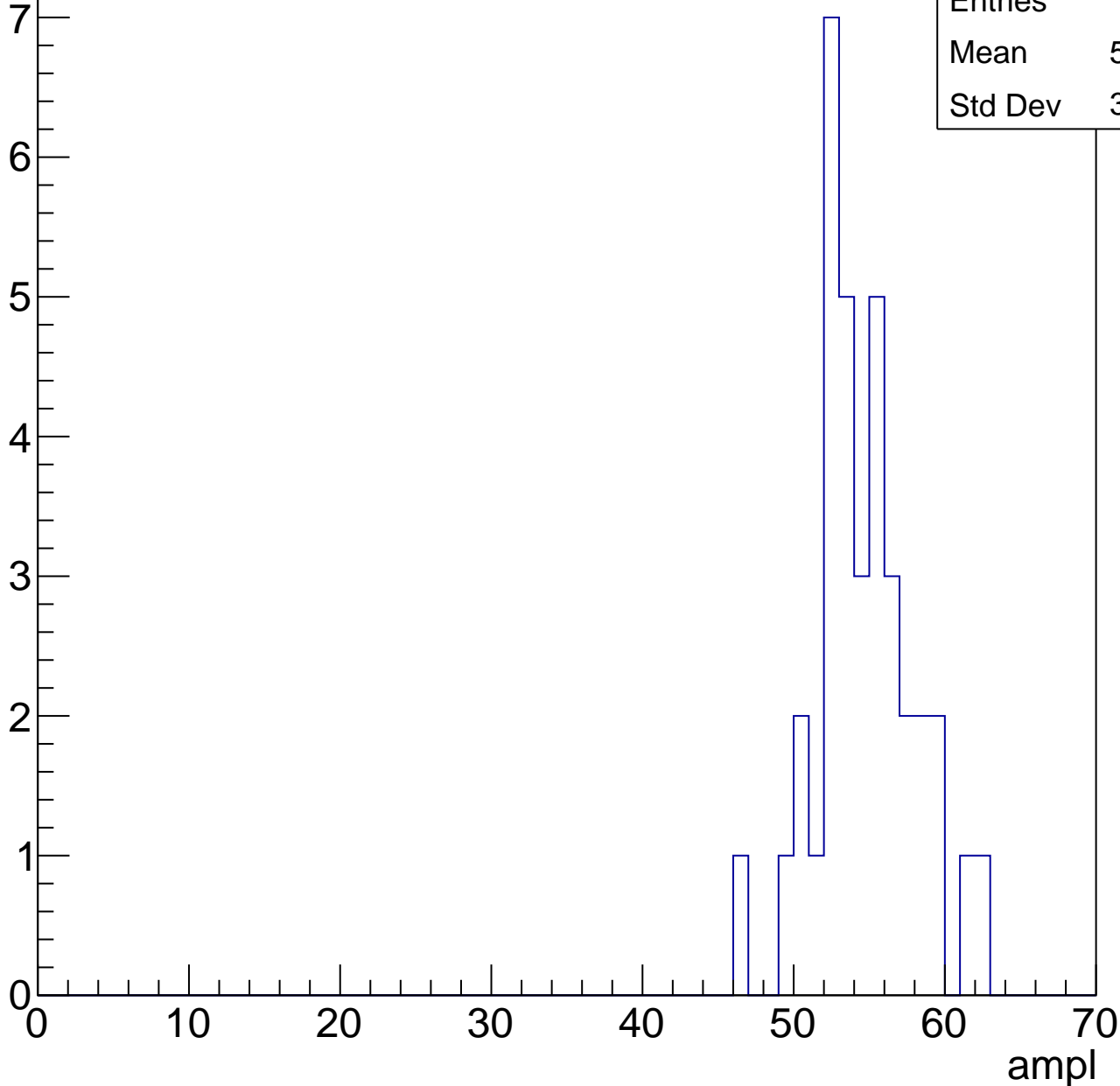


# B1L100S, U2-ch50, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

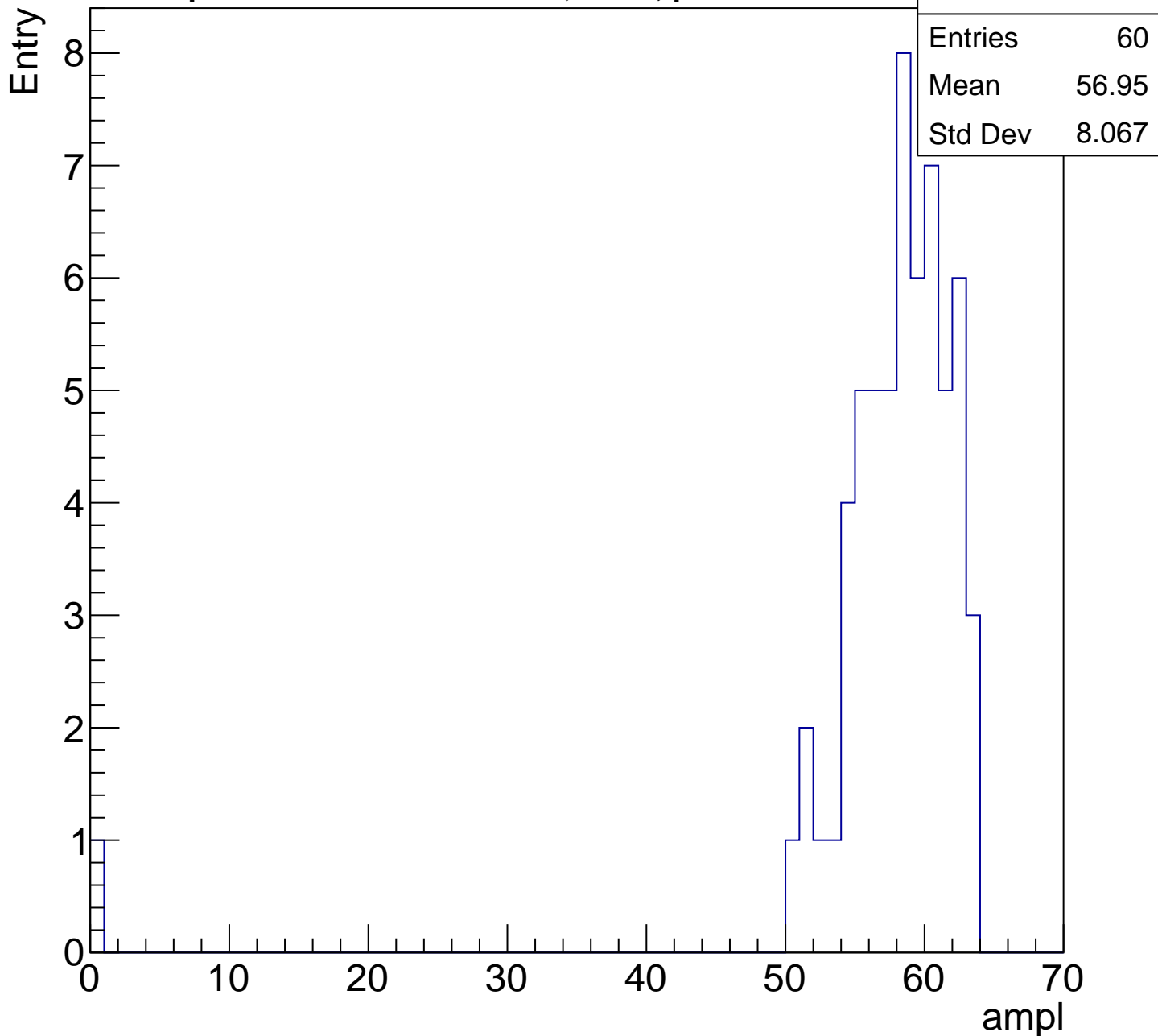
Entry

Entries	36
Mean	54.19
Std Dev	3.298



# B1L100S, U2-ch50, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

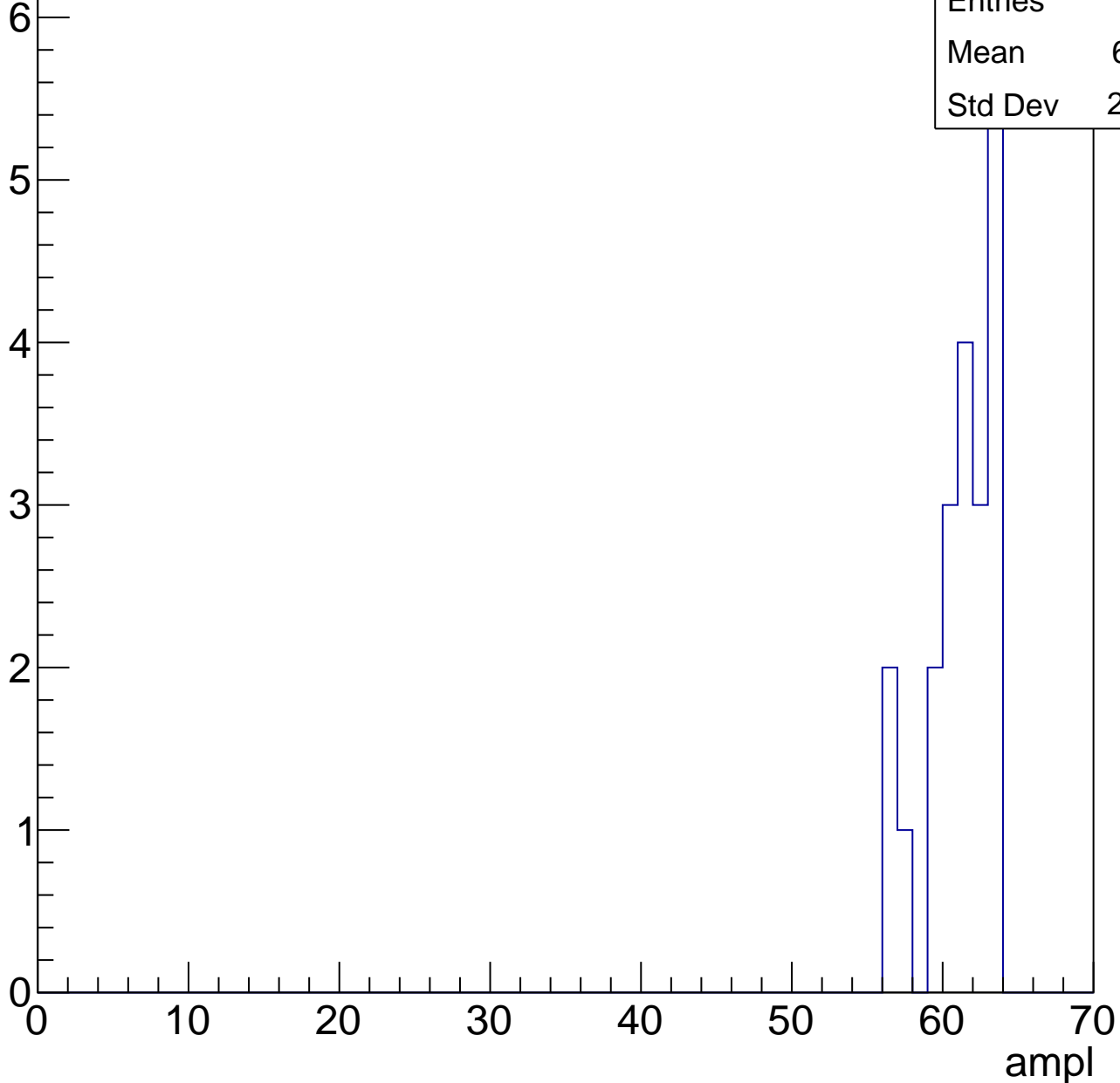


# B1L100S, U2-ch50, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	21
Mean	60.71
Std Dev	2.207





# B1L100S, U2-ch50, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



# B1L100S, U2-ch51, adc0

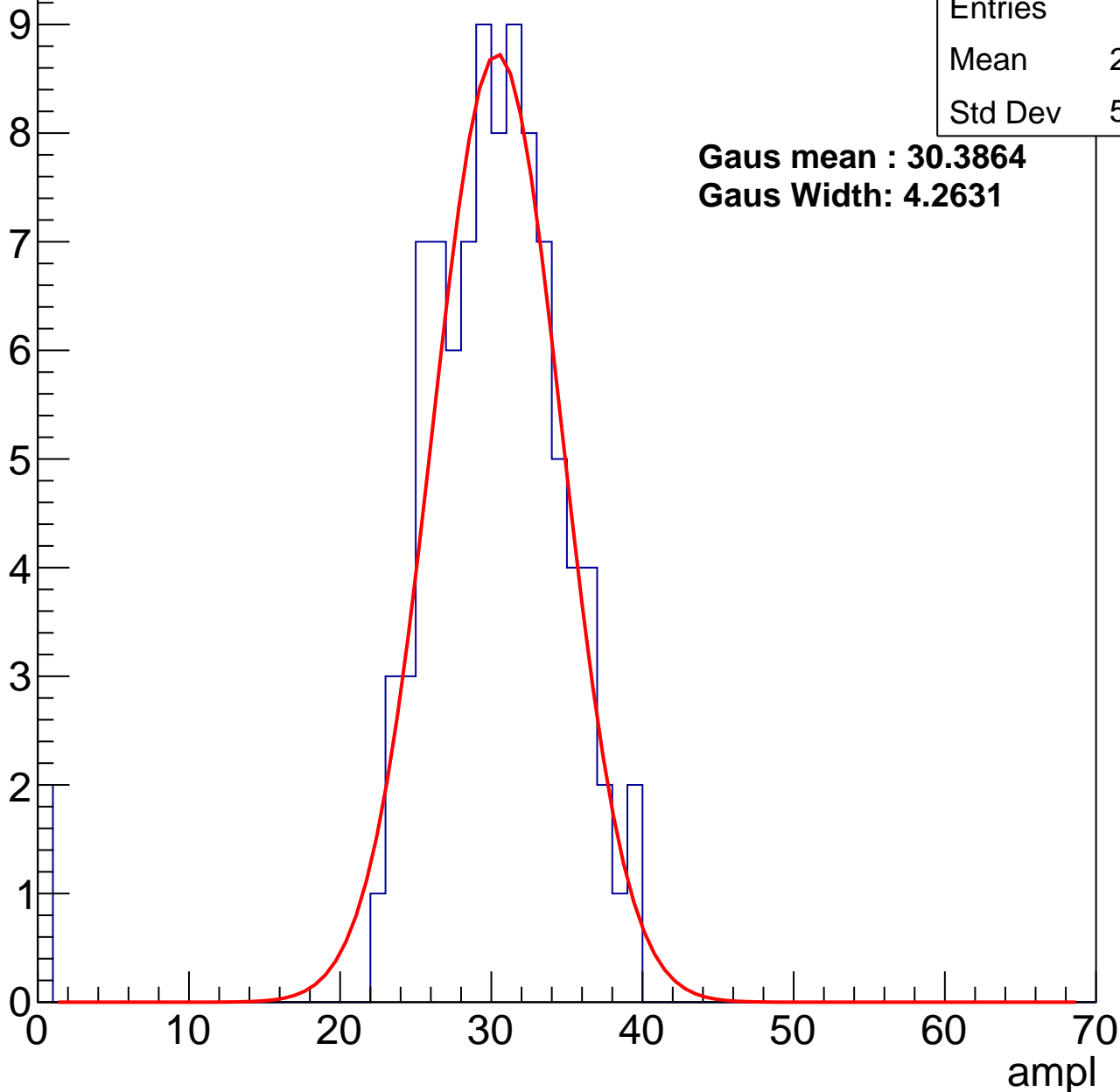
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	95
Mean	29.36
Std Dev	5.813

**Gaus mean : 30.3864**

**Gaus Width: 4.2631**



# B1L100S, U2-ch51, adc1

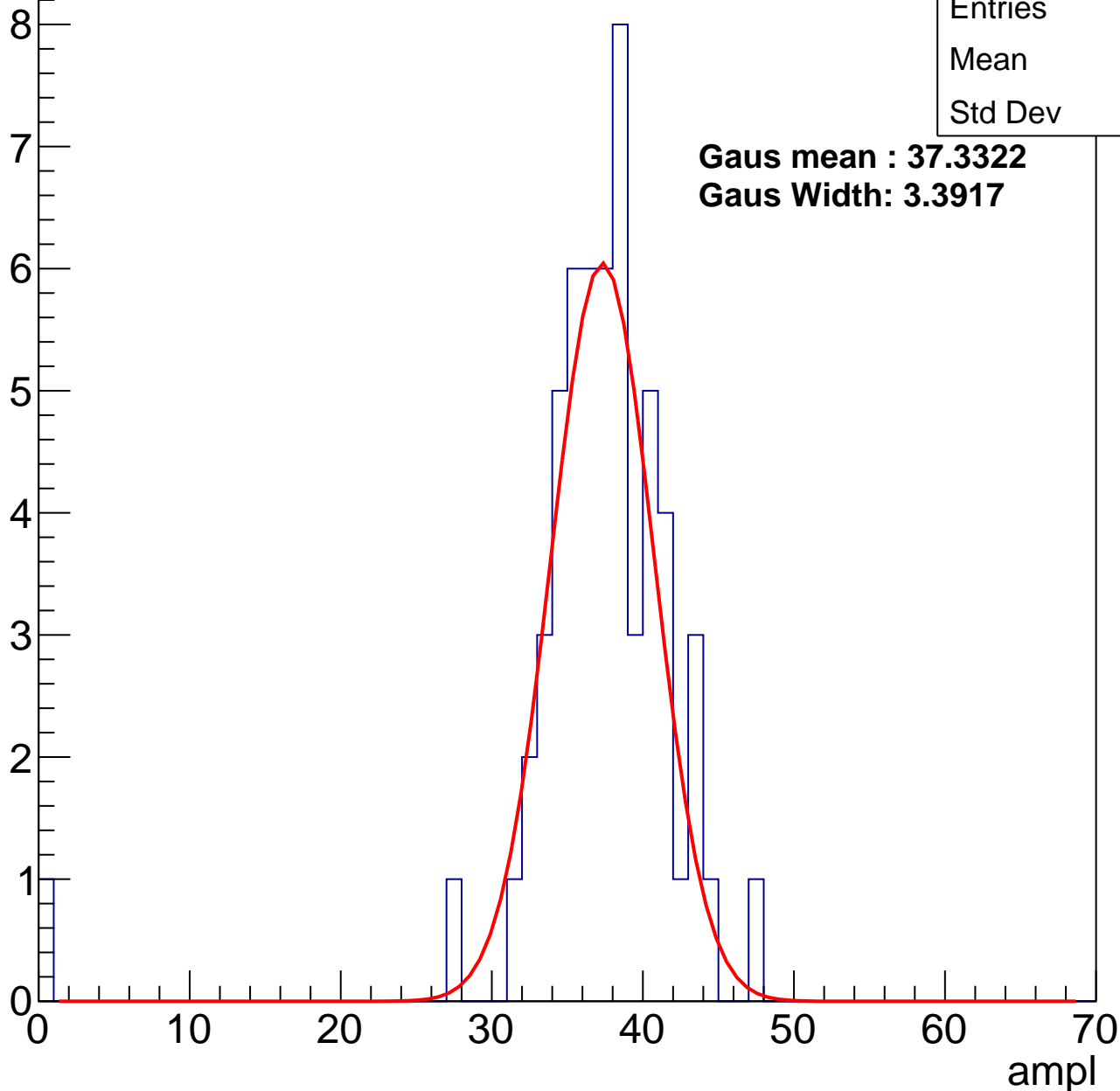
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	57
Mean	36.6
Std Dev	6.04

**Gaus mean : 37.3322**

**Gaus Width: 3.3917**



# B1L100S, U2-ch51, adc2

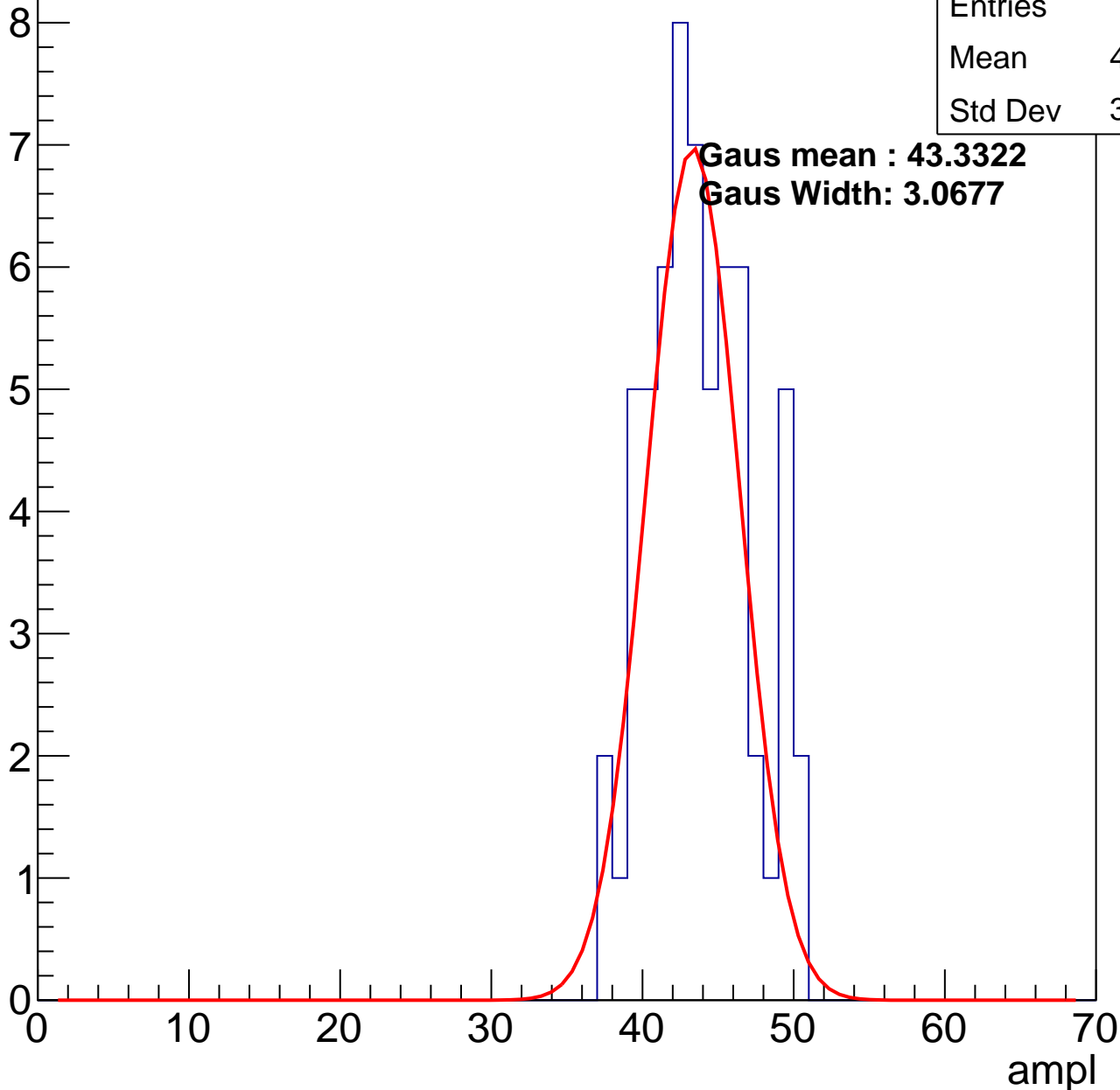
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	61
Mean	43.33
Std Dev	3.303

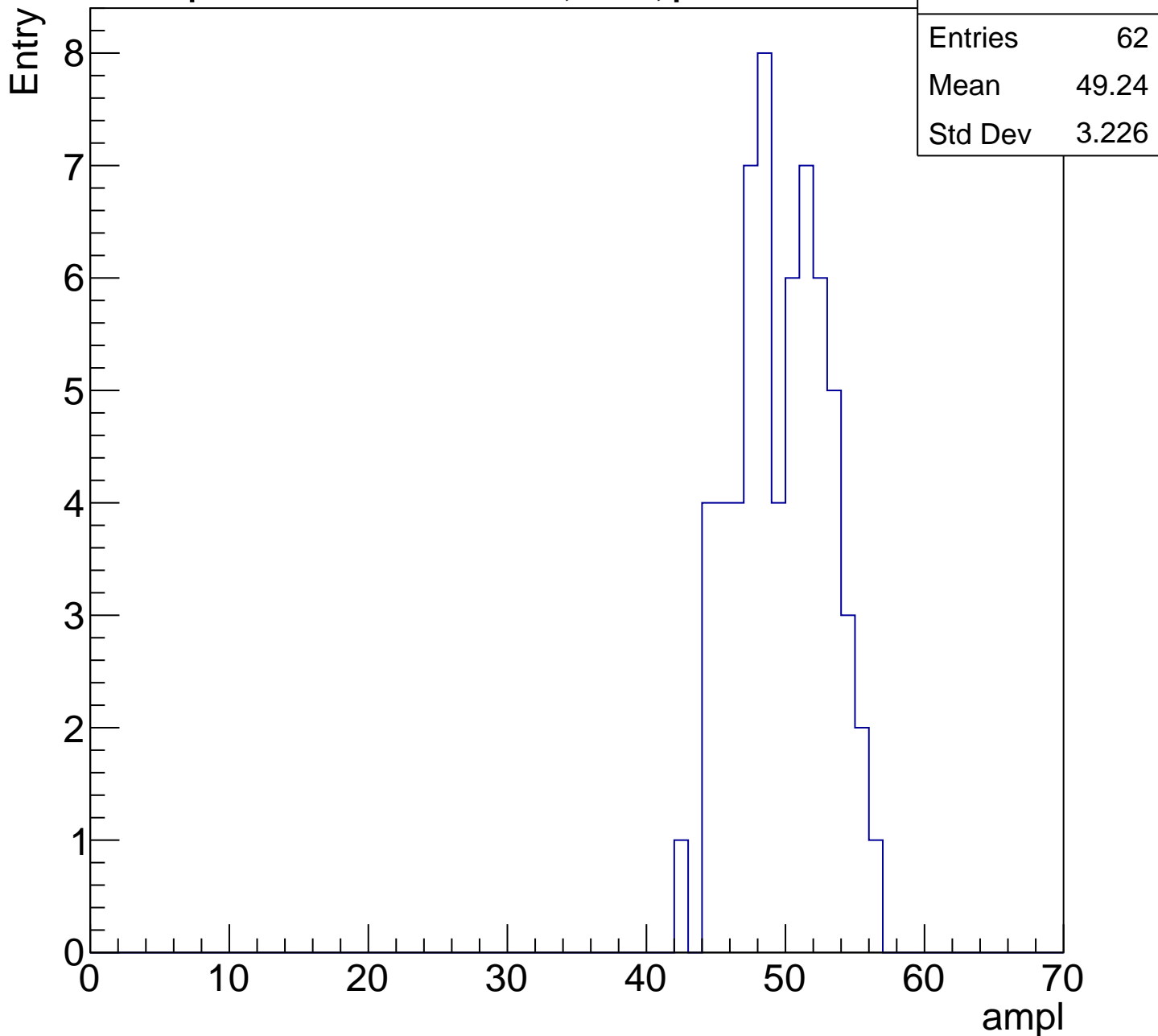
**Gaus mean : 43.3322**

**Gaus Width: 3.0677**



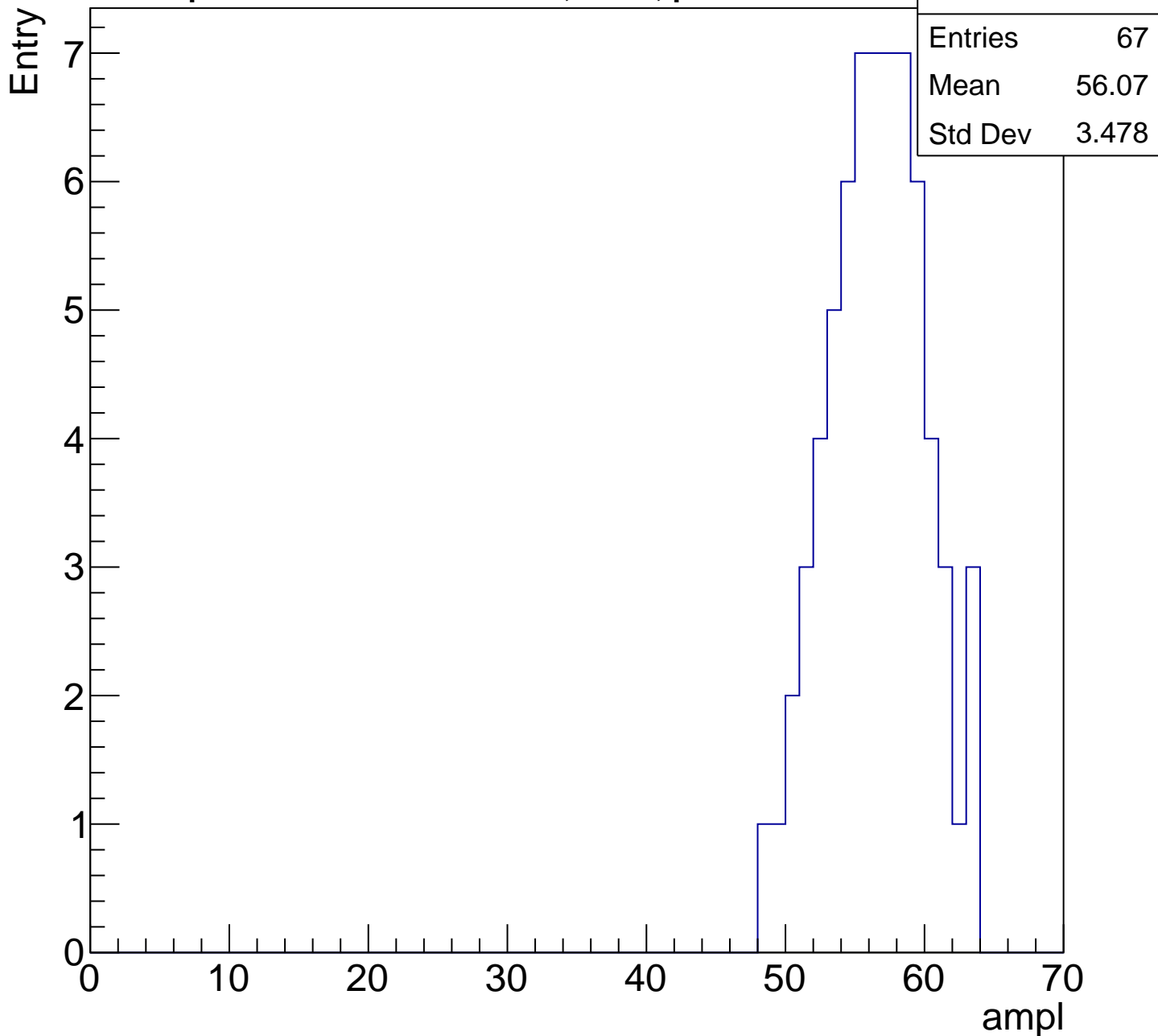
# B1L100S, U2-ch51, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2



# B1L100S, U2-ch51, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

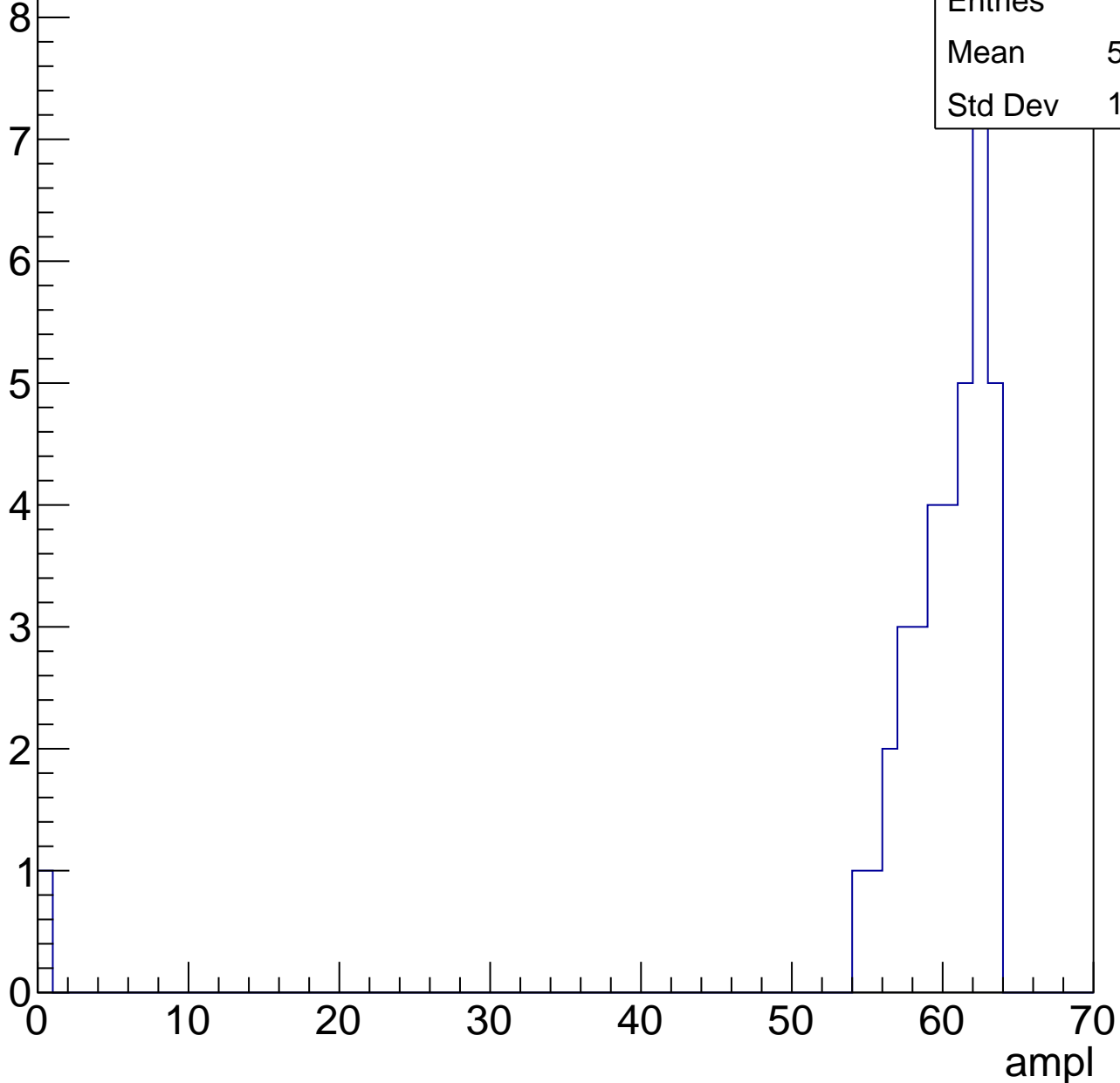


# B1L100S, U2-ch51, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	37
Mean	58.32
Std Dev	10.02



# B1L100S, U2-ch51, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

0

10

20

30

40

50

60

70

ampl

Entries

7

Mean

61.43

Std Dev

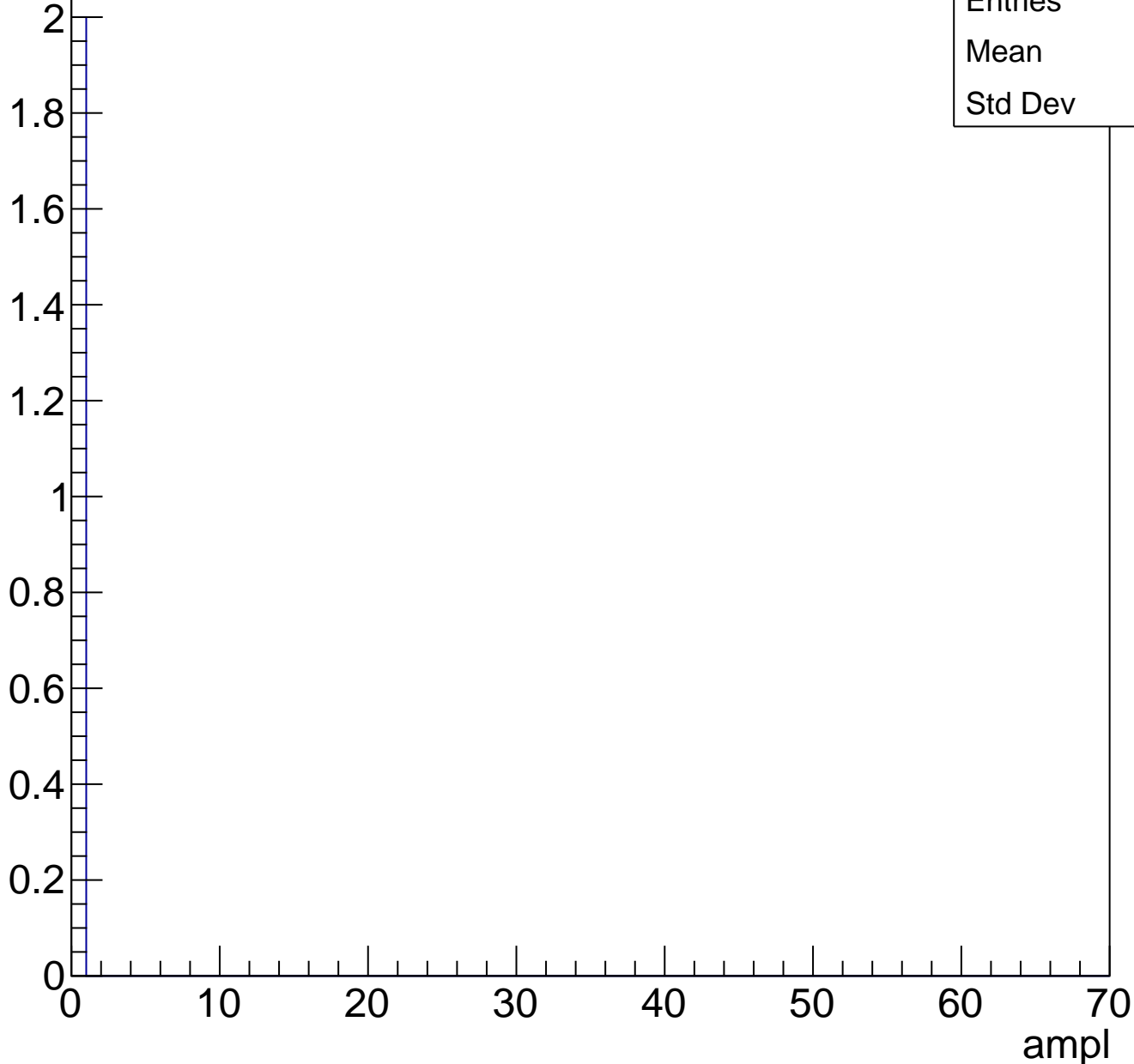
1.178



# B1L100S, U2-ch51, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L100S, U2-ch52, adc0

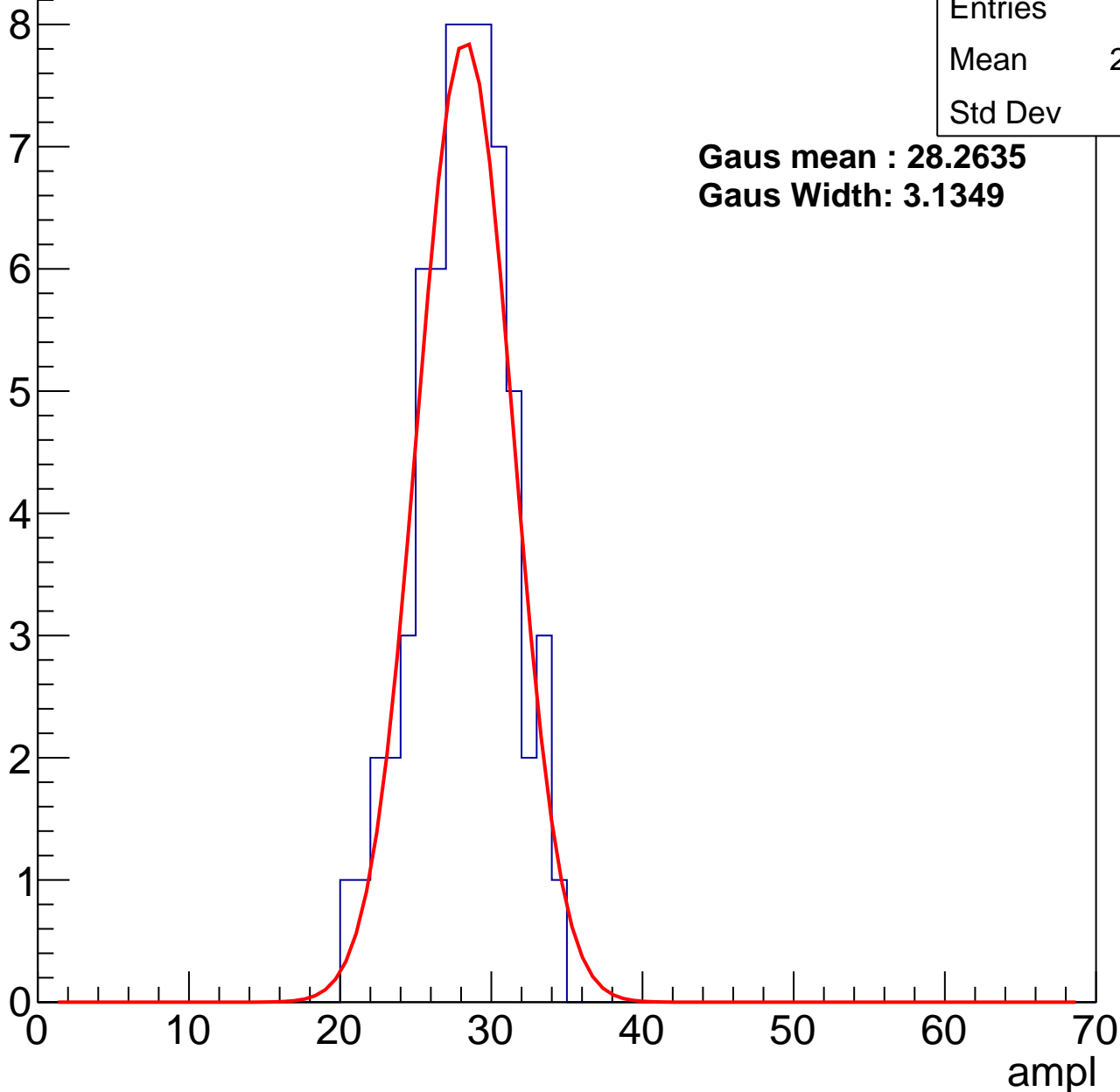
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	63
Mean	27.67
Std Dev	3.05

**Gaus mean : 28.2635**

**Gaus Width: 3.1349**



# B1L100S, U2-ch52, adc1

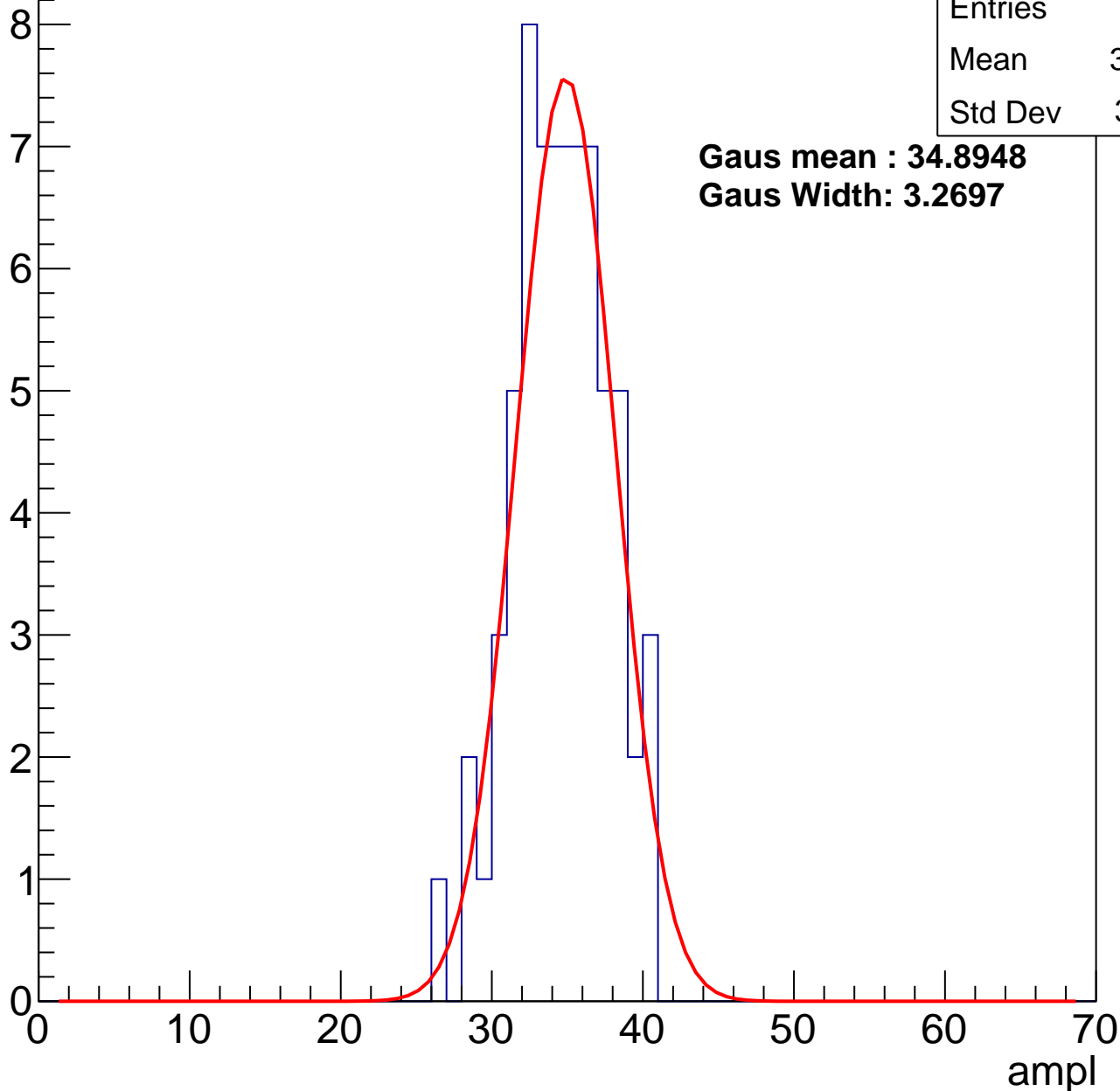
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	63
Mean	34.14
Std Dev	3.111

**Gaus mean : 34.8948**

**Gaus Width: 3.2697**



# B1L100S, U2-ch52, adc2

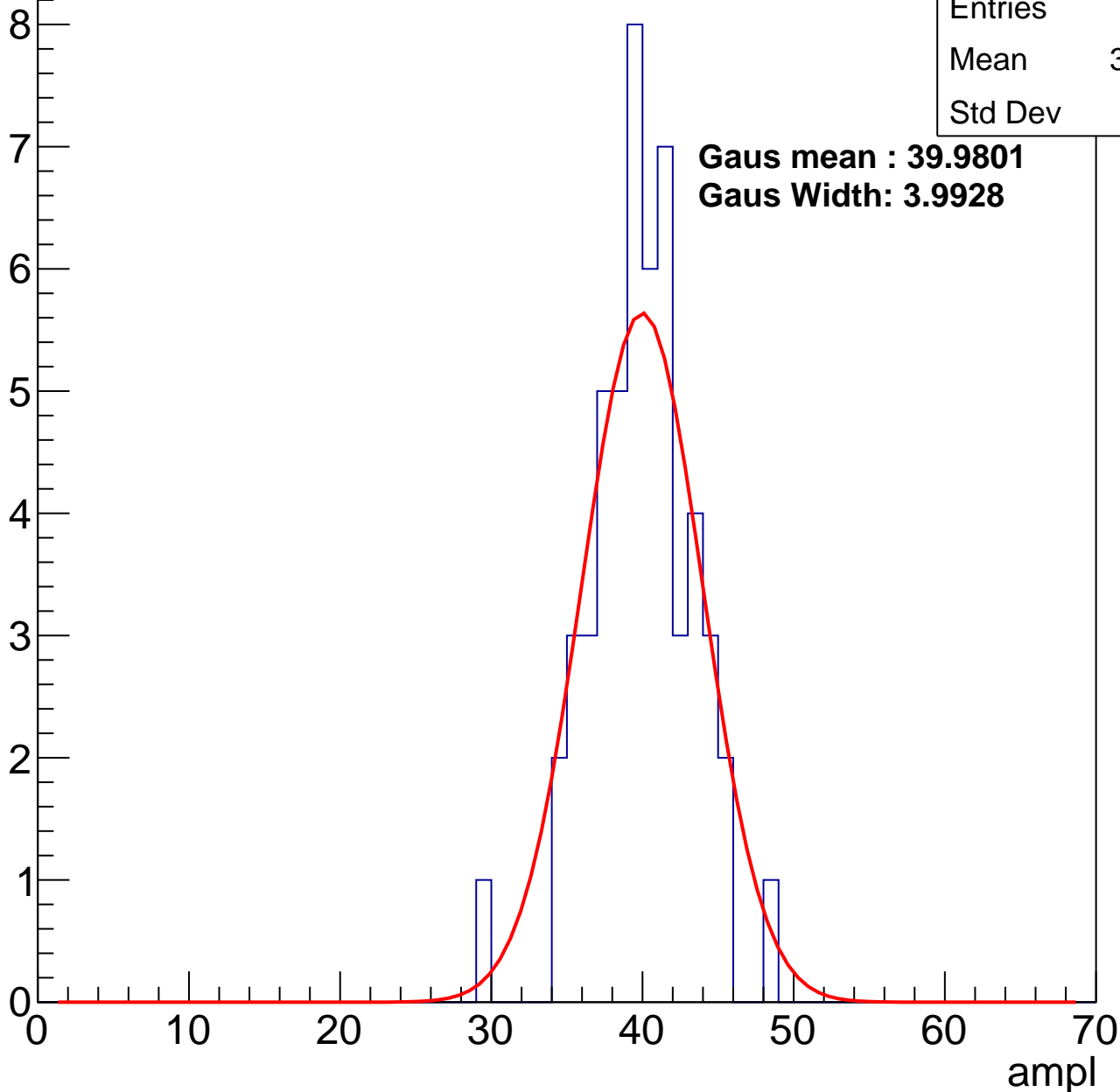
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	53
Mean	39.47
Std Dev	3.34

**Gaus mean : 39.9801**

**Gaus Width: 3.9928**

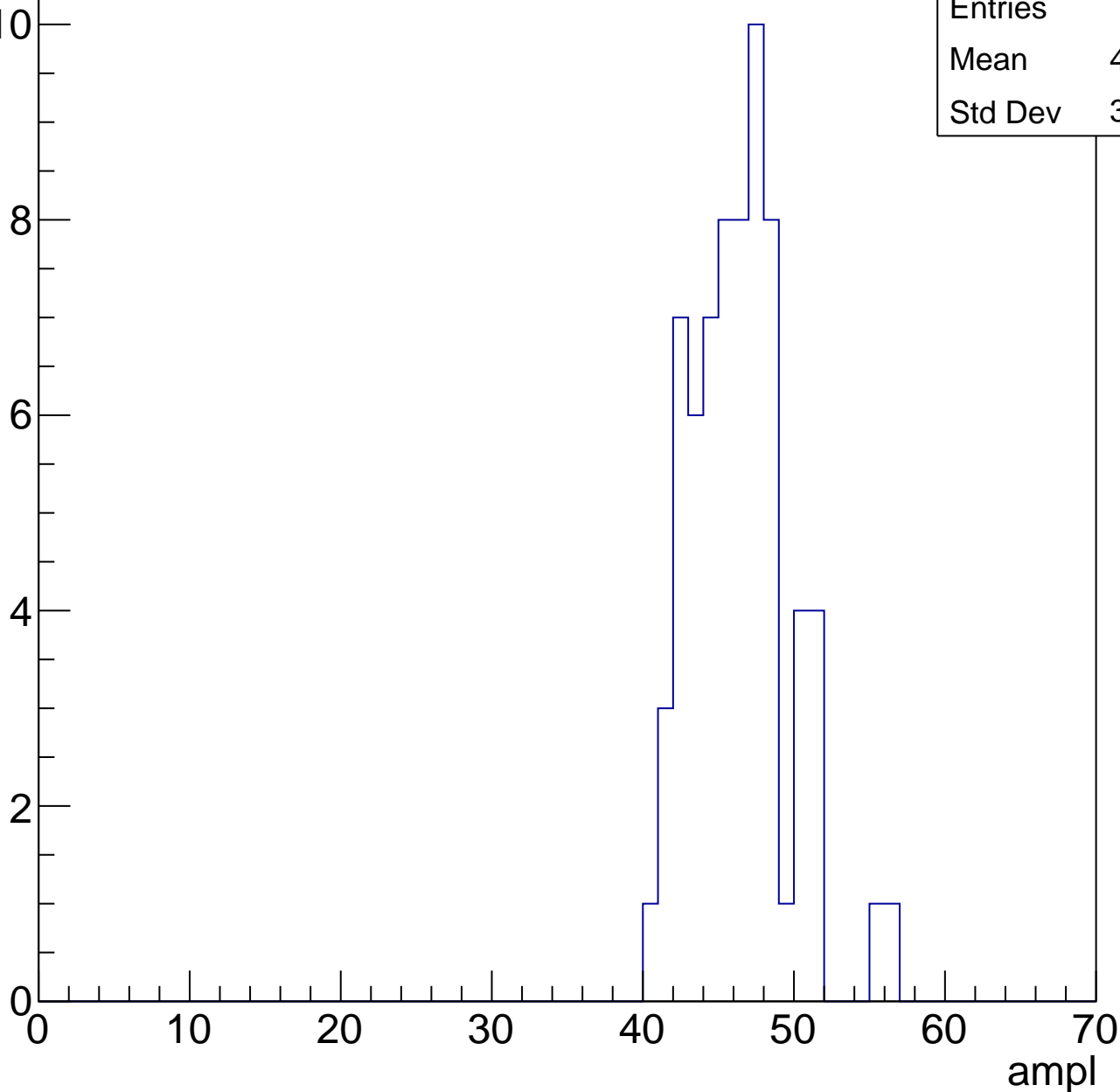


# B1L100S, U2-ch52, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

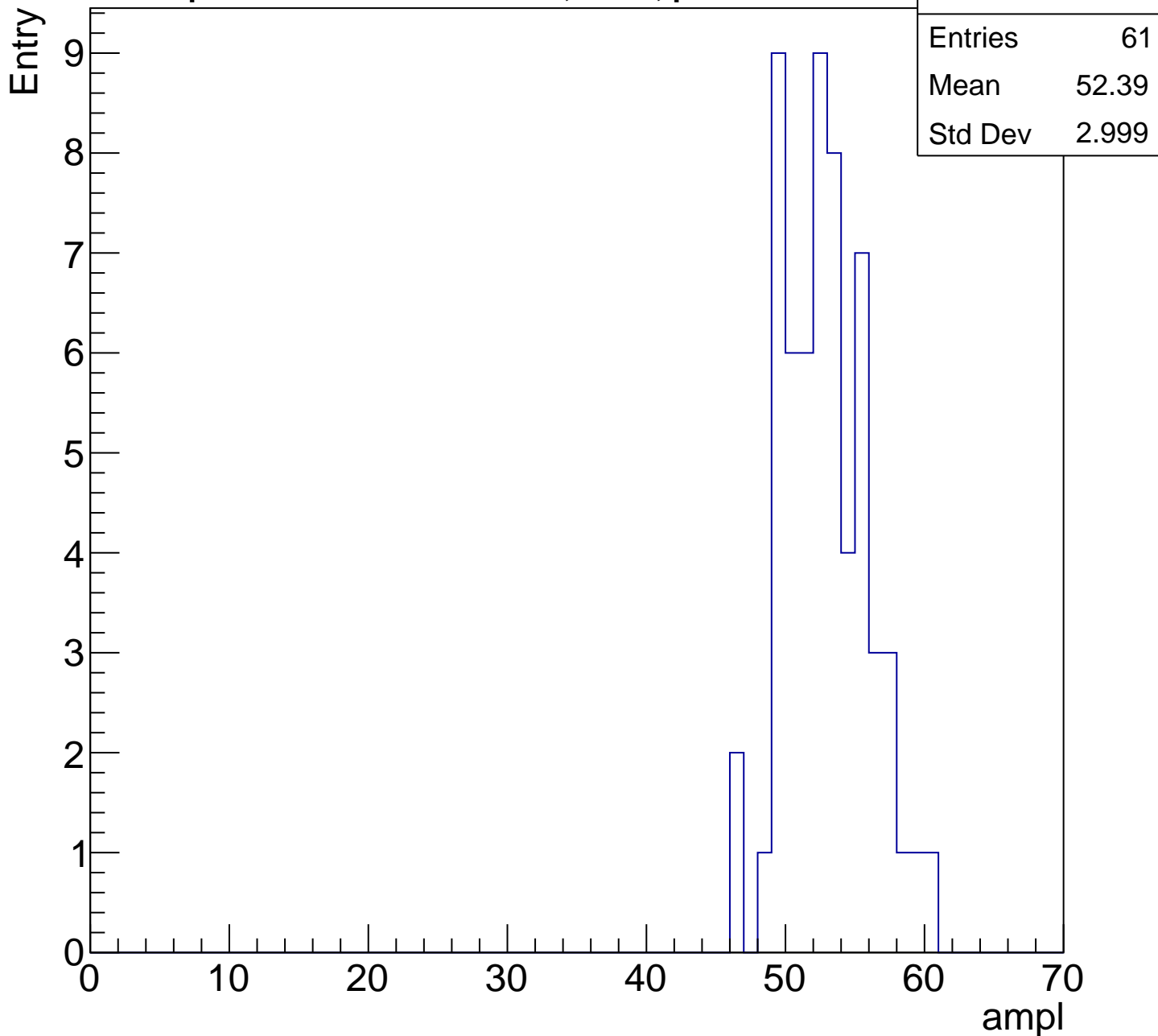
Entry

Entries	69
Mean	45.93
Std Dev	3.205



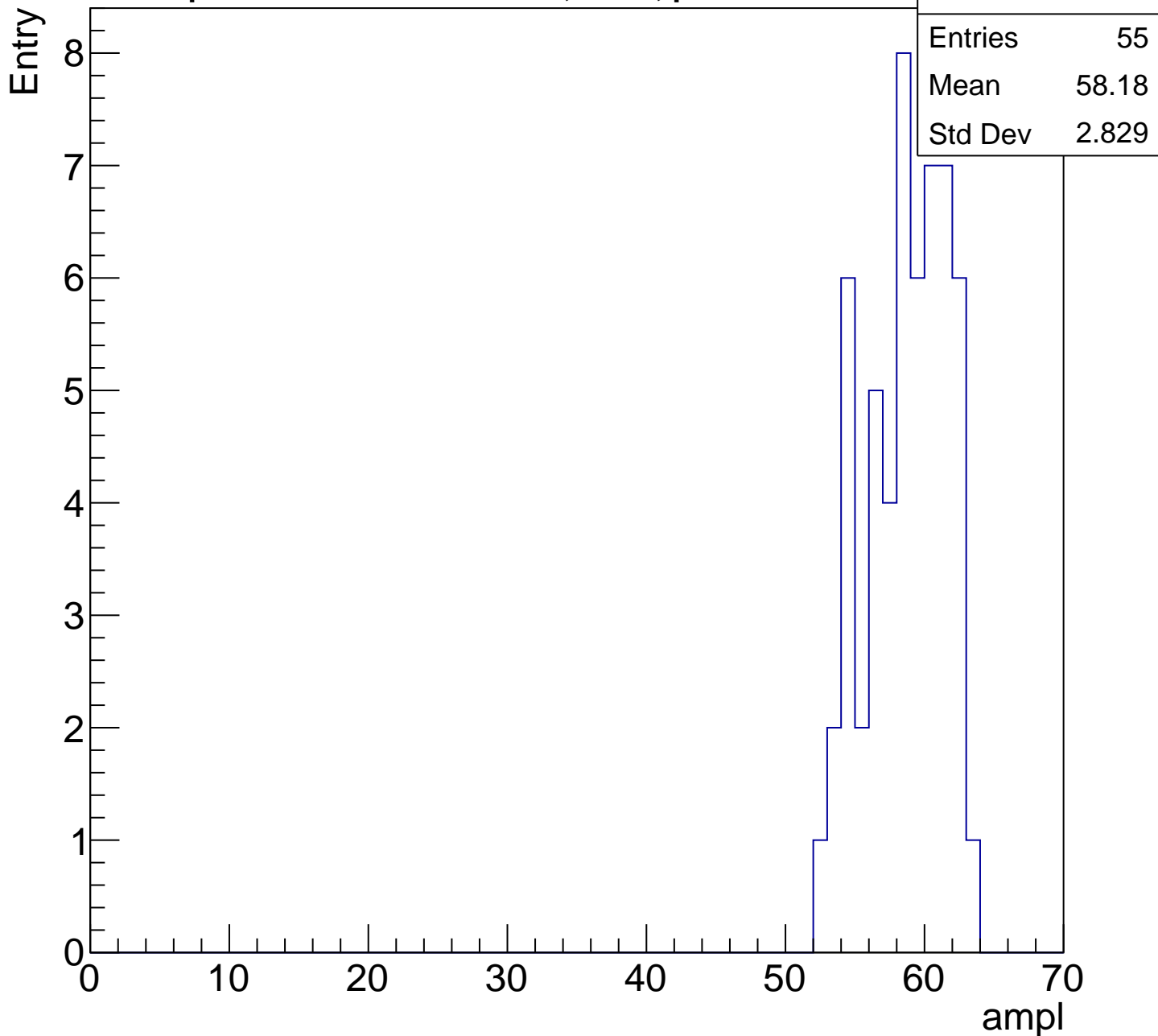
# B1L100S, U2-ch52, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2



# B1L100S, U2-ch52, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

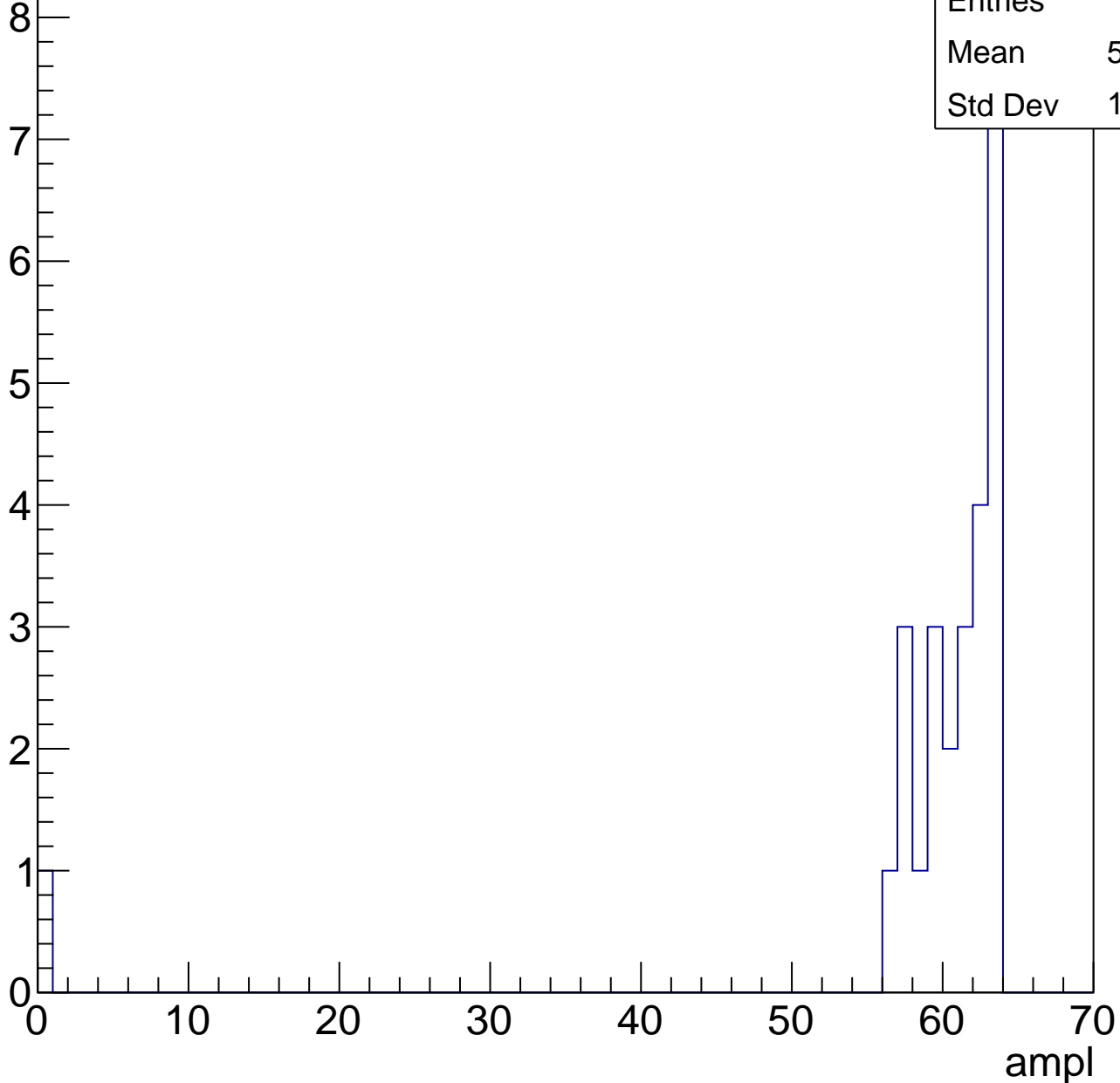


# B1L100S, U2-ch52, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	26
Mean	58.35
Std Dev	11.88





# B1L100S, U2-ch52, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



# B1L100S, U2-ch53, adc0

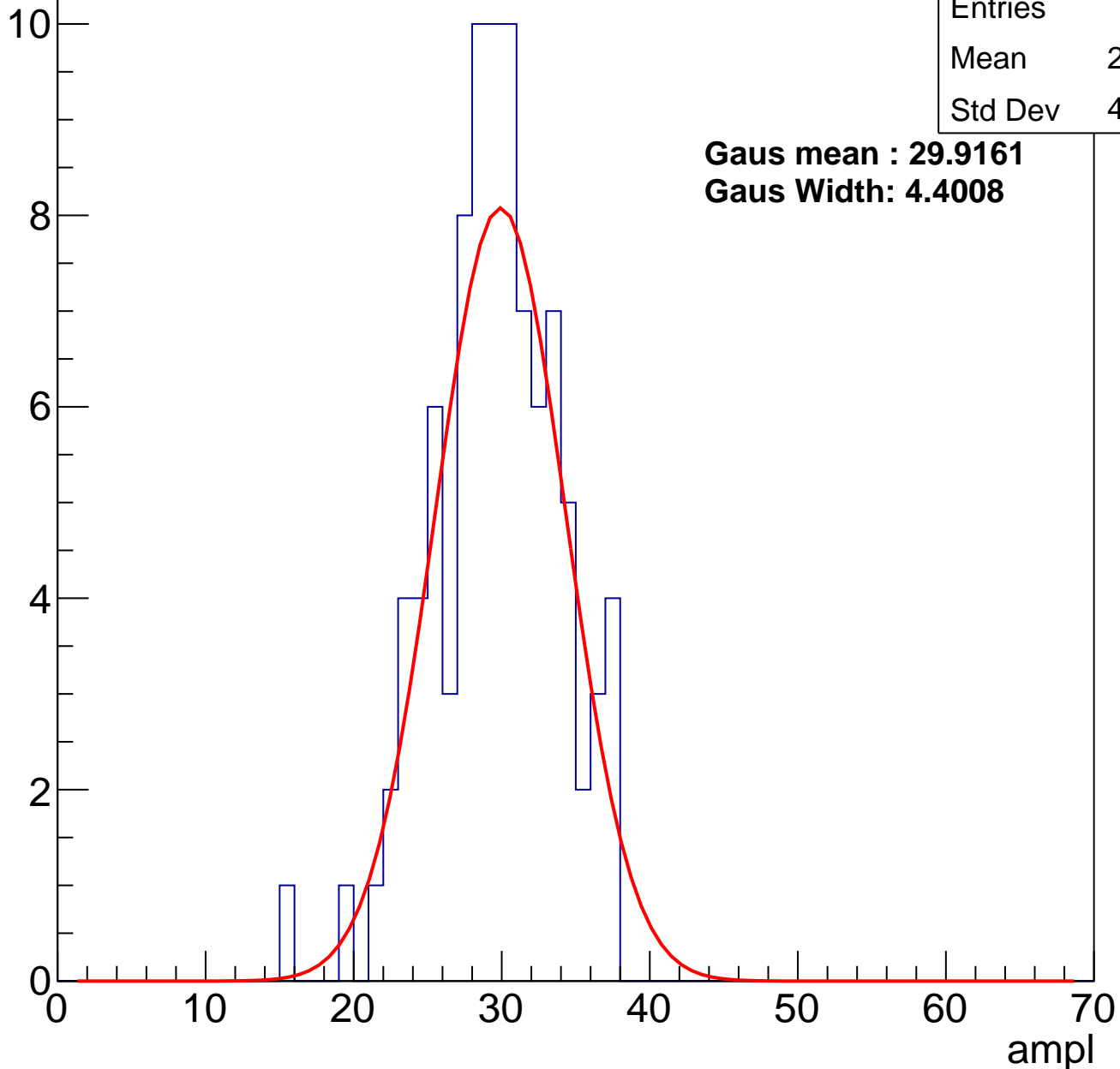
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	94
Mean	29.12
Std Dev	4.215

**Gaus mean : 29.9161**

**Gaus Width: 4.4008**

Entry



# B1L100S, U2-ch53, adc1

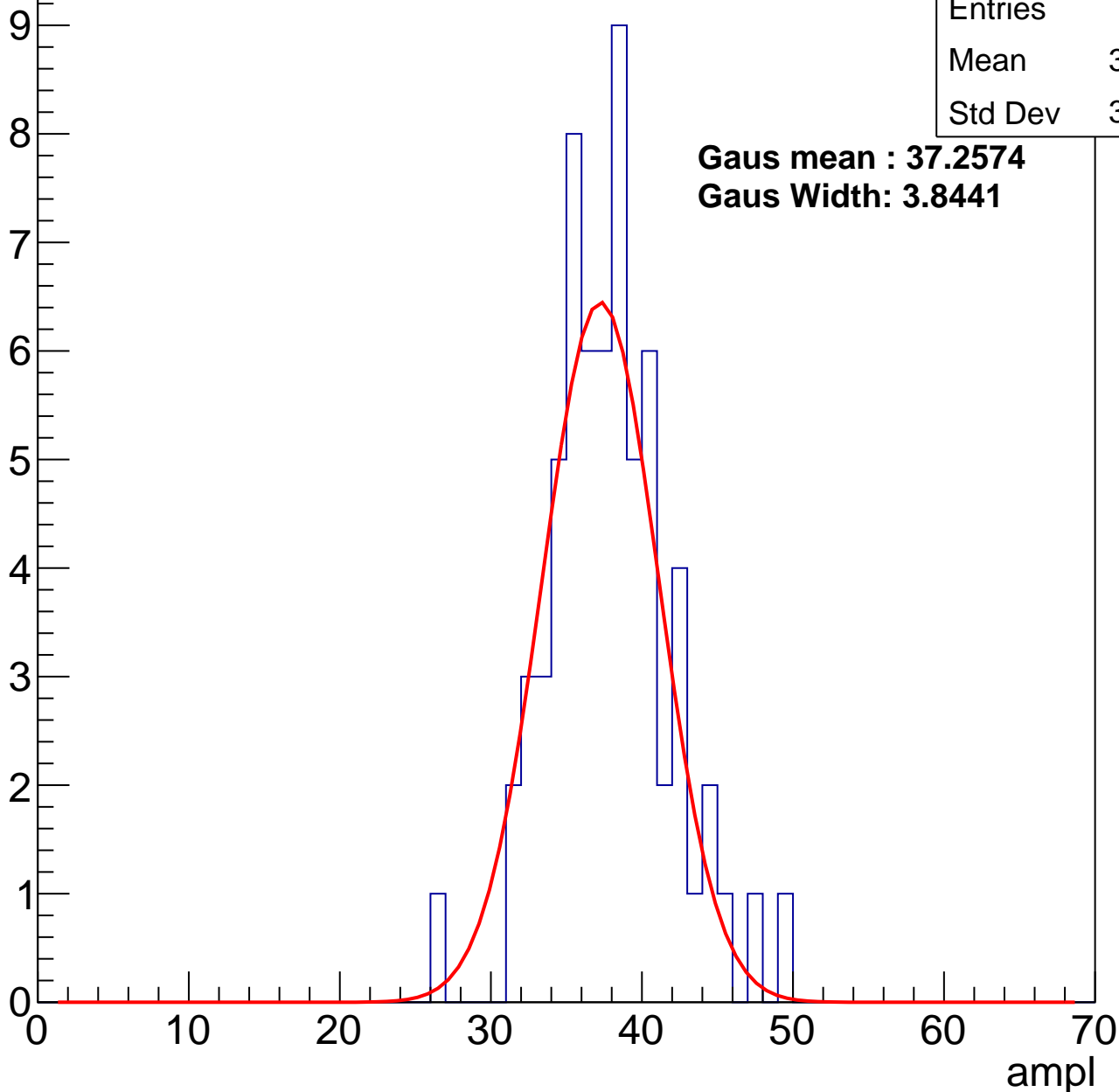
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	66
Mean	37.42
Std Dev	3.977

**Gaus mean : 37.2574**

**Gaus Width: 3.8441**



# B1L100S, U2-ch53, adc2

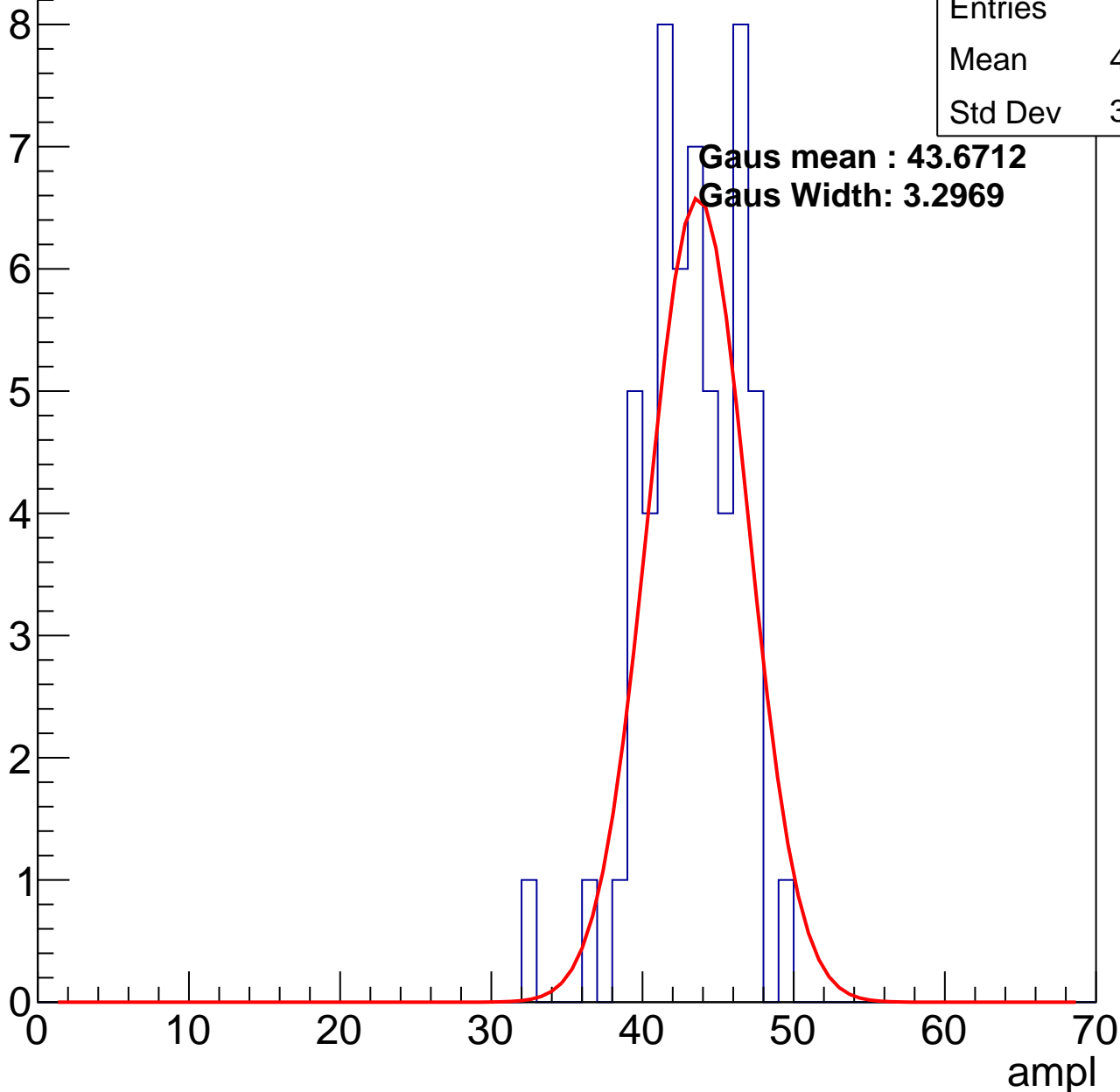
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	56
Mean	42.75
Std Dev	3.147

**Gaus mean : 43.6712**

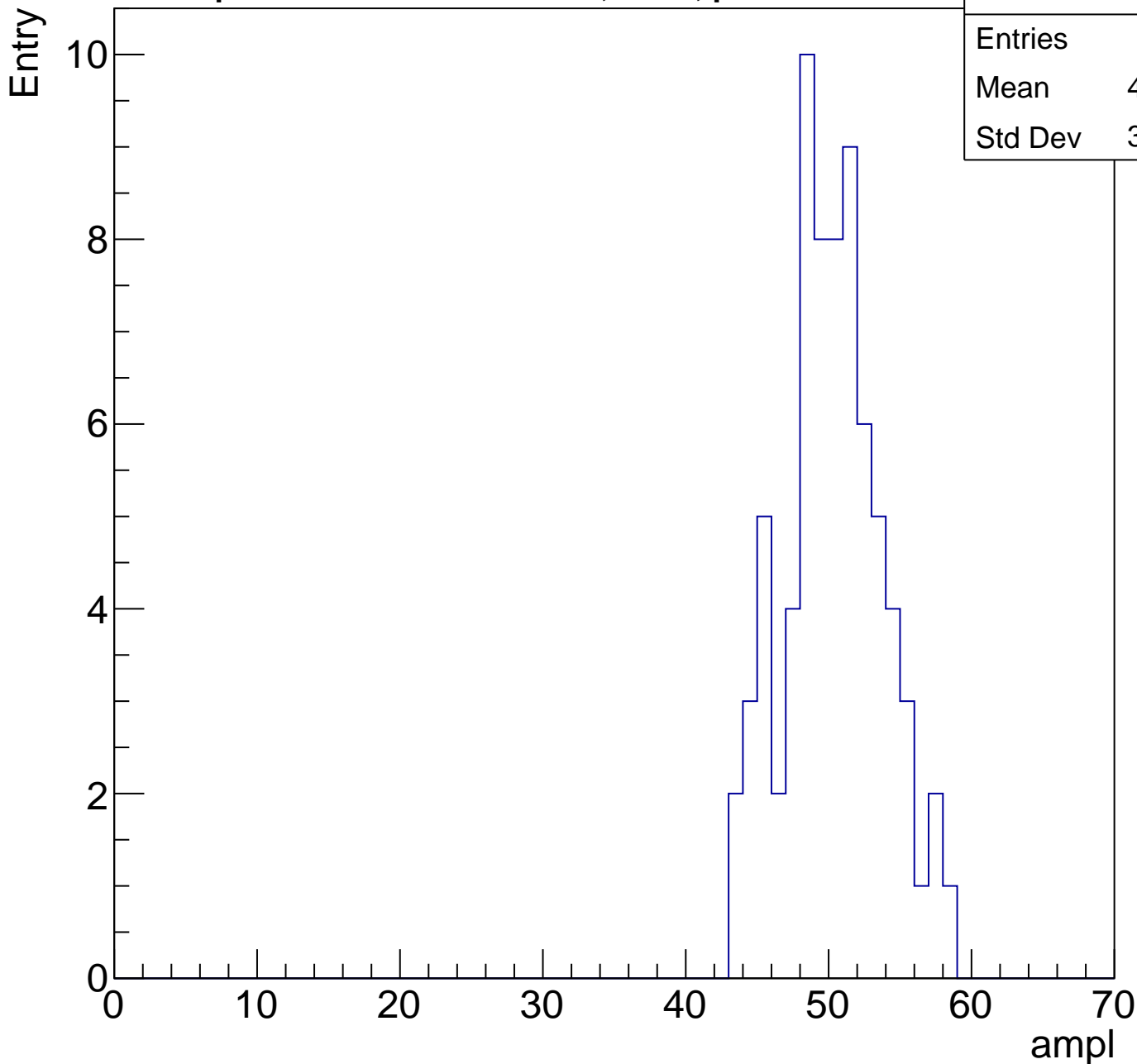
**Gaus Width: 3.2969**



# B1L100S, U2-ch53, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	73
Mean	49.86
Std Dev	3.434

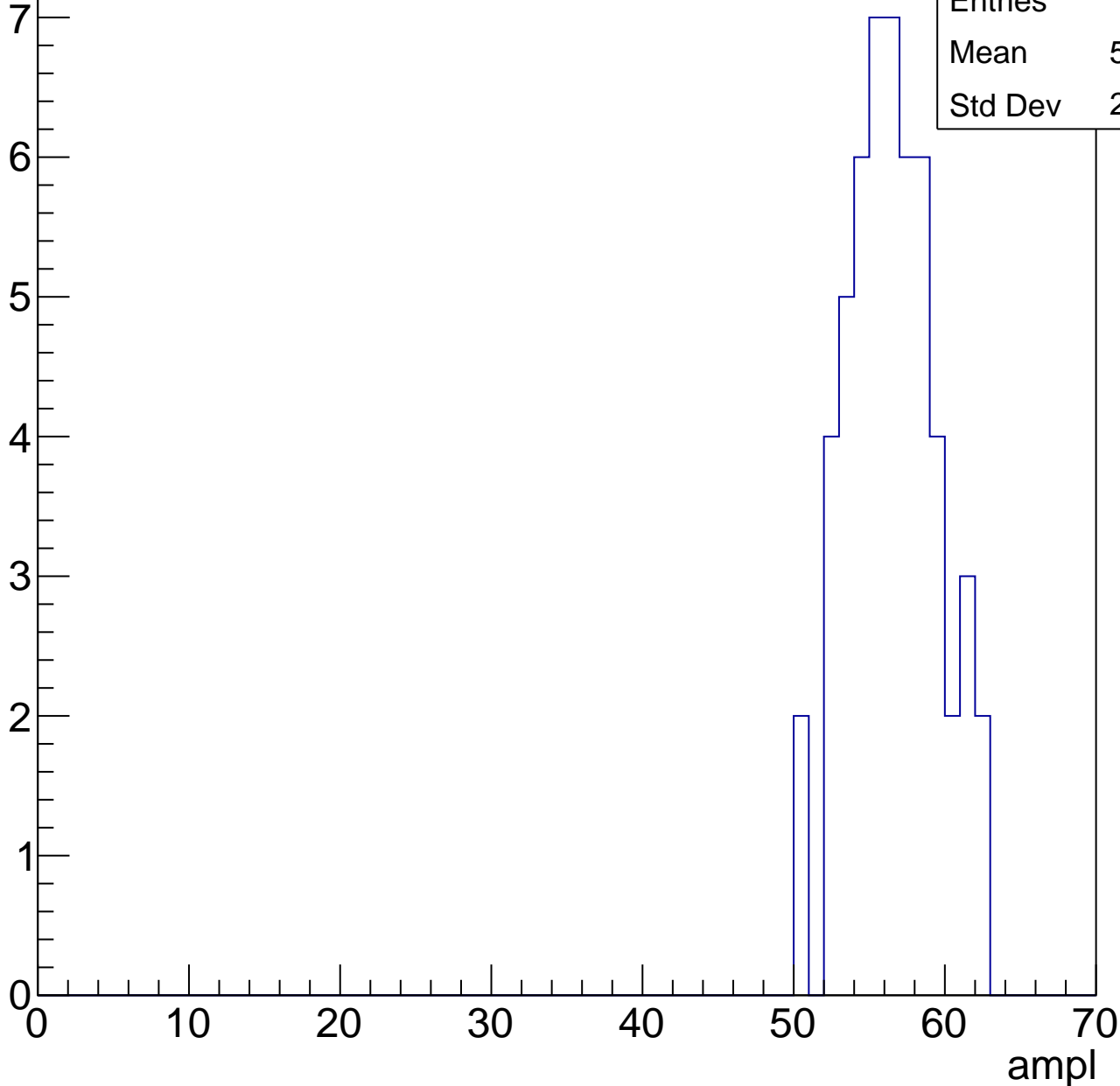


# B1L100S, U2-ch53, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	54
Mean	56.06
Std Dev	2.909



# B1L100S, U2-ch53, adc5

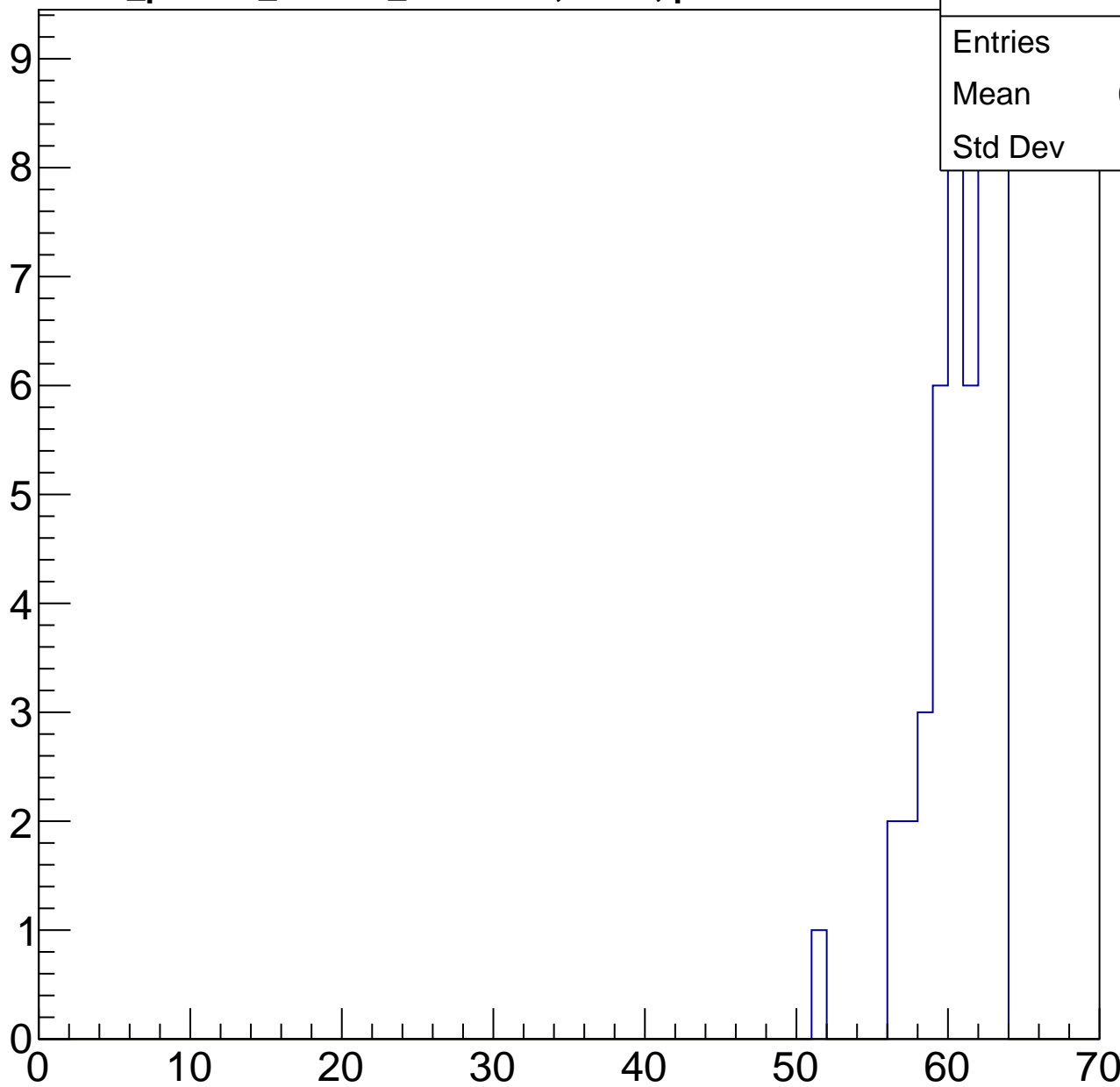
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	45
Mean	60.31
Std Dev	2.42

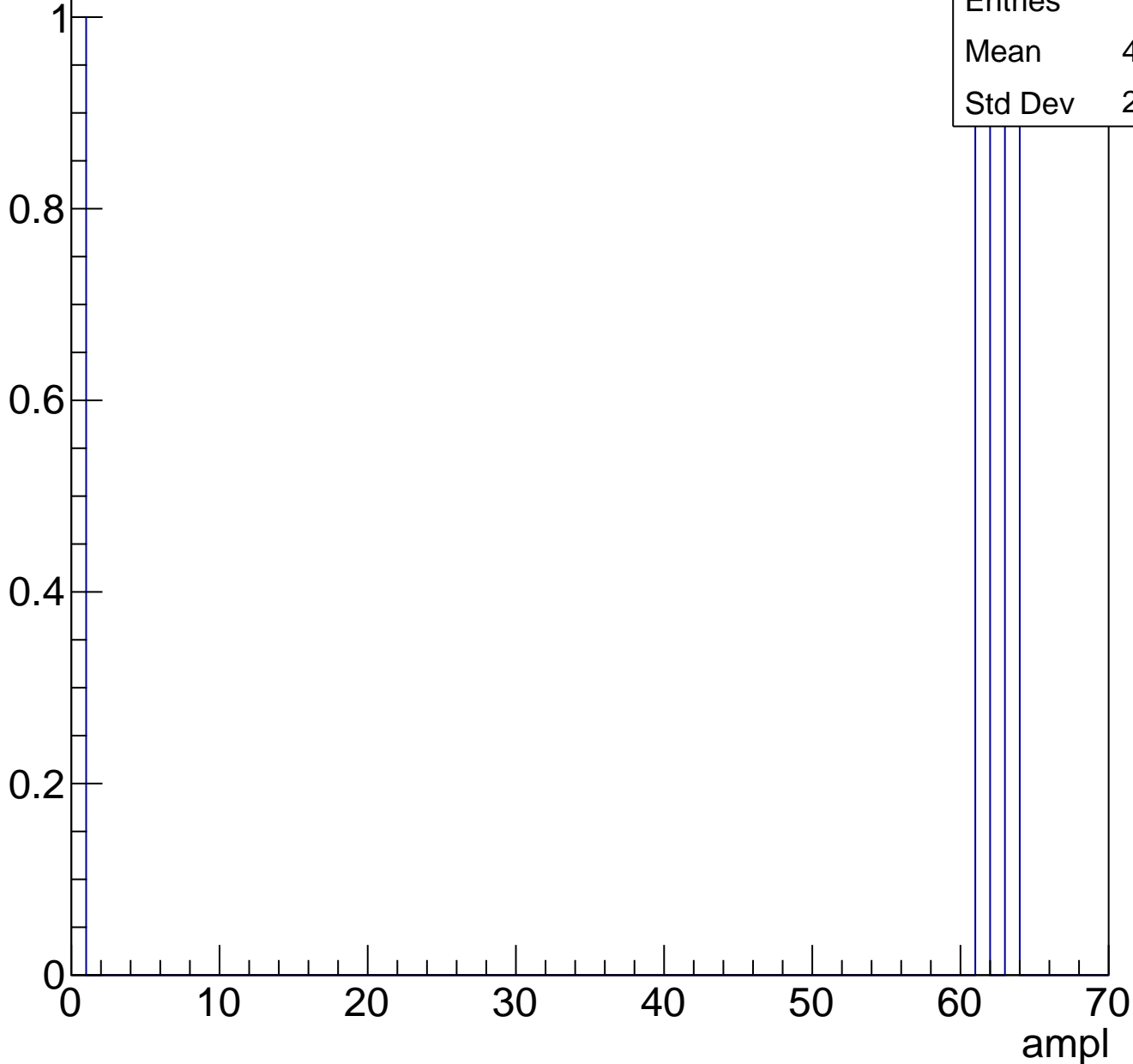
ampl



# B1L100S, U2-ch53, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry





# B1L100S, U2-ch53, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L100S, U2-ch54, adc0

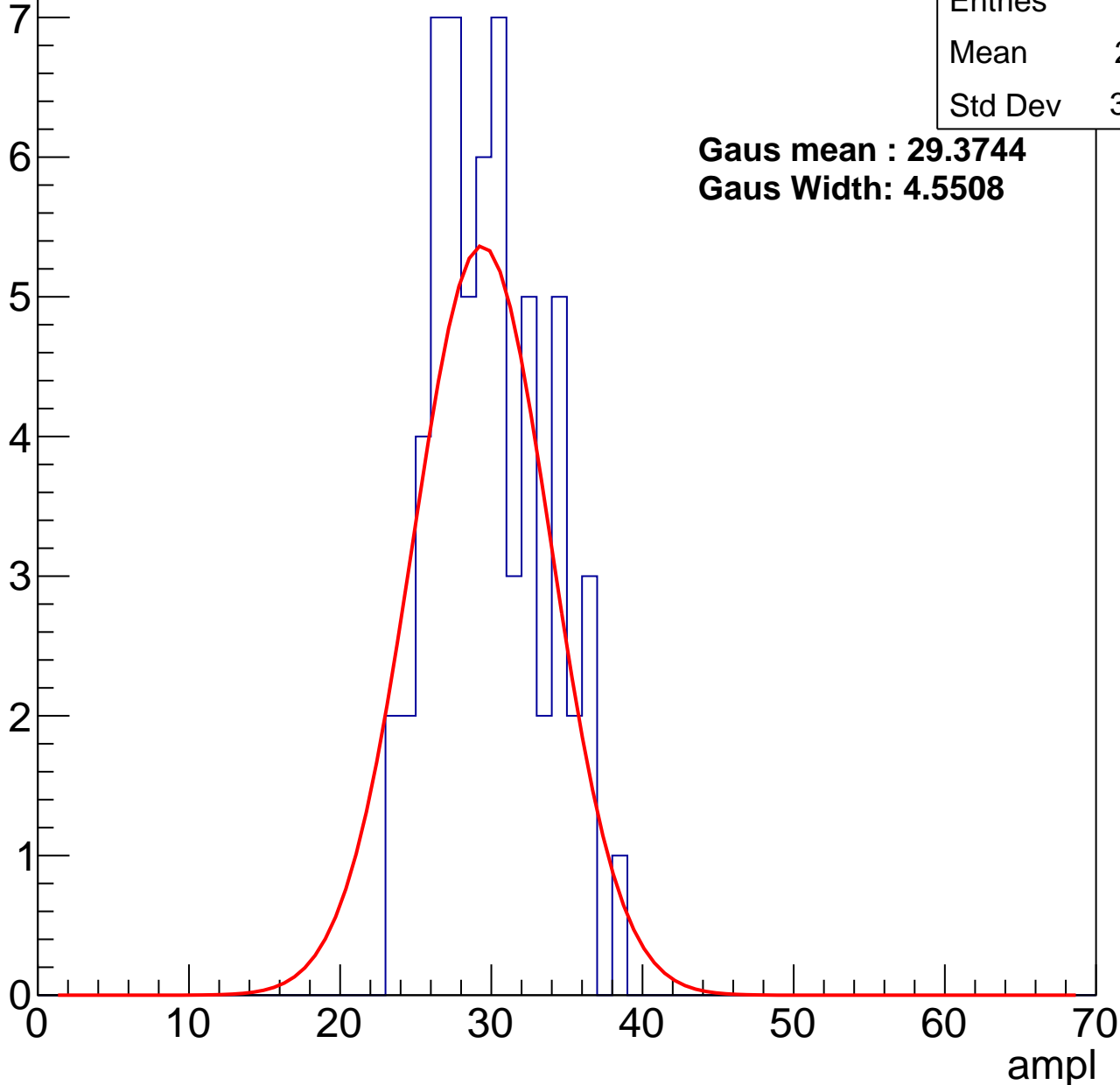
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	61
Mean	29.41
Std Dev	3.605

**Gaus mean : 29.3744**

**Gaus Width: 4.5508**



# B1L100S, U2-ch54, adc1

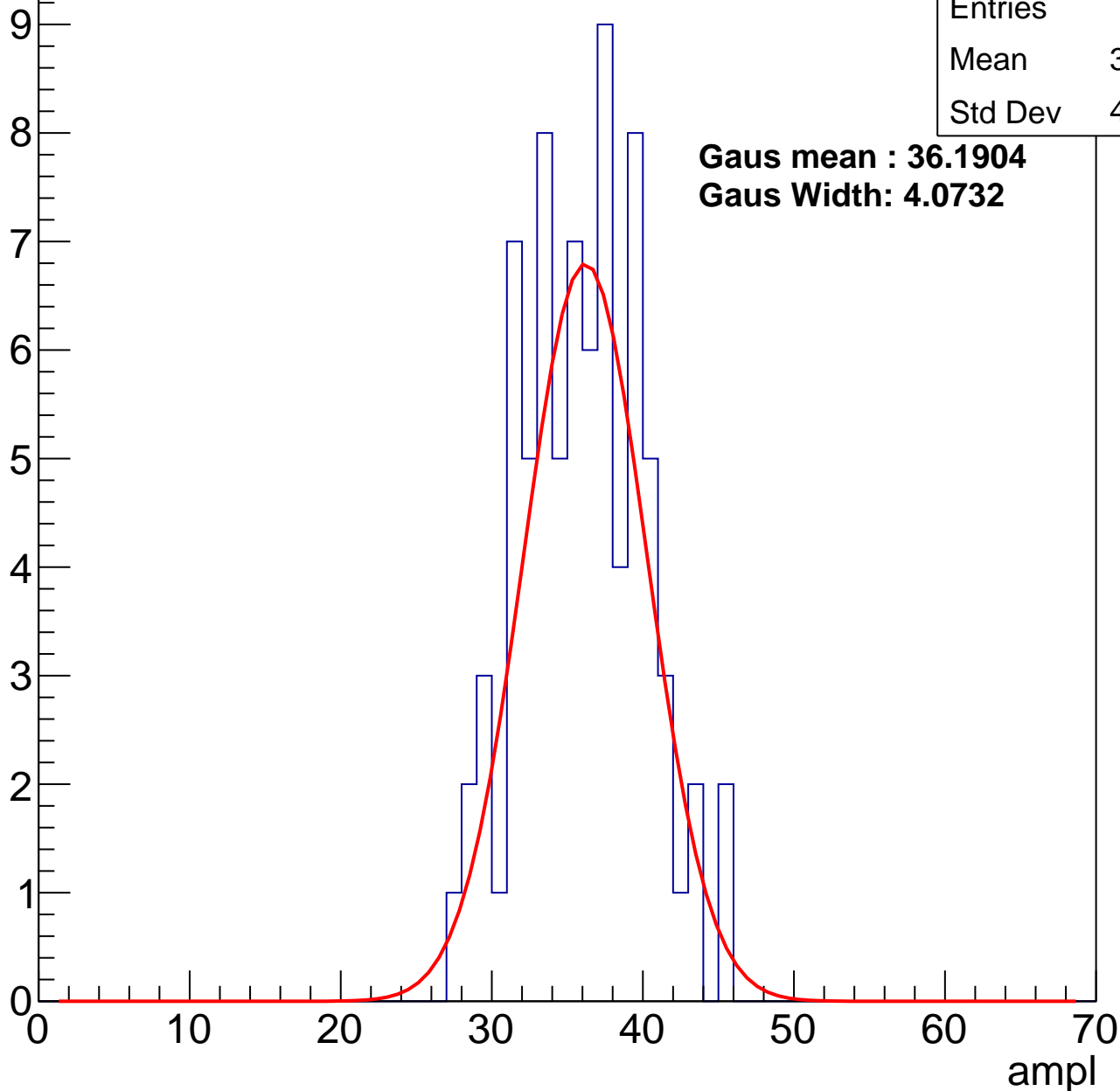
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	79
Mean	35.57
Std Dev	4.024

**Gaus mean : 36.1904**

**Gaus Width: 4.0732**



# B1L100S, U2-ch54, adc2

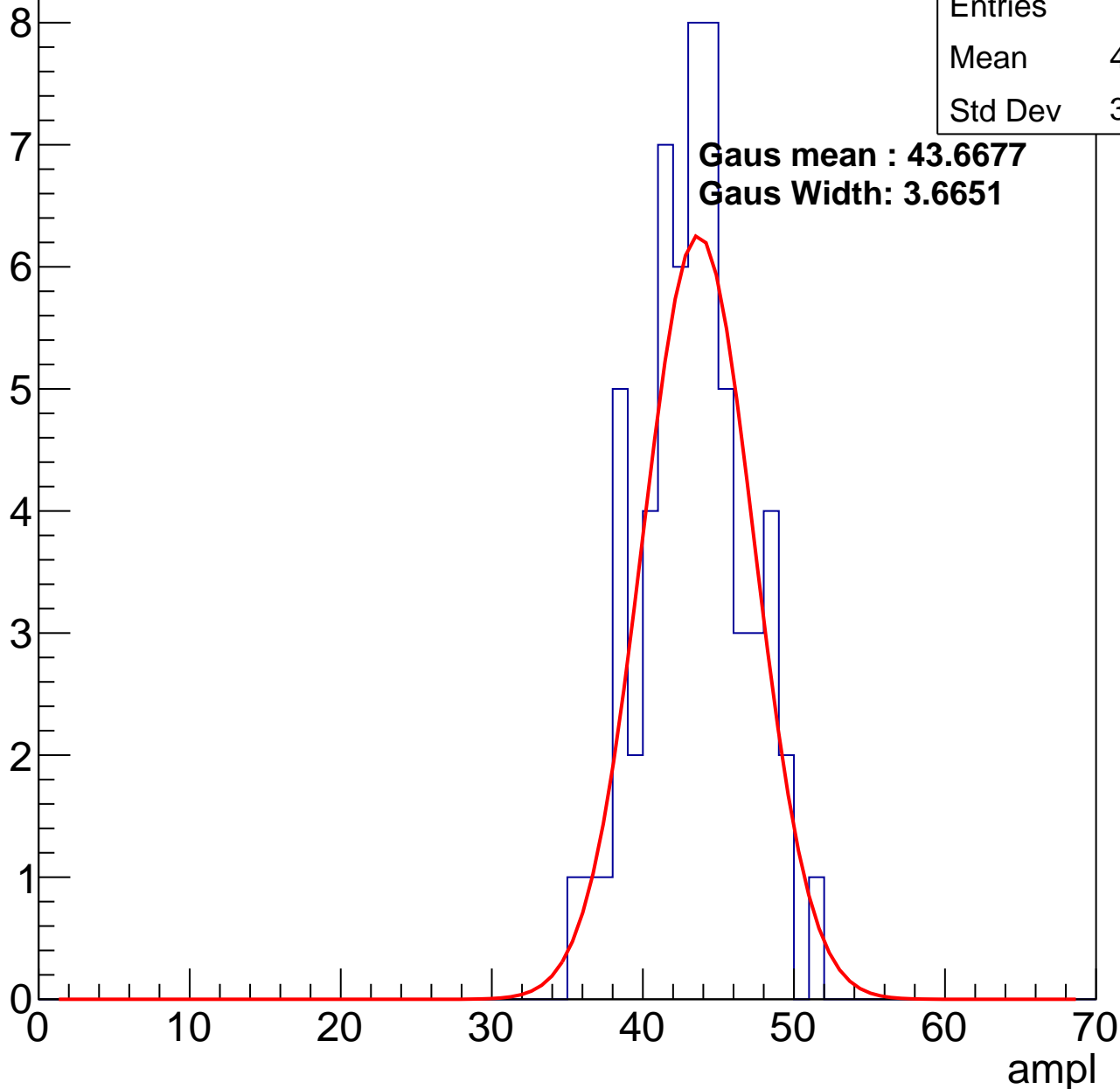
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	61
Mean	42.89
Std Dev	3.422

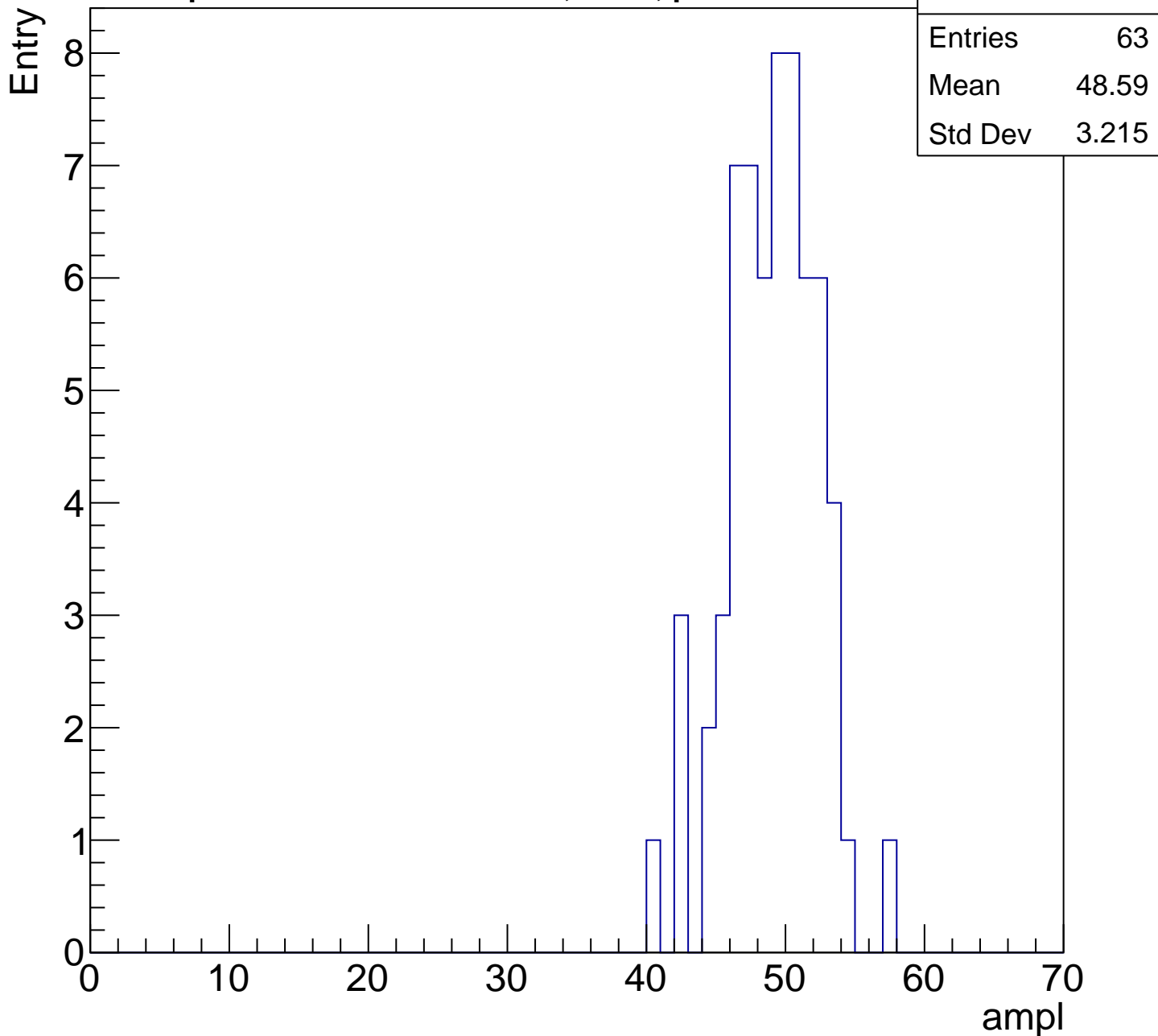
**Gaus mean : 43.6677**

**Gaus Width: 3.6651**



# B1L100S, U2-ch54, adc3

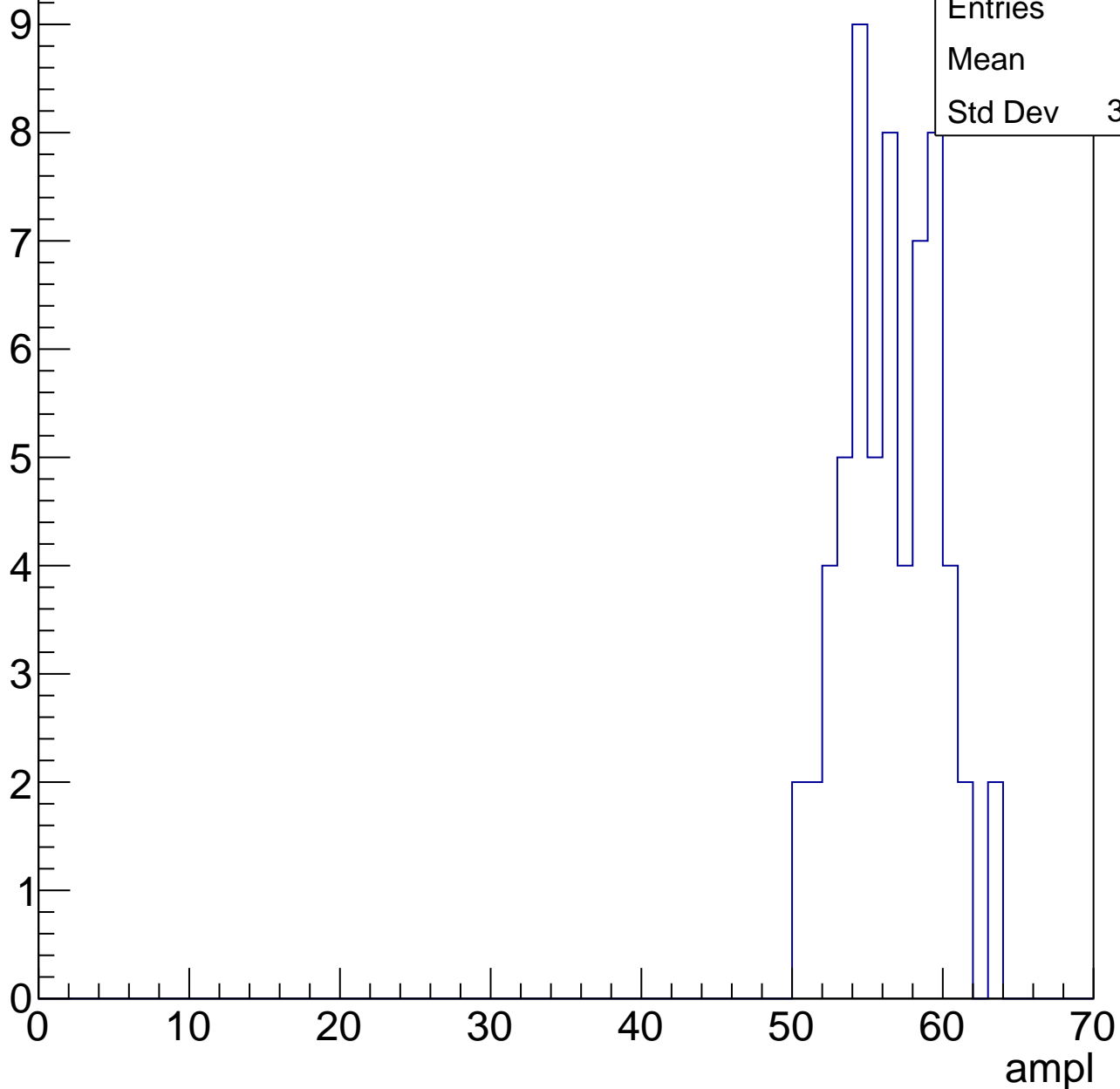
calib\_packv5\_042523\_0143.root, FC#4, port A2



# B1L100S, U2-ch54, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

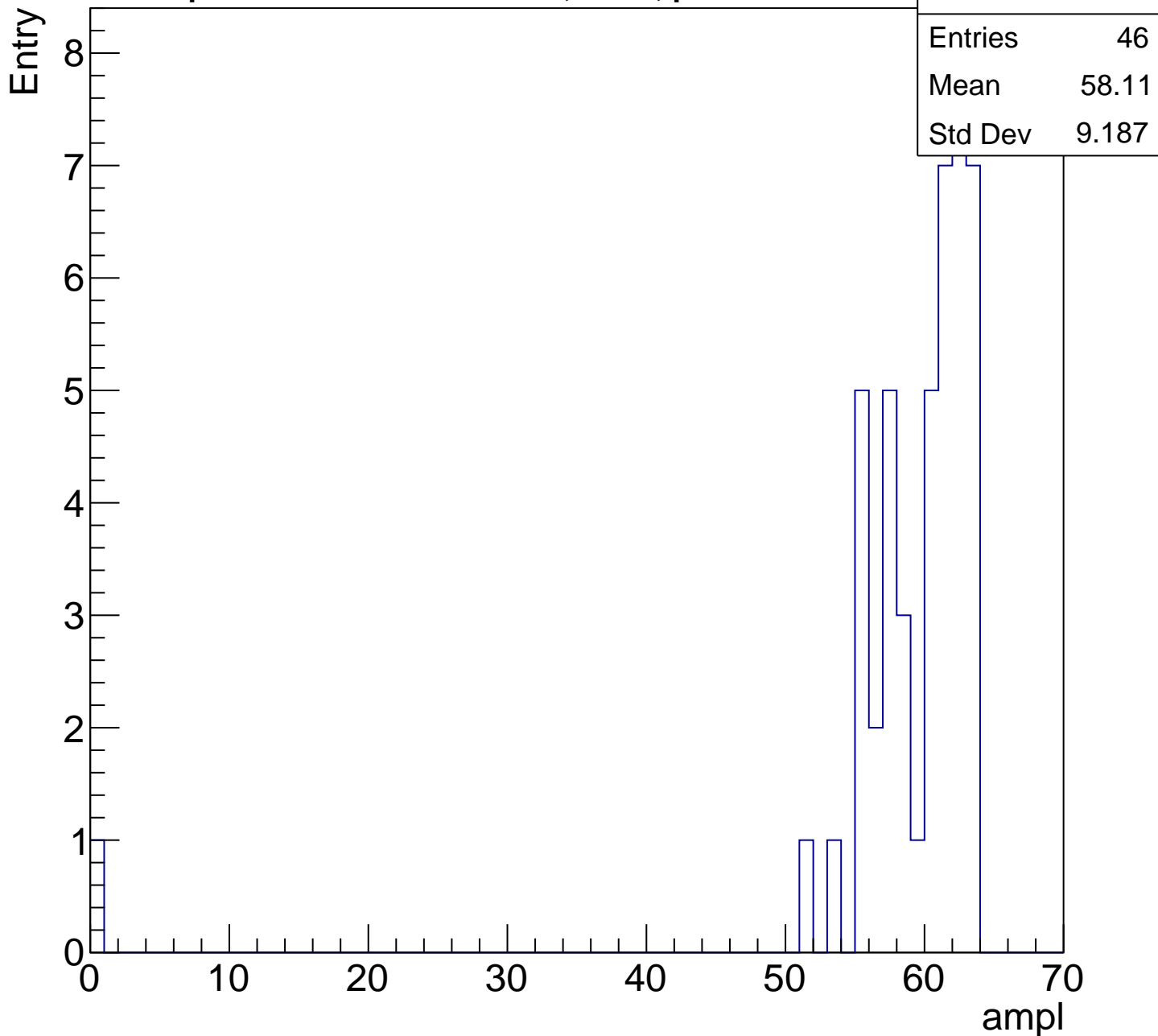
Entry



Entries	62
Mean	56.1
Std Dev	3.078

# B1L100S, U2-ch54, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2



# B1L100S, U2-ch54, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

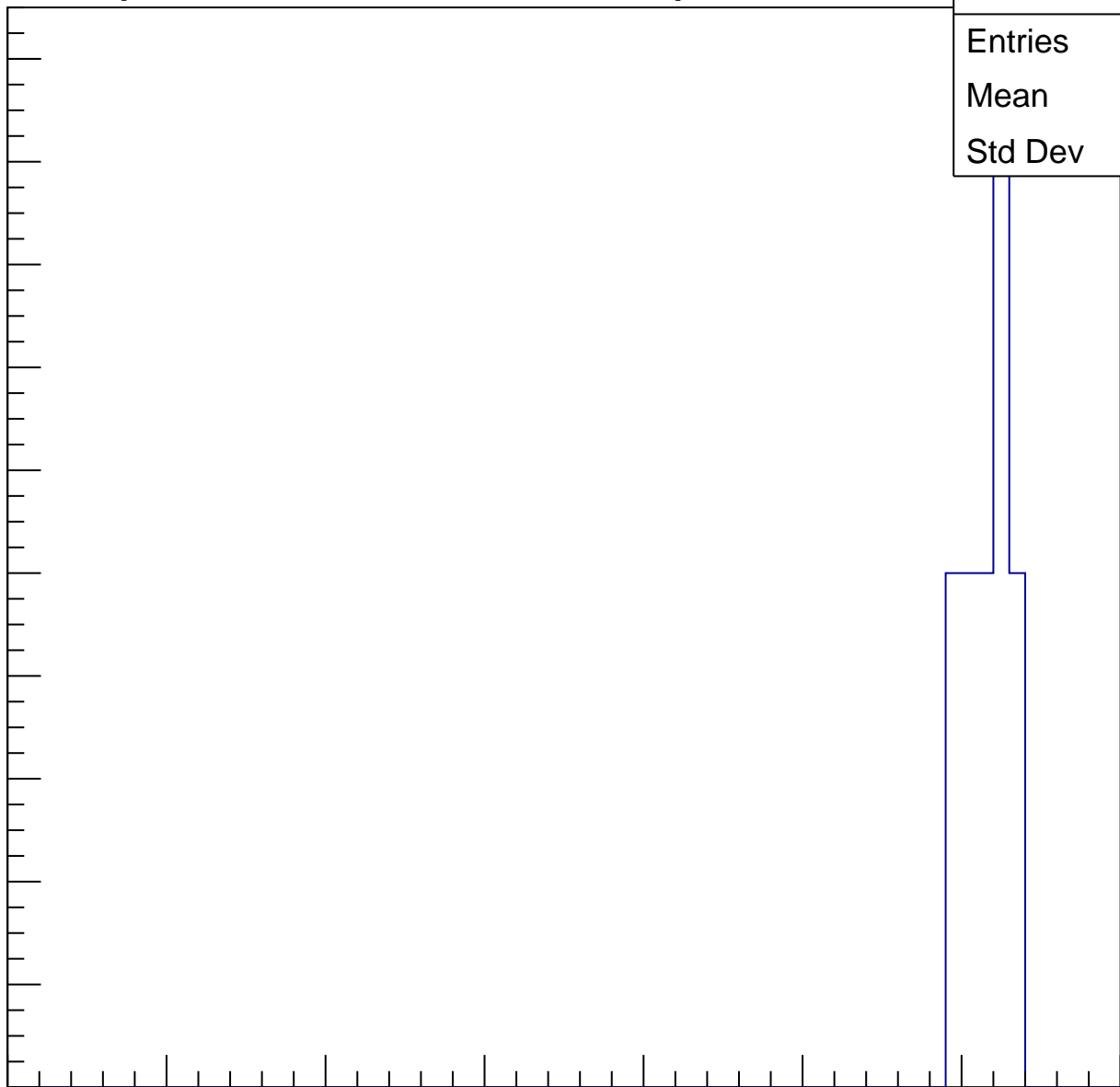
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	6
Mean	61.17
Std Dev	1.344

0 10 20 30 40 50 60 70

ampl





# B1L100S, U2-ch54, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L100S, U2-ch55, adc0

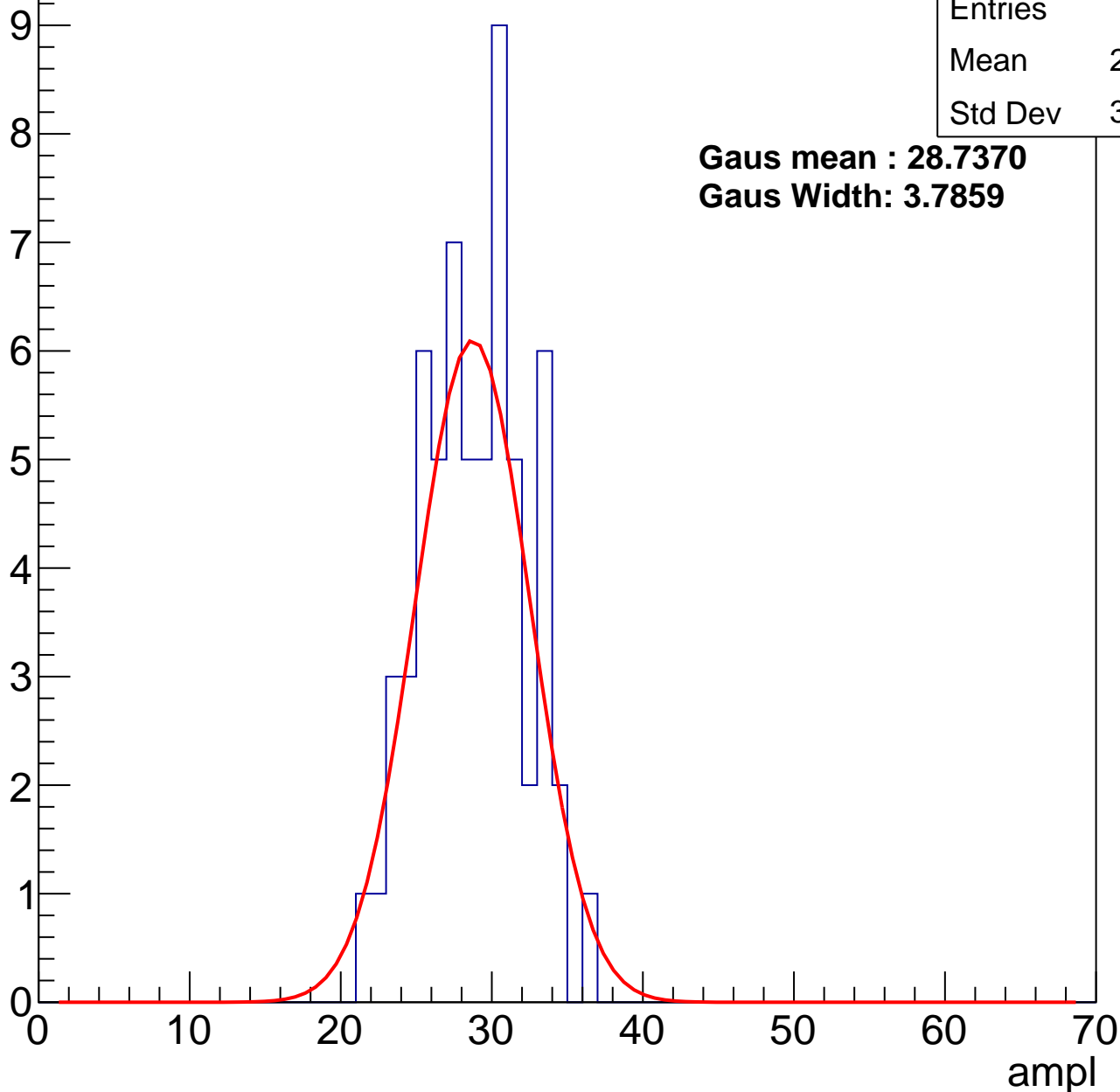
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	61
Mean	28.34
Std Dev	3.353

**Gaus mean : 28.7370**

**Gaus Width: 3.7859**



# B1L100S, U2-ch55, adc1

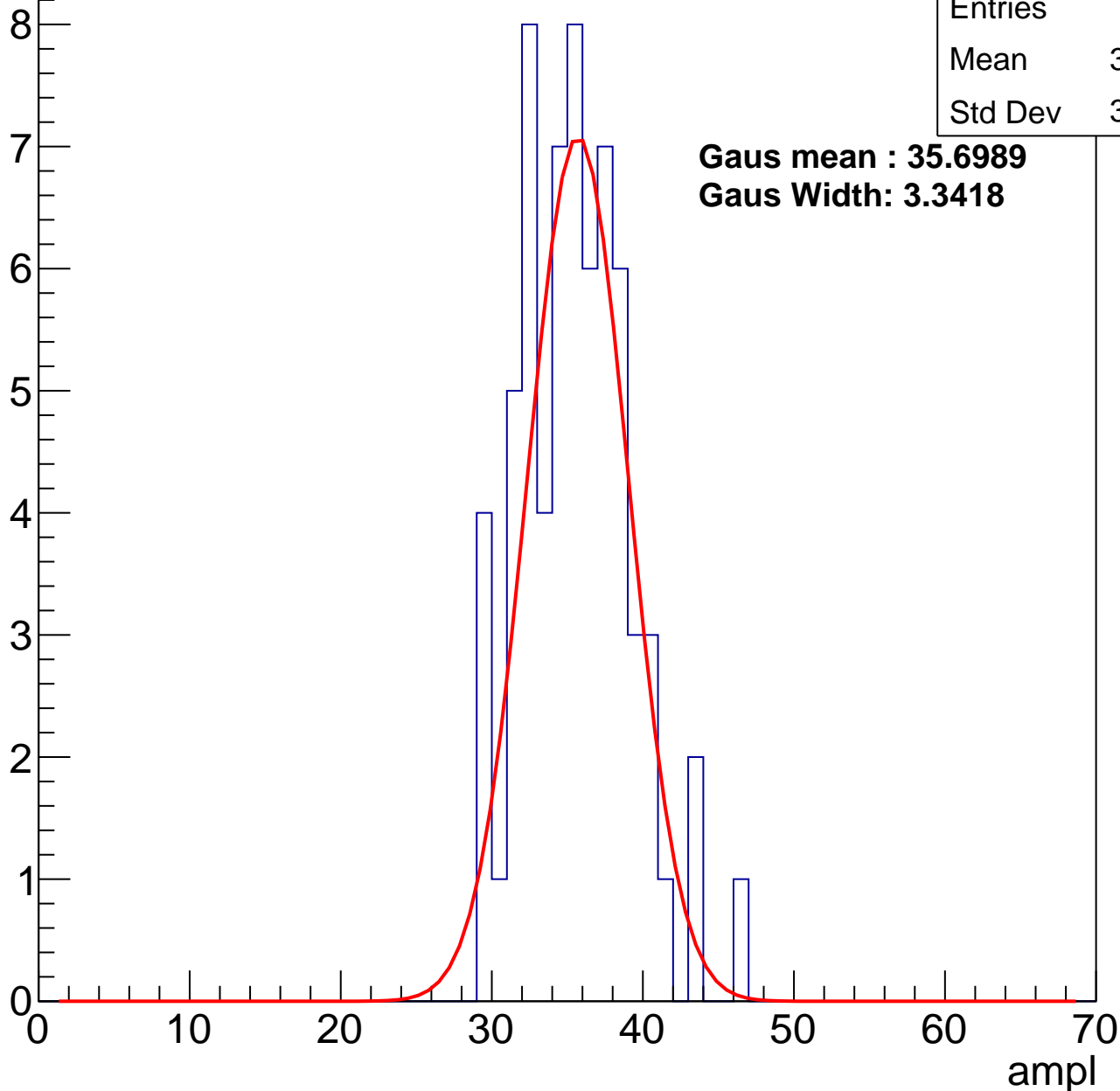
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	66
Mean	35.15
Std Dev	3.564

**Gaus mean : 35.6989**

**Gaus Width: 3.3418**



# B1L100S, U2-ch55, adc2

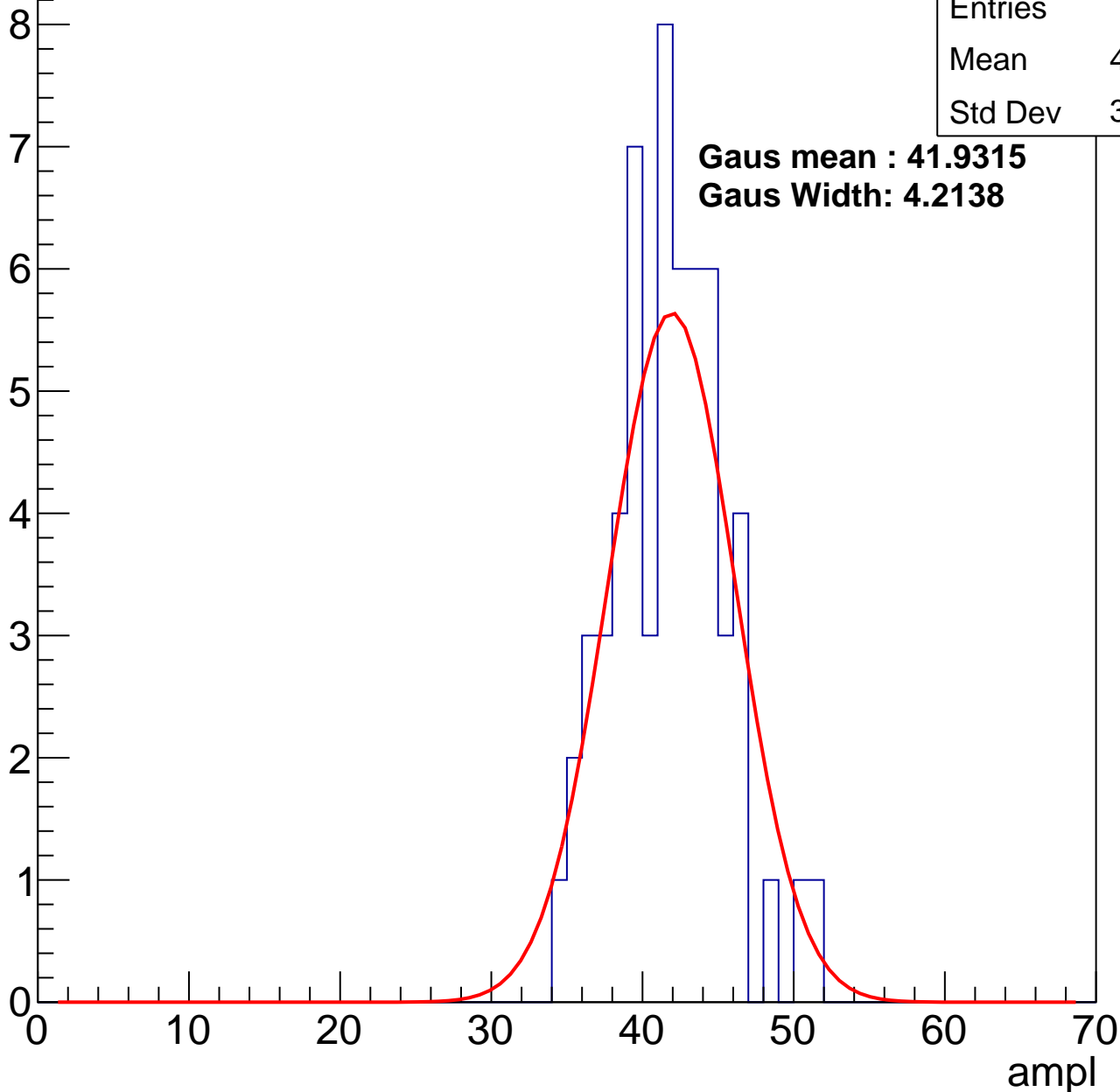
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	59
Mean	41.32
Std Dev	3.605

**Gaus mean : 41.9315**

**Gaus Width: 4.2138**



# B1L100S, U2-ch55, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

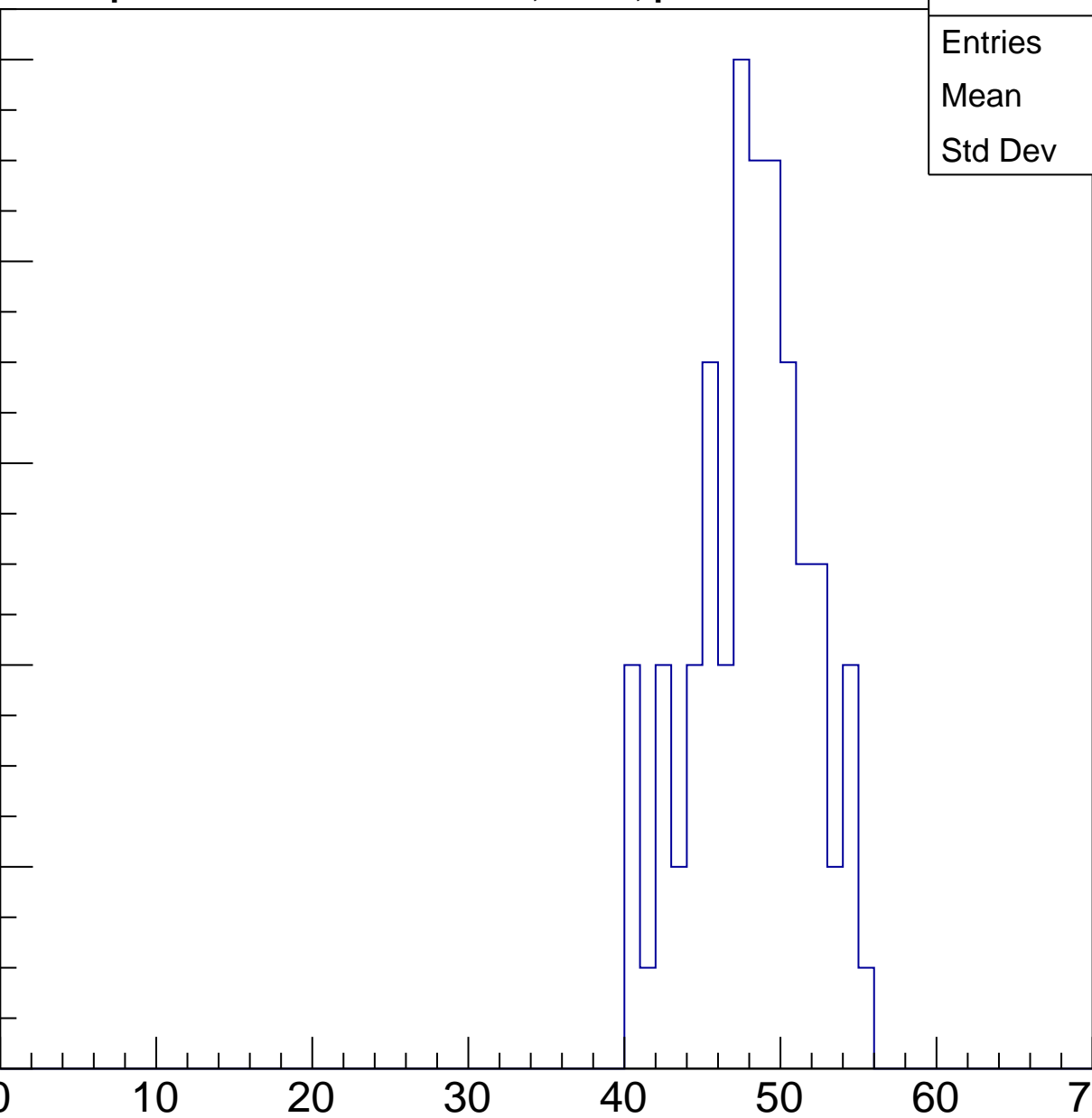
Entries	78
Mean	47.63
Std Dev	3.662

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

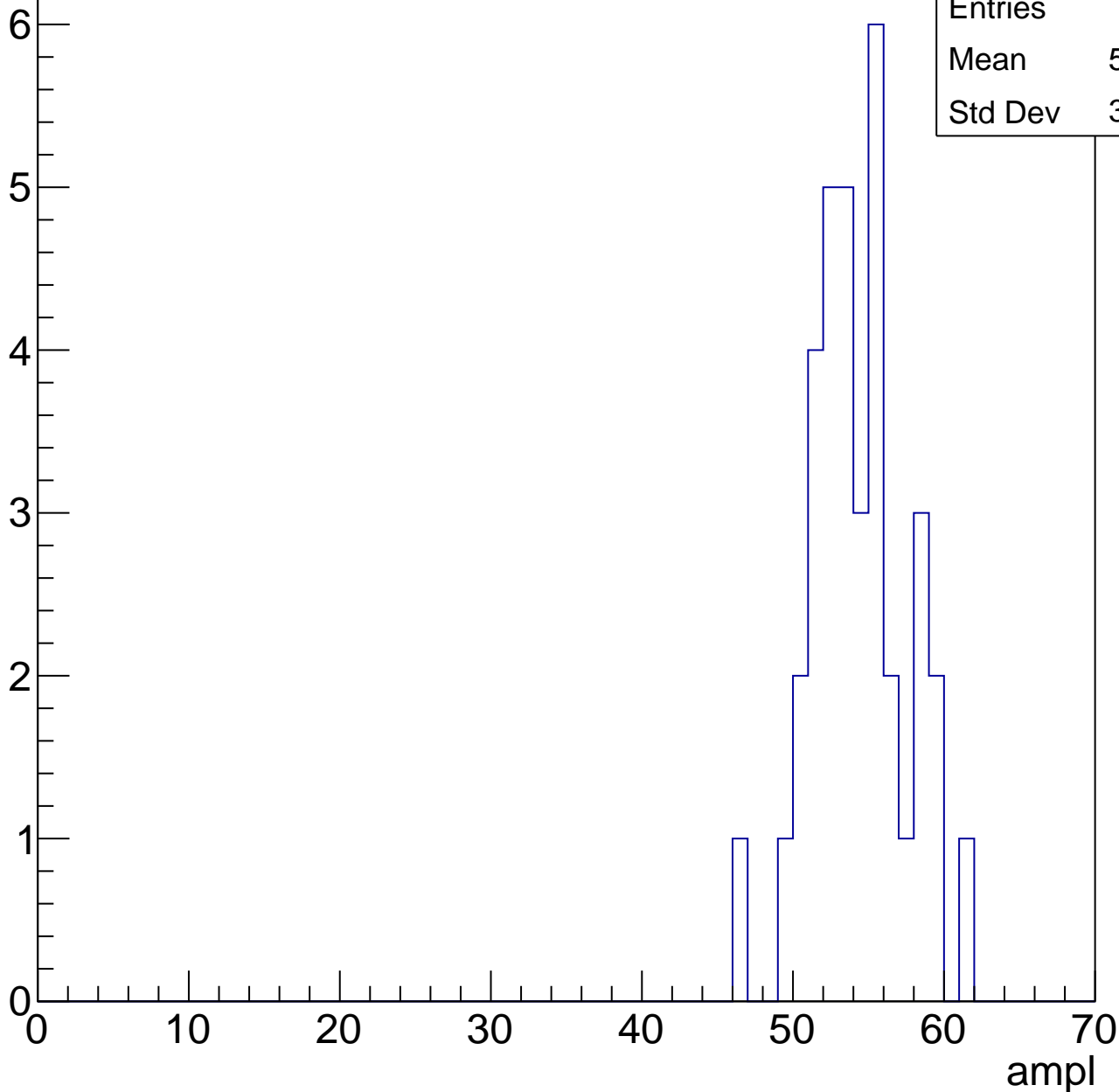


# B1L100S, U2-ch55, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

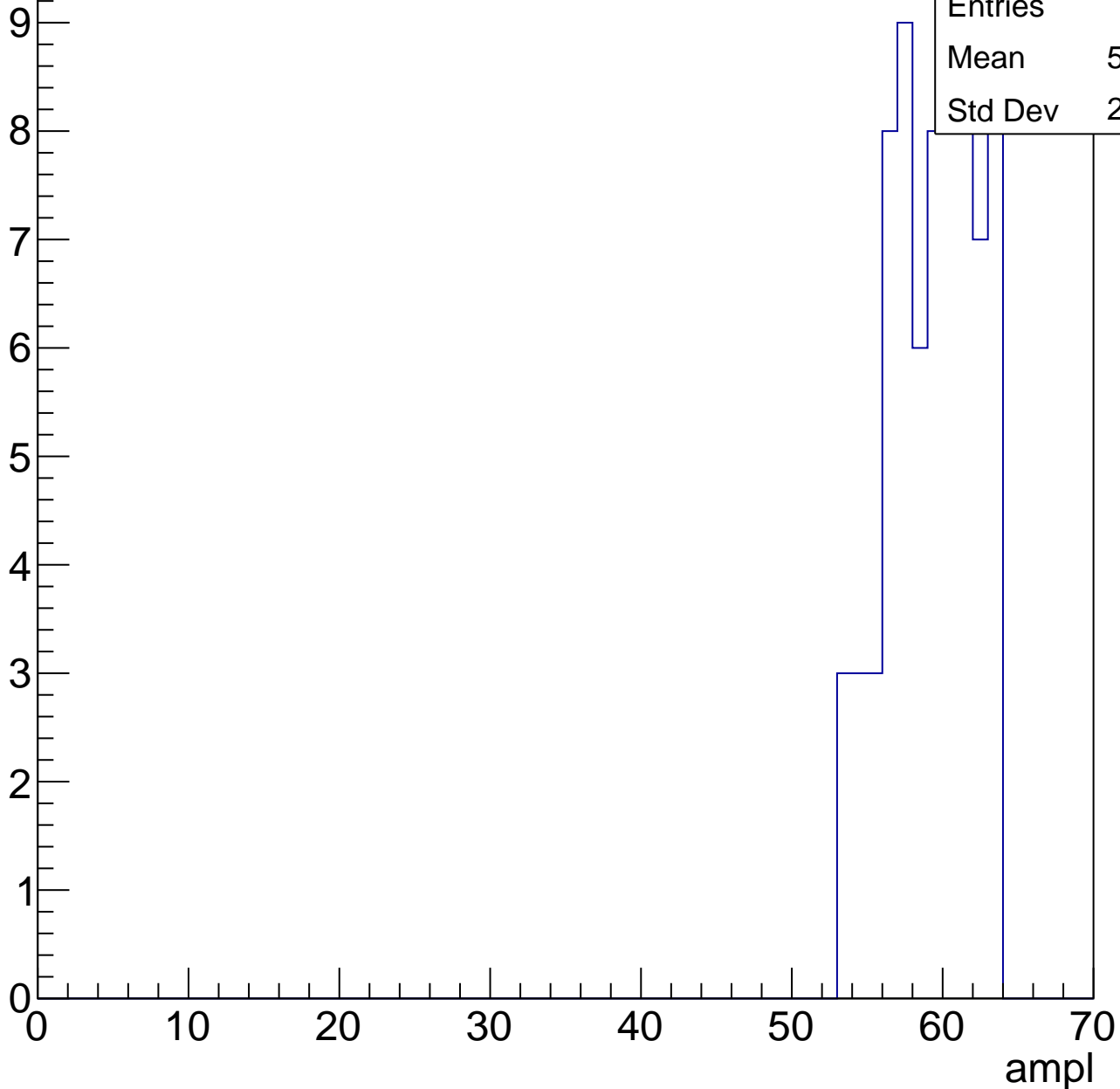
Entries	36
Mean	53.83
Std Dev	3.122



# B1L100S, U2-ch55, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	72
Mean	58.79
Std Dev	2.823

# B1L100S, U2-ch55, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

3

2.5

2

1.5

1

0.5

0

0

10

20

30

40

50

60

70

ampl

Entries

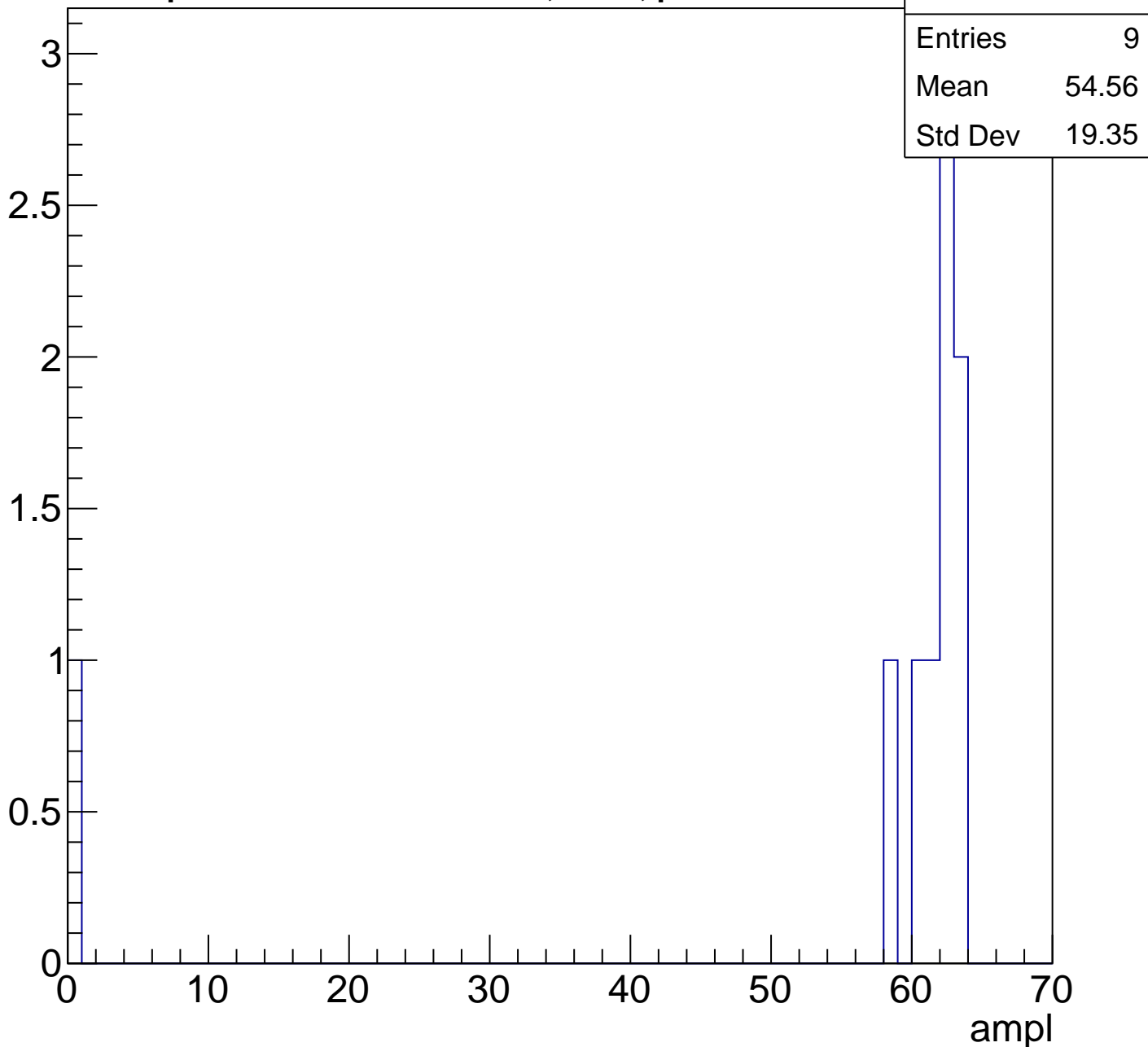
9

Mean

54.56

Std Dev

19.35





# B1L100S, U2-ch55, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L100S, U2-ch56, adc0

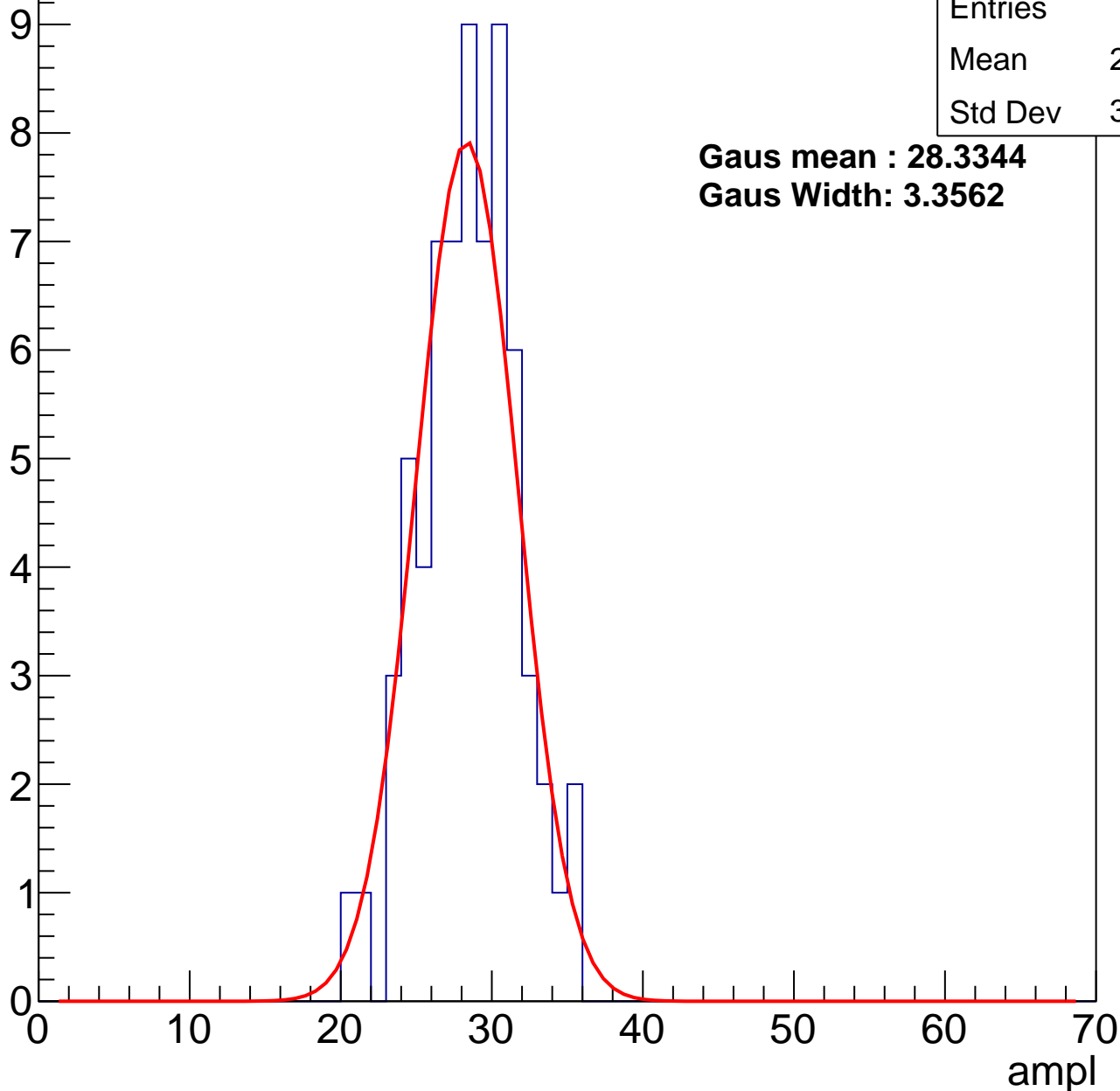
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	67
Mean	28.03
Std Dev	3.157

**Gaus mean : 28.3344**

**Gaus Width: 3.3562**



# B1L100S, U2-ch56, adc1

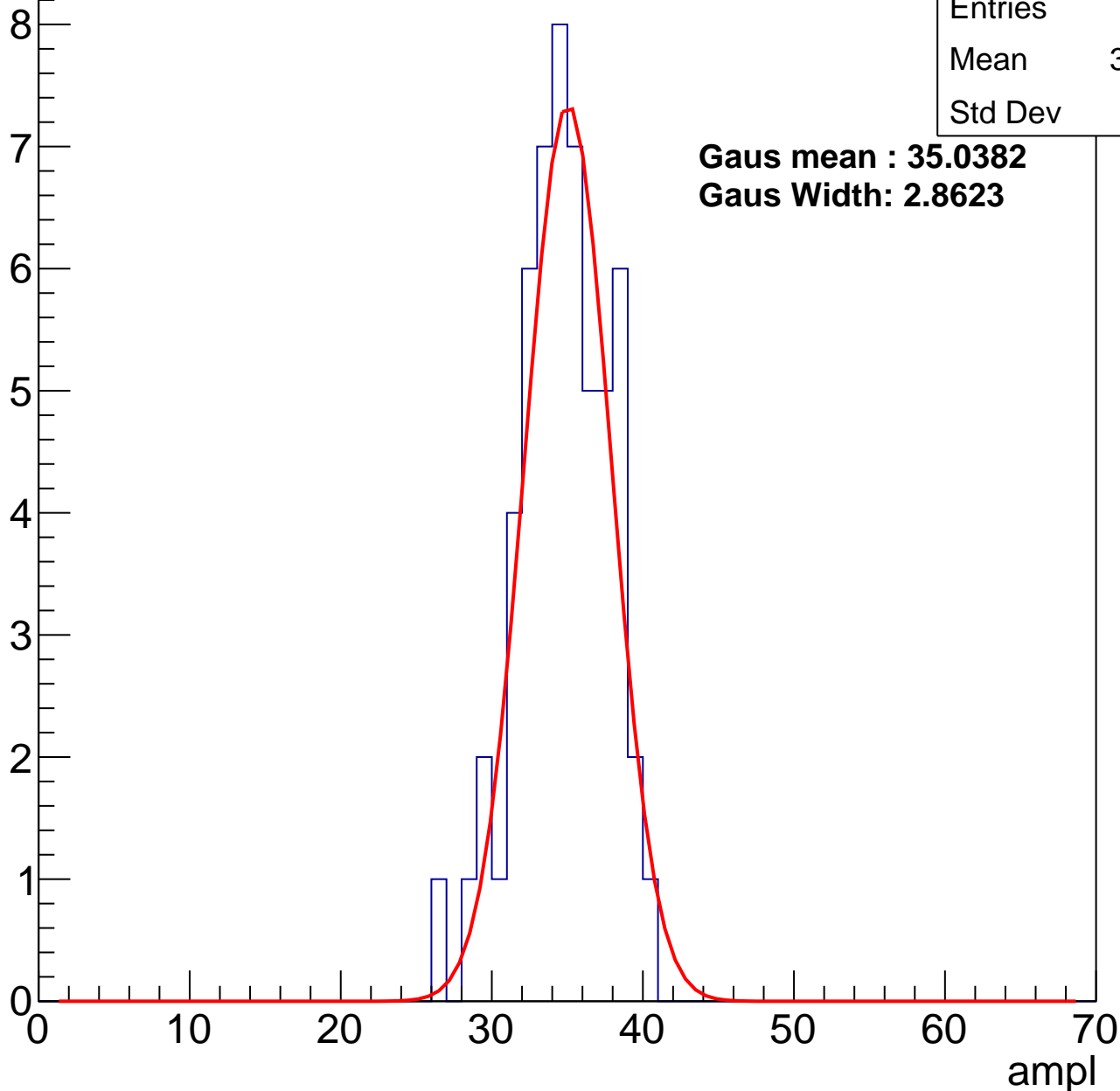
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	56
Mean	34.23
Std Dev	2.94

**Gaus mean : 35.0382**

**Gaus Width: 2.8623**



# B1L100S, U2-ch56, adc2

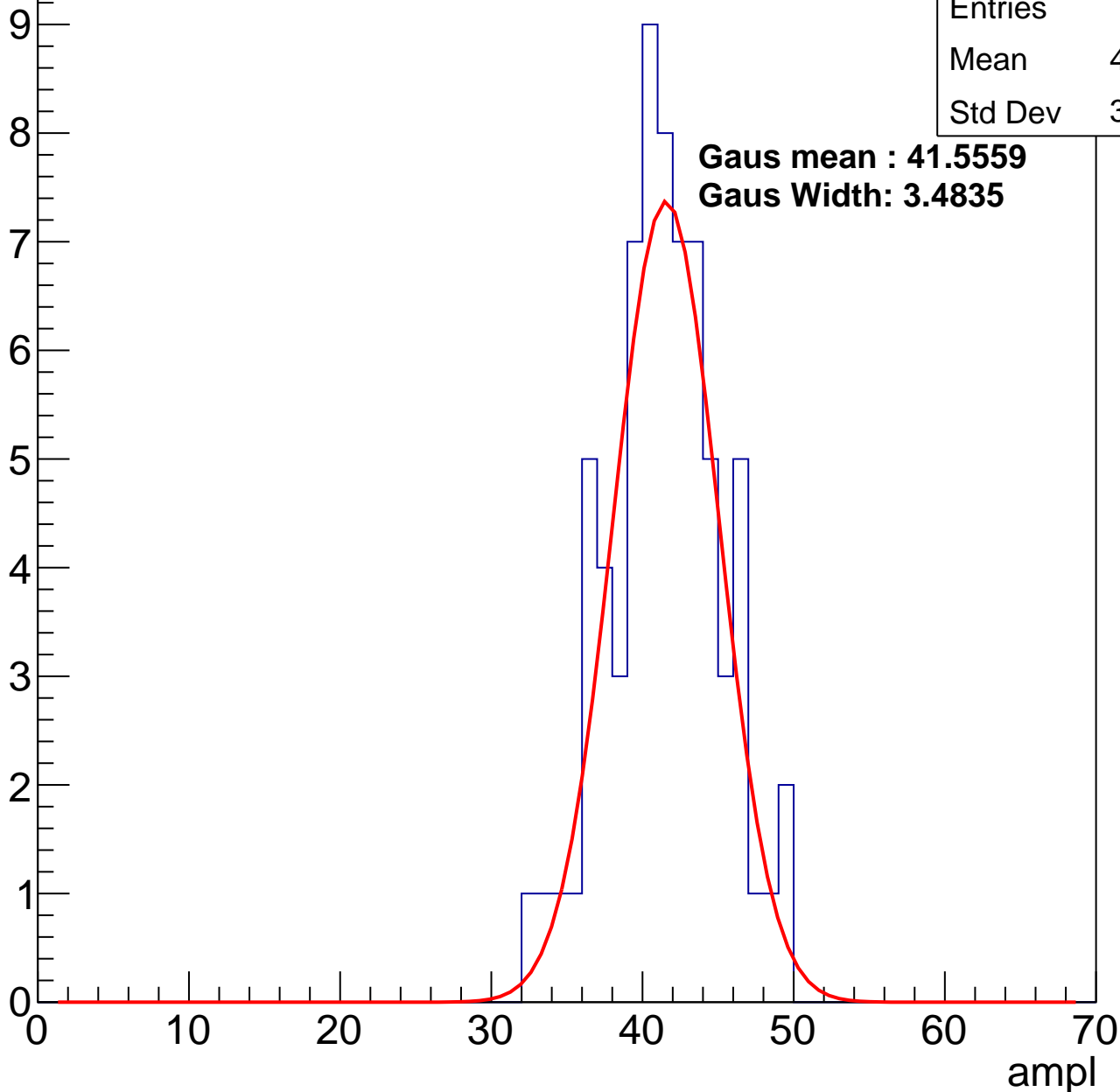
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	71
Mean	40.99
Std Dev	3.656

**Gaus mean : 41.5559**

**Gaus Width: 3.4835**

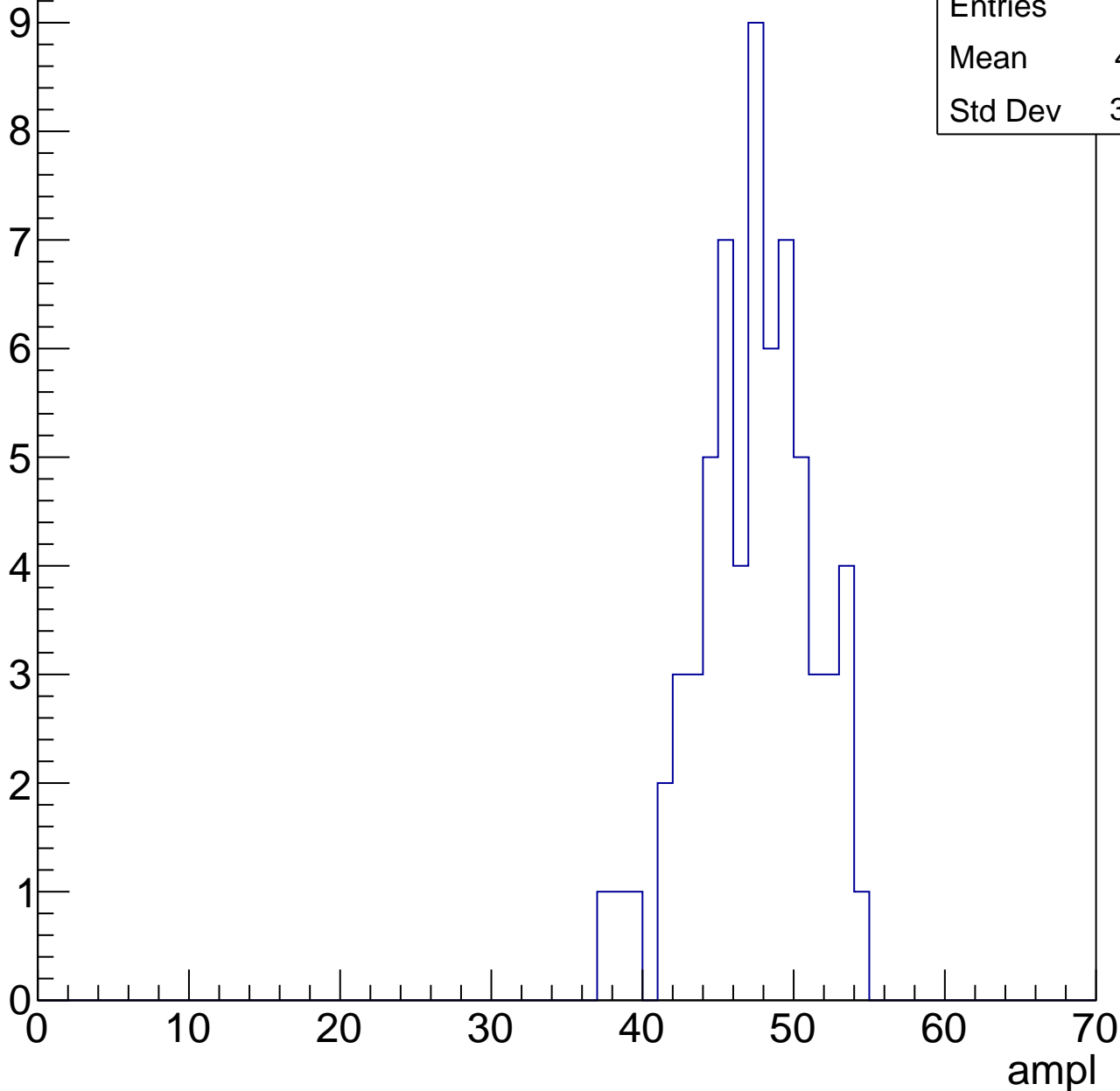


# B1L100S, U2-ch56, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	65
Mean	46.91
Std Dev	3.745

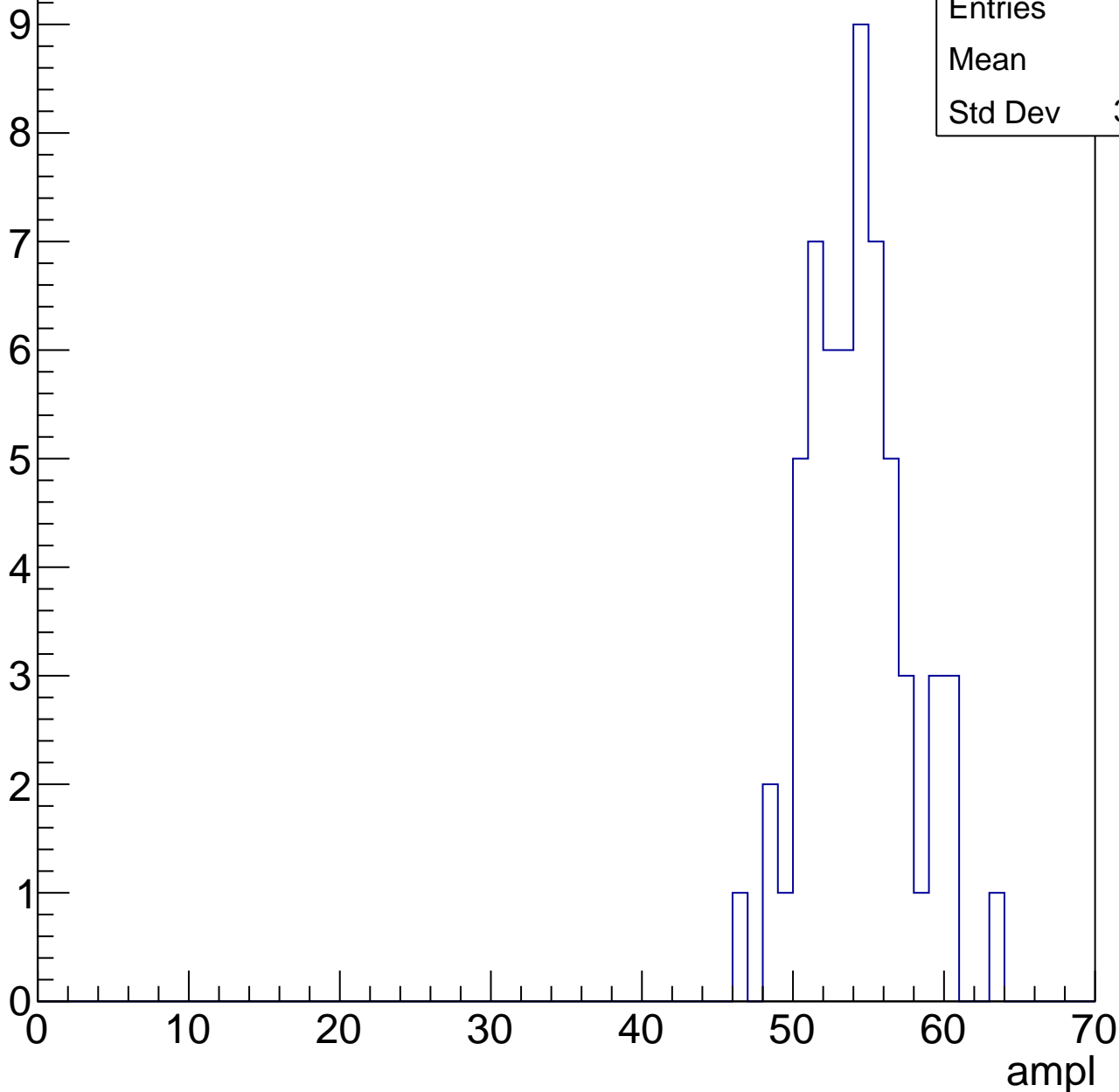


# B1L100S, U2-ch56, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

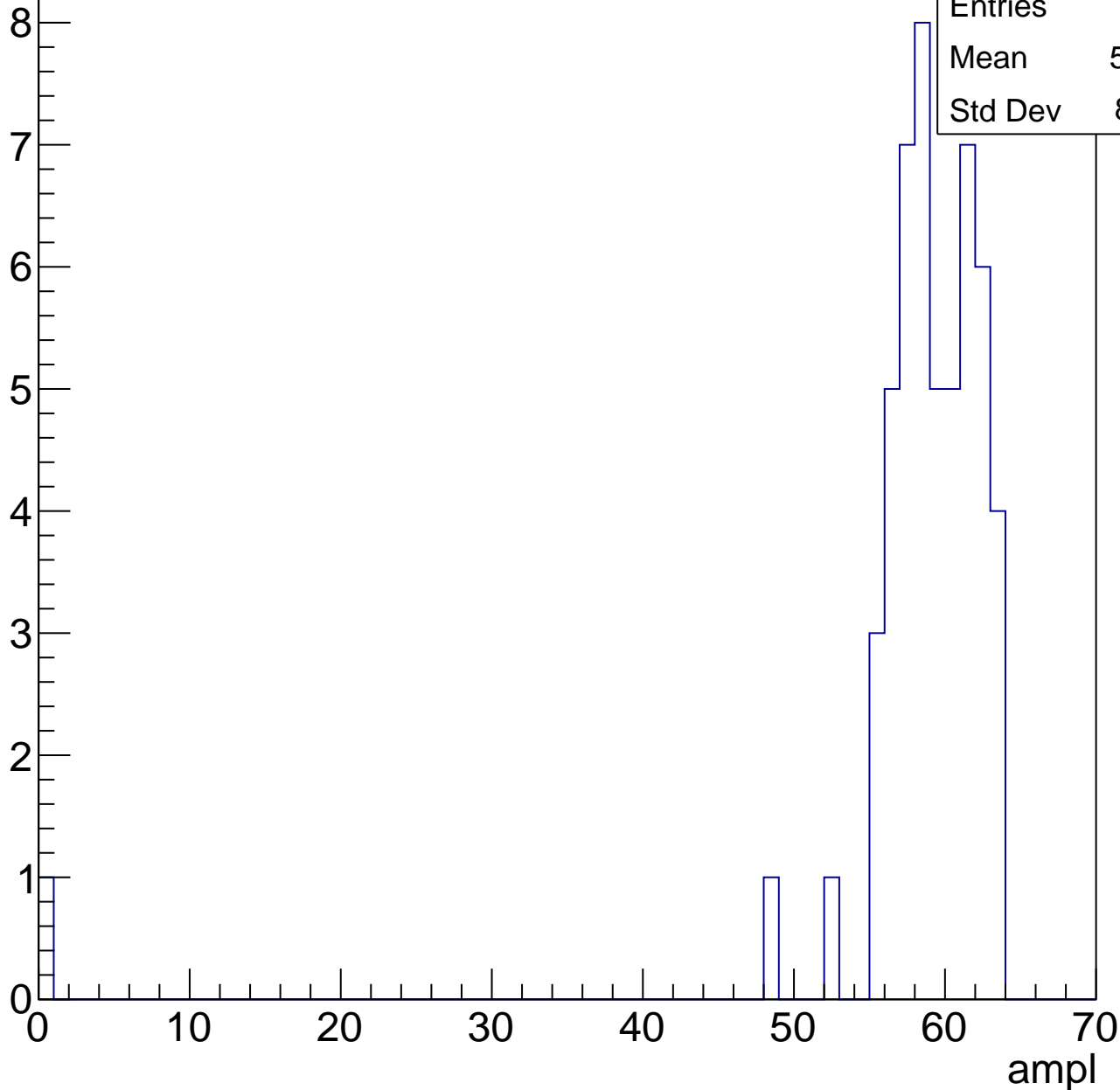
Entries	60
Mean	53.8
Std Dev	3.331



# B1L100S, U2-ch56, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

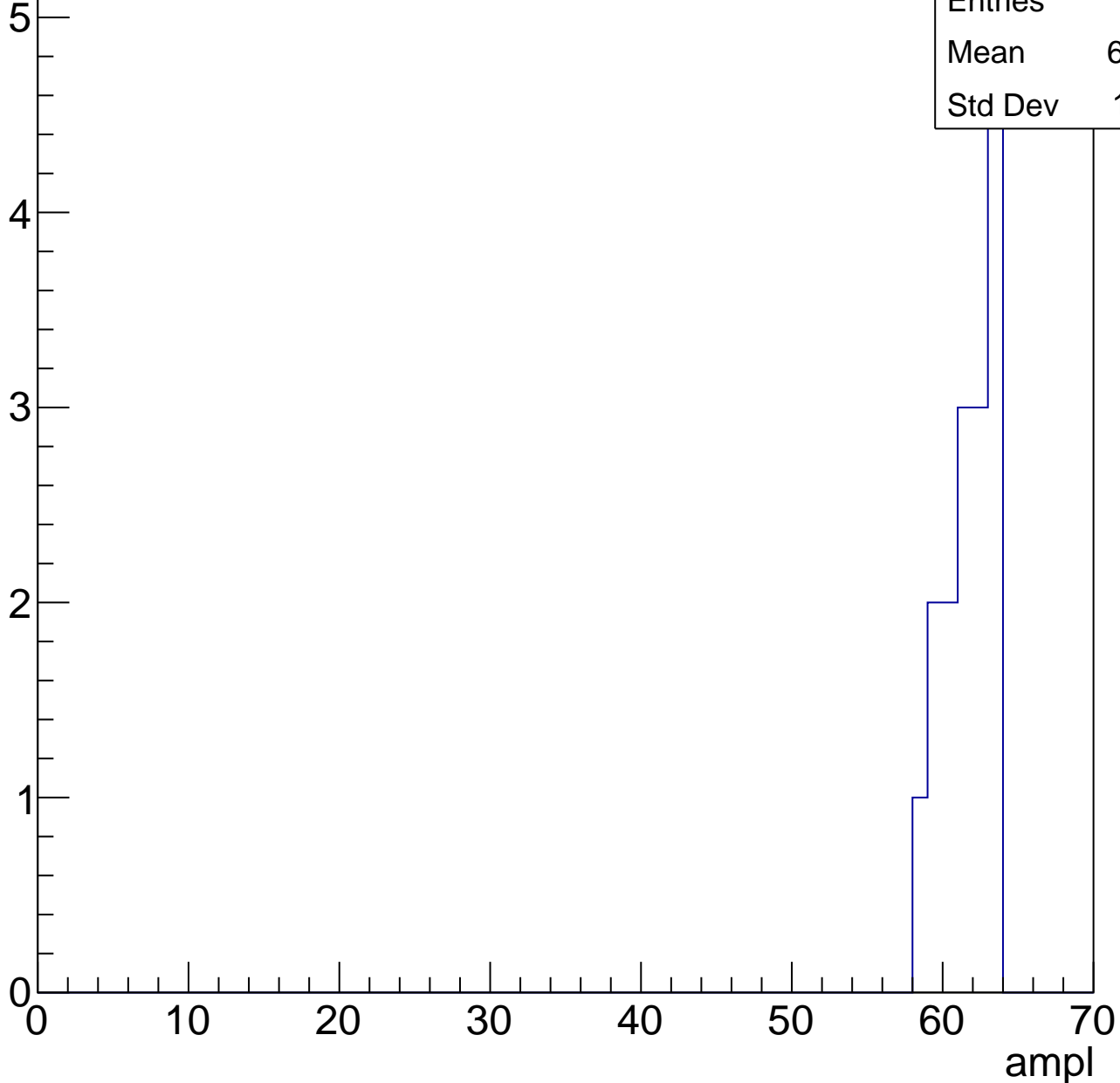


# B1L100S, U2-ch56, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	16
Mean	61.25
Std Dev	1.601





# B1L100S, U2-ch56, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



# B1L100S, U2-ch57, adc0

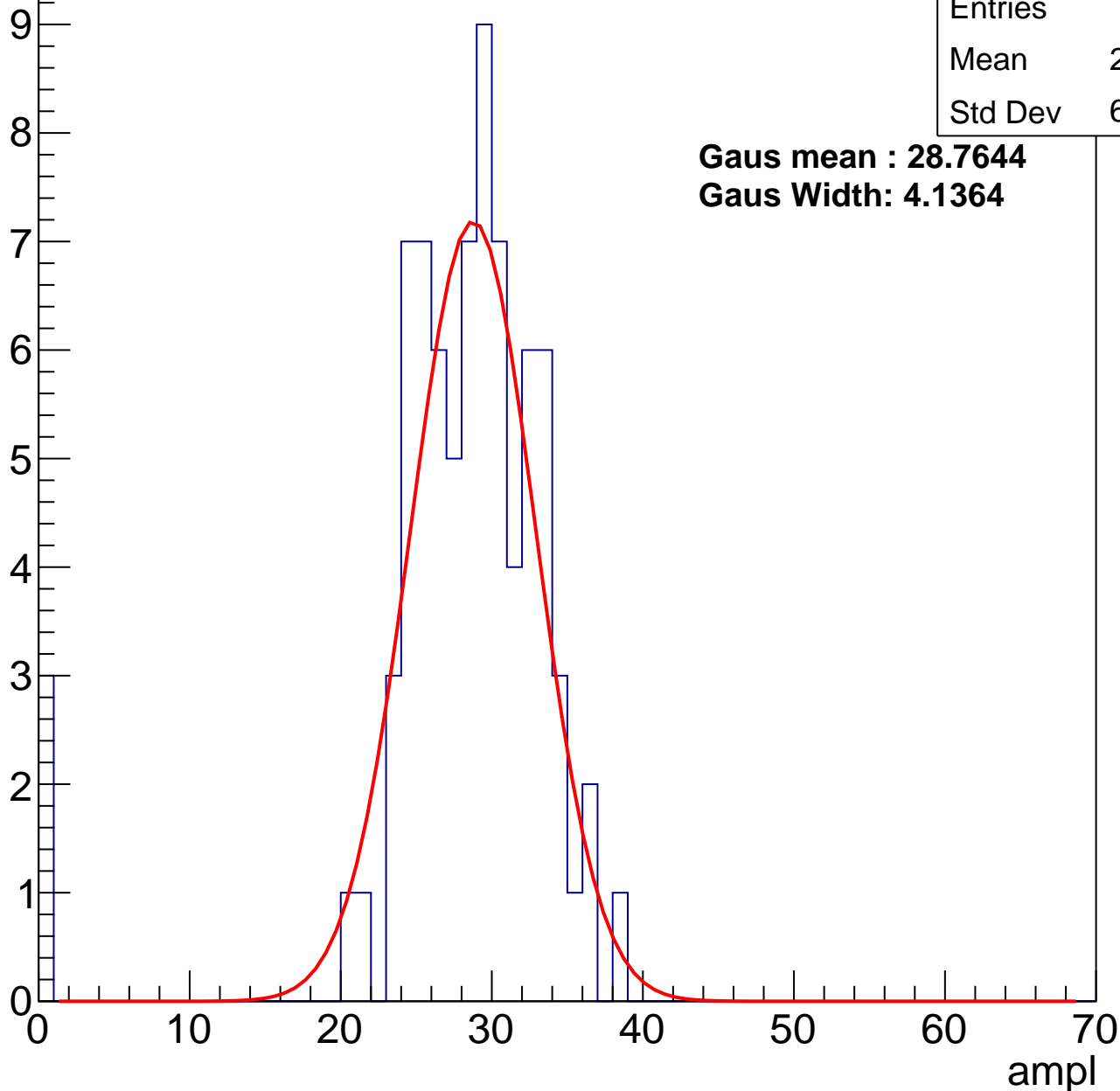
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	79
Mean	27.49
Std Dev	6.587

**Gaus mean : 28.7644**

**Gaus Width: 4.1364**



# B1L100S, U2-ch57, adc1

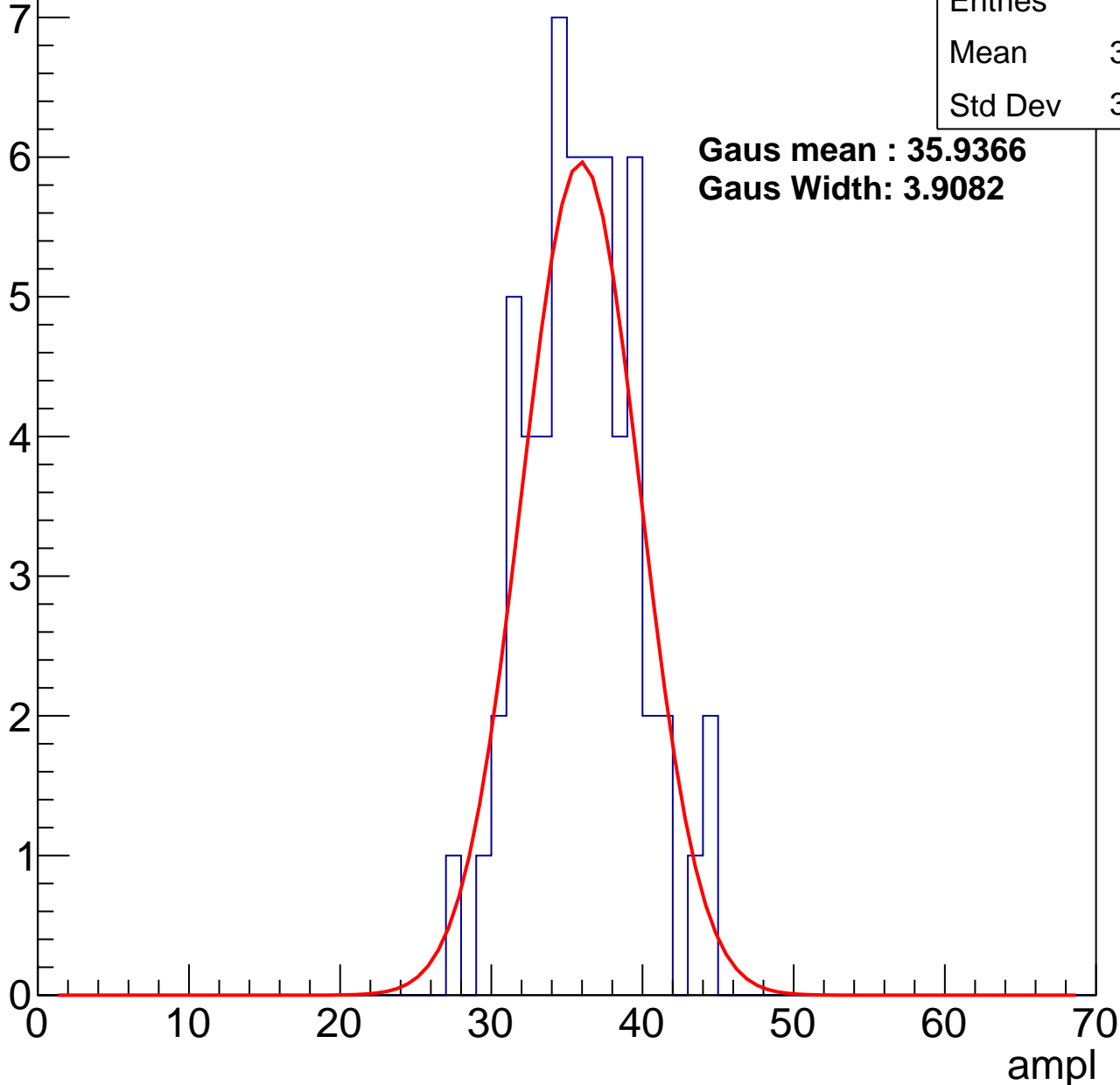
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	59
Mean	35.53
Std Dev	3.642

**Gaus mean : 35.9366**

**Gaus Width: 3.9082**



# B1L100S, U2-ch57, adc2

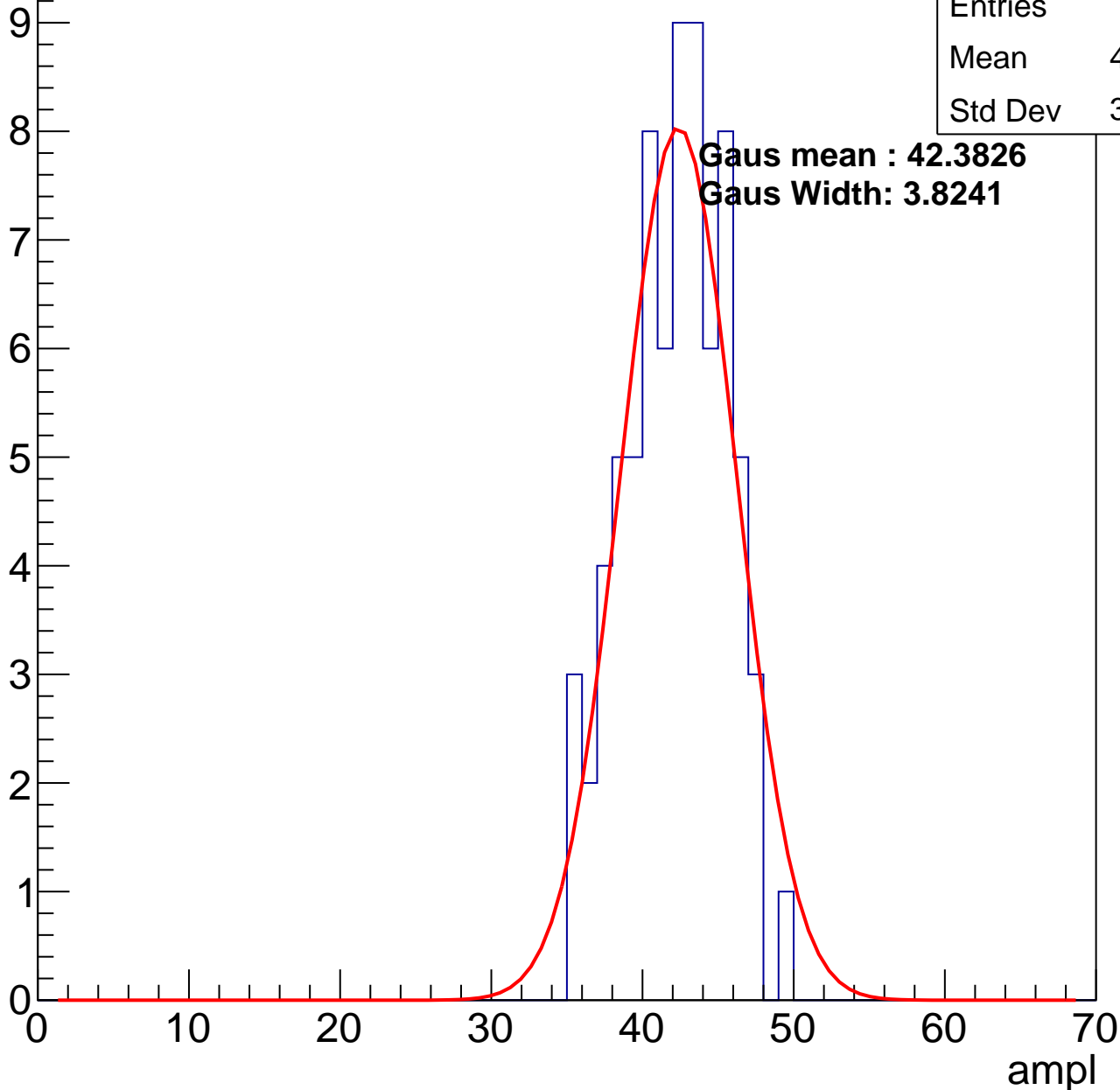
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	74
Mean	41.69
Std Dev	3.255

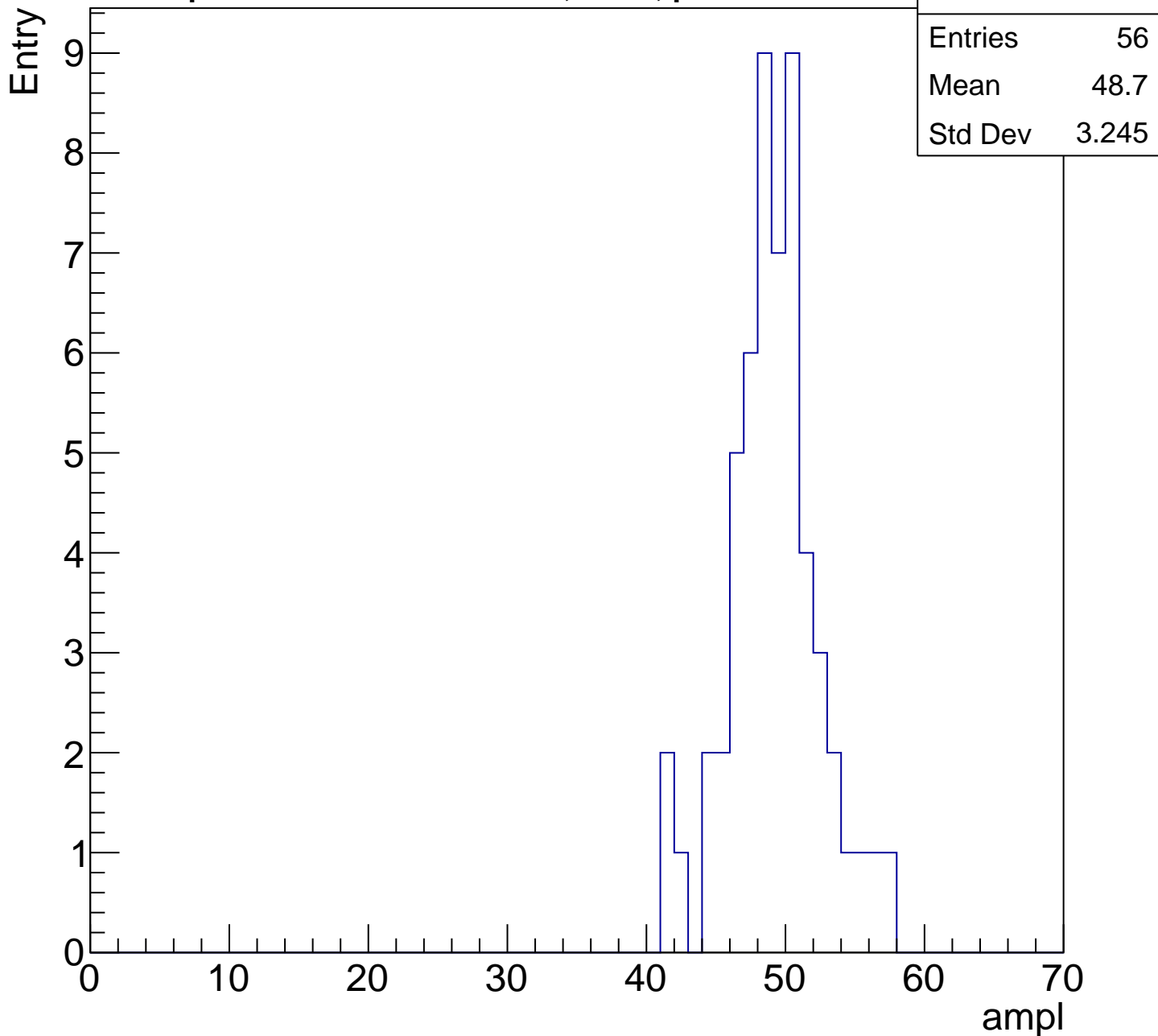
**Gaus mean : 42.3826**

**Gaus Width: 3.8241**



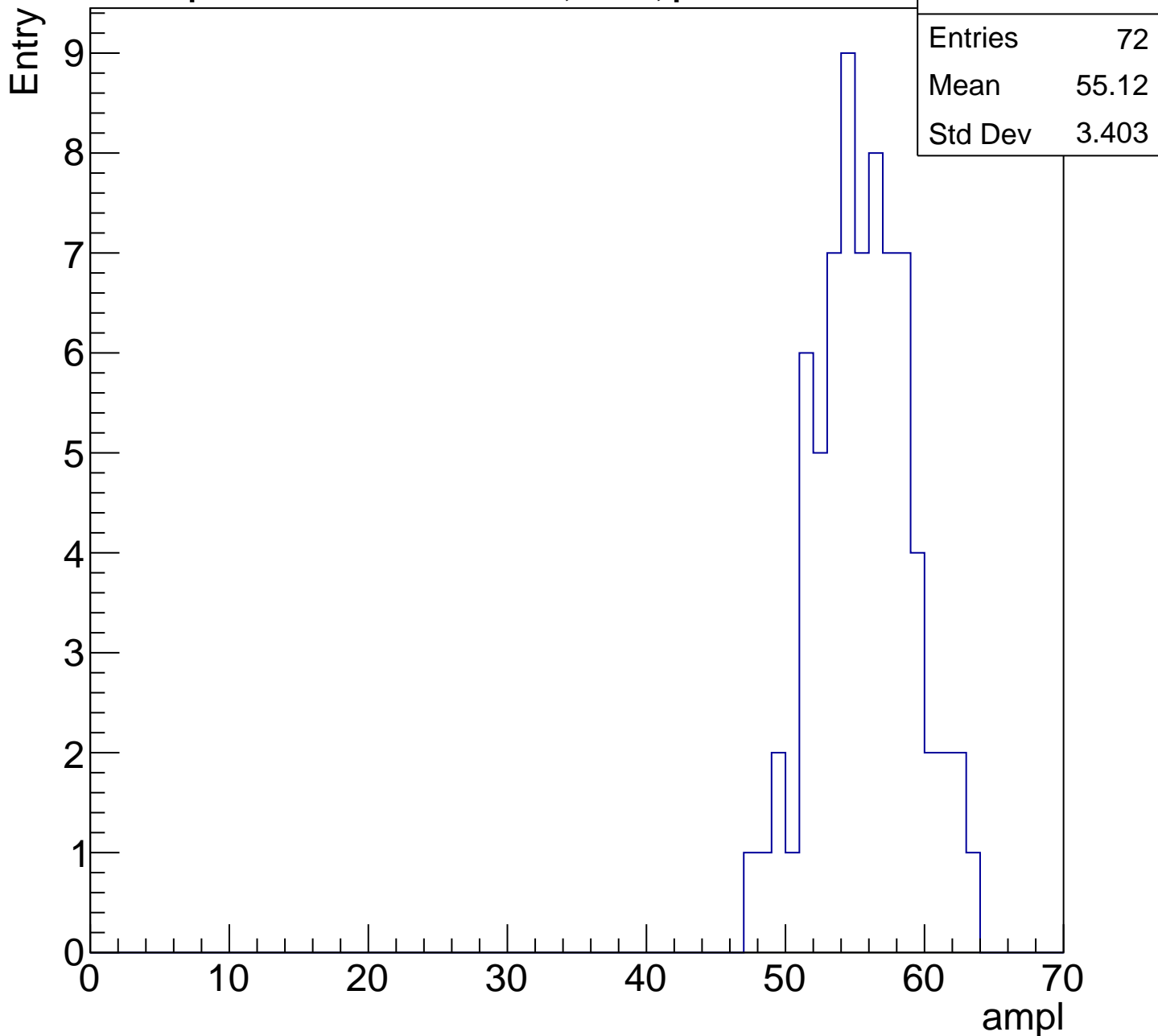
# B1L100S, U2-ch57, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2



# B1L100S, U2-ch57, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2



# B1L100S, U2-ch57, adc5

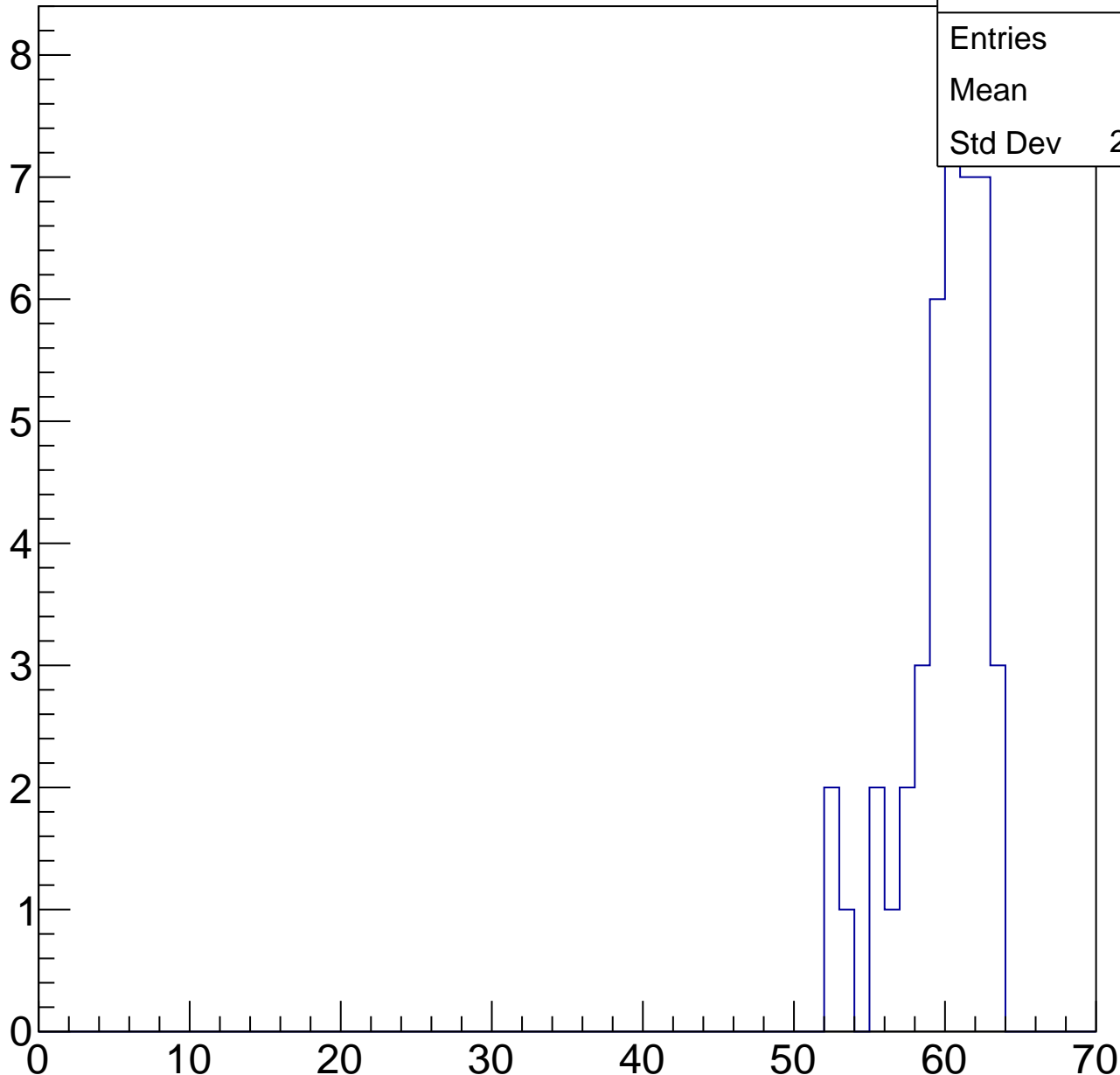
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	42
Mean	59.4
Std Dev	2.787

ampl

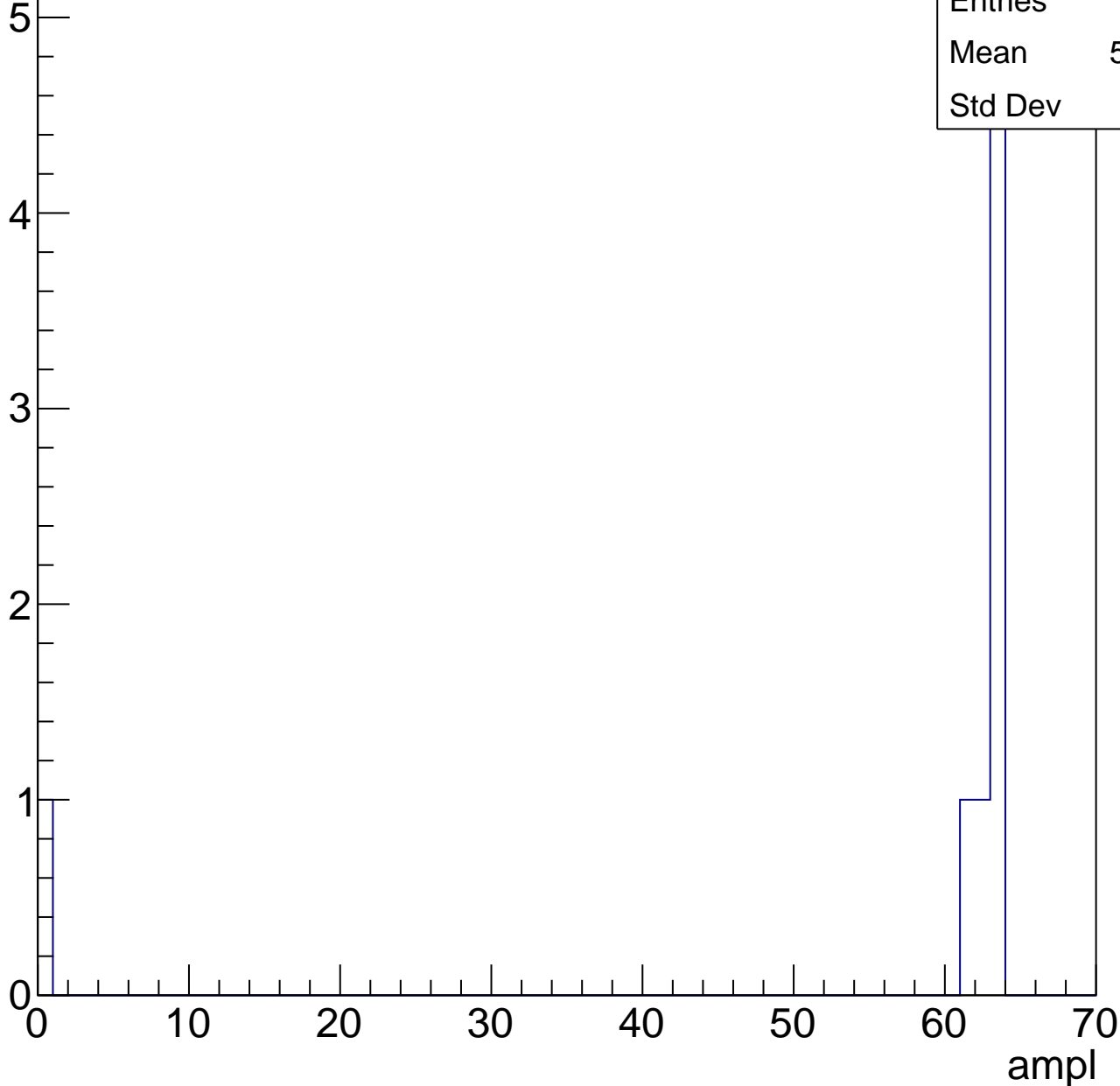


# B1L100S, U2-ch57, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	8
Mean	54.75
Std Dev	20.7

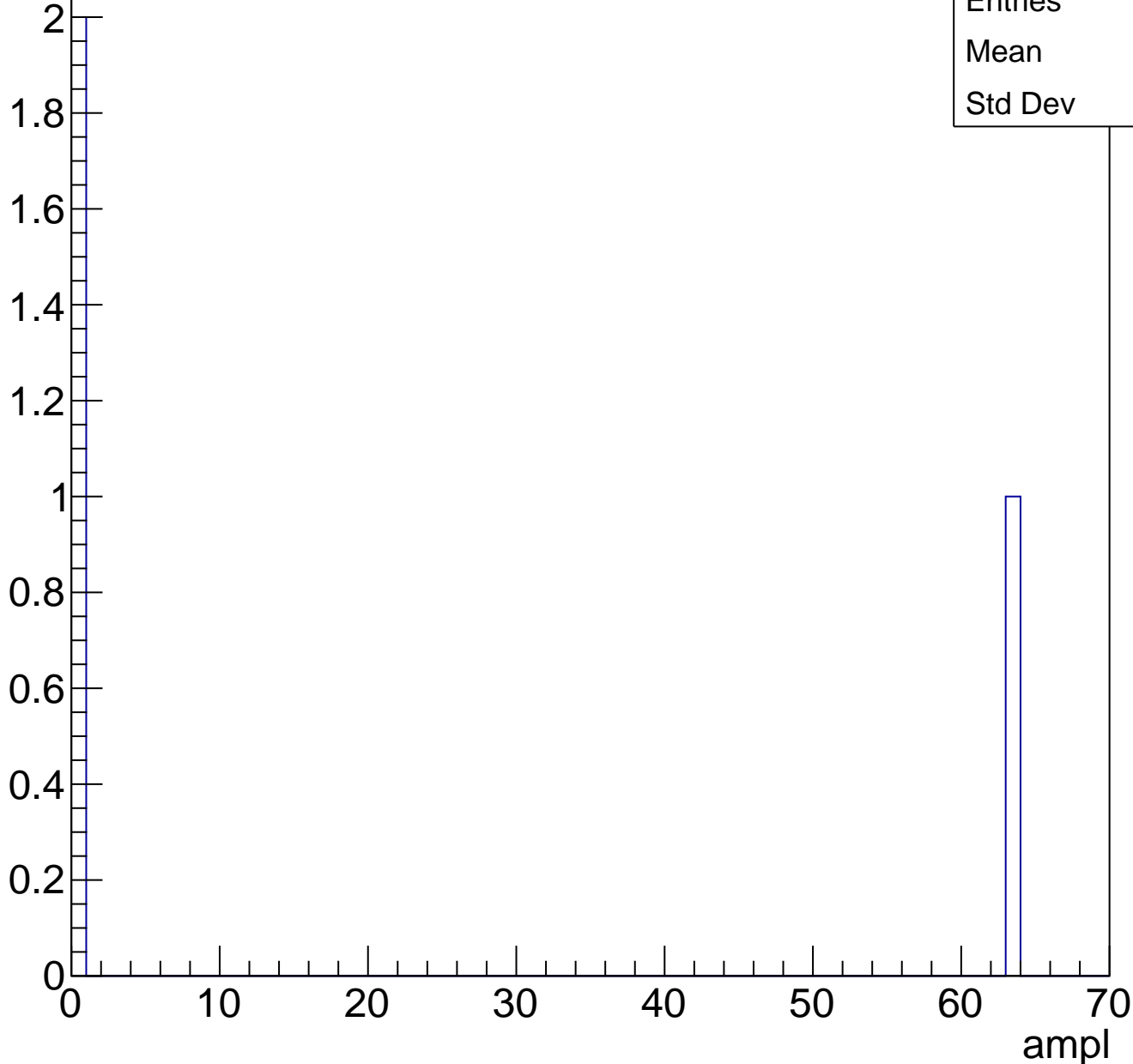




# B1L100S, U2-ch57, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	3
Mean	21
Std Dev	29.7

# B1L100S, U2-ch58, adc0

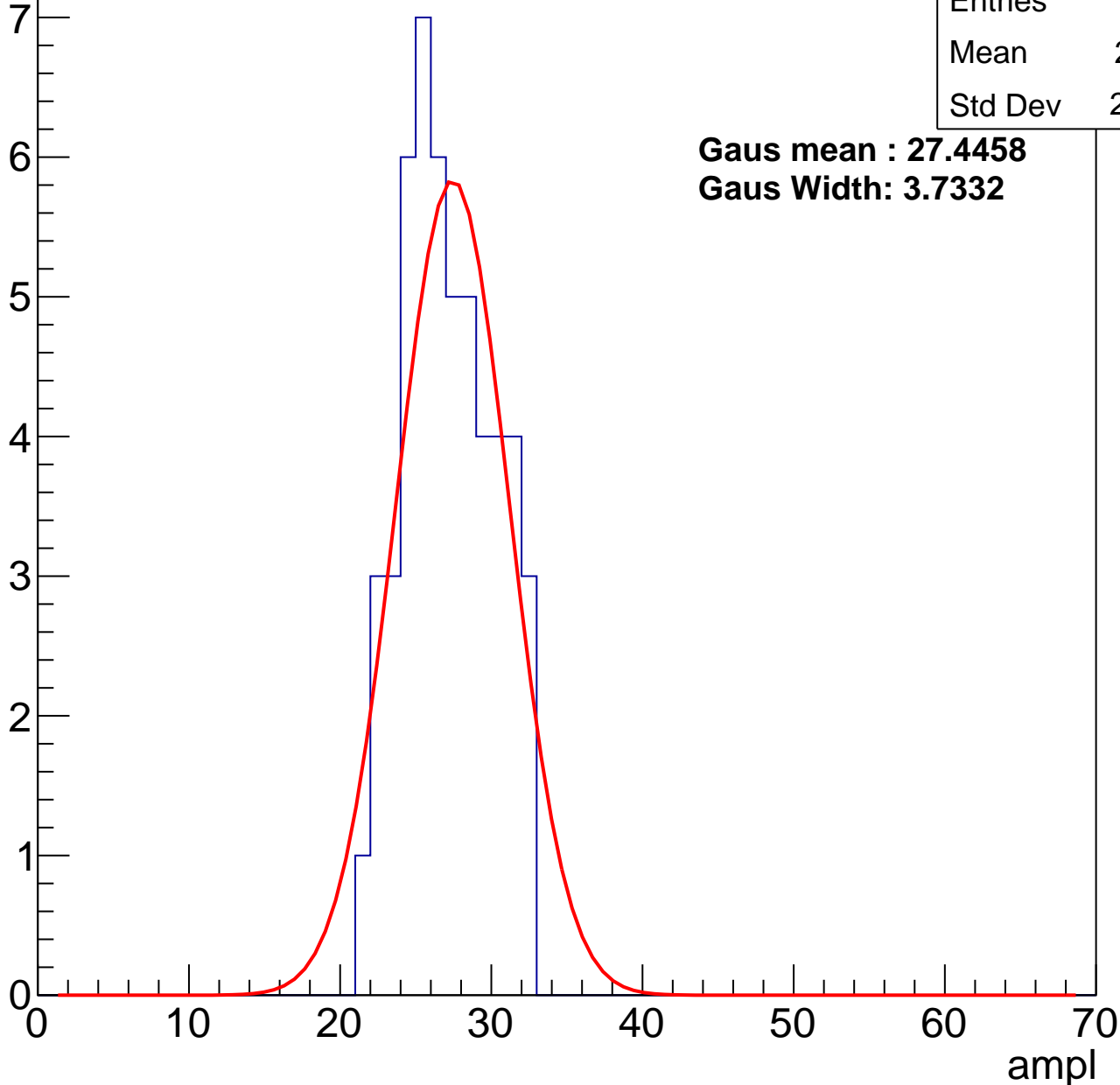
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	51
Mean	26.71
Std Dev	2.933

**Gaus mean : 27.4458**

**Gaus Width: 3.7332**



# B1L100S, U2-ch58, adc1

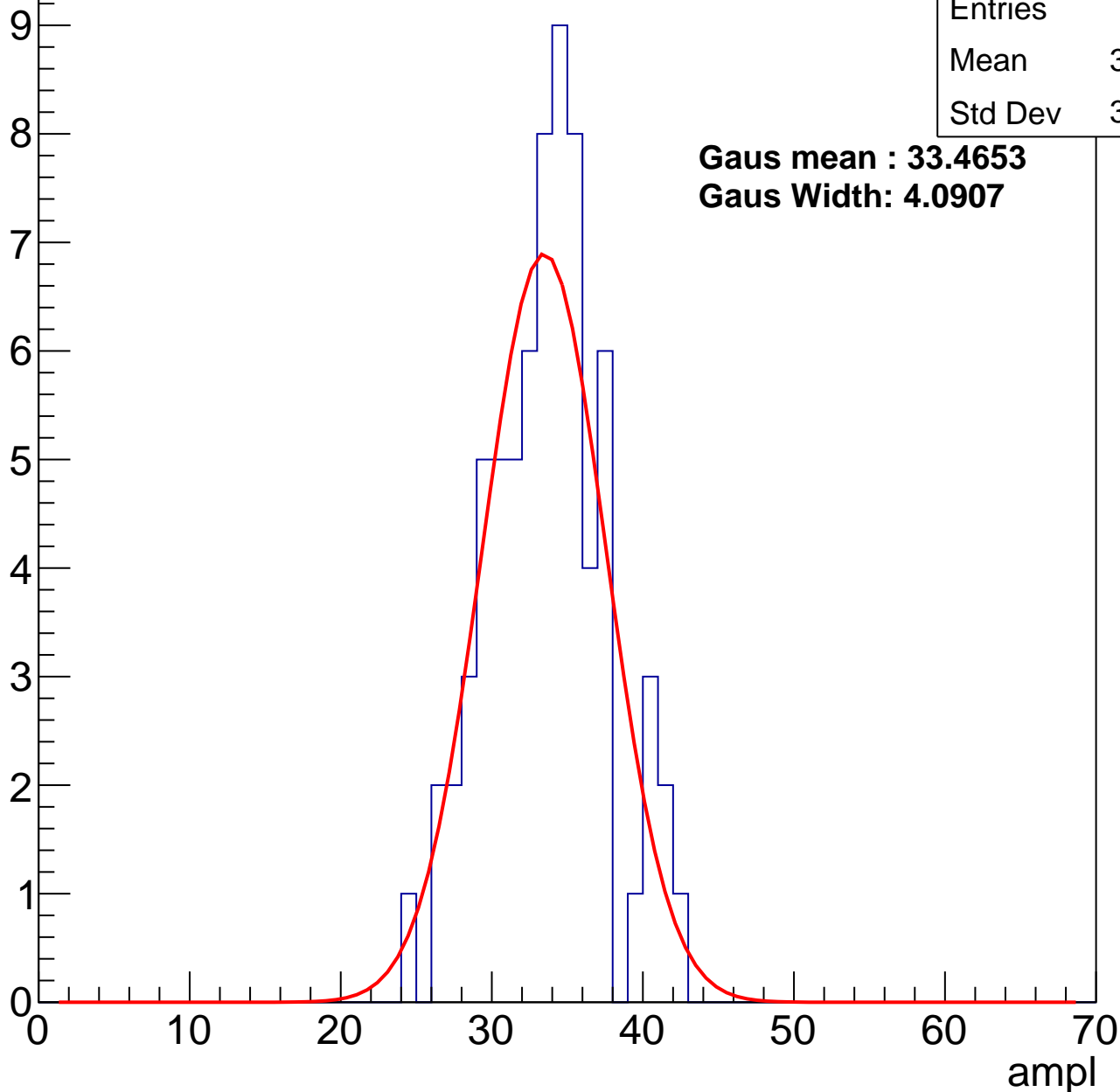
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	71
Mean	33.17
Std Dev	3.827

**Gaus mean : 33.4653**

**Gaus Width: 4.0907**



# B1L100S, U2-ch58, adc2

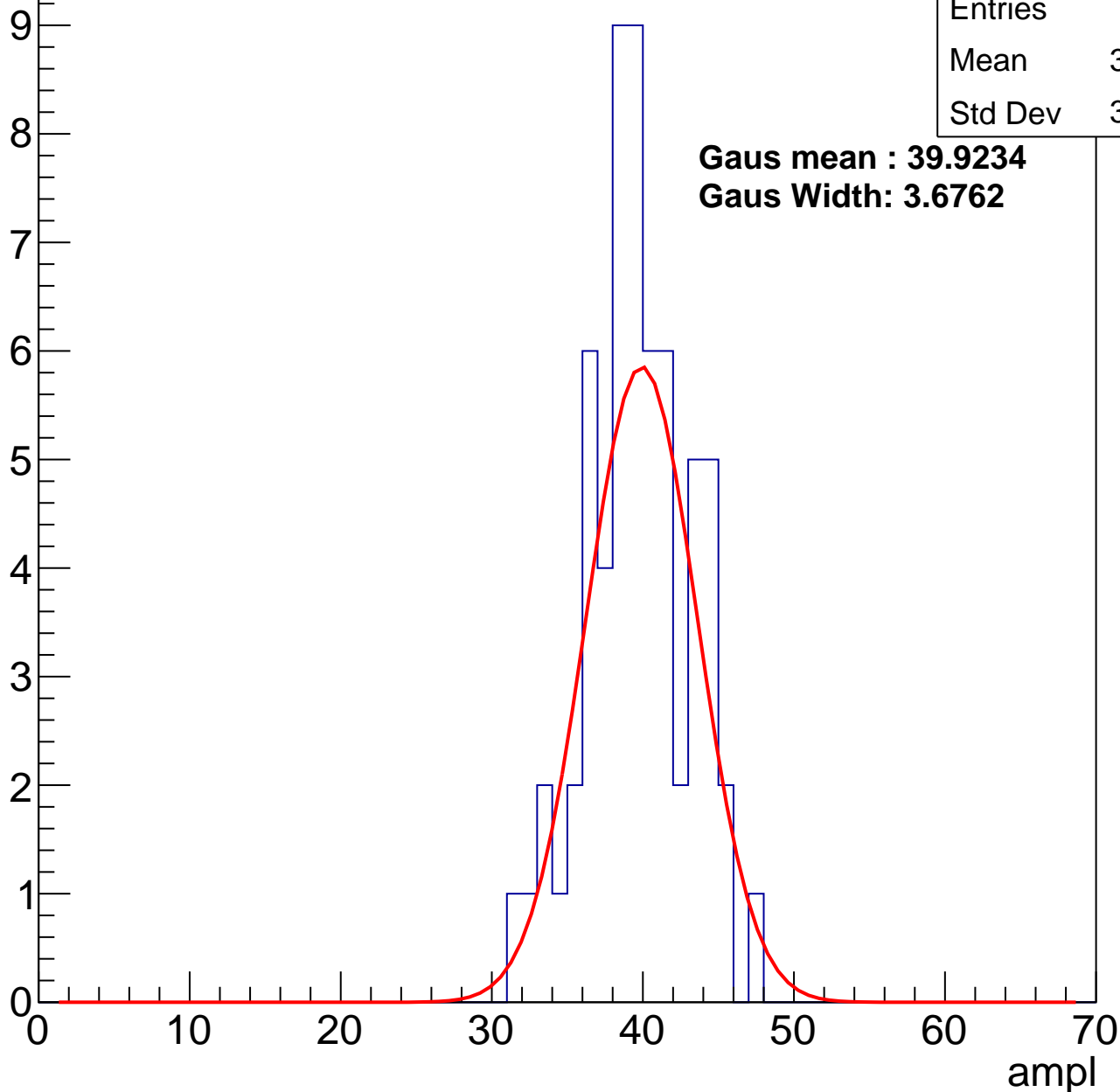
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	62
Mean	39.23
Std Dev	3.376

**Gaus mean : 39.9234**

**Gaus Width: 3.6762**

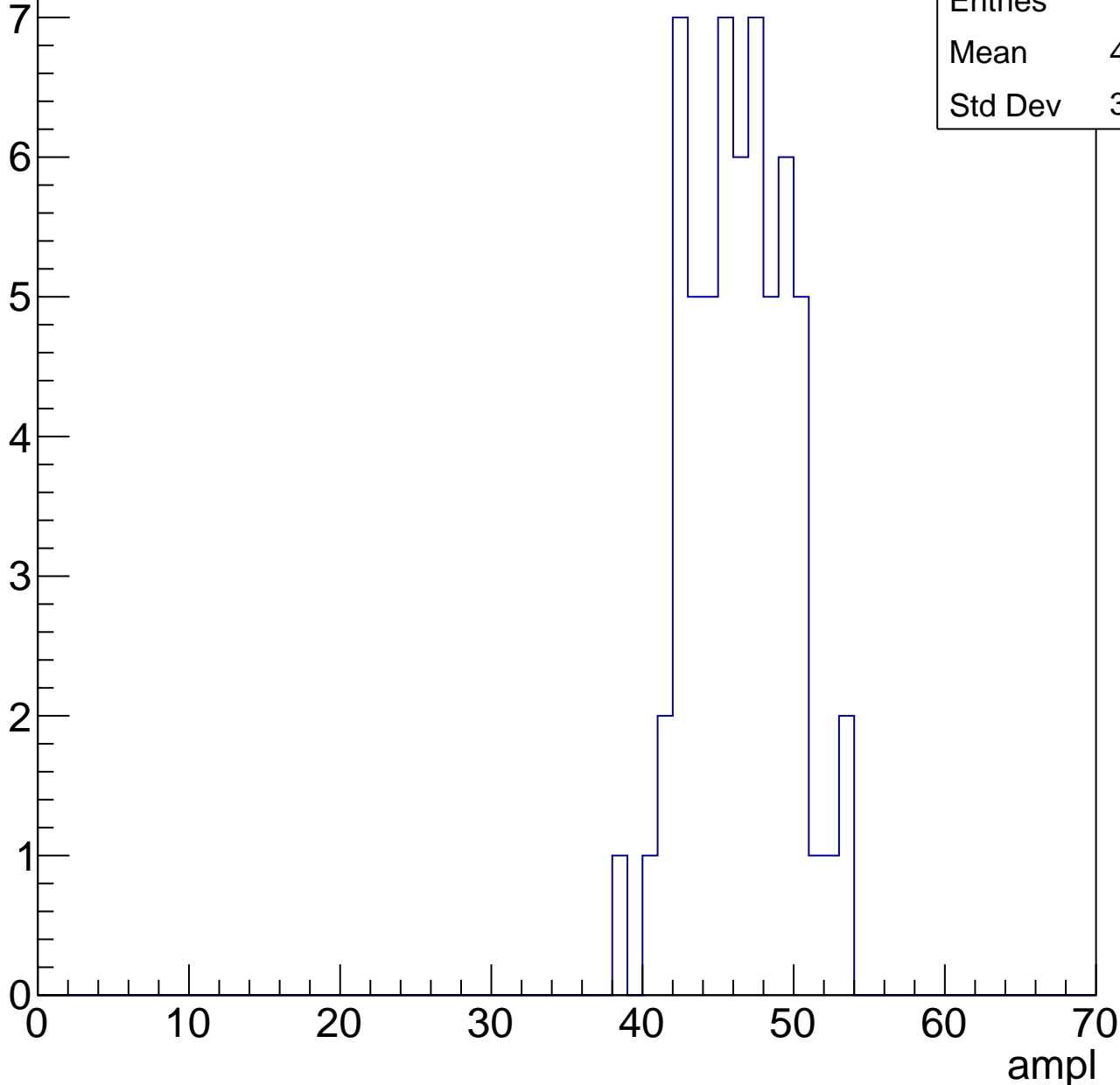


# B1L100S, U2-ch58, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

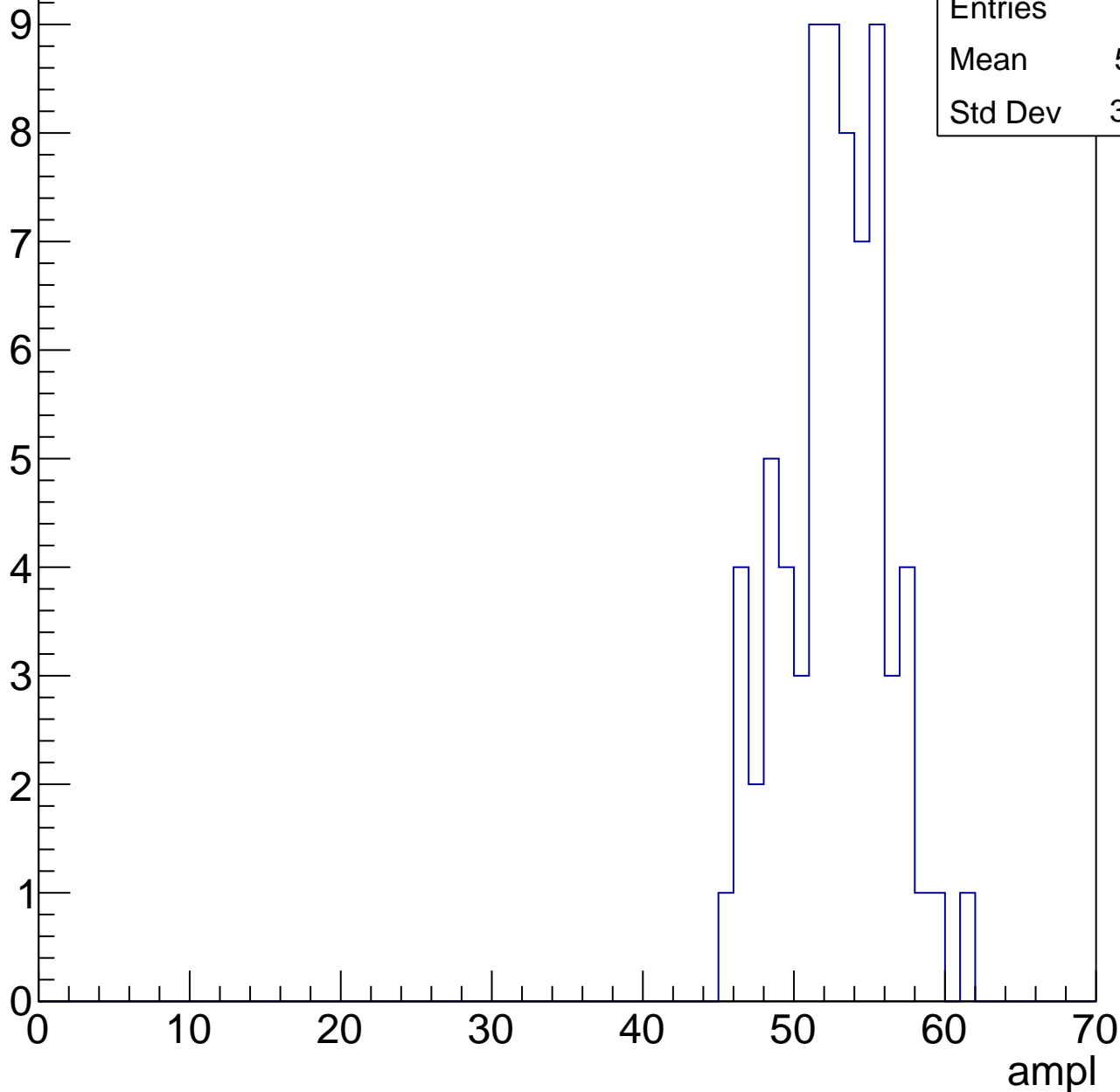
Entries	61
Mean	45.93
Std Dev	3.274



# B1L100S, U2-ch58, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

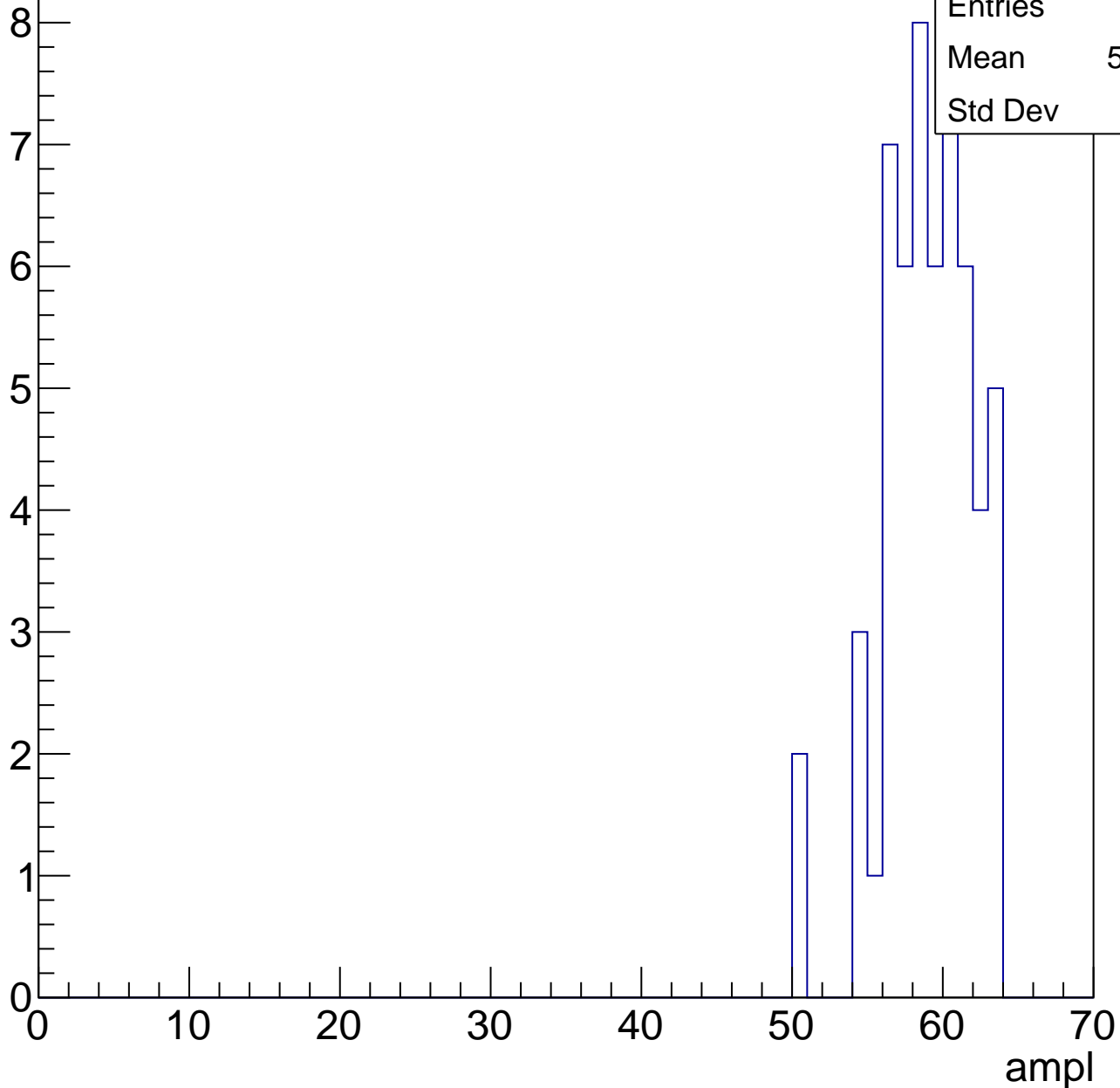
Entry



# B1L100S, U2-ch58, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

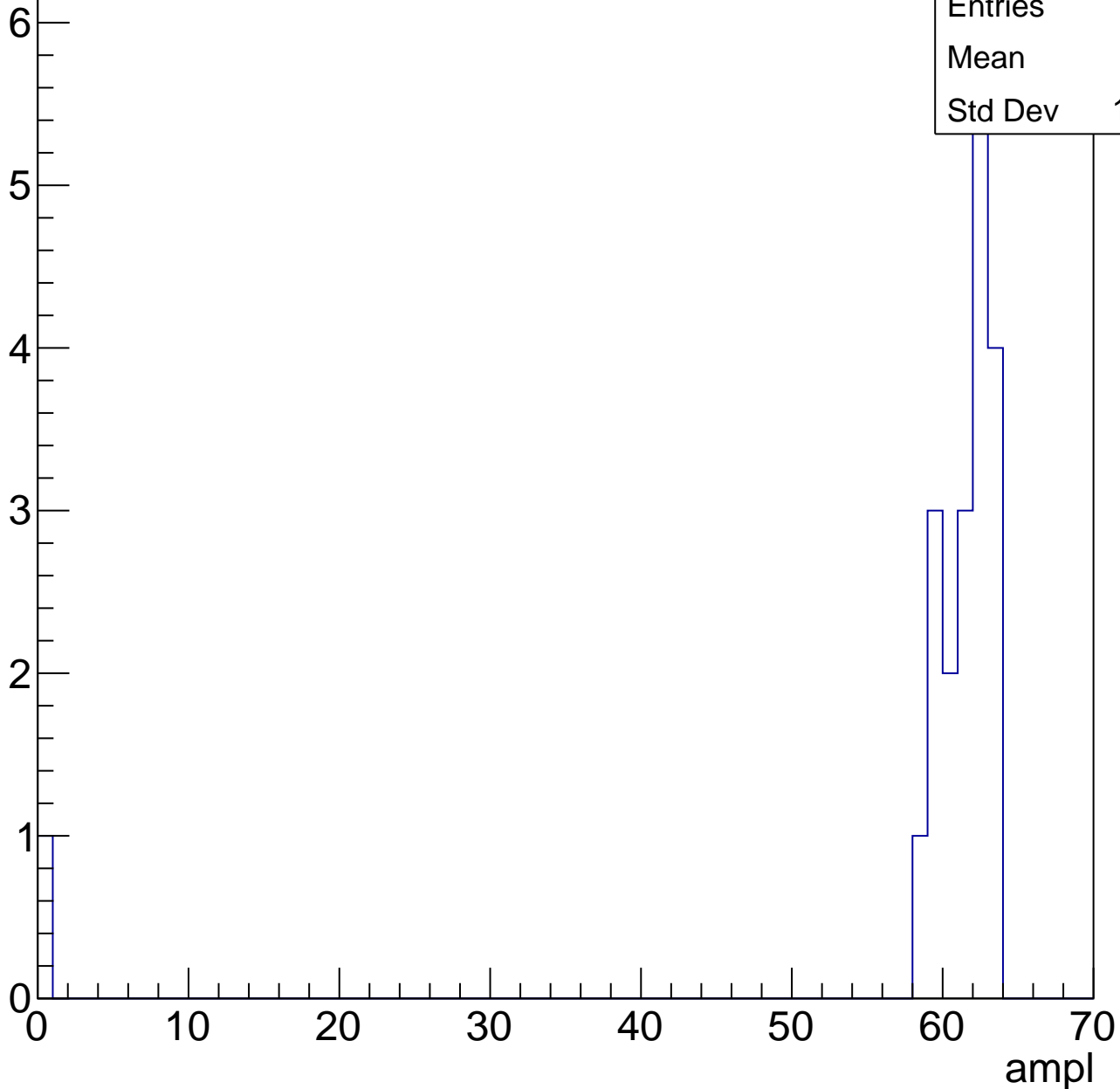


# B1L100S, U2-ch58, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	20
Mean	58.1
Std Dev	13.41





# B1L100S, U2-ch58, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



# B1L100S, U2-ch59, adc0

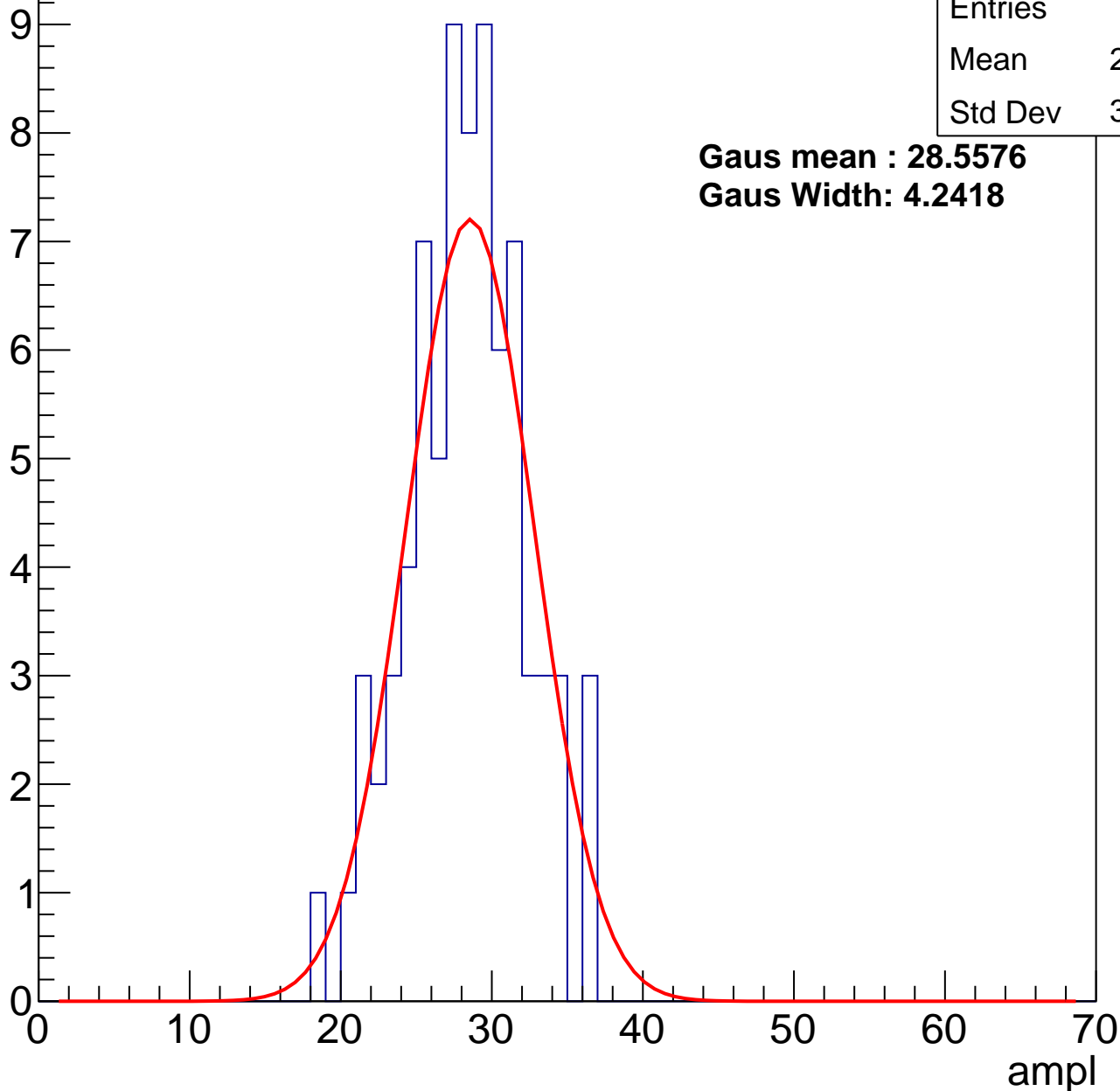
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	77
Mean	27.86
Std Dev	3.833

**Gaus mean : 28.5576**

**Gaus Width: 4.2418**



# B1L100S, U2-ch59, adc1

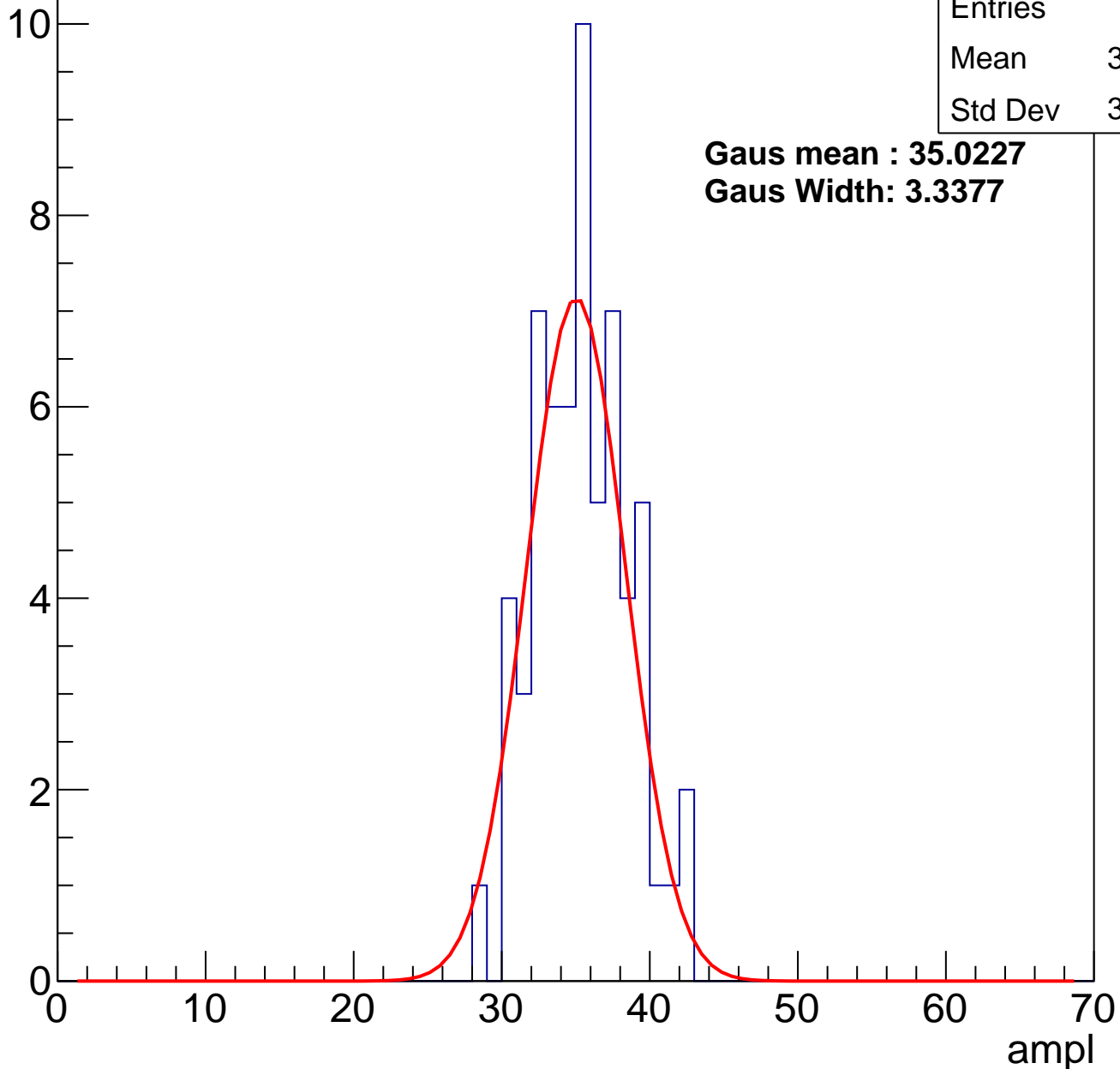
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	62
Mean	34.97
Std Dev	3.105

**Gaus mean : 35.0227**

**Gaus Width: 3.3377**

Entry



# B1L100S, U2-ch59, adc2

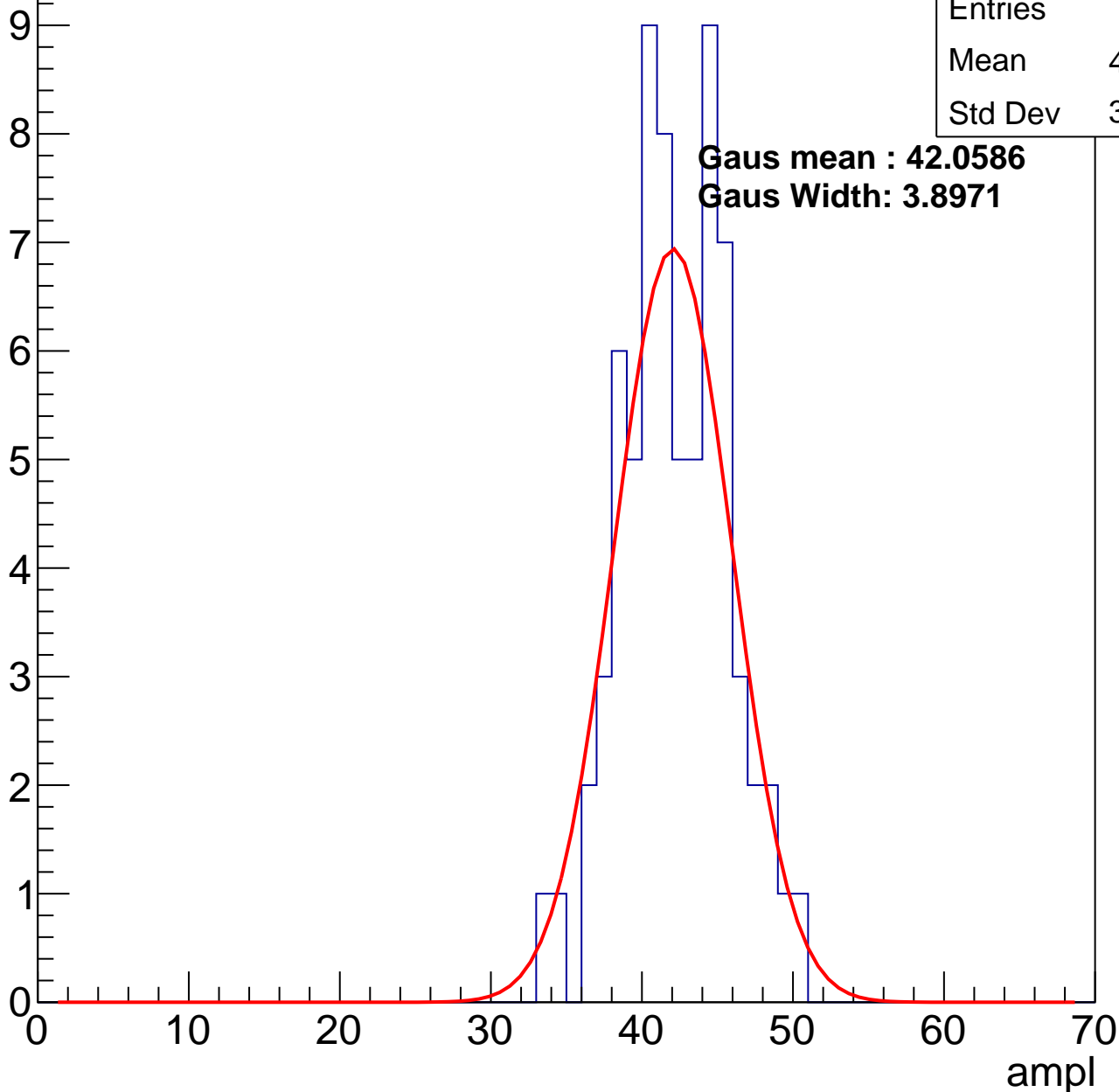
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	70
Mean	41.77
Std Dev	3.506

**Gaus mean : 42.0586**

**Gaus Width: 3.8971**

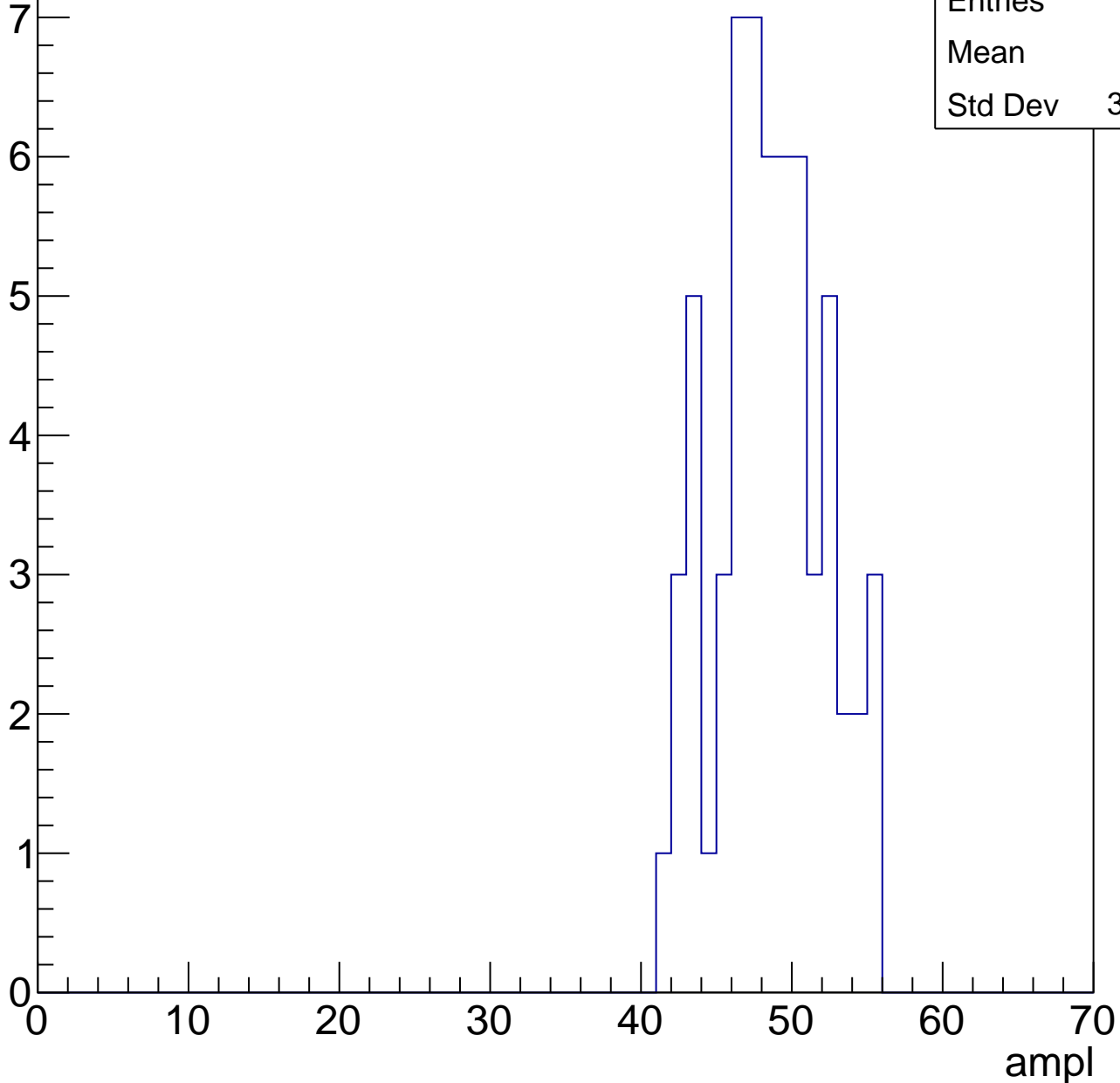


# B1L100S, U2-ch59, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	60
Mean	48.1
Std Dev	3.572

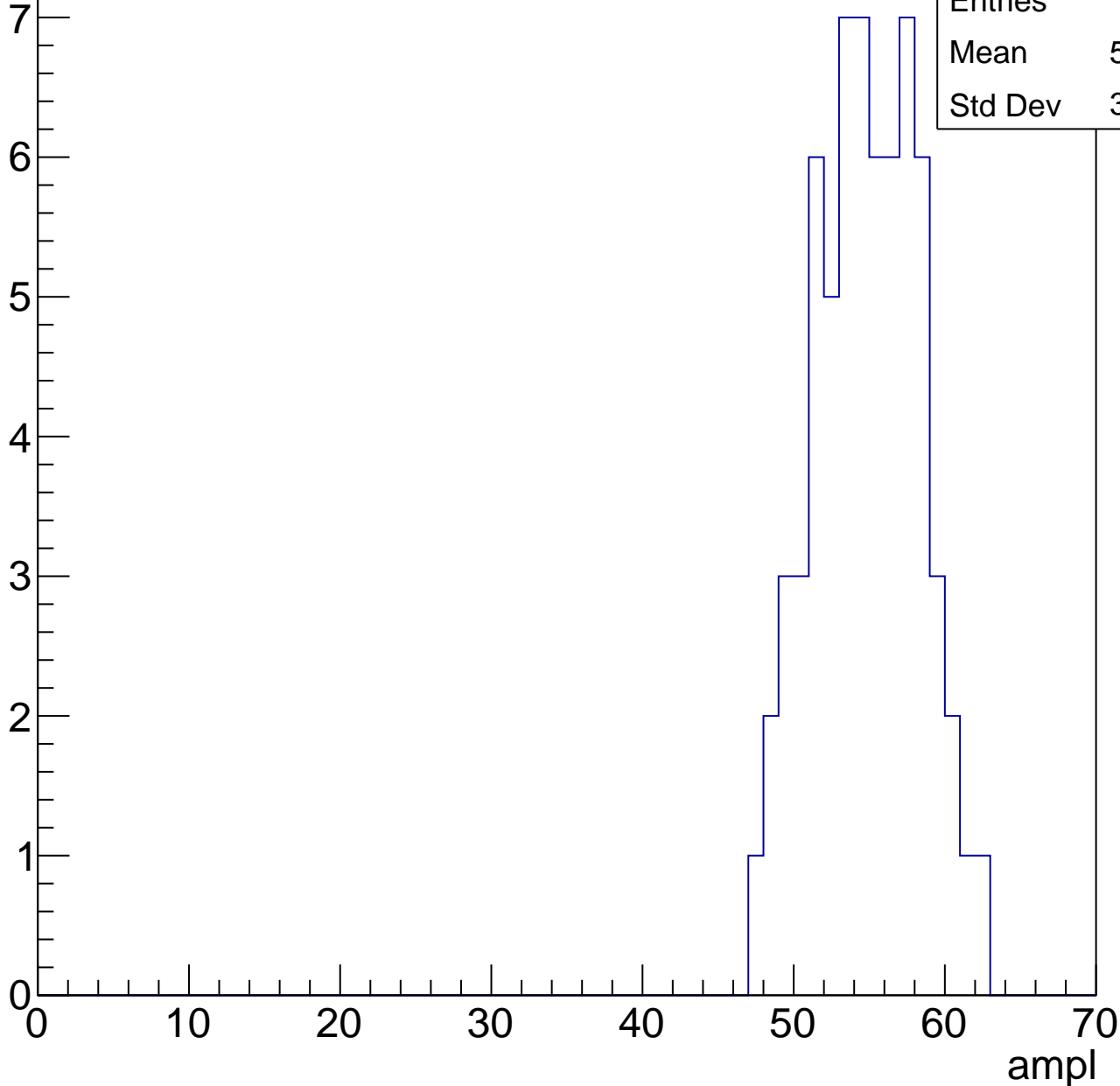


# B1L100S, U2-ch59, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	66
Mean	54.36
Std Dev	3.405

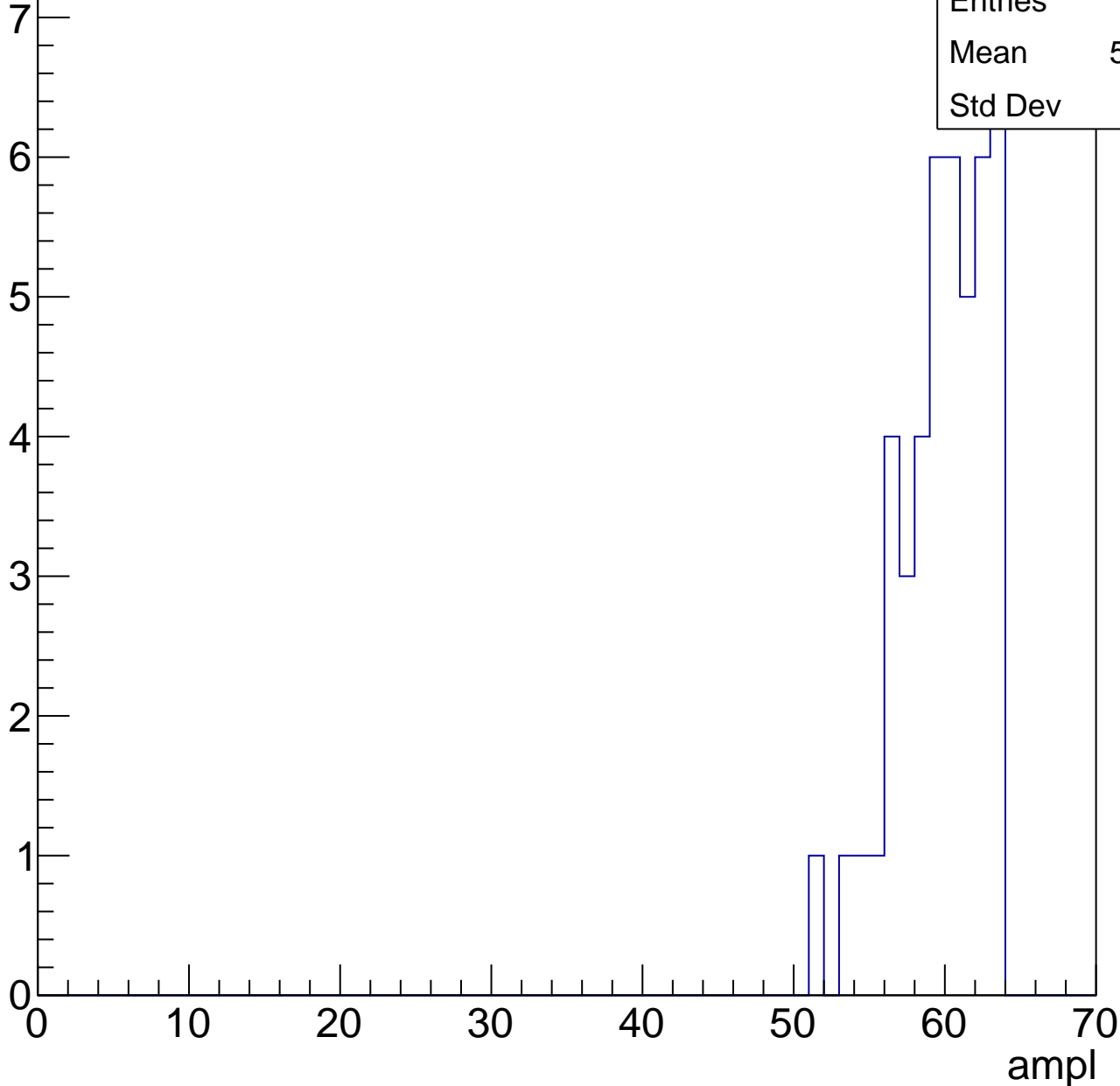


# B1L100S, U2-ch59, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

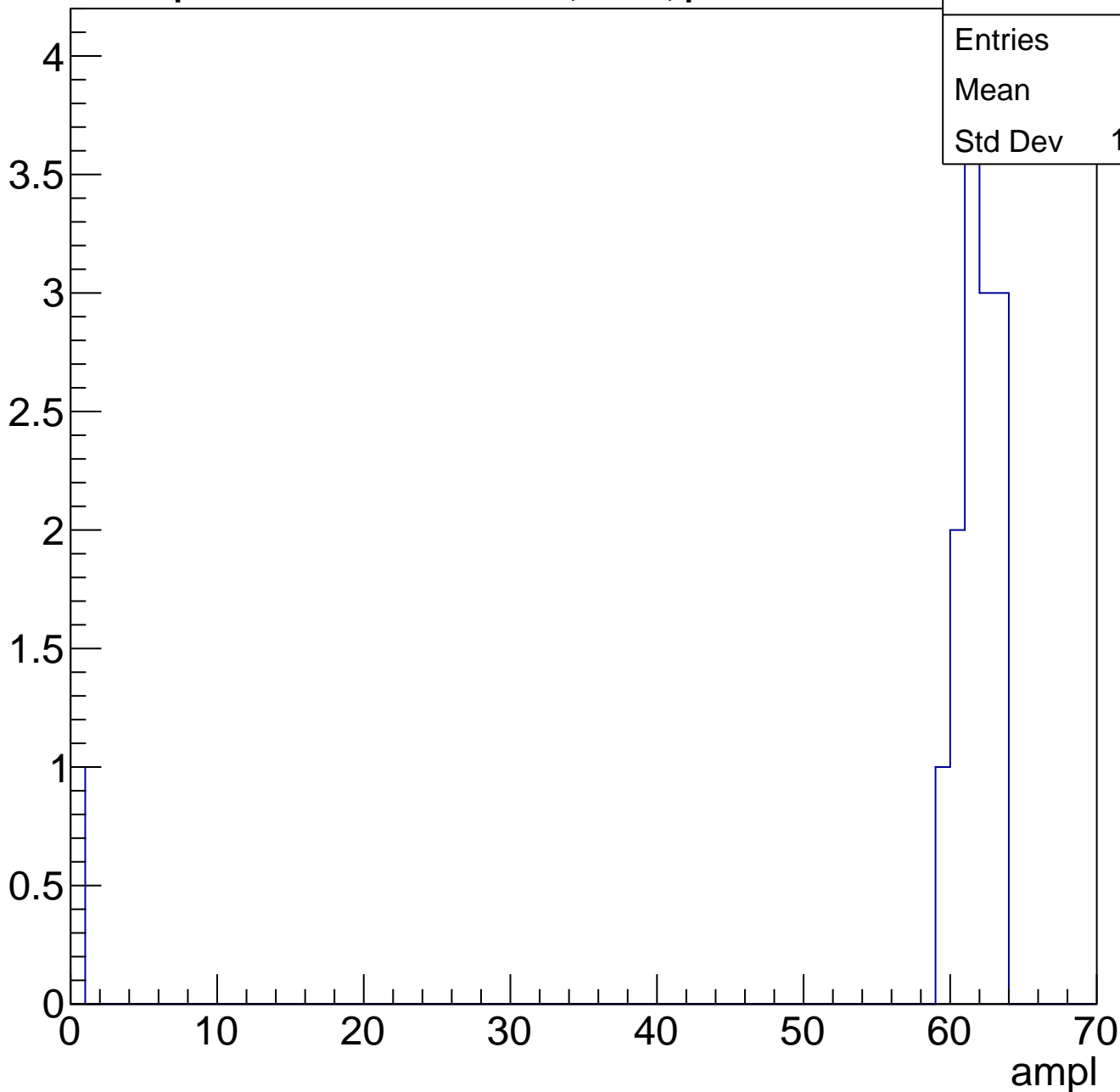
Entries	45
Mean	59.38
Std Dev	2.9



# B1L100S, U2-ch59, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry





# B1L100S, U2-ch59, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L100S, U2-ch60, adc0

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	69
Mean	29.03
Std Dev	3.497

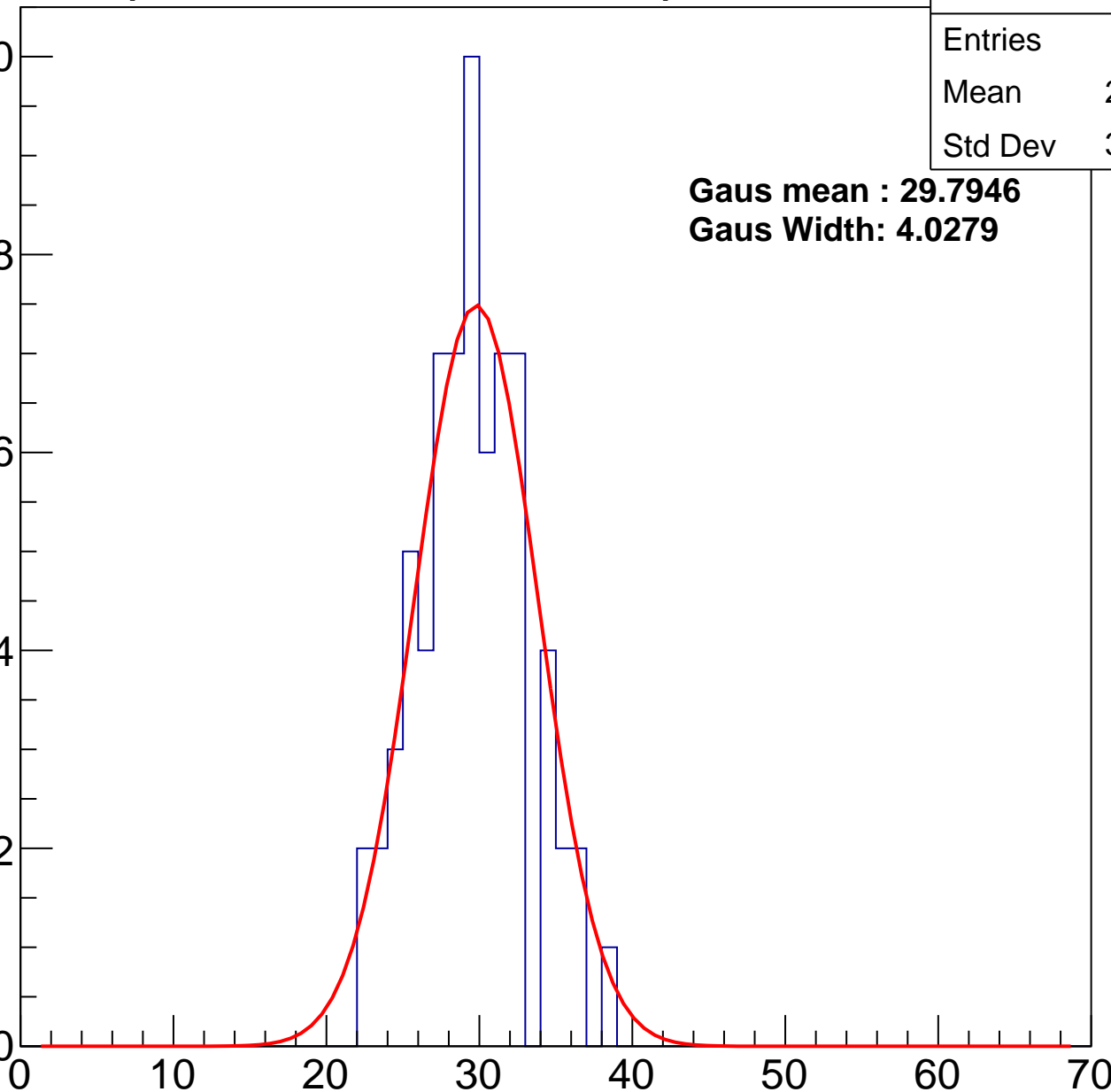
**Gaus mean : 29.7946**

**Gaus Width: 4.0279**

Entry

10  
8  
6  
4  
2  
0

ampl



# B1L100S, U2-ch60, adc1

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	59
Mean	34.97
Std Dev	3.226

**Gaus mean : 35.4365**

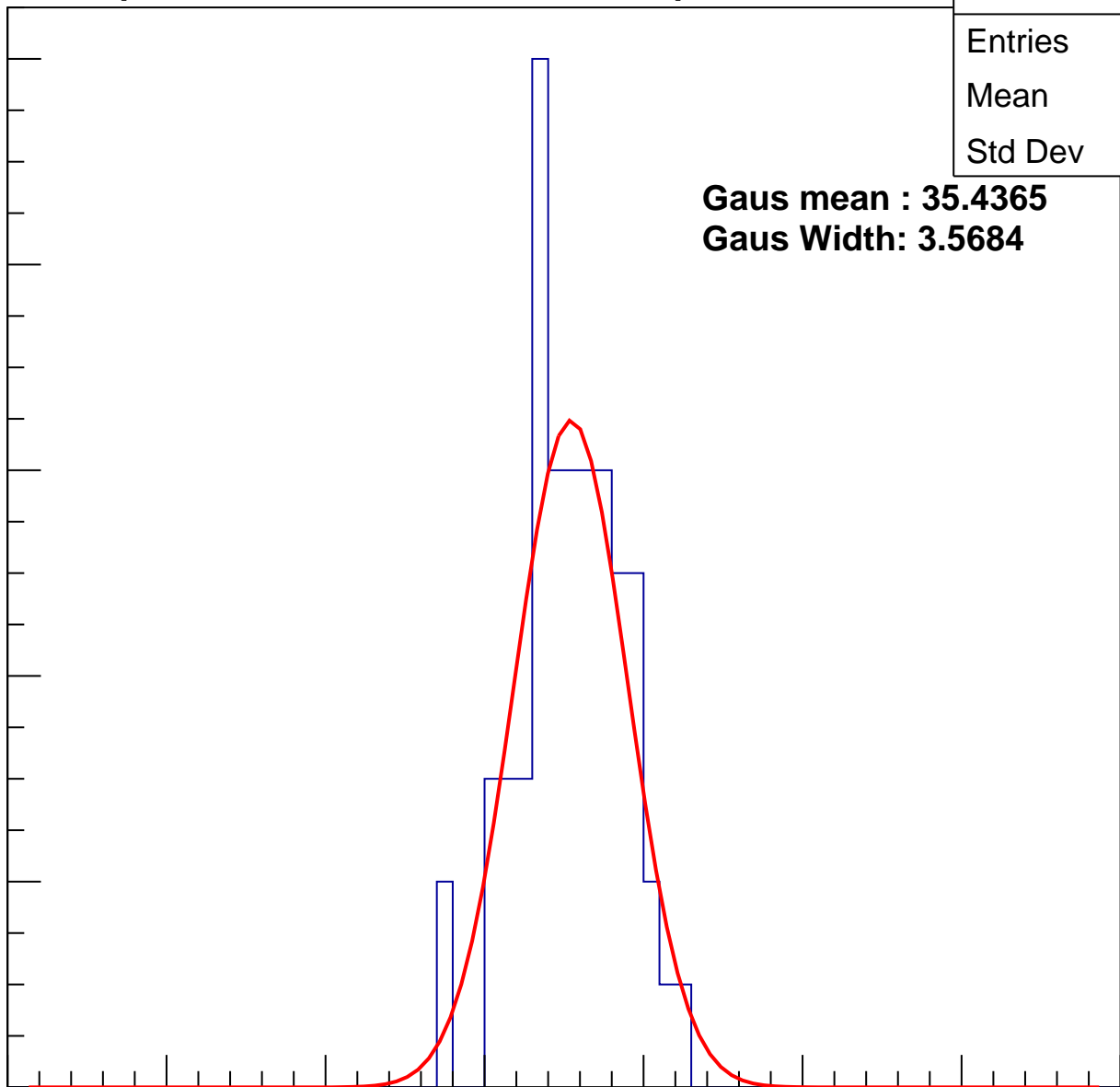
**Gaus Width: 3.5684**

Entry

10  
8  
6  
4  
2  
0

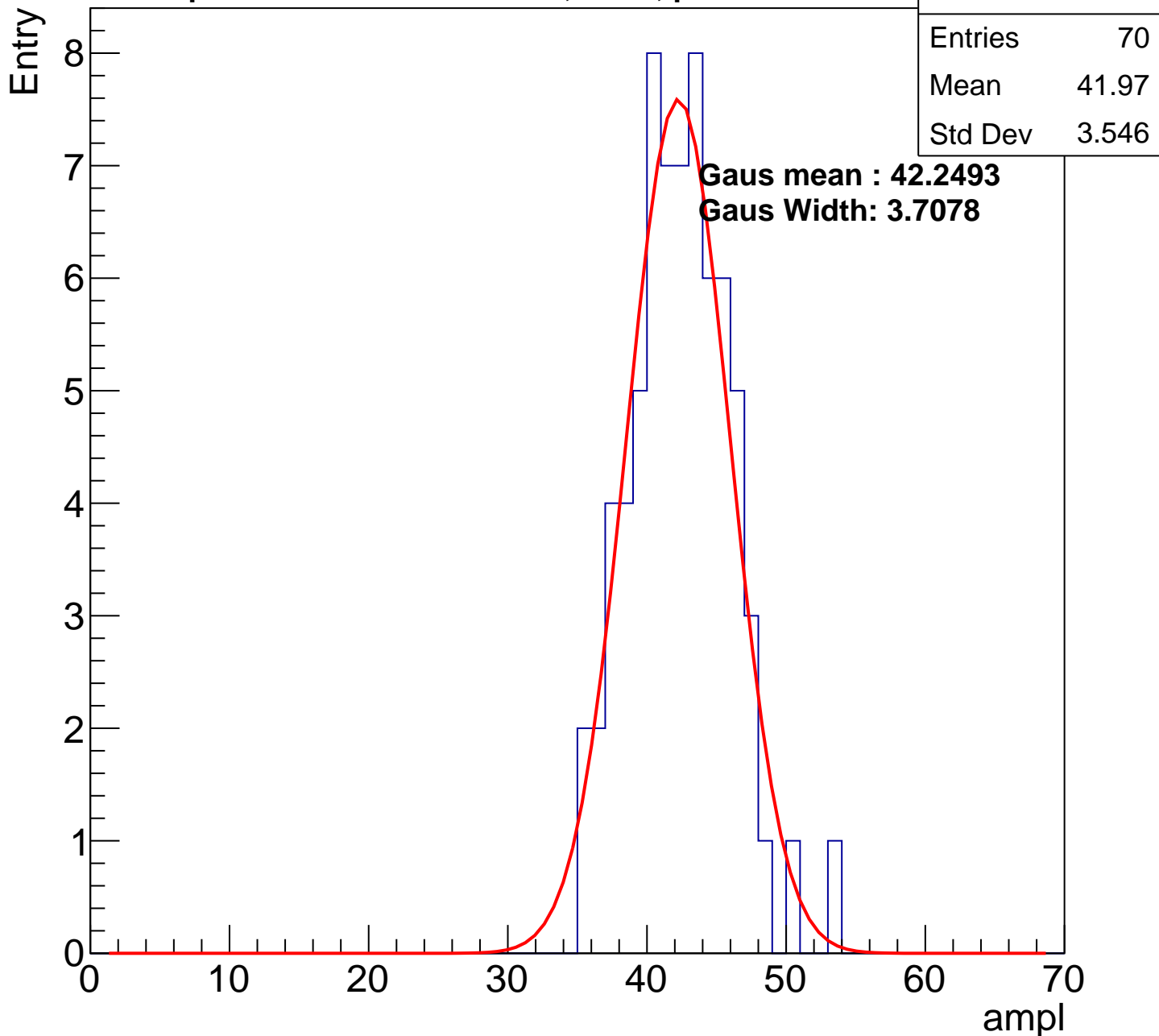
ampl

0 10 20 30 40 50 60 70



# B1L100S, U2-ch60, adc2

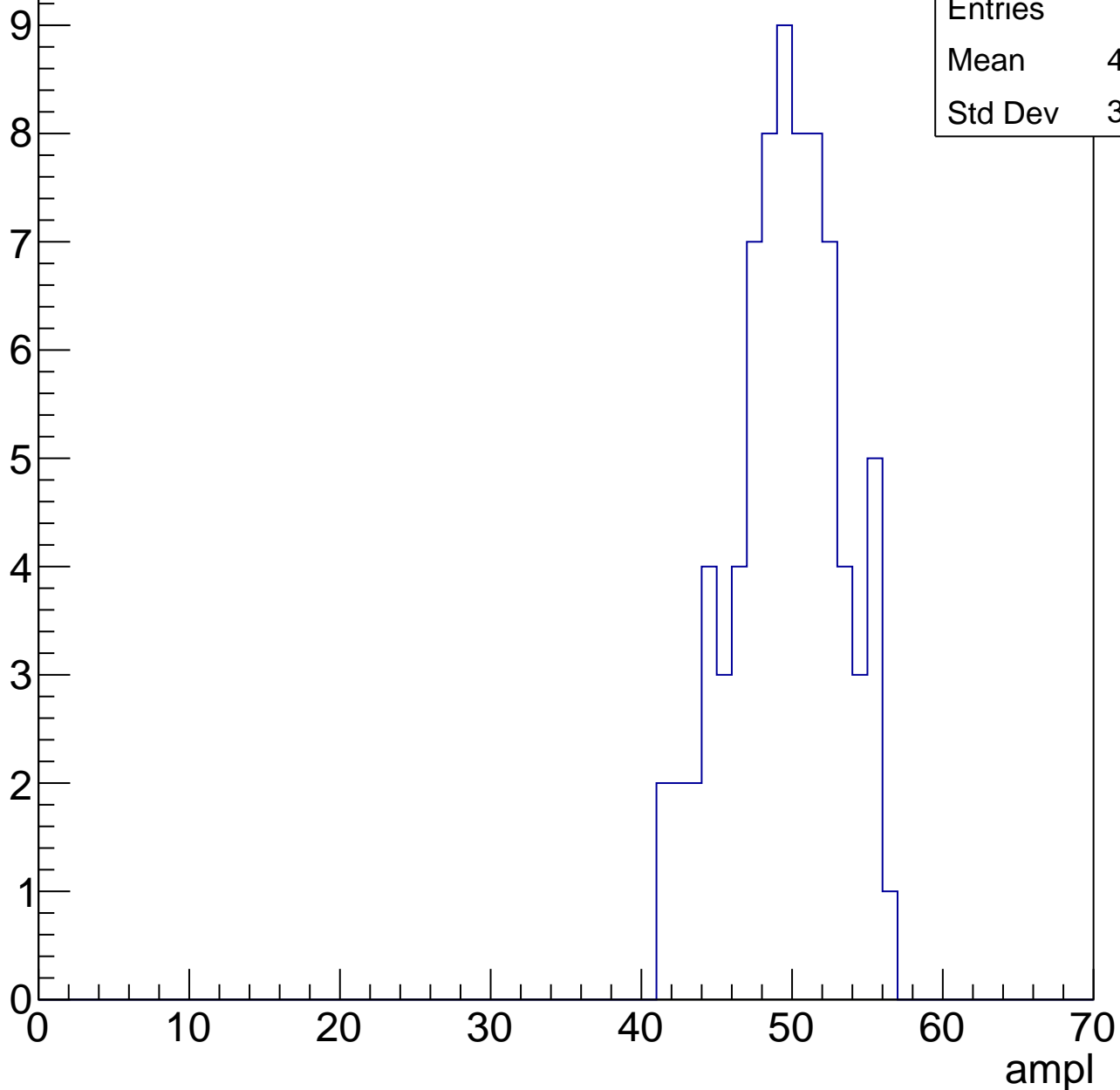
calib\_packv5\_042523\_0143.root, FC#4, port A2



# B1L100S, U2-ch60, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

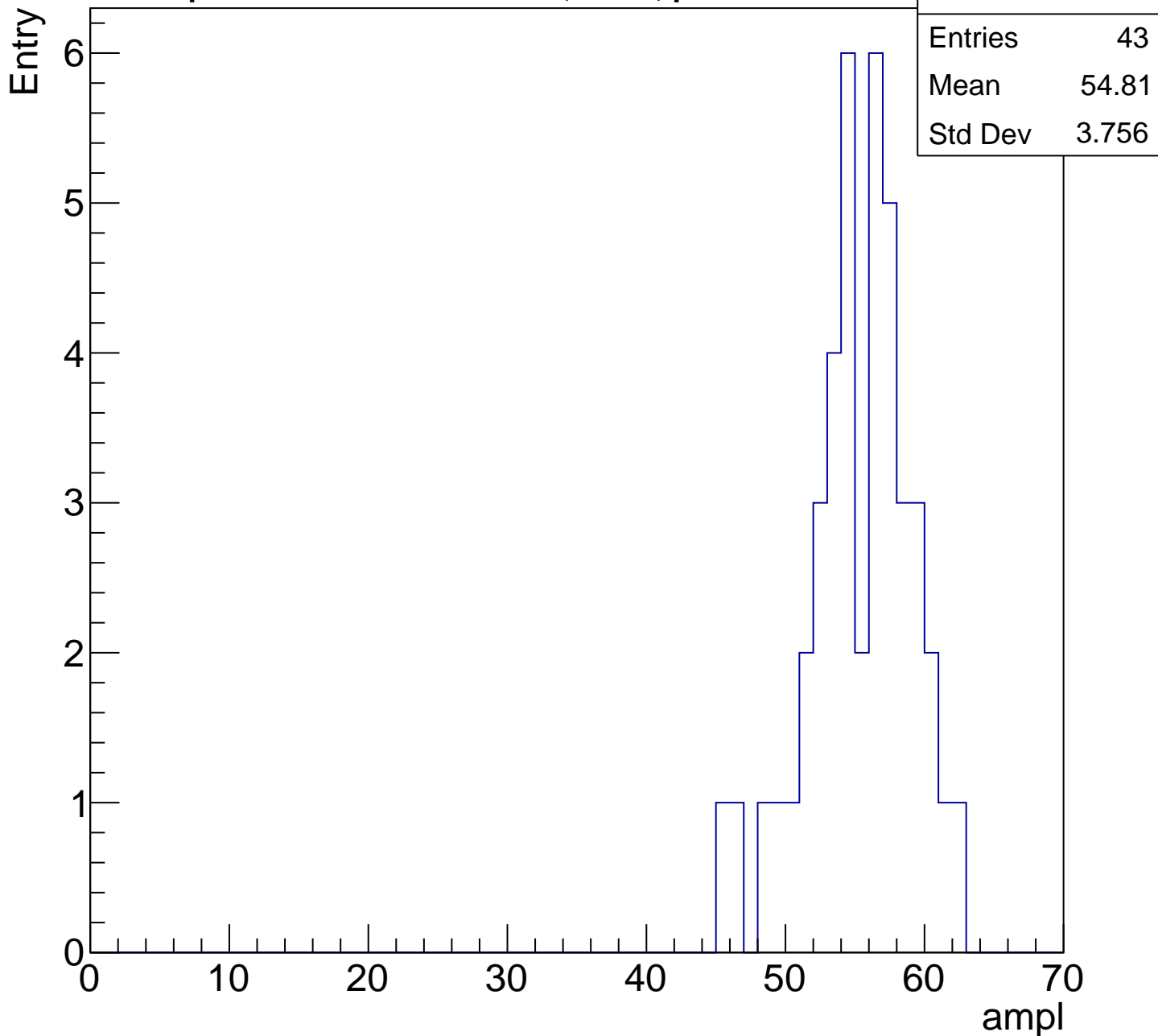
Entry



Entries	77
Mean	49.06
Std Dev	3.583

# B1L100S, U2-ch60, adc4

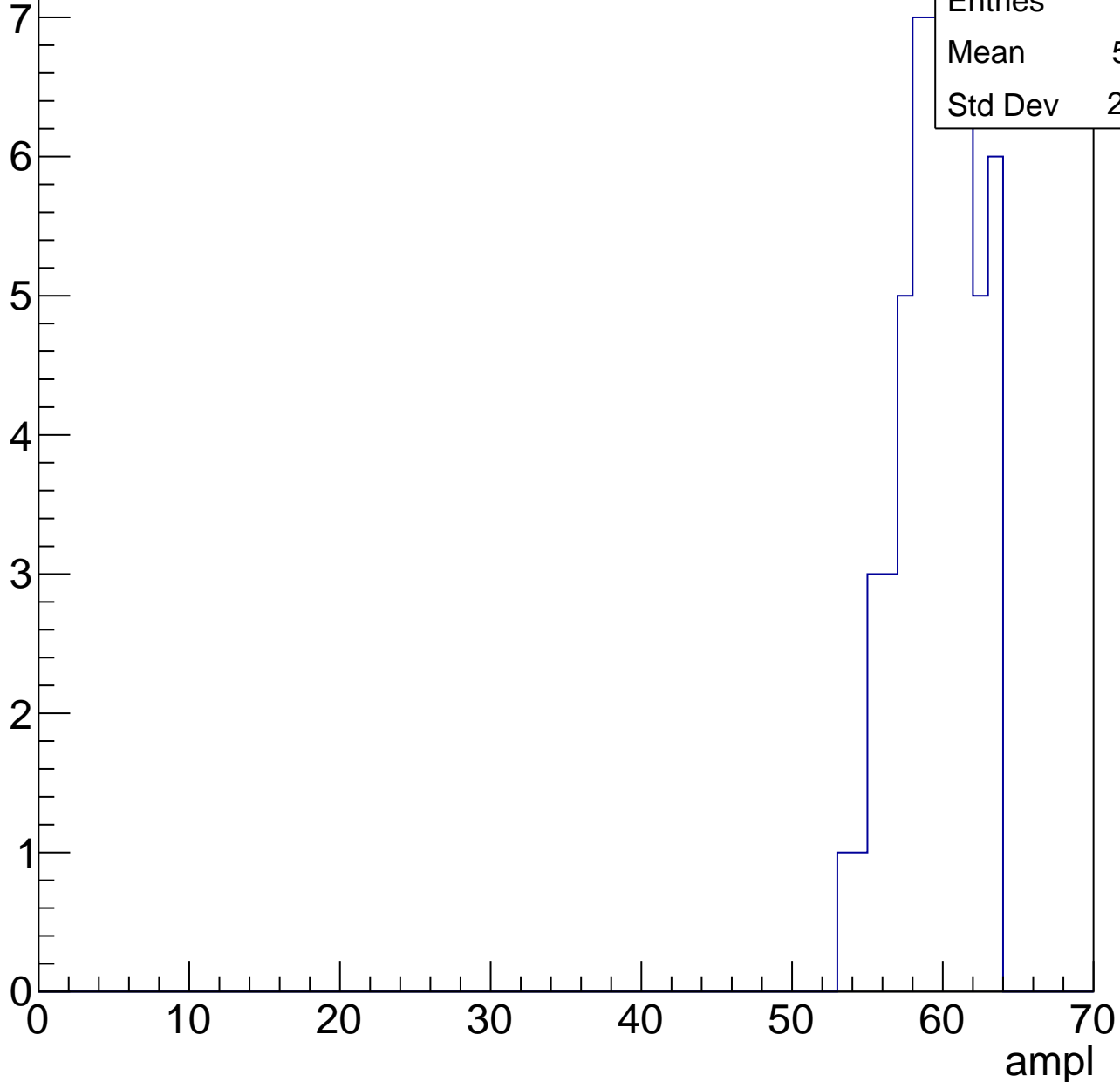
calib\_packv5\_042523\_0143.root, FC#4, port A2



# B1L100S, U2-ch60, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

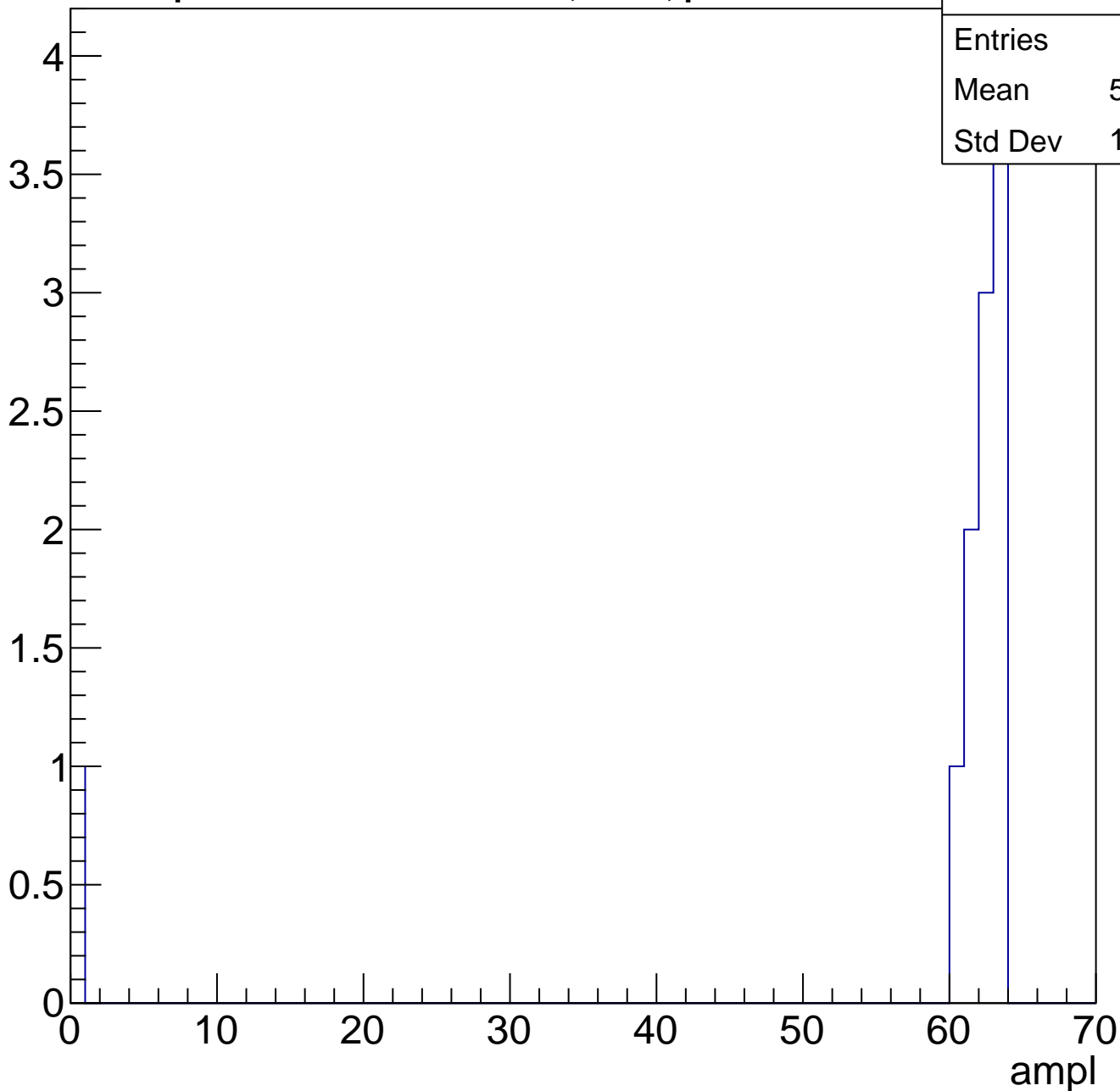
Entry



# B1L100S, U2-ch60, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

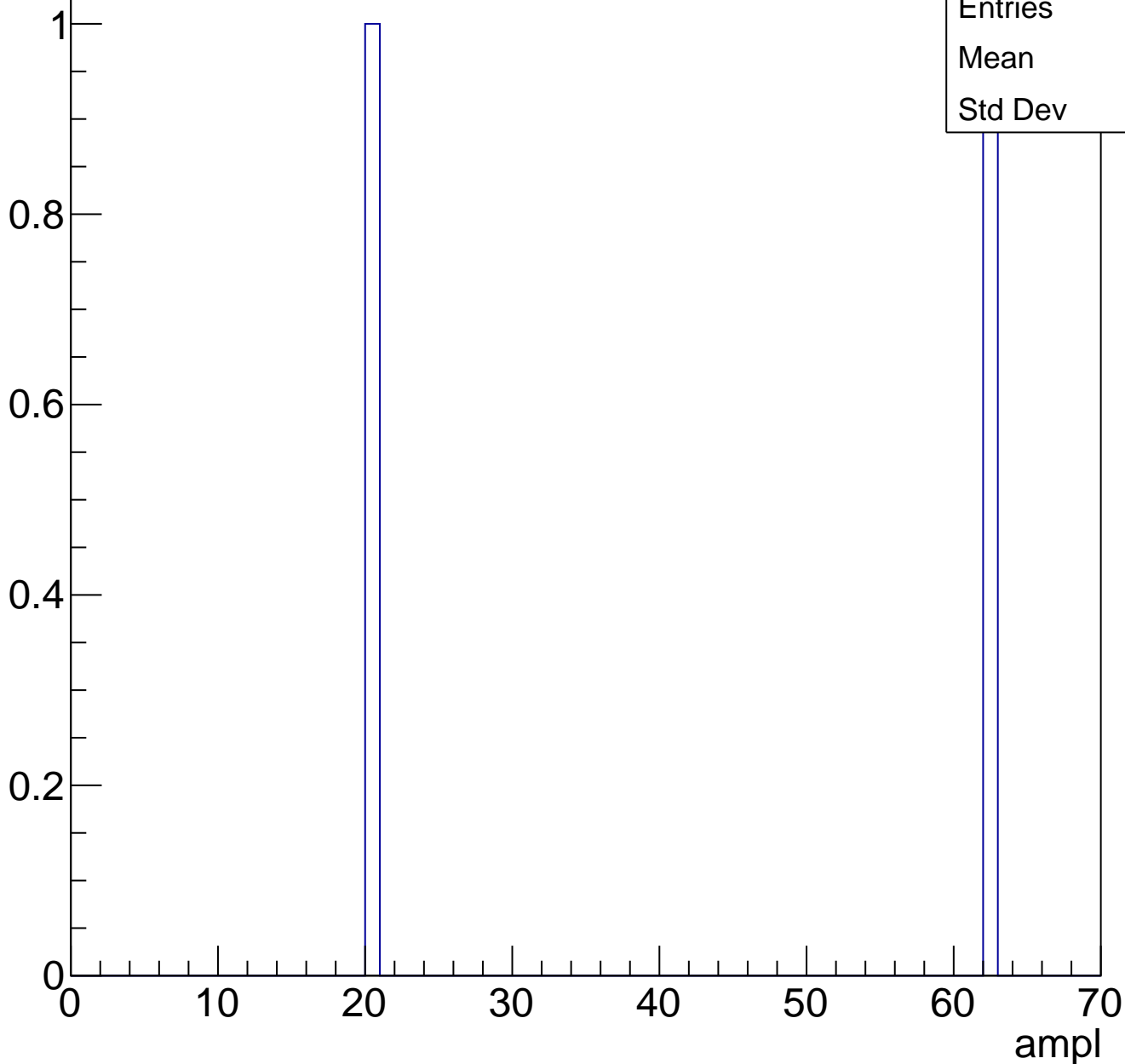




# B1L100S, U2-ch60, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



# B1L100S, U2-ch61, adc0

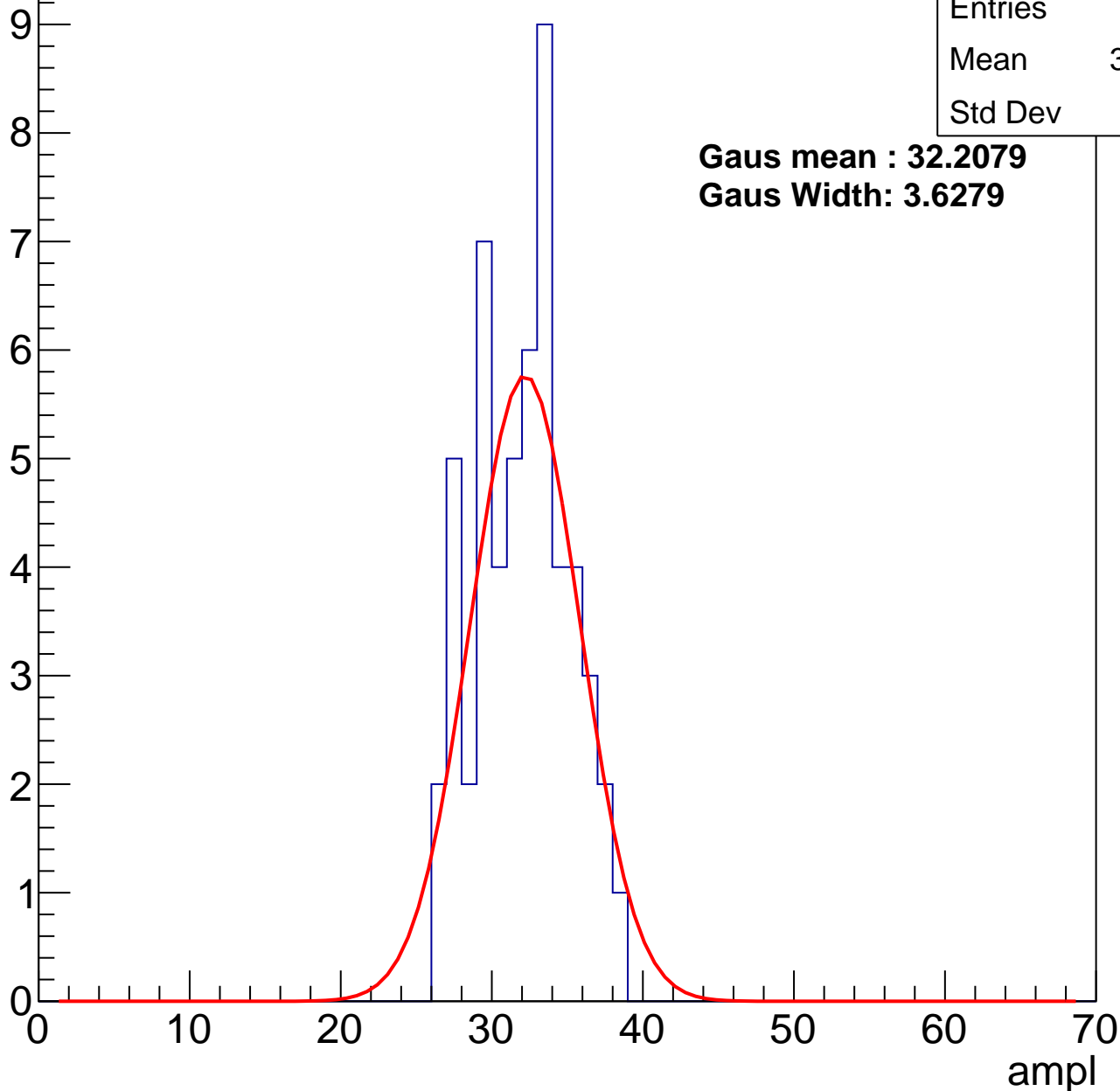
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	54
Mean	31.59
Std Dev	3.04

**Gaus mean : 32.2079**

**Gaus Width: 3.6279**



# B1L100S, U2-ch61, adc1

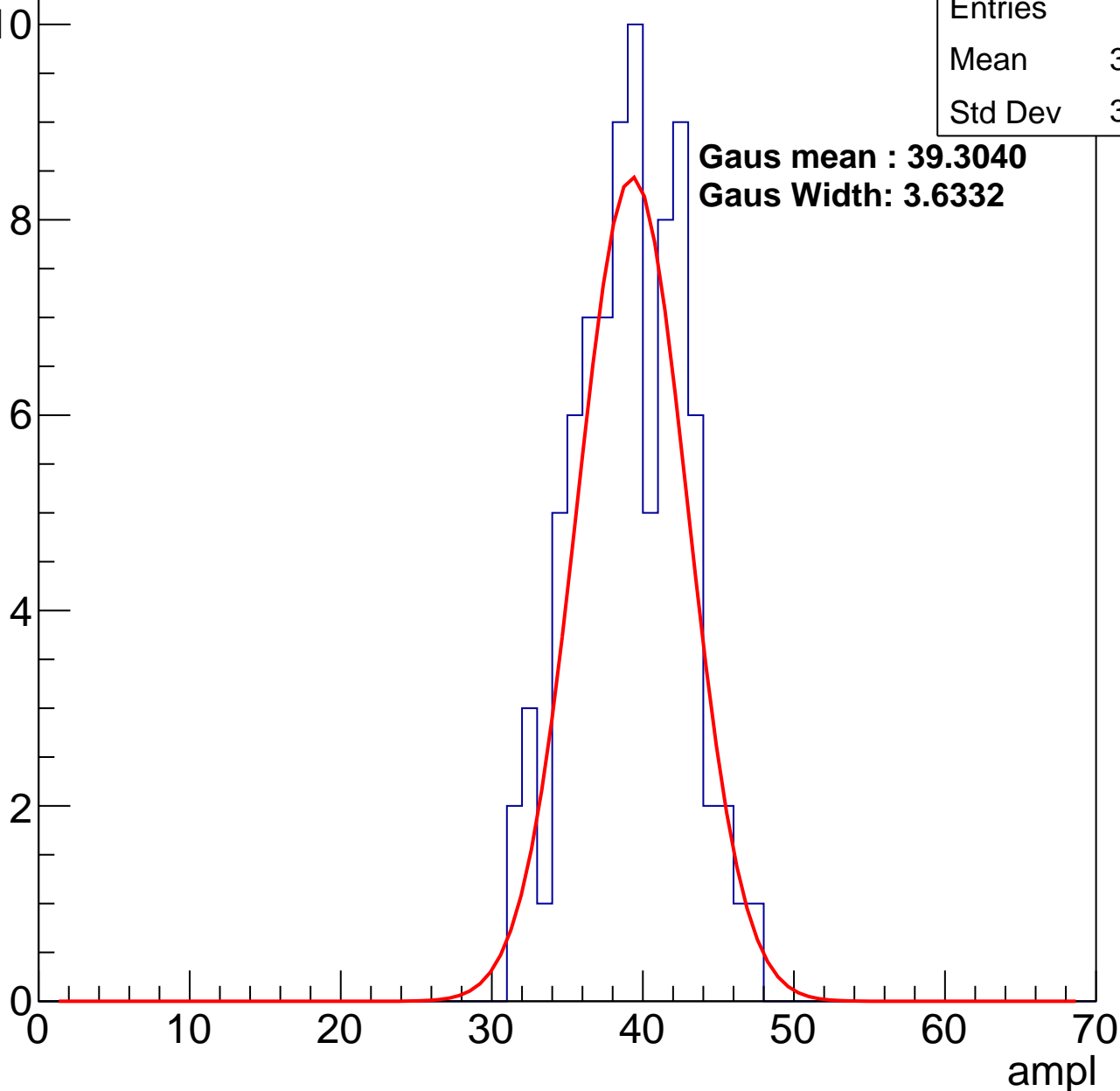
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	84
Mean	38.68
Std Dev	3.573

**Gaus mean : 39.3040**

**Gaus Width: 3.6332**



# B1L100S, U2-ch61, adc2

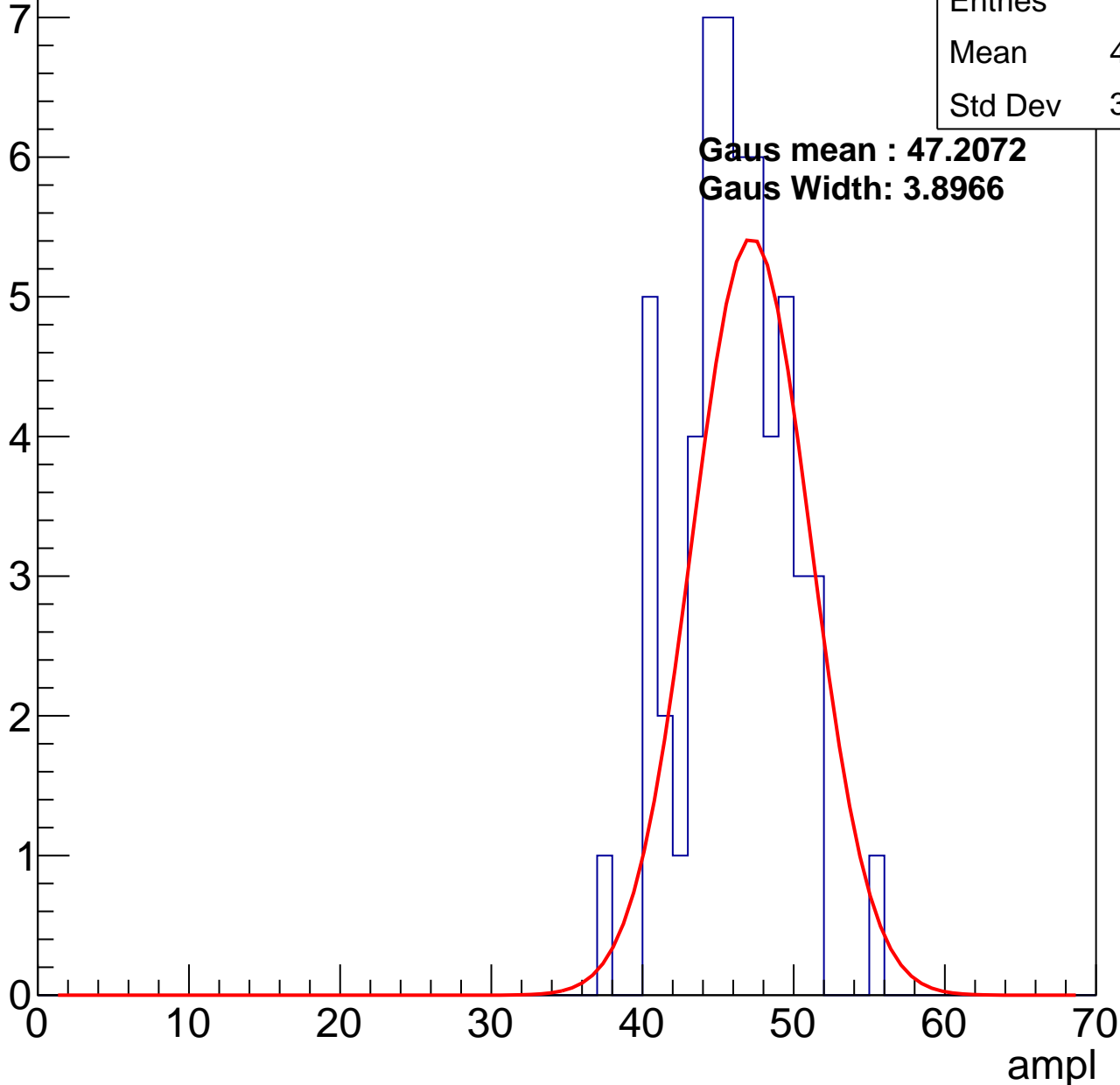
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	55
Mean	45.62
Std Dev	3.467

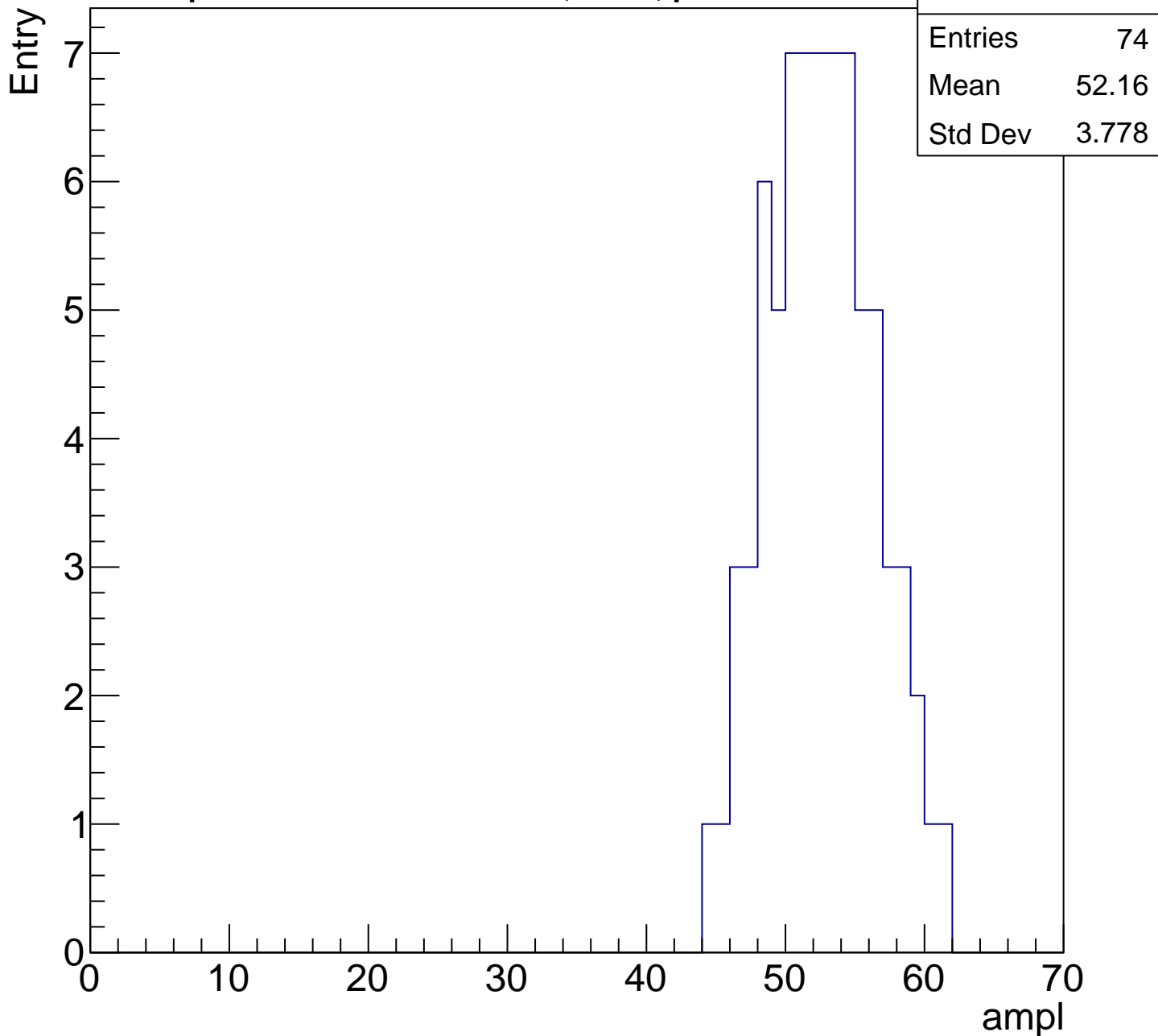
**Gaus mean : 47.2072**

**Gaus Width: 3.8966**



# B1L100S, U2-ch61, adc3

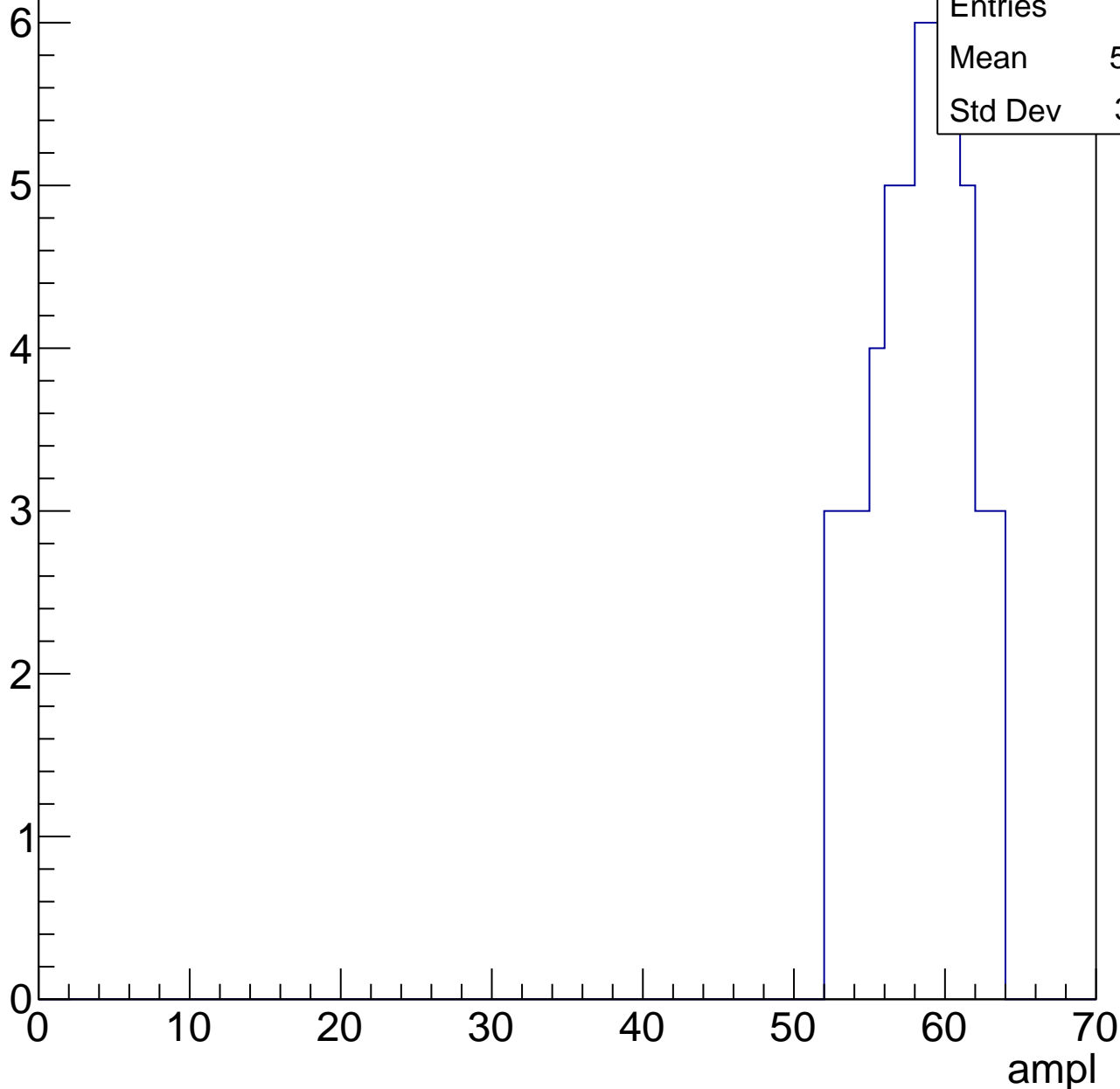
calib\_packv5\_042523\_0143.root, FC#4, port A2



# B1L100S, U2-ch61, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

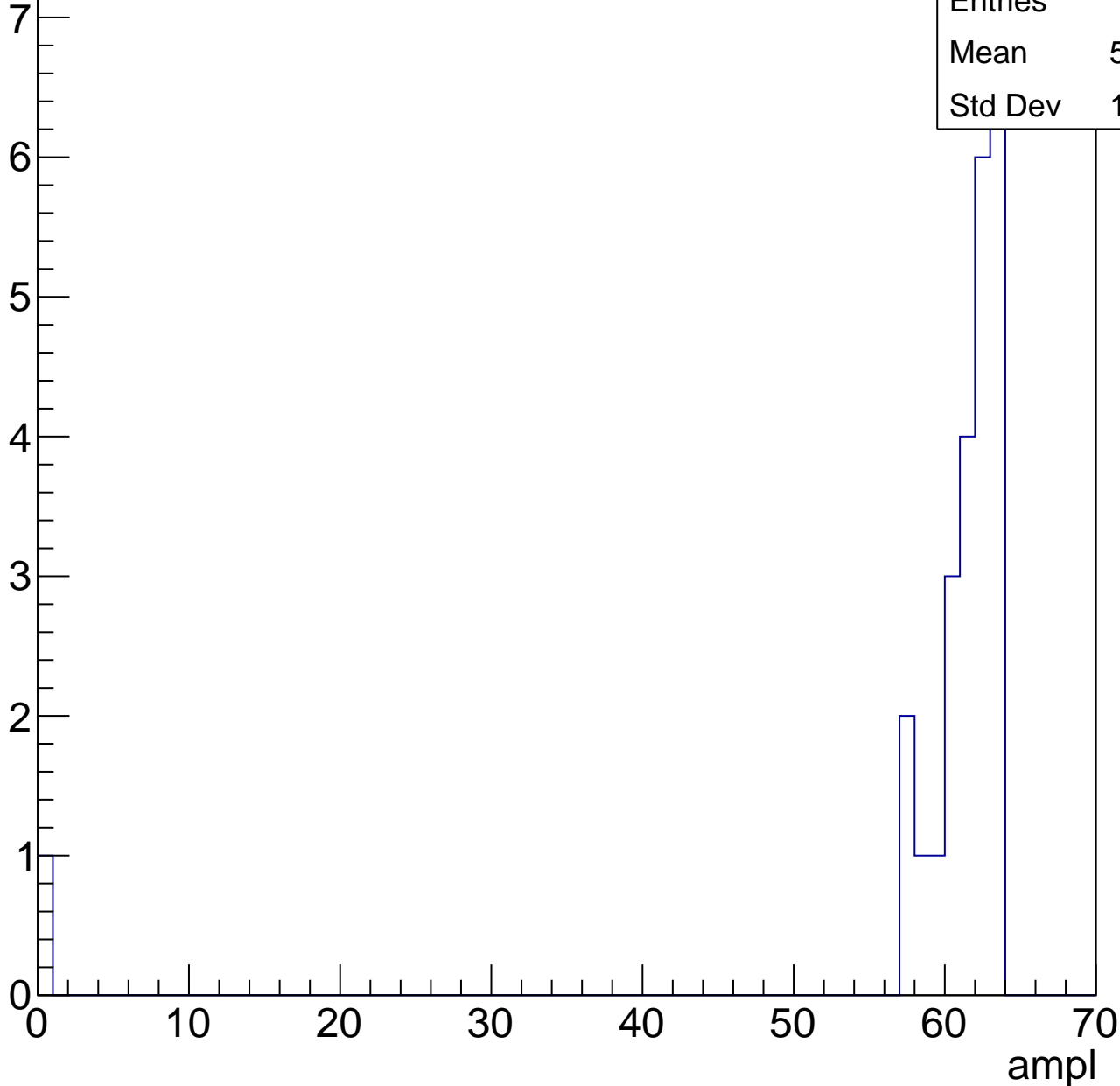


# B1L100S, U2-ch61, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

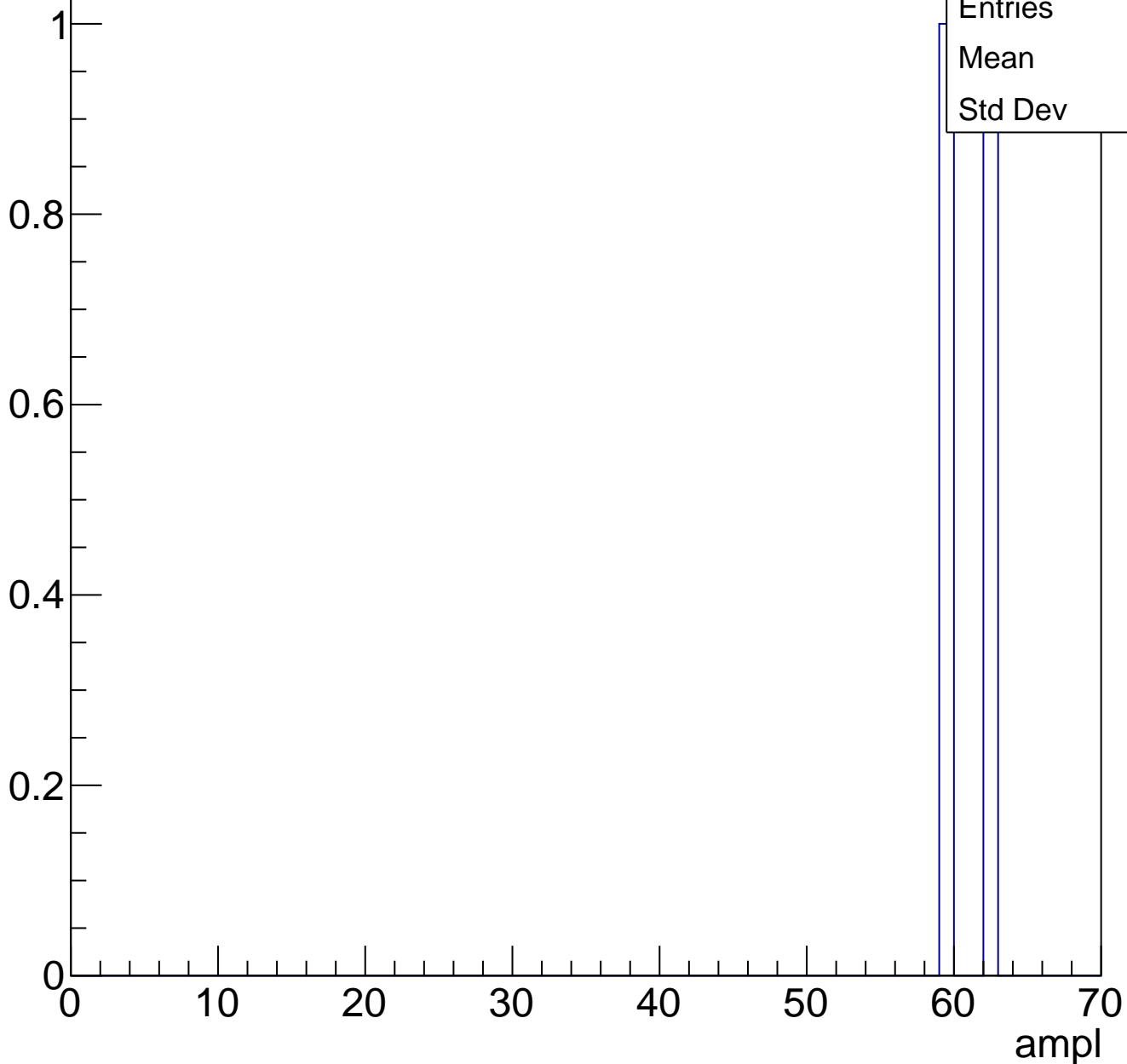
Entries	25
Mean	58.72
Std Dev	12.12



# B1L100S, U2-ch61, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry





# B1L100S, U2-ch61, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

1  
0.8  
0.6  
0.4  
0.2  
0

Entries	1
Mean	25
Std Dev	0

ampl

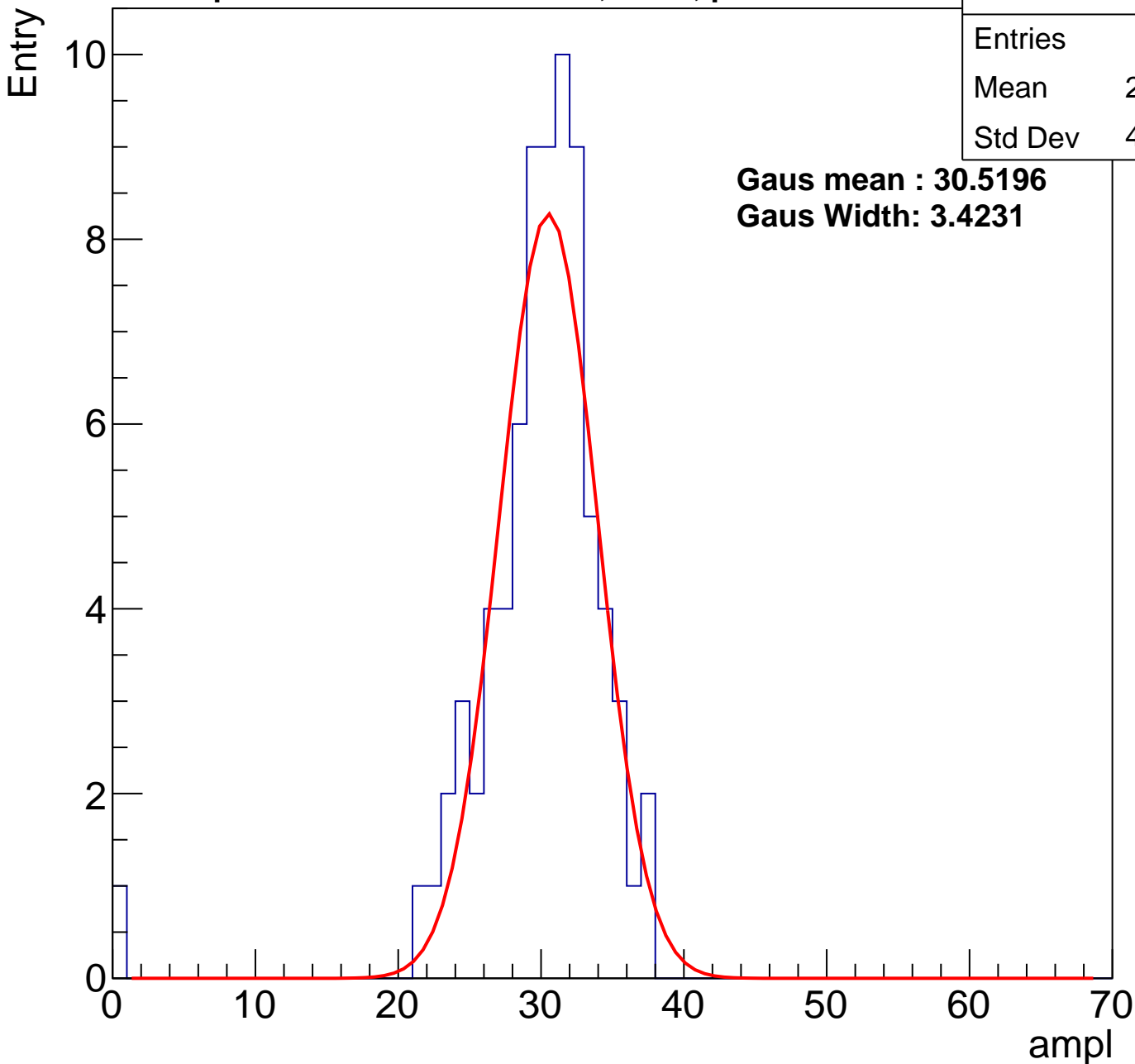
# B1L100S, U2-ch62, adc0

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	76
Mean	29.42
Std Dev	4.829

**Gaus mean : 30.5196**

**Gaus Width: 3.4231**



# B1L100S, U2-ch62, adc1

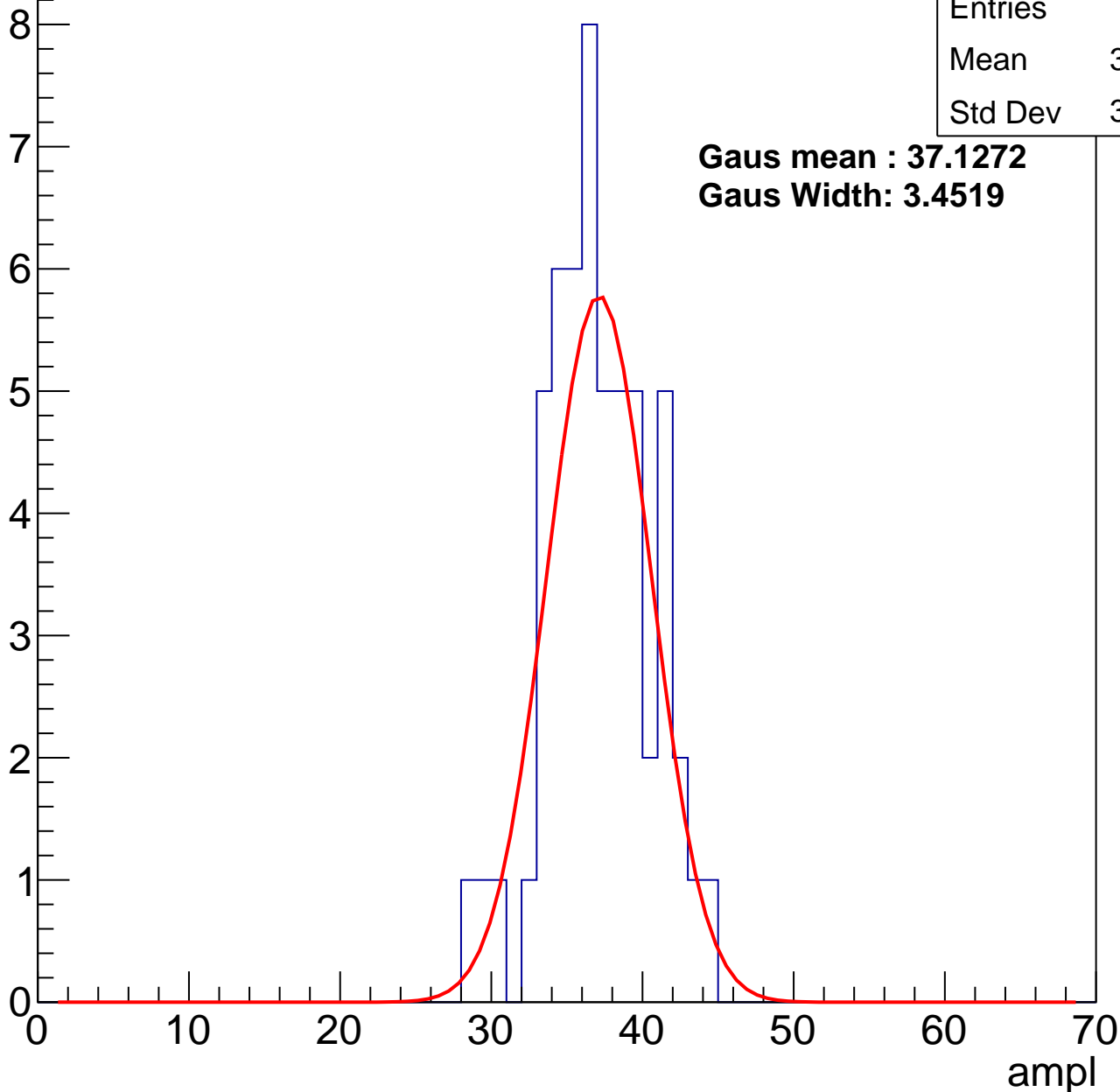
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	55
Mean	36.58
Std Dev	3.394

**Gaus mean : 37.1272**

**Gaus Width: 3.4519**

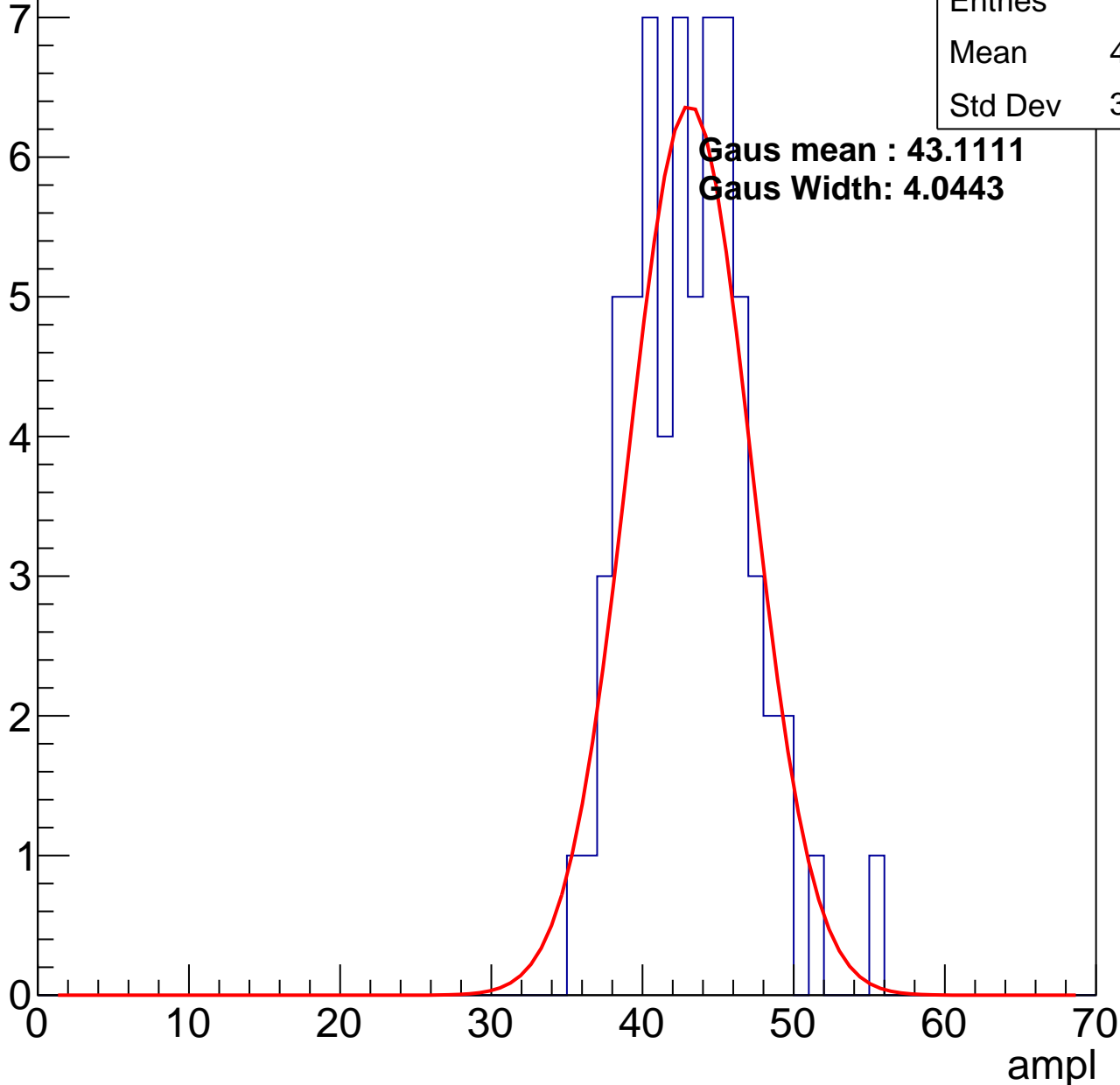


# B1L100S, U2-ch62, adc2

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

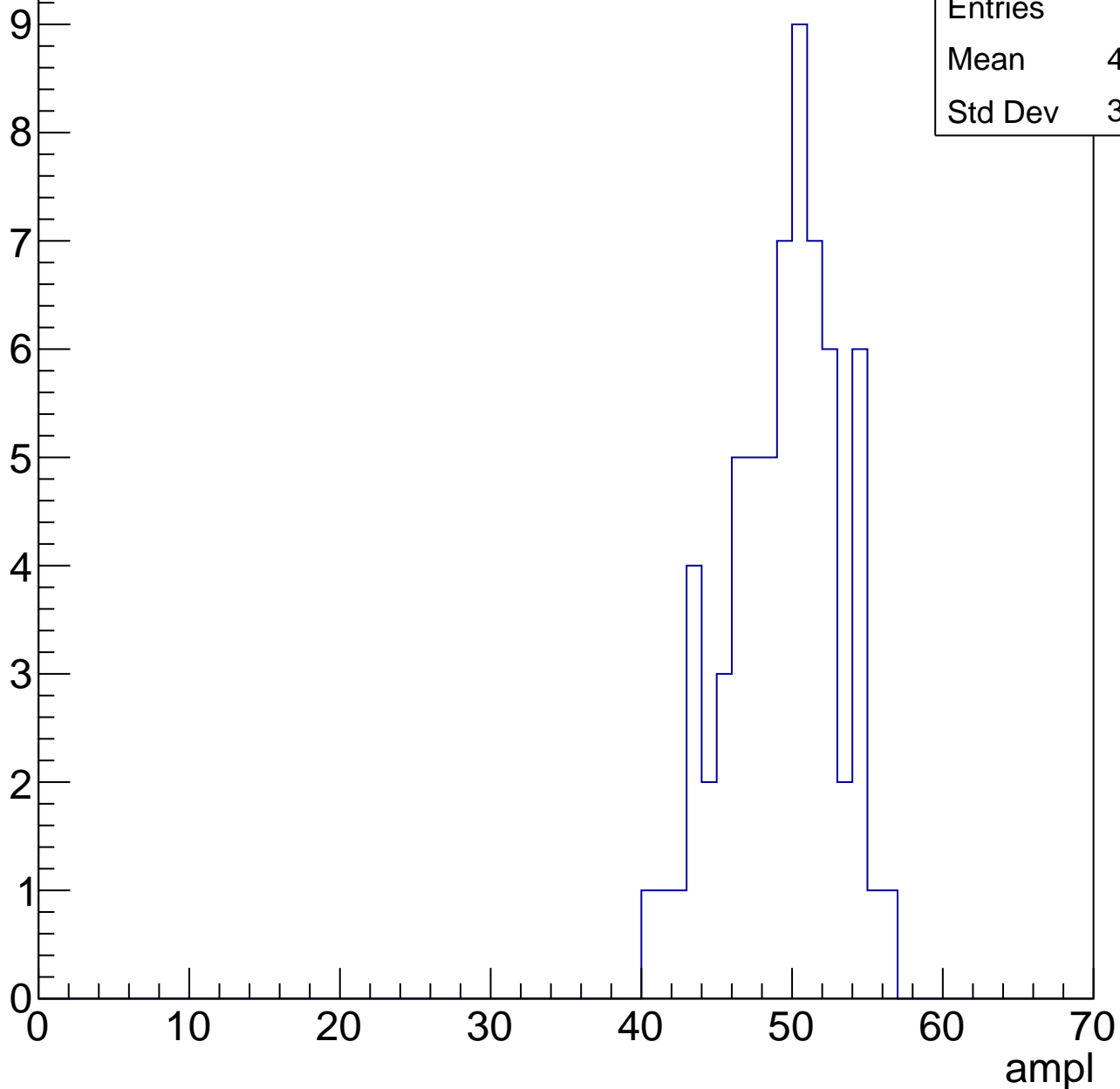
Entries	66
Mean	42.64
Std Dev	3.816



# B1L100S, U2-ch62, adc3

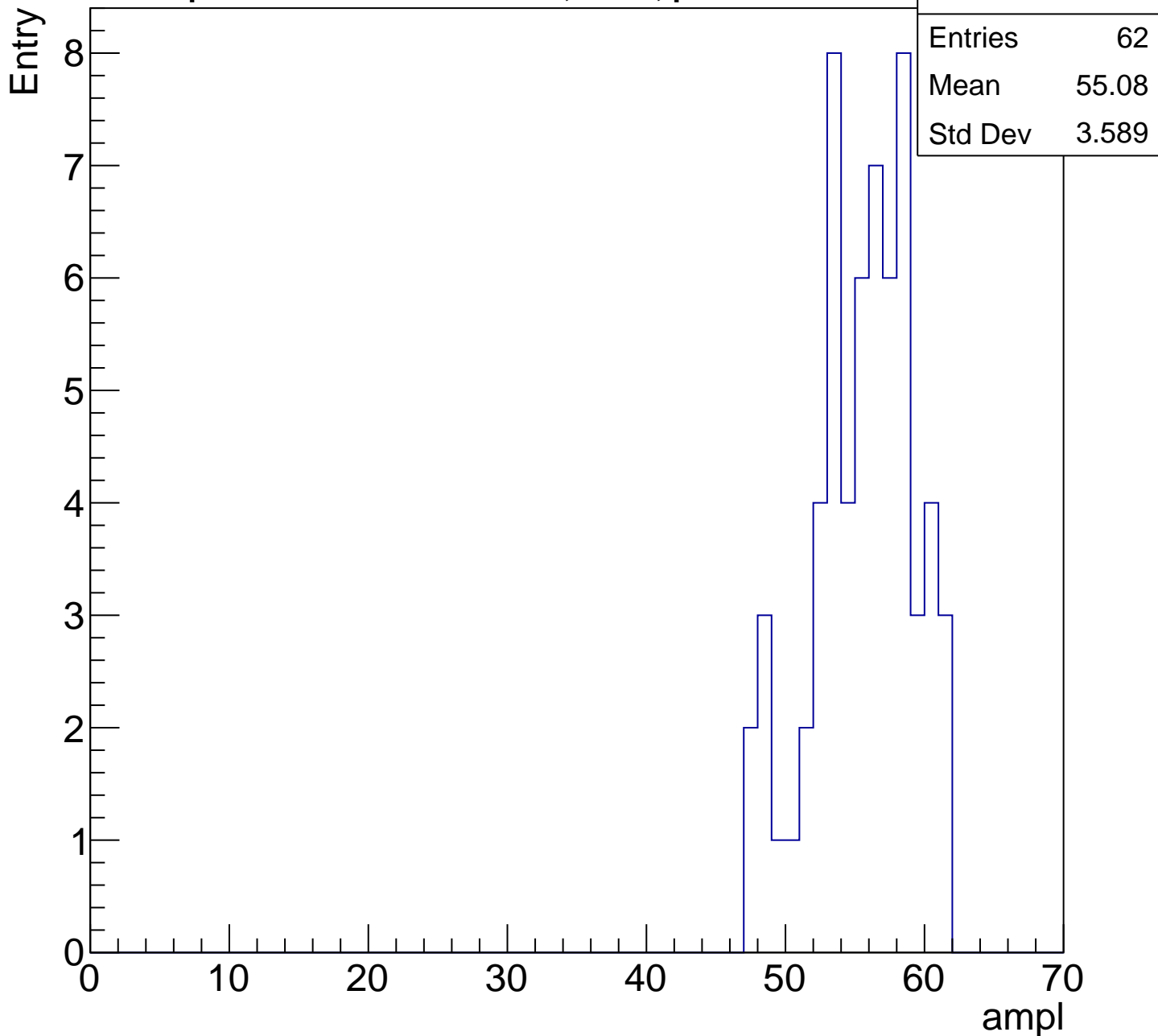
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



# B1L100S, U2-ch62, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2



# B1L100S, U2-ch62, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

7

6

5

4

3

2

1

0

0

10

20

30

40

50

60

70

ampl

Entries	38
Mean	59.79
Std Dev	2.284

0

1

2

3

4

5

6

7

8

9

10

11

12

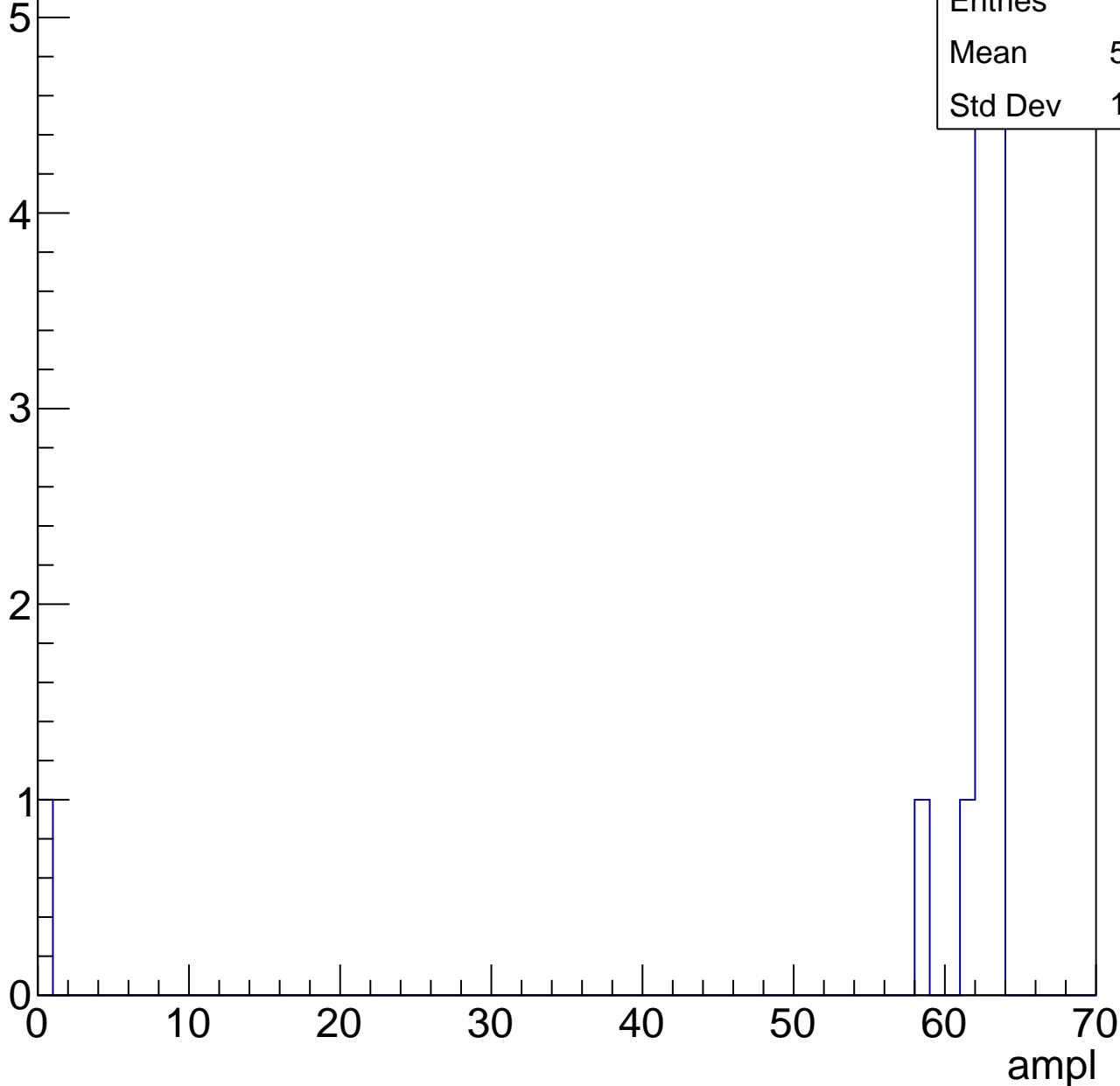
13

# B1L100S, U2-ch62, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	13
Mean	57.23
Std Dev	16.57





# B1L100S, U2-ch62, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L100S, U2-ch63, adc0

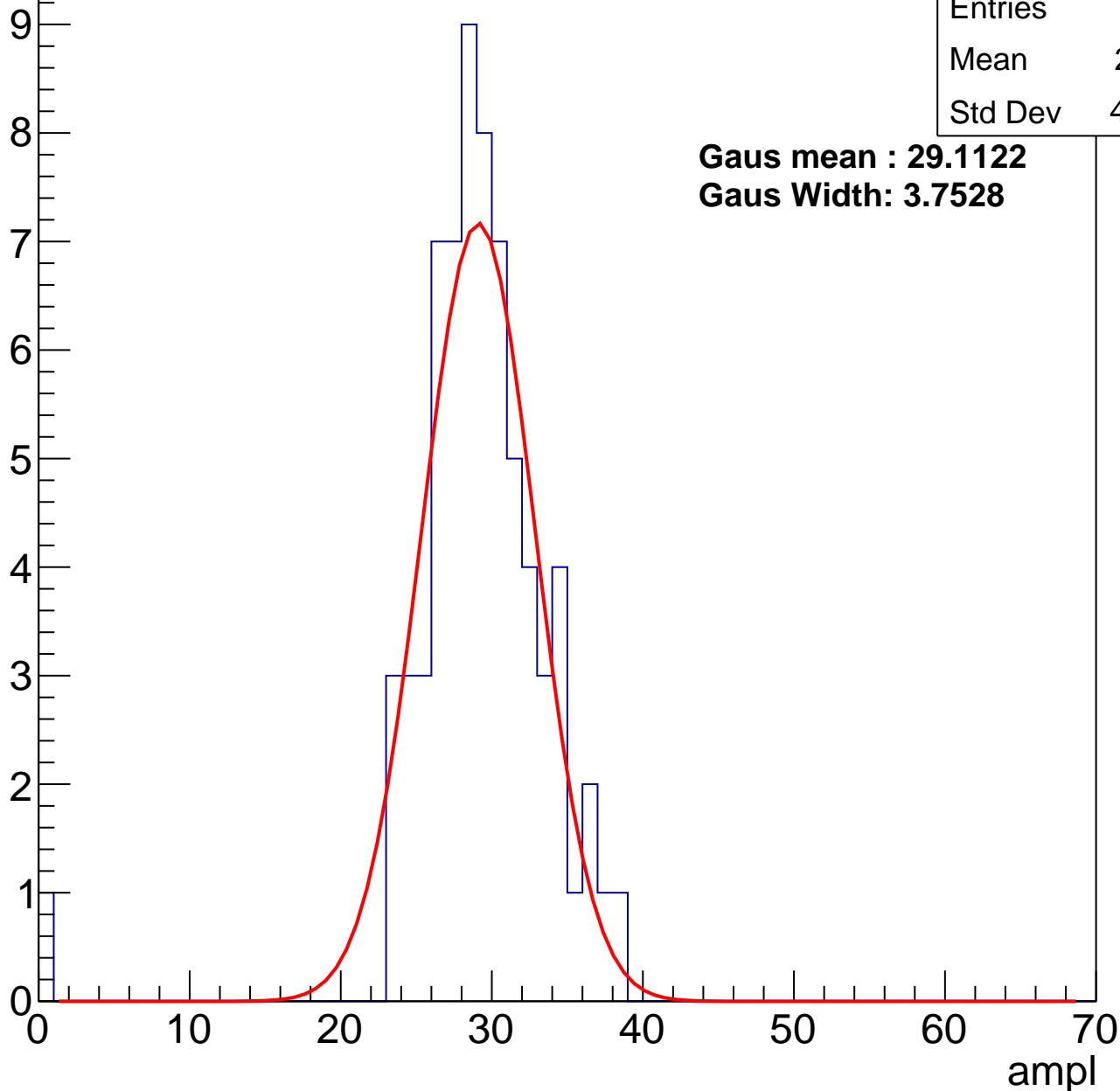
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	69
Mean	28.71
Std Dev	4.899

**Gaus mean : 29.122**

**Gaus Width: 3.7528**



# B1L100S, U2-ch63, adc1

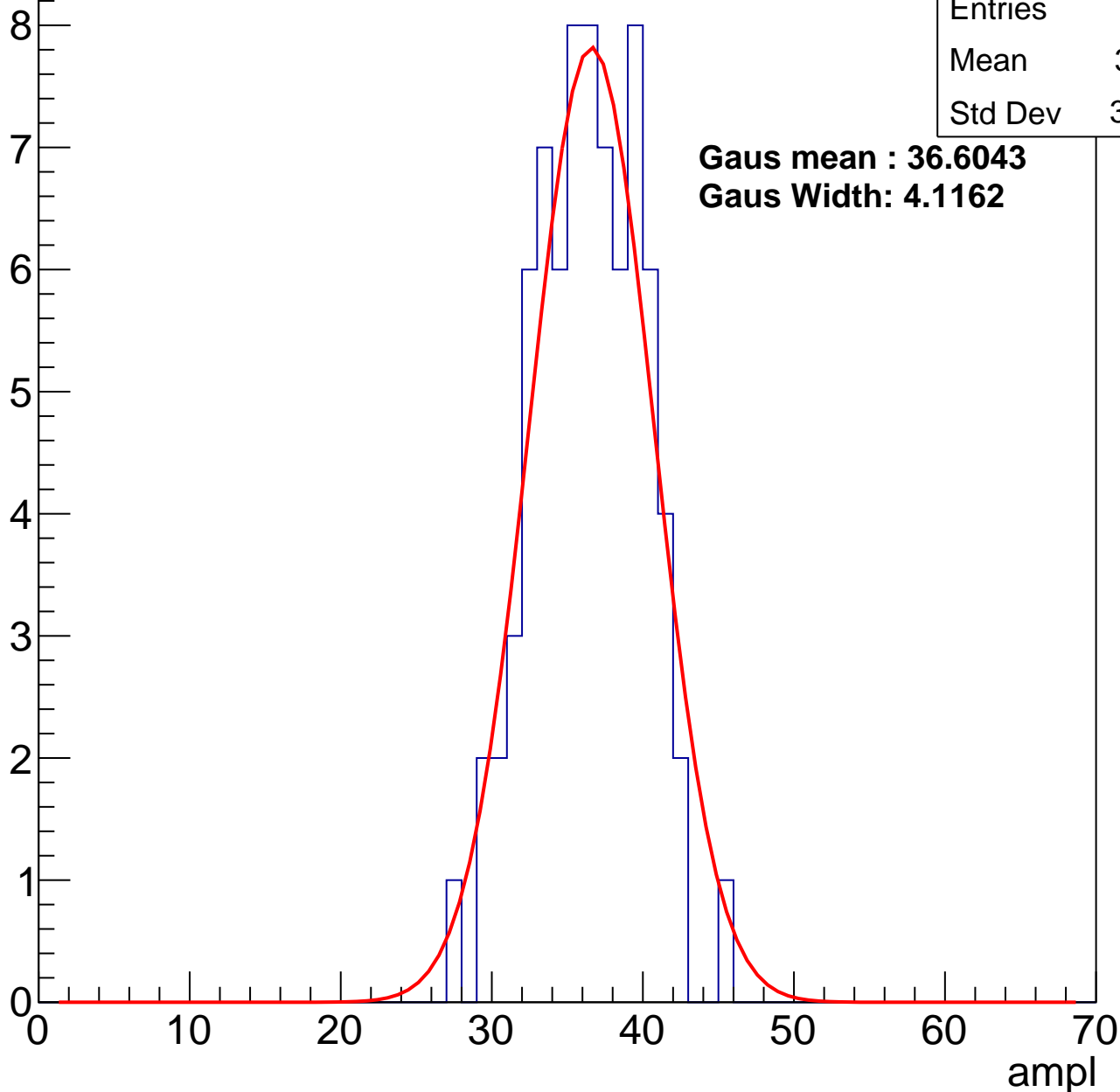
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	77
Mean	35.91
Std Dev	3.546

**Gaus mean : 36.6043**

**Gaus Width: 4.1162**



# B1L100S, U2-ch63, adc2

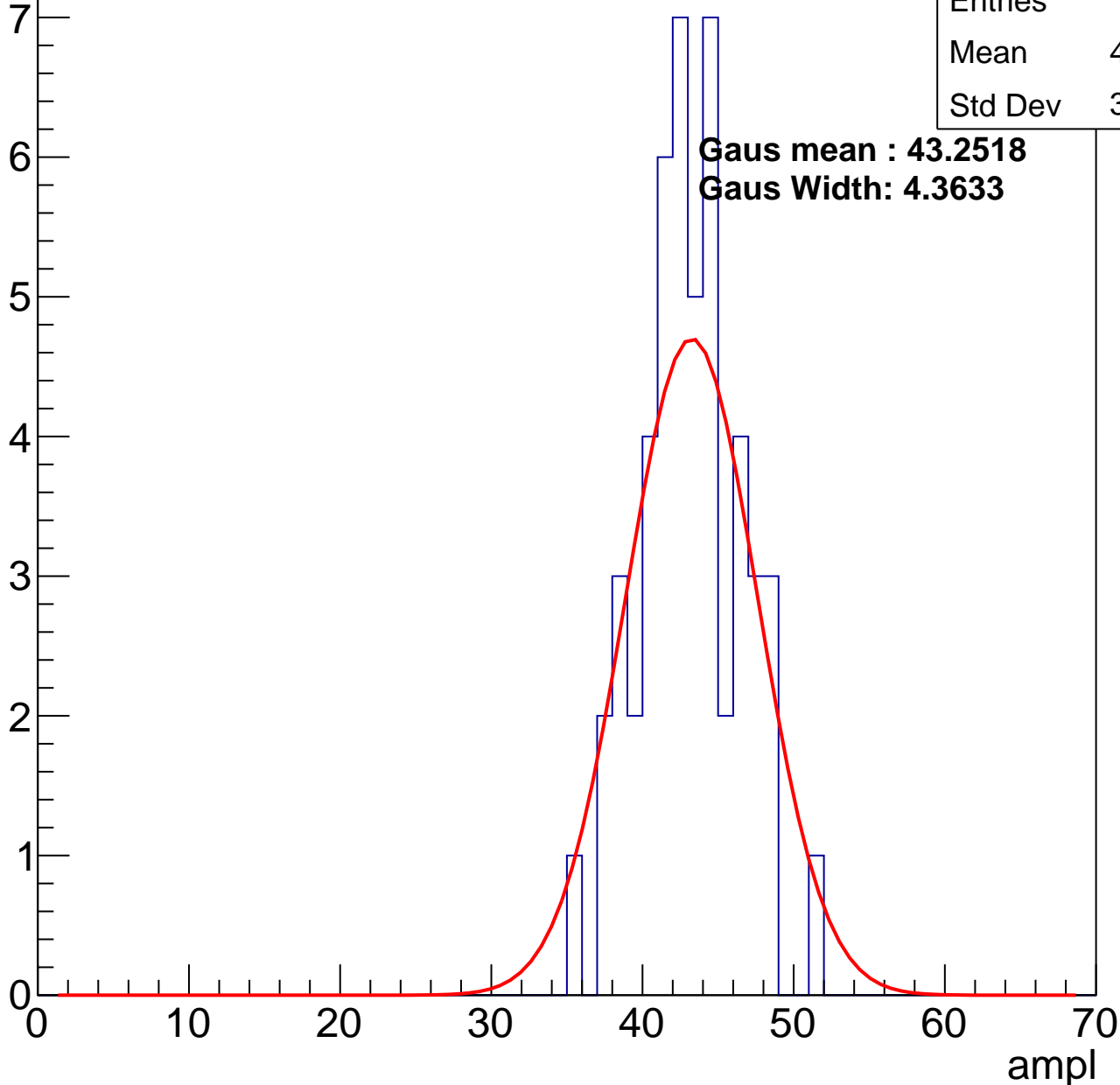
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	50
Mean	42.68
Std Dev	3.295

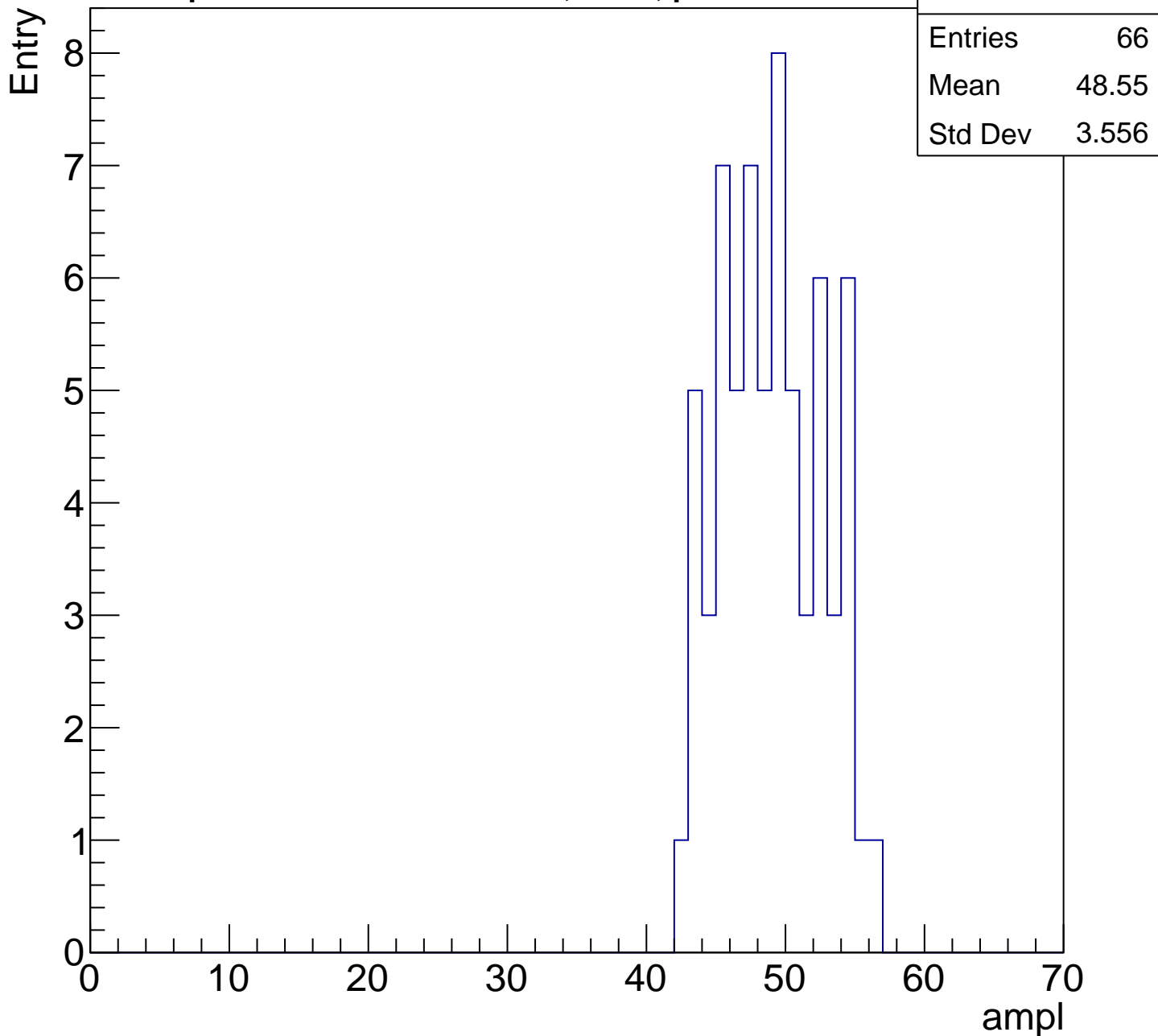
**Gaus mean : 43.2518**

**Gaus Width: 4.3633**



# B1L100S, U2-ch63, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

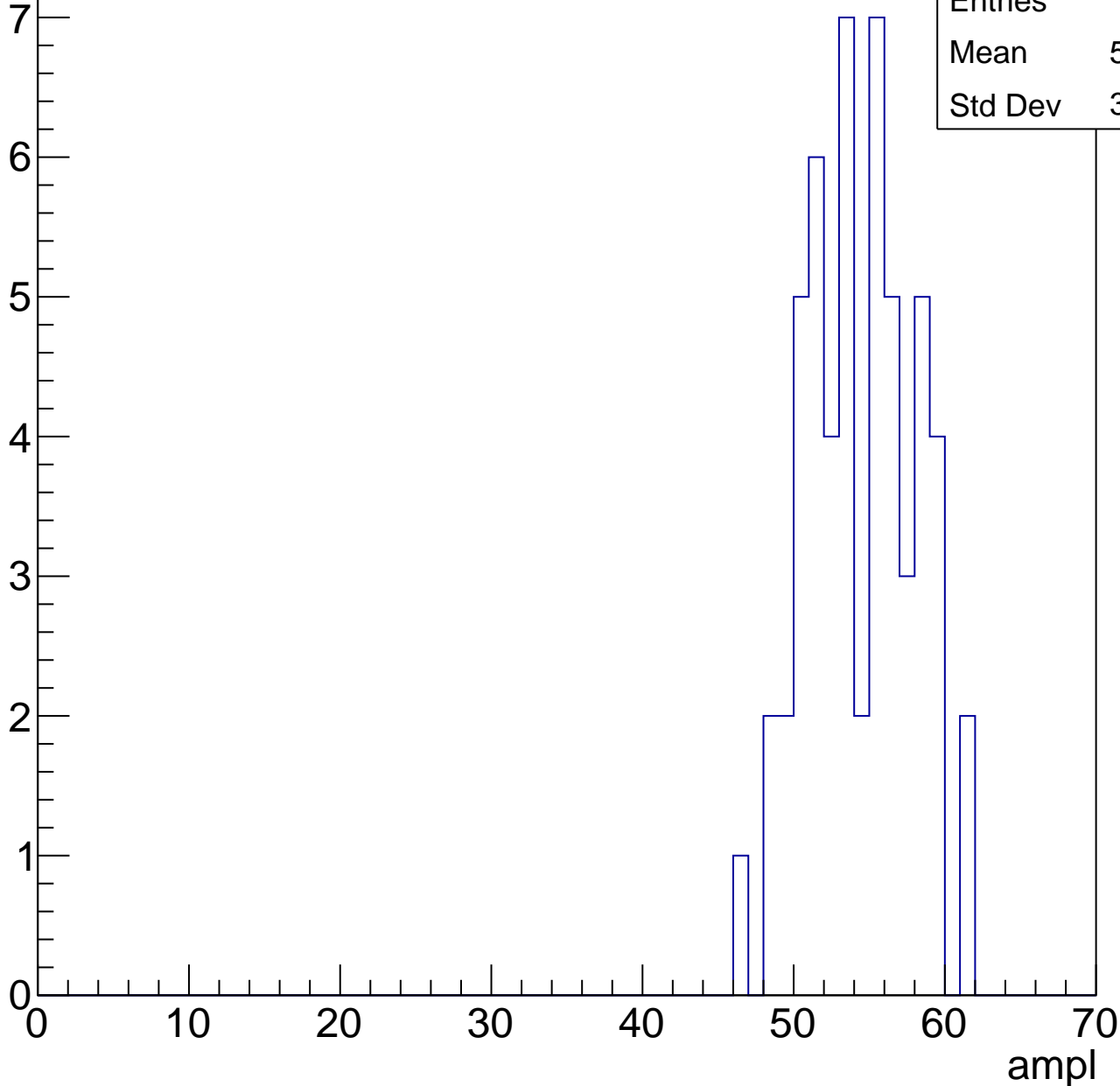


# B1L100S, U2-ch63, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

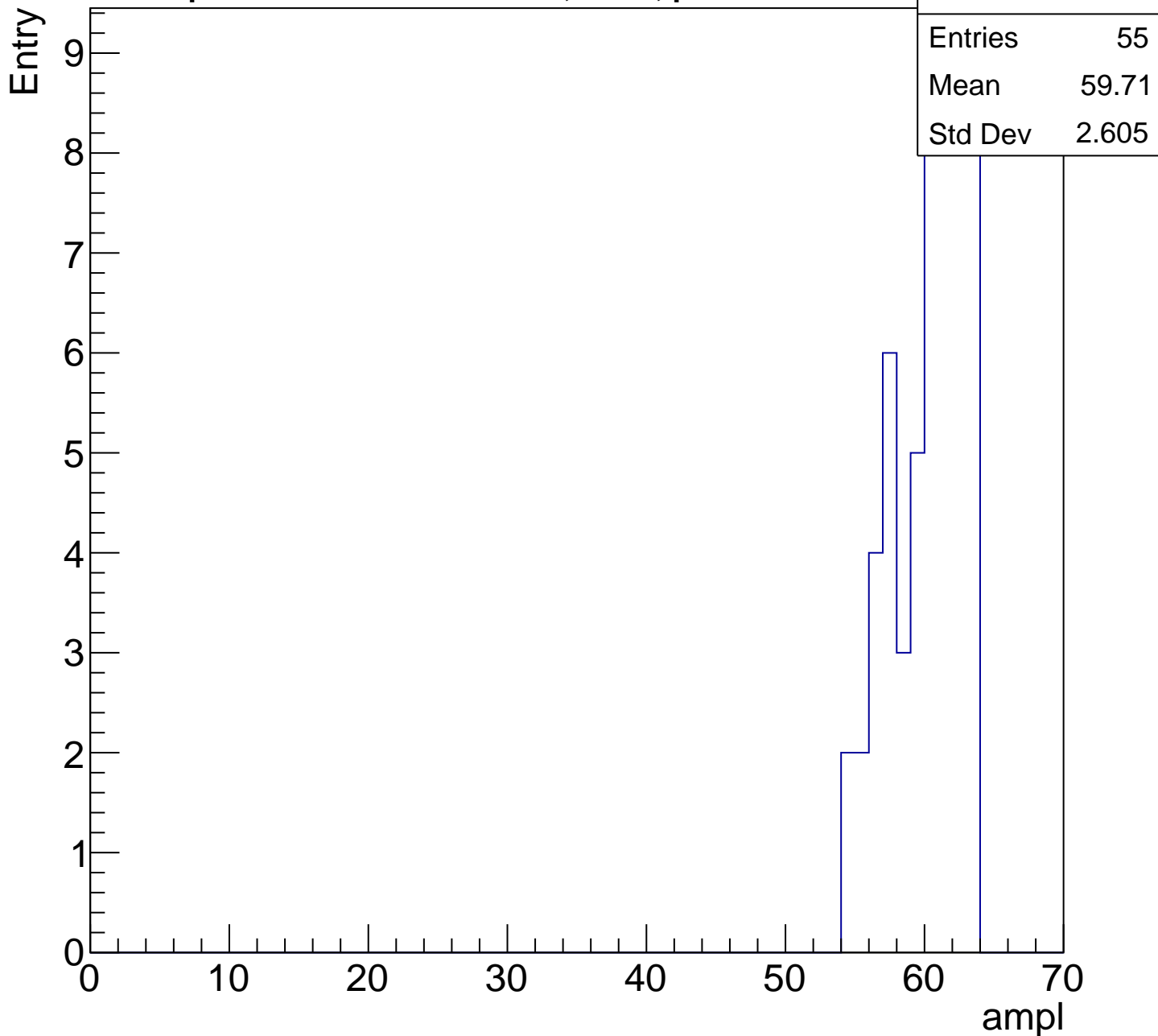
Entry

Entries	55
Mean	53.95
Std Dev	3.503



# B1L100S, U2-ch63, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2



# B1L100S, U2-ch63, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

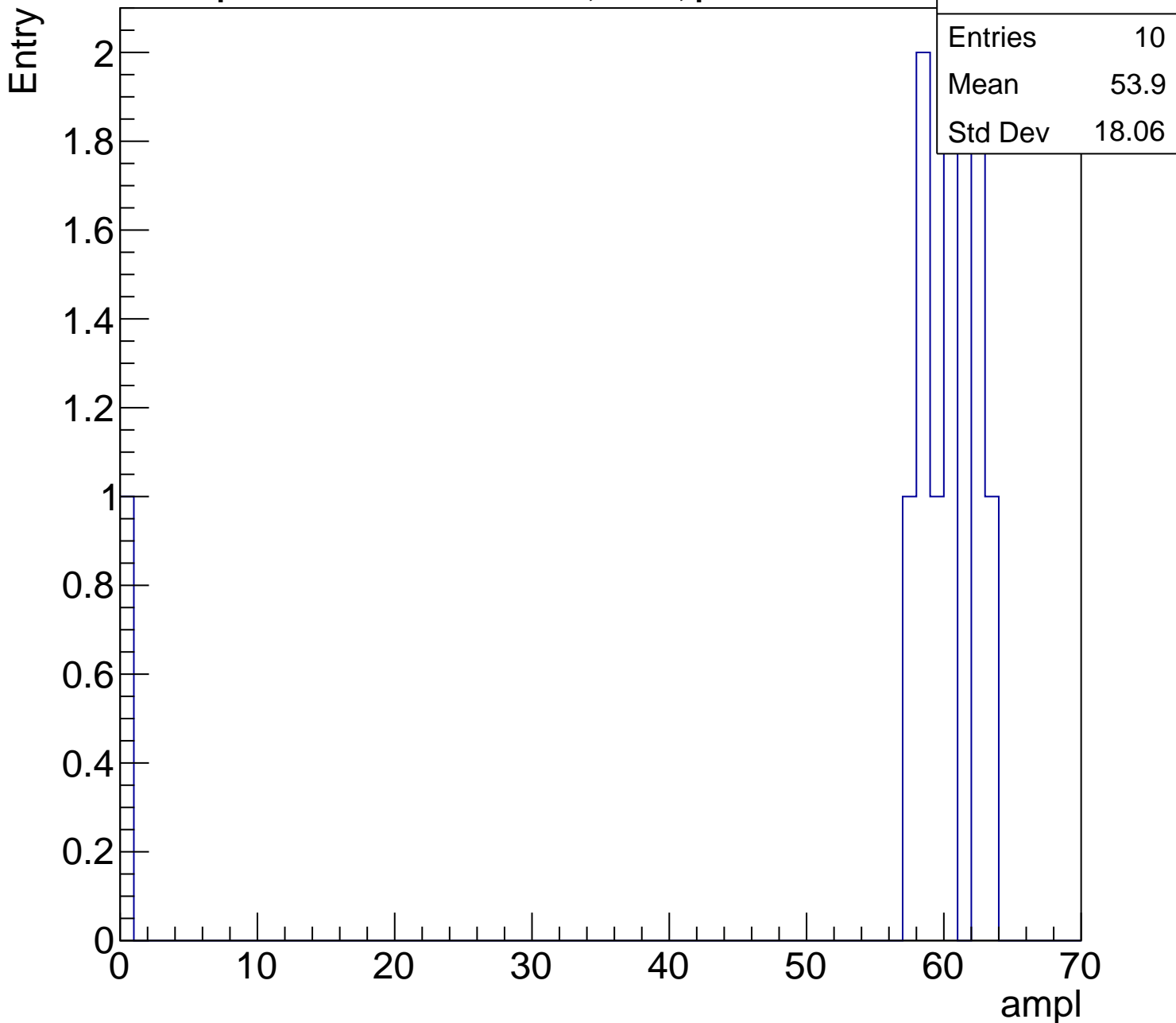
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	10
Mean	53.9
Std Dev	18.06

0 10 20 30 40 50 60 70

ampl





# B1L100S, U2-ch63, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L100S, U2-ch64, adc0

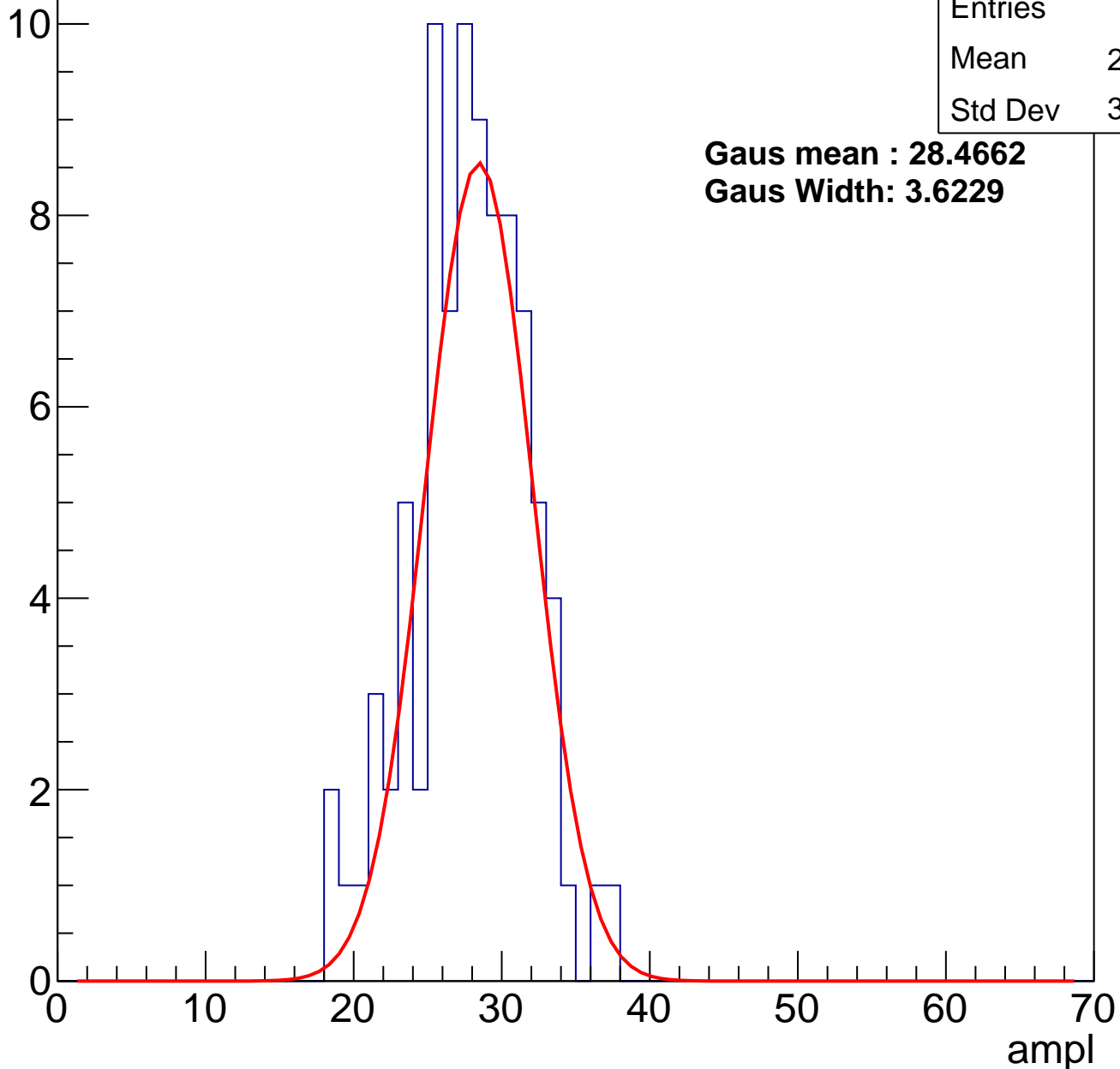
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	87
Mean	27.44
Std Dev	3.844

**Gaus mean : 28.4662**

**Gaus Width: 3.6229**

Entry



# B1L100S, U2-ch64, adc1

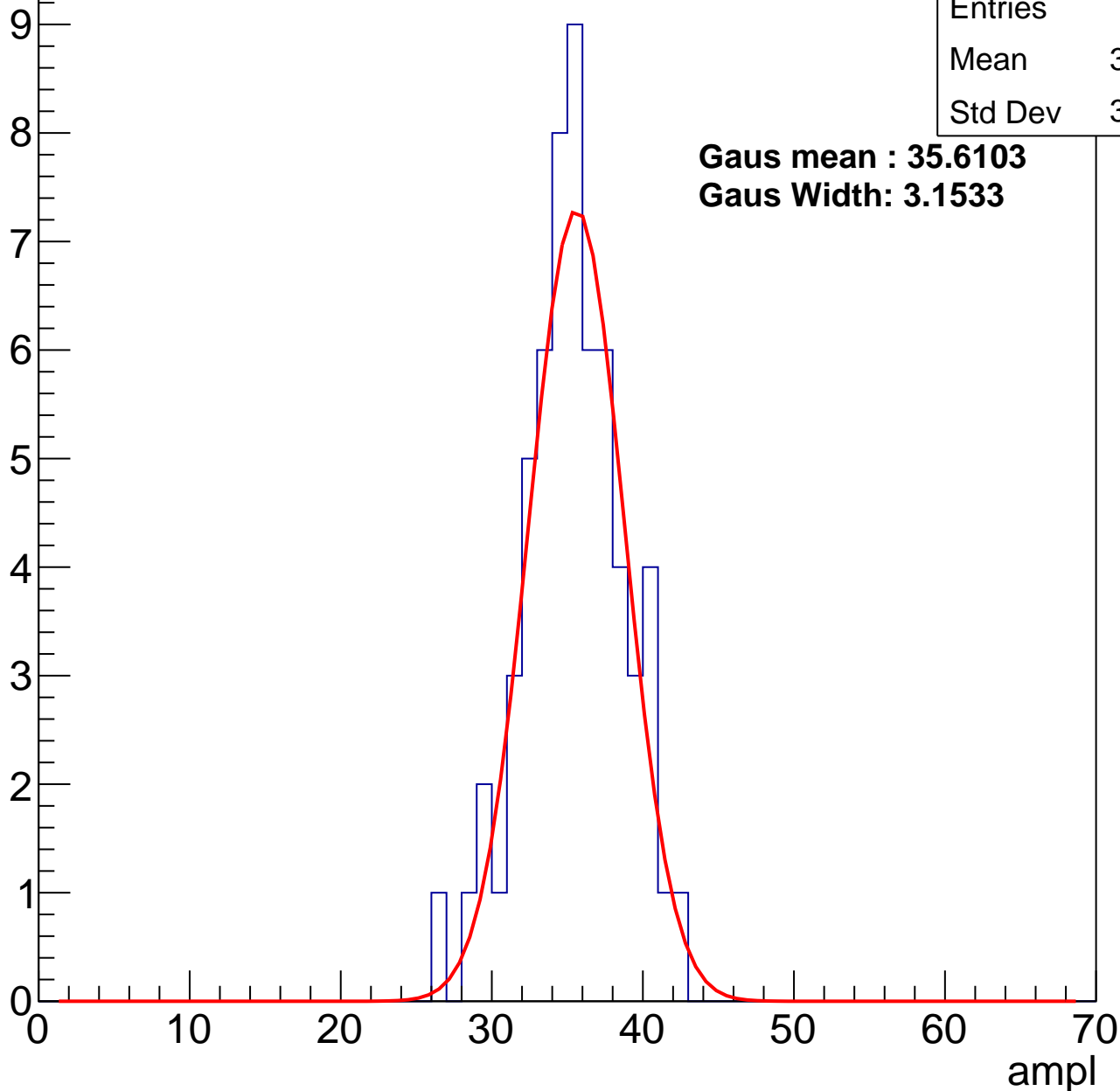
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	61
Mean	34.92
Std Dev	3.266

**Gaus mean : 35.6103**

**Gaus Width: 3.1533**



# B1L100S, U2-ch64, adc2

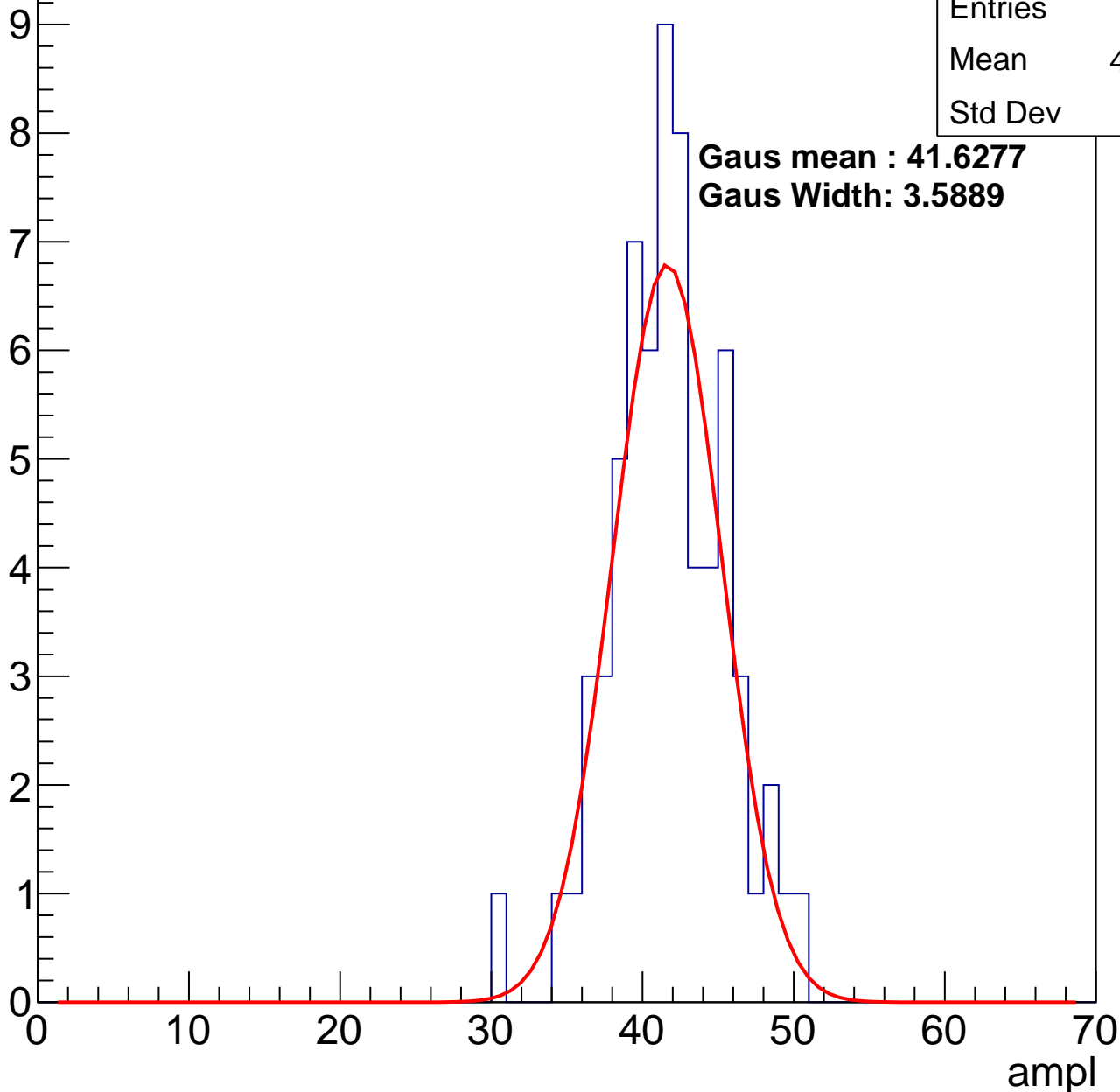
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	66
Mean	41.27
Std Dev	3.72

**Gaus mean : 41.6277**

**Gaus Width: 3.5889**

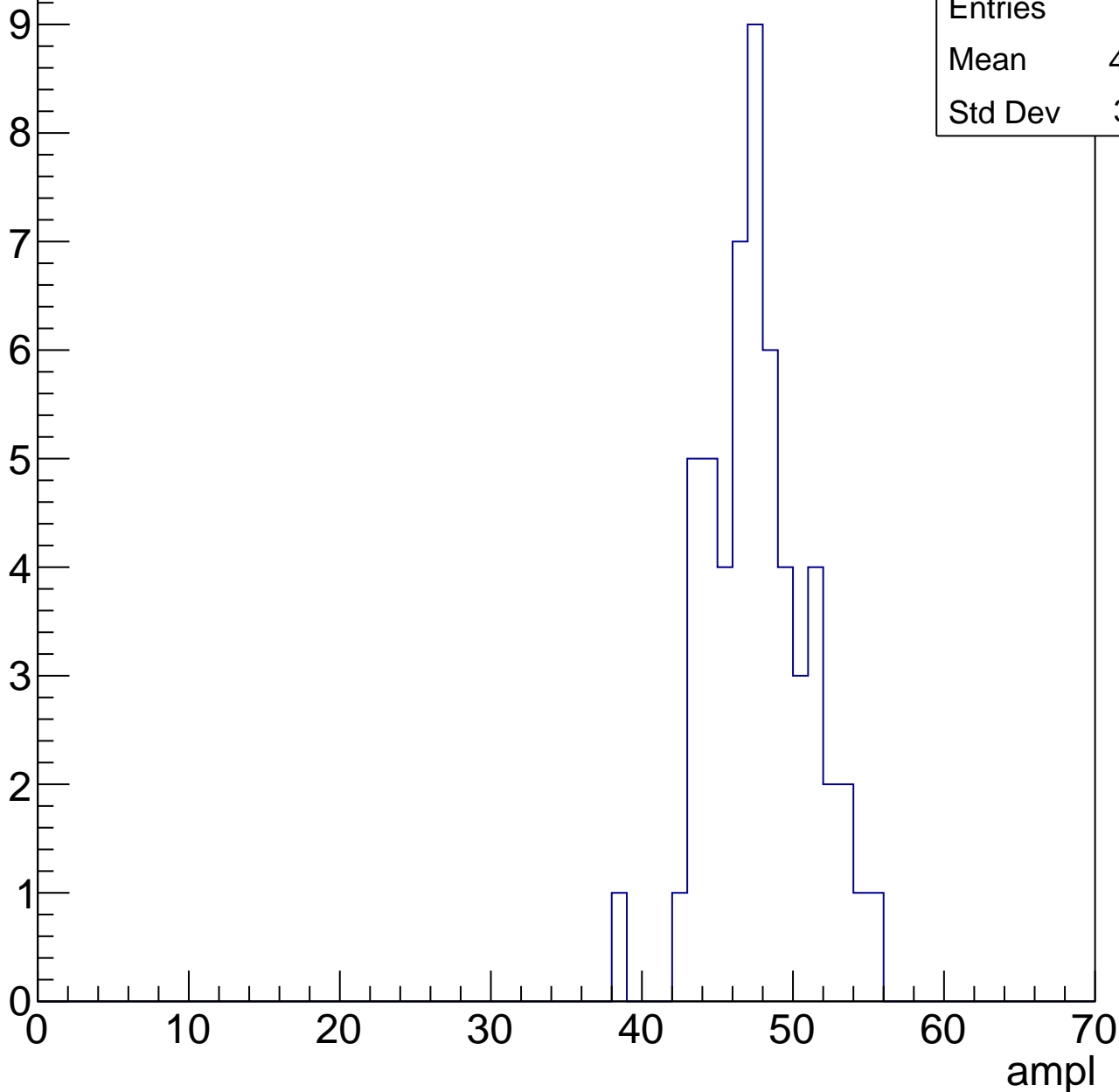


# B1L100S, U2-ch64, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

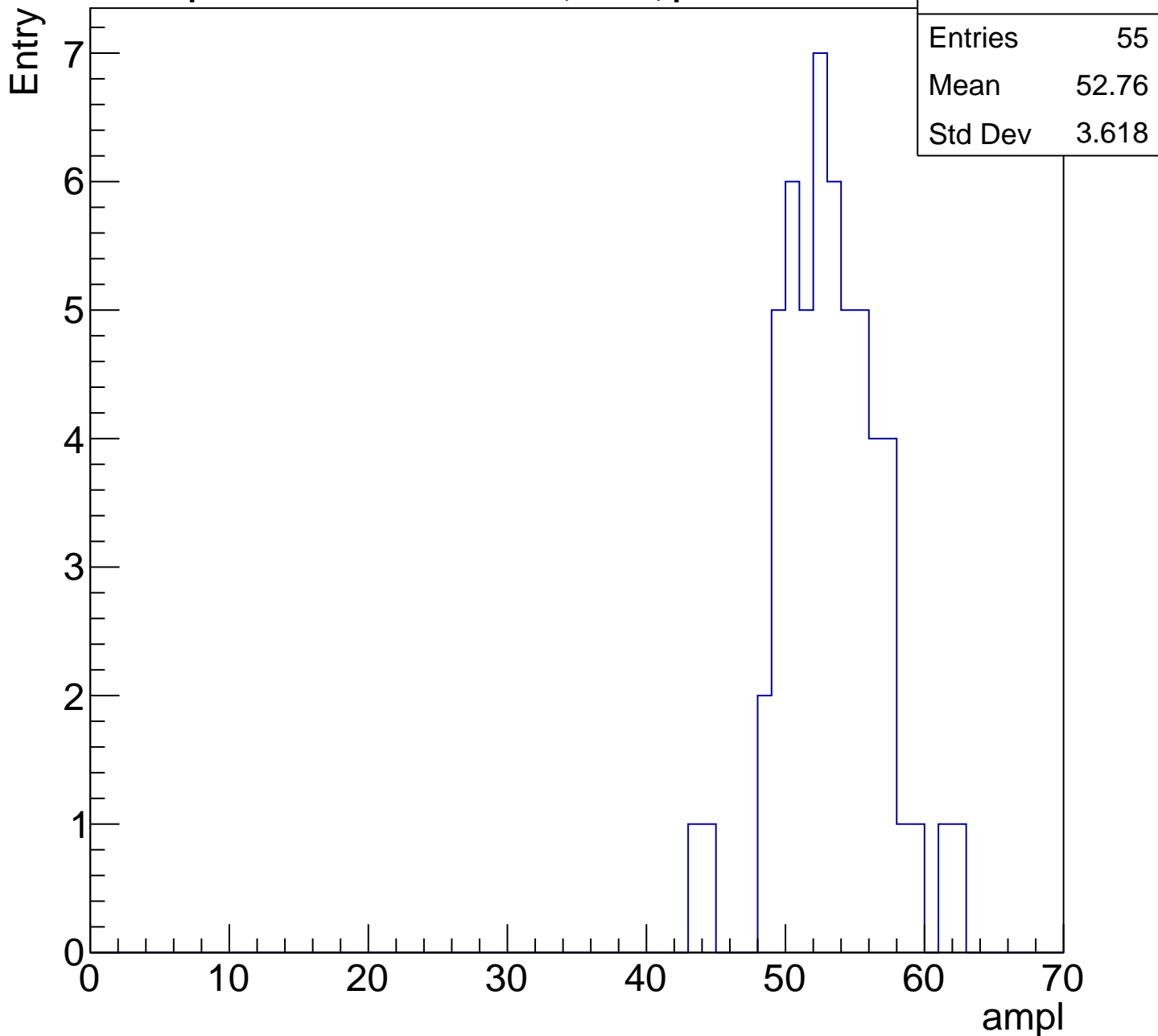
Entry

Entries	55
Mean	47.22
Std Dev	3.301



# B1L100S, U2-ch64, adc4

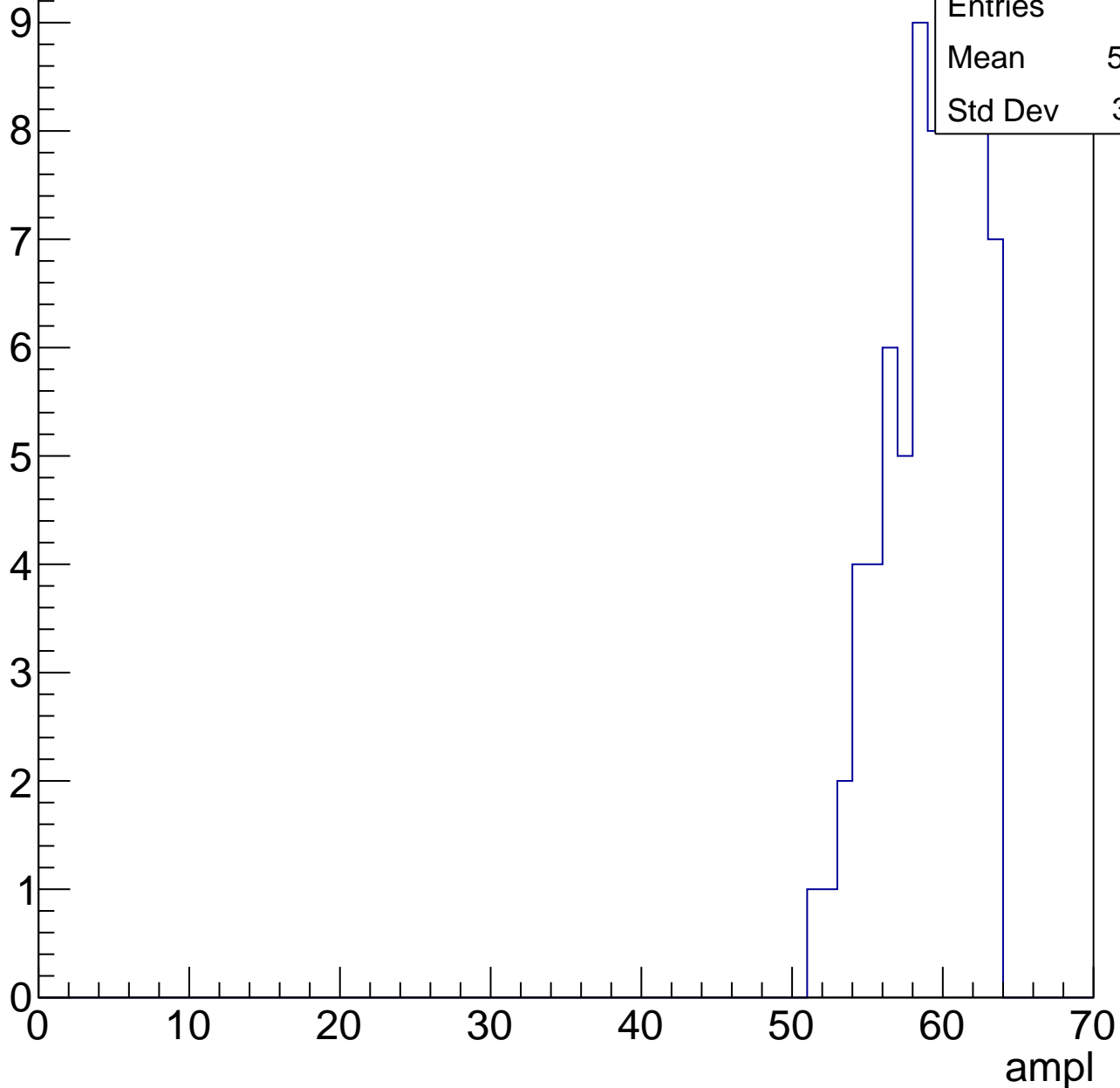
calib\_packv5\_042523\_0143.root, FC#4, port A2



# B1L100S, U2-ch64, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

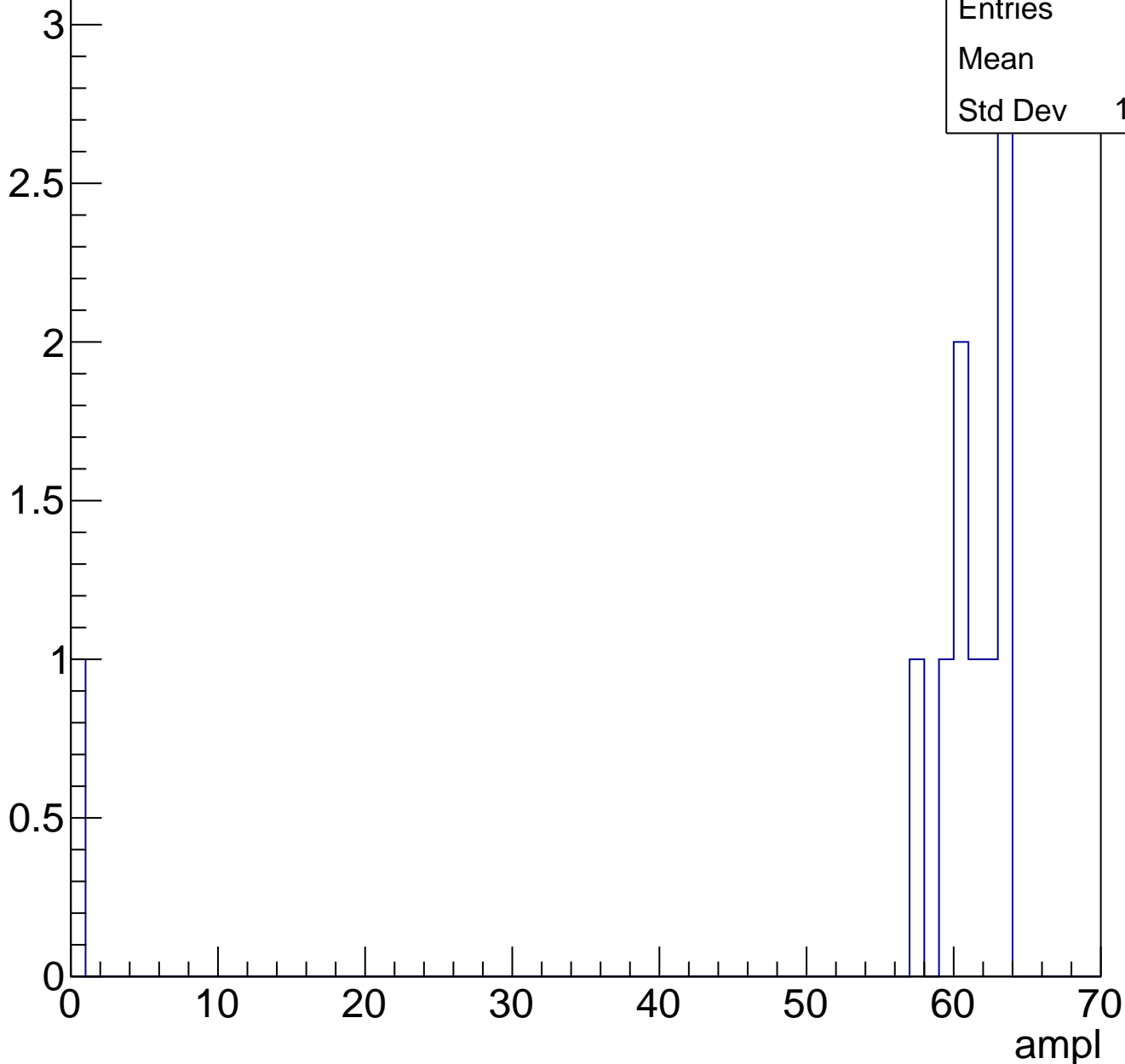
Entry



# B1L100S, U2-ch64, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry





# B1L100S, U2-ch64, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L100S, U2-ch65, adc0

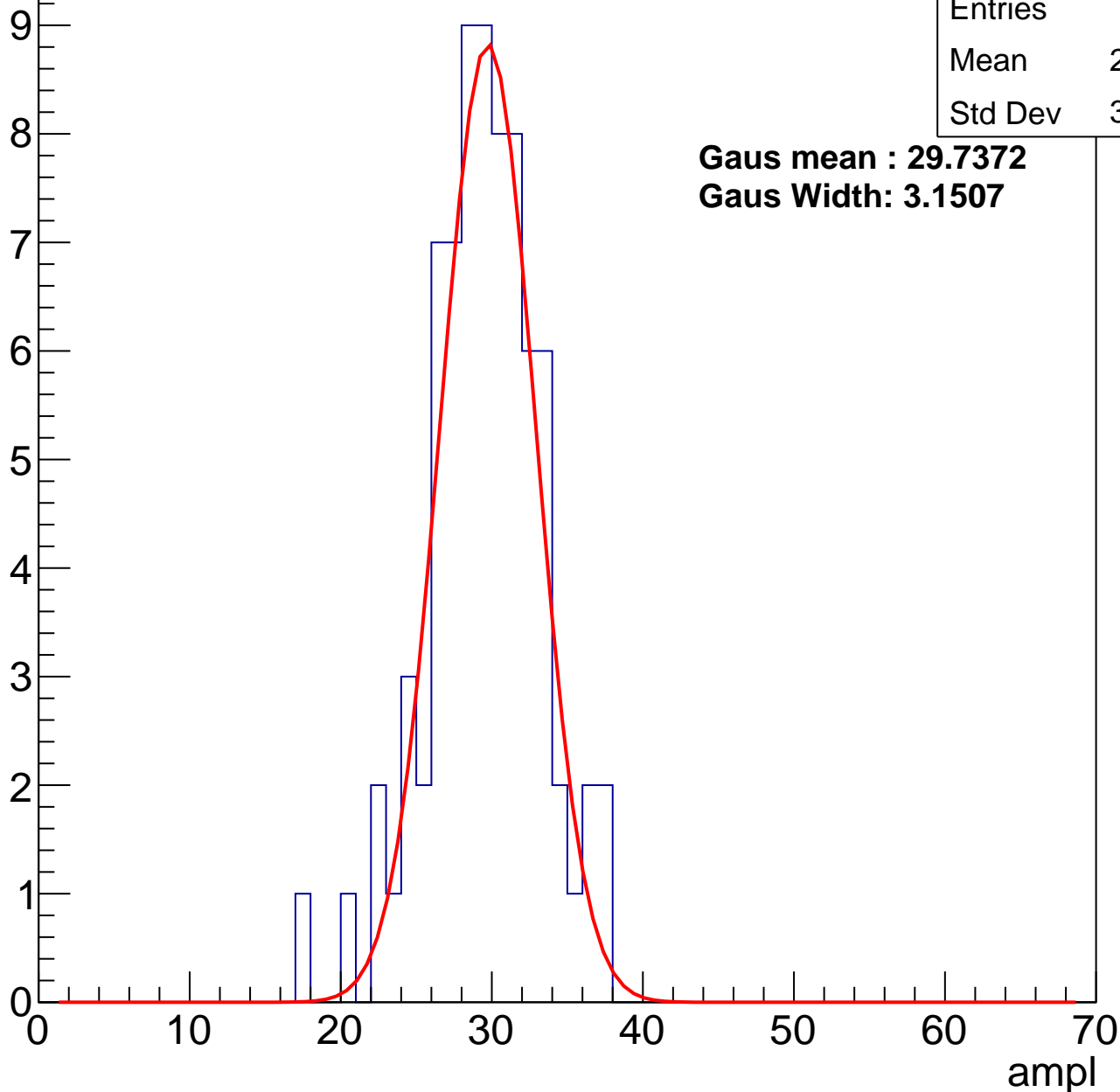
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	77
Mean	29.05
Std Dev	3.724

**Gaus mean : 29.7372**

**Gaus Width: 3.1507**



# B1L100S, U2-ch65, adc1

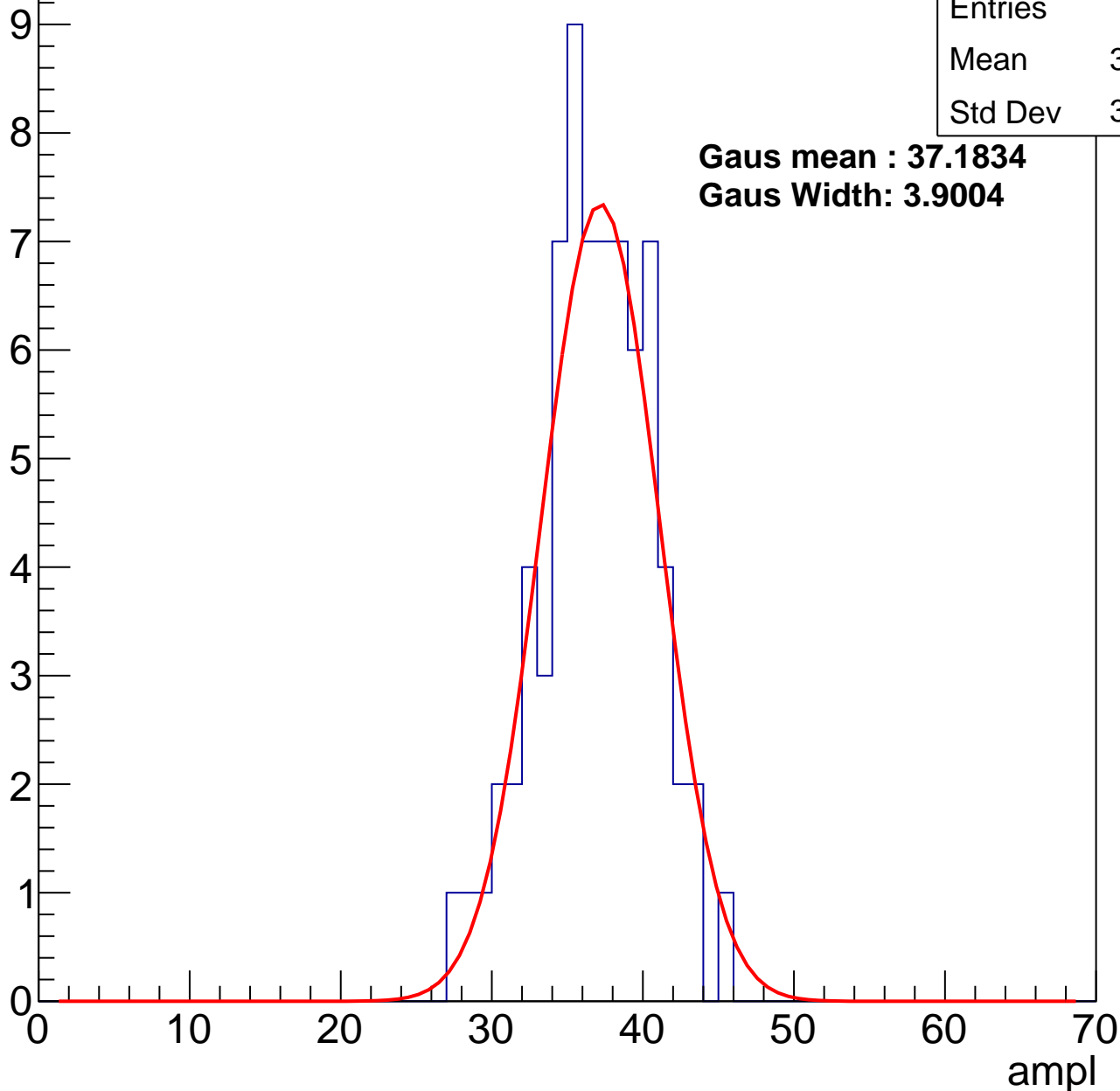
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	73
Mean	36.38
Std Dev	3.674

**Gaus mean : 37.1834**

**Gaus Width: 3.9004**



# B1L100S, U2-ch65, adc2

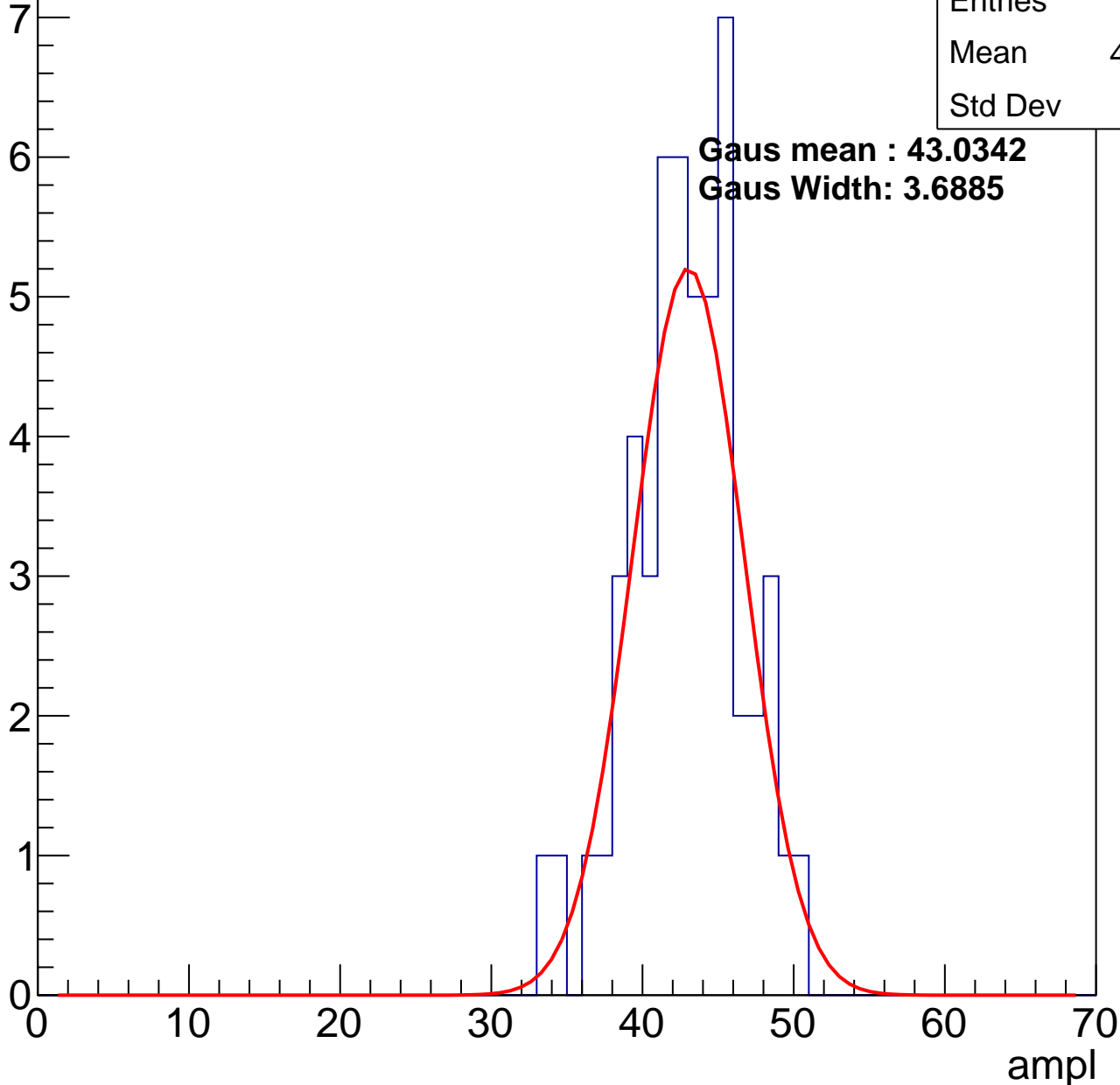
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	52
Mean	42.44
Std Dev	3.64

**Gaus mean : 43.0342**

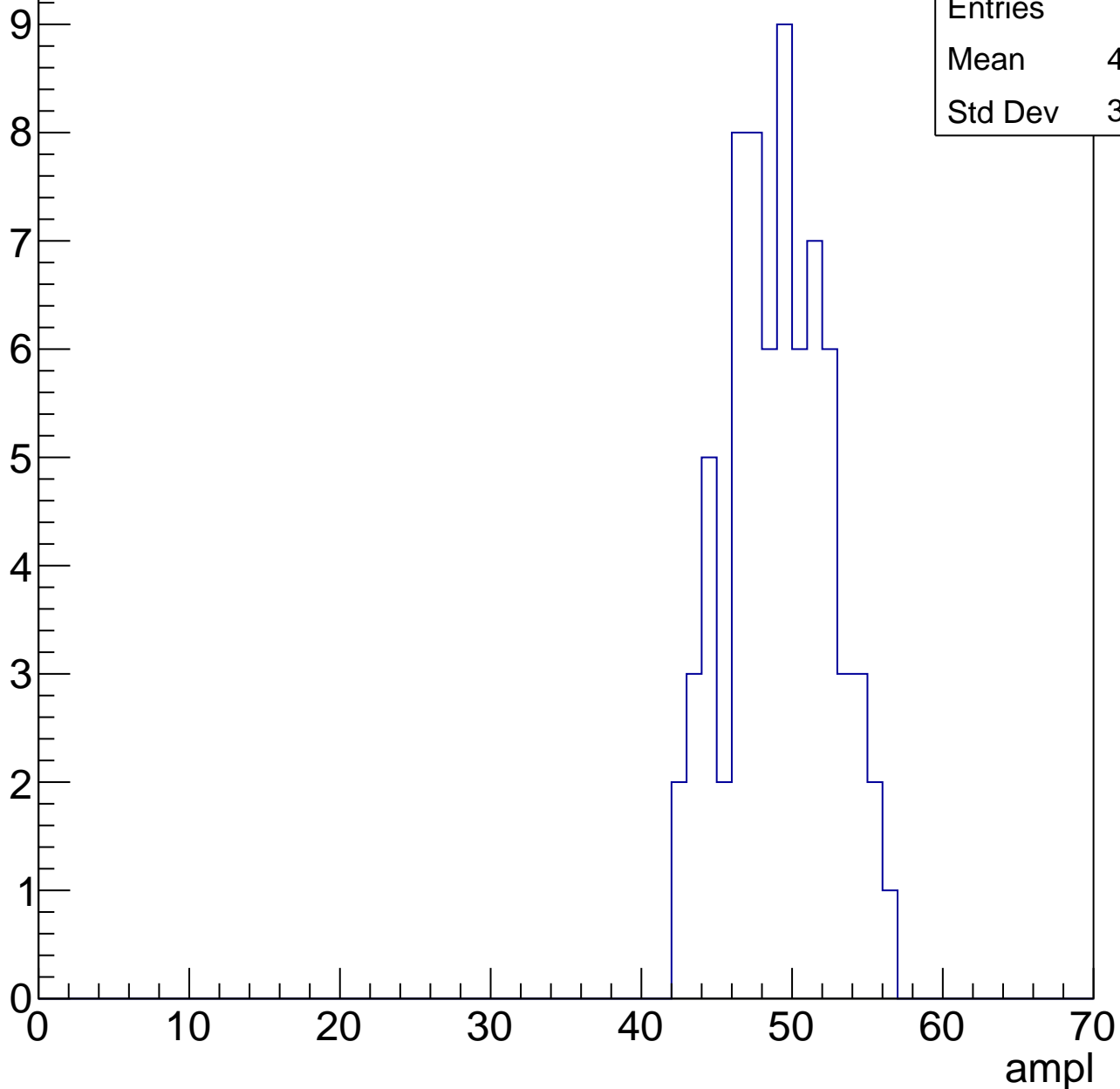
**Gaus Width: 3.6885**



# B1L100S, U2-ch65, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

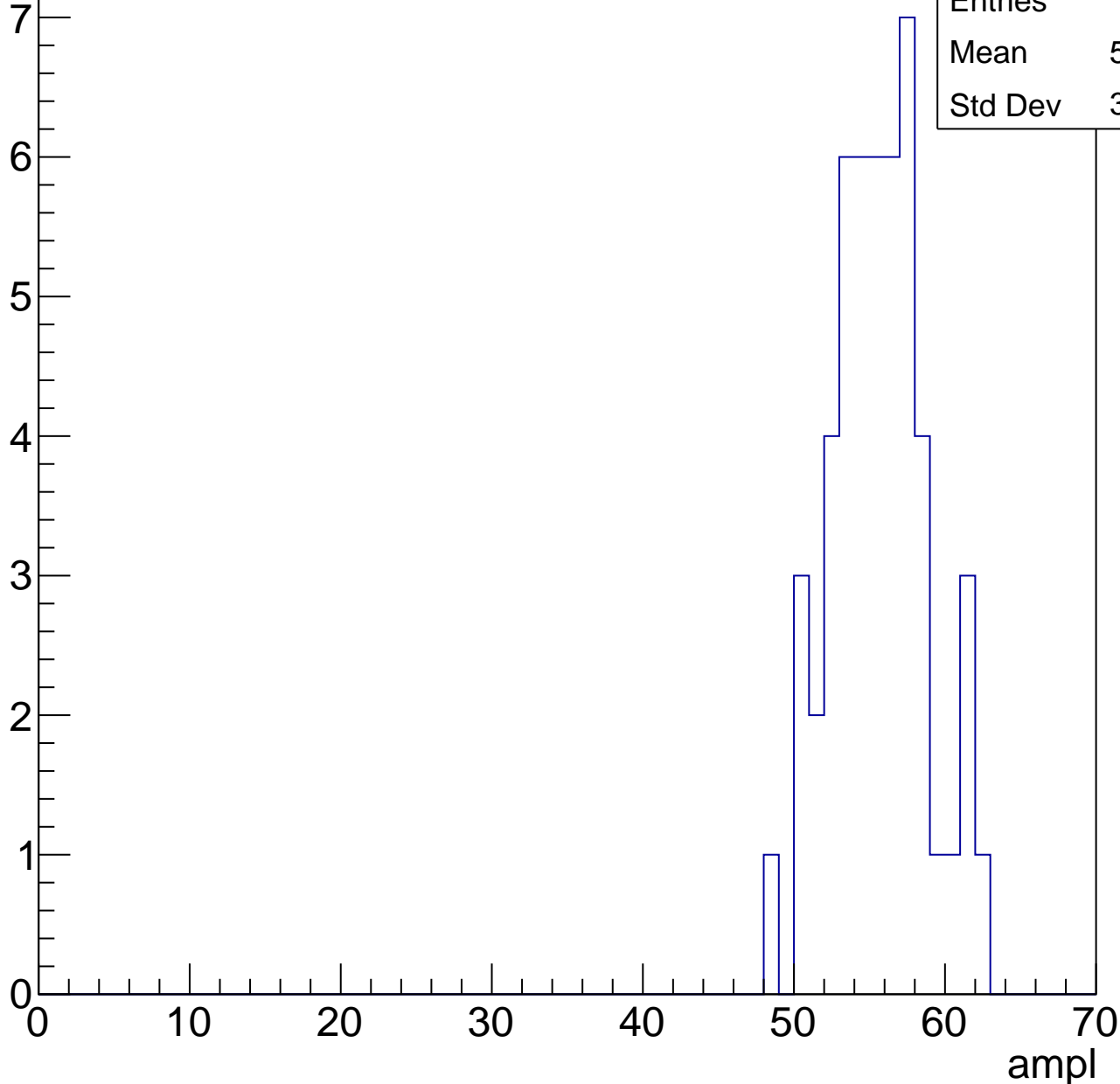


Entries	71
Mean	48.62
Std Dev	3.346

# B1L100S, U2-ch65, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

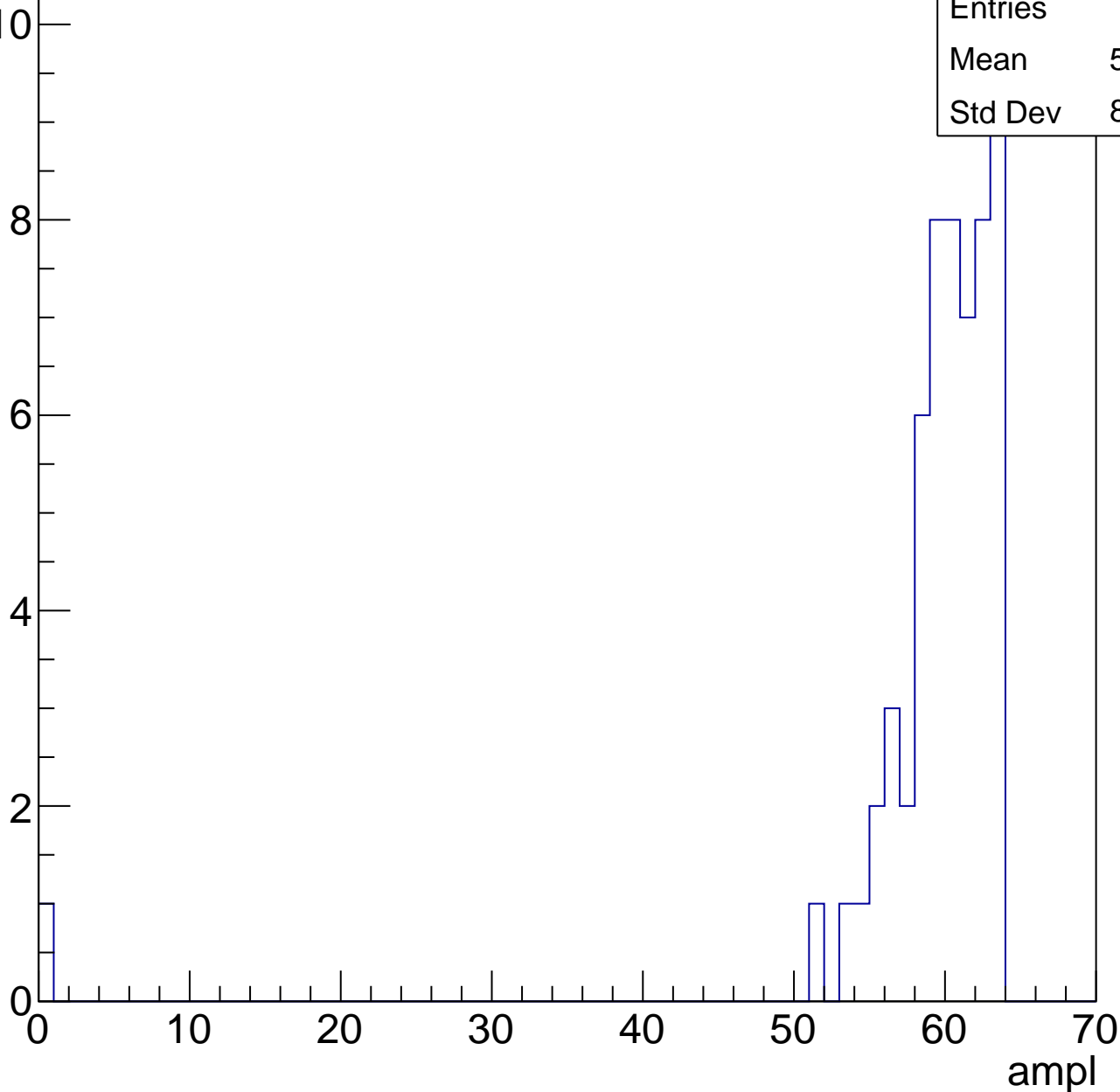


# B1L100S, U2-ch65, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

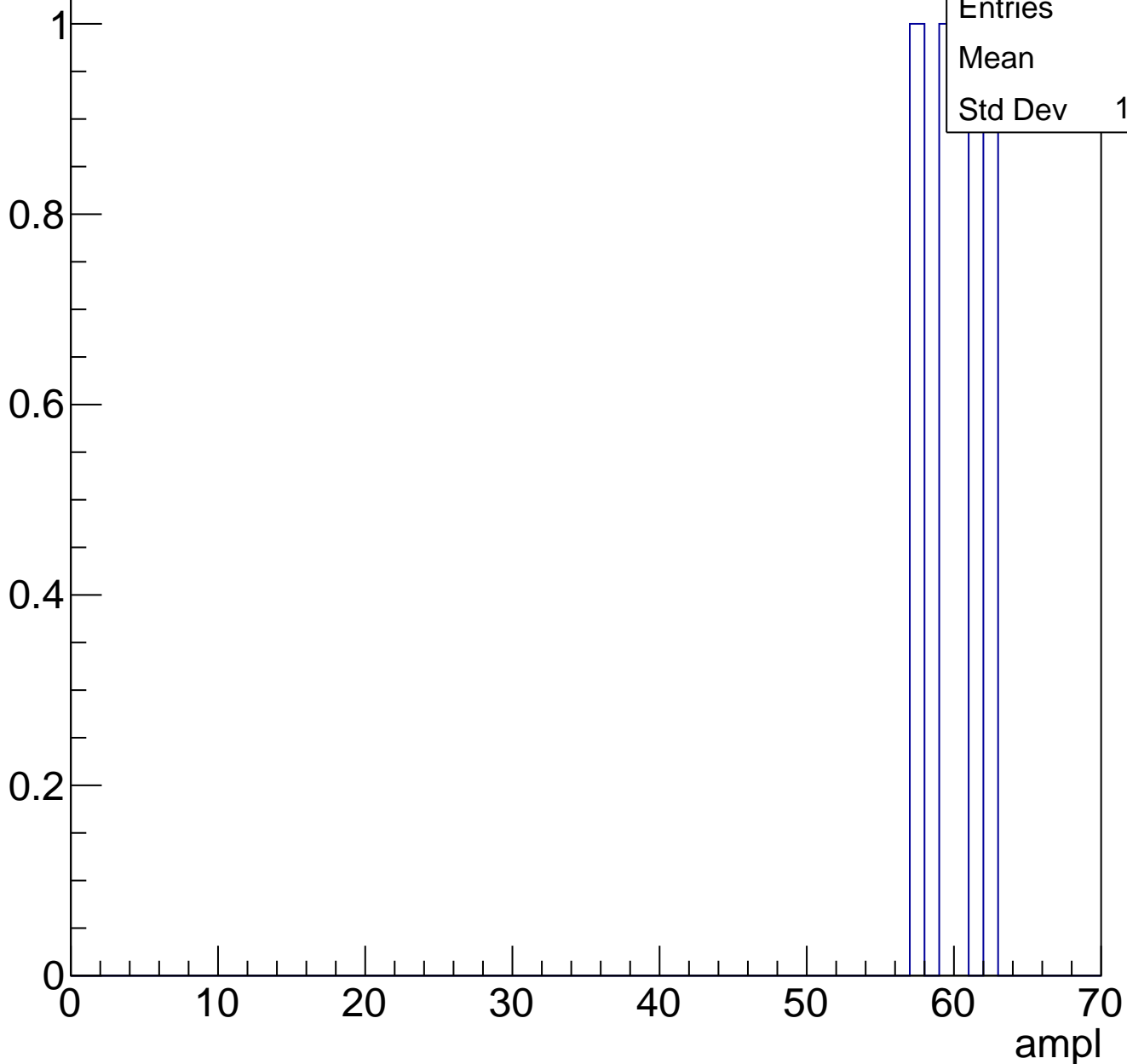
Entries	58
Mean	58.67
Std Dev	8.243



# B1L100S, U2-ch65, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry





# B1L100S, U2-ch65, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



# B1L100S, U2-ch66, adc0

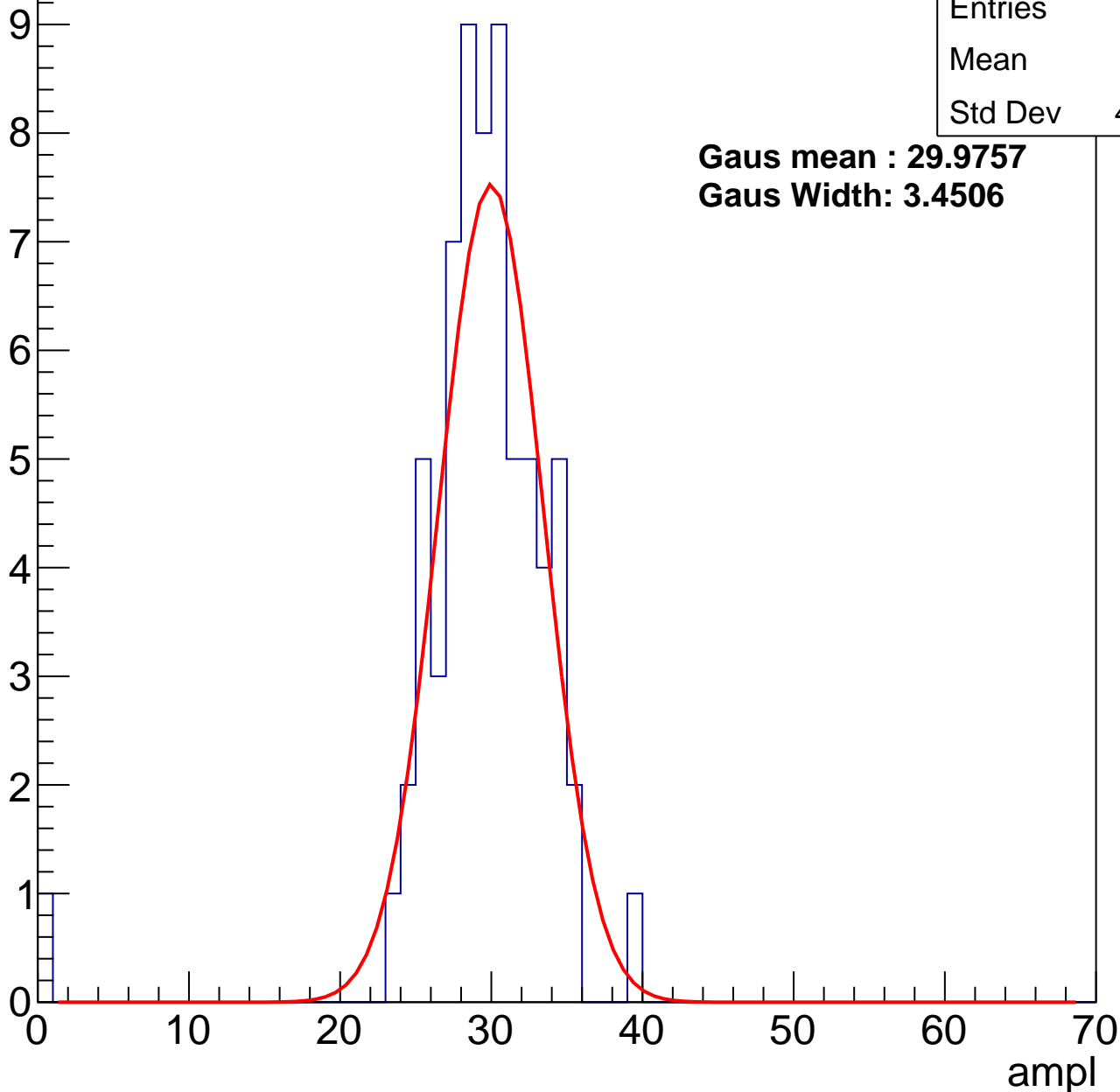
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	67
Mean	29
Std Dev	4.741

**Gaus mean : 29.9757**

**Gaus Width: 3.4506**



# B1L100S, U2-ch66, adc1

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	73
Mean	36.03
Std Dev	3.205

**Gaus mean : 36.5115**

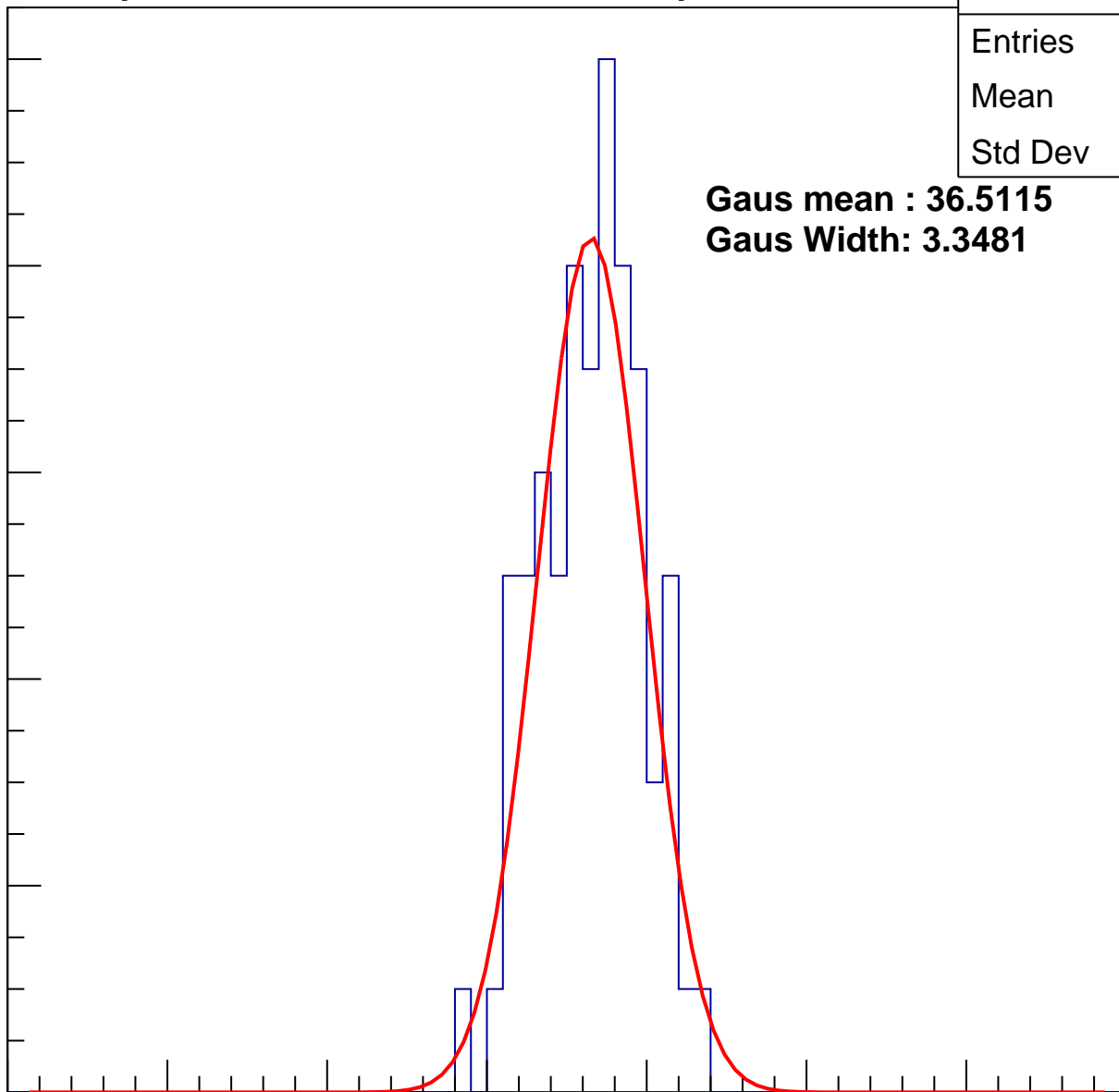
**Gaus Width: 3.3481**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B1L100S, U2-ch66, adc2

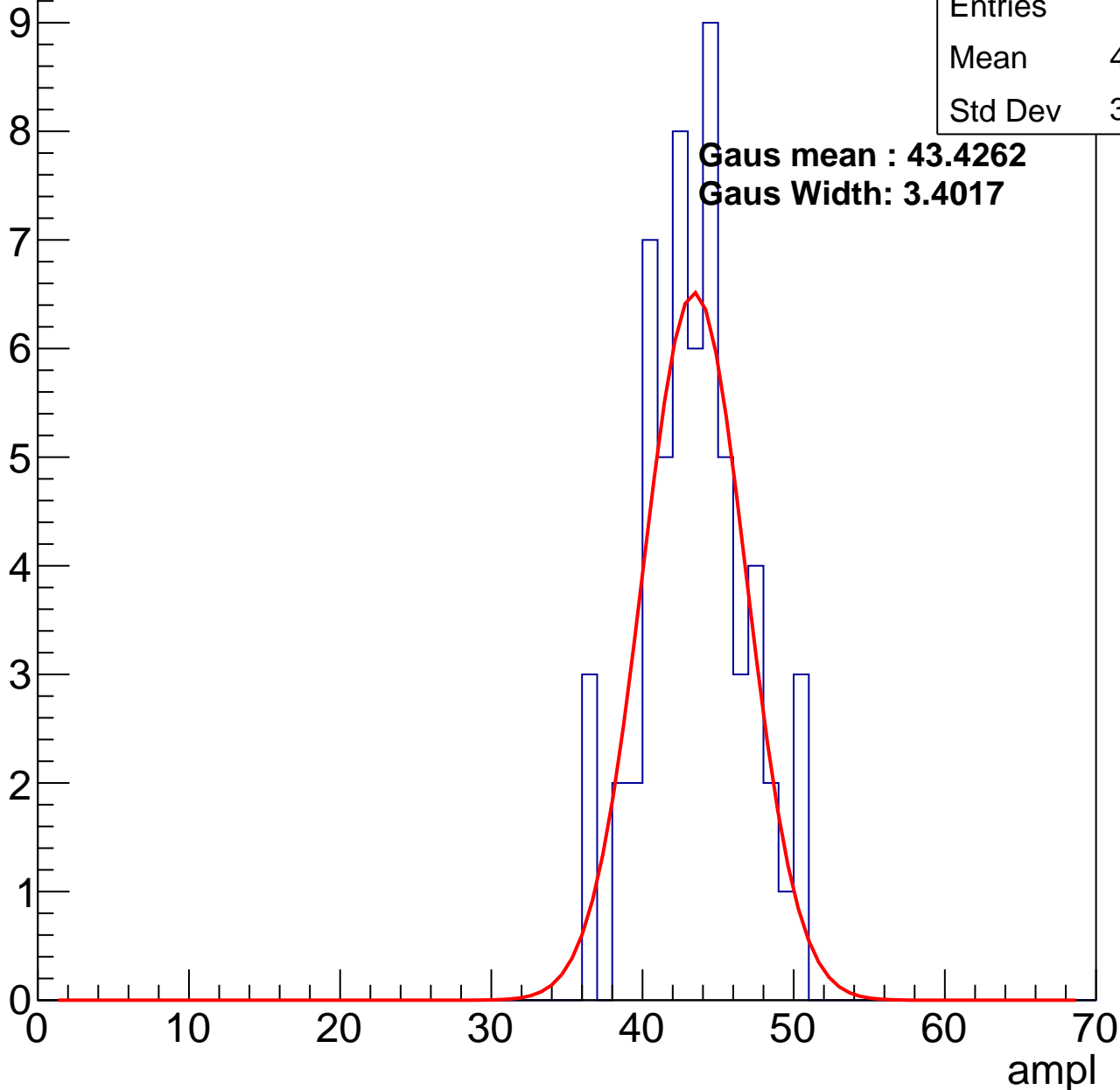
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	60
Mean	43.05
Std Dev	3.349

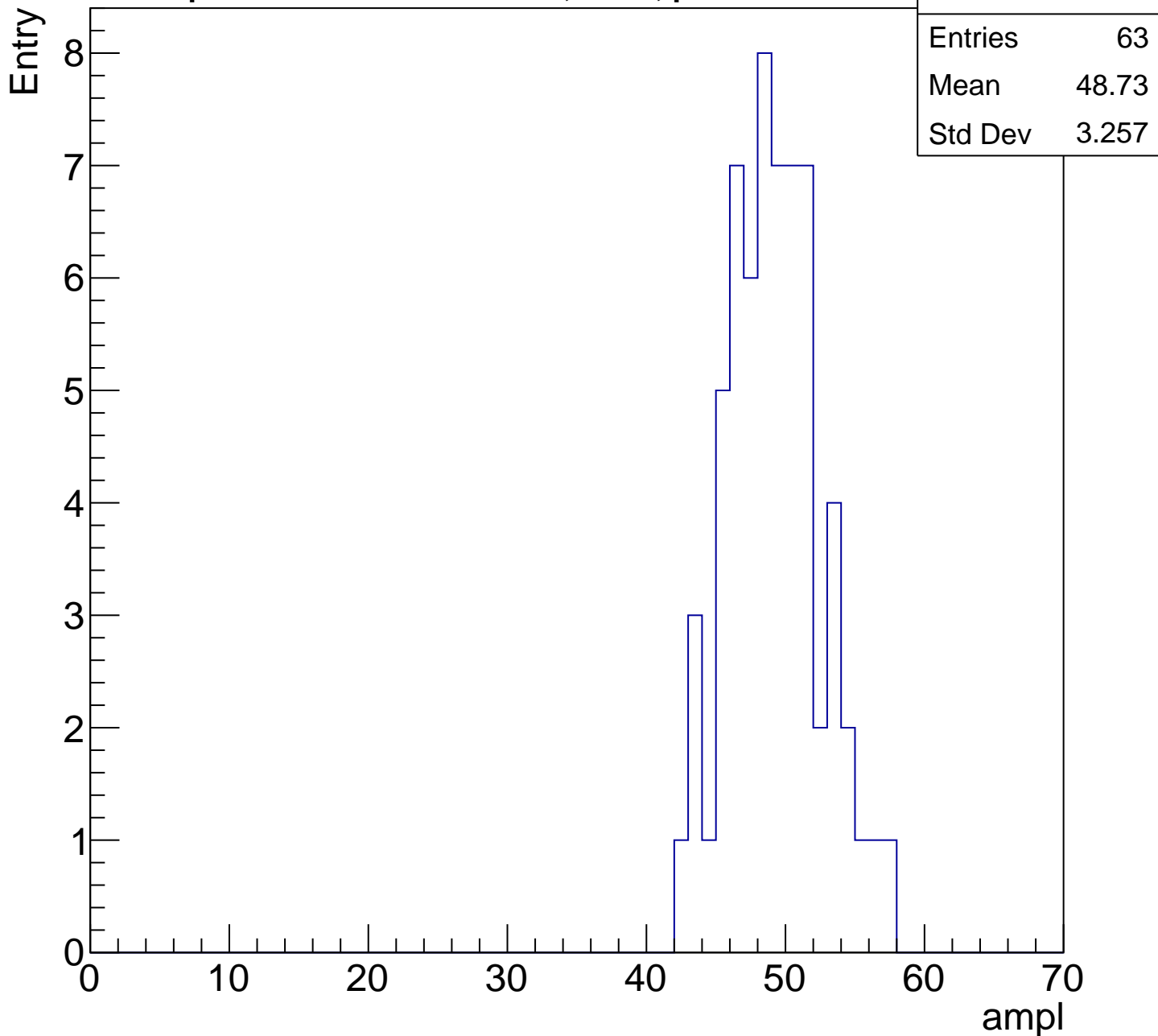
**Gaus mean : 43.4262**

**Gaus Width: 3.4017**



# B1L100S, U2-ch66, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

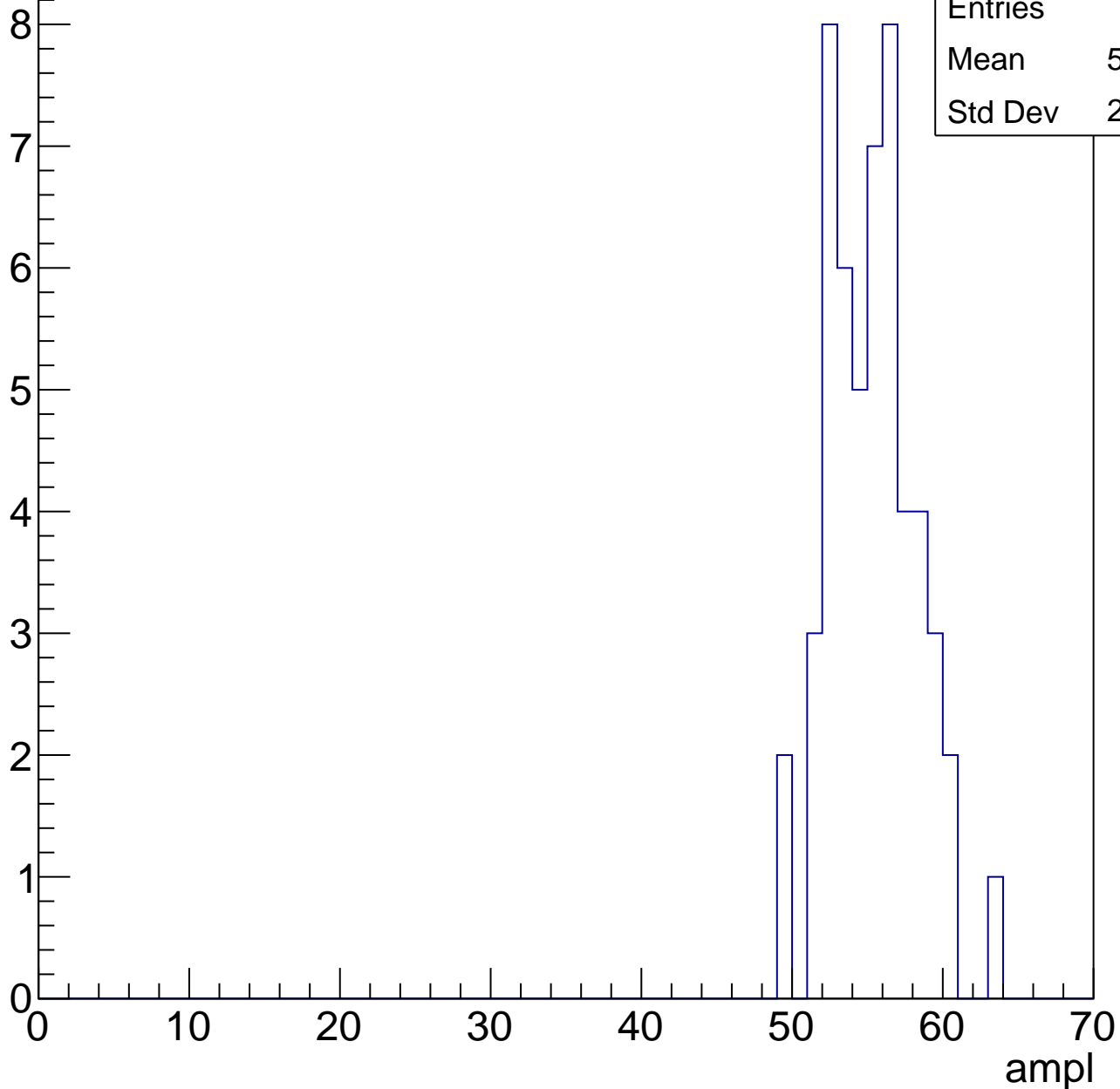


# B1L100S, U2-ch66, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	53
Mean	54.87
Std Dev	2.888

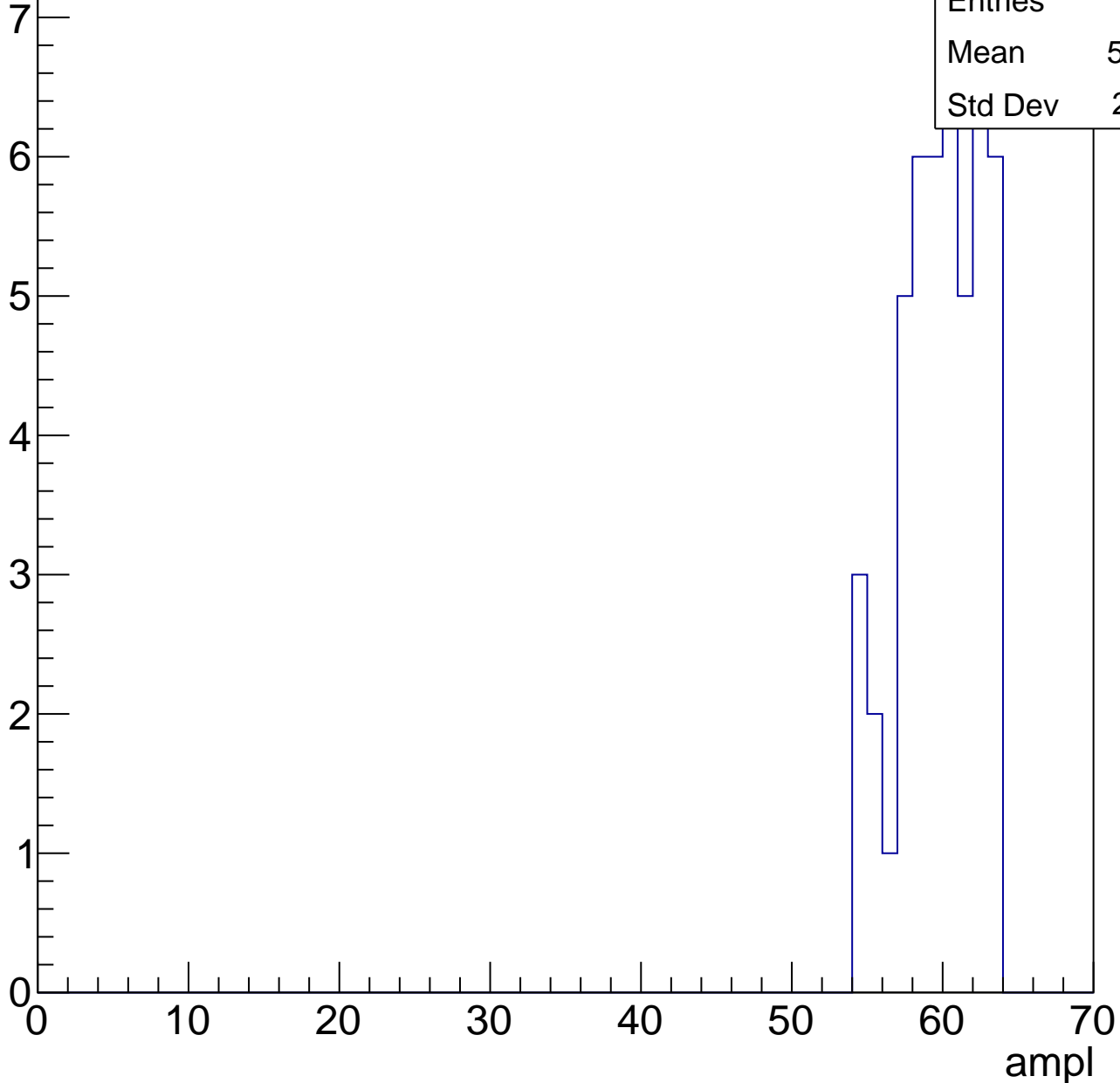


# B1L100S, U2-ch66, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	48
Mean	59.42
Std Dev	2.581

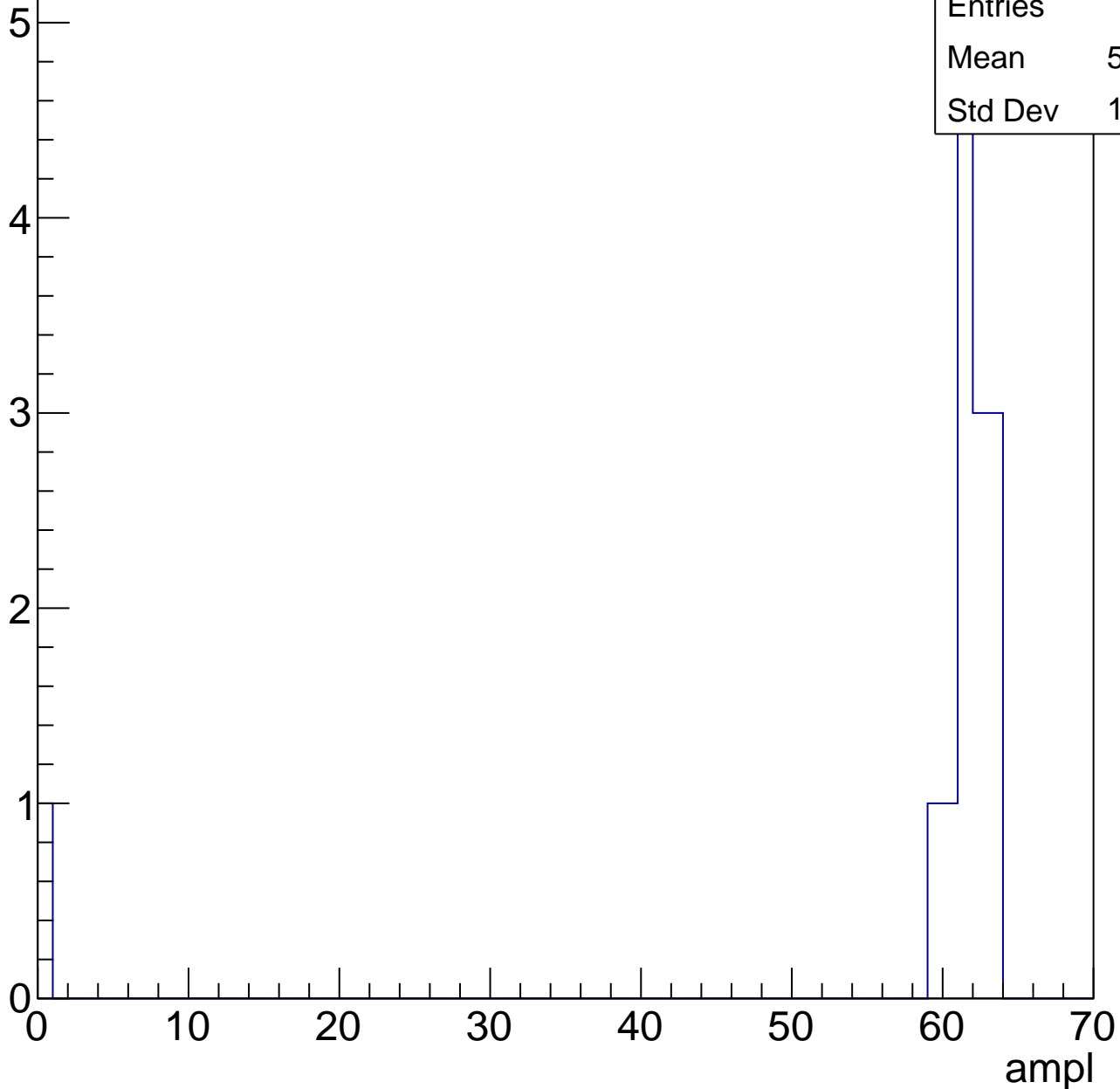


# B1L100S, U2-ch66, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	14
Mean	57.07
Std Dev	15.87





# B1L100S, U2-ch66, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



# B1L100S, U2-ch67, adc0

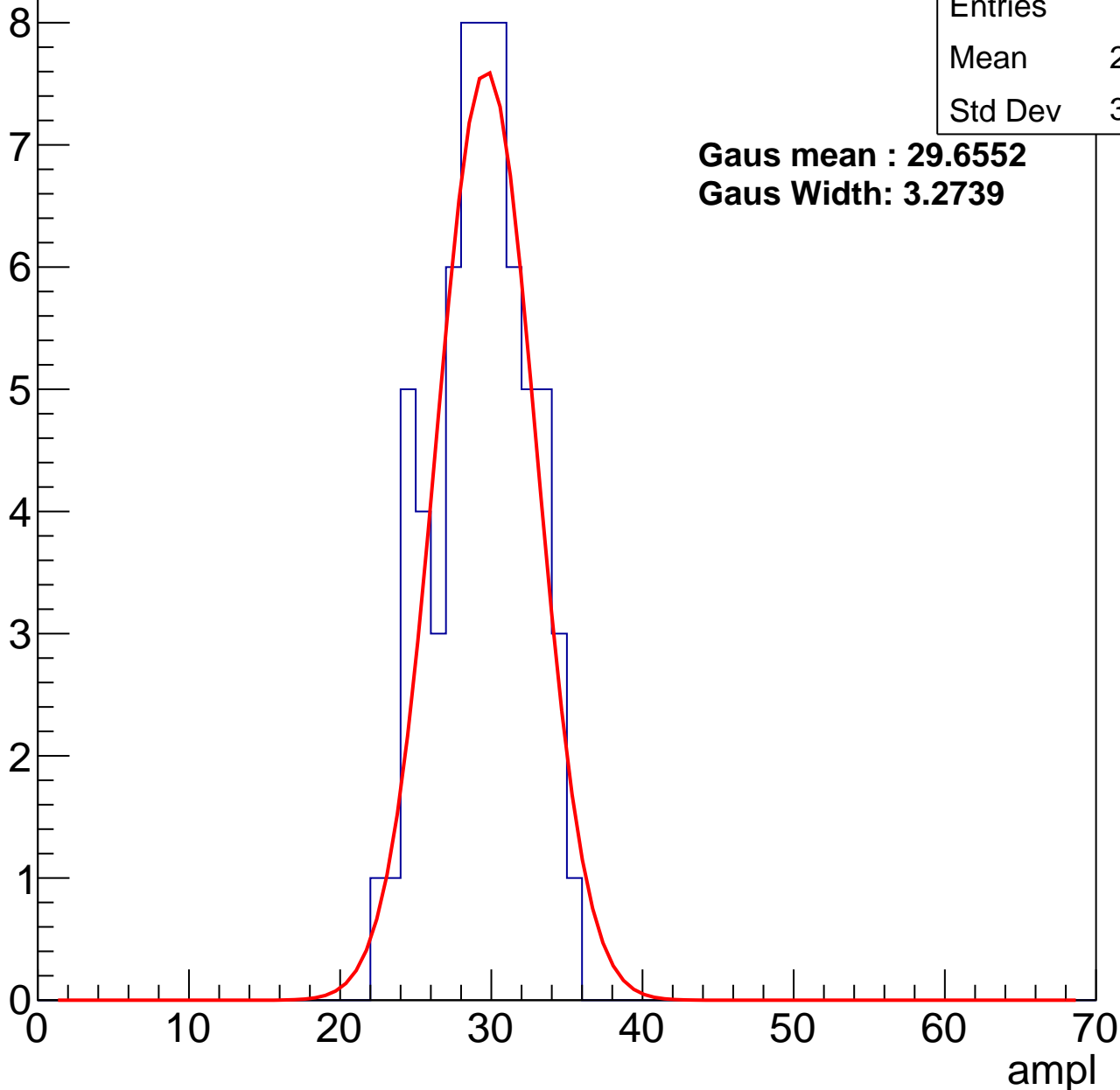
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	64
Mean	28.89
Std Dev	3.062

**Gaus mean : 29.6552**

**Gaus Width: 3.2739**



# B1L100S, U2-ch67, adc1

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	90
Mean	36.13
Std Dev	5.425

**Gaus mean : 37.2690**

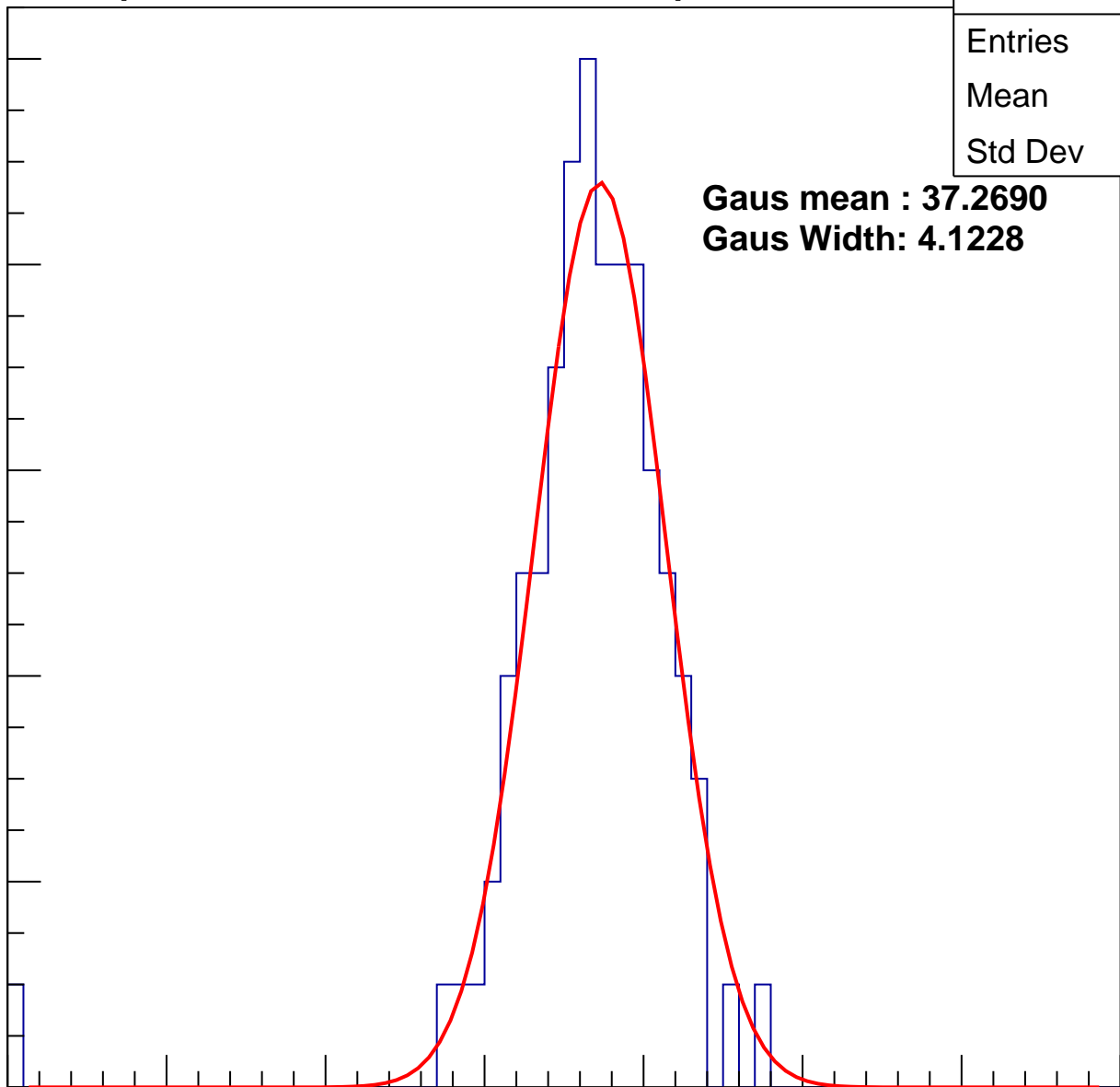
**Gaus Width: 4.1228**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B1L100S, U2-ch67, adc2

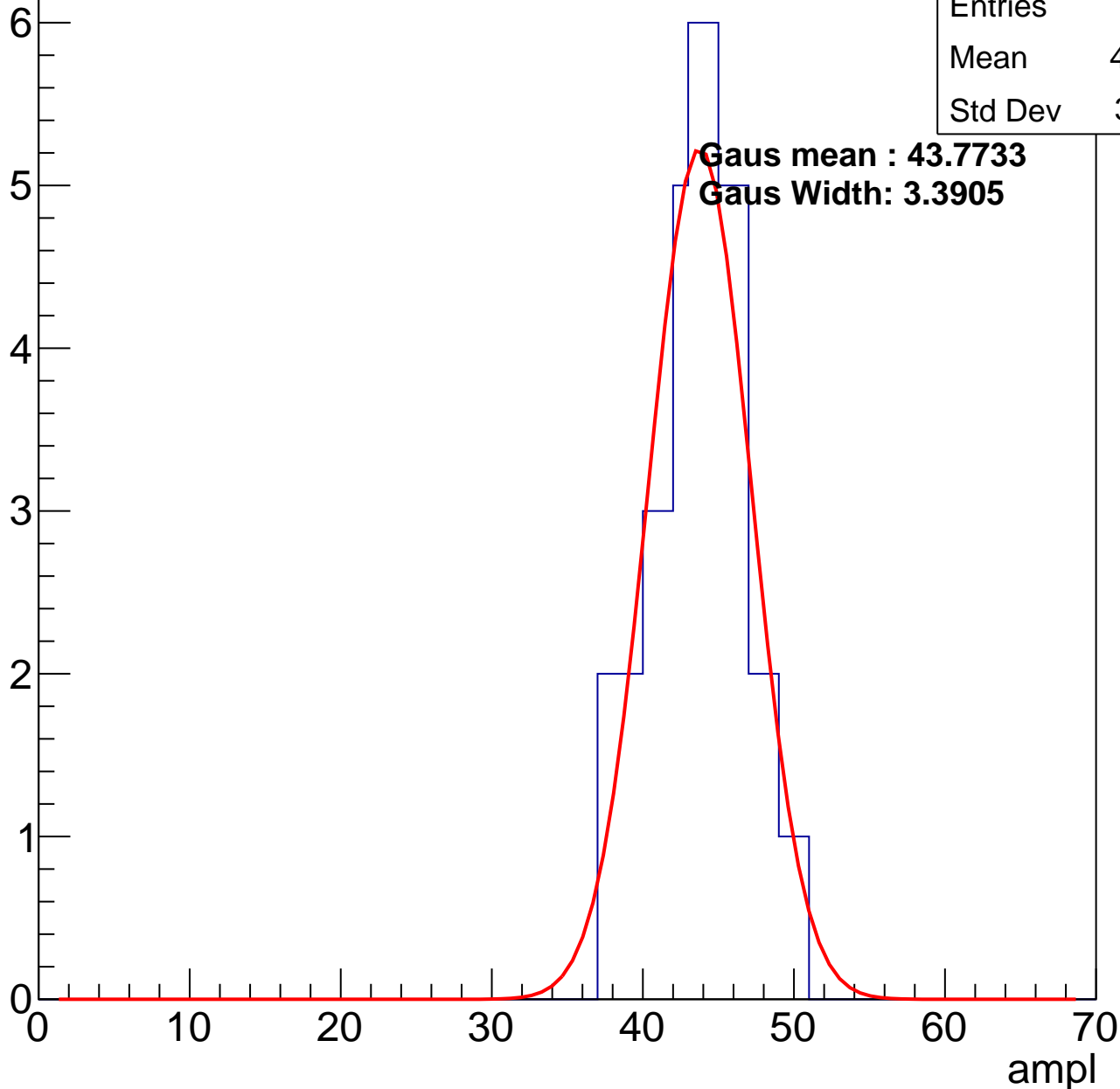
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	45
Mean	43.27
Std Dev	3.101

**Gaus mean : 43.7733**

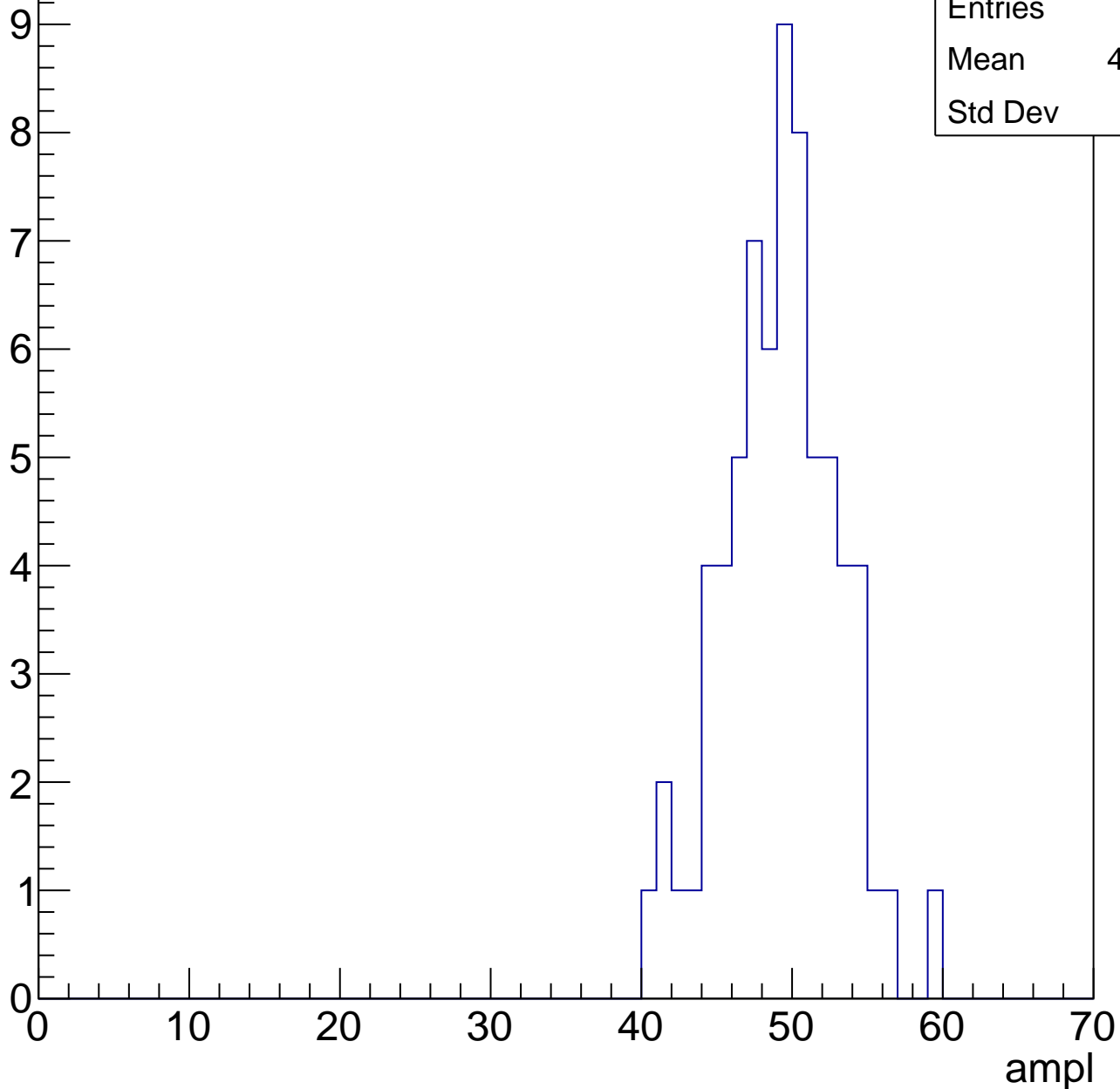
**Gaus Width: 3.3905**



# B1L100S, U2-ch67, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

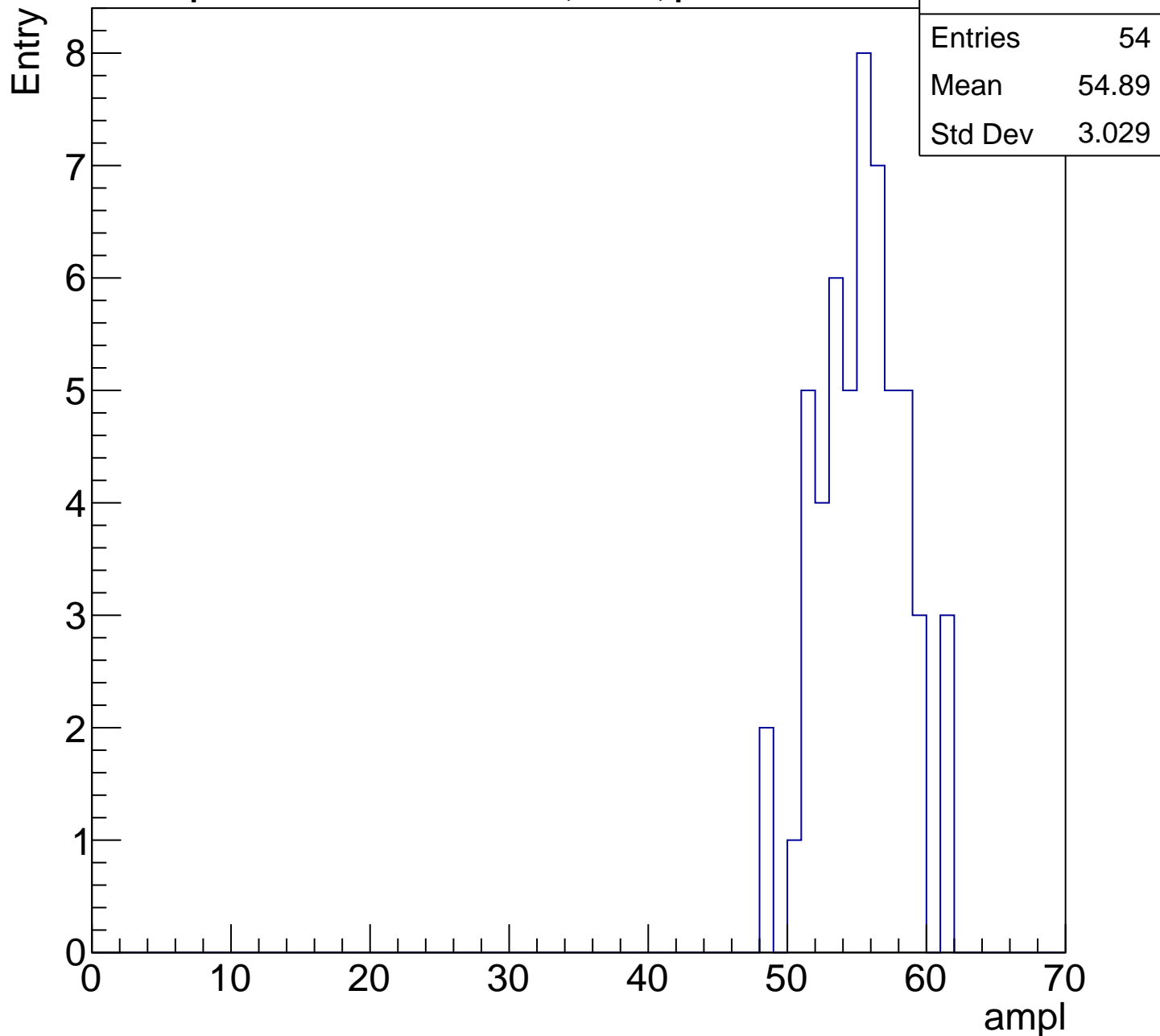
Entry



Entries	69
Mean	48.75
Std Dev	3.72

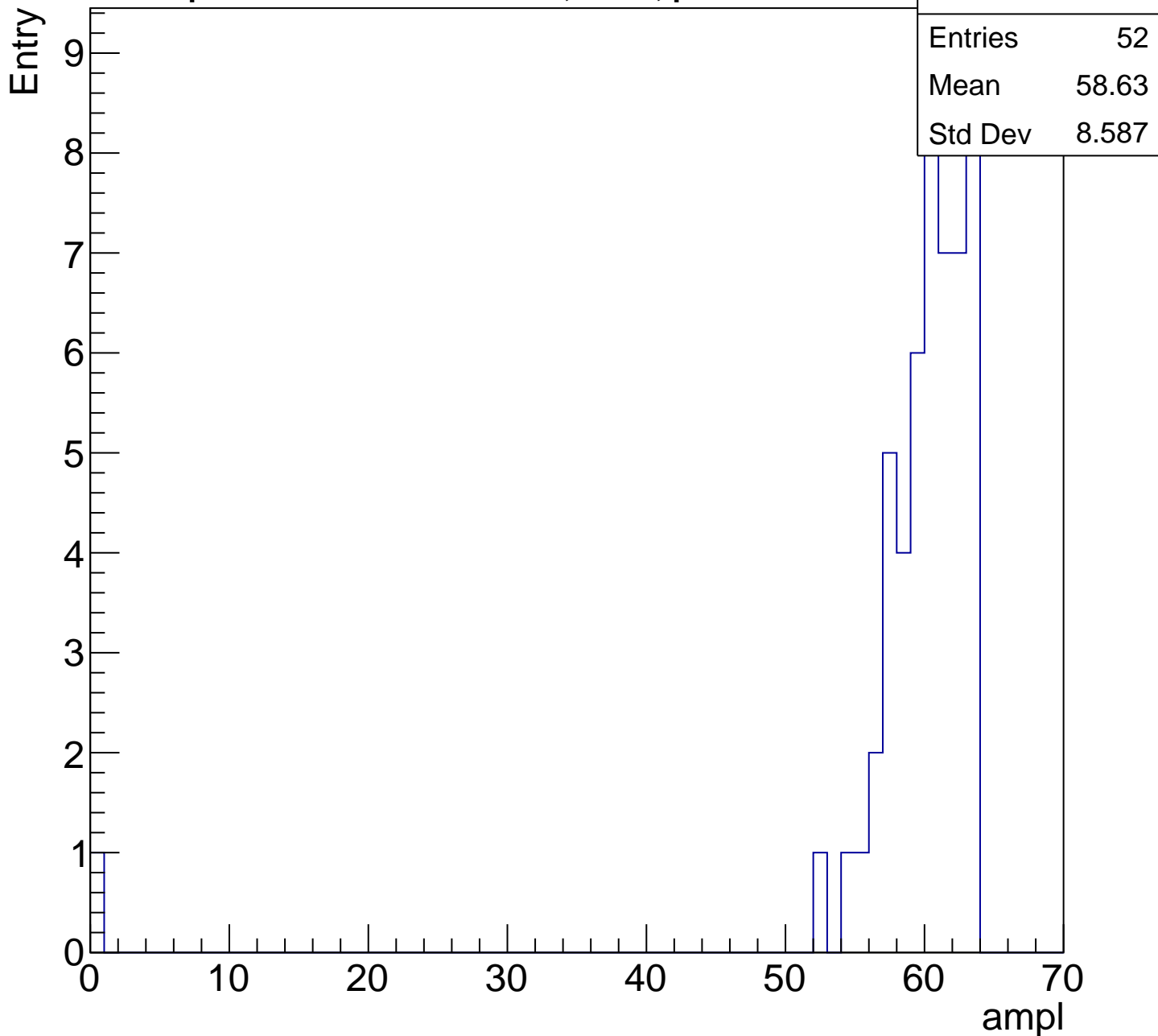
# B1L100S, U2-ch67, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2



# B1L100S, U2-ch67, adc5

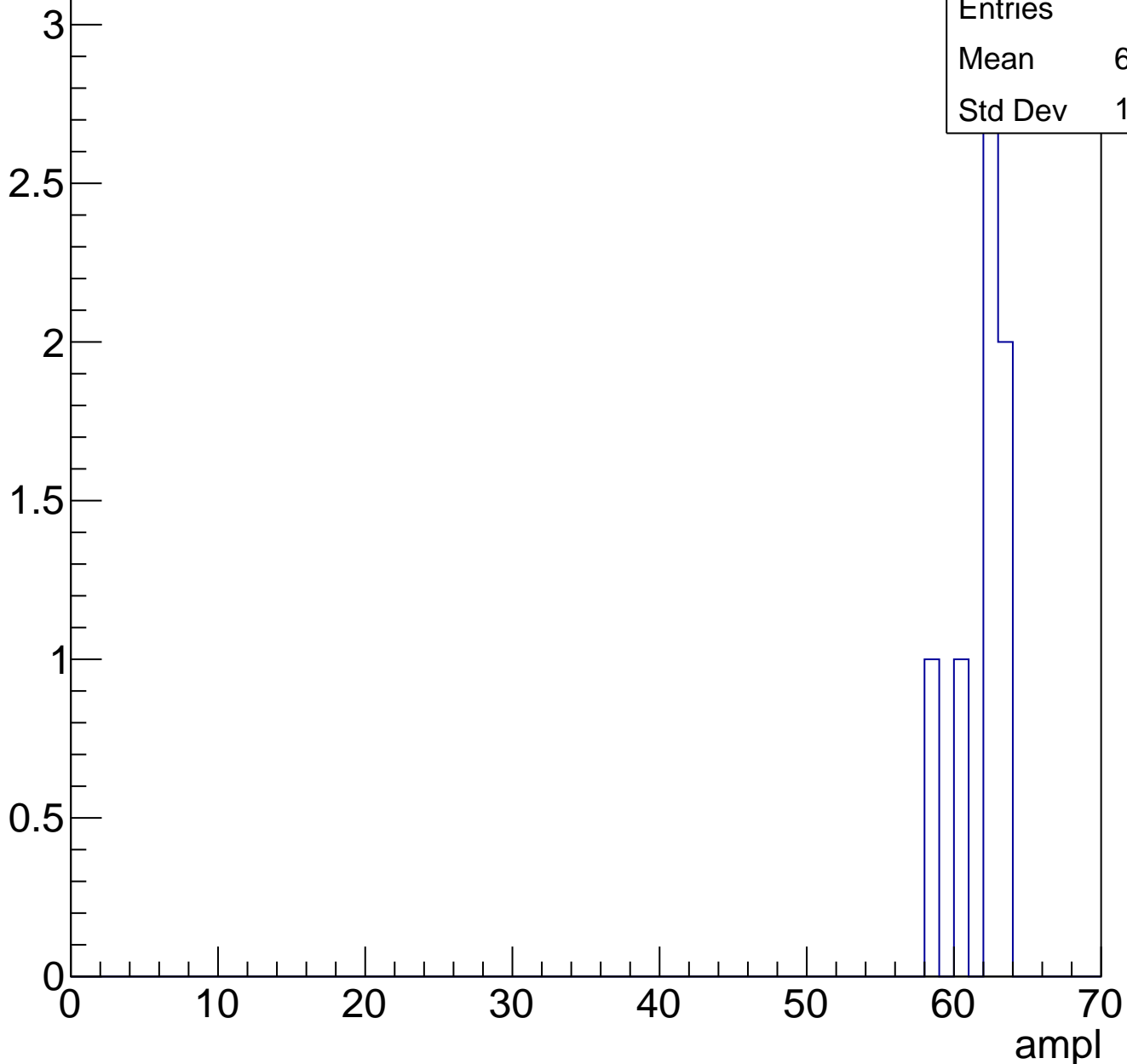
calib\_packv5\_042523\_0143.root, FC#4, port A2



# B1L100S, U2-ch67, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry





# B1L100S, U2-ch67, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L100S, U2-ch68, adc0

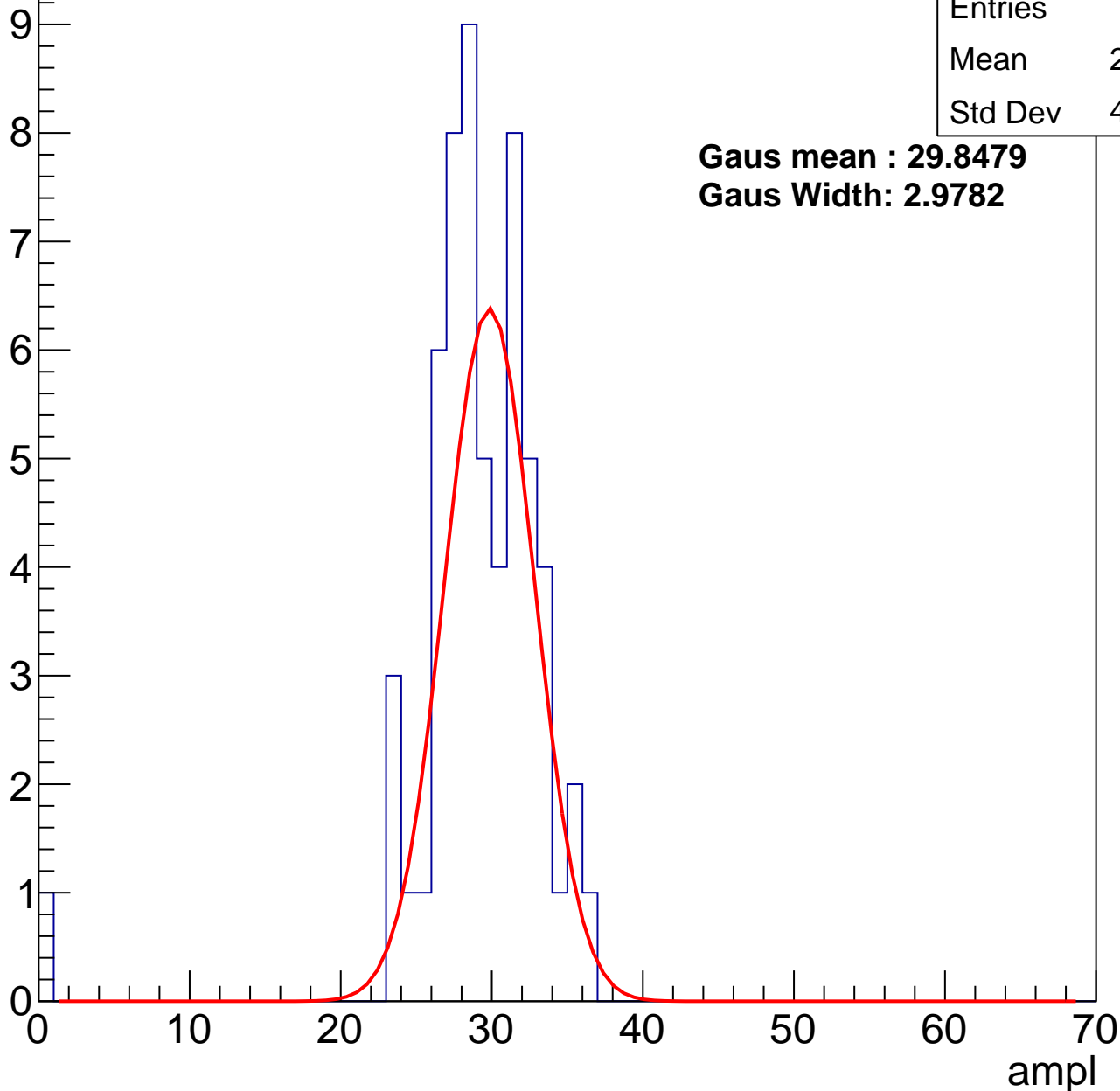
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	59
Mean	28.59
Std Dev	4.812

**Gaus mean : 29.8479**

**Gaus Width: 2.9782**



# B1L100S, U2-ch68, adc1

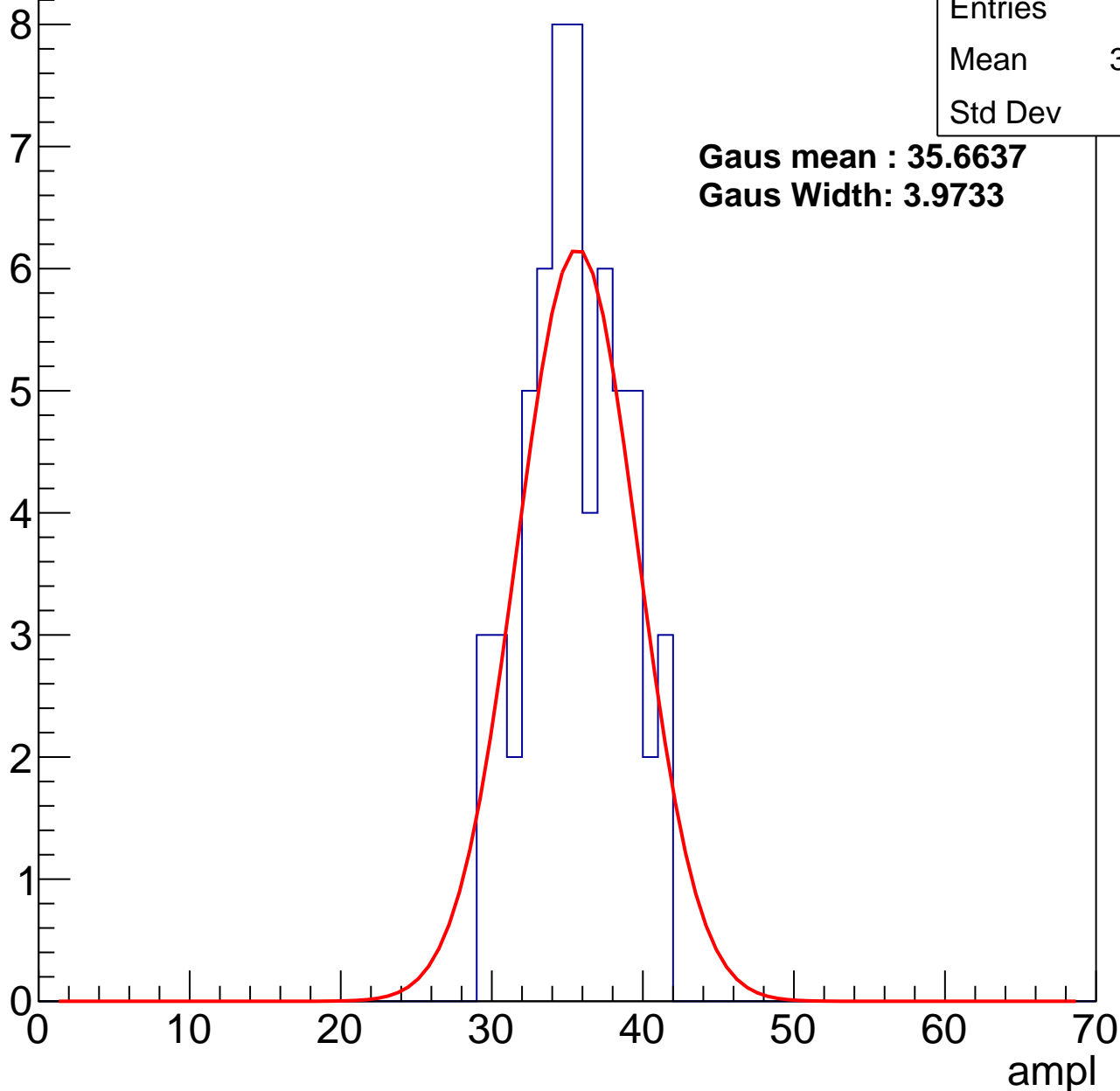
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	60
Mean	35.05
Std Dev	3.17

**Gaus mean : 35.6637**

**Gaus Width: 3.9733**



# B1L100S, U2-ch68, adc2

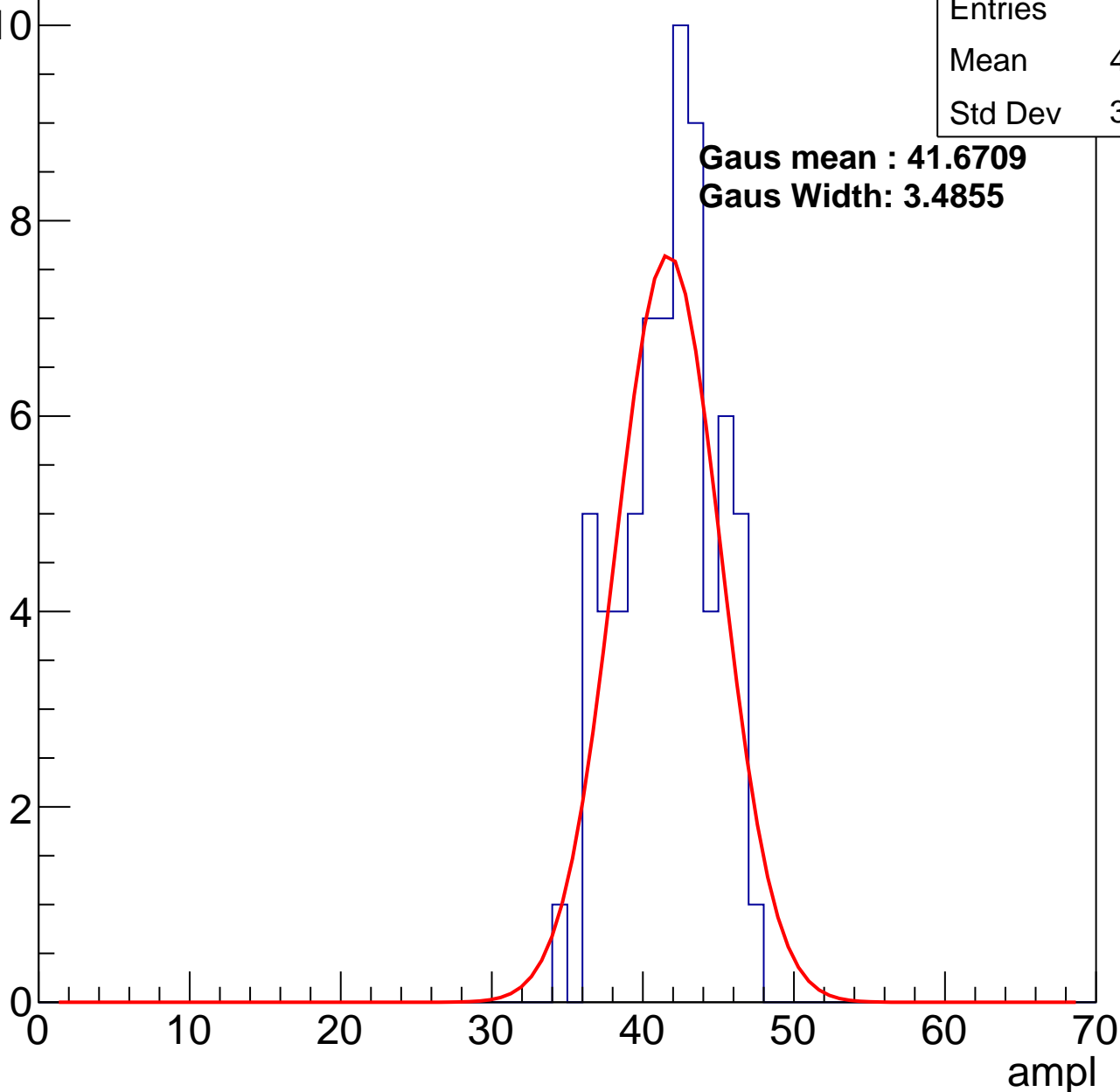
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	68
Mean	41.26
Std Dev	3.056

**Gaus mean : 41.6709**

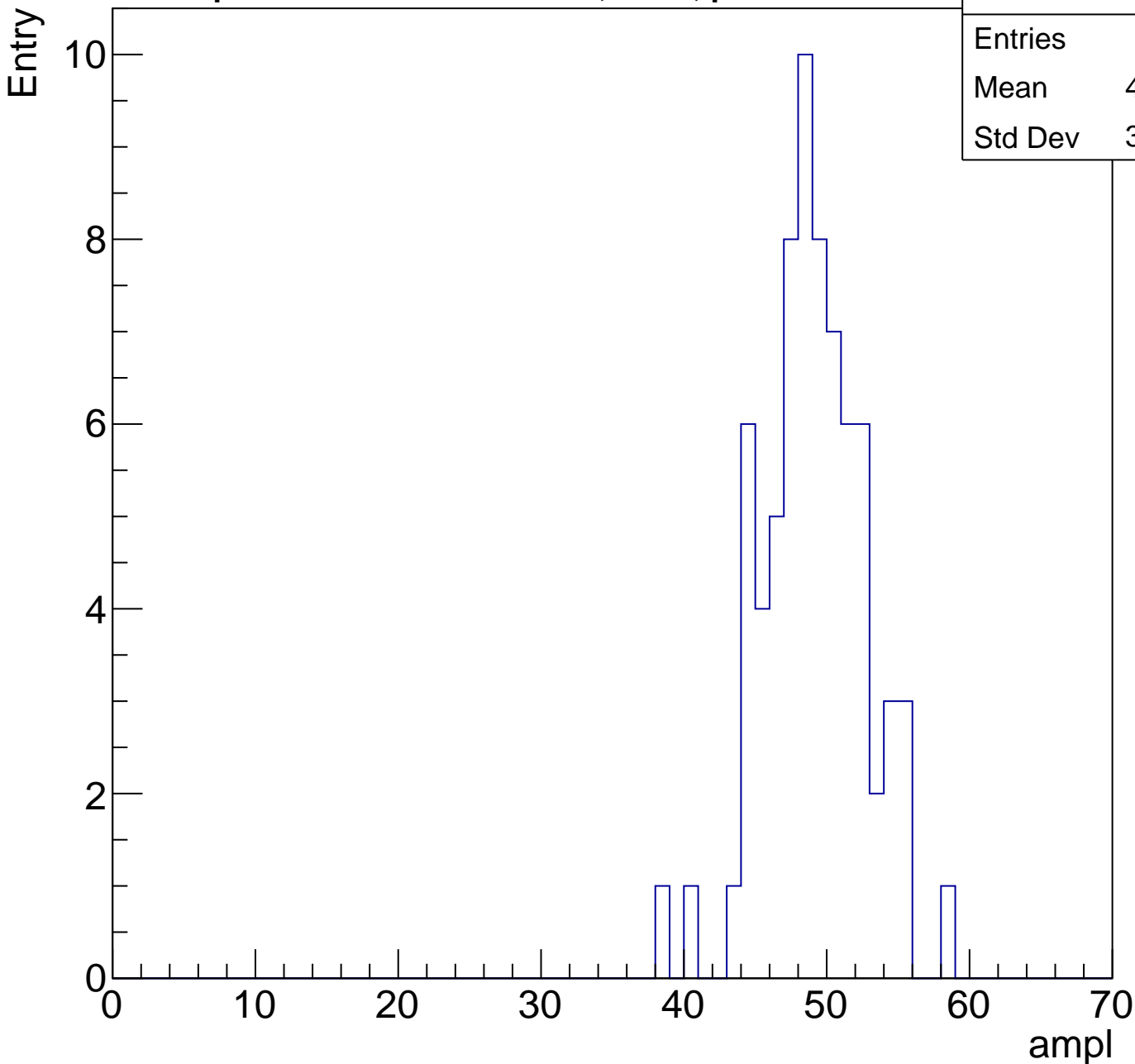
**Gaus Width: 3.4855**



# B1L100S, U2-ch68, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	72
Mean	48.64
Std Dev	3.556

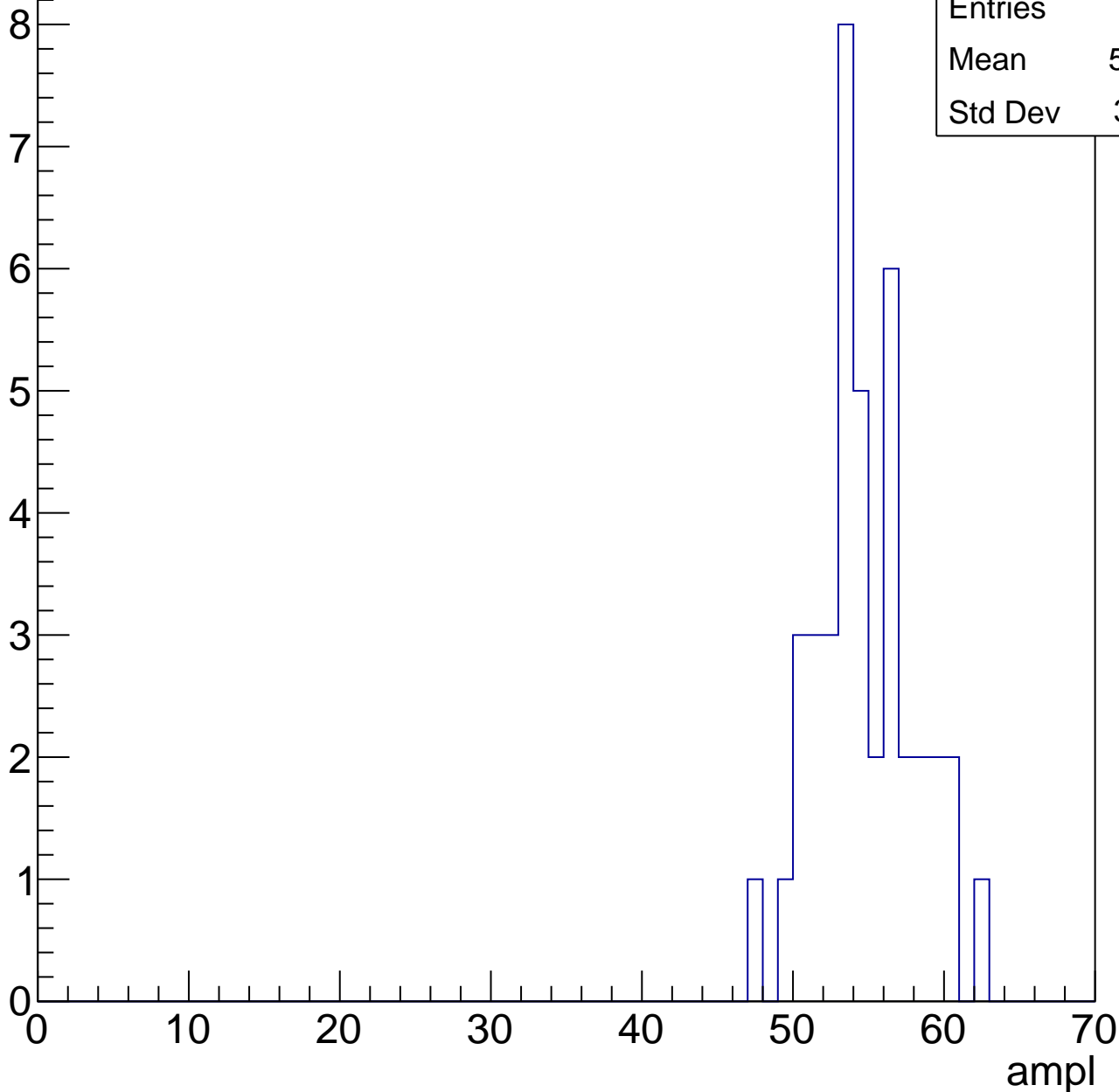


# B1L100S, U2-ch68, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	41
Mean	54.27
Std Dev	3.231

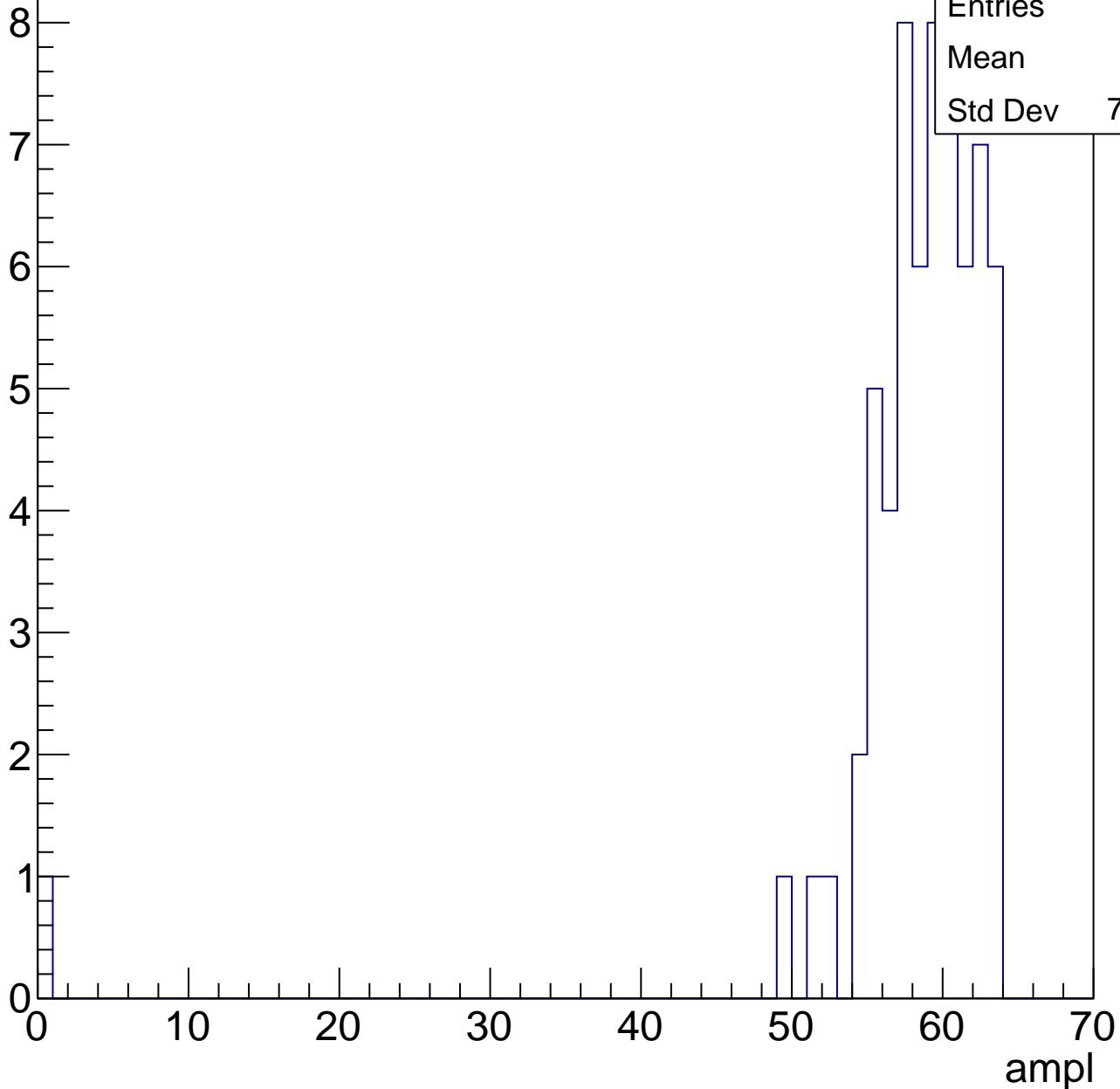


# B1L100S, U2-ch68, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

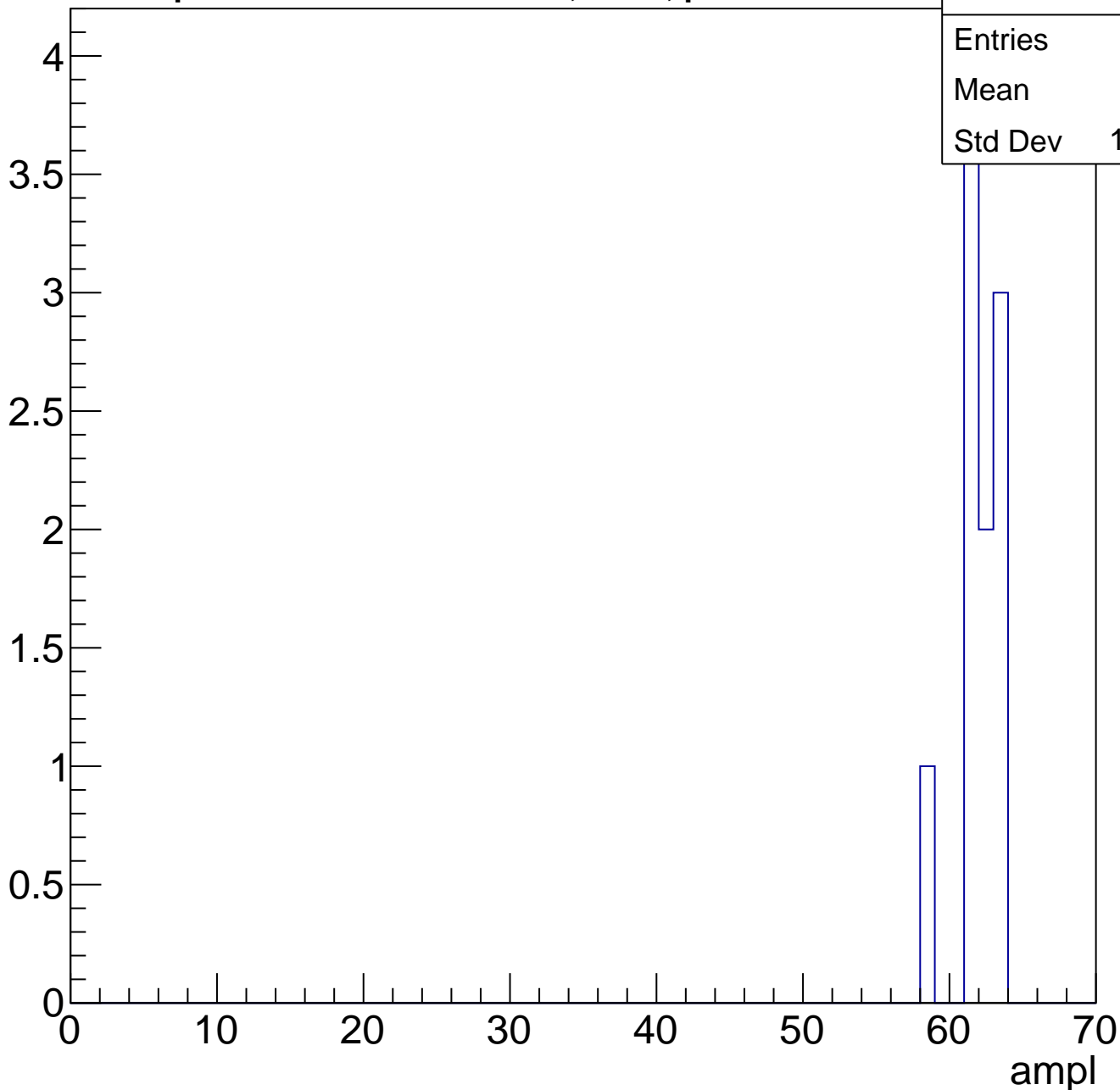
Entries	64
Mean	57.7
Std Dev	7.887



# B1L100S, U2-ch68, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry





# B1L100S, U2-ch68, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



# B1L100S, U2-ch69, adc0

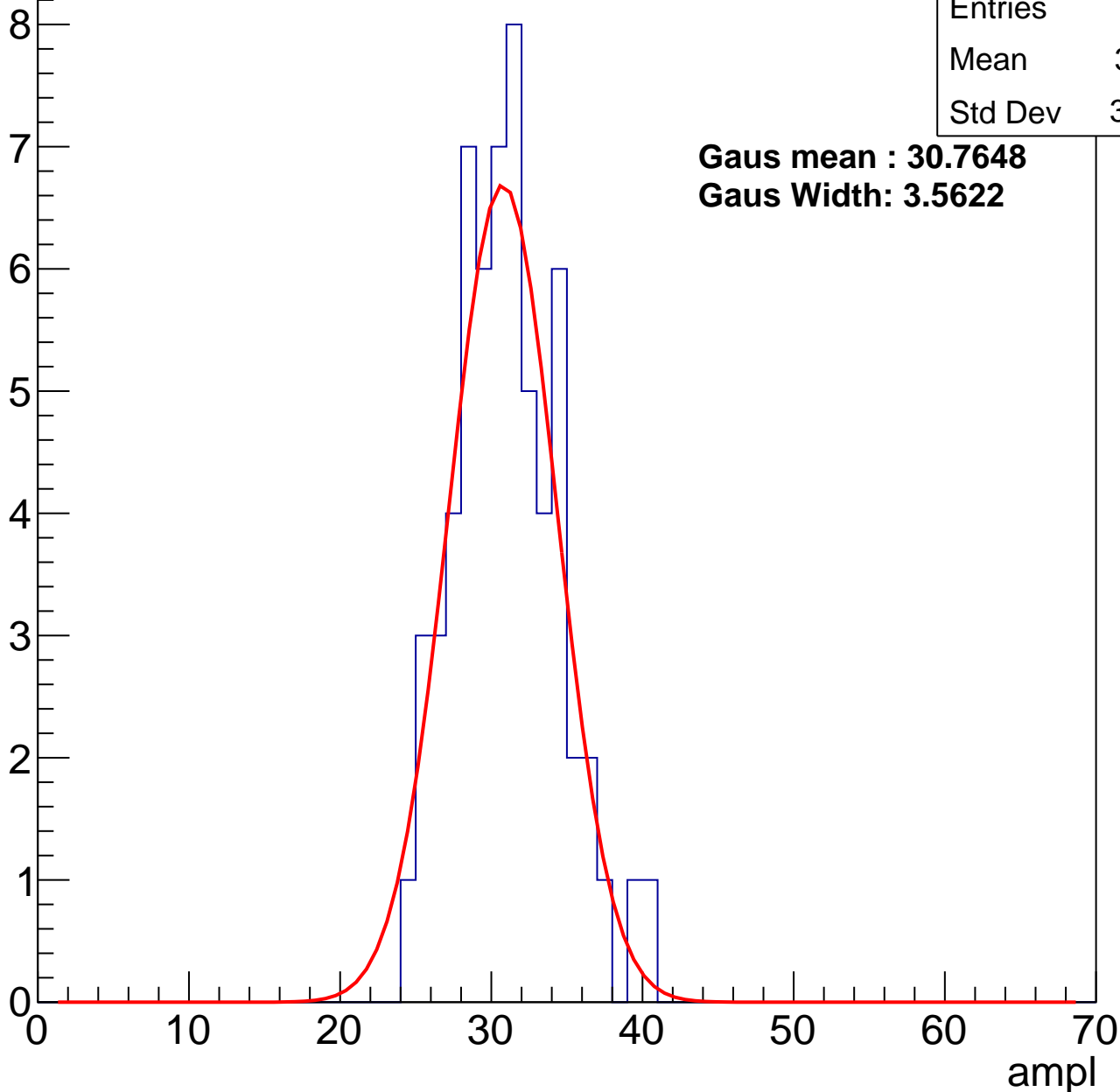
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	61
Mean	30.61
Std Dev	3.432

**Gaus mean : 30.7648**

**Gaus Width: 3.5622**



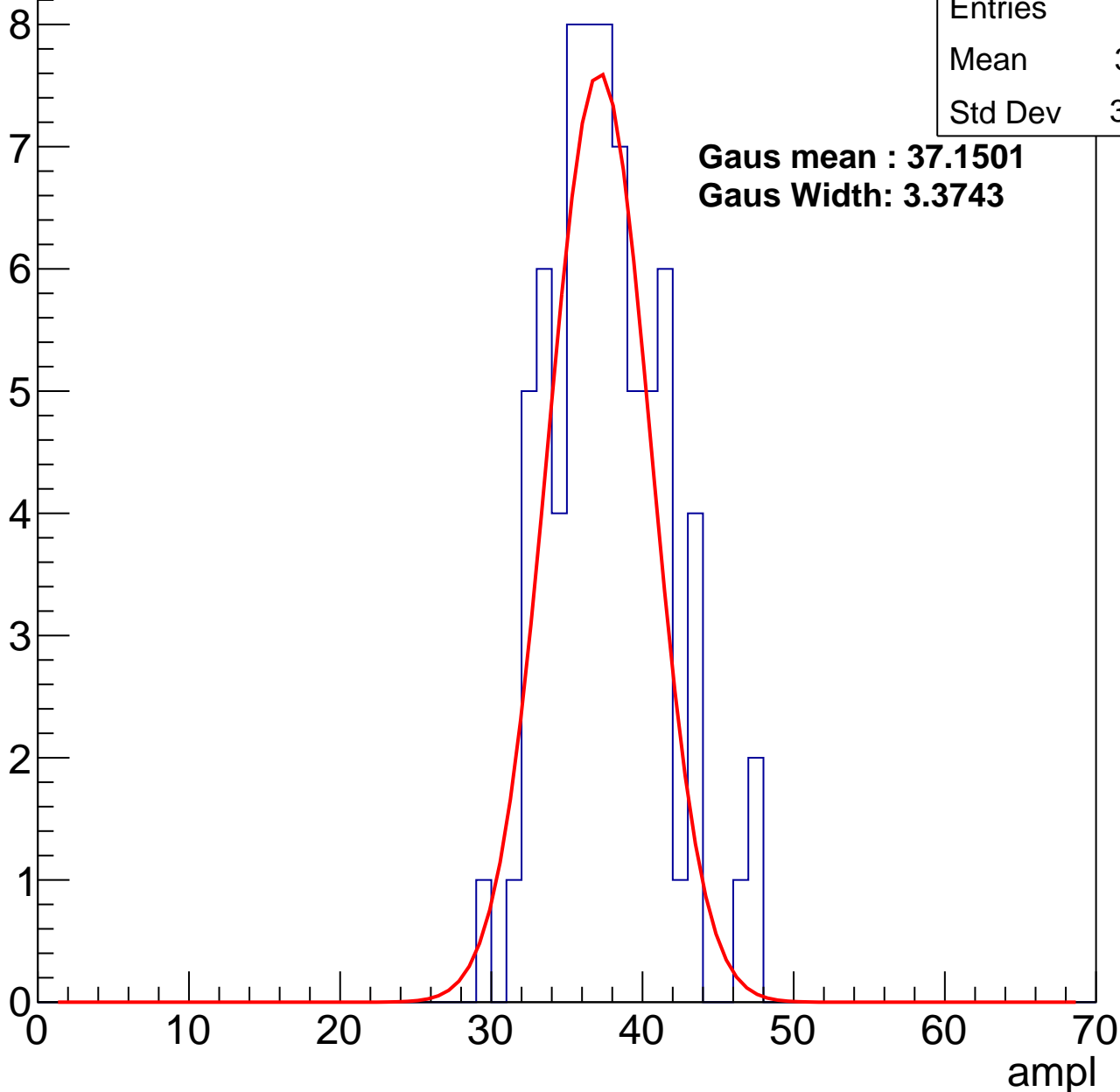
# B1L100S, U2-ch69, adc1

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

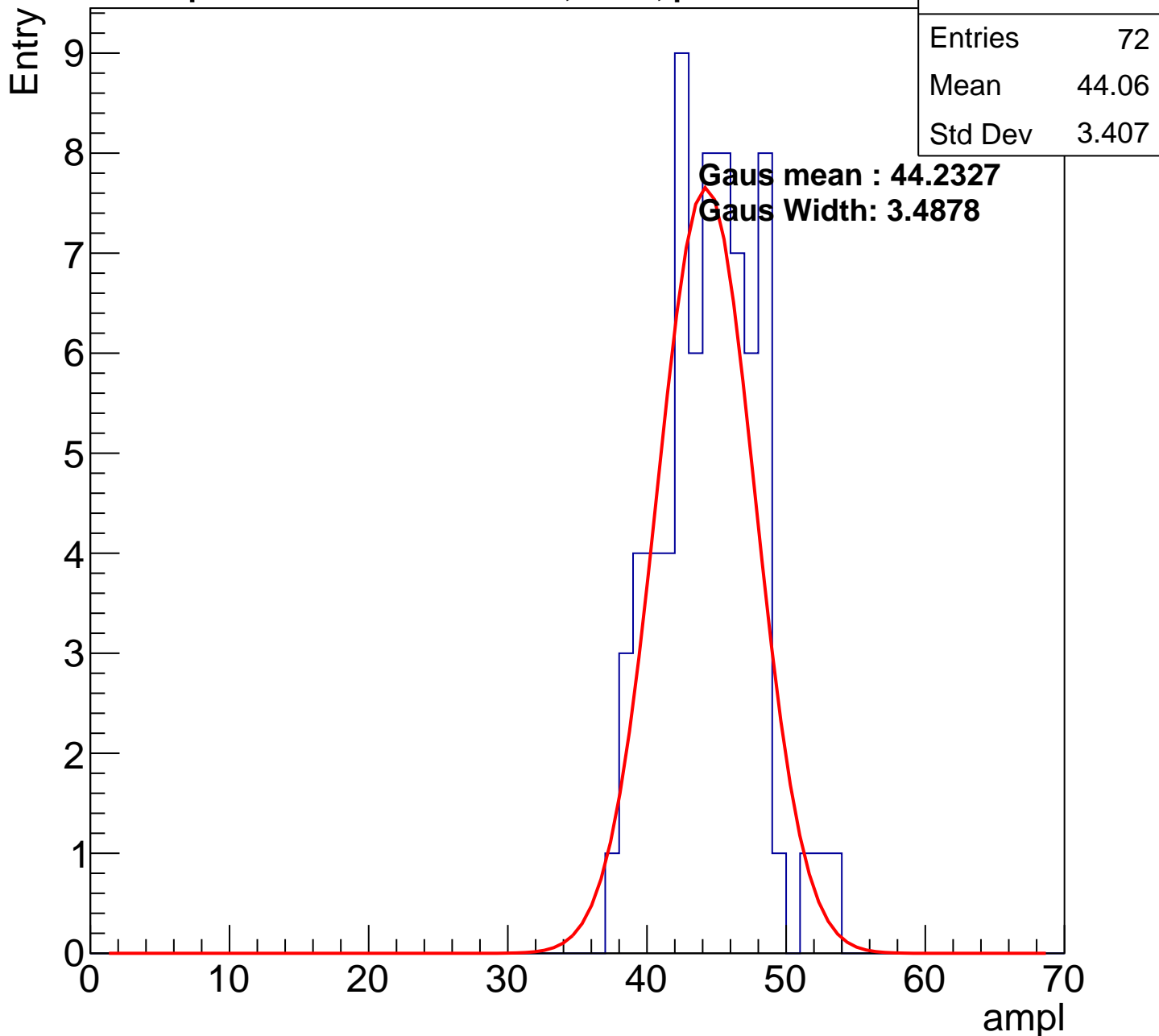
Entries	72
Mean	37.21
Std Dev	3.749

**Gaus mean : 37.1501**  
**Gaus Width: 3.3743**



# B1L100S, U2-ch69, adc2

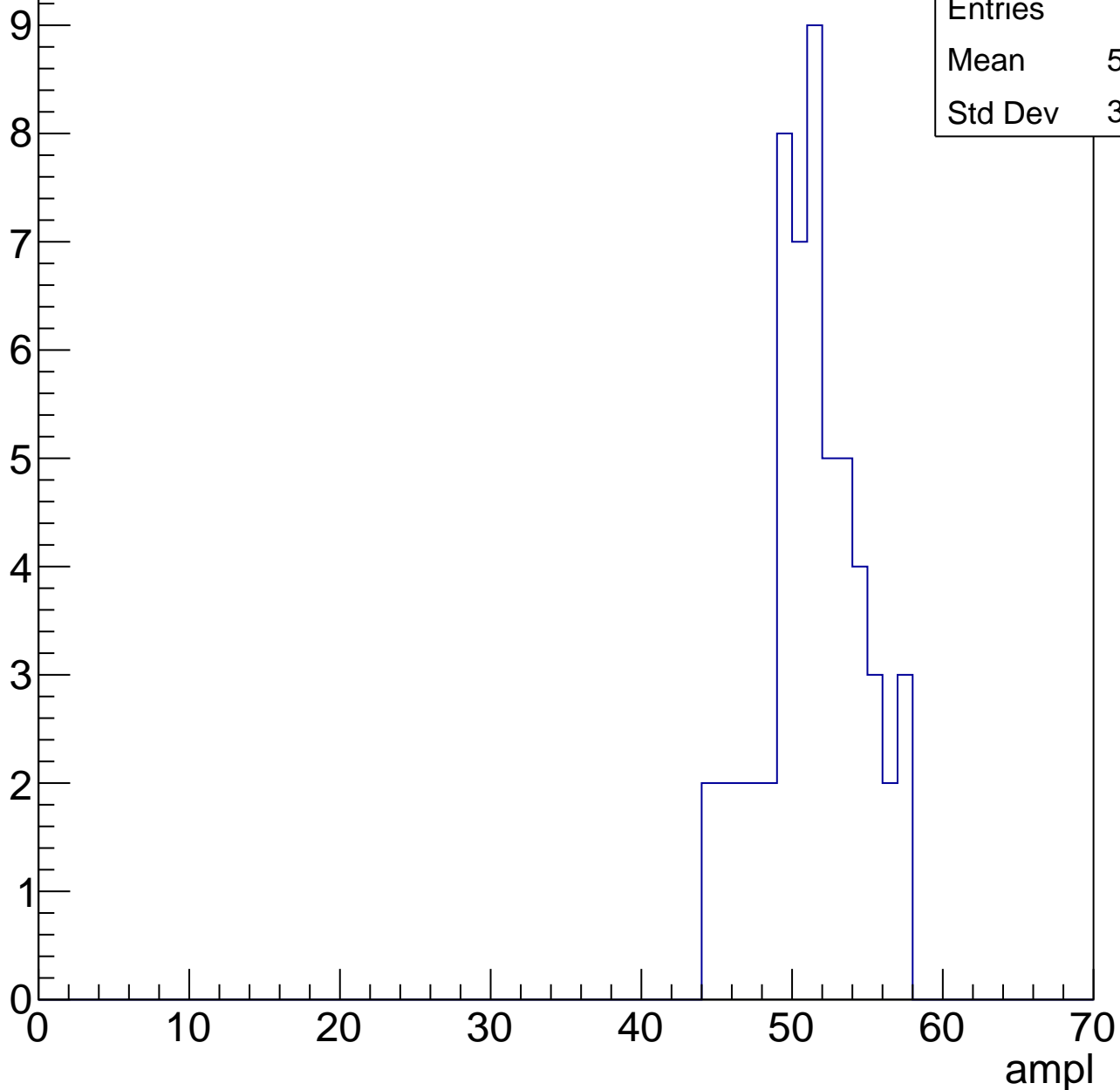
calib\_packv5\_042523\_0143.root, FC#4, port A2



# B1L100S, U2-ch69, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

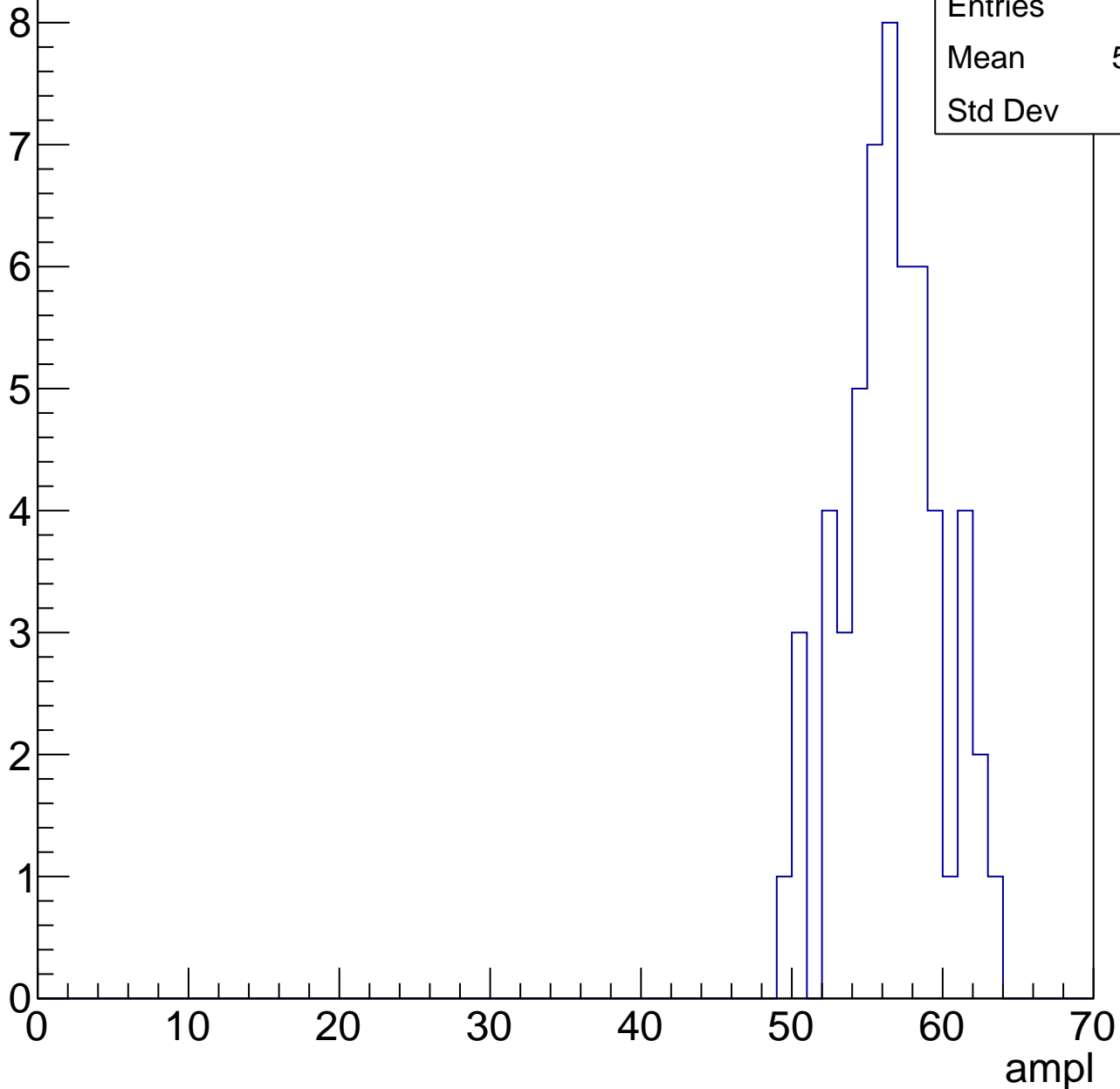


# B1L100S, U2-ch69, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	55
Mean	56.11
Std Dev	3.24



# B1L100S, U2-ch69, adc5

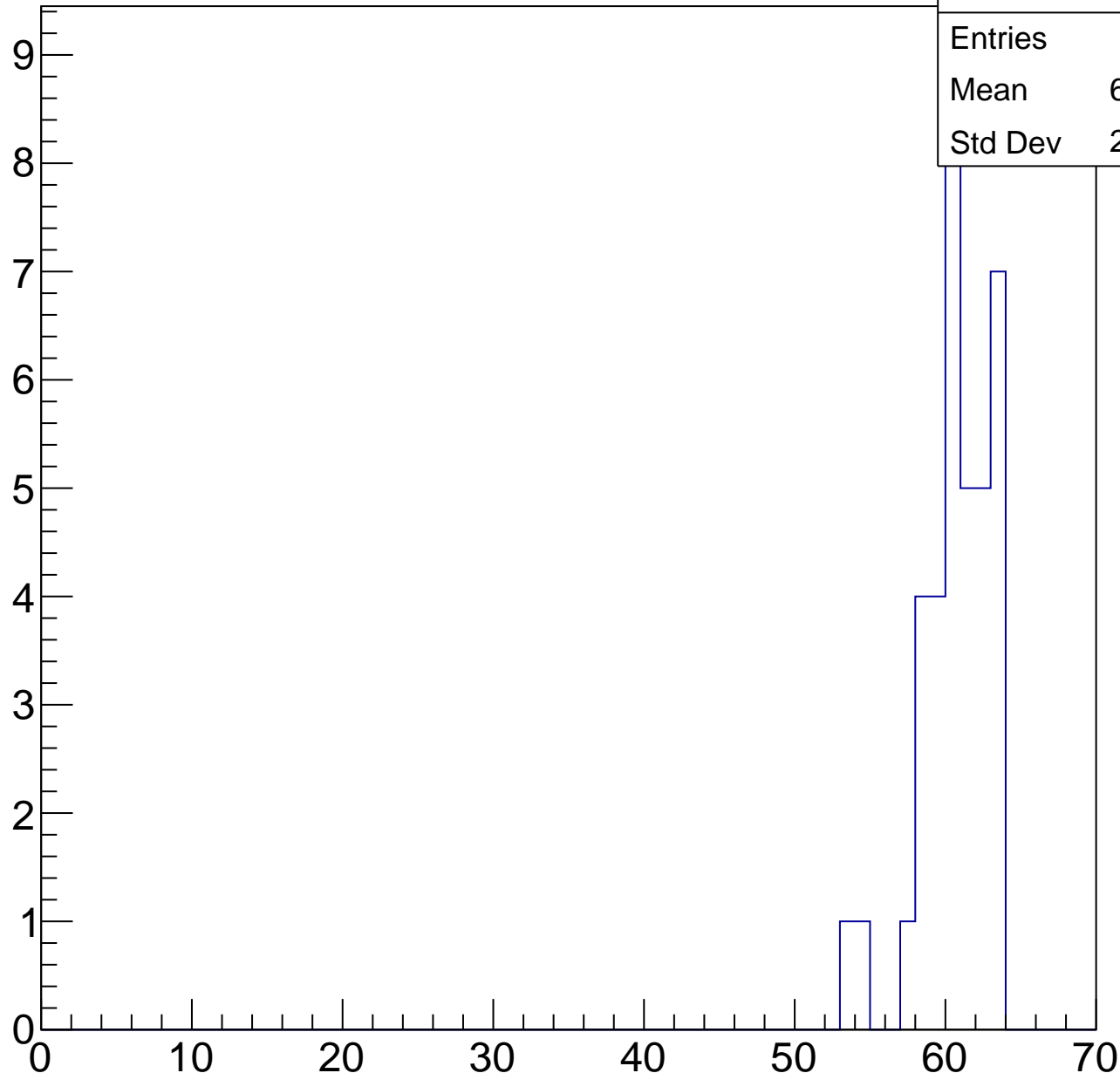
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	37
Mean	60.22
Std Dev	2.327

ampl



# B1L100S, U2-ch69, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

3

2.5

2

1.5

1

0.5

0

0

10

20

30

40

50

60

70

ampl

Entries

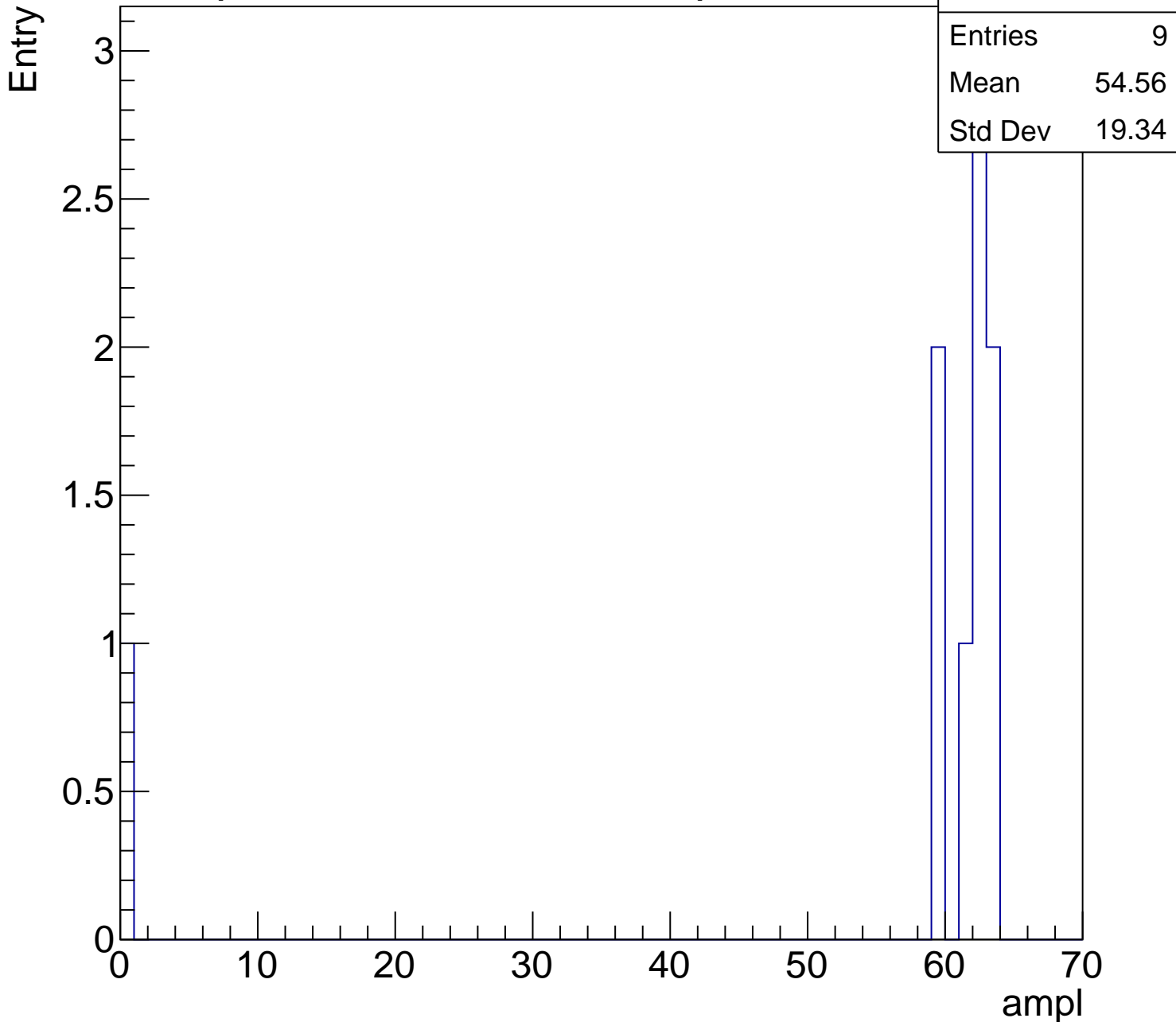
9

Mean

54.56

Std Dev

19.34





# B1L100S, U2-ch69, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



# B1L100S, U2-ch70, adc0

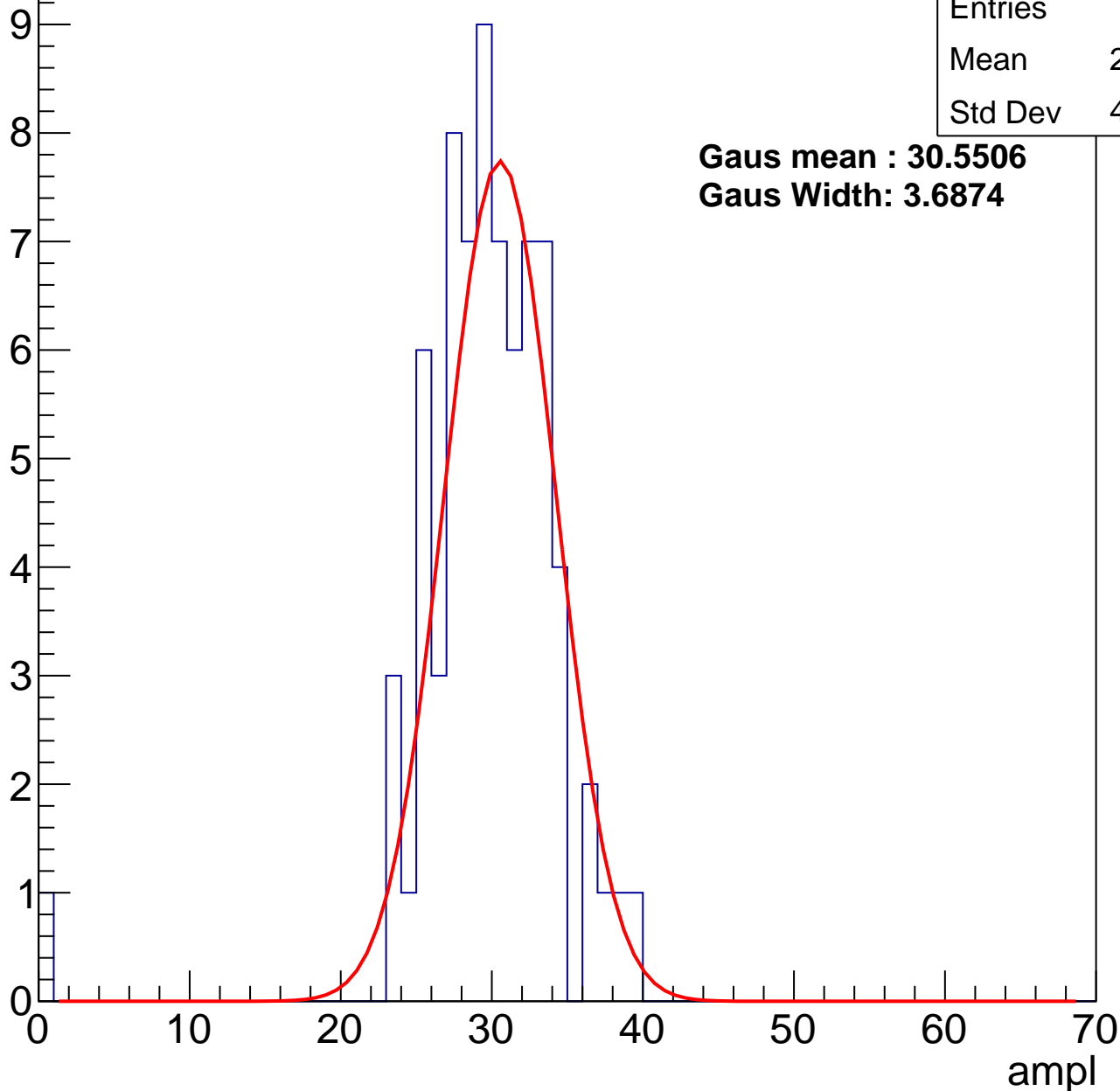
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	74
Mean	29.28
Std Dev	4.903

**Gaus mean : 30.5506**

**Gaus Width: 3.6874**



# B1L100S, U2-ch70, adc1

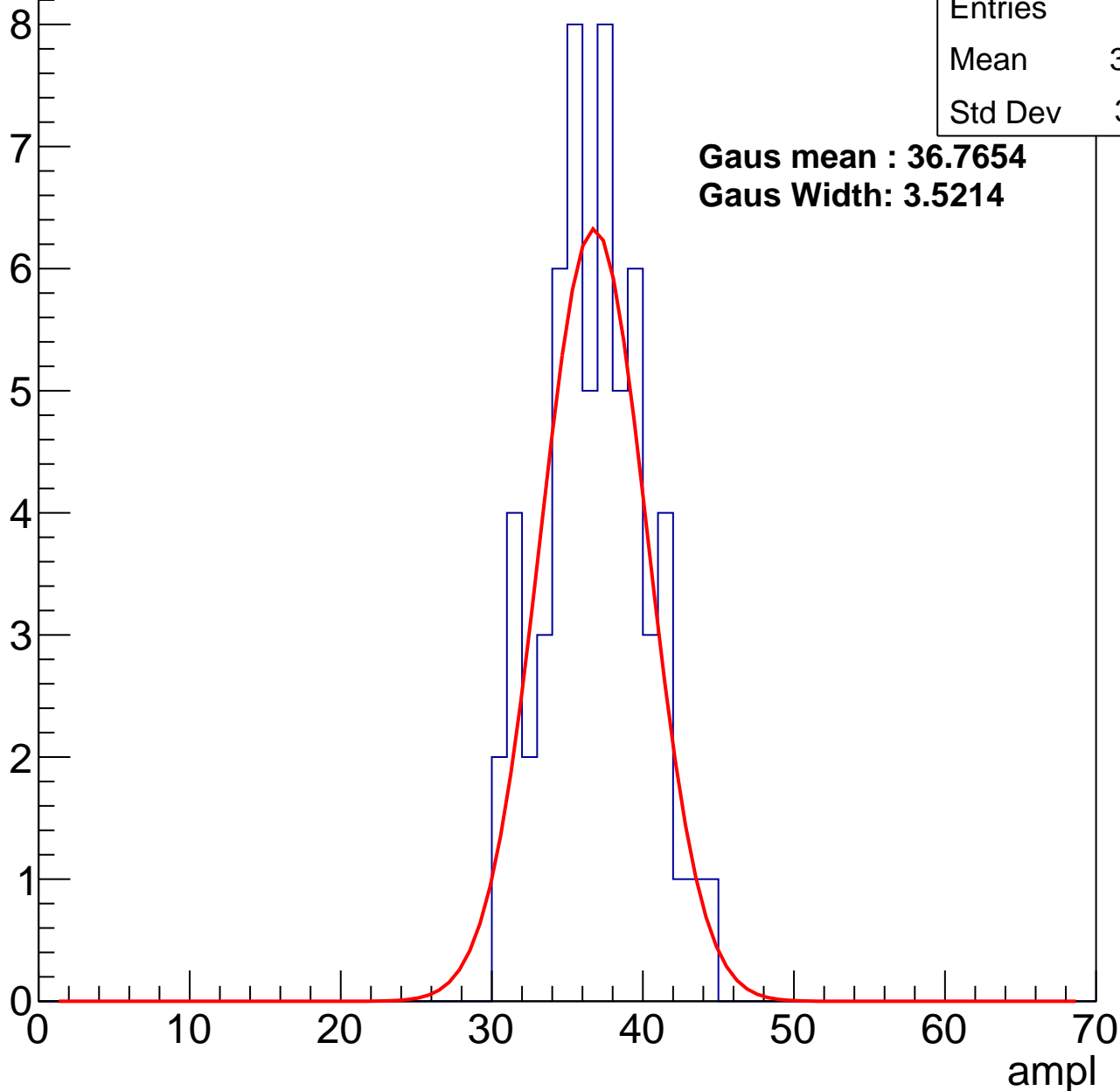
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	59
Mean	36.34
Std Dev	3.281

**Gaus mean : 36.7654**

**Gaus Width: 3.5214**



# B1L100S, U2-ch70, adc2

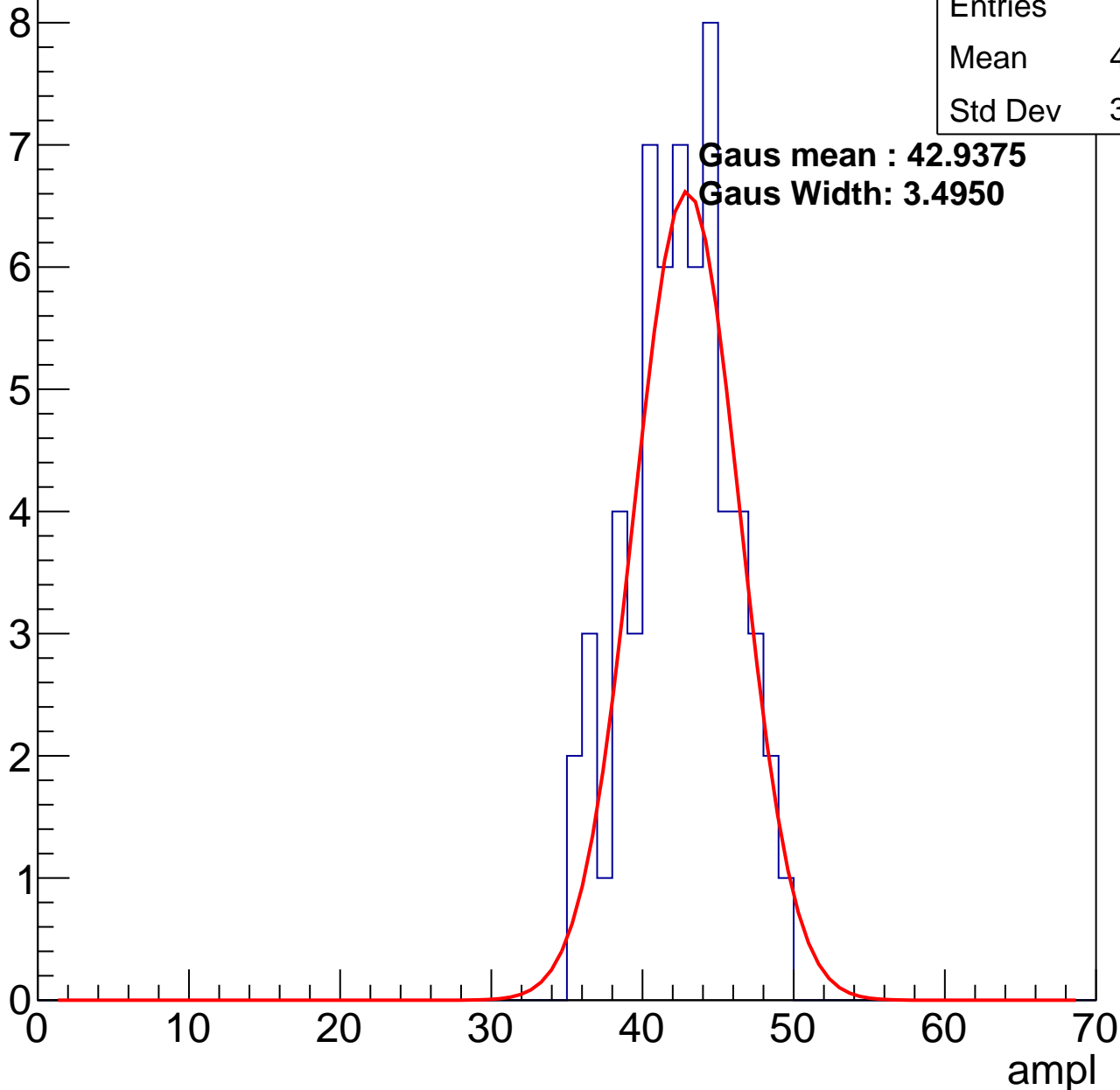
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	61
Mean	42.03
Std Dev	3.363

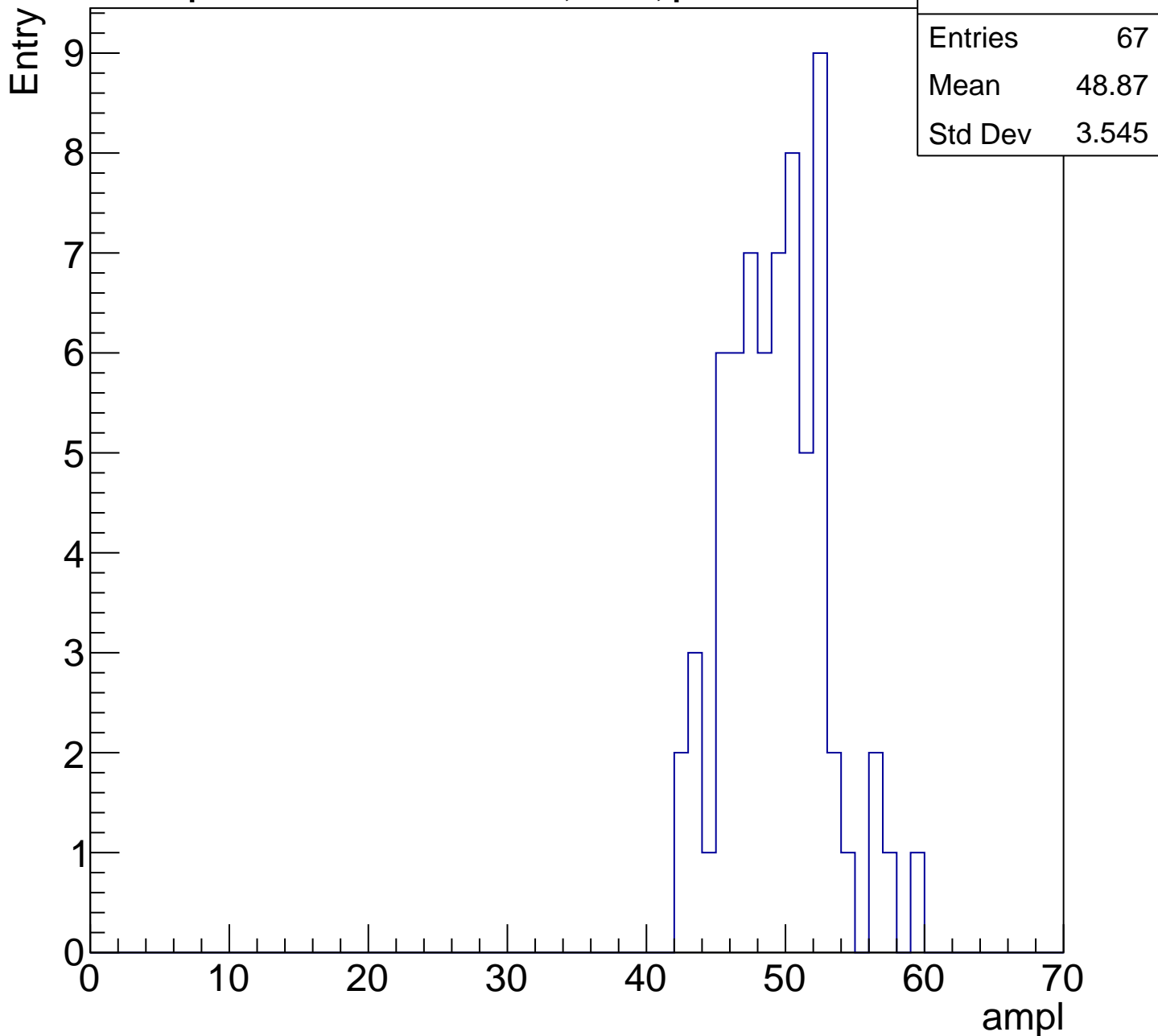
**Gaus mean : 42.9375**

**Gaus Width: 3.4950**



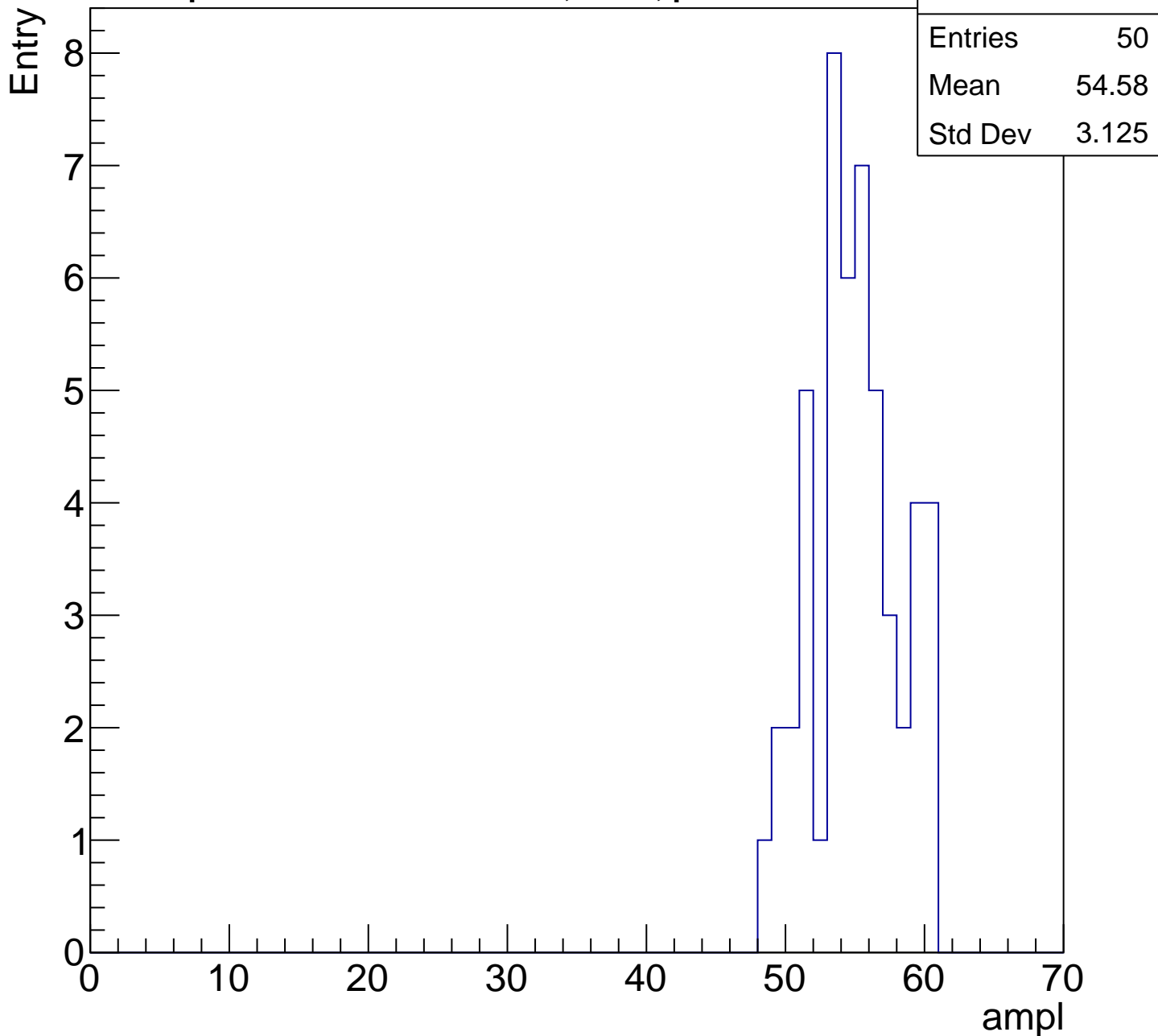
# B1L100S, U2-ch70, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2



# B1L100S, U2-ch70, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

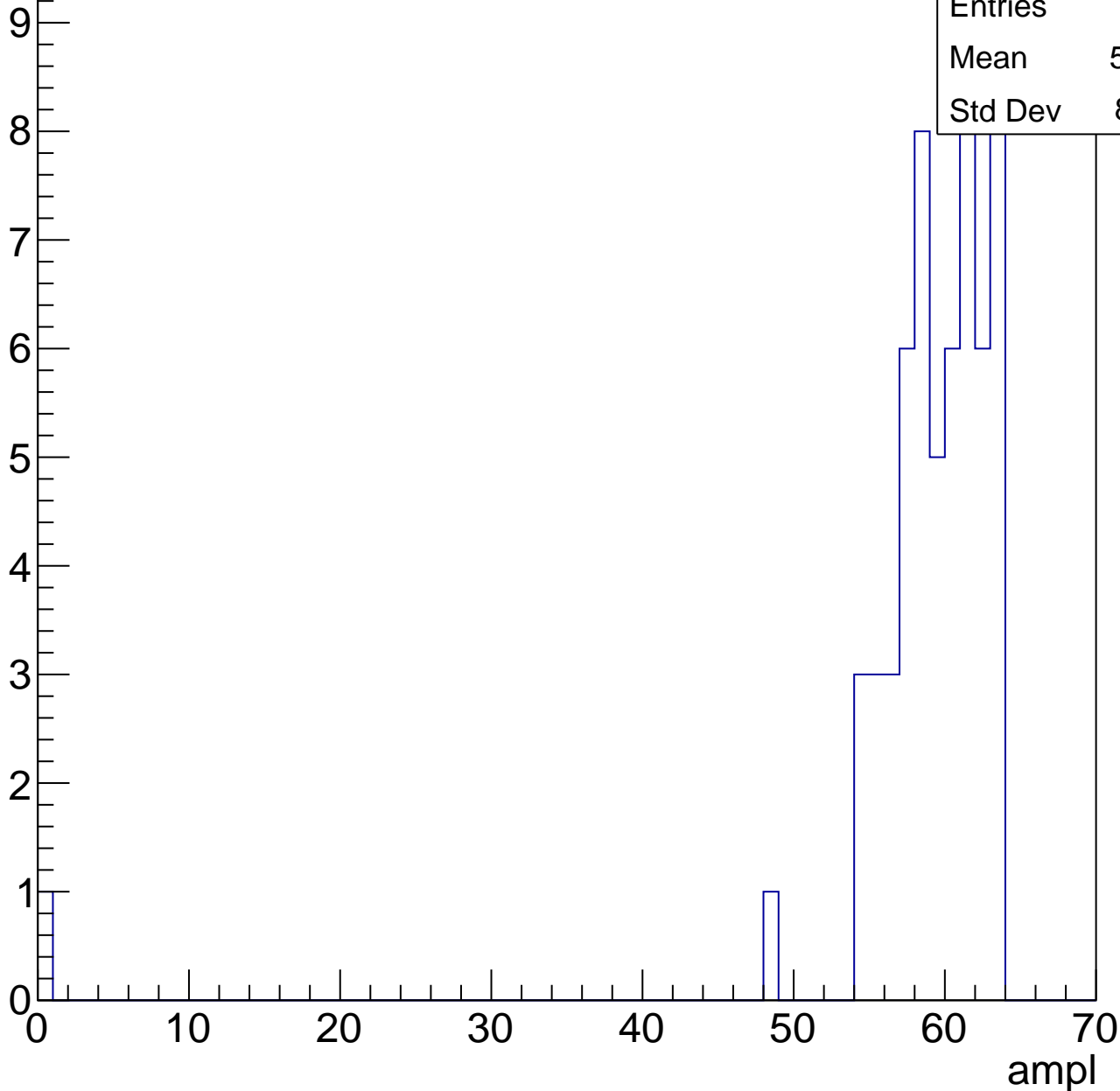


# B1L100S, U2-ch70, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

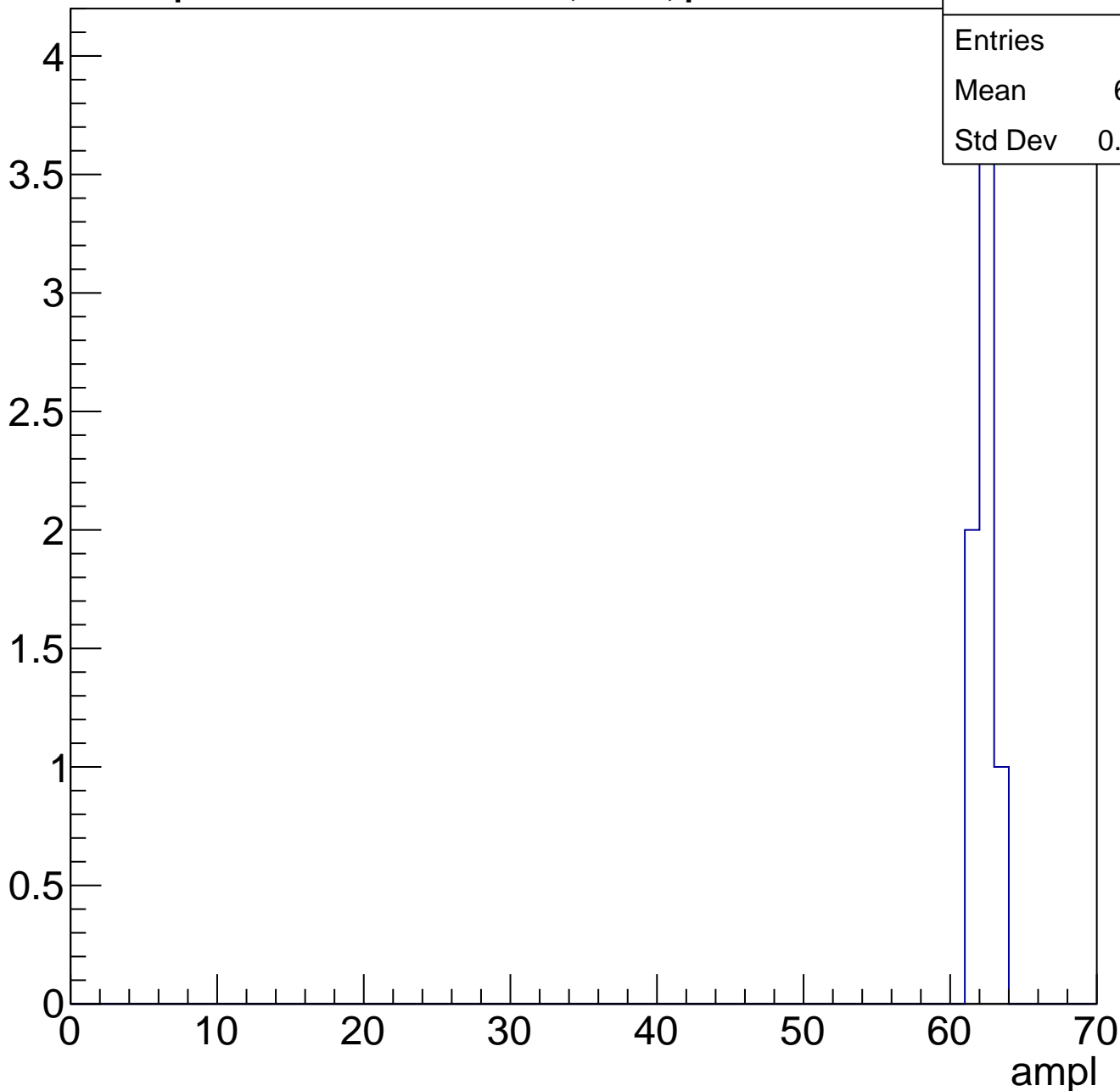
Entries	59
Mean	58.15
Std Dev	8.211



# B1L100S, U2-ch70, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry





# B1L100S, U2-ch70, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L100S, U2-ch71, adc0

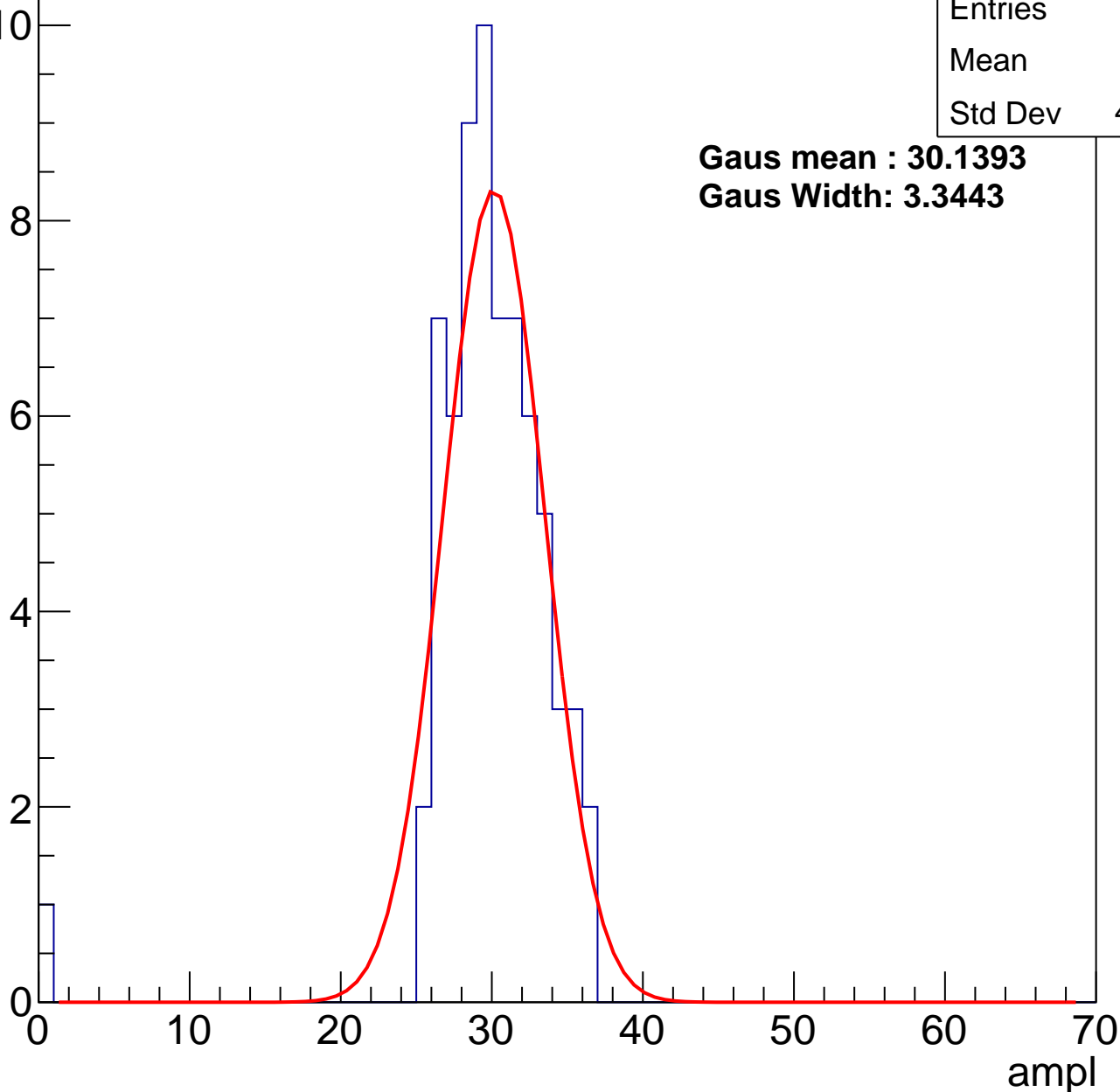
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	68
Mean	29.4
Std Dev	4.551

**Gaus mean : 30.1393**

**Gaus Width: 3.3443**



# B1L100S, U2-ch71, adc1

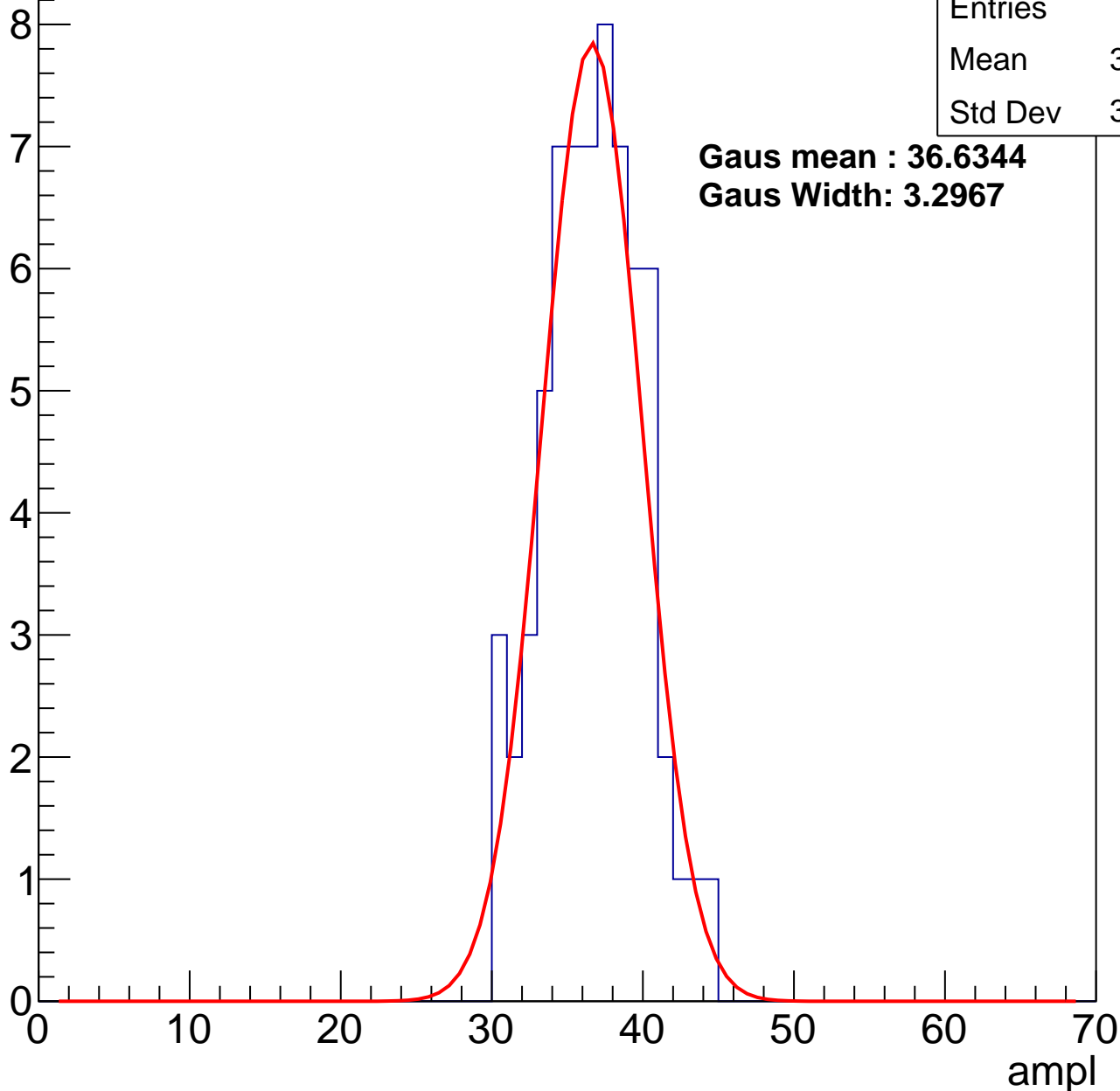
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	66
Mean	36.29
Std Dev	3.175

**Gaus mean : 36.6344**

**Gaus Width: 3.2967**



# B1L100S, U2-ch71, adc2

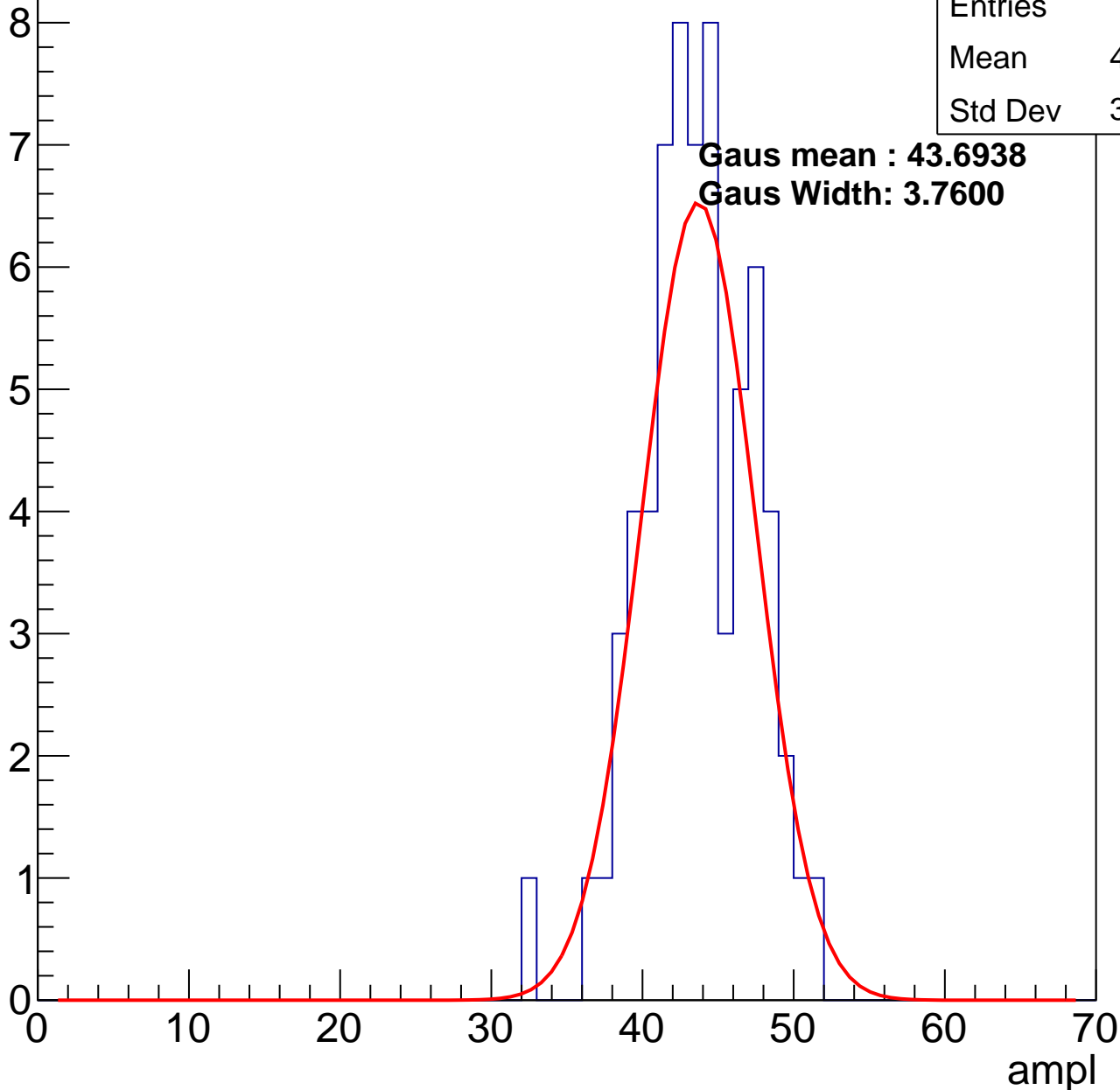
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	66
Mean	43.17
Std Dev	3.612

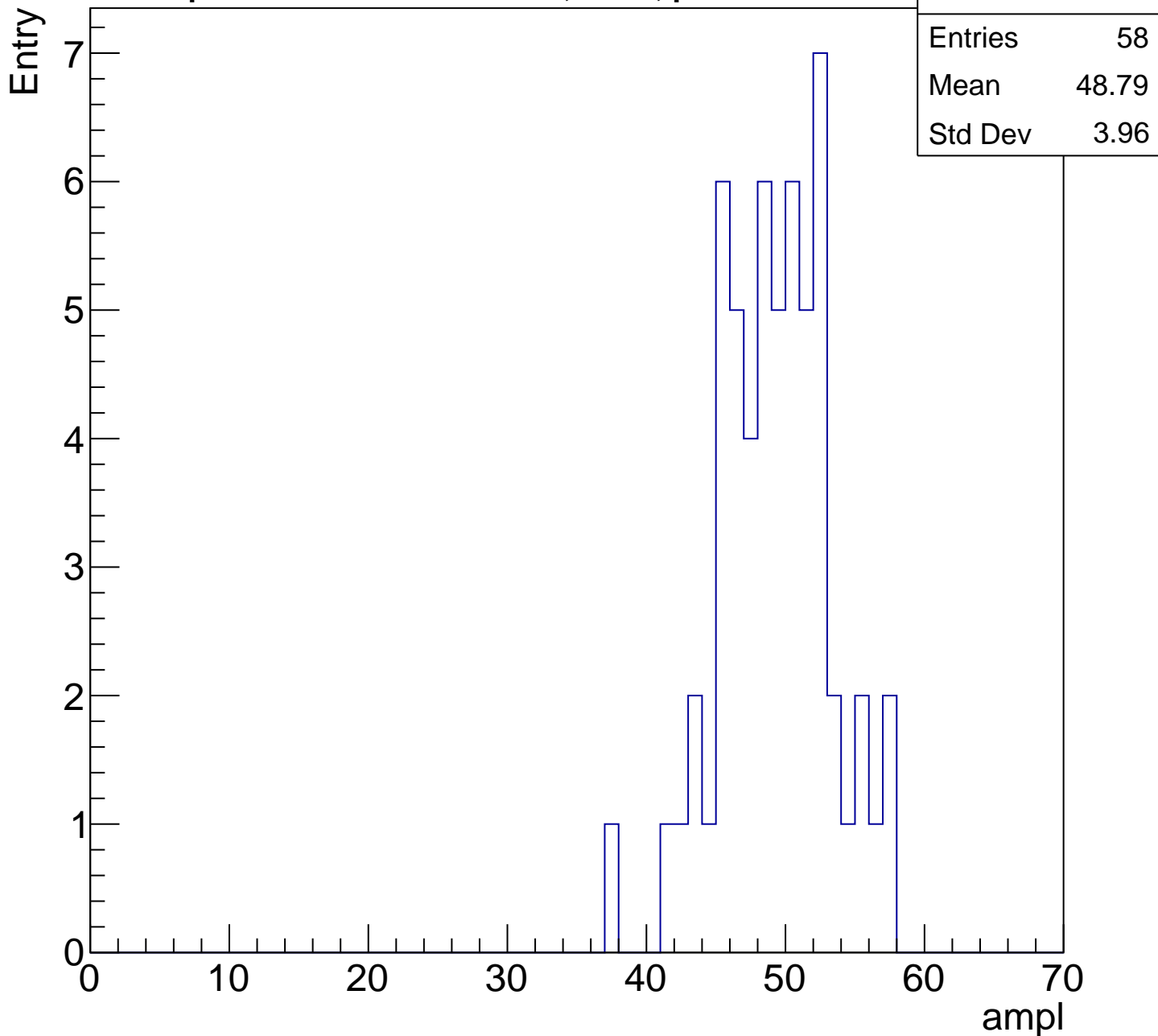
**Gaus mean : 43.6938**

**Gaus Width: 3.7600**



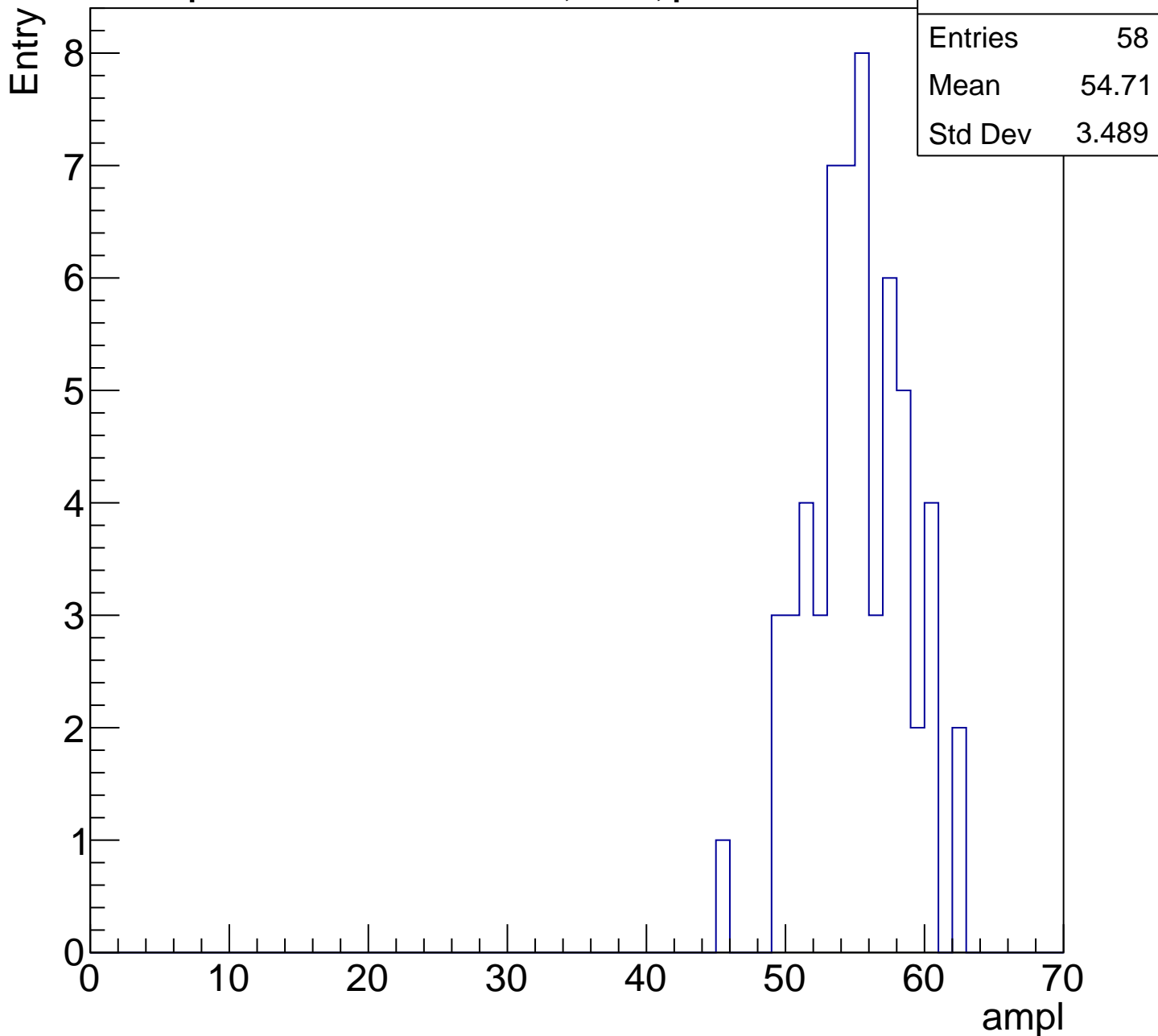
# B1L100S, U2-ch71, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2



# B1L100S, U2-ch71, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2



# B1L100S, U2-ch71, adc5

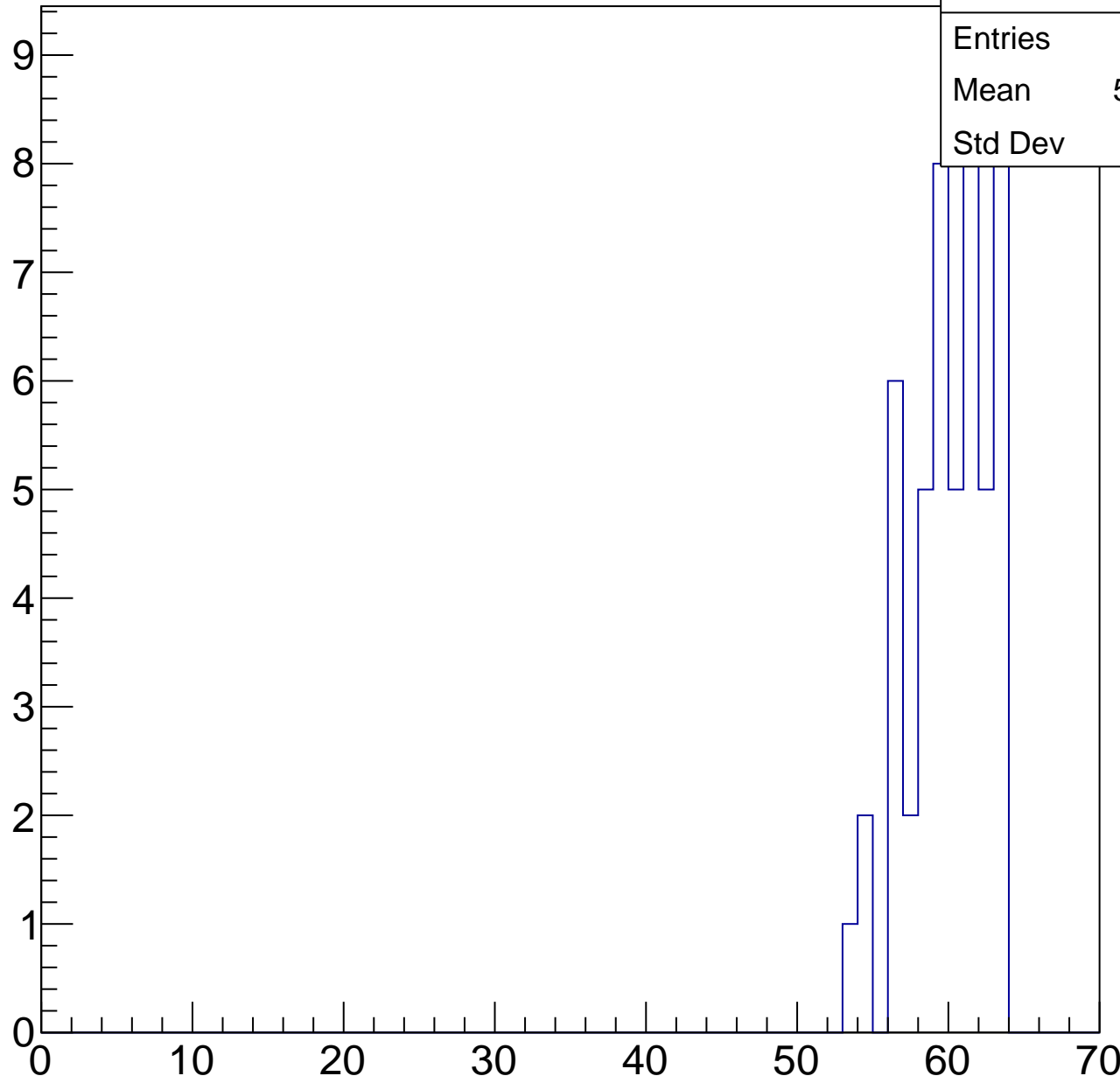
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	51
Mean	59.53
Std Dev	2.63

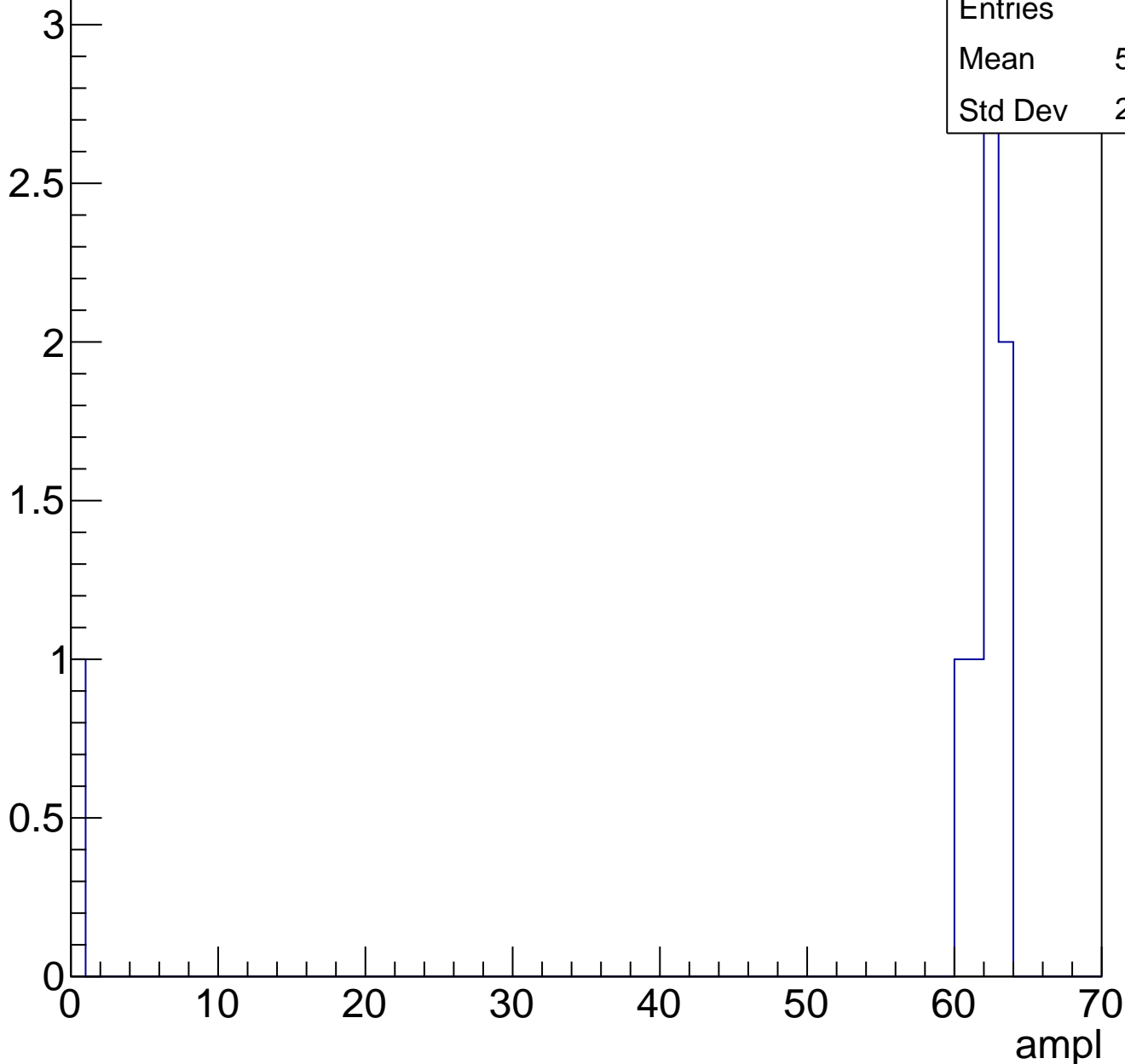
ampl



# B1L100S, U2-ch71, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry





# B1L100S, U2-ch71, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L100S, U2-ch72, adc0

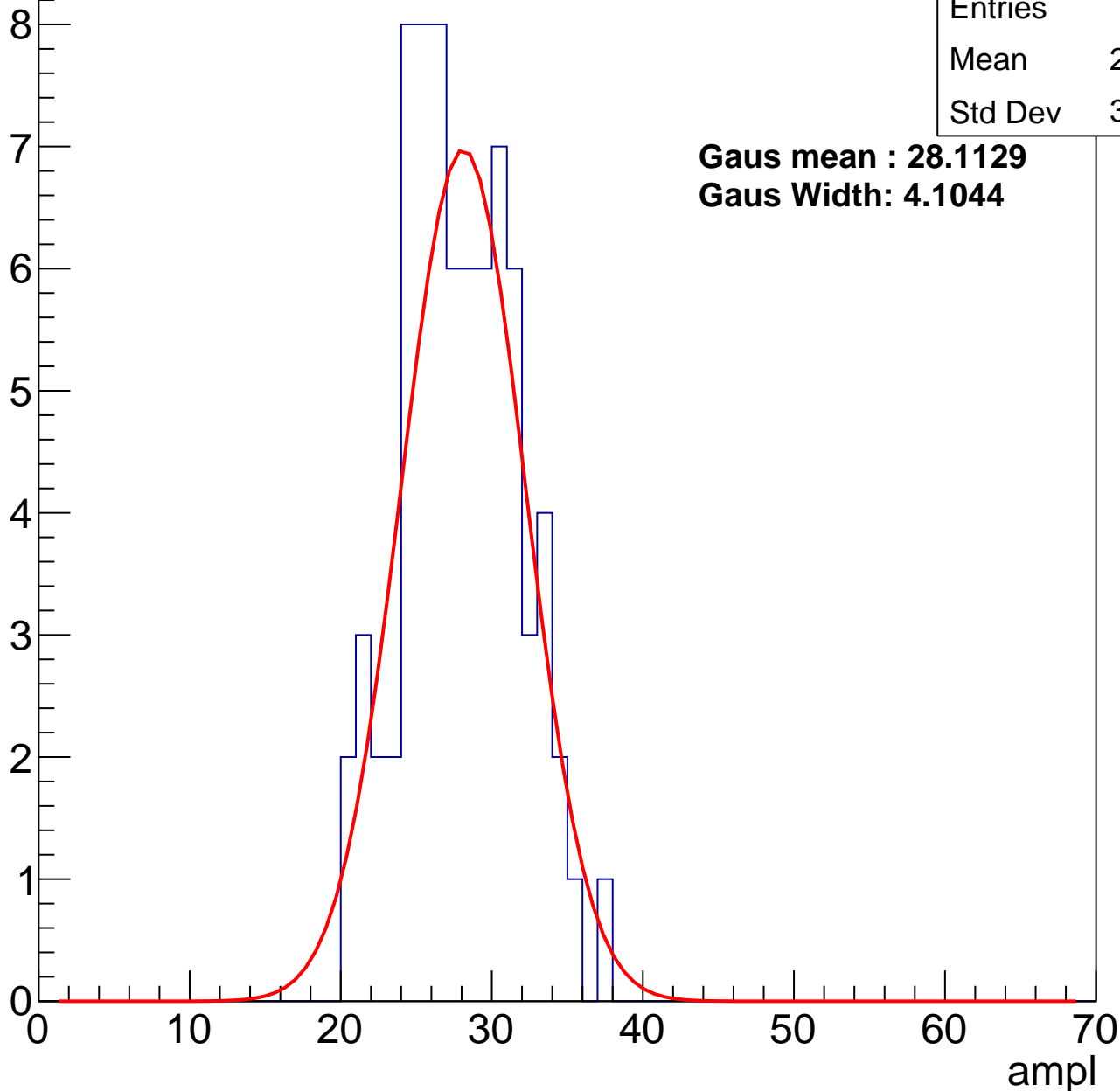
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	75
Mean	27.48
Std Dev	3.747

**Gaus mean : 28.1129**

**Gaus Width: 4.1044**



# B1L100S, U2-ch72, adc1

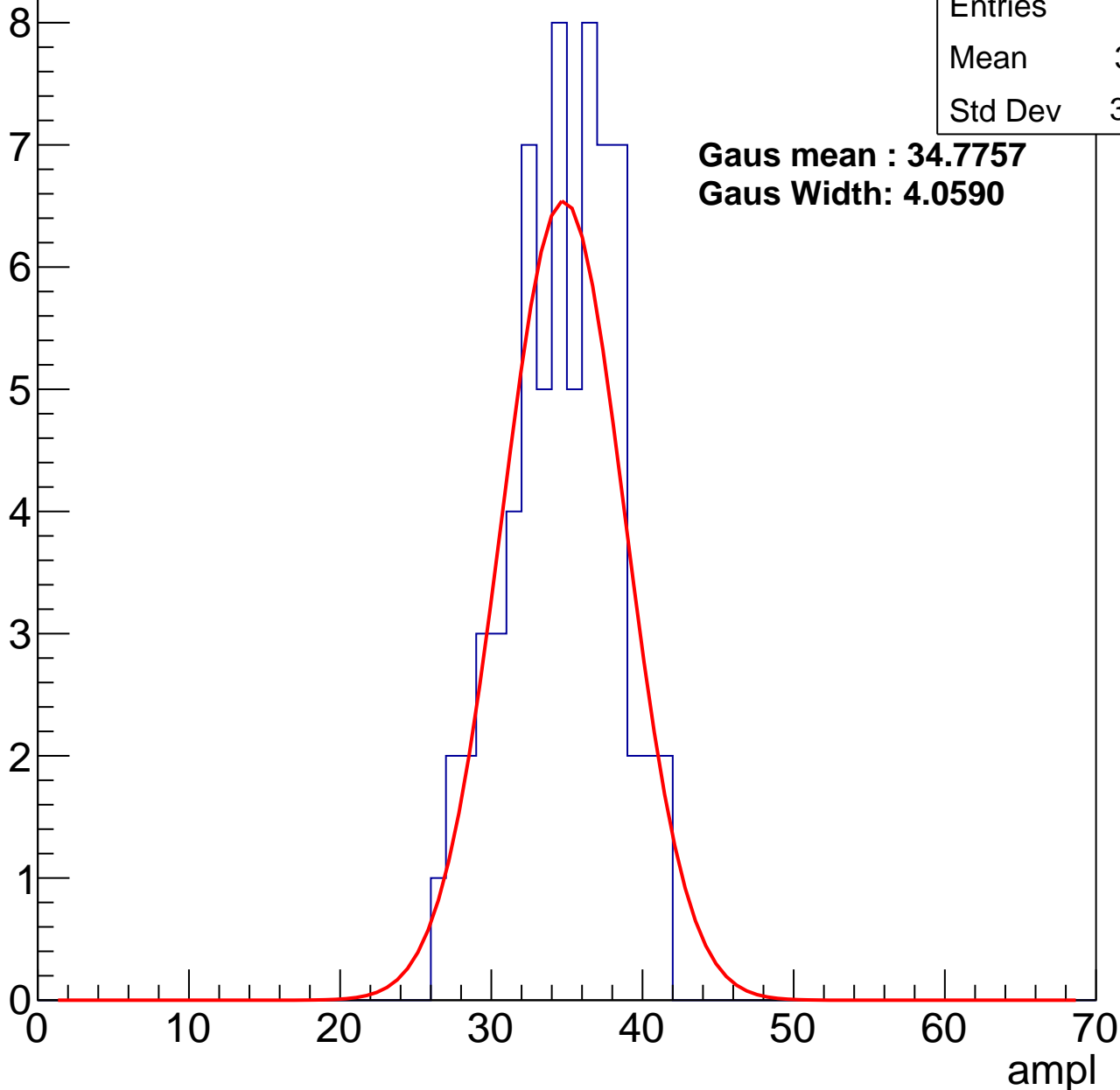
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	68
Mean	34.21
Std Dev	3.546

**Gaus mean : 34.7757**

**Gaus Width: 4.0590**



# B1L100S, U2-ch72, adc2

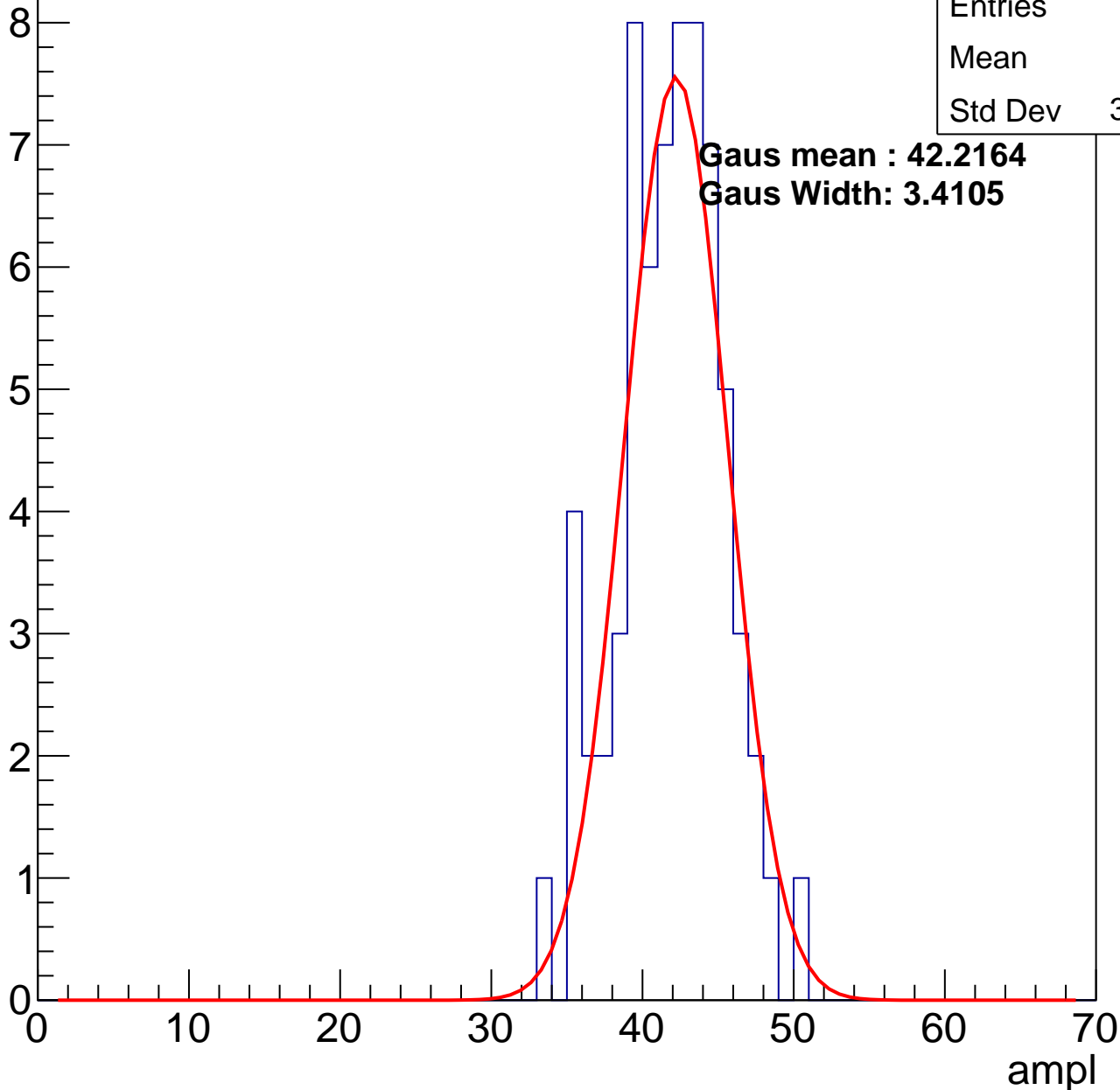
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	68
Mean	41.4
Std Dev	3.439

**Gaus mean : 42.2164**

**Gaus Width: 3.4105**

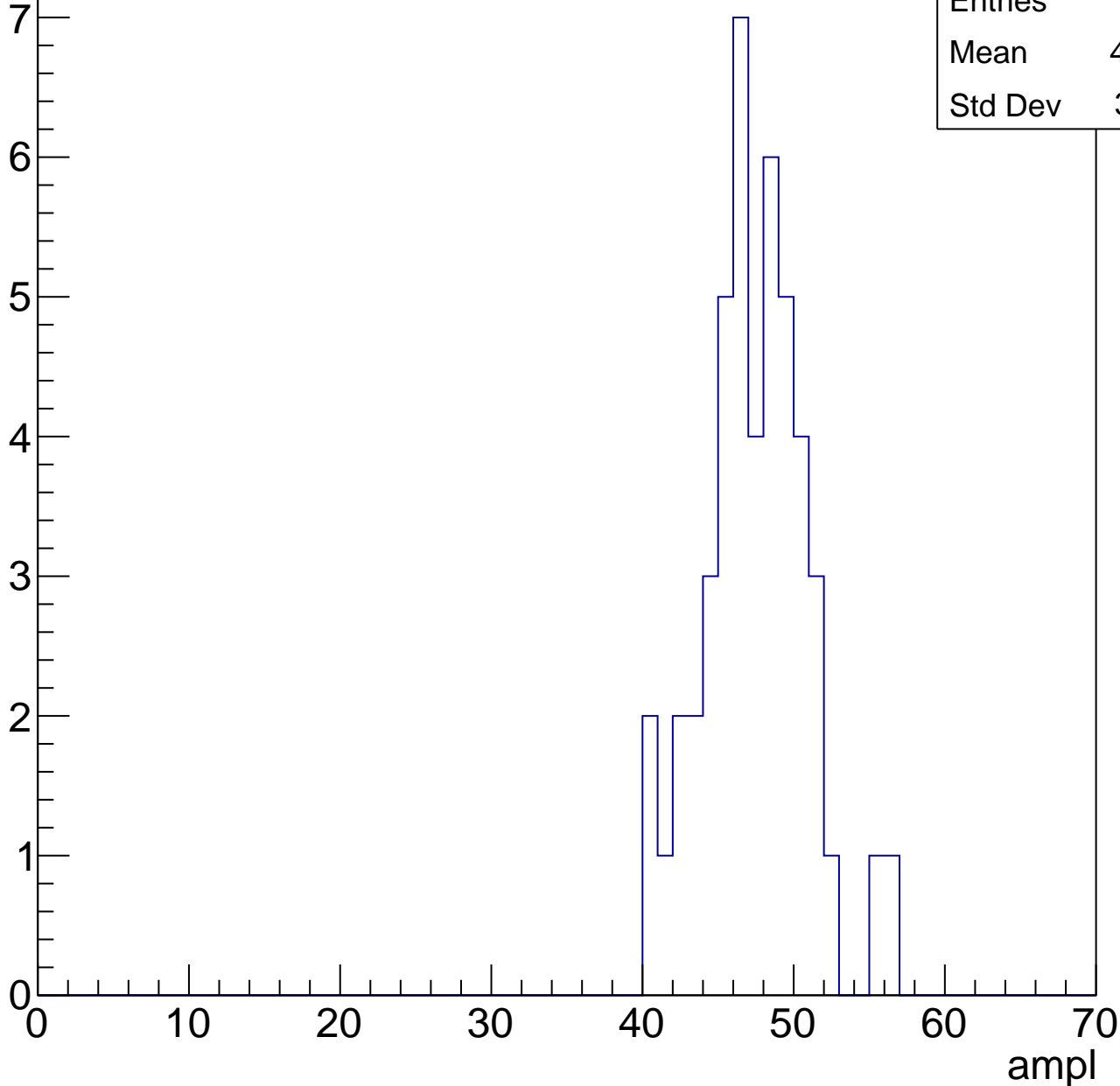


# B1L100S, U2-ch72, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	47
Mean	46.96
Std Dev	3.421

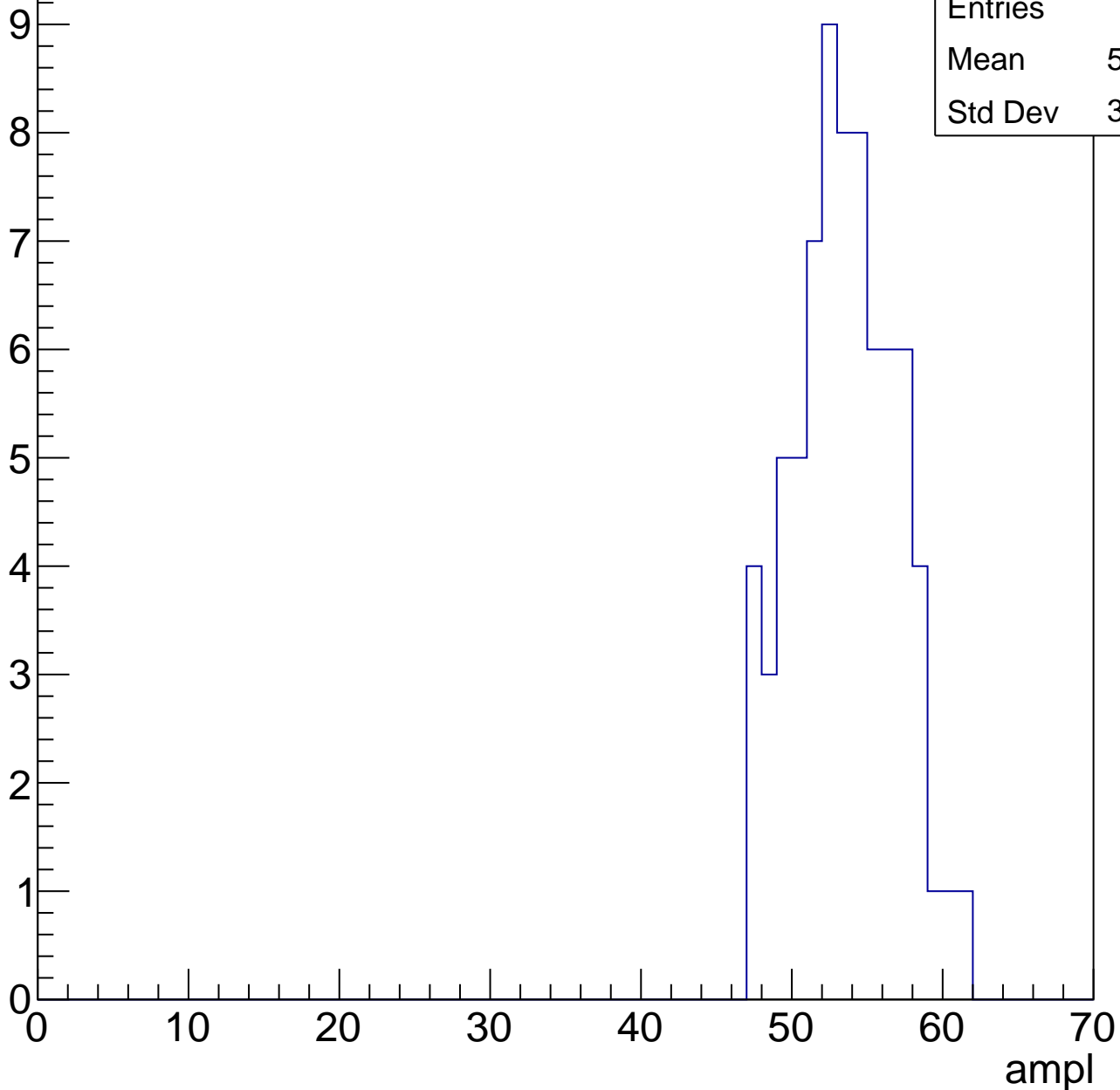


# B1L100S, U2-ch72, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

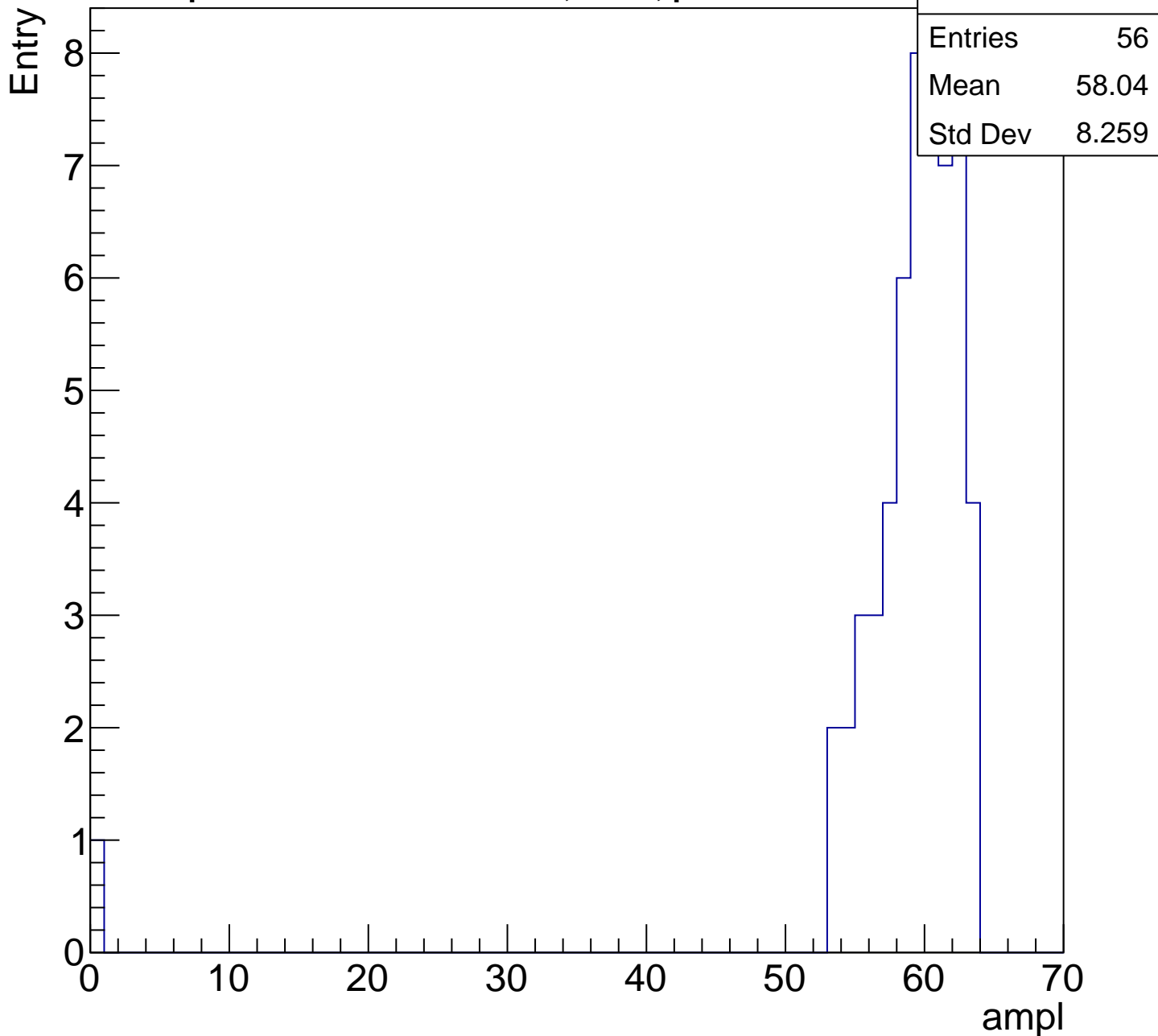
Entry

Entries	74
Mean	53.08
Std Dev	3.312



# B1L100S, U2-ch72, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

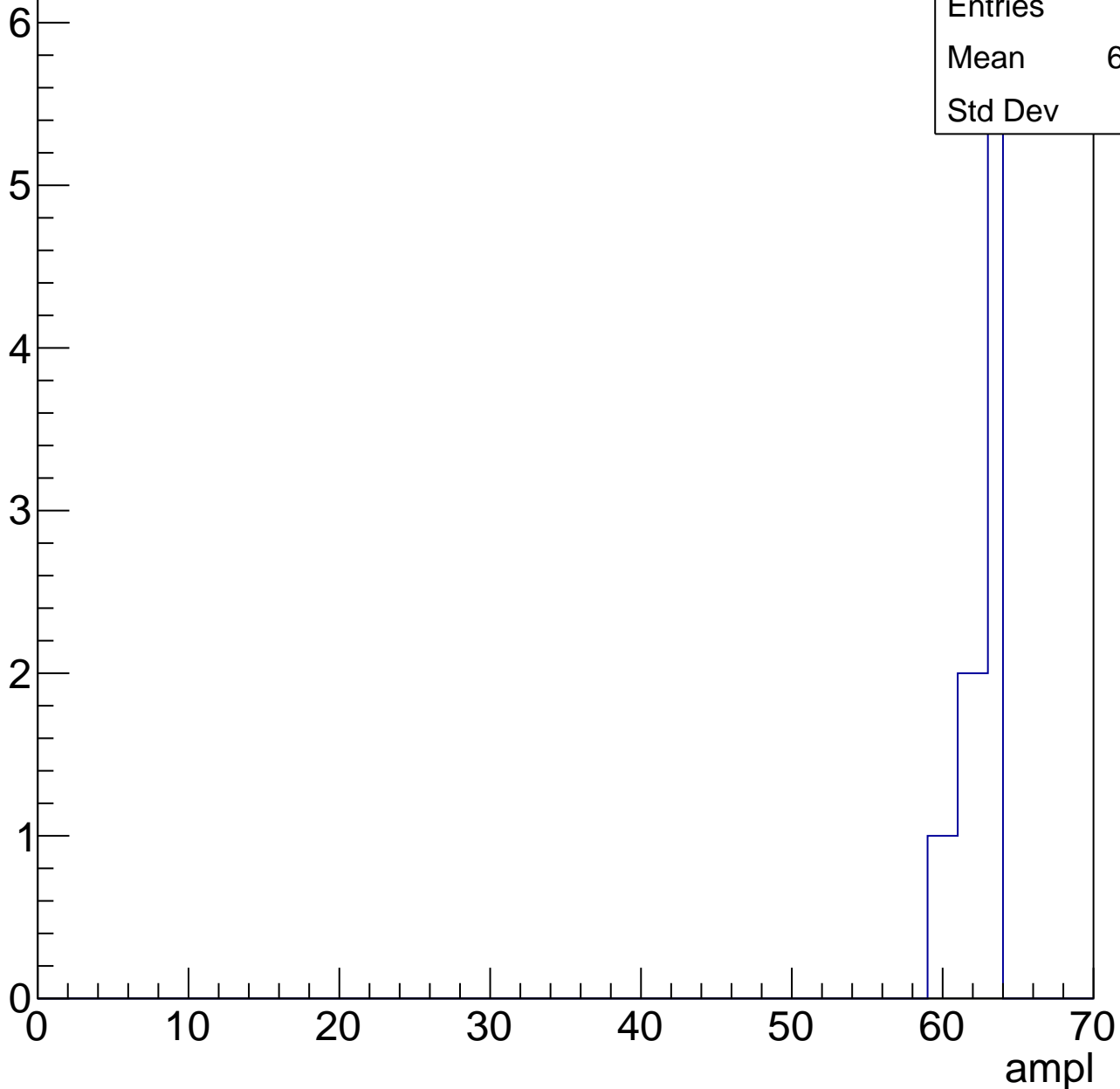


# B1L100S, U2-ch72, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	12
Mean	61.92
Std Dev	1.32





# B1L100S, U2-ch72, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L100S, U2-ch73, adc0

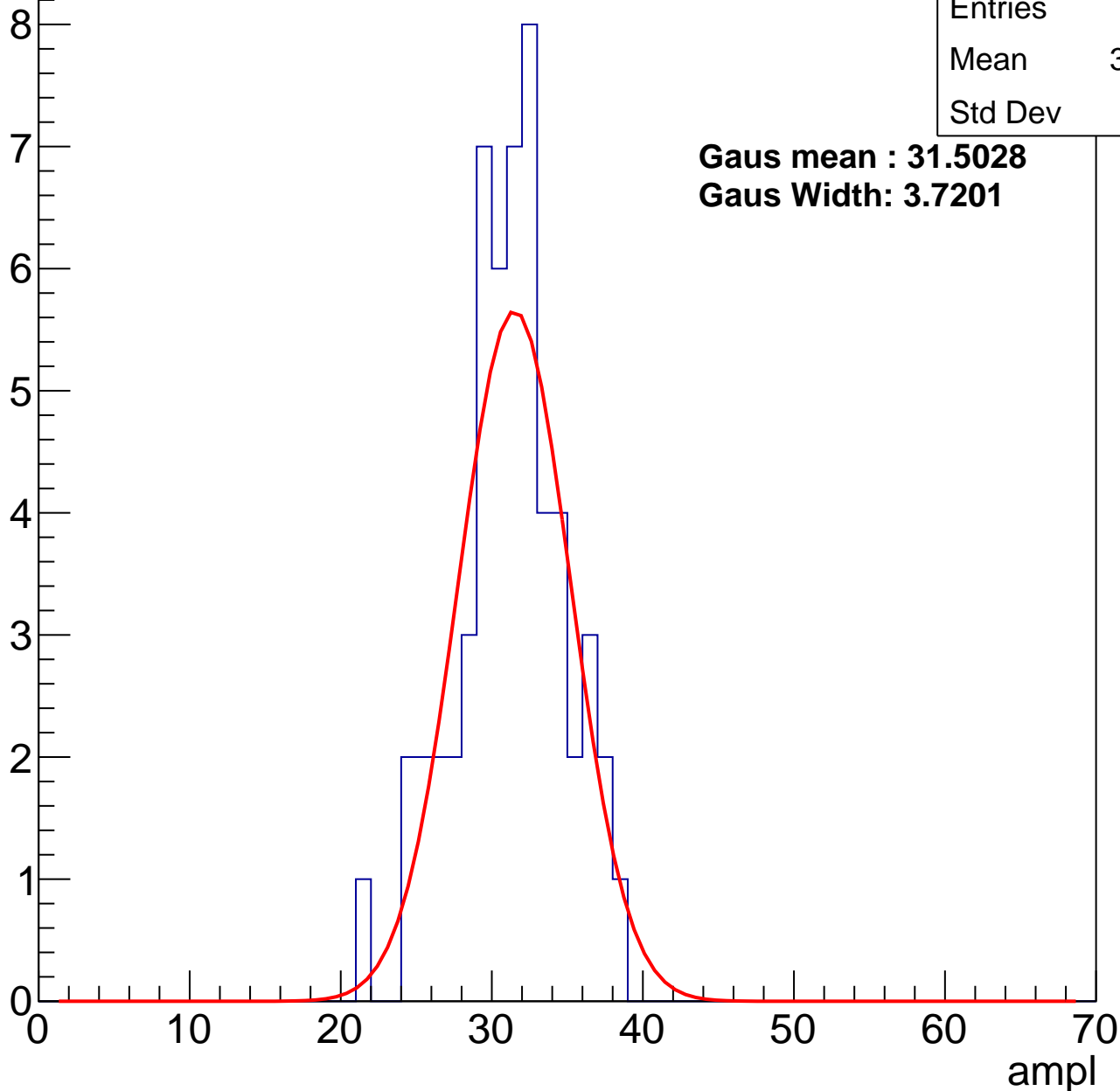
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	56
Mean	30.77
Std Dev	3.53

**Gaus mean : 31.5028**

**Gaus Width: 3.7201**



# B1L100S, U2-ch73, adc1

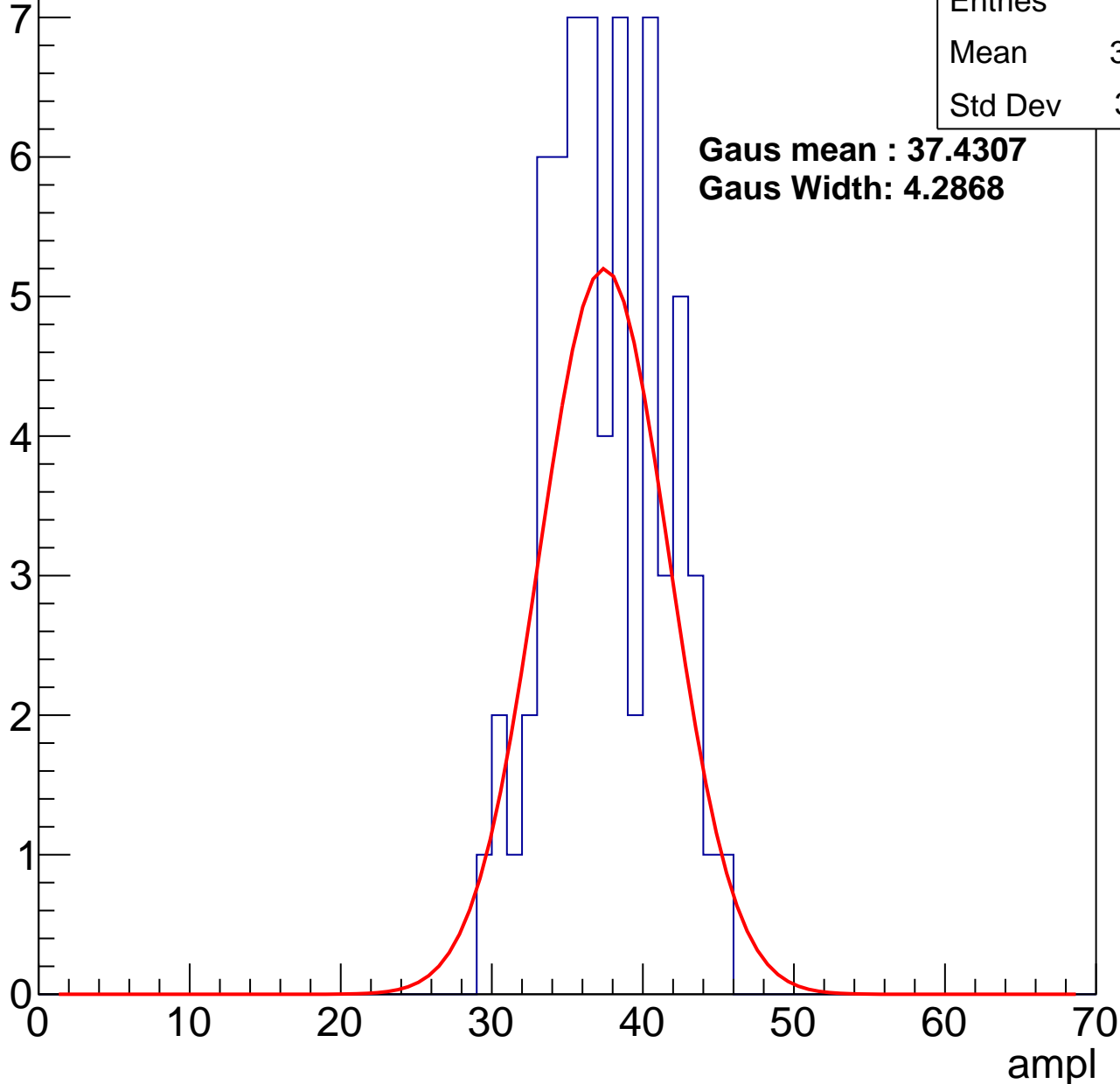
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	65
Mean	37.02
Std Dev	3.731

**Gaus mean : 37.4307**

**Gaus Width: 4.2868**



# B1L100S, U2-ch73, adc2

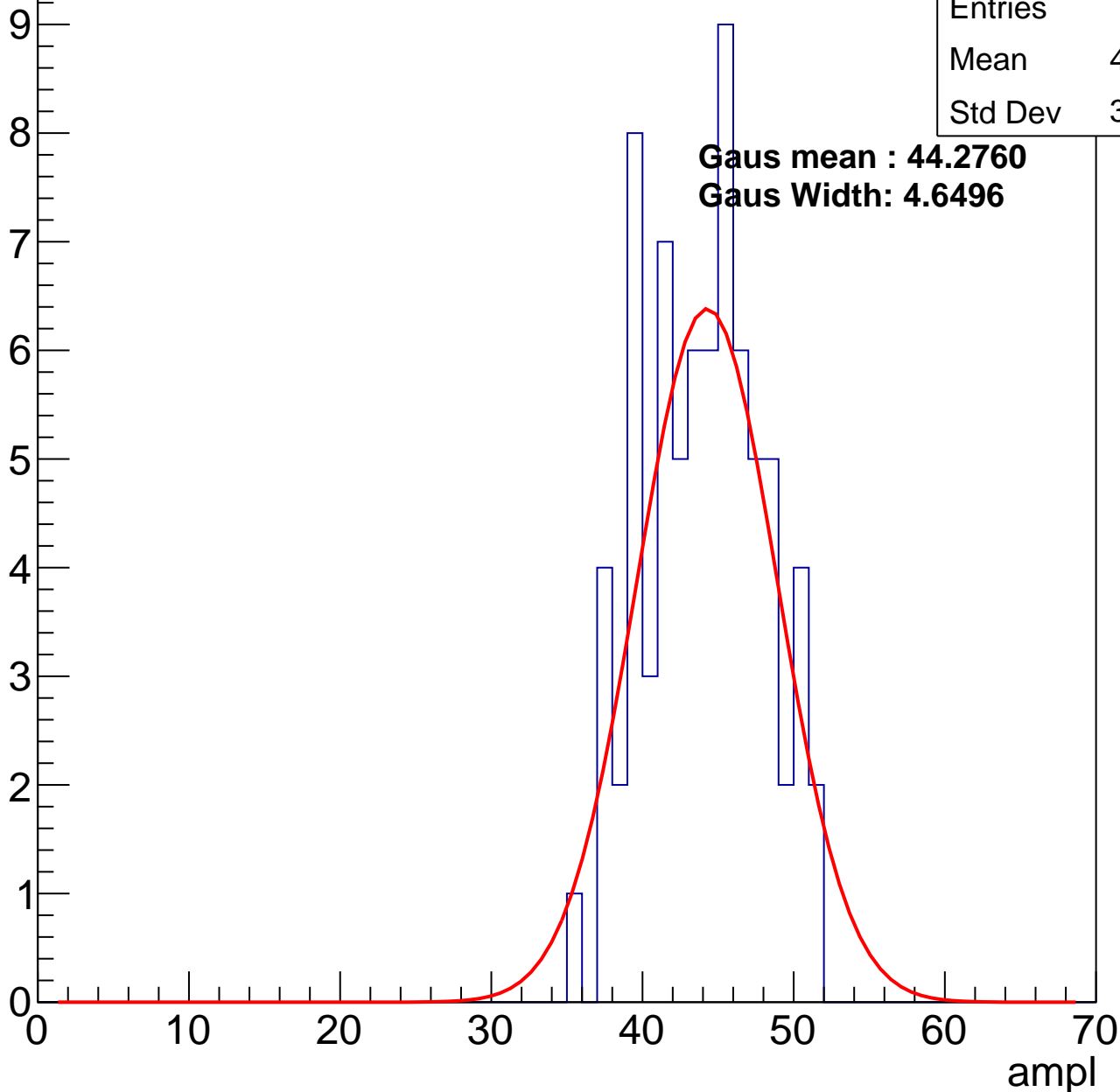
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	75
Mean	43.55
Std Dev	3.865

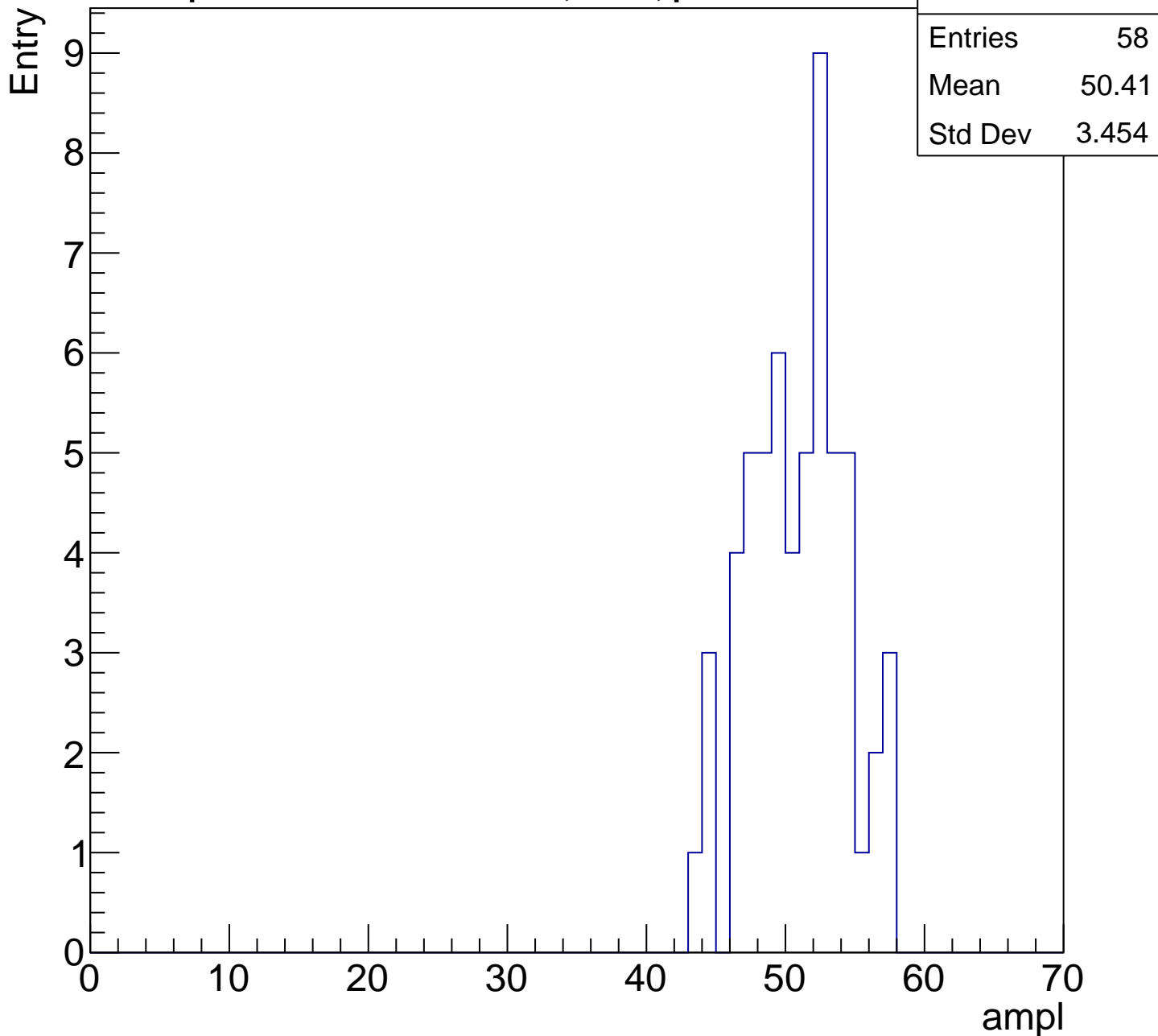
**Gaus mean : 44.2760**

**Gaus Width: 4.6496**



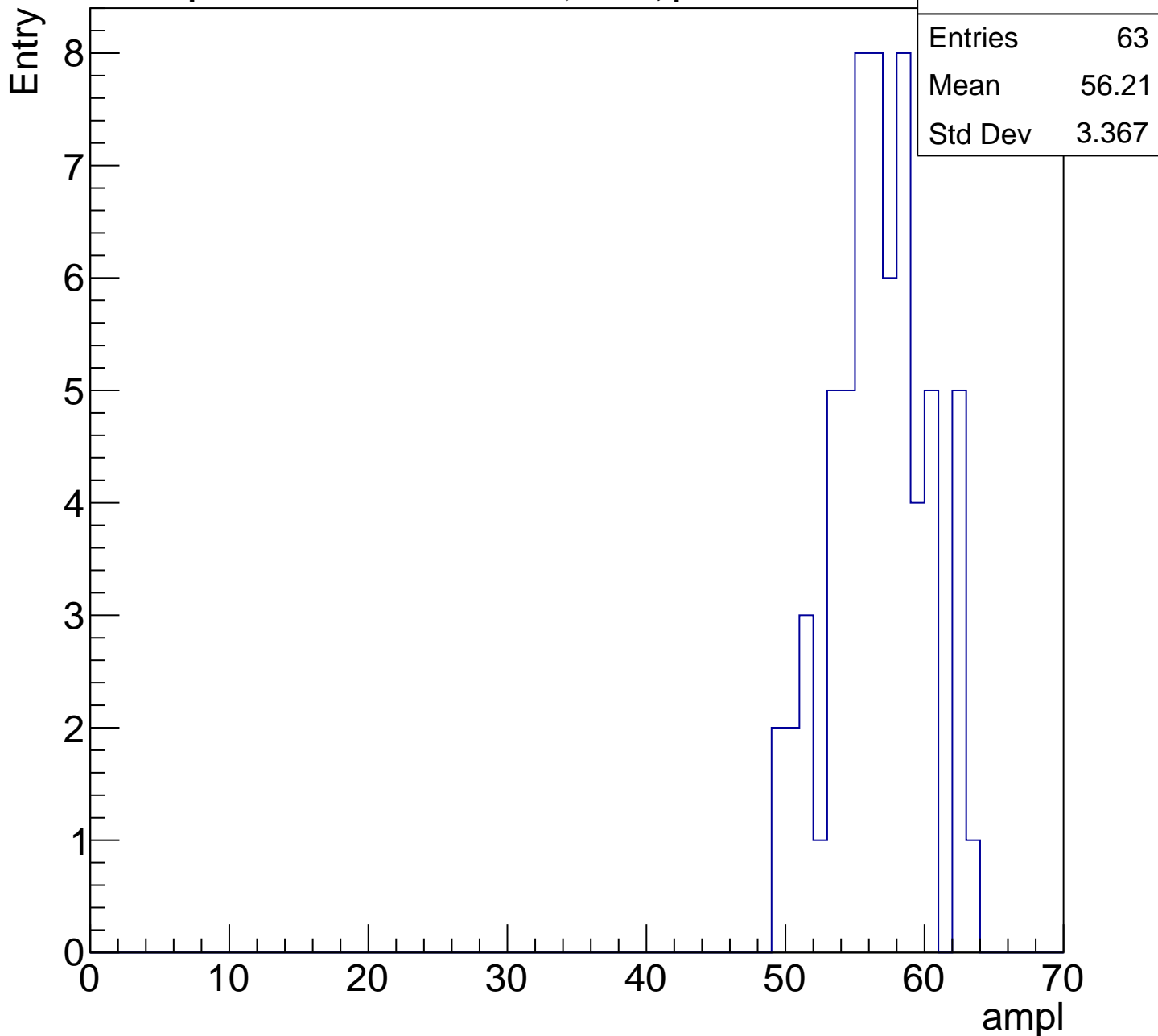
# B1L100S, U2-ch73, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2



# B1L100S, U2-ch73, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

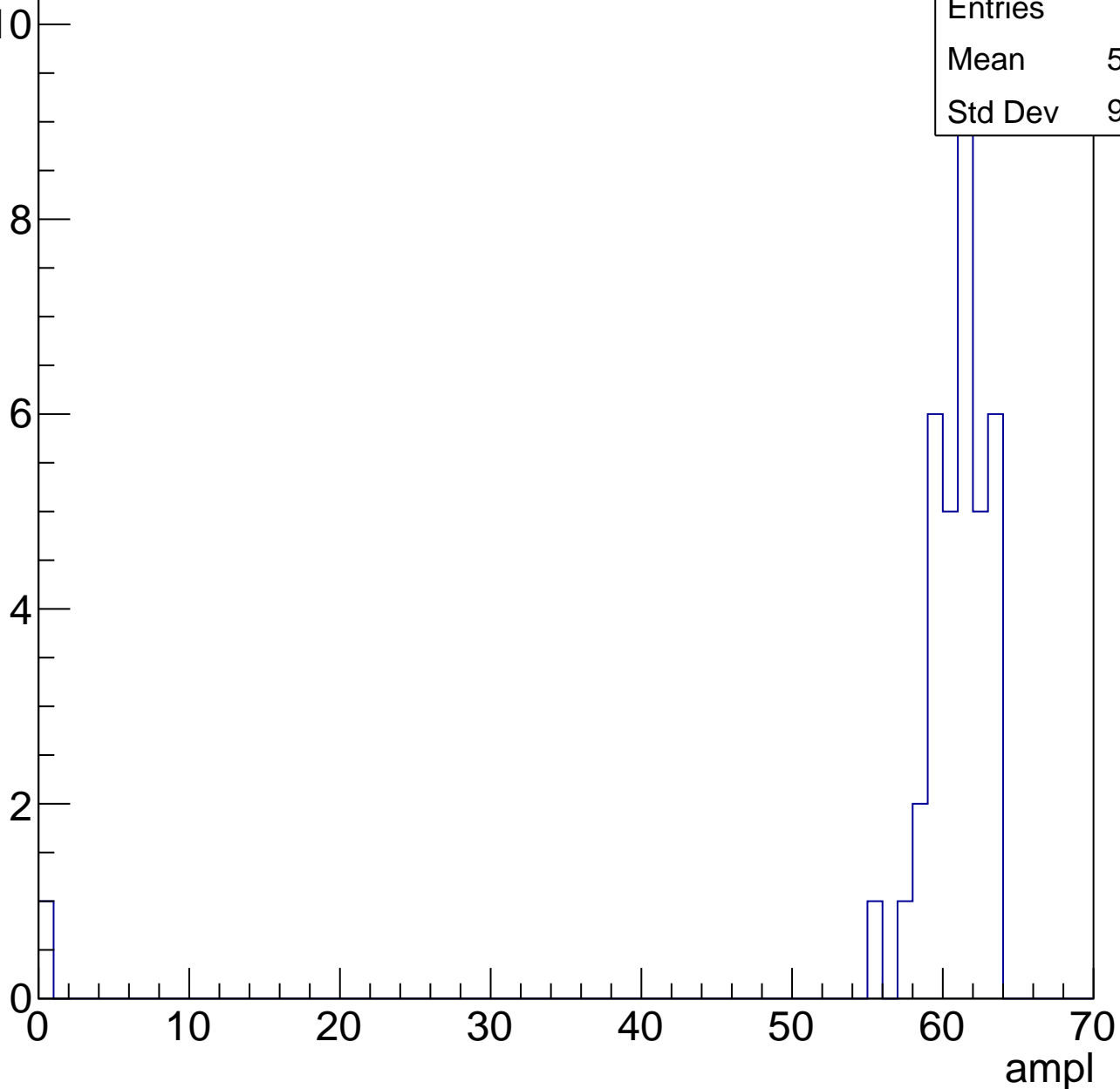


# B1L100S, U2-ch73, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	37
Mean	58.92
Std Dev	9.985



# B1L100S, U2-ch73, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry





# B1L100S, U2-ch73, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L100S, U2-ch74, adc0

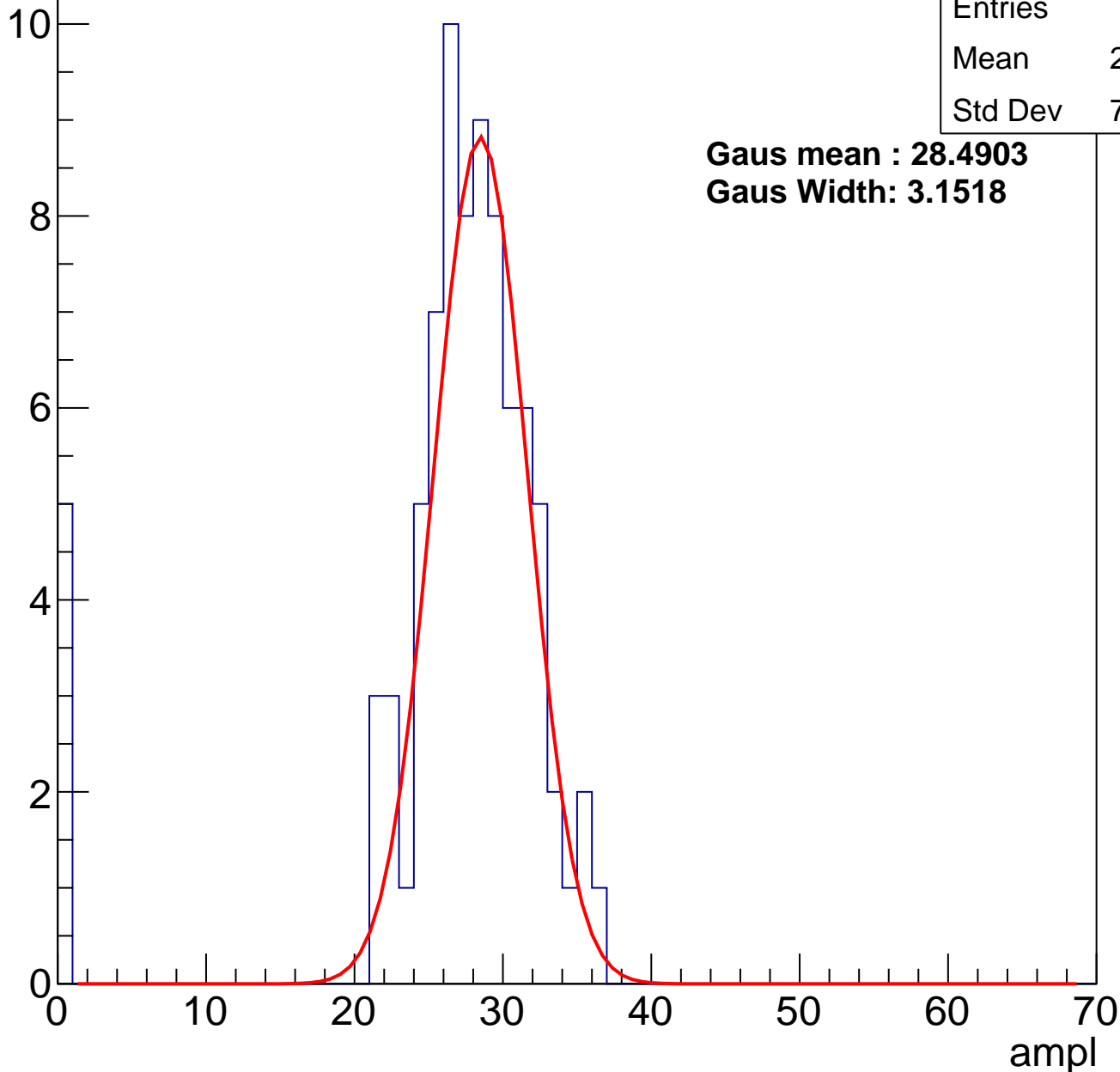
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	82
Mean	26.09
Std Dev	7.412

**Gaus mean : 28.4903**

**Gaus Width: 3.1518**

Entry



# B1L100S, U2-ch74, adc1

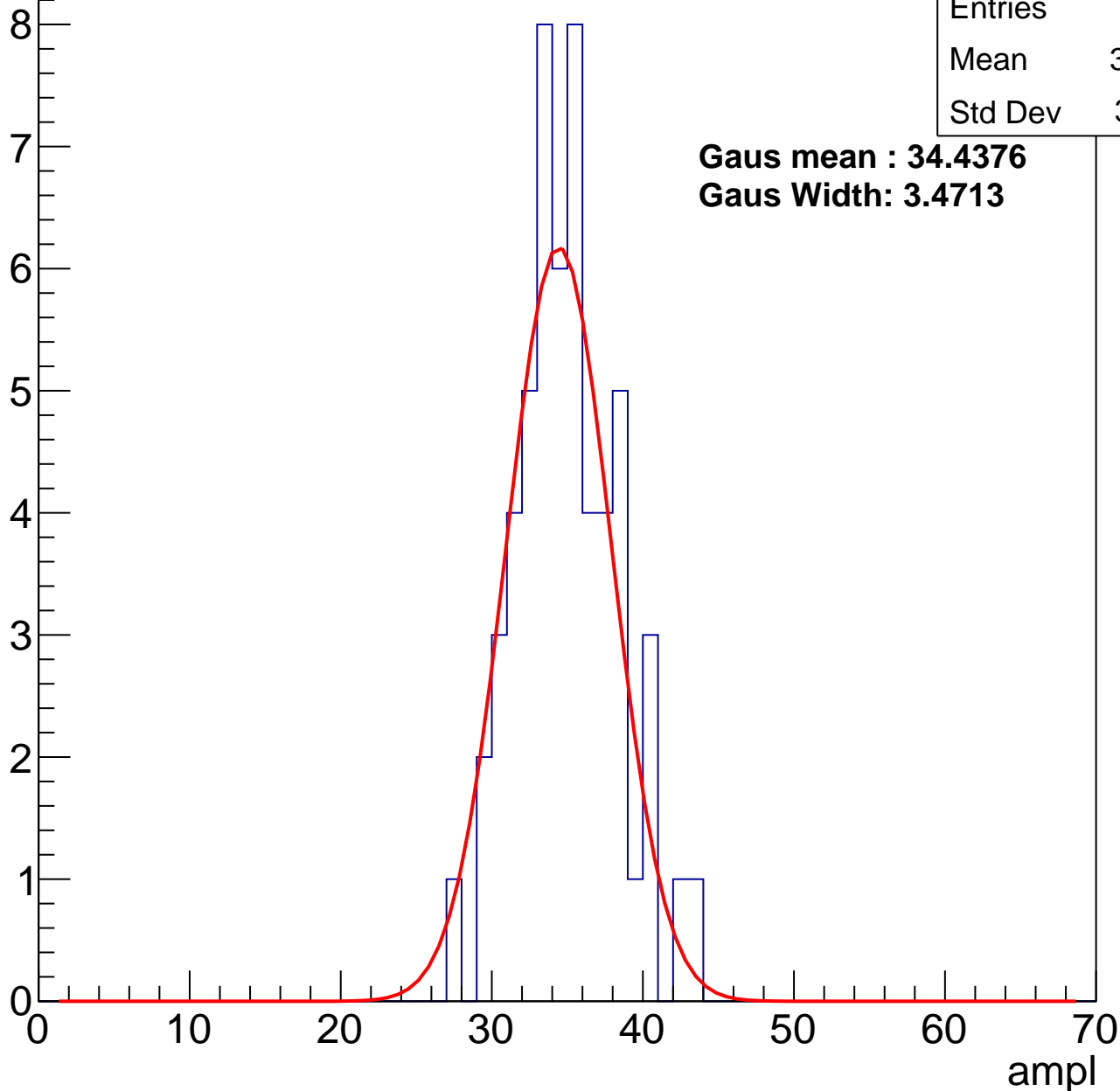
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	56
Mean	34.52
Std Dev	3.311

**Gaus mean : 34.4376**

**Gaus Width: 3.4713**



# B1L100S, U2-ch74, adc2

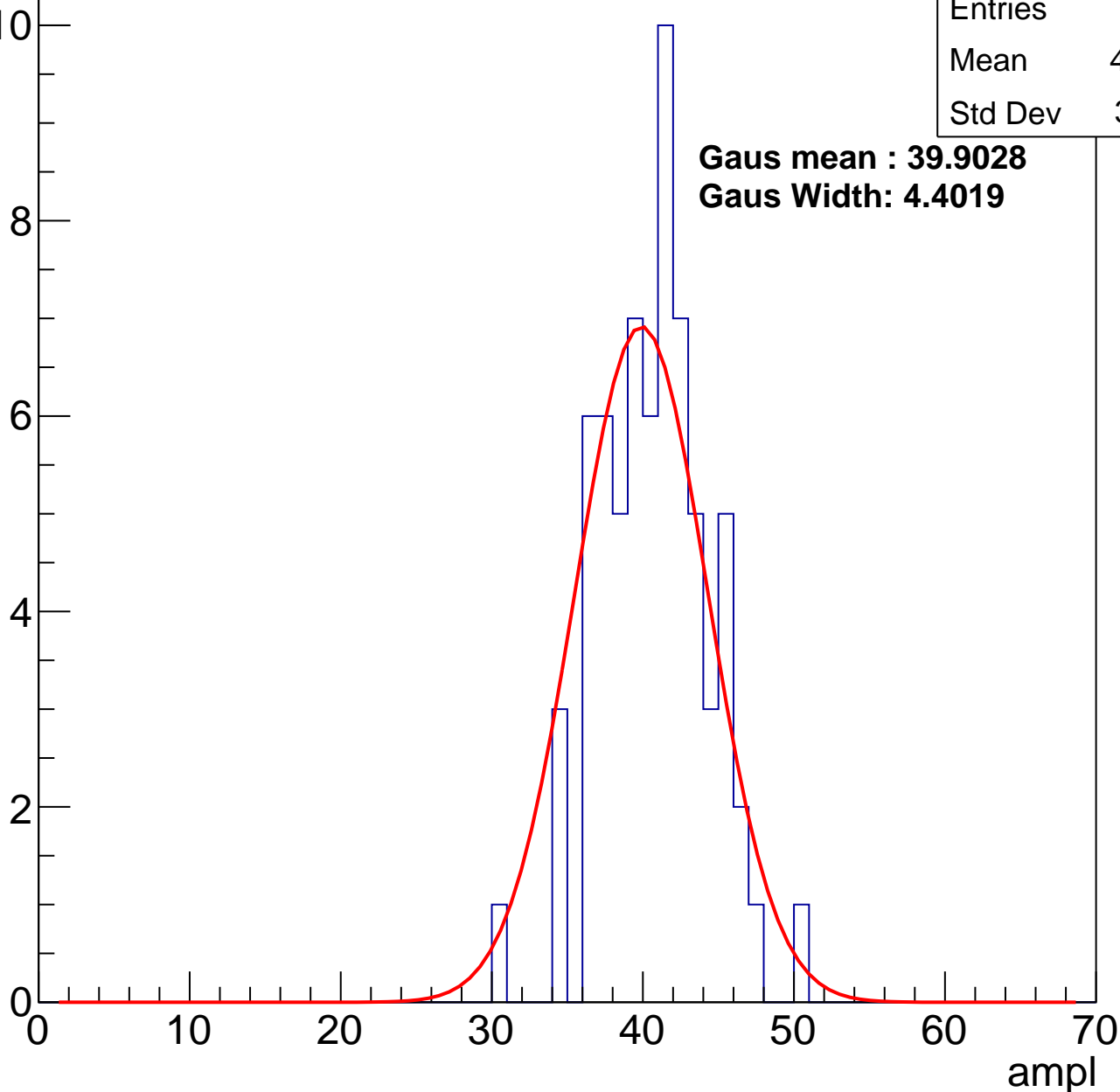
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	68
Mean	40.26
Std Dev	3.551

**Gaus mean : 39.9028**

**Gaus Width: 4.4019**

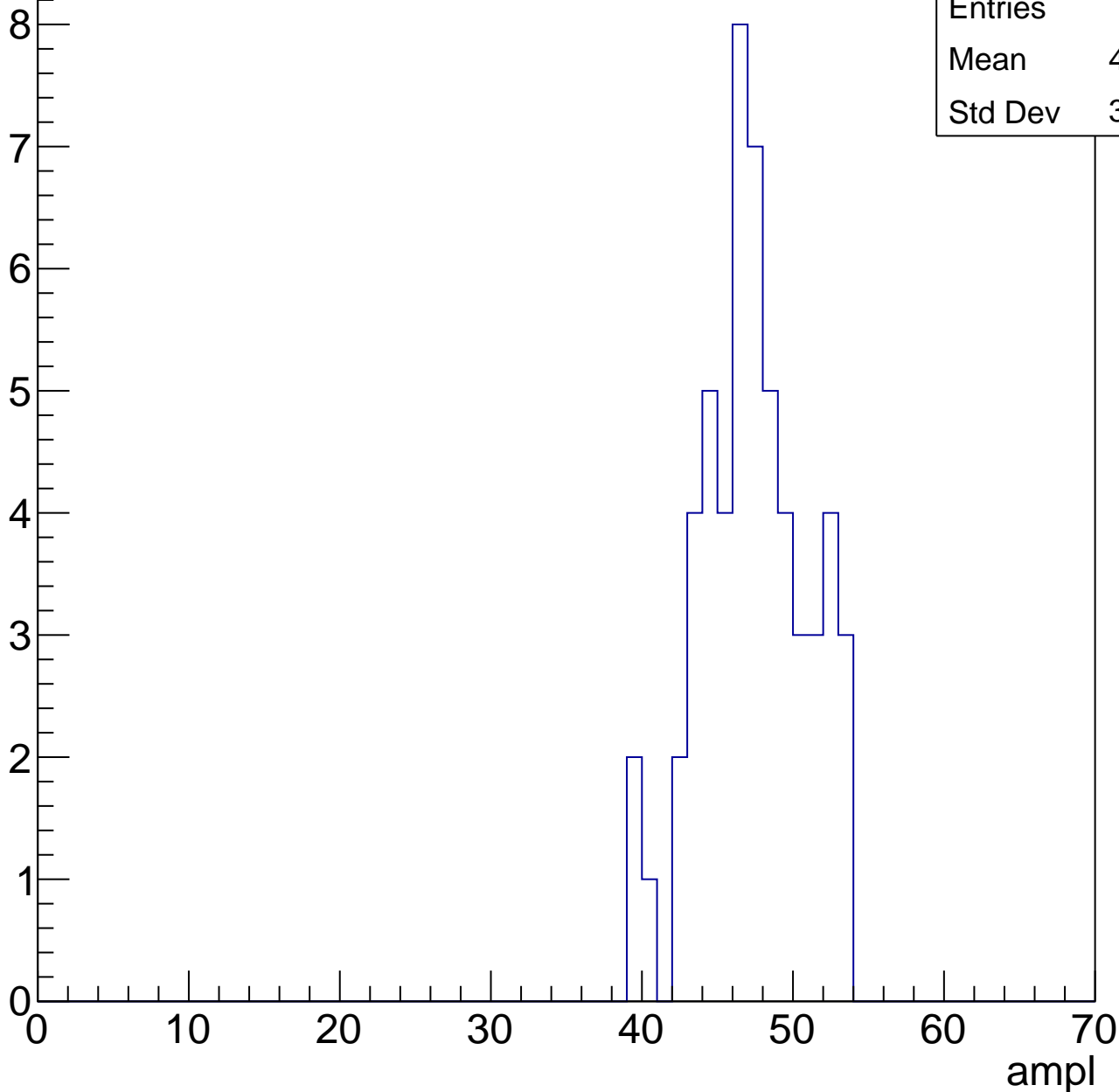


# B1L100S, U2-ch74, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

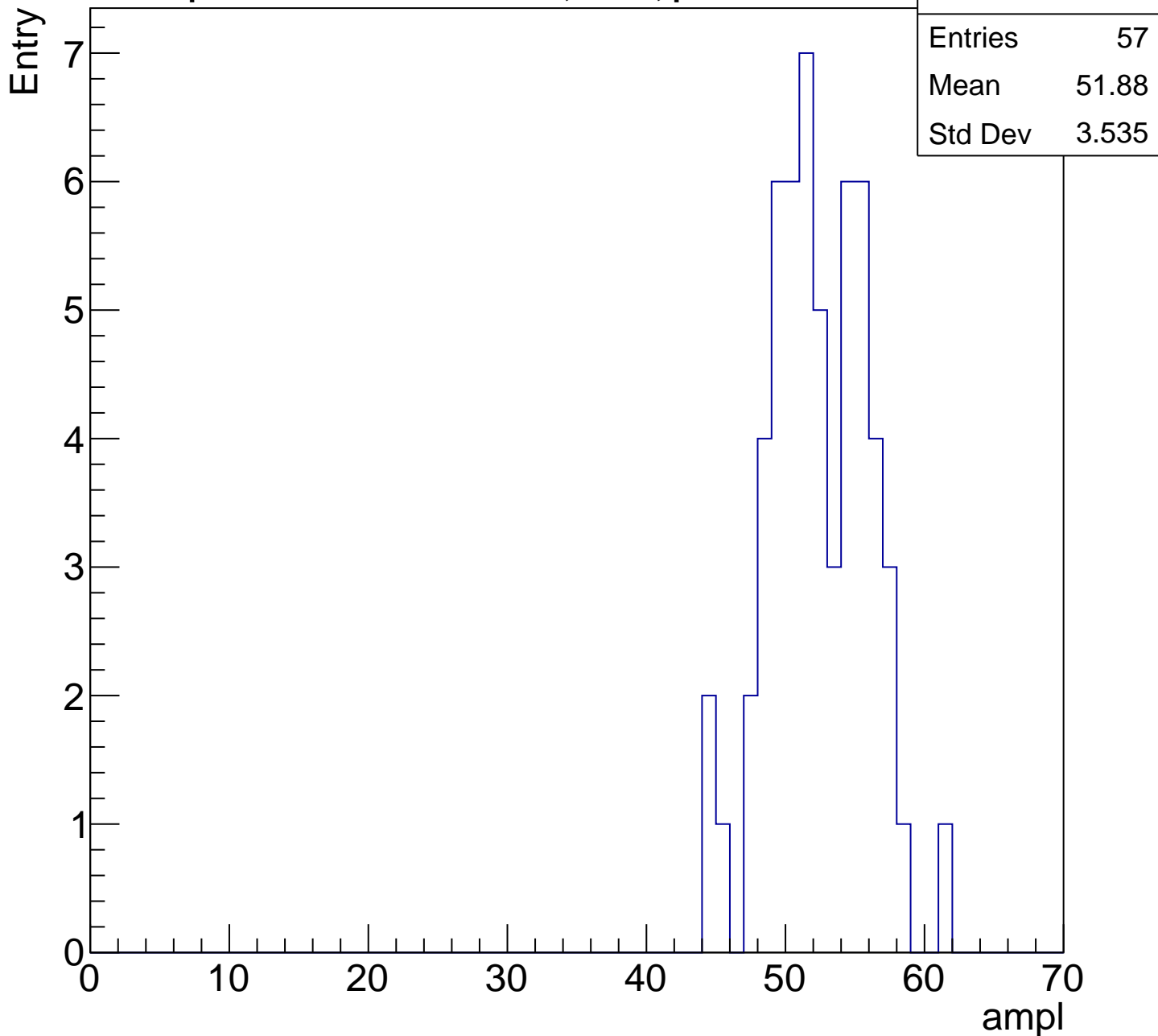
Entry

Entries	55
Mean	46.85
Std Dev	3.472



# B1L100S, U2-ch74, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

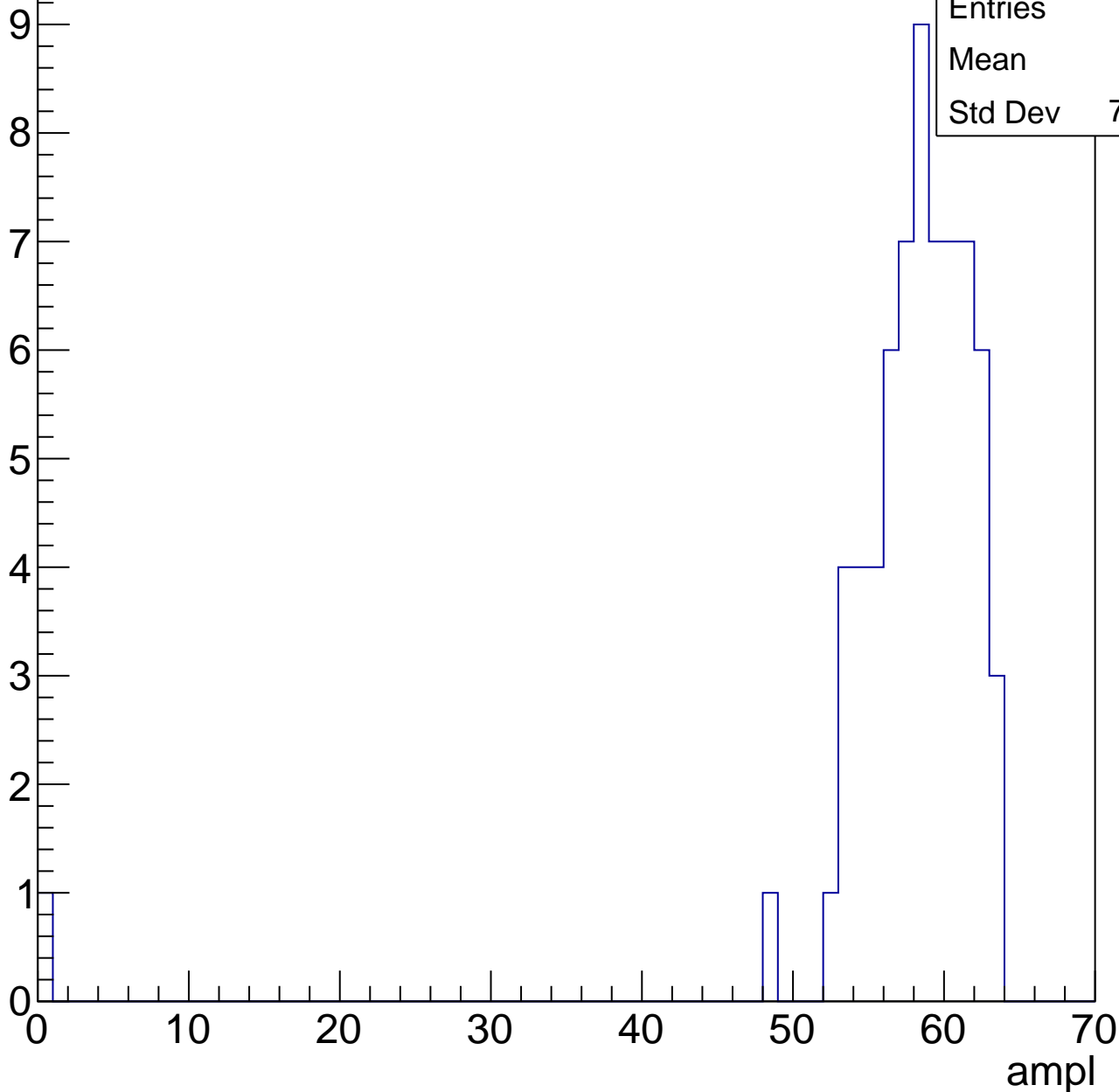


# B1L100S, U2-ch74, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

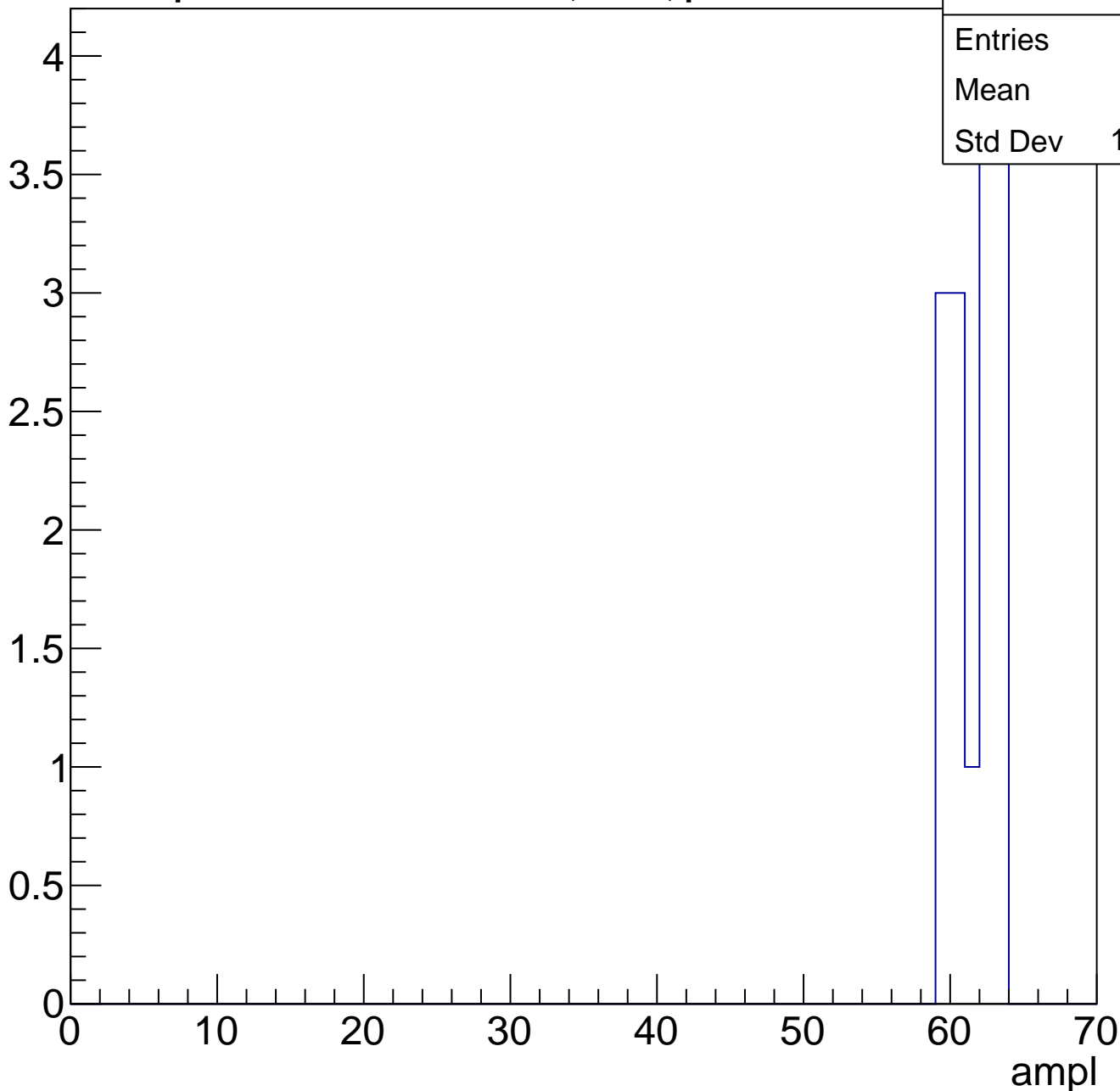
Entries	67
Mean	57.1
Std Dev	7.675



# B1L100S, U2-ch74, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

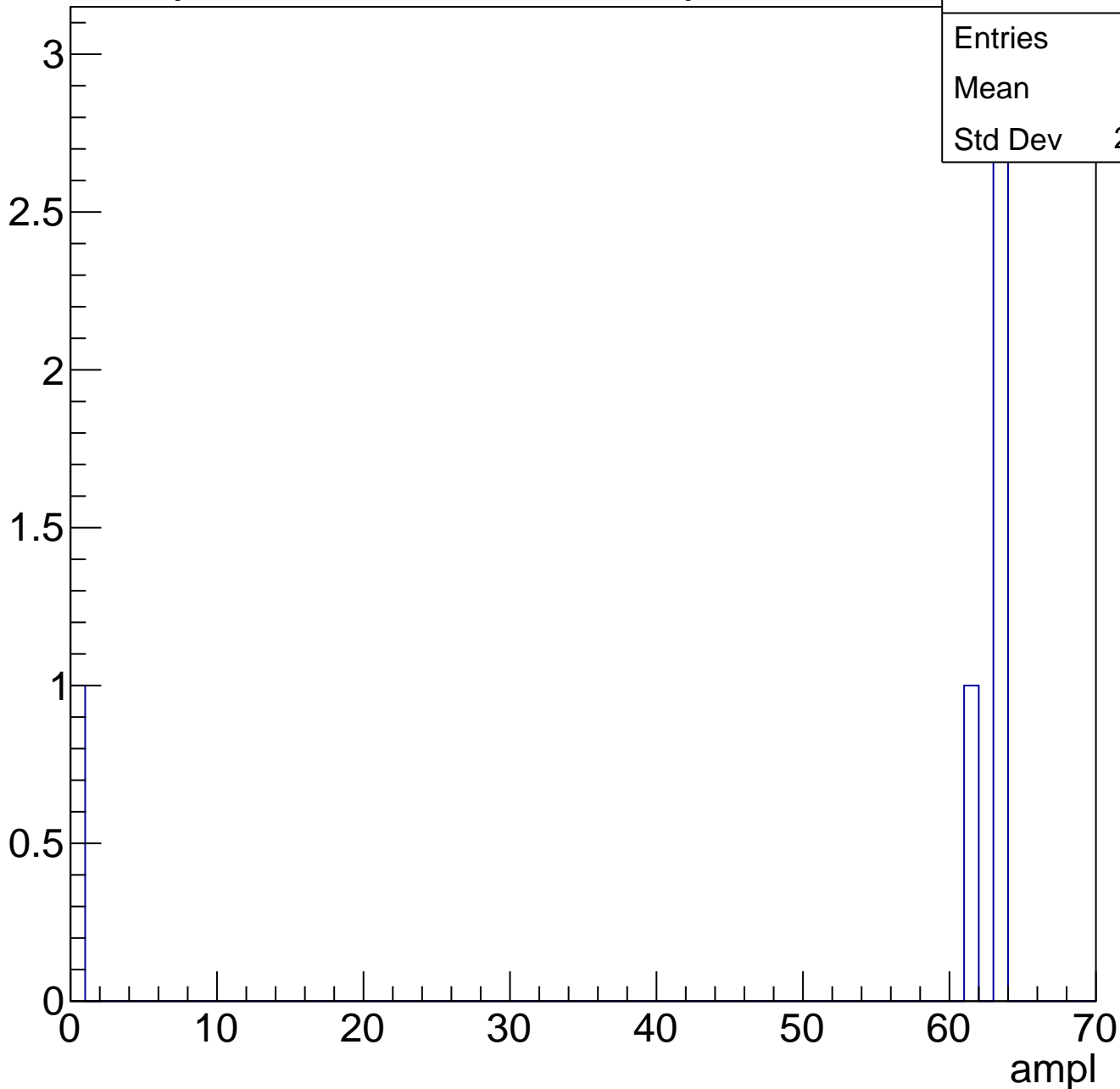




# B1L100S, U2-ch74, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



# B1L100S, U2-ch75, adc0

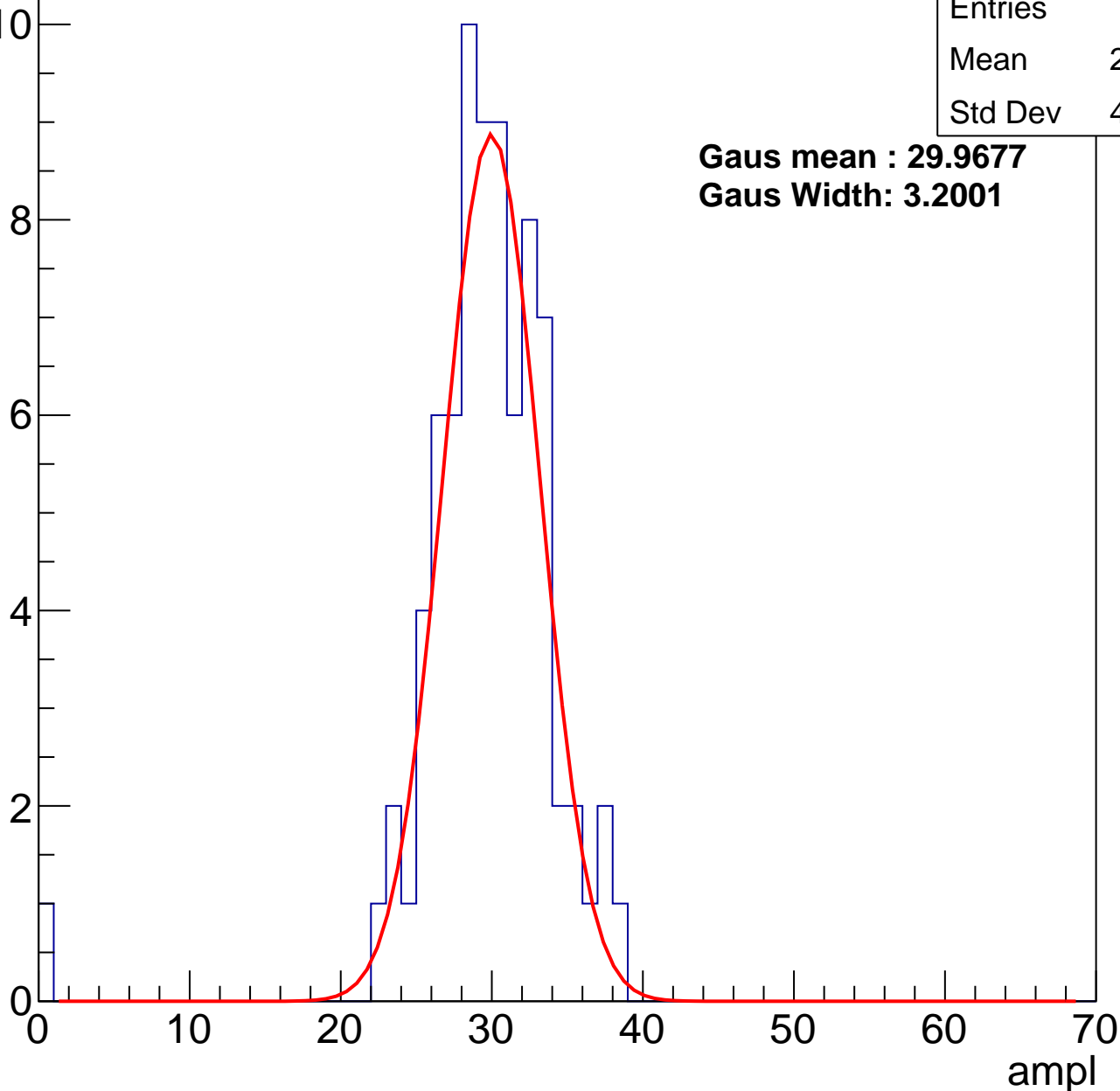
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	78
Mean	29.23
Std Dev	4.712

**Gaus mean : 29.9677**

**Gaus Width: 3.2001**



# B1L100S, U2-ch75, adc1

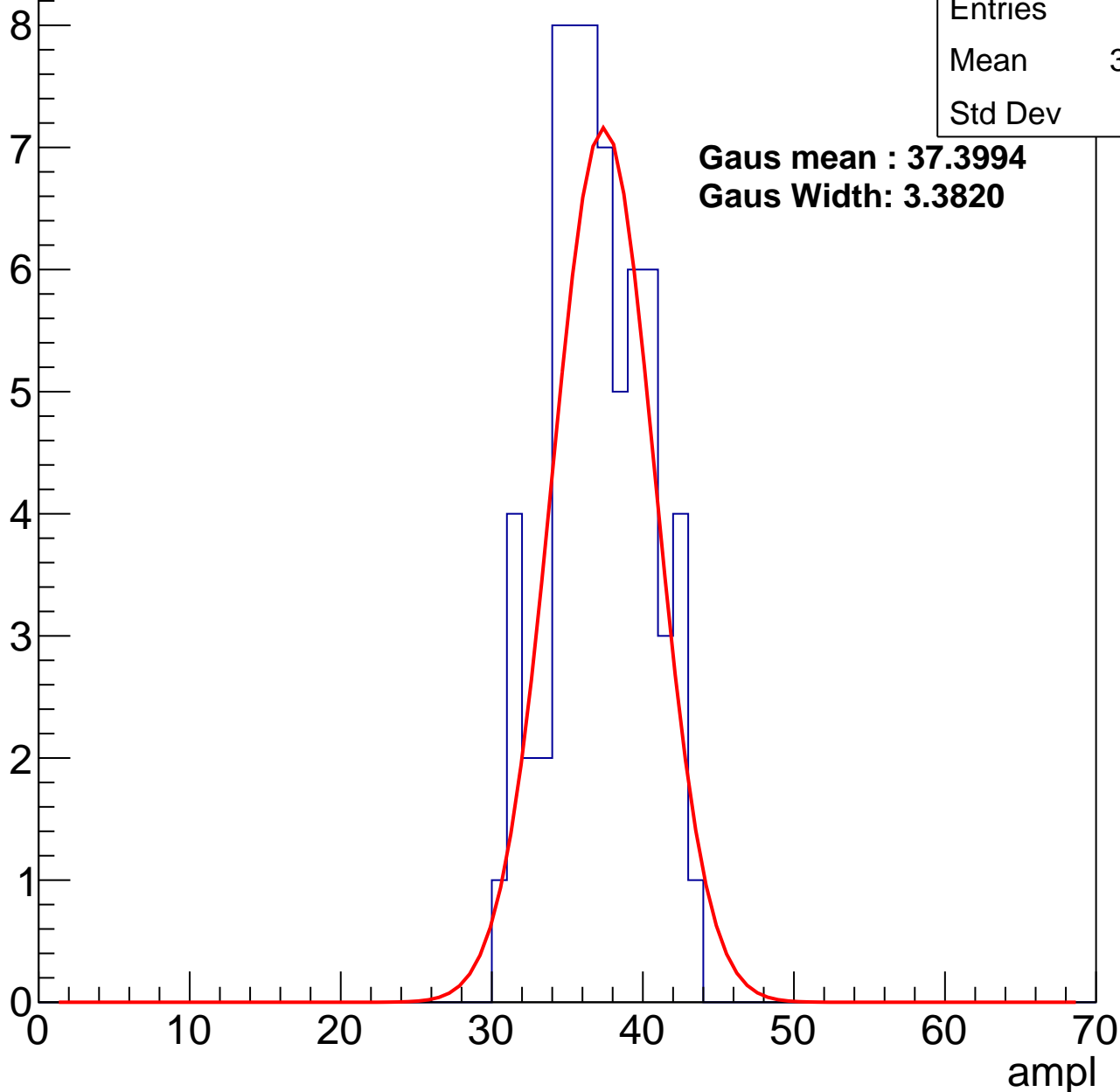
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	65
Mean	36.63
Std Dev	3.15

**Gaus mean : 37.3994**

**Gaus Width: 3.3820**



# B1L100S, U2-ch75, adc2

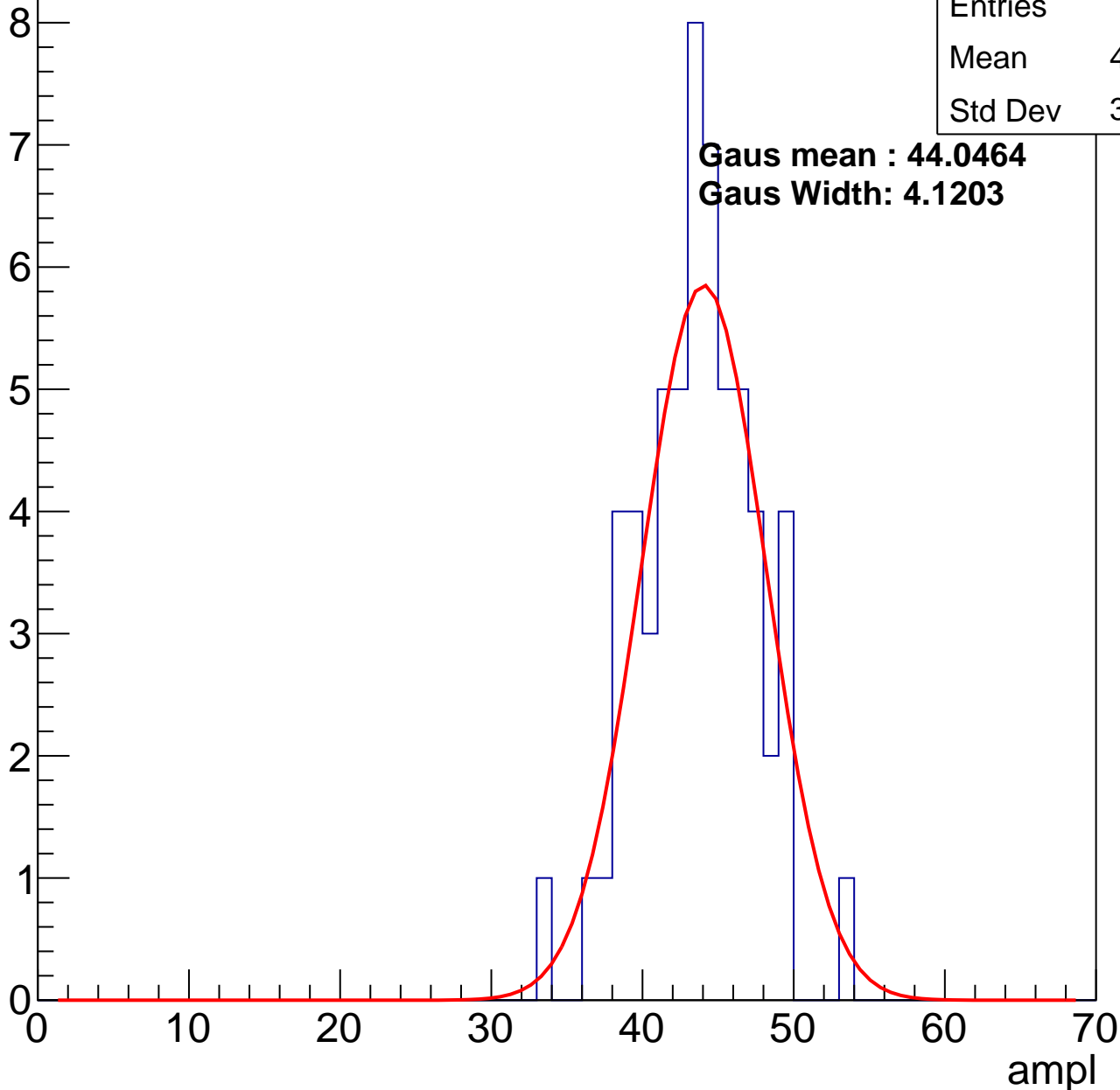
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	60
Mean	43.15
Std Dev	3.719

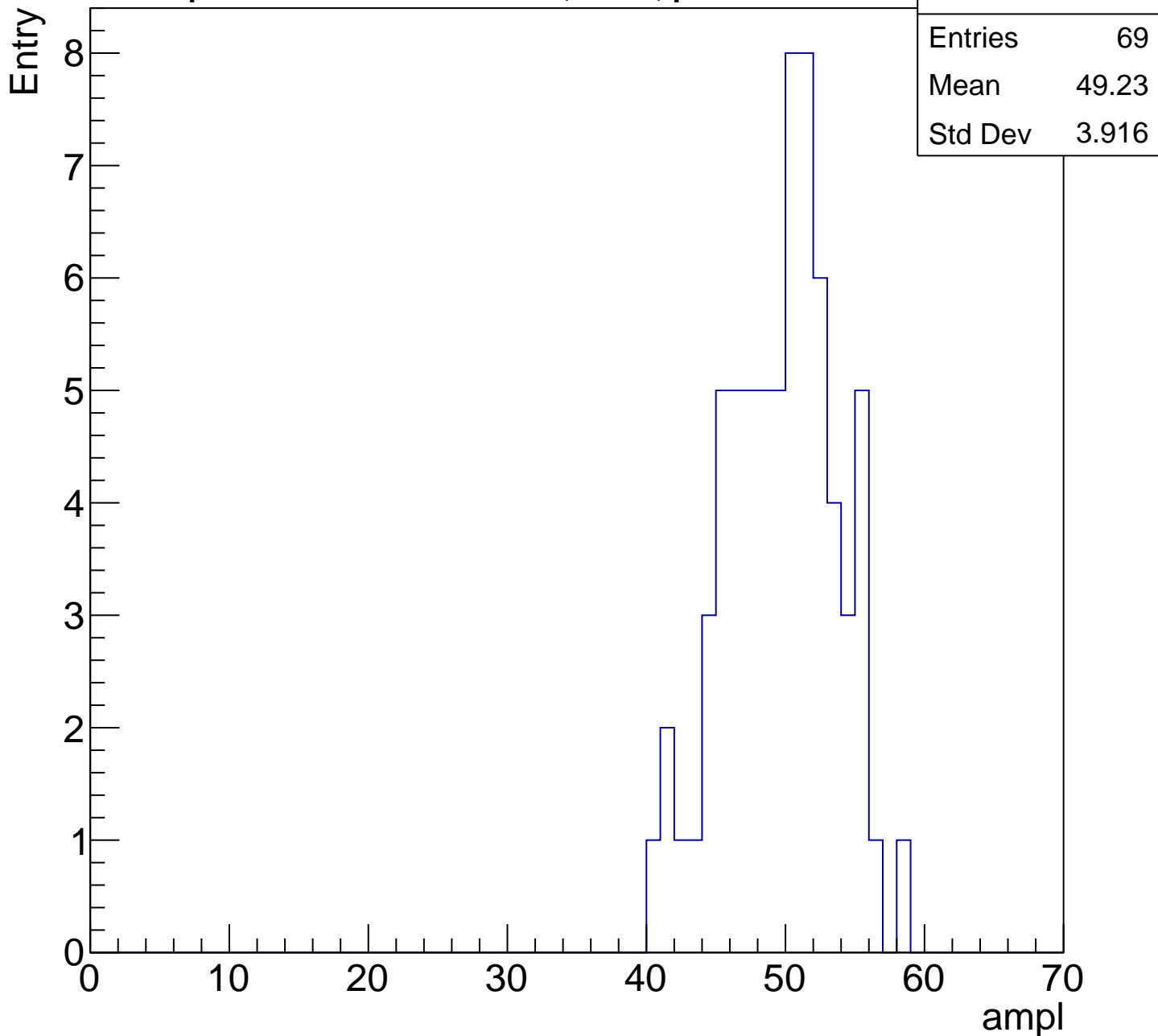
**Gaus mean : 44.0464**

**Gaus Width: 4.1203**



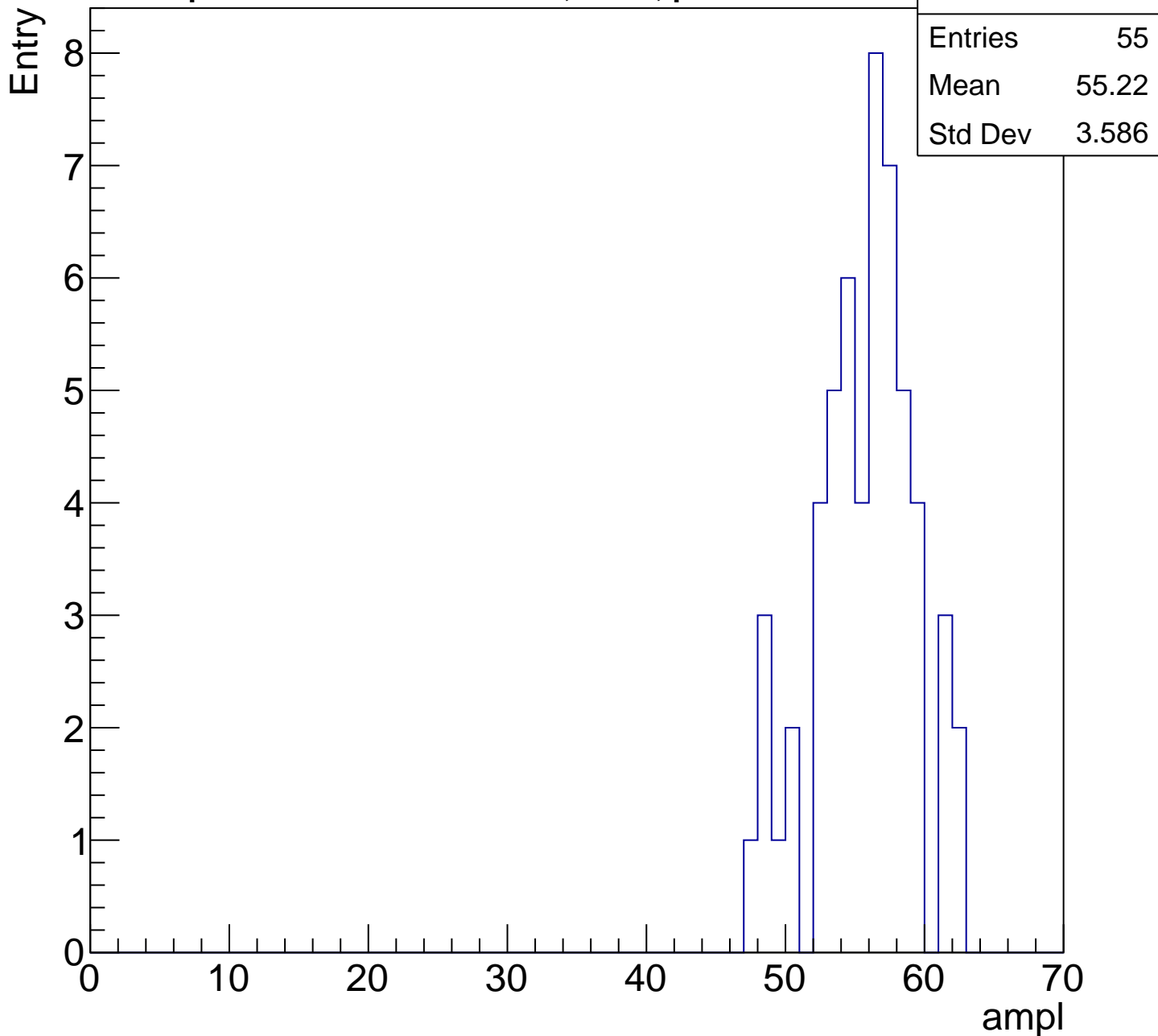
# B1L100S, U2-ch75, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2



# B1L100S, U2-ch75, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

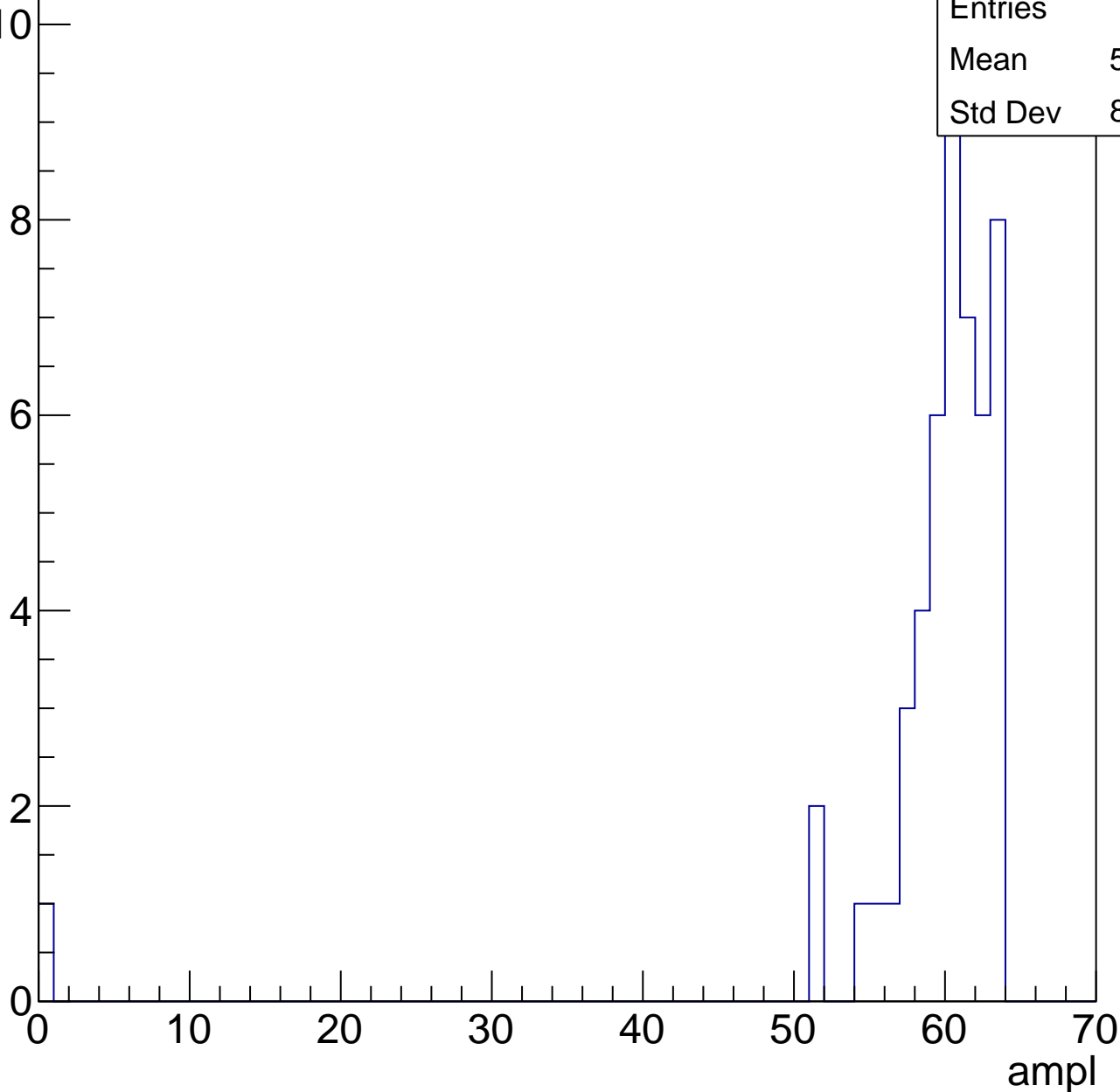


# B1L100S, U2-ch75, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	50
Mean	58.54
Std Dev	8.814



# B1L100S, U2-ch75, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry





# B1L100S, U2-ch75, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



# B1L100S, U2-ch76, adc0

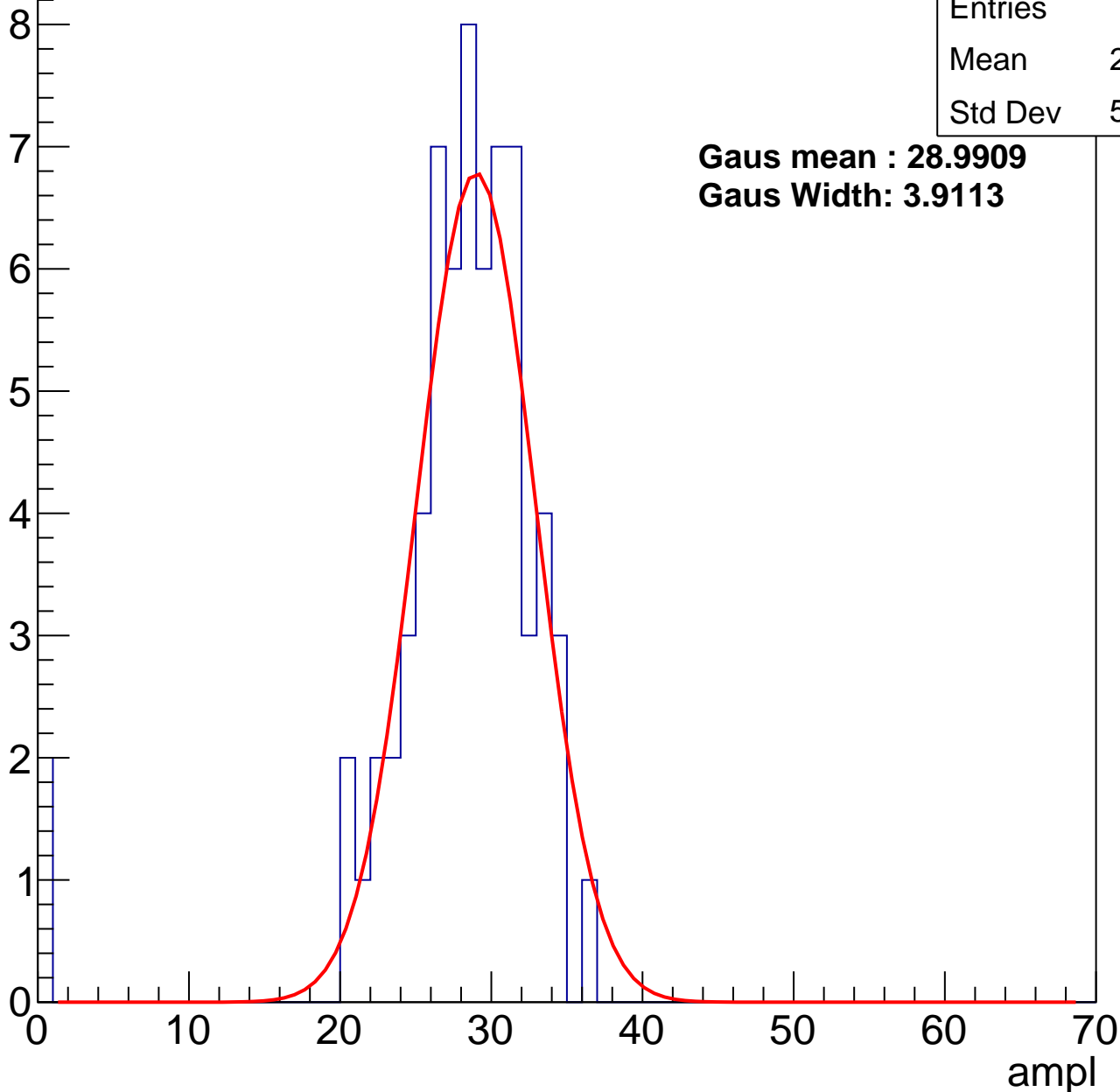
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	68
Mean	27.32
Std Dev	5.905

**Gaus mean : 28.9909**

**Gaus Width: 3.9113**



# B1L100S, U2-ch76, adc1

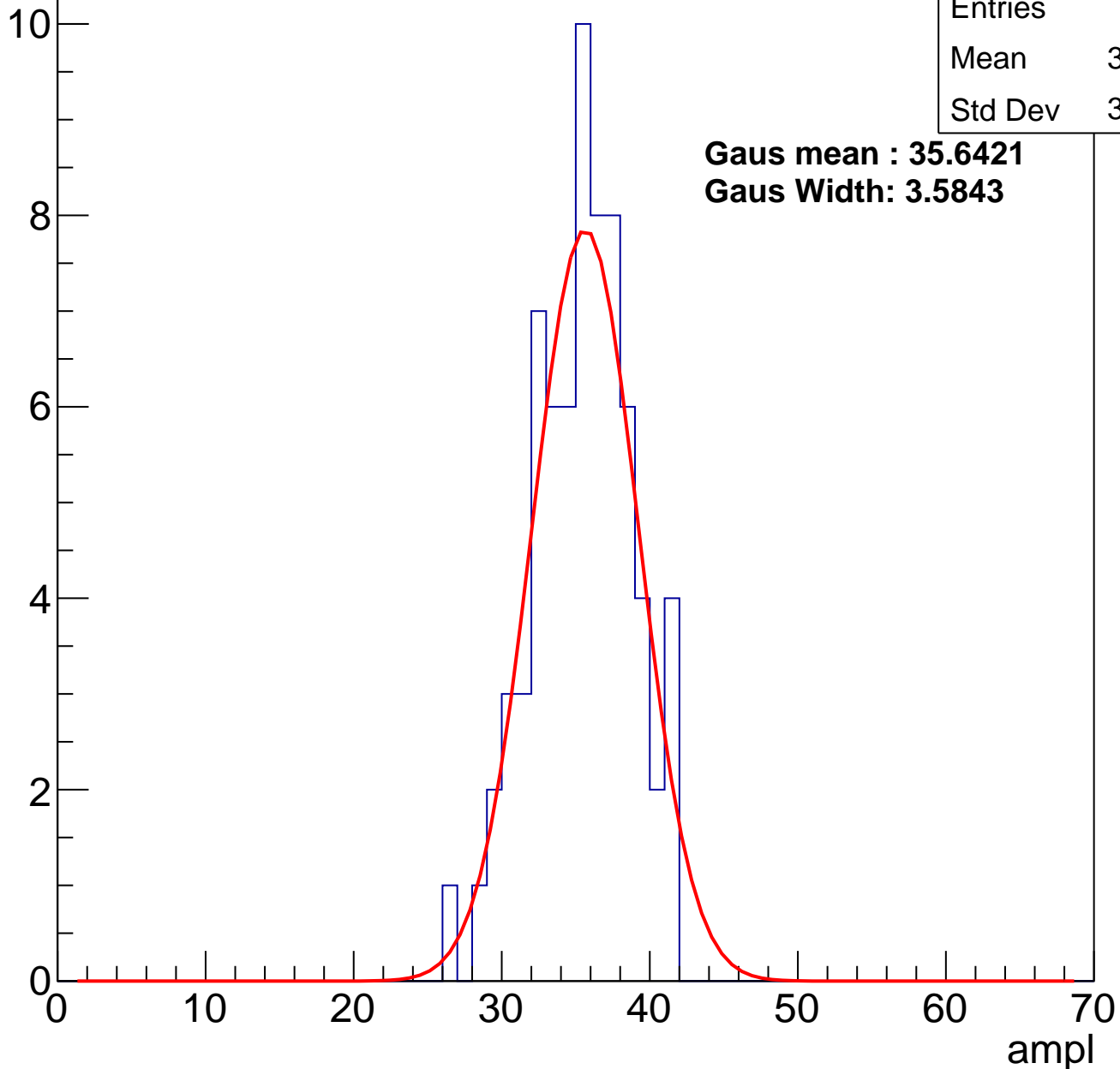
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	71
Mean	34.97
Std Dev	3.293

**Gaus mean : 35.6421**

**Gaus Width: 3.5843**

Entry



# B1L100S, U2-ch76, adc2

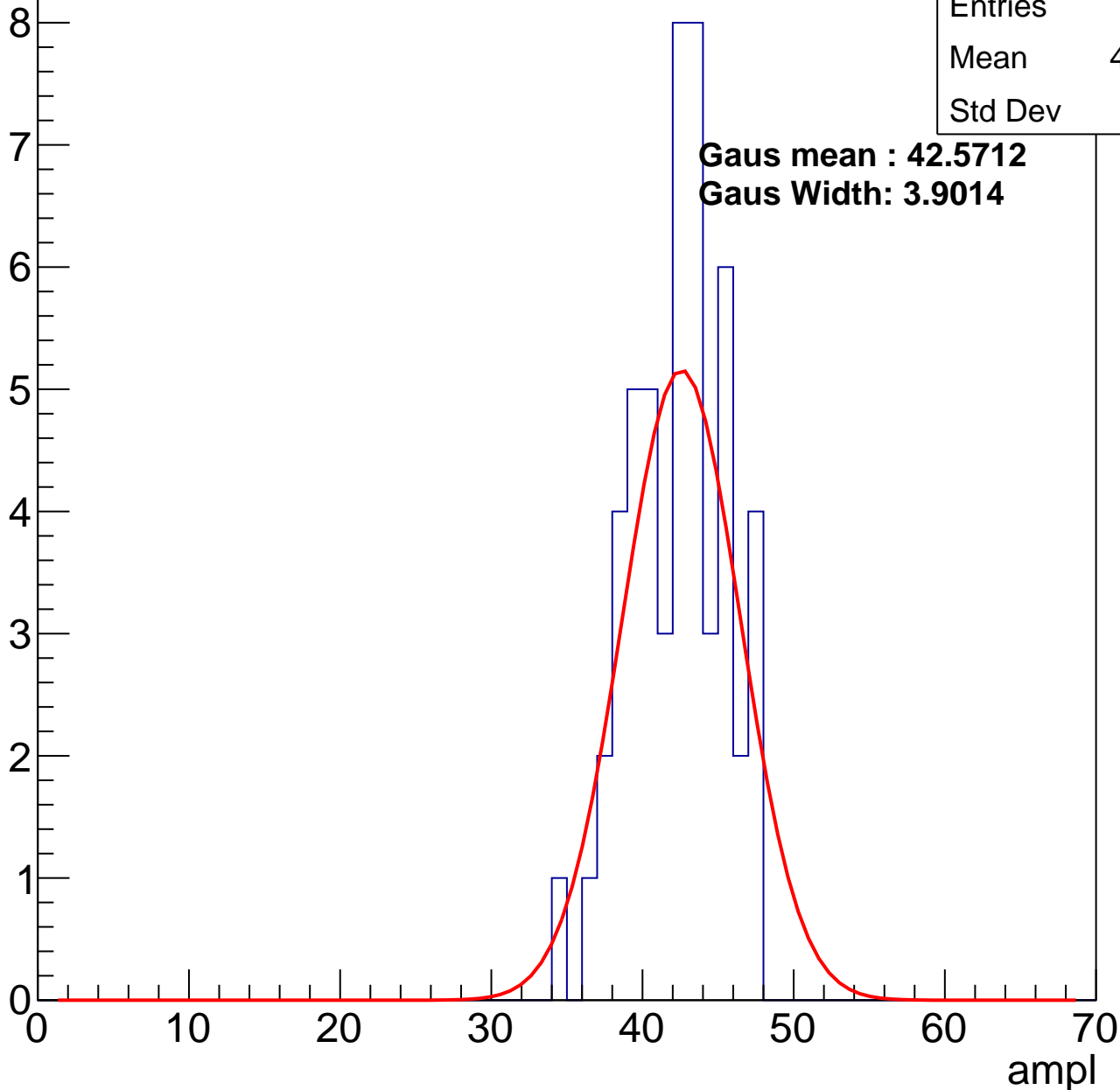
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	52
Mean	41.85
Std Dev	3.06

**Gaus mean : 42.5712**

**Gaus Width: 3.9014**



# B1L100S, U2-ch76, adc3

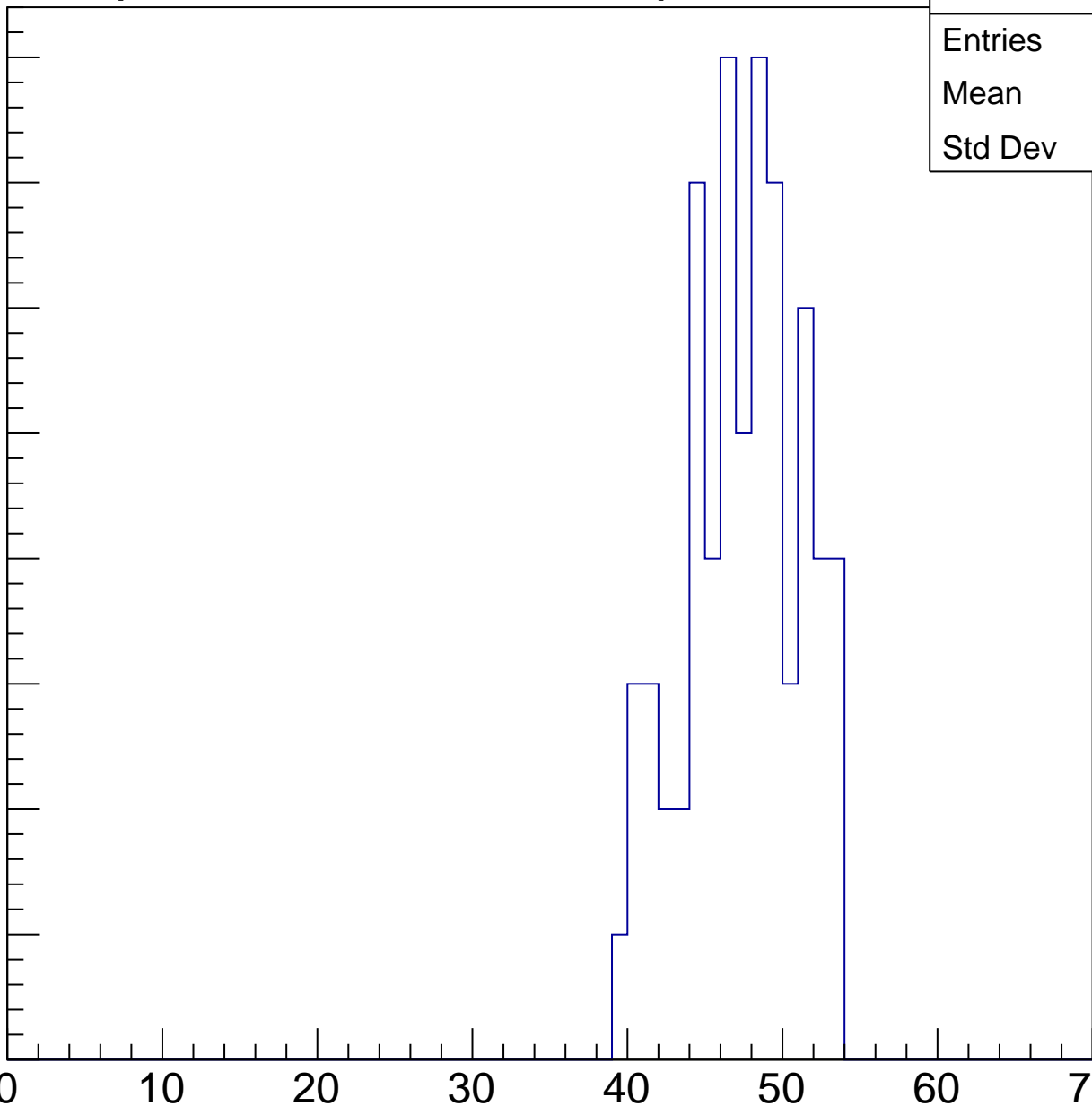
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	67
Mean	46.96
Std Dev	3.646

ampl



# B1L100S, U2-ch76, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

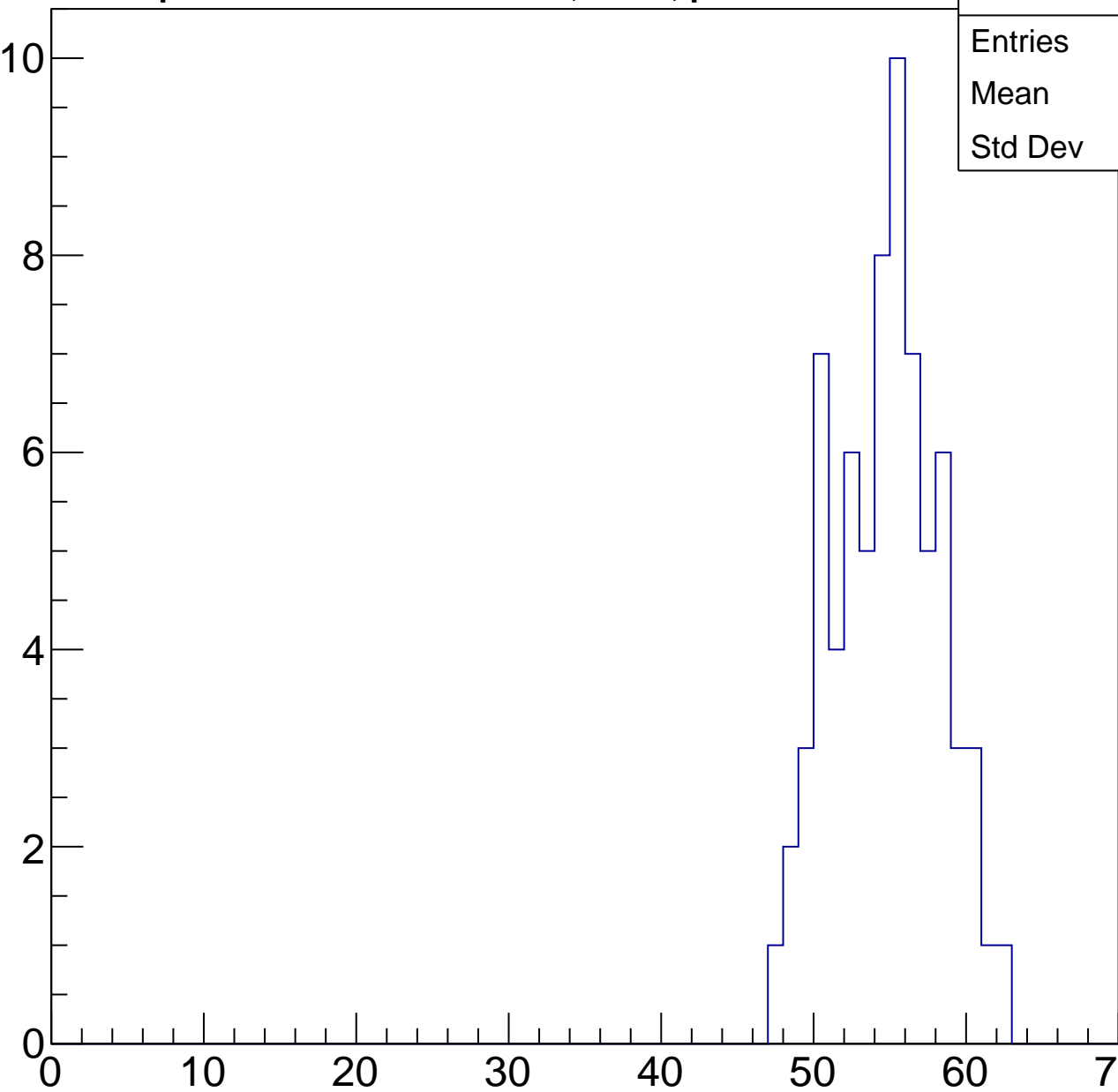
Entries	72
Mean	54.28
Std Dev	3.421

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

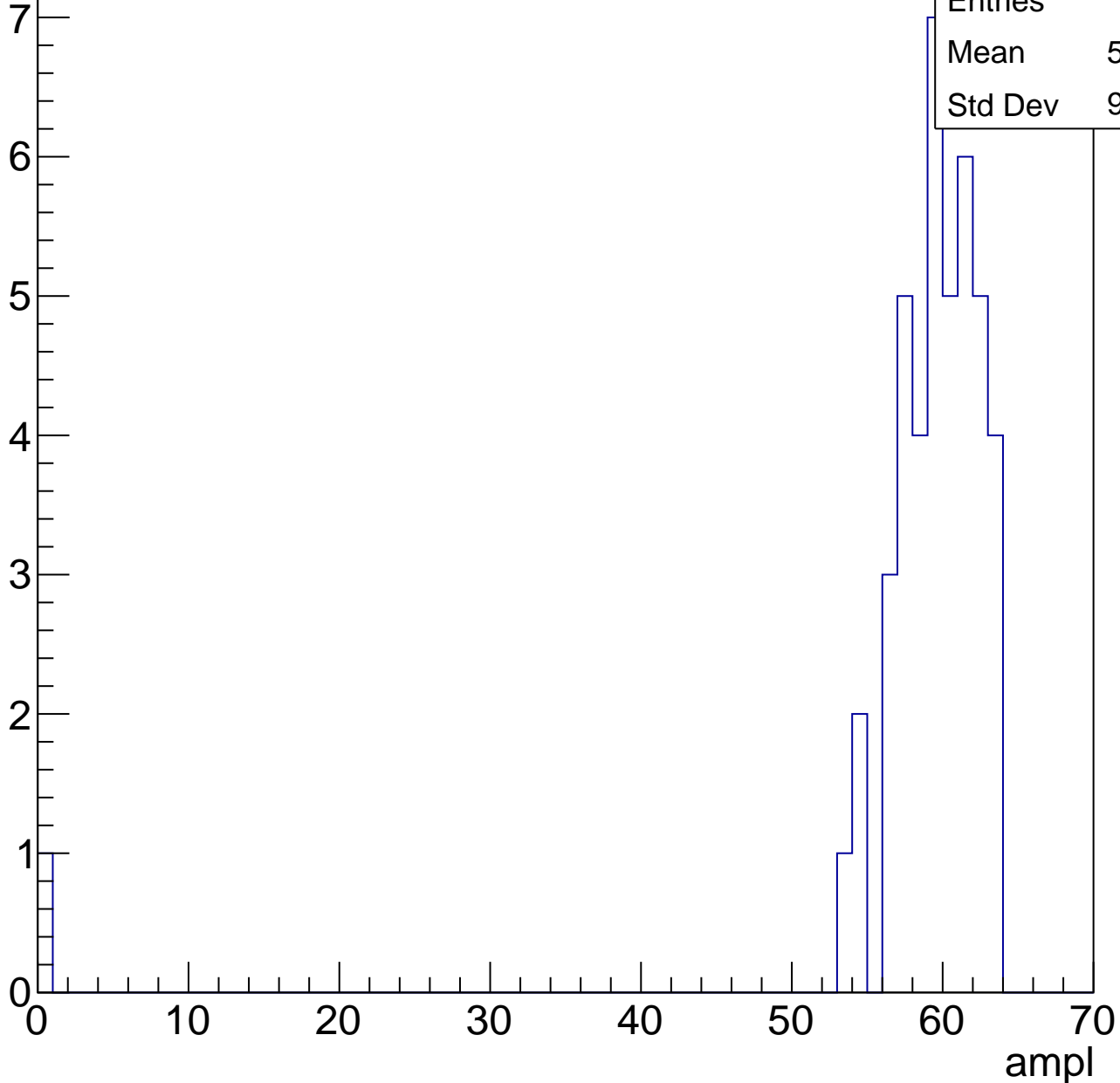


# B1L100S, U2-ch76, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	43
Mean	57.84
Std Dev	9.273

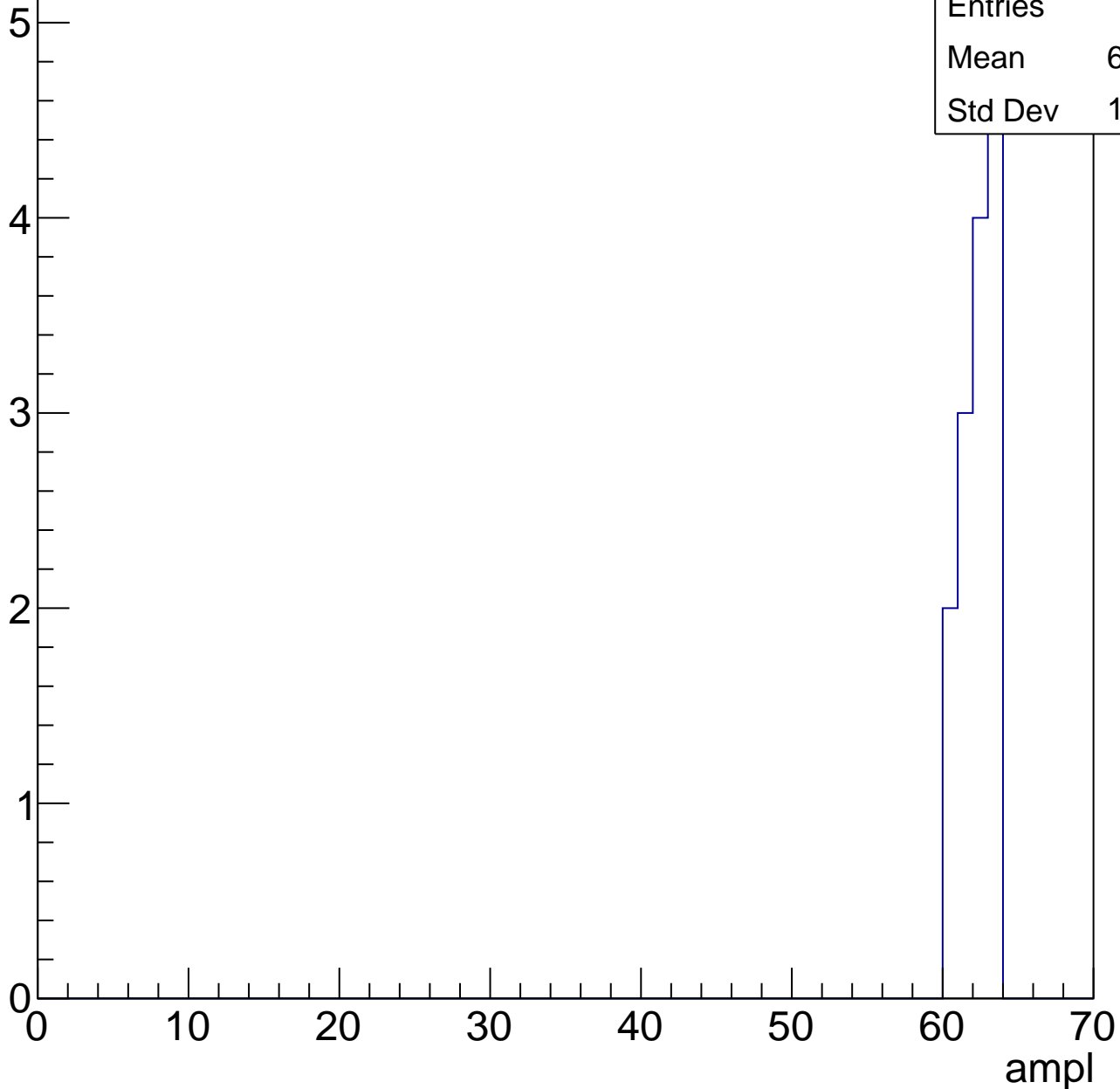


# B1L100S, U2-ch76, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	14
Mean	61.86
Std Dev	1.059





# B1L100S, U2-ch76, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	3
Mean	21
Std Dev	29.7

# B1L100S, U2-ch77, adc0

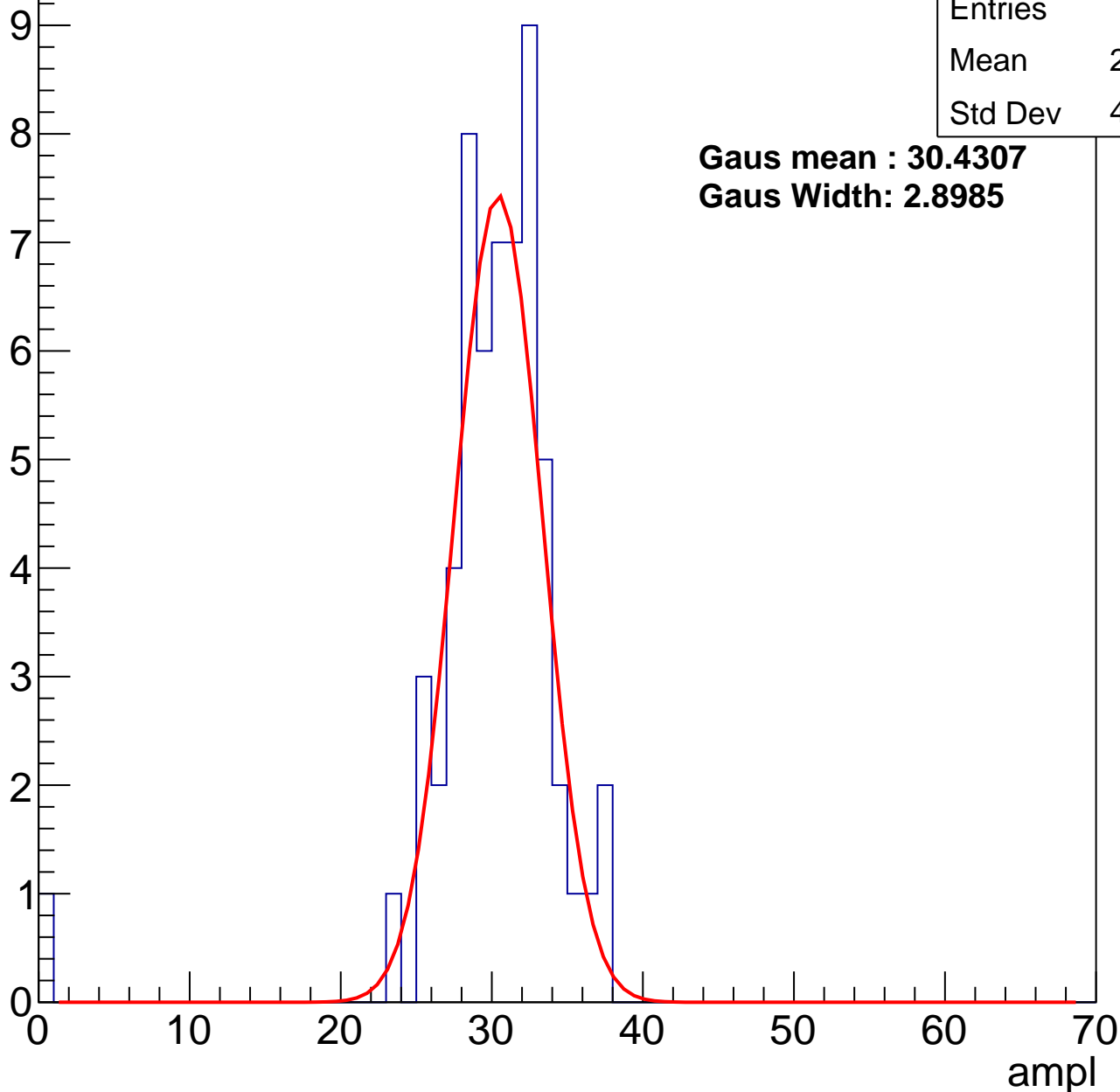
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	59
Mean	29.64
Std Dev	4.874

**Gaus mean : 30.4307**

**Gaus Width: 2.8985**



# B1L100S, U2-ch77, adc1

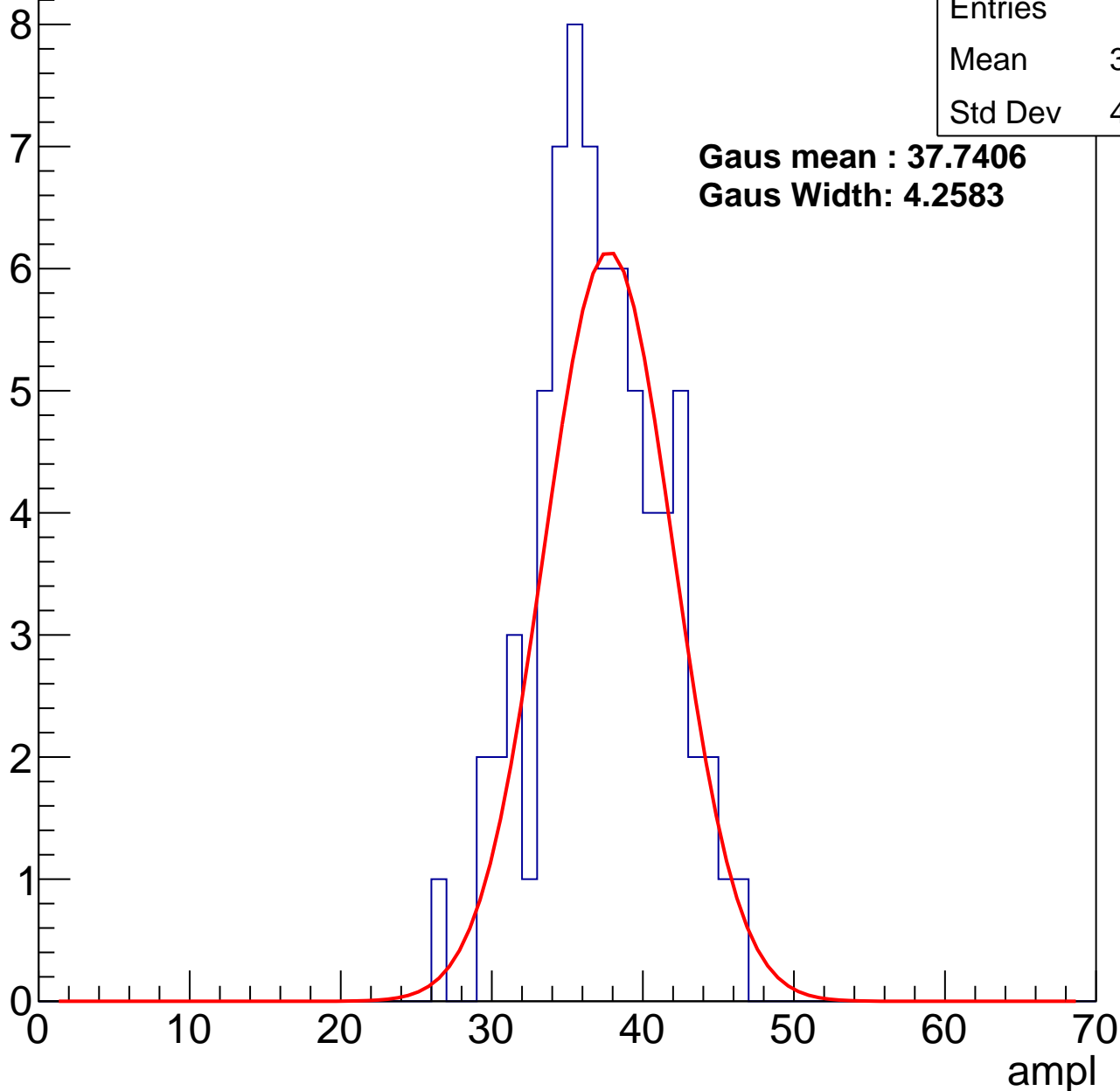
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	72
Mean	36.78
Std Dev	4.124

**Gaus mean : 37.7406**

**Gaus Width: 4.2583**



# B1L100S, U2-ch77, adc2

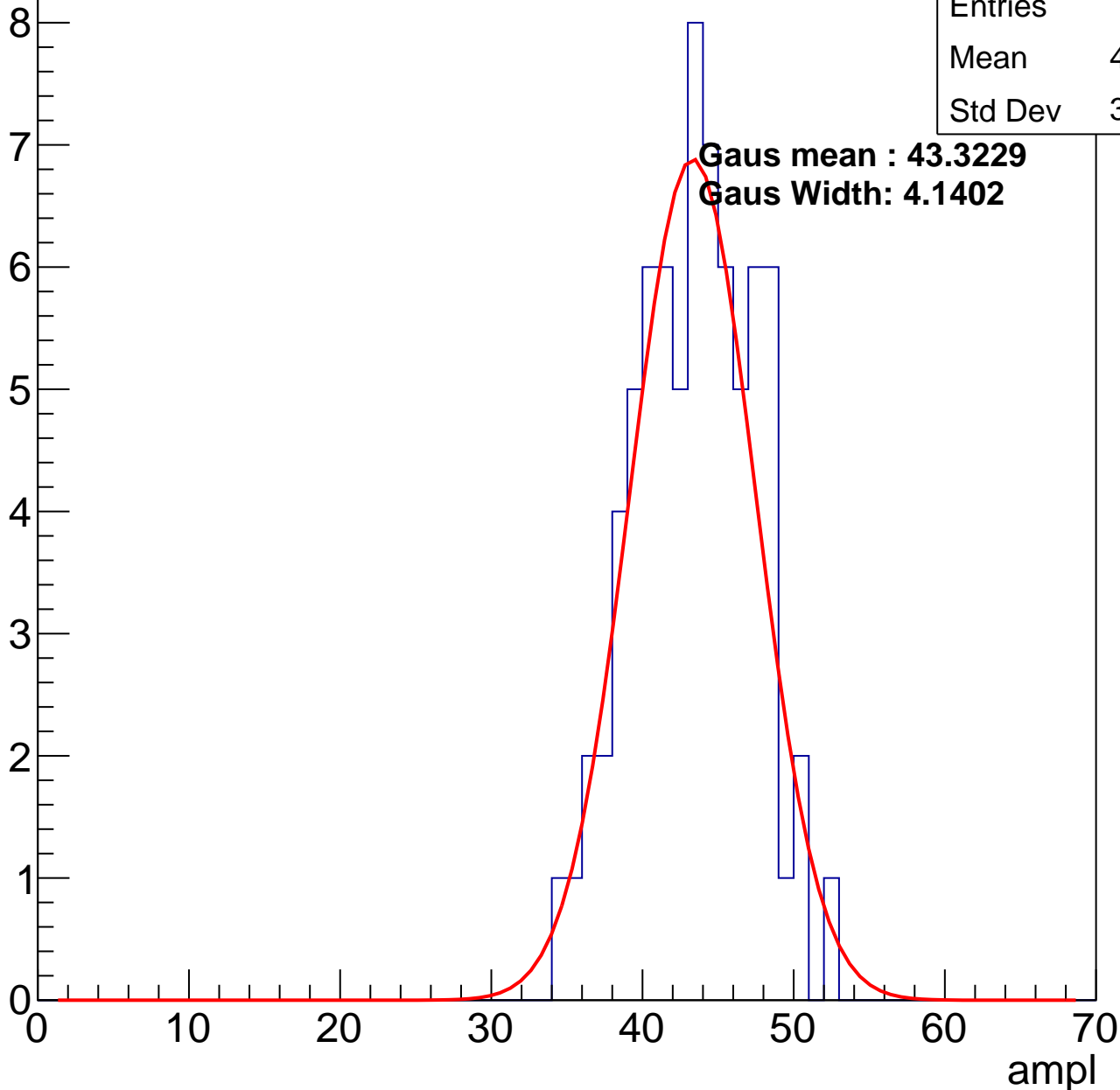
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	74
Mean	42.99
Std Dev	3.882

**Gaus mean : 43.3229**

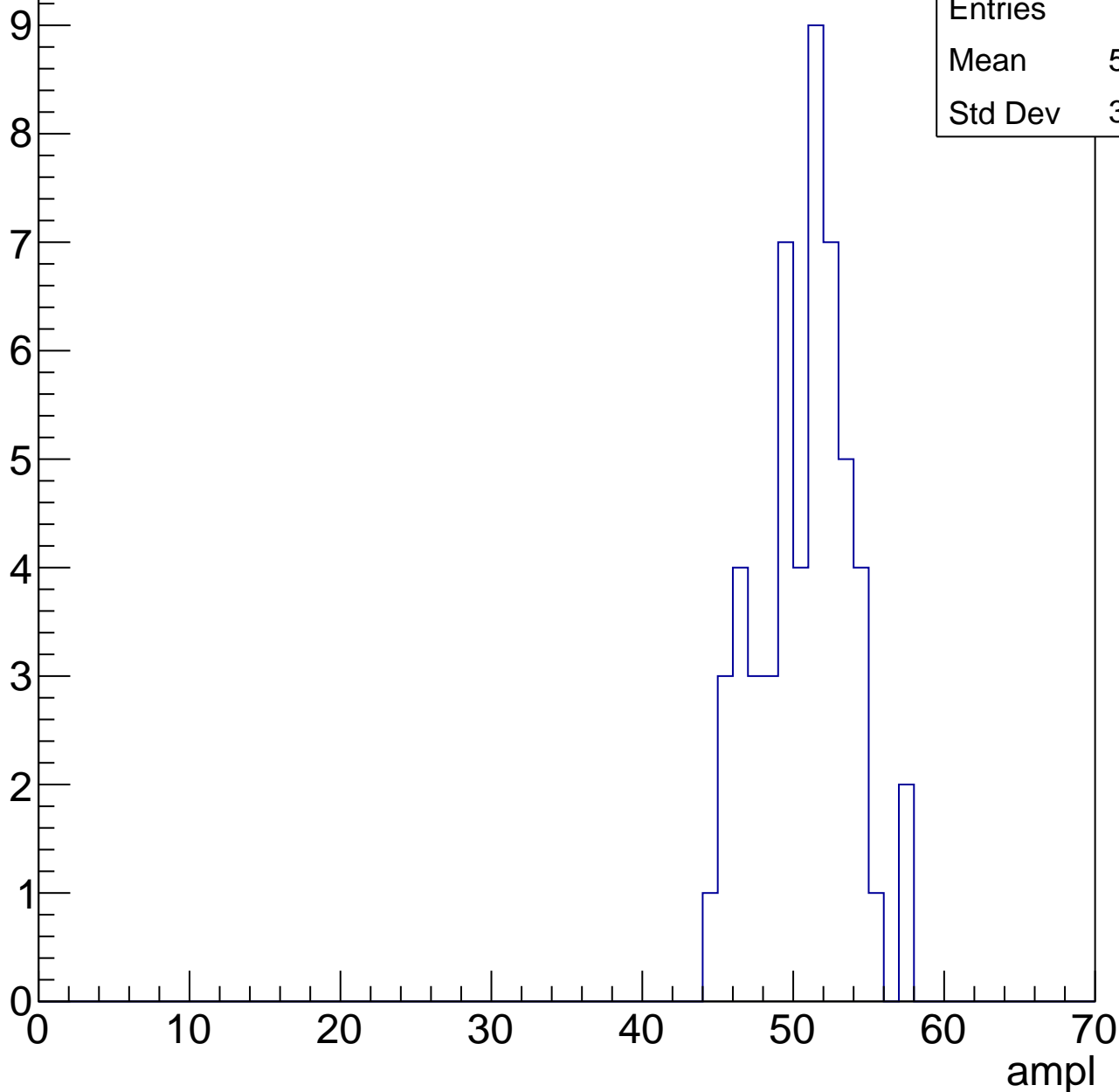
**Gaus Width: 4.1402**



# B1L100S, U2-ch77, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



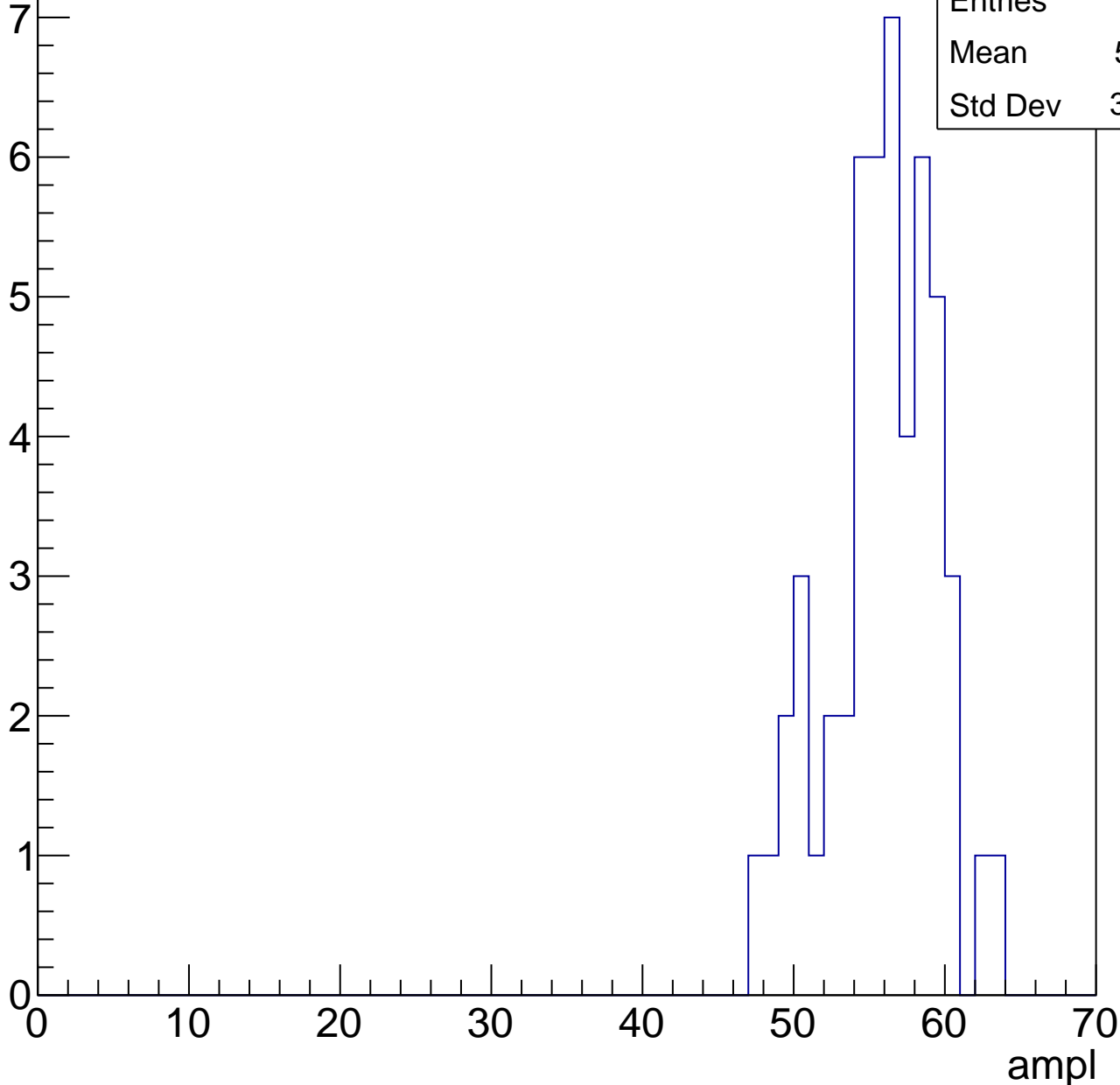
Entries	53
Mean	50.26
Std Dev	3.029

# B1L100S, U2-ch77, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	51
Mean	55.41
Std Dev	3.554

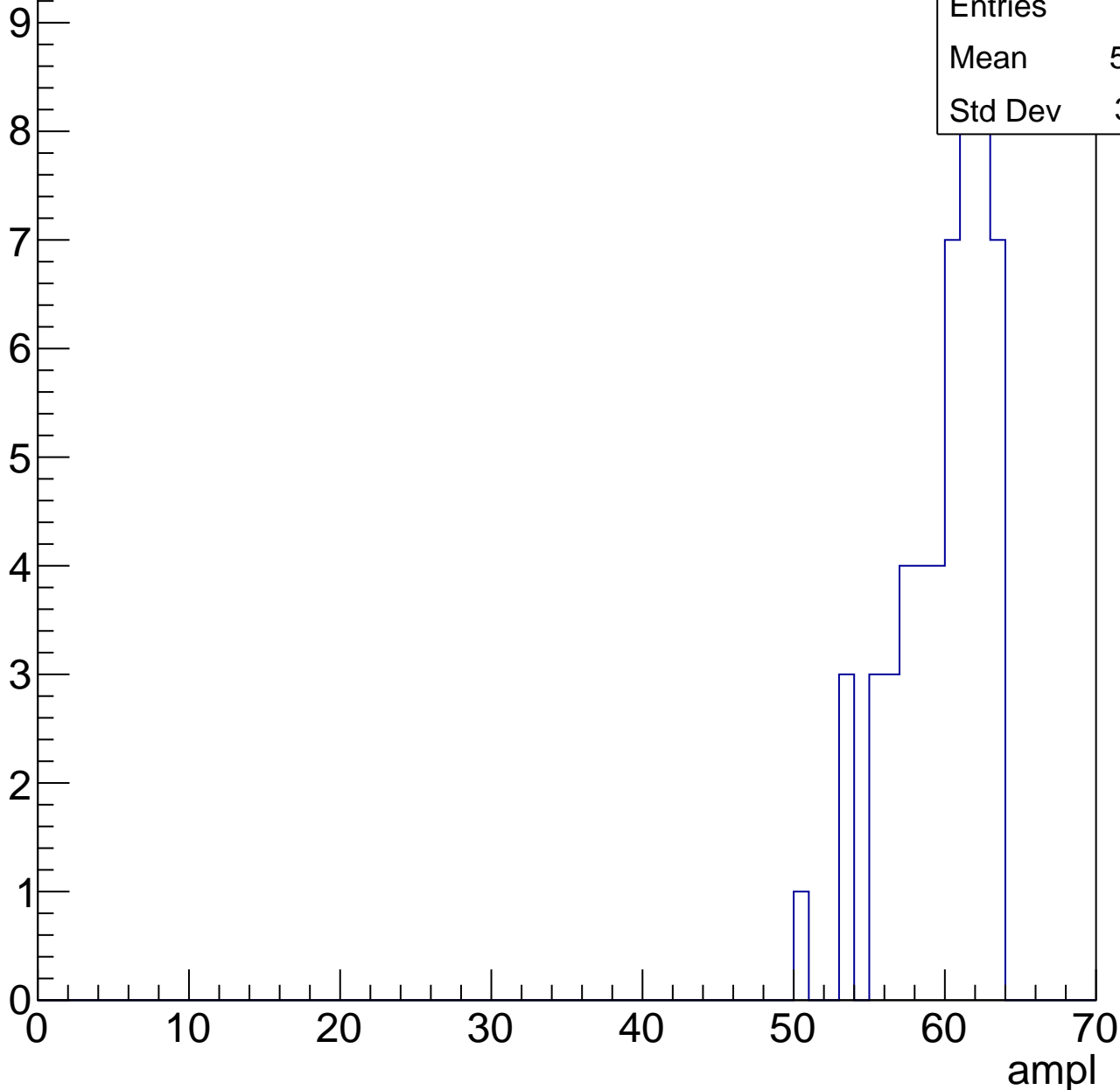


# B1L100S, U2-ch77, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

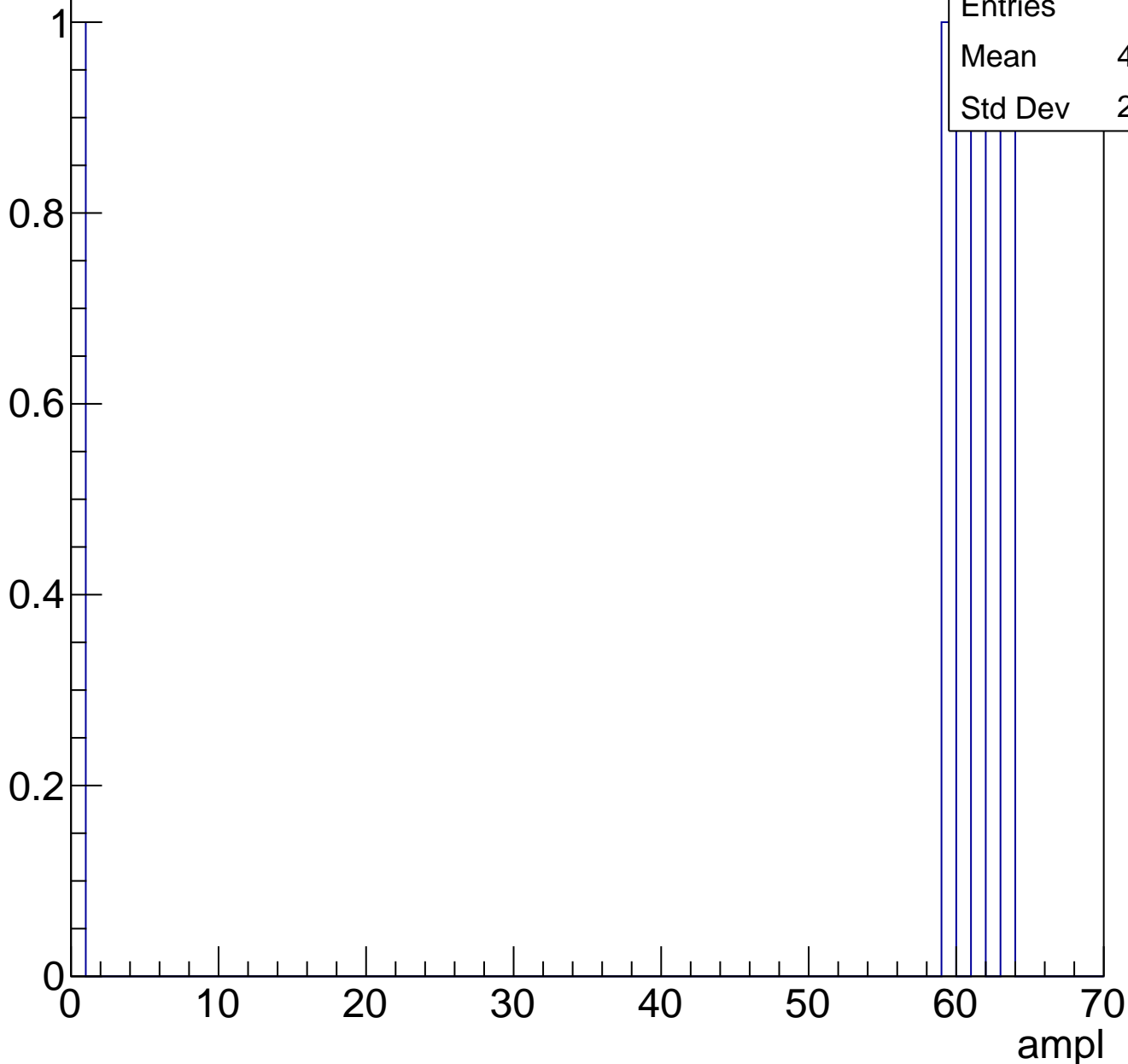
Entries	54
Mean	59.37
Std Dev	3.081



# B1L100S, U2-ch77, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry





# B1L100S, U2-ch77, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



# B1L100S, U2-ch78, adc0

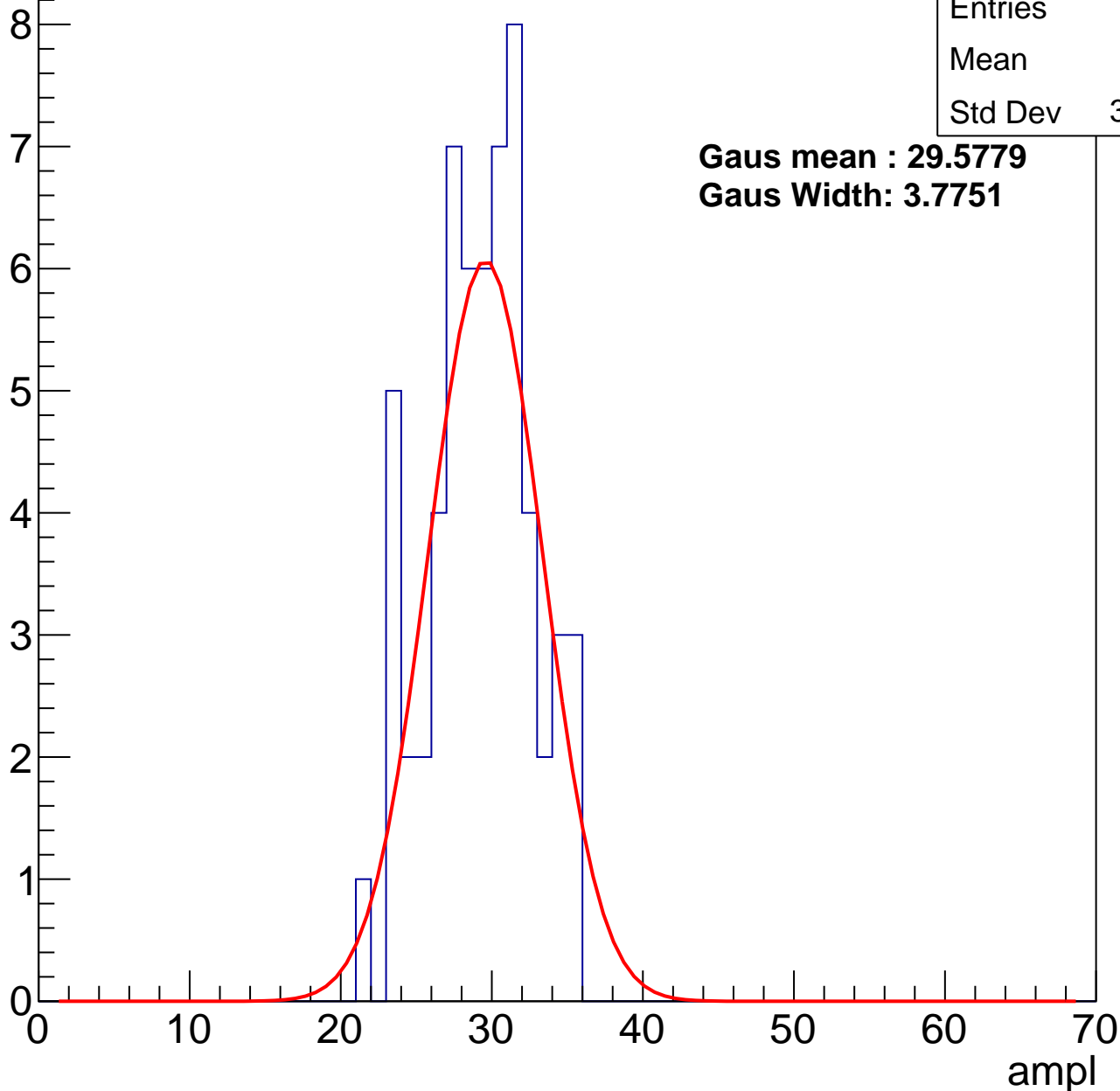
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	60
Mean	28.8
Std Dev	3.375

**Gaus mean : 29.5779**

**Gaus Width: 3.7751**



# B1L100S, U2-ch78, adc1

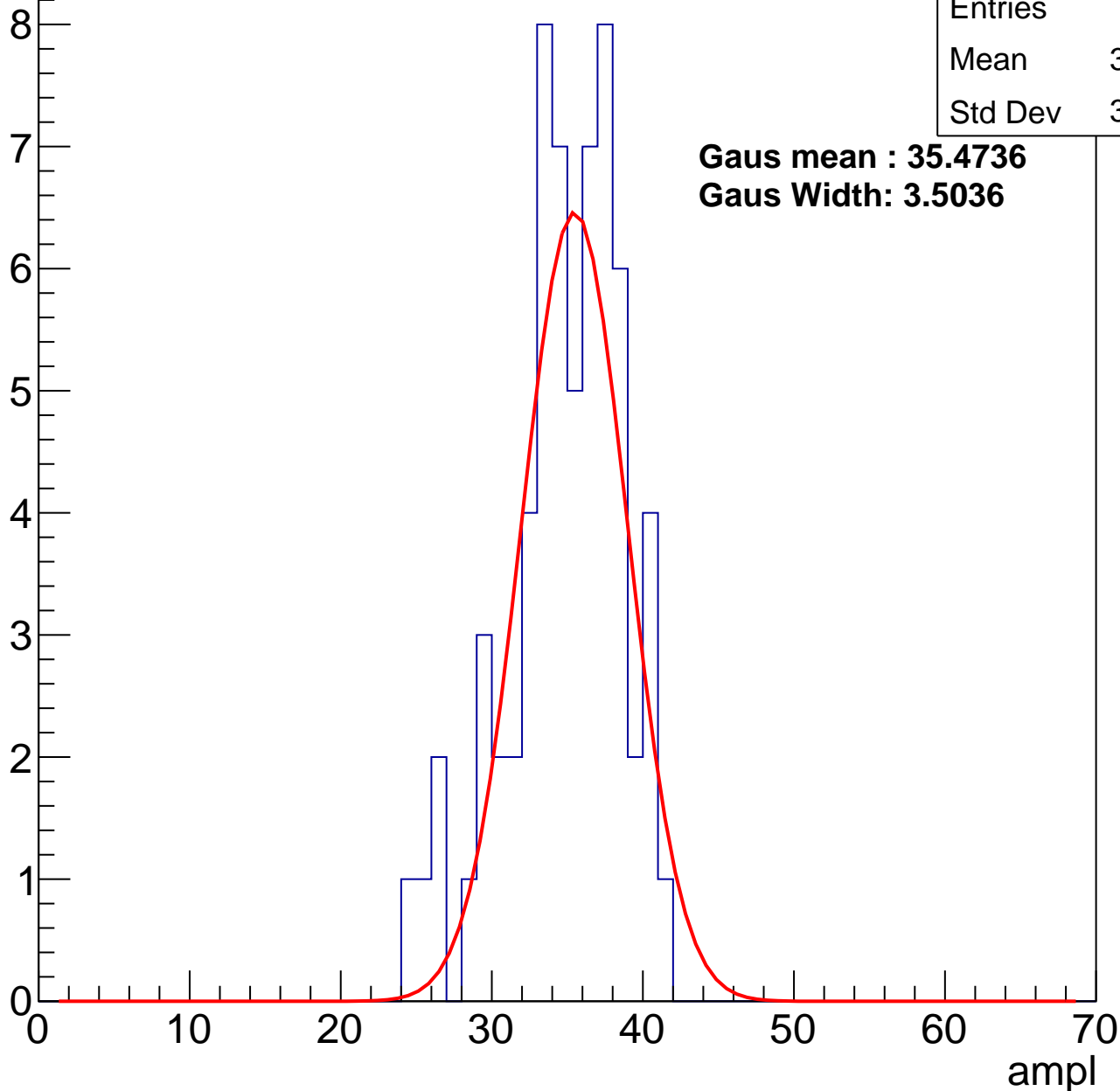
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	64
Mean	34.34
Std Dev	3.813

**Gaus mean : 35.4736**

**Gaus Width: 3.5036**



# B1L100S, U2-ch78, adc2

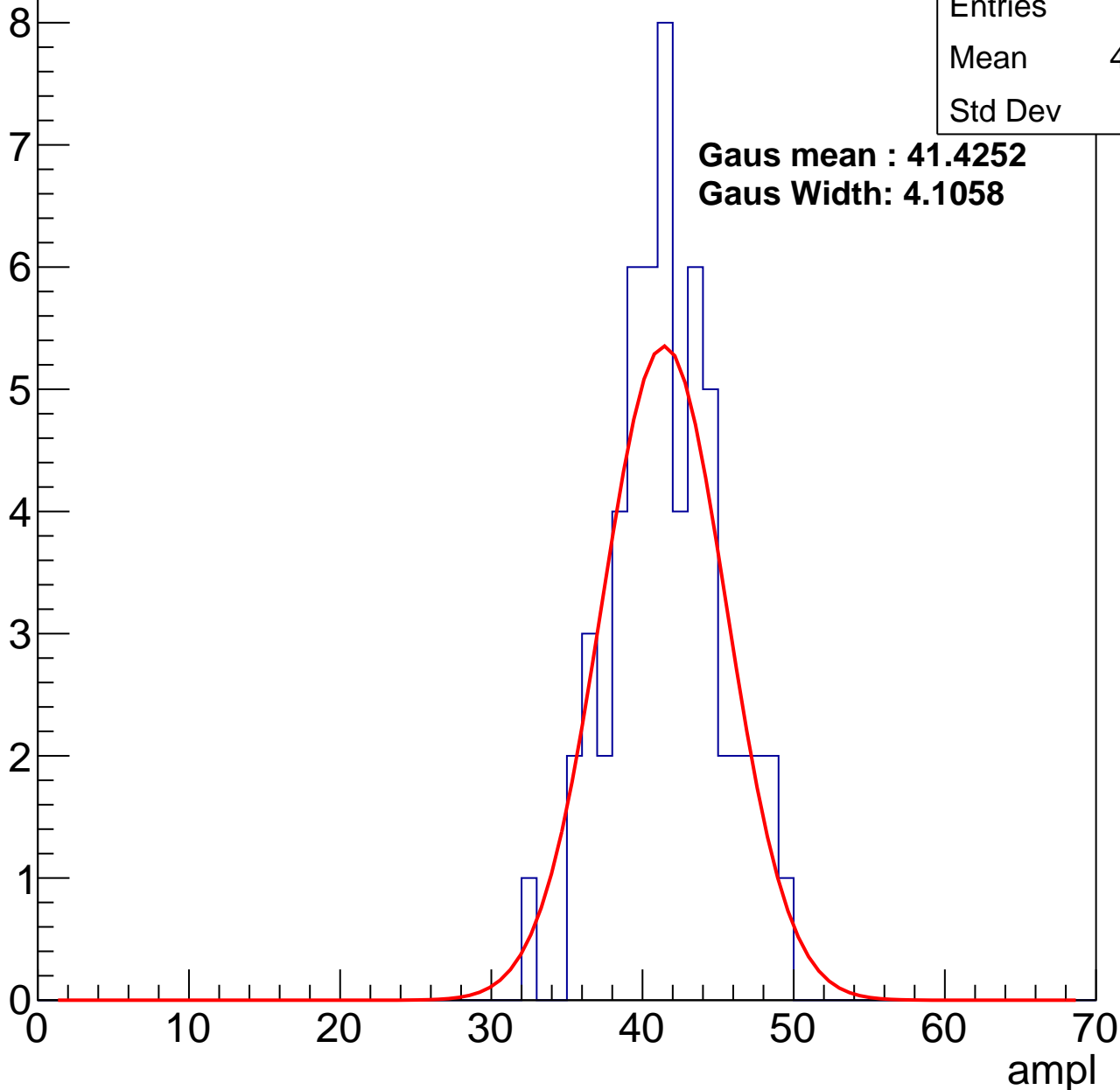
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	56
Mean	41.16
Std Dev	3.57

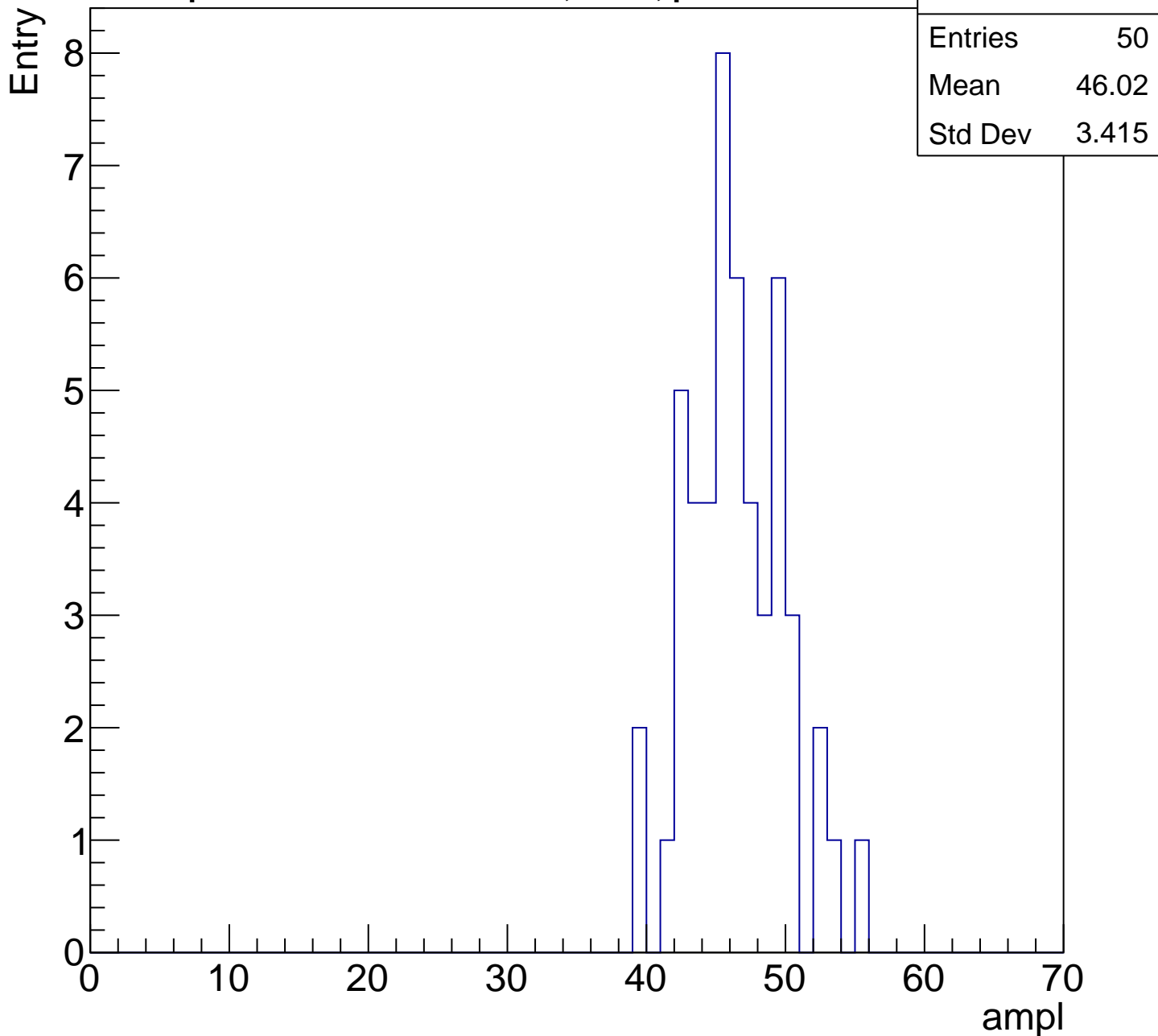
**Gaus mean : 41.4252**

**Gaus Width: 4.1058**



# B1L100S, U2-ch78, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2



# B1L100S, U2-ch78, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

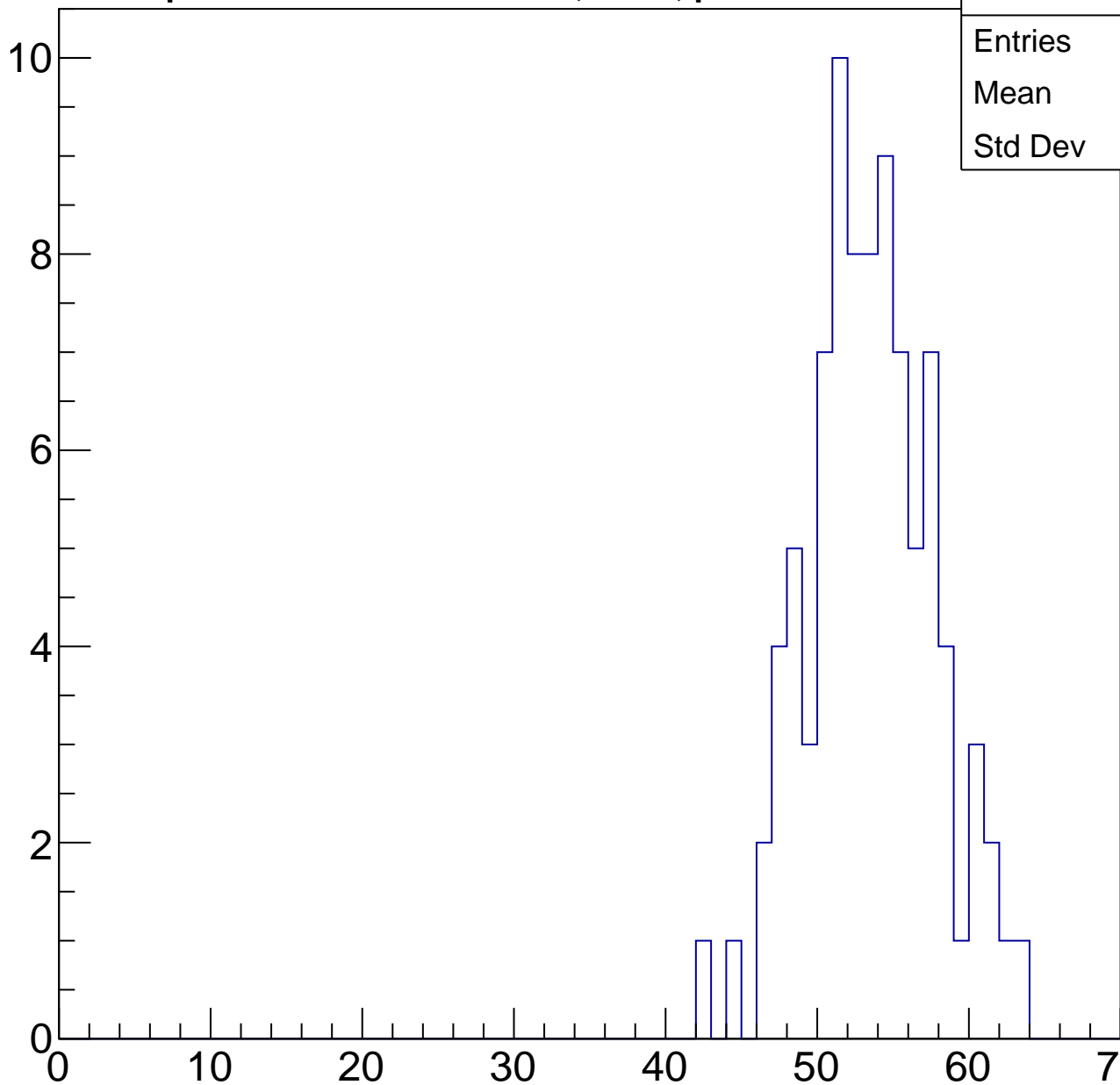
Entries	89
Mean	53.04
Std Dev	4.124

Entry

10  
8  
6  
4  
2  
0

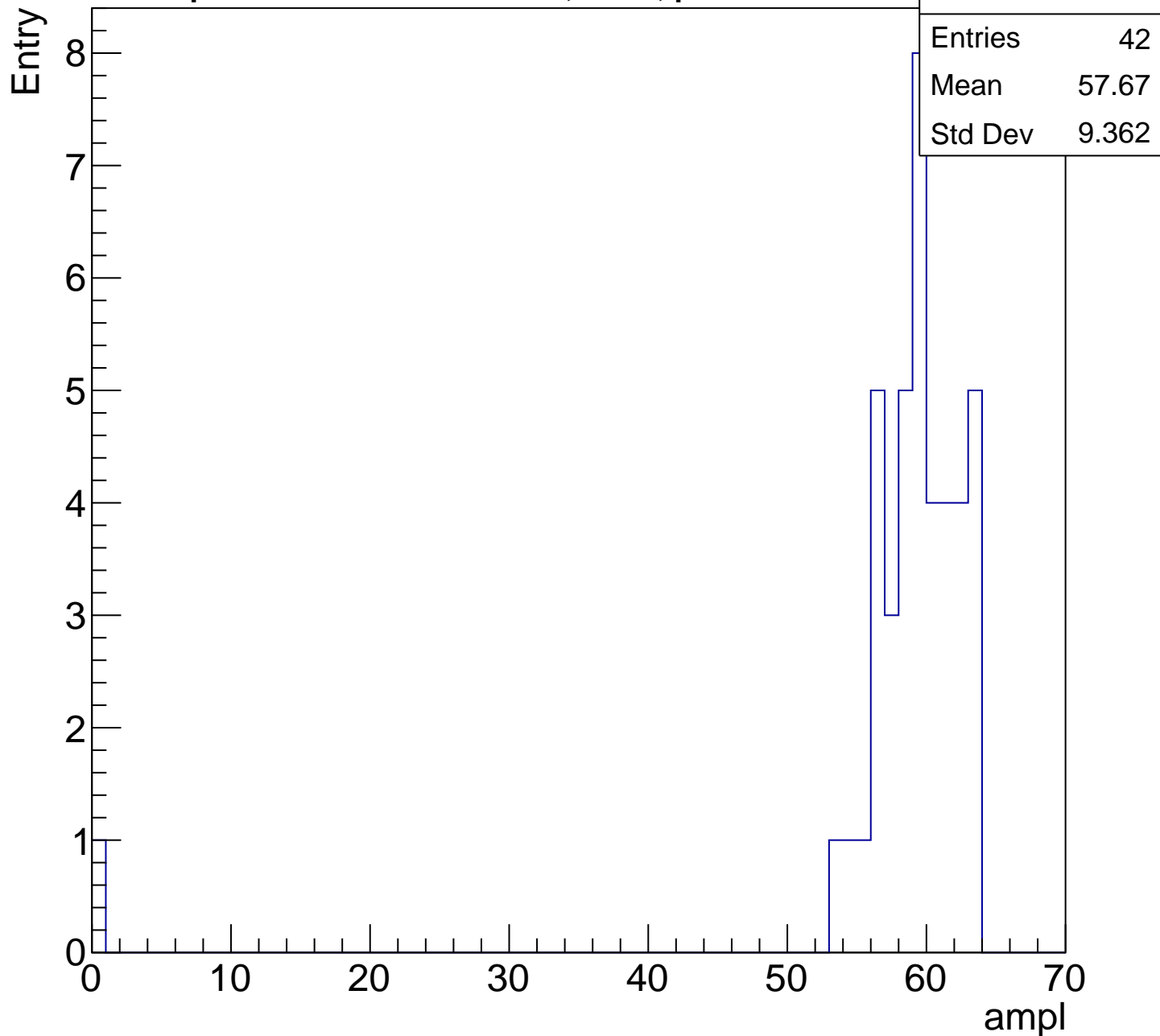
0 10 20 30 40 50 60 70

ampl



# B1L100S, U2-ch78, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

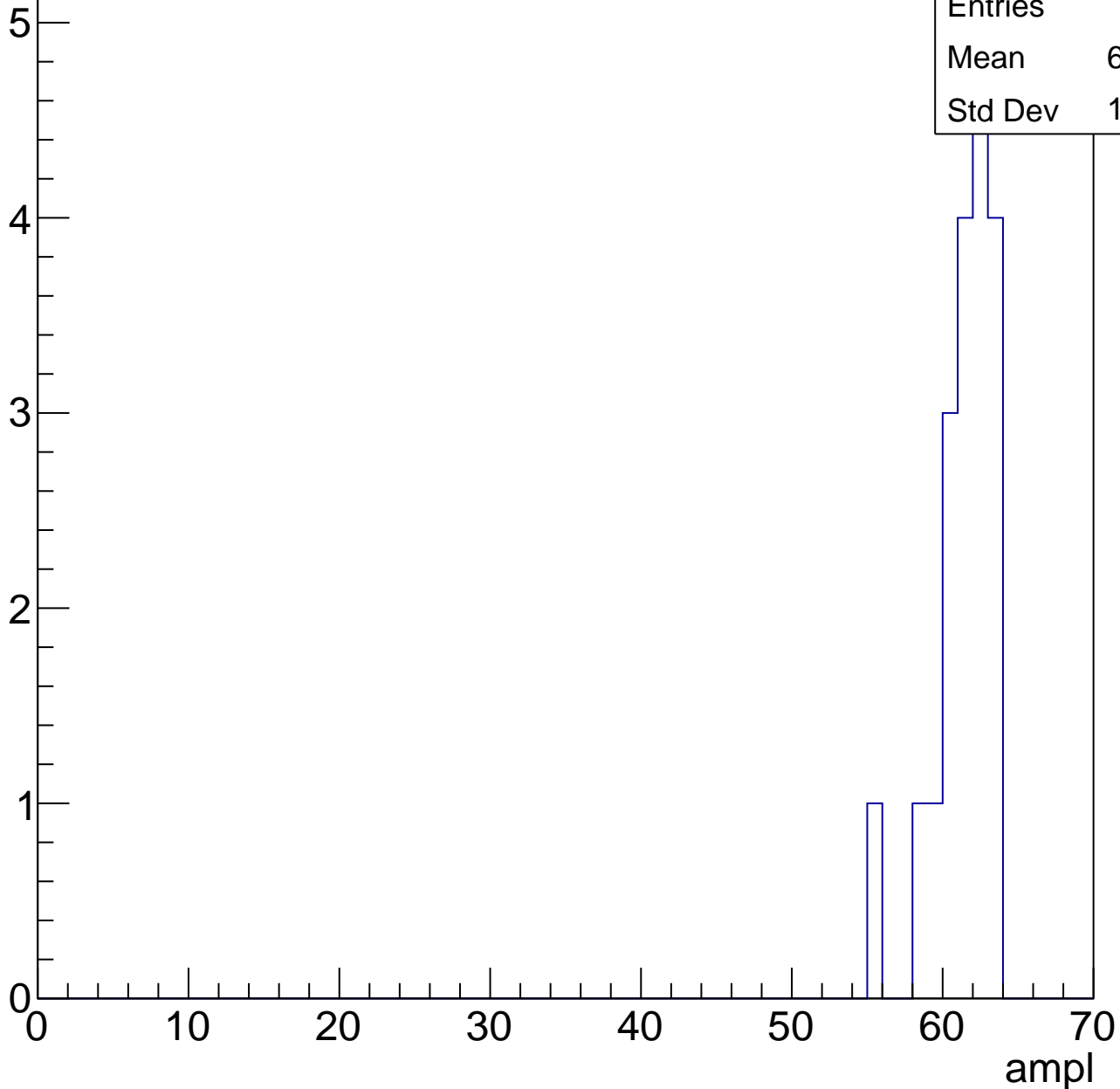


# B1L100S, U2-ch78, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	19
Mean	60.95
Std Dev	1.959





# B1L100S, U2-ch78, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



# B1L100S, U2-ch79, adc0

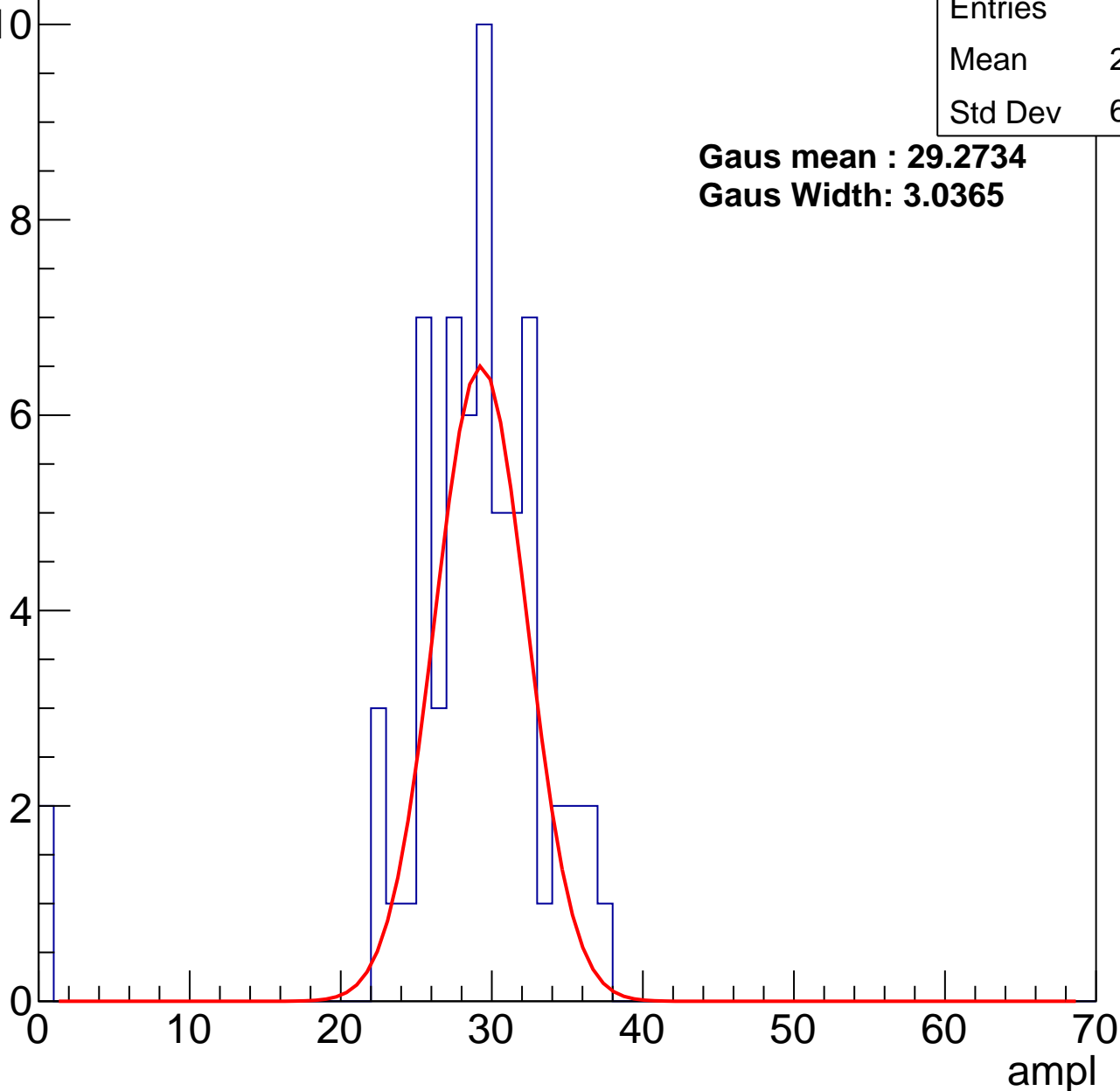
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	65
Mean	28.03
Std Dev	6.064

**Gaus mean : 29.2734**

**Gaus Width: 3.0365**



# B1L100S, U2-ch79, adc1

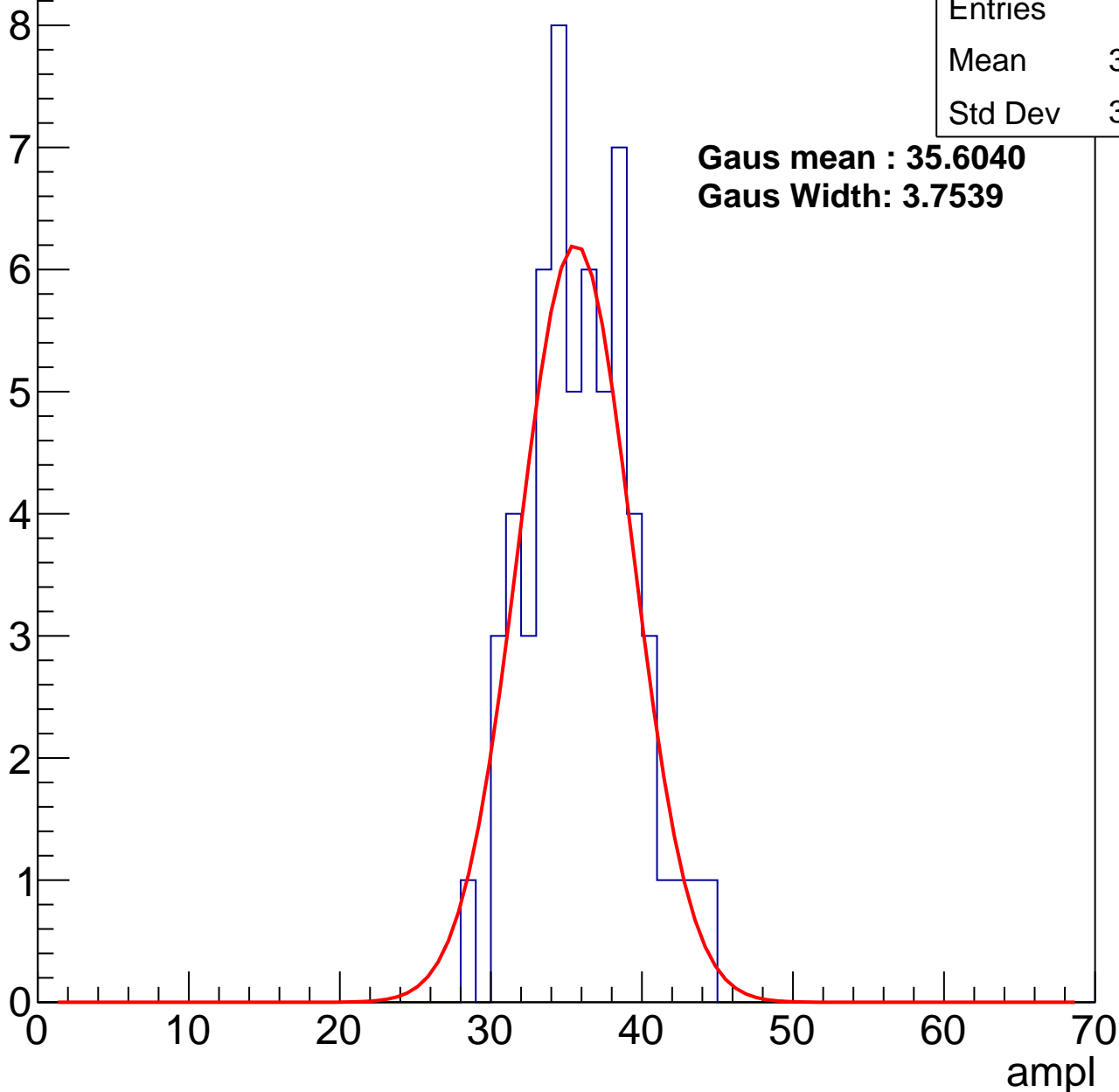
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	59
Mean	35.53
Std Dev	3.417

**Gaus mean : 35.6040**

**Gaus Width: 3.7539**



# B1L100S, U2-ch79, adc2

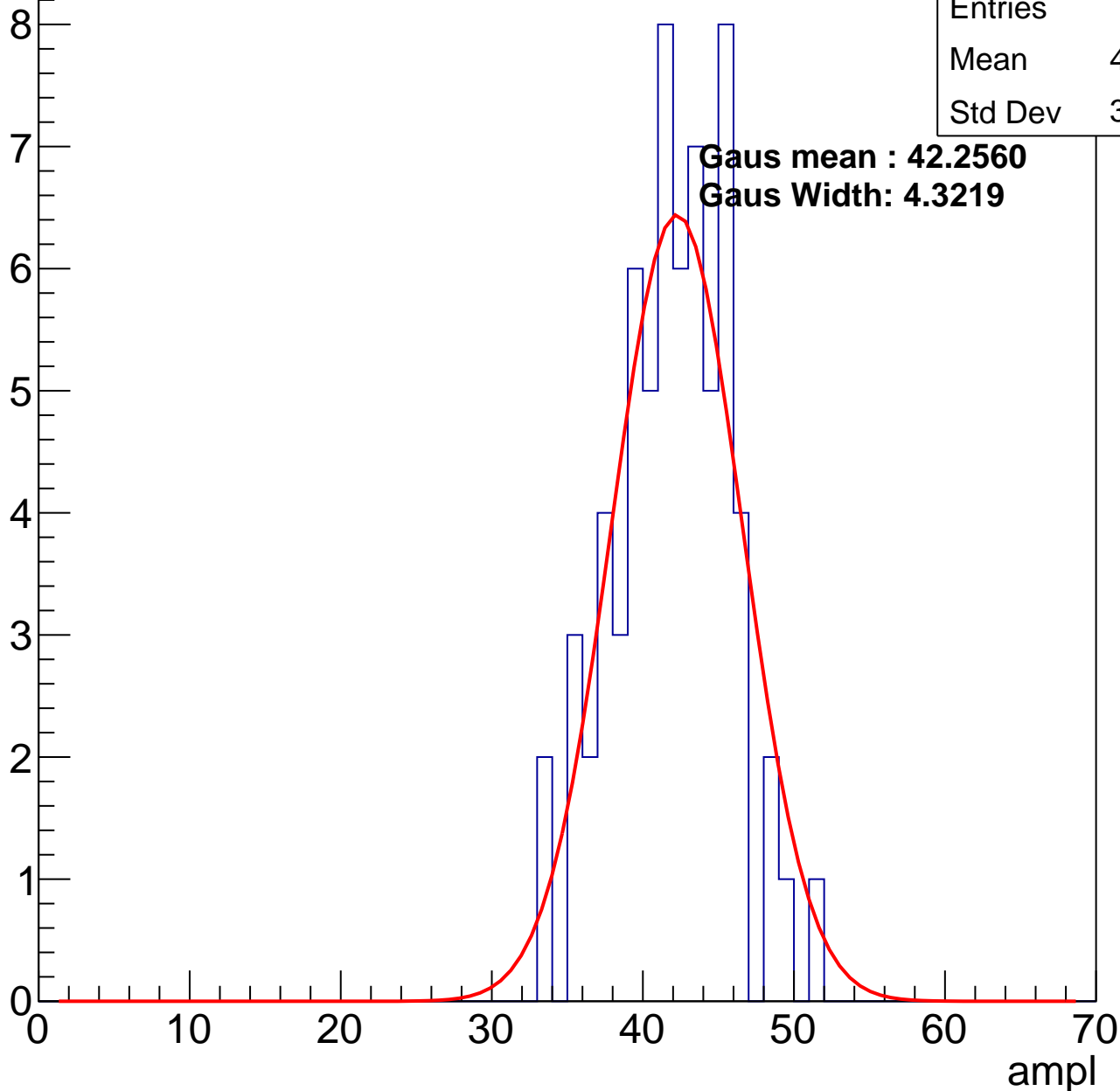
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	67
Mean	41.49
Std Dev	3.783

**Gaus mean : 42.2560**

**Gaus Width: 4.3219**



# B1L100S, U2-ch79, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

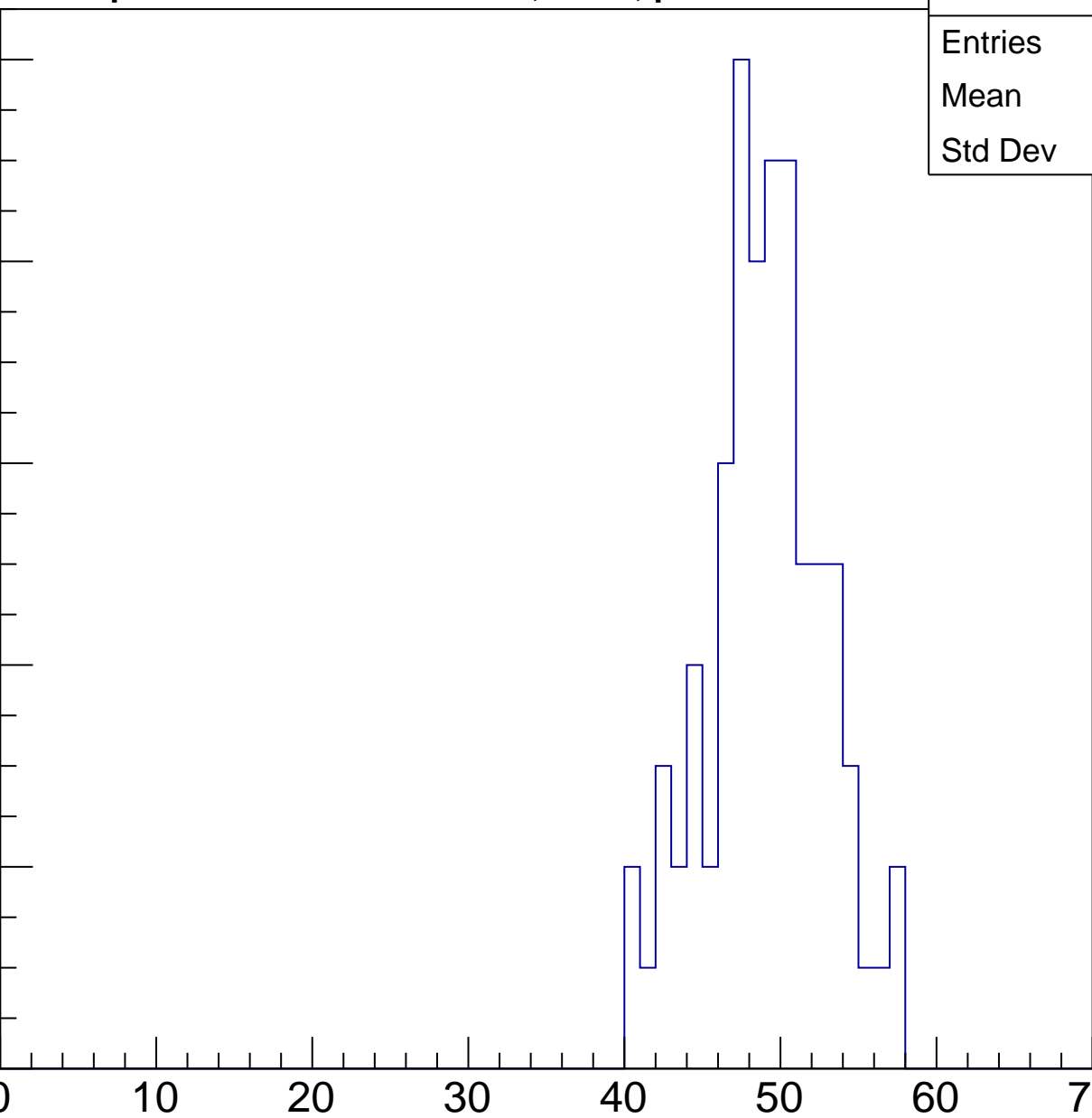
Entries	78
Mean	48.55
Std Dev	3.764

Entry

10  
8  
6  
4  
2  
0

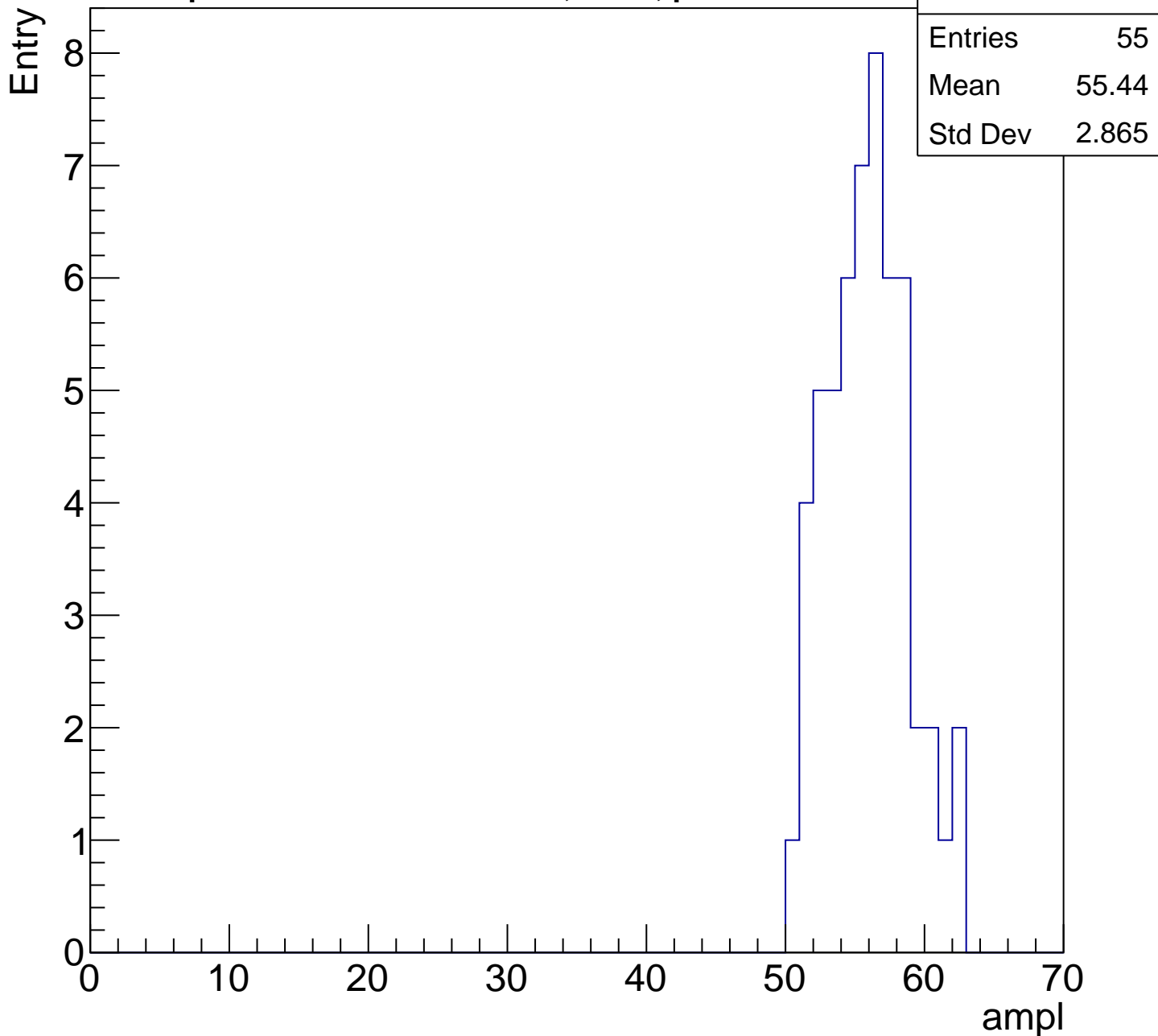
0 10 20 30 40 50 60 70

ampl



# B1L100S, U2-ch79, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

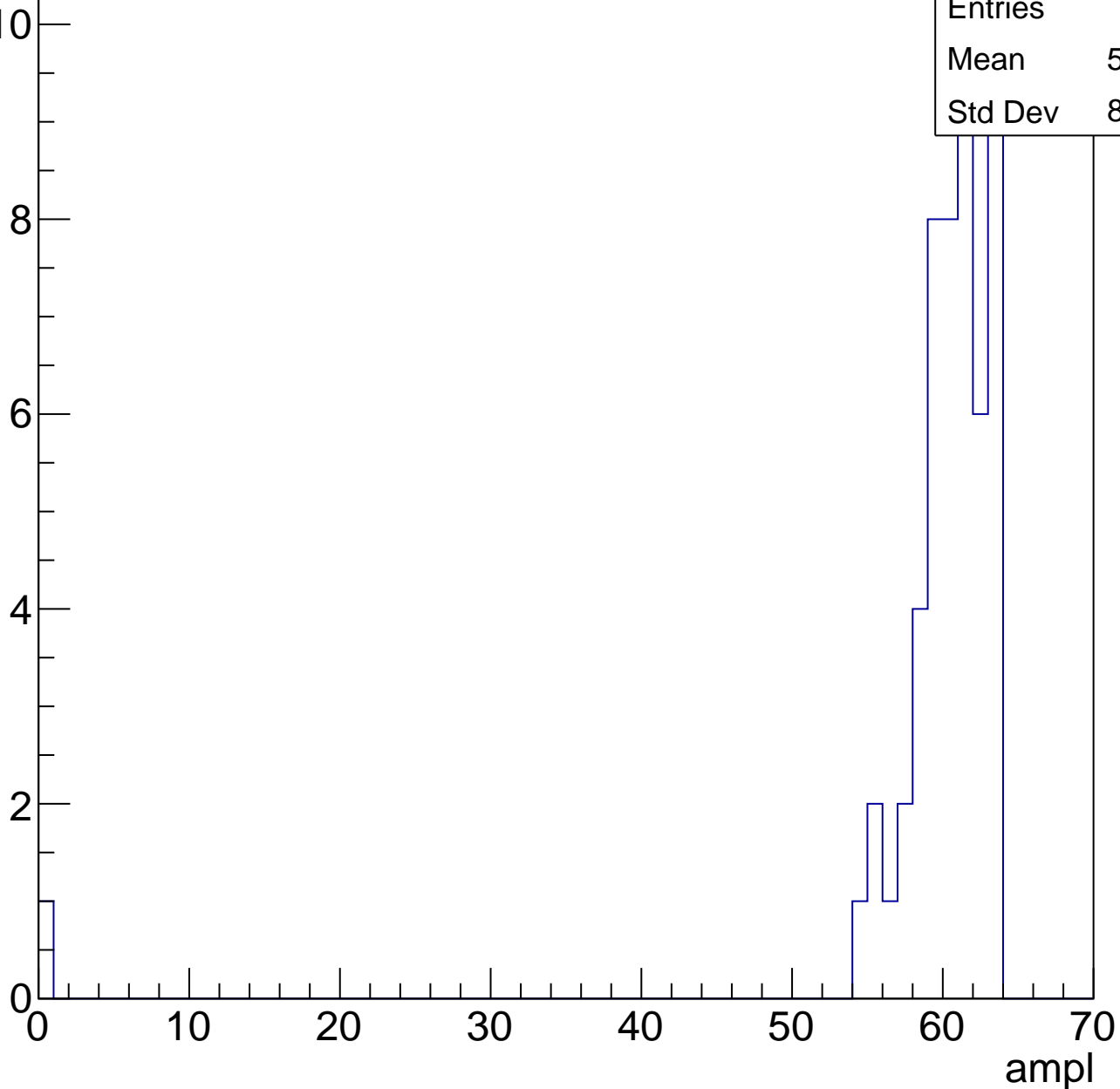


# B1L100S, U2-ch79, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	52
Mean	59.02
Std Dev	8.568



# B1L100S, U2-ch79, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry





# B1L100S, U2-ch79, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



# B1L100S, U2-ch80, adc0

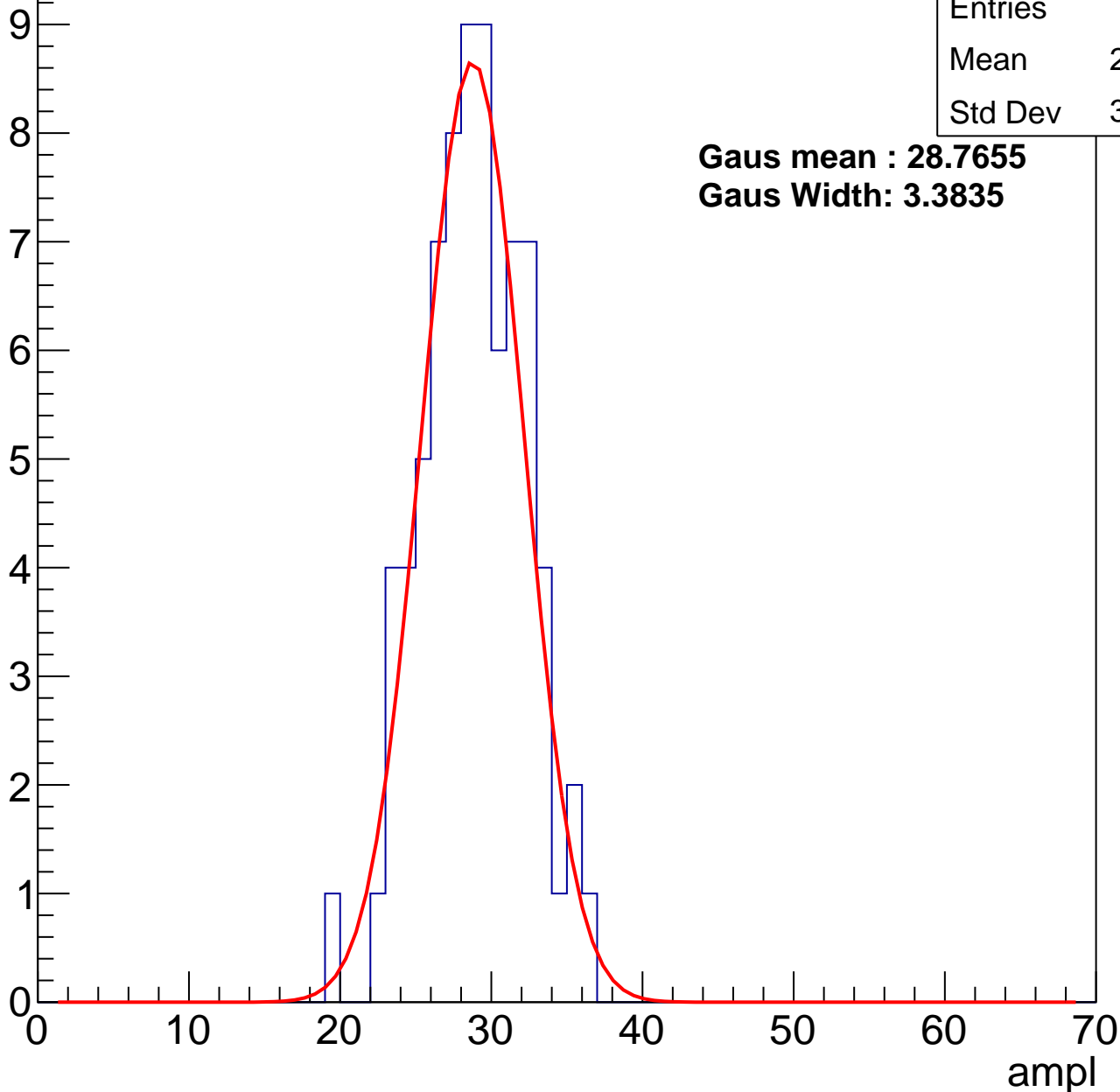
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	76
Mean	28.39
Std Dev	3.356

**Gaus mean : 28.7655**

**Gaus Width: 3.3835**



# B1L100S, U2-ch80, adc1

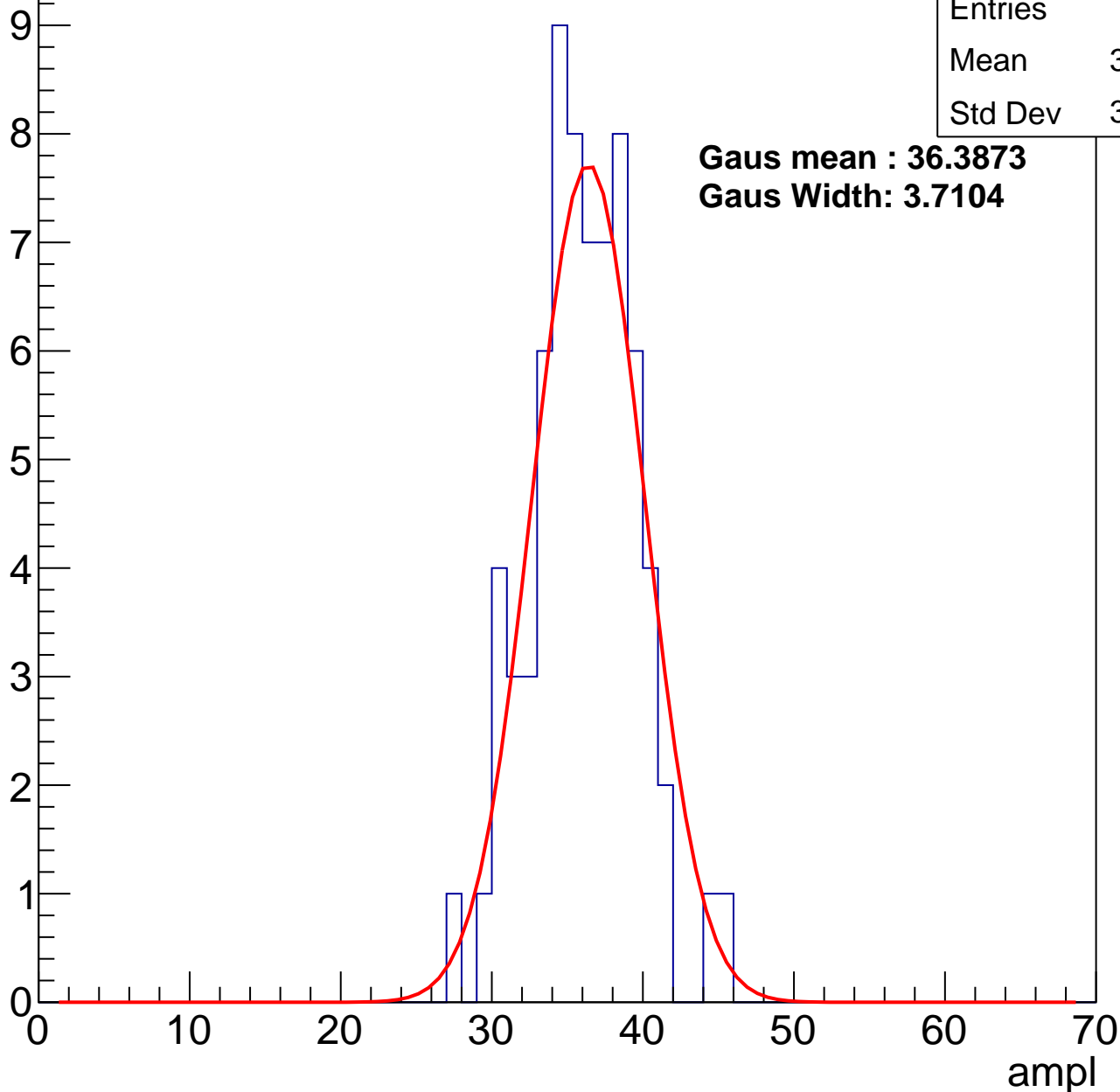
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	71
Mean	35.62
Std Dev	3.433

**Gaus mean : 36.3873**

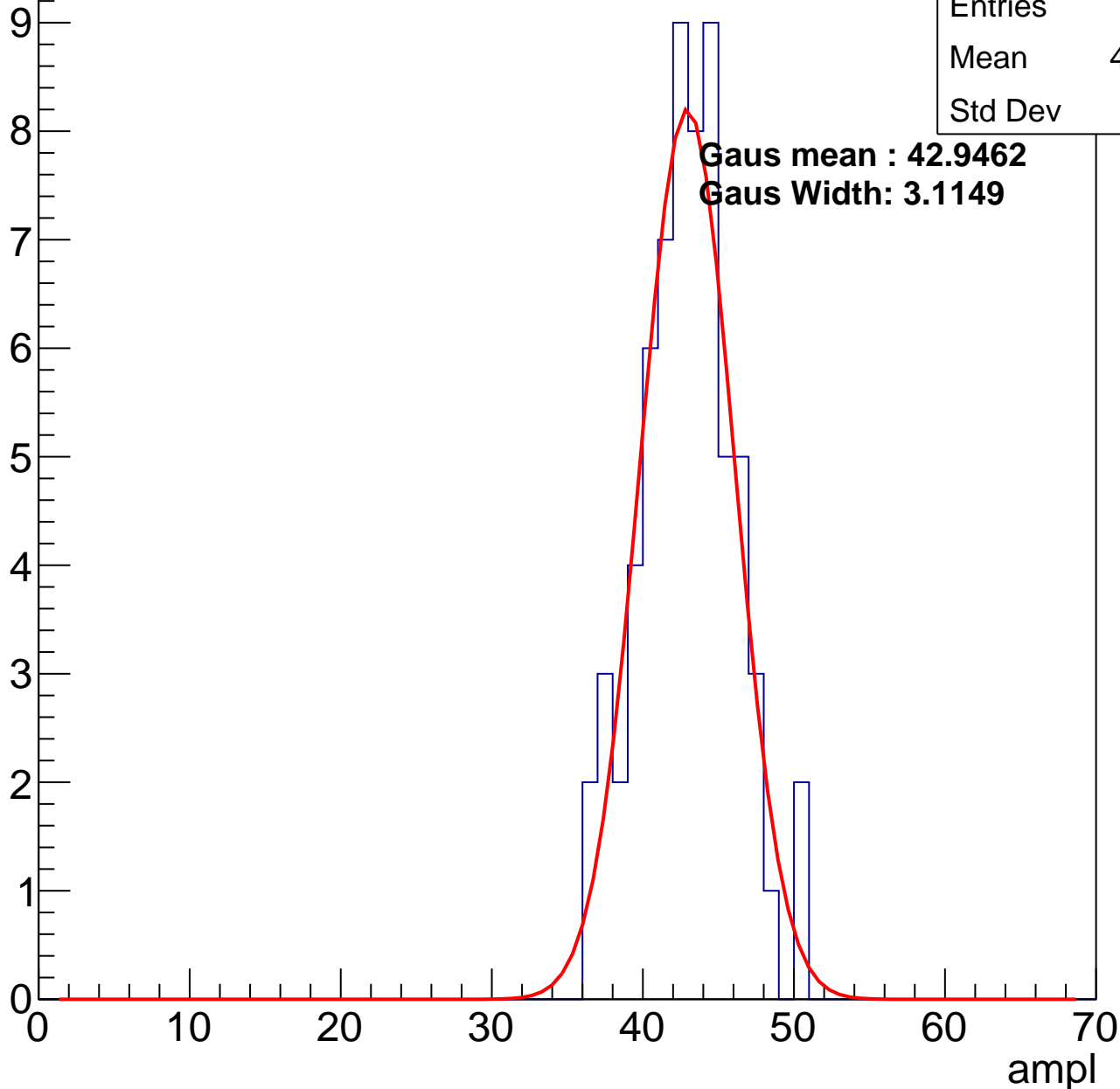
**Gaus Width: 3.7104**



# B1L100S, U2-ch80, adc2

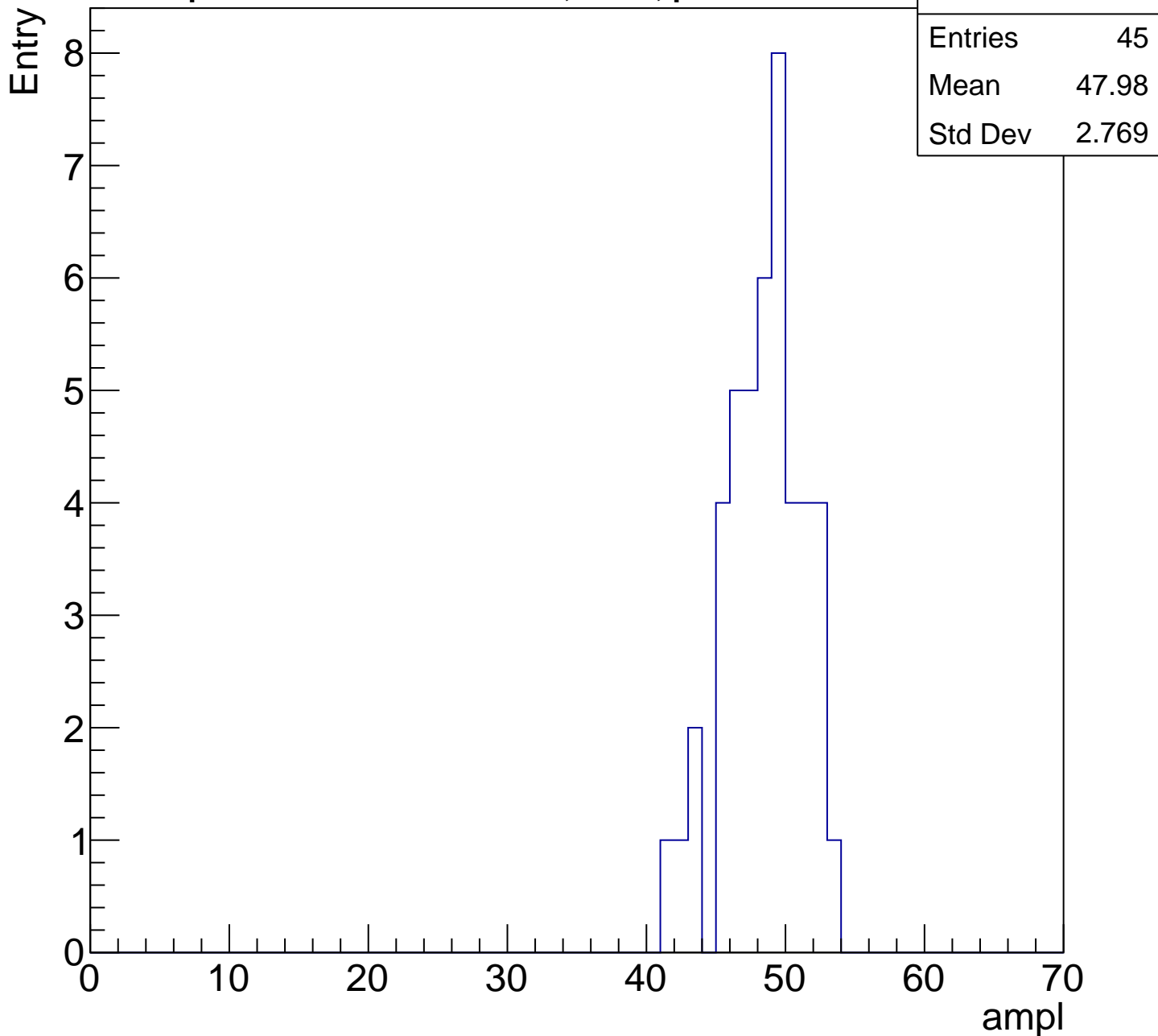
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



# B1L100S, U2-ch80, adc3

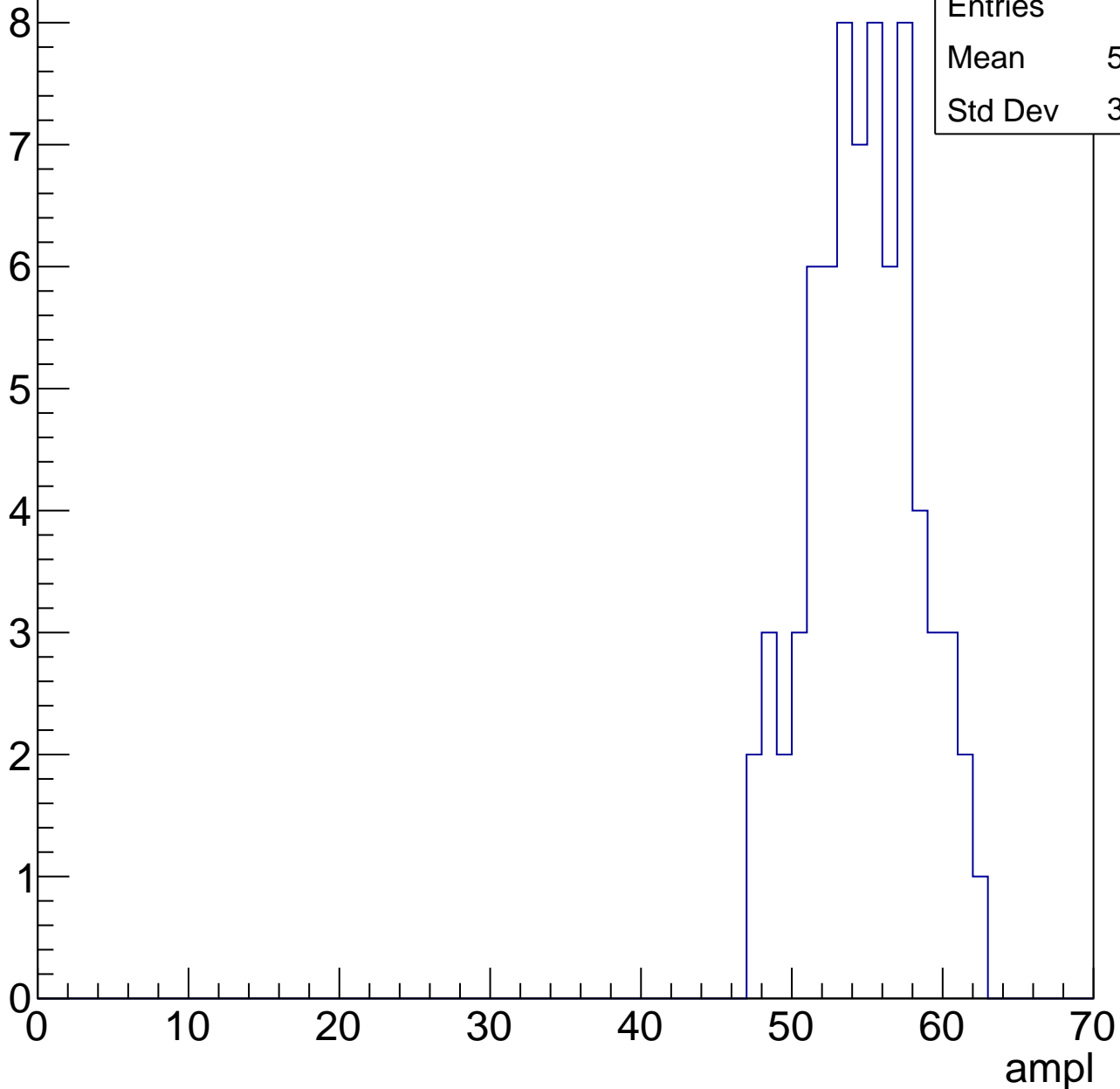
calib\_packv5\_042523\_0143.root, FC#4, port A2



# B1L100S, U2-ch80, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

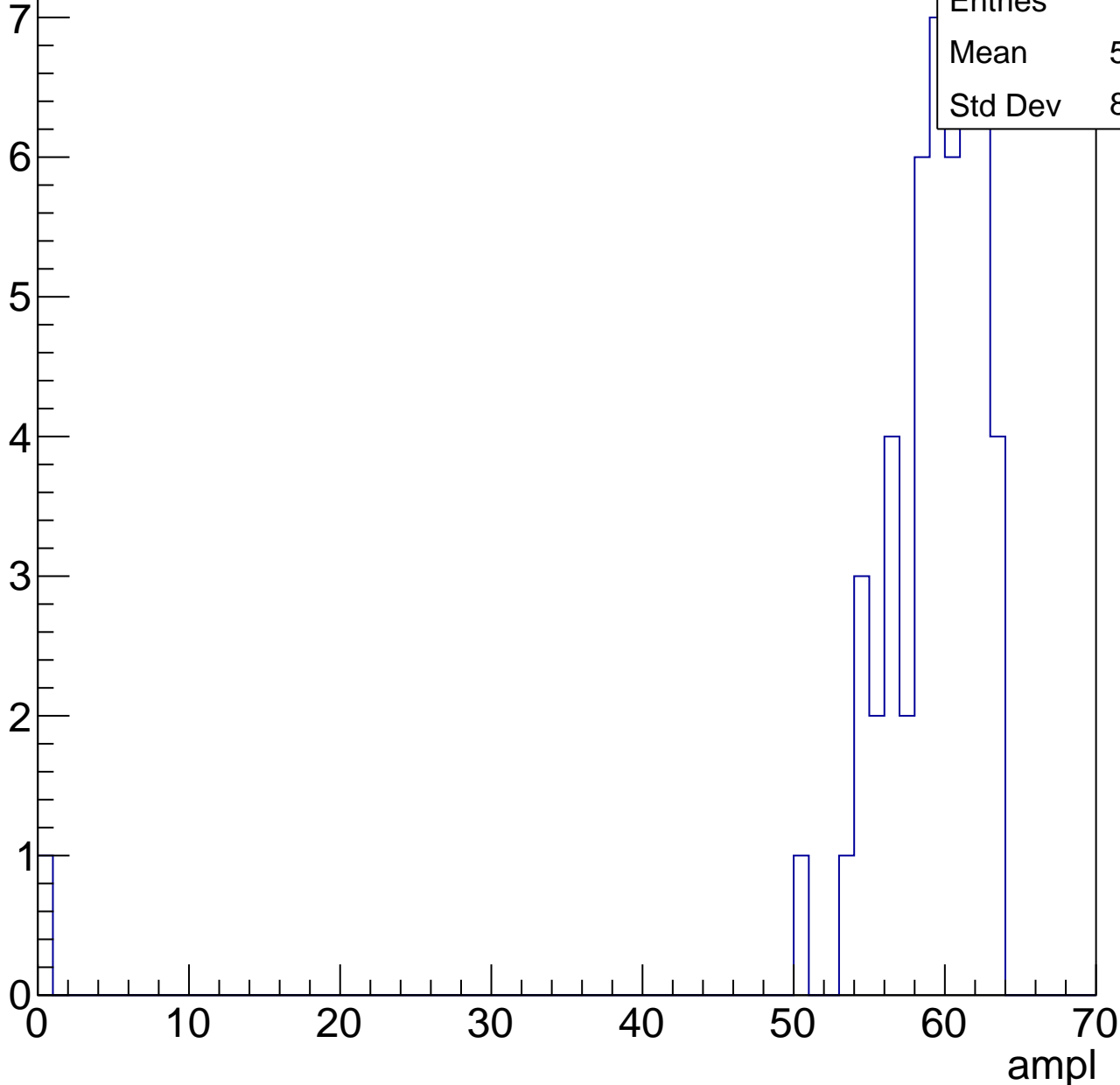


# B1L100S, U2-ch80, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	51
Mean	57.78
Std Dev	8.678

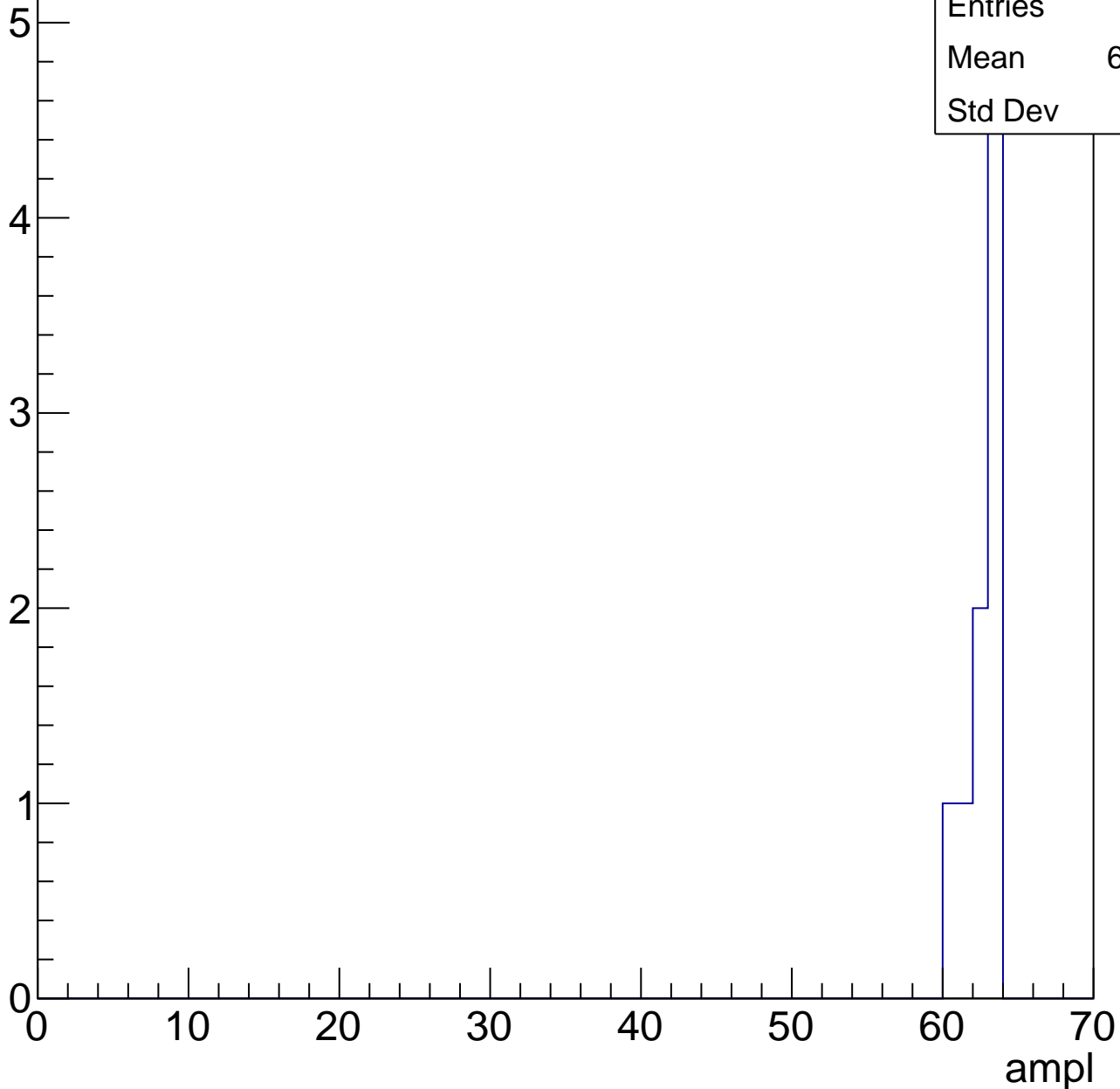


# B1L100S, U2-ch80, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	9
Mean	62.22
Std Dev	1.03





# B1L100S, U2-ch80, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



# B1L100S, U2-ch81, adc0

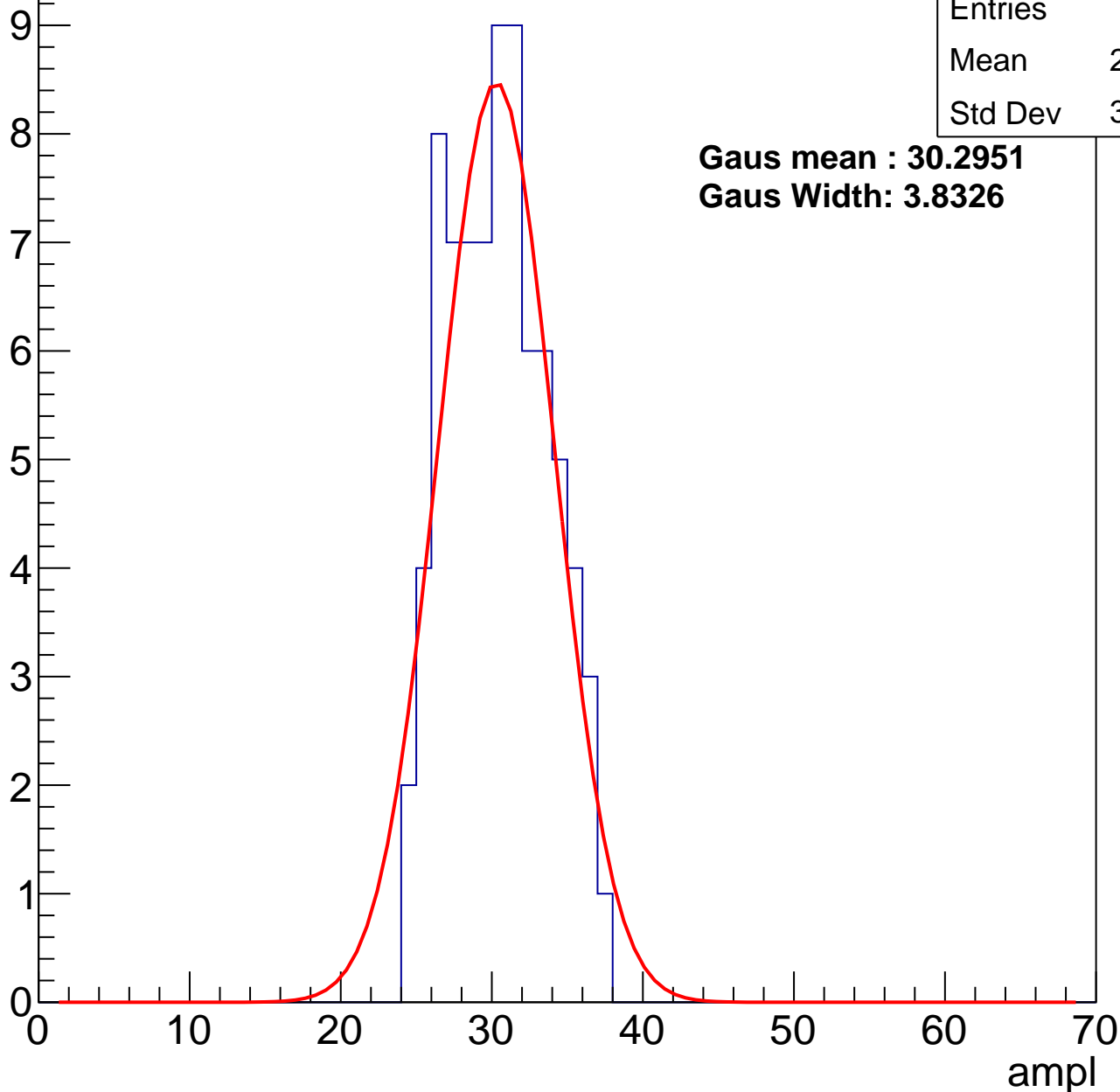
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	78
Mean	29.97
Std Dev	3.246

**Gaus mean : 30.2951**

**Gaus Width: 3.8326**



# B1L100S, U2-ch81, adc1

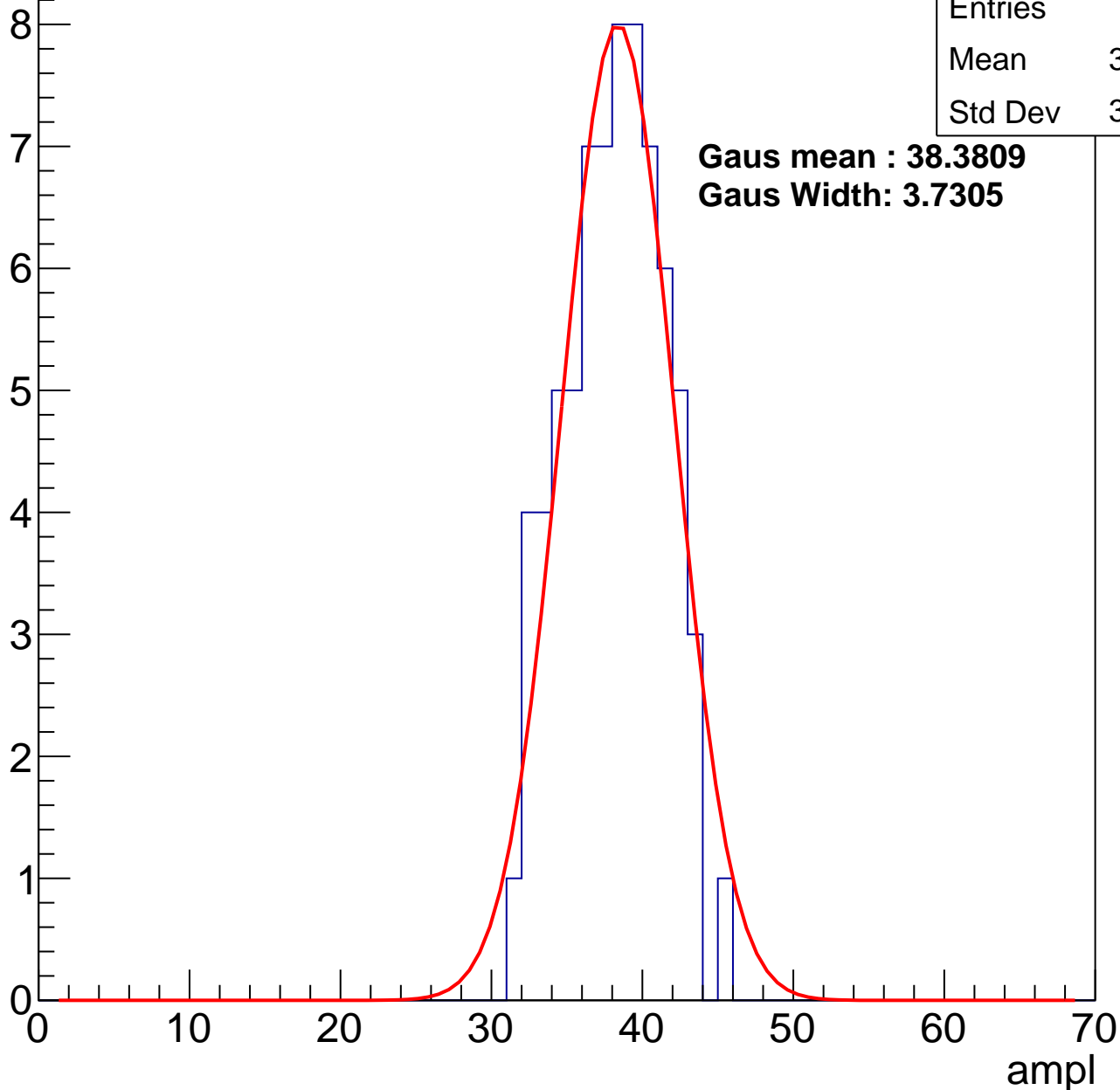
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	71
Mean	37.65
Std Dev	3.224

**Gaus mean : 38.3809**

**Gaus Width: 3.7305**



# B1L100S, U2-ch81, adc2

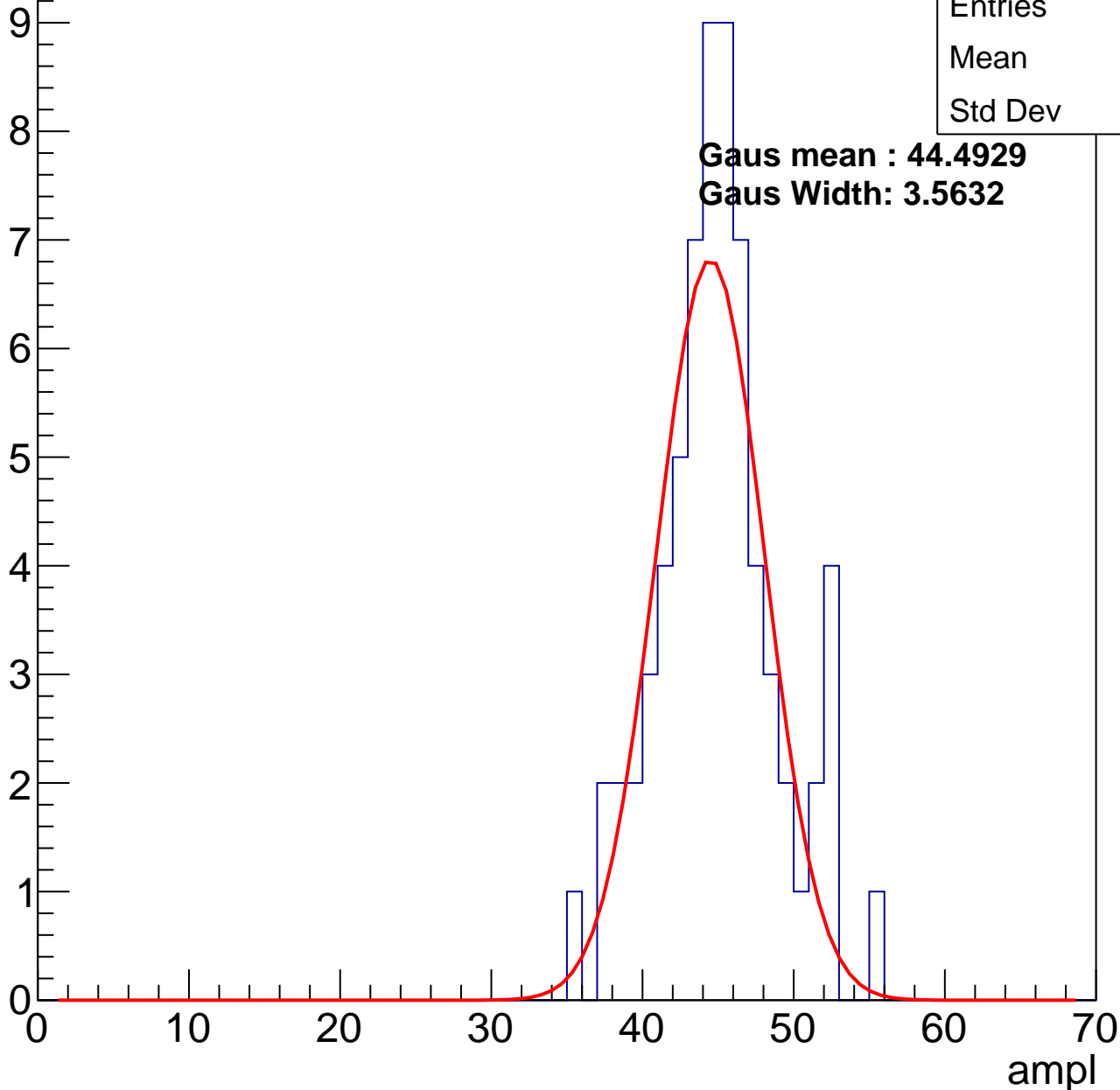
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	68
Mean	44.5
Std Dev	3.98

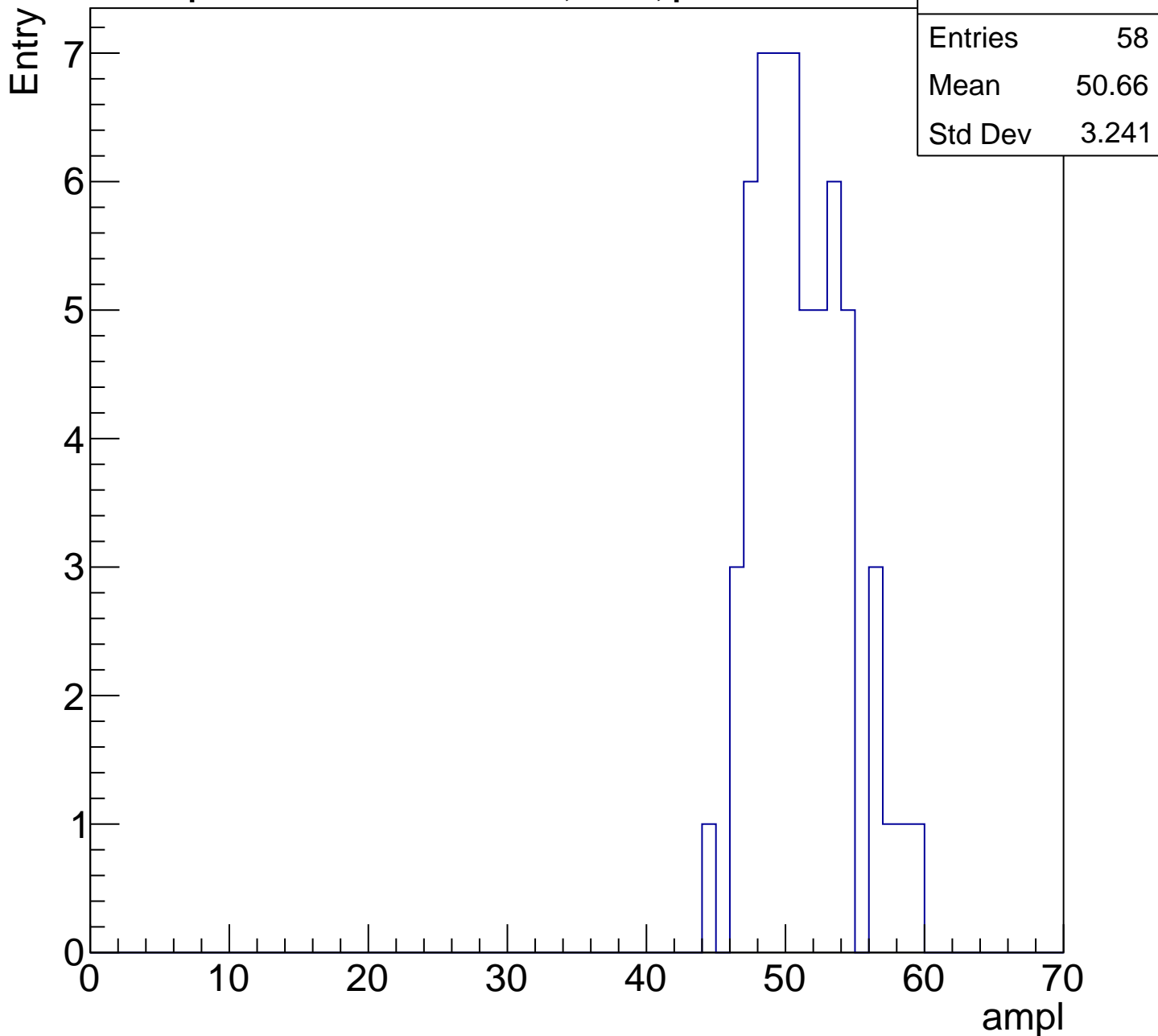
**Gaus mean : 44.4929**

**Gaus Width: 3.5632**



# B1L100S, U2-ch81, adc3

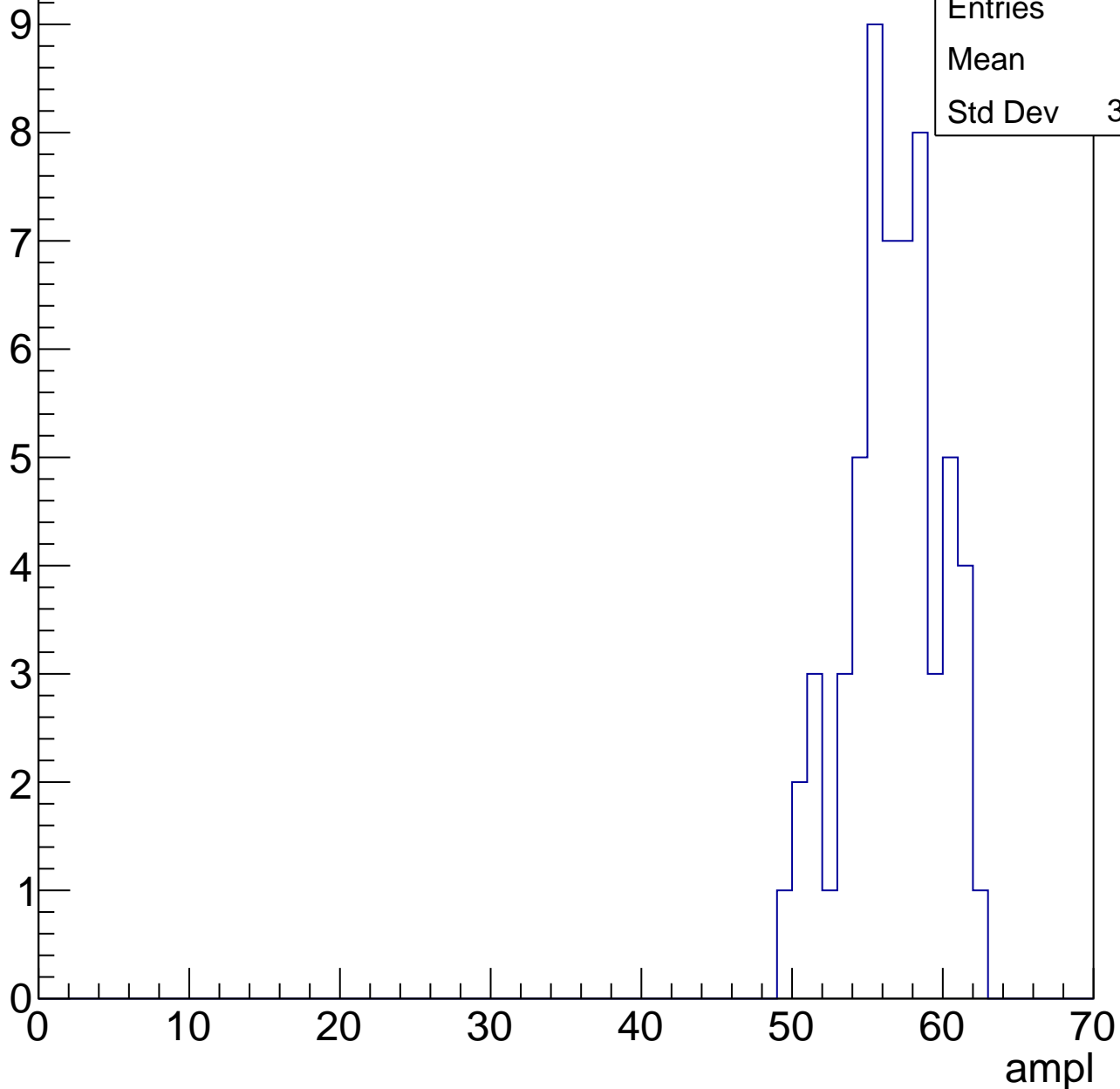
calib\_packv5\_042523\_0143.root, FC#4, port A2



# B1L100S, U2-ch81, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



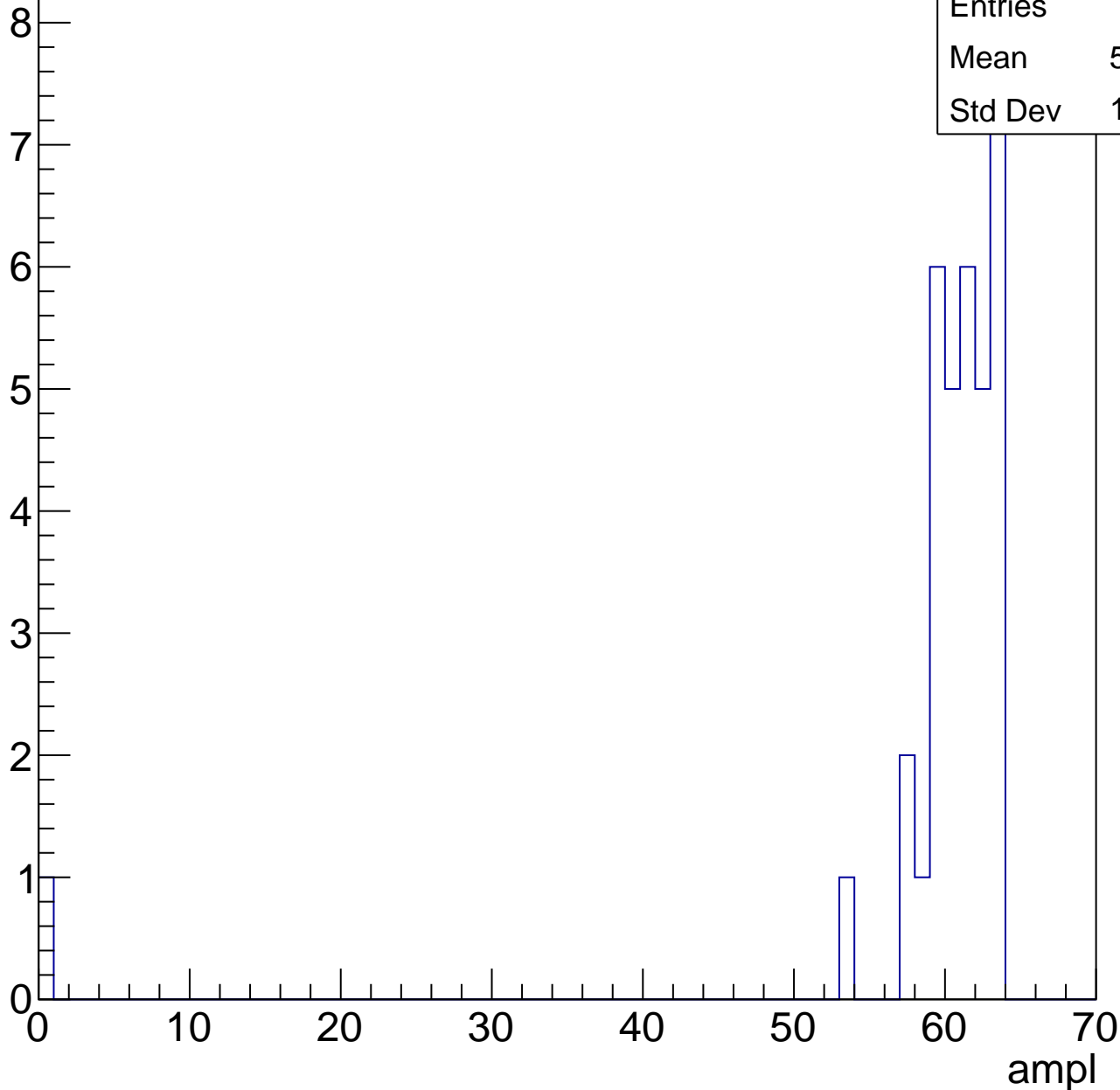
Entries	59
Mean	56.2
Std Dev	3.046

# B1L100S, U2-ch81, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

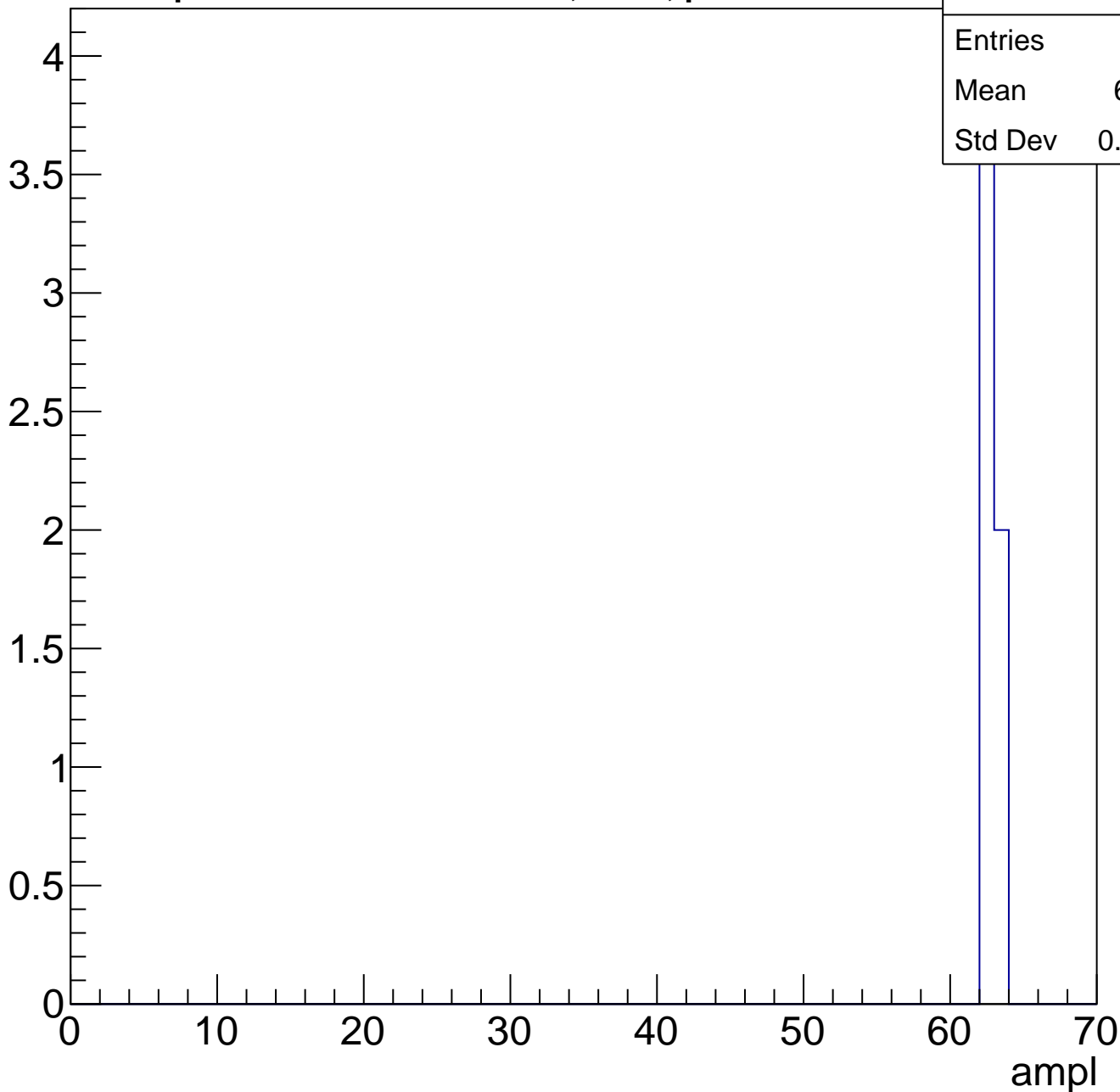
Entries	35
Mean	58.83
Std Dev	10.32



# B1L100S, U2-ch81, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry





# B1L100S, U2-ch81, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L100S, U2-ch82, adc0

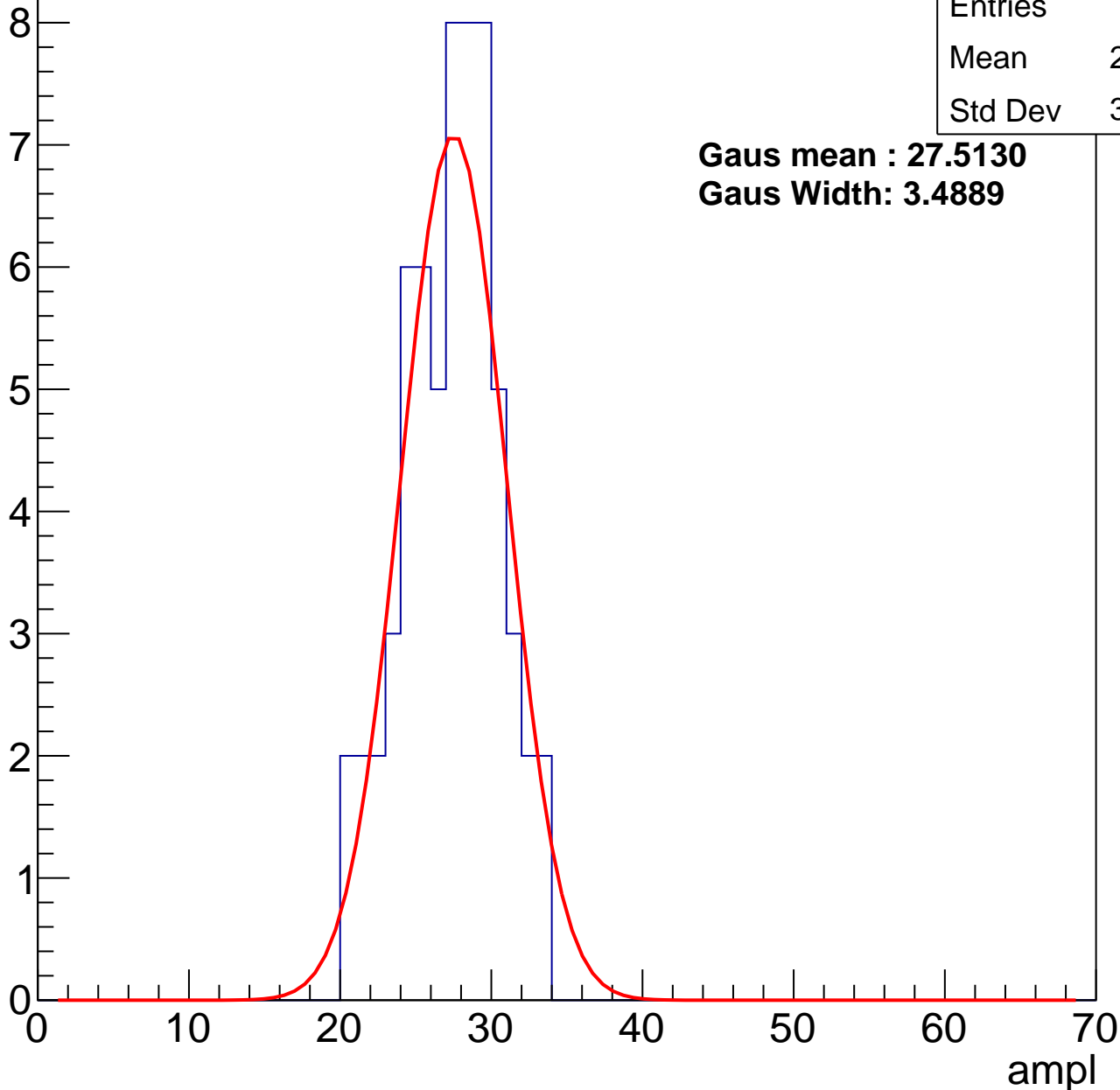
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	62
Mean	26.84
Std Dev	3.122

**Gaus mean : 27.5130**

**Gaus Width: 3.4889**



# B1L100S, U2-ch82, adc1

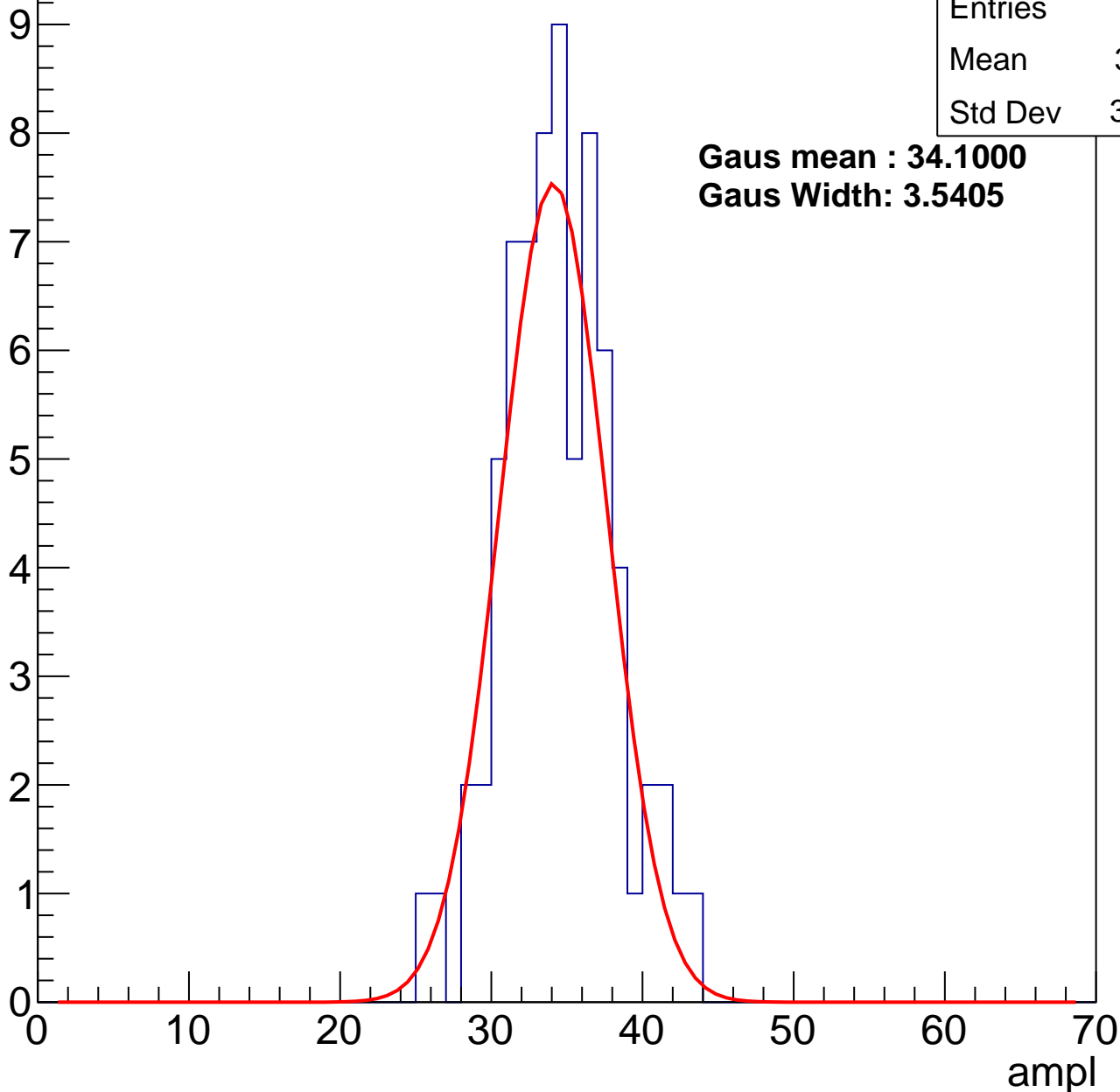
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	72
Mean	34.01
Std Dev	3.615

**Gaus mean : 34.1000**

**Gaus Width: 3.5405**



# B1L100S, U2-ch82, adc2

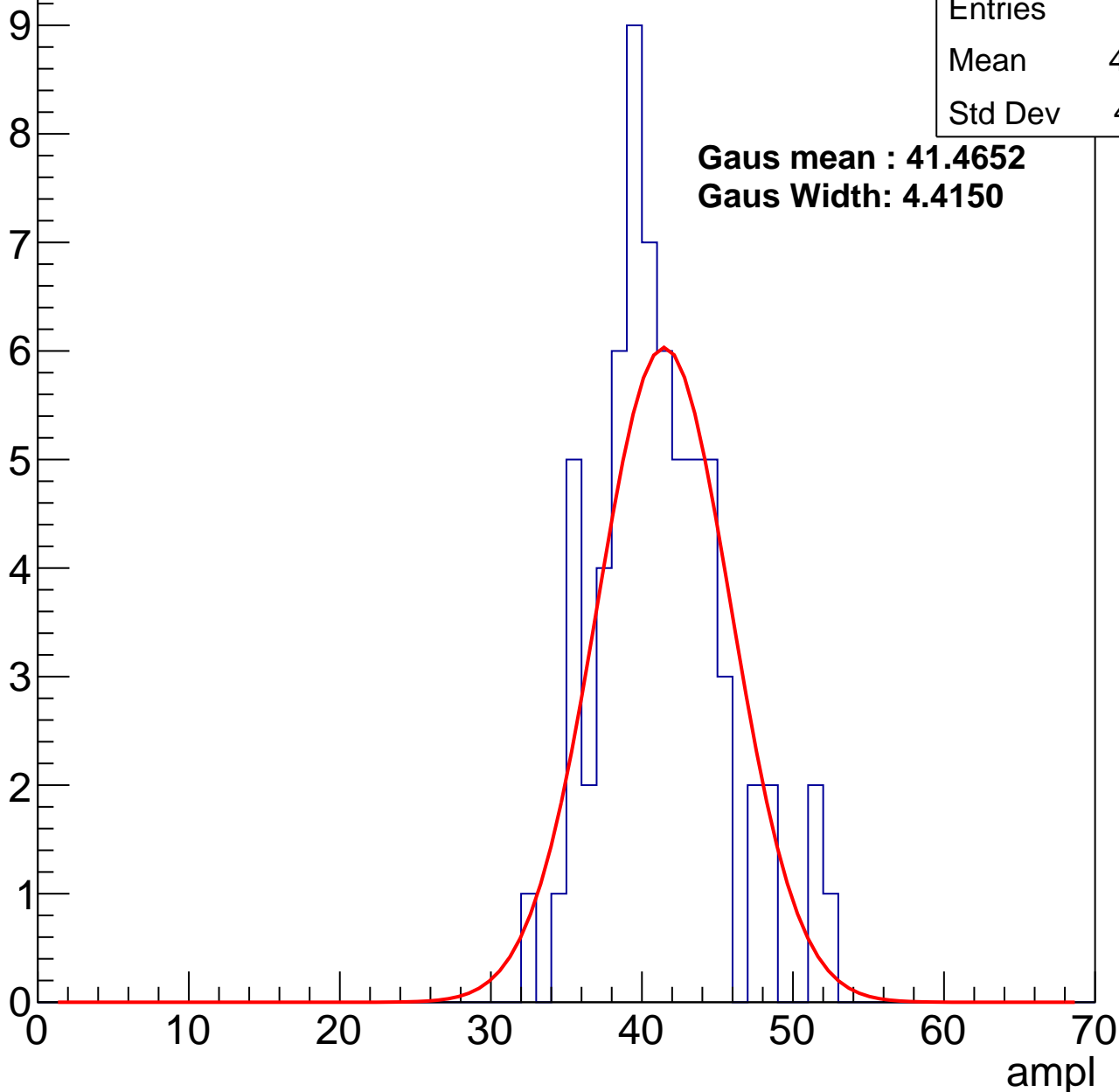
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	66
Mean	40.76
Std Dev	4.131

**Gaus mean : 41.4652**

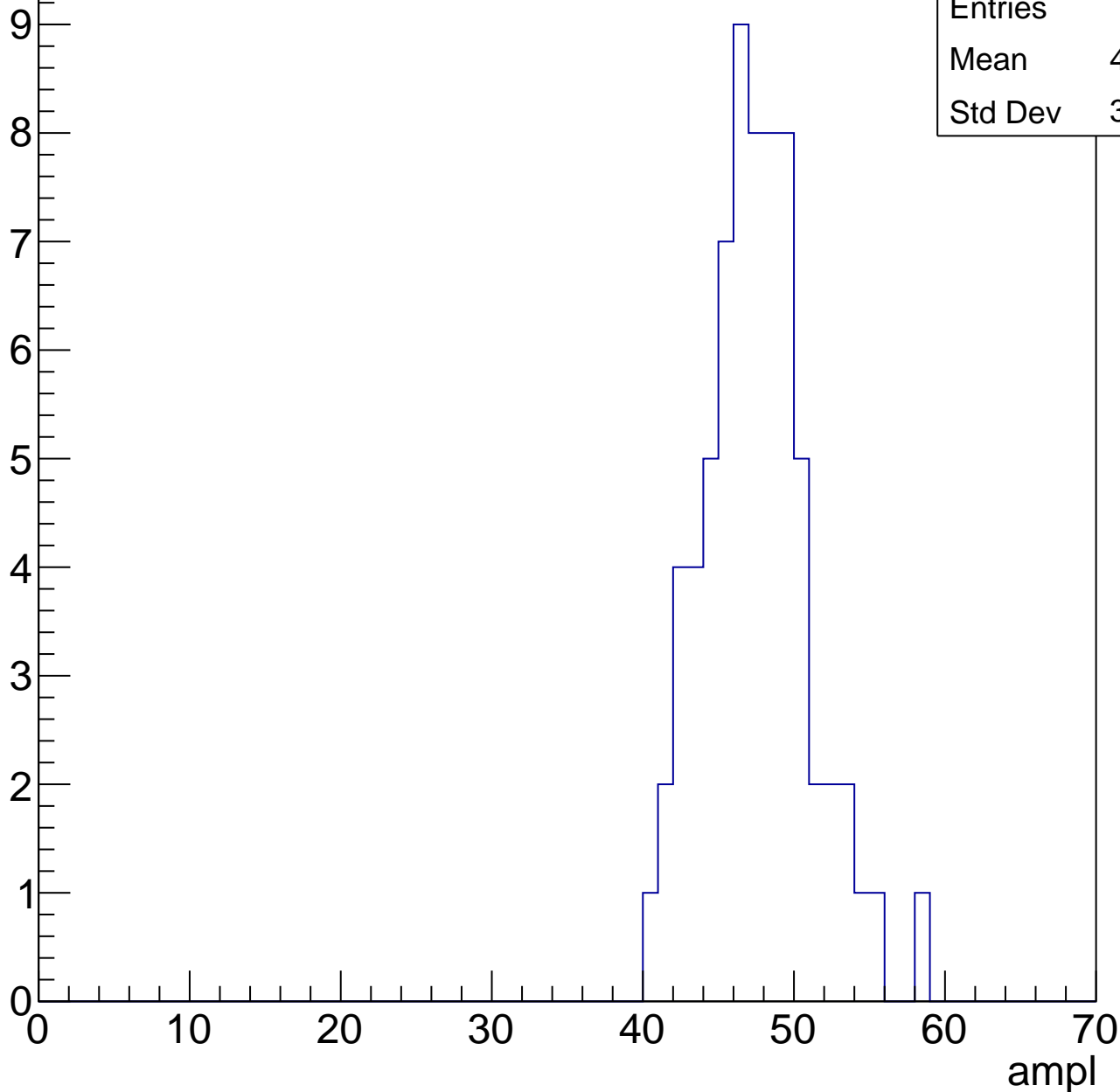
**Gaus Width: 4.4150**



# B1L100S, U2-ch82, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

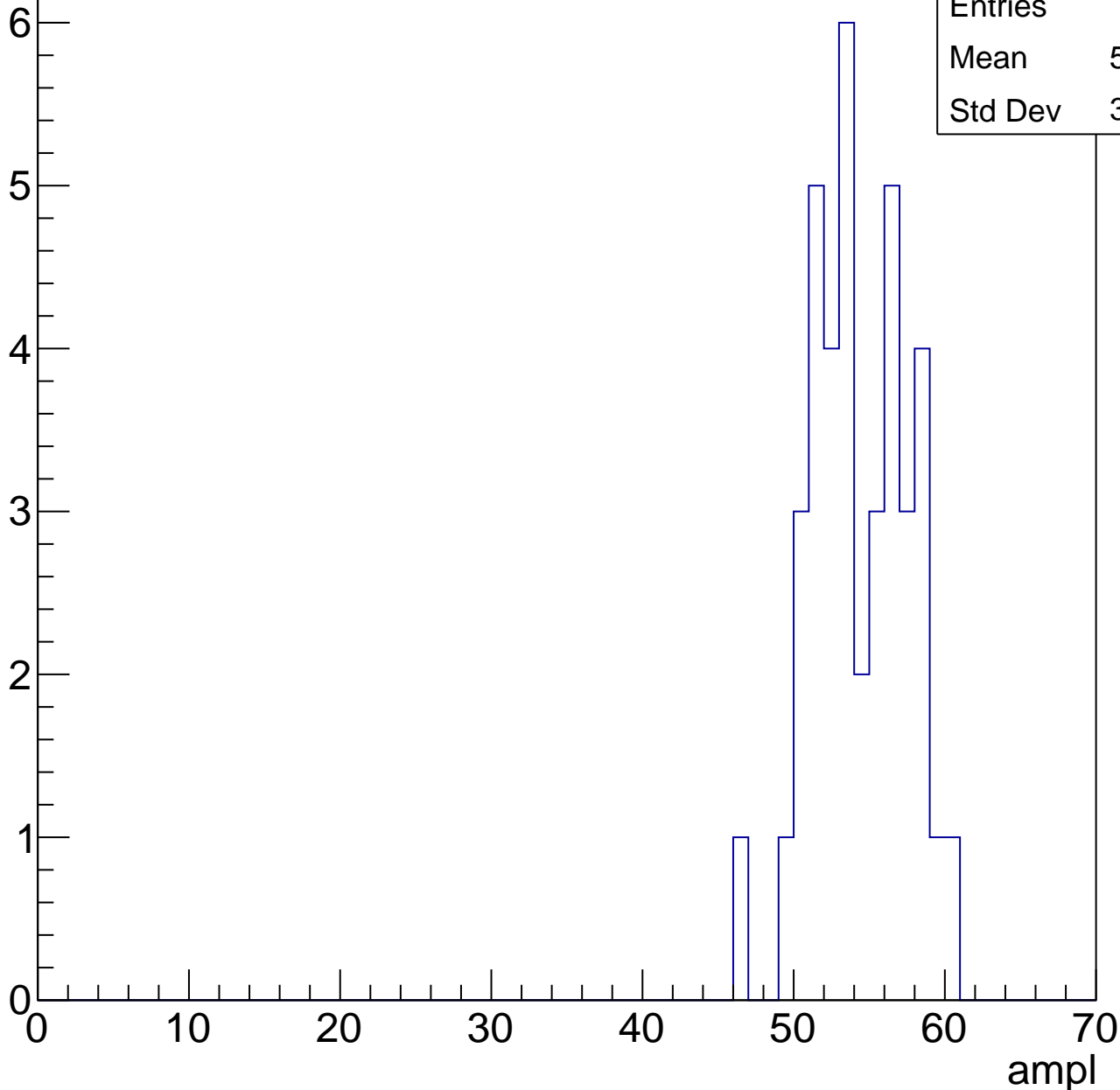


# B1L100S, U2-ch82, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	39
Mean	53.87
Std Dev	3.115

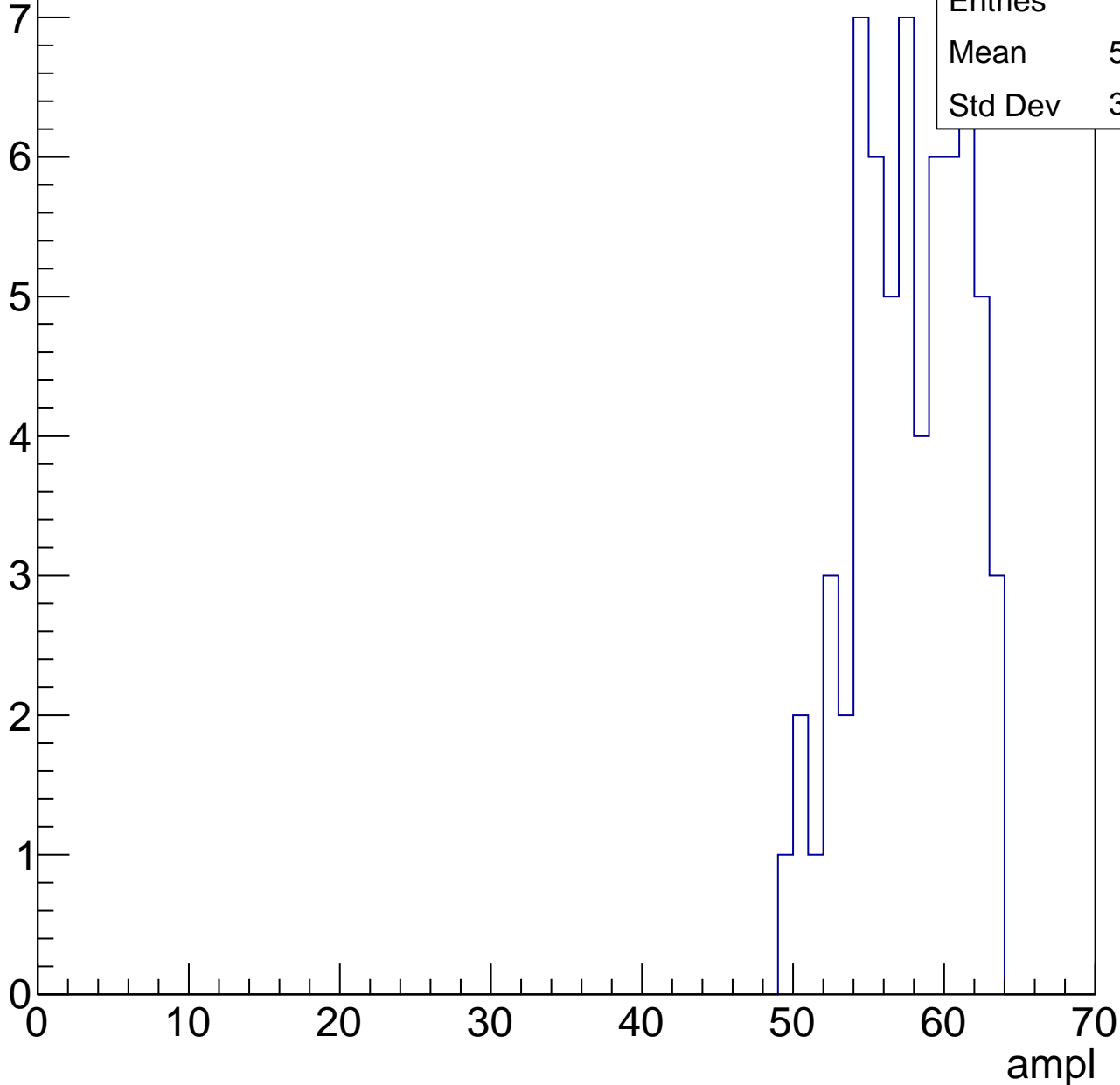


# B1L100S, U2-ch82, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	65
Mean	57.25
Std Dev	3.552

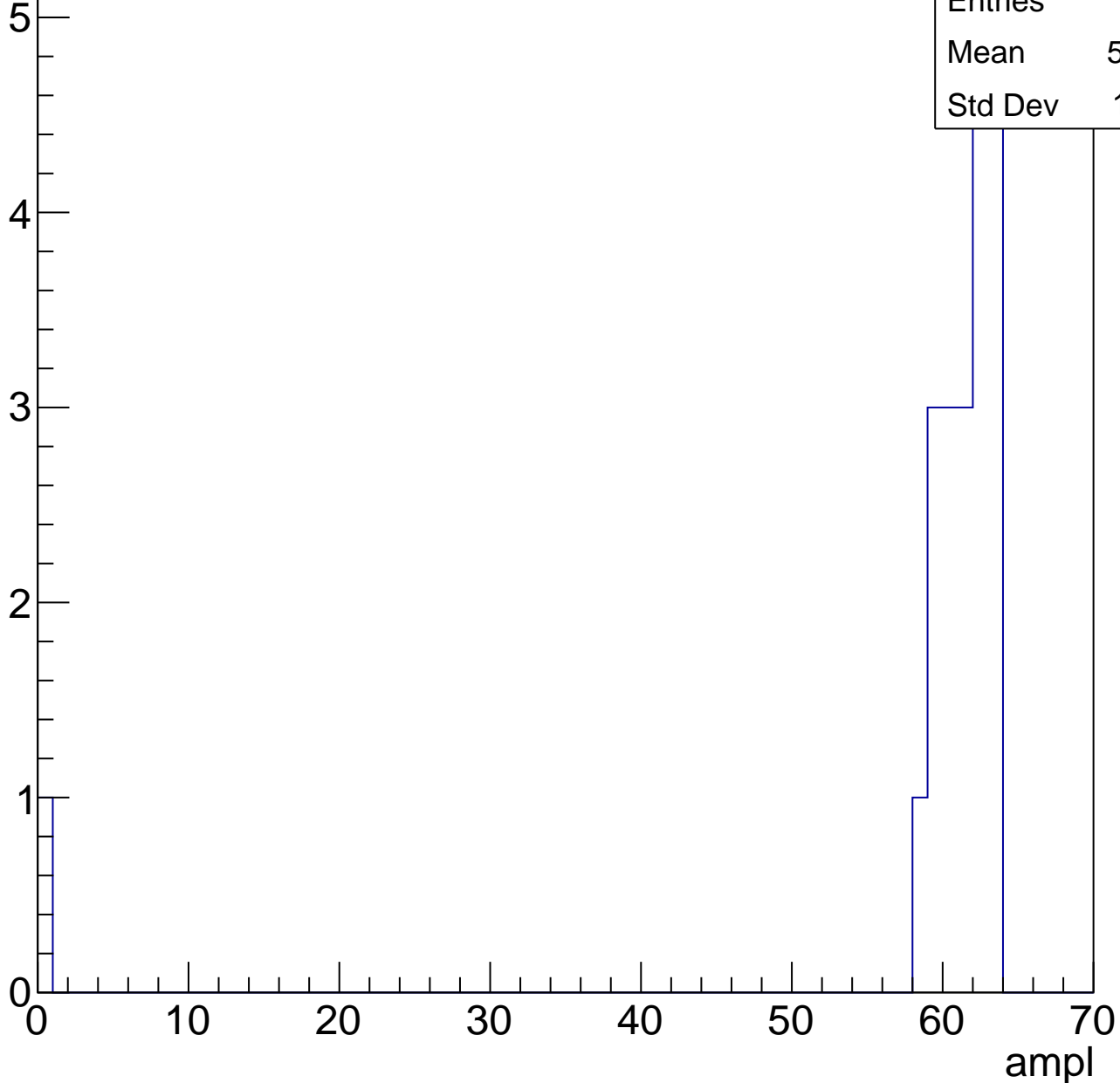


# B1L100S, U2-ch82, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	21
Mean	58.24
Std Dev	13.11





# B1L100S, U2-ch82, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



# B1L100S, U2-ch83, adc0

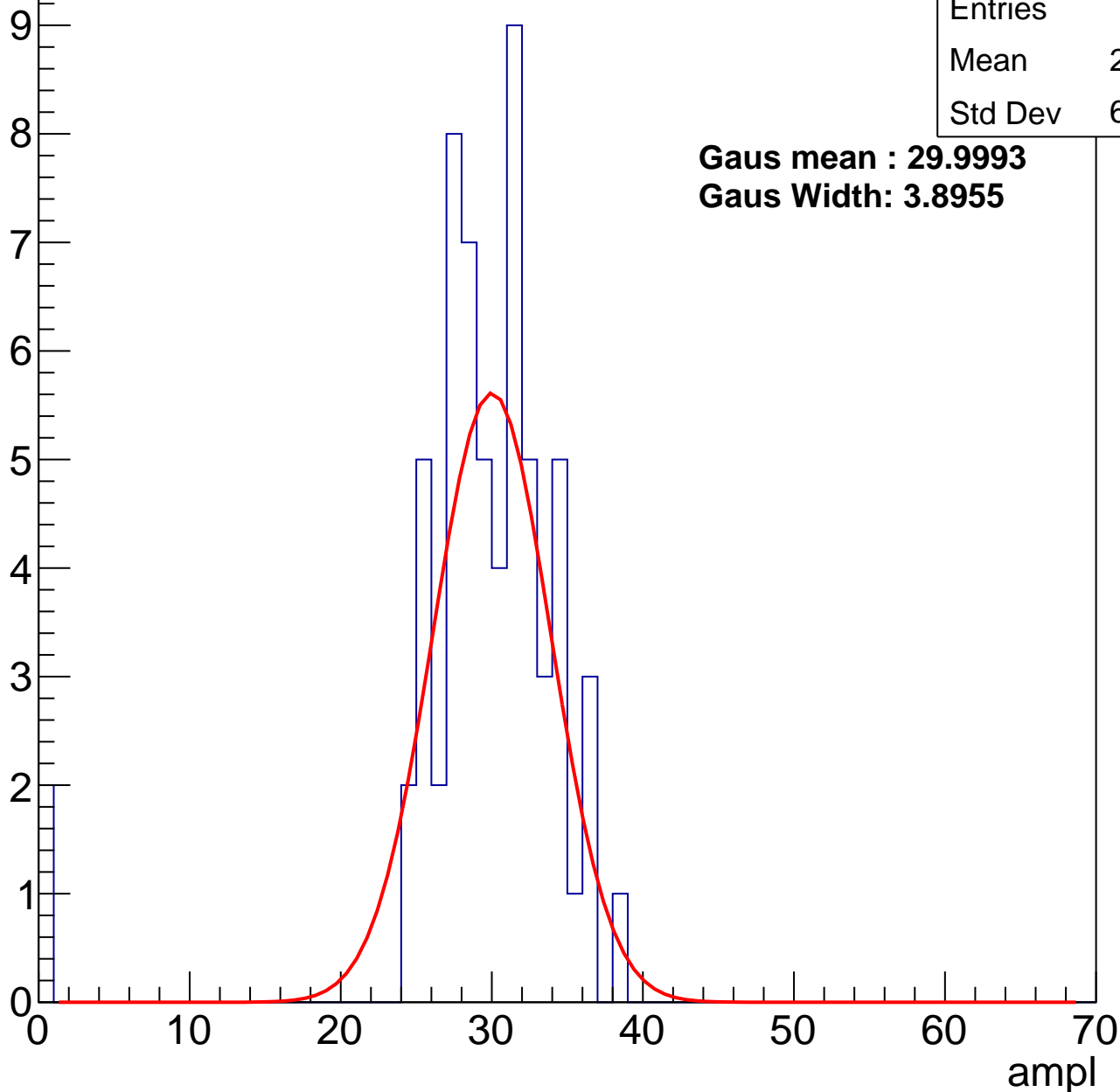
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	62
Mean	28.89
Std Dev	6.209

**Gaus mean : 29.9993**

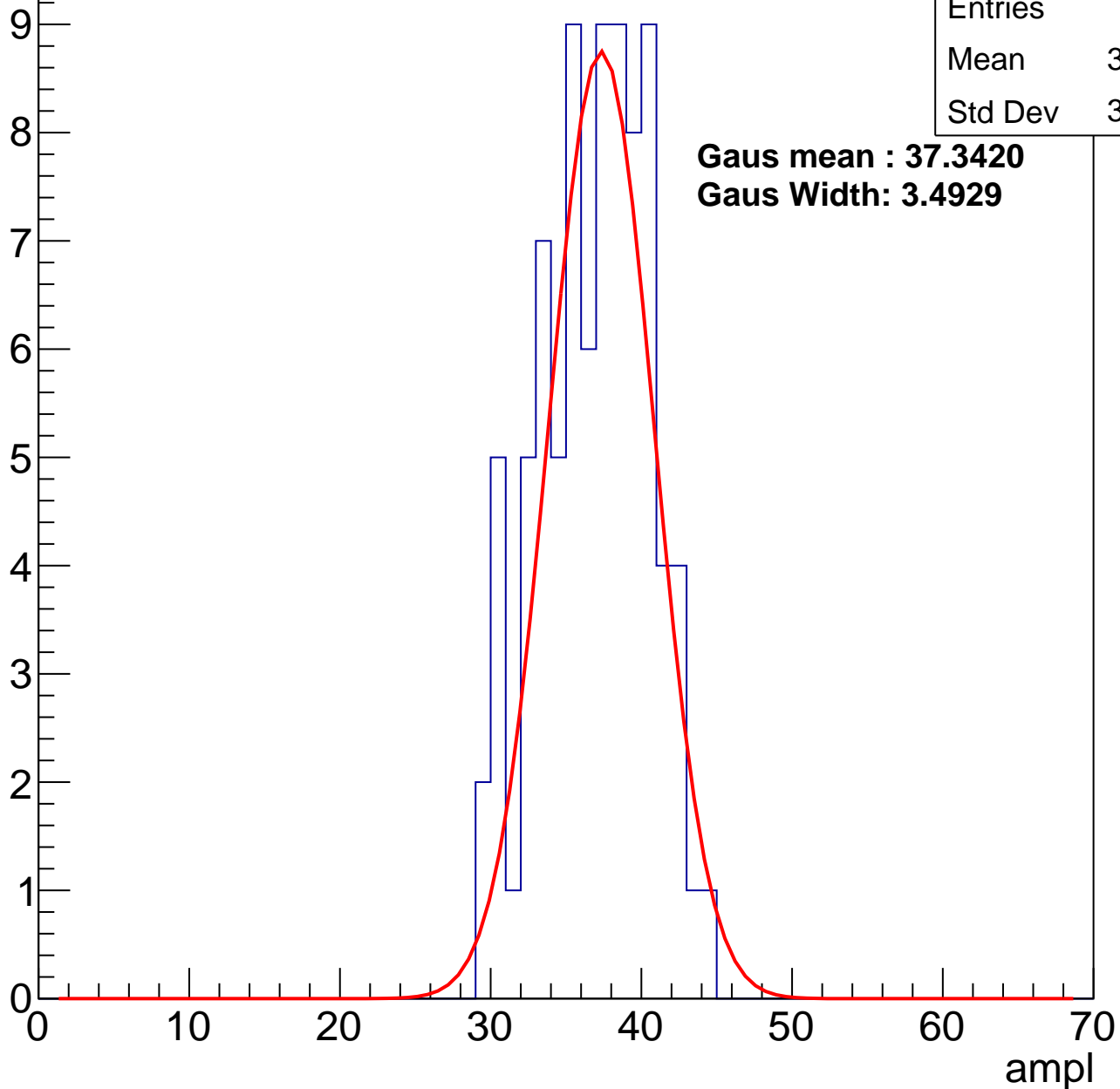
**Gaus Width: 3.8955**



# B1L100S, U2-ch83, adc1

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



# B1L100S, U2-ch83, adc2

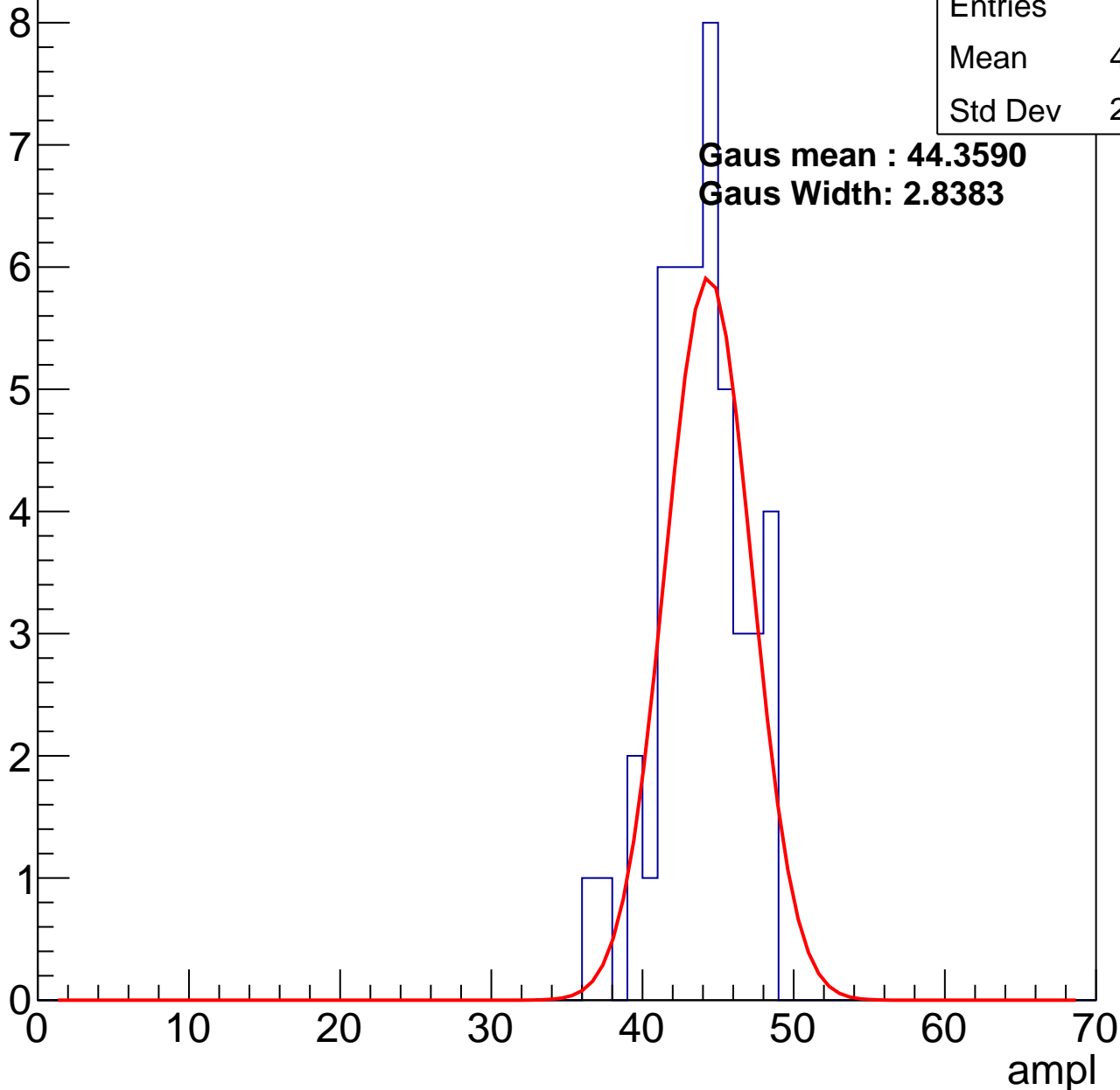
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	46
Mean	43.37
Std Dev	2.769

**Gaus mean : 44.3590**

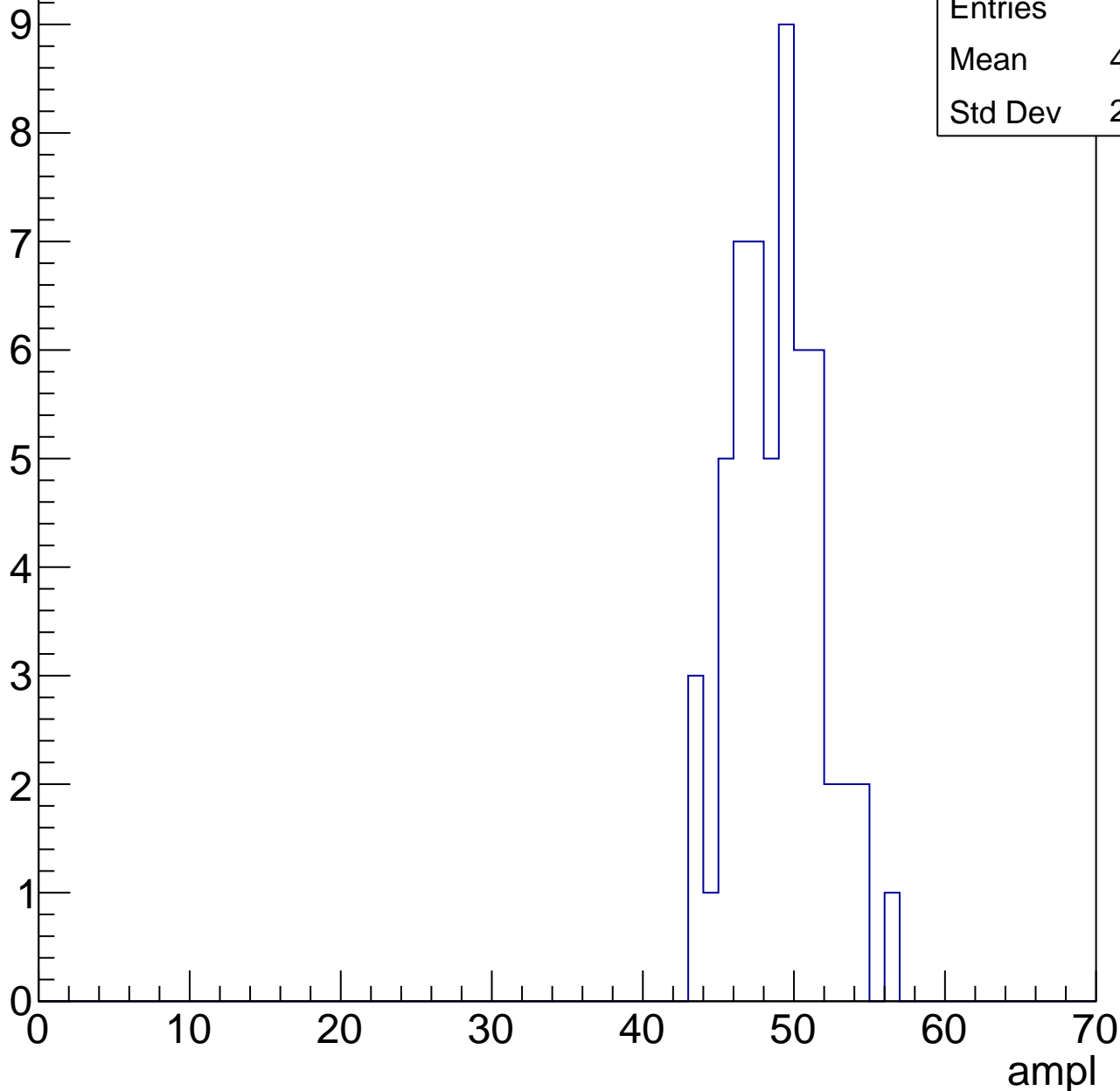
**Gaus Width: 2.8383**



# B1L100S, U2-ch83, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

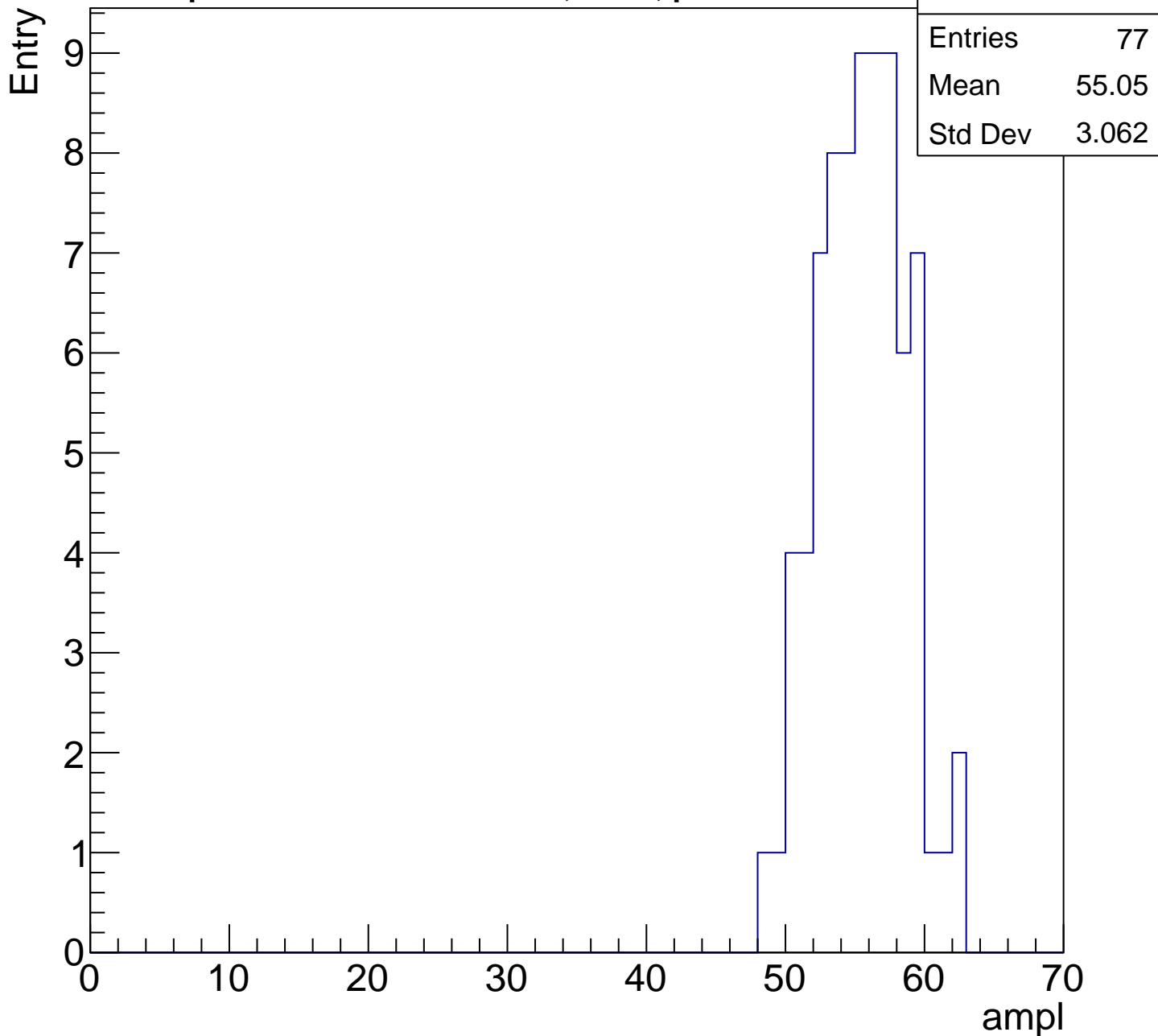
Entry



Entries	56
Mean	48.39
Std Dev	2.889

# B1L100S, U2-ch83, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

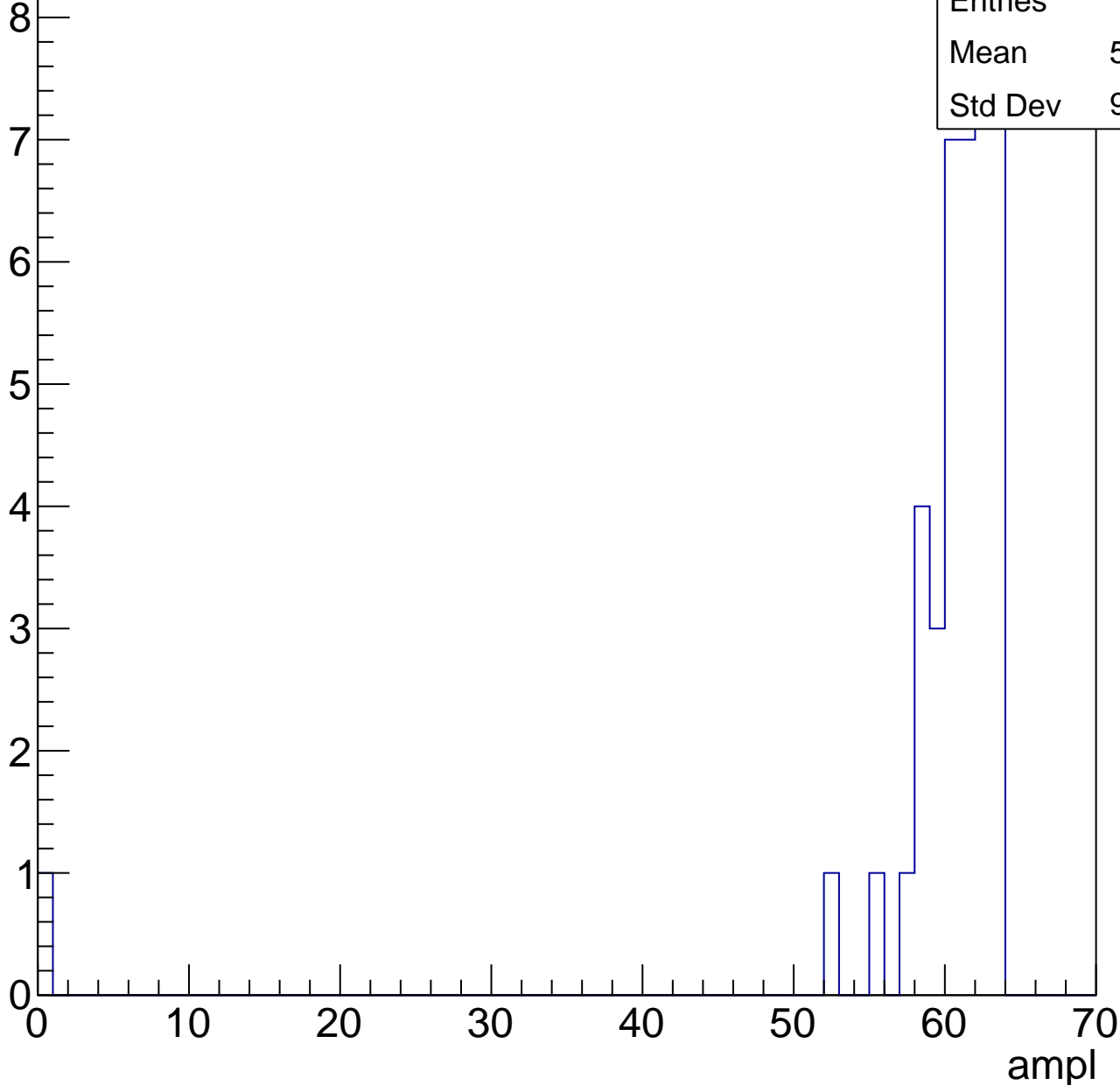


# B1L100S, U2-ch83, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	41
Mean	59.02
Std Dev	9.613



# B1L100S, U2-ch83, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	6
Mean	61.33
Std Dev	1.247

0 10 20 30 40 50 60 70

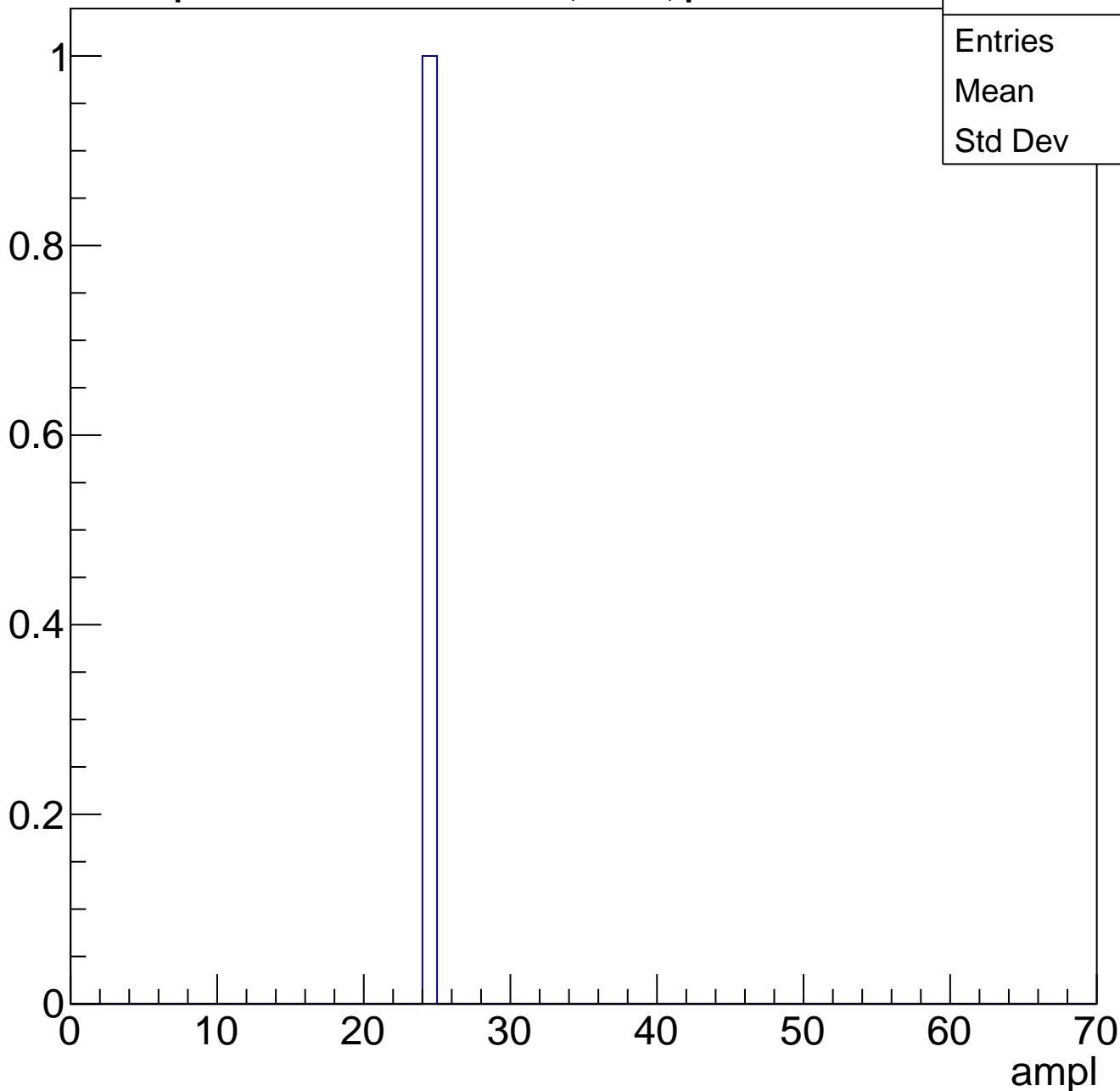
ampl



# B1L100S, U2-ch83, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	1
Mean	24
Std Dev	0

# B1L100S, U2-ch84, adc0

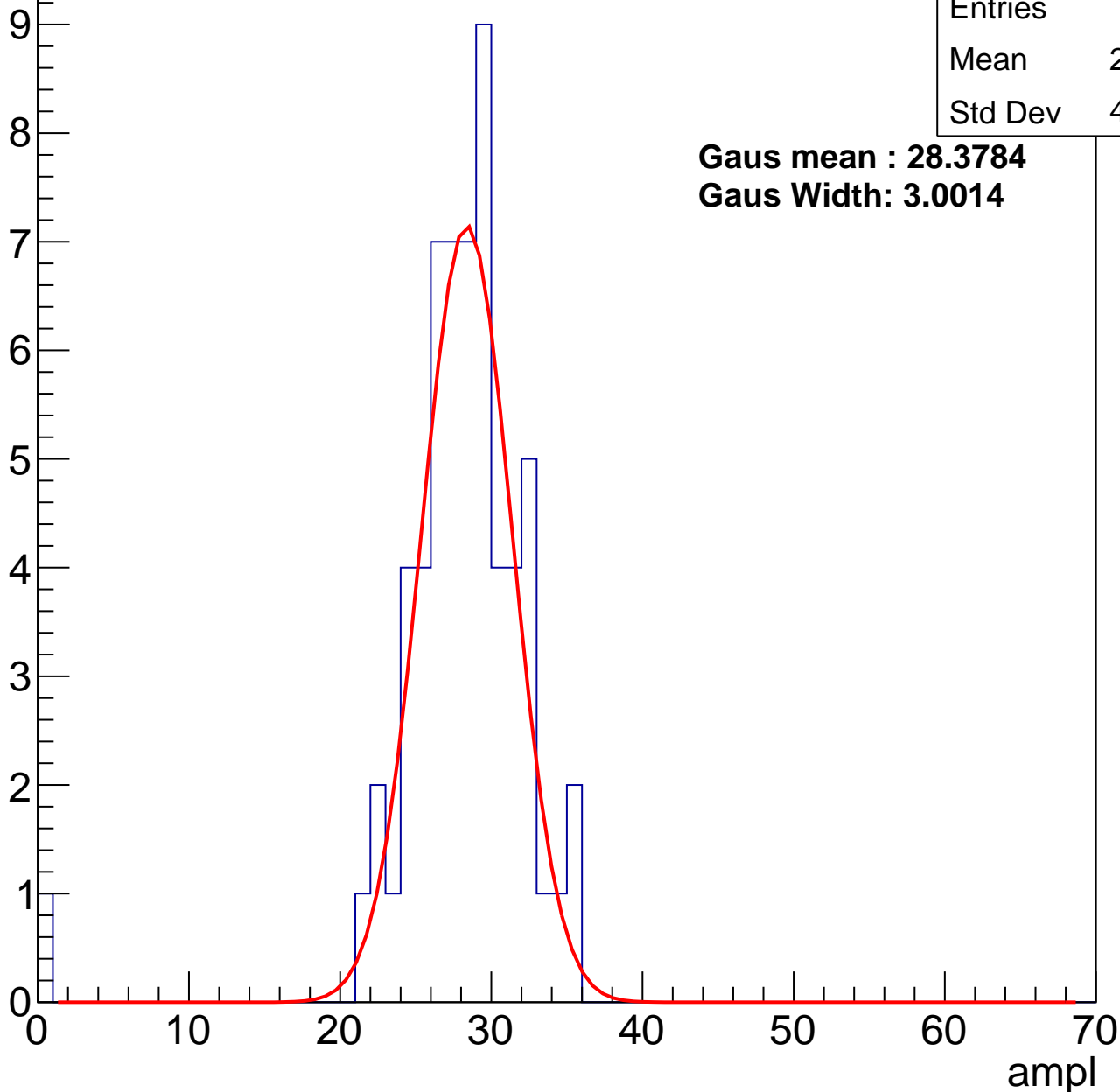
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	60
Mean	27.55
Std Dev	4.748

**Gaus mean : 28.3784**

**Gaus Width: 3.0014**



# B1L100S, U2-ch84, adc1

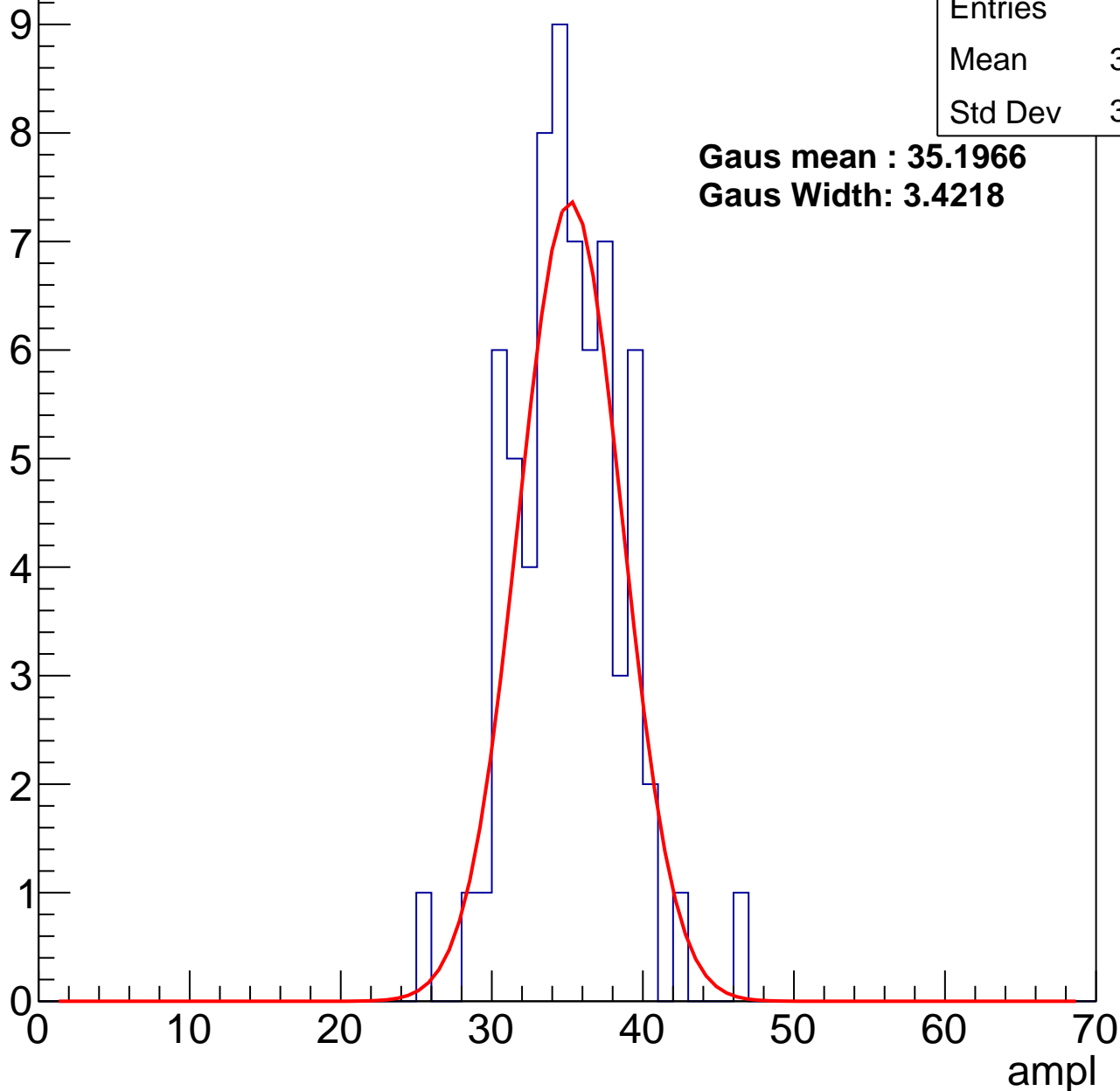
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	68
Mean	34.57
Std Dev	3.549

**Gaus mean : 35.1966**

**Gaus Width: 3.4218**



# B1L100S, U2-ch84, adc2

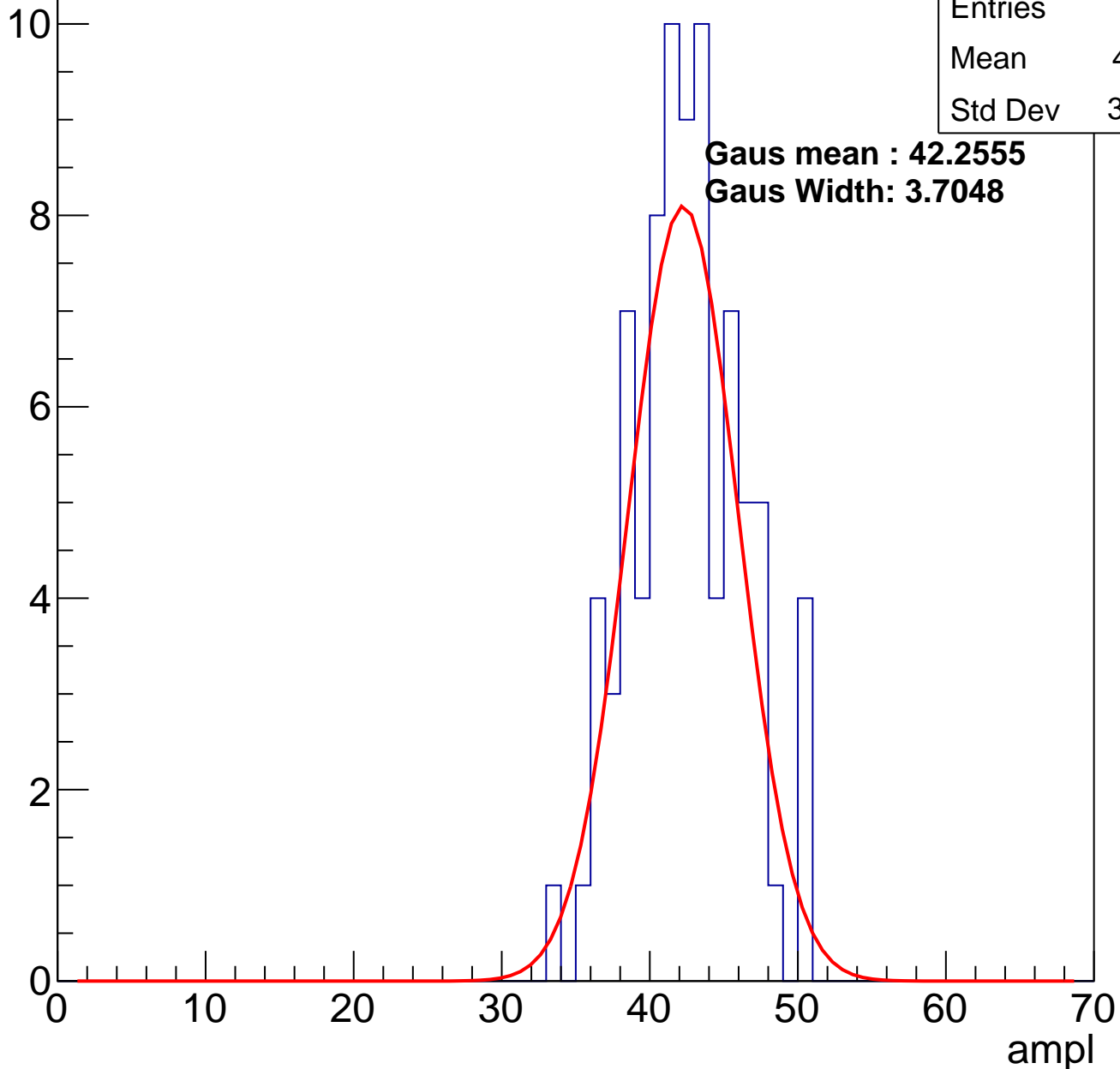
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	83
Mean	42.01
Std Dev	3.682

**Gaus mean : 42.2555**

**Gaus Width: 3.7048**

Entry

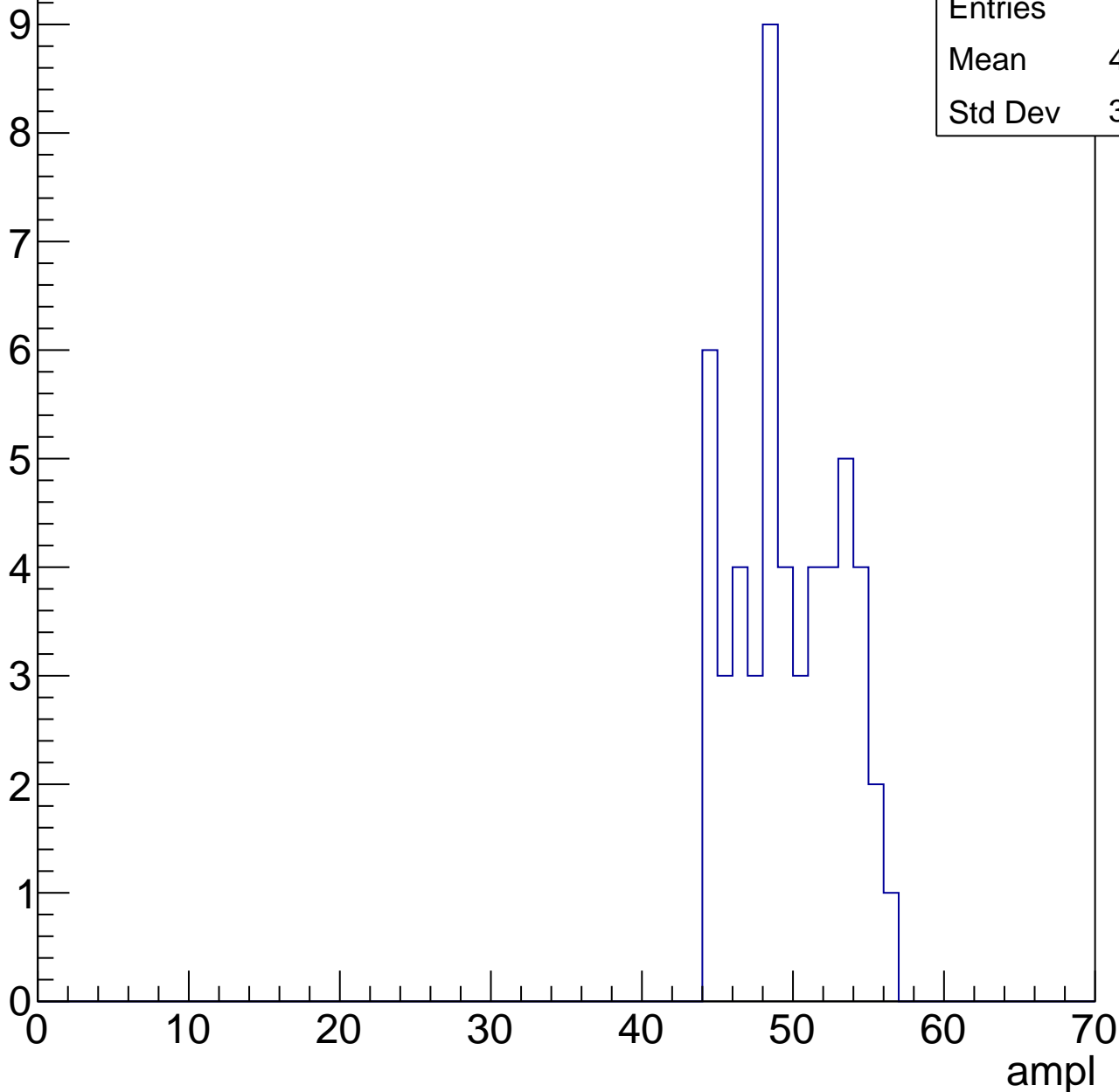


# B1L100S, U2-ch84, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	52
Mean	49.25
Std Dev	3.419

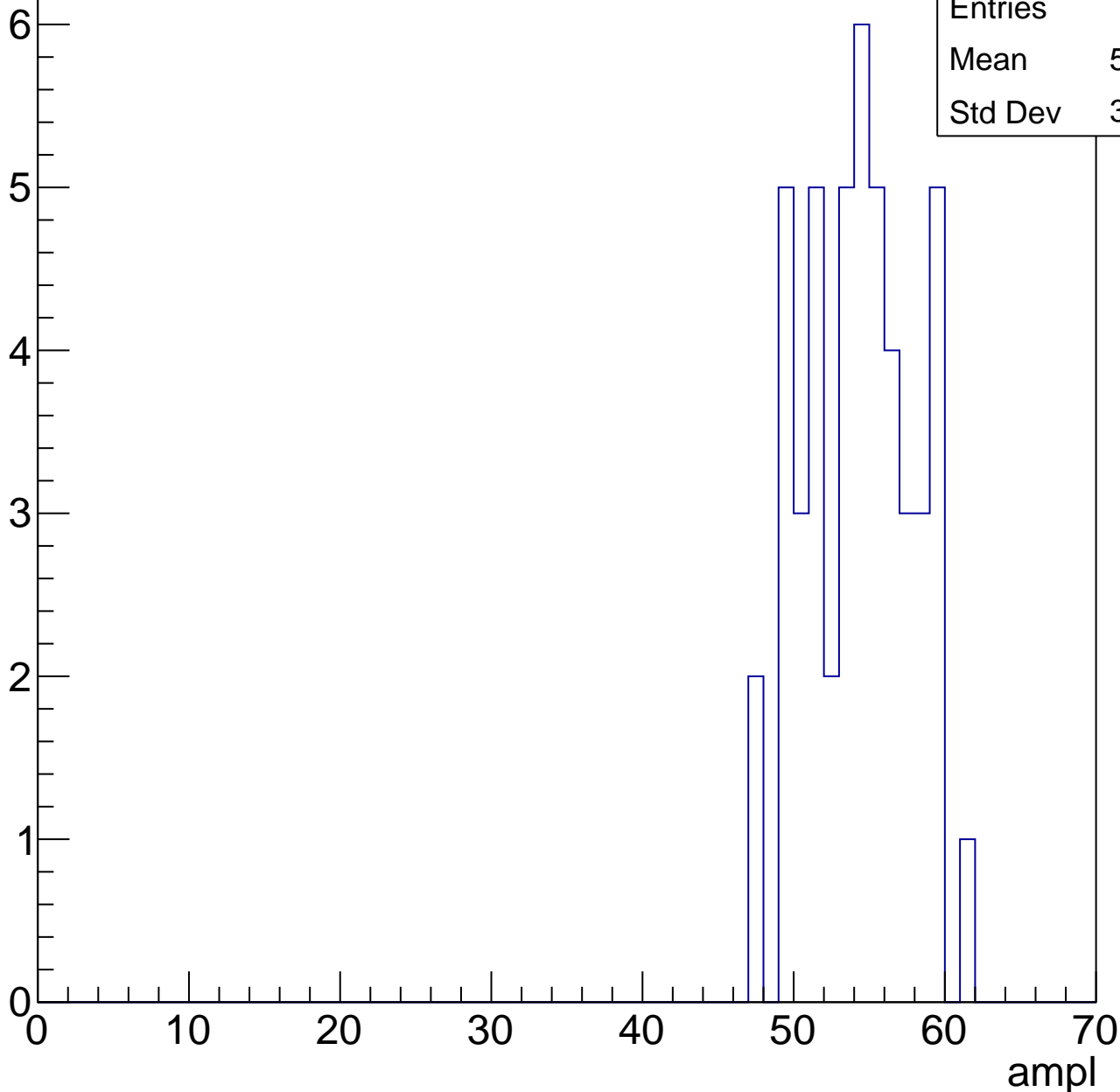


# B1L100S, U2-ch84, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	49
Mean	53.82
Std Dev	3.492



# B1L100S, U2-ch84, adc5

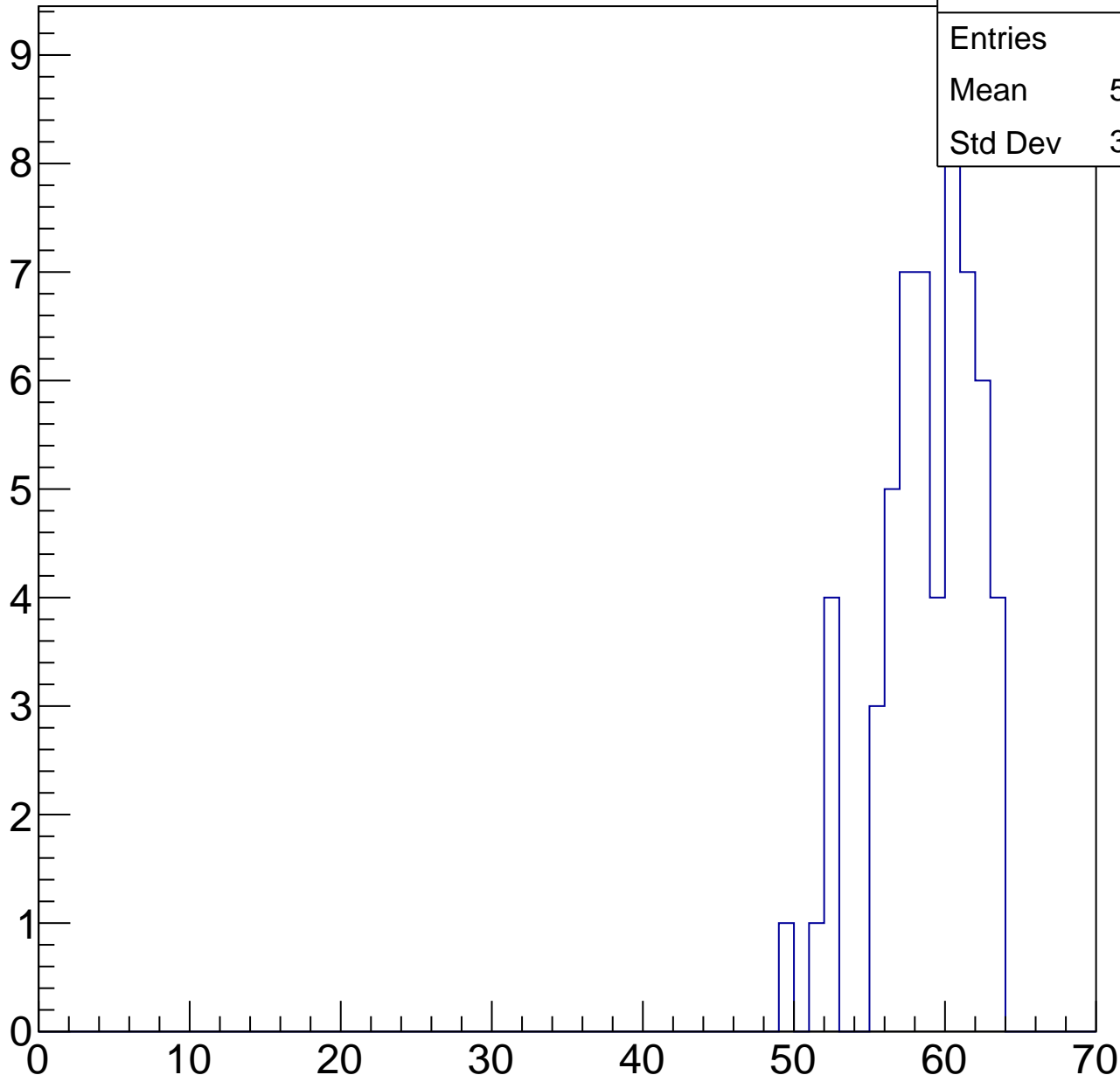
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	58
Mean	58.36
Std Dev	3.268

ampl

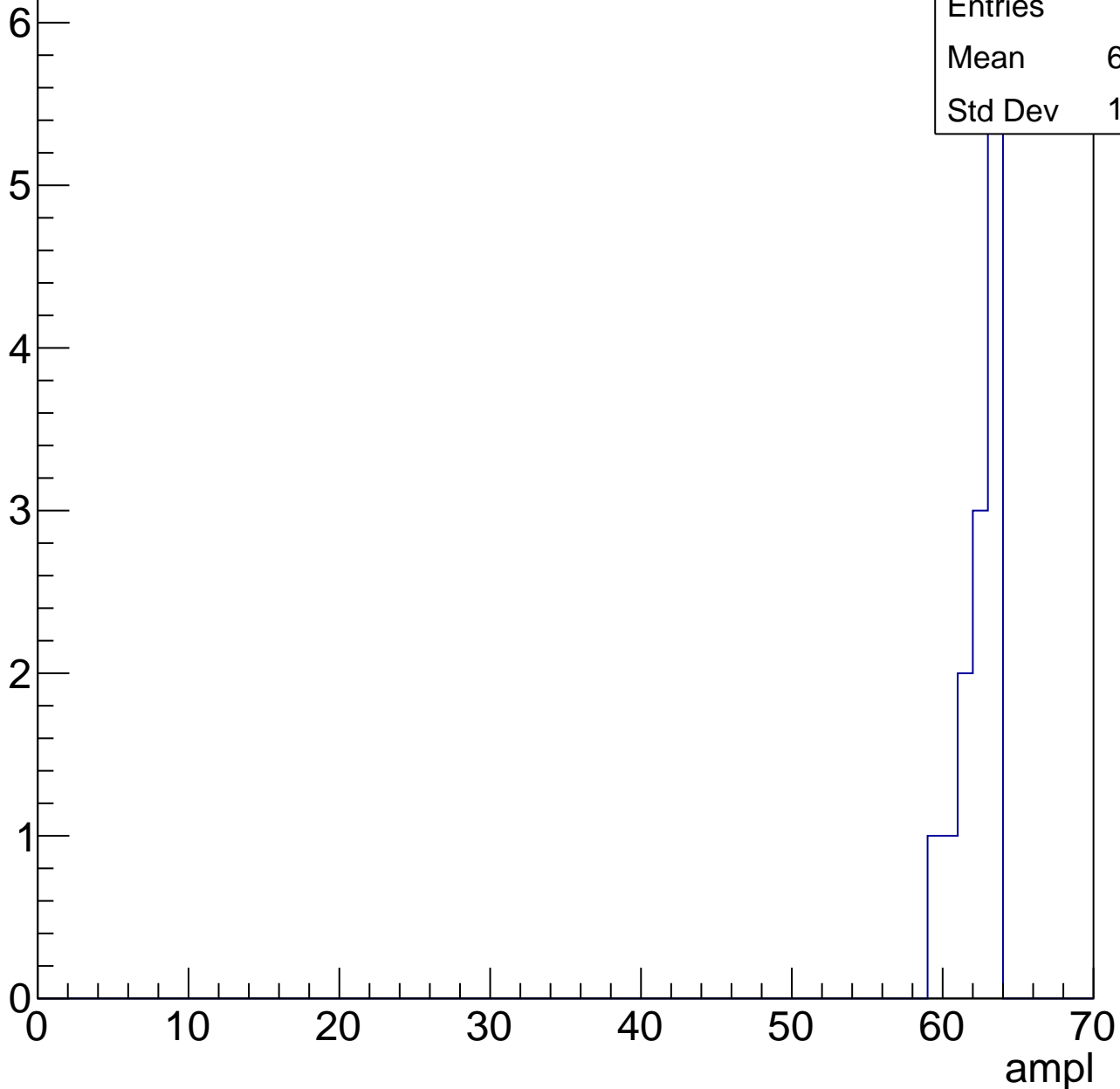


# B1L100S, U2-ch84, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	13
Mean	61.92
Std Dev	1.269





# B1L100S, U2-ch84, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



# B1L100S, U2-ch85, adc0

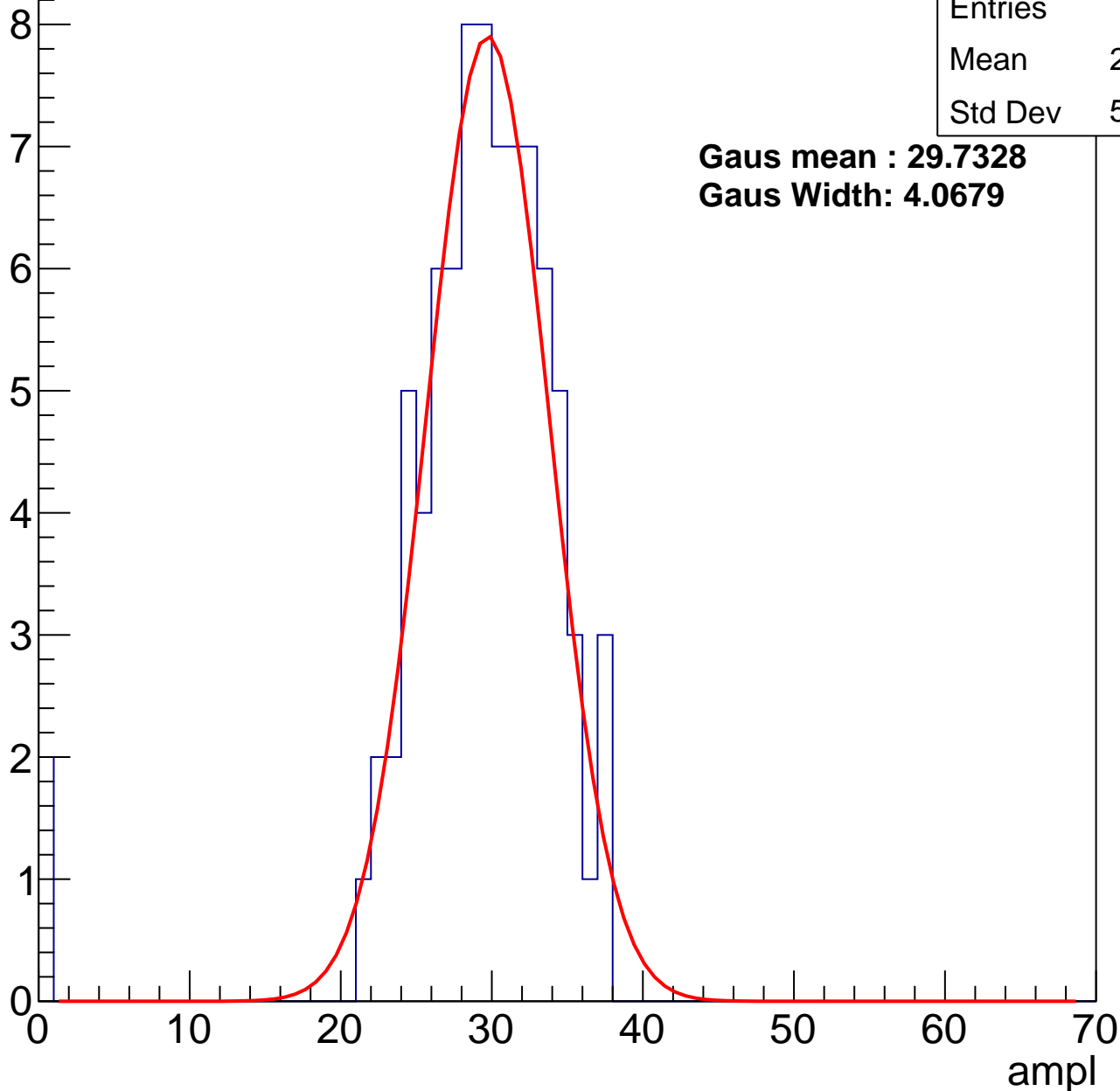
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	83
Mean	28.63
Std Dev	5.857

**Gaus mean : 29.7328**

**Gaus Width: 4.0679**



# B1L100S, U2-ch85, adc1

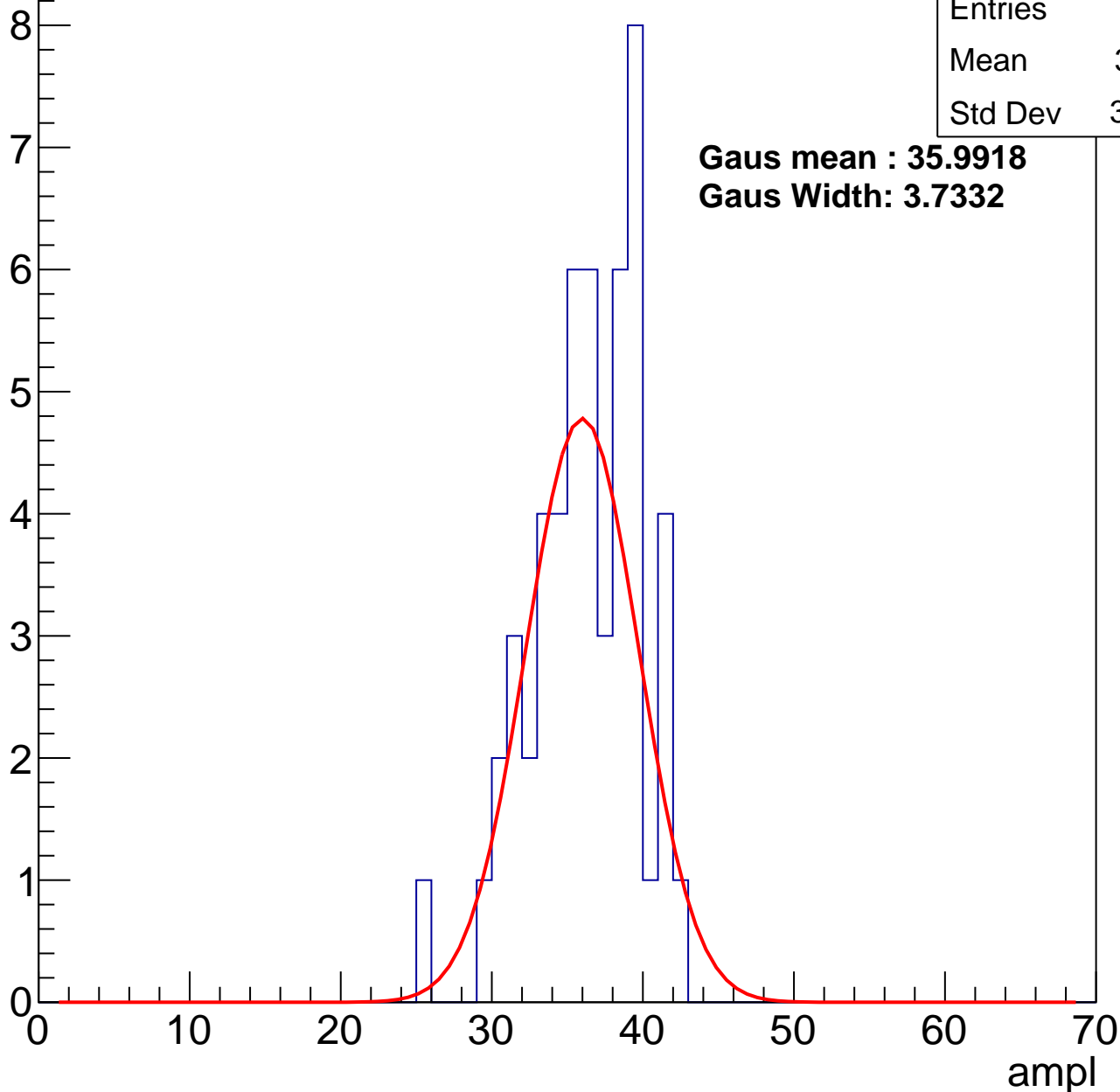
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	52
Mean	35.81
Std Dev	3.552

**Gaus mean : 35.9918**

**Gaus Width: 3.7332**



# B1L100S, U2-ch85, adc2

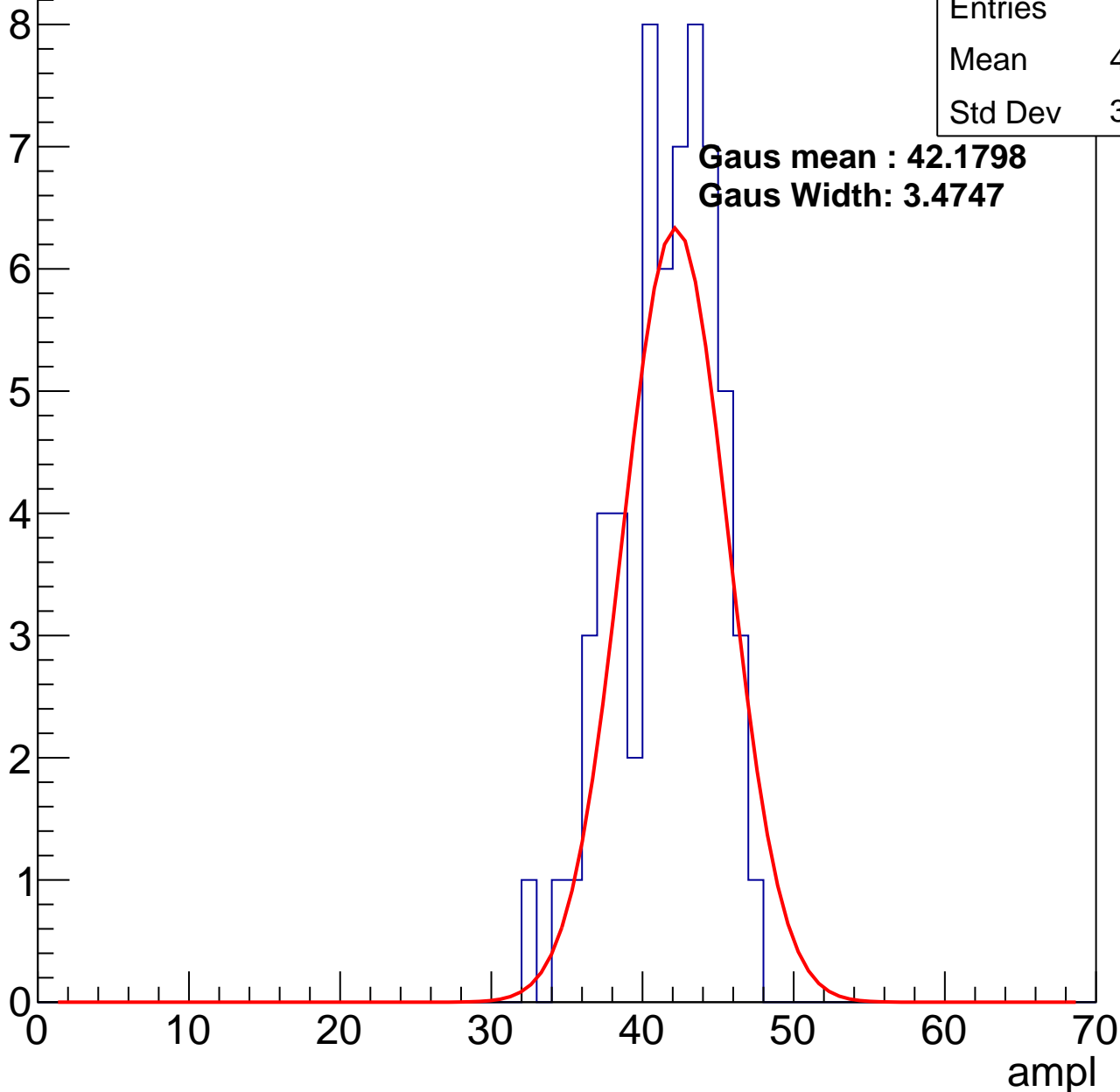
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	61
Mean	41.13
Std Dev	3.262

**Gaus mean : 42.1798**

**Gaus Width: 3.4747**



# B1L100S, U2-ch85, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

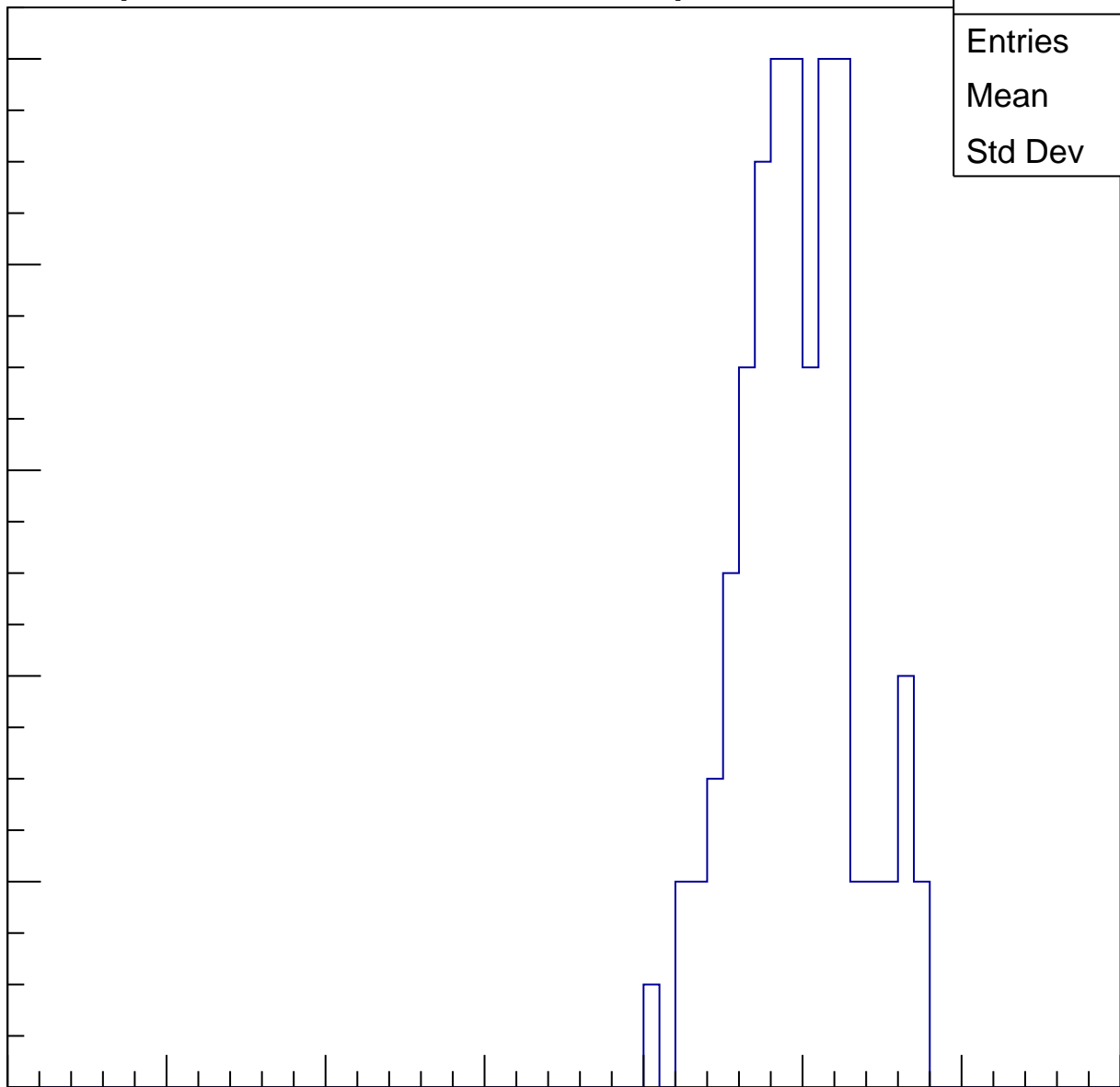
Entries	88
Mean	49.14
Std Dev	3.581

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

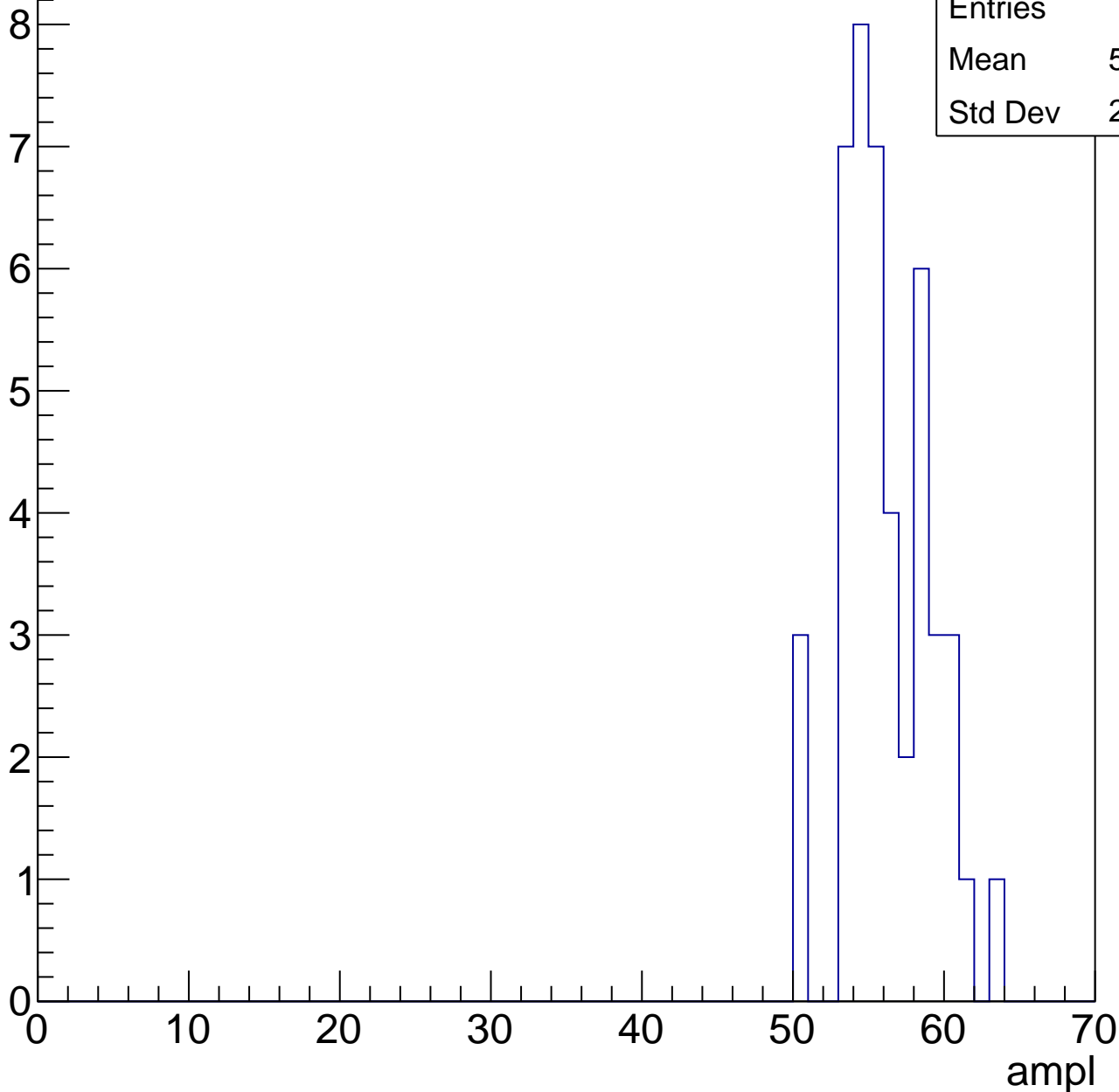


# B1L100S, U2-ch85, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	45
Mean	55.67
Std Dev	2.906

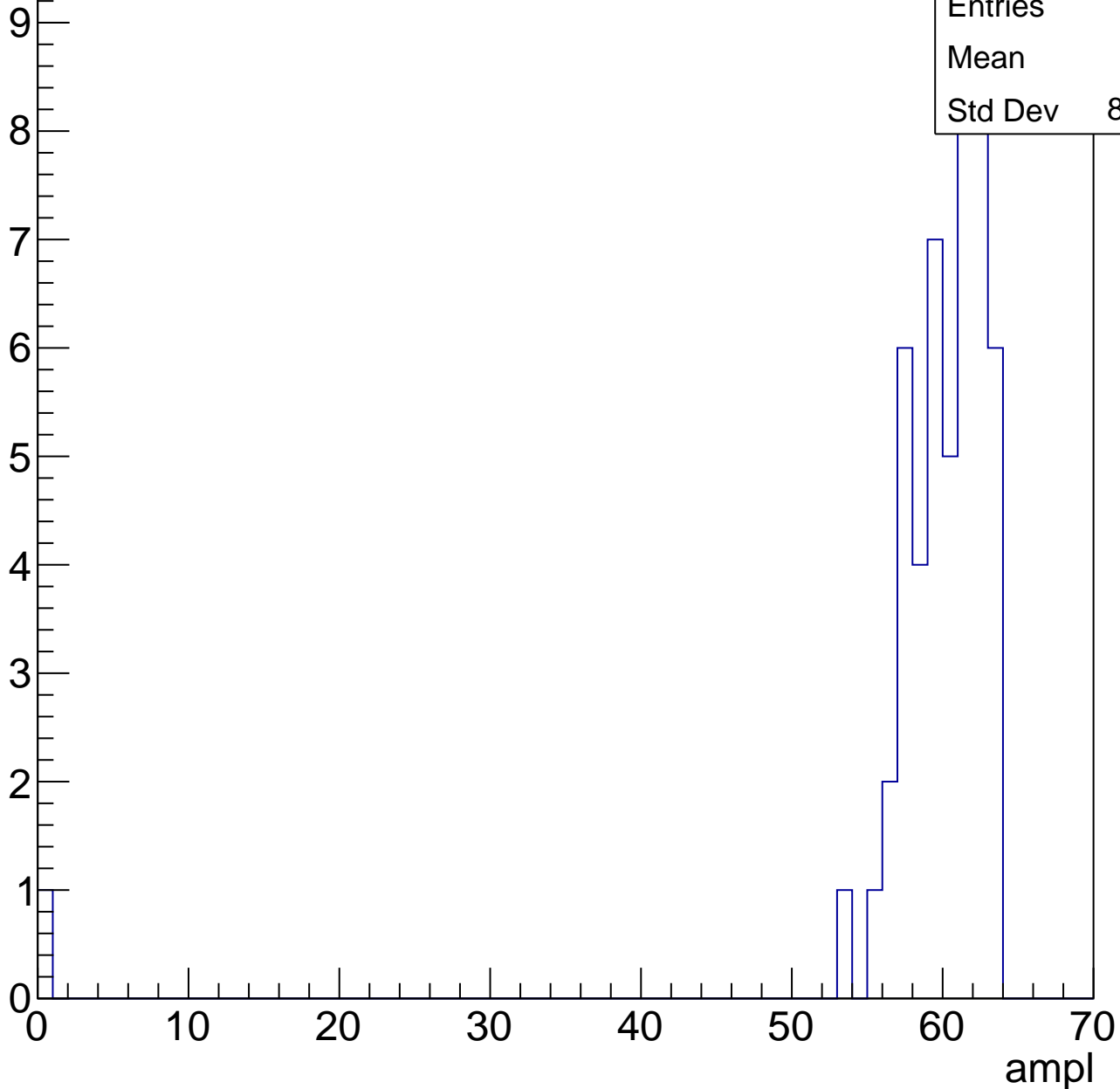


# B1L100S, U2-ch85, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

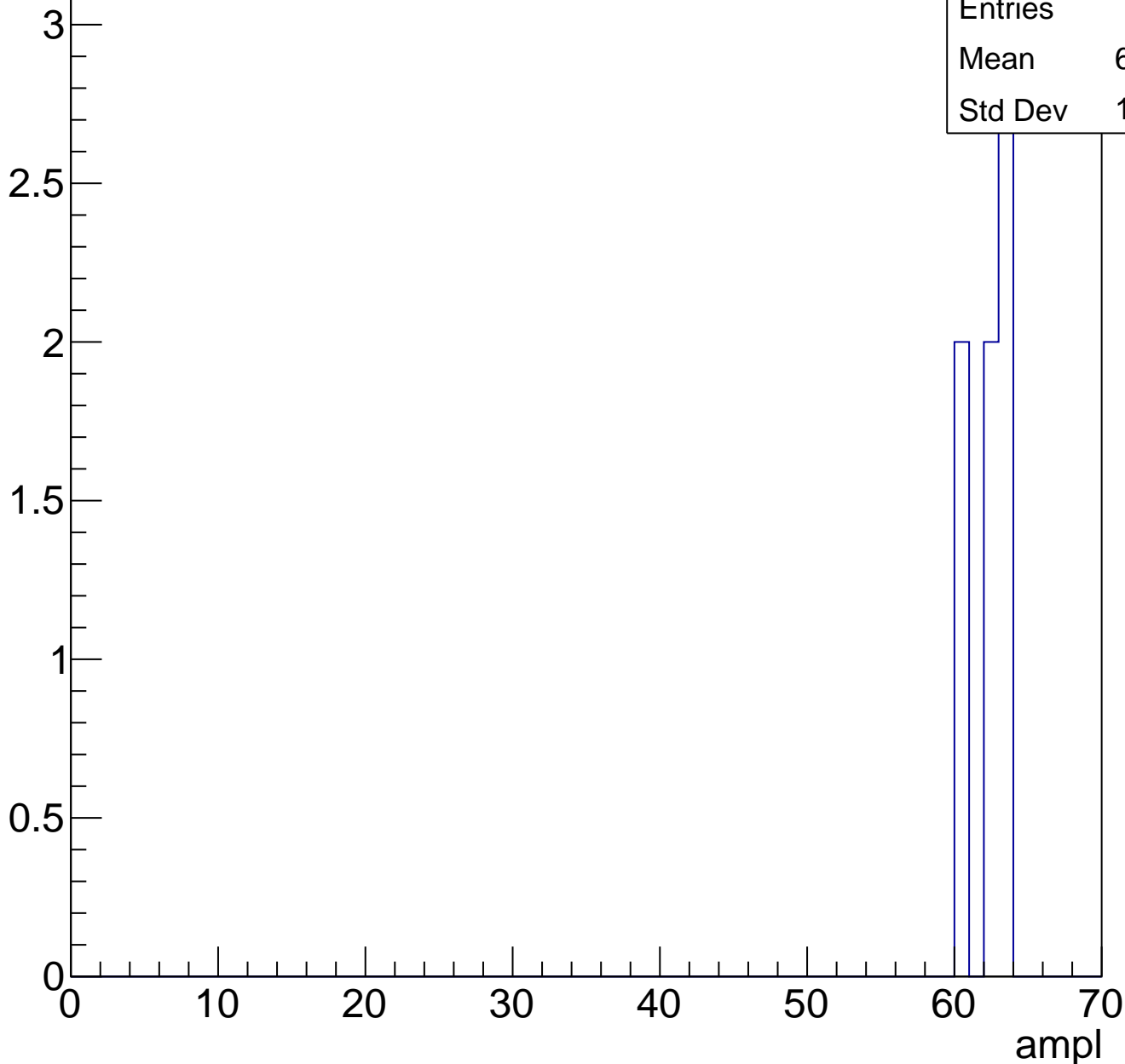
Entries	50
Mean	58.6
Std Dev	8.695



# B1L100S, U2-ch85, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry





# B1L100S, U2-ch85, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



# B1L100S, U2-ch86, adc0

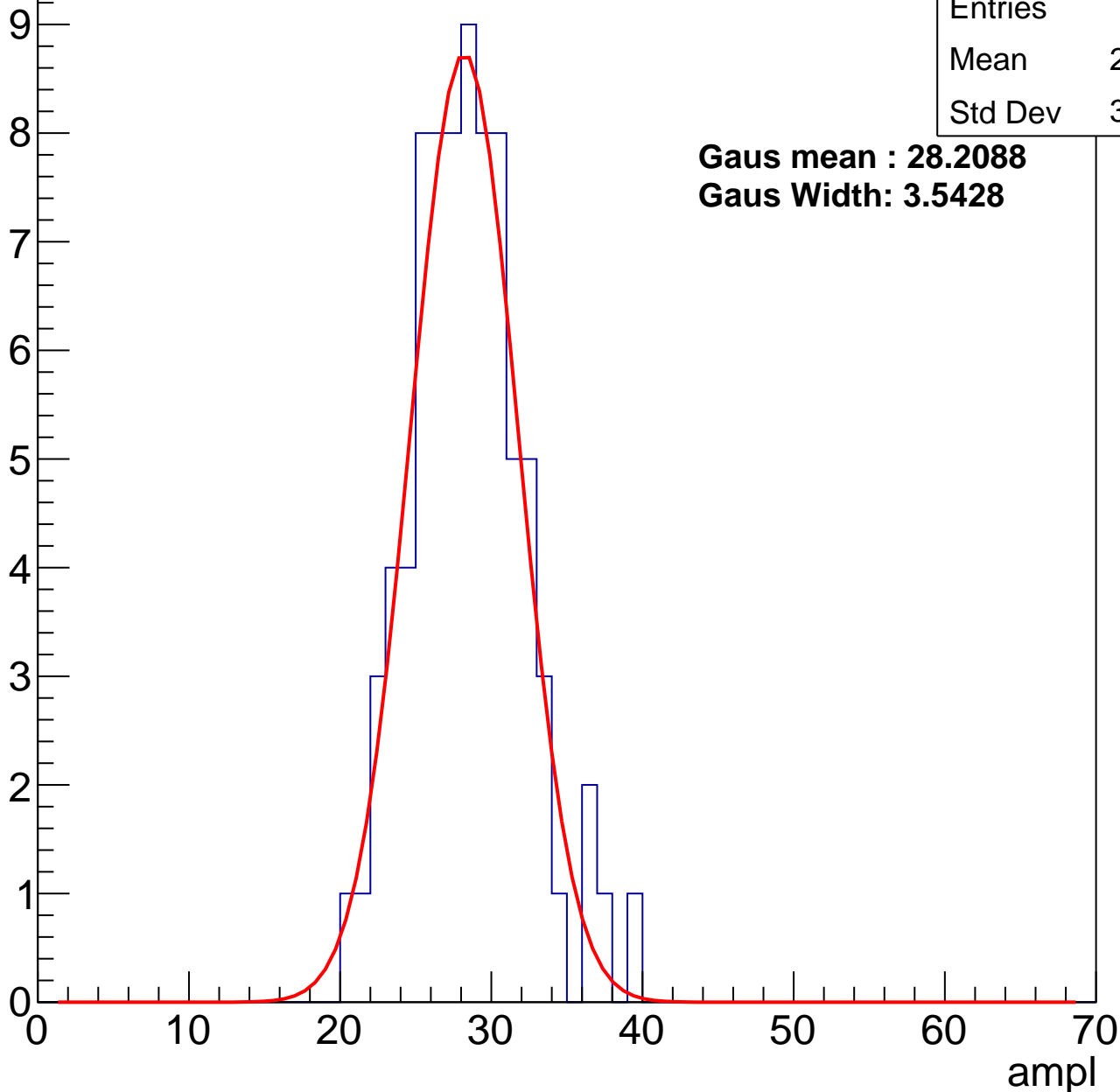
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	80
Mean	27.99
Std Dev	3.713

**Gaus mean : 28.2088**

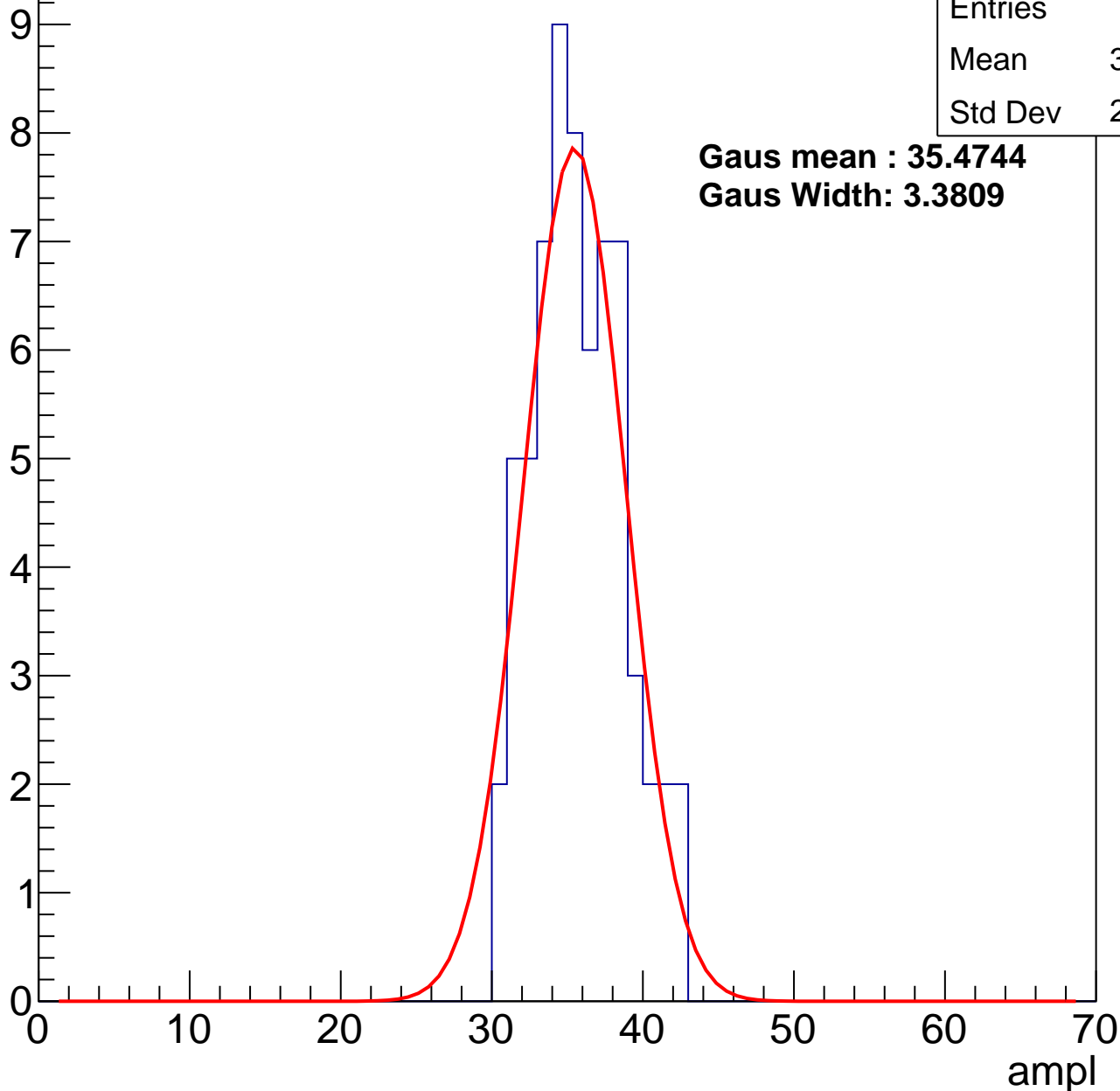
**Gaus Width: 3.5428**



# B1L100S, U2-ch86, adc1

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



# B1L100S, U2-ch86, adc2

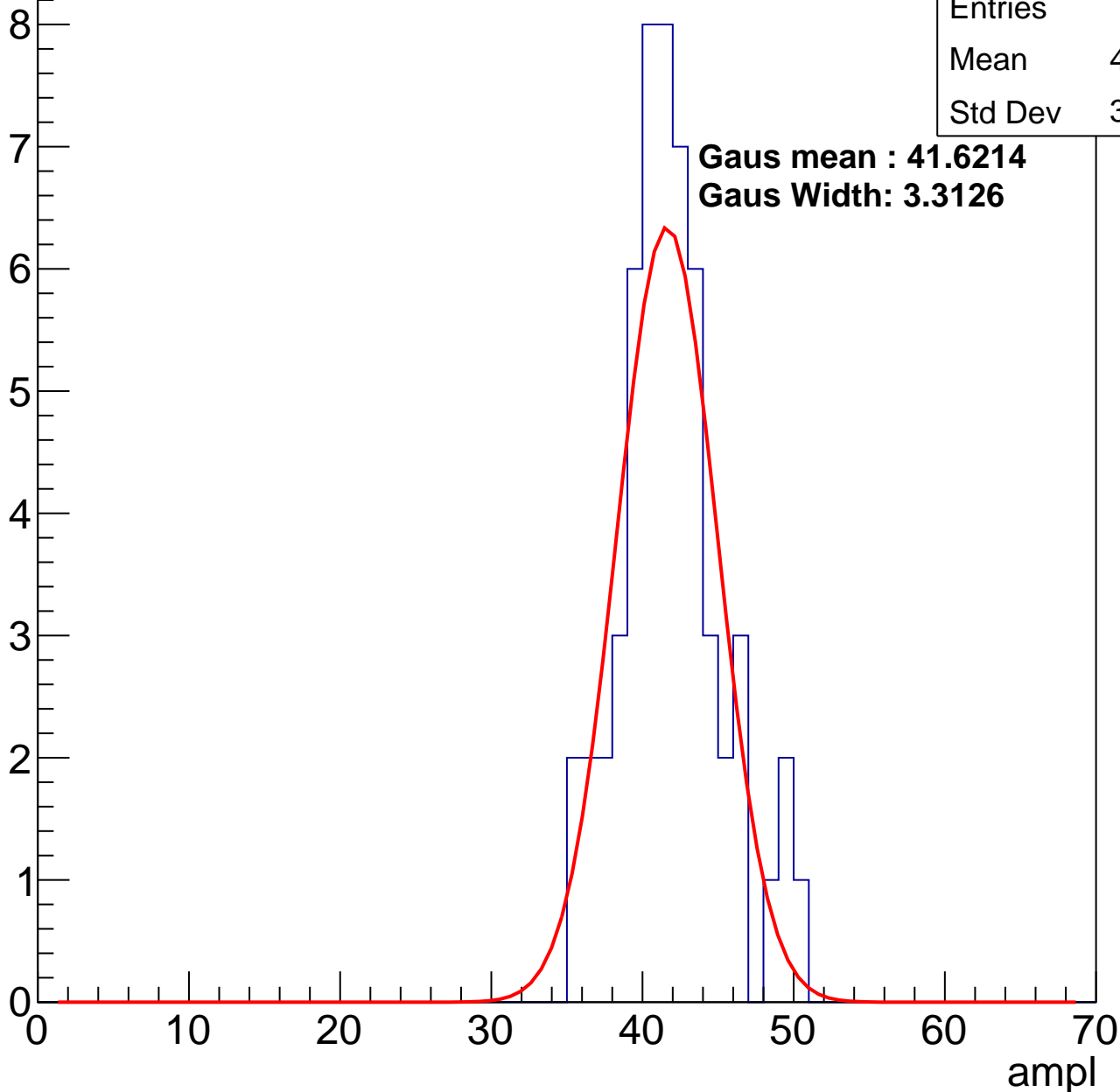
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	56
Mean	41.43
Std Dev	3.343

**Gaus mean : 41.6214**

**Gaus Width: 3.3126**



# B1L100S, U2-ch86, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	77
Mean	48.18
Std Dev	3.341

Entry

10

8

6

4

2

0

0

10

20

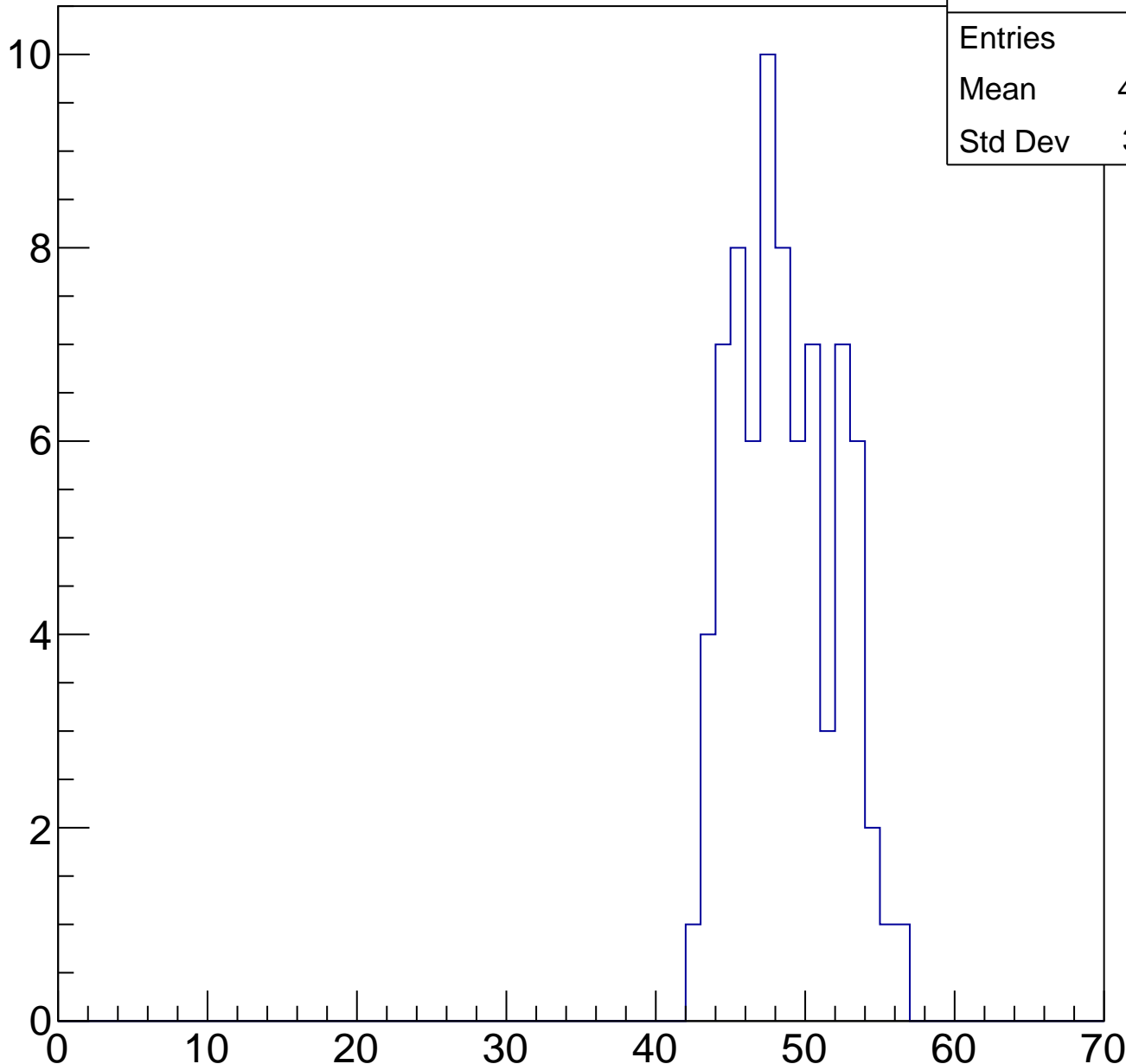
30

40

50

60

ampl

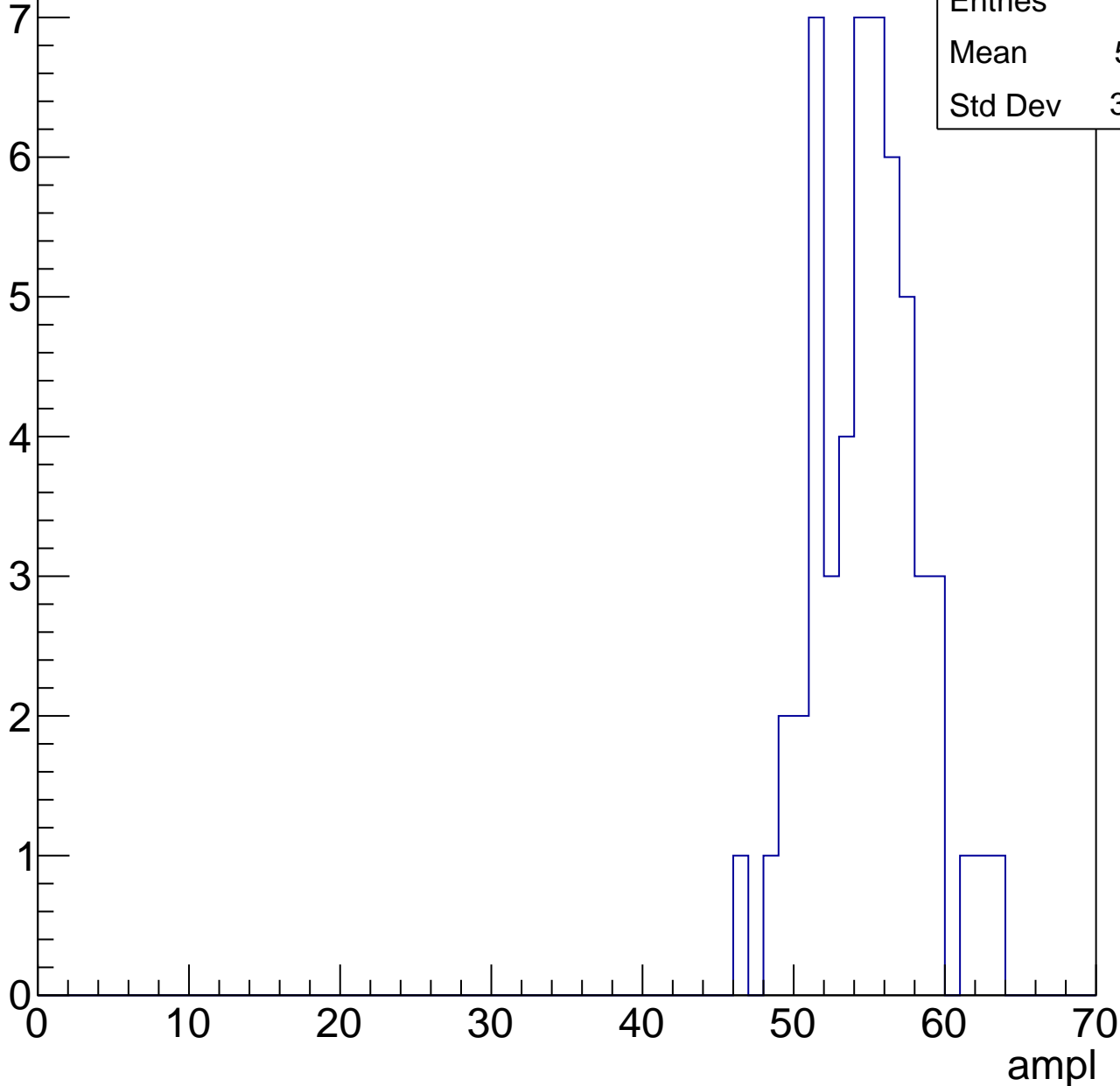


# B1L100S, U2-ch86, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	54
Mean	54.41
Std Dev	3.456

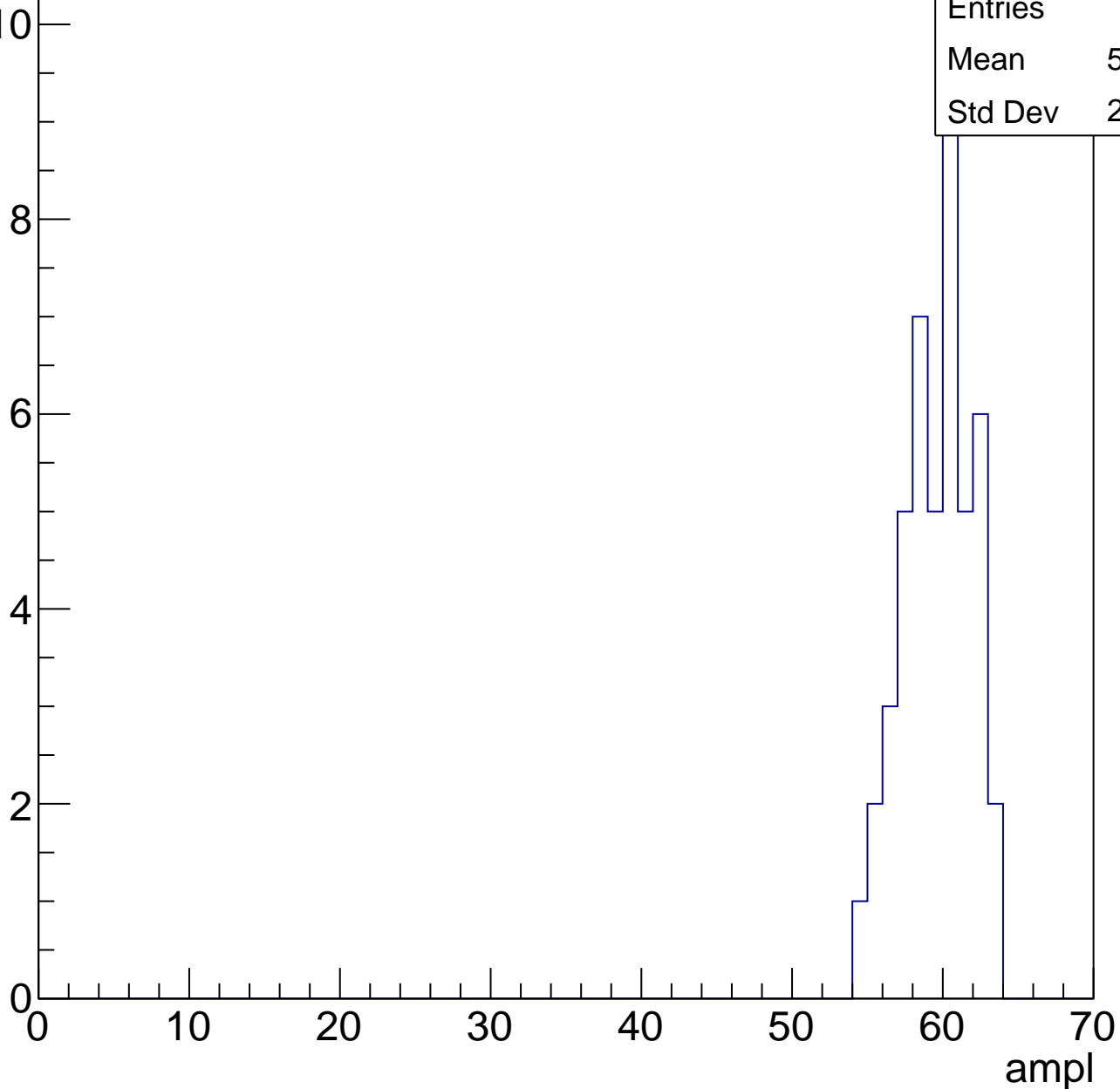


# B1L100S, U2-ch86, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	46
Mean	59.15
Std Dev	2.216

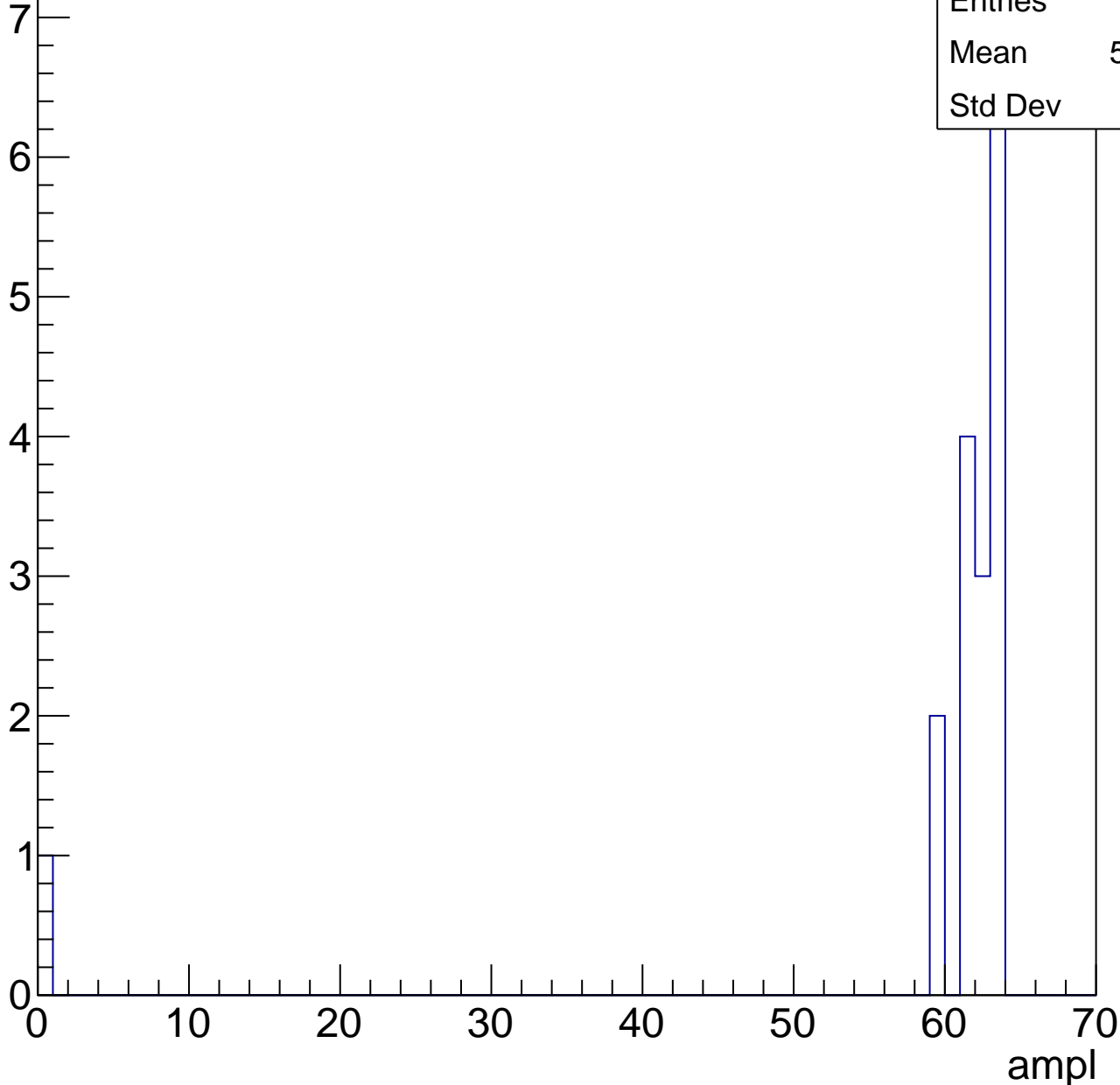


# B1L100S, U2-ch86, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	17
Mean	58.18
Std Dev	14.6

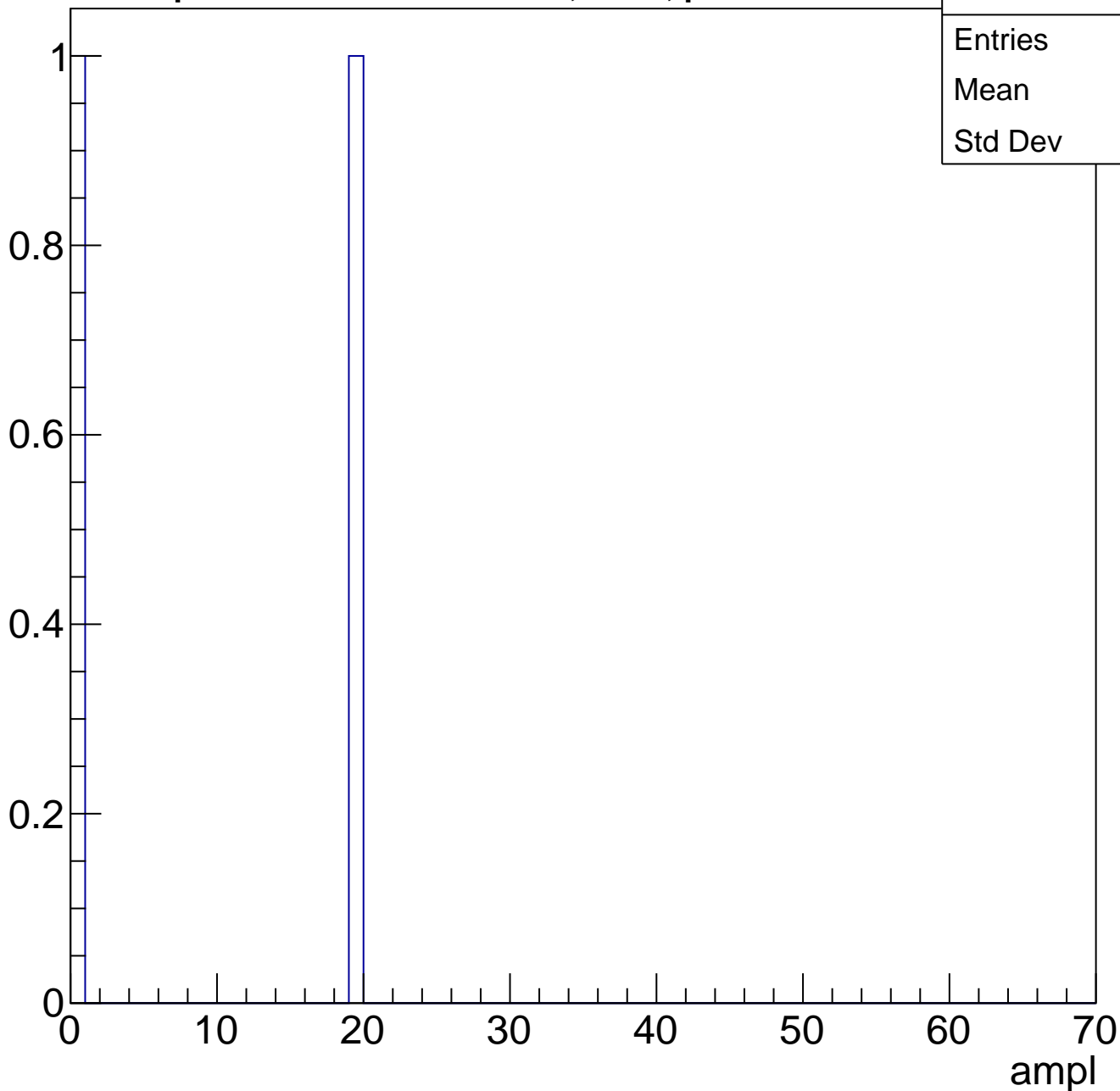




# B1L100S, U2-ch86, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	2
Mean	9.5
Std Dev	9.5

# B1L100S, U2-ch87, adc0

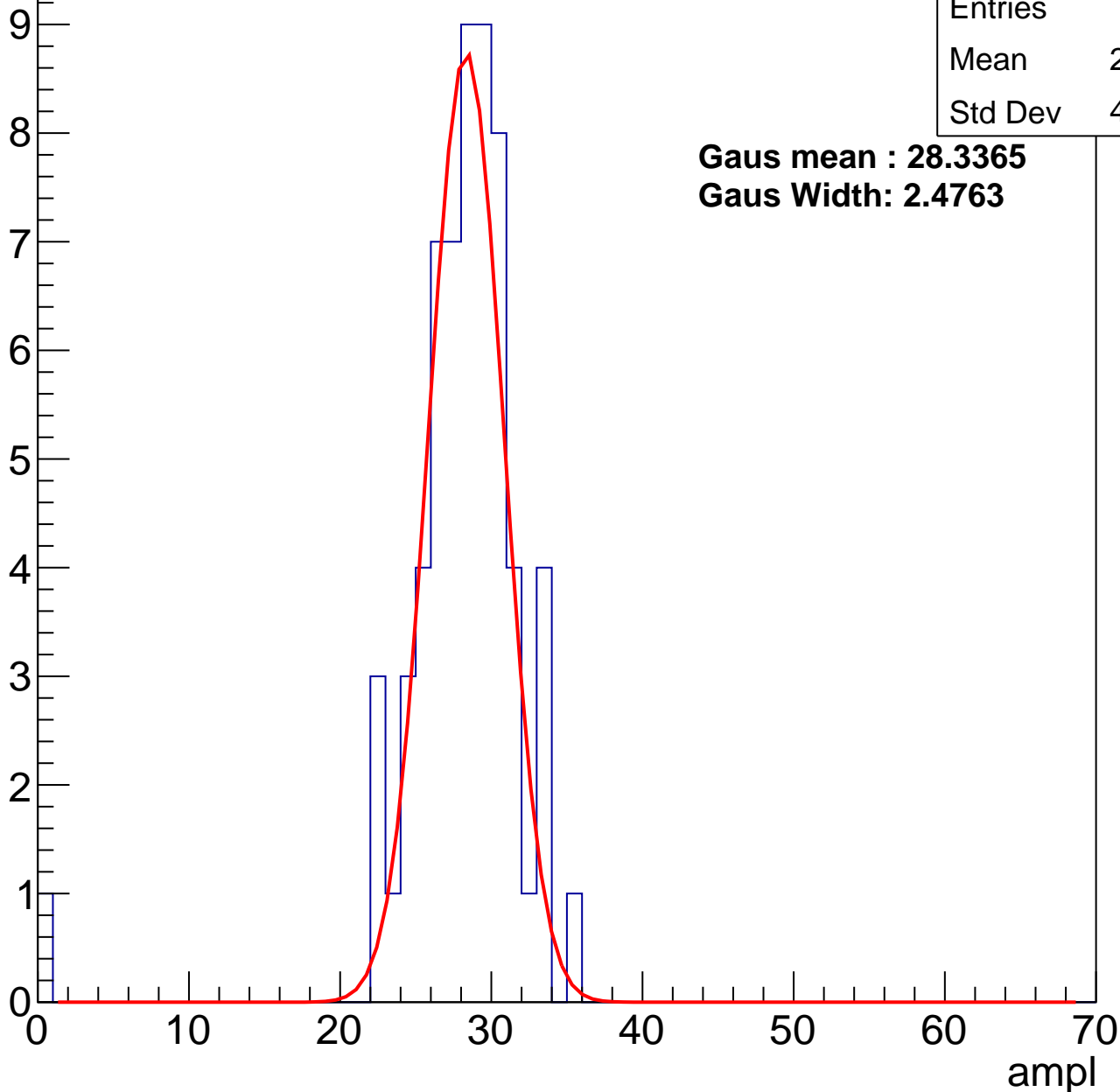
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	62
Mean	27.55
Std Dev	4.518

**Gaus mean : 28.3365**

**Gaus Width: 2.4763**



# B1L100S, U2-ch87, adc1

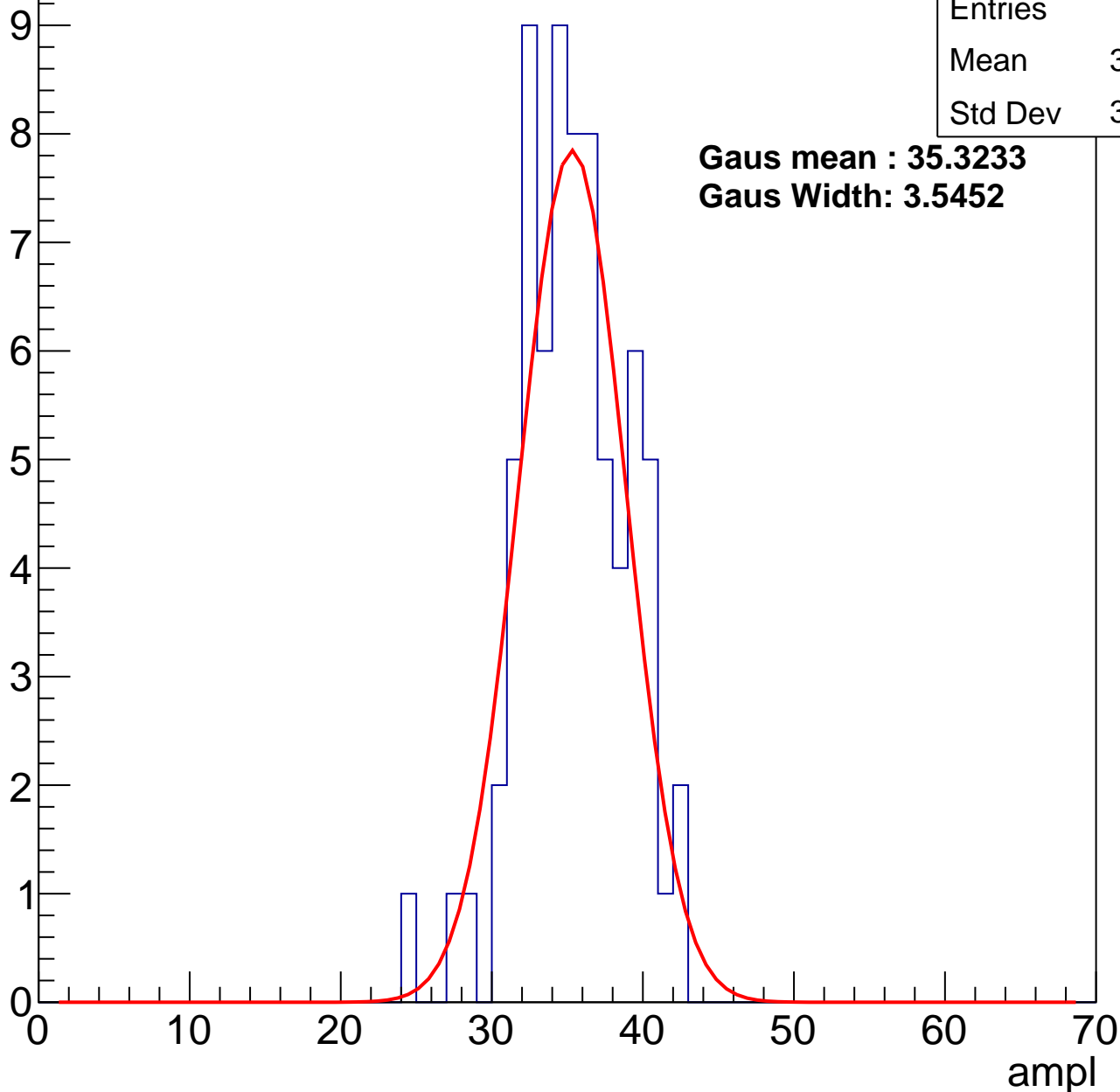
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	73
Mean	34.93
Std Dev	3.505

**Gaus mean : 35.3233**

**Gaus Width: 3.5452**



# B1L100S, U2-ch87, adc2

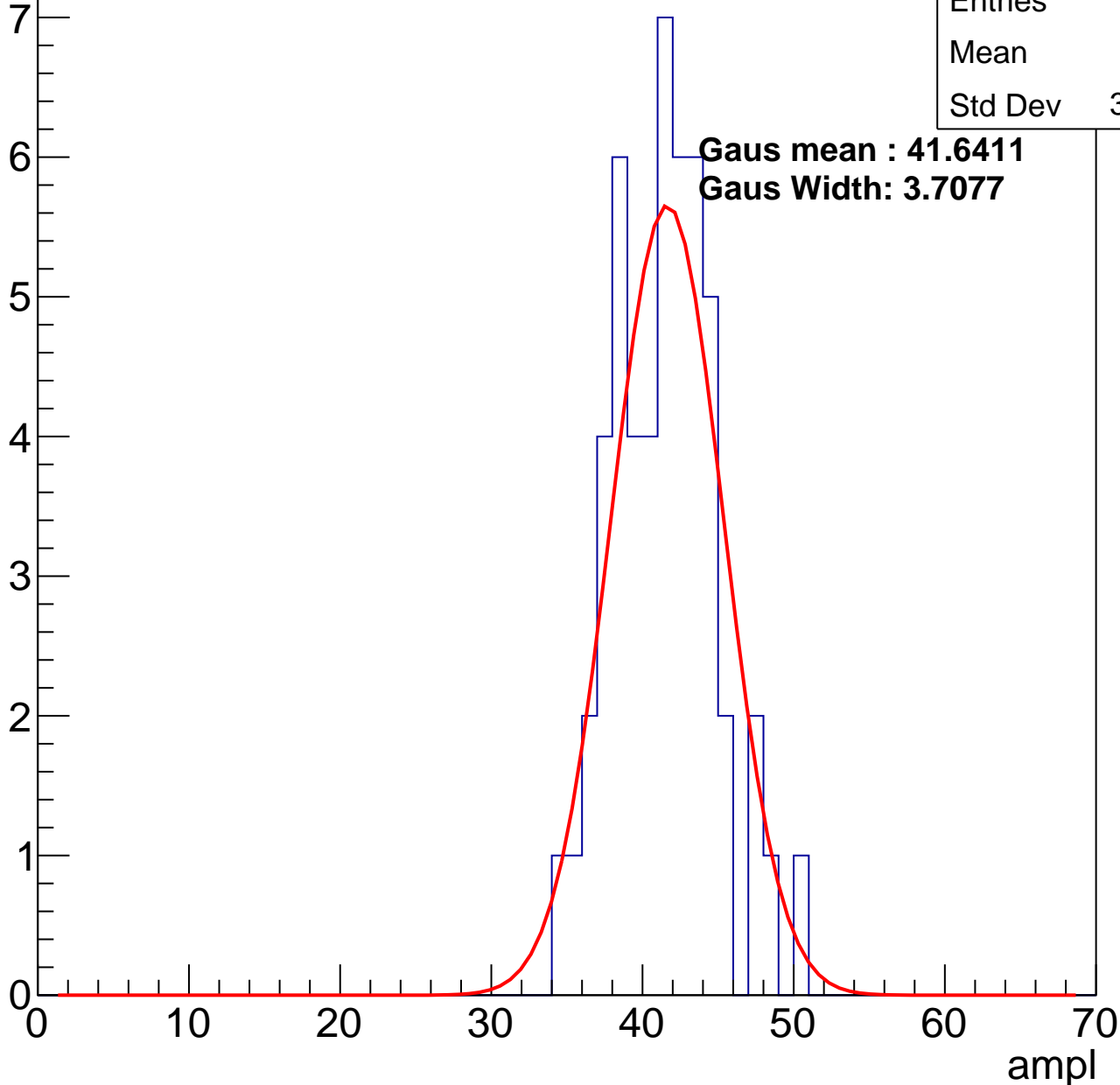
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	52
Mean	41
Std Dev	3.345

**Gaus mean : 41.6411**

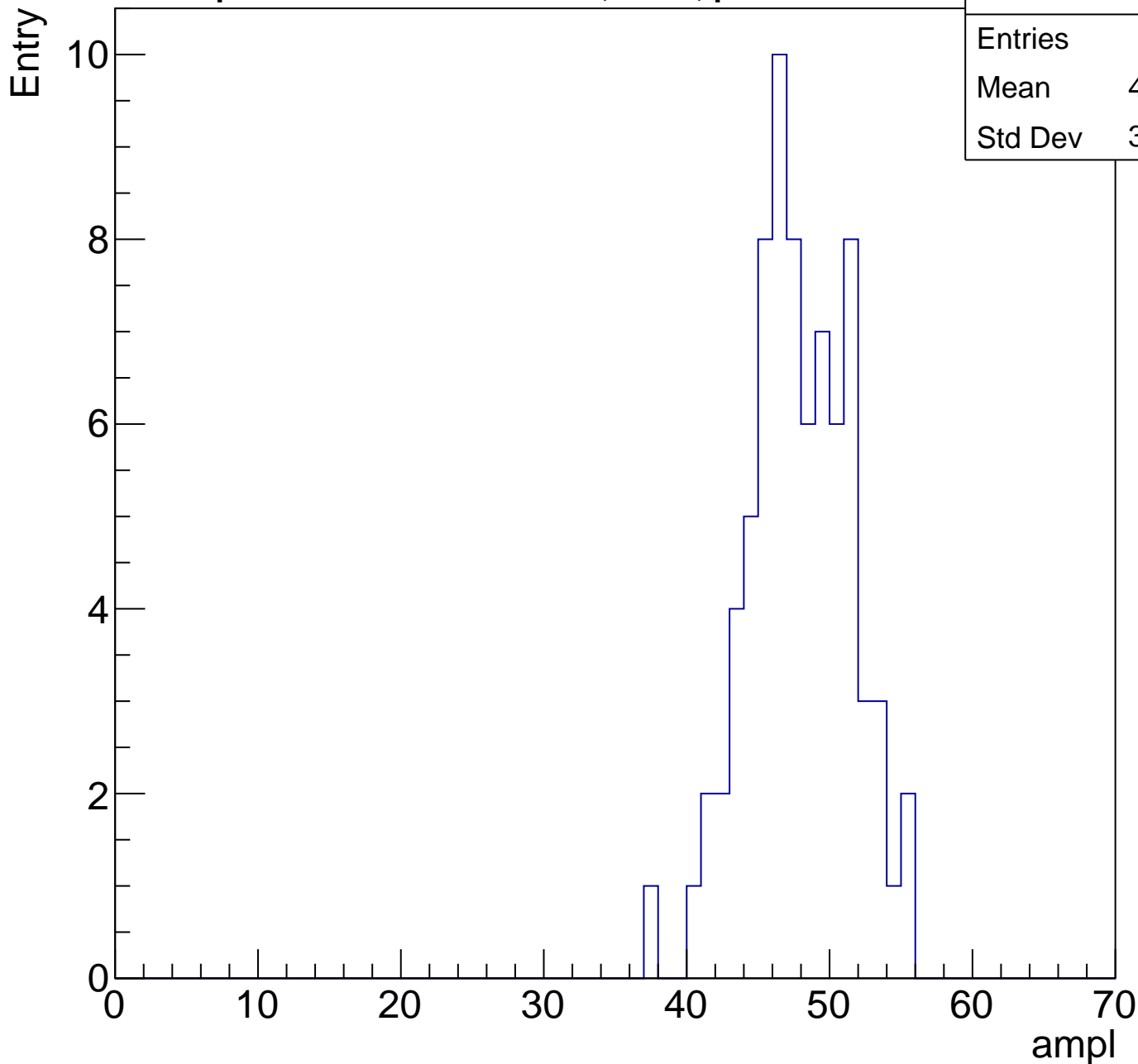
**Gaus Width: 3.7077**



# B1L100S, U2-ch87, adc3

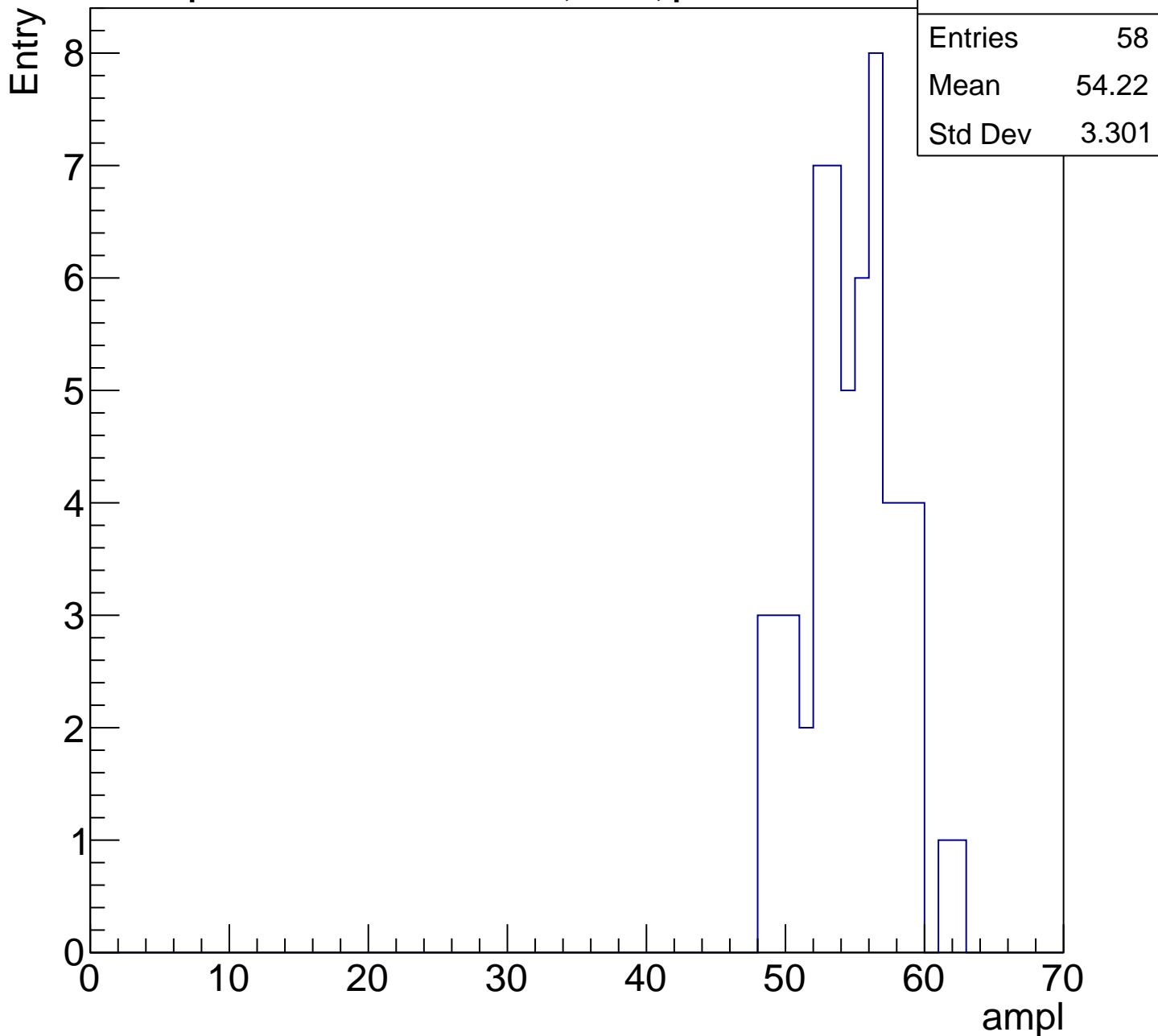
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	77
Mean	47.39
Std Dev	3.579



# B1L100S, U2-ch87, adc4

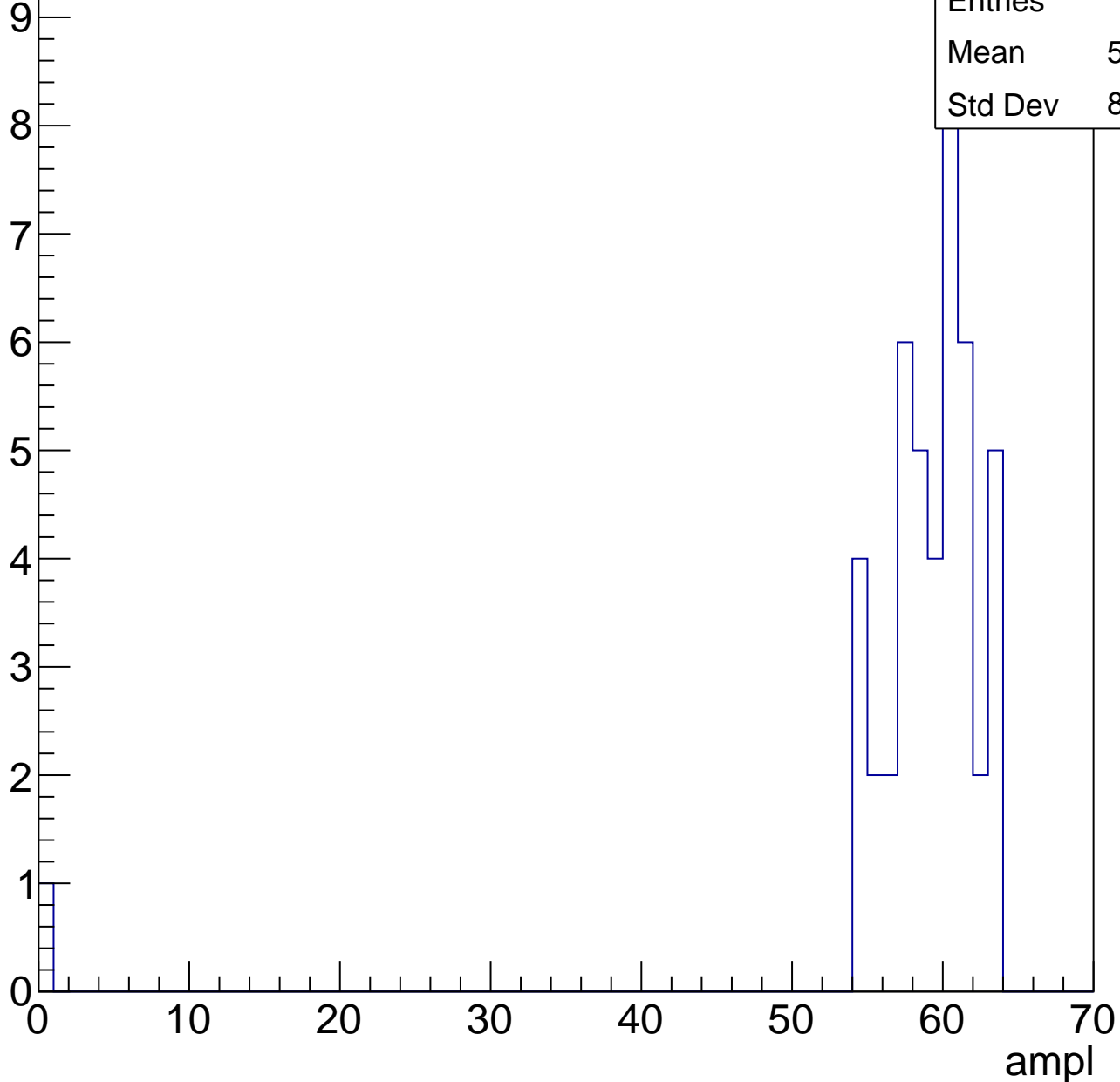
calib\_packv5\_042523\_0143.root, FC#4, port A2



# B1L100S, U2-ch87, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

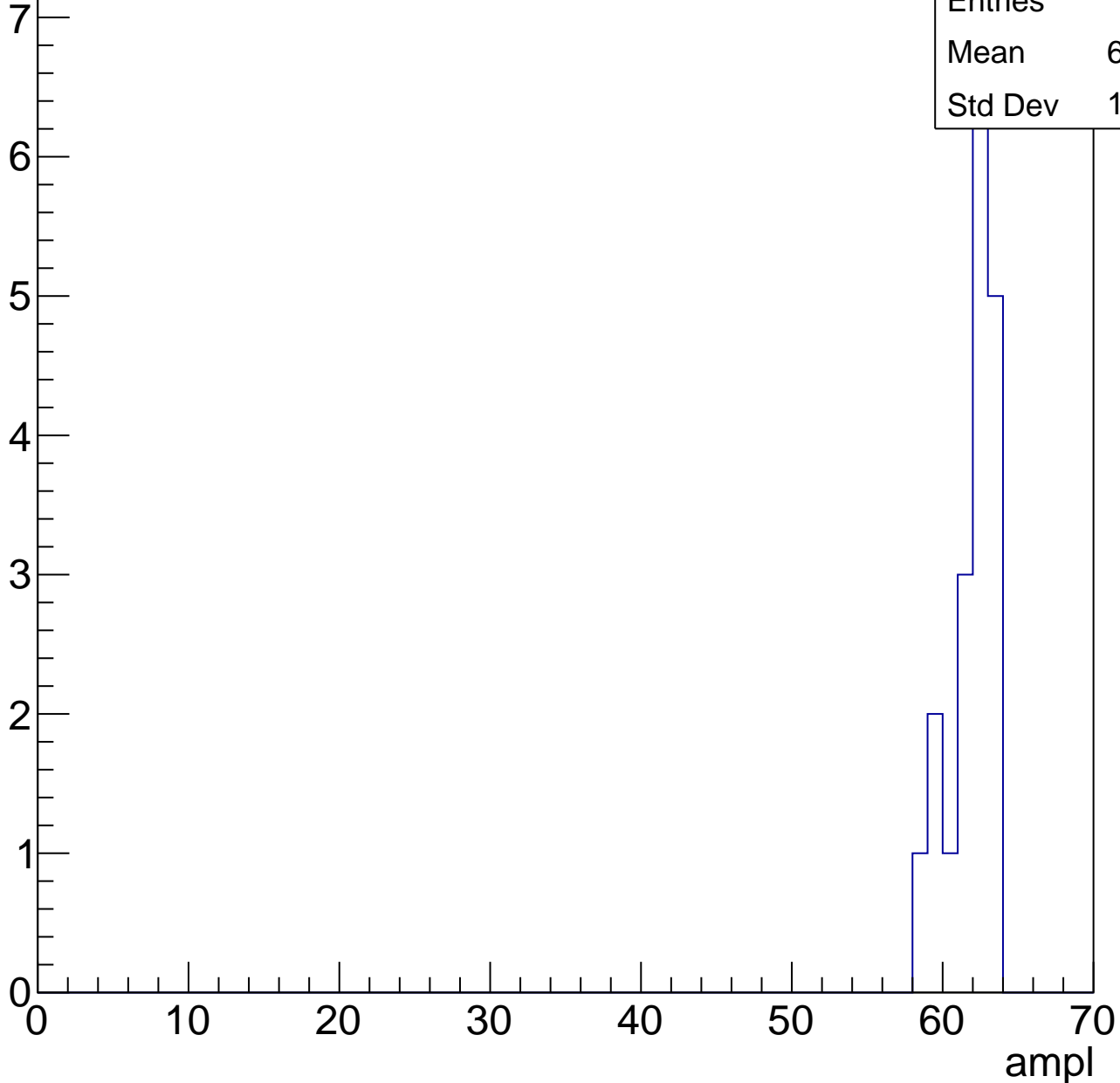


# B1L100S, U2-ch87, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	19
Mean	61.47
Std Dev	1.464

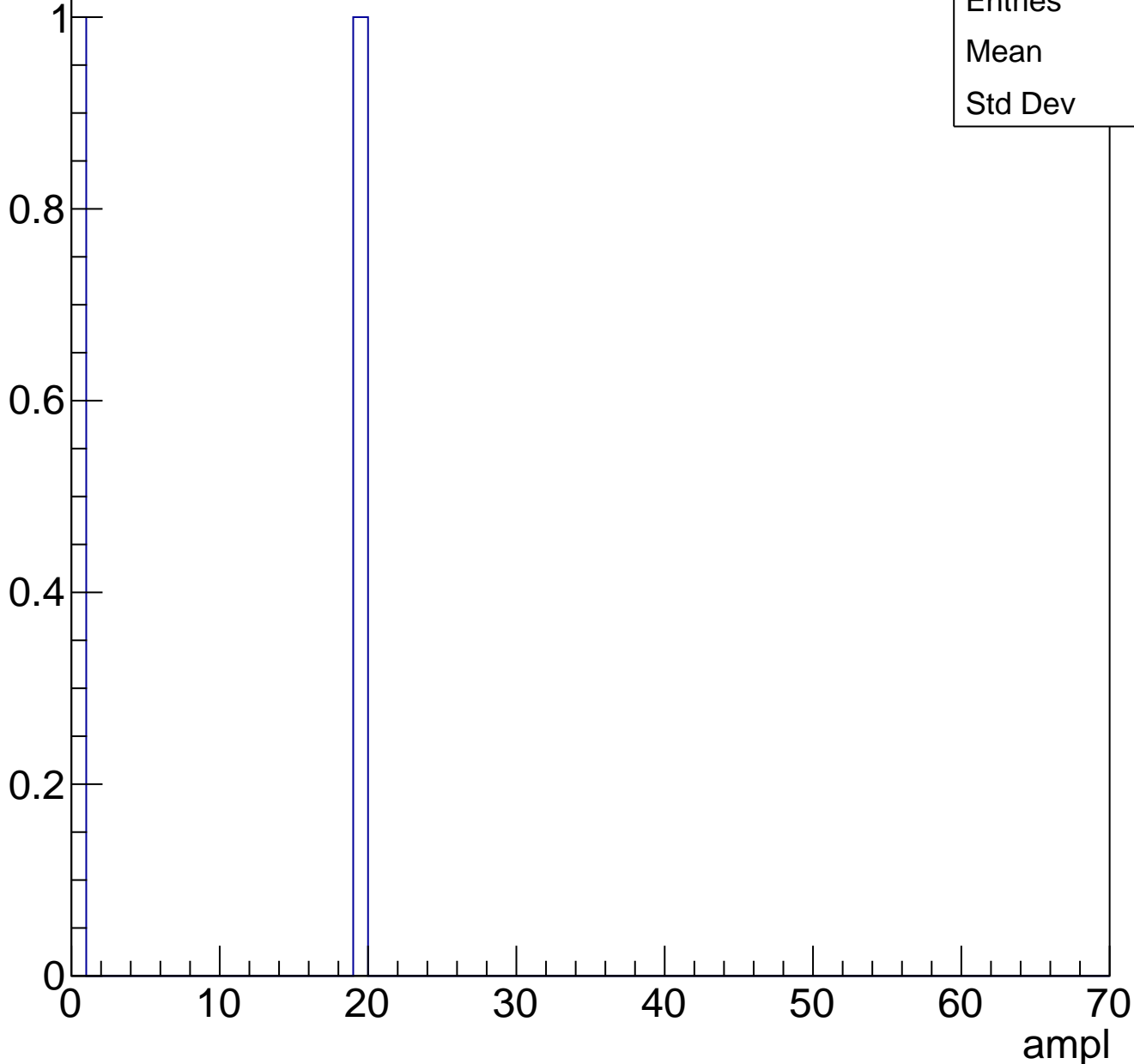




# B1L100S, U2-ch87, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



# B1L100S, U2-ch88, adc0

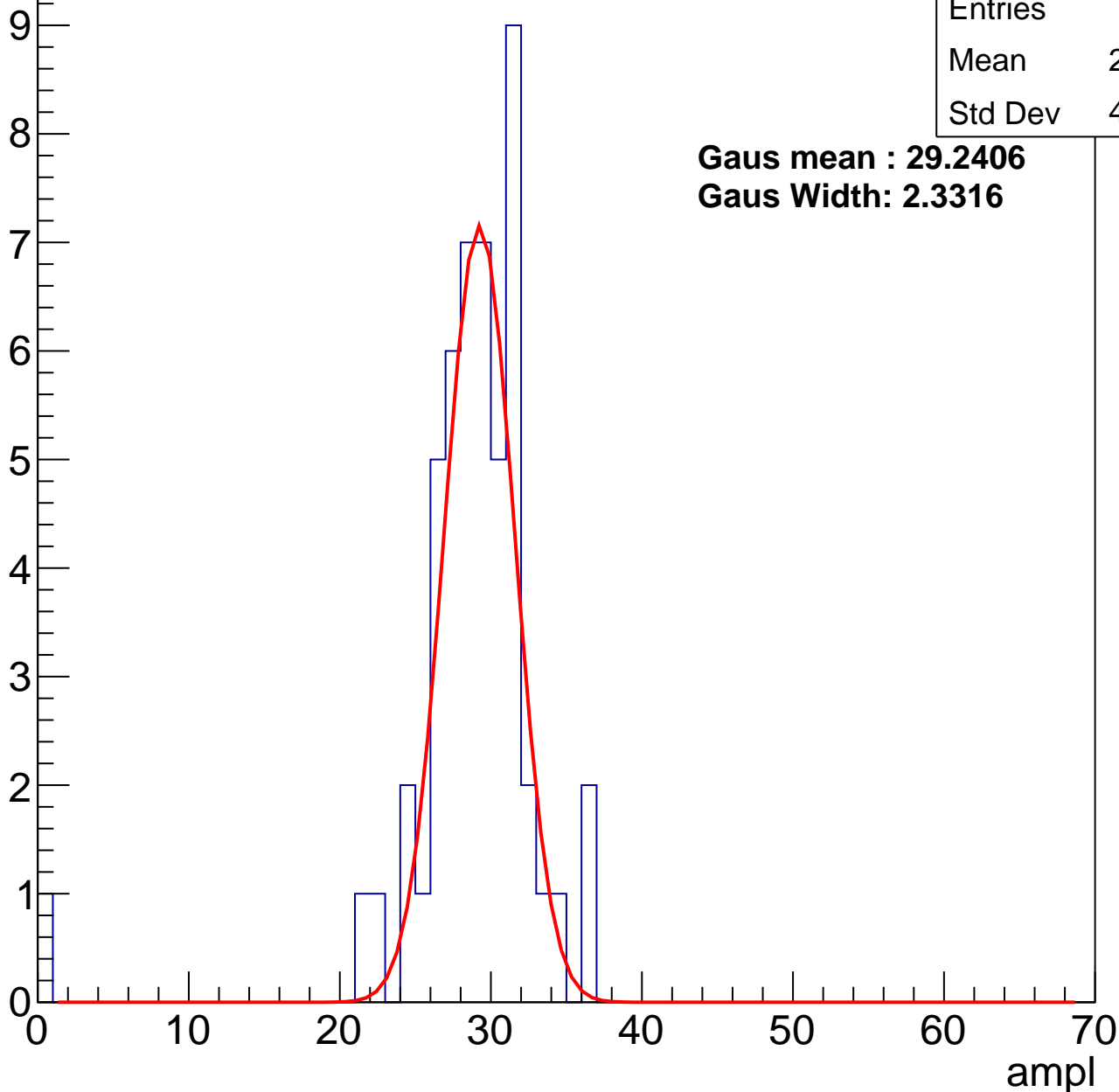
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	51
Mean	28.22
Std Dev	4.976

**Gaus mean : 29.2406**

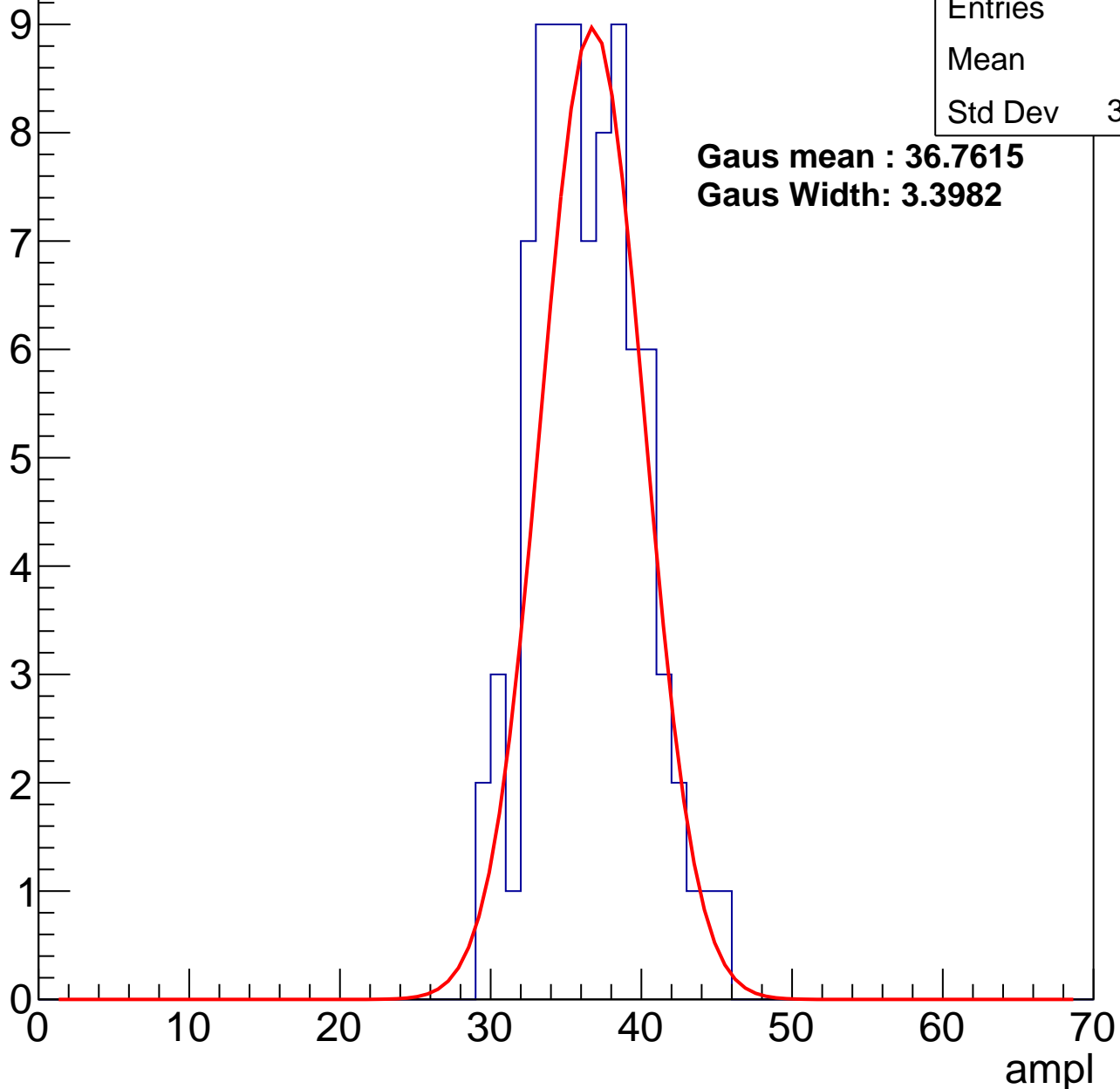
**Gaus Width: 2.3316**



# B1L100S, U2-ch88, adc1

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	84
Mean	36
Std Dev	3.457

# B1L100S, U2-ch88, adc2

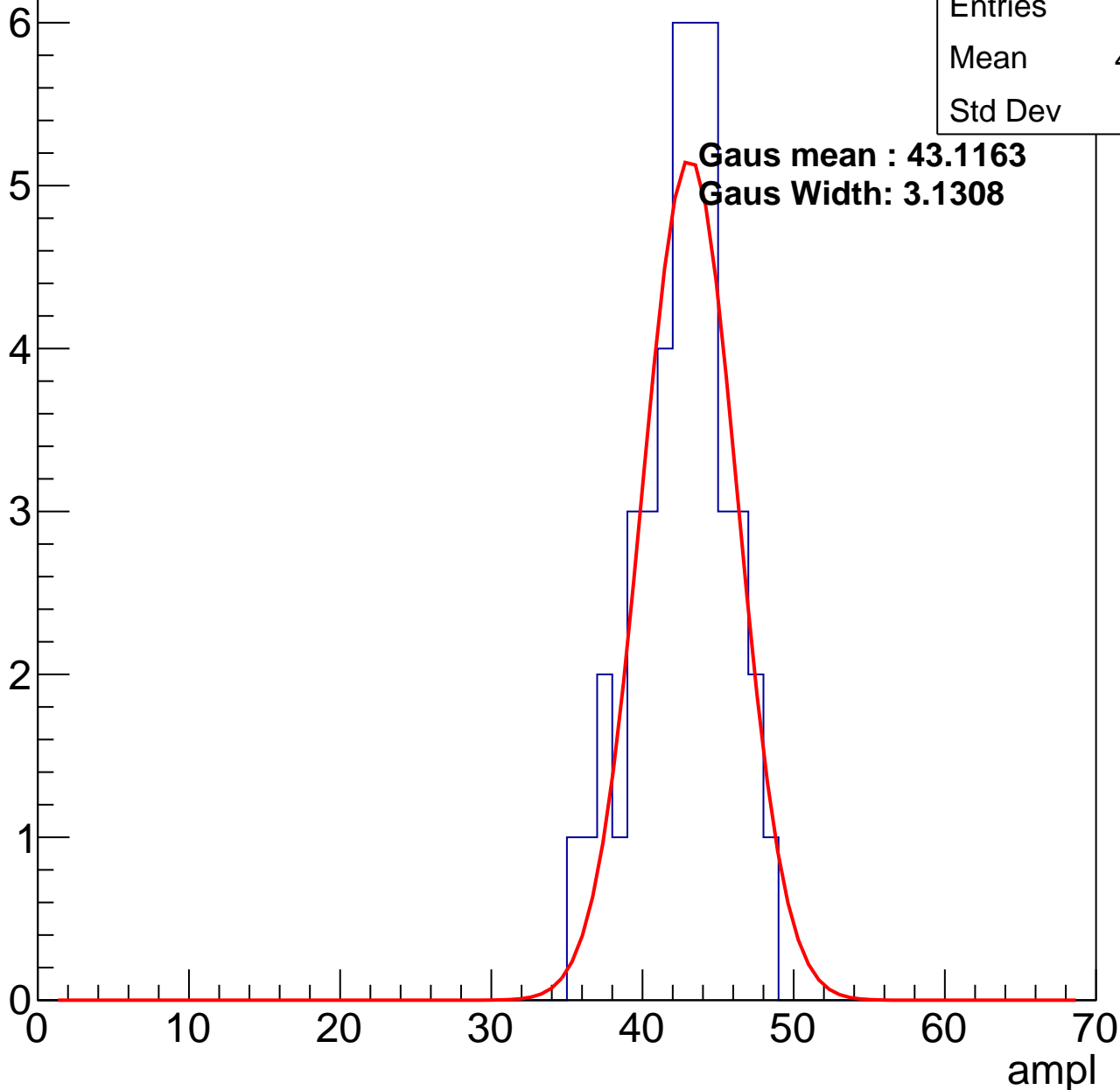
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	42
Mean	42.21
Std Dev	3.02

**Gaus mean : 43.163**

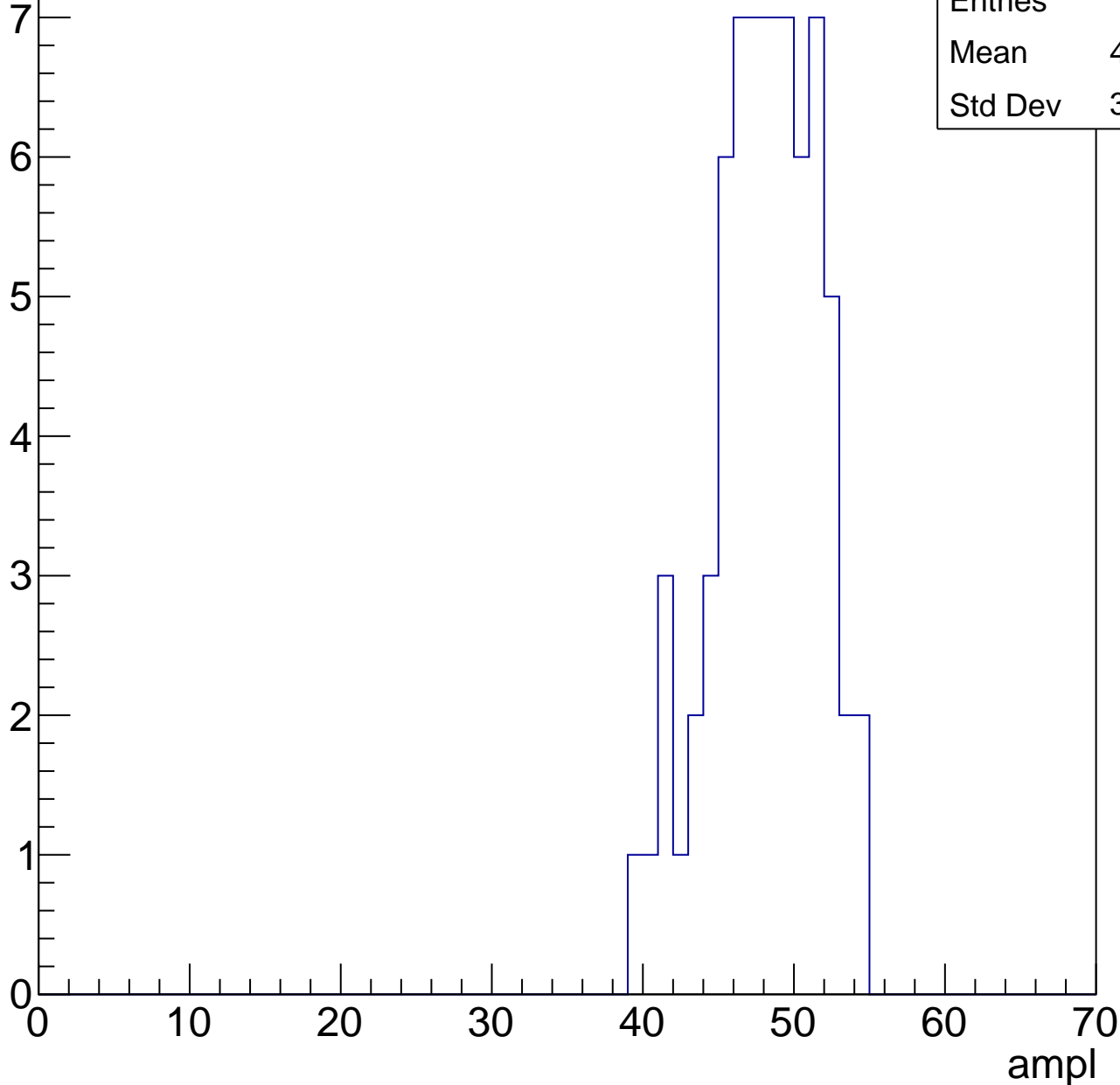
**Gaus Width: 3.1308**



# B1L100S, U2-ch88, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

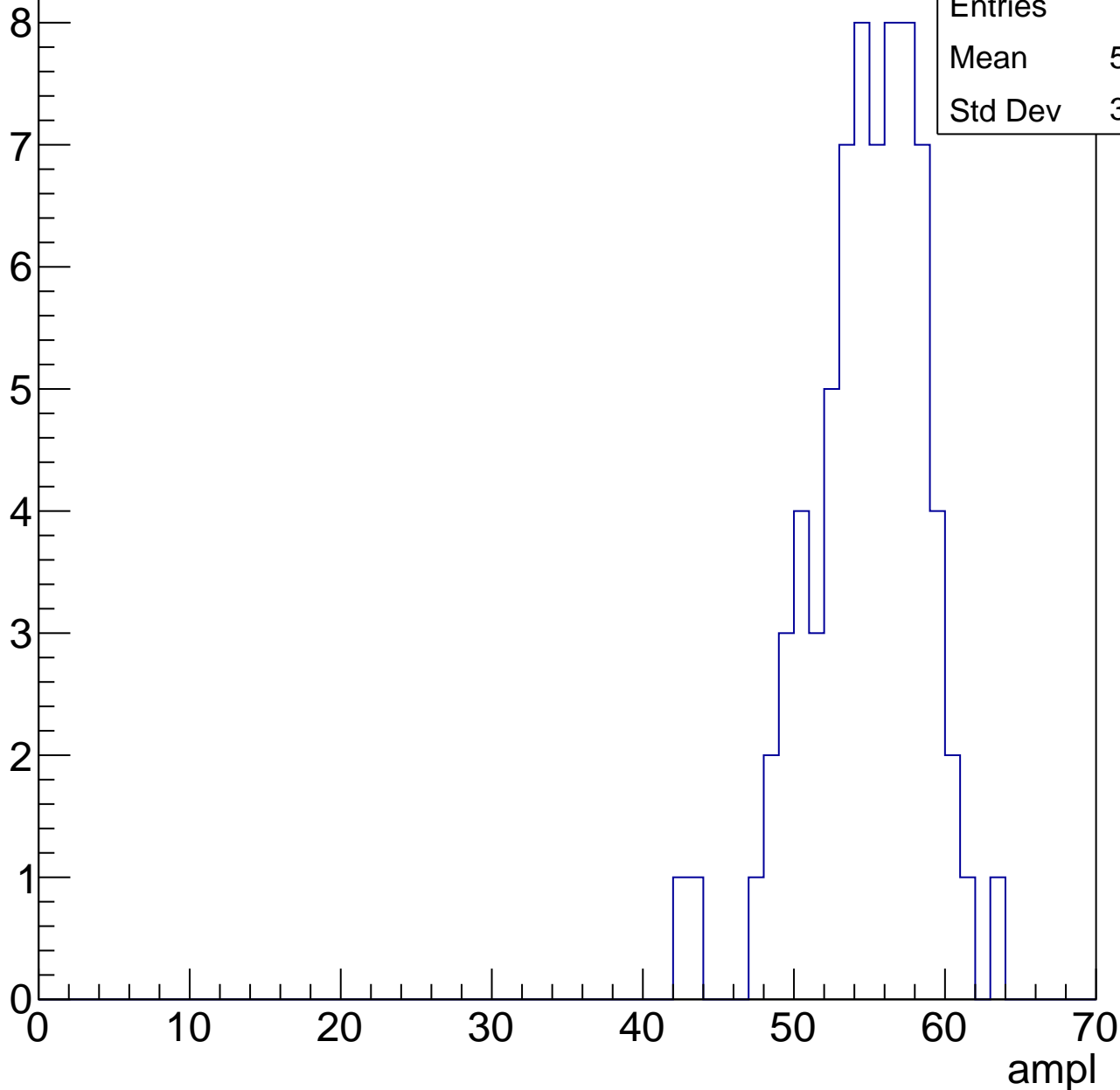


Entries	67
Mean	47.66
Std Dev	3.462

# B1L100S, U2-ch88, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

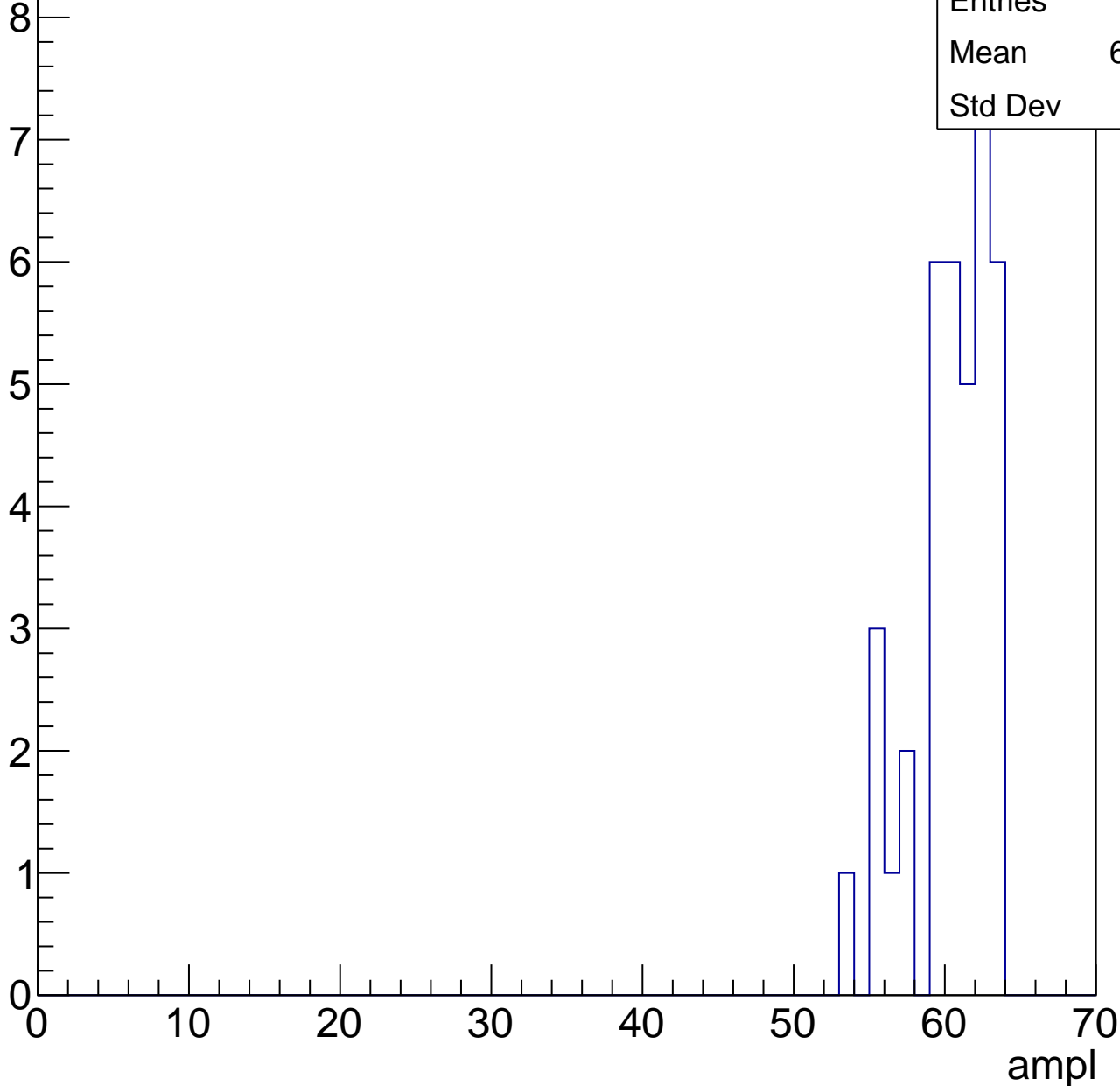


# B1L100S, U2-ch88, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

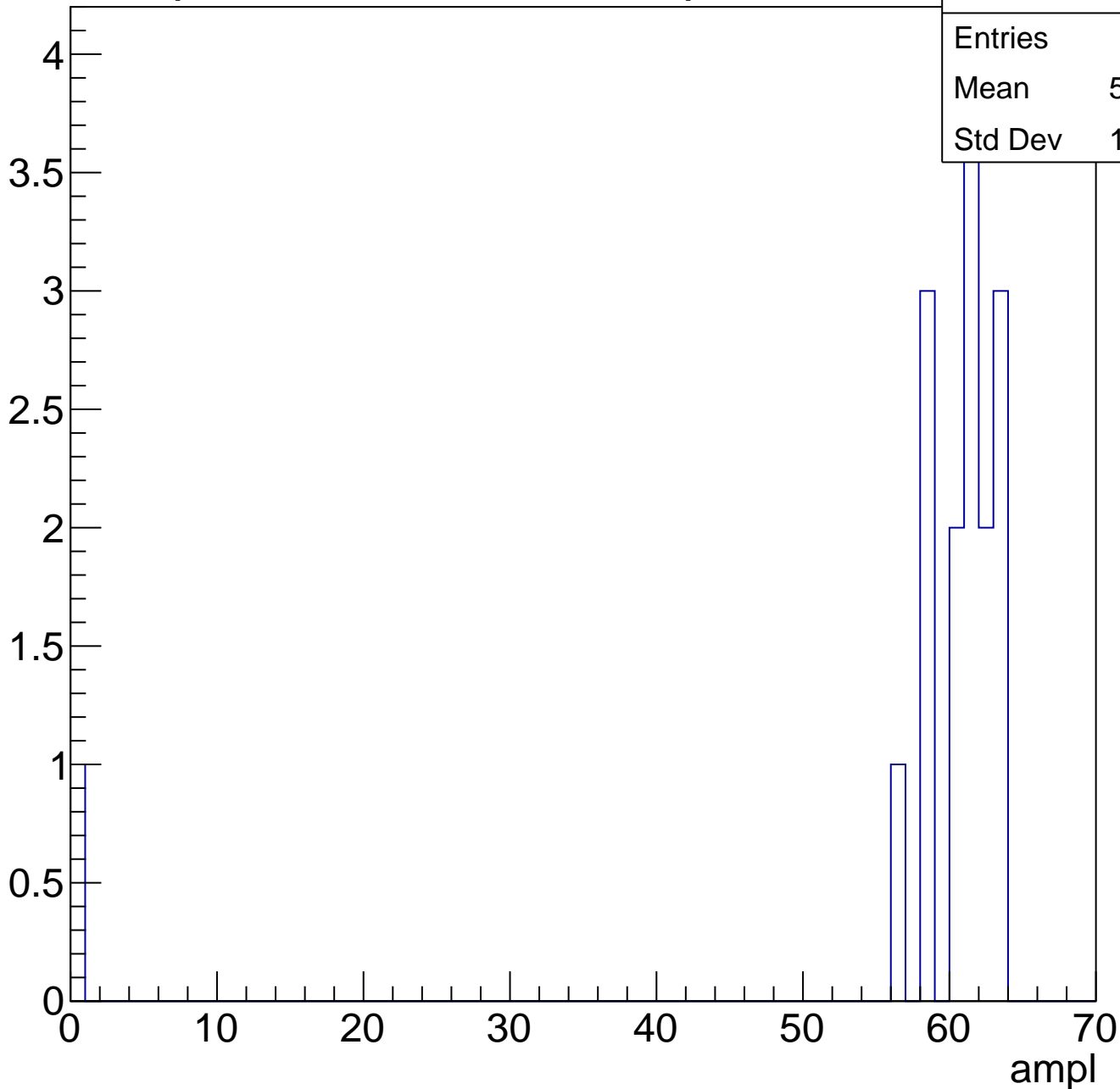
Entries	38
Mean	60.03
Std Dev	2.59



# B1L100S, U2-ch88, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry





# B1L100S, U2-ch88, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L100S, U2-ch89, adc0

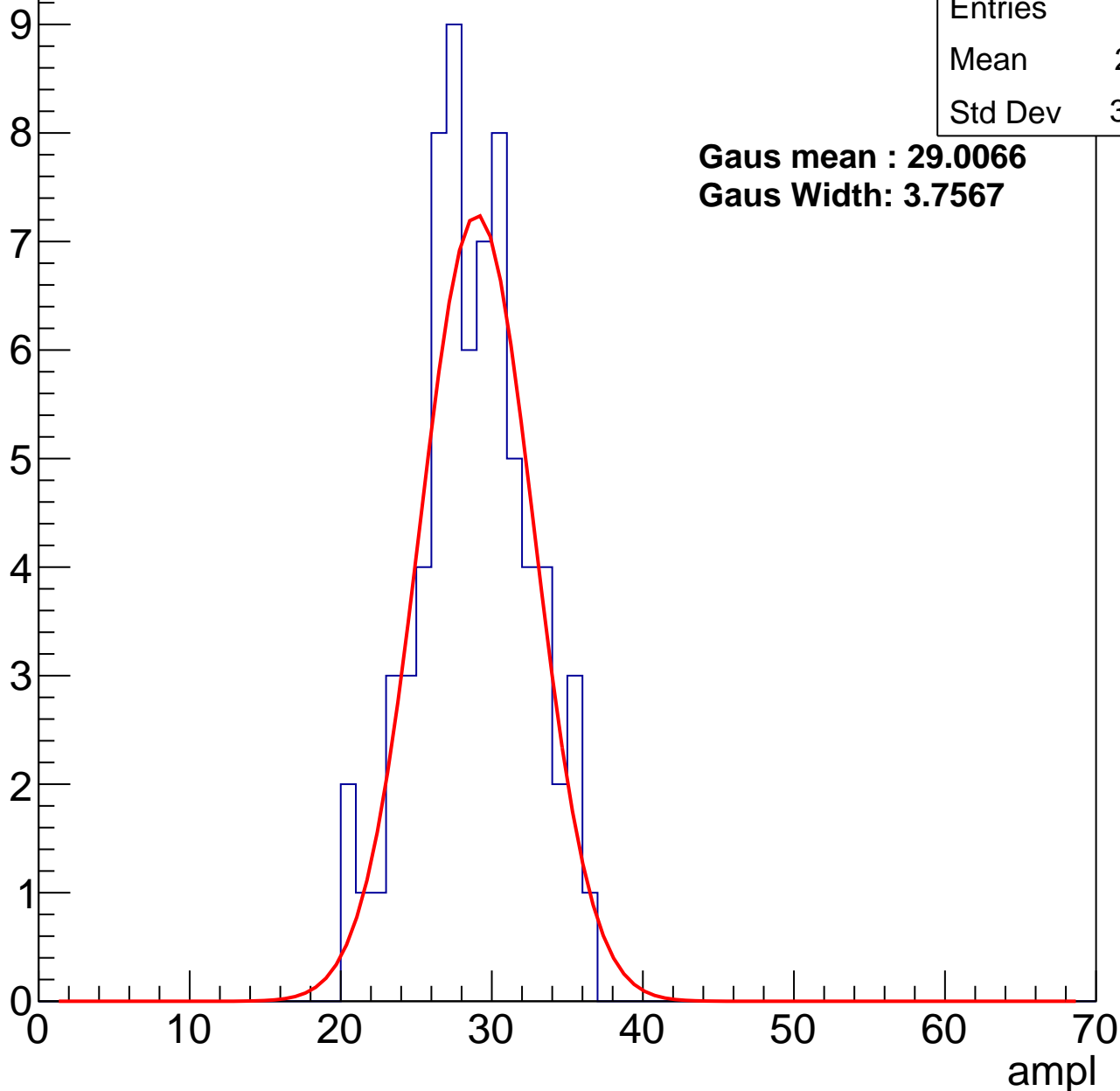
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	71
Mean	28.31
Std Dev	3.633

**Gaus mean : 29.0066**

**Gaus Width: 3.7567**



# B1L100S, U2-ch89, adc1

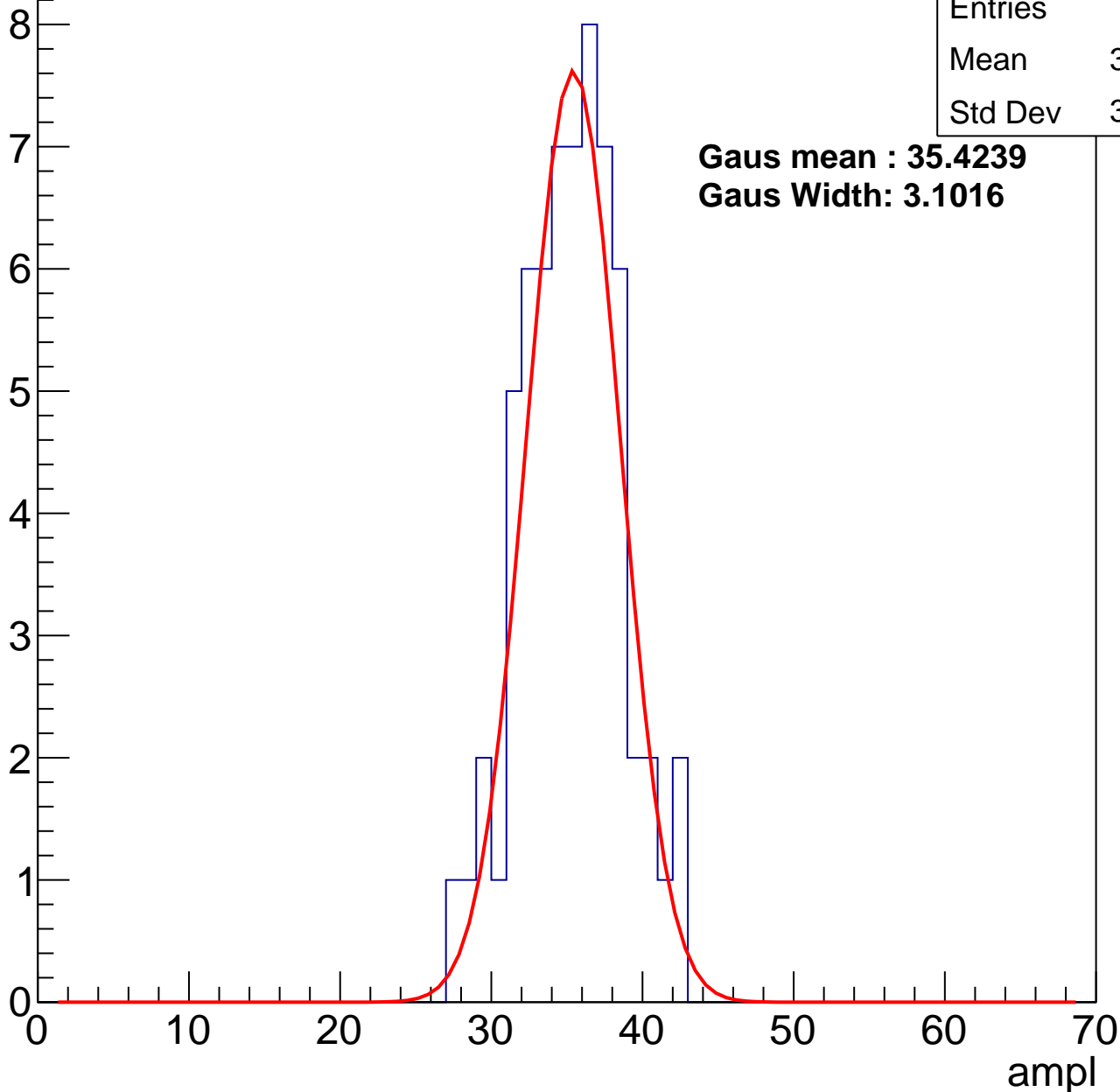
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	64
Mean	34.83
Std Dev	3.257

**Gaus mean : 35.4239**

**Gaus Width: 3.1016**



# B1L100S, U2-ch89, adc2

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

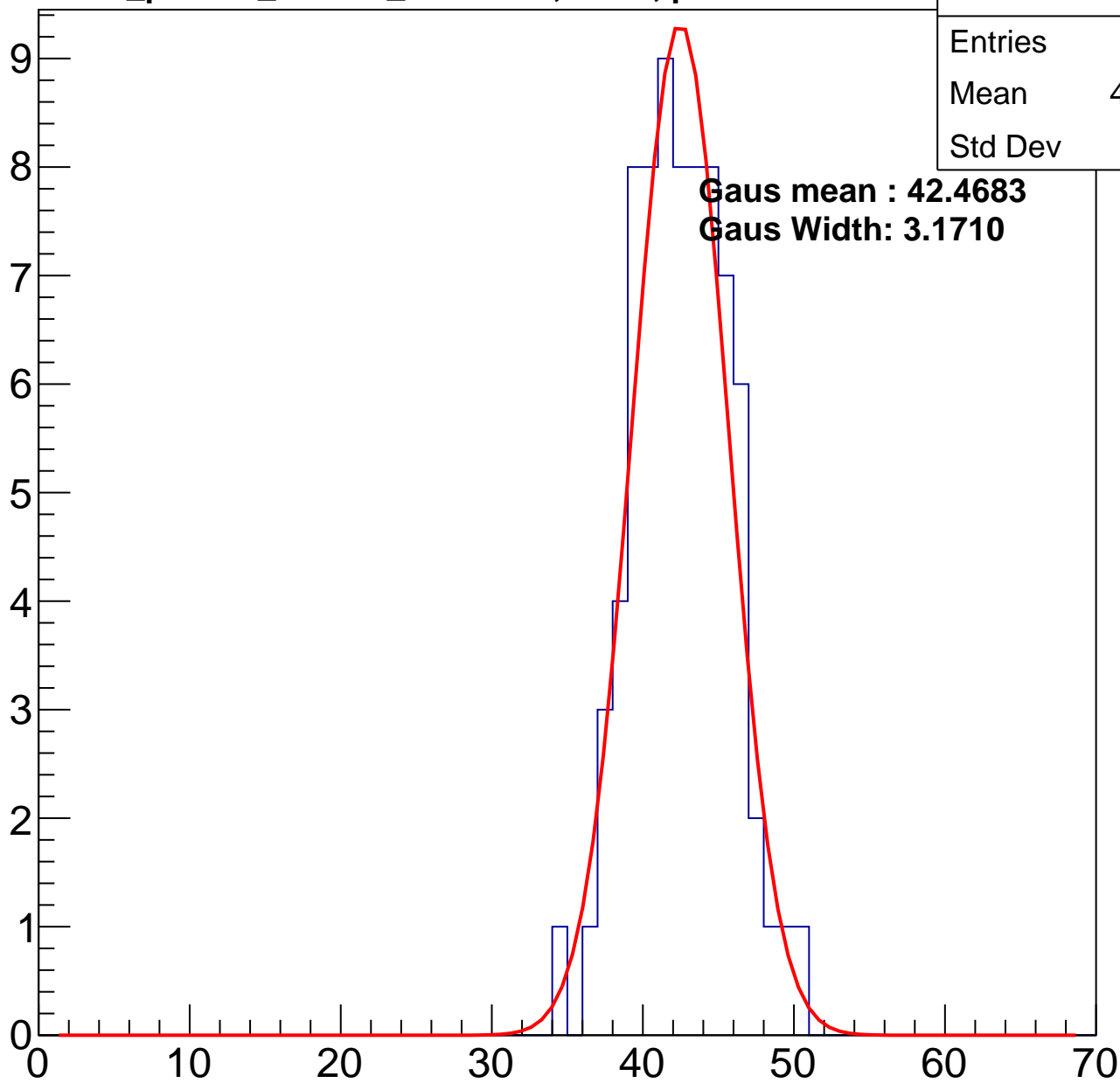
9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	76
Mean	42.08
Std Dev	3.14

**Gaus mean : 42.4683**

**Gaus Width: 3.1710**

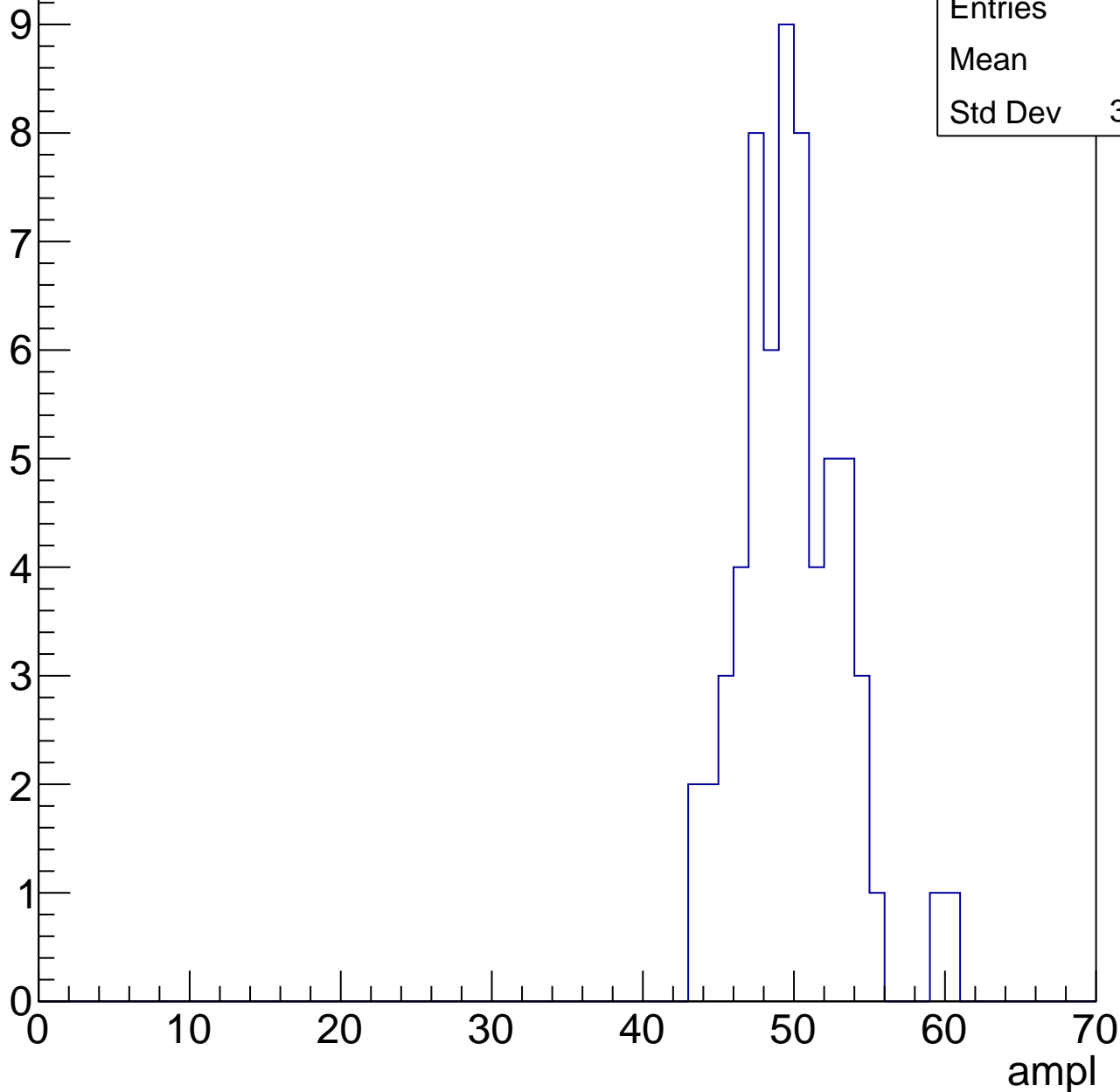
ampl



# B1L100S, U2-ch89, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

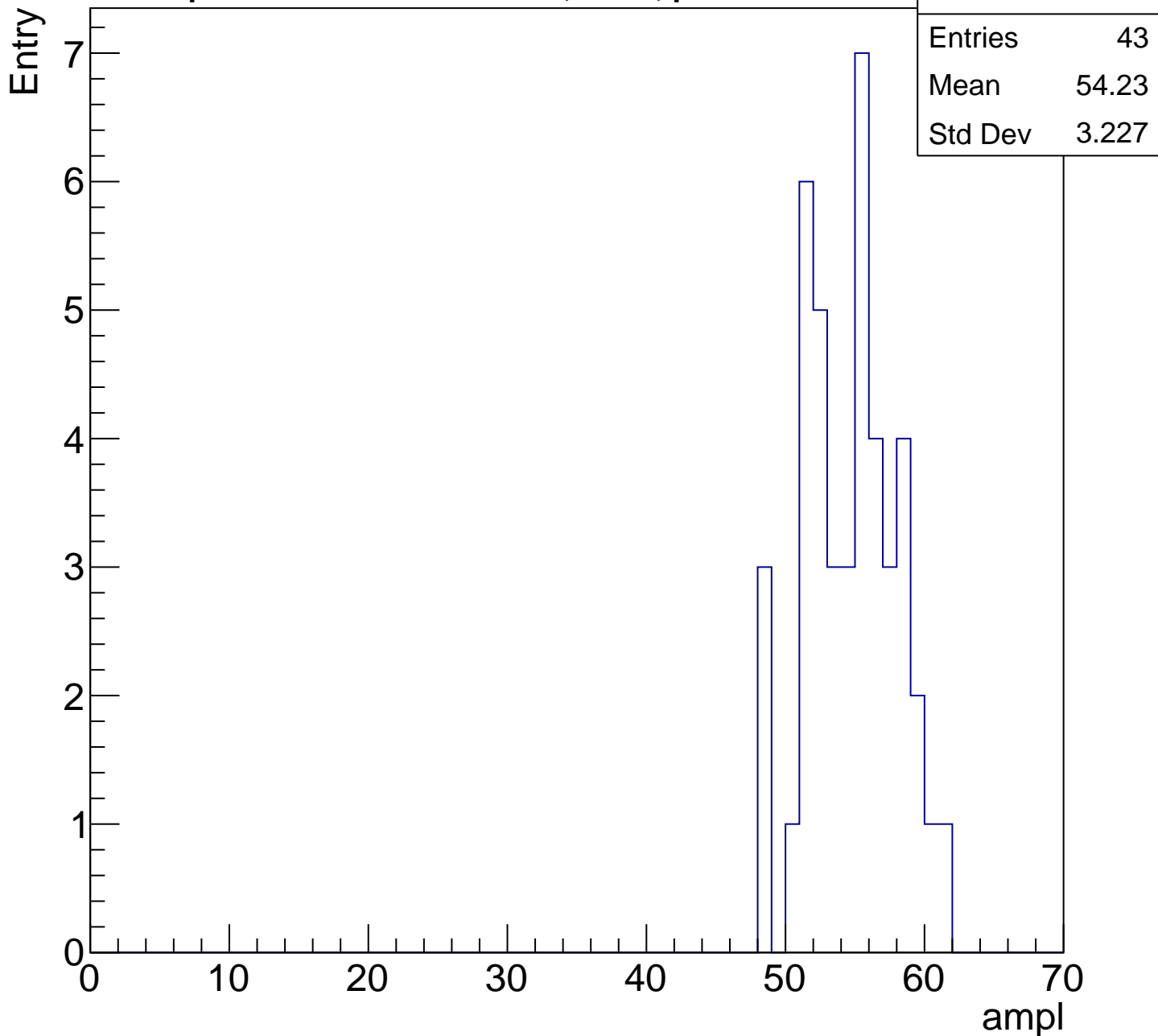
Entry



Entries	62
Mean	49.4
Std Dev	3.396

# B1L100S, U2-ch89, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2



# B1L100S, U2-ch89, adc5

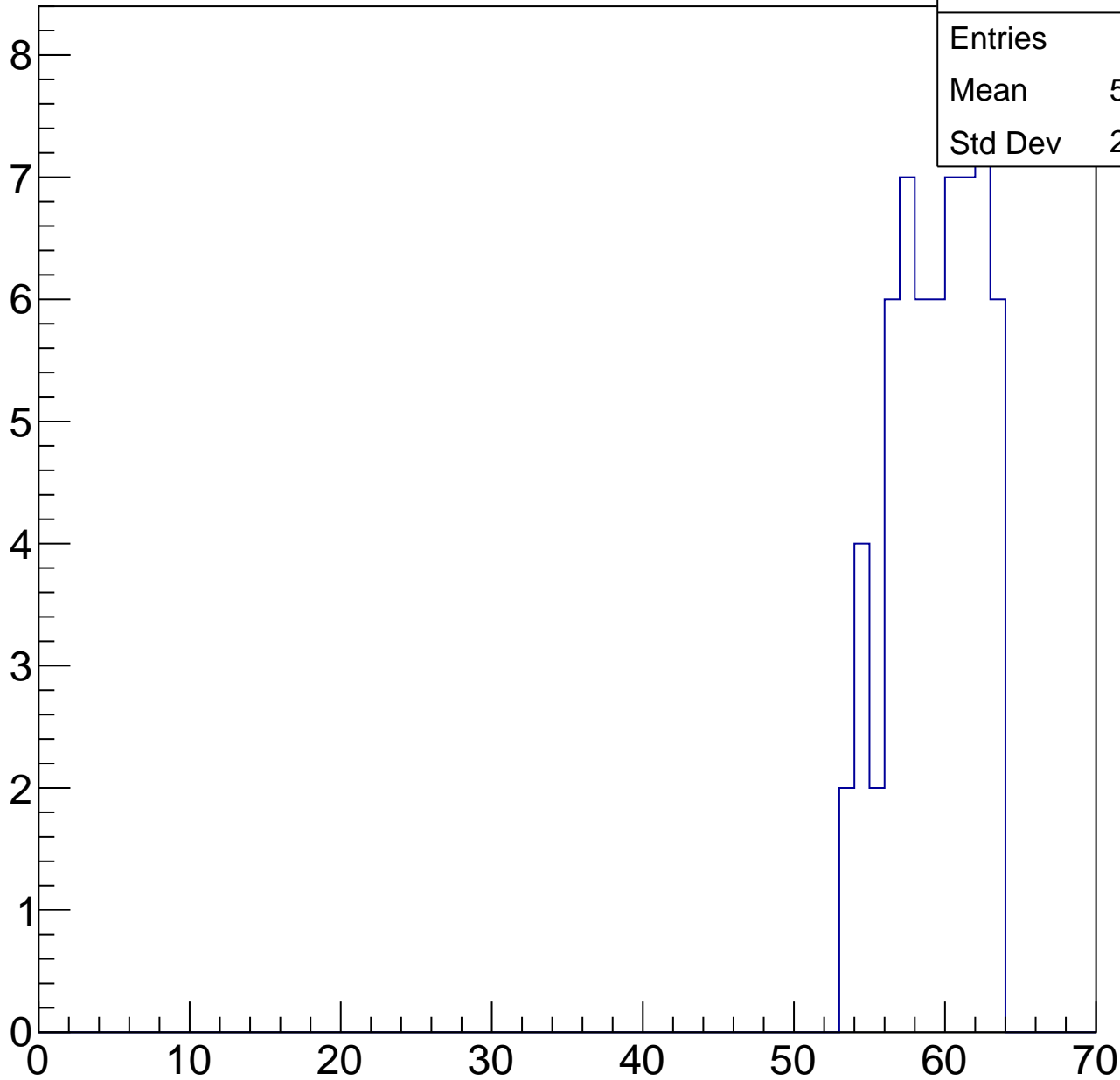
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	61
Mean	58.85
Std Dev	2.845

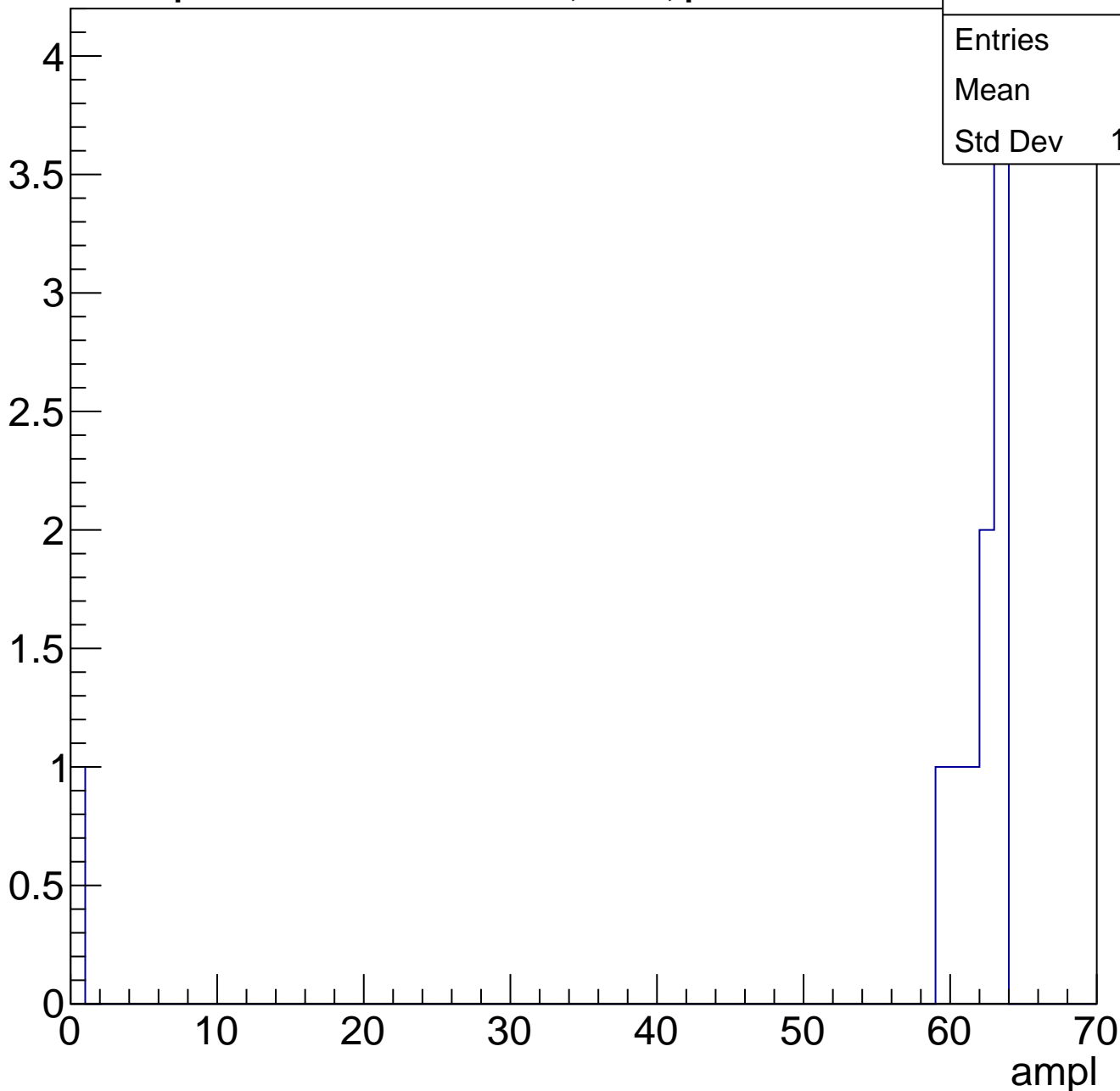
ampl



# B1L100S, U2-ch89, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

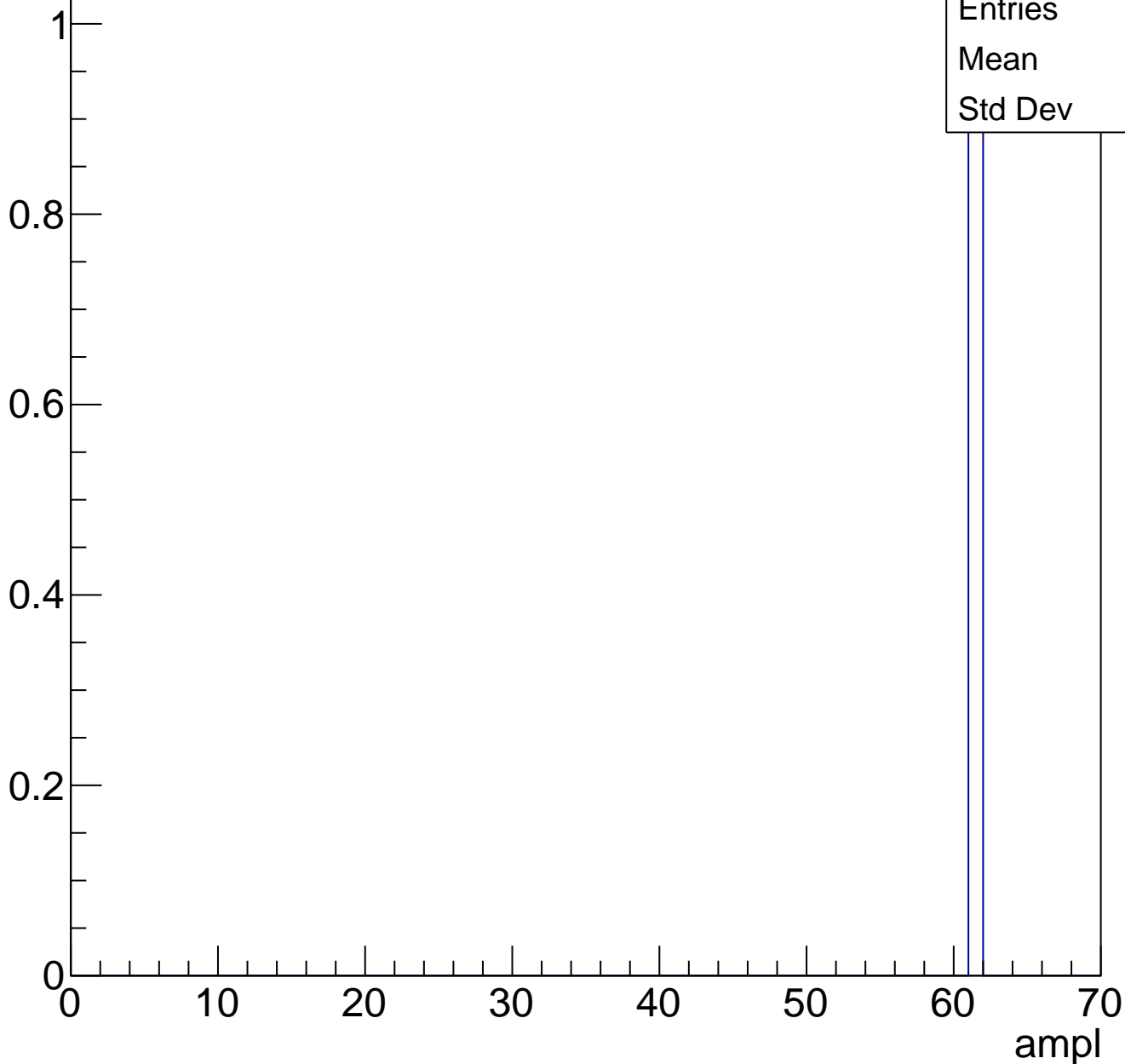




# B1L100S, U2-ch89, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



# B1L100S, U2-ch90, adc0

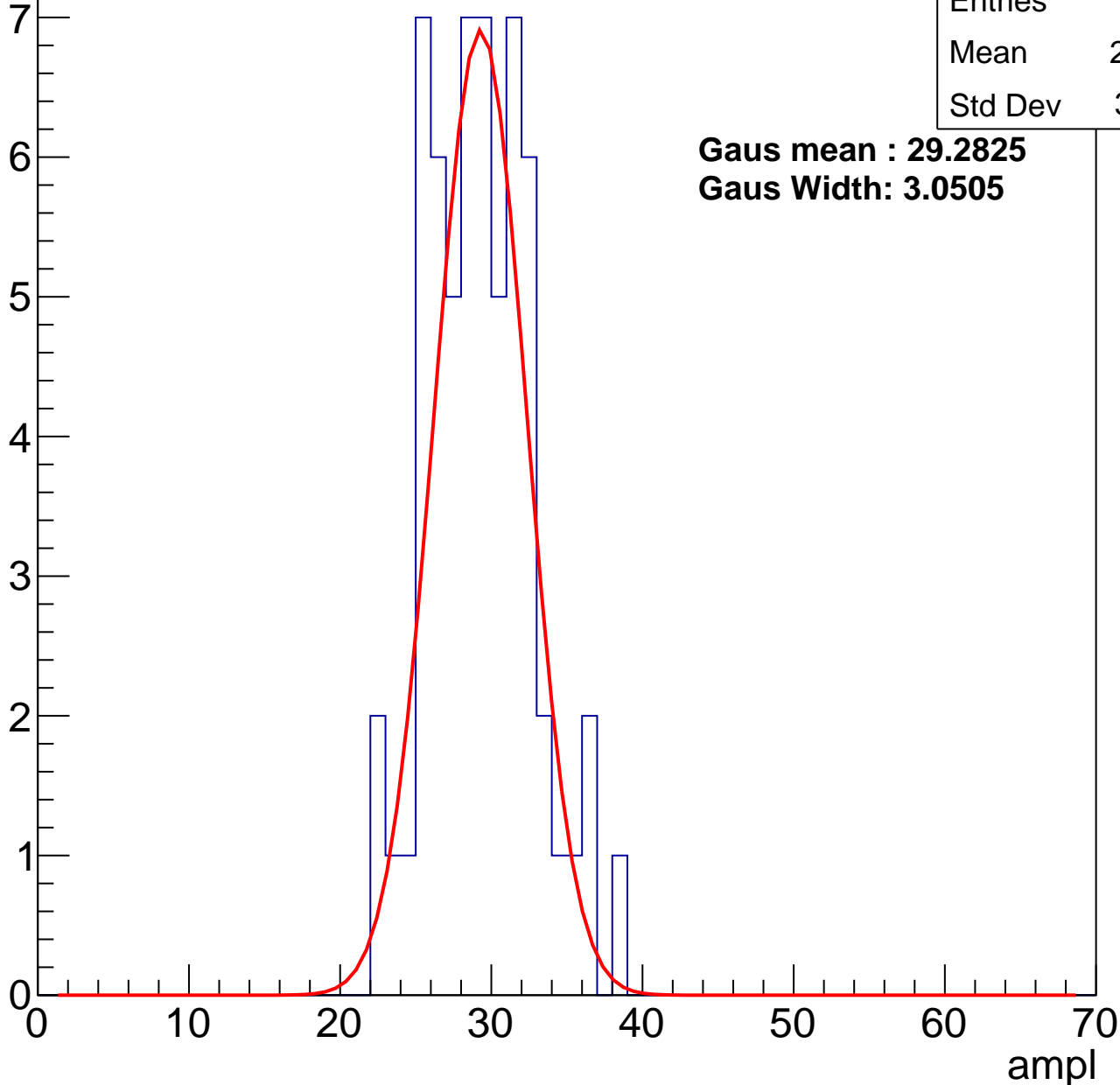
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	61
Mean	28.85
Std Dev	3.411

**Gaus mean : 29.2825**

**Gaus Width: 3.0505**



# B1L100S, U2-ch90, adc1

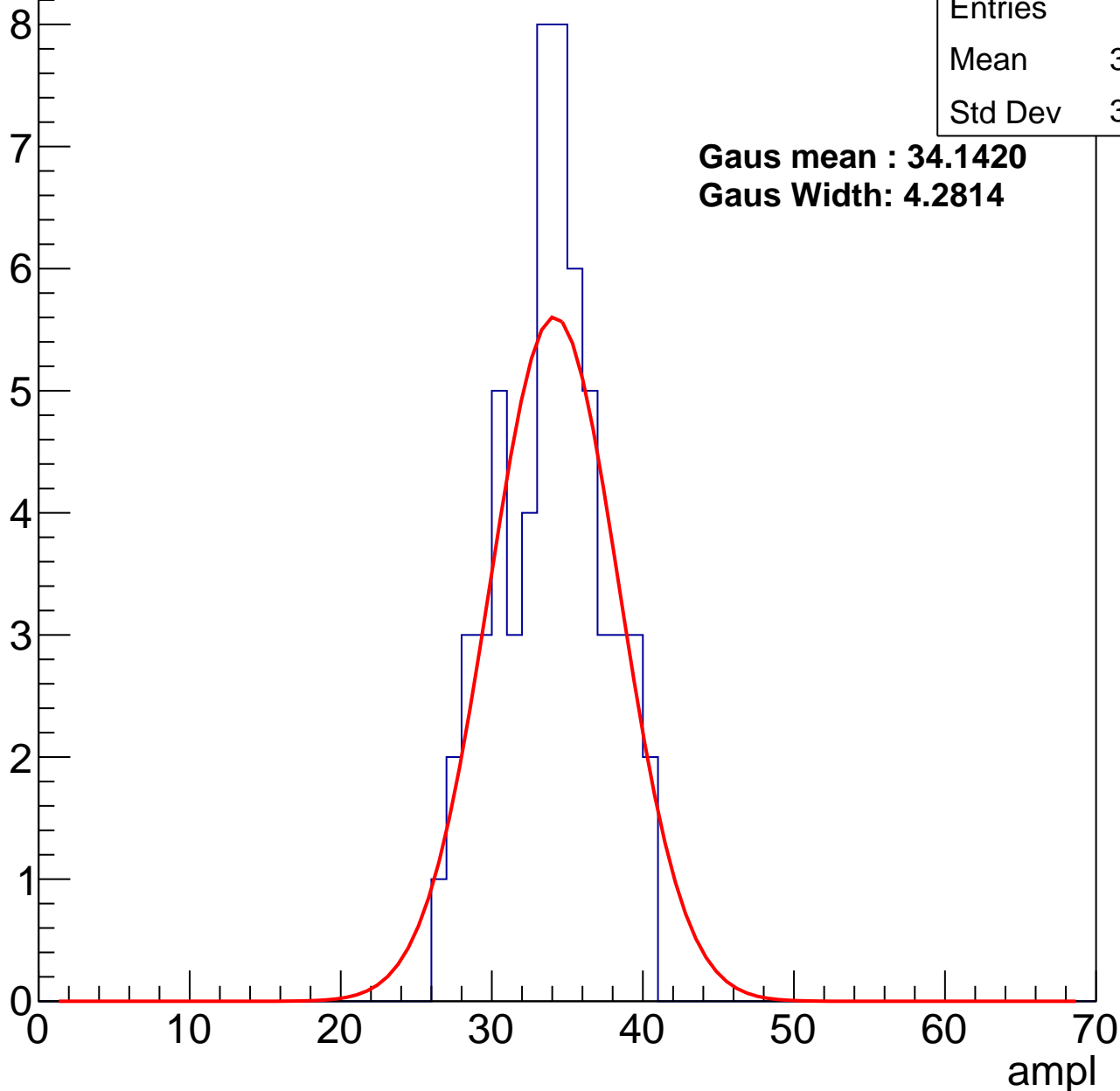
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	59
Mean	33.39
Std Dev	3.449

**Gaus mean : 34.1420**

**Gaus Width: 4.2814**



# B1L100S, U2-ch90, adc2

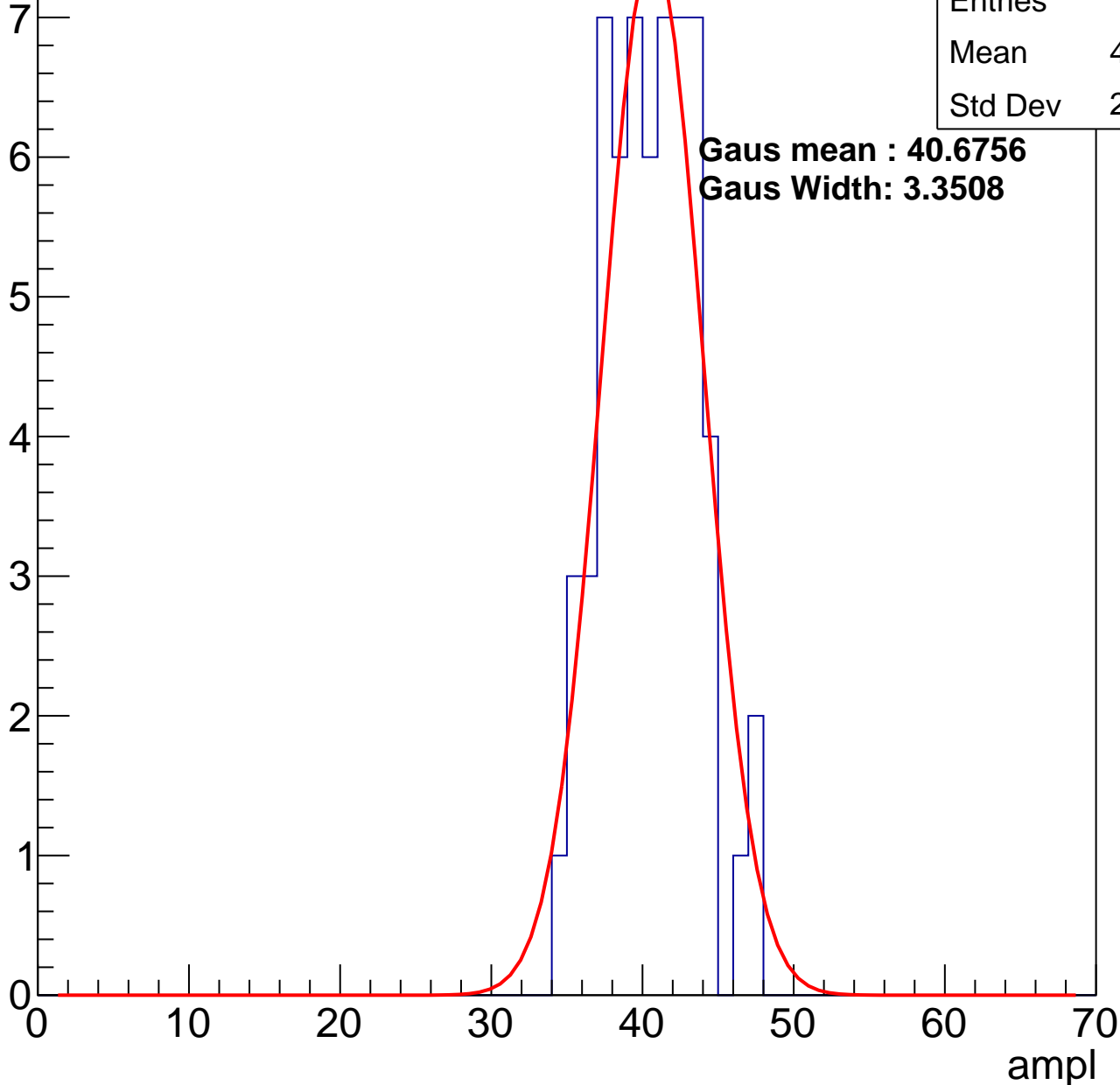
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	61
Mean	40.08
Std Dev	2.999

**Gaus mean : 40.6756**

**Gaus Width: 3.3508**



# B1L100S, U2-ch90, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

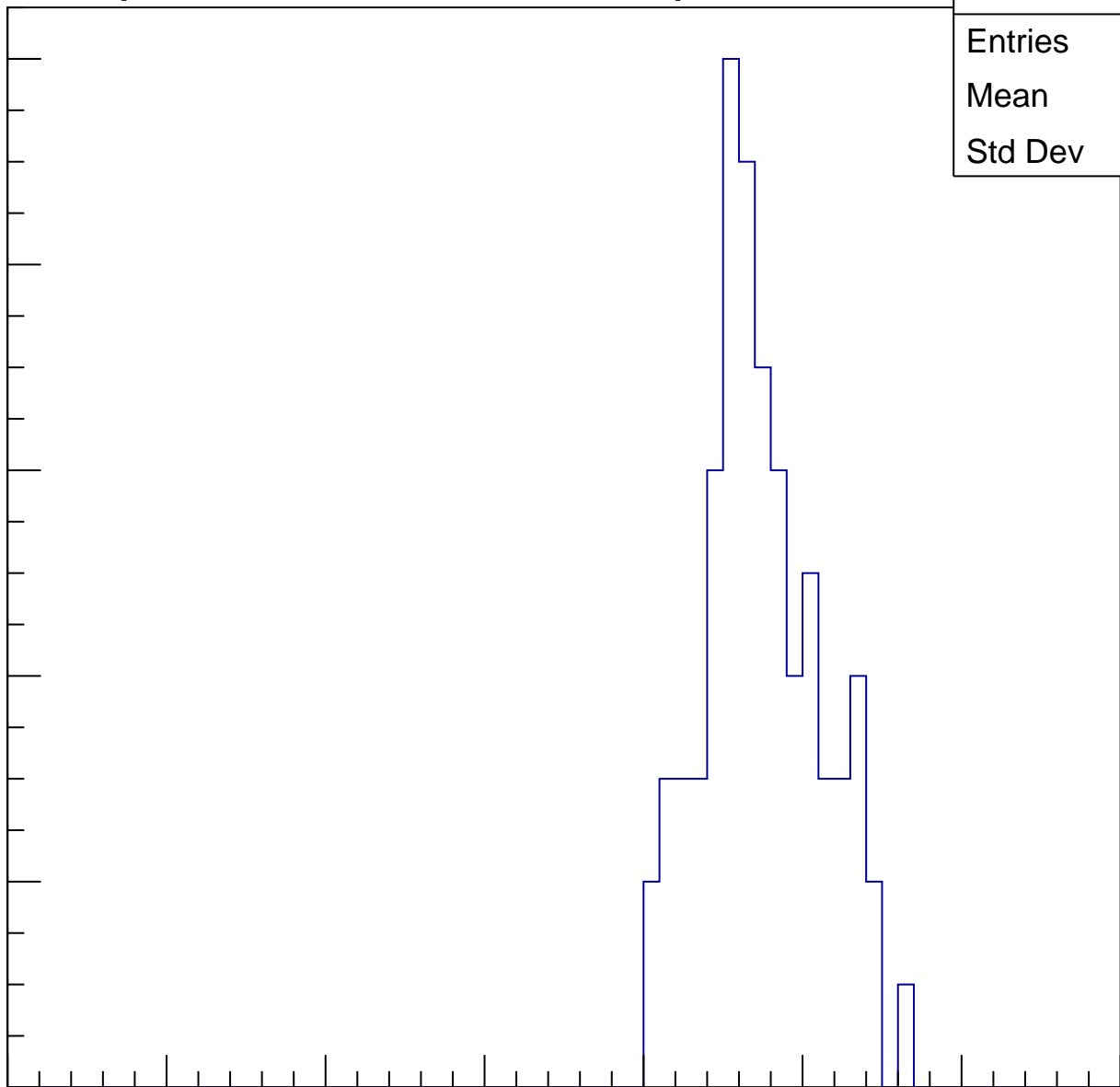
Entries	71
Mean	46.96
Std Dev	3.648

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

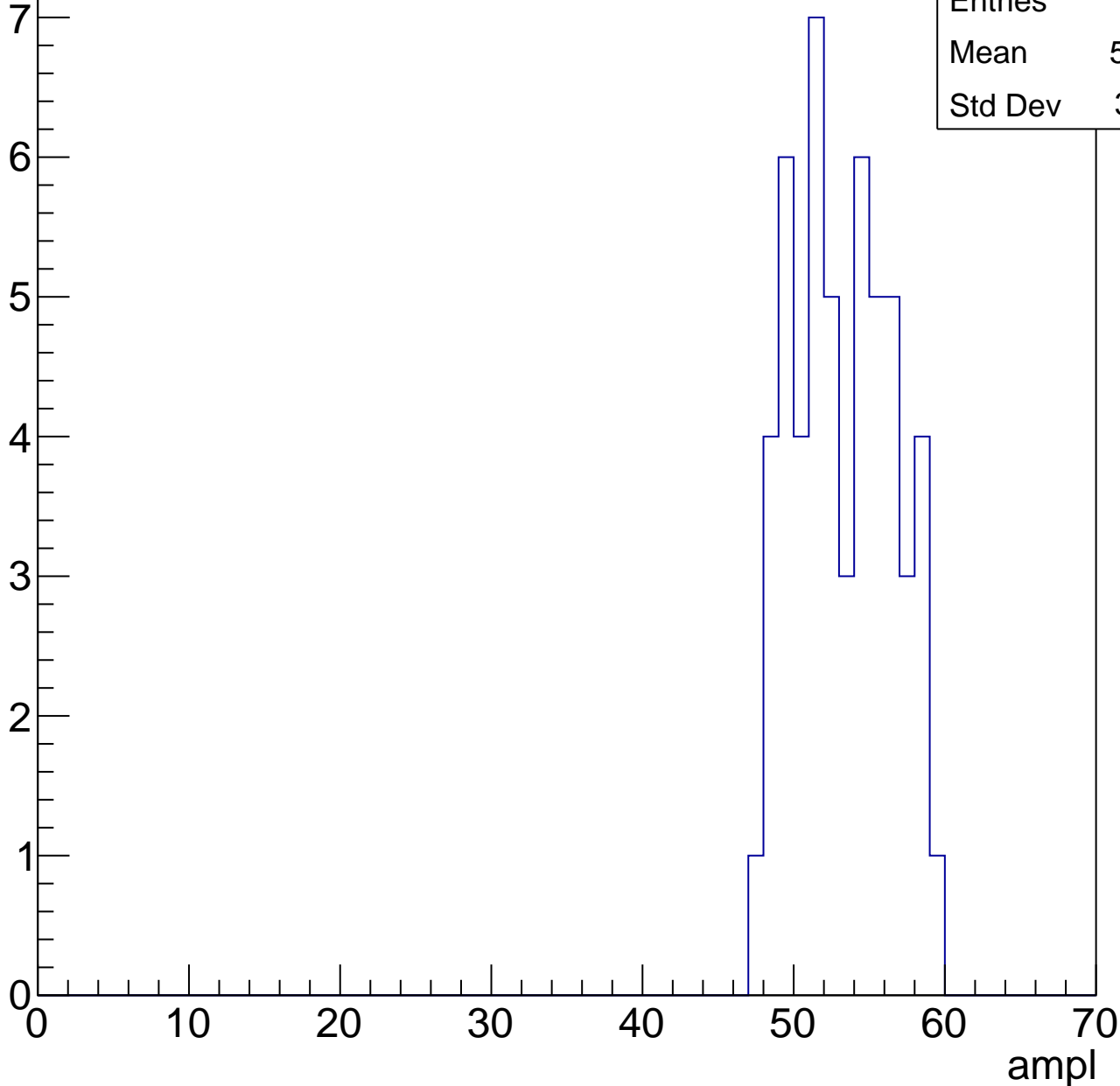


# B1L100S, U2-ch90, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	54
Mean	52.78
Std Dev	3.201



# B1L100S, U2-ch90, adc5

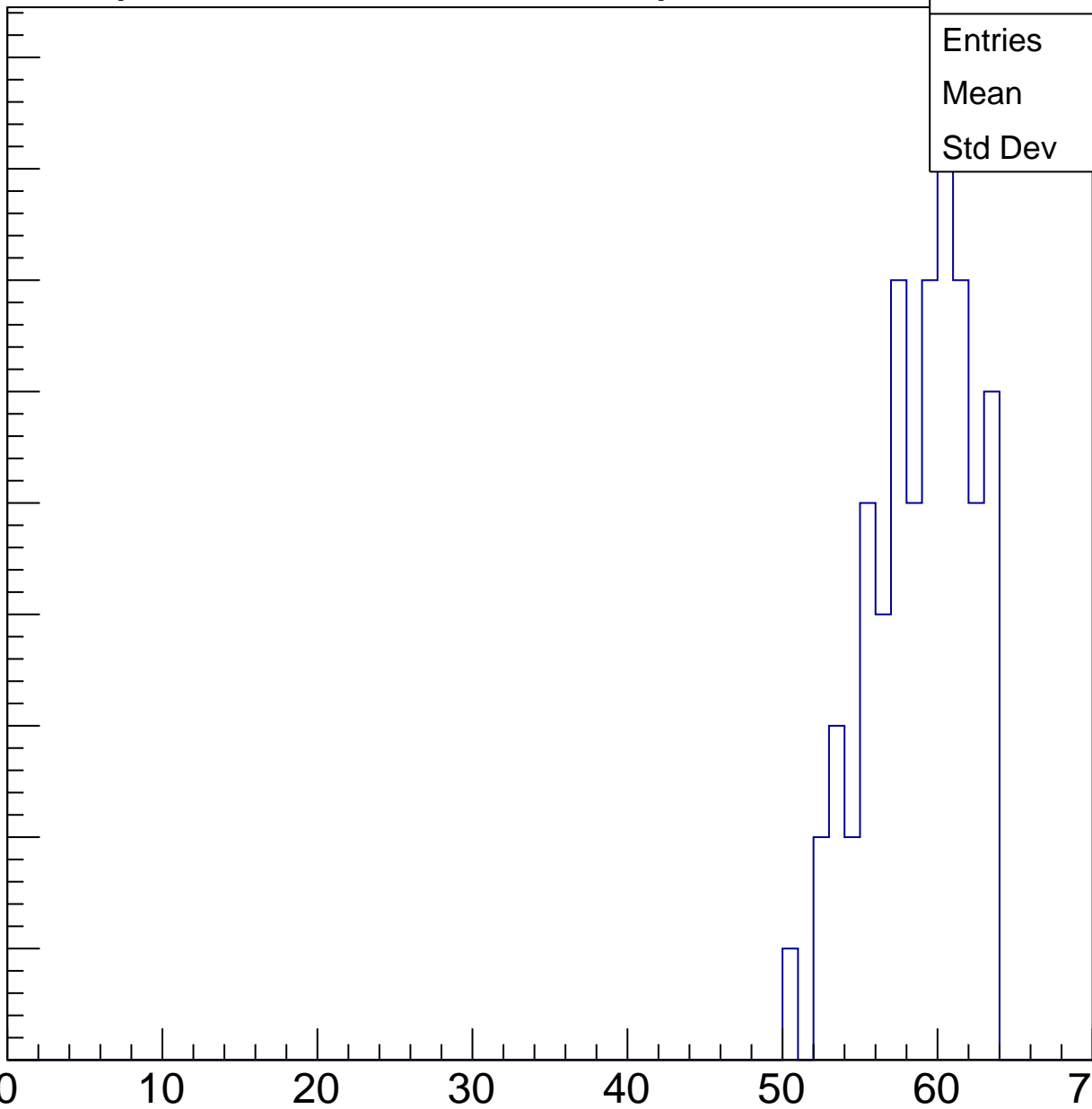
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	63
Mean	58.37
Std Dev	3.184

ampl

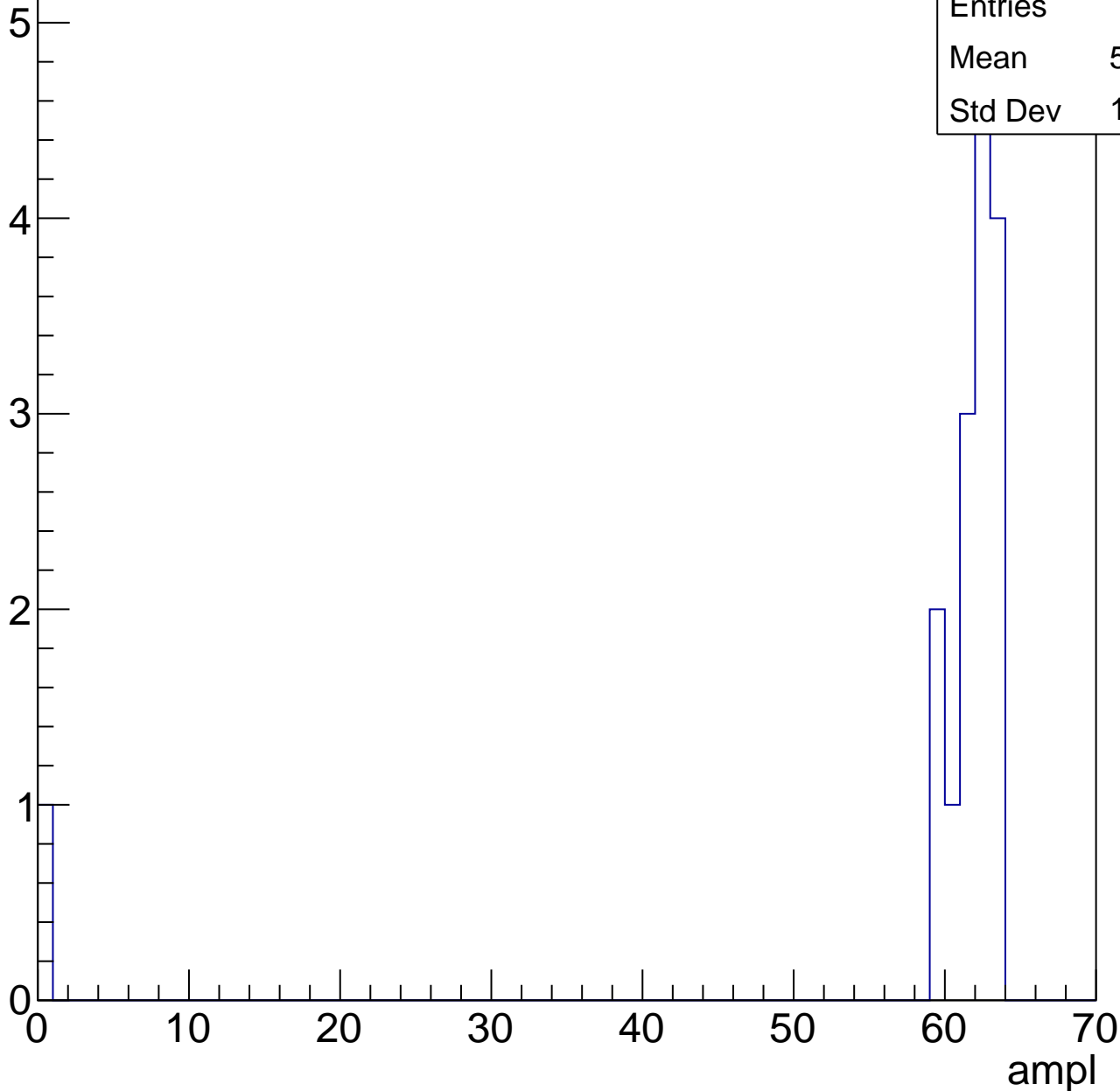


# B1L100S, U2-ch90, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	16
Mean	57.69
Std Dev	14.95

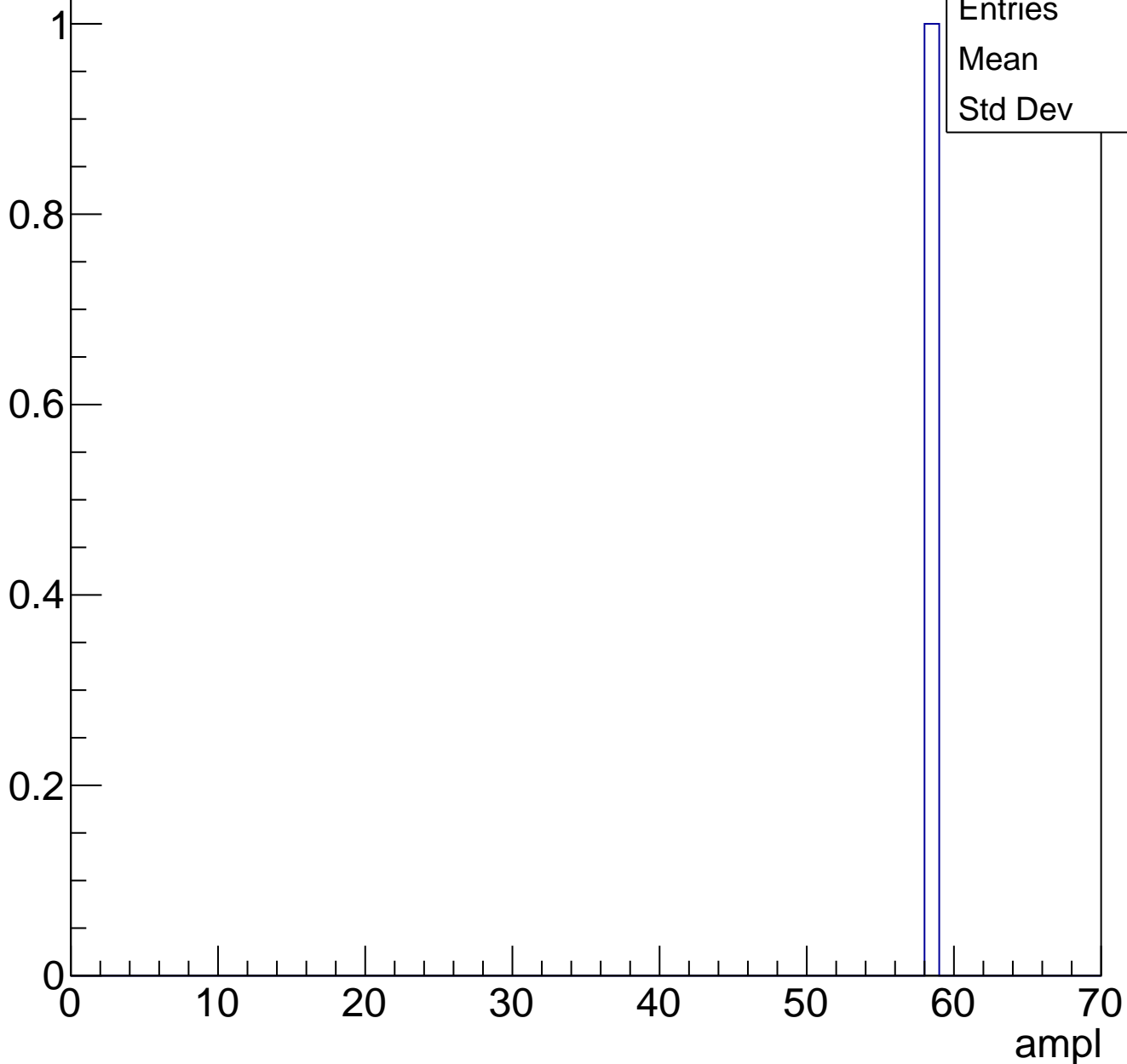




# B1L100S, U2-ch90, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



# B1L100S, U2-ch91, adc0

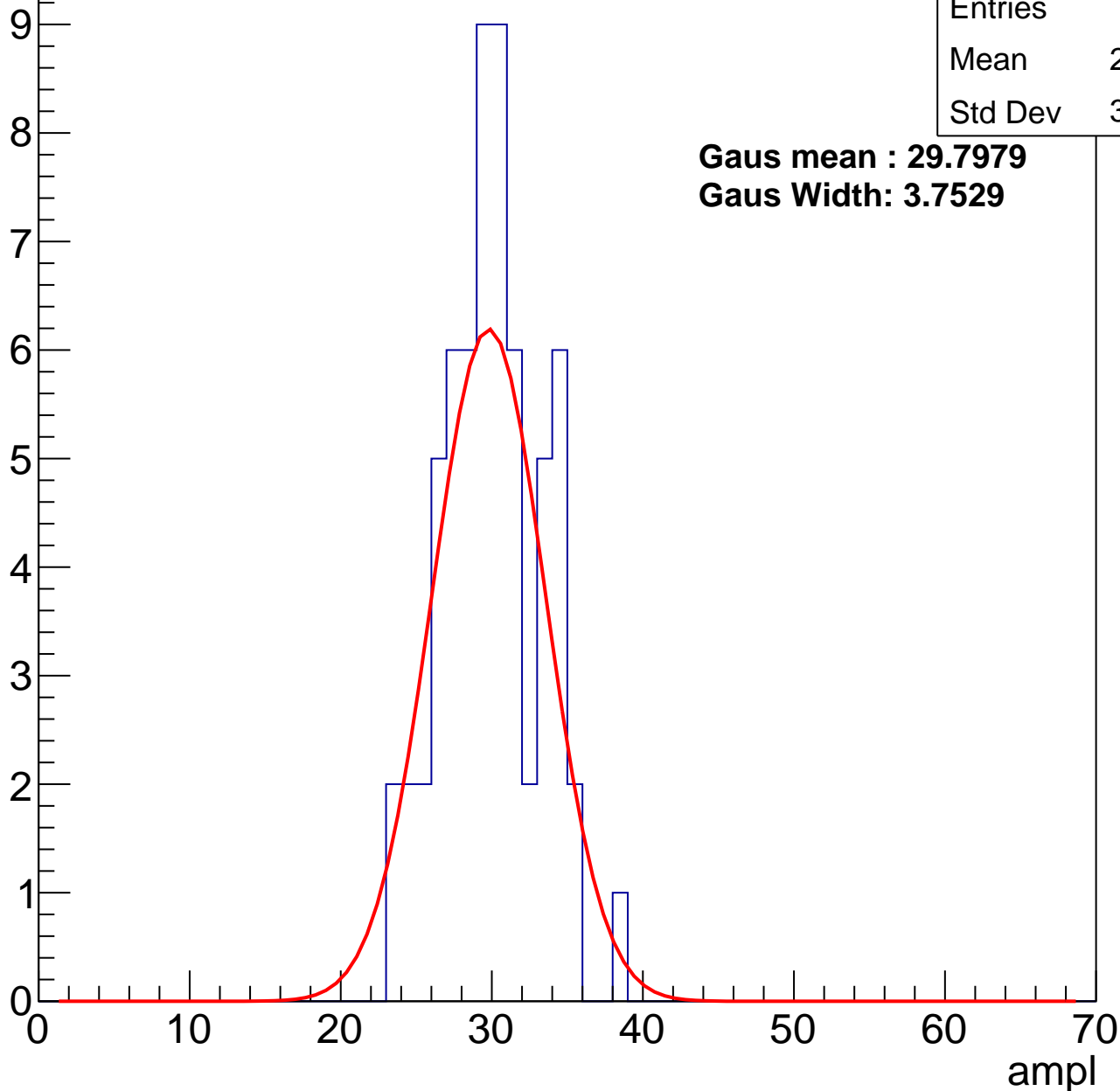
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	63
Mean	29.56
Std Dev	3.196

**Gaus mean : 29.7979**

**Gaus Width: 3.7529**



# B1L100S, U2-ch91, adc1

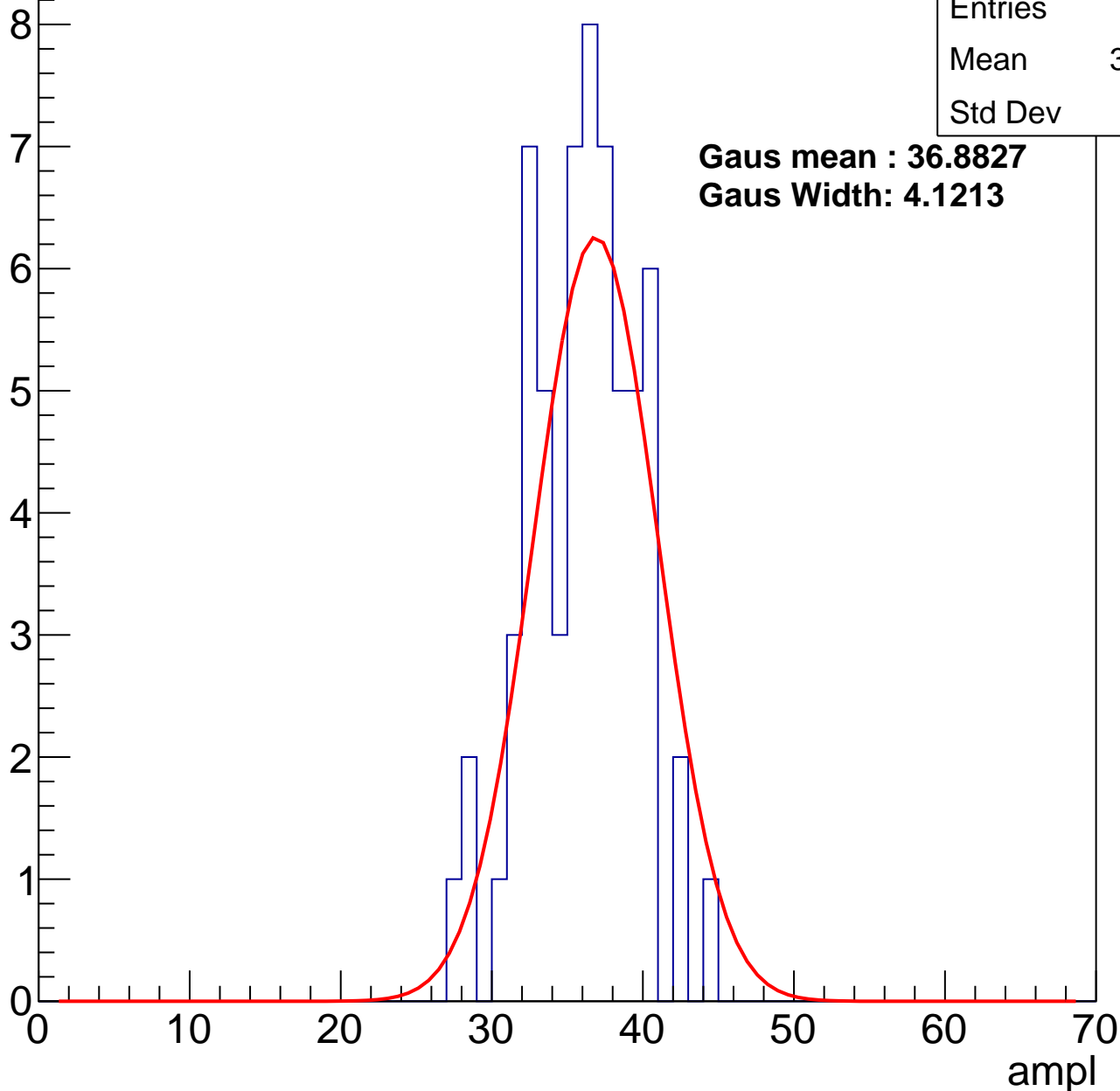
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	63
Mean	35.59
Std Dev	3.54

**Gaus mean : 36.8827**

**Gaus Width: 4.1213**



# B1L100S, U2-ch91, adc2

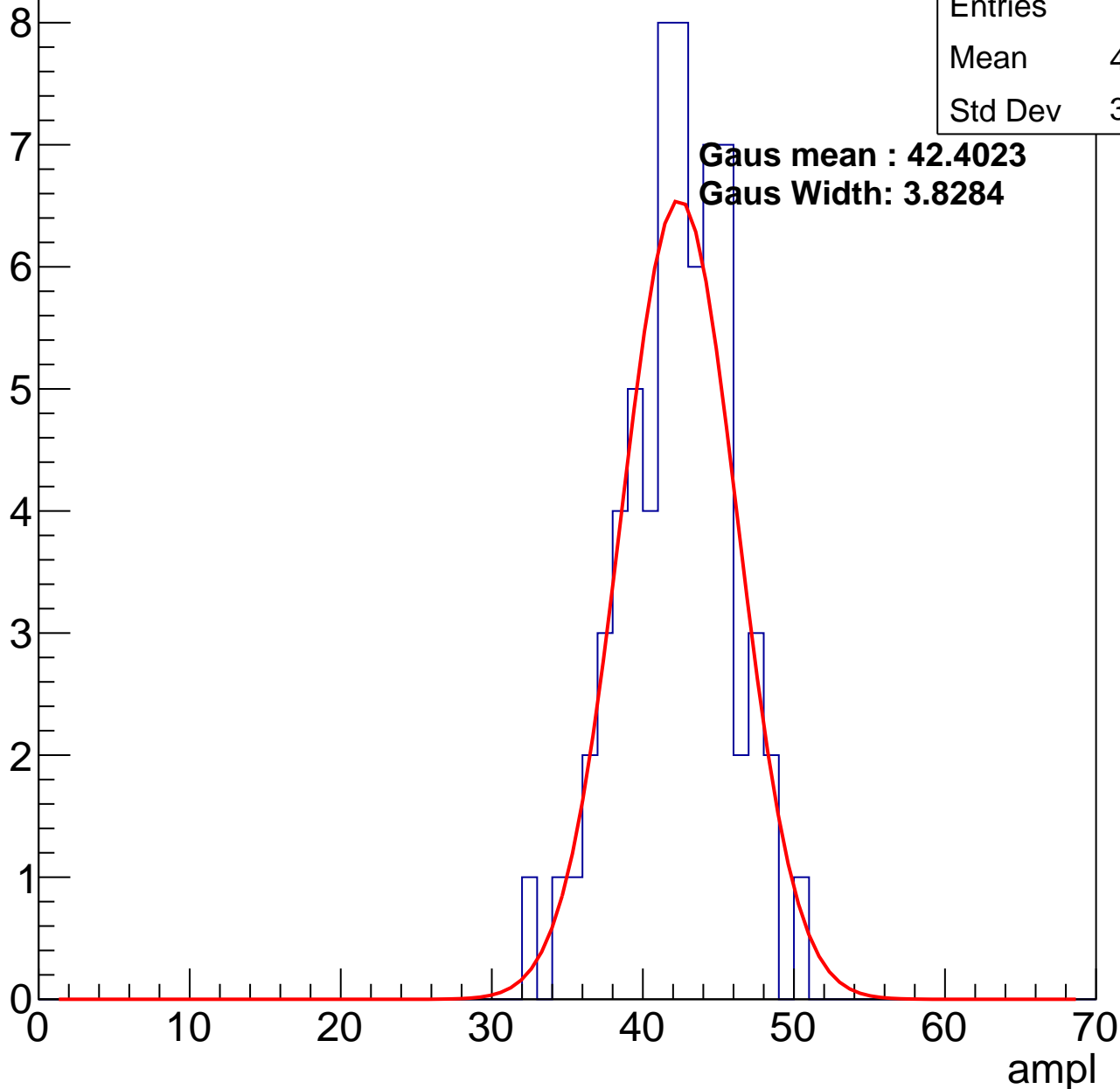
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	65
Mean	41.77
Std Dev	3.572

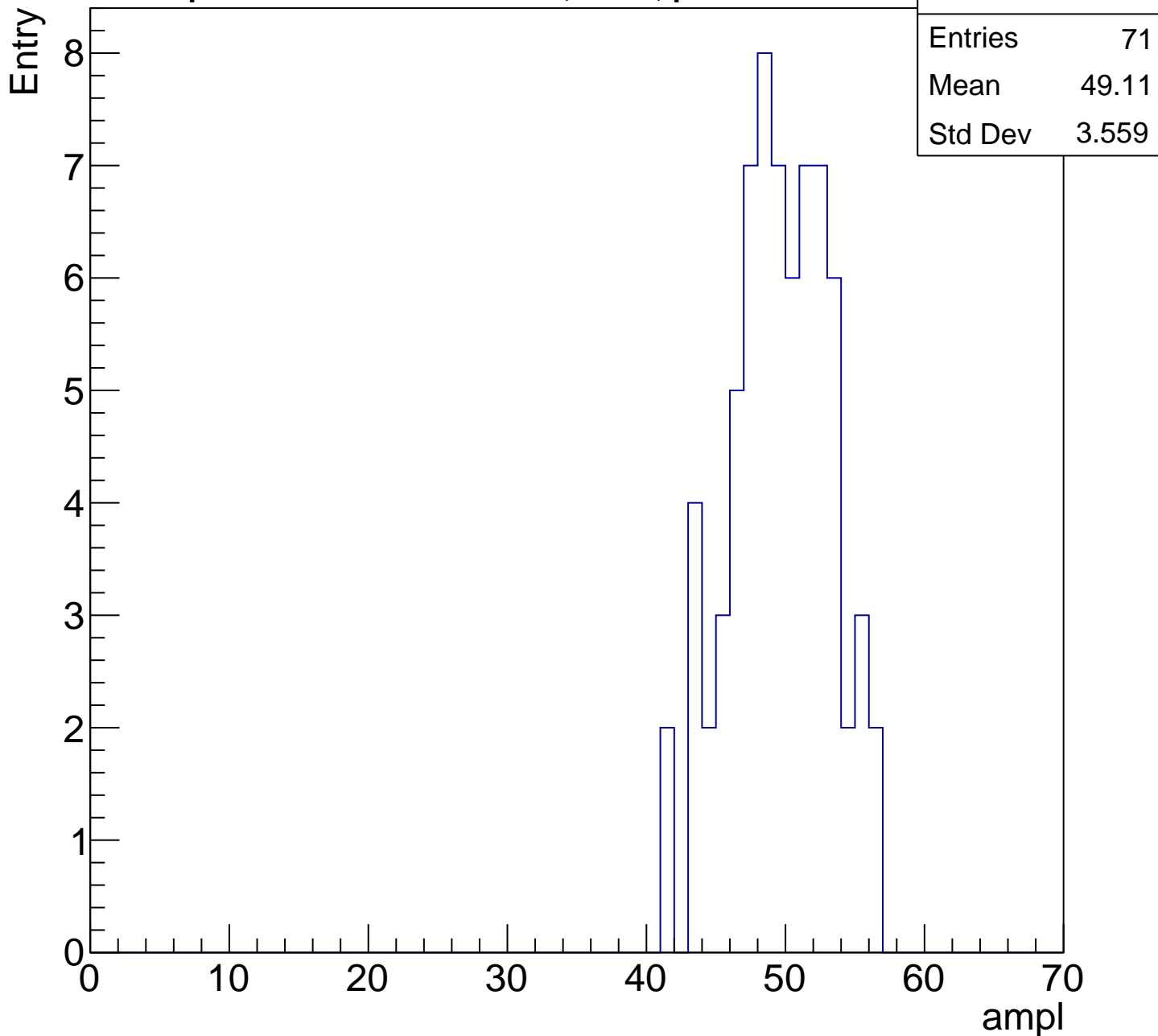
**Gaus mean : 42.4023**

**Gaus Width: 3.8284**



# B1L100S, U2-ch91, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2



# B1L100S, U2-ch91, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

10

8

6

4

2

0

0

10

20

30

40

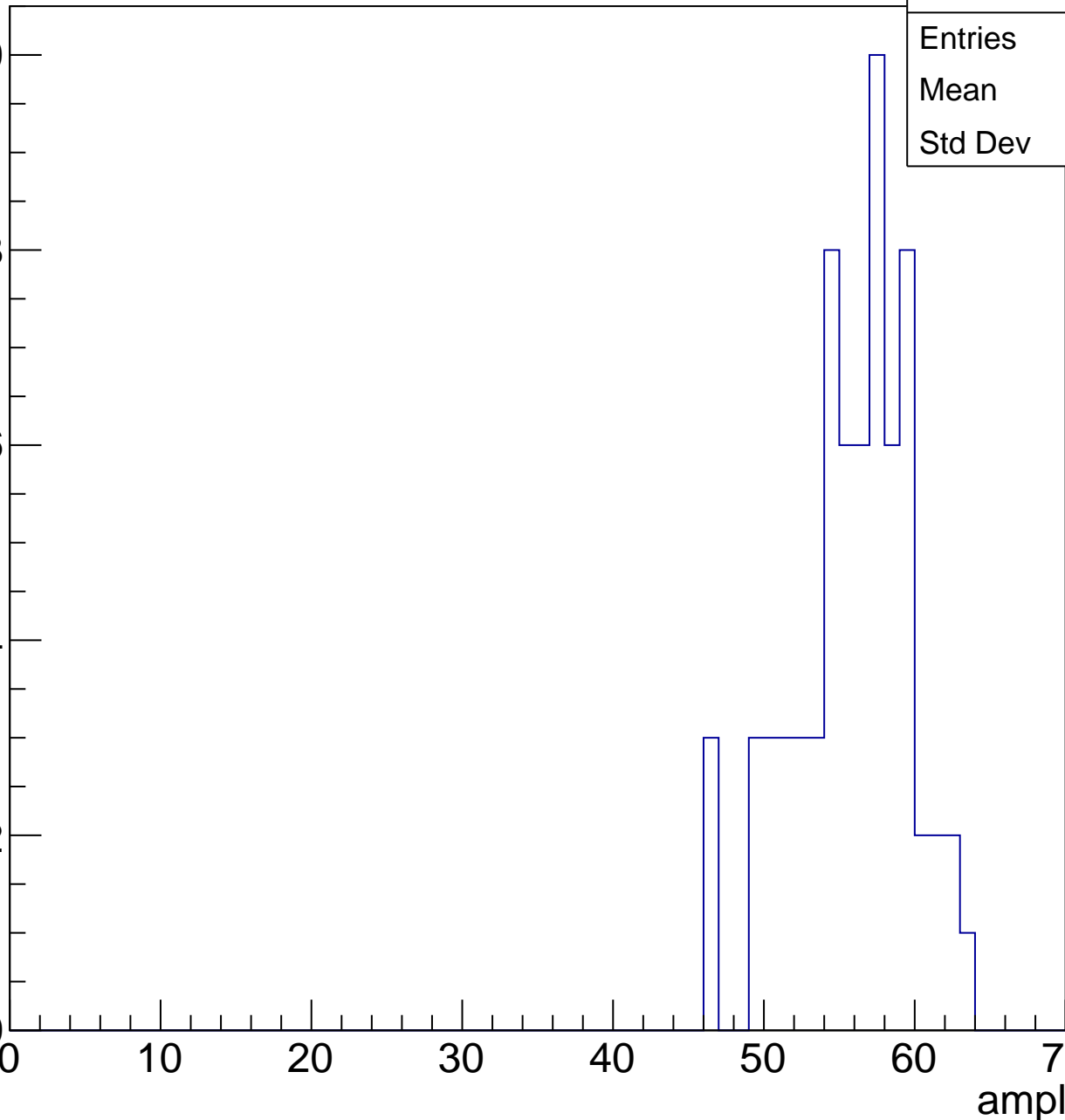
50

60

70

ampl

Entries	69
Mean	55.36
Std Dev	3.852

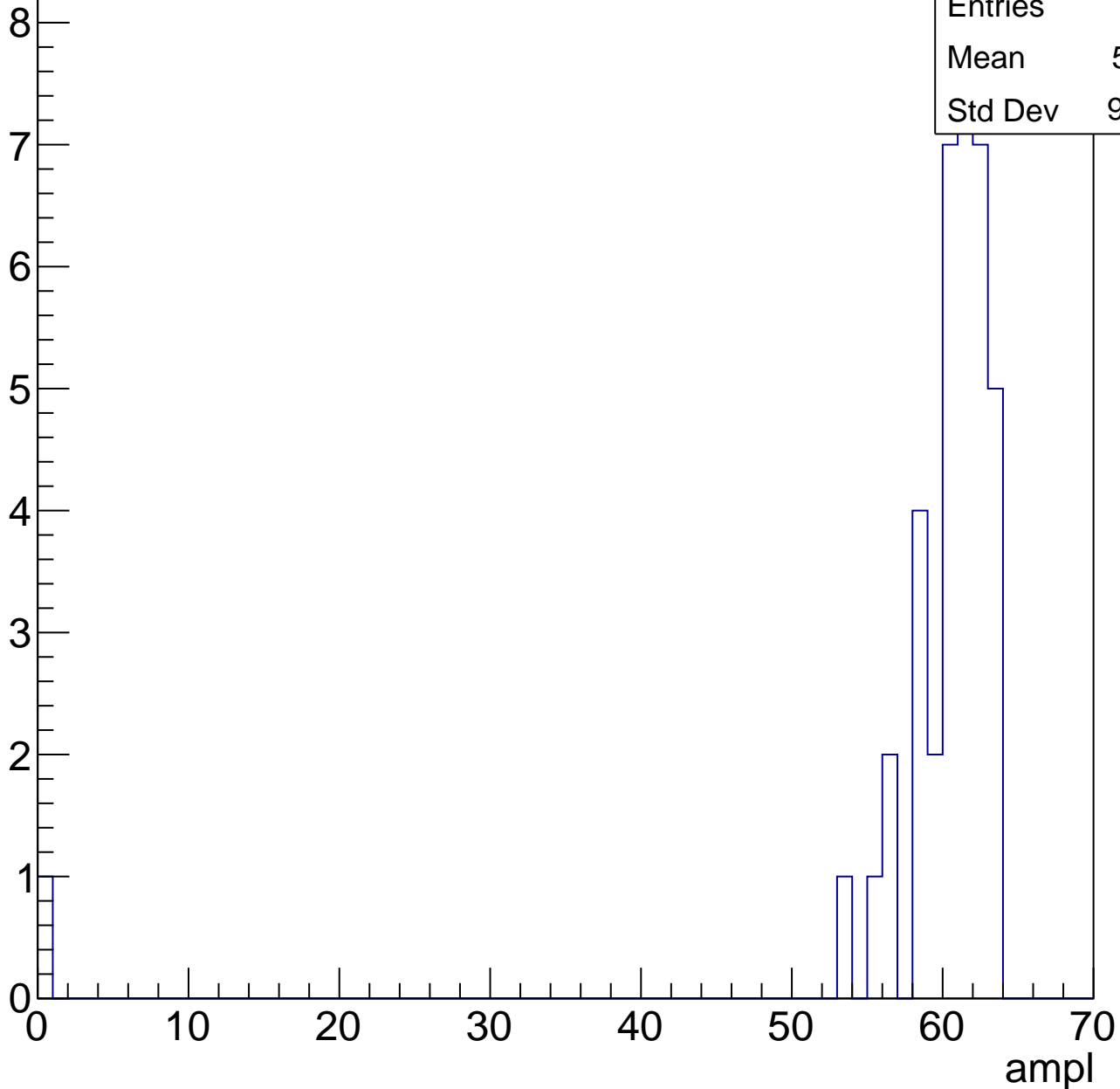


# B1L100S, U2-ch91, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

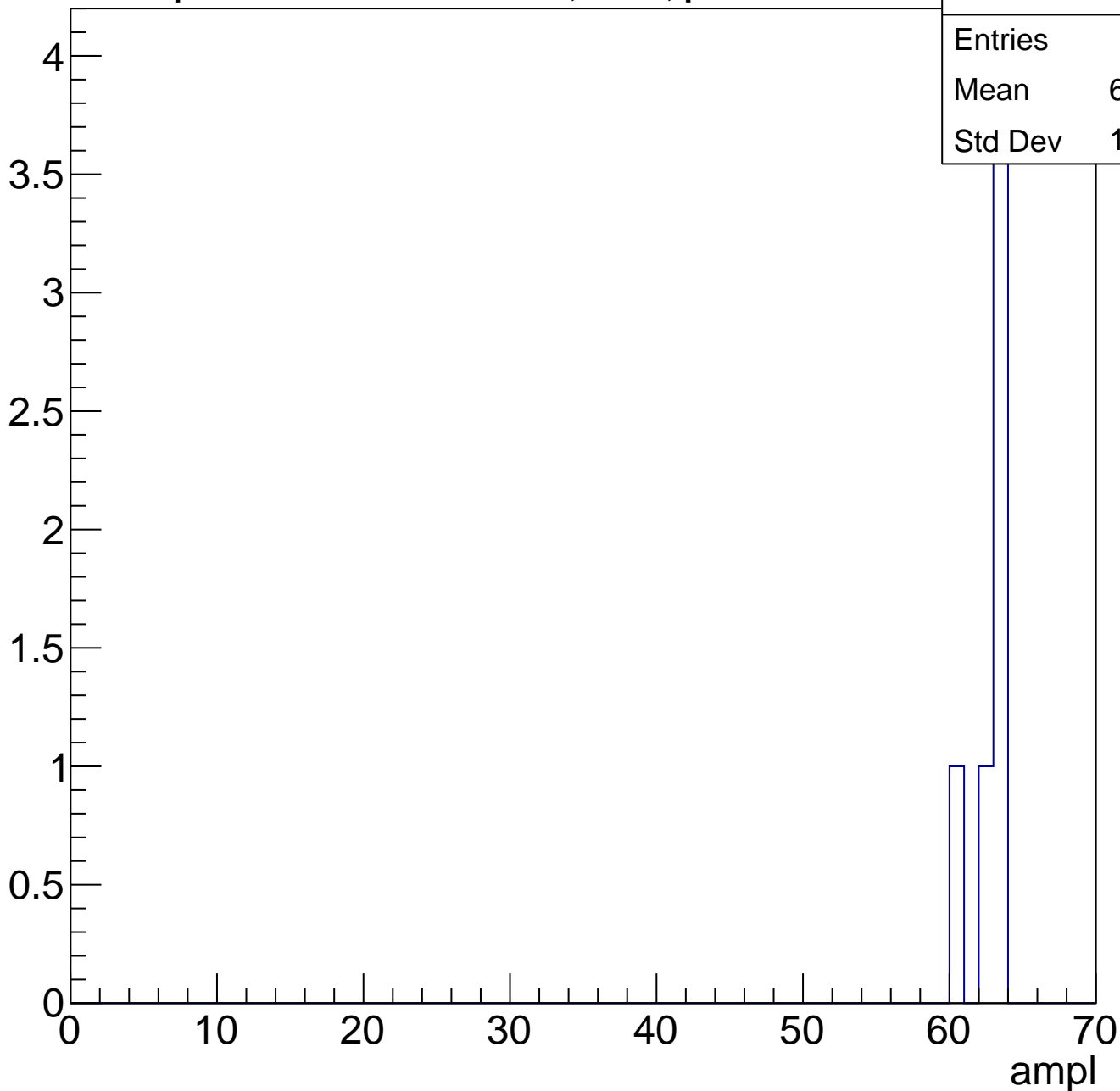
Entries	38
Mean	58.61
Std Dev	9.909



# B1L100S, U2-ch91, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry





# B1L100S, U2-ch91, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L100S, U2-ch92, adc0

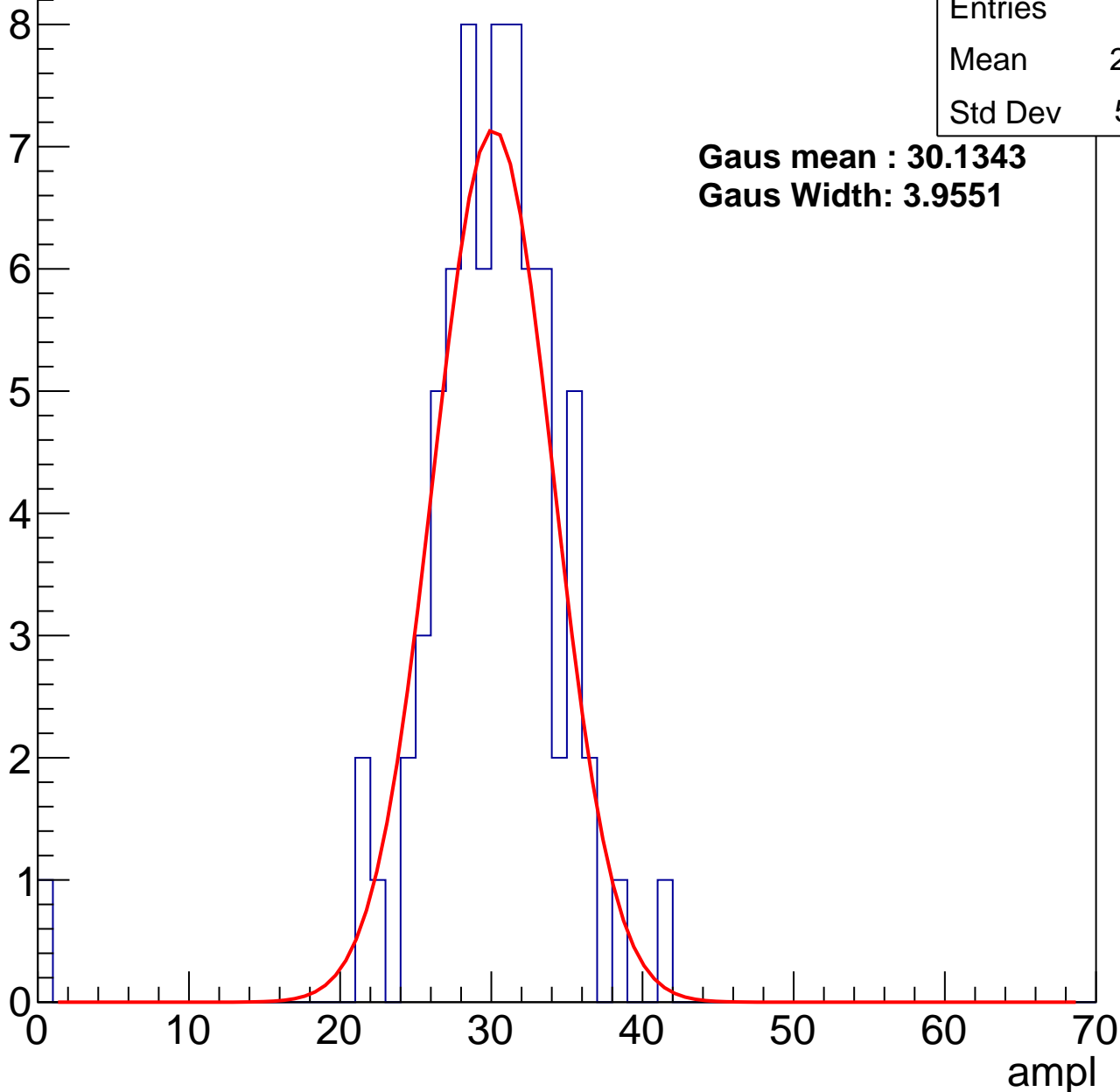
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	73
Mean	29.44
Std Dev	5.131

**Gaus mean : 30.1343**

**Gaus Width: 3.9551**



# B1L100S, U2-ch92, adc1

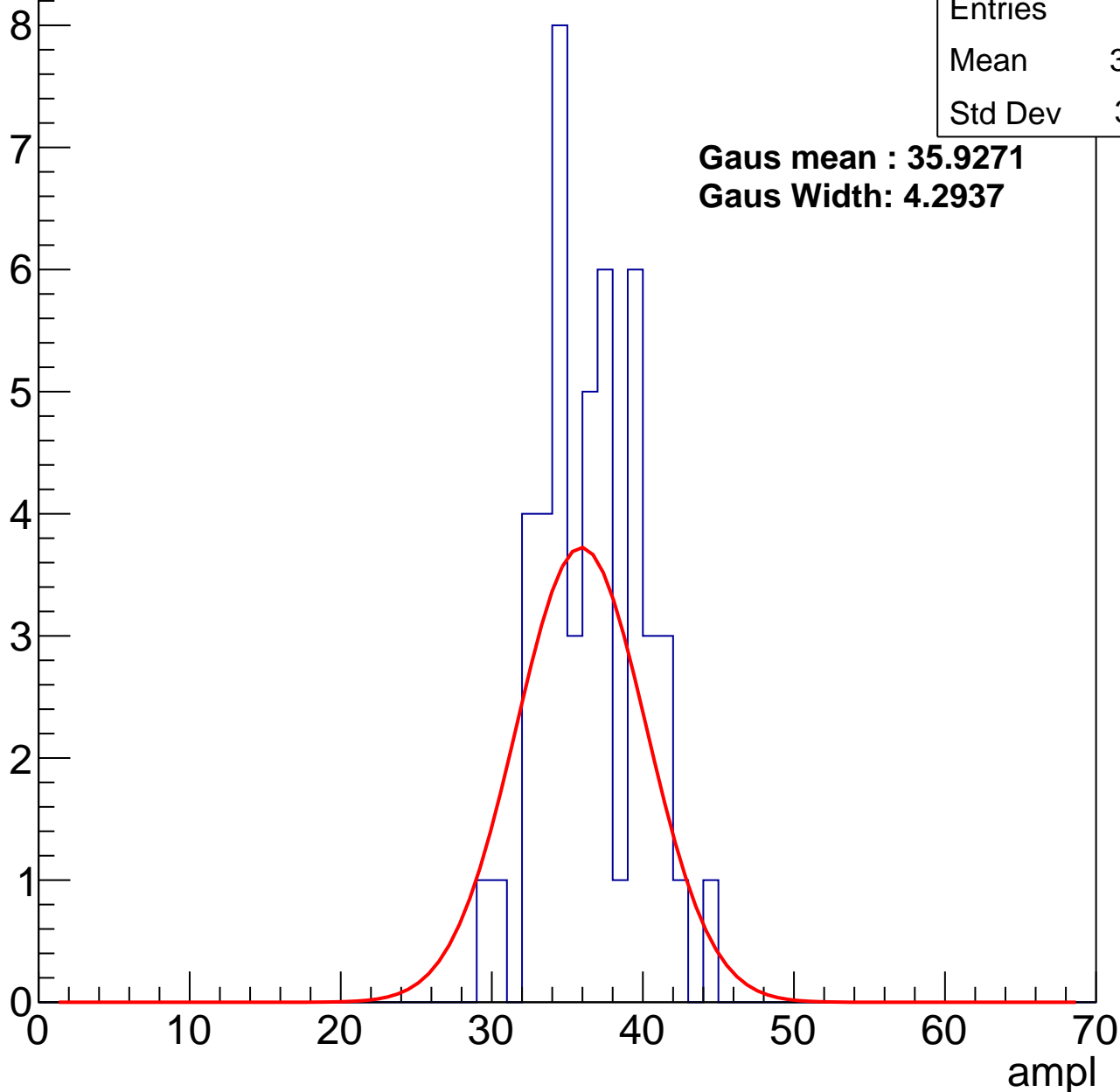
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	47
Mean	36.15
Std Dev	3.281

**Gaus mean : 35.9271**

**Gaus Width: 4.2937**



# B1L100S, U2-ch92, adc2

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	85
Mean	42.12
Std Dev	3.972

**Gaus mean : 42.4582**

**Gaus Width: 4.2451**

10

8

6

4

2

0

0

10

20

30

40

50

60

70

ampl

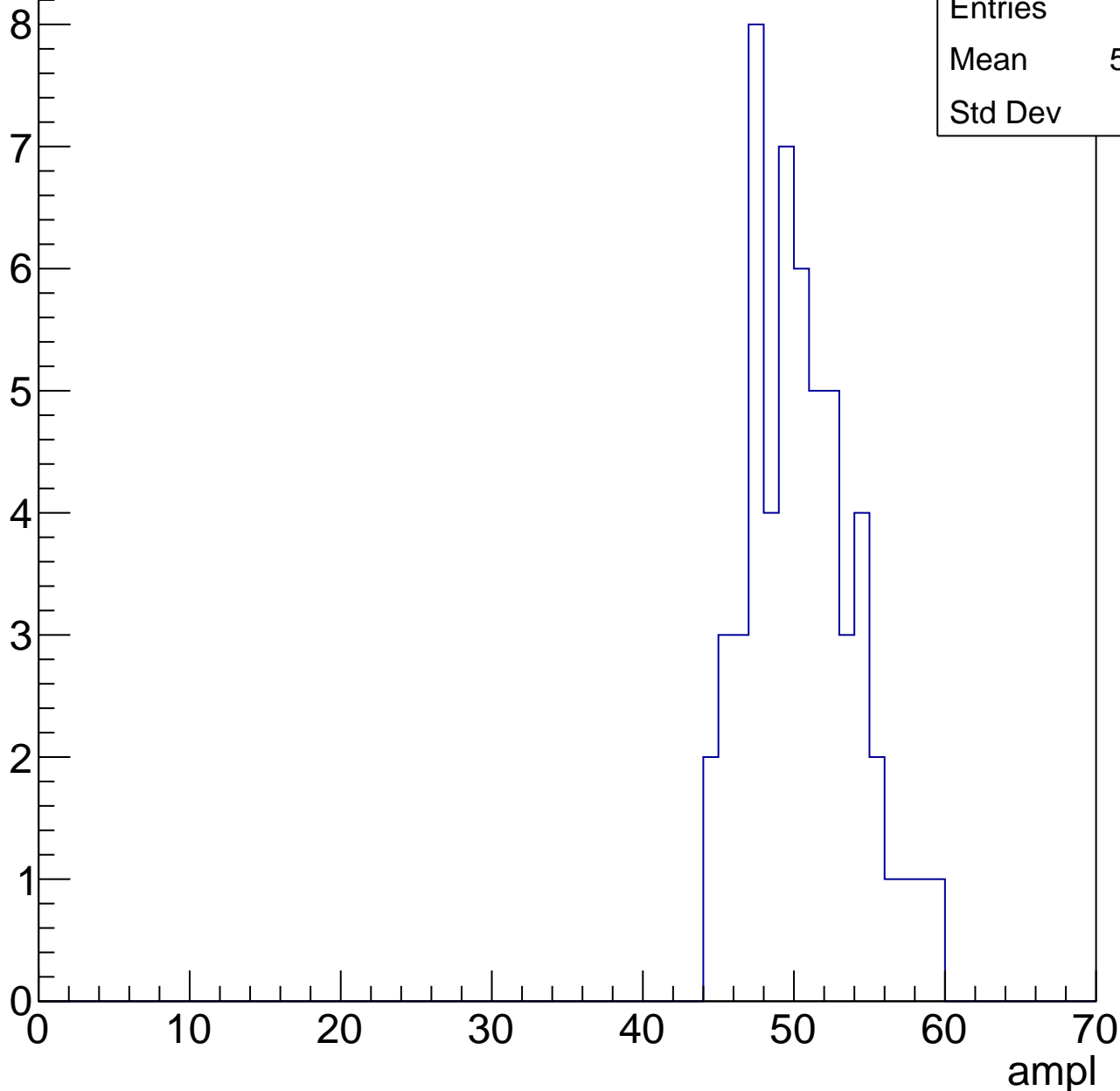


# B1L100S, U2-ch92, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

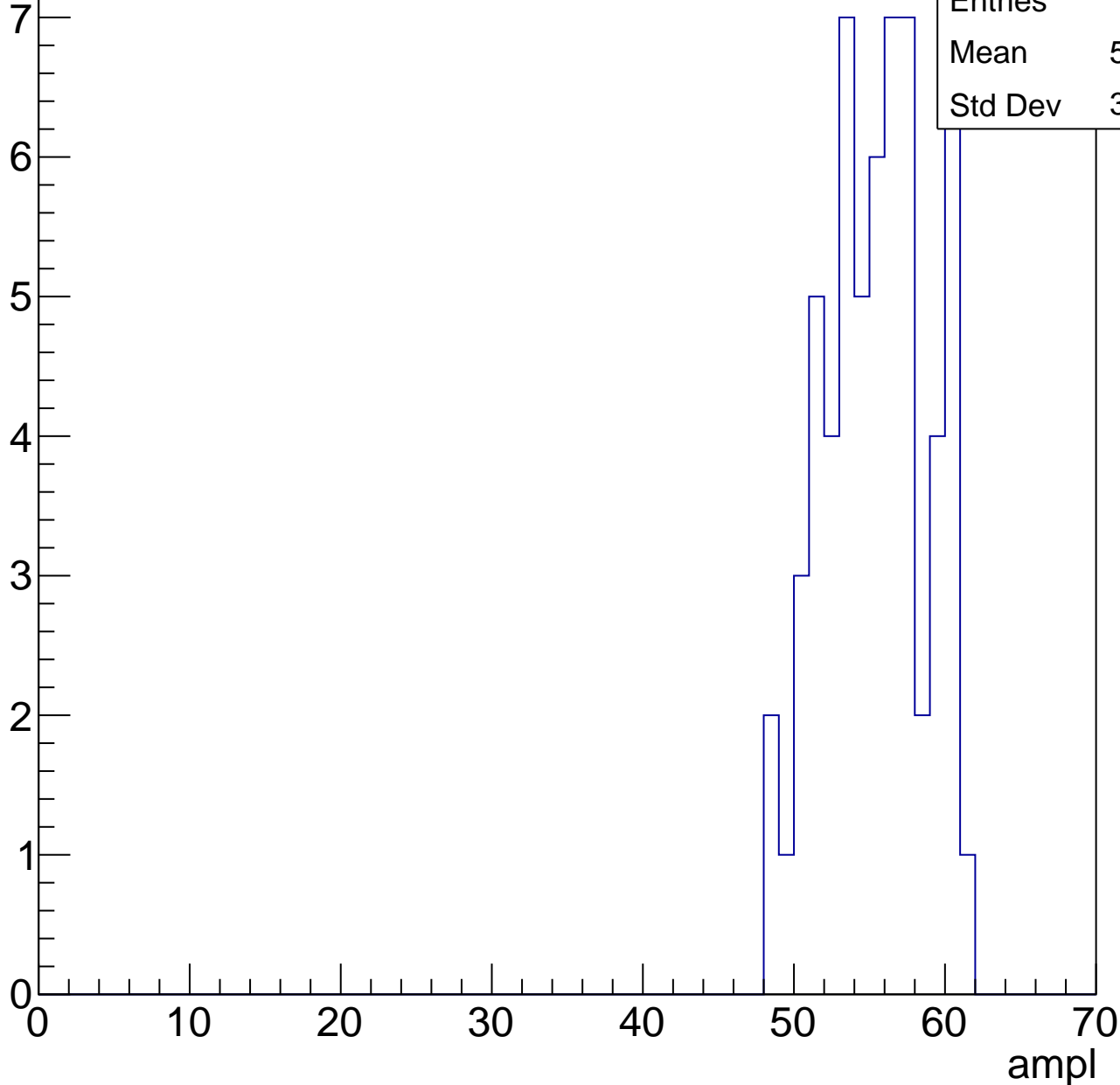
Entries	56
Mean	50.04
Std Dev	3.5



# B1L100S, U2-ch92, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	61
Mean	54.97
Std Dev	3.353

# B1L100S, U2-ch92, adc5

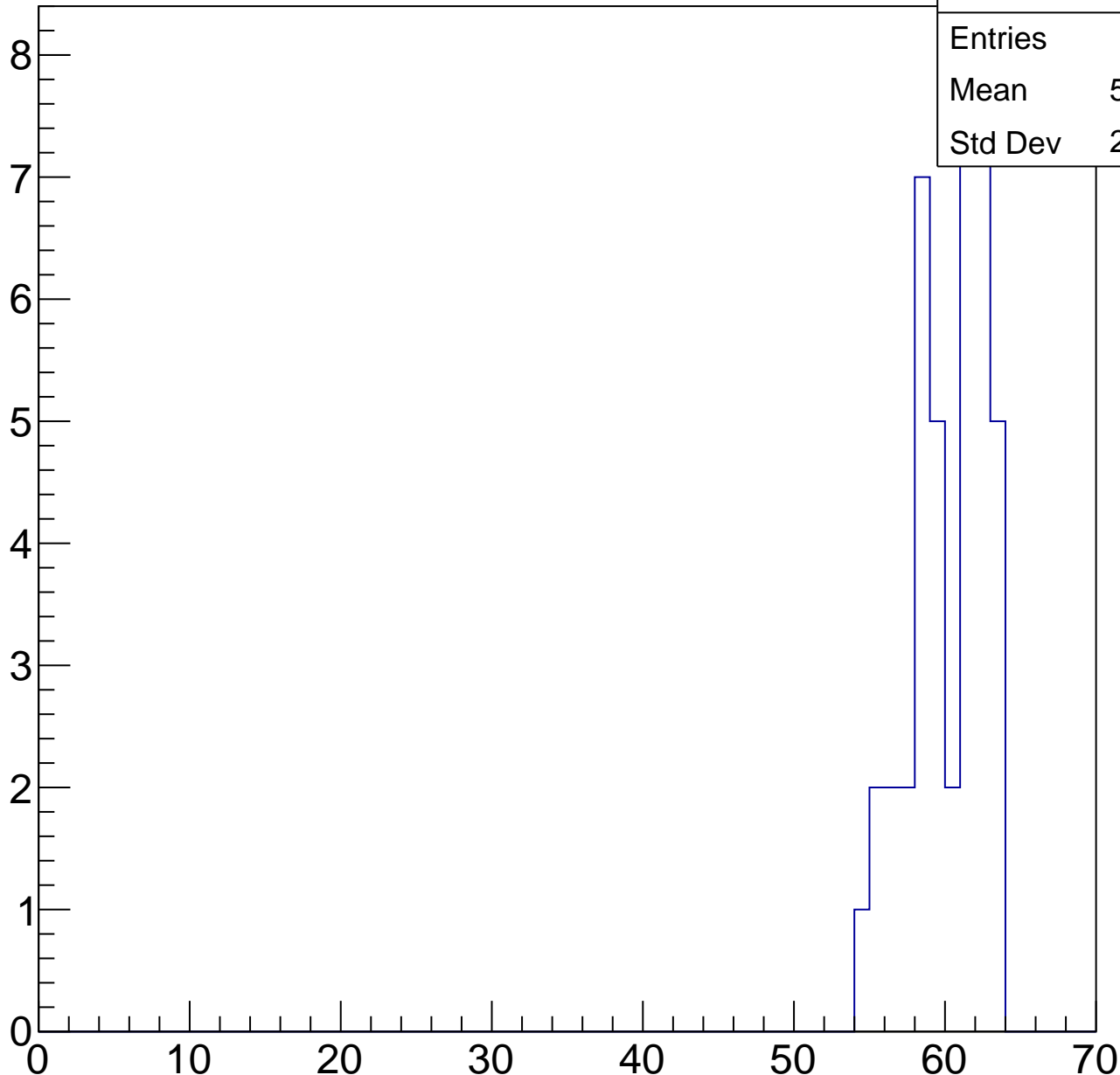
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	42
Mean	59.76
Std Dev	2.448

ampl

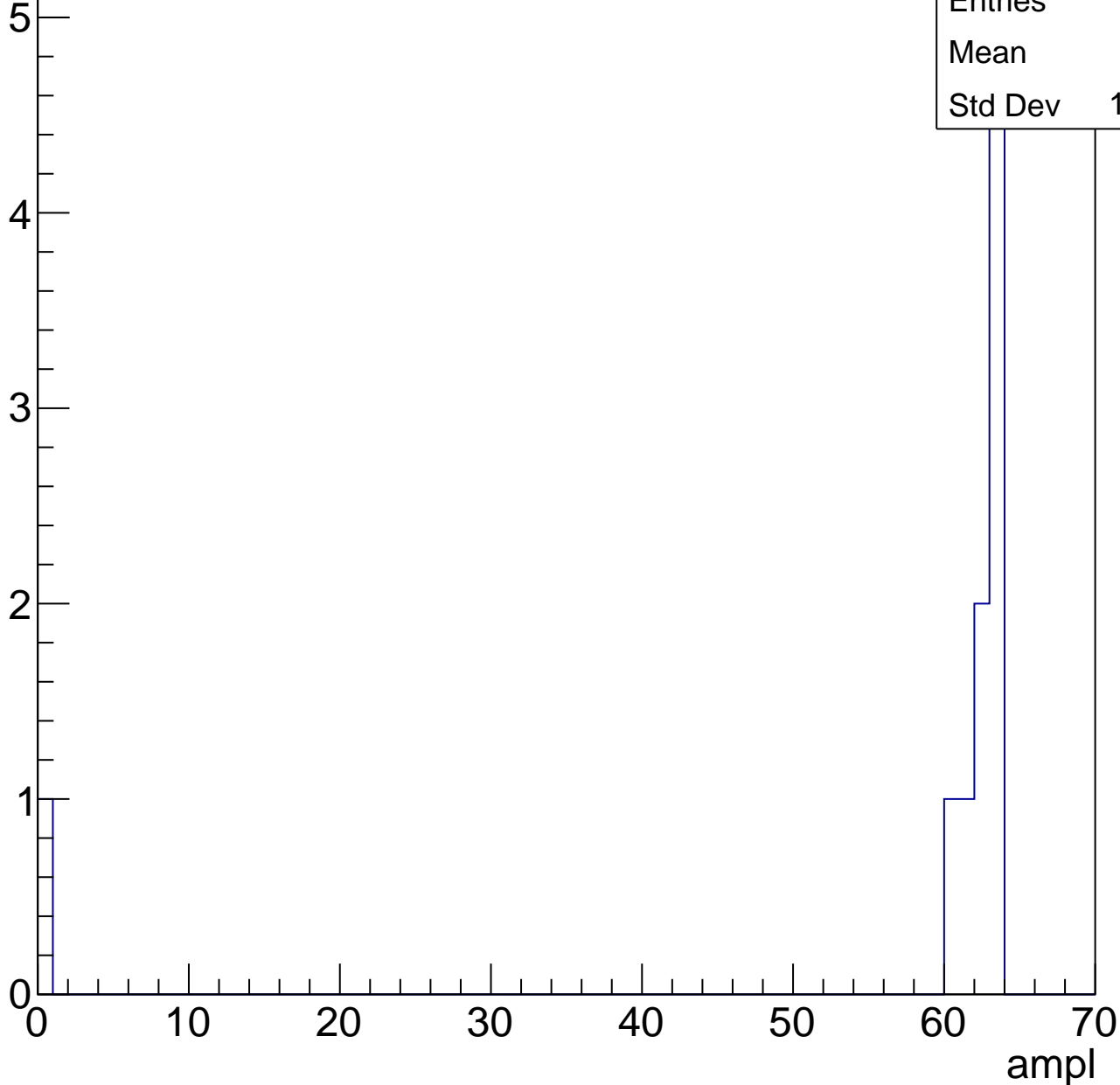


# B1L100S, U2-ch92, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	10
Mean	56
Std Dev	18.69





# B1L100S, U2-ch92, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L100S, U2-ch93, adc0

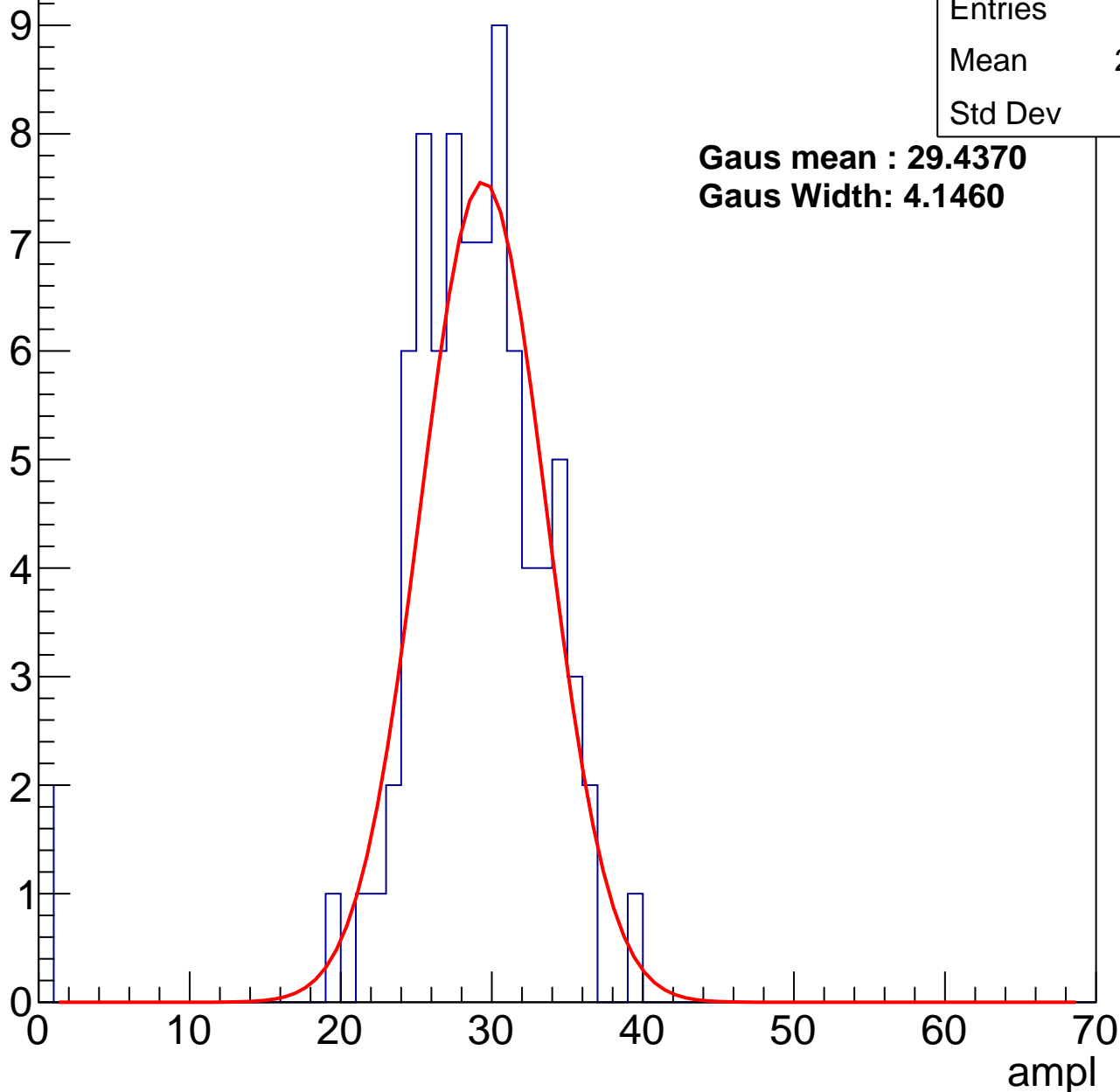
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	83
Mean	28.01
Std Dev	5.83

**Gaus mean : 29.4370**

**Gaus Width: 4.1460**



# B1L100S, U2-ch93, adc1

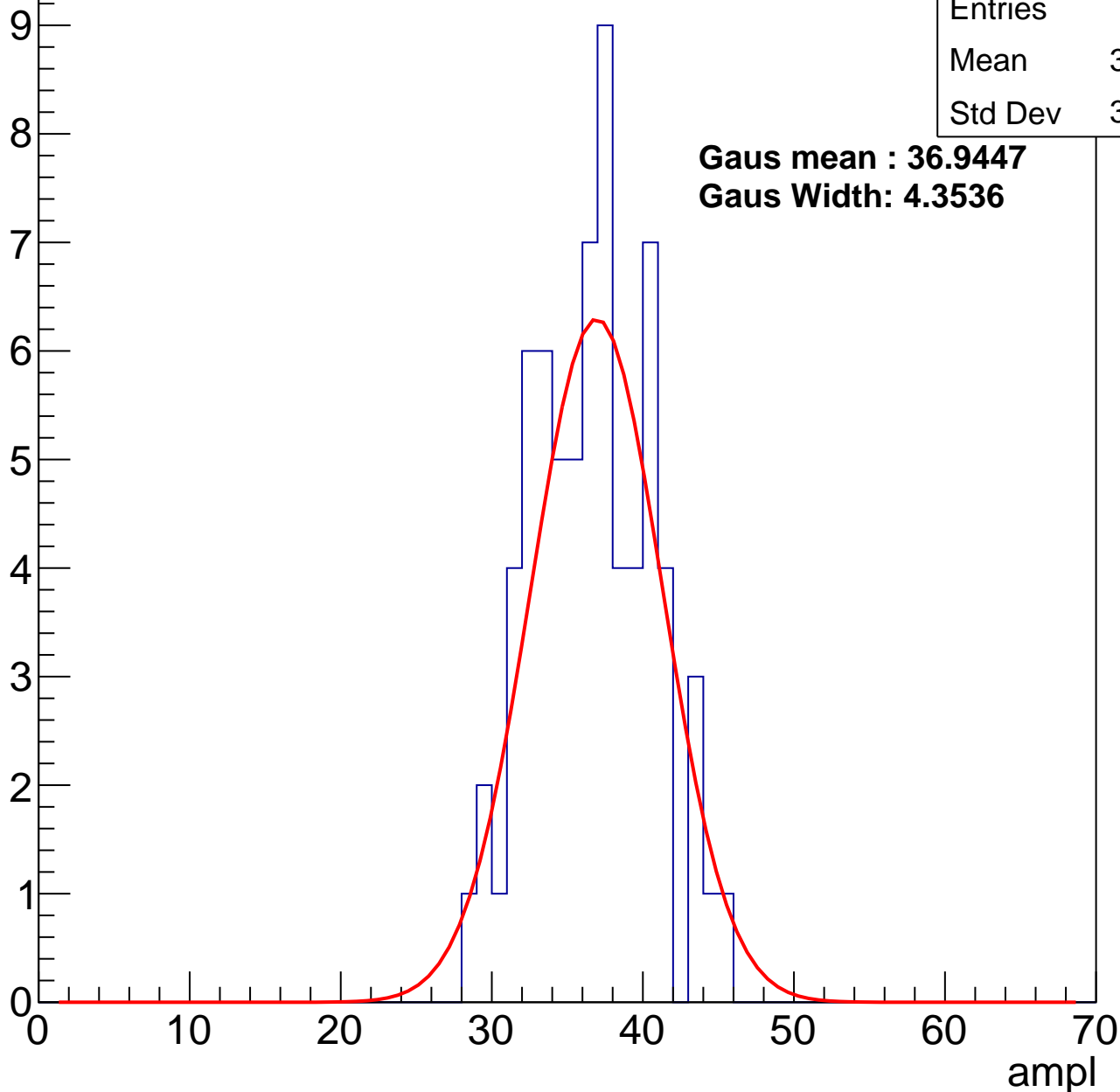
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	70
Mean	36.14
Std Dev	3.848

**Gaus mean : 36.9447**

**Gaus Width: 4.3536**



# B1L100S, U2-ch93, adc2

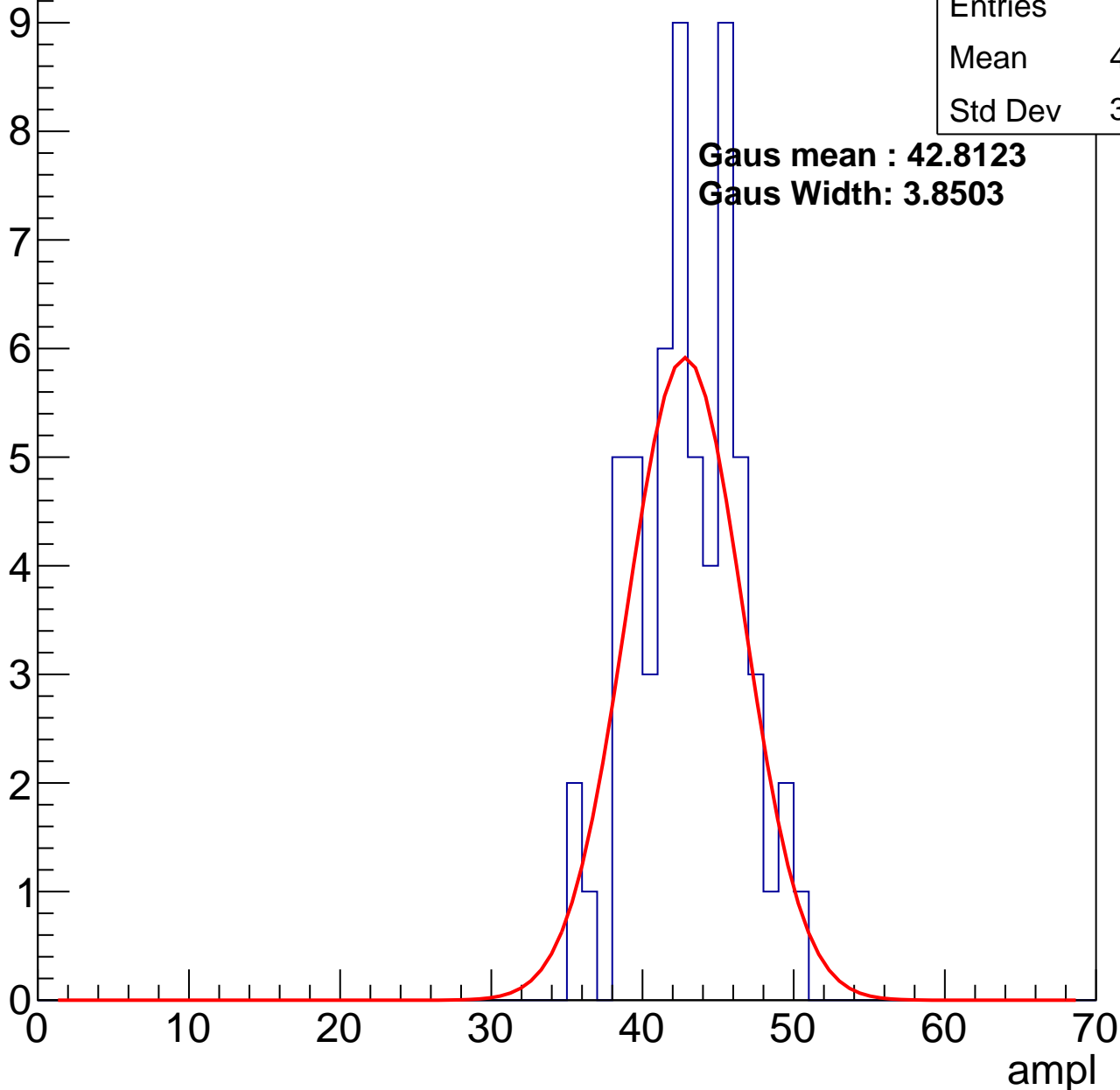
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	61
Mean	42.59
Std Dev	3.413

**Gaus mean : 42.8123**

**Gaus Width: 3.8503**

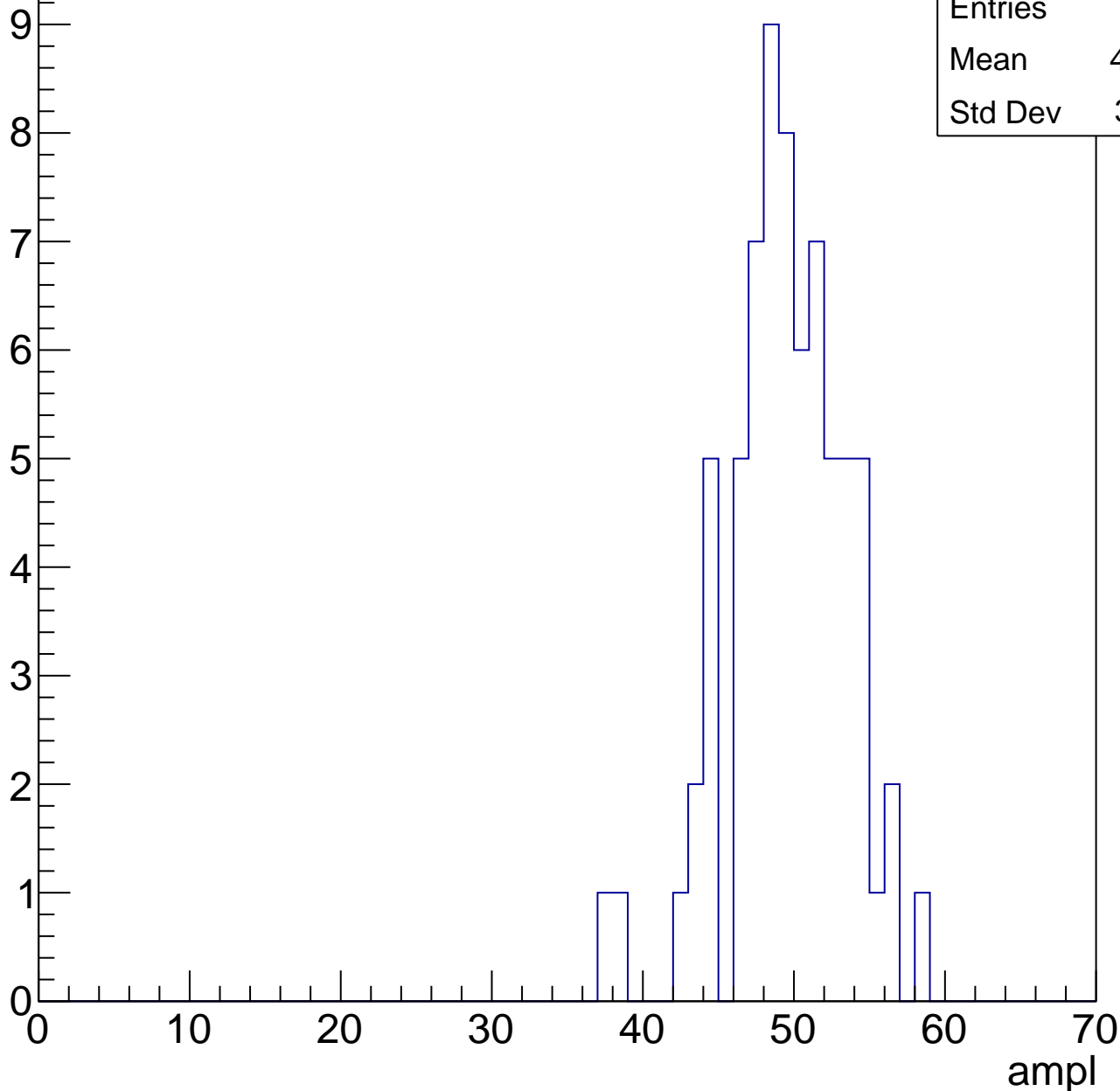


# B1L100S, U2-ch93, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	71
Mean	49.06
Std Dev	3.921

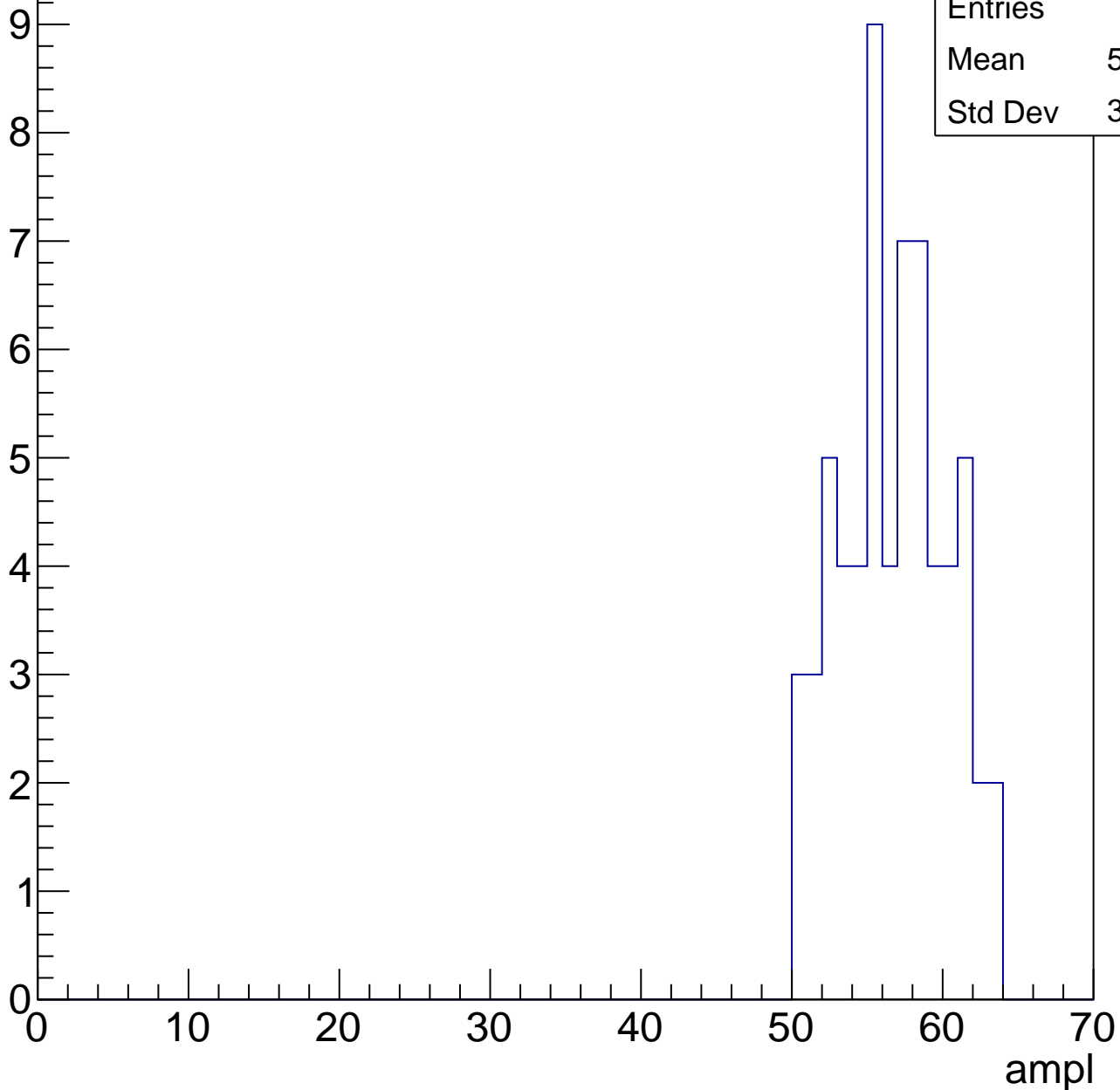


# B1L100S, U2-ch93, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	63
Mean	56.29
Std Dev	3.448

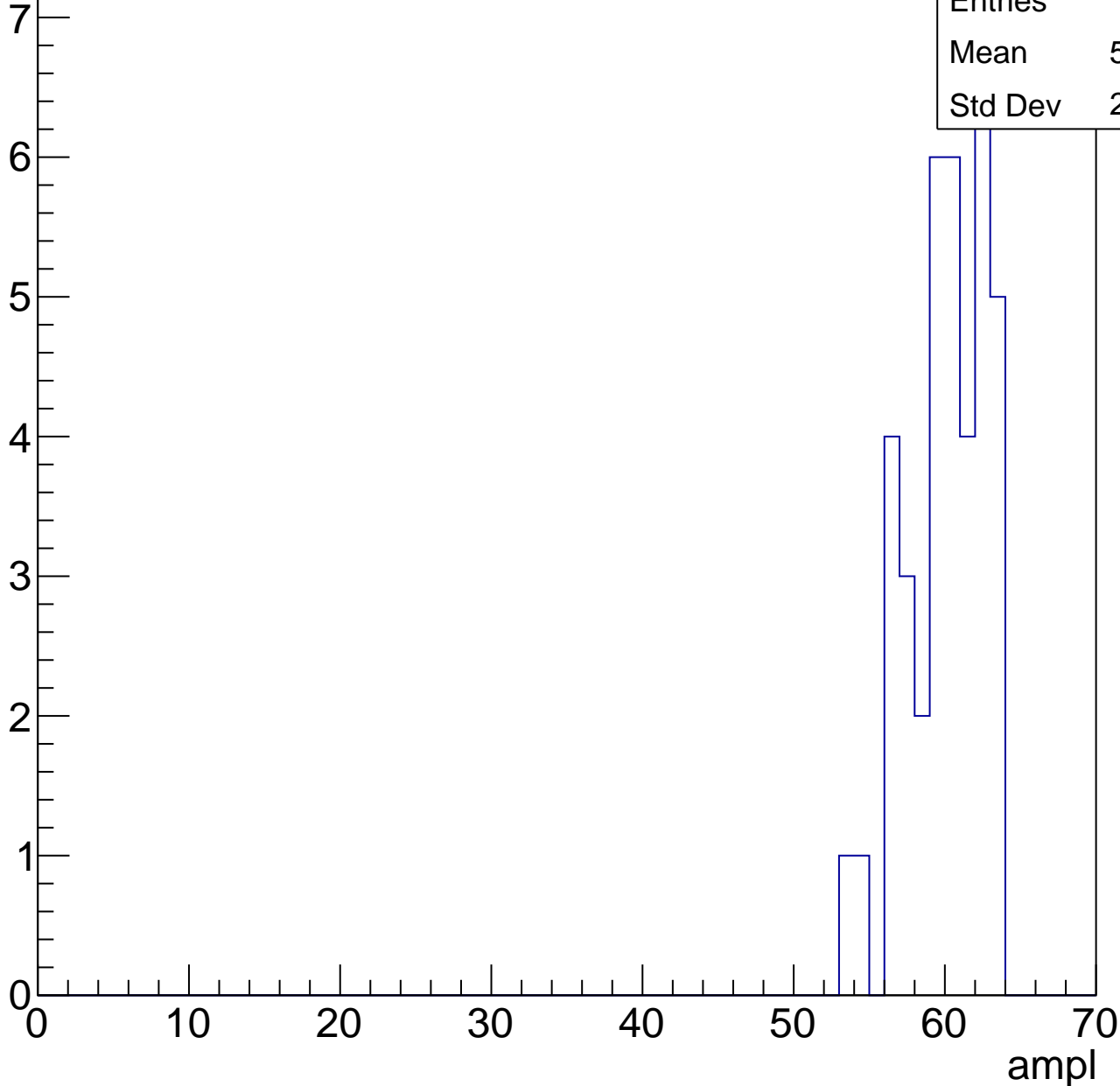


# B1L100S, U2-ch93, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

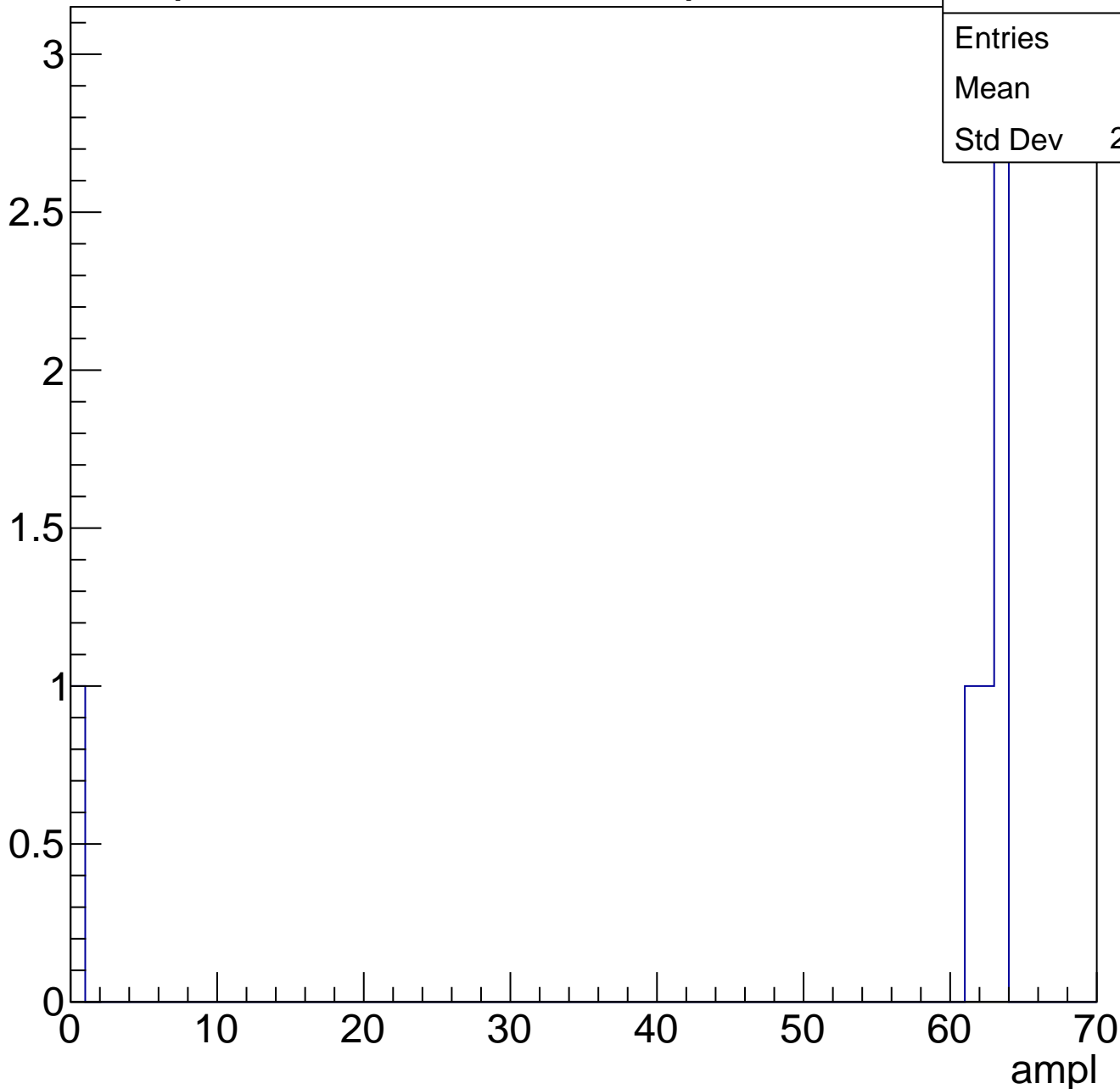
Entries	39
Mean	59.62
Std Dev	2.588



# B1L100S, U2-ch93, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	6
Mean	52
Std Dev	23.27



# B1L100S, U2-ch93, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



# B1L100S, U2-ch94, adc0

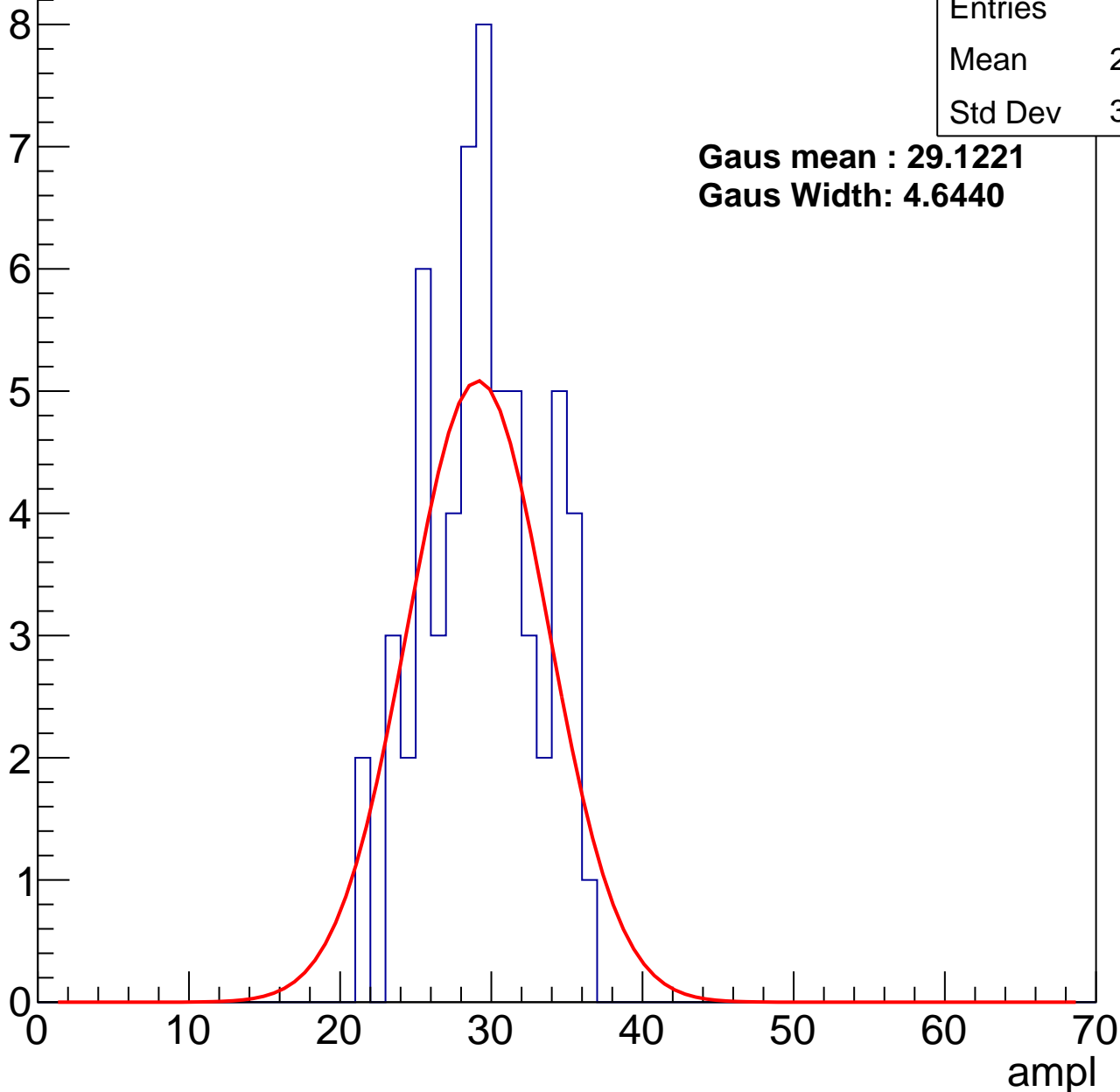
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	60
Mean	28.93
Std Dev	3.728

**Gaus mean : 29.1221**

**Gaus Width: 4.6440**



# B1L100S, U2-ch94, adc1

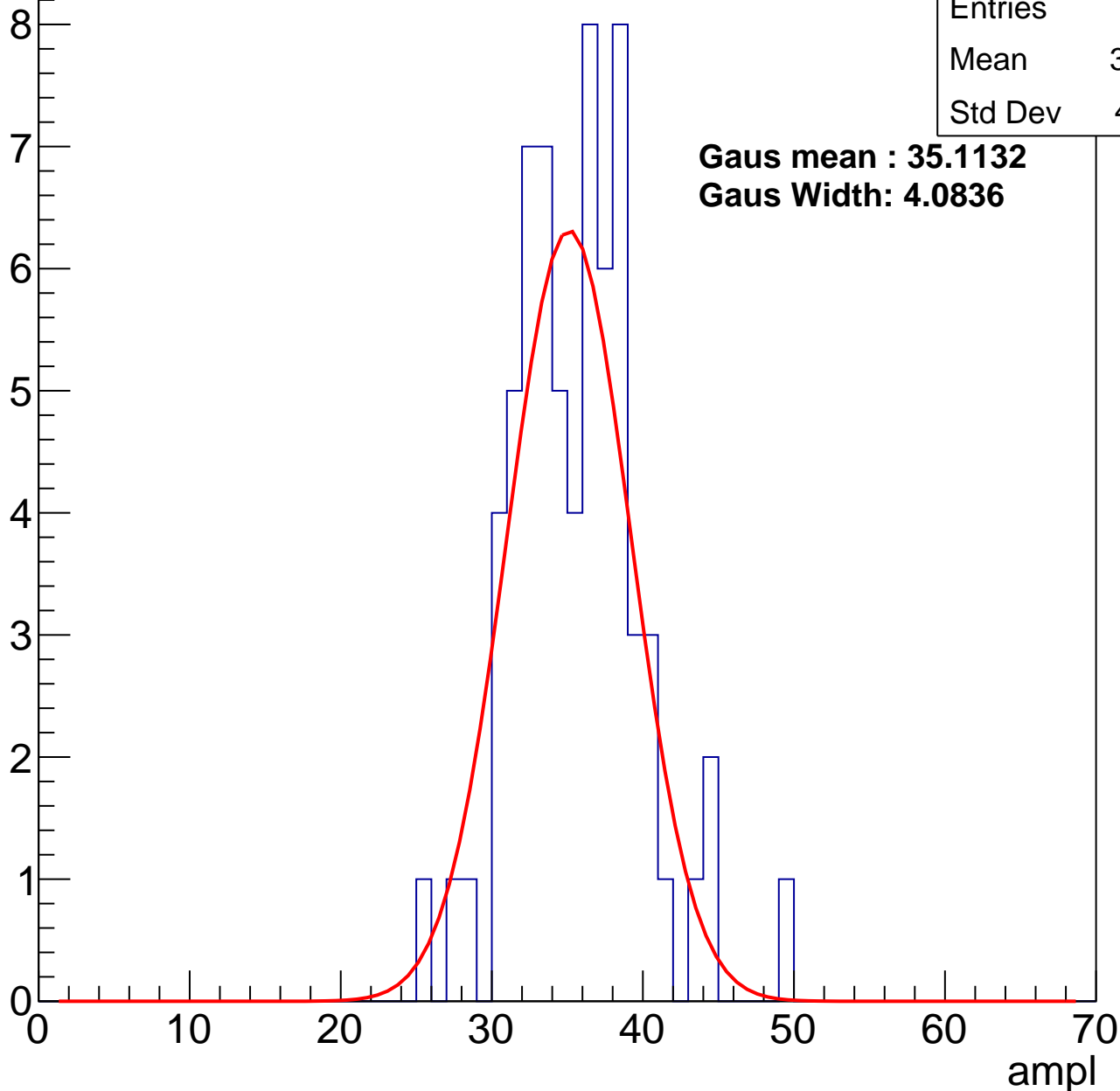
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	68
Mean	35.18
Std Dev	4.151

**Gaus mean : 35.1132**

**Gaus Width: 4.0836**



# B1L100S, U2-ch94, adc2

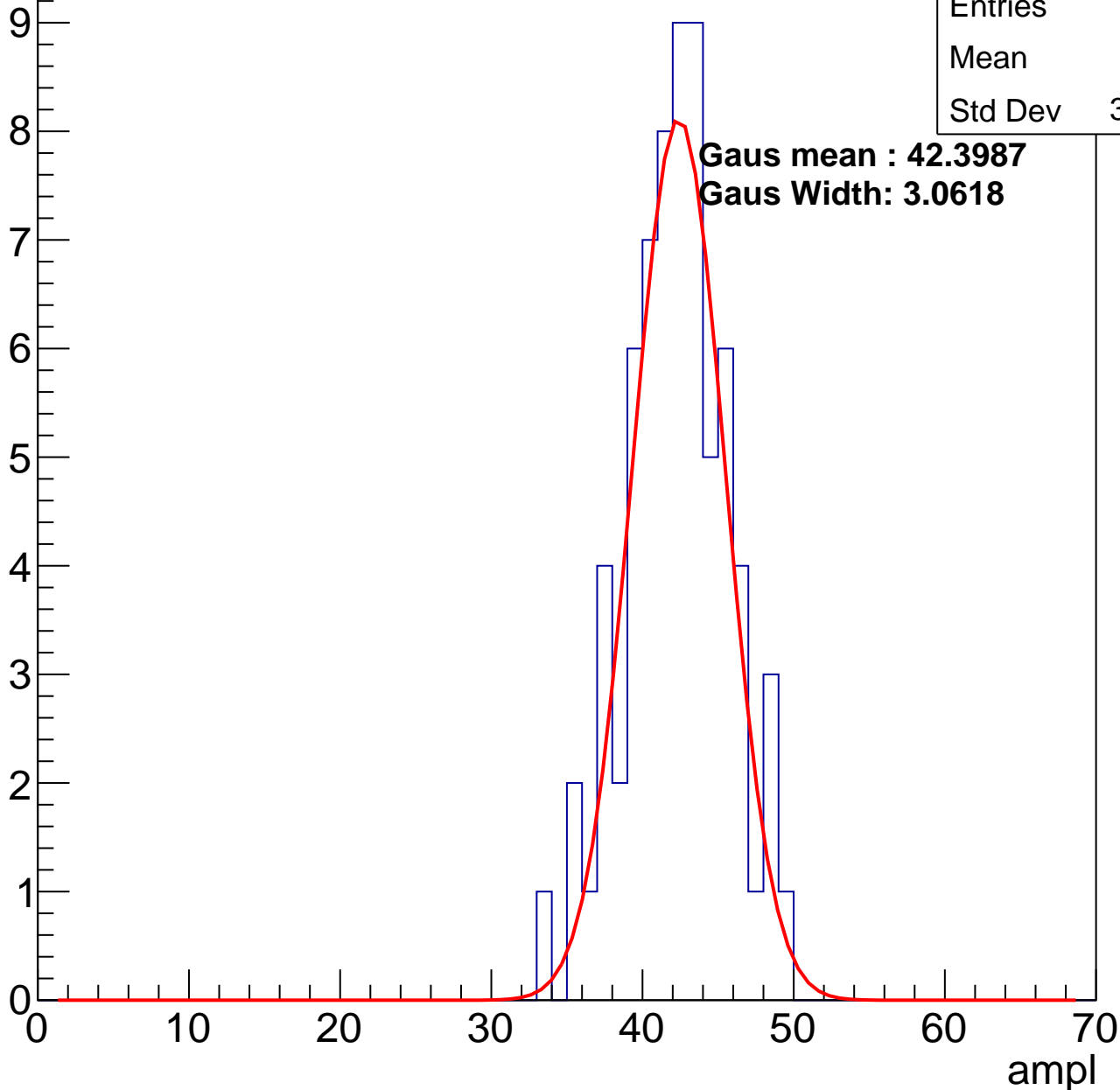
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	69
Mean	41.8
Std Dev	3.326

**Gaus mean : 42.3987**

**Gaus Width: 3.0618**

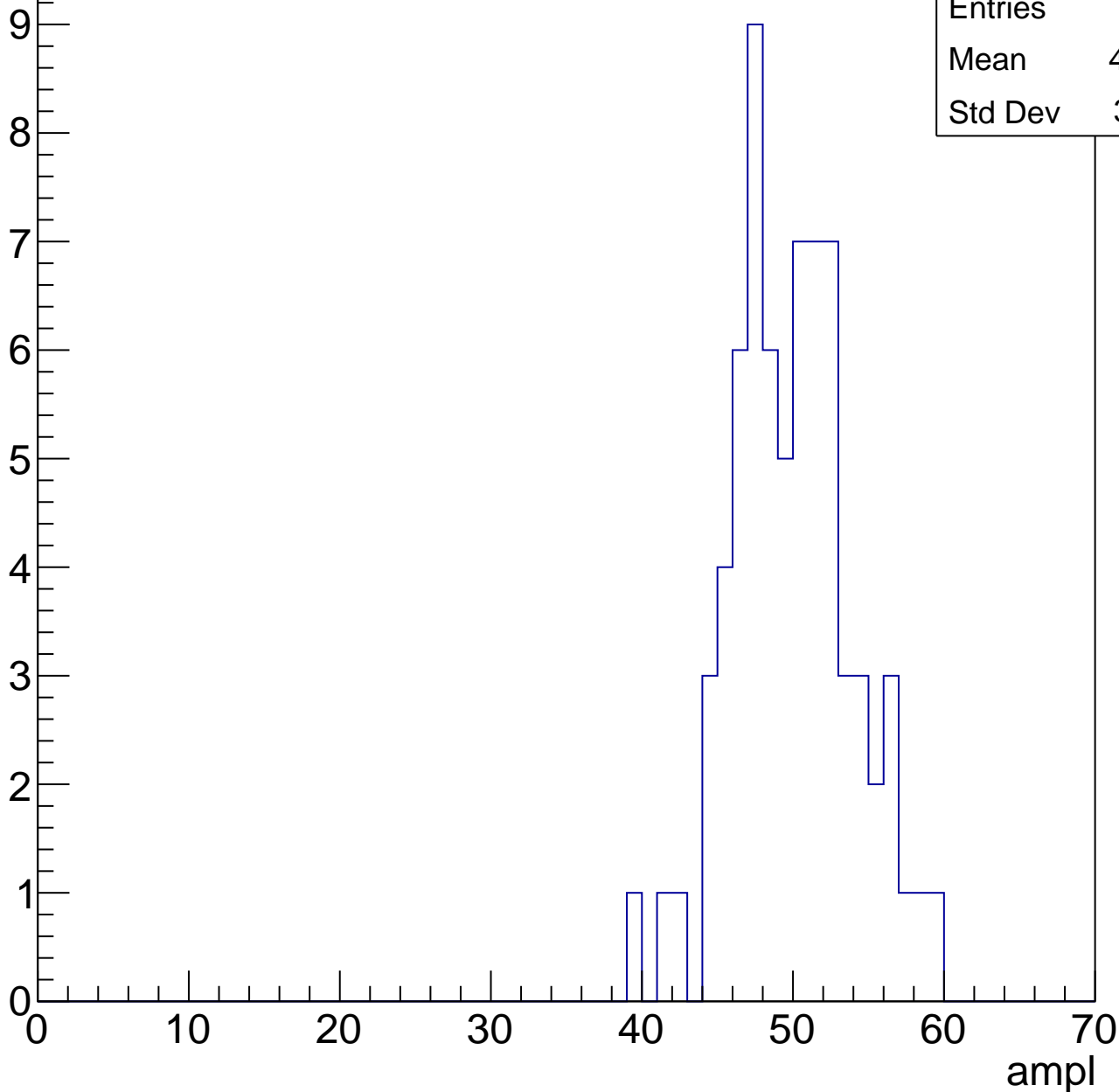


# B1L100S, U2-ch94, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	71
Mean	49.44
Std Dev	3.971

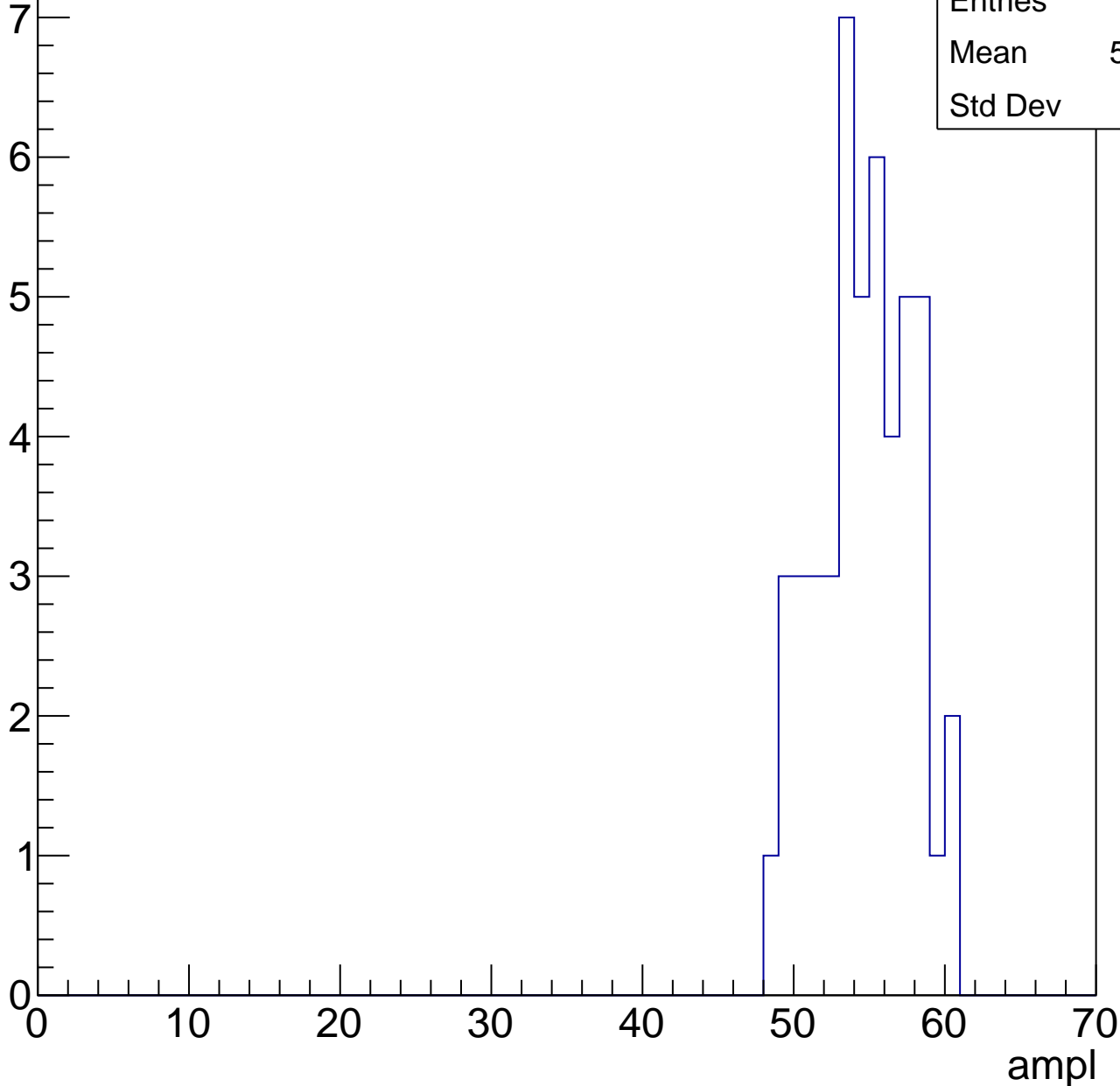


# B1L100S, U2-ch94, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	48
Mean	54.23
Std Dev	3.05



# B1L100S, U2-ch94, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

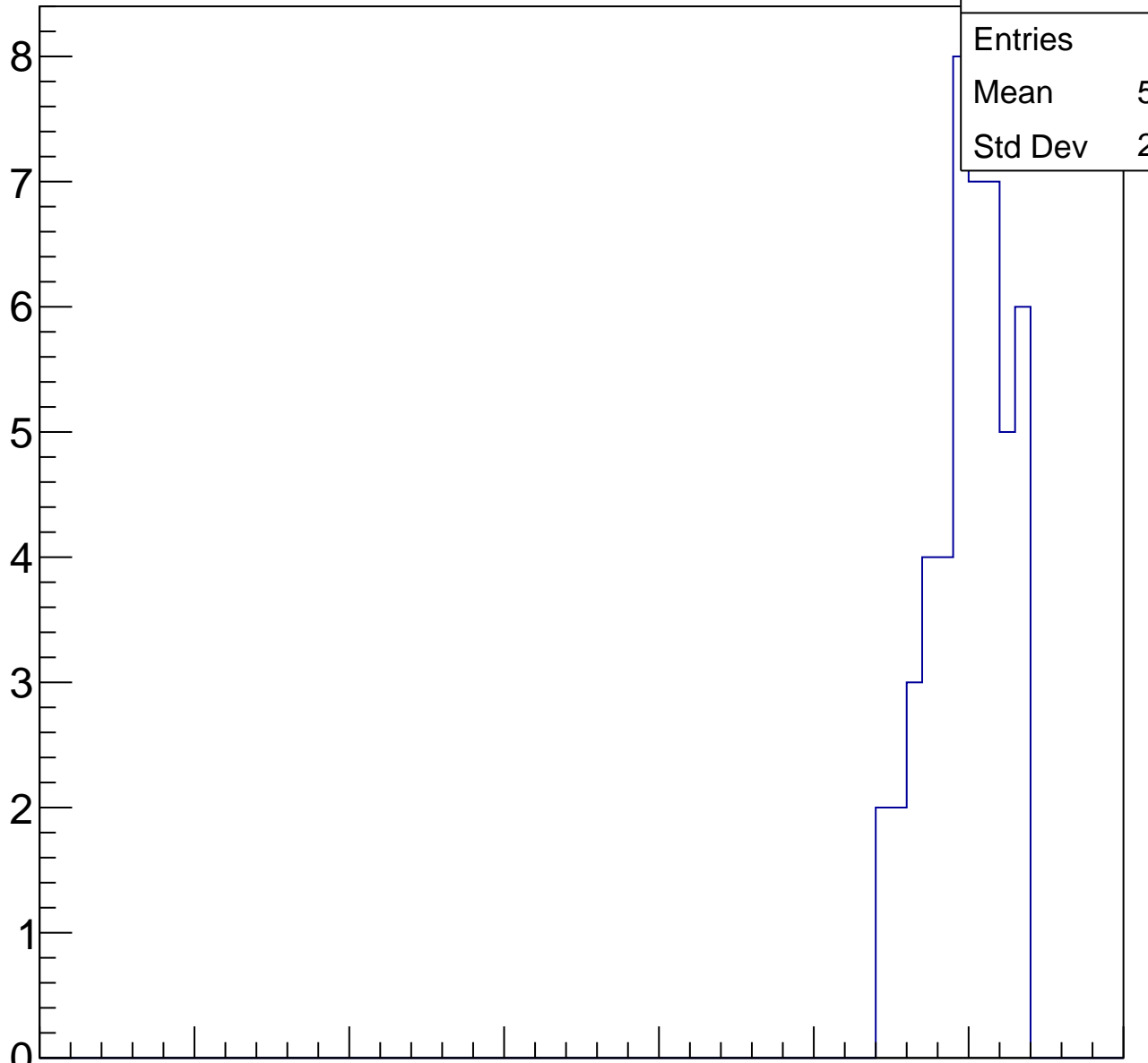
Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	48
Mean	59.44
Std Dev	2.482

ampl

0 10 20 30 40 50 60 70

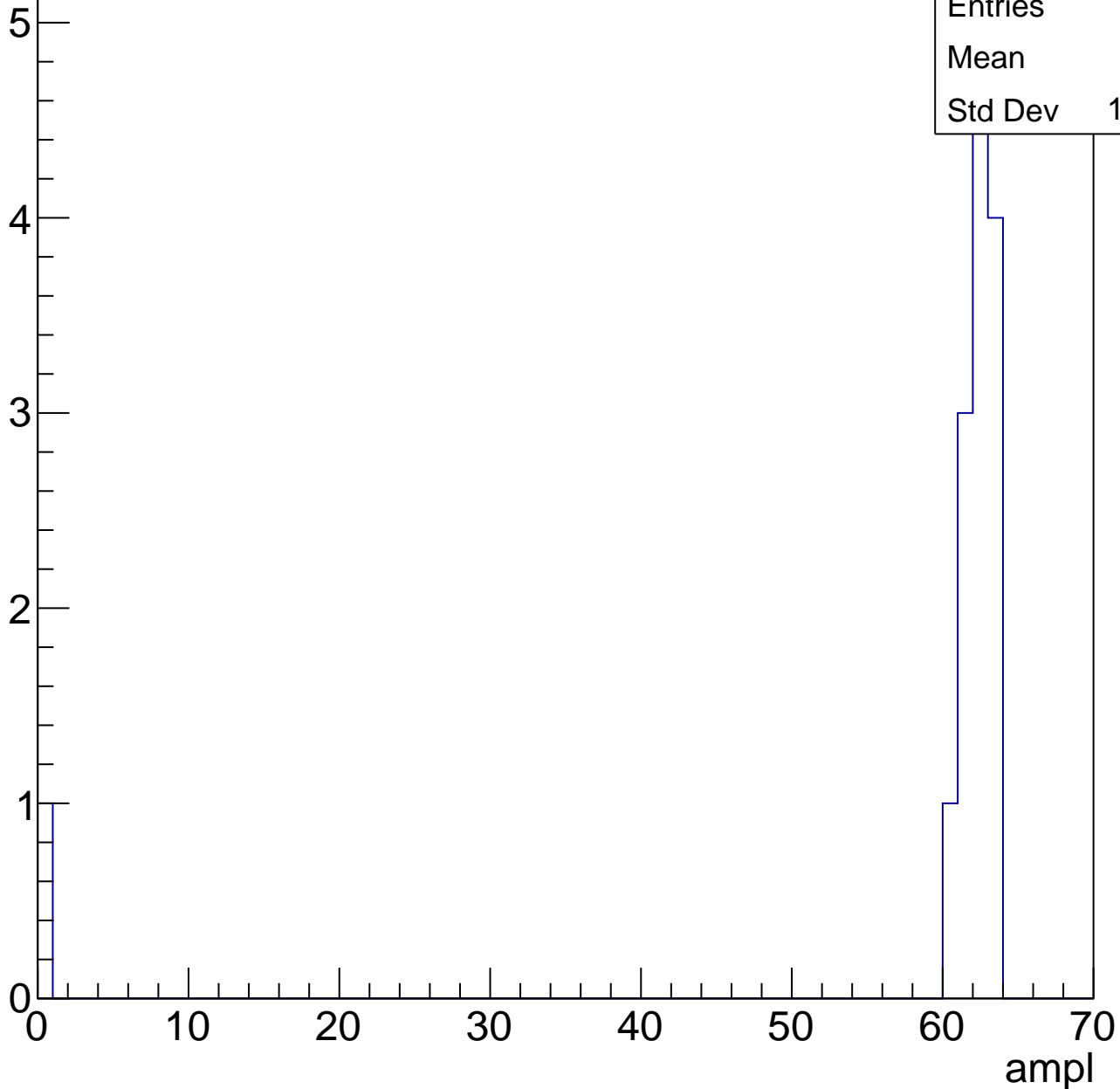


# B1L100S, U2-ch94, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	14
Mean	57.5
Std Dev	15.97





# B1L100S, U2-ch94, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L100S, U2-ch95, adc0

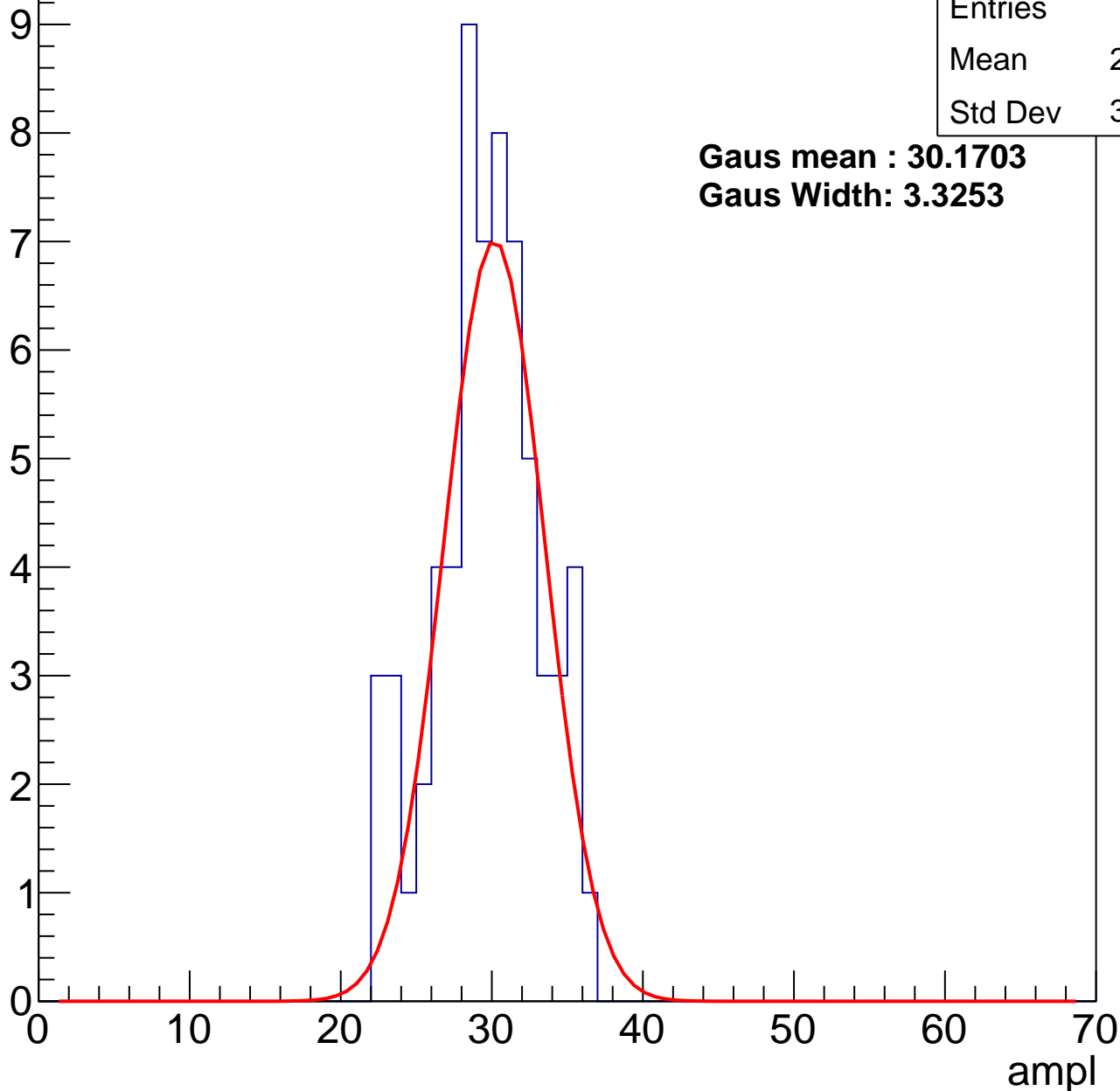
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	64
Mean	29.22
Std Dev	3.462

**Gaus mean : 30.1703**

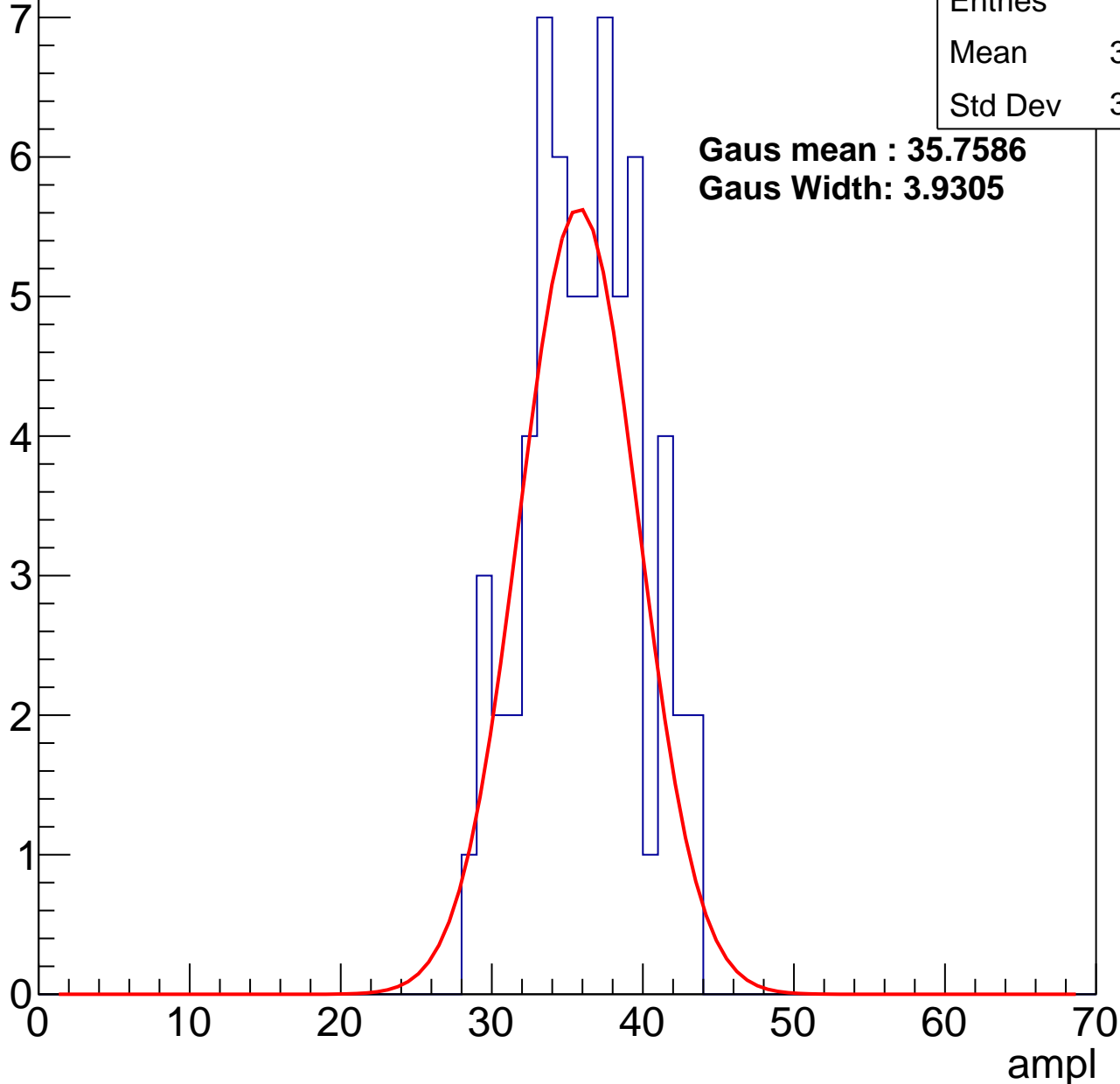
**Gaus Width: 3.3253**



# B1L100S, U2-ch95, adc1

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



# B1L100S, U2-ch95, adc2

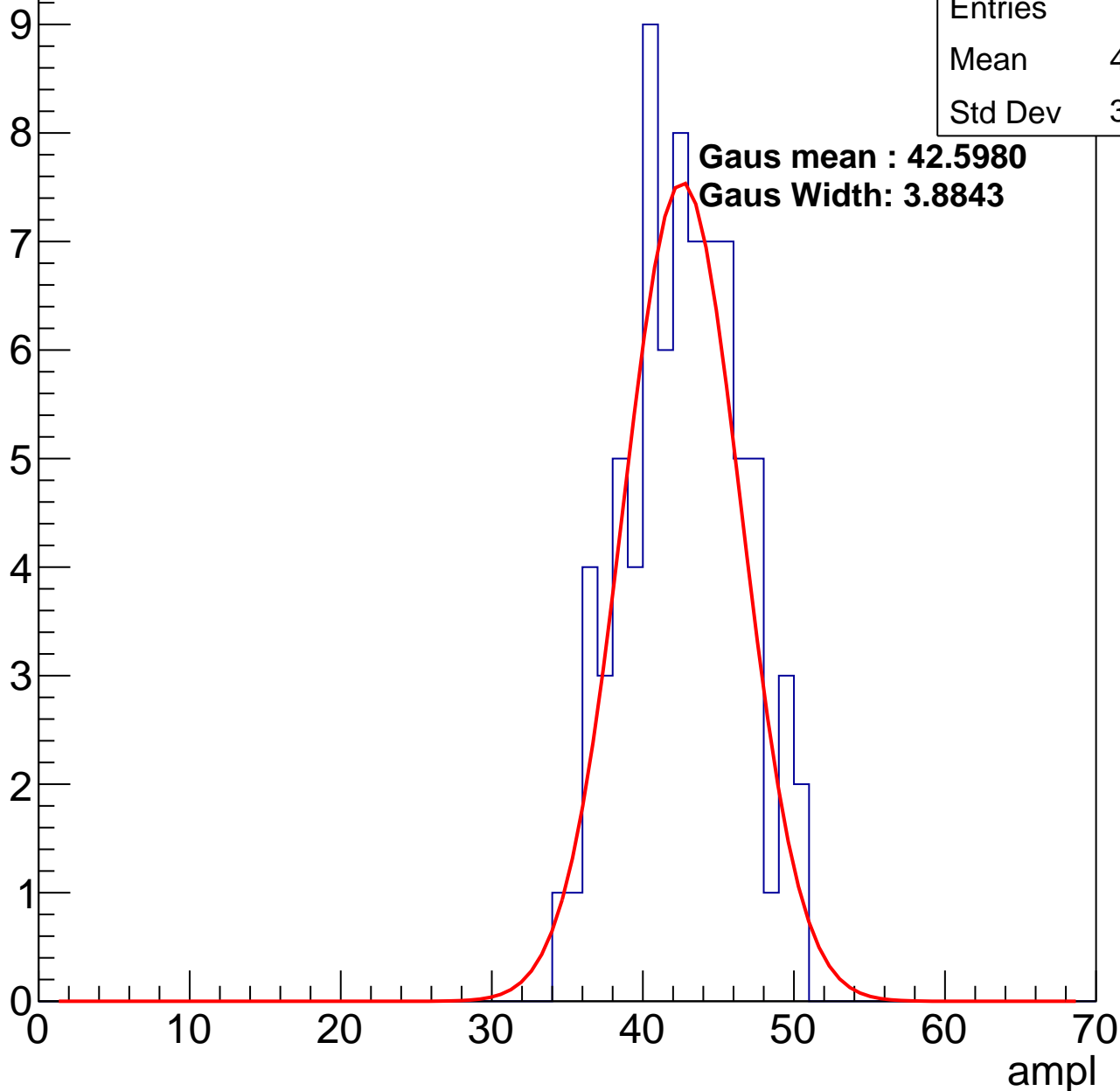
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	78
Mean	42.26
Std Dev	3.753

**Gaus mean : 42.5980**

**Gaus Width: 3.8843**



# B1L100S, U2-ch95, adc3

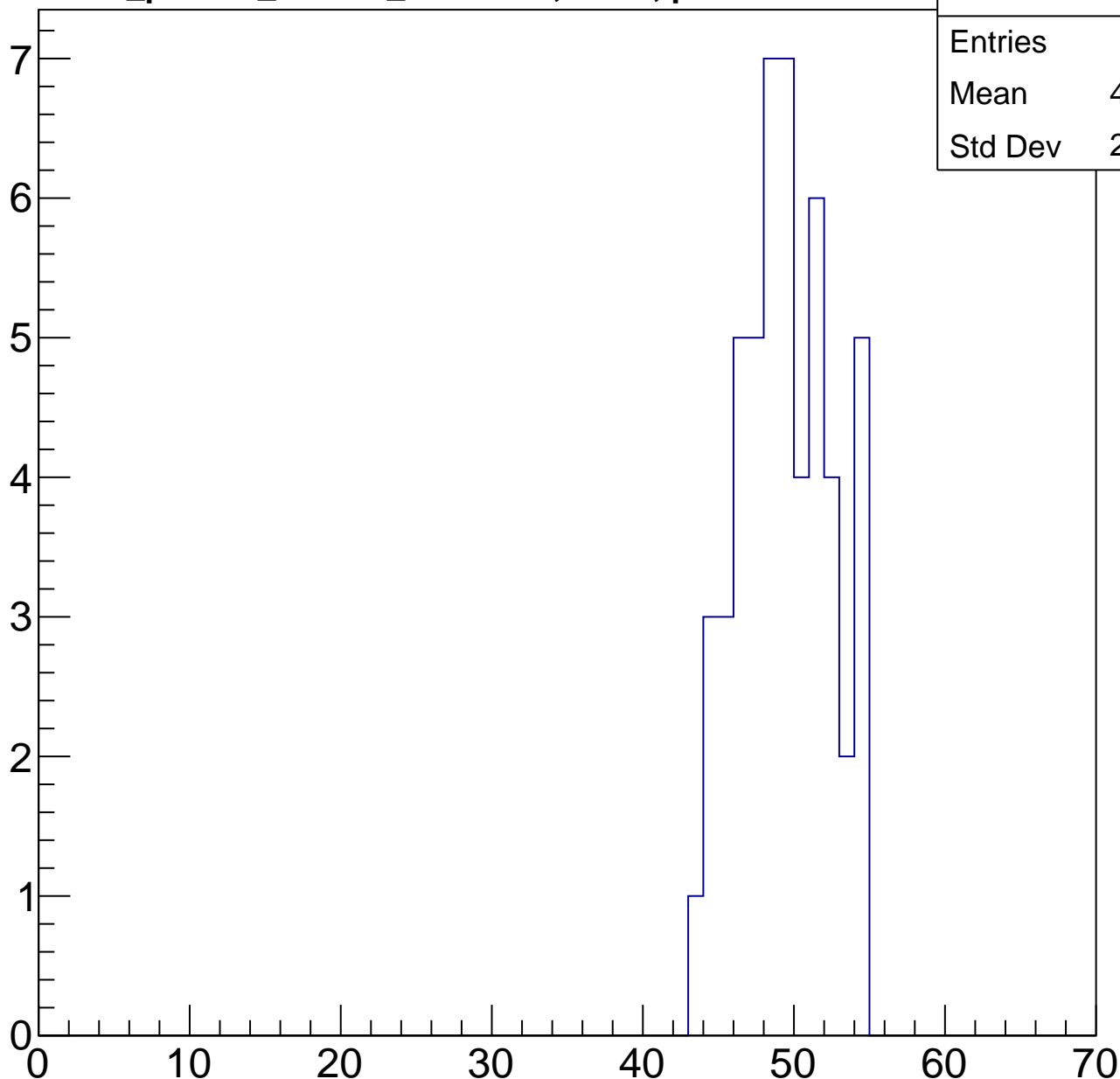
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

7  
6  
5  
4  
3  
2  
1  
0

Entries	52
Mean	48.92
Std Dev	2.947

ampl



# B1L100S, U2-ch95, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

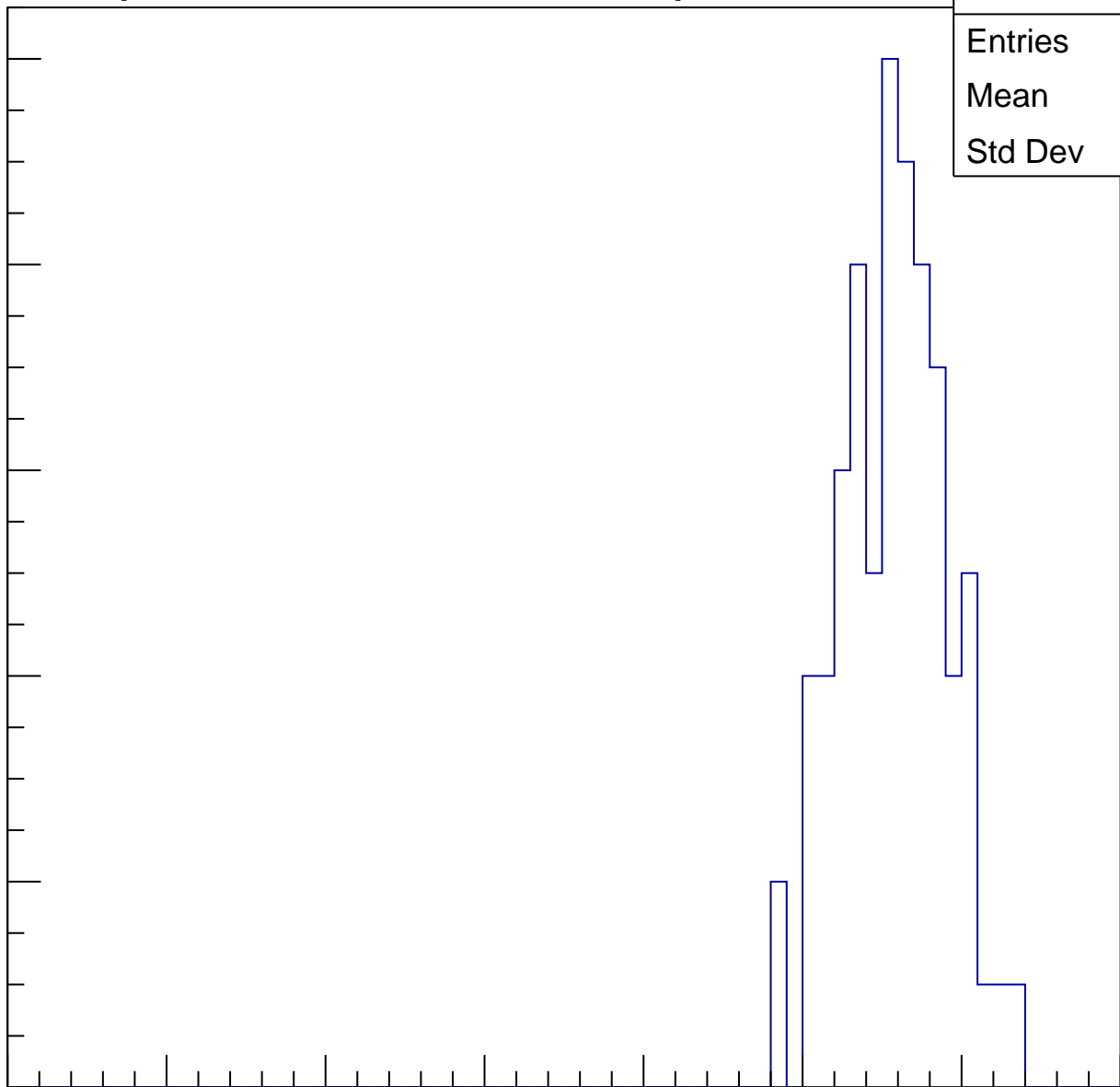
Entries	75
Mean	55.25
Std Dev	3.246

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

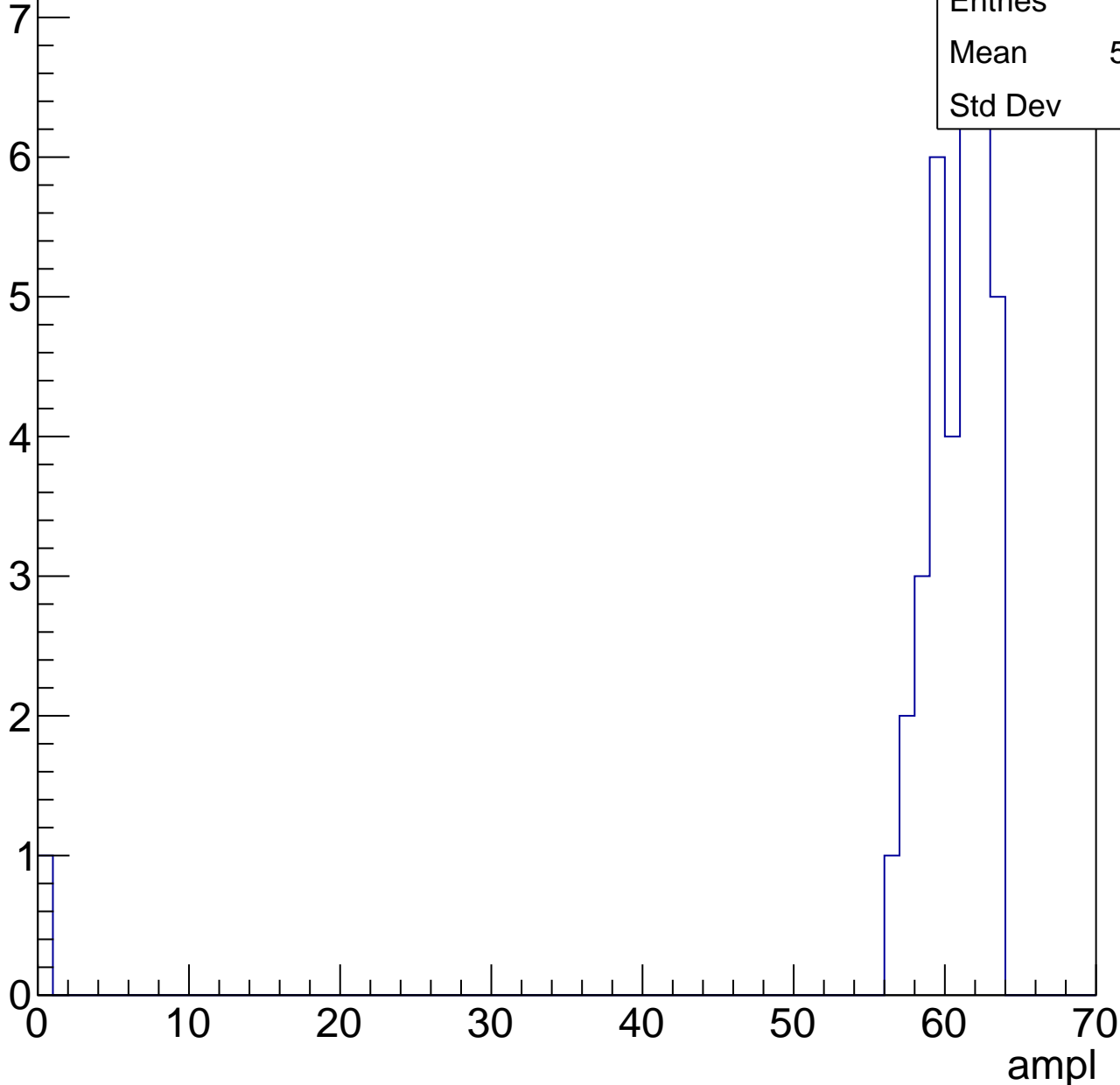


# B1L100S, U2-ch95, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

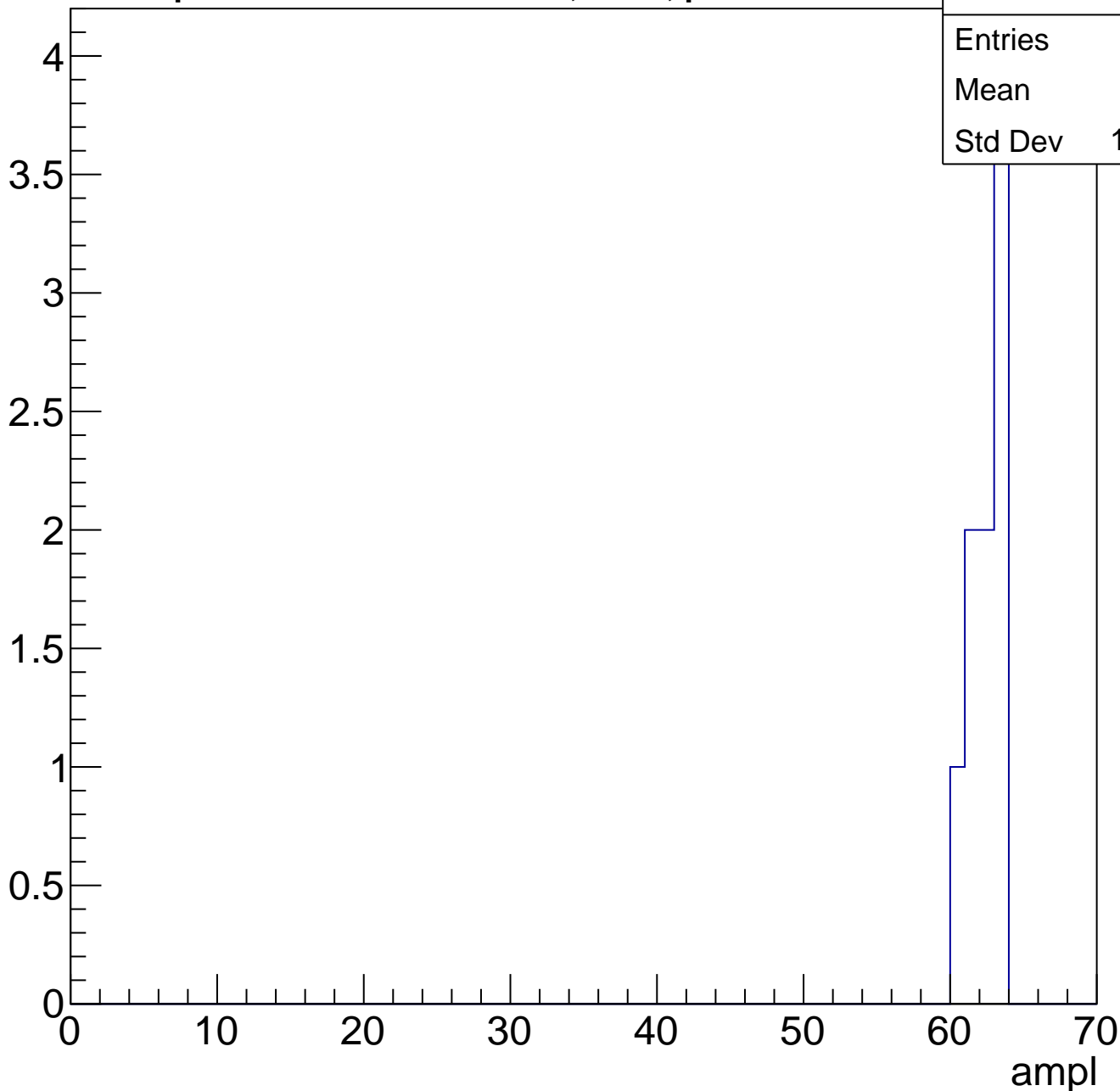
Entries	36
Mean	58.72
Std Dev	10.1



# B1L100S, U2-ch95, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry





# B1L100S, U2-ch95, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L100S, U2-ch96, adc0

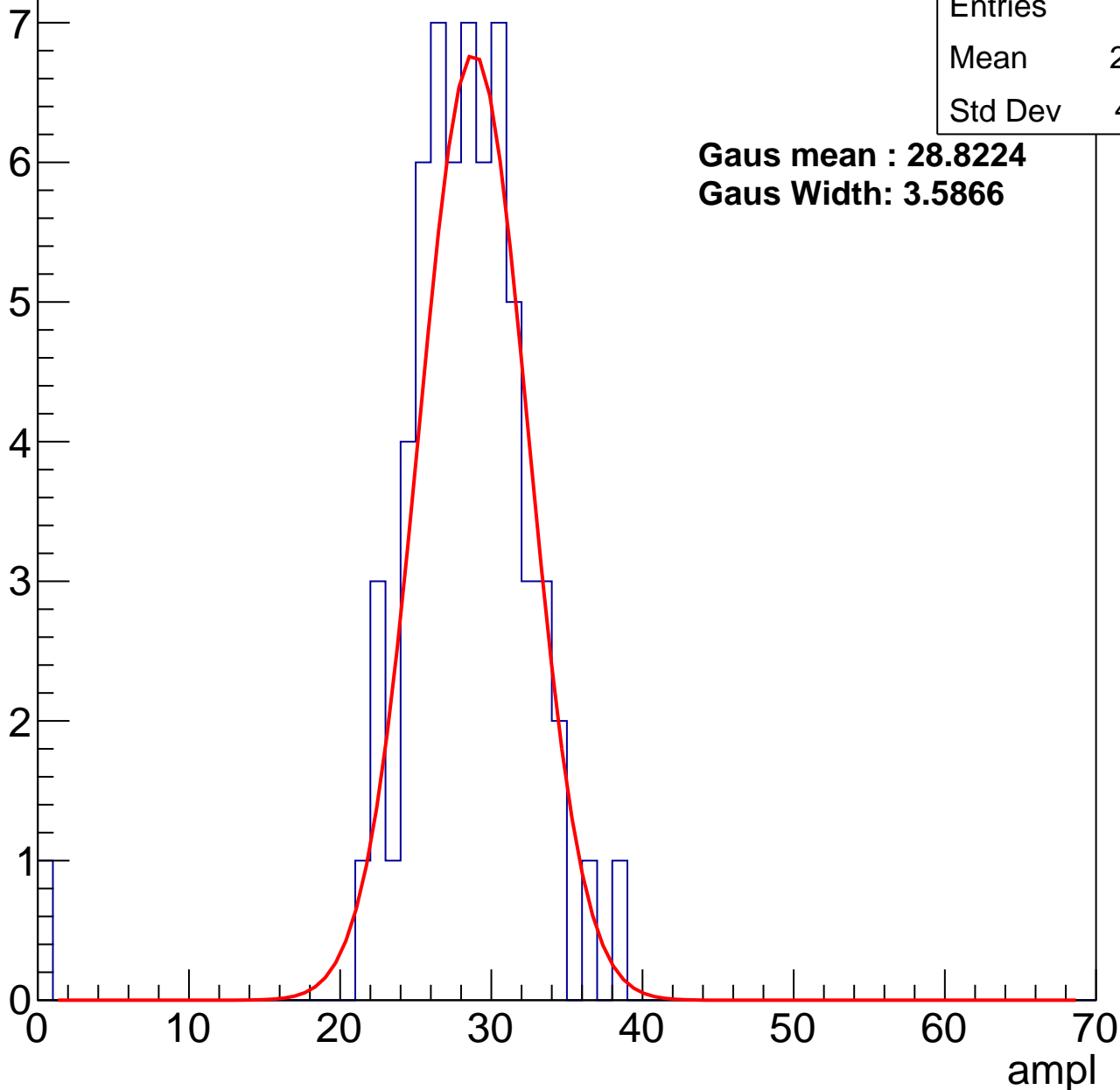
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	64
Mean	27.69
Std Dev	4.921

**Gaus mean : 28.8224**

**Gaus Width: 3.5866**



# B1L100S, U2-ch96, adc1

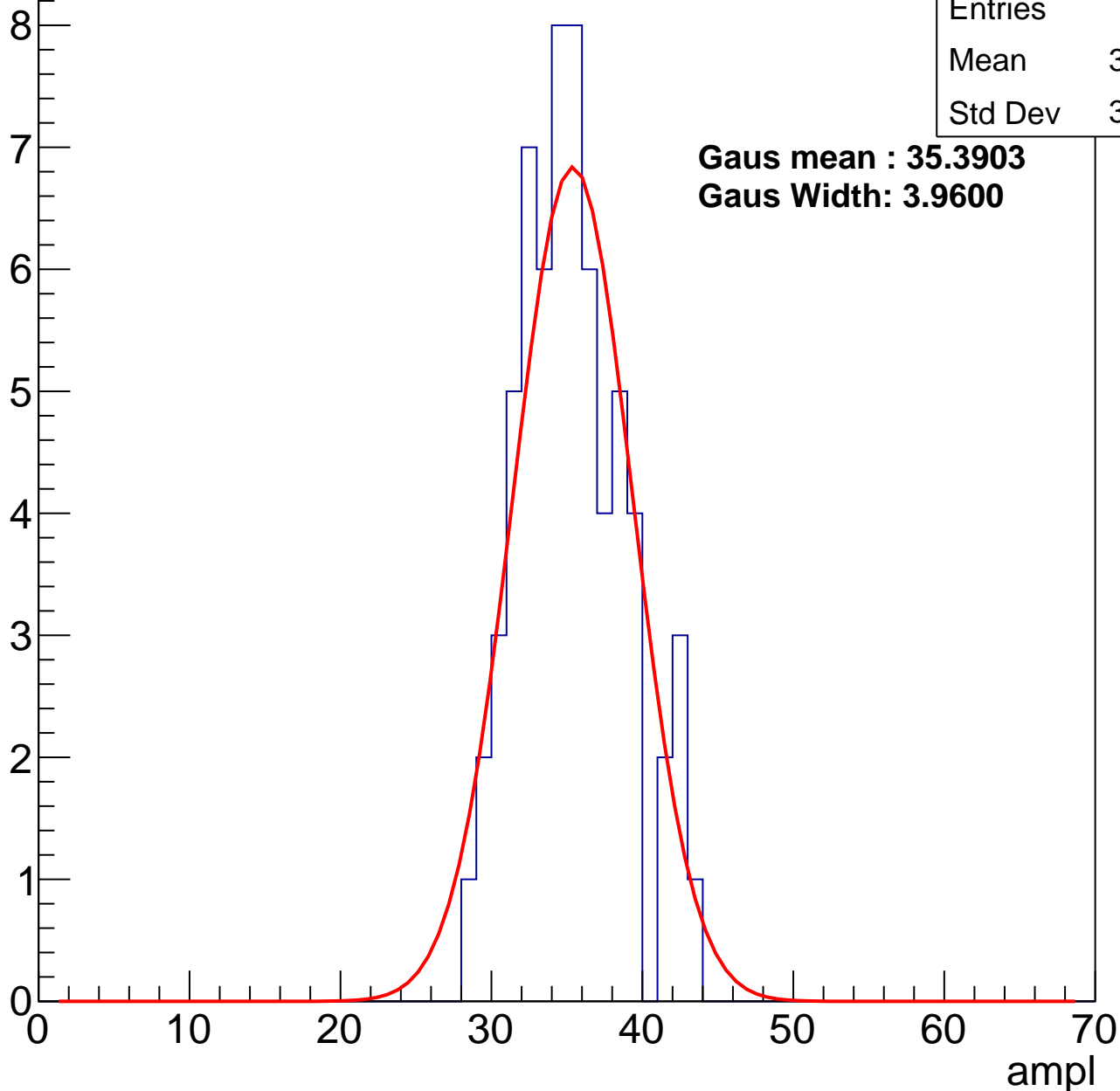
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	65
Mean	34.86
Std Dev	3.472

**Gaus mean : 35.3903**

**Gaus Width: 3.9600**



# B1L100S, U2-ch96, adc2

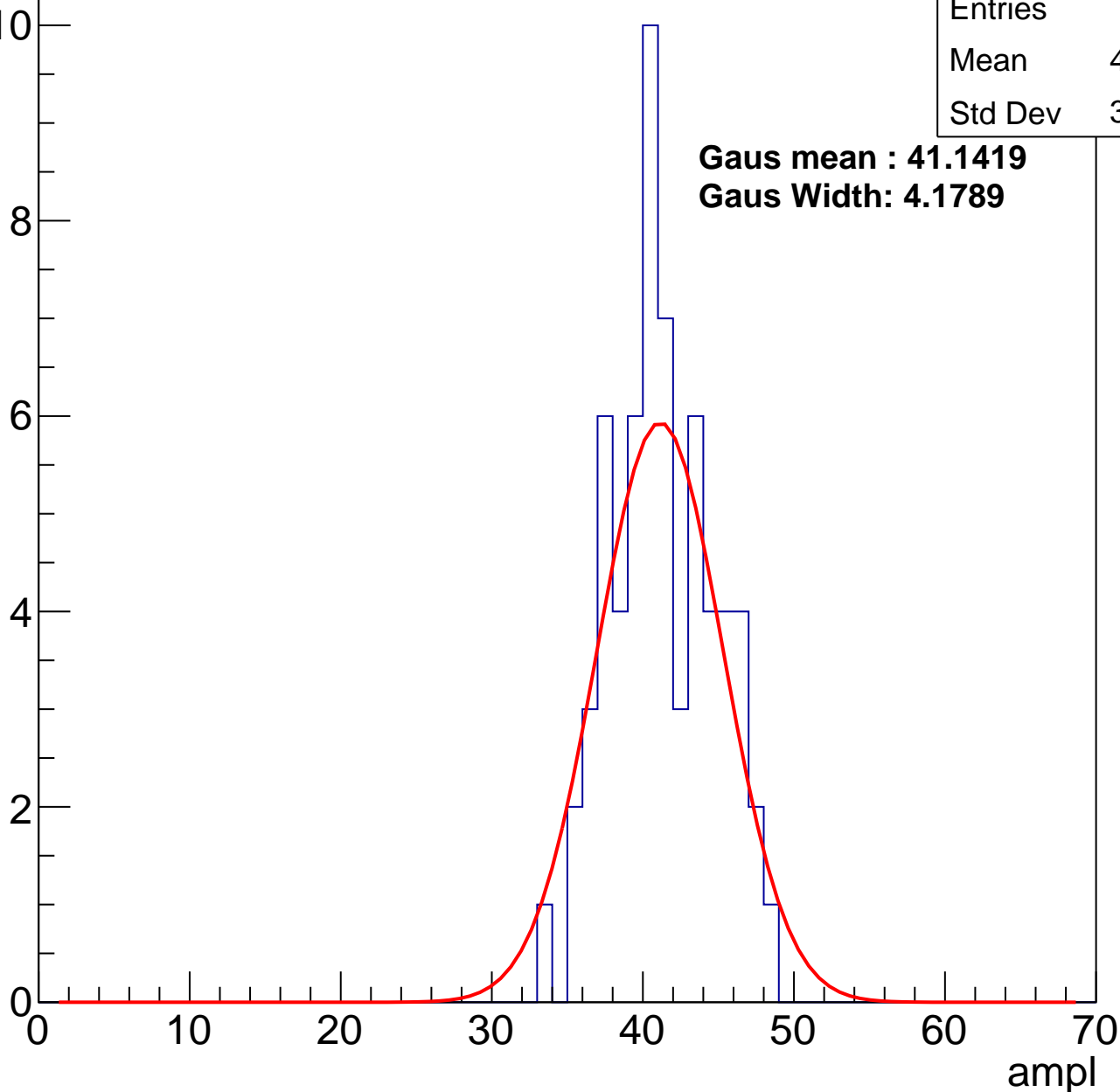
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	63
Mean	40.83
Std Dev	3.388

**Gaus mean : 41.1419**

**Gaus Width: 4.1789**

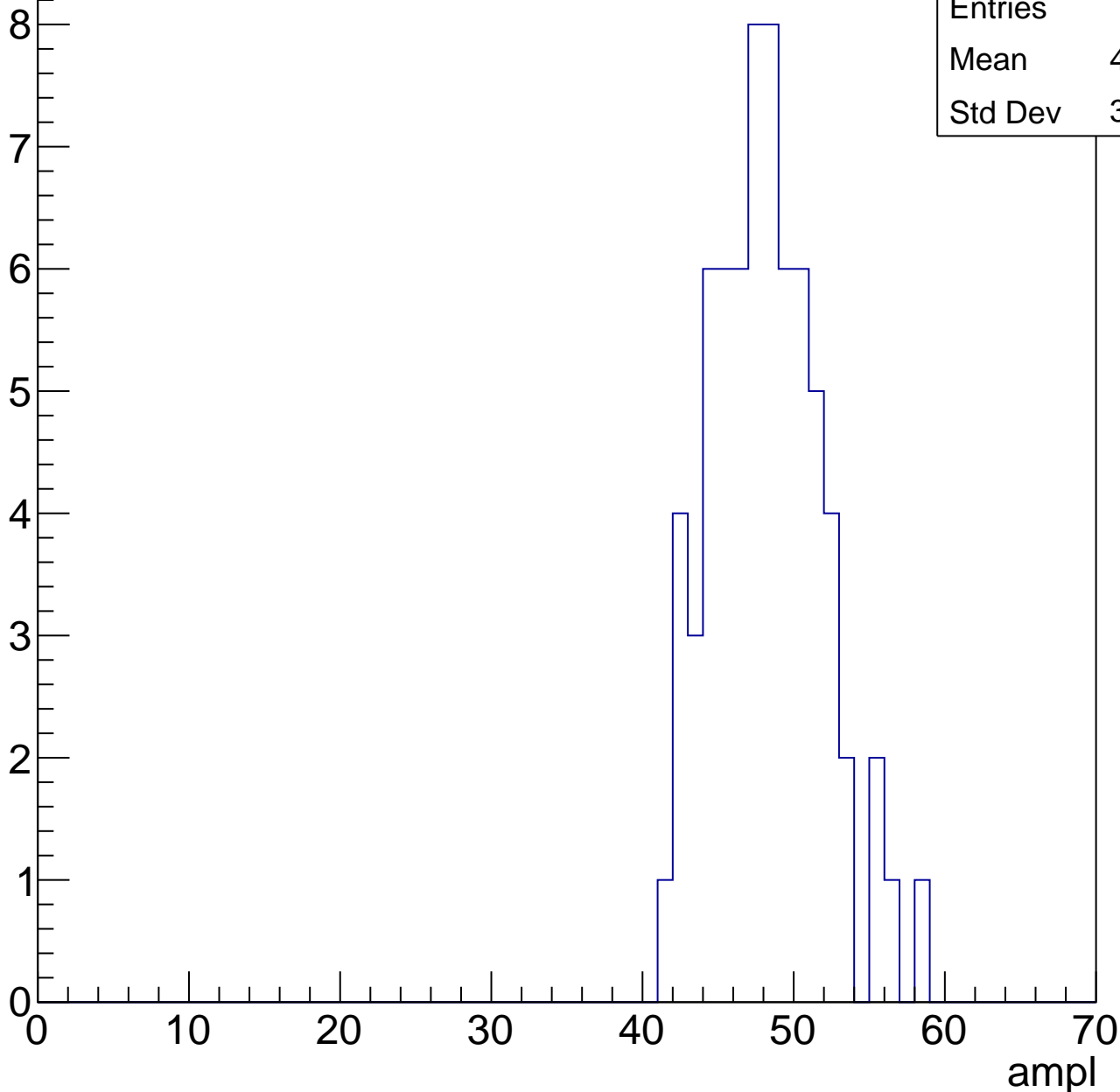


# B1L100S, U2-ch96, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

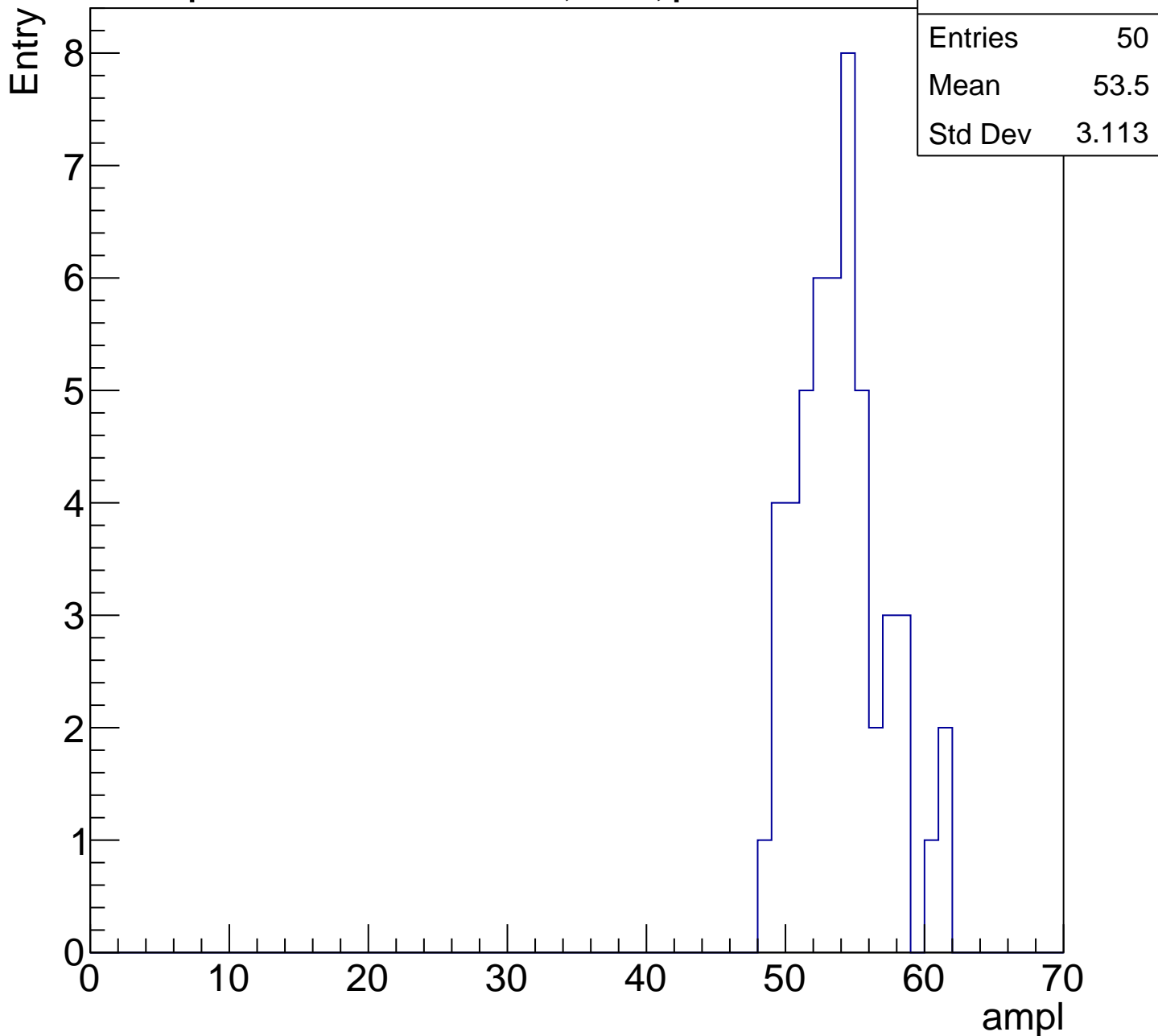
Entry

Entries	69
Mean	47.75
Std Dev	3.605



# B1L100S, U2-ch96, adc4

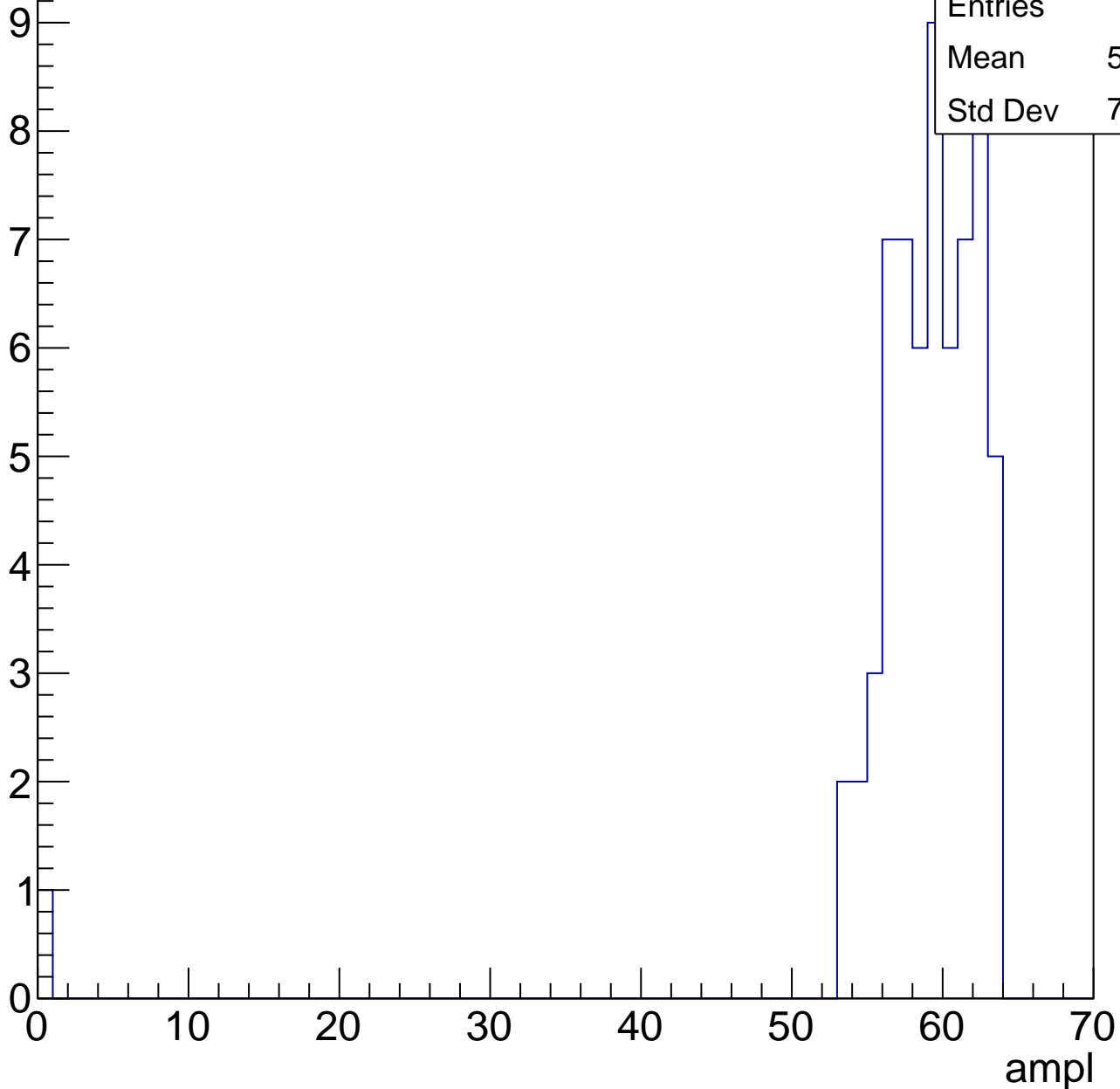
calib\_packv5\_042523\_0143.root, FC#4, port A2



# B1L100S, U2-ch96, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

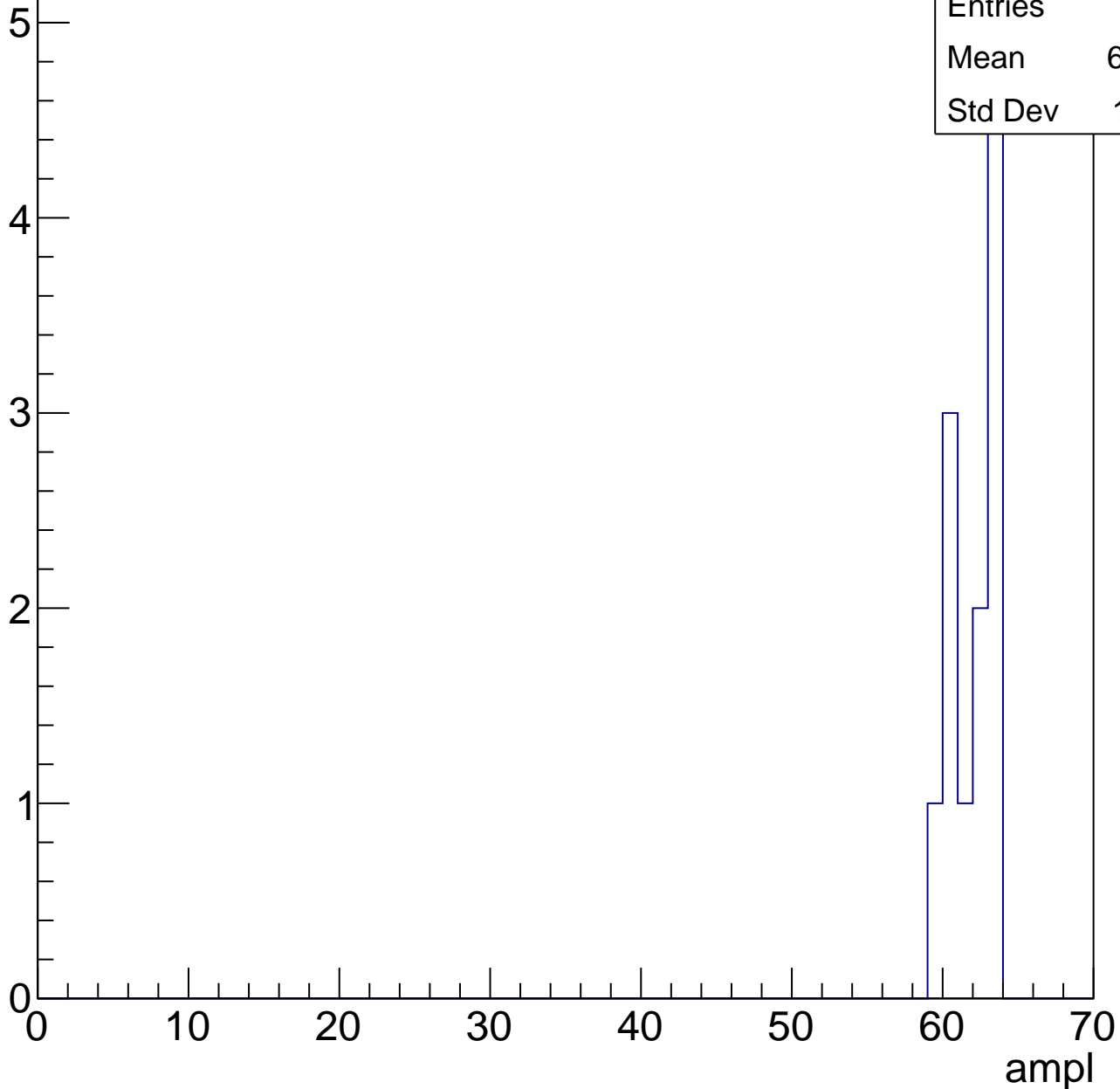


# B1L100S, U2-ch96, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	12
Mean	61.58
Std Dev	1.441





# B1L100S, U2-ch96, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L100S, U2-ch97, adc0

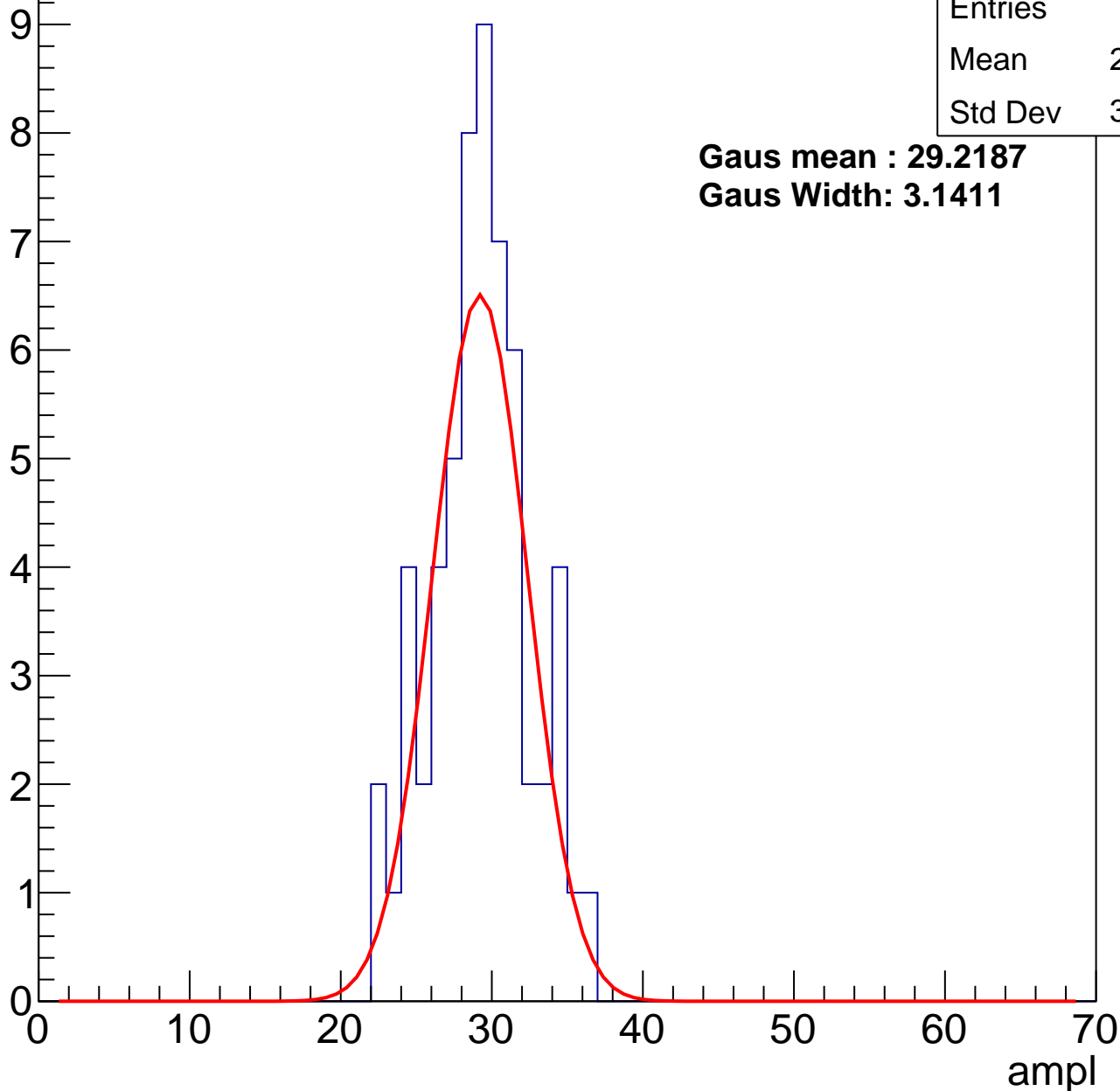
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	58
Mean	28.79
Std Dev	3.199

**Gaus mean : 29.2187**

**Gaus Width: 3.1411**



# B1L100S, U2-ch97, adc1

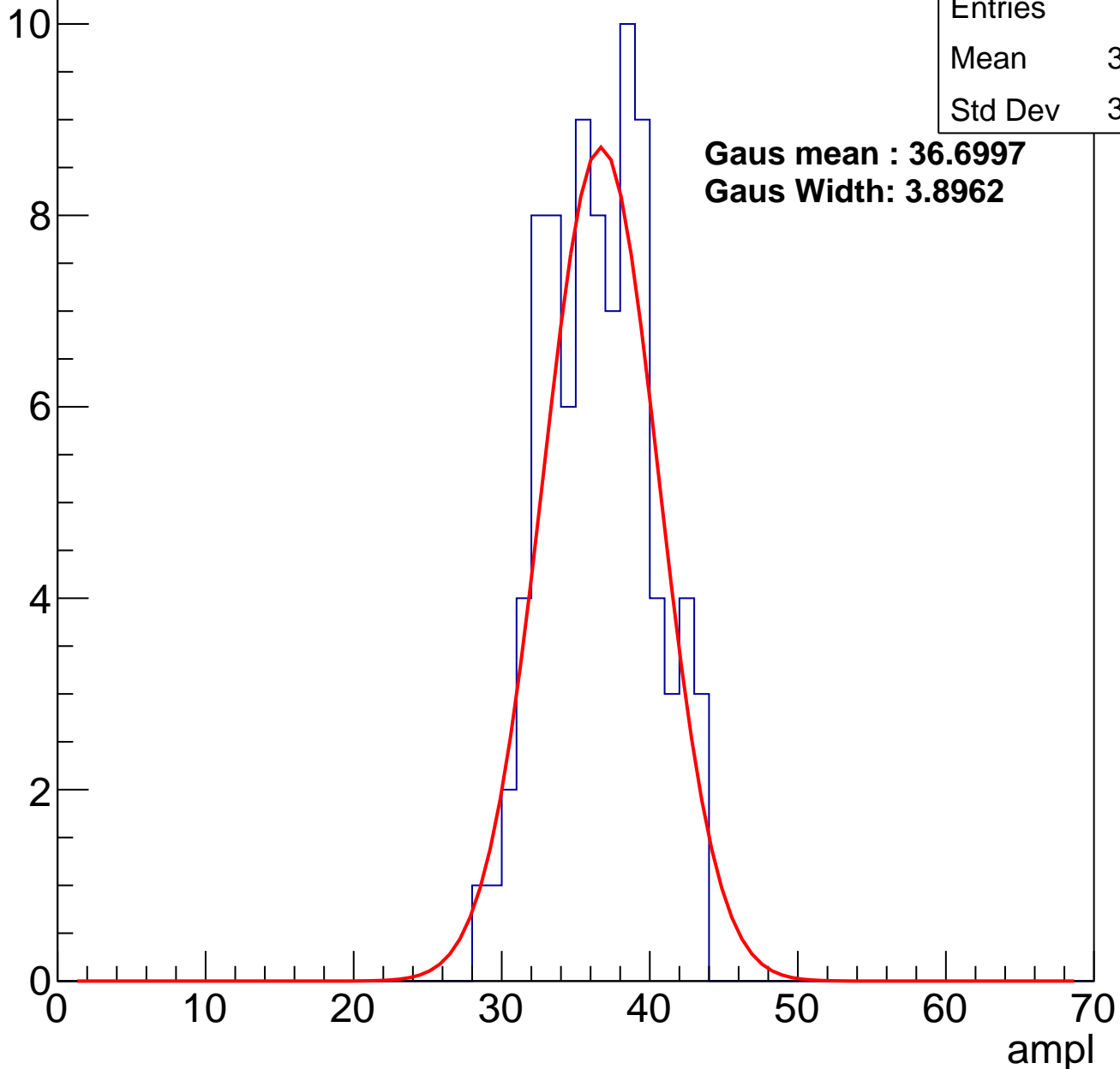
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	87
Mean	36.07
Std Dev	3.516

**Gaus mean : 36.6997**

**Gaus Width: 3.8962**

Entry



# B1L100S, U2-ch97, adc2

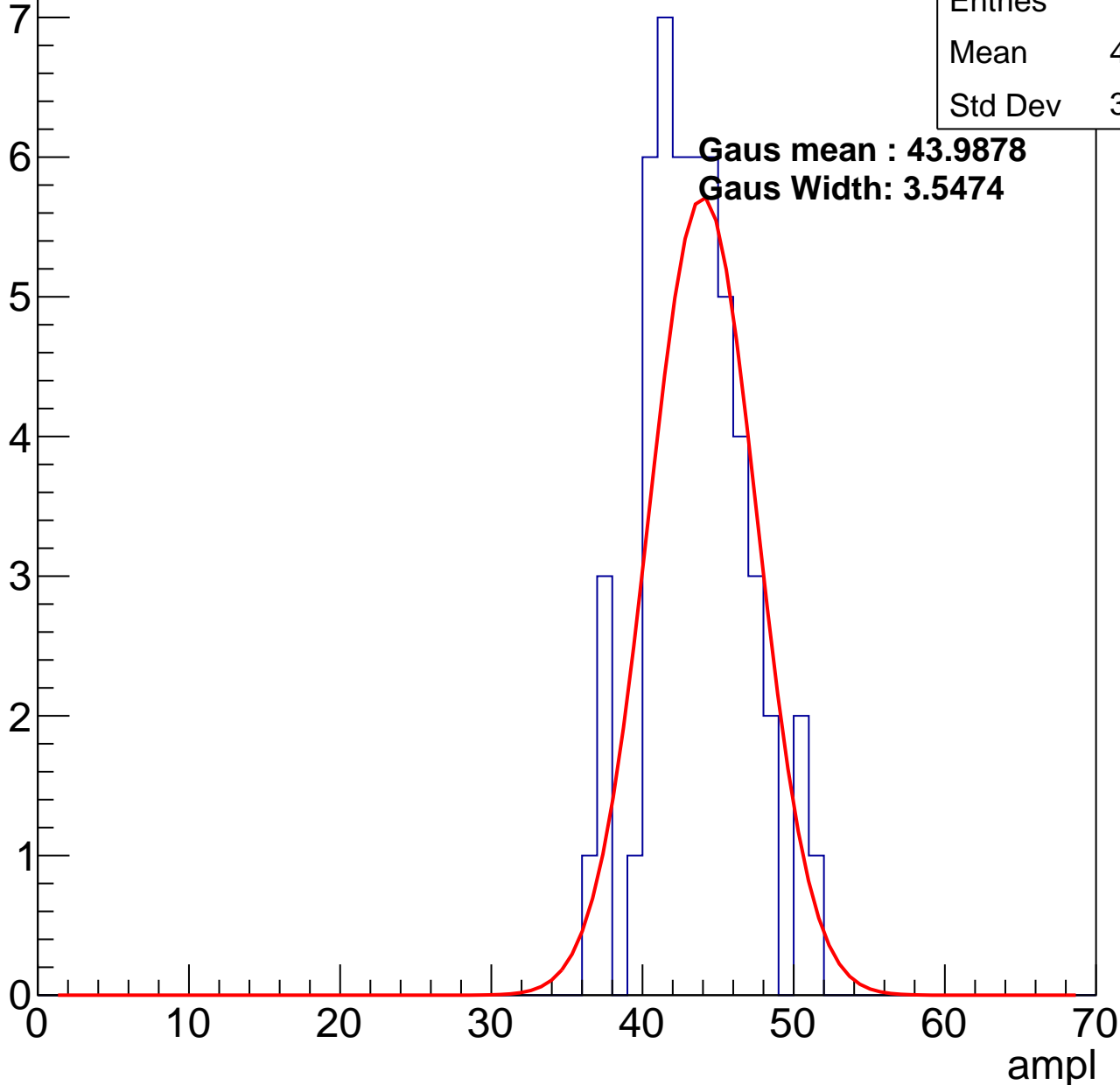
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	53
Mean	43.09
Std Dev	3.315

**Gaus mean : 43.9878**

**Gaus Width: 3.5474**

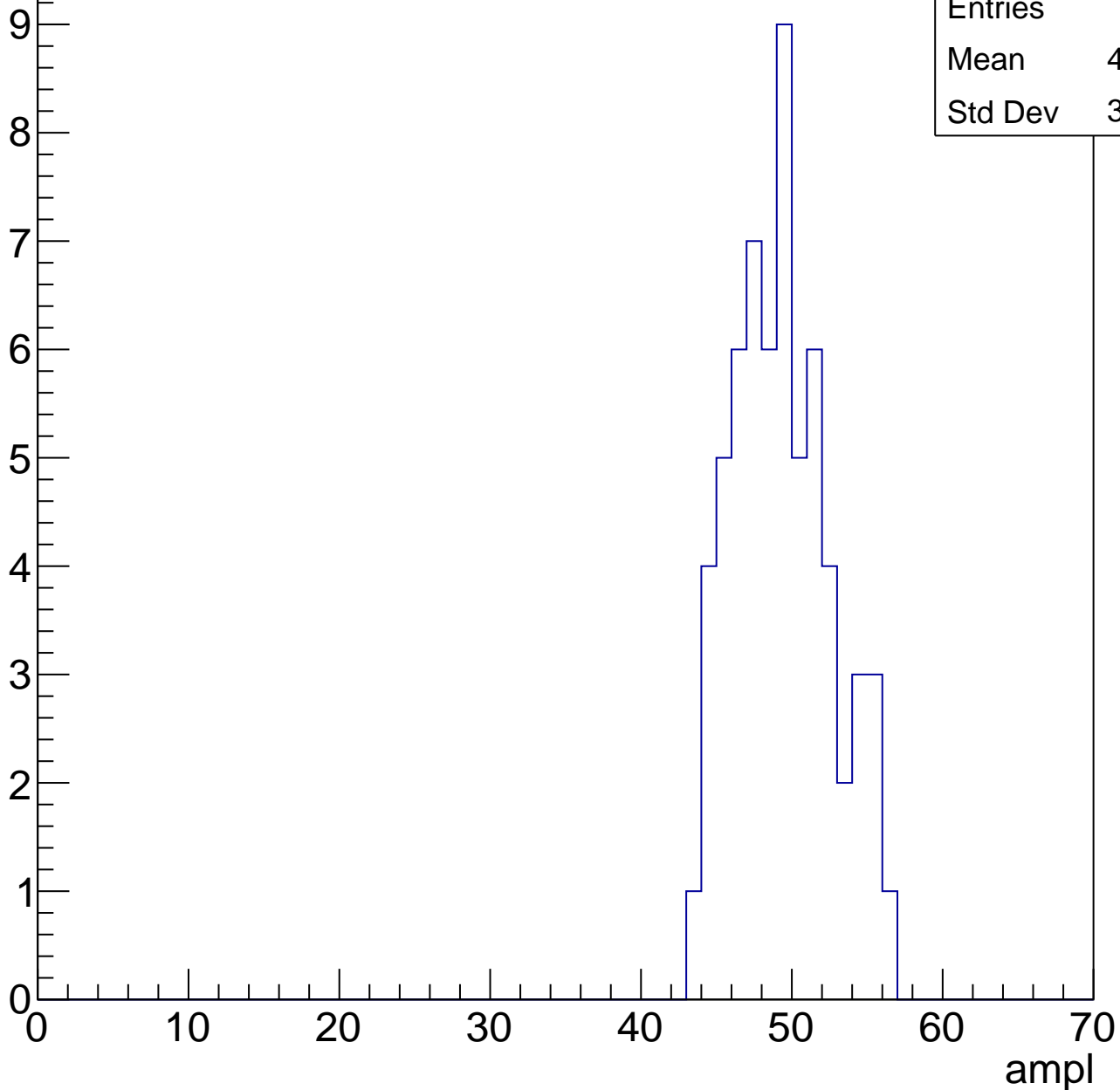


# B1L100S, U2-ch97, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

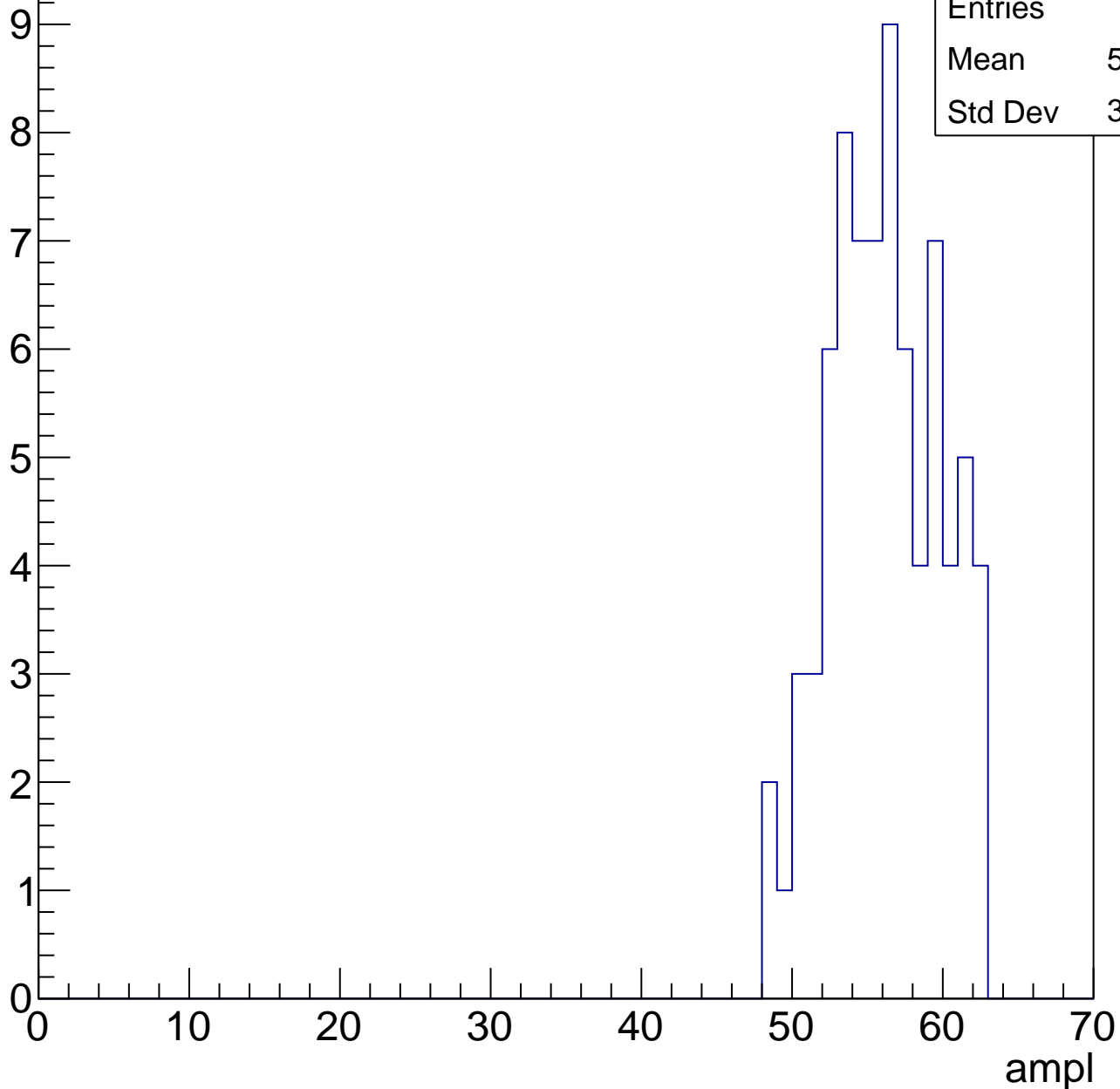
Entries	62
Mean	48.89
Std Dev	3.193



# B1L100S, U2-ch97, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

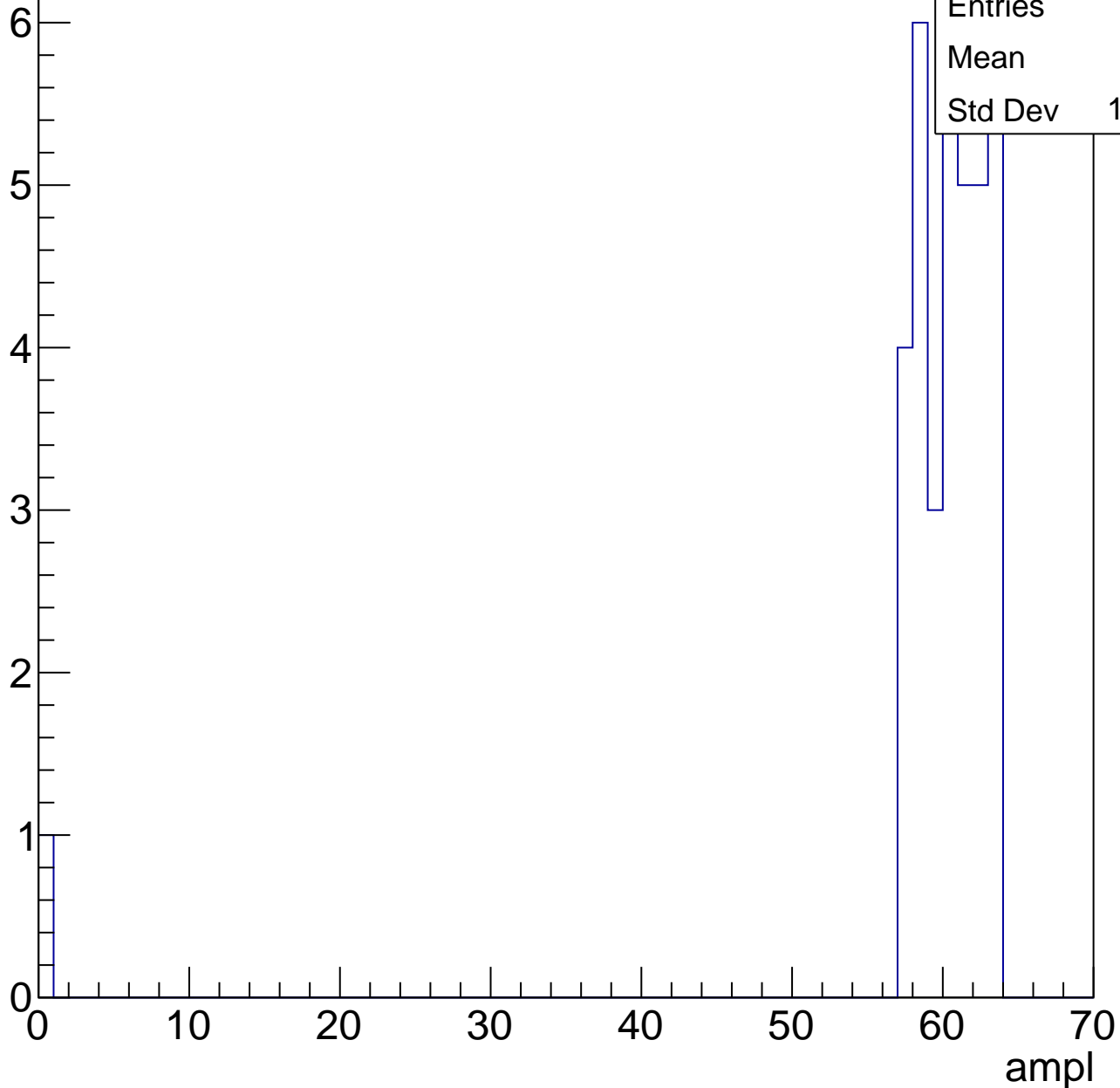


Entries	76
Mean	55.67
Std Dev	3.578

# B1L100S, U2-ch97, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

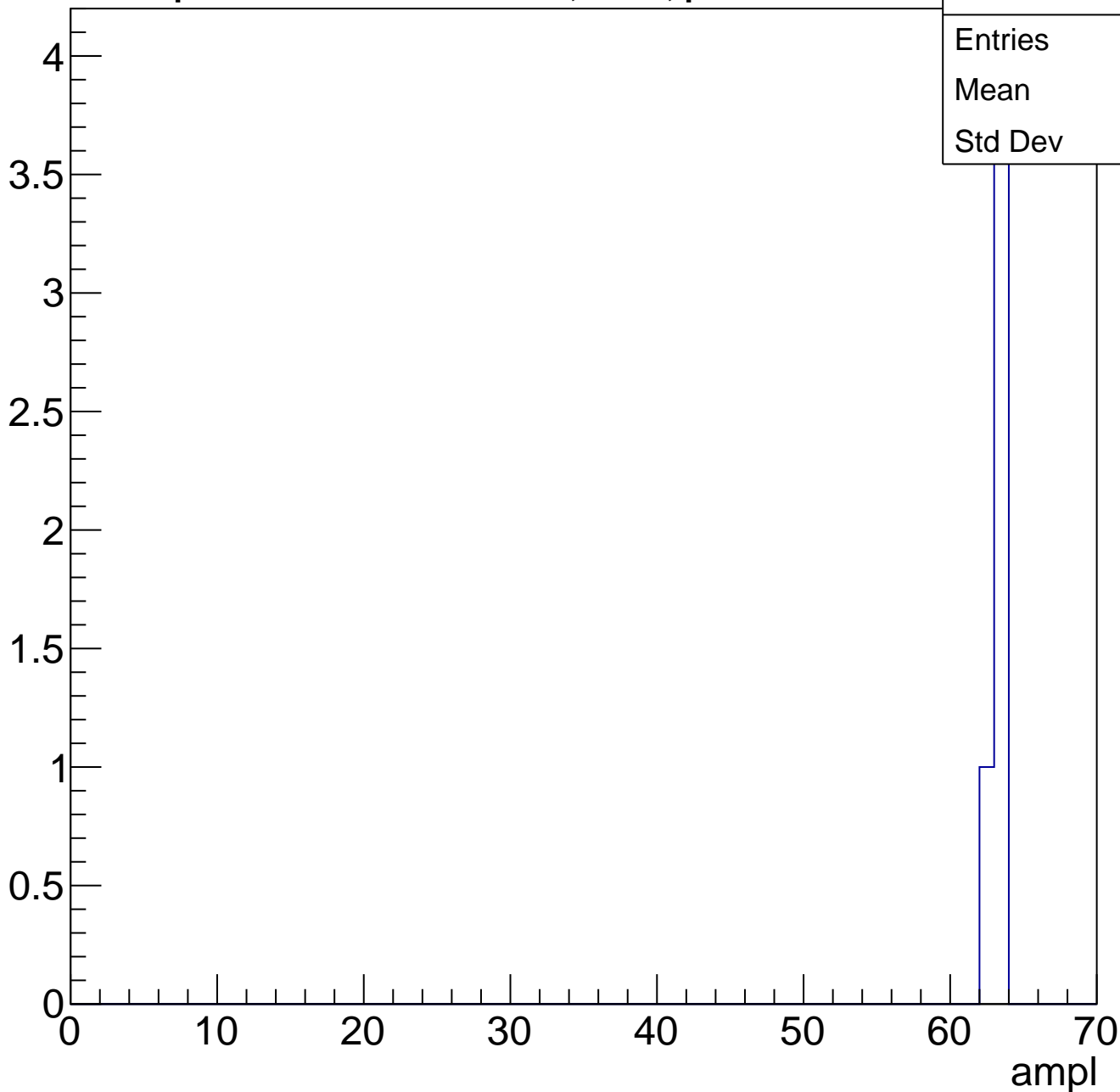
Entry



# B1L100S, U2-ch97, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry





# B1L100S, U2-ch97, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



# B1L100S, U2-ch98, adc0

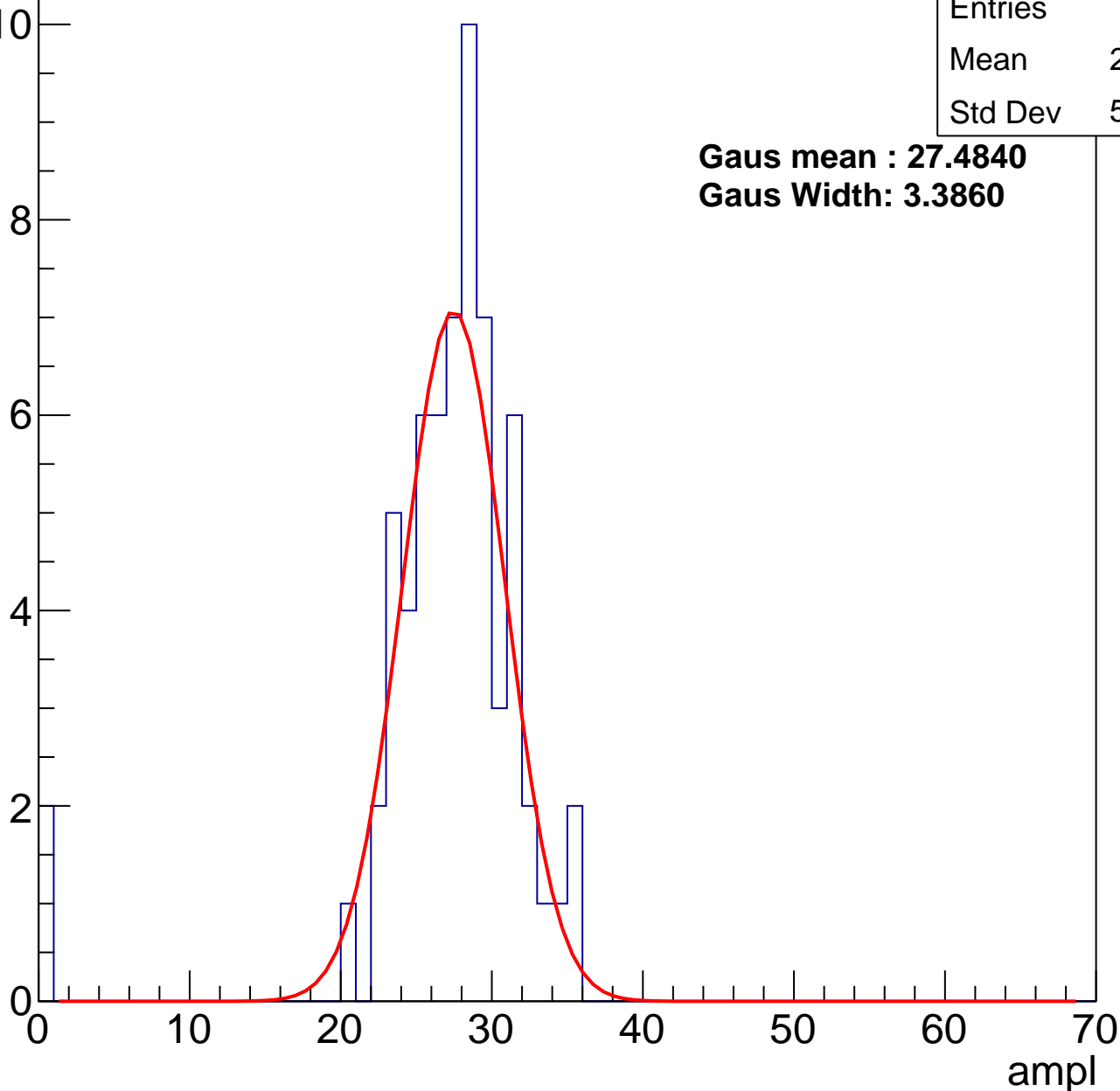
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	65
Mean	26.62
Std Dev	5.707

**Gaus mean : 27.4840**

**Gaus Width: 3.3860**



# B1L100S, U2-ch98, adc1

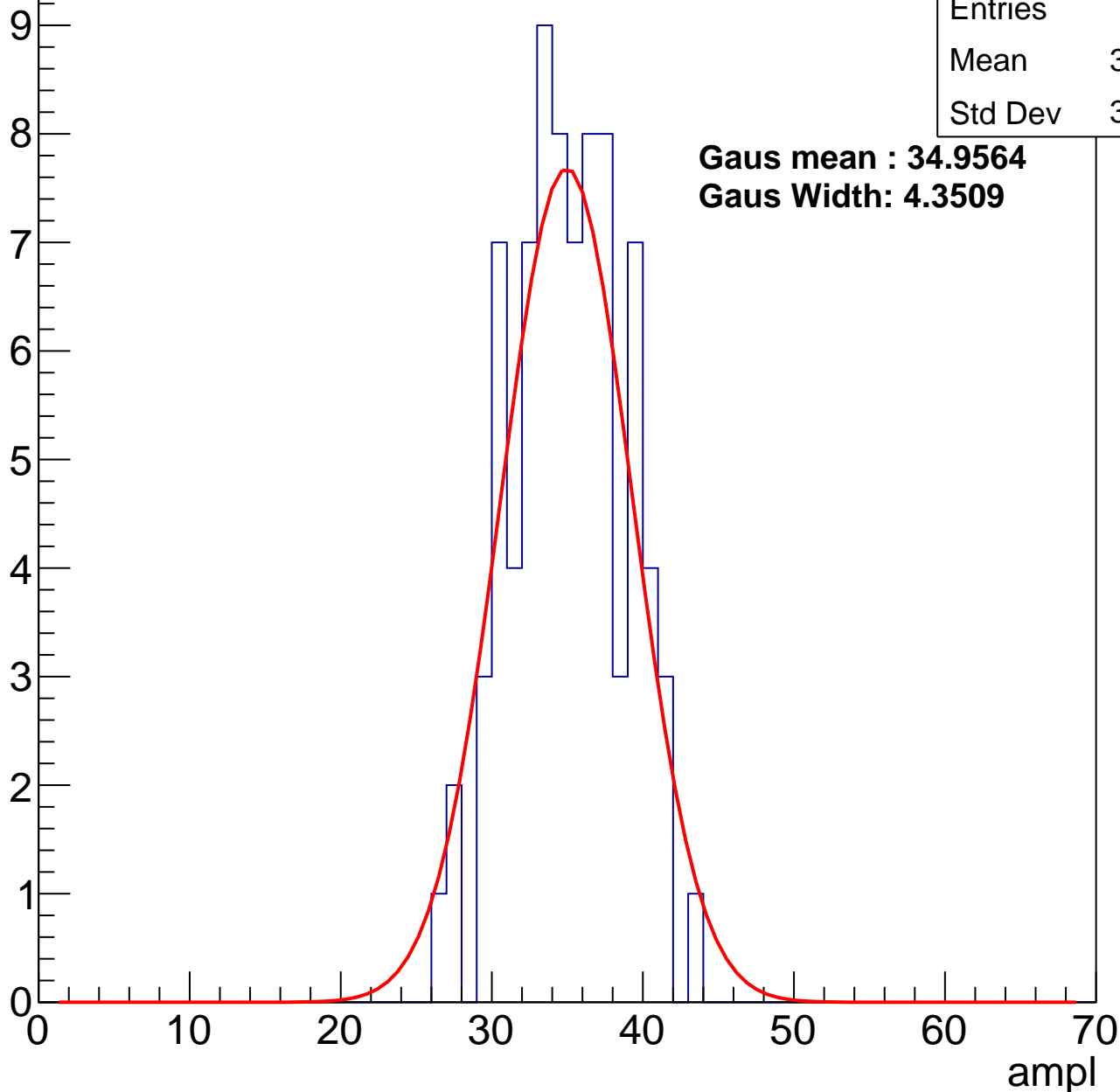
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	82
Mean	34.59
Std Dev	3.662

**Gaus mean : 34.9564**

**Gaus Width: 4.3509**



# B1L100S, U2-ch98, adc2

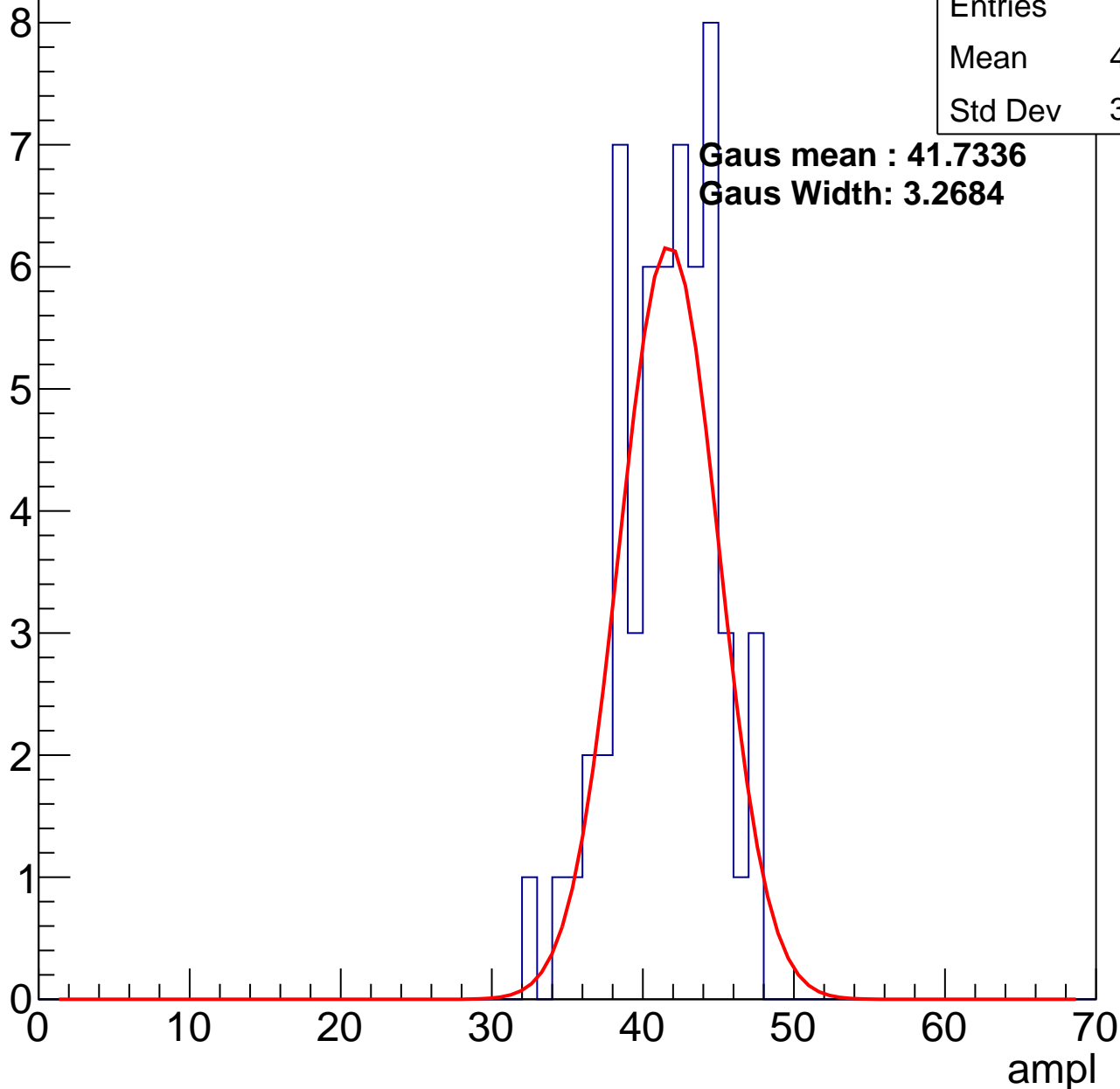
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	57
Mean	41.09
Std Dev	3.278

**Gaus mean : 41.7336**

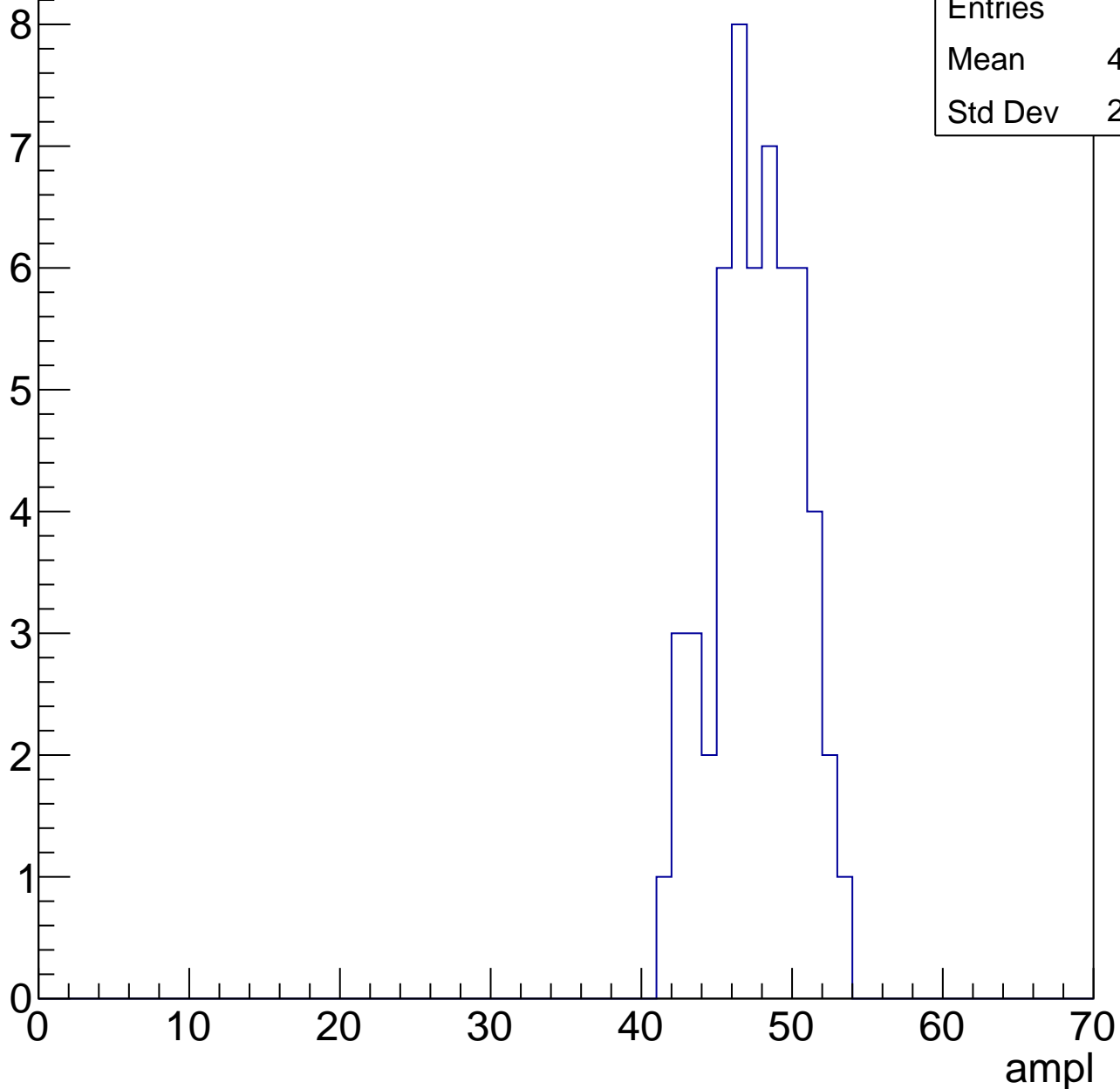
**Gaus Width: 3.2684**



# B1L100S, U2-ch98, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

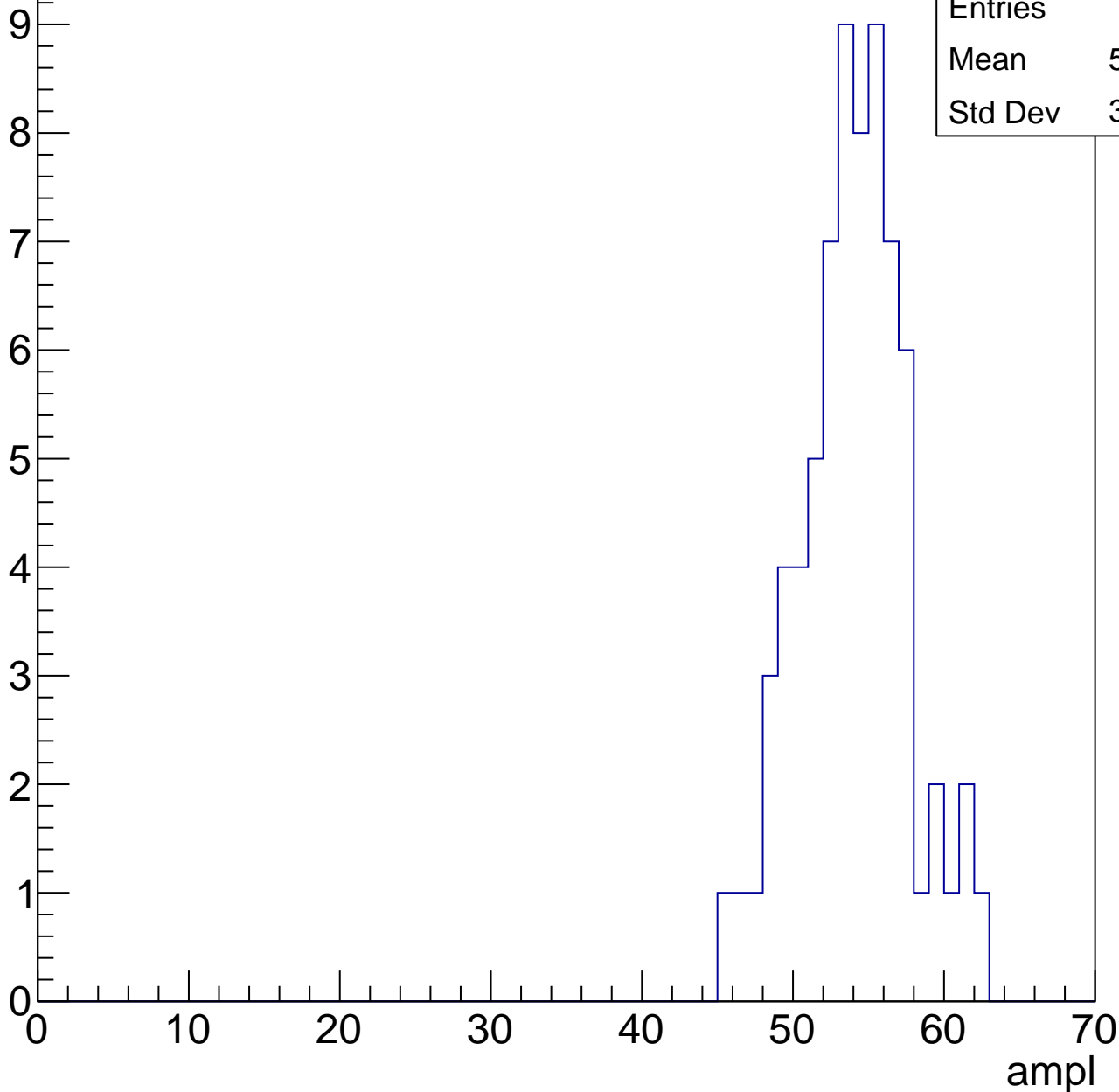


Entries	55
Mean	47.18
Std Dev	2.835

# B1L100S, U2-ch98, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

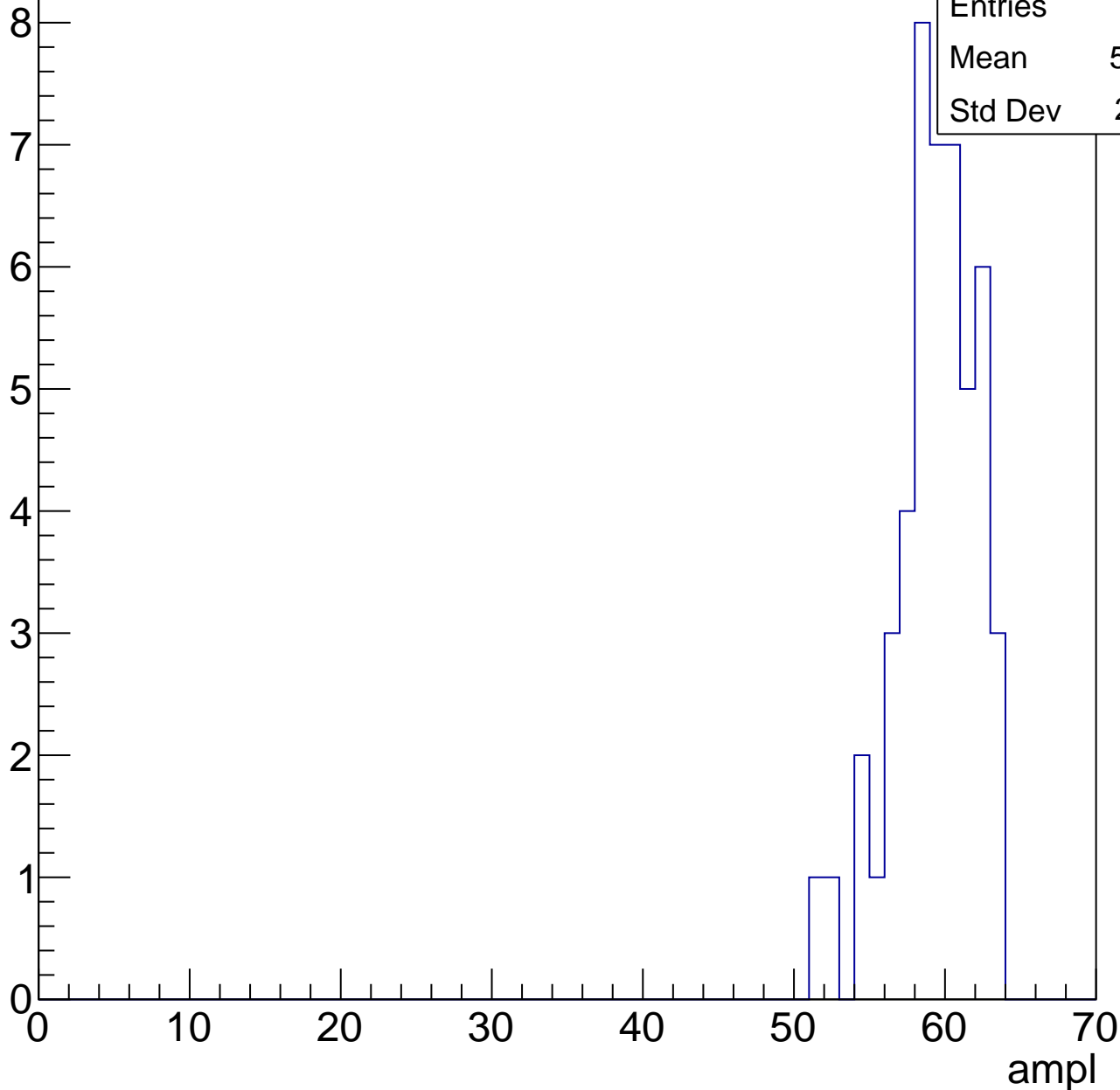
Entry



# B1L100S, U2-ch98, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

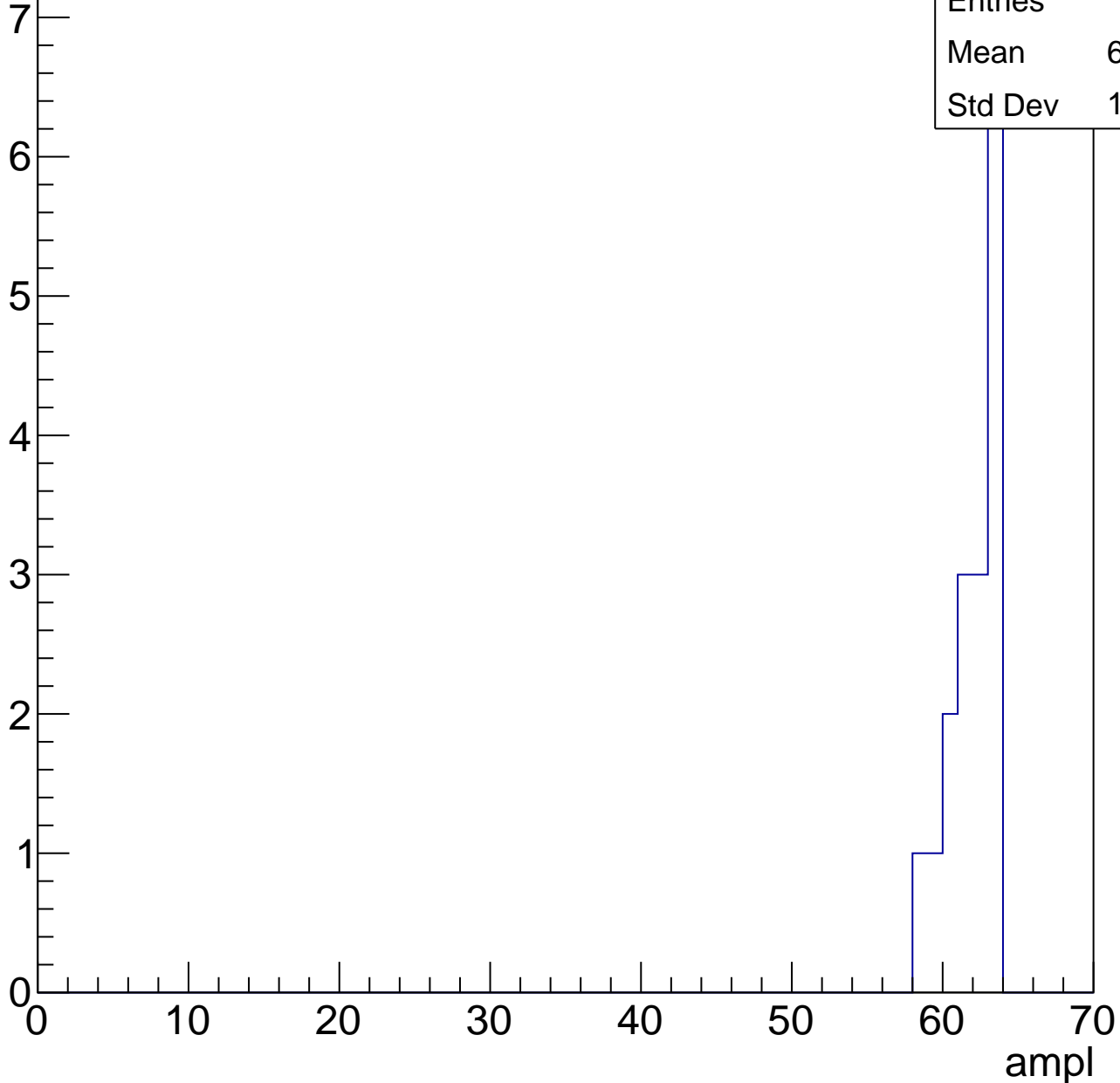


Entries	48
Mean	58.85
Std Dev	2.731

# B1L100S, U2-ch98, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry





# B1L100S, U2-ch98, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L100S, U2-ch99, adc0

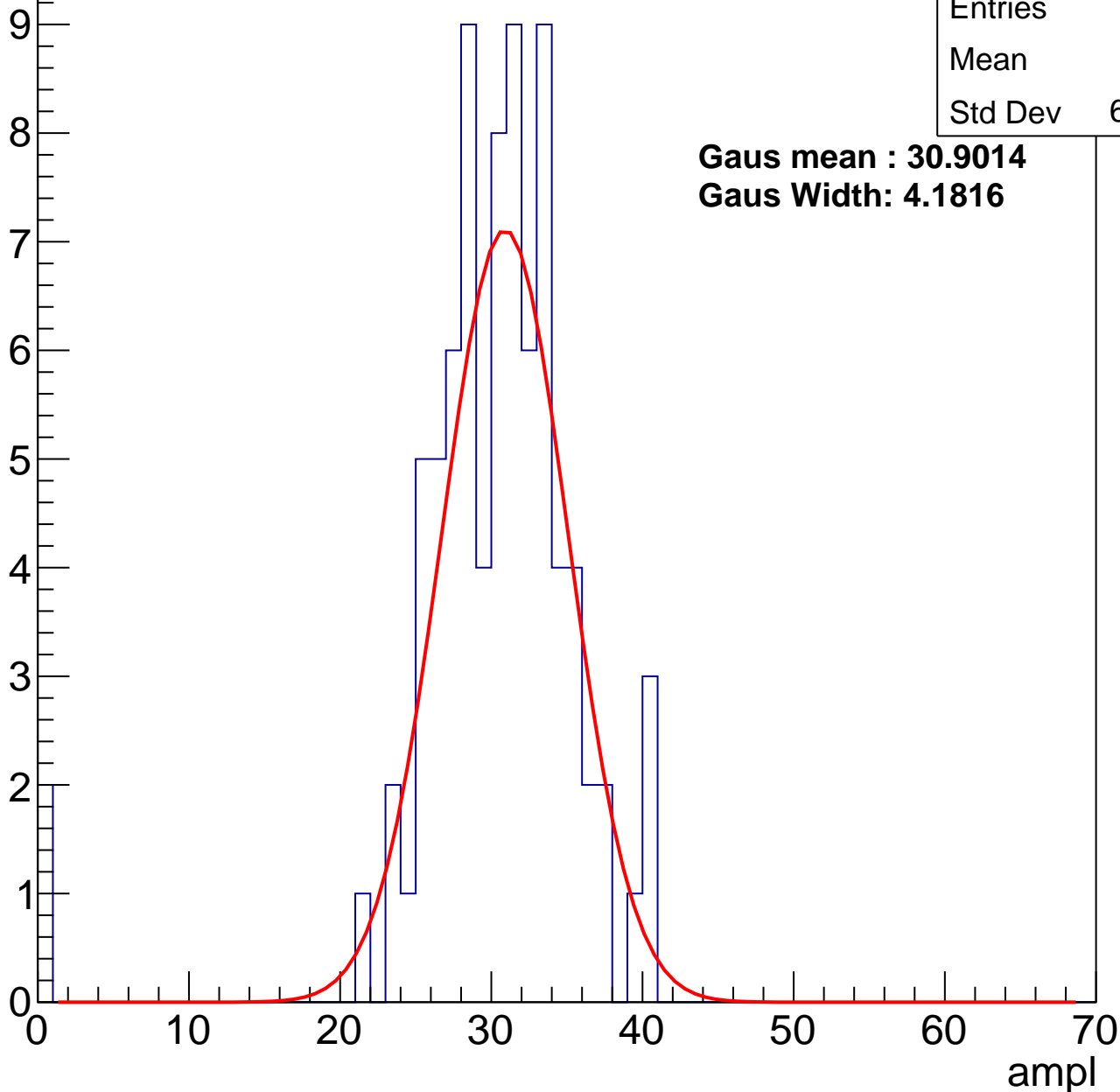
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	83
Mean	29.7
Std Dev	6.146

**Gaus mean : 30.9014**

**Gaus Width: 4.1816**



# B1L100S, U2-ch99, adc1

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	77
Mean	38.01
Std Dev	3.691

**Gaus mean : 39.0990**

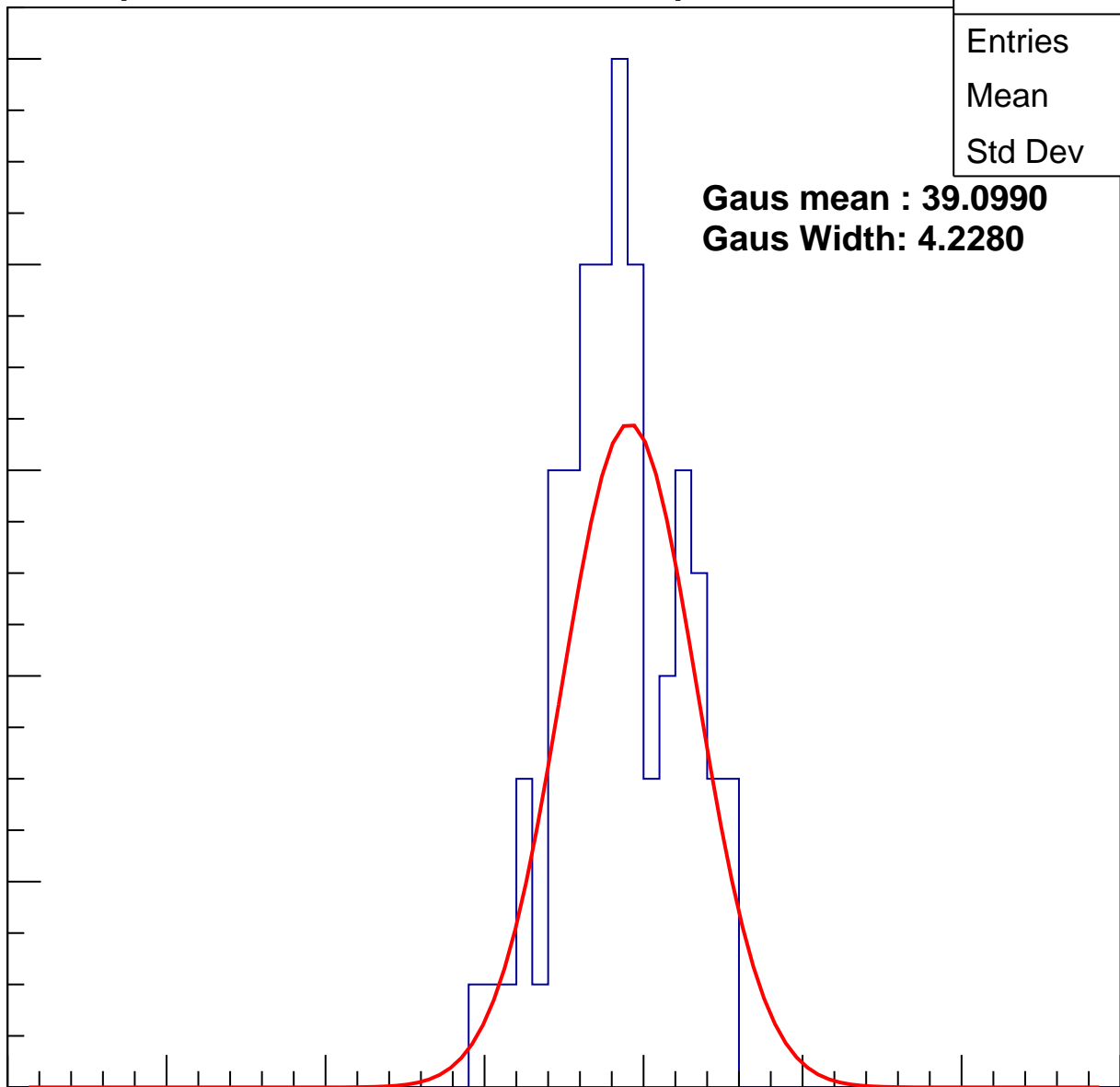
**Gaus Width: 4.2280**

Entry

10  
8  
6  
4  
2  
0

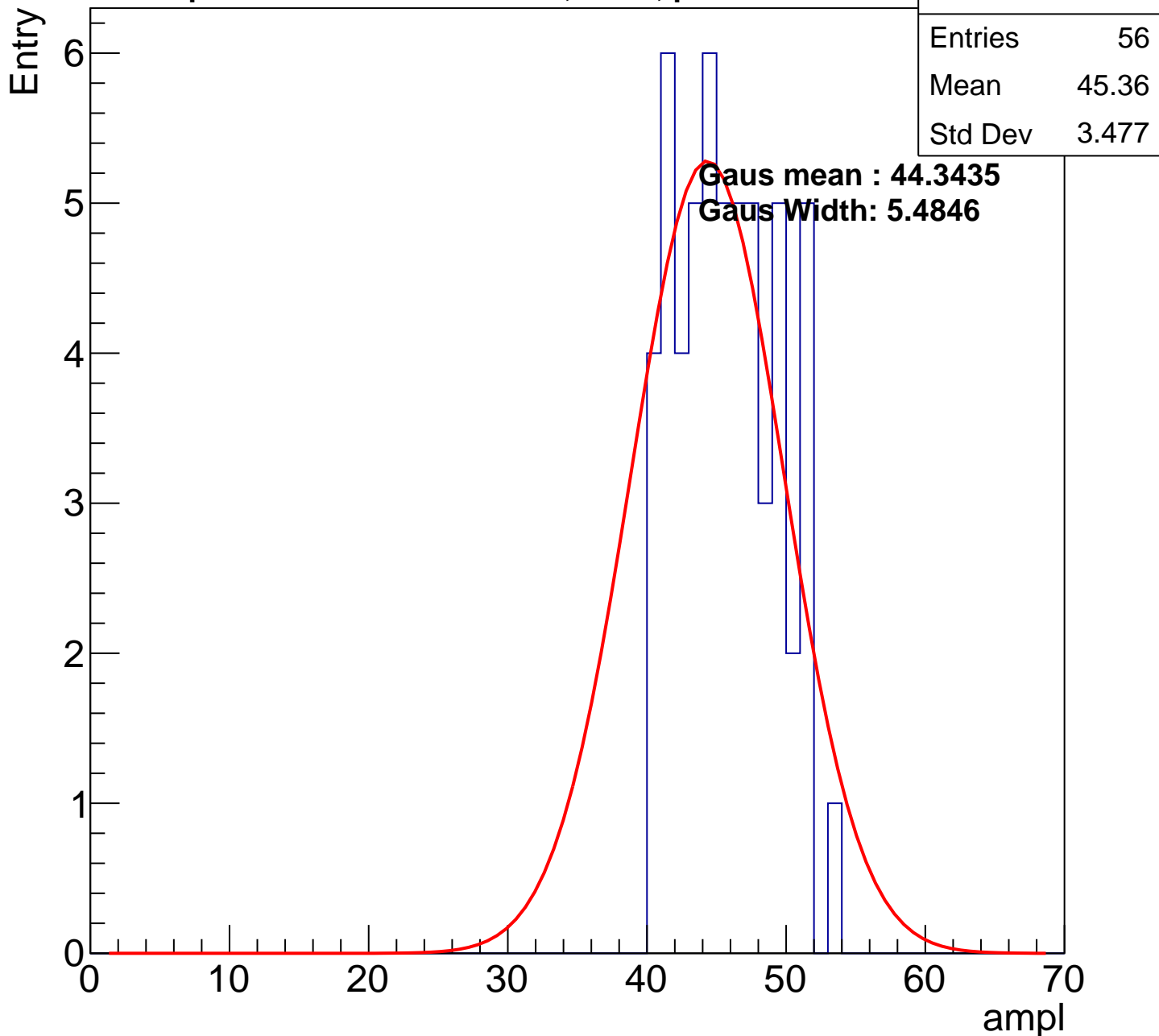
0 10 20 30 40 50 60 70

ampl



# B1L100S, U2-ch99, adc2

calib\_packv5\_042523\_0143.root, FC#4, port A2

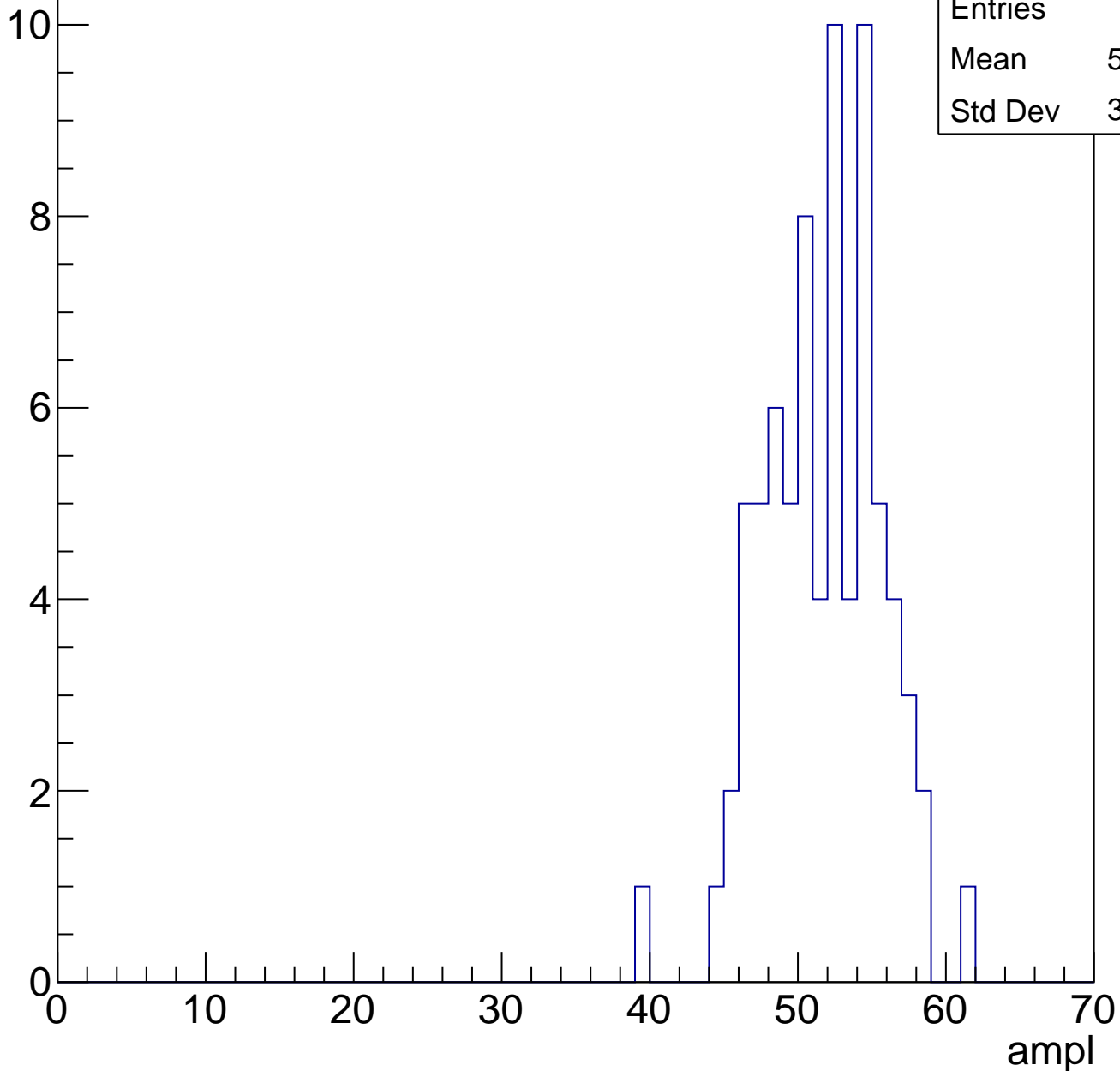


# B1L100S, U2-ch99, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	76
Mean	51.24
Std Dev	3.889

Entry

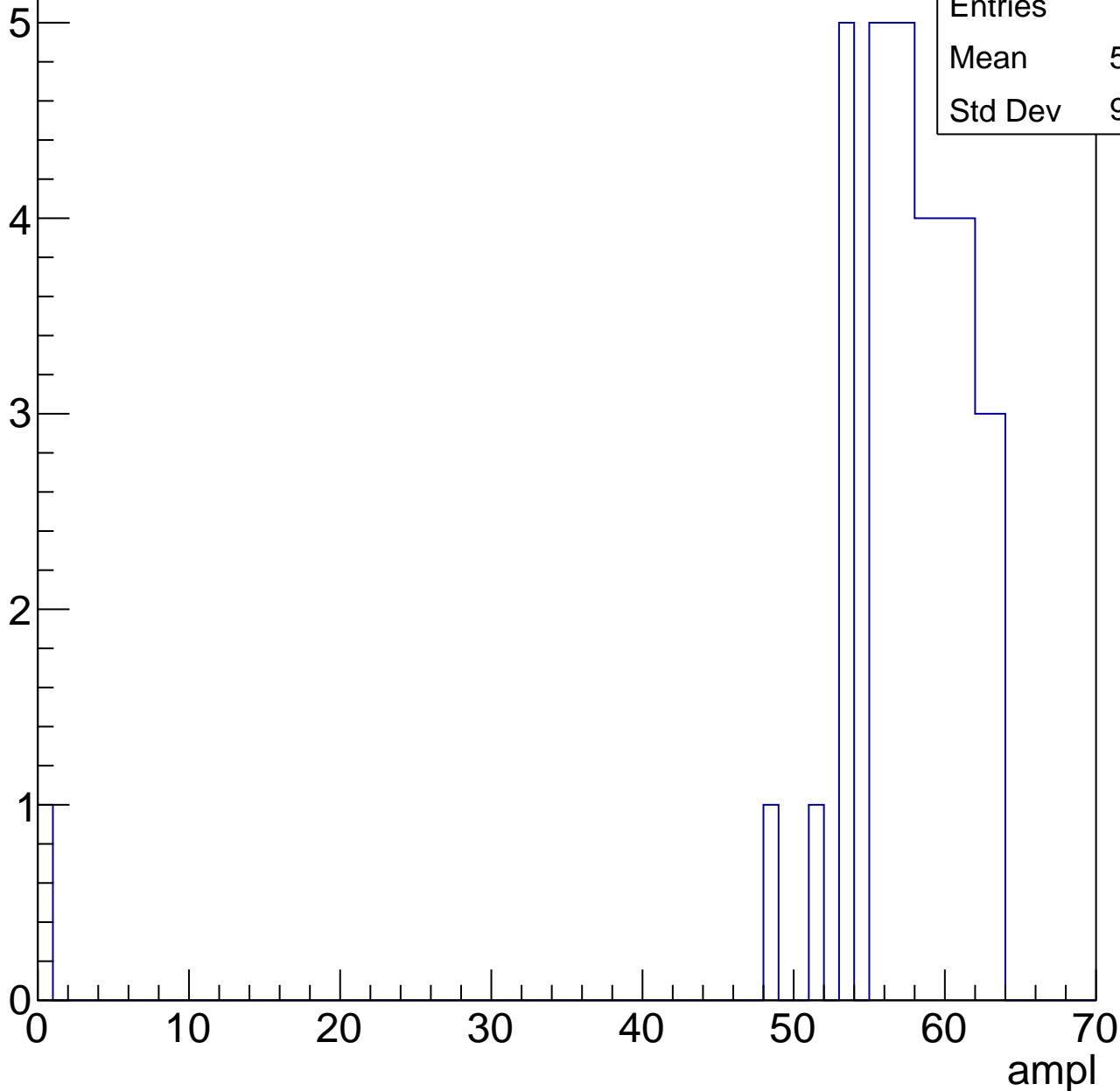


# B1L100S, U2-ch99, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	45
Mean	56.24
Std Dev	9.127

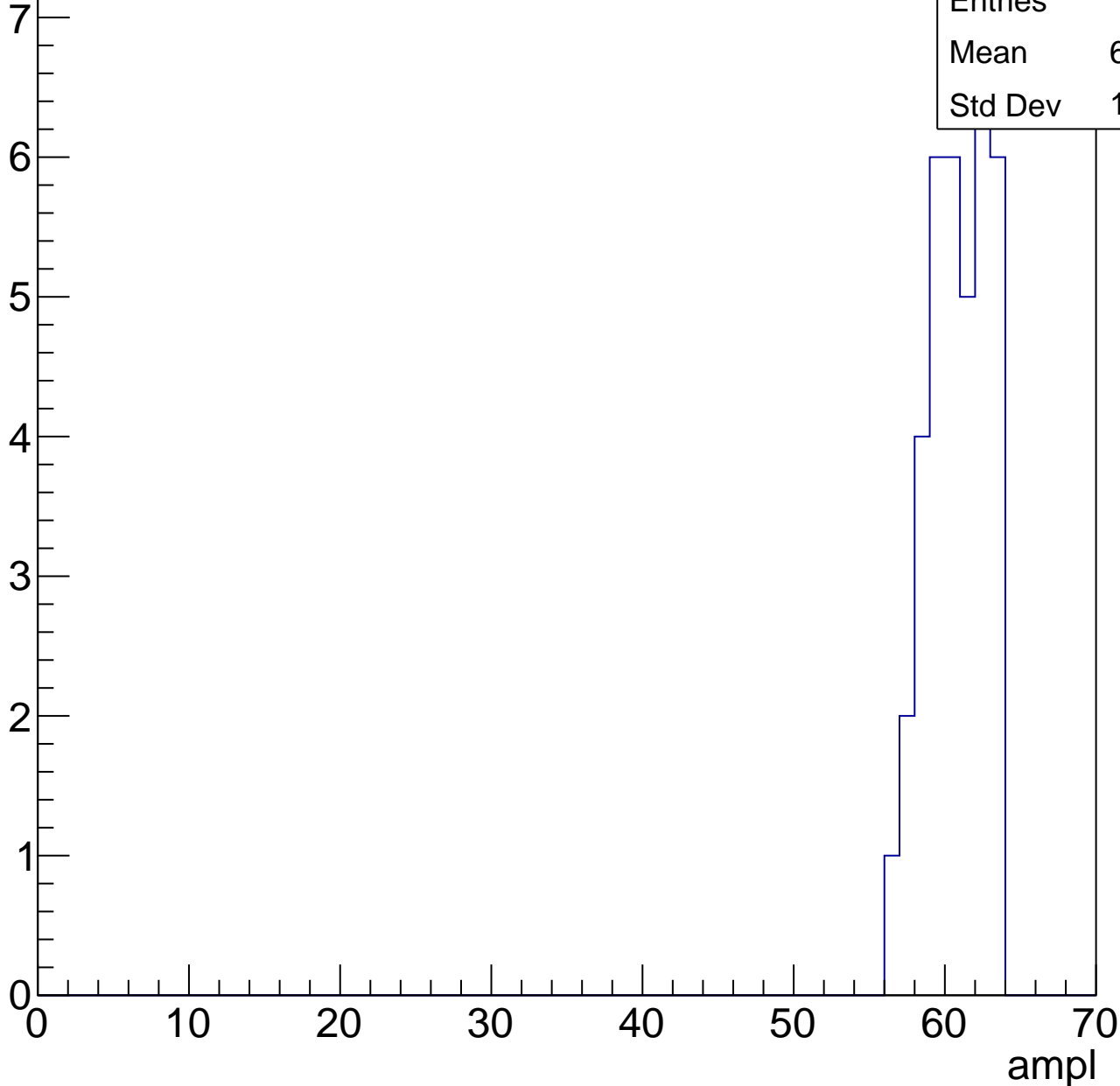


# B1L100S, U2-ch99, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	37
Mean	60.35
Std Dev	1.934



# B1L100S, U2-ch99, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry





# B1L100S, U2-ch99, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



# B1L100S, U2-ch100, adc0

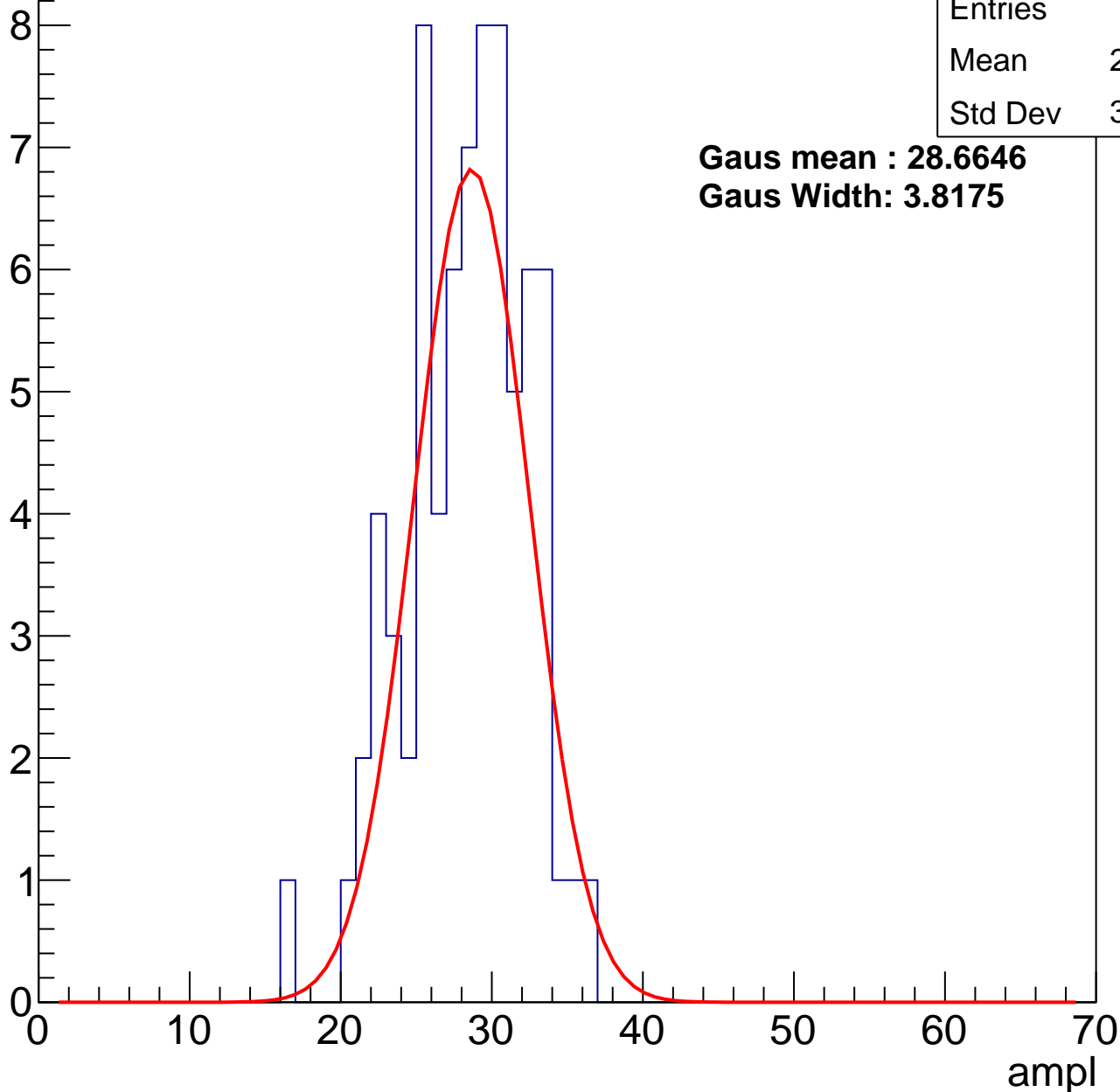
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	74
Mean	27.93
Std Dev	3.909

**Gaus mean : 28.6646**

**Gaus Width: 3.8175**



# B1L100S, U2-ch100, adc1

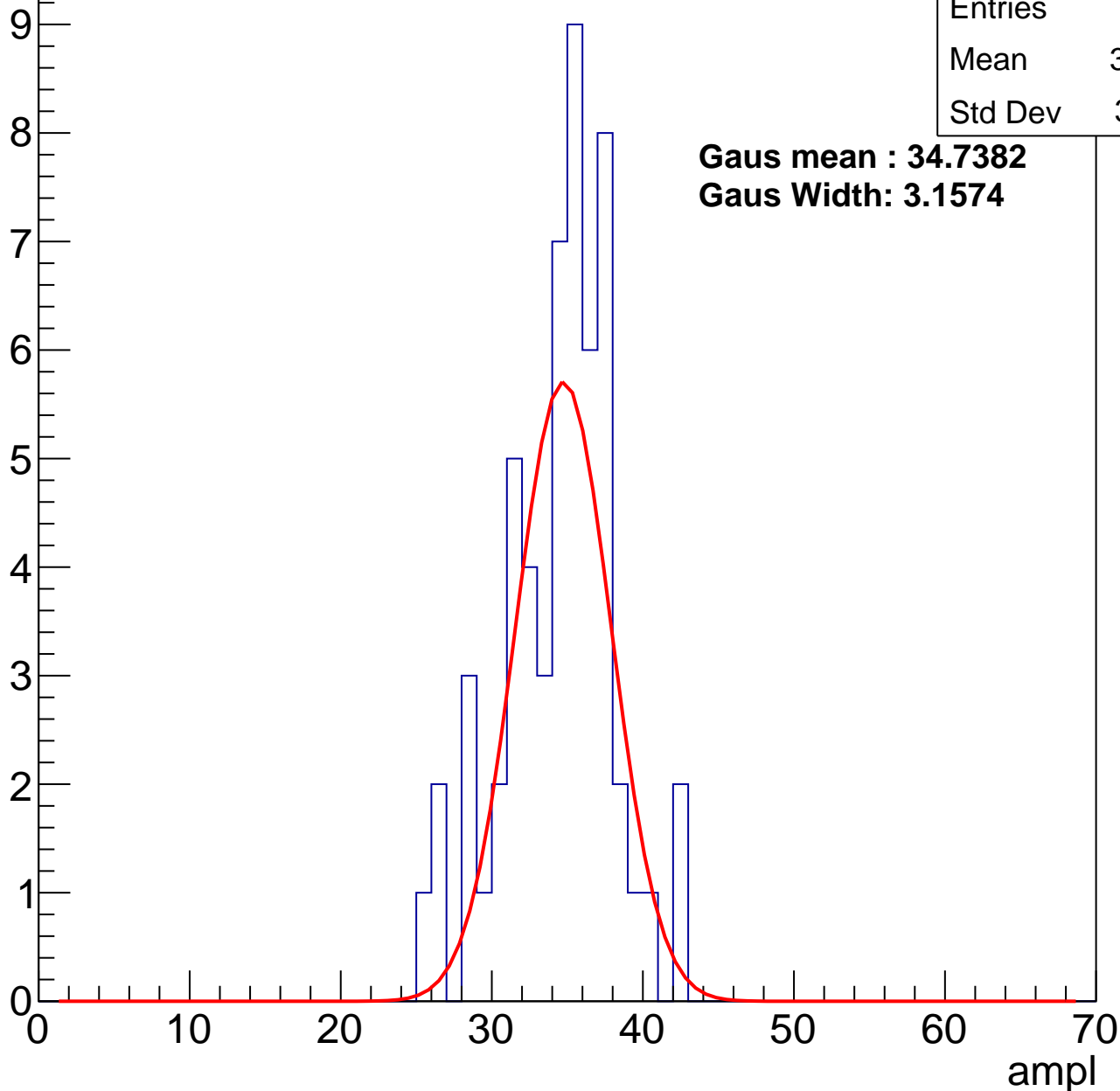
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	57
Mean	33.96
Std Dev	3.661

**Gaus mean : 34.7382**

**Gaus Width: 3.1574**



# B1L100S, U2-ch100, adc2

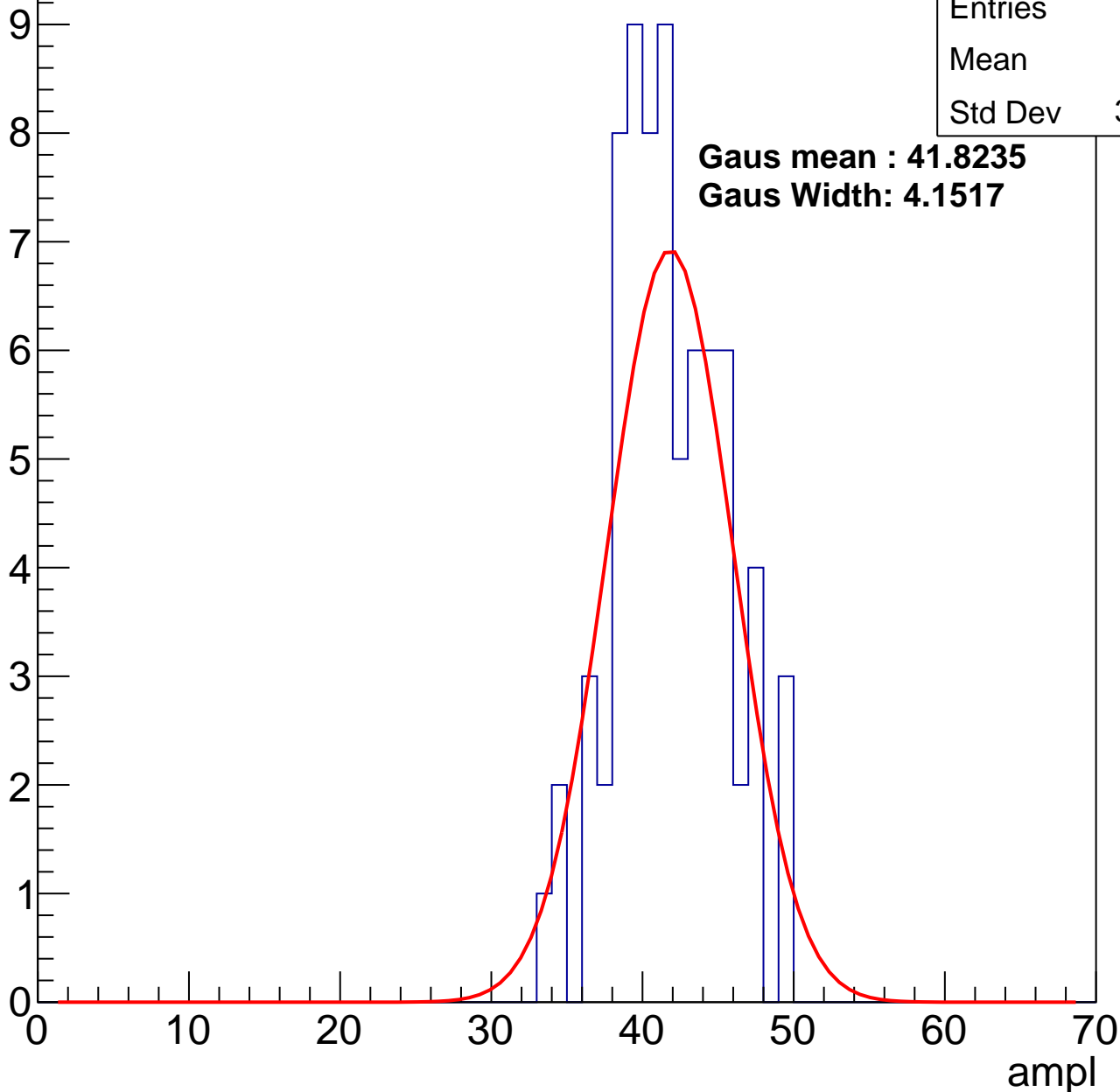
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	74
Mean	41.3
Std Dev	3.571

**Gaus mean : 41.8235**

**Gaus Width: 4.1517**

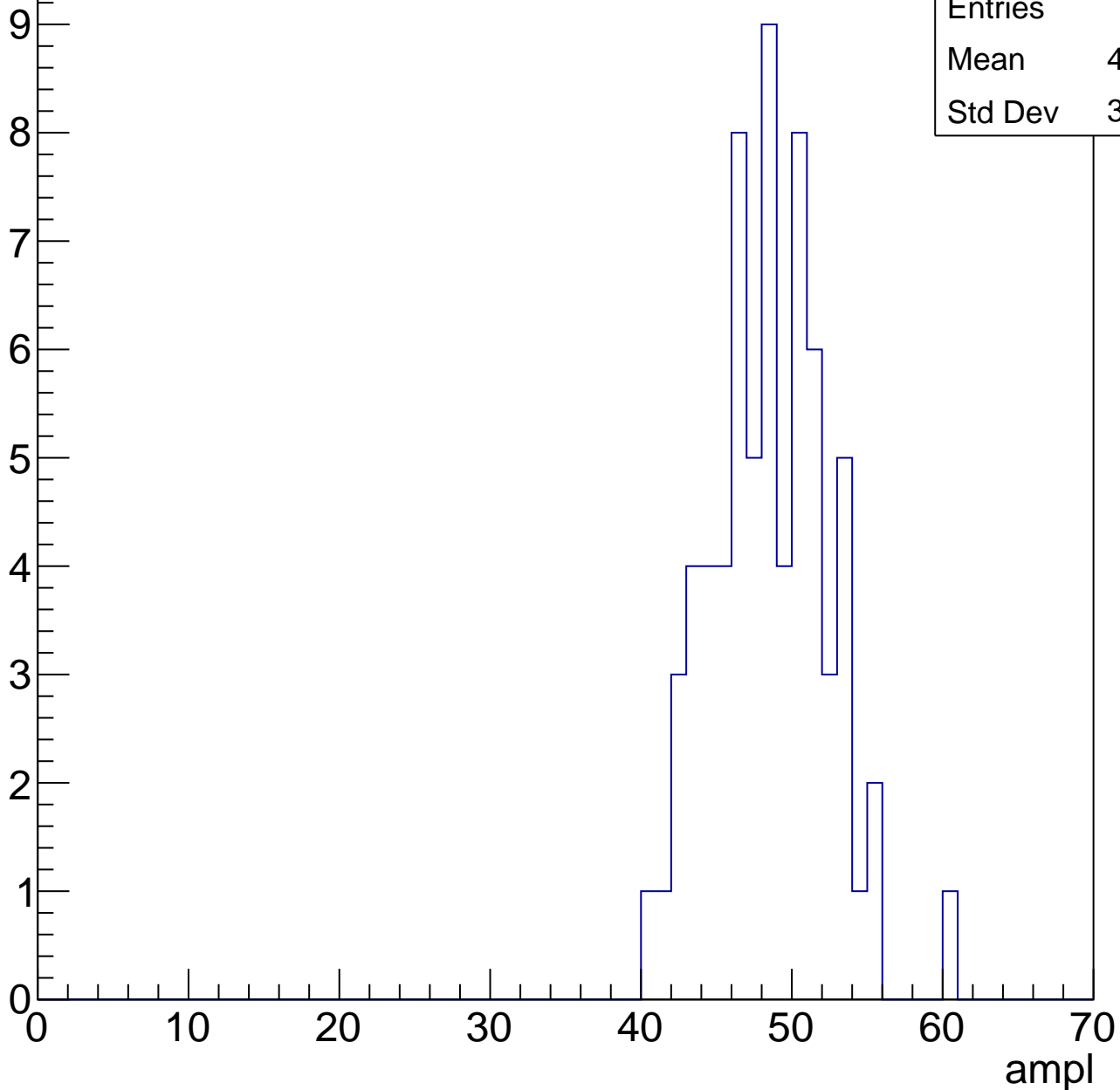


# B1L100S, U2-ch100, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	69
Mean	48.07
Std Dev	3.804

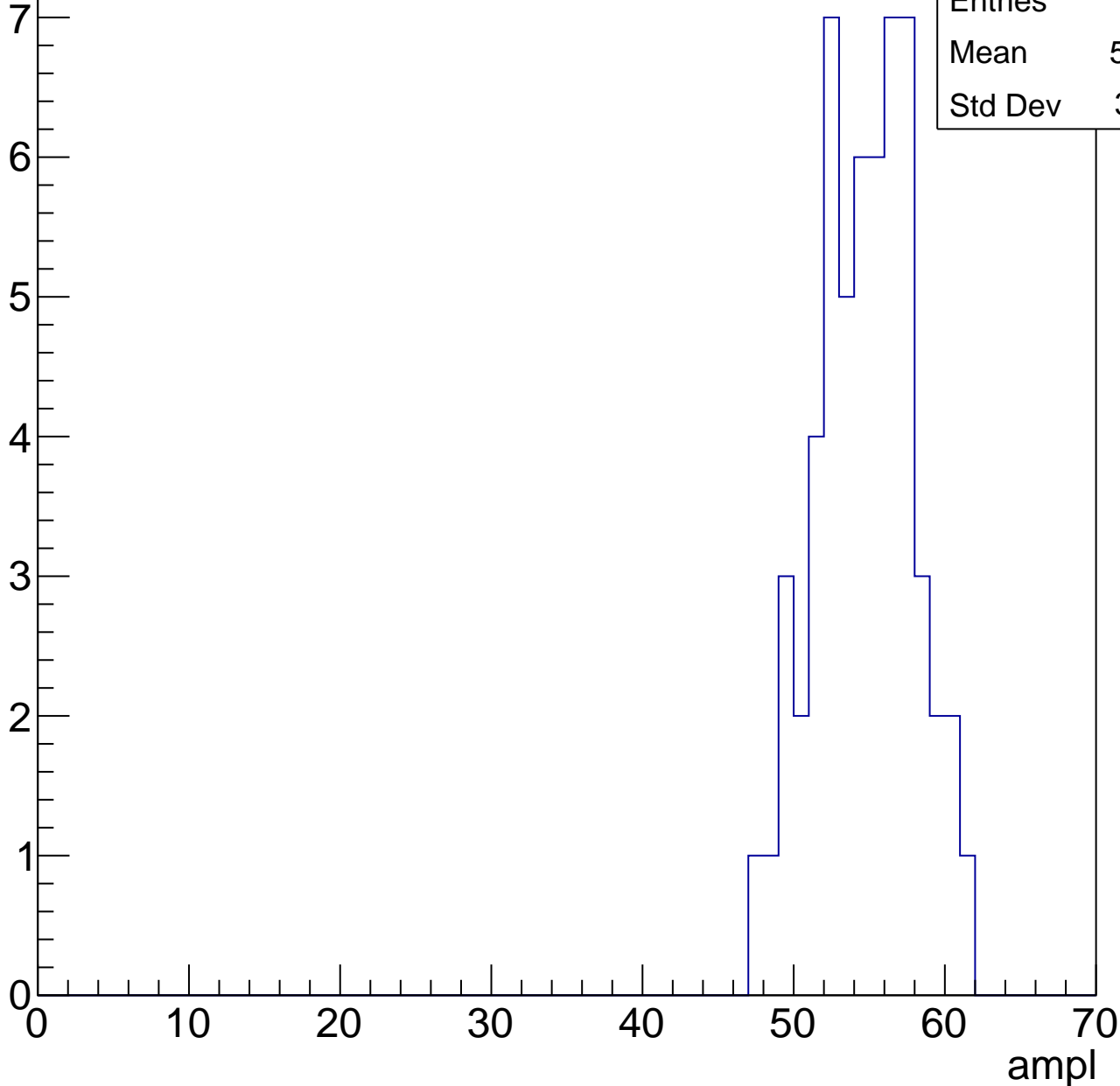


# B1L100S, U2-ch100, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	57
Mean	54.26
Std Dev	3.171

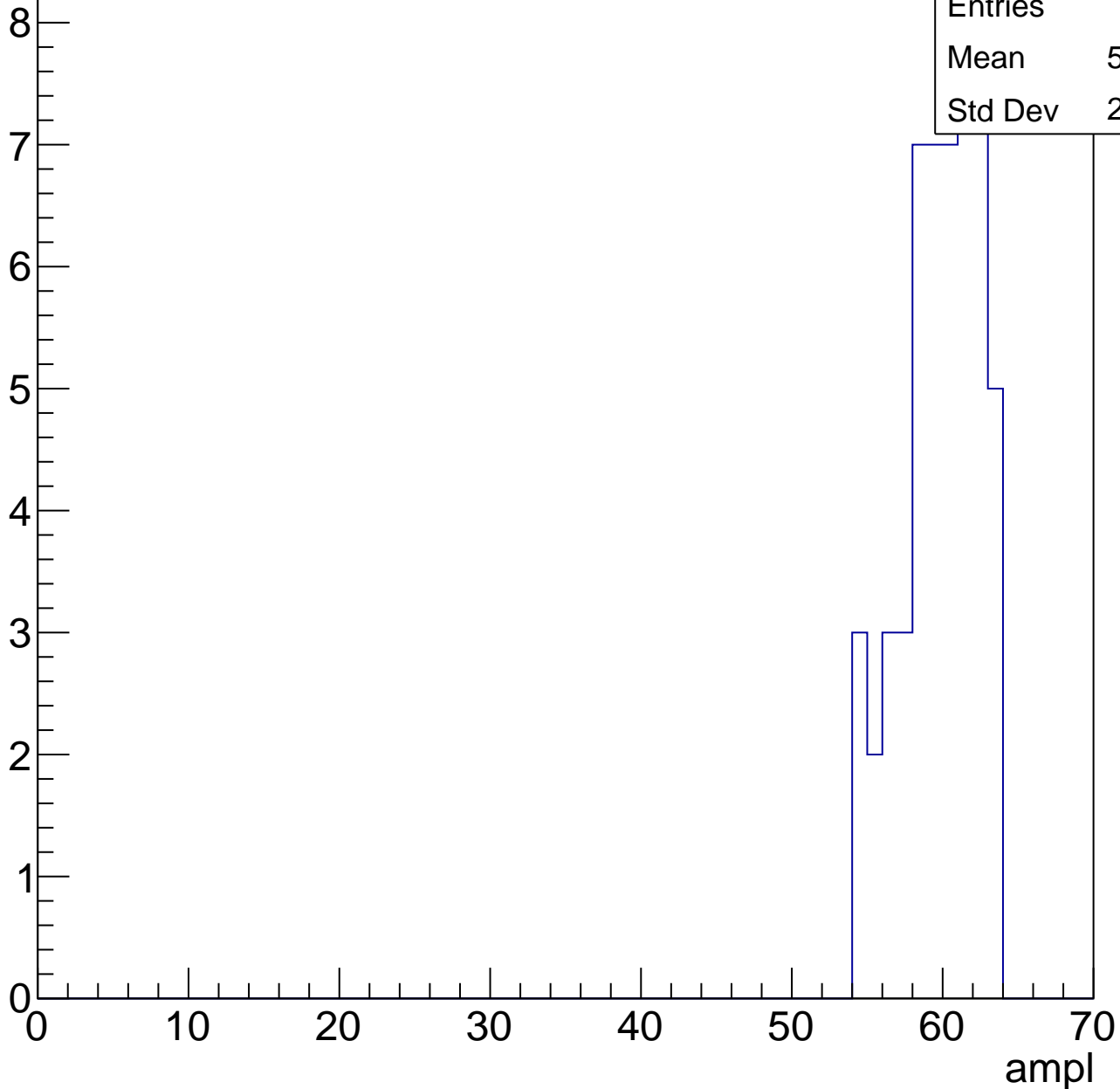


# B1L100S, U2-ch100, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

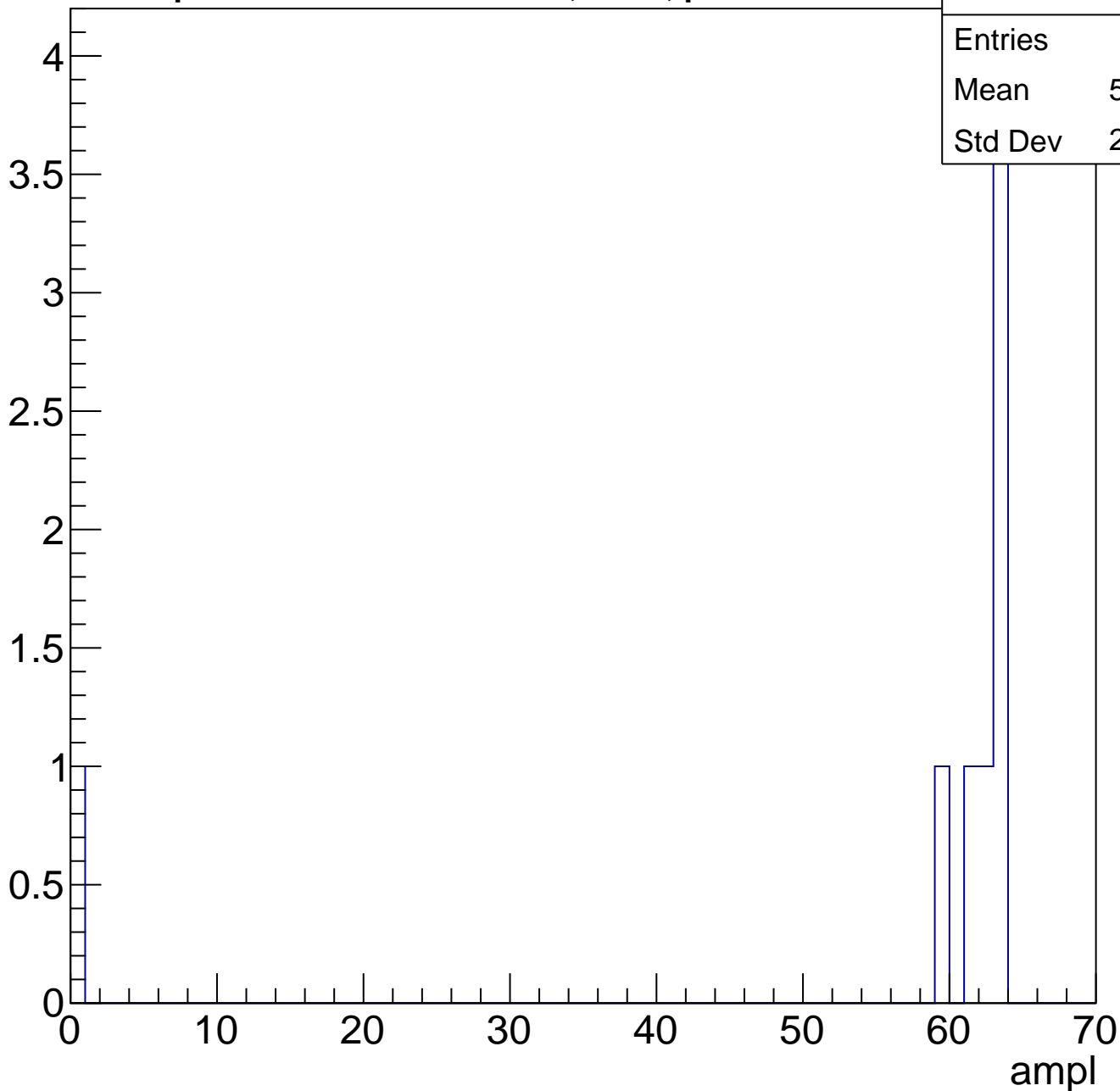
Entries	53
Mean	59.42
Std Dev	2.514



# B1L100S, U2-ch100, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

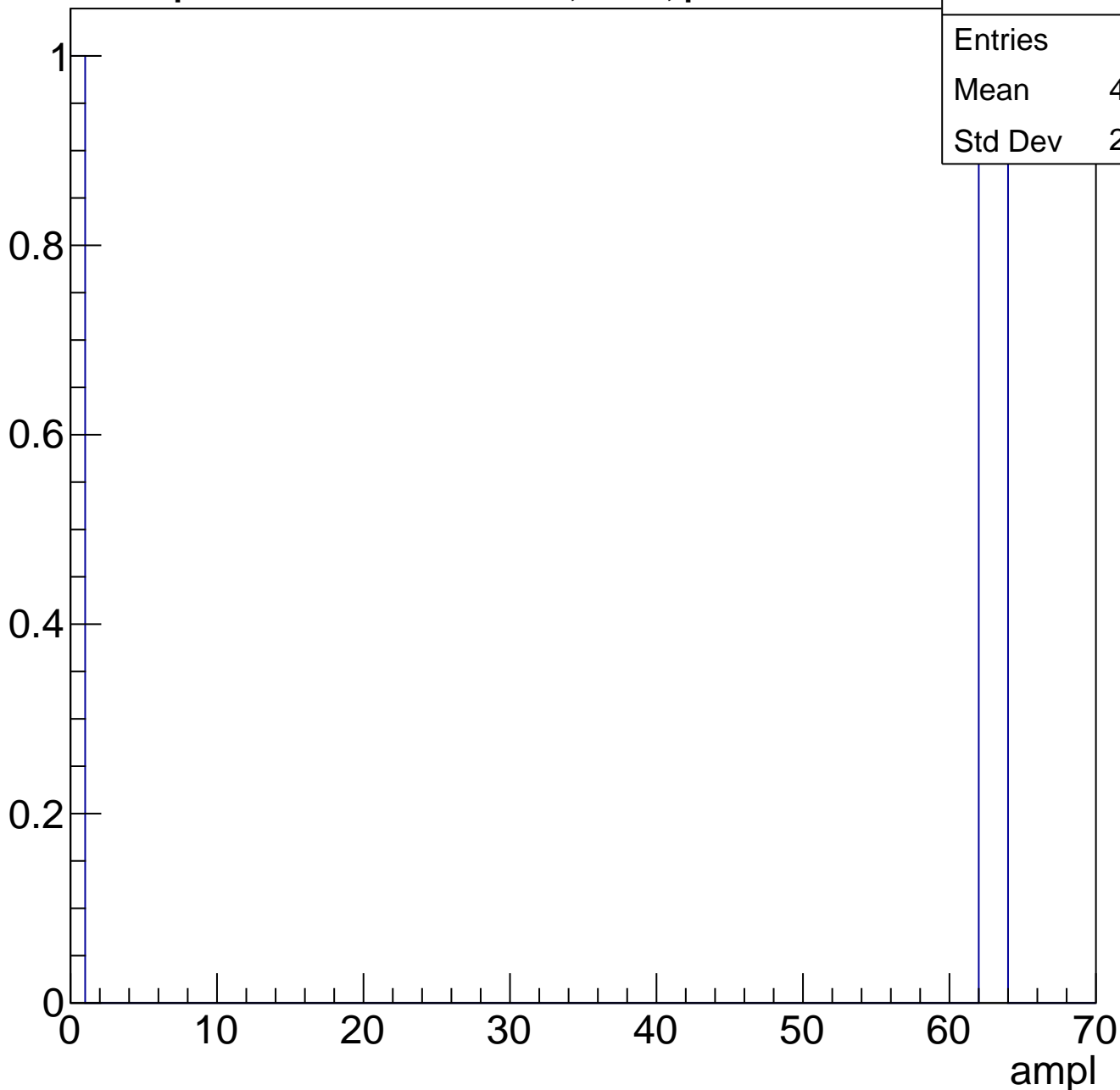




# B1L100S, U2-ch100, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



# B1L100S, U2-ch101, adc0

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	81
Mean	29.57
Std Dev	3.489

**Gaus mean : 29.8166**

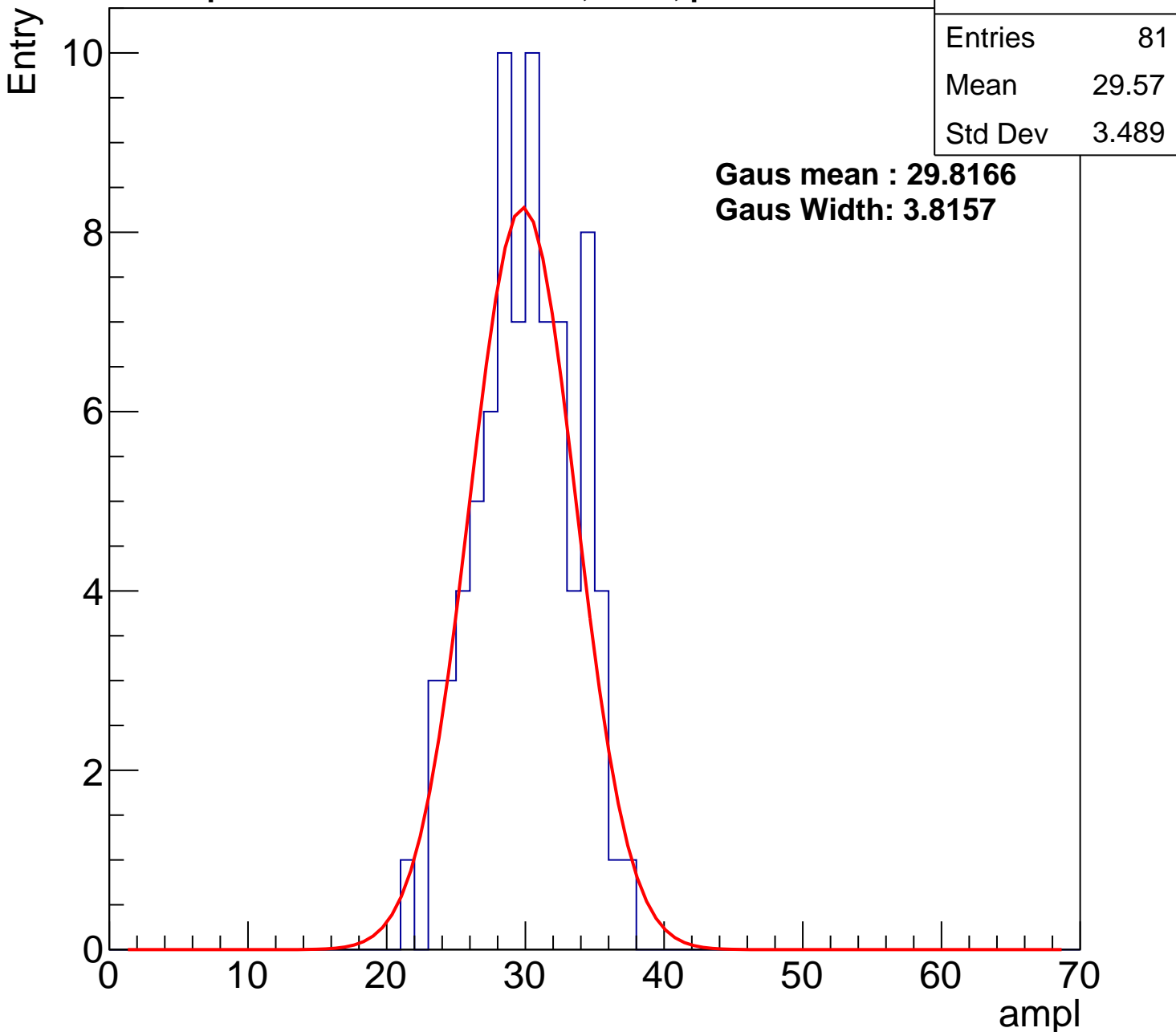
**Gaus Width: 3.8157**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L100S, U2-ch101, adc1

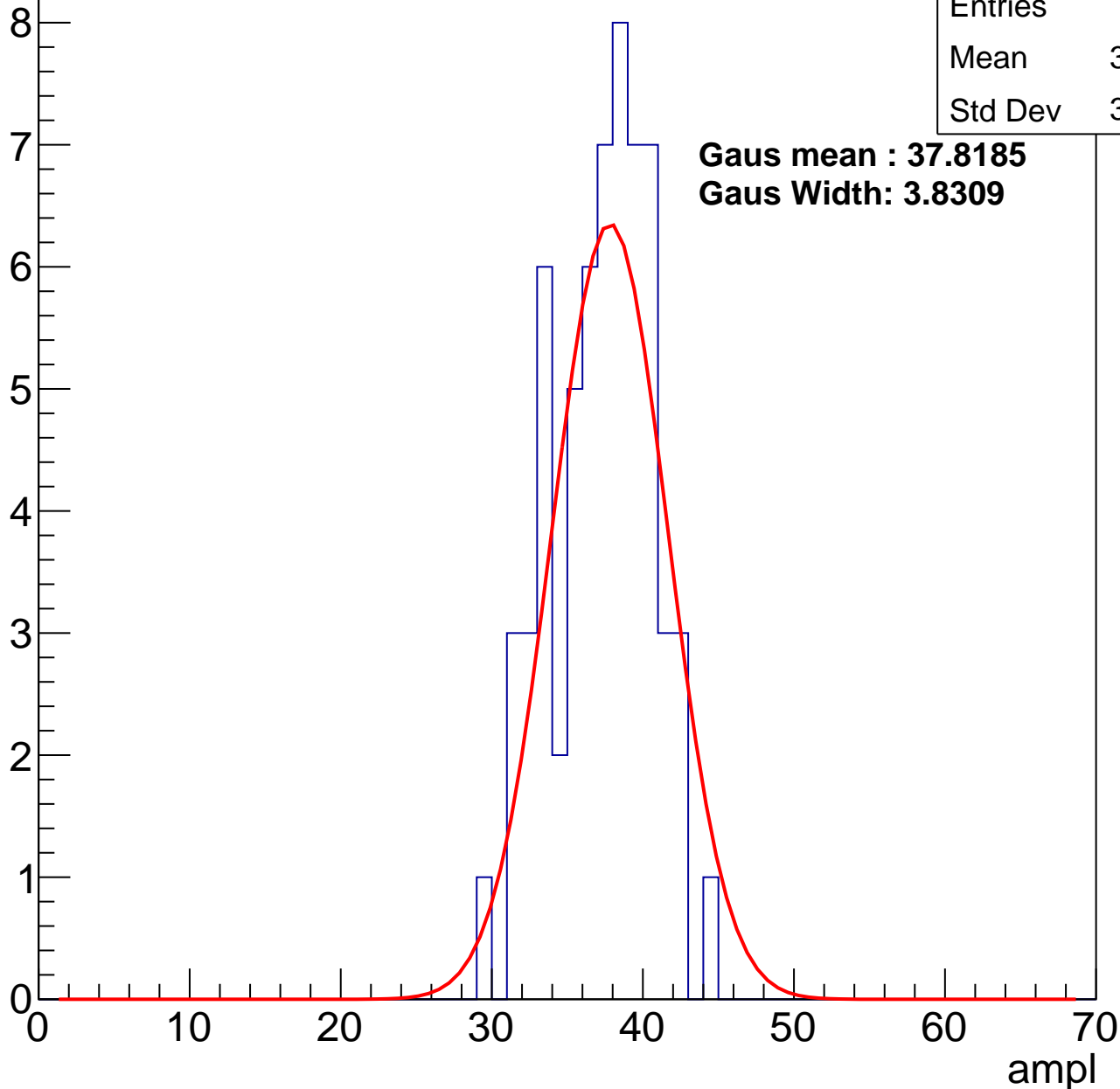
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	62
Mean	36.84
Std Dev	3.254

**Gaus mean : 37.8185**

**Gaus Width: 3.8309**



# B1L100S, U2-ch101, adc2

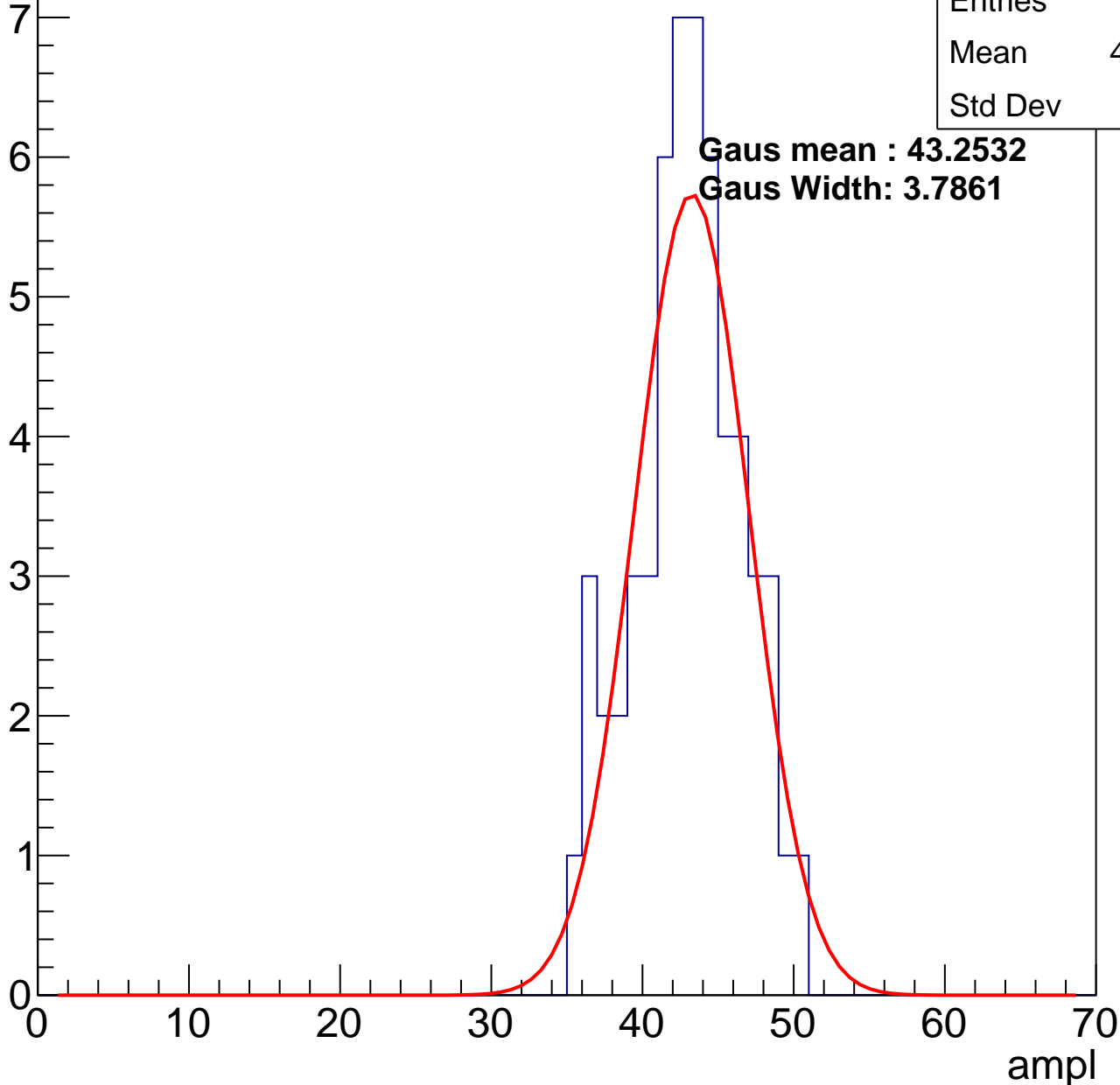
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	56
Mean	42.55
Std Dev	3.52

**Gaus mean : 43.2532**

**Gaus Width: 3.7861**

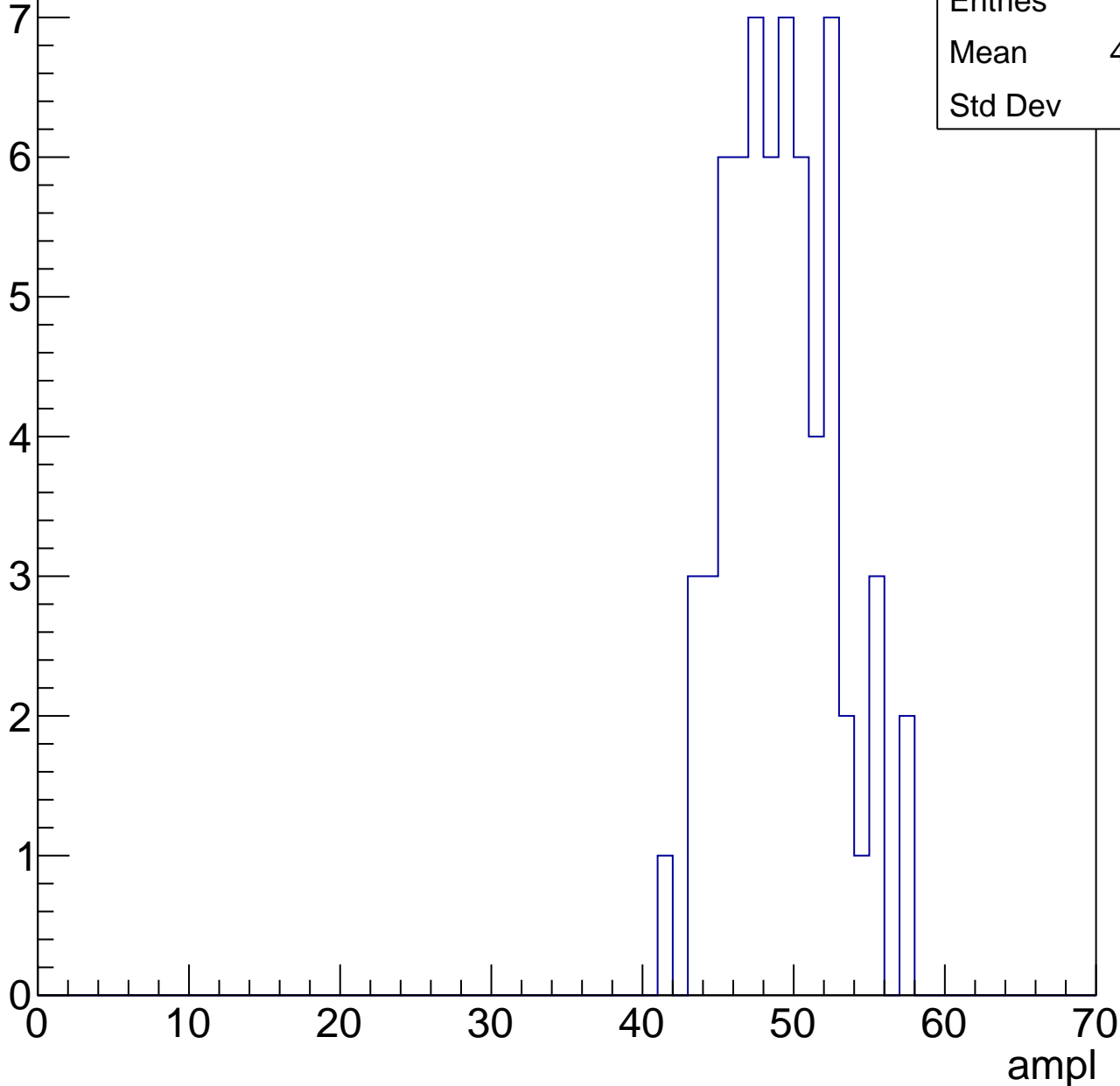


# B1L100S, U2-ch101, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	64
Mean	48.67
Std Dev	3.54

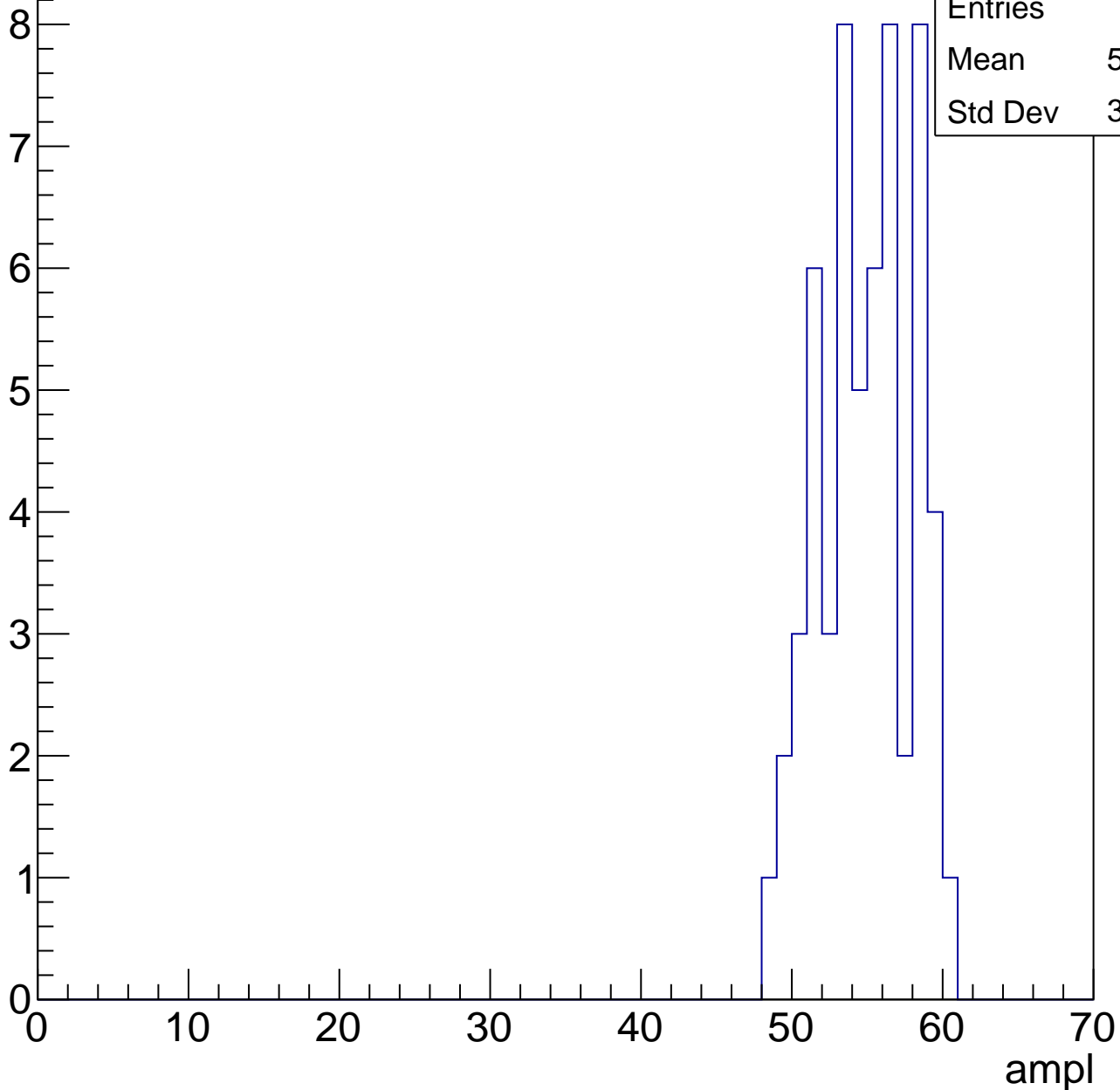


# B1L100S, U2-ch101, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	57
Mean	54.46
Std Dev	3.009

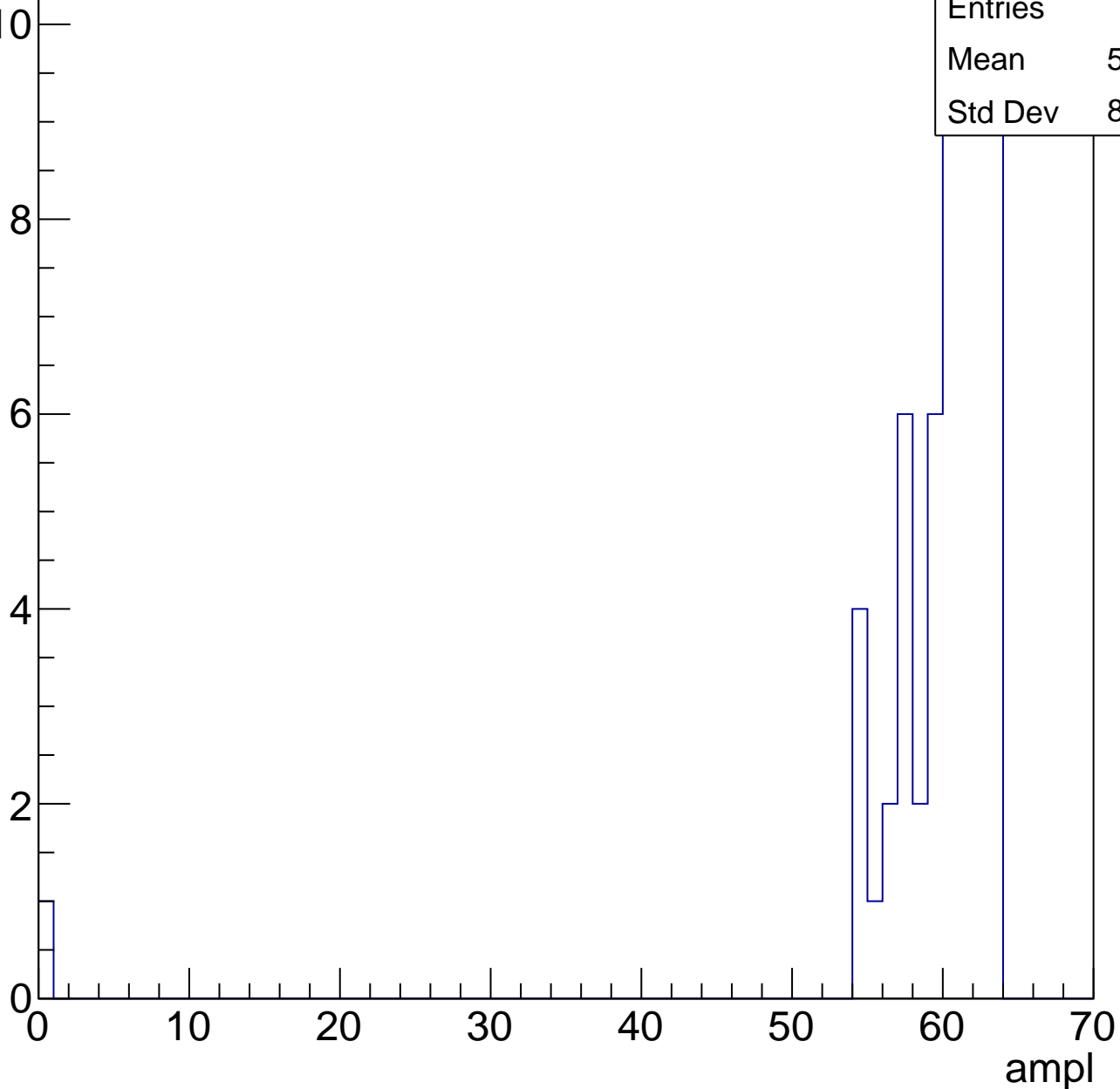


# B1L100S, U2-ch101, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	60
Mean	58.87
Std Dev	8.086



# B1L100S, U2-ch101, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry





# B1L100S, U2-ch101, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L100S, U2-ch102, adc0

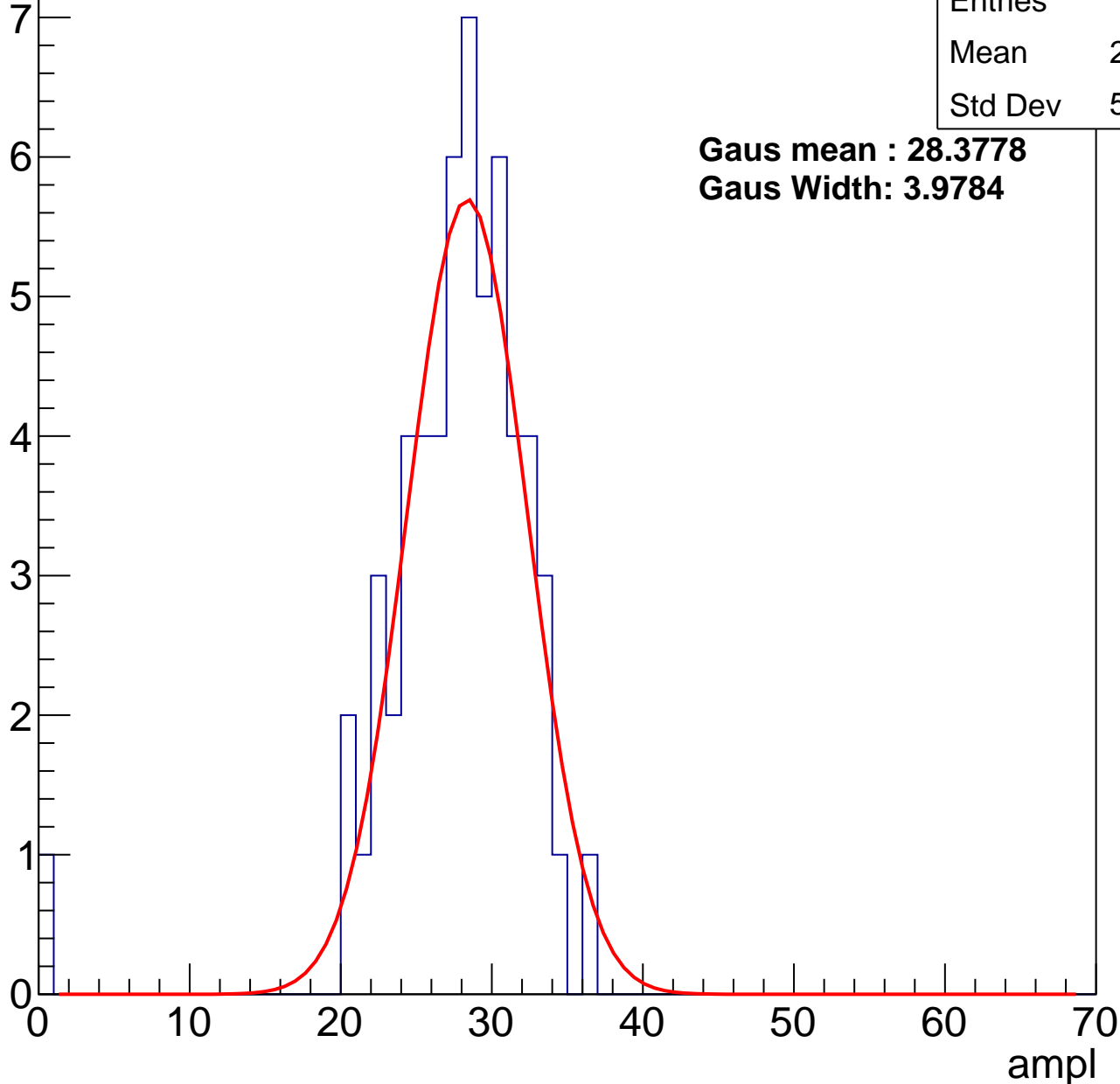
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	58
Mean	27.19
Std Dev	5.097

**Gaus mean : 28.3778**

**Gaus Width: 3.9784**



# B1L100S, U2-ch102, adc1

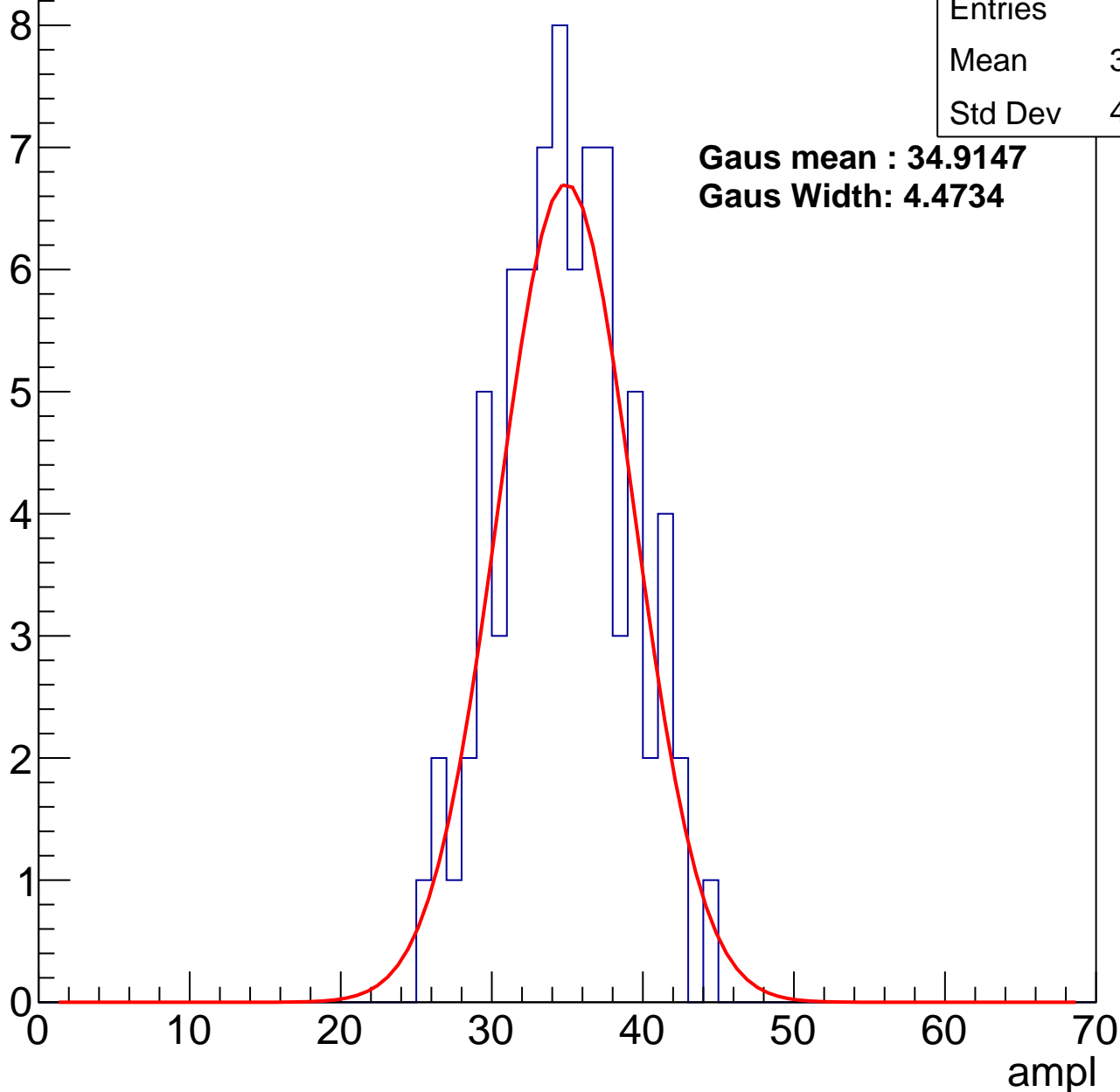
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	78
Mean	34.33
Std Dev	4.153

**Gaus mean : 34.9147**

**Gaus Width: 4.4734**



# B1L100S, U2-ch102, adc2

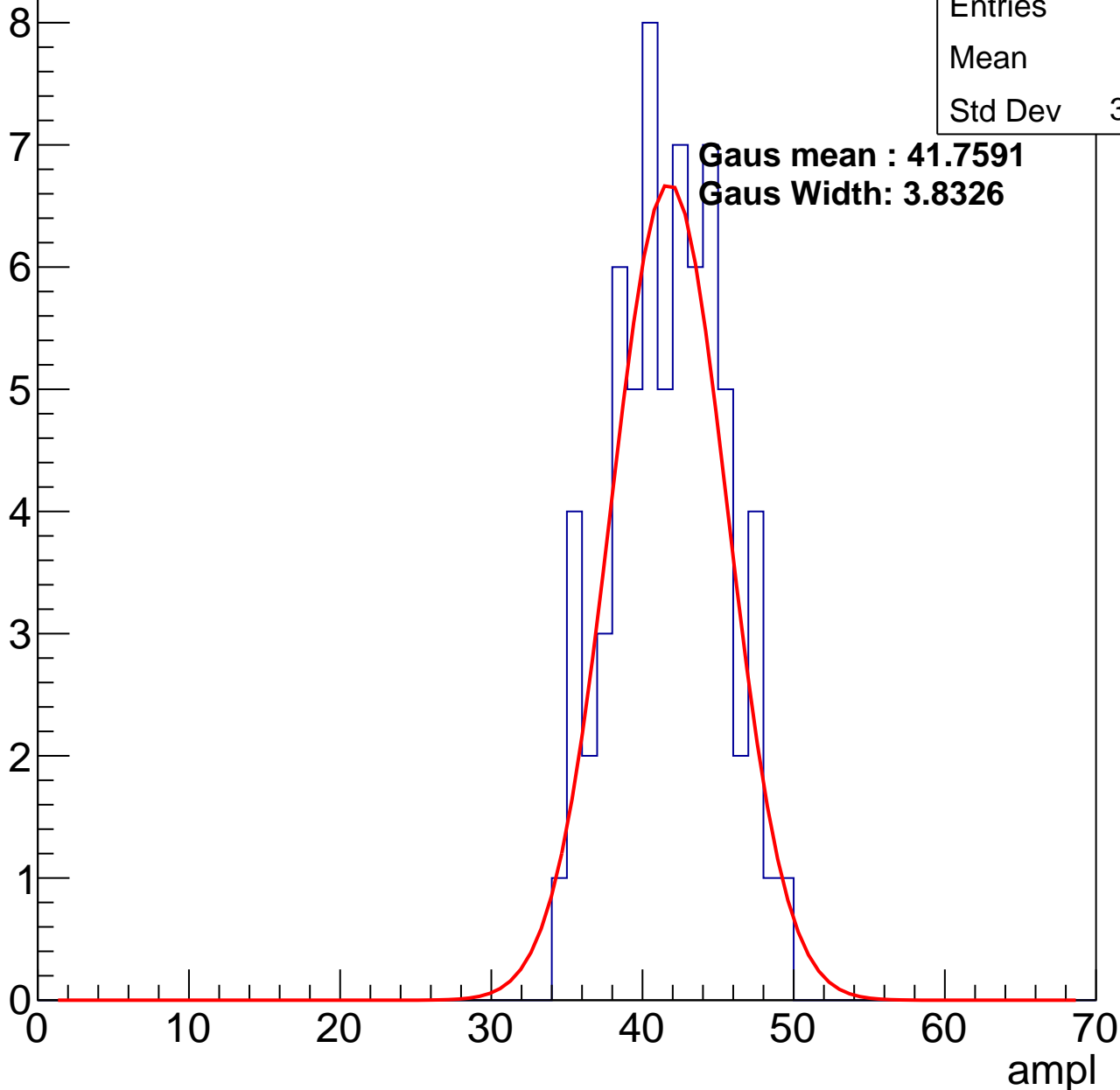
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	67
Mean	41.3
Std Dev	3.558

**Gaus mean : 41.7591**

**Gaus Width: 3.8326**

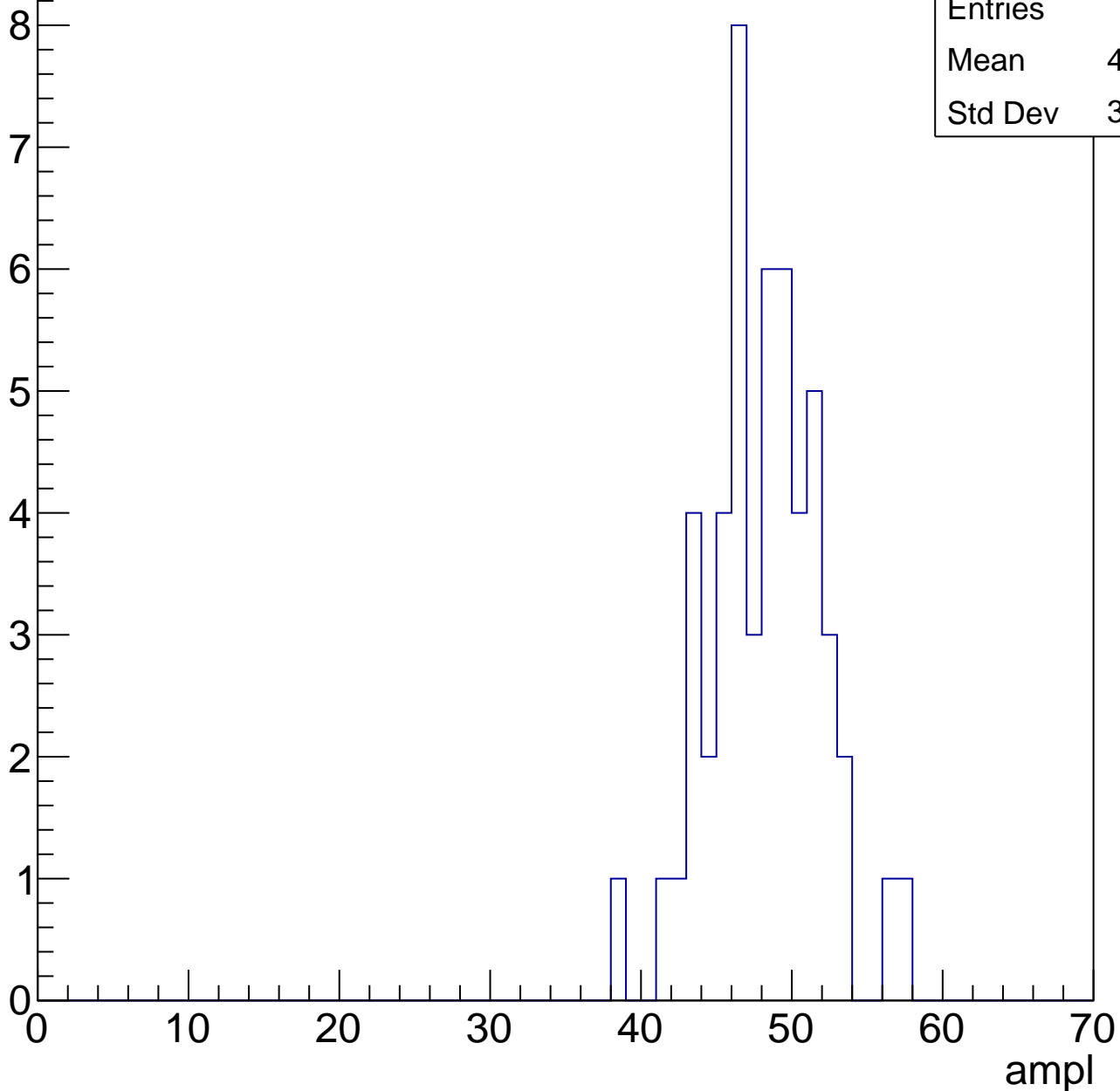


# B1L100S, U2-ch102, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

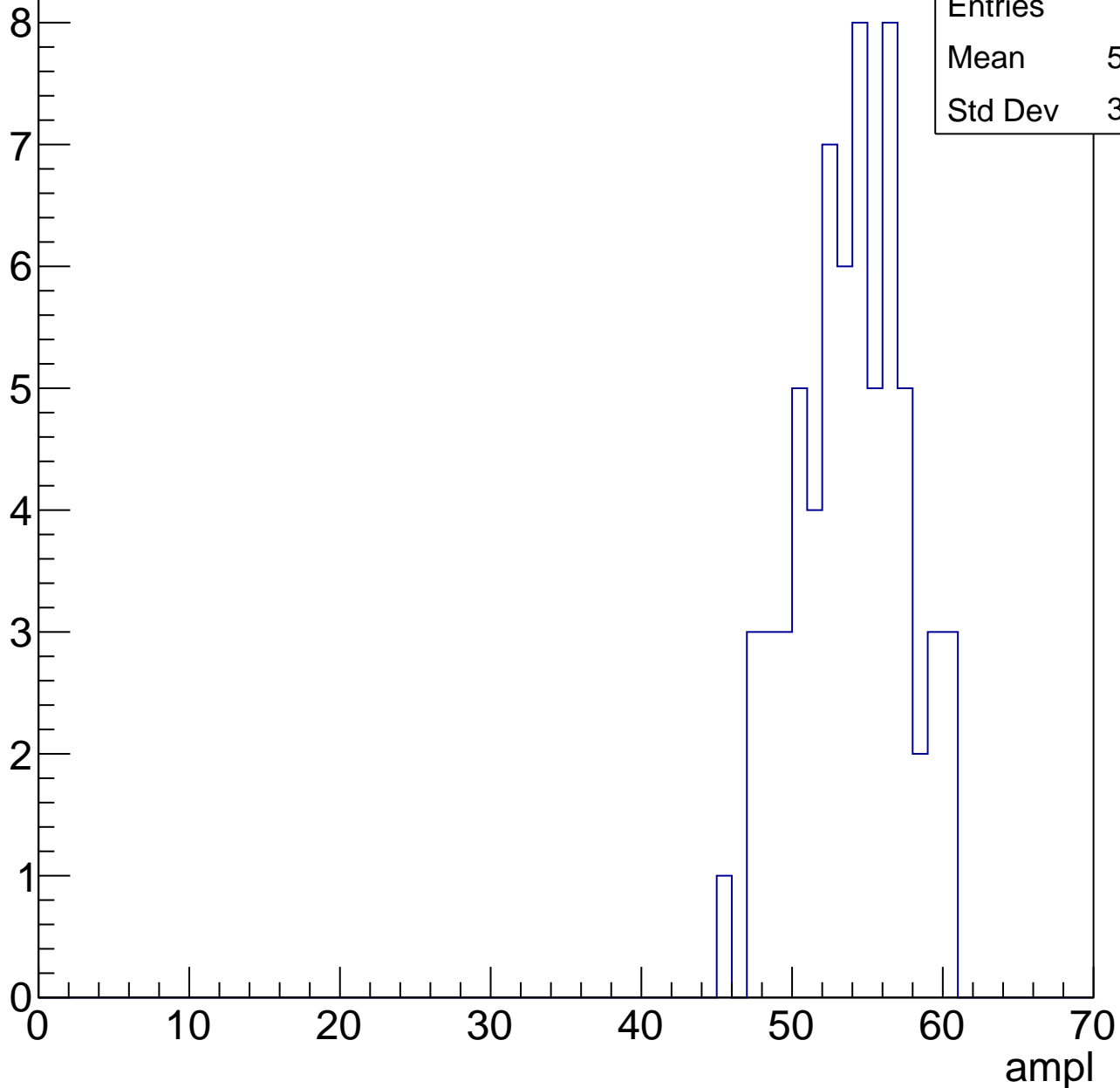
Entries	52
Mean	47.73
Std Dev	3.654



# B1L100S, U2-ch102, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

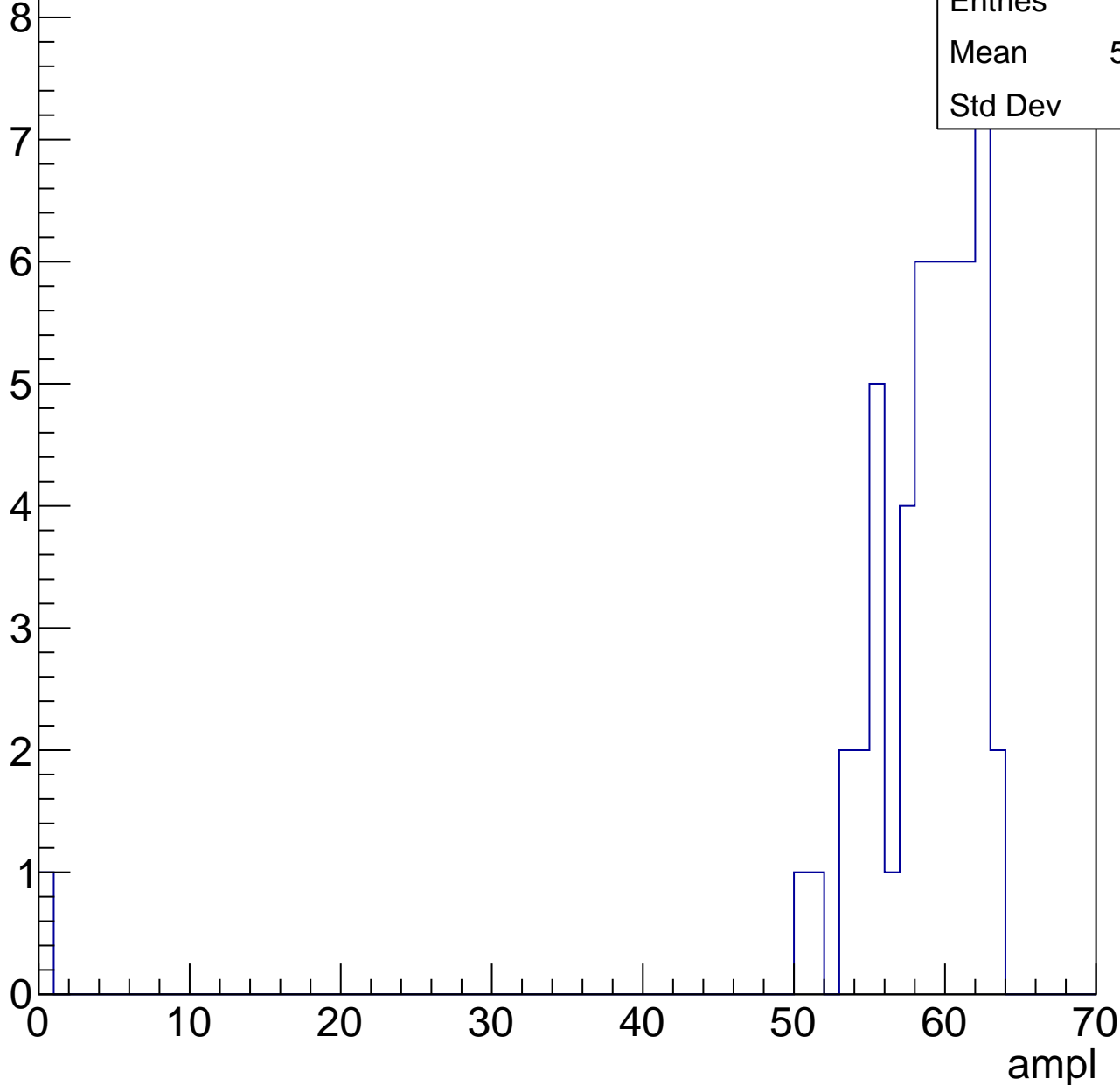


# B1L100S, U2-ch102, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	51
Mean	57.33
Std Dev	8.69



# B1L100S, U2-ch102, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

6

5

4

3

2

1

0

Entries

16

Mean

61.31

Std Dev

1.722

ampl

0

10

20

30

40

50

60

70



# B1L100S, U2-ch102, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



# B1L100S, U2-ch103, adc0

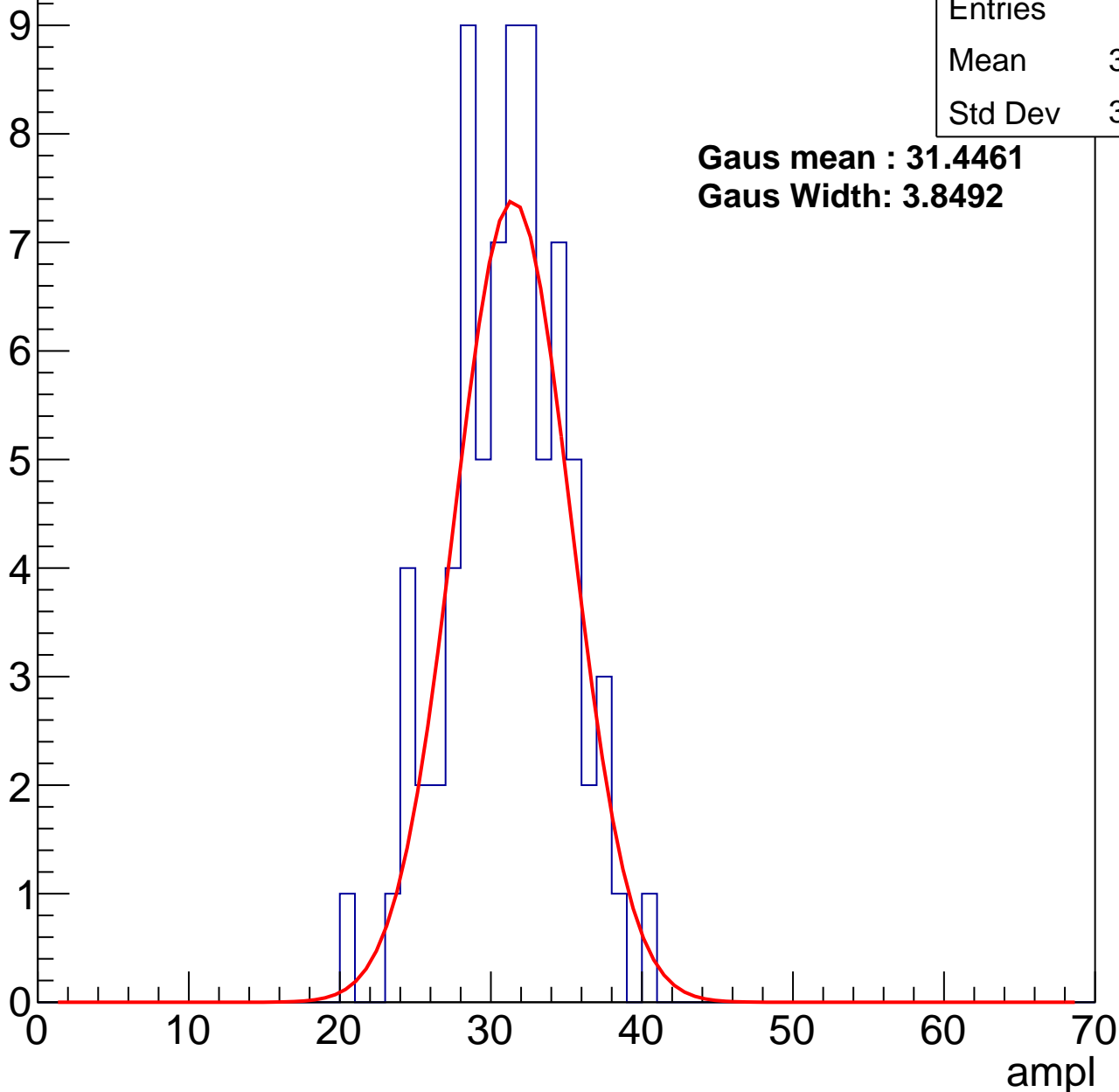
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	77
Mean	30.68
Std Dev	3.826

**Gaus mean : 31.4461**

**Gaus Width: 3.8492**



# B1L100S, U2-ch103, adc1

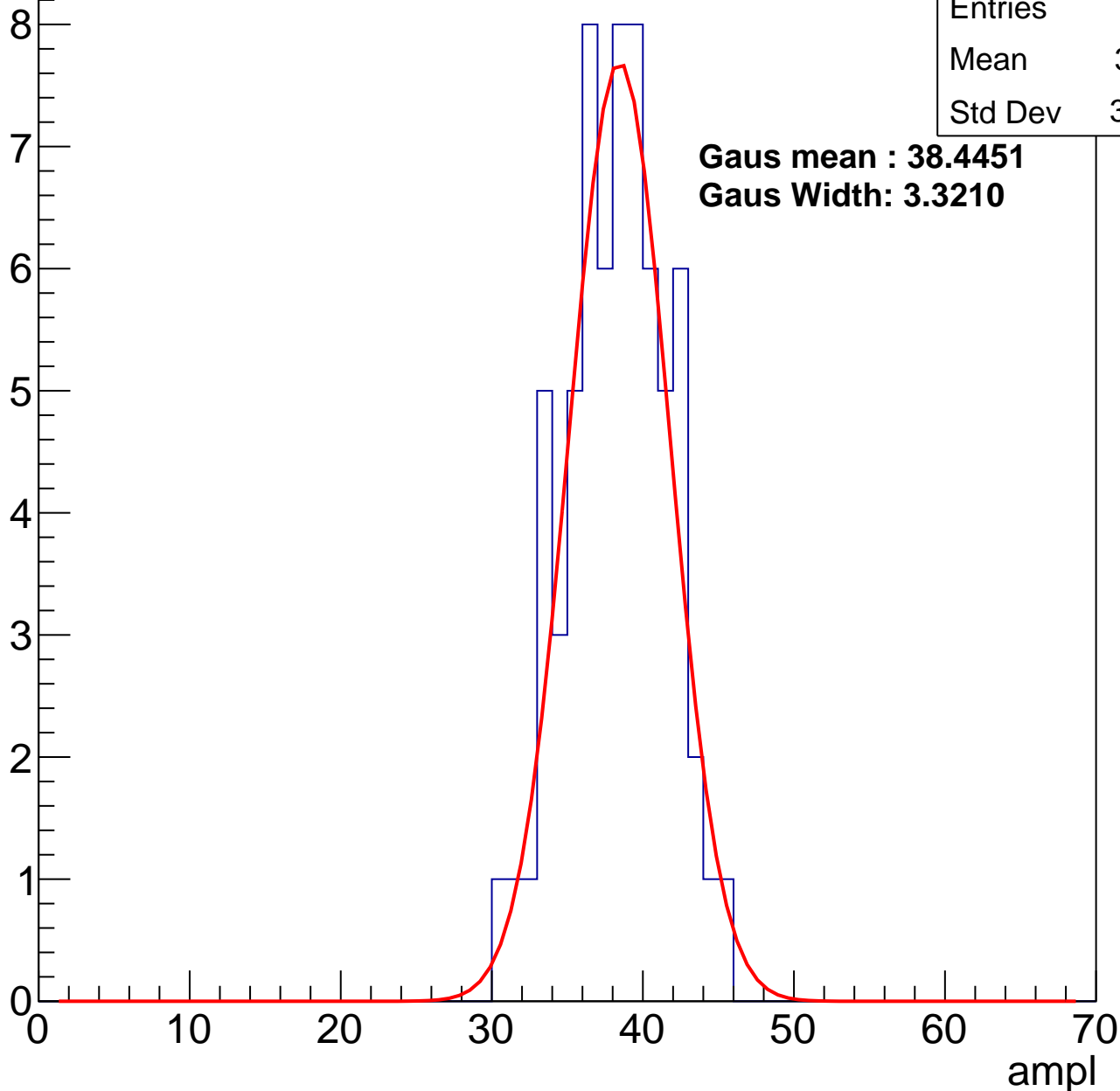
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	67
Mean	37.81
Std Dev	3.256

**Gaus mean : 38.4451**

**Gaus Width: 3.3210**



# B1L100S, U2-ch103, adc2

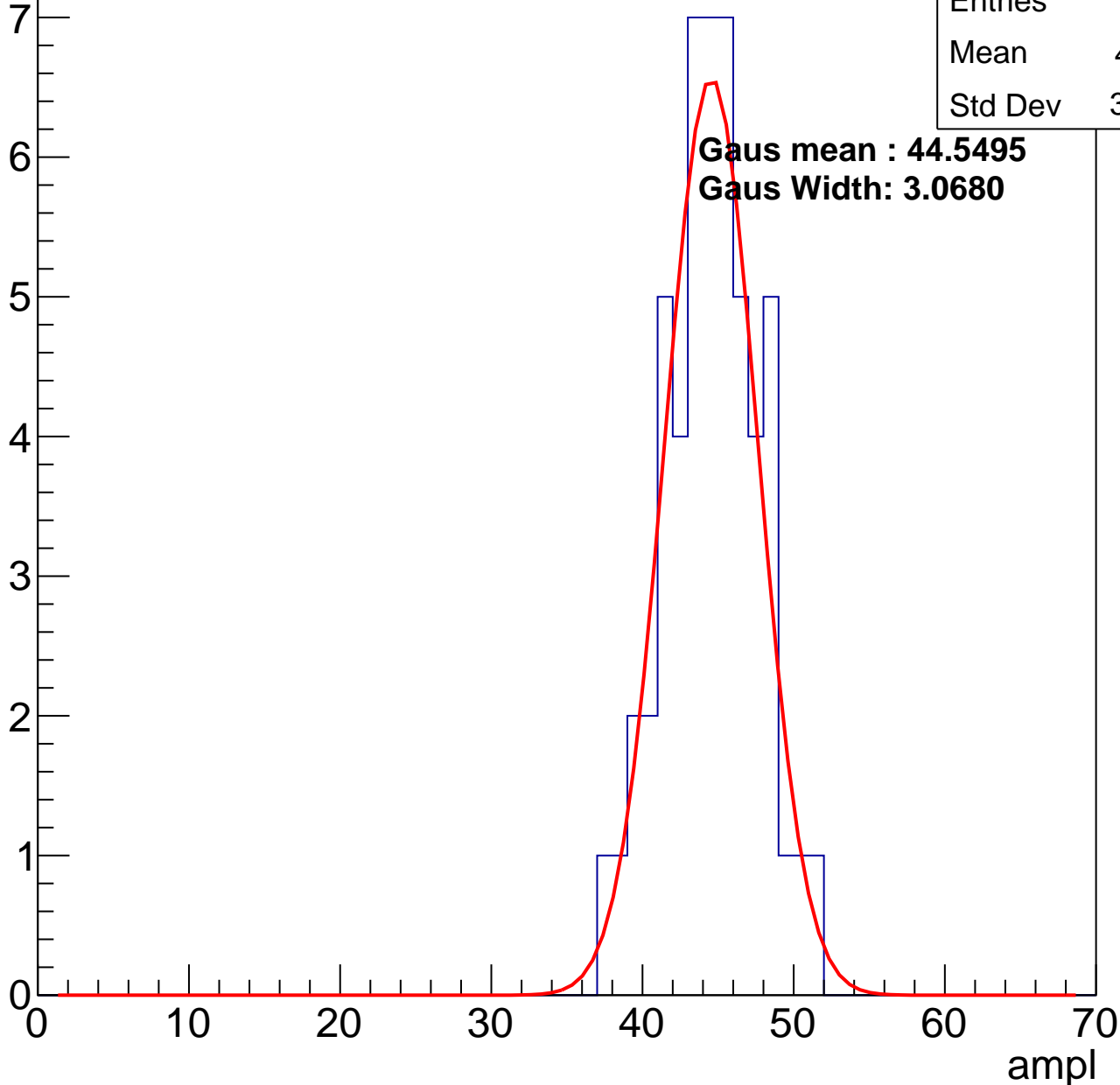
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	53
Mean	44.11
Std Dev	3.032

**Gaus mean : 44.5495**

**Gaus Width: 3.0680**

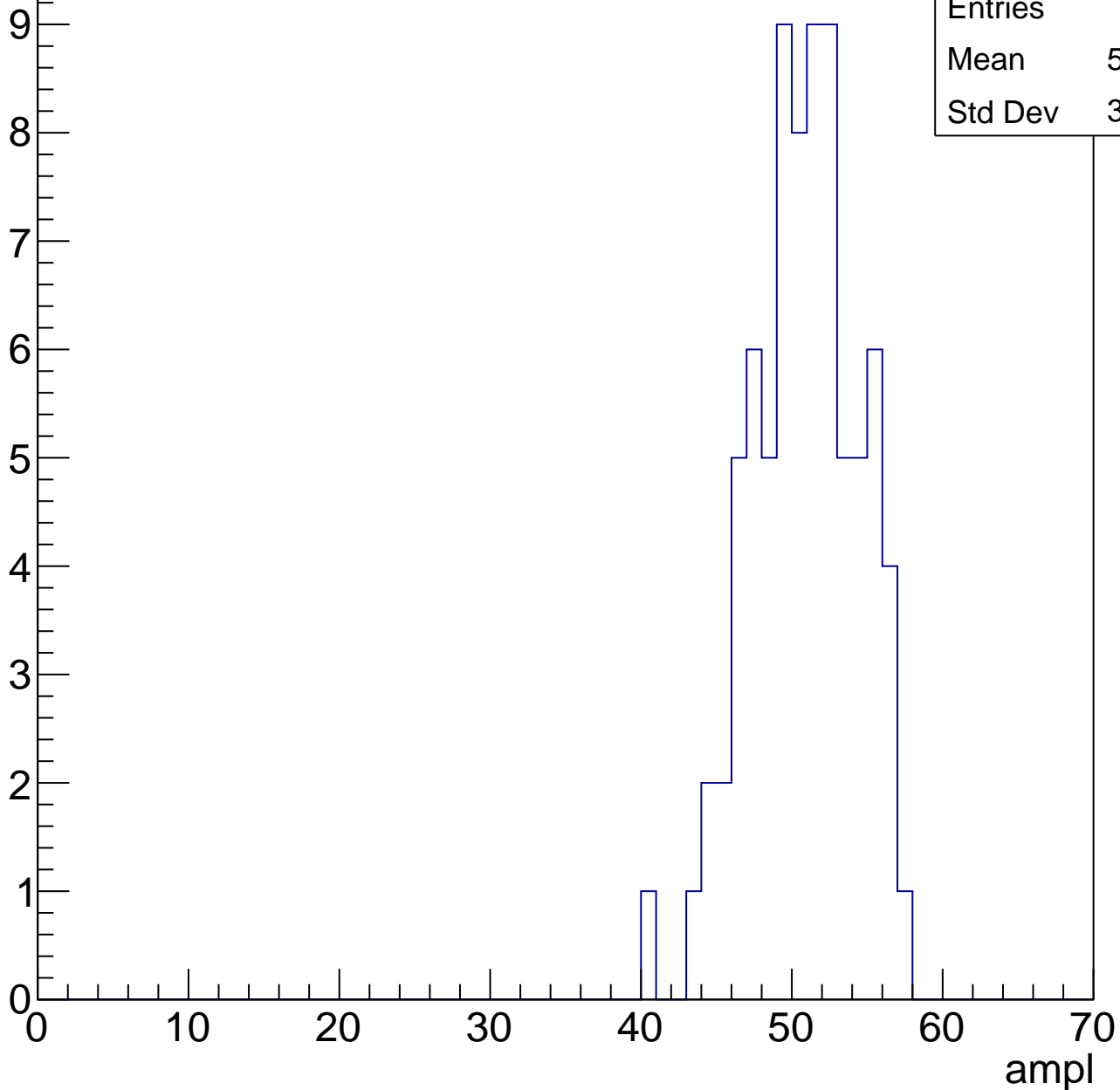


# B1L100S, U2-ch103, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	78
Mean	50.35
Std Dev	3.467

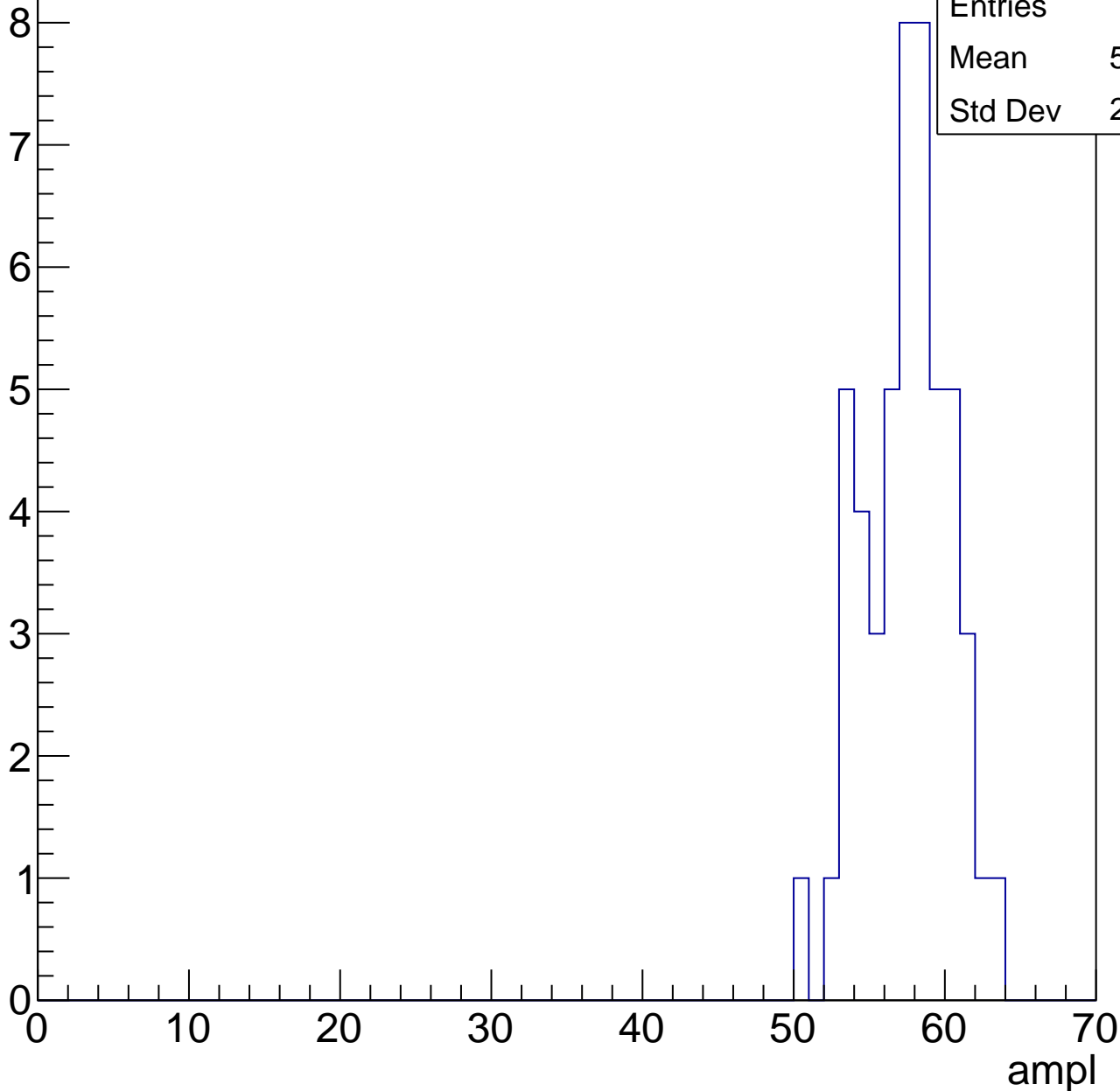


# B1L100S, U2-ch103, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

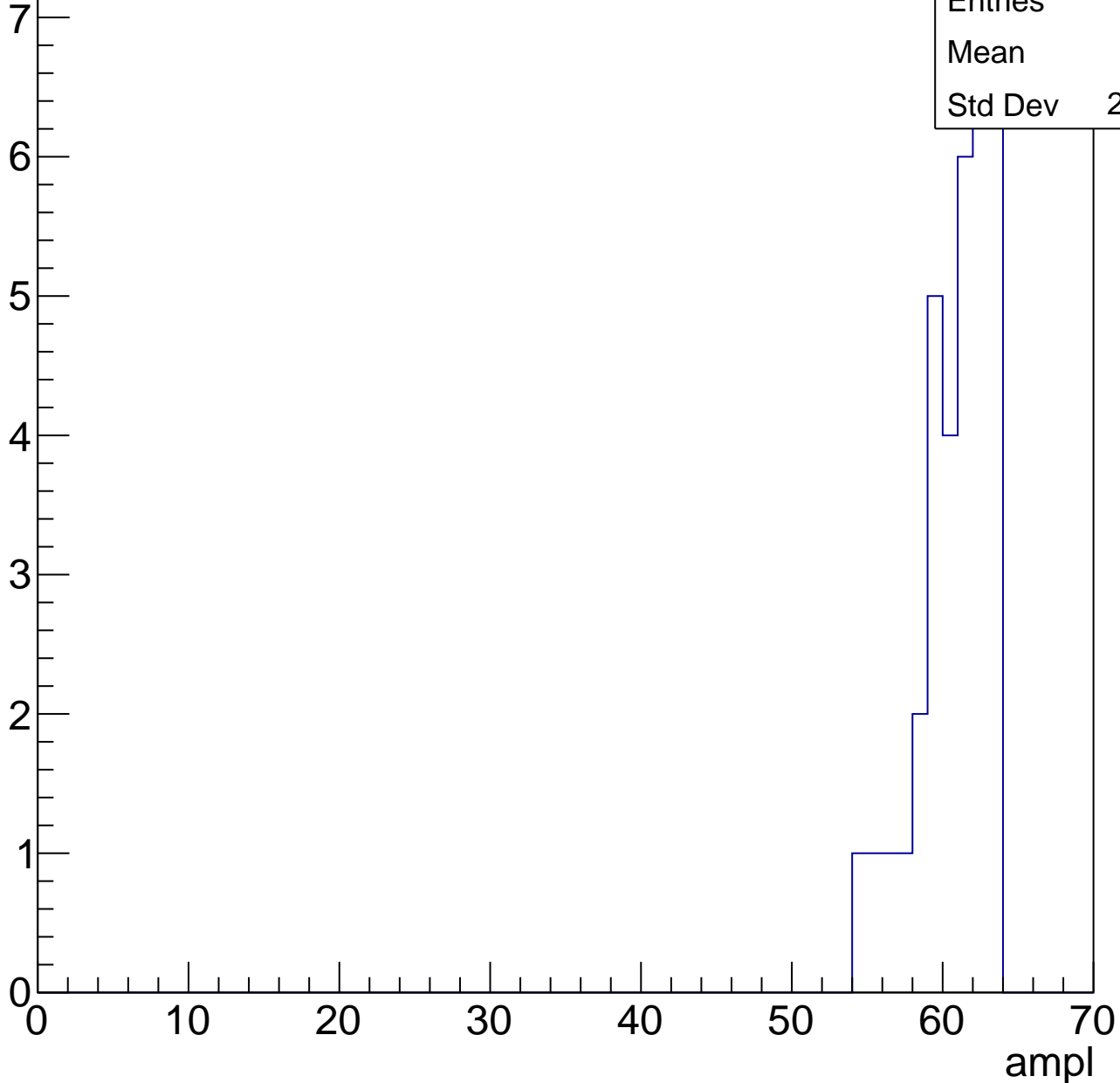
Entries	50
Mean	57.02
Std Dev	2.789



# B1L100S, U2-ch103, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

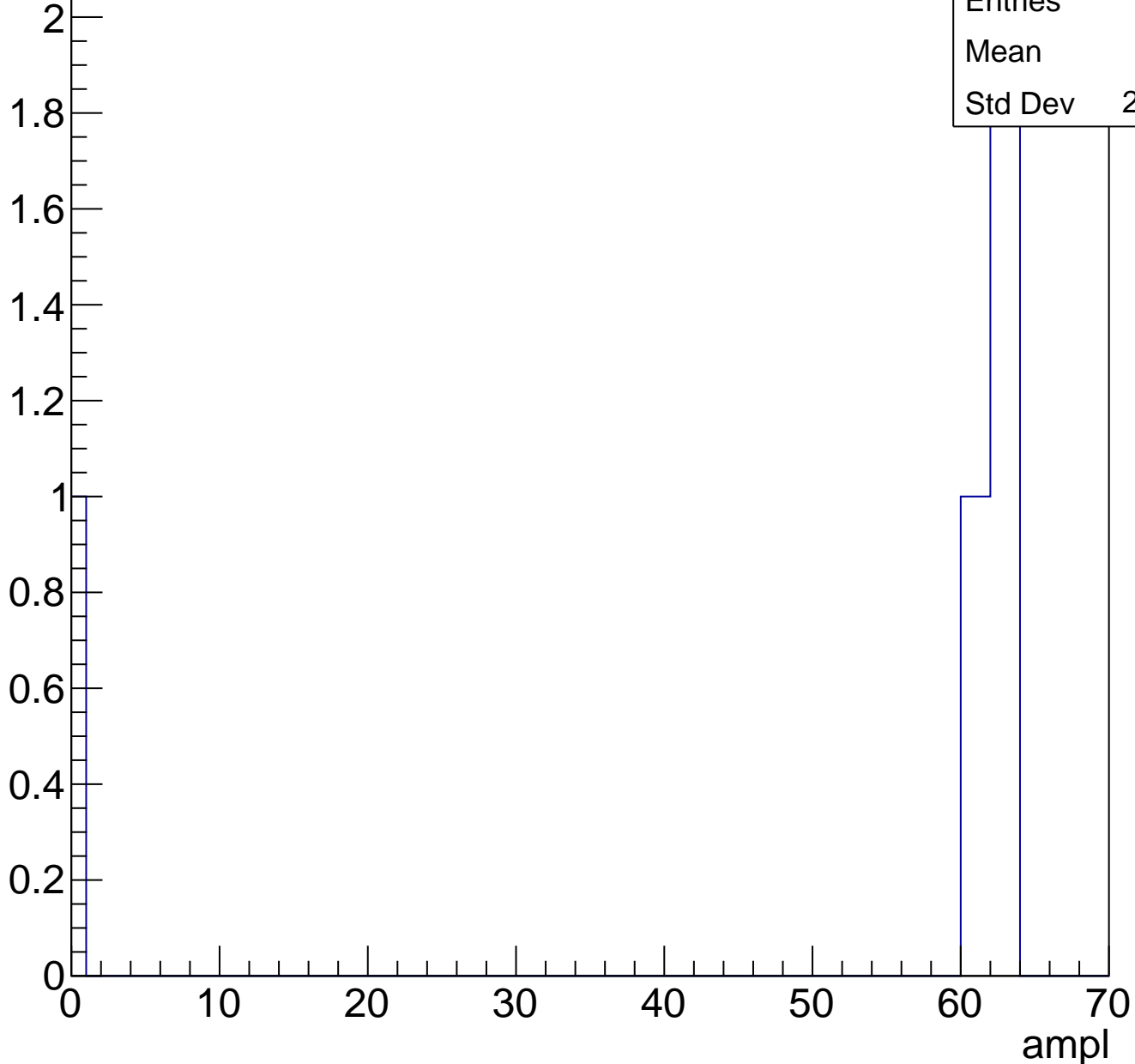
Entry



# B1L100S, U2-ch103, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	7
Mean	53
Std Dev	21.66



# B1L100S, U2-ch103, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L100S, U2-ch104, adc0

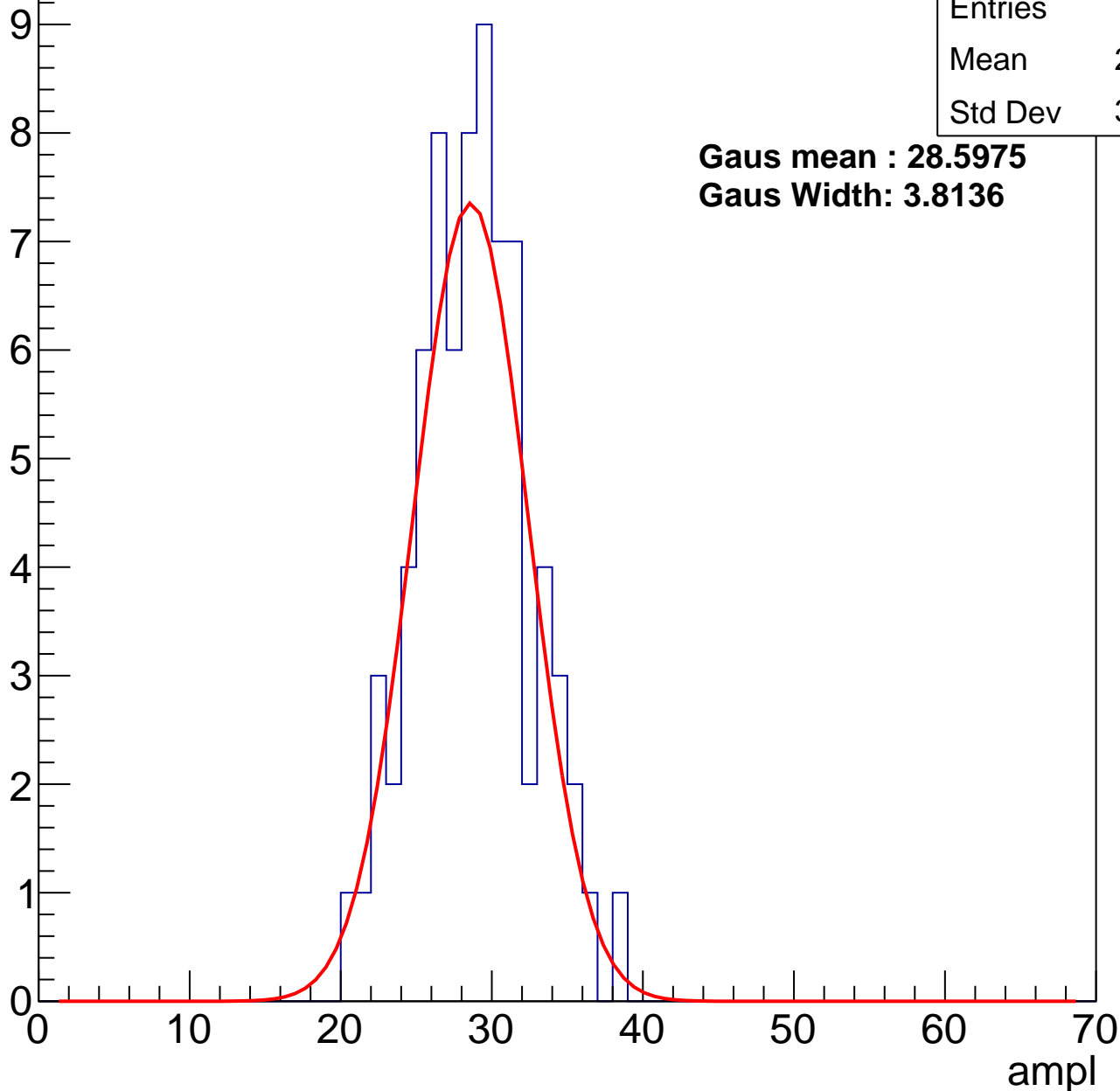
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	75
Mean	28.31
Std Dev	3.691

**Gaus mean : 28.5975**

**Gaus Width: 3.8136**



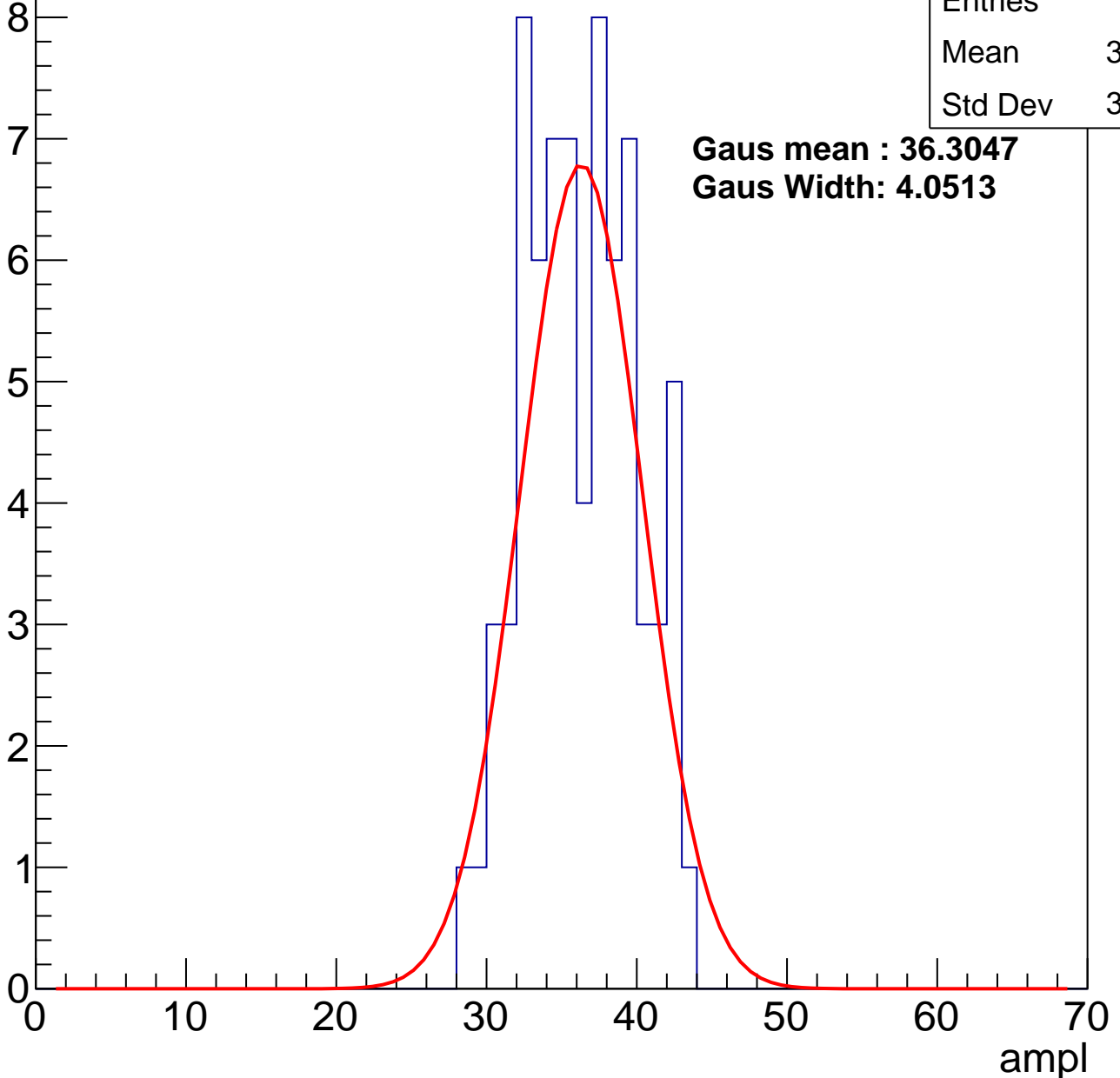
# B1L100S, U2-ch104, adc1

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	73
Mean	35.81
Std Dev	3.621

**Gaus mean : 36.3047**  
**Gaus Width: 4.0513**



# B1L100S, U2-ch104, adc2

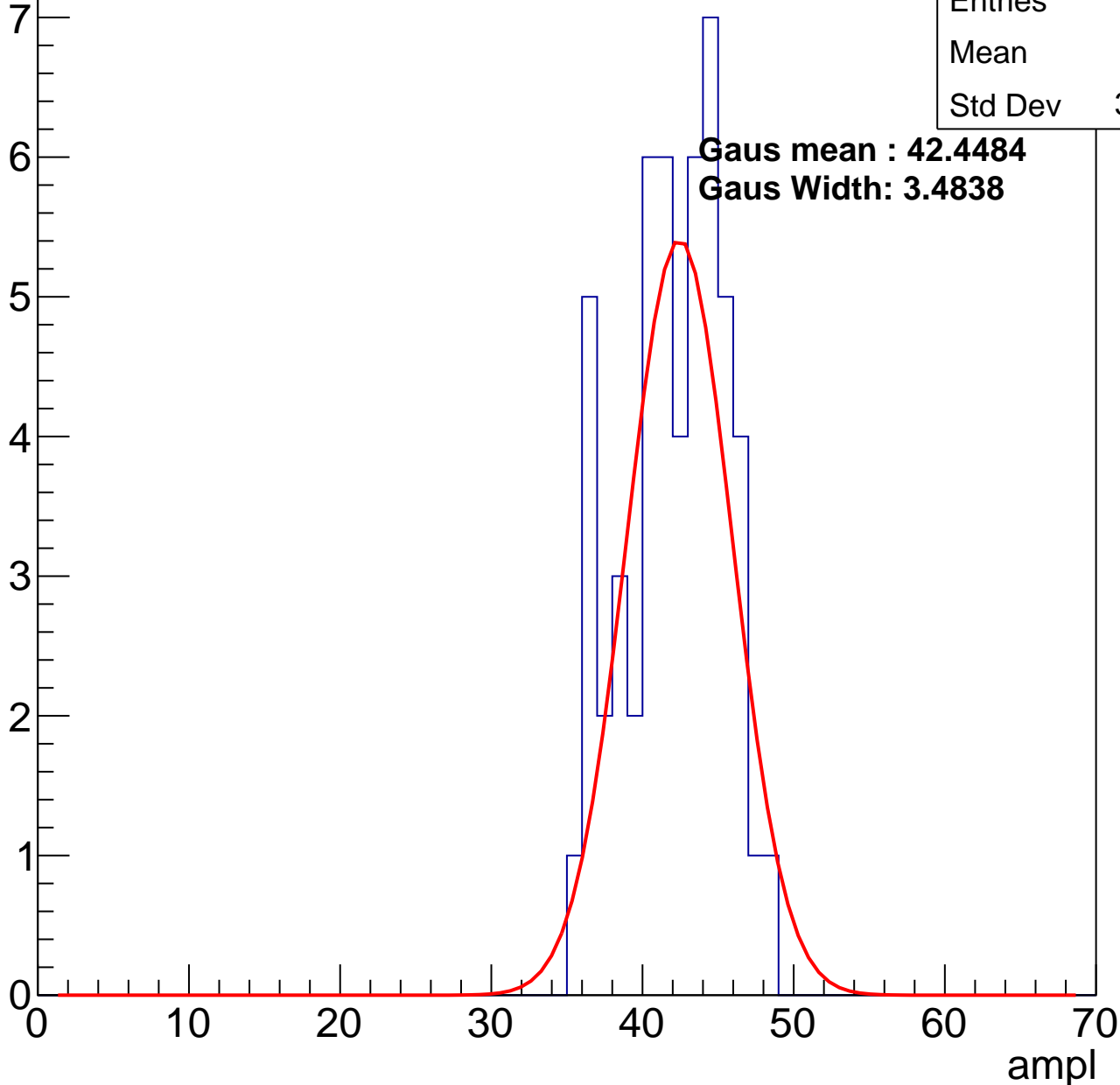
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	53
Mean	41.6
Std Dev	3.281

**Gaus mean : 42.4484**

**Gaus Width: 3.4838**



# B1L100S, U2-ch104, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	67
Mean	47.87
Std Dev	3.218

Entry

10

8

6

4

2

0

0

10

20

30

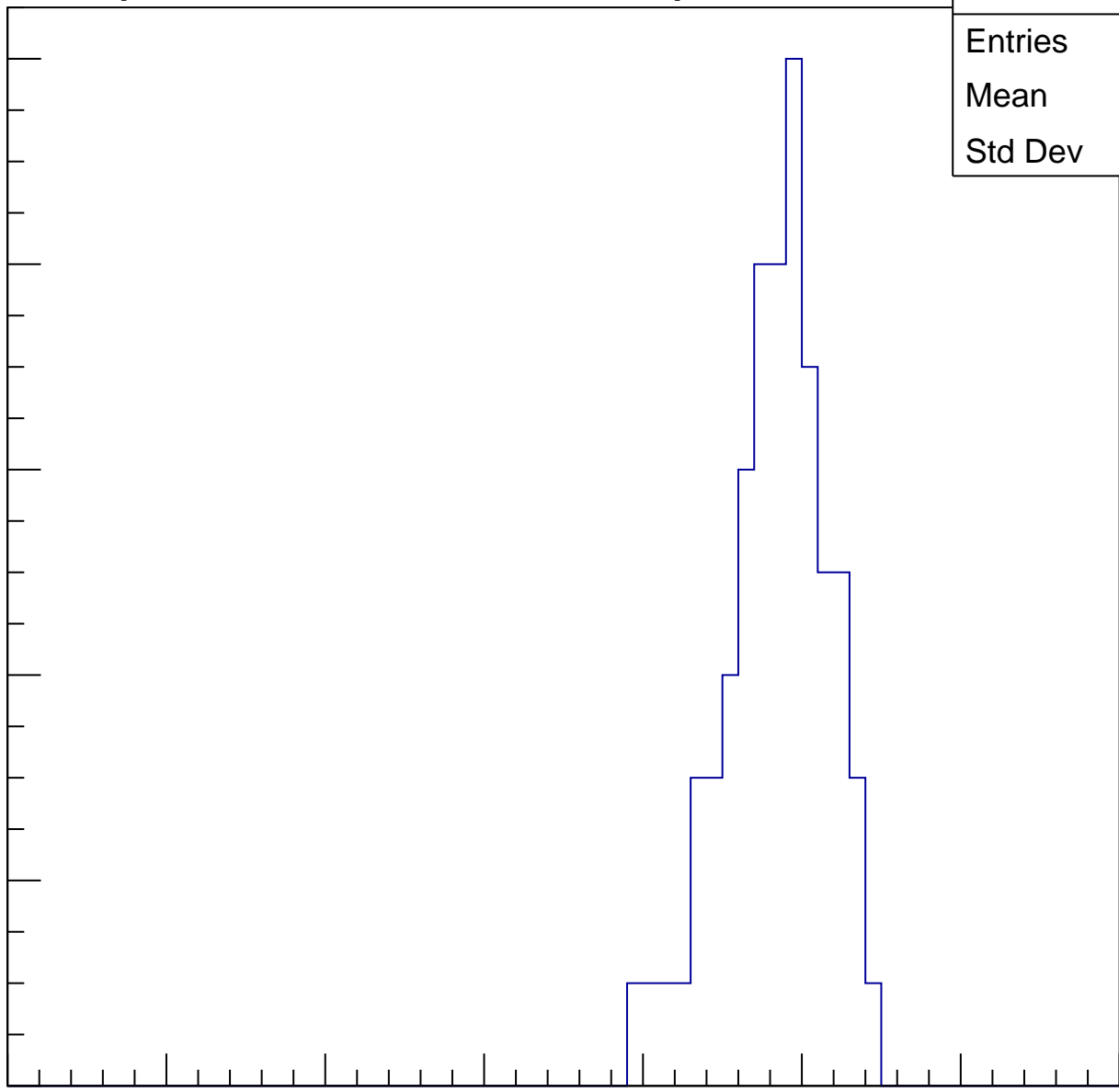
40

50

60

70

ampl

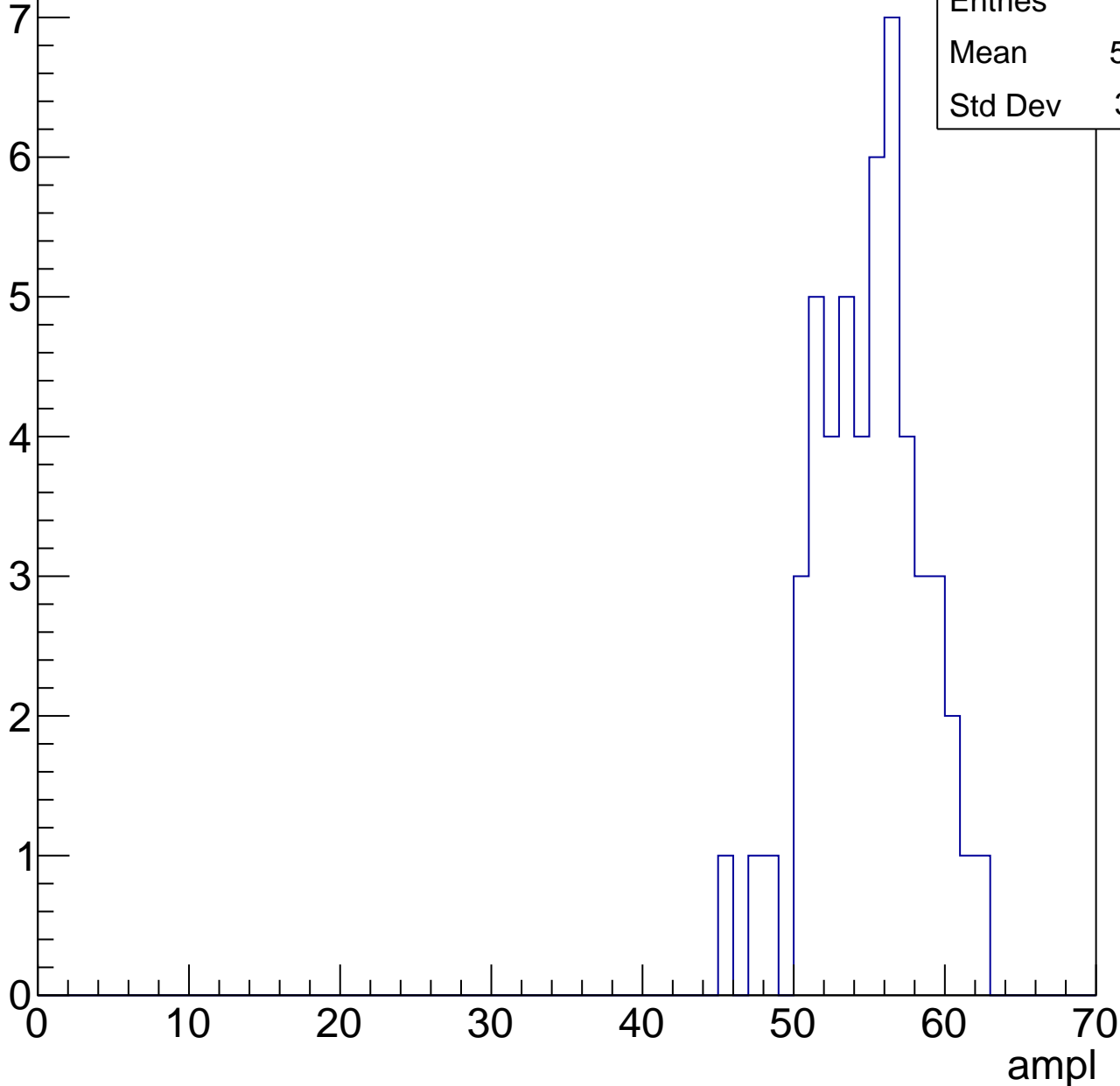


# B1L100S, U2-ch104, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	51
Mean	54.47
Std Dev	3.561

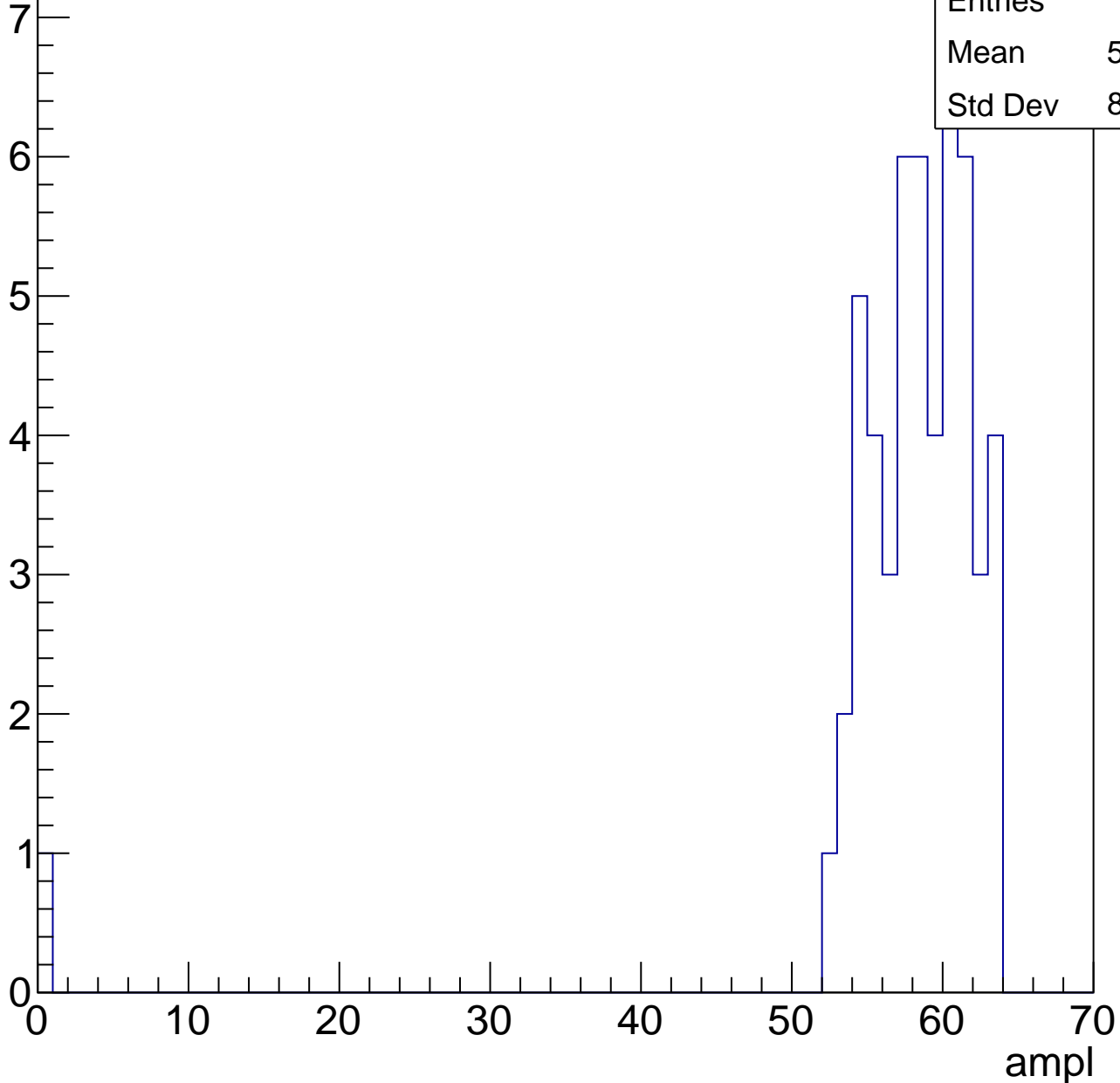


# B1L100S, U2-ch104, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	52
Mean	57.04
Std Dev	8.515

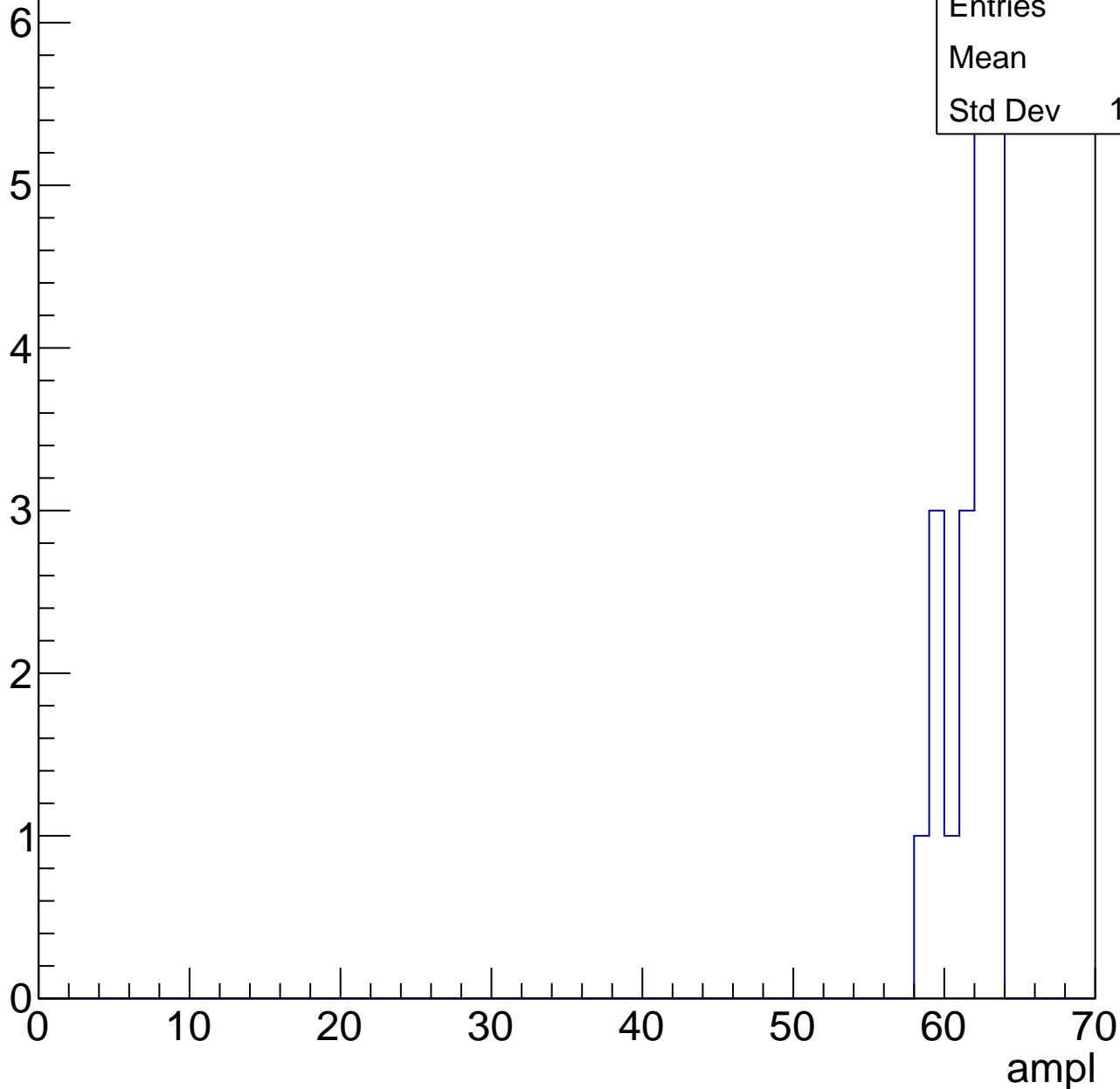


# B1L100S, U2-ch104, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	20
Mean	61.4
Std Dev	1.562





# B1L100S, U2-ch104, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	3
Mean	6.667
Std Dev	9.428

# B1L100S, U2-ch105, adc0

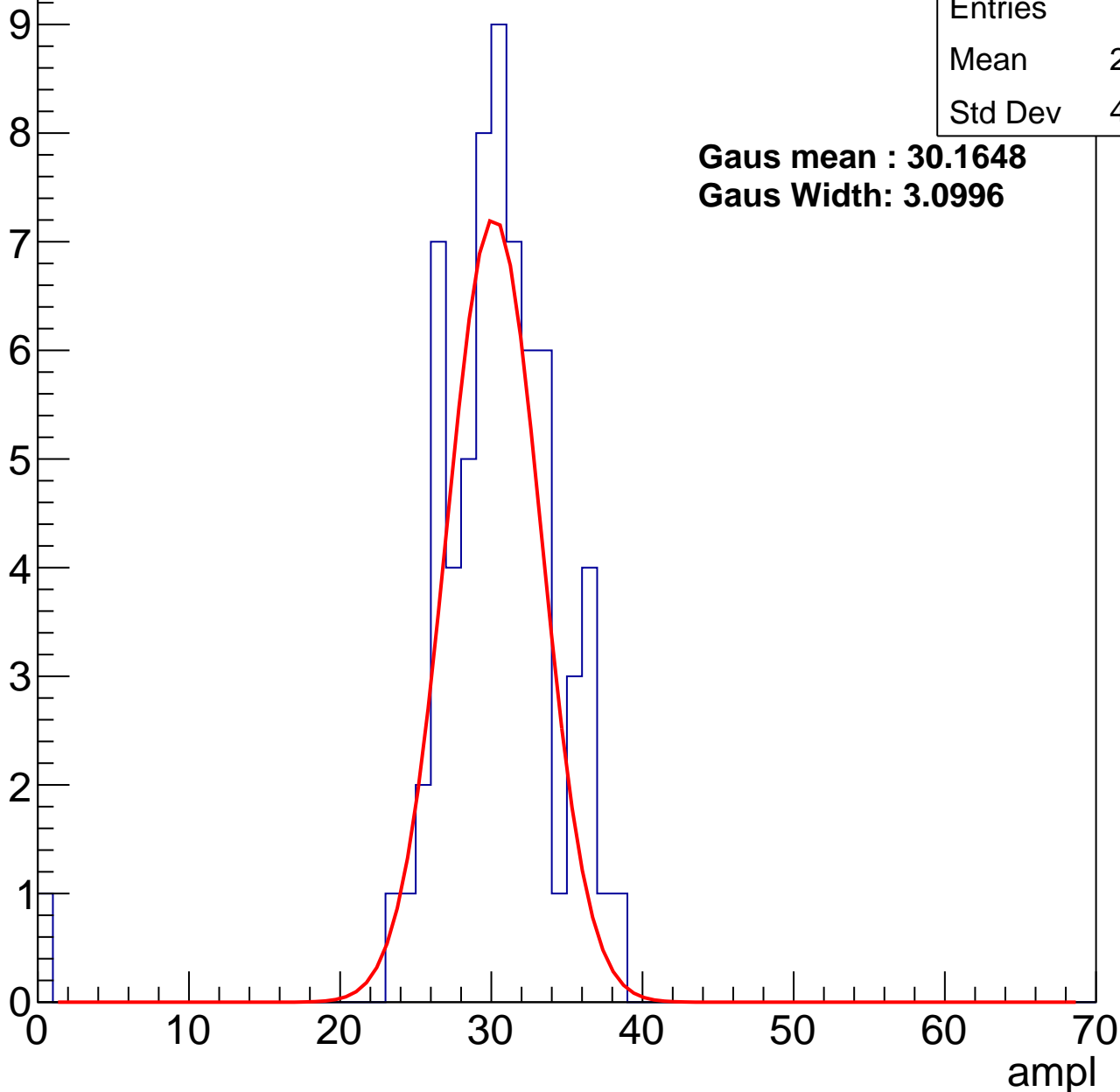
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	67
Mean	29.76
Std Dev	4.948

**Gaus mean : 30.1648**

**Gaus Width: 3.0996**



# B1L100S, U2-ch105, adc1

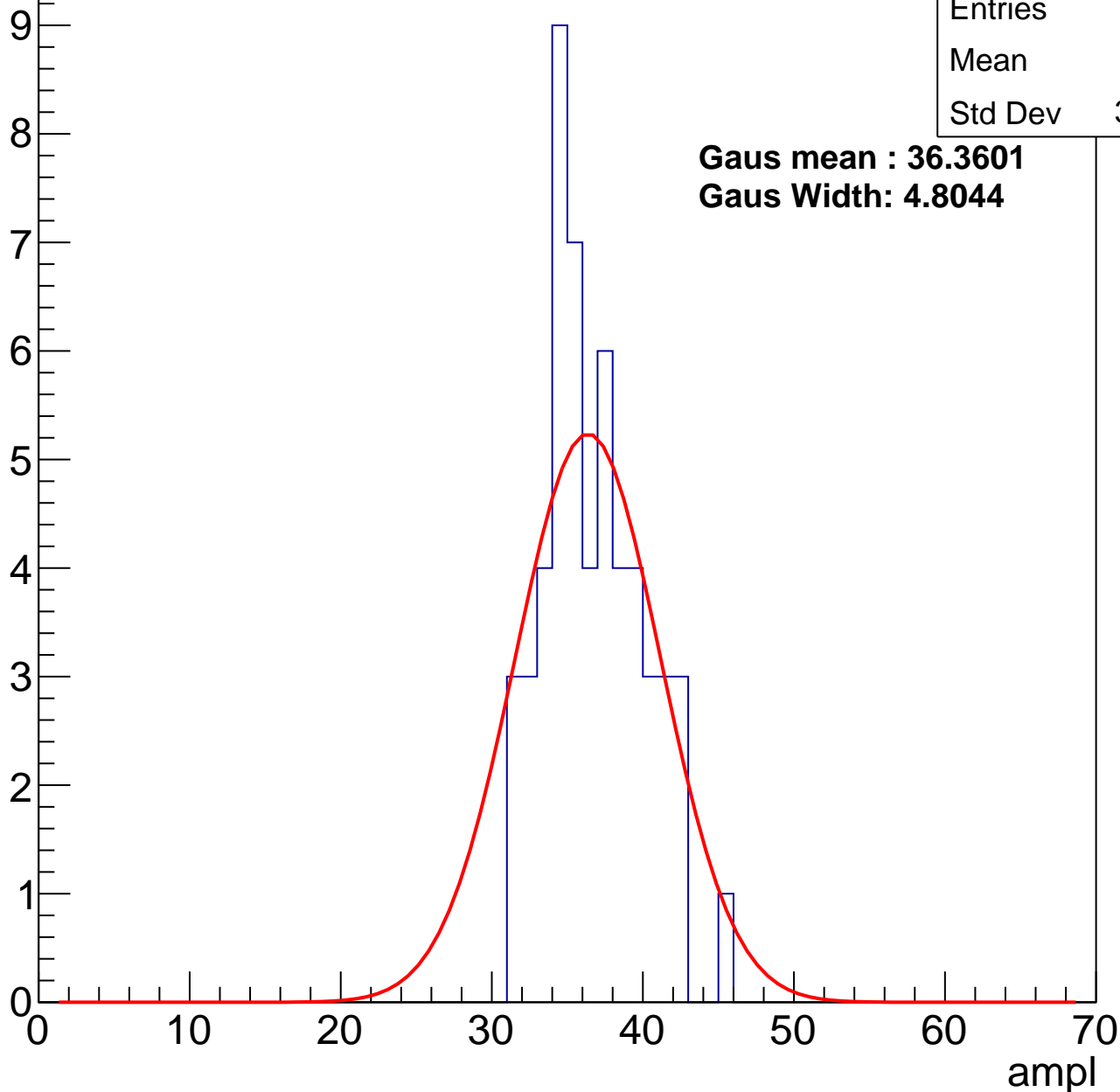
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	54
Mean	36.3
Std Dev	3.241

**Gaus mean : 36.3601**

**Gaus Width: 4.8044**



# B1L100S, U2-ch105, adc2

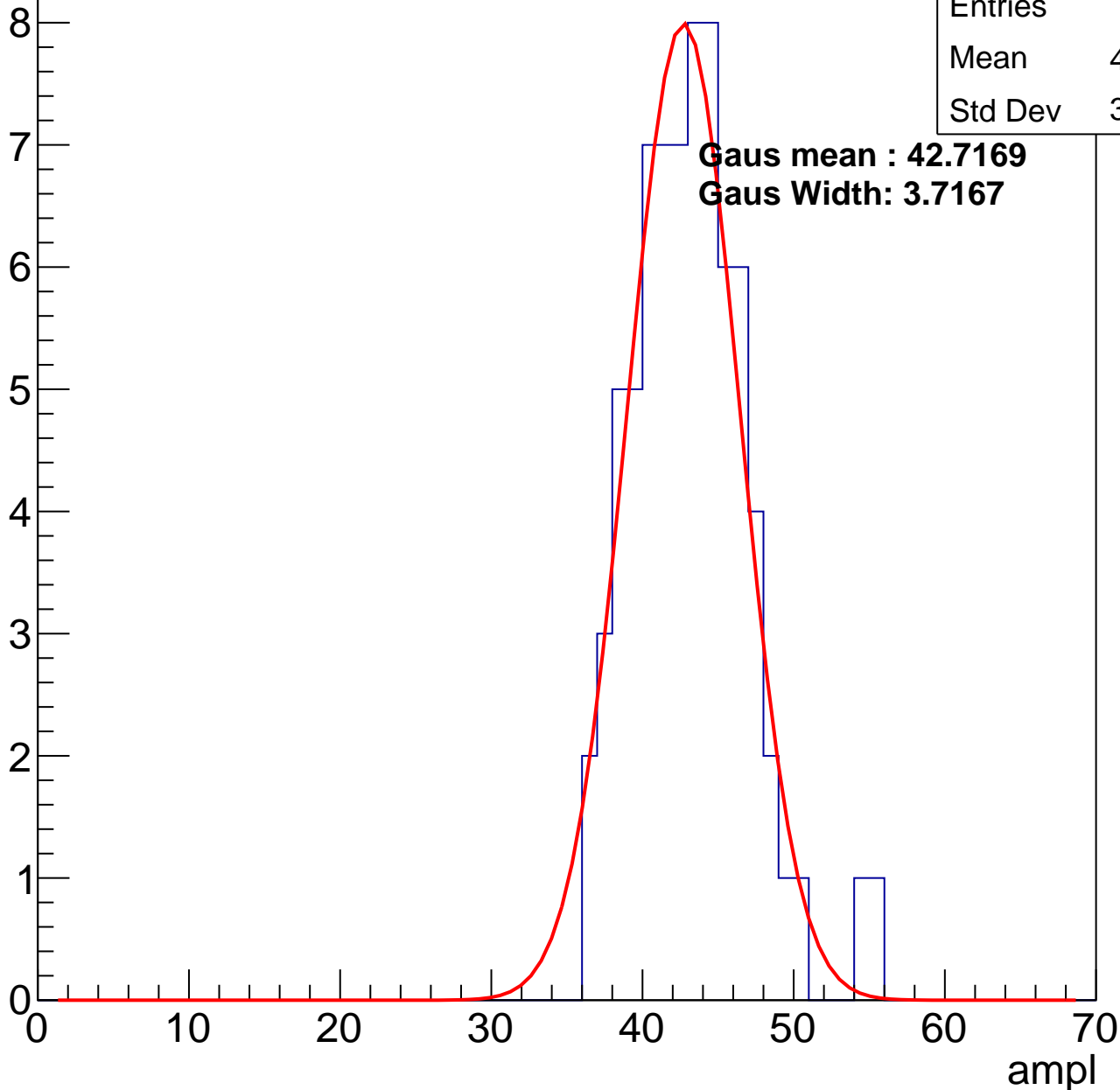
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	74
Mean	42.74
Std Dev	3.774

**Gaus mean : 42.7169**

**Gaus Width: 3.7167**

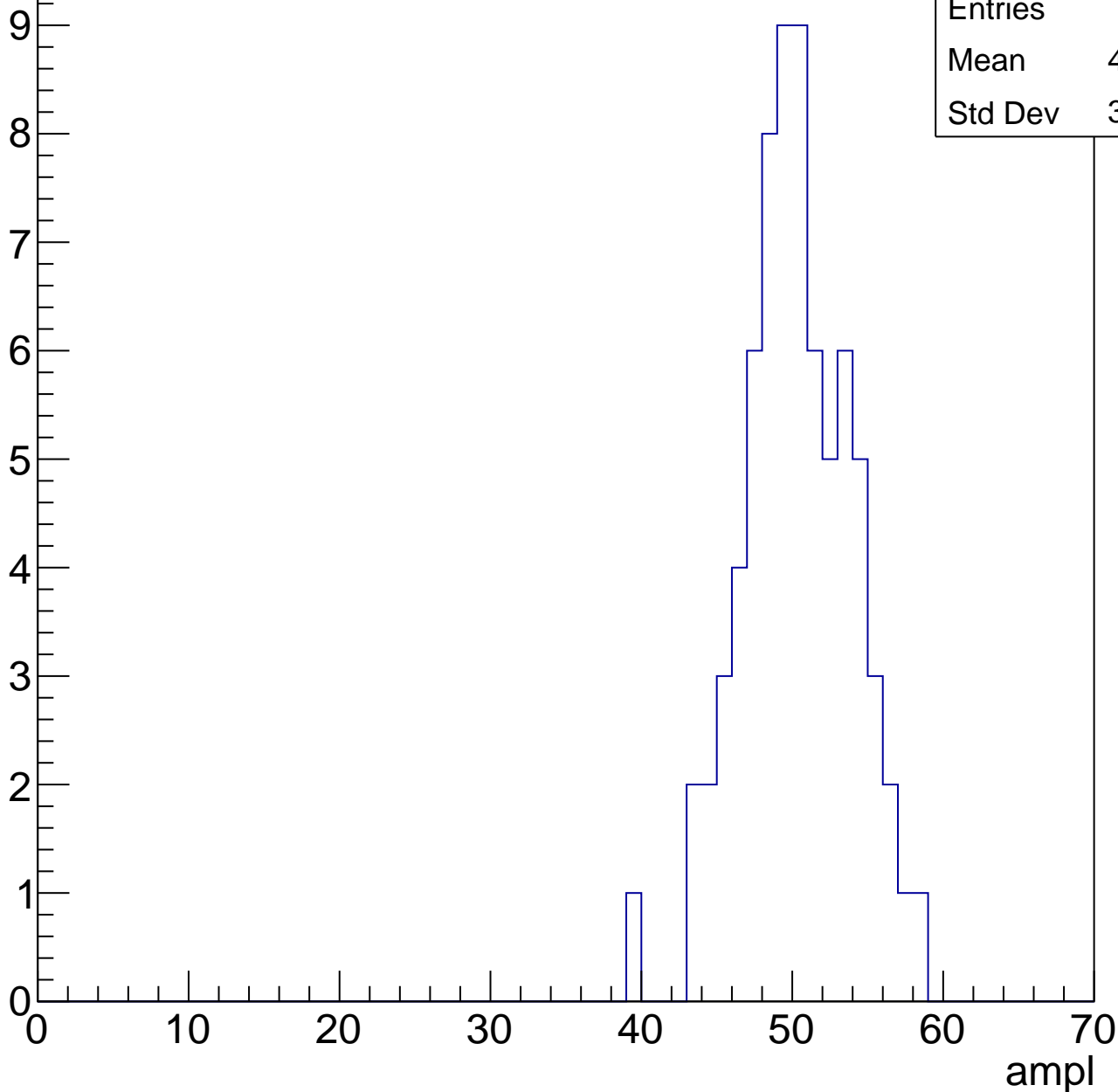


# B1L100S, U2-ch105, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	73
Mean	49.79
Std Dev	3.592

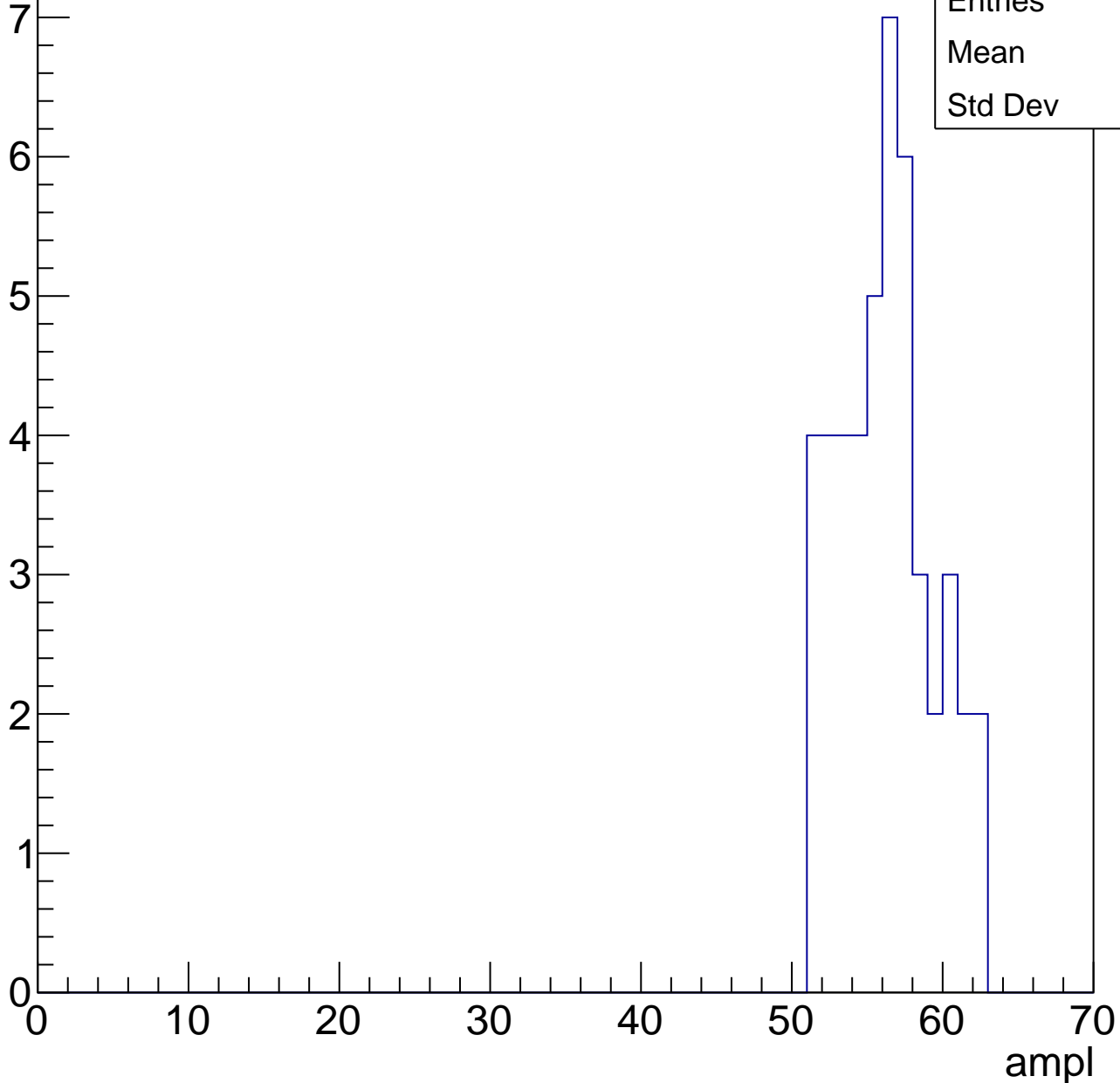


# B1L100S, U2-ch105, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

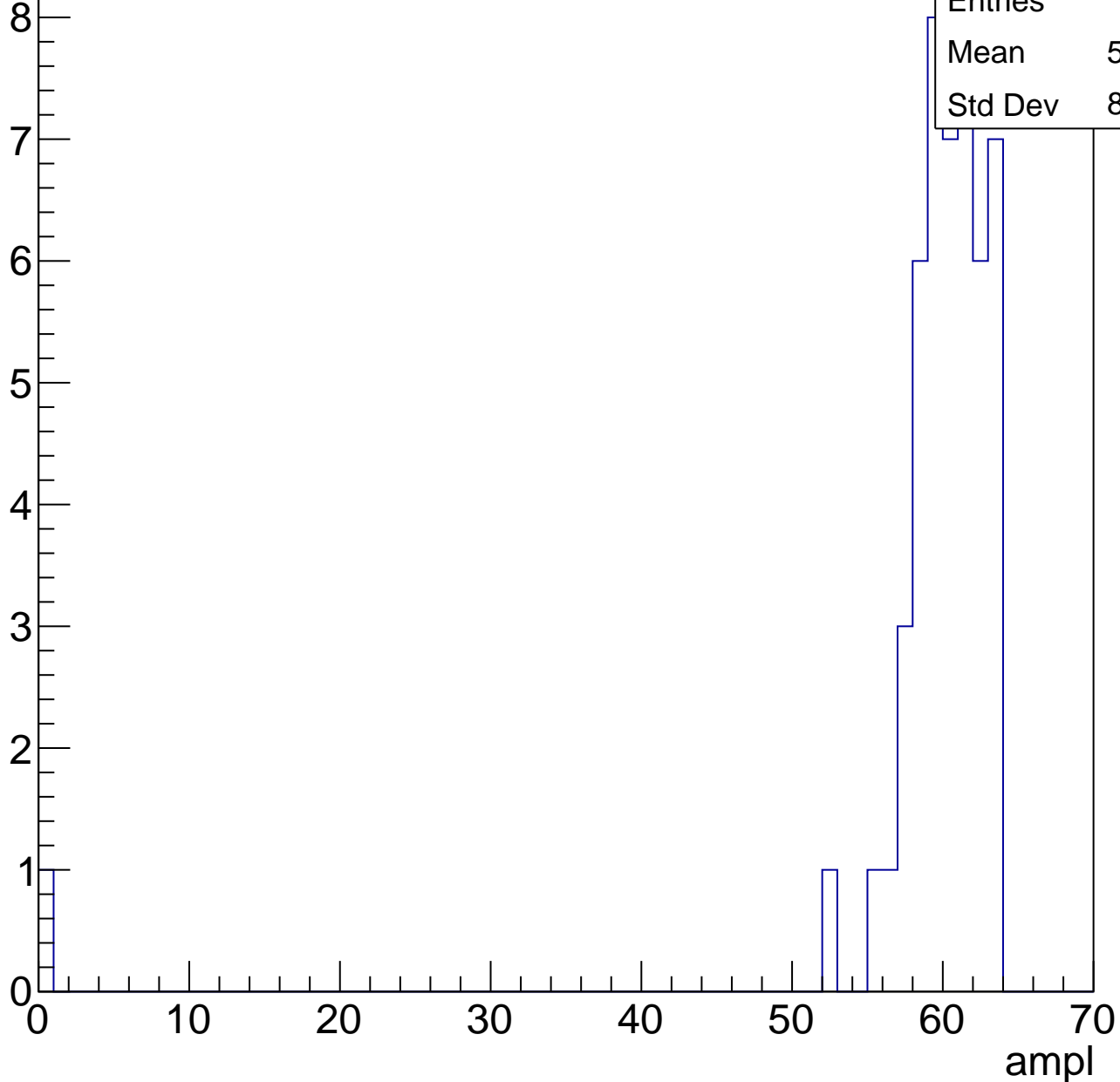
Entries	46
Mean	55.8
Std Dev	3.04



# B1L100S, U2-ch105, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



# B1L100S, U2-ch105, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry





# B1L100S, U2-ch105, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



# B1L100S, U2-ch106, adc0

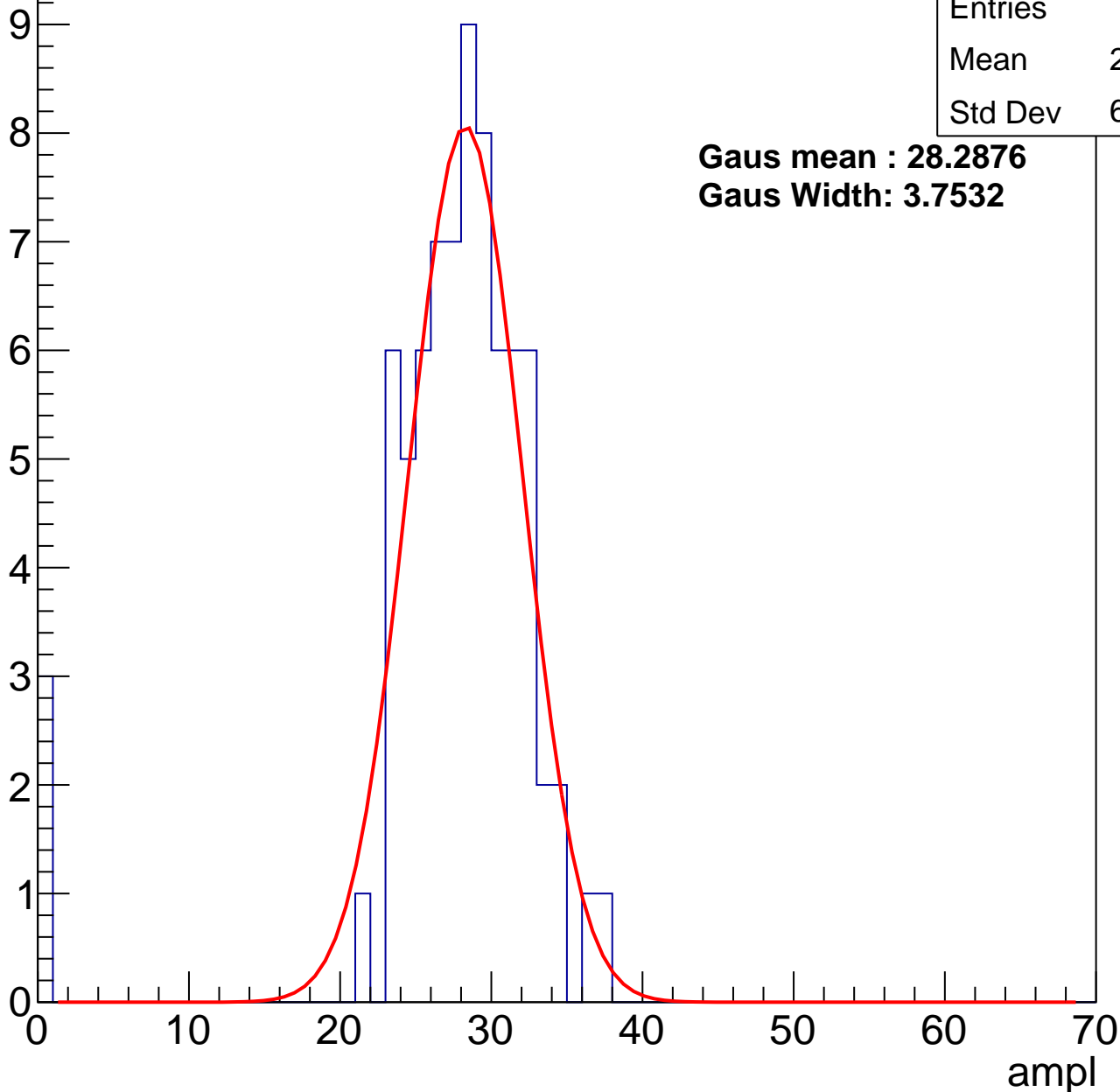
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	76
Mean	26.96
Std Dev	6.373

**Gaus mean : 28.2876**

**Gaus Width: 3.7532**



# B1L100S, U2-ch106, adc1

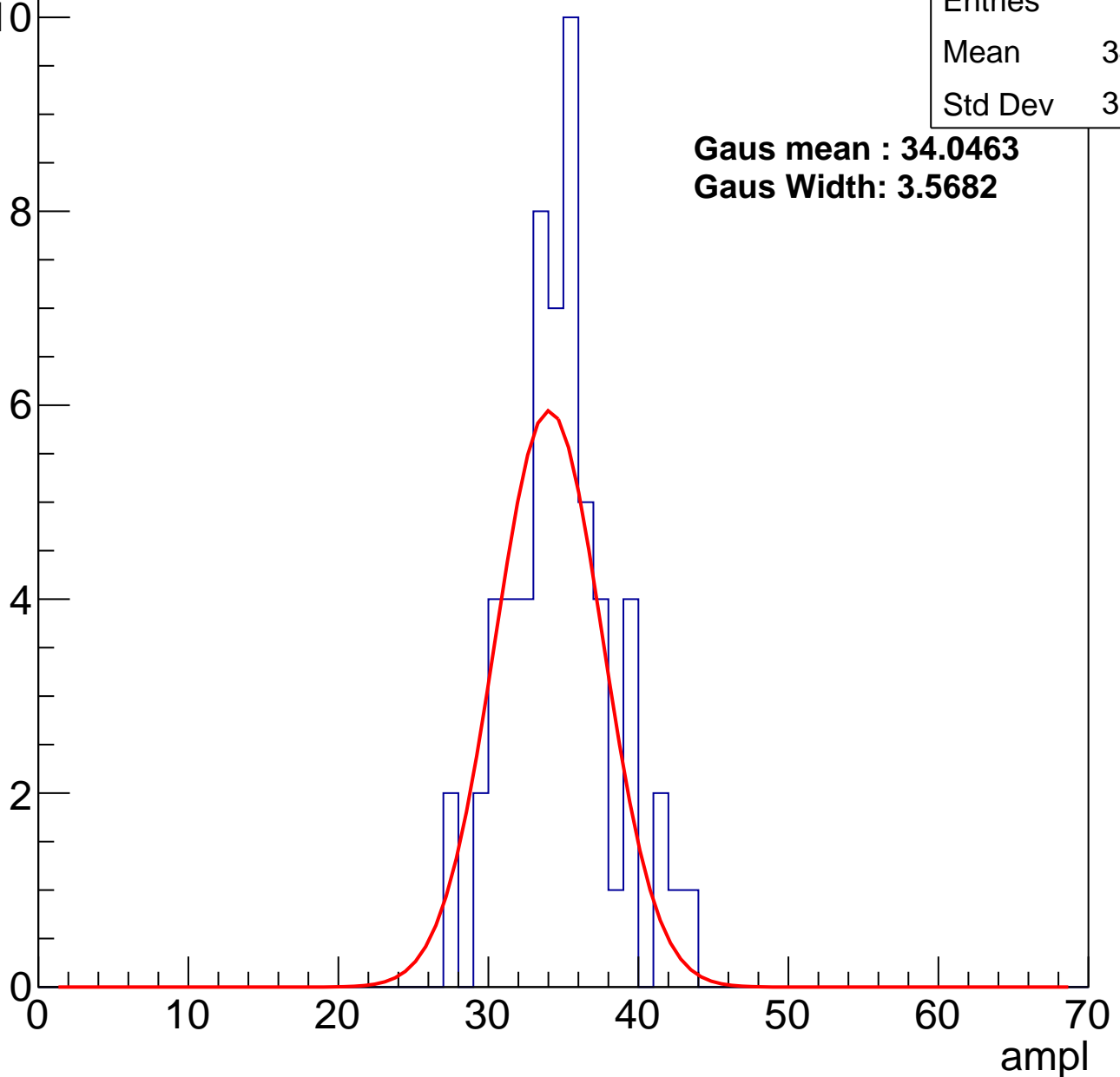
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	59
Mean	34.32
Std Dev	3.422

**Gaus mean : 34.0463**

**Gaus Width: 3.5682**



# B1L100S, U2-ch106, adc2

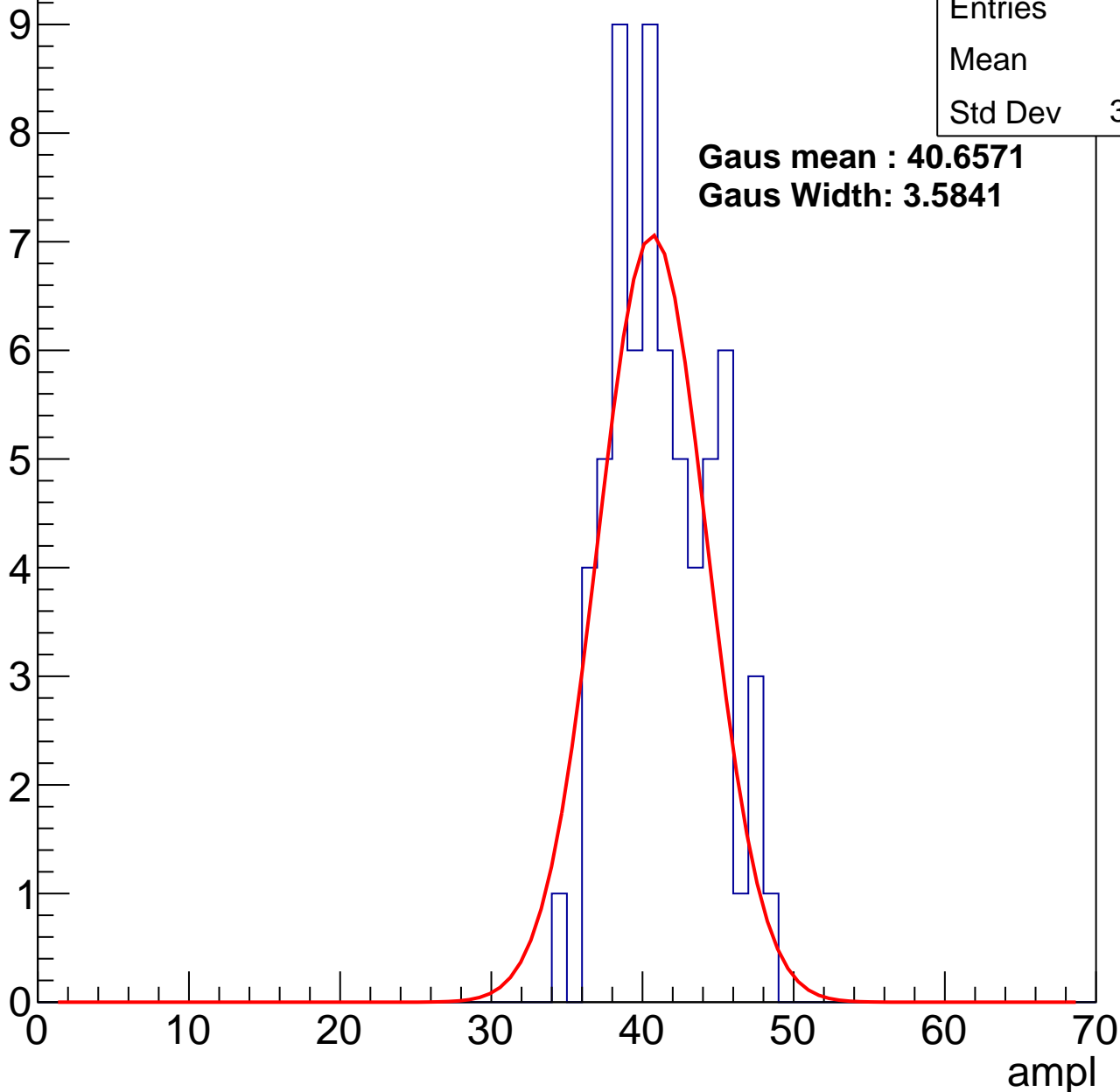
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	65
Mean	40.8
Std Dev	3.245

**Gaus mean : 40.6571**

**Gaus Width: 3.5841**

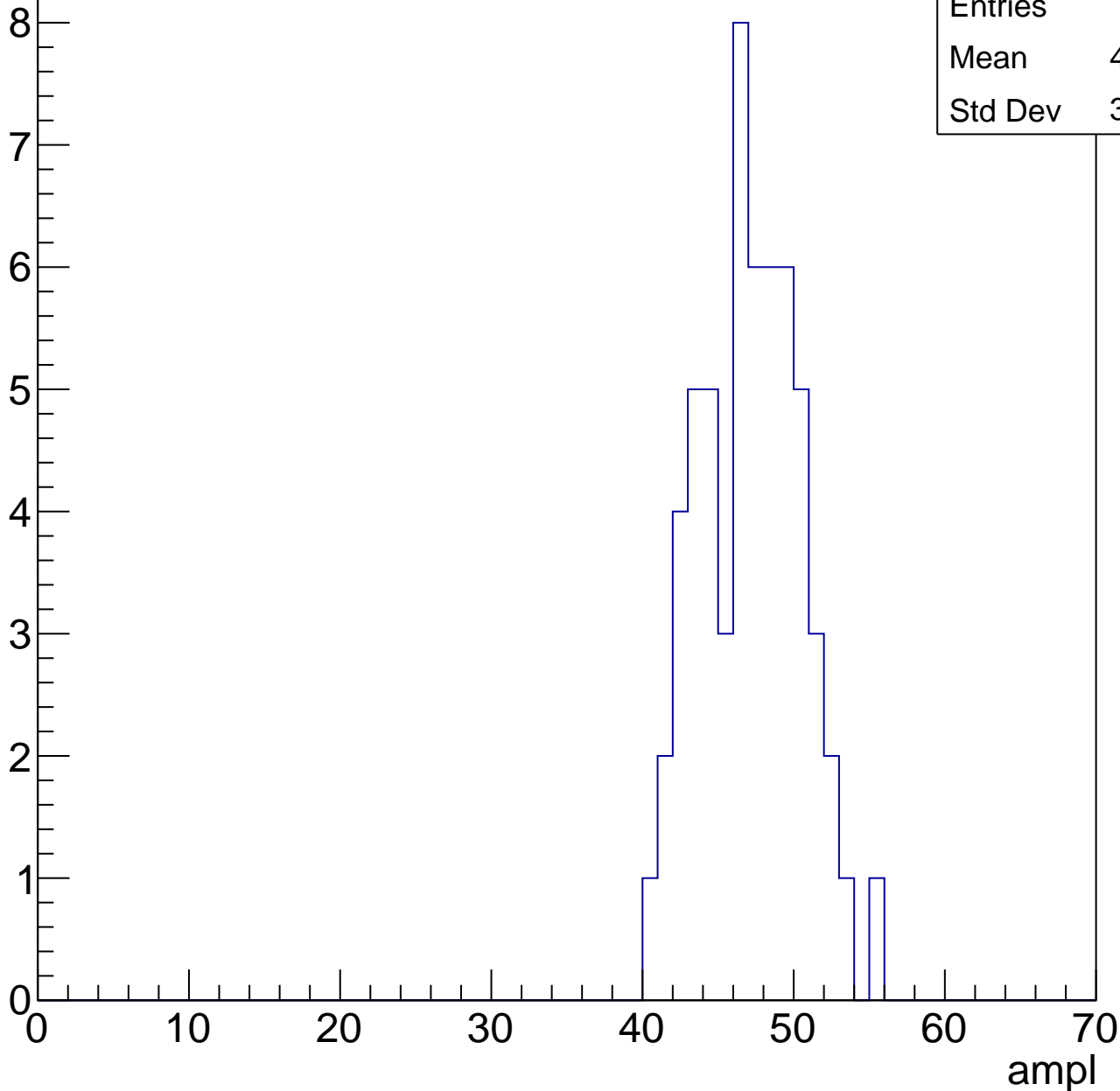


# B1L100S, U2-ch106, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

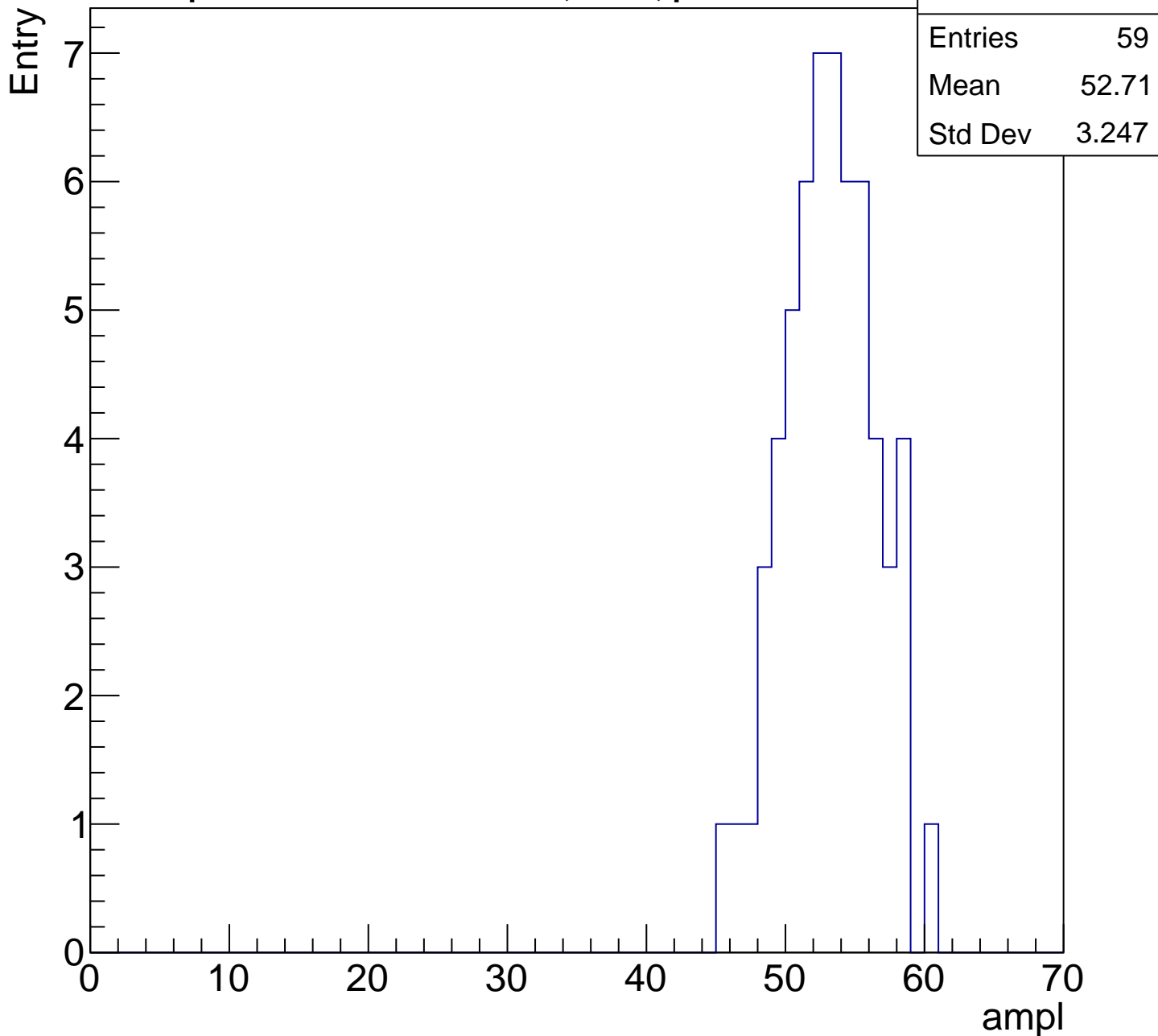
Entry

Entries	58
Mean	46.67
Std Dev	3.303



# B1L100S, U2-ch106, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

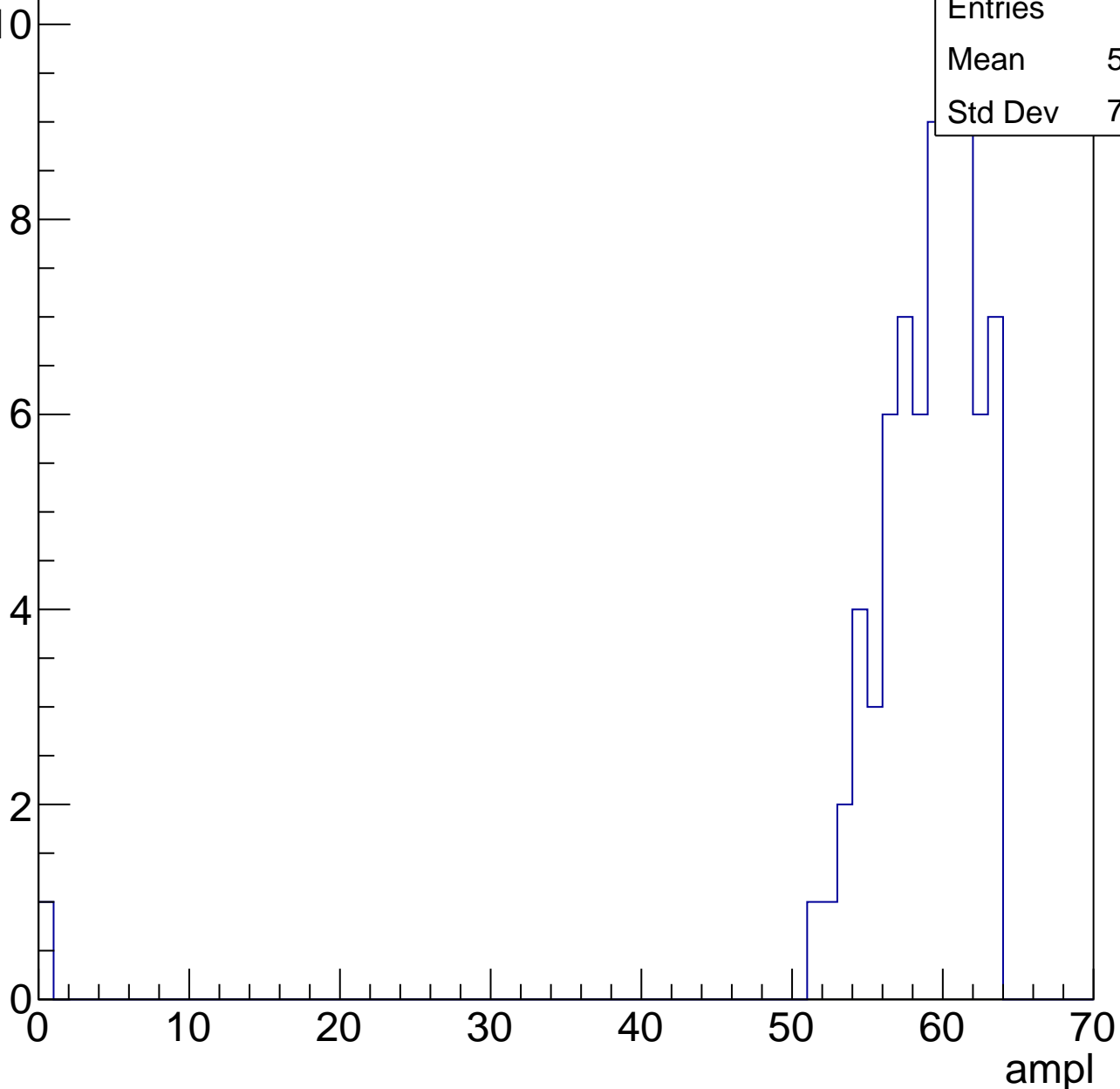


# B1L100S, U2-ch106, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

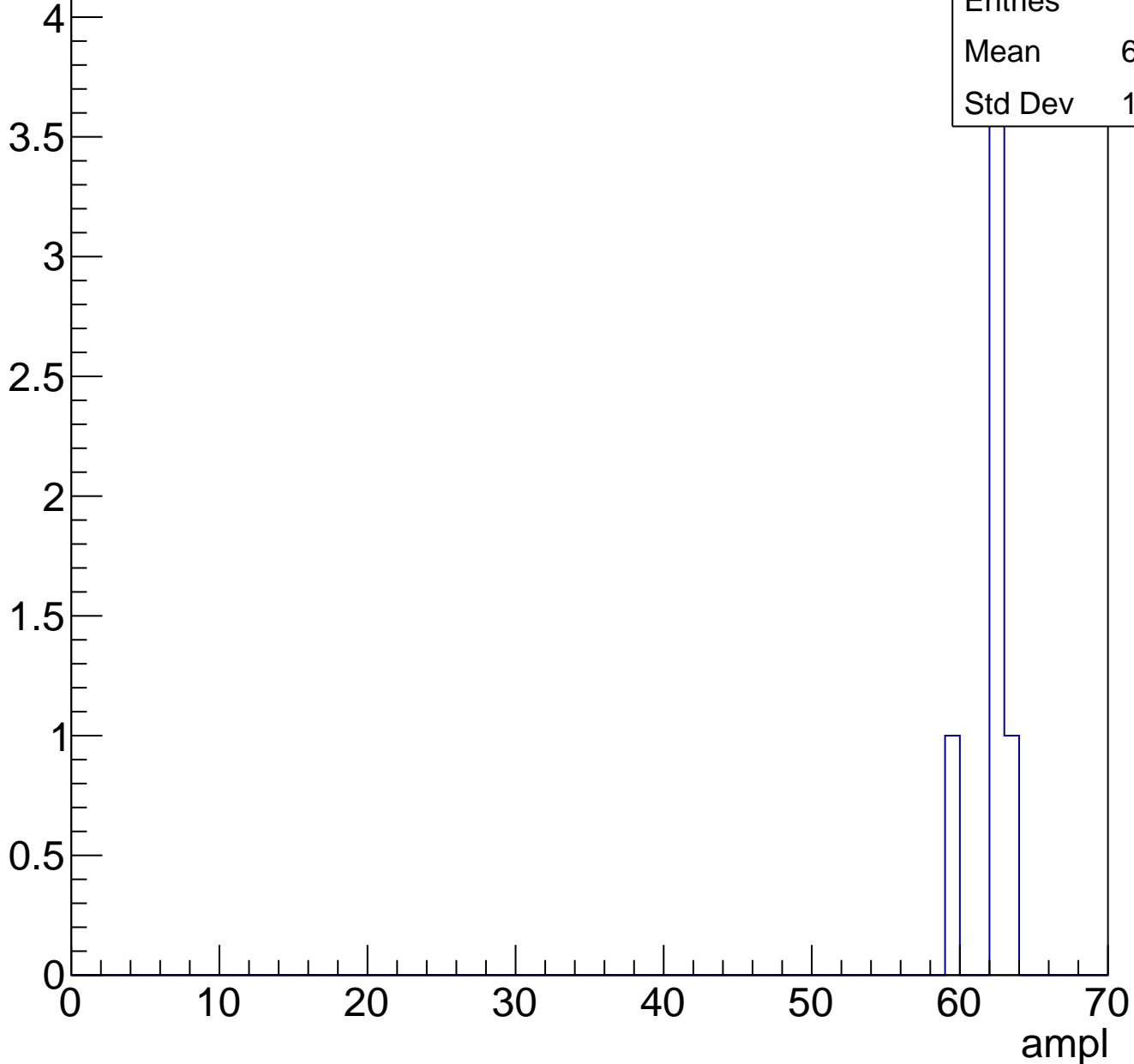
Entries	72
Mean	57.88
Std Dev	7.478



# B1L100S, U2-ch106, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

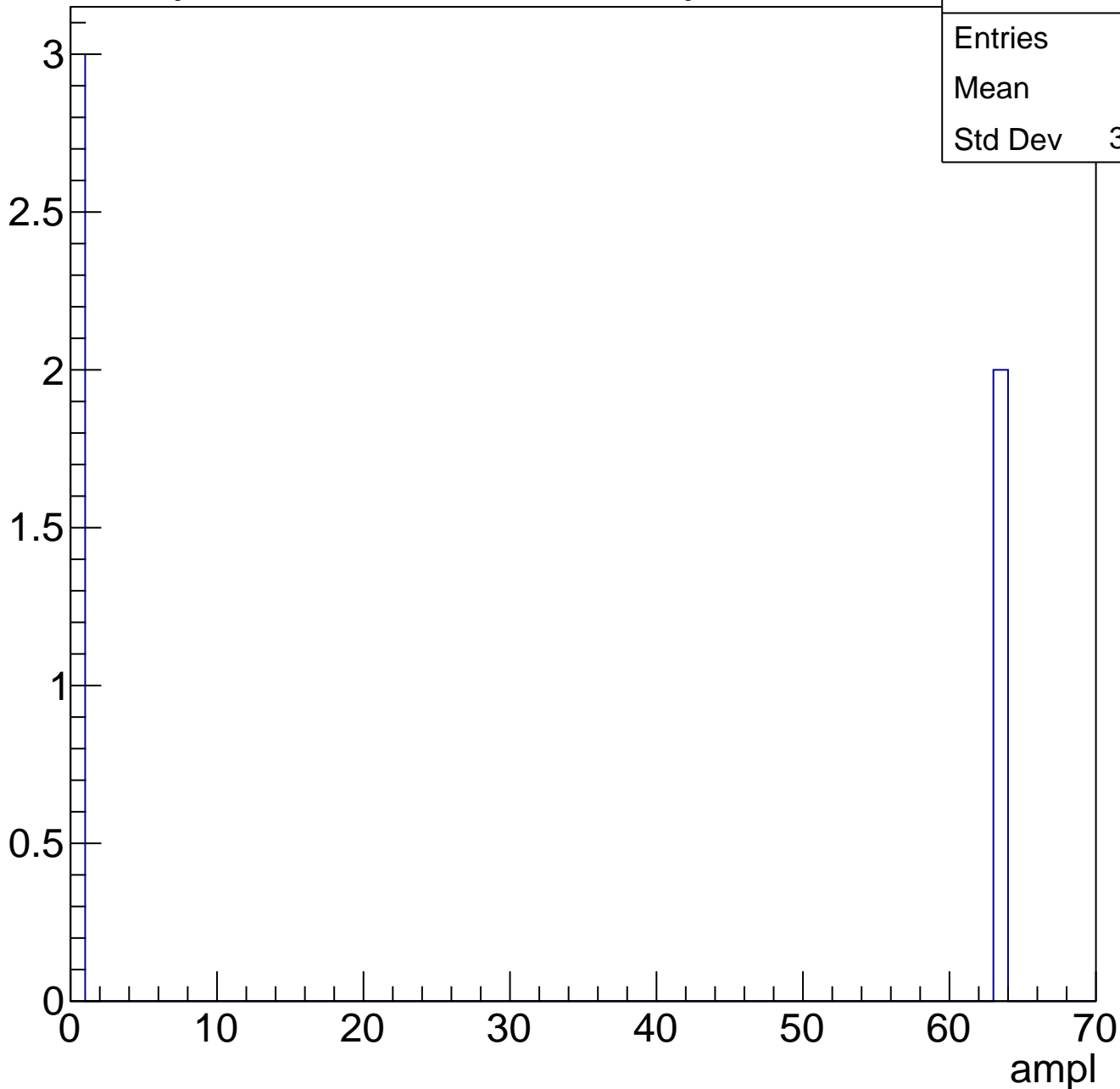




# B1L100S, U2-ch106, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



# B1L100S, U2-ch107, adc0

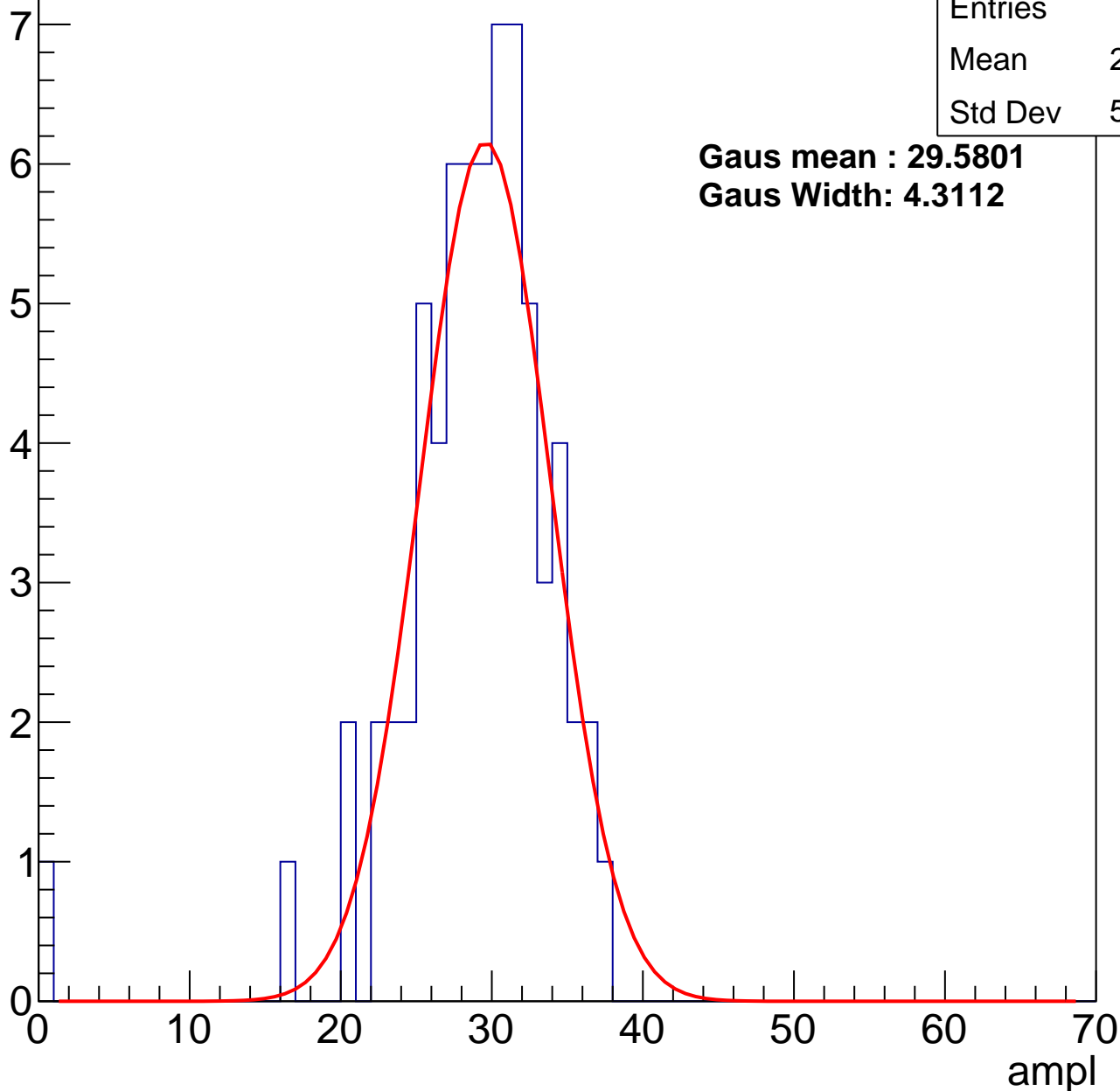
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	68
Mean	28.35
Std Dev	5.385

**Gaus mean : 29.5801**

**Gaus Width: 4.3112**



# B1L100S, U2-ch107, adc1

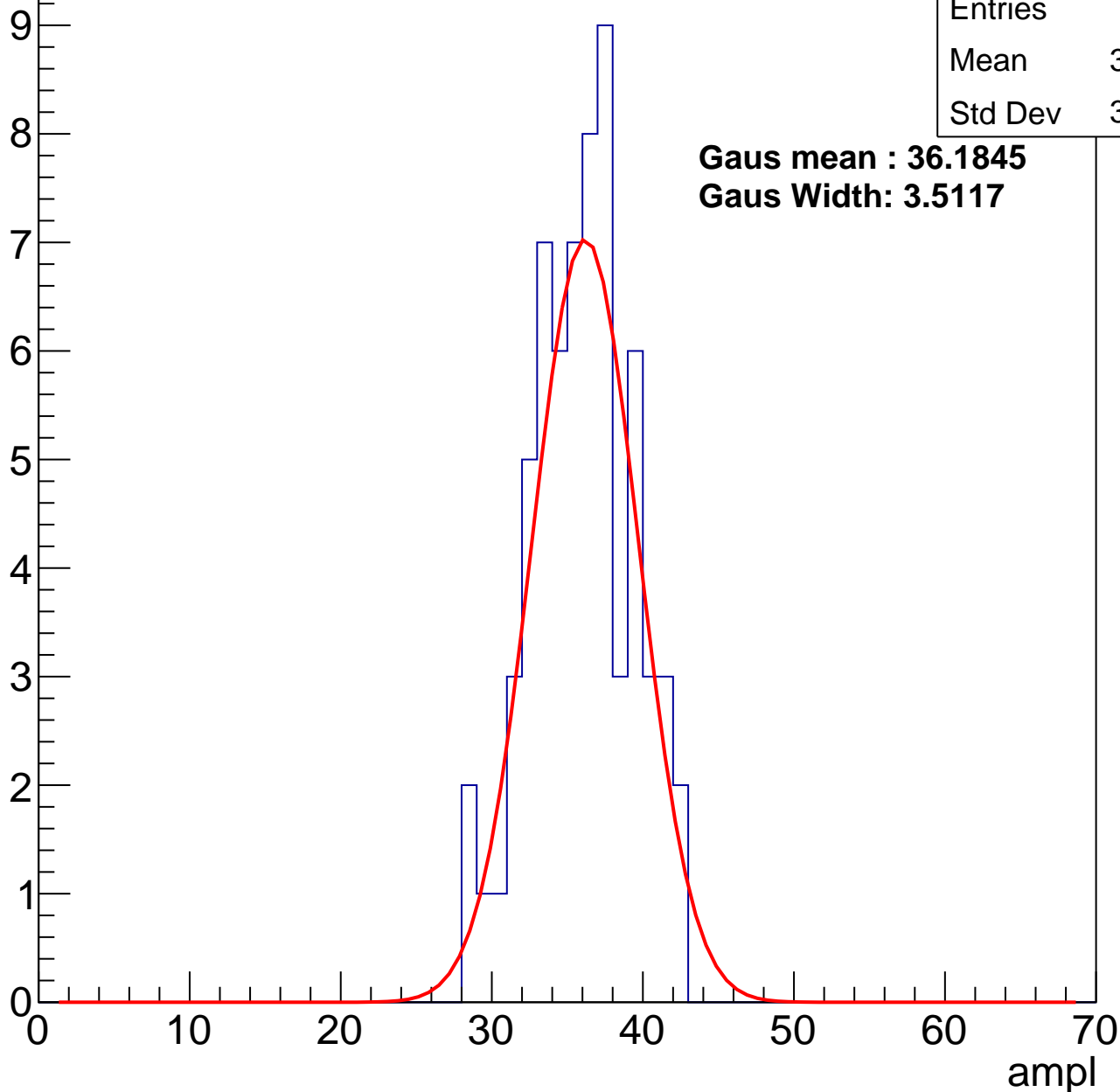
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	66
Mean	35.52
Std Dev	3.295

**Gaus mean : 36.1845**

**Gaus Width: 3.5117**



# B1L100S, U2-ch107, adc2

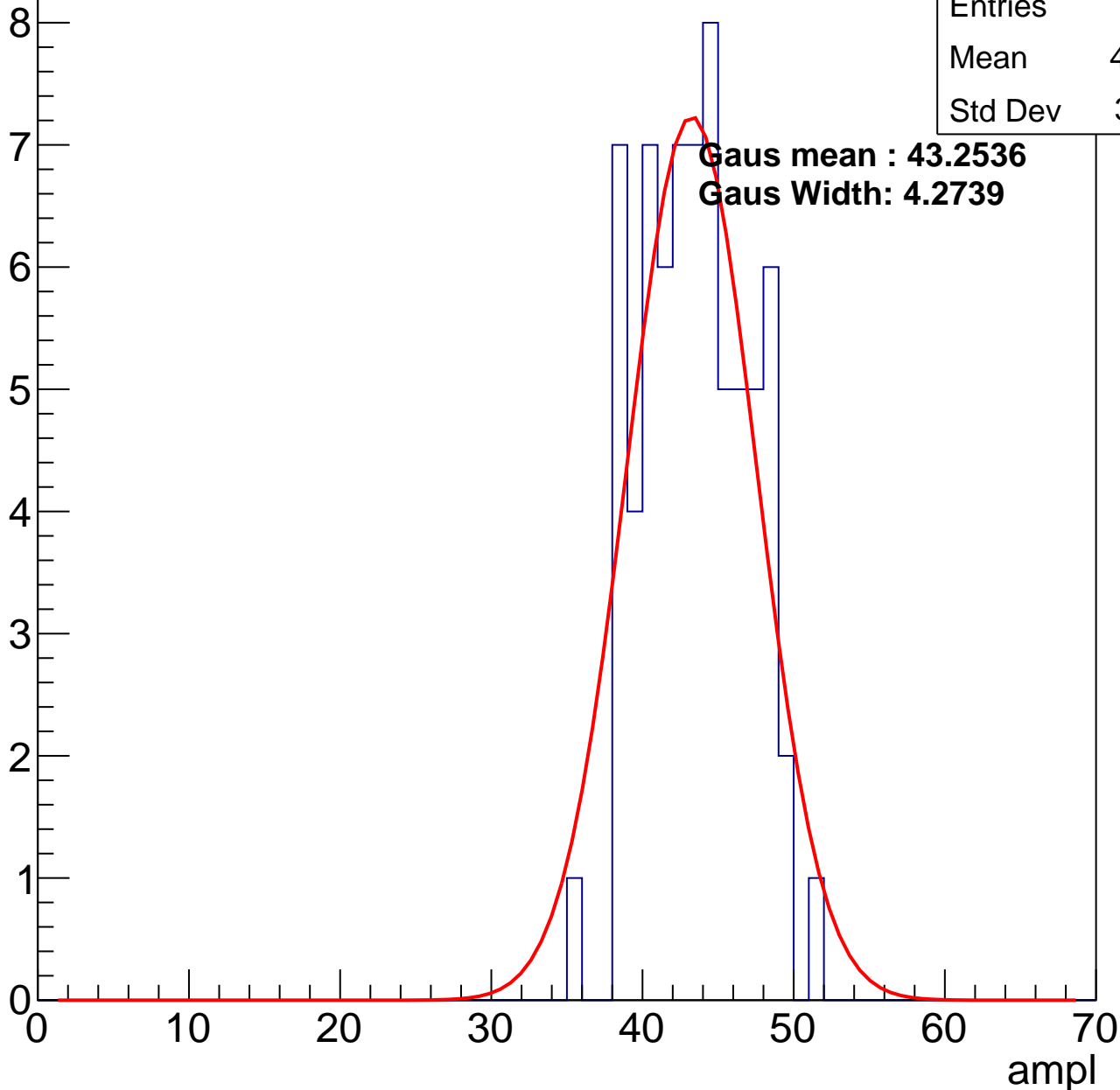
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	71
Mean	43.06
Std Dev	3.431

**Gaus mean : 43.2536**

**Gaus Width: 4.2739**

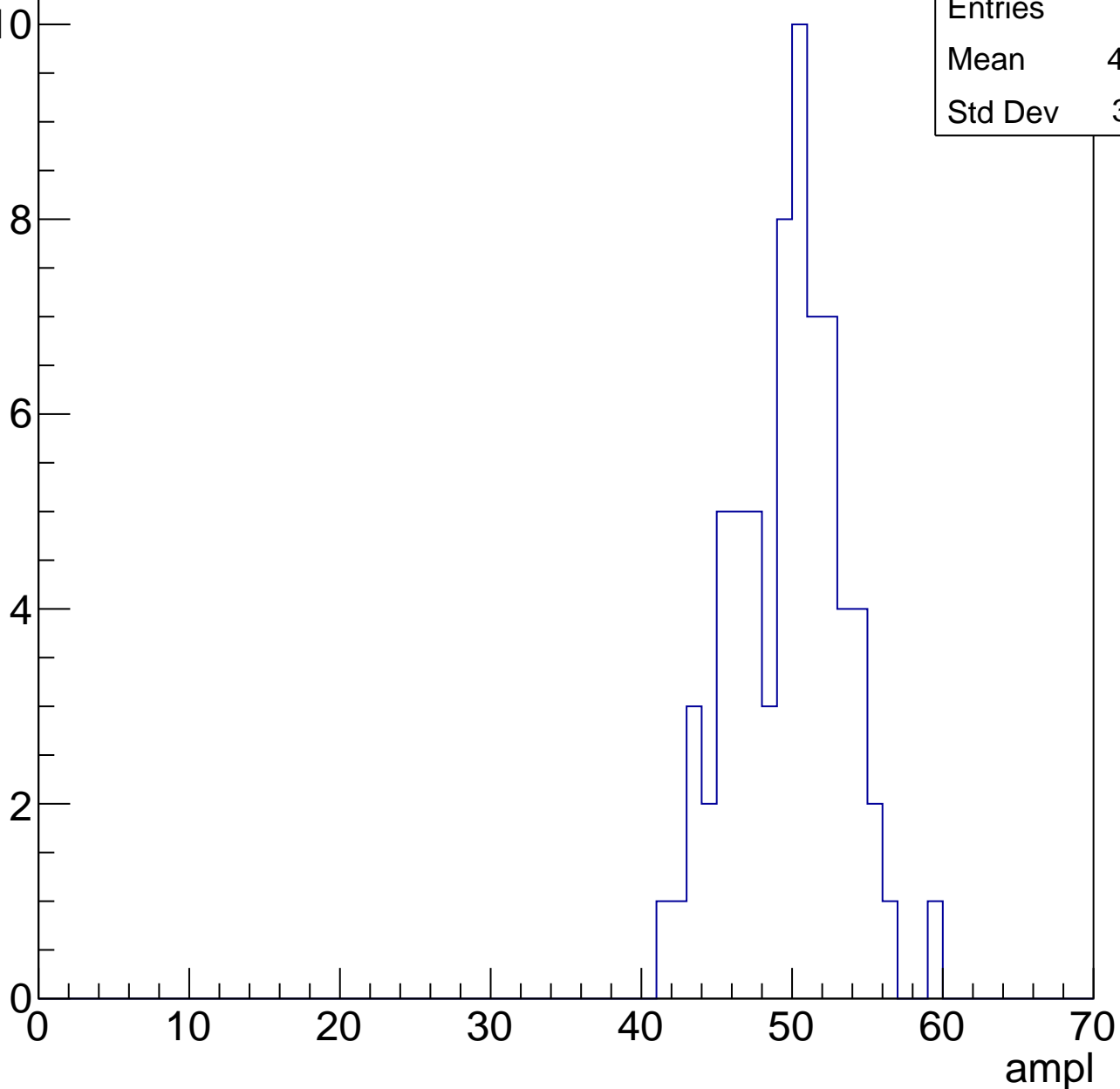


# B1L100S, U2-ch107, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	69
Mean	49.28
Std Dev	3.611

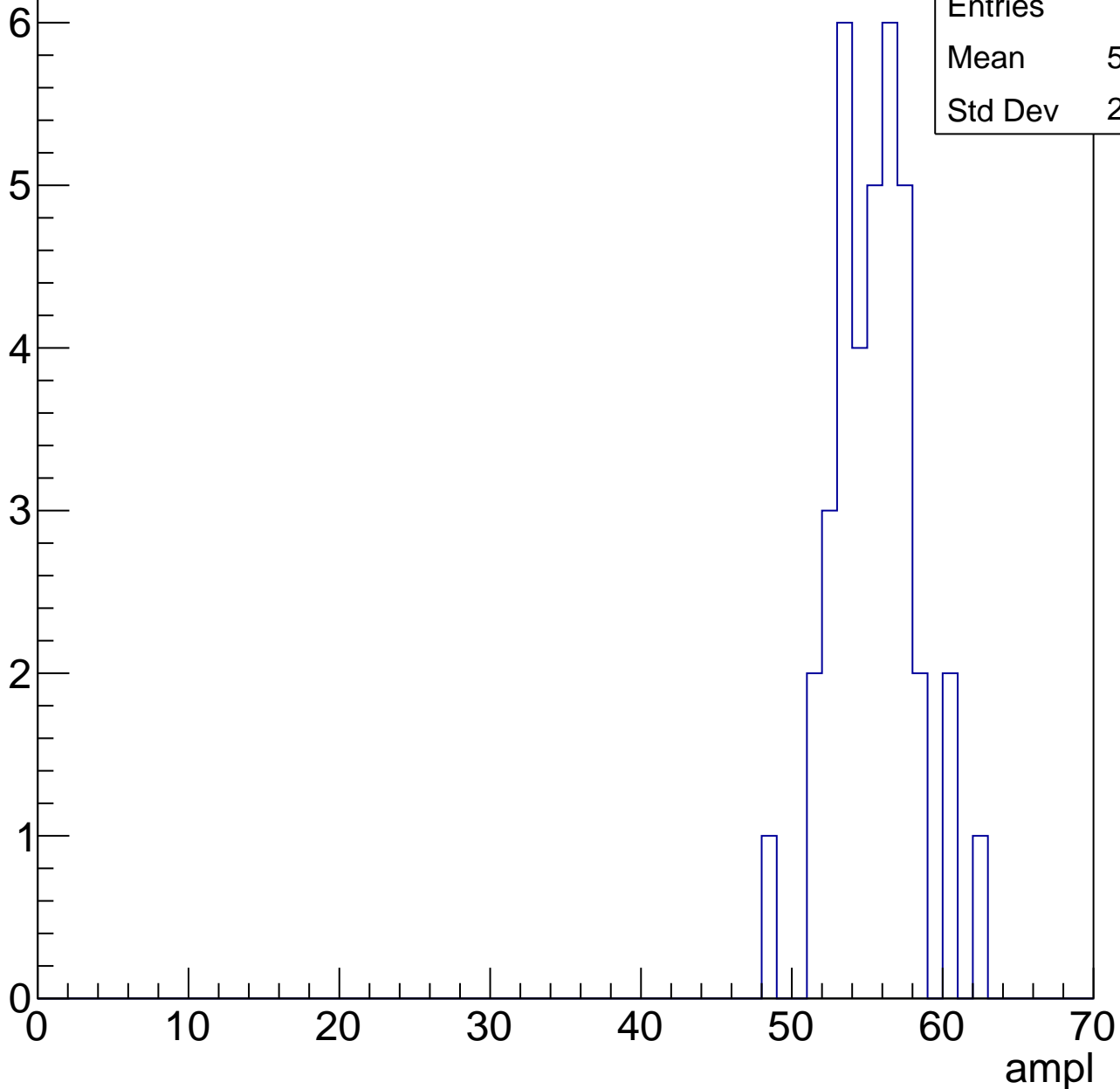


# B1L100S, U2-ch107, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	37
Mean	54.97
Std Dev	2.746



# B1L100S, U2-ch107, adc5

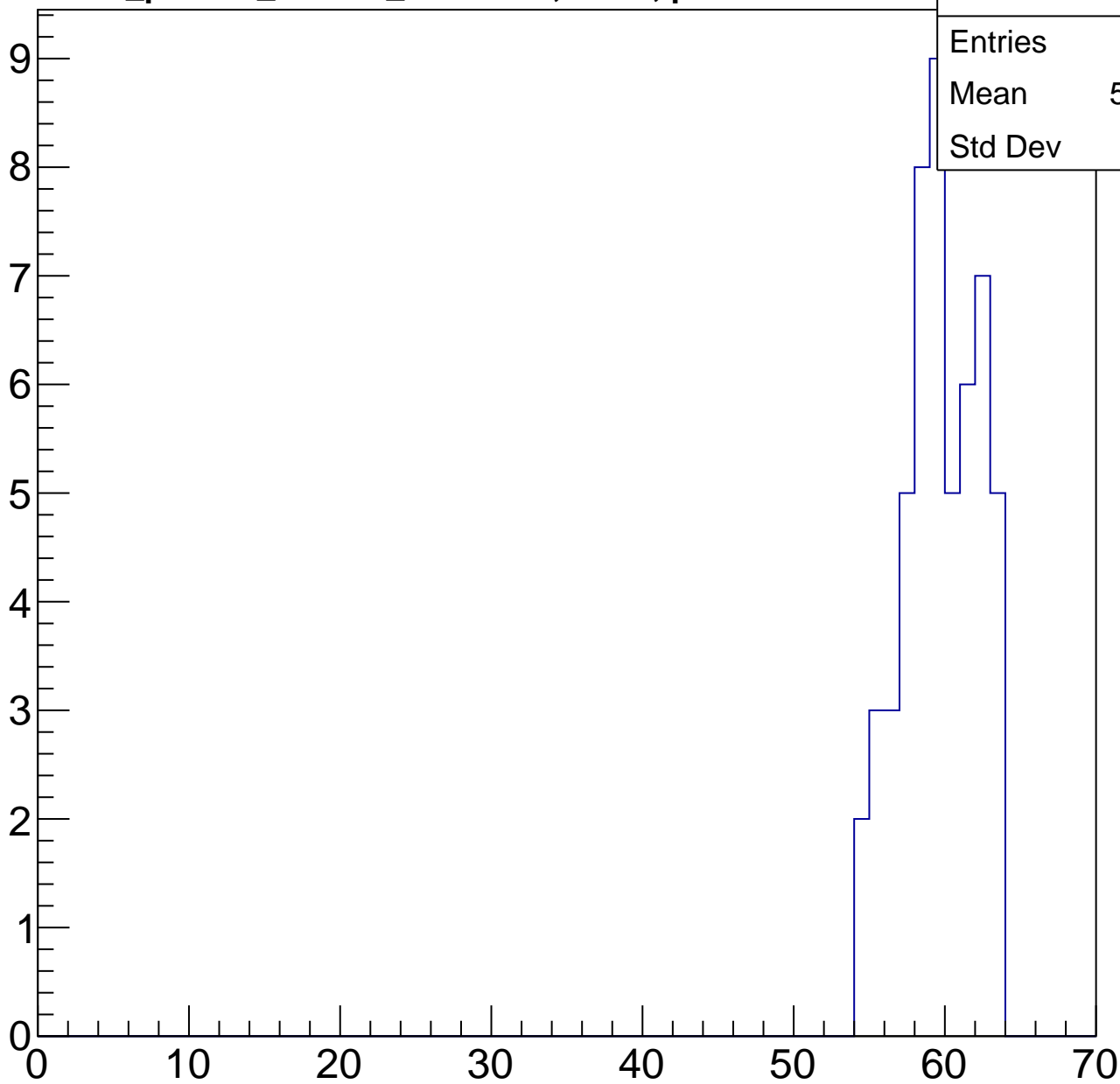
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	53
Mean	59.17
Std Dev	2.47

ampl

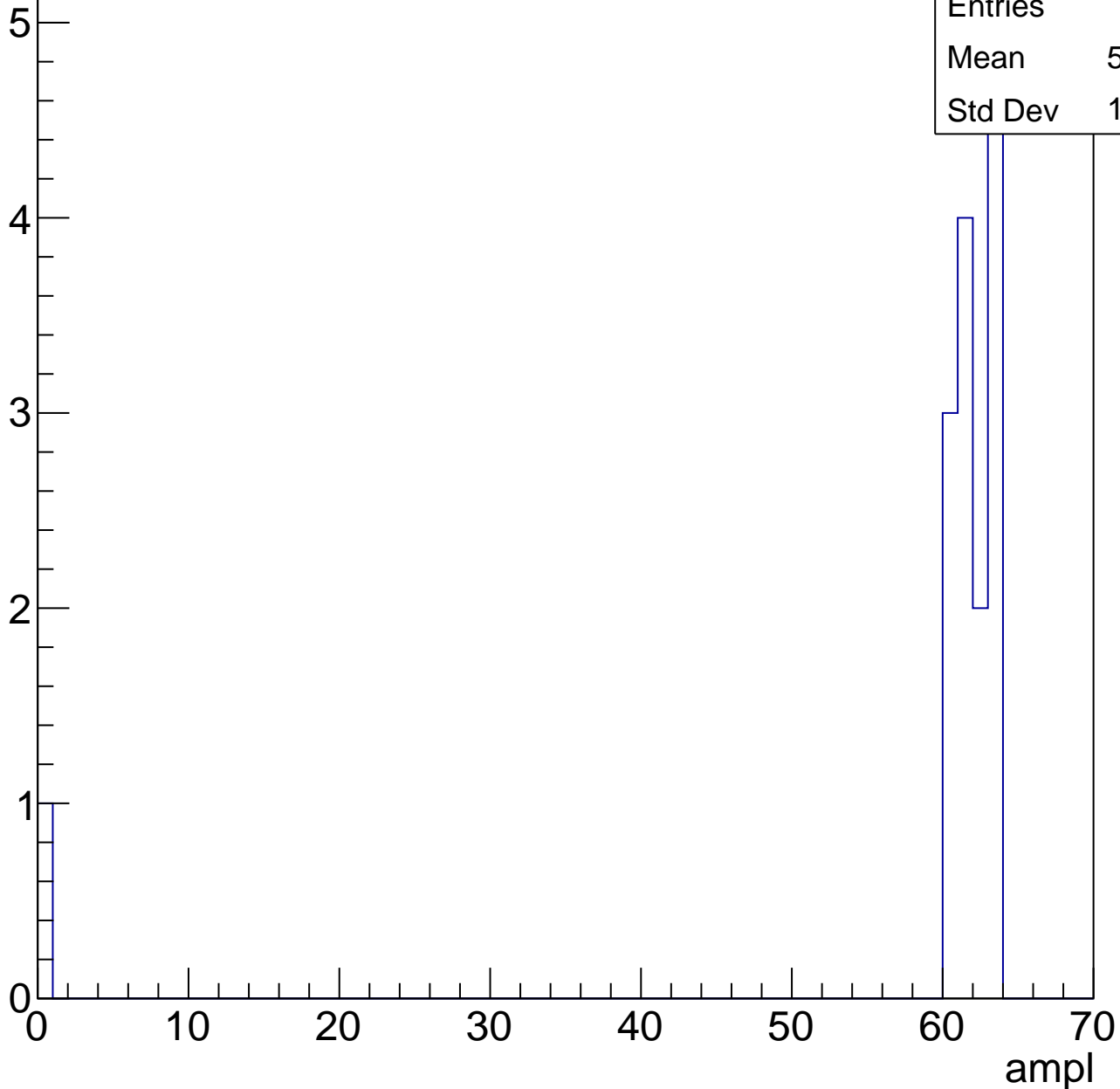


# B1L100S, U2-ch107, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	15
Mean	57.53
Std Dev	15.42





# B1L100S, U2-ch107, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	3
Mean	0
Std Dev	0

# B1L100S, U2-ch108, adc0

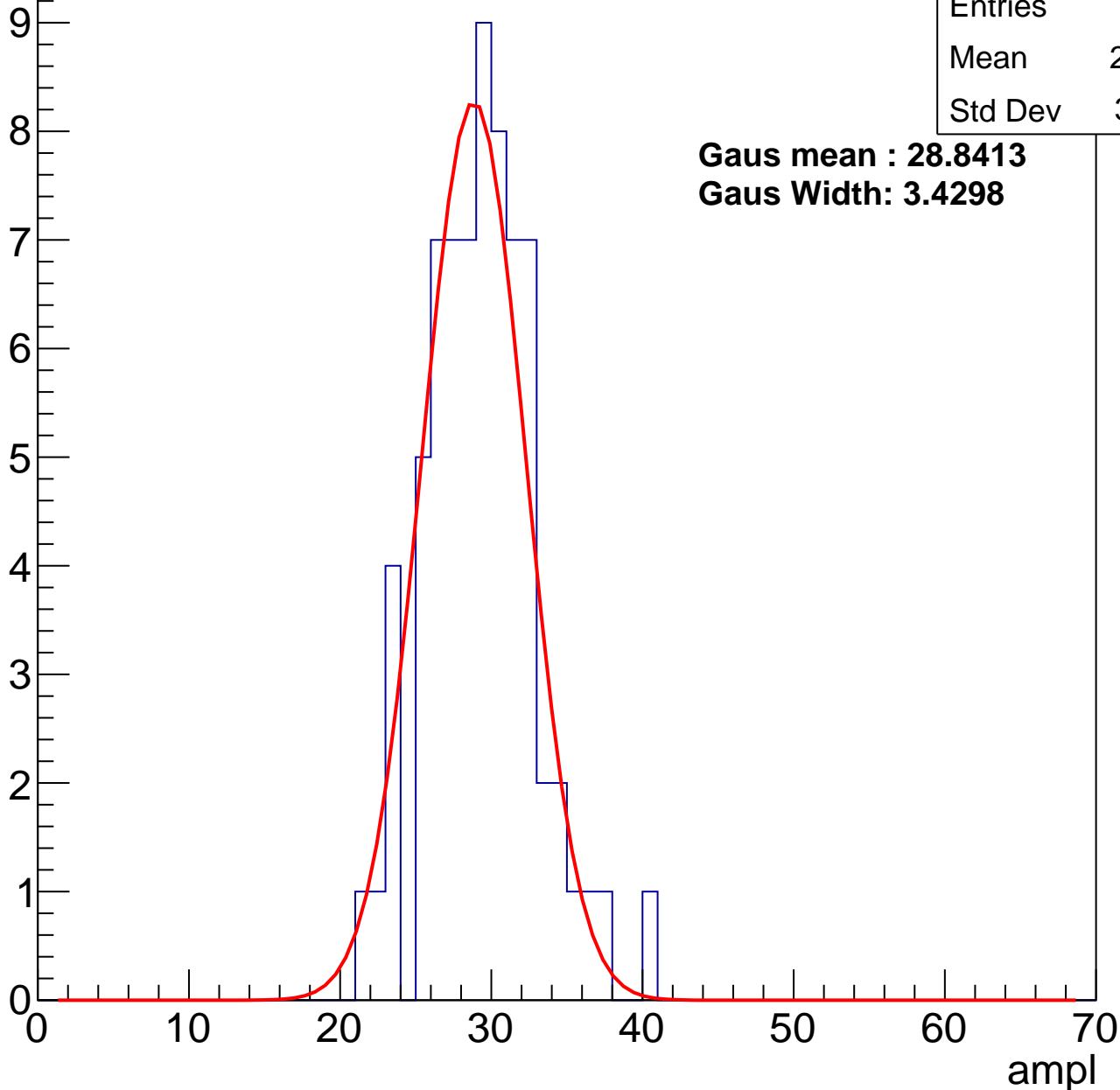
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	71
Mean	28.89
Std Dev	3.531

**Gaus mean : 28.8413**

**Gaus Width: 3.4298**



# B1L100S, U2-ch108, adc1

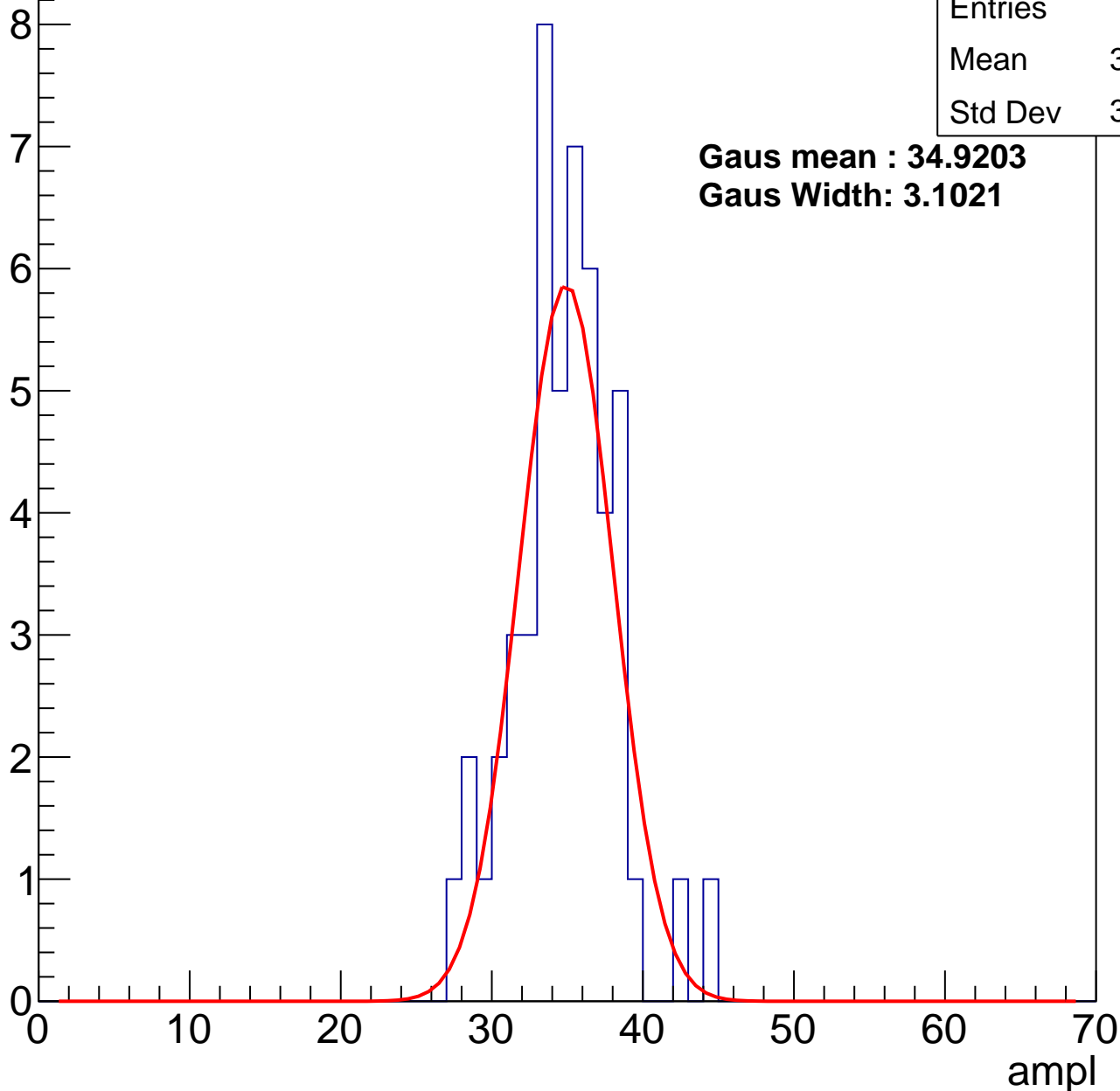
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	50
Mean	34.38
Std Dev	3.328

**Gaus mean : 34.9203**

**Gaus Width: 3.1021**



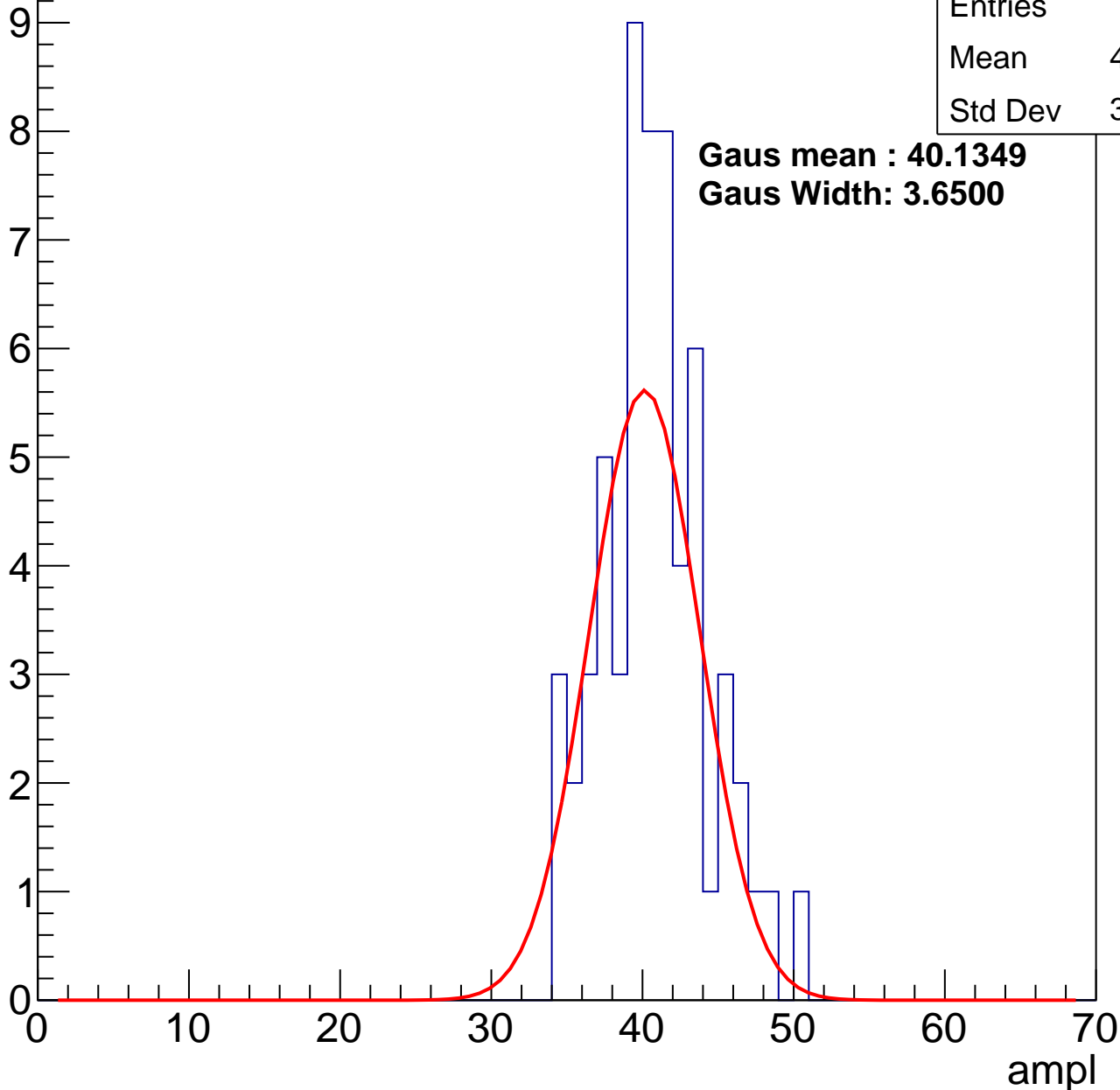
# B1L100S, U2-ch108, adc2

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	60
Mean	40.33
Std Dev	3.462

**Gaus mean : 40.1349**  
**Gaus Width: 3.6500**

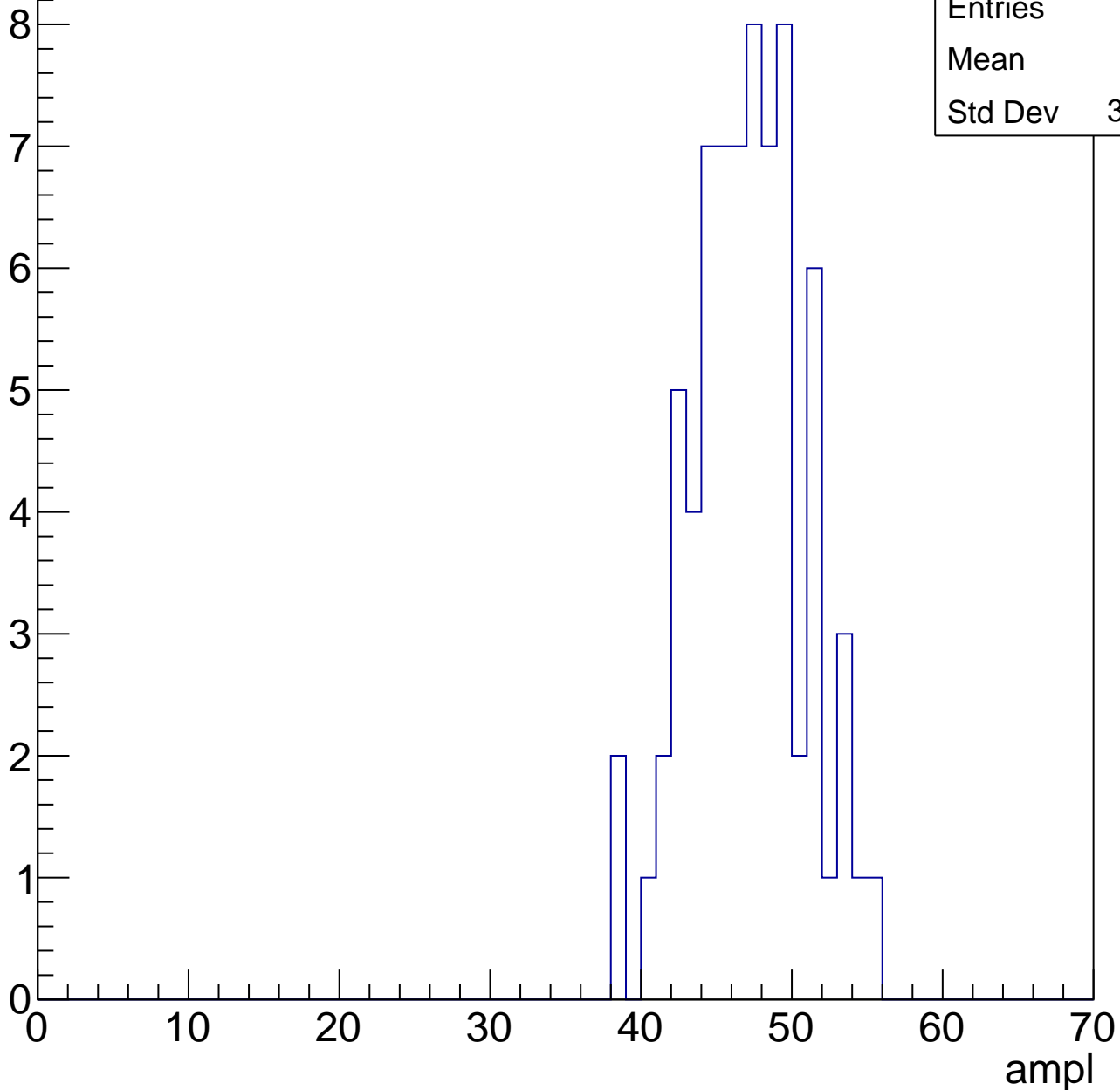


# B1L100S, U2-ch108, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	72
Mean	46.6
Std Dev	3.646

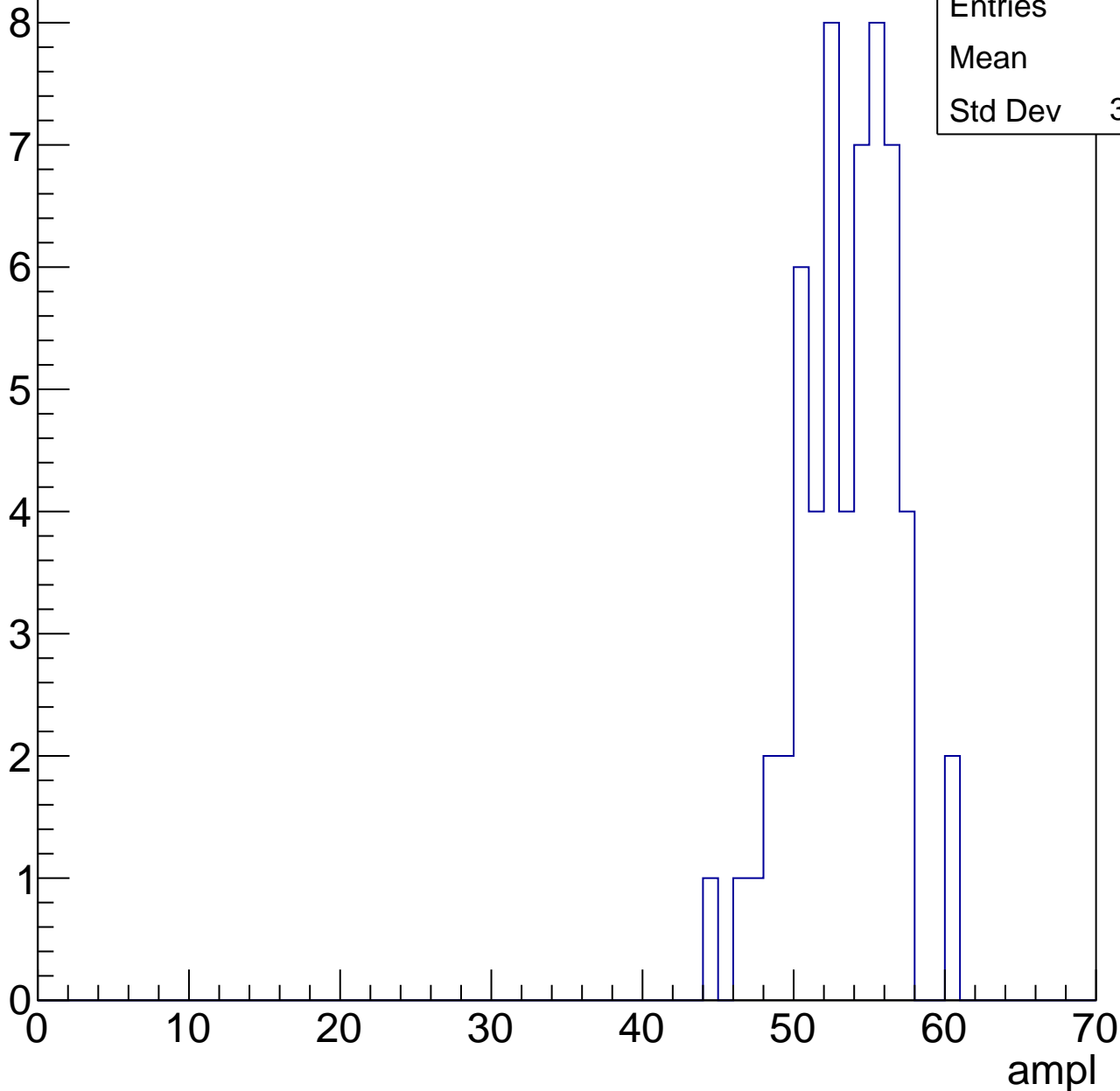


# B1L100S, U2-ch108, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	57
Mean	53
Std Dev	3.217

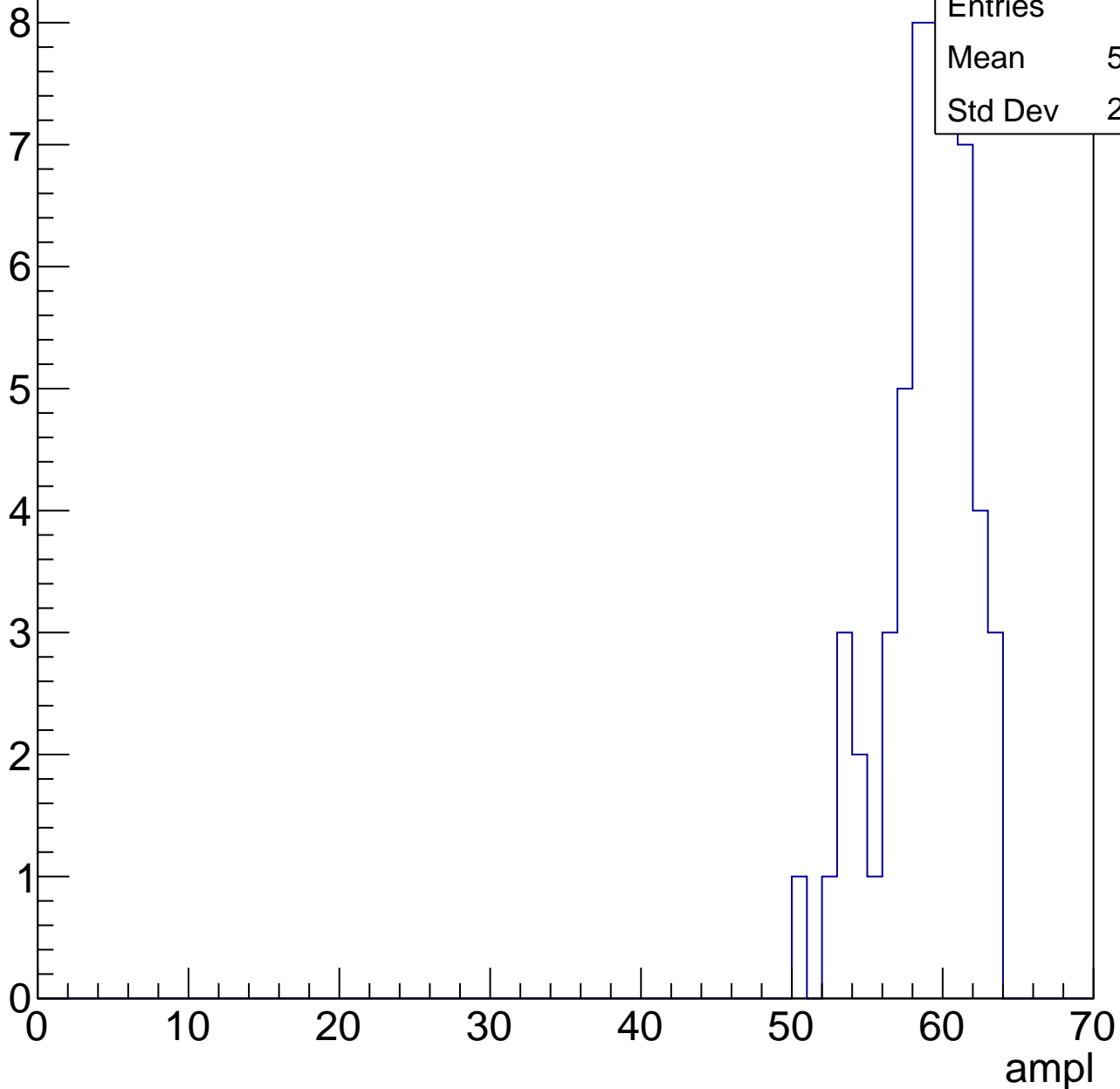


# B1L100S, U2-ch108, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	54
Mean	58.46
Std Dev	2.929

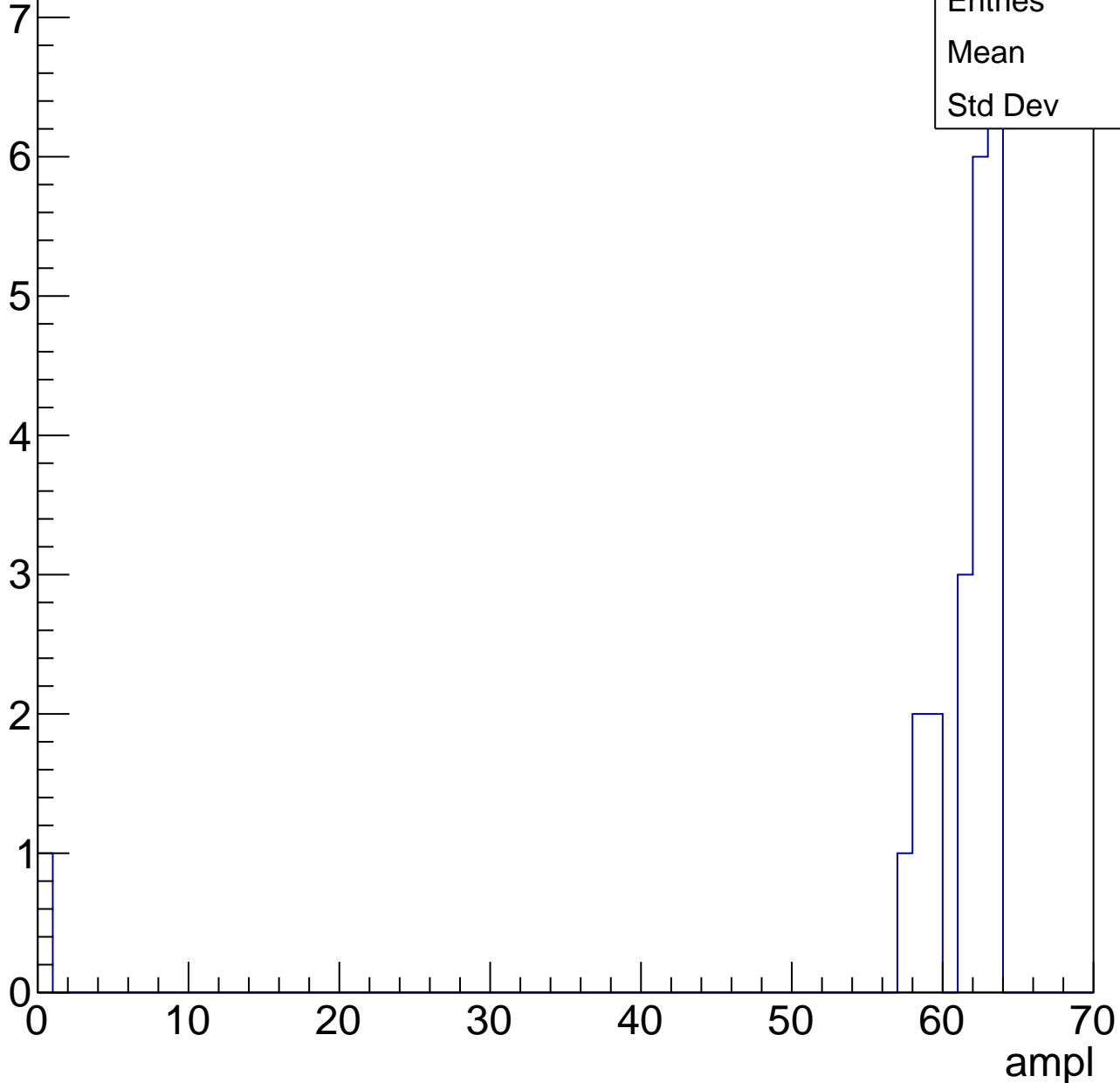


# B1L100S, U2-ch108, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	22
Mean	58.5
Std Dev	12.9





# B1L100S, U2-ch108, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L100S, U2-ch109, adc0

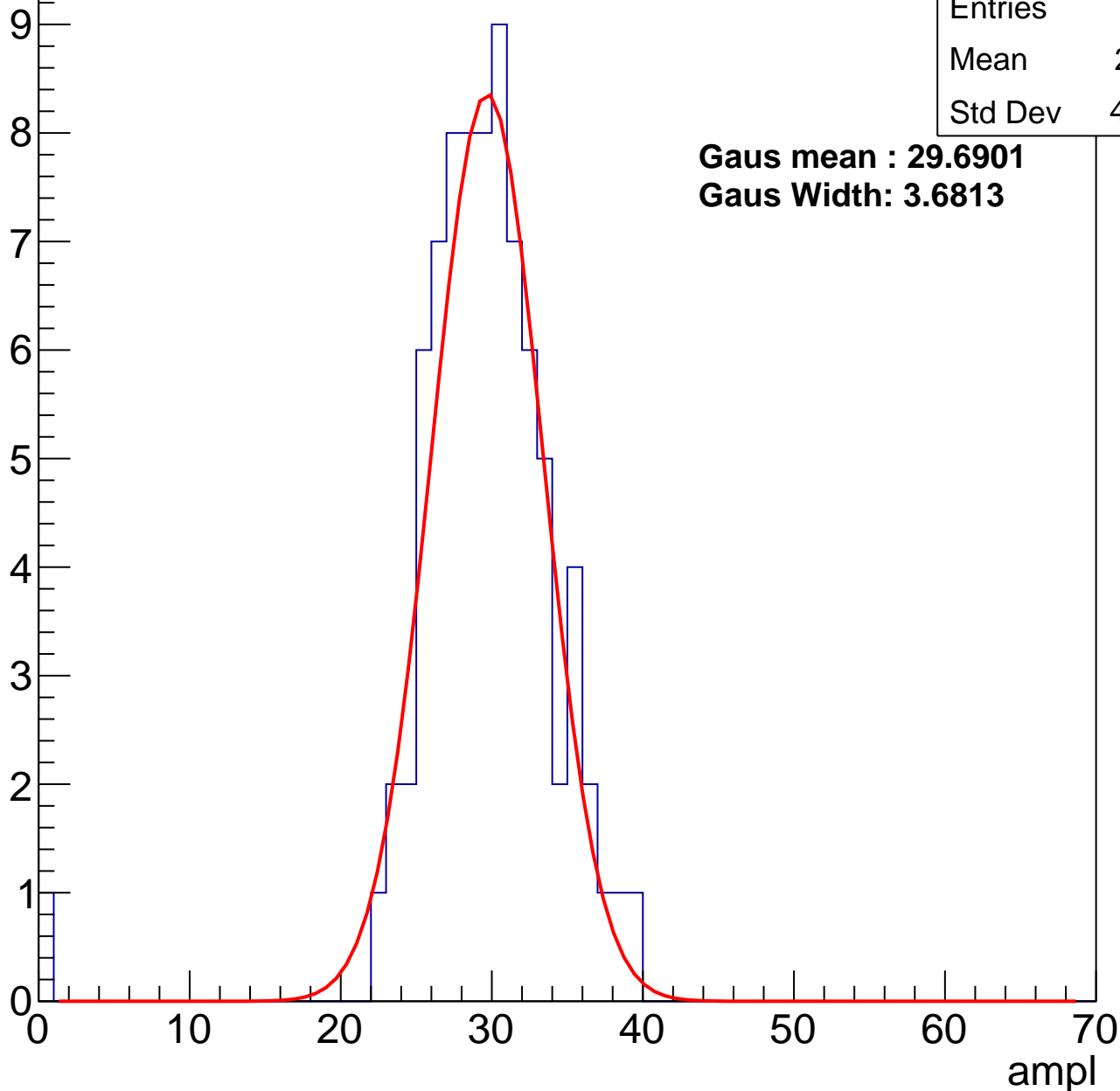
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	81
Mean	29.11
Std Dev	4.866

**Gaus mean : 29.6901**

**Gaus Width: 3.6813**



# B1L100S, U2-ch109, adc1

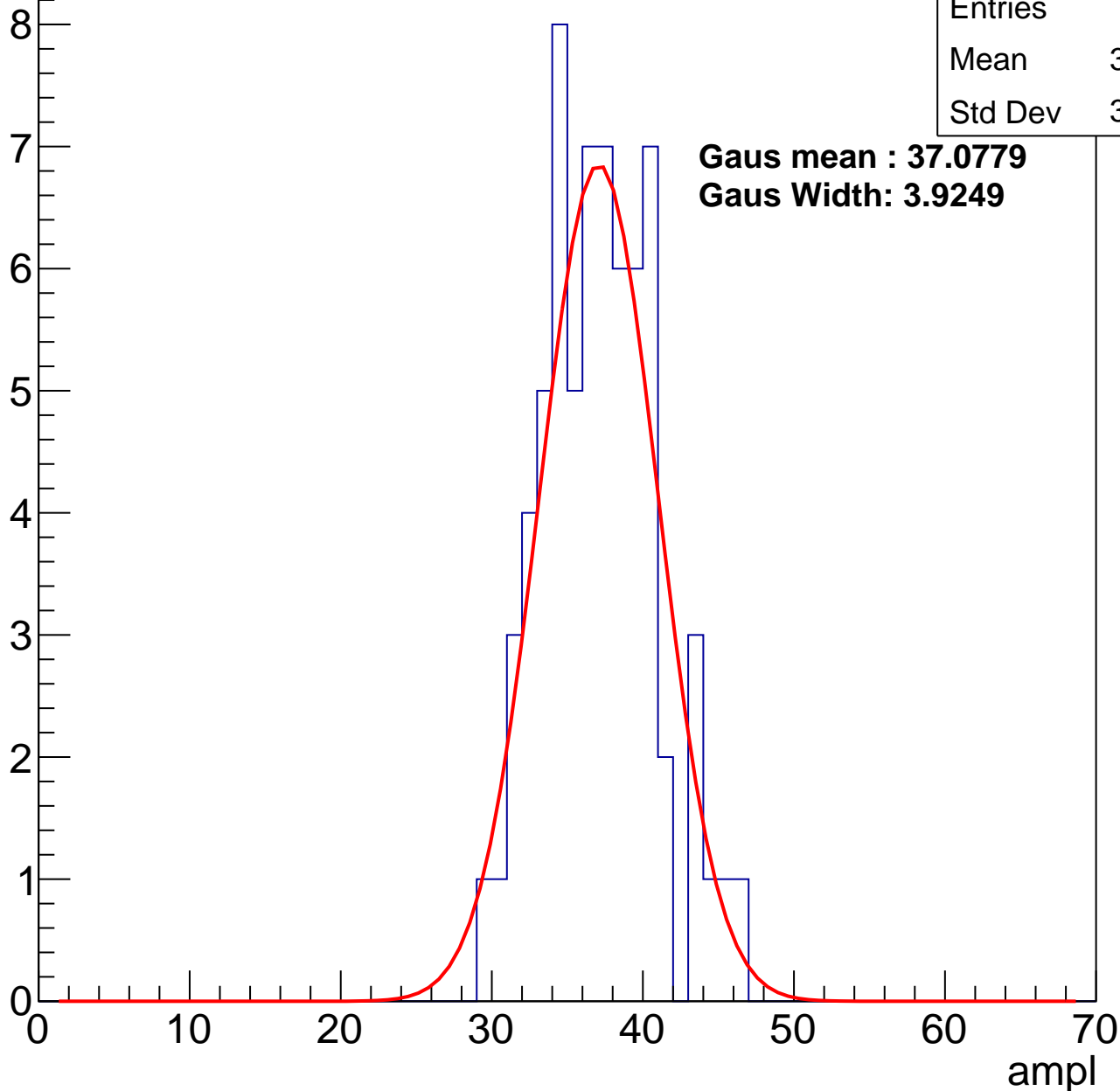
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	68
Mean	36.63
Std Dev	3.674

**Gaus mean : 37.0779**

**Gaus Width: 3.9249**



# B1L100S, U2-ch109, adc2

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	69
Mean	43.23
Std Dev	3.452

**Gaus mean : 43.9076**

**Gaus Width: 3.9244**

10

8

6

4

2

0

0

10

20

30

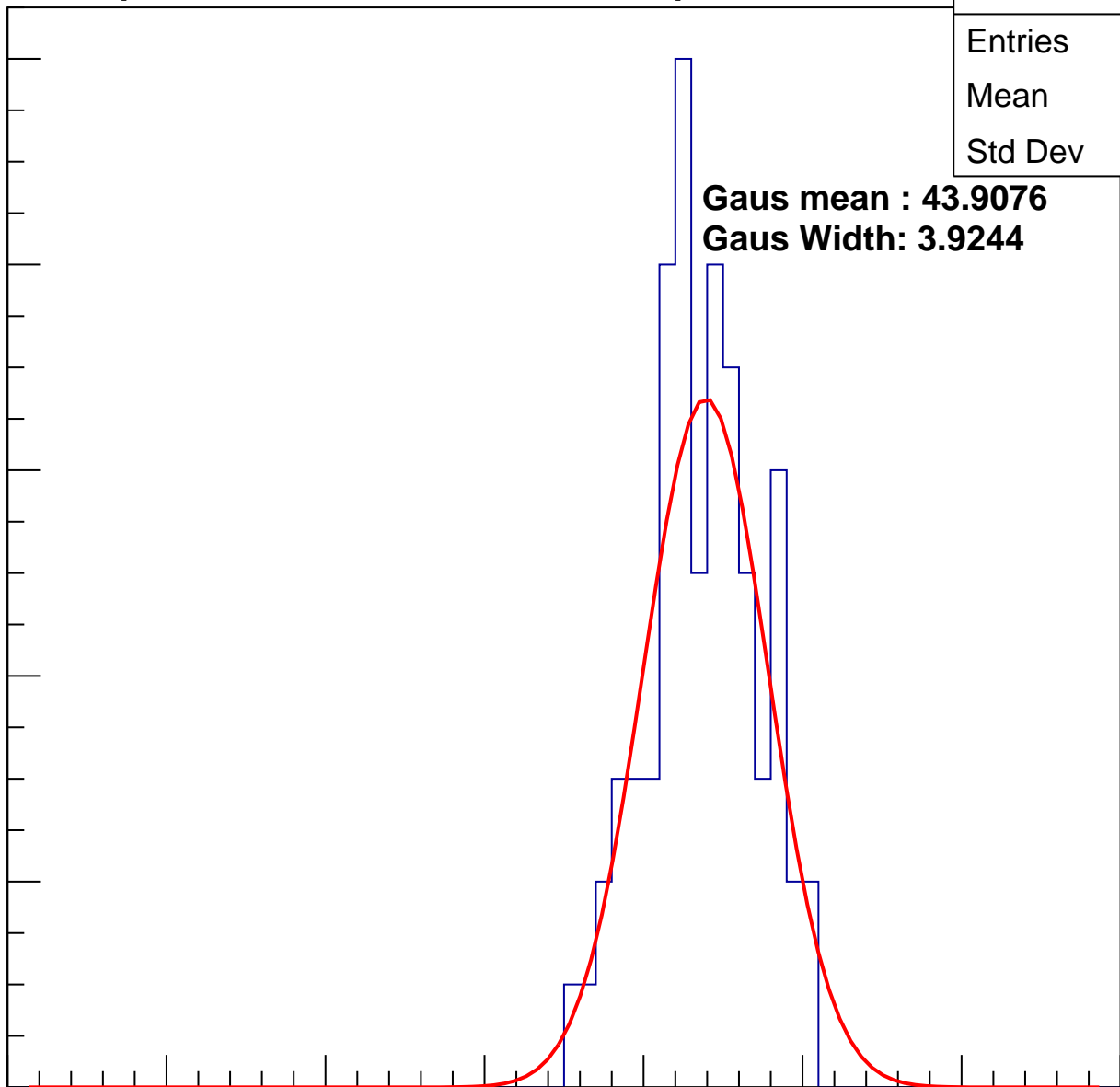
40

50

60

70

ampl

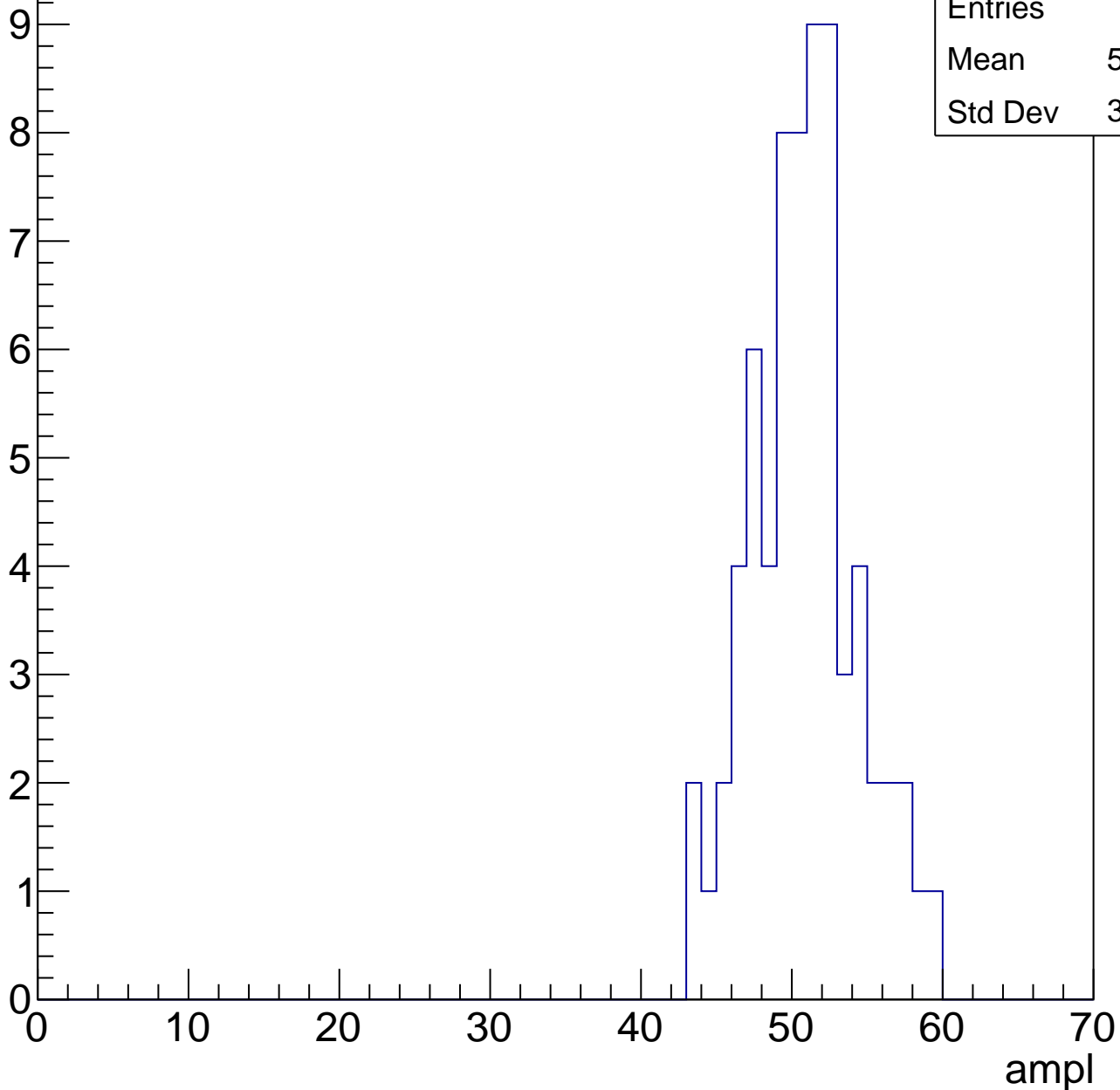


# B1L100S, U2-ch109, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	68
Mean	50.37
Std Dev	3.468

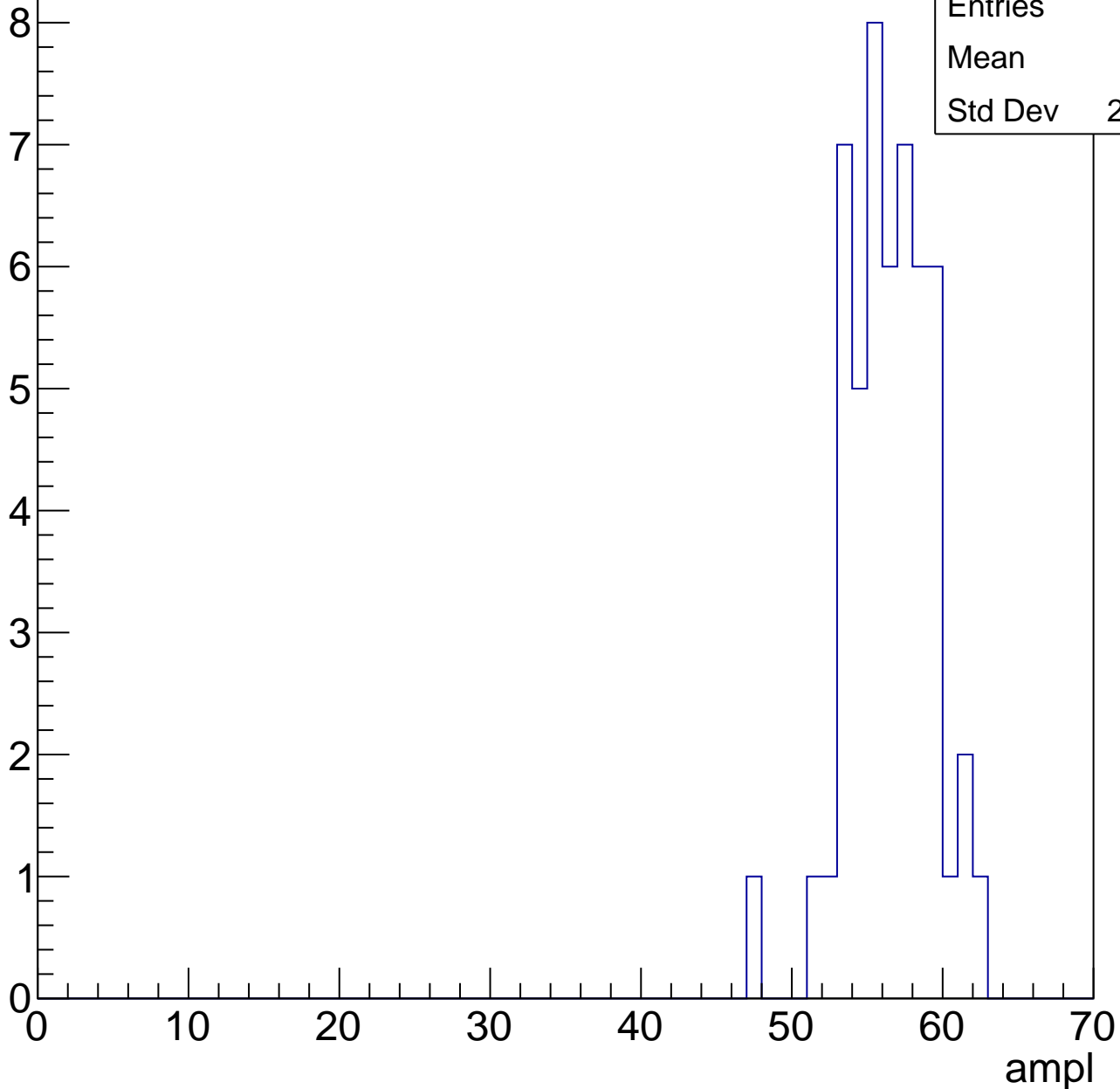


# B1L100S, U2-ch109, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	52
Mean	56
Std Dev	2.774



# B1L100S, U2-ch109, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

10

8

6

4

2

0

0

10

20

30

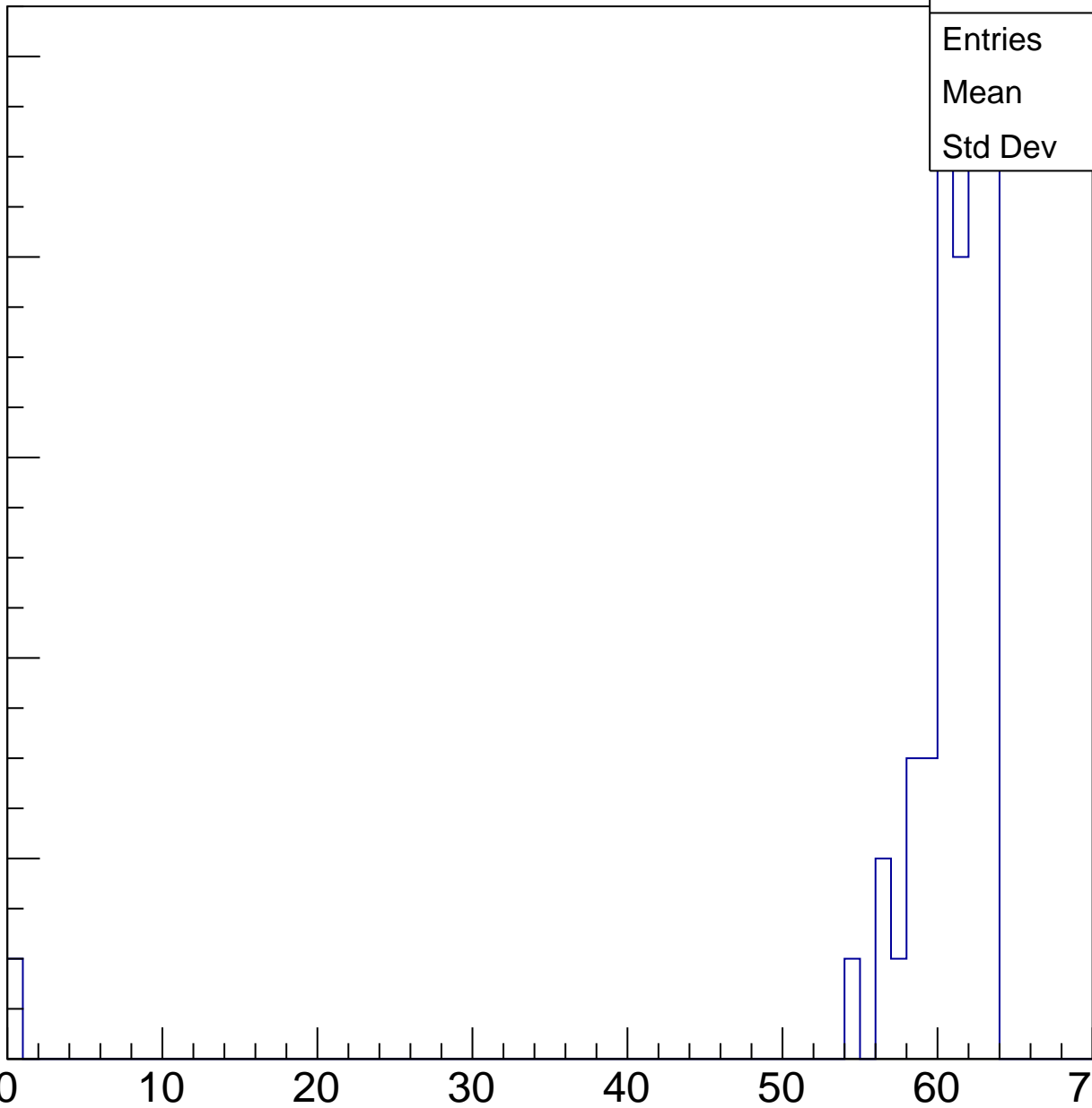
40

50

60

ampl

Entries	47
Mean	59.36
Std Dev	9



# B1L100S, U2-ch109, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	0
Mean	0
Std Dev	0



# B1L100S, U2-ch109, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L100S, U2-ch110, adc0

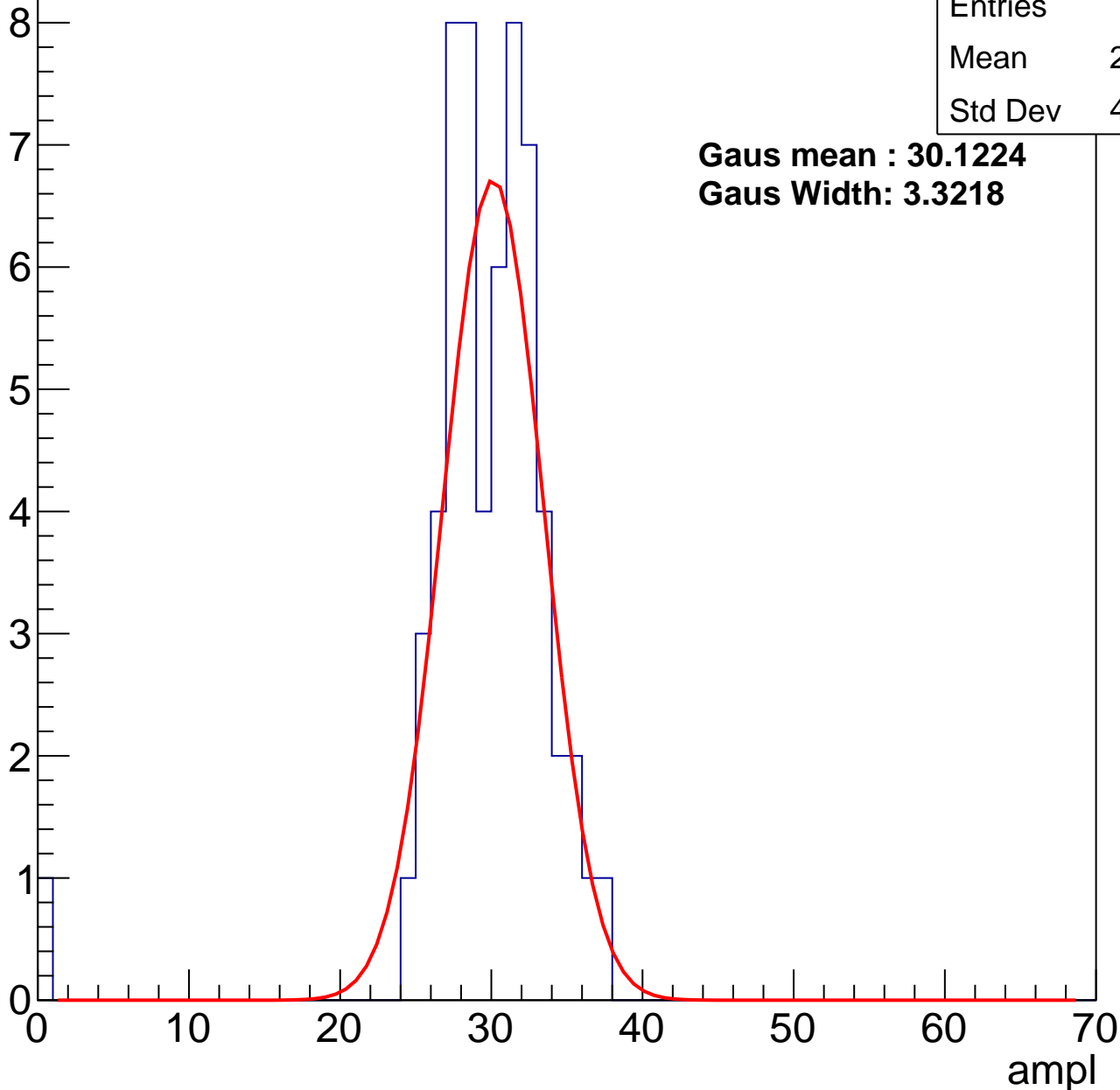
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	60
Mean	29.23
Std Dev	4.808

**Gaus mean : 30.1224**

**Gaus Width: 3.3218**



# B1L100S, U2-ch110, adc1

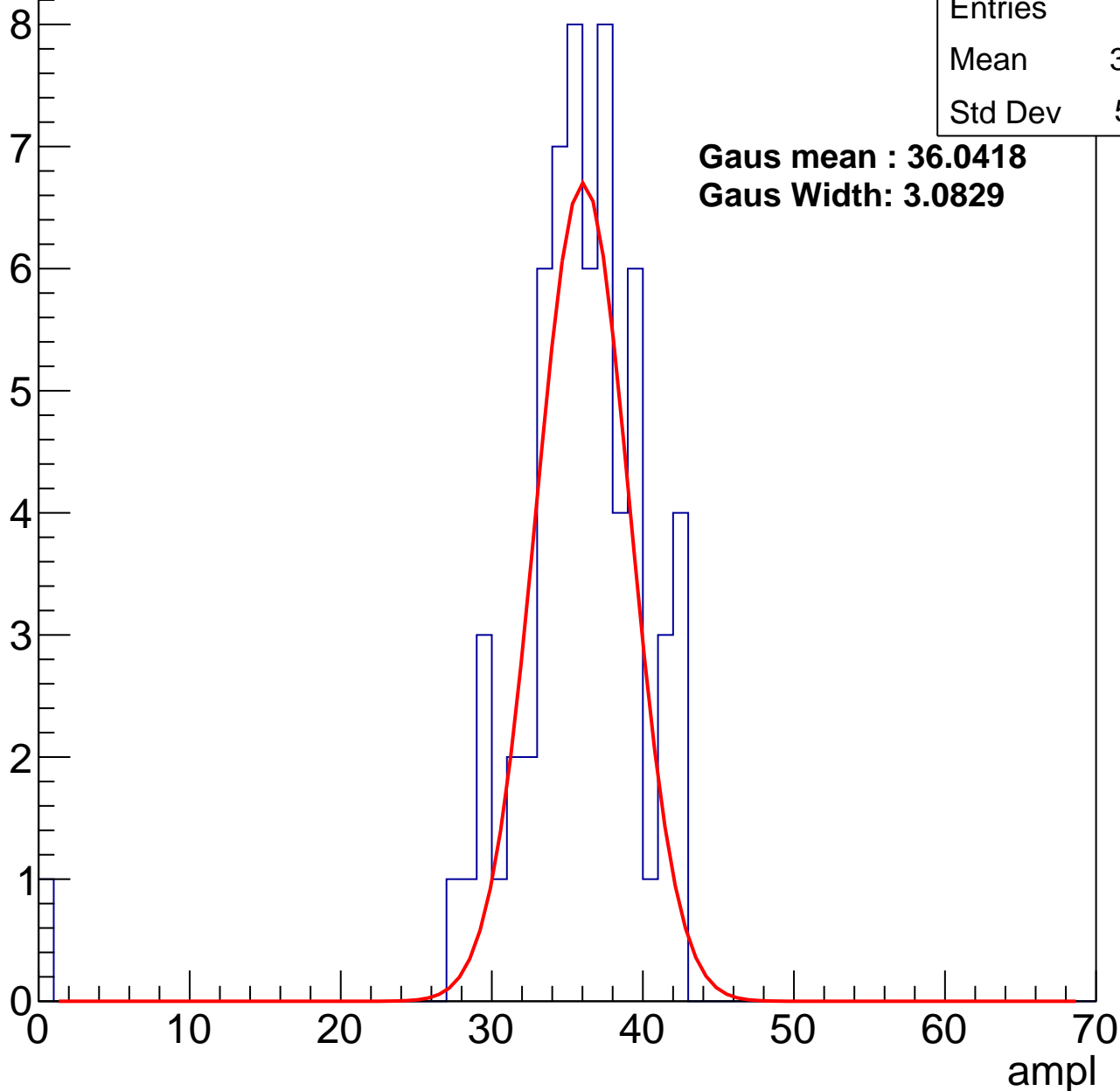
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	64
Mean	35.05
Std Dev	5.661

**Gaus mean : 36.0418**

**Gaus Width: 3.0829**



# B1L100S, U2-ch110, adc2

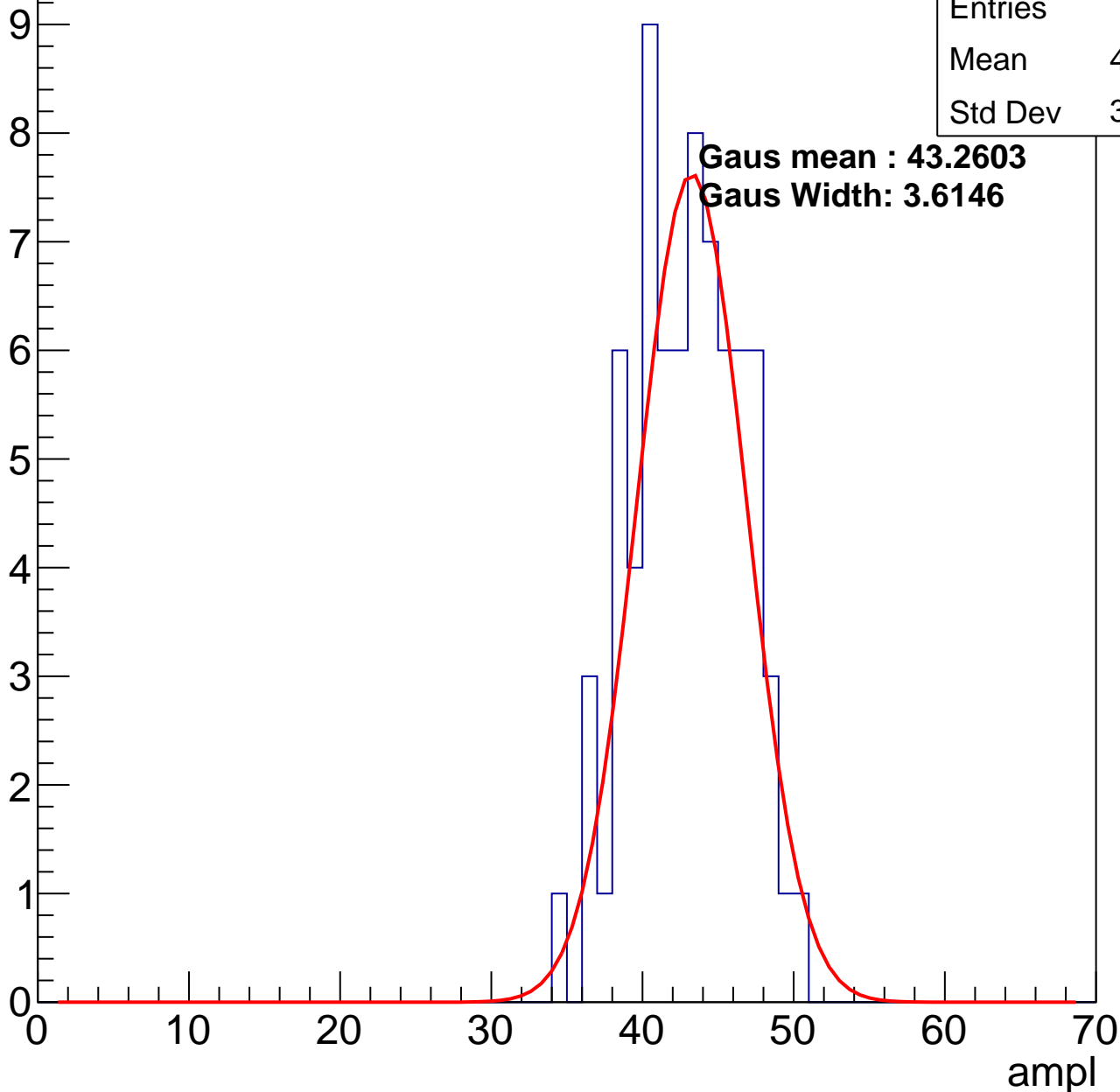
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	74
Mean	42.49
Std Dev	3.508

**Gaus mean : 43.2603**

**Gaus Width: 3.6146**

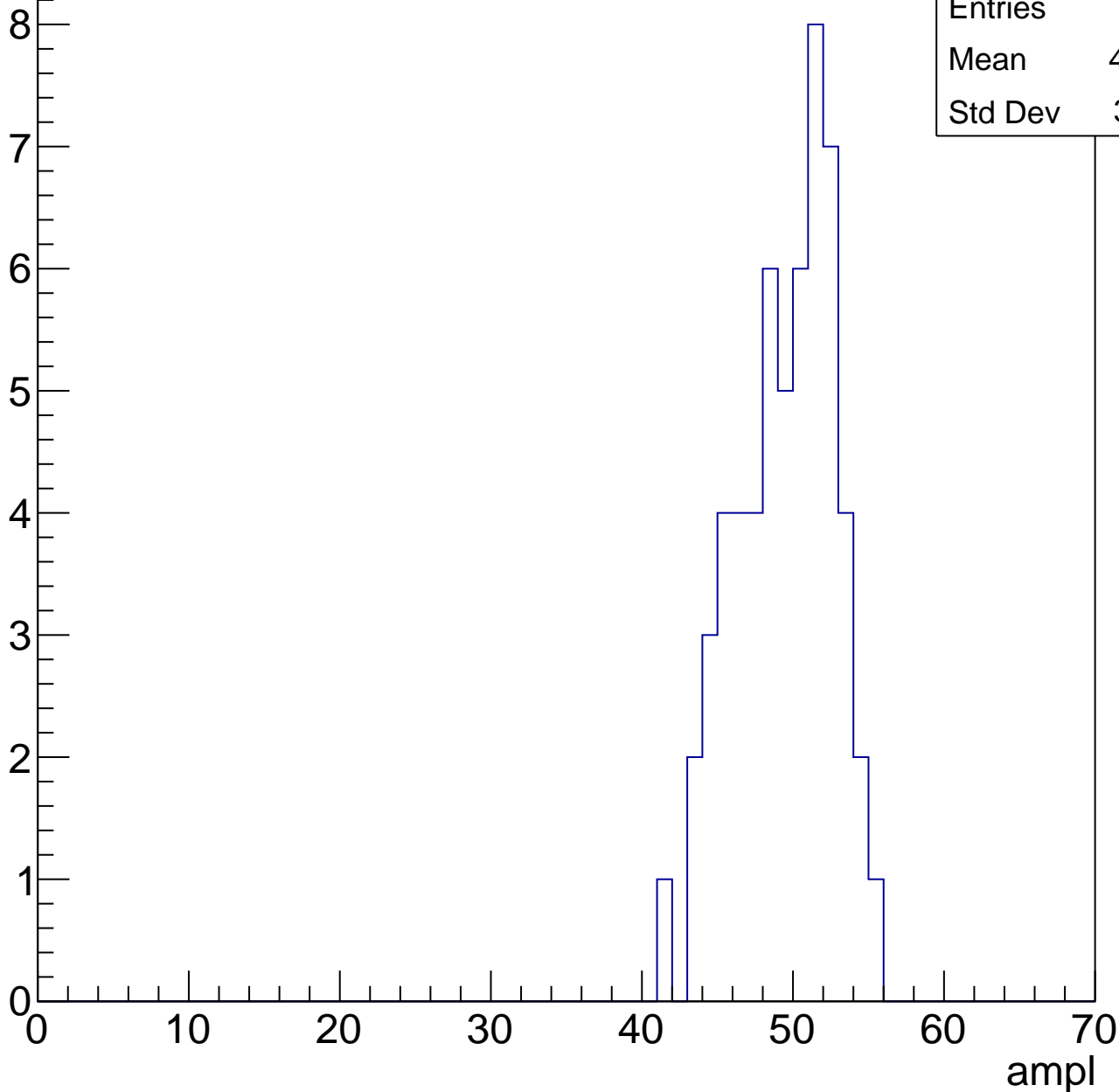


# B1L100S, U2-ch110, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

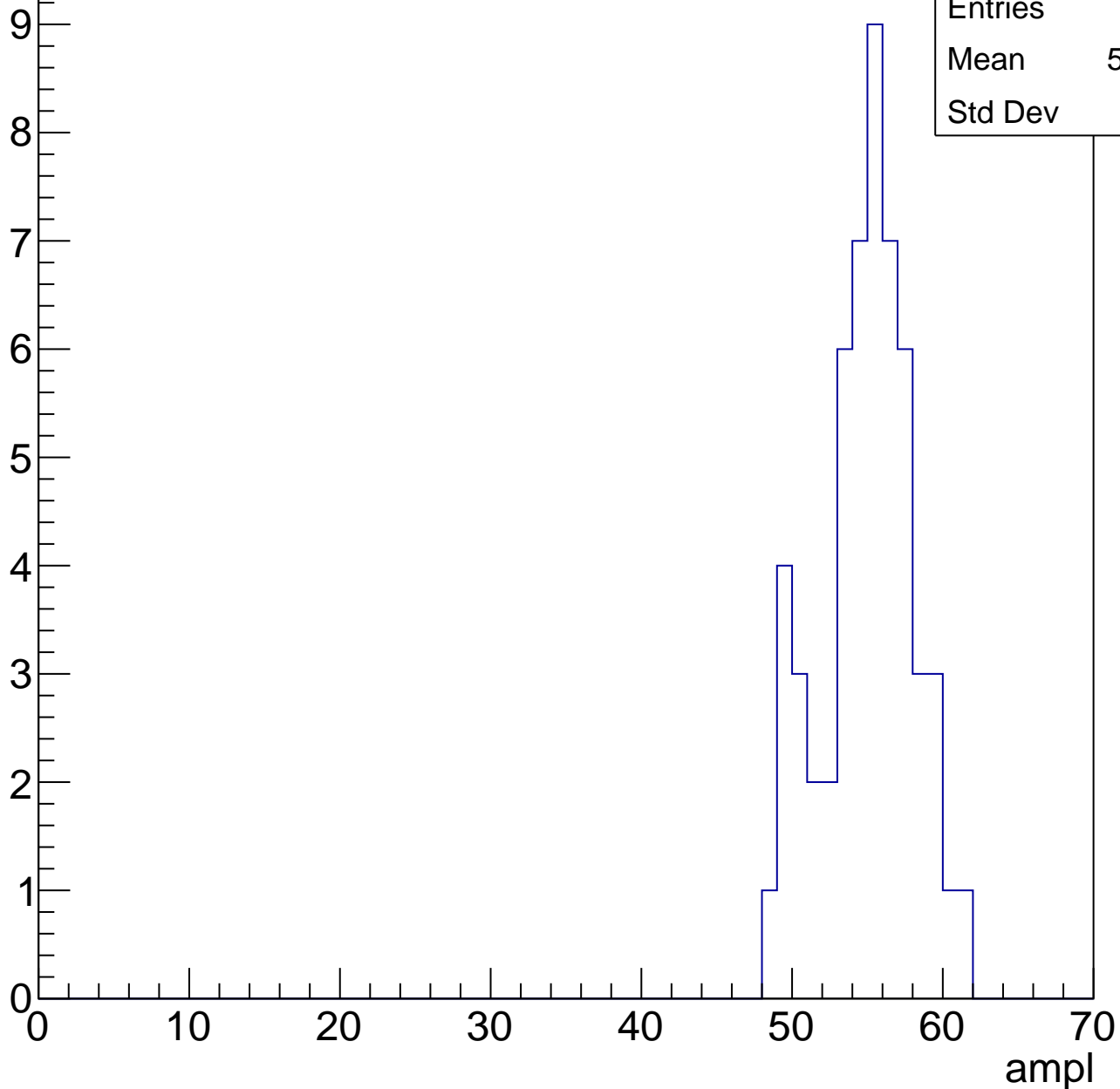
Entries	57
Mean	48.96
Std Dev	3.201



# B1L100S, U2-ch110, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



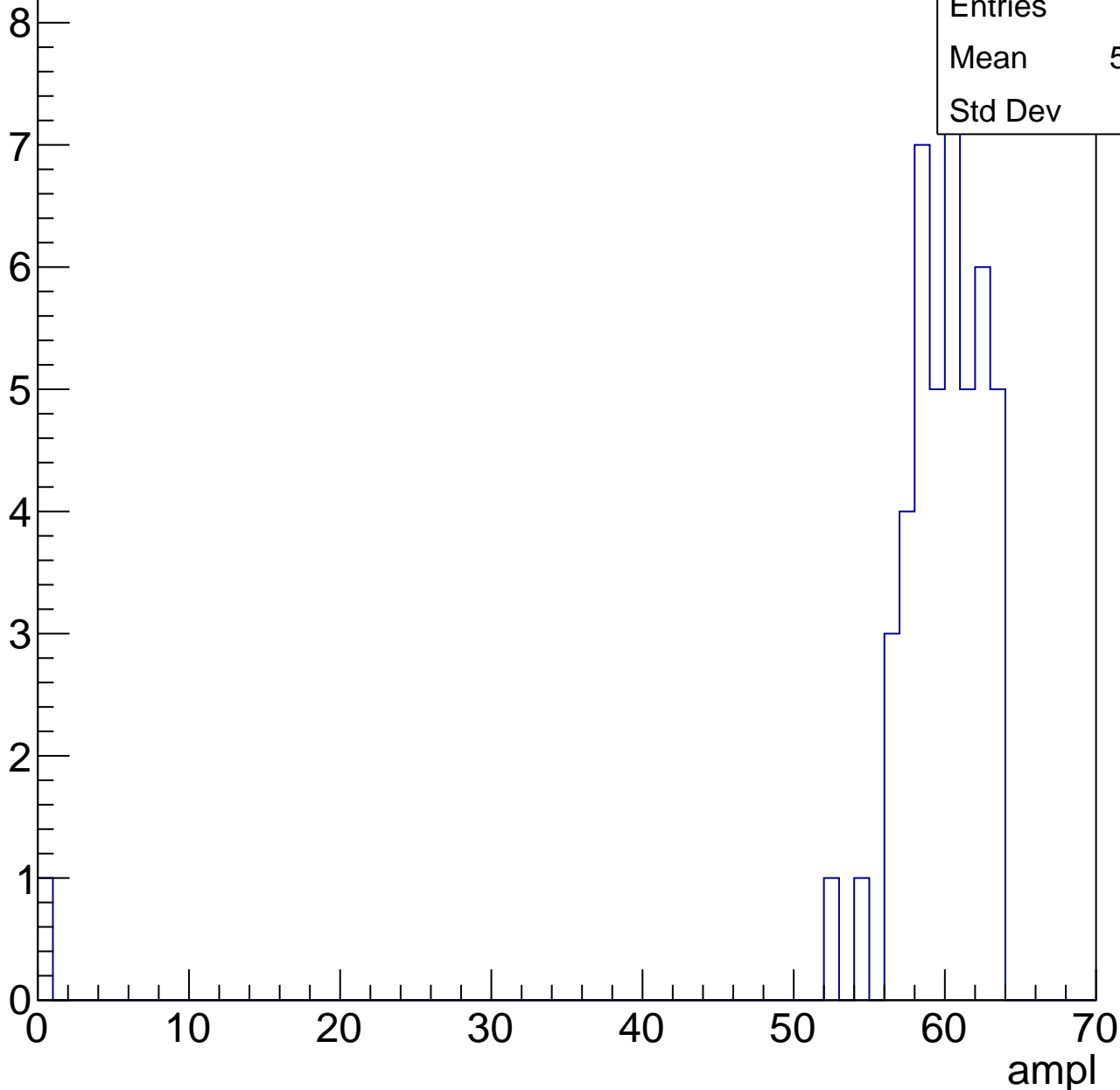
Entries	55
Mean	54.49
Std Dev	3.02

# B1L100S, U2-ch110, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	46
Mean	58.15
Std Dev	9.01

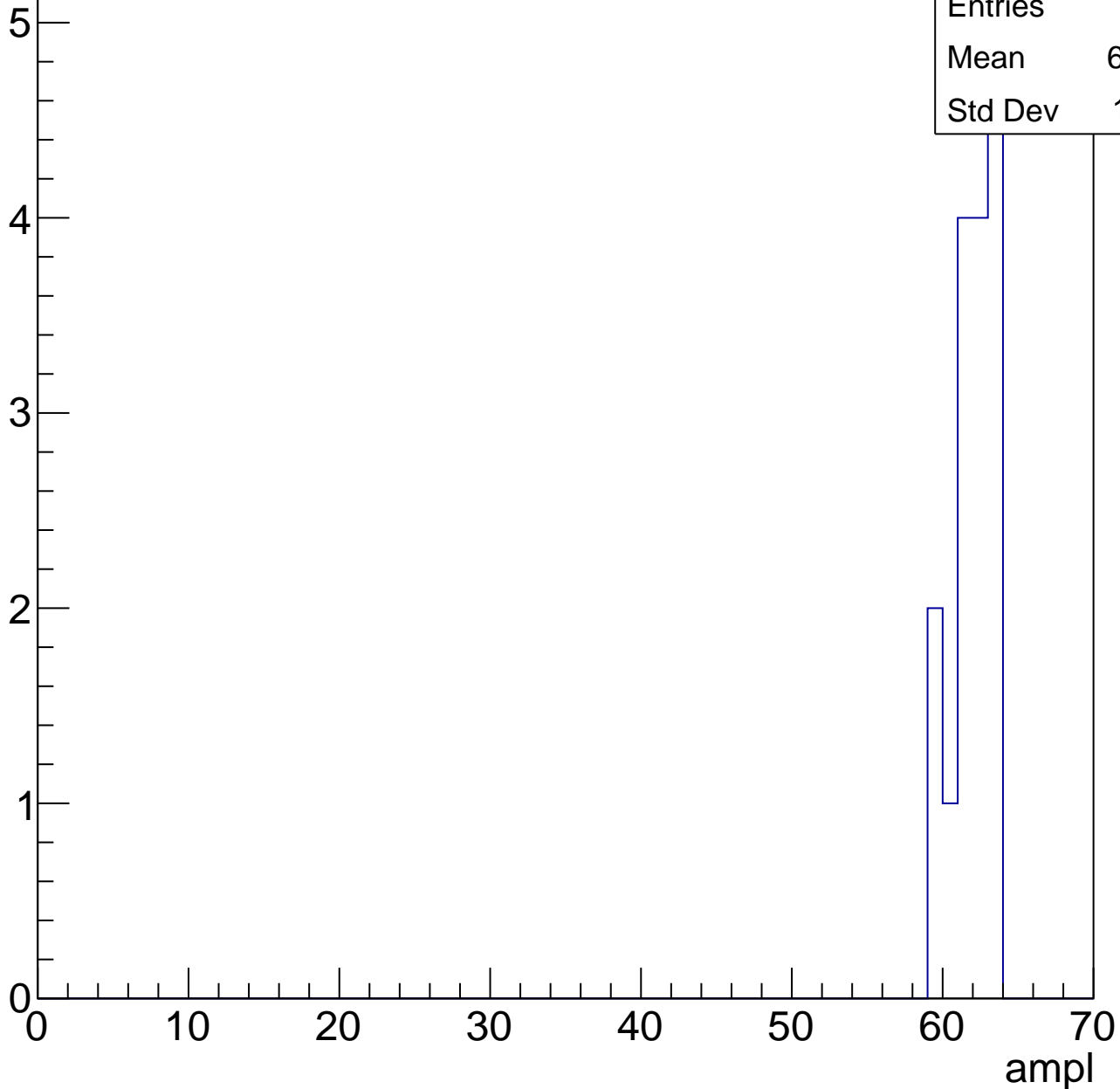


# B1L100S, U2-ch110, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	16
Mean	61.56
Std Dev	1.321





# B1L100S, U2-ch110, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



# B1L100S, U2-ch111, adc0

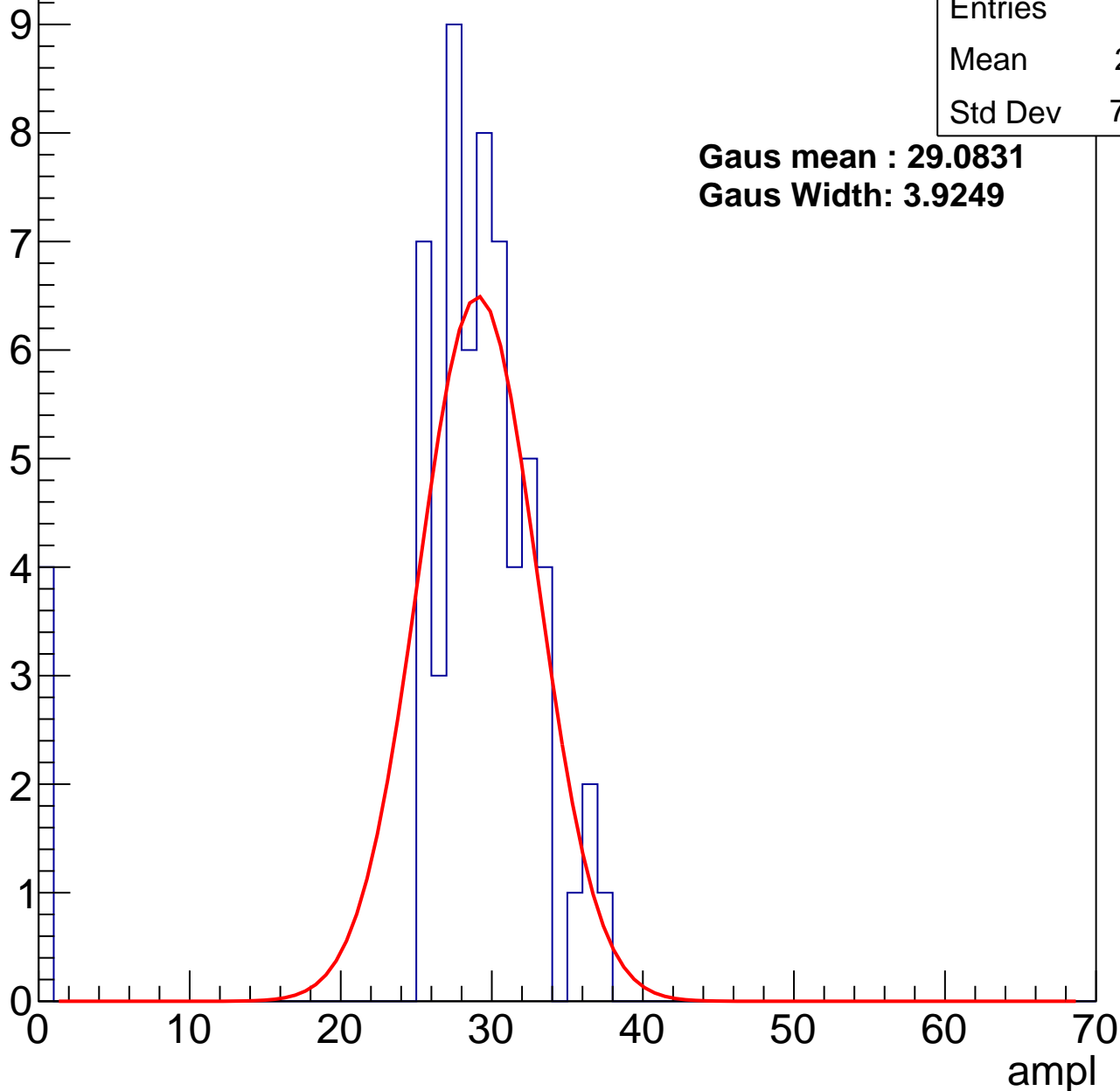
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	61
Mean	27.31
Std Dev	7.789

**Gaus mean : 29.0831**

**Gaus Width: 3.9249**



# B1L100S, U2-ch111, adc1

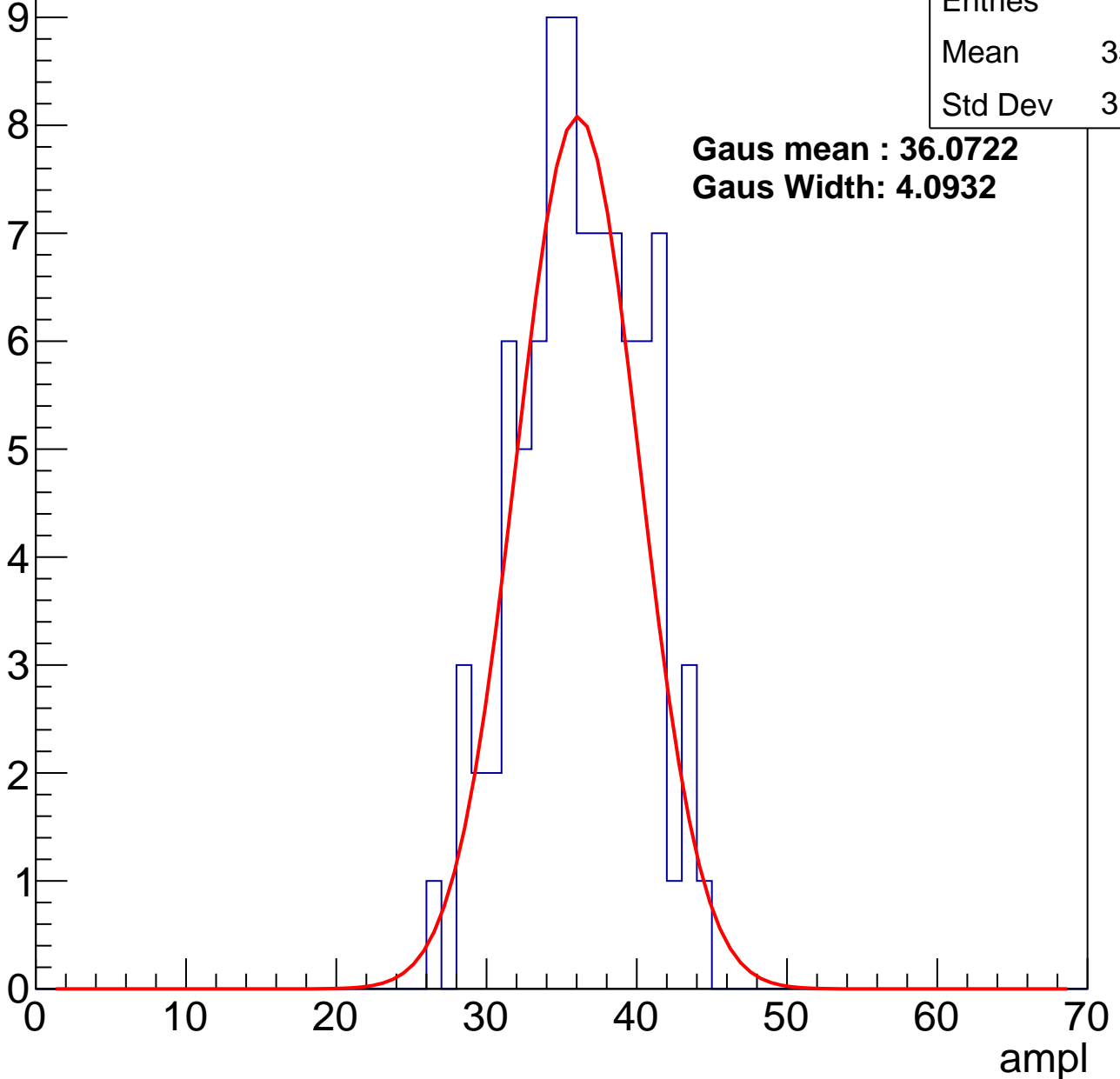
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	88
Mean	35.75
Std Dev	3.978

**Gaus mean : 36.0722**

**Gaus Width: 4.0932**



# B1L100S, U2-ch111, adc2

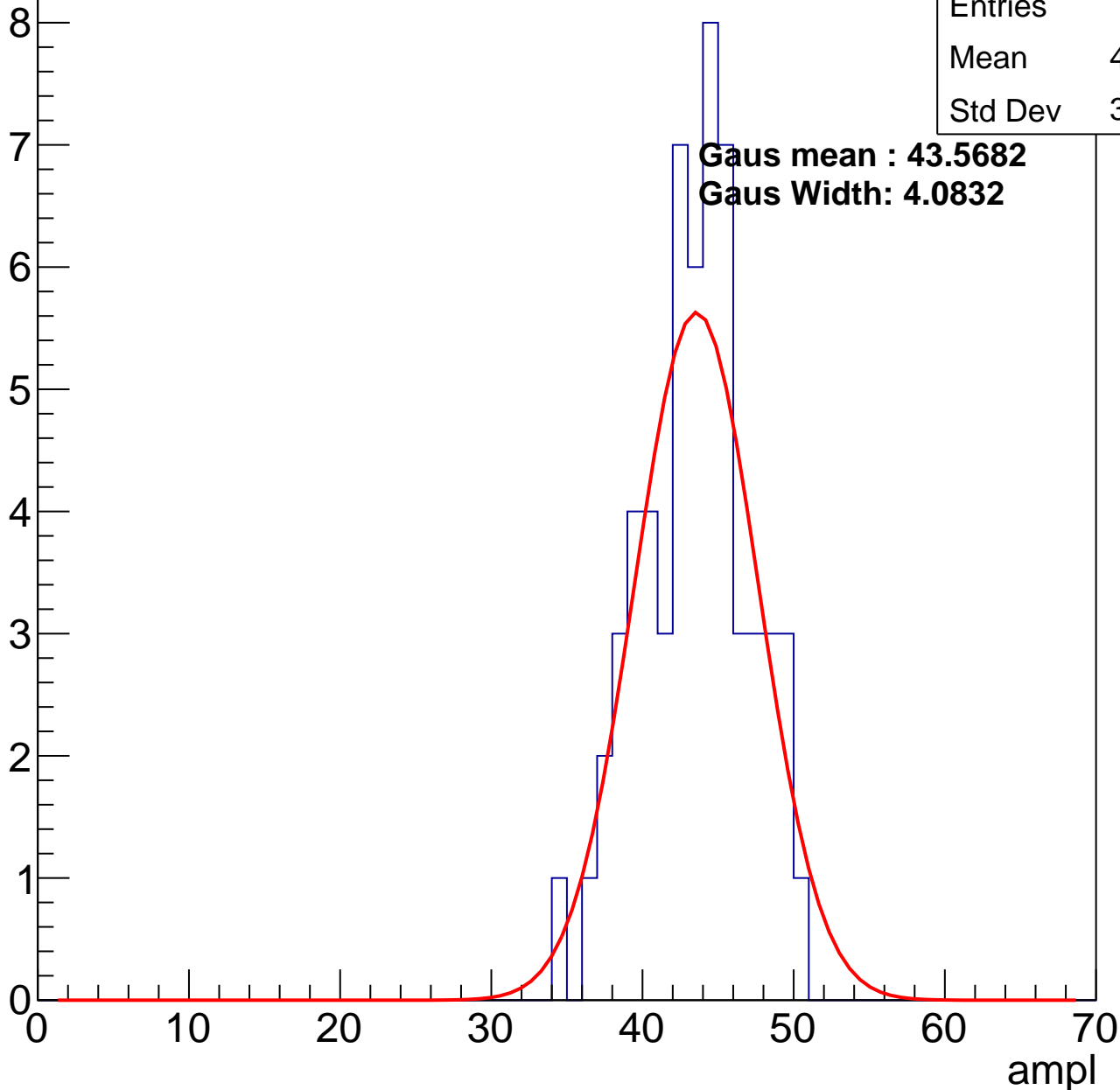
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	59
Mean	42.98
Std Dev	3.539

**Gaus mean : 43.5682**

**Gaus Width: 4.0832**

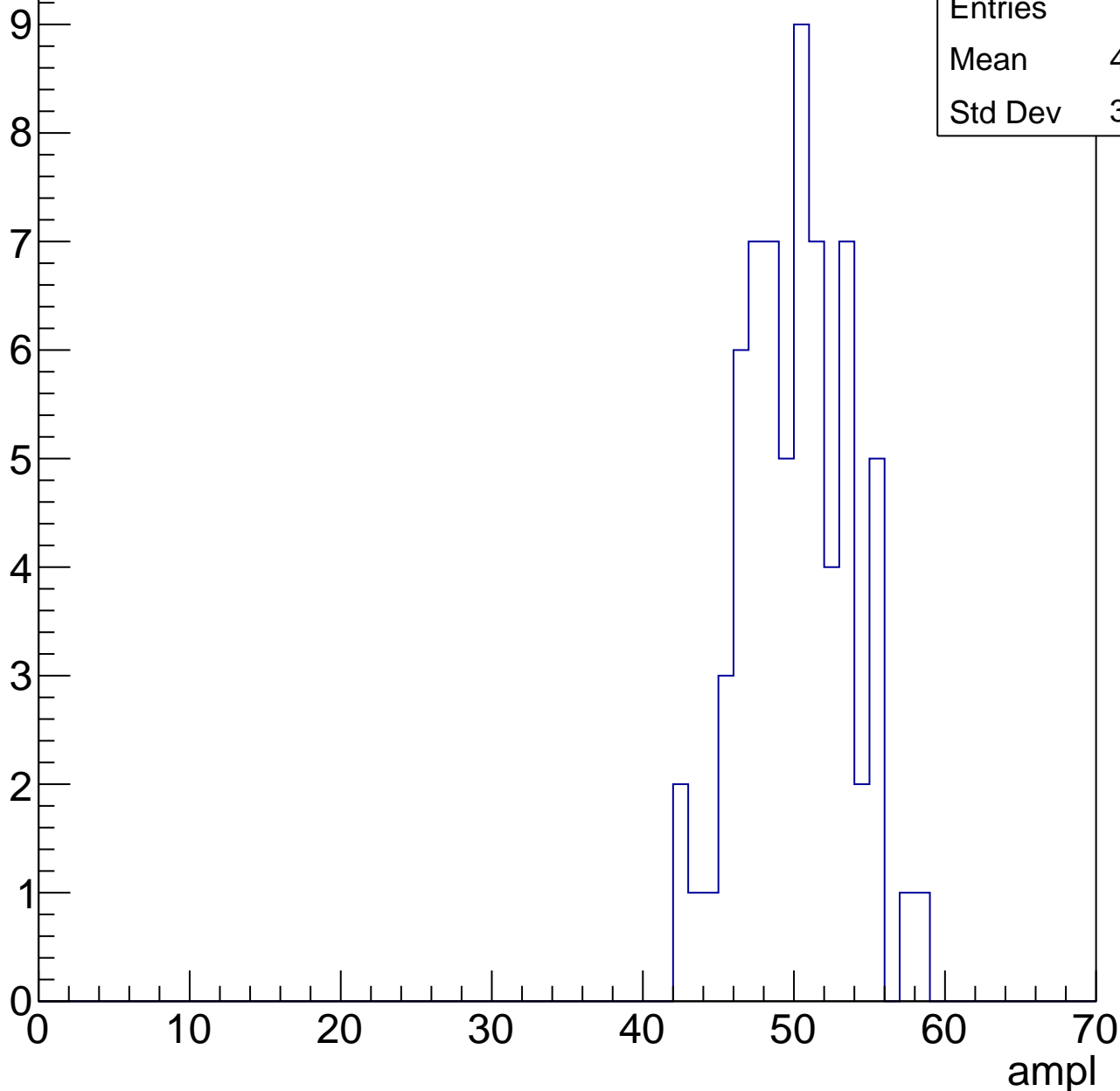


# B1L100S, U2-ch111, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	68
Mean	49.65
Std Dev	3.488

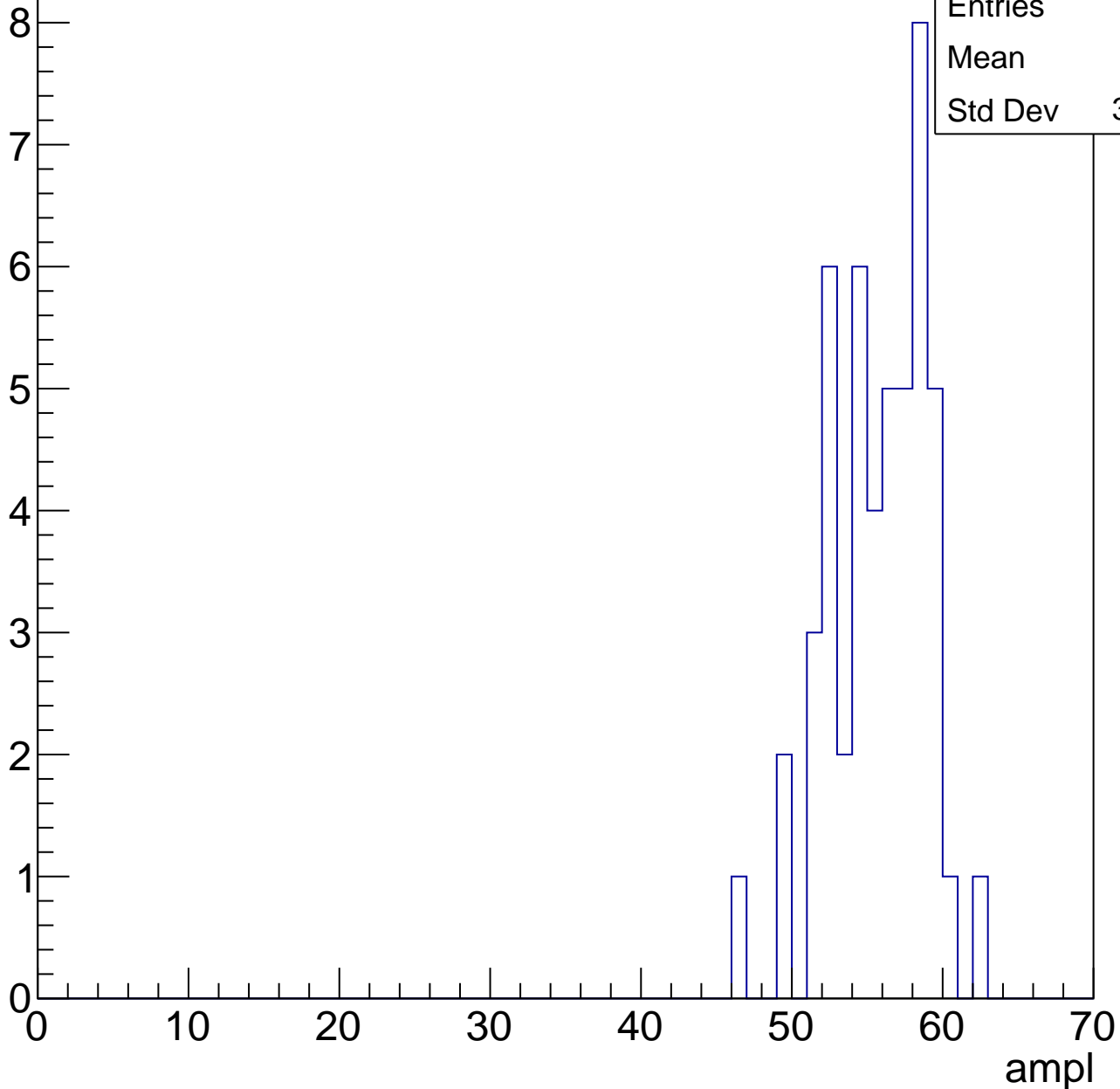


# B1L100S, U2-ch111, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	49
Mean	55.2
Std Dev	3.251



# B1L100S, U2-ch111, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

10

8

6

4

2

0

0

10

20

30

40

50

60

ampl

Entries	55
Mean	58.67
Std Dev	8.408

0

0

0

0

0

0

0

0

0

0

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# B1L100S, U2-ch111, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	2
Mean	63
Std Dev	0

0 10 20 30 40 50 60 70

ampl



# B1L100S, U2-ch111, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



# B1L100S, U2-ch112, adc0

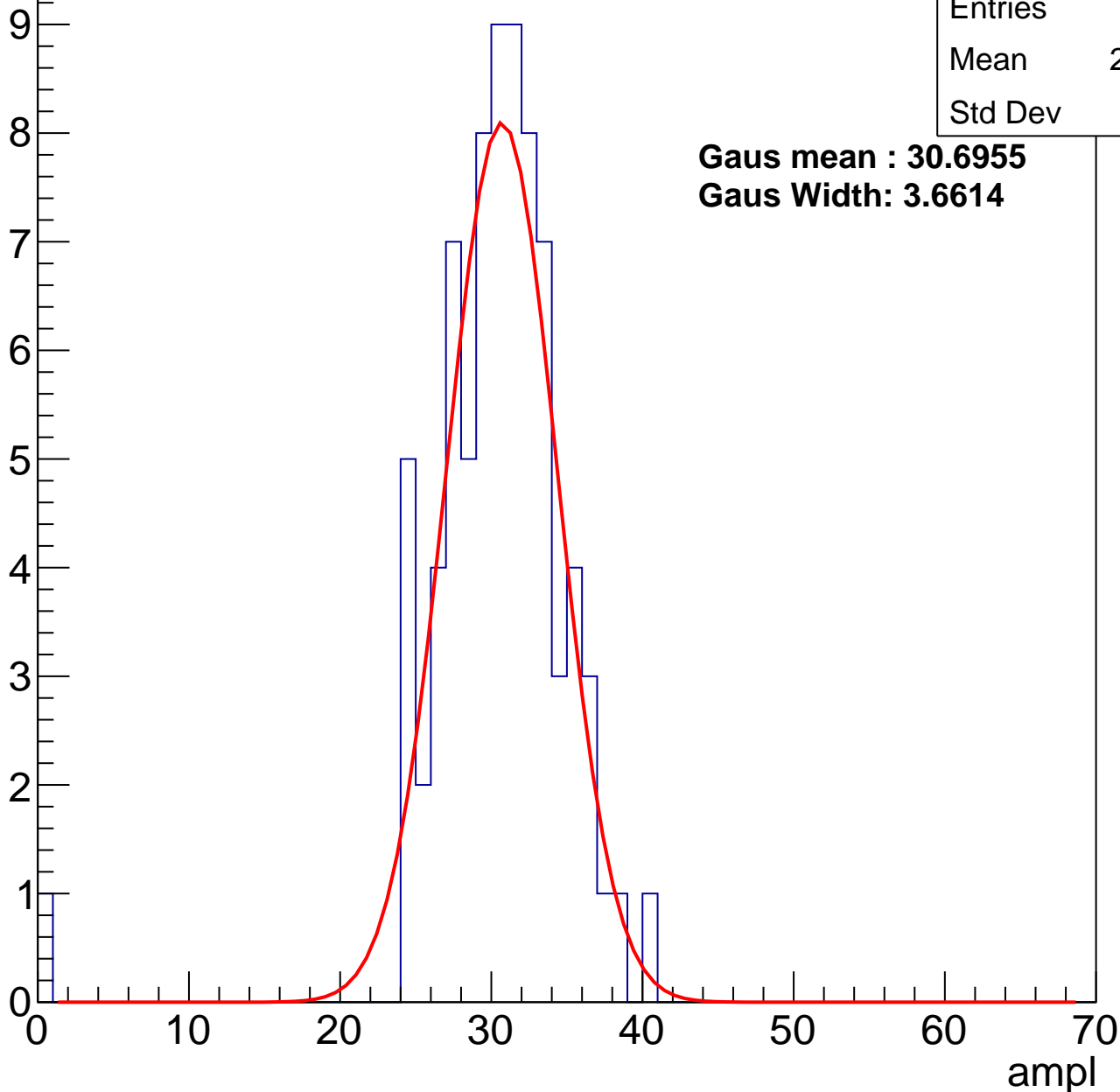
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	78
Mean	29.95
Std Dev	4.88

**Gaus mean : 30.6955**

**Gaus Width: 3.6614**



# B1L100S, U2-ch112, adc1

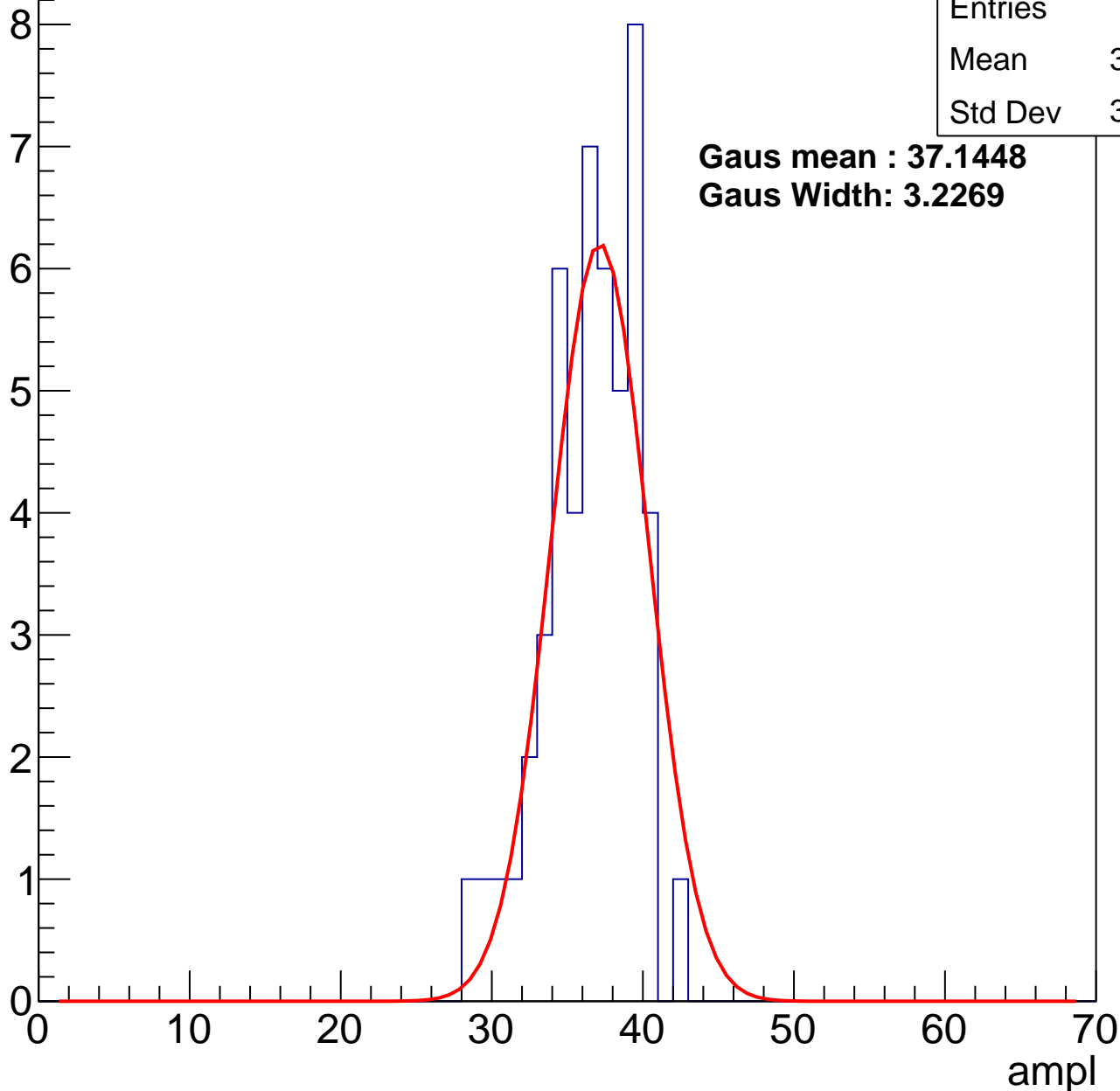
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	50
Mean	36.06
Std Dev	3.029

**Gaus mean : 37.1448**

**Gaus Width: 3.2269**



# B1L100S, U2-ch112, adc2

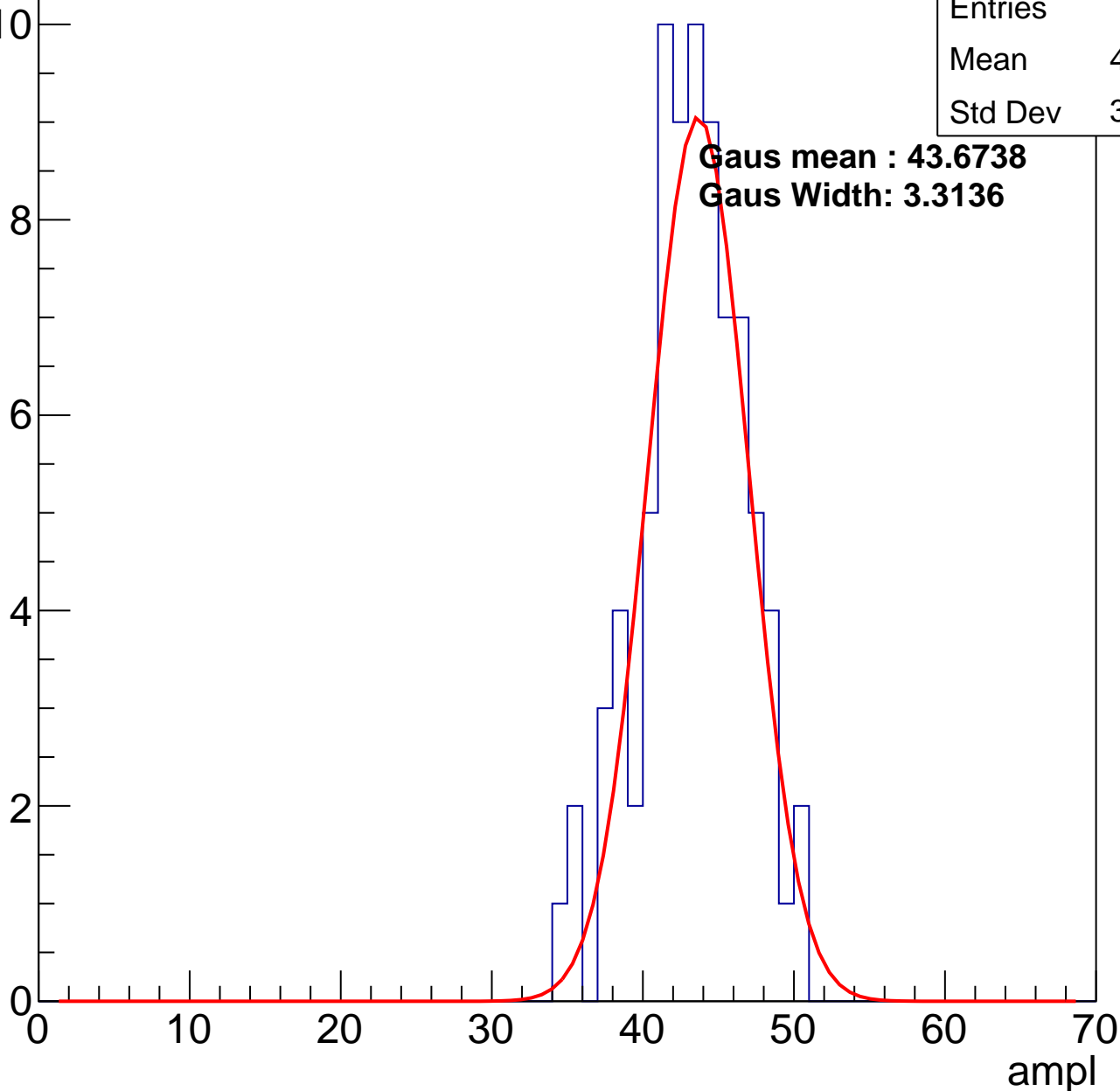
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	81
Mean	42.86
Std Dev	3.435

**Gaus mean : 43.6738**

**Gaus Width: 3.3136**

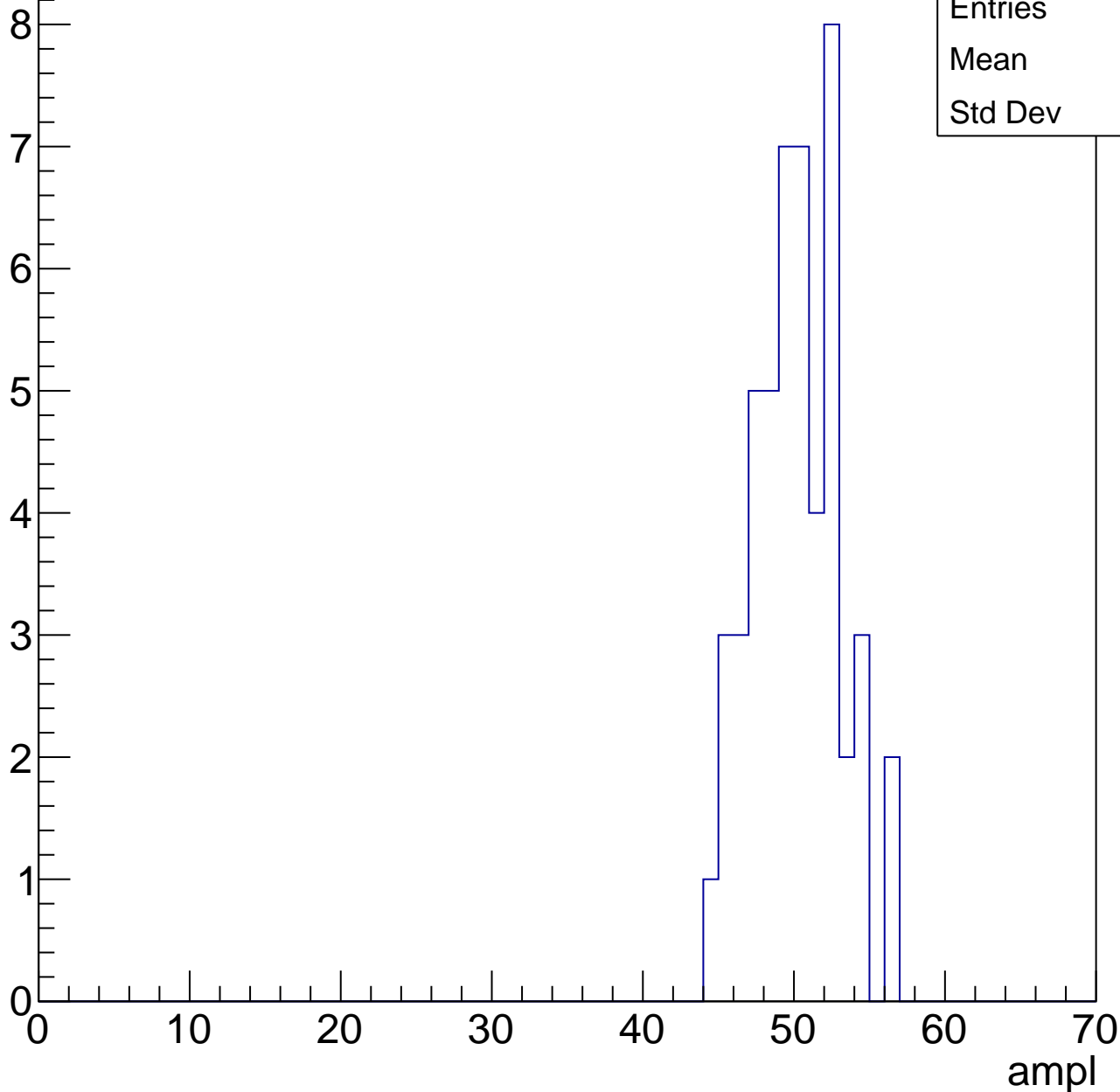


# B1L100S, U2-ch112, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	50
Mean	49.7
Std Dev	2.83

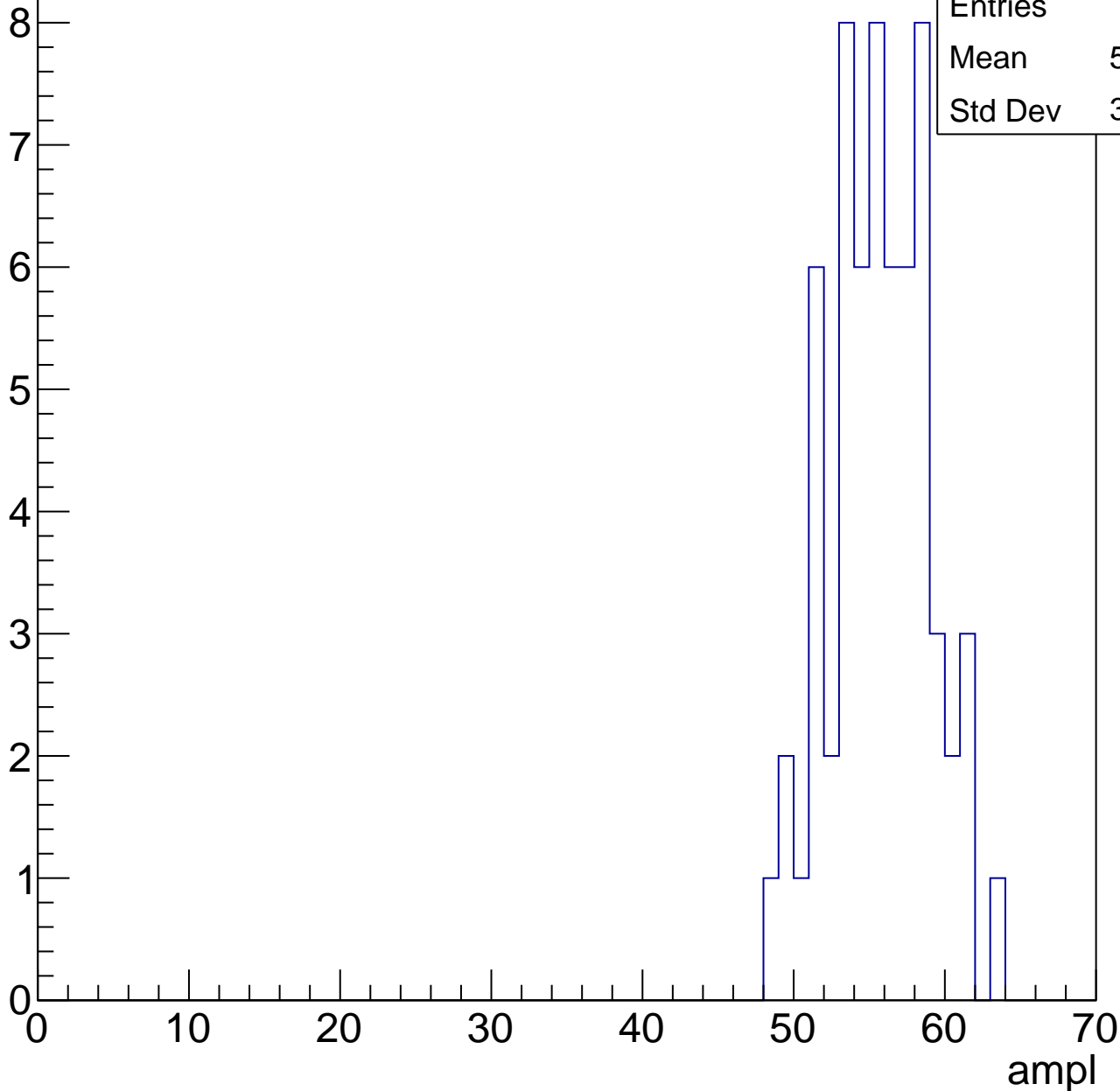


# B1L100S, U2-ch112, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

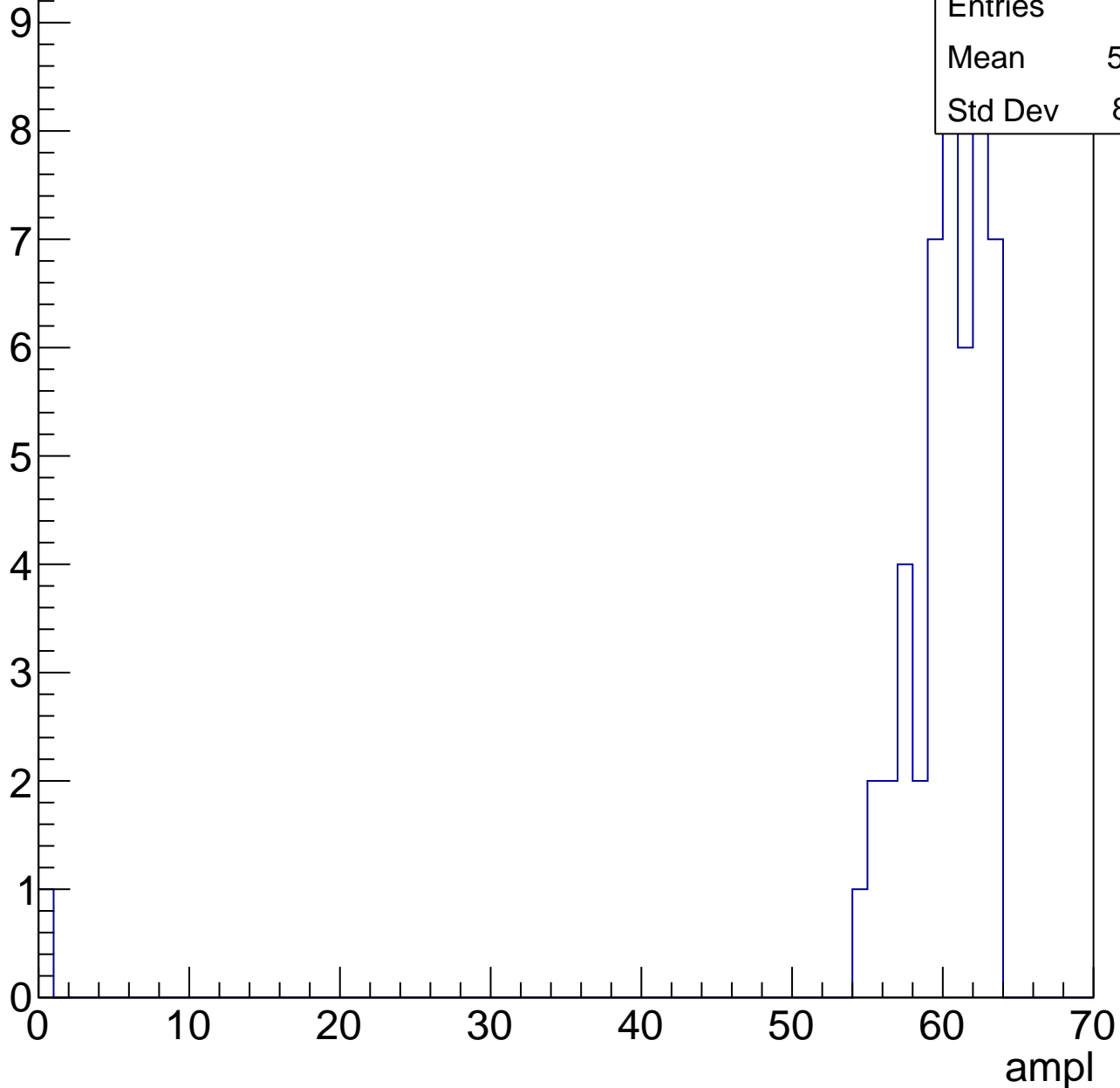
Entries	63
Mean	55.22
Std Dev	3.254



# B1L100S, U2-ch112, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



# B1L100S, U2-ch112, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	4
Mean	62.25
Std Dev	0.8292

ampl

0 10 20 30 40 50 60 70



# B1L100S, U2-ch112, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



# B1L100S, U2-ch113, adc0

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	78
Mean	29.74
Std Dev	4.609

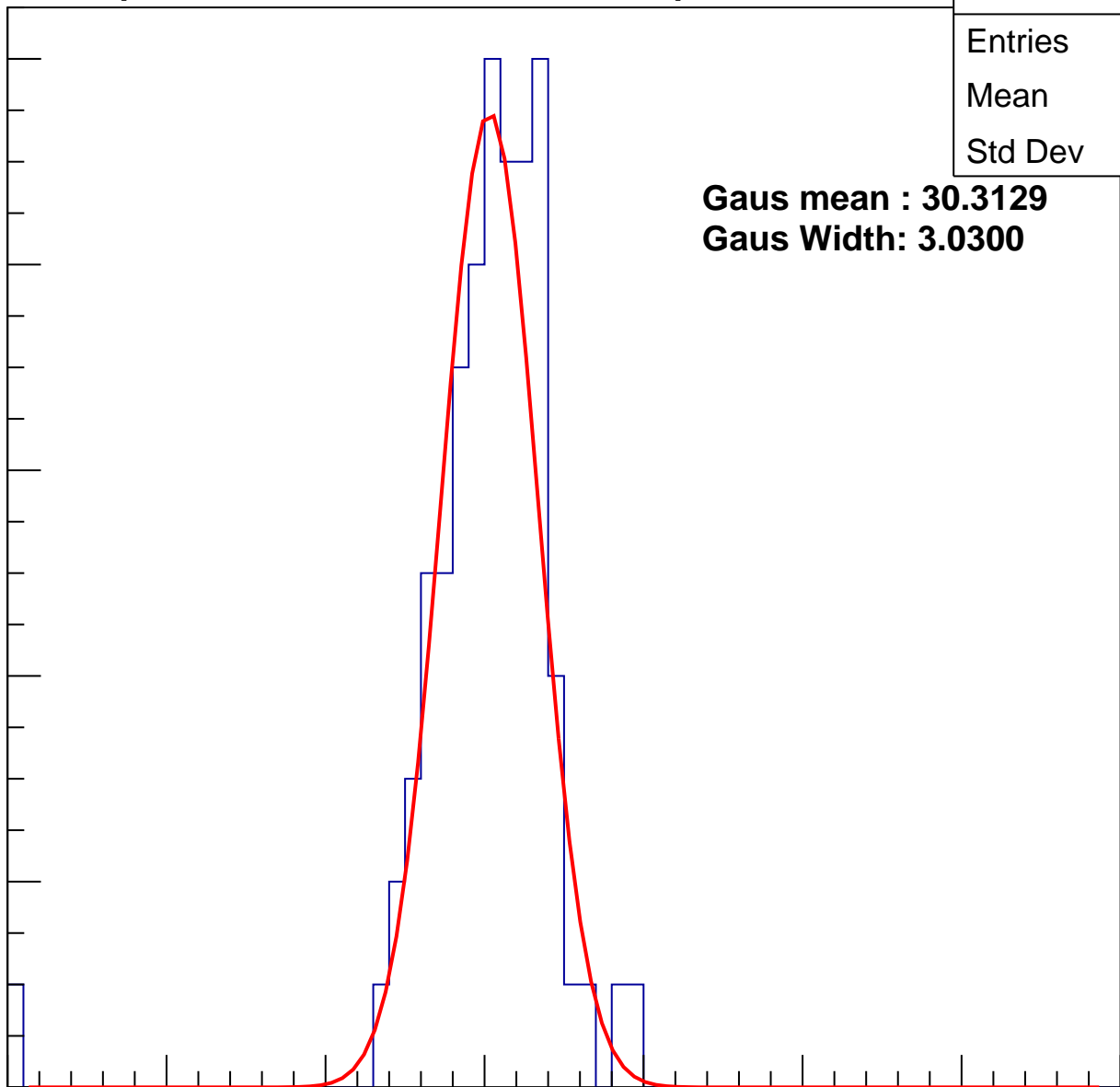
**Gaus mean : 30.3129**  
**Gaus Width: 3.0300**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



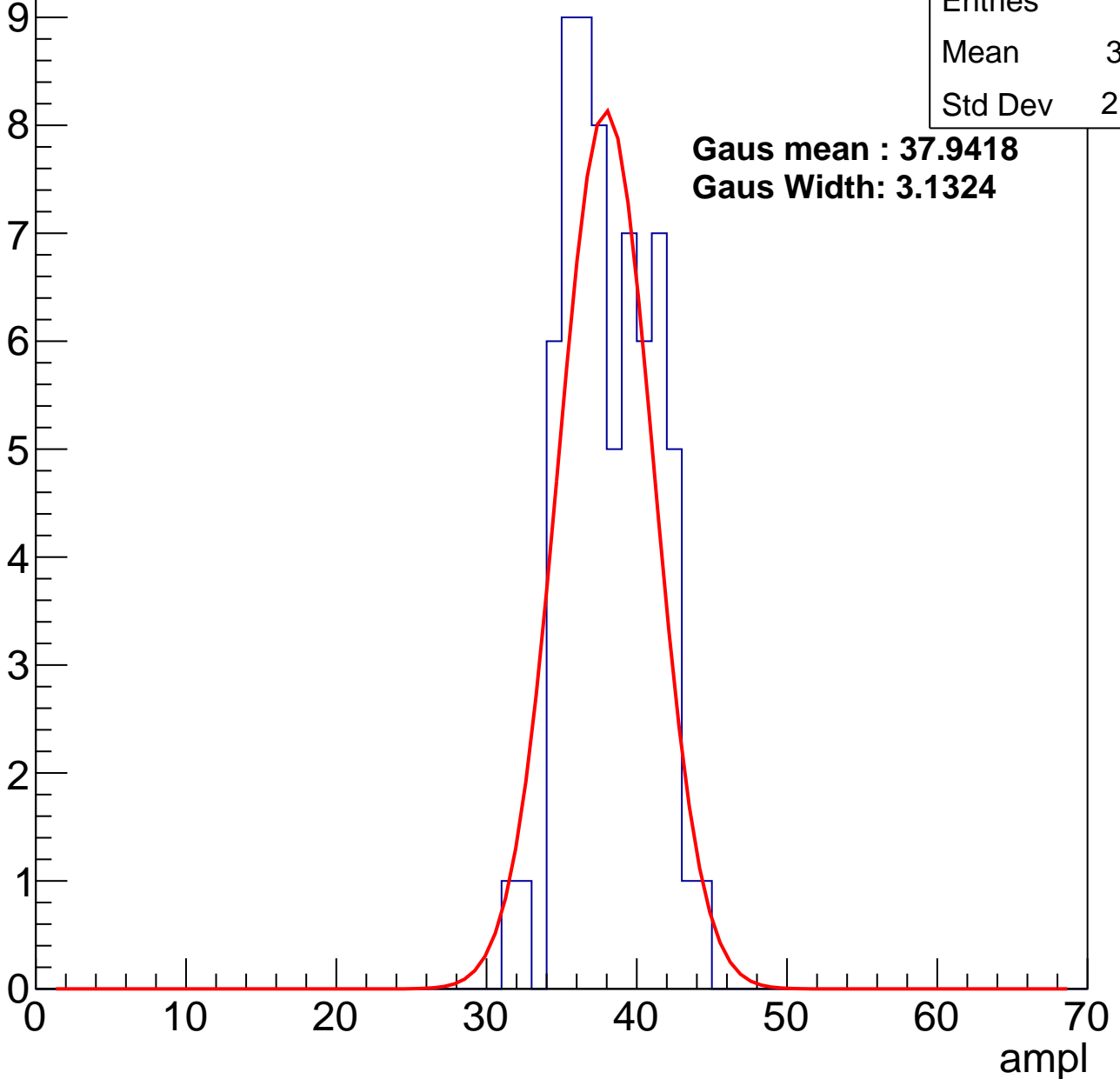
# B1L100S, U2-ch113, adc1

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	66
Mean	37.71
Std Dev	2.849

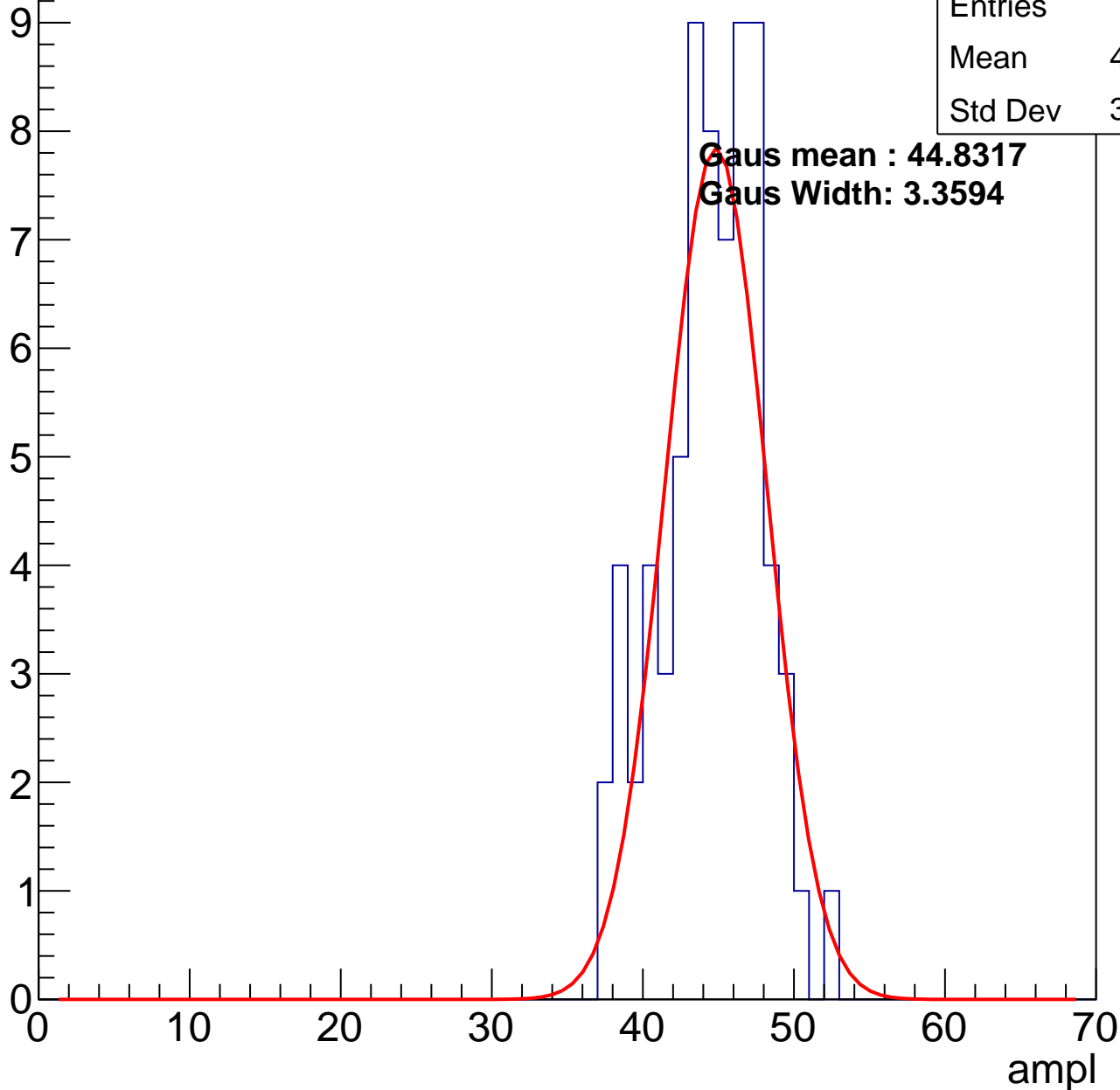
**Gaus mean : 37.9418**  
**Gaus Width: 3.1324**



# B1L100S, U2-ch113, adc2

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

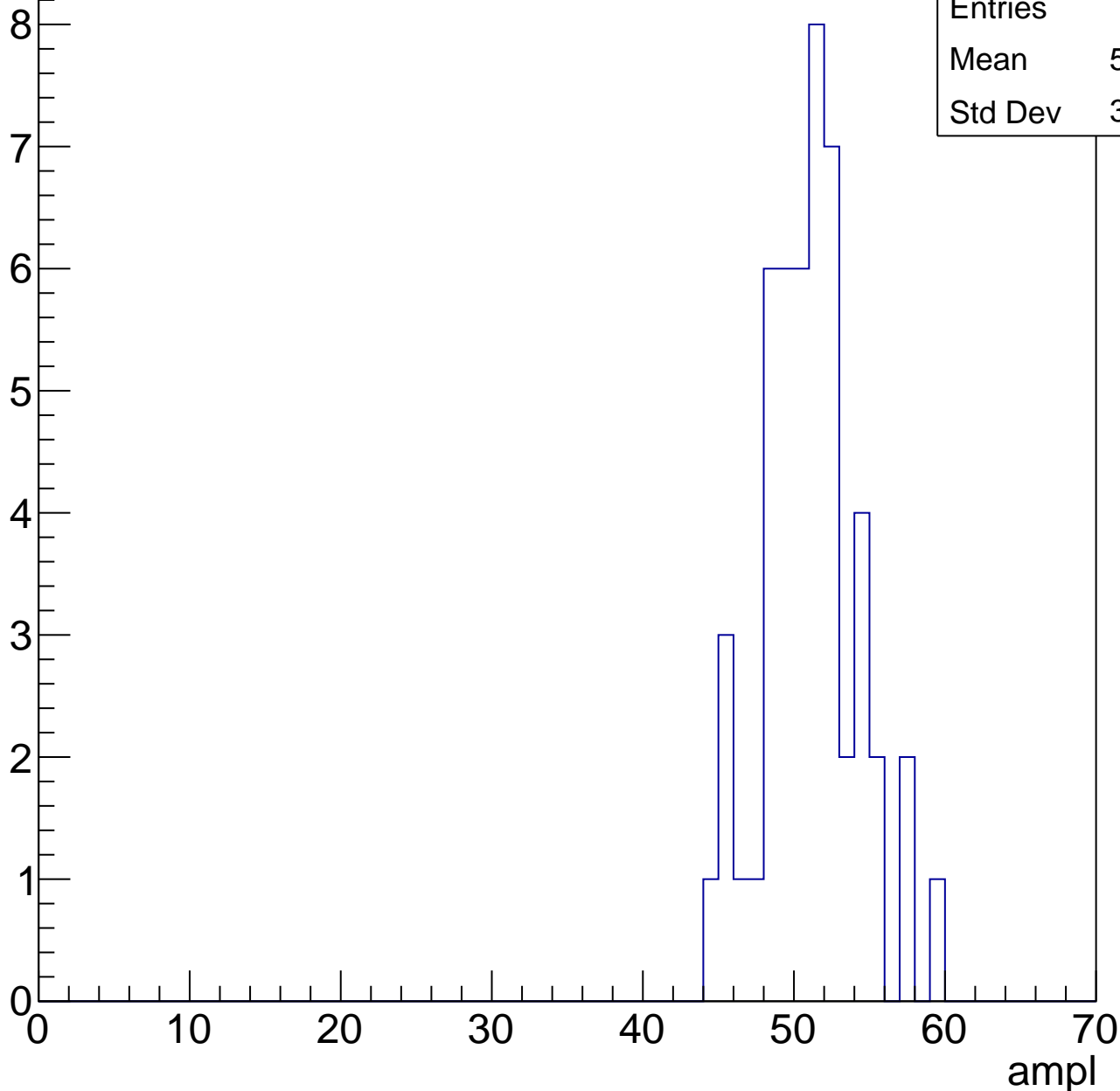


# B1L100S, U2-ch113, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	50
Mean	50.62
Std Dev	3.143



# B1L100S, U2-ch113, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

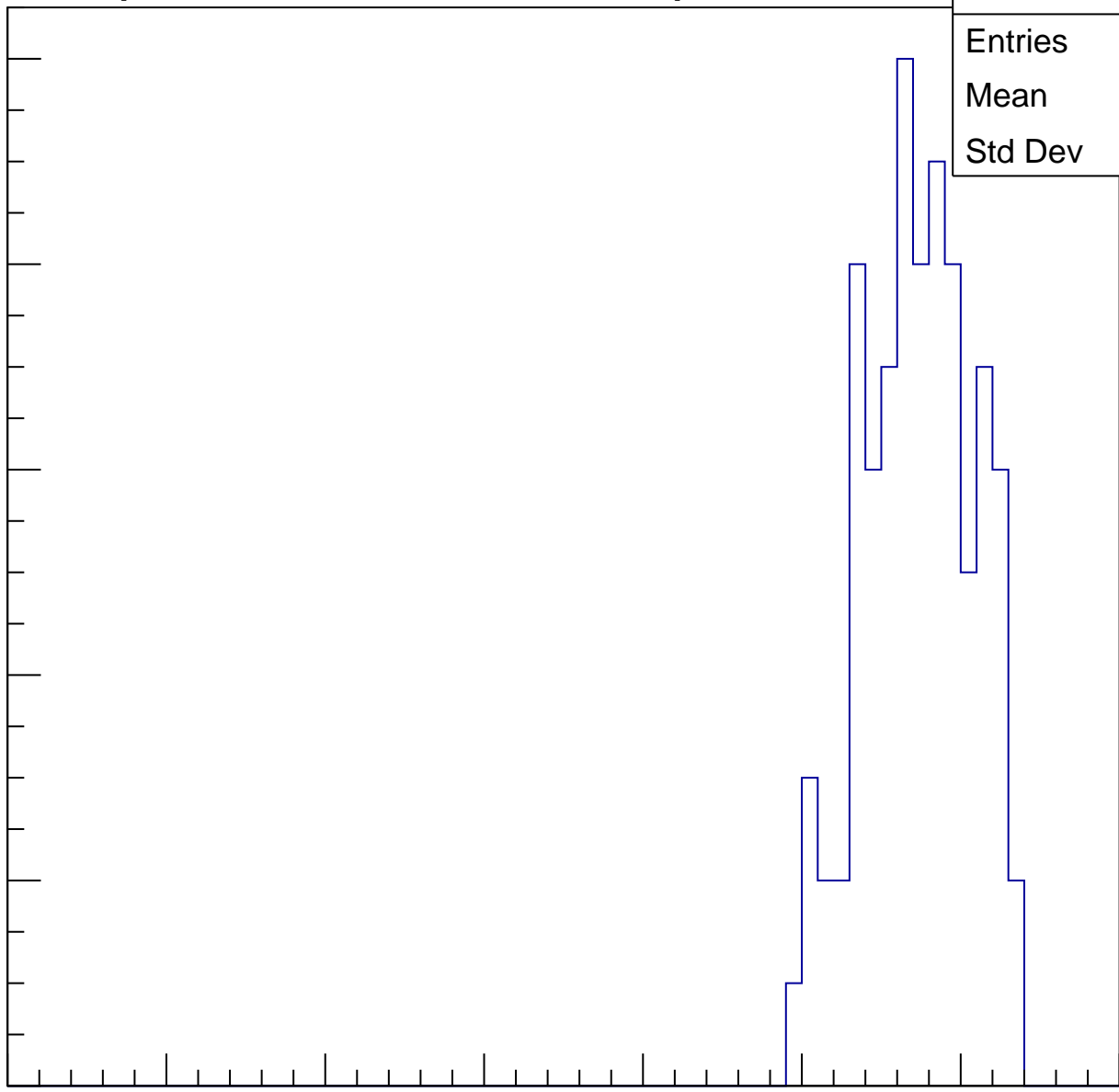
Entries	84
Mean	56.82
Std Dev	3.399

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

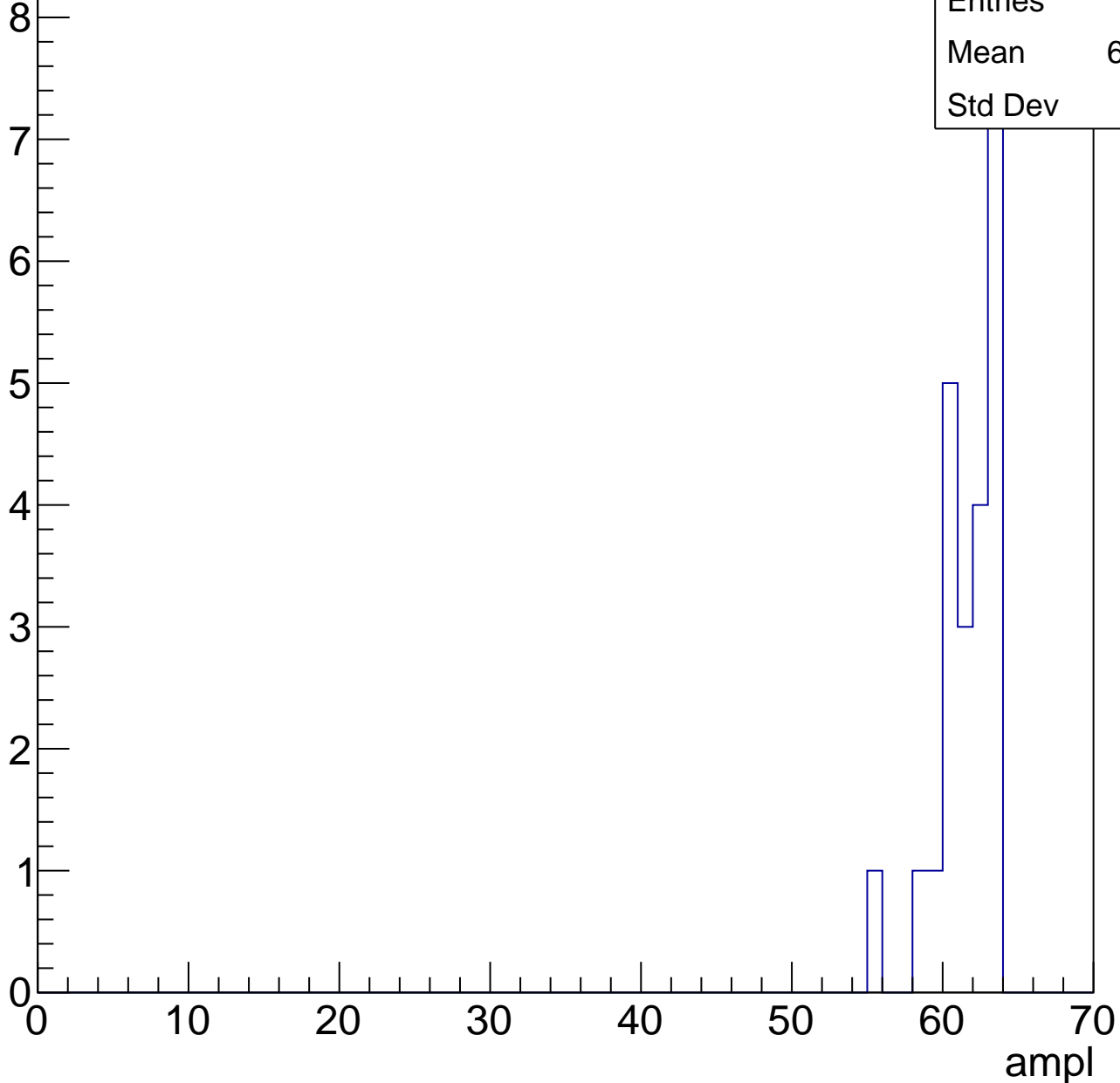


# B1L100S, U2-ch113, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

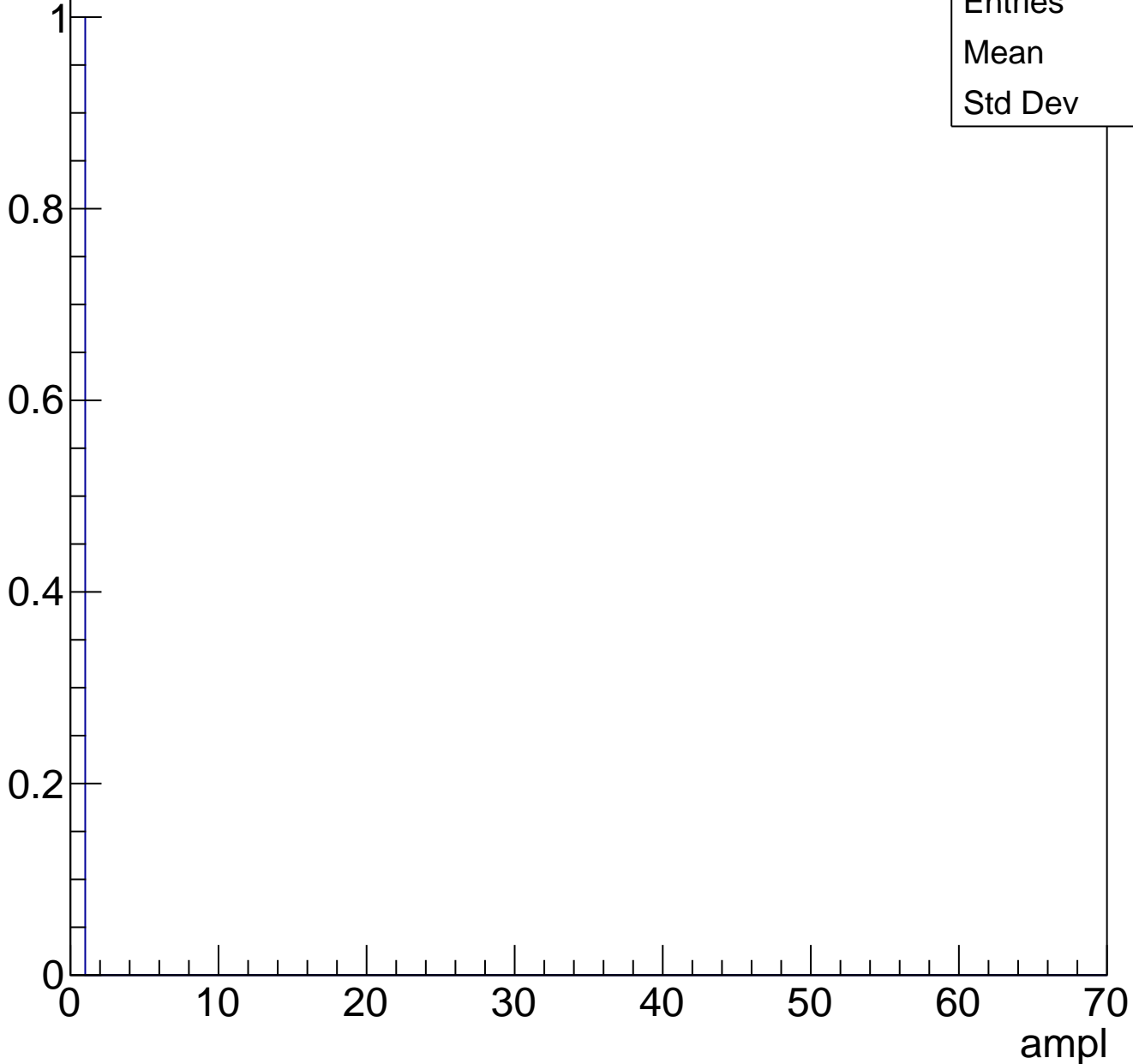
Entries	23
Mean	61.17
Std Dev	1.97



# B1L100S, U2-ch113, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry





# B1L100S, U2-ch113, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

1  
0.8  
0.6  
0.4  
0.2  
0

Entries	1
Mean	22
Std Dev	0

ampl

# B1L100S, U2-ch114, adc0

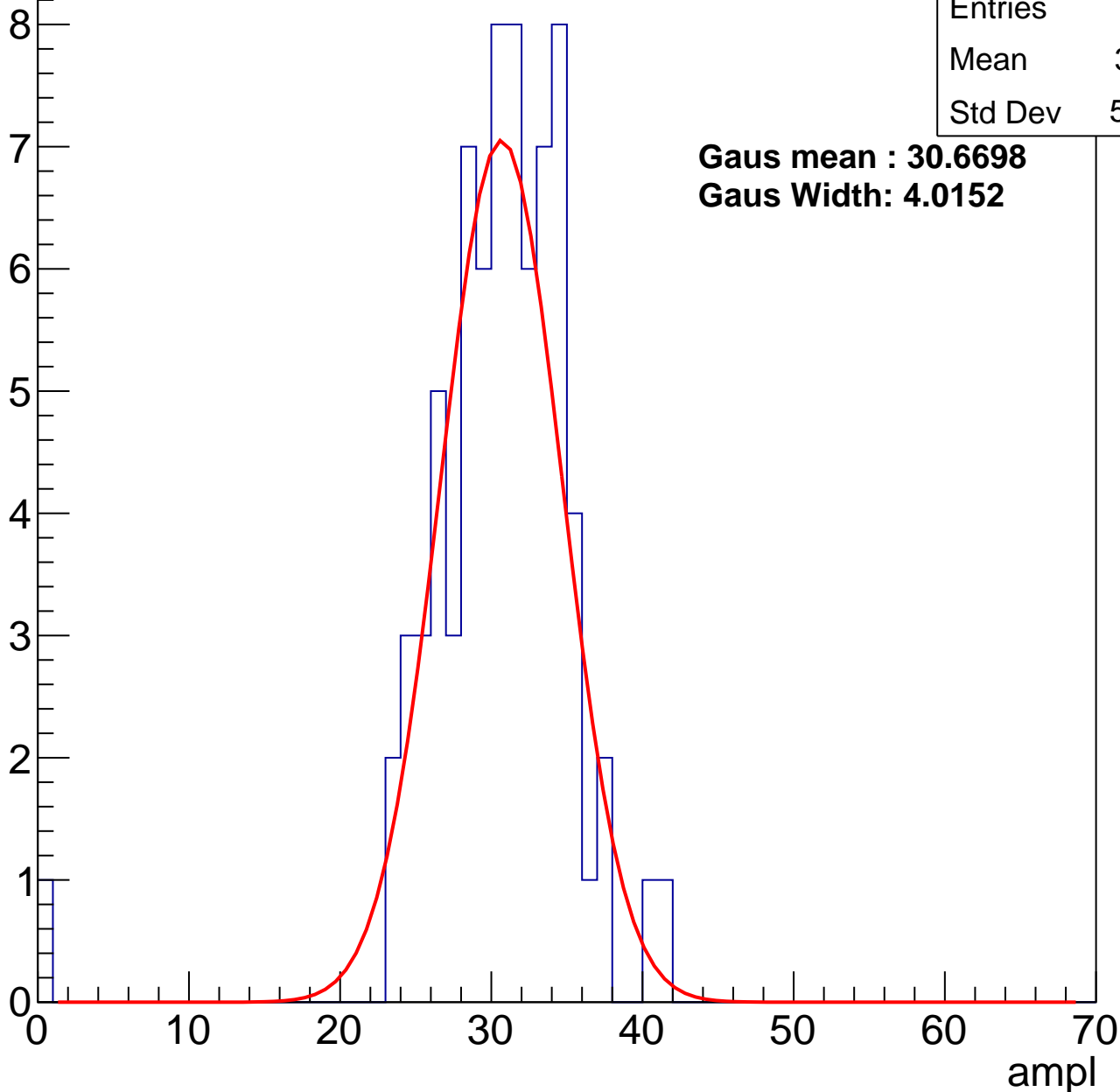
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	76
Mean	30.11
Std Dev	5.129

**Gaus mean : 30.6698**

**Gaus Width: 4.0152**



# B1L100S, U2-ch114, adc1

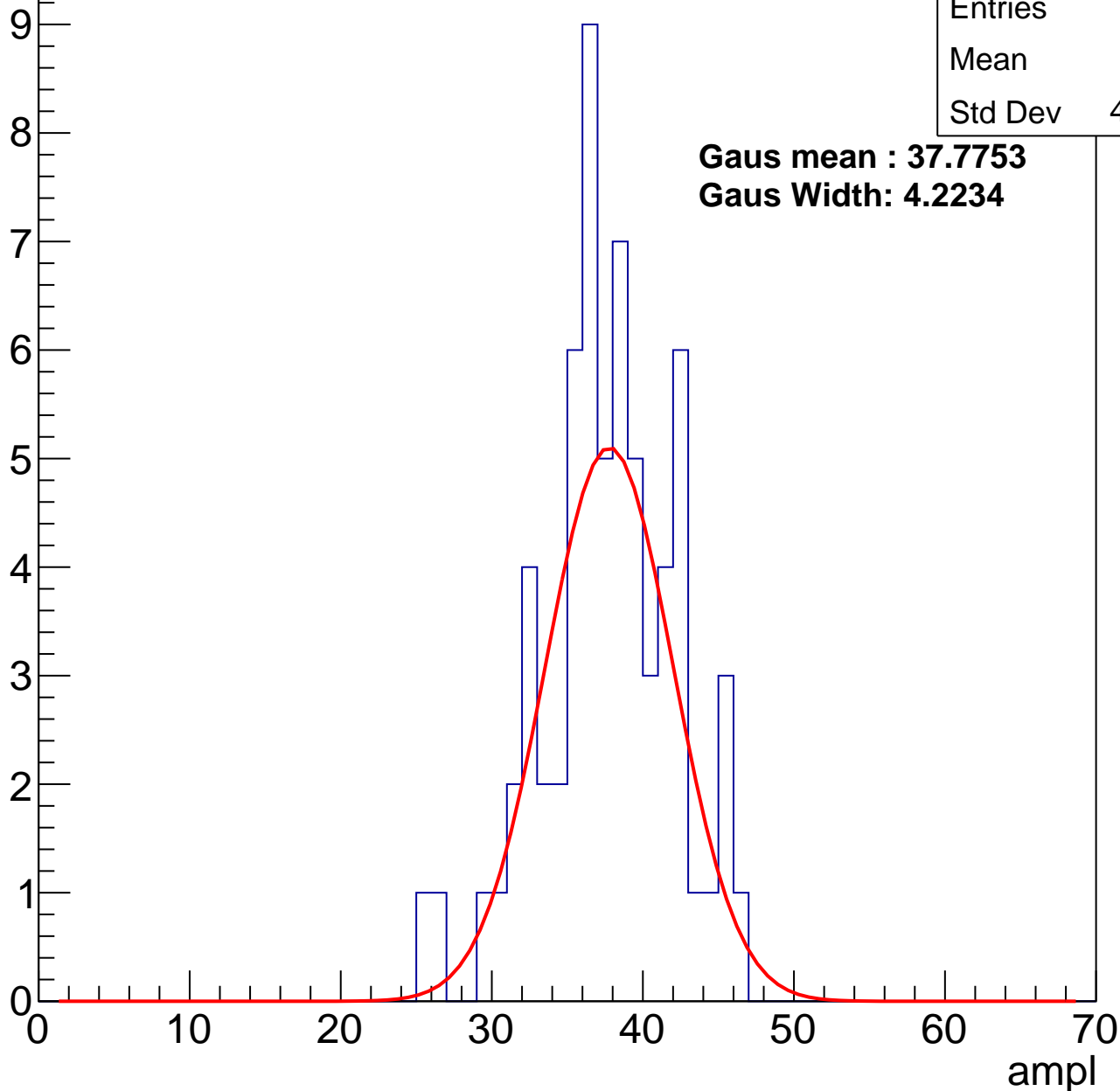
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	65
Mean	37.2
Std Dev	4.397

**Gaus mean : 37.7753**

**Gaus Width: 4.2234**



# B1L100S, U2-ch114, adc2

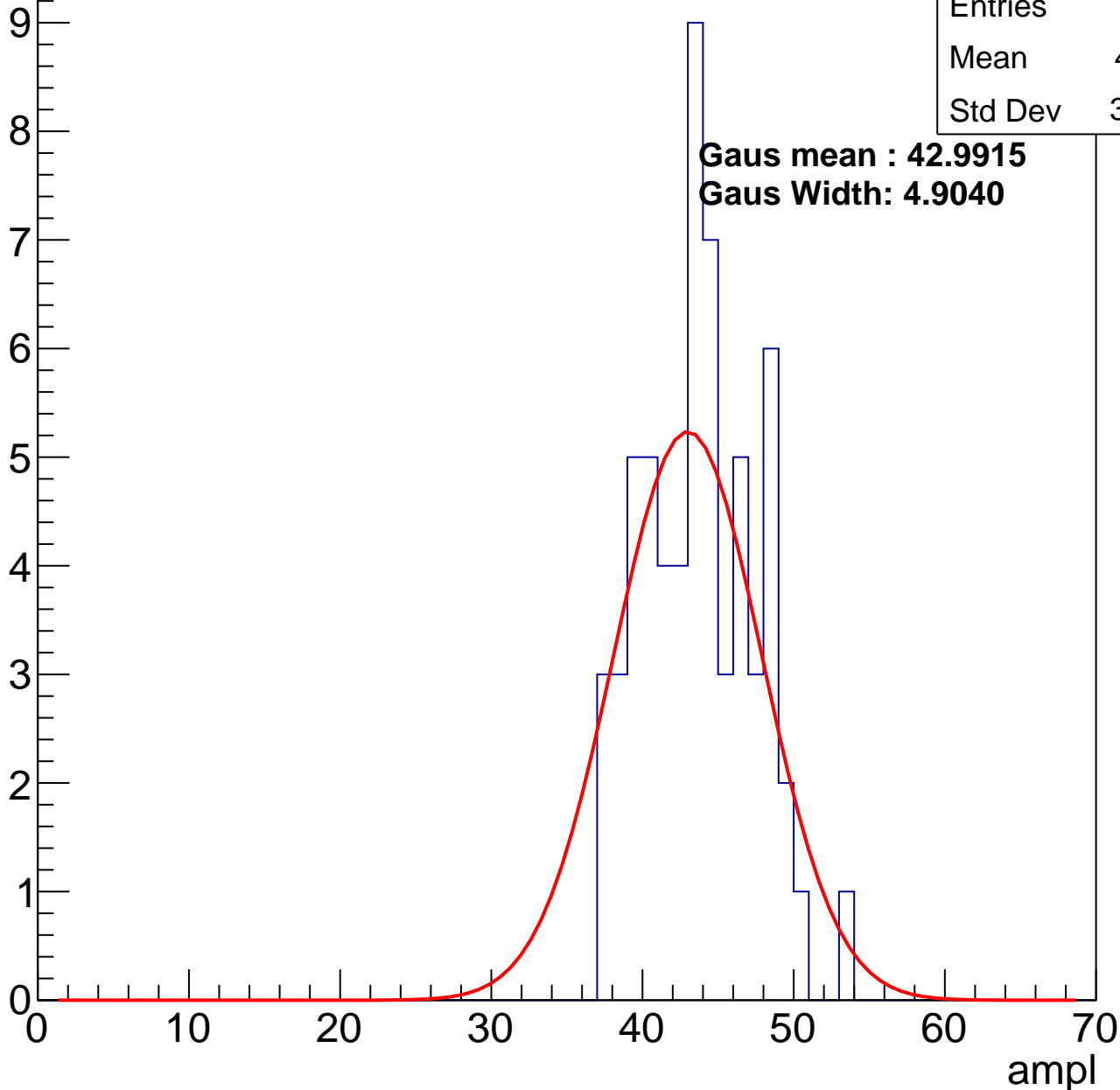
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	61
Mean	43.31
Std Dev	3.633

**Gaus mean : 42.9915**

**Gaus Width: 4.9040**

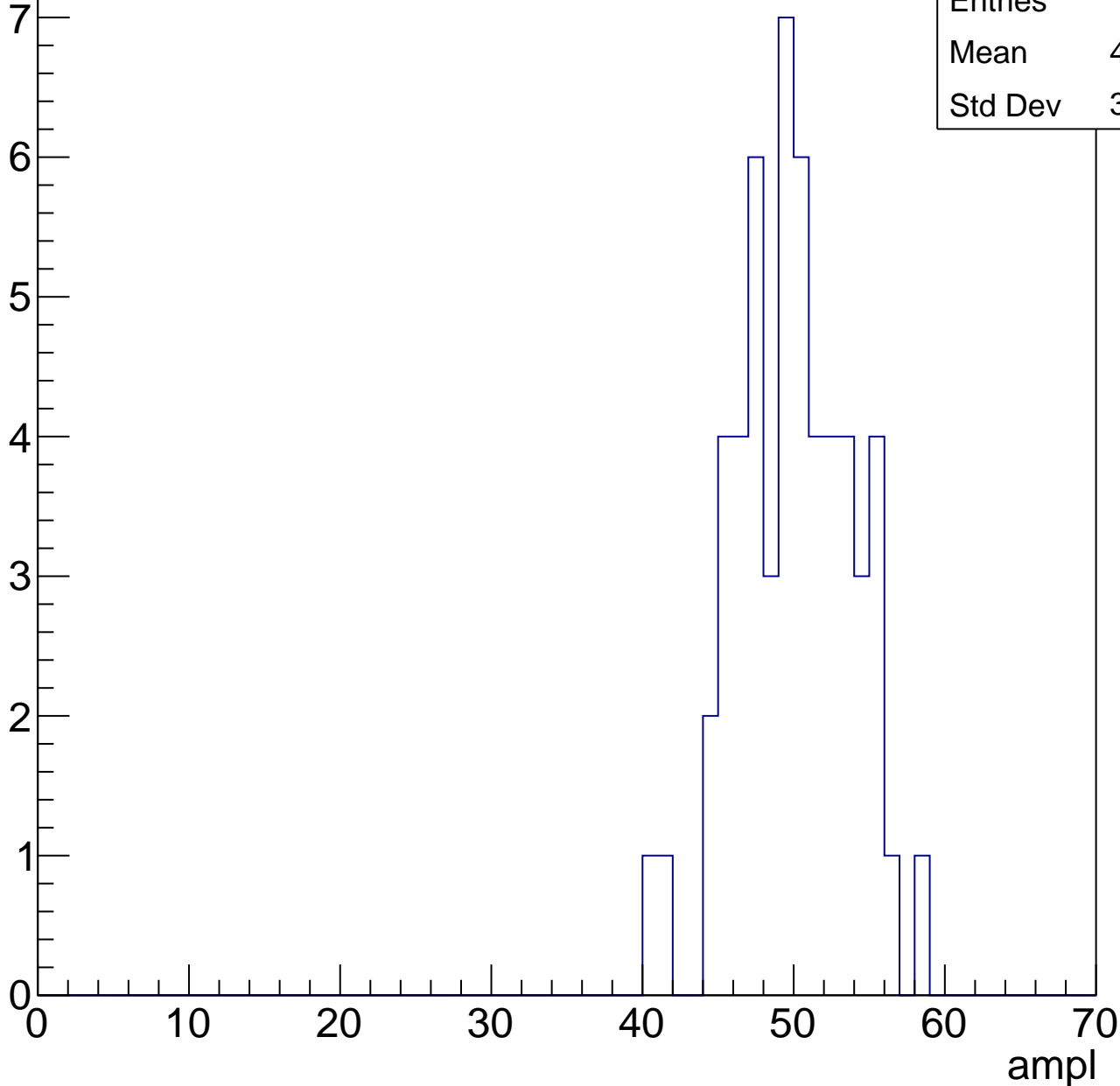


# B1L100S, U2-ch114, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	55
Mean	49.49
Std Dev	3.765



# B1L100S, U2-ch114, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

10

8

6

4

2

0

0

10

20

30

40

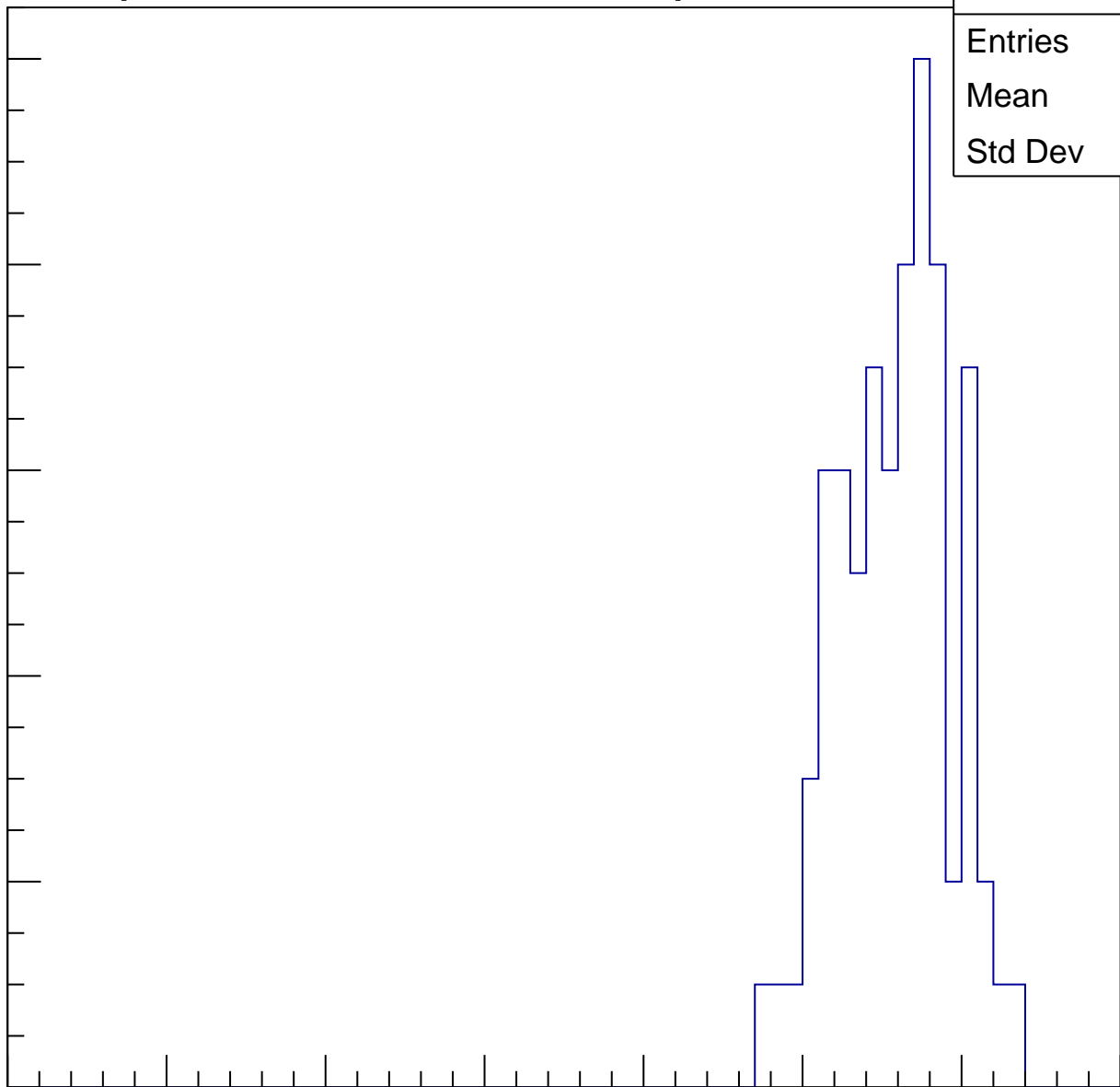
50

60

70

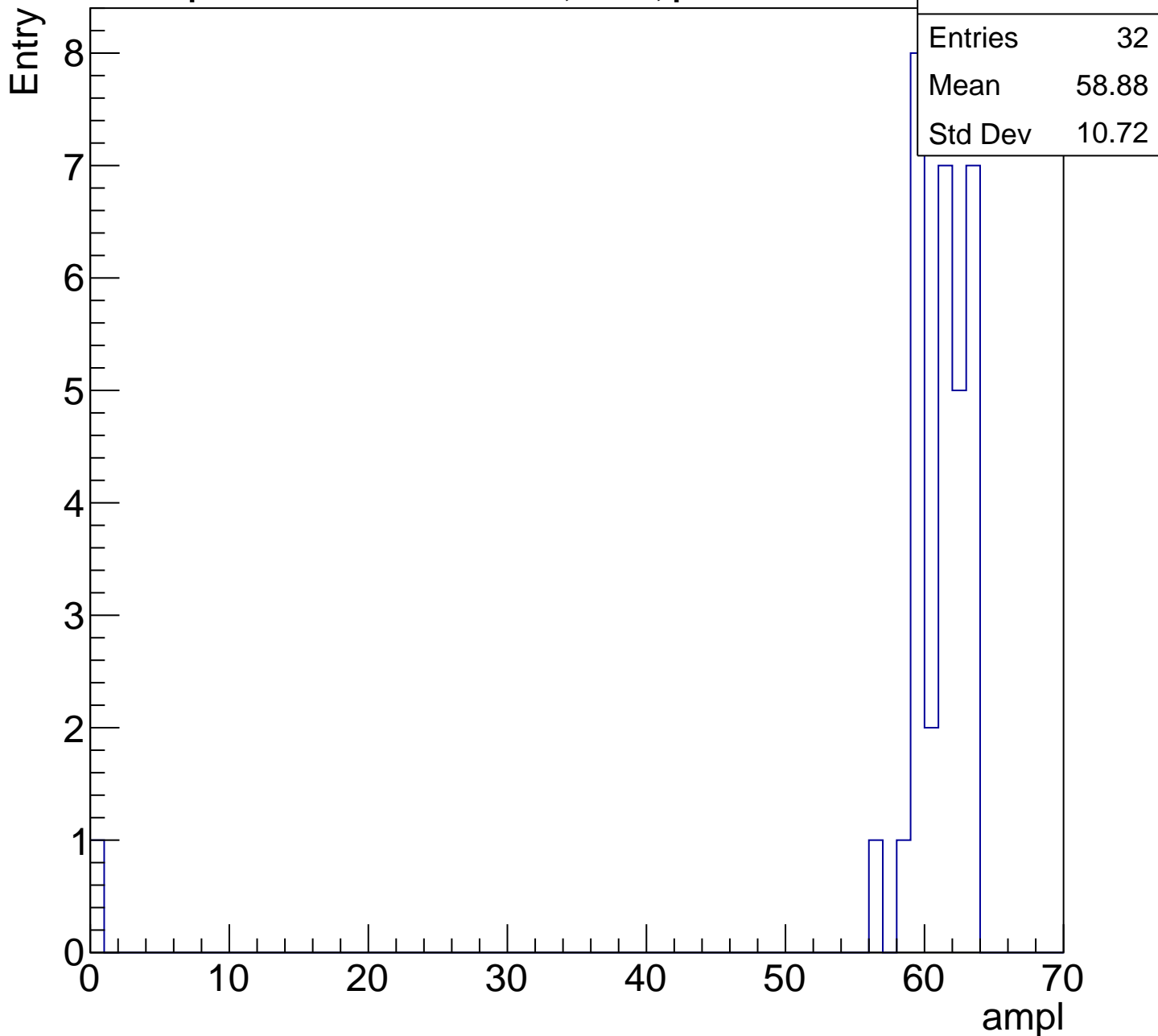
ampl

Entries	75
Mean	55.36
Std Dev	3.47



# B1L100S, U2-ch114, adc5

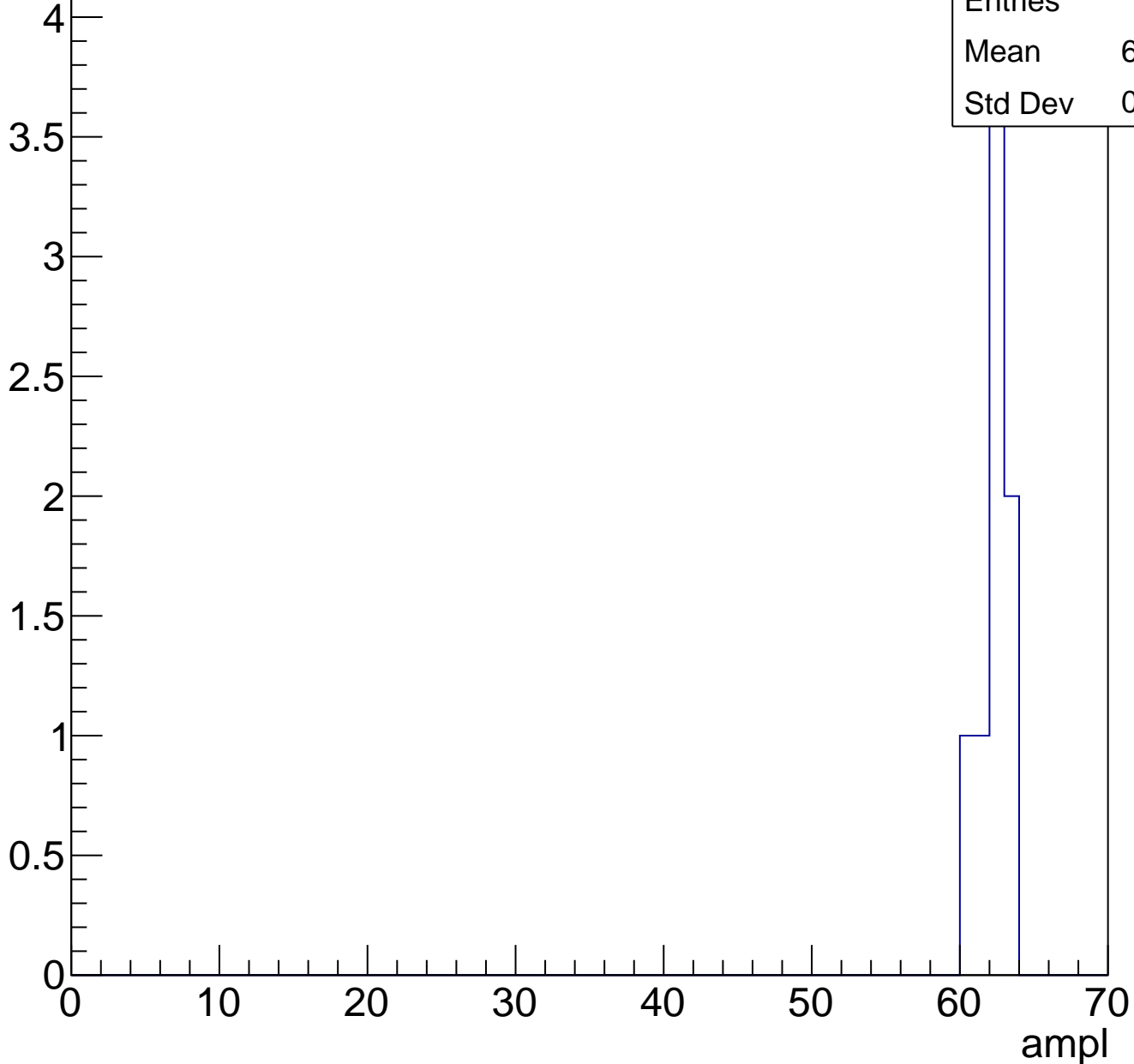
calib\_packv5\_042523\_0143.root, FC#4, port A2



# B1L100S, U2-ch114, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry





# B1L100S, U2-ch114, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L100S, U2-ch115, adc0

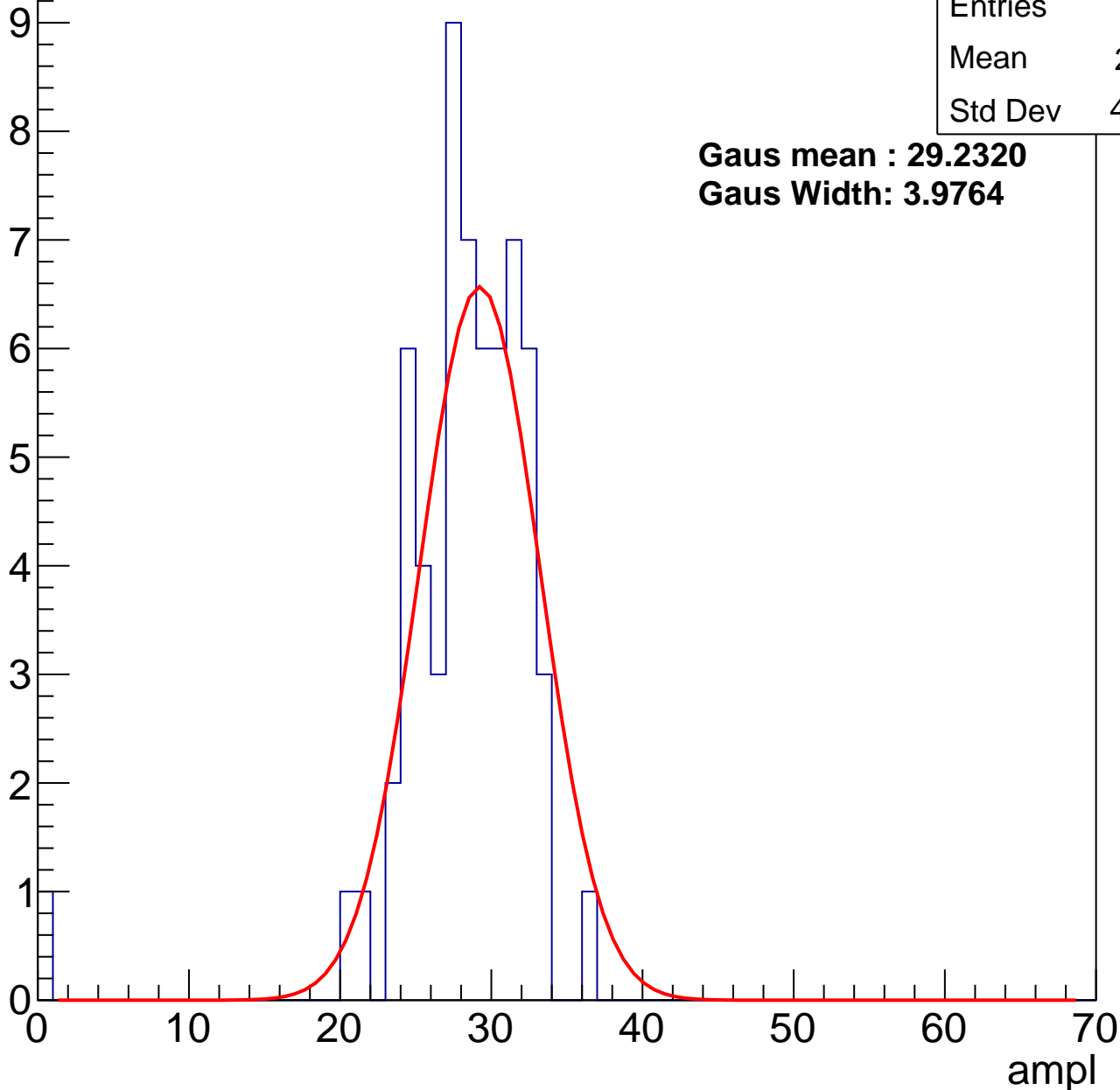
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	63
Mean	27.71
Std Dev	4.752

**Gaus mean : 29.2320**

**Gaus Width: 3.9764**



# B1L100S, U2-ch115, adc1

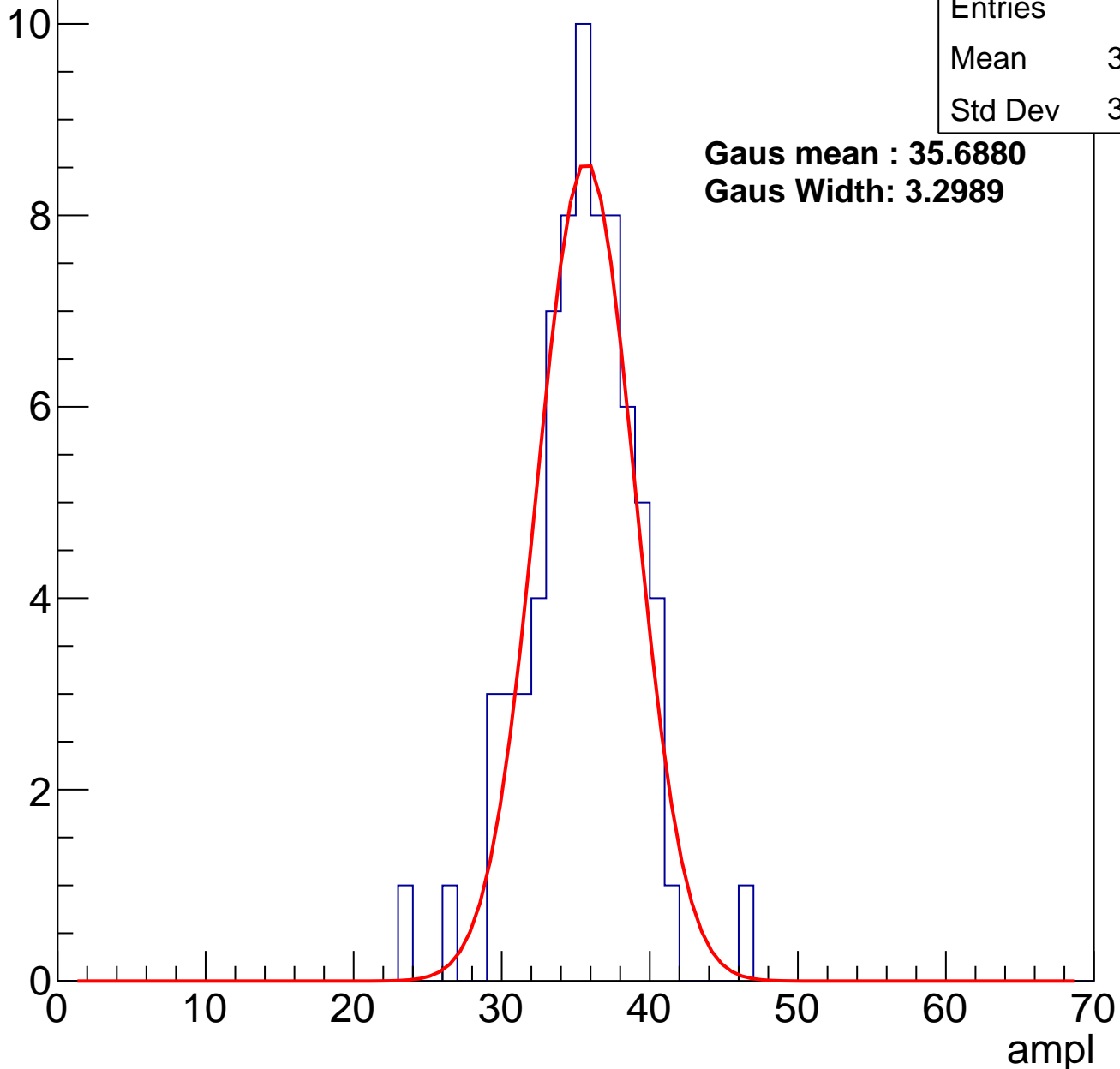
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	73
Mean	34.99
Std Dev	3.624

**Gaus mean : 35.6880**

**Gaus Width: 3.2989**

Entry



# B1L100S, U2-ch115, adc2

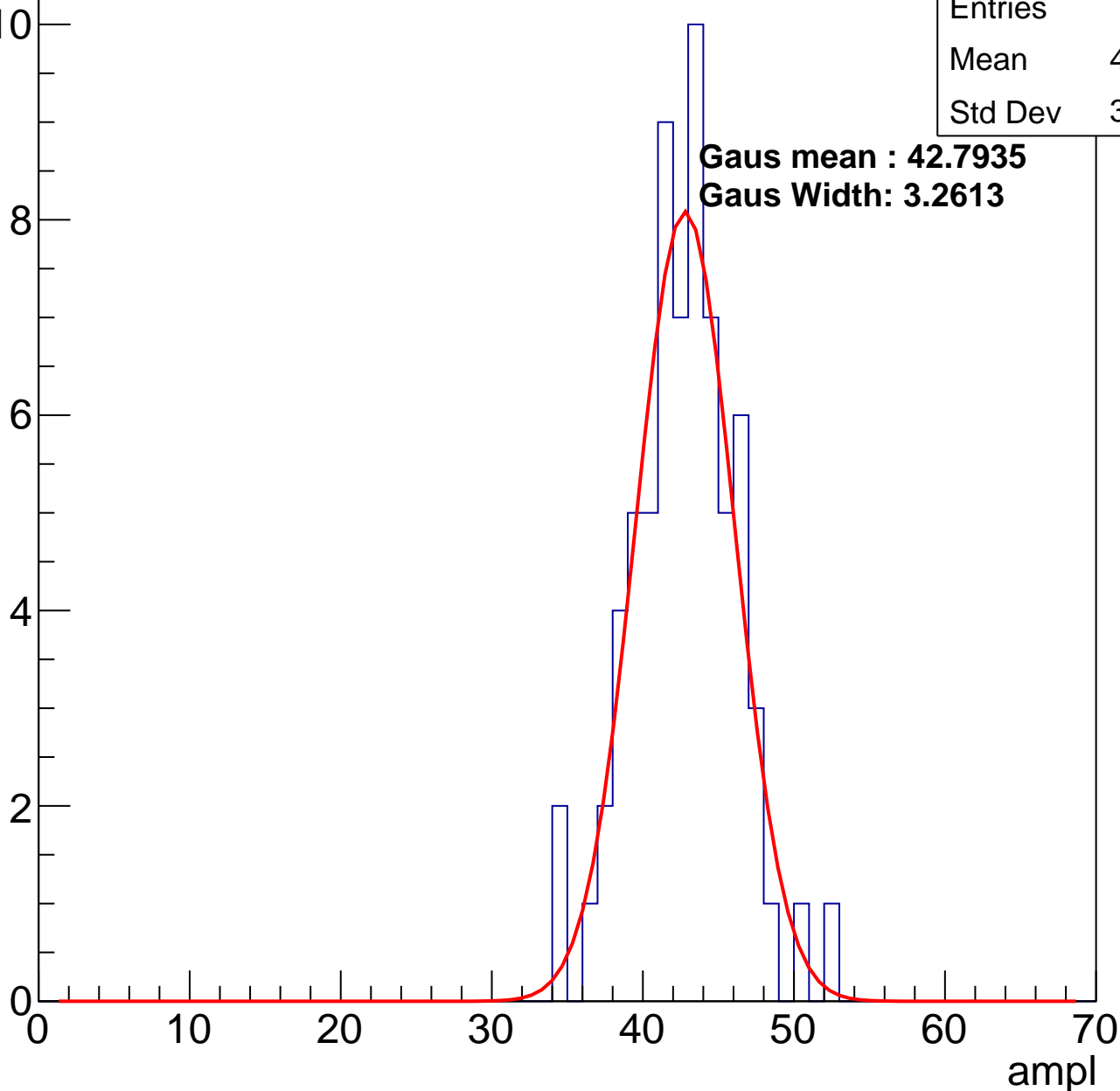
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	69
Mean	42.29
Std Dev	3.405

**Gaus mean : 42.7935**

**Gaus Width: 3.2613**

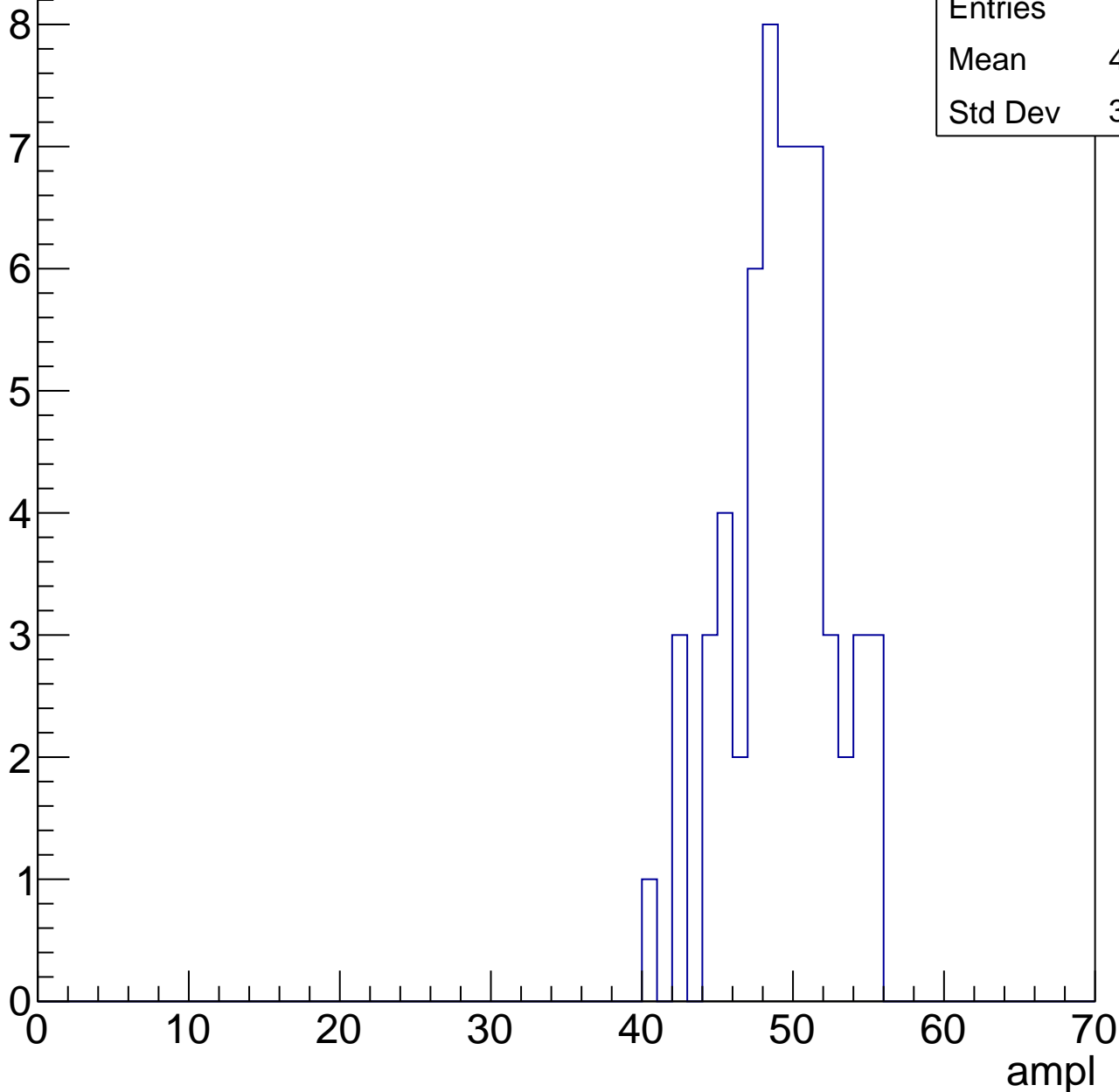


# B1L100S, U2-ch115, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

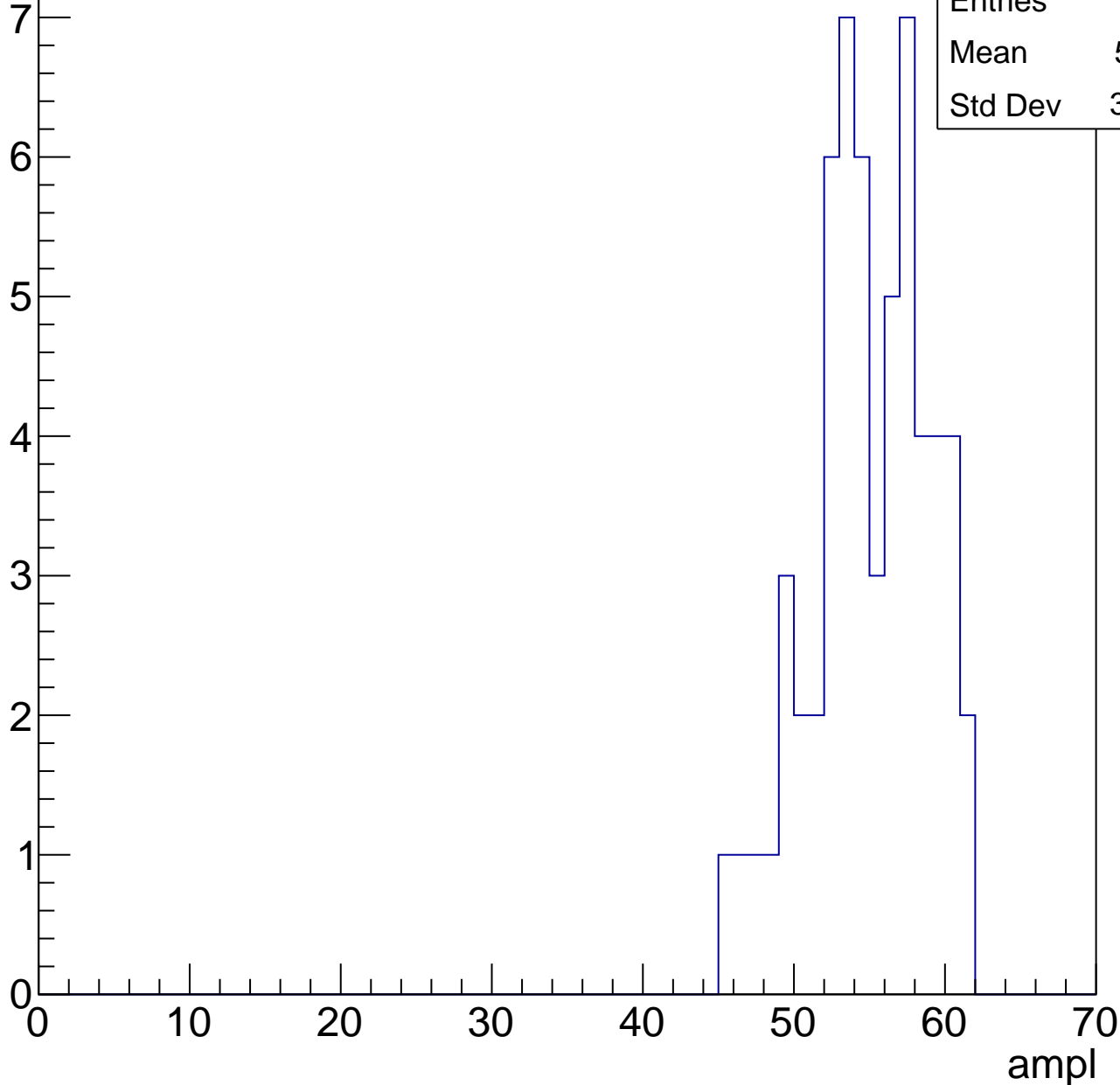
Entries	59
Mean	48.73
Std Dev	3.419



# B1L100S, U2-ch115, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



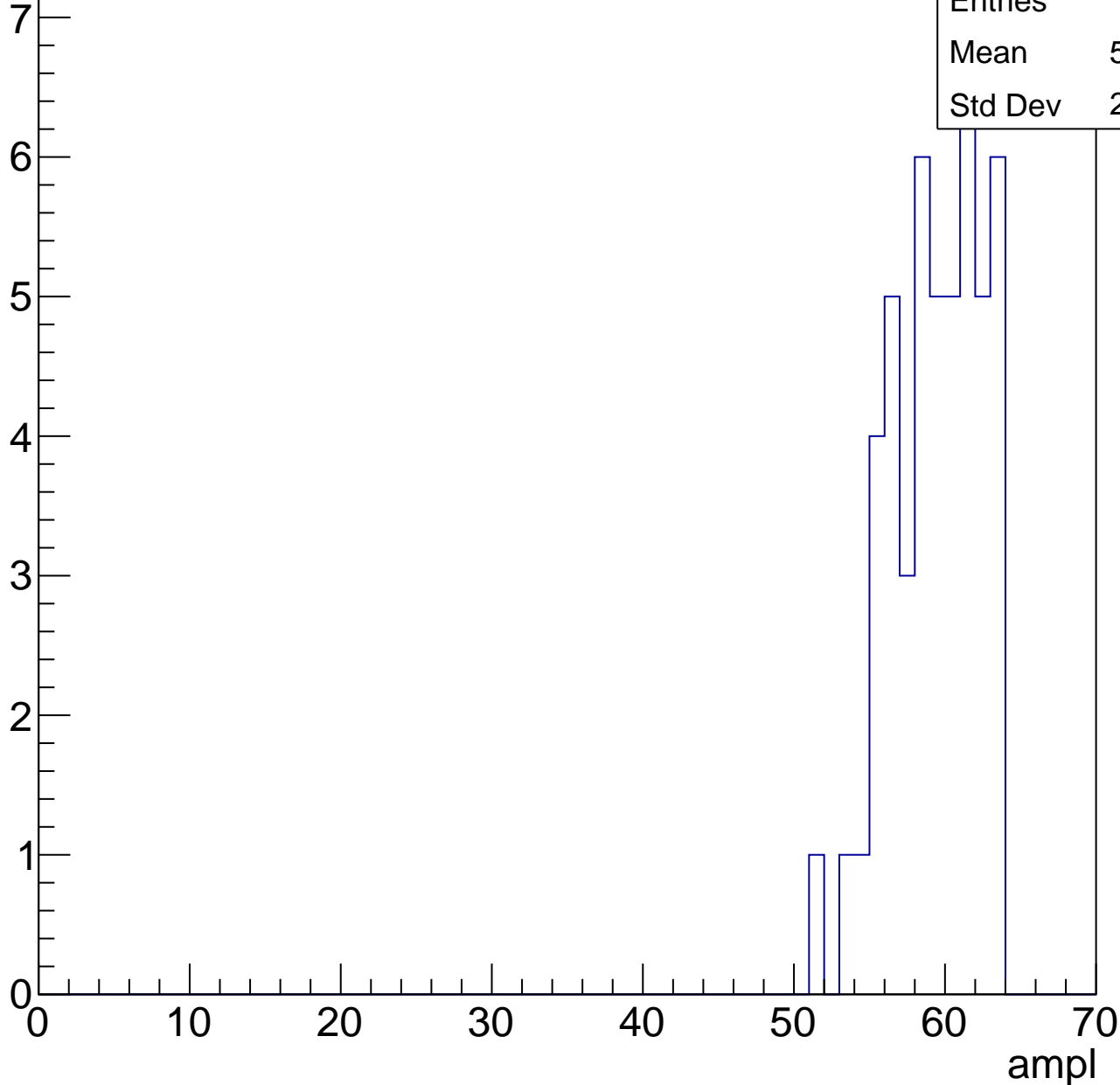
Entries	59
Mean	54.51
Std Dev	3.824

# B1L100S, U2-ch115, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	49
Mean	58.92
Std Dev	2.947

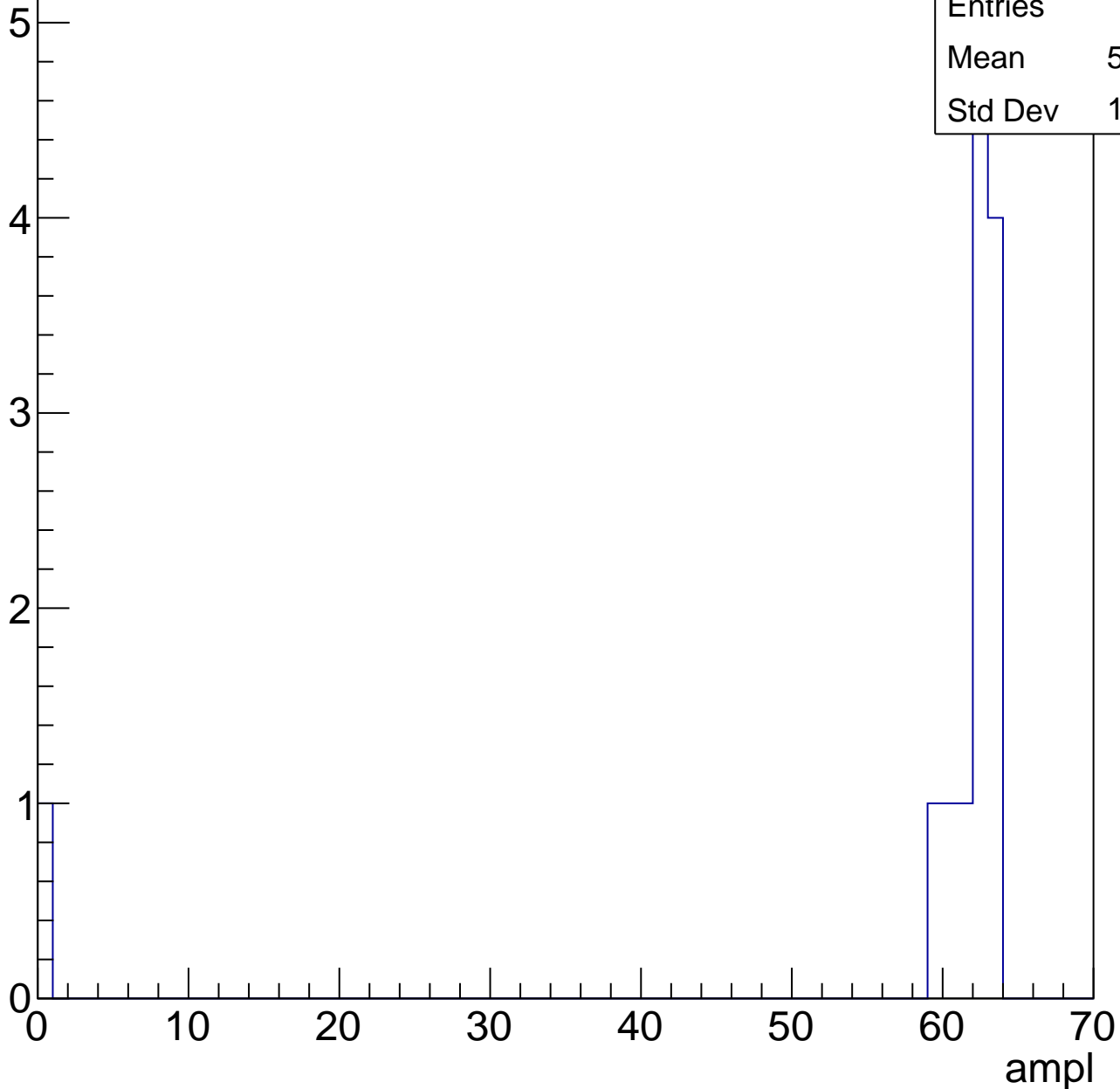


# B1L100S, U2-ch115, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	13
Mean	57.08
Std Dev	16.52





# B1L100S, U2-ch115, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



# B1L100S, U2-ch116, adc0

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	84
Mean	29.35
Std Dev	4.886

**Gaus mean : 29.7222**

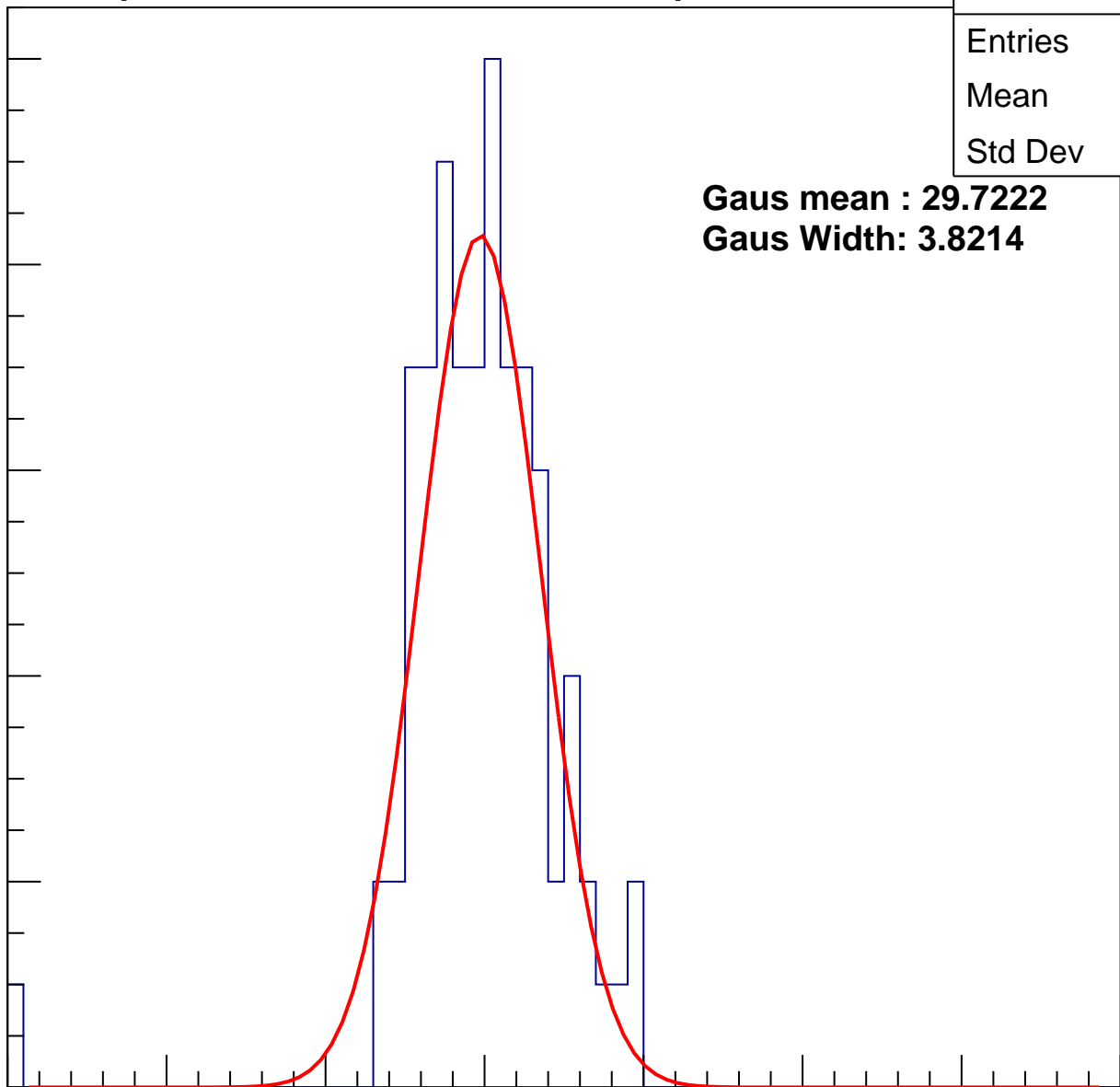
**Gaus Width: 3.8214**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L100S, U2-ch116, adc1

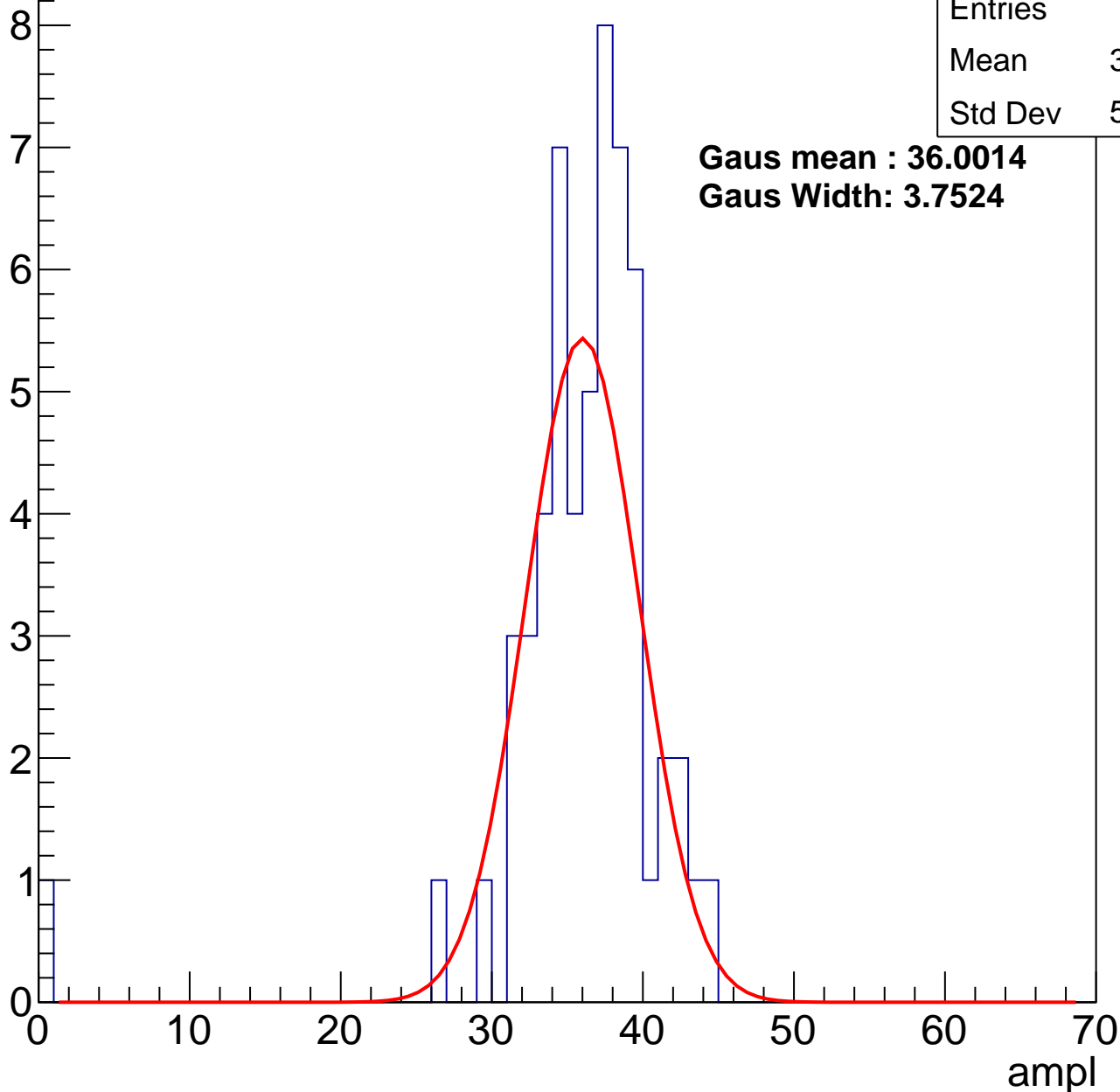
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	57
Mean	35.49
Std Dev	5.867

**Gaus mean : 36.0014**

**Gaus Width: 3.7524**



# B1L100S, U2-ch116, adc2

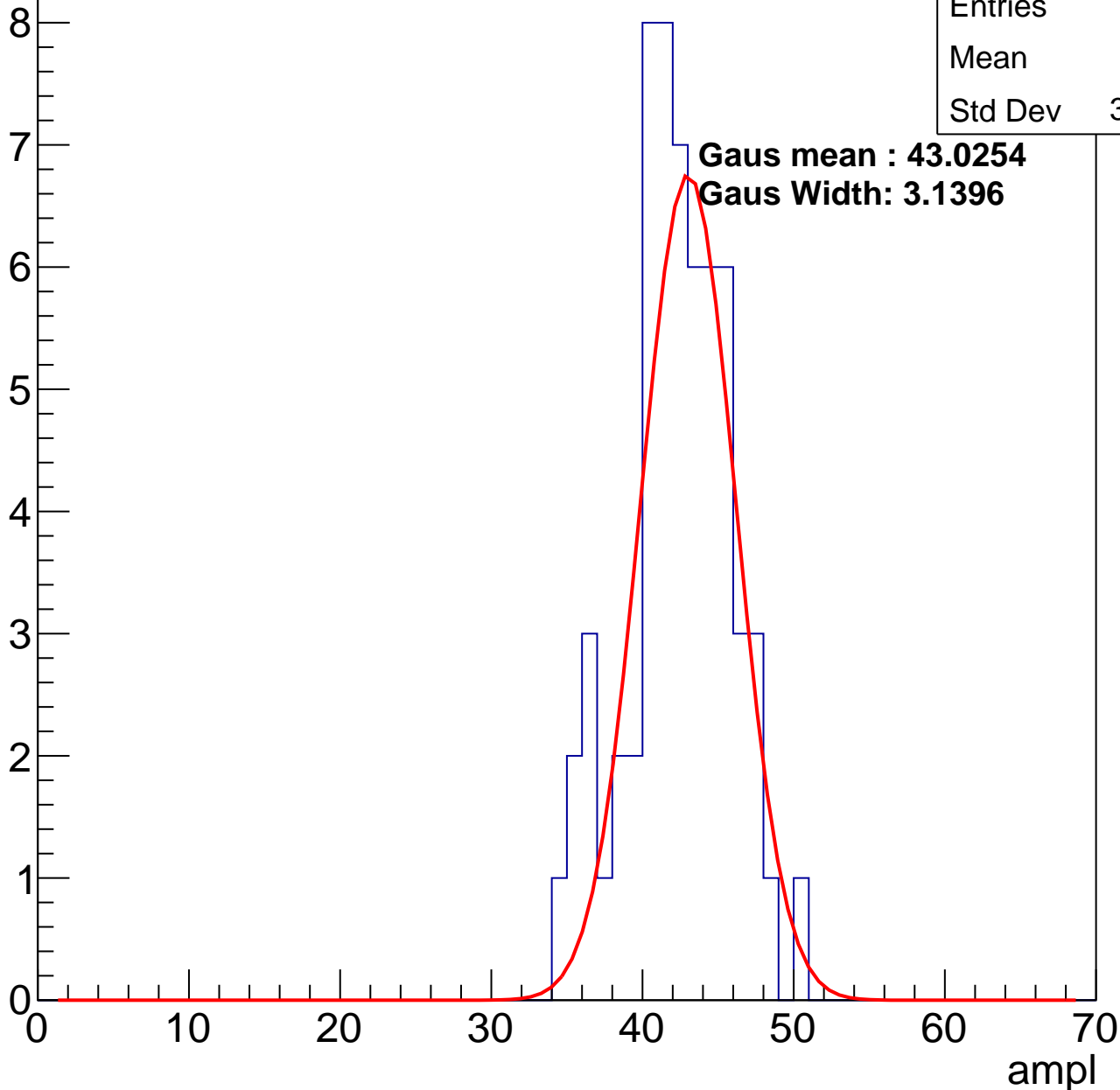
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	60
Mean	41.9
Std Dev	3.395

**Gaus mean : 43.0254**

**Gaus Width: 3.1396**

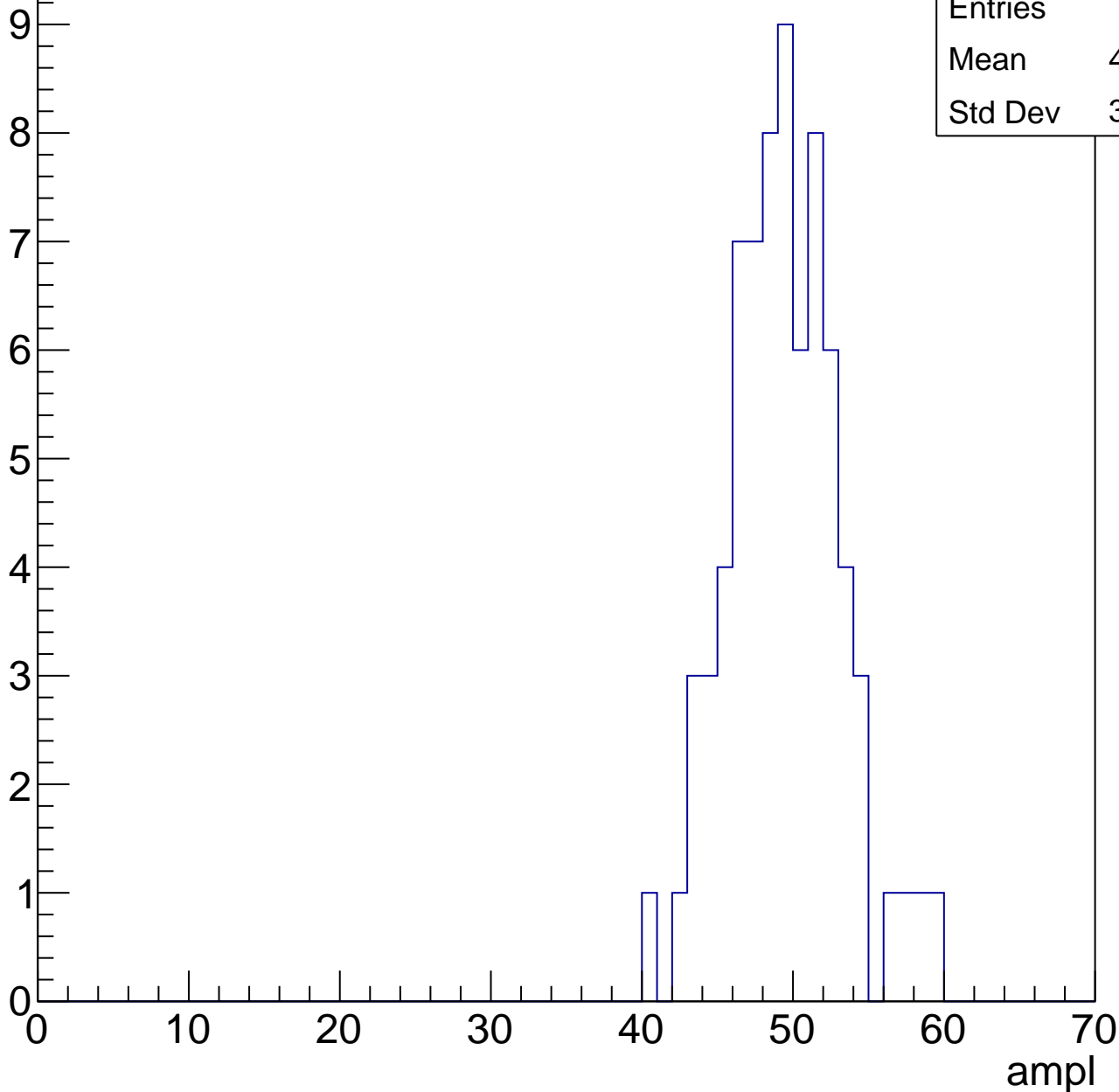


# B1L100S, U2-ch116, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	74
Mean	48.96
Std Dev	3.678

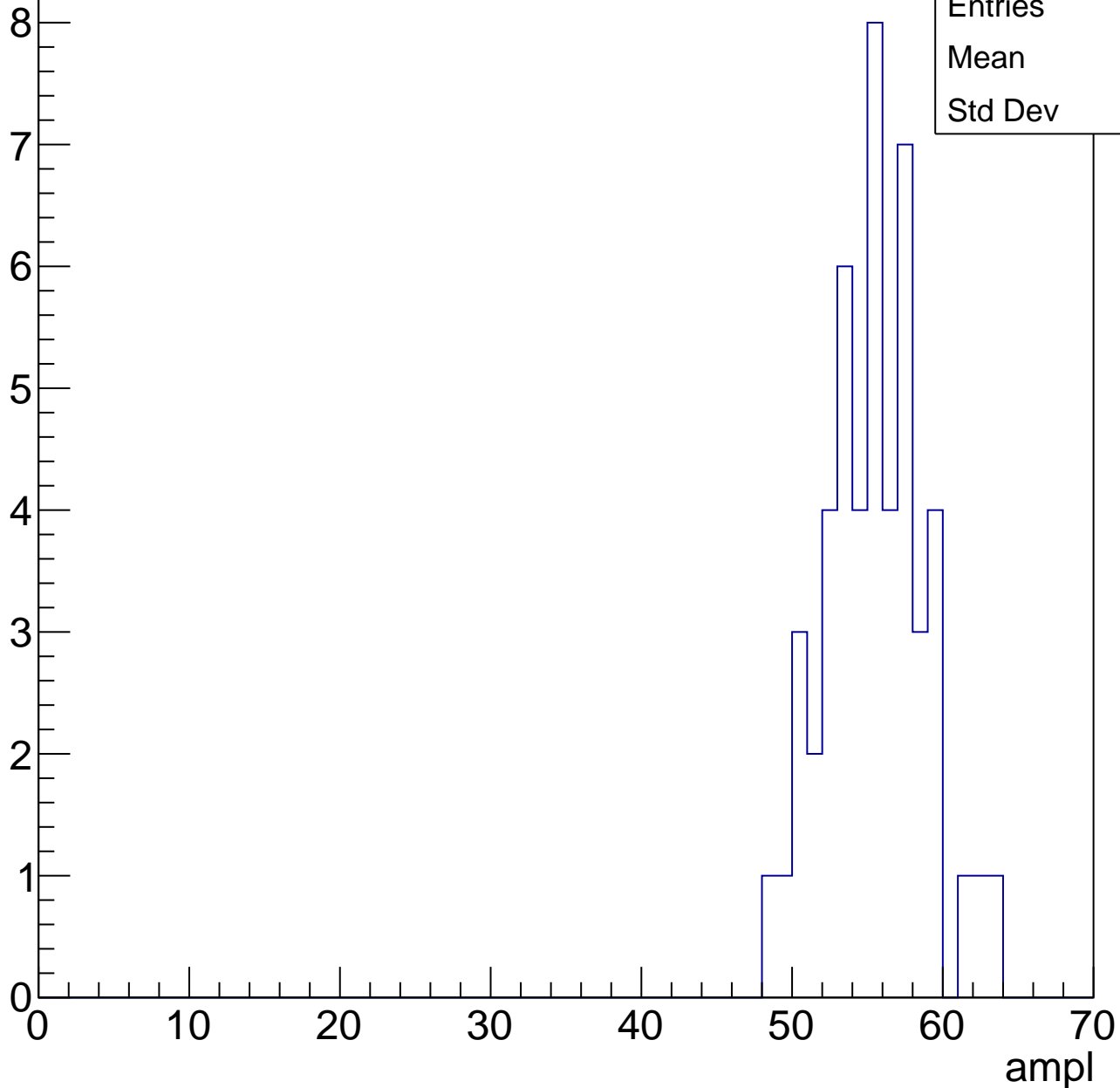


# B1L100S, U2-ch116, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

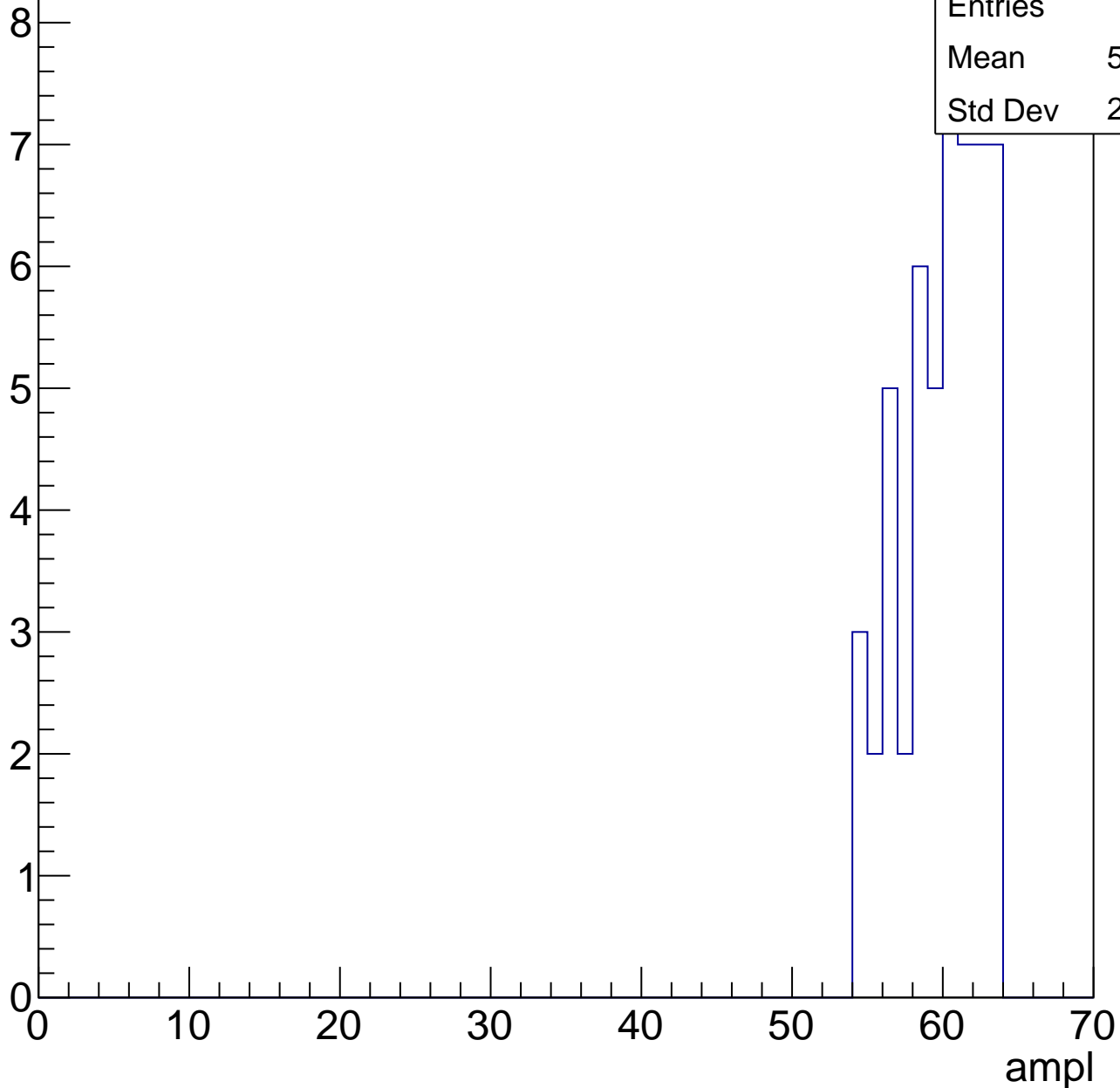
Entries	50
Mean	55
Std Dev	3.25



# B1L100S, U2-ch116, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



# B1L100S, U2-ch116, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	9
Mean	54.67
Std Dev	19.36

0 10 20 30 40 50 60 70

ampl



# B1L100S, U2-ch116, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L100S, U2-ch117, adc0

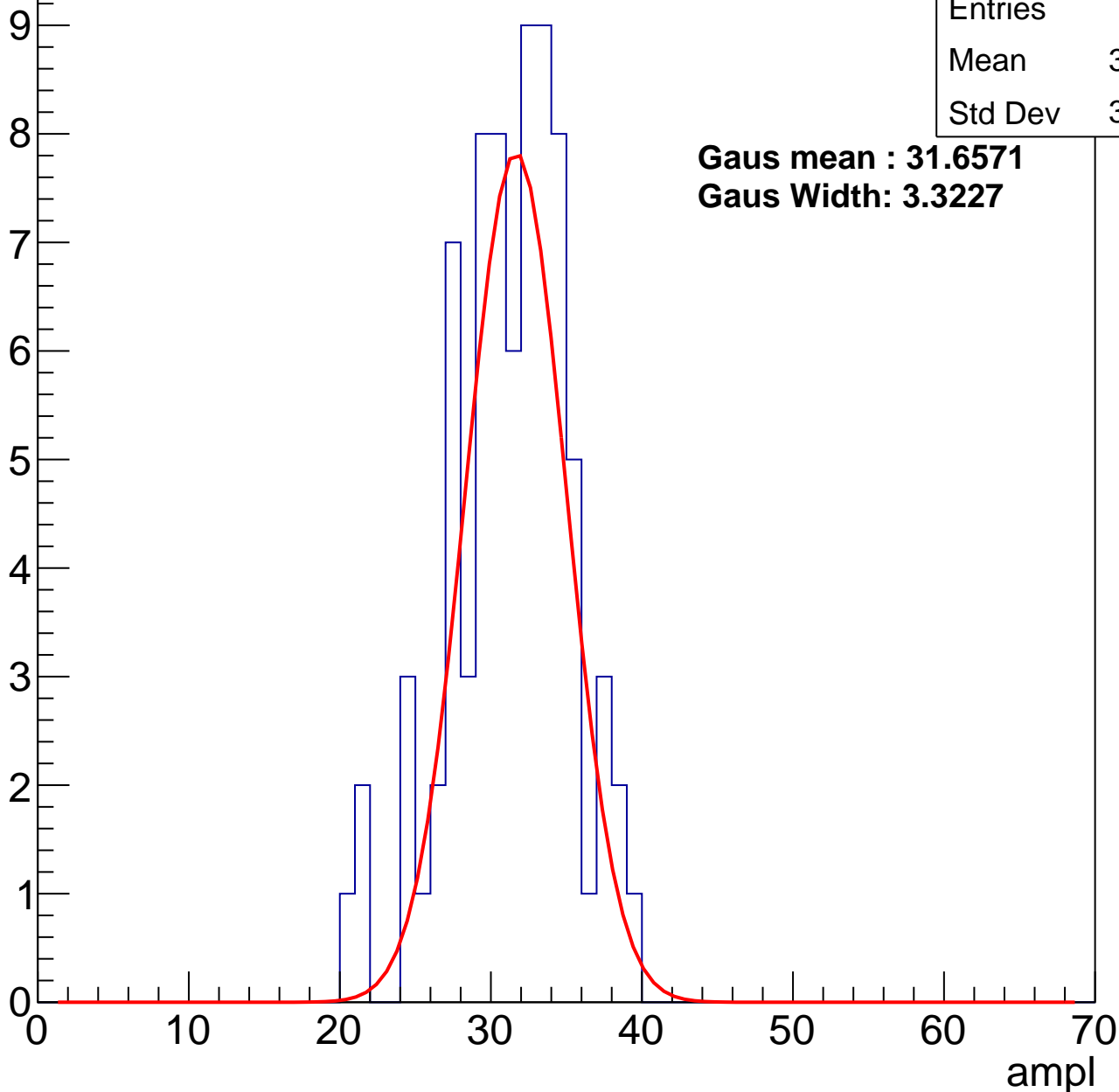
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	79
Mean	30.84
Std Dev	3.934

**Gaus mean : 31.6571**

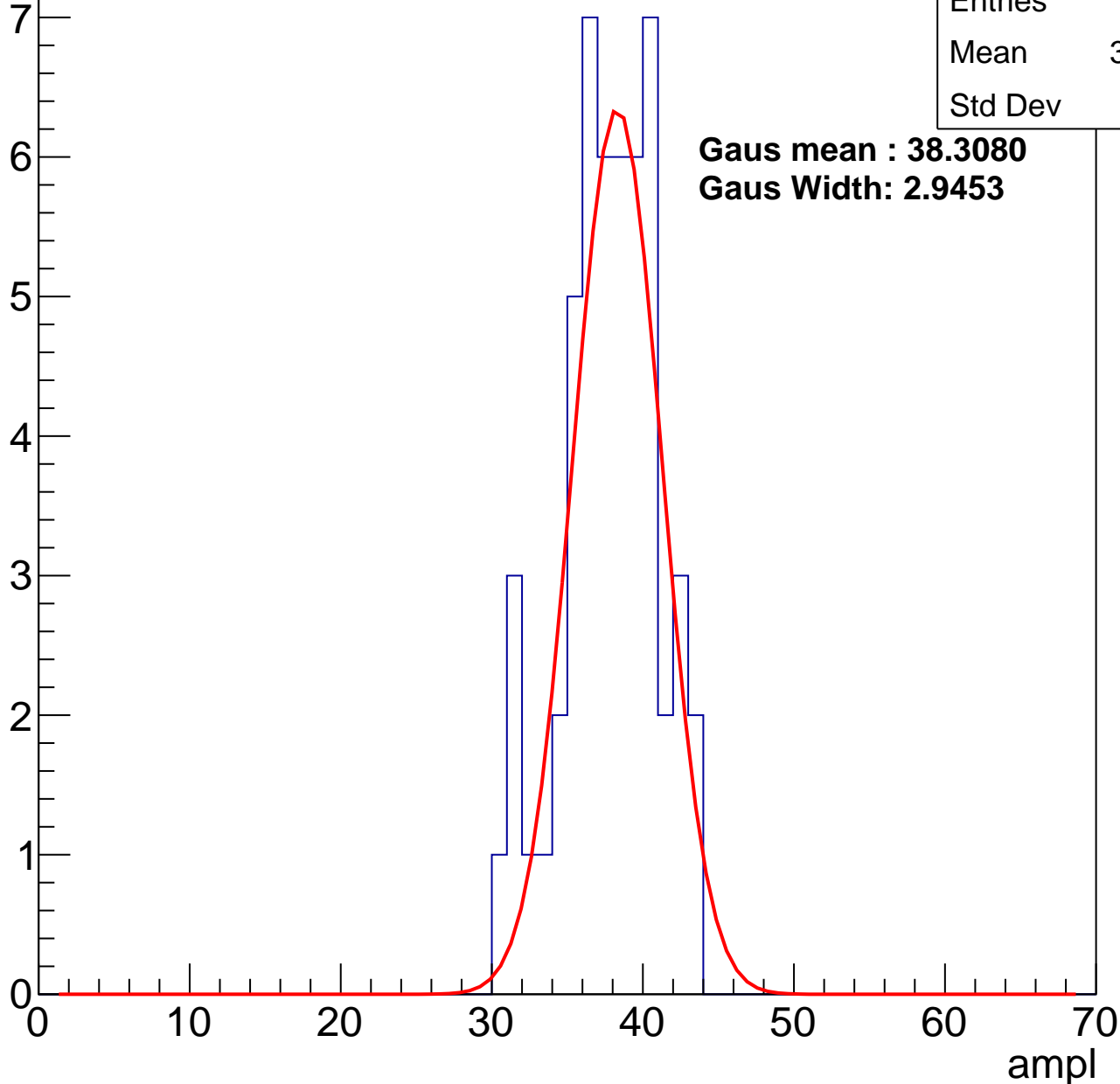
**Gaus Width: 3.3227**



# B1L100S, U2-ch117, adc1

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



# B1L100S, U2-ch117, adc2

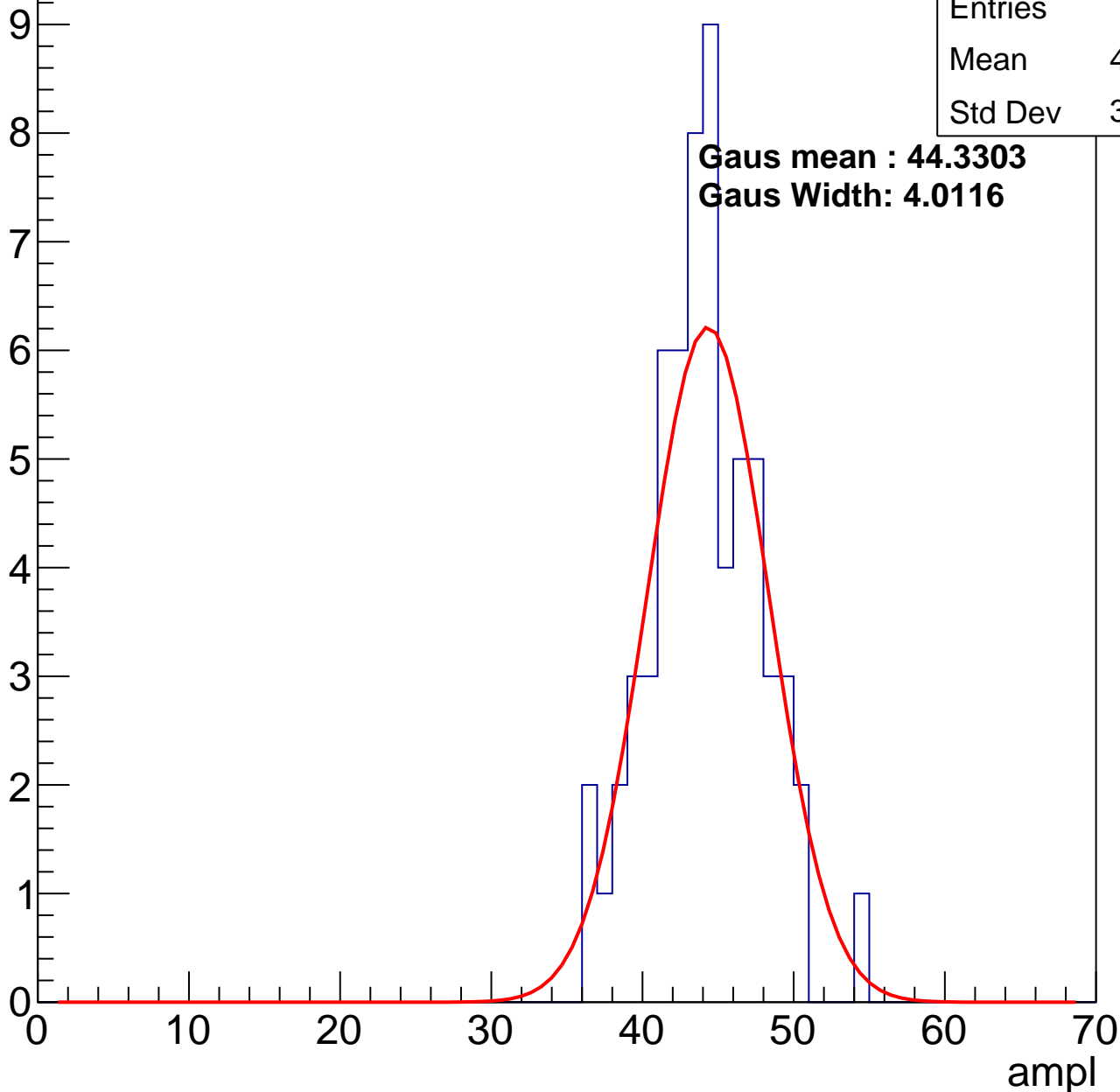
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	63
Mean	43.65
Std Dev	3.595

**Gaus mean : 44.3303**

**Gaus Width: 4.0116**

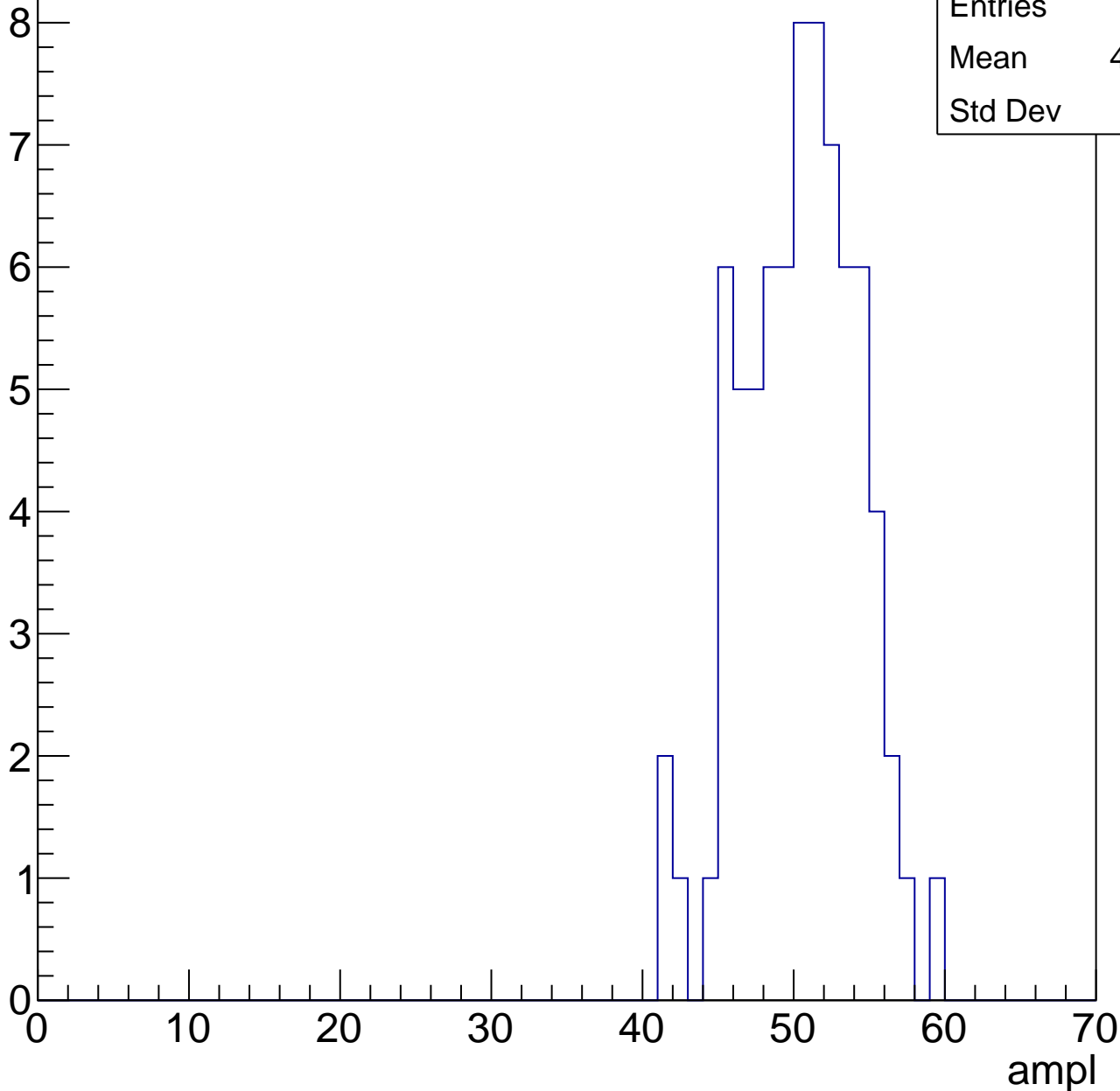


# B1L100S, U2-ch117, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

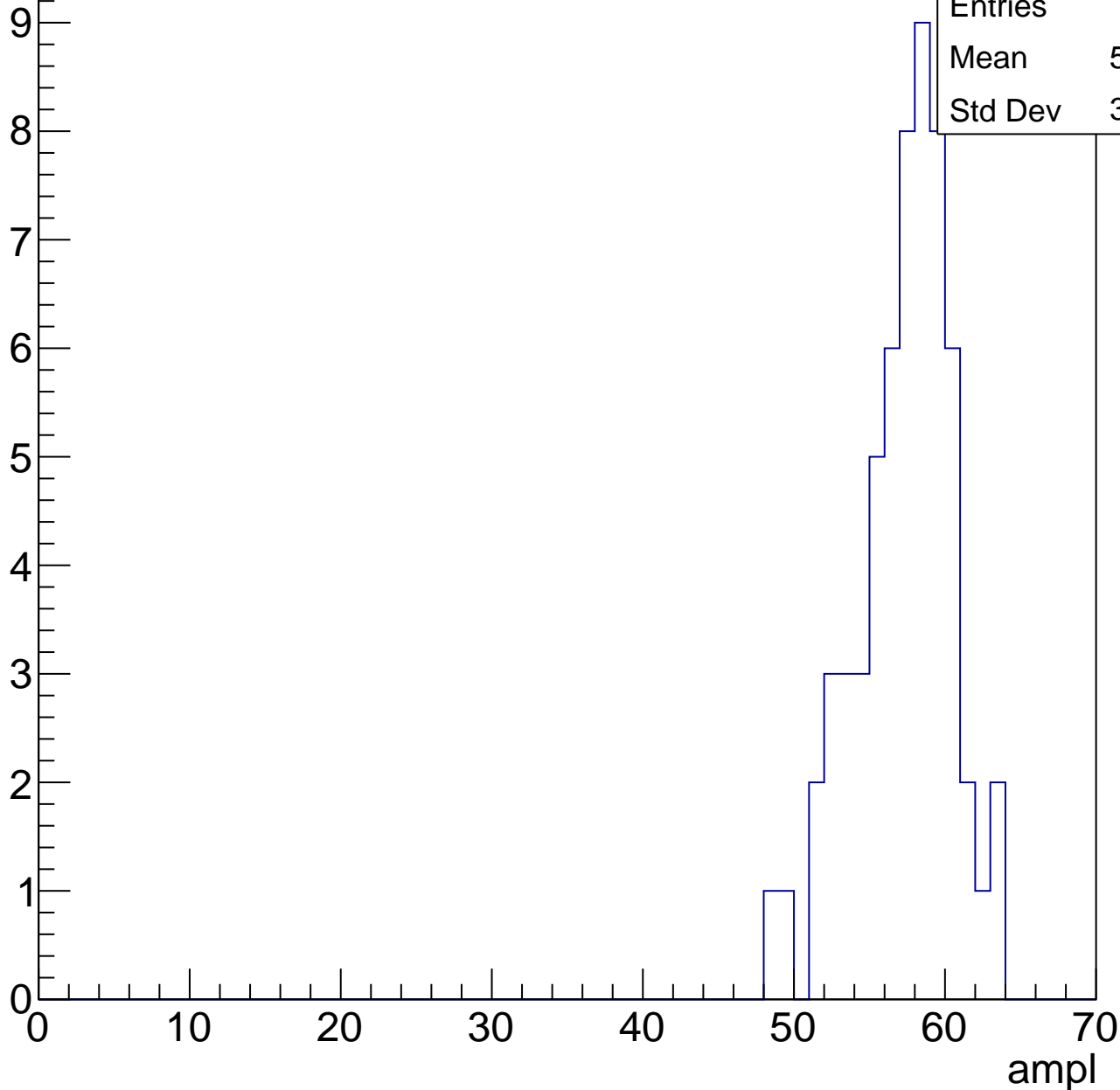
Entries	75
Mean	49.96
Std Dev	3.75



# B1L100S, U2-ch117, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

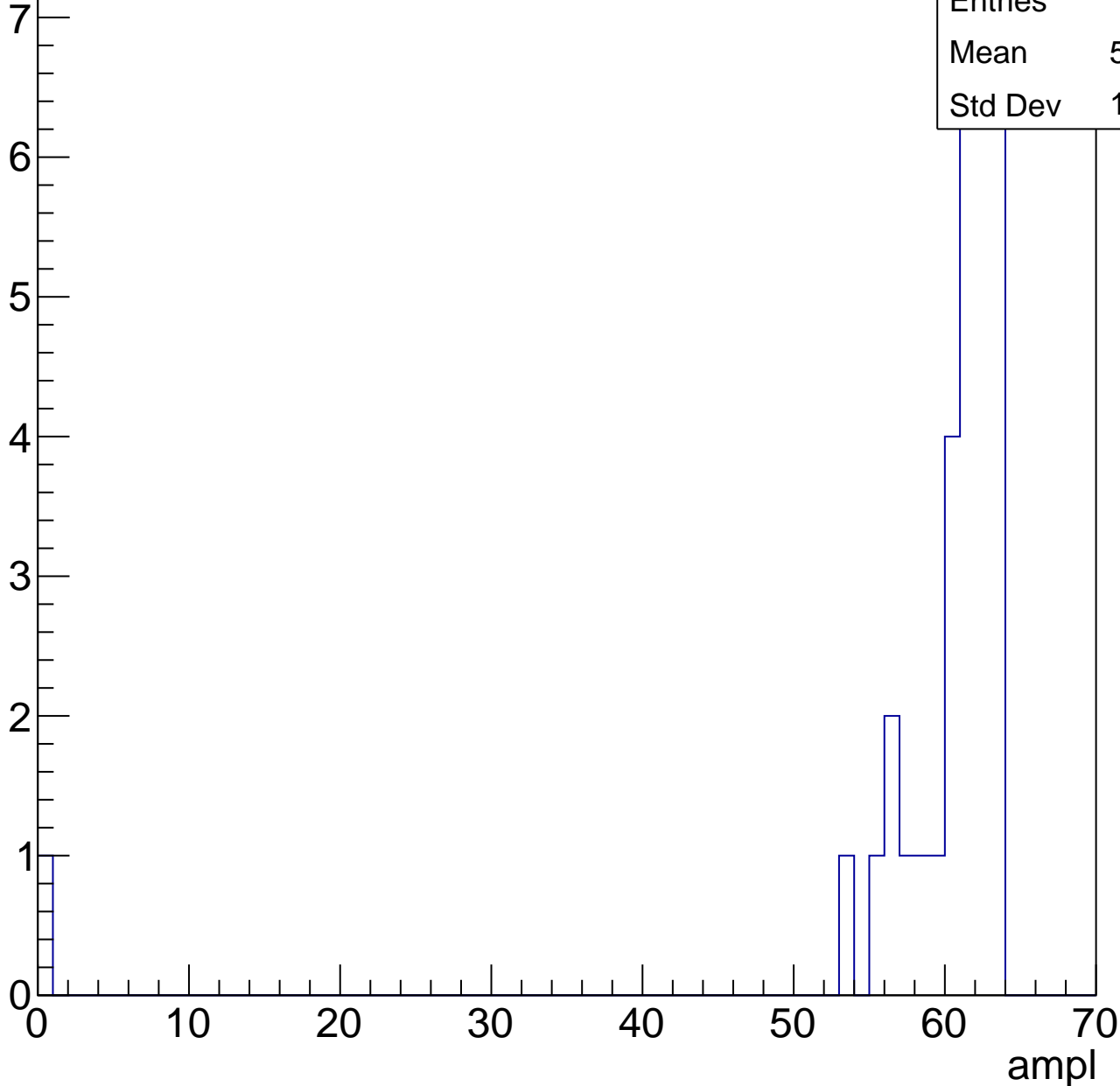


# B1L100S, U2-ch117, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	33
Mean	58.67
Std Dev	10.67



# B1L100S, U2-ch117, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry





# B1L100S, U2-ch117, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



# B1L100S, U2-ch118, adc0

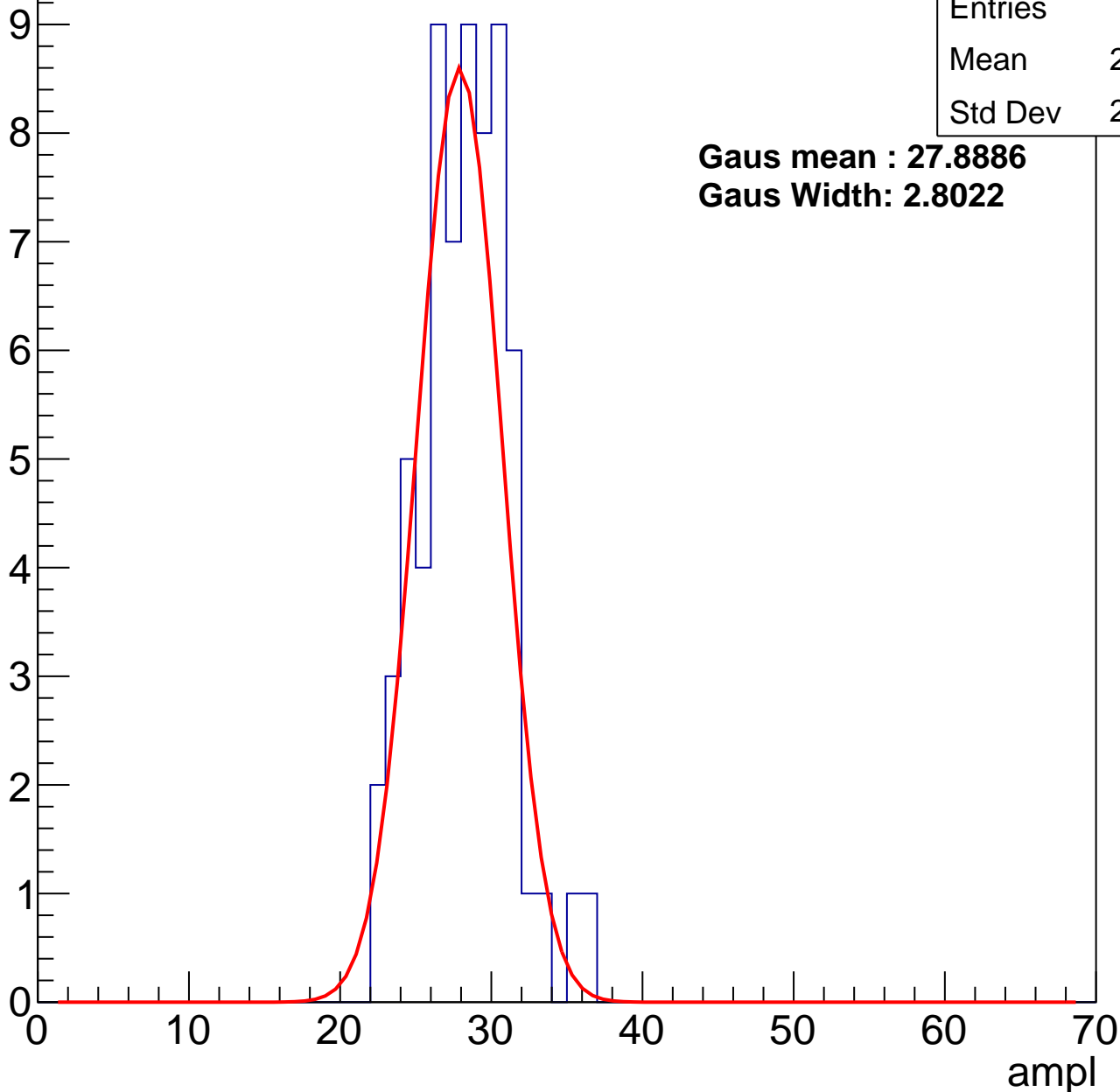
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	66
Mean	27.76
Std Dev	2.898

**Gaus mean : 27.8886**

**Gaus Width: 2.8022**



# B1L100S, U2-ch118, adc1

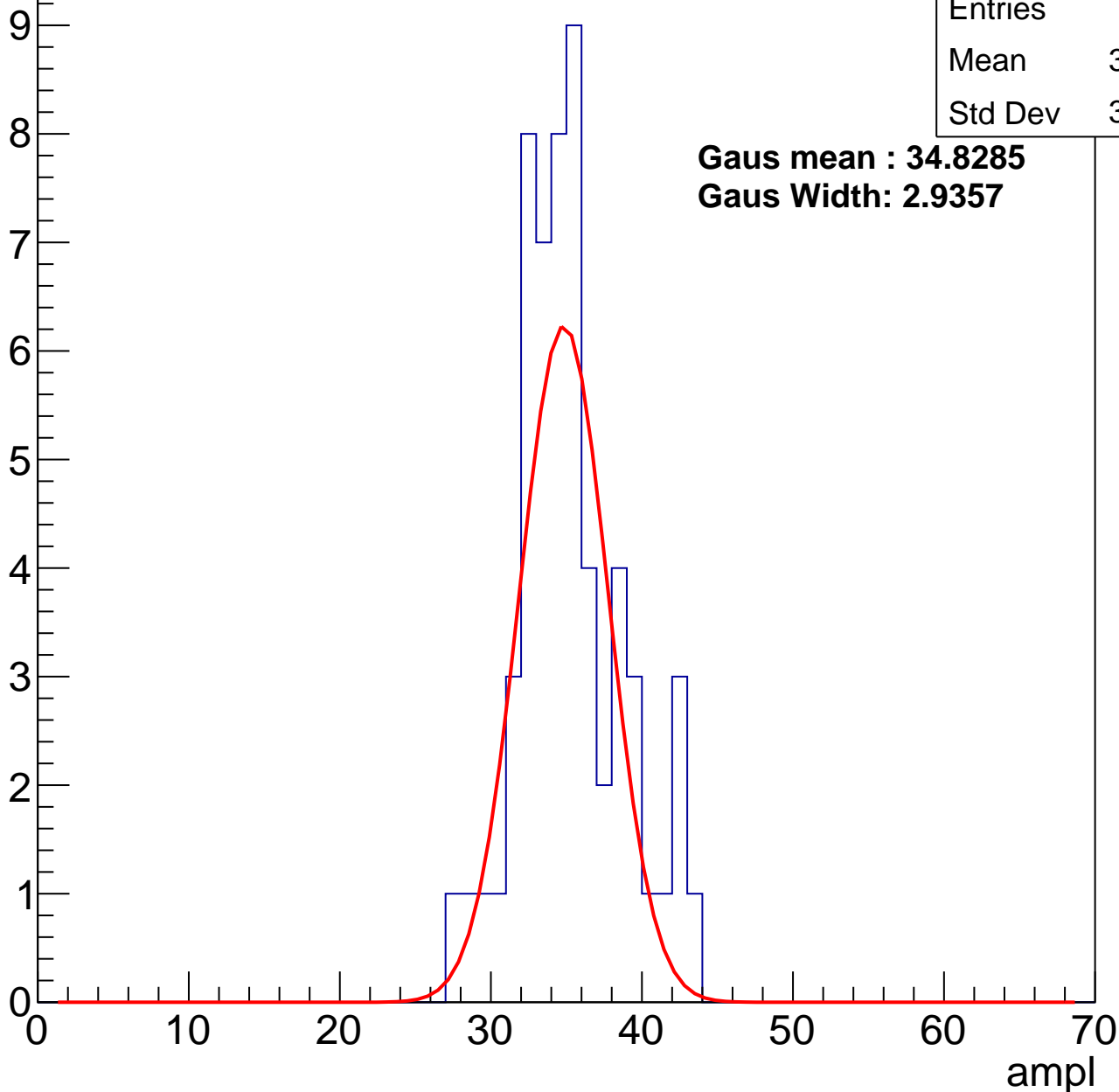
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	58
Mean	34.79
Std Dev	3.463

**Gaus mean : 34.8285**

**Gaus Width: 2.9357**



# B1L100S, U2-ch118, adc2

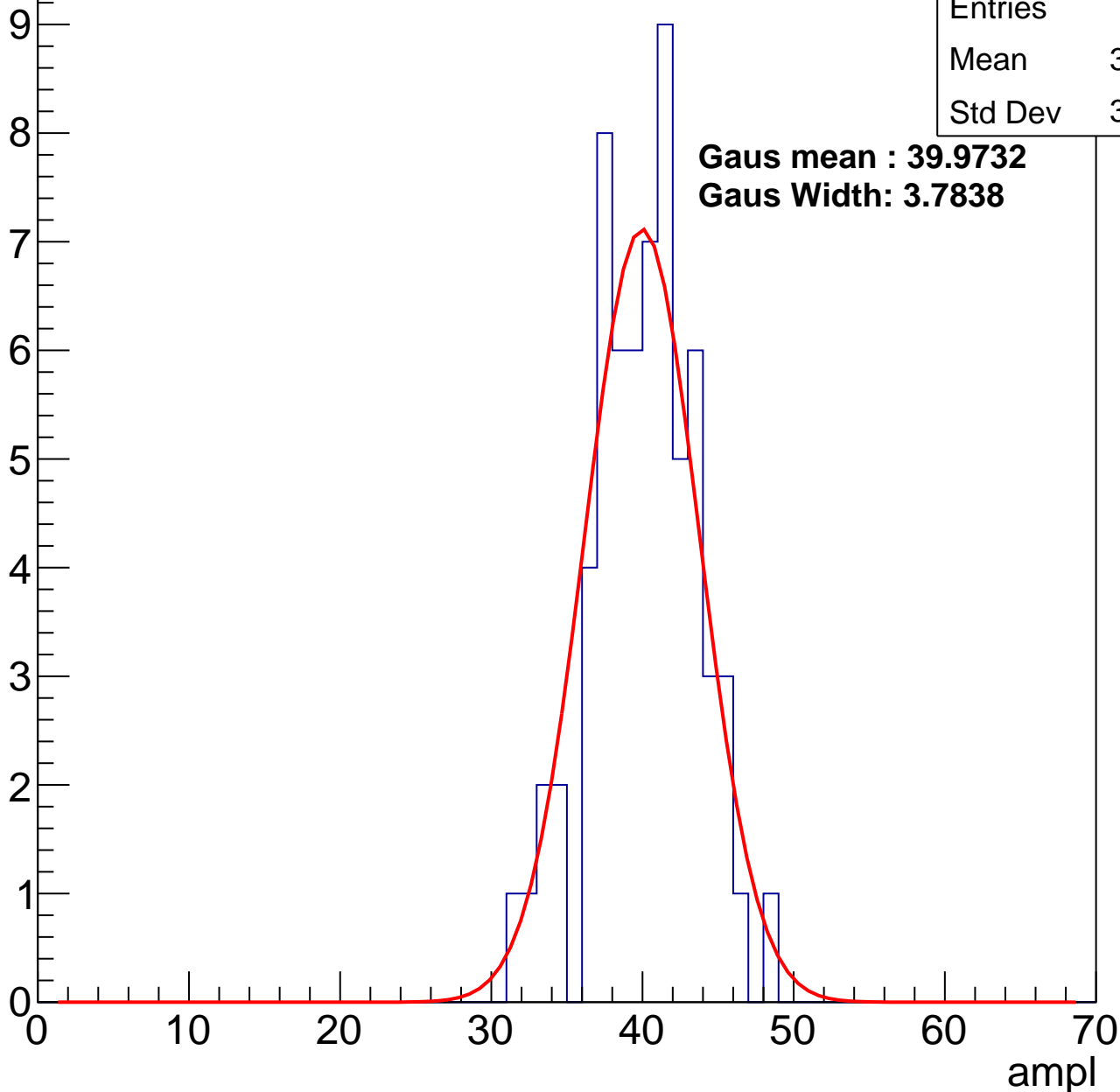
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	65
Mean	39.65
Std Dev	3.462

**Gaus mean : 39.9732**

**Gaus Width: 3.7838**

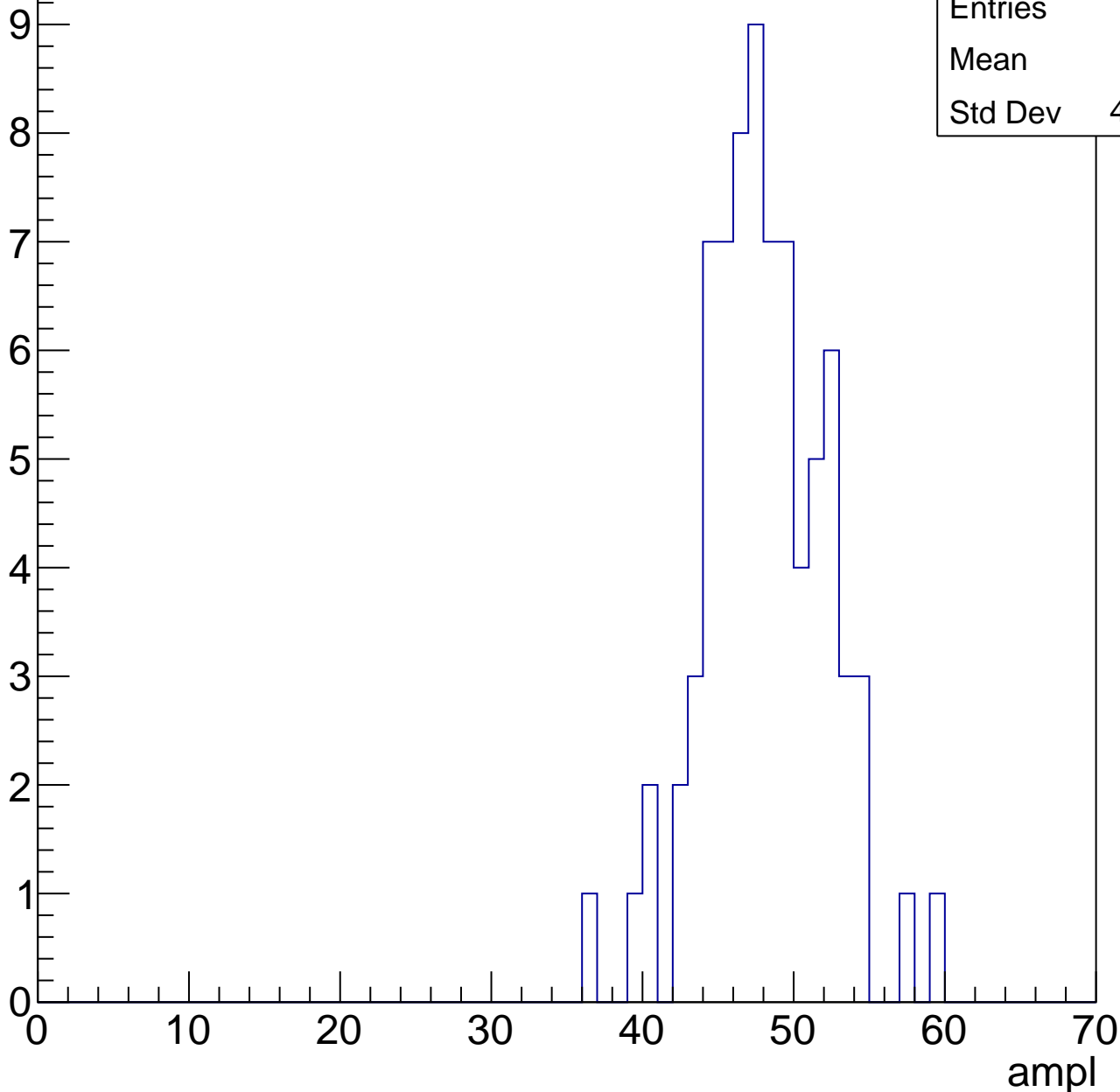


# B1L100S, U2-ch118, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

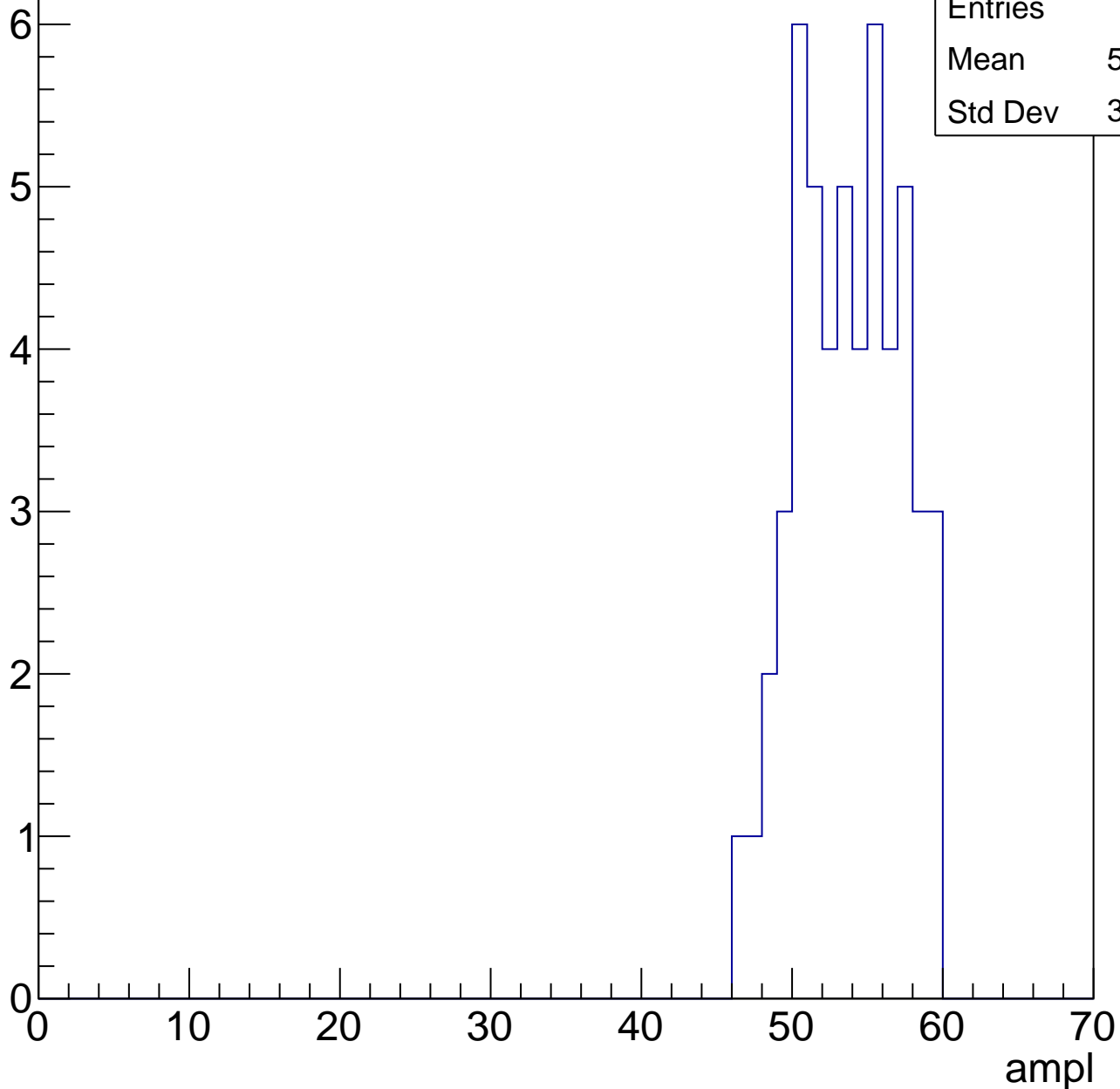
Entries	77
Mean	47.6
Std Dev	4.033



# B1L100S, U2-ch118, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

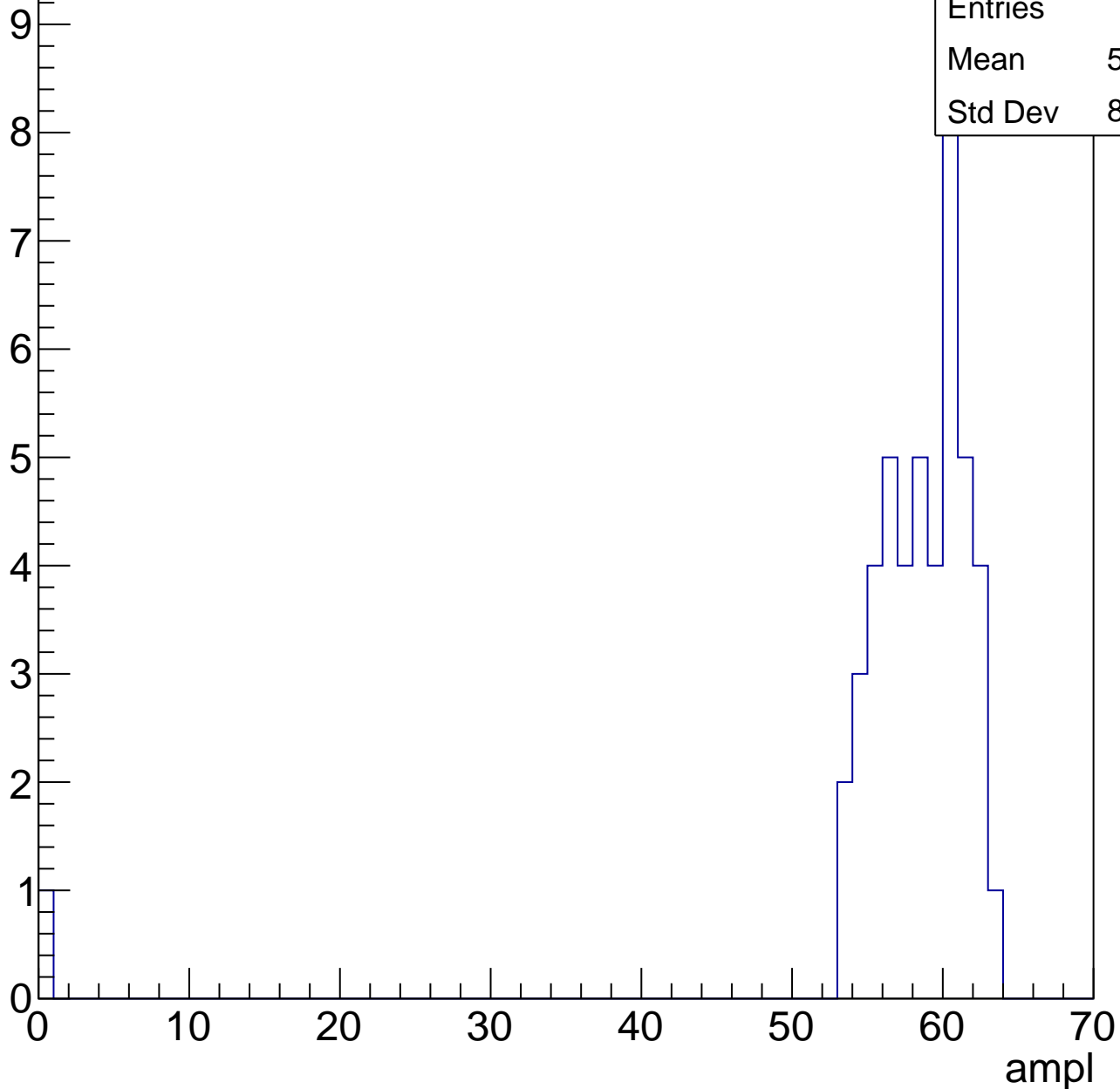


Entries	52
Mean	53.27
Std Dev	3.352

# B1L100S, U2-ch118, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



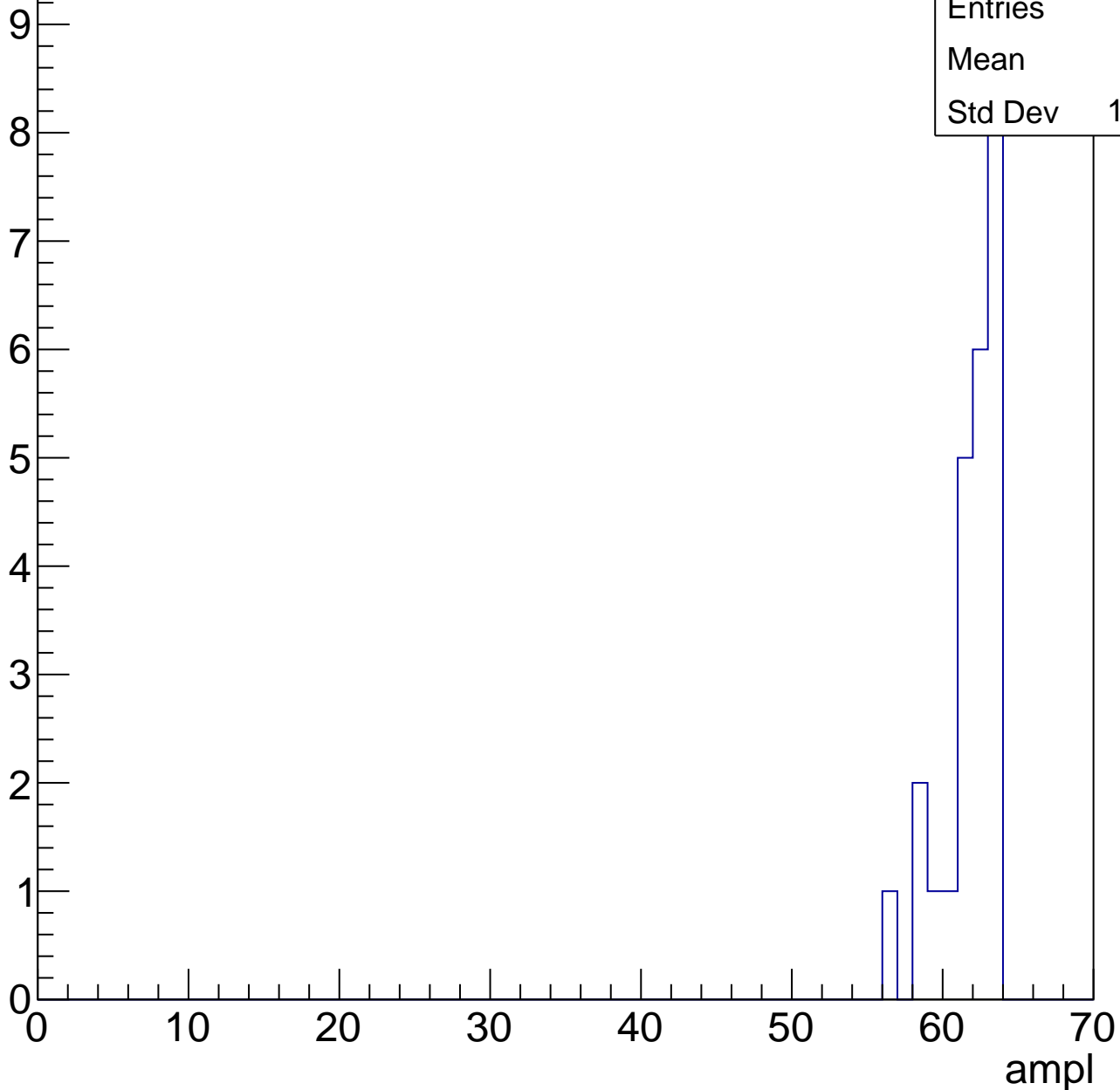
Entries	47
Mean	56.98
Std Dev	8.809

# B1L100S, U2-ch118, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	25
Mean	61.4
Std Dev	1.855

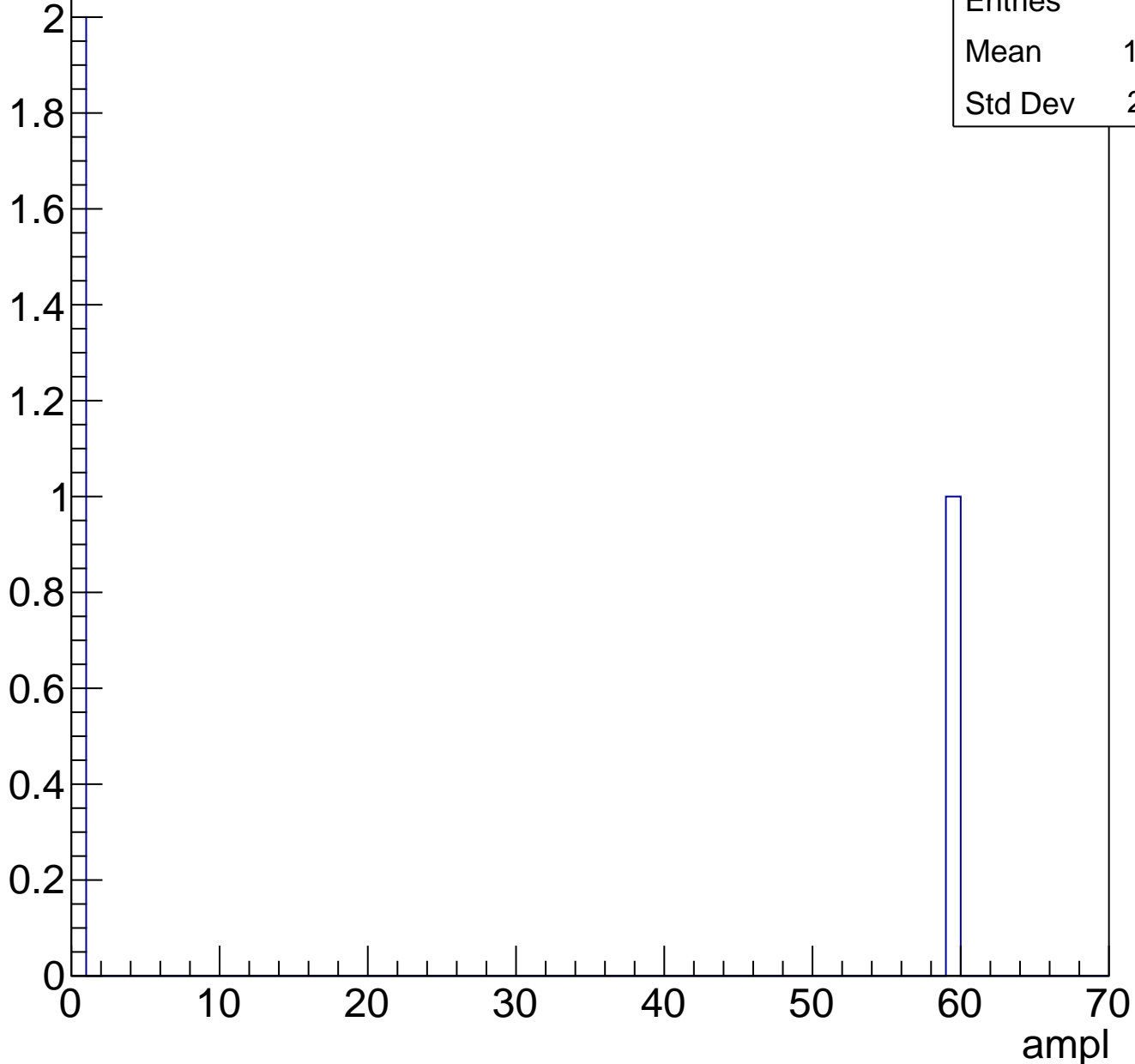




# B1L100S, U2-ch118, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	3
Mean	19.67
Std Dev	27.81

# B1L100S, U2-ch119, adc0

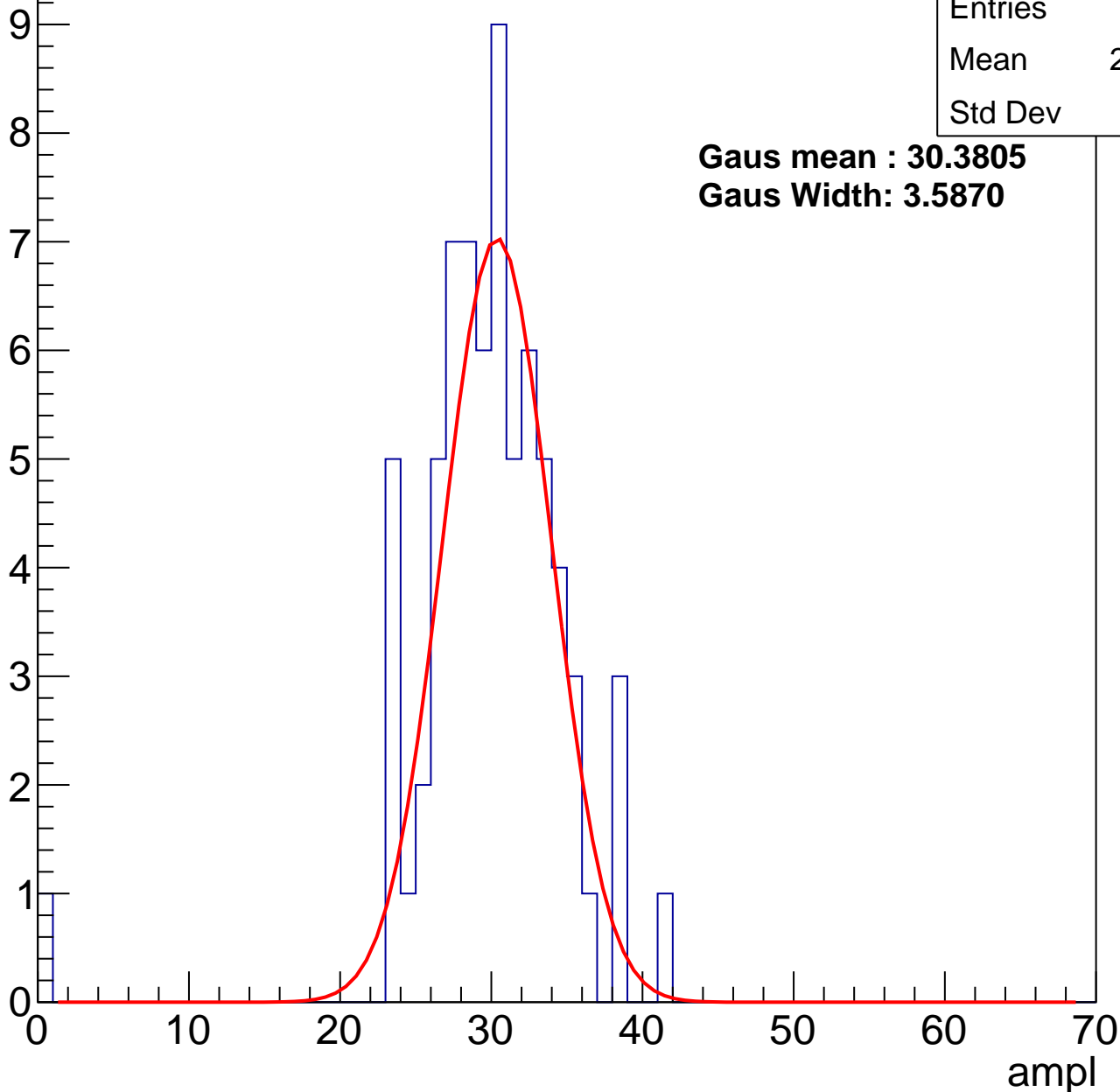
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	71
Mean	29.46
Std Dev	5.24

**Gaus mean : 30.3805**

**Gaus Width: 3.5870**



# B1L100S, U2-ch119, adc1

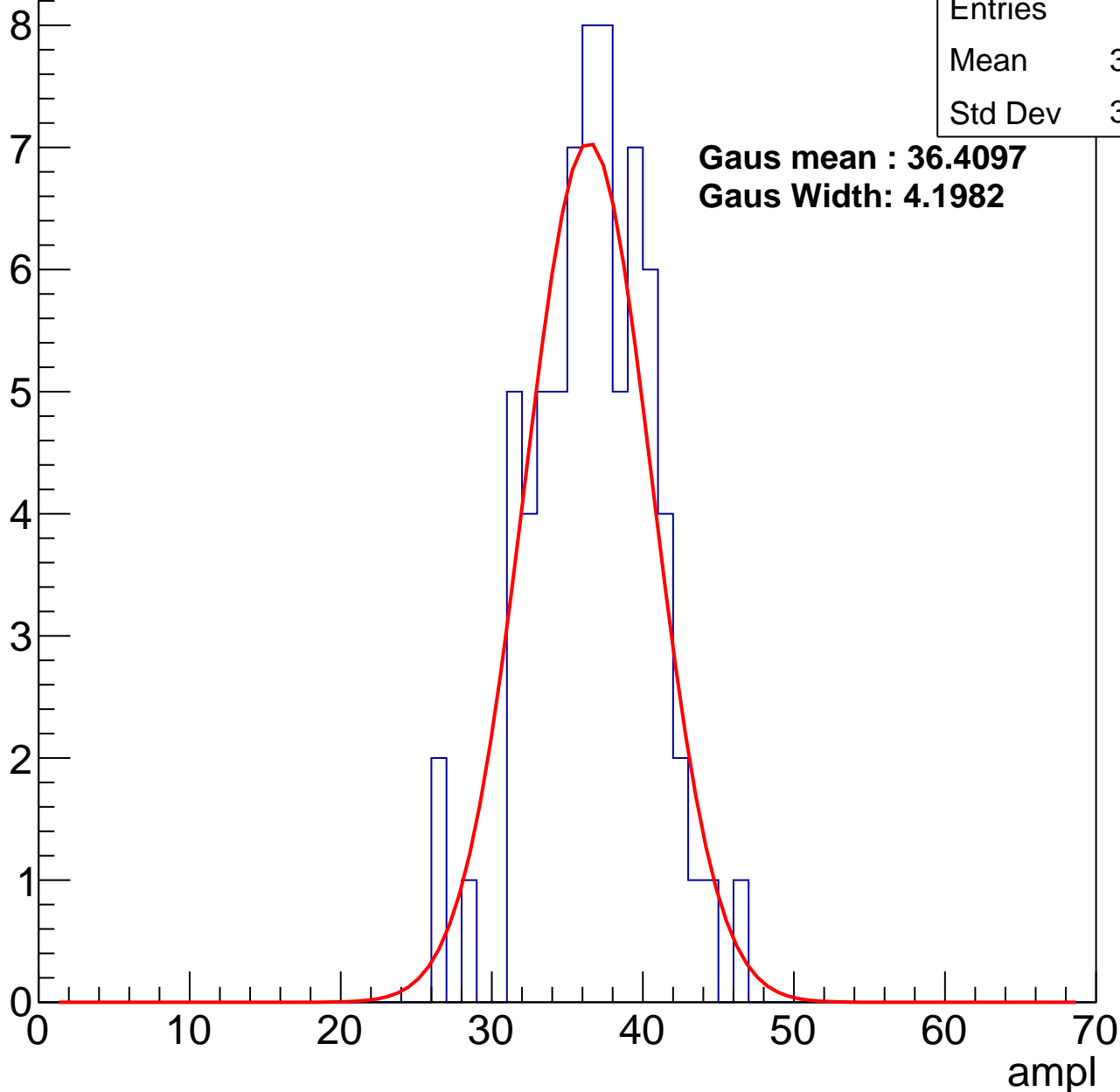
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	72
Mean	36.26
Std Dev	3.894

**Gaus mean : 36.4097**

**Gaus Width: 4.1982**



# B1L100S, U2-ch119, adc2

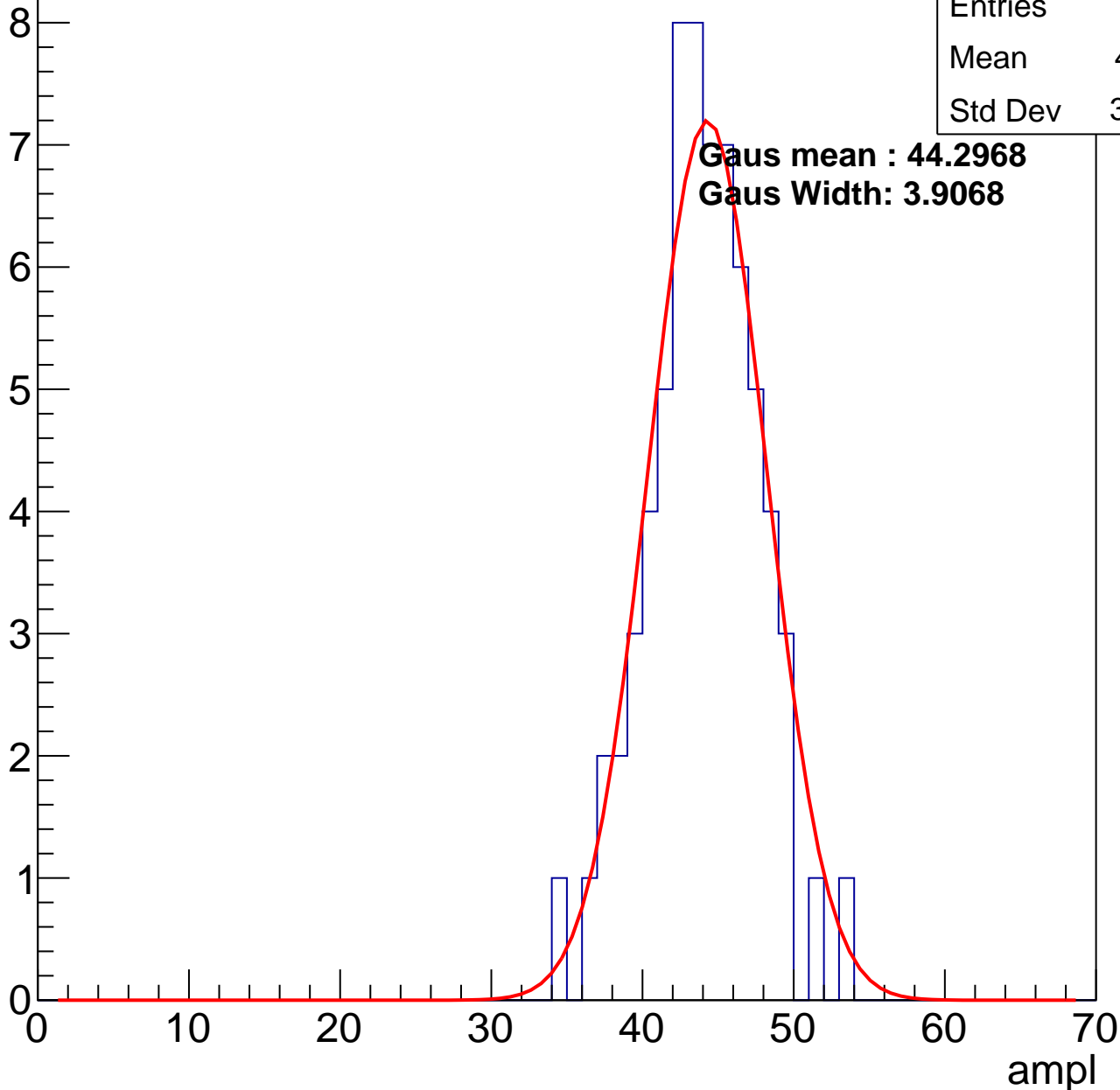
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	68
Mean	43.51
Std Dev	3.612

**Gaus mean : 44.2968**

**Gaus Width: 3.9068**

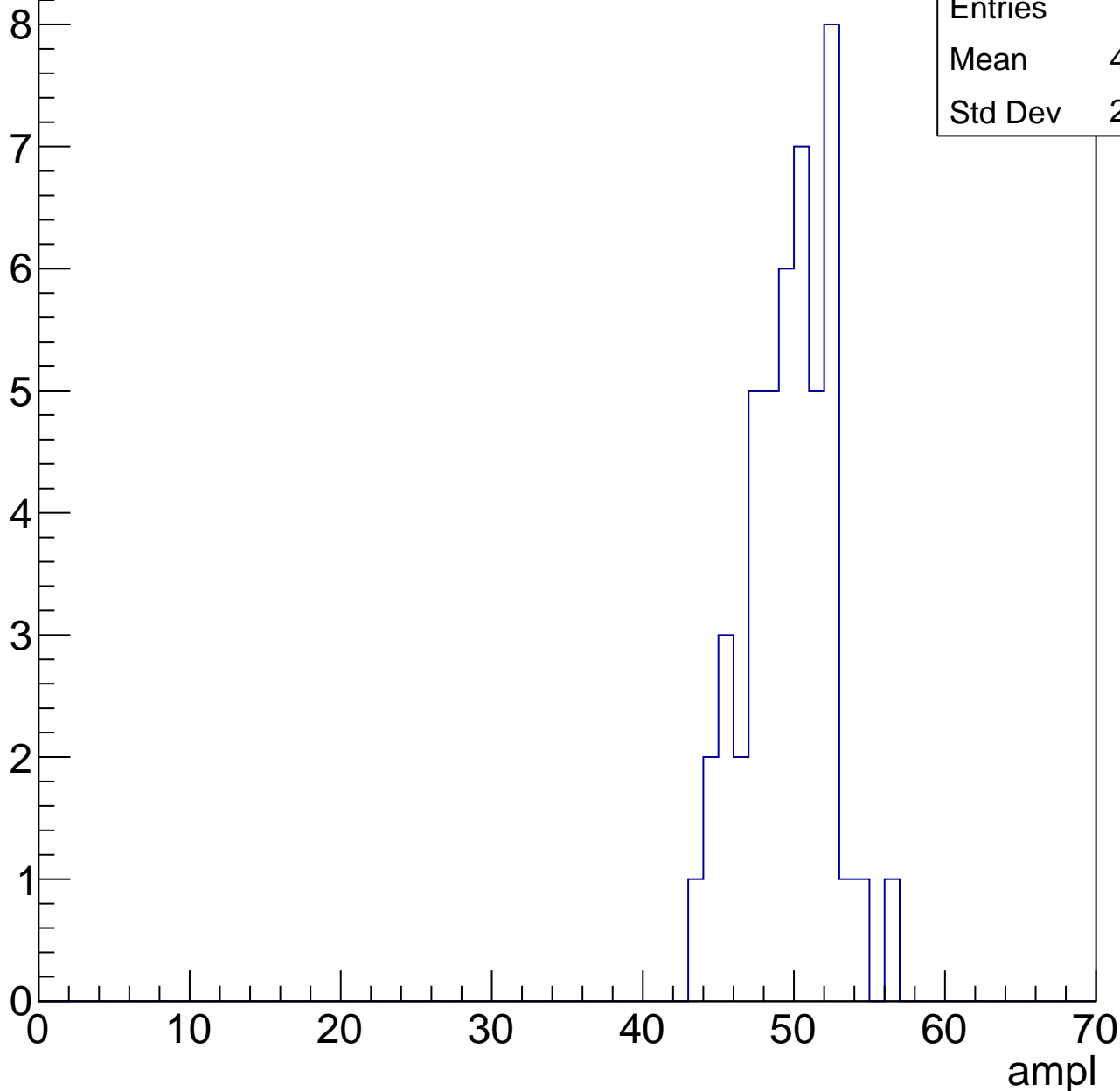


# B1L100S, U2-ch119, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	47
Mean	49.17
Std Dev	2.785

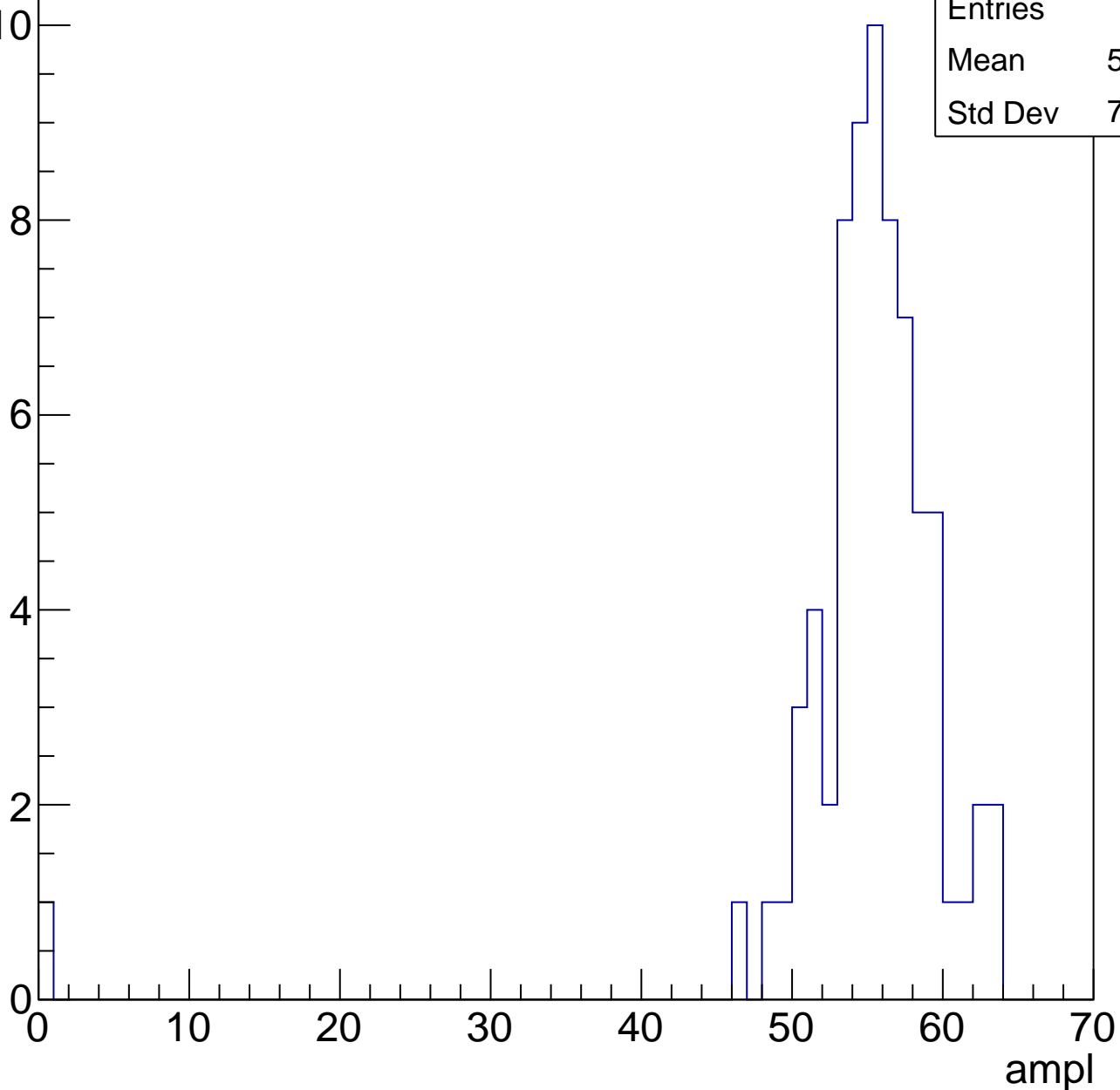


# B1L100S, U2-ch119, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	71
Mean	54.42
Std Dev	7.329



# B1L100S, U2-ch119, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	43
Mean	60.3
Std Dev	1.911

ampl

0

10

20

30

40

50

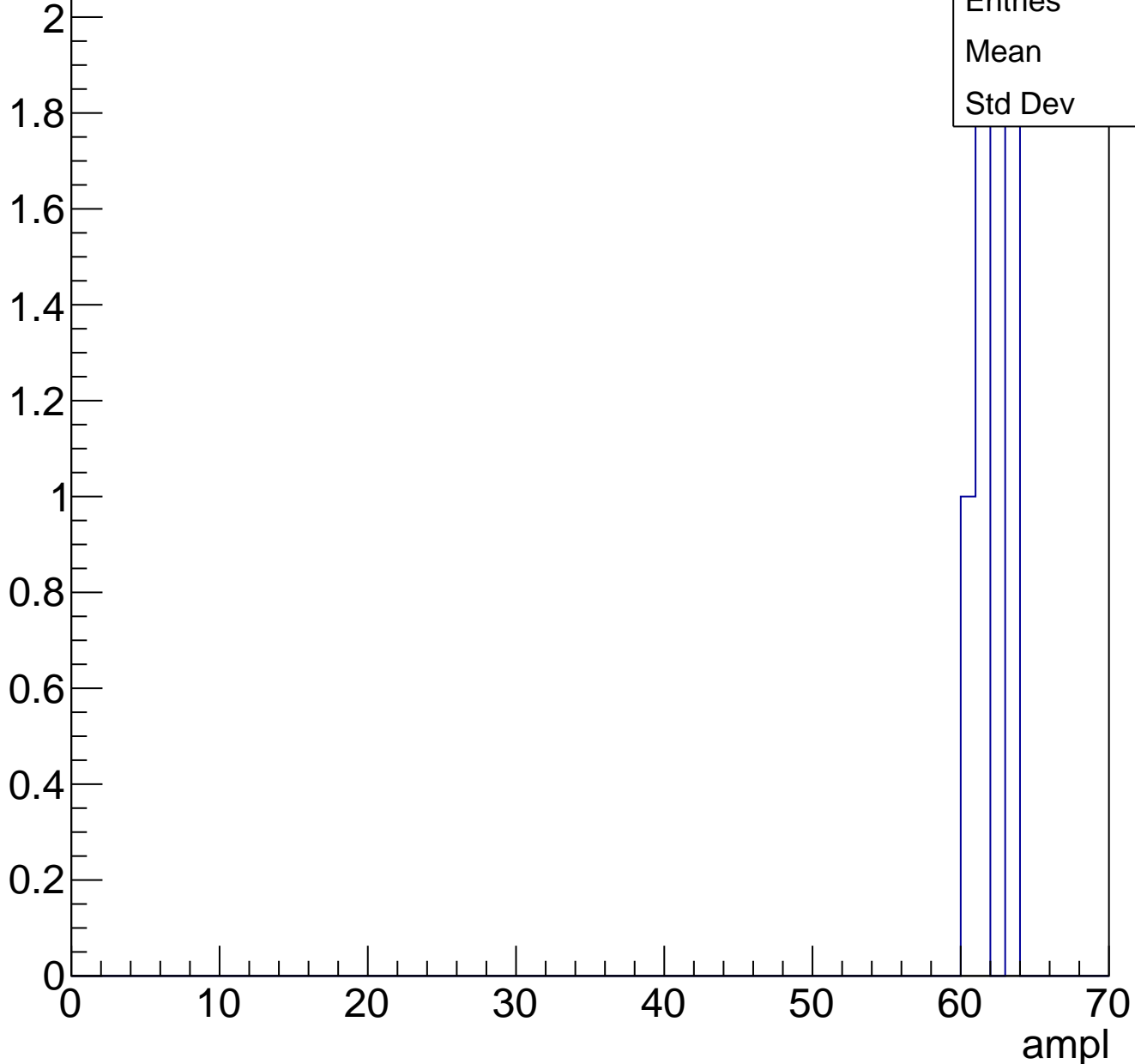
60

70

# B1L100S, U2-ch119, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry





# B1L100S, U2-ch119, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



# B1L100S, U2-ch120, adc0

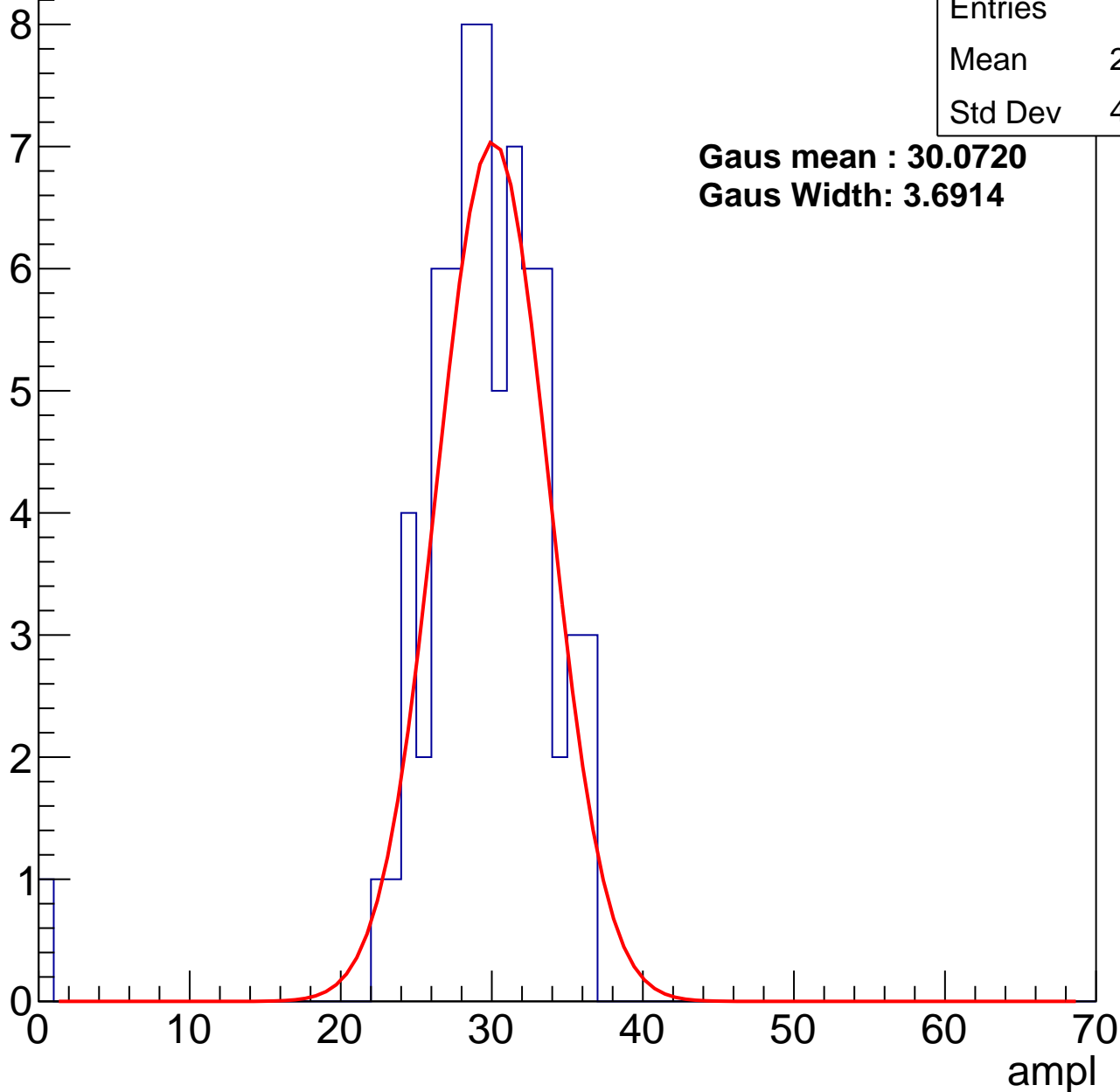
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	69
Mean	29.03
Std Dev	4.863

**Gaus mean : 30.0720**

**Gaus Width: 3.6914**



# B1L100S, U2-ch120, adc1

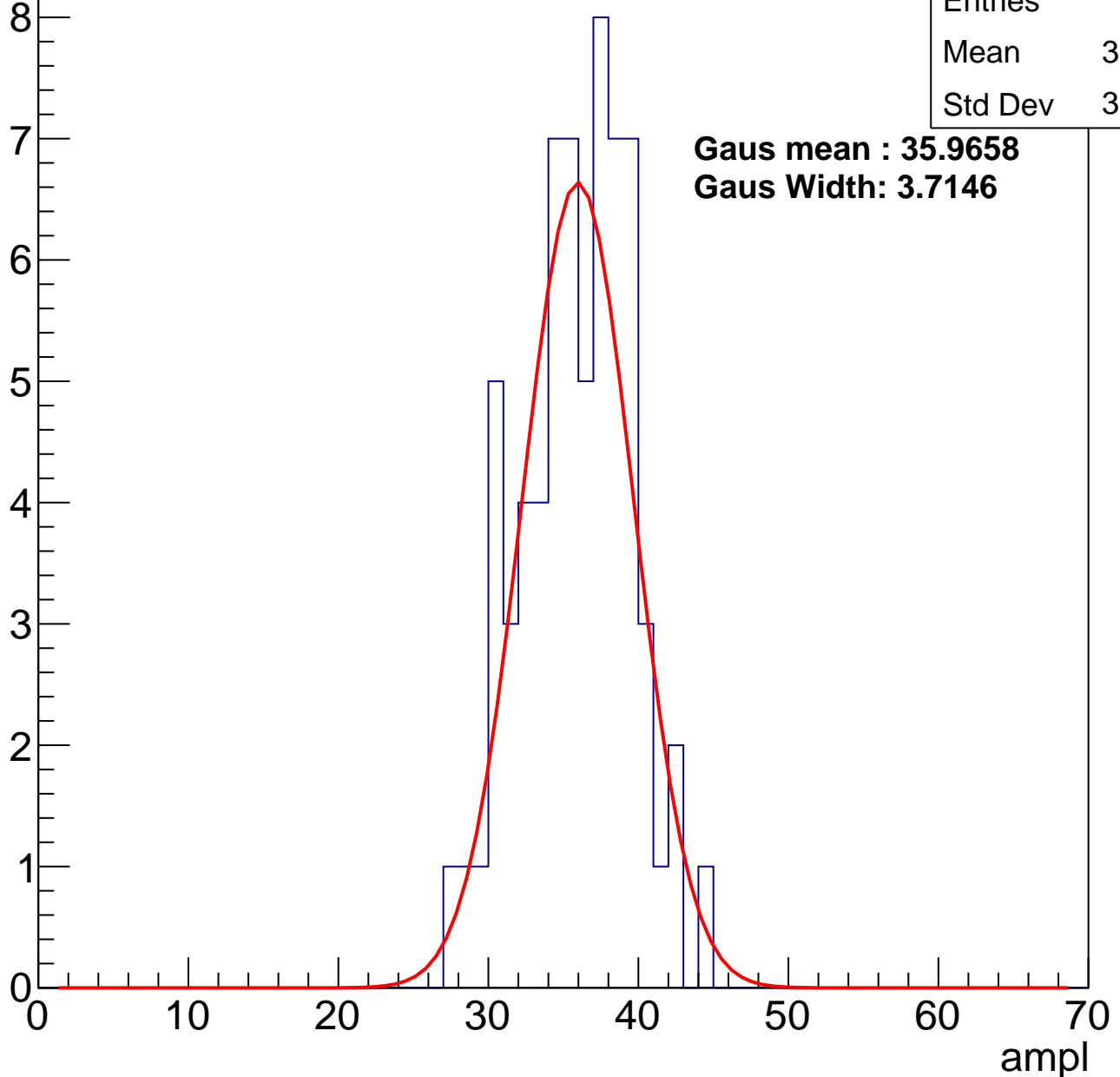
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	67
Mean	35.43
Std Dev	3.604

**Gaus mean : 35.9658**

**Gaus Width: 3.7146**



# B1L100S, U2-ch120, adc2

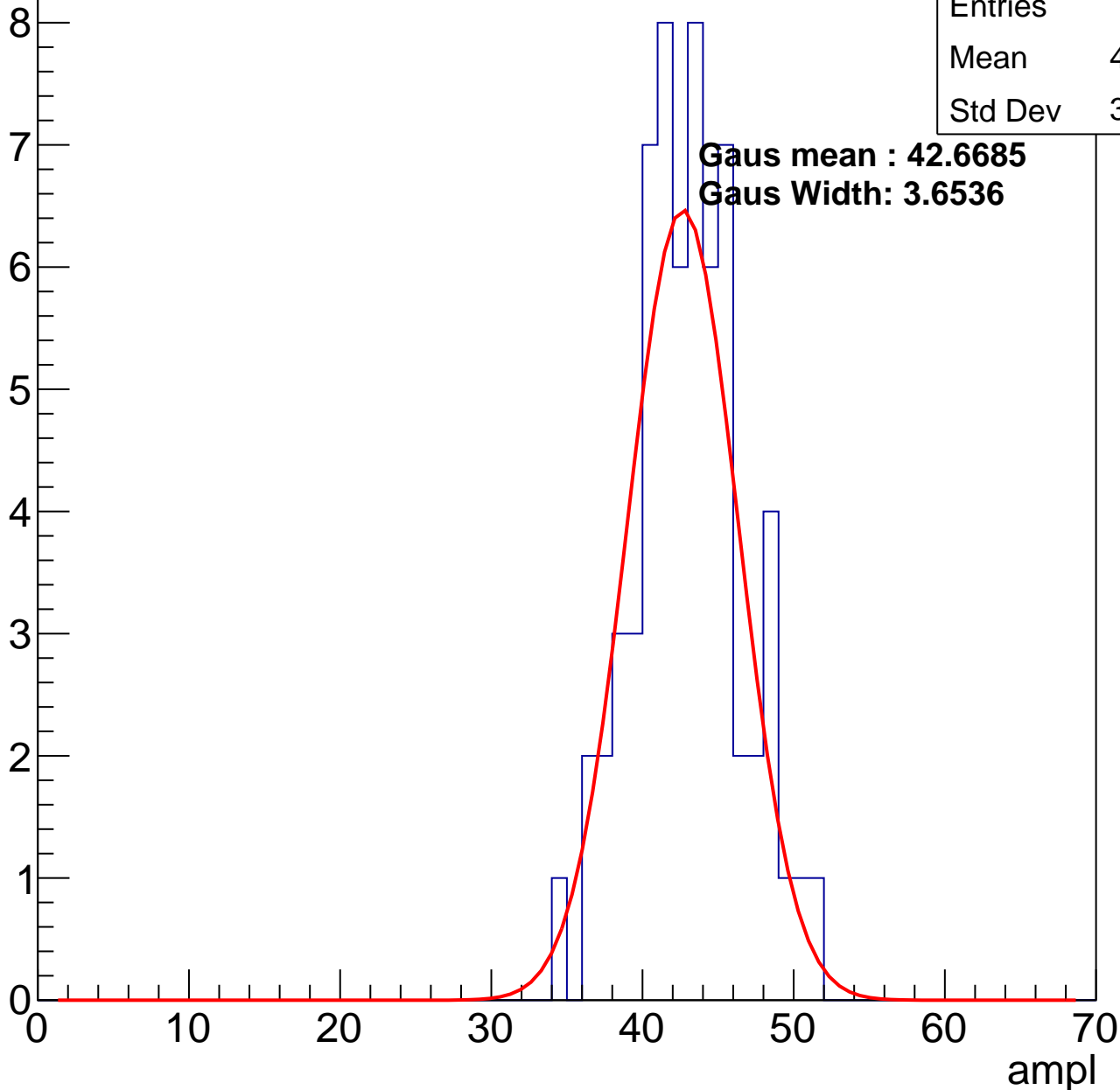
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	64
Mean	42.53
Std Dev	3.522

**Gaus mean : 42.6685**

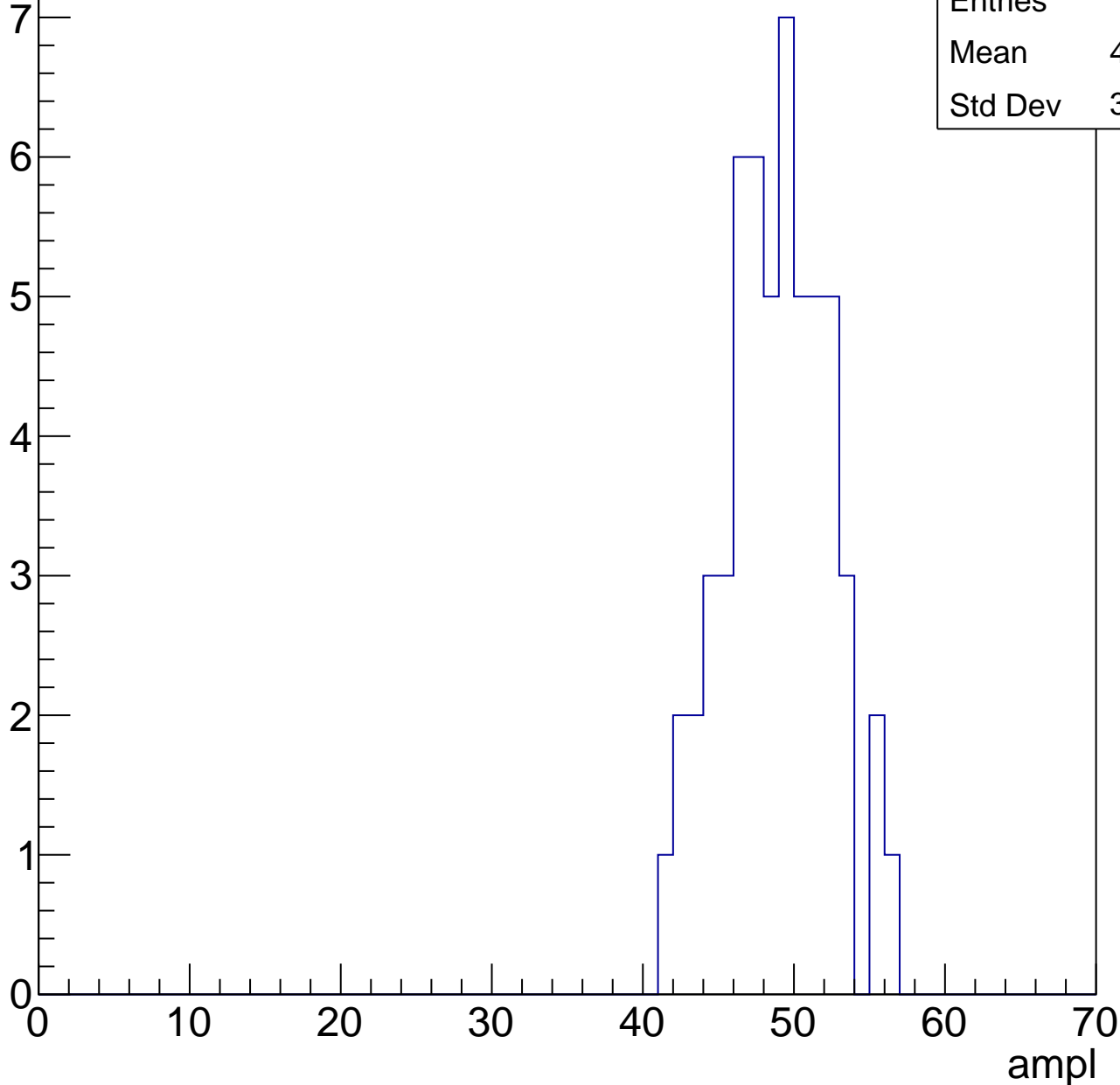
**Gaus Width: 3.6536**



# B1L100S, U2-ch120, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



# B1L100S, U2-ch120, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	57
Mean	53.67
Std Dev	3.435

Entry

10

8

6

4

2

0

0

10

20

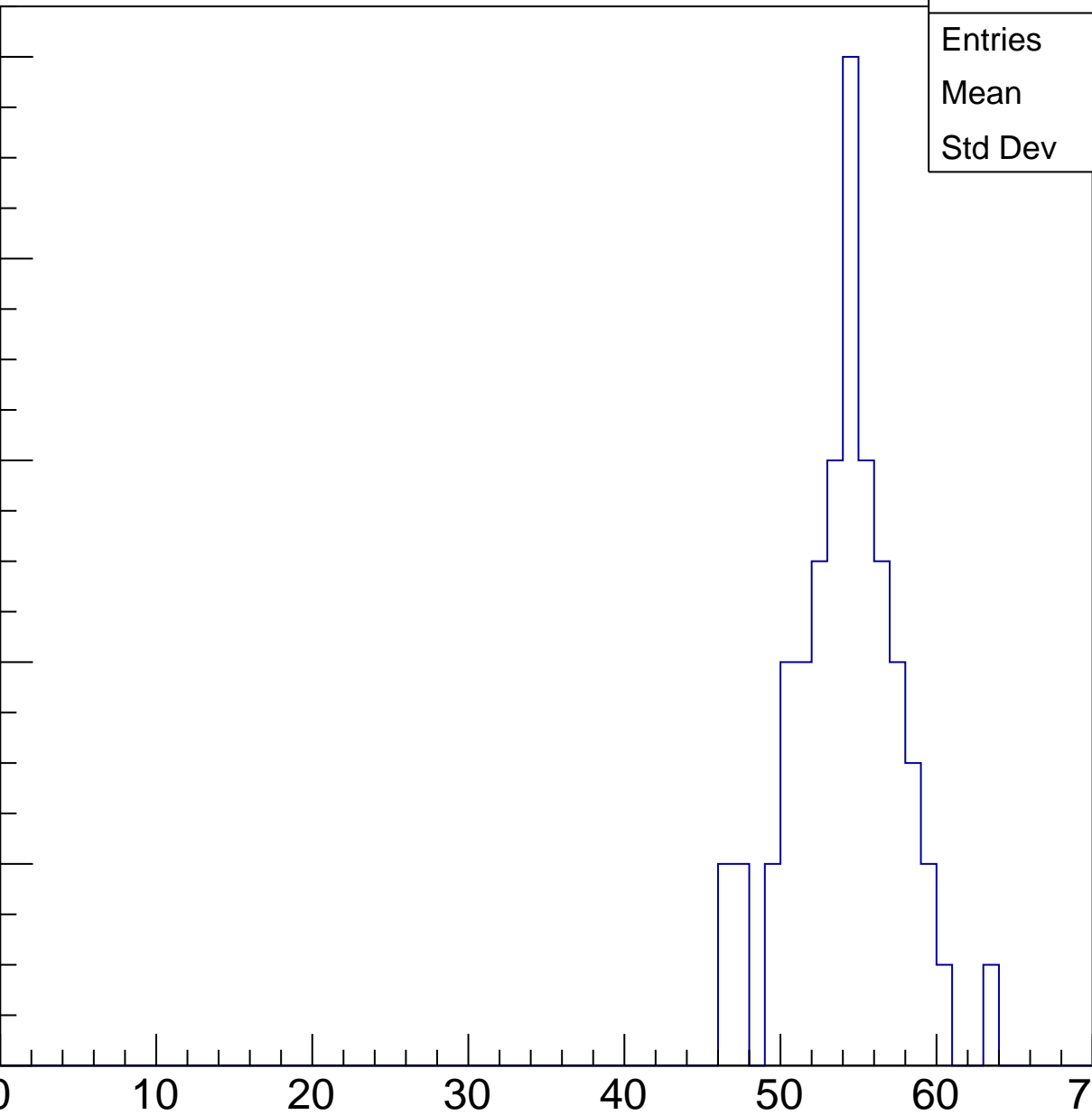
30

40

50

60

ampl

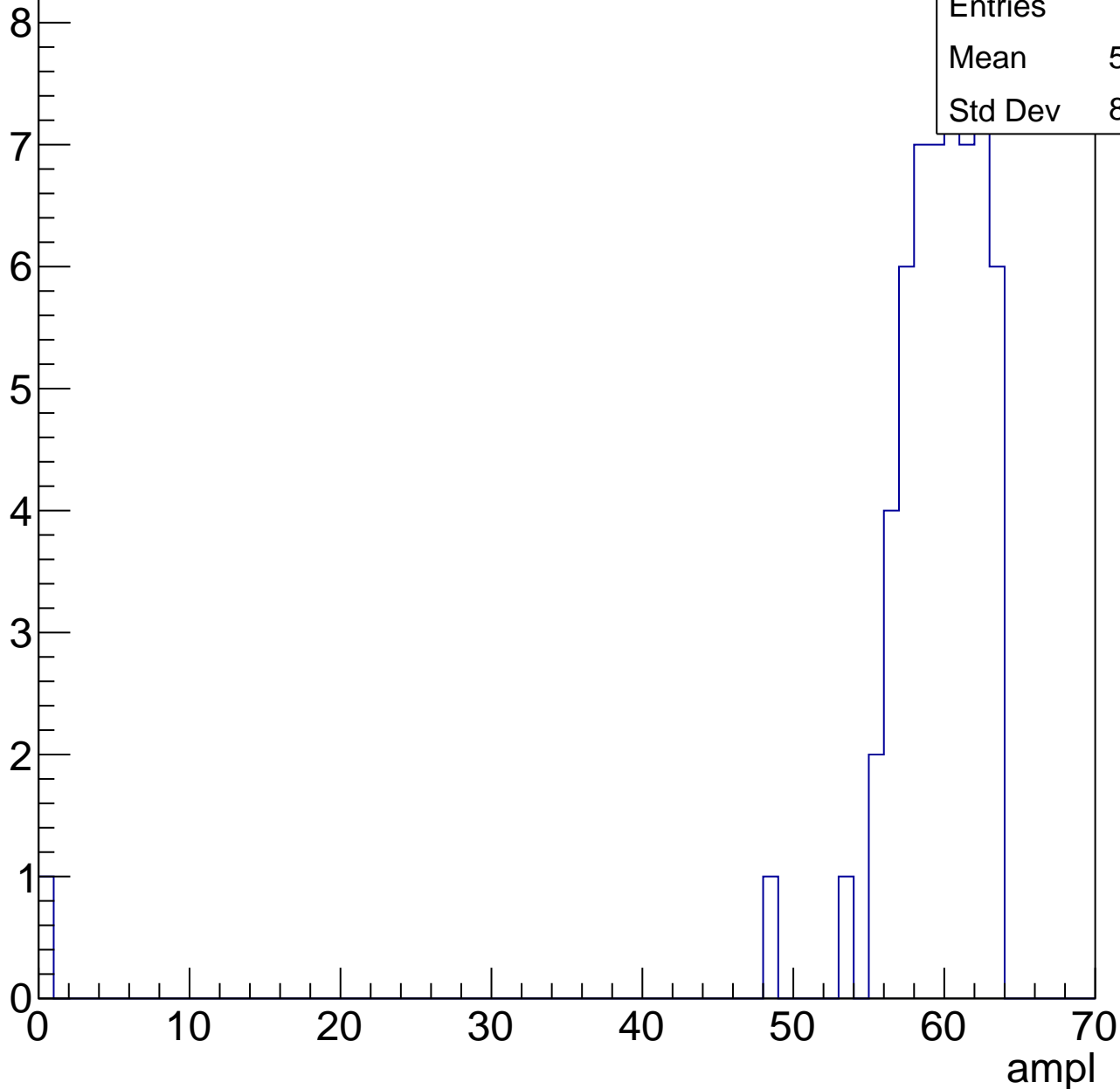


# B1L100S, U2-ch120, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

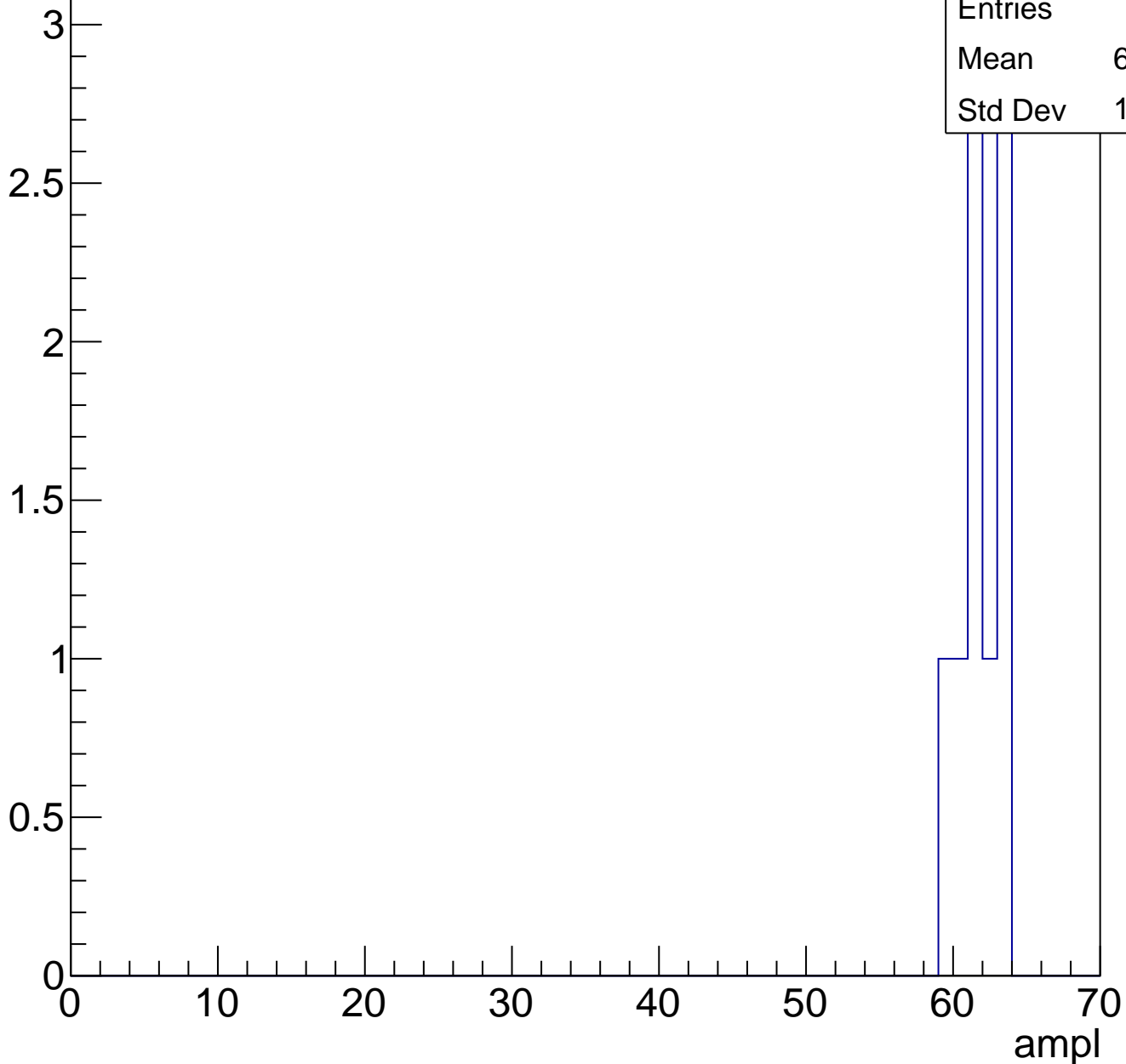
Entries	58
Mean	58.22
Std Dev	8.206



# B1L100S, U2-ch120, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry





# B1L100S, U2-ch120, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



# B1L100S, U2-ch121, adc0

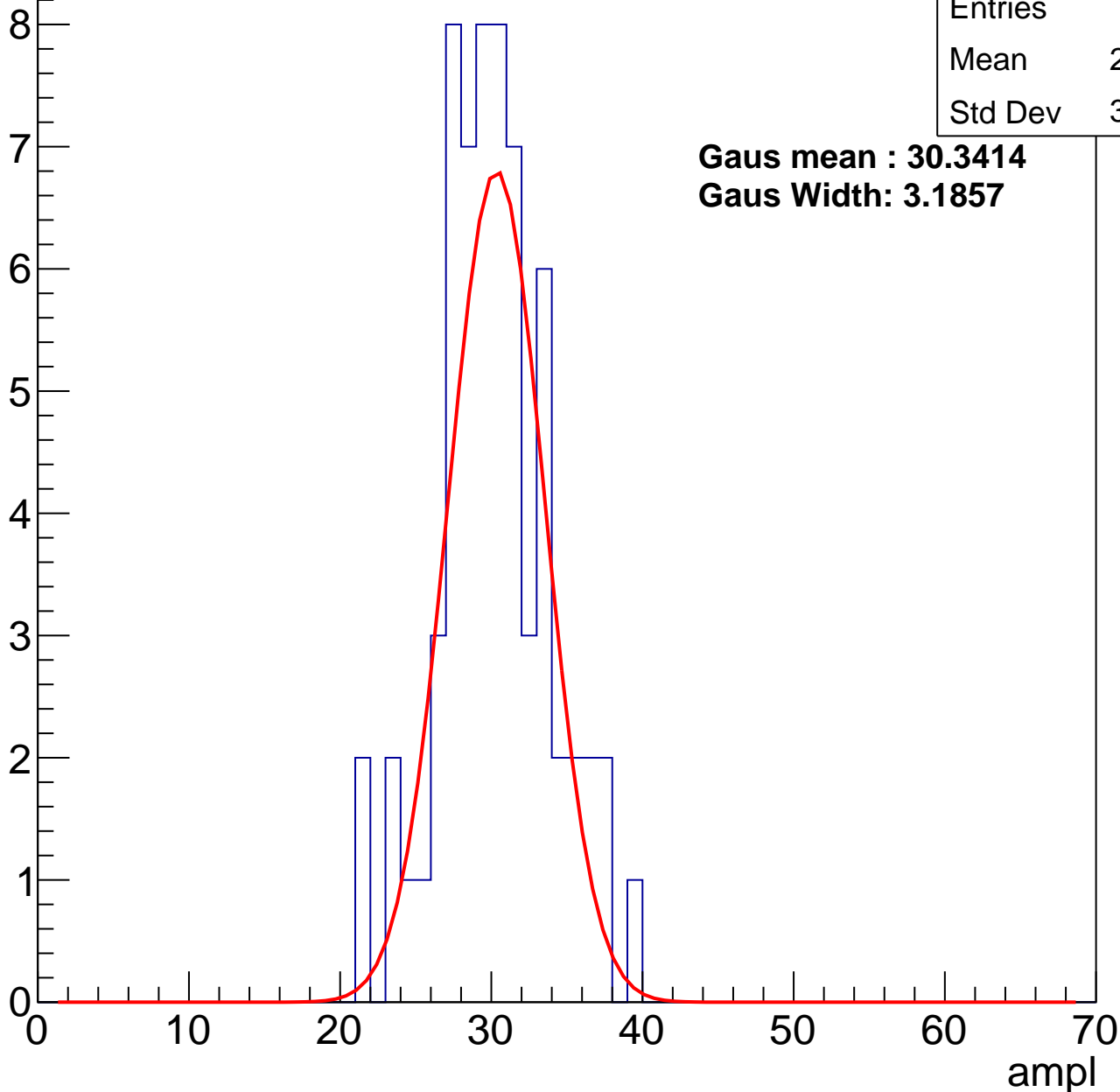
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	65
Mean	29.74
Std Dev	3.676

**Gaus mean : 30.3414**

**Gaus Width: 3.1857**



# B1L100S, U2-ch121, adc1

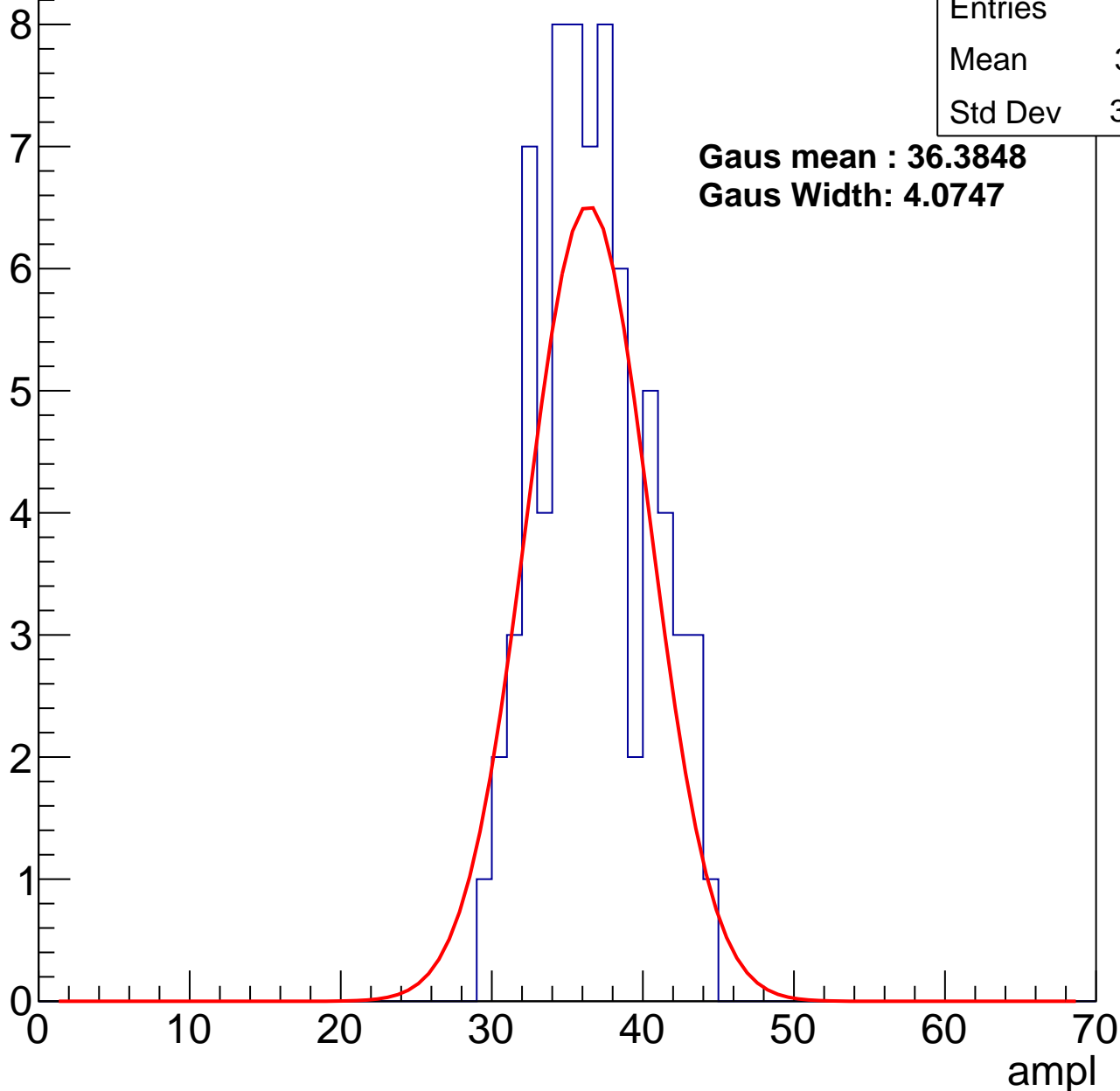
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	72
Mean	36.21
Std Dev	3.594

**Gaus mean : 36.3848**

**Gaus Width: 4.0747**



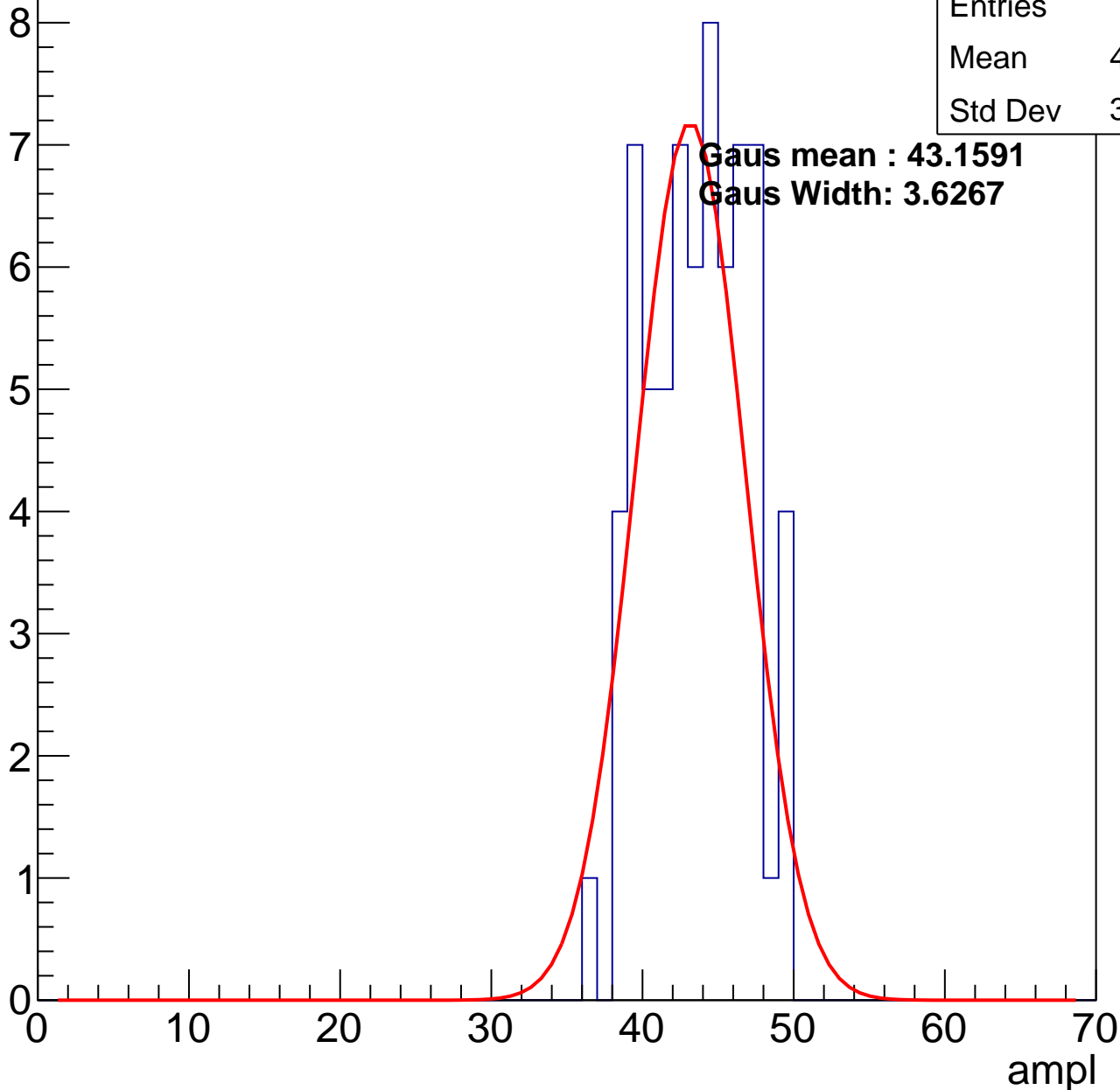
# B1L100S, U2-ch121, adc2

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	68
Mean	43.16
Std Dev	3.225

**Gaus mean : 43.1591**  
**Gaus Width: 3.6267**

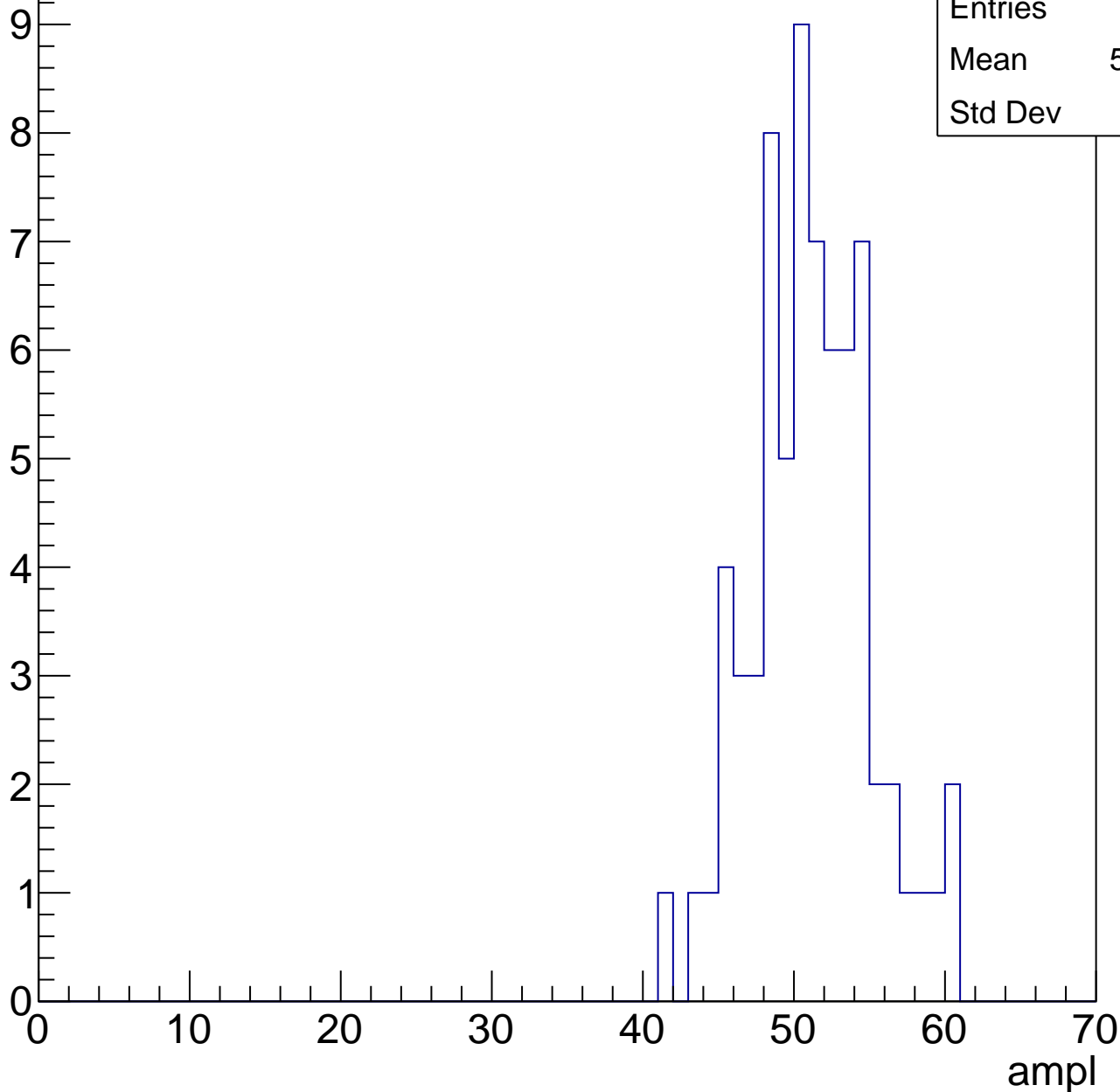


# B1L100S, U2-ch121, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	70
Mean	50.67
Std Dev	3.89

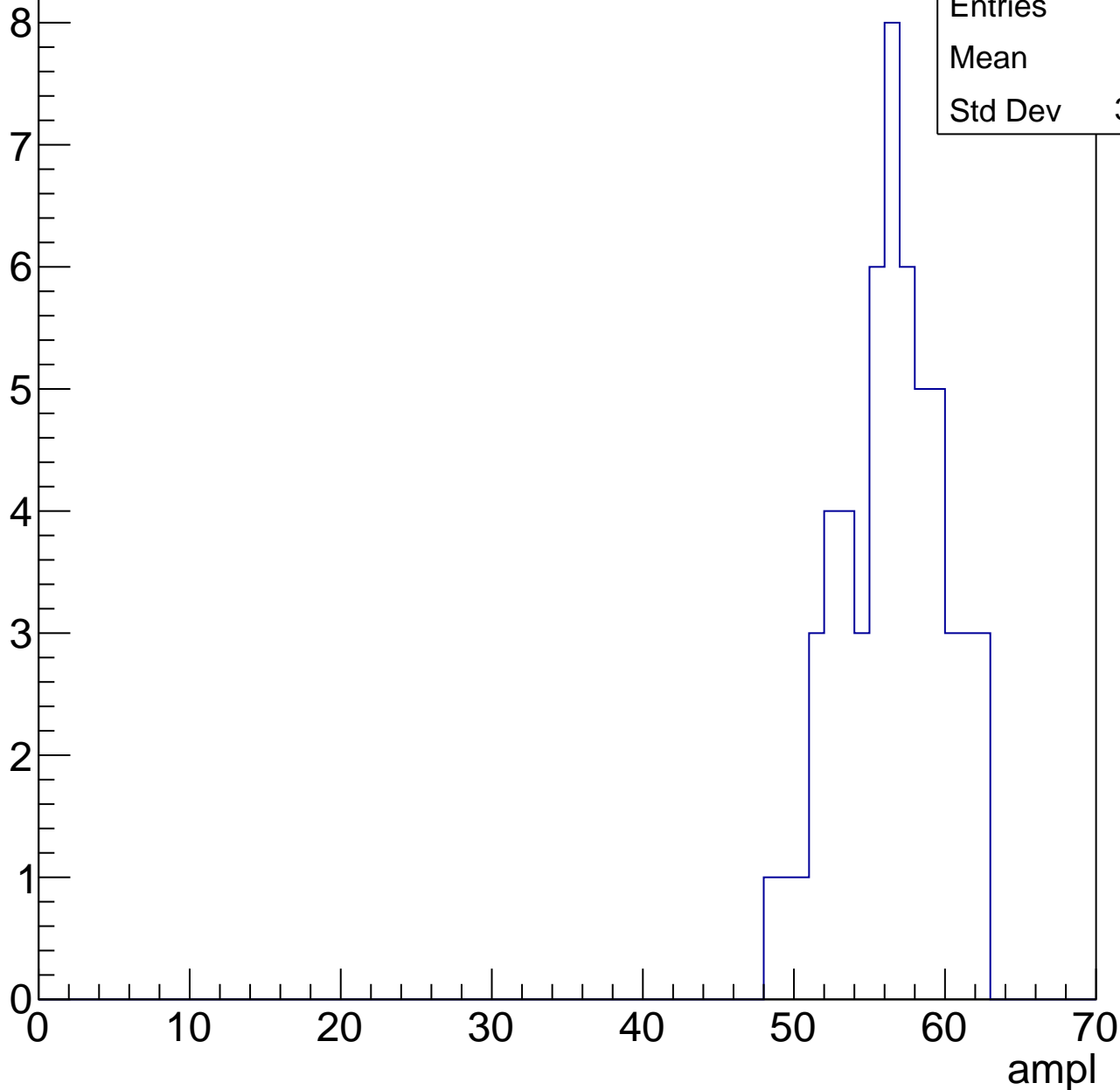


# B1L100S, U2-ch121, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	56
Mean	56
Std Dev	3.391

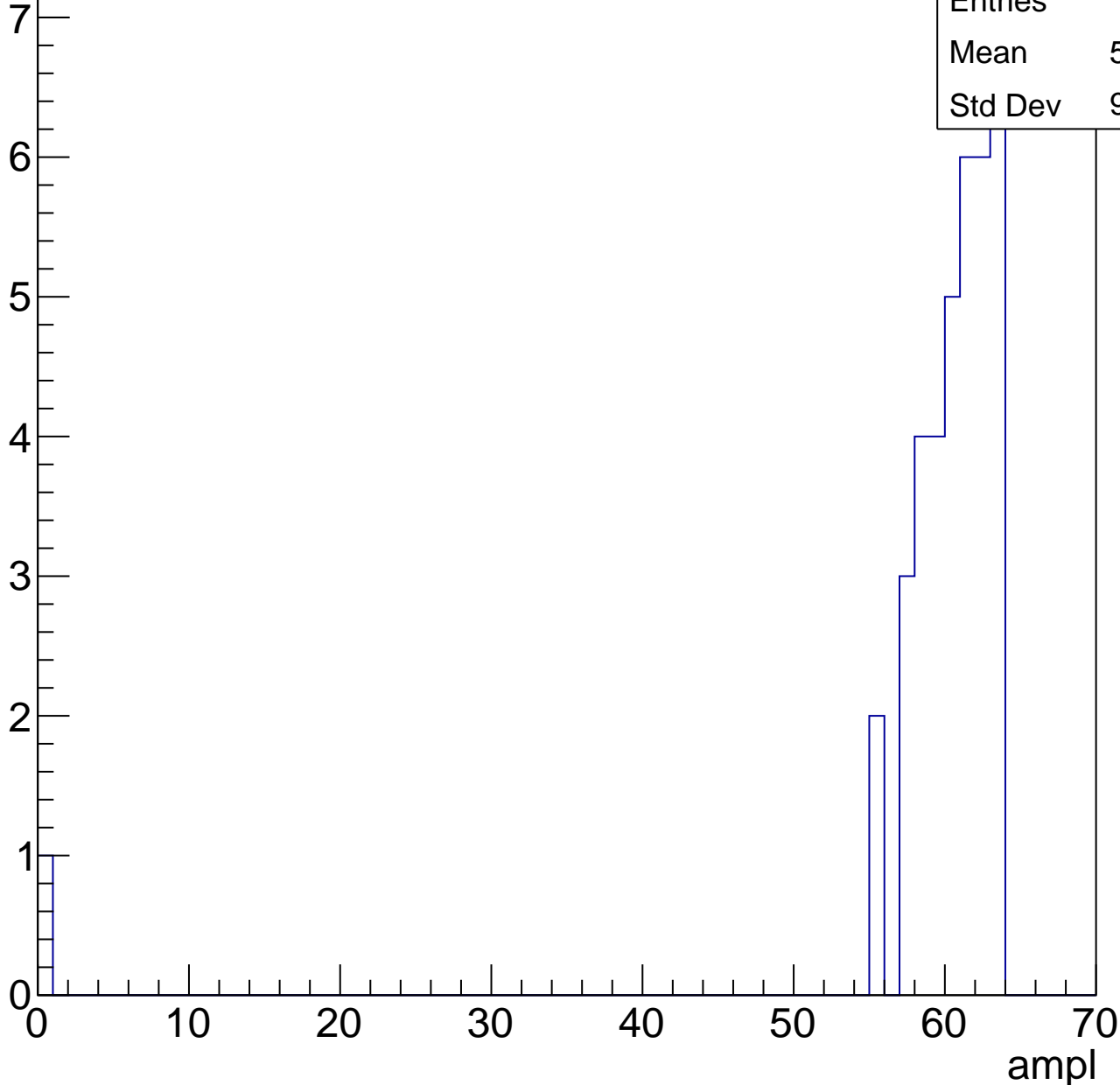


# B1L100S, U2-ch121, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	38
Mean	58.63
Std Dev	9.893



# B1L100S, U2-ch121, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry





# B1L100S, U2-ch121, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L100S, U2-ch122, adc0

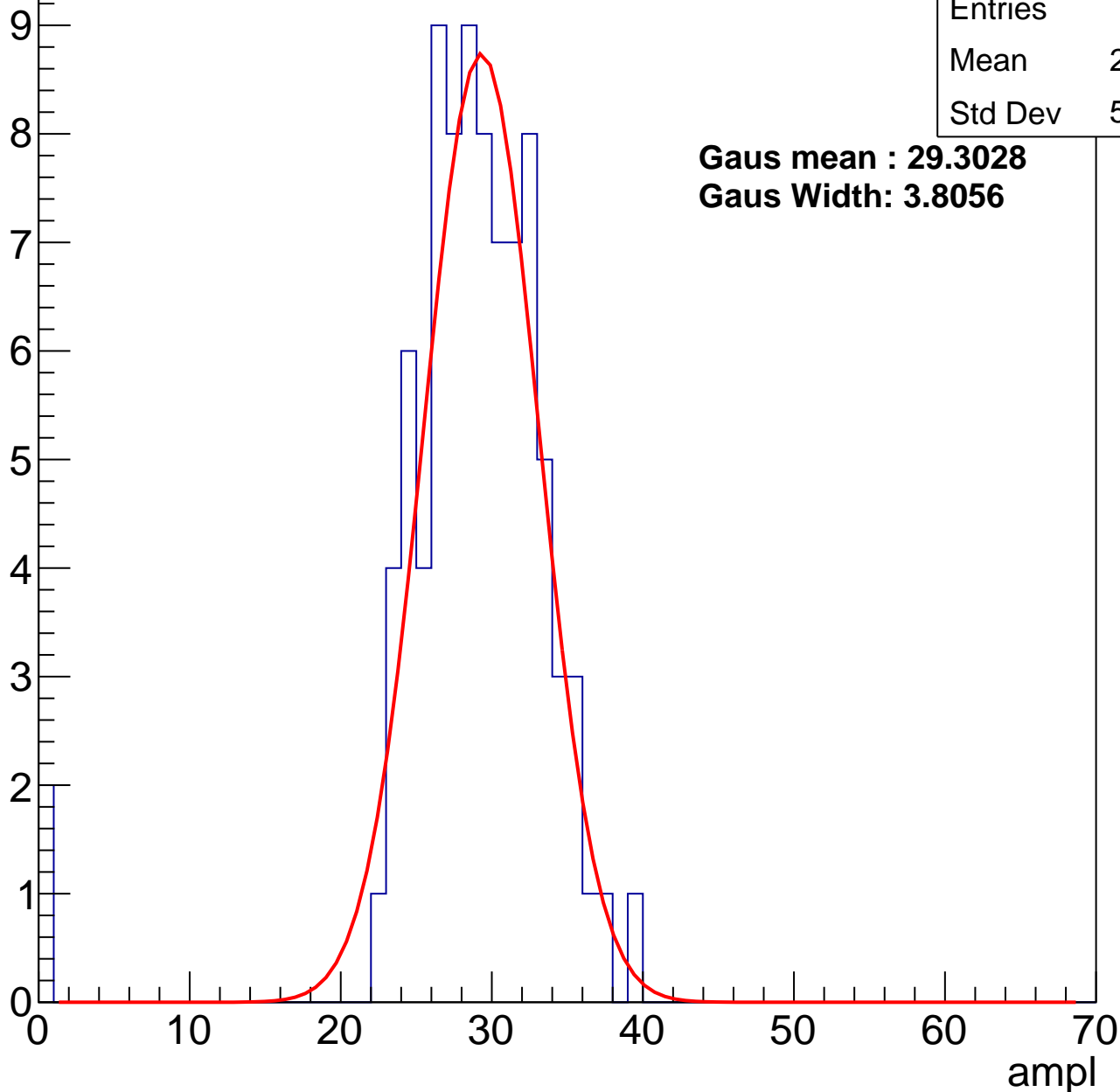
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	87
Mean	28.26
Std Dev	5.619

**Gaus mean : 29.3028**

**Gaus Width: 3.8056**



# B1L100S, U2-ch122, adc1

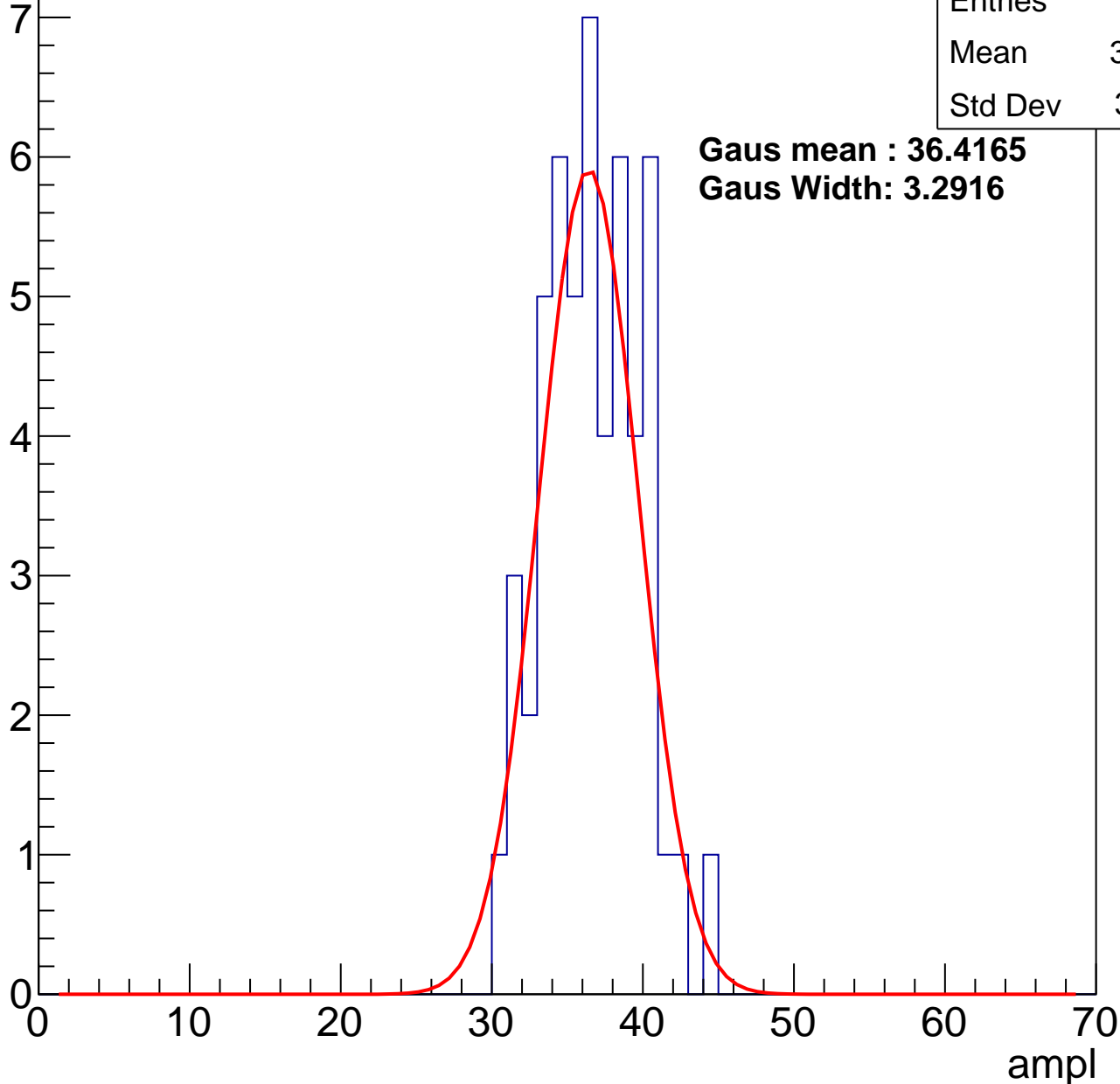
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	52
Mean	36.19
Std Dev	3.101

**Gaus mean : 36.4165**

**Gaus Width: 3.2916**



# B1L100S, U2-ch122, adc2

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	79
Mean	42.59
Std Dev	4.014

**Gaus mean : 42.9411**

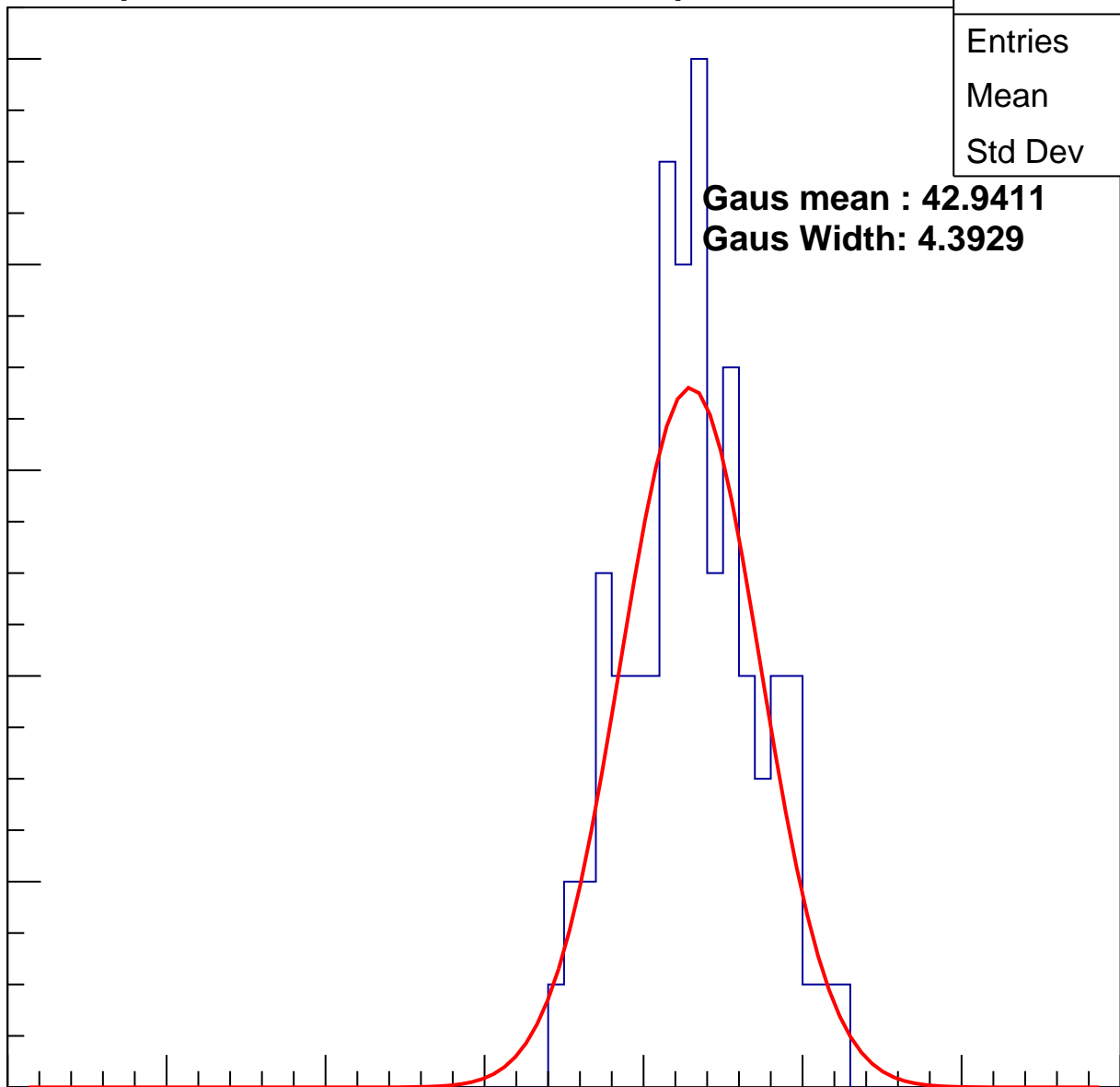
**Gaus Width: 4.3929**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

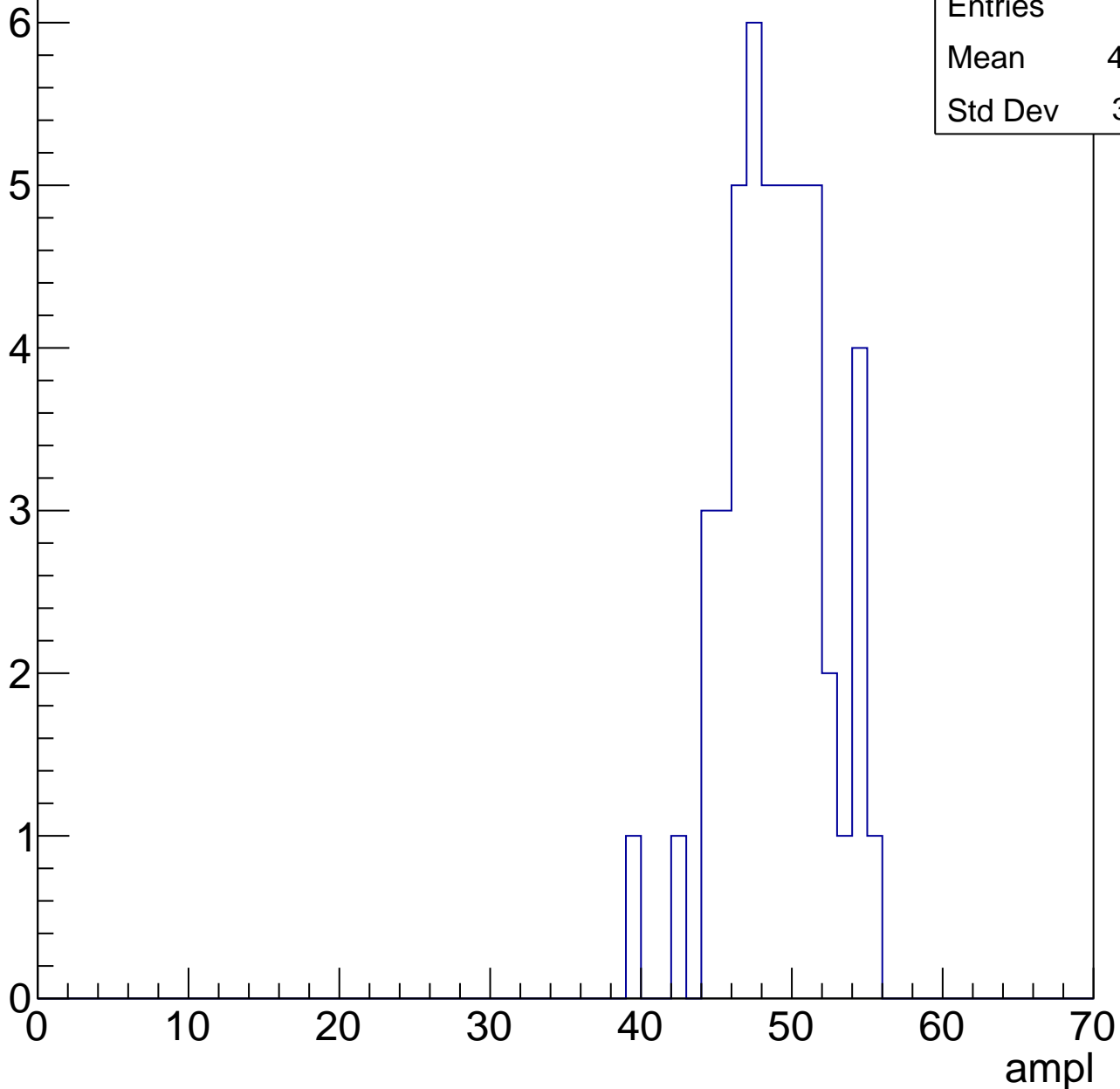


# B1L100S, U2-ch122, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	47
Mean	48.47
Std Dev	3.351

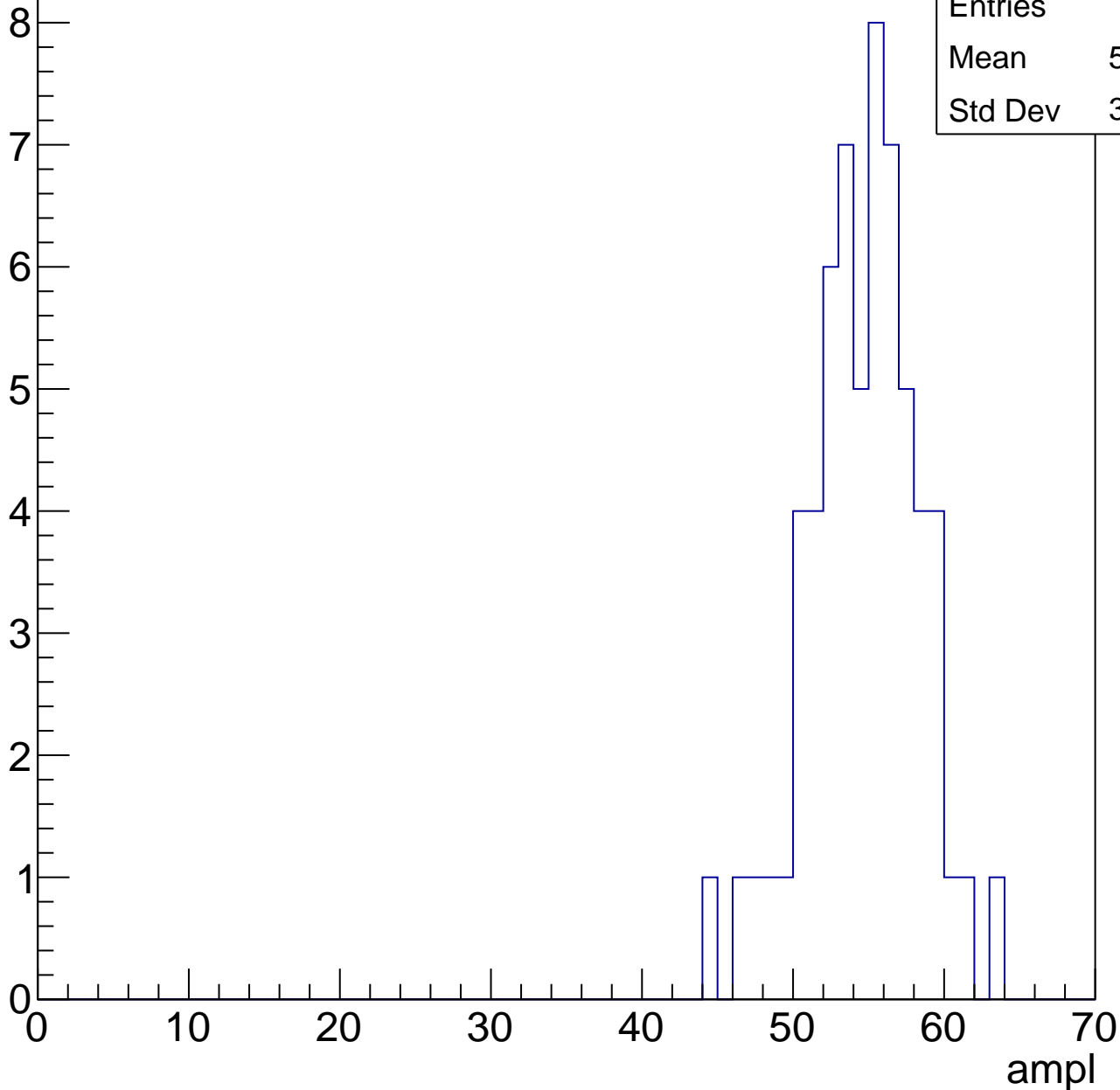


# B1L100S, U2-ch122, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	62
Mean	54.19
Std Dev	3.623

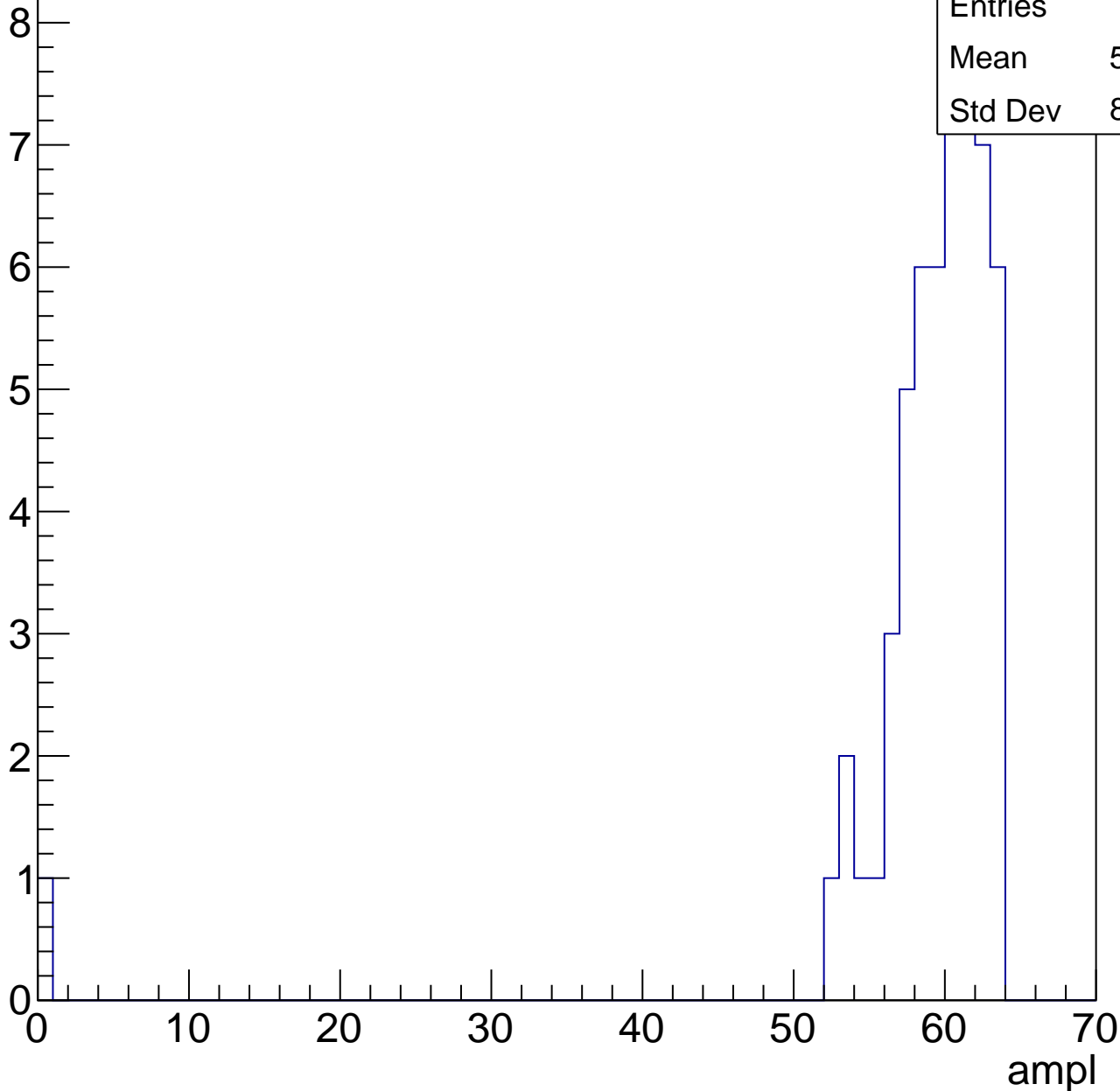


# B1L100S, U2-ch122, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	55
Mean	58.22
Std Dev	8.379



# B1L100S, U2-ch122, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry





# B1L100S, U2-ch122, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



# B1L100S, U2-ch123, adc0

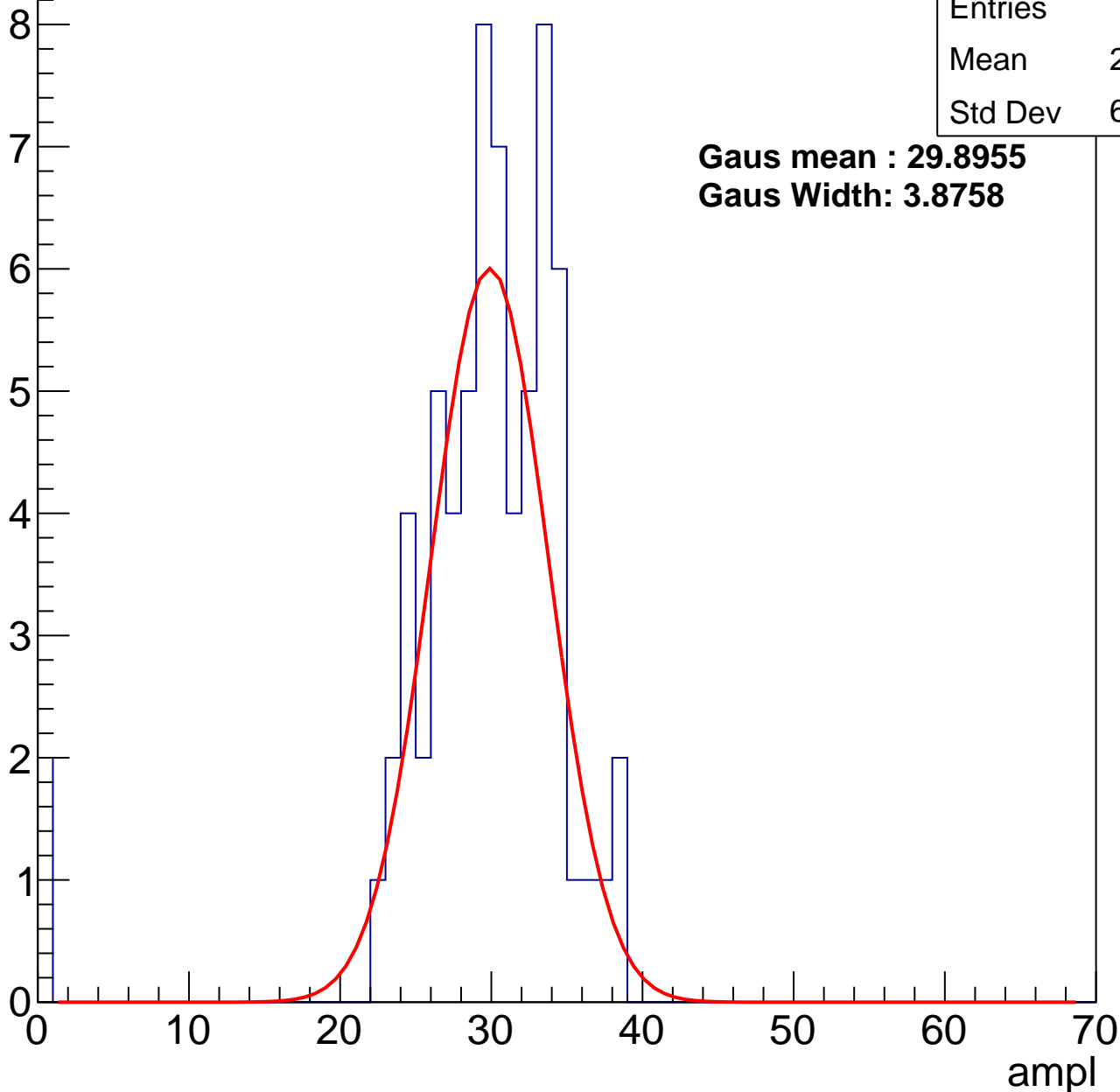
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	68
Mean	28.97
Std Dev	6.252

**Gaus mean : 29.8955**

**Gaus Width: 3.8758**



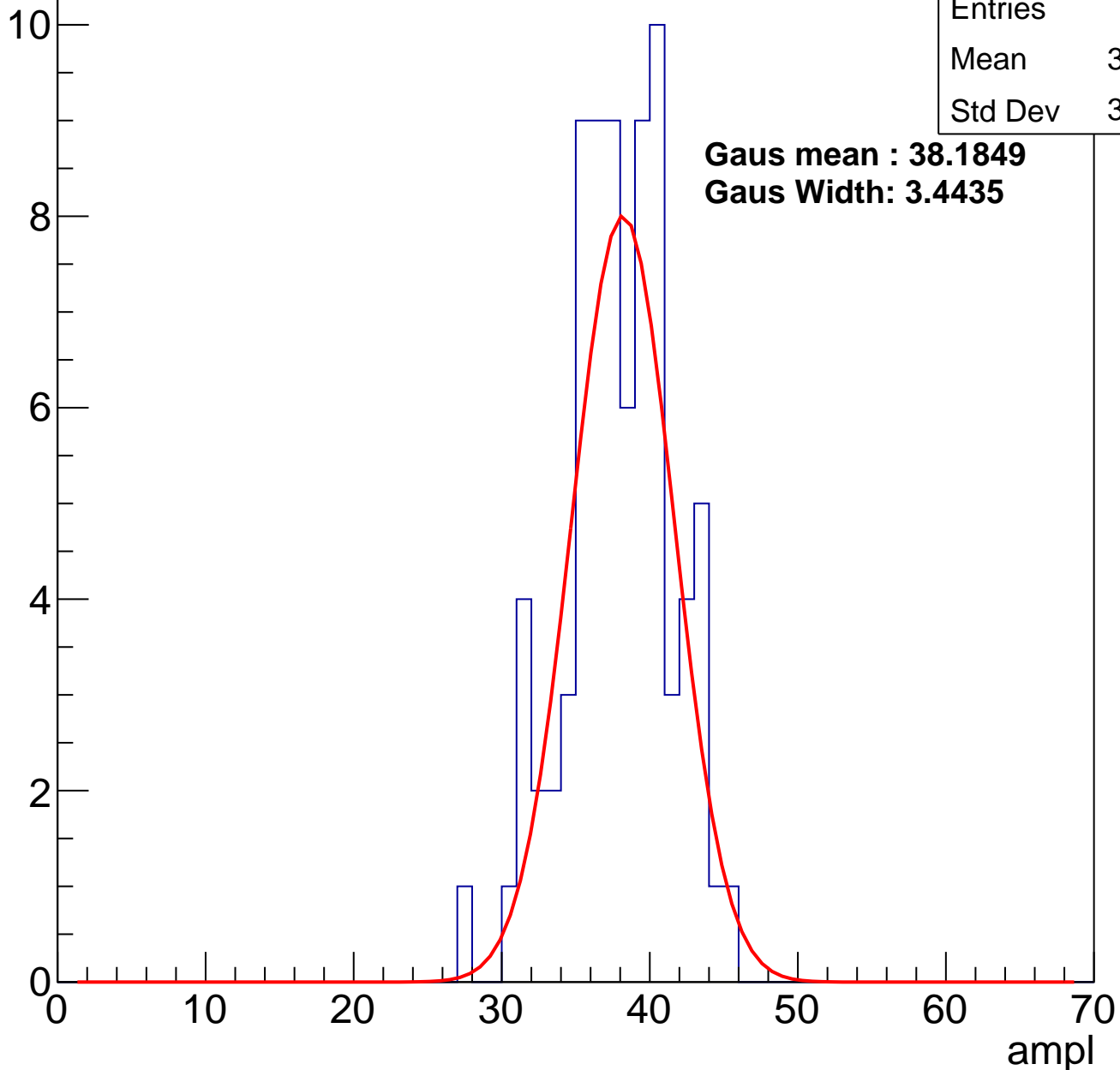
# B1L100S, U2-ch123, adc1

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	79
Mean	37.46
Std Dev	3.564

**Gaus mean : 38.1849**  
**Gaus Width: 3.4435**

Entry



# B1L100S, U2-ch123, adc2

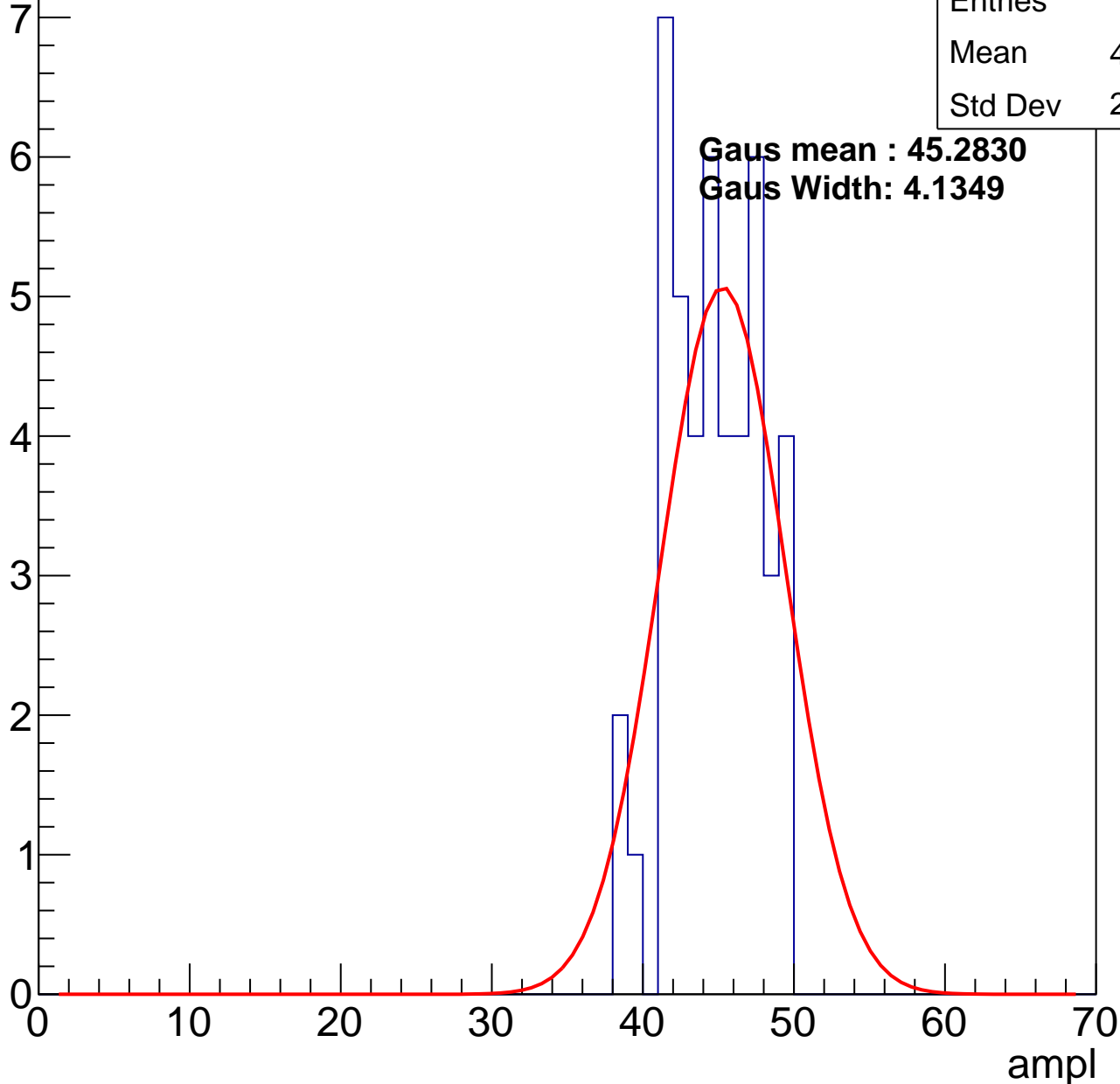
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	46
Mean	44.22
Std Dev	2.963

**Gaus mean : 45.2830**

**Gaus Width: 4.1349**



# B1L100S, U2-ch123, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

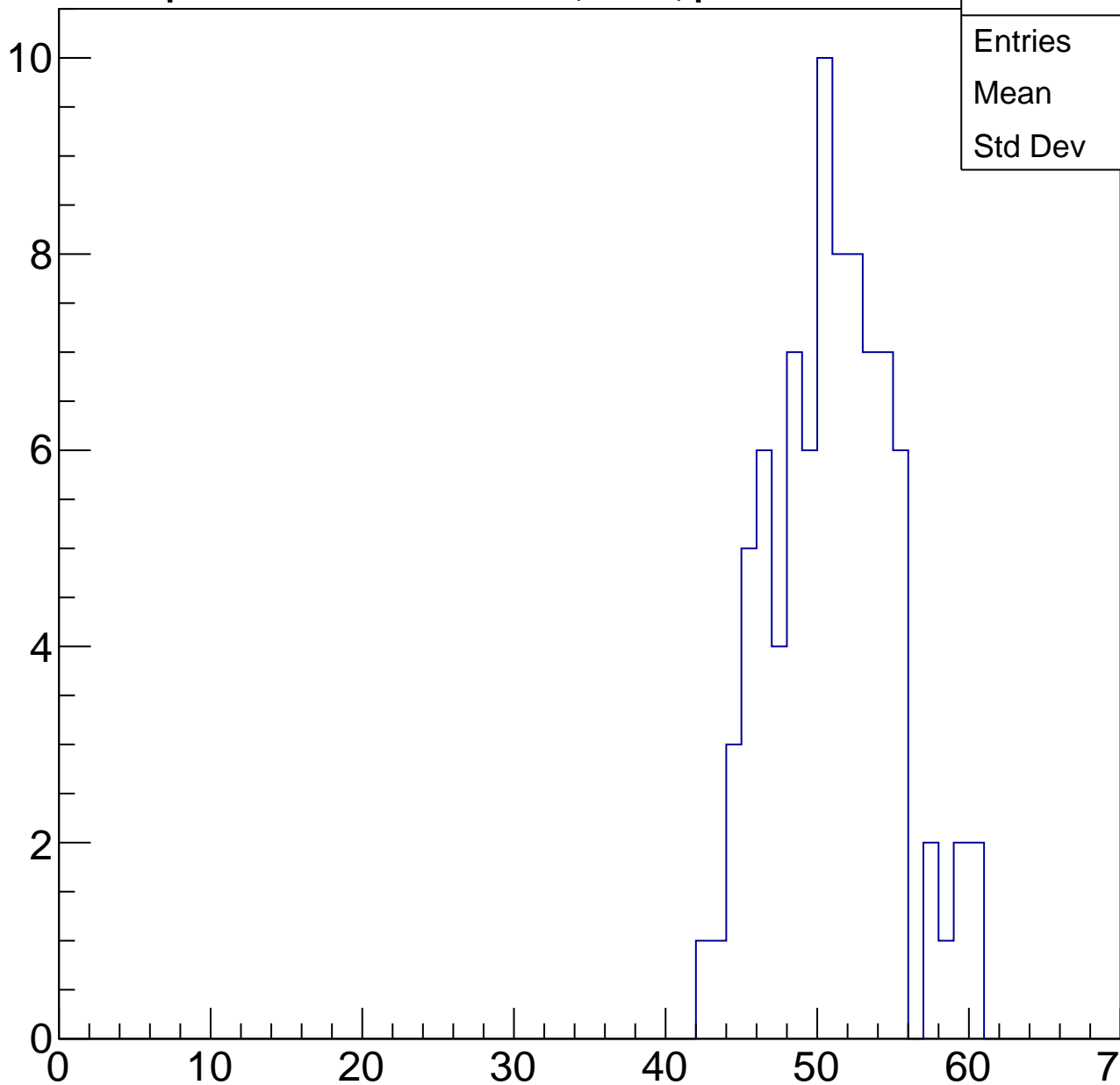
Entries	86
Mean	50.57
Std Dev	3.996

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

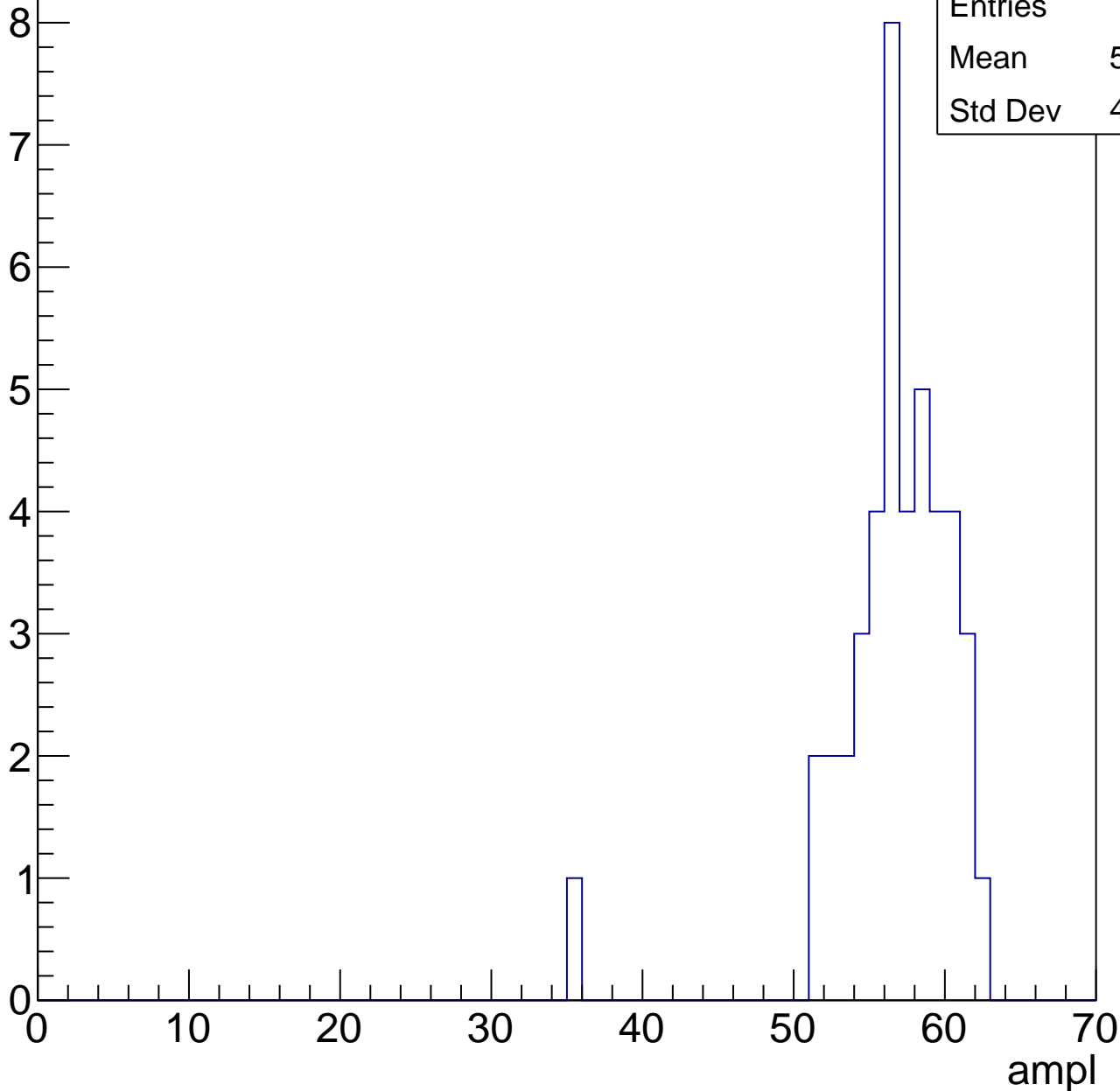


# B1L100S, U2-ch123, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	43
Mean	56.19
Std Dev	4.288

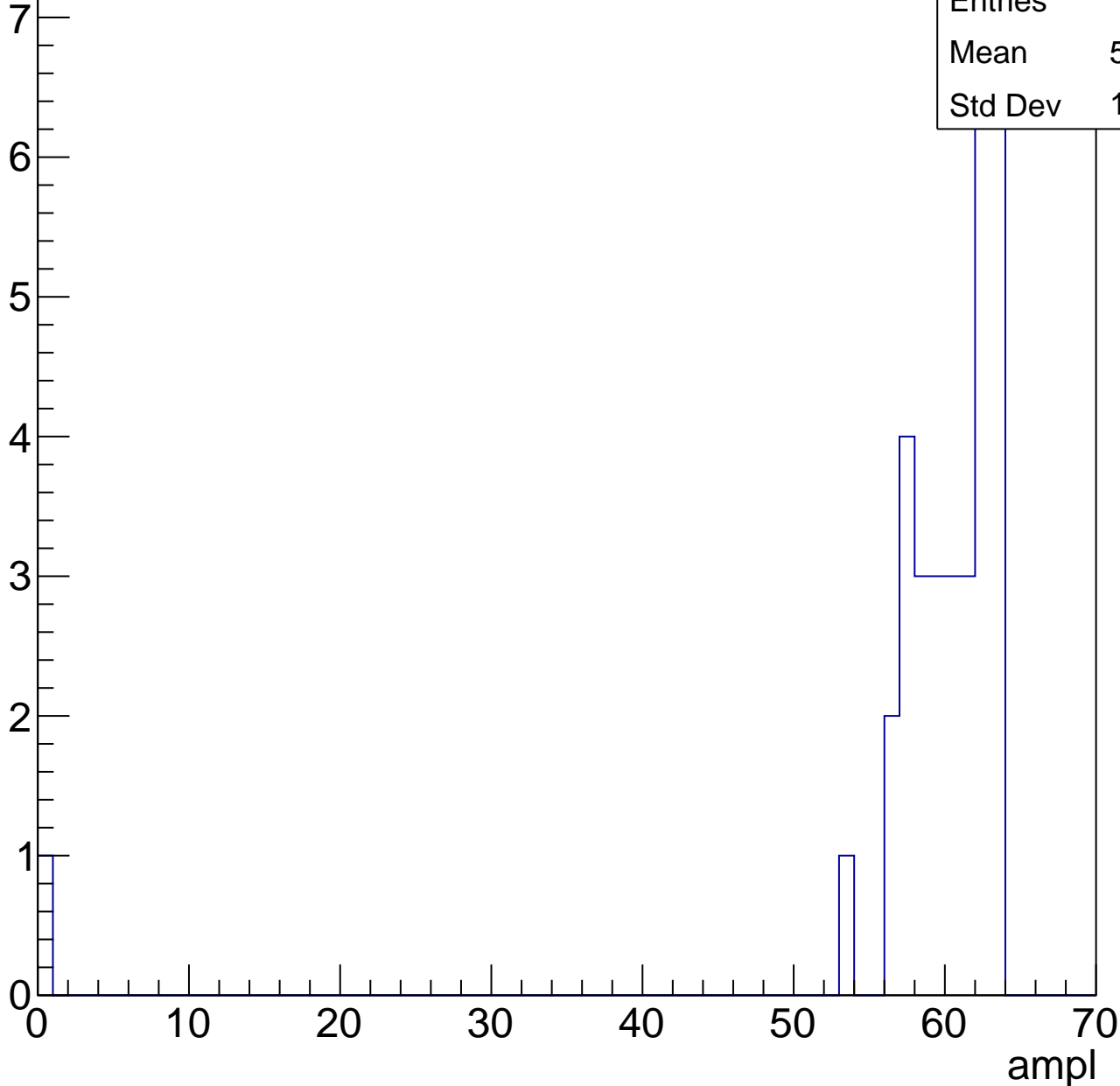


# B1L100S, U2-ch123, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

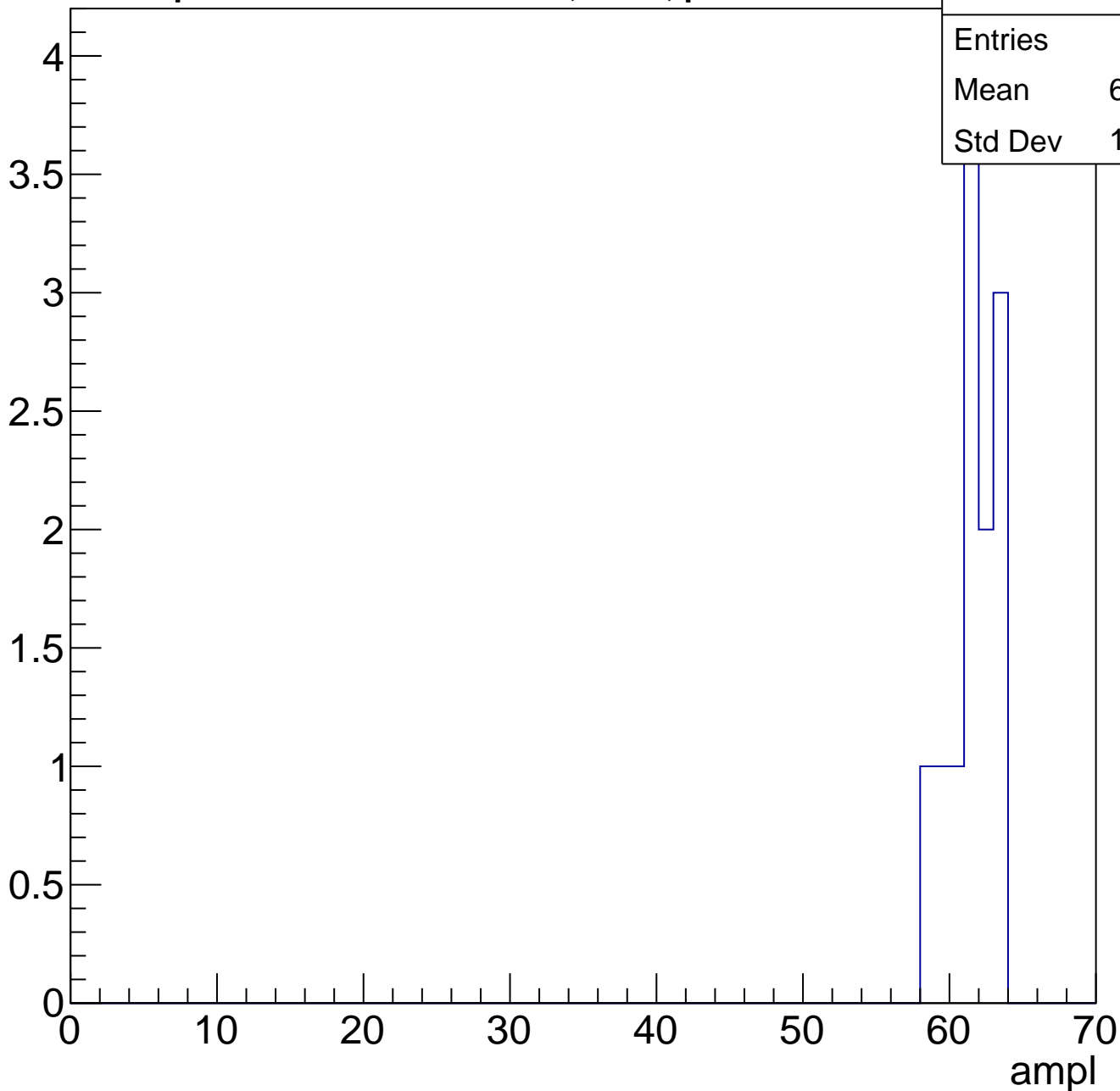
Entries	34
Mean	58.29
Std Dev	10.47



# B1L100S, U2-ch123, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry





# B1L100S, U2-ch123, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



# B1L100S, U2-ch124, adc0

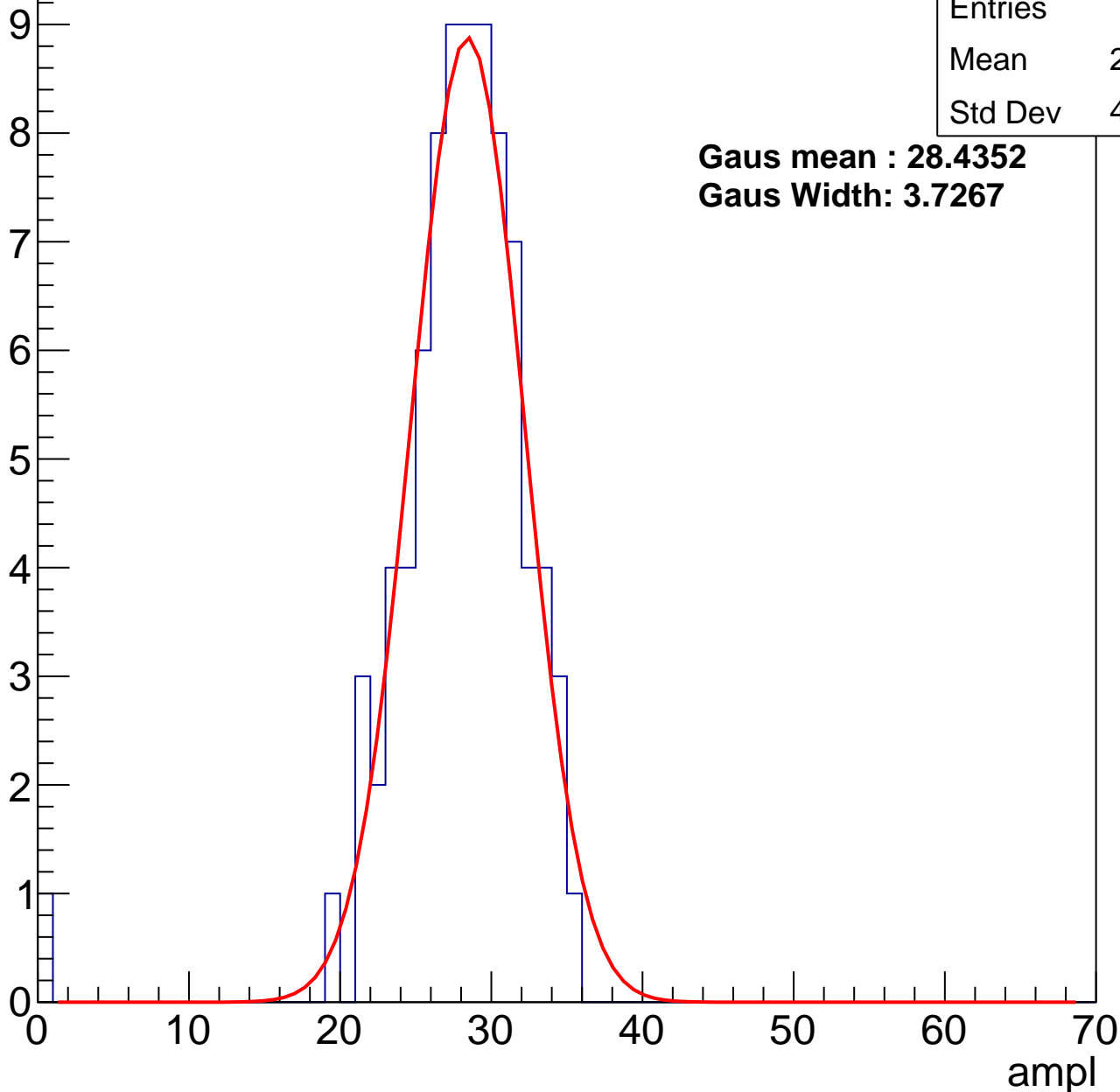
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	83
Mean	27.49
Std Dev	4.587

**Gaus mean : 28.4352**

**Gaus Width: 3.7267**



# B1L100S, U2-ch124, adc1

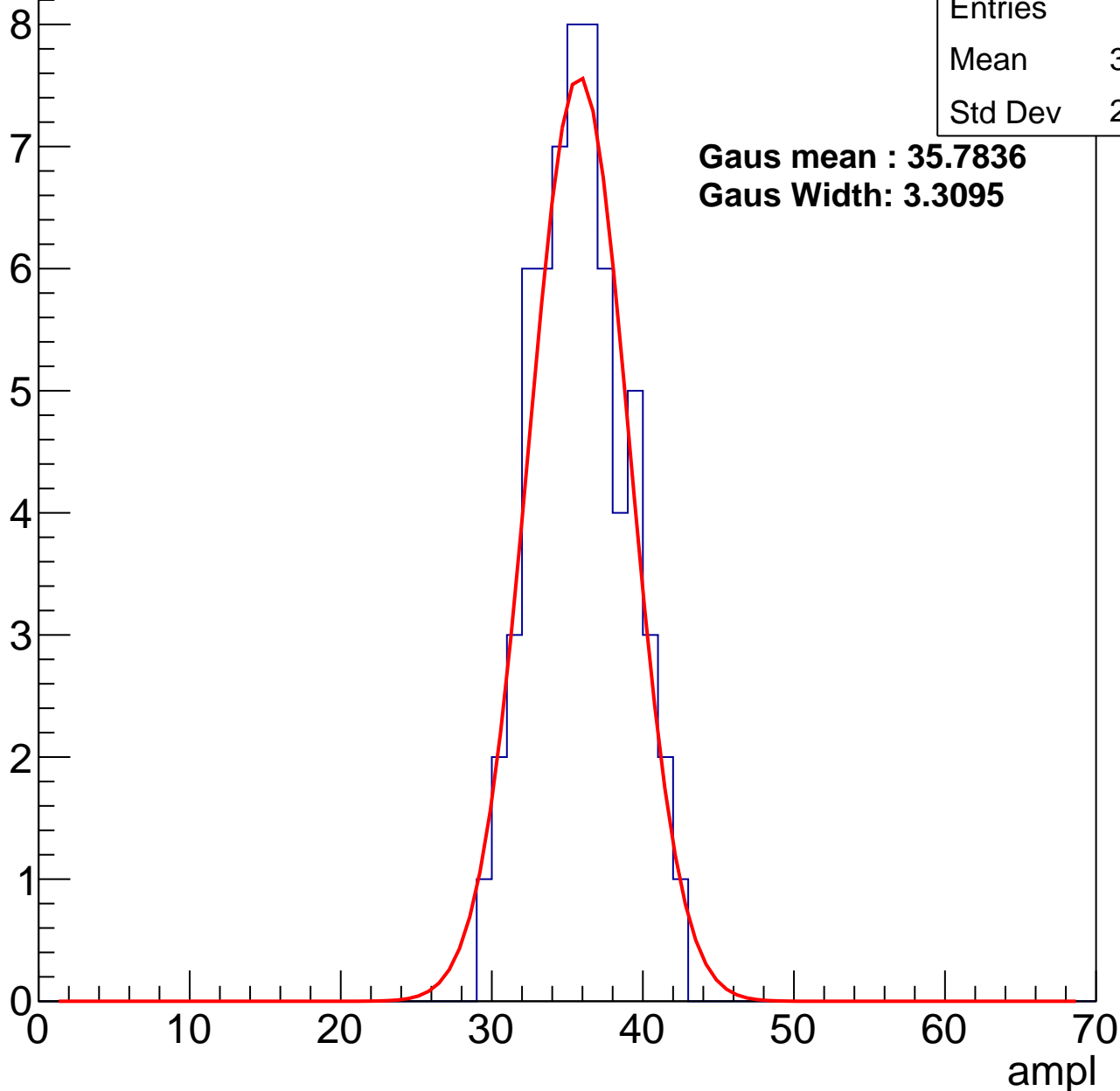
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	62
Mean	35.34
Std Dev	2.994

**Gaus mean : 35.7836**

**Gaus Width: 3.3095**



# B1L100S, U2-ch124, adc2

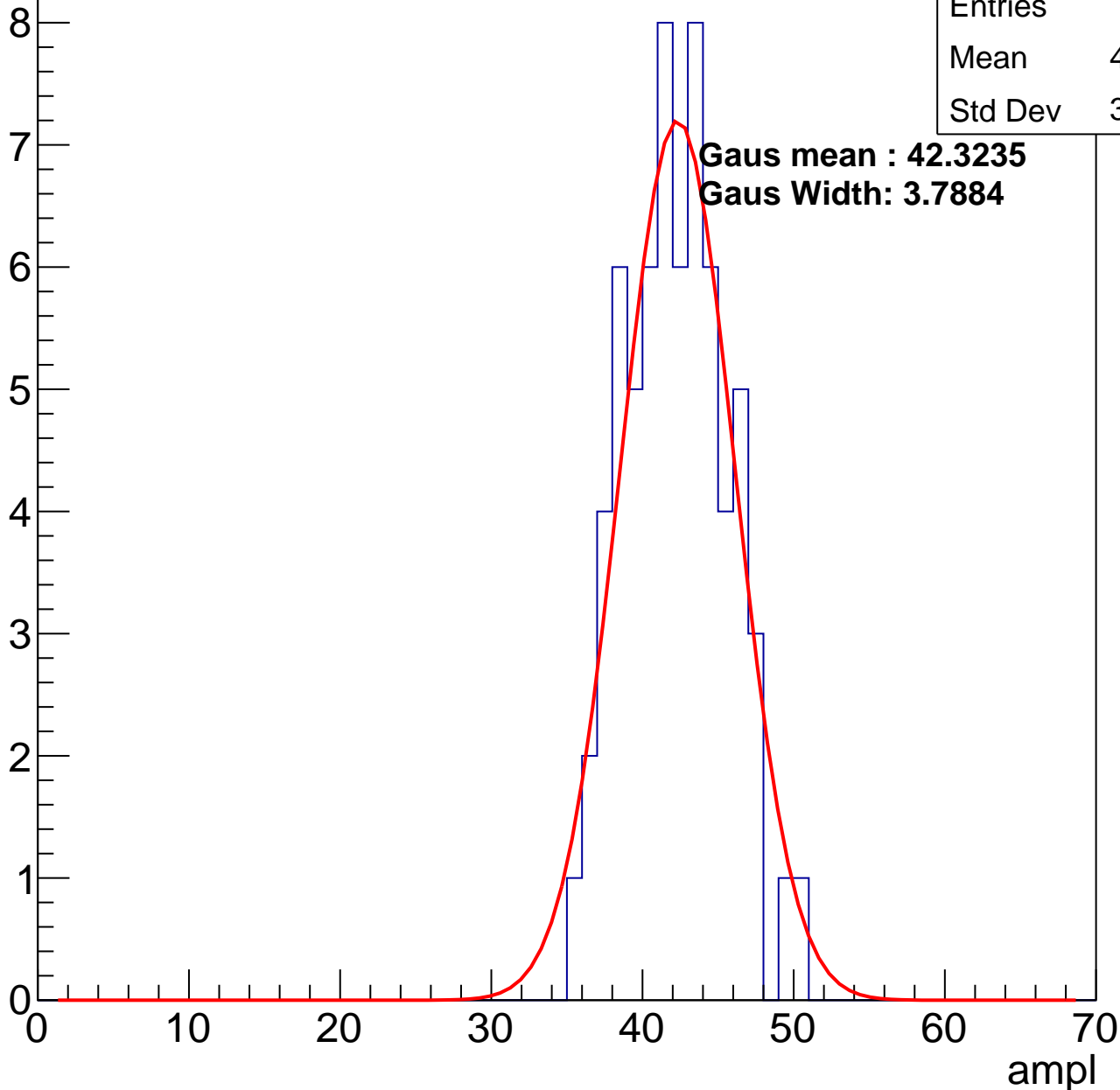
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	66
Mean	41.76
Std Dev	3.317

**Gaus mean : 42.3235**

**Gaus Width: 3.7884**

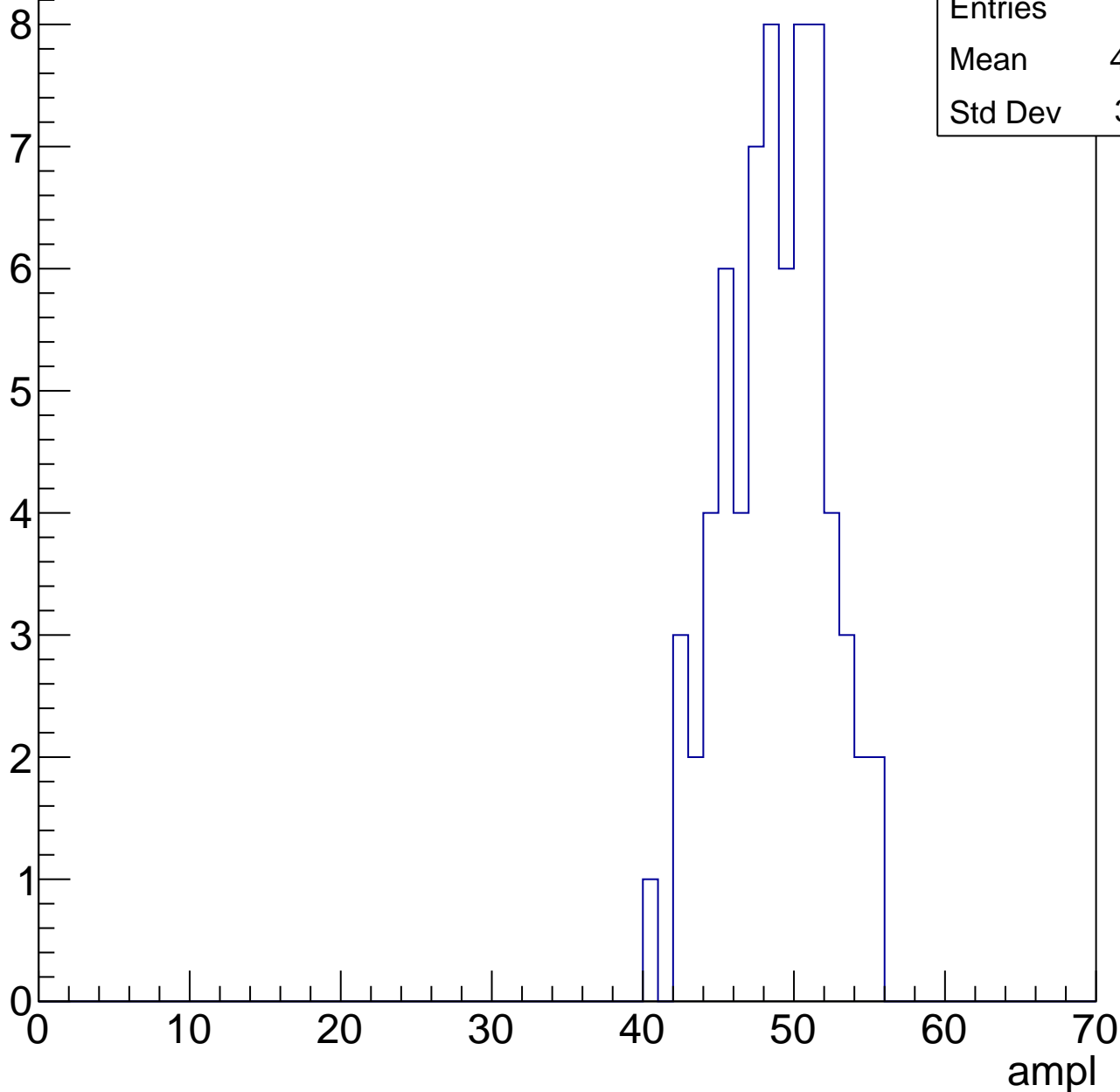


# B1L100S, U2-ch124, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	68
Mean	48.26
Std Dev	3.381

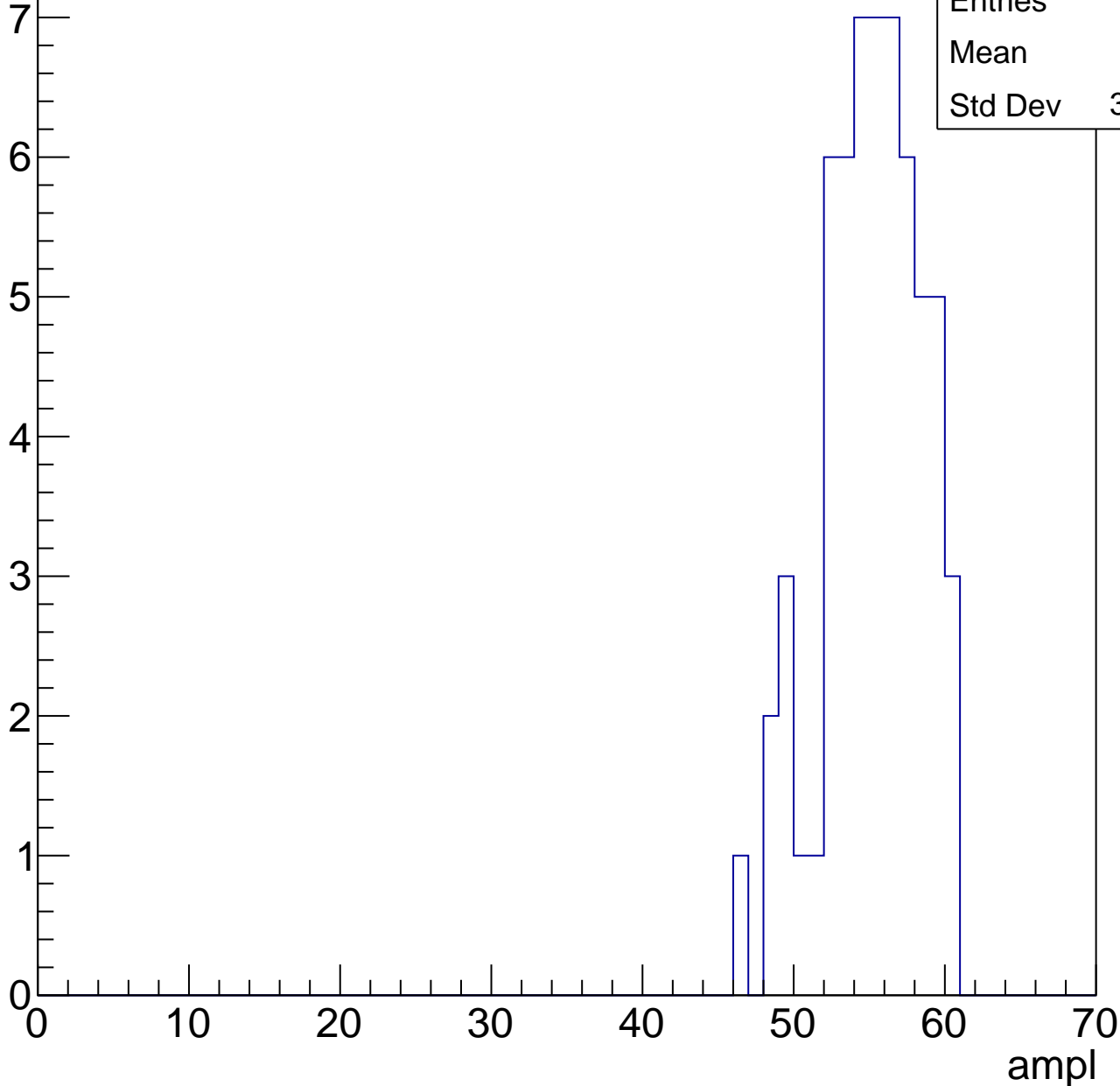


# B1L100S, U2-ch124, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	60
Mean	54.7
Std Dev	3.262



# B1L100S, U2-ch124, adc5

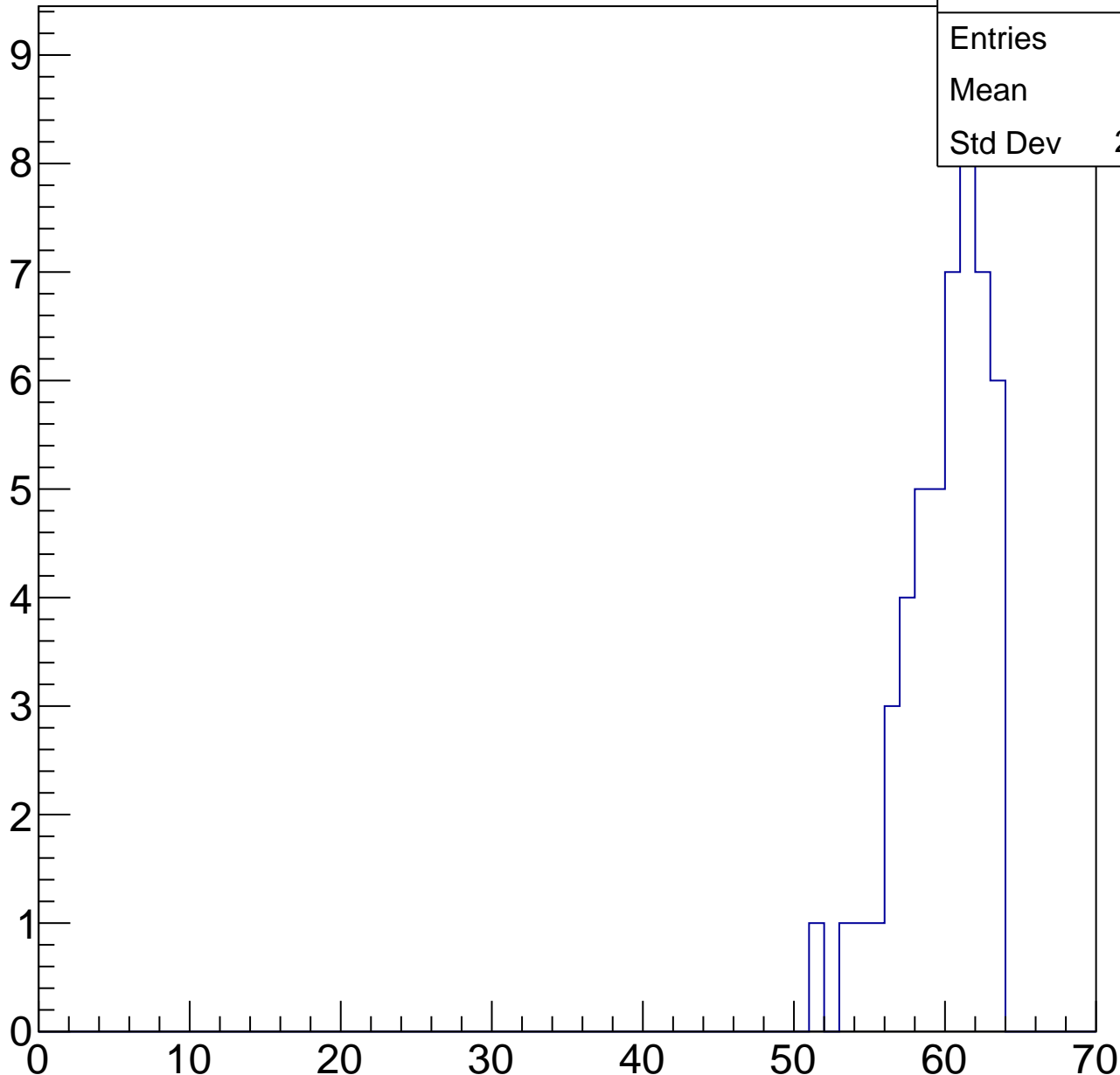
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	50
Mean	59.5
Std Dev	2.751

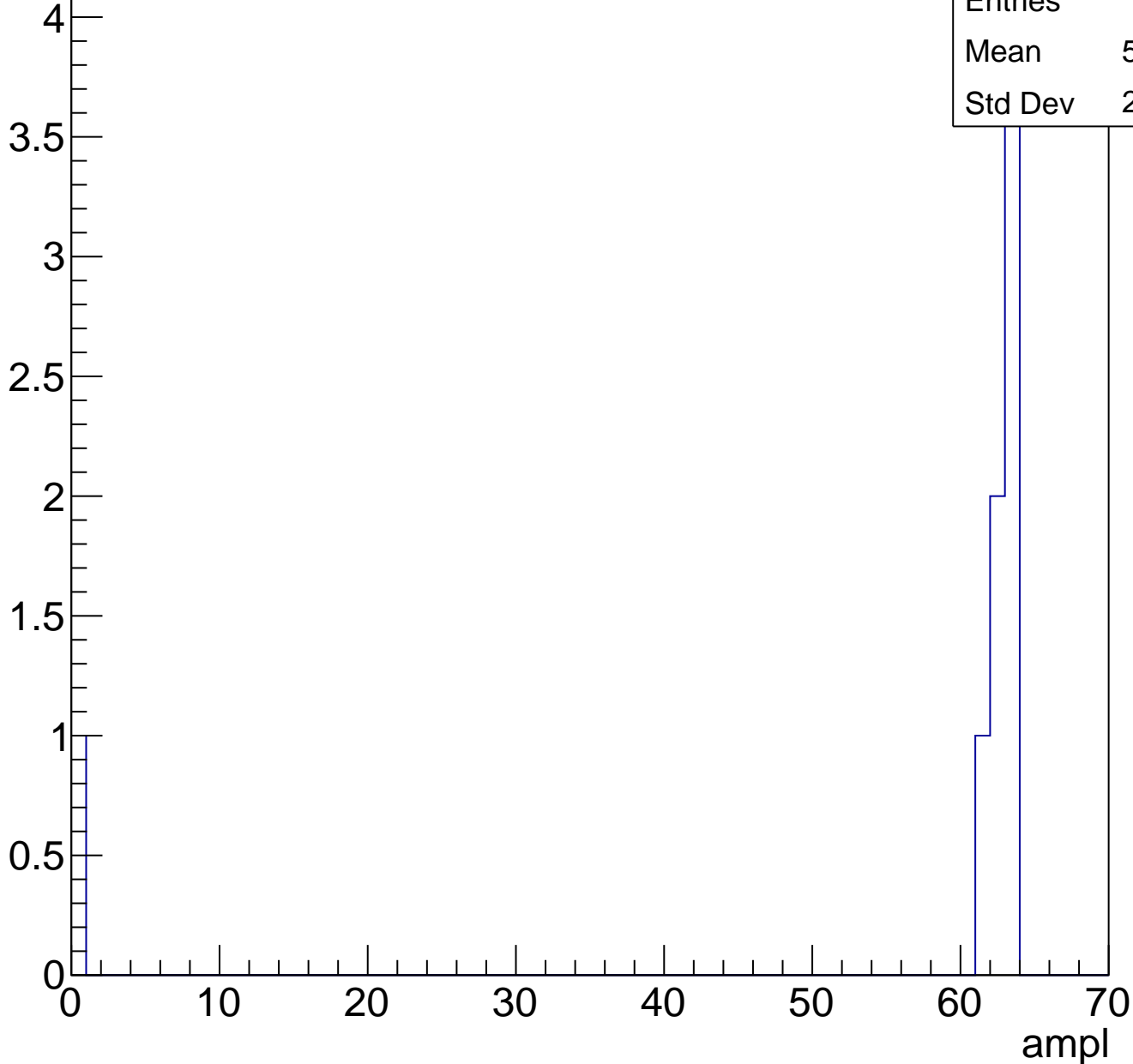
ampl



# B1L100S, U2-ch124, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry





# B1L100S, U2-ch124, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



# B1L100S, U2-ch125, adc0

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	78
Mean	27.91
Std Dev	5.702

**Gaus mean : 28.7286**

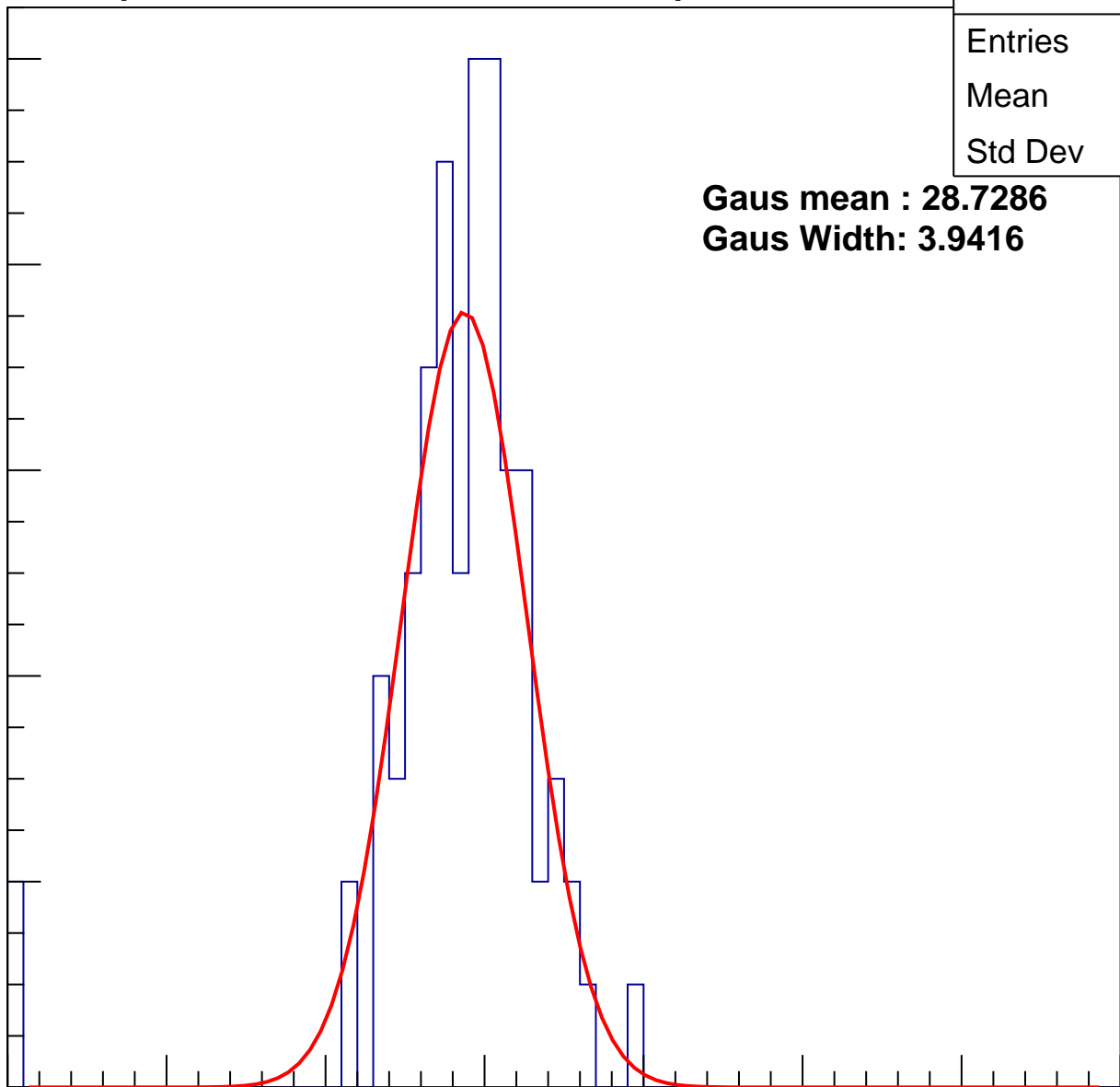
**Gaus Width: 3.9416**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L100S, U2-ch125, adc1

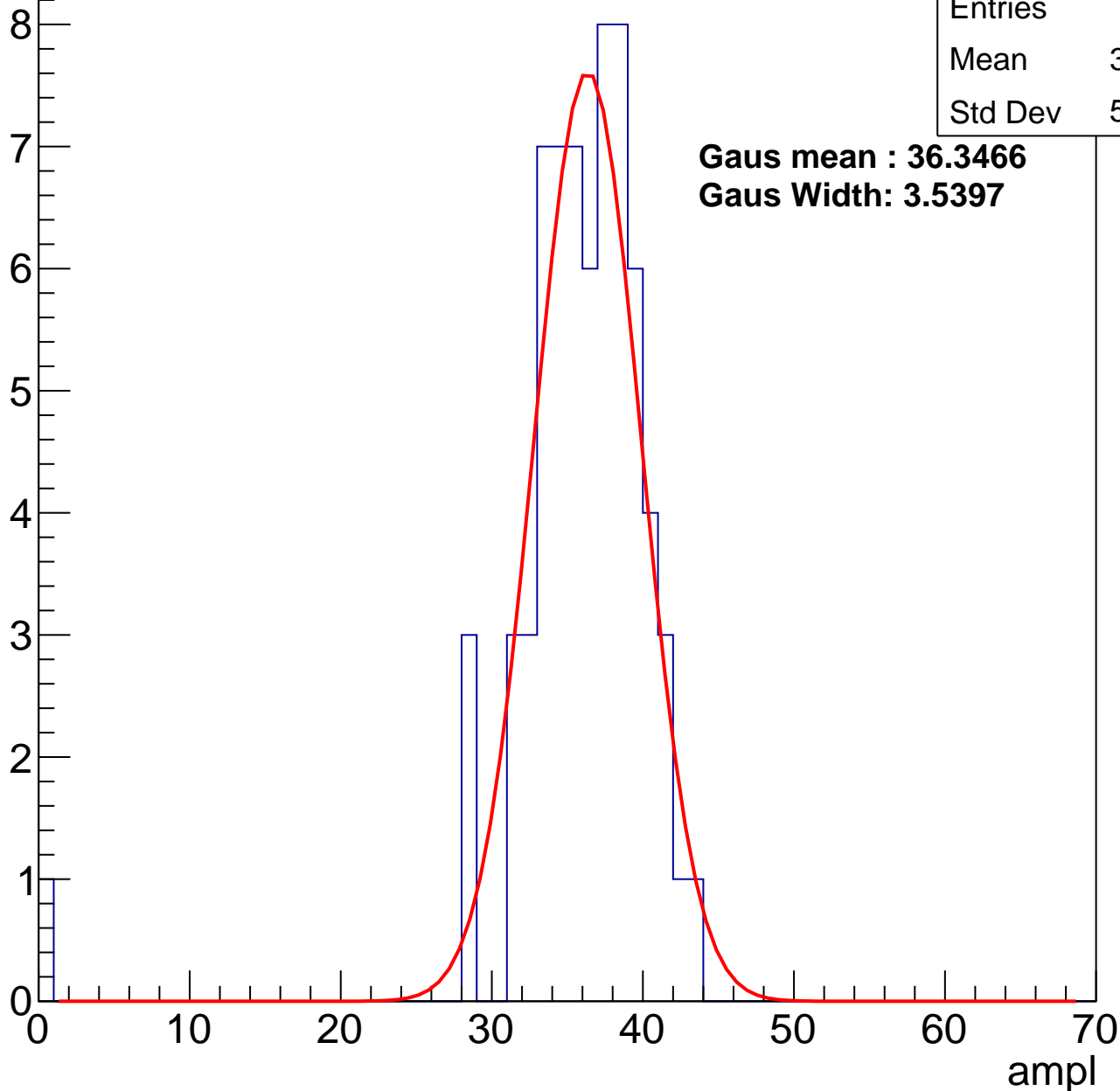
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	68
Mean	35.37
Std Dev	5.423

**Gaus mean : 36.3466**

**Gaus Width: 3.5397**



# B1L100S, U2-ch125, adc2

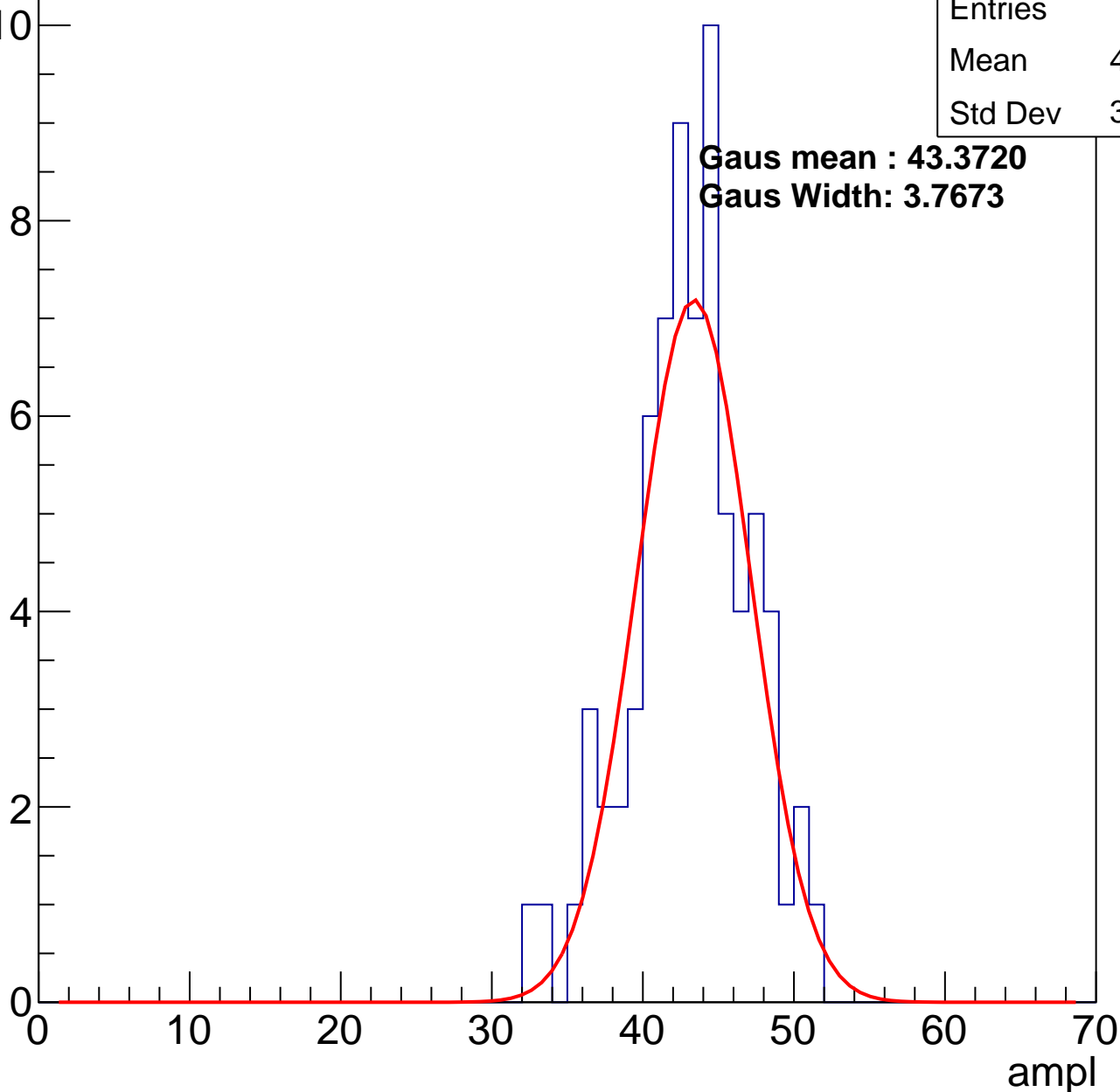
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	74
Mean	42.66
Std Dev	3.905

**Gaus mean : 43.3720**

**Gaus Width: 3.7673**

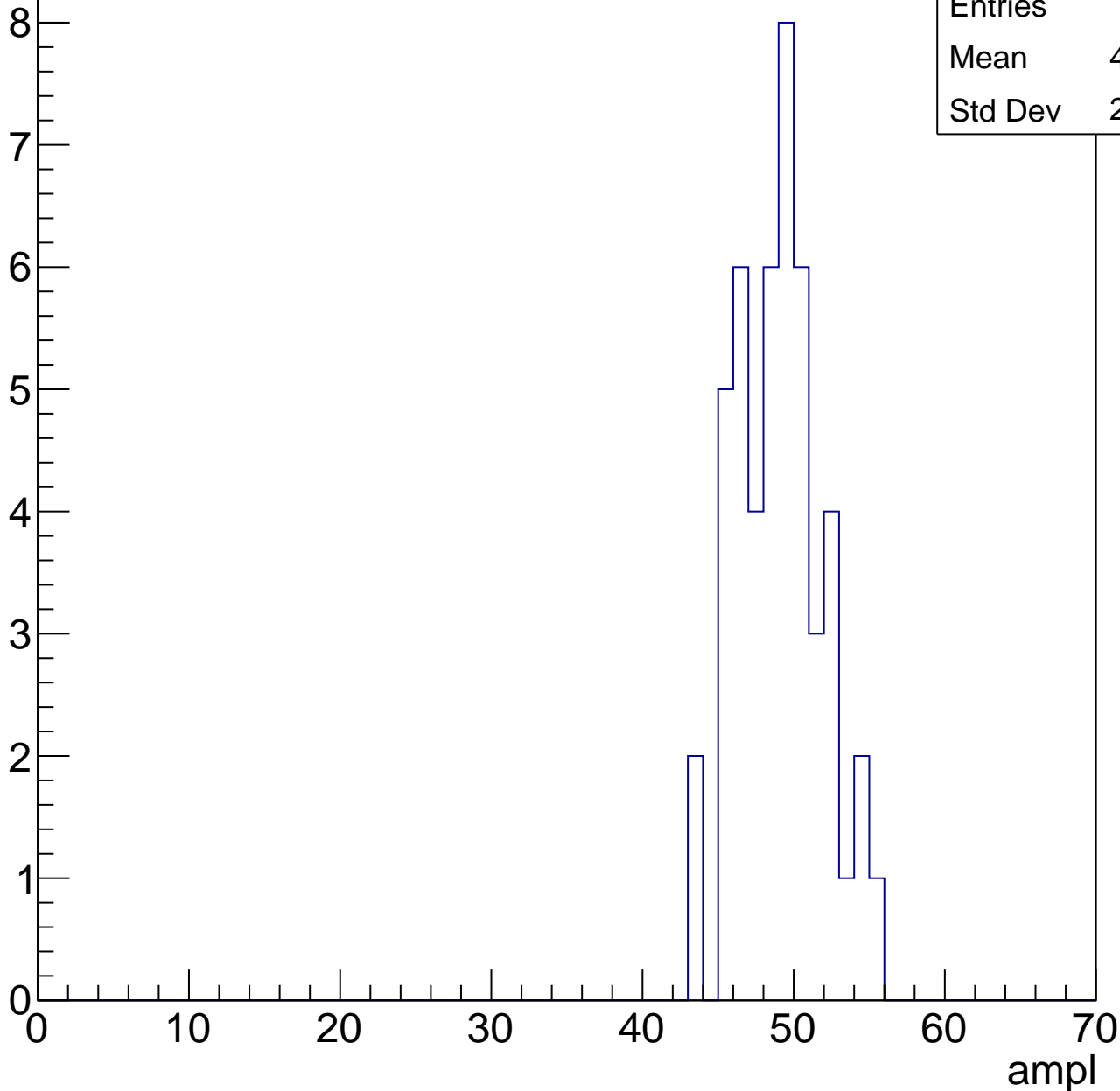


# B1L100S, U2-ch125, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	48
Mean	48.58
Std Dev	2.798

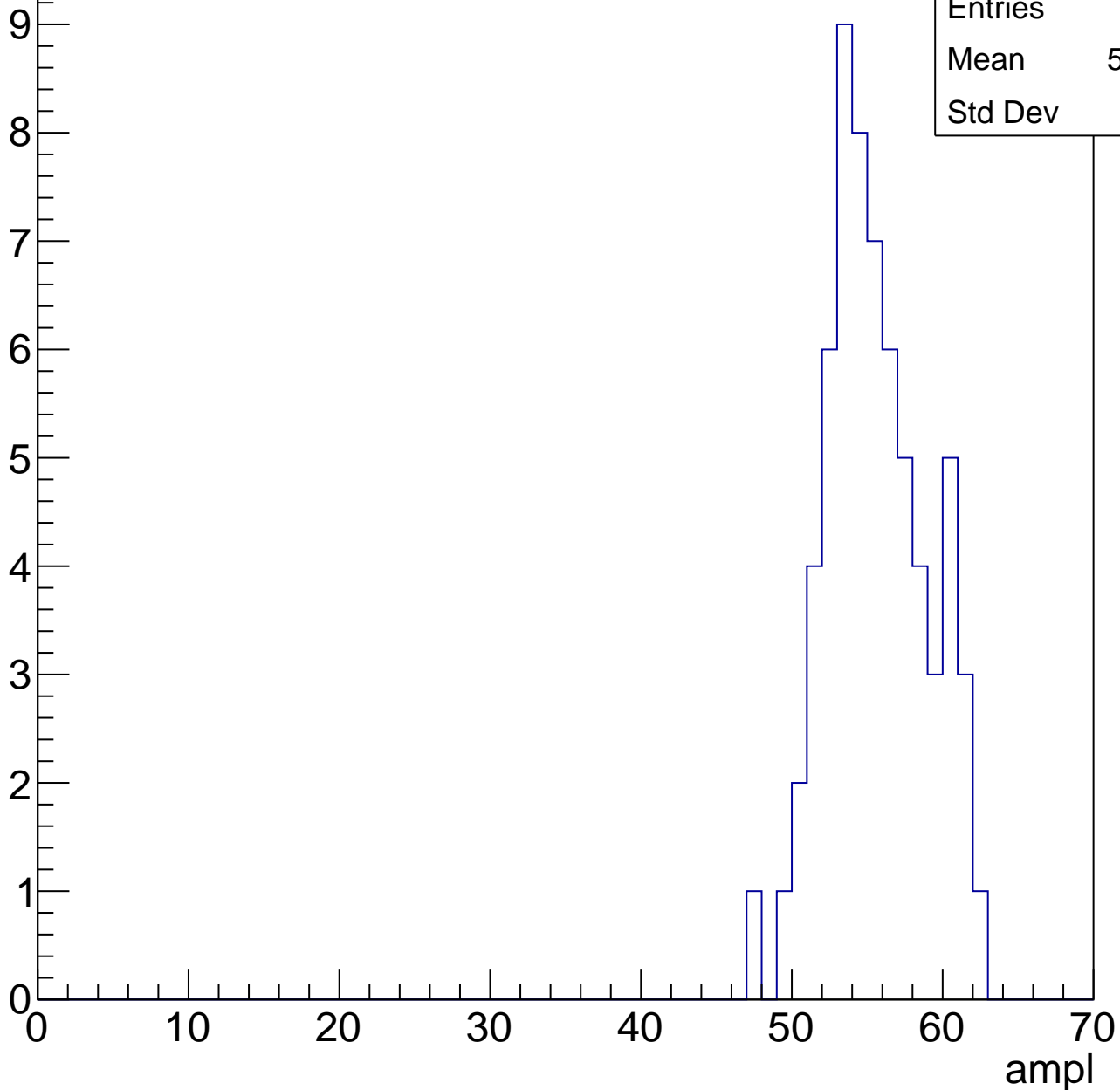


# B1L100S, U2-ch125, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	65
Mean	55.09
Std Dev	3.29

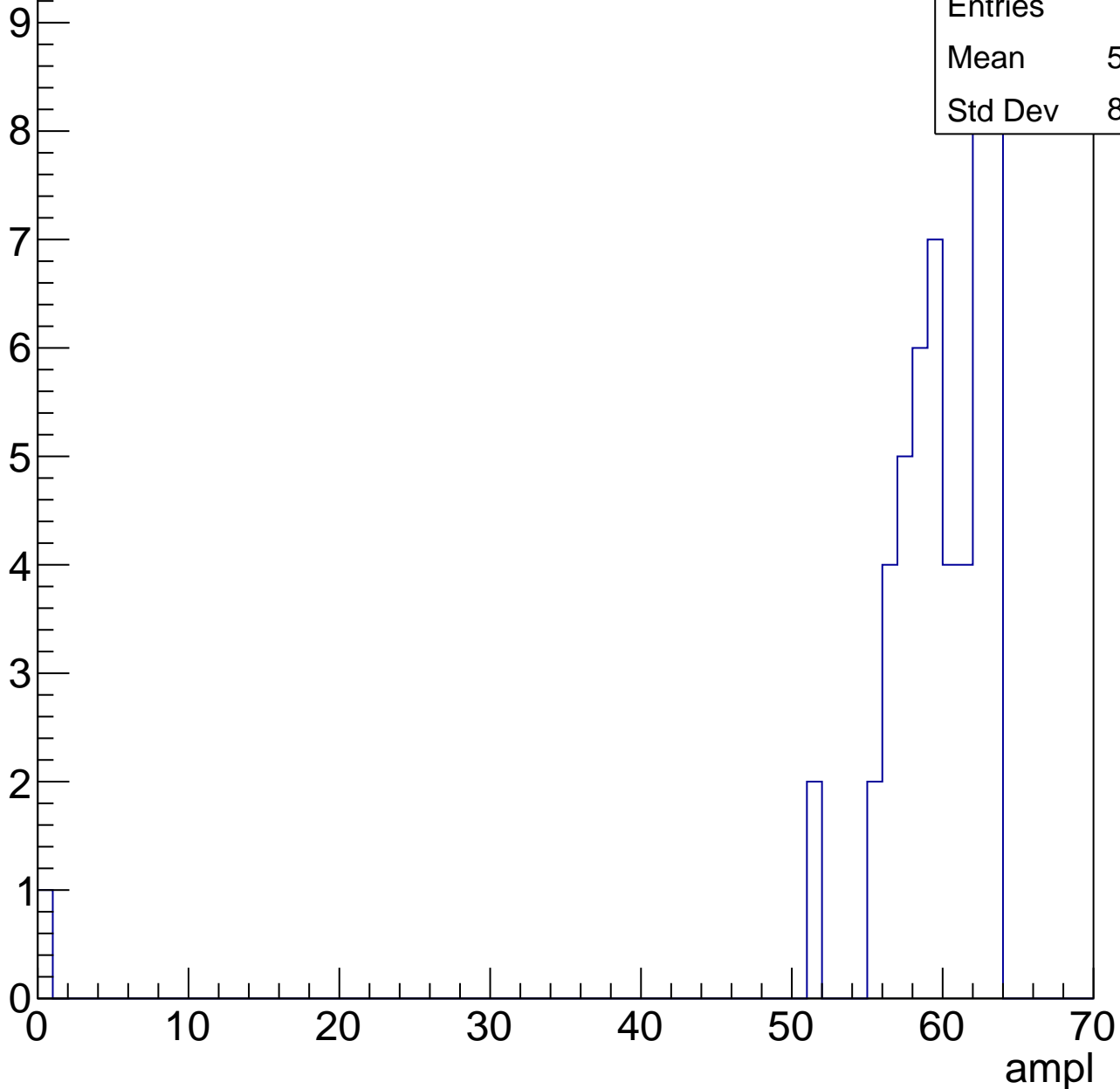


# B1L100S, U2-ch125, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

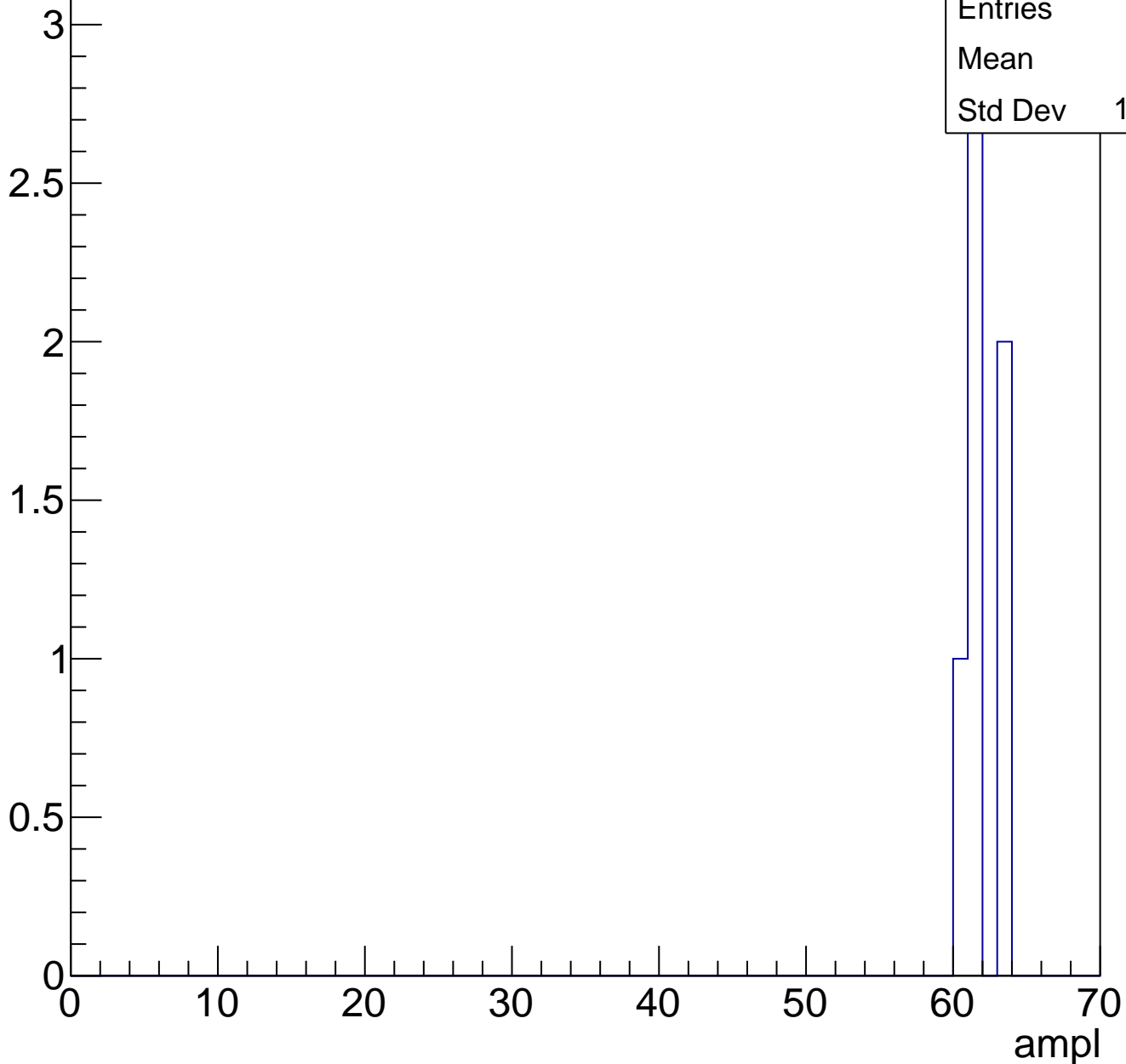
Entries	52
Mean	58.23
Std Dev	8.662



# B1L100S, U2-ch125, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	6
Mean	61.5
Std Dev	1.118



# B1L100S, U2-ch125, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L100S, U2-ch126, adc0

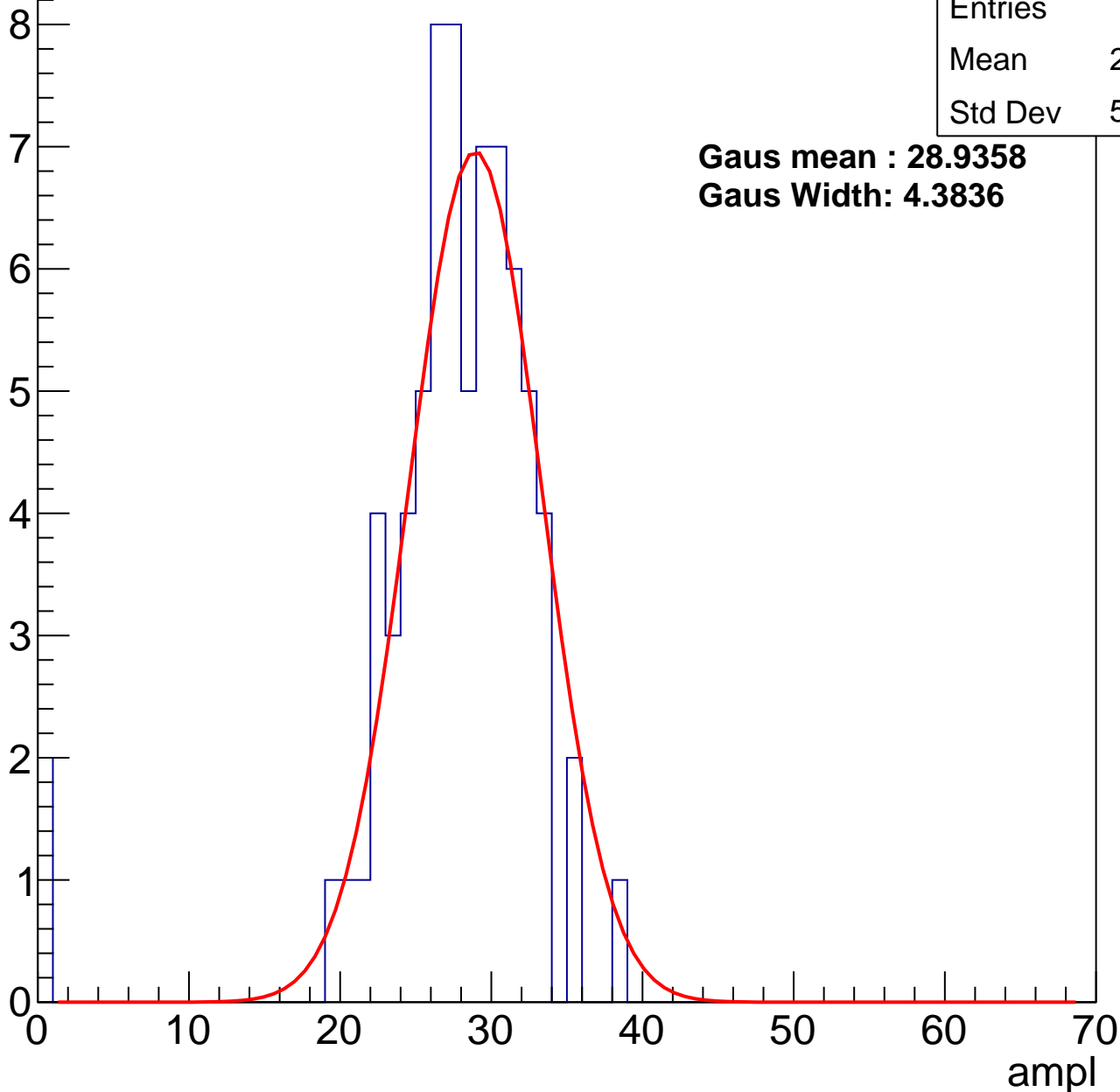
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	74
Mean	27.04
Std Dev	5.846

**Gaus mean : 28.9358**

**Gaus Width: 4.3836**



# B1L100S, U2-ch126, adc1

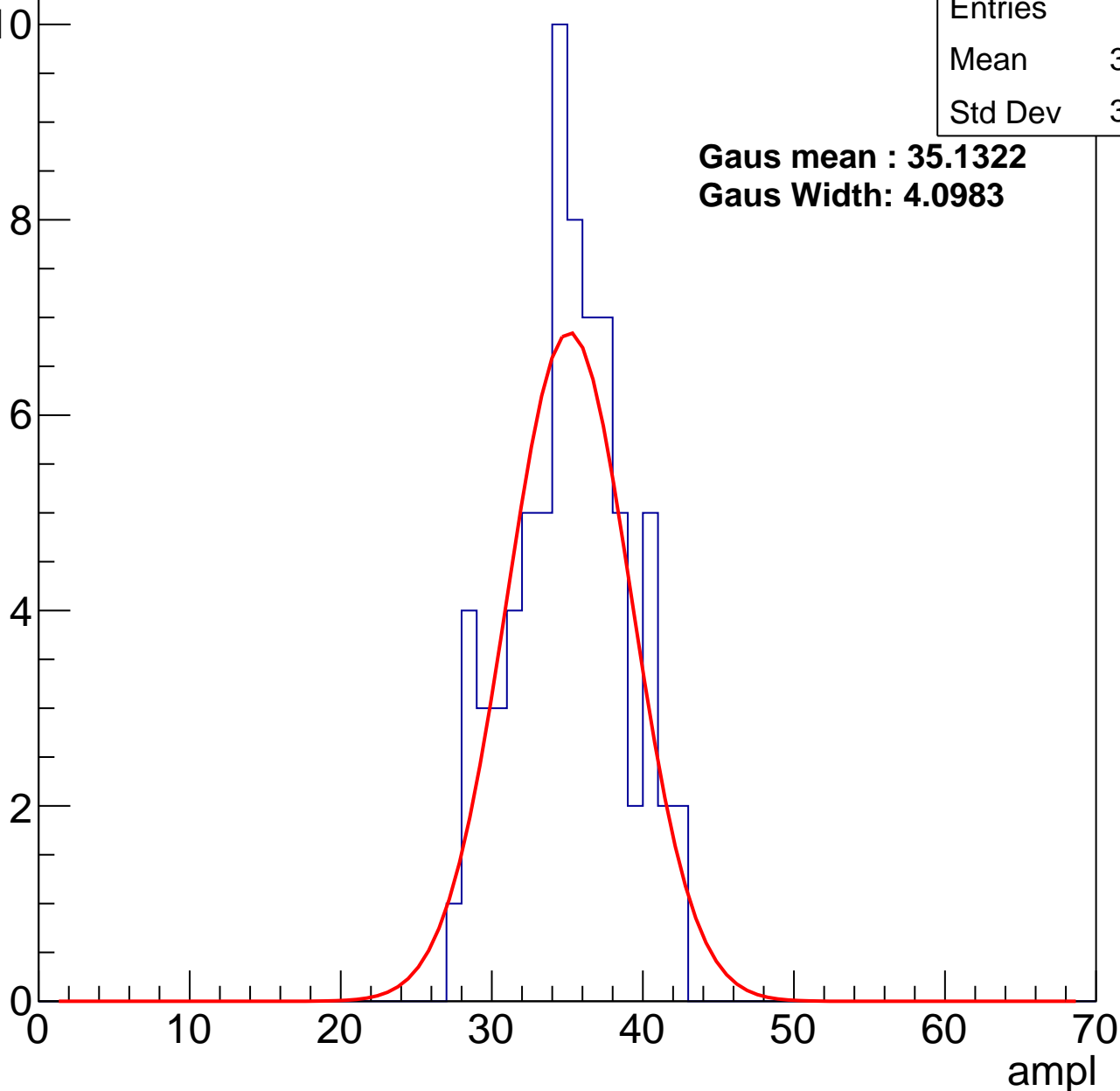
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	73
Mean	34.66
Std Dev	3.665

**Gaus mean : 35.1322**

**Gaus Width: 4.0983**



# B1L100S, U2-ch126, adc2

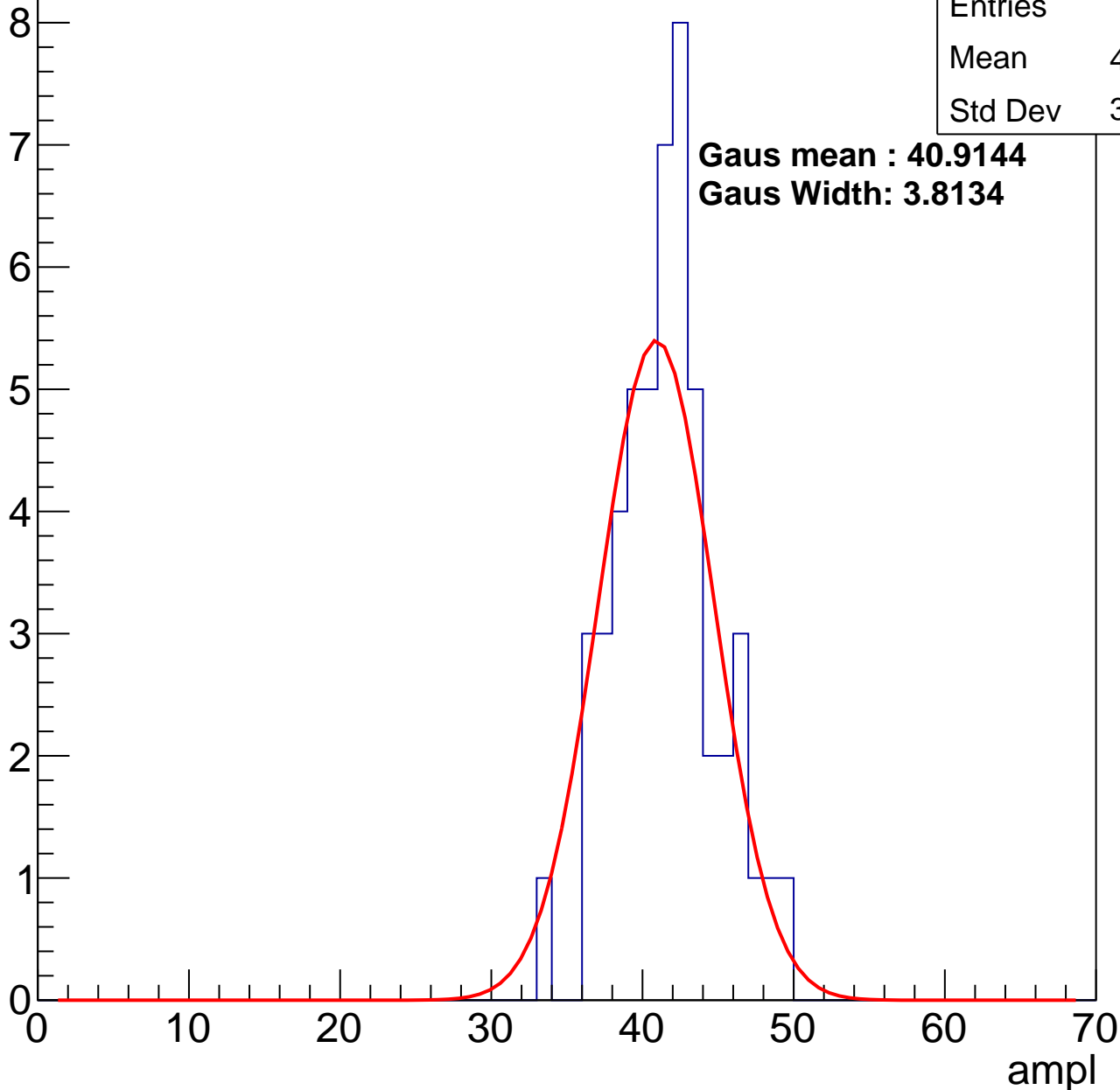
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	51
Mean	41.12
Std Dev	3.282

**Gaus mean : 40.9144**

**Gaus Width: 3.8134**

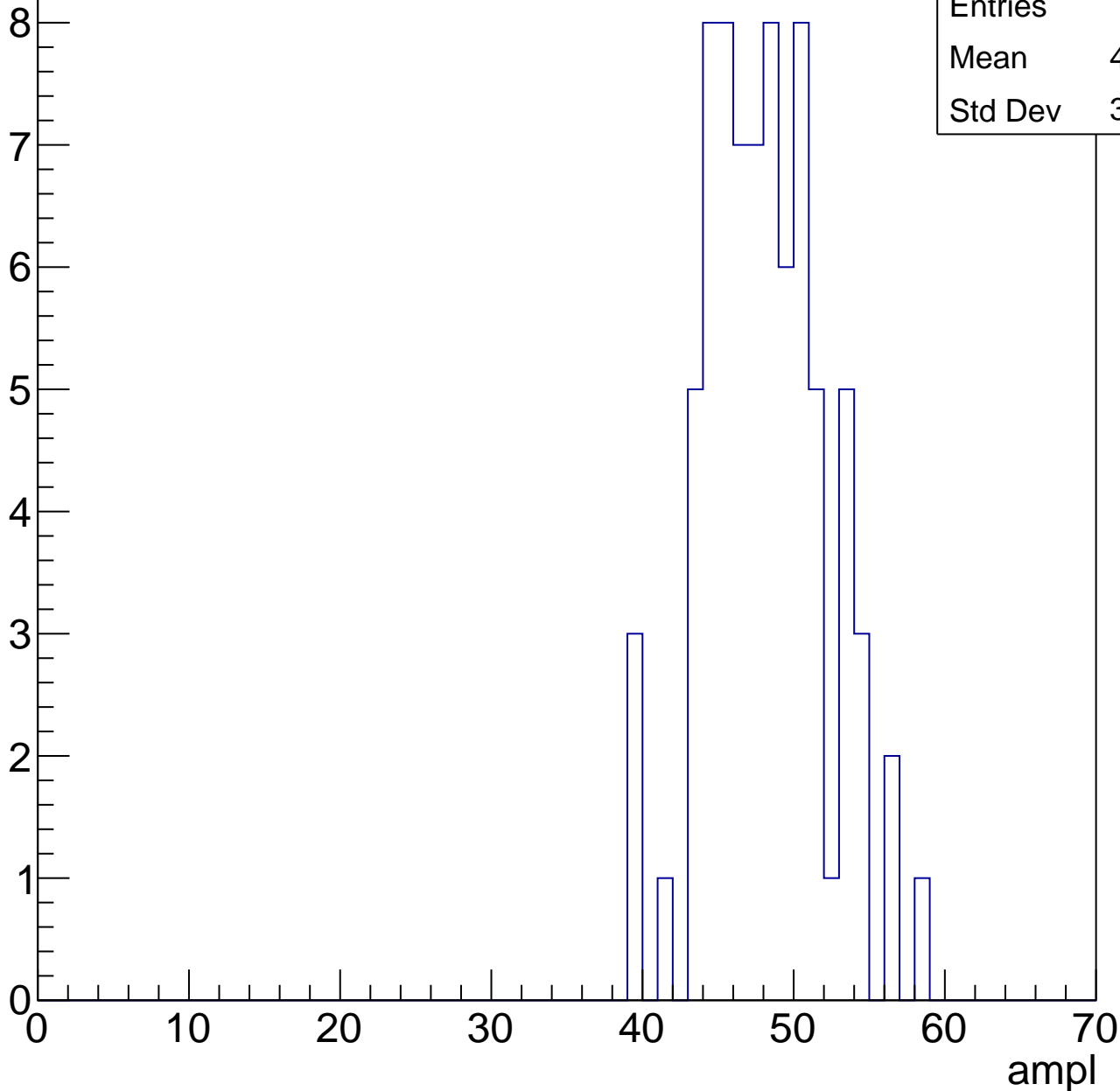


# B1L100S, U2-ch126, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

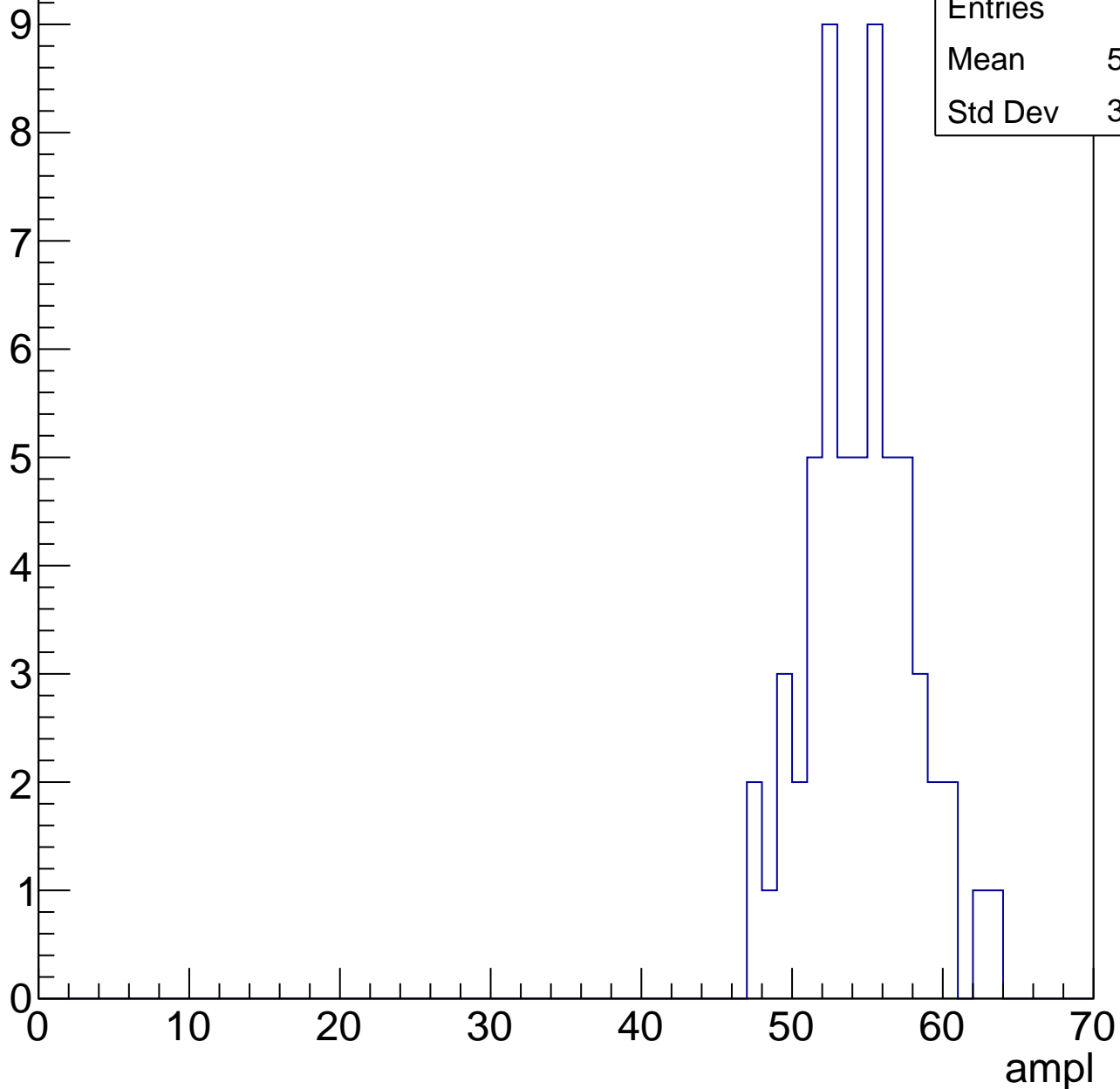
Entries	78
Mean	47.67
Std Dev	3.928



# B1L100S, U2-ch126, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

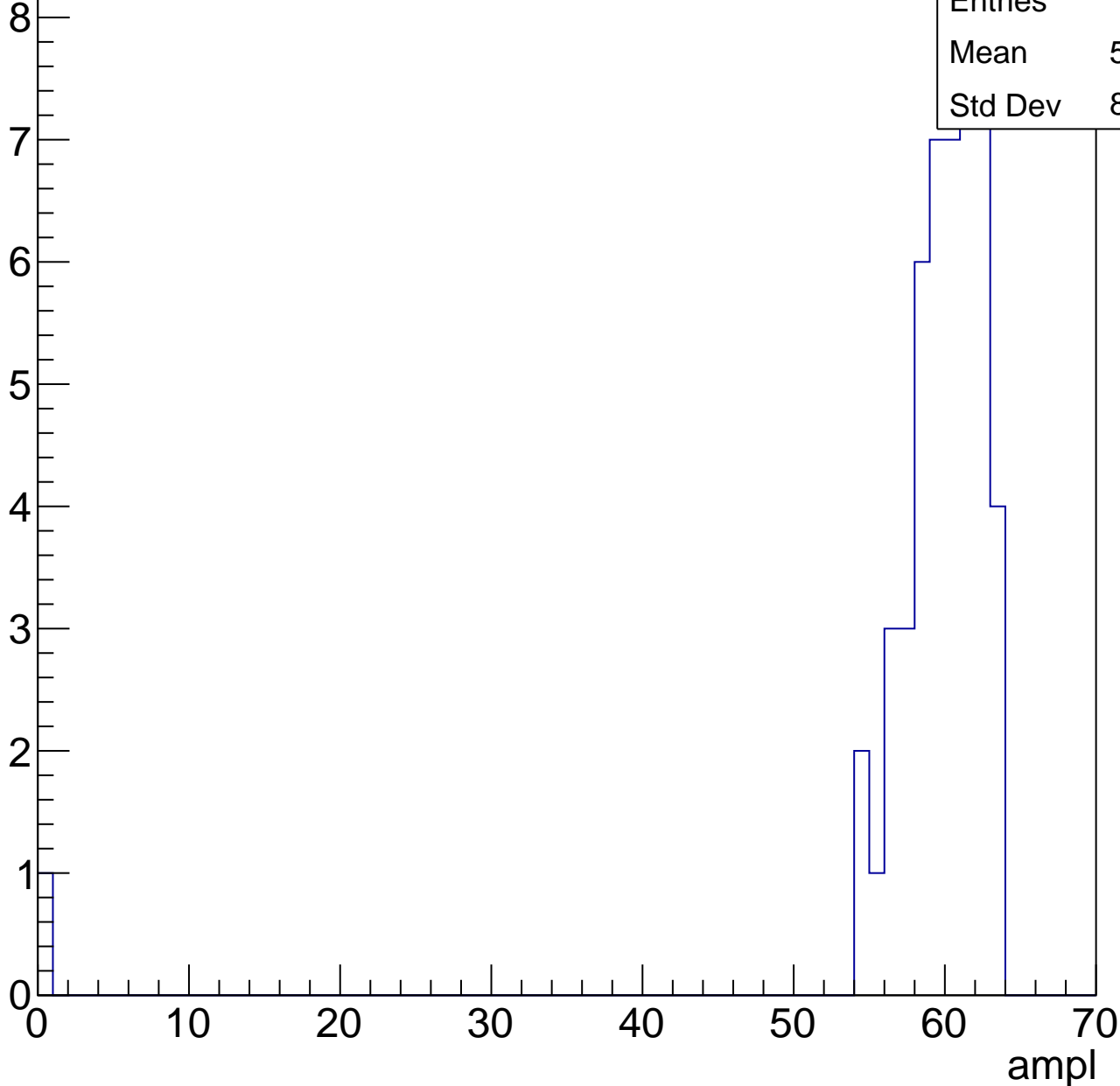


# B1L100S, U2-ch126, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	50
Mean	58.38
Std Dev	8.658

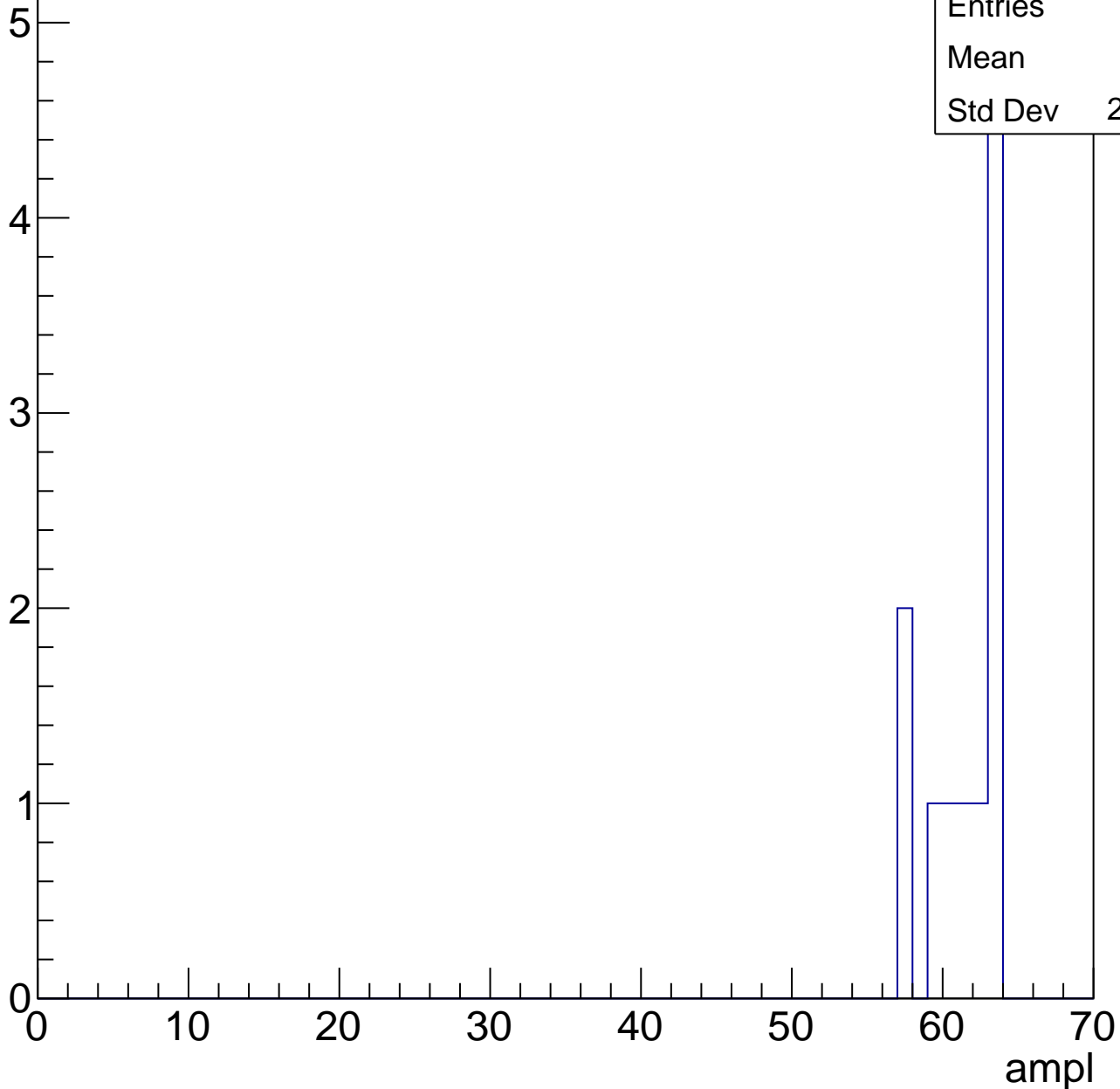


# B1L100S, U2-ch126, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	11
Mean	61
Std Dev	2.296

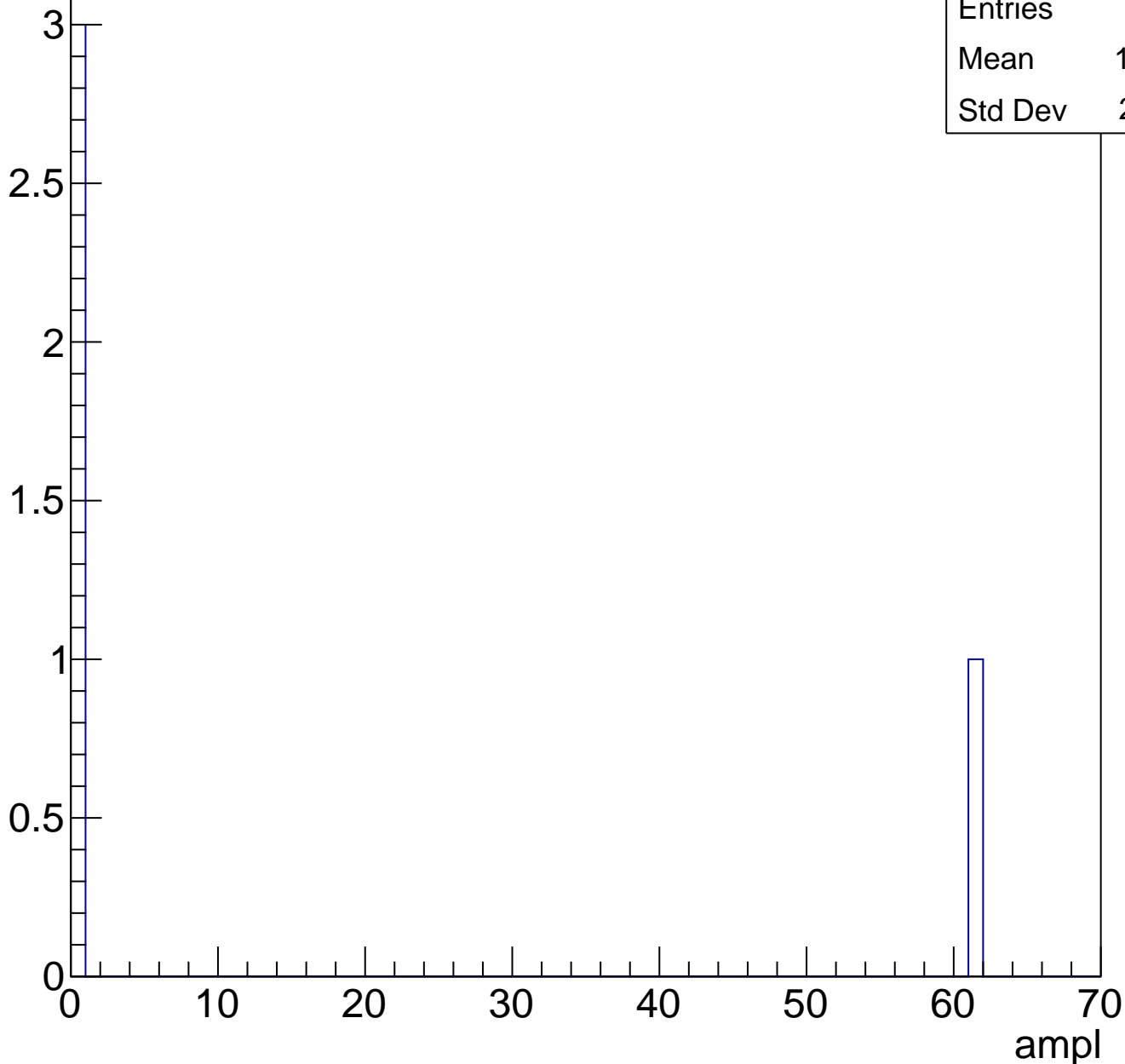




# B1L100S, U2-ch126, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



# B1L100S, U2-ch127, adc0

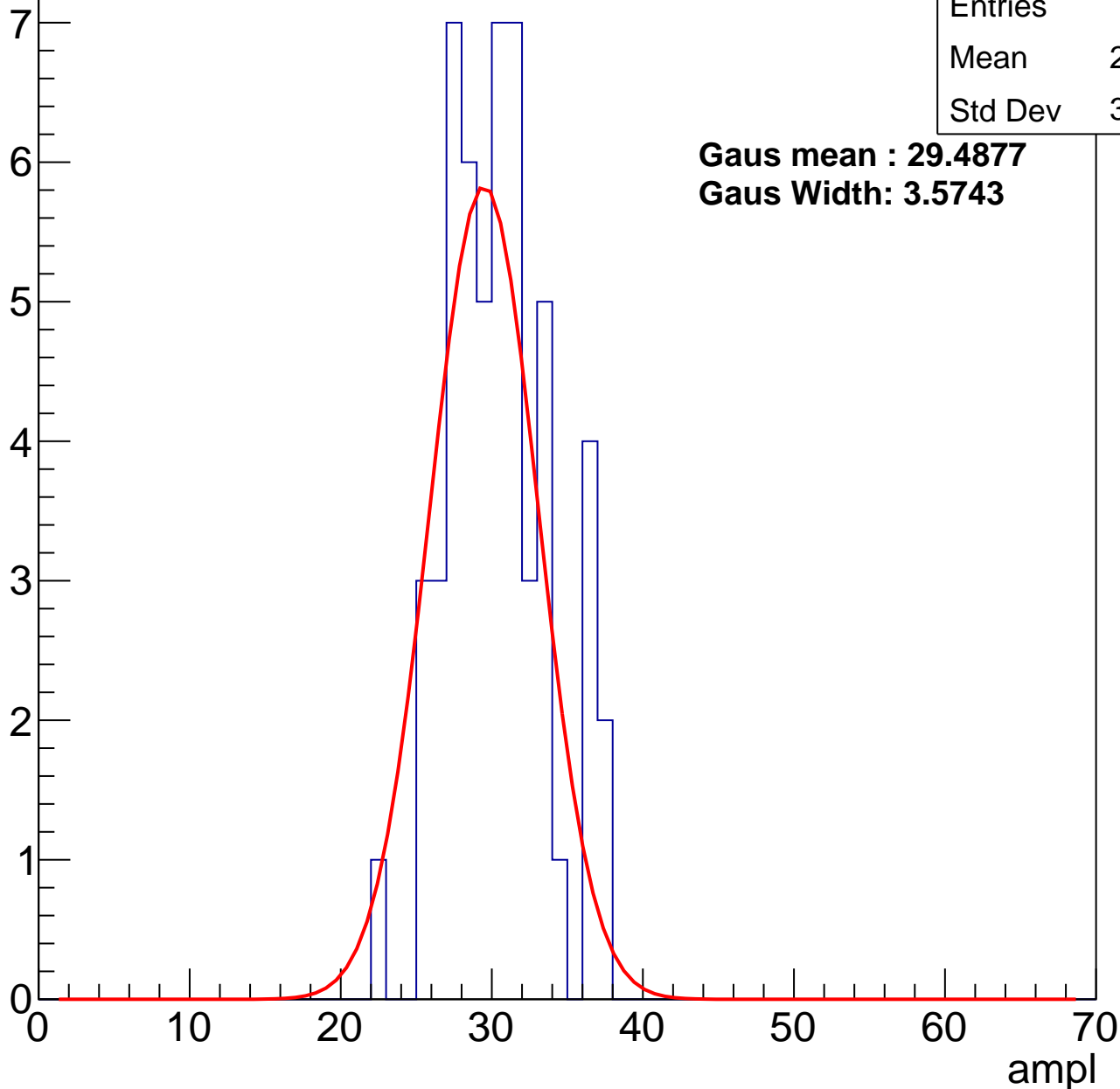
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	54
Mean	29.94
Std Dev	3.336

**Gaus mean : 29.4877**

**Gaus Width: 3.5743**

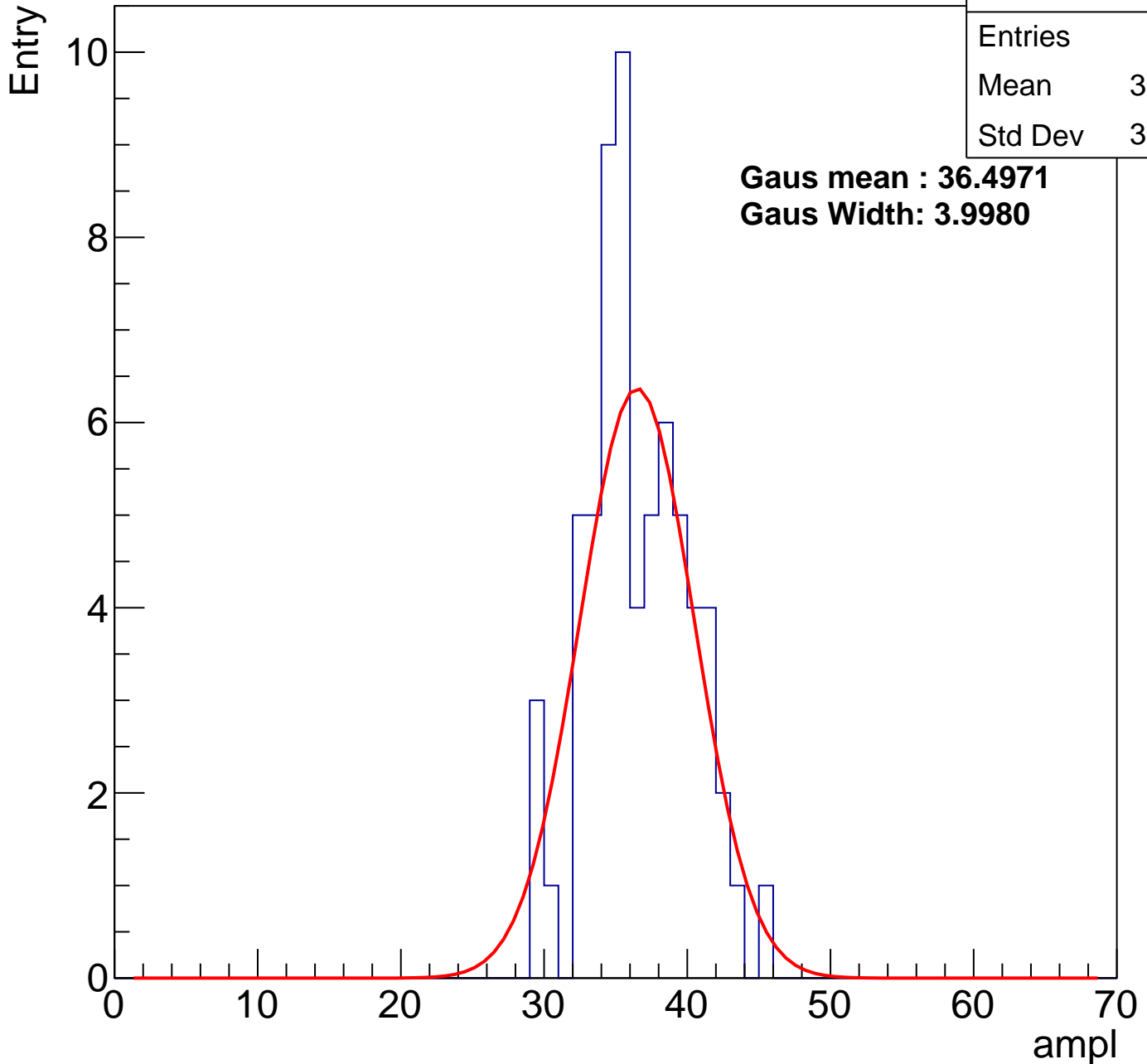


# B1L100S, U2-ch127, adc1

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	65
Mean	36.09
Std Dev	3.494

**Gaus mean : 36.4971**  
**Gaus Width: 3.9980**



# B1L100S, U2-ch127, adc2

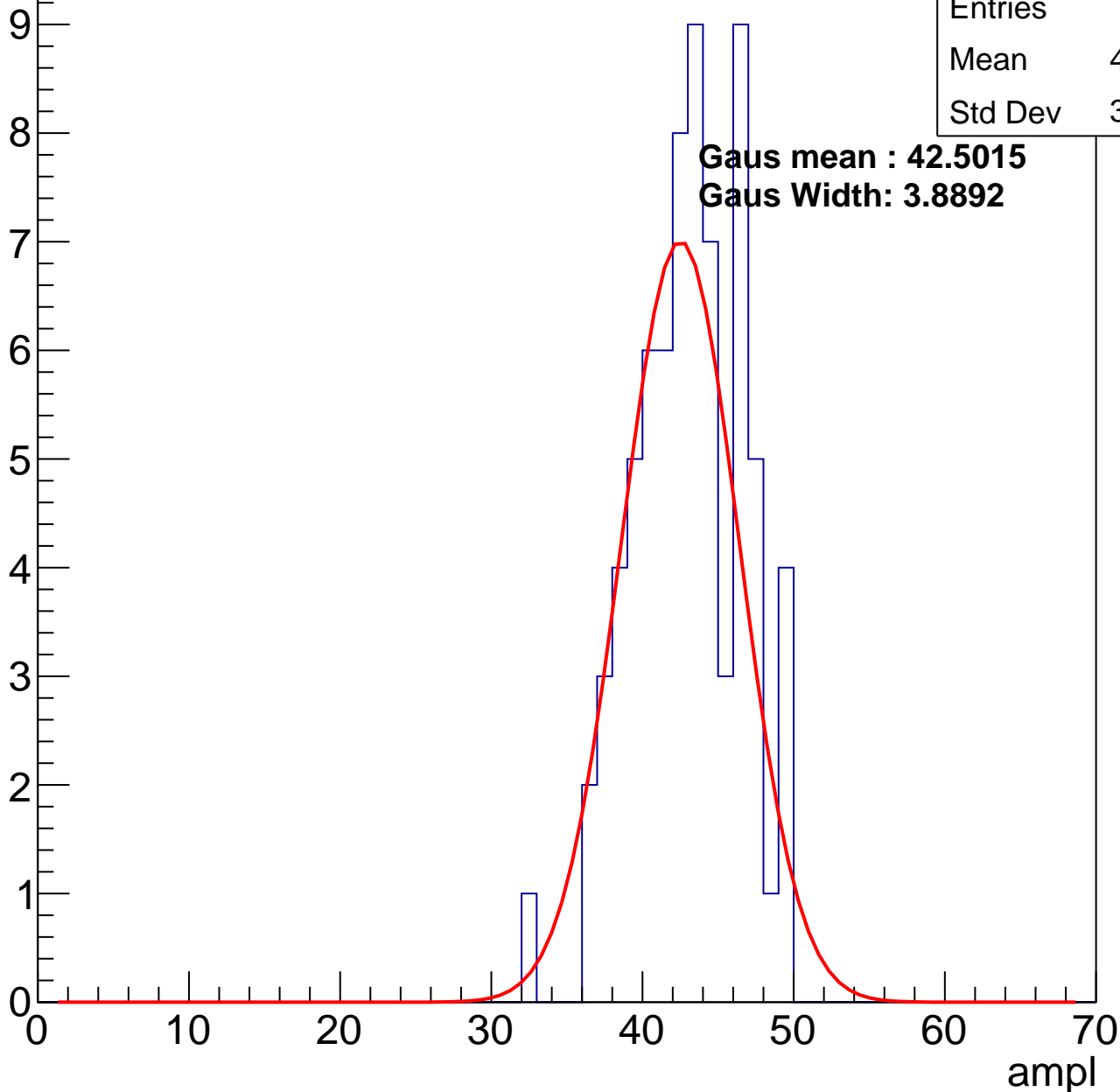
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	73
Mean	42.56
Std Dev	3.565

**Gaus mean : 42.5015**

**Gaus Width: 3.8892**

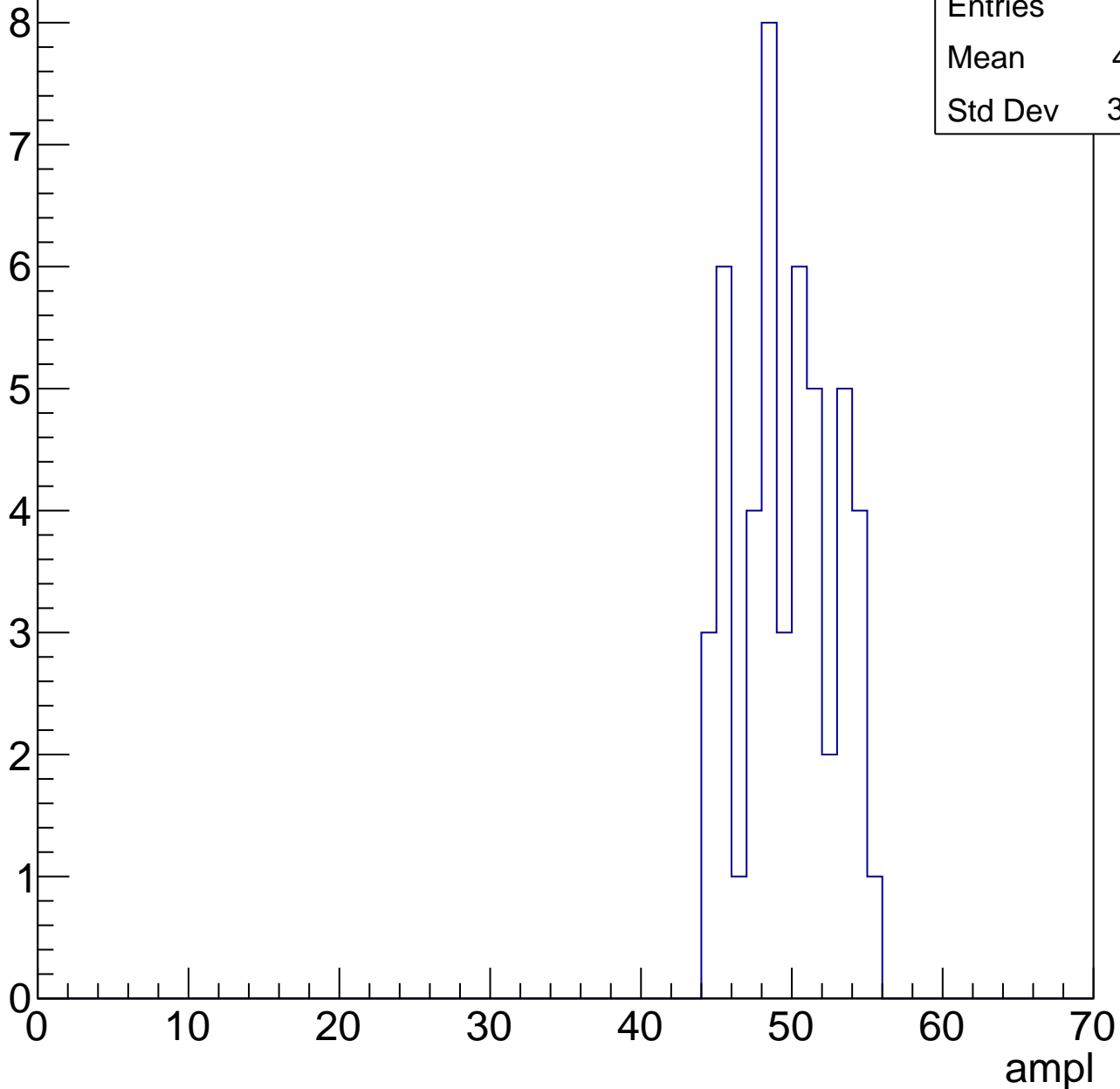


# B1L100S, U2-ch127, adc3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	48
Mean	49.21
Std Dev	3.102

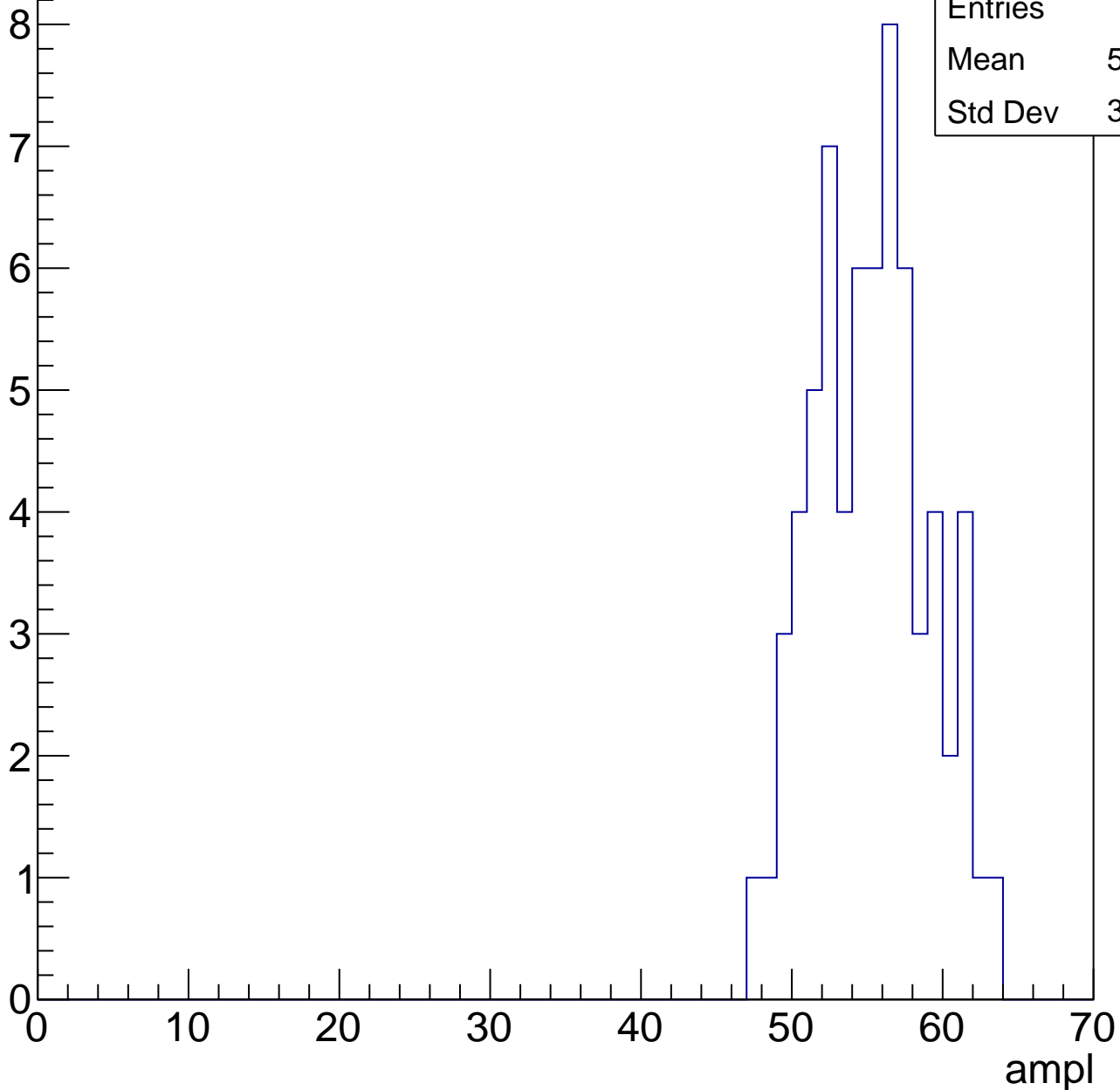


# B1L100S, U2-ch127, adc4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	66
Mean	54.79
Std Dev	3.719

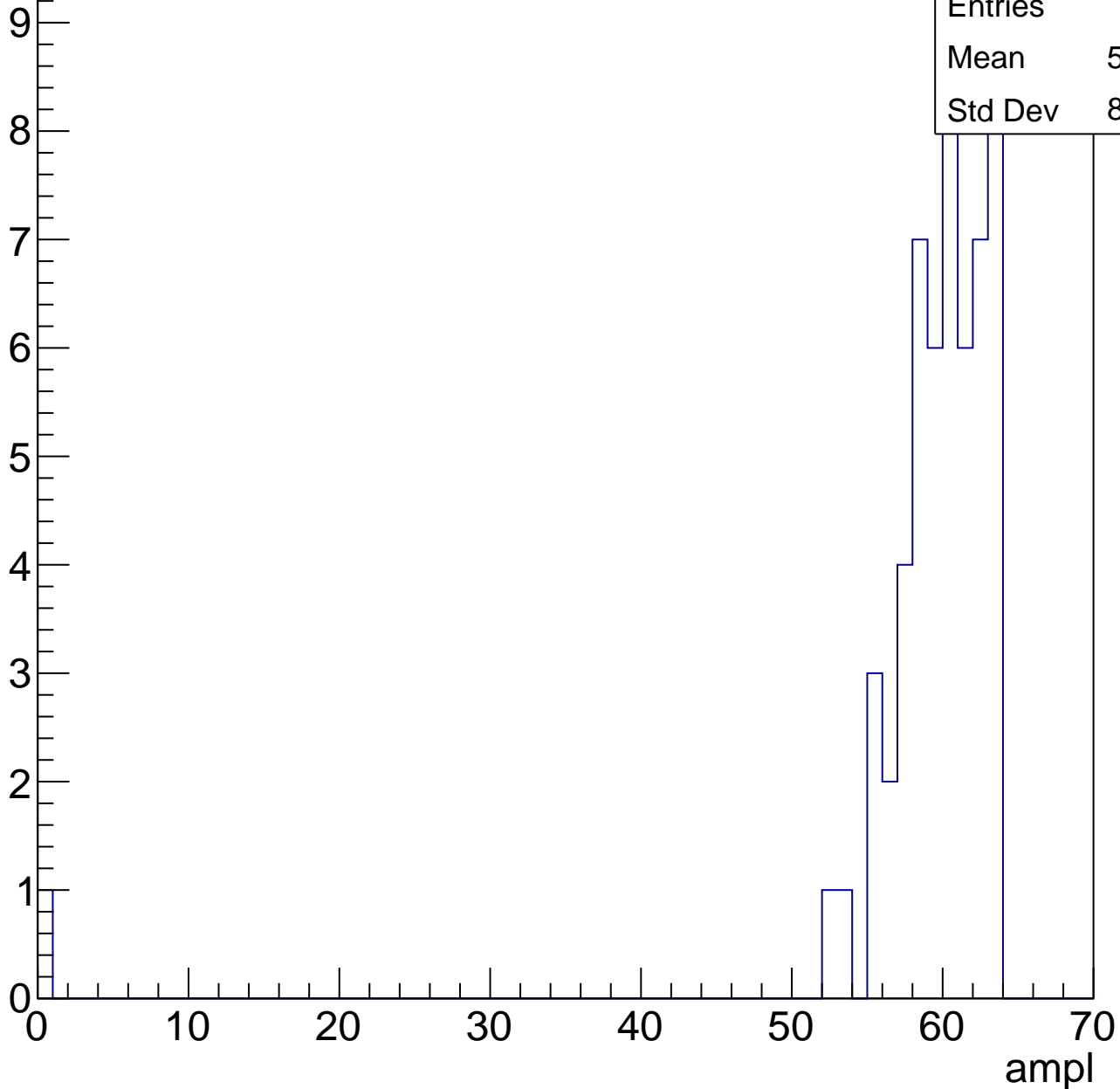


# B1L100S, U2-ch127, adc5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry

Entries	55
Mean	58.49
Std Dev	8.399



# B1L100S, U2-ch127, adc6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry





# B1L100S, U2-ch127, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



# B1L100S, U2-ch127, adc7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entry



Entries	1
Mean	0
Std Dev	0