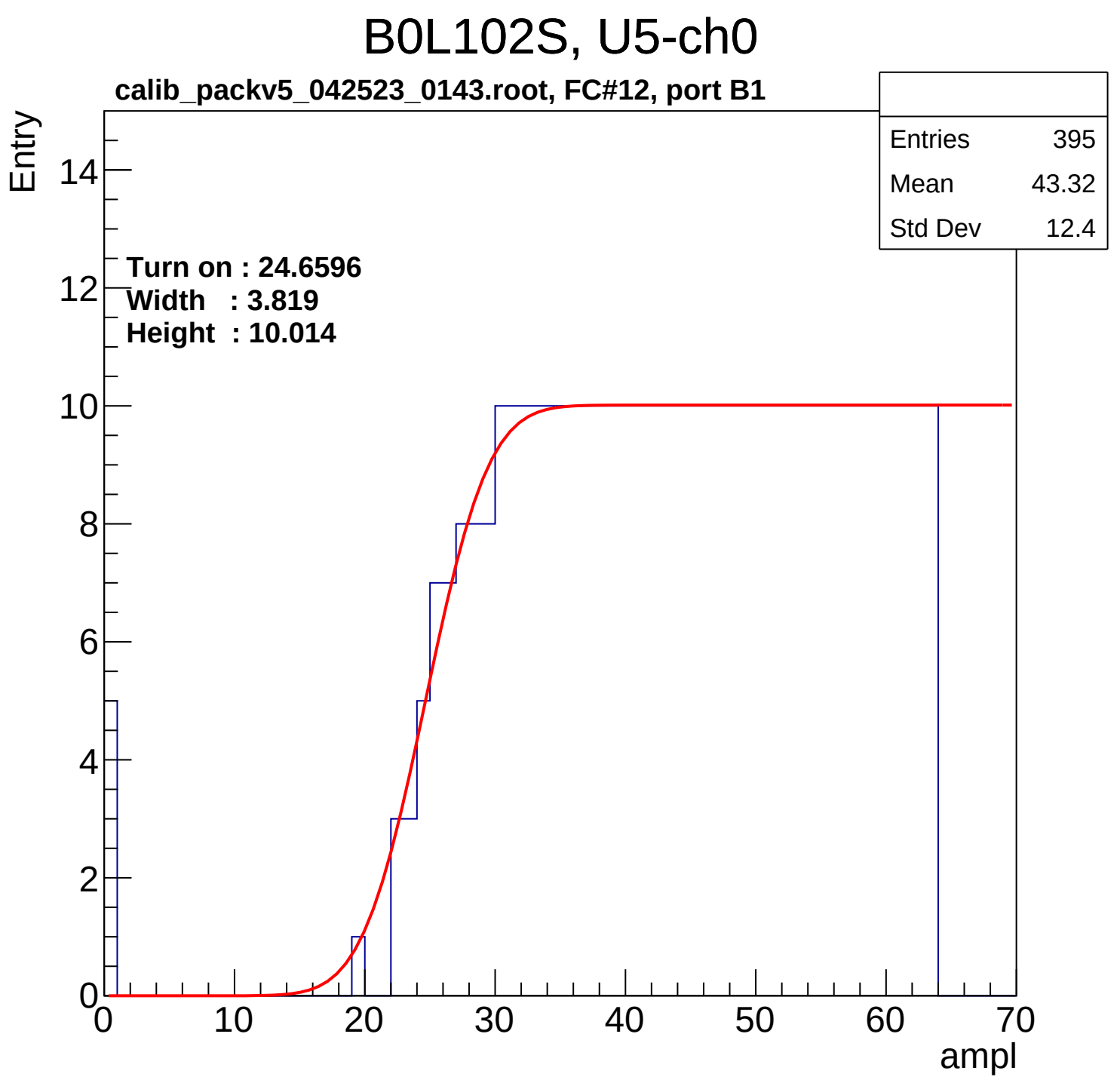
B0L102S, U5-ch0
calib_packv5_042523_0143.root, FC#12, port B1
Entries 395
Mean 43.32
Std Dev 12.4
Turn on : 24.6596
Width : 3.819
Height : 10.014
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ampl
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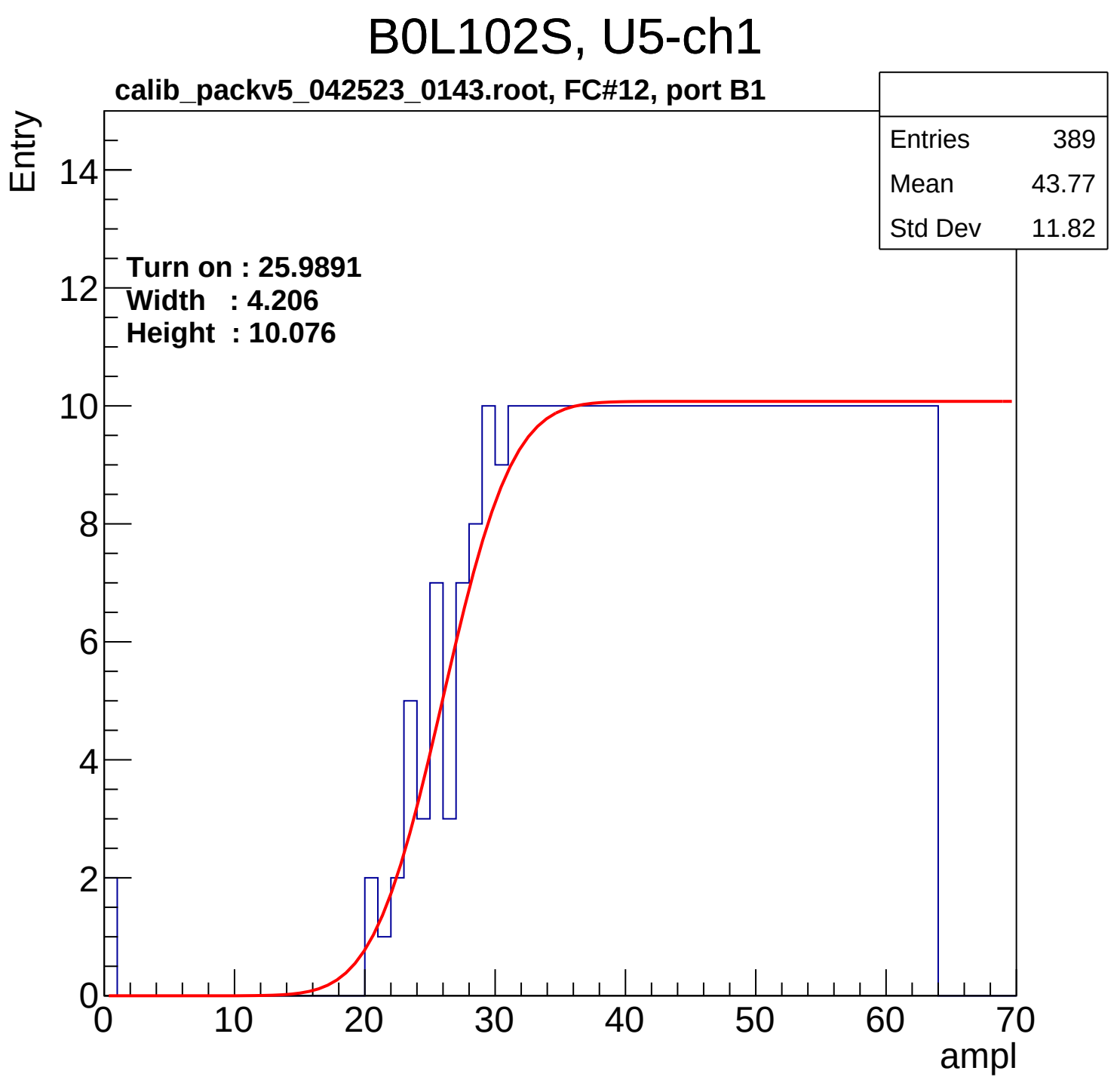
B0L102S, U5-ch1
calib_packv5_042523_0143.root, FC#12, port B1
Entries 389
Mean 43.77
Std Dev 11.82
Turn on : 25.9891
Width : 4.206
Height : 10.076
Entry
ampl
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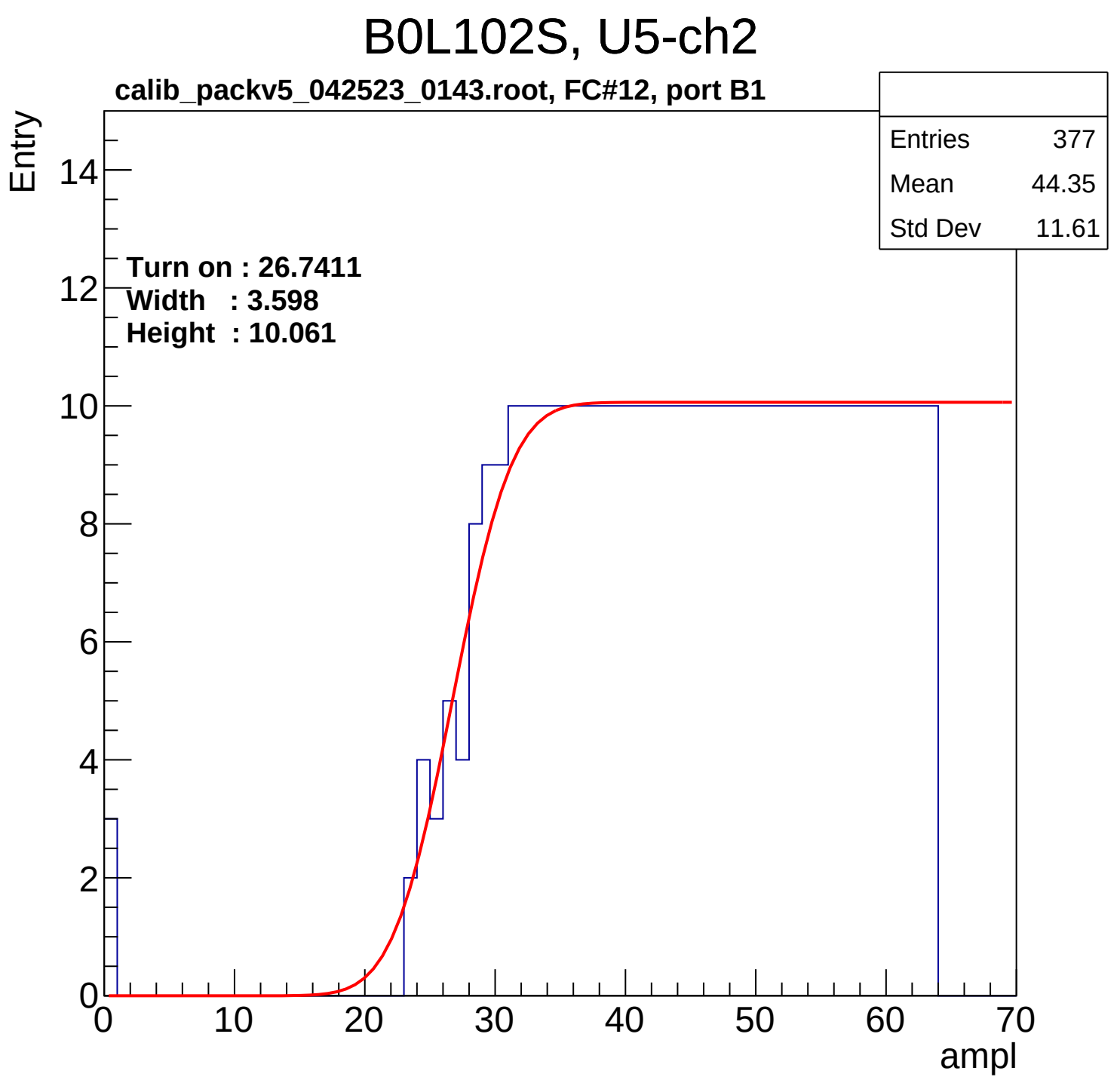
B0L102S, U5-ch2
calib_packv5_042523_0143.root, FC#12, port B1
Entries 377
Mean 44.35
Std Dev 11.61
Turn on : 26.7411
Width : 3.598
Height : 10.061
Entry
ampl
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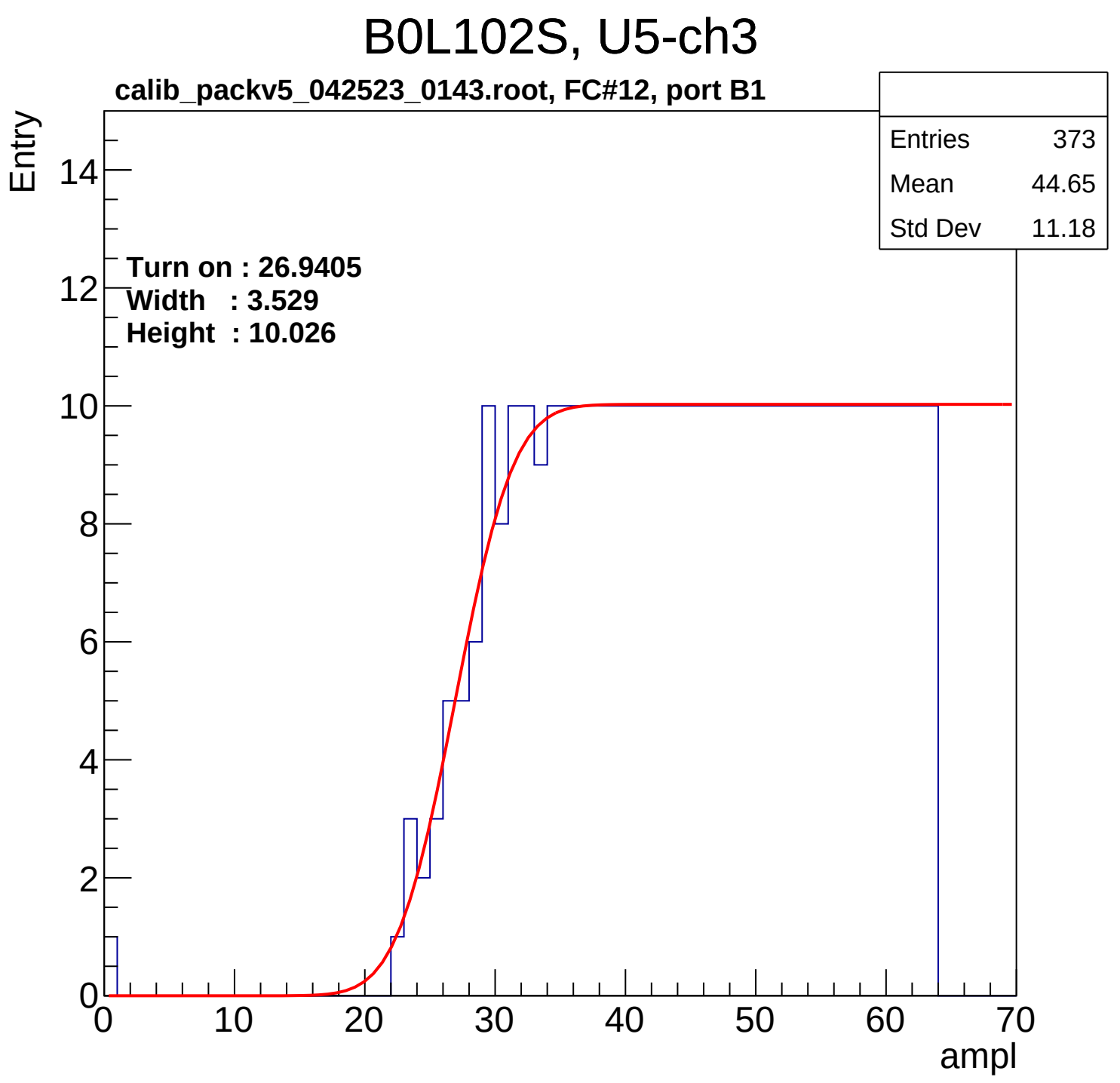
B0L102S, U5-ch3
calib_packv5_042523_0143.root, FC#12, port B1
Entries 373
Mean 44.65
Std Dev 11.18
Turn on : 26.9405
Width : 3.529
Height : 10.026
Entry
ampl
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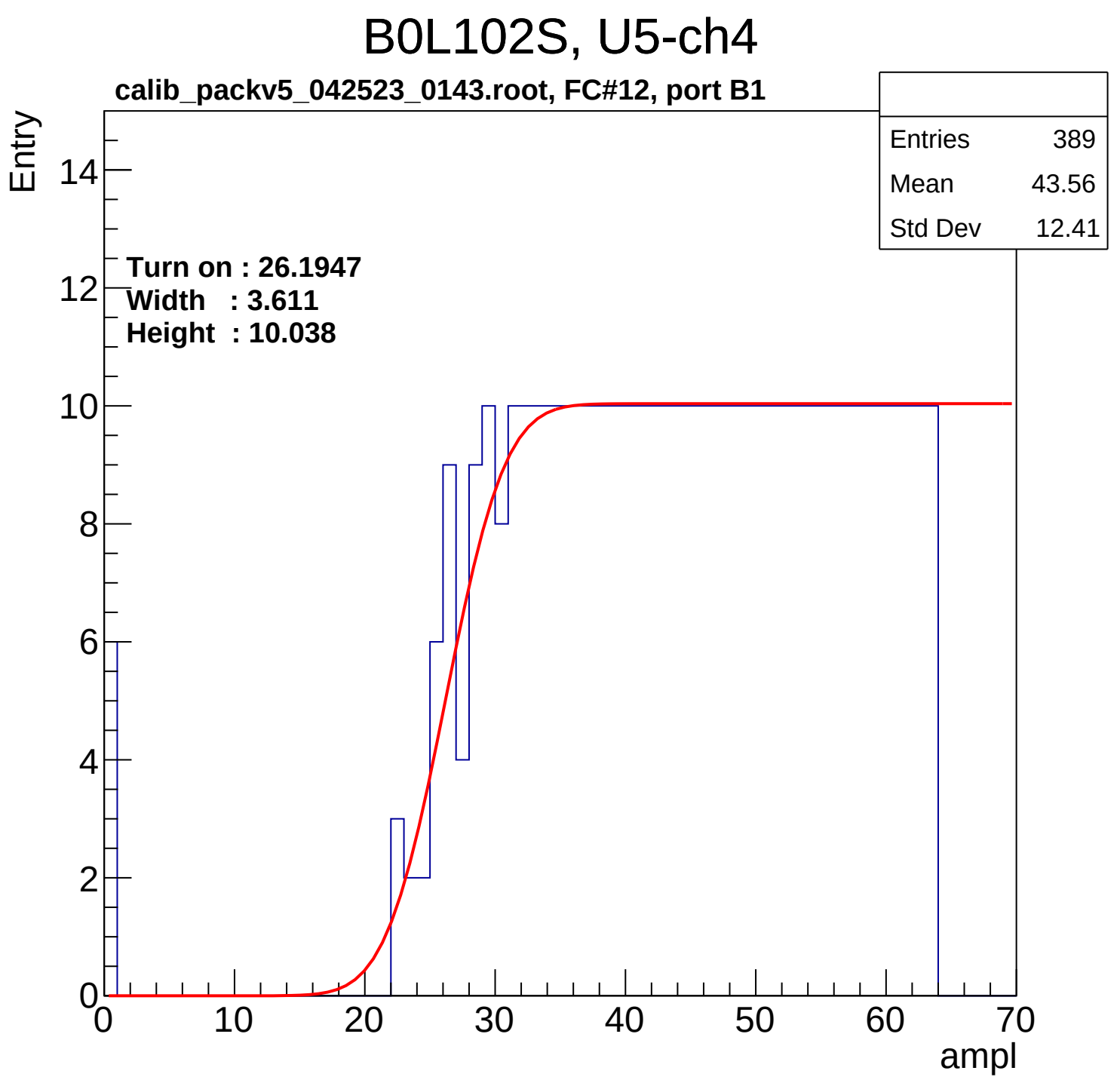
B0L102S, U5-ch4
calib_packv5_042523_0143.root, FC#12, port B1
Entries 389
Mean 43.56
Std Dev 12.41
Turn on : 26.1947
Width : 3.611
Height : 10.038
Entry
ampl
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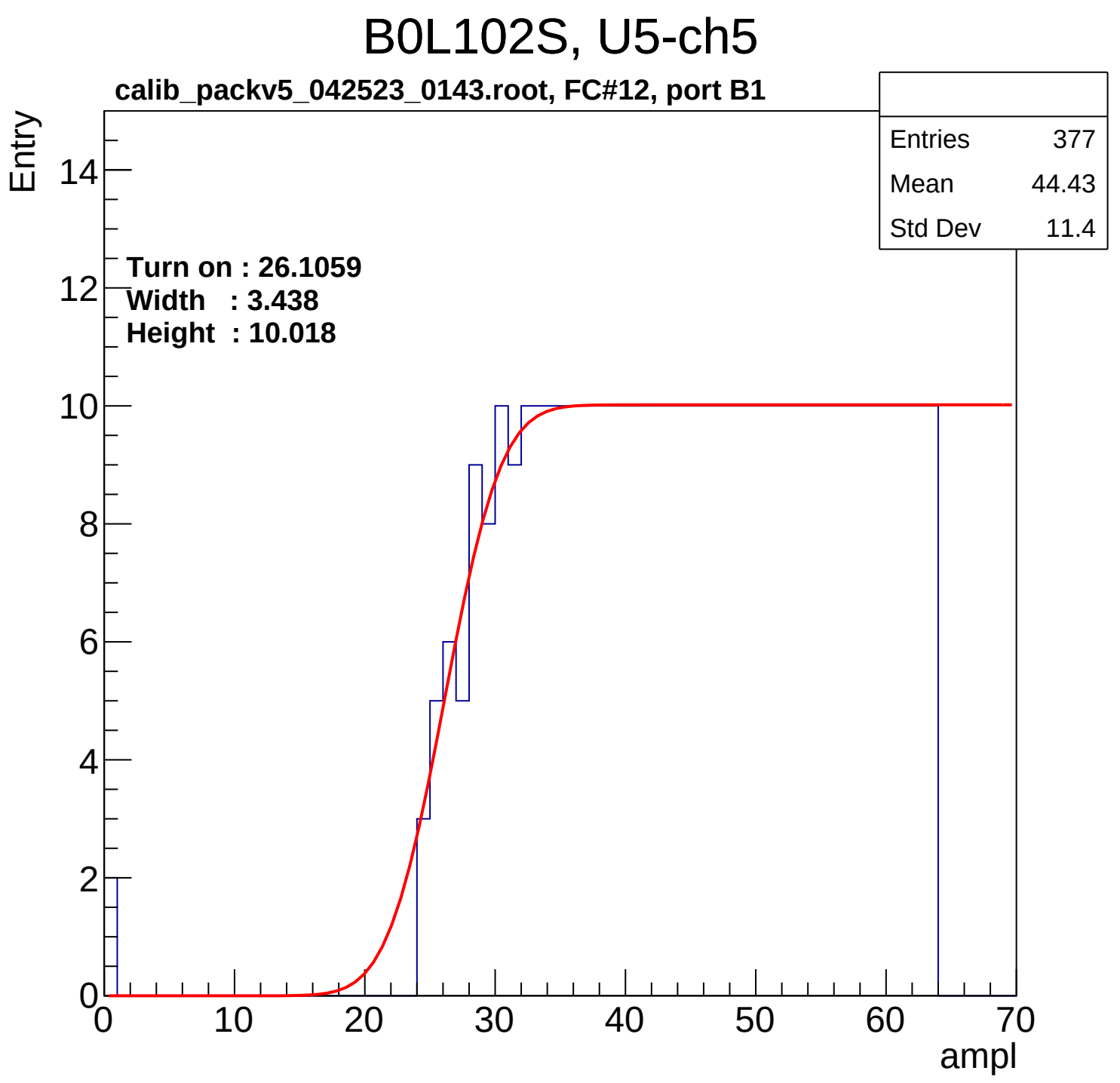
B0L102S, U5-ch5
calib_packv5_042523_0143.root, FC#12, port B1
Entries 377
Mean 44.43
Std Dev 11.4
Turn on : 26.1059
Width : 3.438
Height : 10.018
Entry
ampl
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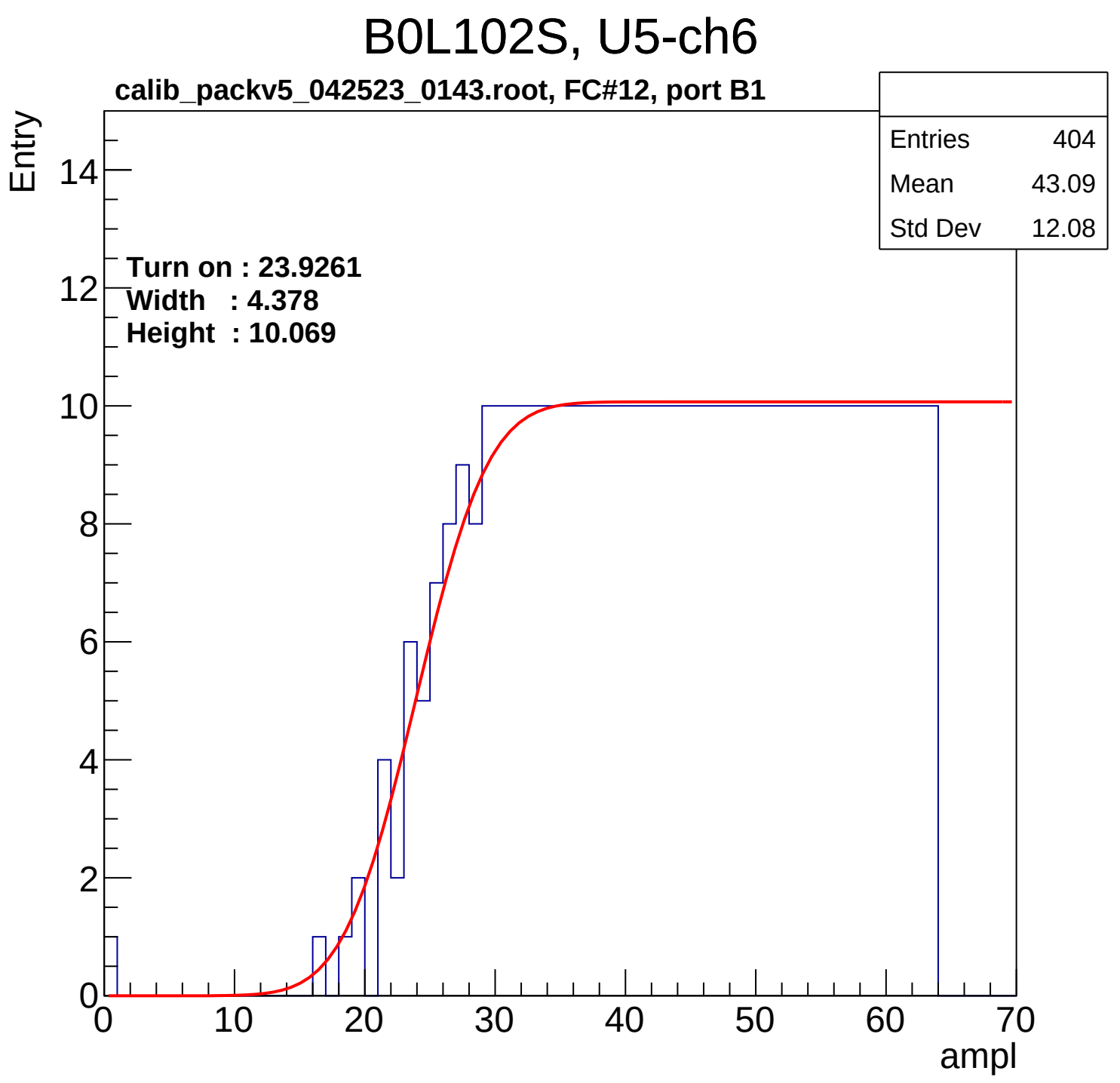
B0L102S, U5-ch6
calib_packv5_042523_0143.root, FC#12, port B1
Entries 404
Mean 43.09
Std Dev 12.08
Turn on : 23.9261
Width : 4.378
Height : 10.069
Entry
ampl
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6
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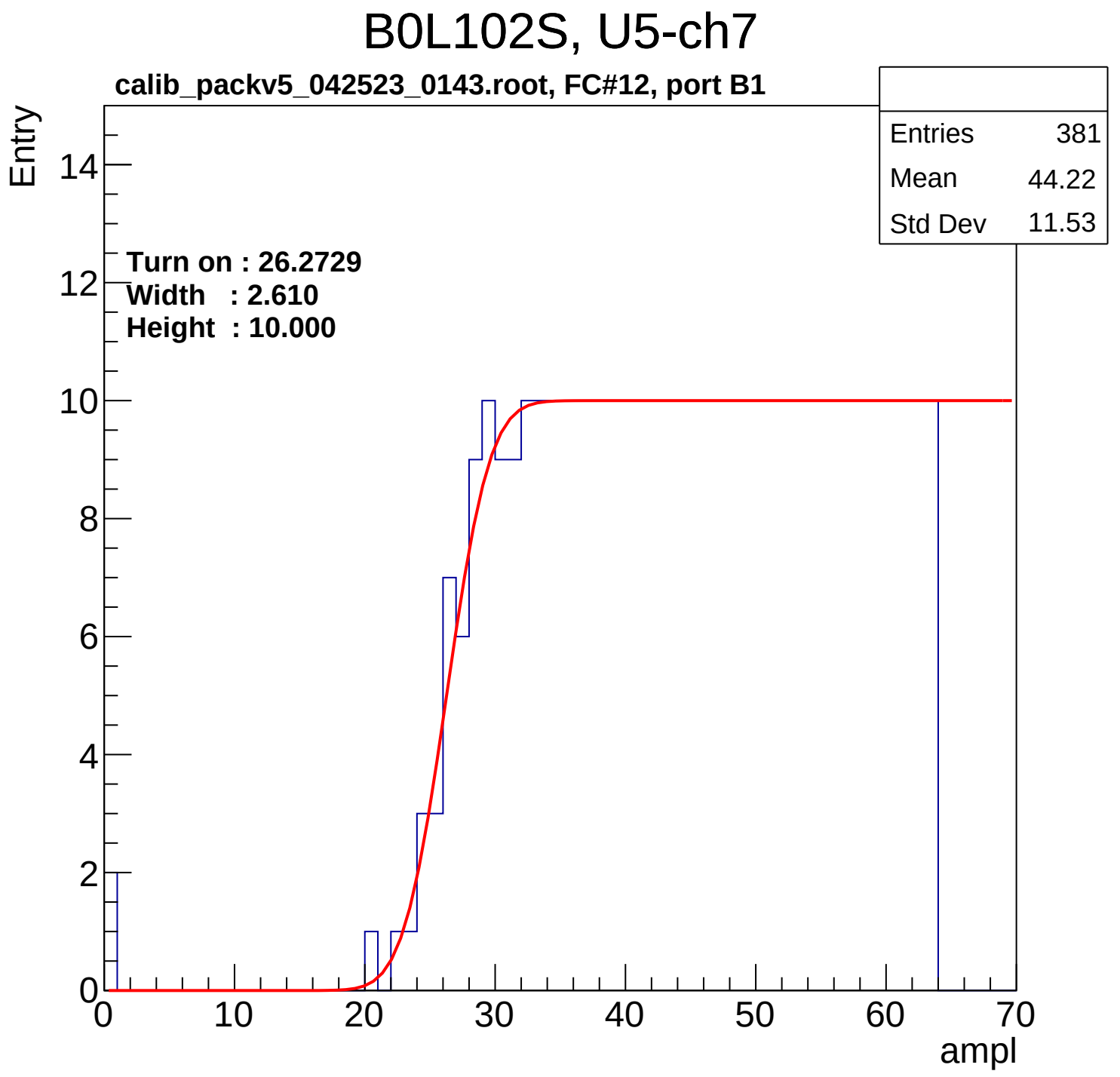
B0L102S, U5-ch7
calib_packv5_042523_0143.root, FC#12, port B1
Entries 381
Mean 44.22
Std Dev 11.53
Turn on : 26.2729
Width : 2.610
Height : 10.000
Entry
ampl
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4
6
8
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0
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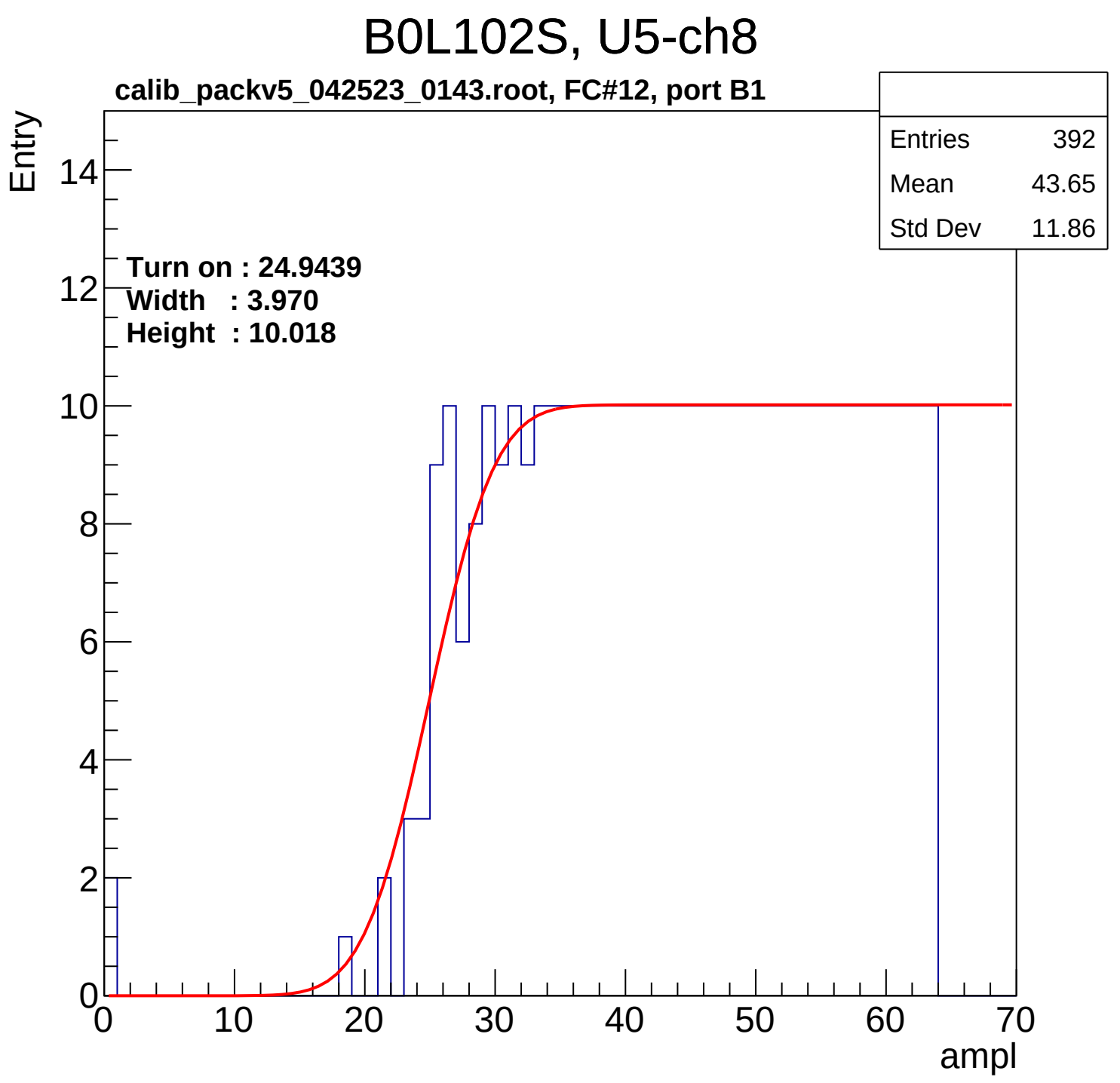
B0L102S, U5-ch8
calib_packv5_042523_0143.root, FC#12, port B1
Entries 392
Mean 43.65
Std Dev 11.86
Turn on : 24.9439
Width : 3.970
Height : 10.018
Entry
ampl
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8
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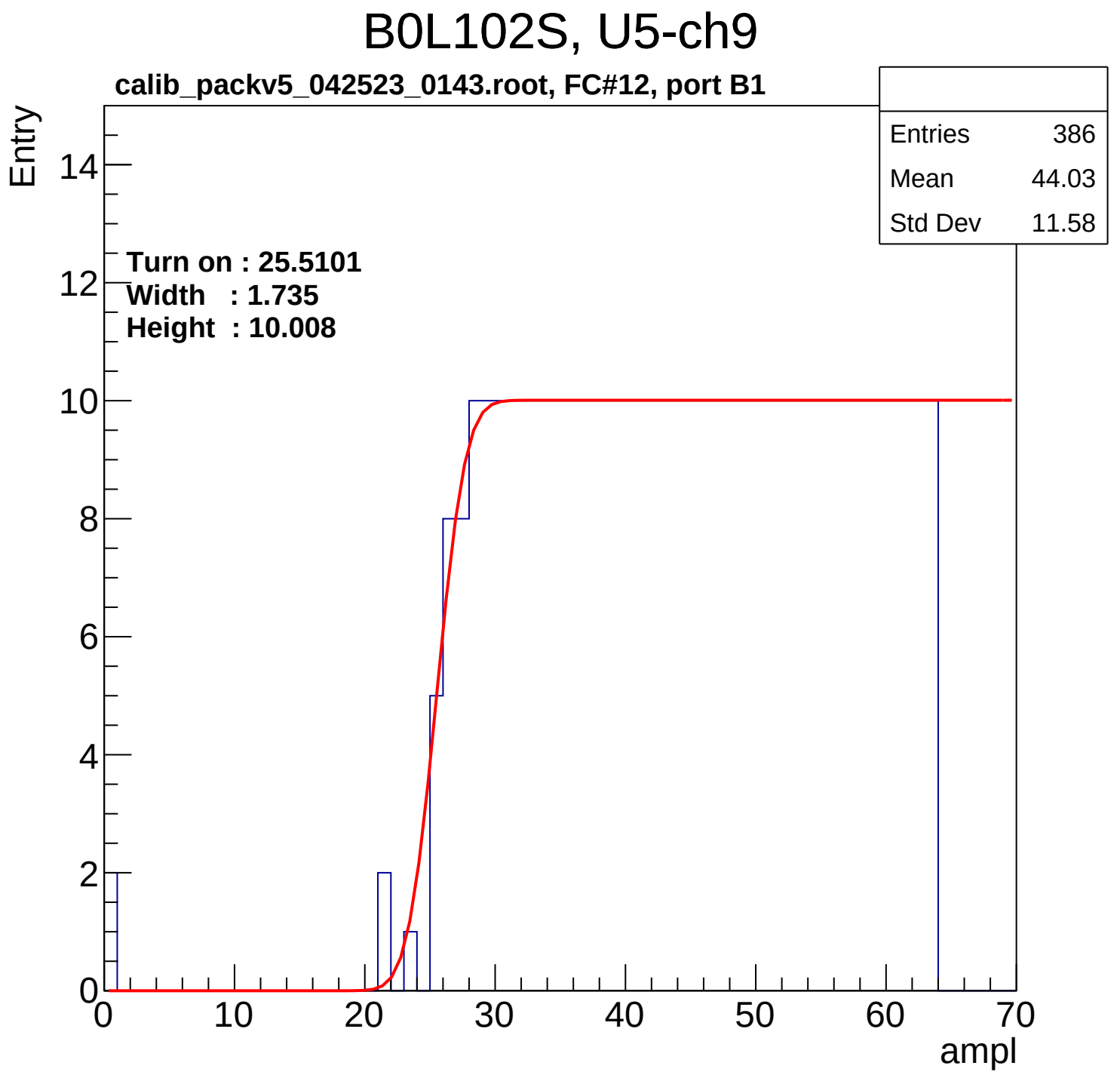
B0L102S, U5-ch9
calib_packv5_042523_0143.root, FC#12, port B1
Entries 386
Mean 44.03
Std Dev 11.58
Turn on : 25.5101
Width : 1.735
Height : 10.008
Entry
ampl
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4
6
8
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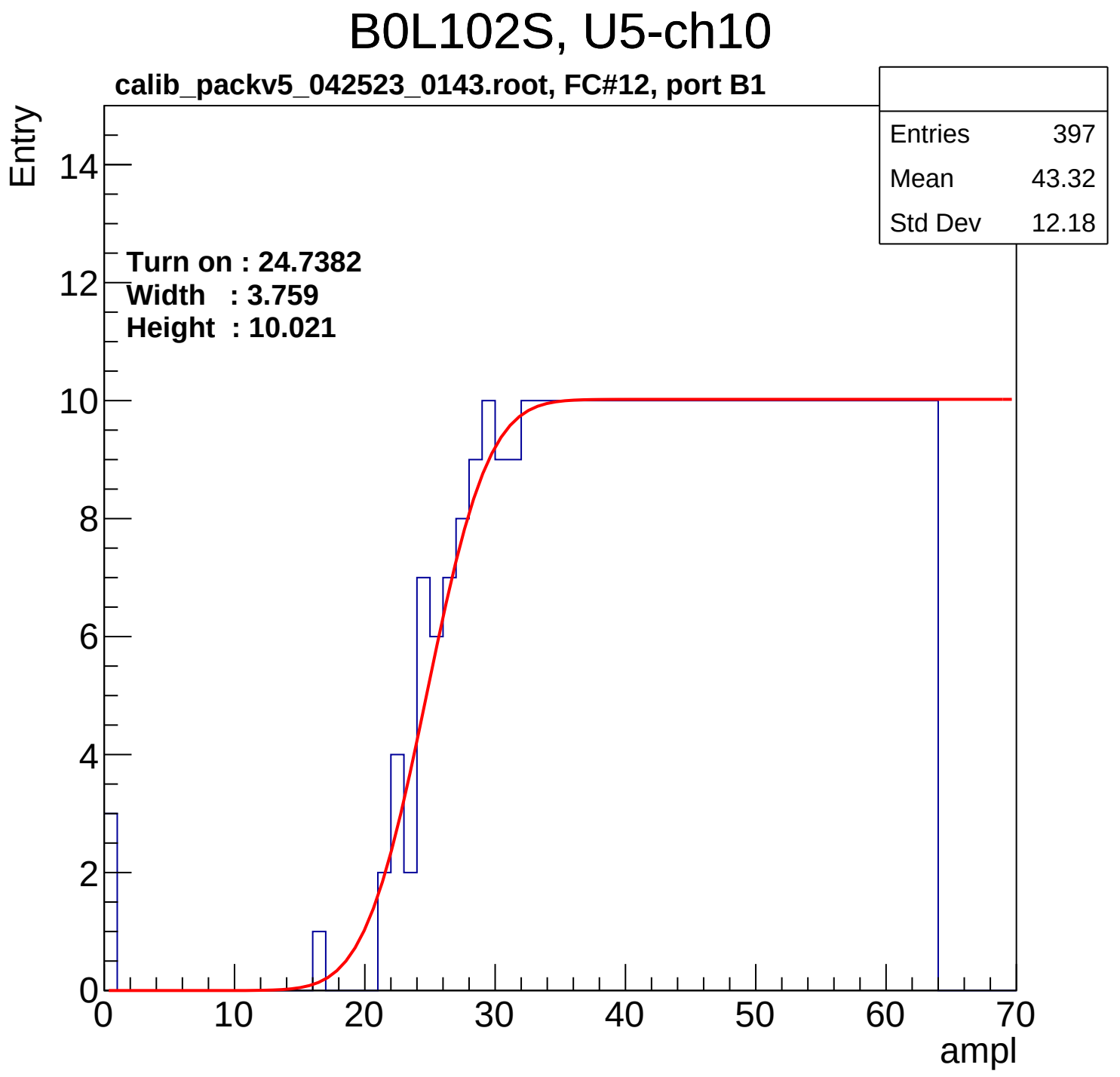
B0L102S, U5-ch10
calib_packv5_042523_0143.root, FC#12, port B1
Entries 397
Mean 43.32
Std Dev 12.18
Turn on : 24.7382
Width : 3.759
Height : 10.021
Entry
ampl
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6
8
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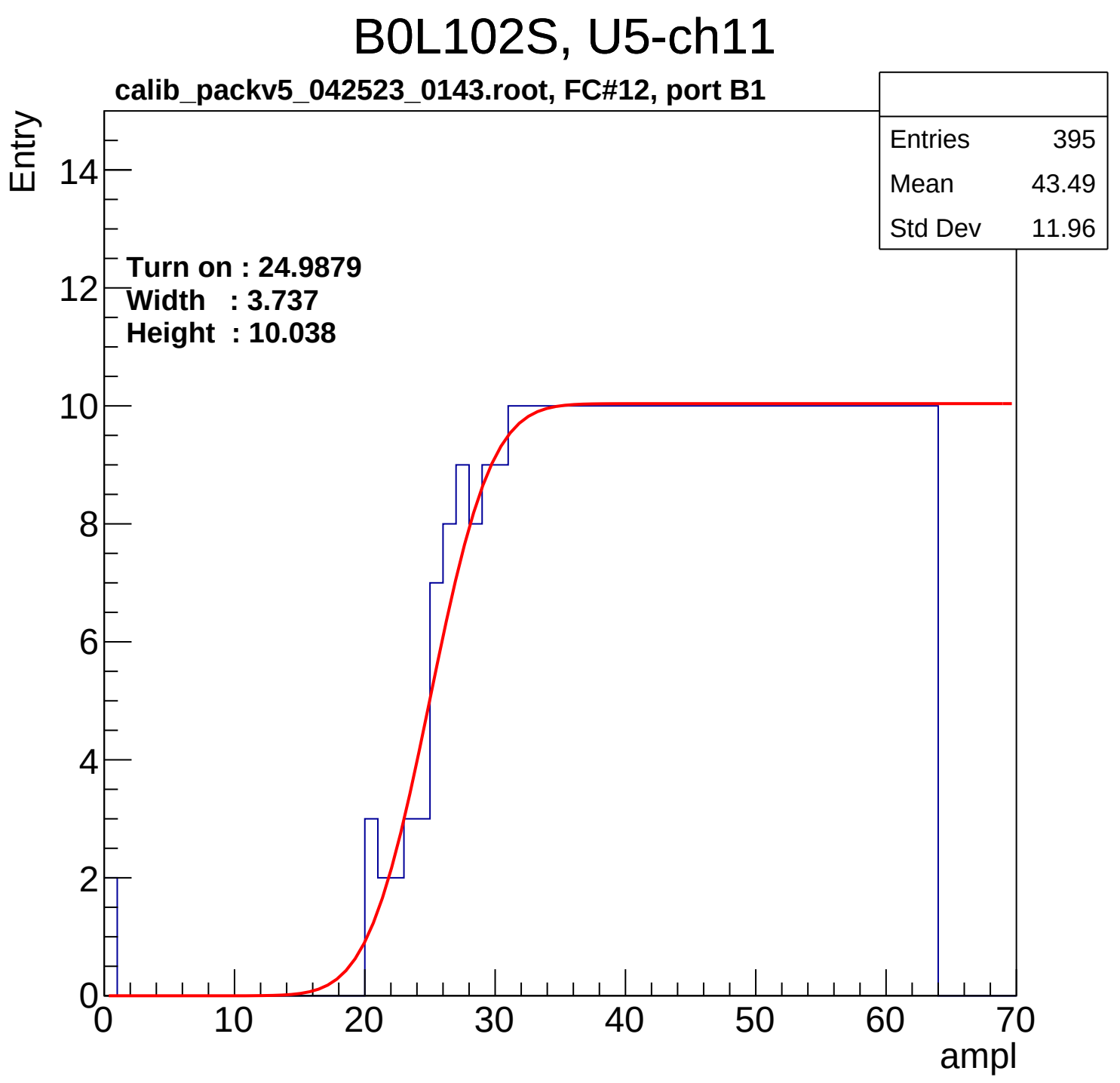
B0L102S, U5-ch11
calib_packv5_042523_0143.root, FC#12, port B1
Entries 395
Mean 43.49
Std Dev 11.96
Turn on : 24.9879
Width : 3.737
Height : 10.038
Entry
ampl
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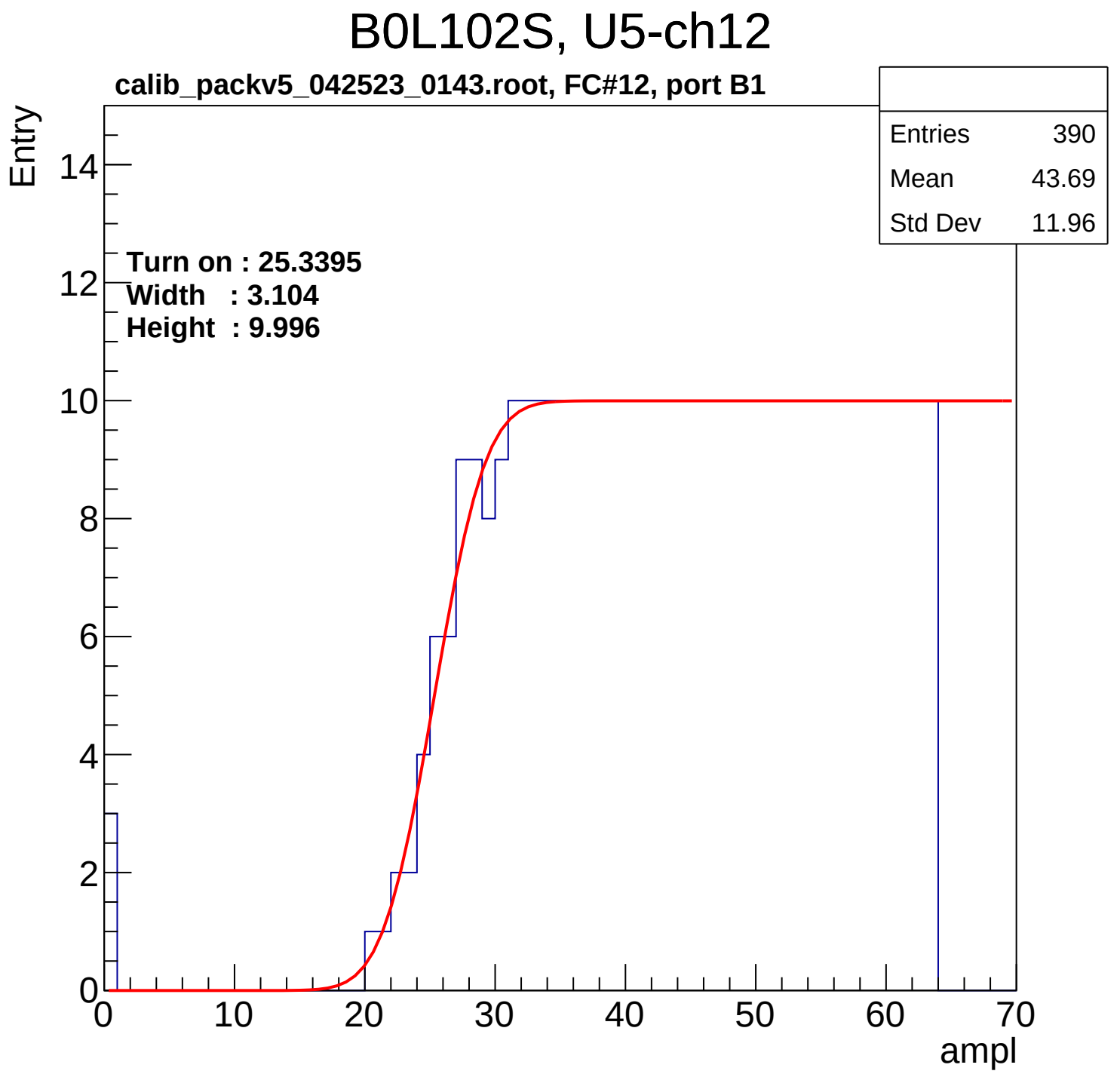
B0L102S, U5-ch12
calib_packv5_042523_0143.root, FC#12, port B1
Entries 390
Mean 43.69
Std Dev 11.96
Turn on : 25.3395
Width : 3.104
Height : 9.996
Entry
ampl
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6
8
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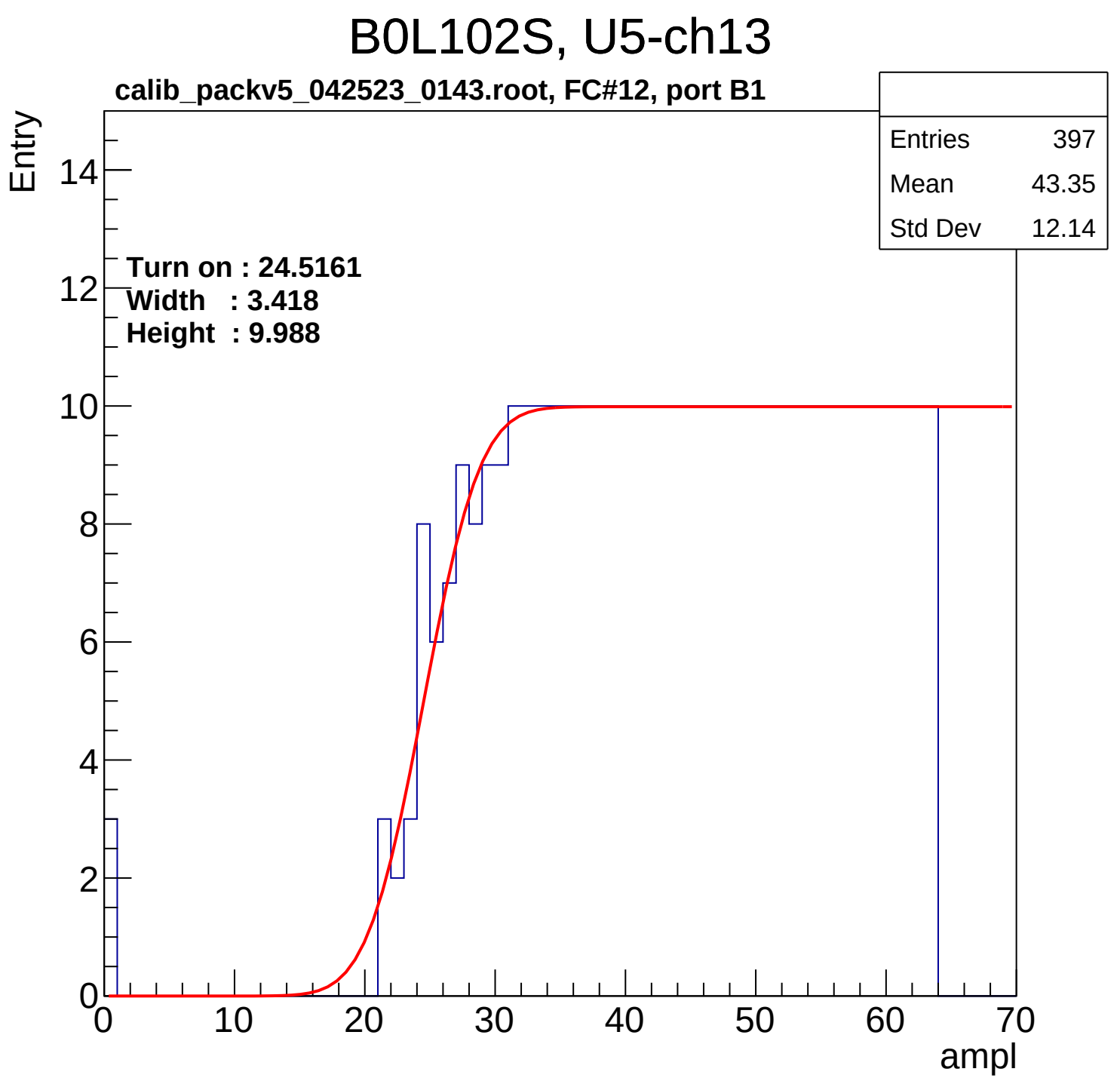
B0L102S, U5-ch13
calib_packv5_042523_0143.root, FC#12, port B1
Entries 397
Mean 43.35
Std Dev 12.14
Turn on : 24.5161
Width : 3.418
Height : 9.988
Entry
ampl
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6
8
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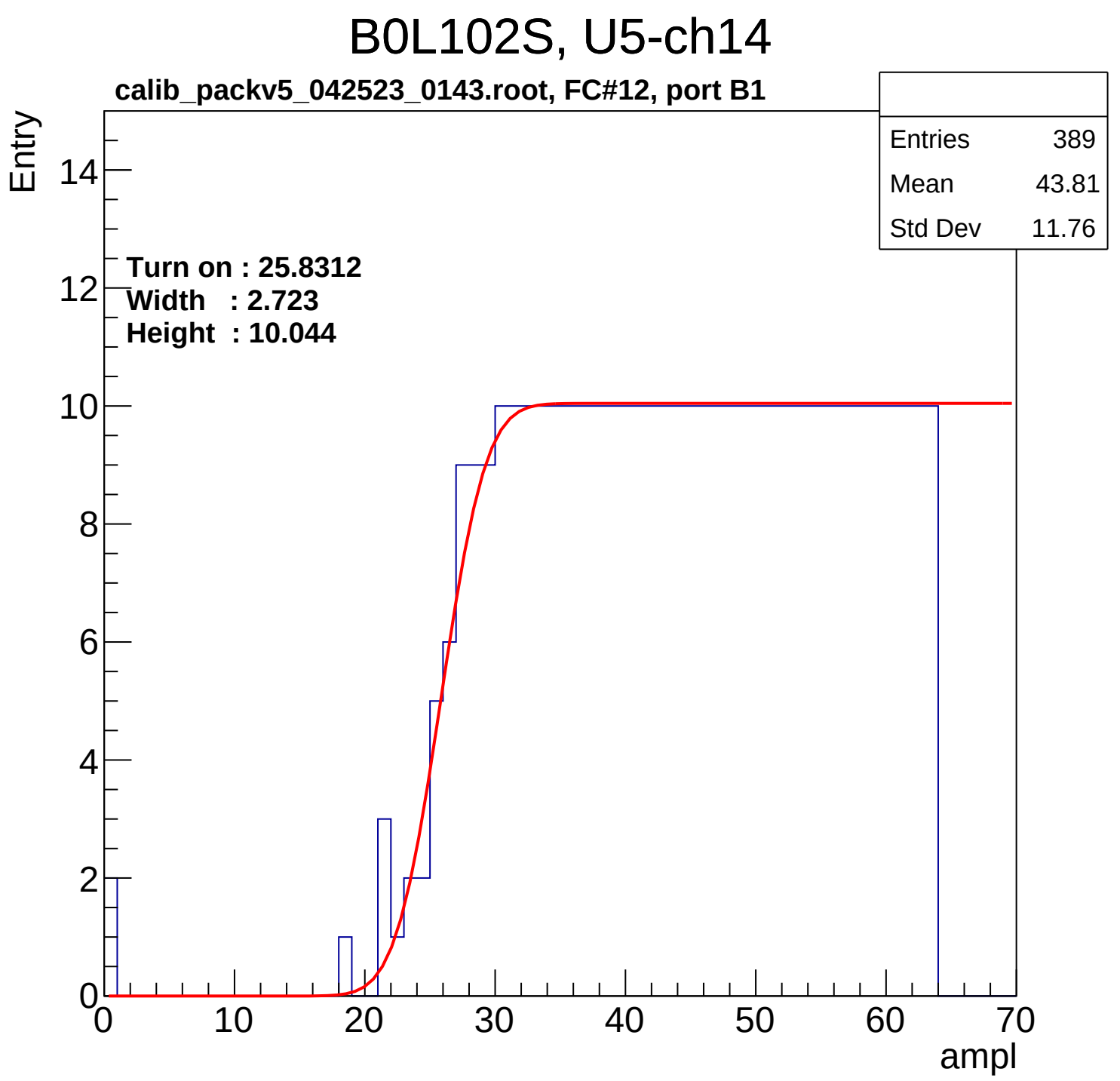
B0L102S, U5-ch14
calib_packv5_042523_0143.root, FC#12, port B1
Entries 389
Mean 43.81
Std Dev 11.76
Turn on : 25.8312
Width : 2.723
Height : 10.044
Entry
ampl
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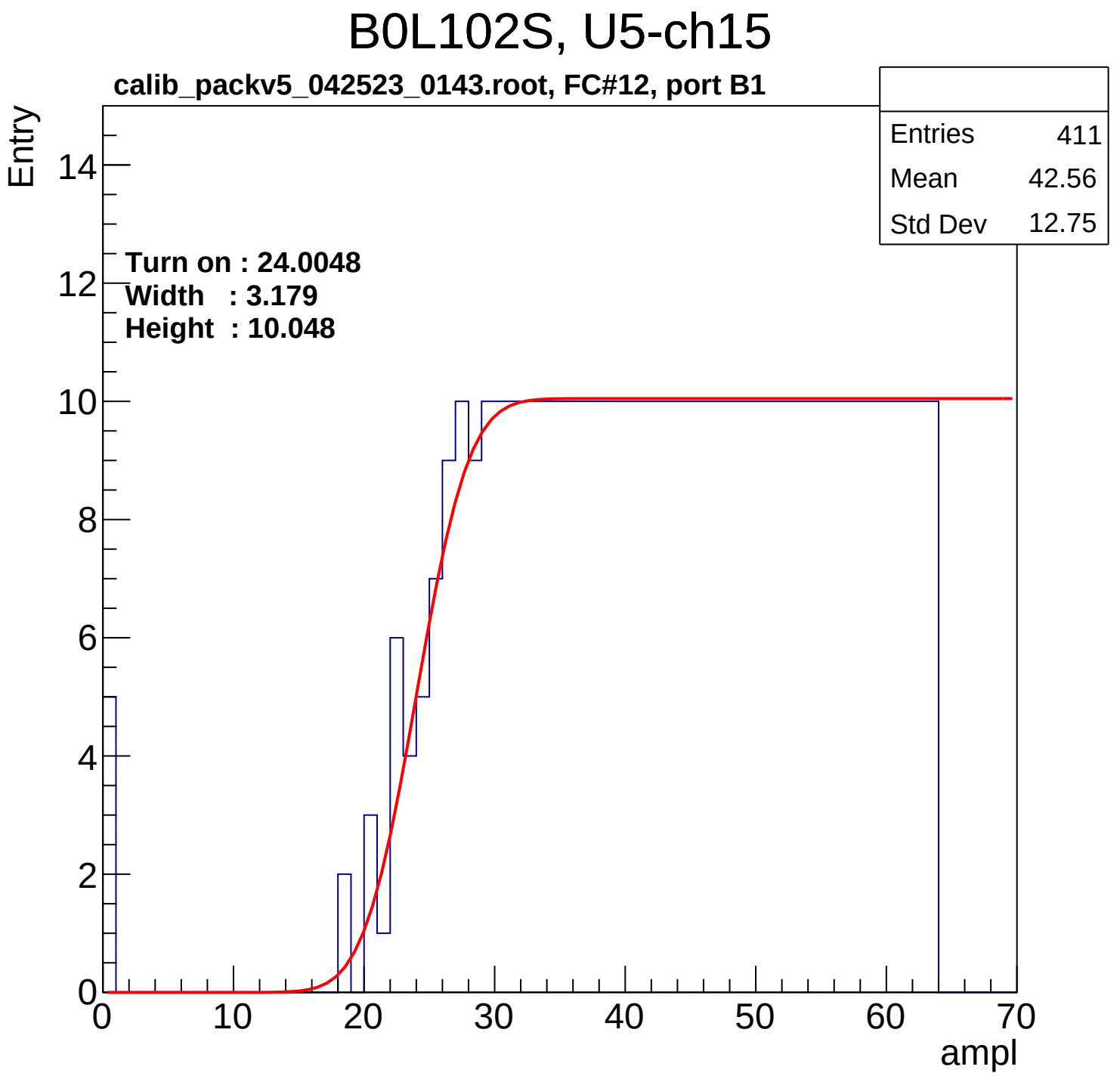
B0L102S, U5-ch15
calib_packv5_042523_0143.root, FC#12, port B1
Entries 411
Mean 42.56
Std Dev 12.75
Turn on : 24.0048
Width : 3.179
Height : 10.048
Entry
ampl
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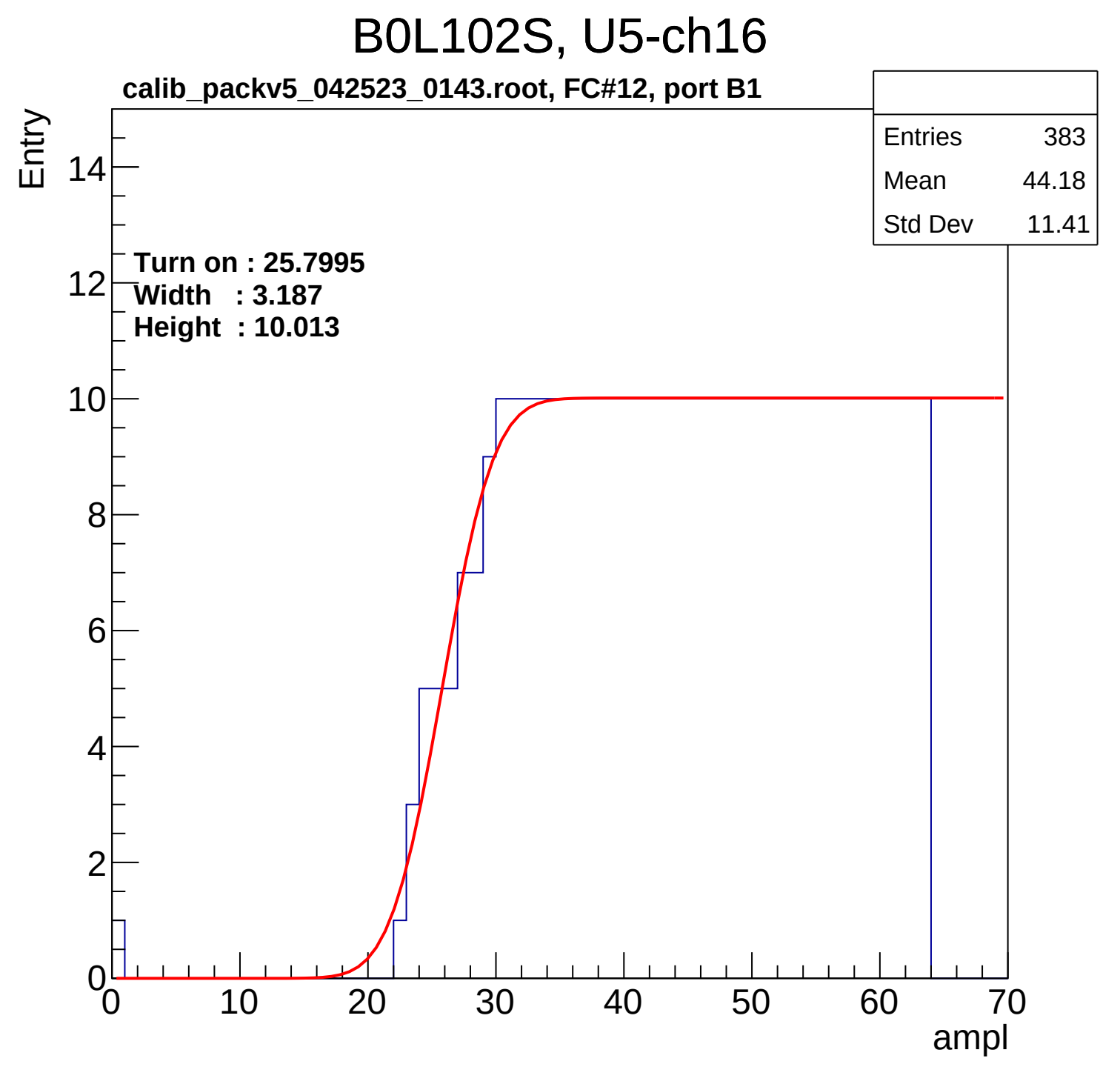
B0L102S, U5-ch16
calib_packv5_042523_0143.root, FC#12, port B1
Entries 383
Mean 44.18
Std Dev 11.41
Turn on : 25.7995
Width : 3.187
Height : 10.013
Entry
ampl
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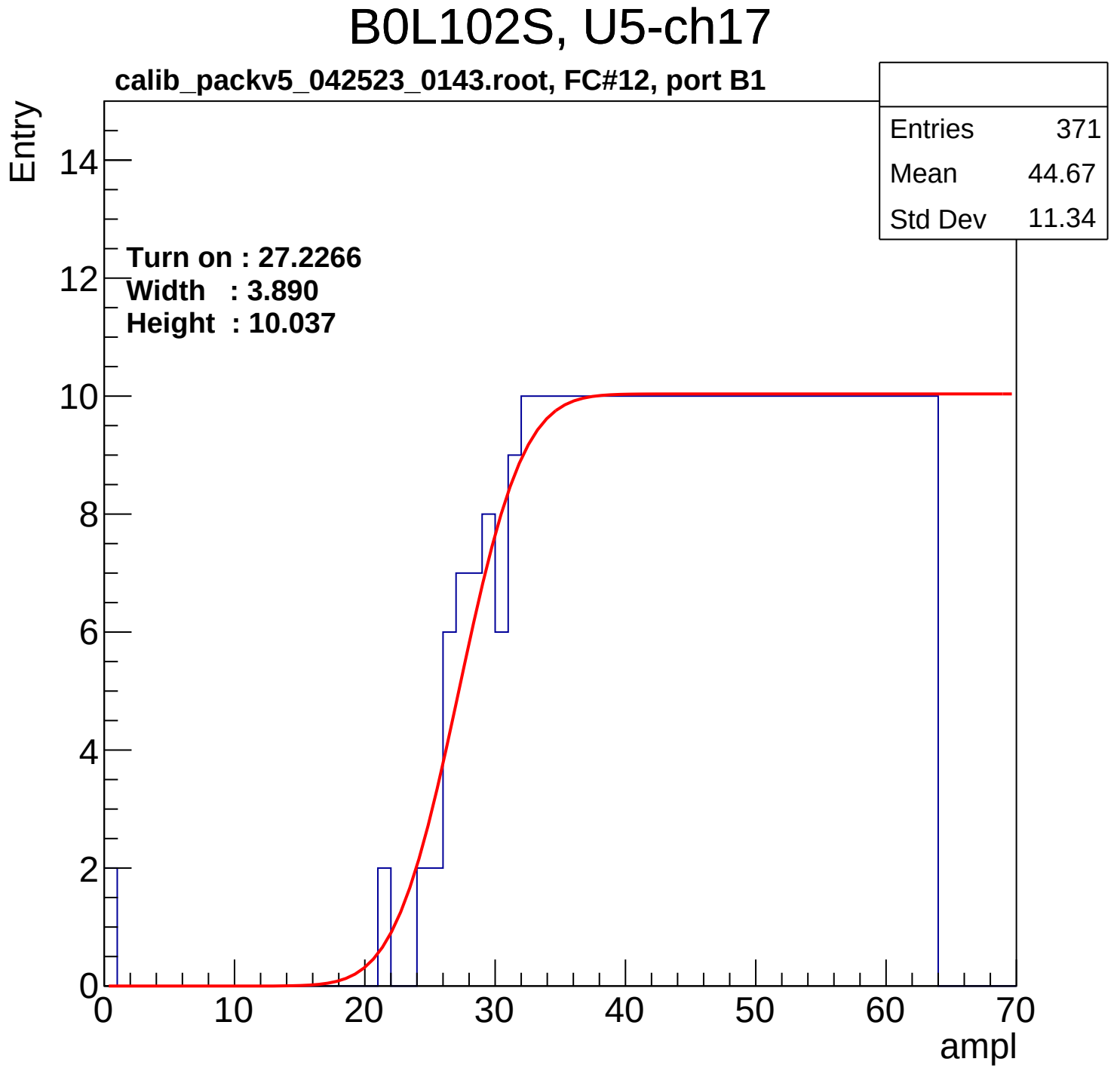
B0L102S, U5-ch17
calib_packv5_042523_0143.root, FC#12, port B1
Entries 371
Mean 44.67
Std Dev 11.34
Turn on : 27.2266
Width : 3.890
Height : 10.037
Entry
ampl
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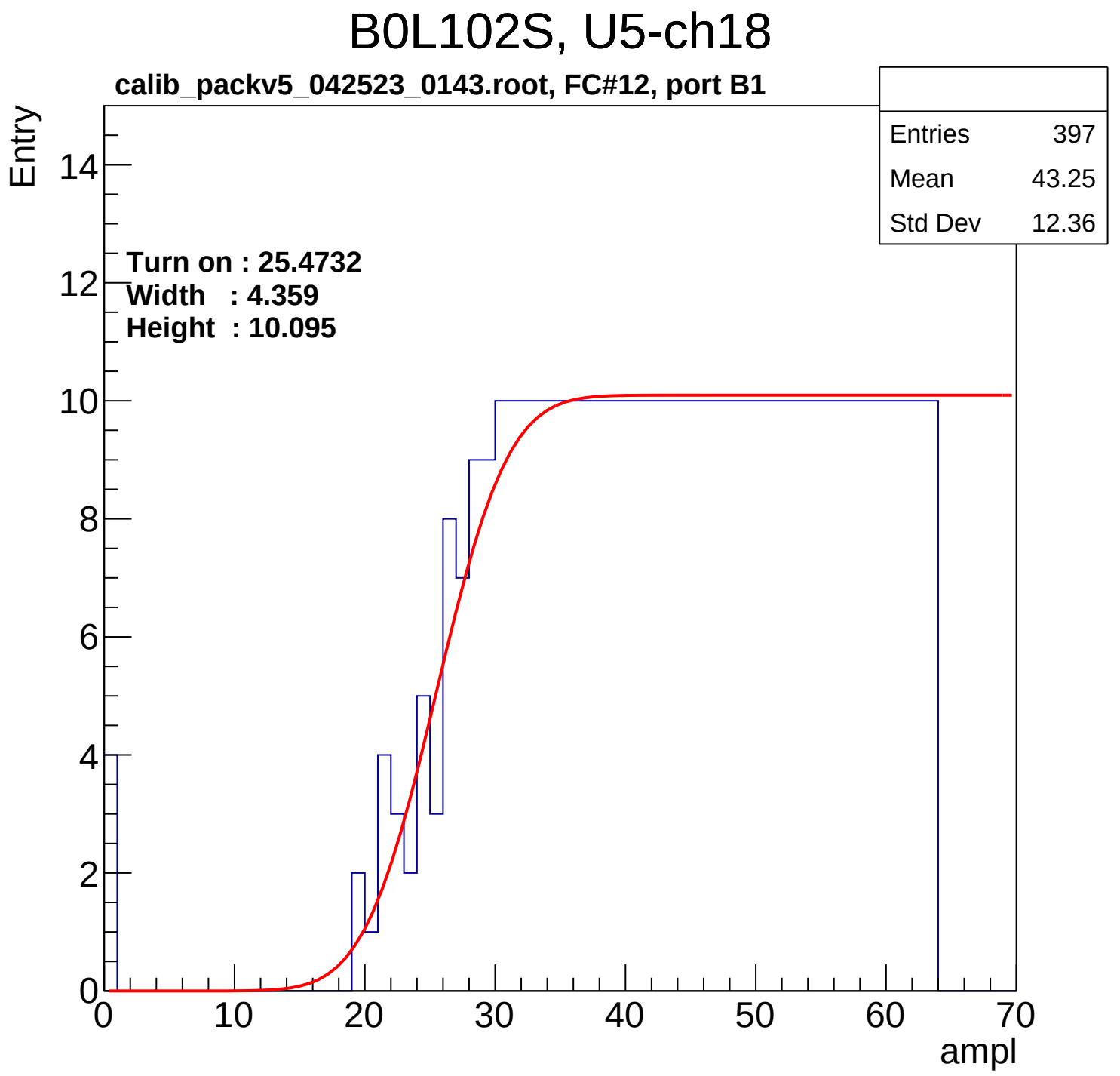
B0L102S, U5-ch18
calib_packv5_042523_0143.root, FC#12, port B1
Entries 397
Mean 43.25
Std Dev 12.36
Turn on : 25.4732
Width : 4.359
Height : 10.095
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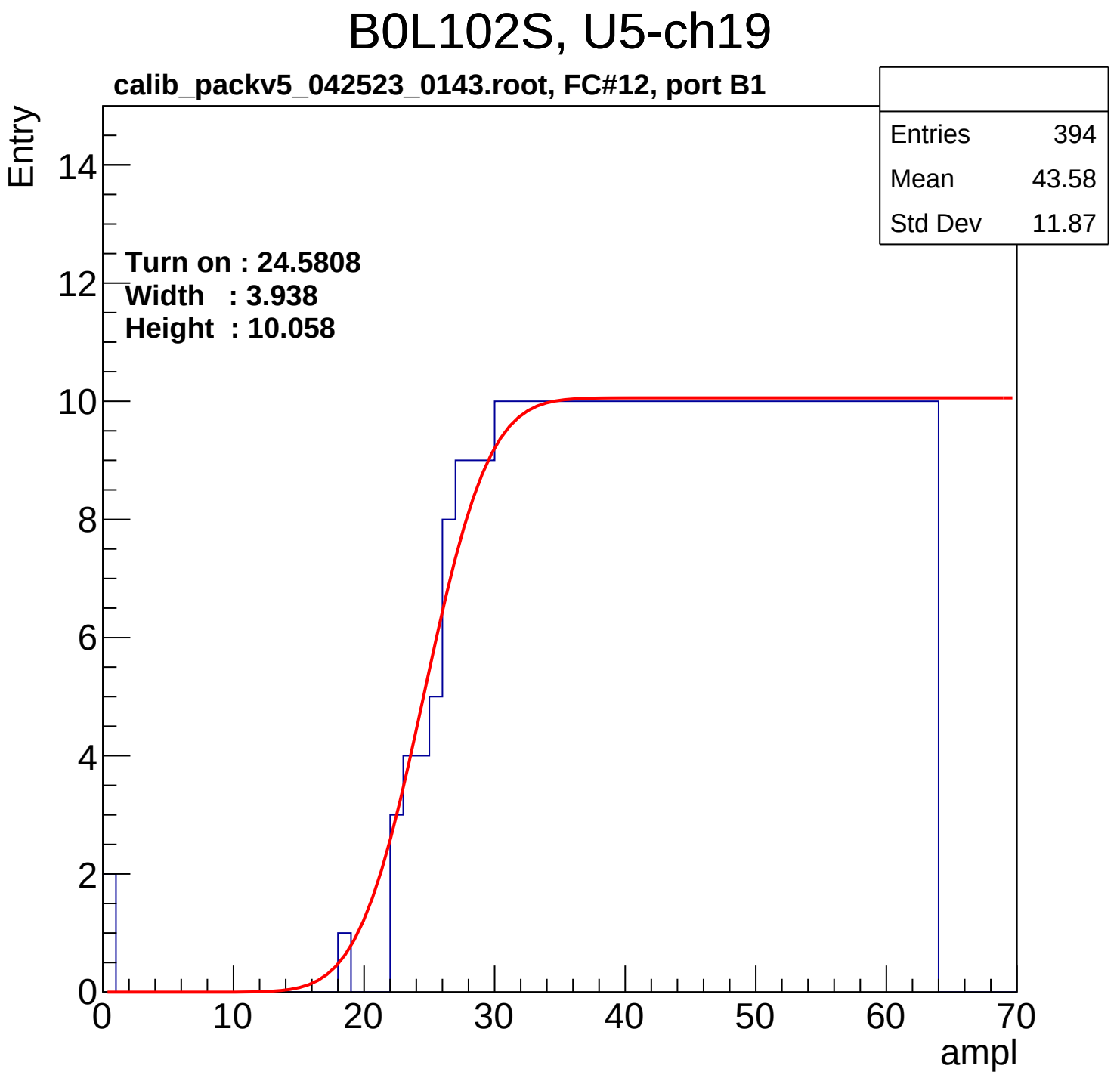
B0L102S, U5-ch19
calib_packv5_042523_0143.root, FC#12, port B1
Entries 394
Mean 43.58
Std Dev 11.87
Turn on : 24.5808
Width : 3.938
Height : 10.058
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ampl
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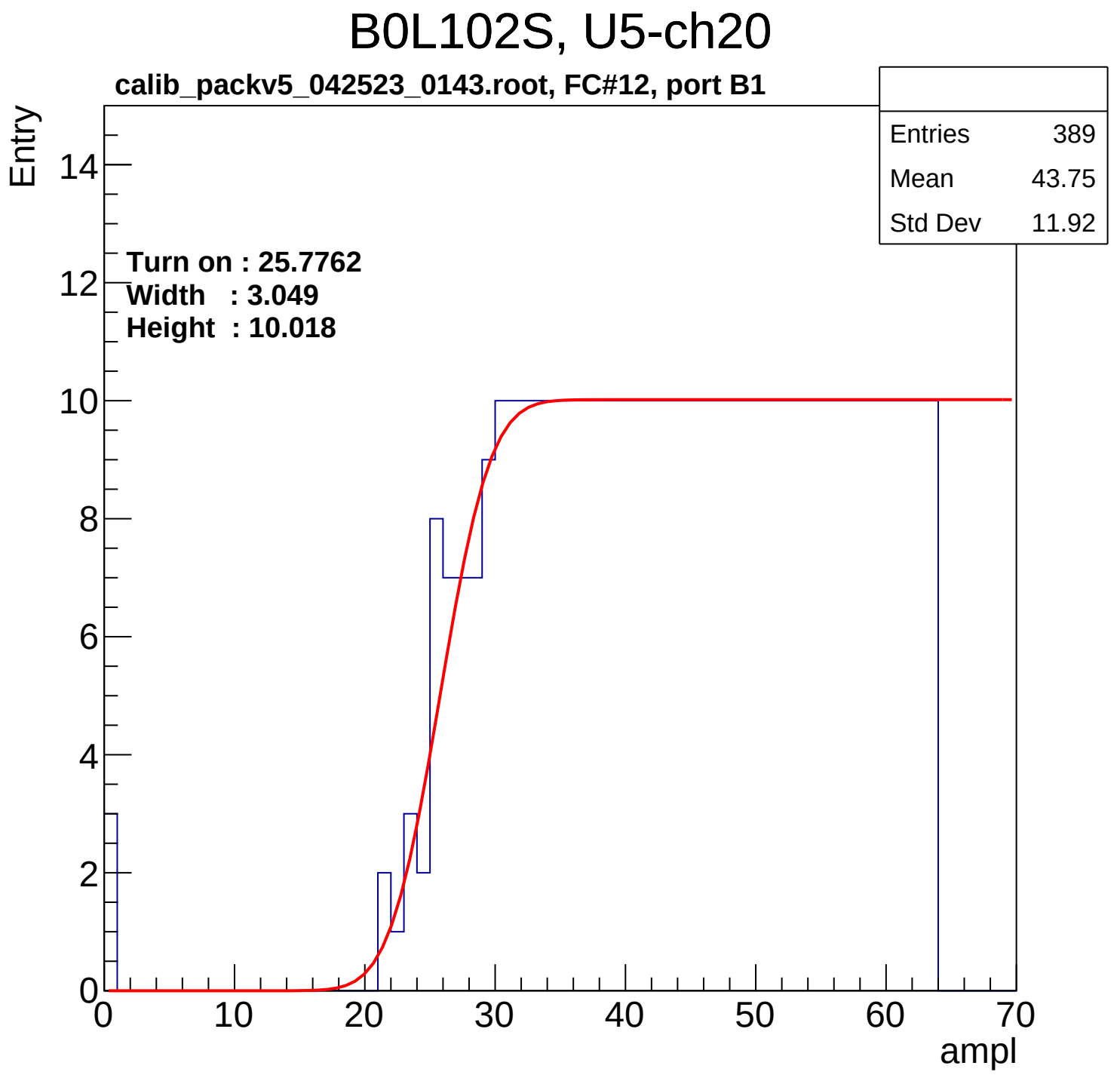
B0L102S, U5-ch20
calib_packv5_042523_0143.root, FC#12, port B1
Entries 389
Mean 43.75
Std Dev 11.92
Turn on : 25.7762
Width : 3.049
Height : 10.018
Entry
ampl
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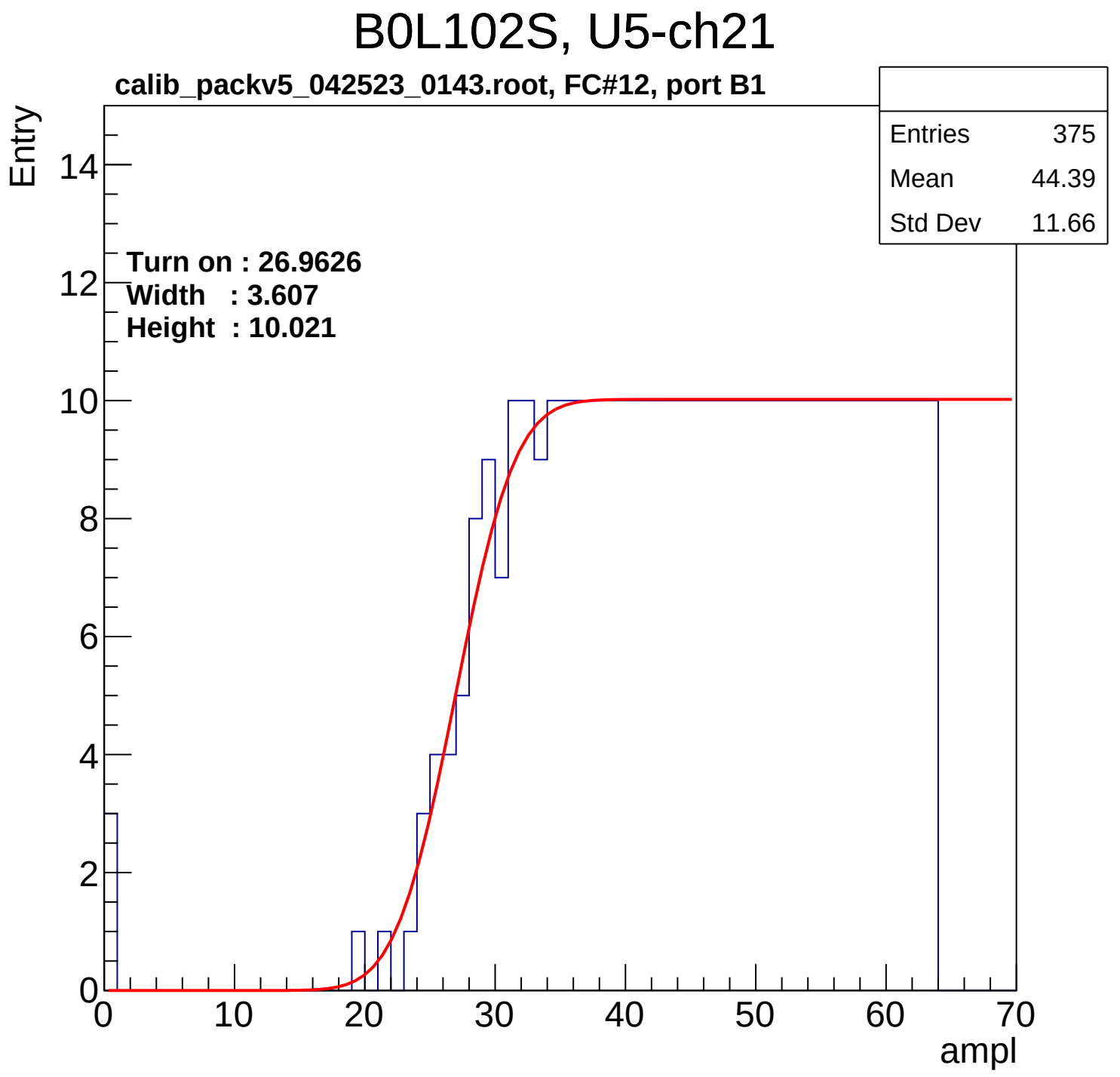
B0L102S, U5-ch21
calib_packv5_042523_0143.root, FC#12, port B1
Entries 375
Mean 44.39
Std Dev 11.66
Turn on : 26.9626
Width : 3.607
Height : 10.021
Entry
ampl
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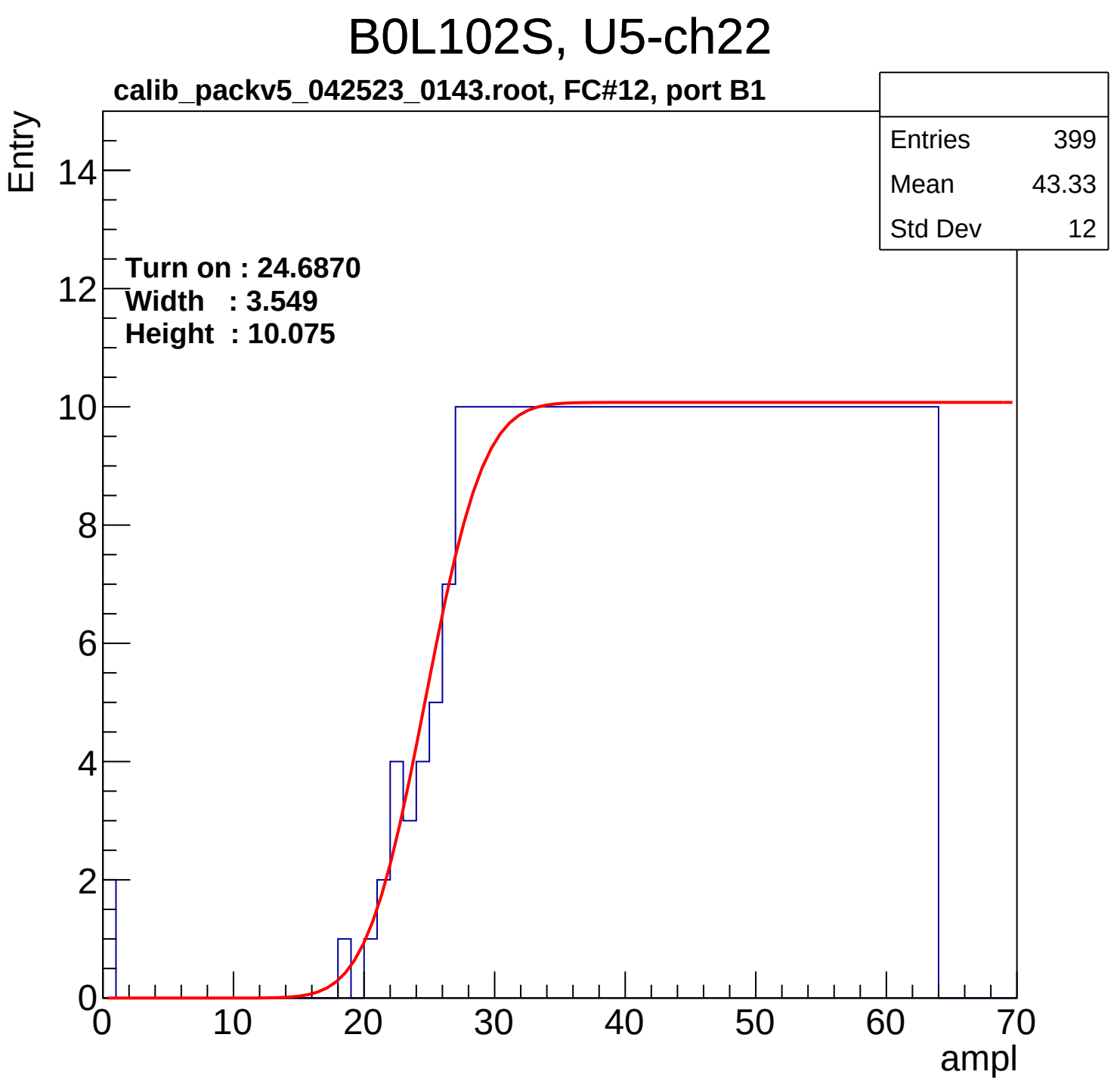
B0L102S, U5-ch22
calib_packv5_042523_0143.root, FC#12, port B1
Entries 399
Mean 43.33
Std Dev 12
Turn on : 24.6870
Width : 3.549
Height : 10.075
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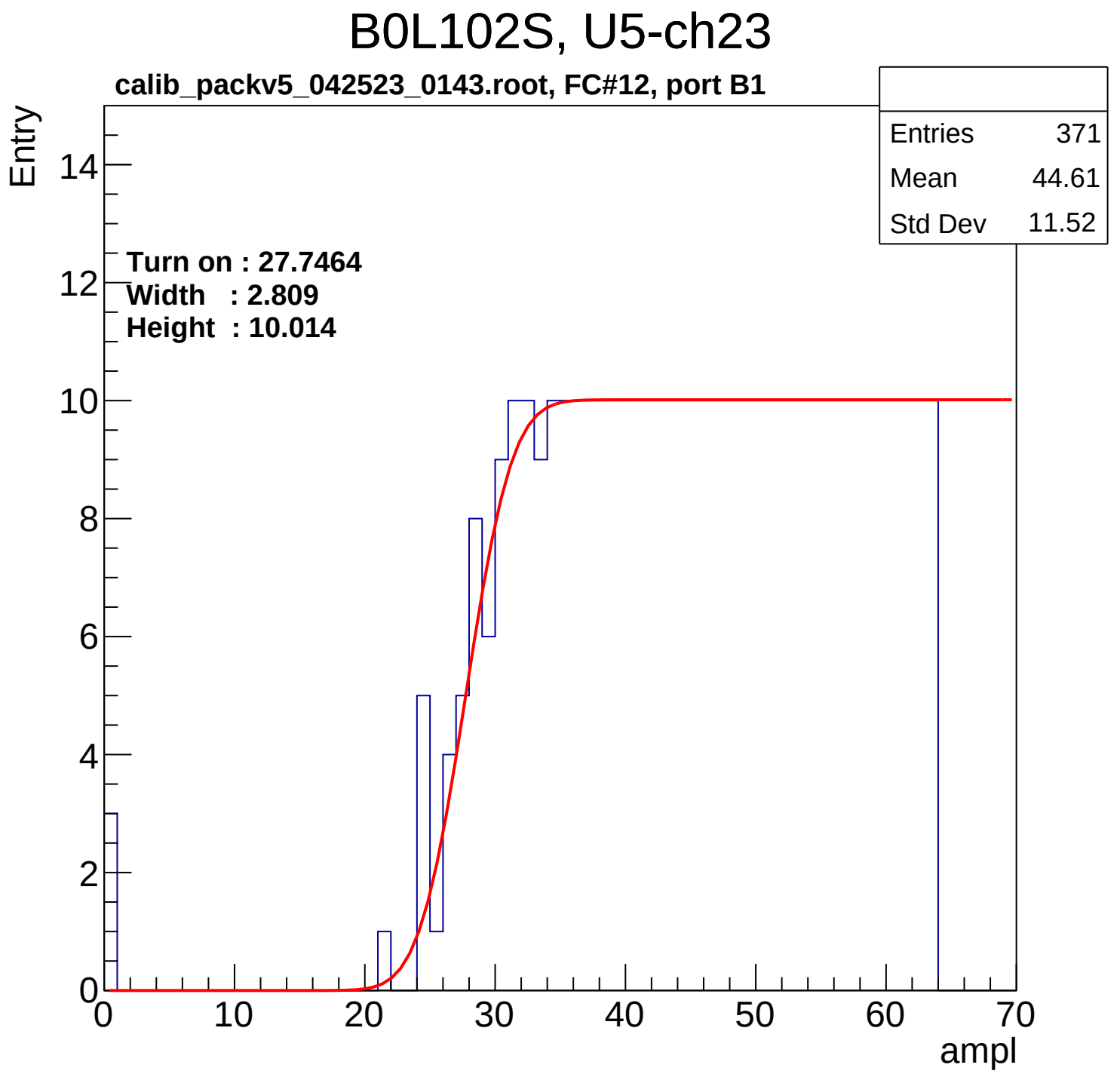
B0L102S, U5-ch23
calib_packv5_042523_0143.root, FC#12, port B1
Entries 371
Mean 44.61
Std Dev 11.52
Turn on : 27.7464
Width : 2.809
Height : 10.014
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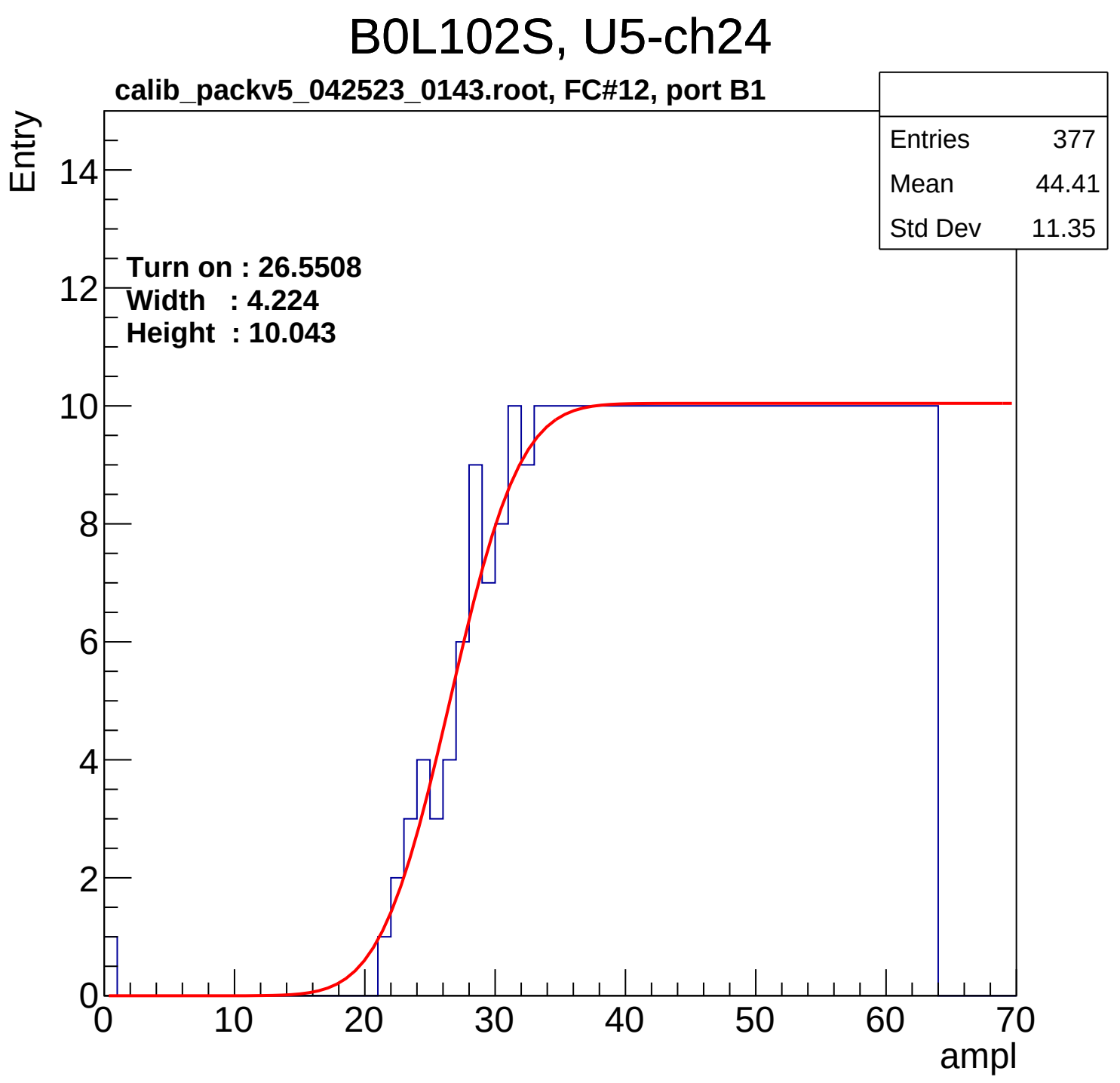
B0L102S, U5-ch24
calib_packv5_042523_0143.root, FC#12, port B1
Entries 377
Mean 44.41
Std Dev 11.35
Turn on : 26.5508
Width : 4.224
Height : 10.043
Entry
ampl
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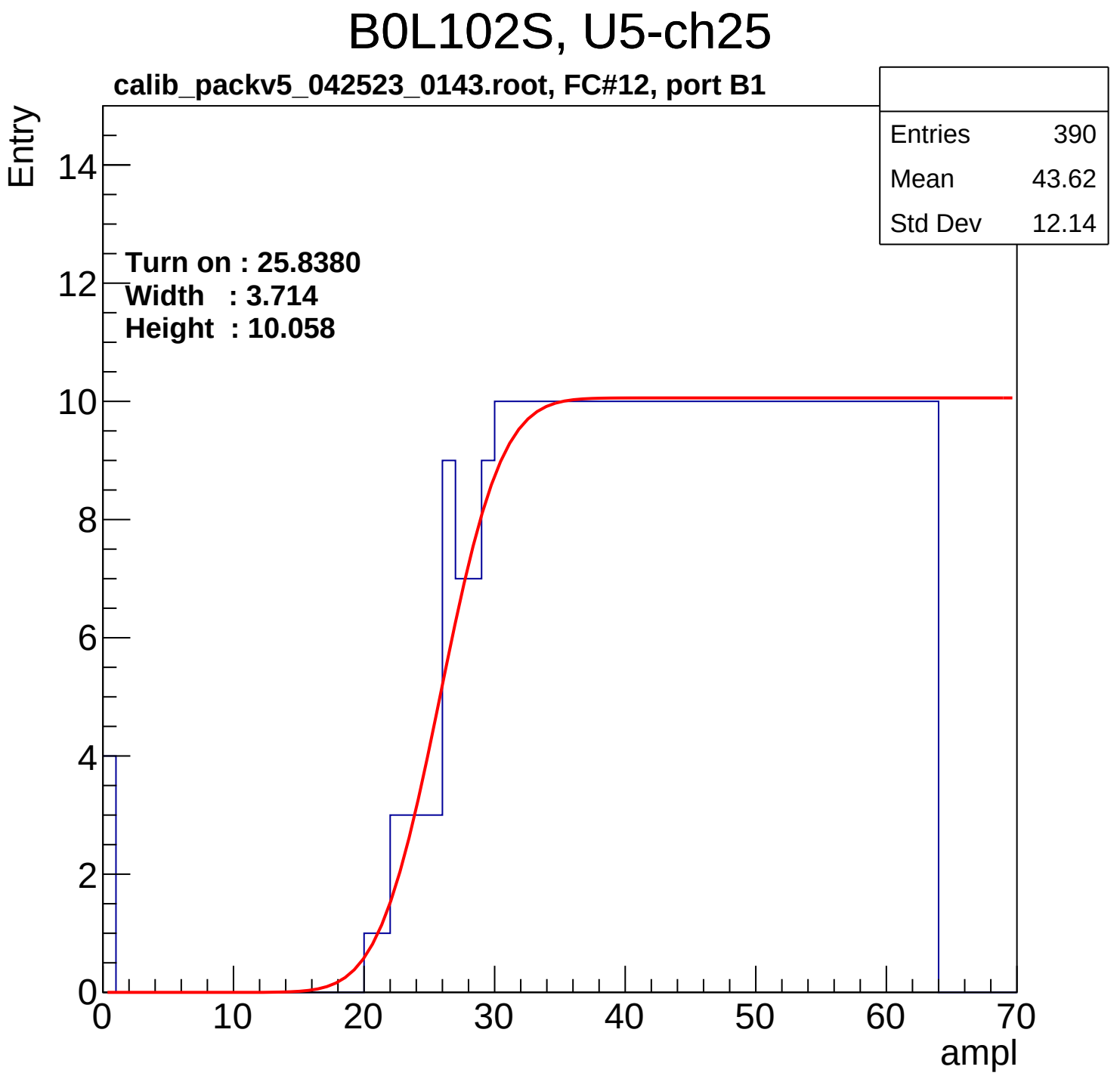
B0L102S, U5-ch25
calib_packv5_042523_0143.root, FC#12, port B1
Entries 390
Mean 43.62
Std Dev 12.14
Turn on : 25.8380
Width : 3.714
Height : 10.058
Entry
ampl
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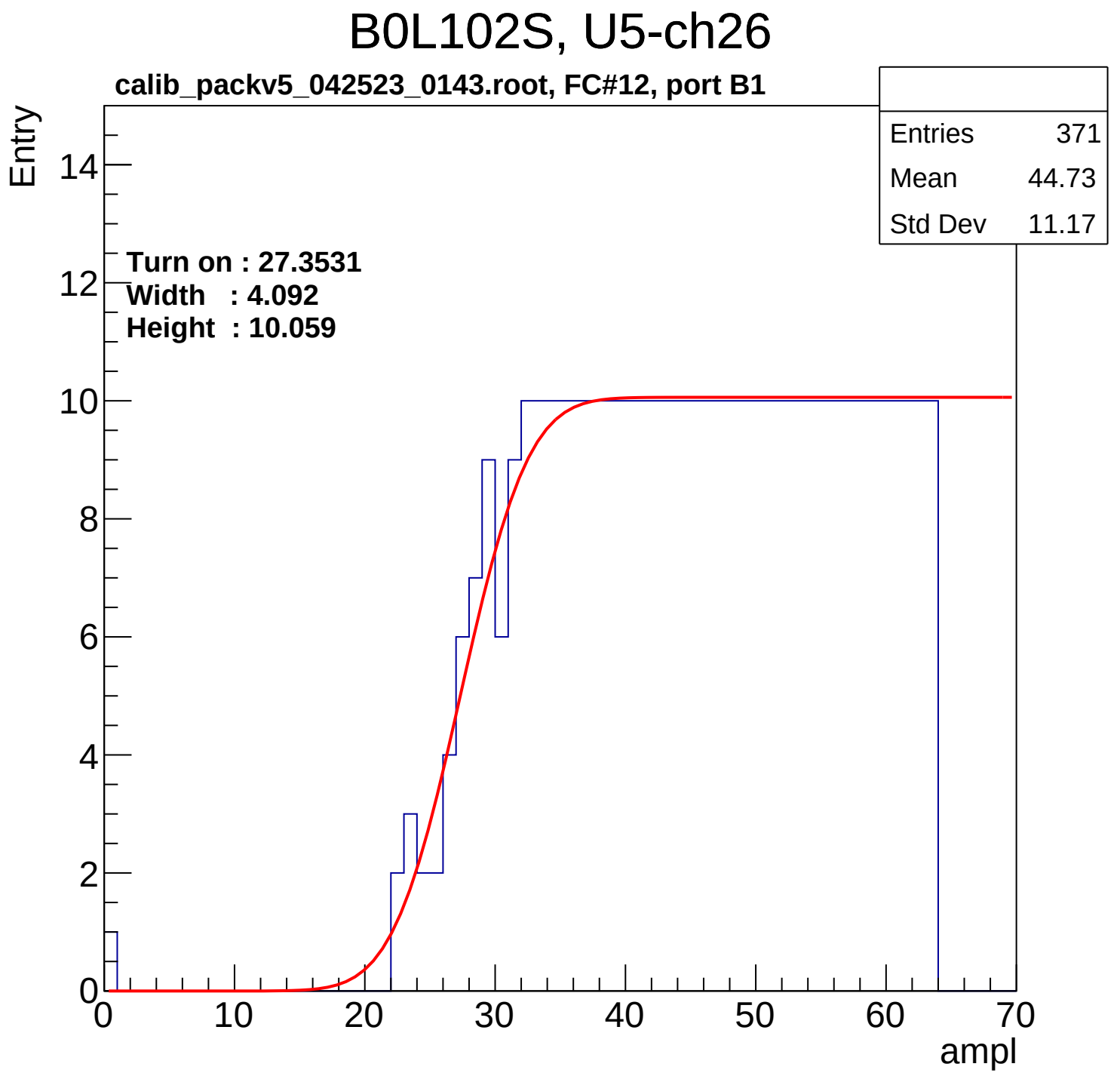
B0L102S, U5-ch26
calib_packv5_042523_0143.root, FC#12, port B1
Entries 371
Mean 44.73
Std Dev 11.17
Turn on : 27.3531
Width : 4.092
Height : 10.059
Entry
ampl
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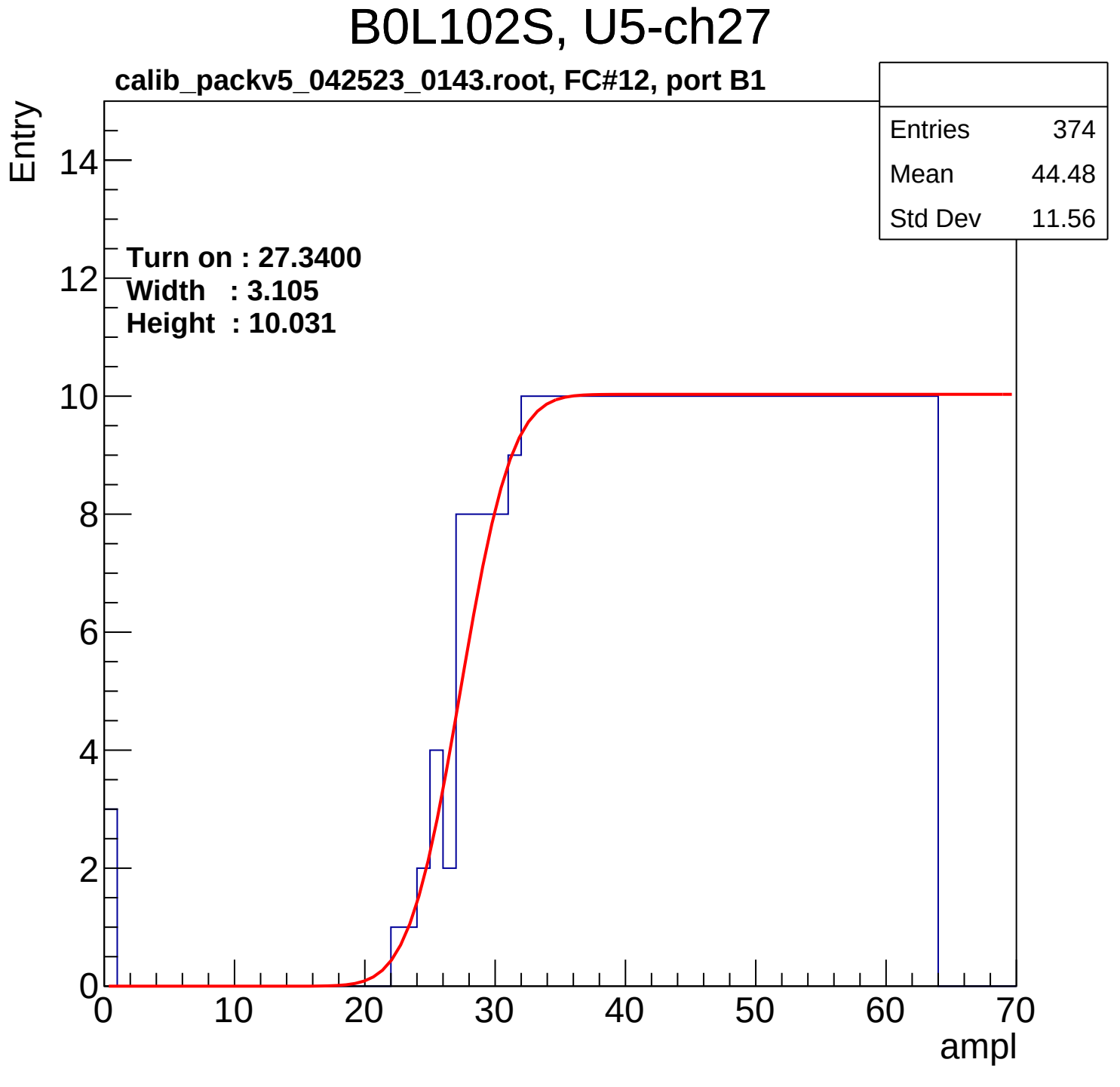
B0L102S, U5-ch27
calib_packv5_042523_0143.root, FC#12, port B1
Entries 374
Mean 44.48
Std Dev 11.56
Turn on : 27.3400
Width : 3.105
Height : 10.031
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ampl
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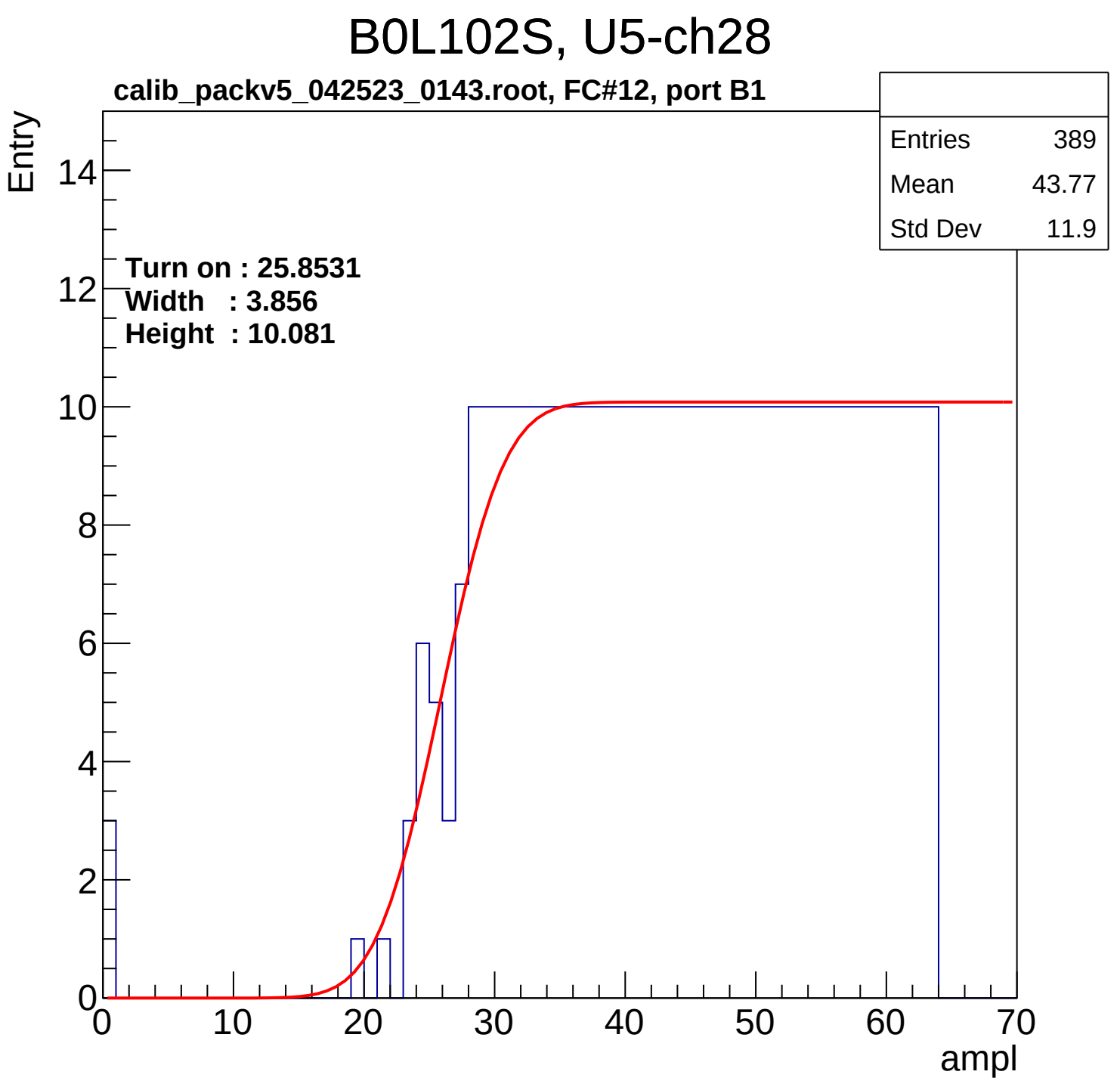
B0L102S, U5-ch28
calib_packv5_042523_0143.root, FC#12, port B1
Entries 389
Mean 43.77
Std Dev 11.9
Turn on : 25.8531
Width : 3.856
Height : 10.081
Entry
ampl
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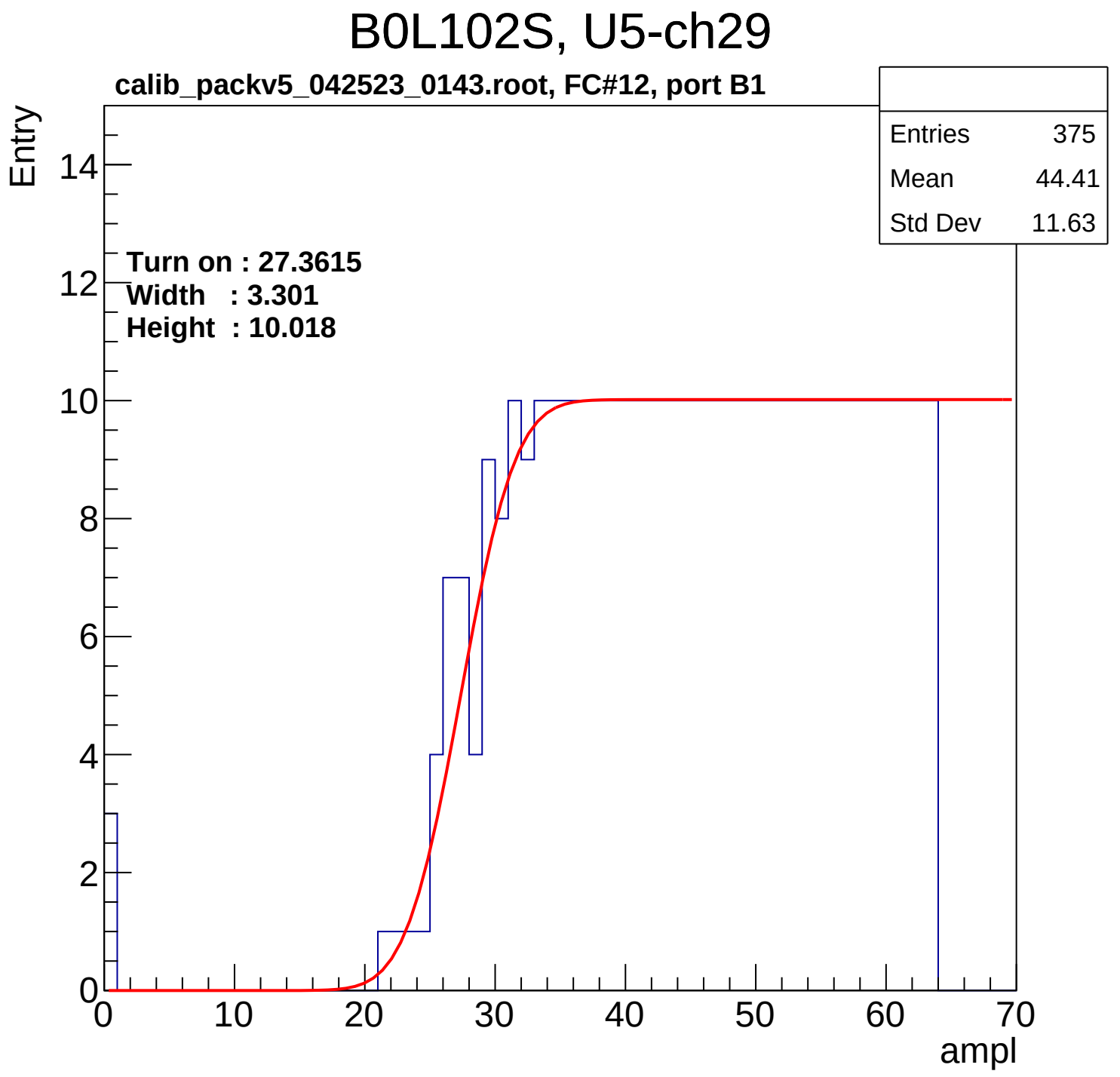
B0L102S, U5-ch29
calib_packv5_042523_0143.root, FC#12, port B1
Entries 375
Mean 44.41
Std Dev 11.63
Turn on : 27.3615
Width : 3.301
Height : 10.018
Entry
ampl
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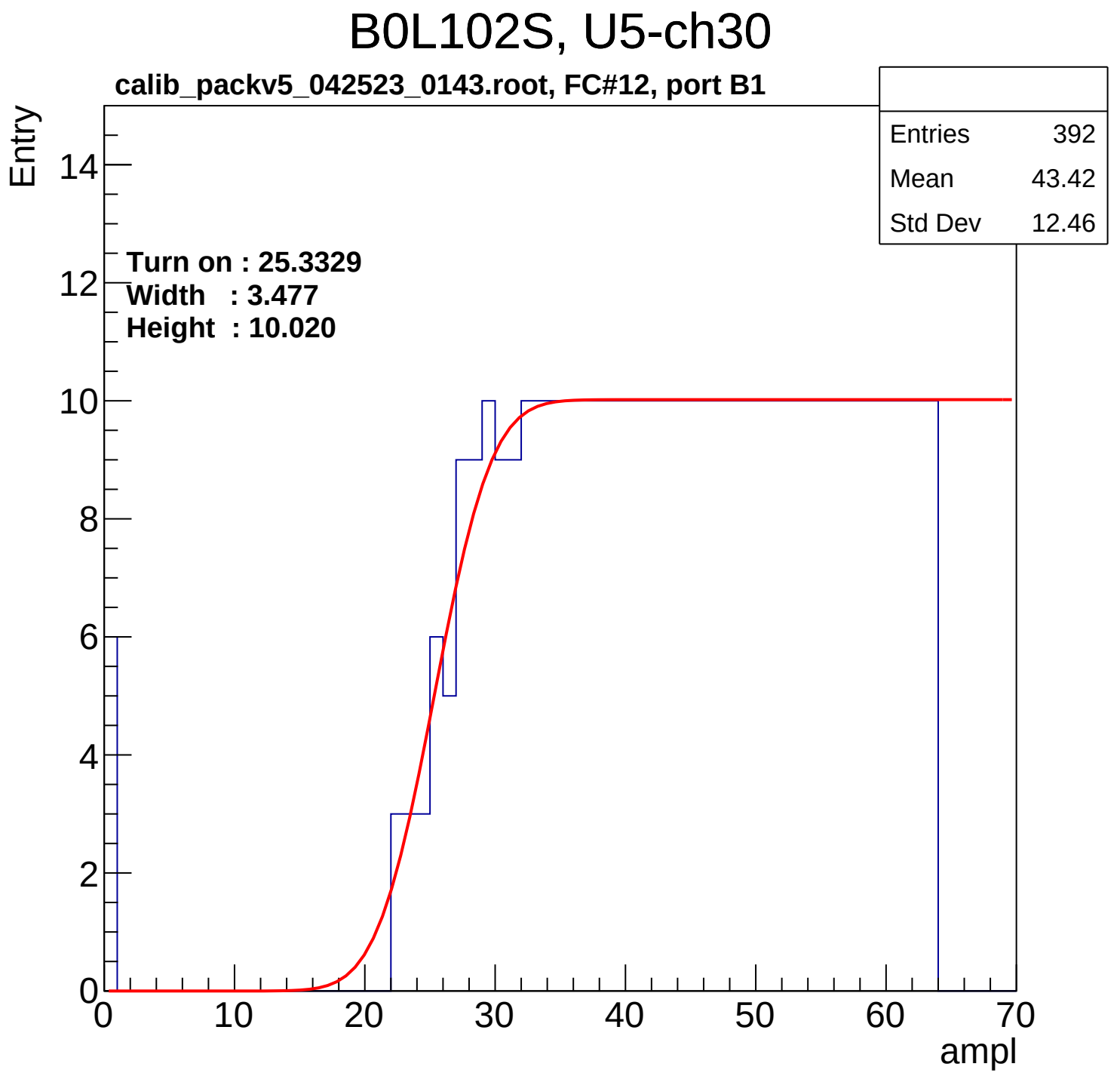
B0L102S, U5-ch30
calib_packv5_042523_0143.root, FC#12, port B1
Entries 392
Mean 43.42
Std Dev 12.46
Turn on : 25.3329
Width : 3.477
Height : 10.020
Entry
ampl
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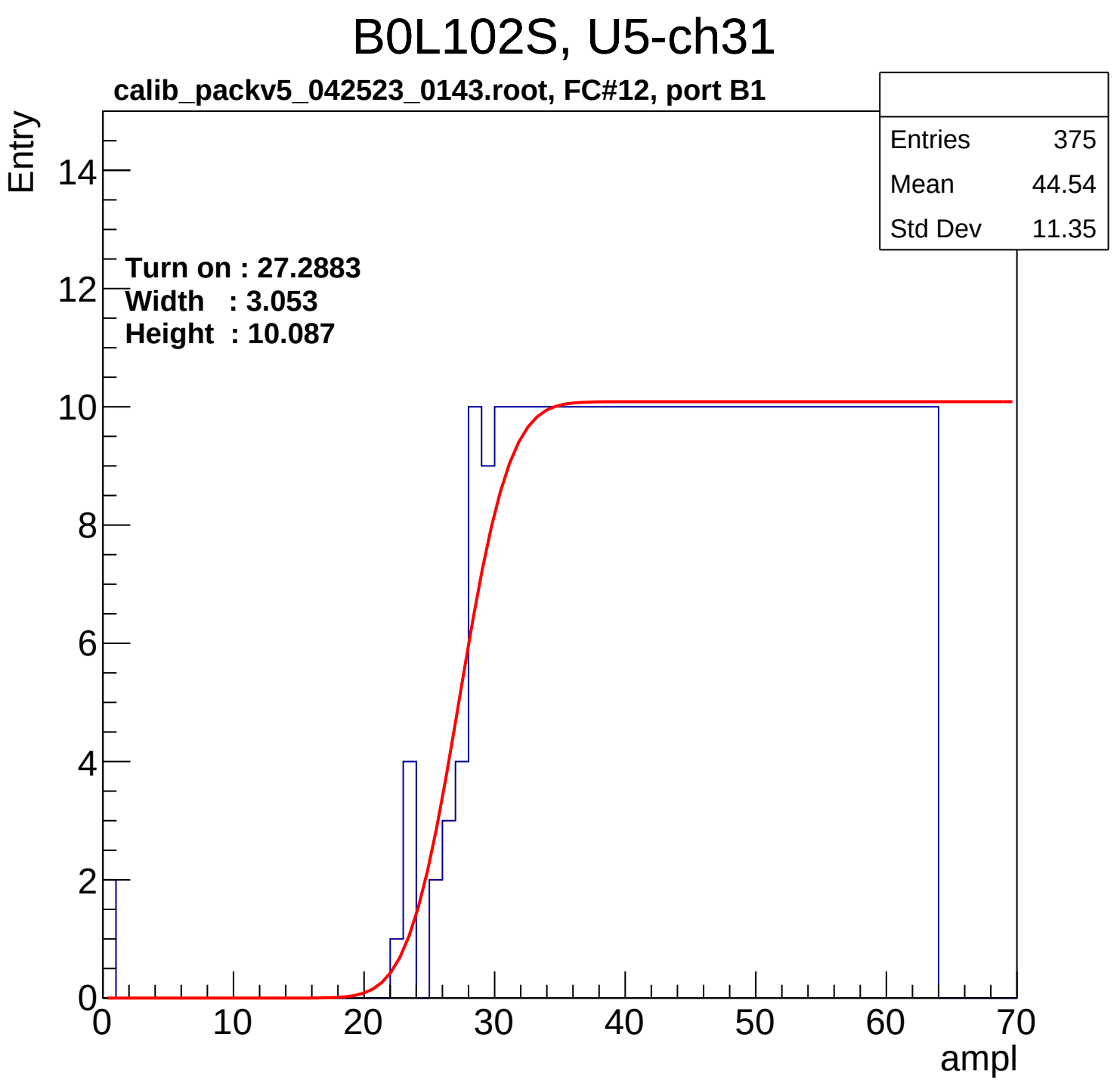
B0L102S, U5-ch31
calib_packv5_042523_0143.root, FC#12, port B1
Entries 375
Mean 44.54
Std Dev 11.35
Turn on : 27.2883
Width : 3.053
Height : 10.087
Entry
ampl
0
2
4
6
8
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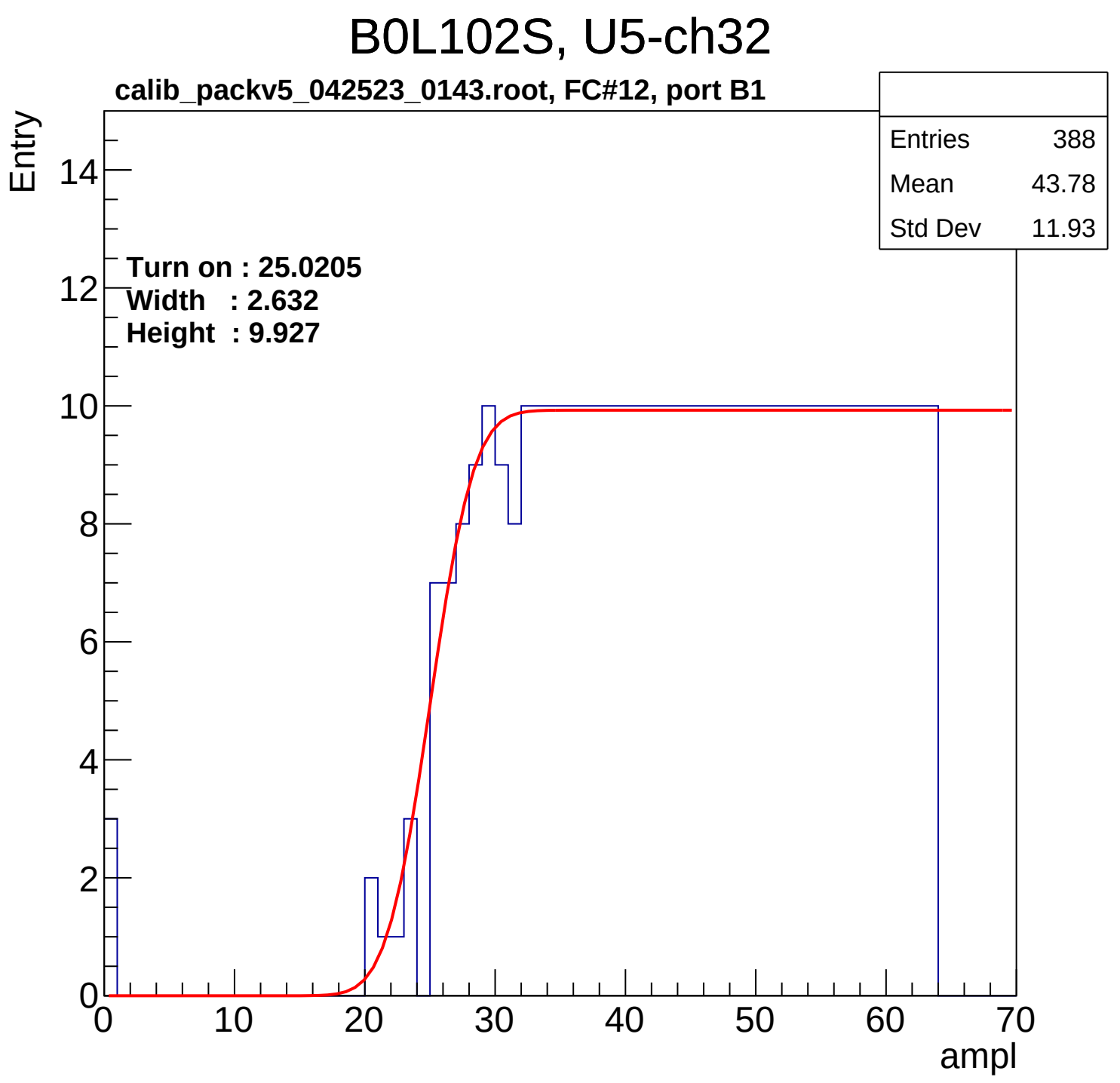
B0L102S, U5-ch32
calib_packv5_042523_0143.root, FC#12, port B1
Entries 388
Mean 43.78
Std Dev 11.93
Turn on : 25.0205
Width : 2.632
Height : 9.927
Entry
ampl
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0
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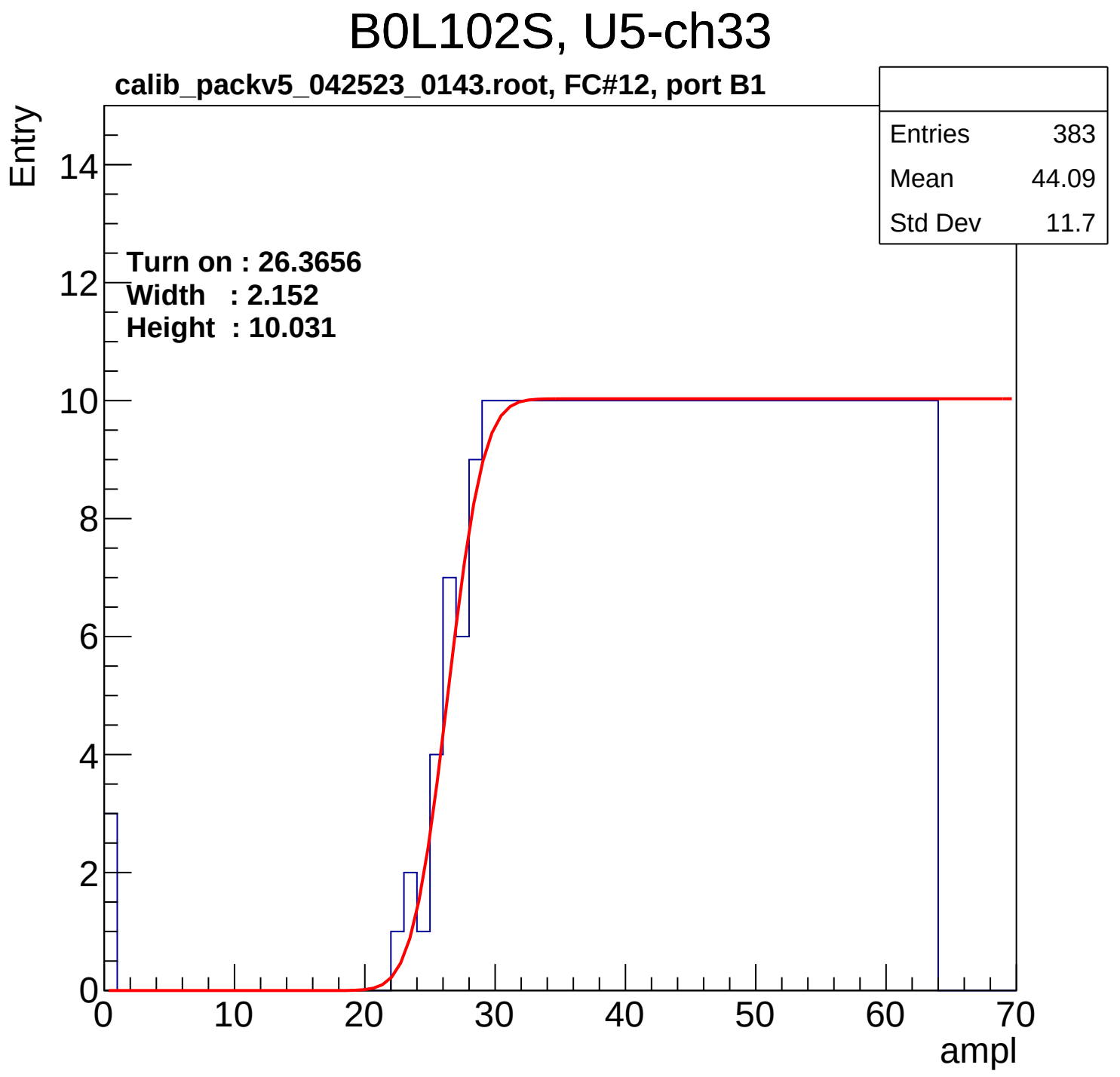
B0L102S, U5-ch33
calib_packv5_042523_0143.root, FC#12, port B1
Entries 383
Mean 44.09
Std Dev 11.7
Turn on : 26.3656
Width : 2.152
Height : 10.031
Entry
ampl
0
2
4
6
8
10
12
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0
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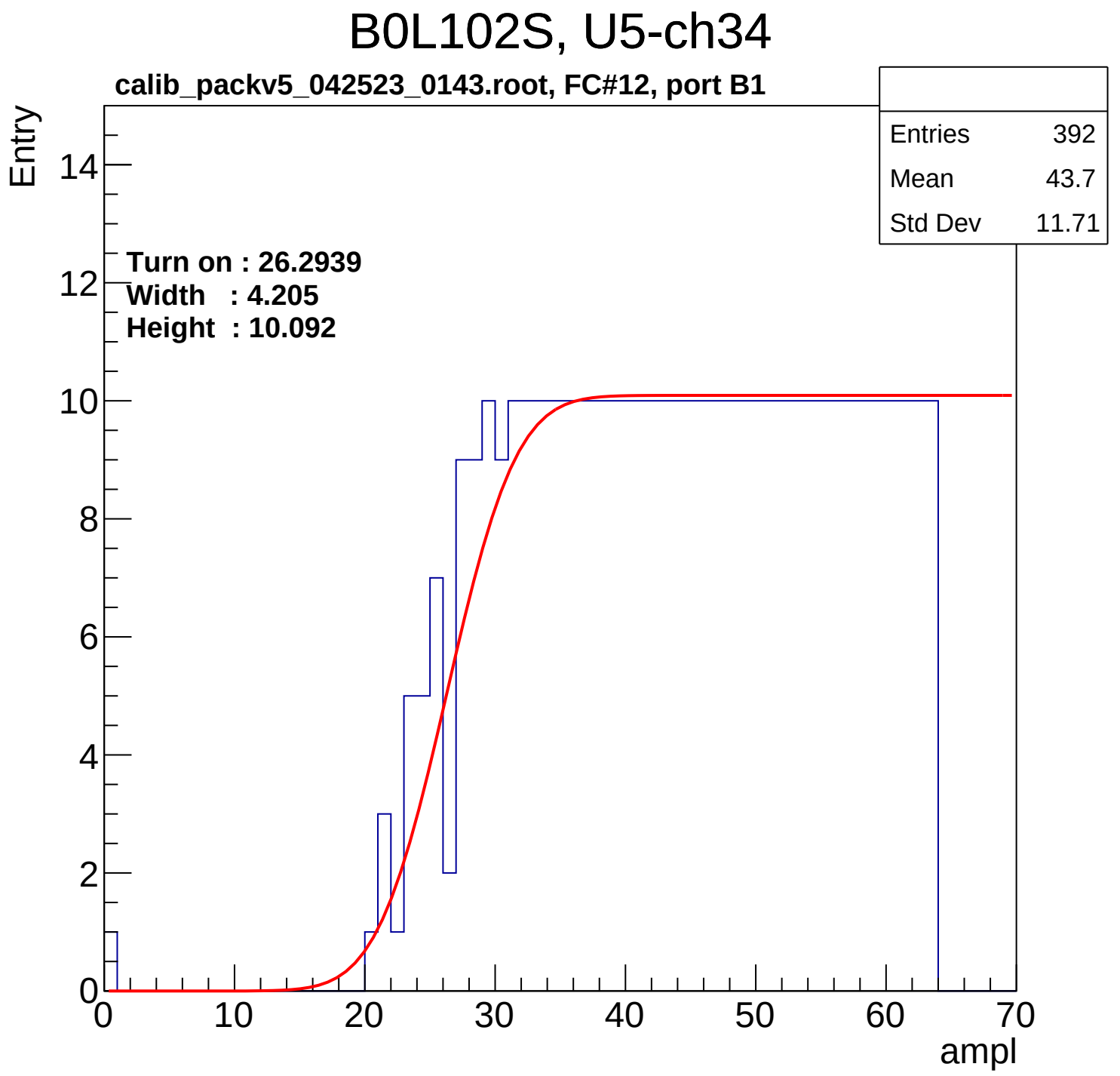
B0L102S, U5-ch34
calib_packv5_042523_0143.root, FC#12, port B1
Entries 392
Mean 43.7
Std Dev 11.71
Turn on : 26.2939
Width : 4.205
Height : 10.092
Entry
ampl
0
2
4
6
8
10
12
14
0
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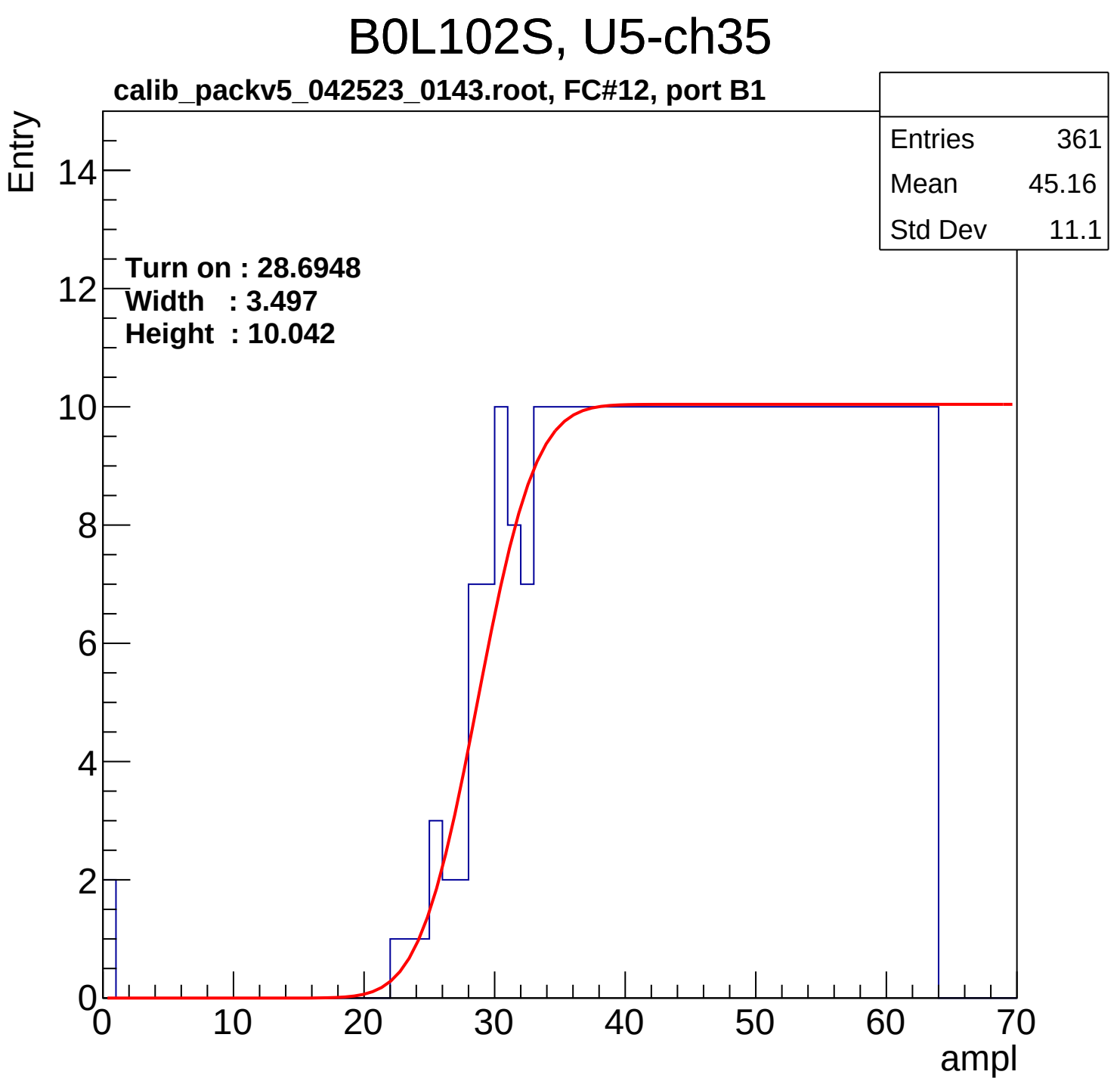
B0L102S, U5-ch35
calib_packv5_042523_0143.root, FC#12, port B1
Entries 361
Mean 45.16
Std Dev 11.1
Turn on : 28.6948
Width : 3.497
Height : 10.042
Entry
ampl
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6
8
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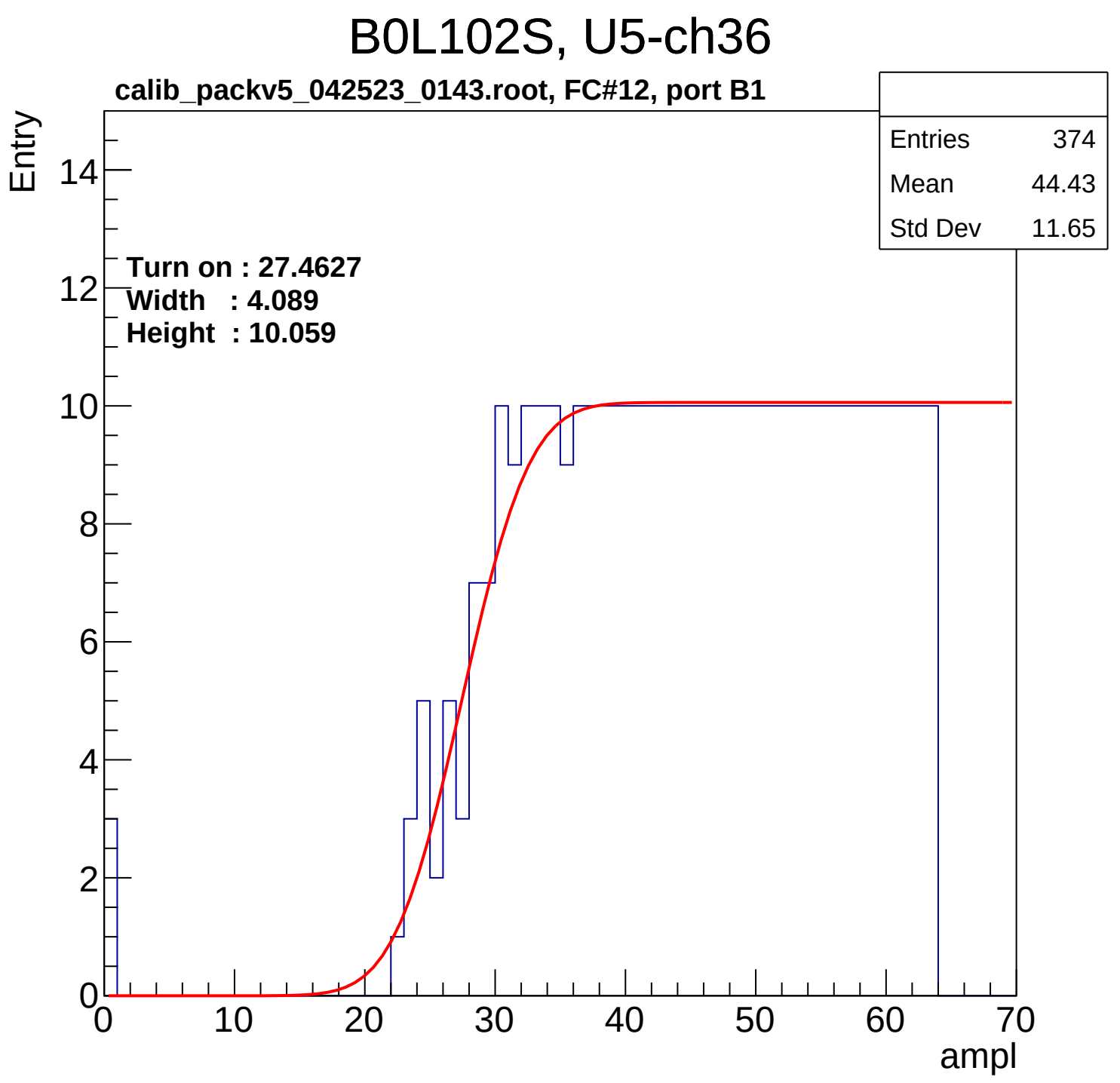
B0L102S, U5-ch36
calib_packv5_042523_0143.root, FC#12, port B1
Entries 374
Mean 44.43
Std Dev 11.65
Turn on : 27.4627
Width : 4.089
Height : 10.059
Entry
ampl
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2
4
6
8
10
12
14
0
10
20
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40
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60
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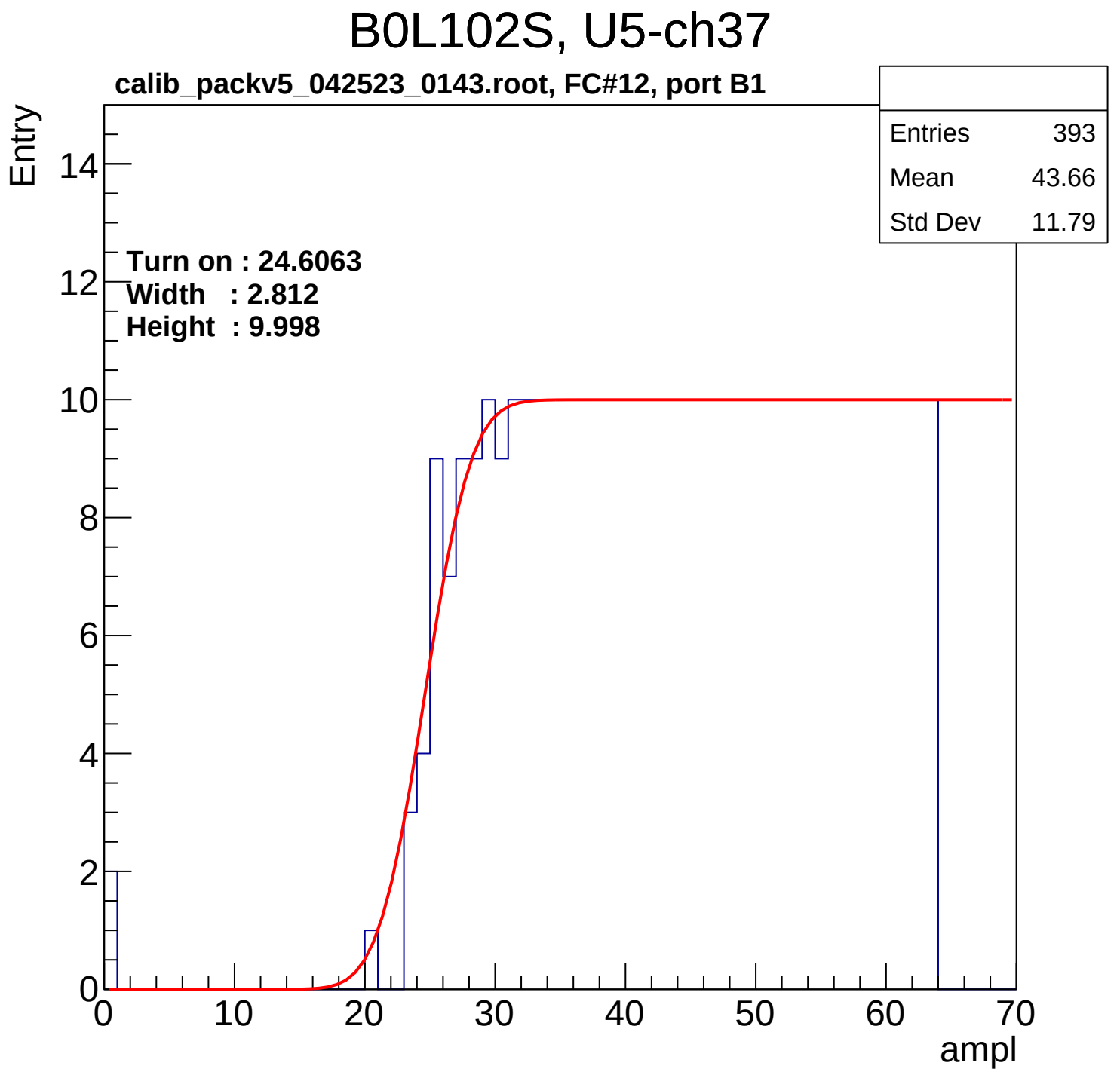
B0L102S, U5-ch37
calib_packv5_042523_0143.root, FC#12, port B1
Entries 393
Mean 43.66
Std Dev 11.79
Turn on : 24.6063
Width : 2.812
Height : 9.998
Entry
ampl
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2
4
6
8
10
12
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0
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60
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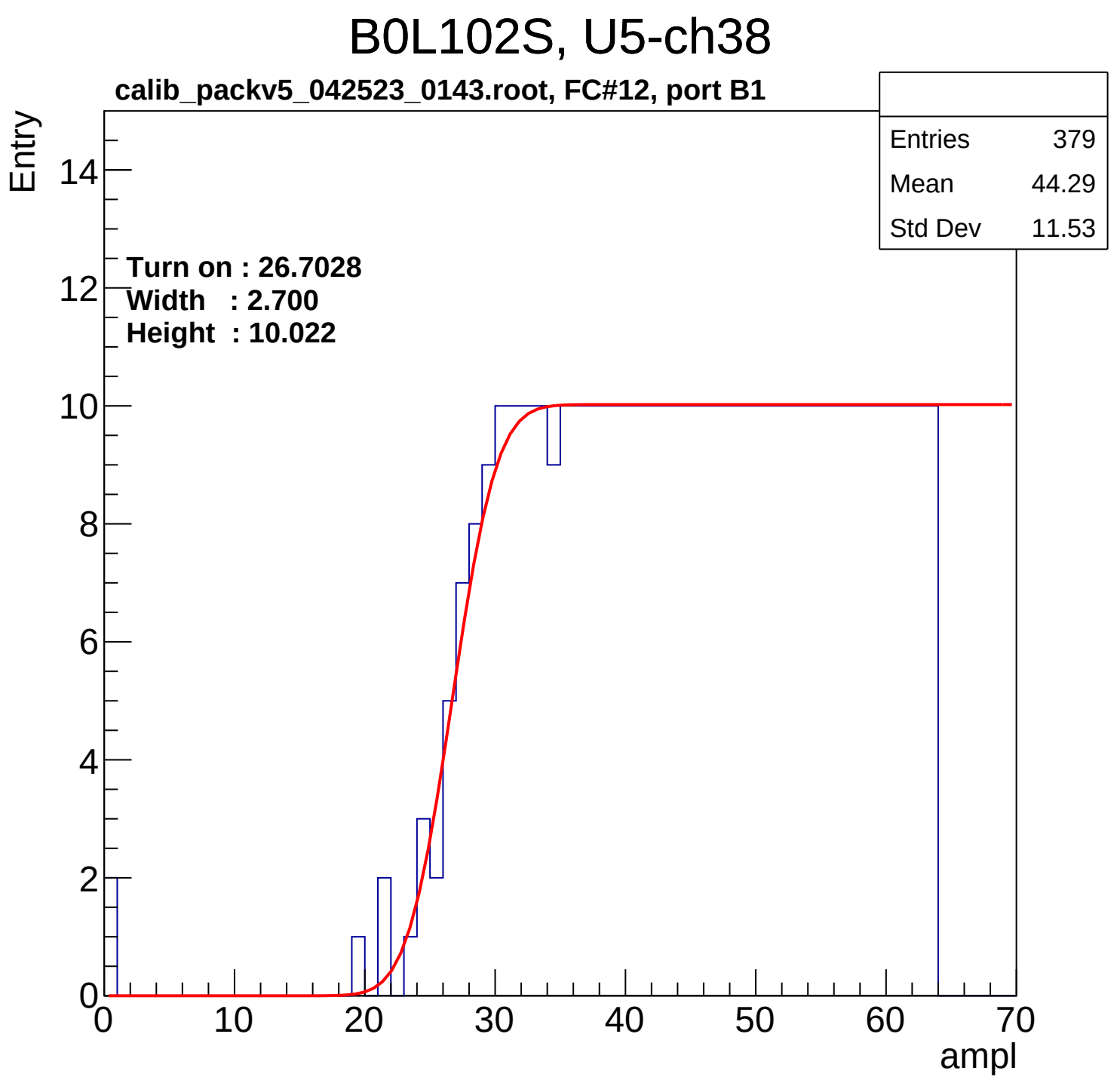
B0L102S, U5-ch38
calib_packv5_042523_0143.root, FC#12, port B1
Entries 379
Mean 44.29
Std Dev 11.53
Turn on : 26.7028
Width : 2.700
Height : 10.022
Entry
ampl
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2
4
6
8
10
12
14
0
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20
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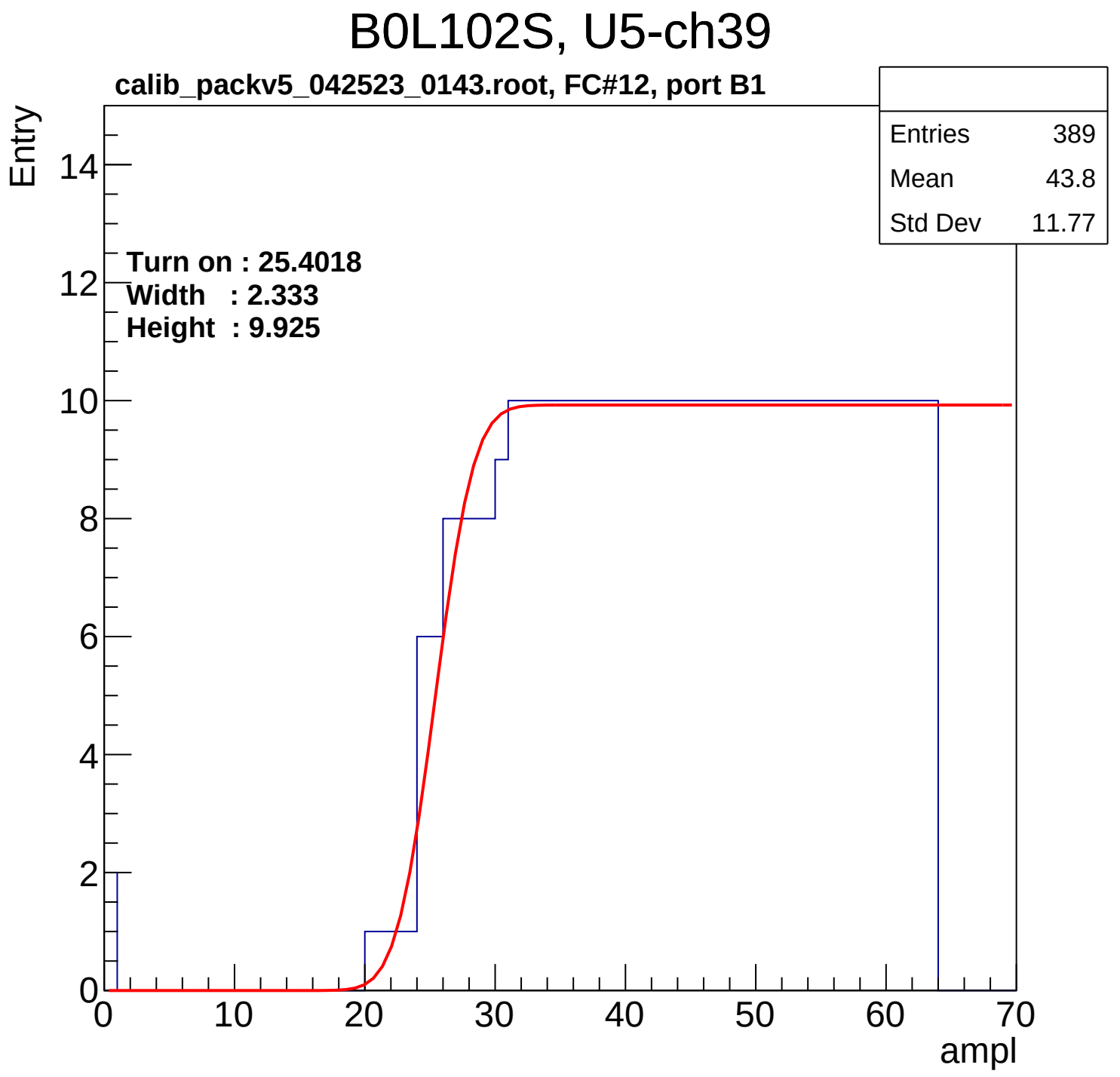
B0L102S, U5-ch39
calib_packv5_042523_0143.root, FC#12, port B1
Entries 389
Mean 43.8
Std Dev 11.77
Turn on : 25.4018
Width : 2.333
Height : 9.925
Entry
ampl
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2
4
6
8
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0
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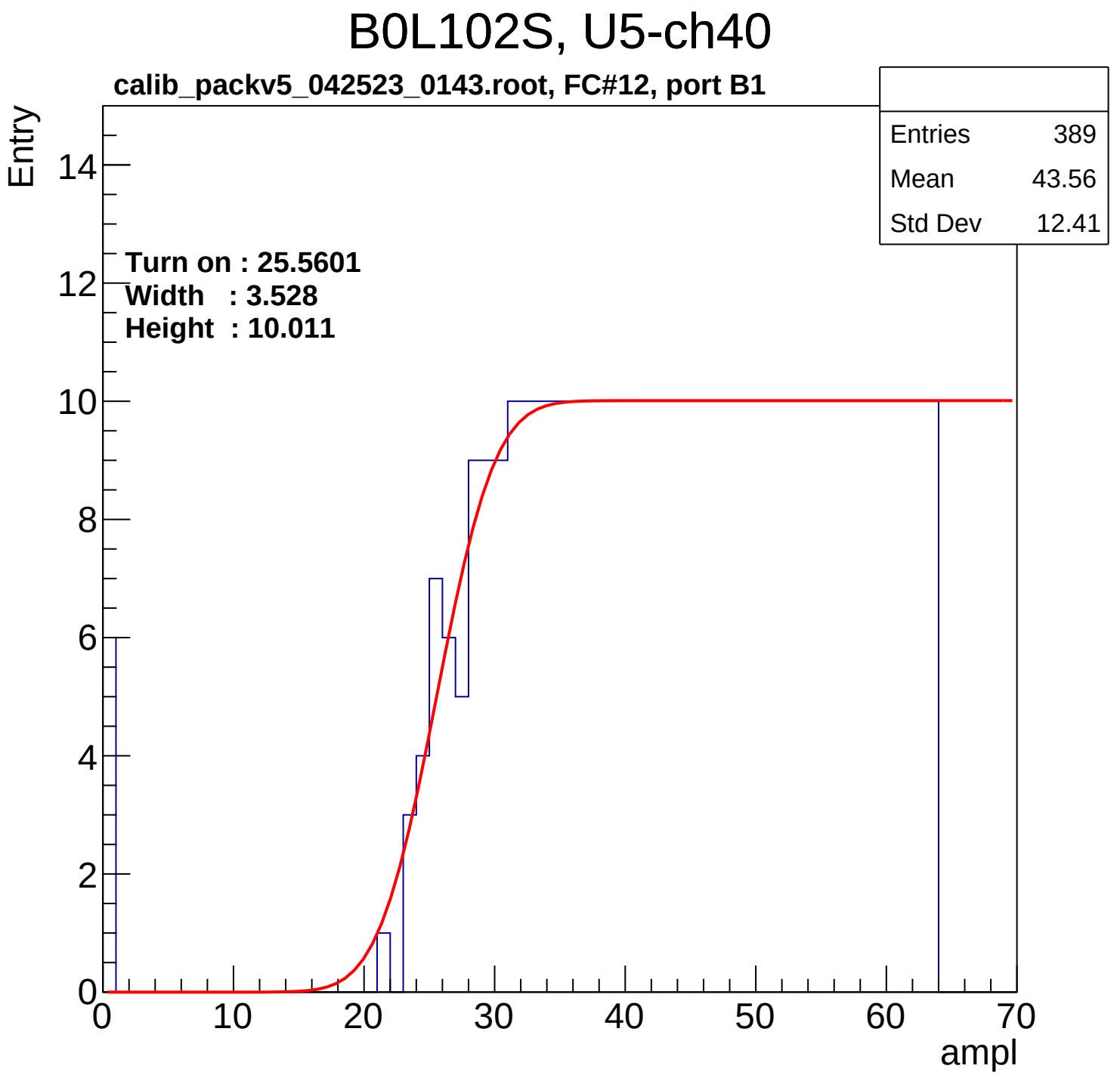
B0L102S, U5-ch40
calib_packv5_042523_0143.root, FC#12, port B1
Entries 389
Mean 43.56
Std Dev 12.41
Turn on : 25.5601
Width : 3.528
Height : 10.011
Entry
ampl
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4
6
8
10
12
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0
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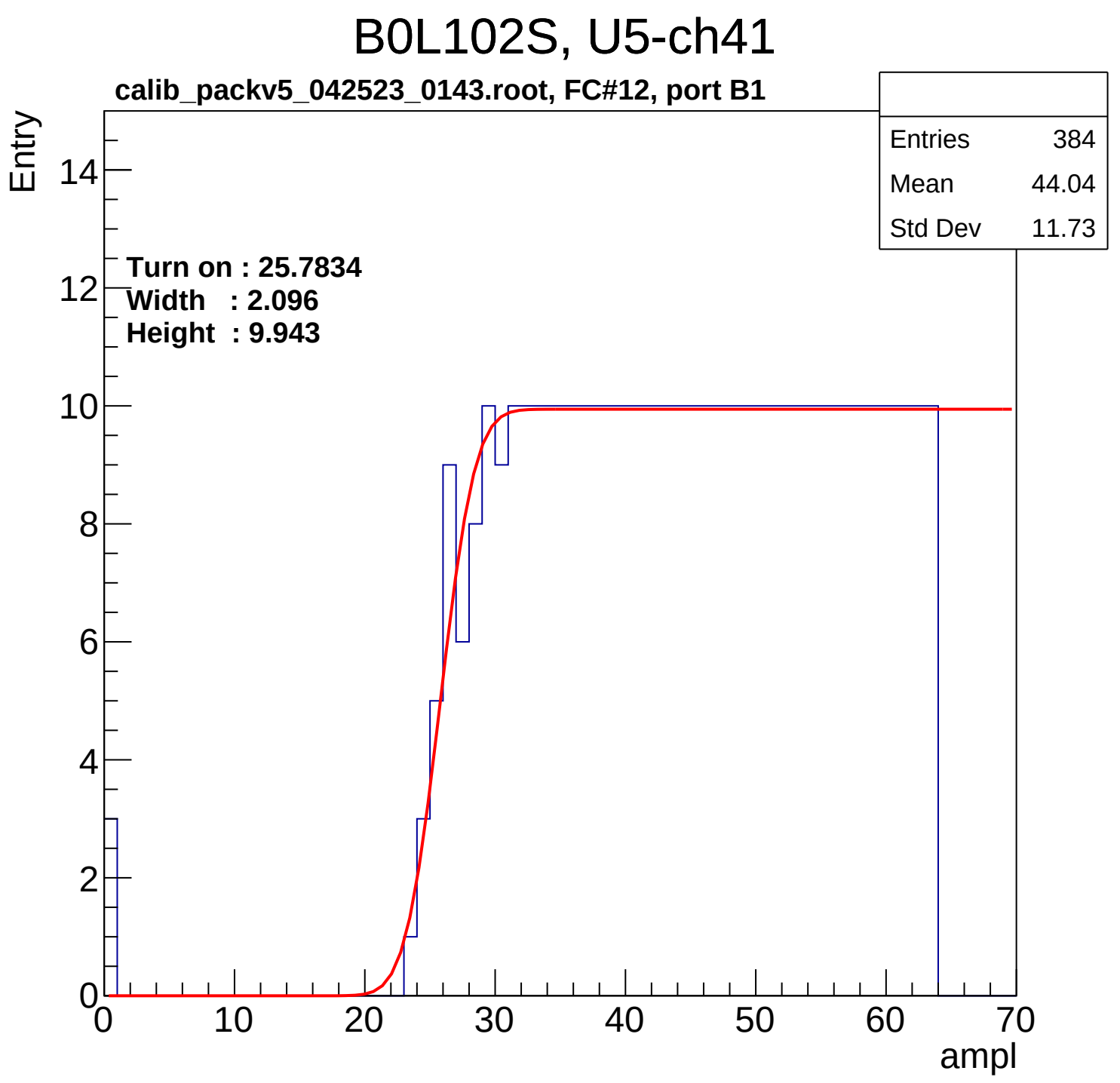
B0L102S, U5-ch41
calib_packv5_042523_0143.root, FC#12, port B1
Entries 384
Mean 44.04
Std Dev 11.73
Turn on : 25.7834
Width : 2.096
Height : 9.943
Entry
ampl
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6
8
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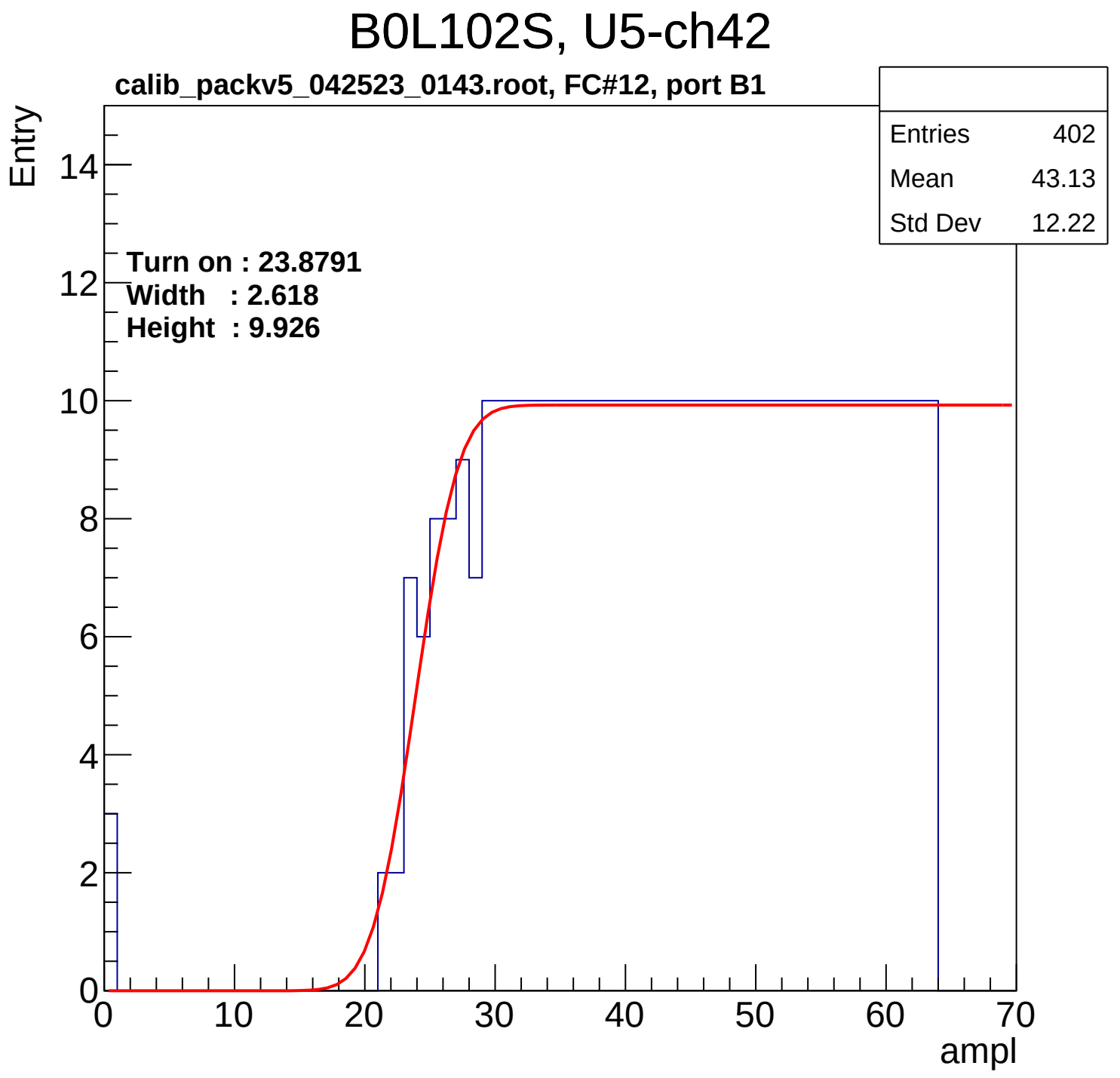
B0L102S, U5-ch42
calib_packv5_042523_0143.root, FC#12, port B1
Entries 402
Mean 43.13
Std Dev 12.22
Turn on : 23.8791
Width : 2.618
Height : 9.926
Entry
ampl
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6
8
10
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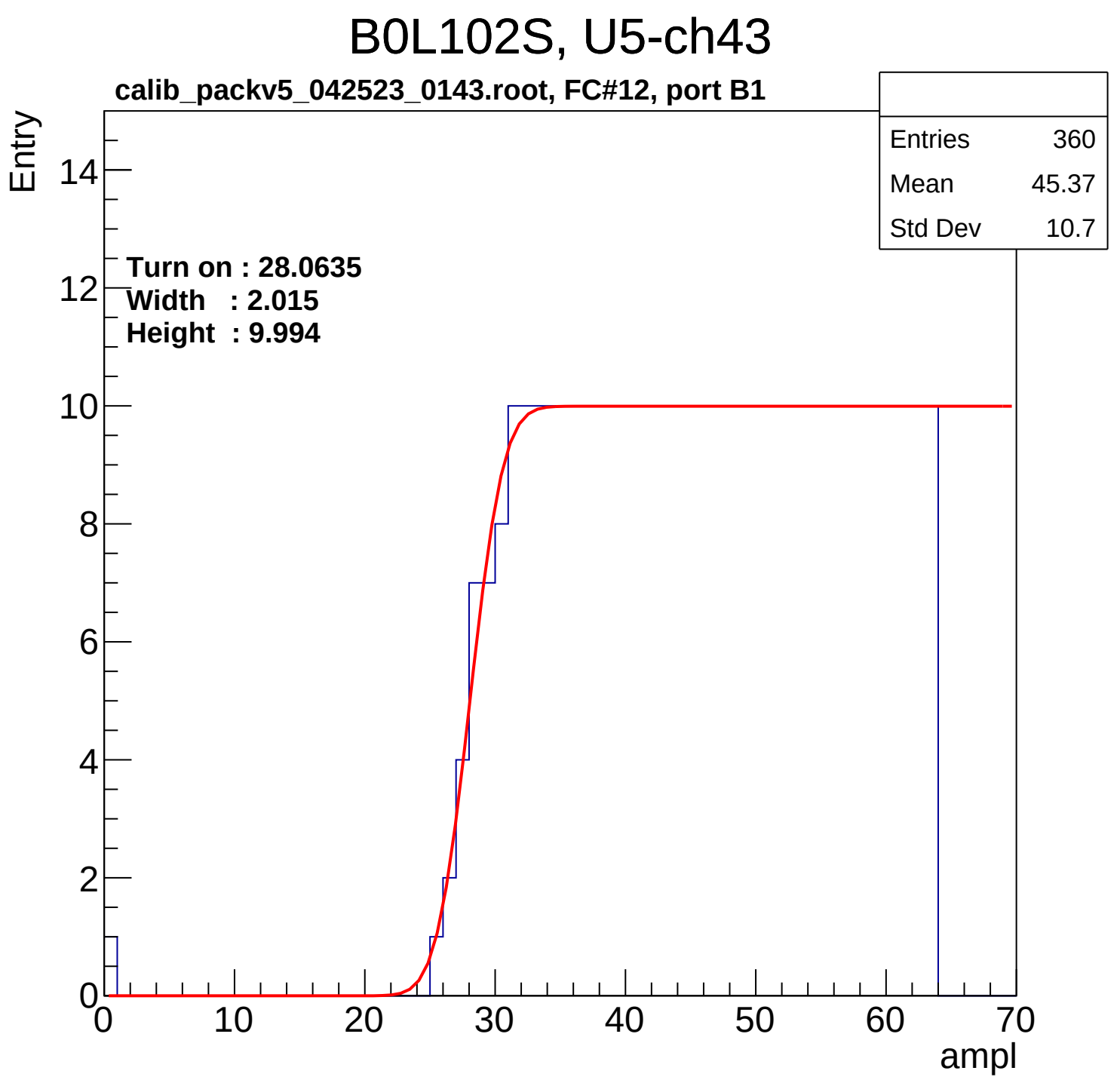
B0L102S, U5-ch43
calib_packv5_042523_0143.root, FC#12, port B1
Entries 360
Mean 45.37
Std Dev 10.7
Turn on : 28.0635
Width : 2.015
Height : 9.994
Entry
ampl
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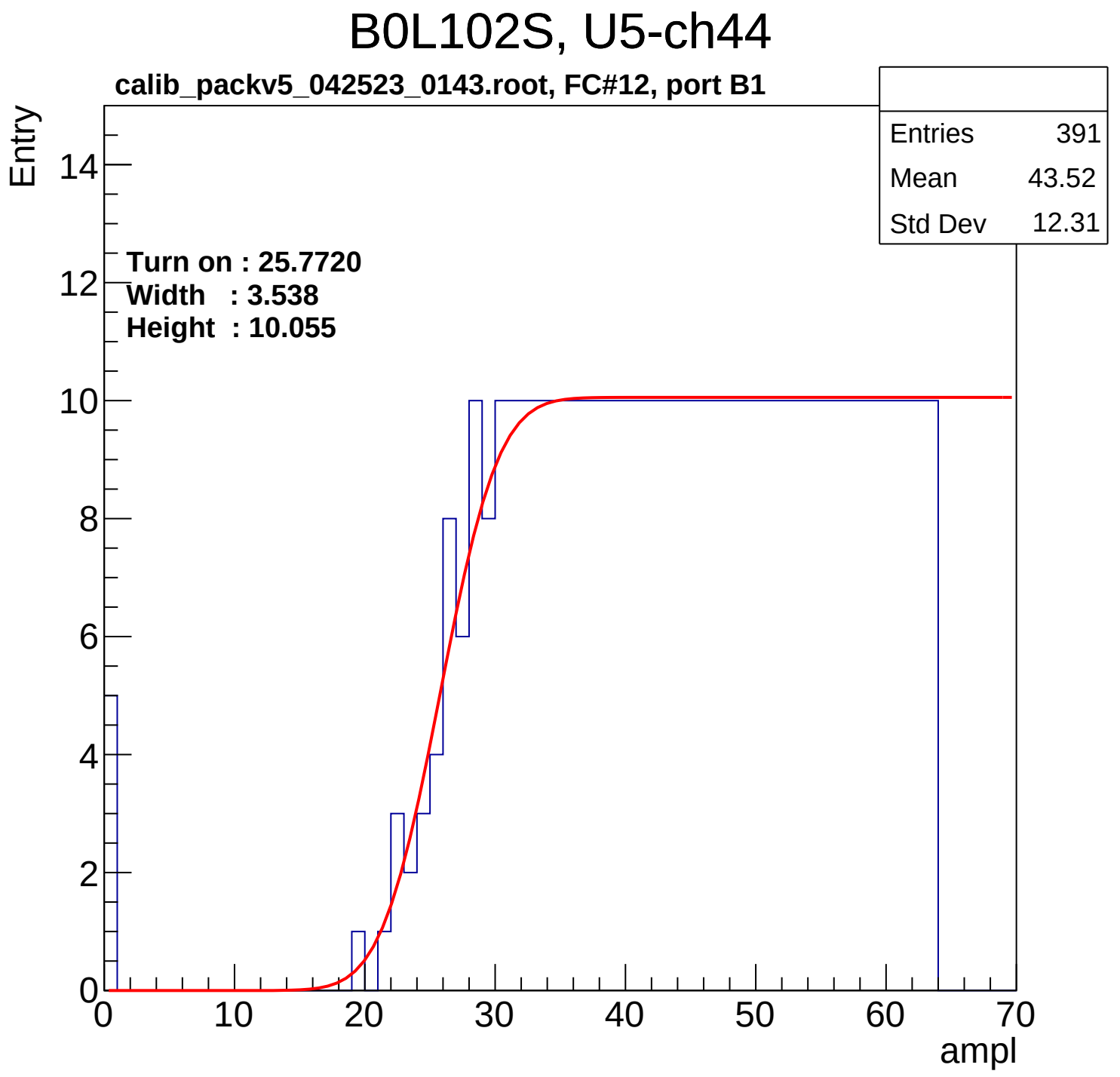
B0L102S, U5-ch44
calib_packv5_042523_0143.root, FC#12, port B1
Entries 391
Mean 43.52
Std Dev 12.31
Turn on : 25.7720
Width : 3.538
Height : 10.055
Entry
ampl
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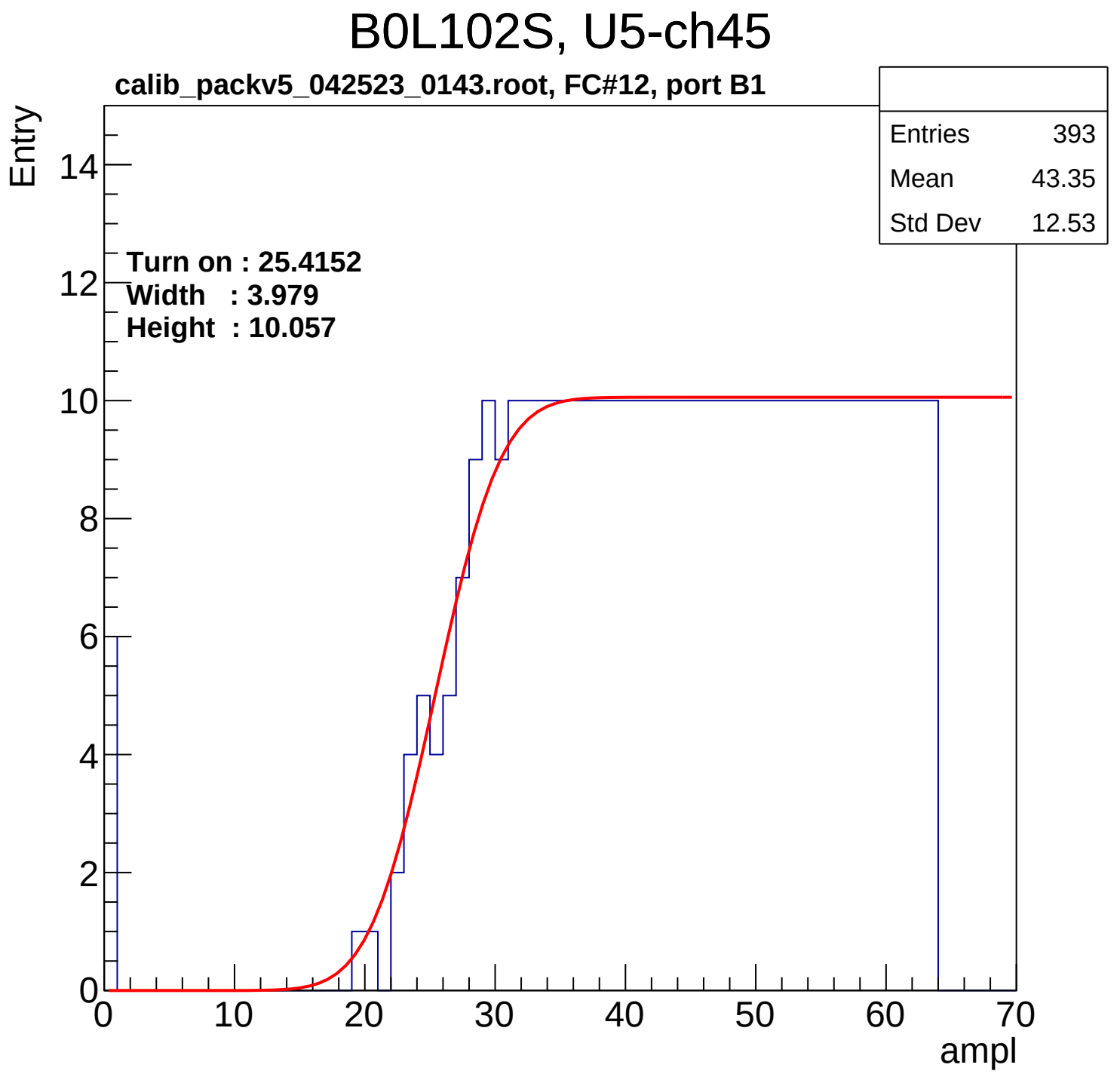
B0L102S, U5-ch45
calib_packv5_042523_0143.root, FC#12, port B1
Entries 393
Mean 43.35
Std Dev 12.53
Turn on : 25.4152
Width : 3.979
Height : 10.057
Entry
ampl
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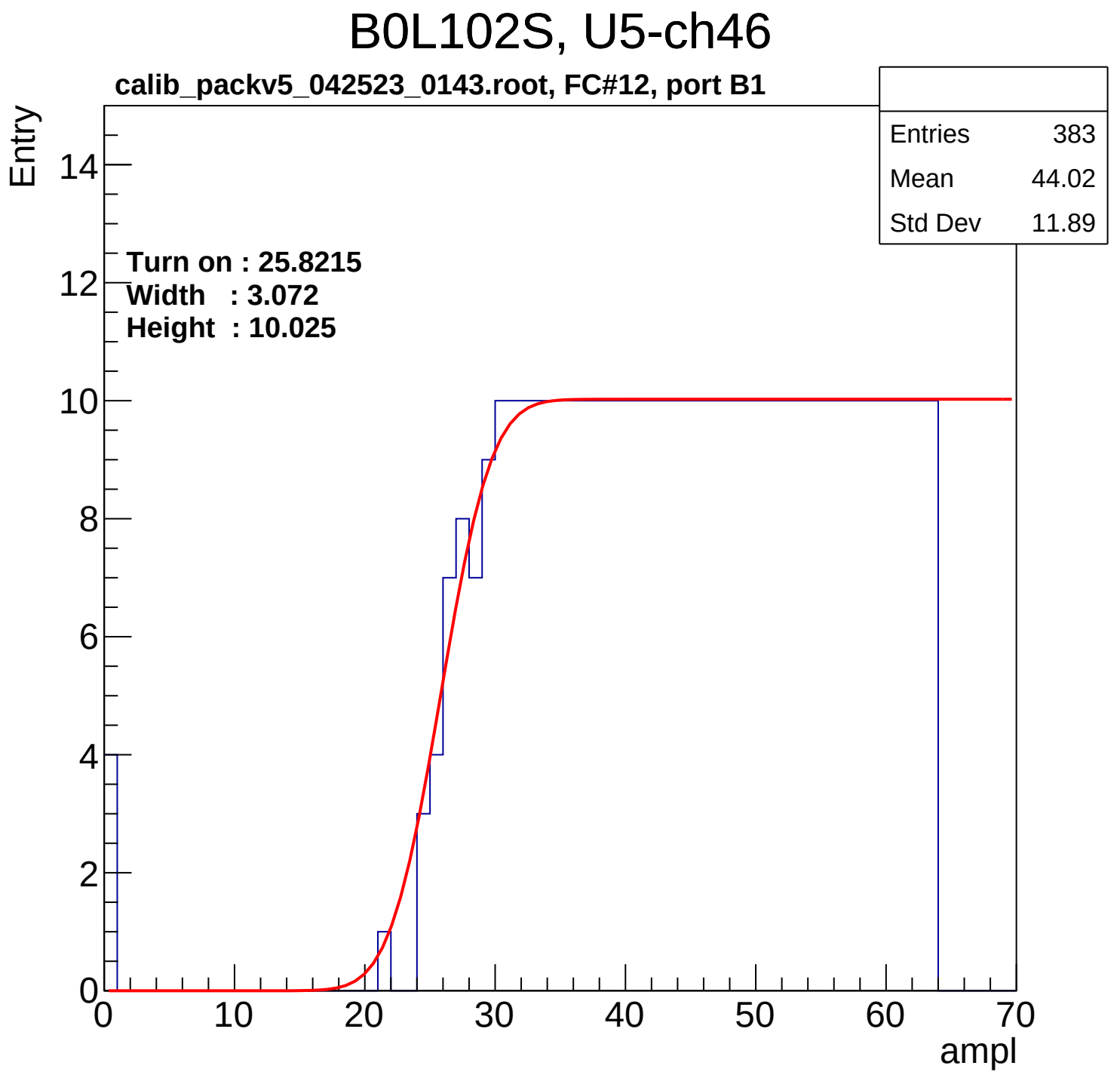
B0L102S, U5-ch46
calib_packv5_042523_0143.root, FC#12, port B1
Entries 383
Mean 44.02
Std Dev 11.89
Turn on : 25.8215
Width : 3.072
Height : 10.025
Entry
ampl
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4
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8
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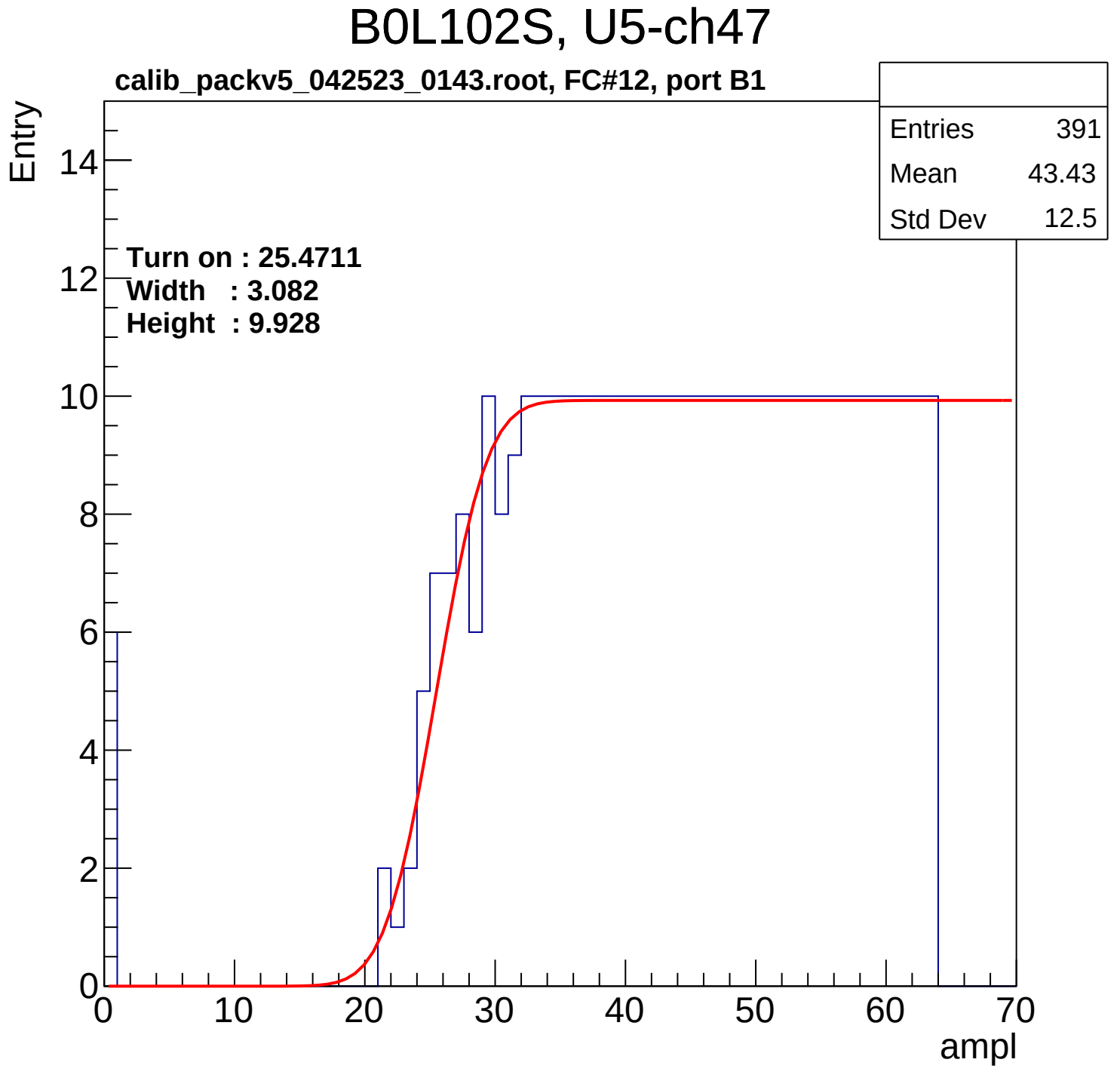
B0L102S, U5-ch47
calib_packv5_042523_0143.root, FC#12, port B1
Entries 391
Mean 43.43
Std Dev 12.5
Turn on : 25.4711
Width : 3.082
Height : 9.928
Entry
ampl
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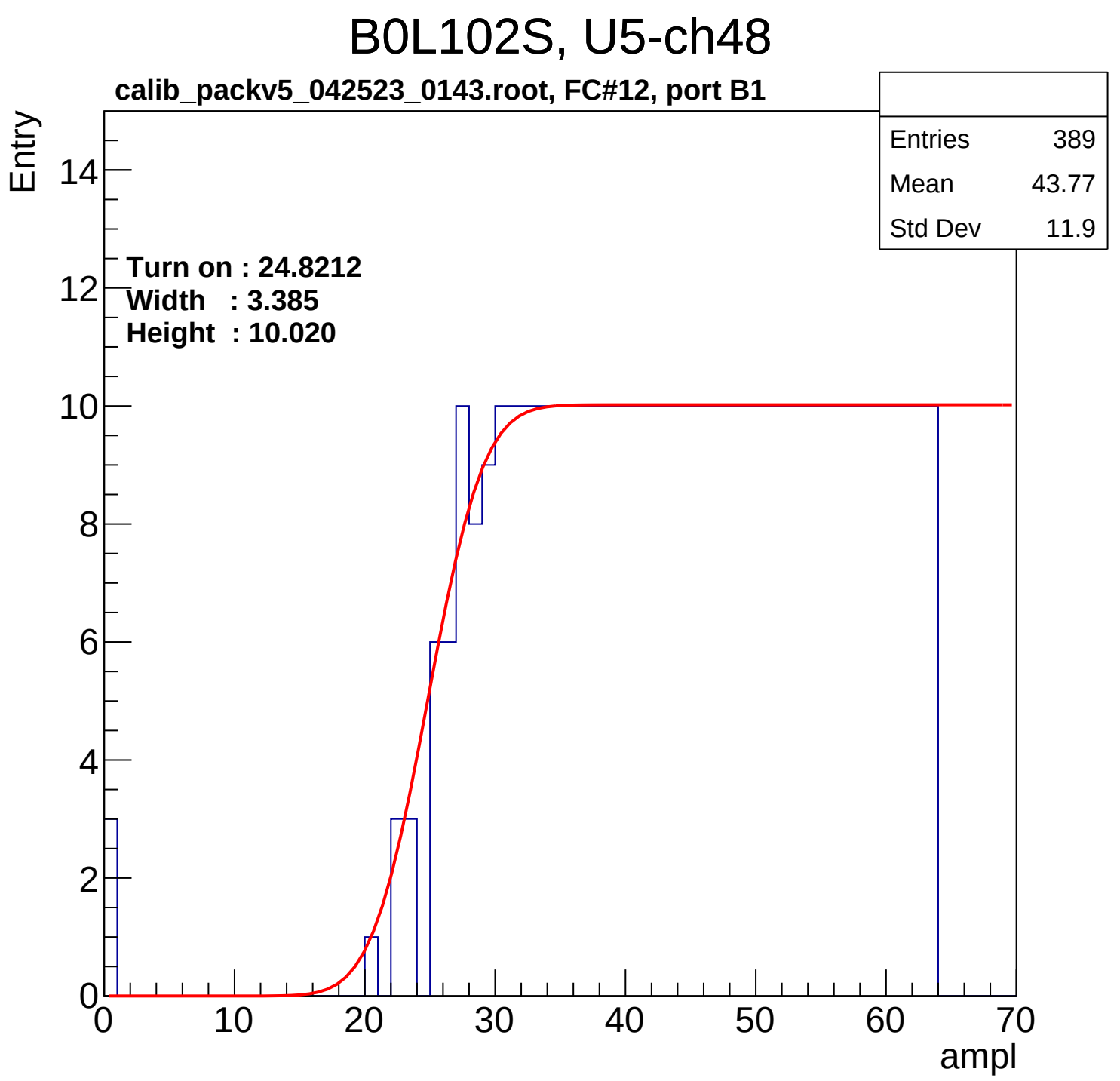
B0L102S, U5-ch48
calib_packv5_042523_0143.root, FC#12, port B1
Entries 389
Mean 43.77
Std Dev 11.9
Turn on : 24.8212
Width : 3.385
Height : 10.020
Entry
ampl
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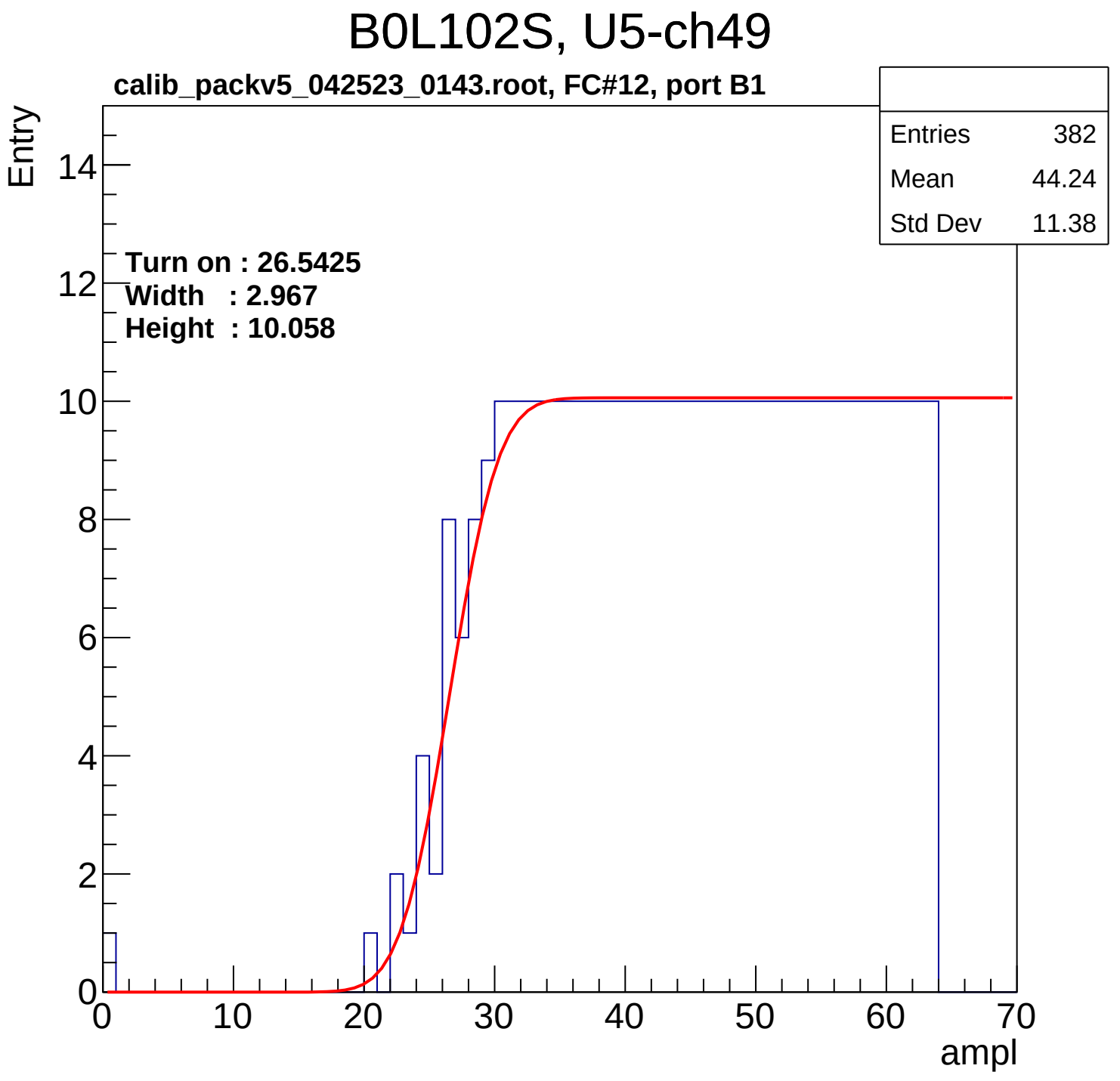
B0L102S, U5-ch49
calib_packv5_042523_0143.root, FC#12, port B1
Entries 382
Mean 44.24
Std Dev 11.38
Turn on : 26.5425
Width : 2.967
Height : 10.058
Entry
ampl
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6
8
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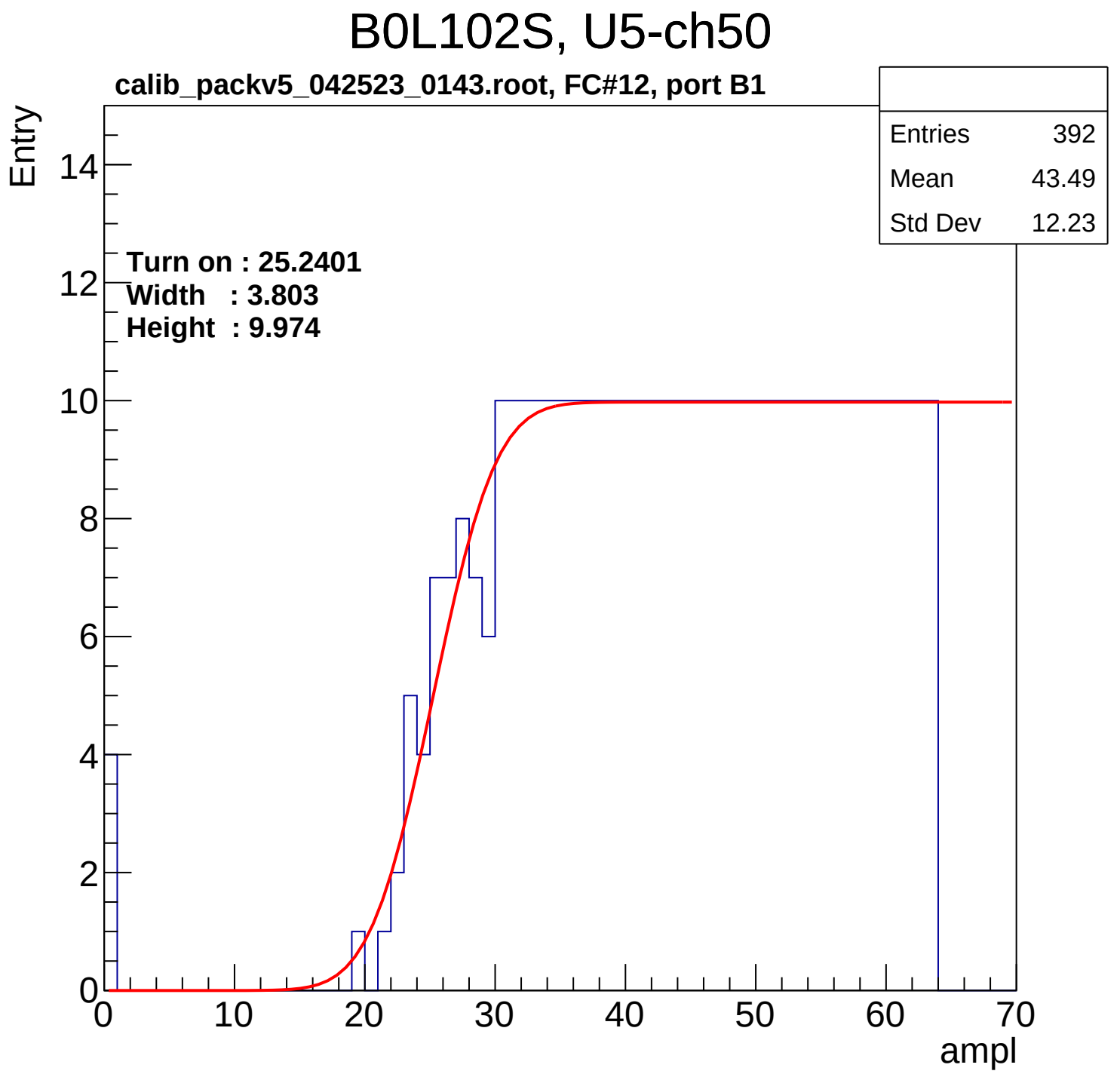
B0L102S, U5-ch50
calib_packv5_042523_0143.root, FC#12, port B1
Entries 392
Mean 43.49
Std Dev 12.23
Turn on : 25.2401
Width : 3.803
Height : 9.974
Entry
ampl
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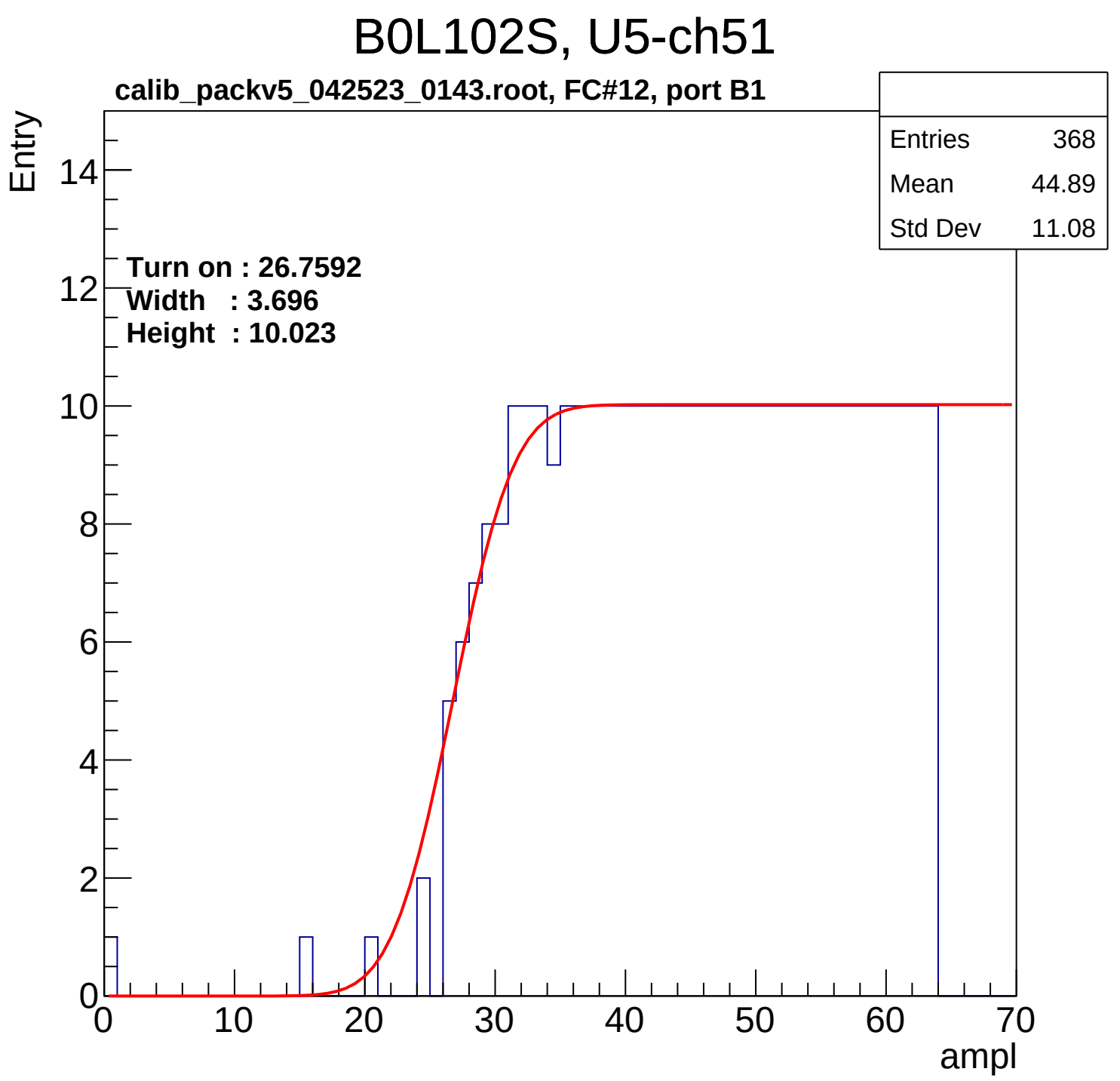
B0L102S, U5-ch51
calib_packv5_042523_0143.root, FC#12, port B1
Entries 368
Mean 44.89
Std Dev 11.08
Turn on : 26.7592
Width : 3.696
Height : 10.023
Entry
ampl
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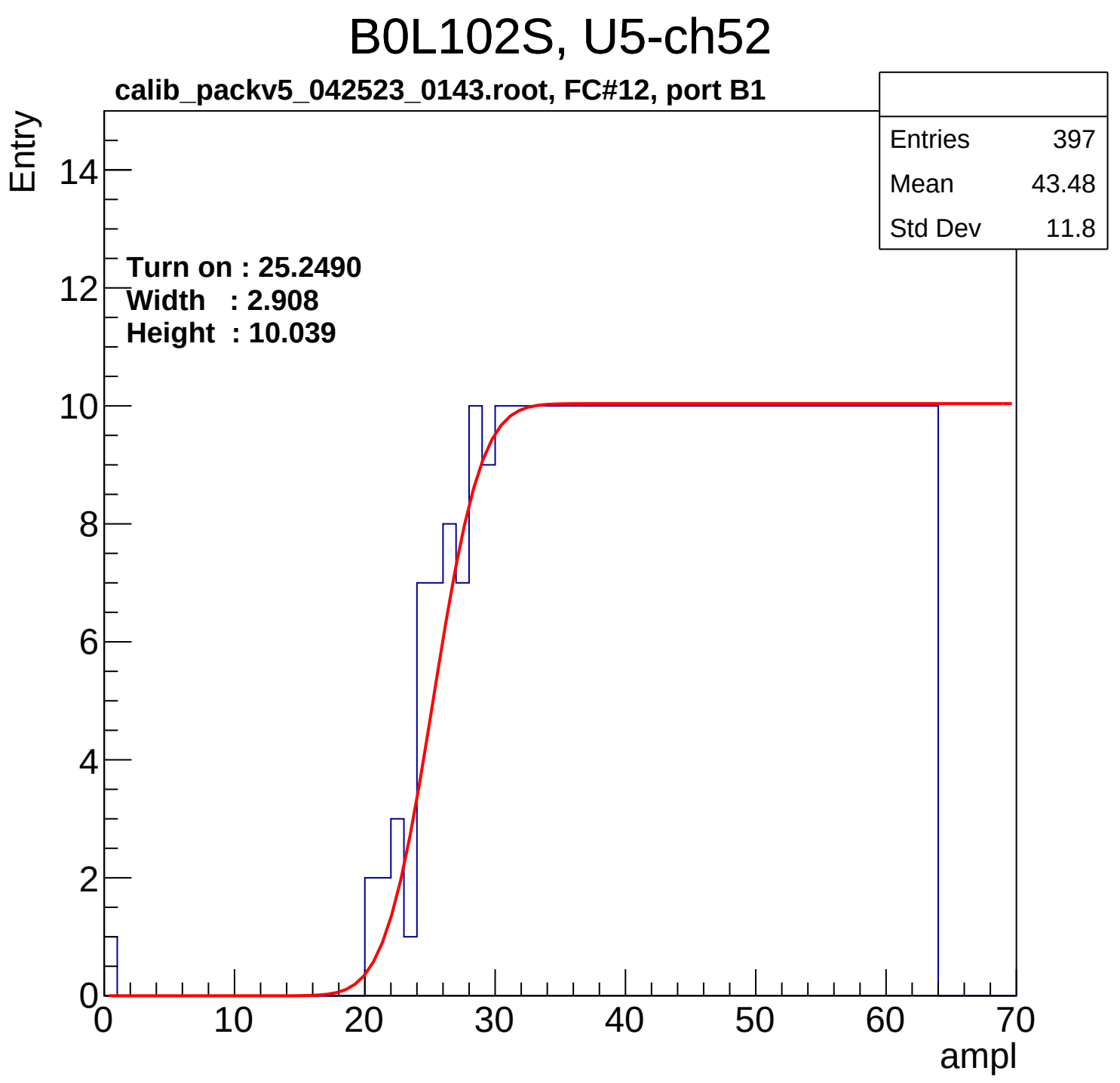
B0L102S, U5-ch52
calib_packv5_042523_0143.root, FC#12, port B1
Entries 397
Mean 43.48
Std Dev 11.8
Turn on : 25.2490
Width : 2.908
Height : 10.039
Entry
ampl
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2
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6
8
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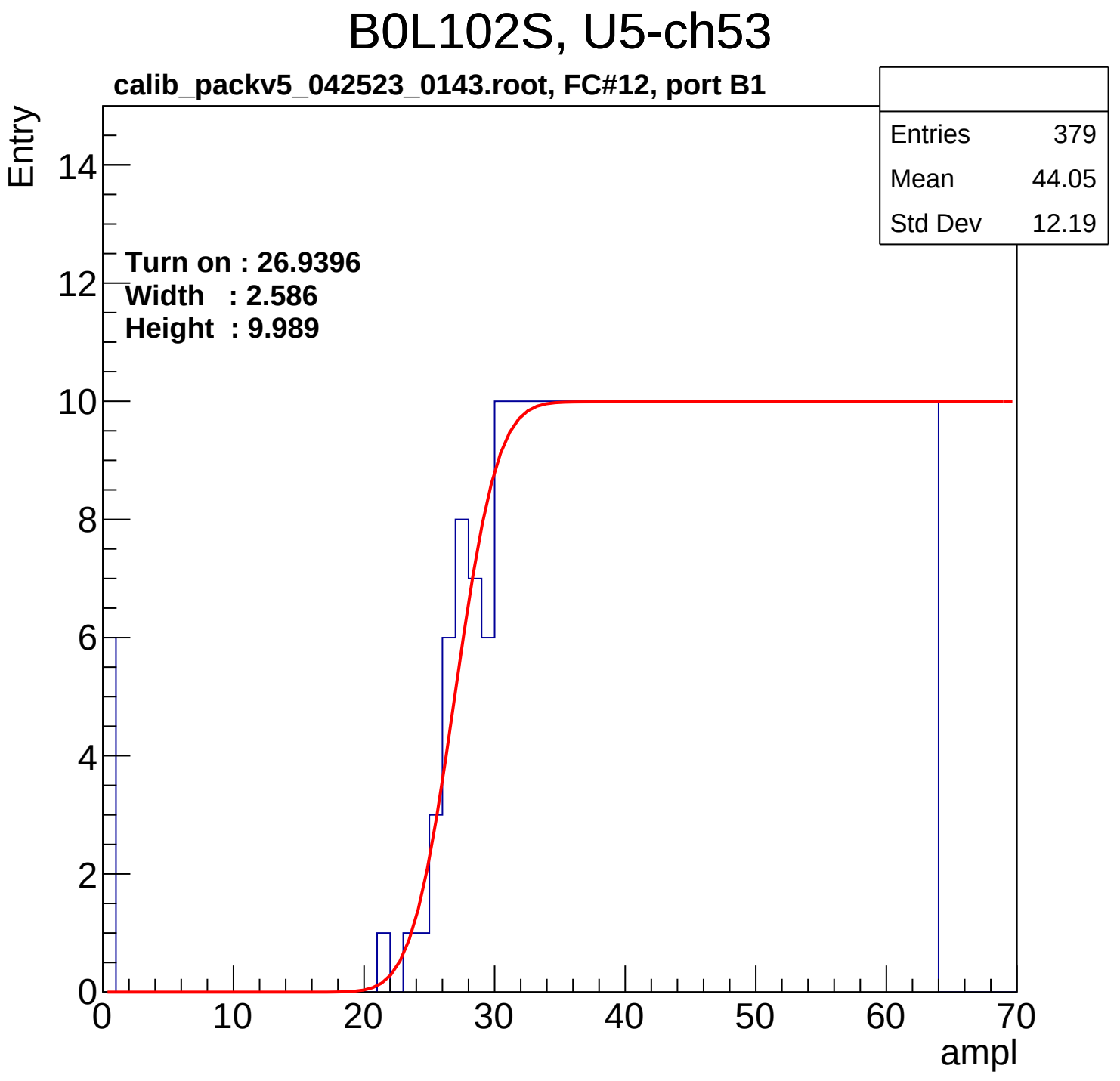
B0L102S, U5-ch53
calib_packv5_042523_0143.root, FC#12, port B1
Entries 379
Mean 44.05
Std Dev 12.19
Turn on : 26.9396
Width : 2.586
Height : 9.989
Entry
ampl
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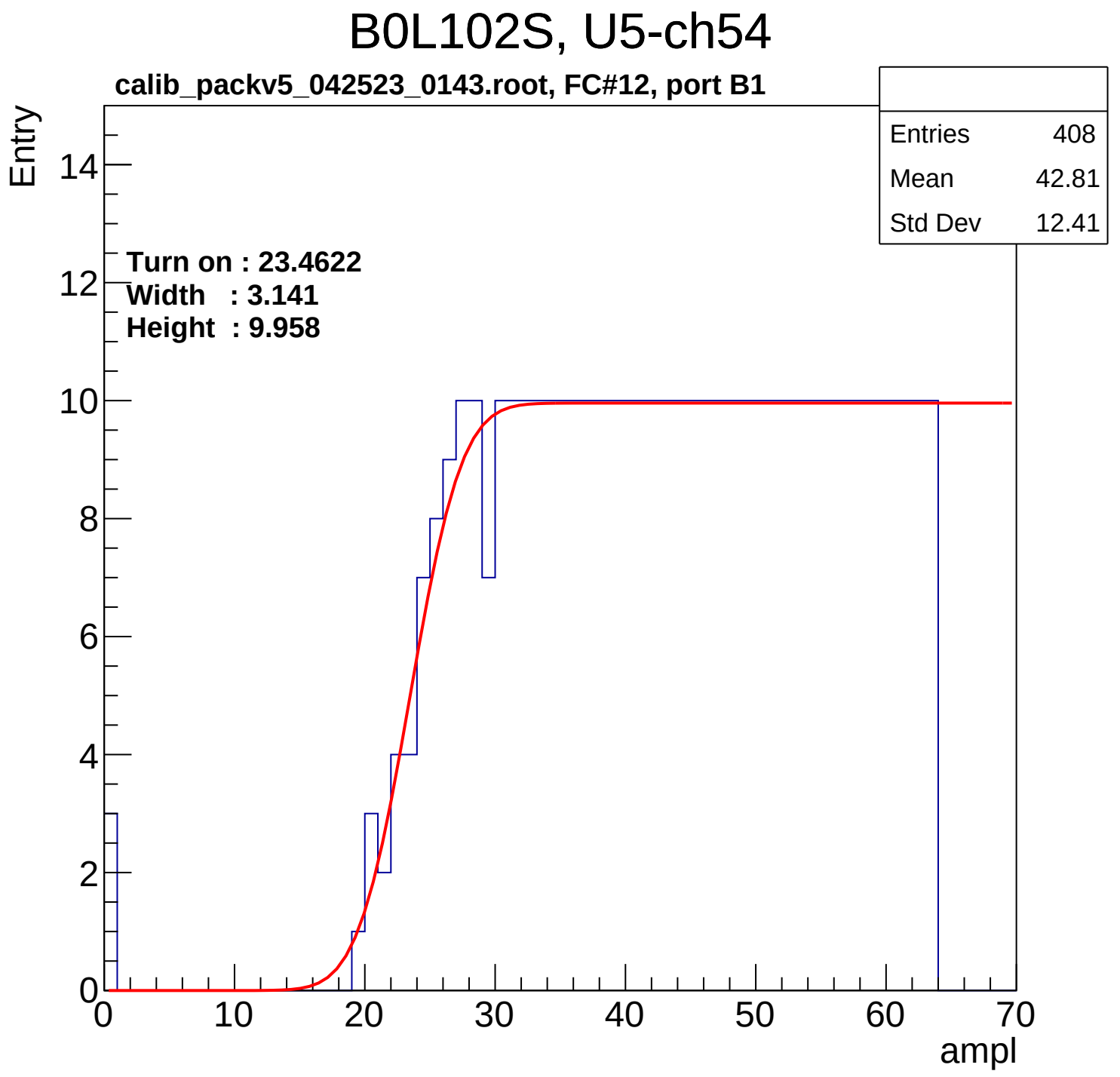
B0L102S, U5-ch54
calib_packv5_042523_0143.root, FC#12, port B1
Entries 408
Mean 42.81
Std Dev 12.41
Turn on : 23.4622
Width : 3.141
Height : 9.958
Entry
ampl
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4
6
8
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0
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60
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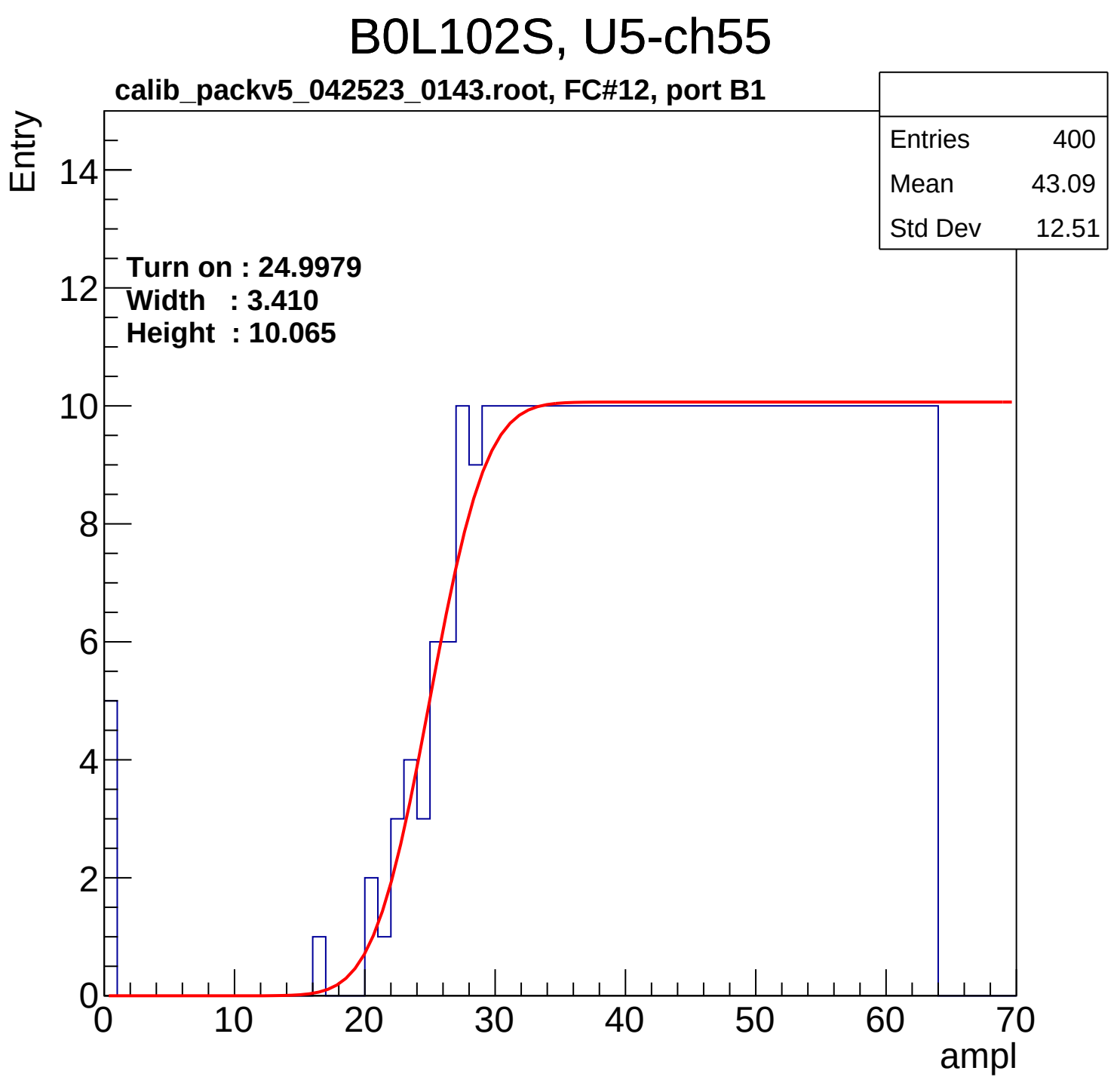
B0L102S, U5-ch55
calib_packv5_042523_0143.root, FC#12, port B1
Entries 400
Mean 43.09
Std Dev 12.51
Turn on : 24.9979
Width : 3.410
Height : 10.065
Entry
ampl
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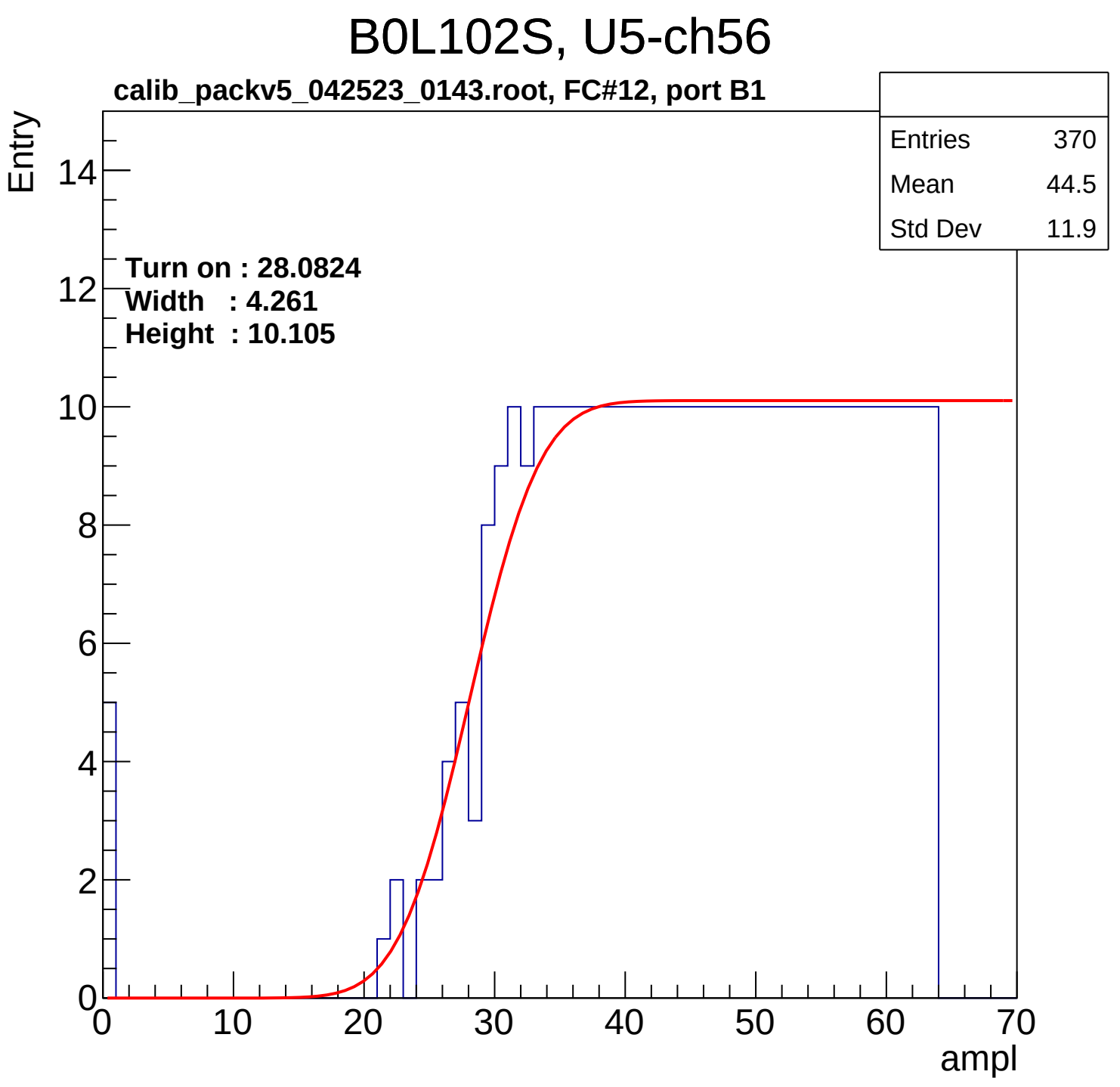
B0L102S, U5-ch56
calib_packv5_042523_0143.root, FC#12, port B1
Entries 370
Mean 44.5
Std Dev 11.9
Turn on : 28.0824
Width : 4.261
Height : 10.105
Entry
ampl
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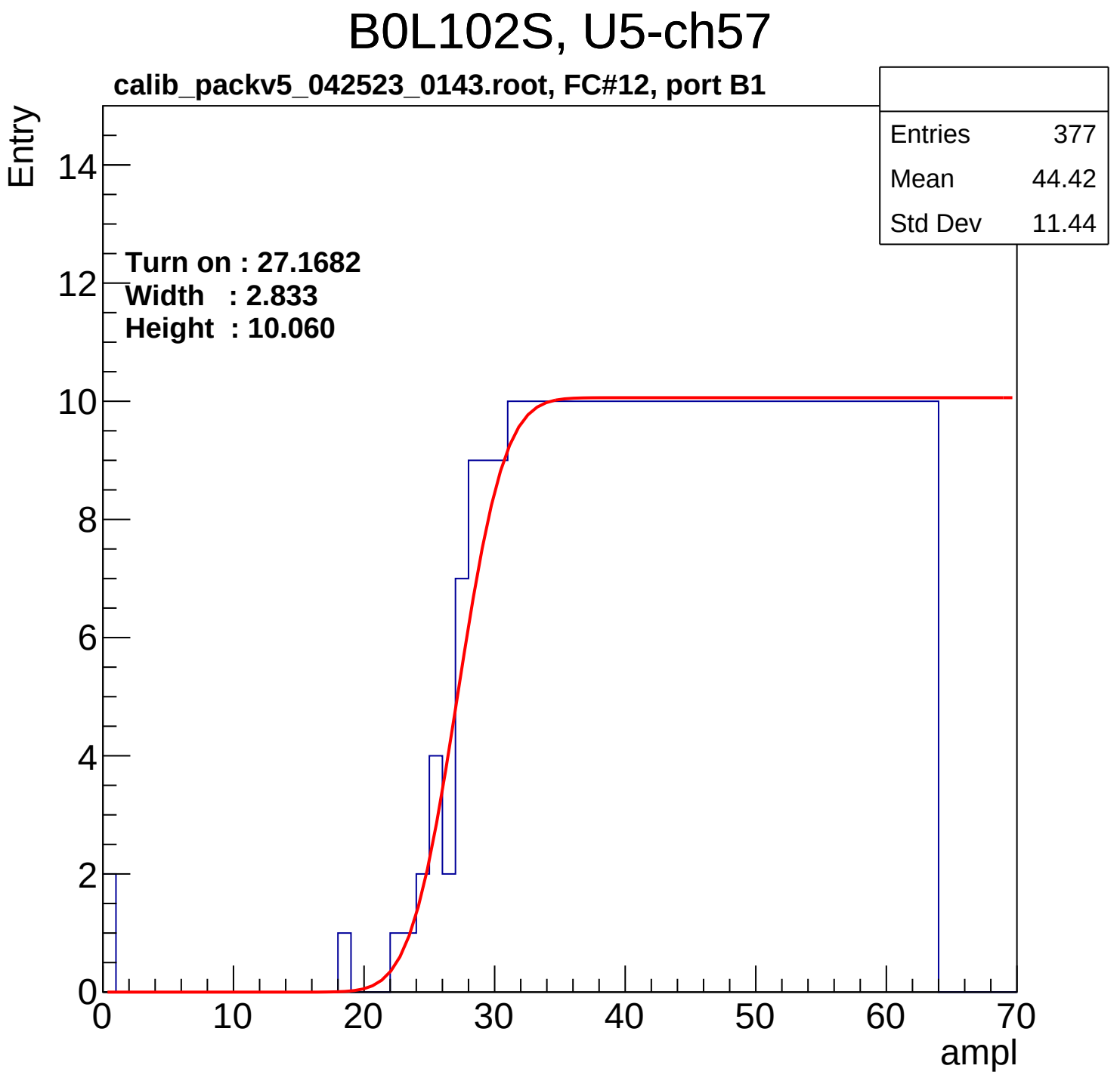
B0L102S, U5-ch57
calib_packv5_042523_0143.root, FC#12, port B1
Entries 377
Mean 44.42
Std Dev 11.44
Turn on : 27.1682
Width : 2.833
Height : 10.060
Entry
ampl
0
2
4
6
8
10
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10
20
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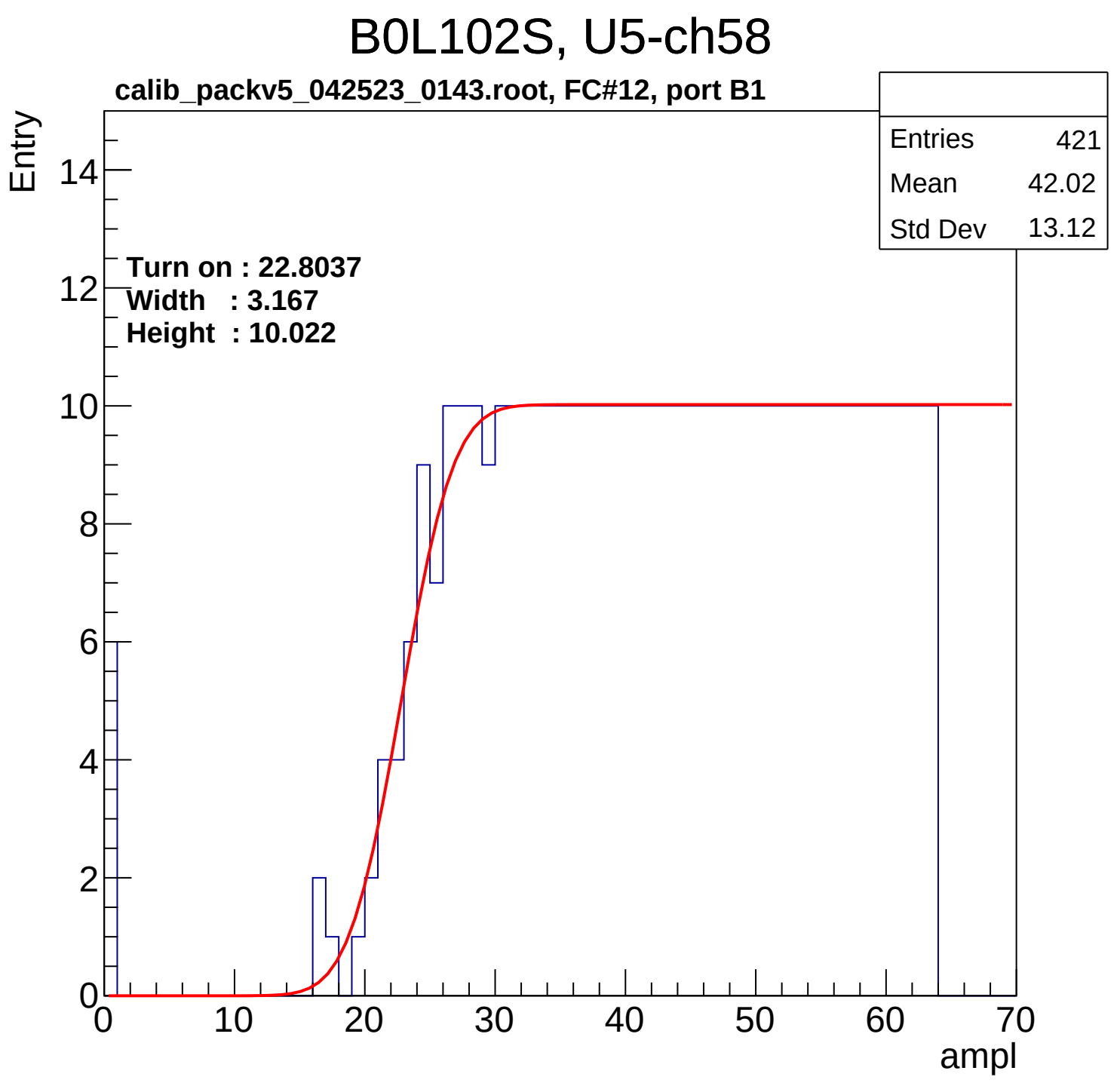
B0L102S, U5-ch58
calib_packv5_042523_0143.root, FC#12, port B1
Entries 421
Mean 42.02
Std Dev 13.12
Turn on : 22.8037
Width : 3.167
Height : 10.022
Entry
ampl
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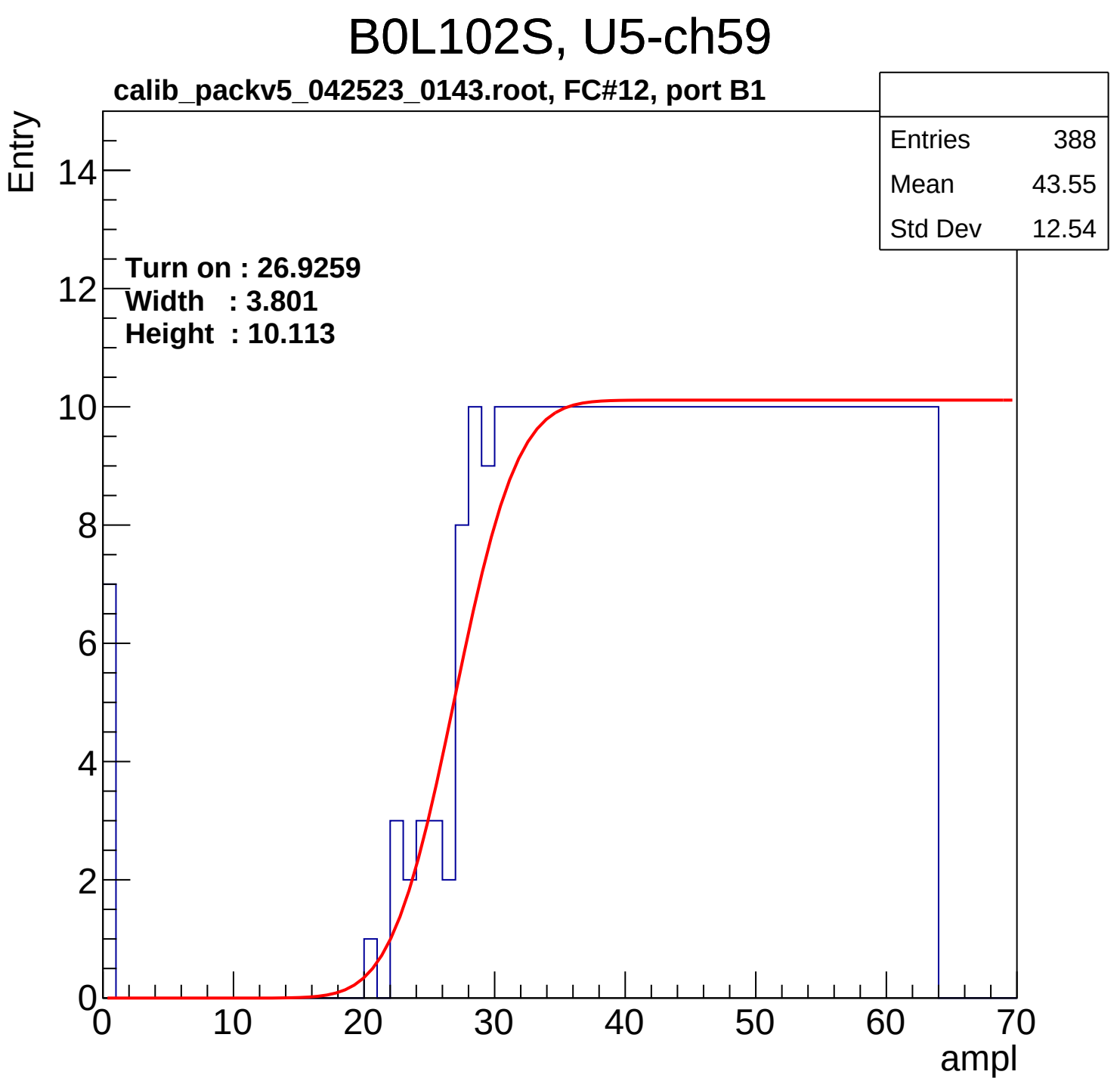
B0L102S, U5-ch59
calib_packv5_042523_0143.root, FC#12, port B1
Entries 388
Mean 43.55
Std Dev 12.54
Turn on : 26.9259
Width : 3.801
Height : 10.113
Entry
ampl
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2
4
6
8
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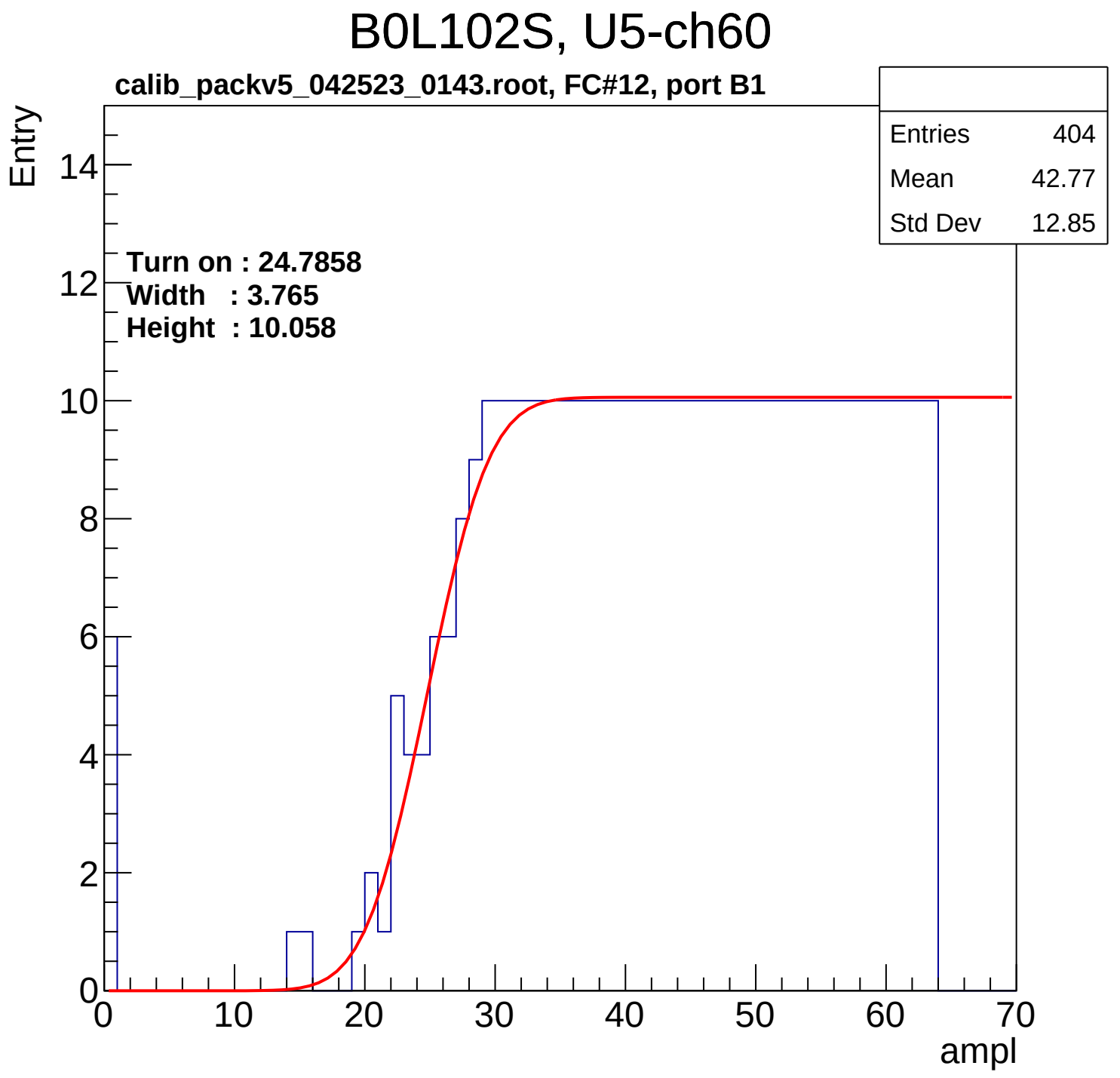
B0L102S, U5-ch60
calib_packv5_042523_0143.root, FC#12, port B1
Entries 404
Mean 42.77
Std Dev 12.85
Turn on : 24.7858
Width : 3.765
Height : 10.058
Entry
ampl
0
2
4
6
8
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0
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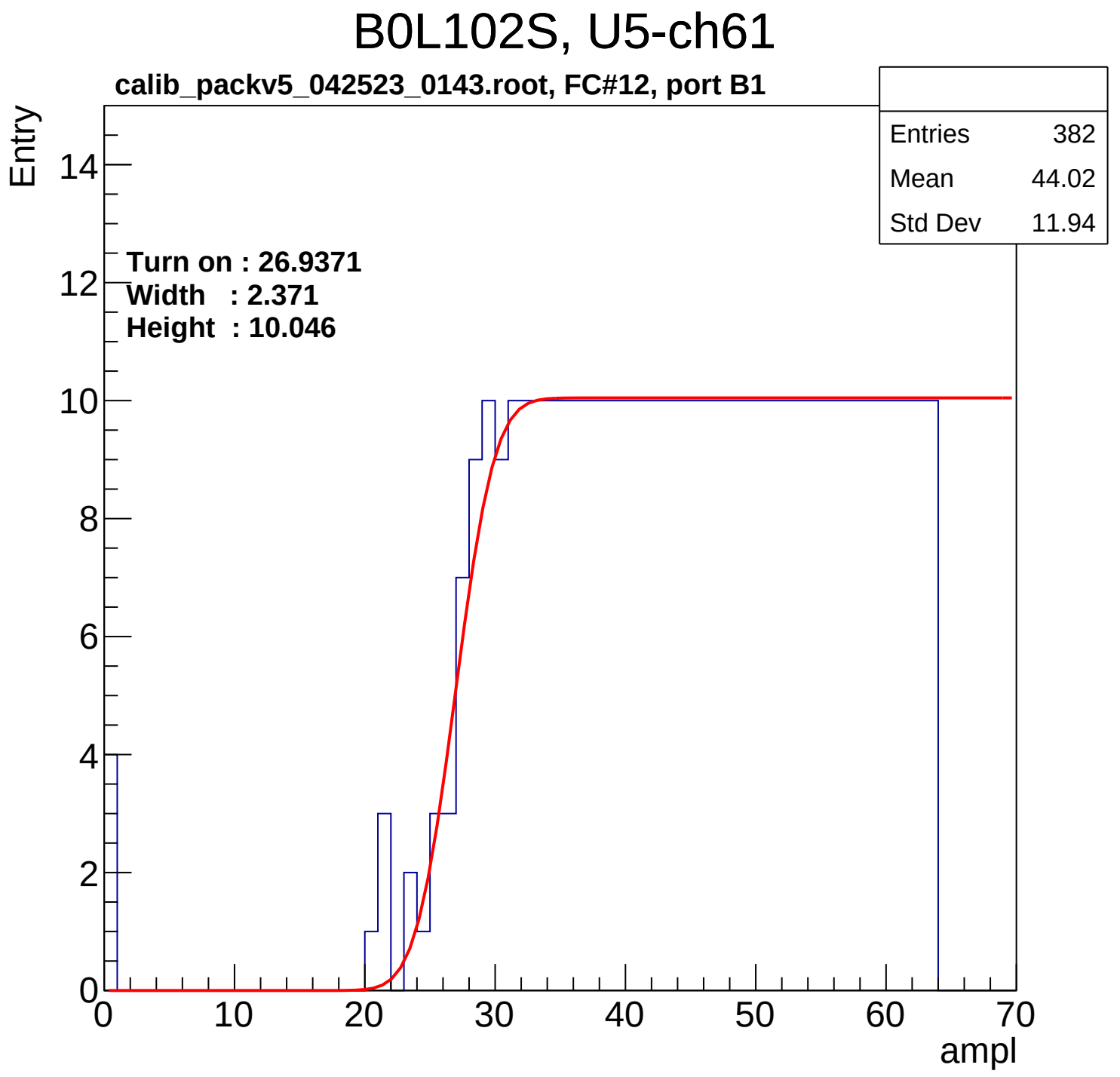
B0L102S, U5-ch61
calib_packv5_042523_0143.root, FC#12, port B1
Entries 382
Mean 44.02
Std Dev 11.94
Turn on : 26.9371
Width : 2.371
Height : 10.046
Entry
ampl
0
2
4
6
8
10
12
14
0
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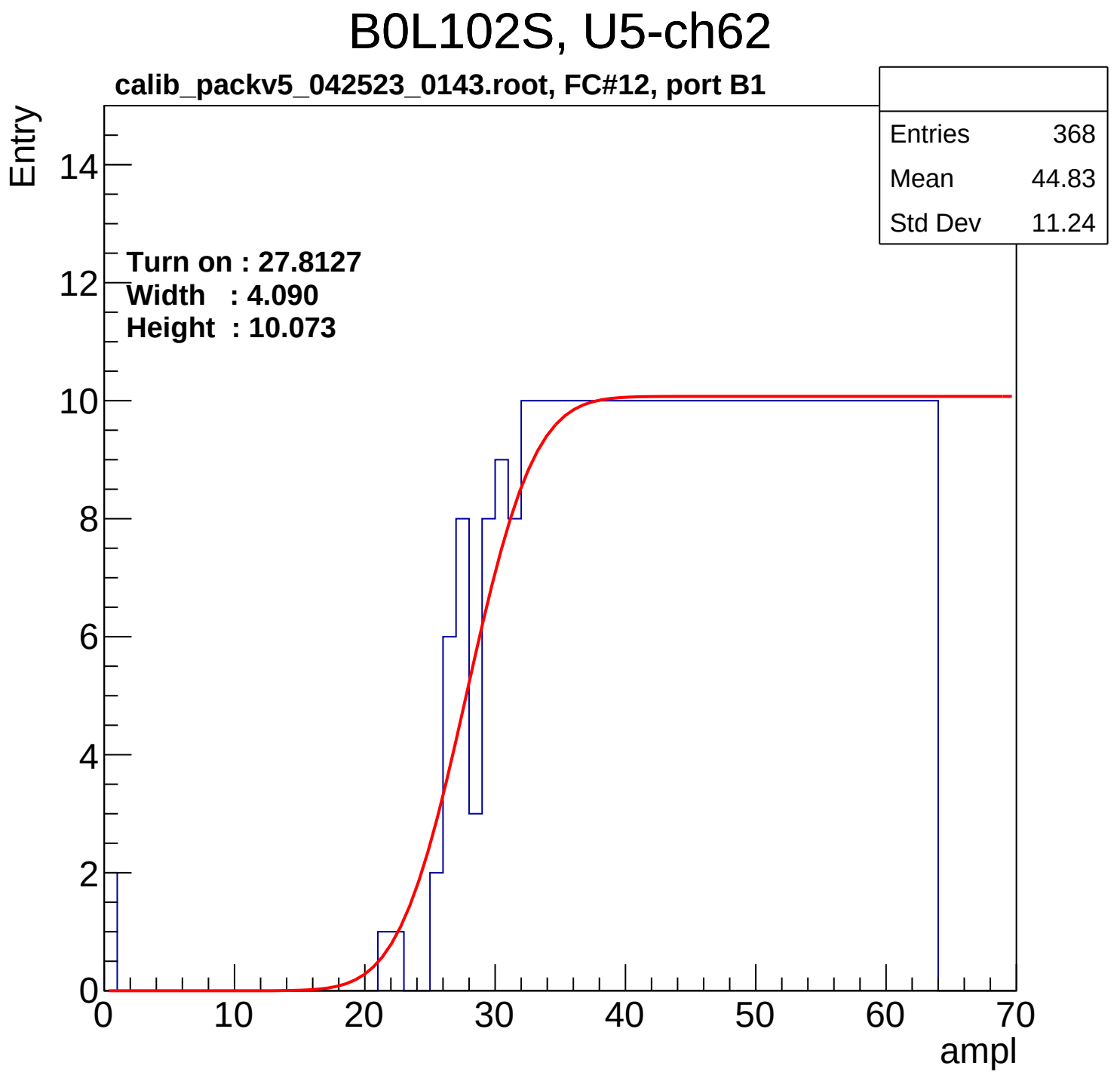
B0L102S, U5-ch62
calib_packv5_042523_0143.root, FC#12, port B1
Entries 368
Mean 44.83
Std Dev 11.24
Turn on : 27.8127
Width : 4.090
Height : 10.073
Entry
ampl
0
2
4
6
8
10
12
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0
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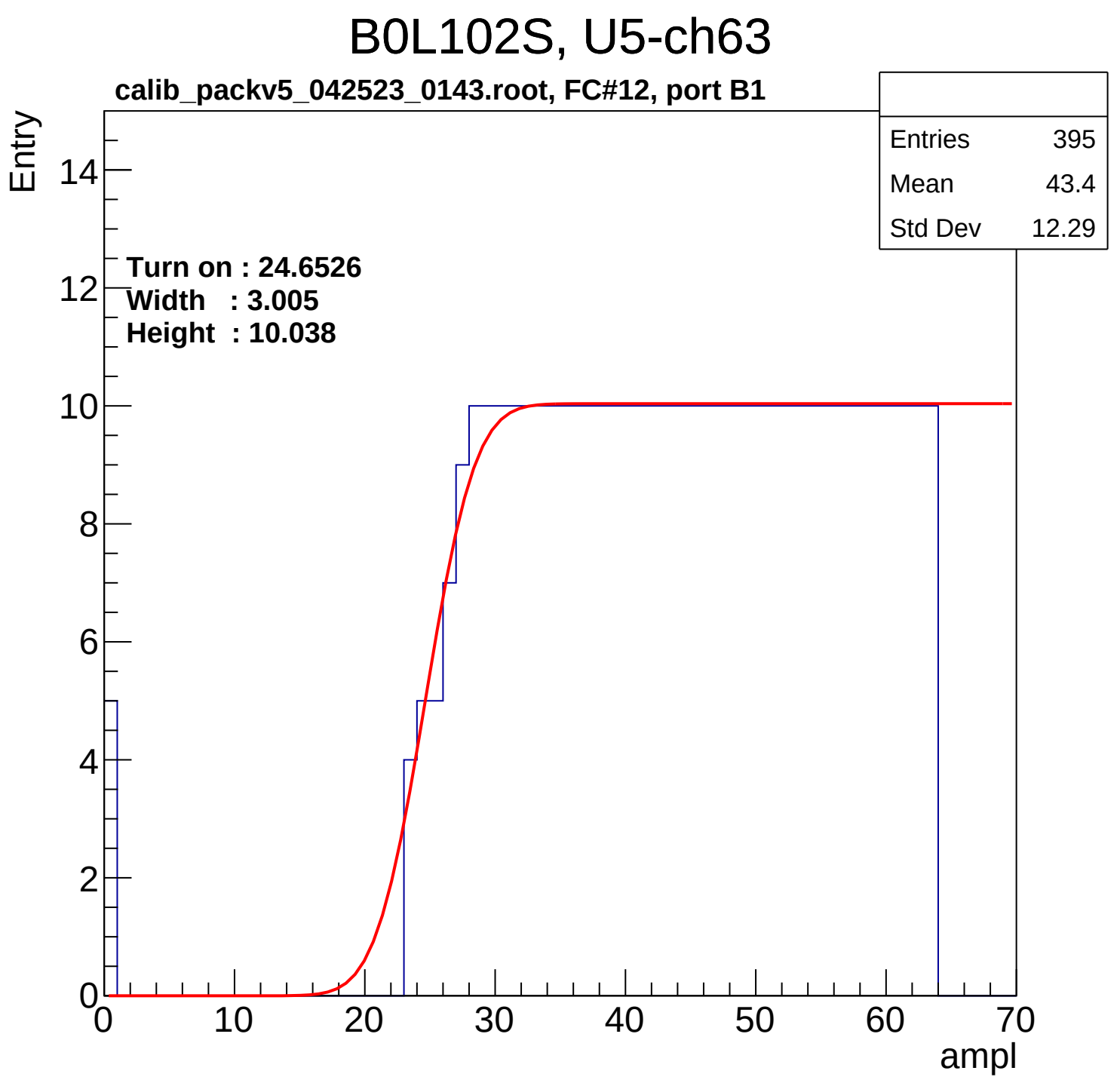
B0L102S, U5-ch63
calib_packv5_042523_0143.root, FC#12, port B1
Entries 395
Mean 43.4
Std Dev 12.29
Turn on : 24.6526
Width : 3.005
Height : 10.038
Entry
ampl
0
2
4
6
8
10
12
14
0
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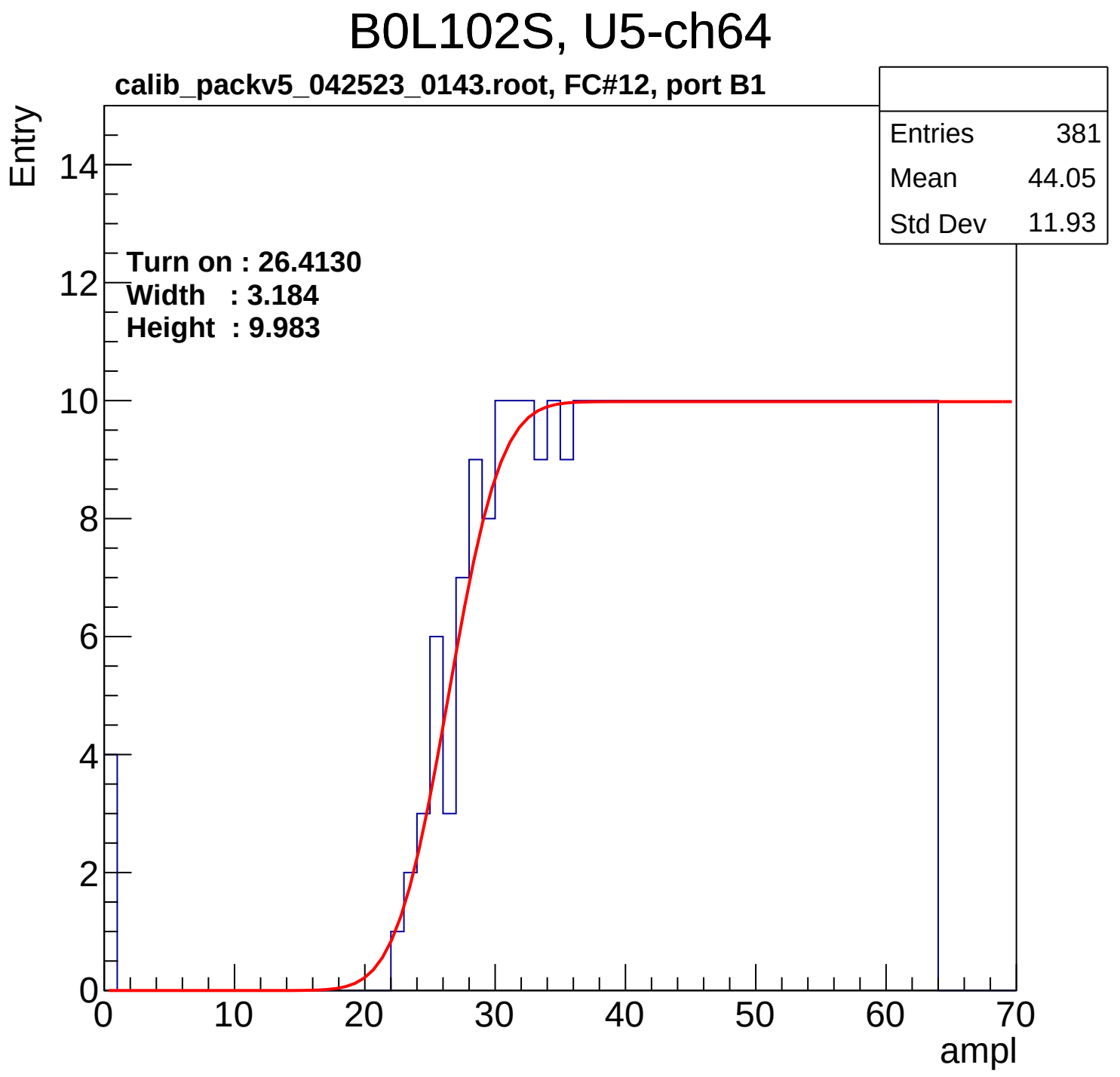
B0L102S, U5-ch64
calib_packv5_042523_0143.root, FC#12, port B1
Entries 381
Mean 44.05
Std Dev 11.93
Turn on : 26.4130
Width : 3.184
Height : 9.983
Entry
ampl
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4
6
8
10
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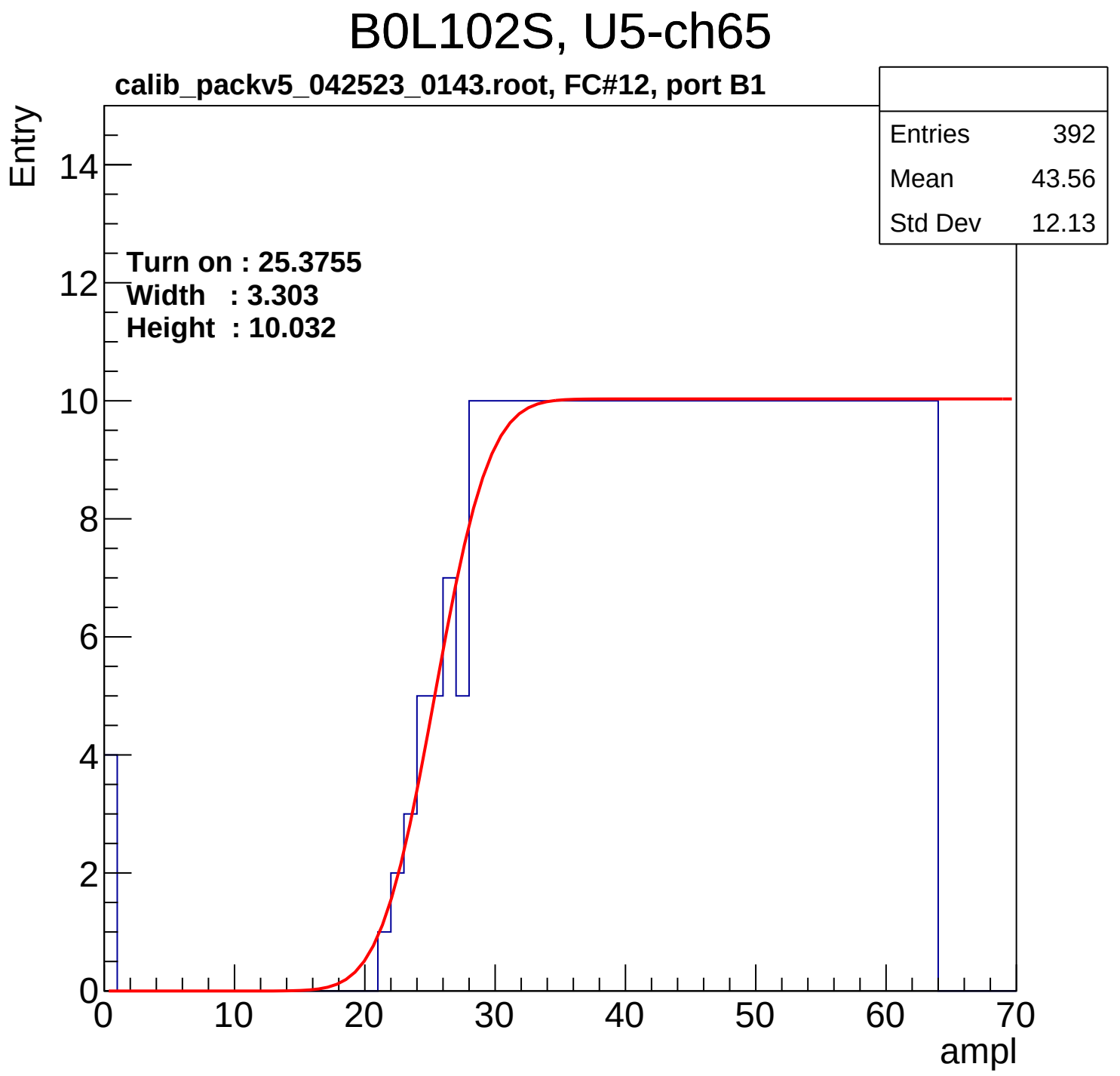
B0L102S, U5-ch65
calib_packv5_042523_0143.root, FC#12, port B1
Entries 392
Mean 43.56
Std Dev 12.13
Turn on : 25.3755
Width : 3.303
Height : 10.032
Entry
ampl
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2
4
6
8
10
12
14
0
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40
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60
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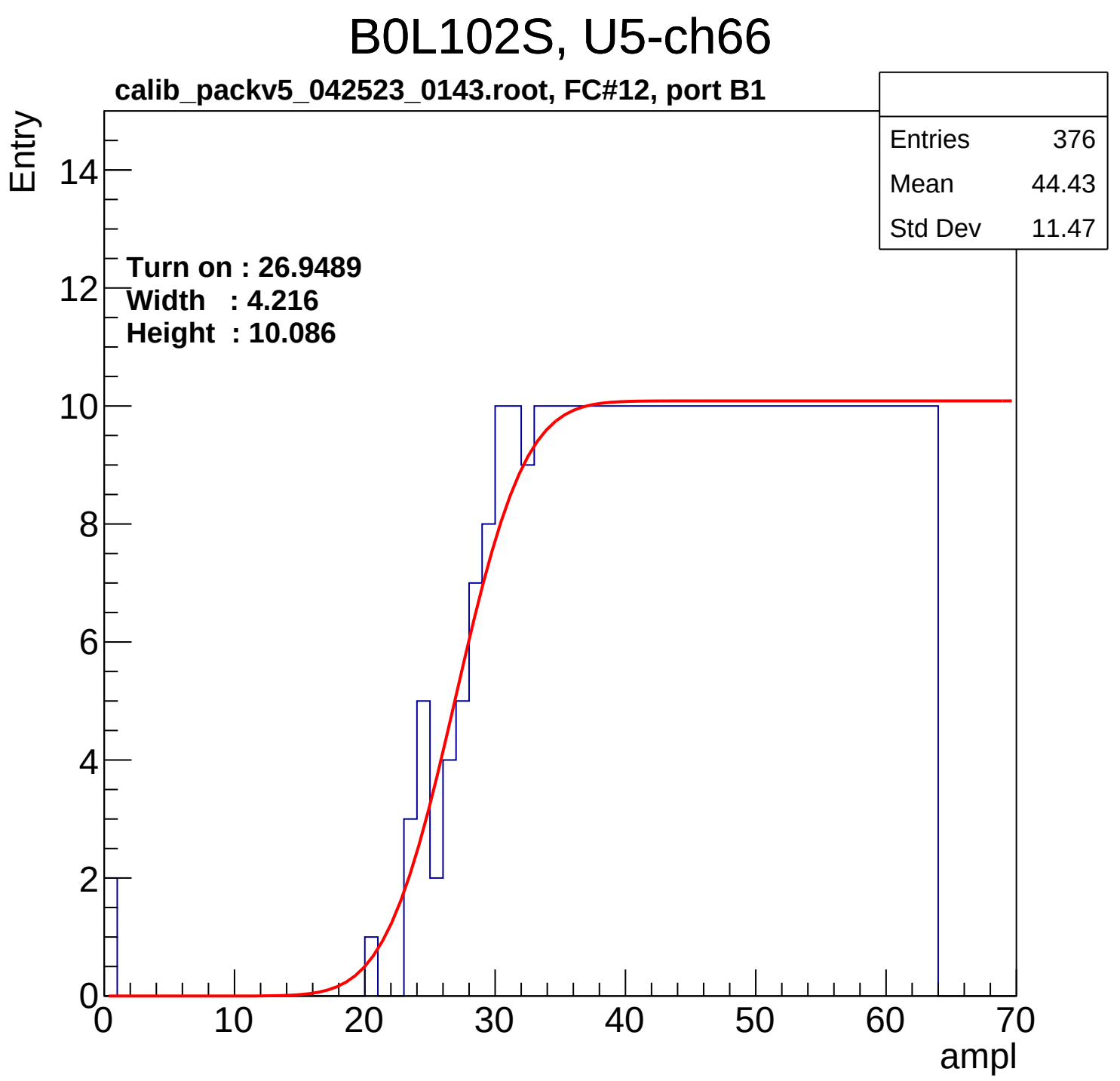
B0L102S, U5-ch66
calib_packv5_042523_0143.root, FC#12, port B1
Entries 376
Mean 44.43
Std Dev 11.47
Turn on : 26.9489
Width : 4.216
Height : 10.086
Entry
ampl
0
2
4
6
8
10
12
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0
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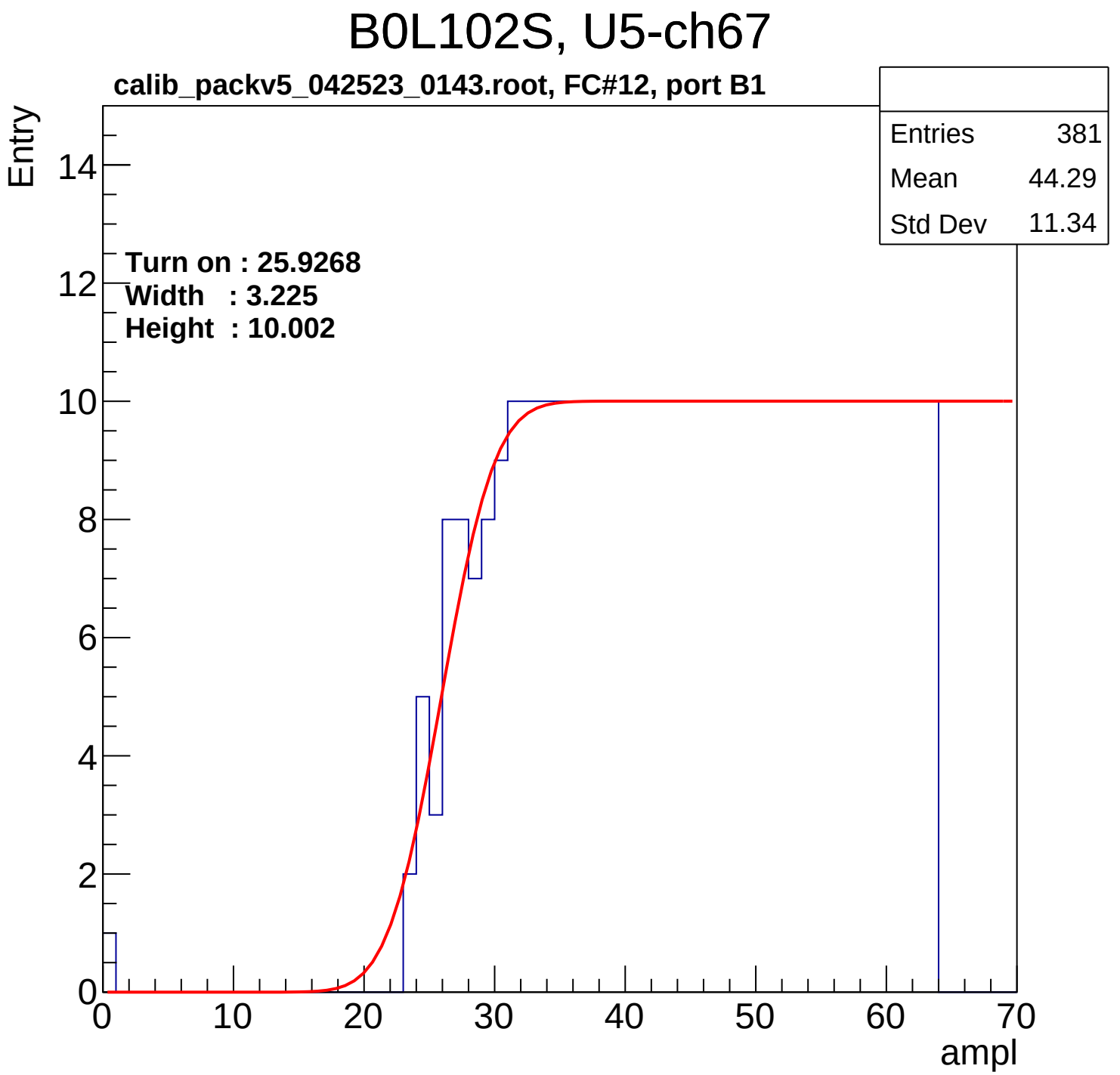
B0L102S, U5-ch67
calib_packv5_042523_0143.root, FC#12, port B1
Entries 381
Mean 44.29
Std Dev 11.34
Turn on : 25.9268
Width : 3.225
Height : 10.002
Entry
ampl
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2
4
6
8
10
12
14
0
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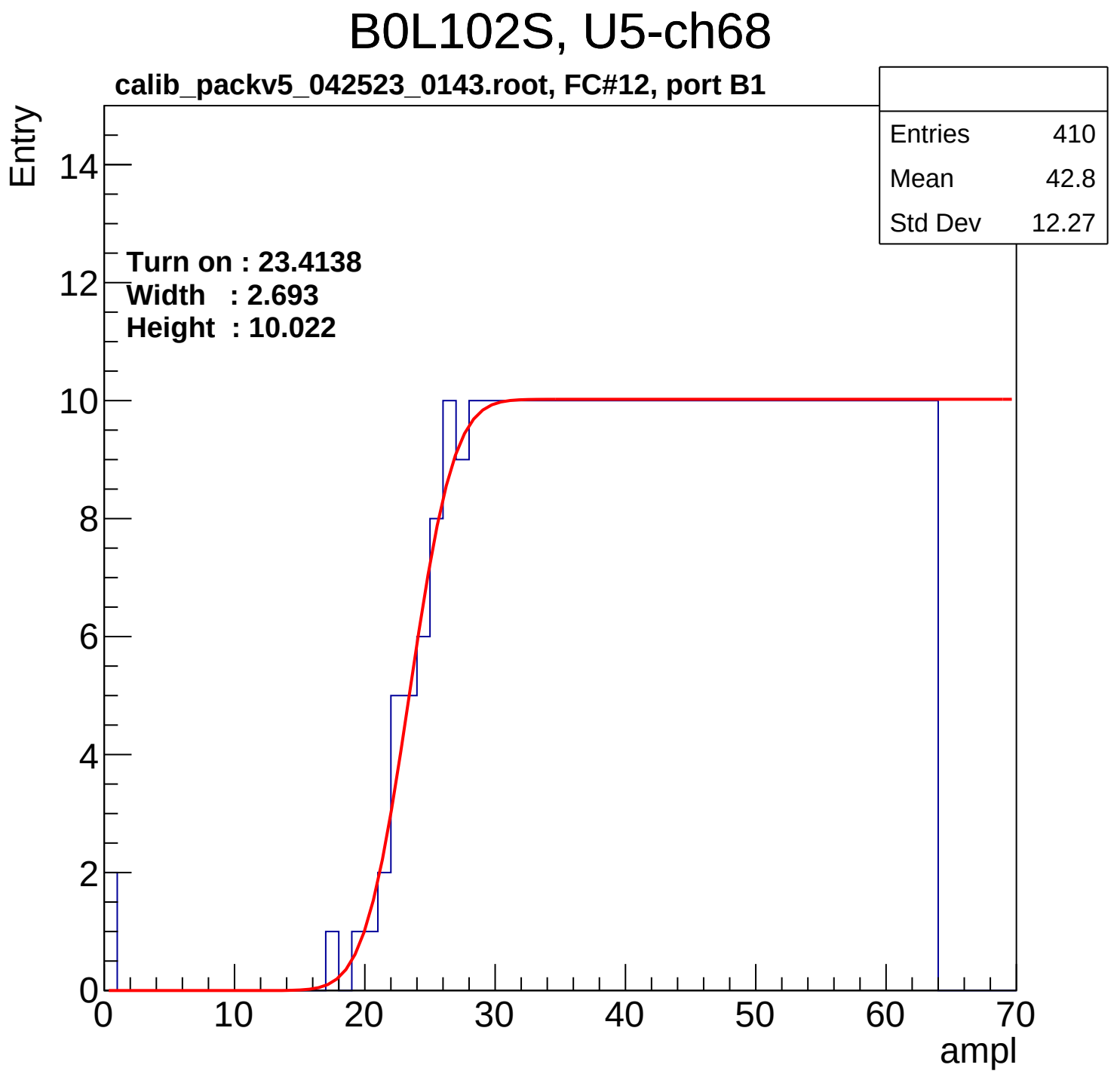
B0L102S, U5-ch68
calib_packv5_042523_0143.root, FC#12, port B1
Entries 410
Mean 42.8
Std Dev 12.27
Turn on : 23.4138
Width : 2.693
Height : 10.022
Entry
ampl
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2
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6
8
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12
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0
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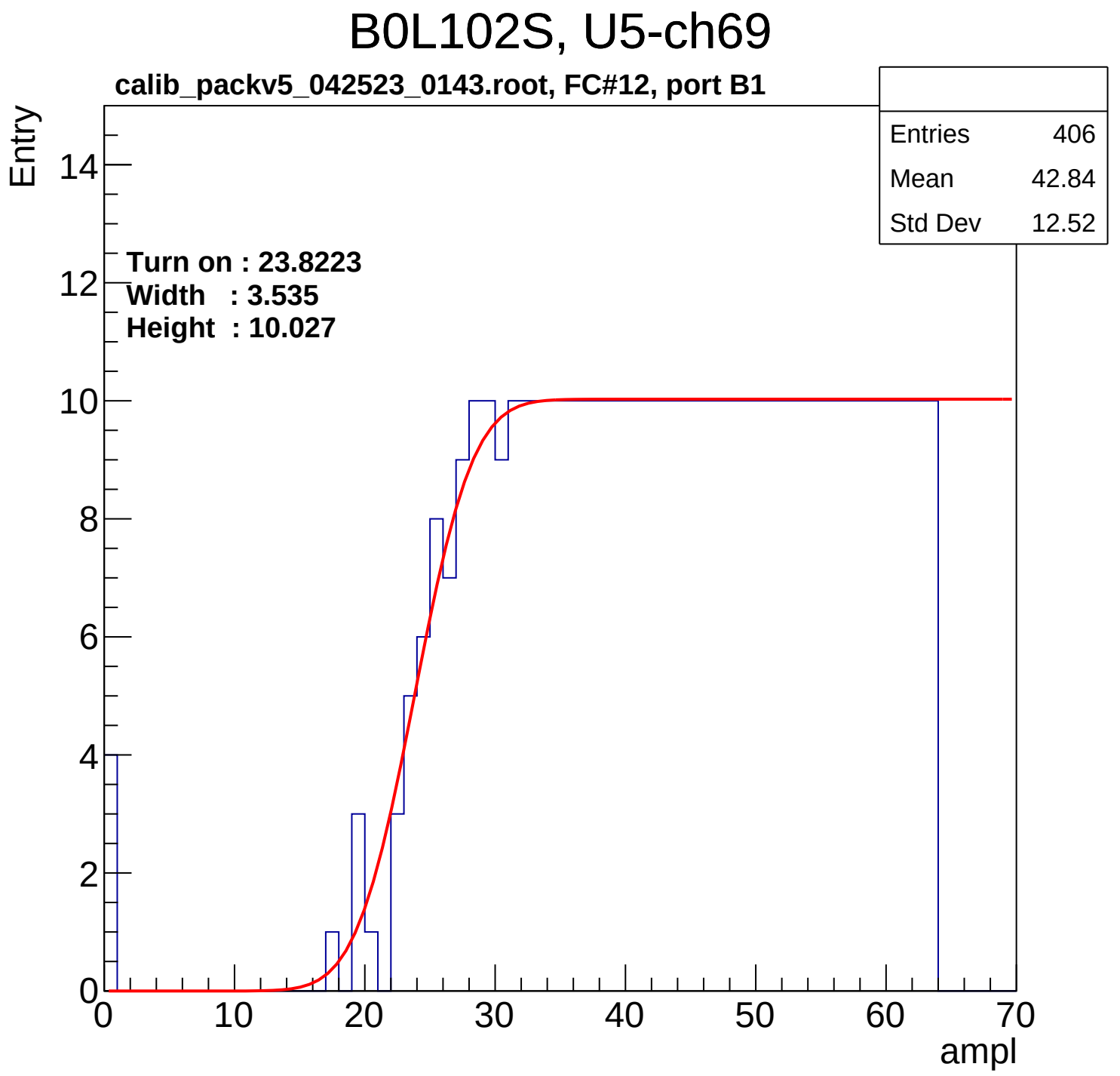
B0L102S, U5-ch69
calib_packv5_042523_0143.root, FC#12, port B1
Entries 406
Mean 42.84
Std Dev 12.52
Turn on : 23.8223
Width : 3.535
Height : 10.027
Entry
ampl
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6
8
10
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0
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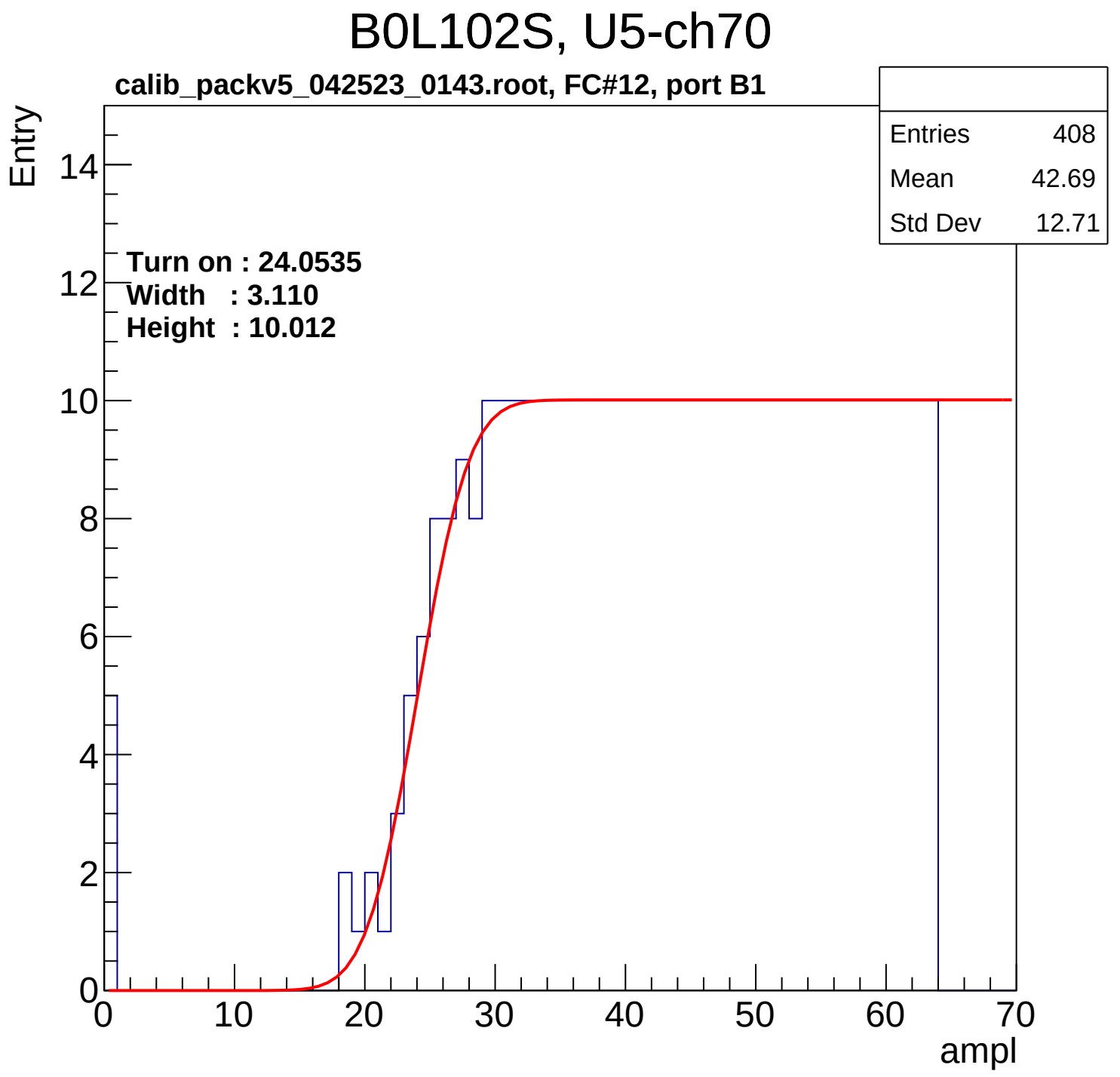
B0L102S, U5-ch70
calib_packv5_042523_0143.root, FC#12, port B1
Entries 408
Mean 42.69
Std Dev 12.71
Turn on : 24.0535
Width : 3.110
Height : 10.012
Entry
ampl
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6
8
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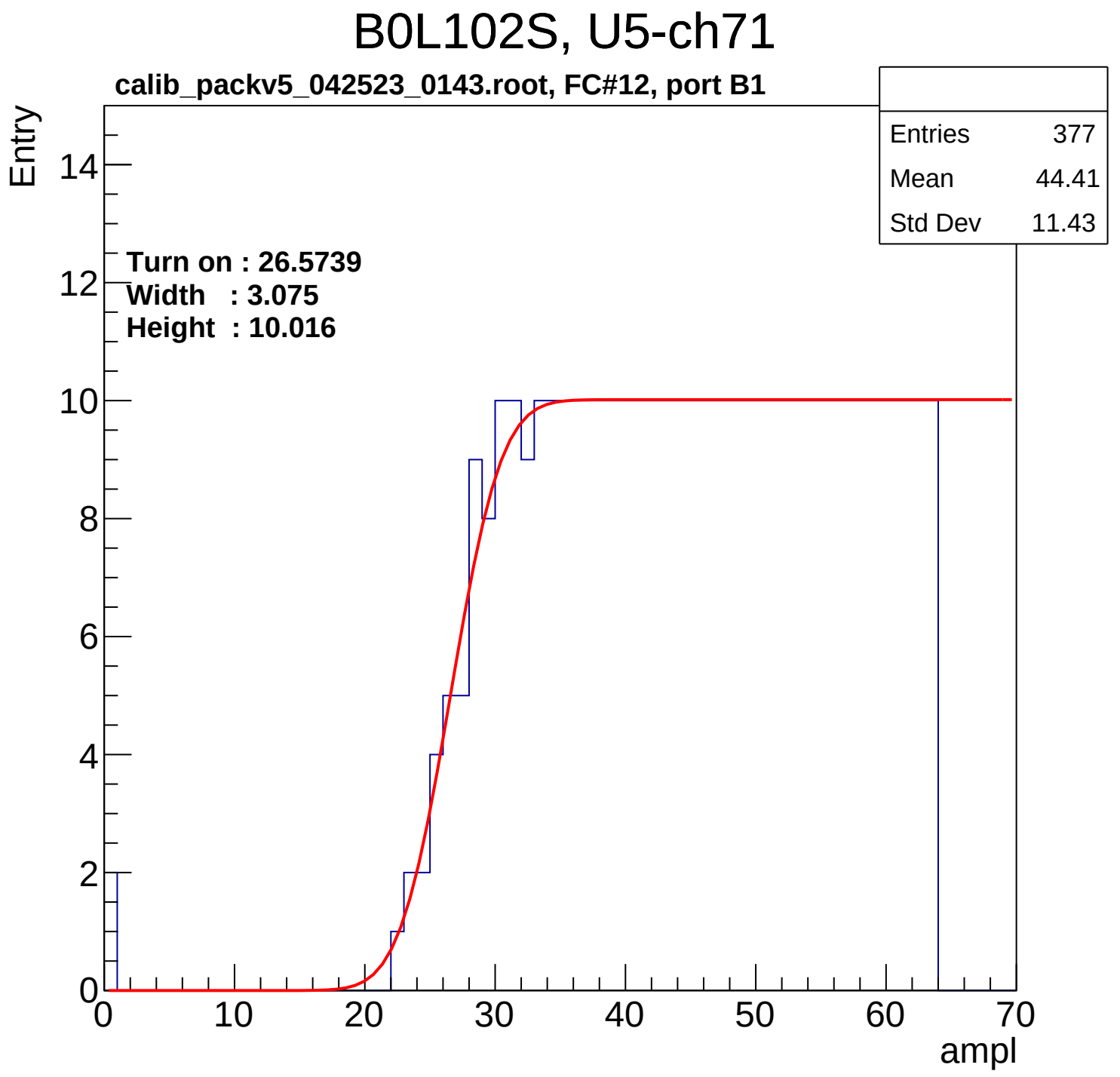
B0L102S, U5-ch71
calib_packv5_042523_0143.root, FC#12, port B1
Entries 377
Mean 44.41
Std Dev 11.43
Turn on : 26.5739
Width : 3.075
Height : 10.016
Entry
ampl
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6
8
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0
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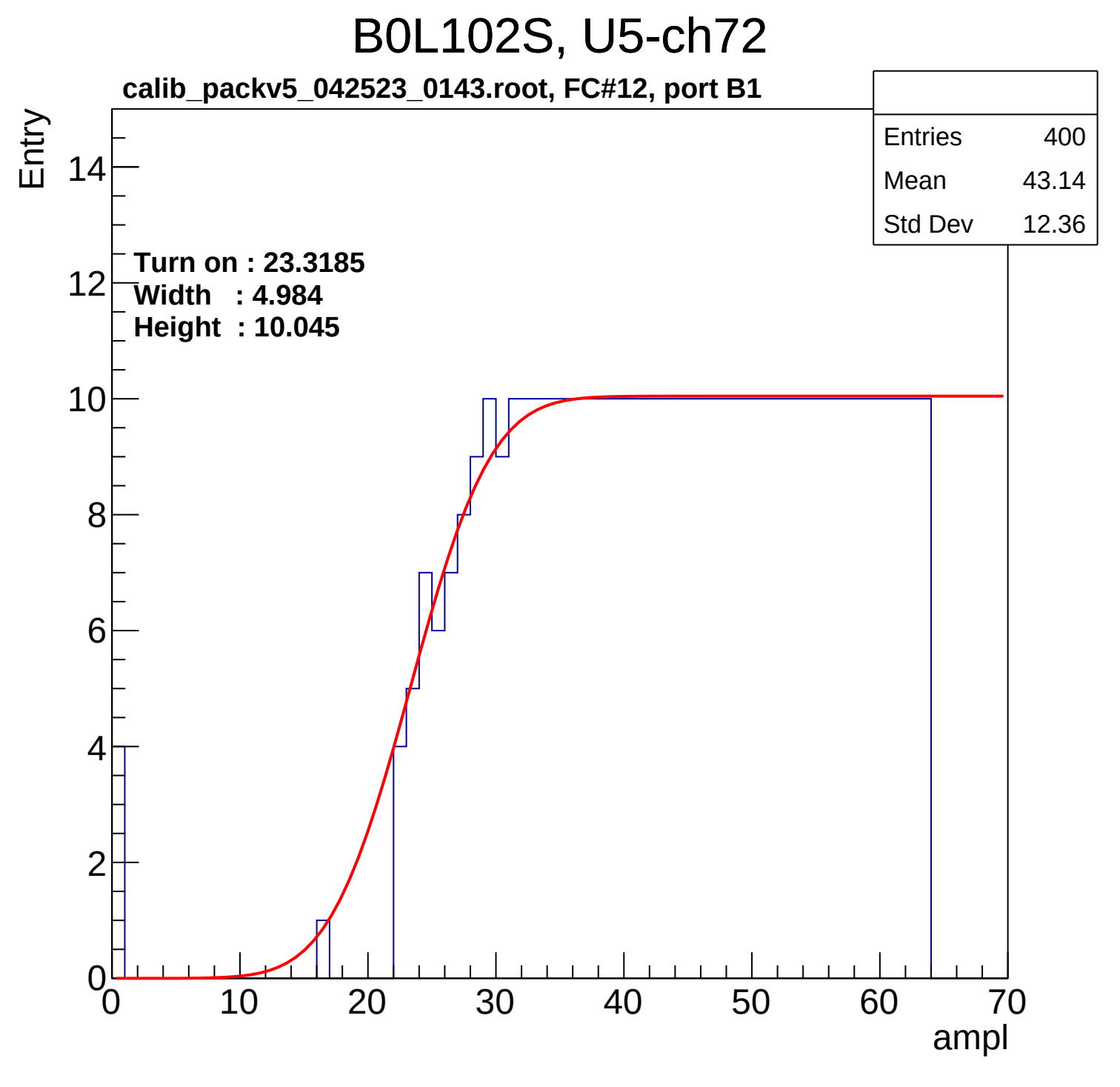
B0L102S, U5-ch72
calib_packv5_042523_0143.root, FC#12, port B1
Entries 400
Mean 43.14
Std Dev 12.36
Turn on : 23.3185
Width : 4.984
Height : 10.045
Entry
ampl
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4
6
8
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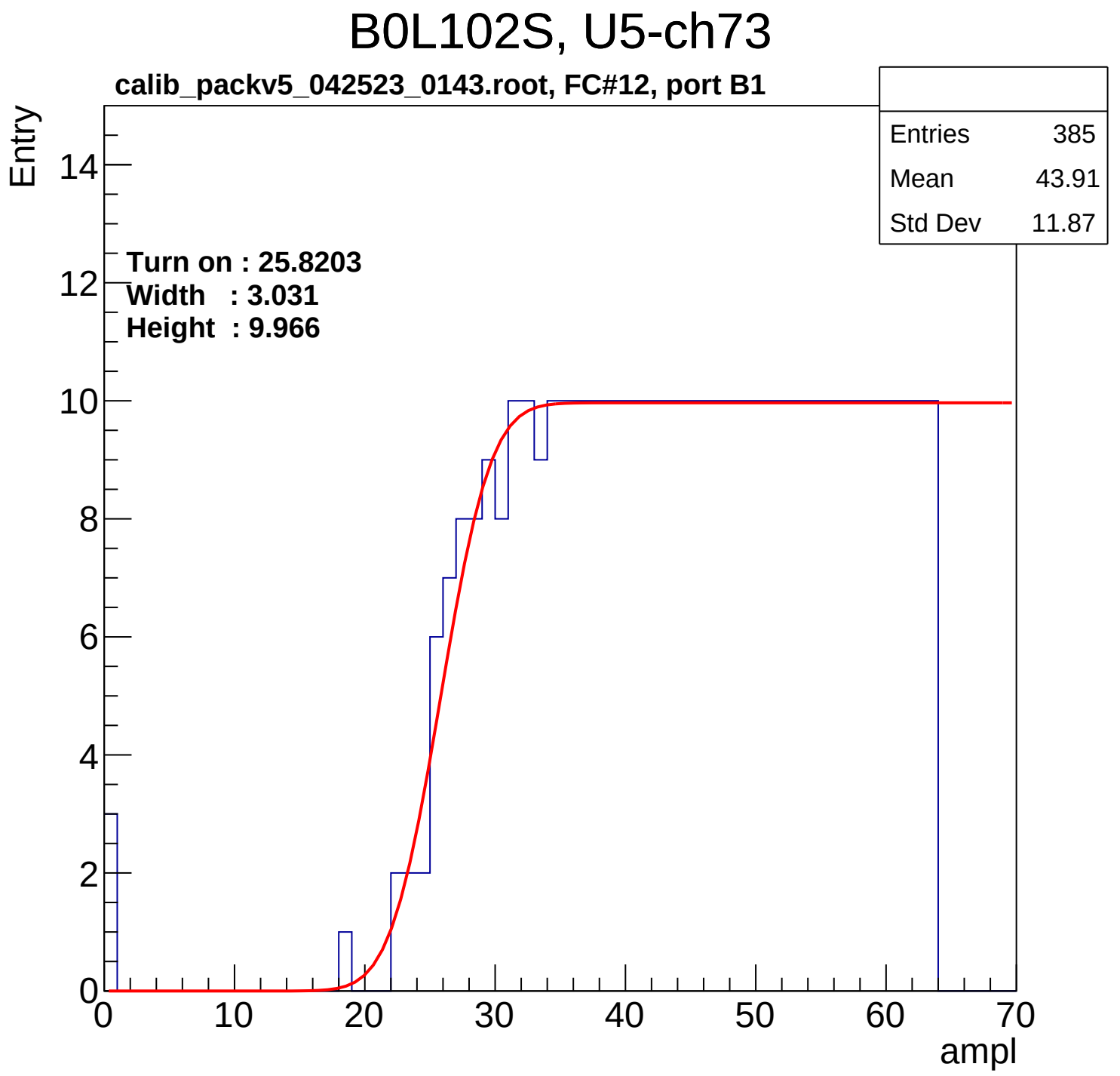
B0L102S, U5-ch73
calib_packv5_042523_0143.root, FC#12, port B1
Entries 385
Mean 43.91
Std Dev 11.87
Turn on : 25.8203
Width : 3.031
Height : 9.966
Entry
ampl
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8
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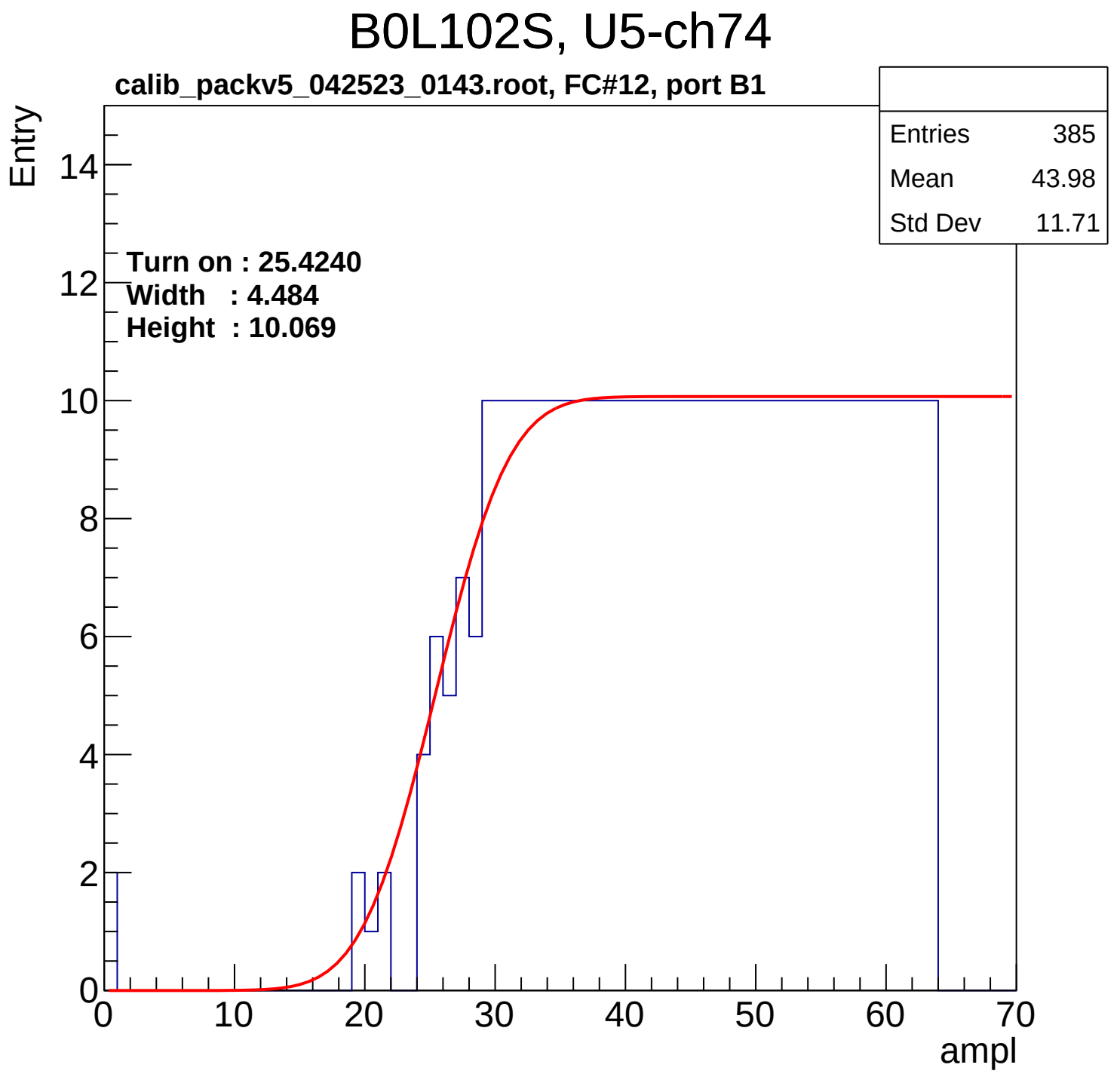
B0L102S, U5-ch74
calib_packv5_042523_0143.root, FC#12, port B1
Entries 385
Mean 43.98
Std Dev 11.71
Turn on : 25.4240
Width : 4.484
Height : 10.069
Entry
ampl
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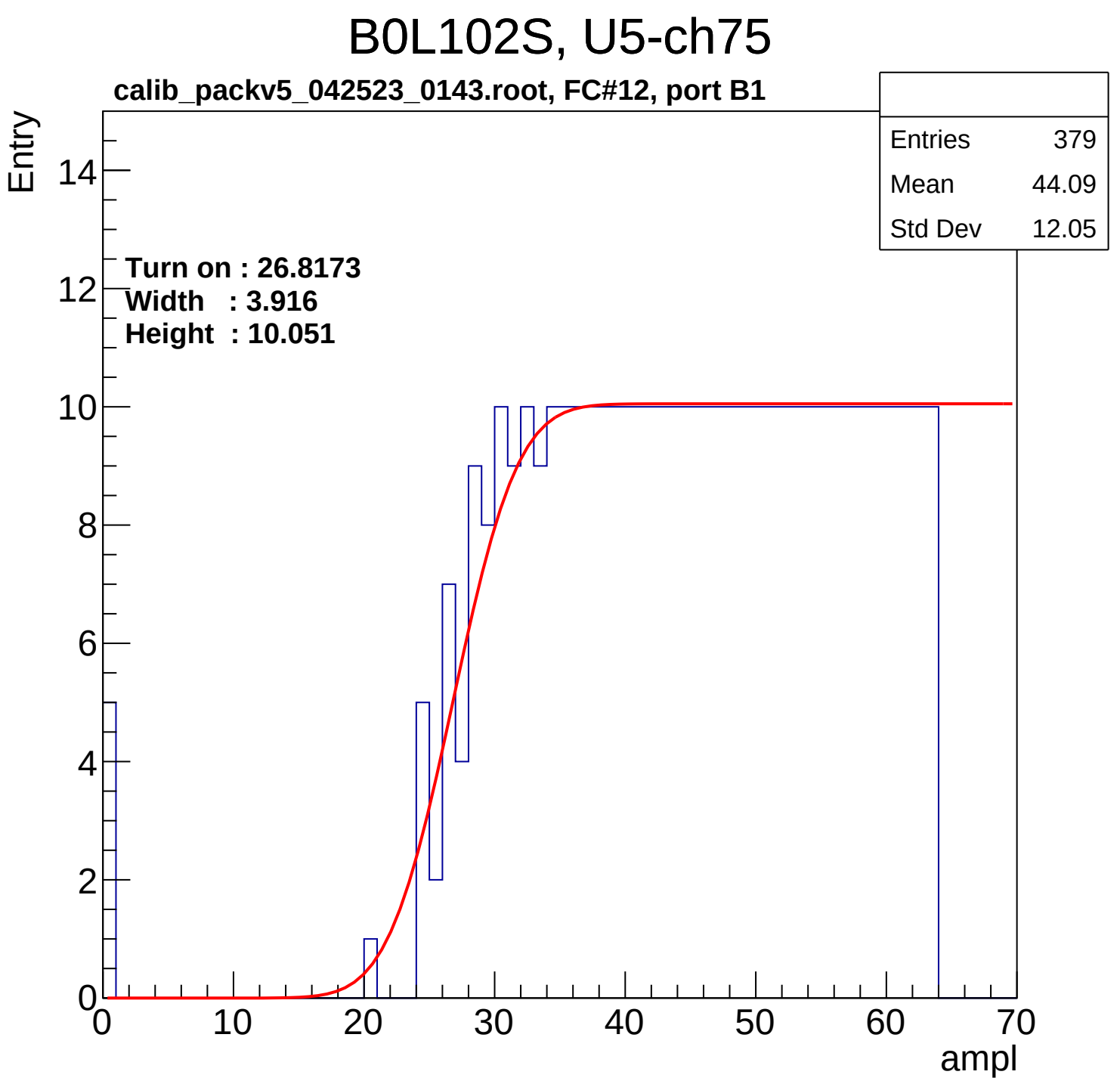
B0L102S, U5-ch75
calib_packv5_042523_0143.root, FC#12, port B1
Entries 379
Mean 44.09
Std Dev 12.05
Turn on : 26.8173
Width : 3.916
Height : 10.051
Entry
ampl
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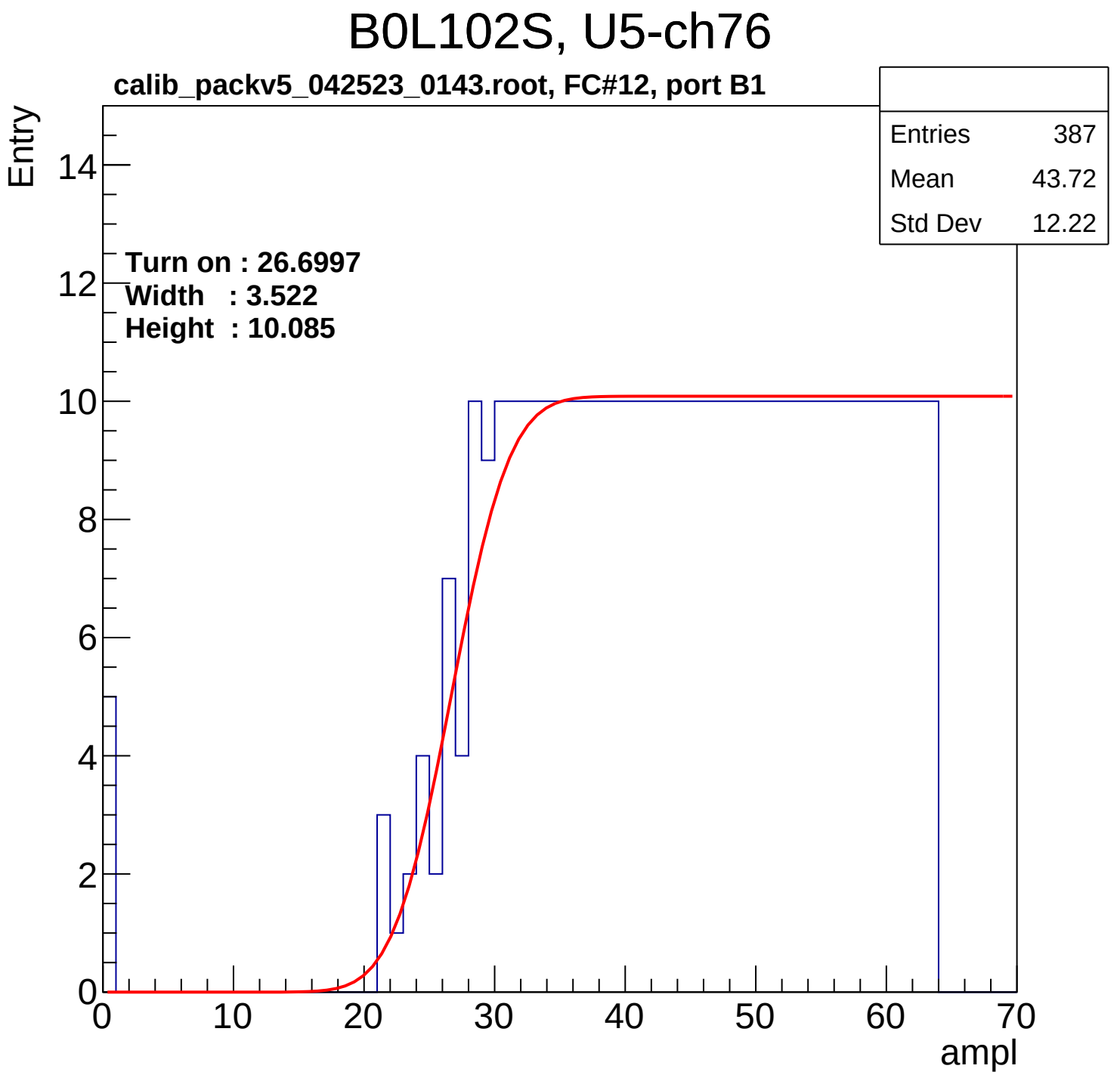
B0L102S, U5-ch76
calib_packv5_042523_0143.root, FC#12, port B1
Entries 387
Mean 43.72
Std Dev 12.22
Turn on : 26.6997
Width : 3.522
Height : 10.085
Entry
ampl
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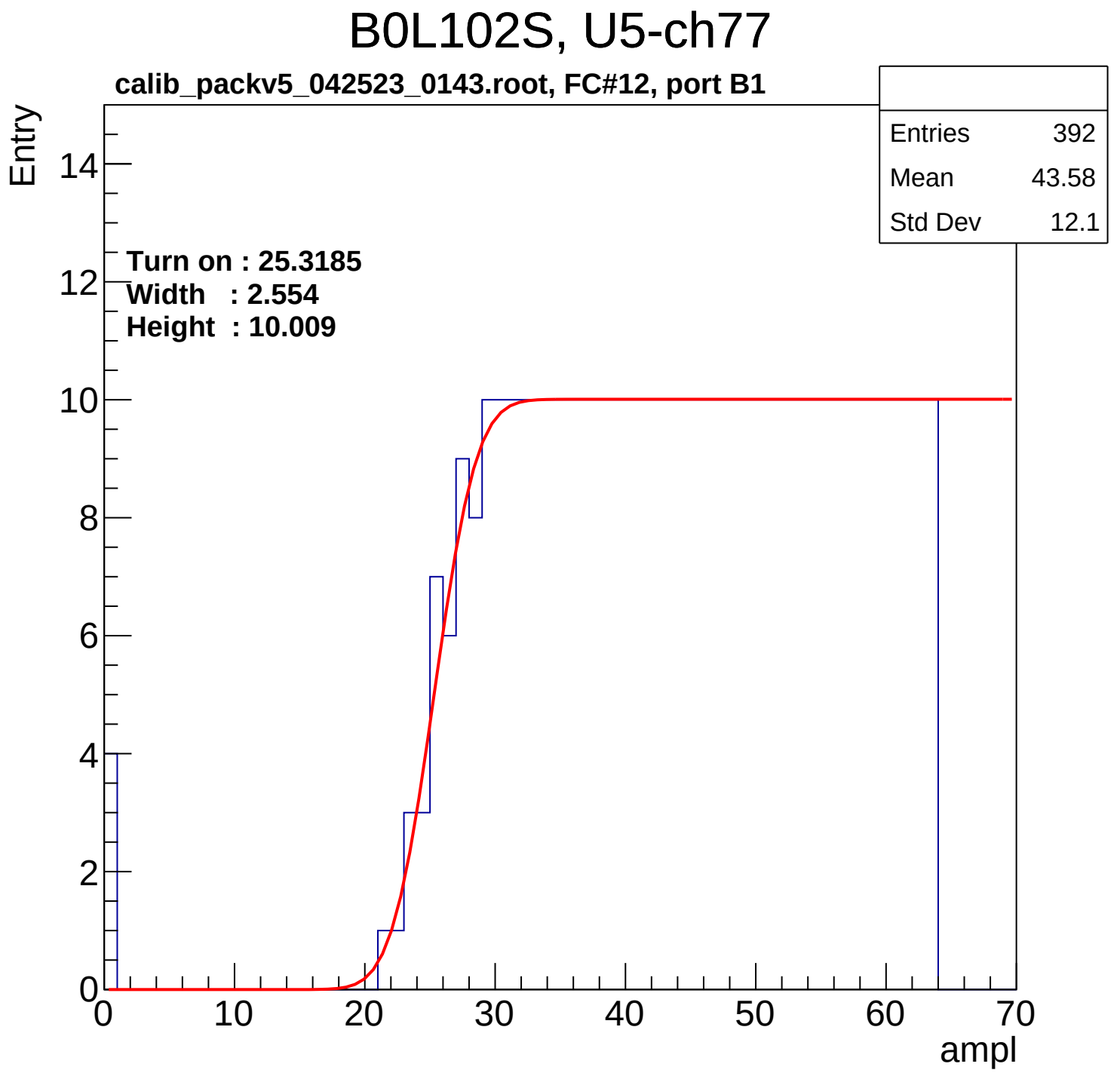
B0L102S, U5-ch77
calib_packv5_042523_0143.root, FC#12, port B1
Entries 392
Mean 43.58
Std Dev 12.1
Turn on : 25.3185
Width : 2.554
Height : 10.009
Entry
ampl
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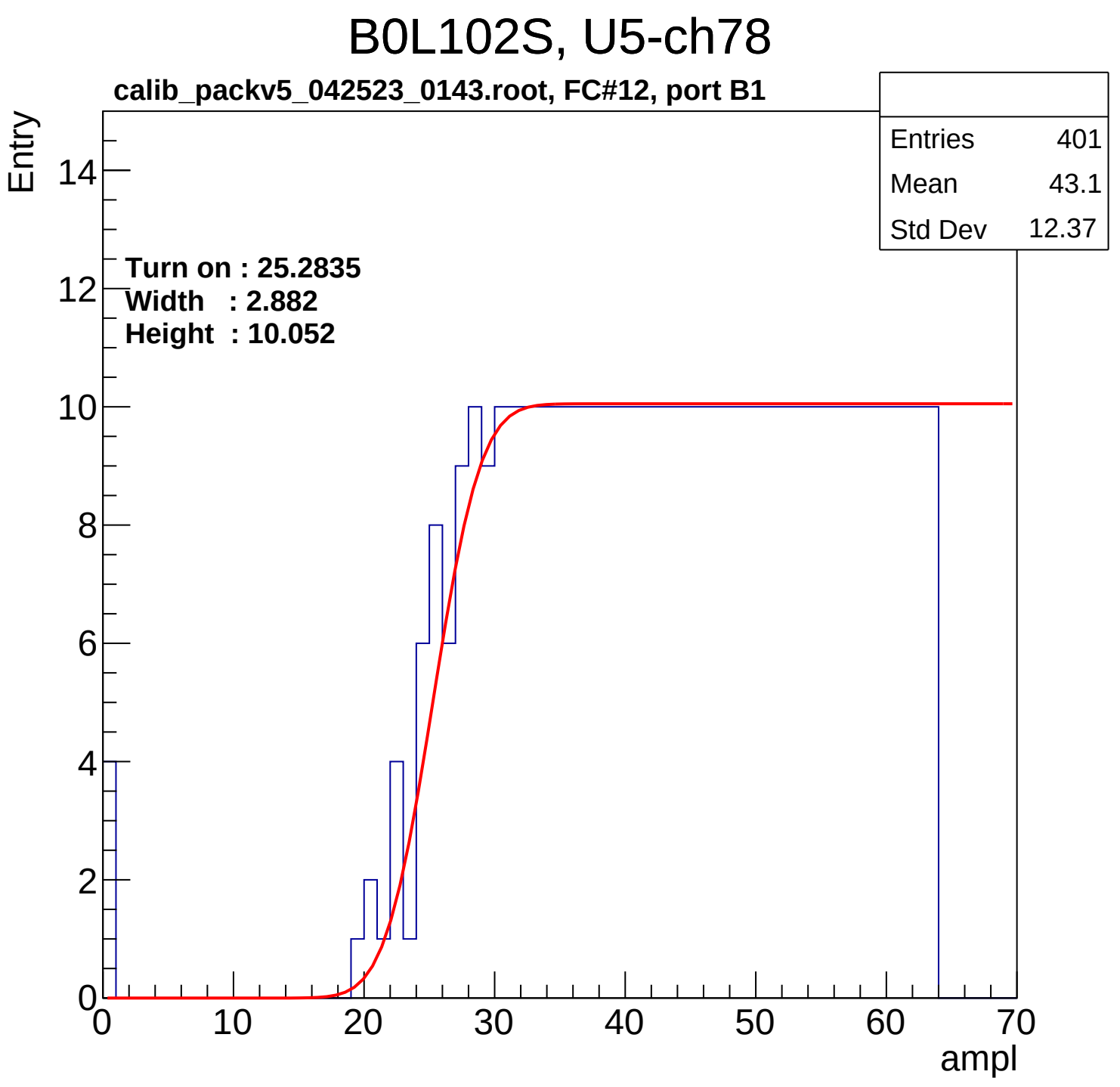
B0L102S, U5-ch78
calib_packv5_042523_0143.root, FC#12, port B1
Entries 401
Mean 43.1
Std Dev 12.37
Turn on : 25.2835
Width : 2.882
Height : 10.052
Entry
ampl
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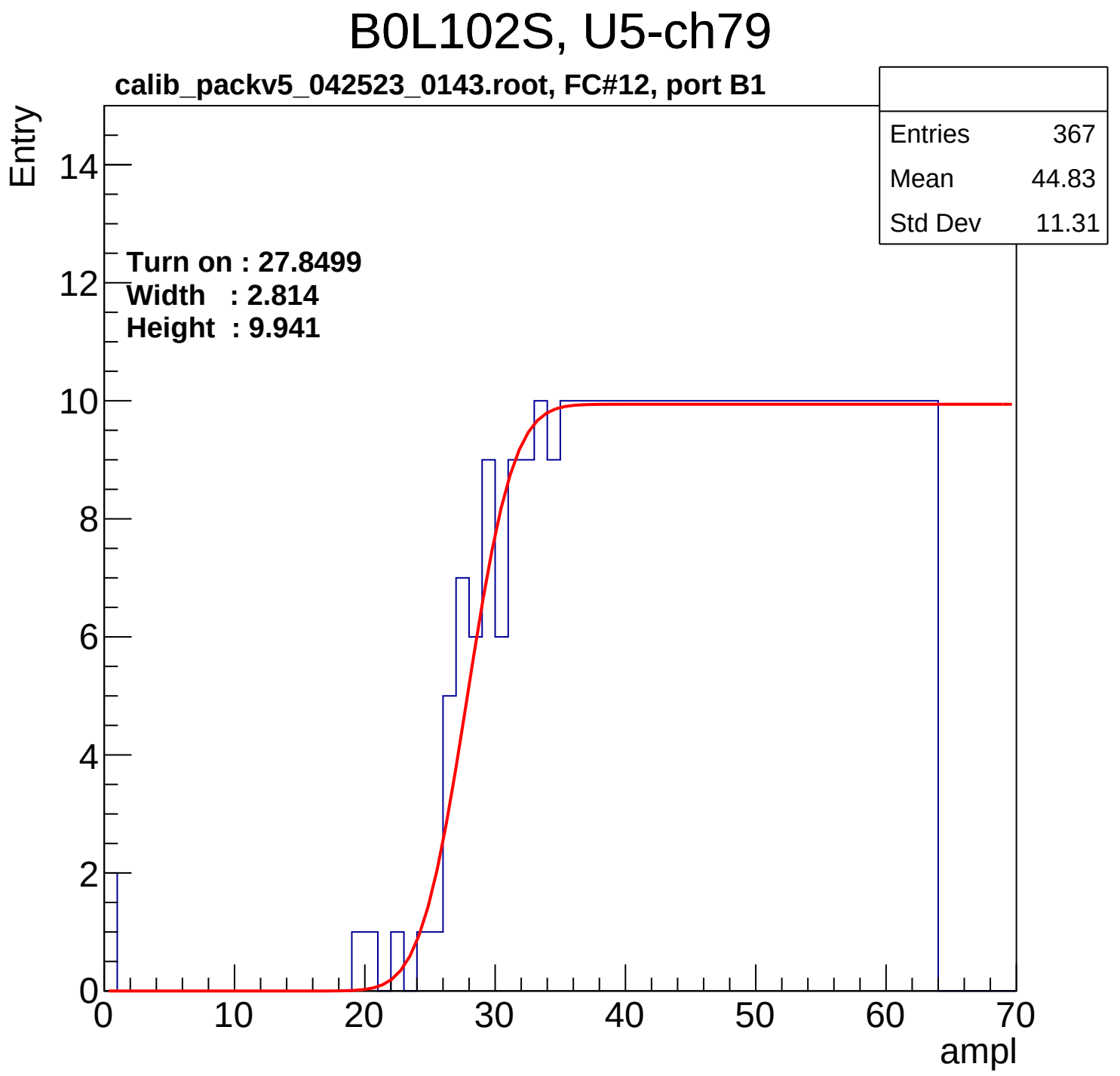
B0L102S, U5-ch79
calib_packv5_042523_0143.root, FC#12, port B1
Entries 367
Mean 44.83
Std Dev 11.31
Turn on : 27.8499
Width : 2.814
Height : 9.941
Entry
ampl
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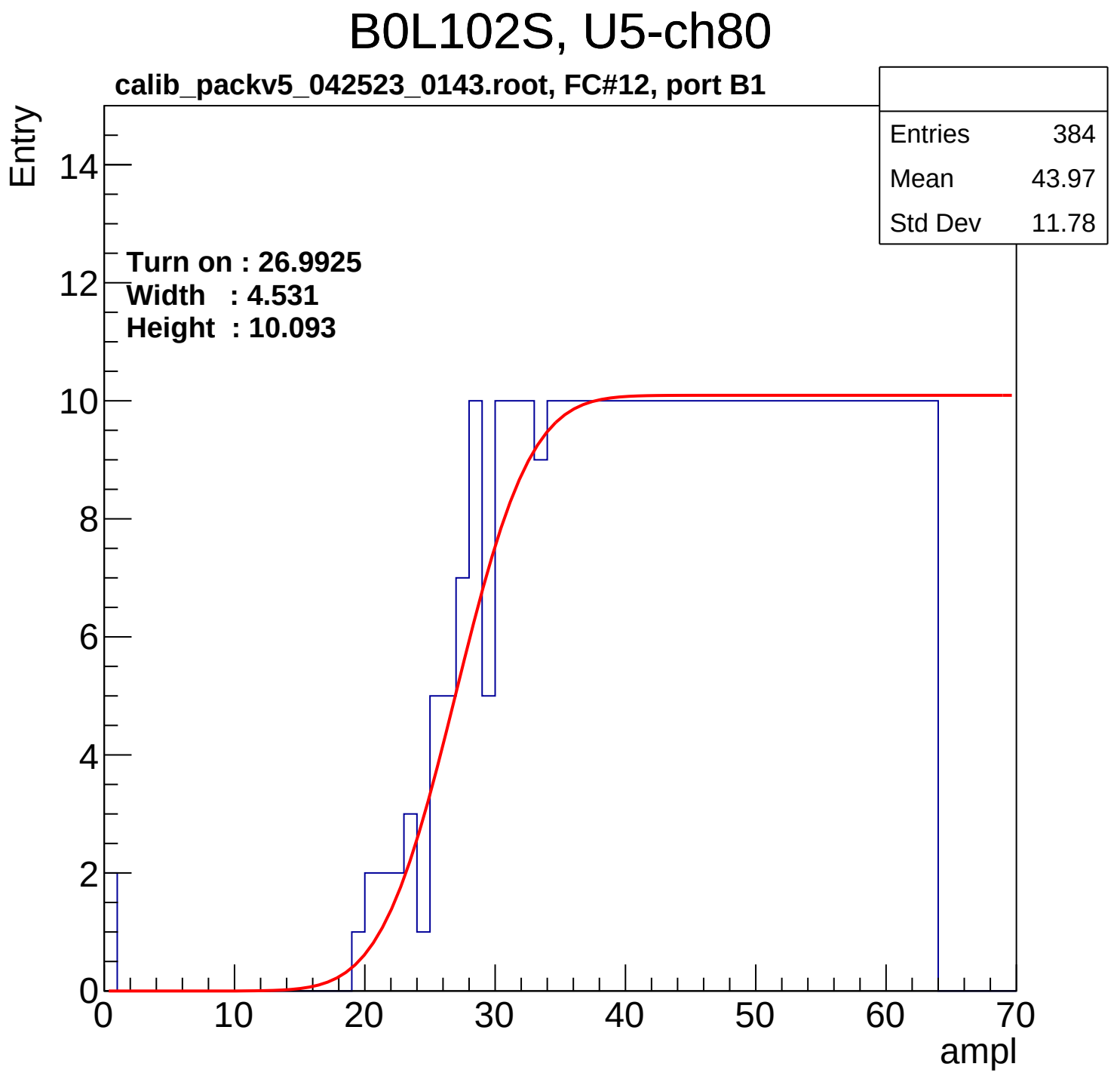
B0L102S, U5-ch80
calib_packv5_042523_0143.root, FC#12, port B1
Entries 384
Mean 43.97
Std Dev 11.78
Turn on : 26.9925
Width : 4.531
Height : 10.093
Entry
ampl
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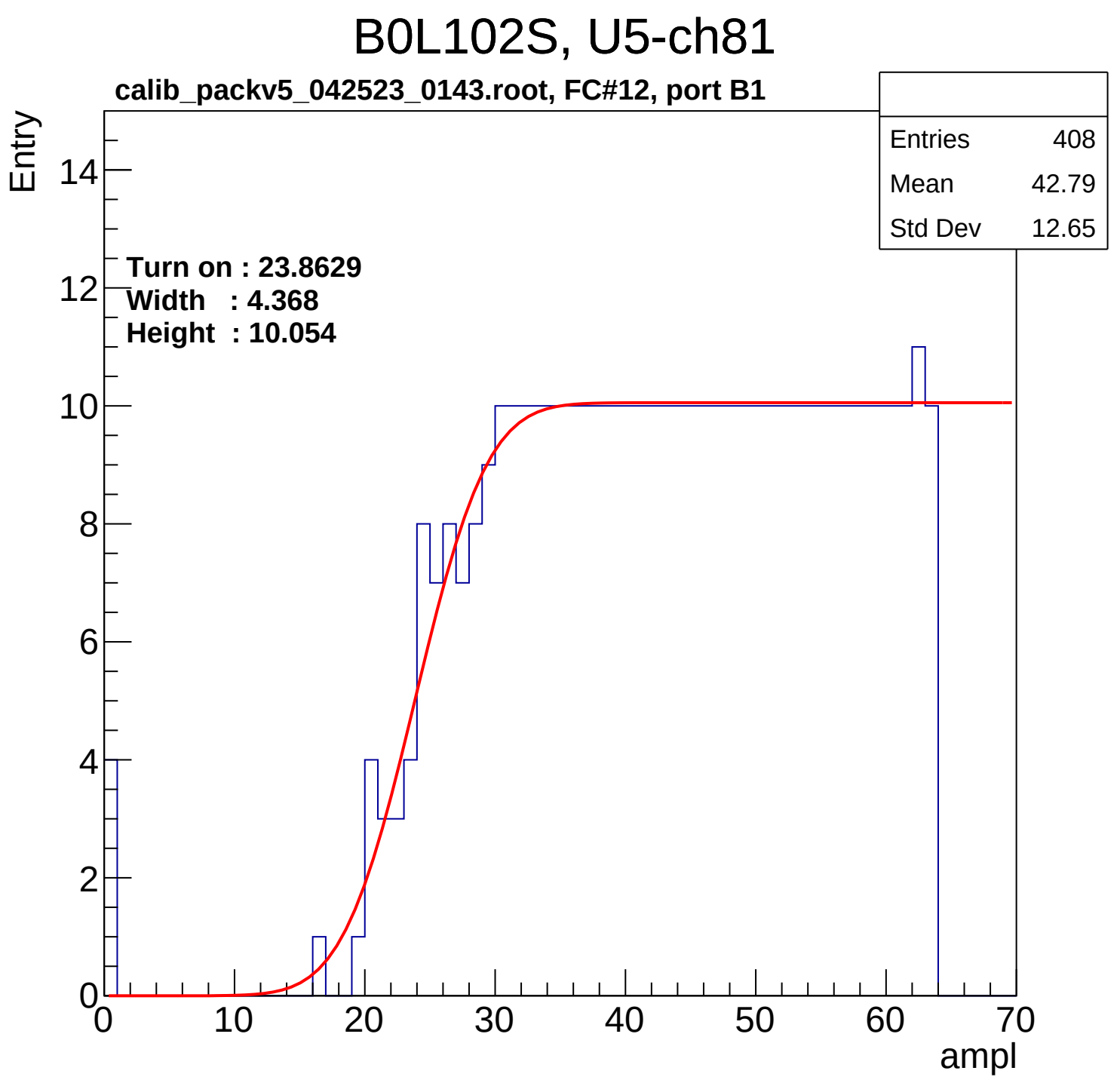
B0L102S, U5-ch81
calib_packv5_042523_0143.root, FC#12, port B1
Entries 408
Mean 42.79
Std Dev 12.65
Turn on : 23.8629
Width : 4.368
Height : 10.054
Entry
ampl
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6
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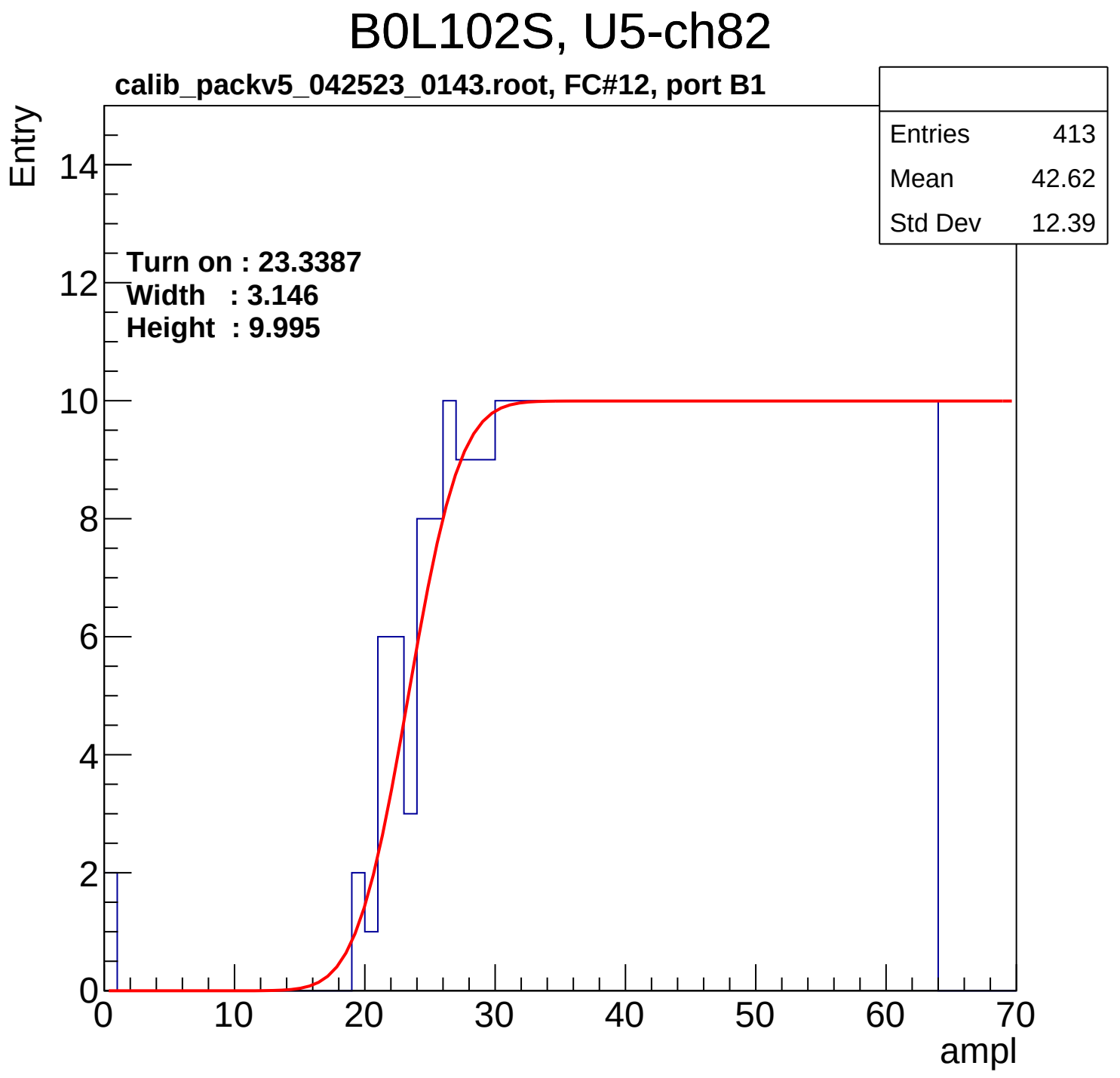
B0L102S, U5-ch82
calib_packv5_042523_0143.root, FC#12, port B1
Entries 413
Mean 42.62
Std Dev 12.39
Turn on : 23.3387
Width : 3.146
Height : 9.995
Entry
ampl
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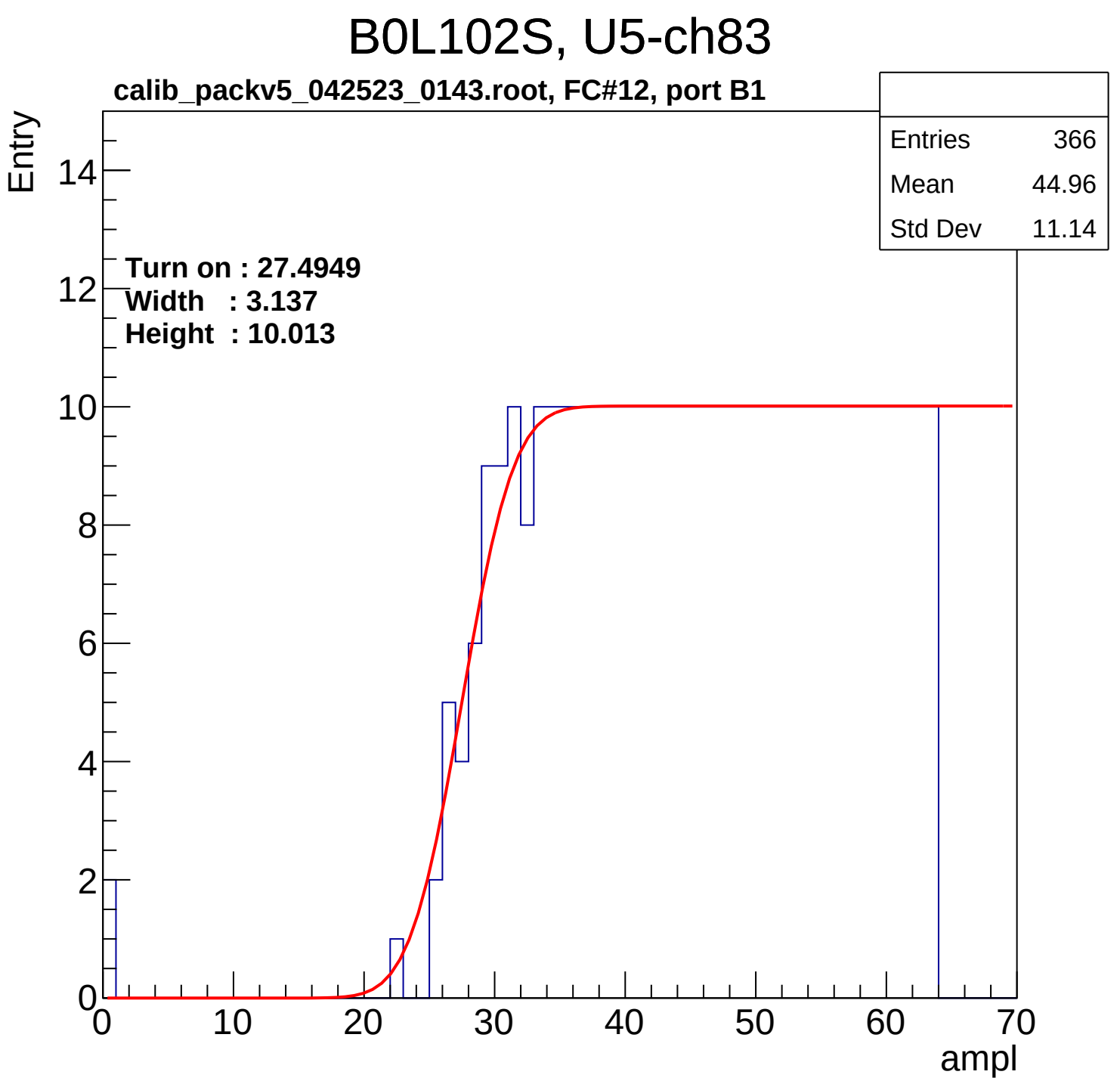
B0L102S, U5-ch83
calib_packv5_042523_0143.root, FC#12, port B1
Entries 366
Mean 44.96
Std Dev 11.14
Turn on : 27.4949
Width : 3.137
Height : 10.013
Entry
ampl
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6
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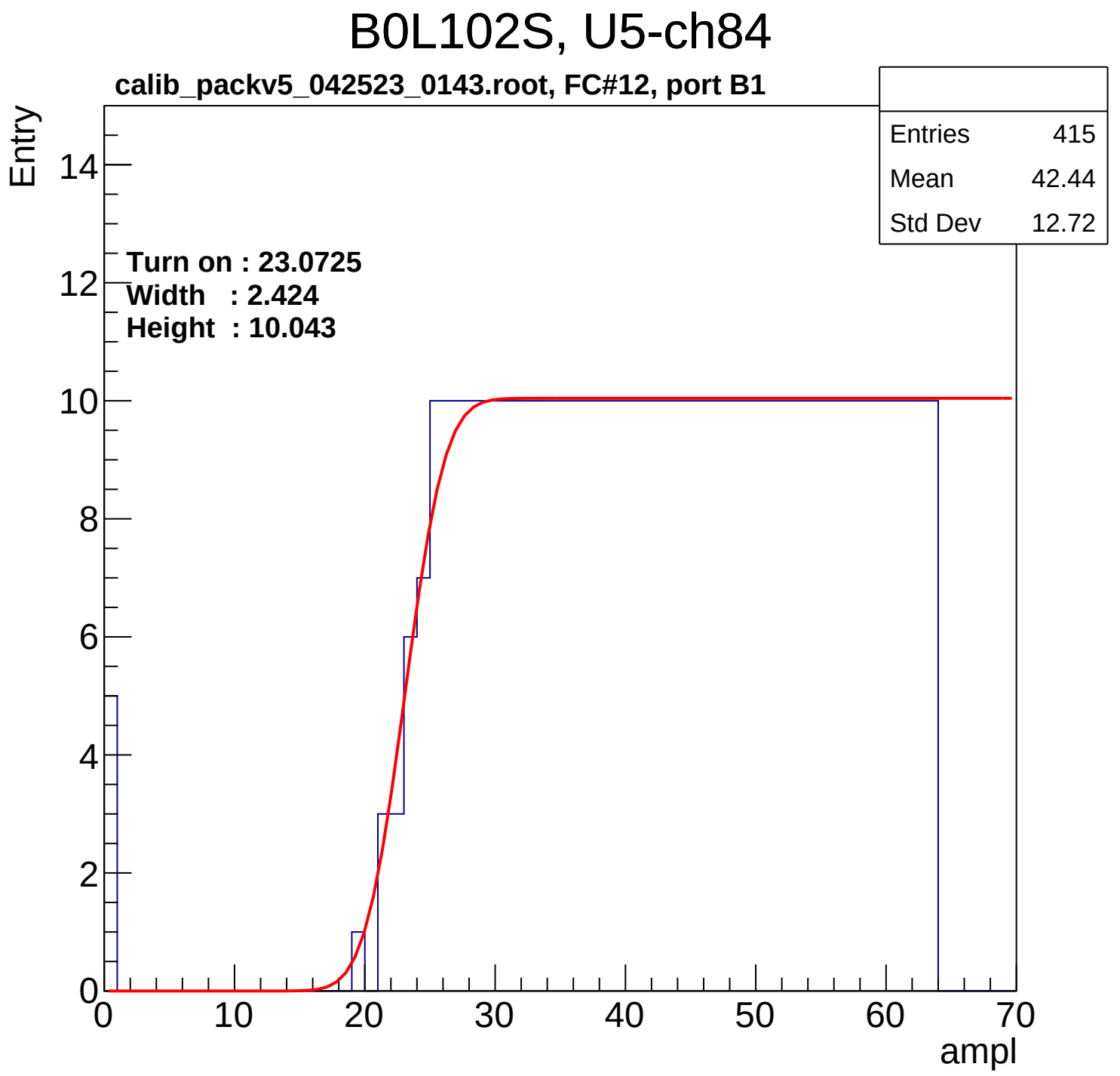
B0L102S, U5-ch84
calib_packv5_042523_0143.root, FC#12, port B1
Entries 415
Mean 42.44
Std Dev 12.72
Turn on : 23.0725
Width : 2.424
Height : 10.043
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ampl
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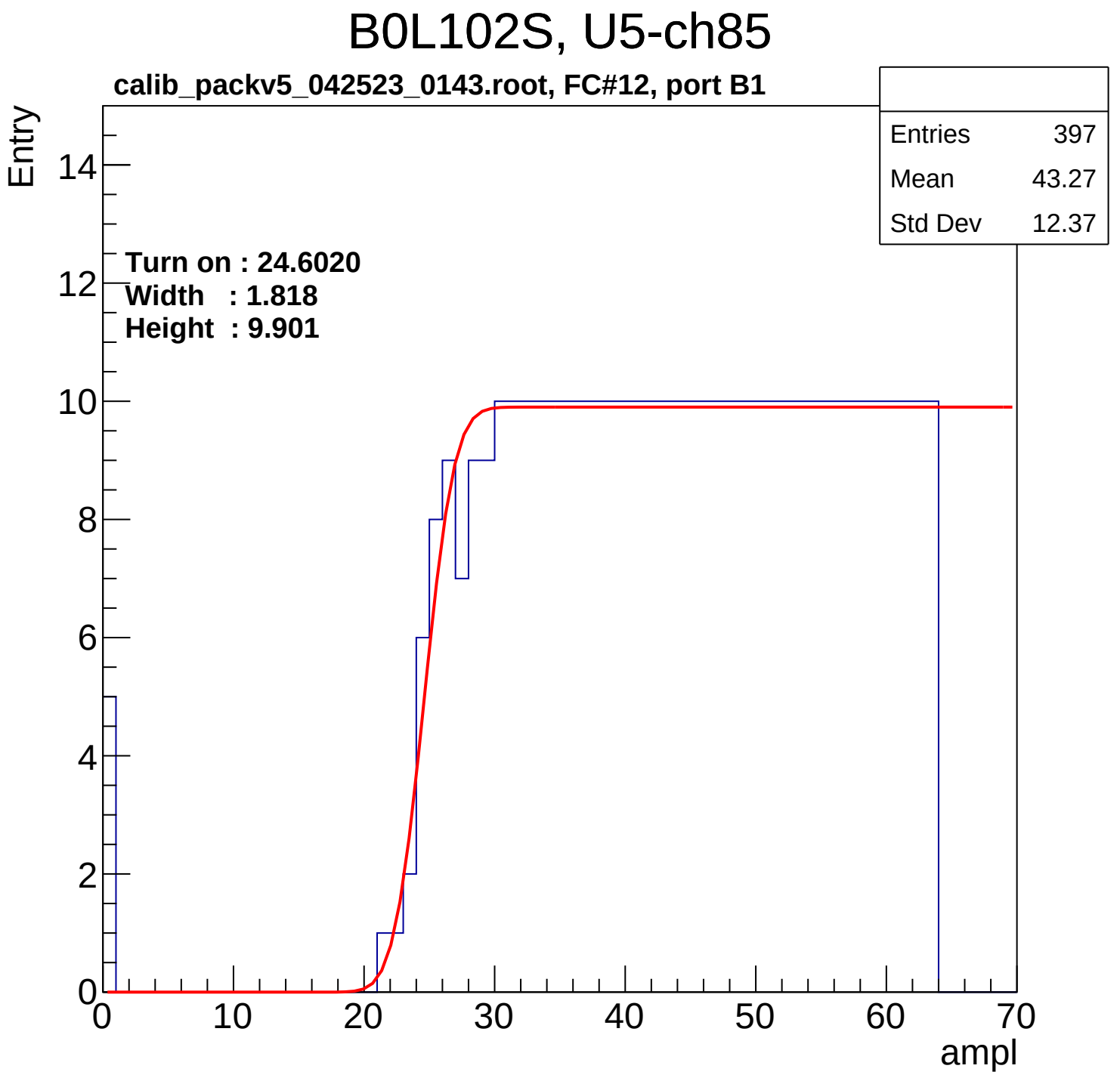
B0L102S, U5-ch85
calib_packv5_042523_0143.root, FC#12, port B1
Entries 397
Mean 43.27
Std Dev 12.37
Turn on : 24.6020
Width : 1.818
Height : 9.901
Entry
ampl
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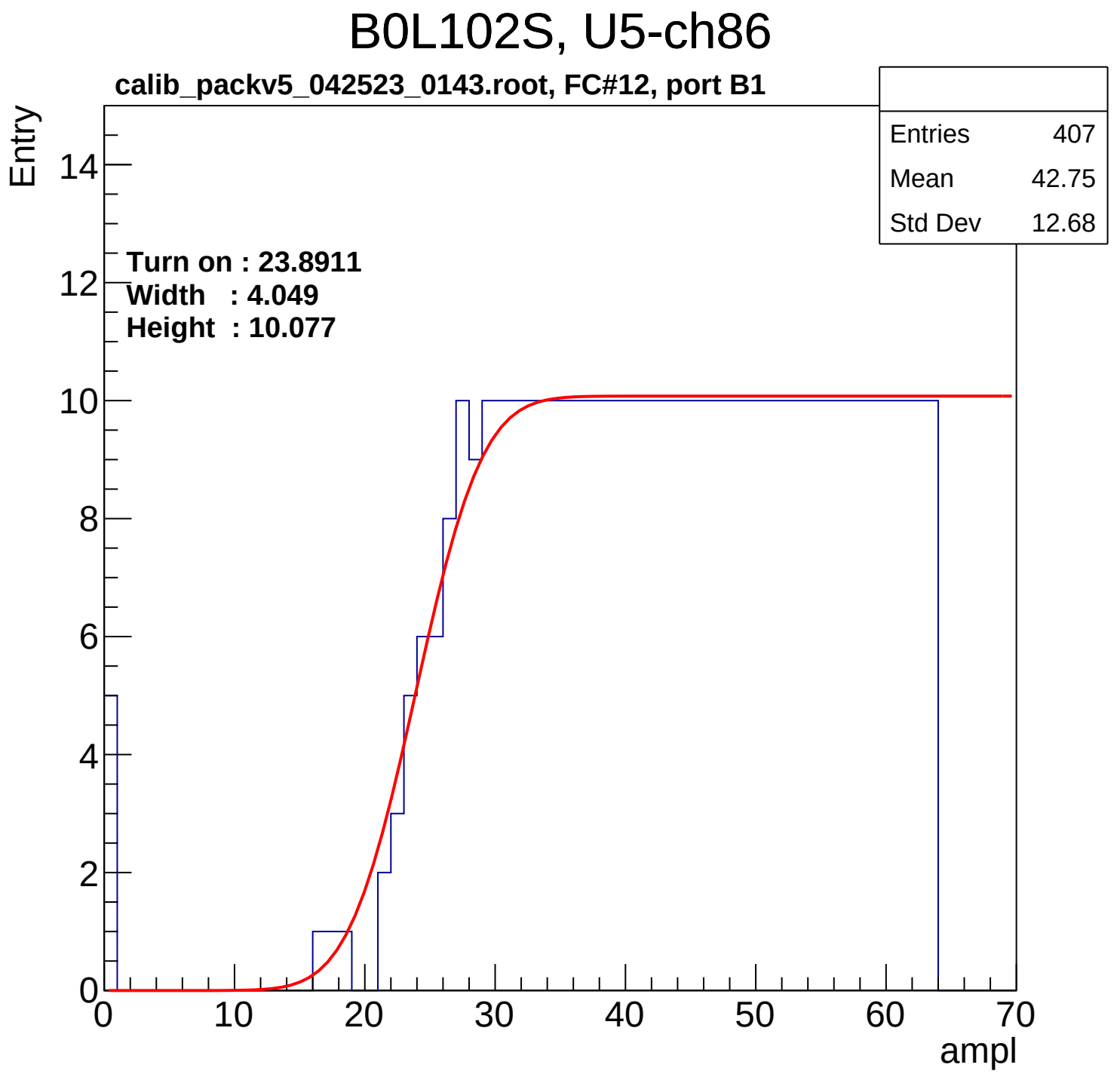
B0L102S, U5-ch86
calib_packv5_042523_0143.root, FC#12, port B1
Entries 407
Mean 42.75
Std Dev 12.68
Turn on : 23.8911
Width : 4.049
Height : 10.077
Entry
ampl
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20
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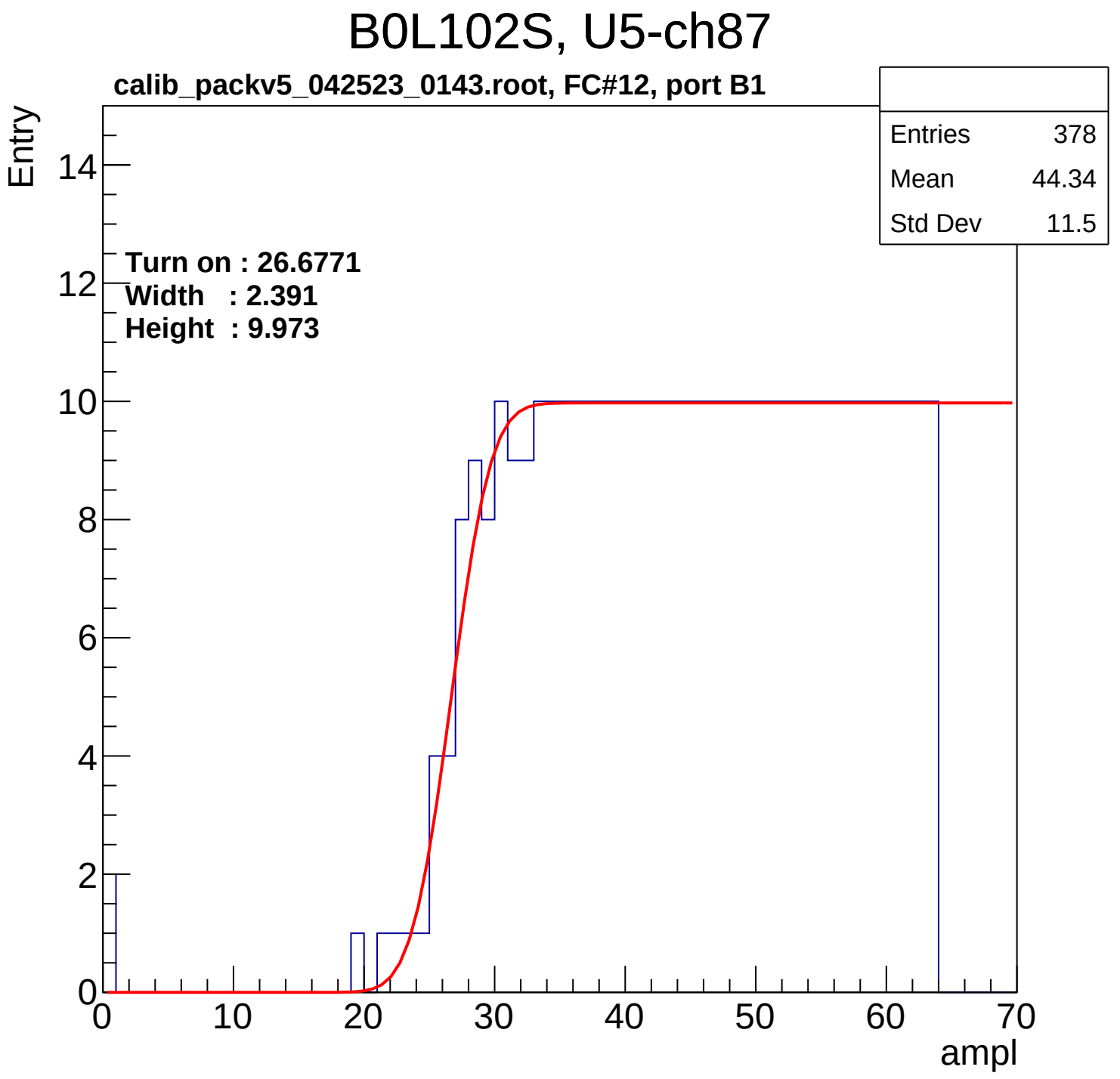
B0L102S, U5-ch87
calib_packv5_042523_0143.root, FC#12, port B1
Entries 378
Mean 44.34
Std Dev 11.5
Turn on : 26.6771
Width : 2.391
Height : 9.973
Entry
ampl
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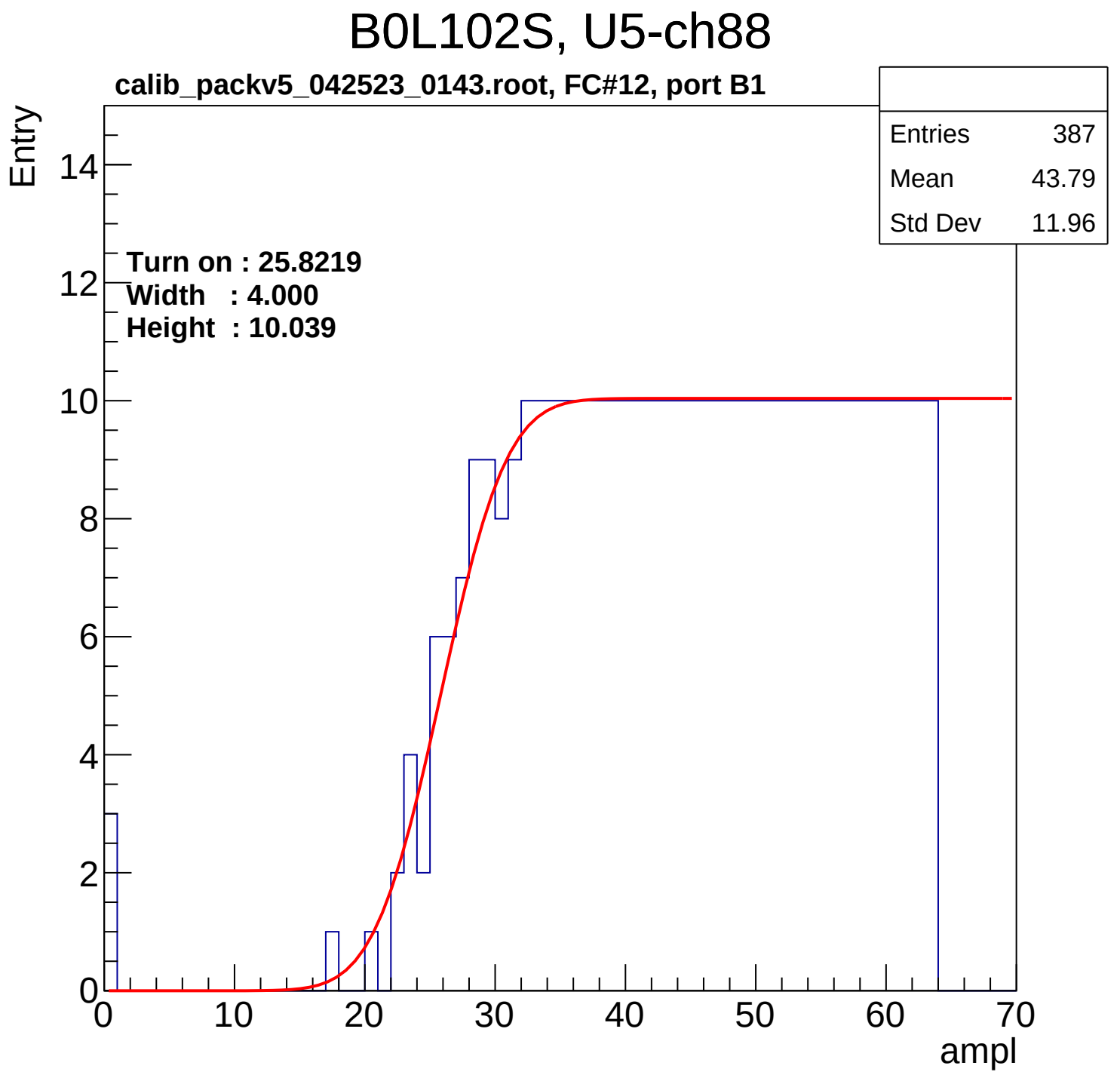
B0L102S, U5-ch88
calib_packv5_042523_0143.root, FC#12, port B1
Entries 387
Mean 43.79
Std Dev 11.96
Turn on : 25.8219
Width : 4.000
Height : 10.039
Entry
ampl
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2
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6
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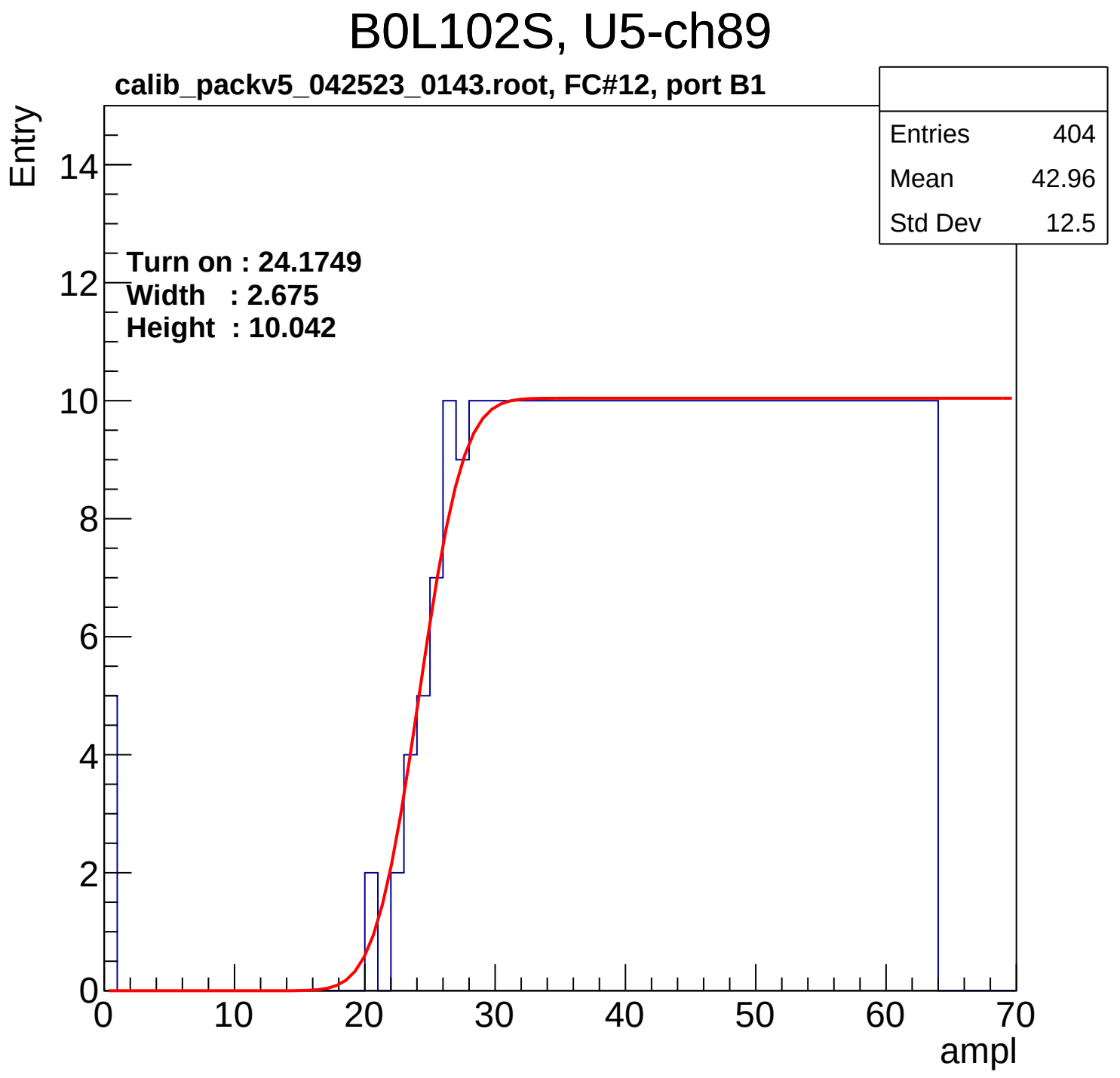
B0L102S, U5-ch89
calib_packv5_042523_0143.root, FC#12, port B1
Entries 404
Mean 42.96
Std Dev 12.5
Turn on : 24.1749
Width : 2.675
Height : 10.042
Entry
ampl
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4
6
8
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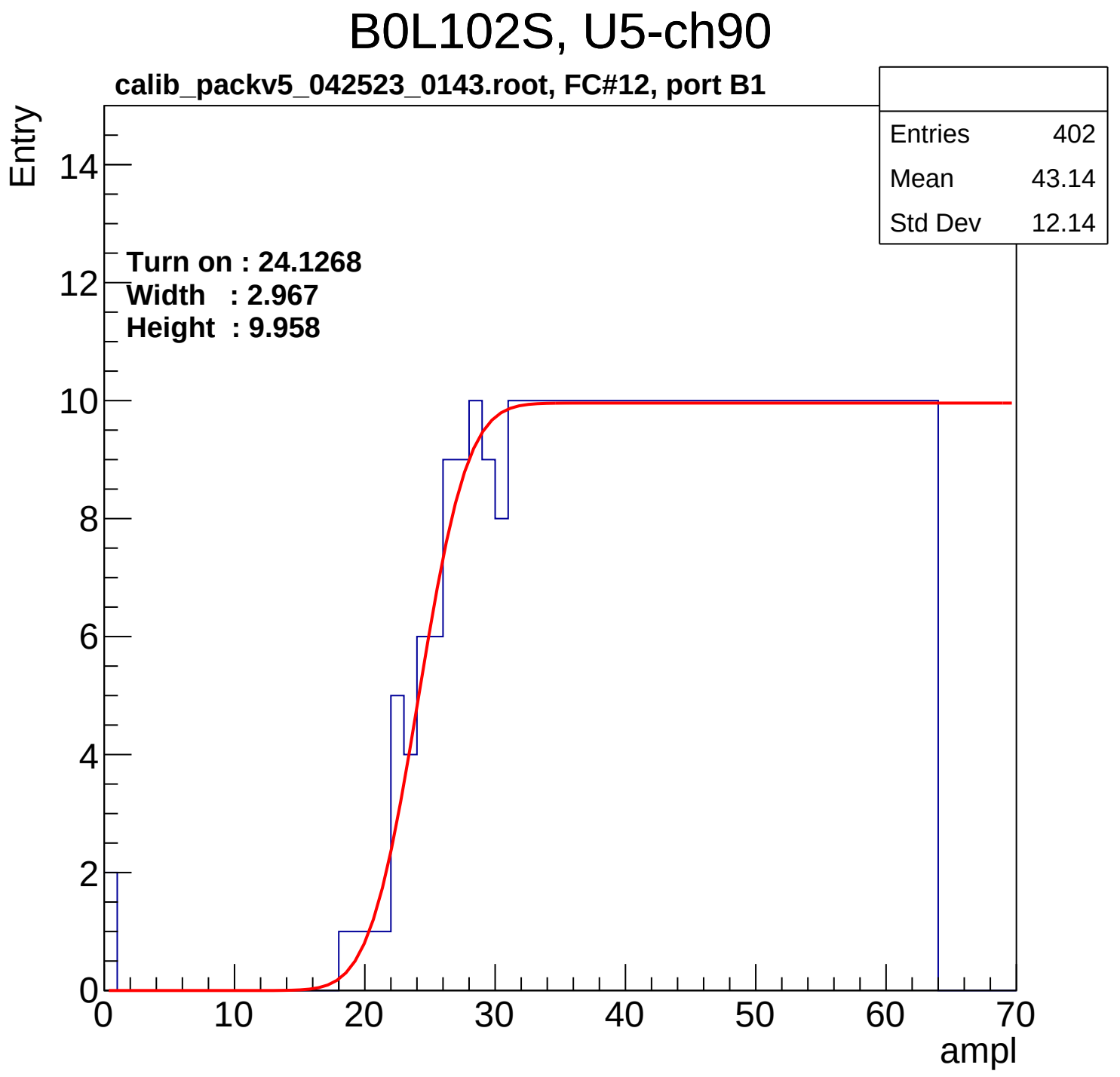
B0L102S, U5-ch90
calib_packv5_042523_0143.root, FC#12, port B1
Entries 402
Mean 43.14
Std Dev 12.14
Turn on : 24.1268
Width : 2.967
Height : 9.958
Entry
ampl
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2
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6
8
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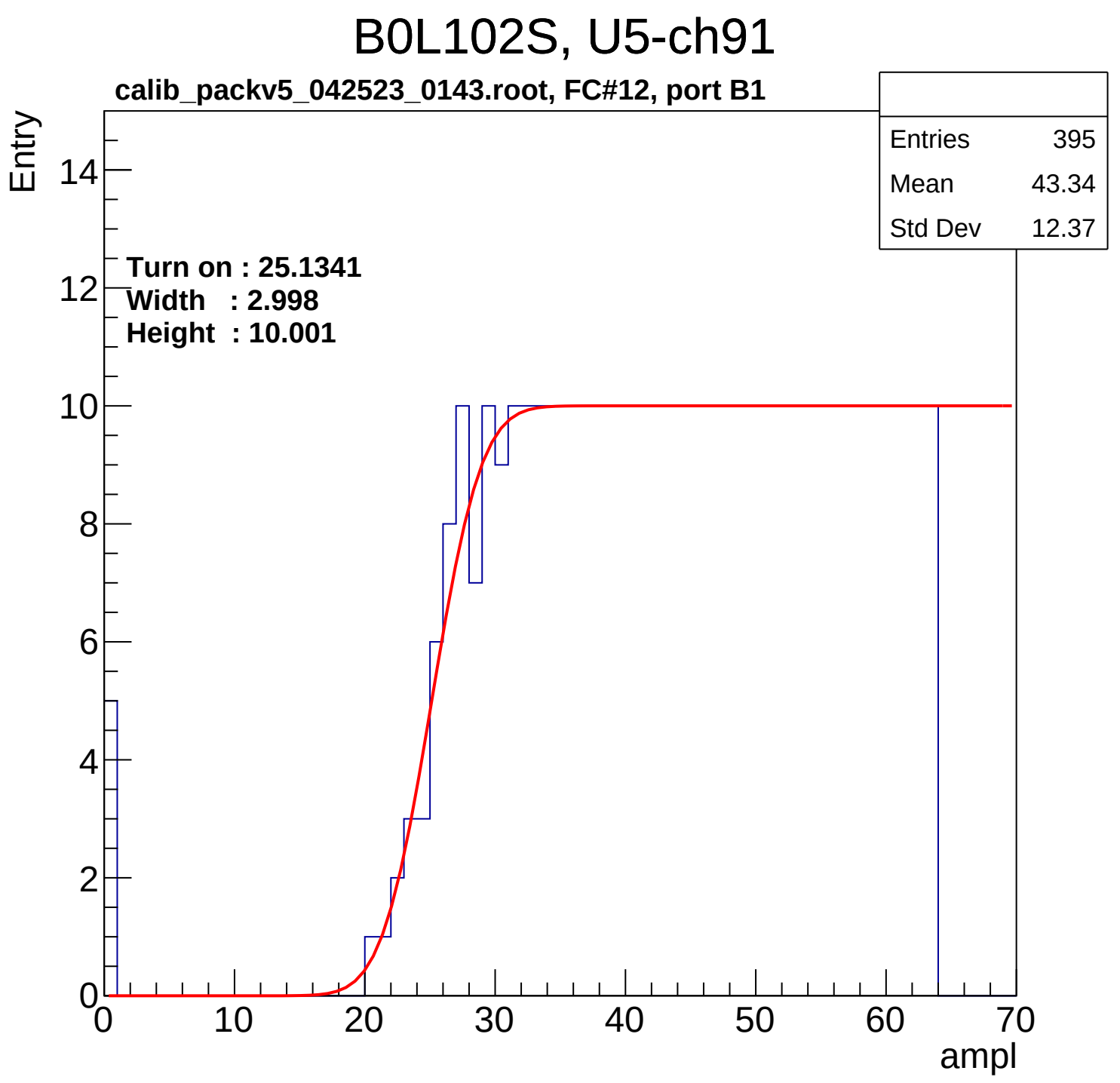
B0L102S, U5-ch91
calib_packv5_042523_0143.root, FC#12, port B1
Entries 395
Mean 43.34
Std Dev 12.37
Turn on : 25.1341
Width : 2.998
Height : 10.001
Entry
ampl
0
2
4
6
8
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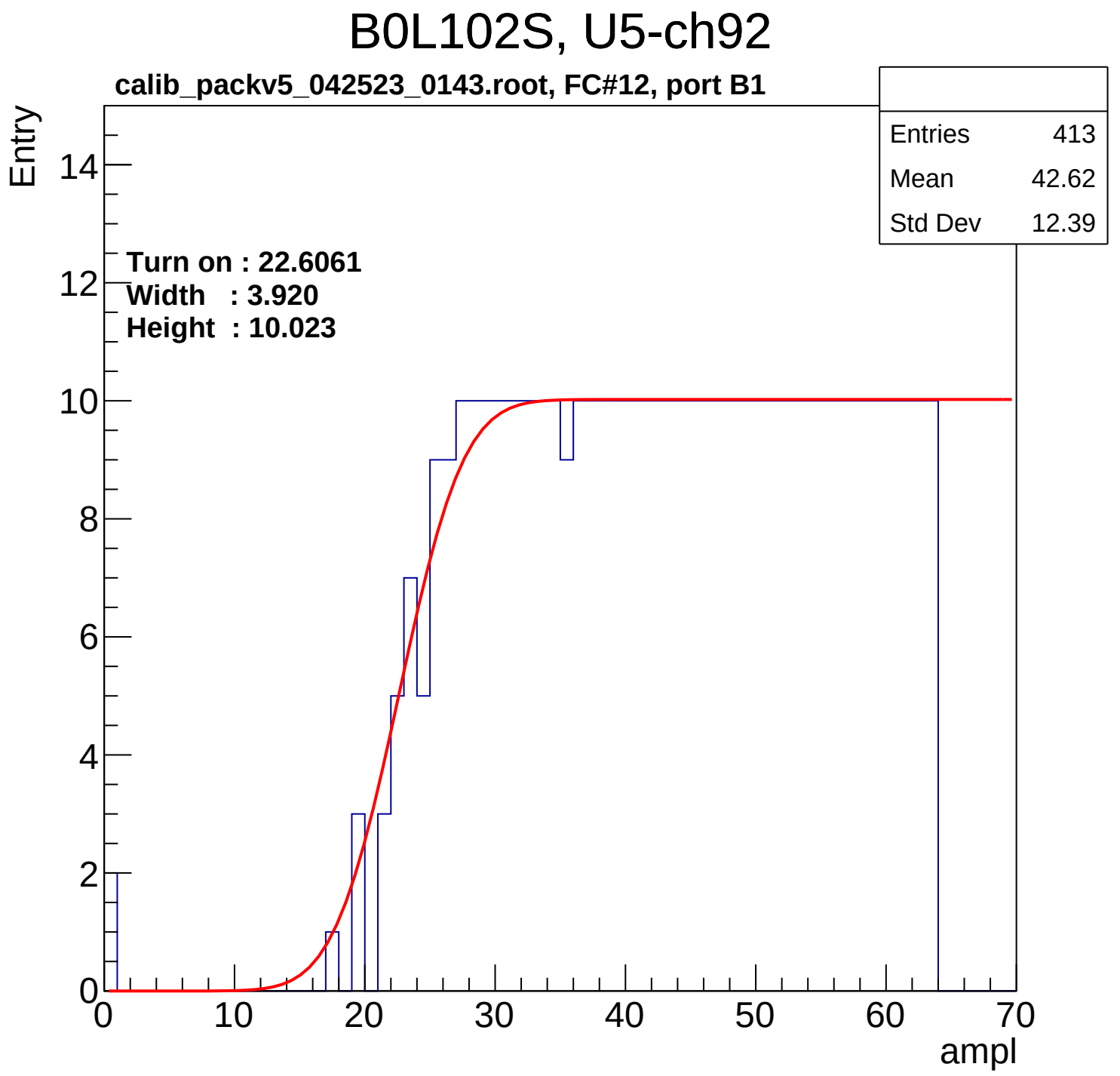
B0L102S, U5-ch92
calib_packv5_042523_0143.root, FC#12, port B1
Entries 413
Mean 42.62
Std Dev 12.39
Turn on : 22.6061
Width : 3.920
Height : 10.023
Entry
ampl
0
2
4
6
8
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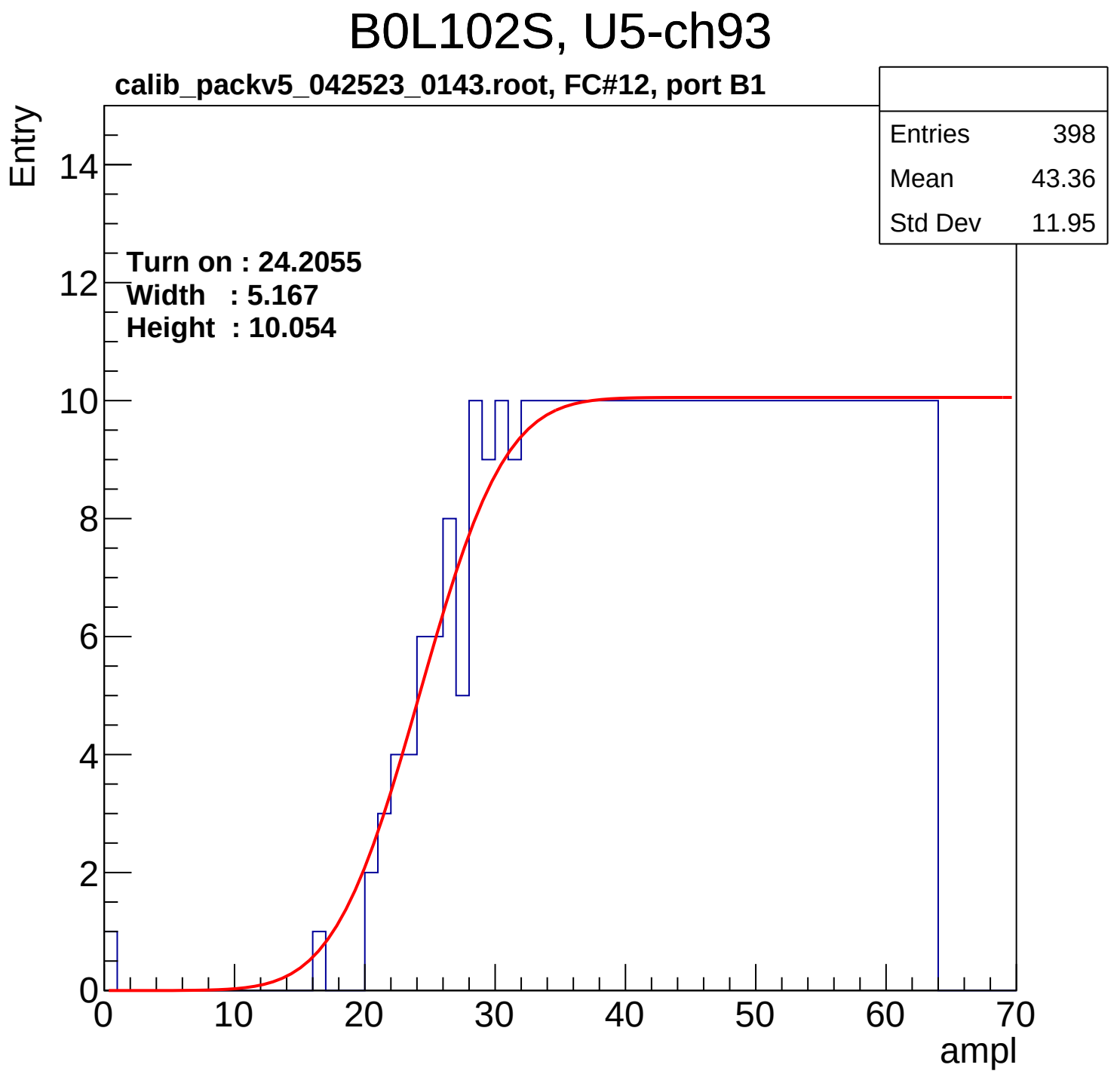
B0L102S, U5-ch93
calib_packv5_042523_0143.root, FC#12, port B1
Entries 398
Mean 43.36
Std Dev 11.95
Turn on : 24.2055
Width : 5.167
Height : 10.054
Entry
ampl
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2
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6
8
10
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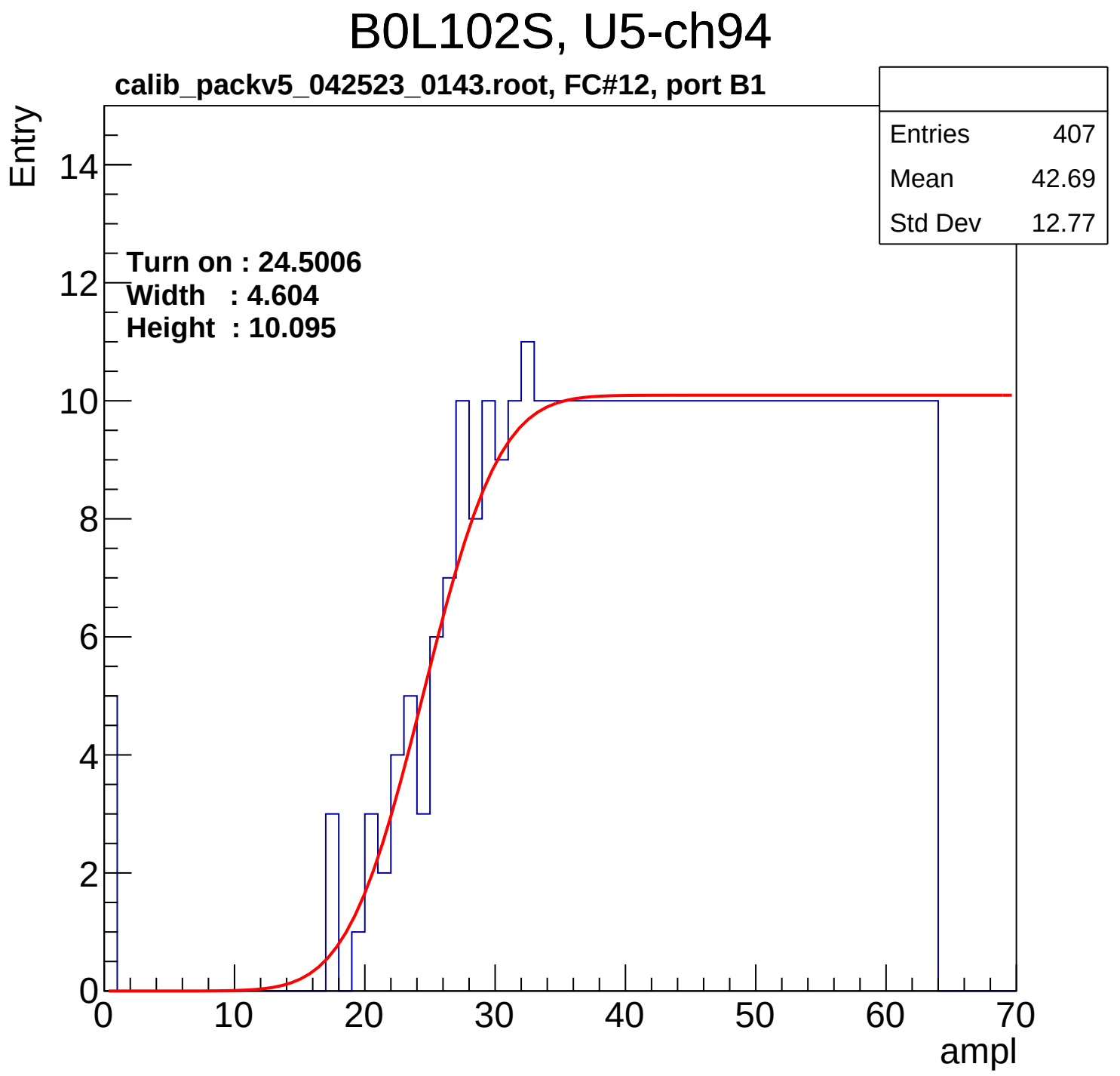
B0L102S, U5-ch94
calib_packv5_042523_0143.root, FC#12, port B1
Entries 407
Mean 42.69
Std Dev 12.77
Turn on : 24.5006
Width : 4.604
Height : 10.095
Entry
ampl
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2
4
6
8
10
12
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0
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60
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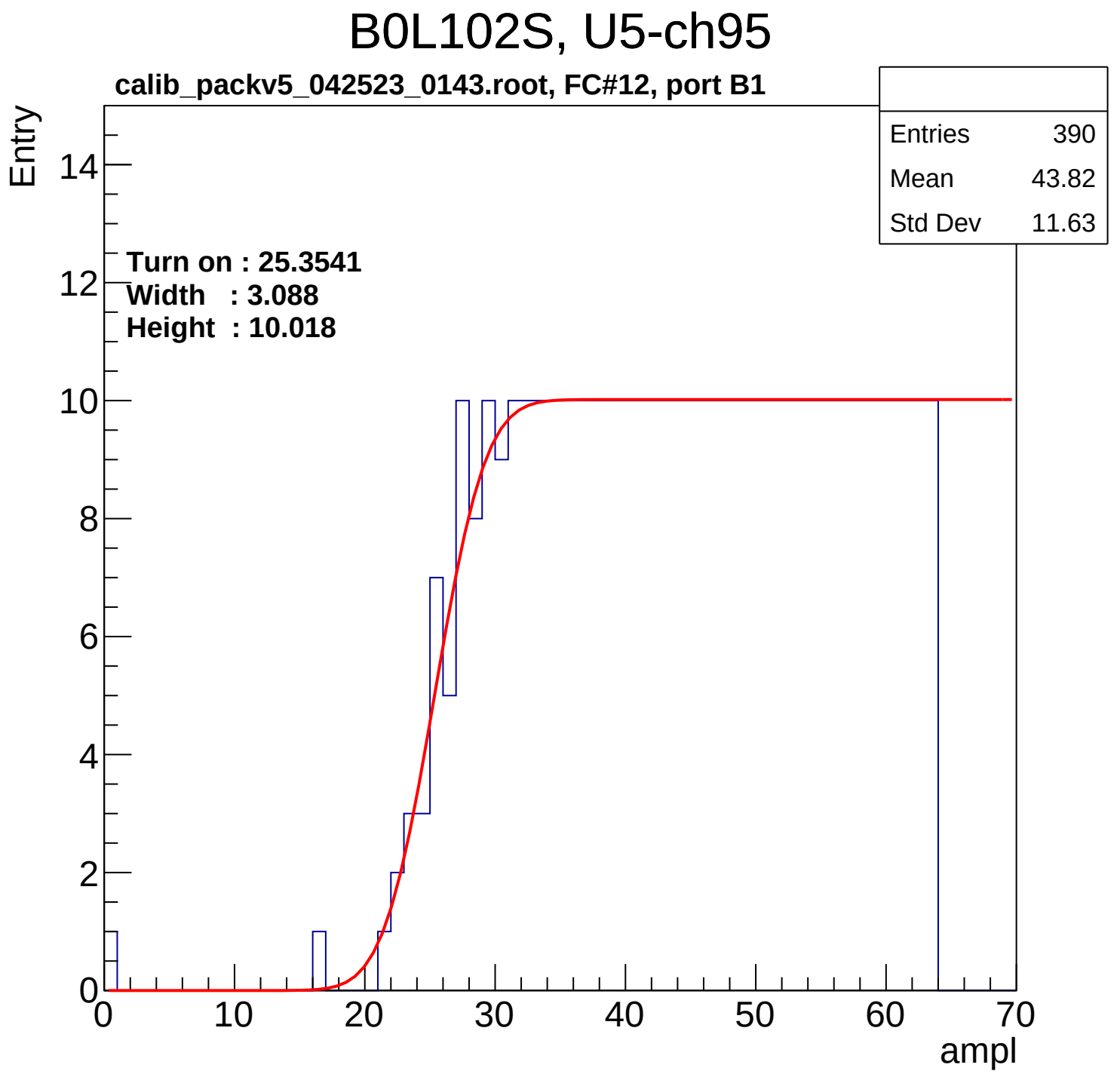
B0L102S, U5-ch95
calib_packv5_042523_0143.root, FC#12, port B1
Entries 390
Mean 43.82
Std Dev 11.63
Turn on : 25.3541
Width : 3.088
Height : 10.018
Entry
ampl
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6
8
10
12
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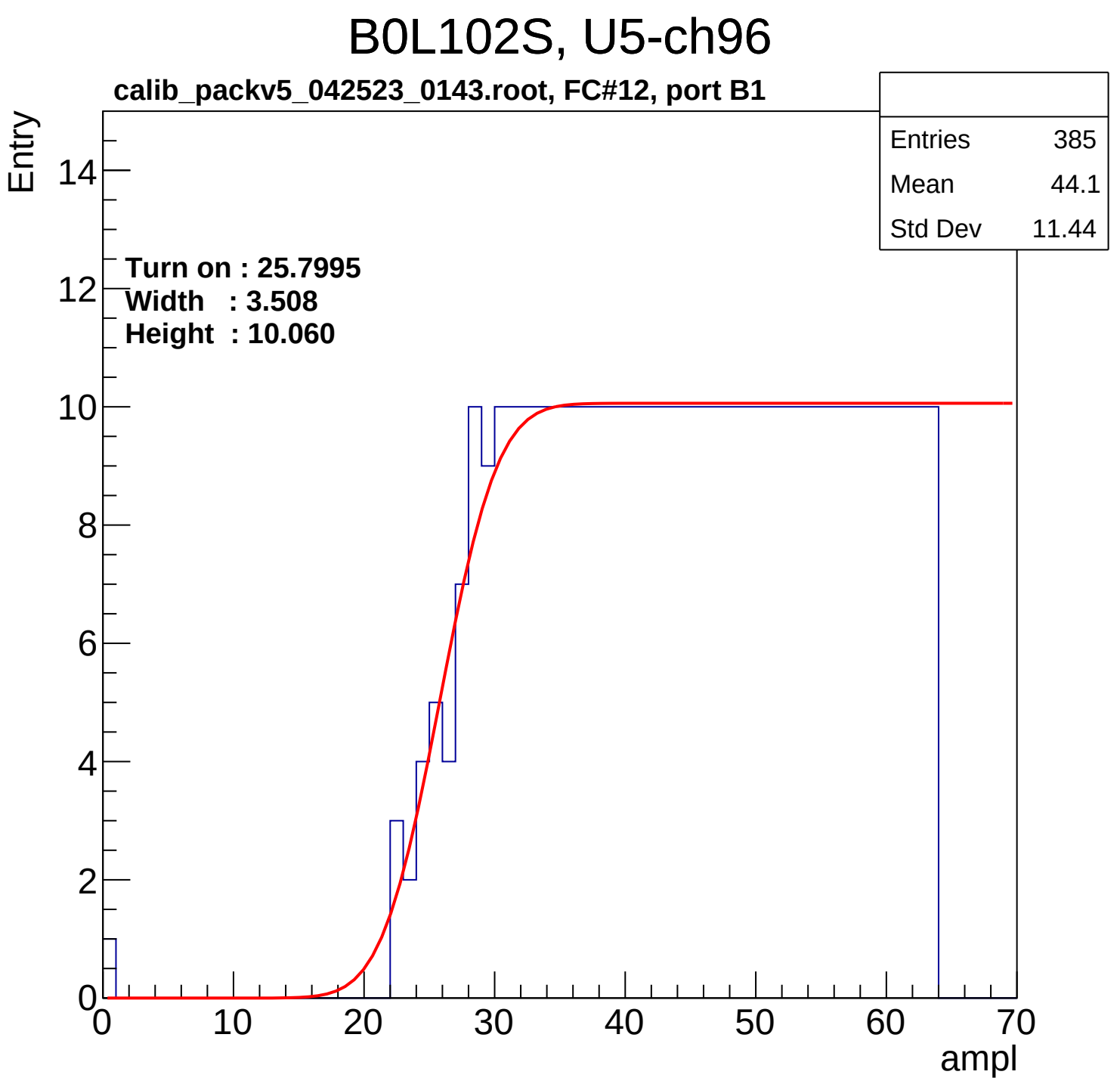
B0L102S, U5-ch96
calib_packv5_042523_0143.root, FC#12, port B1
Entries 385
Mean 44.1
Std Dev 11.44
Turn on : 25.7995
Width : 3.508
Height : 10.060
Entry
ampl
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6
8
10
12
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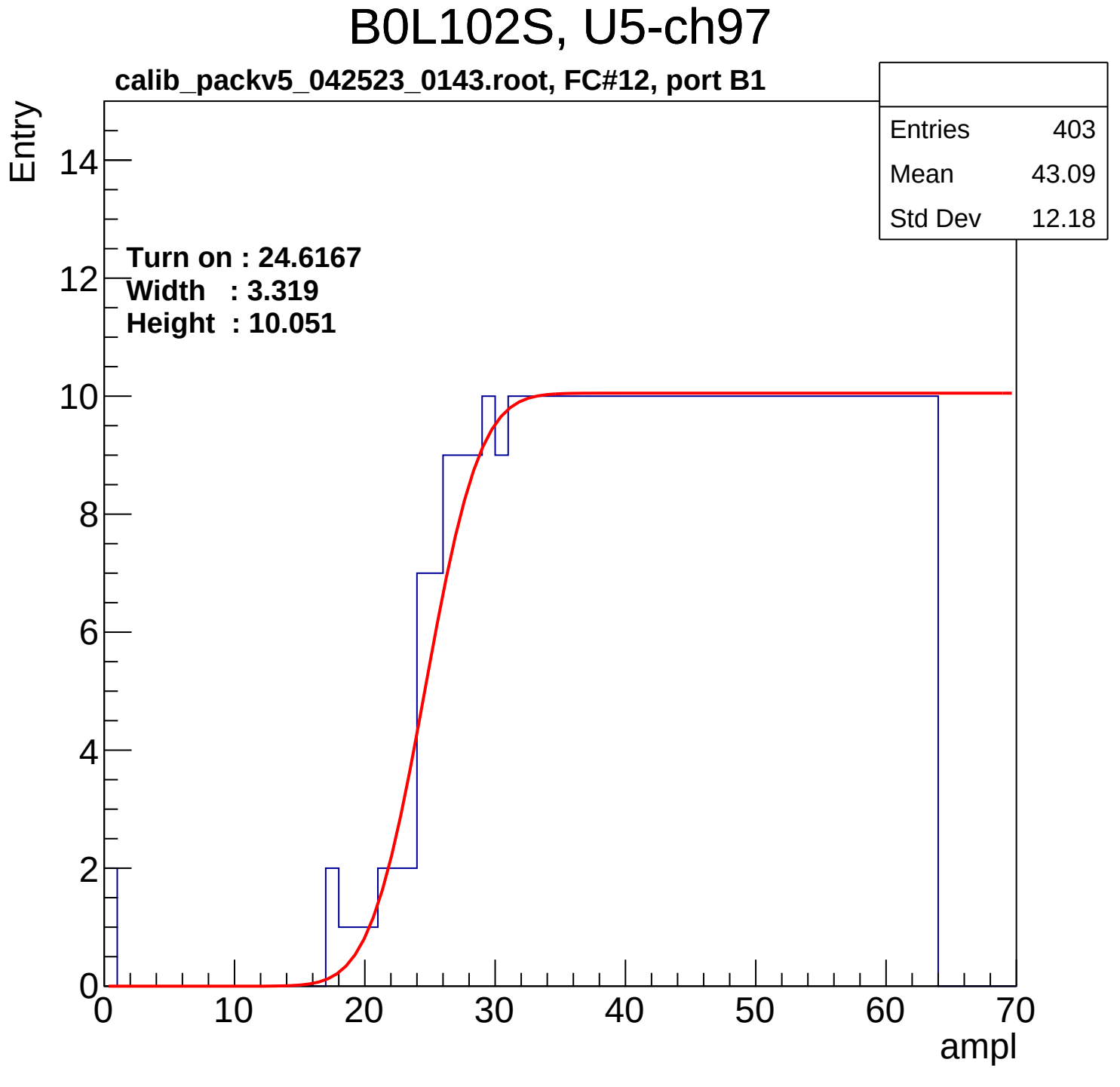
B0L102S, U5-ch97
calib_packv5_042523_0143.root, FC#12, port B1
Entries 403
Mean 43.09
Std Dev 12.18
Turn on : 24.6167
Width : 3.319
Height : 10.051
Entry
ampl
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6
8
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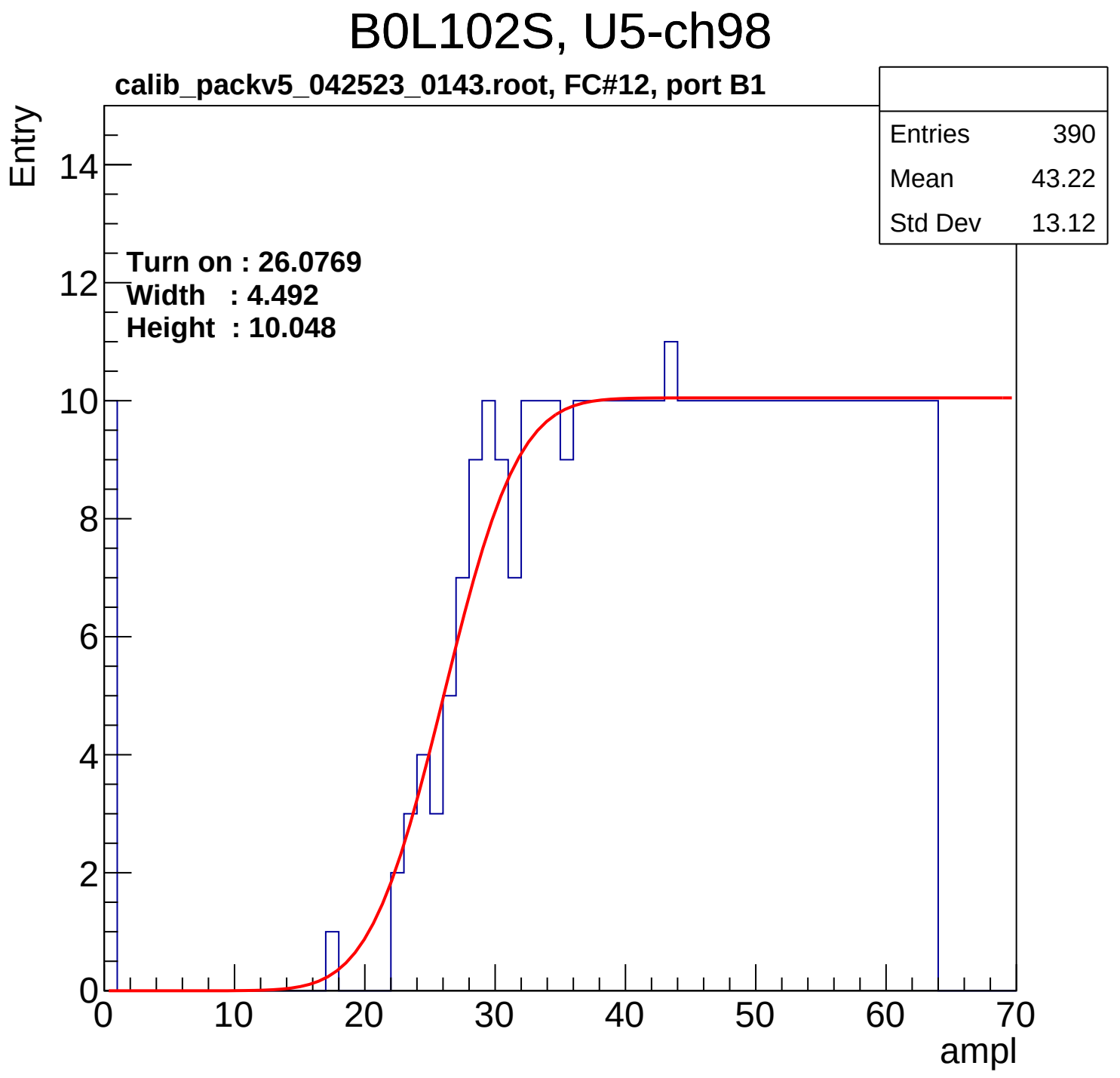
B0L102S, U5-ch98
calib_packv5_042523_0143.root, FC#12, port B1
Entries 390
Mean 43.22
Std Dev 13.12
Turn on : 26.0769
Width : 4.492
Height : 10.048
Entry
ampl
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6
8
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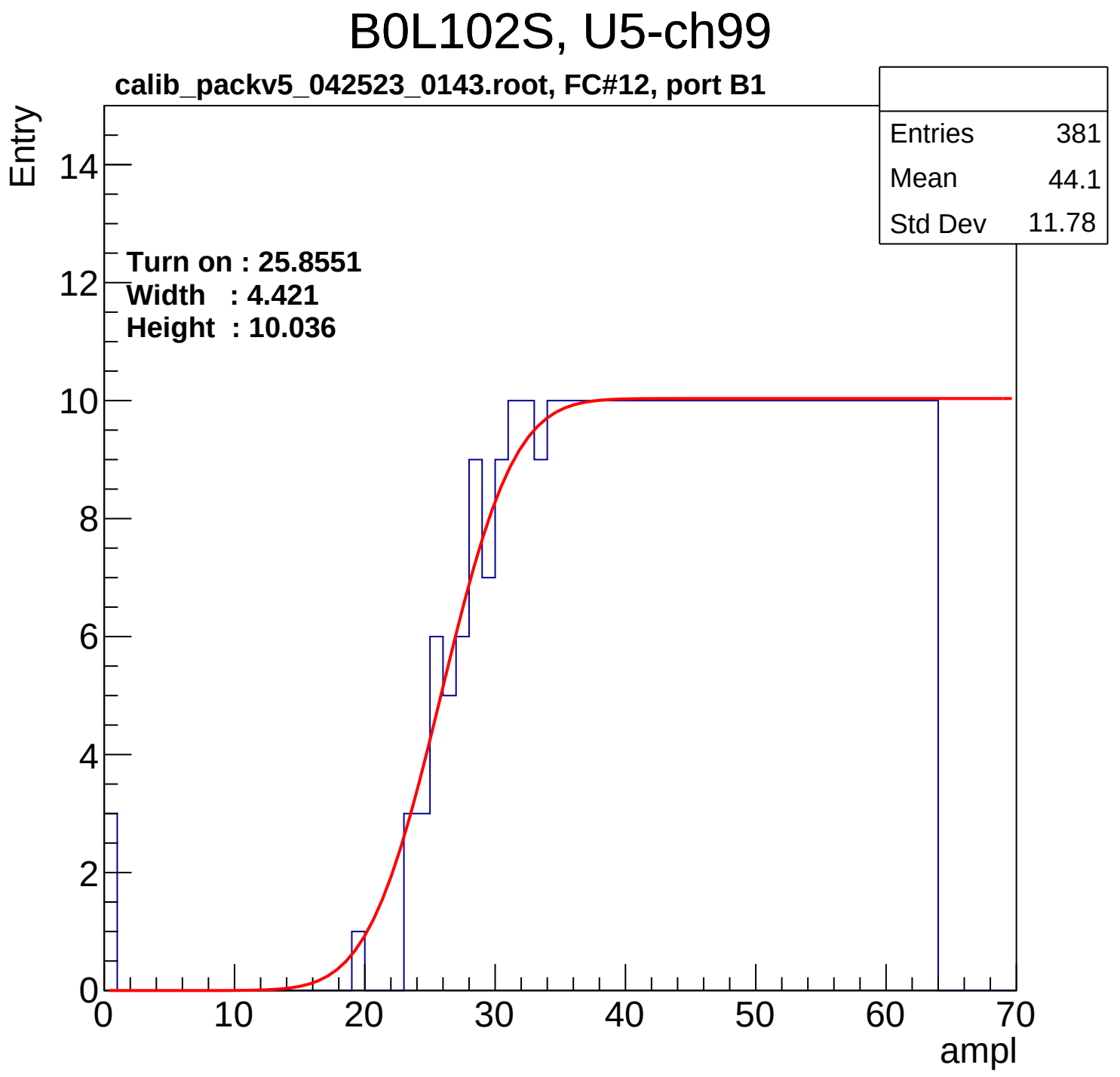
B0L102S, U5-ch99
calib_packv5_042523_0143.root, FC#12, port B1
Entries 381
Mean 44.1
Std Dev 11.78
Turn on : 25.8551
Width : 4.421
Height : 10.036
Entry
ampl
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8
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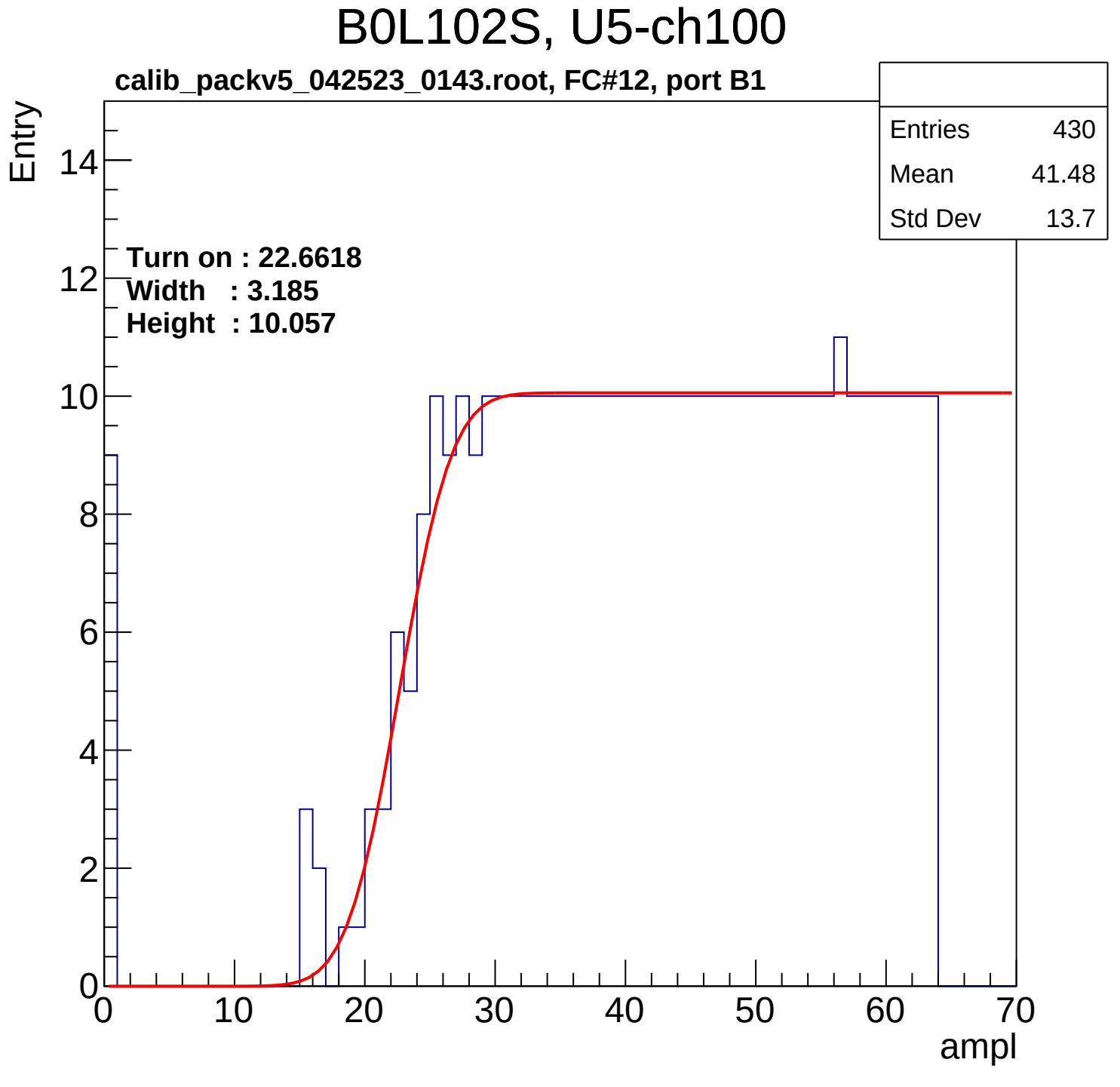
B0L102S, U5-ch100
calib_packv5_042523_0143.root, FC#12, port B1
Entries 430
Mean 41.48
Std Dev 13.7
Turn on : 22.6618
Width : 3.185
Height : 10.057
Entry
ampl
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6
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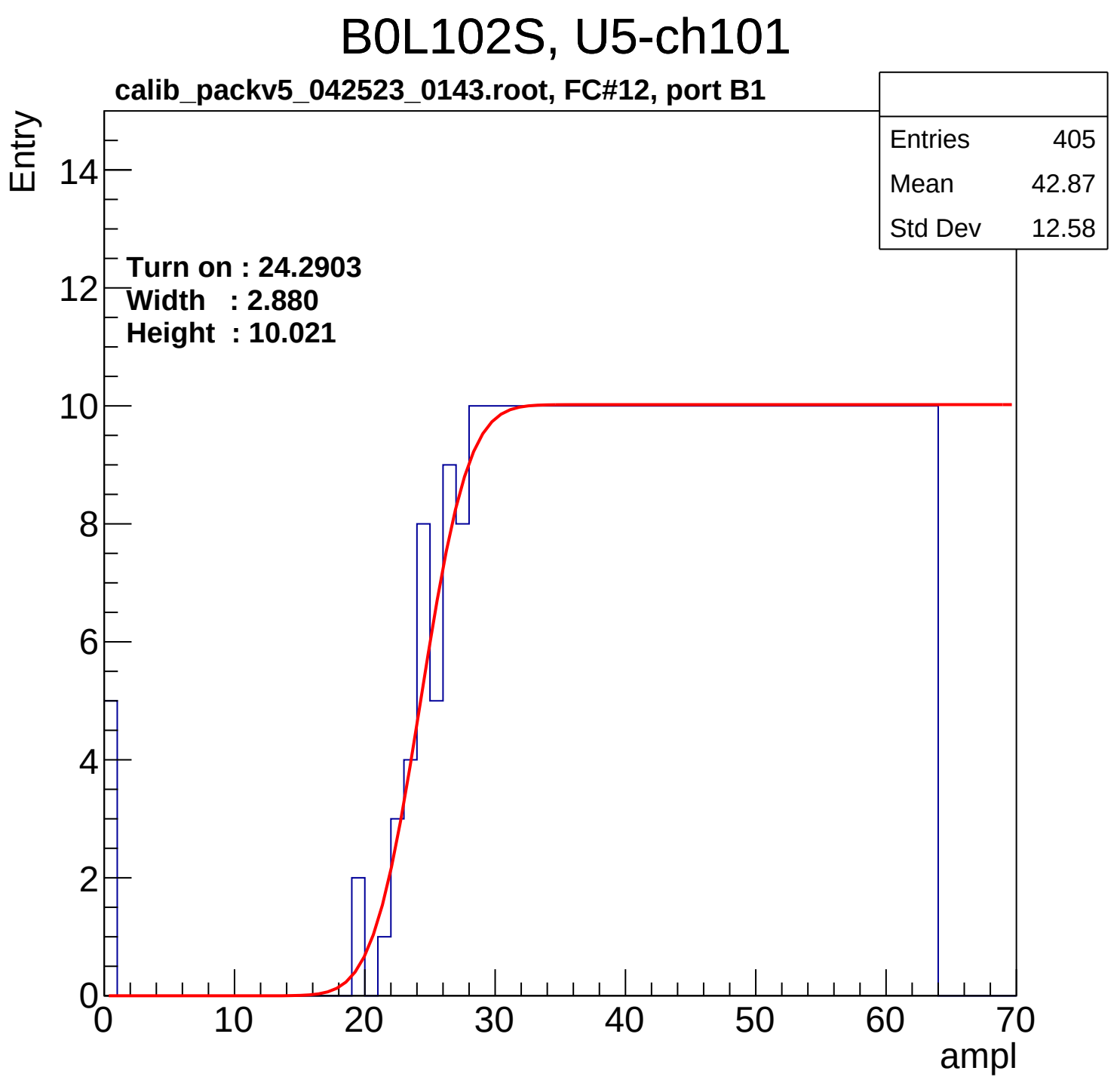
B0L102S, U5-ch101
calib_packv5_042523_0143.root, FC#12, port B1
Entries 405
Mean 42.87
Std Dev 12.58
Turn on : 24.2903
Width : 2.880
Height : 10.021
Entry
ampl
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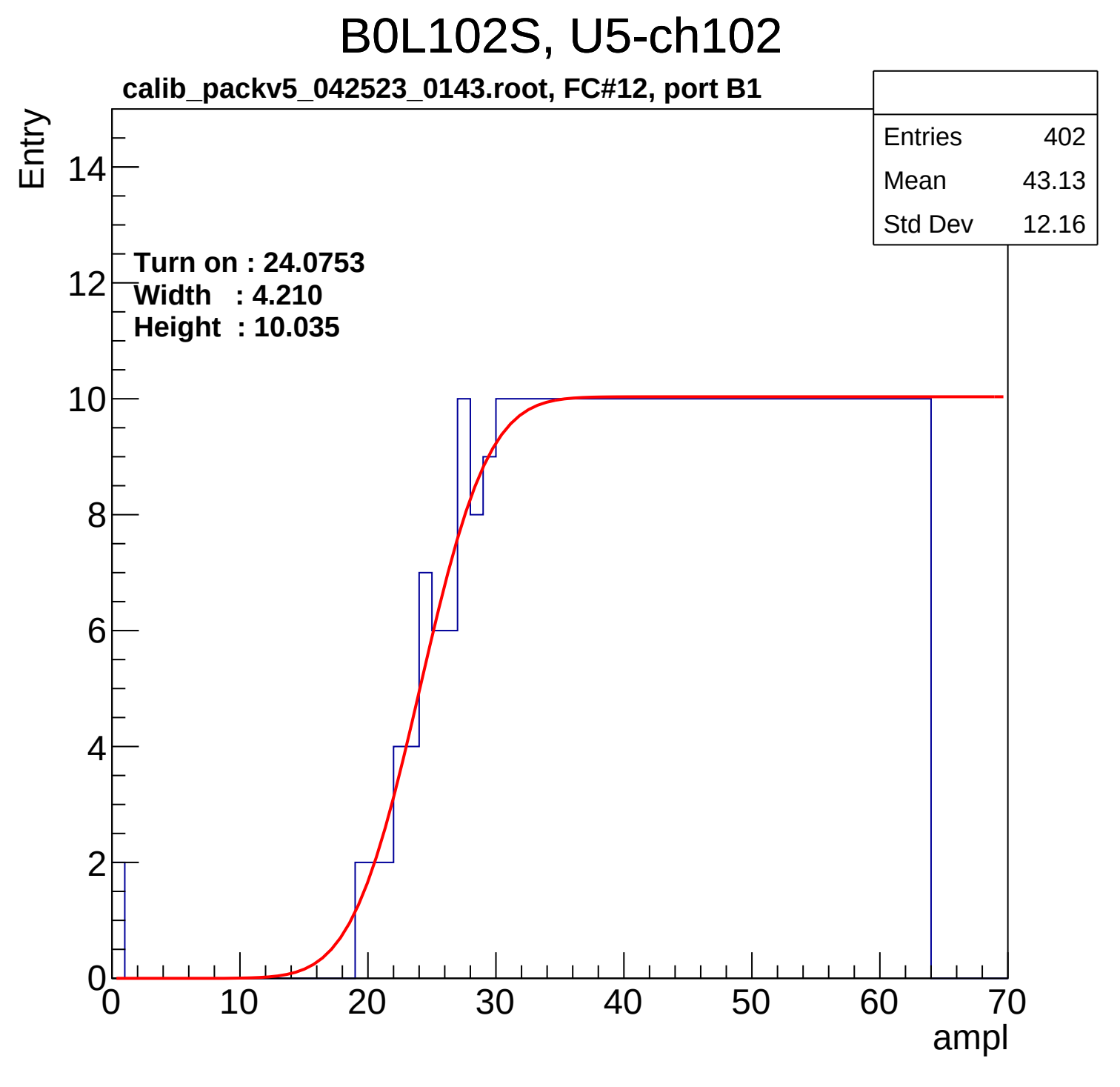
B0L102S, U5-ch102
calib_packv5_042523_0143.root, FC#12, port B1
Entries 402
Mean 43.13
Std Dev 12.16
Turn on : 24.0753
Width : 4.210
Height : 10.035
Entry
ampl
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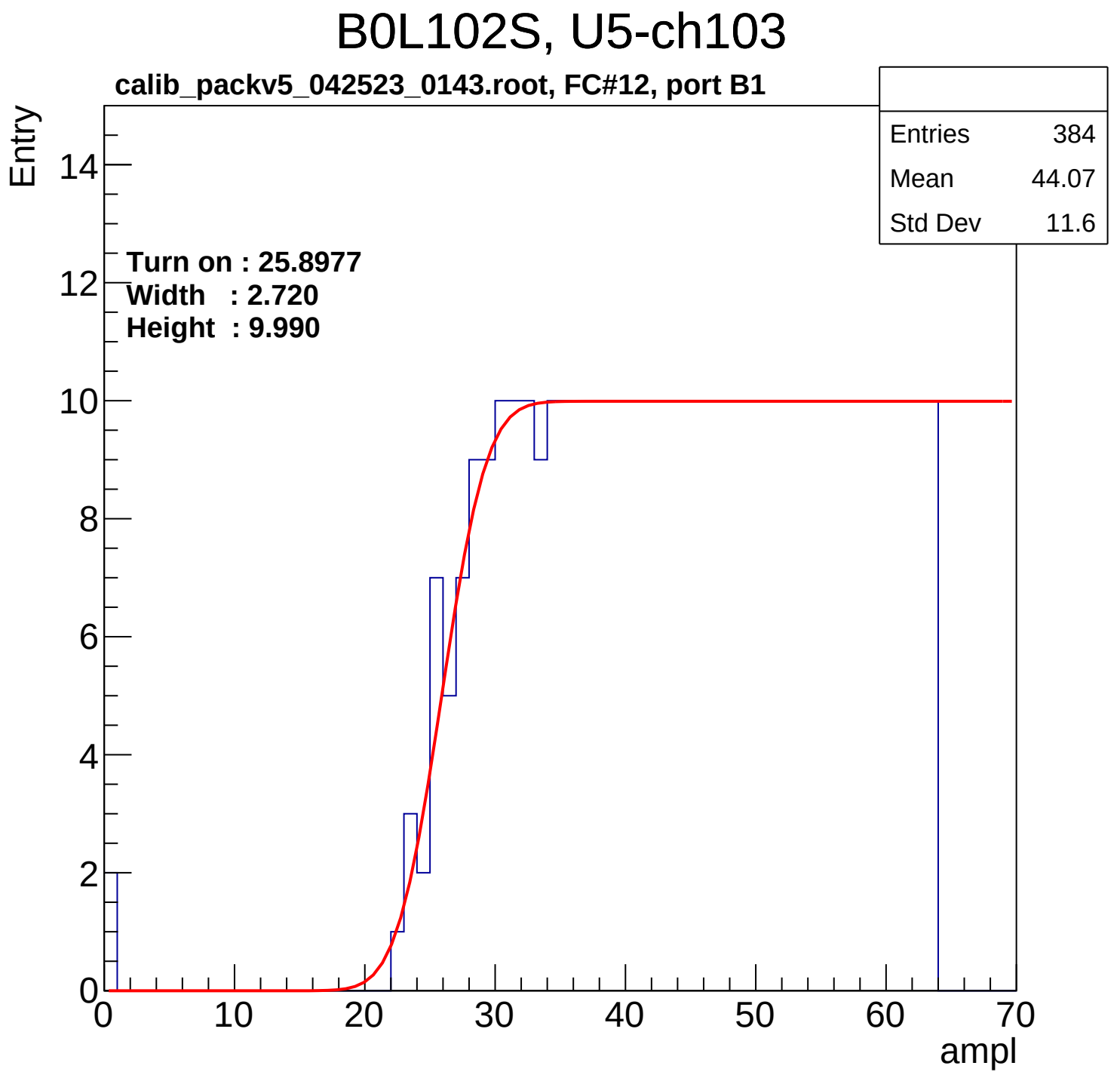
B0L102S, U5-ch103
calib_packv5_042523_0143.root, FC#12, port B1
Entries 384
Mean 44.07
Std Dev 11.6
Turn on : 25.8977
Width : 2.720
Height : 9.990
Entry
ampl
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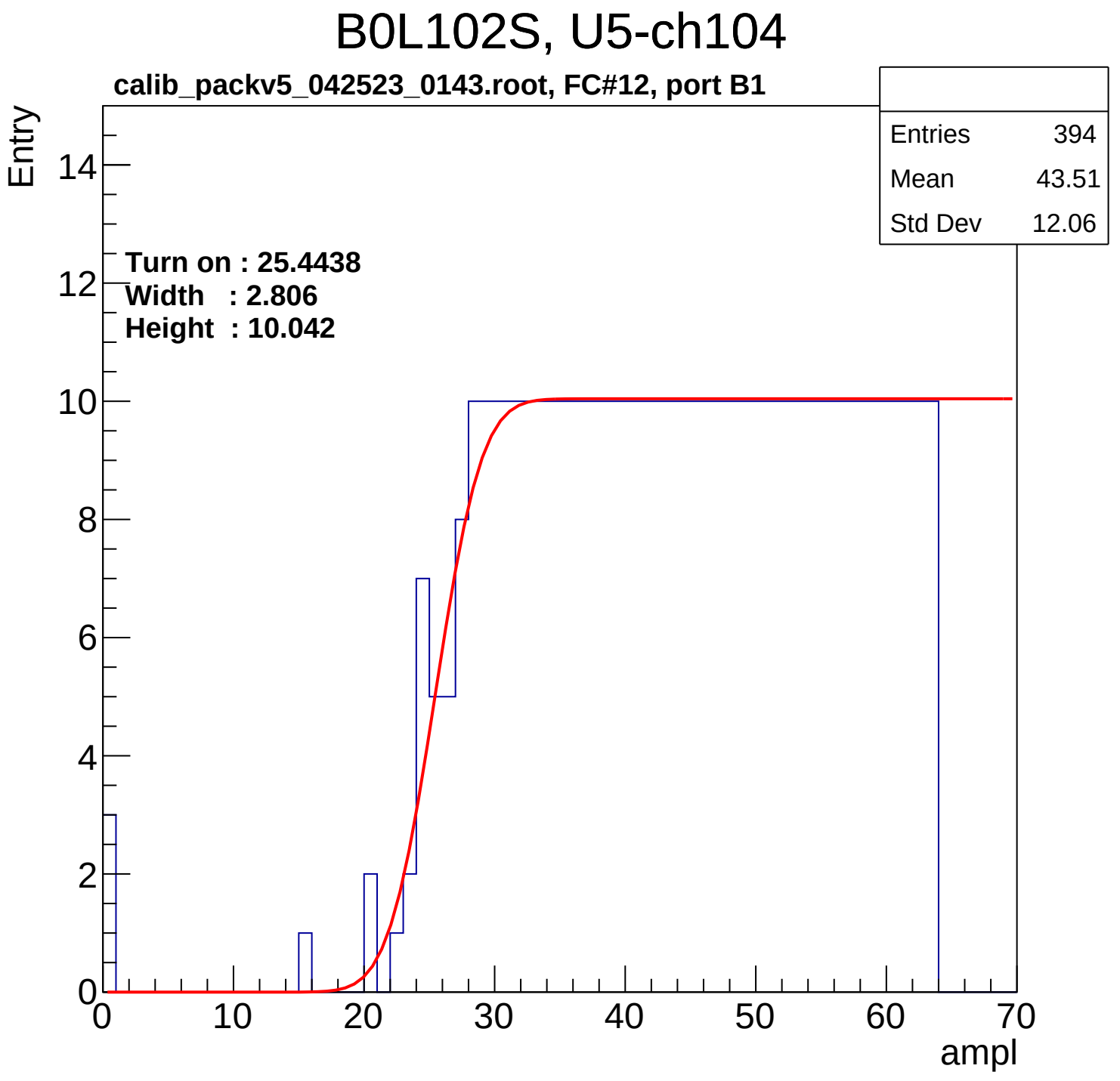
B0L102S, U5-ch104
calib_packv5_042523_0143.root, FC#12, port B1
Entries 394
Mean 43.51
Std Dev 12.06
Turn on : 25.4438
Width : 2.806
Height : 10.042
Entry
ampl
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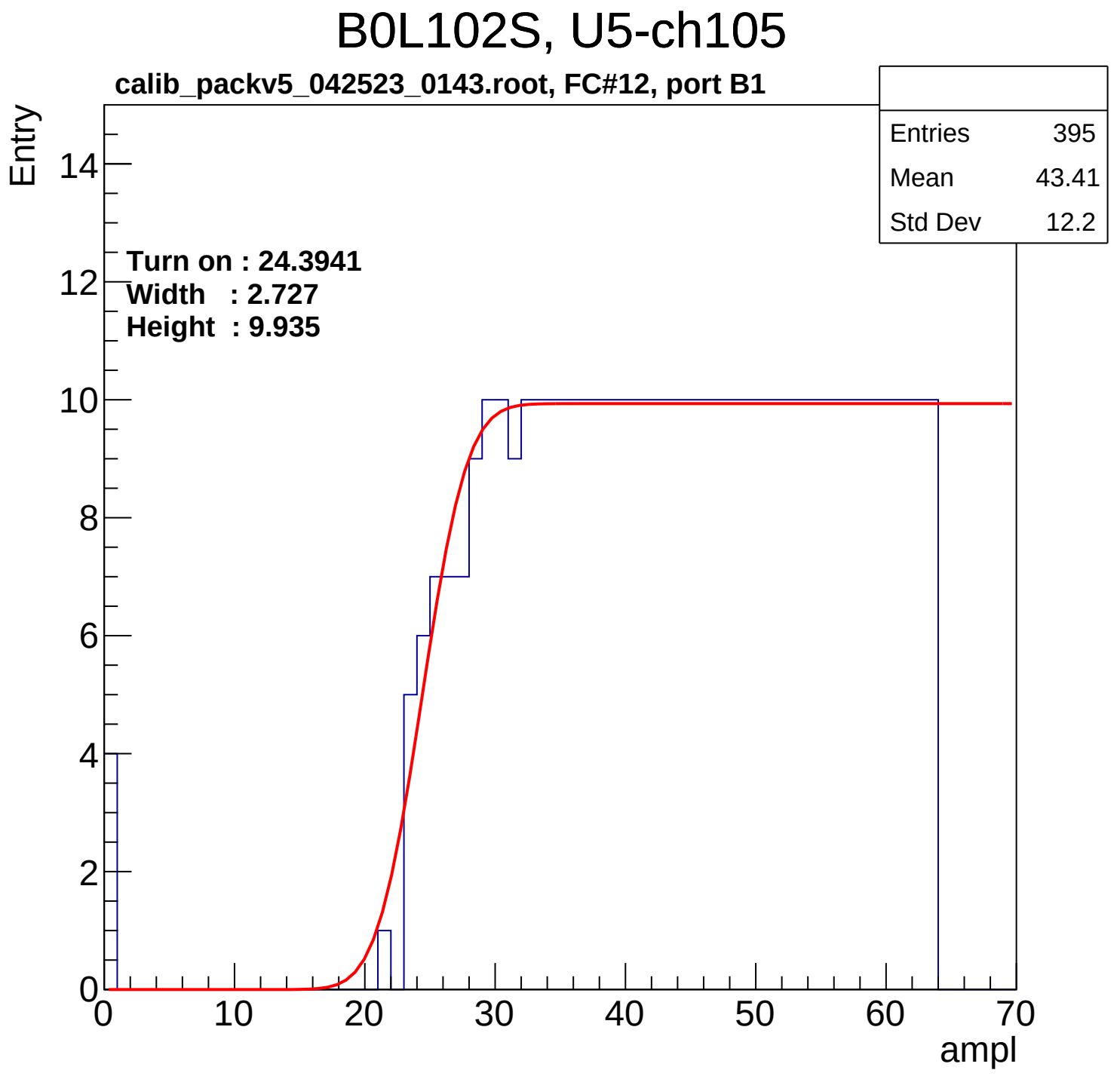
B0L102S, U5-ch105
calib_packv5_042523_0143.root, FC#12, port B1
Entries 395
Mean 43.41
Std Dev 12.2
Turn on : 24.3941
Width : 2.727
Height : 9.935
Entry
ampl
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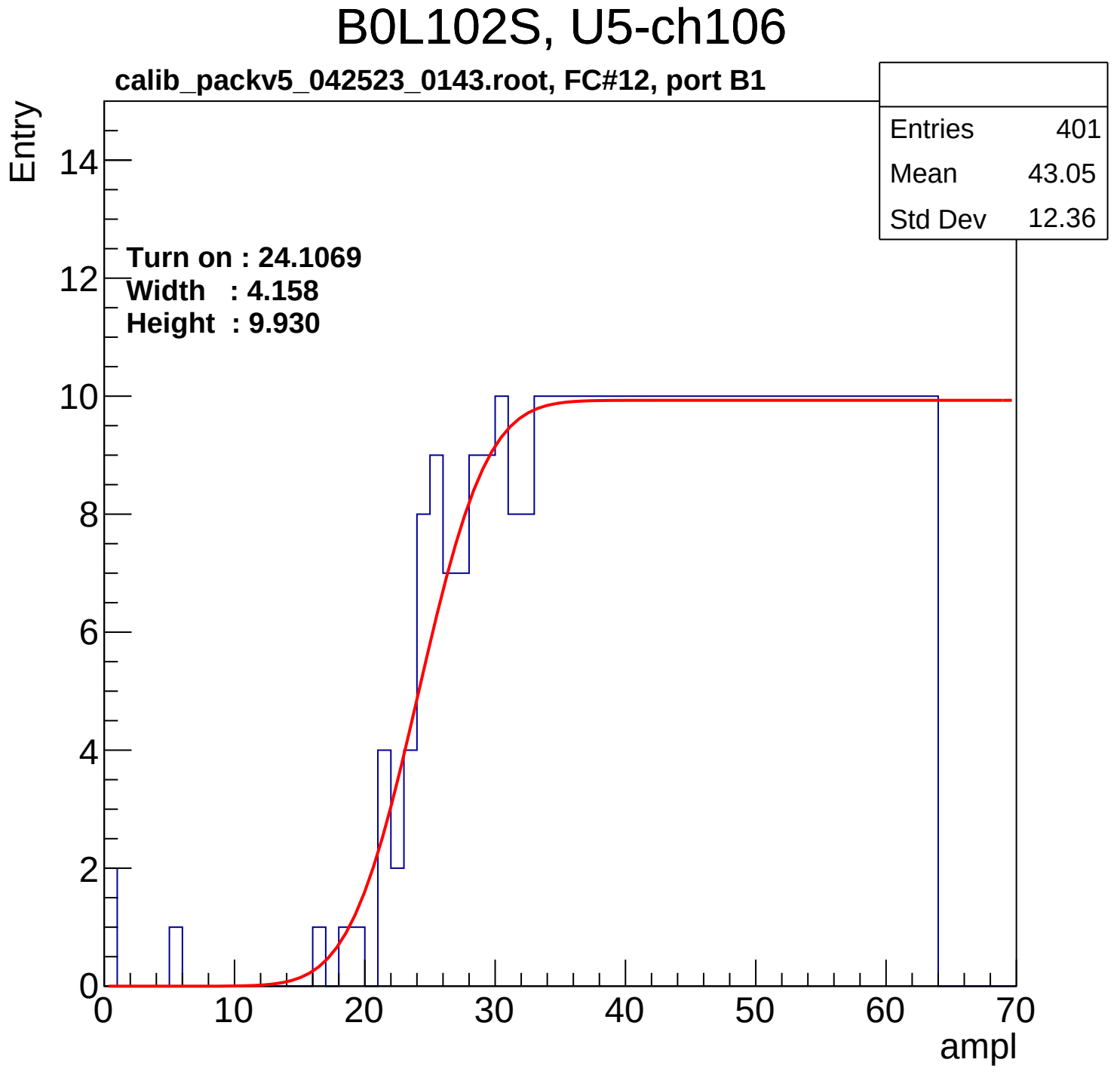
B0L102S, U5-ch106
calib_packv5_042523_0143.root, FC#12, port B1
Entries 401
Mean 43.05
Std Dev 12.36
Turn on : 24.1069
Width : 4.158
Height : 9.930
Entry
ampl
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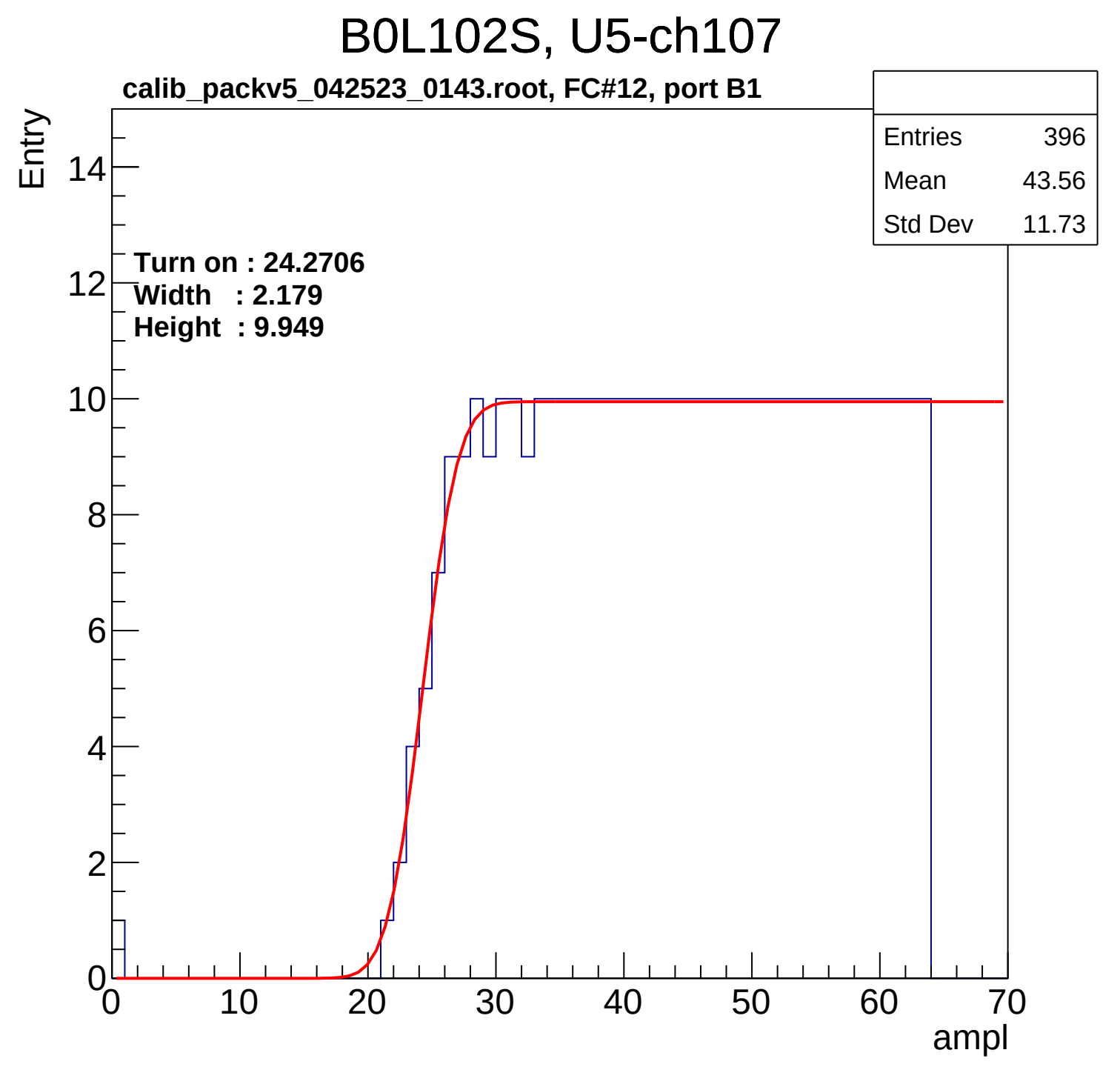
B0L102S, U5-ch107
calib_packv5_042523_0143.root, FC#12, port B1
Entries 396
Mean 43.56
Std Dev 11.73
Turn on : 24.2706
Width : 2.179
Height : 9.949
Entry
ampl
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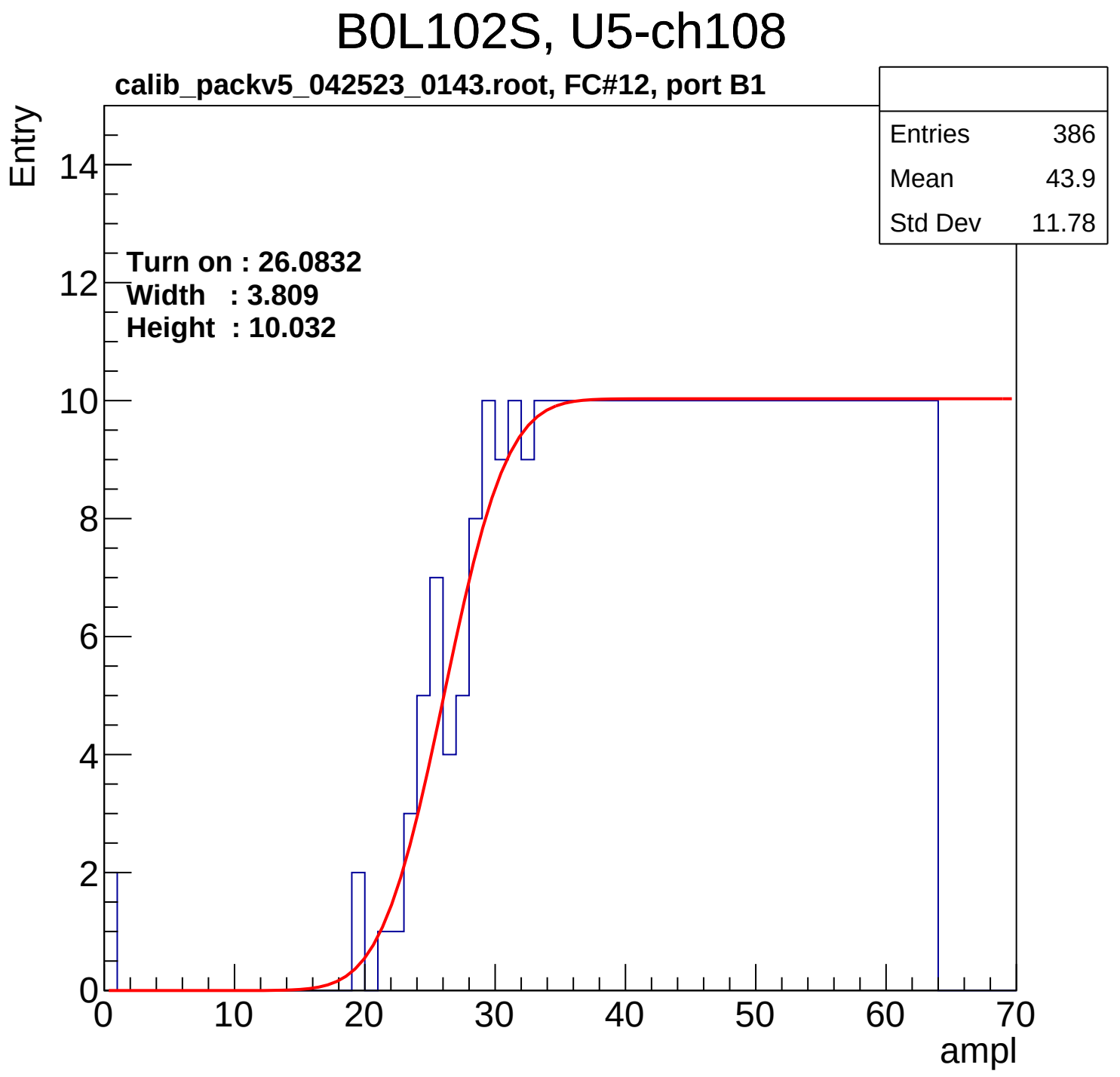
B0L102S, U5-ch108
calib_packv5_042523_0143.root, FC#12, port B1
Entries 386
Mean 43.9
Std Dev 11.78
Turn on : 26.0832
Width : 3.809
Height : 10.032
Entry
ampl
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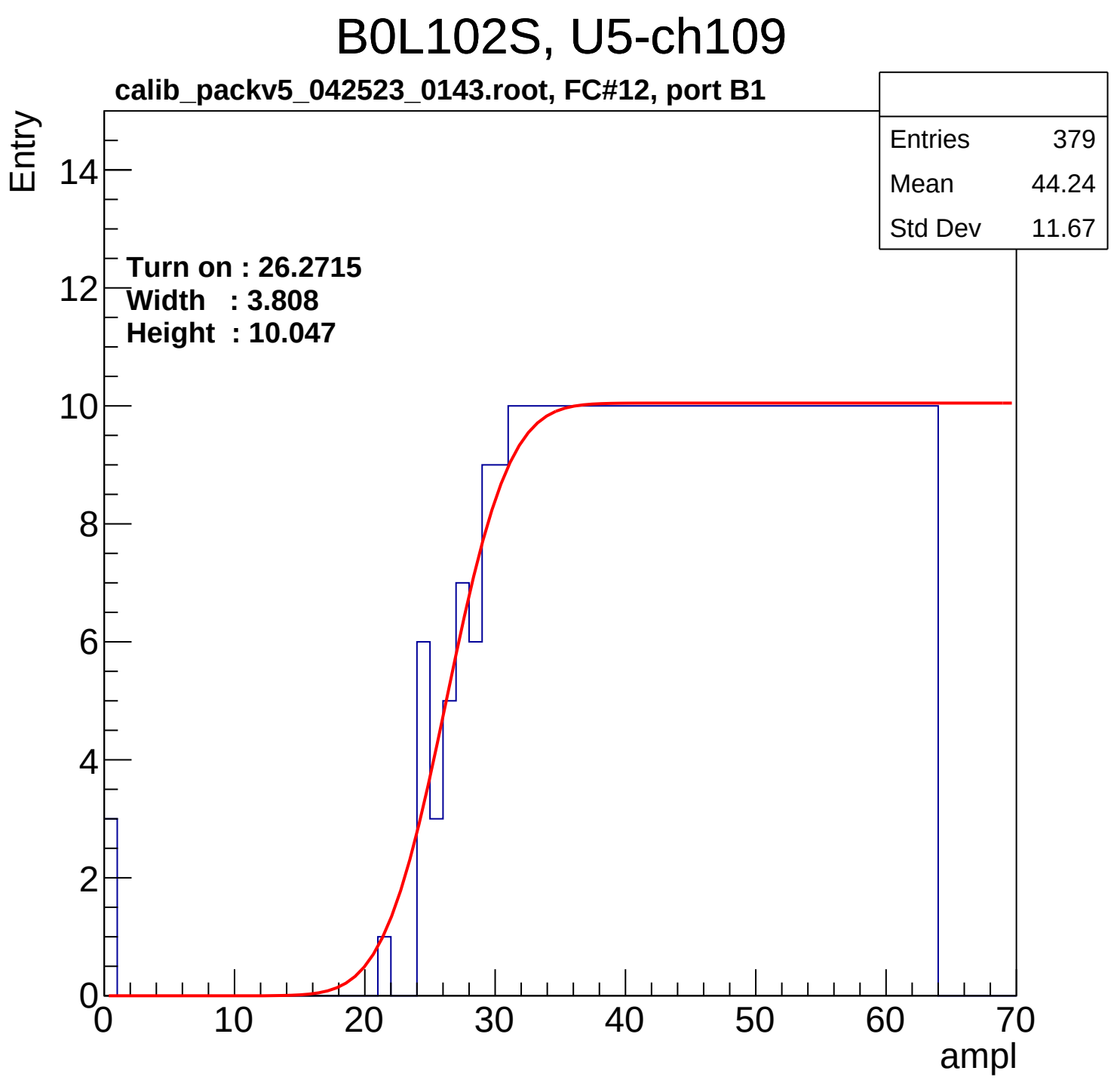
B0L102S, U5-ch109
calib_packv5_042523_0143.root, FC#12, port B1
Entries 379
Mean 44.24
Std Dev 11.67
Turn on : 26.2715
Width : 3.808
Height : 10.047
Entry
ampl
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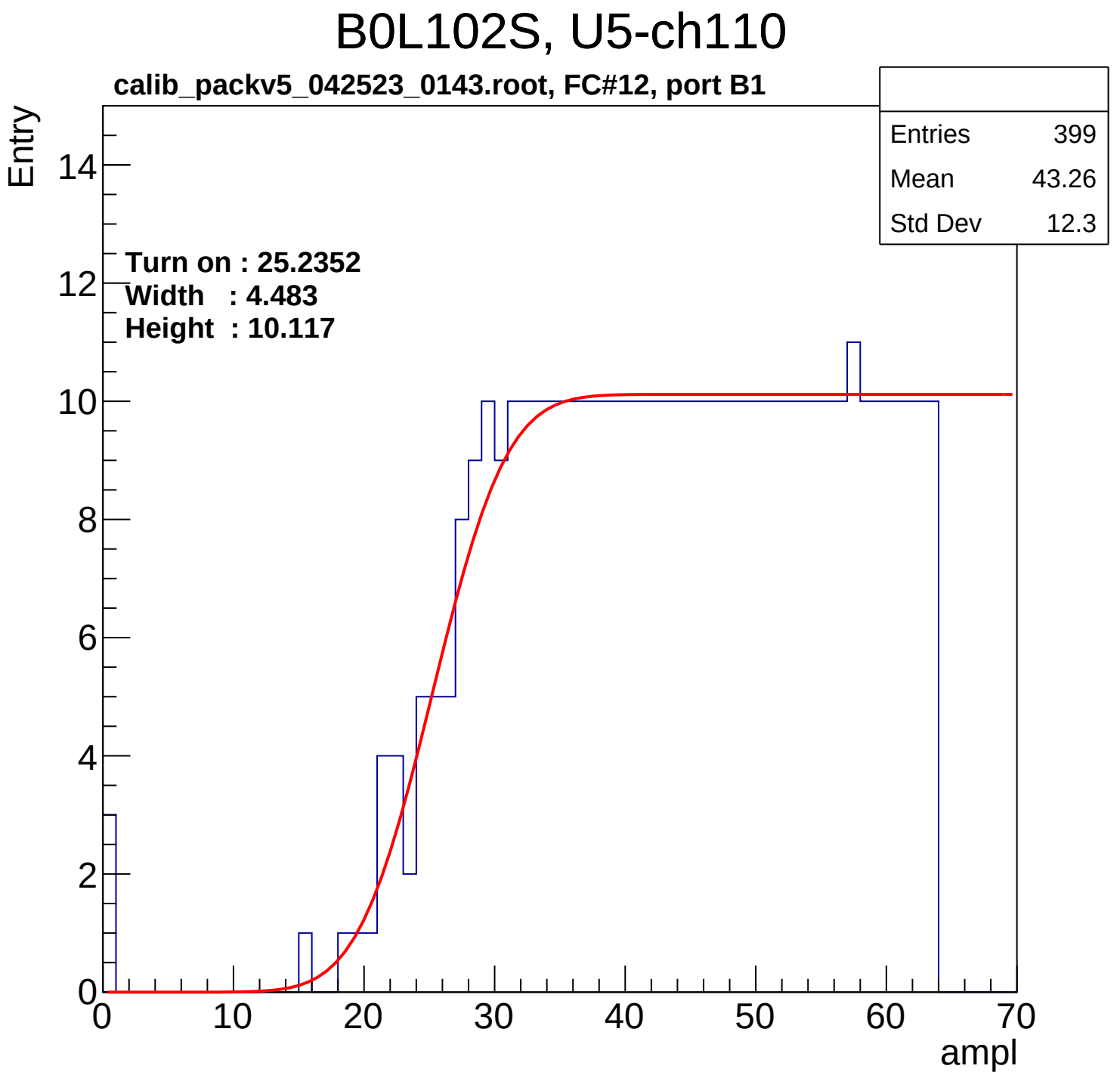
B0L102S, U5-ch110
calib_packv5_042523_0143.root, FC#12, port B1
Entries 399
Mean 43.26
Std Dev 12.3
Turn on : 25.2352
Width : 4.483
Height : 10.117
Entry
ampl
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8
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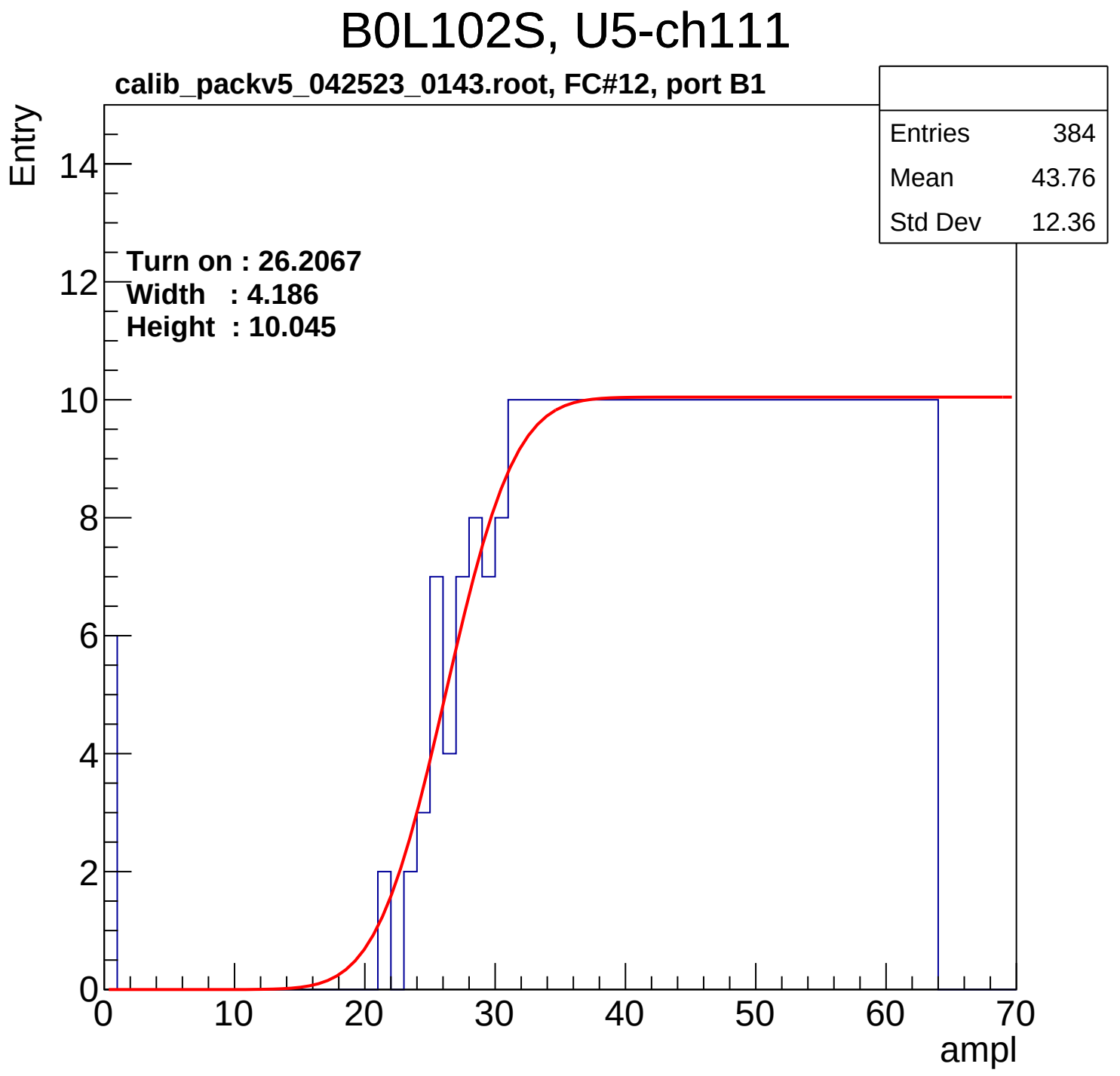
B0L102S, U5-ch111
calib_packv5_042523_0143.root, FC#12, port B1
Entries 384
Mean 43.76
Std Dev 12.36
Turn on : 26.2067
Width : 4.186
Height : 10.045
Entry
ampl
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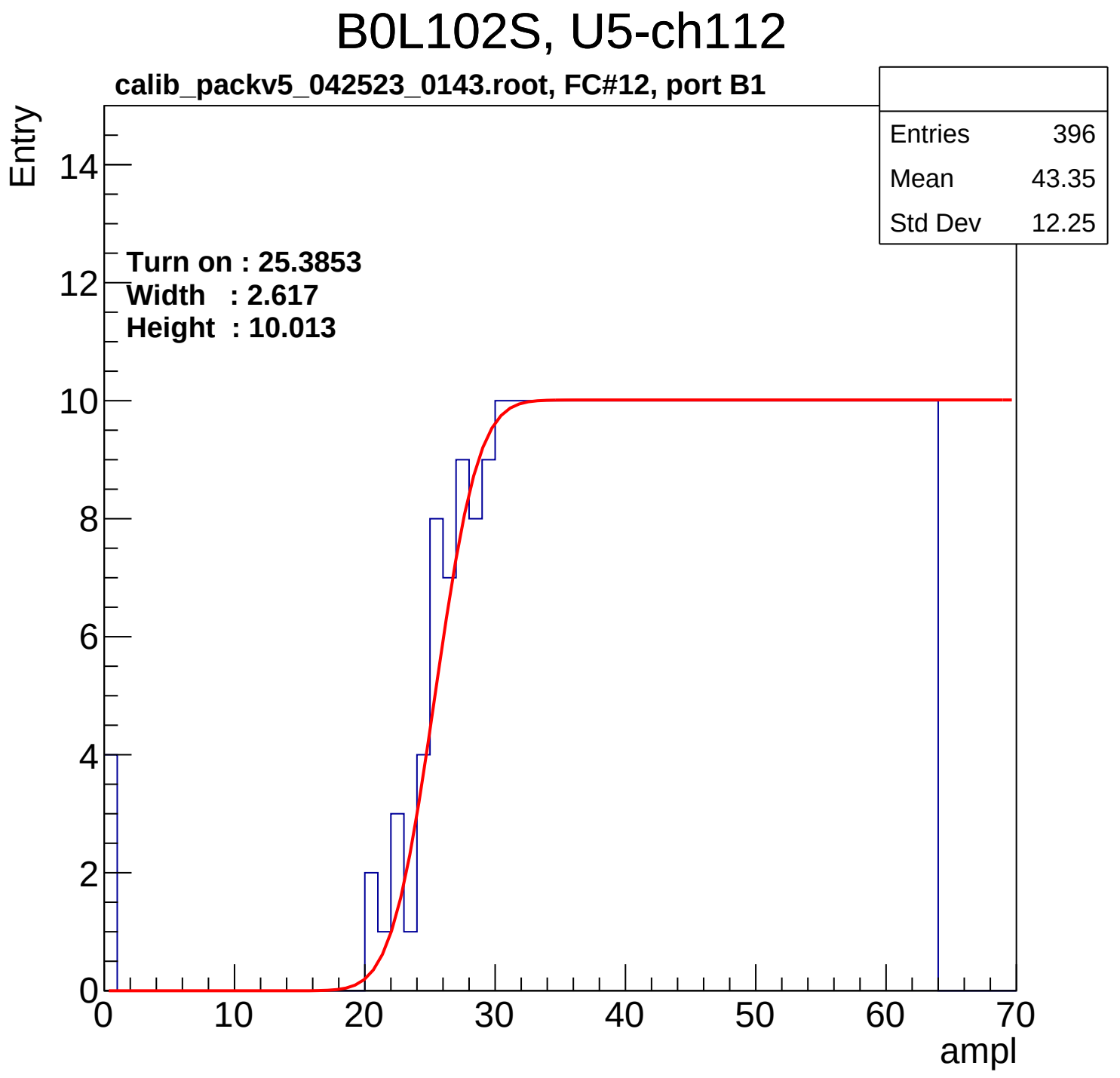
B0L102S, U5-ch112
calib_packv5_042523_0143.root, FC#12, port B1
Entries 396
Mean 43.35
Std Dev 12.25
Turn on : 25.3853
Width : 2.617
Height : 10.013
Entry
ampl
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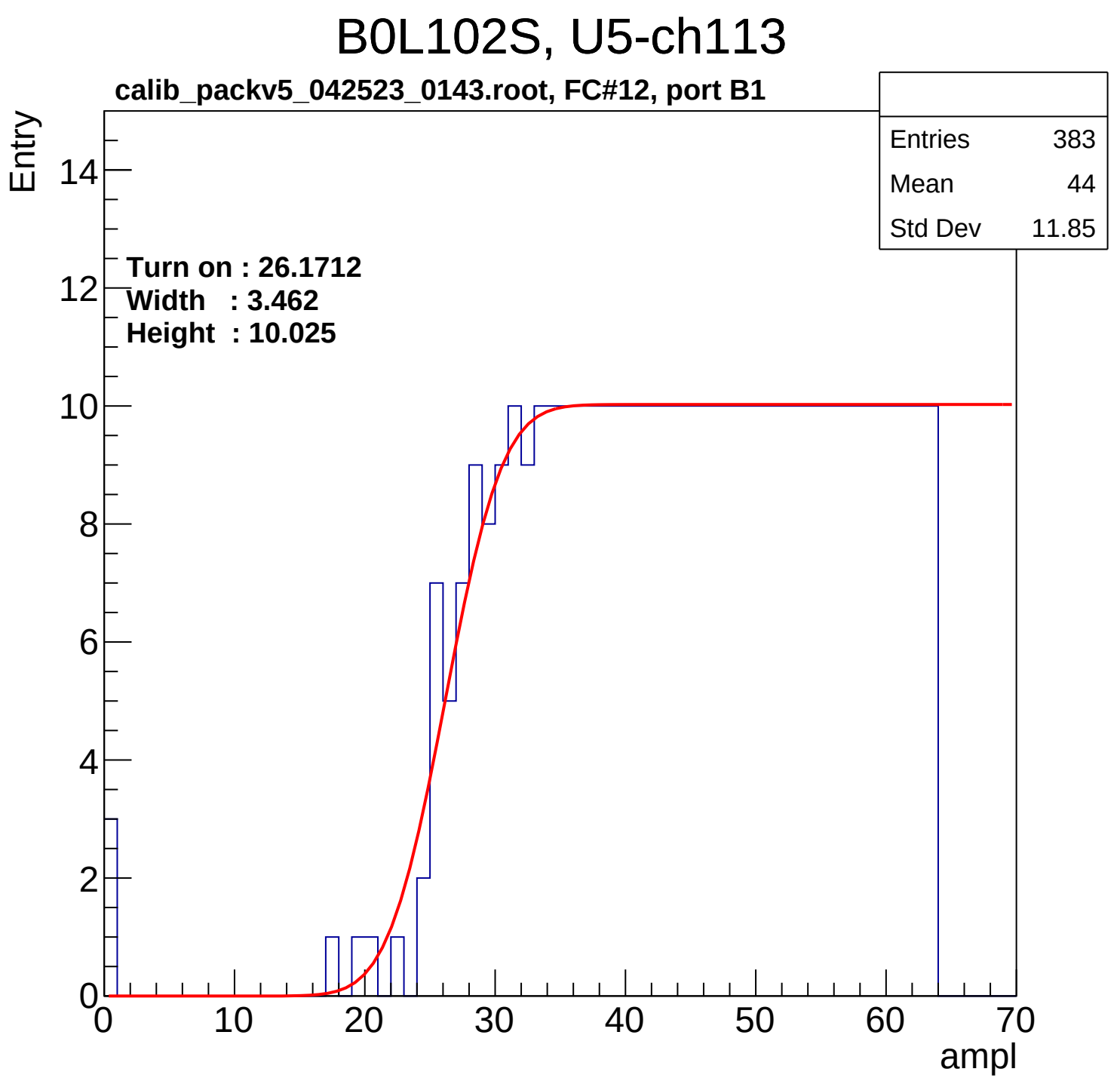
B0L102S, U5-ch113
calib_packv5_042523_0143.root, FC#12, port B1
Entries 383
Mean 44
Std Dev 11.85
Turn on : 26.1712
Width : 3.462
Height : 10.025
Entry
ampl
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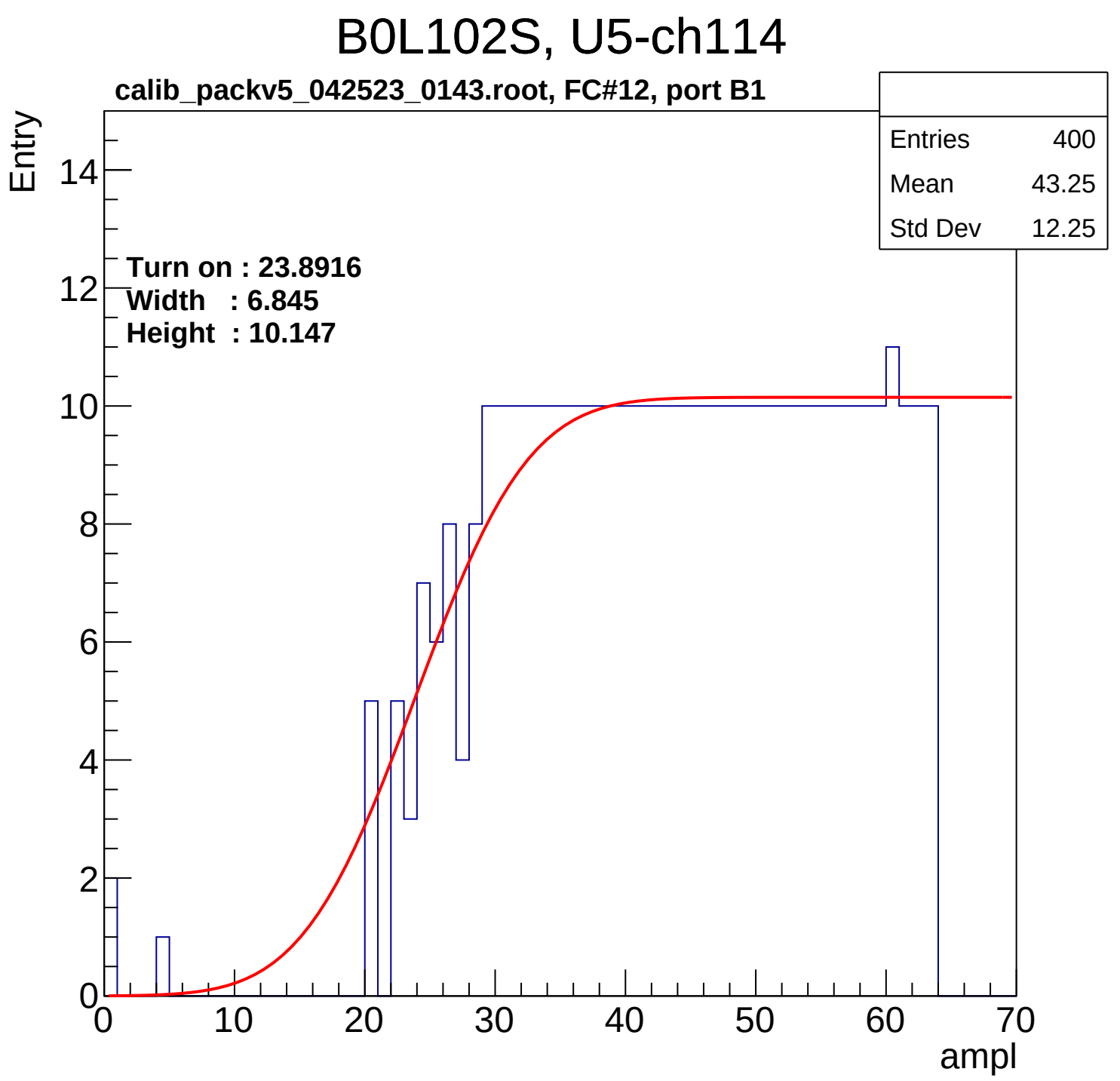
B0L102S, U5-ch114
calib_packv5_042523_0143.root, FC#12, port B1
Entries 400
Mean 43.25
Std Dev 12.25
Turn on : 23.8916
Width : 6.845
Height : 10.147
Entry
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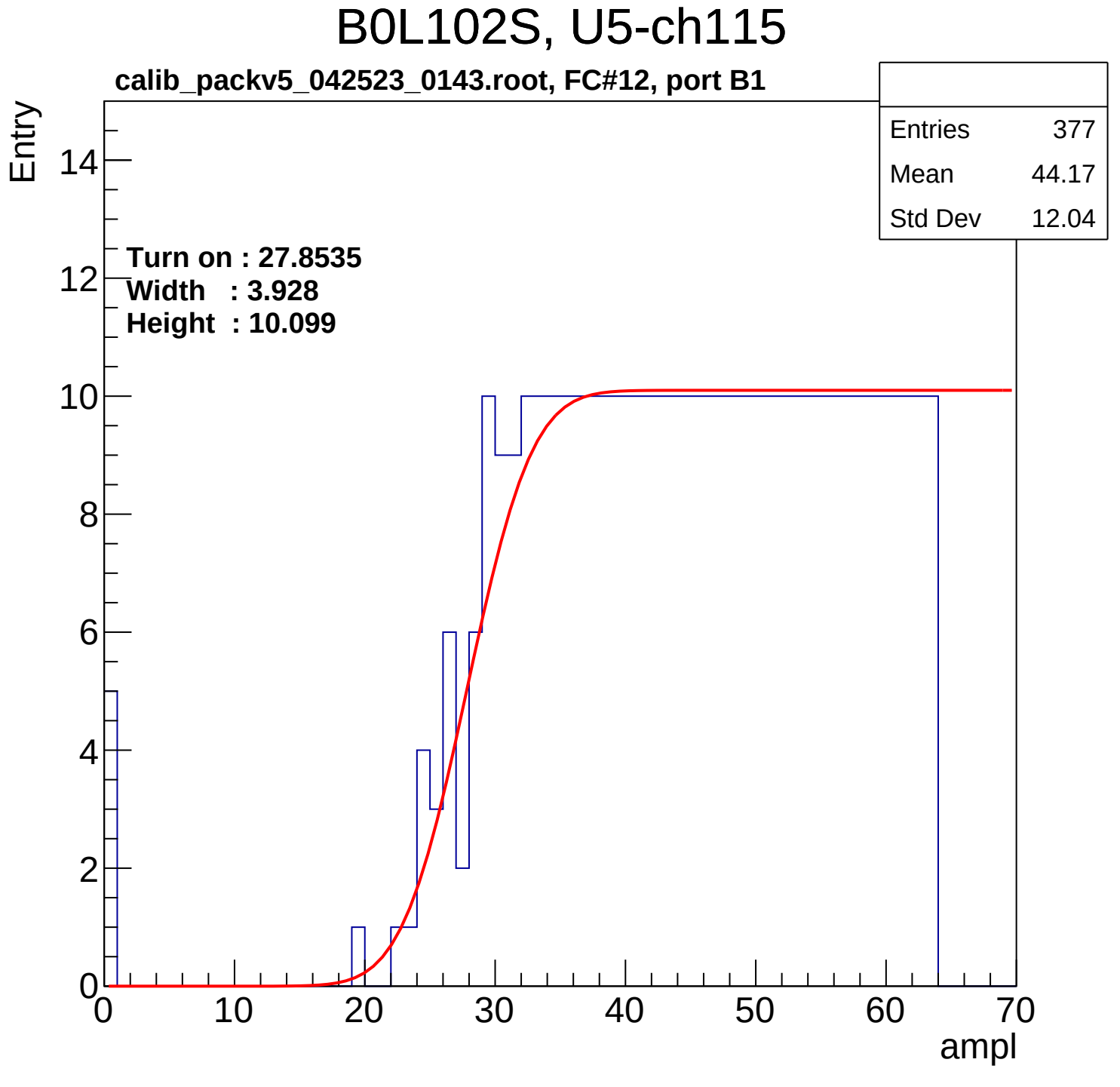
B0L102S, U5-ch115
calib_packv5_042523_0143.root, FC#12, port B1
Entries 377
Mean 44.17
Std Dev 12.04
Turn on : 27.8535
Width : 3.928
Height : 10.099
Entry
ampl
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4
6
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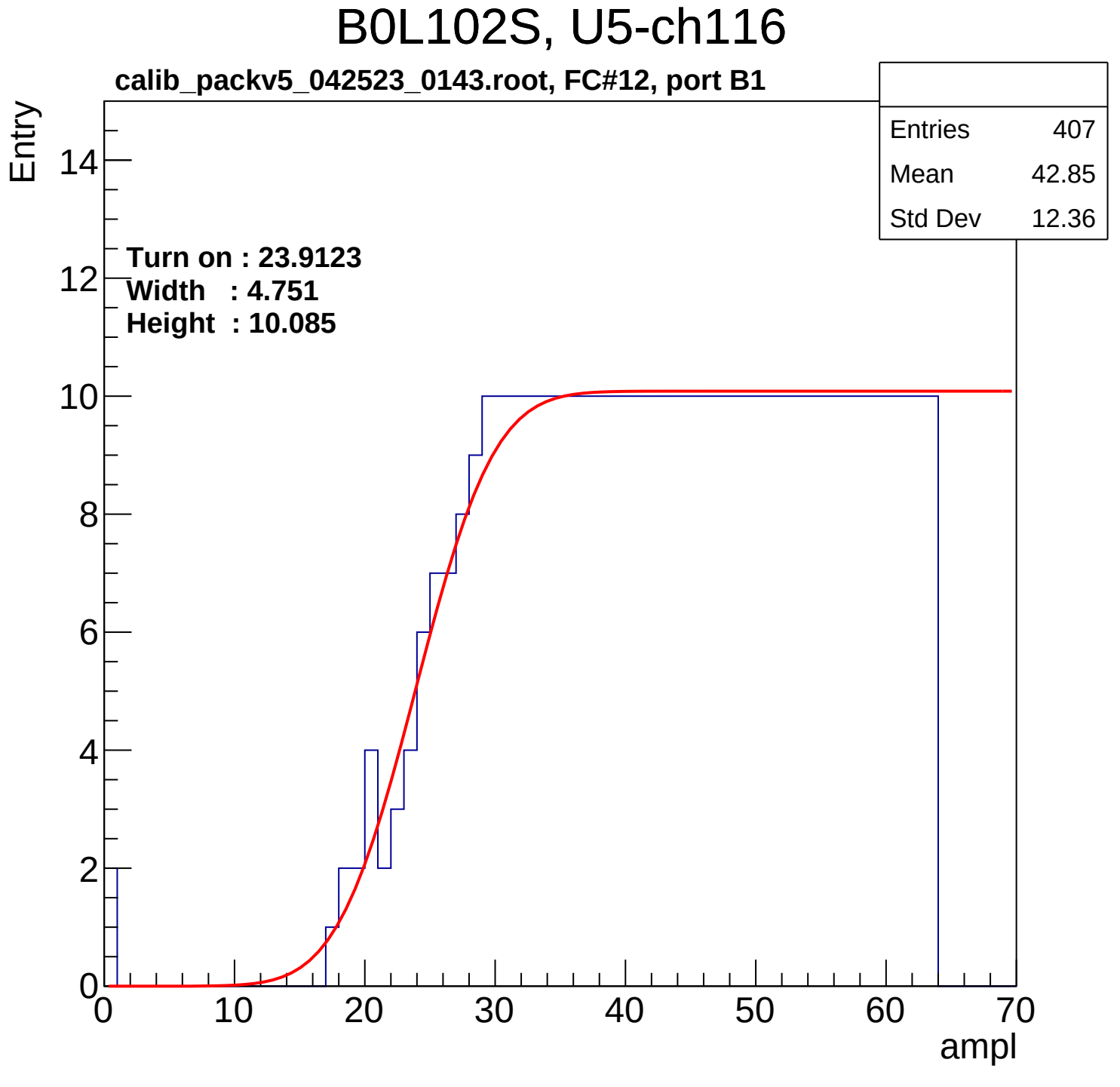
B0L102S, U5-ch116
calib_packv5_042523_0143.root, FC#12, port B1
Entries 407
Mean 42.85
Std Dev 12.36
Turn on : 23.9123
Width : 4.751
Height : 10.085
Entry
ampl
0
2
4
6
8
10
12
14
0
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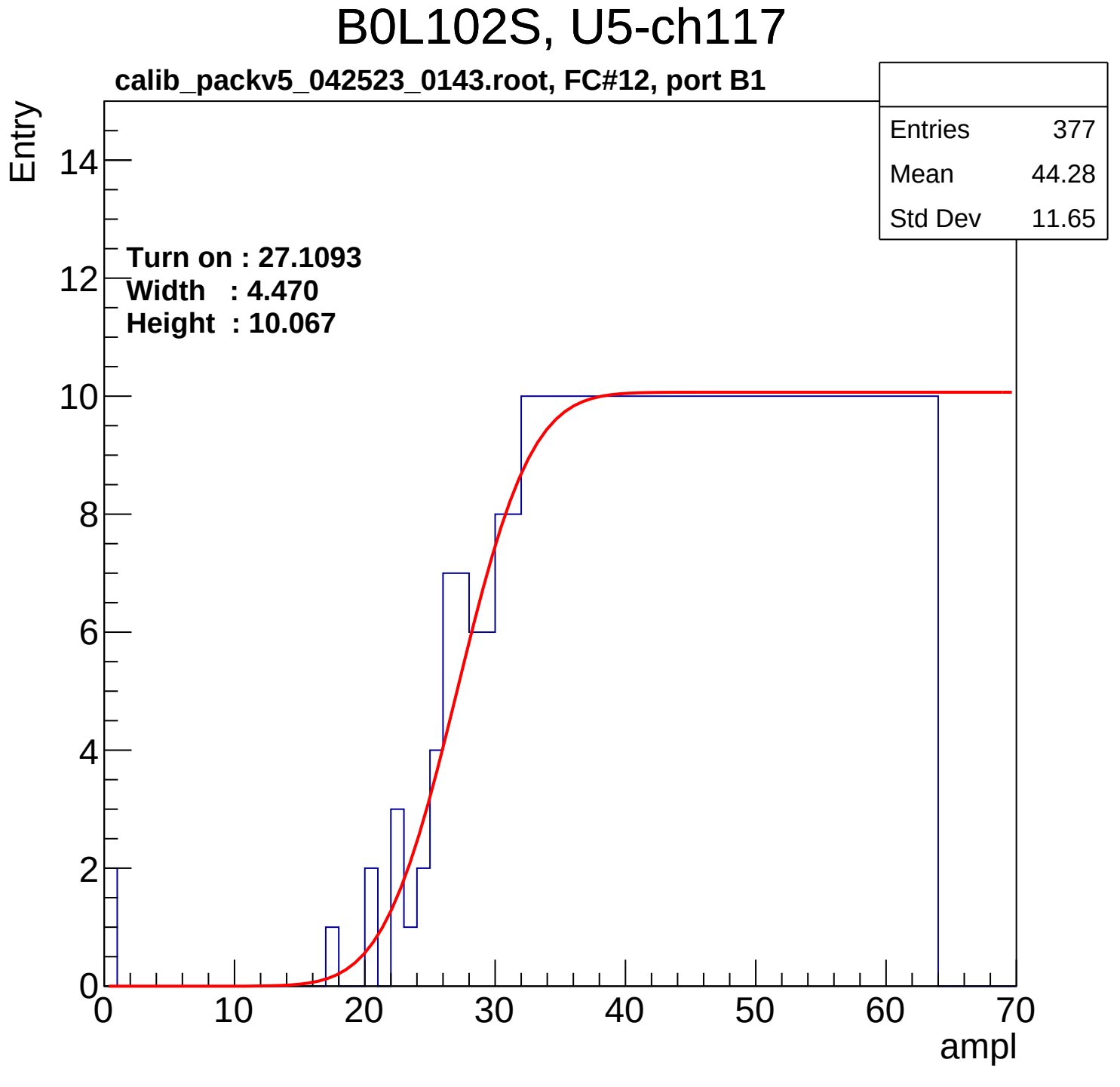
B0L102S, U5-ch117
calib_packv5_042523_0143.root, FC#12, port B1
Entries 377
Mean 44.28
Std Dev 11.65
Turn on : 27.1093
Width : 4.470
Height : 10.067
Entry
ampl
0
2
4
6
8
10
12
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0
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20
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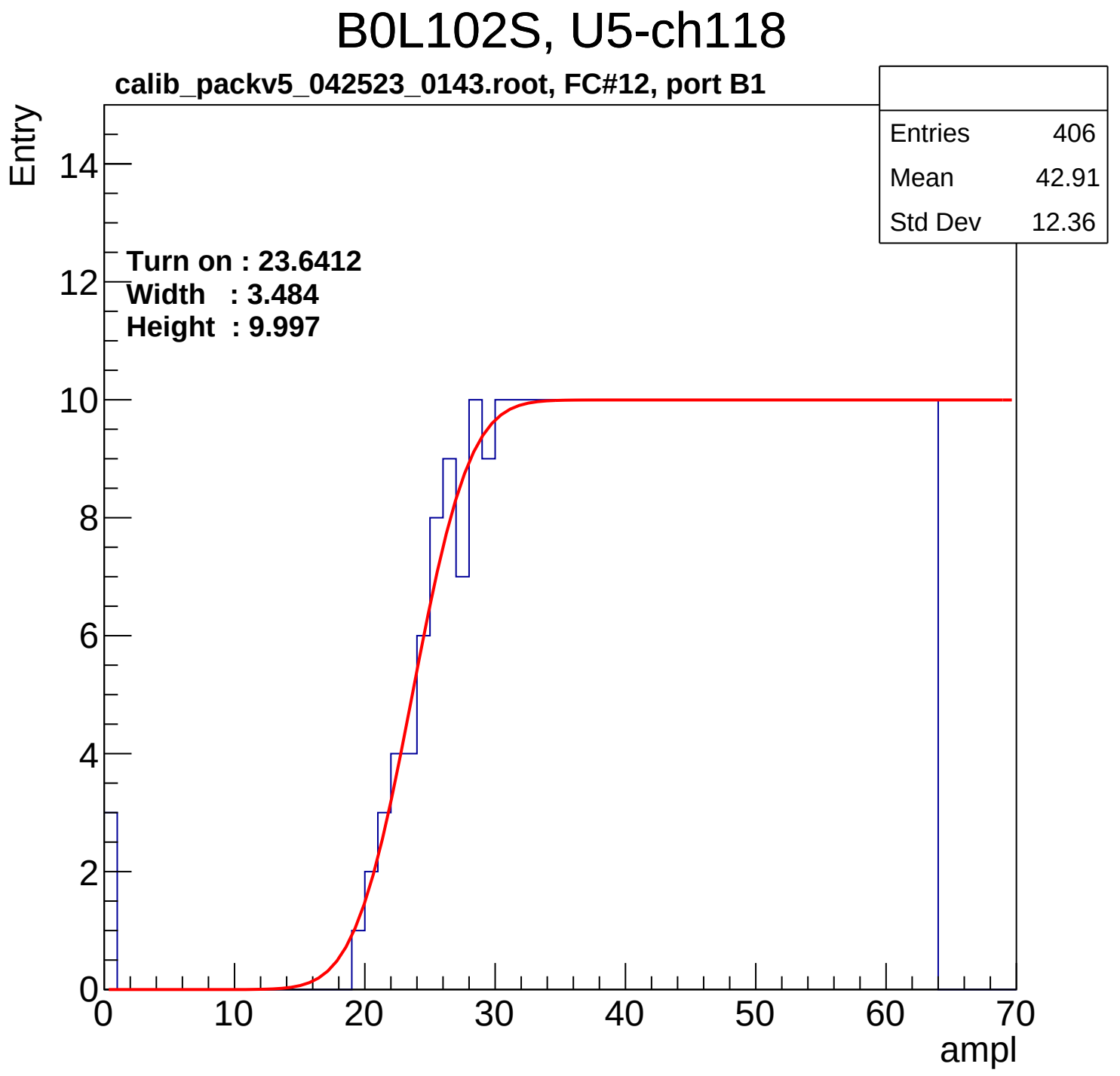
B0L102S, U5-ch118
calib_packv5_042523_0143.root, FC#12, port B1
Entries 406
Mean 42.91
Std Dev 12.36
Turn on : 23.6412
Width : 3.484
Height : 9.997
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
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60
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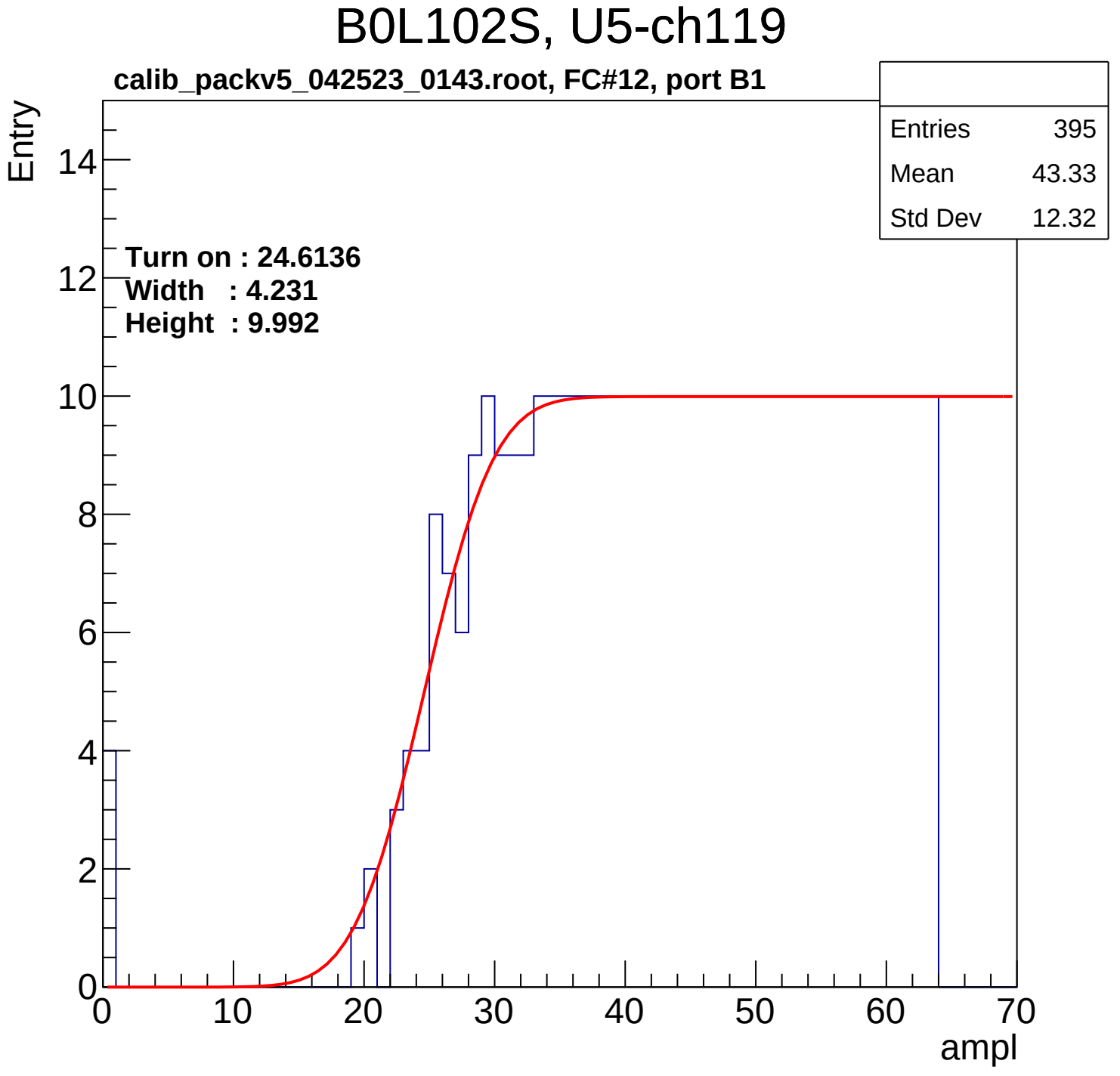
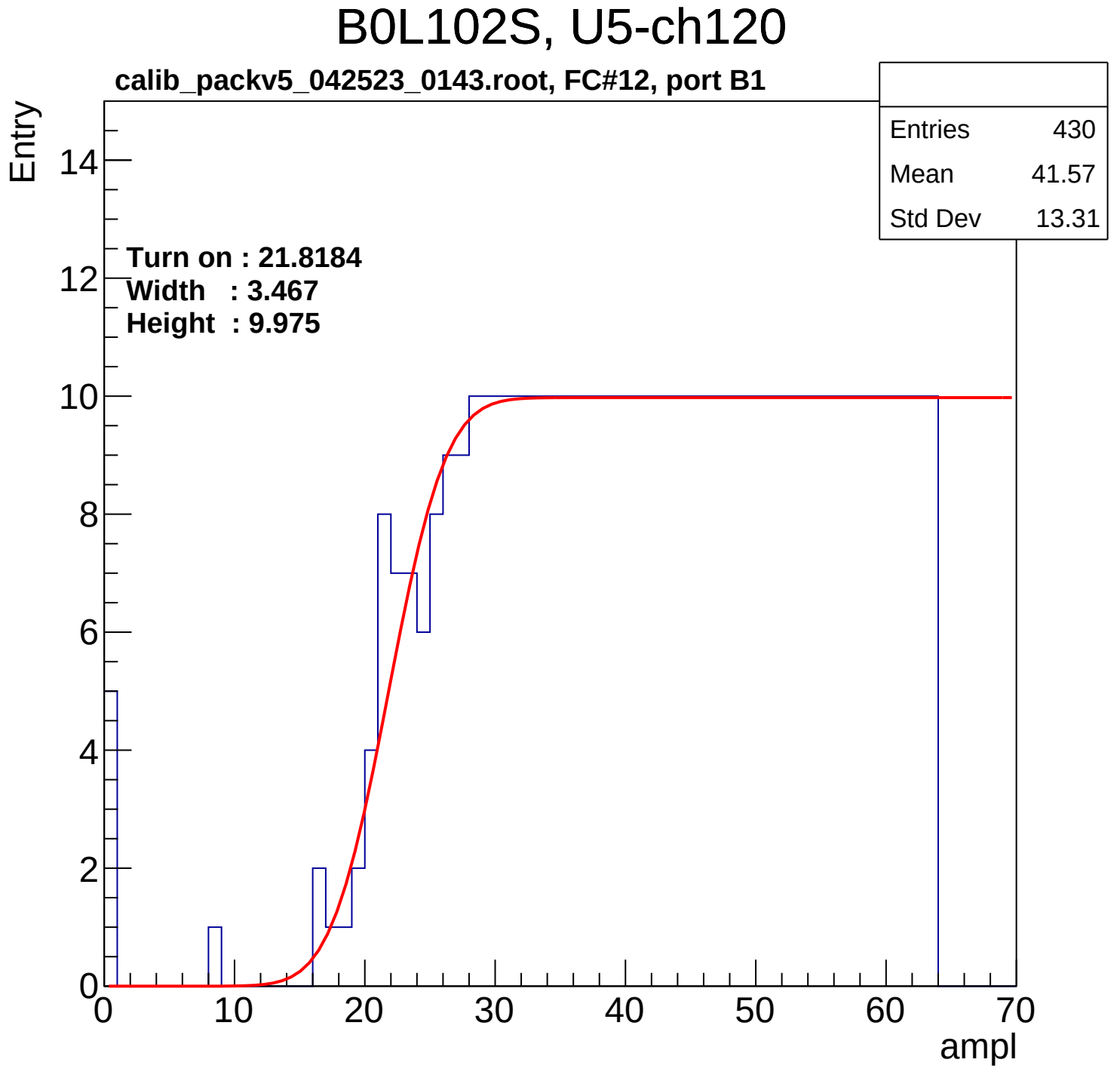

B0L102S, U5-ch119
calib_packv5_042523_0143.root, FC#12, port B1
Entries 395
Mean 43.33
Std Dev 12.32
Turn on : 24.6136
Width : 4.231
Height : 9.992
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L102S, U5-ch120
calib_packv5_042523_0143.root, FC#12, port B1
Entries 430
Mean 41.57
Std Dev 13.31
Turn on : 21.8184
Width : 3.467
Height : 9.975
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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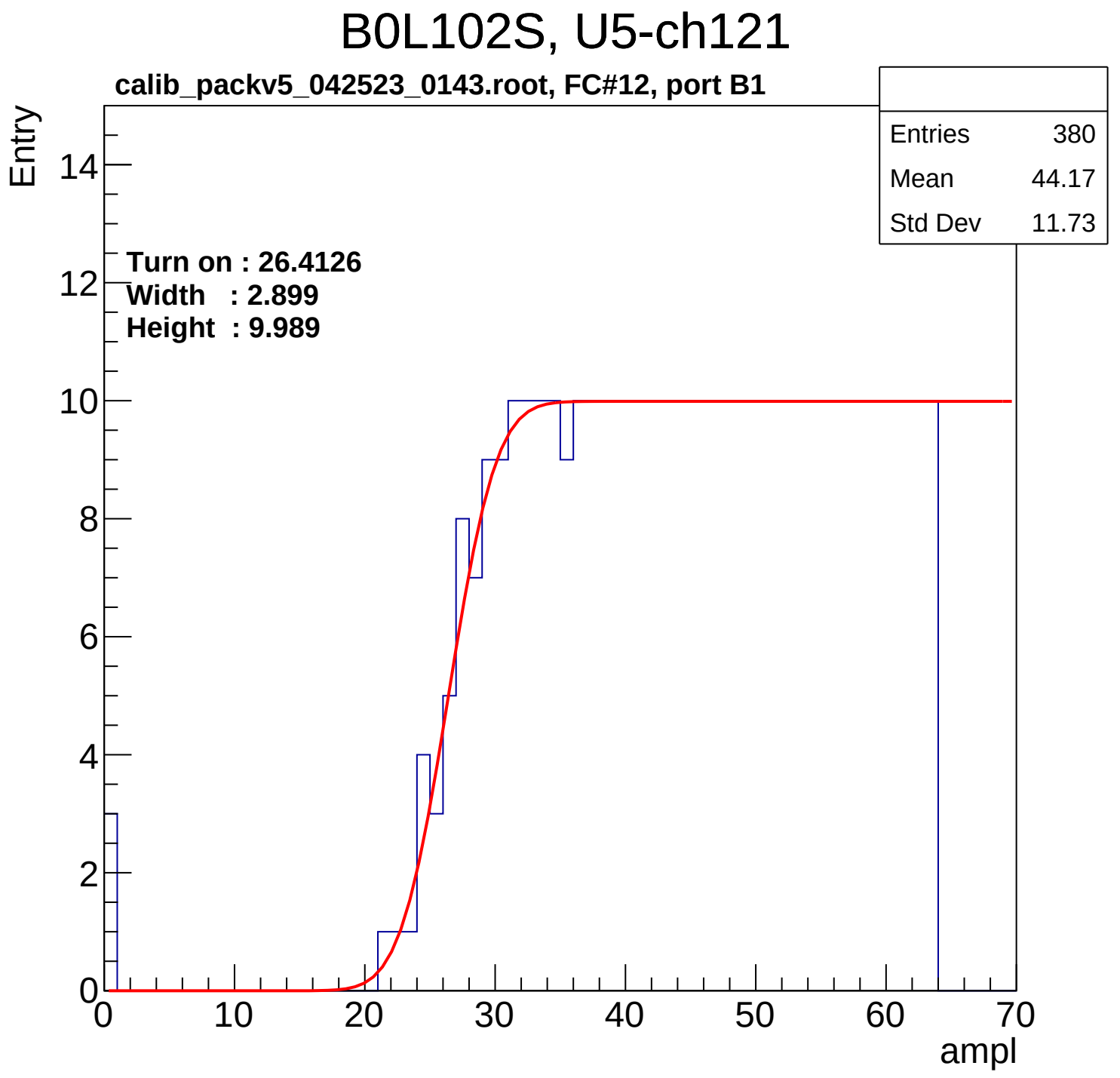
B0L102S, U5-ch121
calib_packv5_042523_0143.root, FC#12, port B1
Entries 380
Mean 44.17
Std Dev 11.73
Turn on : 26.4126
Width : 2.899
Height : 9.989
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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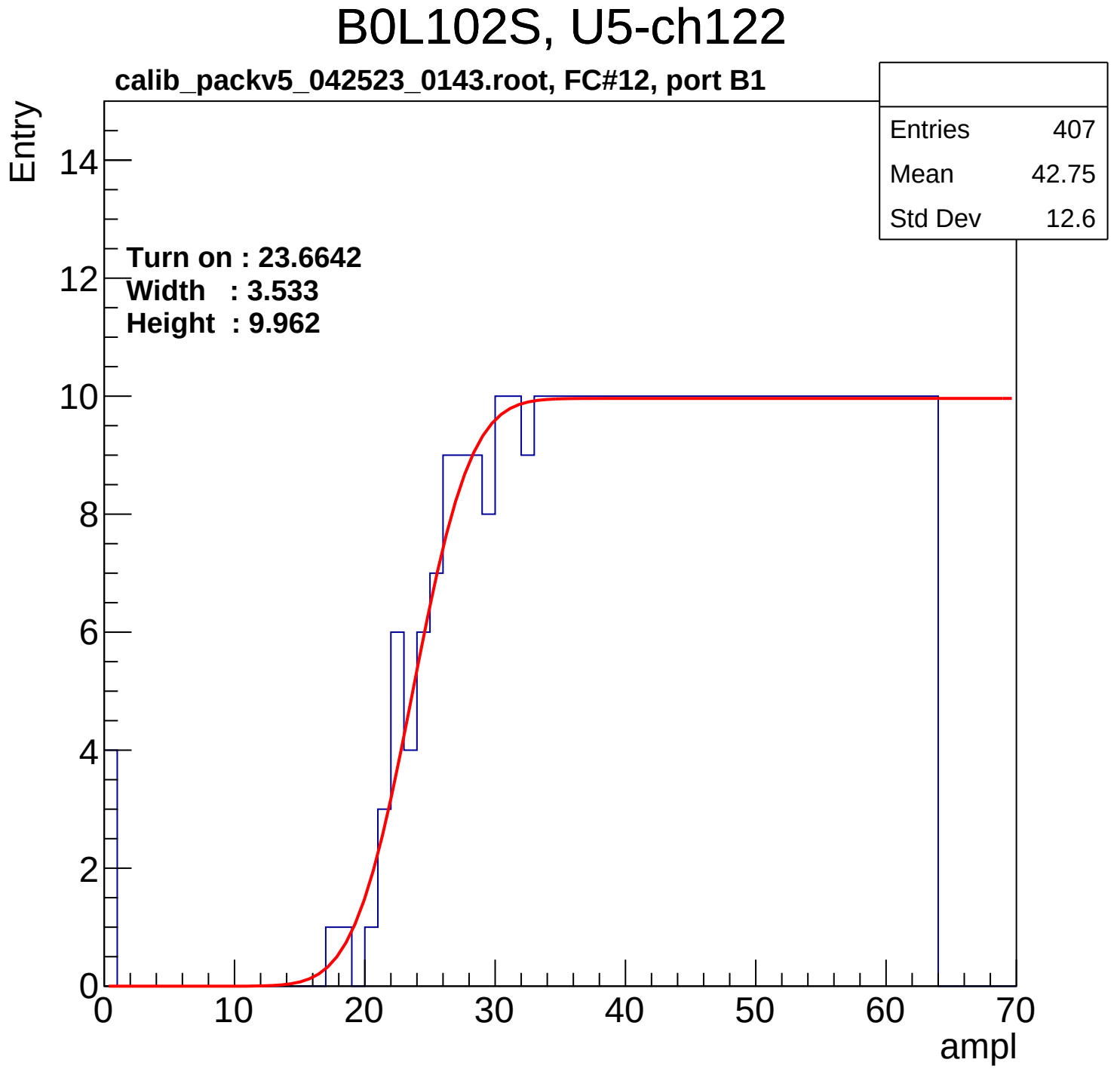
B0L102S, U5-ch122
calib_packv5_042523_0143.root, FC#12, port B1
Entries 407
Mean 42.75
Std Dev 12.6
Turn on : 23.6642
Width : 3.533
Height : 9.962
Entry
ampl
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2
4
6
8
10
12
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0
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20
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40
50
60
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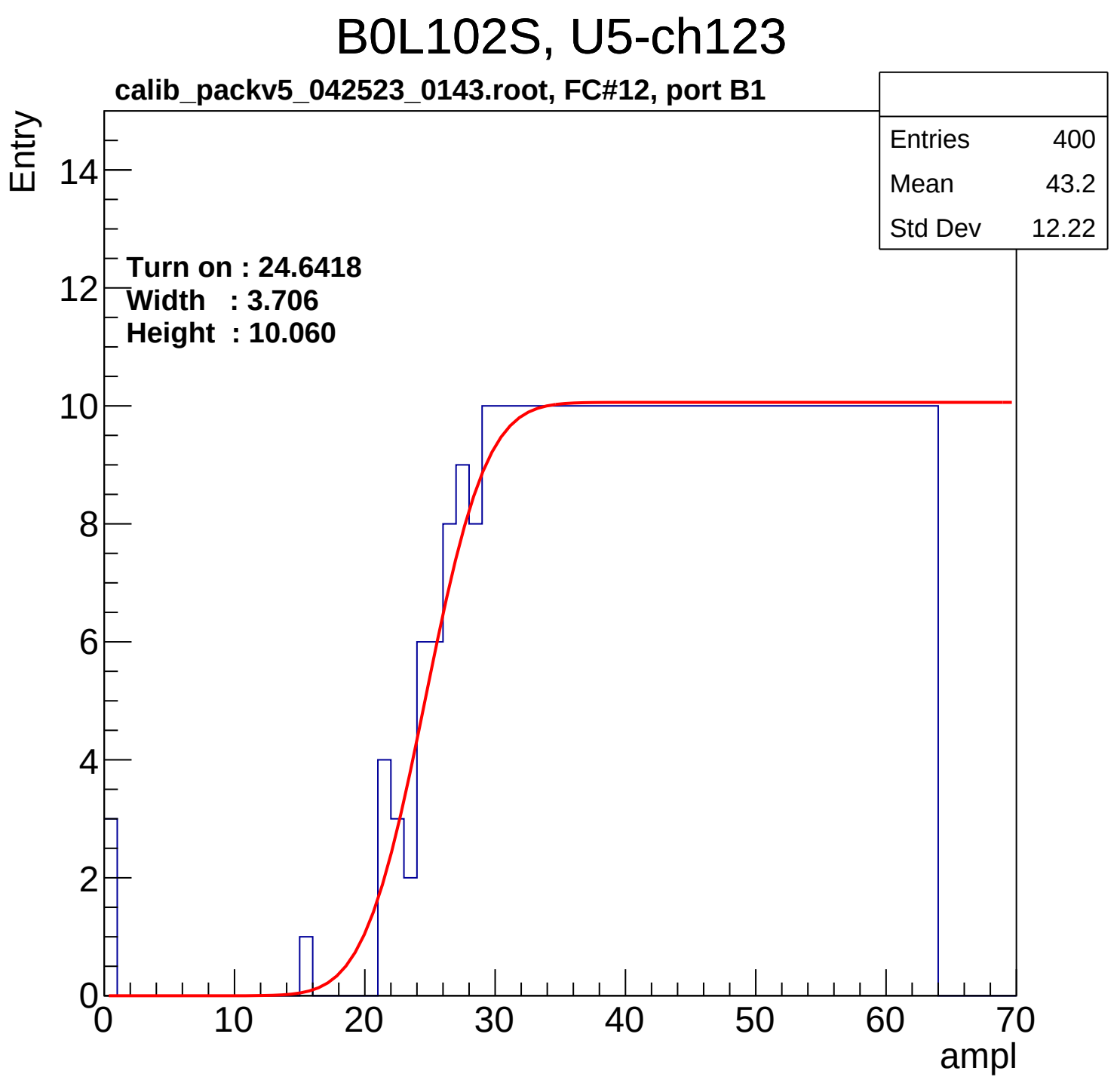
B0L102S, U5-ch123
calib_packv5_042523_0143.root, FC#12, port B1
Entries 400
Mean 43.2
Std Dev 12.22
Turn on : 24.6418
Width : 3.706
Height : 10.060
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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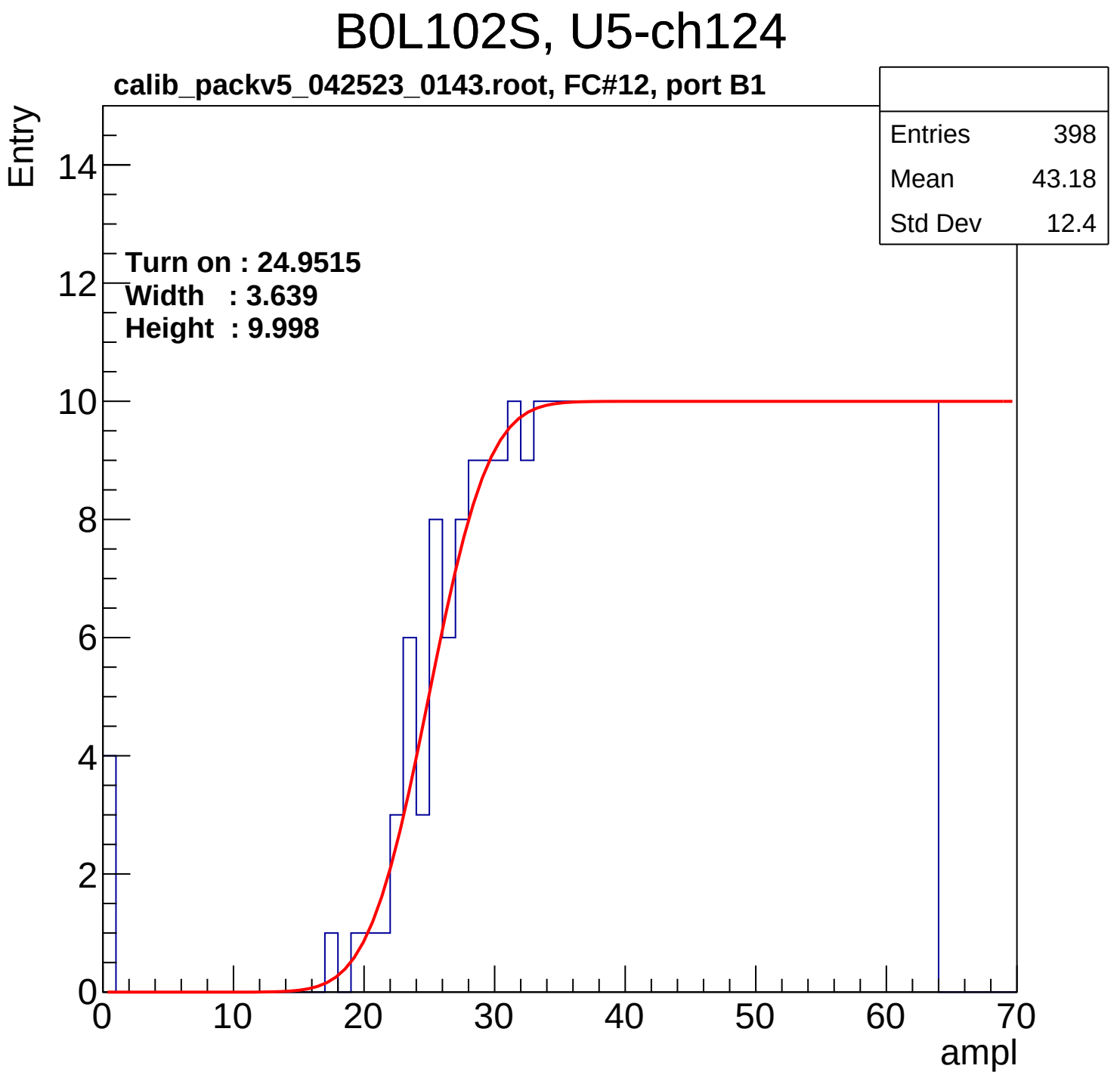
B0L102S, U5-ch124
calib_packv5_042523_0143.root, FC#12, port B1
Entries 398
Mean 43.18
Std Dev 12.4
Turn on : 24.9515
Width : 3.639
Height : 9.998
Entry
ampl
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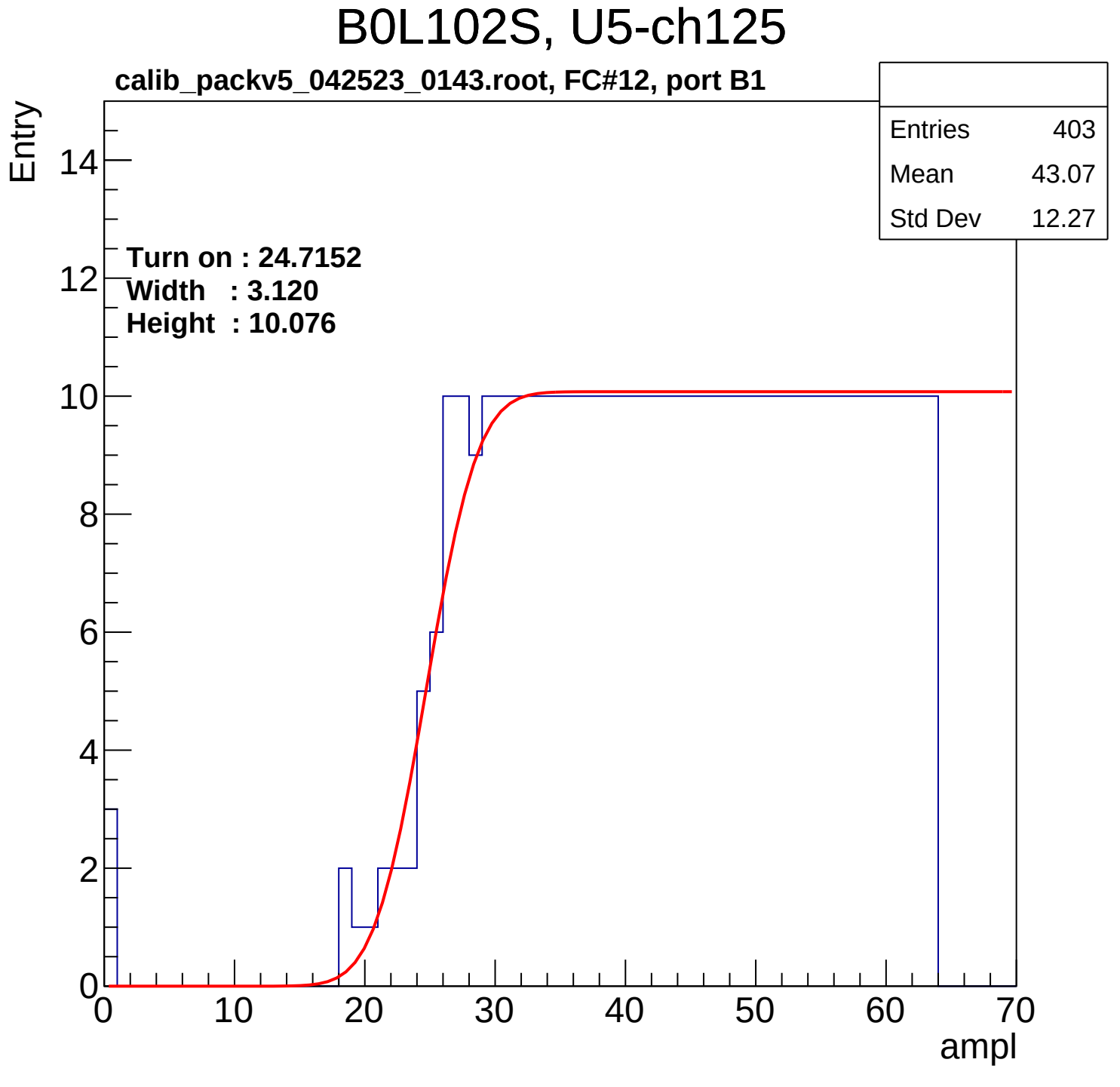
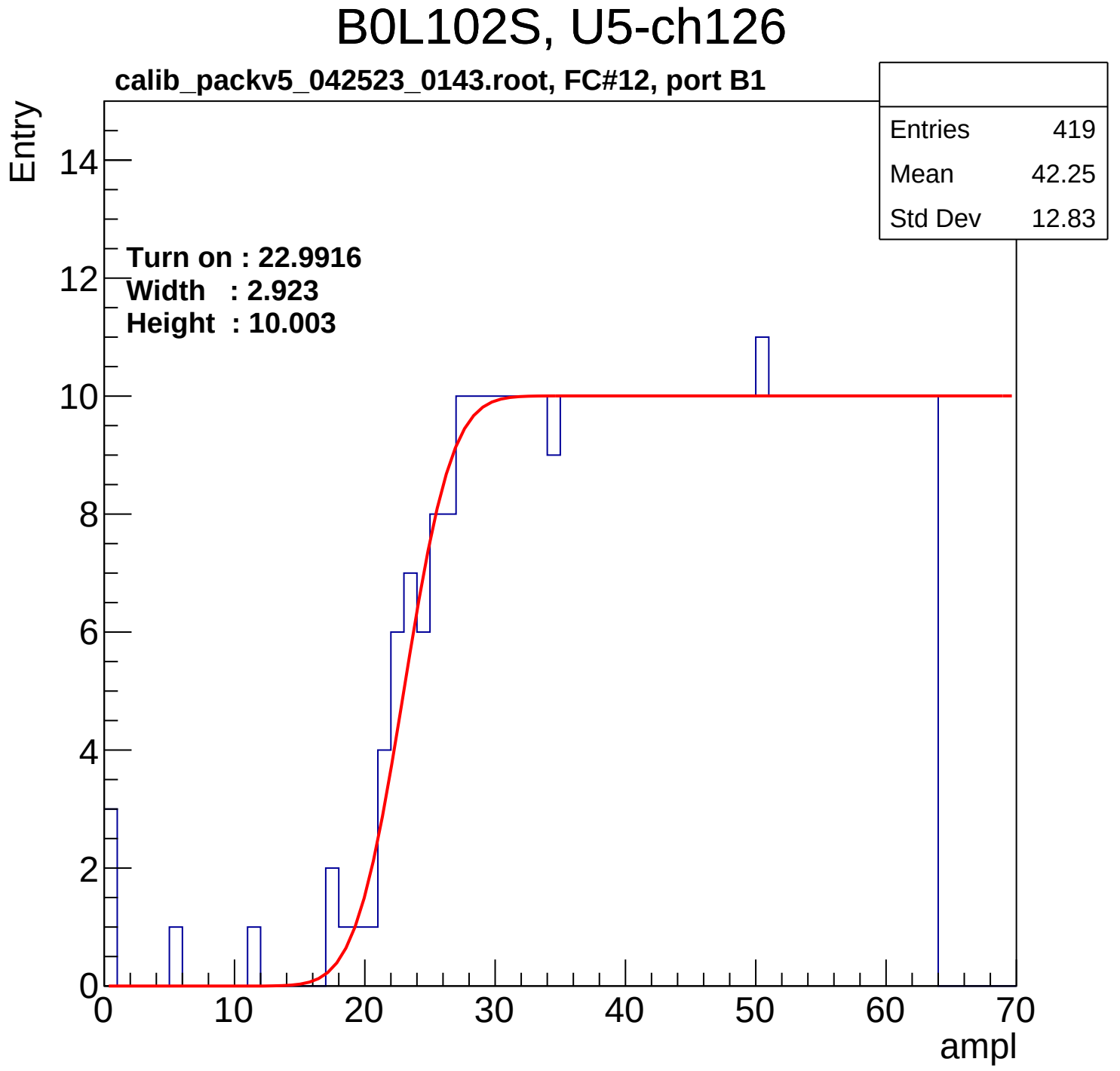
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L102S, U5-ch125
calib_packv5_042523_0143.root, FC#12, port B1
Entries 403
Mean 43.07
Std Dev 12.27
Turn on : 24.7152
Width : 3.120
Height : 10.076
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L102S, U5-ch126
calib_packv5_042523_0143.root, FC#12, port B1
Entries 419
Mean 42.25
Std Dev 12.83
Turn on : 22.9916
Width : 2.923
Height : 10.003
Entry
ampl
0
2
4
6
8
10
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0
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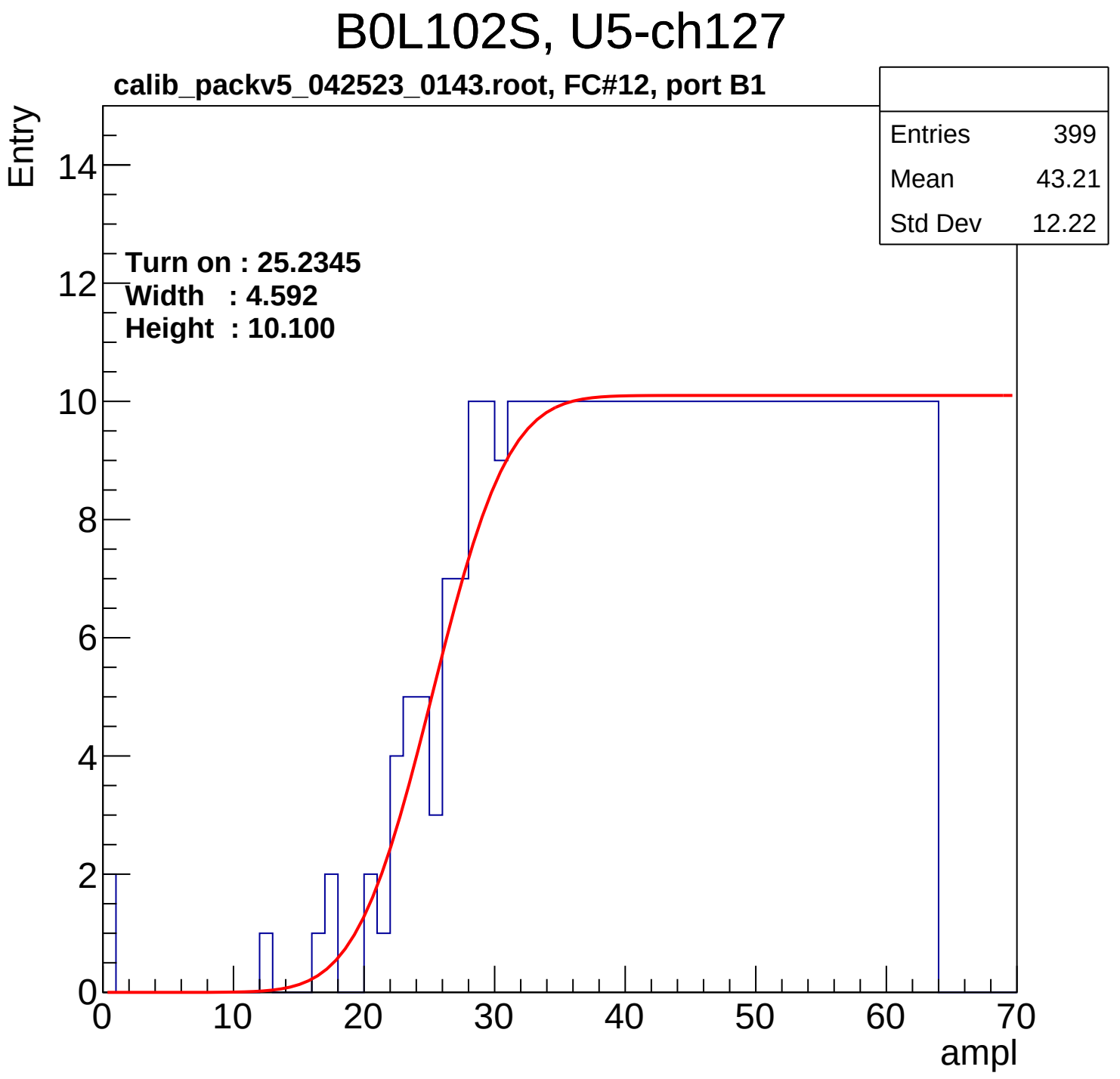
B0L102S, U5-ch127
calib_packv5_042523_0143.root, FC#12, port B1
Entries 399
Mean 43.21
Std Dev 12.22
Turn on : 25.2345
Width : 4.592
Height : 10.100
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
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60
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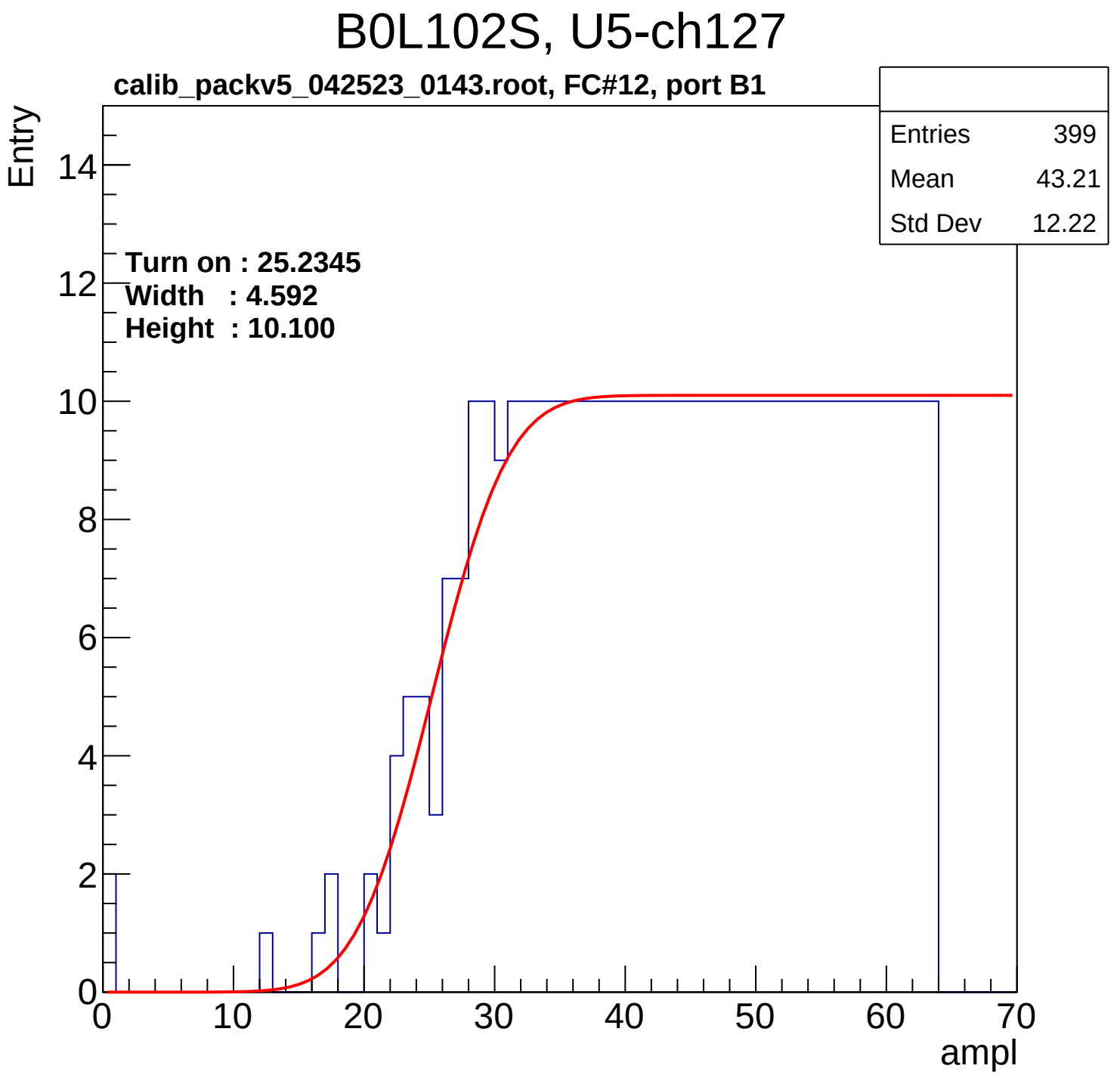
B0L102S, U5-ch127
calib_packv5_042523_0143.root, FC#12, port B1
Entries 399
Mean 43.21
Std Dev 12.22
Turn on : 25.2345
Width : 4.592
Height : 10.100
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70