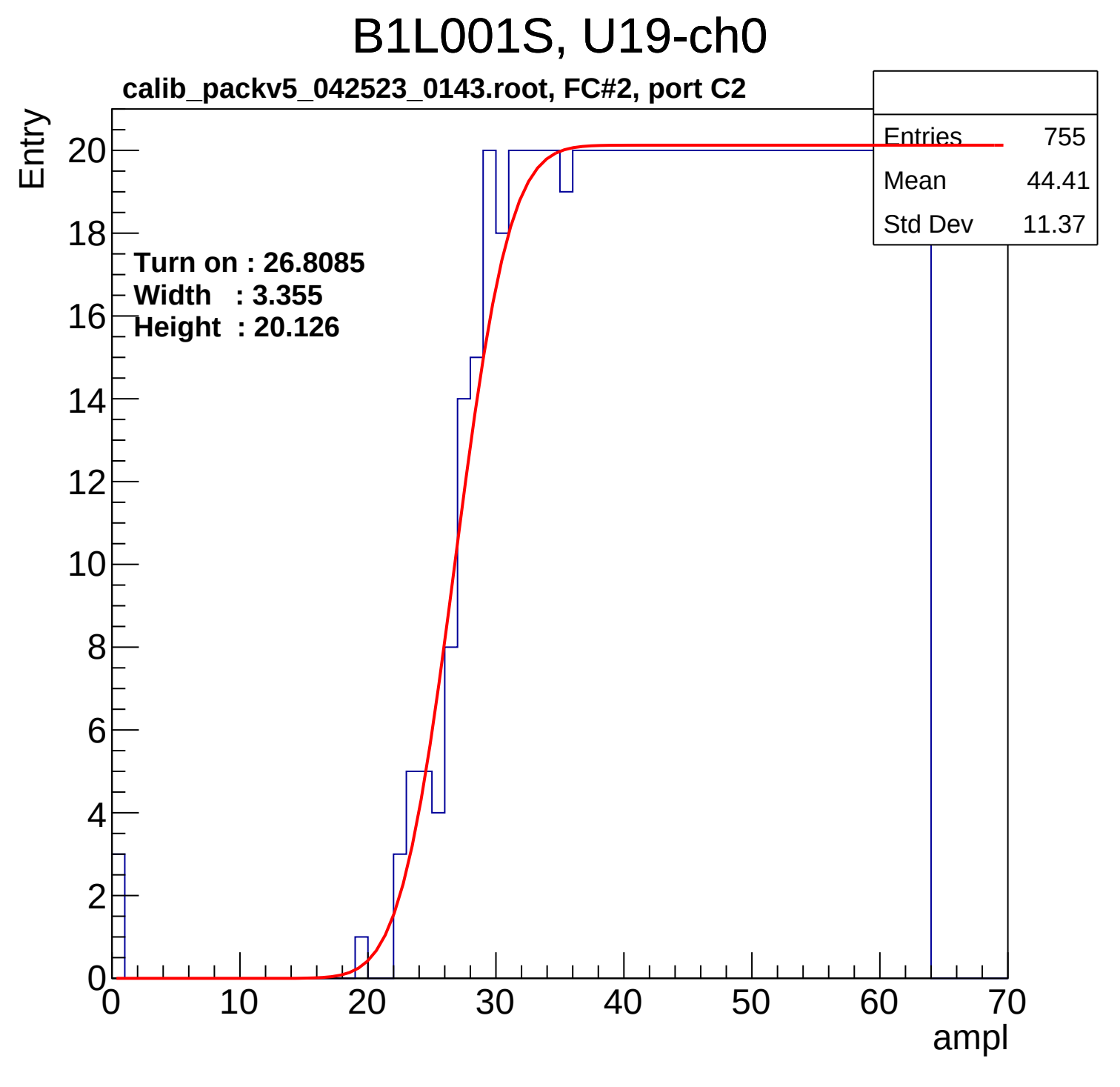
B1L001S, U19-ch0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 755
Mean 44.41
Std Dev 11.37
Turn on : 26.8085
Width : 3.355
Height : 20.126
Entry
ampl
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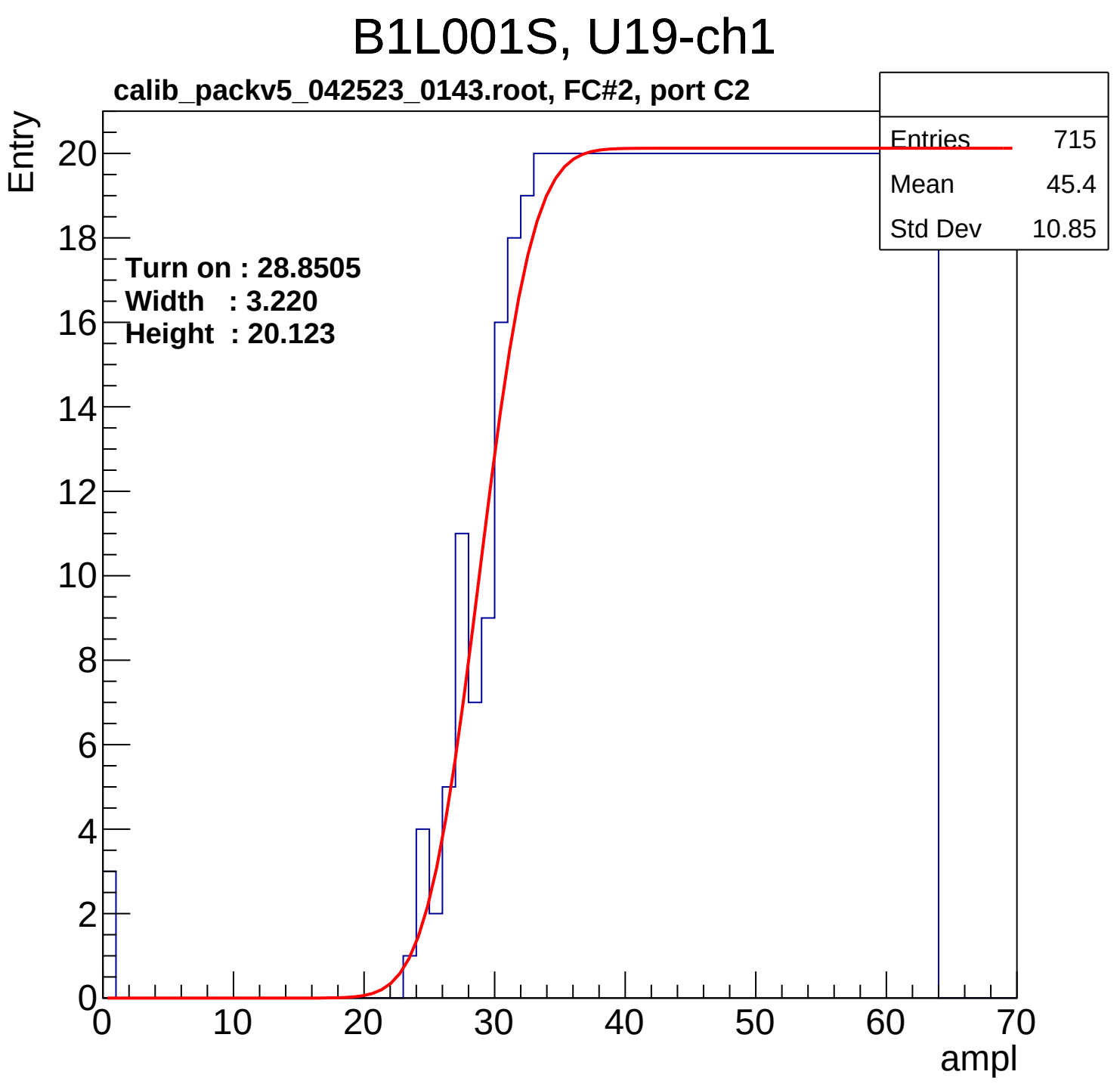
B1L001S, U19-ch1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 715
Mean 45.4
Std Dev 10.85
Turn on : 28.8505
Width : 3.220
Height : 20.123
Entry
ampl
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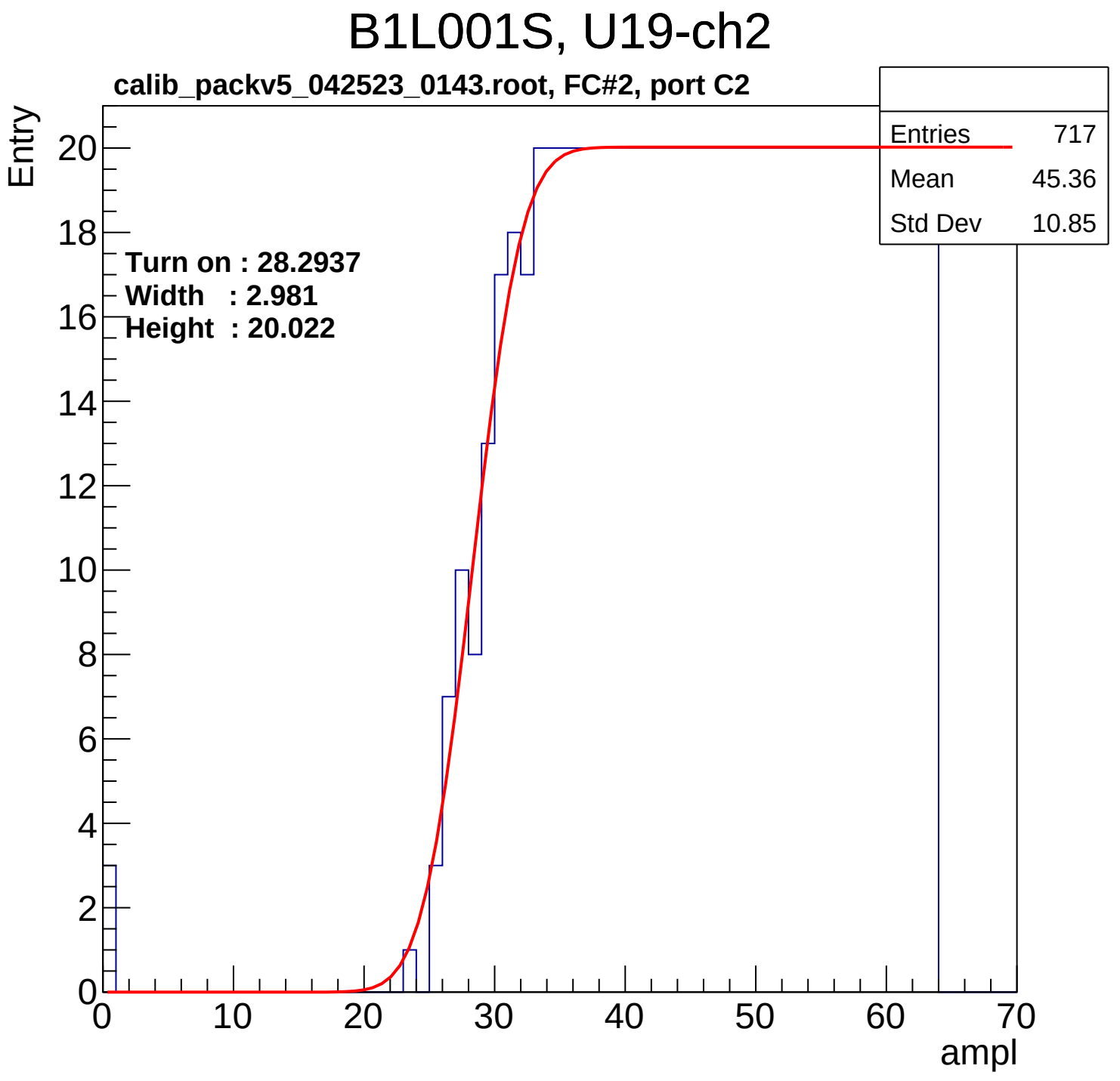
B1L001S, U19-ch2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 717
Mean 45.36
Std Dev 10.85
Turn on : 28.2937
Width : 2.981
Height : 20.022
Entry
ampl
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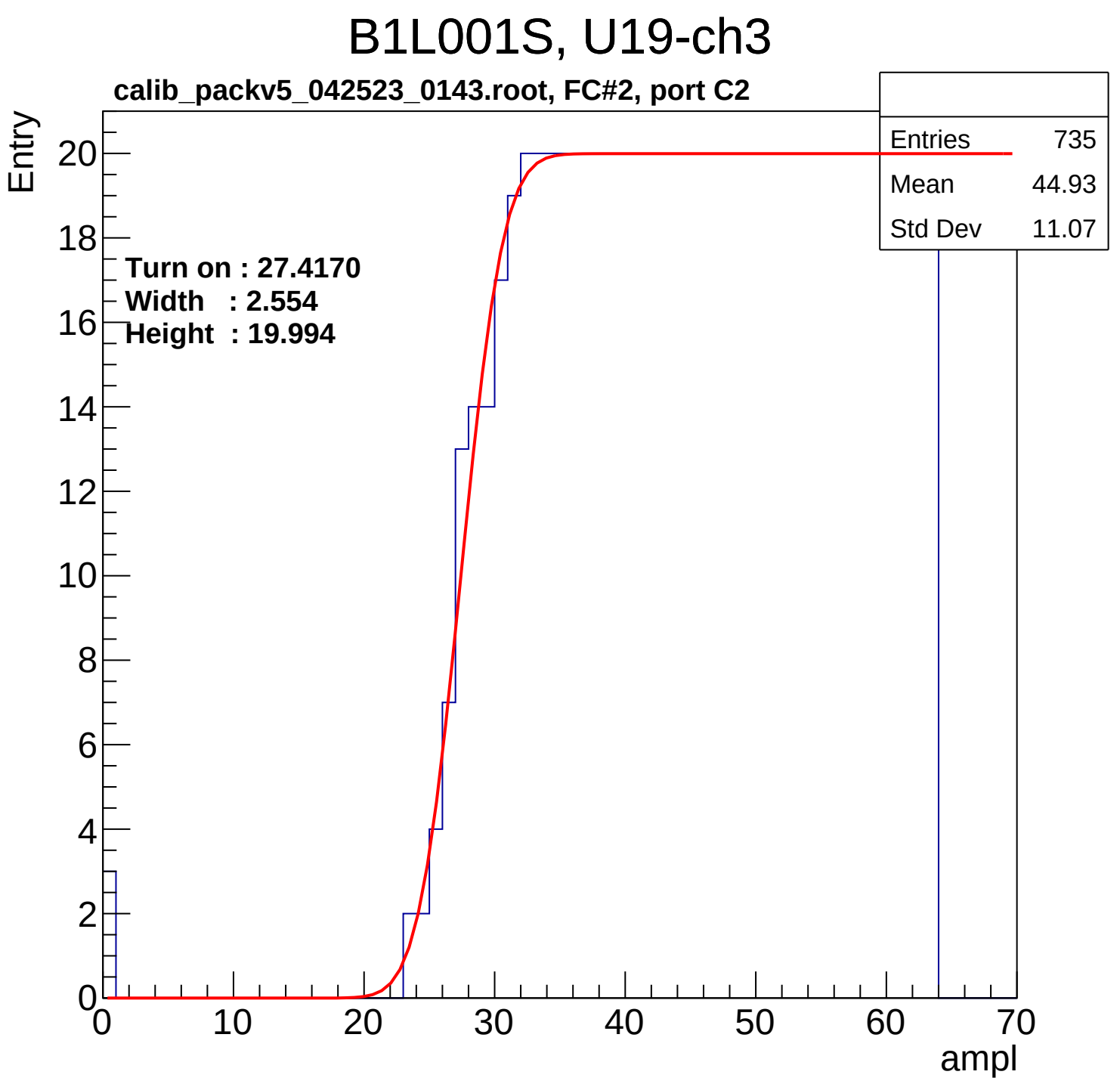
B1L001S, U19-ch3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 735
Mean 44.93
Std Dev 11.07
Turn on : 27.4170
Width : 2.554
Height : 19.994
Entry
ampl
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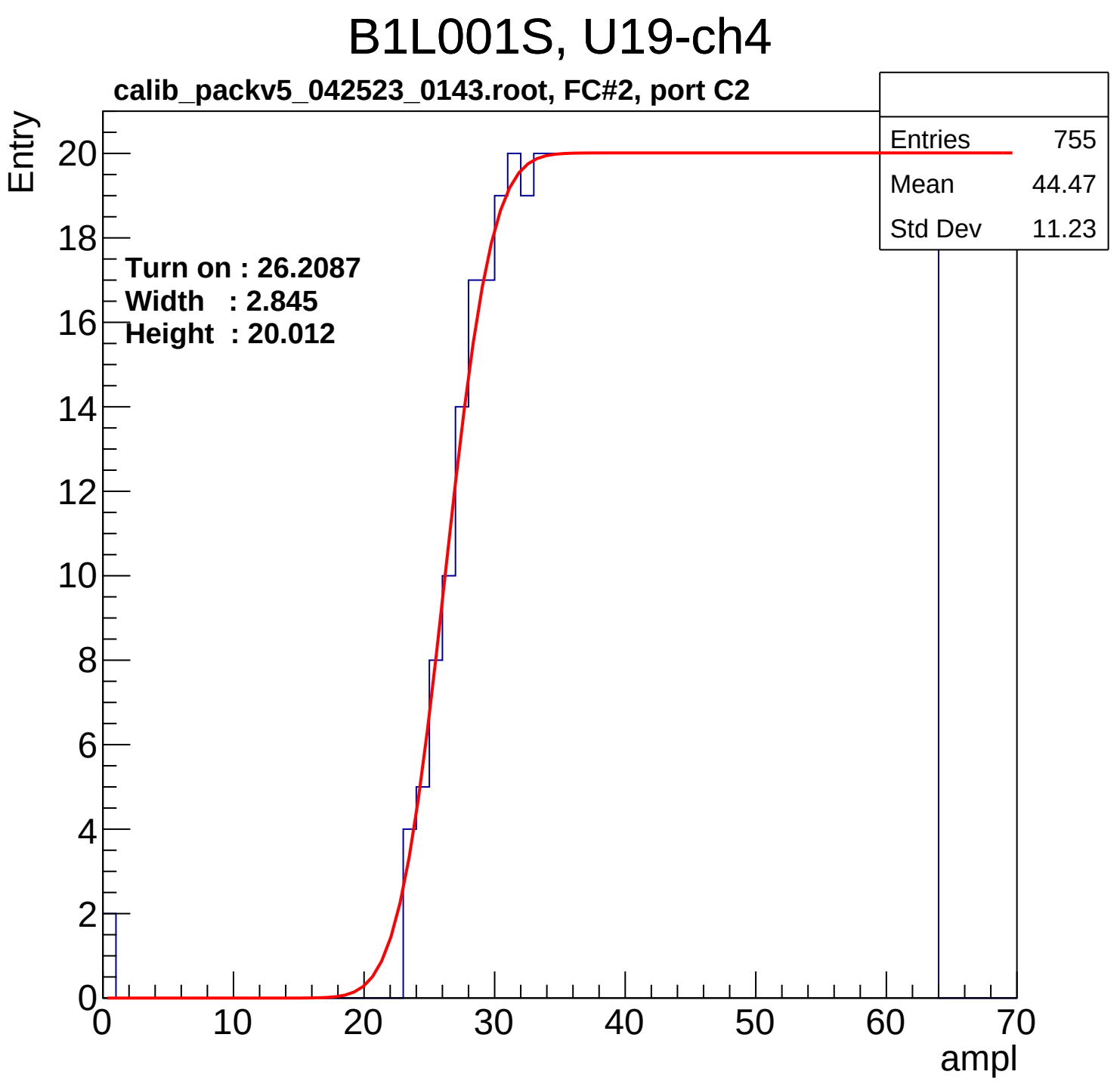
B1L001S, U19-ch4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 755
Mean 44.47
Std Dev 11.23
Turn on : 26.2087
Width : 2.845
Height : 20.012
Entry
ampl
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6
8
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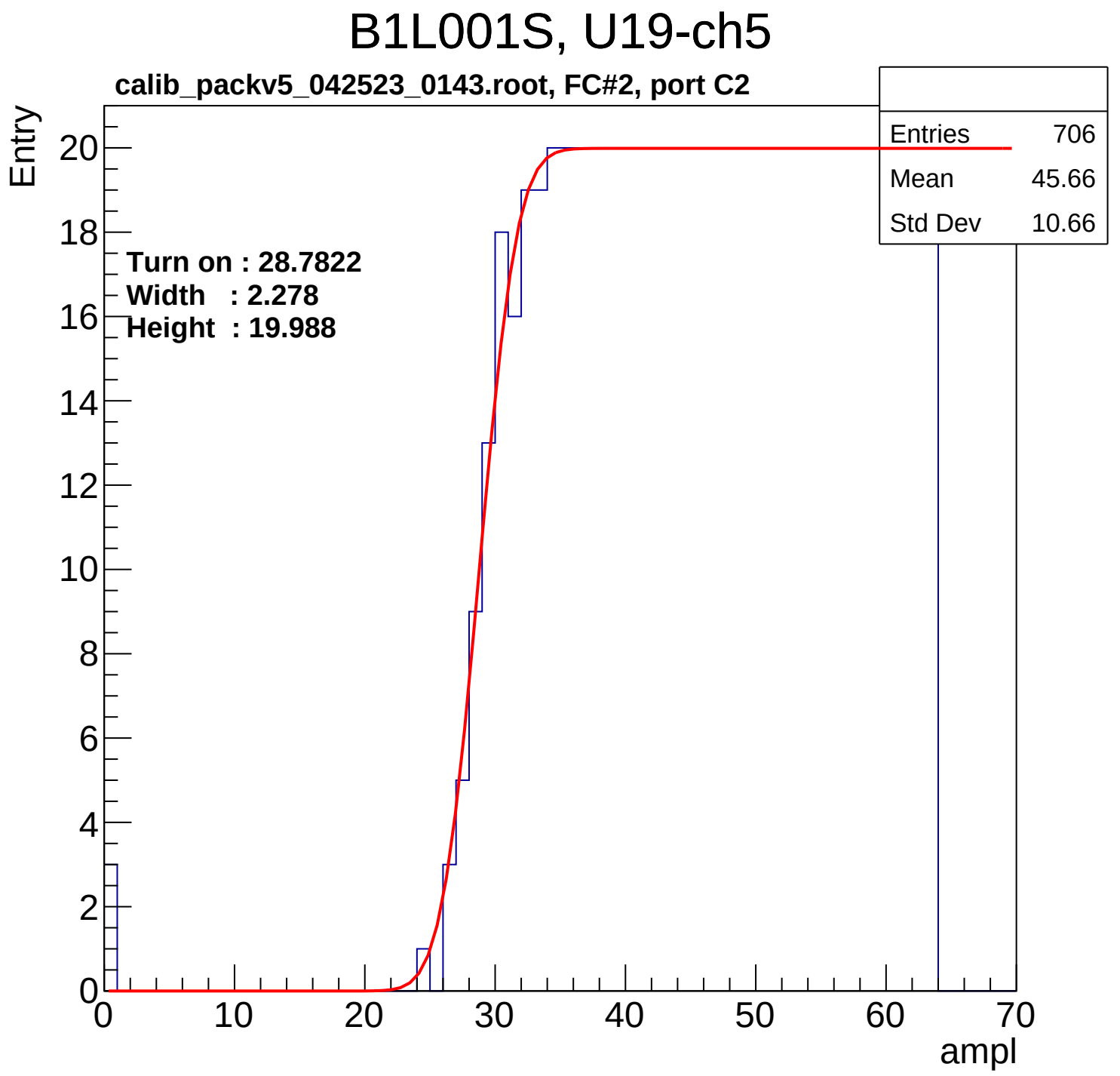
B1L001S, U19-ch5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 706
Mean 45.66
Std Dev 10.66
Turn on : 28.7822
Width : 2.278
Height : 19.988
Entry
ampl
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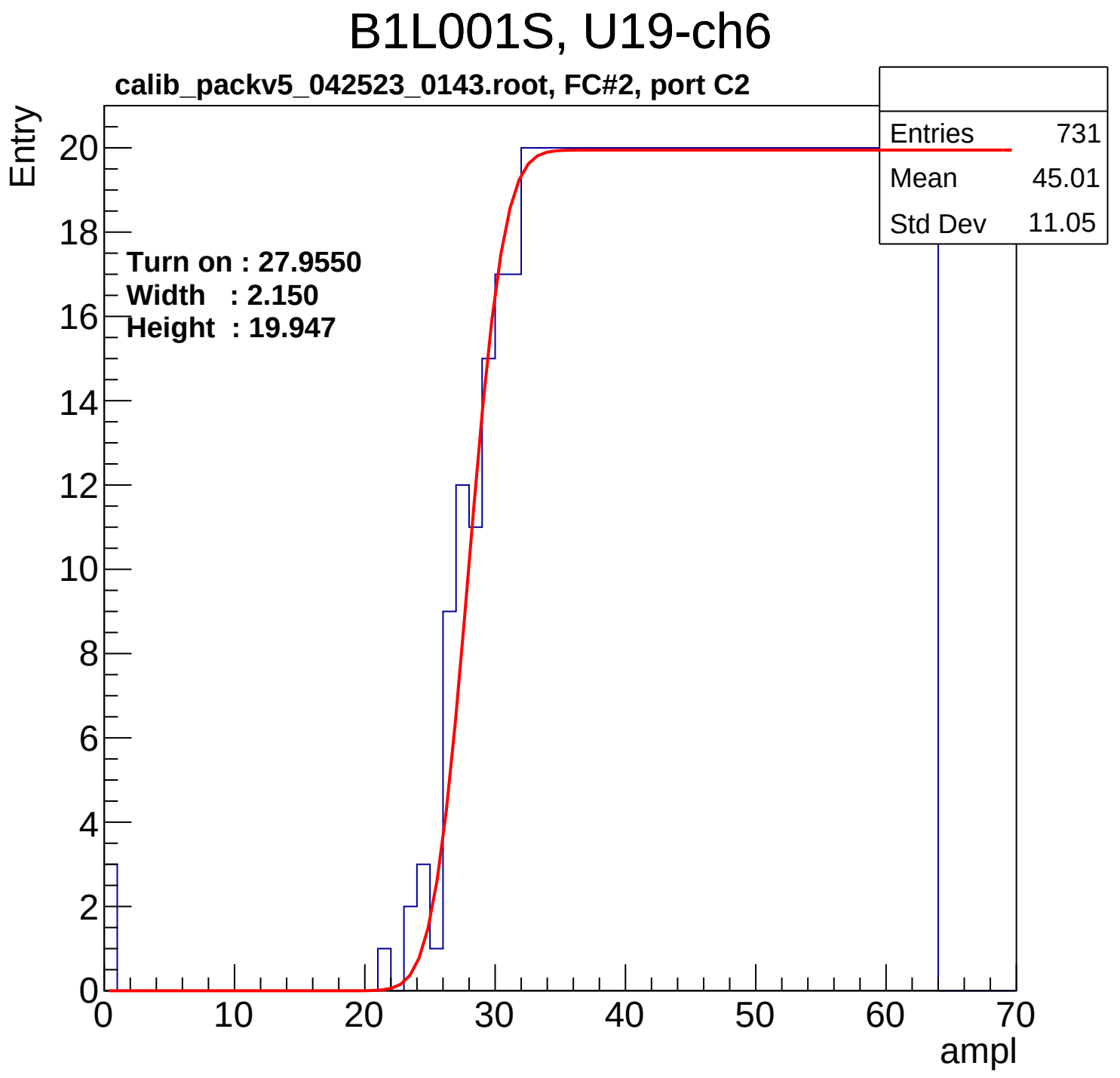
B1L001S, U19-ch6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 731
Mean 45.01
Std Dev 11.05
Turn on : 27.9550
Width : 2.150
Height : 19.947
Entry
ampl
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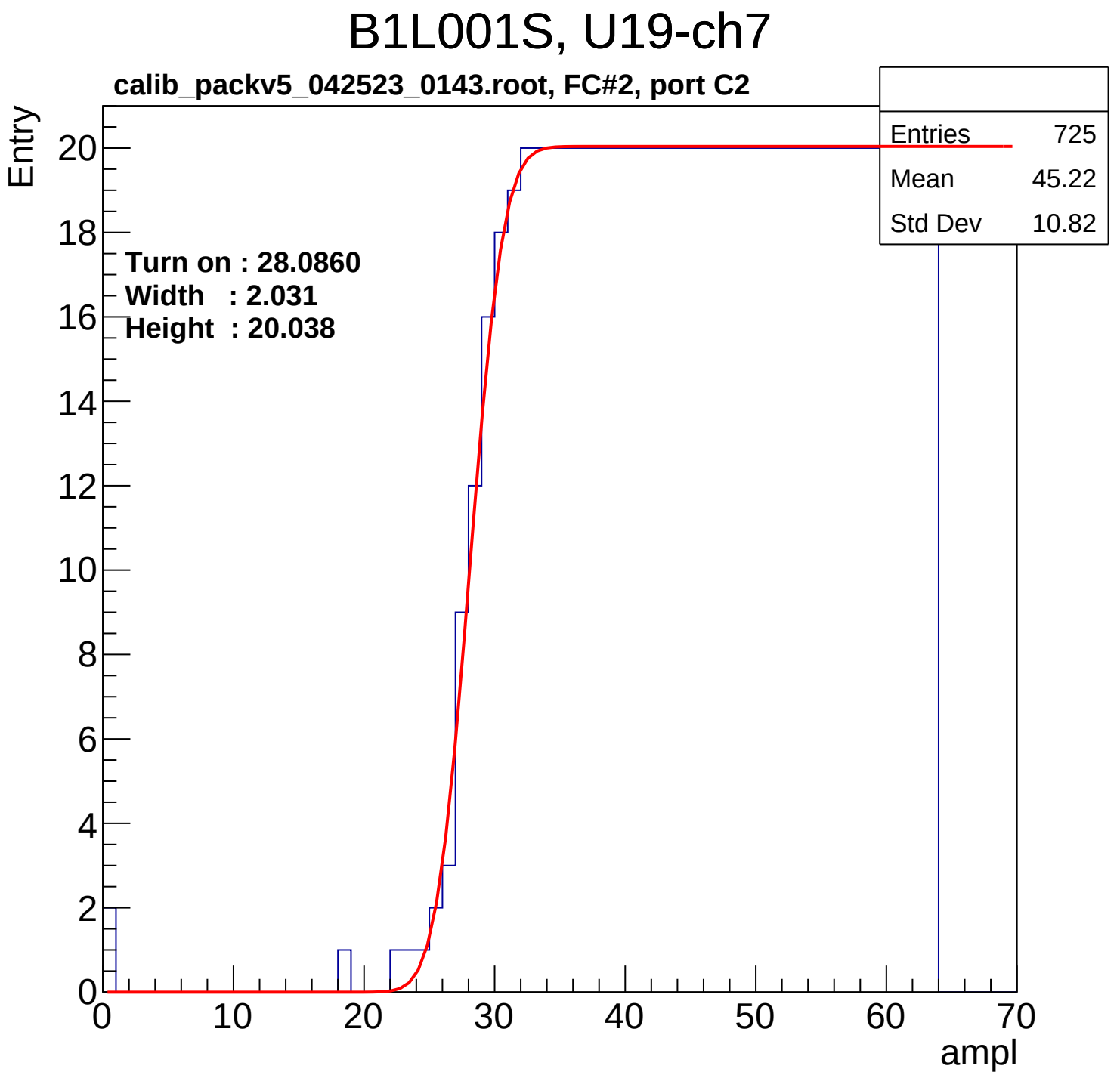
B1L001S, U19-ch7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 725
Mean 45.22
Std Dev 10.82
Turn on : 28.0860
Width : 2.031
Height : 20.038
Entry
ampl
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6
8
10
12
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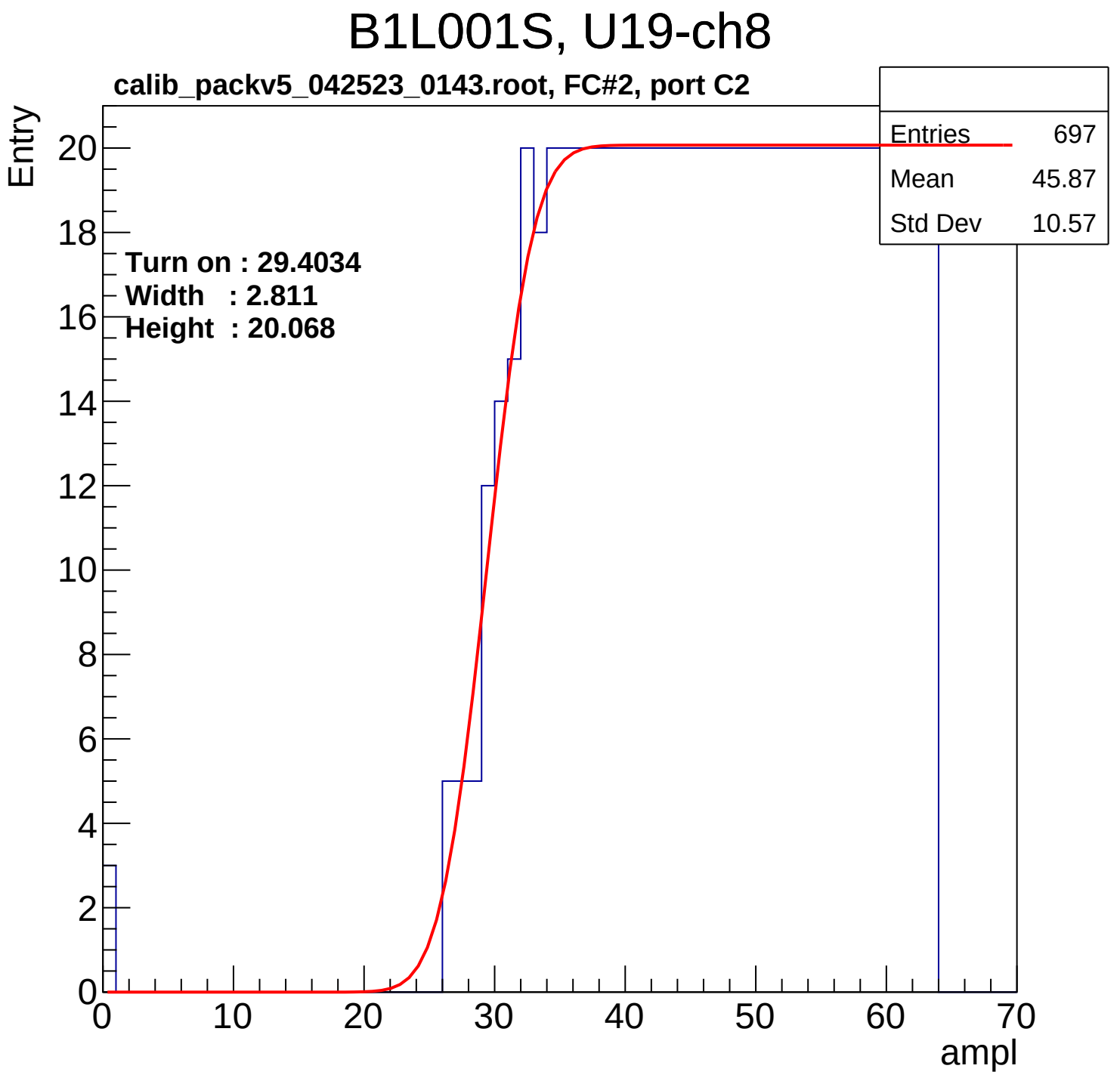
B1L001S, U19-ch8
calib_packv5_042523_0143.root, FC#2, port C2
Entries 697
Mean 45.87
Std Dev 10.57
Turn on : 29.4034
Width : 2.811
Height : 20.068
Entry
ampl
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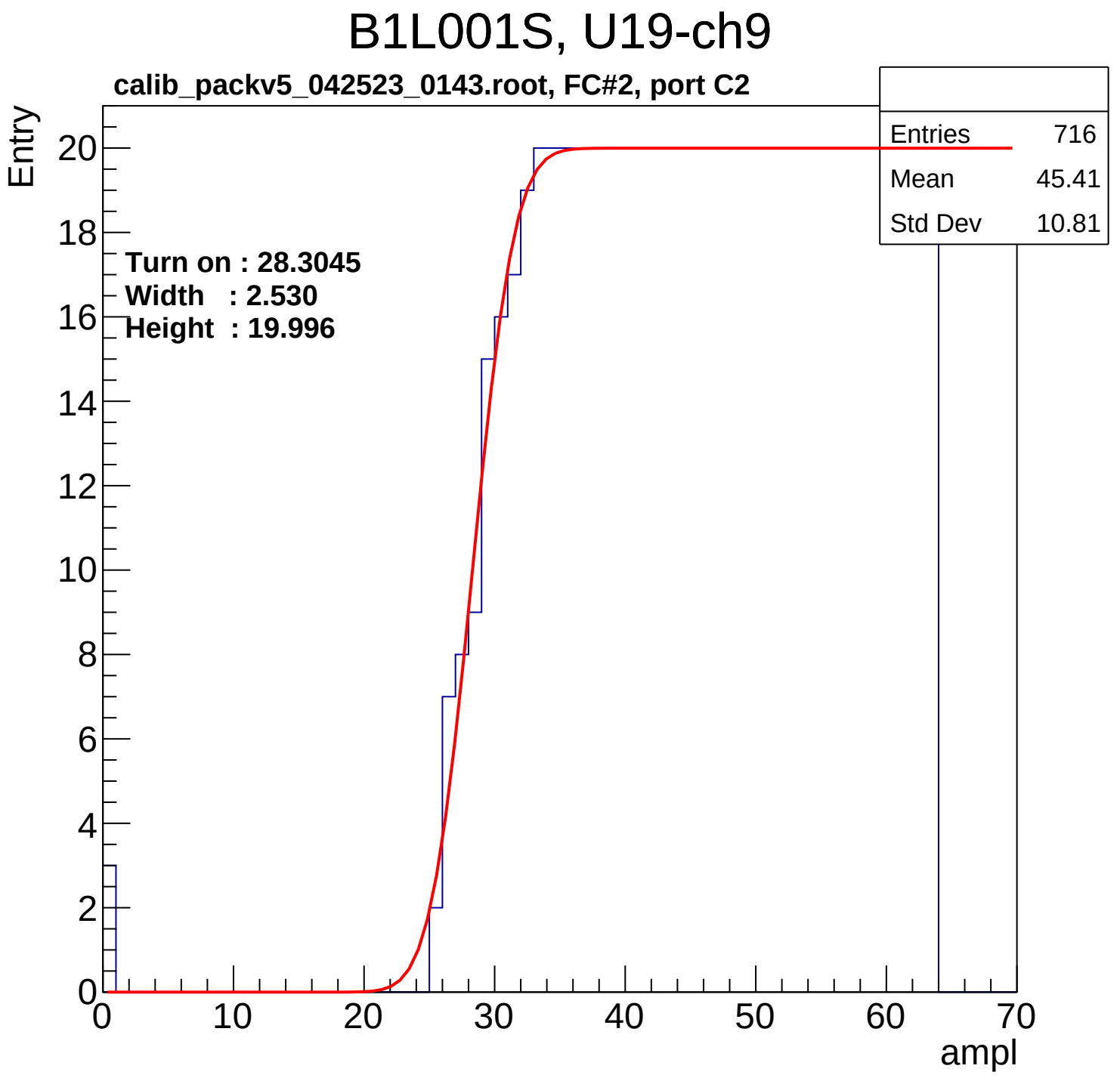
B1L001S, U19-ch9
calib_packv5_042523_0143.root, FC#2, port C2
Entries 716
Mean 45.41
Std Dev 10.81
Turn on : 28.3045
Width : 2.530
Height : 19.996
Entry
ampl
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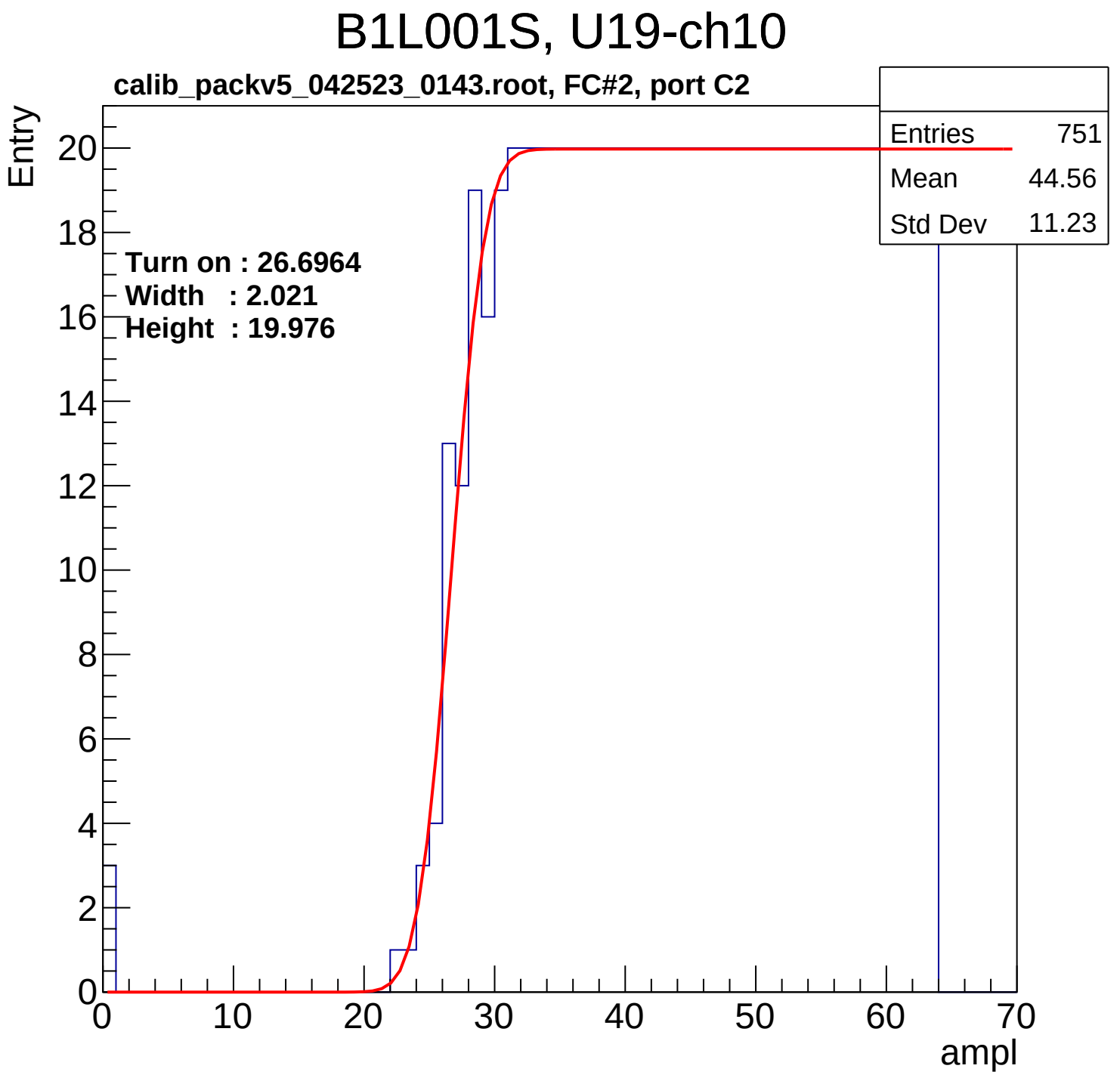
B1L001S, U19-ch10
calib_packv5_042523_0143.root, FC#2, port C2
Entries 751
Mean 44.56
Std Dev 11.23
Turn on : 26.6964
Width : 2.021
Height : 19.976
Entry
ampl
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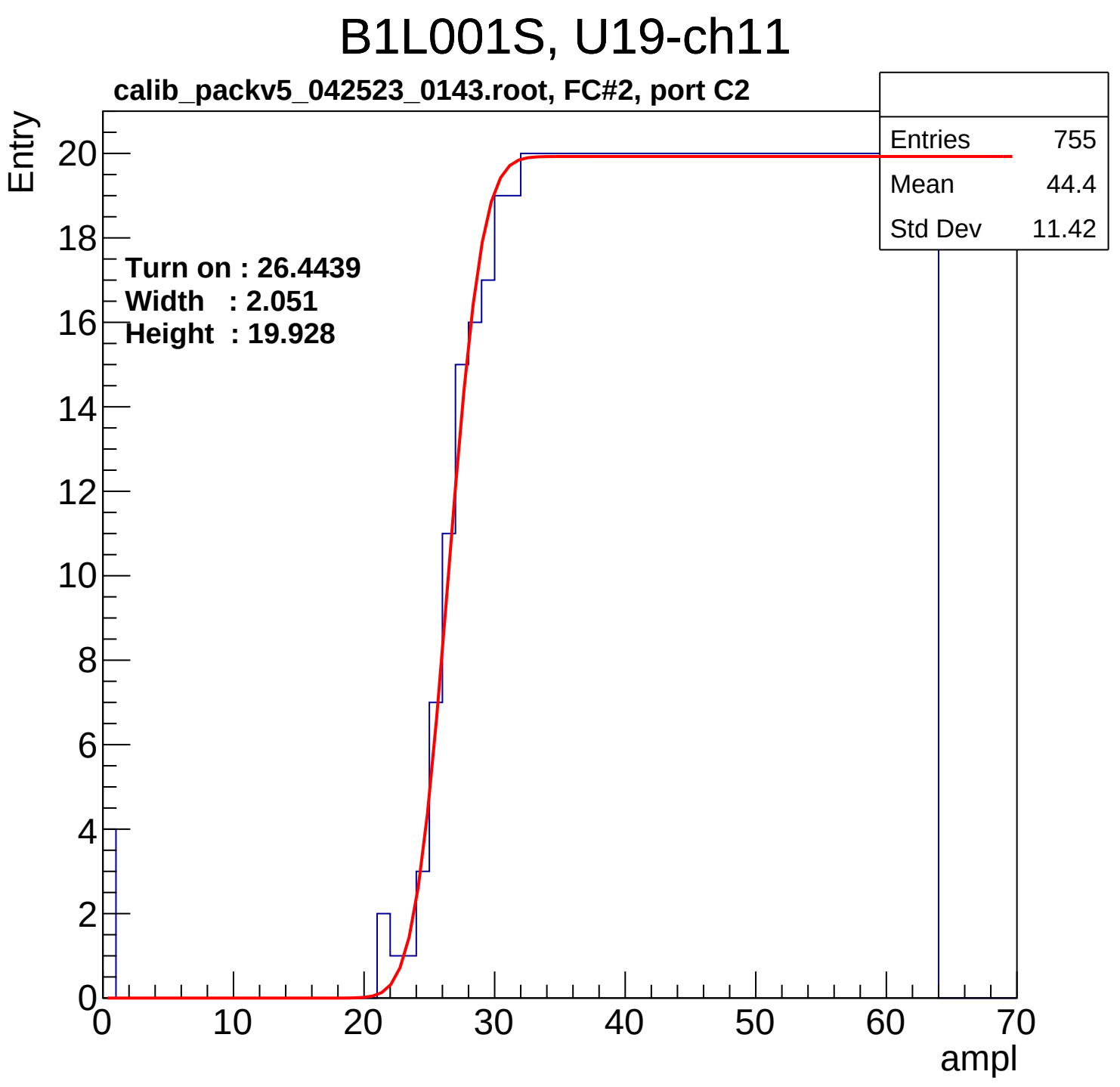
B1L001S, U19-ch11
calib_packv5_042523_0143.root, FC#2, port C2
Entries 755
Mean 44.4
Std Dev 11.42
Turn on : 26.4439
Width : 2.051
Height : 19.928
Entry
ampl
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6
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12
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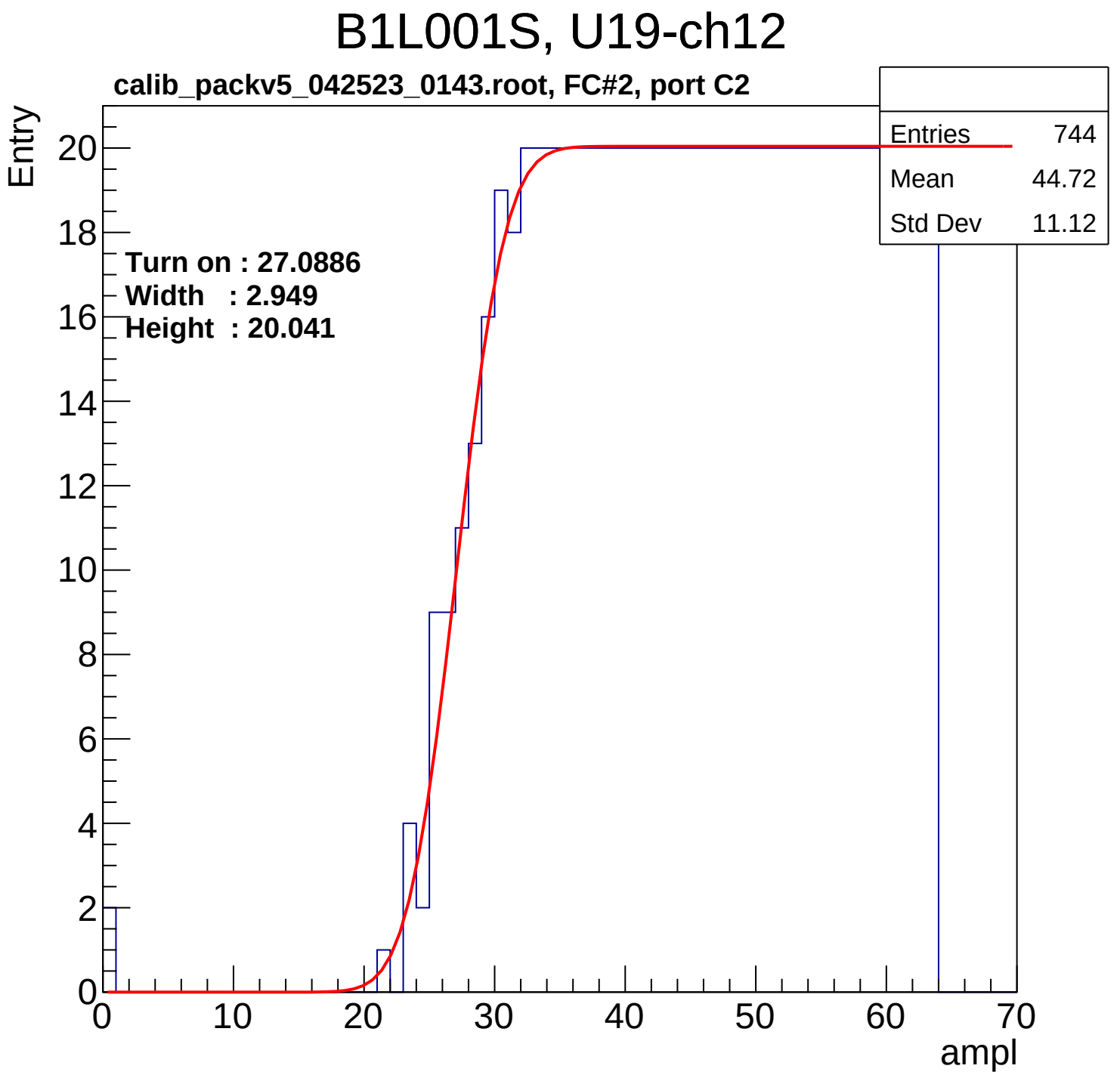
B1L001S, U19-ch12
calib_packv5_042523_0143.root, FC#2, port C2
Entries 744
Mean 44.72
Std Dev 11.12
Turn on : 27.0886
Width : 2.949
Height : 20.041
Entry
ampl
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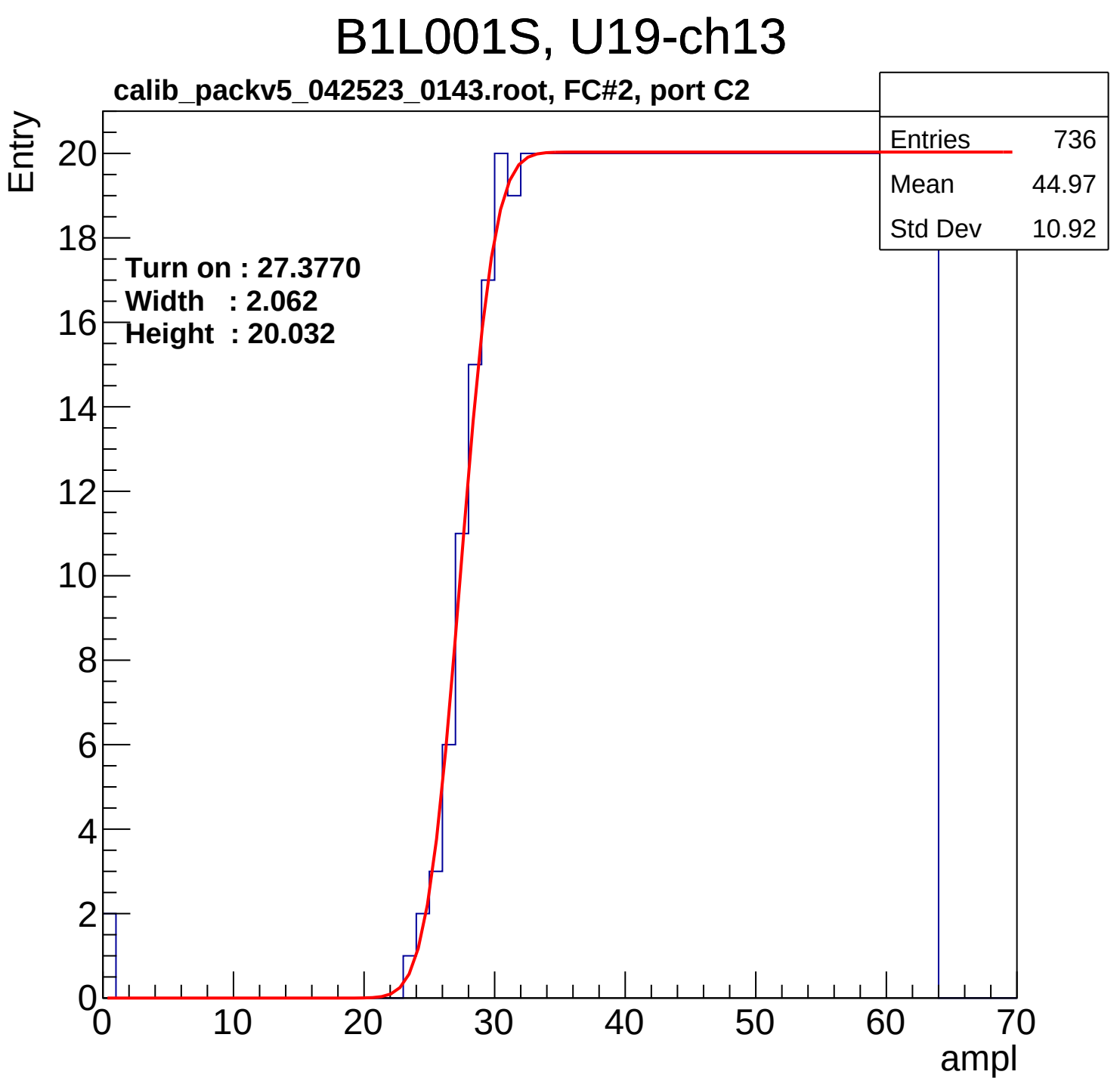
B1L001S, U19-ch13
calib_packv5_042523_0143.root, FC#2, port C2
Entries 736
Mean 44.97
Std Dev 10.92
Turn on : 27.3770
Width : 2.062
Height : 20.032
Entry
ampl
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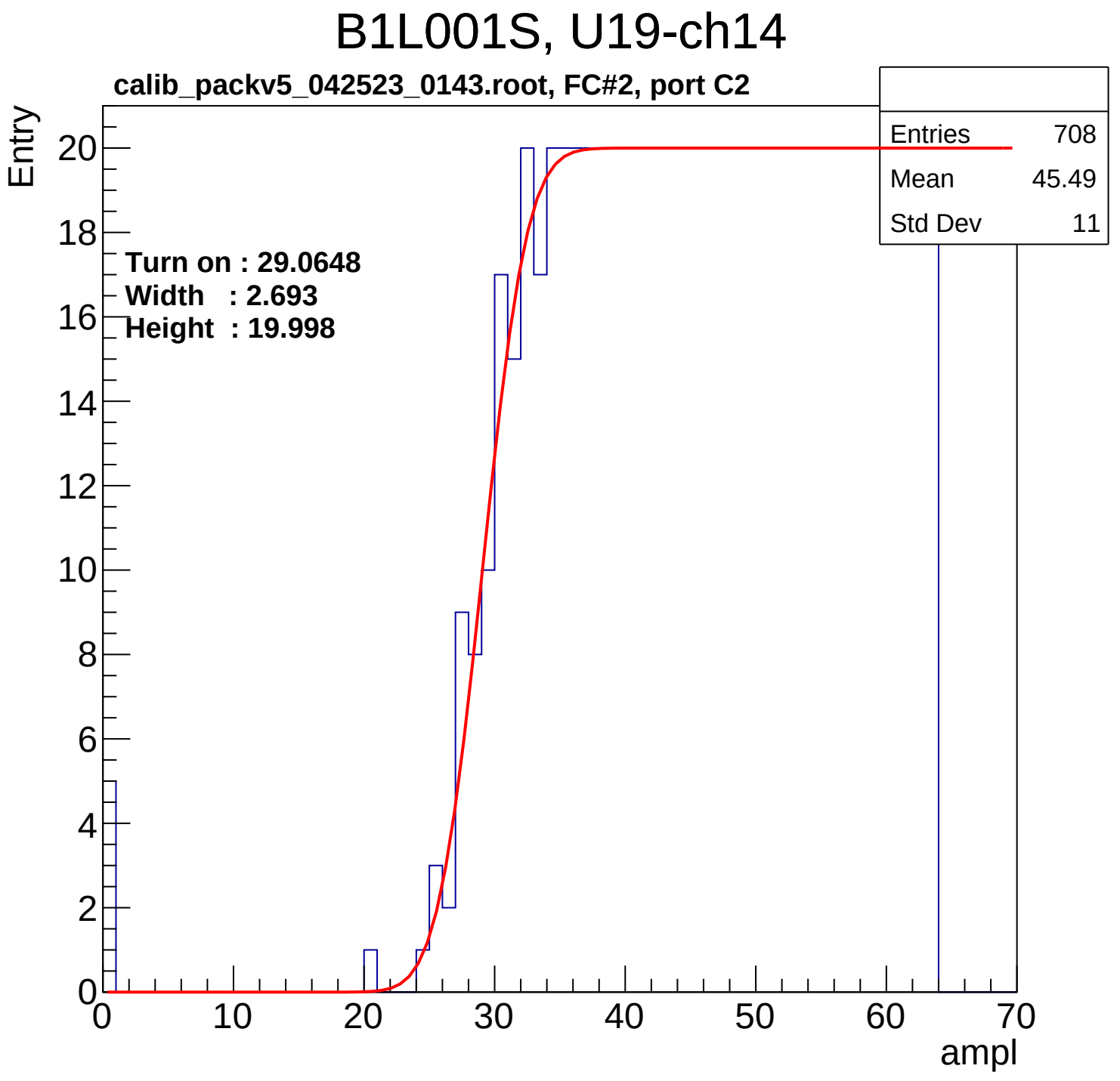
B1L001S, U19-ch14
calib_packv5_042523_0143.root, FC#2, port C2
Entries 708
Mean 45.49
Std Dev 11
Turn on : 29.0648
Width : 2.693
Height : 19.998
Entry
ampl
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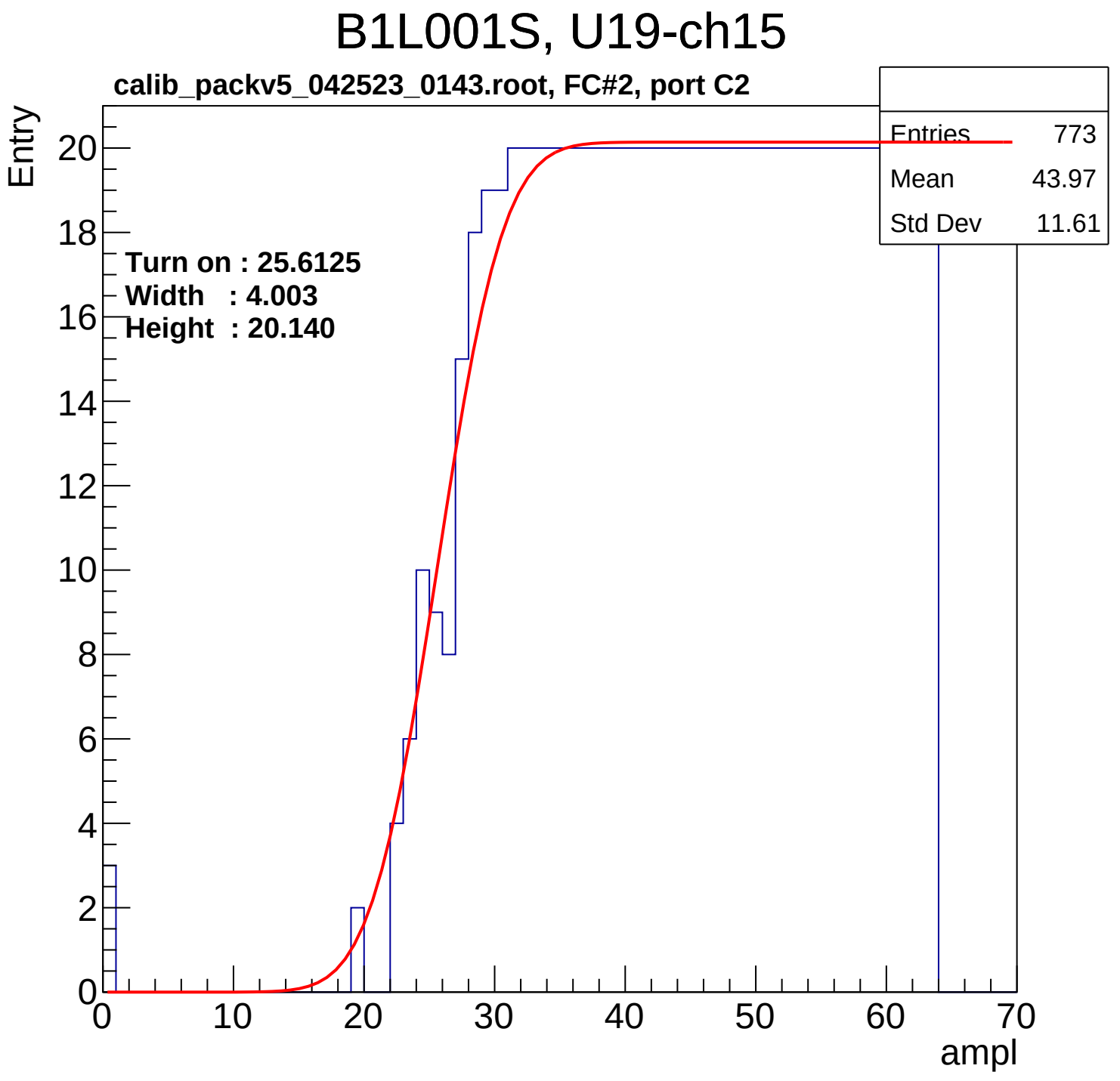
B1L001S, U19-ch15
calib_packv5_042523_0143.root, FC#2, port C2
Entries 773
Mean 43.97
Std Dev 11.61
Turn on : 25.6125
Width : 4.003
Height : 20.140
Entry
ampl
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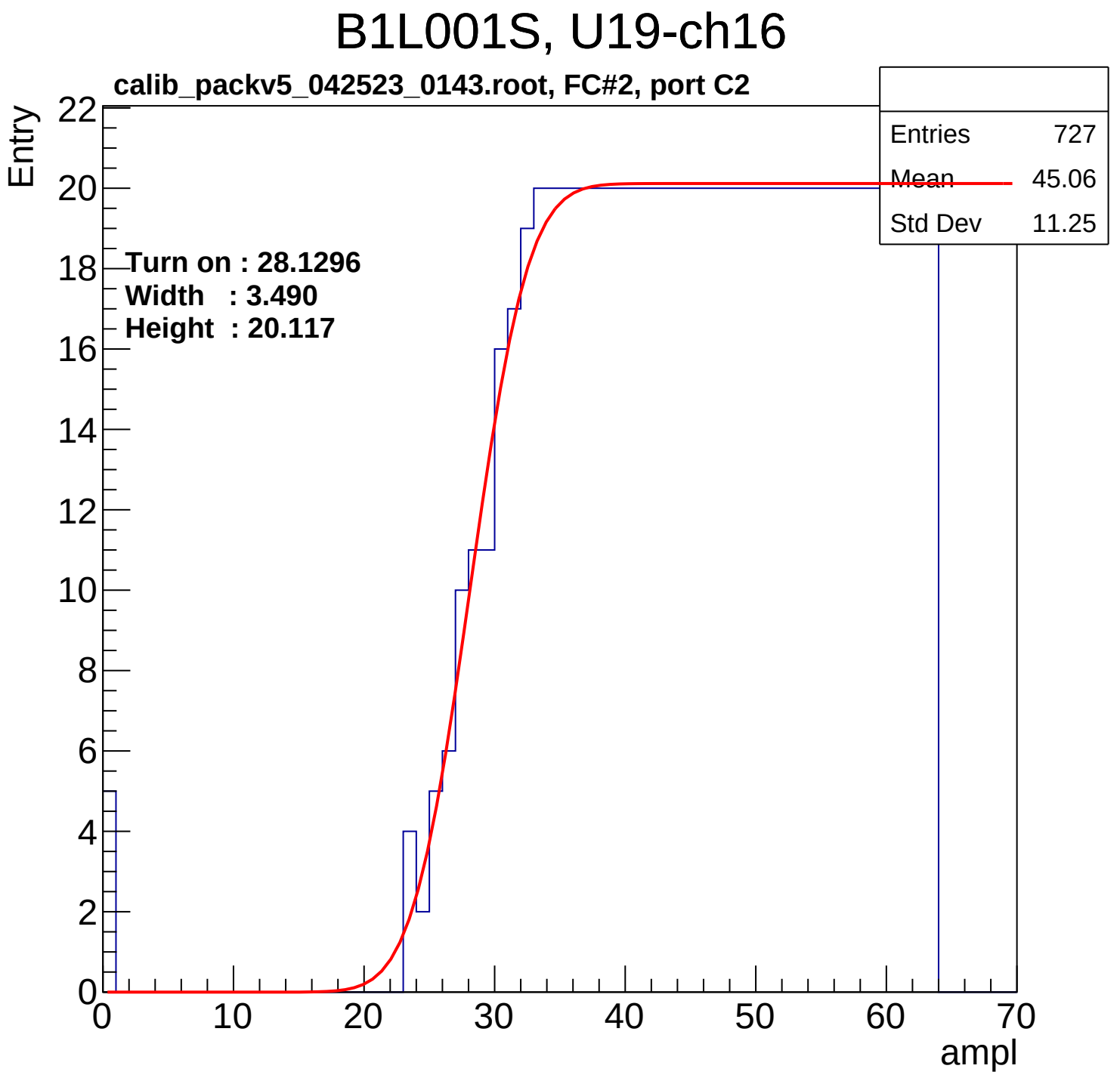
B1L001S, U19-ch16
calib_packv5_042523_0143.root, FC#2, port C2
Entries 727
Mean 45.06
Std Dev 11.25
Turn on : 28.1296
Width : 3.490
Height : 20.117
Entry
ampl
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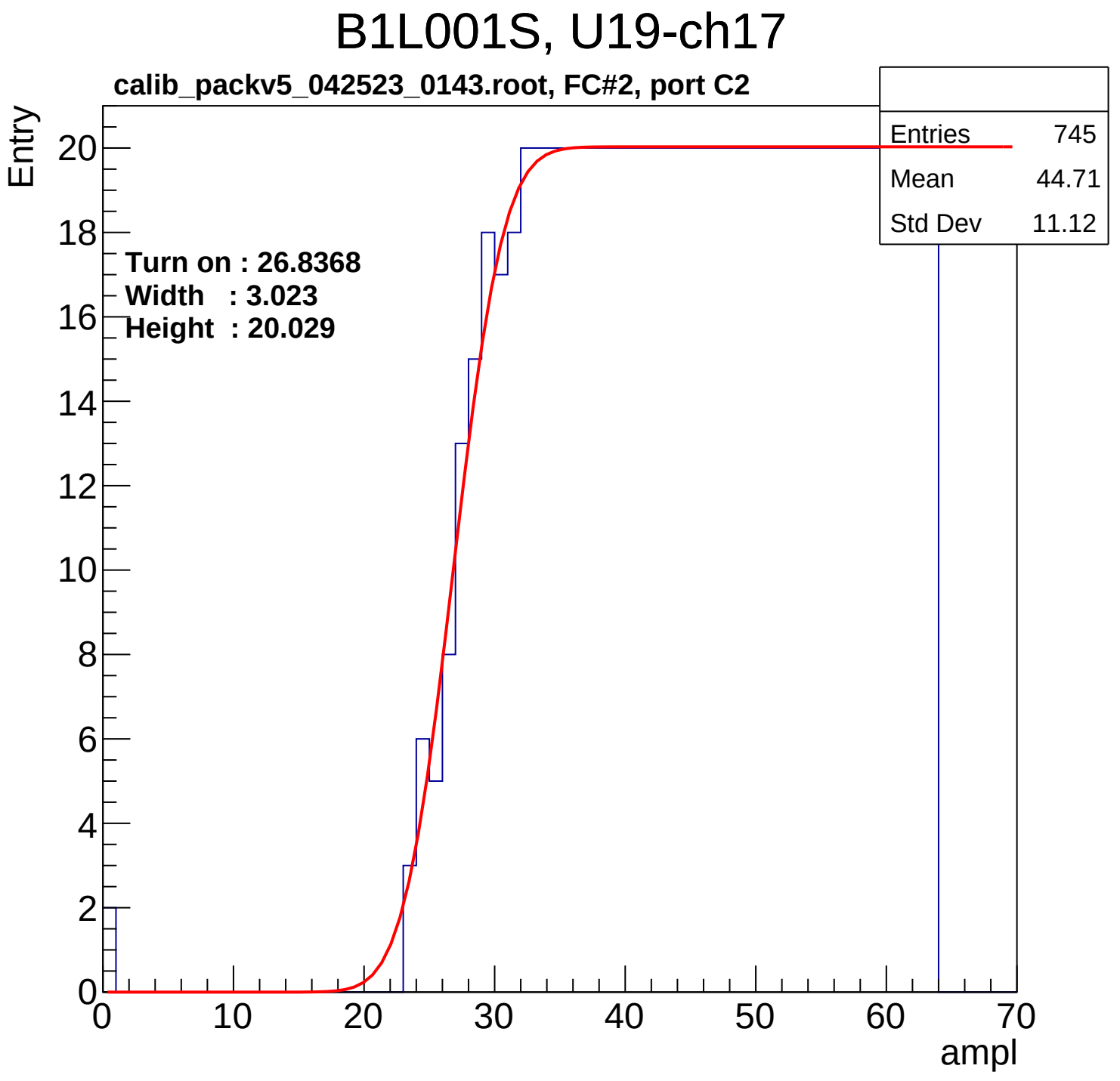
B1L001S, U19-ch17
calib_packv5_042523_0143.root, FC#2, port C2
Entries 745
Mean 44.71
Std Dev 11.12
Turn on : 26.8368
Width : 3.023
Height : 20.029
Entry
ampl
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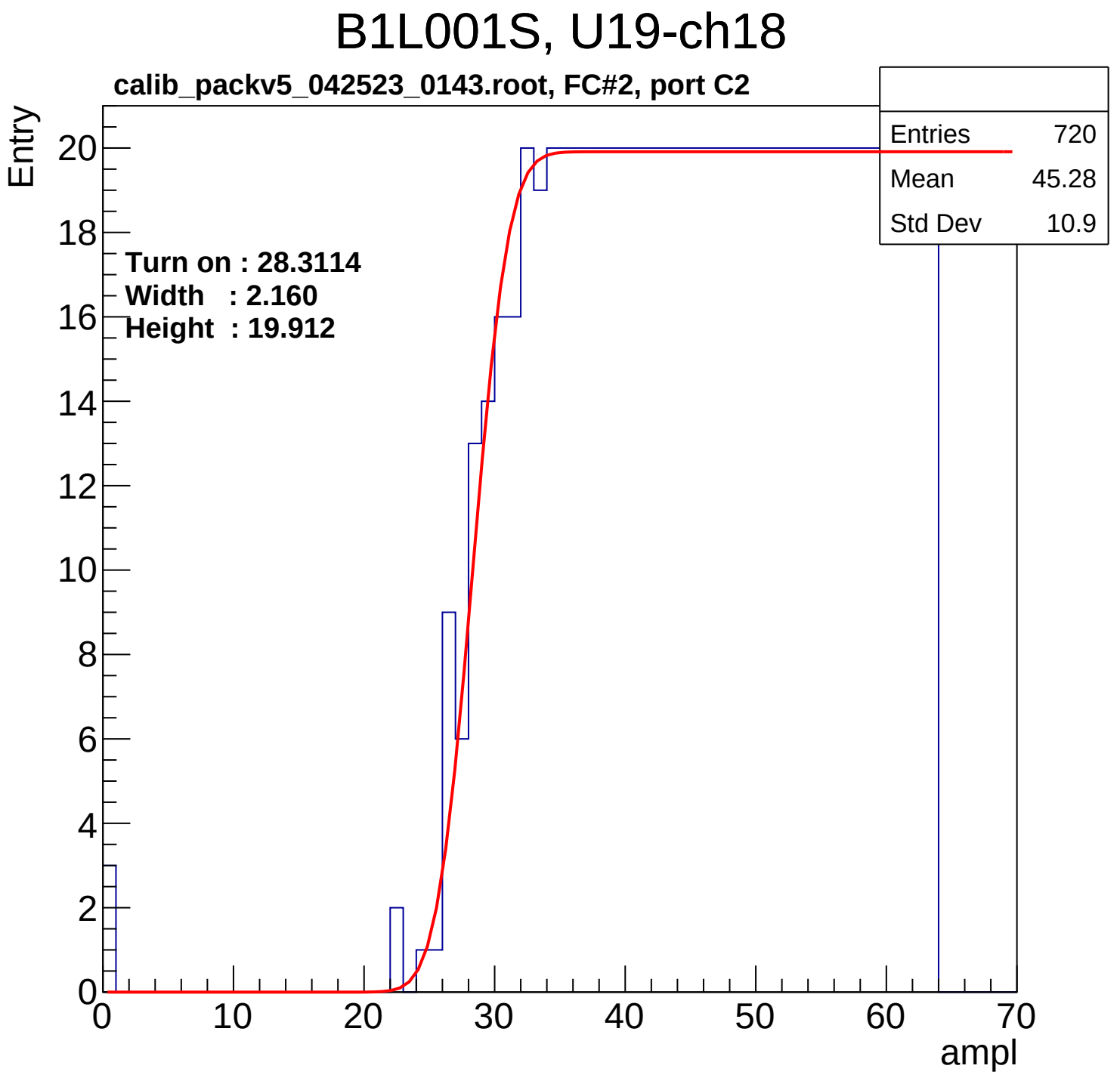
B1L001S, U19-ch18
calib_packv5_042523_0143.root, FC#2, port C2
Entries 720
Mean 45.28
Std Dev 10.9
Turn on : 28.3114
Width : 2.160
Height : 19.912
Entry
ampl
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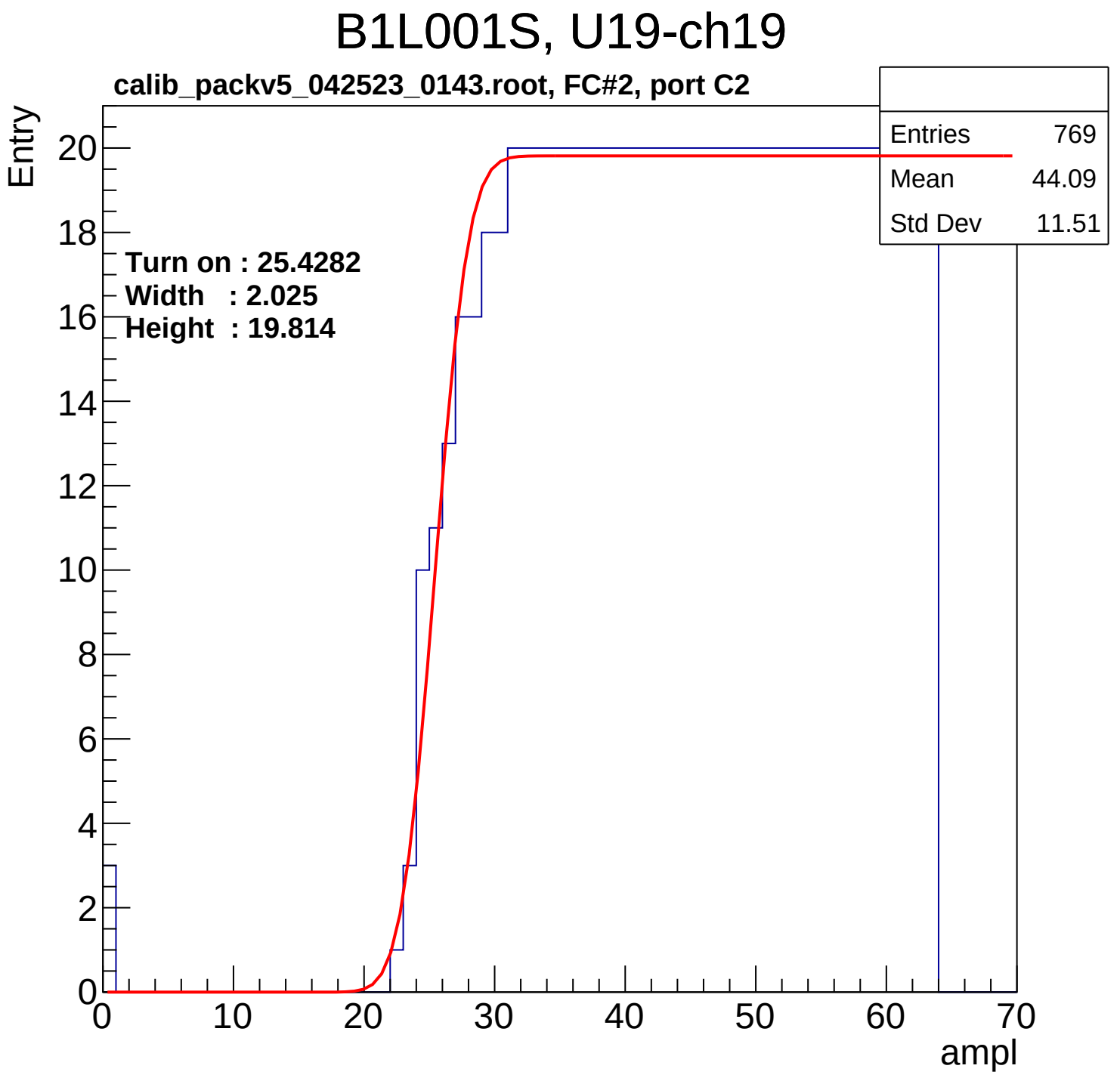
B1L001S, U19-ch19
calib_packv5_042523_0143.root, FC#2, port C2
Entries 769
Mean 44.09
Std Dev 11.51
Turn on : 25.4282
Width : 2.025
Height : 19.814
Entry
ampl
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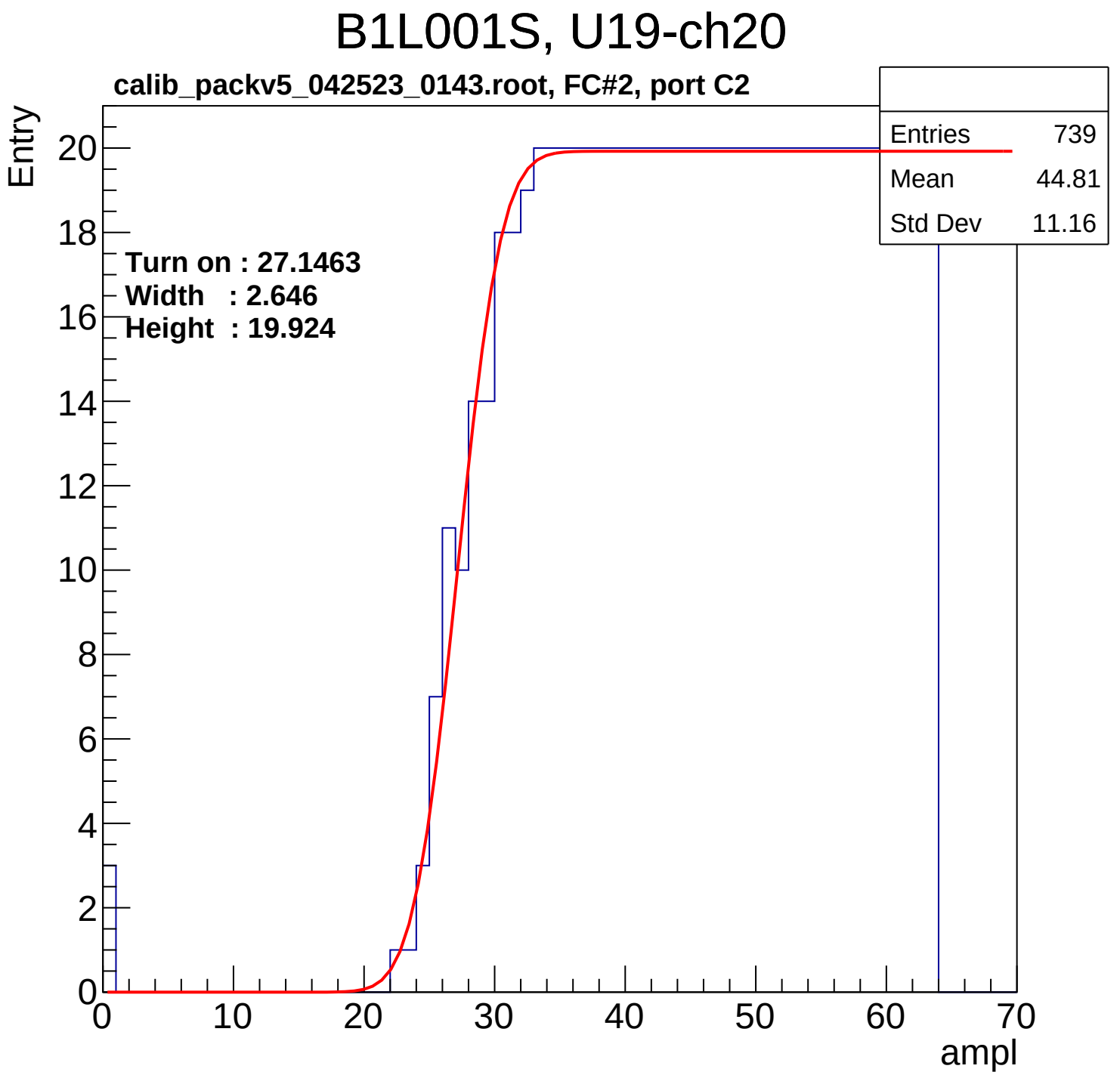
B1L001S, U19-ch20
calib_packv5_042523_0143.root, FC#2, port C2
Entries 739
Mean 44.81
Std Dev 11.16
Turn on : 27.1463
Width : 2.646
Height : 19.924
Entry
ampl
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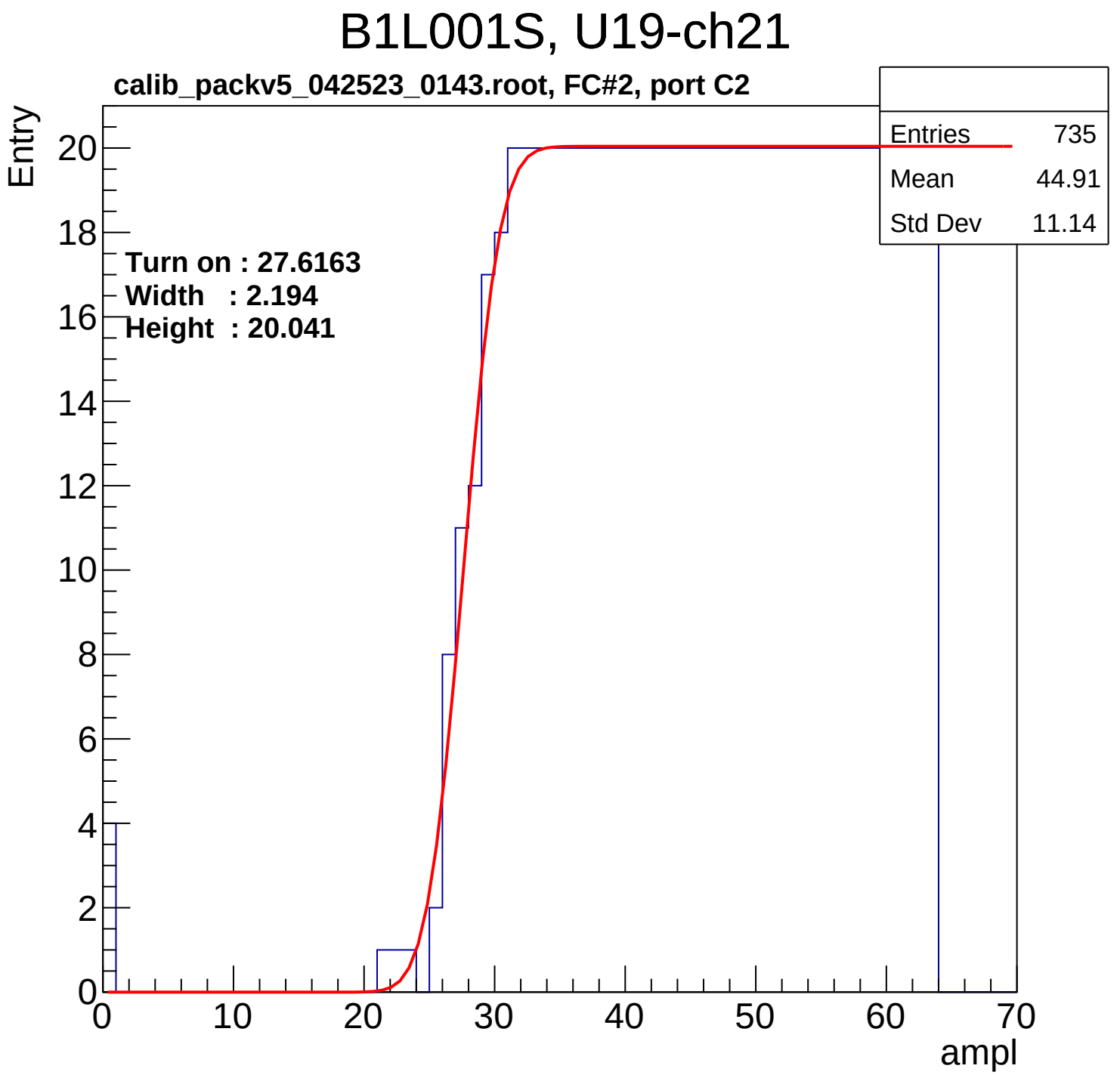
B1L001S, U19-ch21
calib_packv5_042523_0143.root, FC#2, port C2
Entries 735
Mean 44.91
Std Dev 11.14
Turn on : 27.6163
Width : 2.194
Height : 20.041
Entry
ampl
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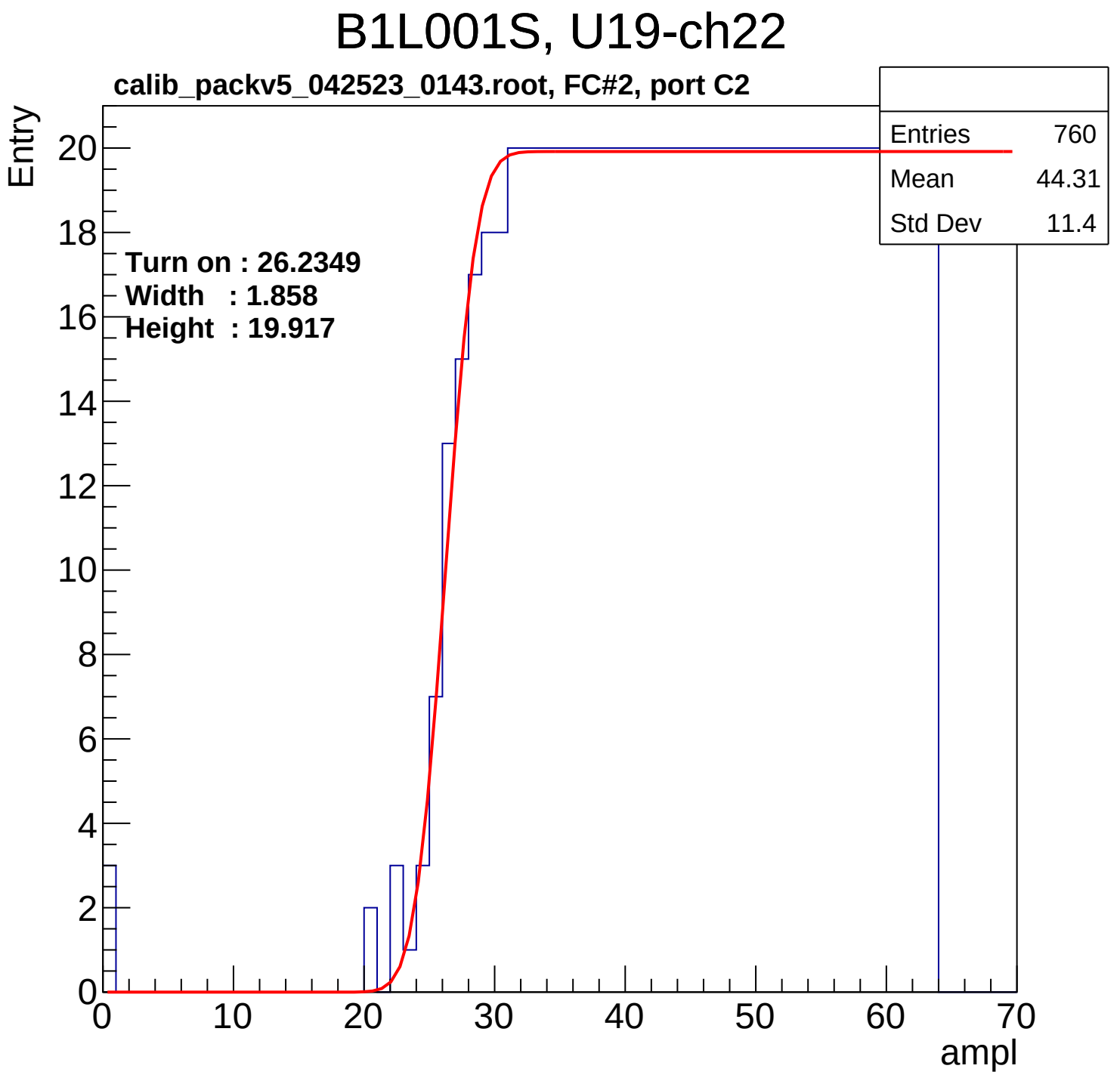
B1L001S, U19-ch22
calib_packv5_042523_0143.root, FC#2, port C2
Entries 760
Mean 44.31
Std Dev 11.4
Turn on : 26.2349
Width : 1.858
Height : 19.917
Entry
ampl
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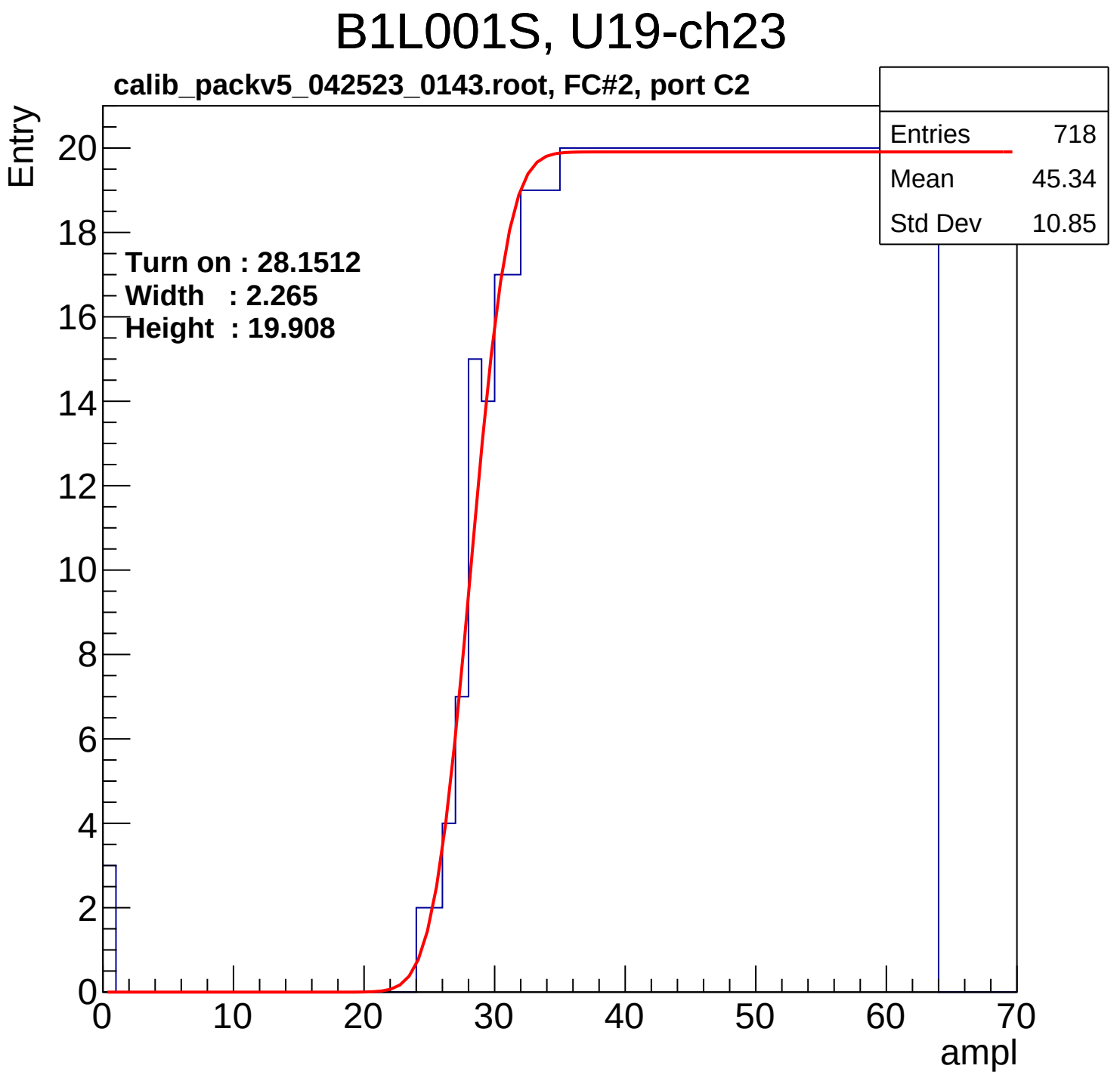
B1L001S, U19-ch23
calib_packv5_042523_0143.root, FC#2, port C2
Entries 718
Mean 45.34
Std Dev 10.85
Turn on : 28.1512
Width : 2.265
Height : 19.908
Entry
ampl
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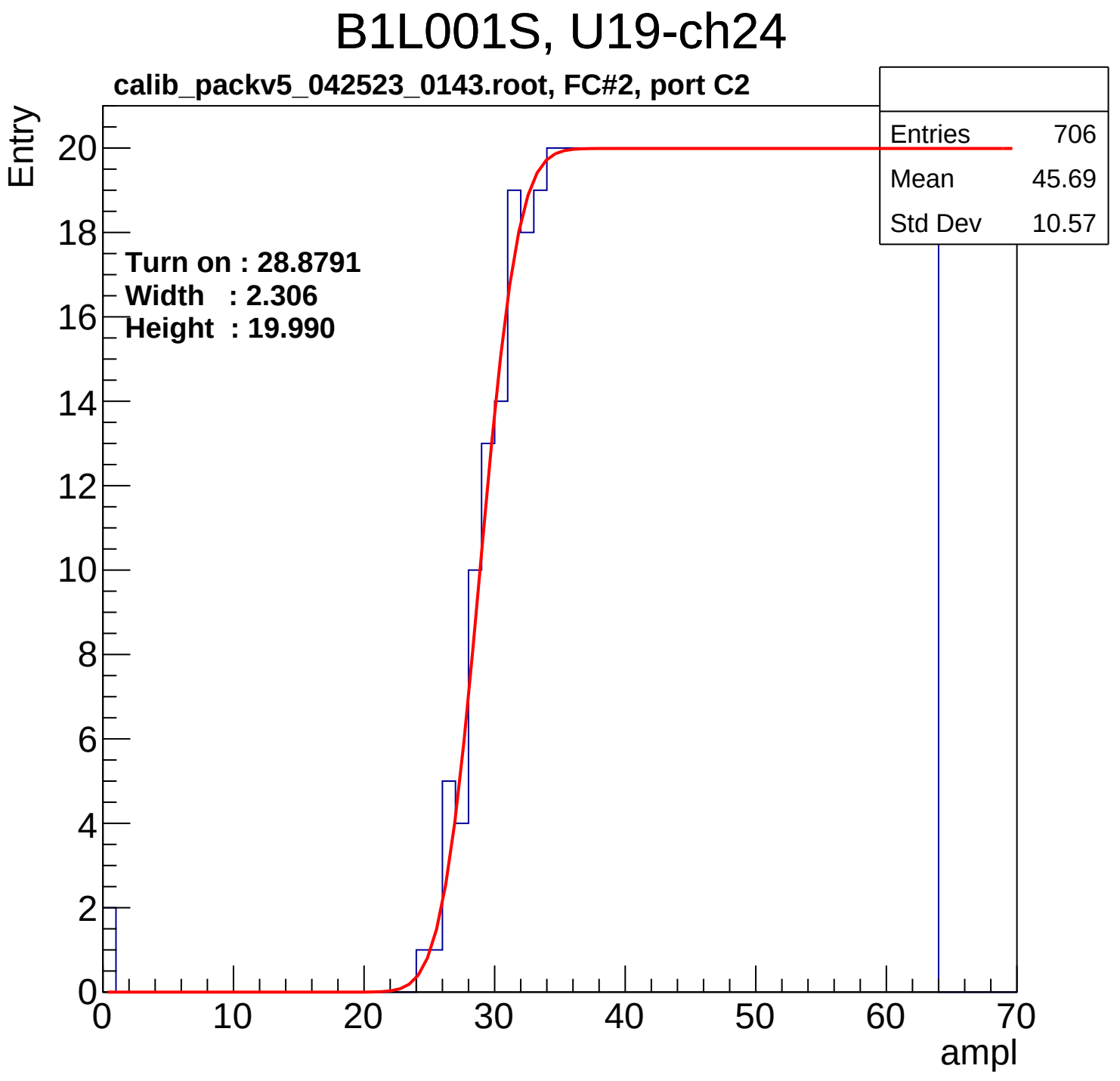
B1L001S, U19-ch24
calib_packv5_042523_0143.root, FC#2, port C2
Entries 706
Mean 45.69
Std Dev 10.57
Turn on : 28.8791
Width : 2.306
Height : 19.990
Entry
ampl
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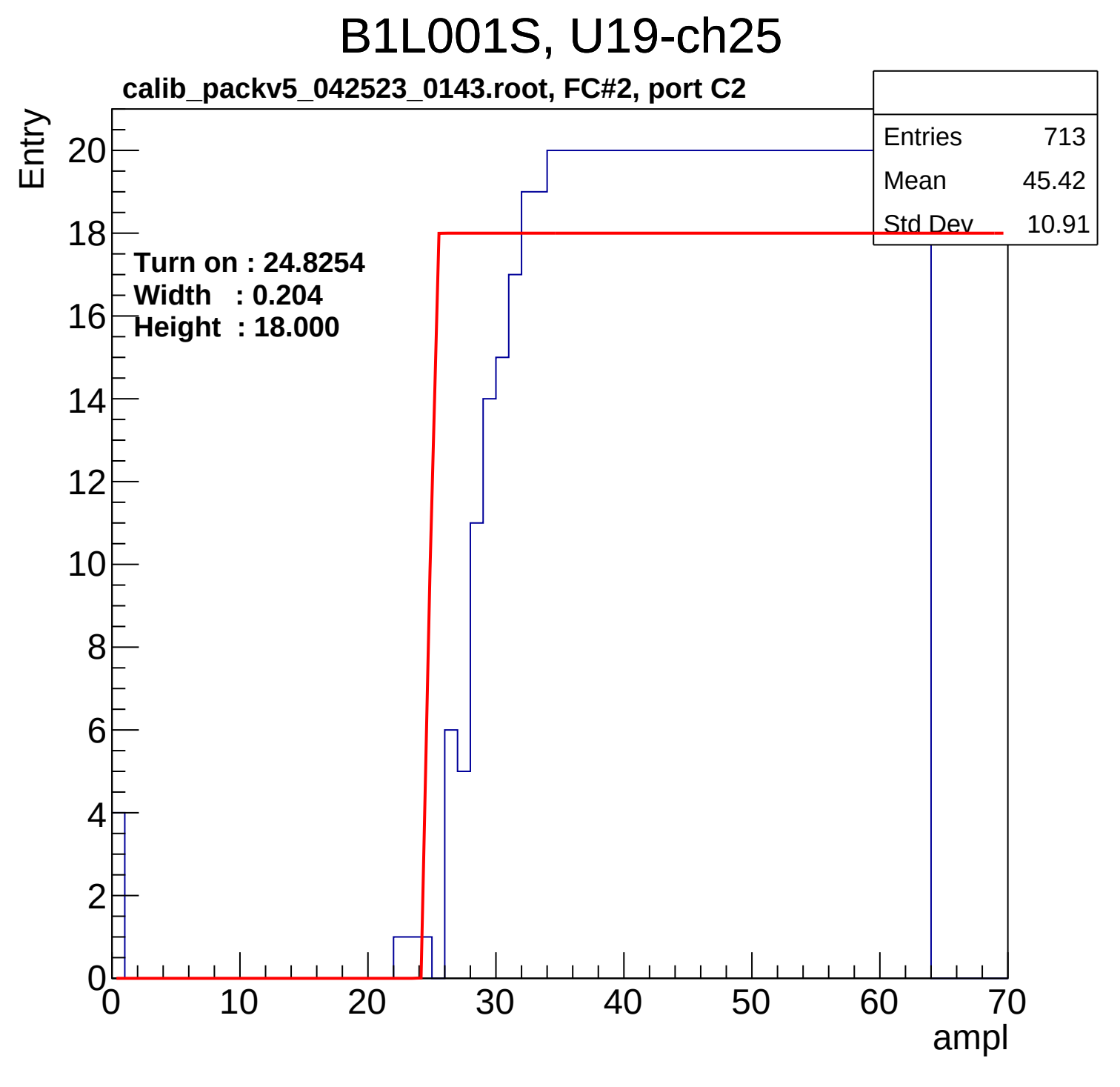
B1L001S, U19-ch25
calib_packv5_042523_0143.root, FC#2, port C2
Entries 713
Mean 45.42
Std Dev 10.91
Turn on : 24.8254
Width : 0.204
Height : 18.000
Entry
ampl
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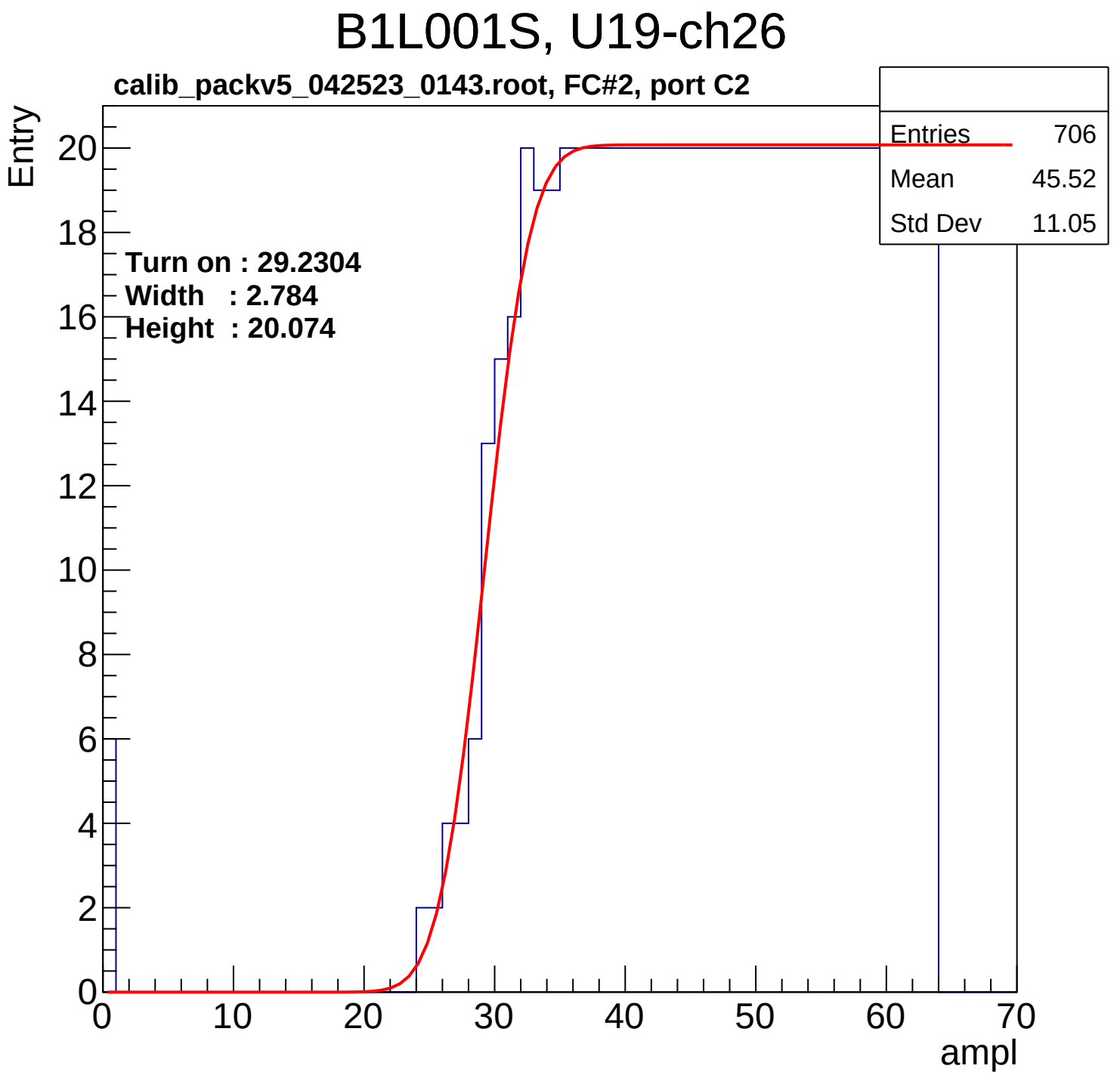
B1L001S, U19-ch26
calib_packv5_042523_0143.root, FC#2, port C2
Entries 706
Mean 45.52
Std Dev 11.05
Turn on : 29.2304
Width : 2.784
Height : 20.074
Entry
ampl
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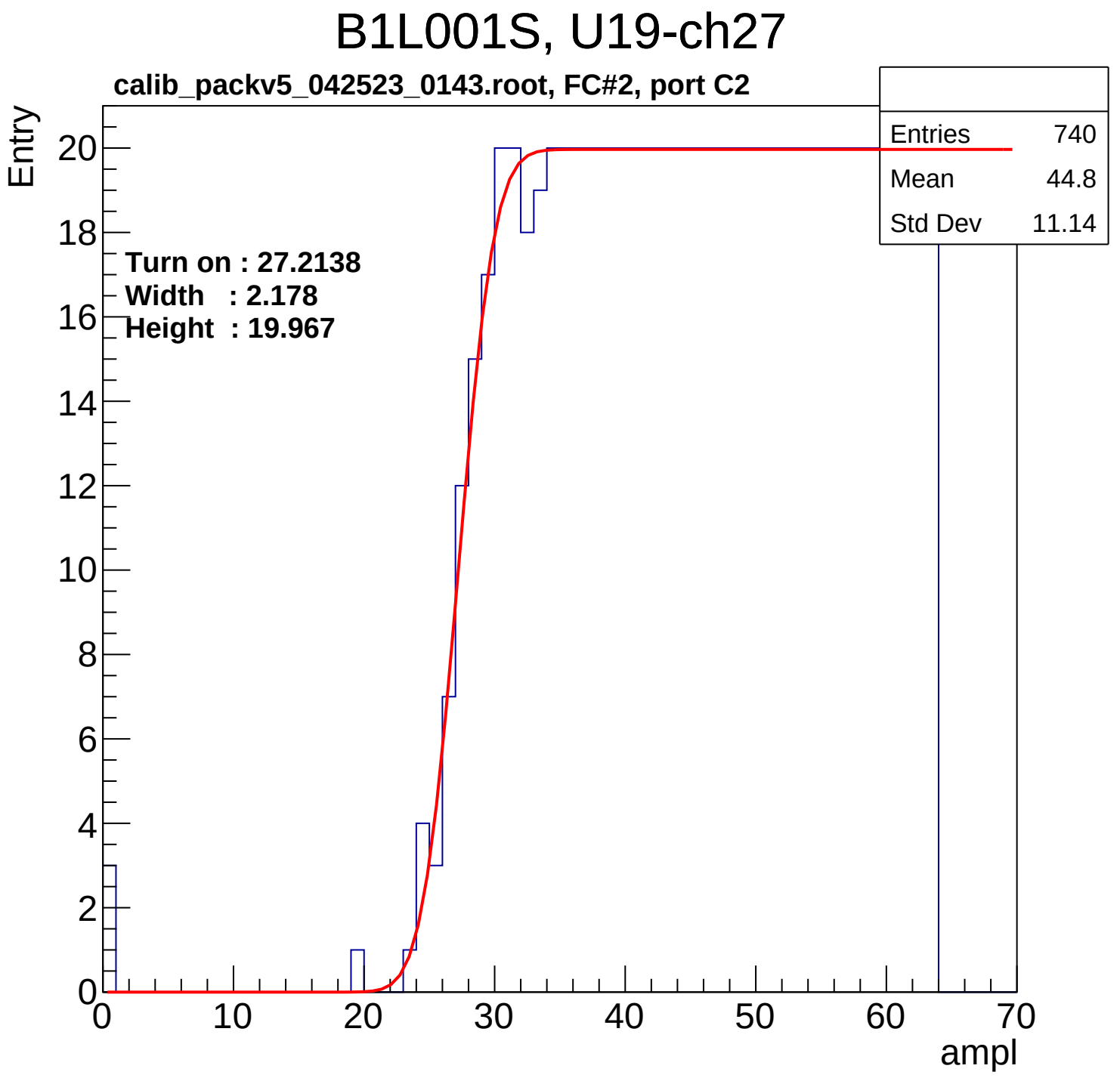
B1L001S, U19-ch27
calib_packv5_042523_0143.root, FC#2, port C2
Entries 740
Mean 44.8
Std Dev 11.14
Turn on : 27.2138
Width : 2.178
Height : 19.967
Entry
ampl
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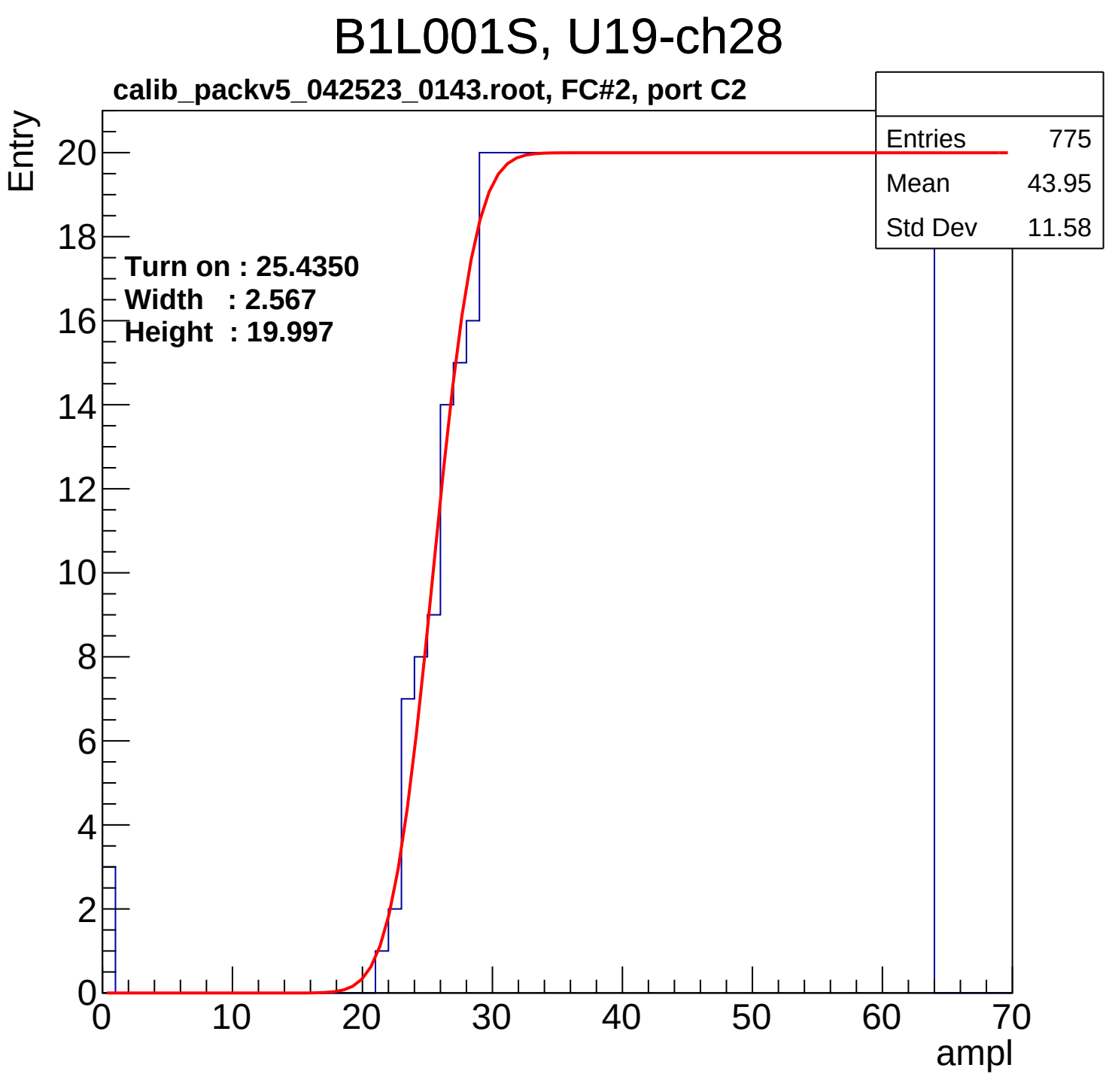
B1L001S, U19-ch28
calib_packv5_042523_0143.root, FC#2, port C2
Entries 775
Mean 43.95
Std Dev 11.58
Turn on : 25.4350
Width : 2.567
Height : 19.997
Entry
ampl
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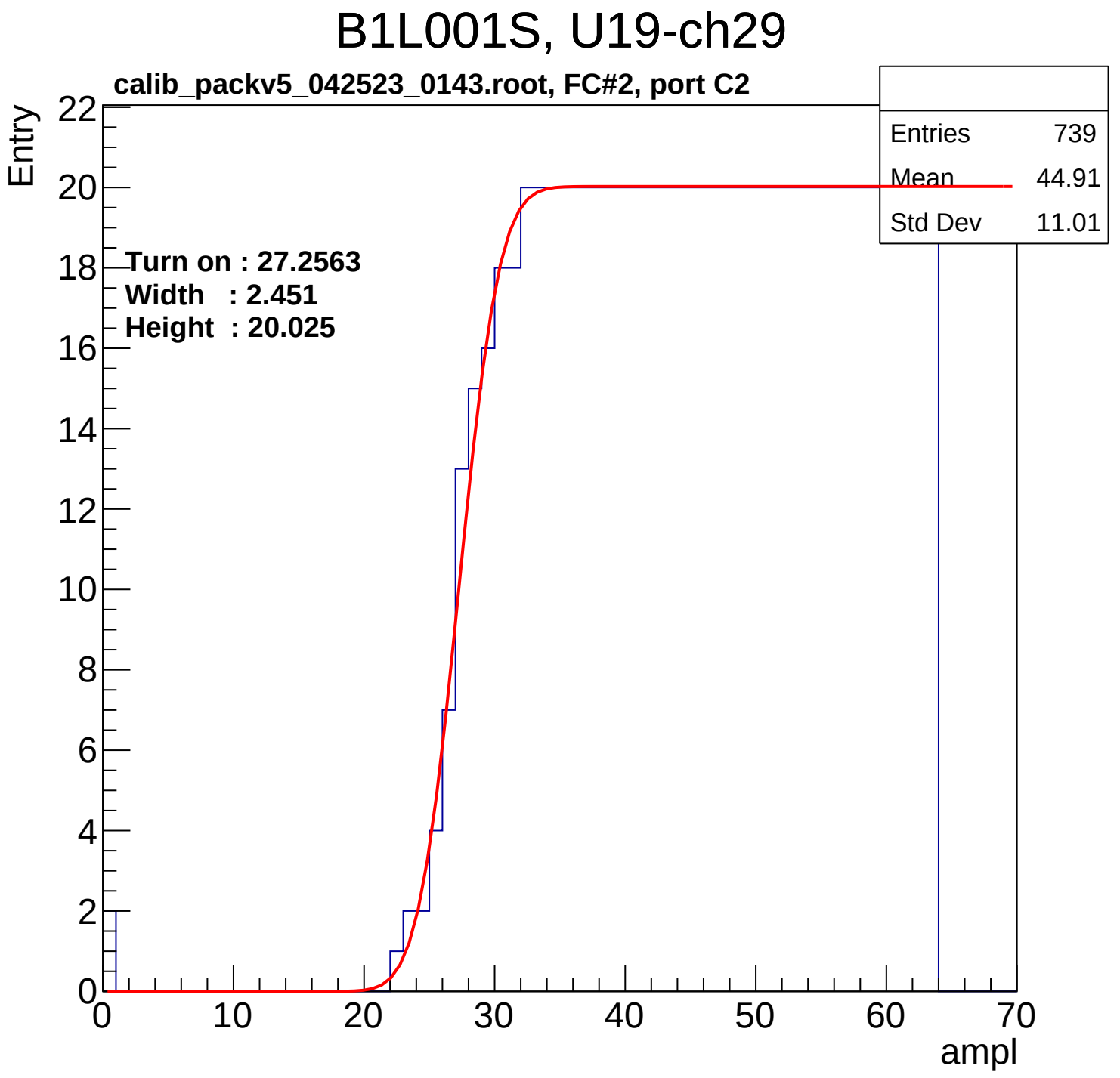
B1L001S, U19-ch29
calib_packv5_042523_0143.root, FC#2, port C2
Entries 739
Mean 44.91
Std Dev 11.01
Turn on : 27.2563
Width : 2.451
Height : 20.025
Entry
ampl
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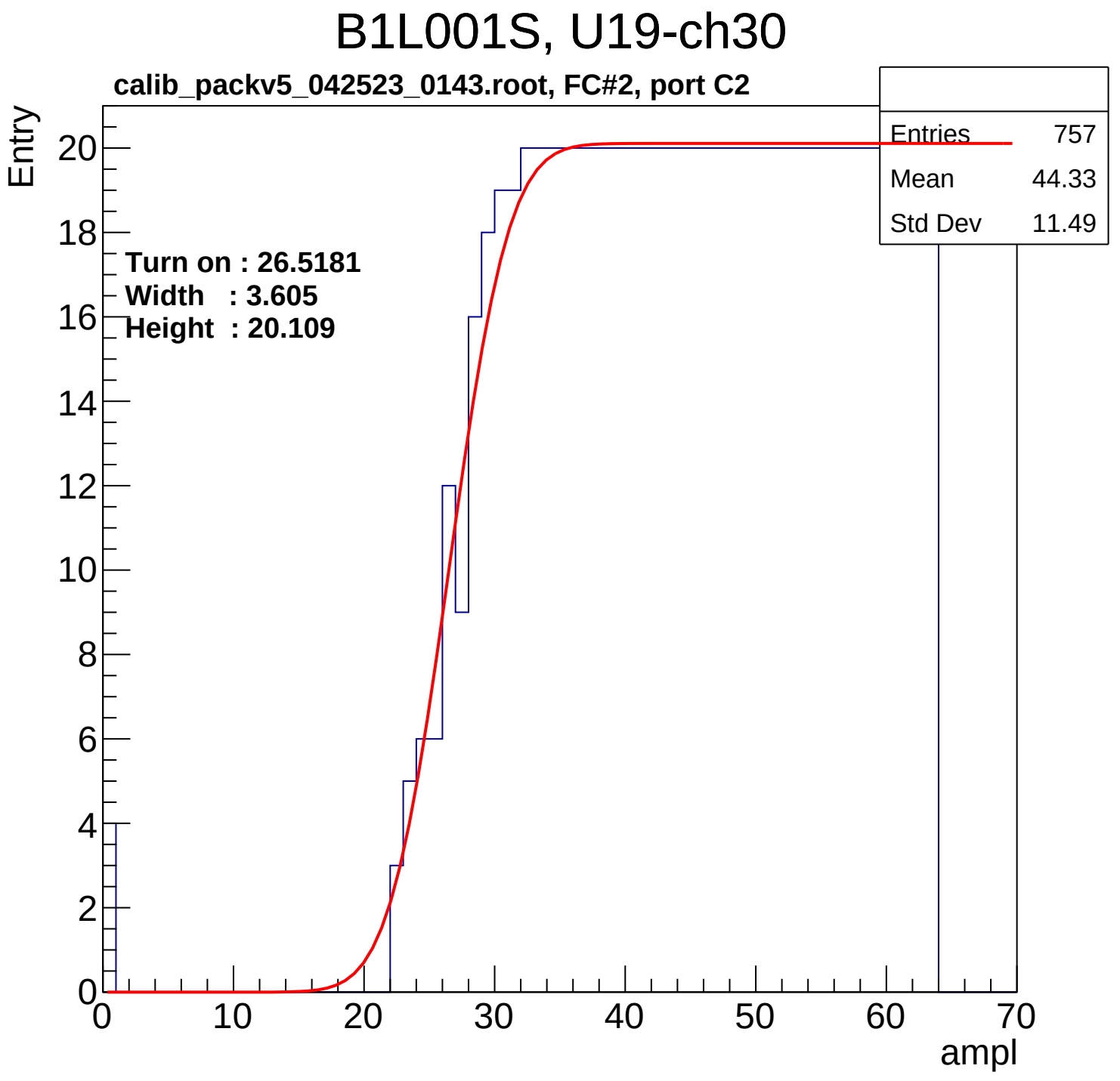
B1L001S, U19-ch30
calib_packv5_042523_0143.root, FC#2, port C2
Entries 757
Mean 44.33
Std Dev 11.49
Turn on : 26.5181
Width : 3.605
Height : 20.109
Entry
ampl
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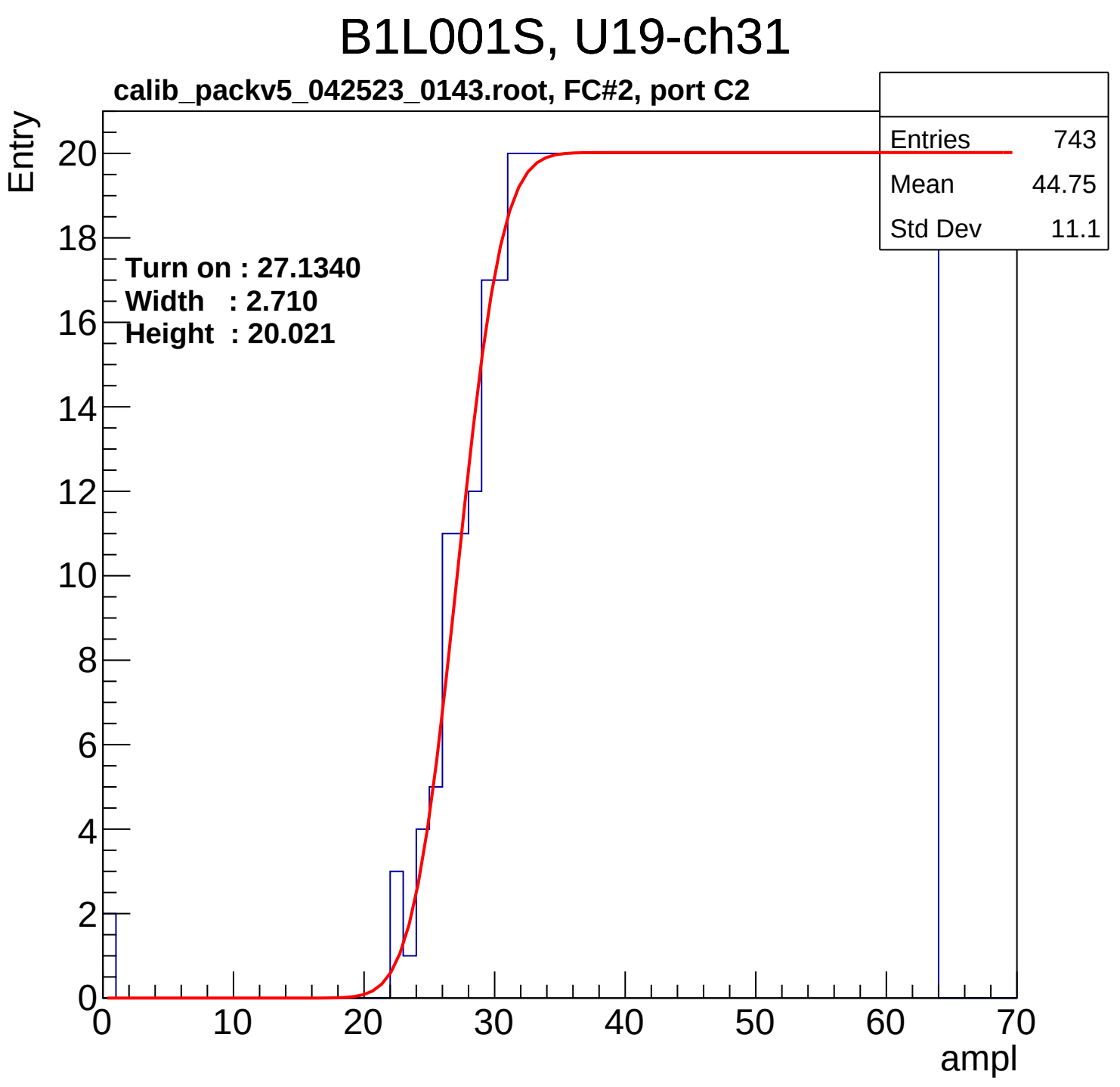
B1L001S, U19-ch31
calib_packv5_042523_0143.root, FC#2, port C2
Entries 743
Mean 44.75
Std Dev 11.1
Turn on : 27.1340
Width : 2.710
Height : 20.021
Entry
ampl
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6
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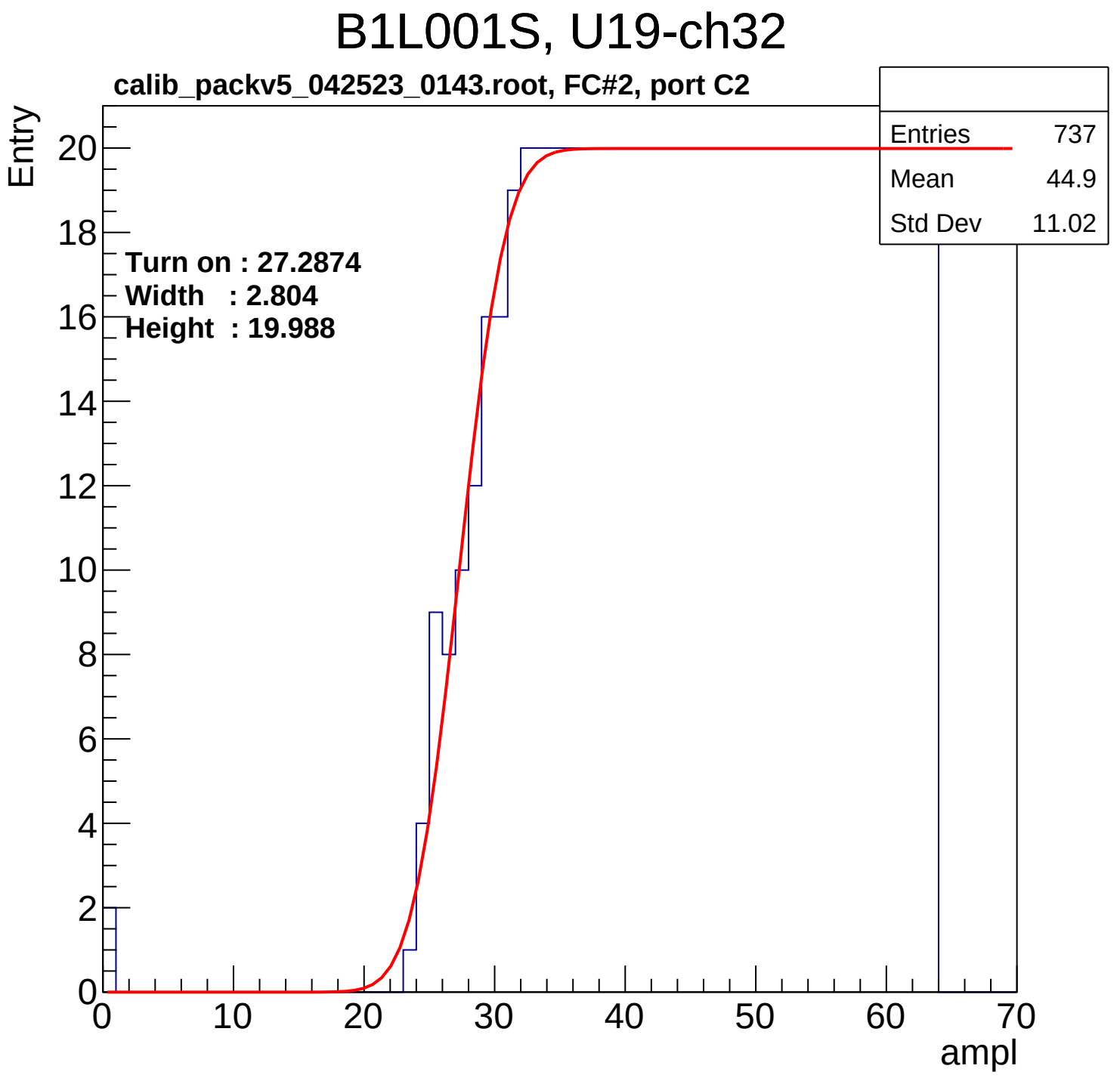
B1L001S, U19-ch32
calib_packv5_042523_0143.root, FC#2, port C2
Entries 737
Mean 44.9
Std Dev 11.02
Turn on : 27.2874
Width : 2.804
Height : 19.988
Entry
ampl
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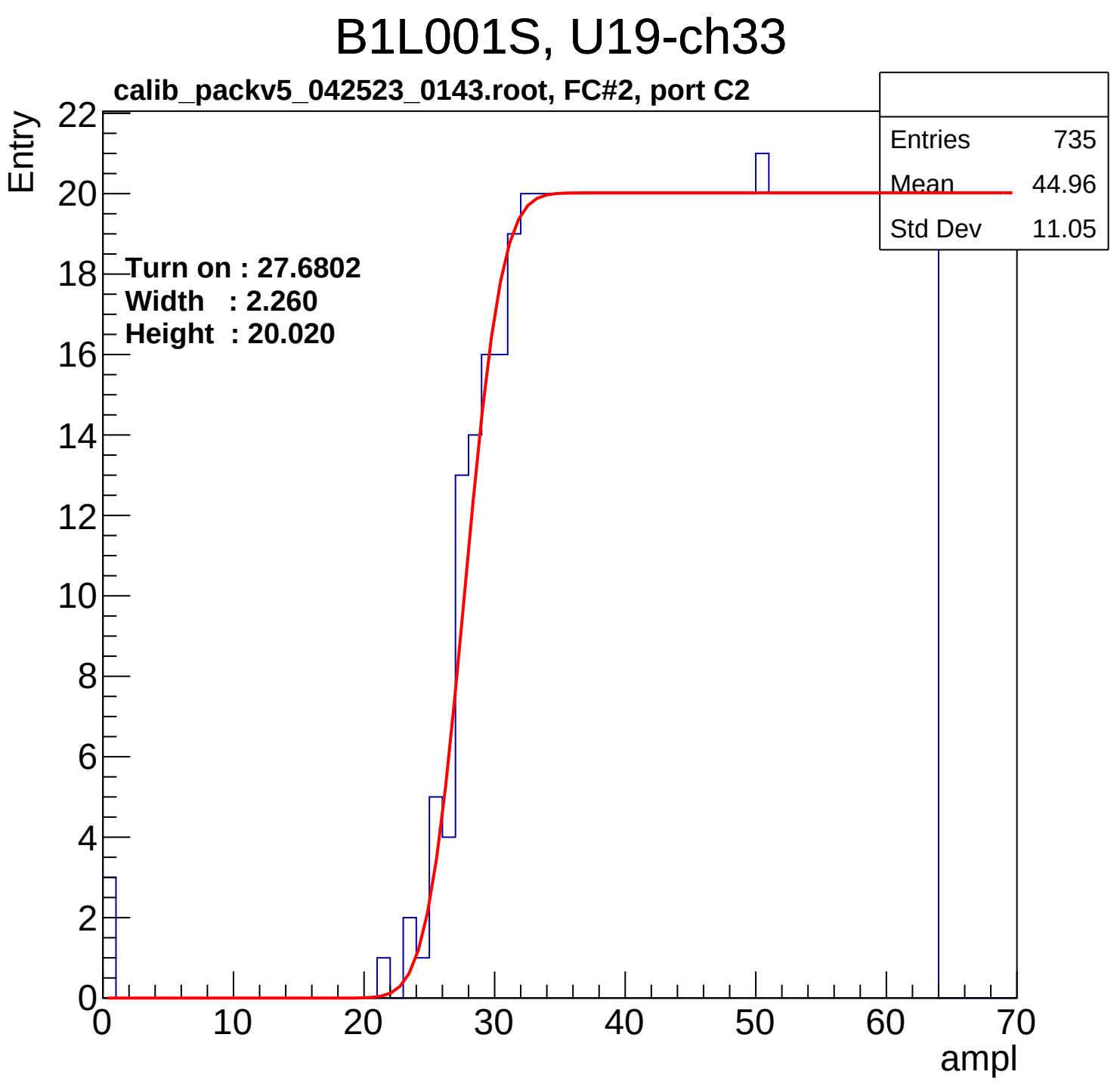
B1L001S, U19-ch33
calib_packv5_042523_0143.root, FC#2, port C2
Entries 735
Mean 44.96
Std Dev 11.05
Turn on : 27.6802
Width : 2.260
Height : 20.020
Entry
ampl
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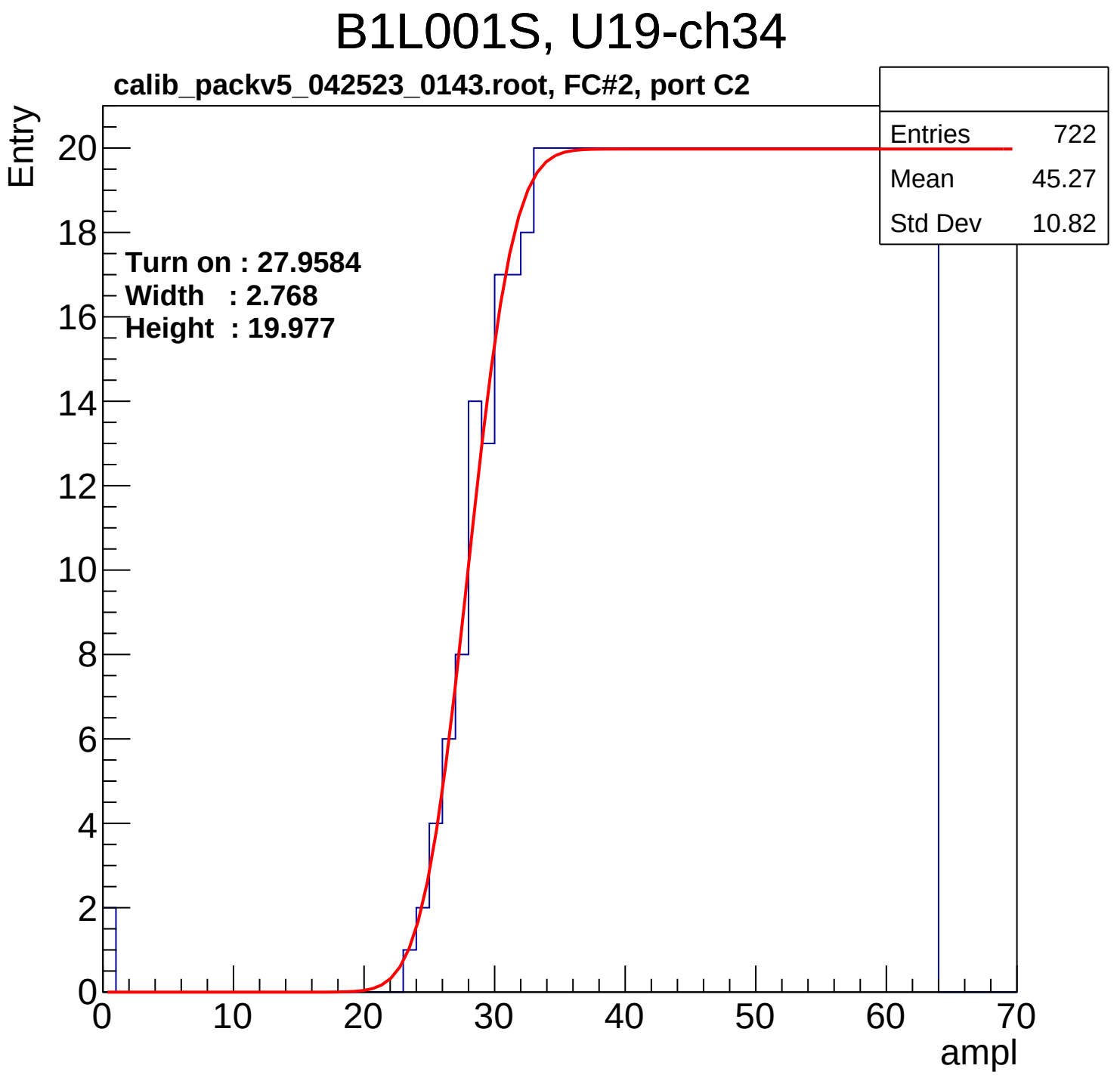
B1L001S, U19-ch34
calib_packv5_042523_0143.root, FC#2, port C2
Entries 722
Mean 45.27
Std Dev 10.82
Turn on : 27.9584
Width : 2.768
Height : 19.977
Entry
ampl
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6
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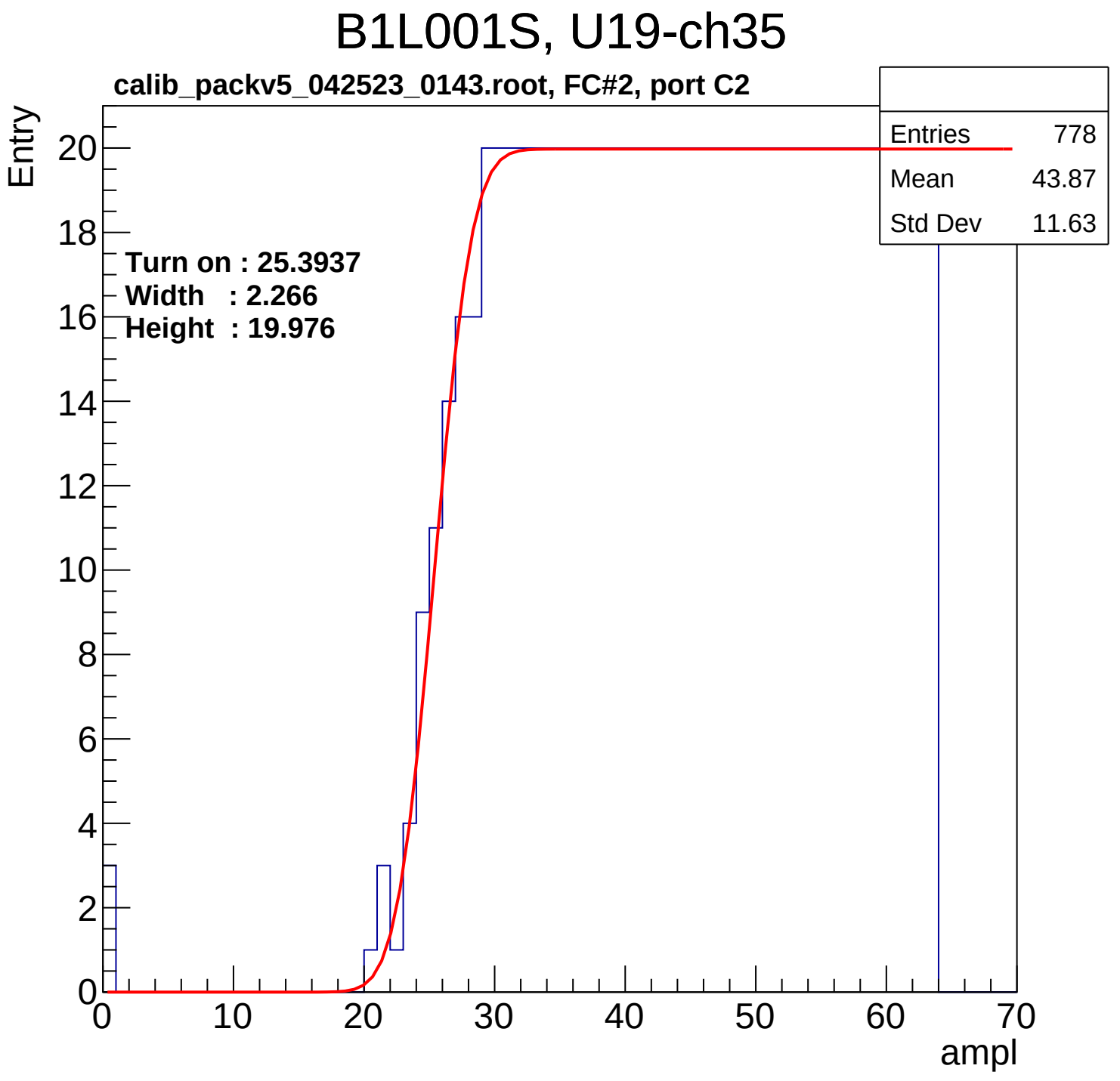
B1L001S, U19-ch35
calib_packv5_042523_0143.root, FC#2, port C2
Entries 778
Mean 43.87
Std Dev 11.63
Turn on : 25.3937
Width : 2.266
Height : 19.976
Entry
ampl
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6
8
10
12
14
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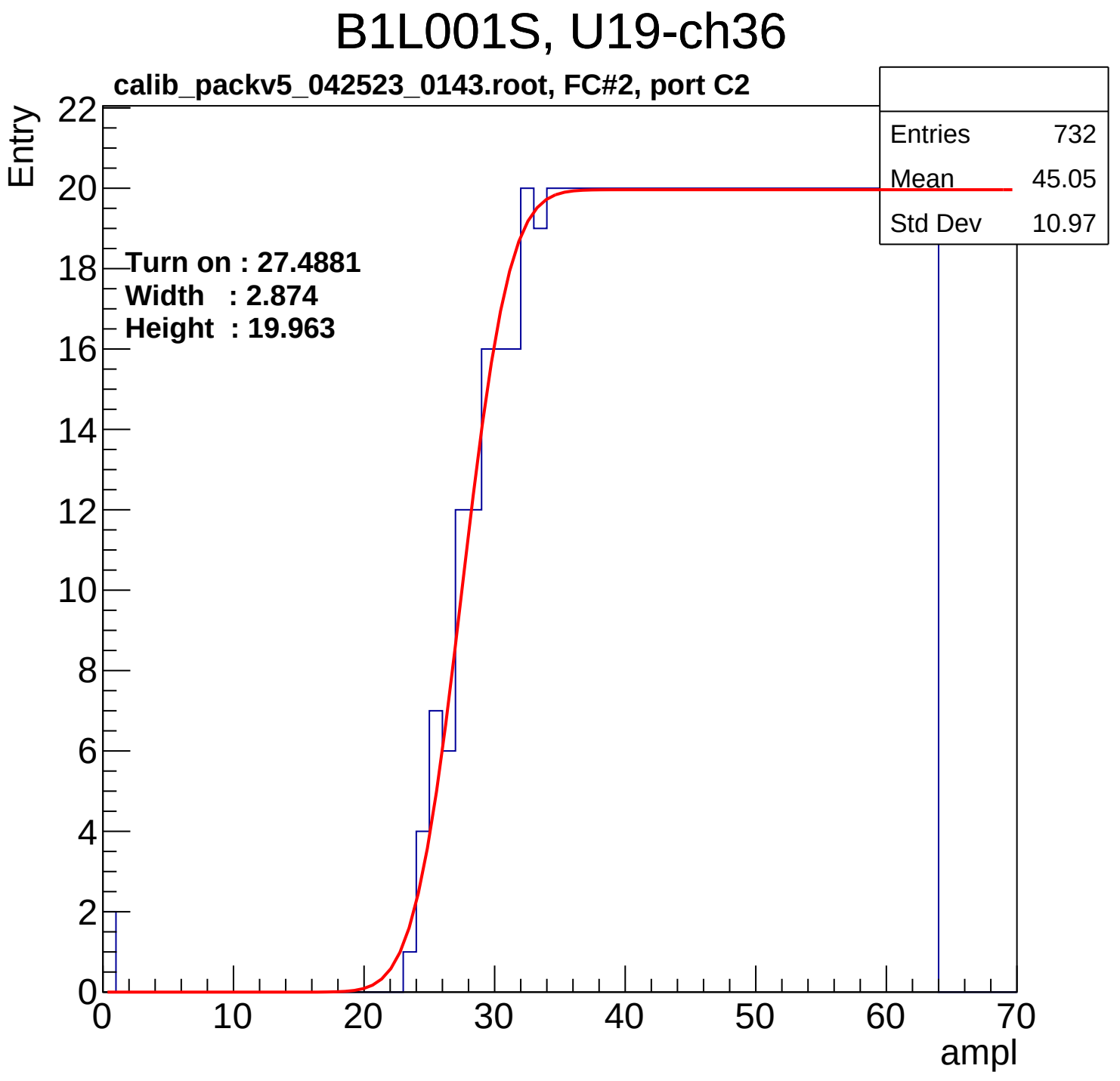
B1L001S, U19-ch36
calib_packv5_042523_0143.root, FC#2, port C2
Entries 732
Mean 45.05
Std Dev 10.97
Turn on : 27.4881
Width : 2.874
Height : 19.963
Entry
ampl
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8
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16
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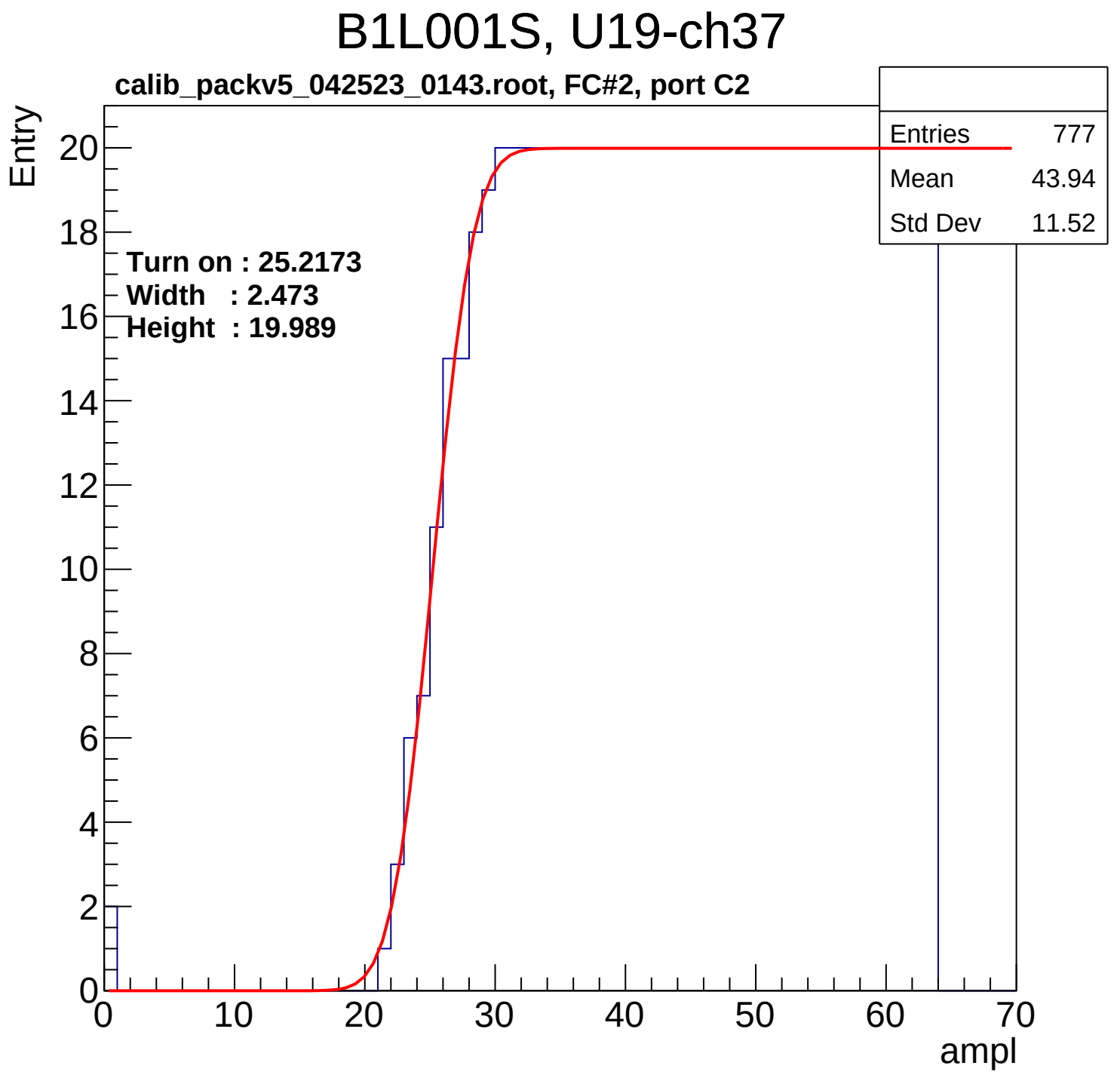
B1L001S, U19-ch37
calib_packv5_042523_0143.root, FC#2, port C2
Entries 777
Mean 43.94
Std Dev 11.52
Turn on : 25.2173
Width : 2.473
Height : 19.989
Entry
ampl
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6
8
10
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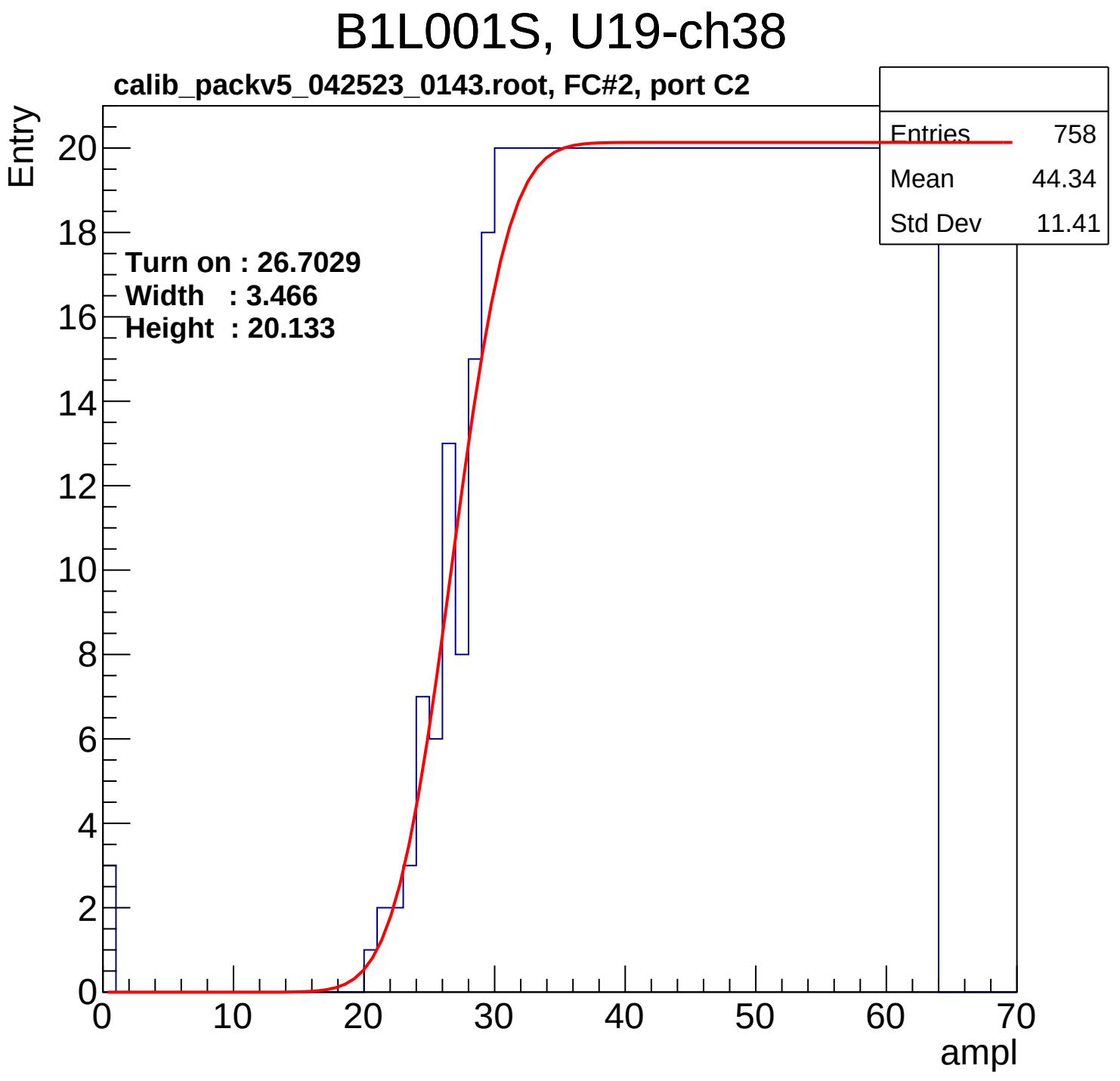
B1L001S, U19-ch38
calib_packv5_042523_0143.root, FC#2, port C2
Entries 758
Mean 44.34
Std Dev 11.41
Turn on : 26.7029
Width : 3.466
Height : 20.133
Entry
ampl
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6
8
10
12
14
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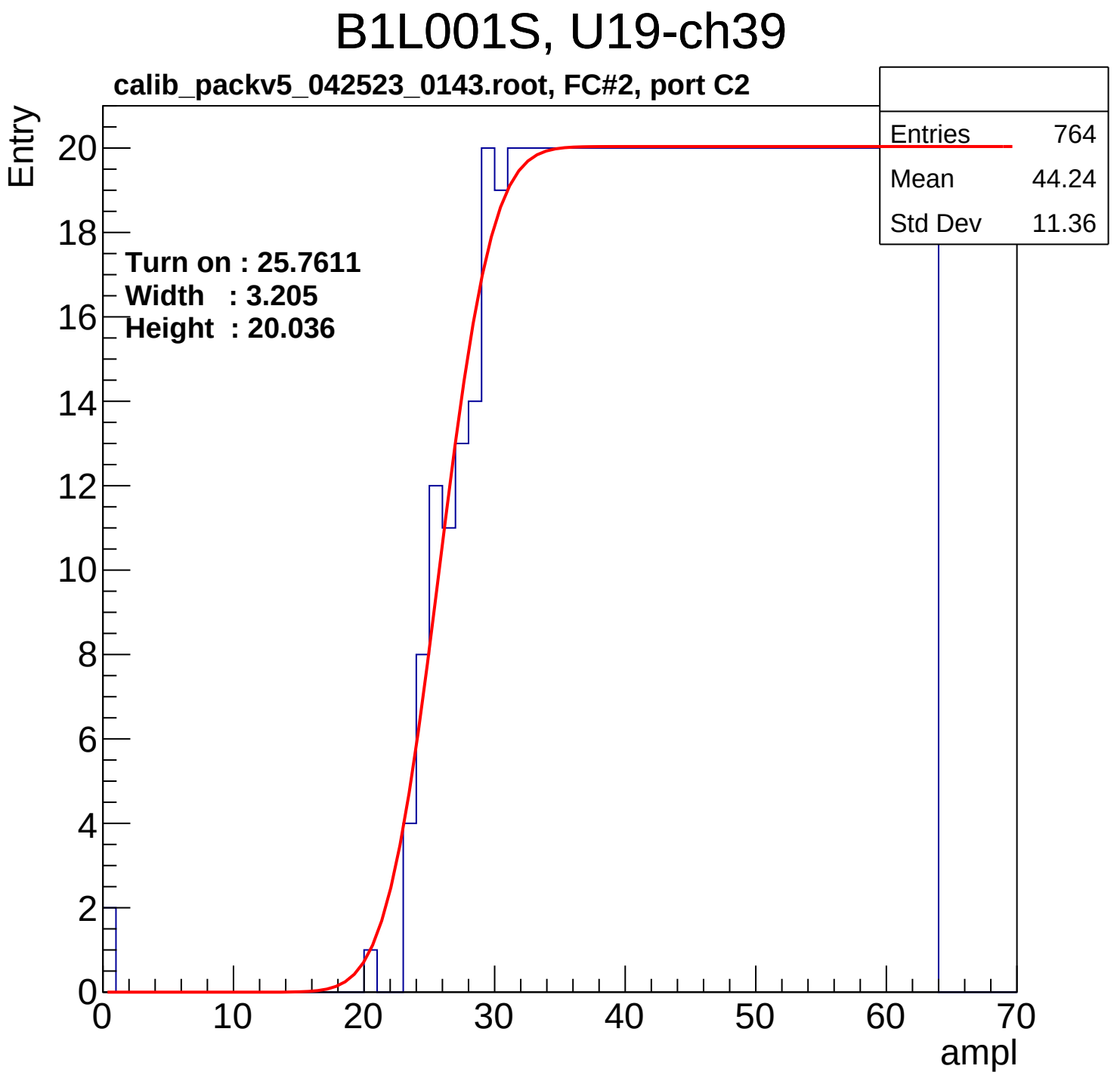
B1L001S, U19-ch39
calib_packv5_042523_0143.root, FC#2, port C2
Entries 764
Mean 44.24
Std Dev 11.36
Turn on : 25.7611
Width : 3.205
Height : 20.036
Entry
ampl
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6
8
10
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14
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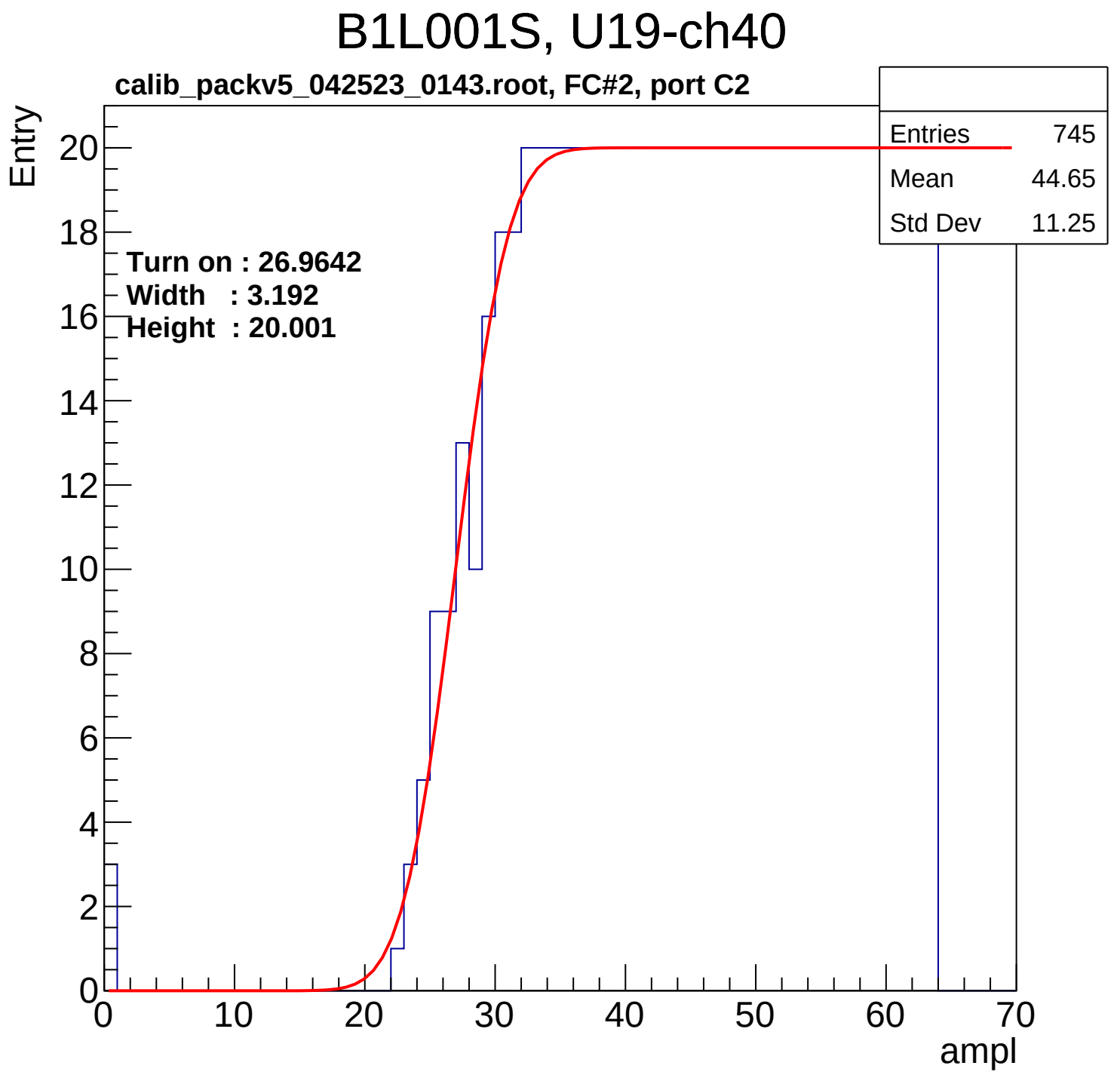
B1L001S, U19-ch40
calib_packv5_042523_0143.root, FC#2, port C2
Entries 745
Mean 44.65
Std Dev 11.25
Turn on : 26.9642
Width : 3.192
Height : 20.001
Entry
ampl
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6
8
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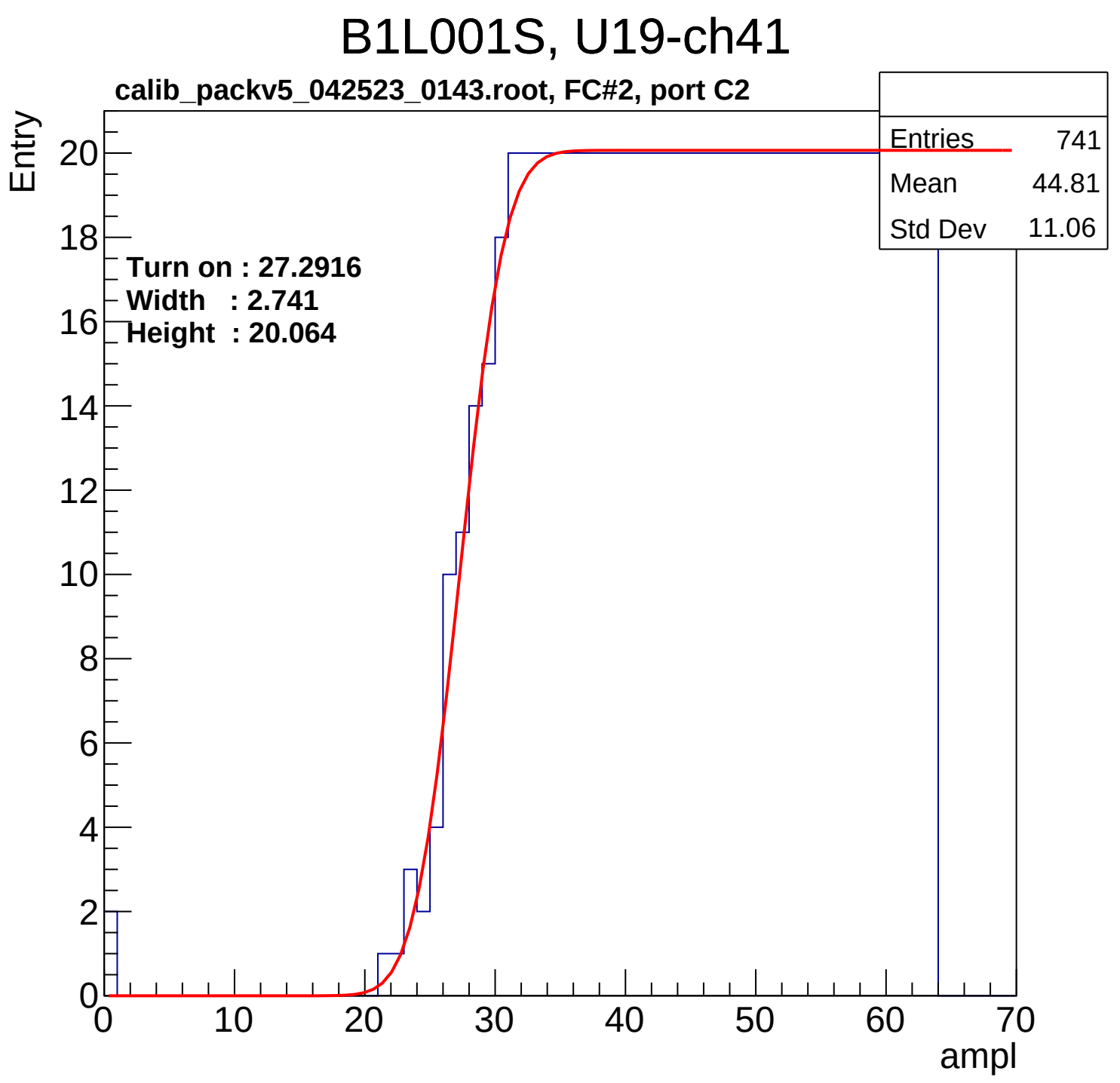
B1L001S, U19-ch41
calib_packv5_042523_0143.root, FC#2, port C2
Entries 741
Mean 44.81
Std Dev 11.06
Turn on : 27.2916
Width : 2.741
Height : 20.064
Entry
ampl
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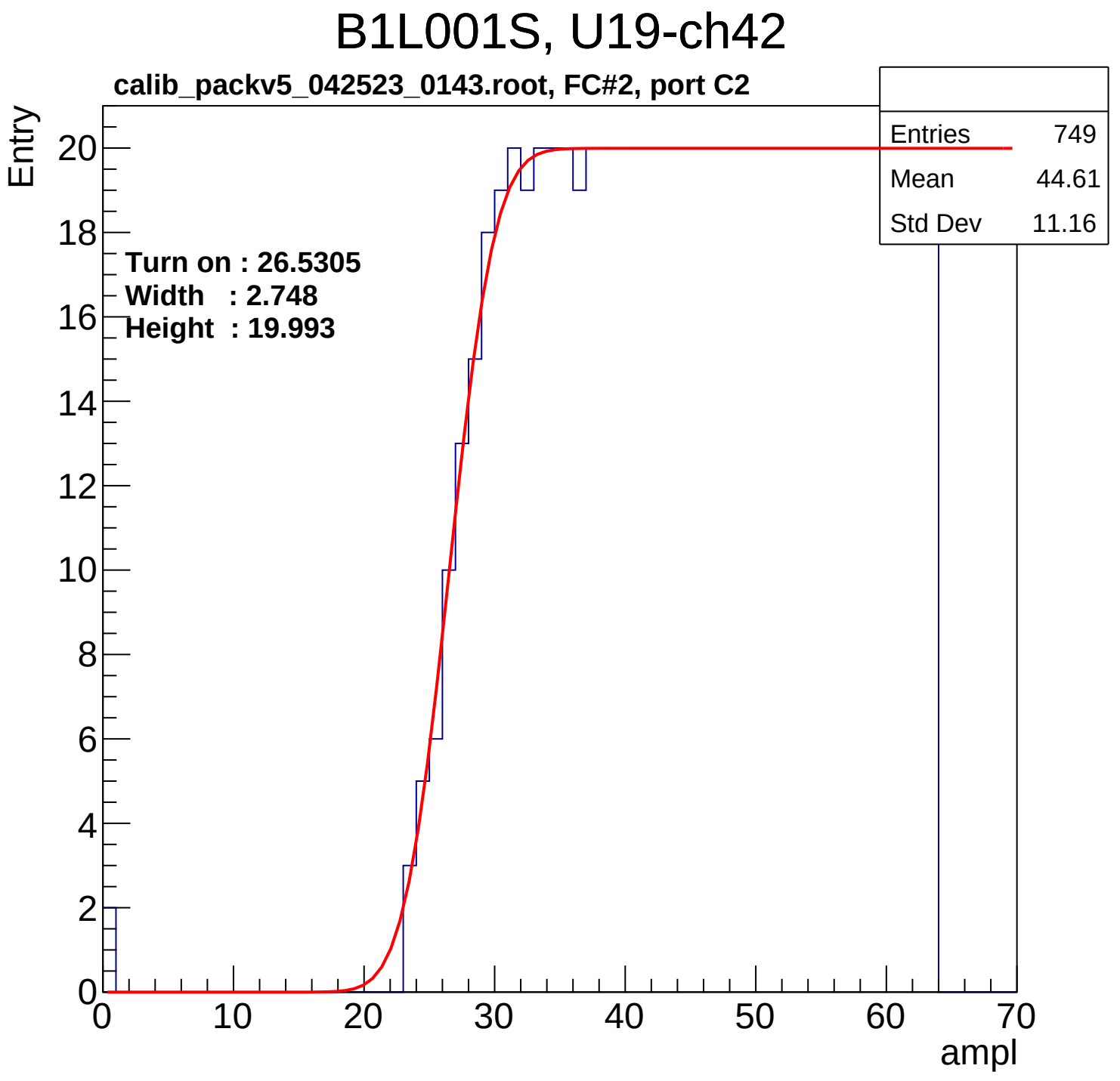
B1L001S, U19-ch42
calib_packv5_042523_0143.root, FC#2, port C2
Entries 749
Mean 44.61
Std Dev 11.16
Turn on : 26.5305
Width : 2.748
Height : 19.993
Entry
ampl
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6
8
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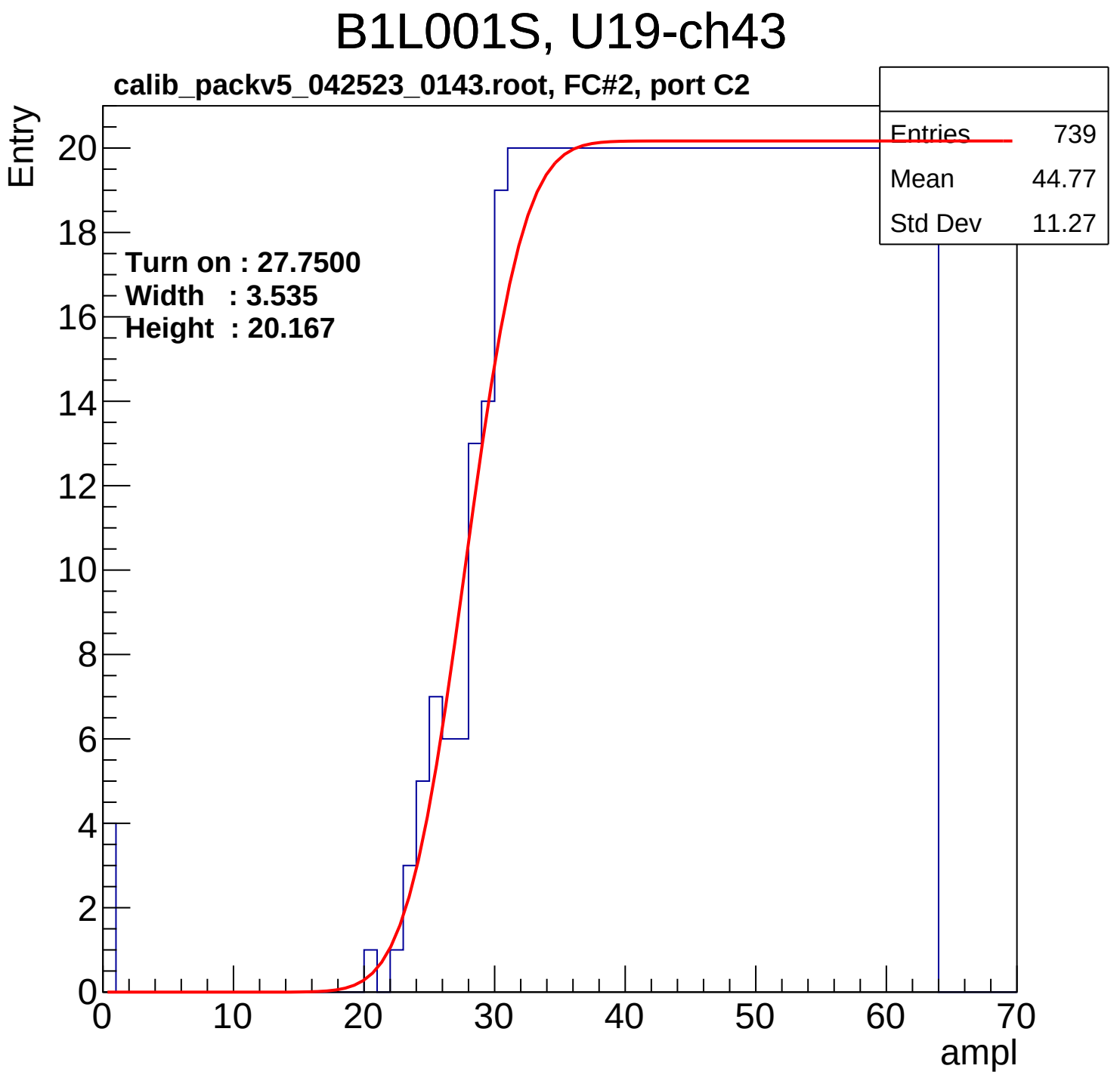
B1L001S, U19-ch43
calib_packv5_042523_0143.root, FC#2, port C2
Entries 739
Mean 44.77
Std Dev 11.27
Turn on : 27.7500
Width : 3.535
Height : 20.167
Entry
ampl
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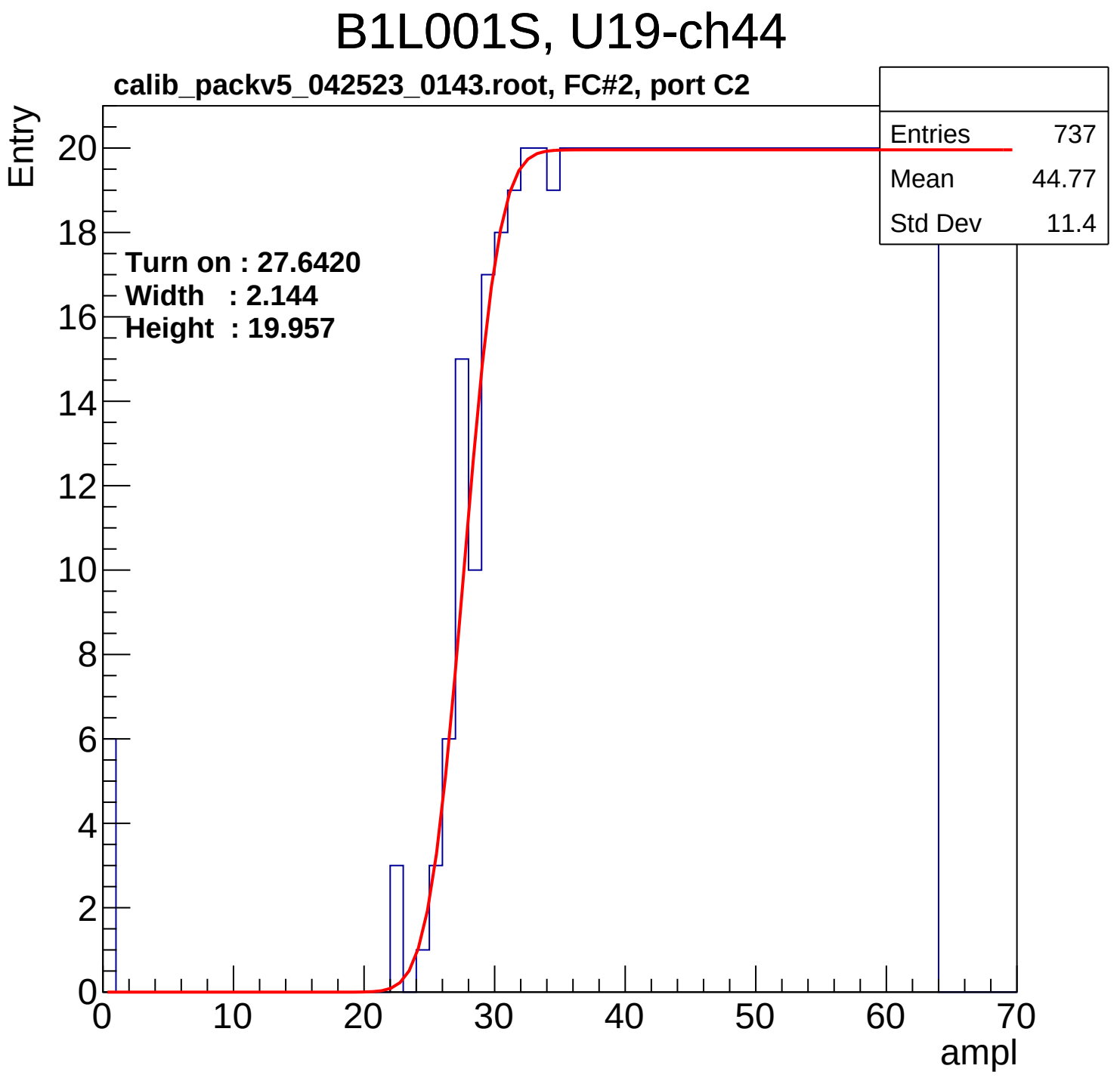
B1L001S, U19-ch44
calib_packv5_042523_0143.root, FC#2, port C2
Entries 737
Mean 44.77
Std Dev 11.4
Turn on : 27.6420
Width : 2.144
Height : 19.957
Entry
ampl
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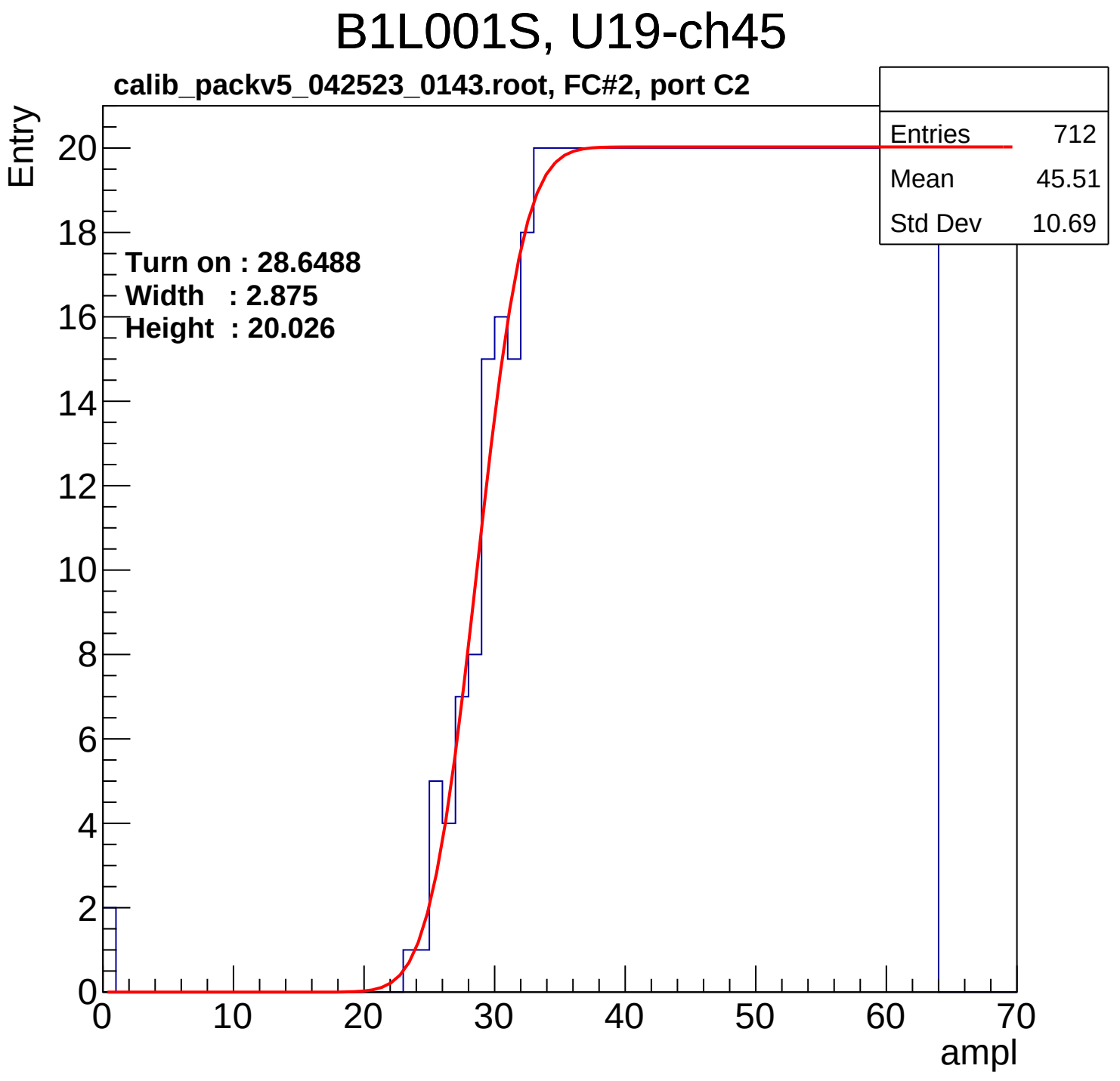
B1L001S, U19-ch45
calib_packv5_042523_0143.root, FC#2, port C2
Entries 712
Mean 45.51
Std Dev 10.69
Turn on : 28.6488
Width : 2.875
Height : 20.026
Entry
ampl
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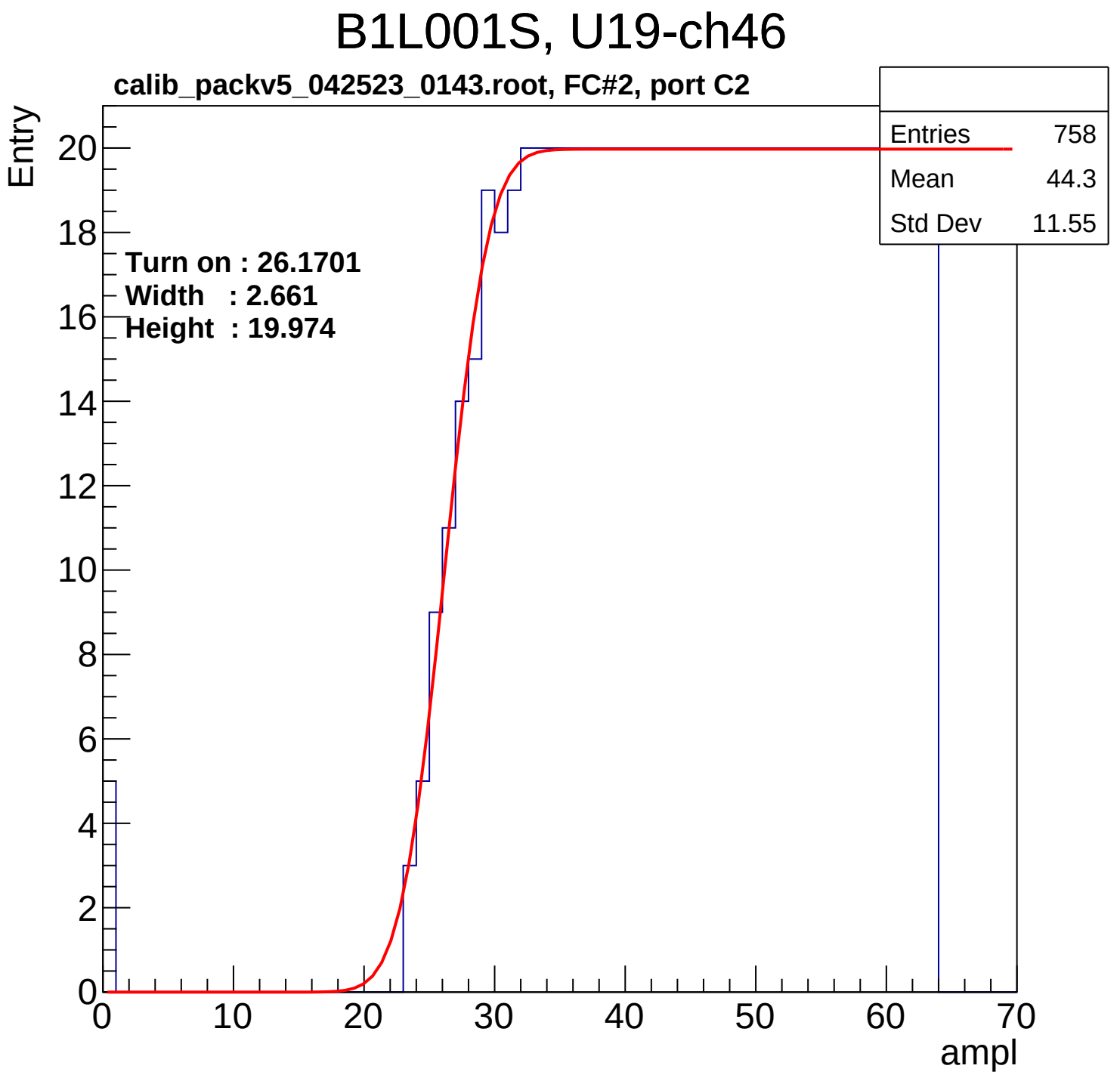
B1L001S, U19-ch46
calib_packv5_042523_0143.root, FC#2, port C2
Entries 758
Mean 44.3
Std Dev 11.55
Turn on : 26.1701
Width : 2.661
Height : 19.974
Entry
ampl
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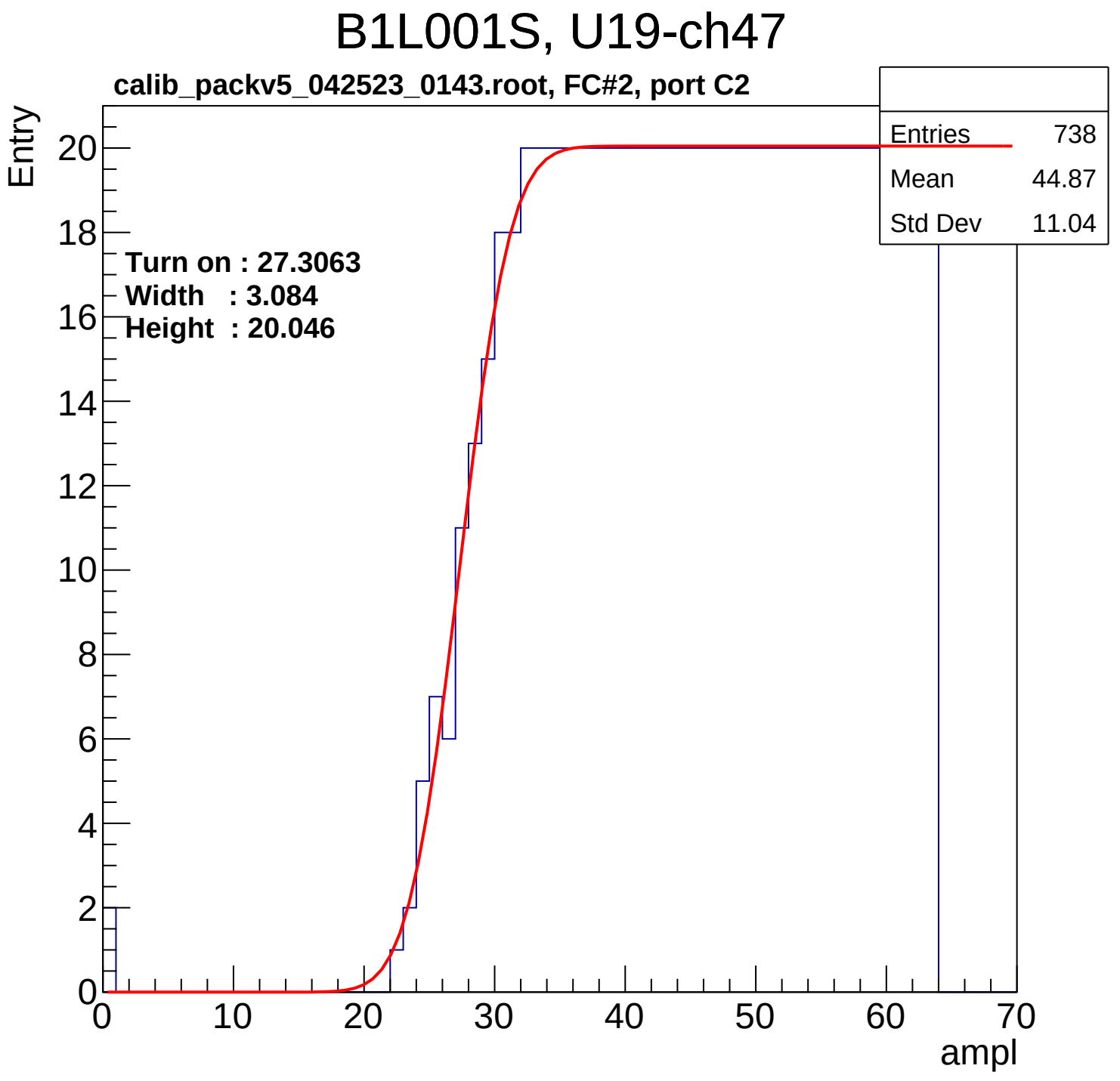
B1L001S, U19-ch47
calib_packv5_042523_0143.root, FC#2, port C2
Entries 738
Mean 44.87
Std Dev 11.04
Turn on : 27.3063
Width : 3.084
Height : 20.046
Entry
ampl
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10
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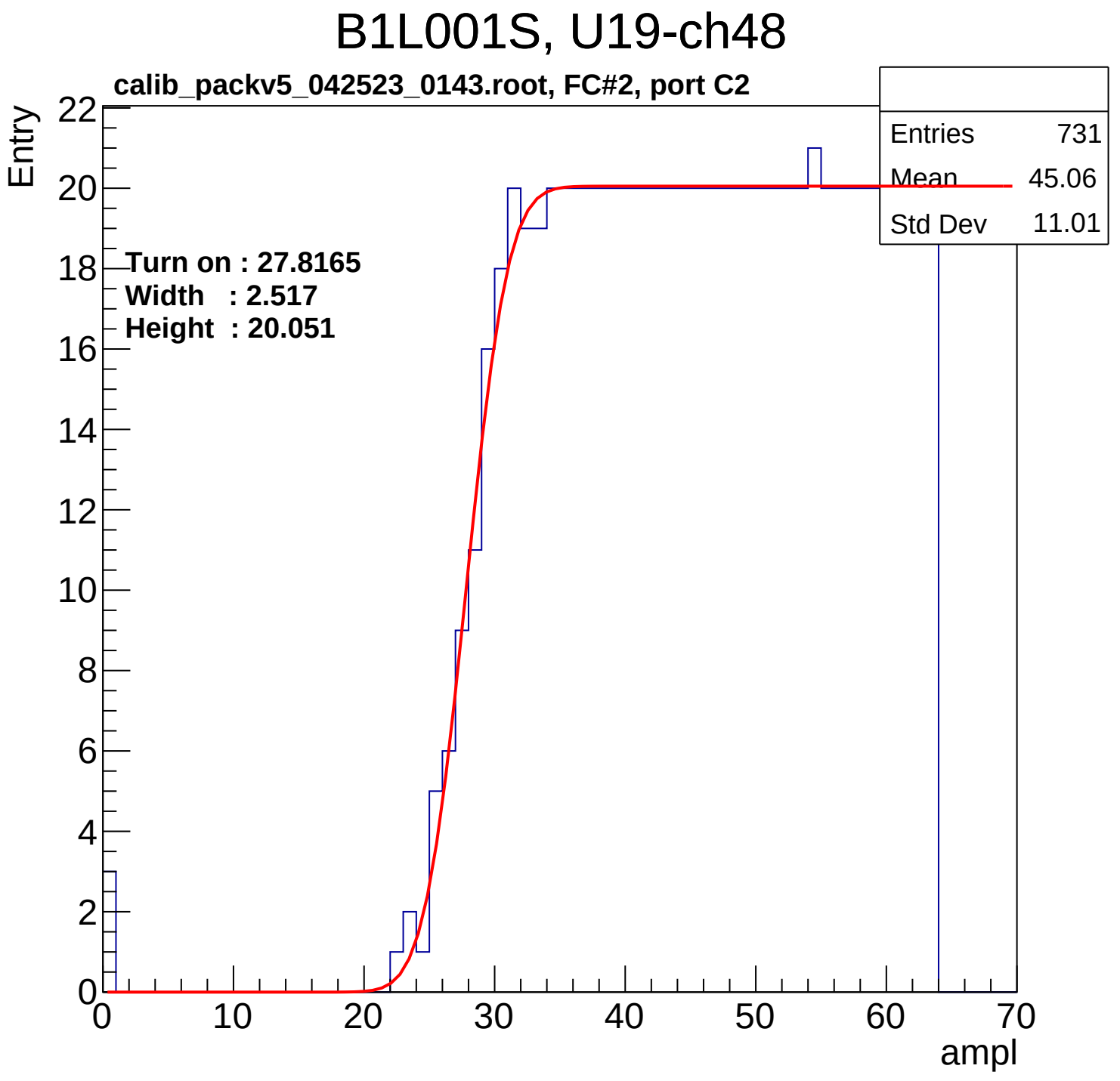
B1L001S, U19-ch48
calib_packv5_042523_0143.root, FC#2, port C2
Entries 731
Mean 45.06
Std Dev 11.01
Turn on : 27.8165
Width : 2.517
Height : 20.051
Entry
ampl
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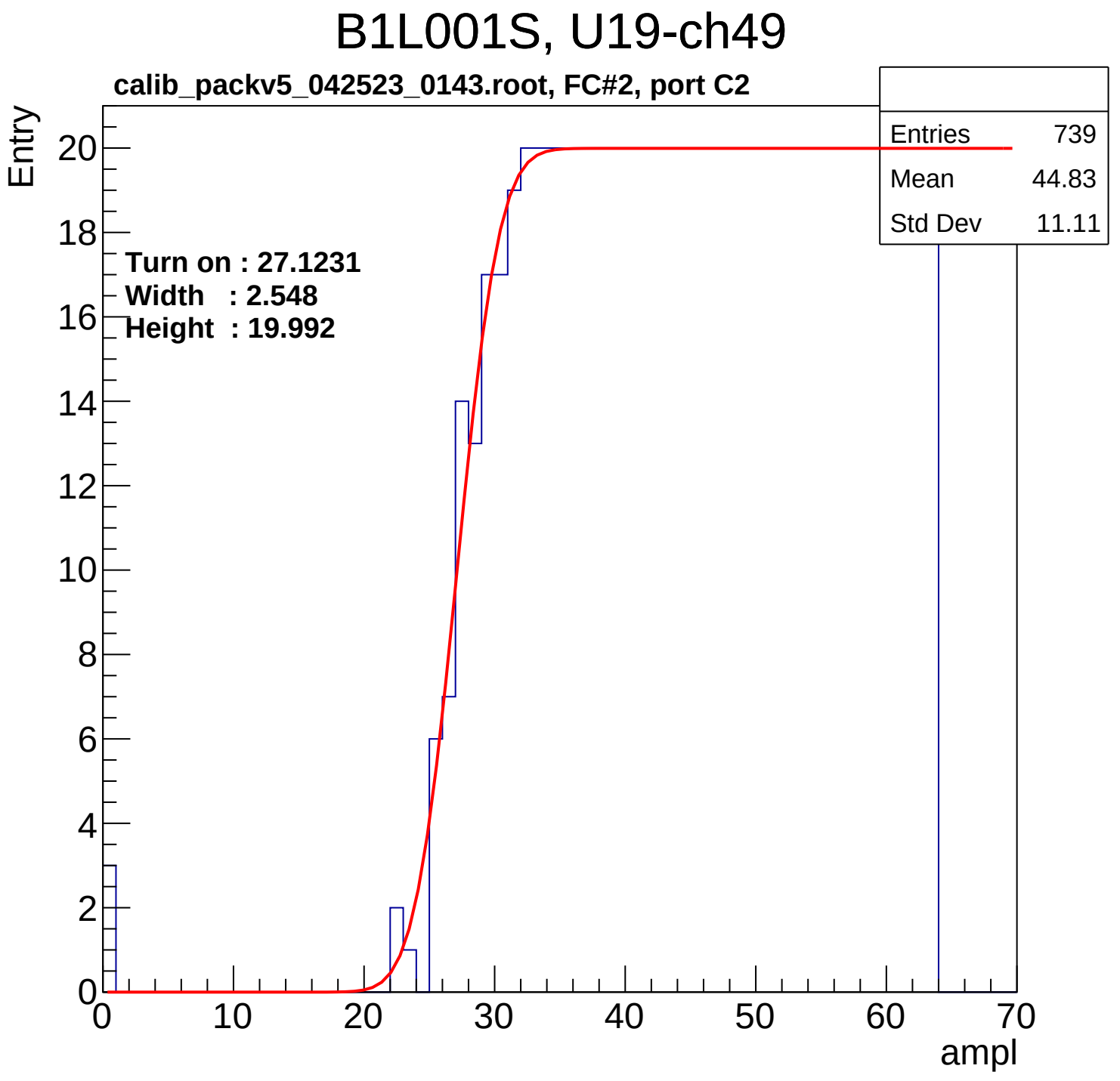
B1L001S, U19-ch49
calib_packv5_042523_0143.root, FC#2, port C2
Entries 739
Mean 44.83
Std Dev 11.11
Turn on : 27.1231
Width : 2.548
Height : 19.992
Entry
ampl
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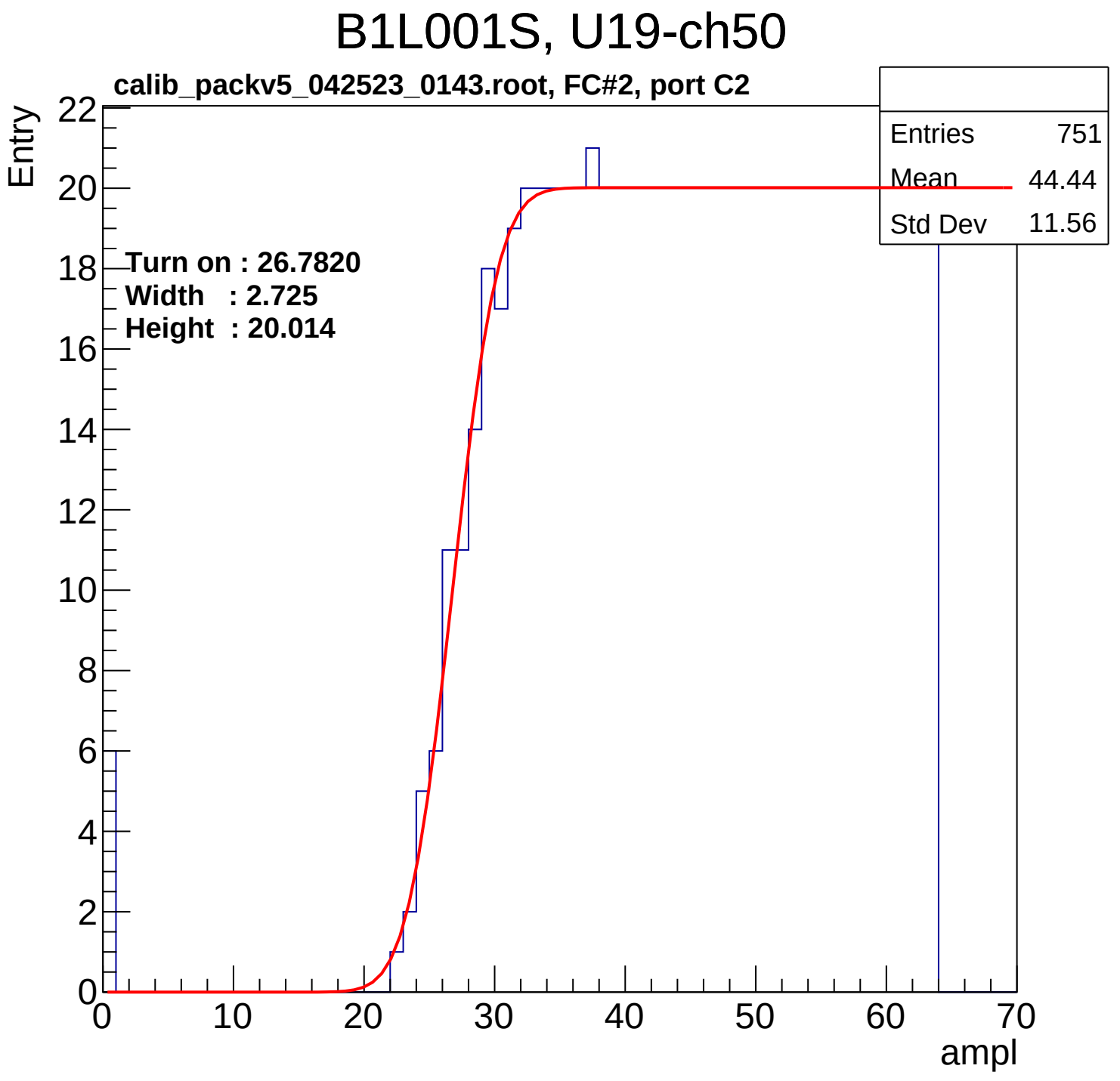
B1L001S, U19-ch50
calib_packv5_042523_0143.root, FC#2, port C2
Entries 751
Mean 44.44
Std Dev 11.56
Turn on : 26.7820
Width : 2.725
Height : 20.014
Entry
ampl
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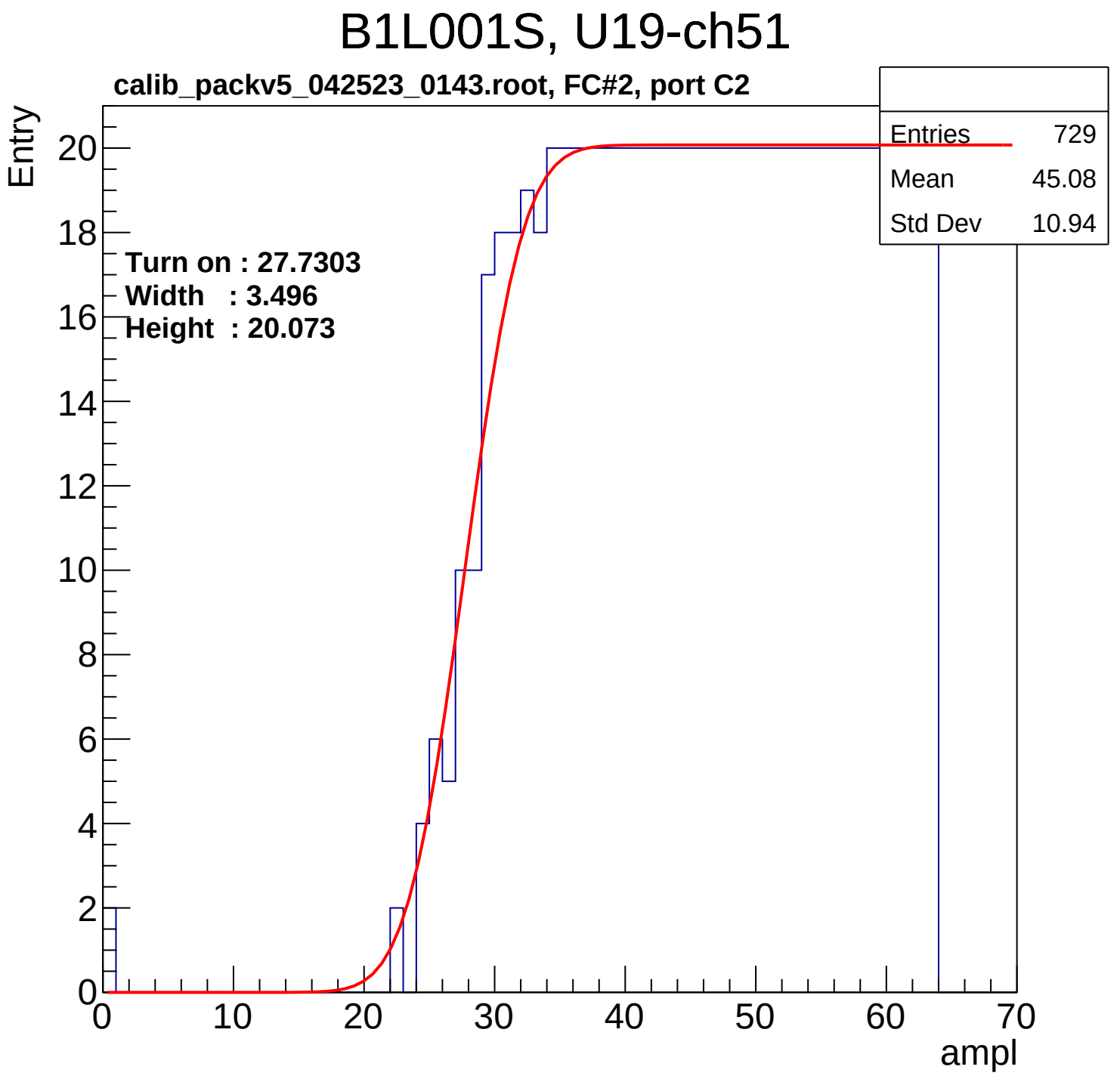
B1L001S, U19-ch51
calib_packv5_042523_0143.root, FC#2, port C2
Entries 729
Mean 45.08
Std Dev 10.94
Turn on : 27.7303
Width : 3.496
Height : 20.073
Entry
ampl
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6
8
10
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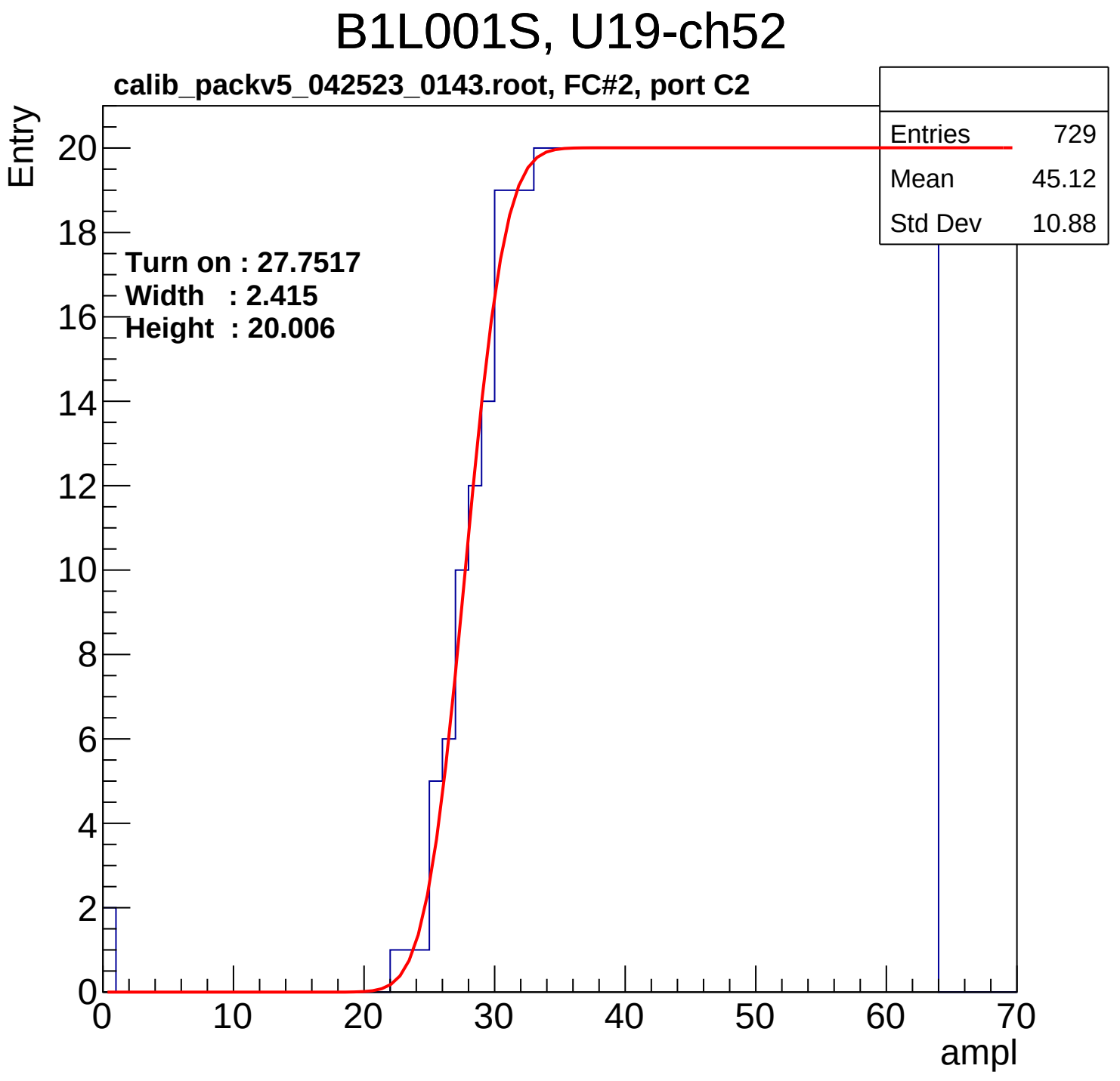
B1L001S, U19-ch52
calib_packv5_042523_0143.root, FC#2, port C2
Entries 729
Mean 45.12
Std Dev 10.88
Turn on : 27.7517
Width : 2.415
Height : 20.006
Entry
ampl
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6
8
10
12
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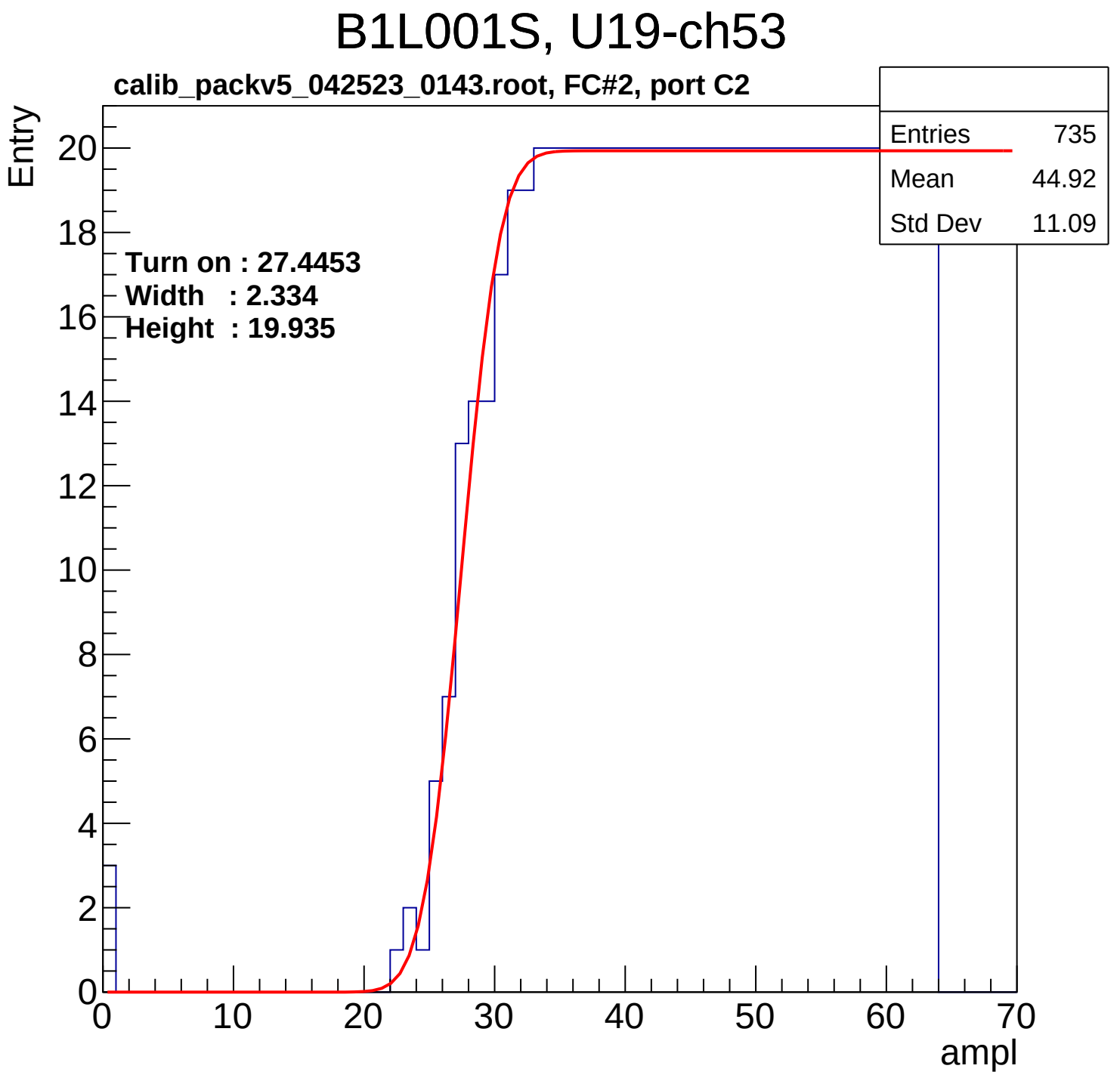
B1L001S, U19-ch53
calib_packv5_042523_0143.root, FC#2, port C2
Entries 735
Mean 44.92
Std Dev 11.09
Turn on : 27.4453
Width : 2.334
Height : 19.935
Entry
ampl
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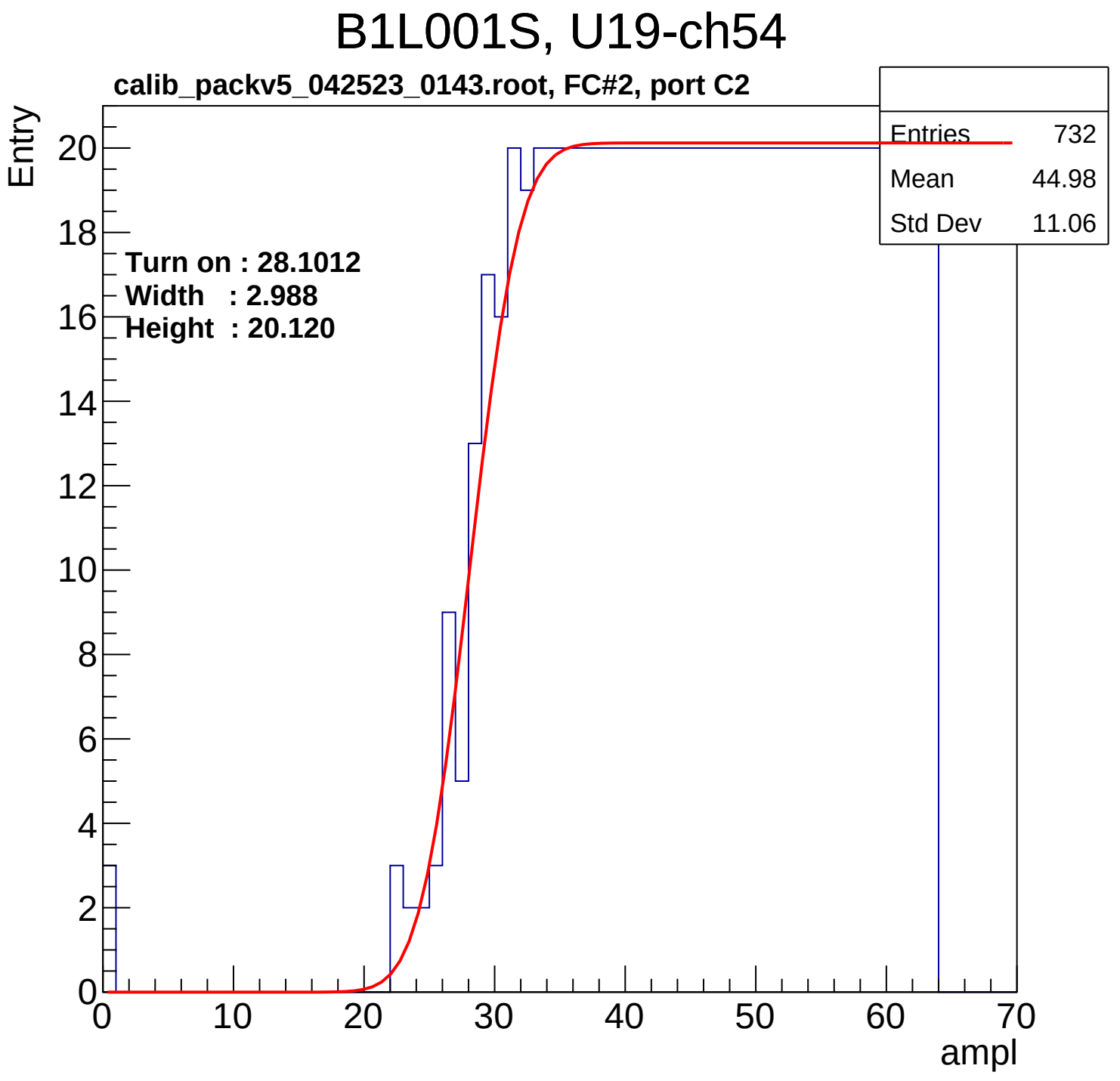
B1L001S, U19-ch54
calib_packv5_042523_0143.root, FC#2, port C2
Entries 732
Mean 44.98
Std Dev 11.06
Turn on : 28.1012
Width : 2.988
Height : 20.120
Entry
ampl
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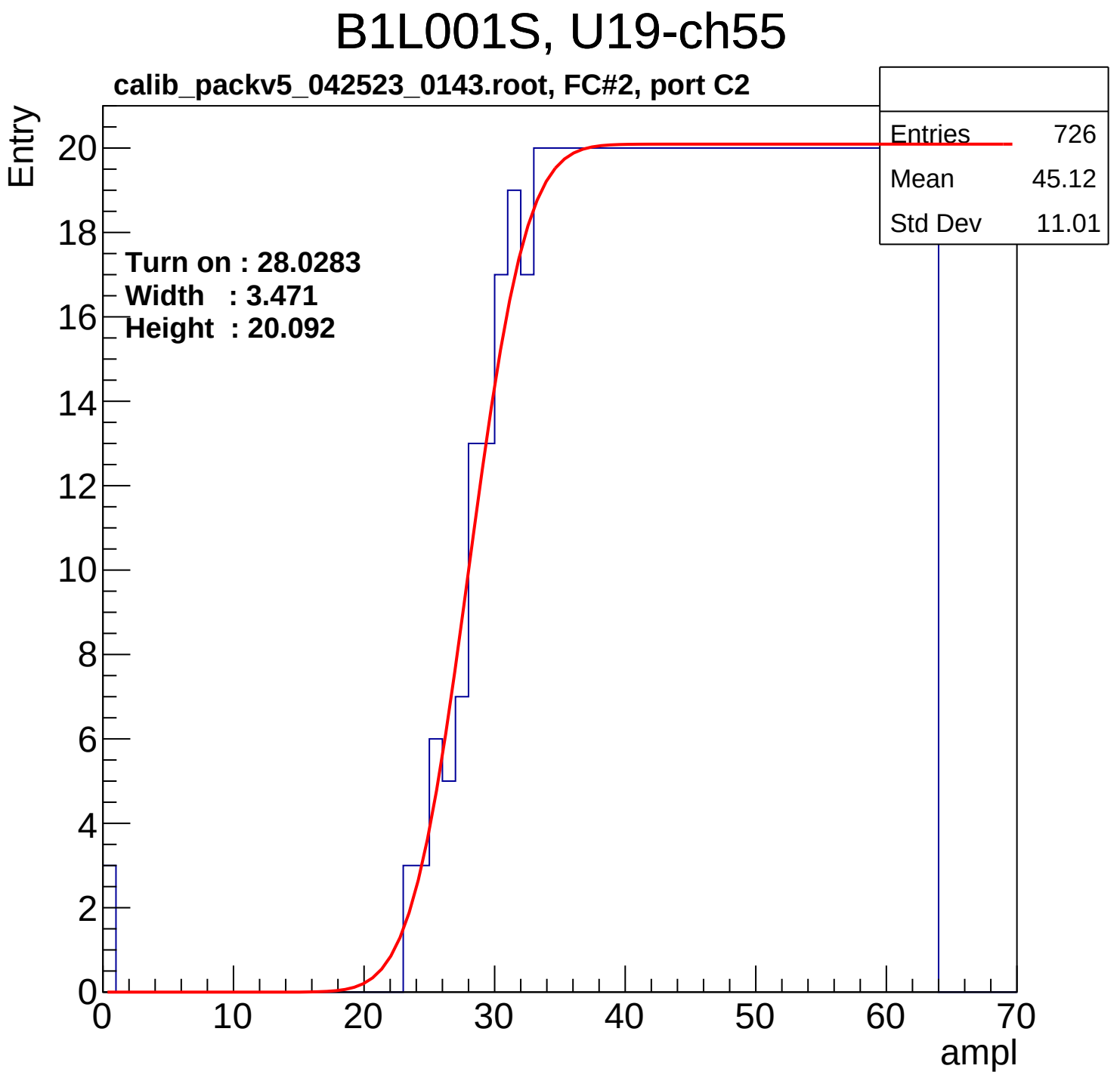
B1L001S, U19-ch55
calib_packv5_042523_0143.root, FC#2, port C2
Entries 726
Mean 45.12
Std Dev 11.01
Turn on : 28.0283
Width : 3.471
Height : 20.092
Entry
ampl
0
2
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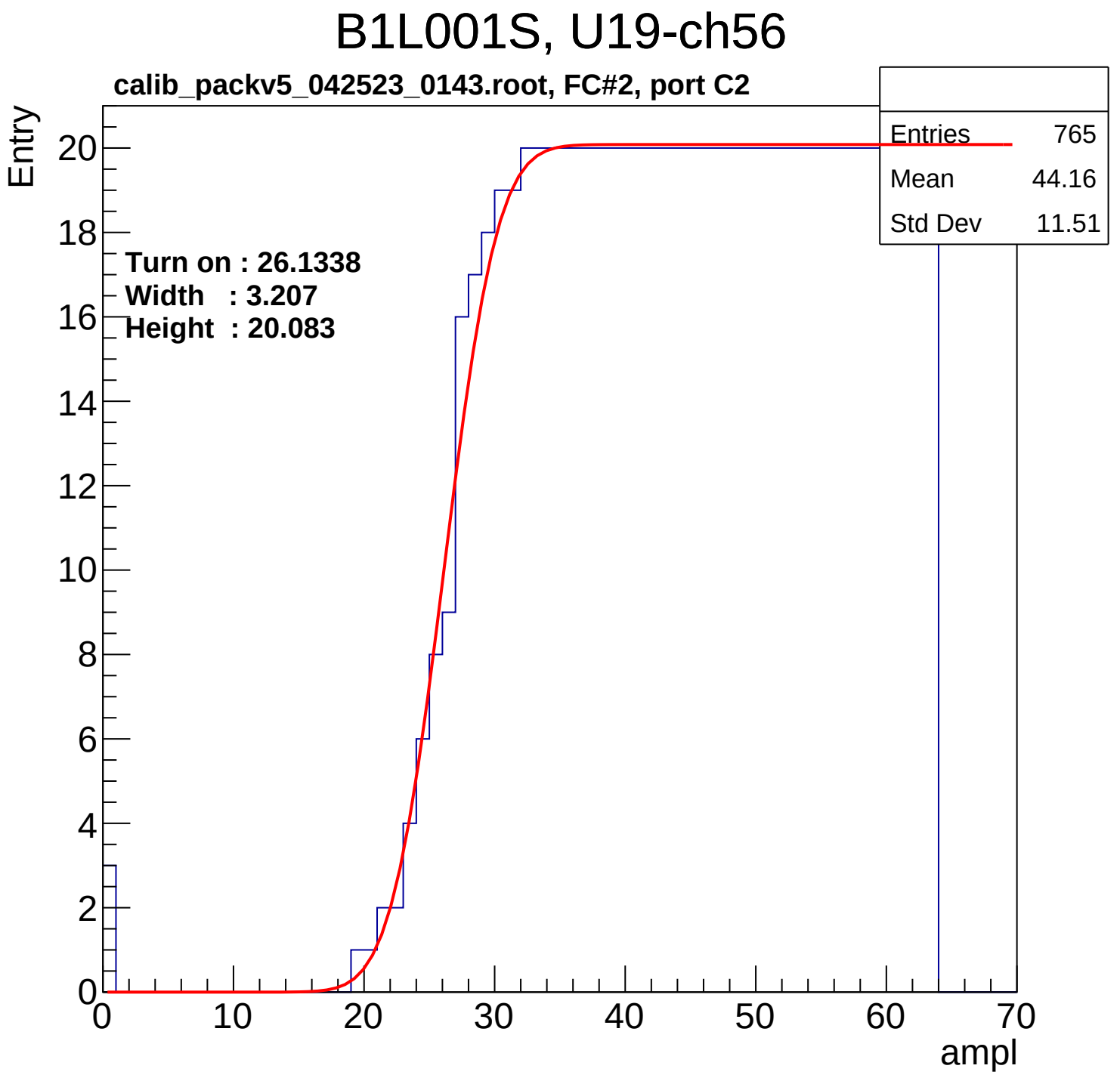
B1L001S, U19-ch56
calib_packv5_042523_0143.root, FC#2, port C2
Entries 765
Mean 44.16
Std Dev 11.51
Turn on : 26.1338
Width : 3.207
Height : 20.083
Entry
ampl
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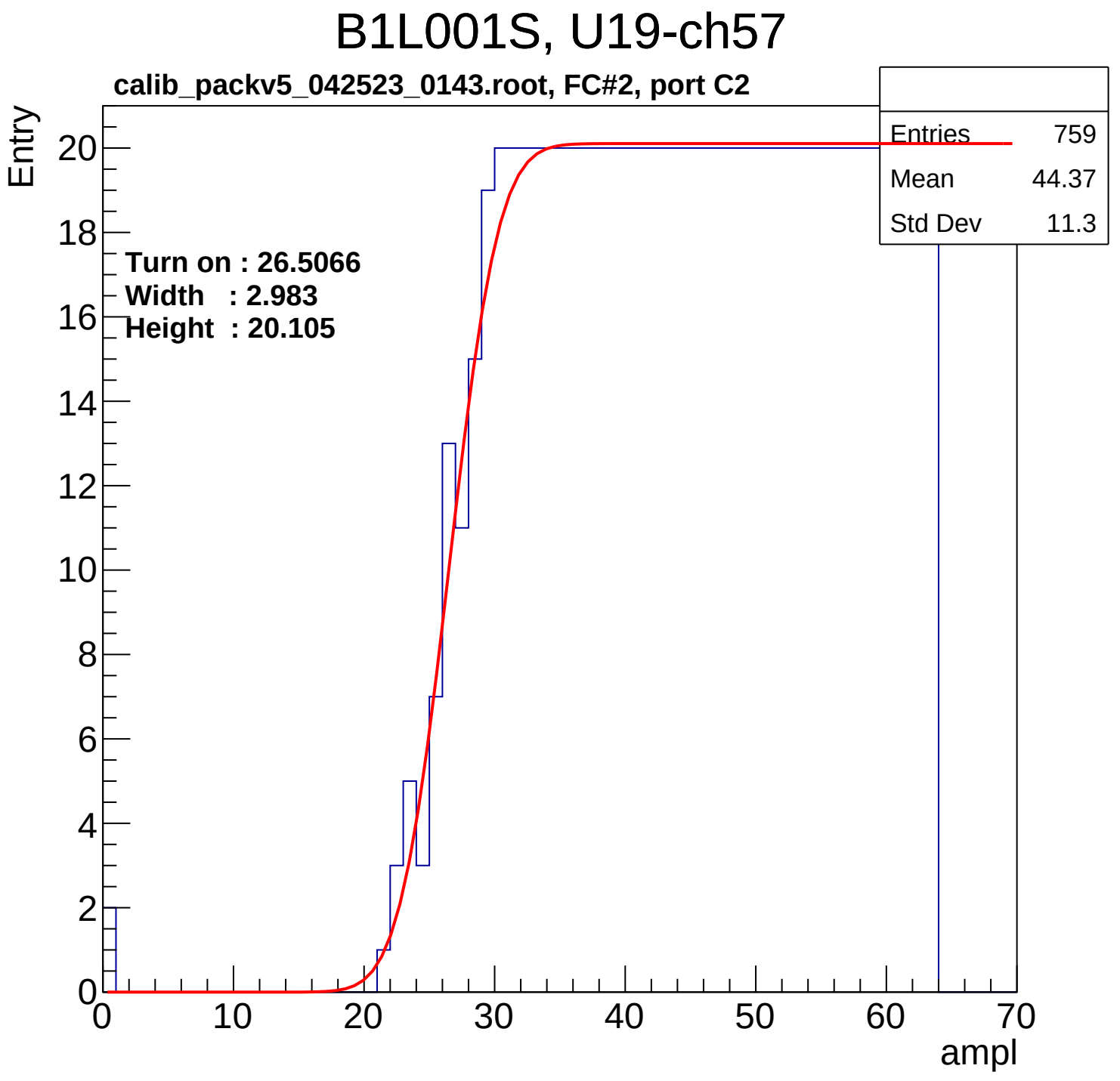
B1L001S, U19-ch57
calib_packv5_042523_0143.root, FC#2, port C2
Entries 759
Mean 44.37
Std Dev 11.3
Turn on : 26.5066
Width : 2.983
Height : 20.105
Entry
ampl
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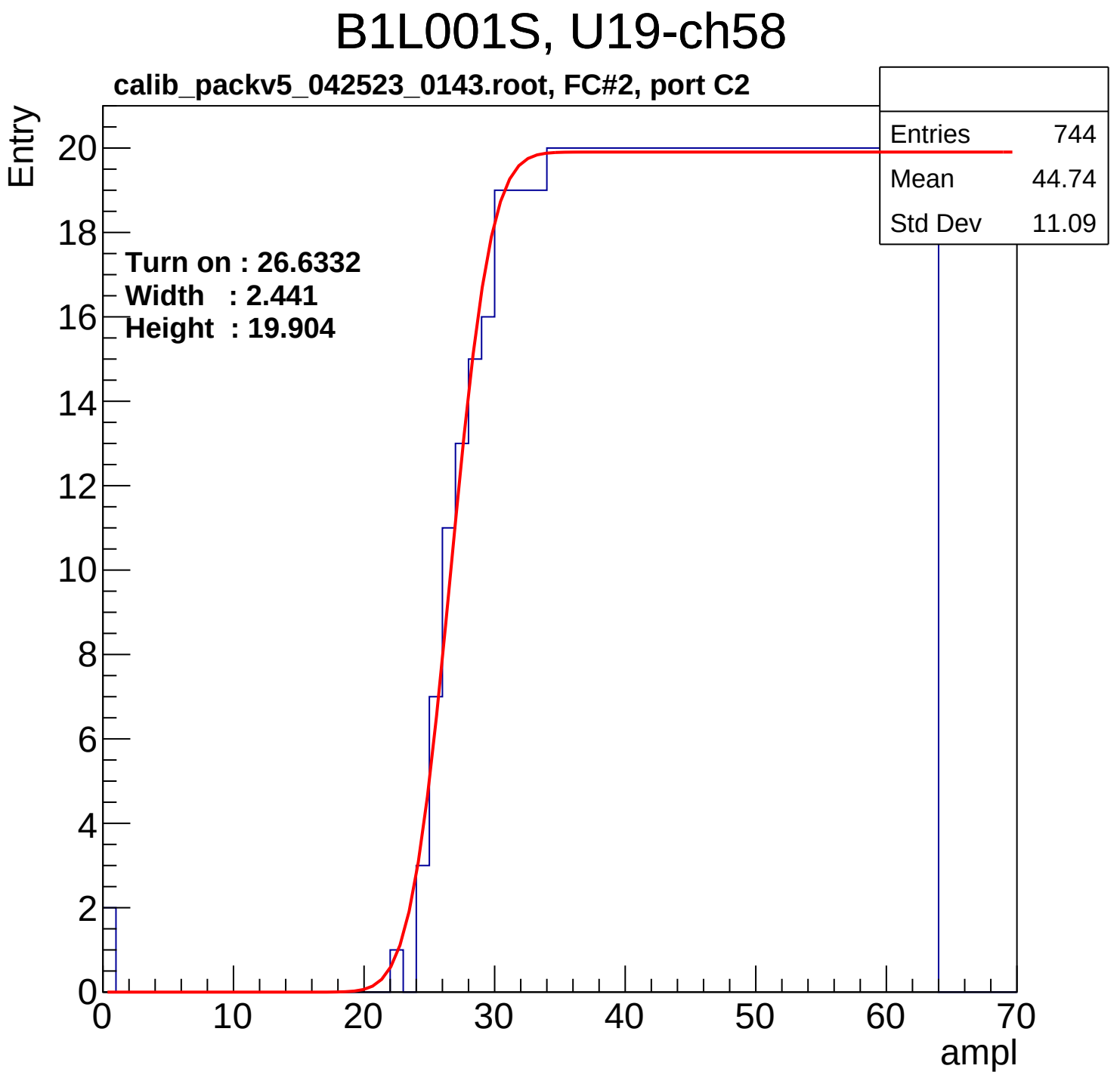
B1L001S, U19-ch58
calib_packv5_042523_0143.root, FC#2, port C2
Entries 744
Mean 44.74
Std Dev 11.09
Turn on : 26.6332
Width : 2.441
Height : 19.904
Entry
ampl
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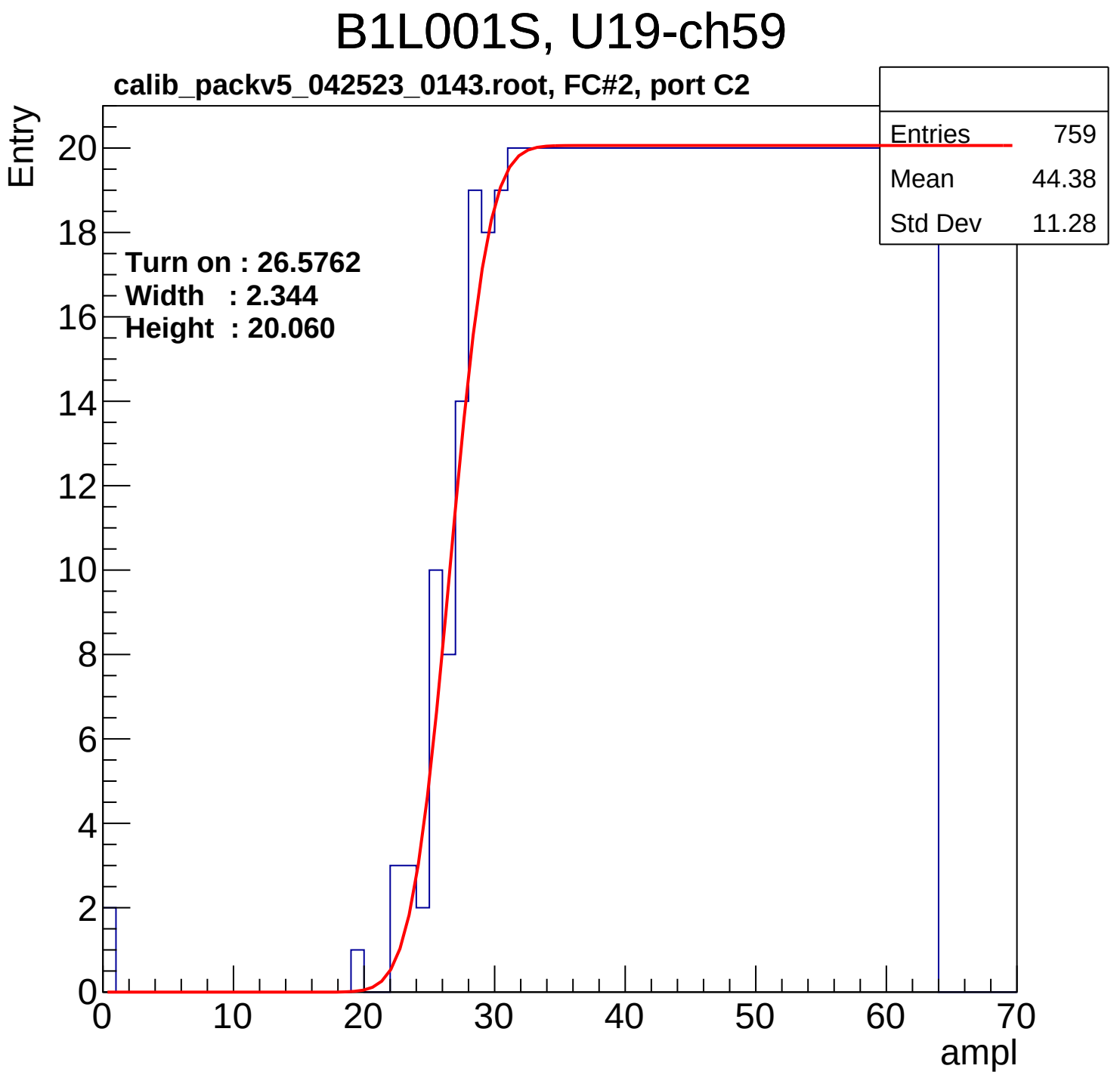
B1L001S, U19-ch59
calib_packv5_042523_0143.root, FC#2, port C2
Entries 759
Mean 44.38
Std Dev 11.28
Turn on : 26.5762
Width : 2.344
Height : 20.060
Entry
ampl
0
2
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6
8
10
12
14
16
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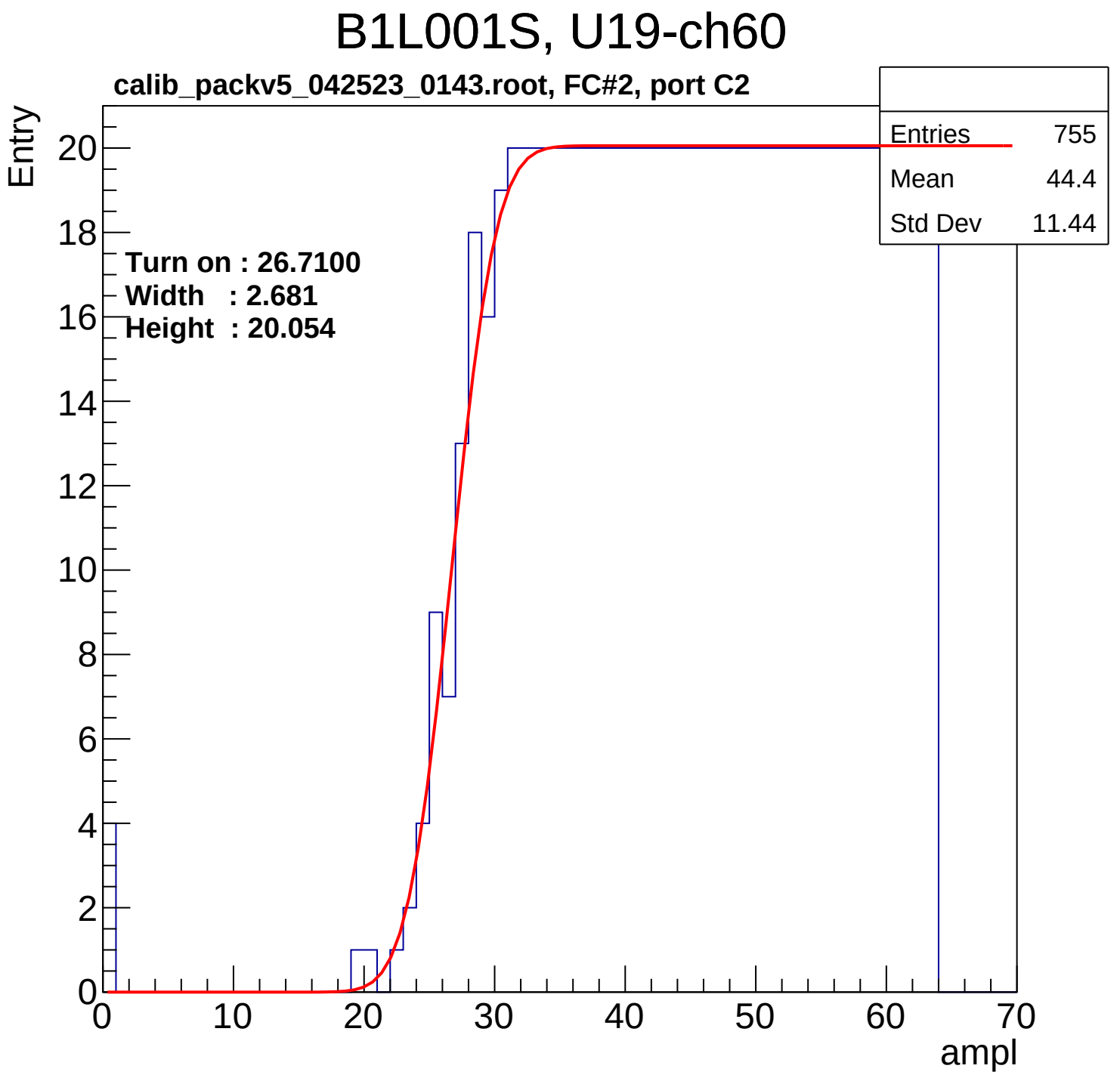
B1L001S, U19-ch60
calib_packv5_042523_0143.root, FC#2, port C2
Entries 755
Mean 44.4
Std Dev 11.44
Turn on : 26.7100
Width : 2.681
Height : 20.054
Entry
ampl
0
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6
8
10
12
14
16
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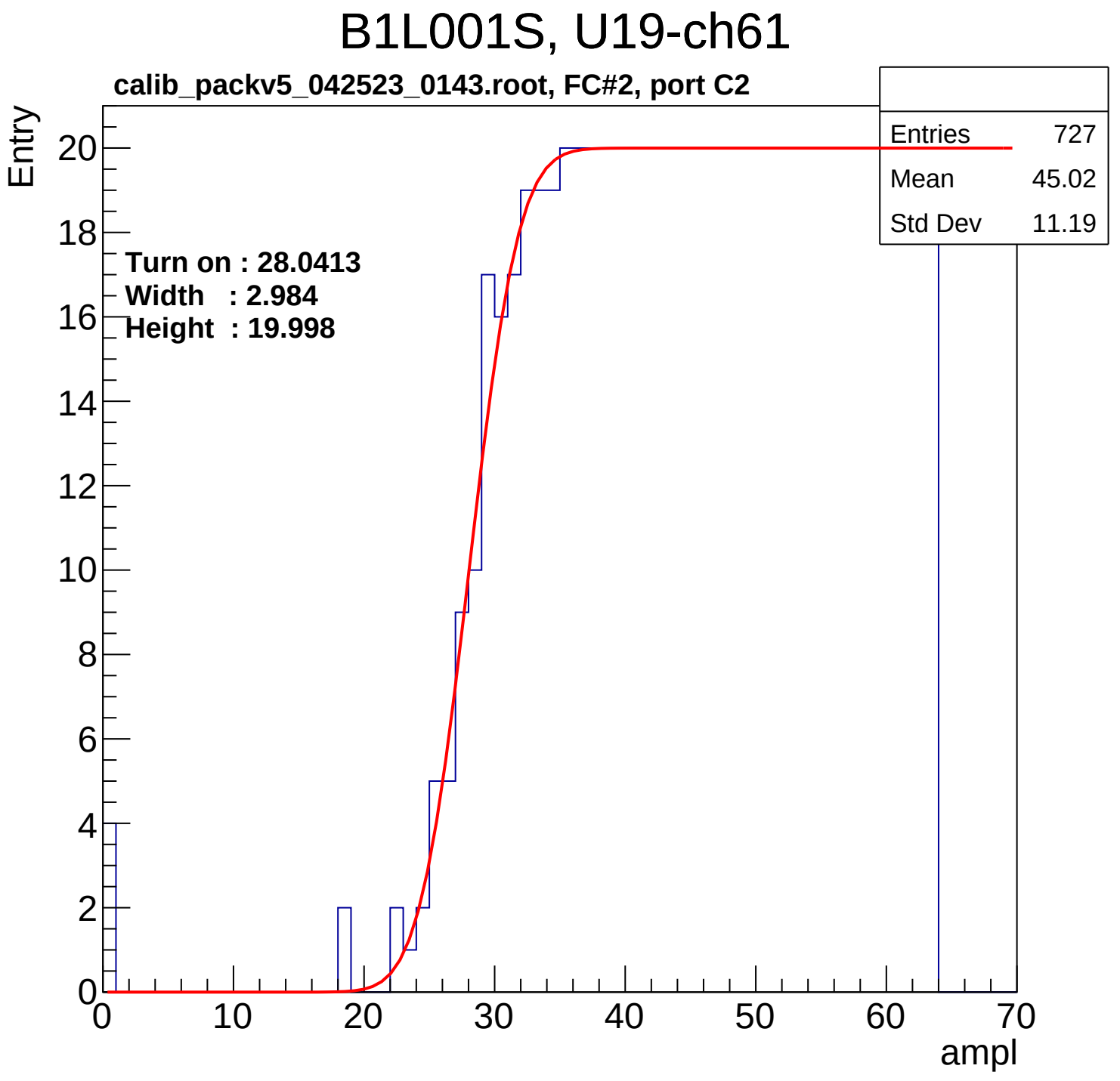
B1L001S, U19-ch61
calib_packv5_042523_0143.root, FC#2, port C2
Entries 727
Mean 45.02
Std Dev 11.19
Turn on : 28.0413
Width : 2.984
Height : 19.998
Entry
ampl
0
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6
8
10
12
14
16
18
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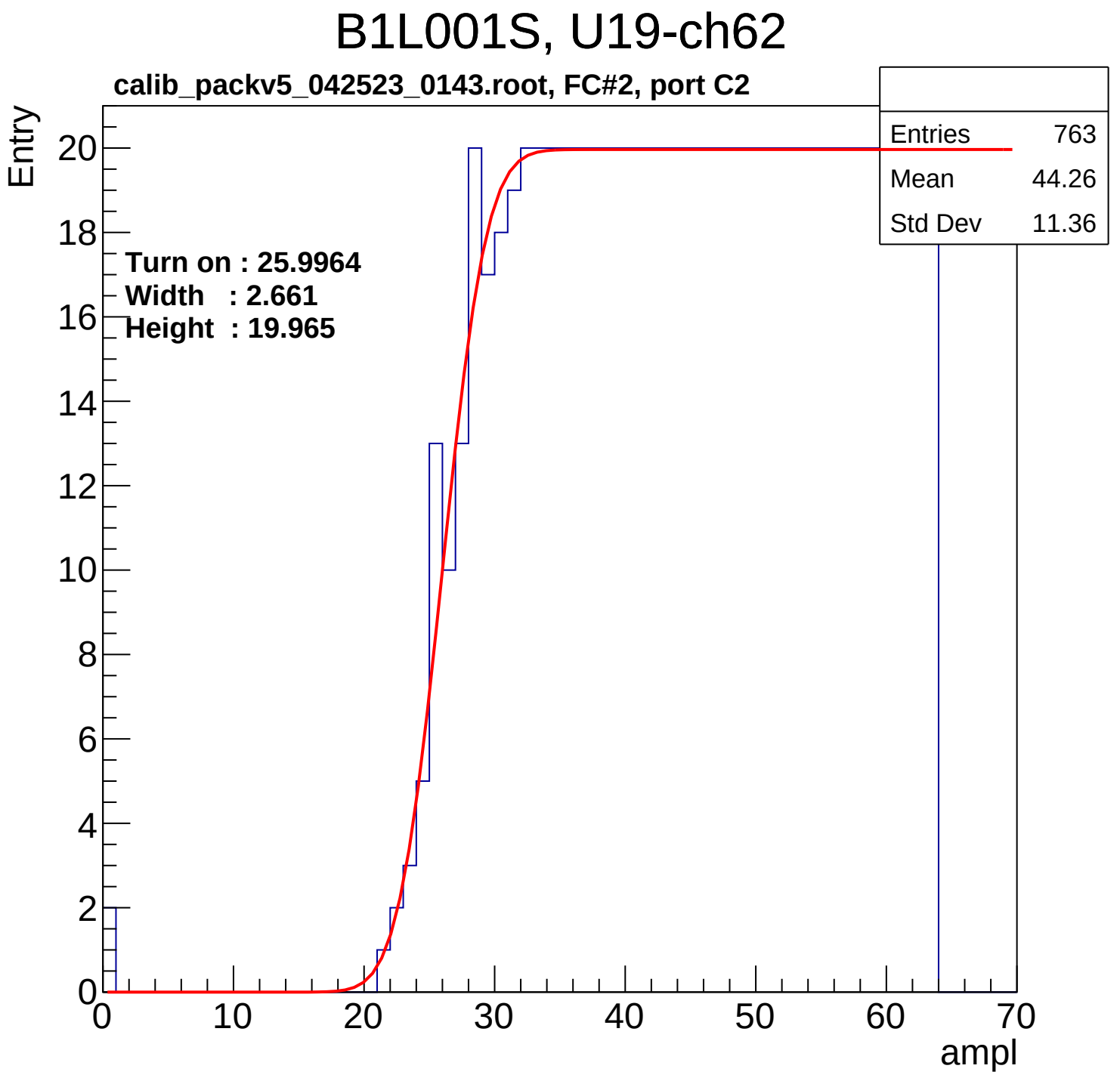
B1L001S, U19-ch62
calib_packv5_042523_0143.root, FC#2, port C2
Entries 763
Mean 44.26
Std Dev 11.36
Turn on : 25.9964
Width : 2.661
Height : 19.965
Entry
ampl
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6
8
10
12
14
16
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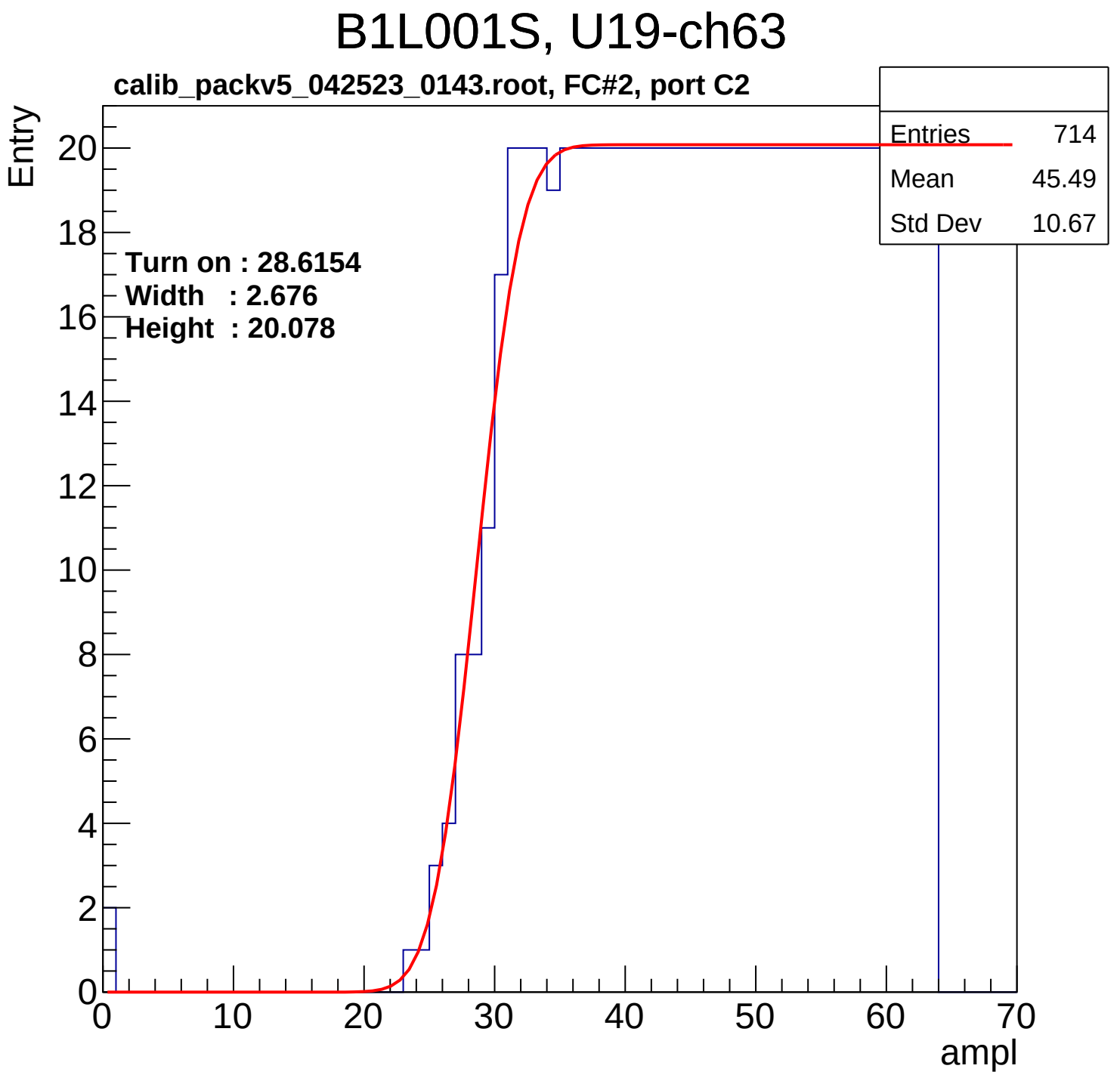
B1L001S, U19-ch63
calib_packv5_042523_0143.root, FC#2, port C2
Entries 714
Mean 45.49
Std Dev 10.67
Turn on : 28.6154
Width : 2.676
Height : 20.078
Entry
ampl
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6
8
10
12
14
16
18
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0
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60
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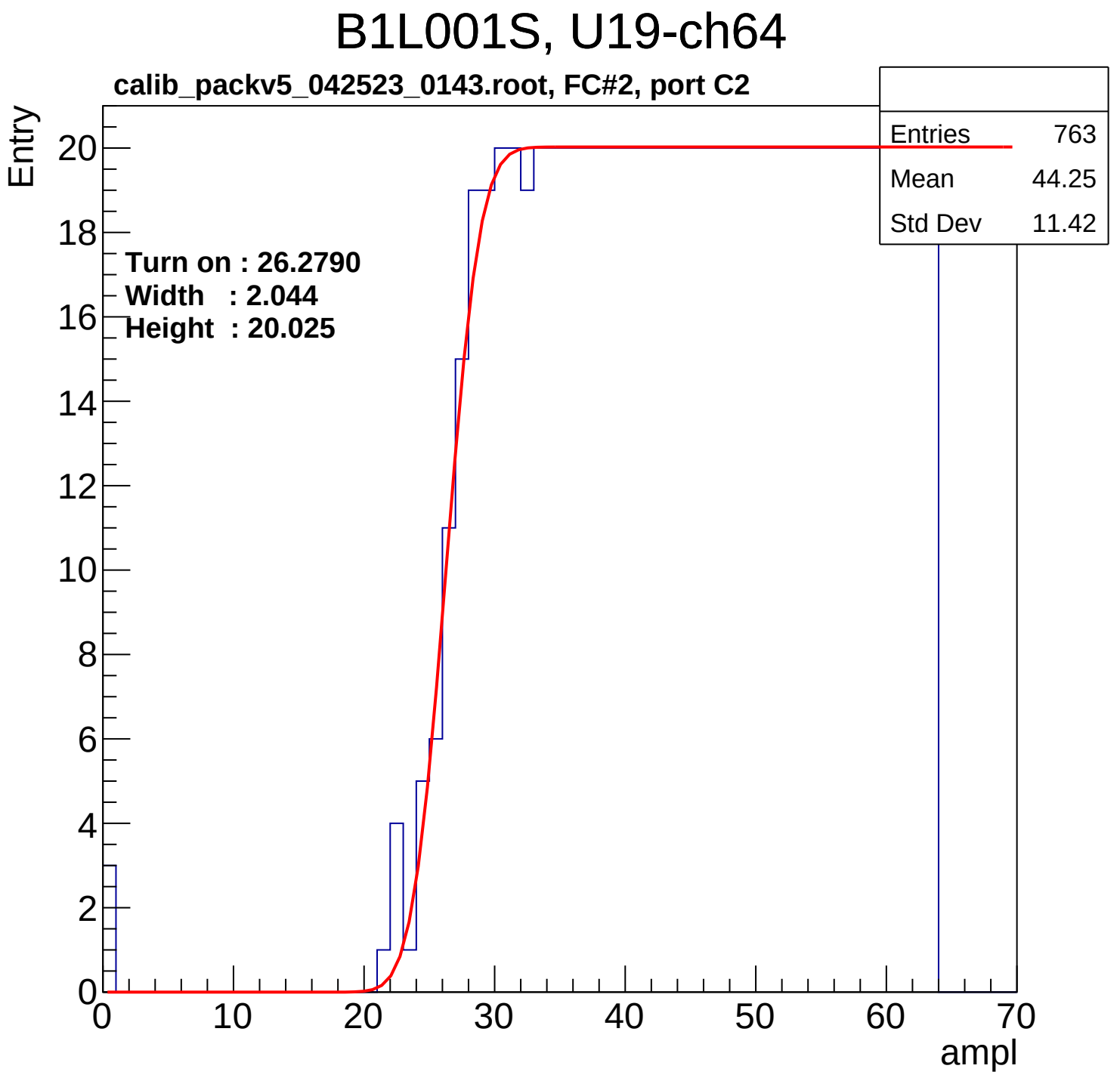
B1L001S, U19-ch64
calib_packv5_042523_0143.root, FC#2, port C2
Entries 763
Mean 44.25
Std Dev 11.42
Turn on : 26.2790
Width : 2.044
Height : 20.025
Entry
ampl
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6
8
10
12
14
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18
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20
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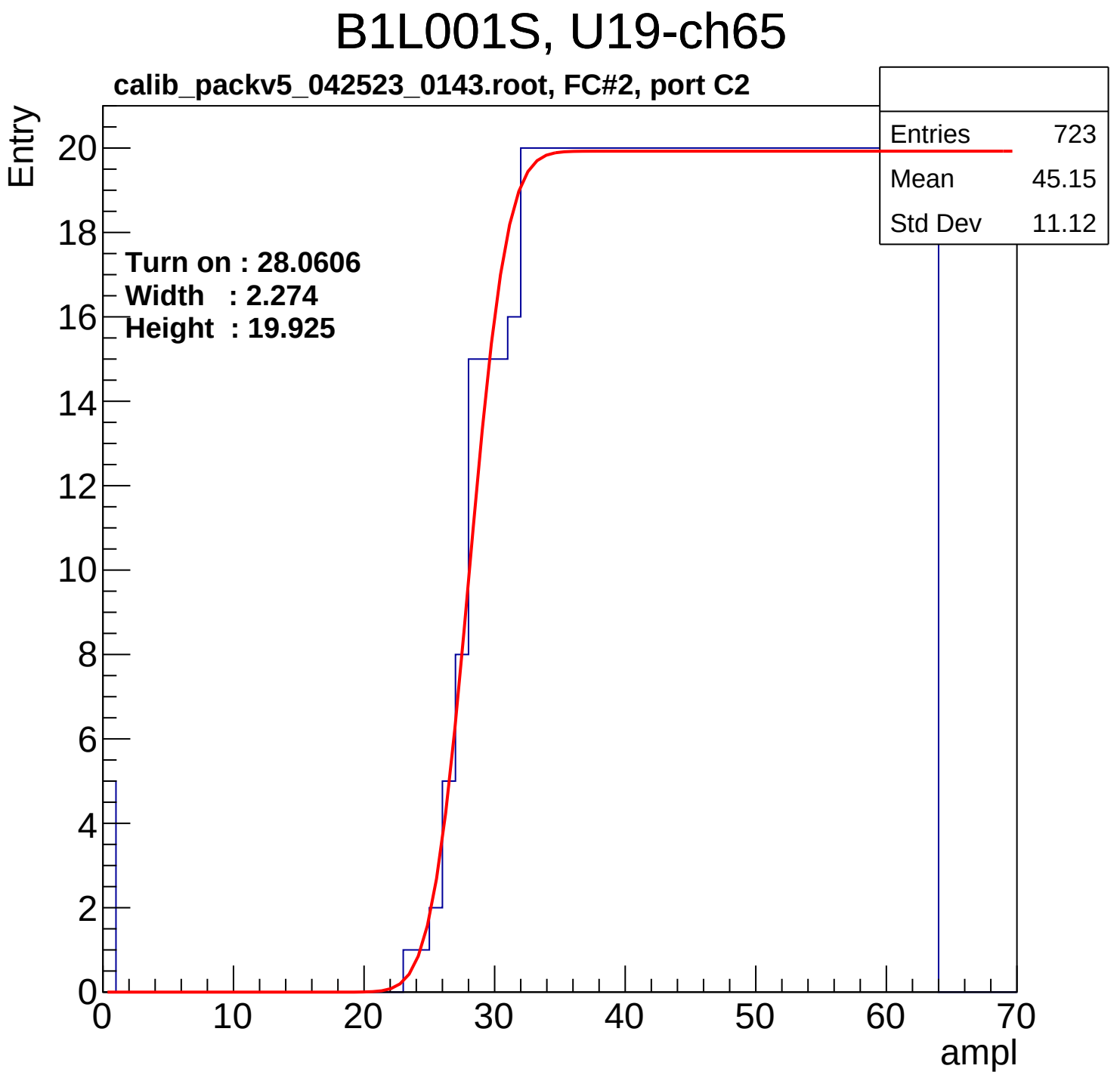
B1L001S, U19-ch65
calib_packv5_042523_0143.root, FC#2, port C2
Entries 723
Mean 45.15
Std Dev 11.12
Turn on : 28.0606
Width : 2.274
Height : 19.925
Entry
ampl
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6
8
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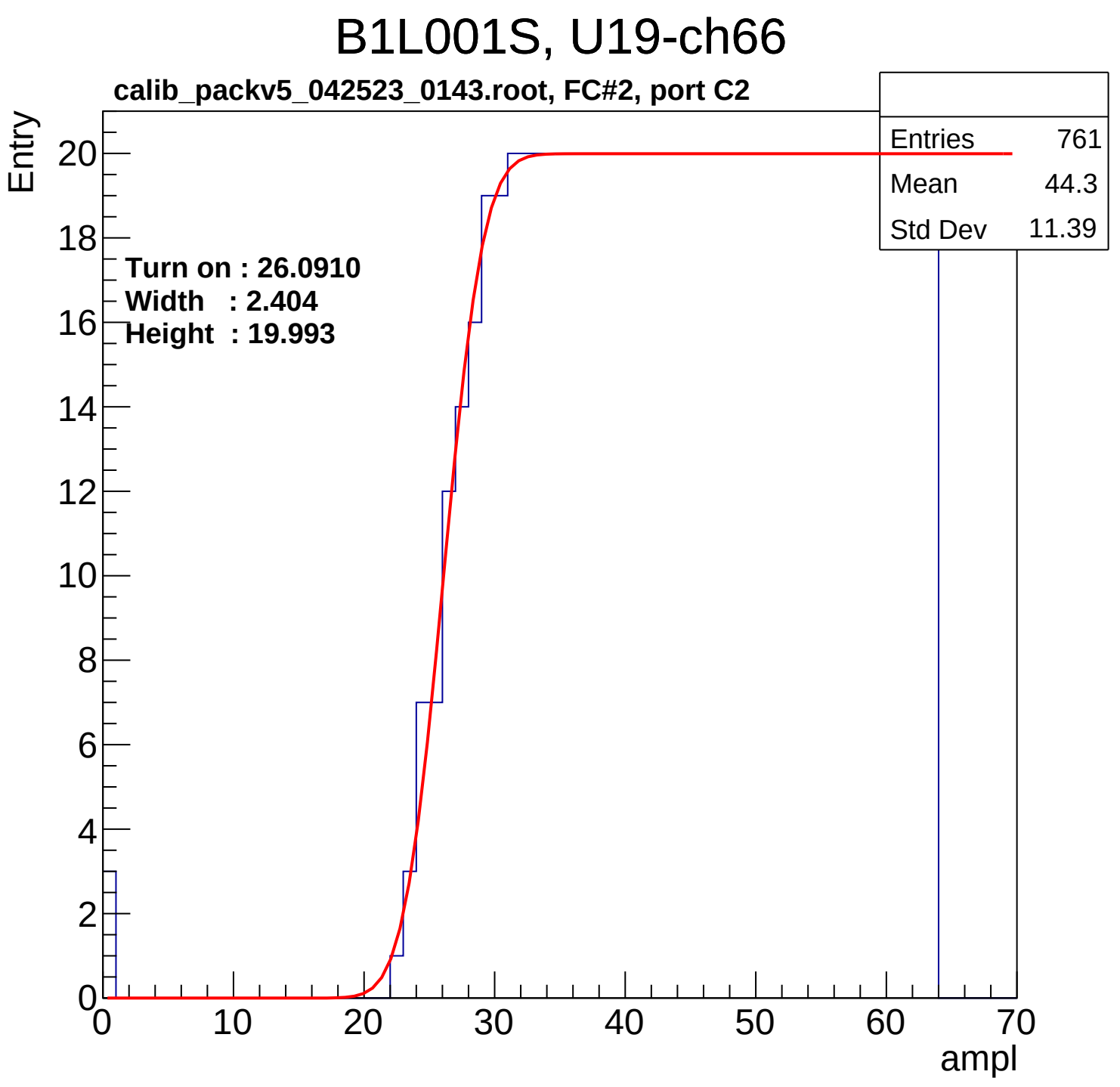
B1L001S, U19-ch66
calib_packv5_042523_0143.root, FC#2, port C2
Entries 761
Mean 44.3
Std Dev 11.39
Turn on : 26.0910
Width : 2.404
Height : 19.993
Entry
ampl
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6
8
10
12
14
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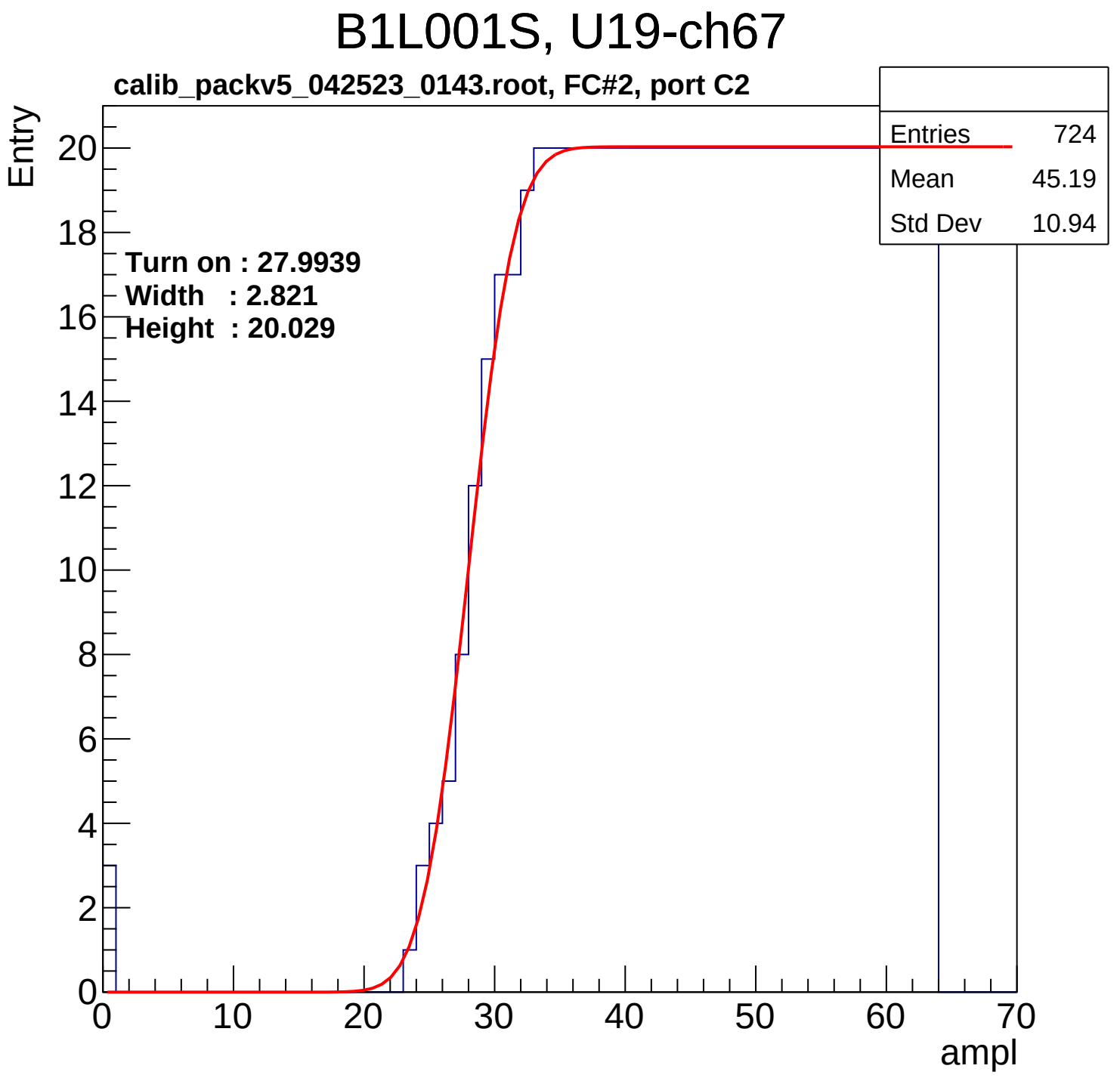
B1L001S, U19-ch67
calib_packv5_042523_0143.root, FC#2, port C2
Entries 724
Mean 45.19
Std Dev 10.94
Turn on : 27.9939
Width : 2.821
Height : 20.029
Entry
ampl
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6
8
10
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14
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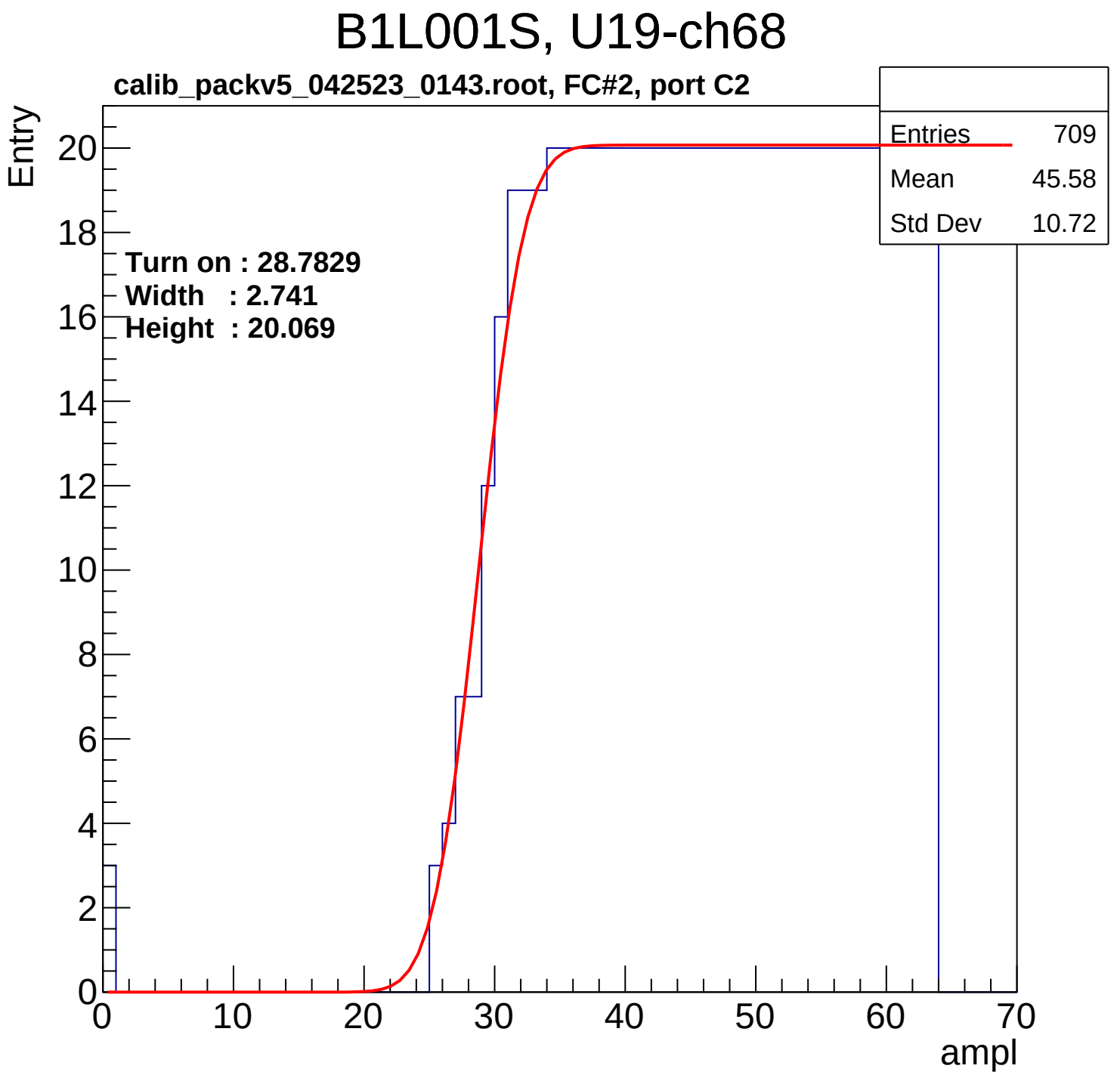
B1L001S, U19-ch68
calib_packv5_042523_0143.root, FC#2, port C2
Entries 709
Mean 45.58
Std Dev 10.72
Turn on : 28.7829
Width : 2.741
Height : 20.069
Entry
ampl
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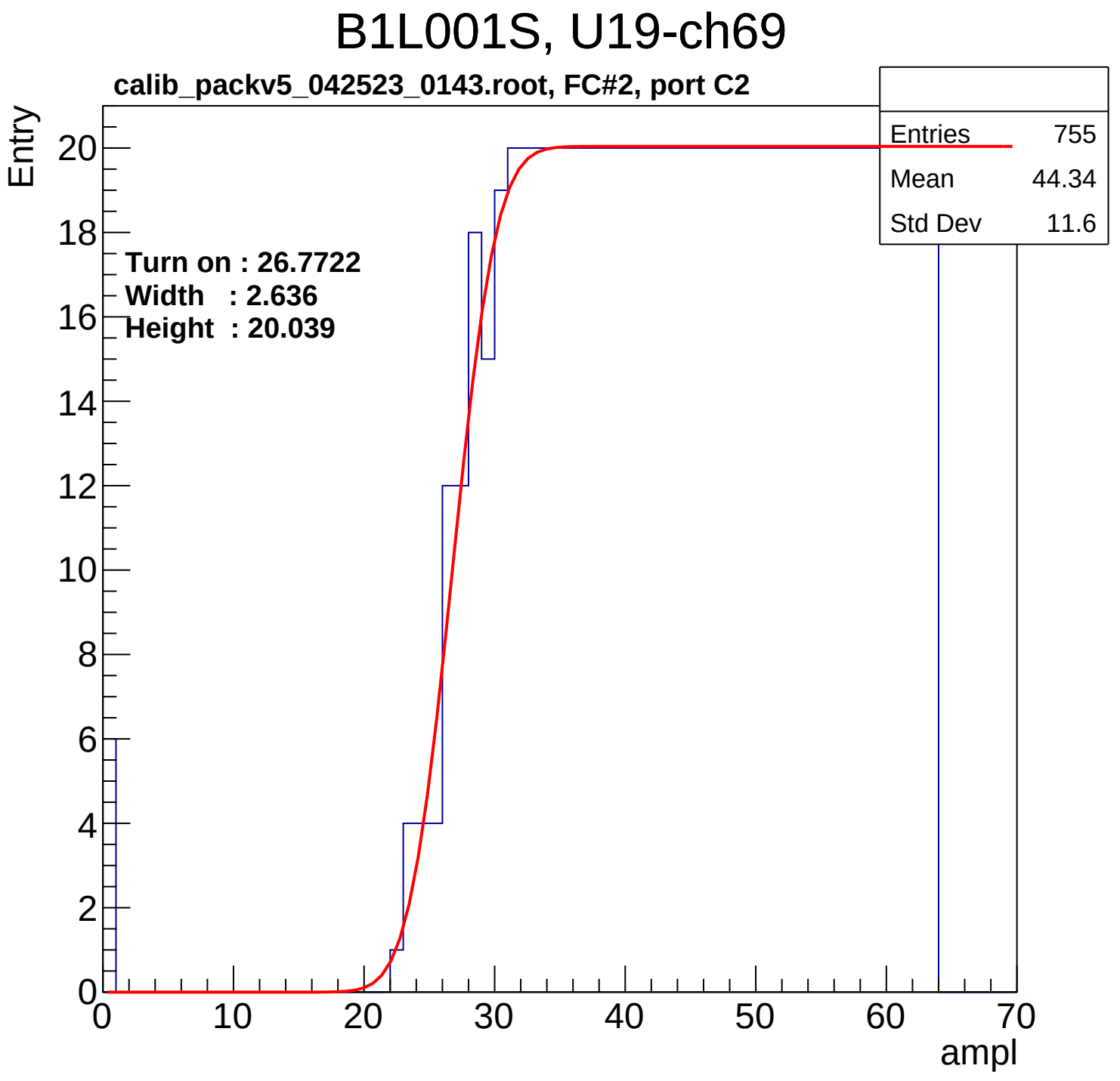
B1L001S, U19-ch69
calib_packv5_042523_0143.root, FC#2, port C2
Entries 755
Mean 44.34
Std Dev 11.6
Turn on : 26.7722
Width : 2.636
Height : 20.039
Entry
ampl
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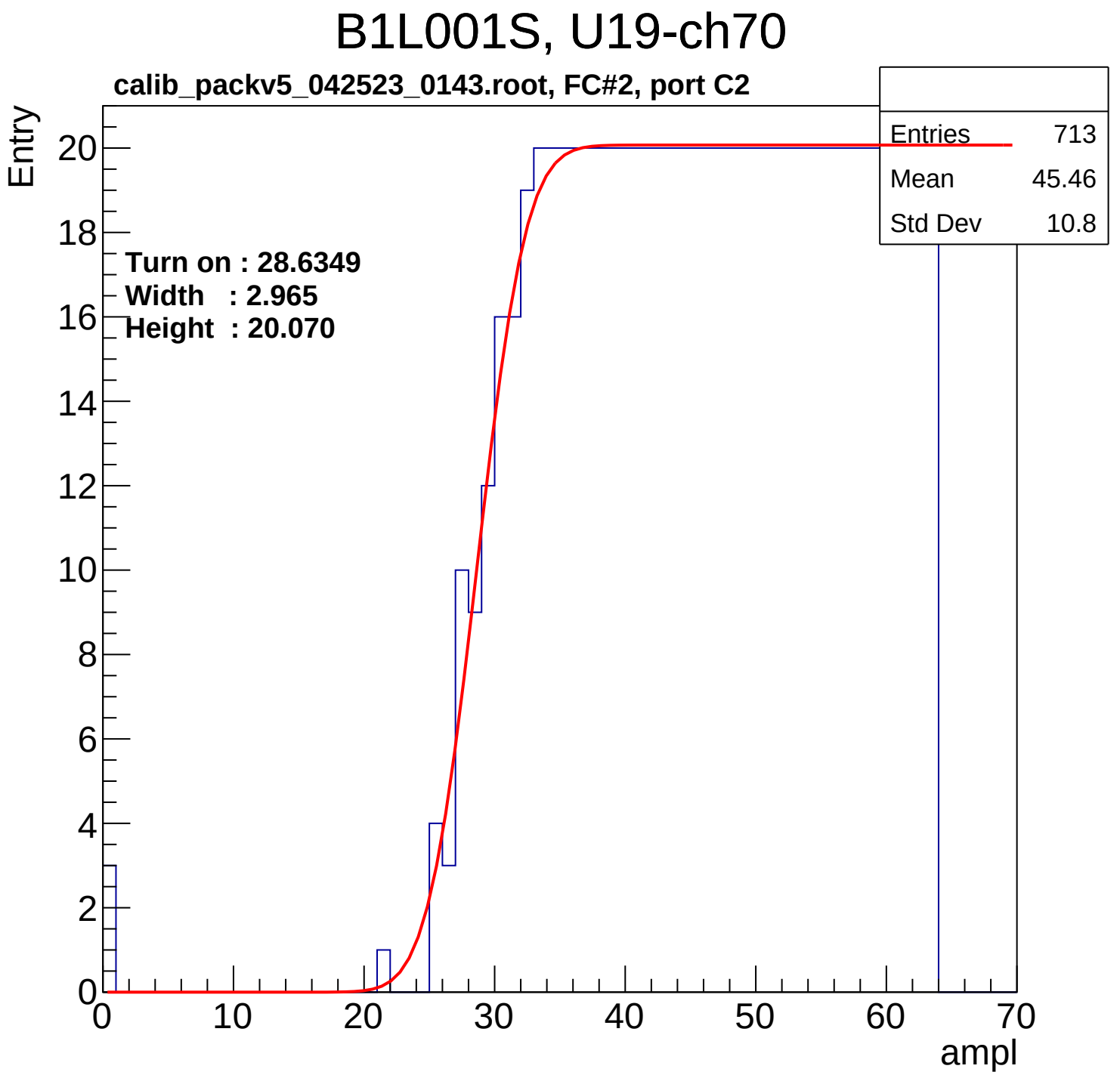
B1L001S, U19-ch70
calib_packv5_042523_0143.root, FC#2, port C2
Entries 713
Mean 45.46
Std Dev 10.8
Turn on : 28.6349
Width : 2.965
Height : 20.070
Entry
ampl
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6
8
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12
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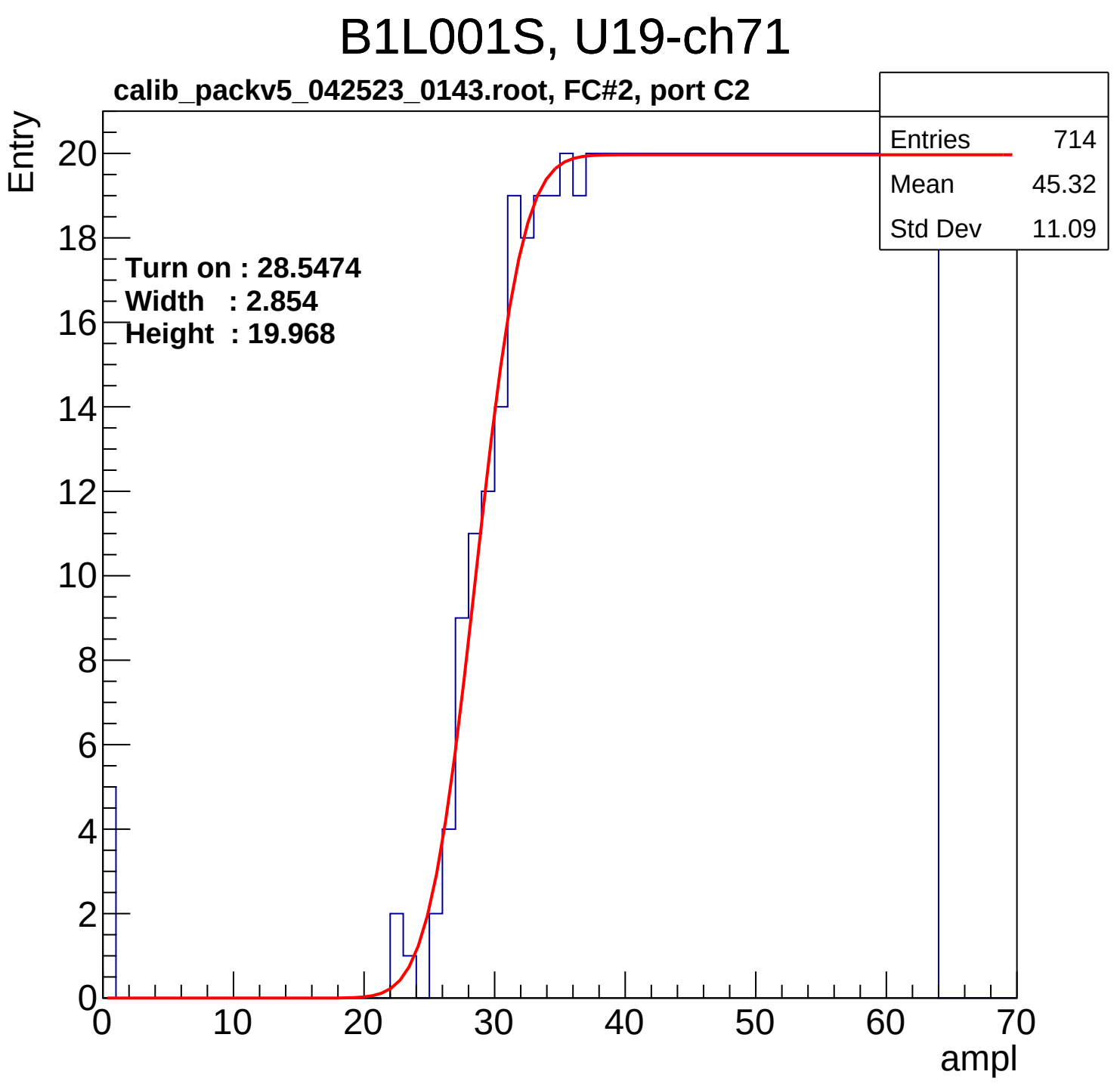
B1L001S, U19-ch71
calib_packv5_042523_0143.root, FC#2, port C2
Entries 714
Mean 45.32
Std Dev 11.09
Turn on : 28.5474
Width : 2.854
Height : 19.968
Entry
ampl
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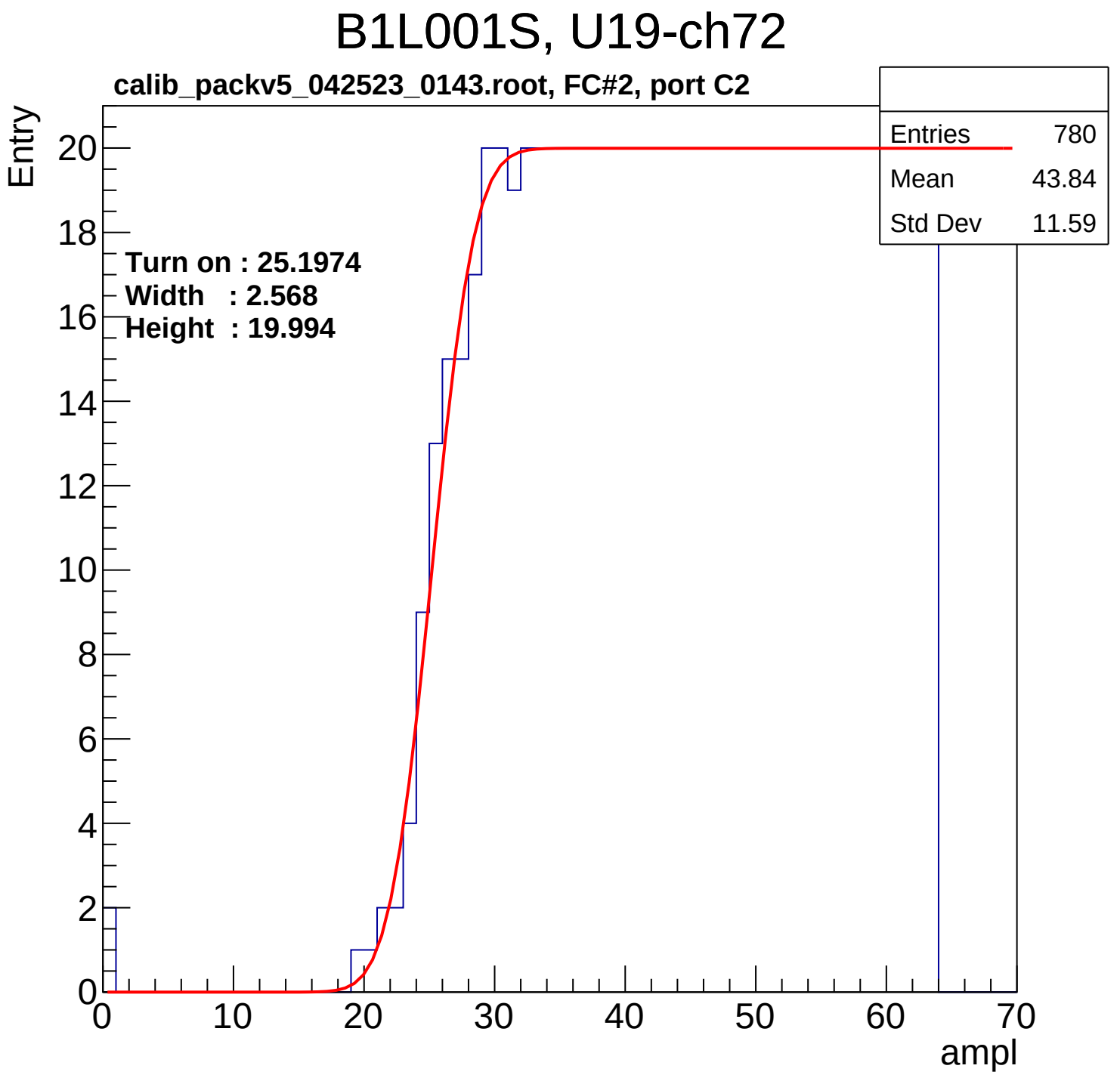
B1L001S, U19-ch72
calib_packv5_042523_0143.root, FC#2, port C2
Entries 780
Mean 43.84
Std Dev 11.59
Turn on : 25.1974
Width : 2.568
Height : 19.994
Entry
ampl
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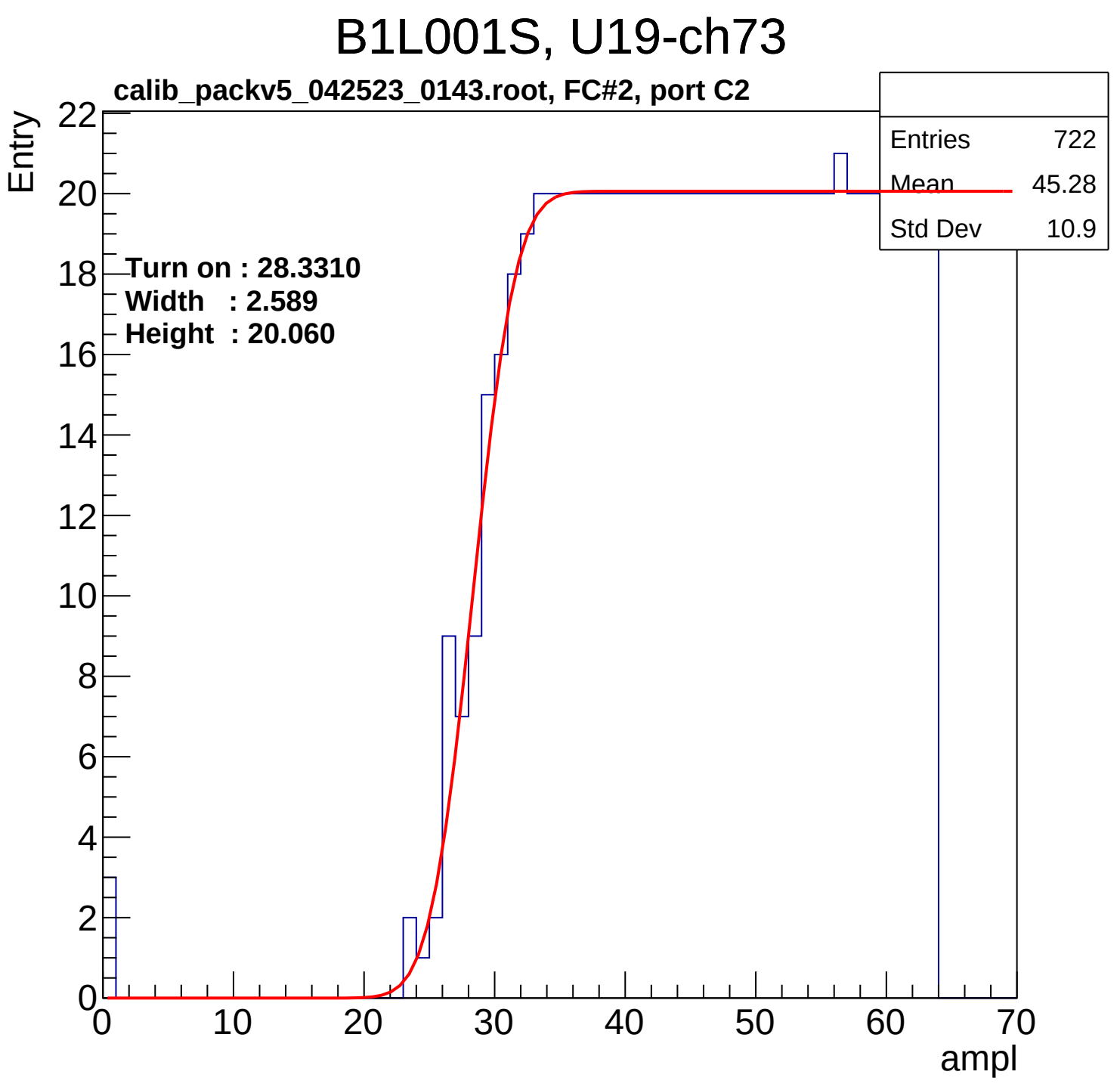
B1L001S, U19-ch73
calib_packv5_042523_0143.root, FC#2, port C2
Entries 722
Mean 45.28
Std Dev 10.9
Turn on : 28.3310
Width : 2.589
Height : 20.060
Entry
ampl
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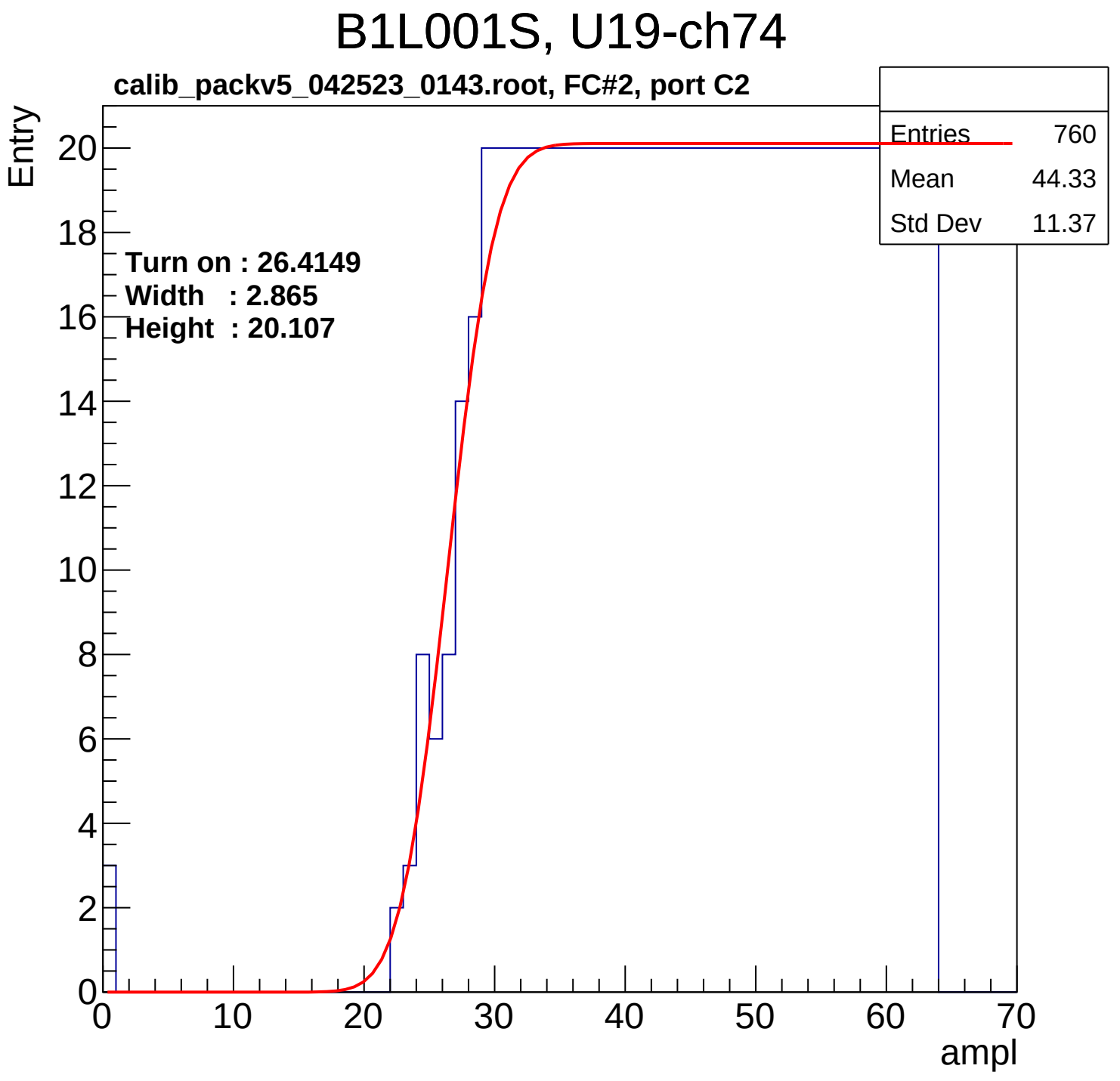
B1L001S, U19-ch74
calib_packv5_042523_0143.root, FC#2, port C2
Entries 760
Mean 44.33
Std Dev 11.37
Turn on : 26.4149
Width : 2.865
Height : 20.107
Entry
ampl
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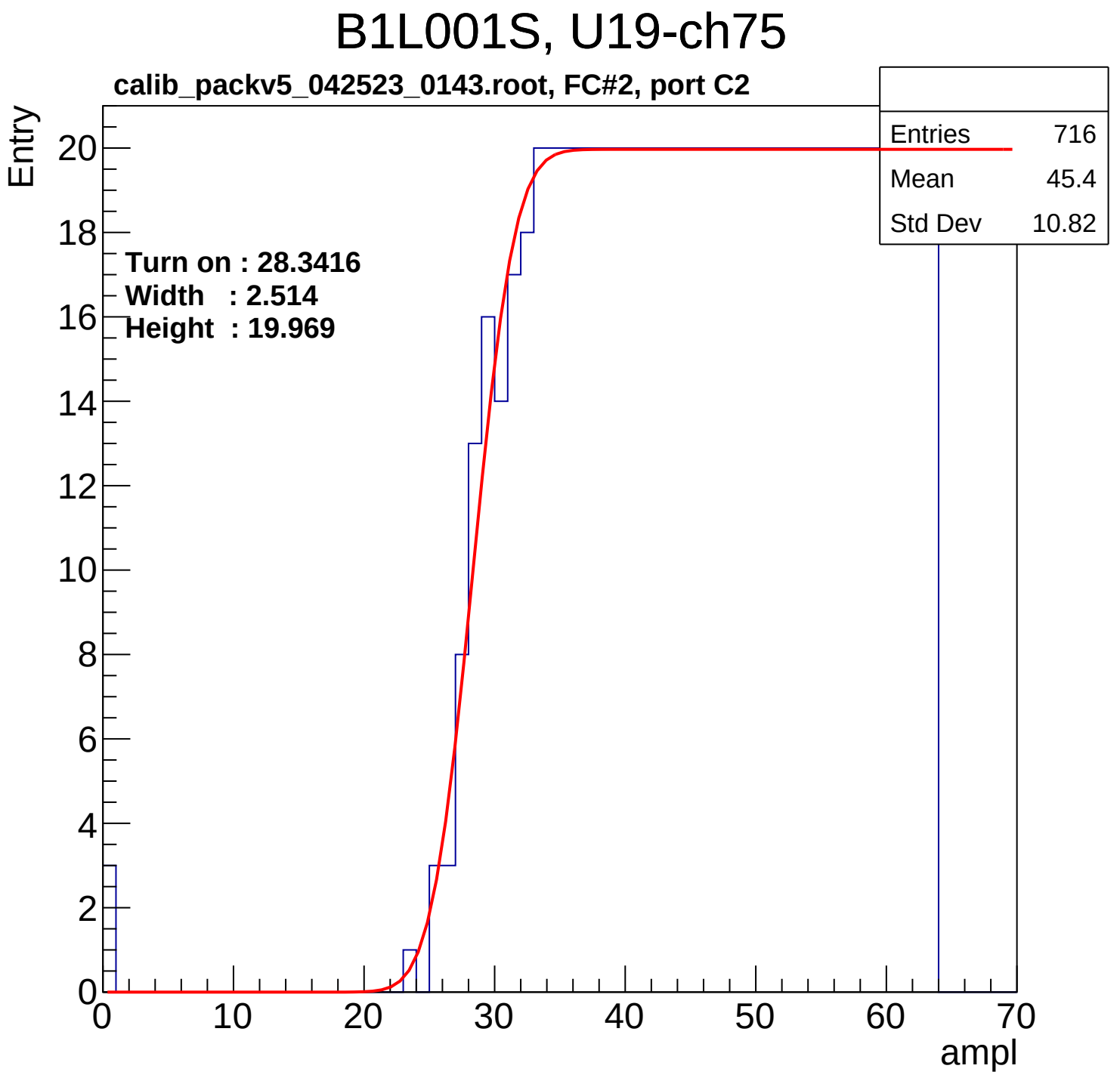
B1L001S, U19-ch75
calib_packv5_042523_0143.root, FC#2, port C2
Entries 716
Mean 45.4
Std Dev 10.82
Turn on : 28.3416
Width : 2.514
Height : 19.969
Entry
ampl
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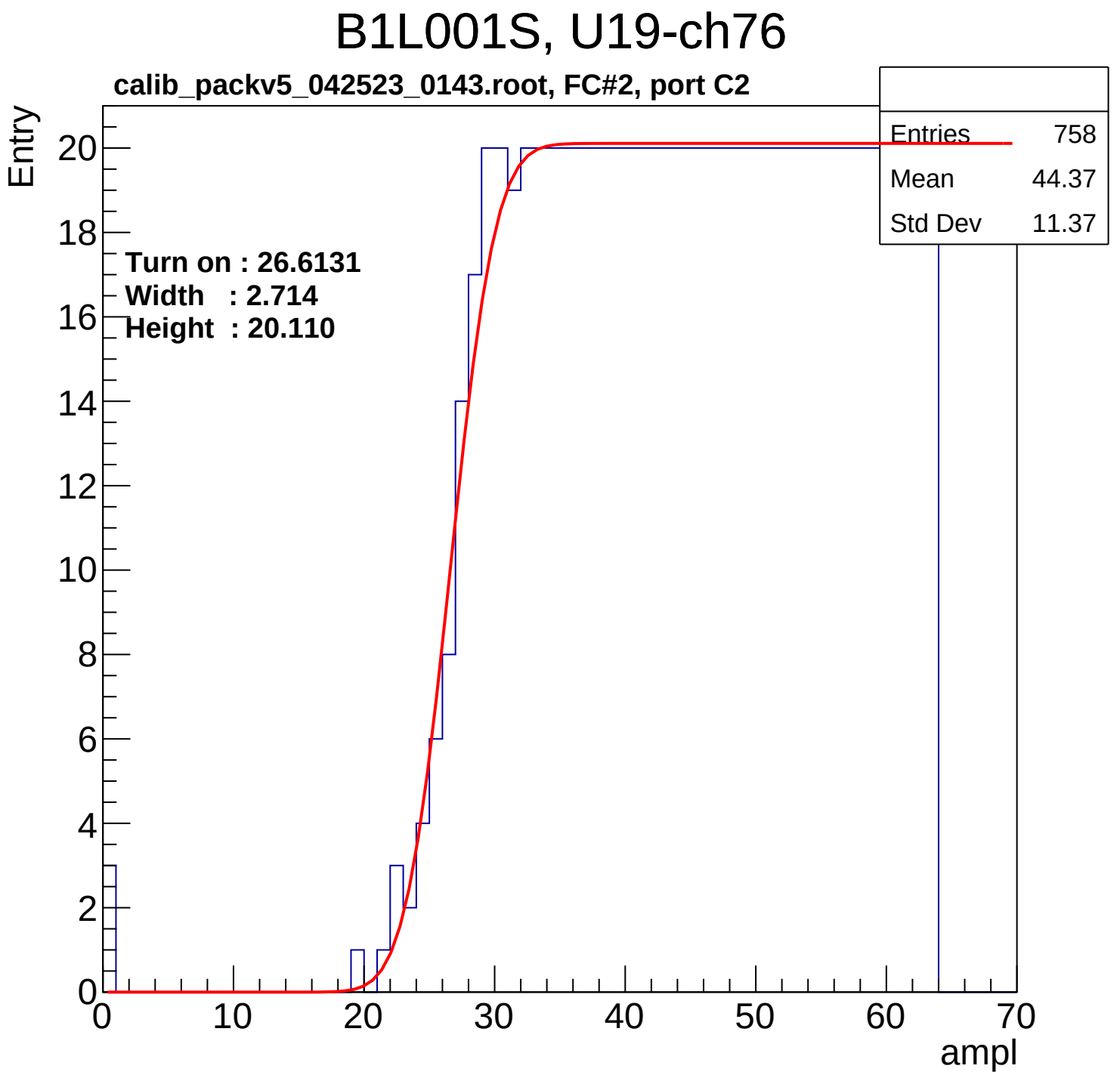
B1L001S, U19-ch76
calib_packv5_042523_0143.root, FC#2, port C2
Entries 758
Mean 44.37
Std Dev 11.37
Turn on : 26.6131
Width : 2.714
Height : 20.110
Entry
ampl
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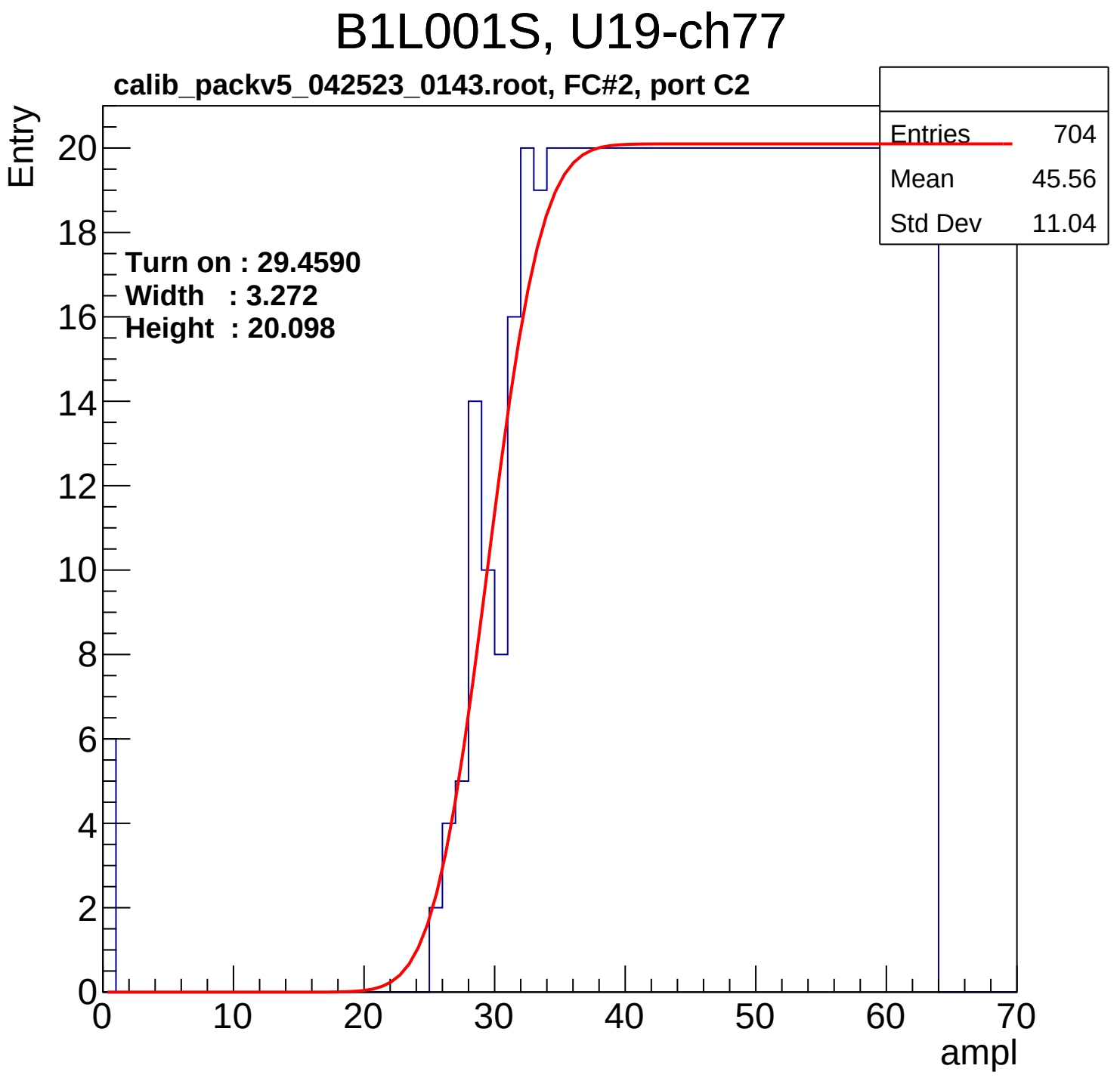
B1L001S, U19-ch77
calib_packv5_042523_0143.root, FC#2, port C2
Entries 704
Mean 45.56
Std Dev 11.04
Turn on : 29.4590
Width : 3.272
Height : 20.098
Entry
ampl
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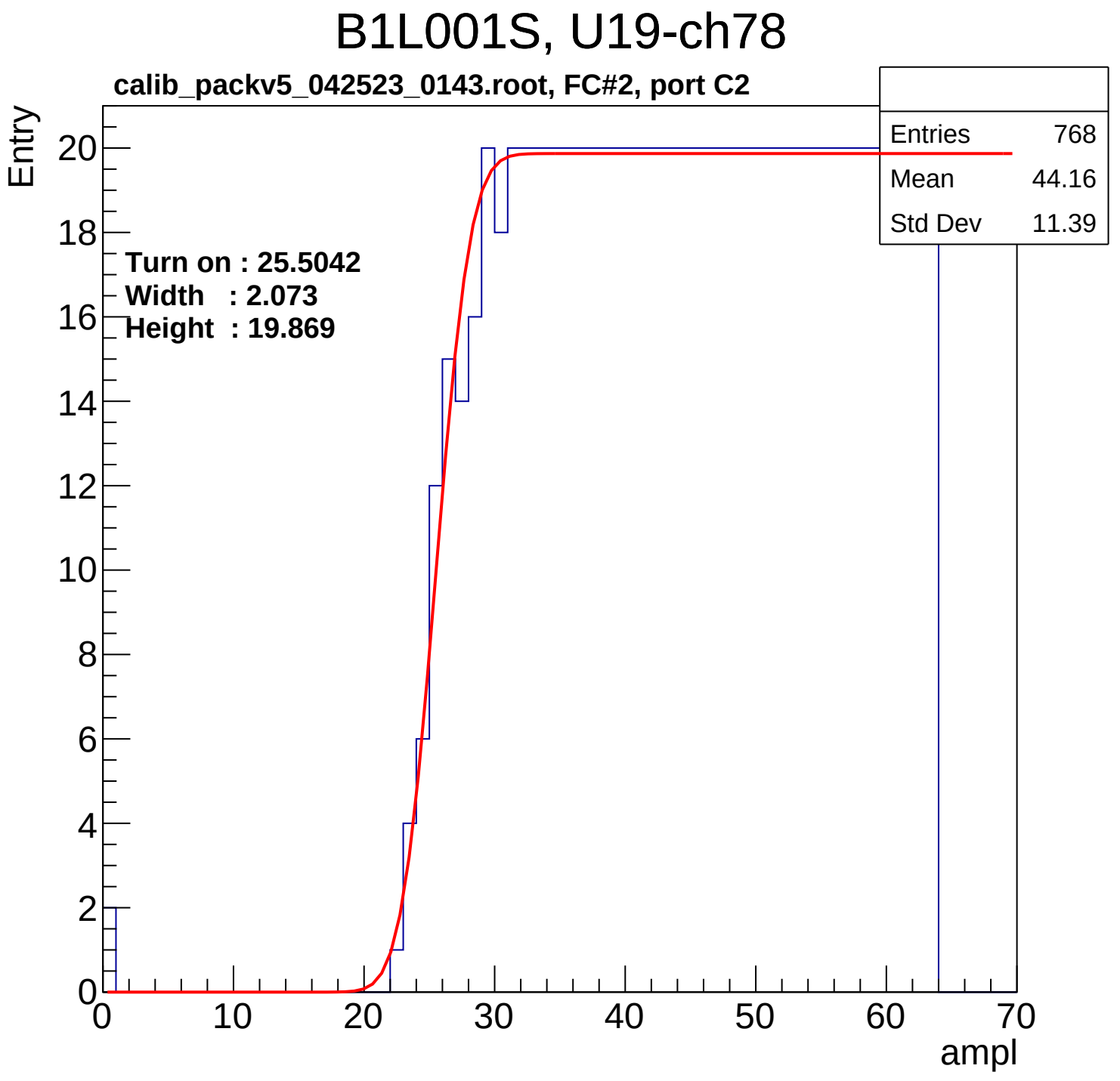
B1L001S, U19-ch78
calib_packv5_042523_0143.root, FC#2, port C2
Entries 768
Mean 44.16
Std Dev 11.39
Turn on : 25.5042
Width : 2.073
Height : 19.869
Entry
ampl
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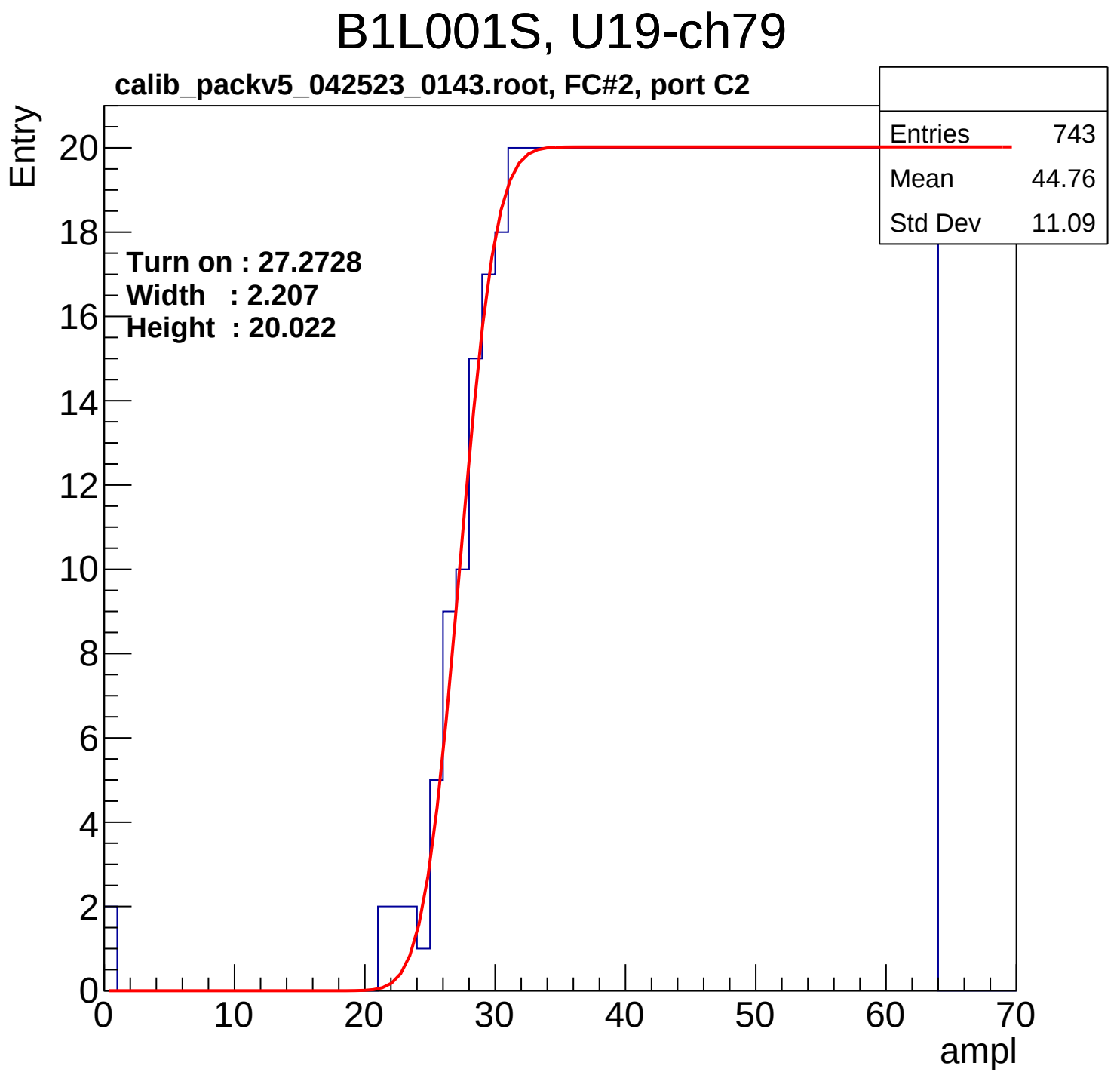
B1L001S, U19-ch79
calib_packv5_042523_0143.root, FC#2, port C2
Entries 743
Mean 44.76
Std Dev 11.09
Turn on : 27.2728
Width : 2.207
Height : 20.022
Entry
ampl
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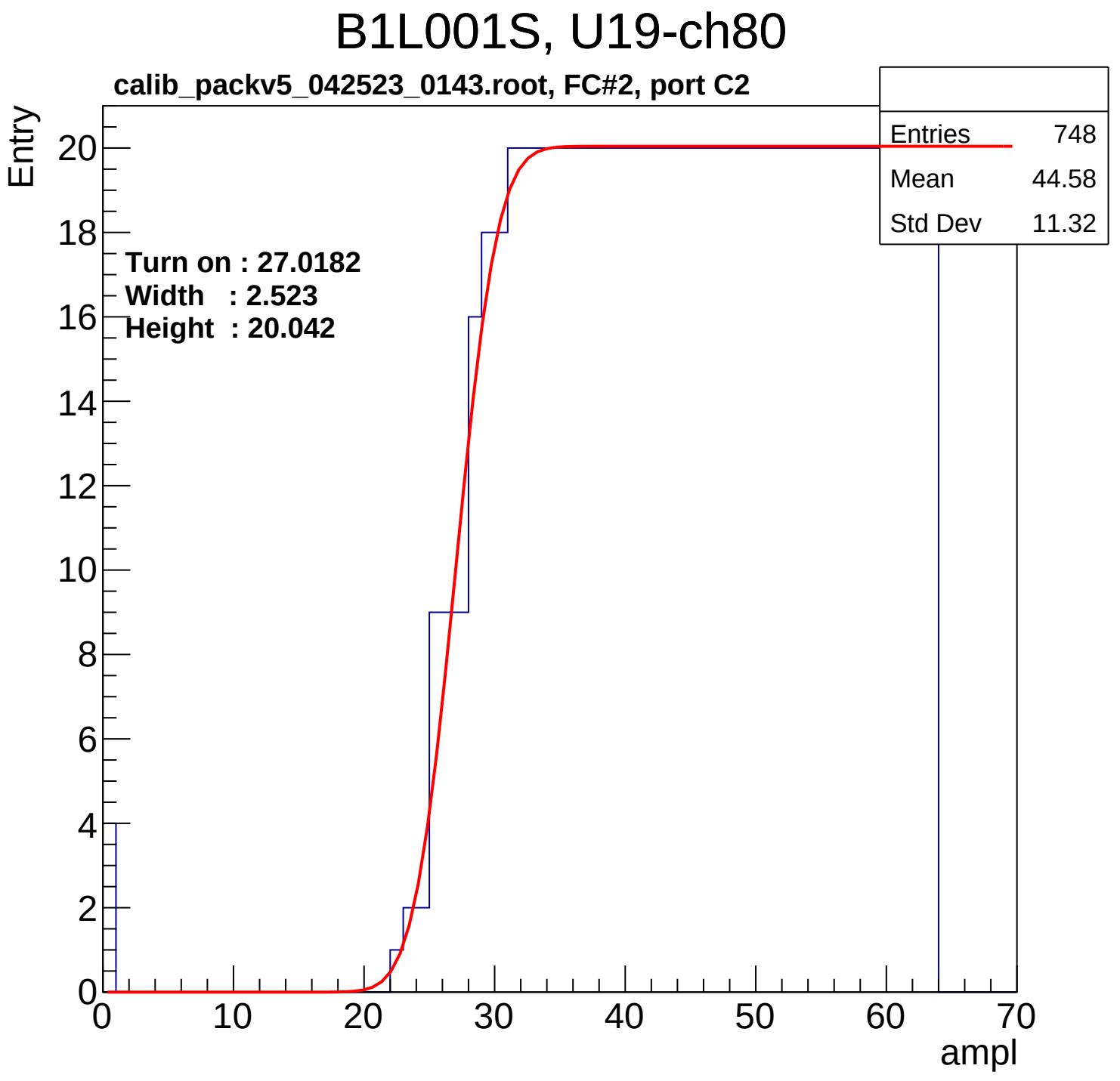
B1L001S, U19-ch80
calib_packv5_042523_0143.root, FC#2, port C2
Entries 748
Mean 44.58
Std Dev 11.32
Turn on : 27.0182
Width : 2.523
Height : 20.042
Entry
ampl
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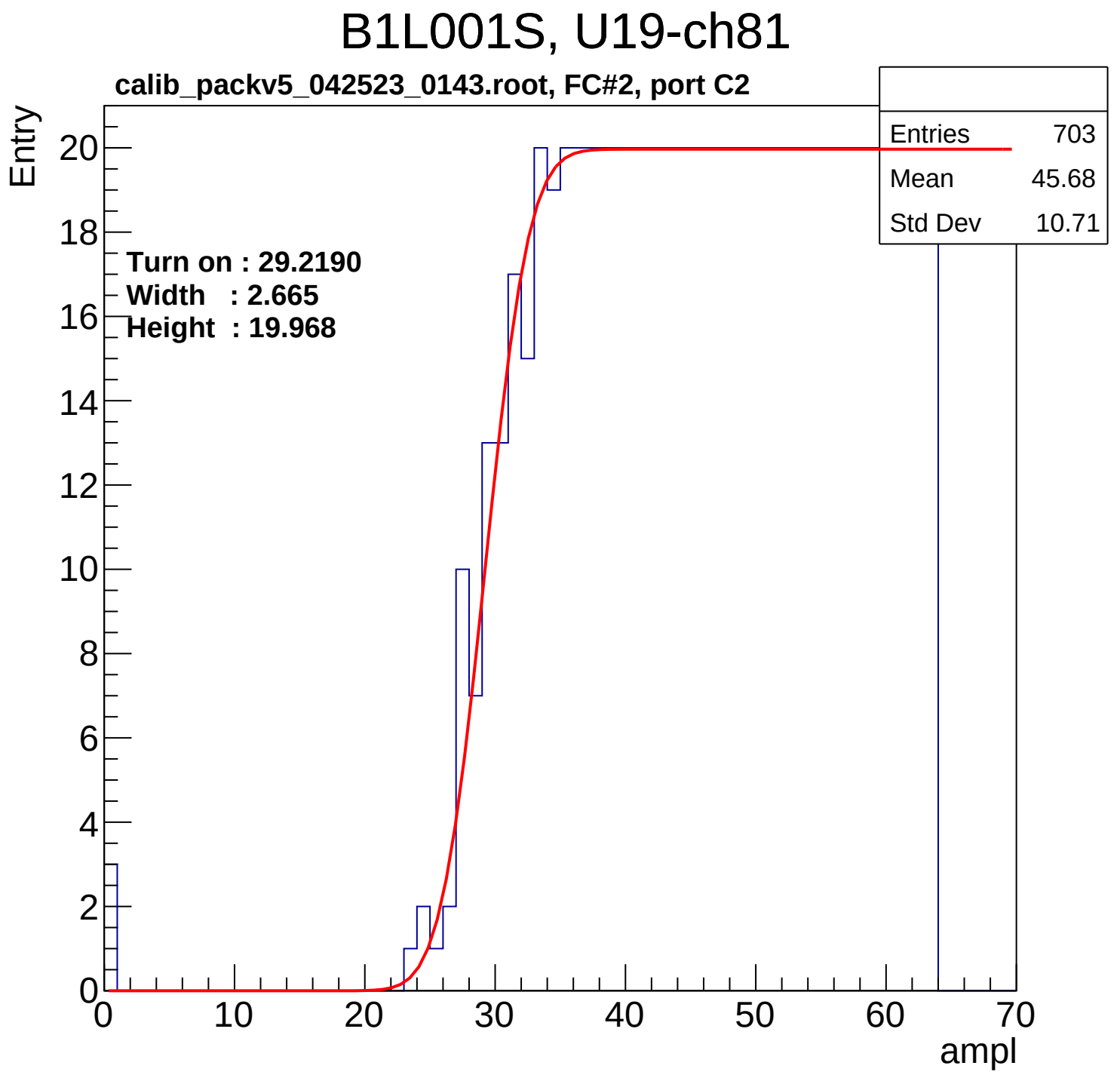
B1L001S, U19-ch81
calib_packv5_042523_0143.root, FC#2, port C2
Entries 703
Mean 45.68
Std Dev 10.71
Turn on : 29.2190
Width : 2.665
Height : 19.968
Entry
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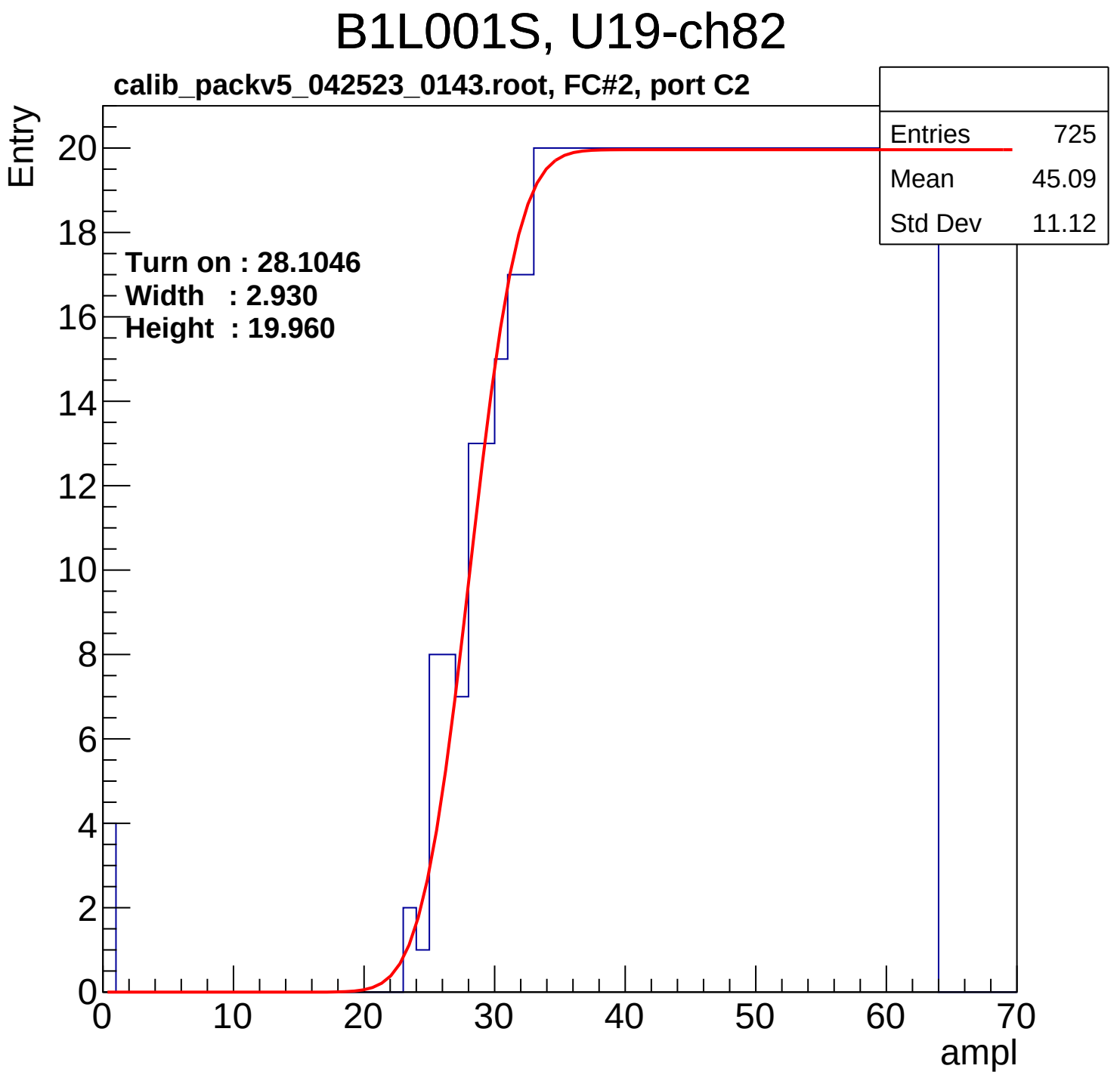
B1L001S, U19-ch82
calib_packv5_042523_0143.root, FC#2, port C2
Entries 725
Mean 45.09
Std Dev 11.12
Turn on : 28.1046
Width : 2.930
Height : 19.960
Entry
ampl
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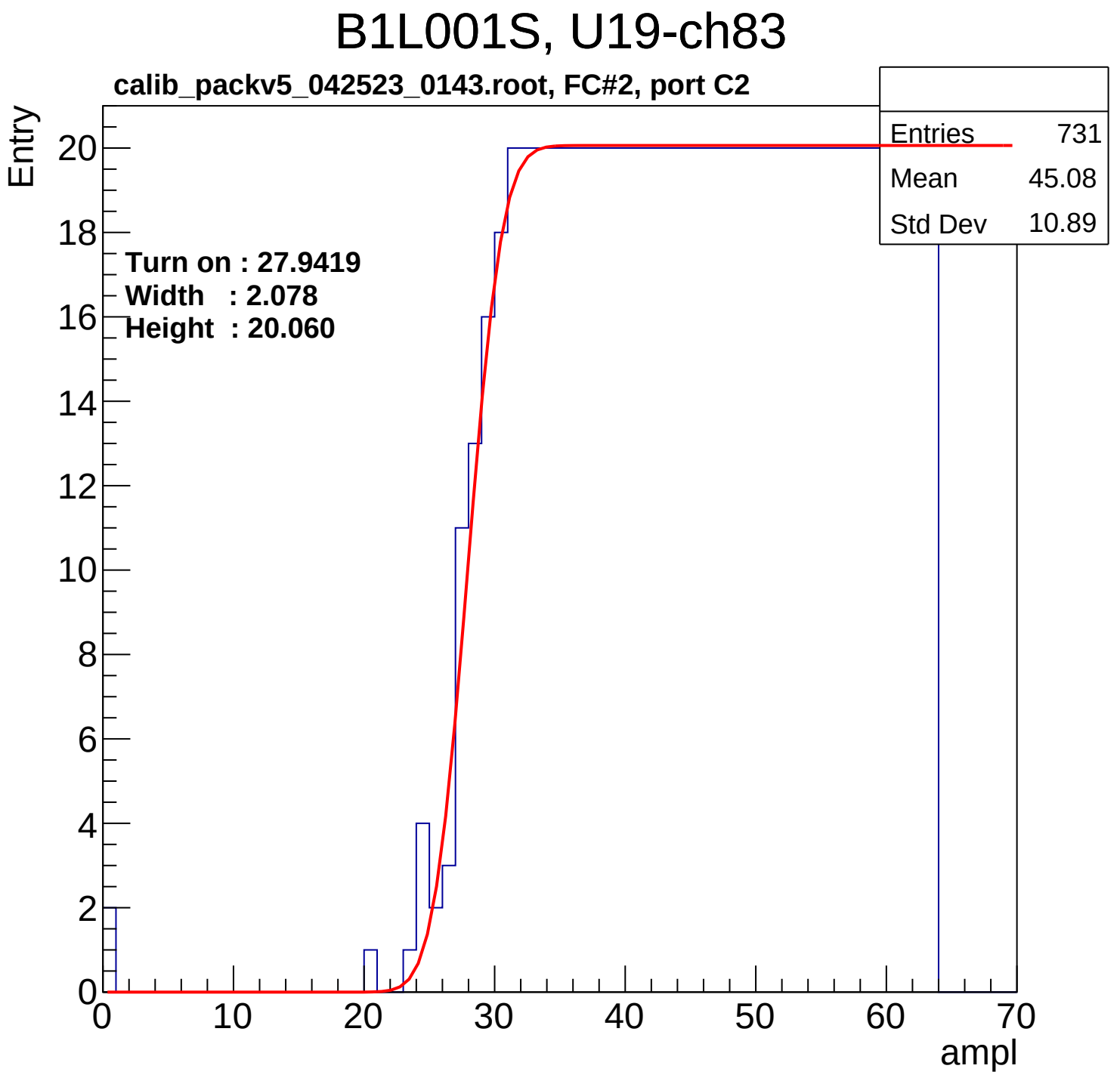
B1L001S, U19-ch83
calib_packv5_042523_0143.root, FC#2, port C2
Entries 731
Mean 45.08
Std Dev 10.89
Turn on : 27.9419
Width : 2.078
Height : 20.060
Entry
ampl
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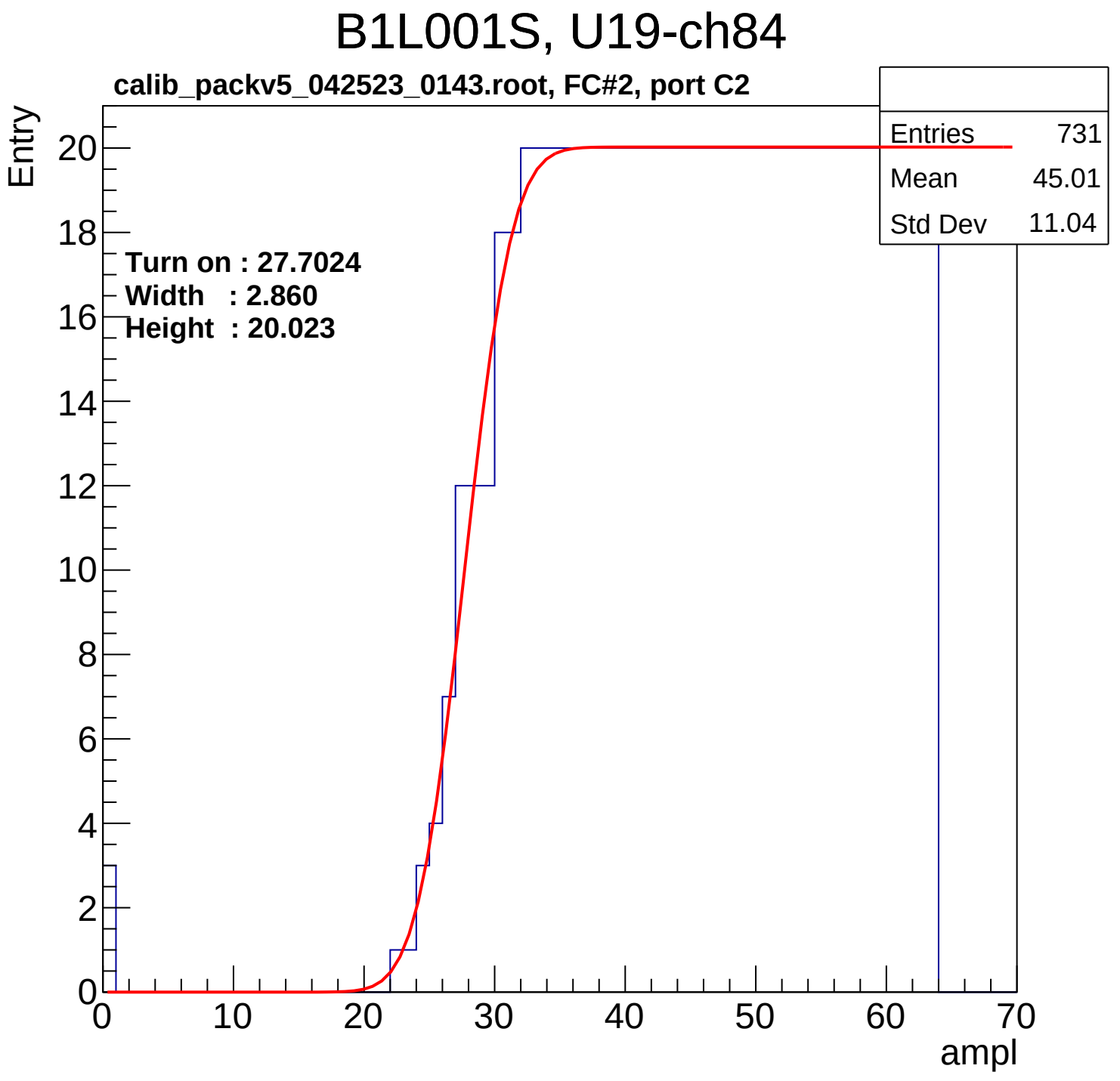
B1L001S, U19-ch84
calib_packv5_042523_0143.root, FC#2, port C2
Entries 731
Mean 45.01
Std Dev 11.04
Turn on : 27.7024
Width : 2.860
Height : 20.023
Entry
ampl
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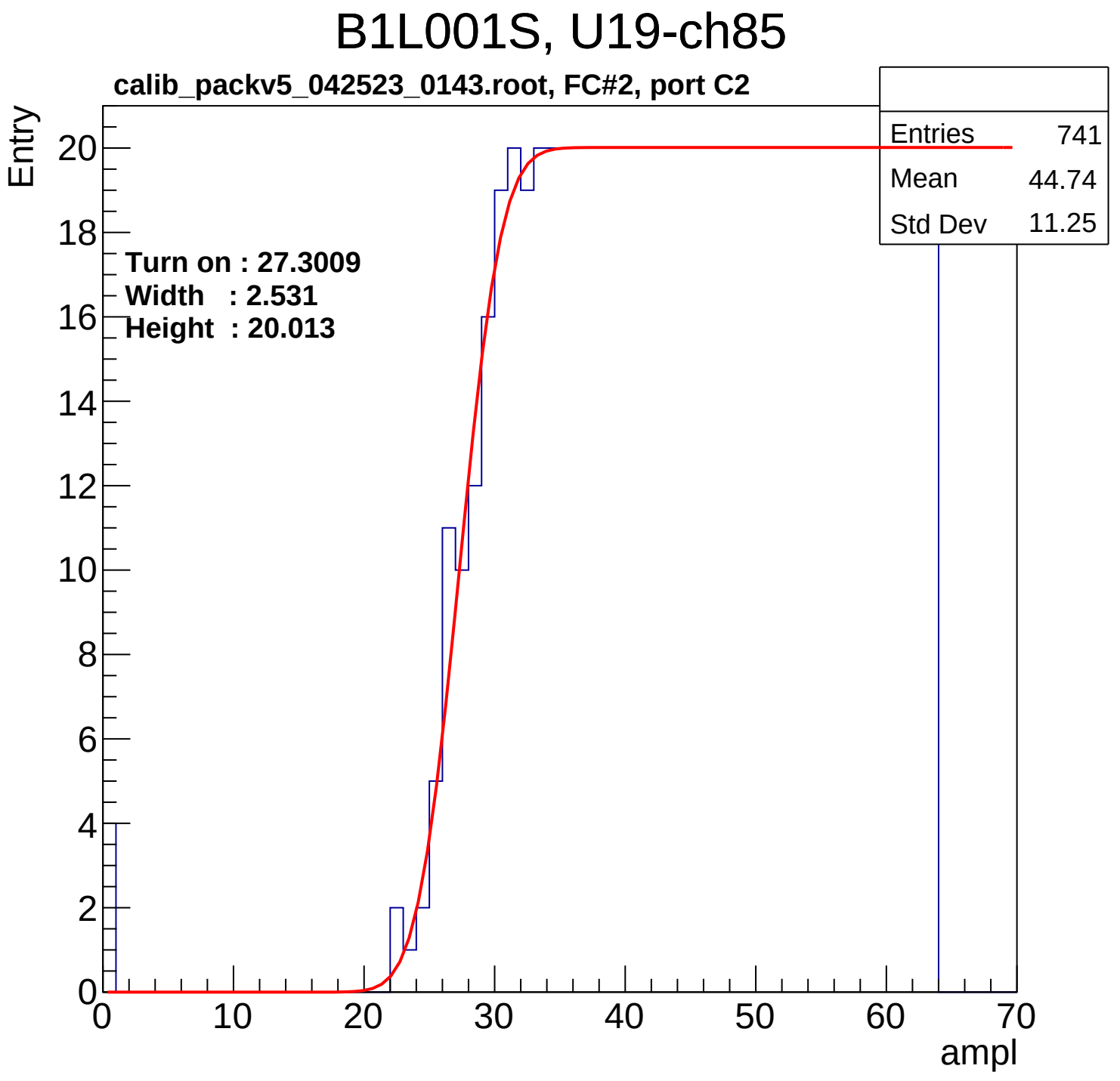
B1L001S, U19-ch85
calib_packv5_042523_0143.root, FC#2, port C2
Entries 741
Mean 44.74
Std Dev 11.25
Turn on : 27.3009
Width : 2.531
Height : 20.013
Entry
ampl
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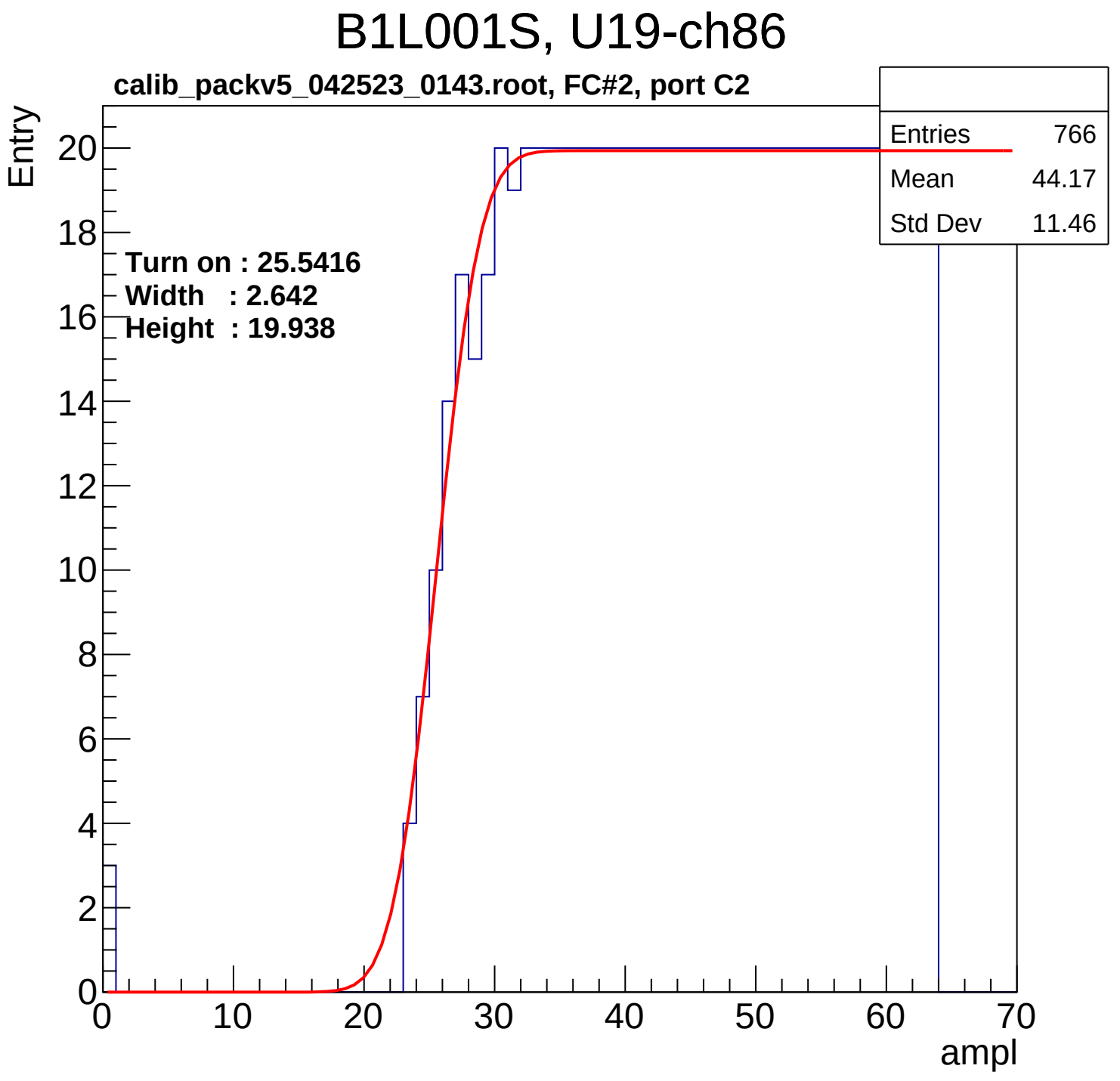
B1L001S, U19-ch86
calib_packv5_042523_0143.root, FC#2, port C2
Entries 766
Mean 44.17
Std Dev 11.46
Turn on : 25.5416
Width : 2.642
Height : 19.938
Entry
ampl
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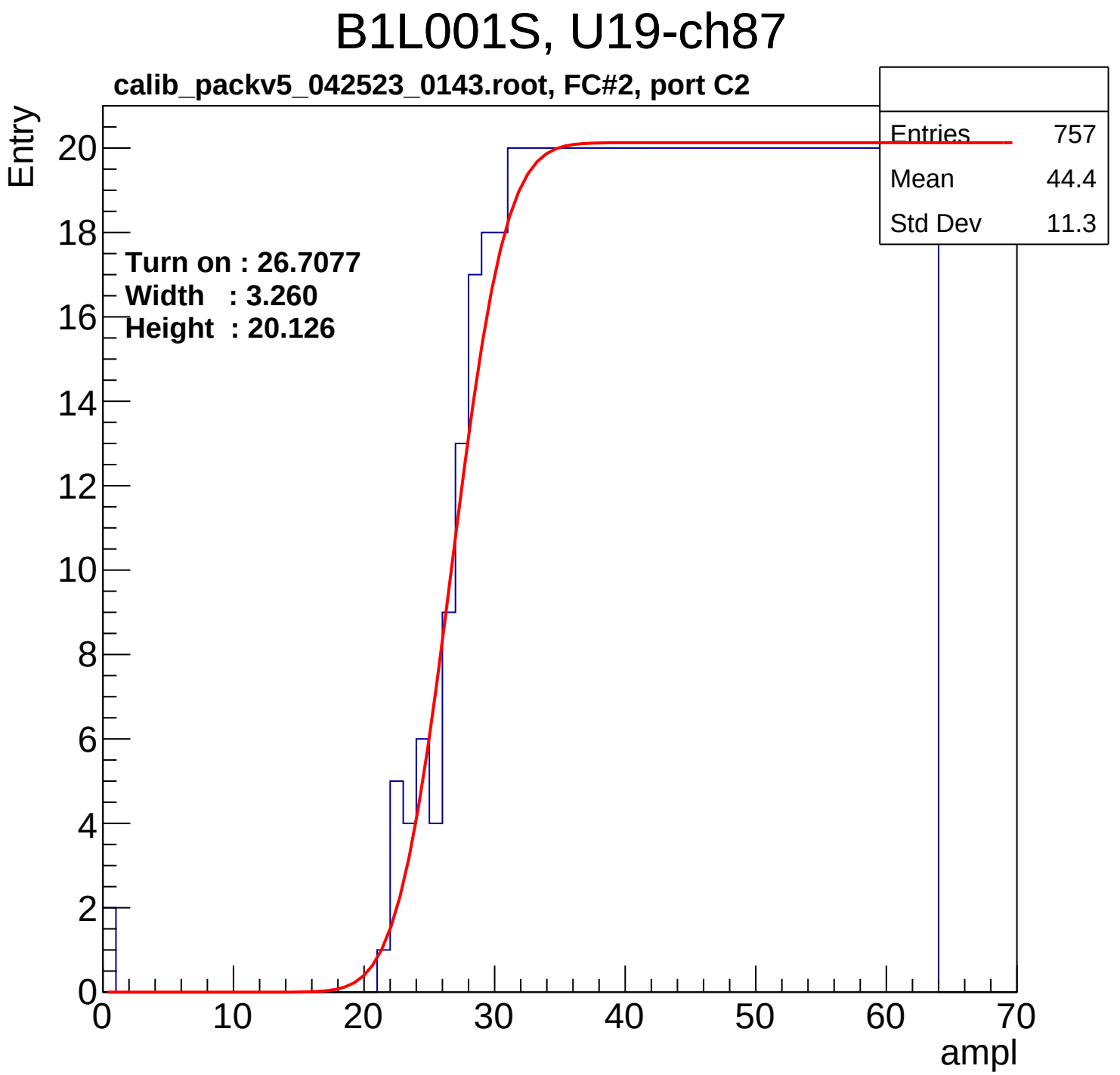
B1L001S, U19-ch87
calib_packv5_042523_0143.root, FC#2, port C2
Entries 757
Mean 44.4
Std Dev 11.3
Turn on : 26.7077
Width : 3.260
Height : 20.126
Entry
ampl
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6
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10
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14
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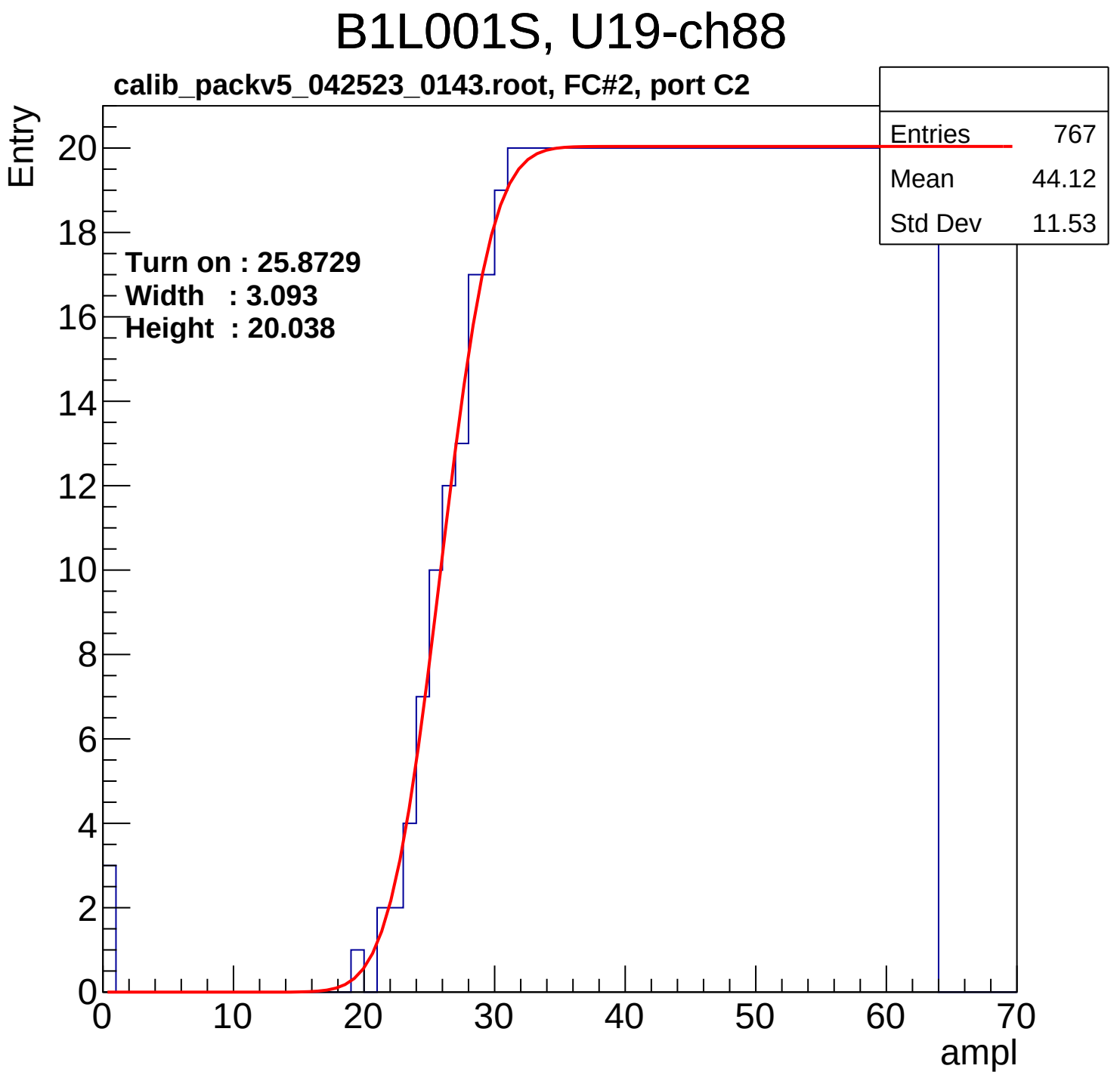
B1L001S, U19-ch88
calib_packv5_042523_0143.root, FC#2, port C2
Entries 767
Mean 44.12
Std Dev 11.53
Turn on : 25.8729
Width : 3.093
Height : 20.038
Entry
ampl
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6
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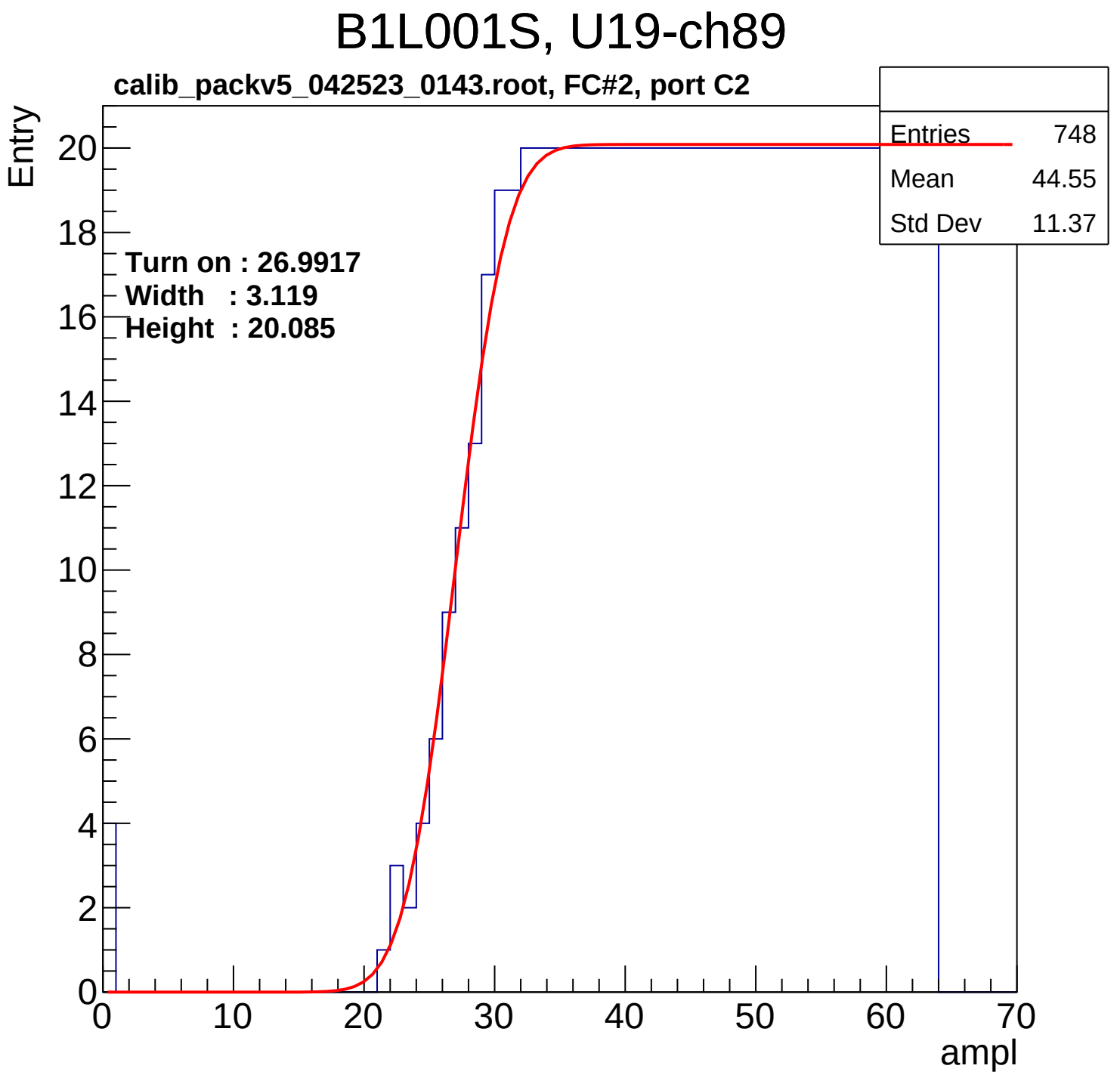
B1L001S, U19-ch89
calib_packv5_042523_0143.root, FC#2, port C2
Entries 748
Mean 44.55
Std Dev 11.37
Turn on : 26.9917
Width : 3.119
Height : 20.085
Entry
ampl
0
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12
14
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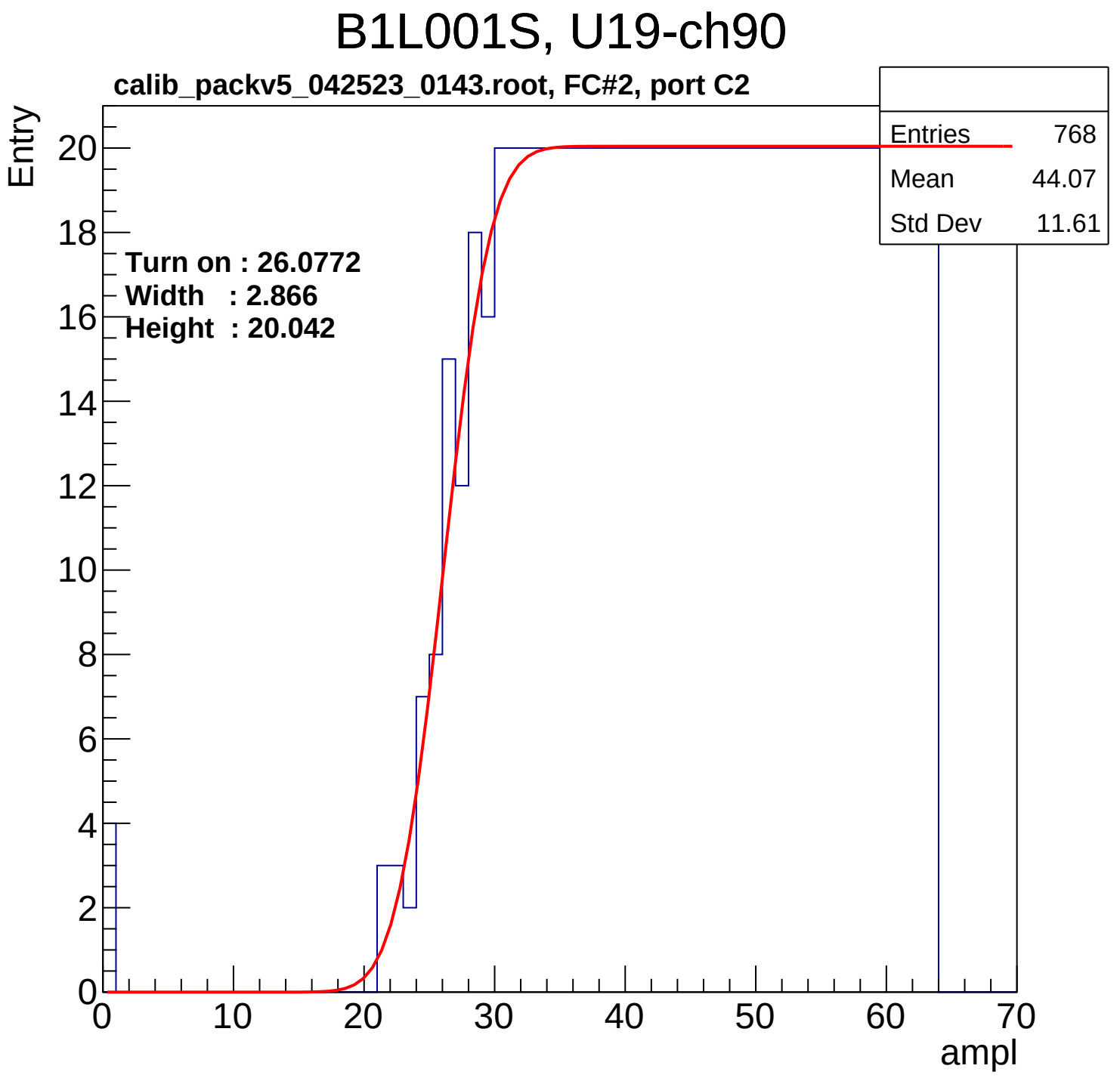
B1L001S, U19-ch90
calib_packv5_042523_0143.root, FC#2, port C2
Entries 768
Mean 44.07
Std Dev 11.61
Turn on : 26.0772
Width : 2.866
Height : 20.042
Entry
ampl
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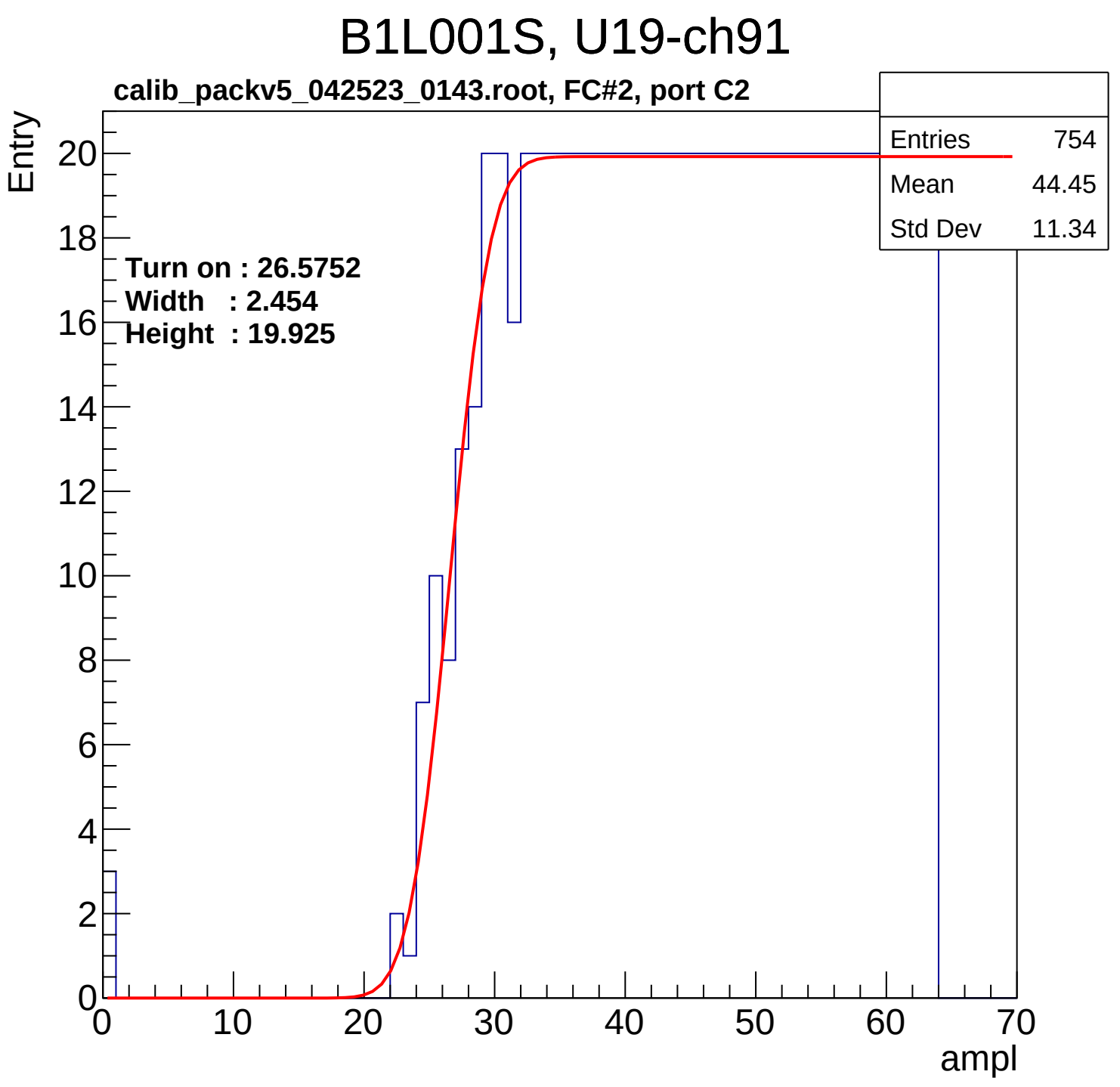
B1L001S, U19-ch91
calib_packv5_042523_0143.root, FC#2, port C2
Entries 754
Mean 44.45
Std Dev 11.34
Turn on : 26.5752
Width : 2.454
Height : 19.925
Entry
ampl
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6
8
10
12
14
16
18
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0
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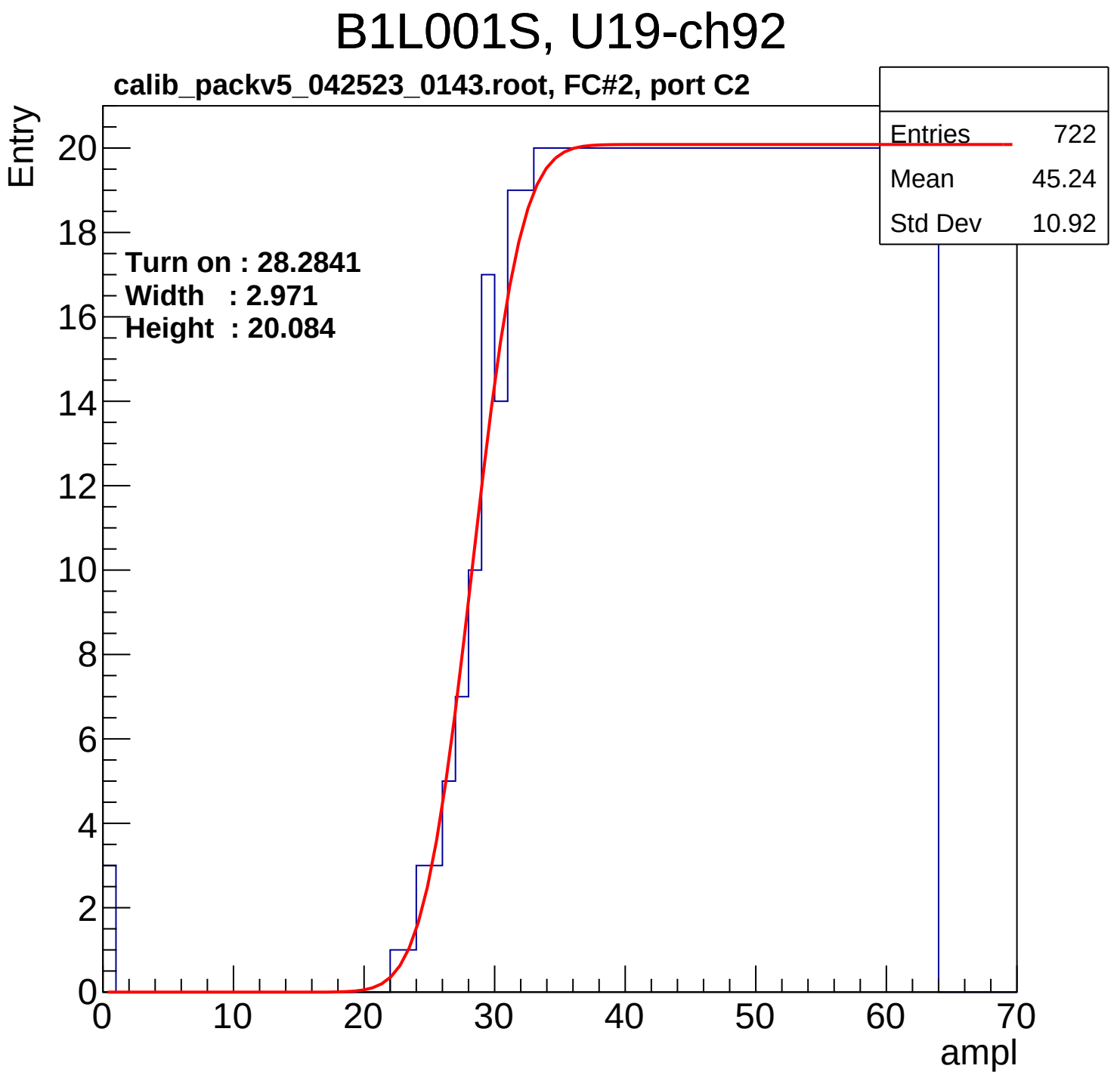
B1L001S, U19-ch92
calib_packv5_042523_0143.root, FC#2, port C2
Entries 722
Mean 45.24
Std Dev 10.92
Turn on : 28.2841
Width : 2.971
Height : 20.084
Entry
ampl
0
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6
8
10
12
14
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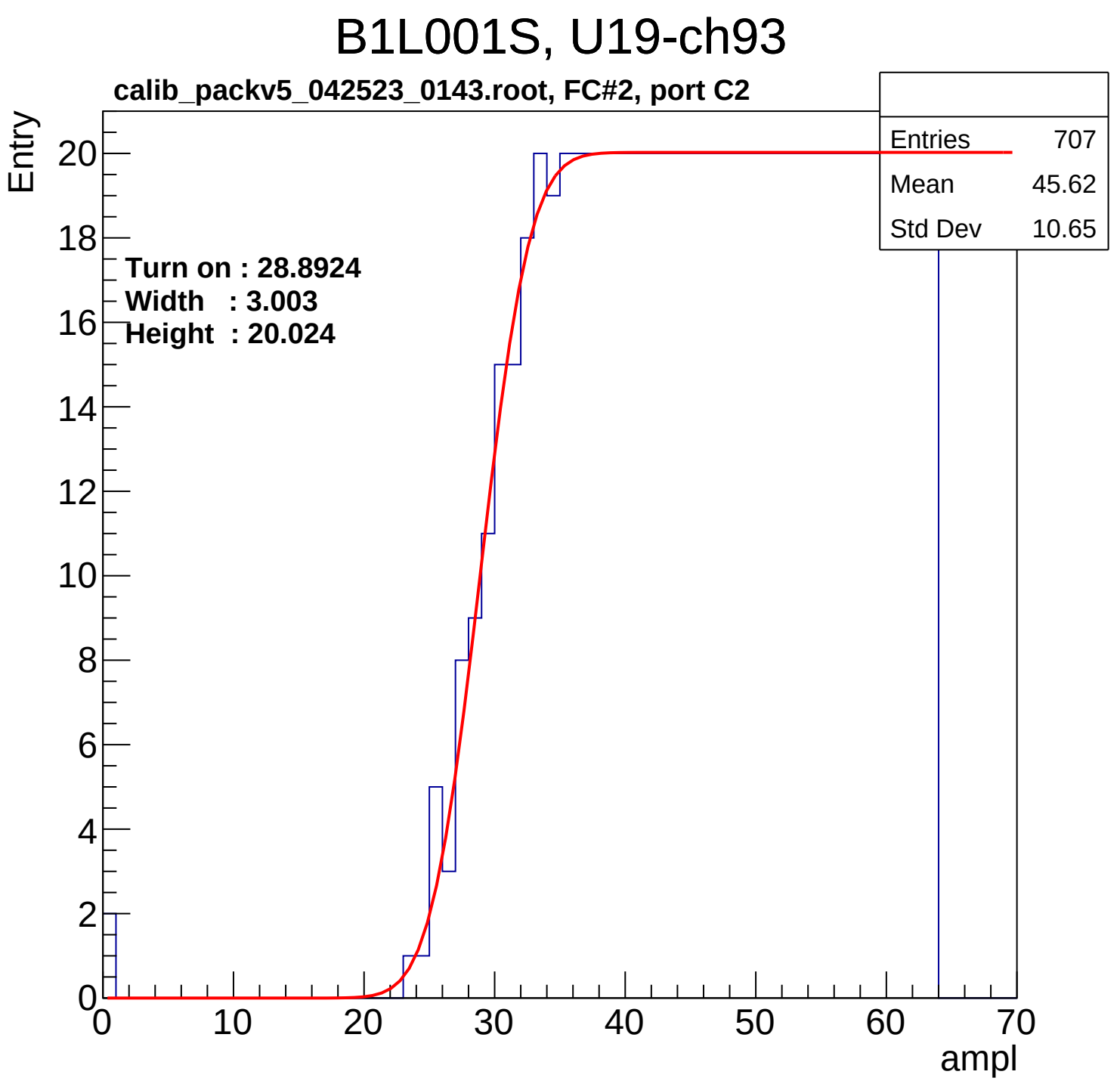
B1L001S, U19-ch93
calib_packv5_042523_0143.root, FC#2, port C2
Entries 707
Mean 45.62
Std Dev 10.65
Turn on : 28.8924
Width : 3.003
Height : 20.024
Entry
ampl
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6
8
10
12
14
16
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0
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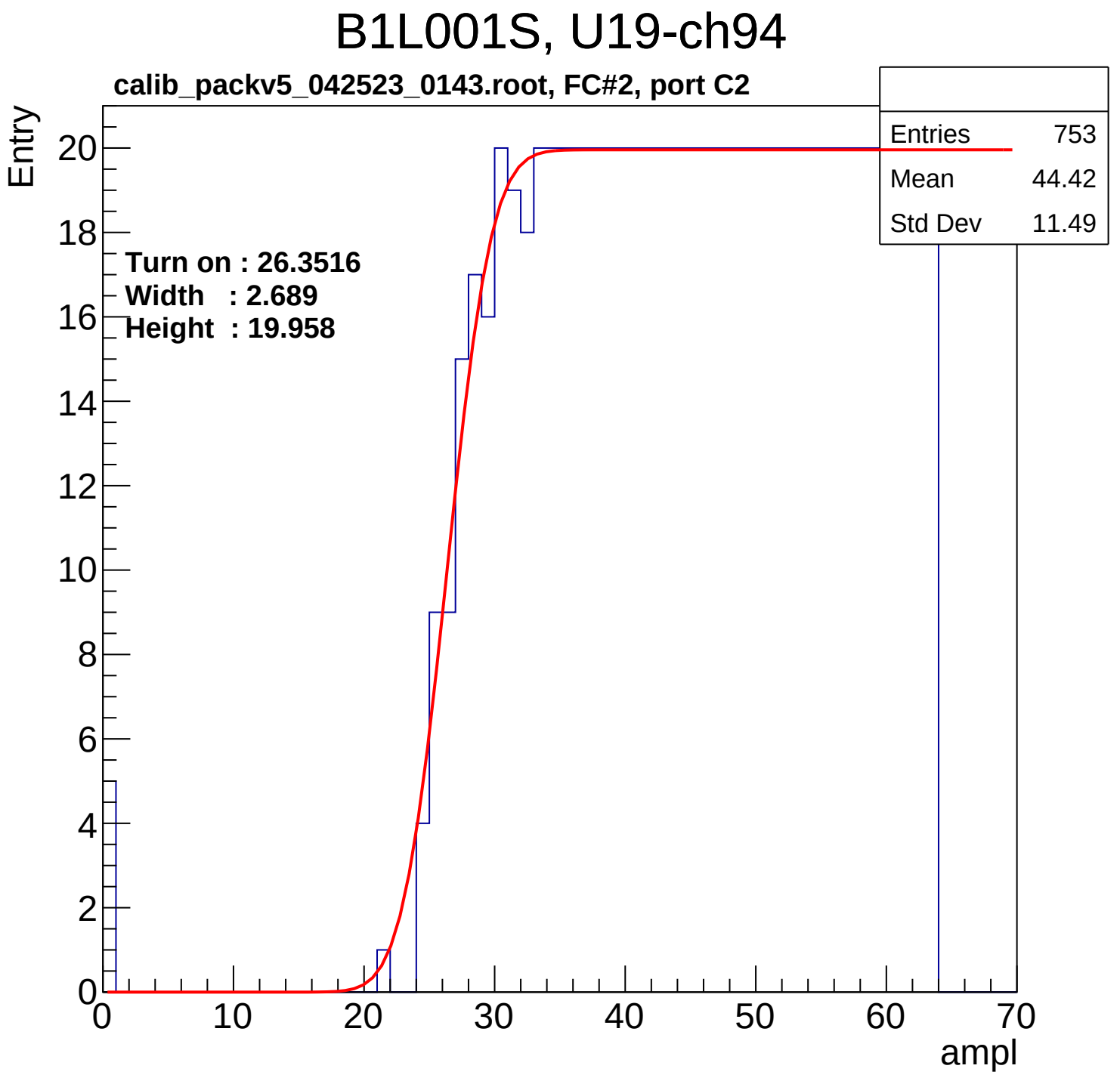
B1L001S, U19-ch94
calib_packv5_042523_0143.root, FC#2, port C2
Entries 753
Mean 44.42
Std Dev 11.49
Turn on : 26.3516
Width : 2.689
Height : 19.958
Entry
ampl
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6
8
10
12
14
16
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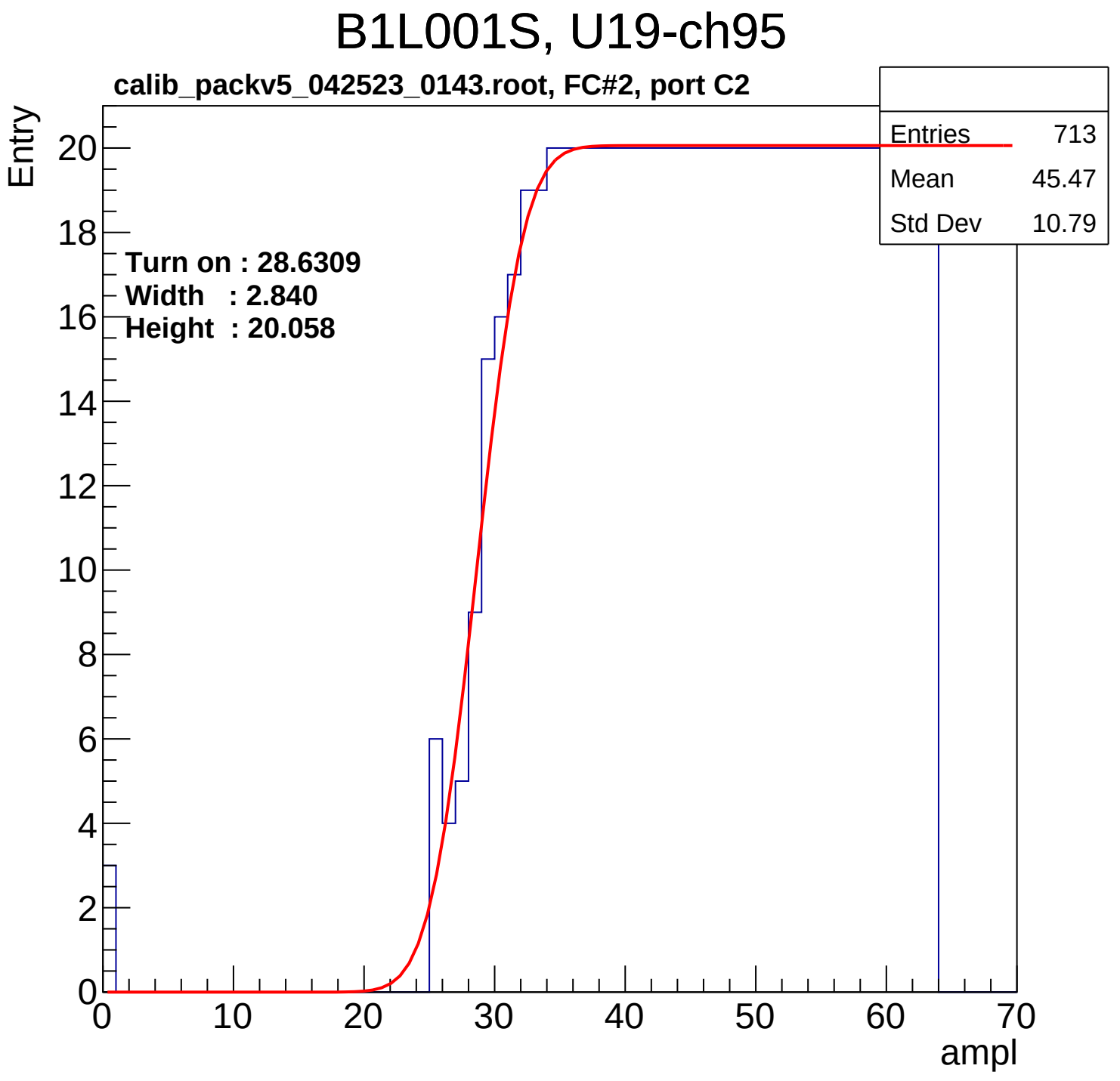
B1L001S, U19-ch95
calib_packv5_042523_0143.root, FC#2, port C2
Entries 713
Mean 45.47
Std Dev 10.79
Turn on : 28.6309
Width : 2.840
Height : 20.058
Entry
ampl
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6
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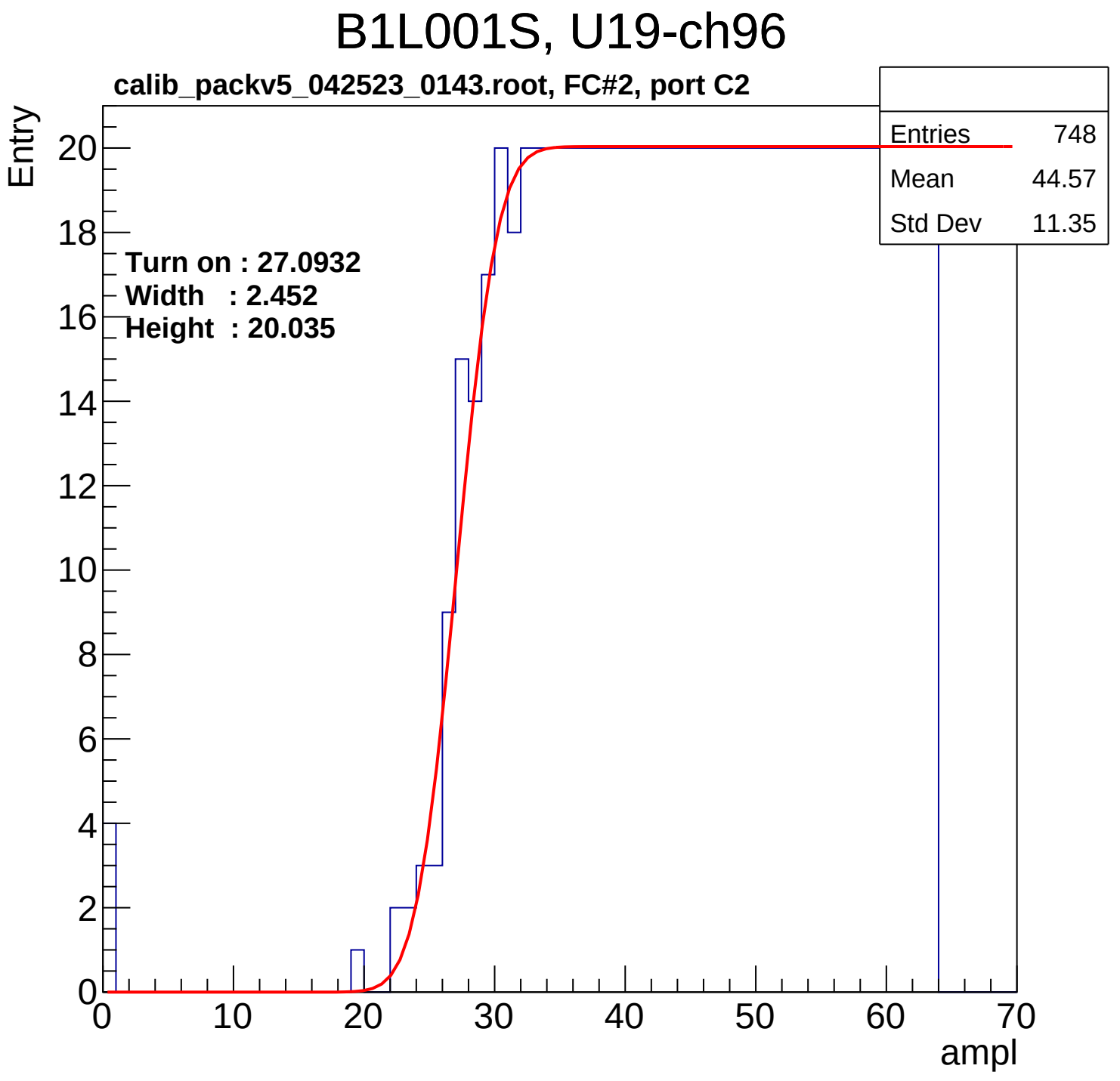
B1L001S, U19-ch96
calib_packv5_042523_0143.root, FC#2, port C2
Entries 748
Mean 44.57
Std Dev 11.35
Turn on : 27.0932
Width : 2.452
Height : 20.035
Entry
ampl
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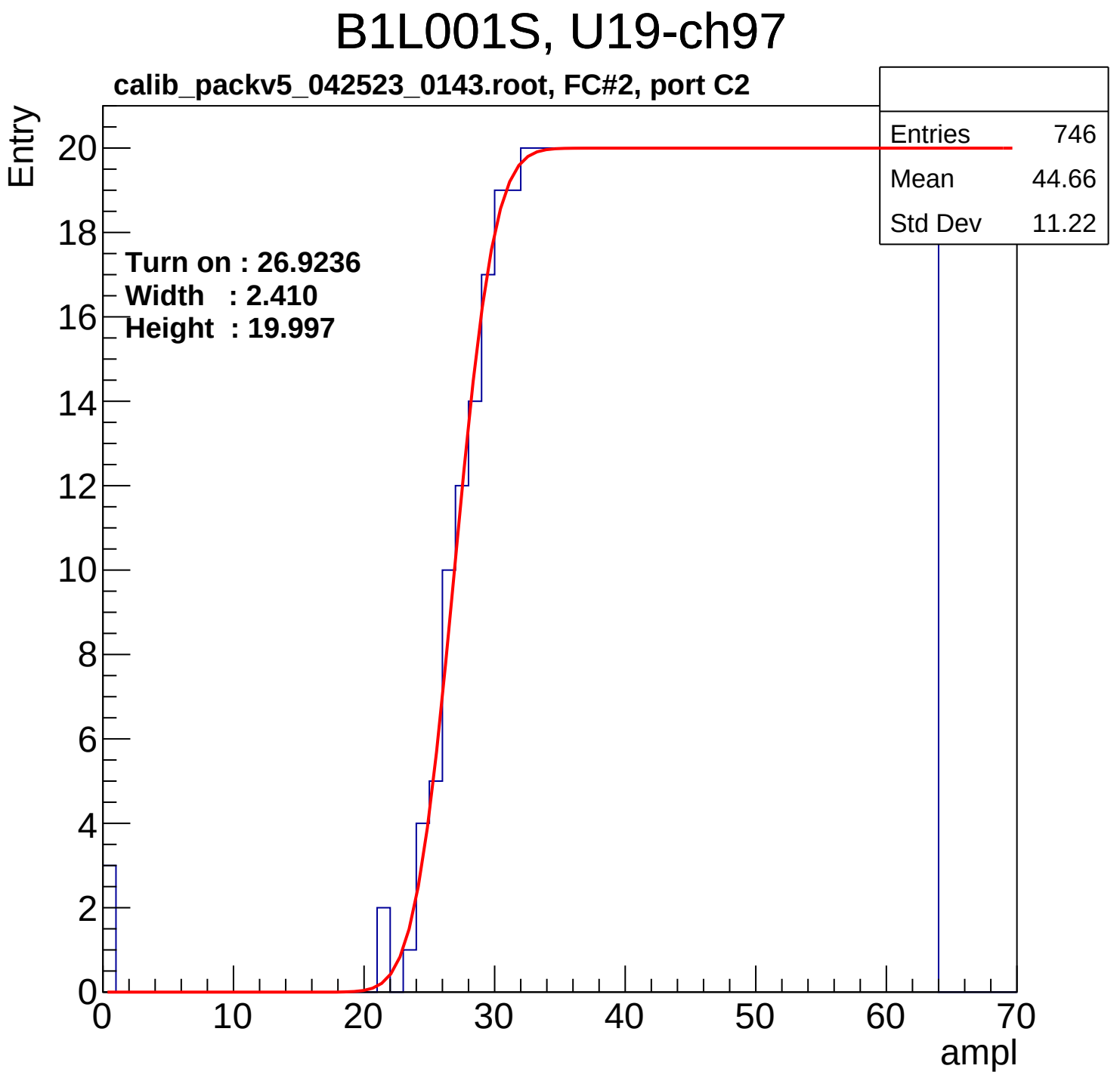
B1L001S, U19-ch97
calib_packv5_042523_0143.root, FC#2, port C2
Entries 746
Mean 44.66
Std Dev 11.22
Turn on : 26.9236
Width : 2.410
Height : 19.997
Entry
ampl
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6
8
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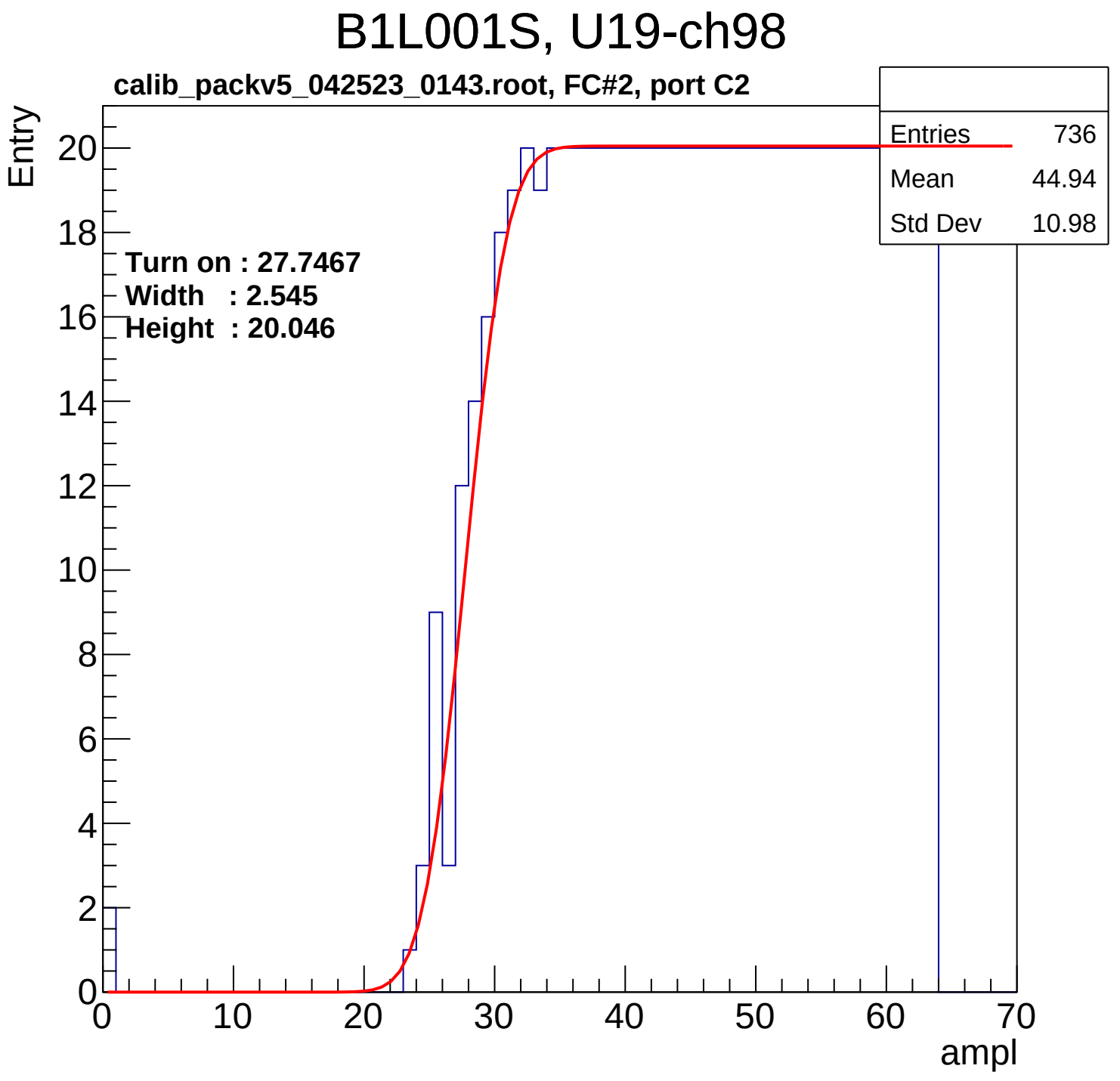
B1L001S, U19-ch98
calib_packv5_042523_0143.root, FC#2, port C2
Entries 736
Mean 44.94
Std Dev 10.98
Turn on : 27.7467
Width : 2.545
Height : 20.046
Entry
ampl
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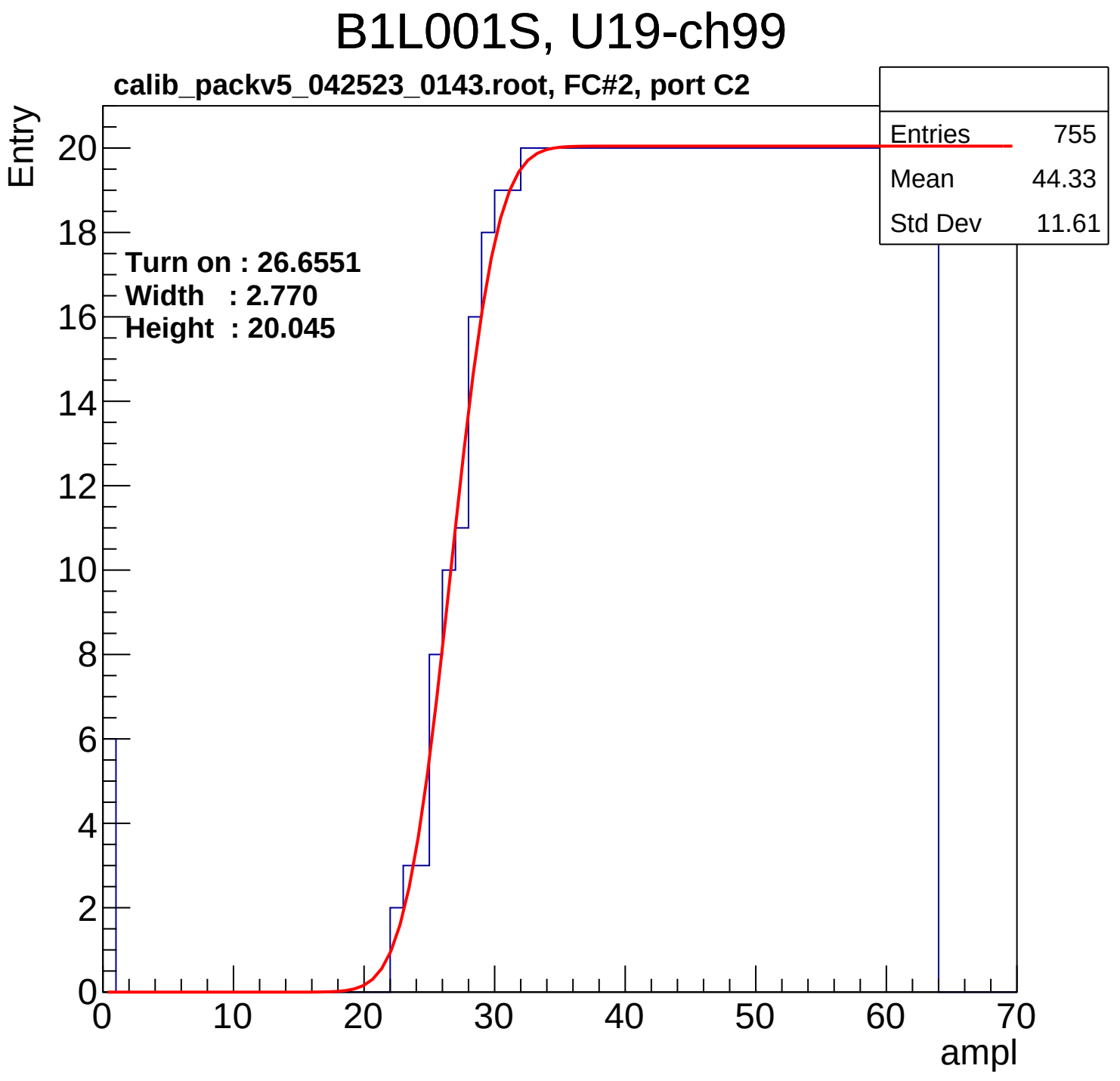
B1L001S, U19-ch99
calib_packv5_042523_0143.root, FC#2, port C2
Entries 755
Mean 44.33
Std Dev 11.61
Turn on : 26.6551
Width : 2.770
Height : 20.045
Entry
ampl
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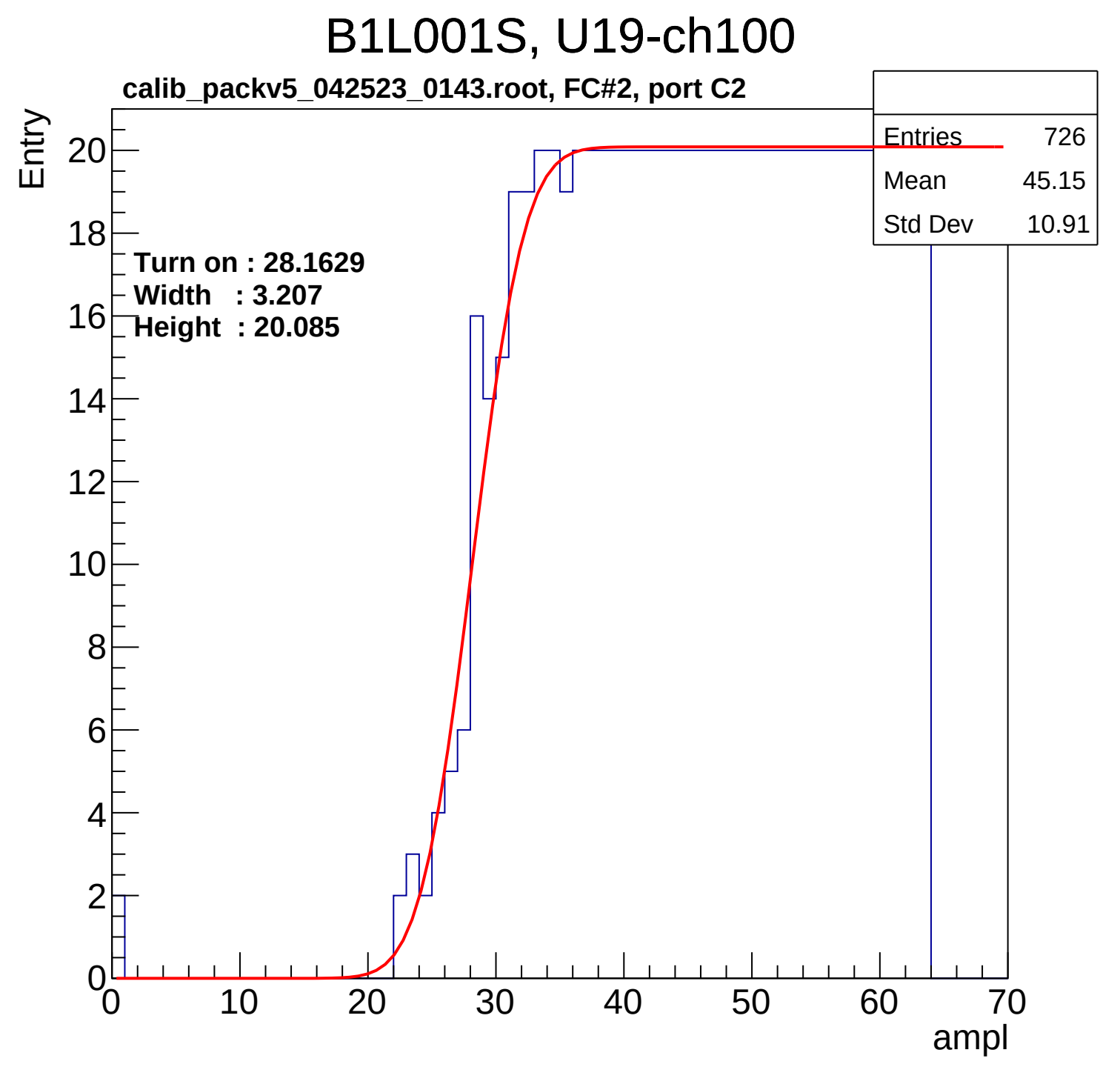
B1L001S, U19-ch100
calib_packv5_042523_0143.root, FC#2, port C2
Entries 726
Mean 45.15
Std Dev 10.91
Turn on : 28.1629
Width : 3.207
Height : 20.085
Entry
ampl
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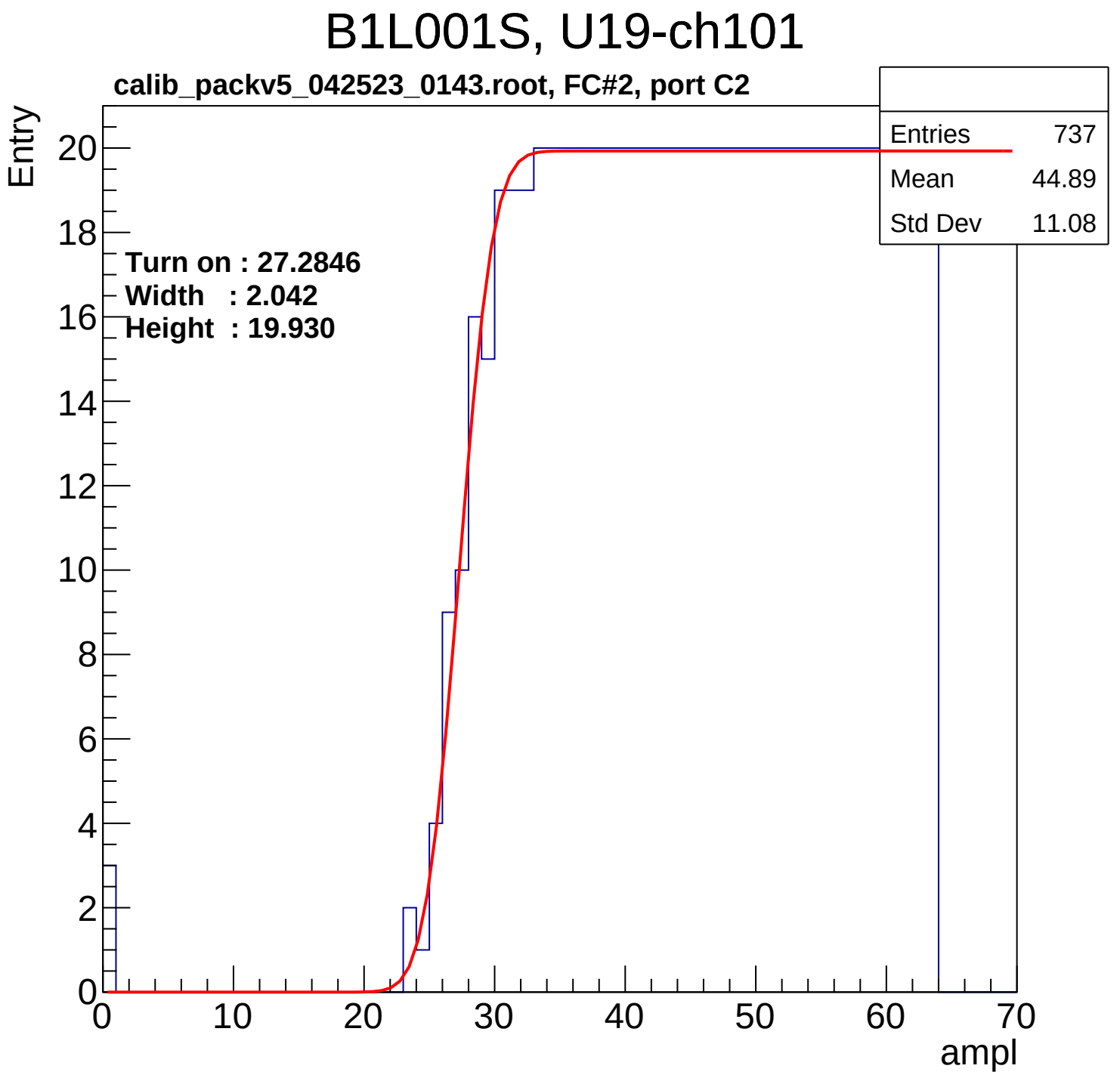
B1L001S, U19-ch101
calib_packv5_042523_0143.root, FC#2, port C2
Entries 737
Mean 44.89
Std Dev 11.08
Turn on : 27.2846
Width : 2.042
Height : 19.930
Entry
ampl
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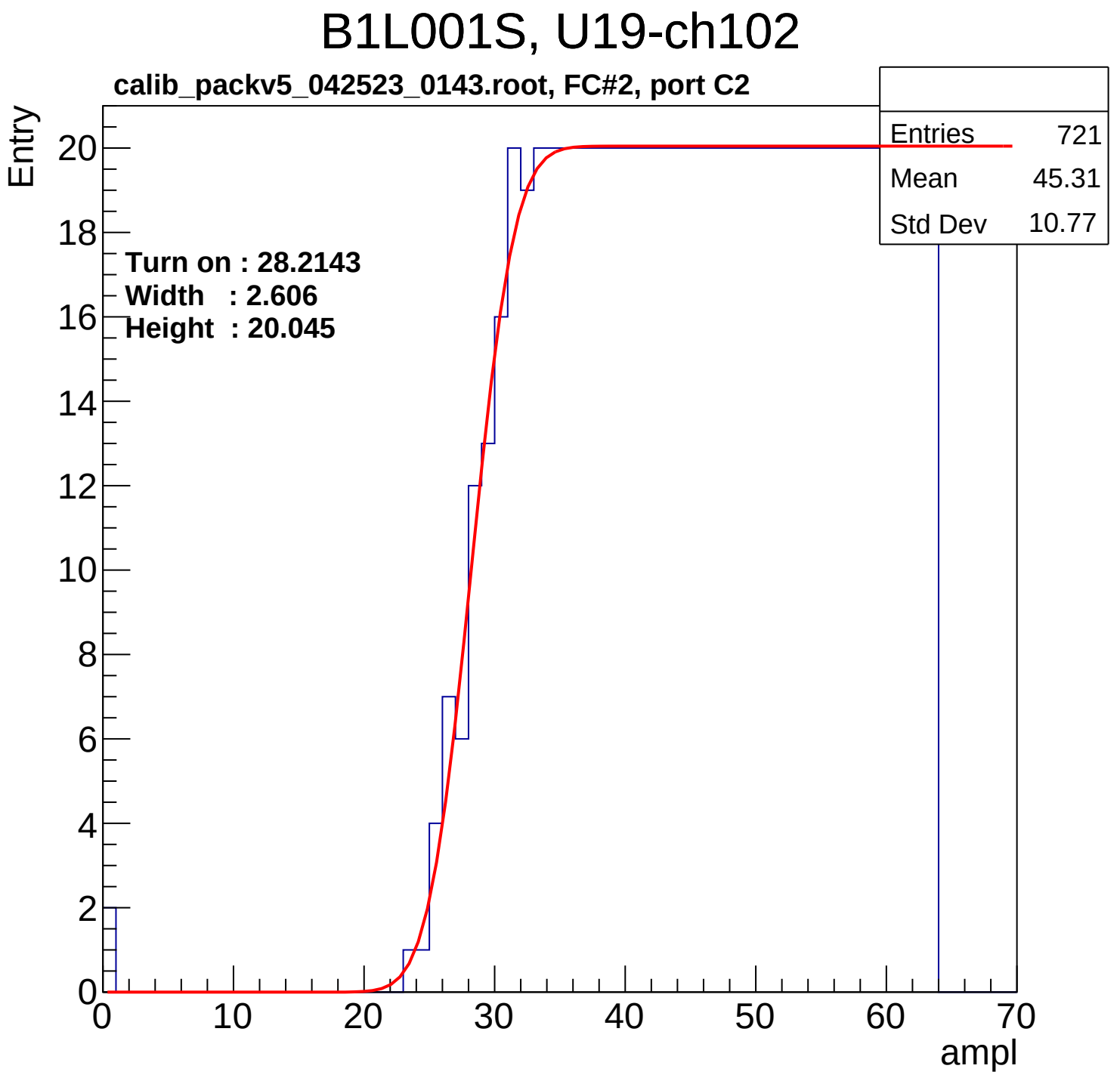
B1L001S, U19-ch102
calib_packv5_042523_0143.root, FC#2, port C2
Entries 721
Mean 45.31
Std Dev 10.77
Turn on : 28.2143
Width : 2.606
Height : 20.045
Entry
ampl
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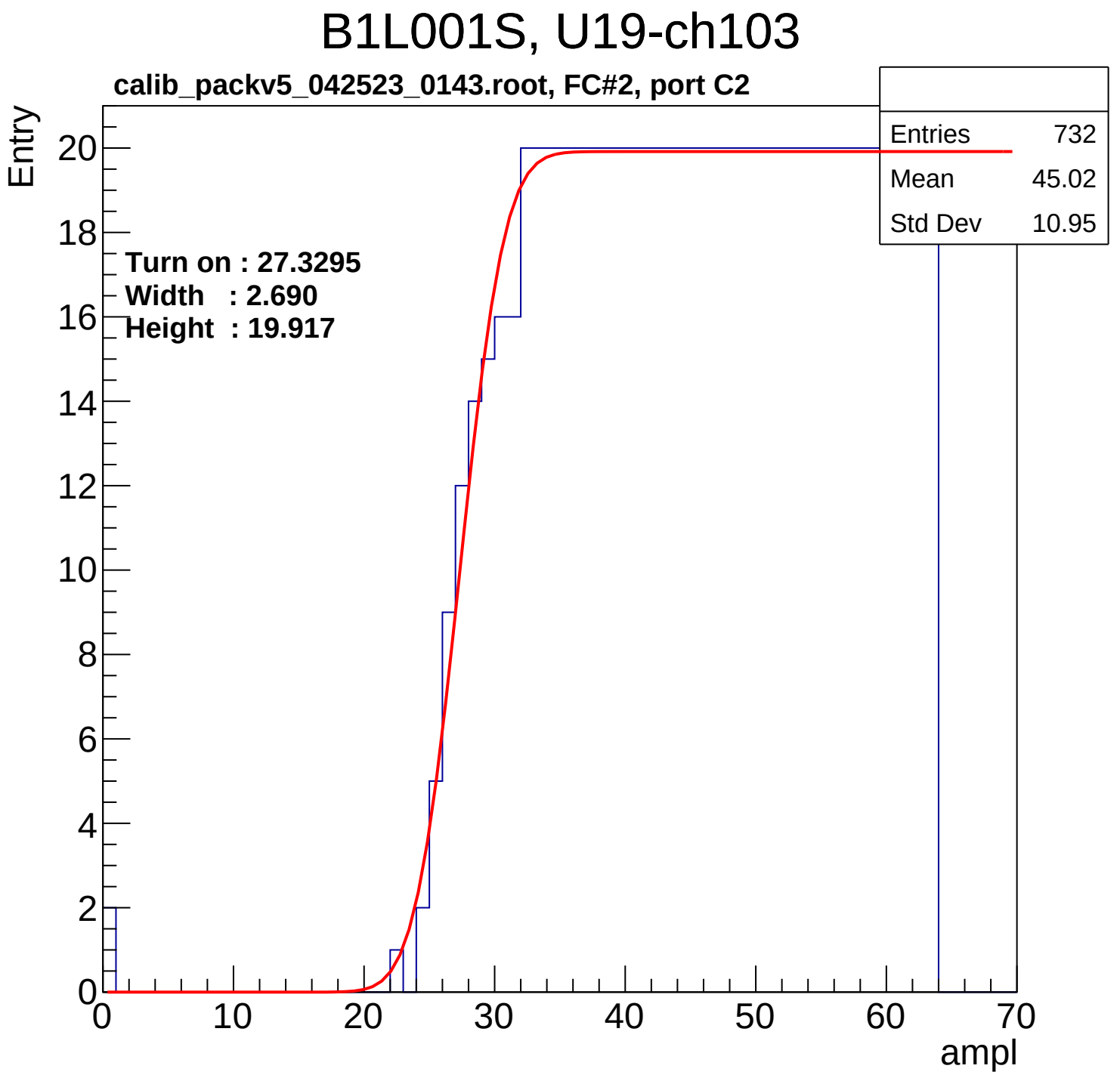
B1L001S, U19-ch103
calib_packv5_042523_0143.root, FC#2, port C2
Entries 732
Mean 45.02
Std Dev 10.95
Turn on : 27.3295
Width : 2.690
Height : 19.917
Entry
ampl
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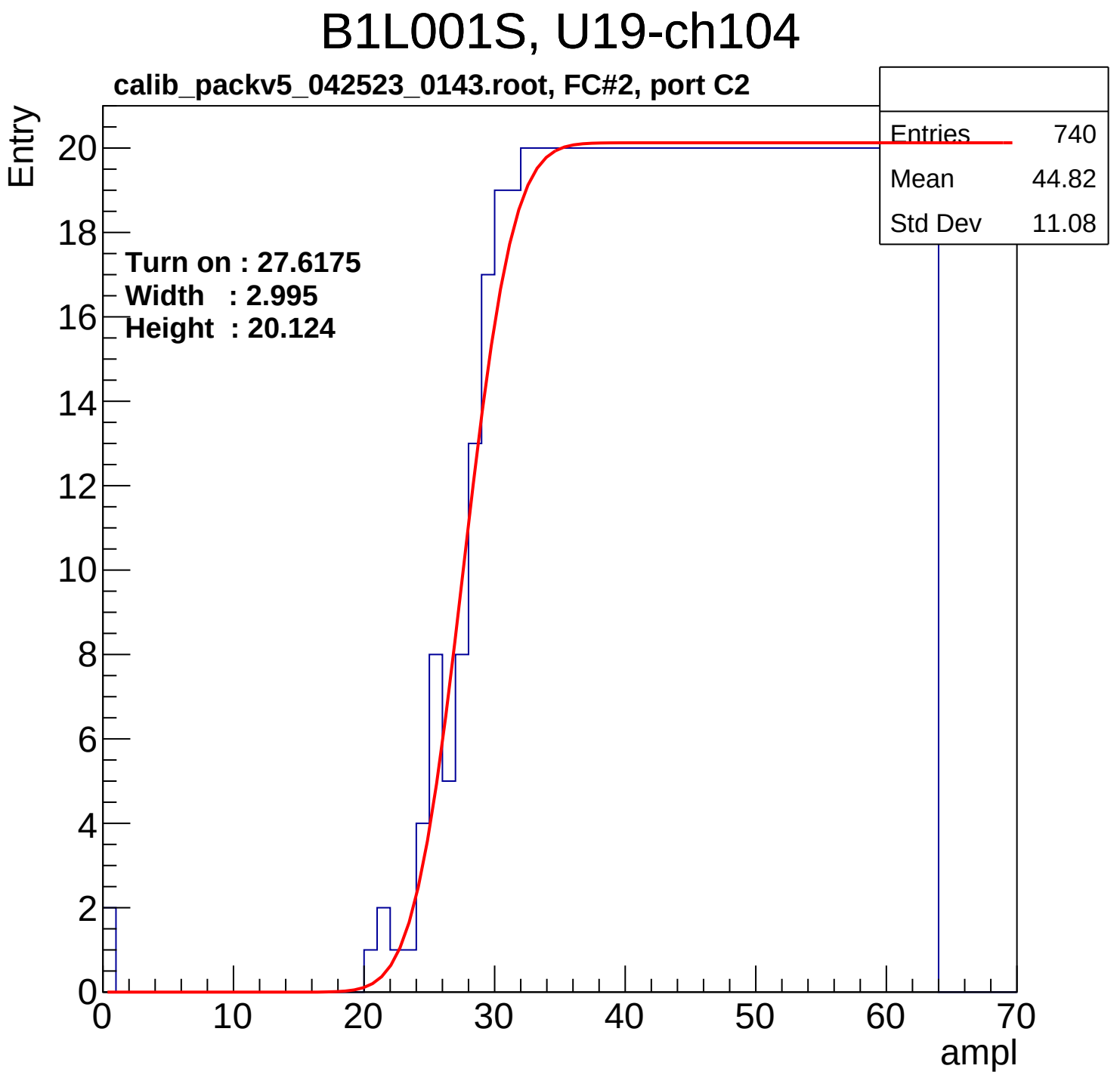
B1L001S, U19-ch104
calib_packv5_042523_0143.root, FC#2, port C2
Entries 740
Mean 44.82
Std Dev 11.08
Turn on : 27.6175
Width : 2.995
Height : 20.124
Entry
ampl
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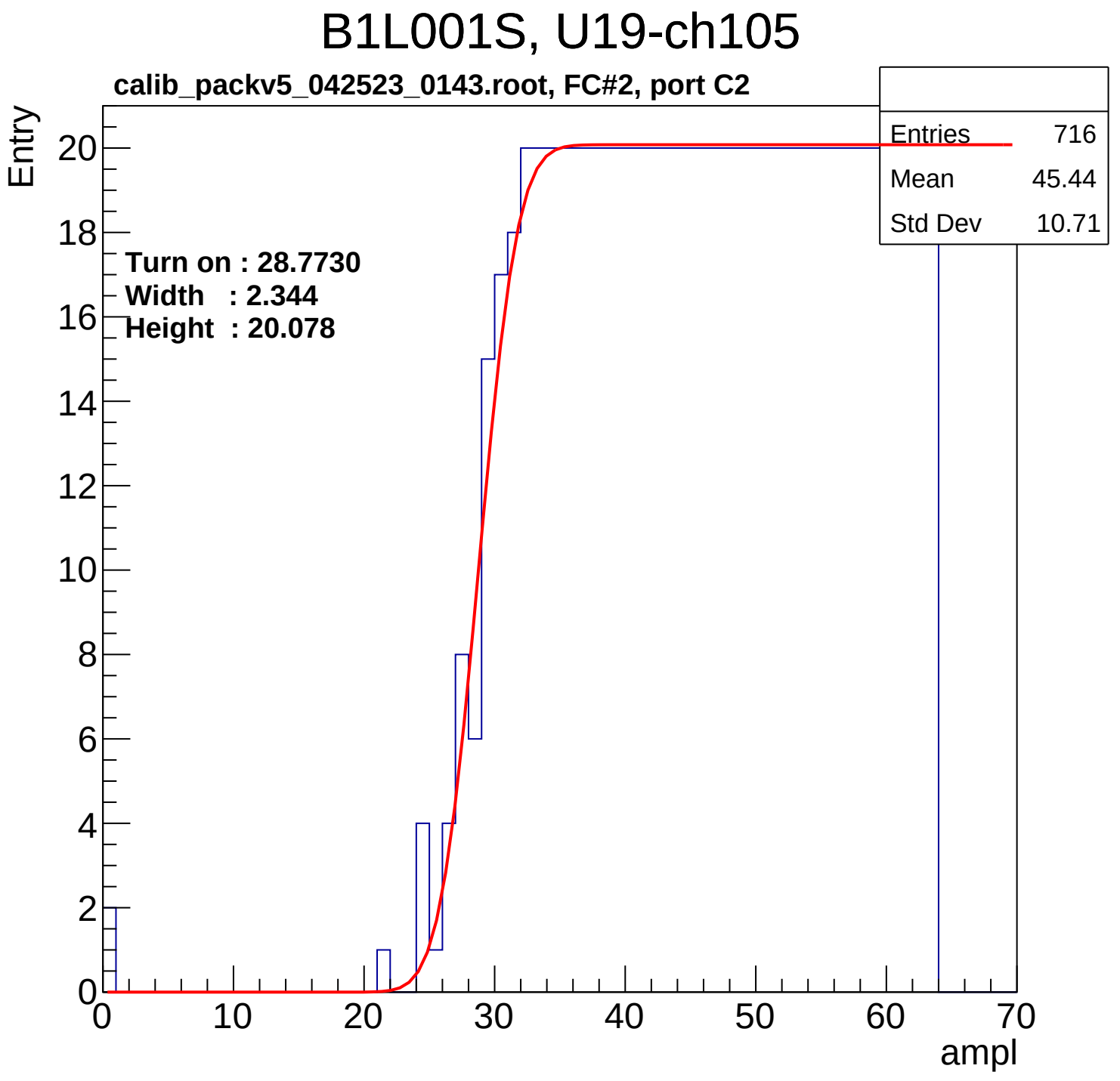
B1L001S, U19-ch105
calib_packv5_042523_0143.root, FC#2, port C2
Entries 716
Mean 45.44
Std Dev 10.71
Turn on : 28.7730
Width : 2.344
Height : 20.078
Entry
ampl
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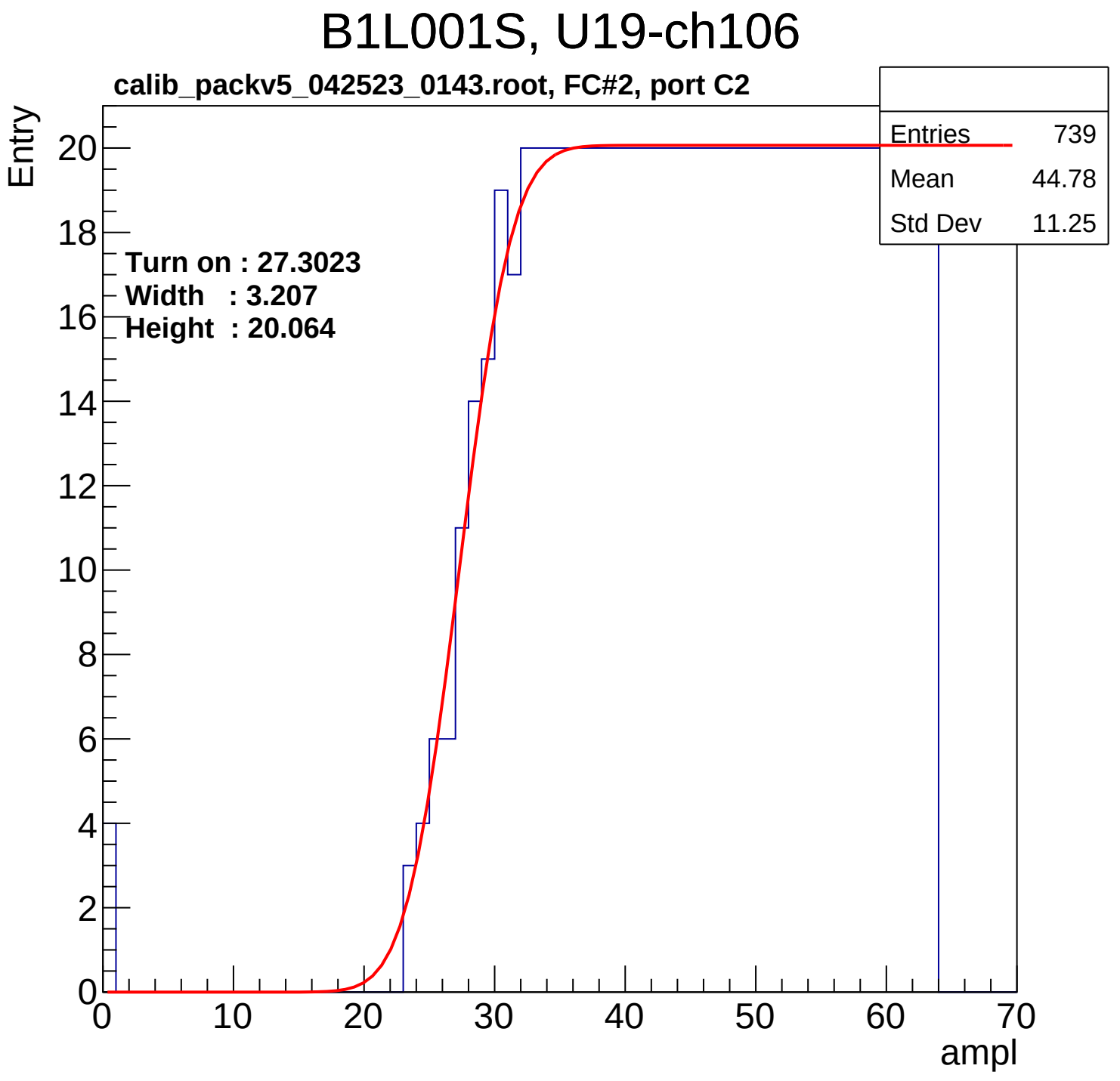
B1L001S, U19-ch106
calib_packv5_042523_0143.root, FC#2, port C2
Entries 739
Mean 44.78
Std Dev 11.25
Turn on : 27.3023
Width : 3.207
Height : 20.064
Entry
ampl
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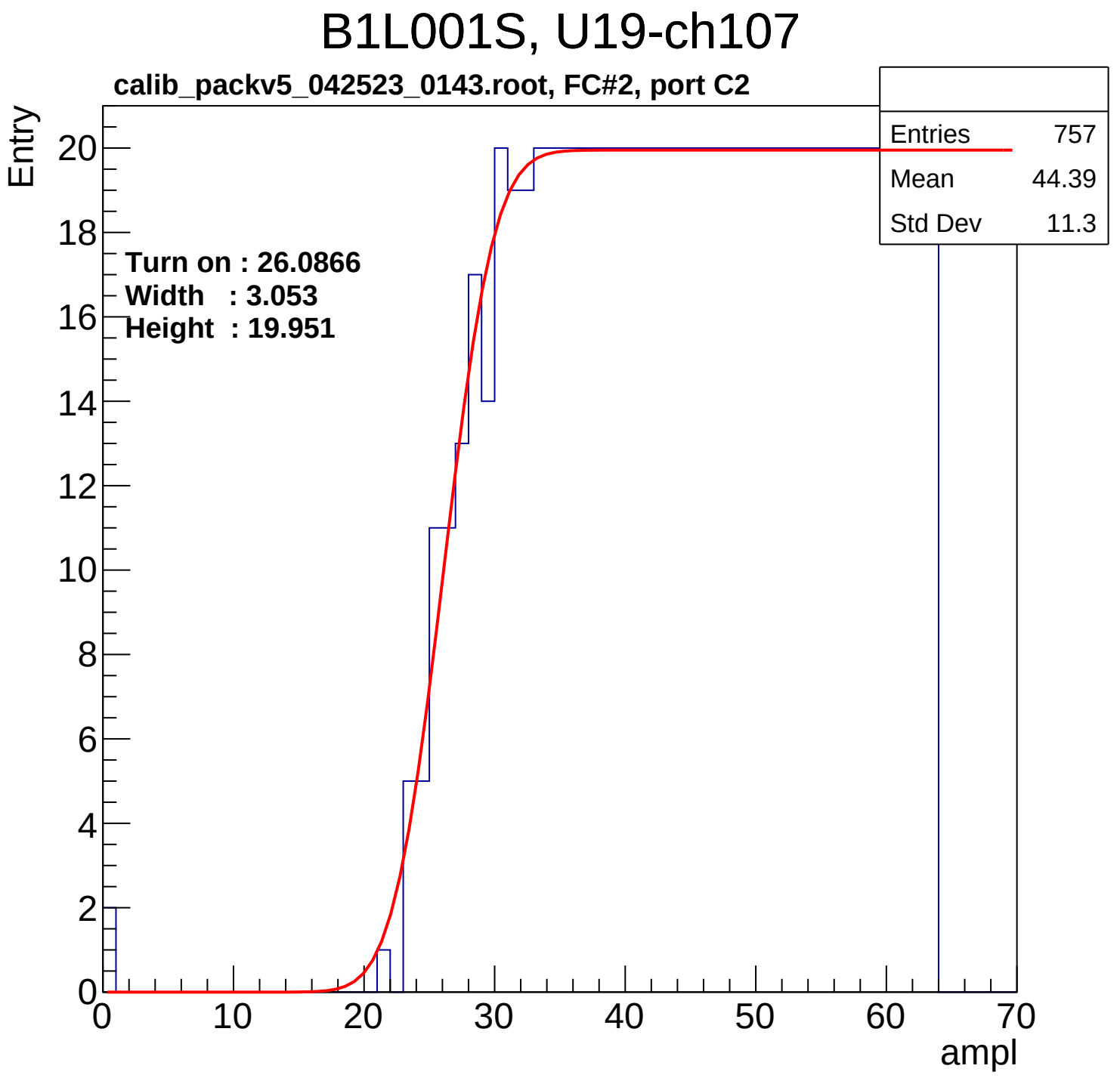
B1L001S, U19-ch107
calib_packv5_042523_0143.root, FC#2, port C2
Entries 757
Mean 44.39
Std Dev 11.3
Turn on : 26.0866
Width : 3.053
Height : 19.951
Entry
ampl
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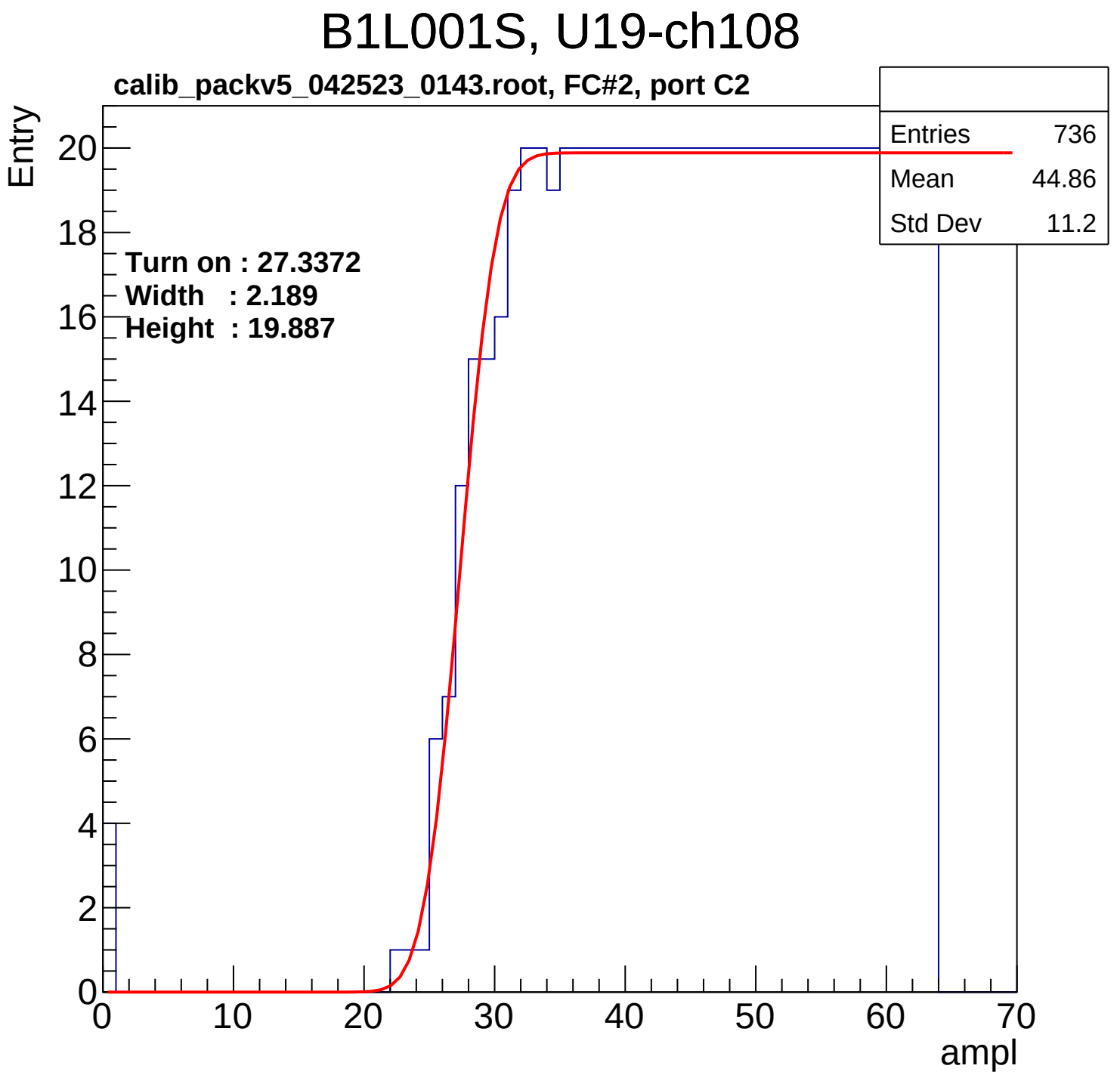
B1L001S, U19-ch108
calib_packv5_042523_0143.root, FC#2, port C2
Entries 736
Mean 44.86
Std Dev 11.2
Turn on : 27.3372
Width : 2.189
Height : 19.887
Entry
ampl
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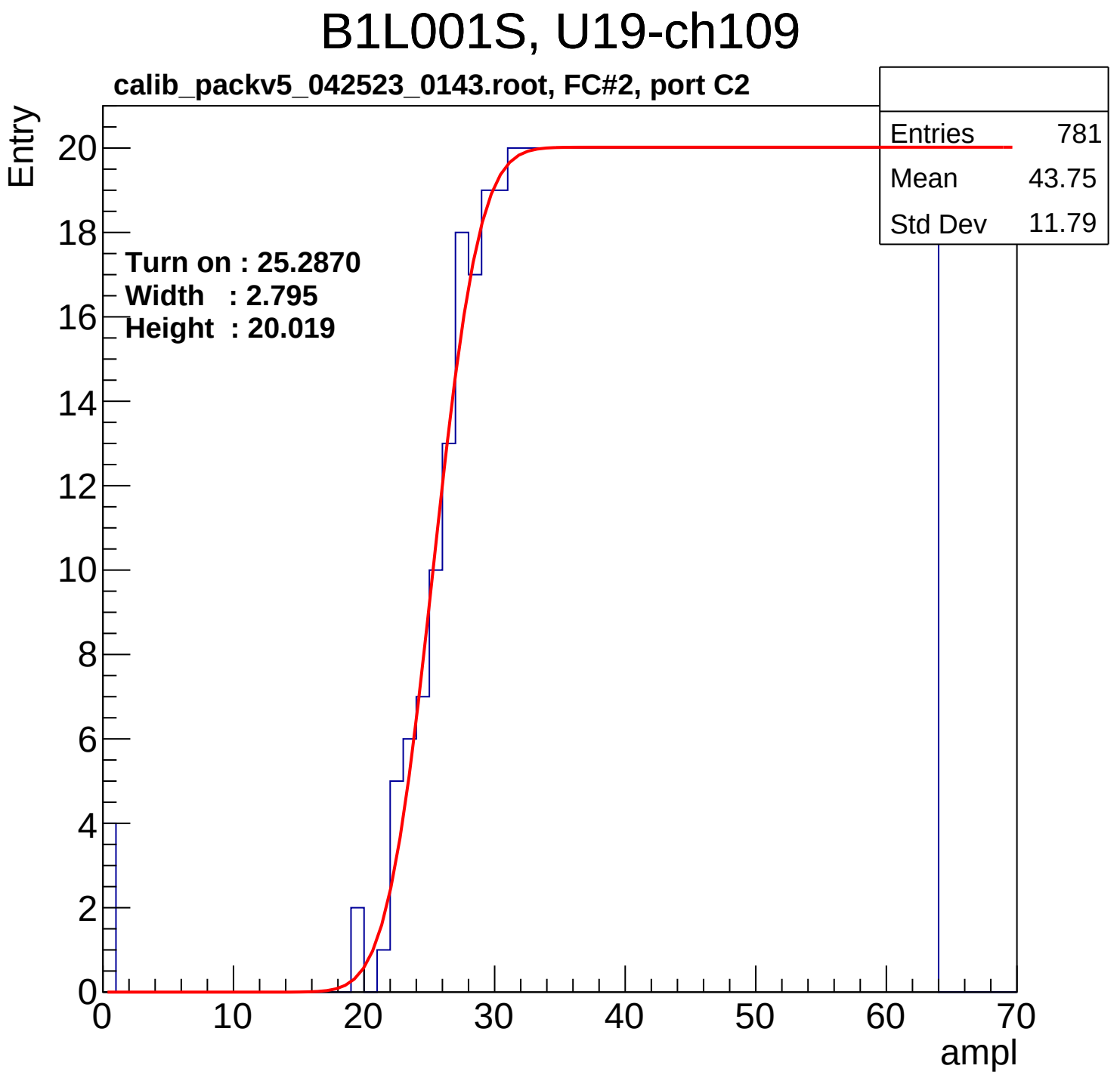
B1L001S, U19-ch109
calib_packv5_042523_0143.root, FC#2, port C2
Entries 781
Mean 43.75
Std Dev 11.79
Turn on : 25.2870
Width : 2.795
Height : 20.019
Entry
ampl
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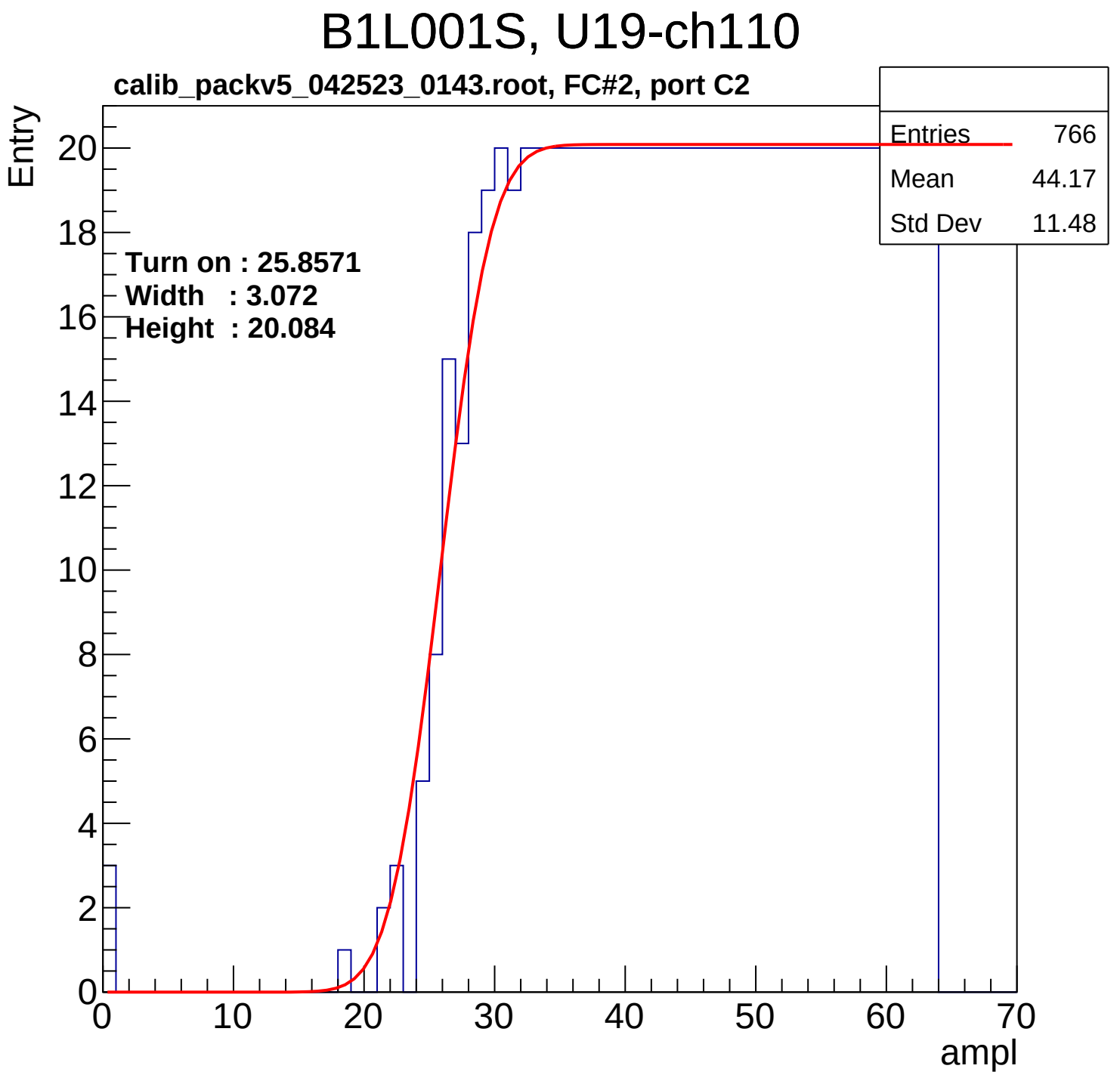
B1L001S, U19-ch110
calib_packv5_042523_0143.root, FC#2, port C2
Entries 766
Mean 44.17
Std Dev 11.48
Turn on : 25.8571
Width : 3.072
Height : 20.084
Entry
ampl
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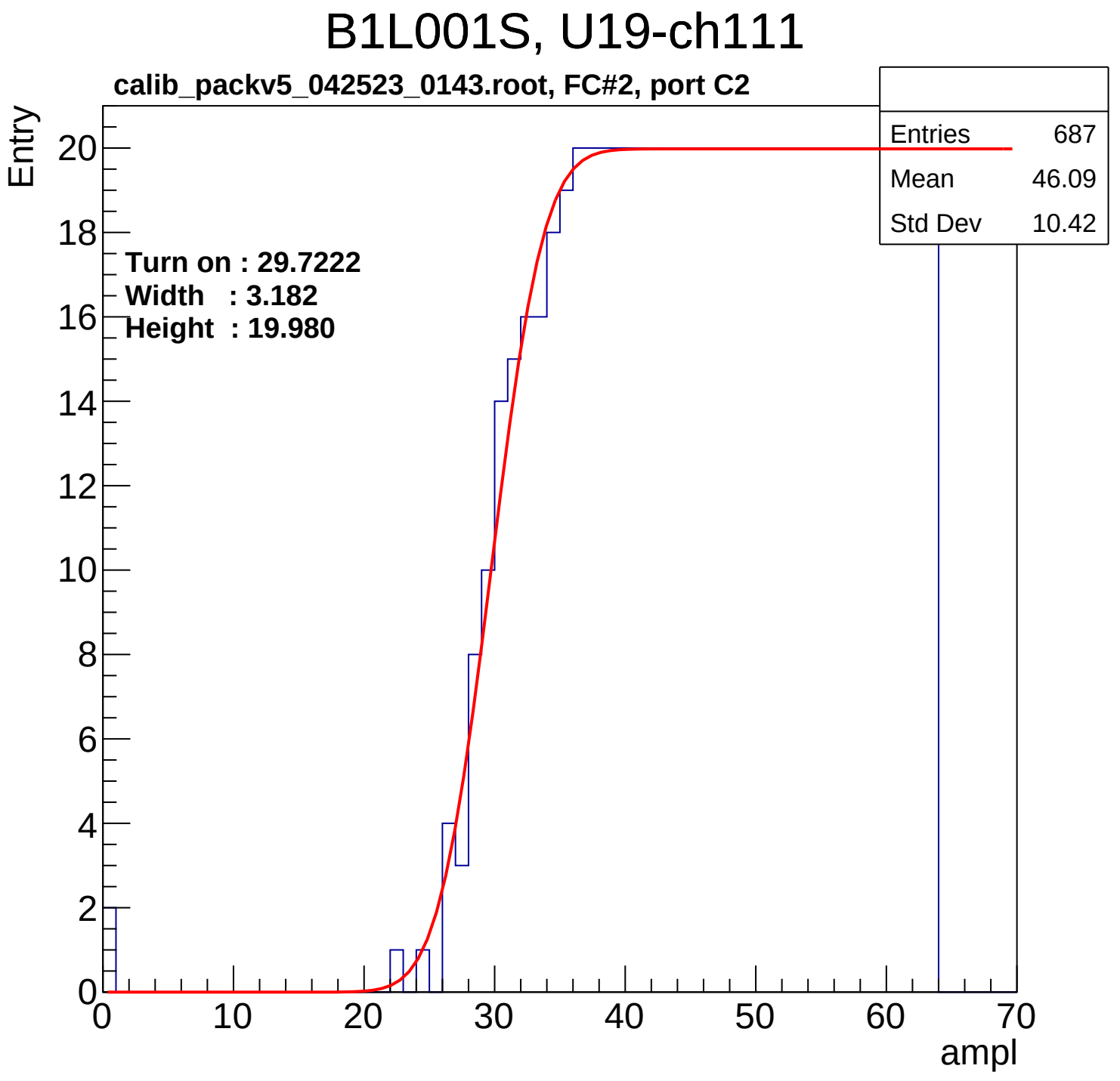
B1L001S, U19-ch111
calib_packv5_042523_0143.root, FC#2, port C2
Entries 687
Mean 46.09
Std Dev 10.42
Turn on : 29.7222
Width : 3.182
Height : 19.980
Entry
ampl
0
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6
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18
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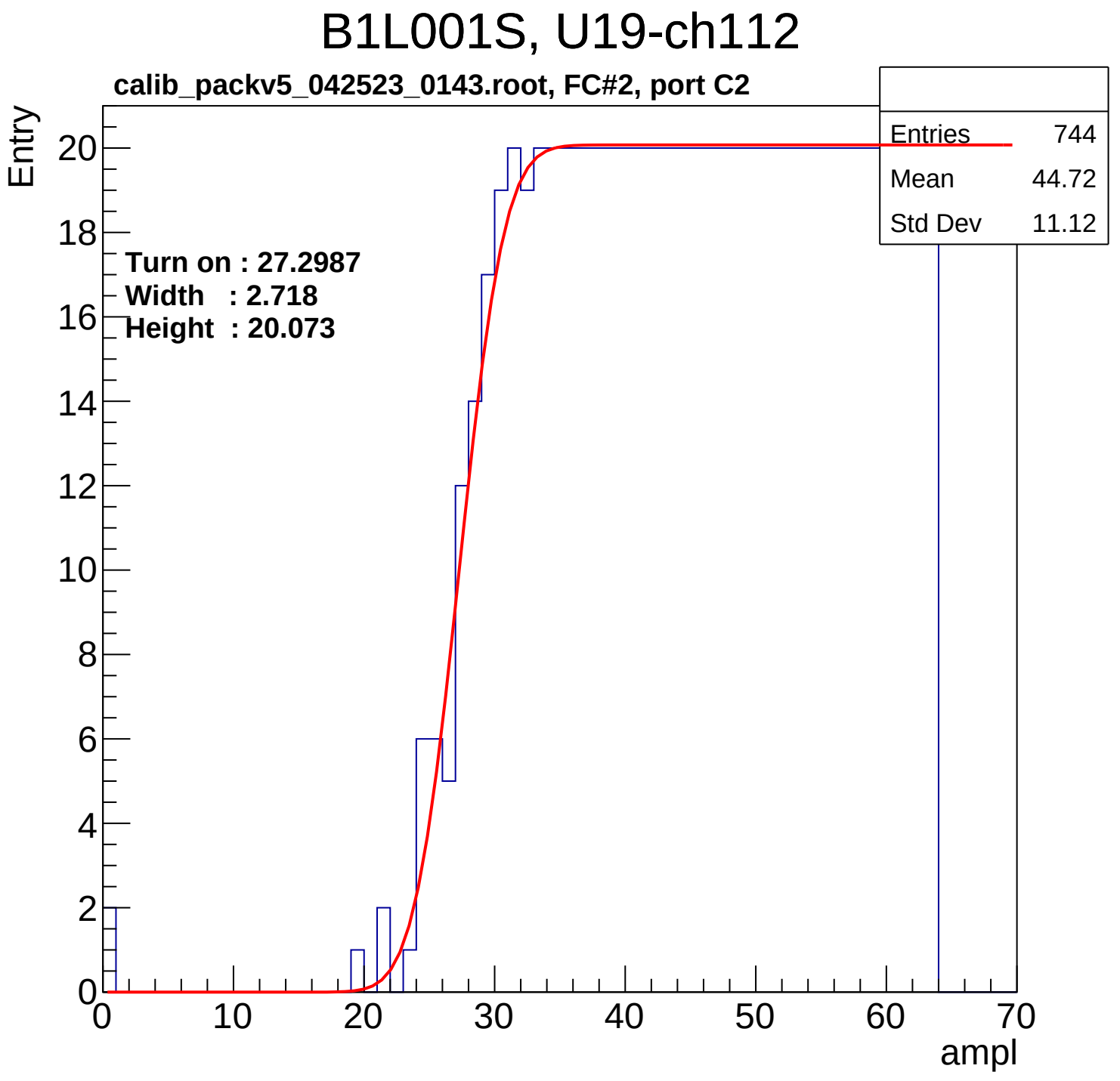
B1L001S, U19-ch112
calib_packv5_042523_0143.root, FC#2, port C2
Entries 744
Mean 44.72
Std Dev 11.12
Turn on : 27.2987
Width : 2.718
Height : 20.073
Entry
ampl
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6
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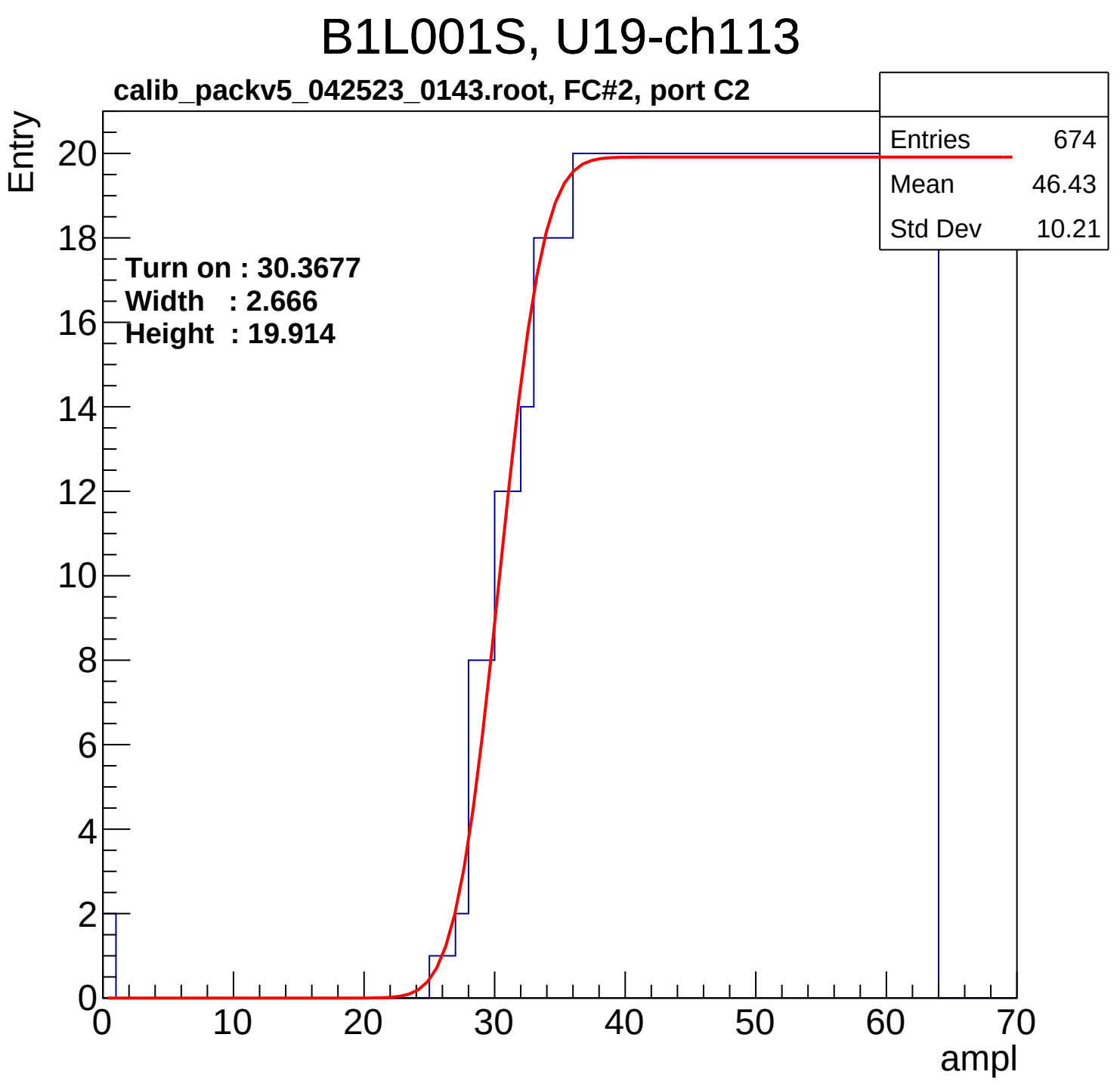
B1L001S, U19-ch113
calib_packv5_042523_0143.root, FC#2, port C2
Entries 674
Mean 46.43
Std Dev 10.21
Turn on : 30.3677
Width : 2.666
Height : 19.914
Entry
ampl
0
2
4
6
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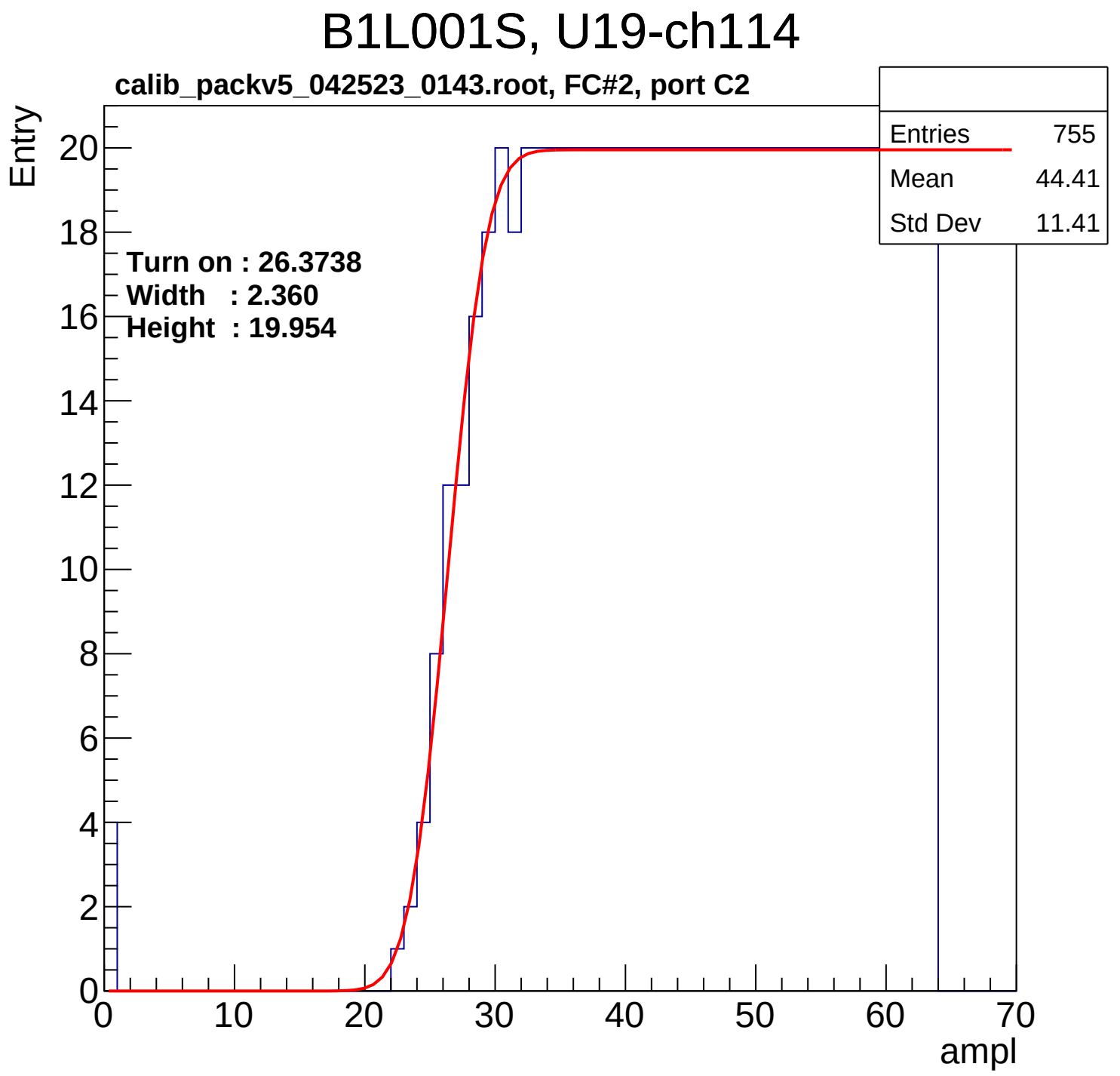
B1L001S, U19-ch114
calib_packv5_042523_0143.root, FC#2, port C2
Entries 755
Mean 44.41
Std Dev 11.41
Turn on : 26.3738
Width : 2.360
Height : 19.954
Entry
ampl
0
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4
6
8
10
12
14
16
18
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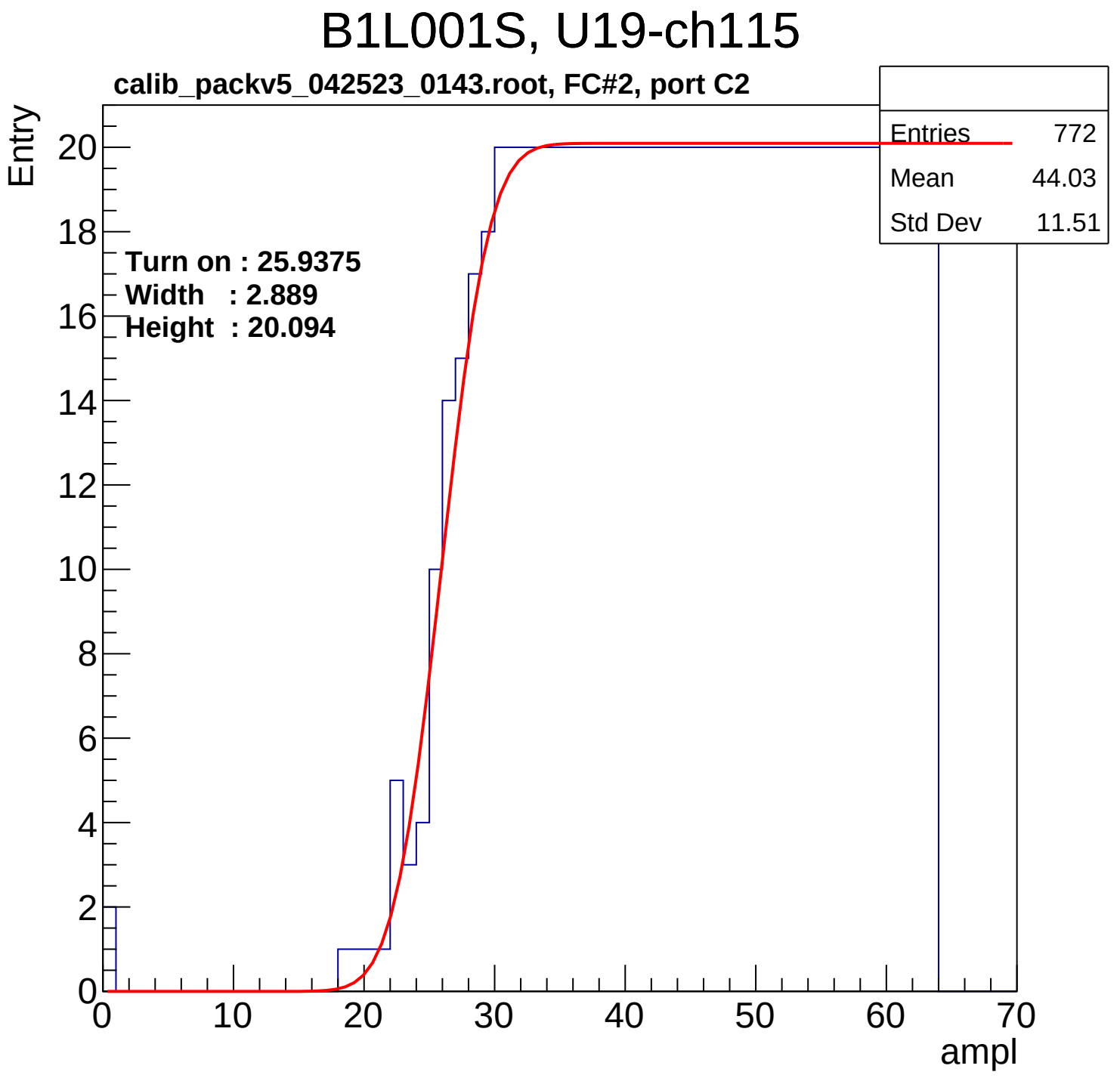
B1L001S, U19-ch115
calib_packv5_042523_0143.root, FC#2, port C2
Entries 772
Mean 44.03
Std Dev 11.51
Turn on : 25.9375
Width : 2.889
Height : 20.094
Entry
ampl
0
2
4
6
8
10
12
14
16
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0
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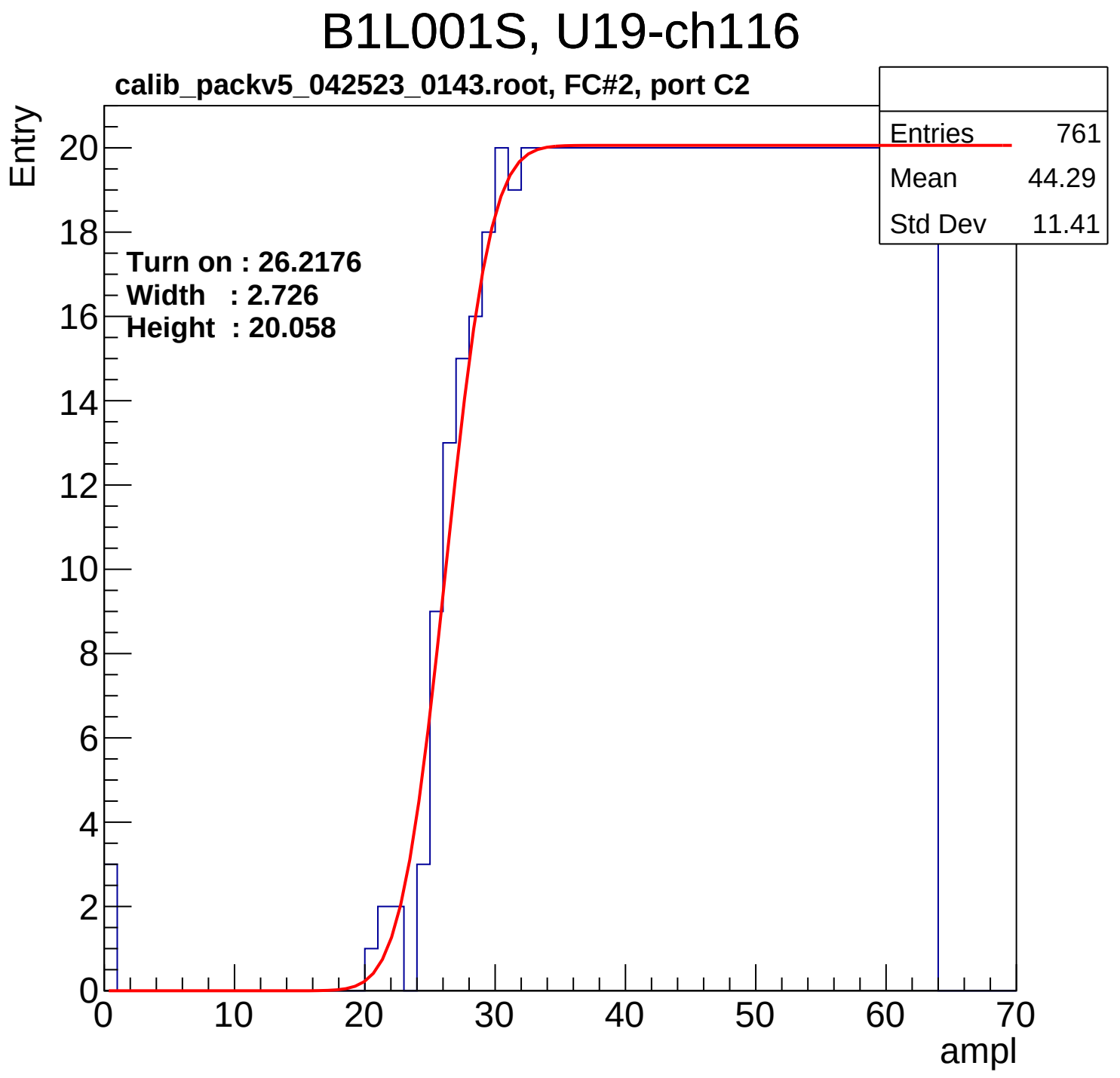
B1L001S, U19-ch116
calib_packv5_042523_0143.root, FC#2, port C2
Entries 761
Mean 44.29
Std Dev 11.41
Turn on : 26.2176
Width : 2.726
Height : 20.058
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
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20
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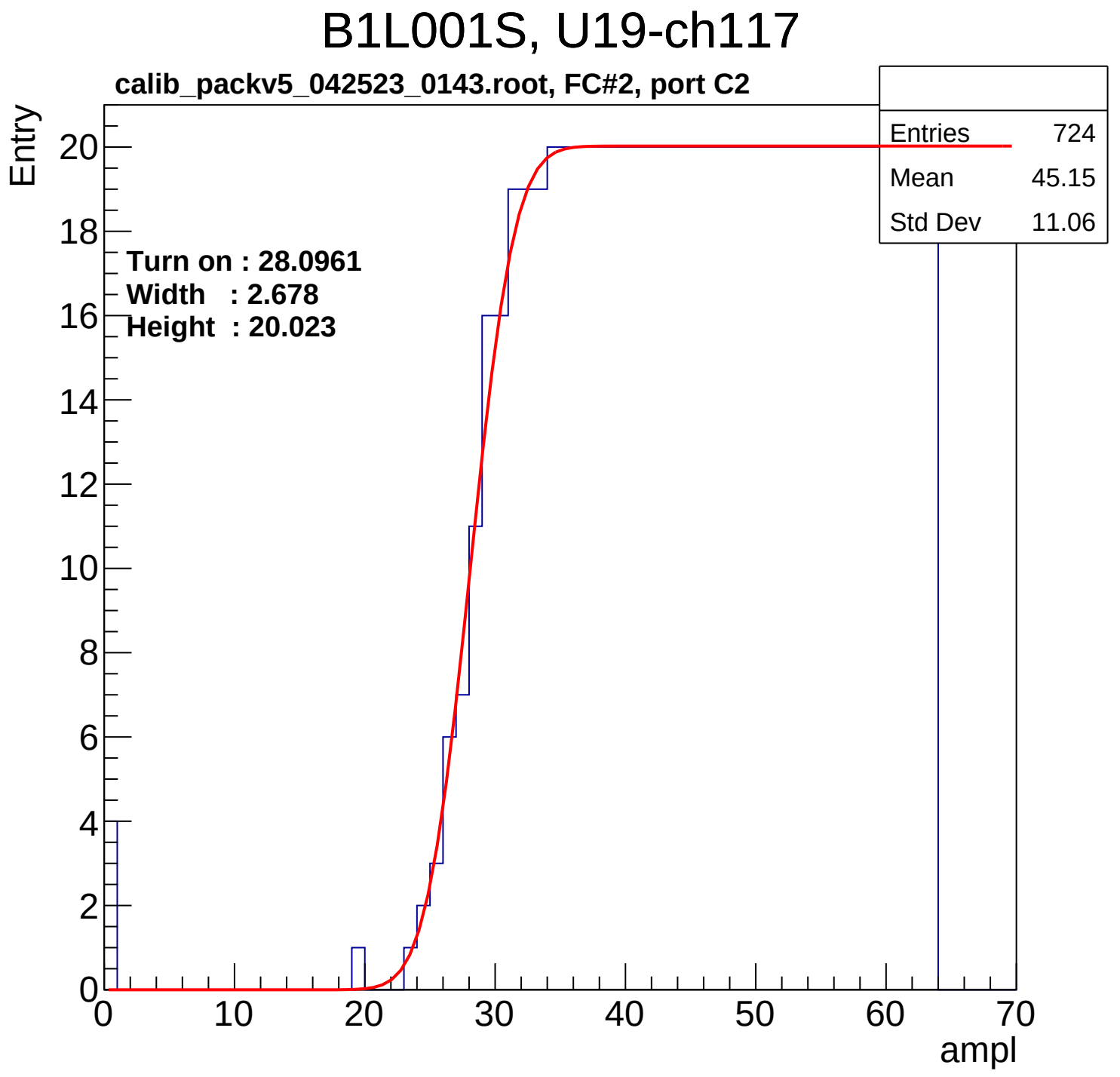
B1L001S, U19-ch117
calib_packv5_042523_0143.root, FC#2, port C2
Entries 724
Mean 45.15
Std Dev 11.06
Turn on : 28.0961
Width : 2.678
Height : 20.023
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
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20
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60
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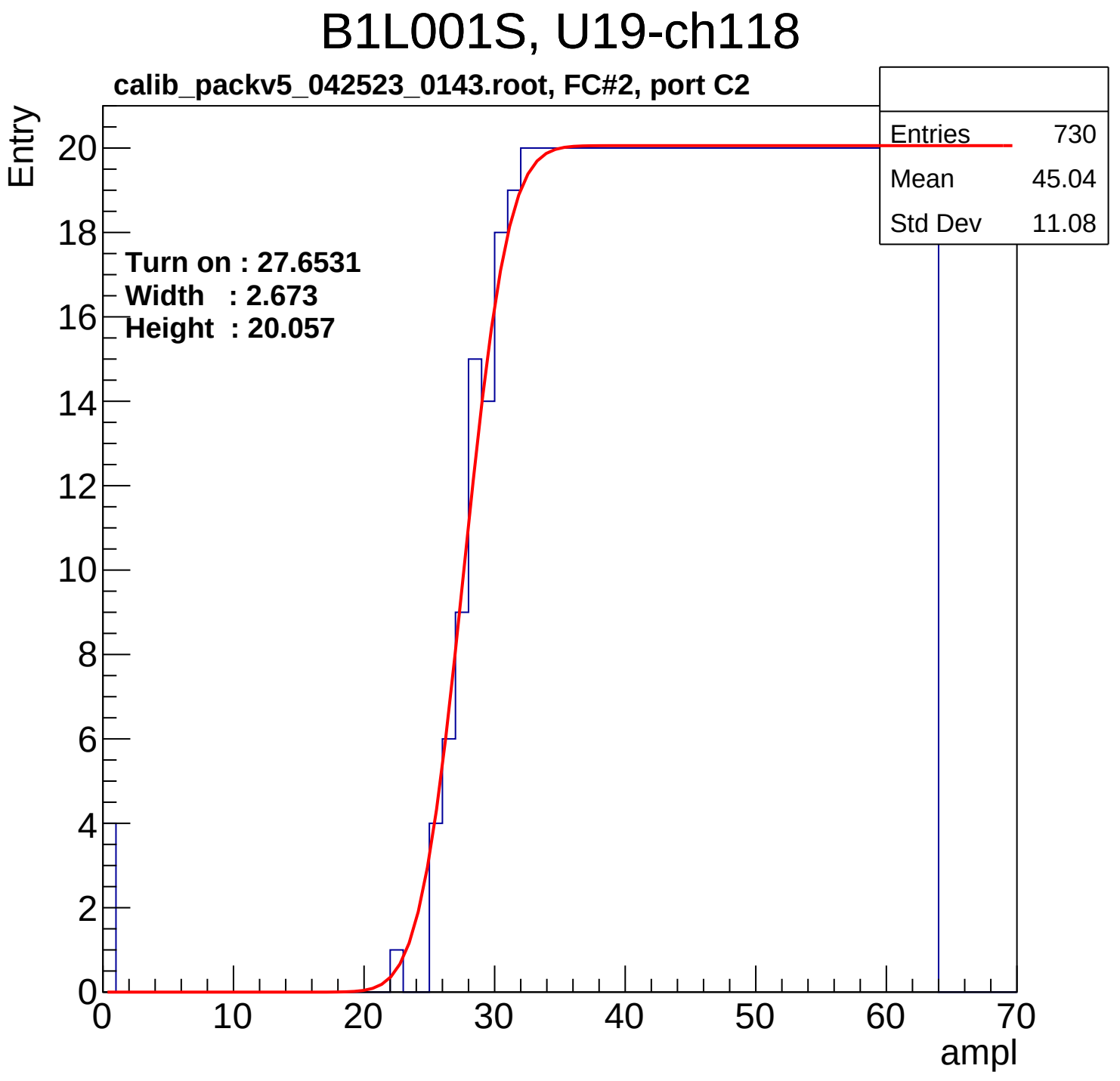
B1L001S, U19-ch118
calib_packv5_042523_0143.root, FC#2, port C2
Entries 730
Mean 45.04
Std Dev 11.08
Turn on : 27.6531
Width : 2.673
Height : 20.057
Entry
ampl
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8
10
12
14
16
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0
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60
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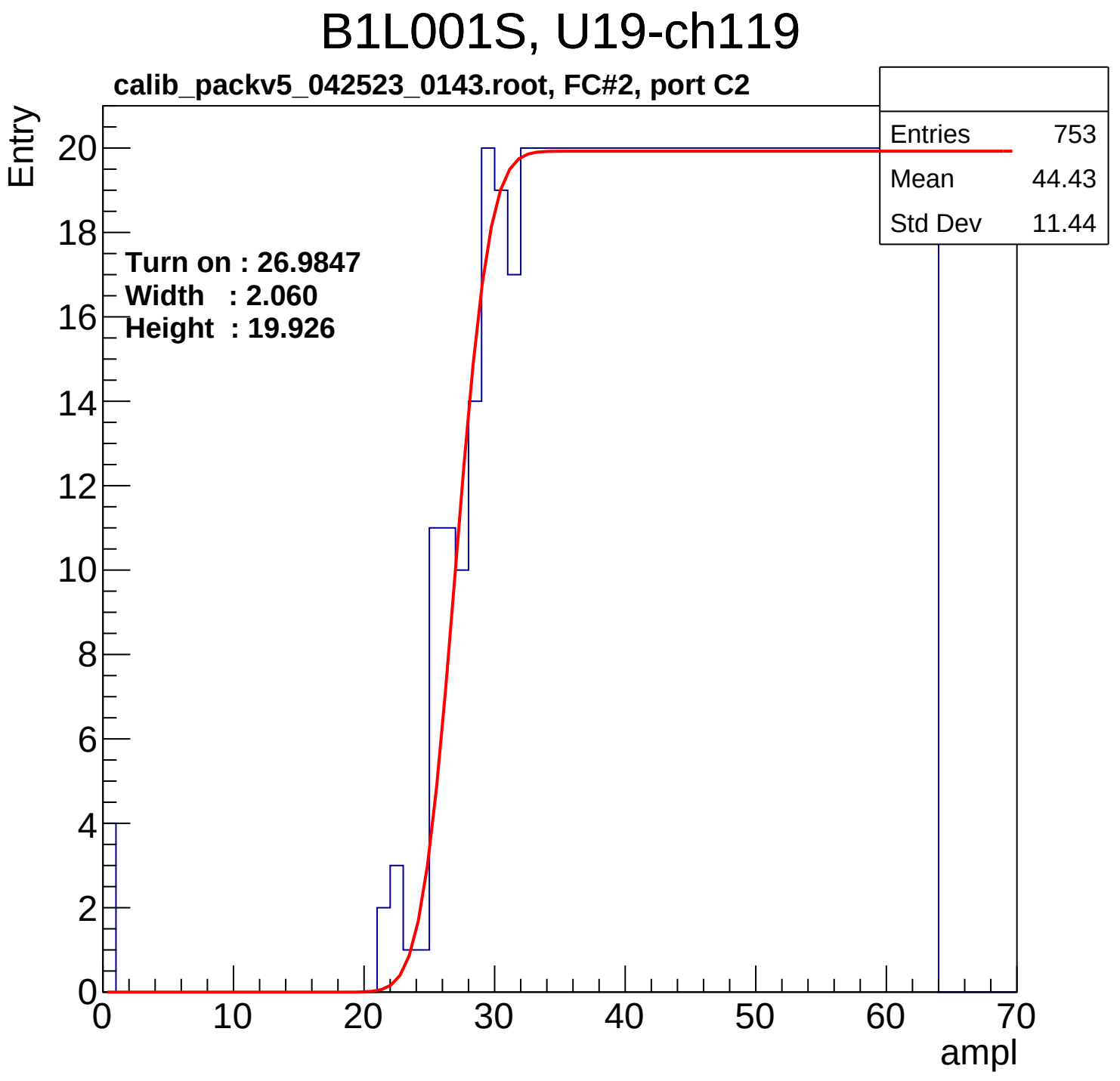
B1L001S, U19-ch119
calib_packv5_042523_0143.root, FC#2, port C2
Entries 753
Mean 44.43
Std Dev 11.44
Turn on : 26.9847
Width : 2.060
Height : 19.926
Entry
ampl
0
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4
6
8
10
12
14
16
18
20
0
10
20
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40
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60
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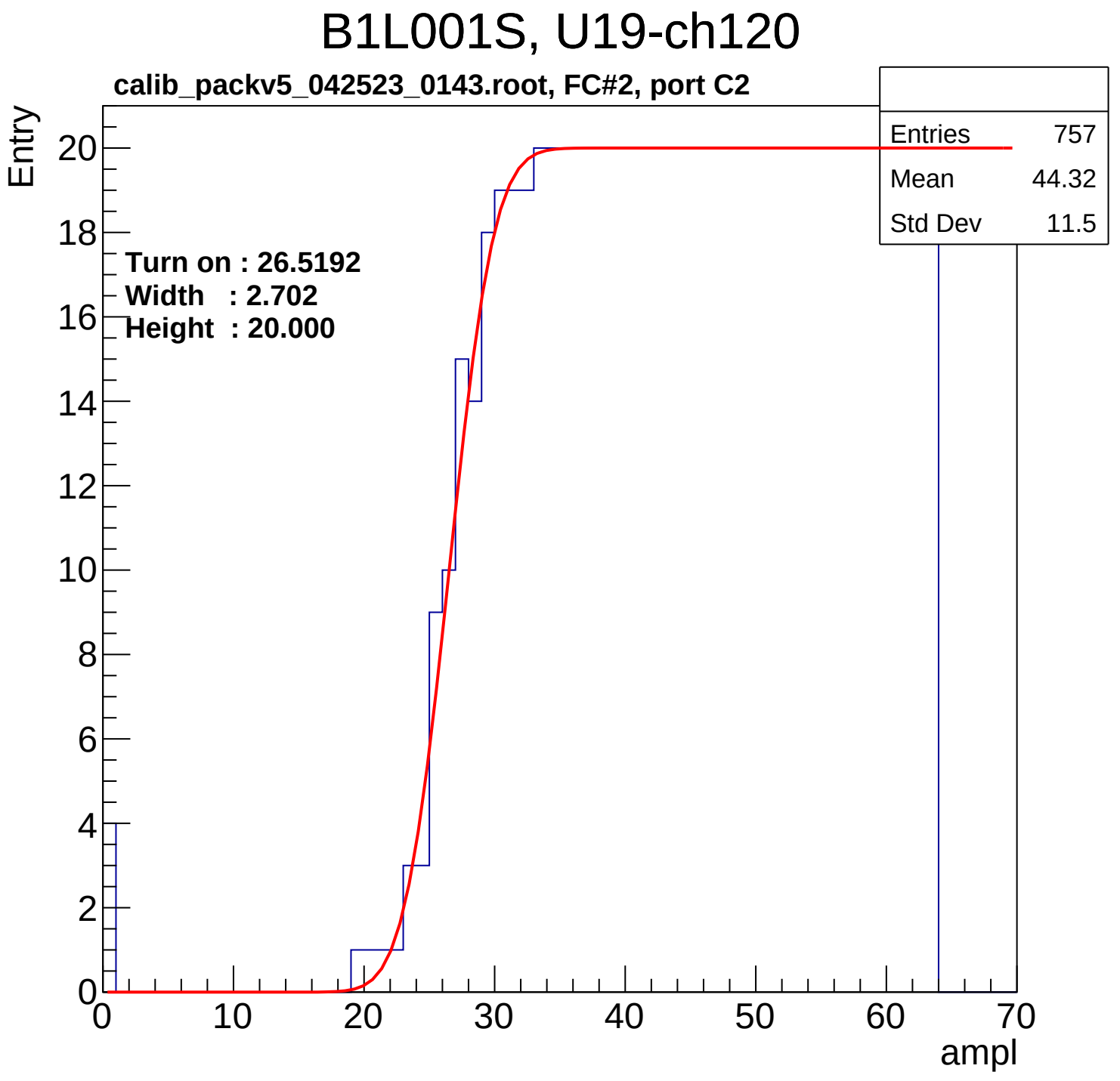
B1L001S, U19-ch120
calib_packv5_042523_0143.root, FC#2, port C2
Entries 757
Mean 44.32
Std Dev 11.5
Turn on : 26.5192
Width : 2.702
Height : 20.000
Entry
ampl
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6
8
10
12
14
16
18
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0
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20
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40
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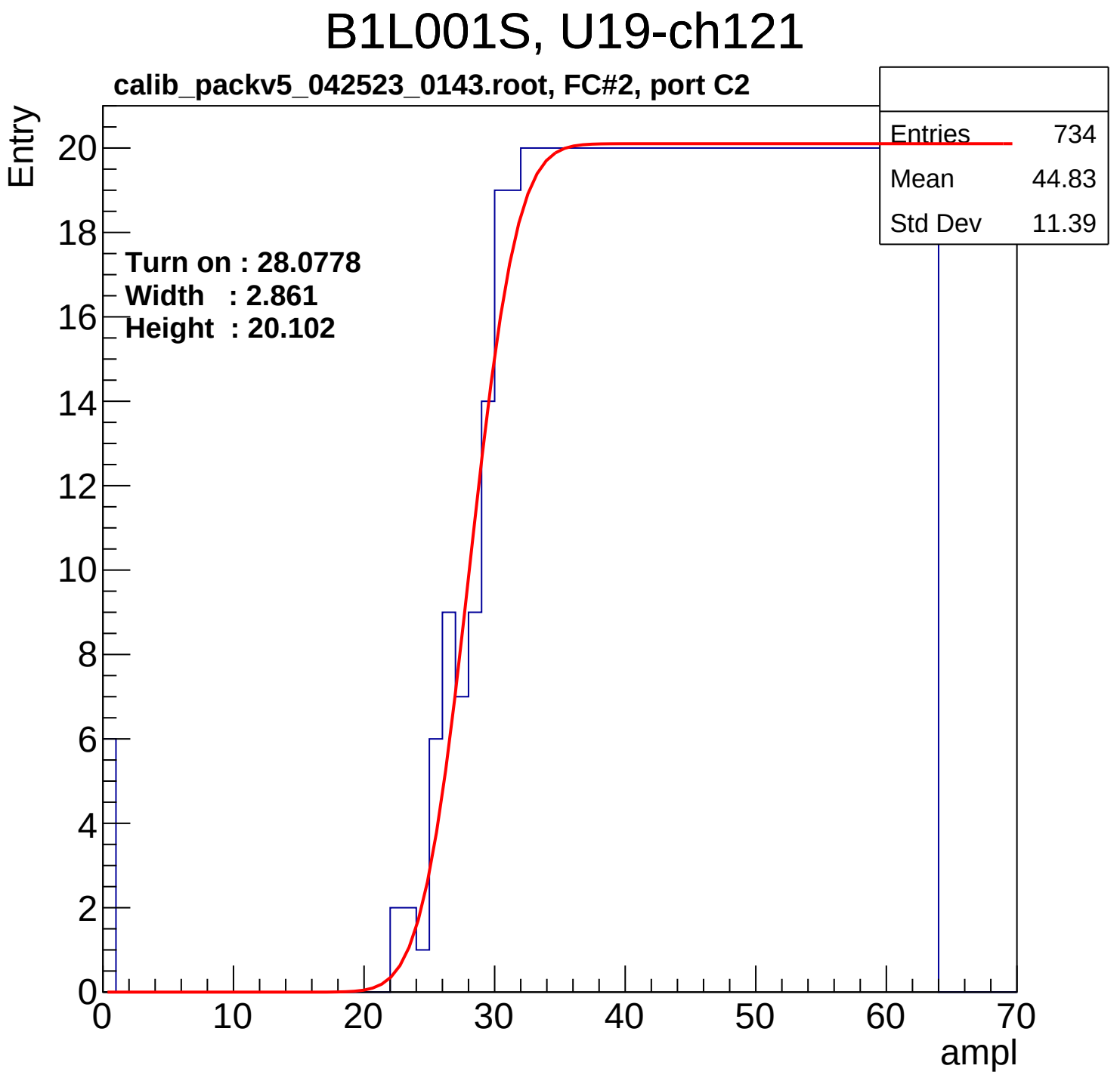
B1L001S, U19-ch121
calib_packv5_042523_0143.root, FC#2, port C2
Entries 734
Mean 44.83
Std Dev 11.39
Turn on : 28.0778
Width : 2.861
Height : 20.102
Entry
ampl
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6
8
10
12
14
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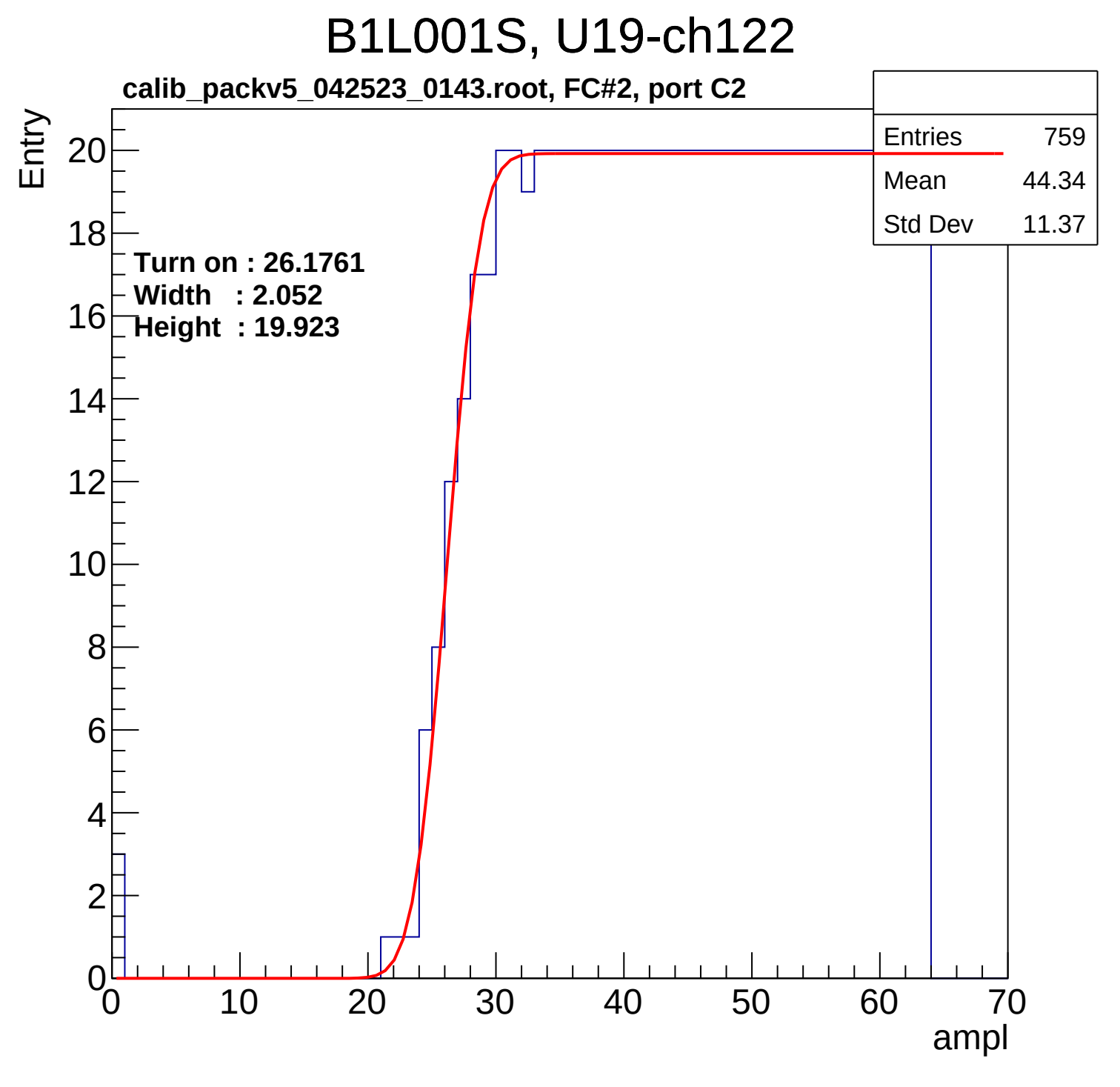
B1L001S, U19-ch122
calib_packv5_042523_0143.root, FC#2, port C2
Entries 759
Mean 44.34
Std Dev 11.37
Turn on : 26.1761
Width : 2.052
Height : 19.923
Entry
ampl
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6
8
10
12
14
16
18
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0
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20
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40
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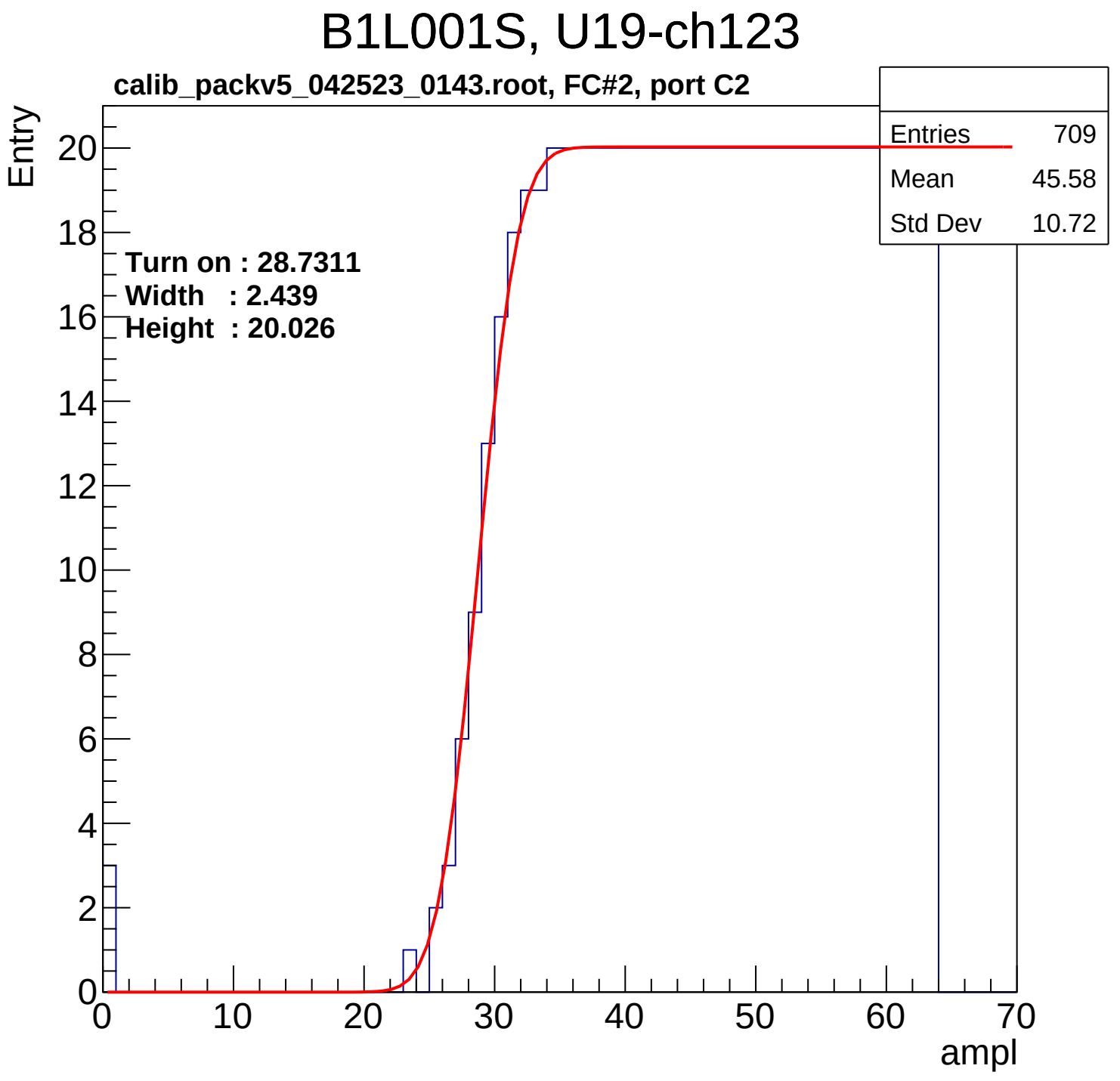
B1L001S, U19-ch123
calib_packv5_042523_0143.root, FC#2, port C2
Entries 709
Mean 45.58
Std Dev 10.72
Turn on : 28.7311
Width : 2.439
Height : 20.026
Entry
ampl
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6
8
10
12
14
16
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0
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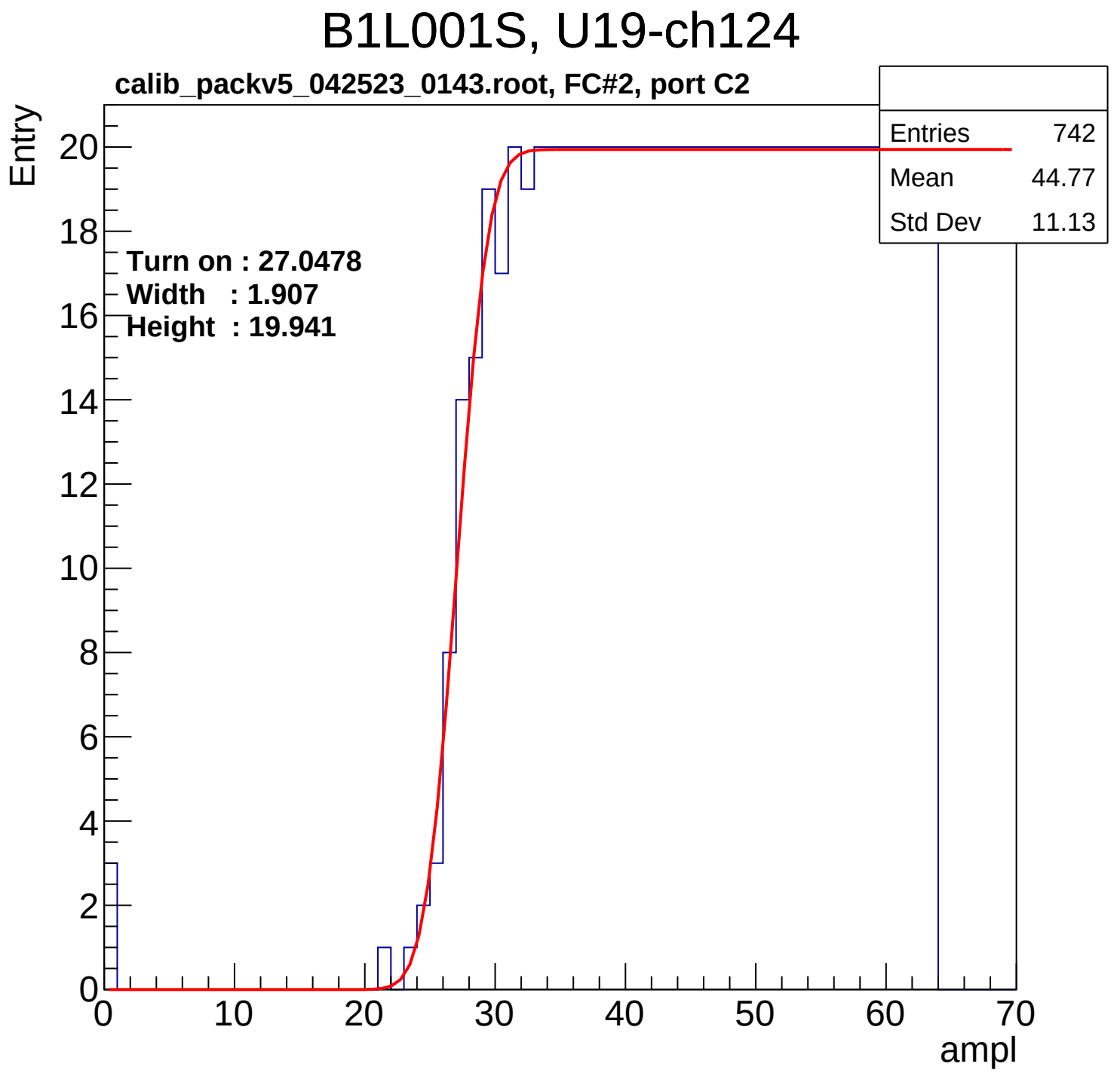
B1L001S, U19-ch124
calib_packv5_042523_0143.root, FC#2, port C2
Entries 742
Mean 44.77
Std Dev 11.13
Turn on : 27.0478
Width : 1.907
Height : 19.941
Entry
ampl
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6
8
10
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14
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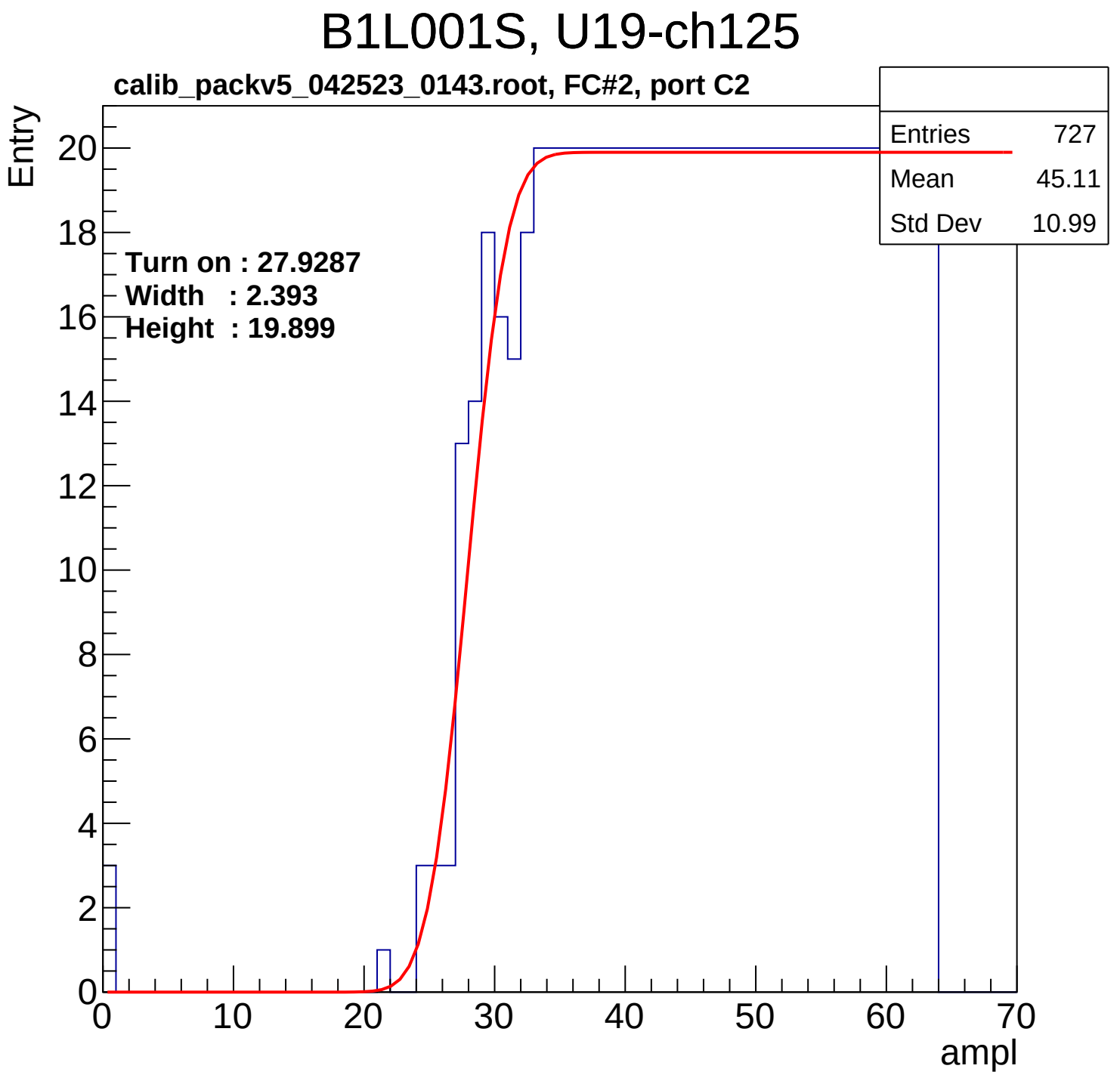
B1L001S, U19-ch125
calib_packv5_042523_0143.root, FC#2, port C2
Entries 727
Mean 45.11
Std Dev 10.99
Turn on : 27.9287
Width : 2.393
Height : 19.899
Entry
ampl
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6
8
10
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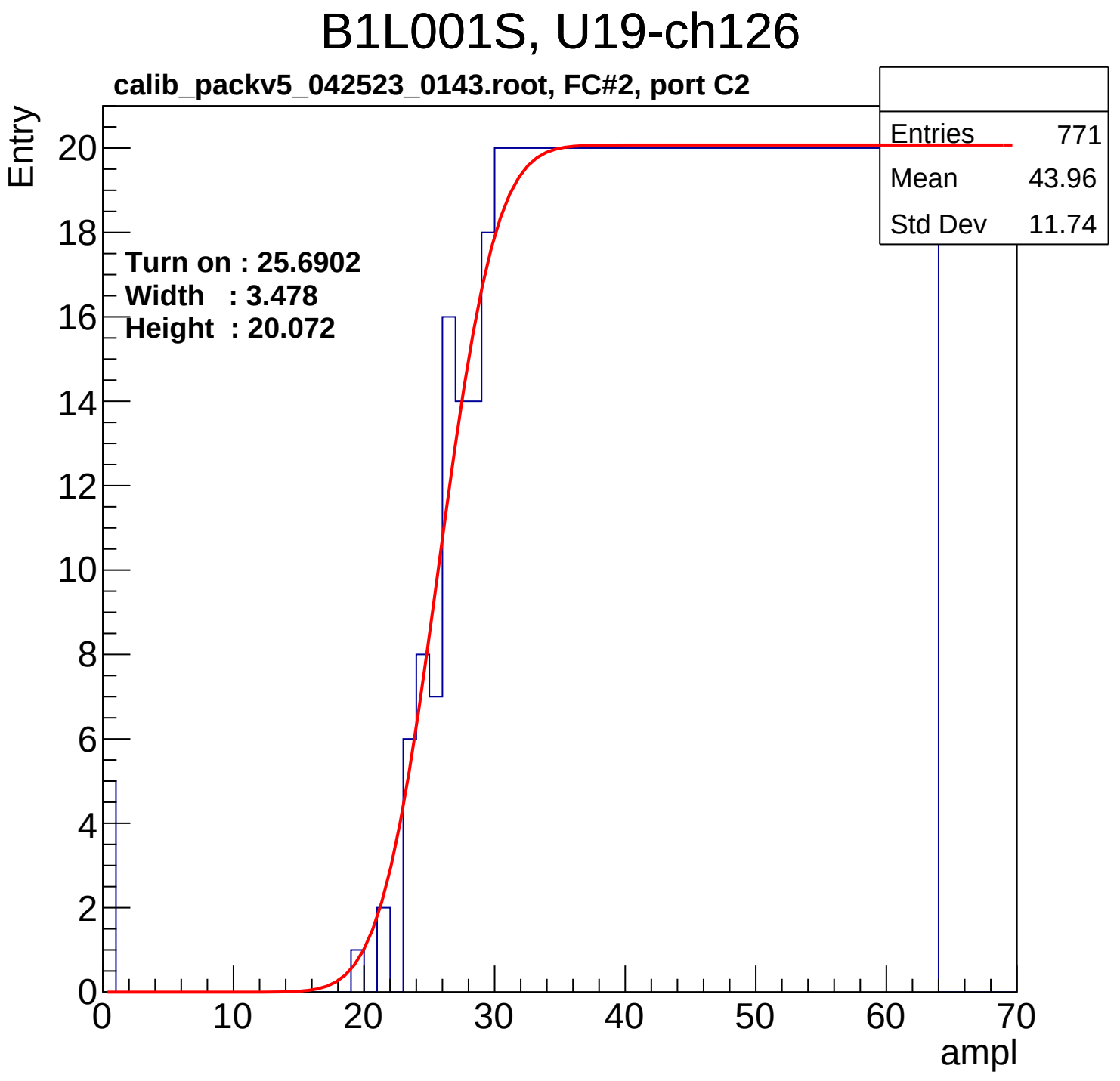
B1L001S, U19-ch126
calib_packv5_042523_0143.root, FC#2, port C2
Entries 771
Mean 43.96
Std Dev 11.74
Turn on : 25.6902
Width : 3.478
Height : 20.072
Entry
ampl
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6
8
10
12
14
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0
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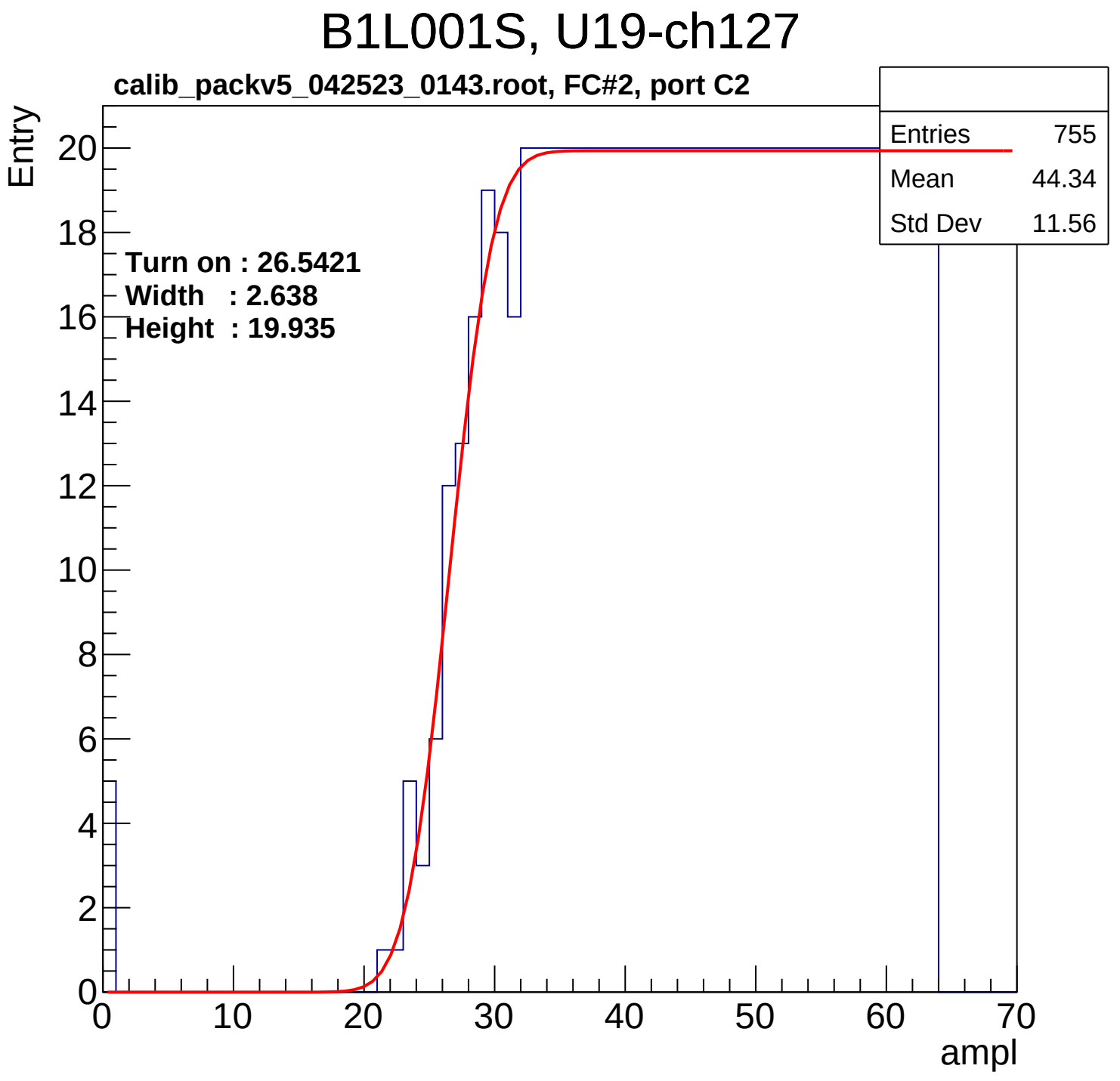
B1L001S, U19-ch127
calib_packv5_042523_0143.root, FC#2, port C2
Entries 755
Mean 44.34
Std Dev 11.56
Turn on : 26.5421
Width : 2.638
Height : 19.935
Entry
ampl
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6
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10
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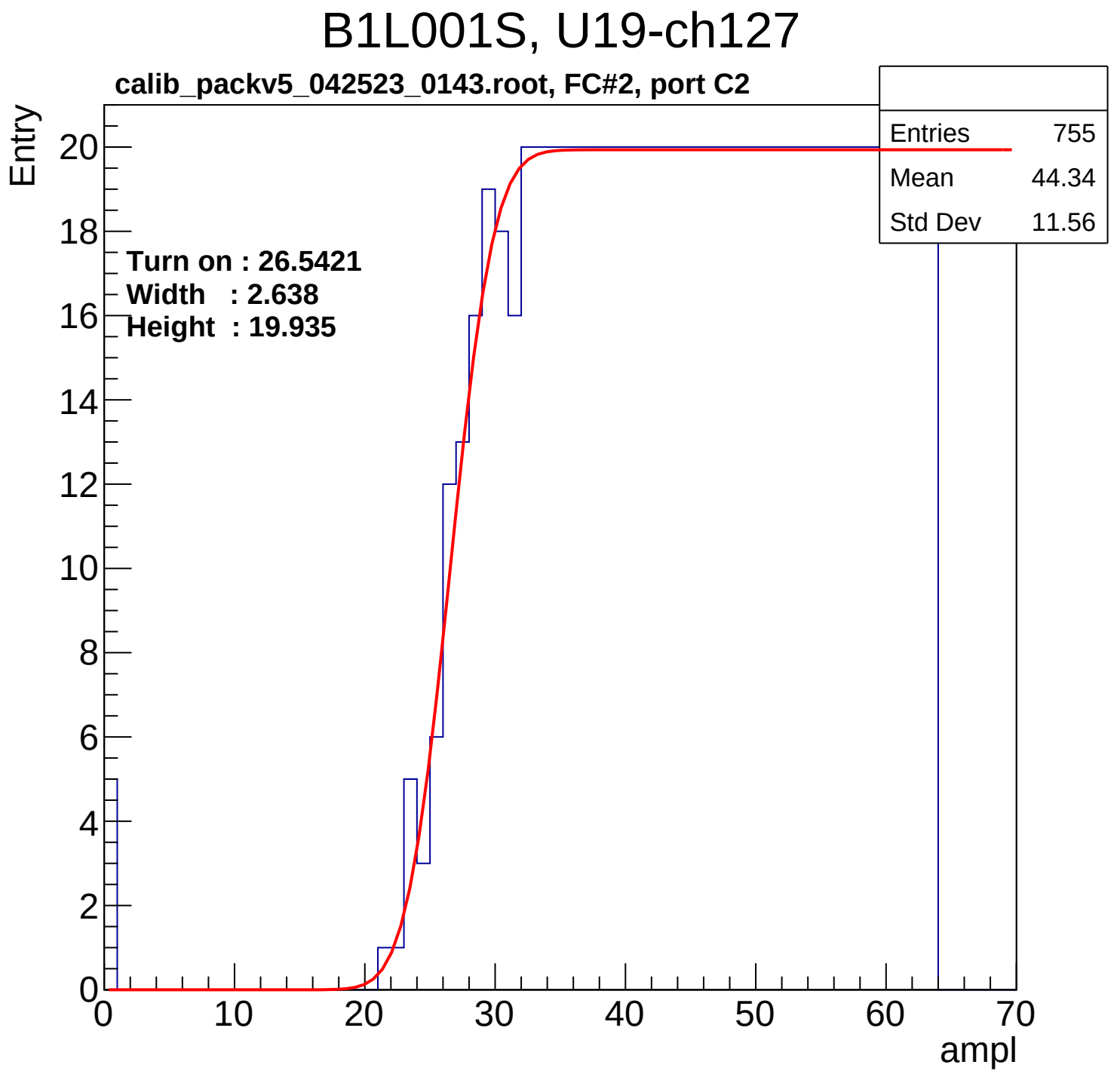
B1L001S, U19-ch127
calib_packv5_042523_0143.root, FC#2, port C2
Entries 755
Mean 44.34
Std Dev 11.56
Turn on : 26.5421
Width : 2.638
Height : 19.935
Entry
ampl
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