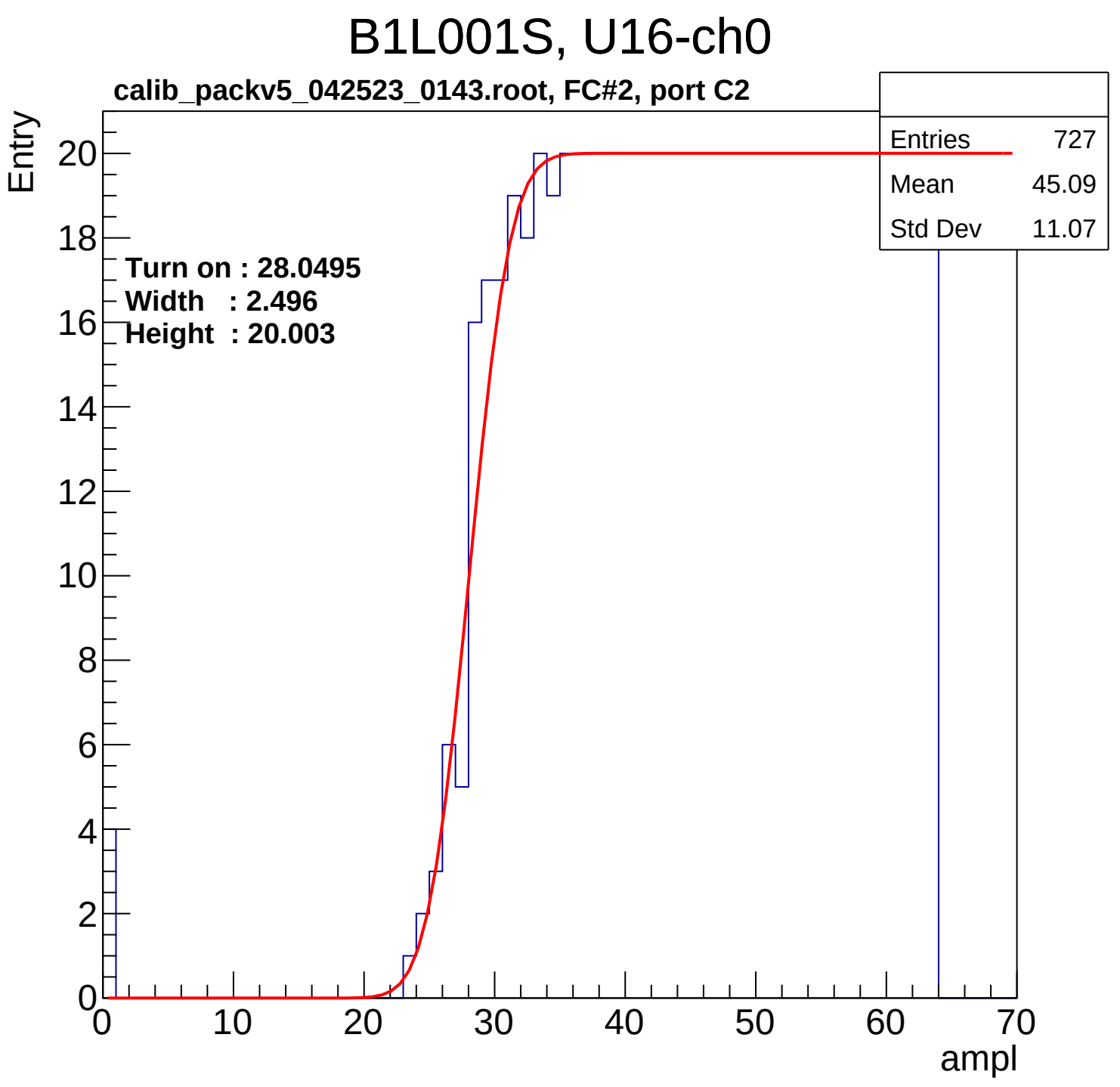
B1L001S, U16-ch0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 727
Mean 45.09
Std Dev 11.07
Turn on : 28.0495
Width : 2.496
Height : 20.003
Entry
ampl
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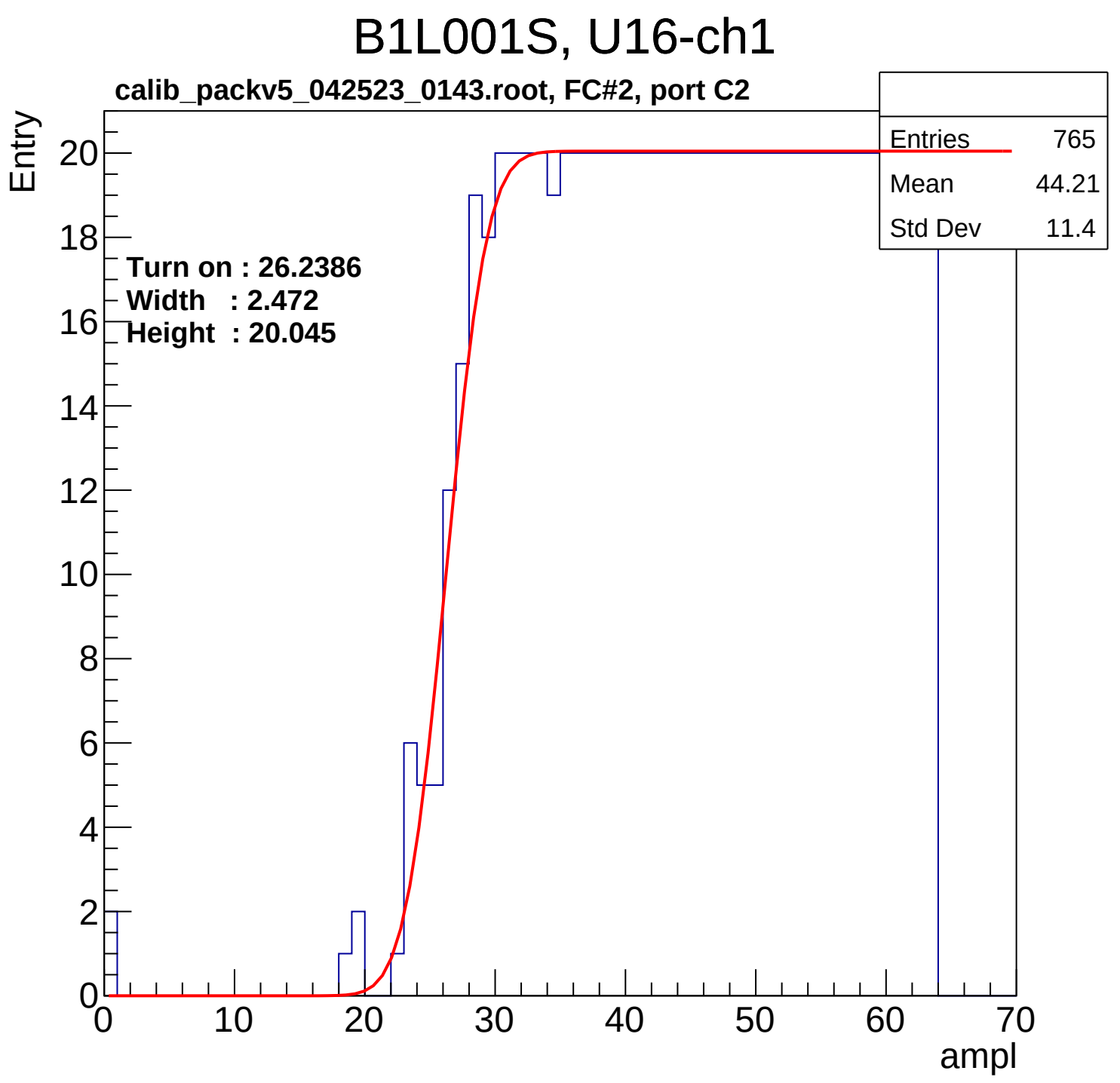
B1L001S, U16-ch1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 765
Mean 44.21
Std Dev 11.4
Turn on : 26.2386
Width : 2.472
Height : 20.045
Entry
ampl
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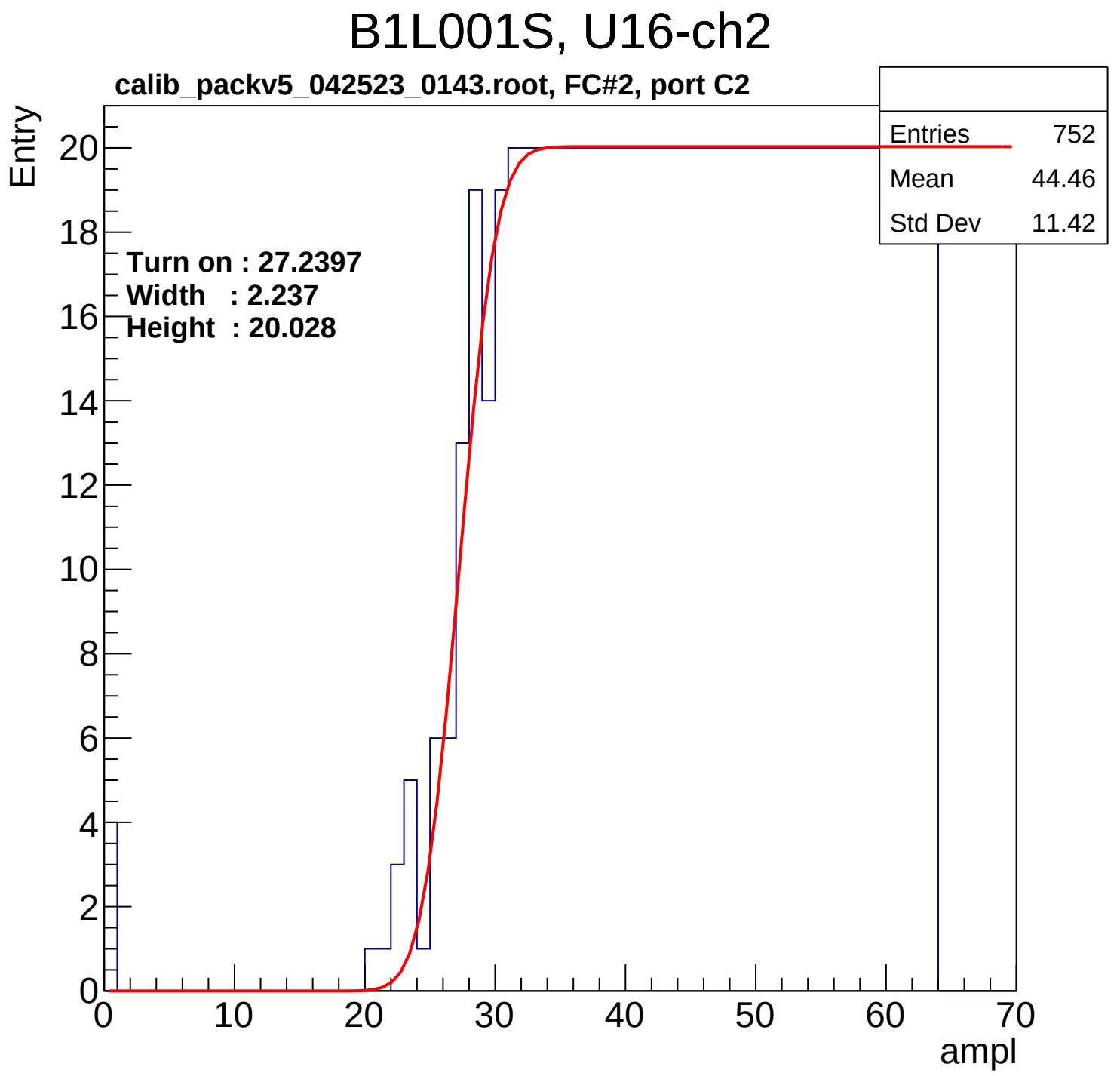
B1L001S, U16-ch2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 752
Mean 44.46
Std Dev 11.42
Turn on : 27.2397
Width : 2.237
Height : 20.028
Entry
ampl
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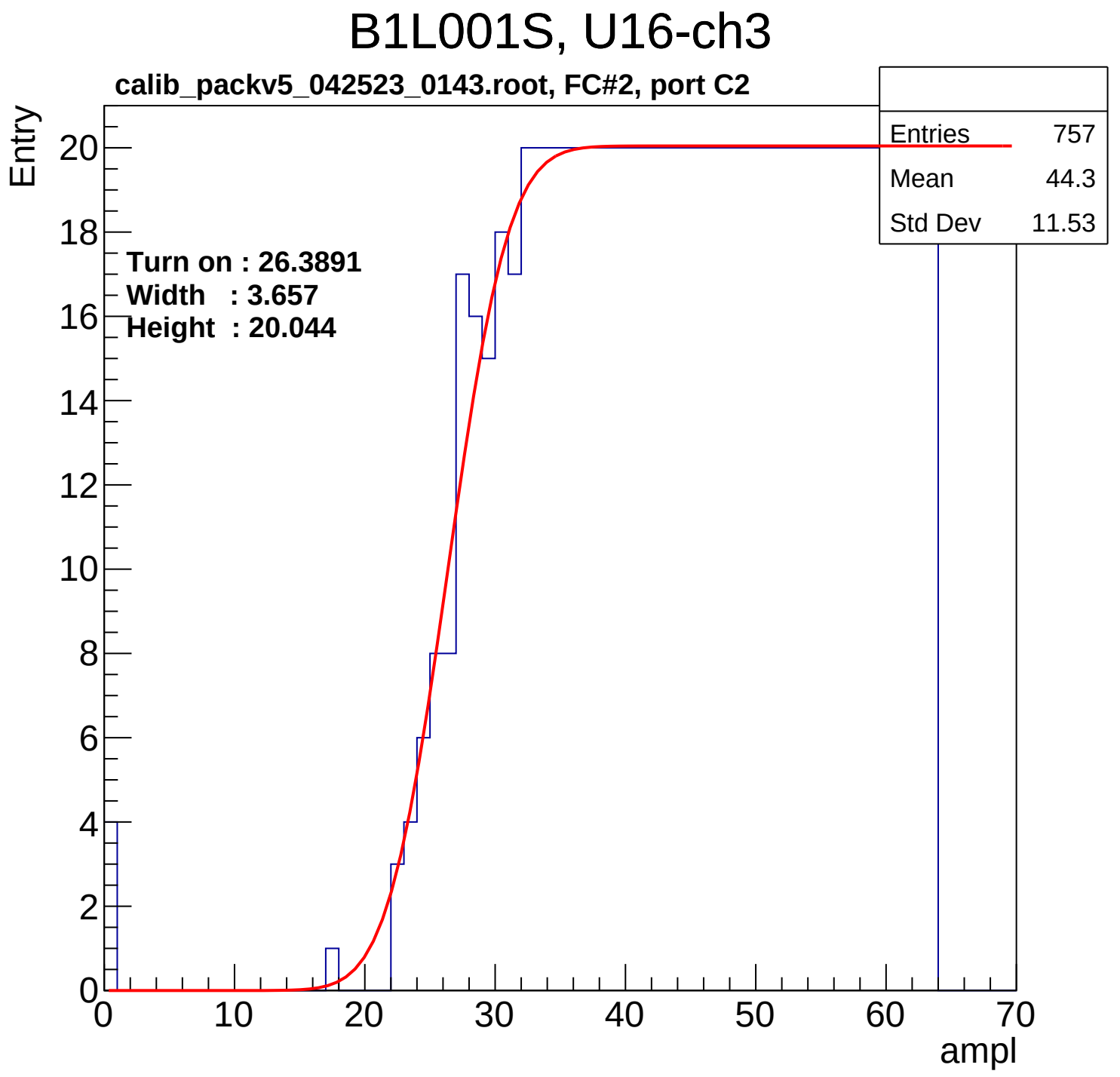
B1L001S, U16-ch3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 757
Mean 44.3
Std Dev 11.53
Turn on : 26.3891
Width : 3.657
Height : 20.044
Entry
ampl
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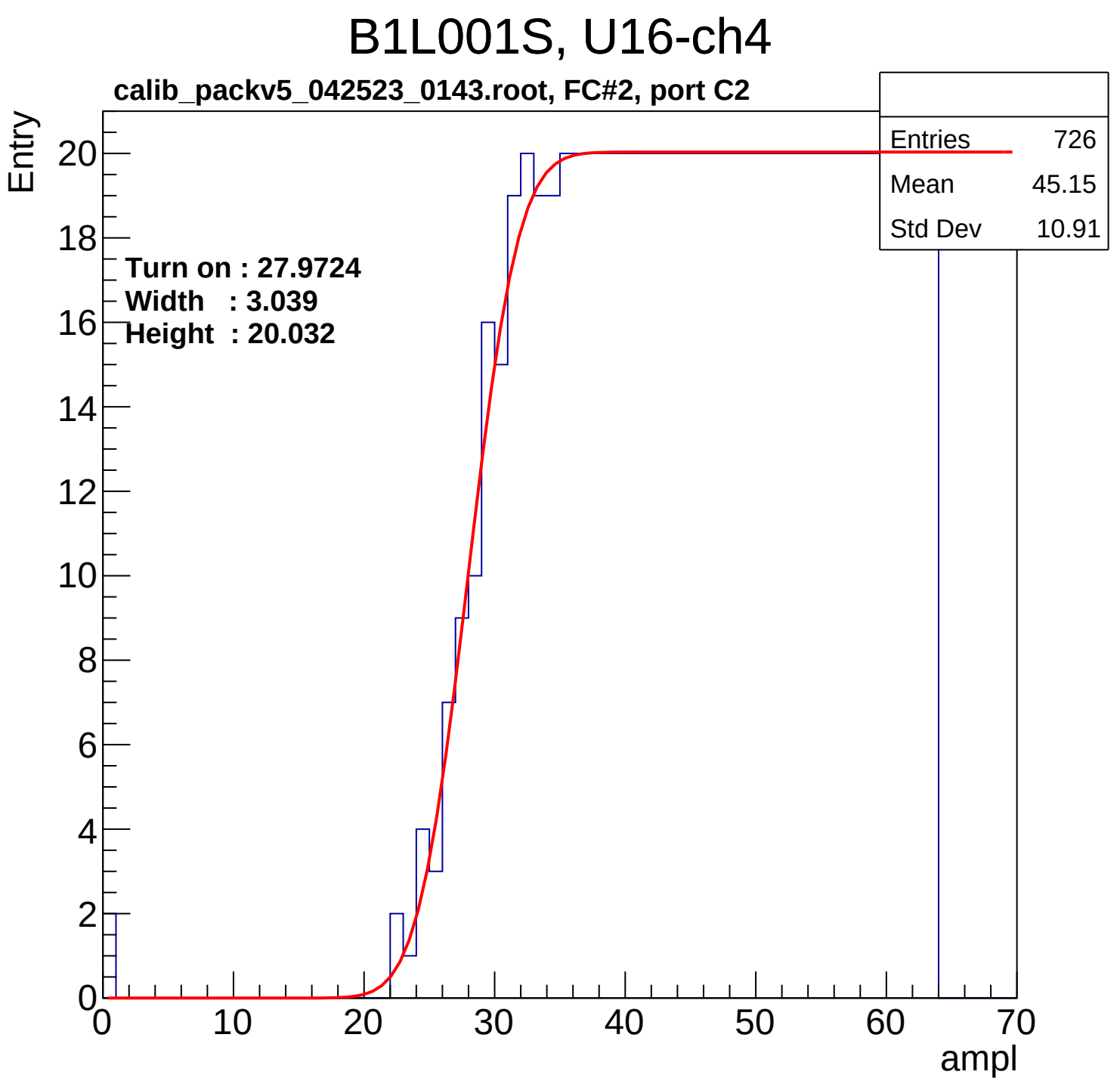
B1L001S, U16-ch4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 726
Mean 45.15
Std Dev 10.91
Turn on : 27.9724
Width : 3.039
Height : 20.032
Entry
ampl
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6
8
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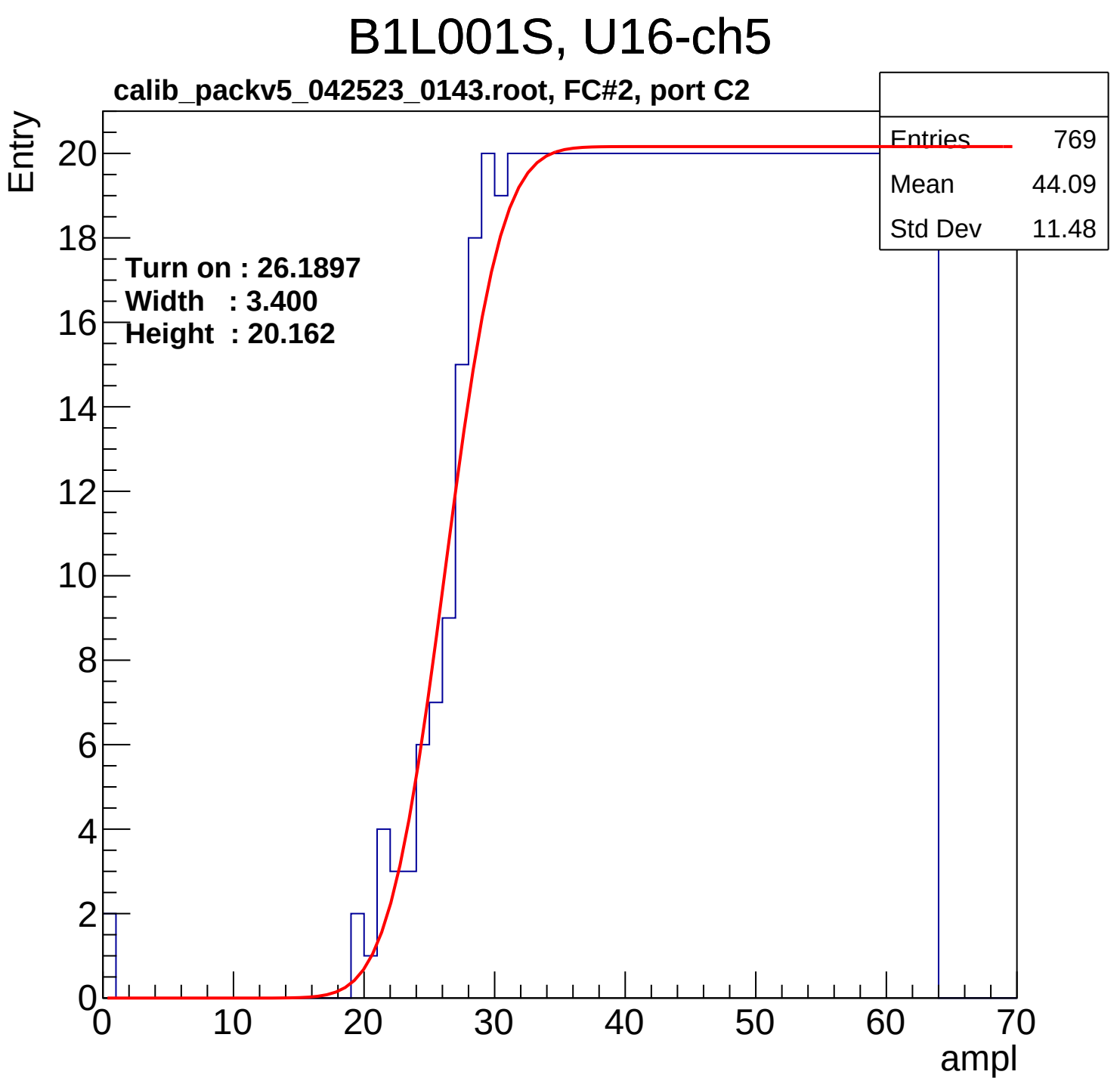
B1L001S, U16-ch5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 769
Mean 44.09
Std Dev 11.48
Turn on : 26.1897
Width : 3.400
Height : 20.162
Entry
ampl
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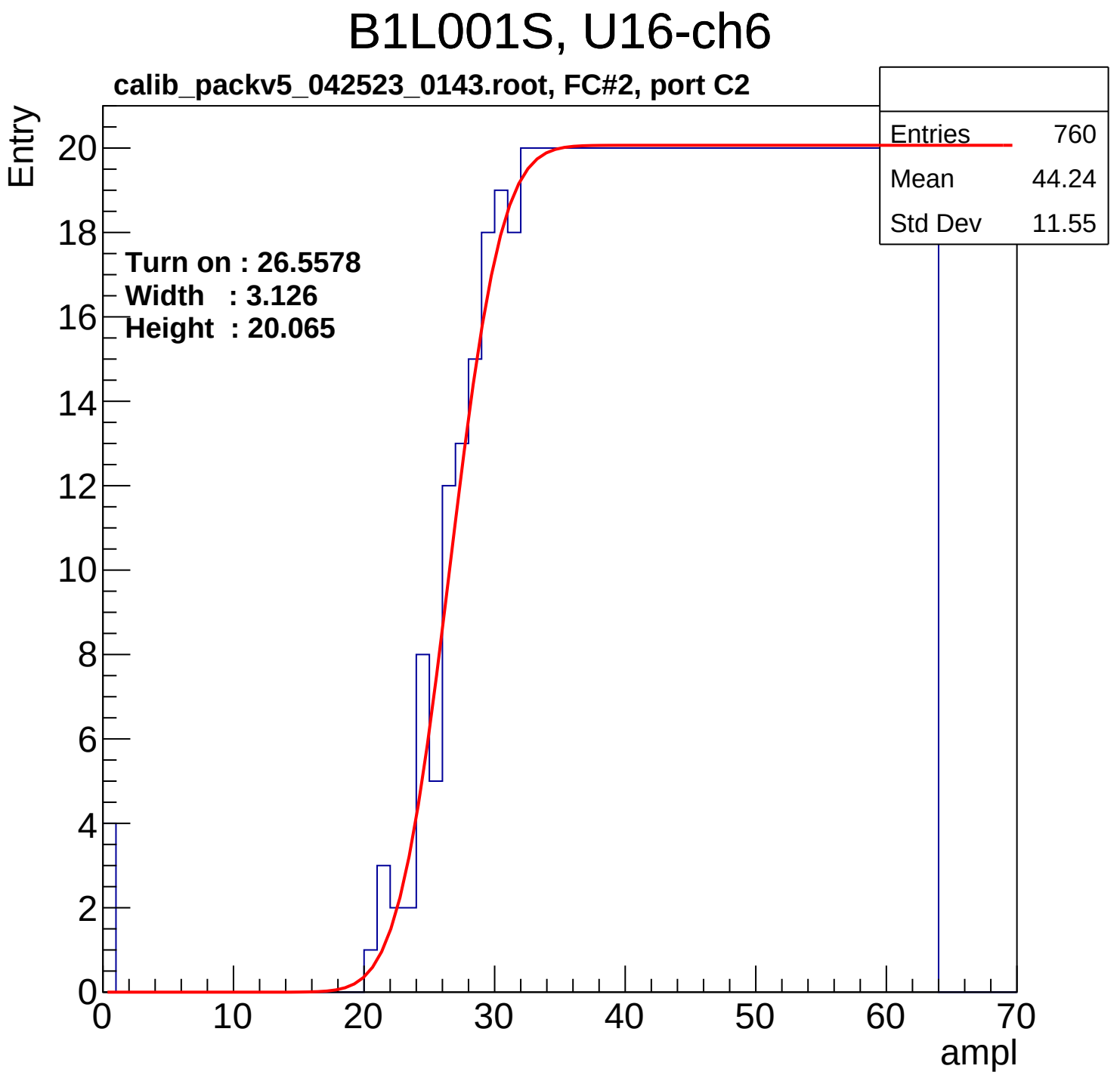
B1L001S, U16-ch6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 760
Mean 44.24
Std Dev 11.55
Turn on : 26.5578
Width : 3.126
Height : 20.065
Entry
ampl
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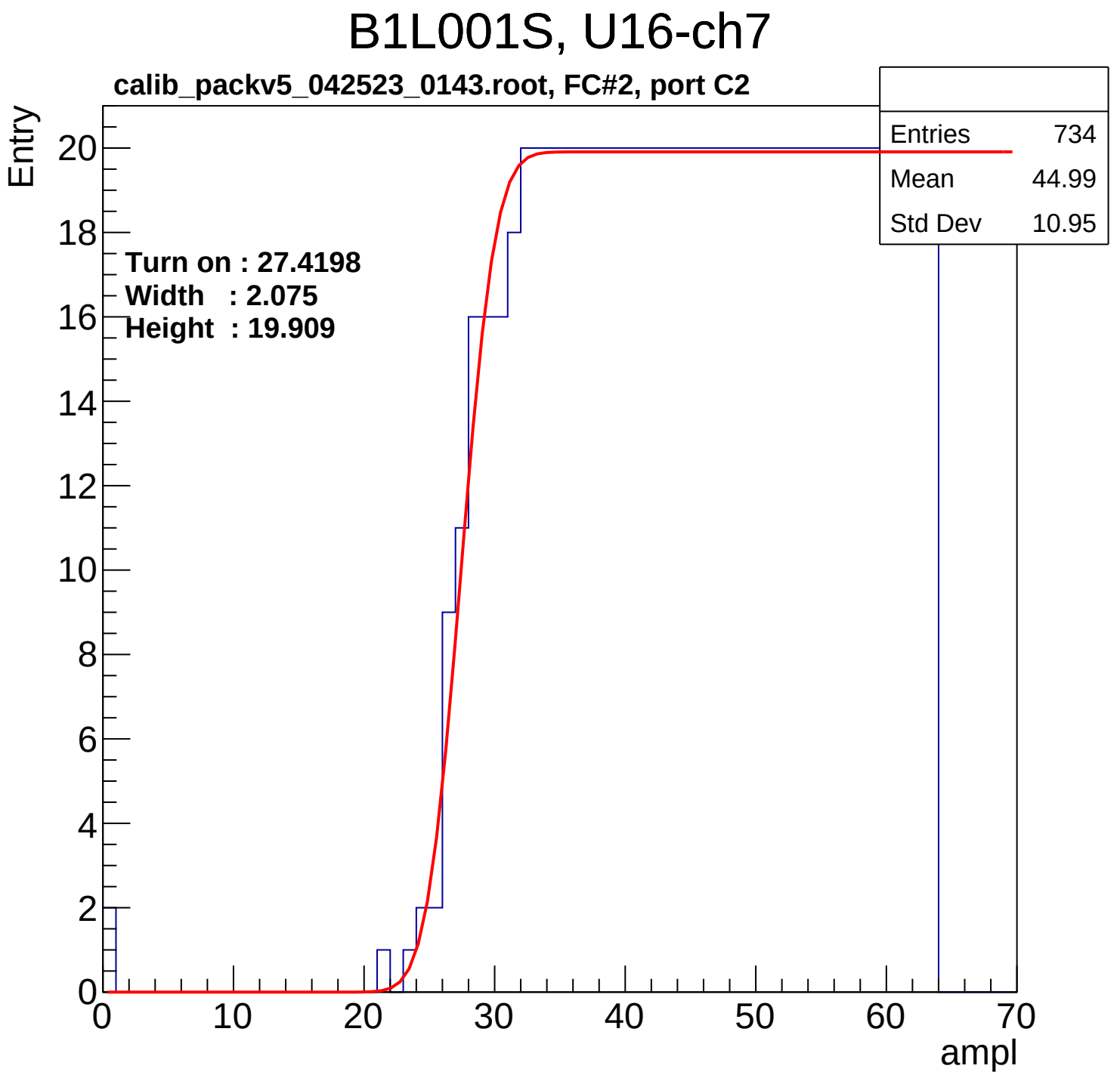
B1L001S, U16-ch7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 734
Mean 44.99
Std Dev 10.95
Turn on : 27.4198
Width : 2.075
Height : 19.909
Entry
ampl
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6
8
10
12
14
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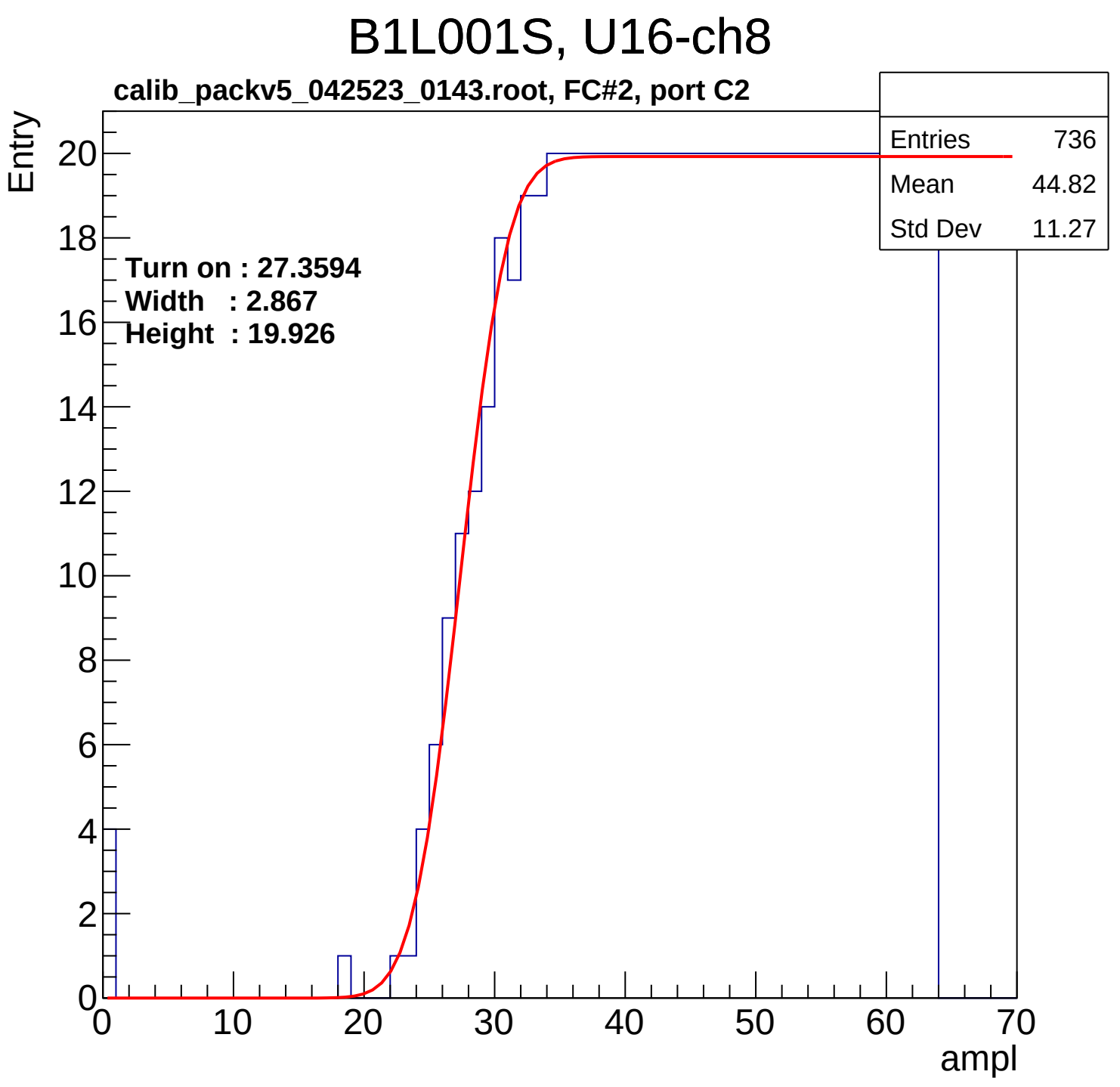
B1L001S, U16-ch8
calib_packv5_042523_0143.root, FC#2, port C2
Entries 736
Mean 44.82
Std Dev 11.27
Turn on : 27.3594
Width : 2.867
Height : 19.926
Entry
ampl
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6
8
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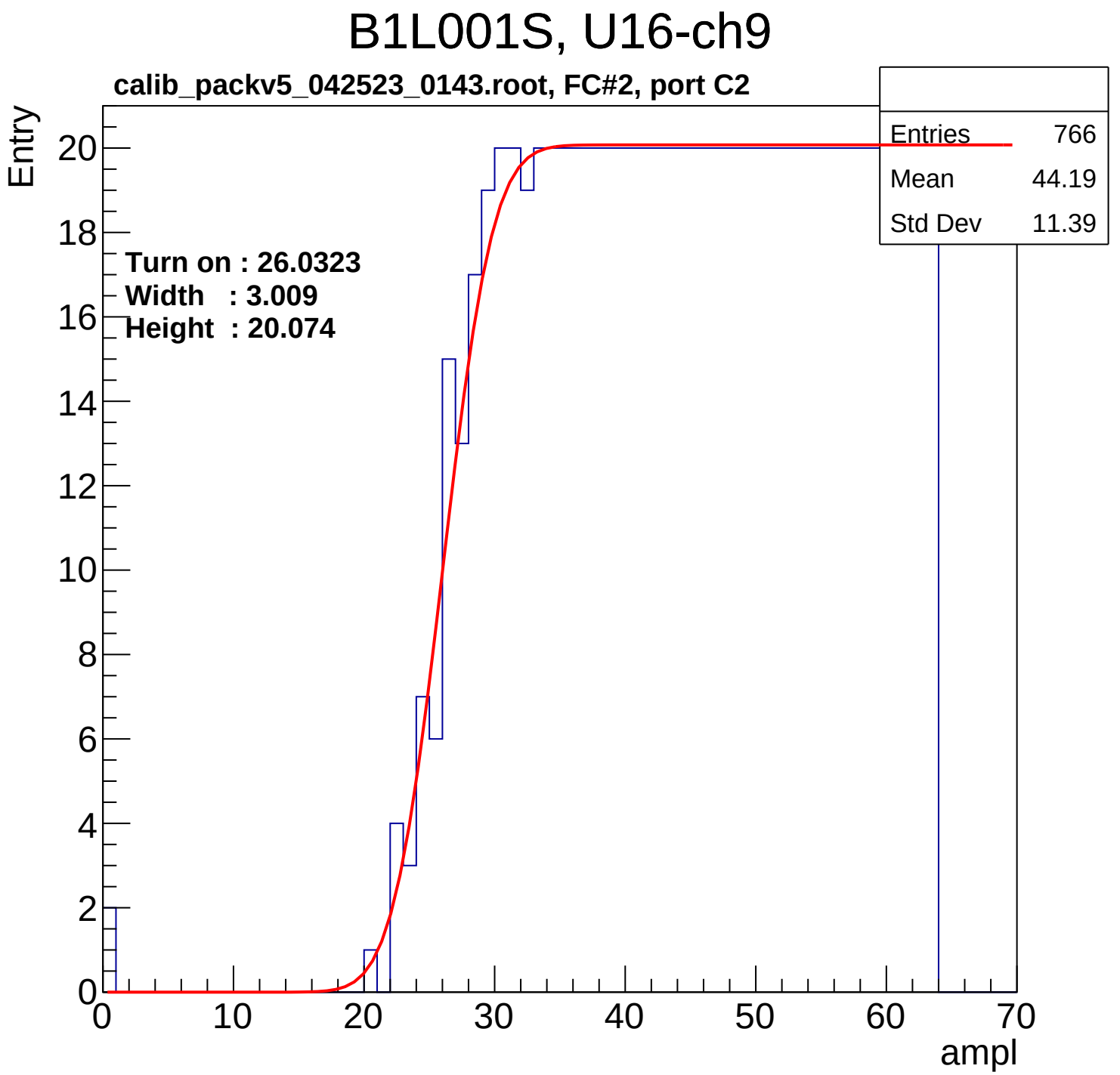
B1L001S, U16-ch9
calib_packv5_042523_0143.root, FC#2, port C2
Entries 766
Mean 44.19
Std Dev 11.39
Turn on : 26.0323
Width : 3.009
Height : 20.074
Entry
ampl
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6
8
10
12
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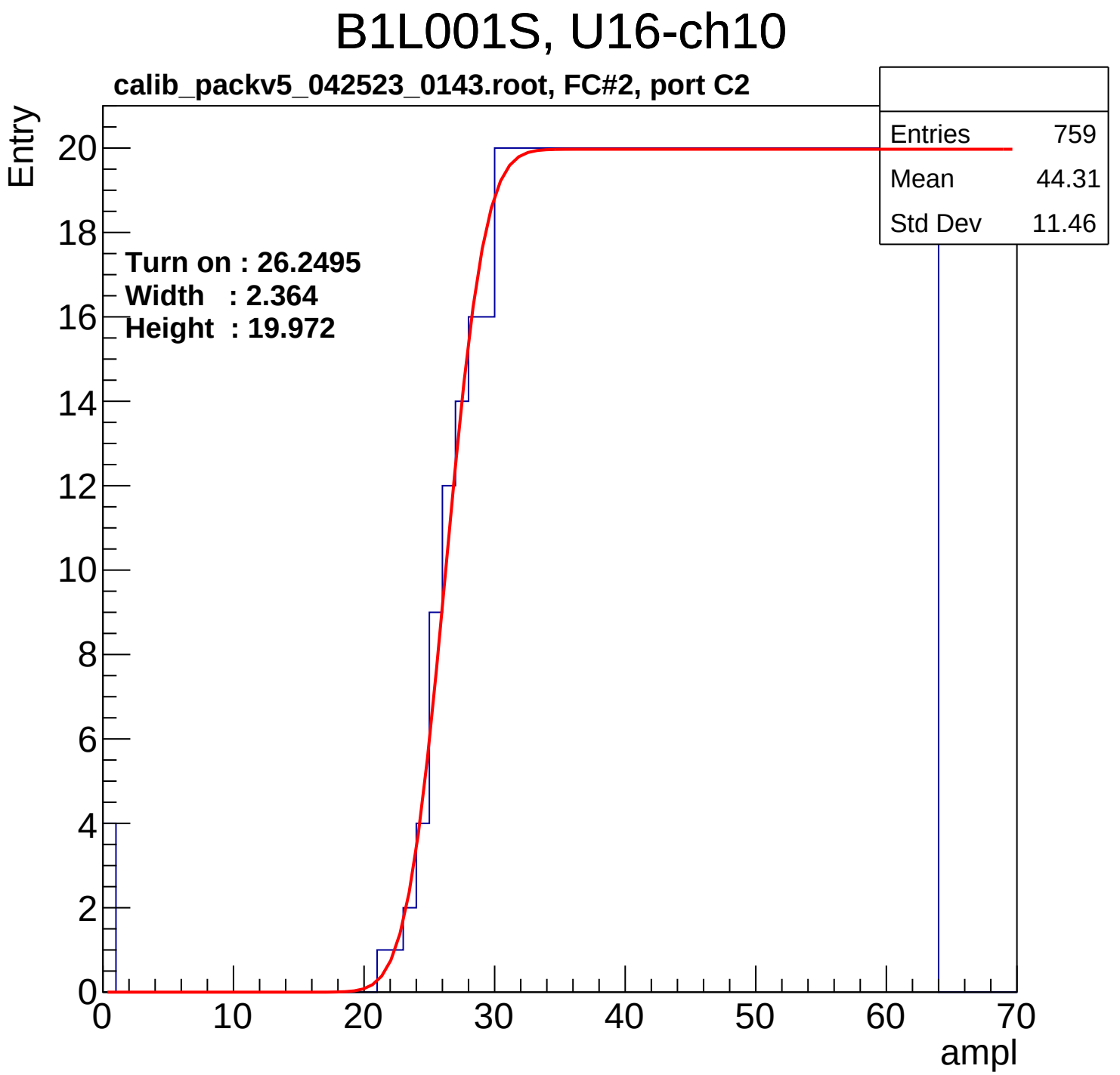
B1L001S, U16-ch10
calib_packv5_042523_0143.root, FC#2, port C2
Entries 759
Mean 44.31
Std Dev 11.46
Turn on : 26.2495
Width : 2.364
Height : 19.972
Entry
ampl
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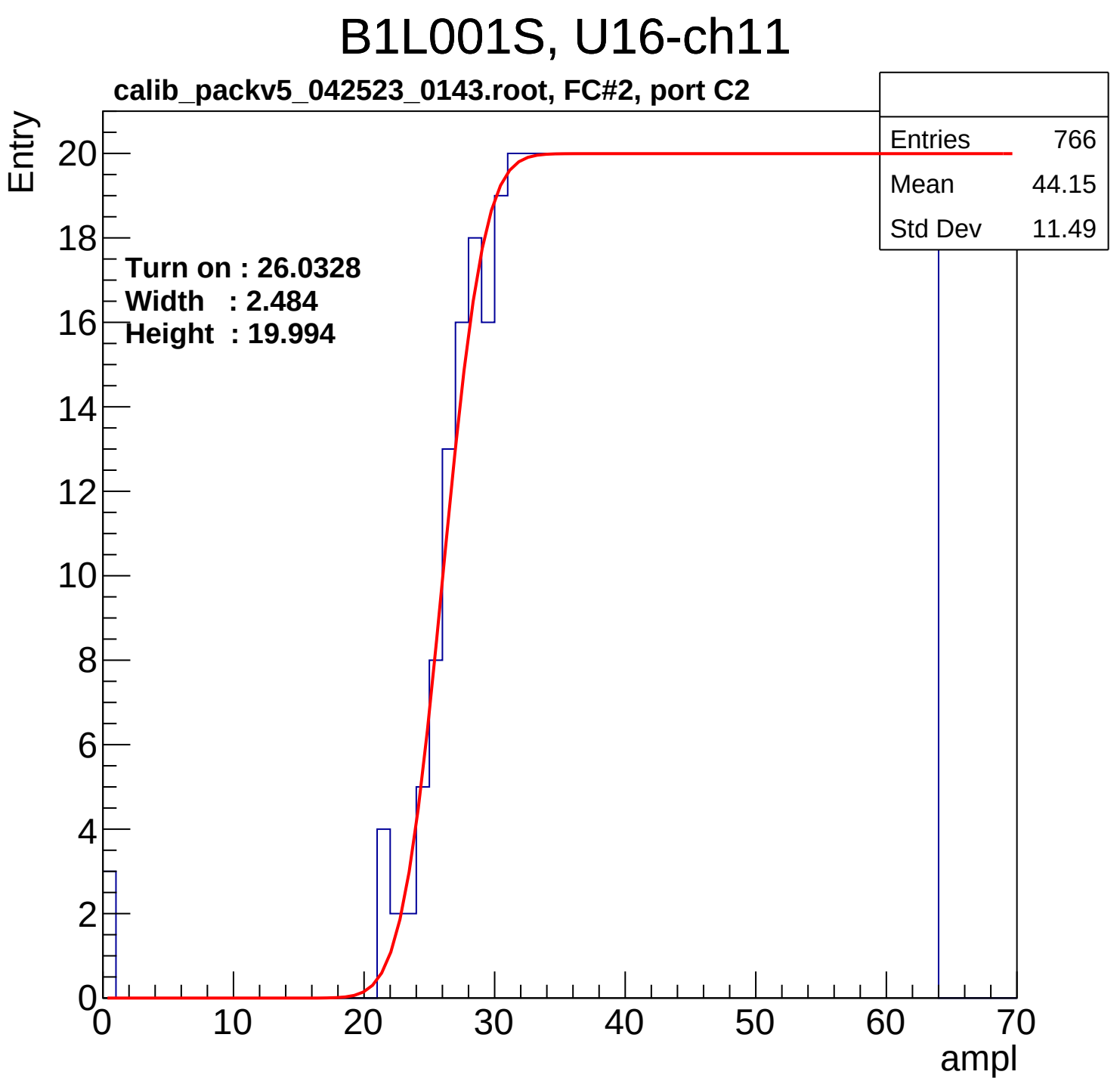
B1L001S, U16-ch11
calib_packv5_042523_0143.root, FC#2, port C2
Entries 766
Mean 44.15
Std Dev 11.49
Turn on : 26.0328
Width : 2.484
Height : 19.994
Entry
ampl
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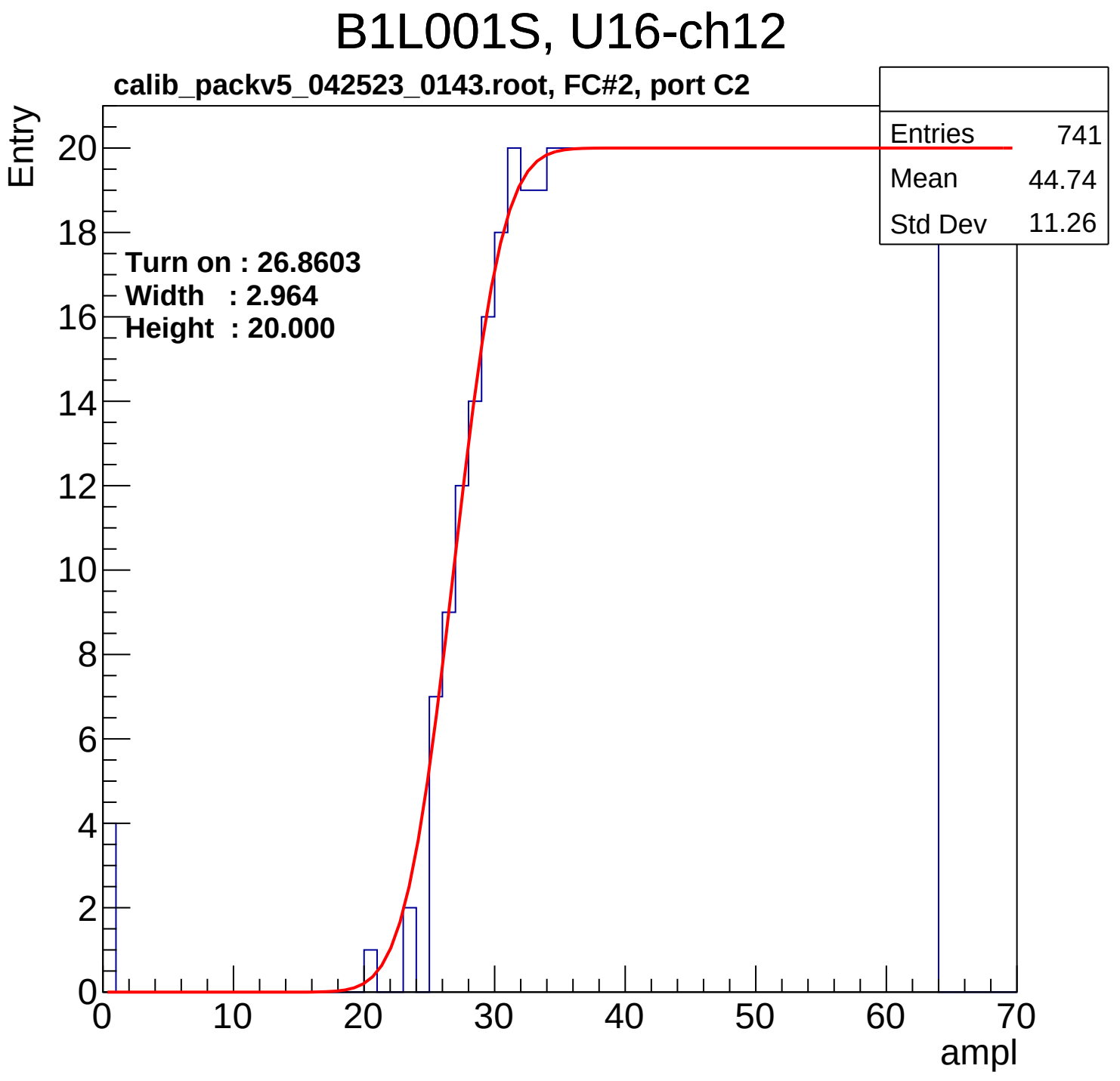
B1L001S, U16-ch12
calib_packv5_042523_0143.root, FC#2, port C2
Entries 741
Mean 44.74
Std Dev 11.26
Turn on : 26.8603
Width : 2.964
Height : 20.000
Entry
ampl
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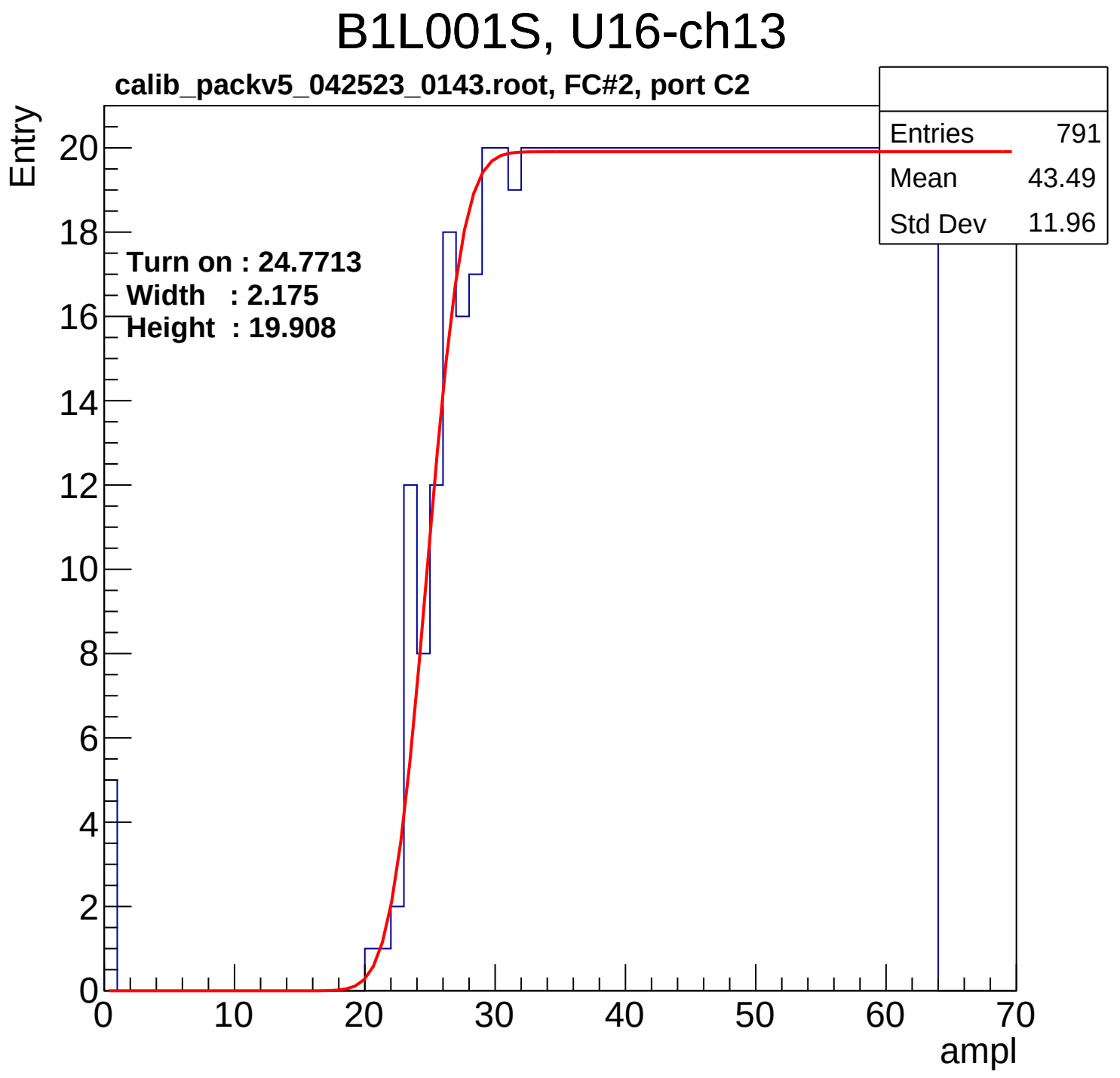
B1L001S, U16-ch13
calib_packv5_042523_0143.root, FC#2, port C2
Entries 791
Mean 43.49
Std Dev 11.96
Turn on : 24.7713
Width : 2.175
Height : 19.908
Entry
ampl
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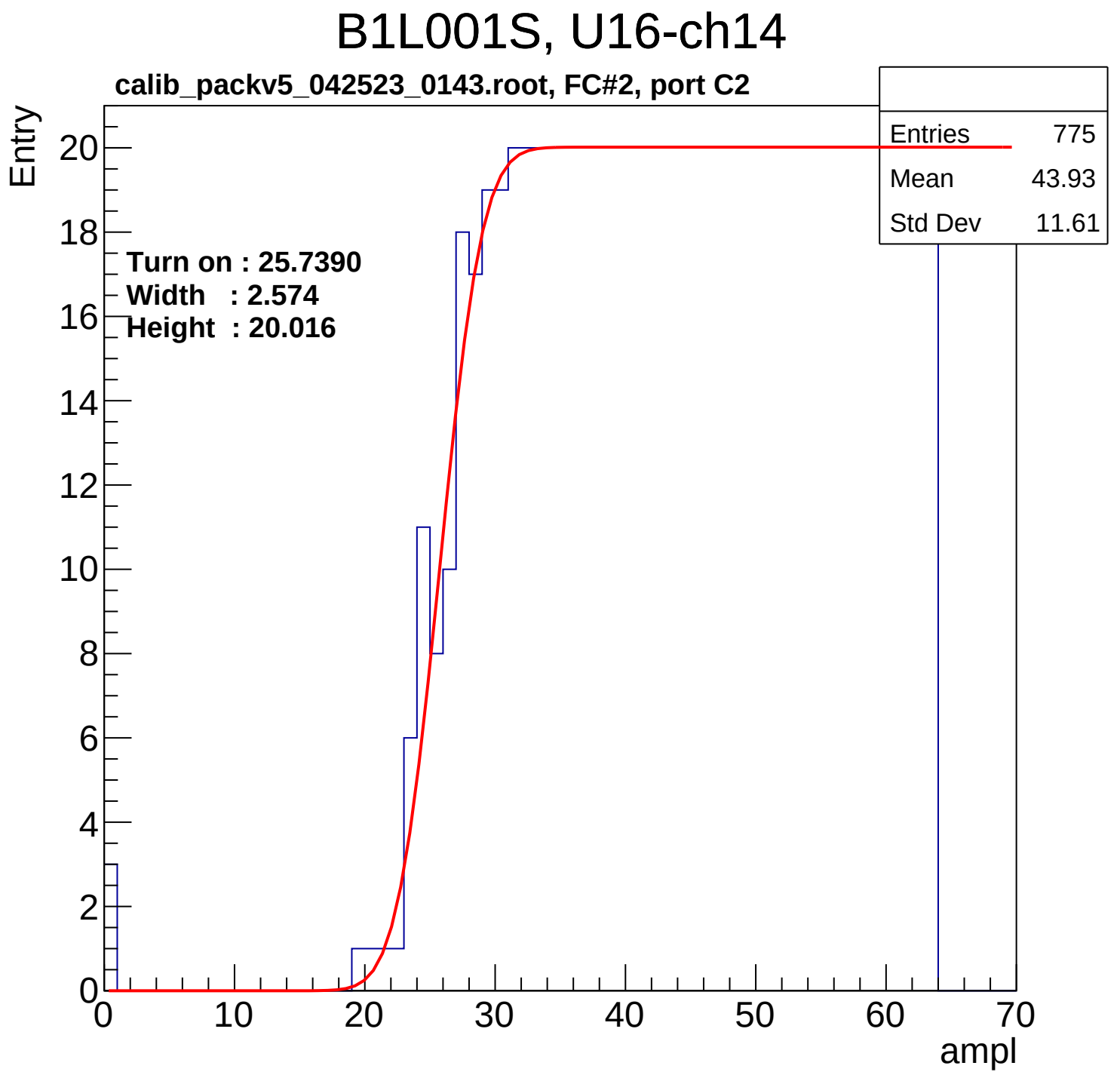
B1L001S, U16-ch14
calib_packv5_042523_0143.root, FC#2, port C2
Entries 775
Mean 43.93
Std Dev 11.61
Turn on : 25.7390
Width : 2.574
Height : 20.016
Entry
ampl
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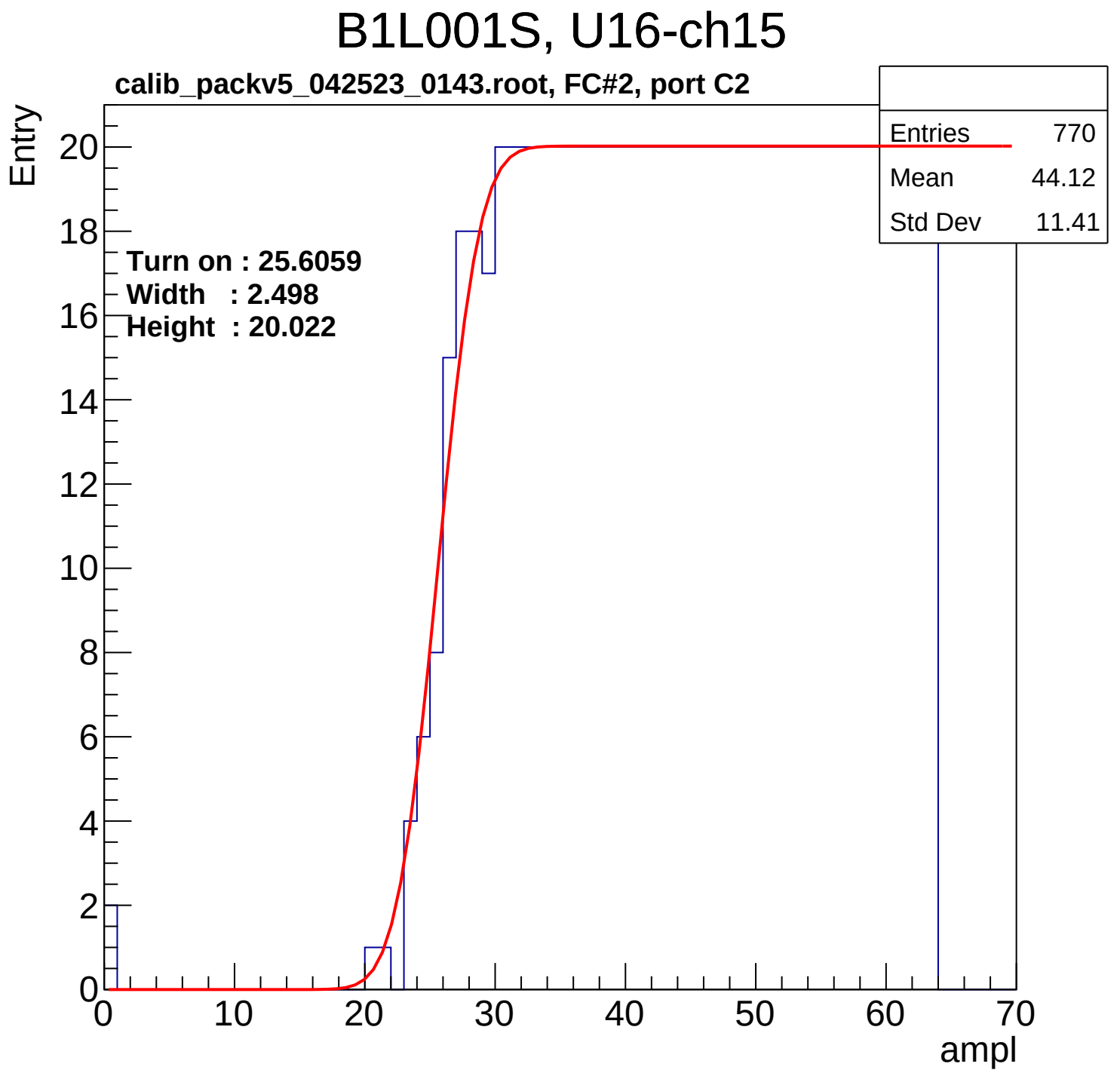
B1L001S, U16-ch15
calib_packv5_042523_0143.root, FC#2, port C2
Entries 770
Mean 44.12
Std Dev 11.41
Turn on : 25.6059
Width : 2.498
Height : 20.022
Entry
ampl
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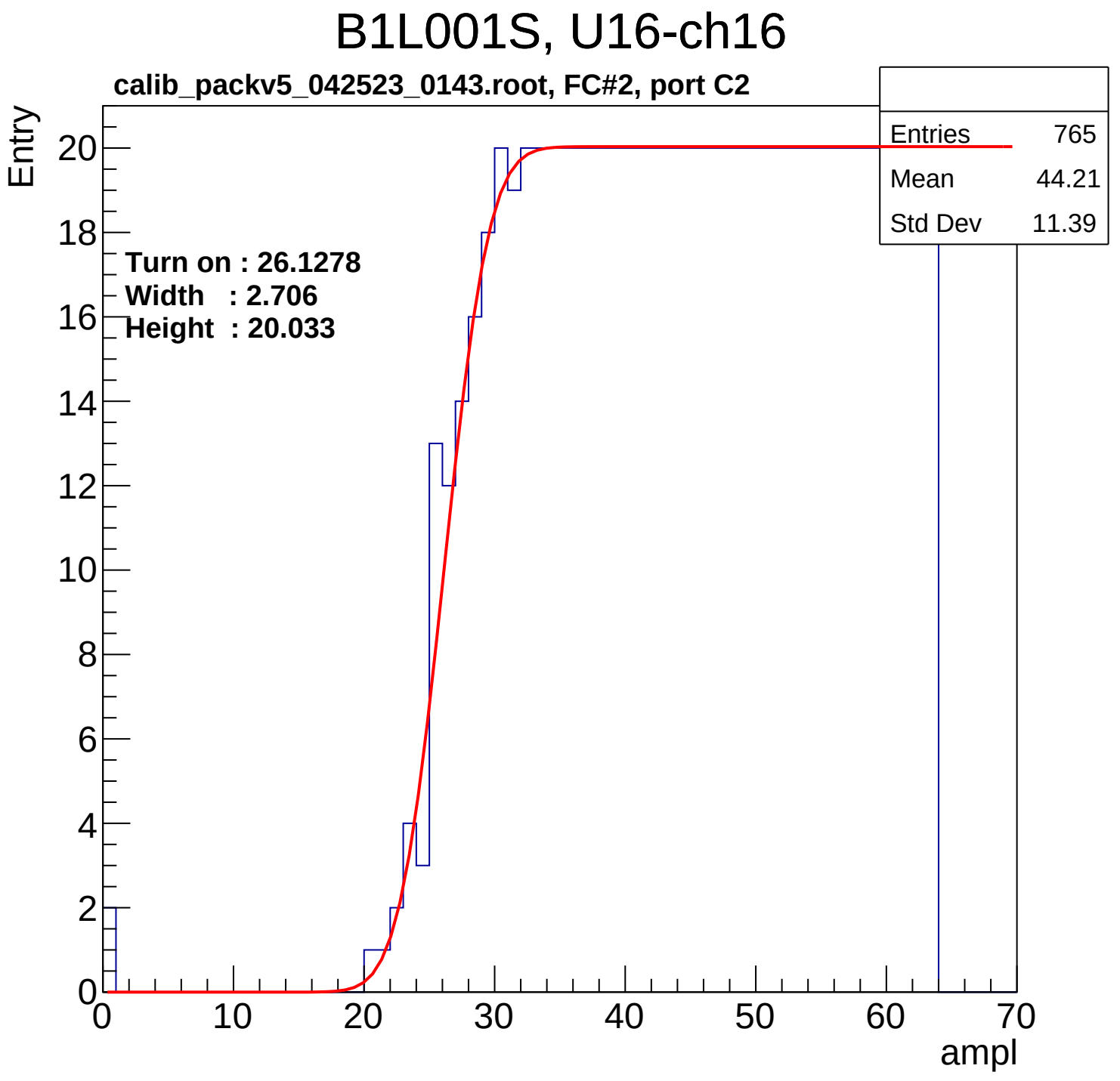
B1L001S, U16-ch16
calib_packv5_042523_0143.root, FC#2, port C2
Entries 765
Mean 44.21
Std Dev 11.39
Turn on : 26.1278
Width : 2.706
Height : 20.033
Entry
ampl
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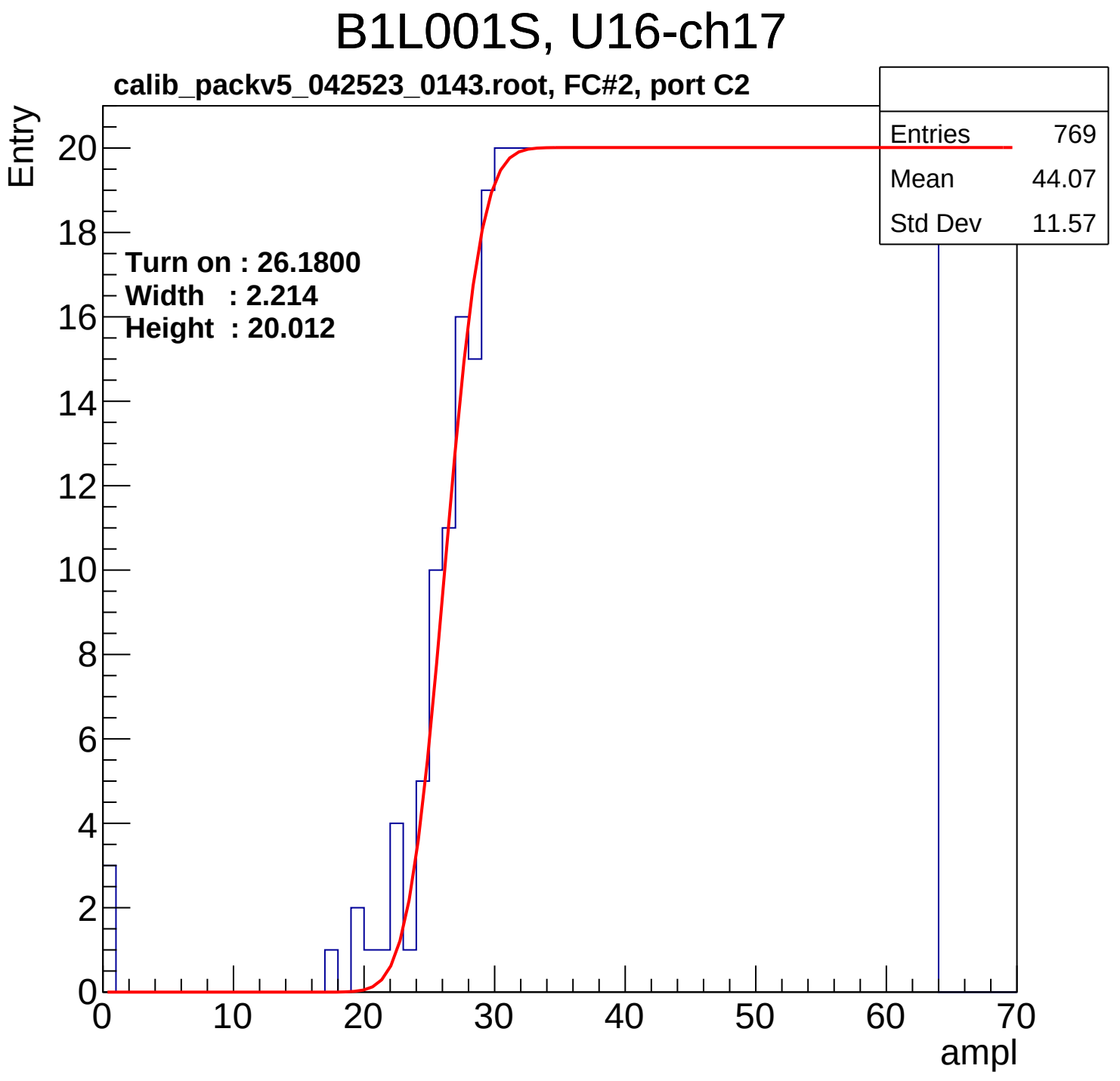
B1L001S, U16-ch17
calib_packv5_042523_0143.root, FC#2, port C2
Entries 769
Mean 44.07
Std Dev 11.57
Turn on : 26.1800
Width : 2.214
Height : 20.012
Entry
ampl
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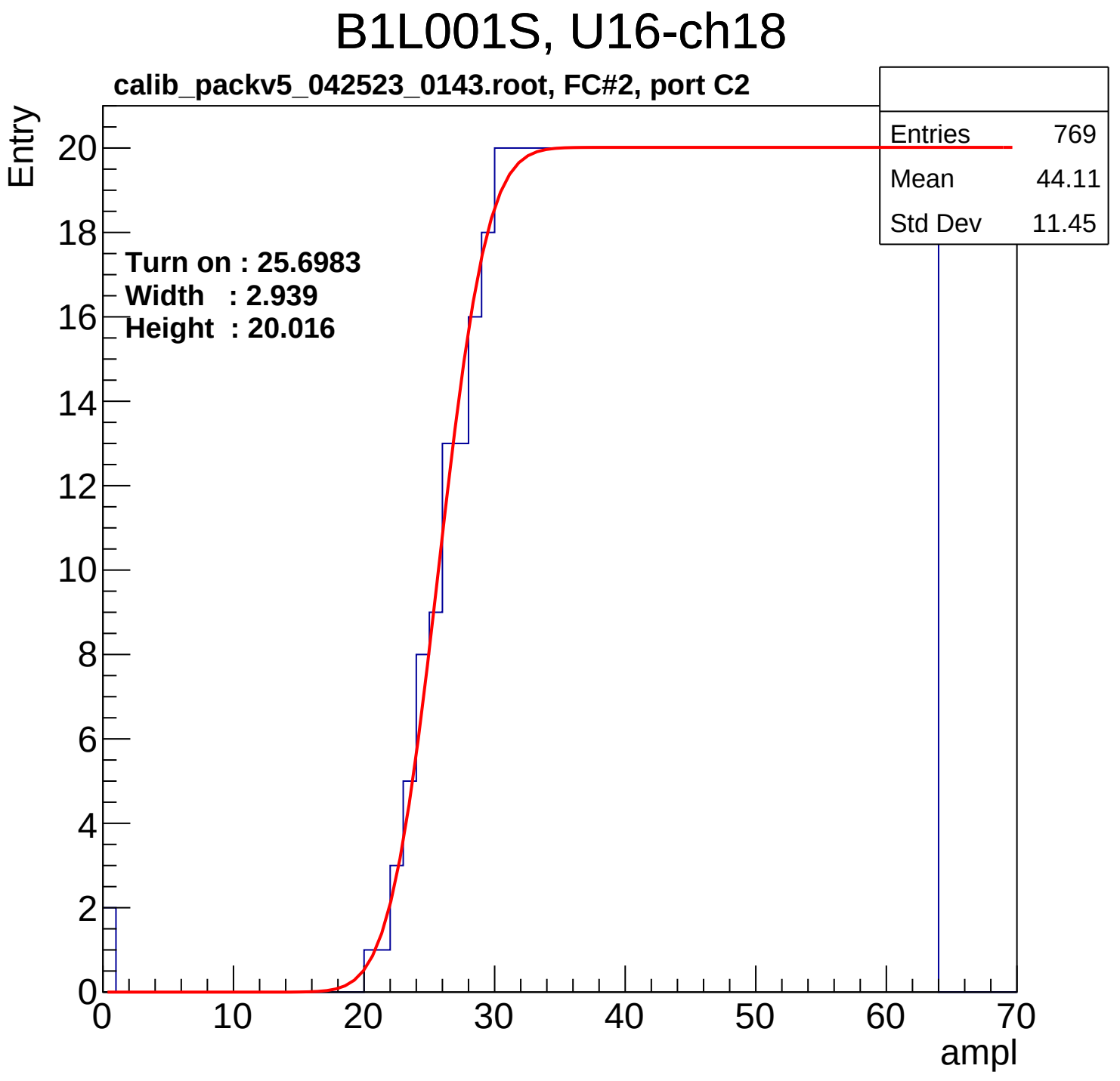
B1L001S, U16-ch18
calib_packv5_042523_0143.root, FC#2, port C2
Entries 769
Mean 44.11
Std Dev 11.45
Turn on : 25.6983
Width : 2.939
Height : 20.016
Entry
ampl
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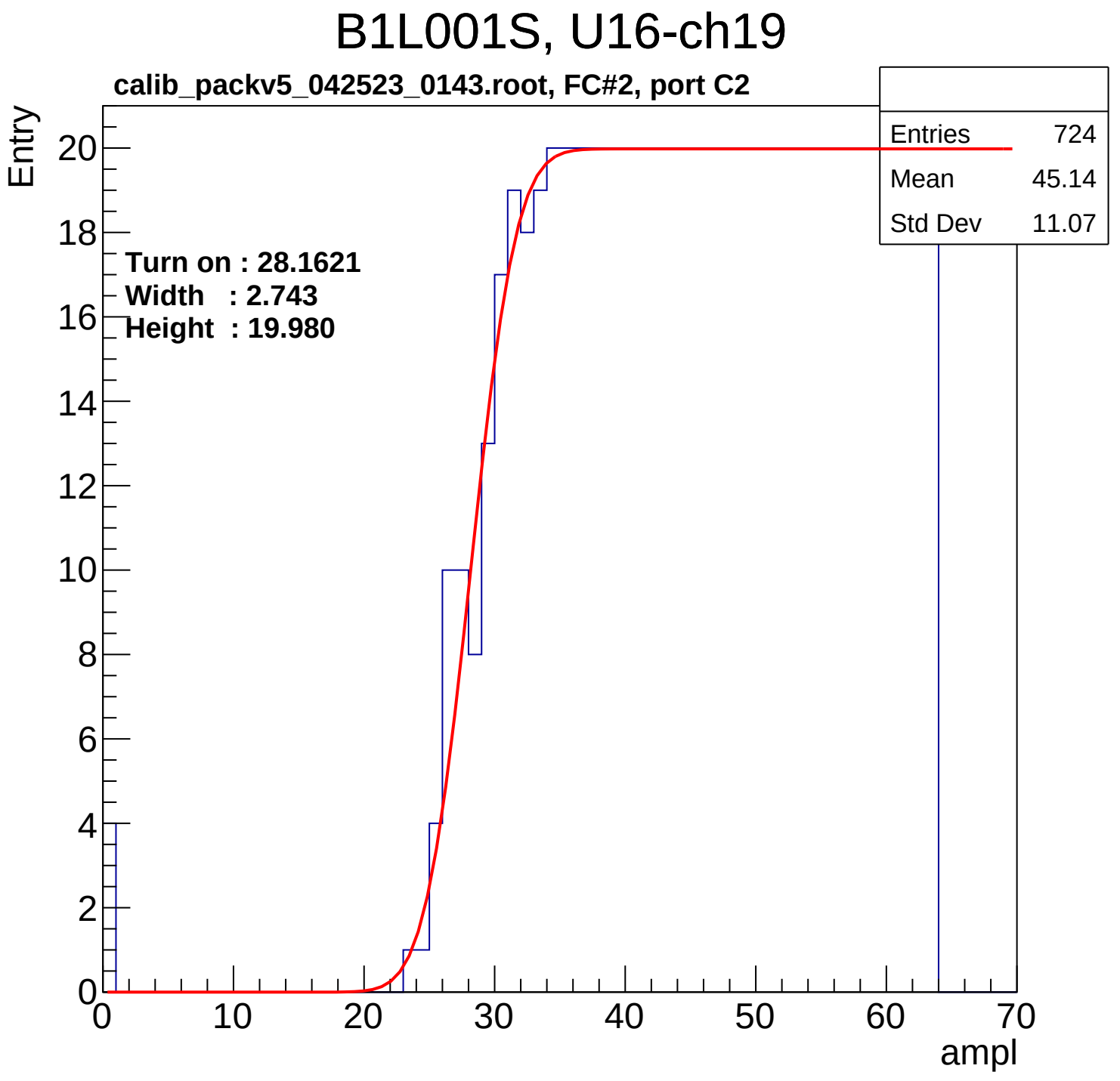
B1L001S, U16-ch19
calib_packv5_042523_0143.root, FC#2, port C2
Entries 724
Mean 45.14
Std Dev 11.07
Turn on : 28.1621
Width : 2.743
Height : 19.980
Entry
ampl
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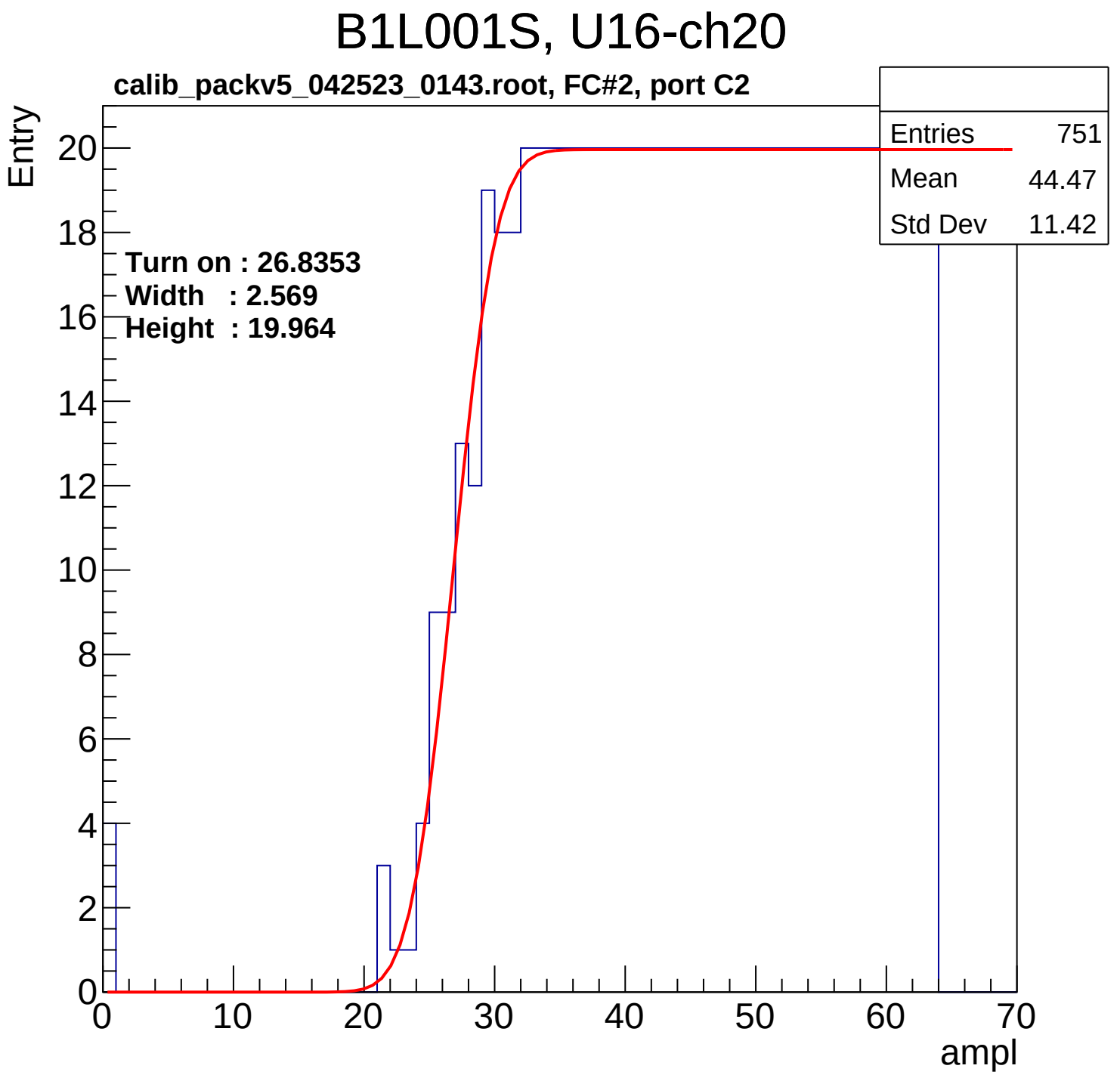
B1L001S, U16-ch20
calib_packv5_042523_0143.root, FC#2, port C2
Entries 751
Mean 44.47
Std Dev 11.42
Turn on : 26.8353
Width : 2.569
Height : 19.964
Entry
ampl
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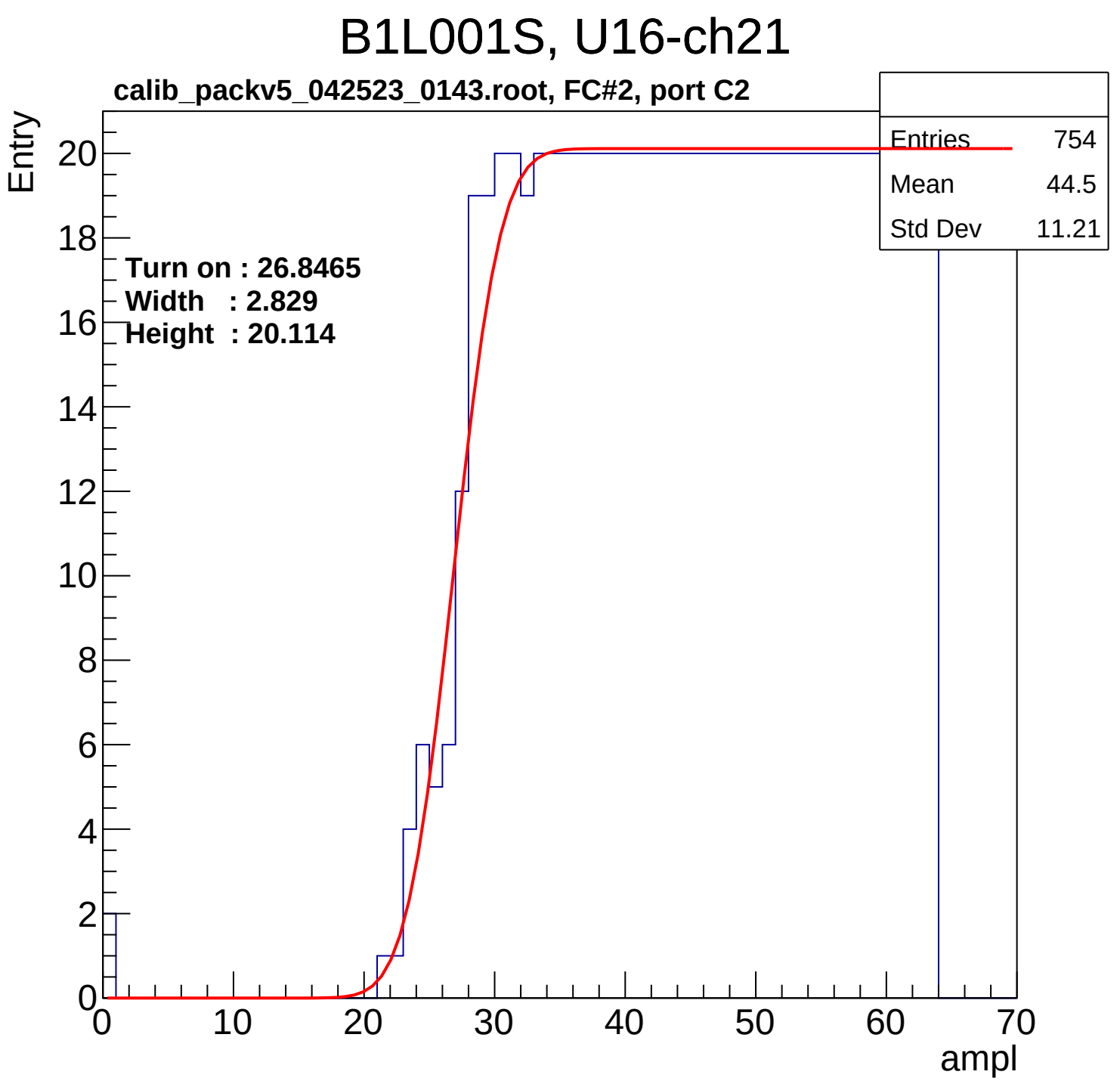
B1L001S, U16-ch21
calib_packv5_042523_0143.root, FC#2, port C2
Entries 754
Mean 44.5
Std Dev 11.21
Turn on : 26.8465
Width : 2.829
Height : 20.114
Entry
ampl
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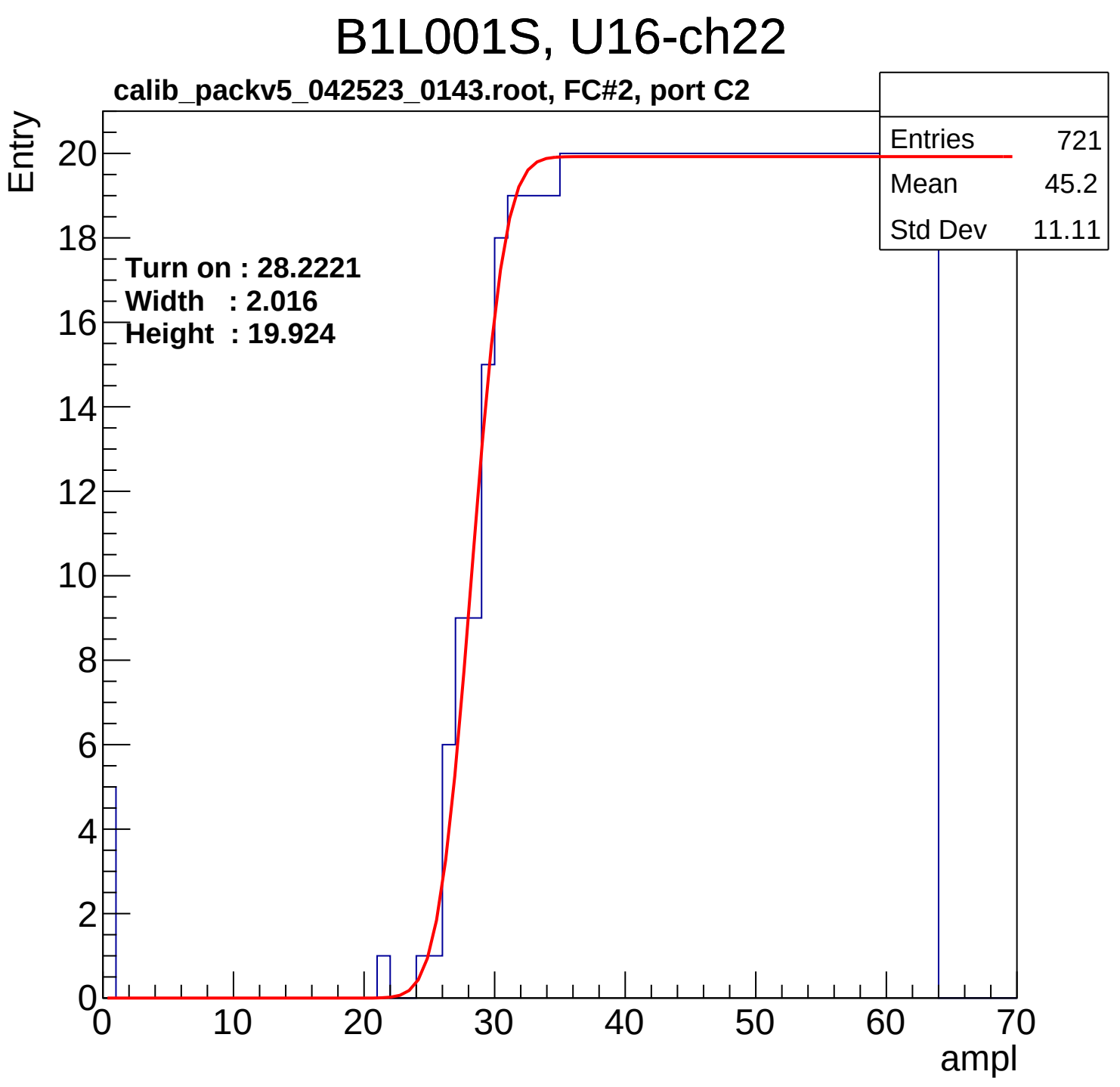
B1L001S, U16-ch22
calib_packv5_042523_0143.root, FC#2, port C2
Entries 721
Mean 45.2
Std Dev 11.11
Turn on : 28.2221
Width : 2.016
Height : 19.924
Entry
ampl
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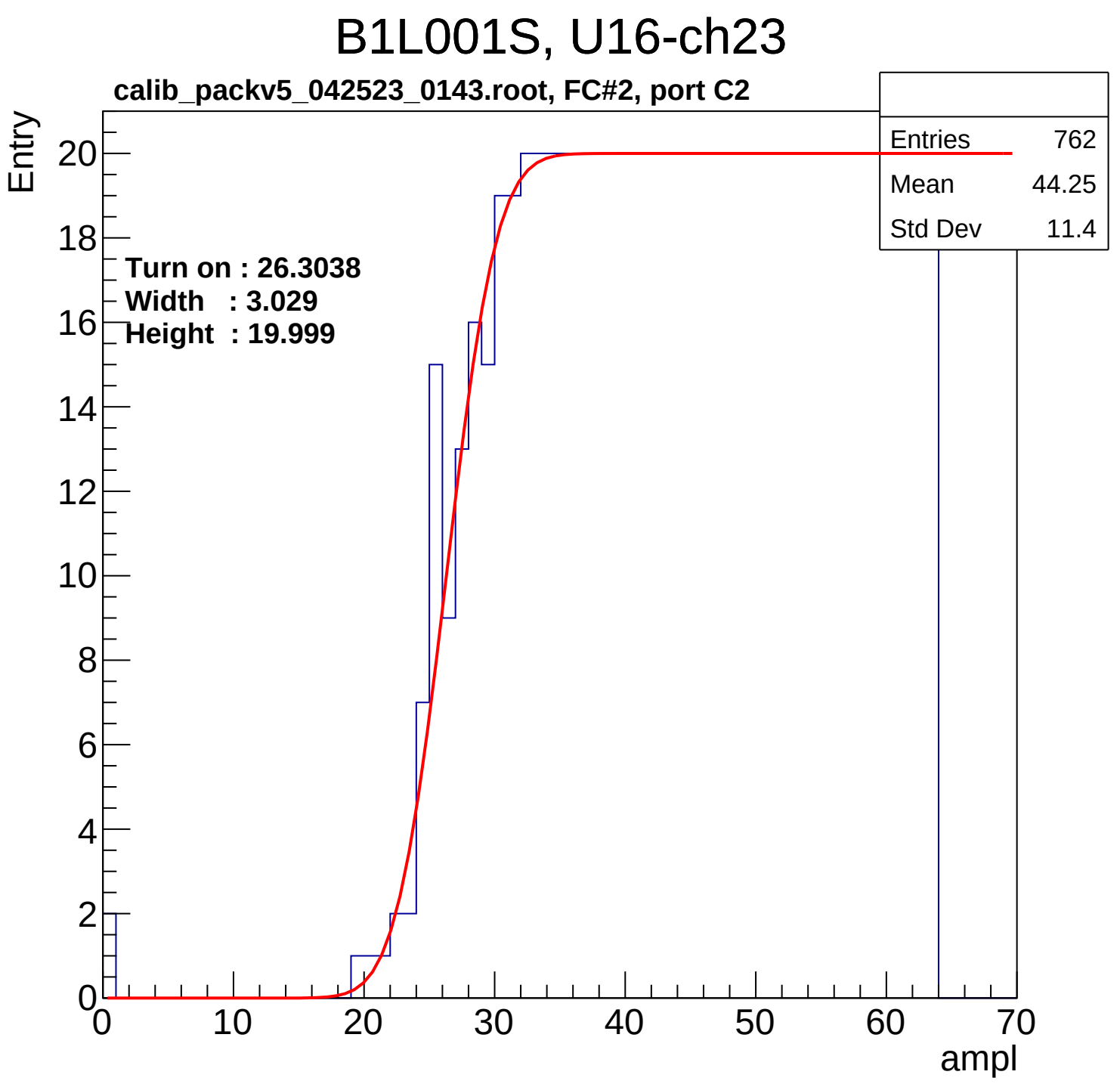
B1L001S, U16-ch23
calib_packv5_042523_0143.root, FC#2, port C2
Entries 762
Mean 44.25
Std Dev 11.4
Turn on : 26.3038
Width : 3.029
Height : 19.999
Entry
ampl
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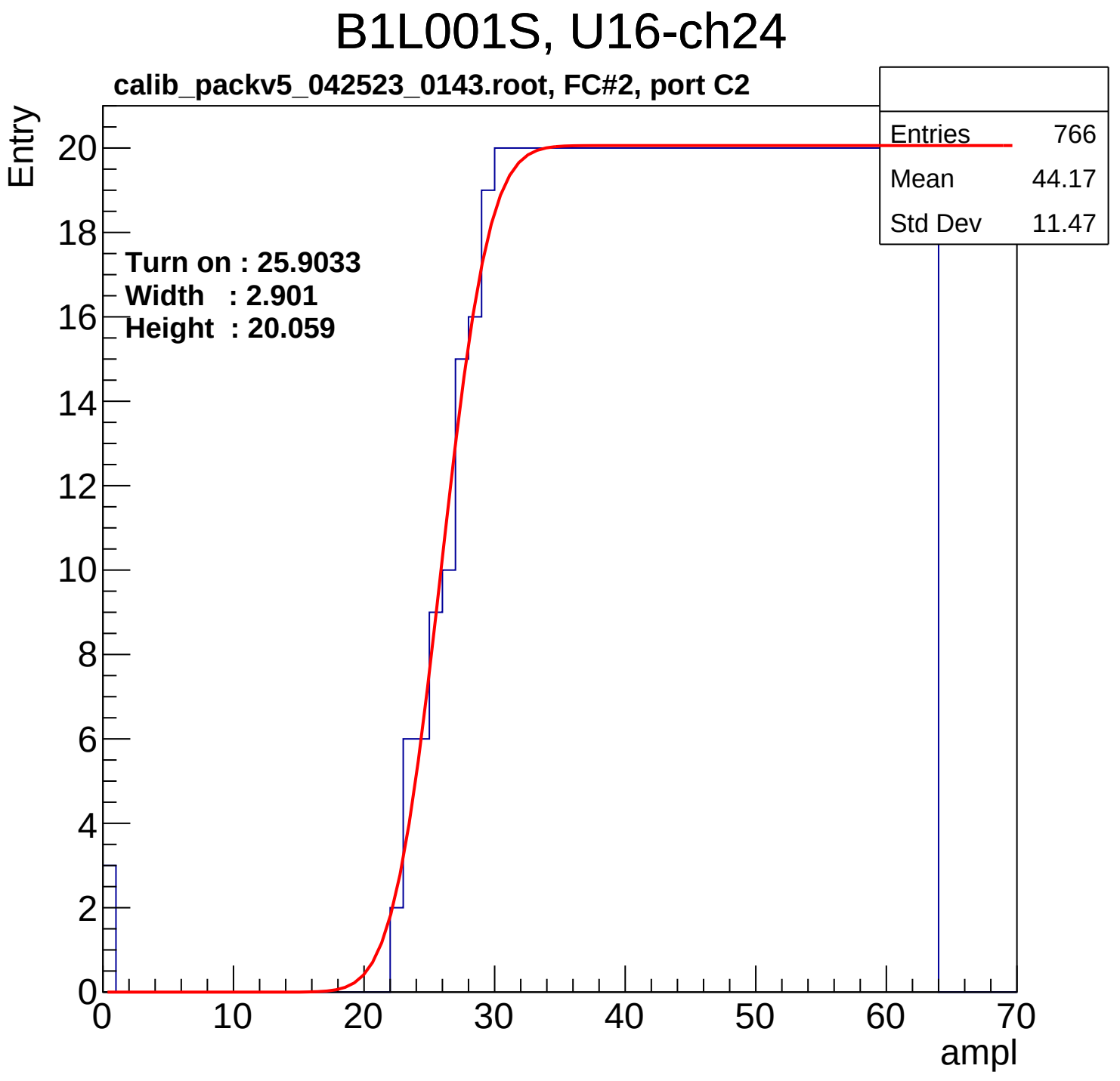
B1L001S, U16-ch24
calib_packv5_042523_0143.root, FC#2, port C2
Entries 766
Mean 44.17
Std Dev 11.47
Turn on : 25.9033
Width : 2.901
Height : 20.059
Entry
ampl
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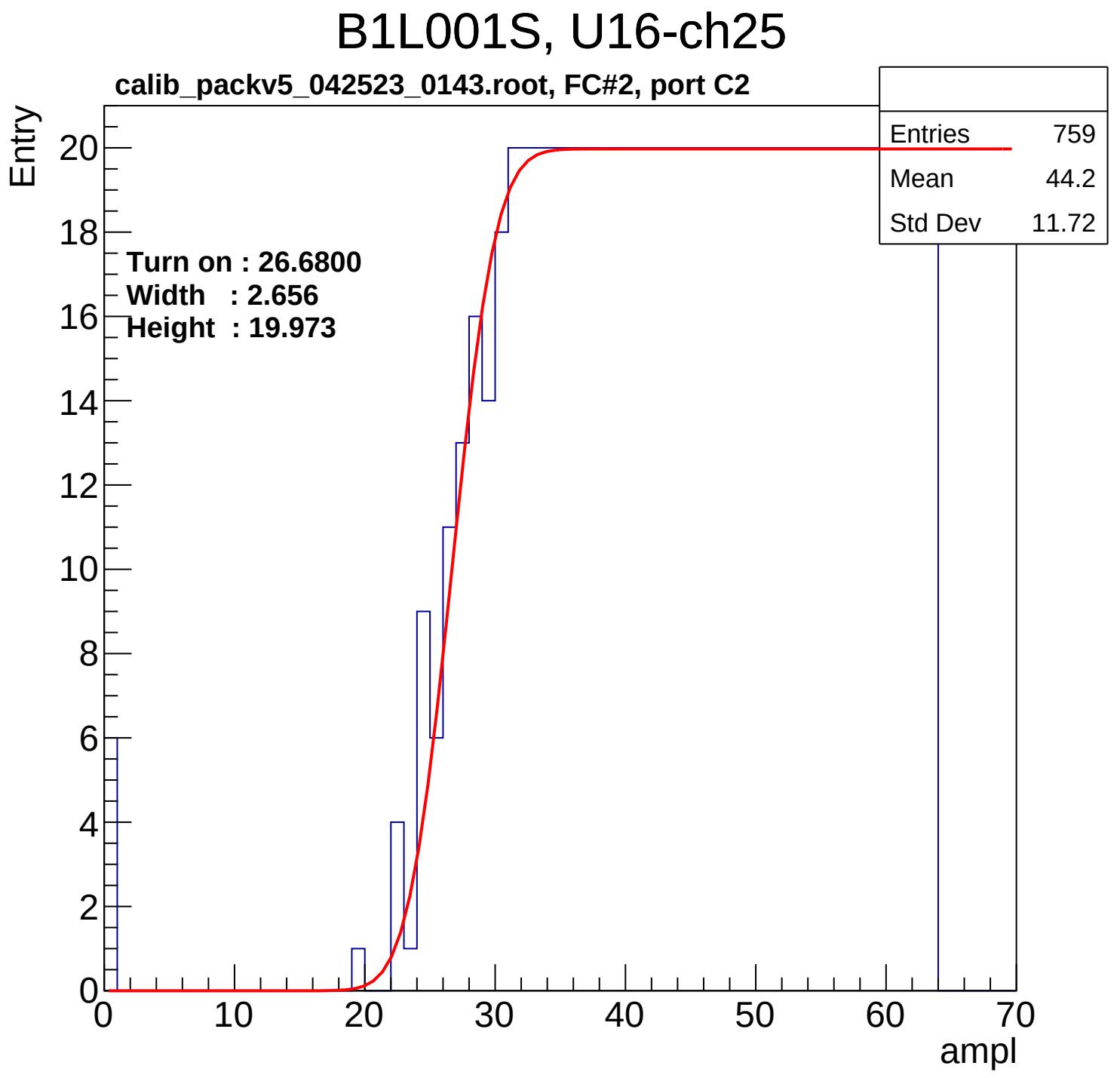
B1L001S, U16-ch25
calib_packv5_042523_0143.root, FC#2, port C2
Entries 759
Mean 44.2
Std Dev 11.72
Turn on : 26.6800
Width : 2.656
Height : 19.973
Entry
ampl
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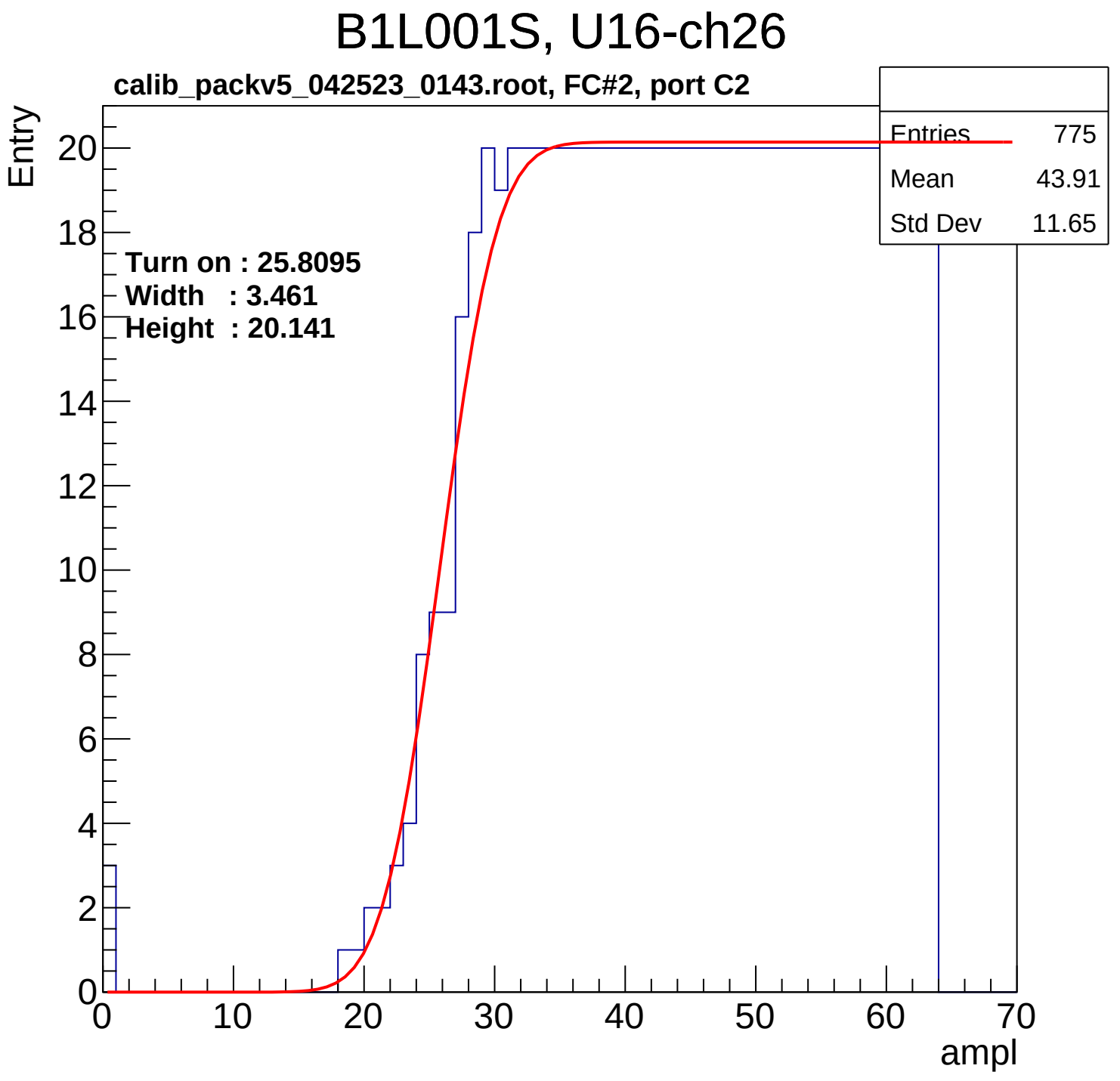
B1L001S, U16-ch26
calib_packv5_042523_0143.root, FC#2, port C2
Entries 775
Mean 43.91
Std Dev 11.65
Turn on : 25.8095
Width : 3.461
Height : 20.141
Entry
ampl
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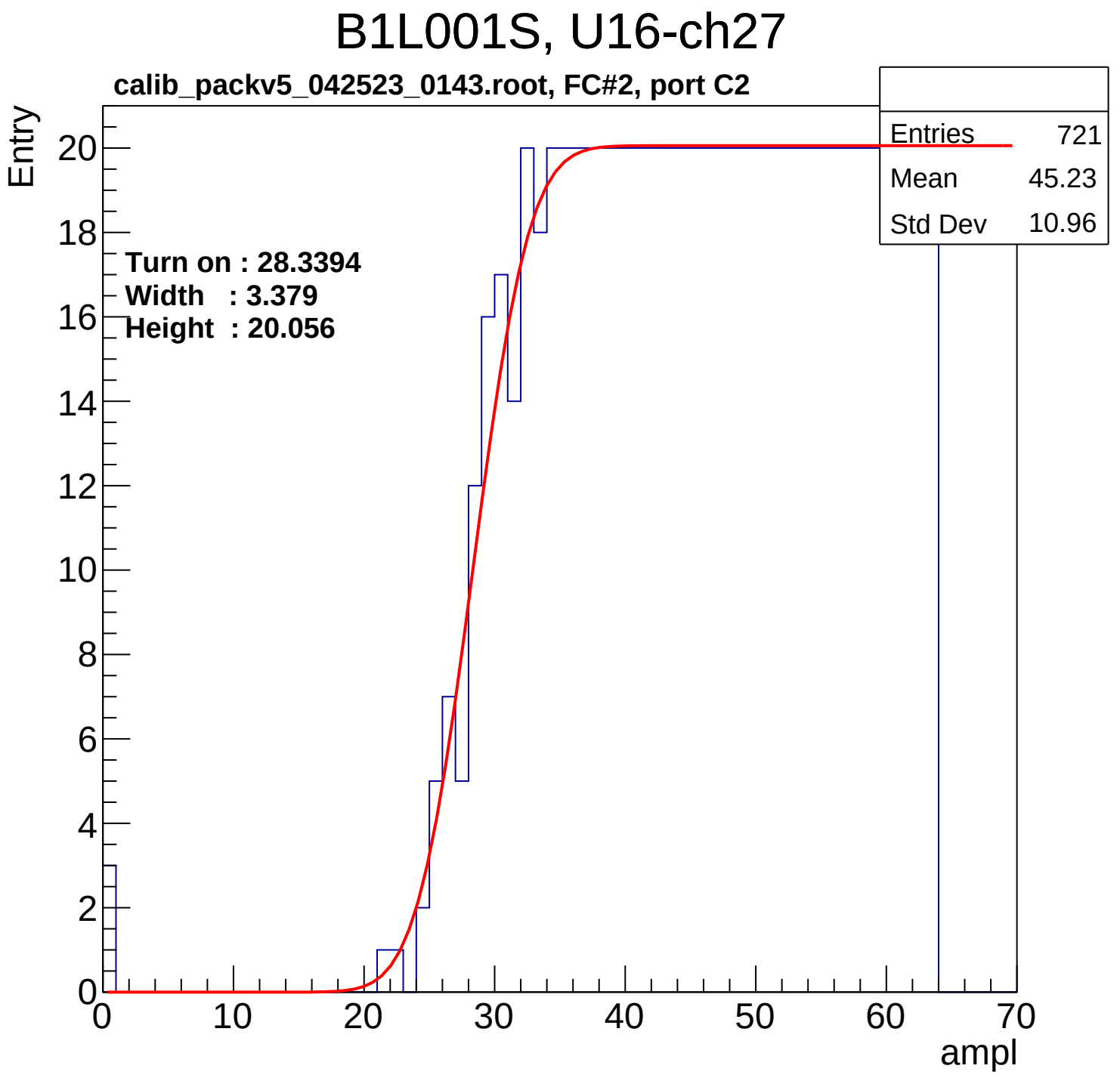
B1L001S, U16-ch27
calib_packv5_042523_0143.root, FC#2, port C2
Entries 721
Mean 45.23
Std Dev 10.96
Turn on : 28.3394
Width : 3.379
Height : 20.056
Entry
ampl
0
2
4
6
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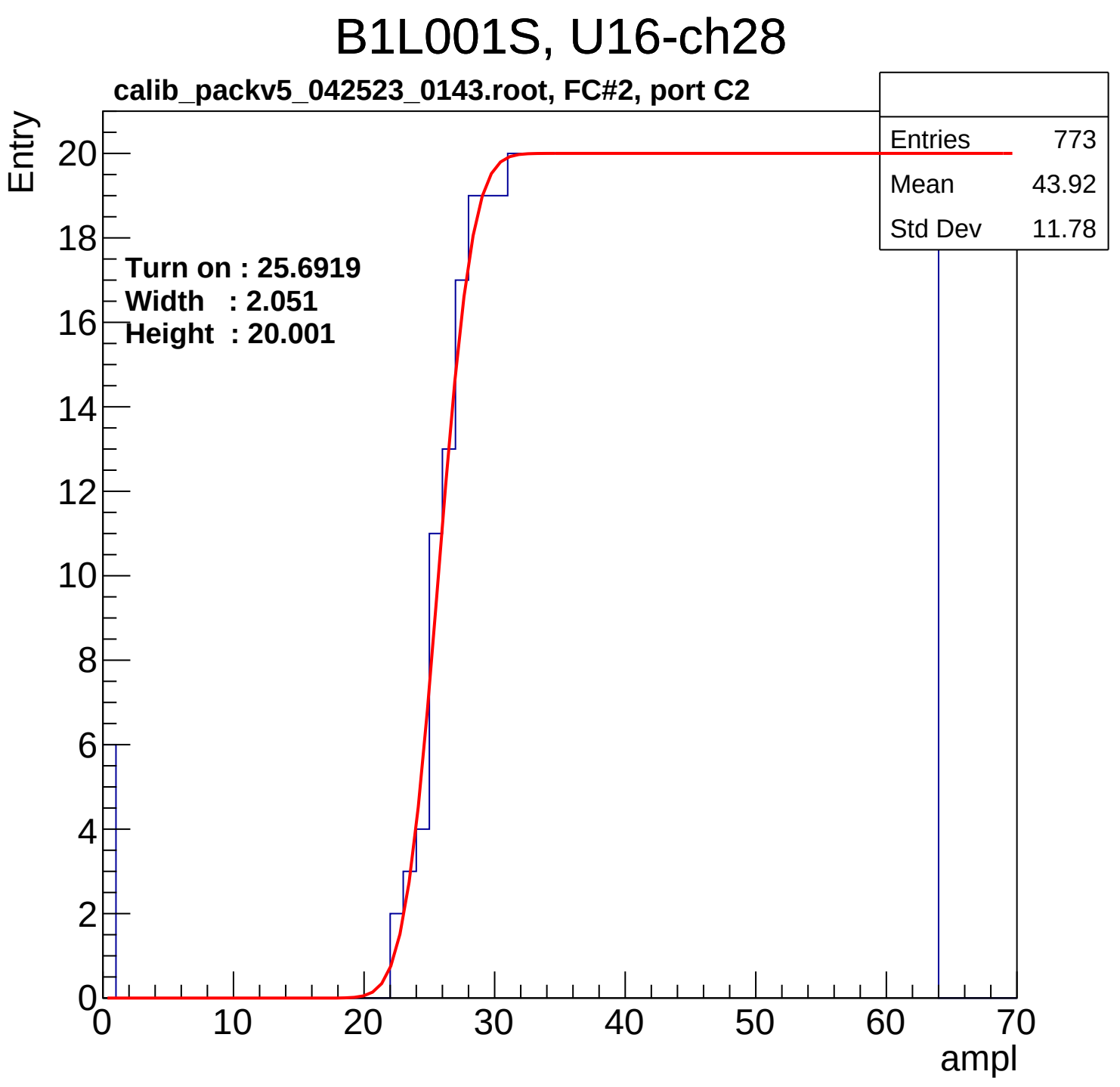
B1L001S, U16-ch28
calib_packv5_042523_0143.root, FC#2, port C2
Entries 773
Mean 43.92
Std Dev 11.78
Turn on : 25.6919
Width : 2.051
Height : 20.001
Entry
ampl
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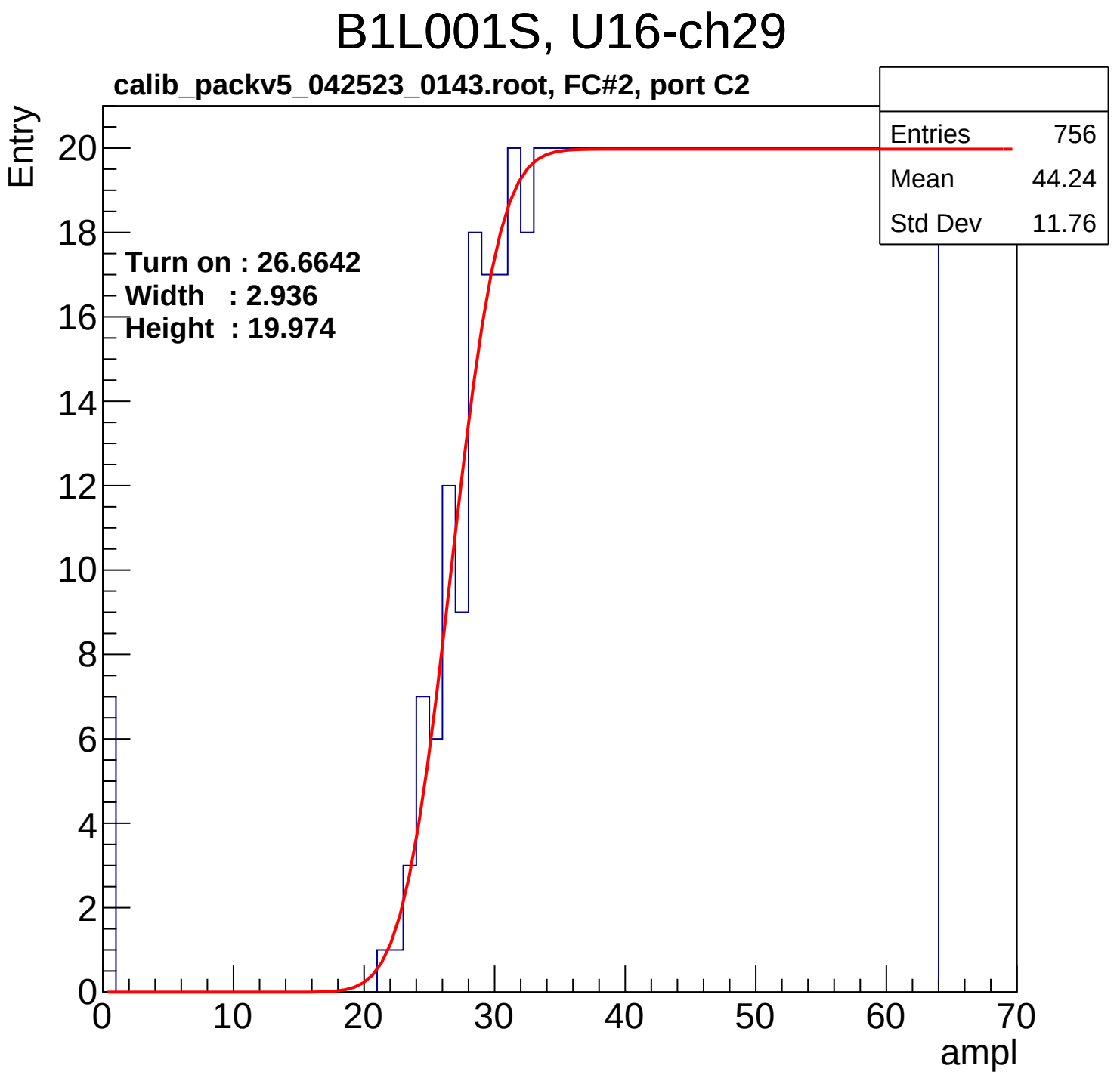
B1L001S, U16-ch29
calib_packv5_042523_0143.root, FC#2, port C2
Entries 756
Mean 44.24
Std Dev 11.76
Turn on : 26.6642
Width : 2.936
Height : 19.974
Entry
ampl
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6
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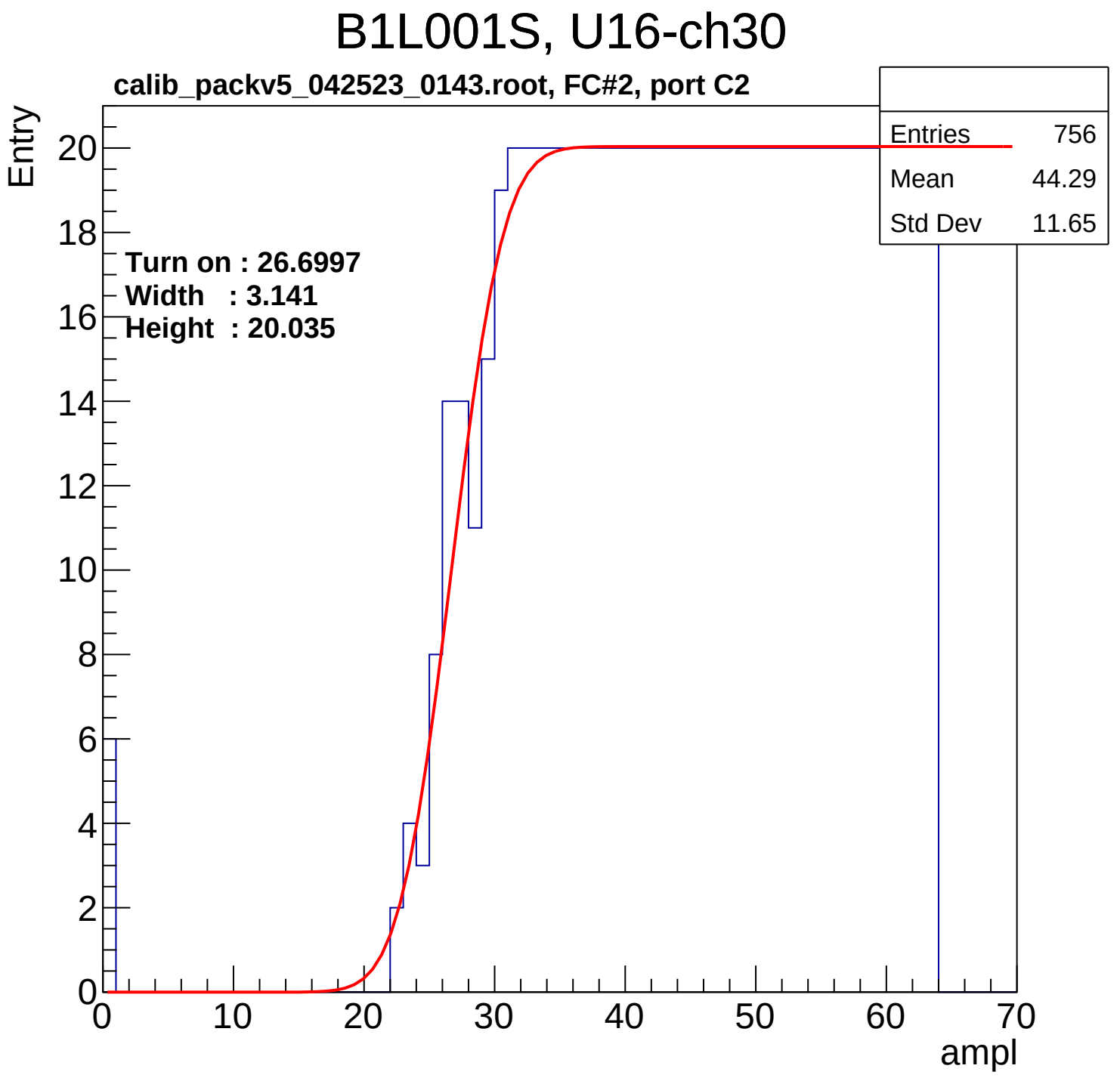
B1L001S, U16-ch30
calib_packv5_042523_0143.root, FC#2, port C2
Entries 756
Mean 44.29
Std Dev 11.65
Turn on : 26.6997
Width : 3.141
Height : 20.035
Entry
ampl
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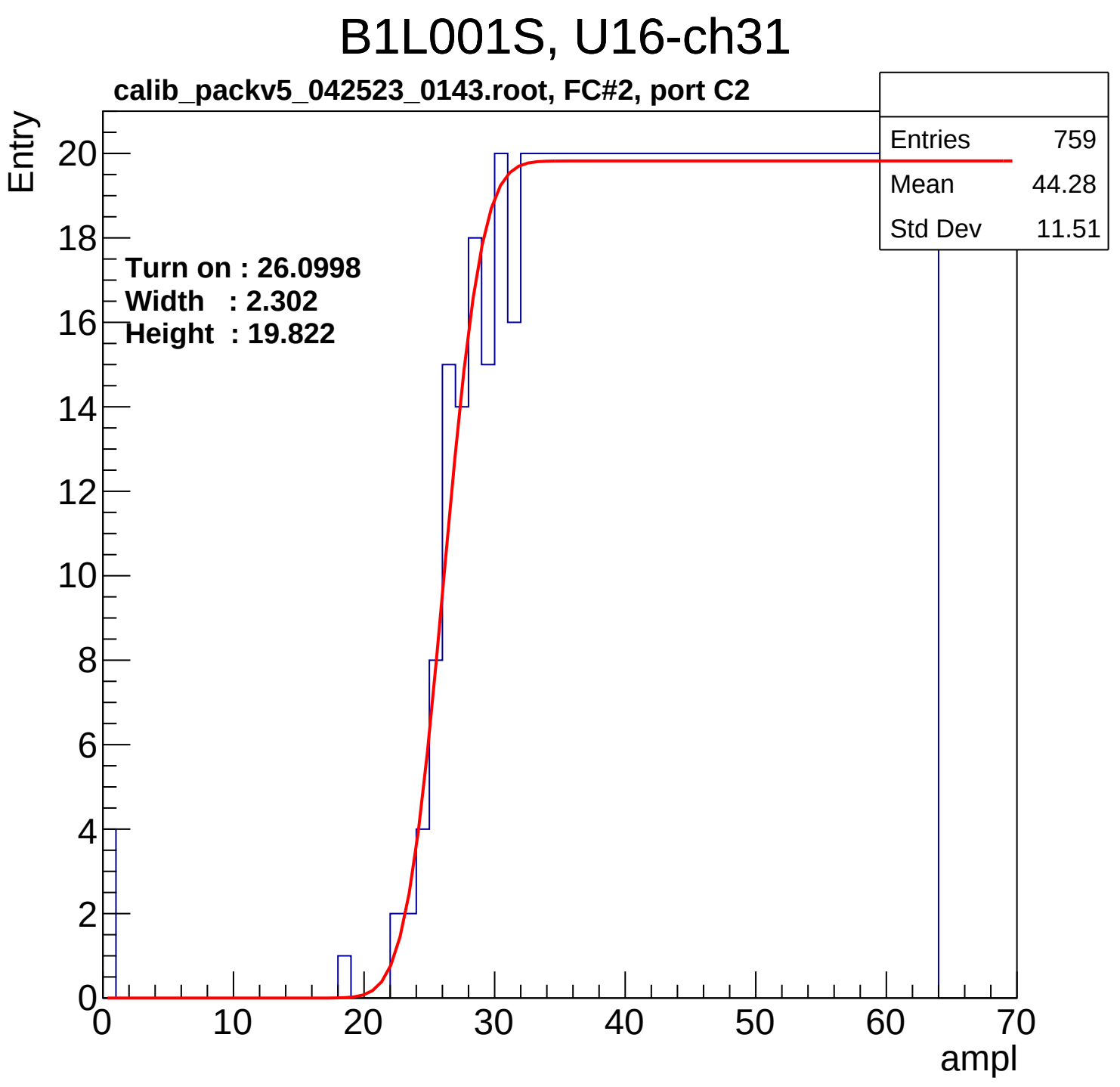
B1L001S, U16-ch31
calib_packv5_042523_0143.root, FC#2, port C2
Entries 759
Mean 44.28
Std Dev 11.51
Turn on : 26.0998
Width : 2.302
Height : 19.822
Entry
ampl
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6
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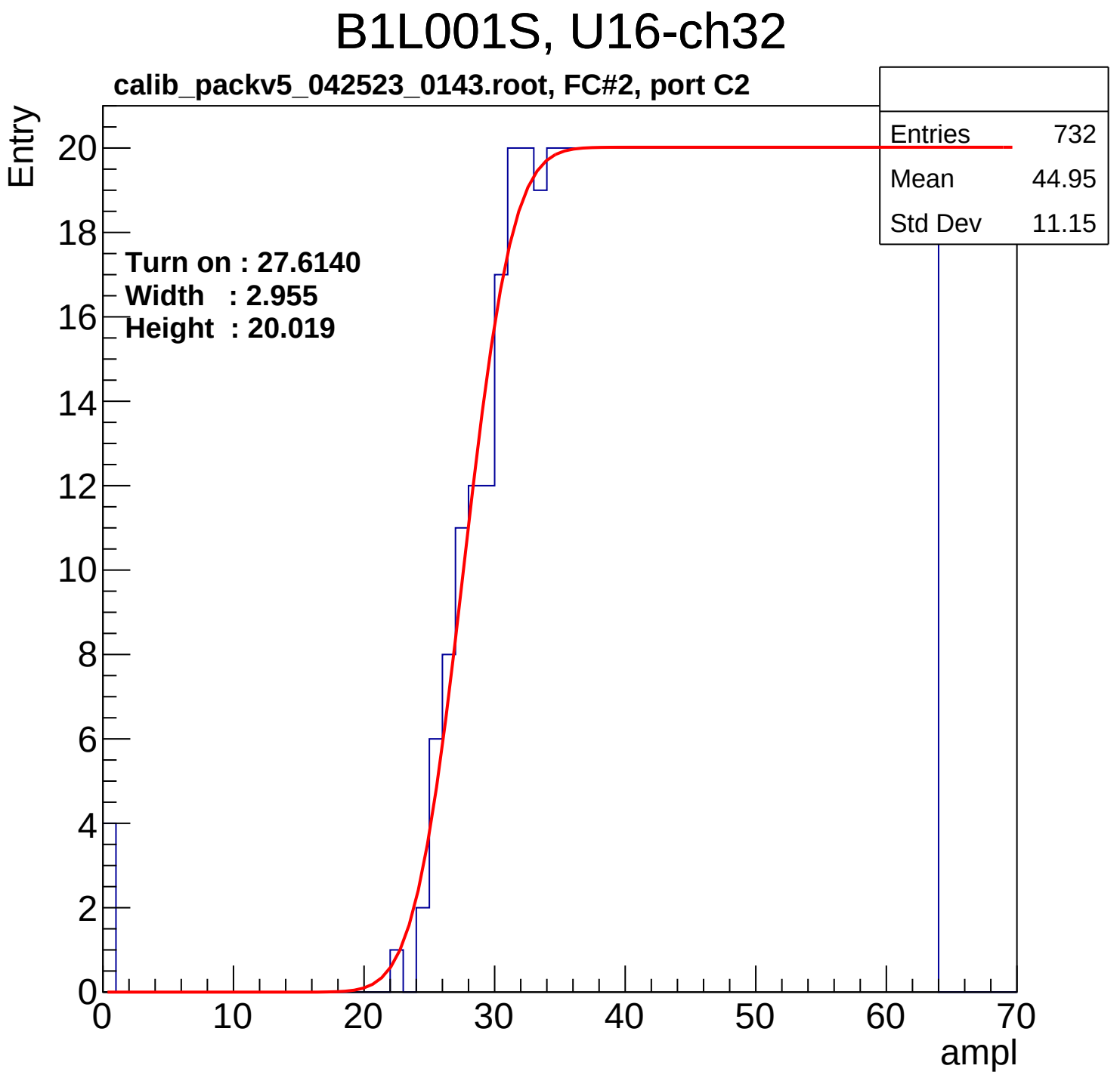
B1L001S, U16-ch32
calib_packv5_042523_0143.root, FC#2, port C2
Entries 732
Mean 44.95
Std Dev 11.15
Turn on : 27.6140
Width : 2.955
Height : 20.019
Entry
ampl
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6
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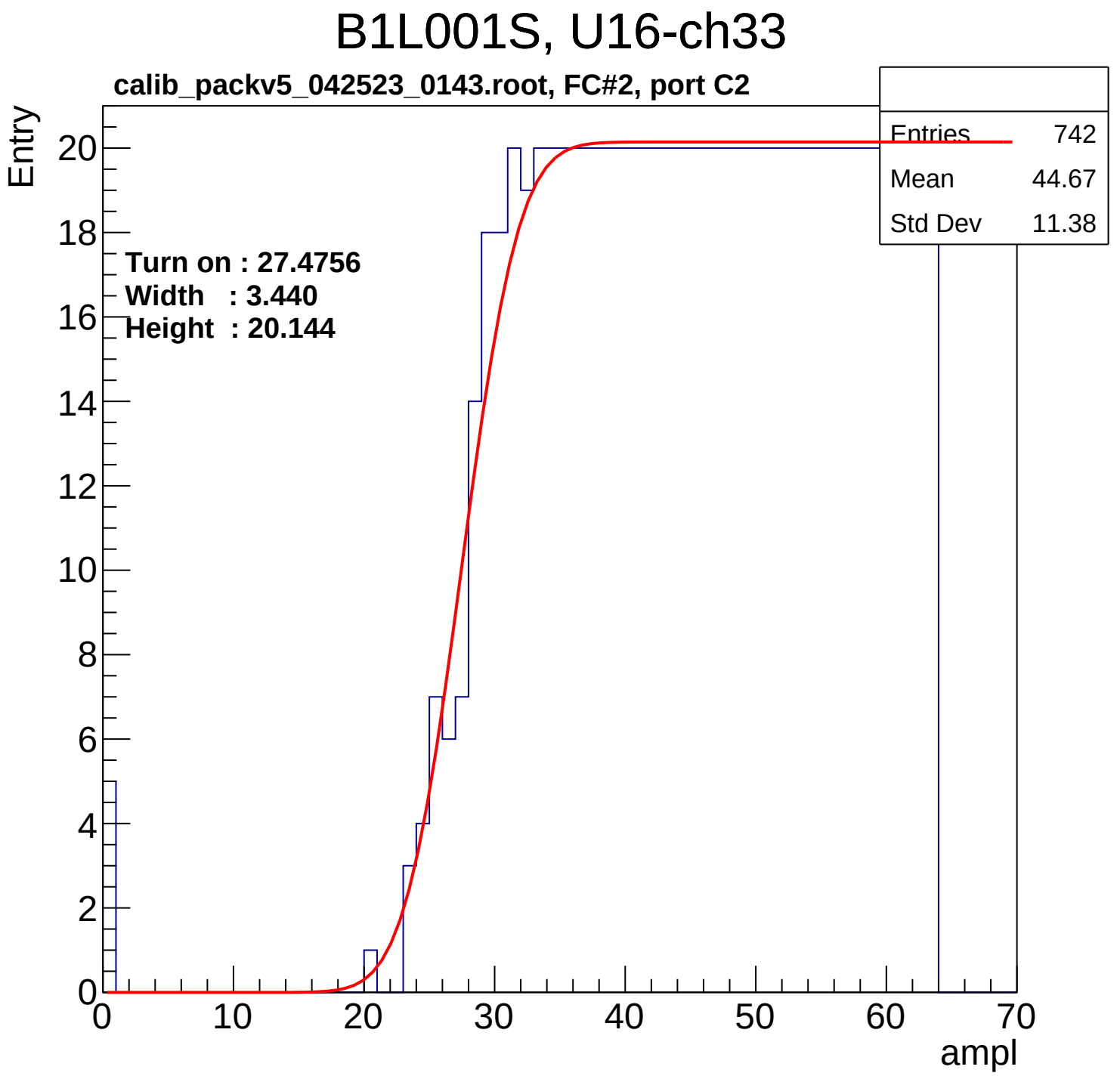
B1L001S, U16-ch33
calib_packv5_042523_0143.root, FC#2, port C2
Entries 742
Mean 44.67
Std Dev 11.38
Turn on : 27.4756
Width : 3.440
Height : 20.144
Entry
ampl
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6
8
10
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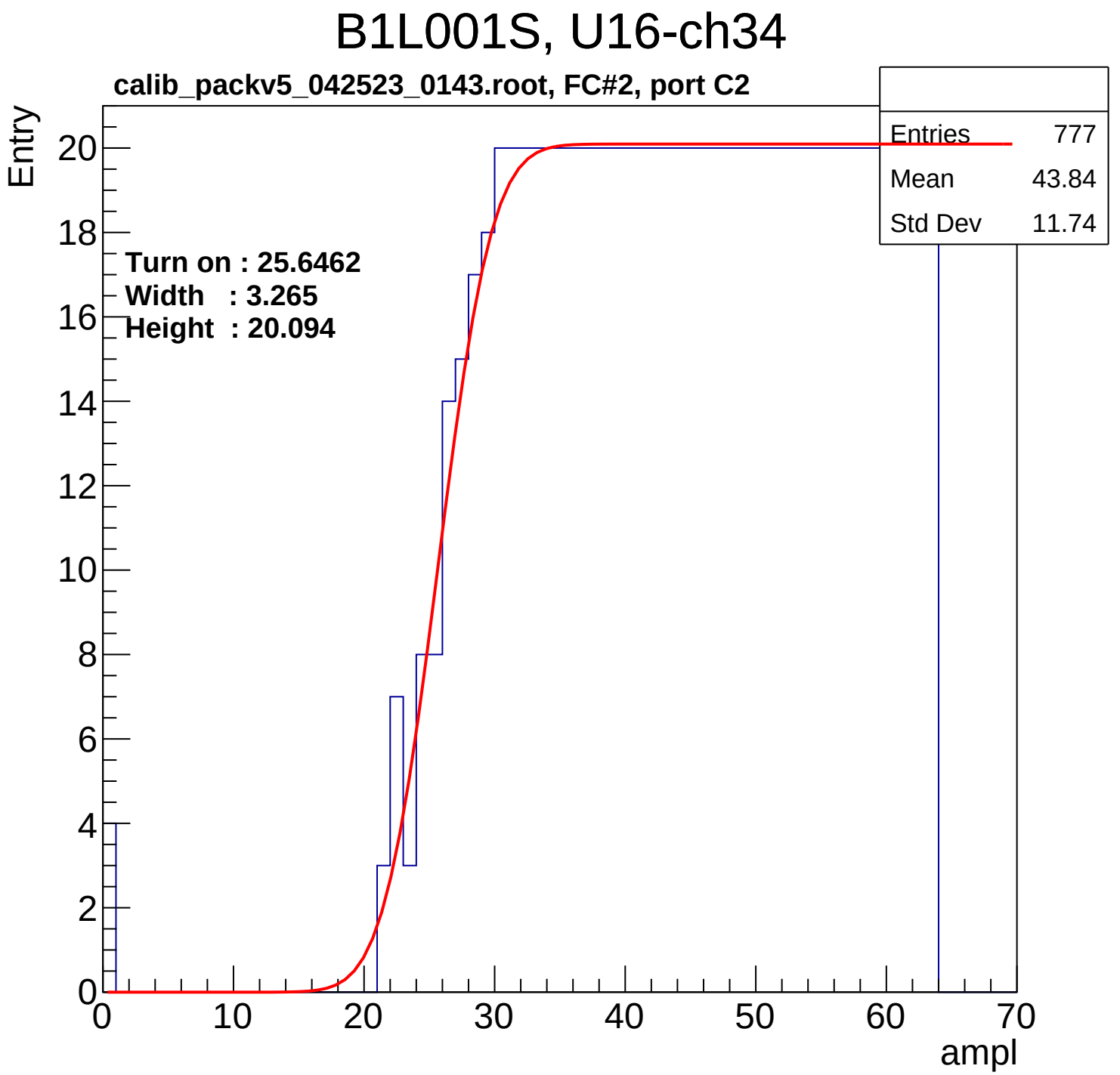
B1L001S, U16-ch34
calib_packv5_042523_0143.root, FC#2, port C2
Entries 777
Mean 43.84
Std Dev 11.74
Turn on : 25.6462
Width : 3.265
Height : 20.094
Entry
ampl
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6
8
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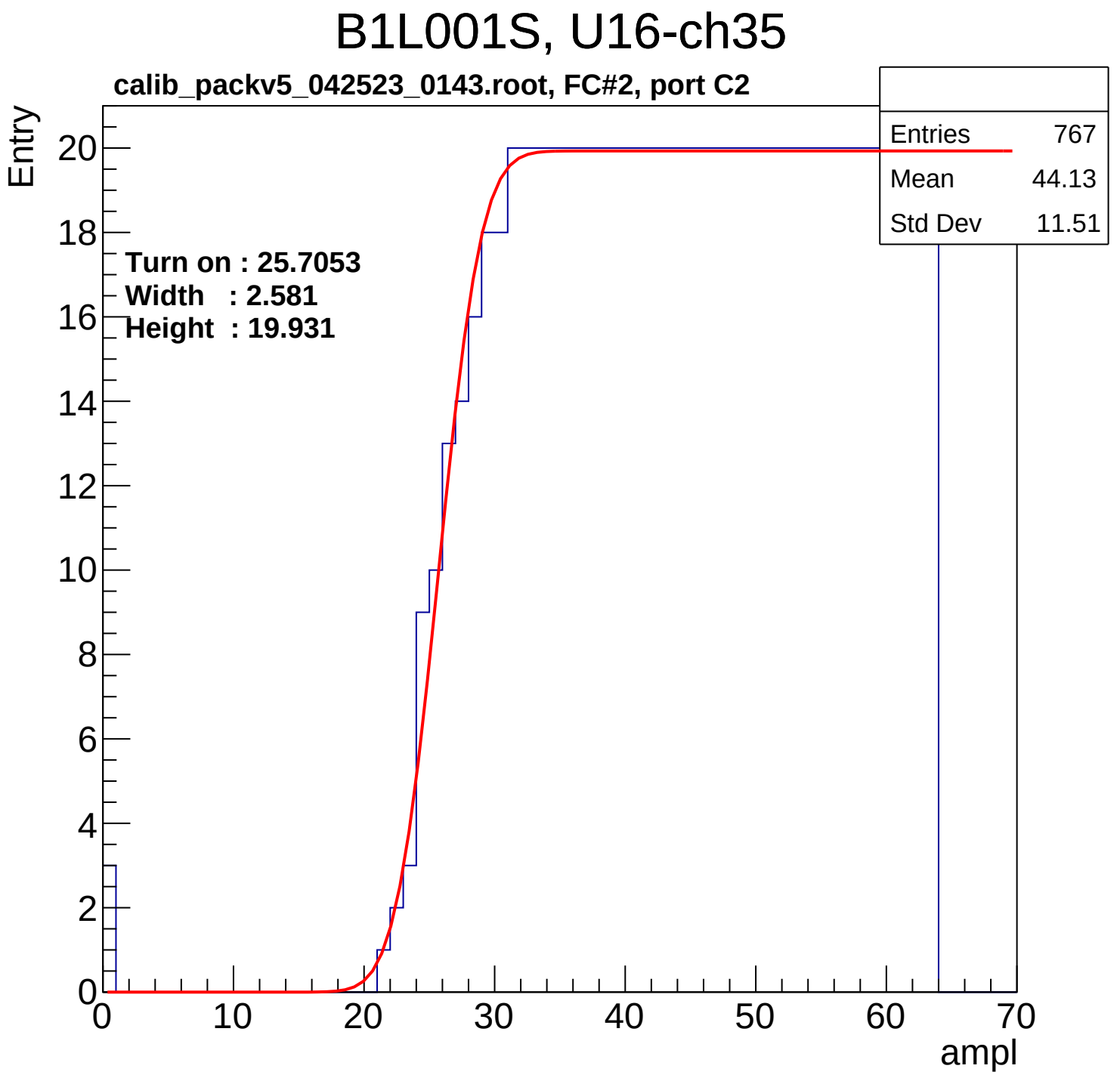
B1L001S, U16-ch35
calib_packv5_042523_0143.root, FC#2, port C2
Entries 767
Mean 44.13
Std Dev 11.51
Turn on : 25.7053
Width : 2.581
Height : 19.931
Entry
ampl
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6
8
10
12
14
16
18
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0
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60
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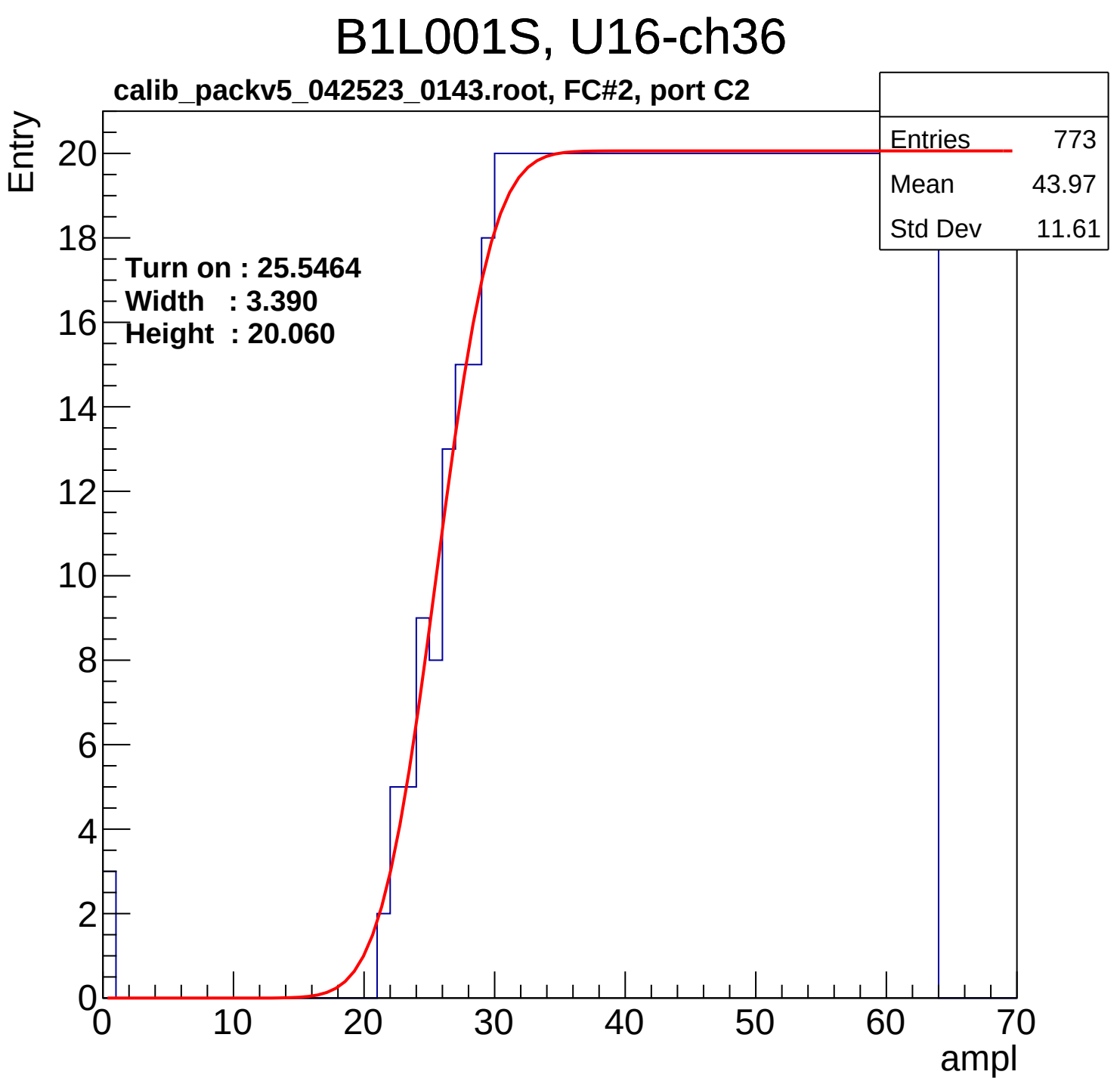
B1L001S, U16-ch36
calib_packv5_042523_0143.root, FC#2, port C2
Entries 773
Mean 43.97
Std Dev 11.61
Turn on : 25.5464
Width : 3.390
Height : 20.060
Entry
ampl
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6
8
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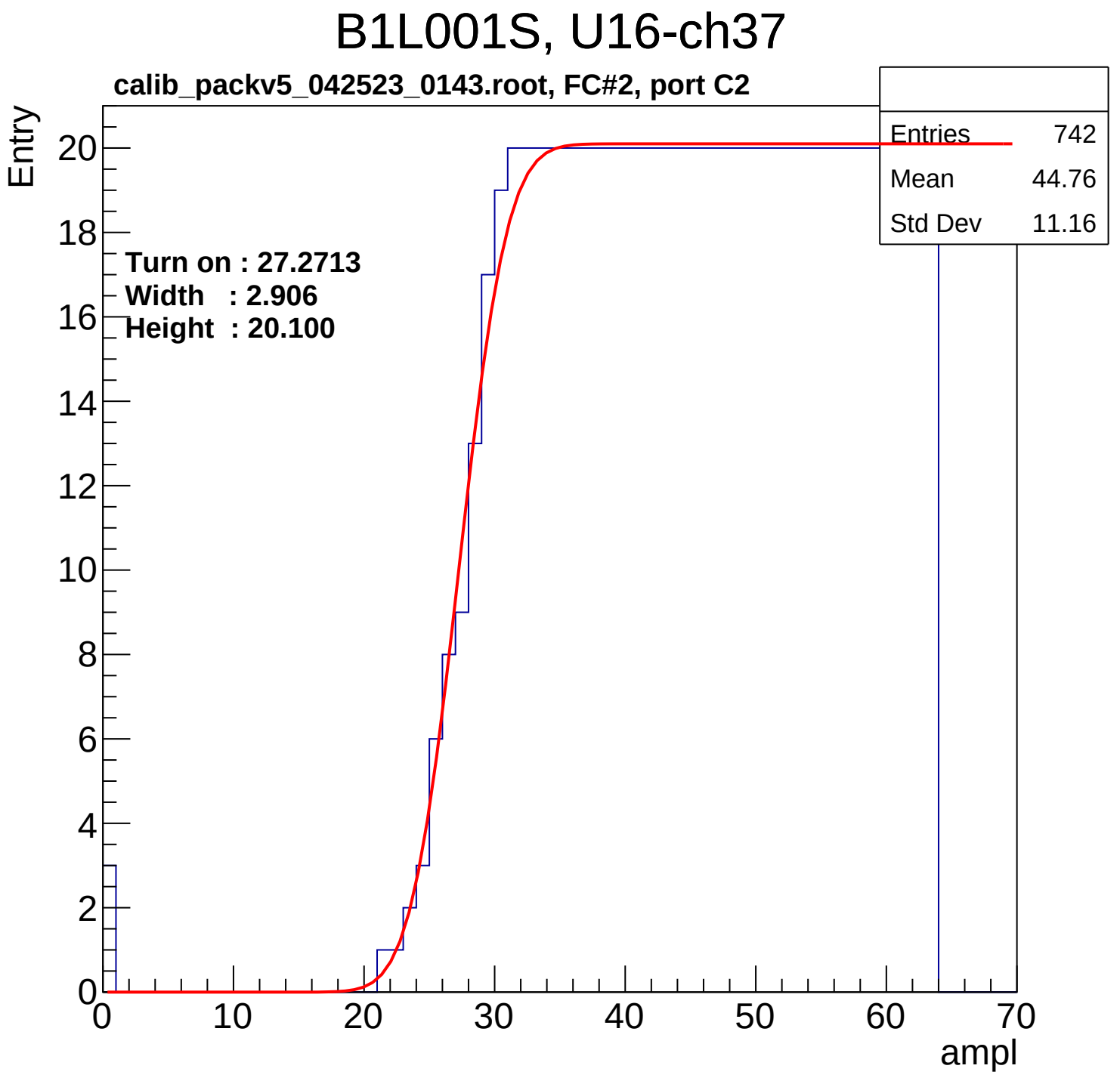
B1L001S, U16-ch37
calib_packv5_042523_0143.root, FC#2, port C2
Entries 742
Mean 44.76
Std Dev 11.16
Turn on : 27.2713
Width : 2.906
Height : 20.100
Entry
ampl
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6
8
10
12
14
16
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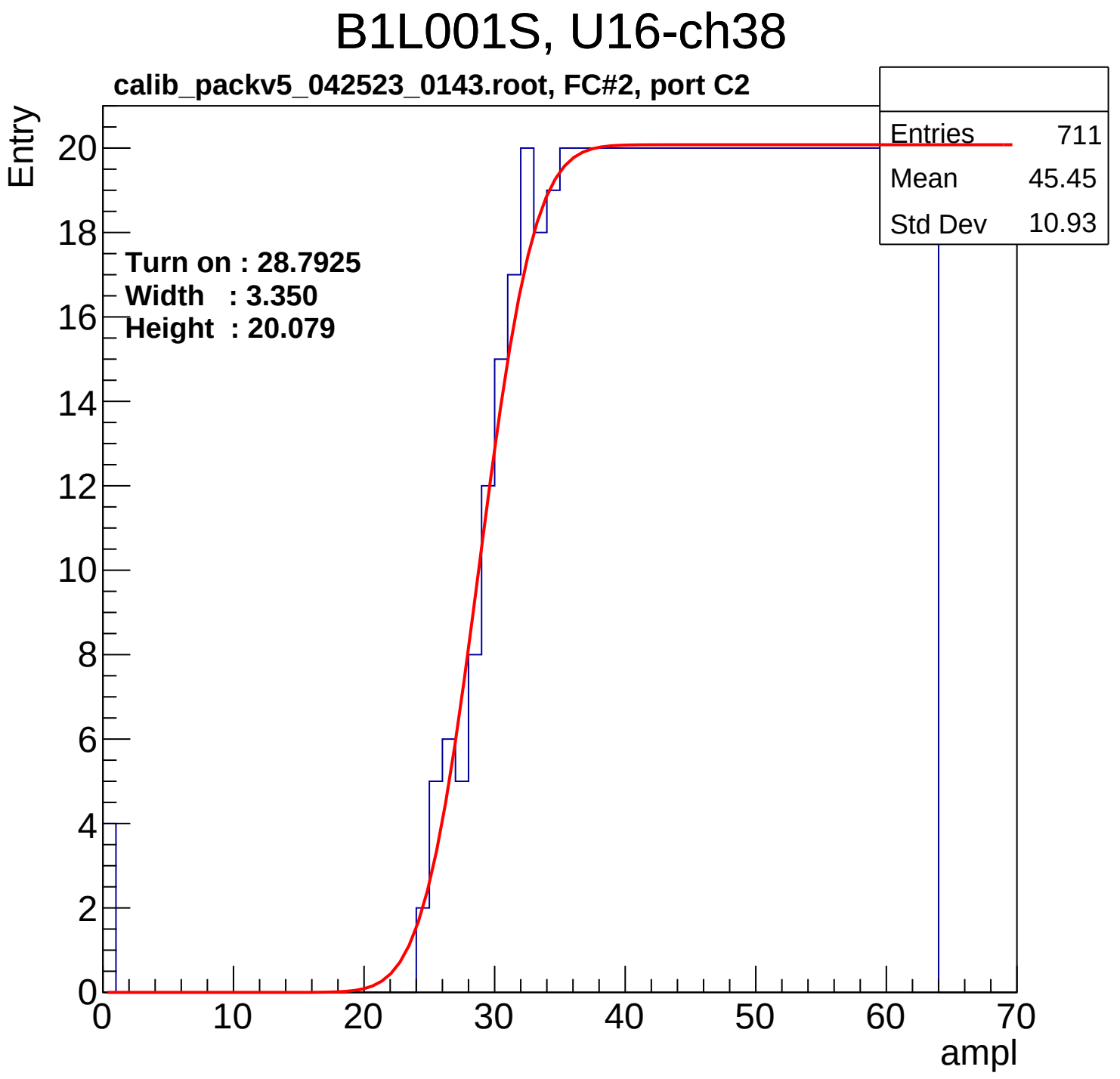
B1L001S, U16-ch38
calib_packv5_042523_0143.root, FC#2, port C2
Entry
Entries 711
Mean 45.45
Std Dev 10.93
Turn on : 28.7925
Width : 3.350
Height : 20.079
0
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8
10
12
14
16
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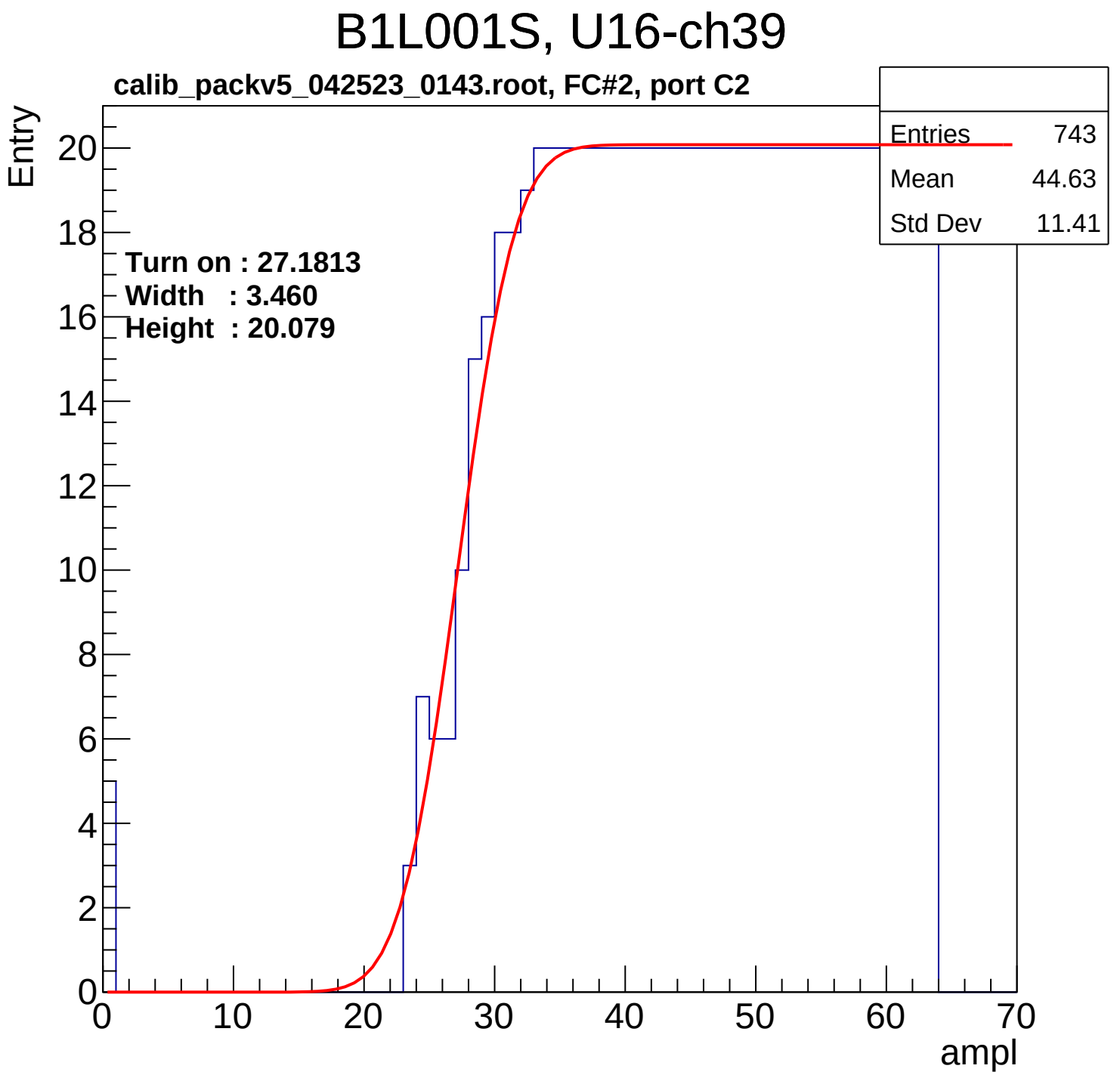
70
ampl


B1L001S, U16-ch39
calib_packv5_042523_0143.root, FC#2, port C2
Entries 743
Mean 44.63
Std Dev 11.41
Turn on : 27.1813
Width : 3.460
Height : 20.079
Entry
ampl
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6
8
10
12
14
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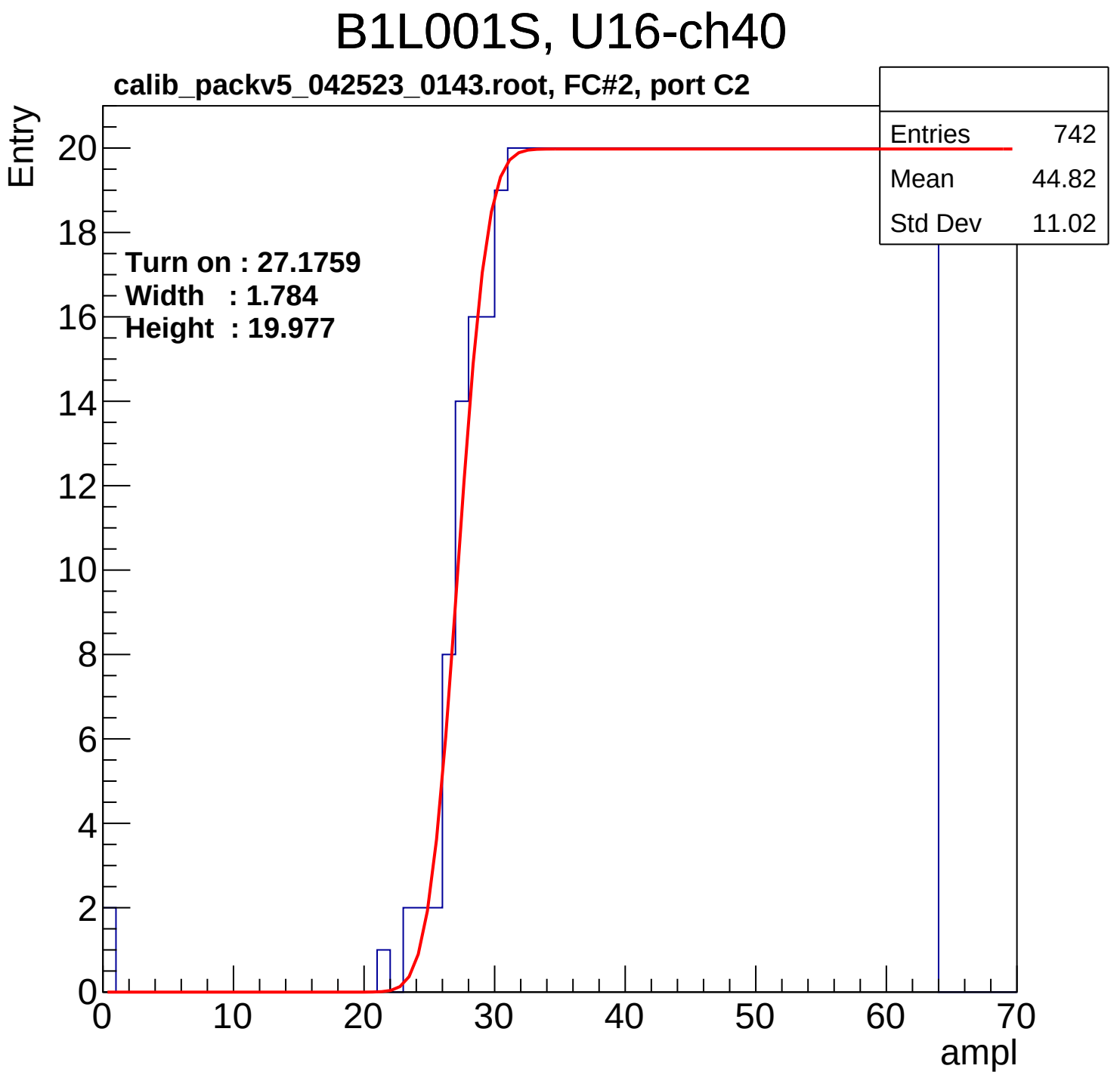
B1L001S, U16-ch40
calib_packv5_042523_0143.root, FC#2, port C2
Entries 742
Mean 44.82
Std Dev 11.02
Turn on : 27.1759
Width : 1.784
Height : 19.977
Entry
ampl
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6
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12
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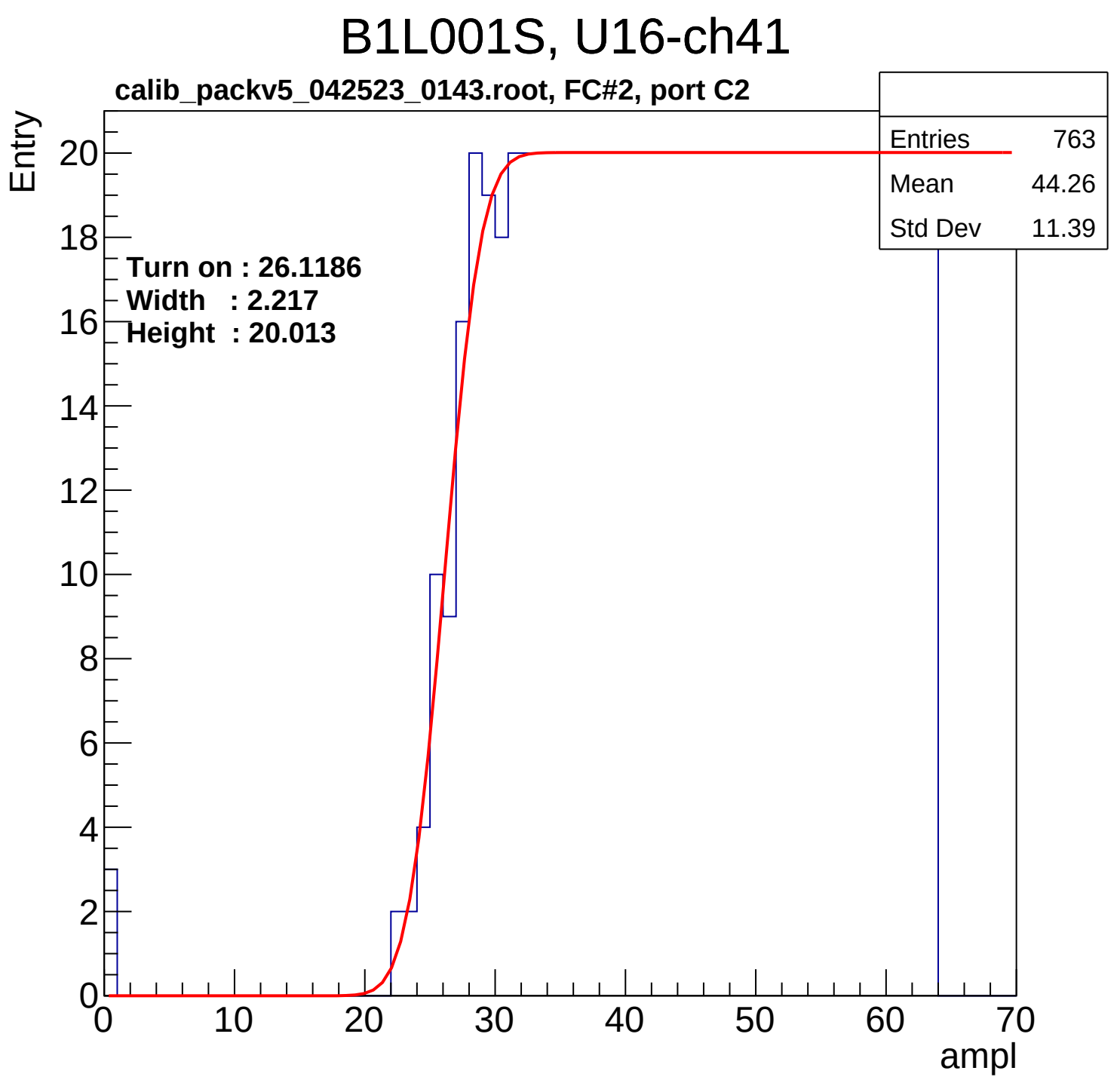
B1L001S, U16-ch41
calib_packv5_042523_0143.root, FC#2, port C2
Entries 763
Mean 44.26
Std Dev 11.39
Turn on : 26.1186
Width : 2.217
Height : 20.013
Entry
ampl
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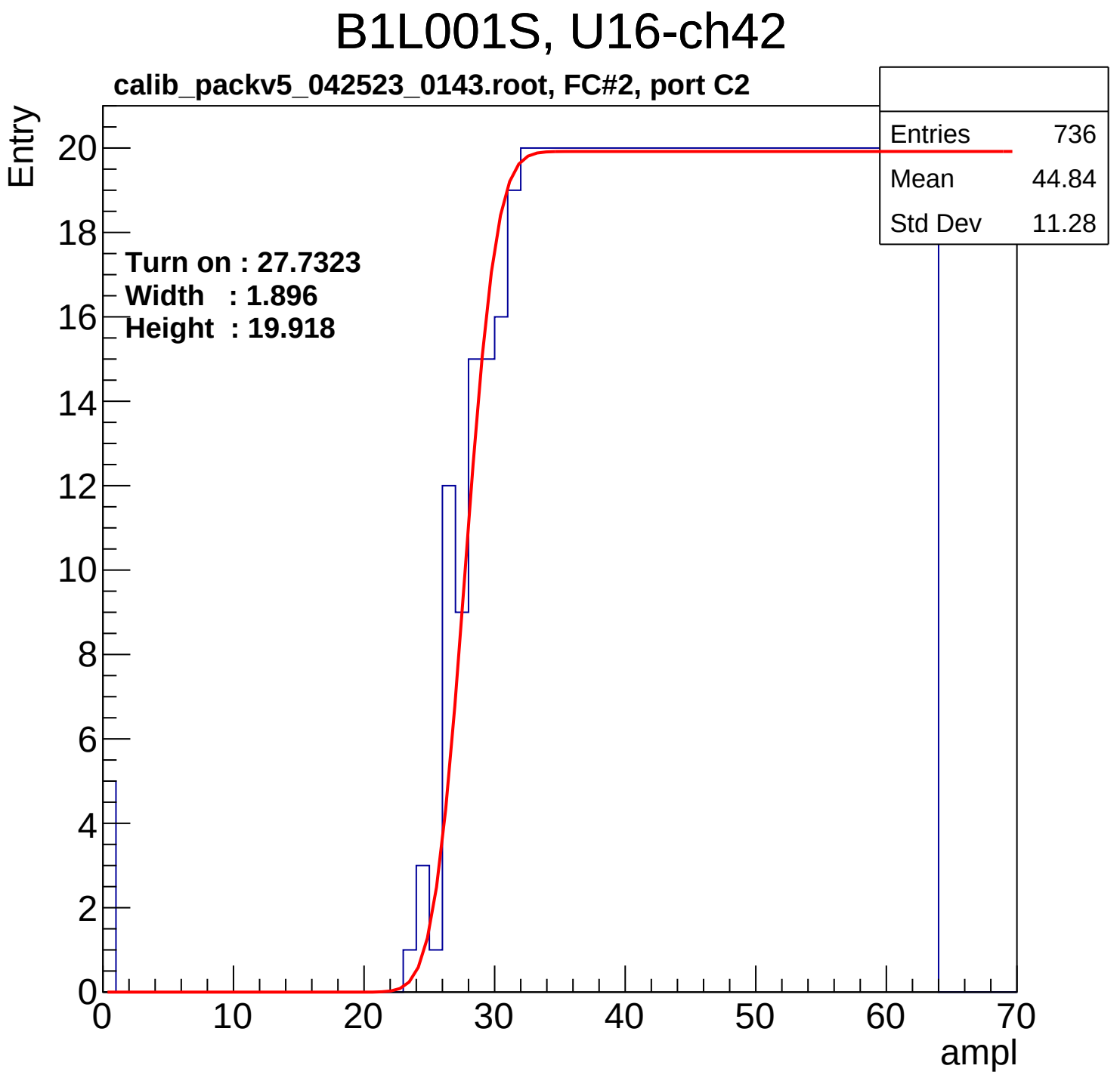
B1L001S, U16-ch42
calib_packv5_042523_0143.root, FC#2, port C2
Entries 736
Mean 44.84
Std Dev 11.28
Turn on : 27.7323
Width : 1.896
Height : 19.918
Entry
ampl
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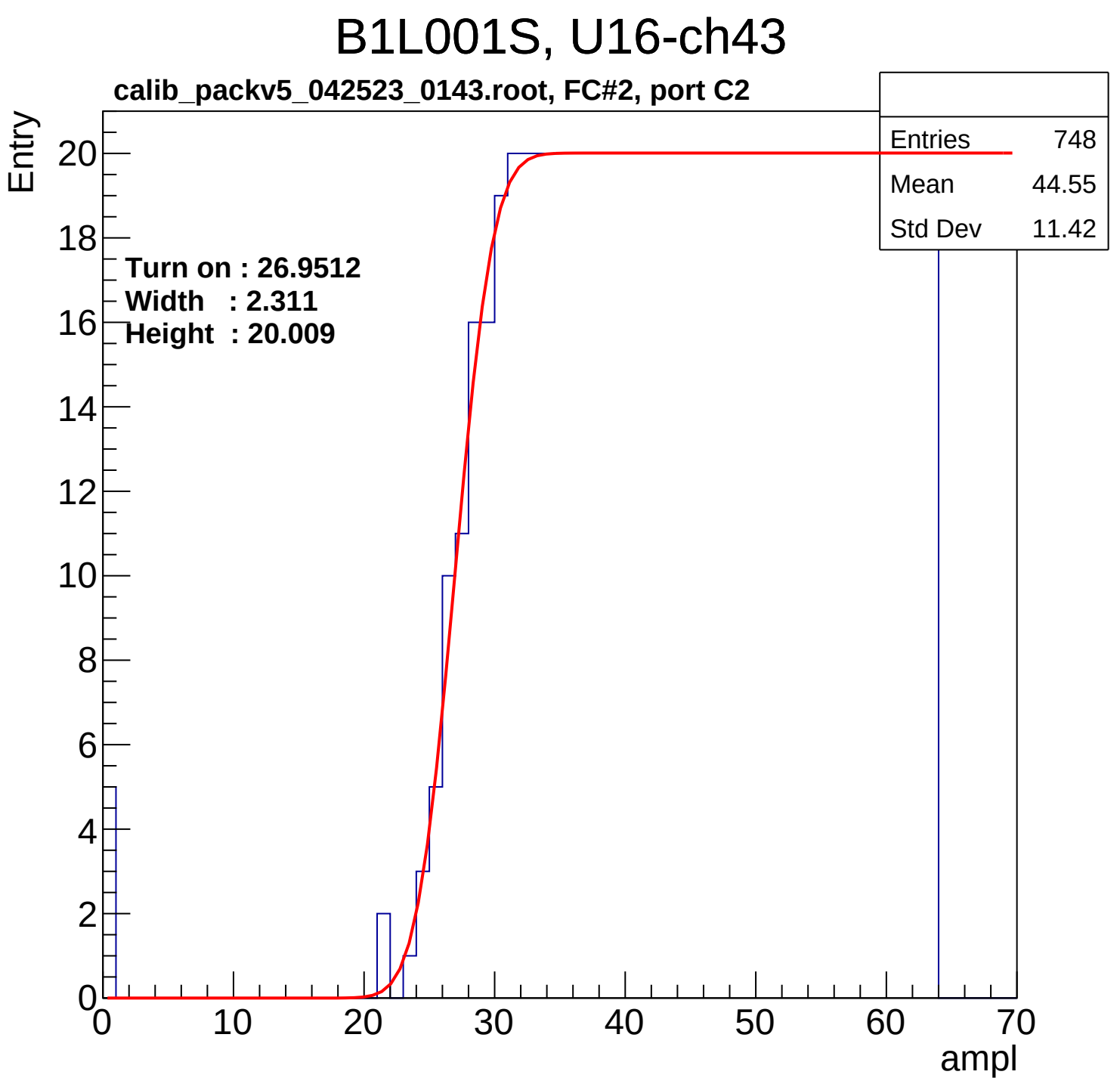
B1L001S, U16-ch43
calib_packv5_042523_0143.root, FC#2, port C2
Entries 748
Mean 44.55
Std Dev 11.42
Turn on : 26.9512
Width : 2.311
Height : 20.009
Entry
ampl
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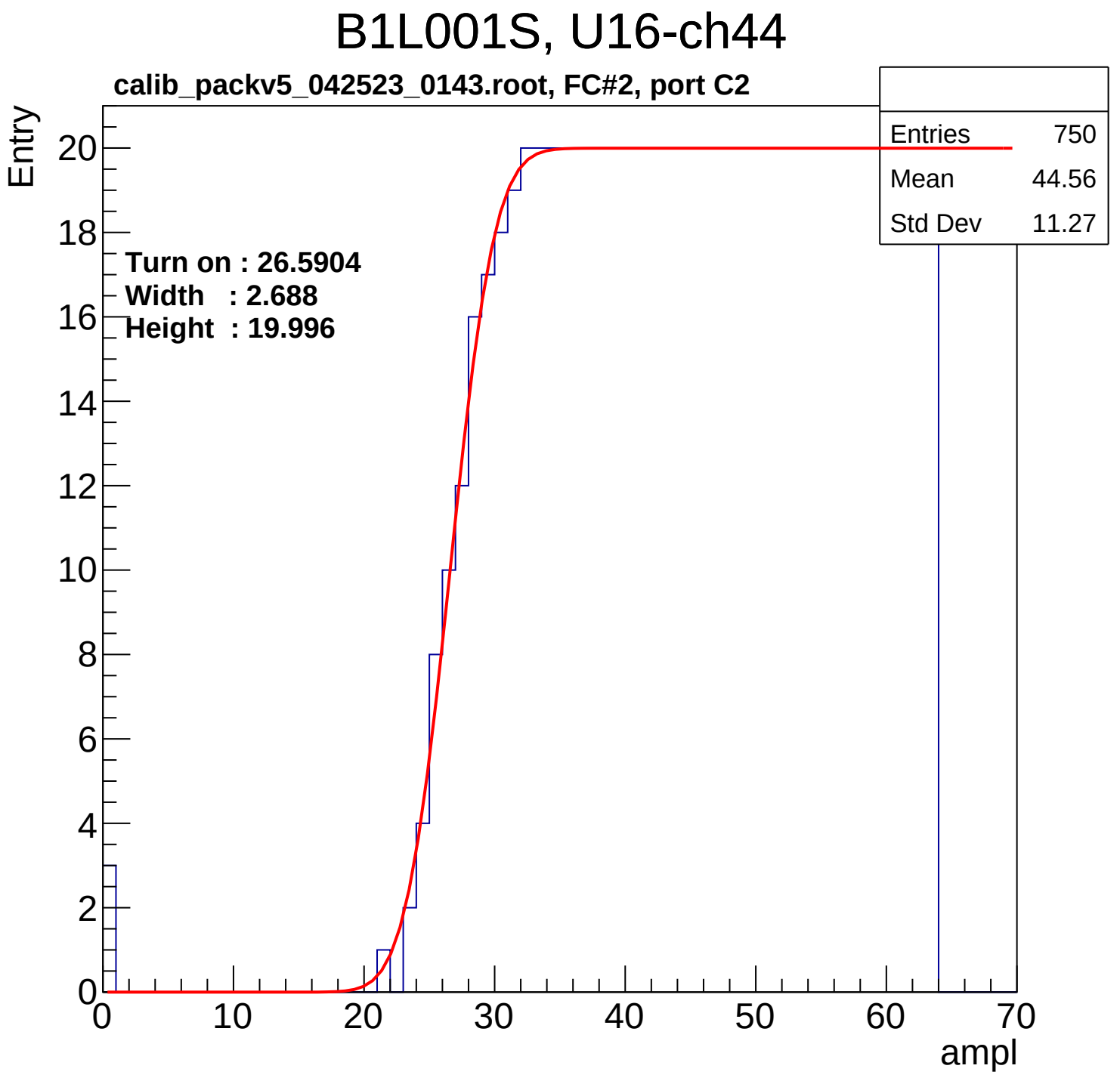
B1L001S, U16-ch44
calib_packv5_042523_0143.root, FC#2, port C2
Entries 750
Mean 44.56
Std Dev 11.27
Turn on : 26.5904
Width : 2.688
Height : 19.996
Entry
ampl
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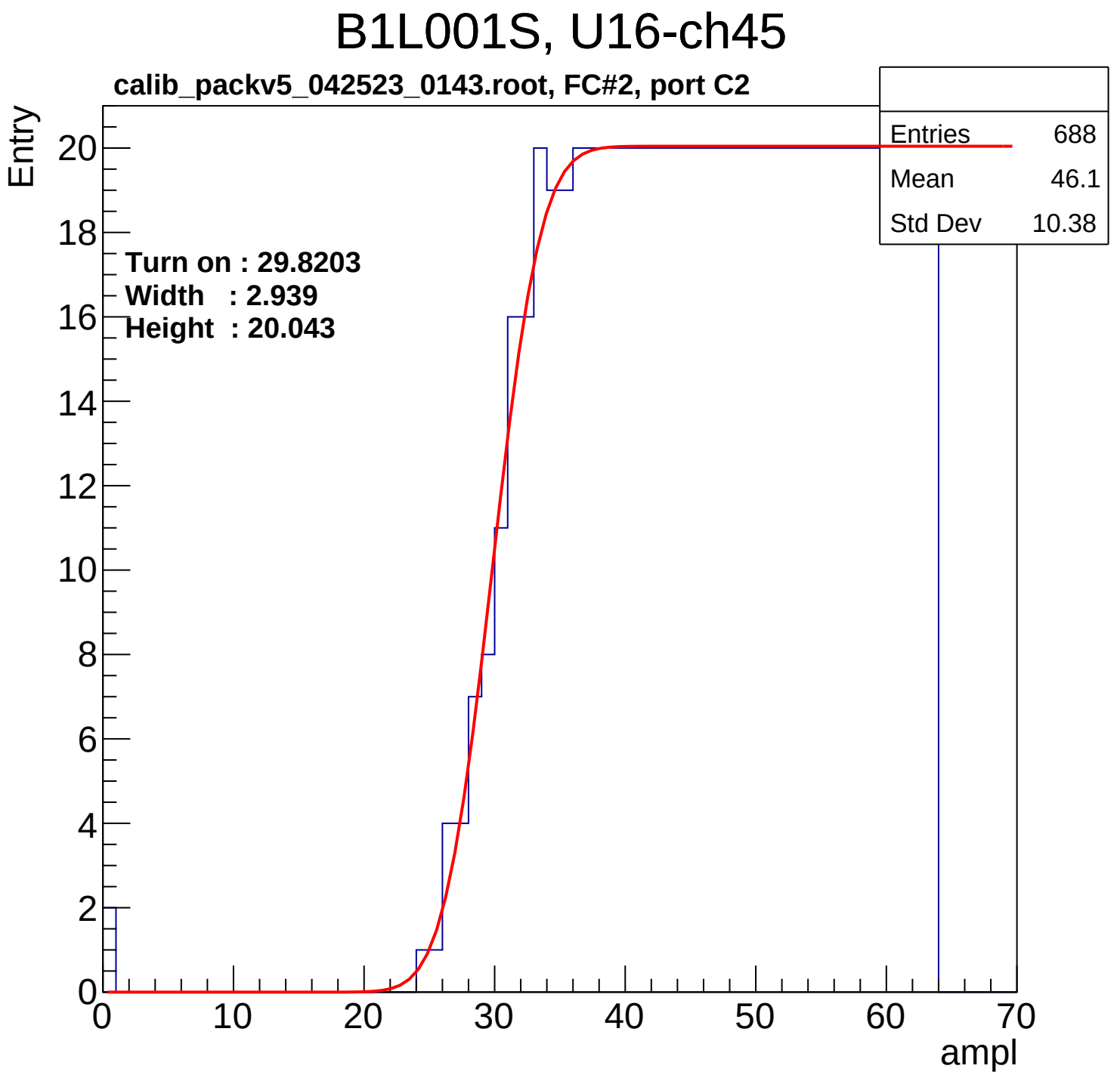
B1L001S, U16-ch45
calib_packv5_042523_0143.root, FC#2, port C2
Entries 688
Mean 46.1
Std Dev 10.38
Turn on : 29.8203
Width : 2.939
Height : 20.043
Entry
ampl
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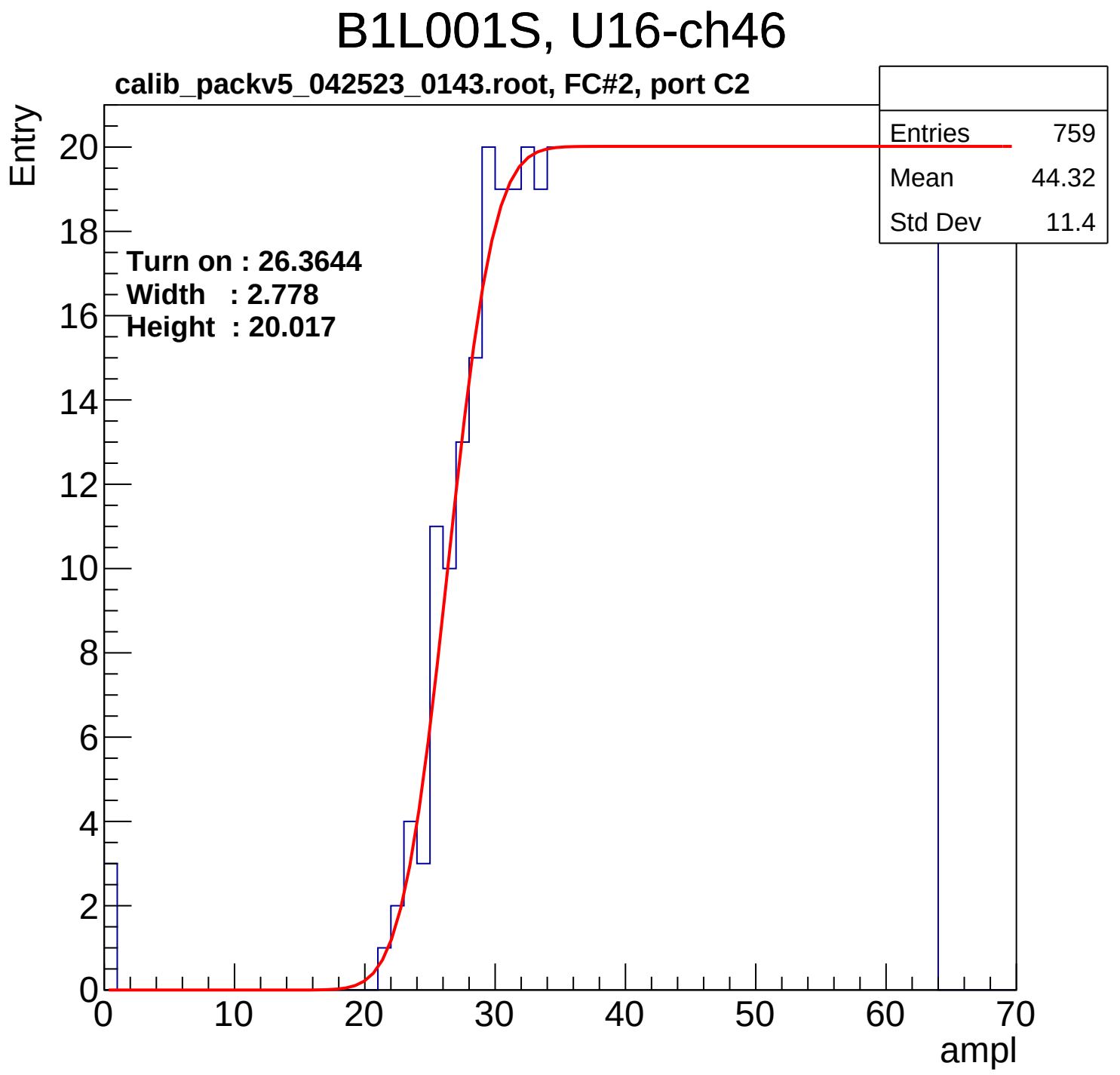
B1L001S, U16-ch46
calib_packv5_042523_0143.root, FC#2, port C2
Entries 759
Mean 44.32
Std Dev 11.4
Turn on : 26.3644
Width : 2.778
Height : 20.017
Entry
ampl
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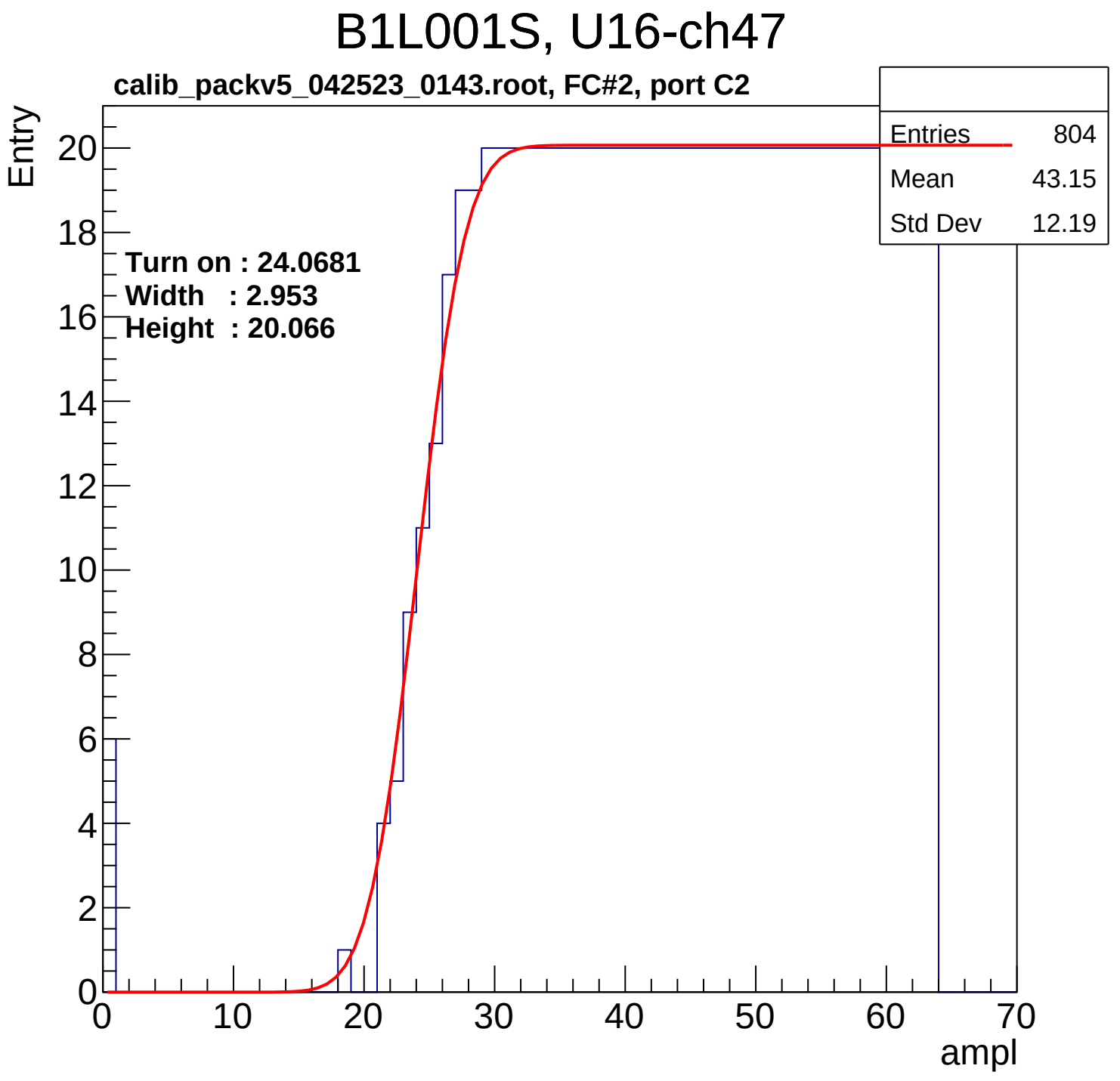
B1L001S, U16-ch47
calib_packv5_042523_0143.root, FC#2, port C2
Entries 804
Mean 43.15
Std Dev 12.19
Turn on : 24.0681
Width : 2.953
Height : 20.066
Entry
ampl
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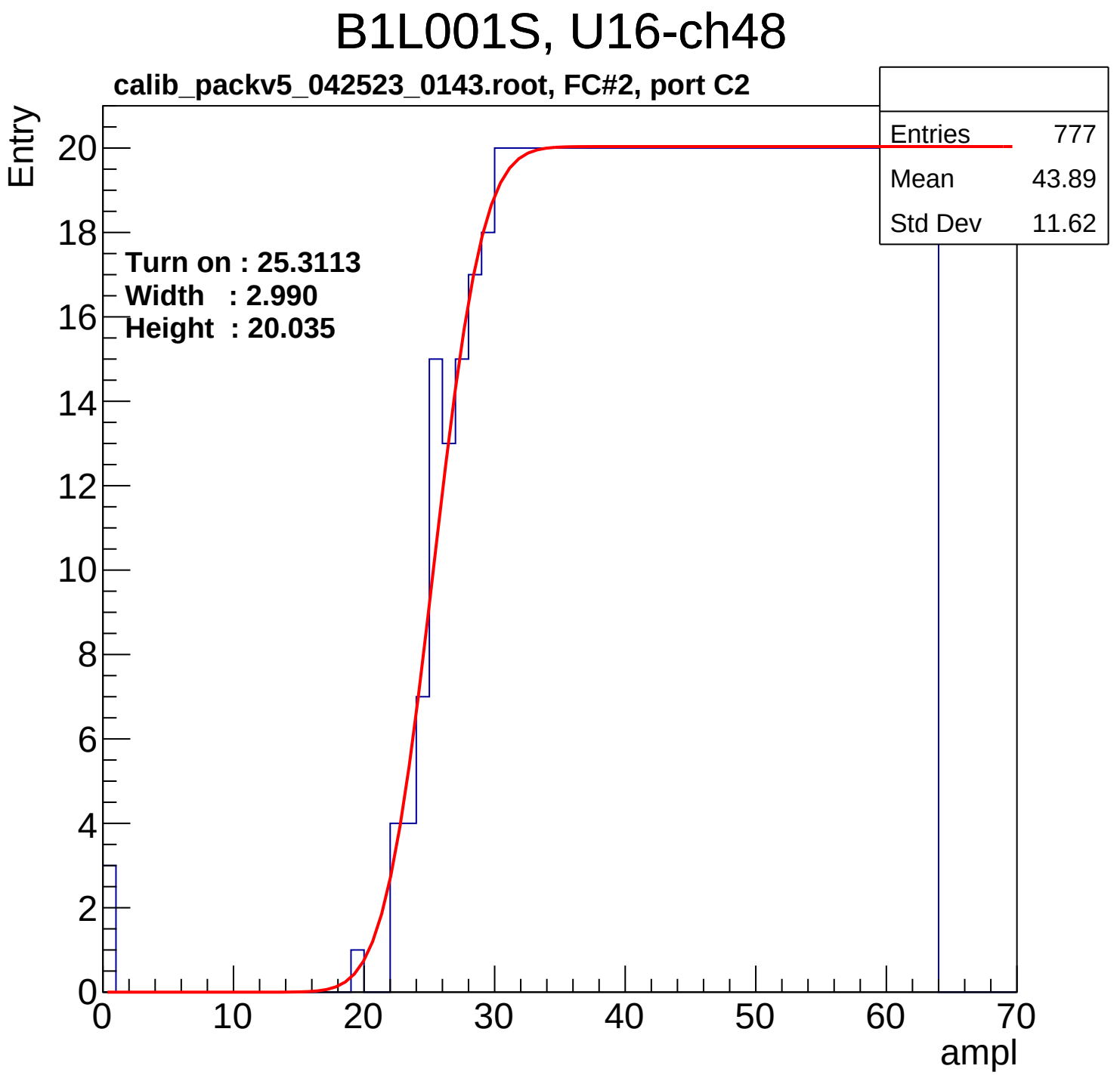
B1L001S, U16-ch48
calib_packv5_042523_0143.root, FC#2, port C2
Entries 777
Mean 43.89
Std Dev 11.62
Turn on : 25.3113
Width : 2.990
Height : 20.035
Entry
ampl
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6
8
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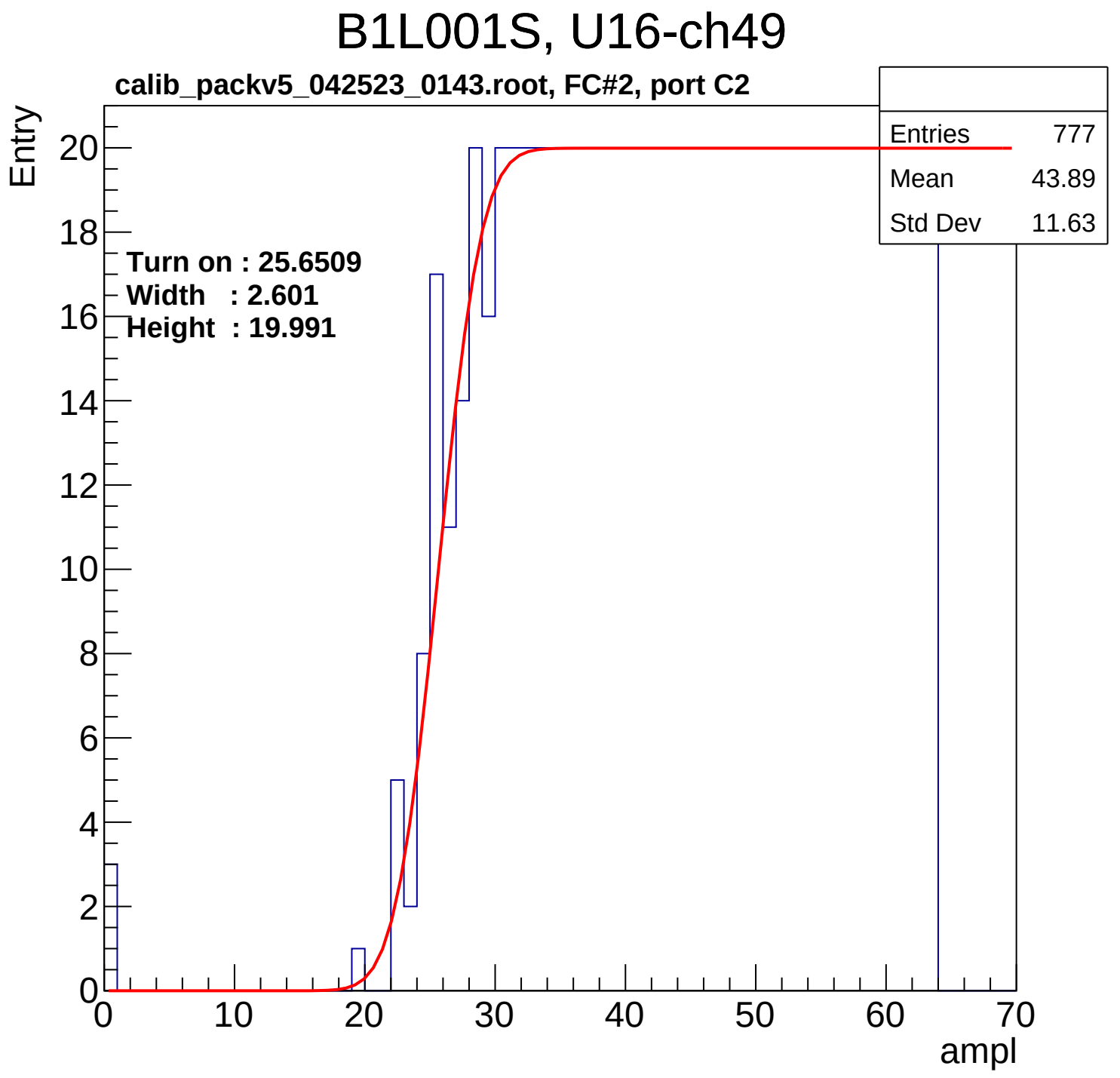
B1L001S, U16-ch49
calib_packv5_042523_0143.root, FC#2, port C2
Entries 777
Mean 43.89
Std Dev 11.63
Turn on : 25.6509
Width : 2.601
Height : 19.991
Entry
ampl
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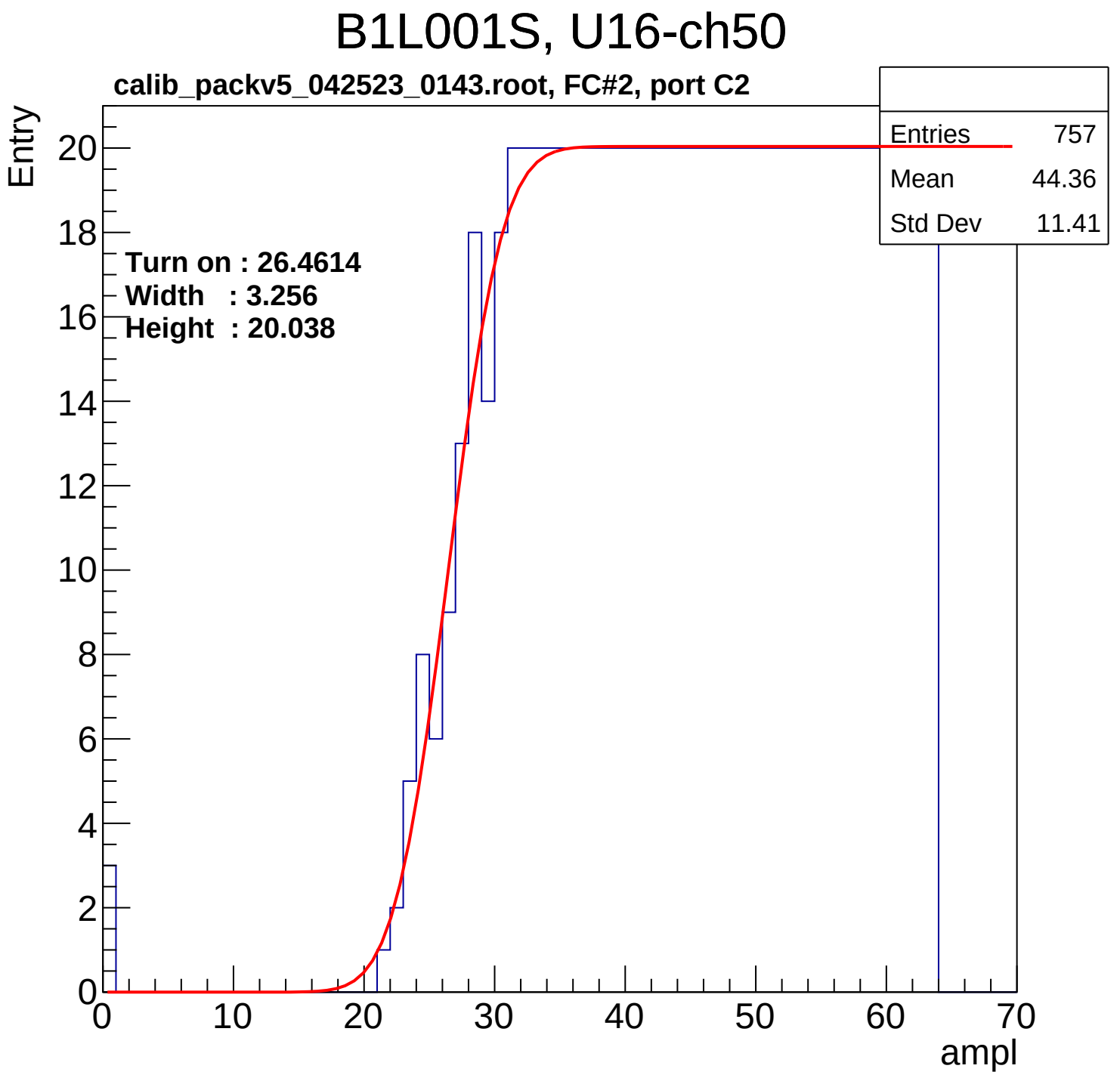
B1L001S, U16-ch50
calib_packv5_042523_0143.root, FC#2, port C2
Entries 757
Mean 44.36
Std Dev 11.41
Turn on : 26.4614
Width : 3.256
Height : 20.038
Entry
ampl
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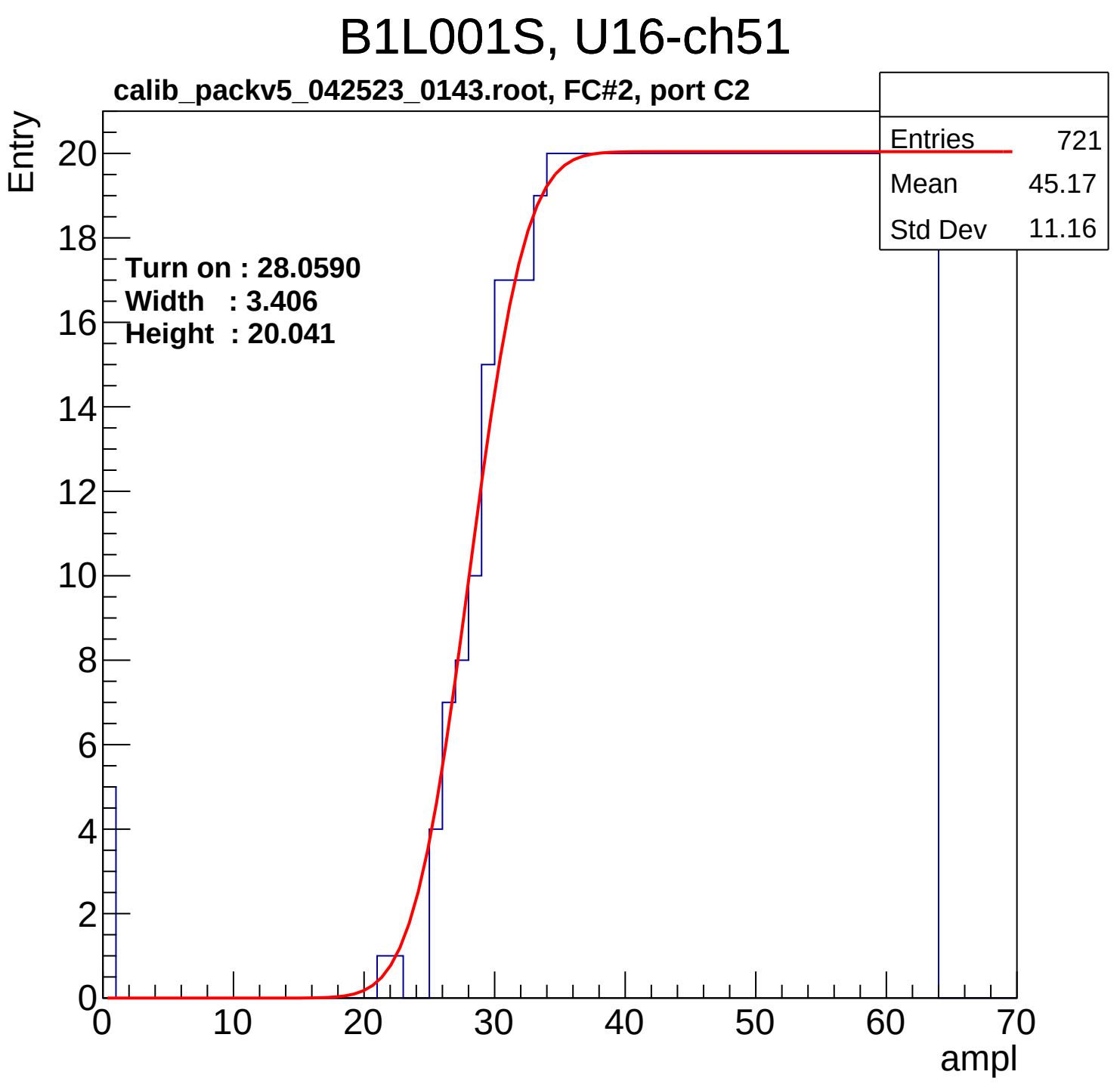
B1L001S, U16-ch51
calib_packv5_042523_0143.root, FC#2, port C2
Entries 721
Mean 45.17
Std Dev 11.16
Turn on : 28.0590
Width : 3.406
Height : 20.041
Entry
ampl
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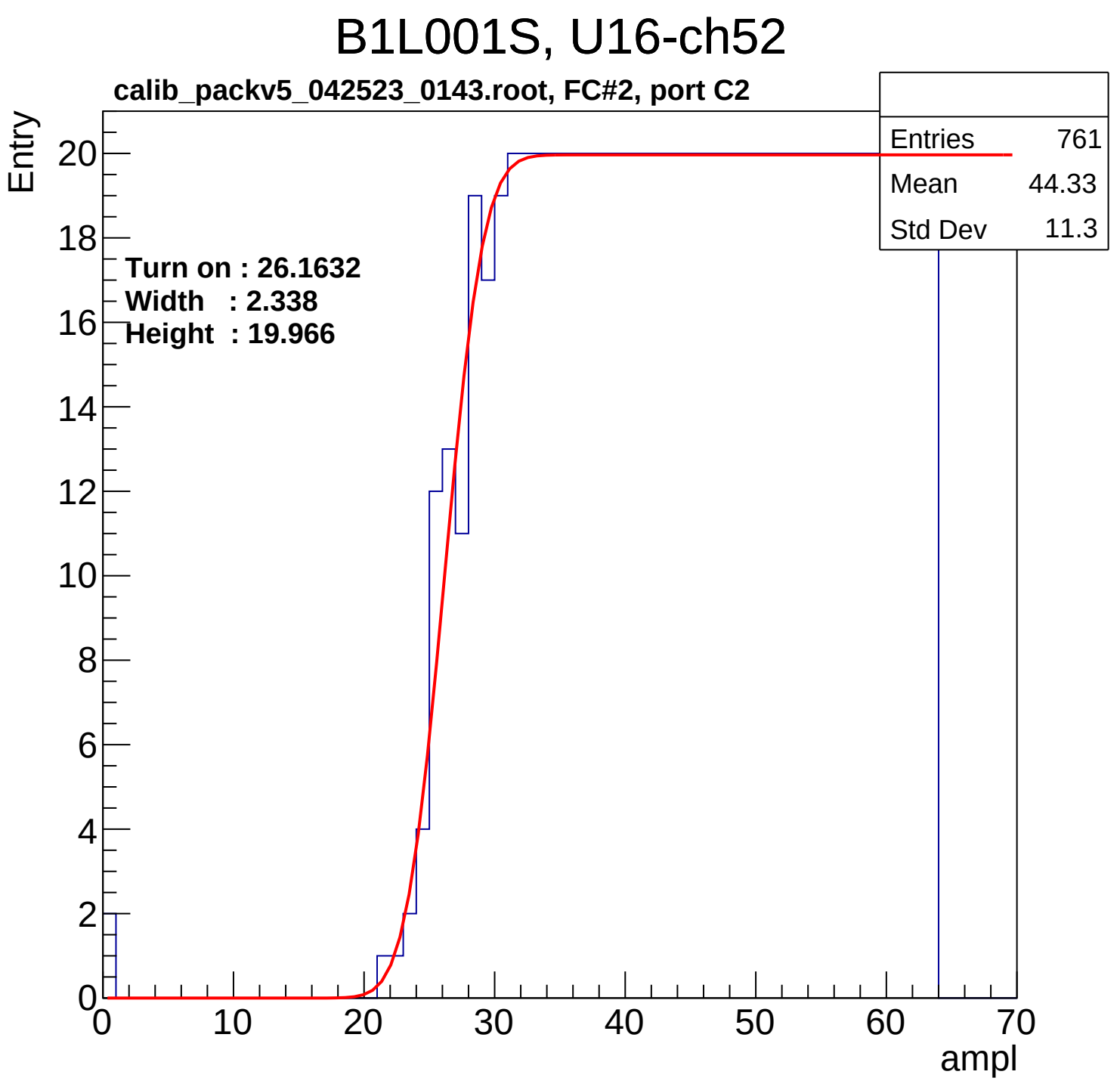
B1L001S, U16-ch52
calib_packv5_042523_0143.root, FC#2, port C2
Entries 761
Mean 44.33
Std Dev 11.3
Turn on : 26.1632
Width : 2.338
Height : 19.966
Entry
ampl
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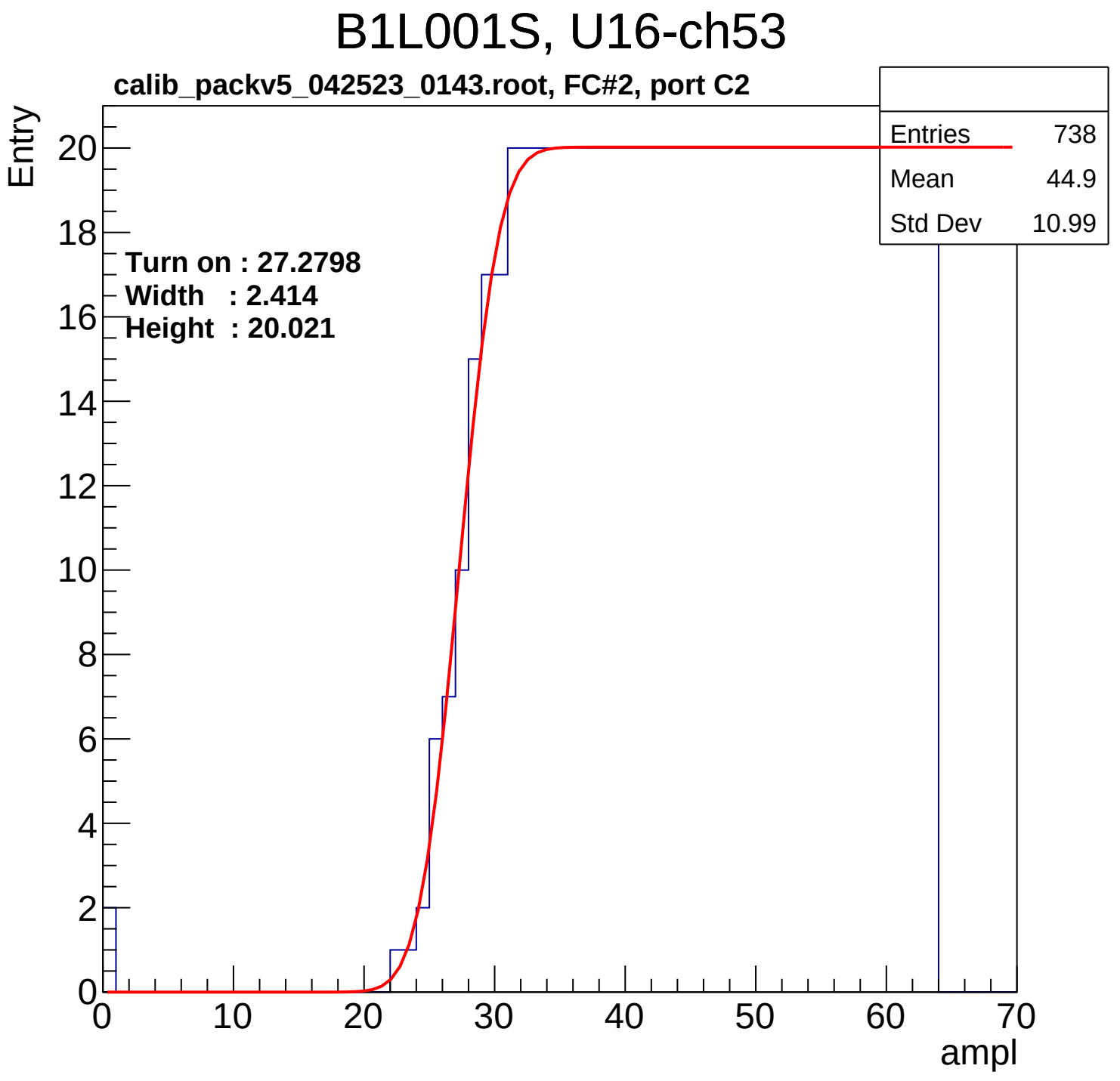
B1L001S, U16-ch53
calib_packv5_042523_0143.root, FC#2, port C2
Entries 738
Mean 44.9
Std Dev 10.99
Turn on : 27.2798
Width : 2.414
Height : 20.021
Entry
ampl
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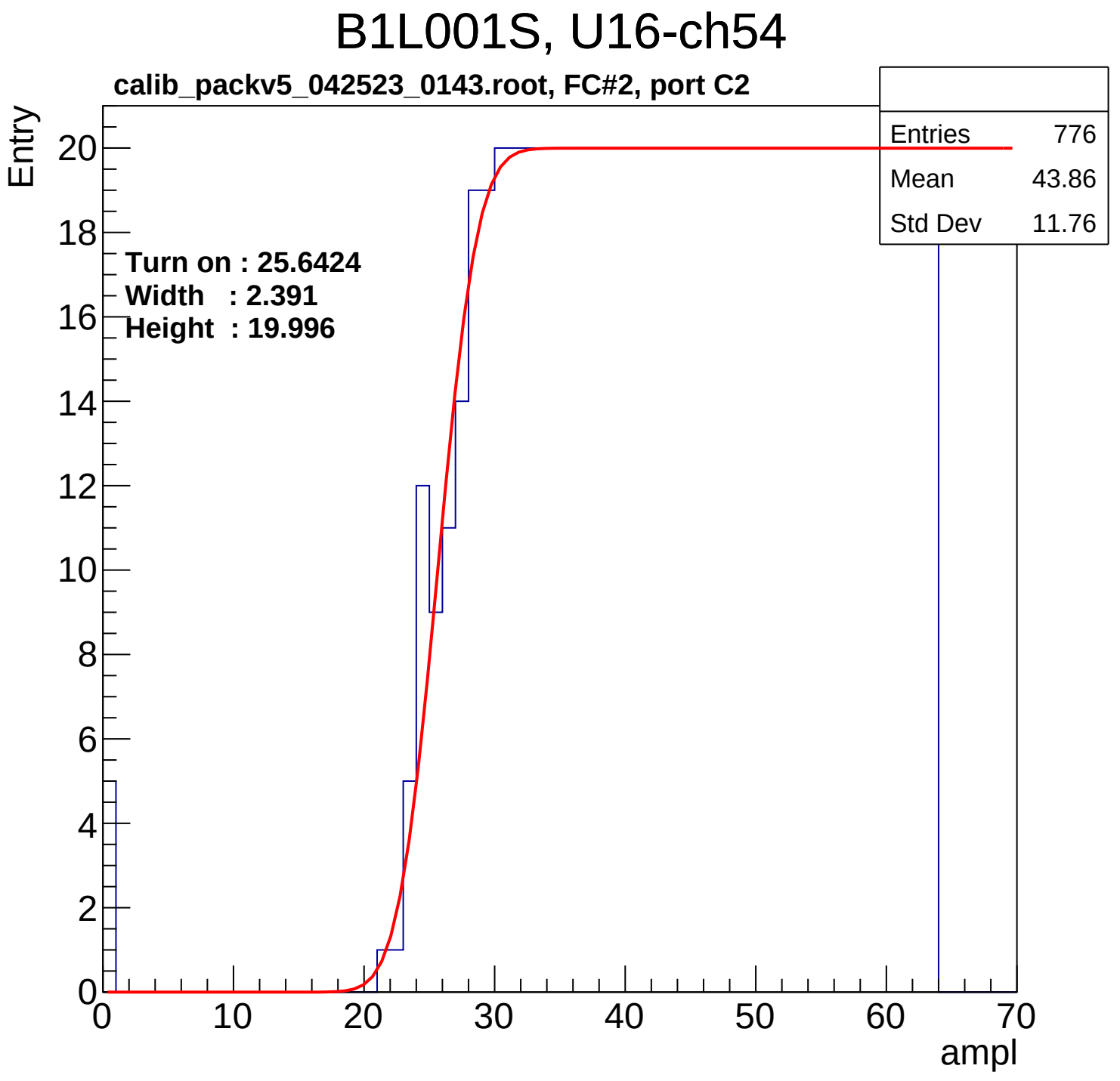
B1L001S, U16-ch54
calib_packv5_042523_0143.root, FC#2, port C2
Entries 776
Mean 43.86
Std Dev 11.76
Turn on : 25.6424
Width : 2.391
Height : 19.996
Entry
ampl
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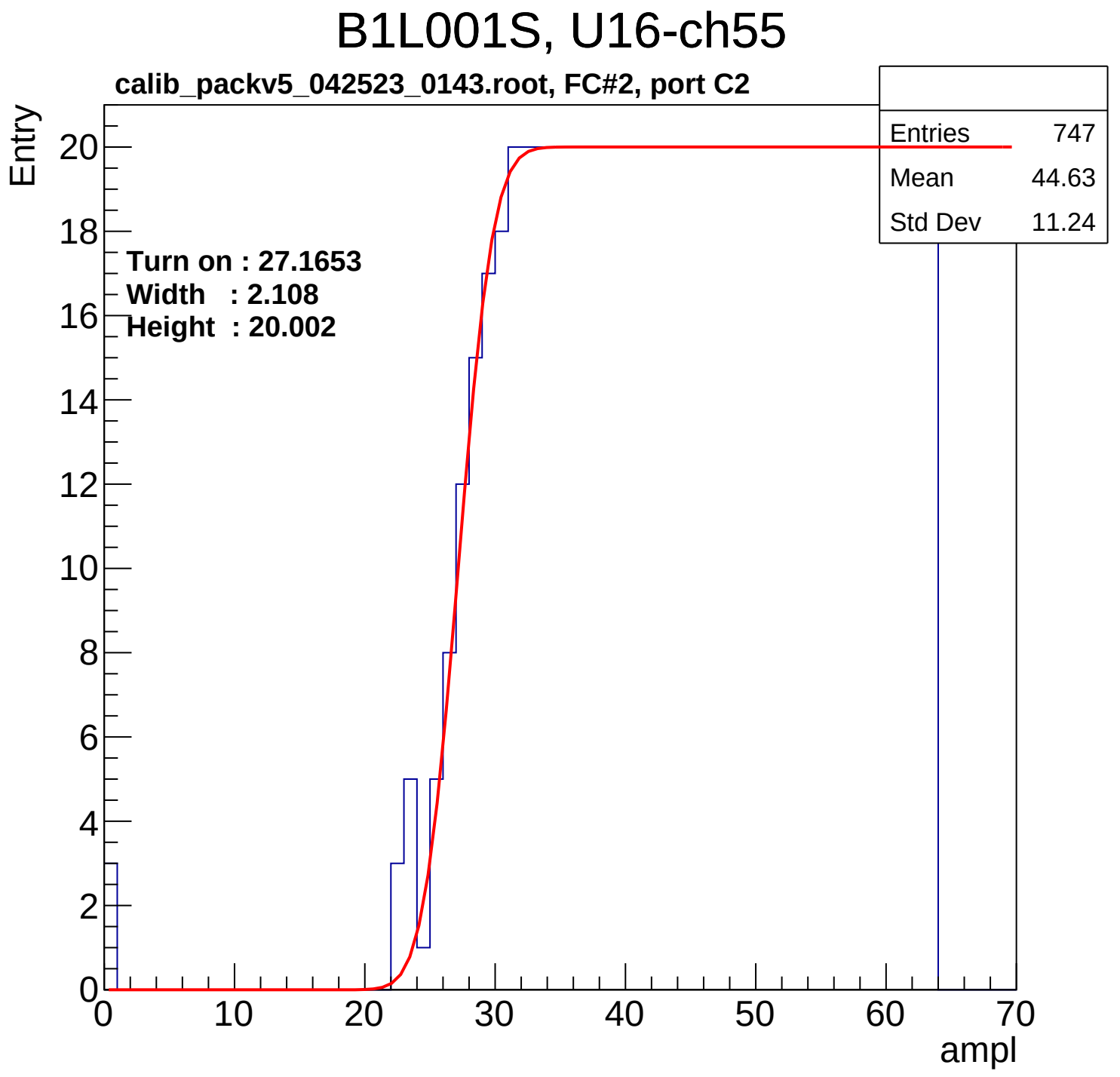
B1L001S, U16-ch55
calib_packv5_042523_0143.root, FC#2, port C2
Entries 747
Mean 44.63
Std Dev 11.24
Turn on : 27.1653
Width : 2.108
Height : 20.002
Entry
ampl
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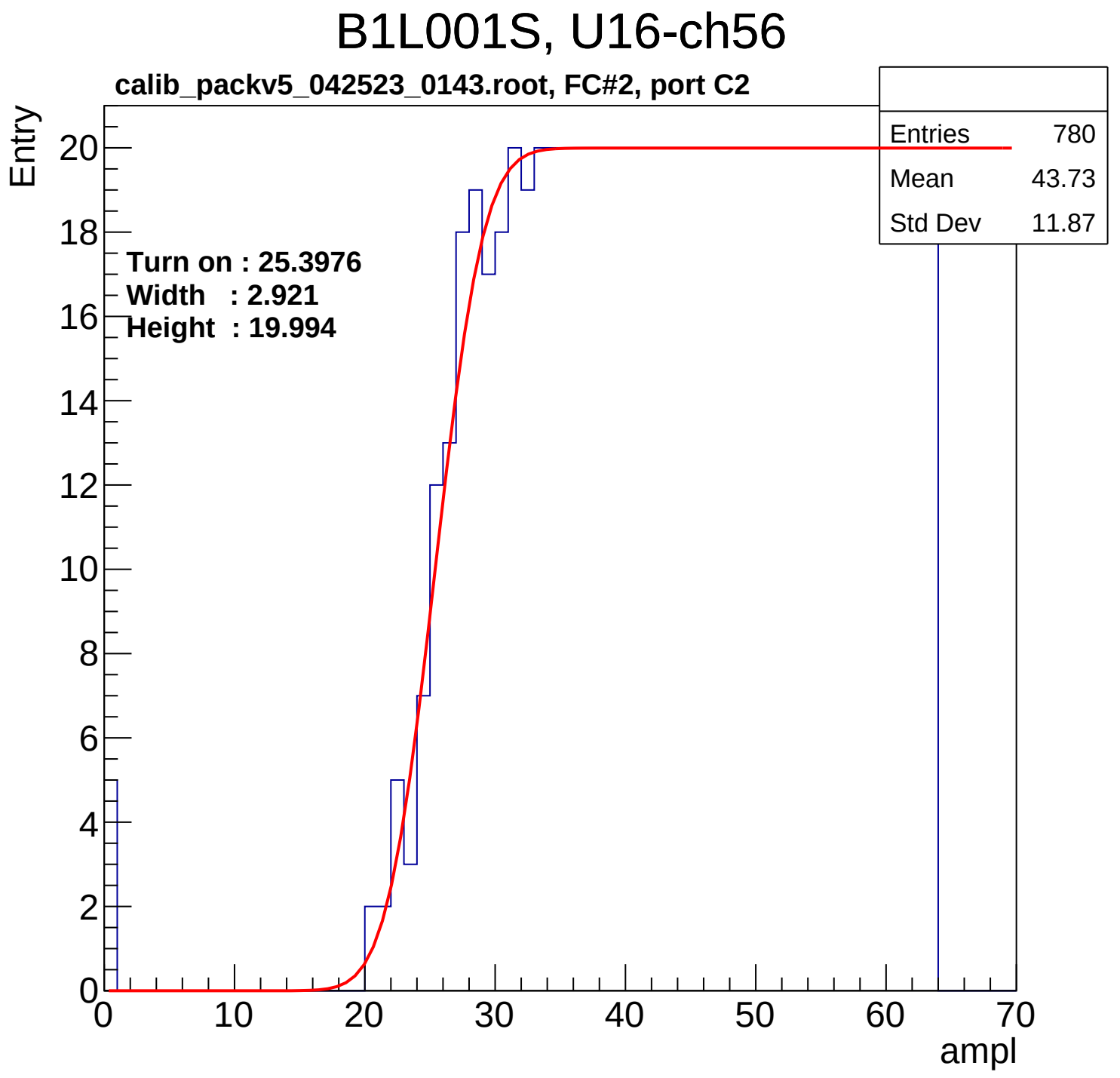
B1L001S, U16-ch56
calib_packv5_042523_0143.root, FC#2, port C2
Entries 780
Mean 43.73
Std Dev 11.87
Turn on : 25.3976
Width : 2.921
Height : 19.994
Entry
ampl
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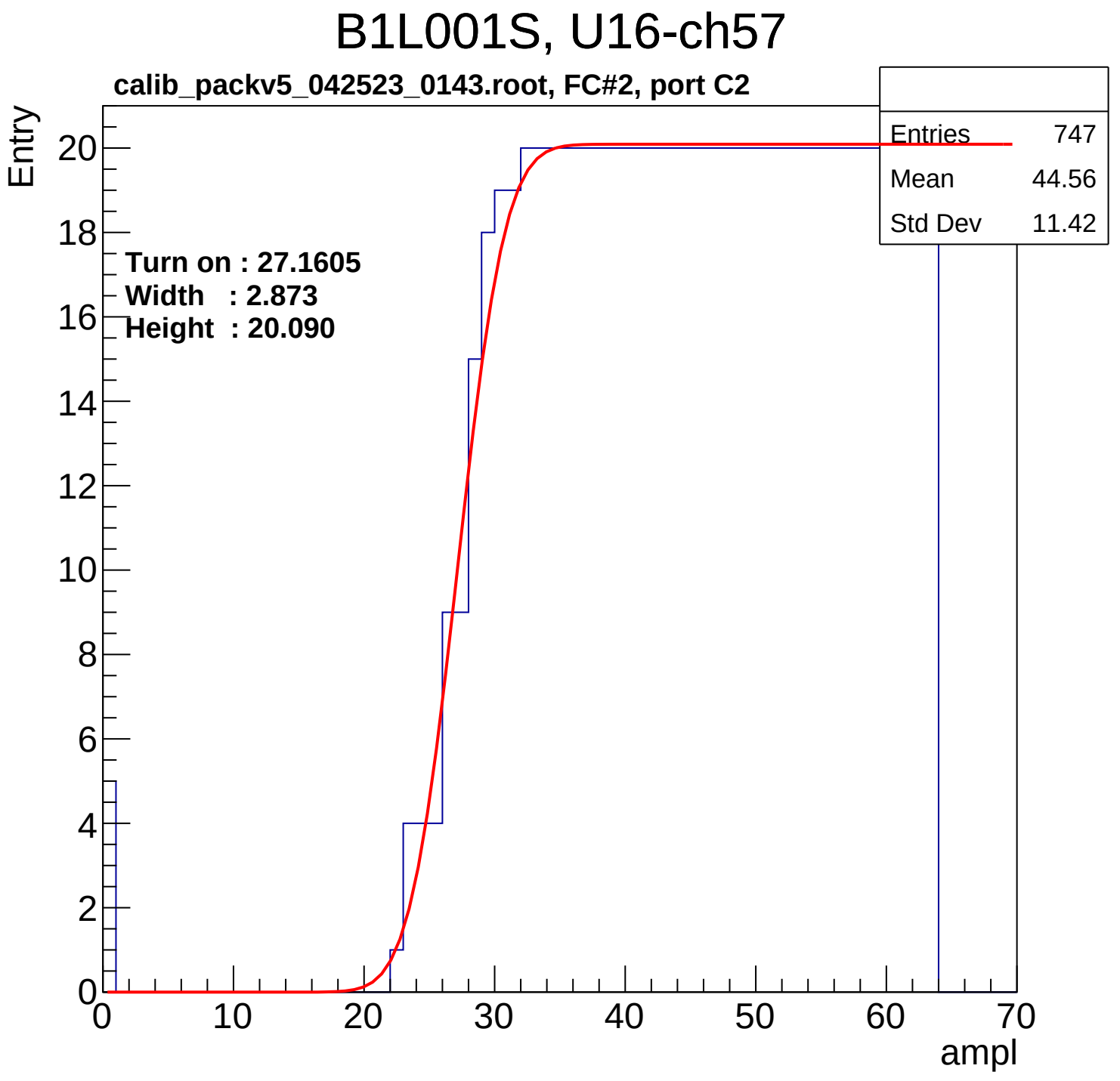
B1L001S, U16-ch57
calib_packv5_042523_0143.root, FC#2, port C2
Entries 747
Mean 44.56
Std Dev 11.42
Turn on : 27.1605
Width : 2.873
Height : 20.090
Entry
ampl
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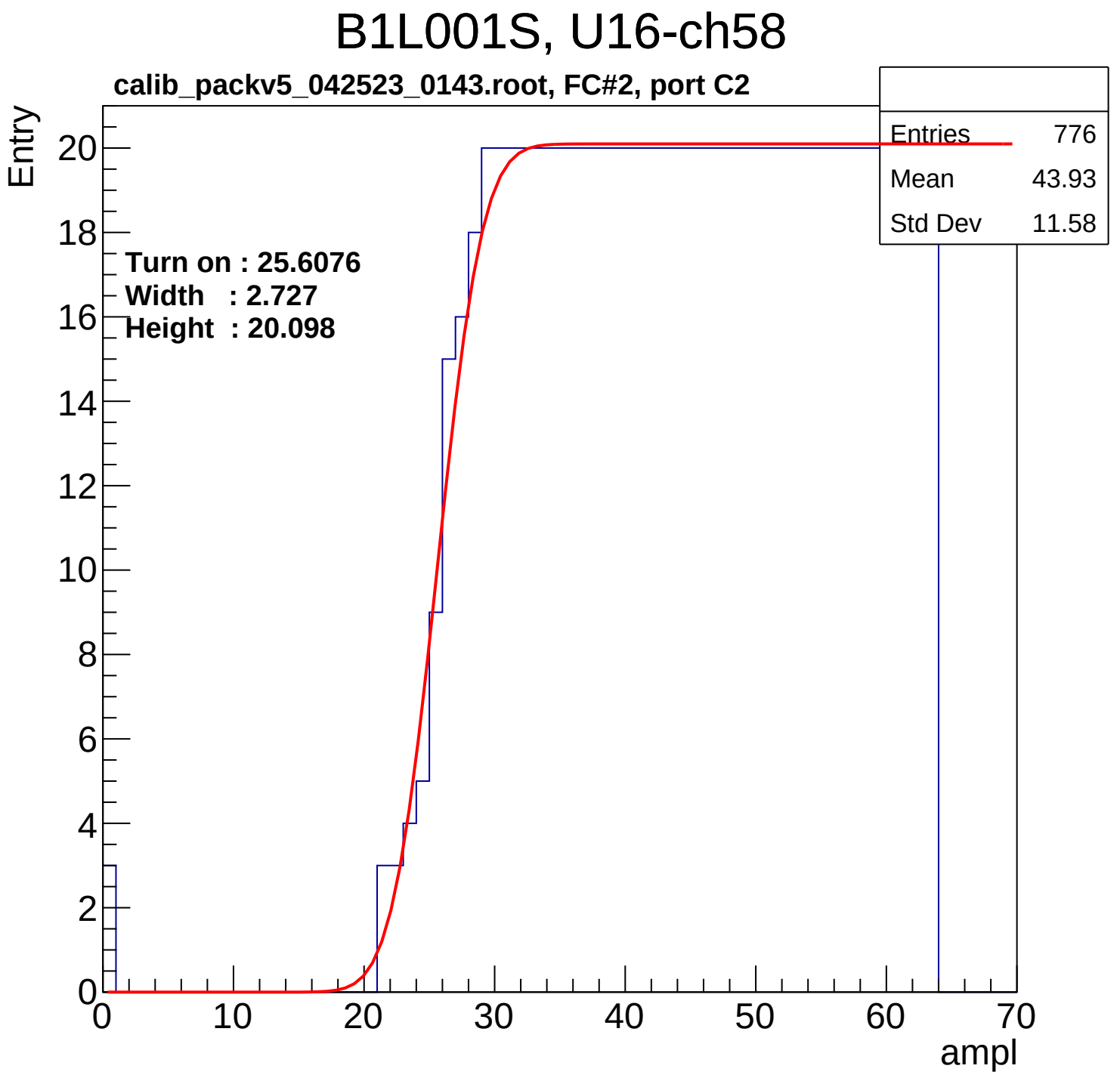
B1L001S, U16-ch58
calib_packv5_042523_0143.root, FC#2, port C2
Entries 776
Mean 43.93
Std Dev 11.58
Turn on : 25.6076
Width : 2.727
Height : 20.098
Entry
ampl
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6
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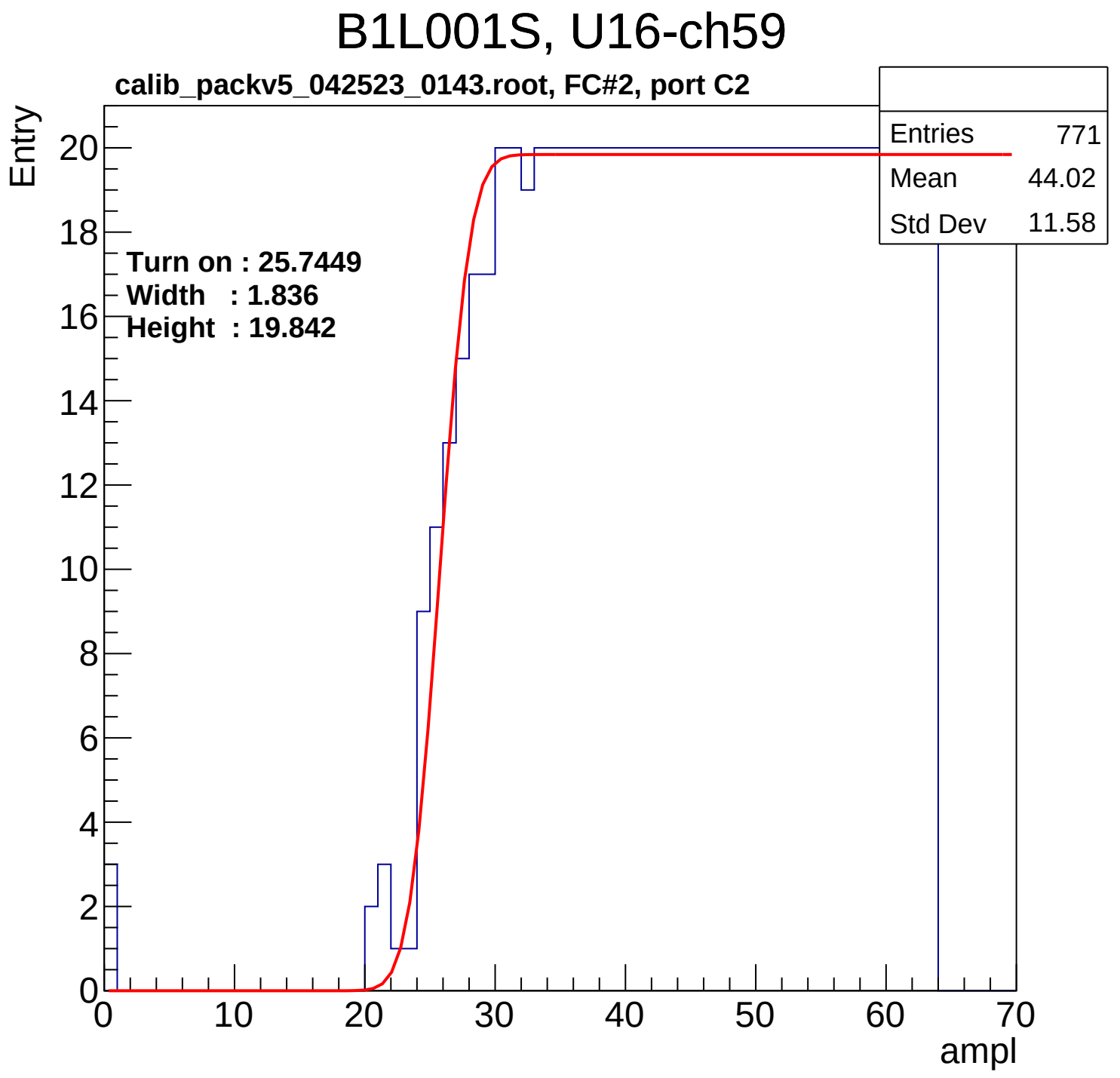
B1L001S, U16-ch59
calib_packv5_042523_0143.root, FC#2, port C2
Entries 771
Mean 44.02
Std Dev 11.58
Turn on : 25.7449
Width : 1.836
Height : 19.842
Entry
ampl
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6
8
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12
14
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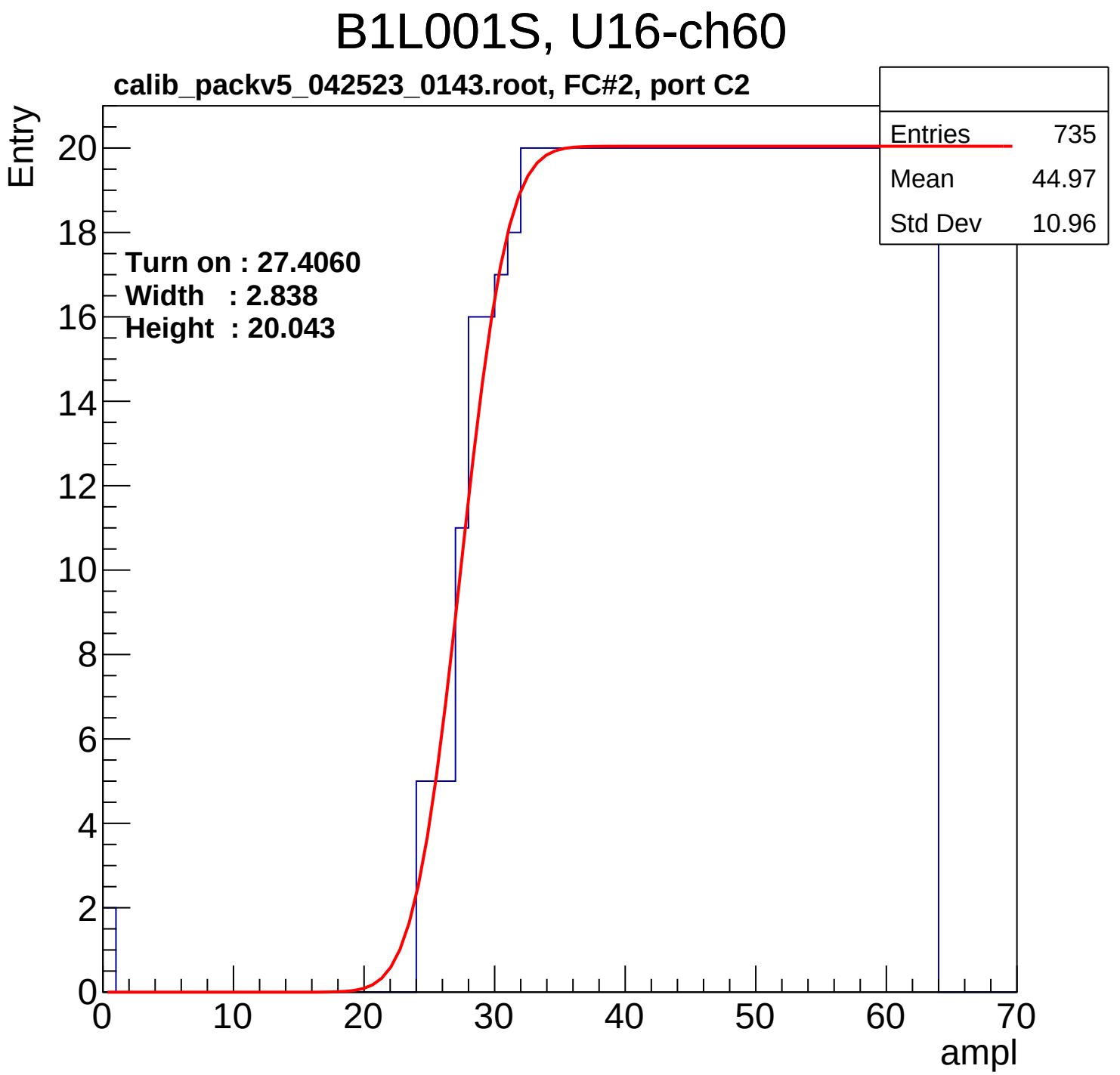
B1L001S, U16-ch60
calib_packv5_042523_0143.root, FC#2, port C2
Entries 735
Mean 44.97
Std Dev 10.96
Turn on : 27.4060
Width : 2.838
Height : 20.043
Entry
ampl
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6
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14
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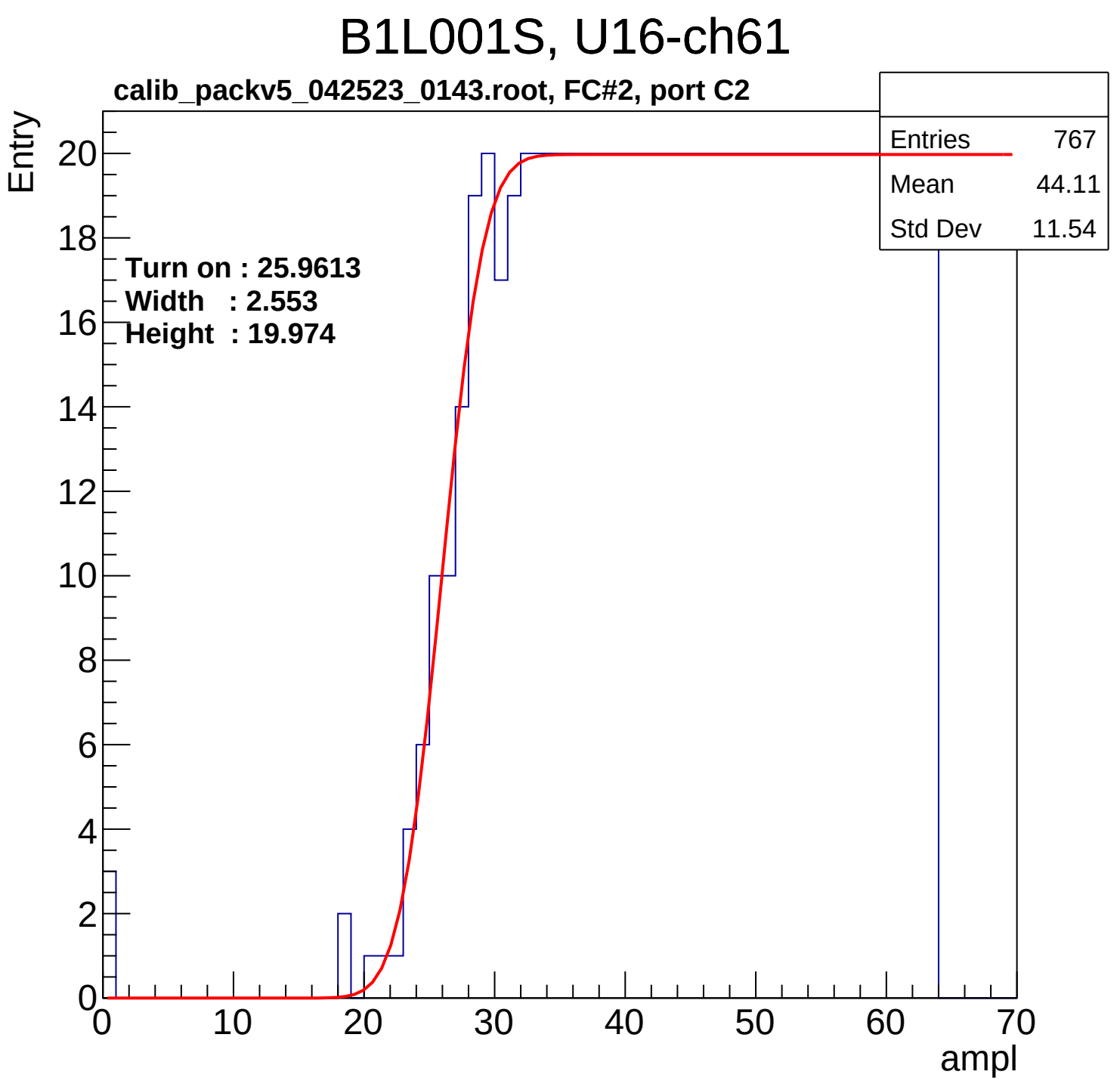
B1L001S, U16-ch61
calib_packv5_042523_0143.root, FC#2, port C2
Entries 767
Mean 44.11
Std Dev 11.54
Turn on : 25.9613
Width : 2.553
Height : 19.974
Entry
ampl
0
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6
8
10
12
14
16
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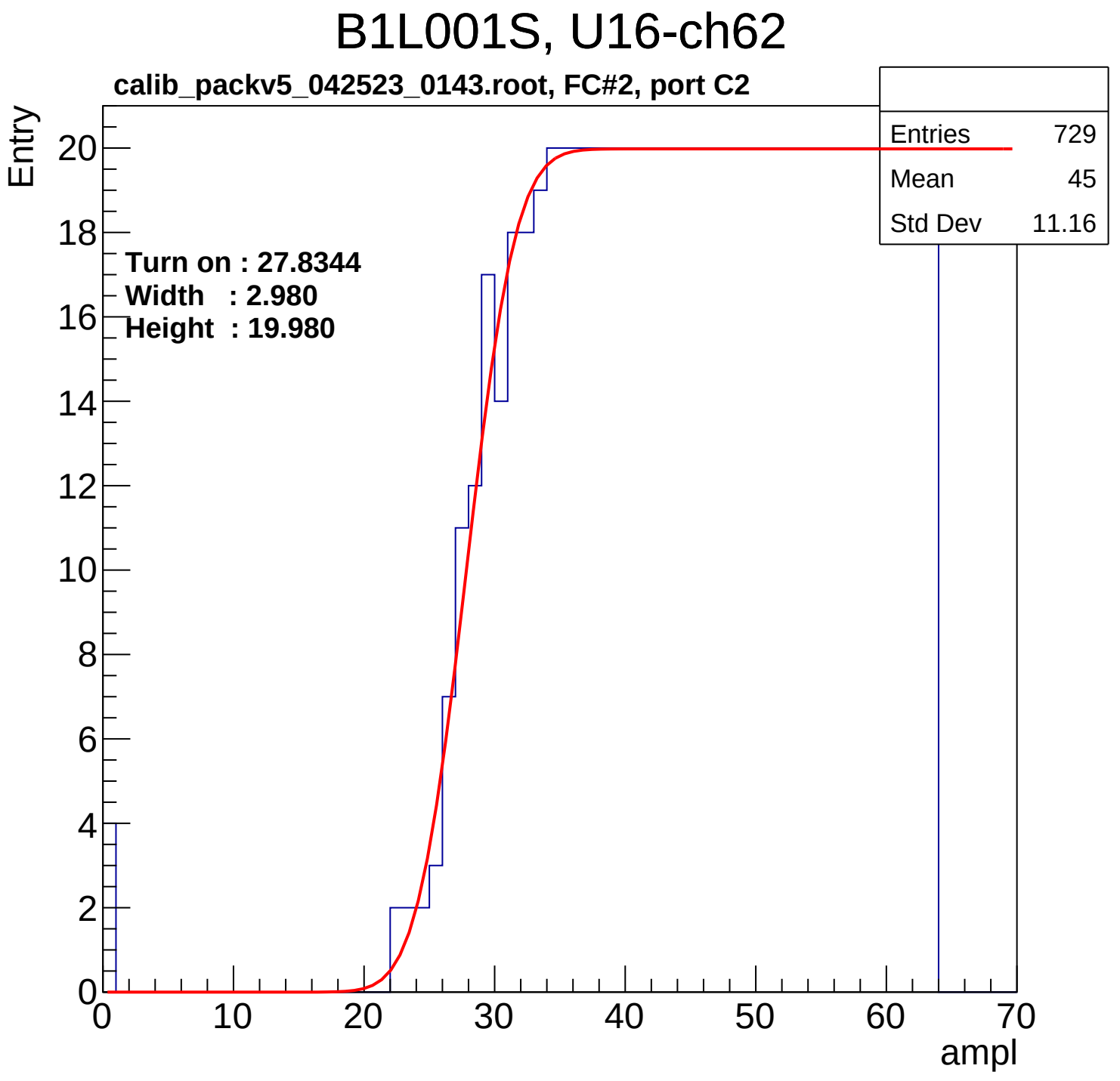
B1L001S, U16-ch62
calib_packv5_042523_0143.root, FC#2, port C2
Entries 729
Mean 45
Std Dev 11.16
Turn on : 27.8344
Width : 2.980
Height : 19.980
Entry
ampl
0
2
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6
8
10
12
14
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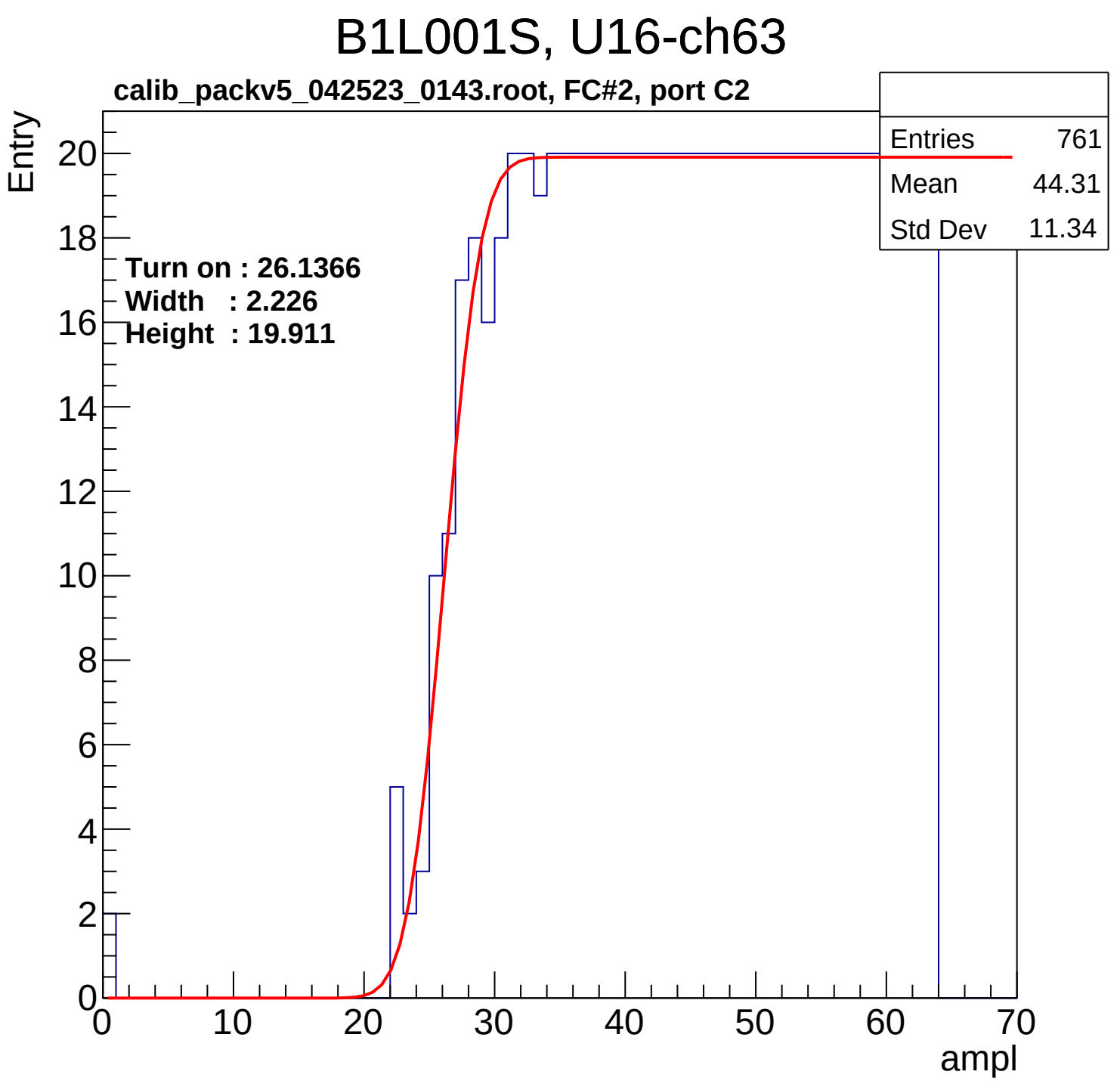
B1L001S, U16-ch63
calib_packv5_042523_0143.root, FC#2, port C2
Entries 761
Mean 44.31
Std Dev 11.34
Turn on : 26.1366
Width : 2.226
Height : 19.911
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
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20
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60
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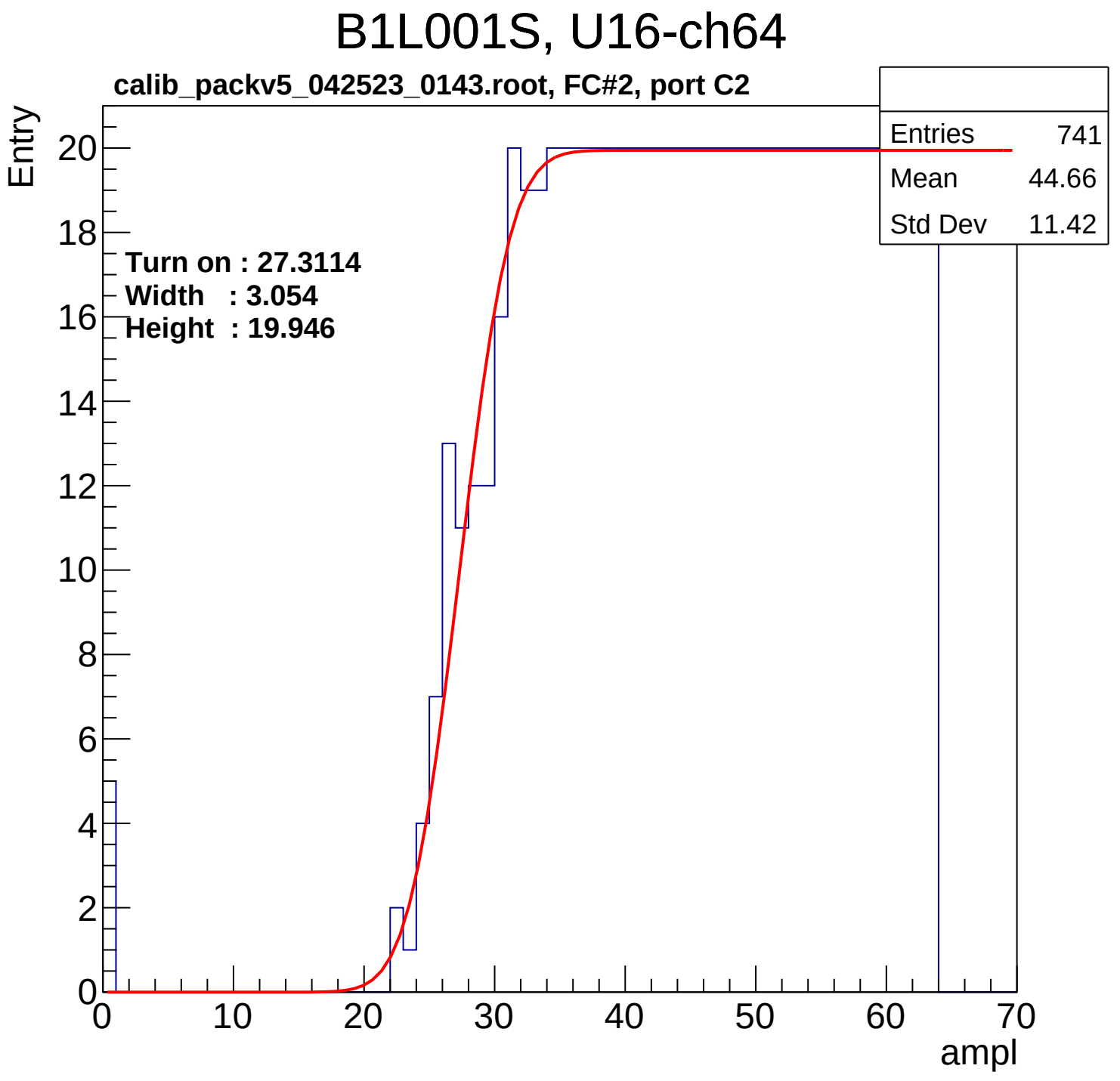
B1L001S, U16-ch64
calib_packv5_042523_0143.root, FC#2, port C2
Entries 741
Mean 44.66
Std Dev 11.42
Turn on : 27.3114
Width : 3.054
Height : 19.946
Entry
ampl
0
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6
8
10
12
14
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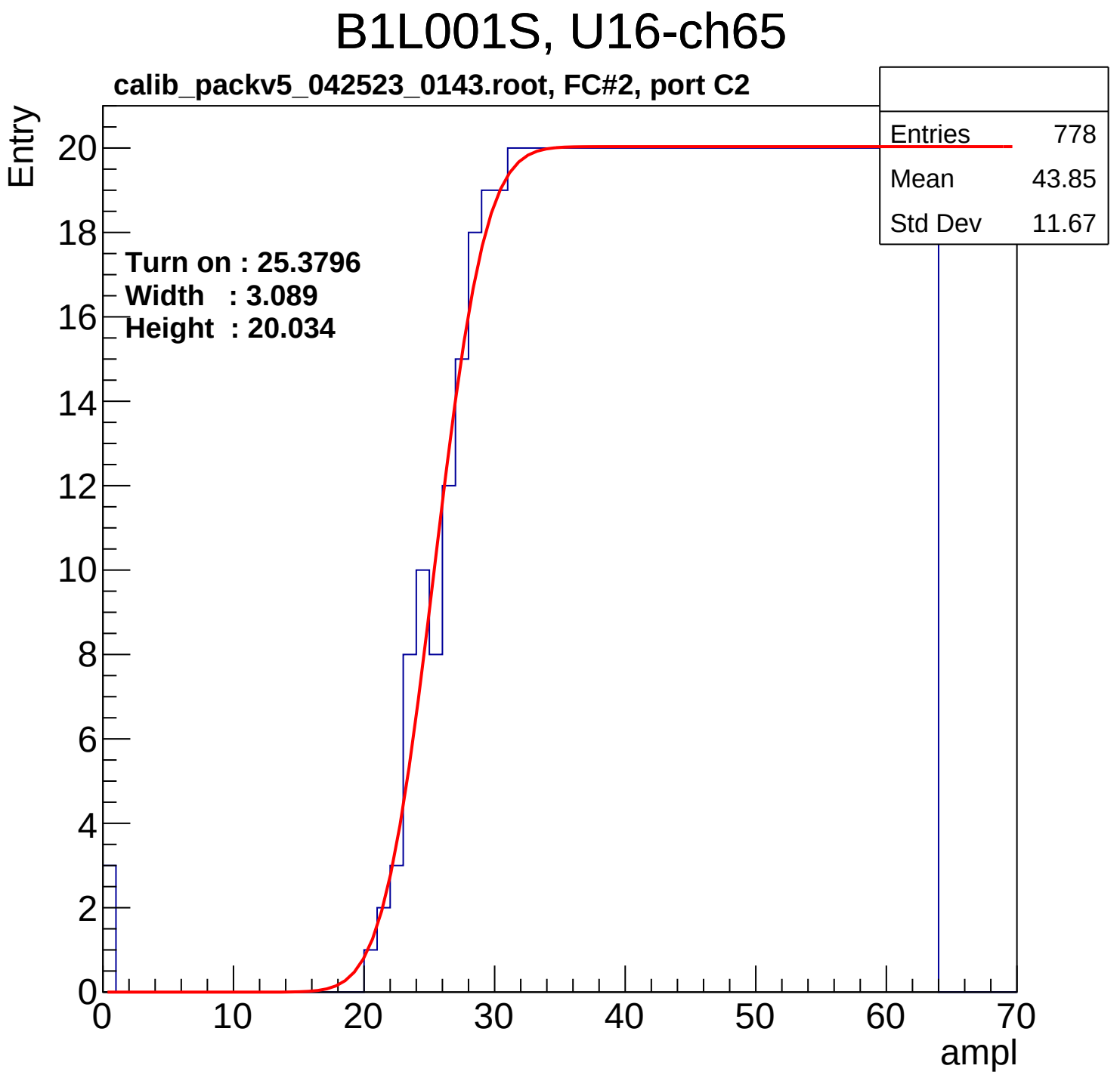
B1L001S, U16-ch65
calib_packv5_042523_0143.root, FC#2, port C2
Entries 778
Mean 43.85
Std Dev 11.67
Turn on : 25.3796
Width : 3.089
Height : 20.034
Entry
ampl
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6
8
10
12
14
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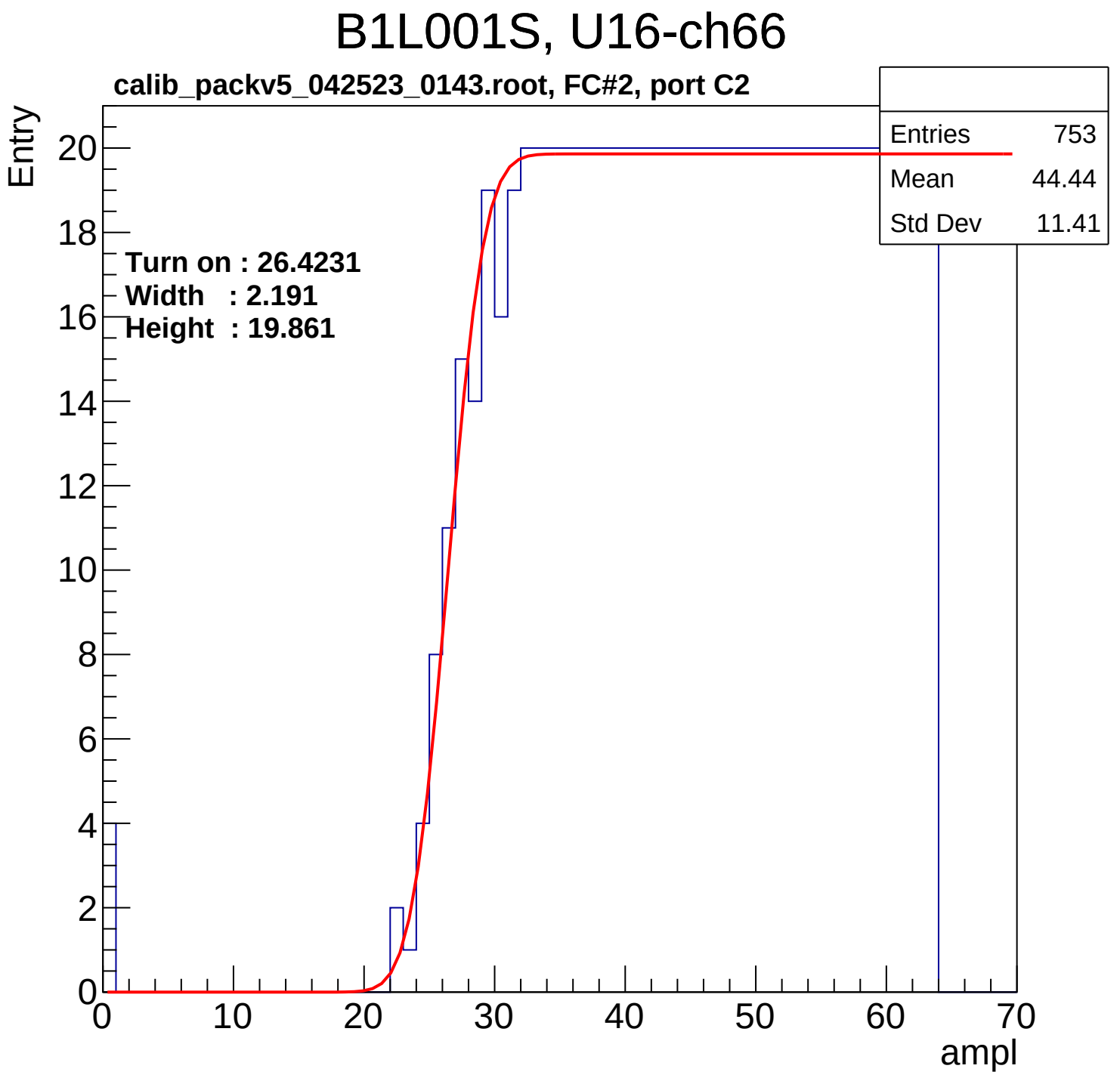
B1L001S, U16-ch66
calib_packv5_042523_0143.root, FC#2, port C2
Entries 753
Mean 44.44
Std Dev 11.41
Turn on : 26.4231
Width : 2.191
Height : 19.861
Entry
ampl
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6
8
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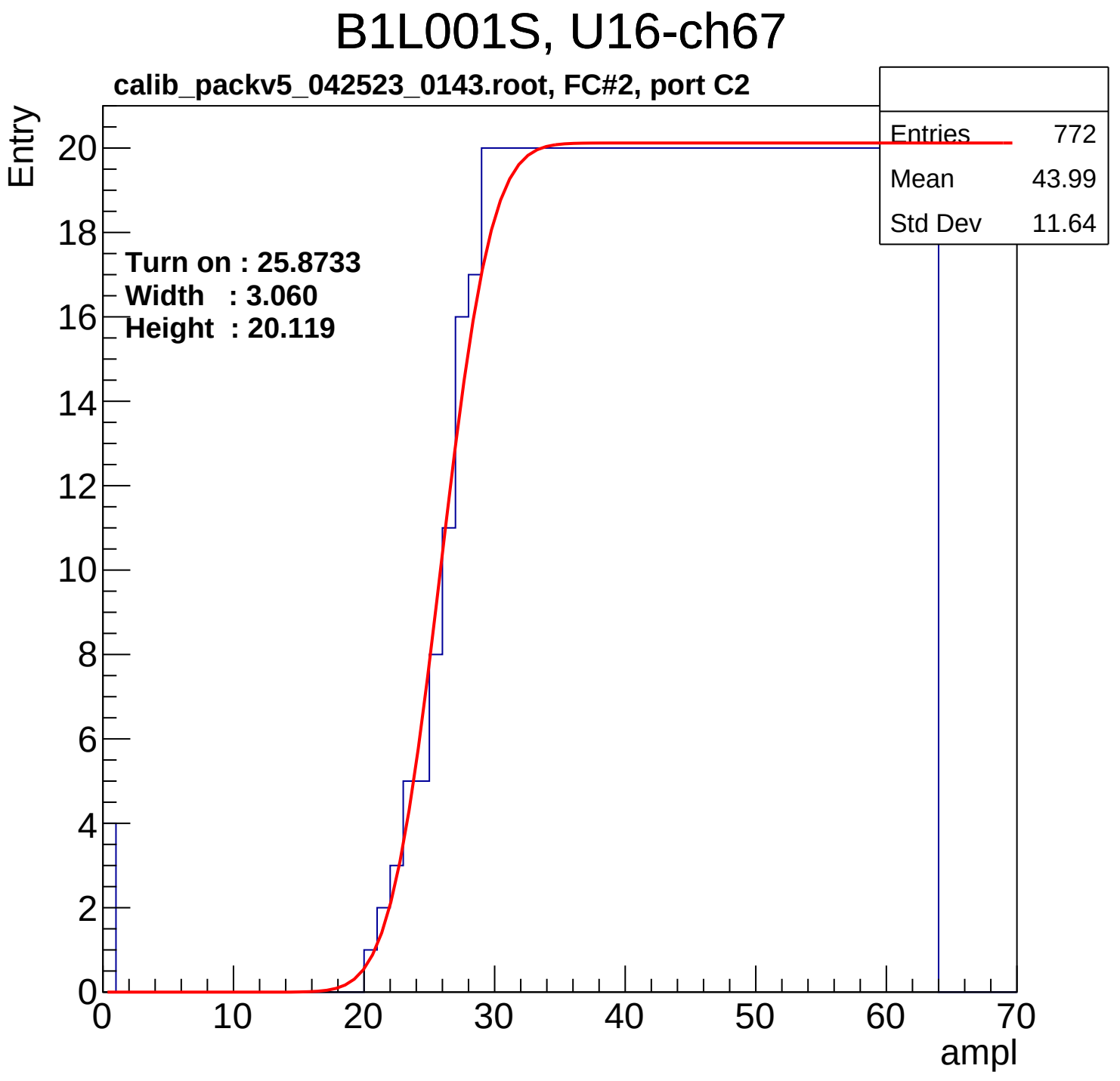
B1L001S, U16-ch67
calib_packv5_042523_0143.root, FC#2, port C2
Entries 772
Mean 43.99
Std Dev 11.64
Turn on : 25.8733
Width : 3.060
Height : 20.119
Entry
ampl
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6
8
10
12
14
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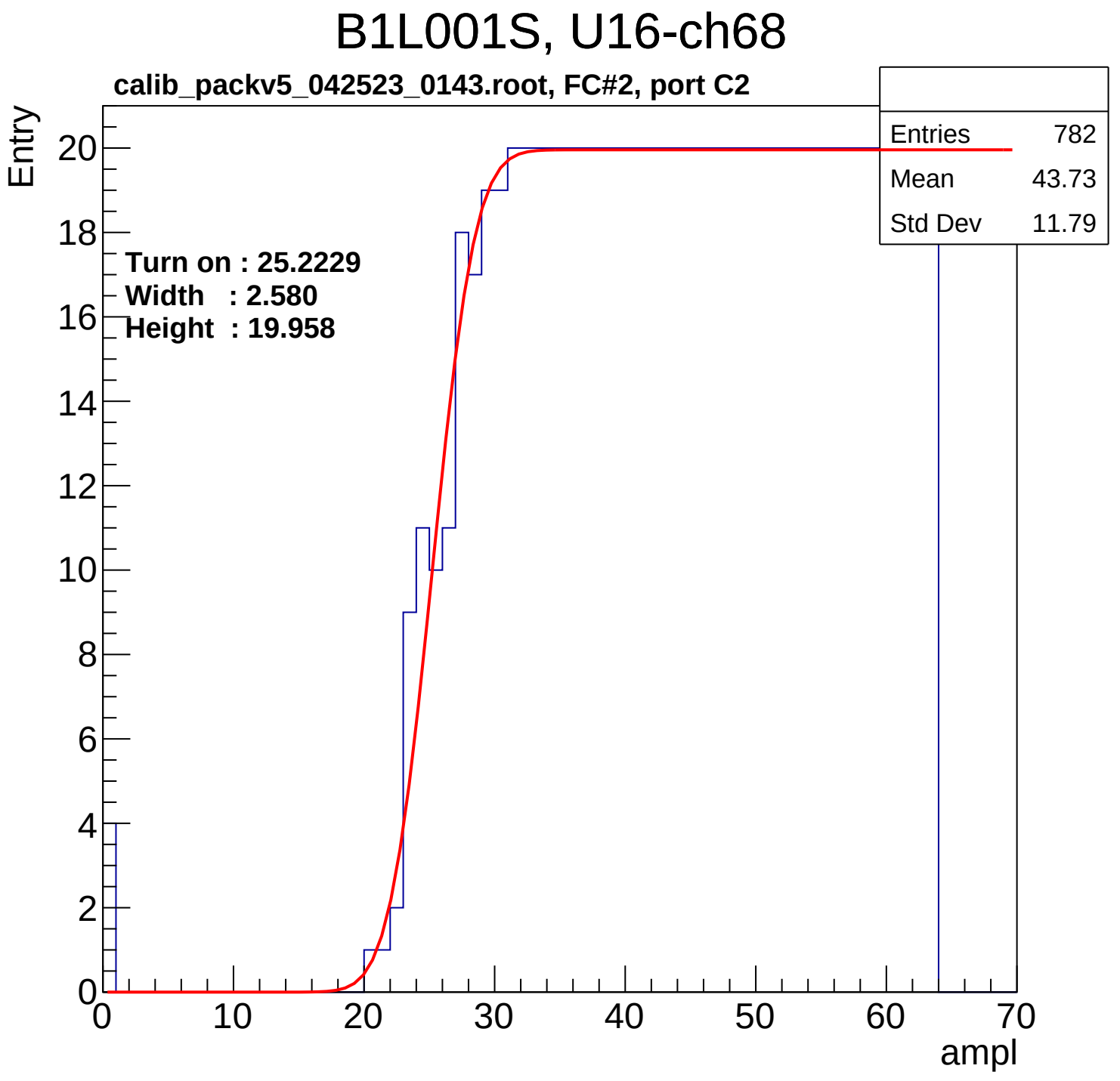
B1L001S, U16-ch68
calib_packv5_042523_0143.root, FC#2, port C2
Entries 782
Mean 43.73
Std Dev 11.79
Turn on : 25.2229
Width : 2.580
Height : 19.958
Entry
ampl
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8
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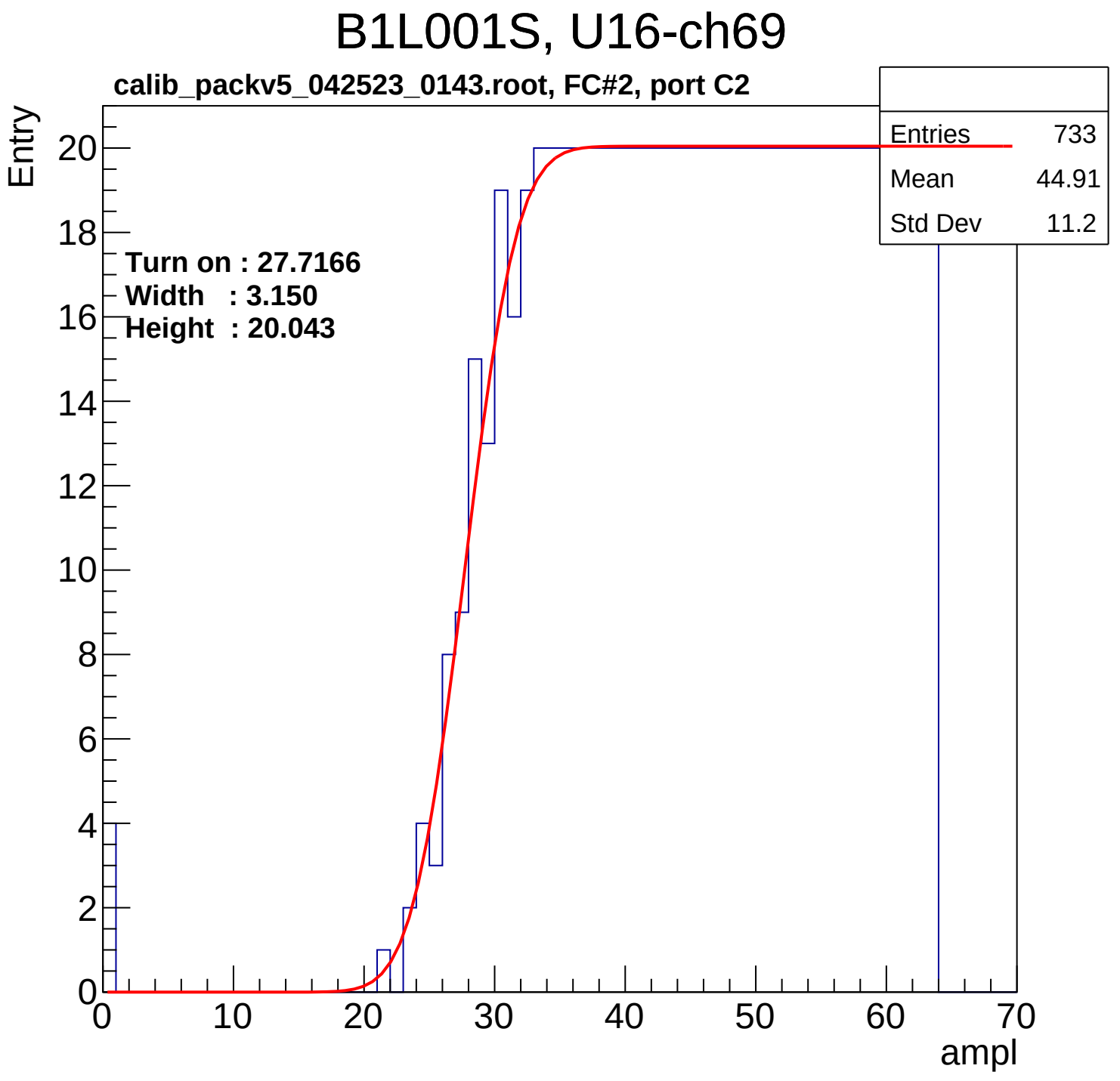
B1L001S, U16-ch69
calib_packv5_042523_0143.root, FC#2, port C2
Entries 733
Mean 44.91
Std Dev 11.2
Turn on : 27.7166
Width : 3.150
Height : 20.043
Entry
ampl
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6
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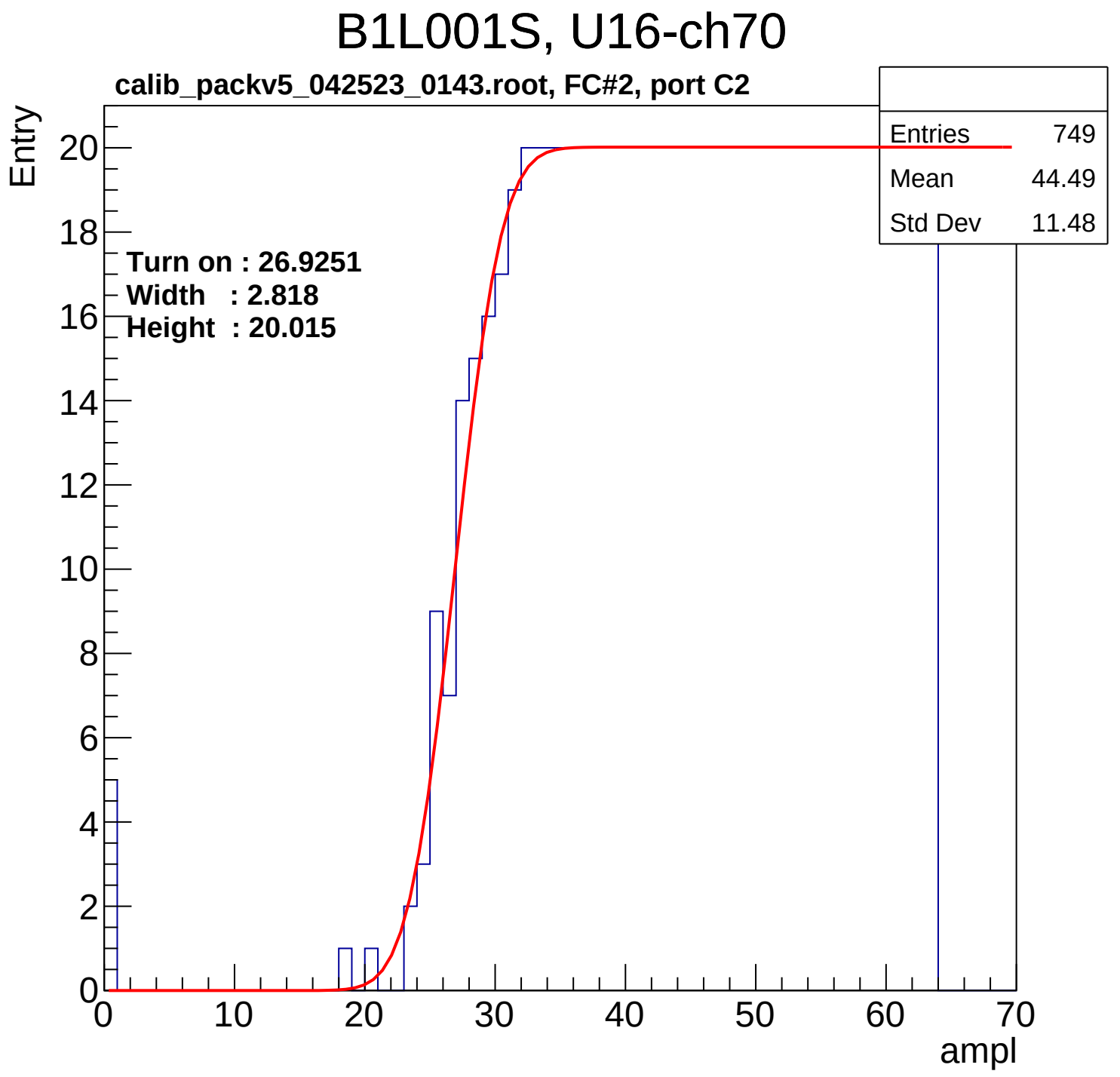
B1L001S, U16-ch70
calib_packv5_042523_0143.root, FC#2, port C2
Entries 749
Mean 44.49
Std Dev 11.48
Turn on : 26.9251
Width : 2.818
Height : 20.015
Entry
ampl
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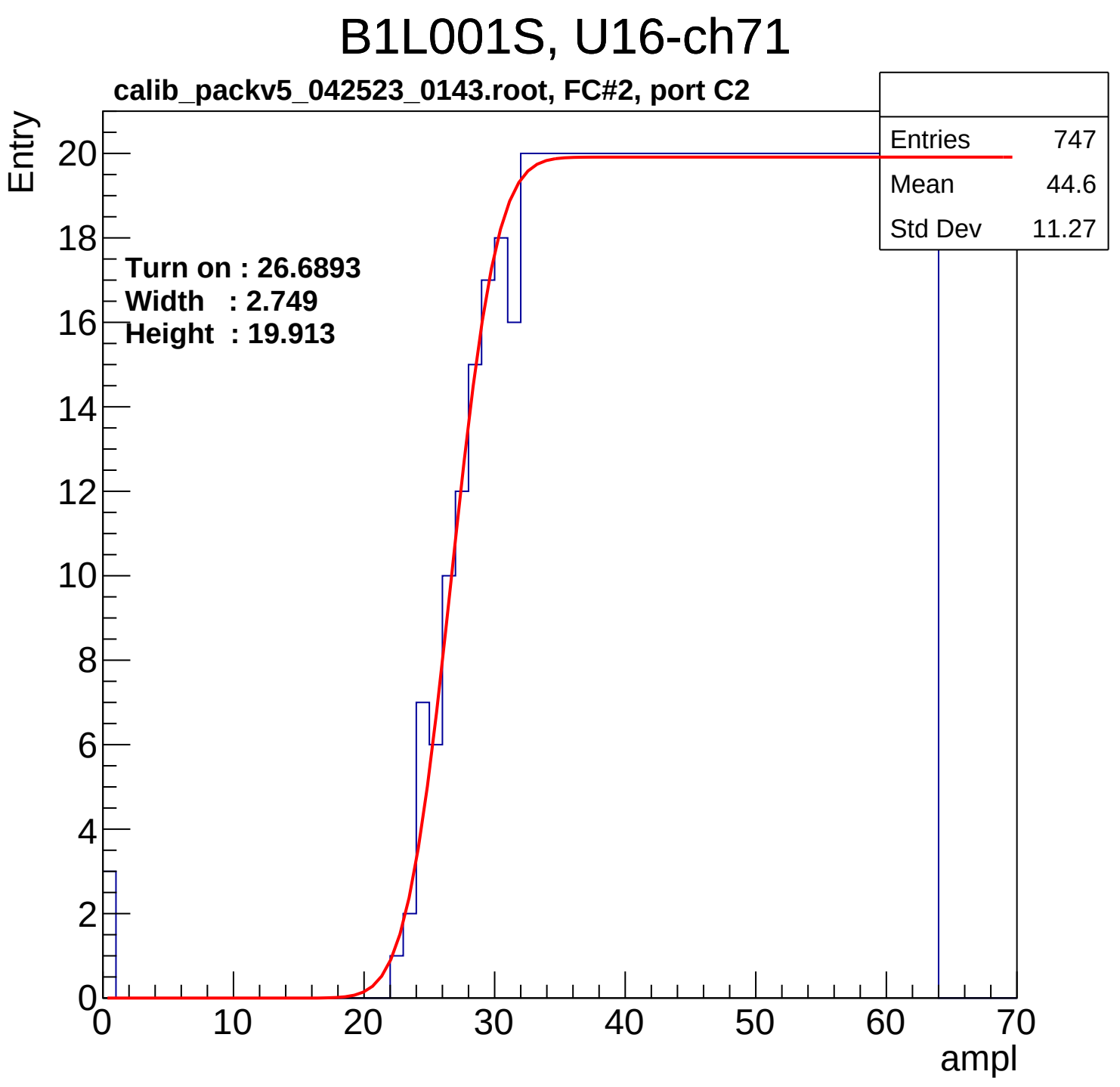
B1L001S, U16-ch71
calib_packv5_042523_0143.root, FC#2, port C2
Entries 747
Mean 44.6
Std Dev 11.27
Turn on : 26.6893
Width : 2.749
Height : 19.913
Entry
ampl
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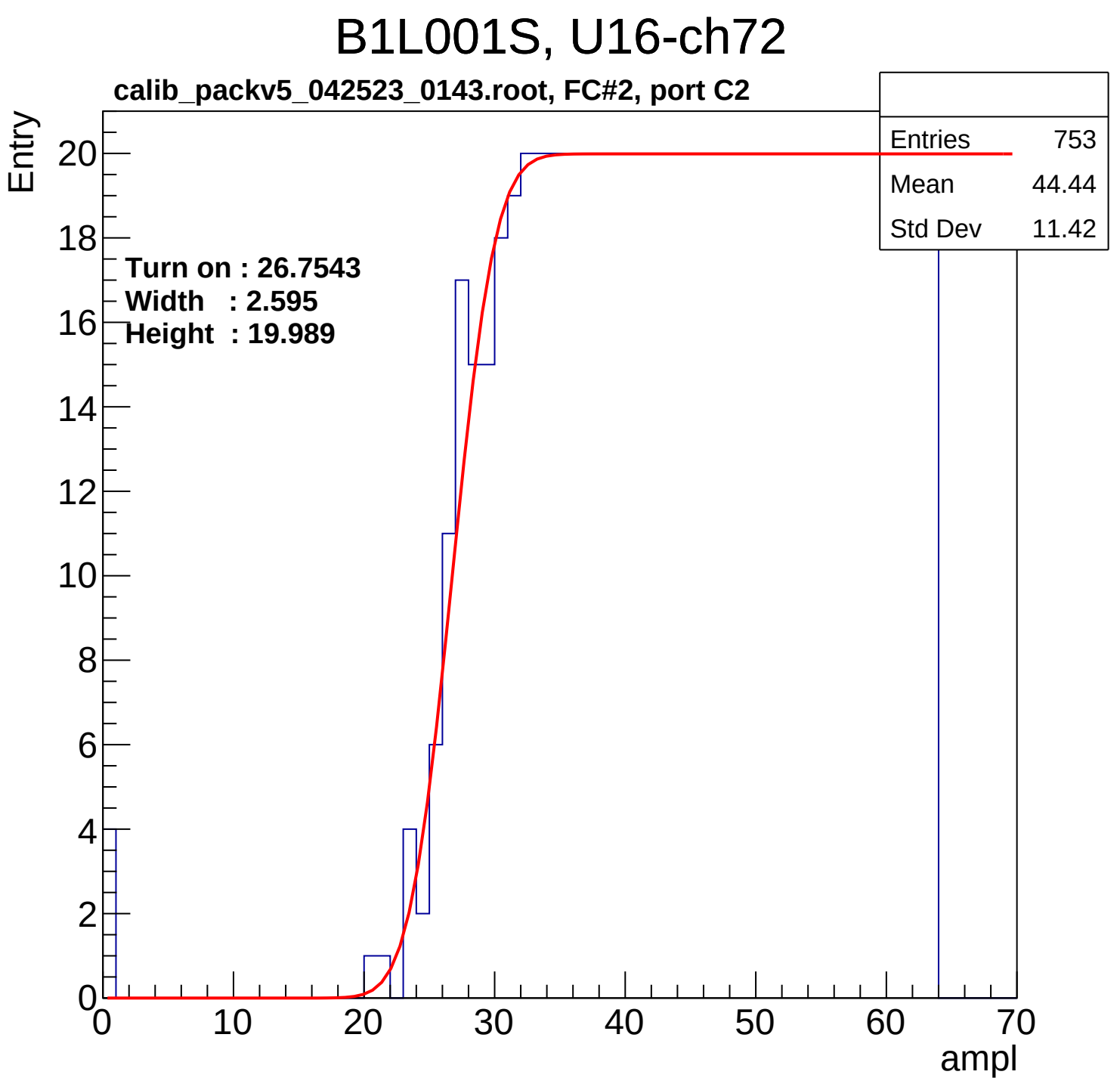
B1L001S, U16-ch72
calib_packv5_042523_0143.root, FC#2, port C2
Entries 753
Mean 44.44
Std Dev 11.42
Turn on : 26.7543
Width : 2.595
Height : 19.989
Entry
ampl
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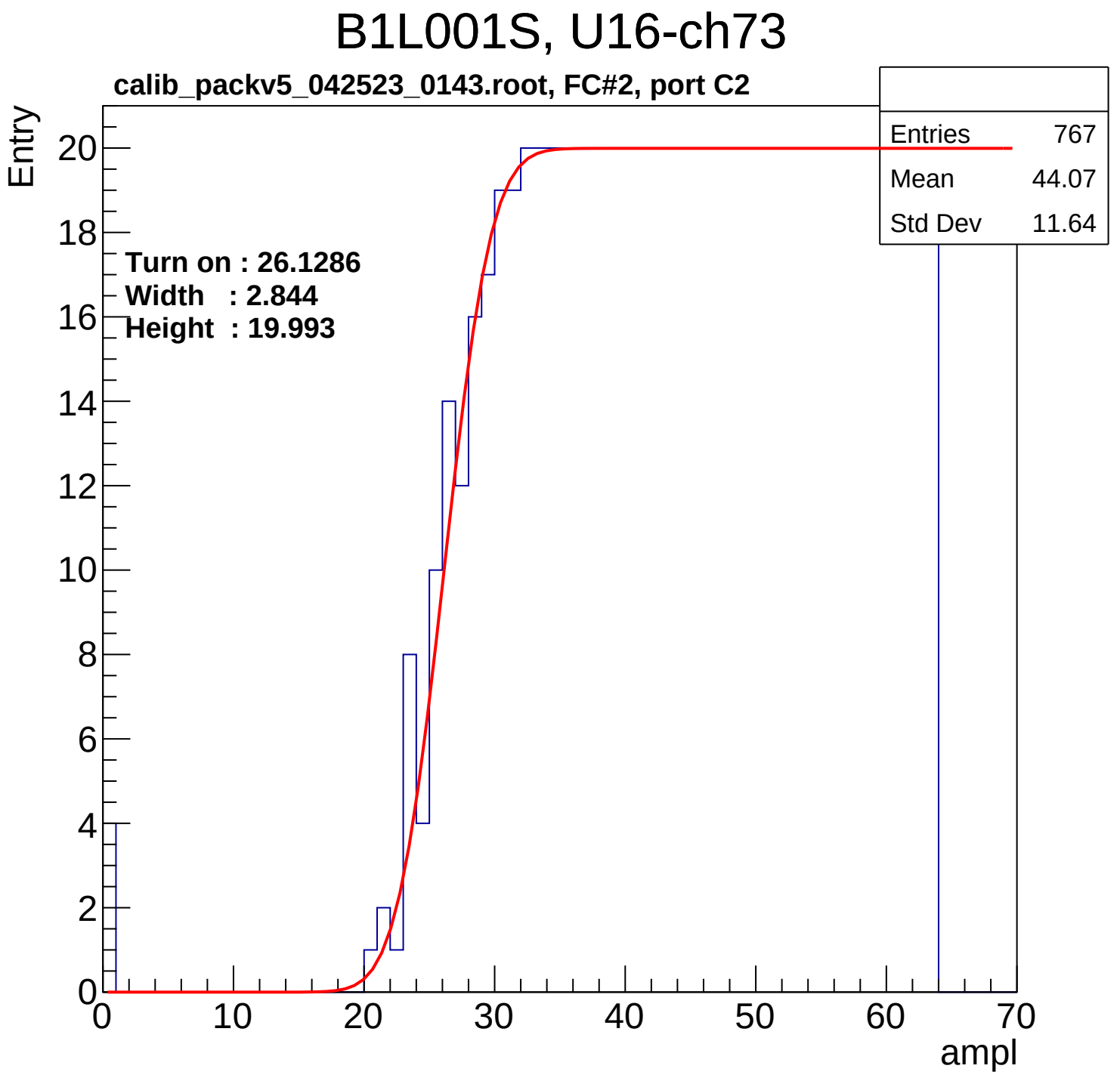
B1L001S, U16-ch73
calib_packv5_042523_0143.root, FC#2, port C2
Entries 767
Mean 44.07
Std Dev 11.64
Turn on : 26.1286
Width : 2.844
Height : 19.993
Entry
ampl
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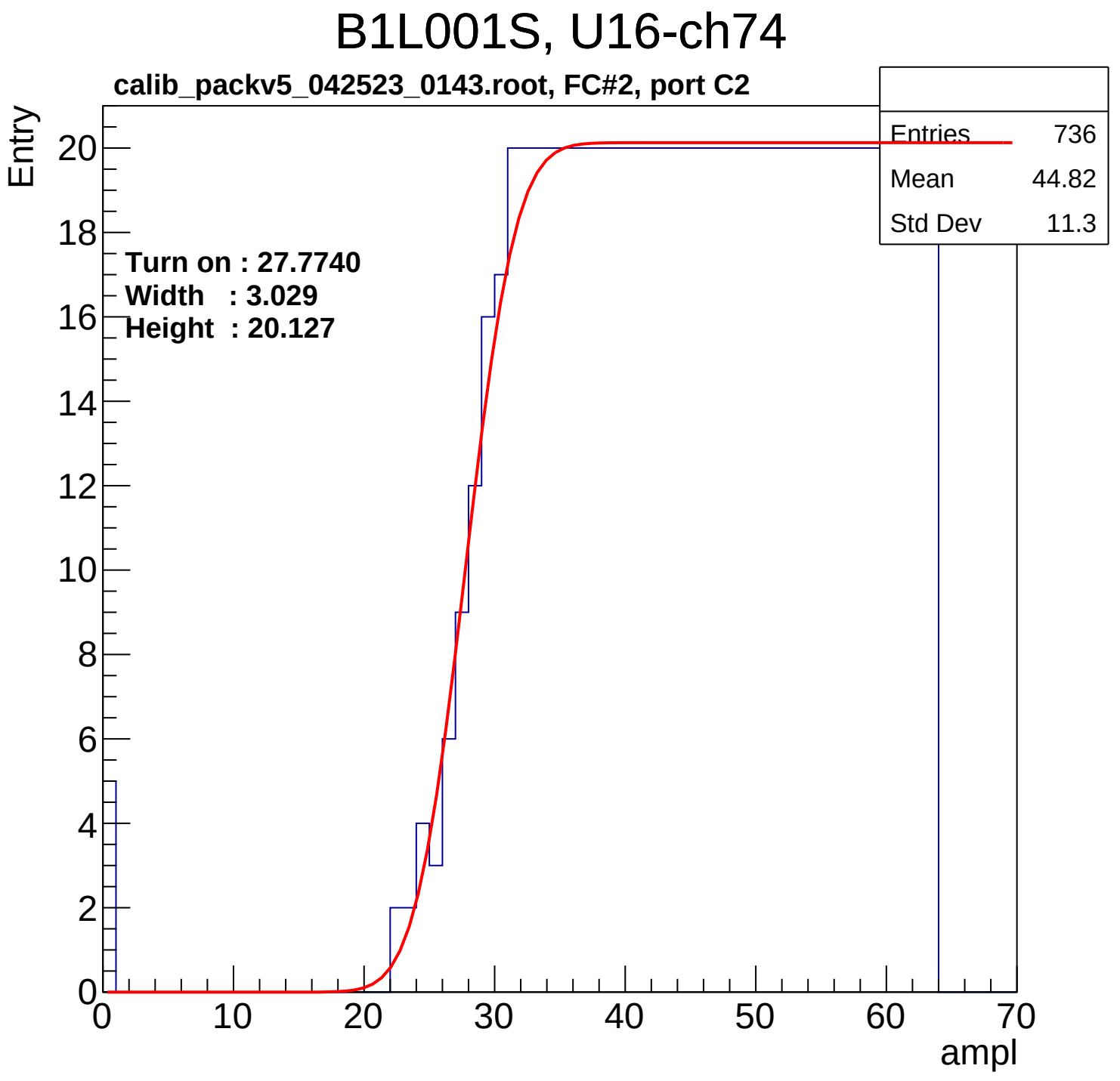
B1L001S, U16-ch74
calib_packv5_042523_0143.root, FC#2, port C2
Entries 736
Mean 44.82
Std Dev 11.3
Turn on : 27.7740
Width : 3.029
Height : 20.127
Entry
ampl
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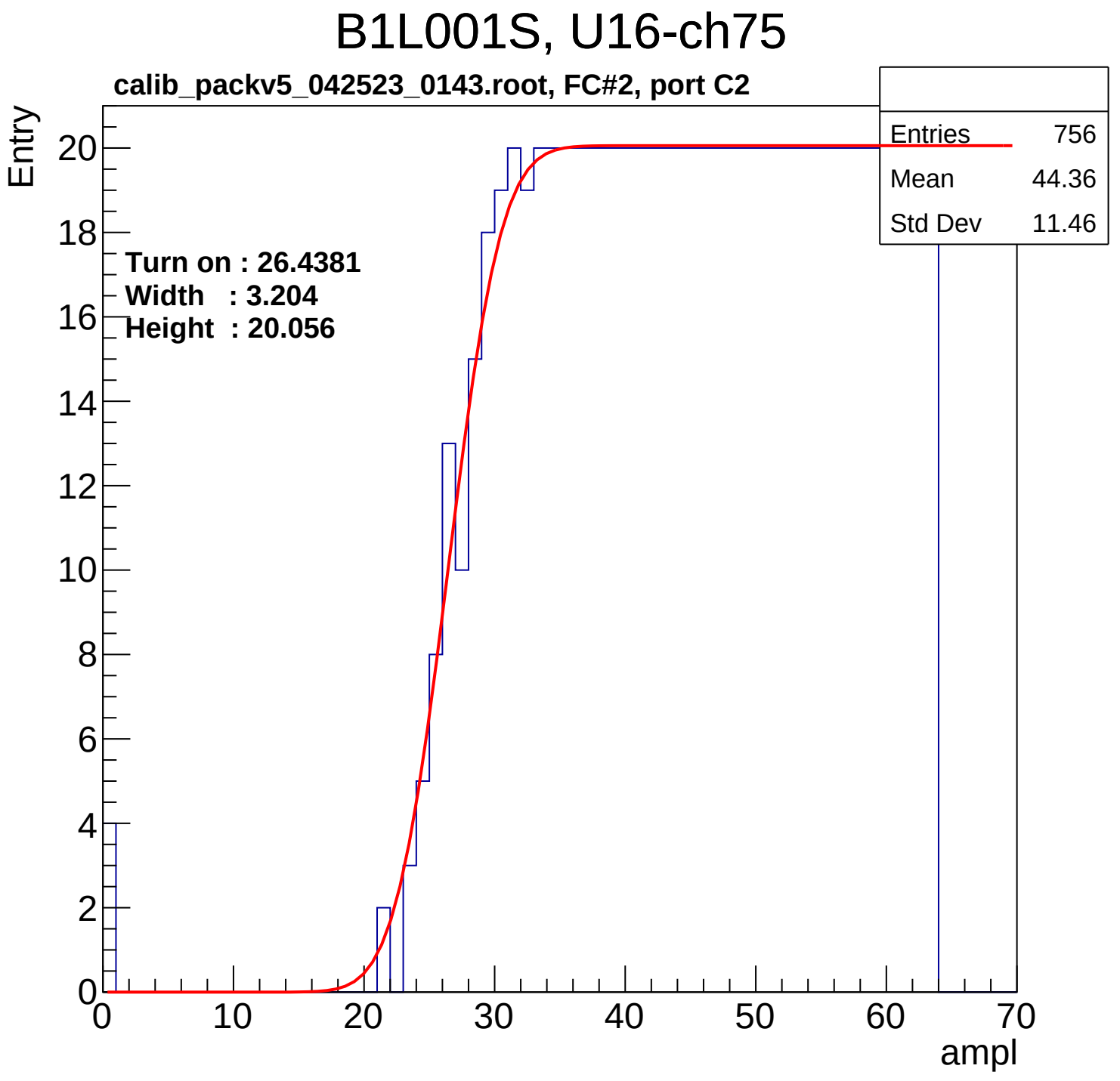
B1L001S, U16-ch75
calib_packv5_042523_0143.root, FC#2, port C2
Entries 756
Mean 44.36
Std Dev 11.46
Turn on : 26.4381
Width : 3.204
Height : 20.056
Entry
ampl
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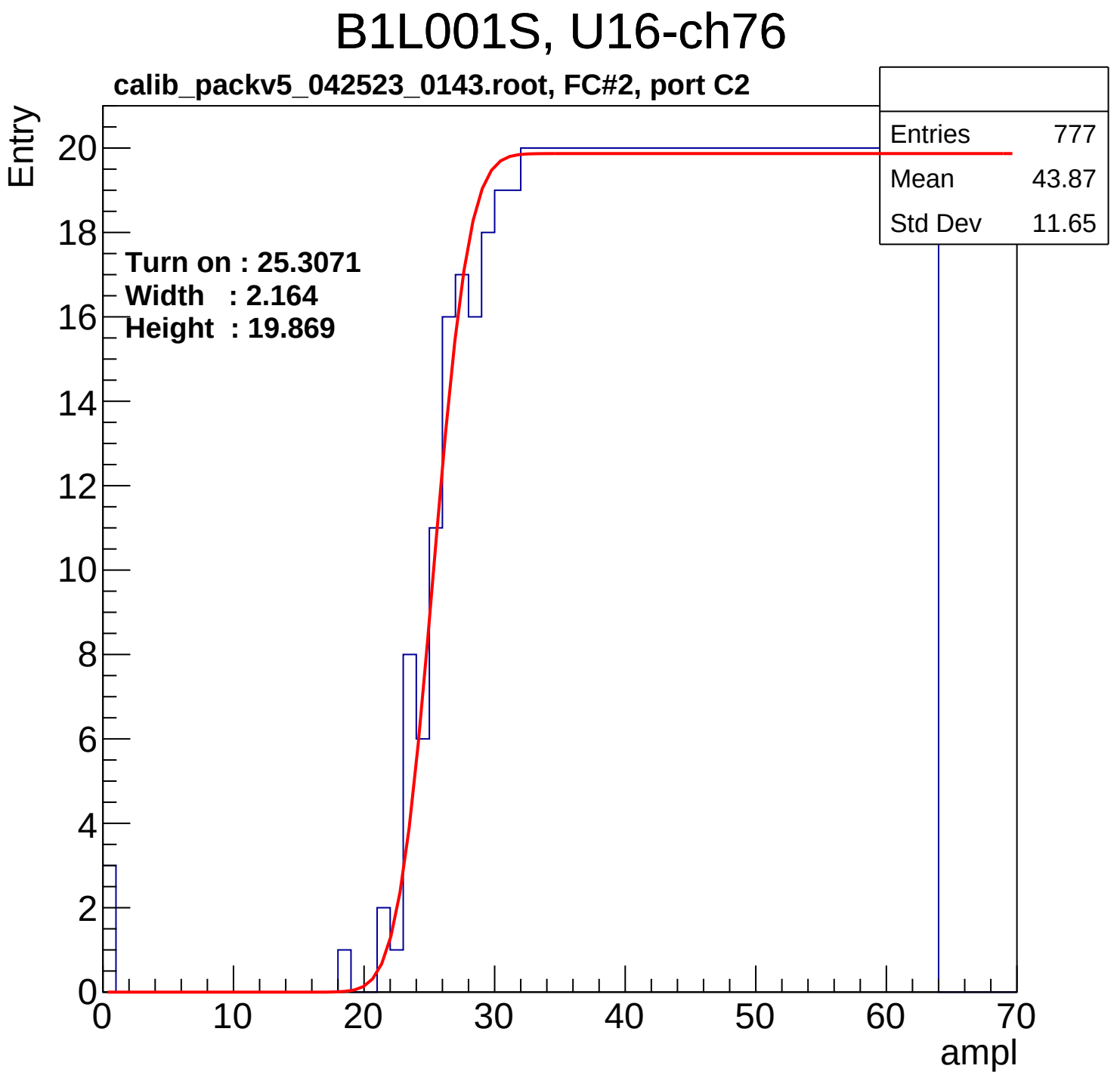
B1L001S, U16-ch76
calib_packv5_042523_0143.root, FC#2, port C2
Entries 777
Mean 43.87
Std Dev 11.65
Turn on : 25.3071
Width : 2.164
Height : 19.869
Entry
ampl
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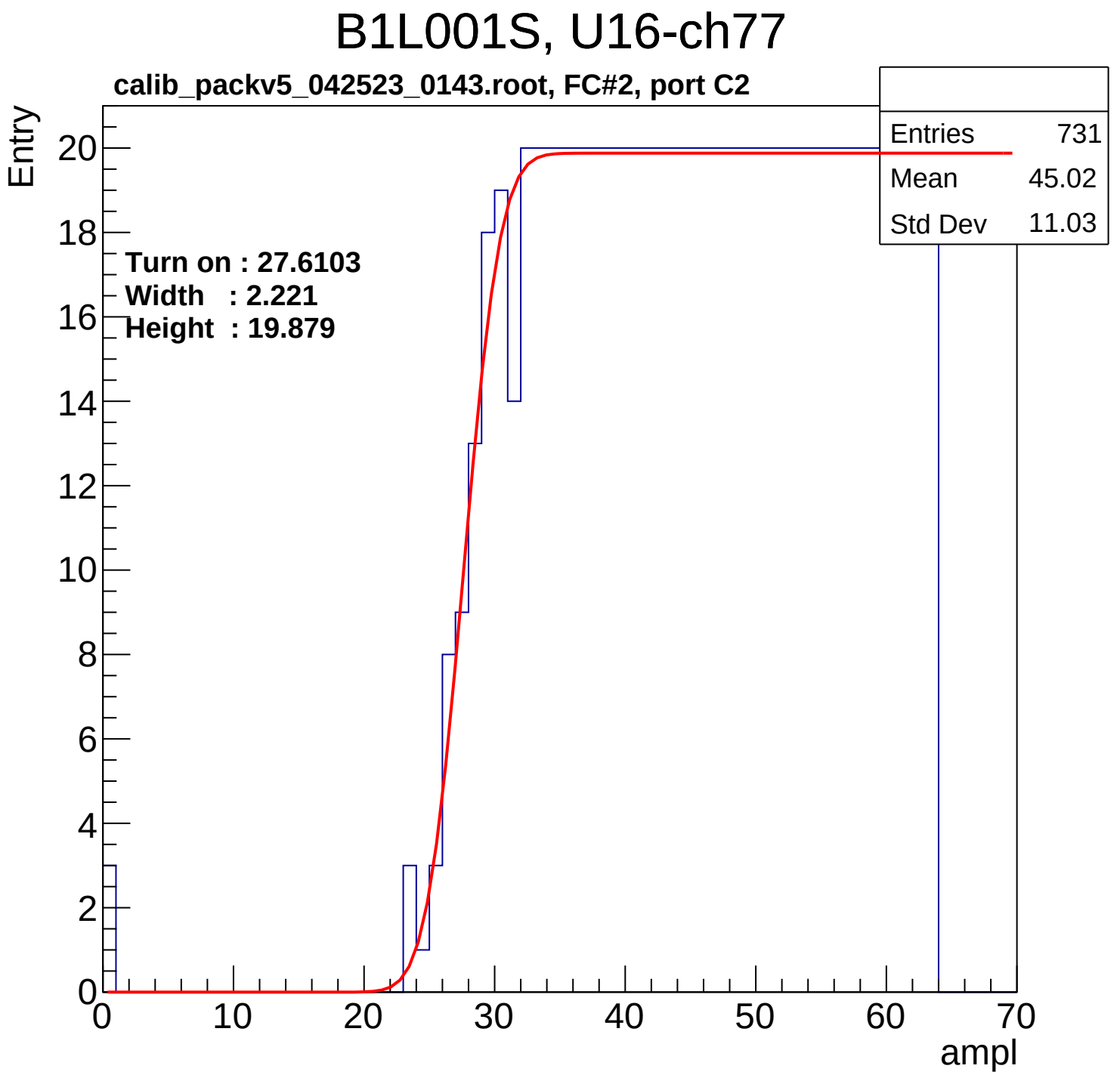
B1L001S, U16-ch77
calib_packv5_042523_0143.root, FC#2, port C2
Entries 731
Mean 45.02
Std Dev 11.03
Turn on : 27.6103
Width : 2.221
Height : 19.879
Entry
ampl
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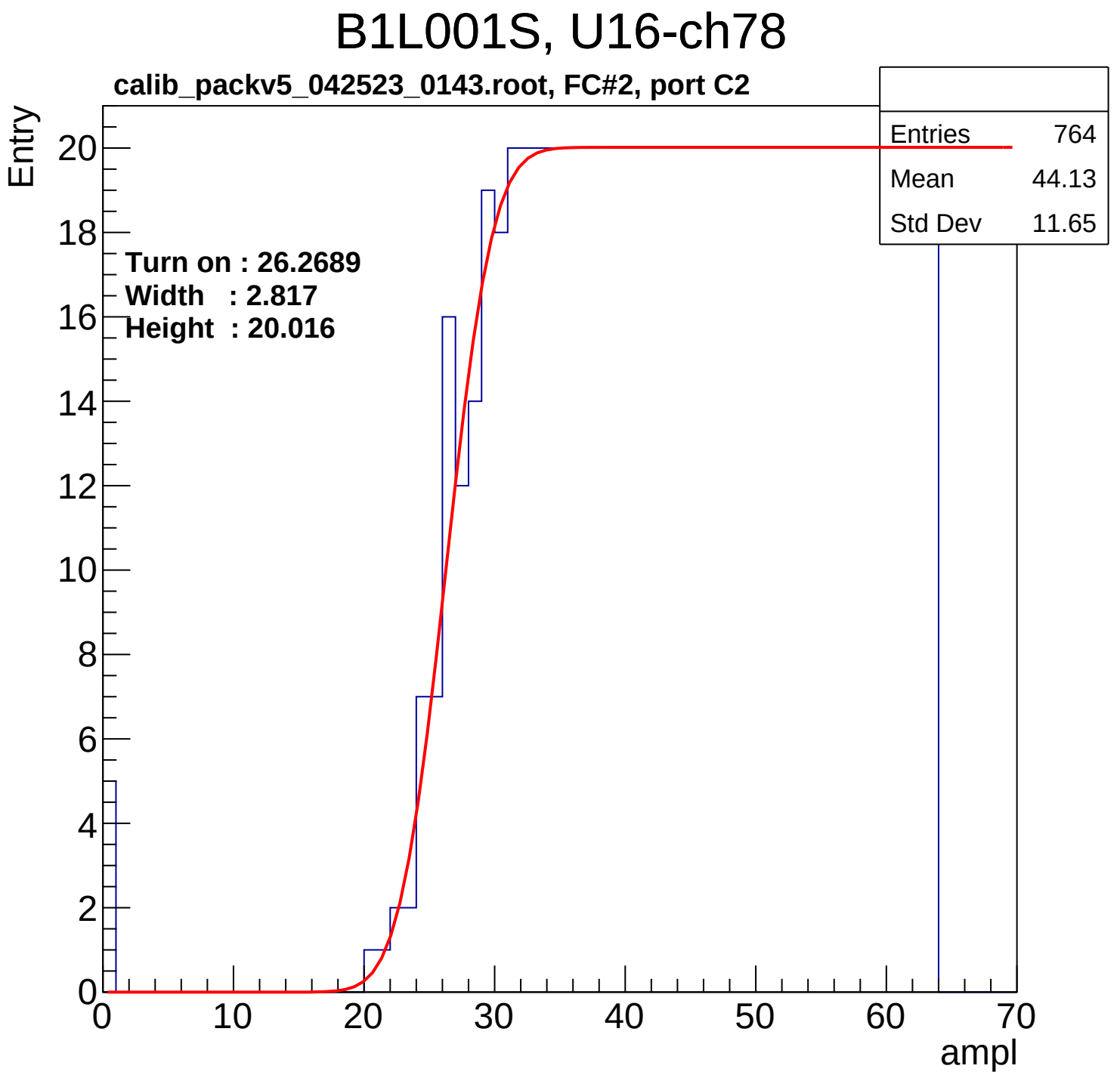
B1L001S, U16-ch78
calib_packv5_042523_0143.root, FC#2, port C2
Entries 764
Mean 44.13
Std Dev 11.65
Turn on : 26.2689
Width : 2.817
Height : 20.016
Entry
ampl
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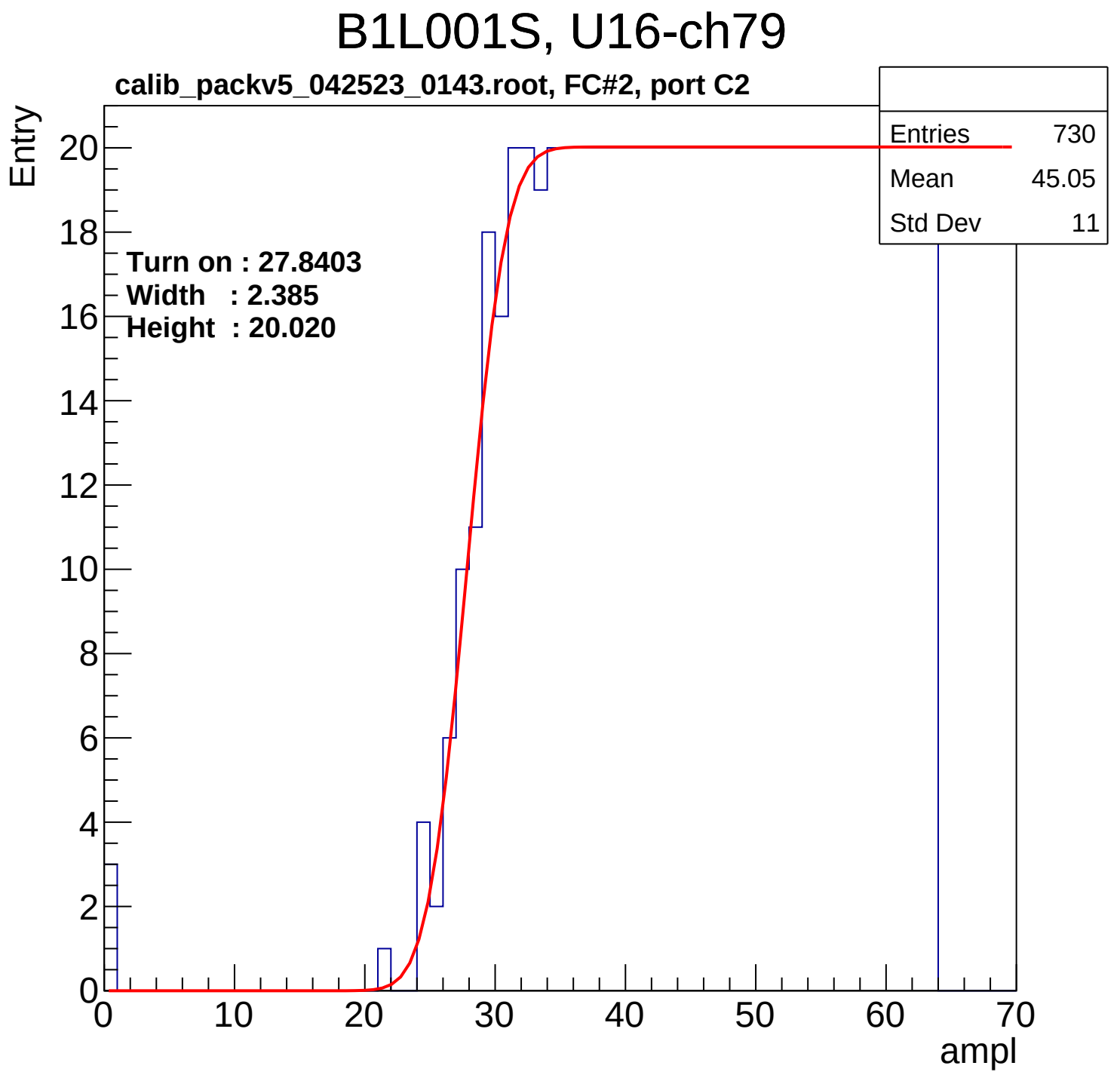
B1L001S, U16-ch79
calib_packv5_042523_0143.root, FC#2, port C2
Entries 730
Mean 45.05
Std Dev 11
Turn on : 27.8403
Width : 2.385
Height : 20.020
Entry
ampl
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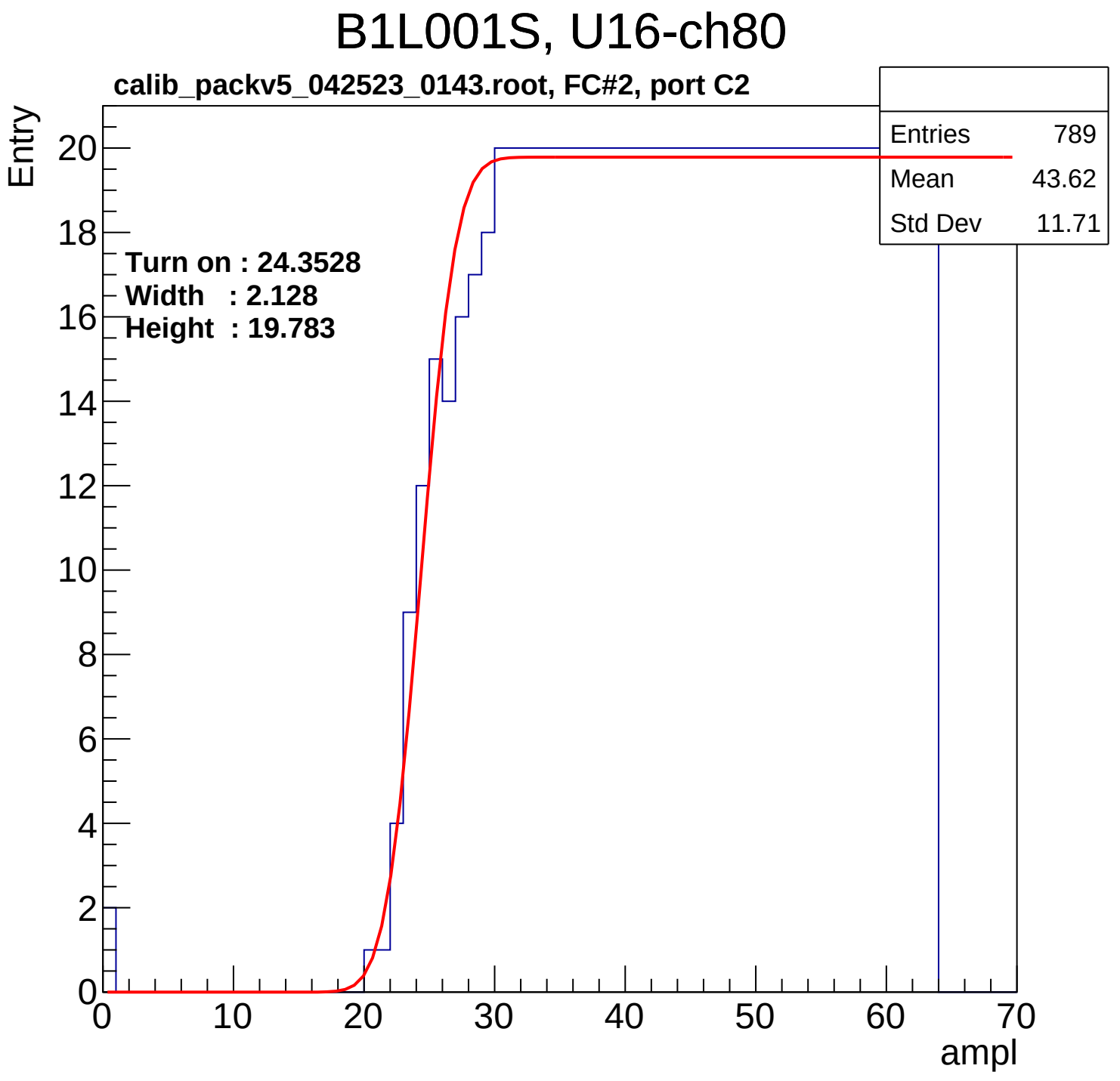
B1L001S, U16-ch80
calib_packv5_042523_0143.root, FC#2, port C2
Entries 789
Mean 43.62
Std Dev 11.71
Turn on : 24.3528
Width : 2.128
Height : 19.783
Entry
ampl
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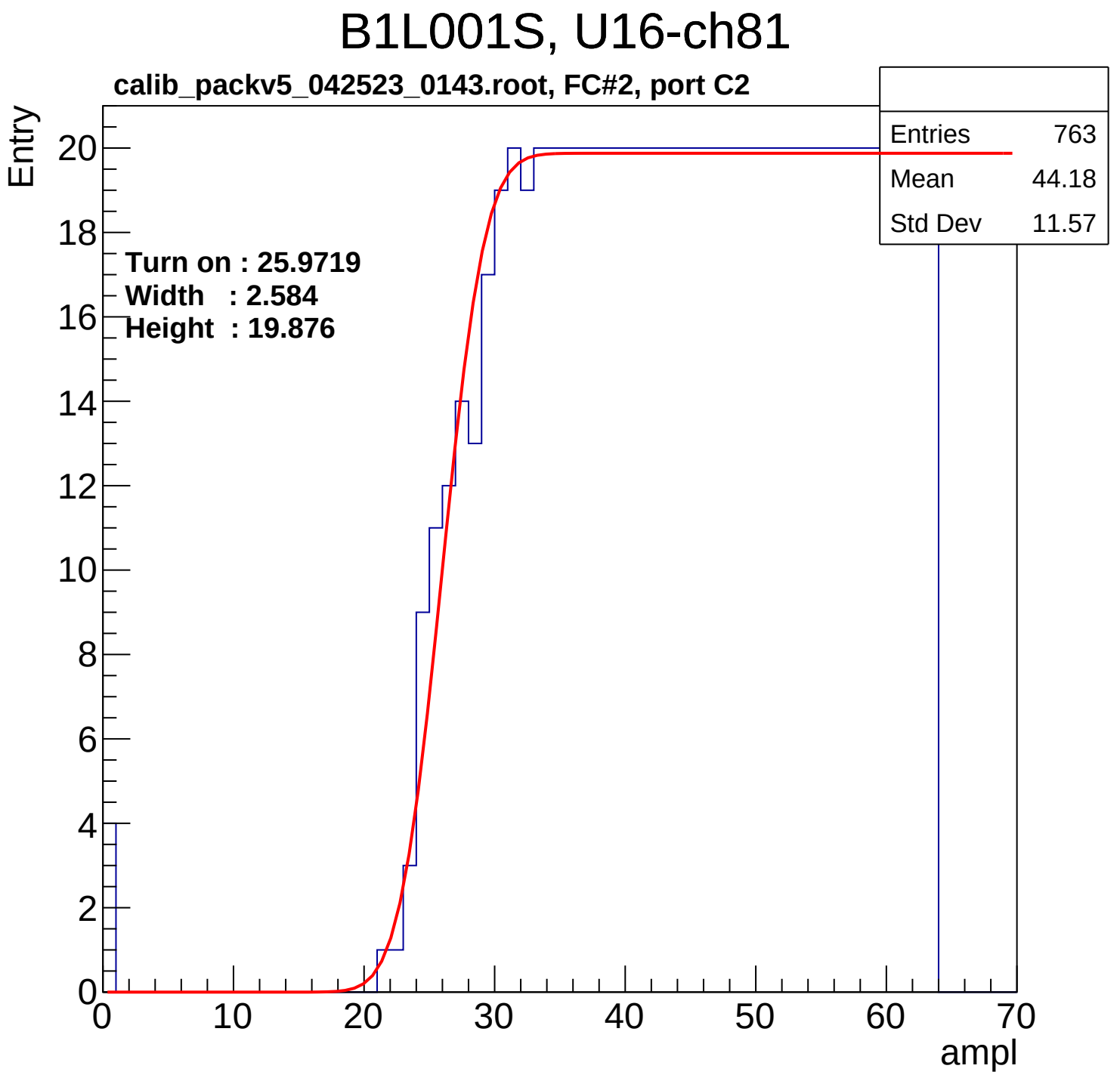
B1L001S, U16-ch81
calib_packv5_042523_0143.root, FC#2, port C2
Entries 763
Mean 44.18
Std Dev 11.57
Turn on : 25.9719
Width : 2.584
Height : 19.876
Entry
ampl
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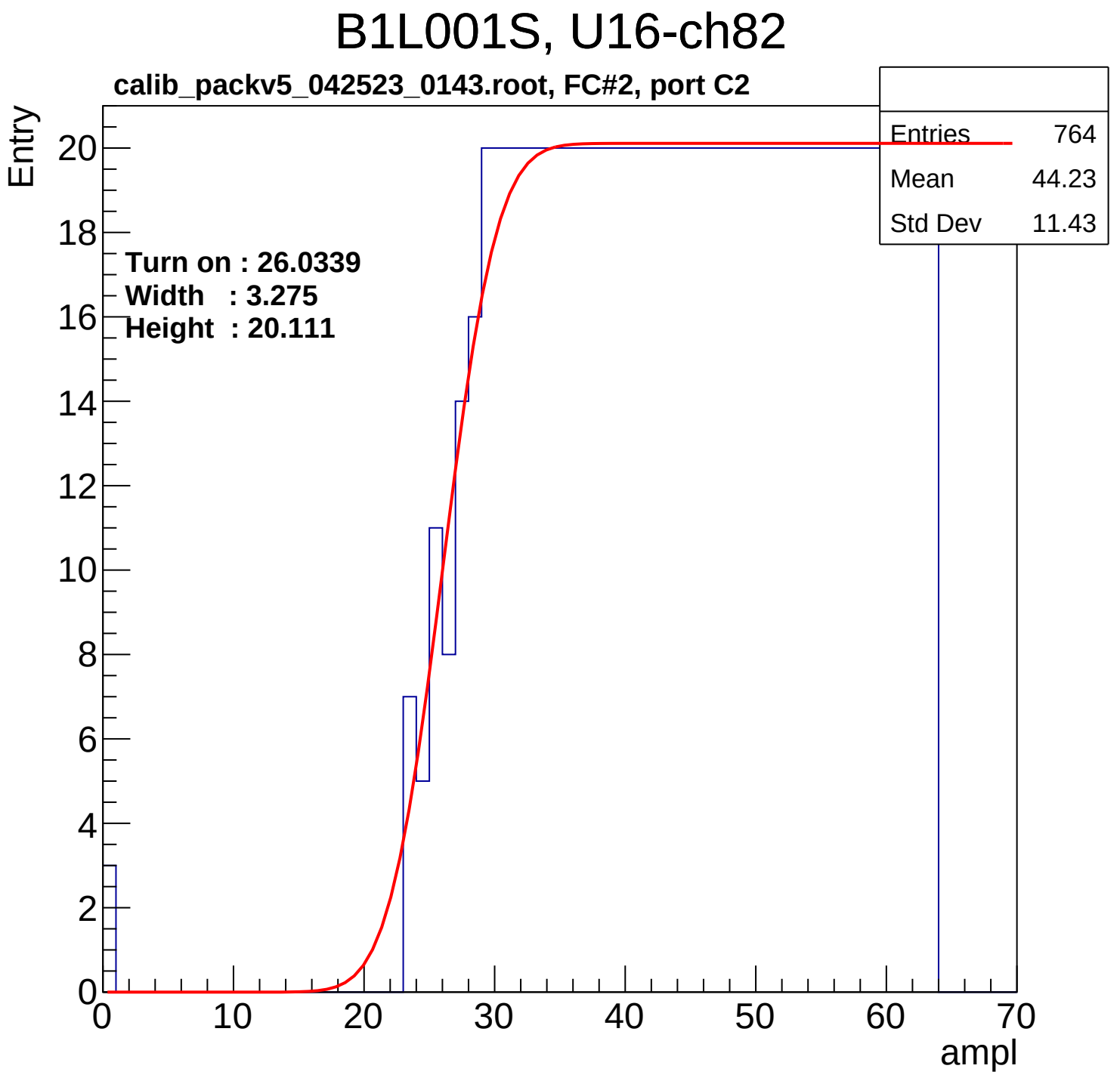
B1L001S, U16-ch82
calib_packv5_042523_0143.root, FC#2, port C2
Entries 764
Mean 44.23
Std Dev 11.43
Turn on : 26.0339
Width : 3.275
Height : 20.111
Entry
ampl
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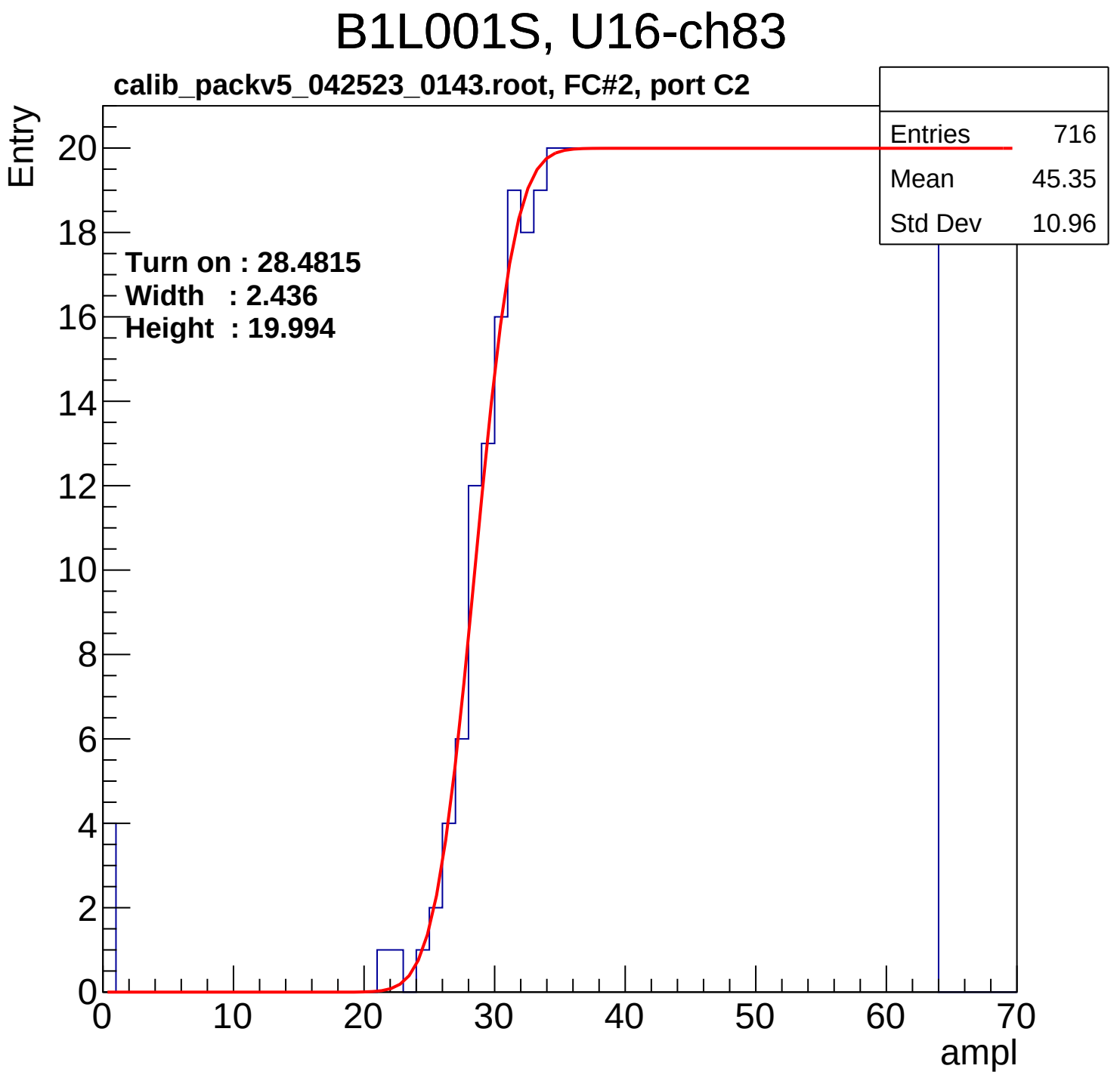
B1L001S, U16-ch83
calib_packv5_042523_0143.root, FC#2, port C2
Entries 716
Mean 45.35
Std Dev 10.96
Turn on : 28.4815
Width : 2.436
Height : 19.994
Entry
ampl
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2
4
6
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10
12
14
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18
20
0
10
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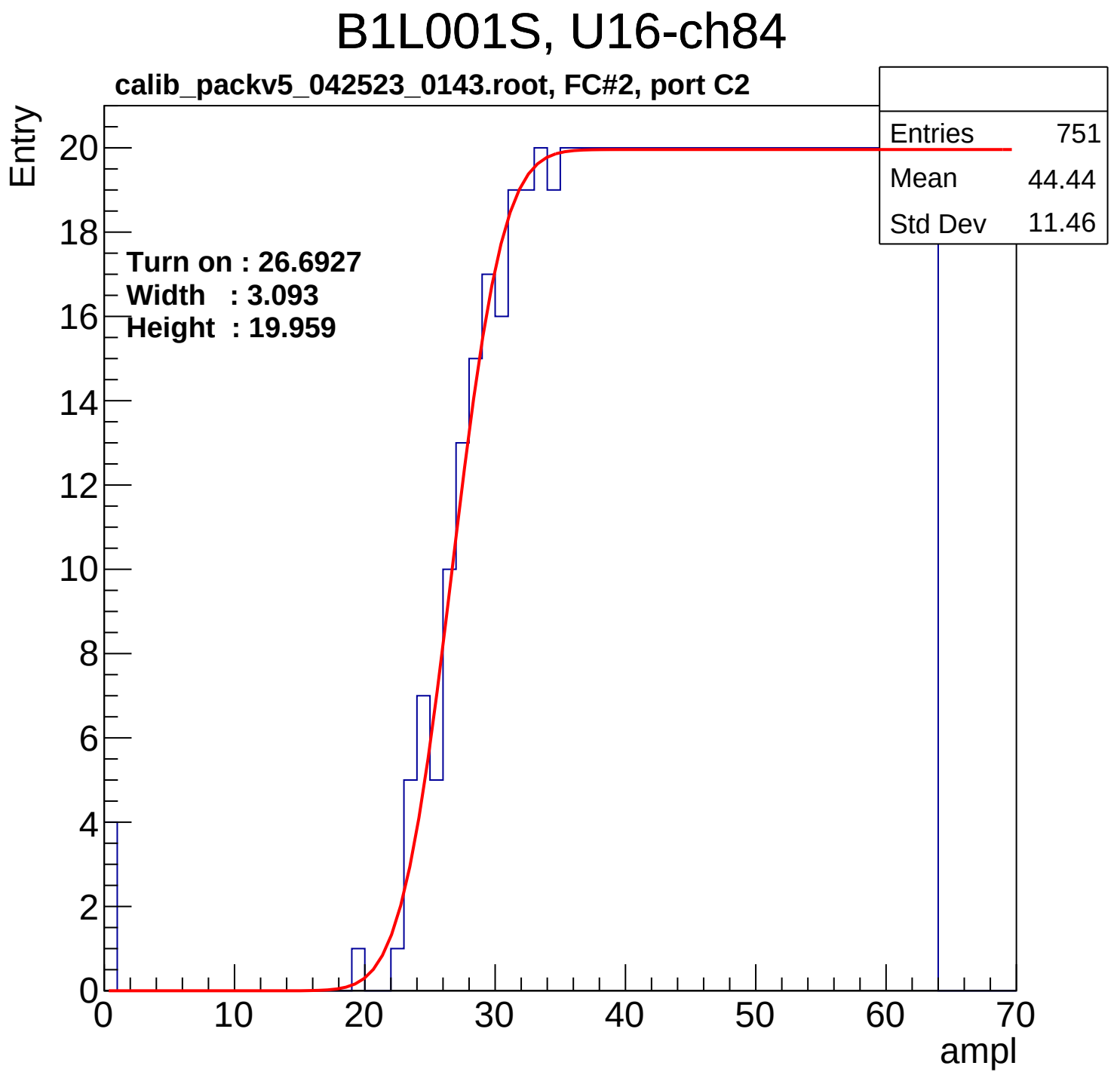
B1L001S, U16-ch84
calib_packv5_042523_0143.root, FC#2, port C2
Entries 751
Mean 44.44
Std Dev 11.46
Turn on : 26.6927
Width : 3.093
Height : 19.959
Entry
ampl
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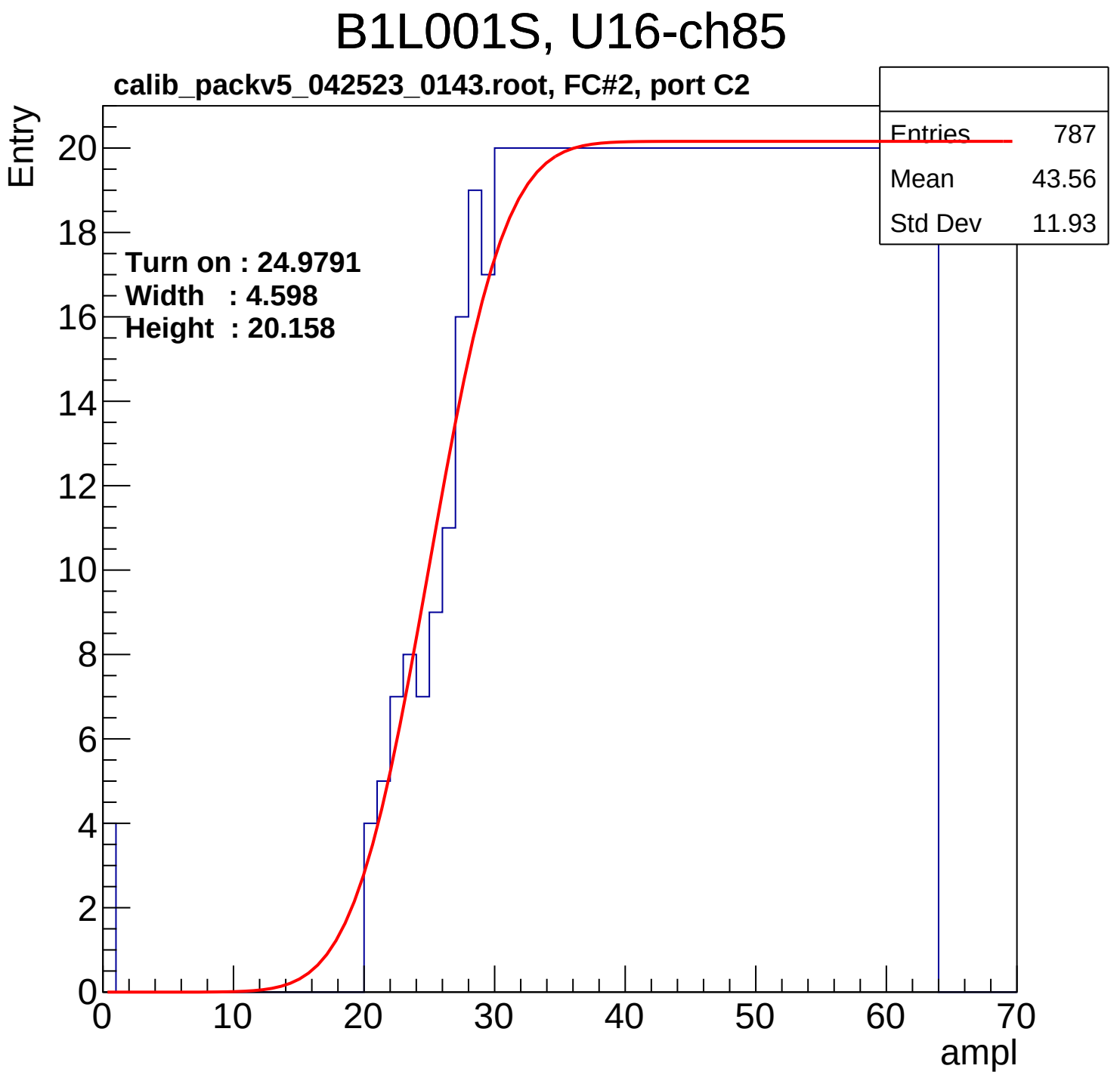
B1L001S, U16-ch85
calib_packv5_042523_0143.root, FC#2, port C2
Entries 787
Mean 43.56
Std Dev 11.93
Turn on : 24.9791
Width : 4.598
Height : 20.158
Entry
ampl
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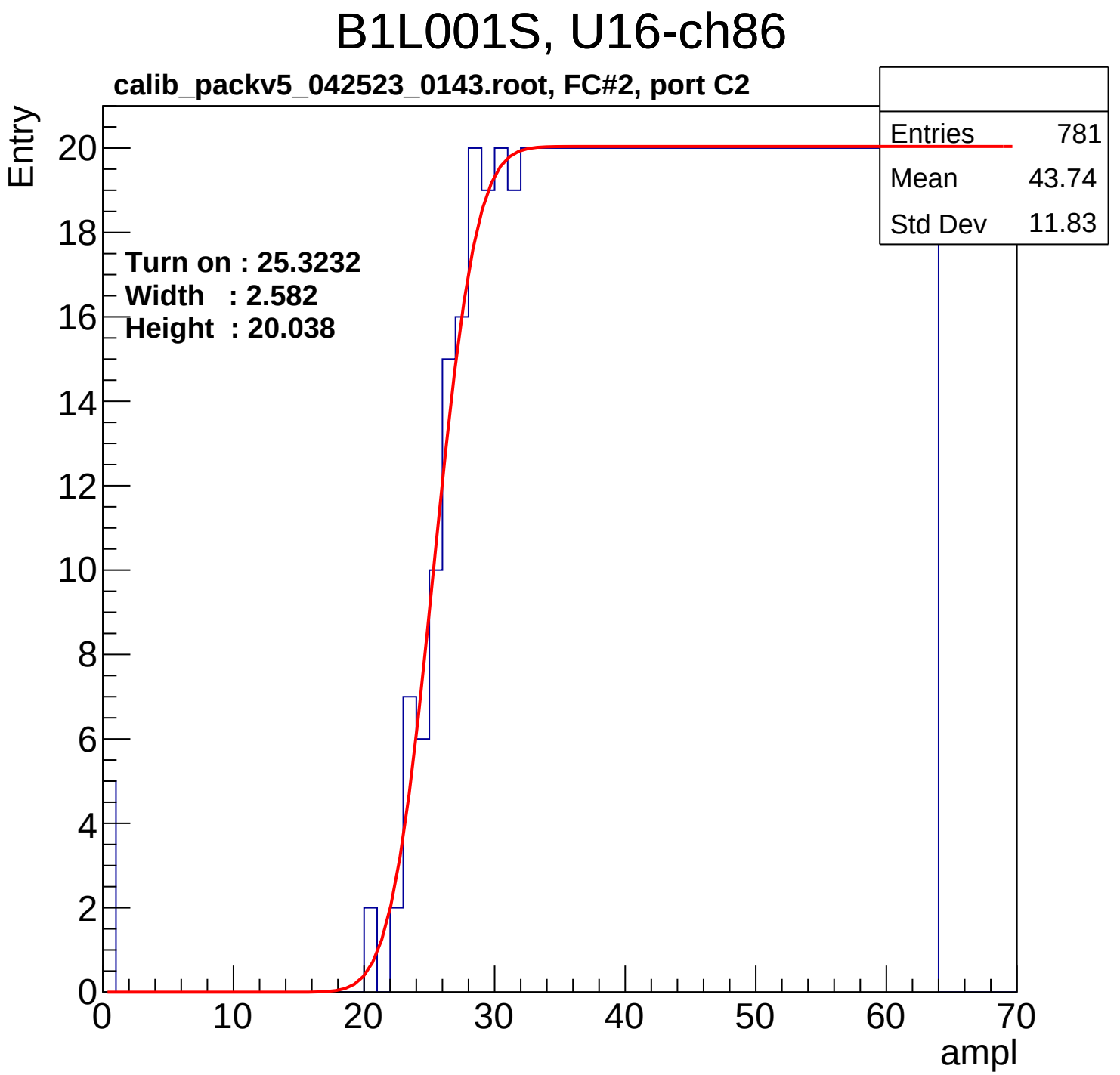
B1L001S, U16-ch86
calib_packv5_042523_0143.root, FC#2, port C2
Entries 781
Mean 43.74
Std Dev 11.83
Turn on : 25.3232
Width : 2.582
Height : 20.038
Entry
ampl
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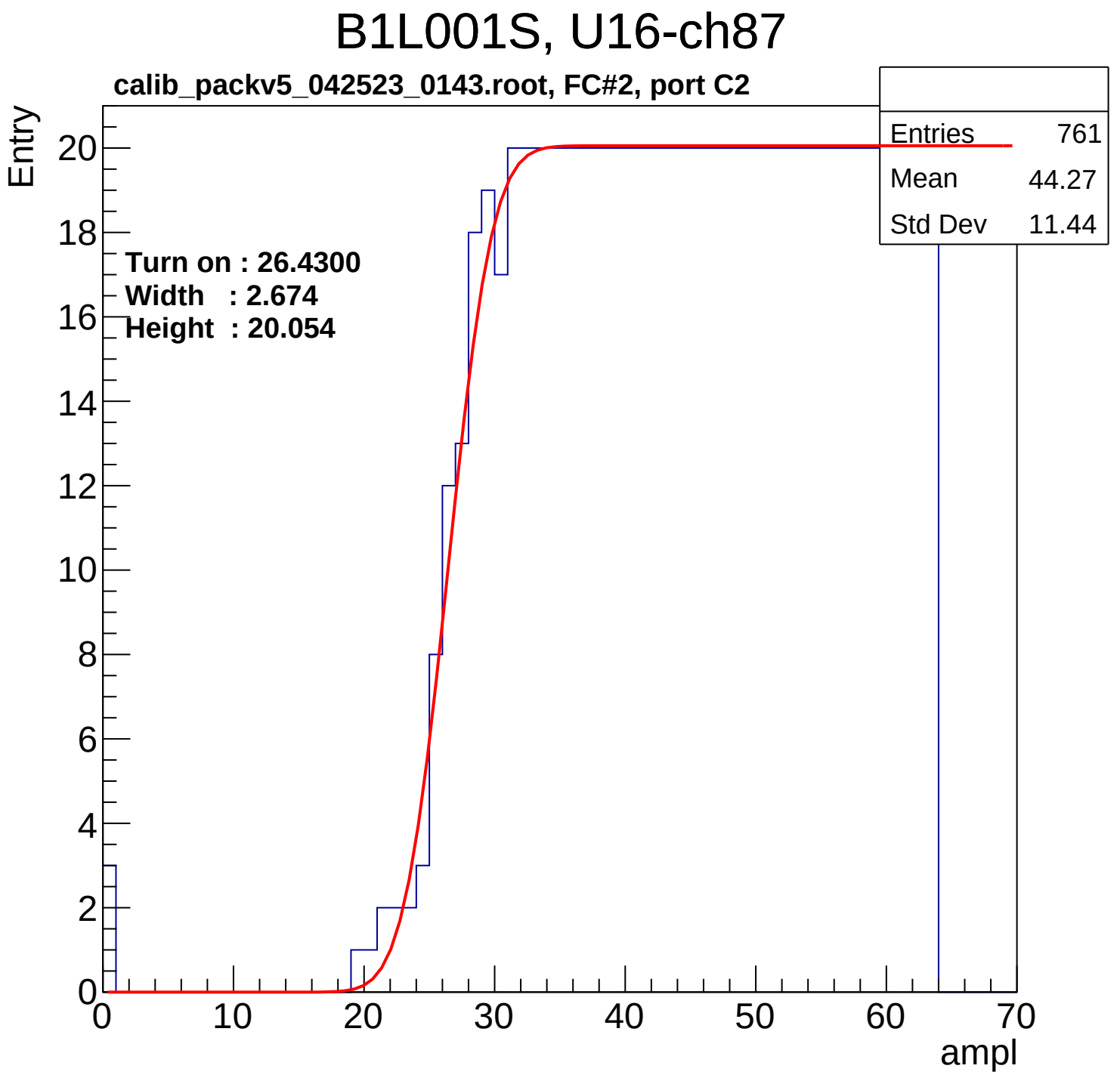
B1L001S, U16-ch87
calib_packv5_042523_0143.root, FC#2, port C2
Entries 761
Mean 44.27
Std Dev 11.44
Turn on : 26.4300
Width : 2.674
Height : 20.054
Entry
ampl
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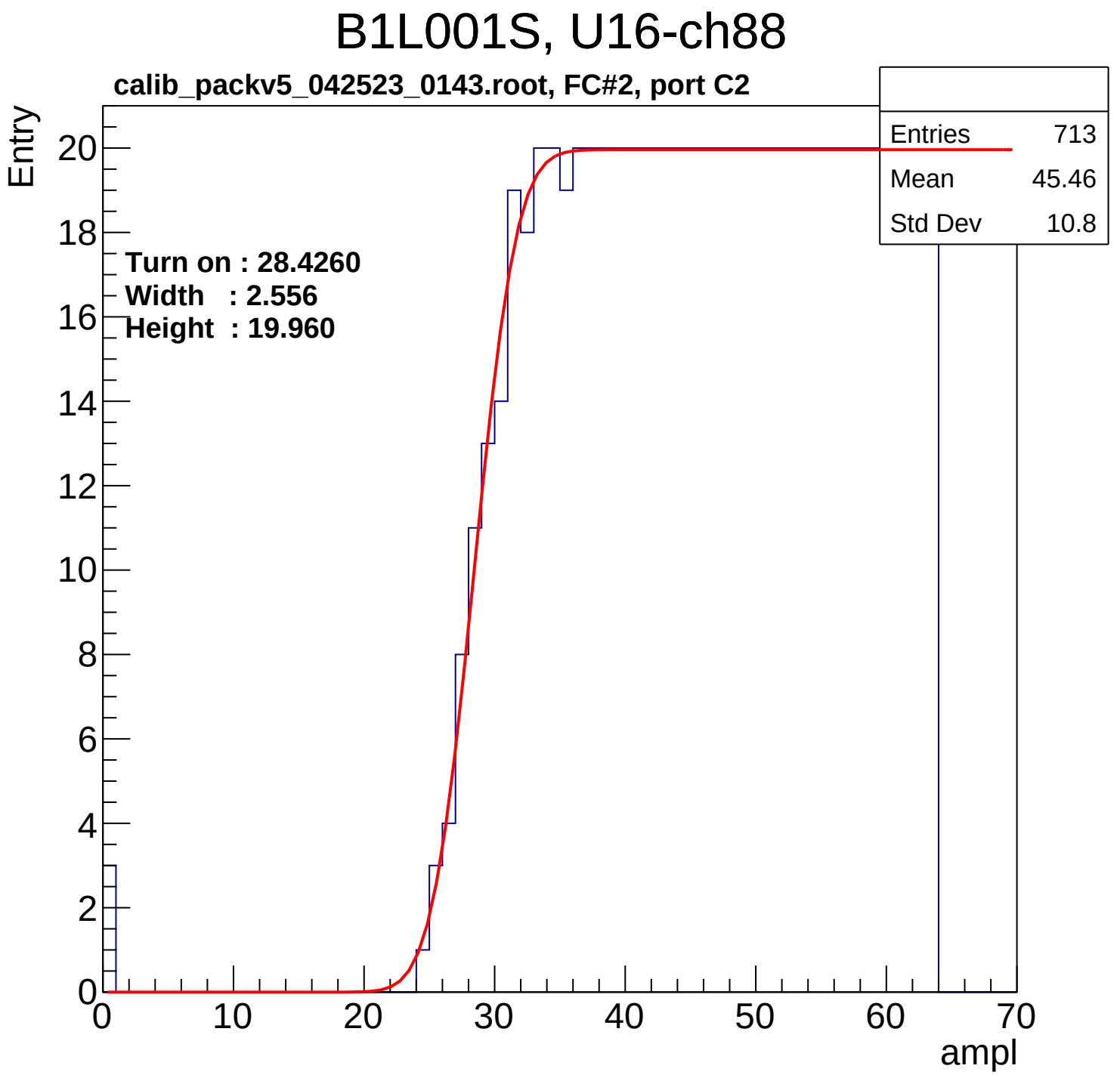
B1L001S, U16-ch88
calib_packv5_042523_0143.root, FC#2, port C2
Entries 713
Mean 45.46
Std Dev 10.8
Turn on : 28.4260
Width : 2.556
Height : 19.960
Entry
ampl
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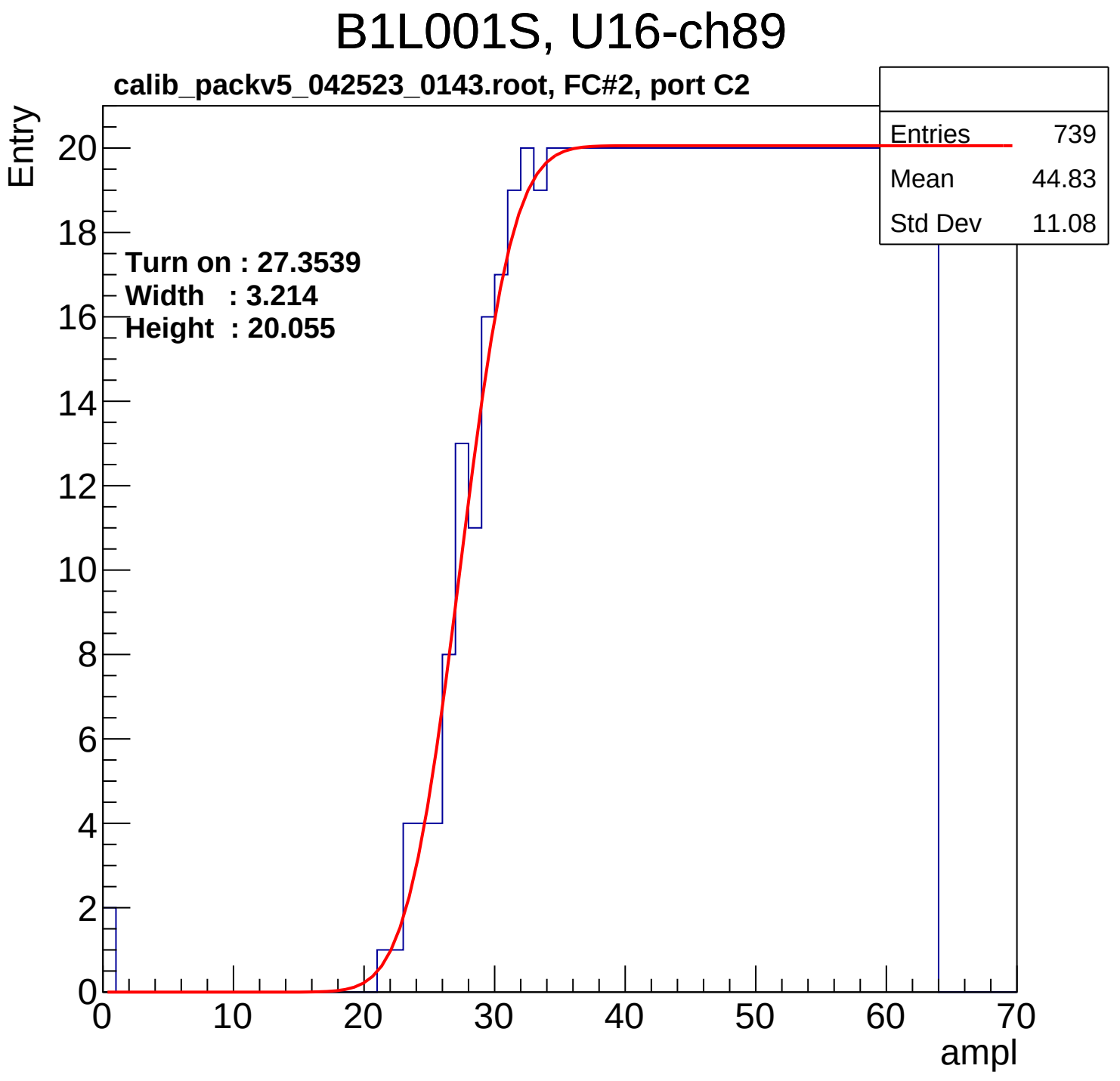
B1L001S, U16-ch89
calib_packv5_042523_0143.root, FC#2, port C2
Entries 739
Mean 44.83
Std Dev 11.08
Turn on : 27.3539
Width : 3.214
Height : 20.055
Entry
ampl
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6
8
10
12
14
16
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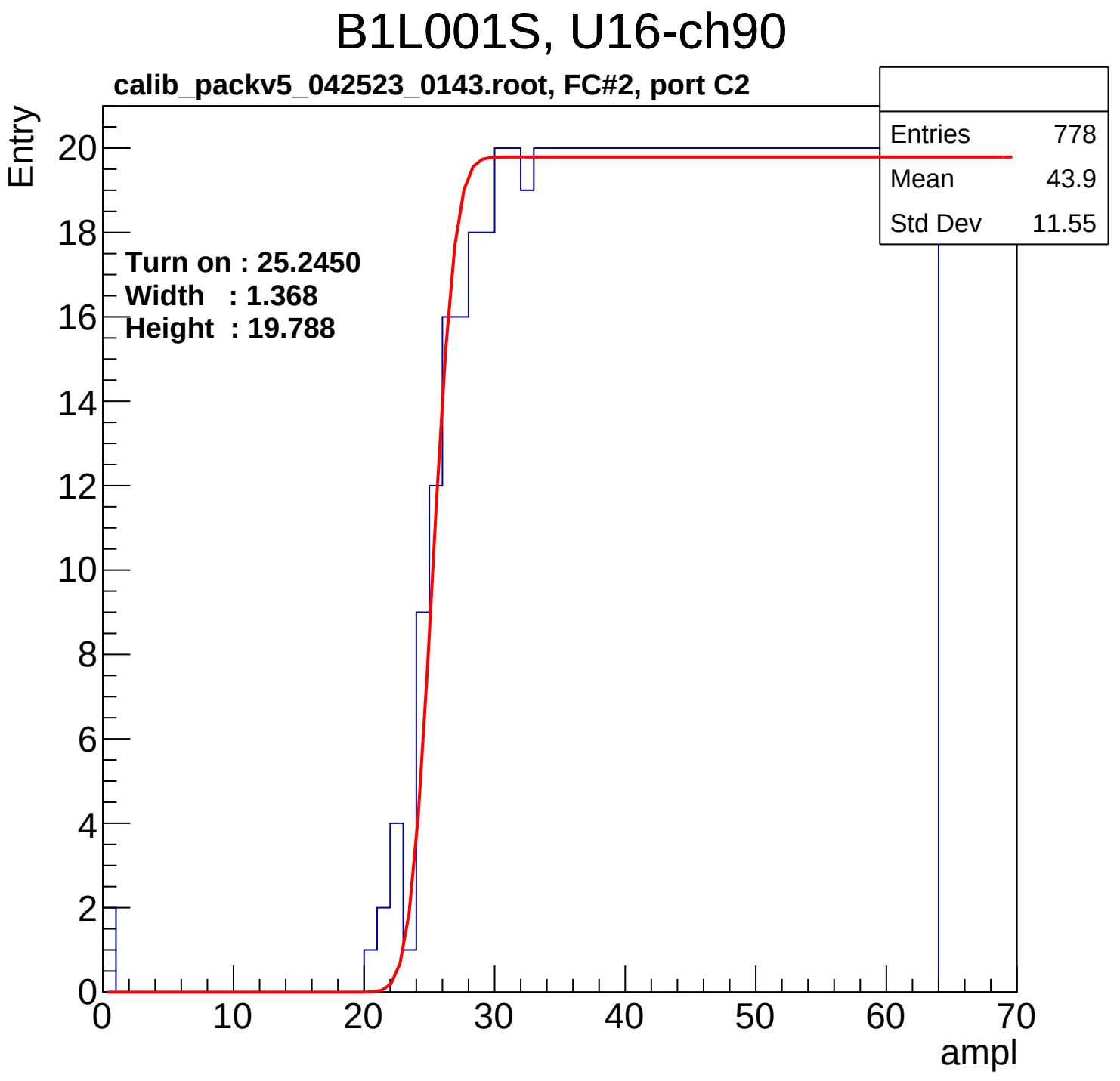
B1L001S, U16-ch90
calib_packv5_042523_0143.root, FC#2, port C2
Entries 778
Mean 43.9
Std Dev 11.55
Turn on : 25.2450
Width : 1.368
Height : 19.788
Entry
ampl
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6
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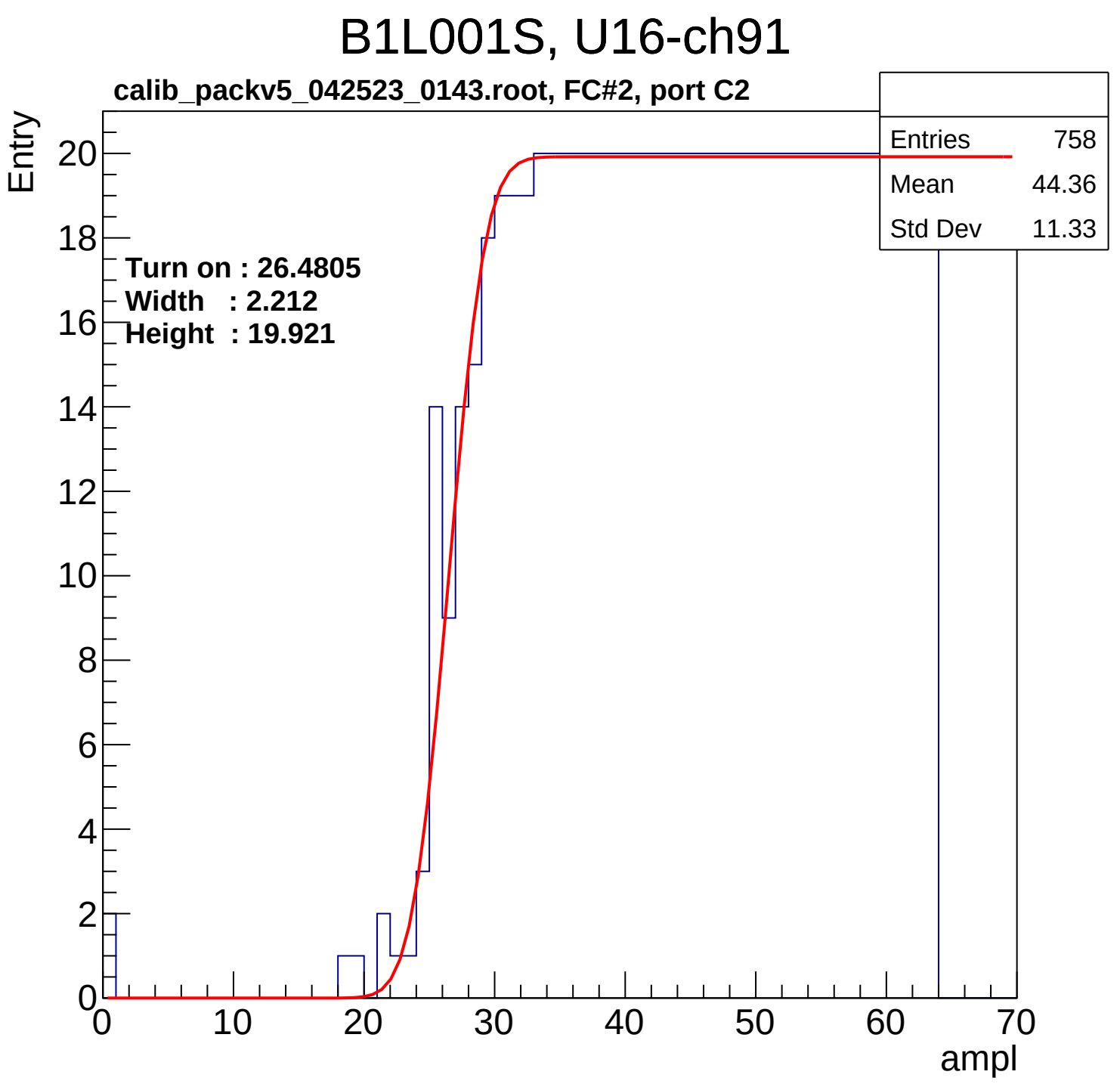
B1L001S, U16-ch91
calib_packv5_042523_0143.root, FC#2, port C2
Entries 758
Mean 44.36
Std Dev 11.33
Turn on : 26.4805
Width : 2.212
Height : 19.921
Entry
ampl
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6
8
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12
14
16
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0
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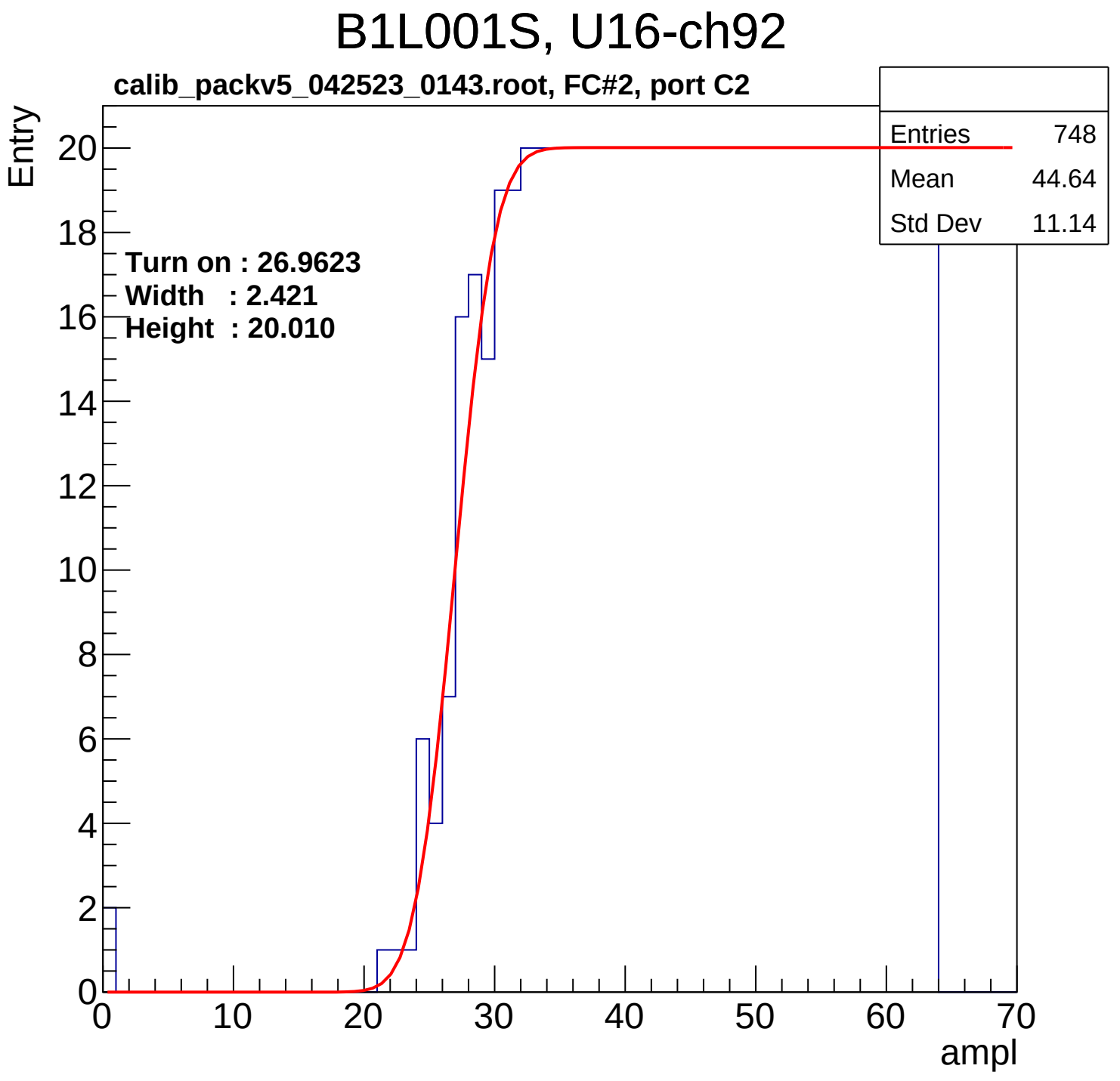
B1L001S, U16-ch92
calib_packv5_042523_0143.root, FC#2, port C2
Entries 748
Mean 44.64
Std Dev 11.14
Turn on : 26.9623
Width : 2.421
Height : 20.010
Entry
ampl
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6
8
10
12
14
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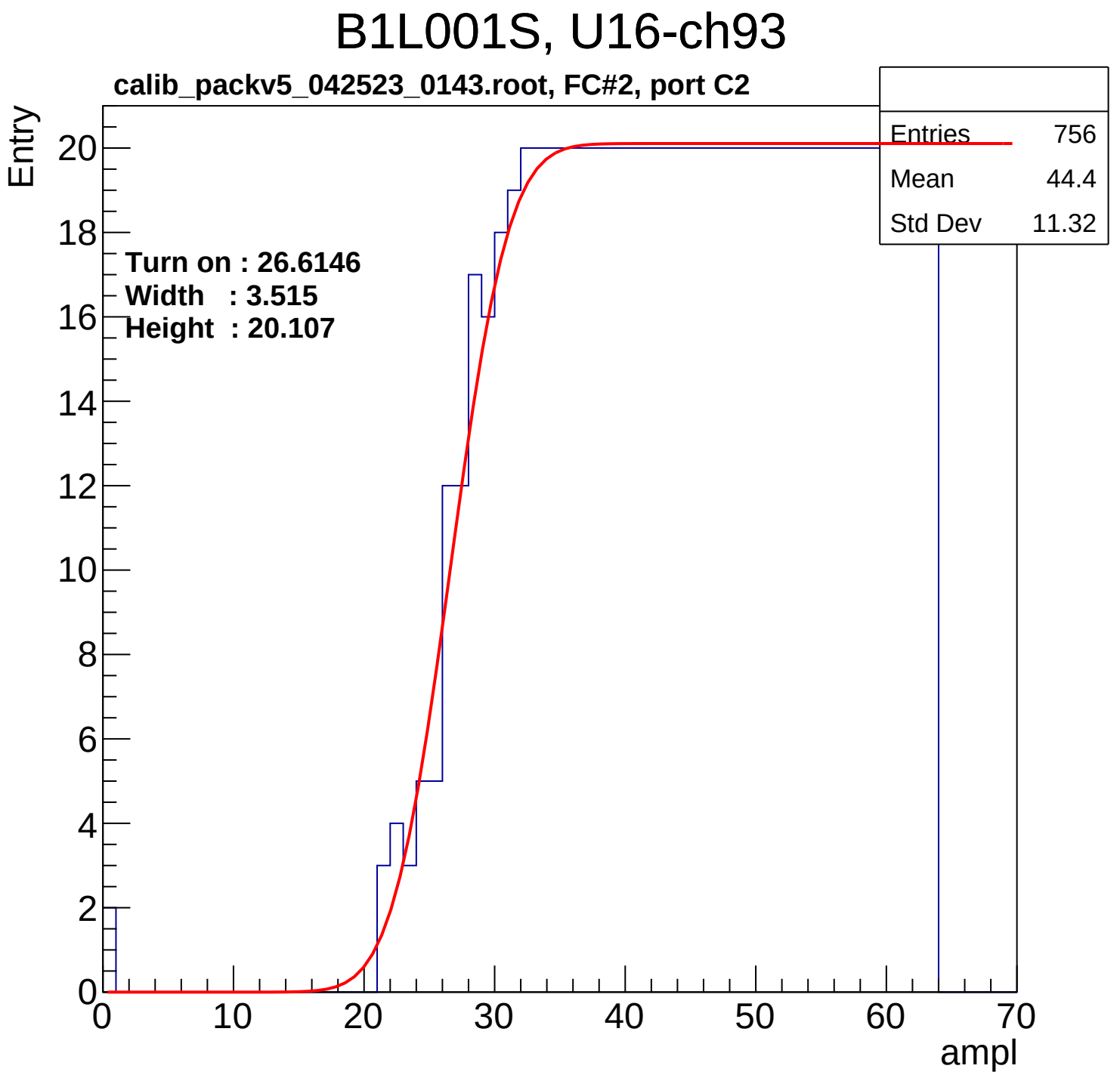
B1L001S, U16-ch93
calib_packv5_042523_0143.root, FC#2, port C2
Entries 756
Mean 44.4
Std Dev 11.32
Turn on : 26.6146
Width : 3.515
Height : 20.107
Entry
ampl
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8
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12
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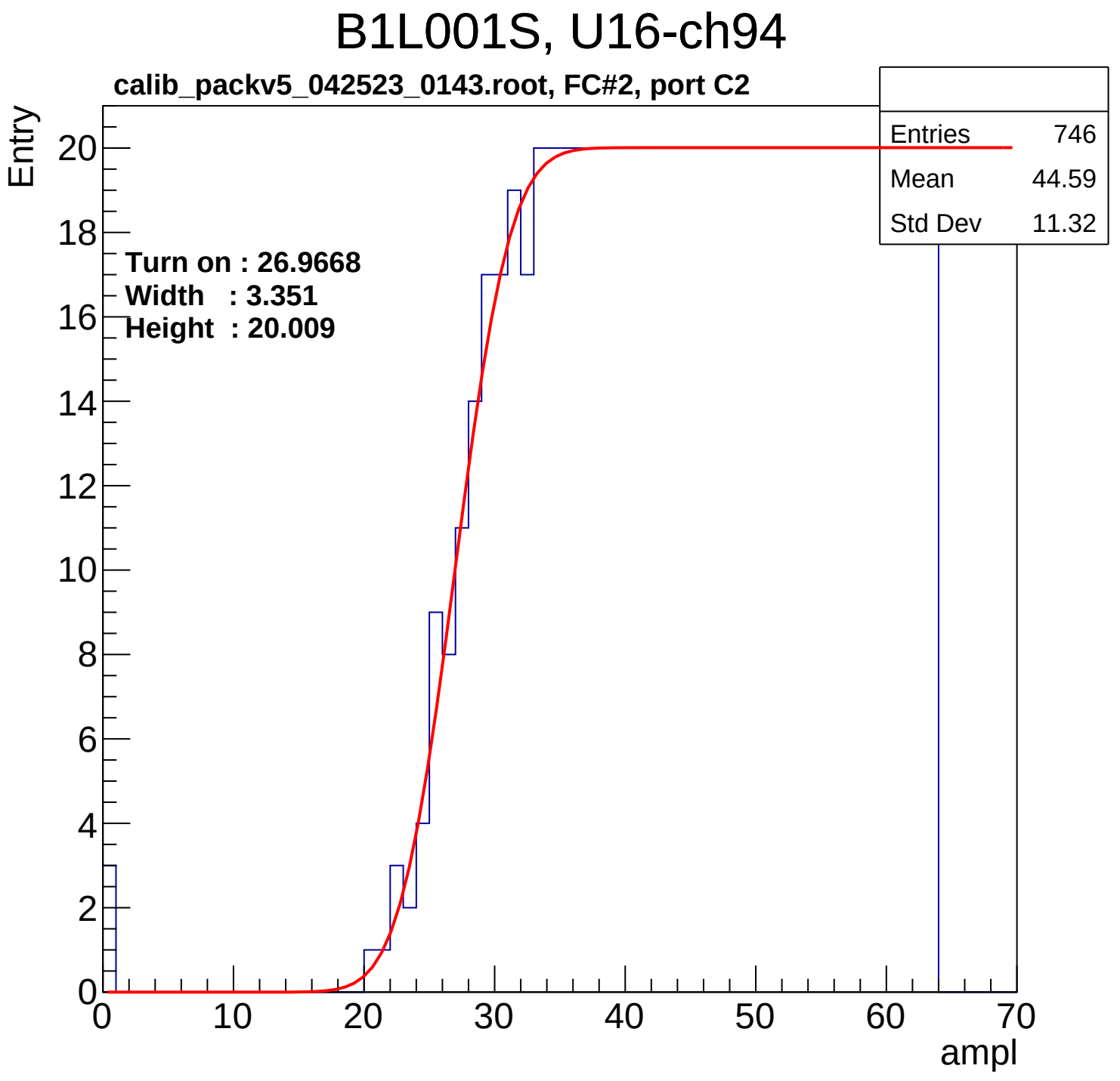
B1L001S, U16-ch94
calib_packv5_042523_0143.root, FC#2, port C2
Entries 746
Mean 44.59
Std Dev 11.32
Turn on : 26.9668
Width : 3.351
Height : 20.009
Entry
ampl
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6
8
10
12
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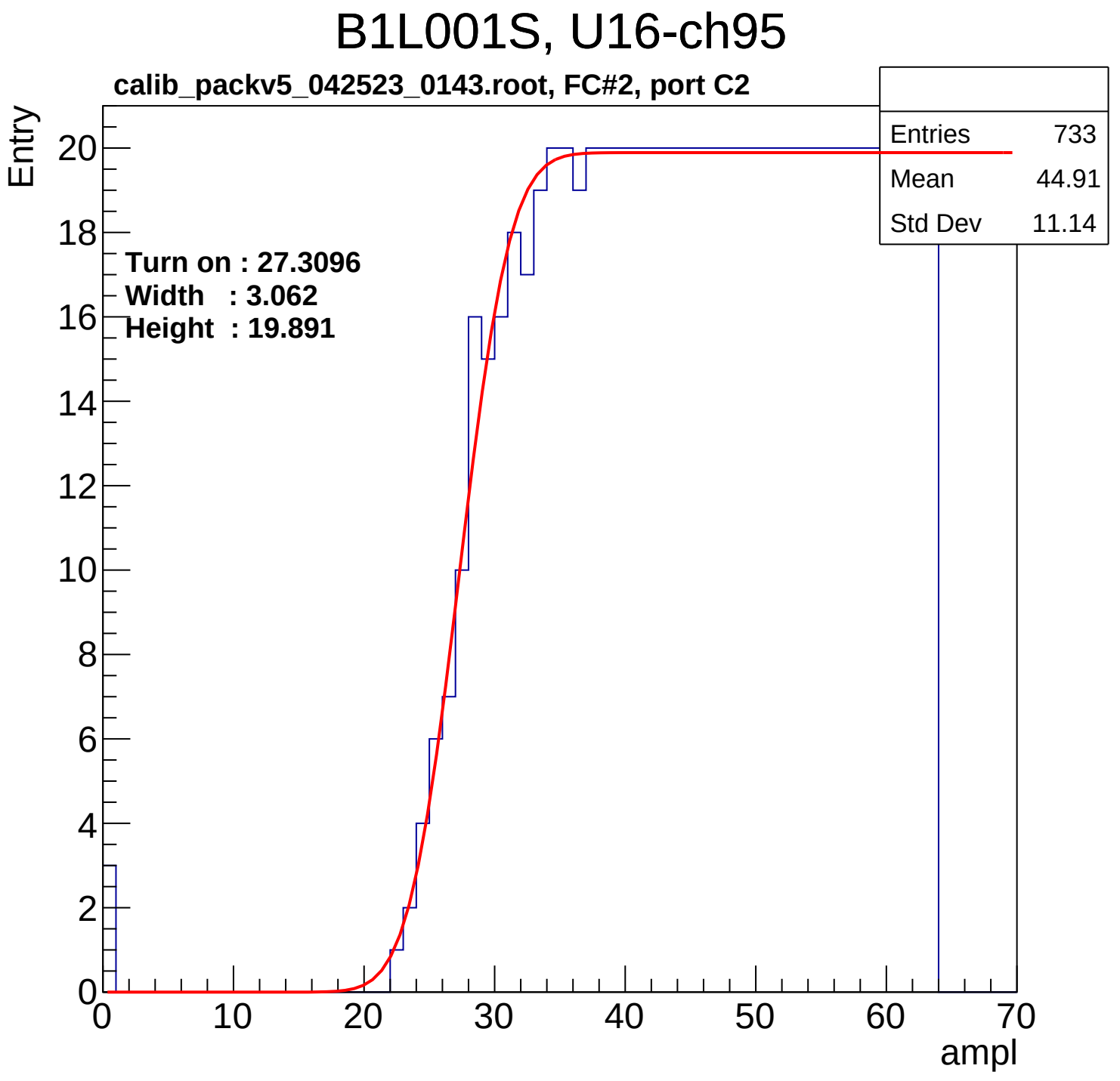
B1L001S, U16-ch95
calib_packv5_042523_0143.root, FC#2, port C2
Entries 733
Mean 44.91
Std Dev 11.14
Turn on : 27.3096
Width : 3.062
Height : 19.891
Entry
ampl
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6
8
10
12
14
16
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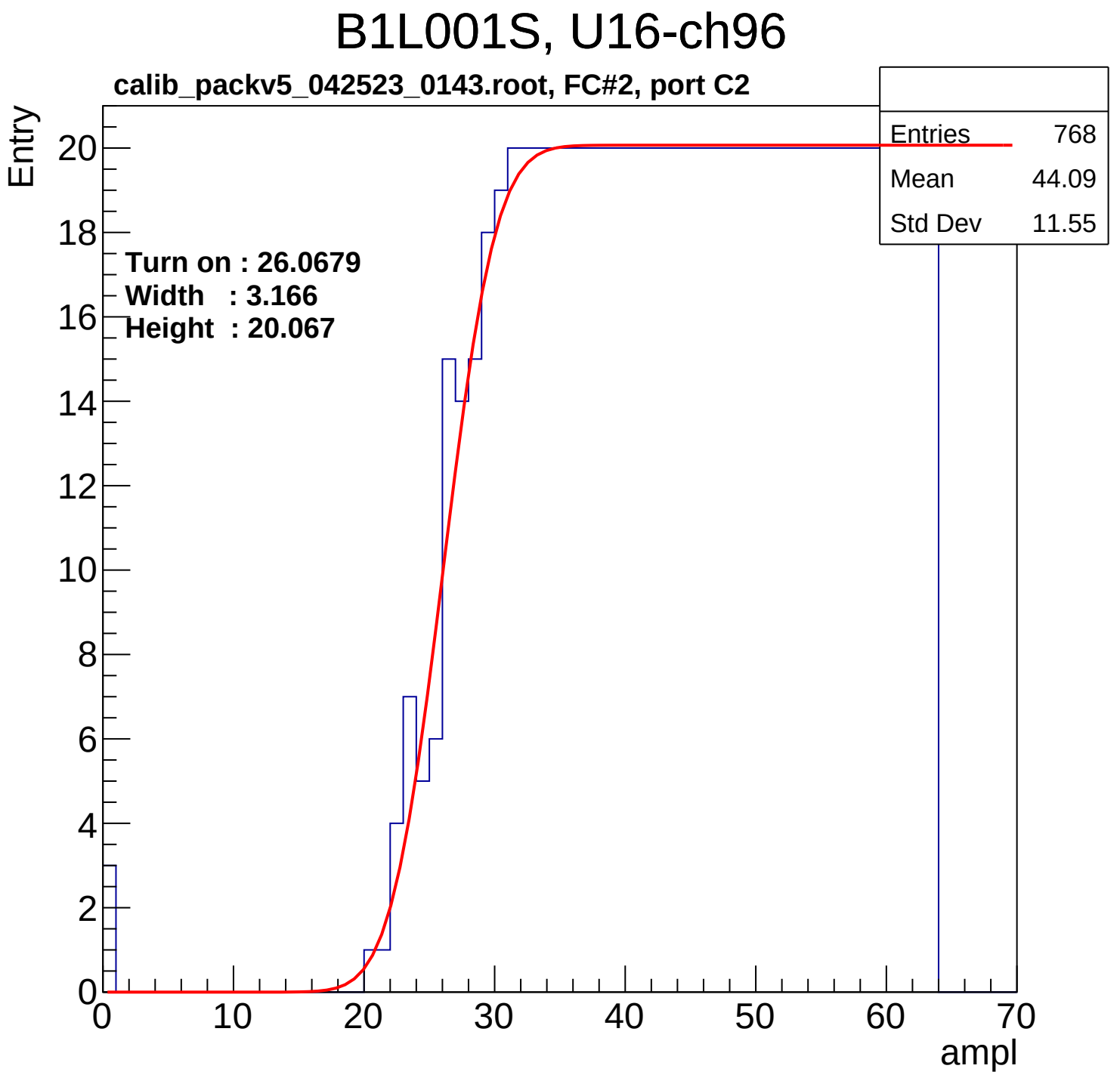
B1L001S, U16-ch96
calib_packv5_042523_0143.root, FC#2, port C2
Entries 768
Mean 44.09
Std Dev 11.55
Turn on : 26.0679
Width : 3.166
Height : 20.067
Entry
ampl
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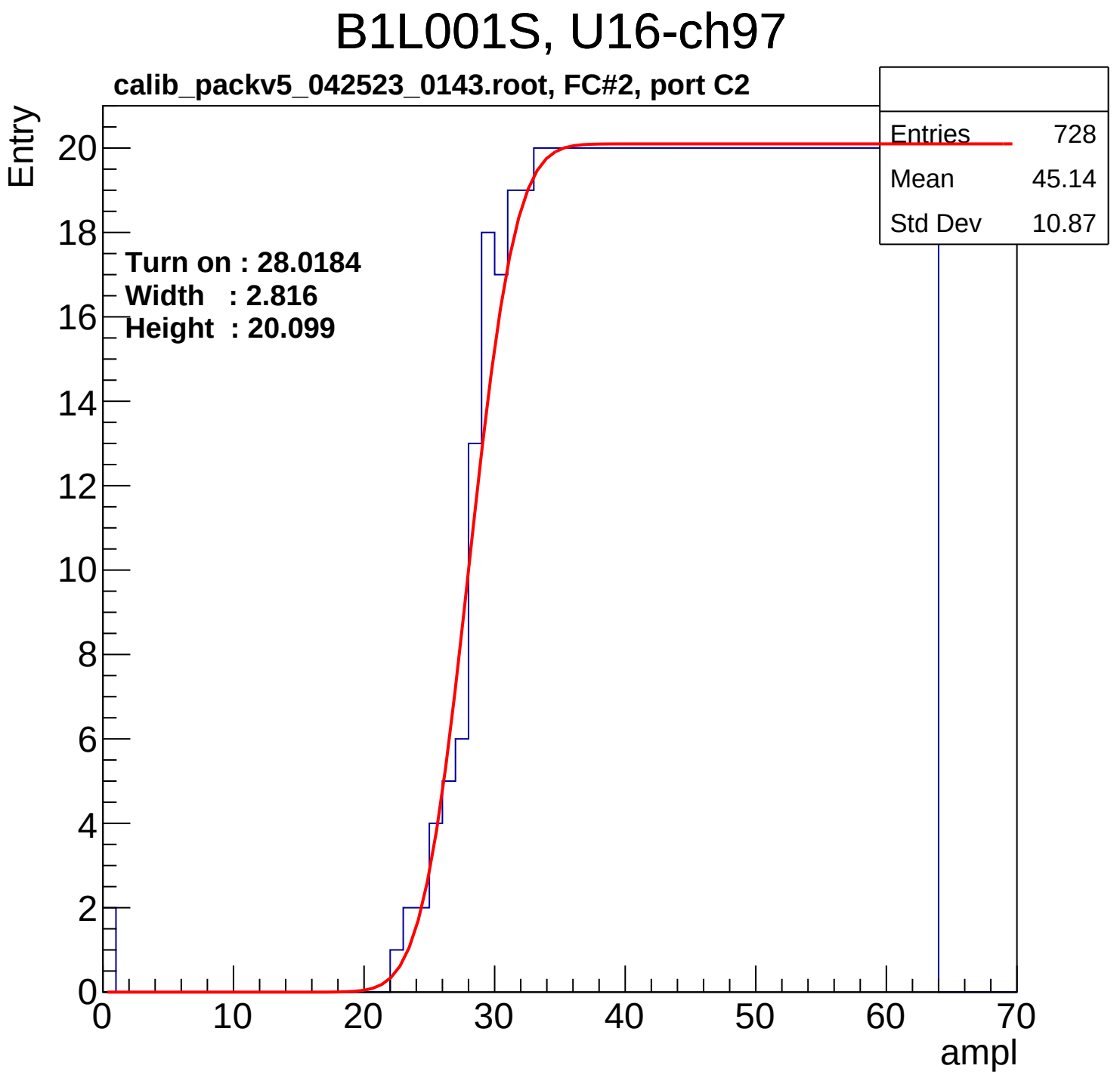
B1L001S, U16-ch97
calib_packv5_042523_0143.root, FC#2, port C2
Entries 728
Mean 45.14
Std Dev 10.87
Turn on : 28.0184
Width : 2.816
Height : 20.099
Entry
ampl
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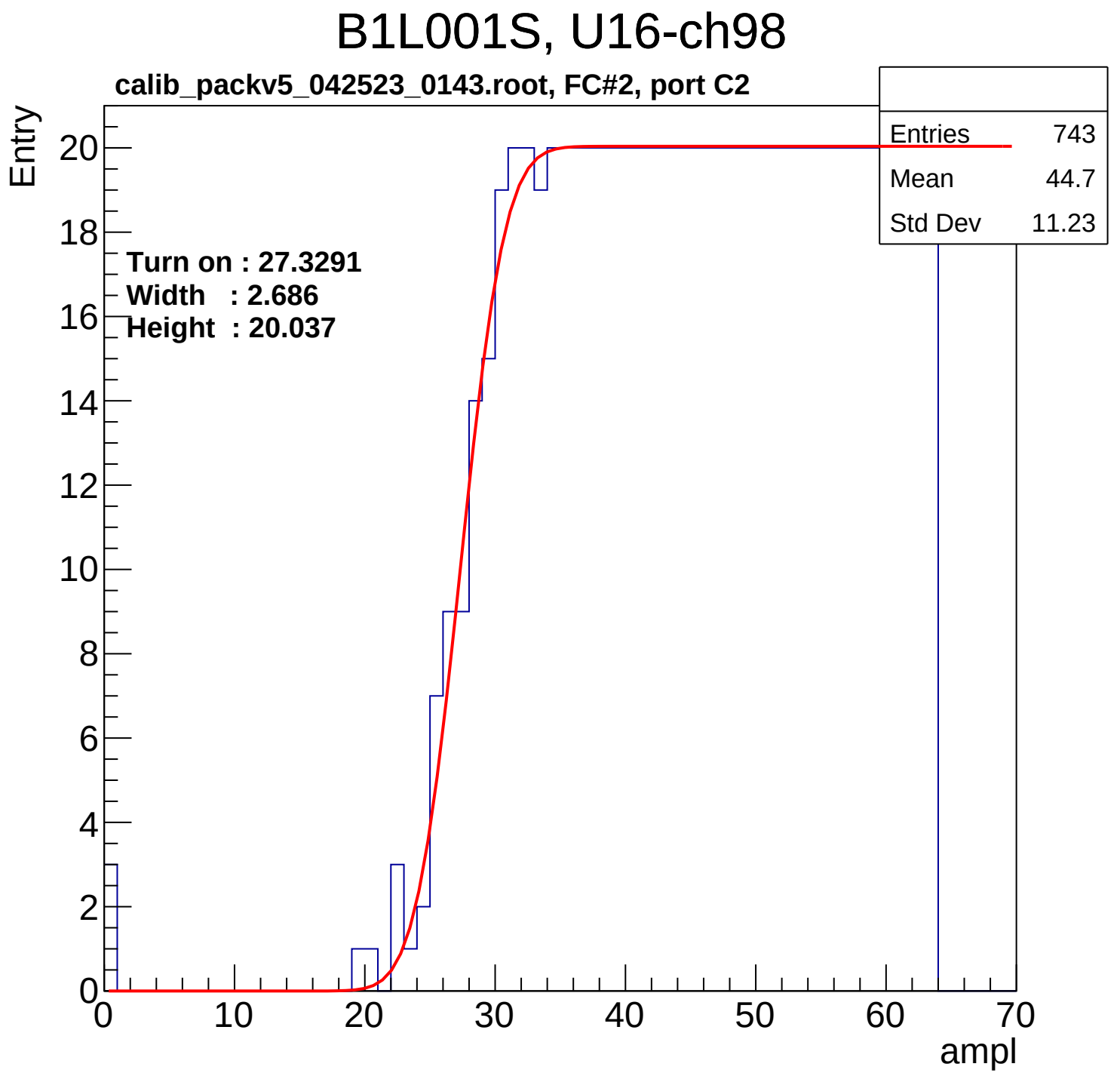
B1L001S, U16-ch98
calib_packv5_042523_0143.root, FC#2, port C2
Entries 743
Mean 44.7
Std Dev 11.23
Turn on : 27.3291
Width : 2.686
Height : 20.037
Entry
ampl
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10
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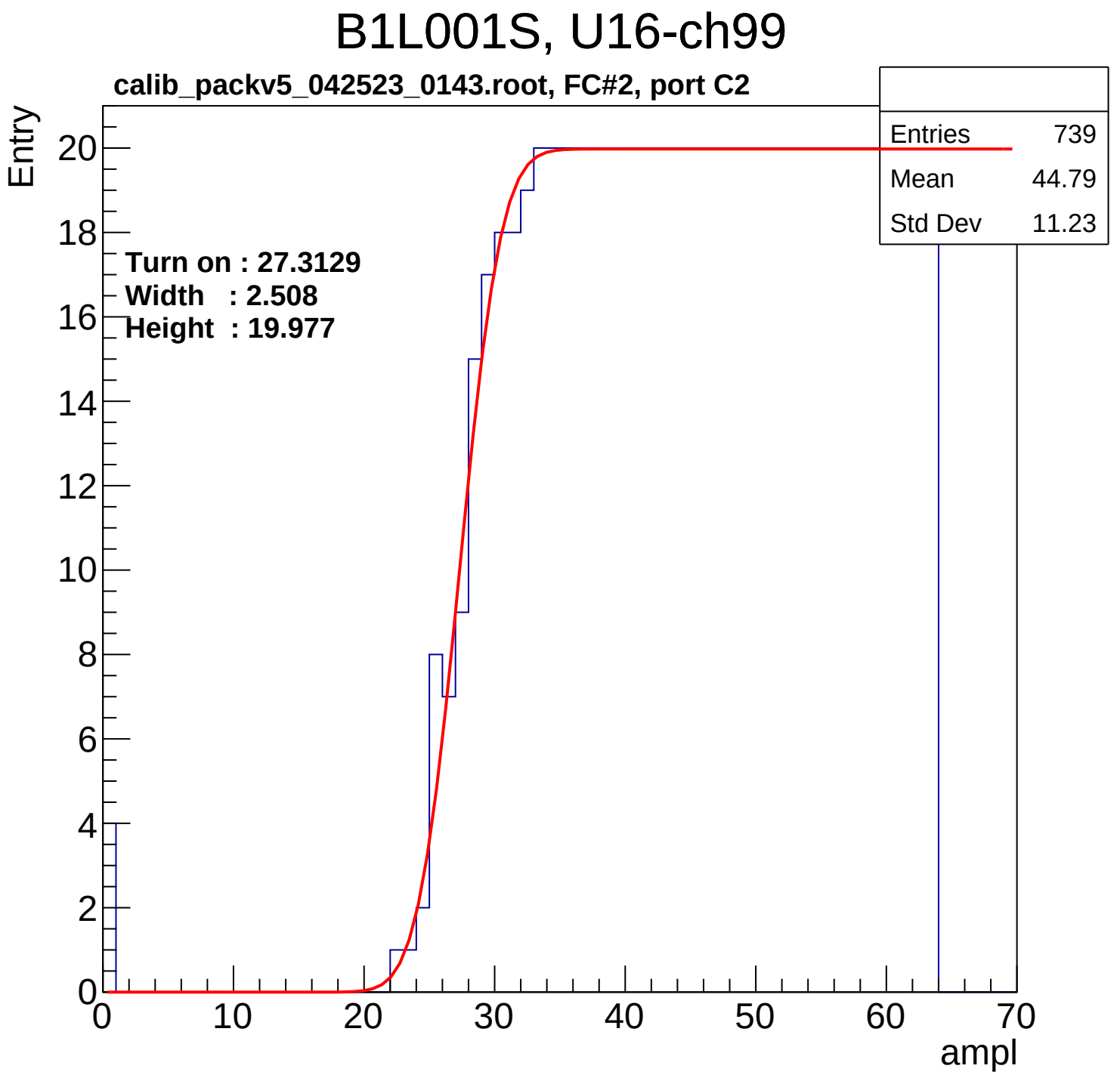
B1L001S, U16-ch99
calib_packv5_042523_0143.root, FC#2, port C2
Entries 739
Mean 44.79
Std Dev 11.23
Turn on : 27.3129
Width : 2.508
Height : 19.977
Entry
ampl
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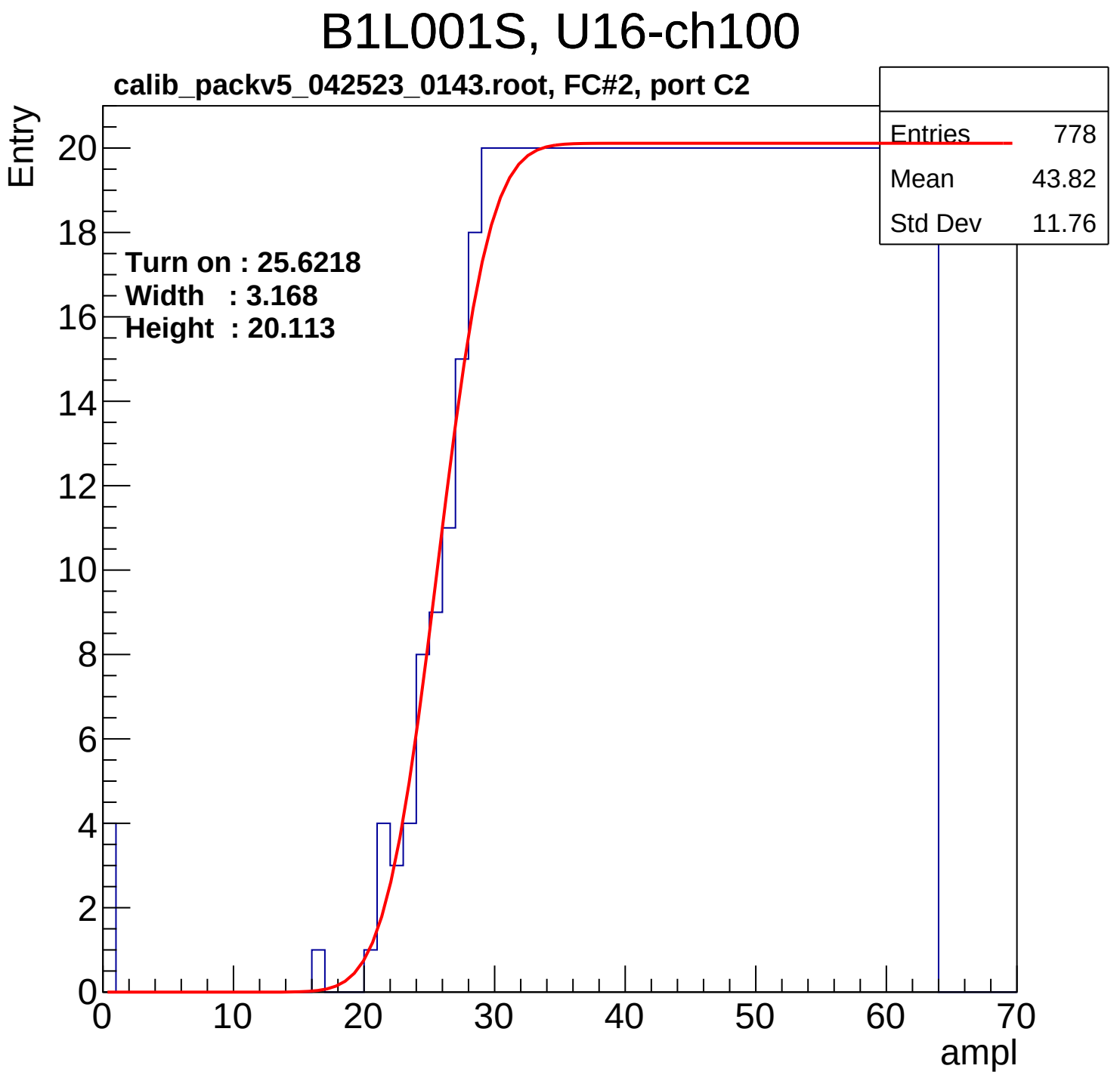
B1L001S, U16-ch100
calib_packv5_042523_0143.root, FC#2, port C2
Entries 778
Mean 43.82
Std Dev 11.76
Turn on : 25.6218
Width : 3.168
Height : 20.113
Entry
ampl
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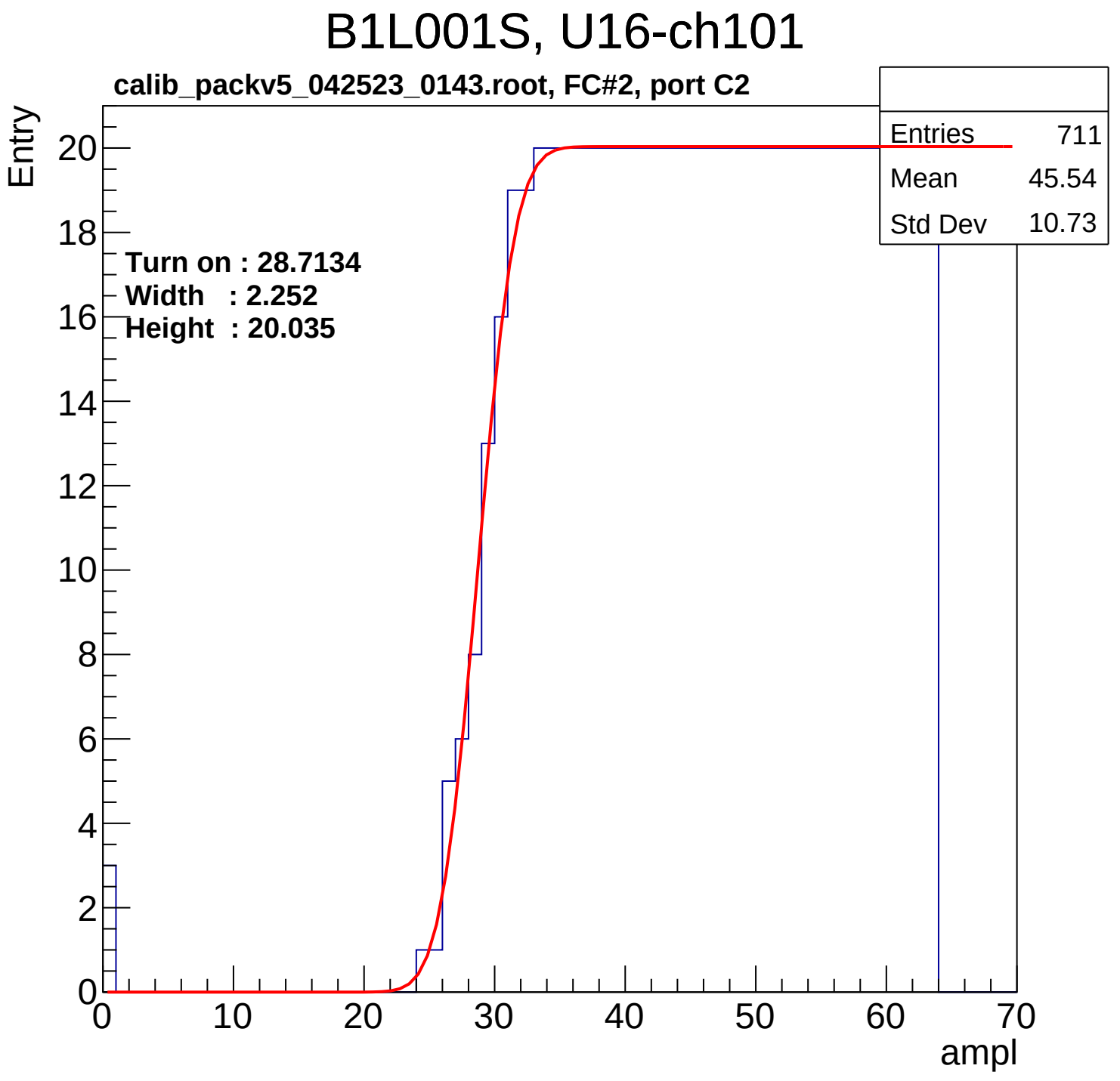
B1L001S, U16-ch101
calib_packv5_042523_0143.root, FC#2, port C2
Entries 711
Mean 45.54
Std Dev 10.73
Turn on : 28.7134
Width : 2.252
Height : 20.035
Entry
ampl
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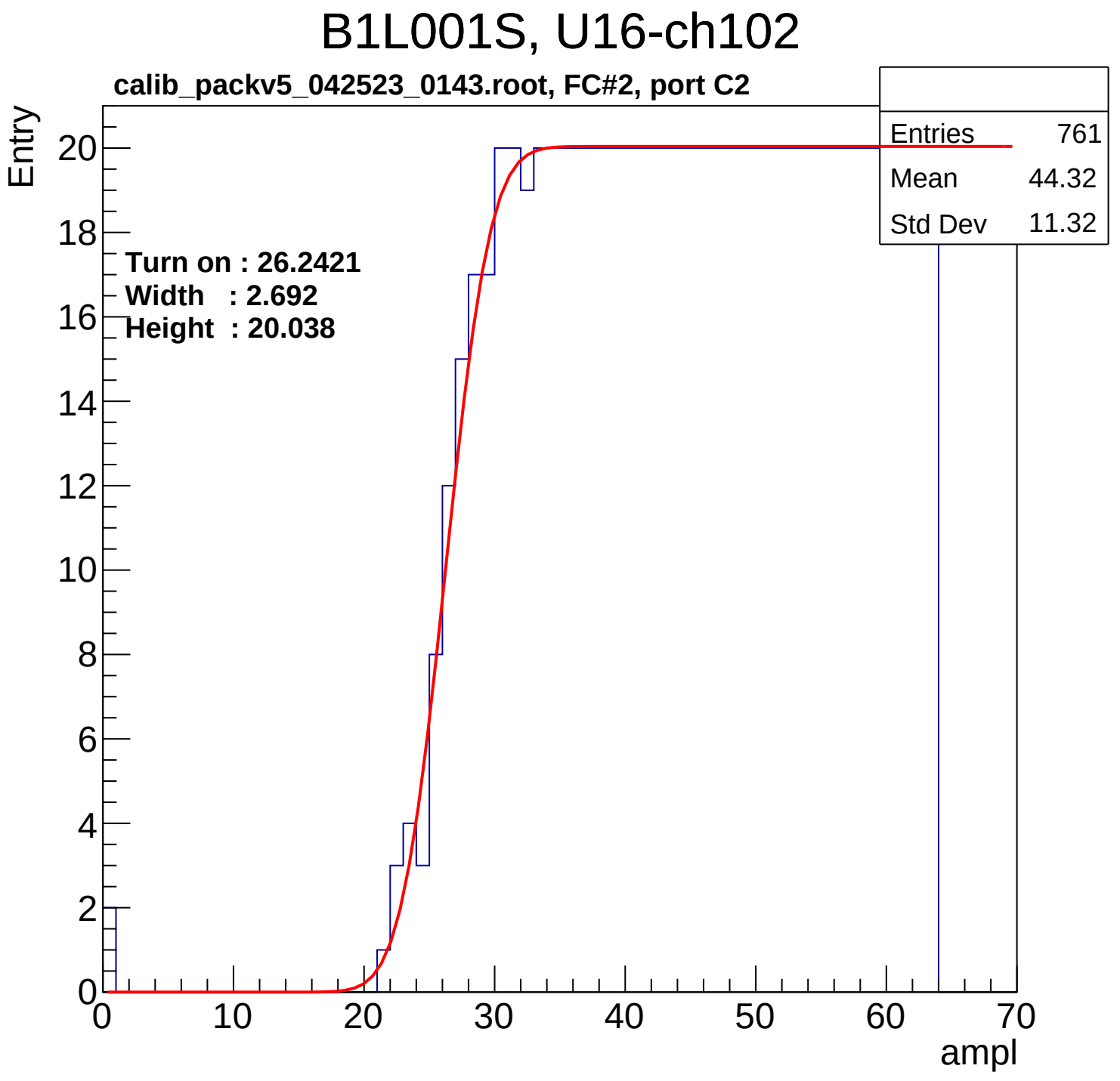
B1L001S, U16-ch102
calib_packv5_042523_0143.root, FC#2, port C2
Entries 761
Mean 44.32
Std Dev 11.32
Turn on : 26.2421
Width : 2.692
Height : 20.038
Entry
ampl
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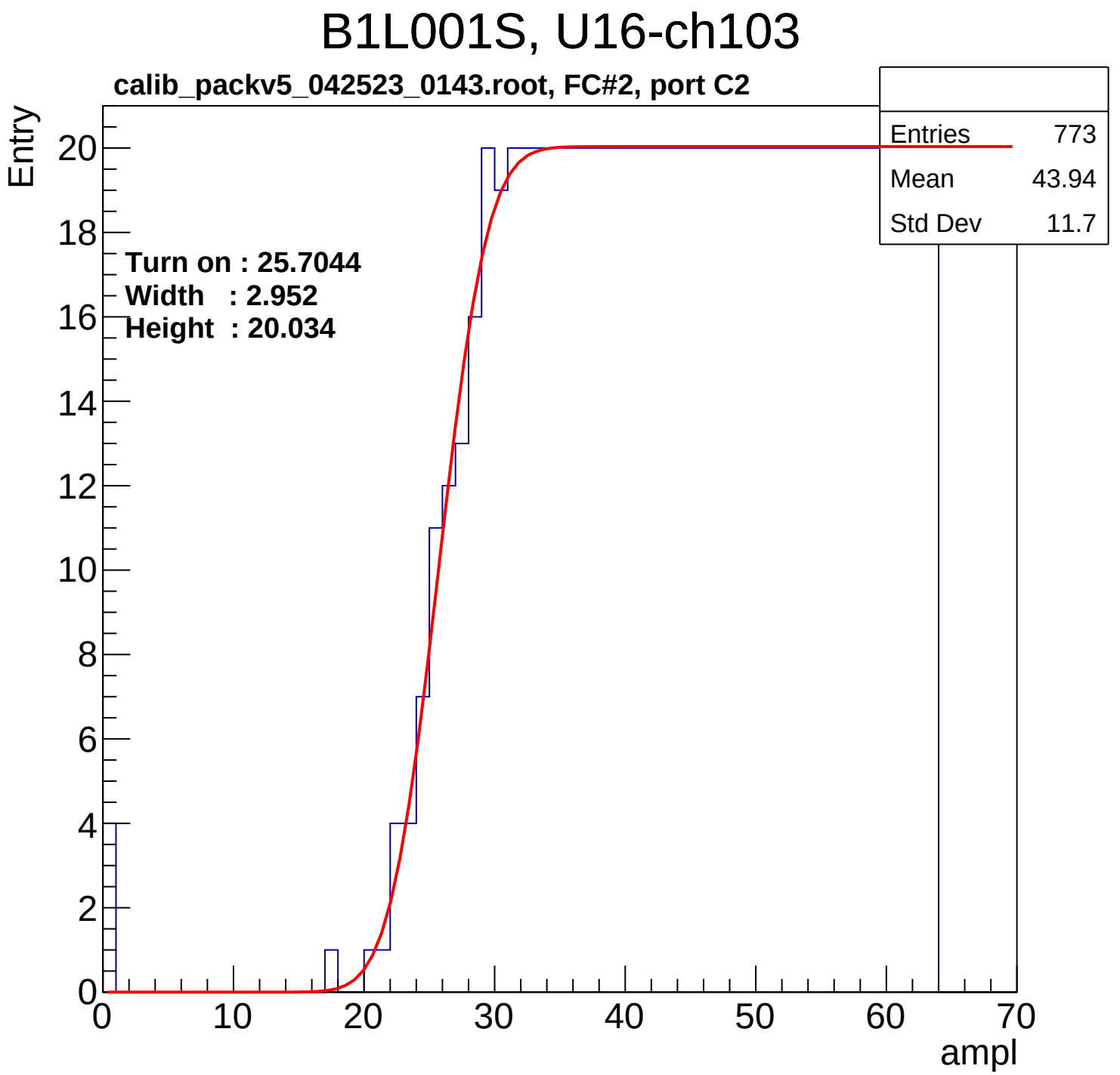
B1L001S, U16-ch103
calib_packv5_042523_0143.root, FC#2, port C2
Entries 773
Mean 43.94
Std Dev 11.7
Turn on : 25.7044
Width : 2.952
Height : 20.034
Entry
ampl
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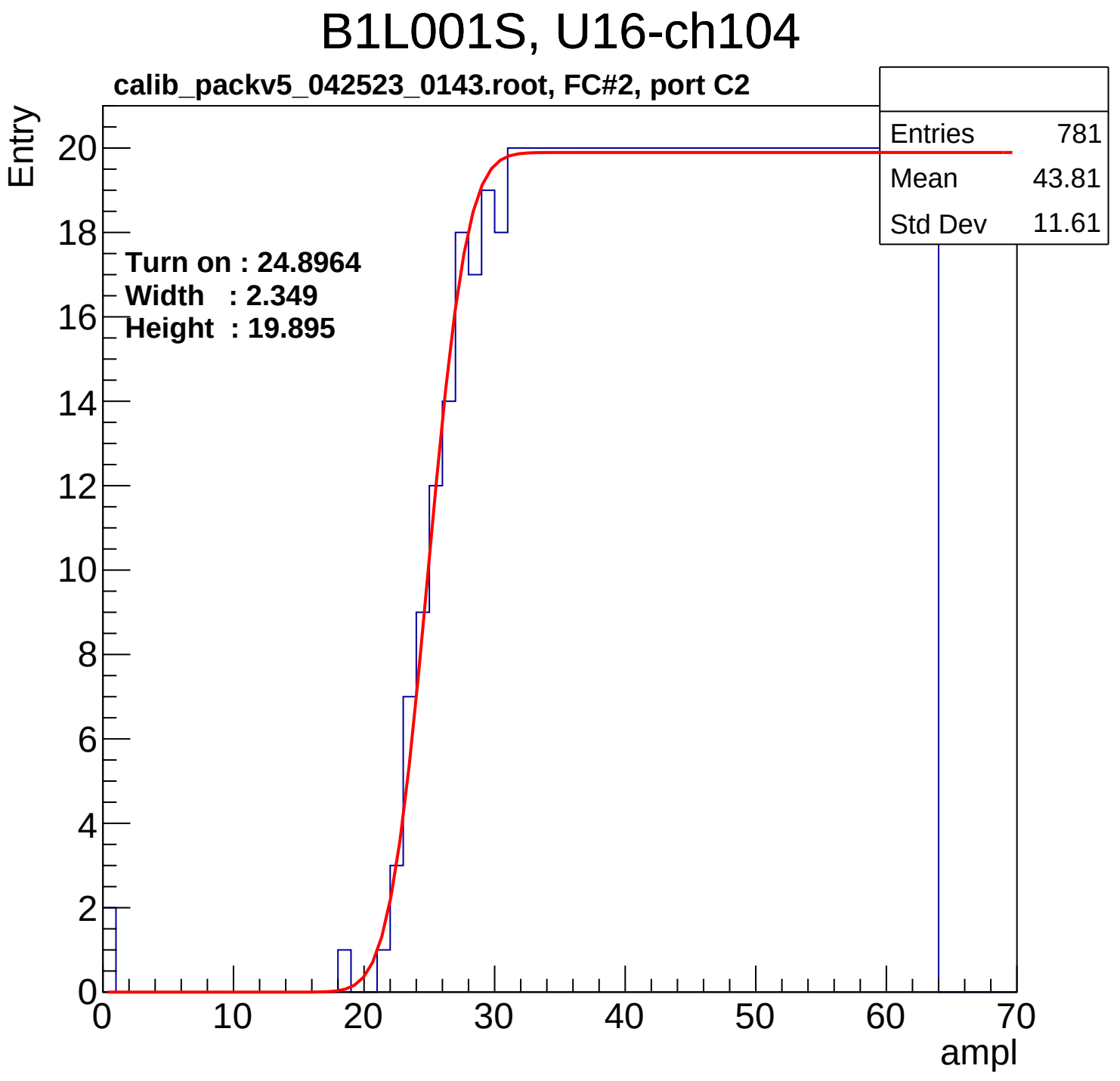
B1L001S, U16-ch104
calib_packv5_042523_0143.root, FC#2, port C2
Entries 781
Mean 43.81
Std Dev 11.61
Turn on : 24.8964
Width : 2.349
Height : 19.895
Entry
ampl
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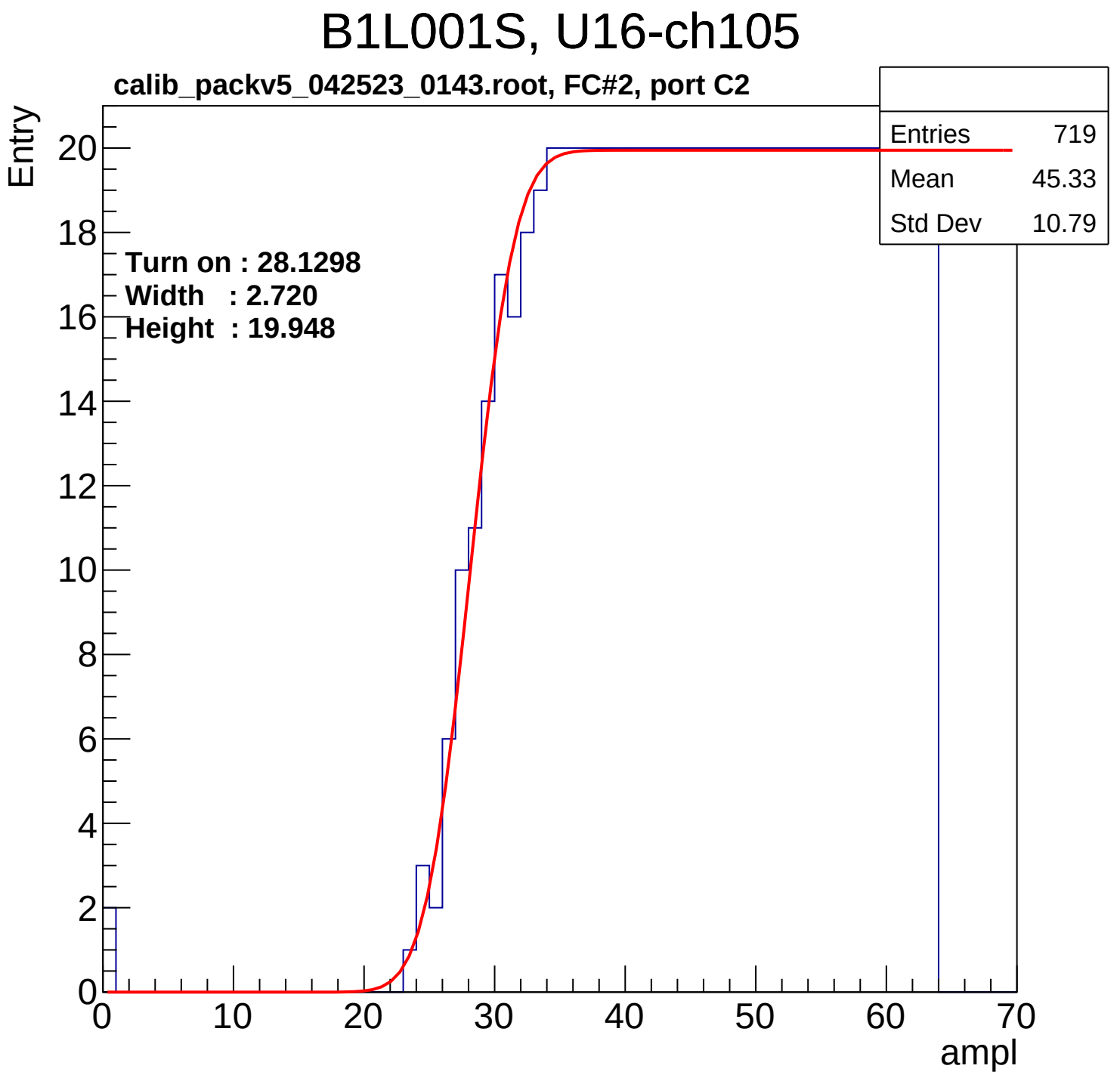
B1L001S, U16-ch105
calib_packv5_042523_0143.root, FC#2, port C2
Entries 719
Mean 45.33
Std Dev 10.79
Turn on : 28.1298
Width : 2.720
Height : 19.948
Entry
ampl
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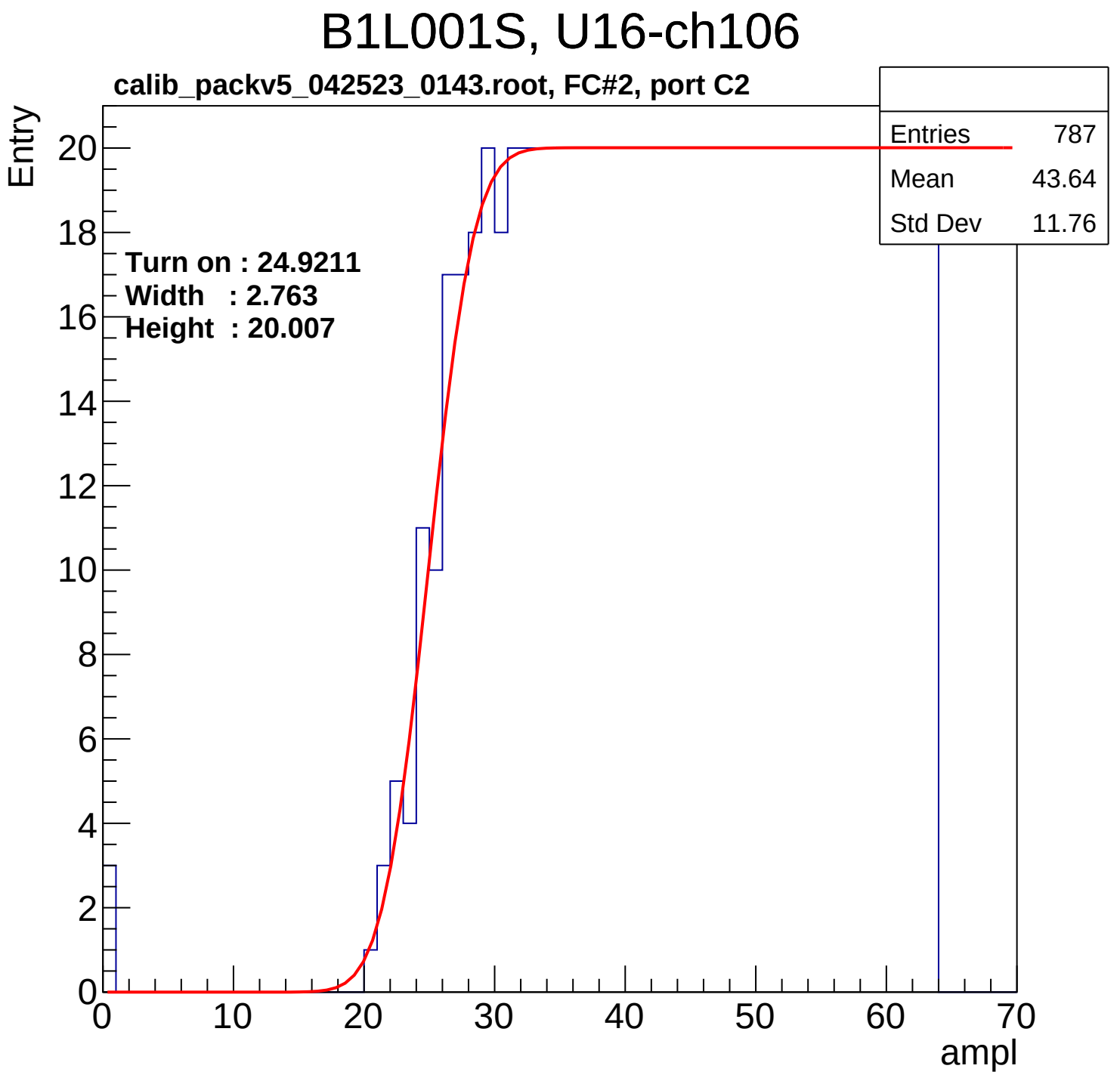
B1L001S, U16-ch106
calib_packv5_042523_0143.root, FC#2, port C2
Entries 787
Mean 43.64
Std Dev 11.76
Turn on : 24.9211
Width : 2.763
Height : 20.007
Entry
ampl
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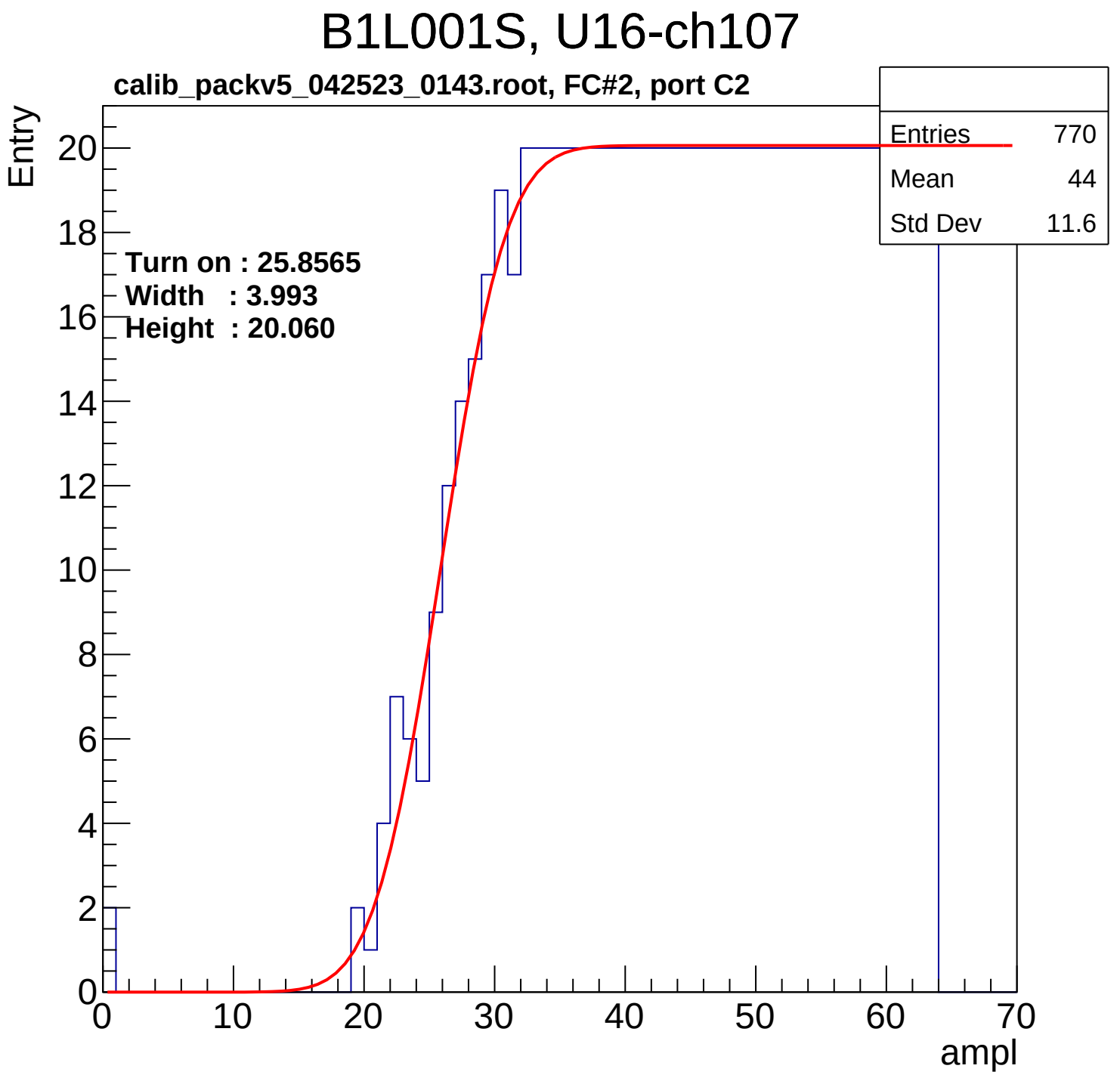
B1L001S, U16-ch107
calib_packv5_042523_0143.root, FC#2, port C2
Entries 770
Mean 44
Std Dev 11.6
Turn on : 25.8565
Width : 3.993
Height : 20.060
Entry
ampl
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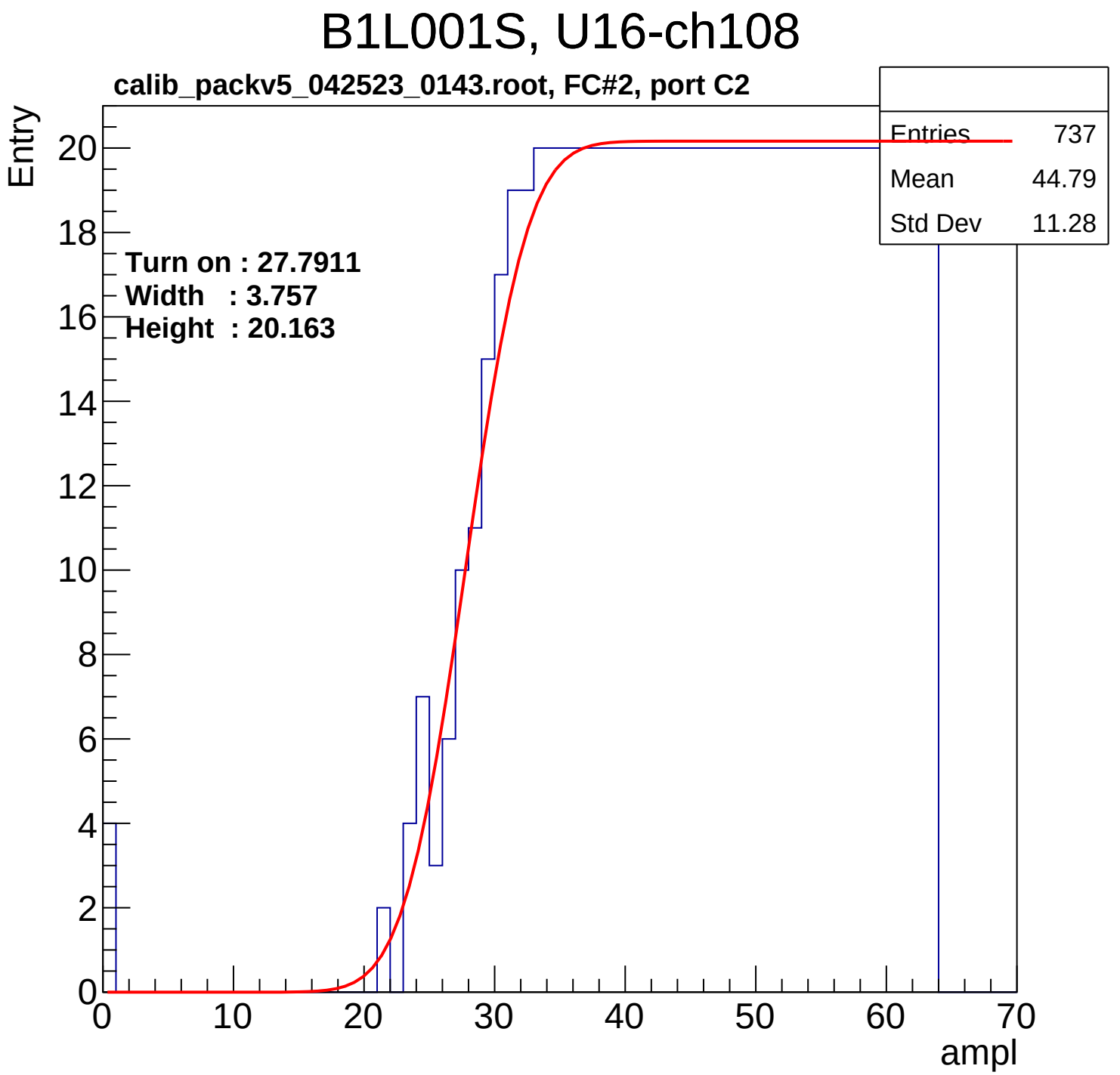
B1L001S, U16-ch108
calib_packv5_042523_0143.root, FC#2, port C2
Entries 737
Mean 44.79
Std Dev 11.28
Turn on : 27.7911
Width : 3.757
Height : 20.163
Entry
ampl
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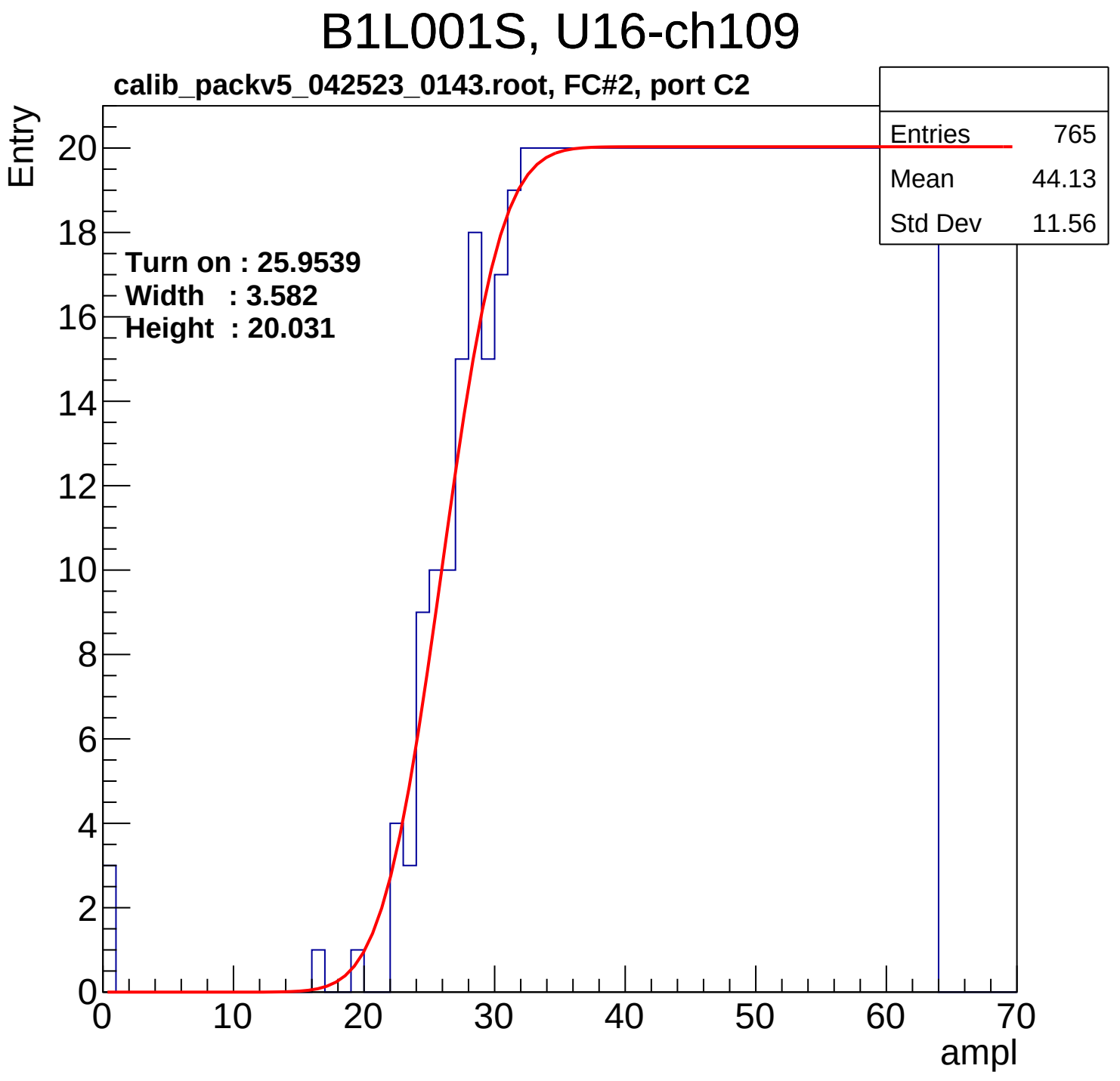
B1L001S, U16-ch109
calib_packv5_042523_0143.root, FC#2, port C2
Entries 765
Mean 44.13
Std Dev 11.56
Turn on : 25.9539
Width : 3.582
Height : 20.031
Entry
ampl
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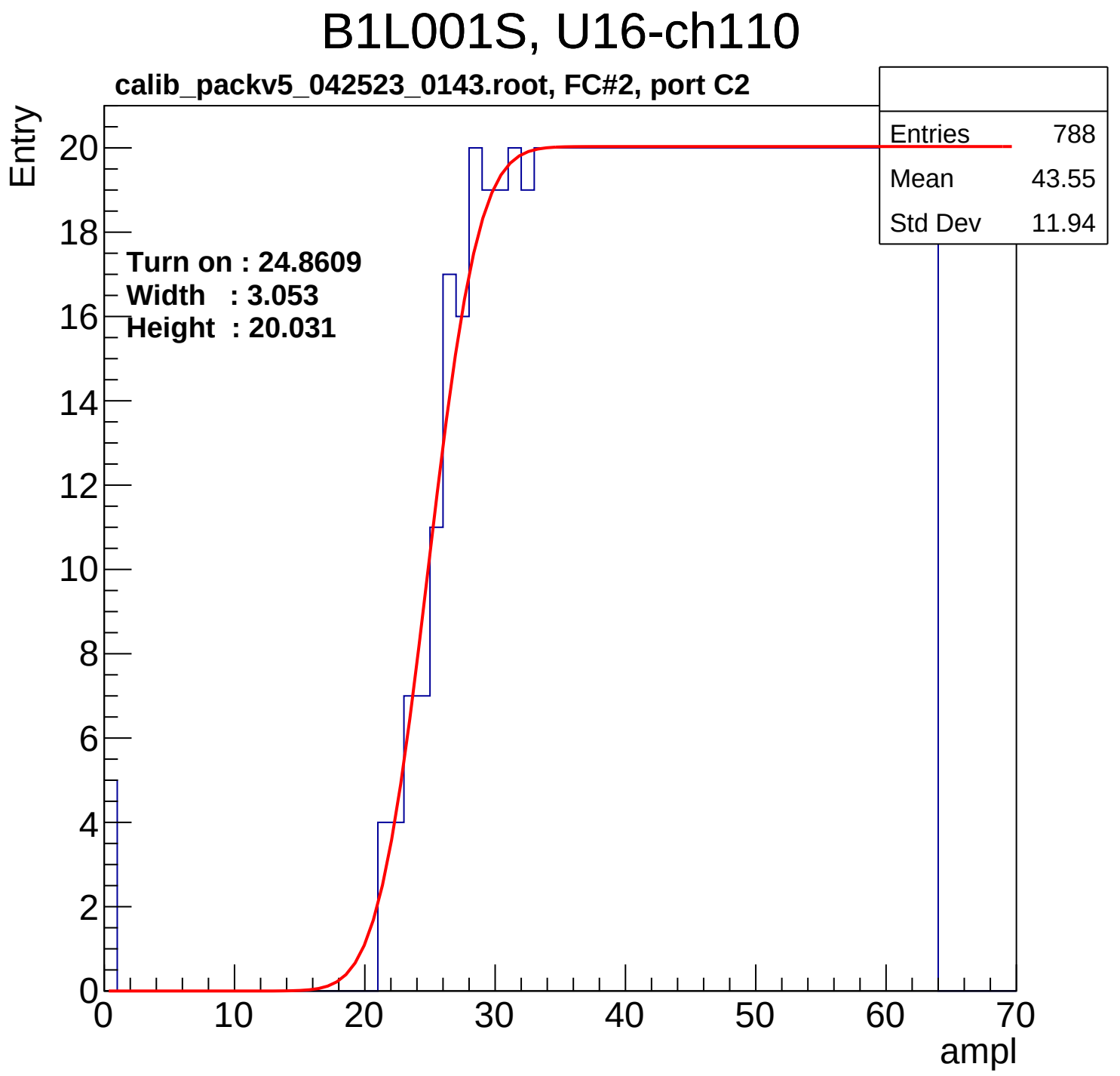
B1L001S, U16-ch110
calib_packv5_042523_0143.root, FC#2, port C2
Entries 788
Mean 43.55
Std Dev 11.94
Turn on : 24.8609
Width : 3.053
Height : 20.031
Entry
ampl
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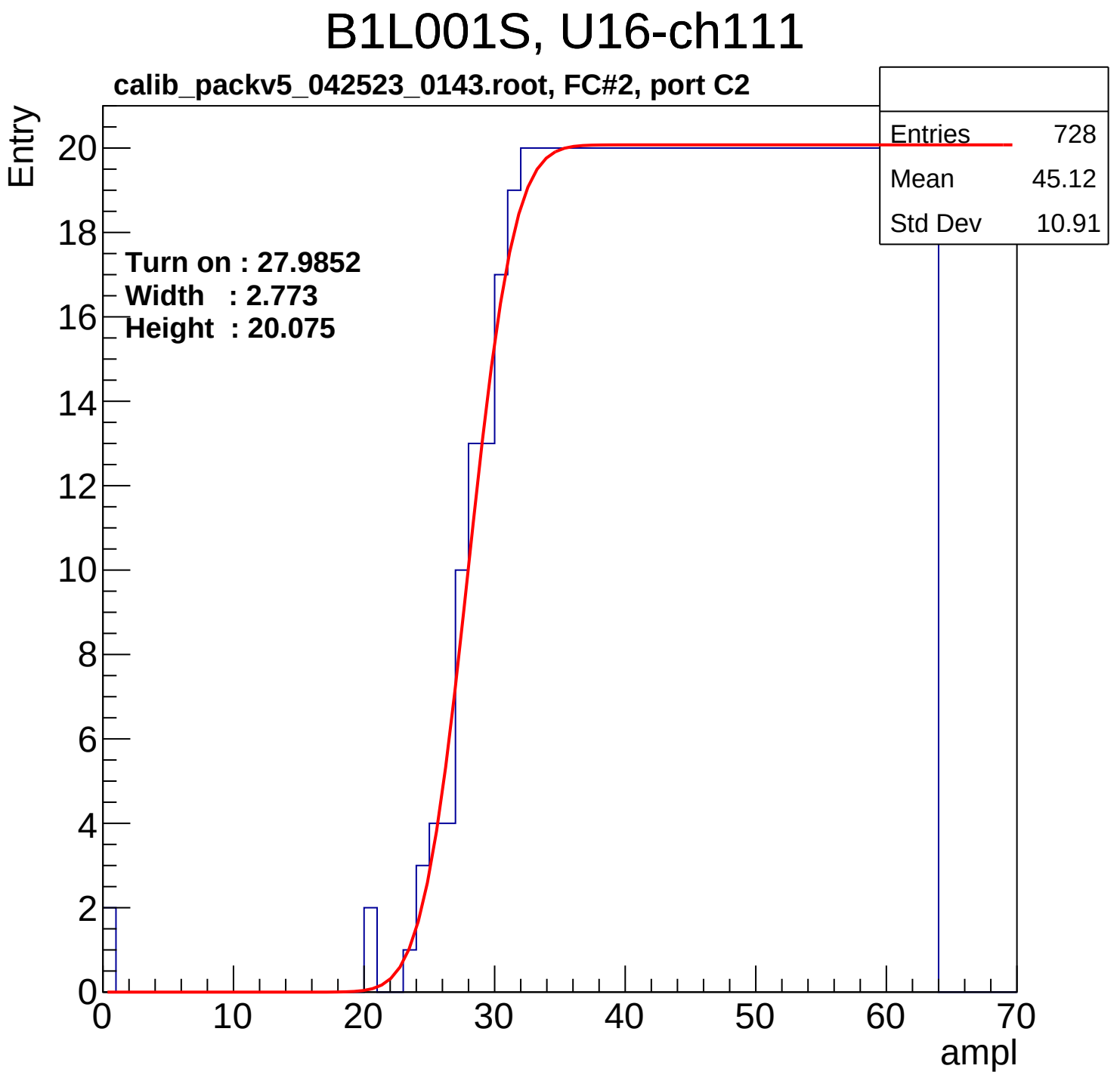
B1L001S, U16-ch111
calib_packv5_042523_0143.root, FC#2, port C2
Entries 728
Mean 45.12
Std Dev 10.91
Turn on : 27.9852
Width : 2.773
Height : 20.075
Entry
ampl
0
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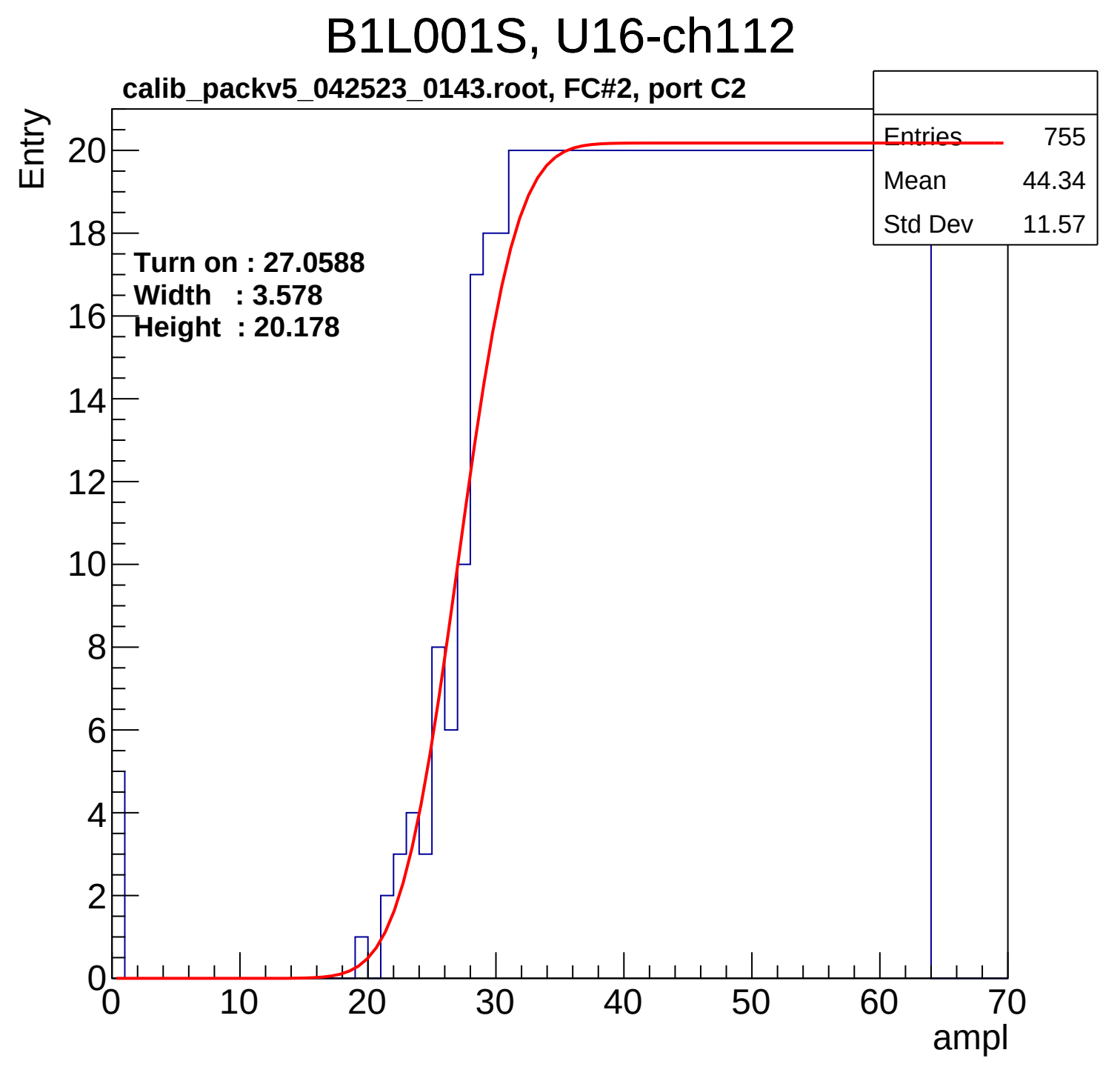
B1L001S, U16-ch112
calib_packv5_042523_0143.root, FC#2, port C2
Entries 755
Mean 44.34
Std Dev 11.57
Turn on : 27.0588
Width : 3.578
Height : 20.178
Entry
ampl
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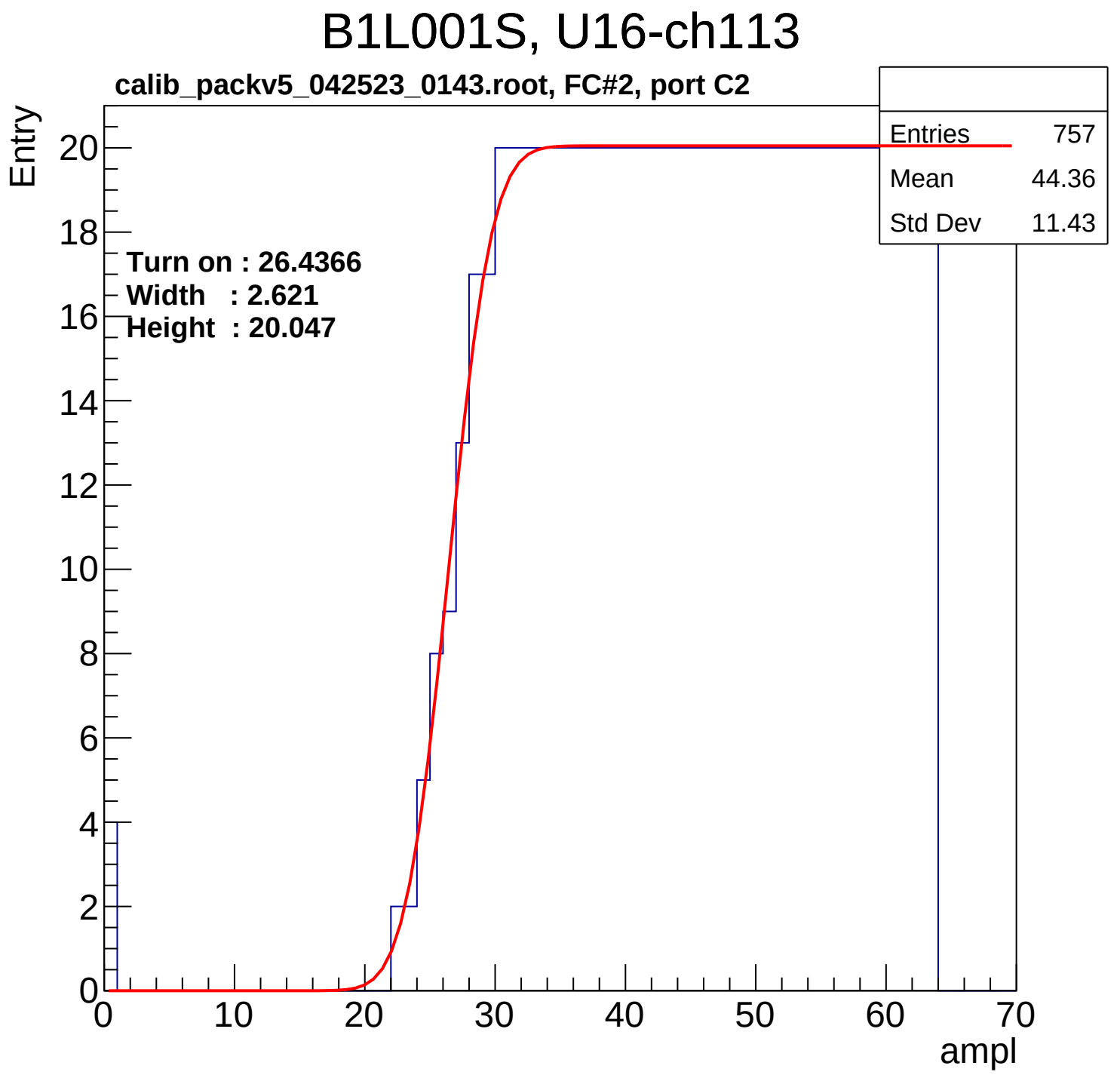
B1L001S, U16-ch113
calib_packv5_042523_0143.root, FC#2, port C2
Entries 757
Mean 44.36
Std Dev 11.43
Turn on : 26.4366
Width : 2.621
Height : 20.047
Entry
ampl
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6
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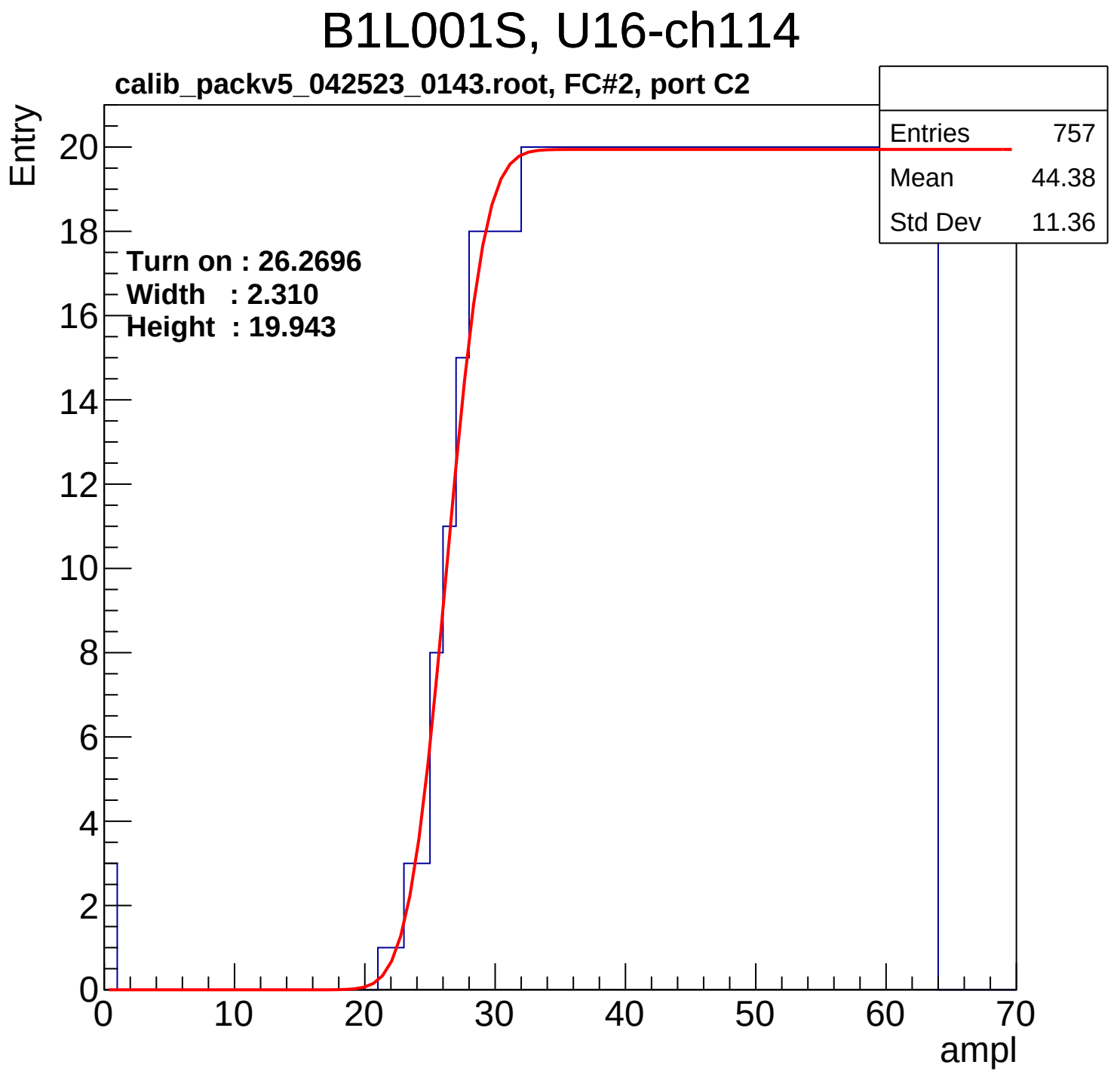
B1L001S, U16-ch114
calib_packv5_042523_0143.root, FC#2, port C2
Entries 757
Mean 44.38
Std Dev 11.36
Turn on : 26.2696
Width : 2.310
Height : 19.943
Entry
ampl
0
2
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6
8
10
12
14
16
18
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0
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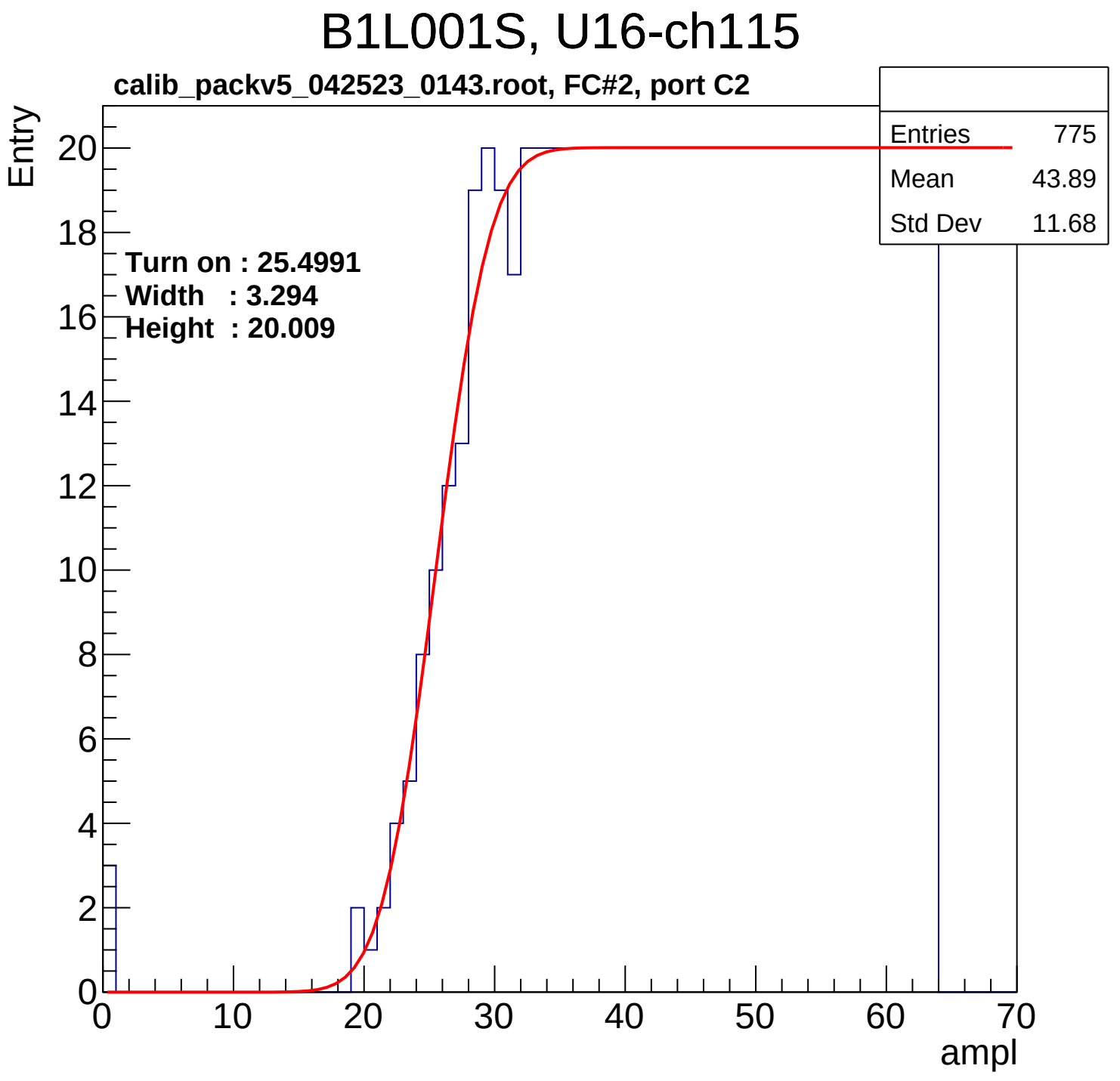
B1L001S, U16-ch115
calib_packv5_042523_0143.root, FC#2, port C2
Entries 775
Mean 43.89
Std Dev 11.68
Turn on : 25.4991
Width : 3.294
Height : 20.009
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
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20
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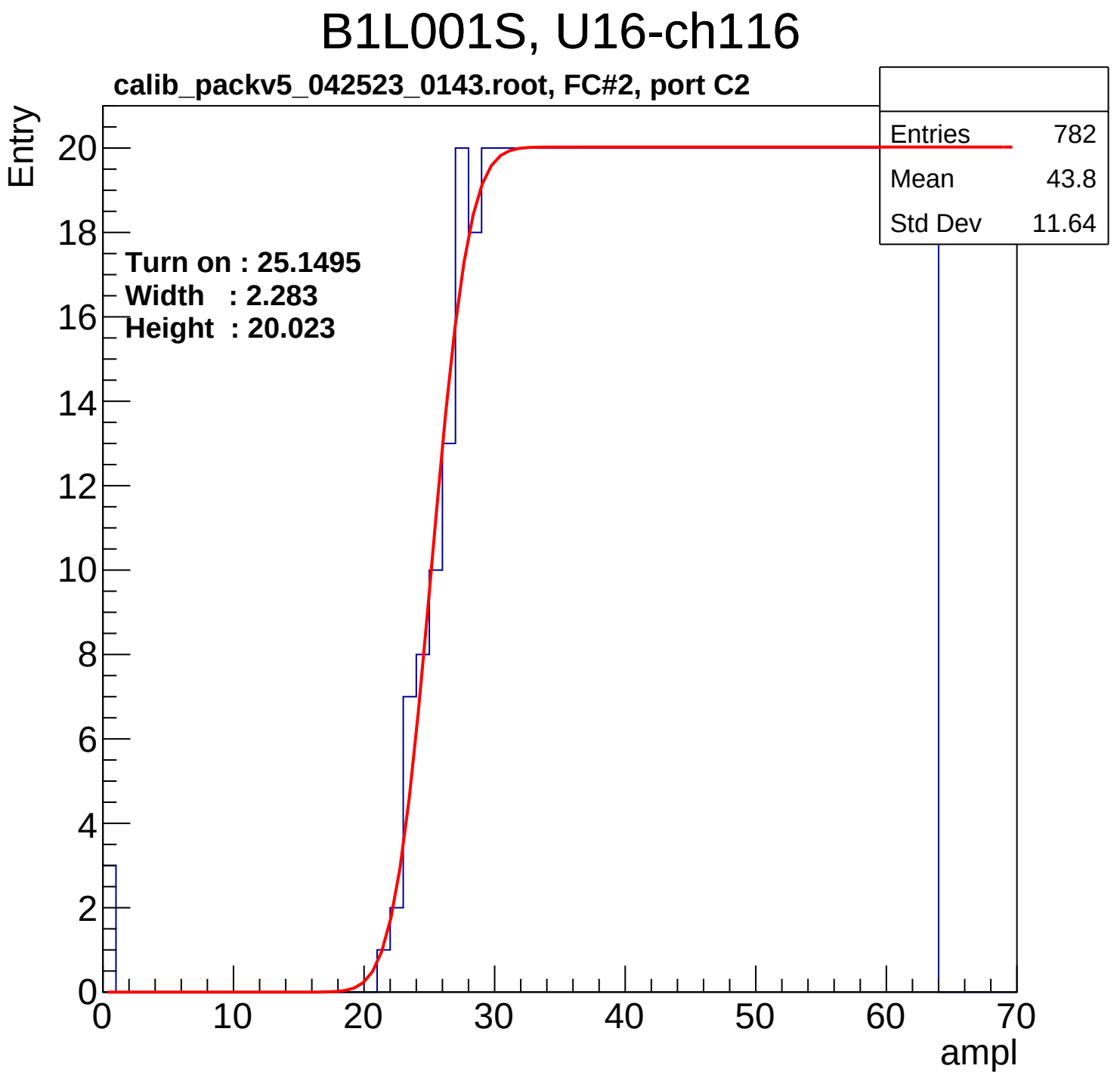
B1L001S, U16-ch116
calib_packv5_042523_0143.root, FC#2, port C2
Entries 782
Mean 43.8
Std Dev 11.64
Turn on : 25.1495
Width : 2.283
Height : 20.023
Entry
ampl
0
2
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6
8
10
12
14
16
18
20
0
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20
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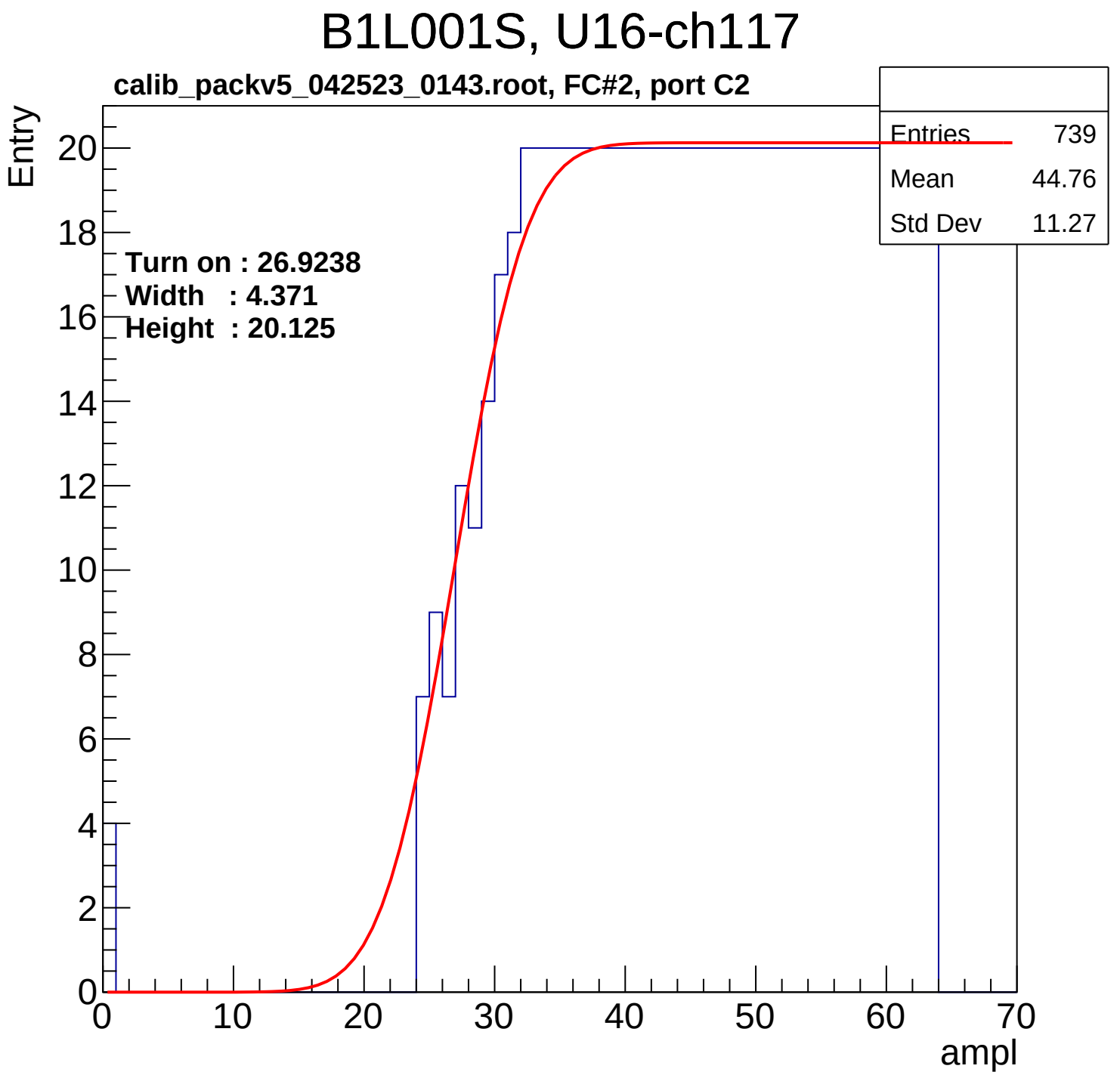
B1L001S, U16-ch117
calib_packv5_042523_0143.root, FC#2, port C2
Entries 739
Mean 44.76
Std Dev 11.27
Turn on : 26.9238
Width : 4.371
Height : 20.125
Entry
ampl
0
2
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6
8
10
12
14
16
18
20
0
10
20
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60
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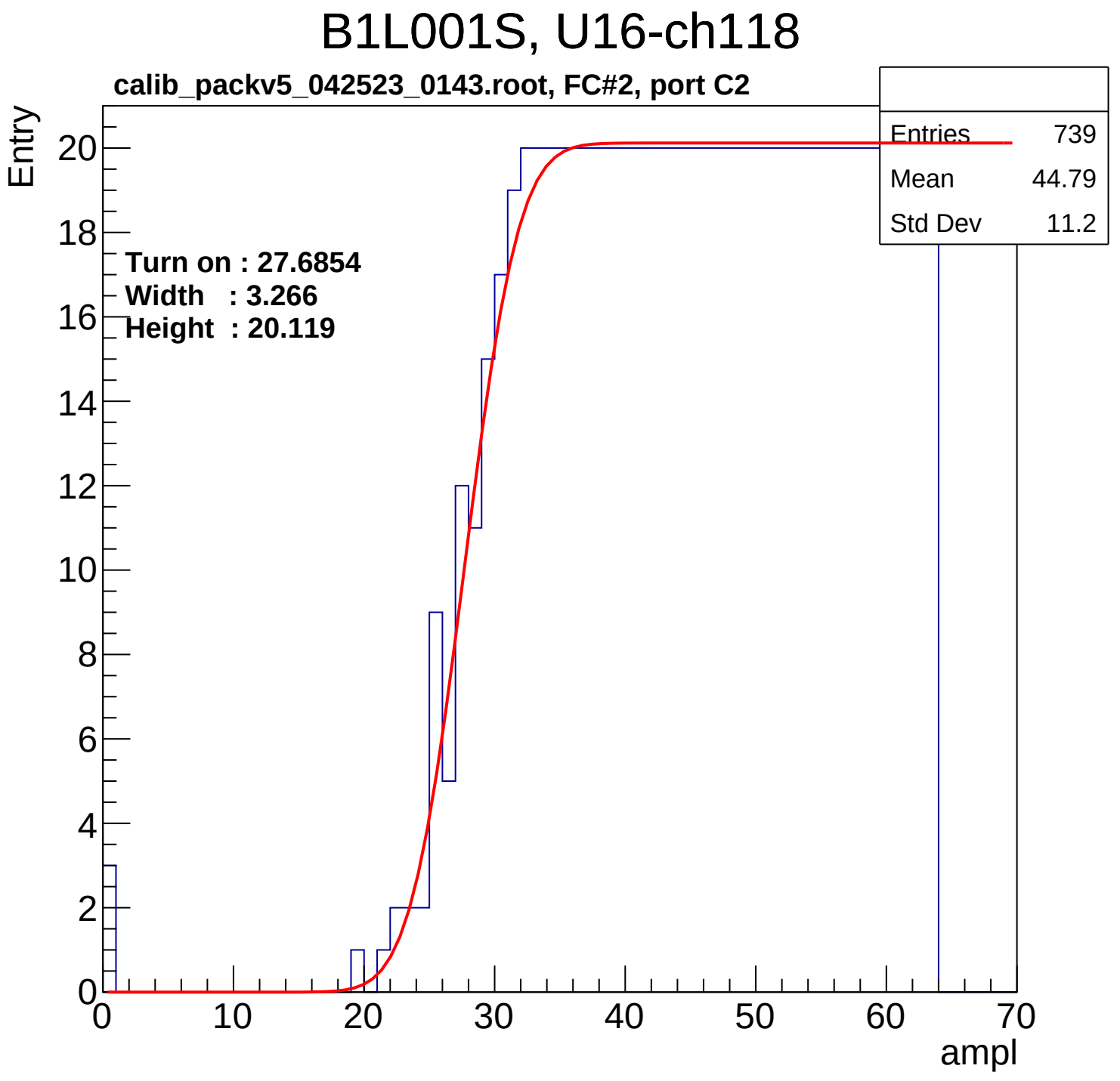
B1L001S, U16-ch118
calib_packv5_042523_0143.root, FC#2, port C2
Entries 739
Mean 44.79
Std Dev 11.2
Turn on : 27.6854
Width : 3.266
Height : 20.119
Entry
ampl
0
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6
8
10
12
14
16
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0
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20
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60
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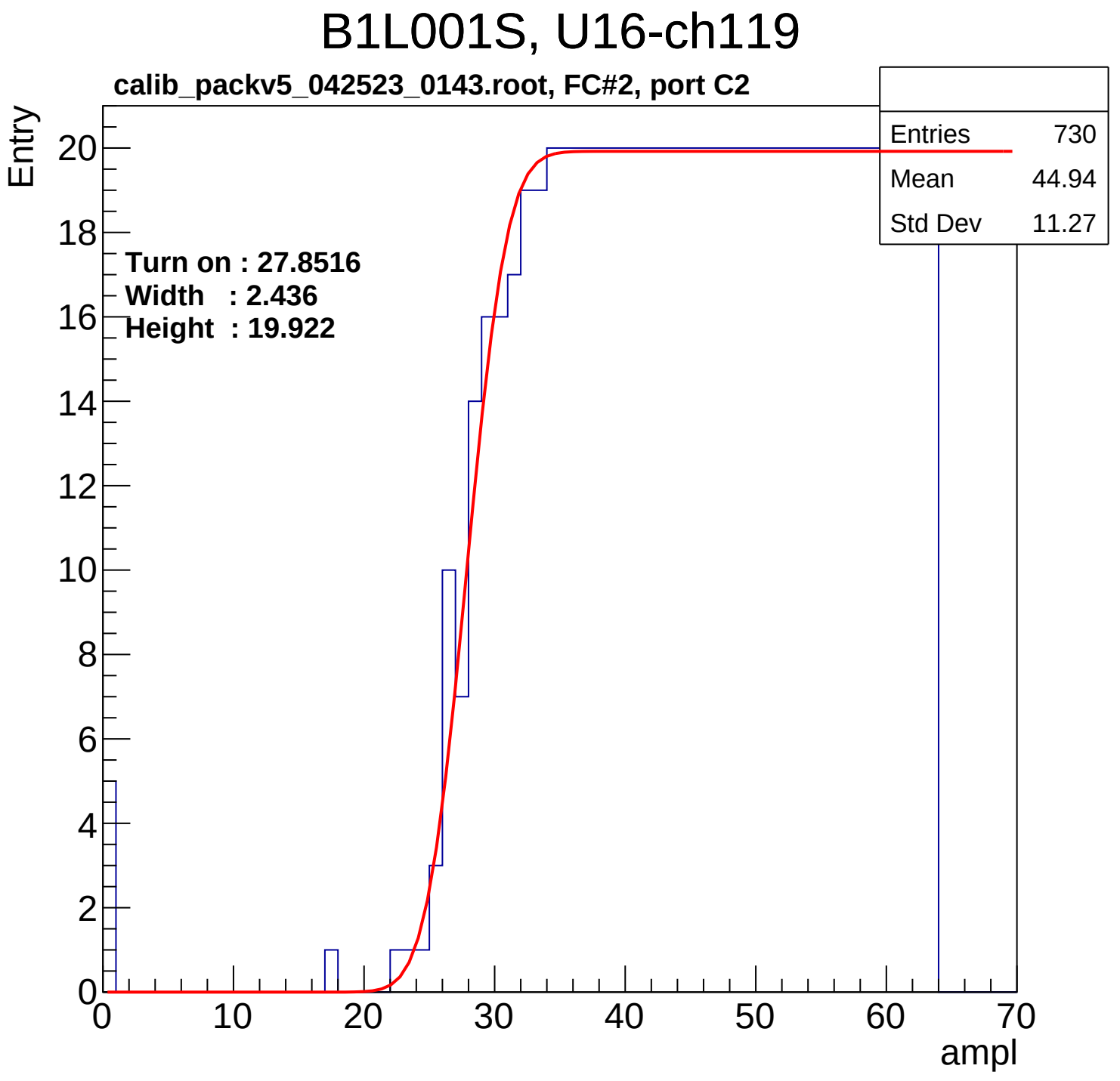
B1L001S, U16-ch119
calib_packv5_042523_0143.root, FC#2, port C2
Entries 730
Mean 44.94
Std Dev 11.27
Turn on : 27.8516
Width : 2.436
Height : 19.922
Entry
ampl
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6
8
10
12
14
16
18
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0
10
20
30
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60
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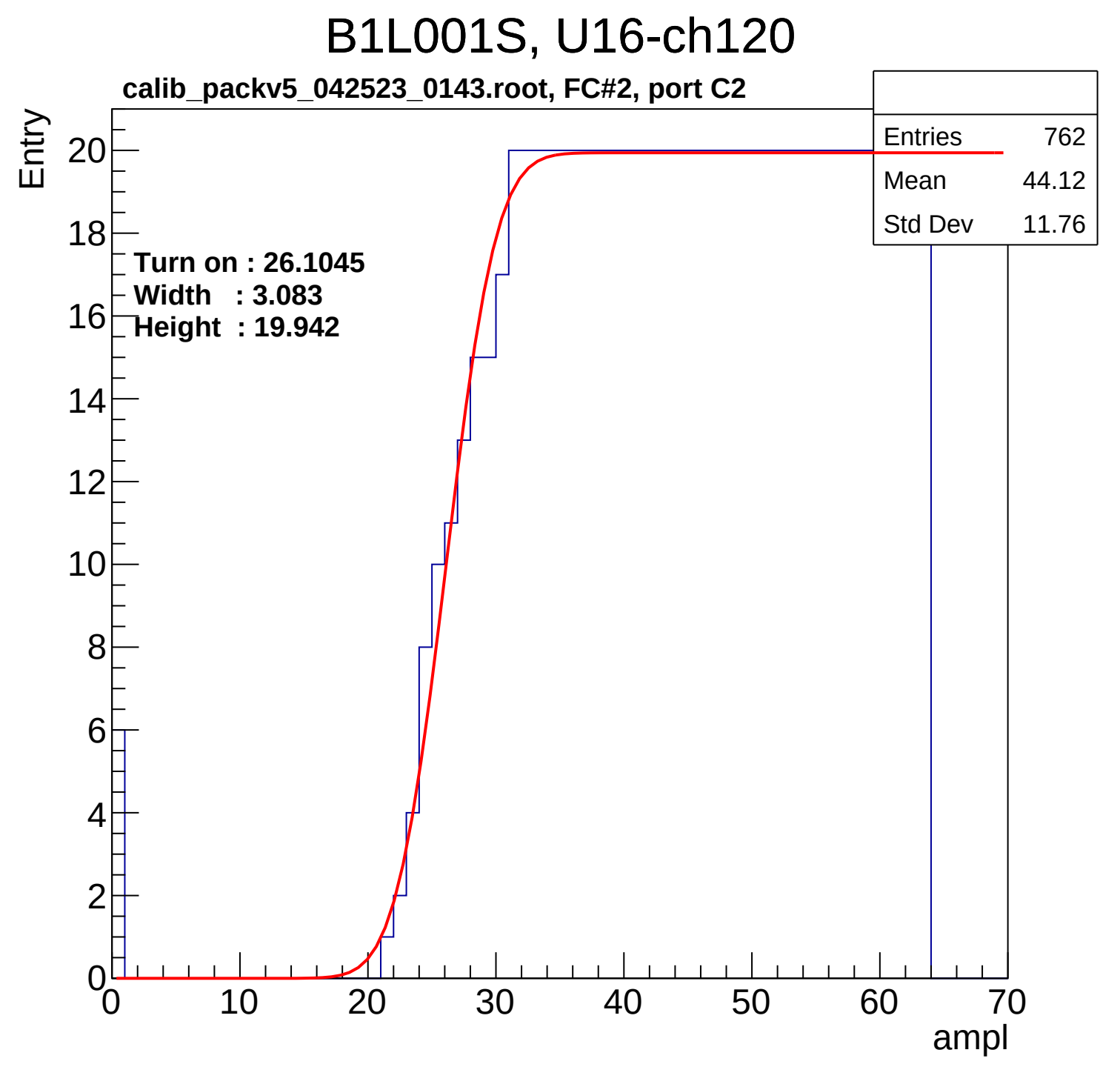
B1L001S, U16-ch120
calib_packv5_042523_0143.root, FC#2, port C2
Entries 762
Mean 44.12
Std Dev 11.76
Turn on : 26.1045
Width : 3.083
Height : 19.942
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
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20
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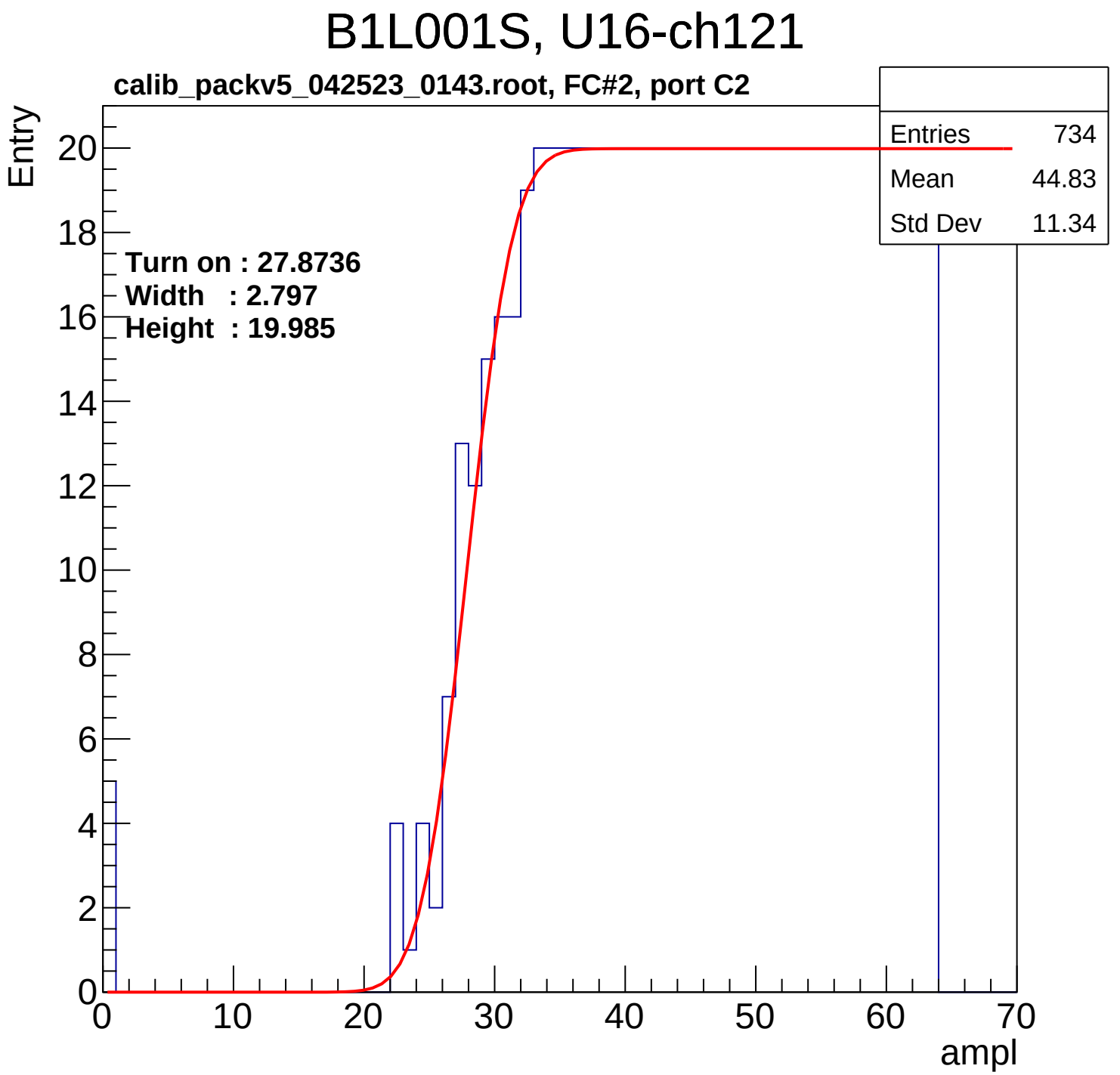
B1L001S, U16-ch121
calib_packv5_042523_0143.root, FC#2, port C2
Entries 734
Mean 44.83
Std Dev 11.34
Turn on : 27.8736
Width : 2.797
Height : 19.985
Entry
ampl
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6
8
10
12
14
16
18
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0
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20
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60
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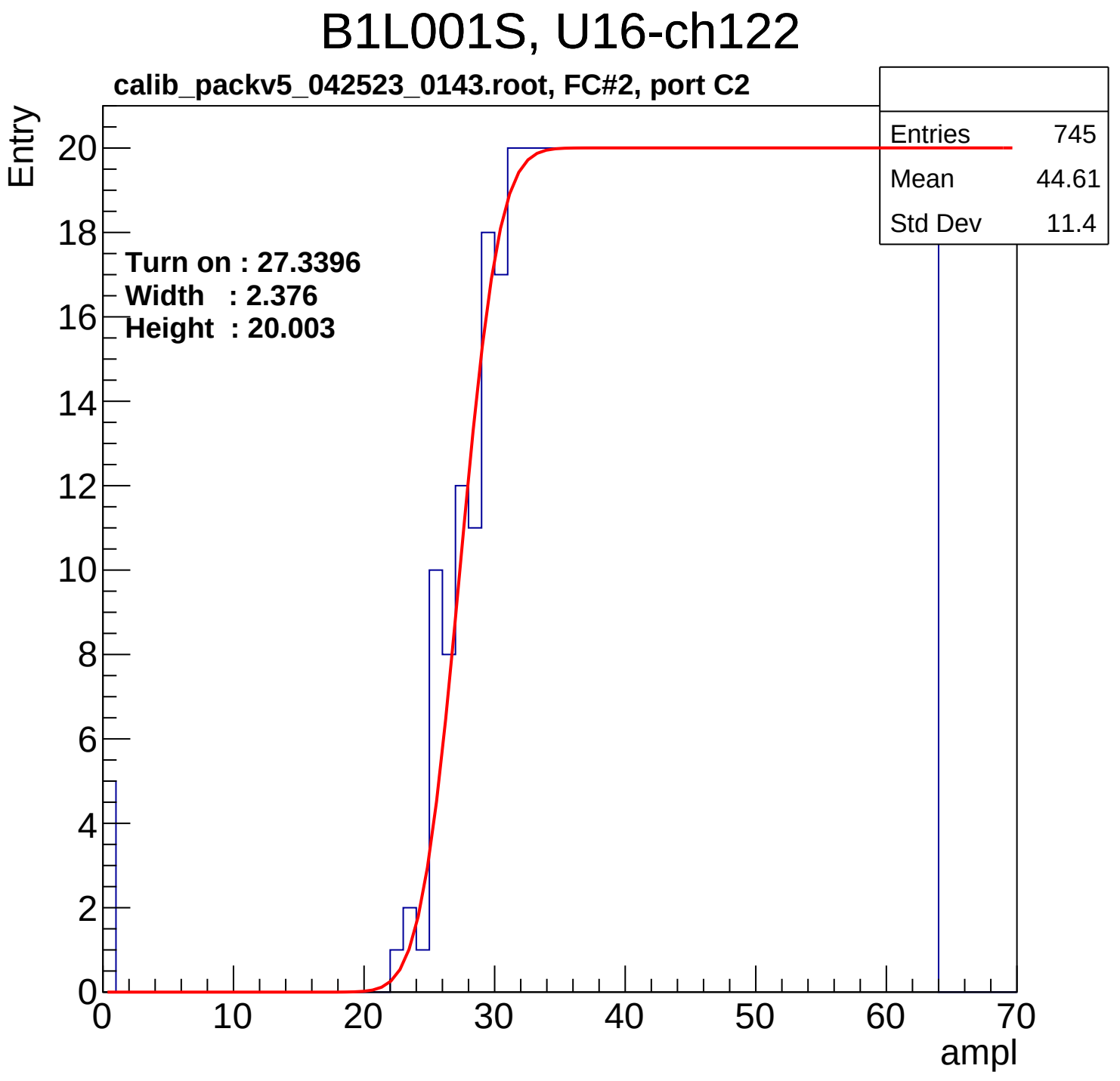
B1L001S, U16-ch122
calib_packv5_042523_0143.root, FC#2, port C2
Entries 745
Mean 44.61
Std Dev 11.4
Turn on : 27.3396
Width : 2.376
Height : 20.003
Entry
ampl
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6
8
10
12
14
16
18
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0
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20
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40
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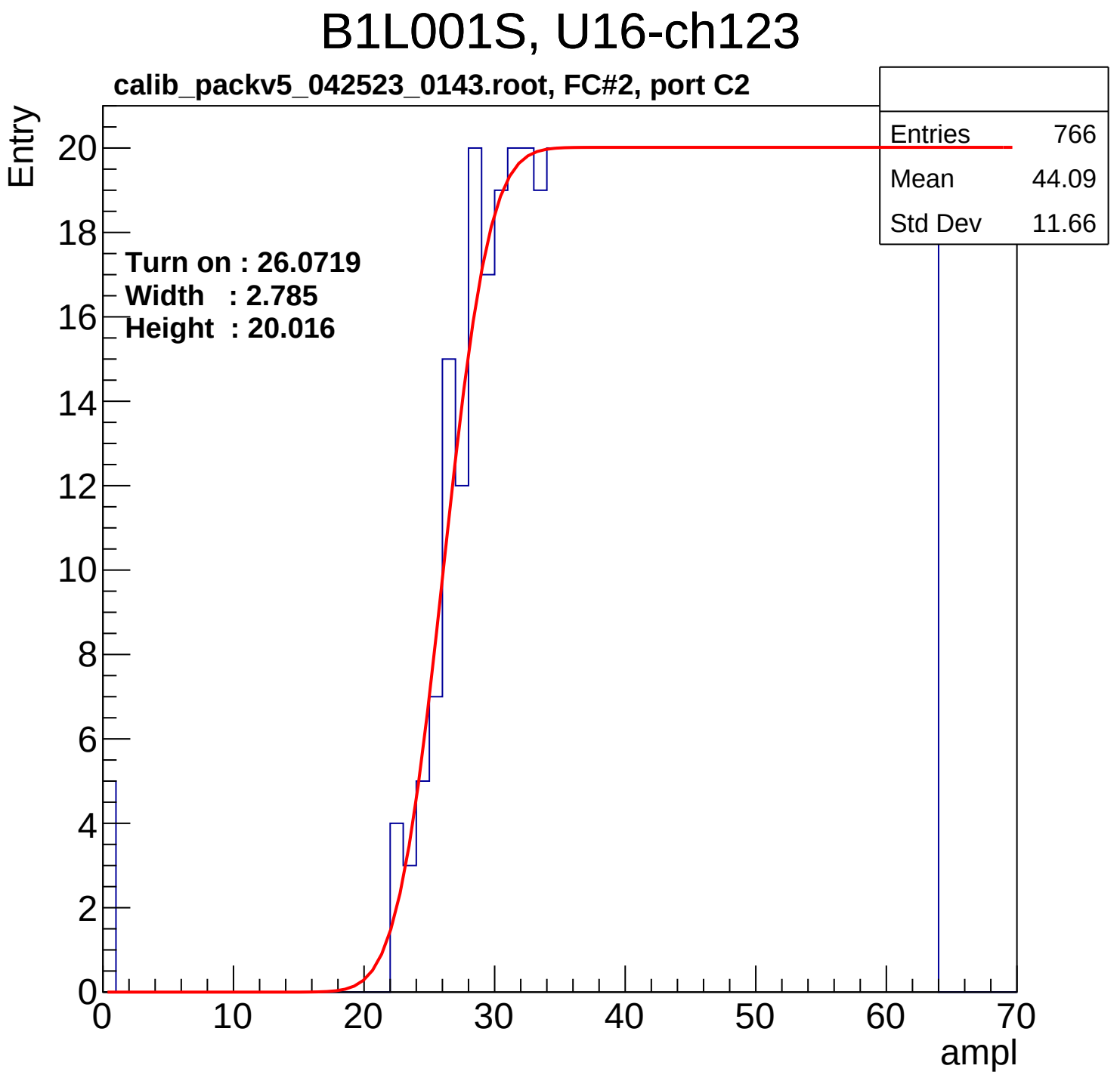
B1L001S, U16-ch123
calib_packv5_042523_0143.root, FC#2, port C2
Entries 766
Mean 44.09
Std Dev 11.66
Turn on : 26.0719
Width : 2.785
Height : 20.016
Entry
ampl
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6
8
10
12
14
16
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0
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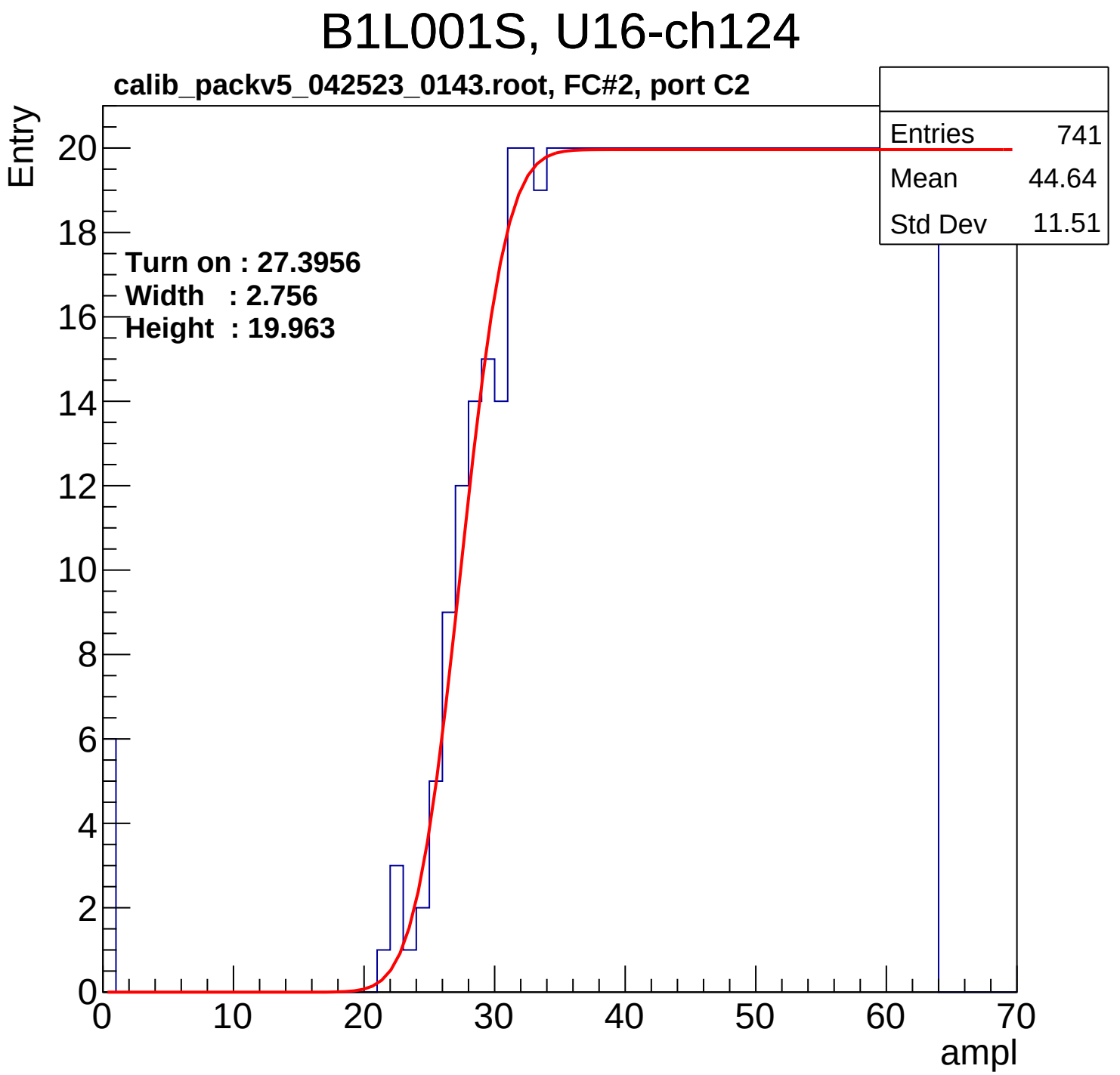
B1L001S, U16-ch124
calib_packv5_042523_0143.root, FC#2, port C2
Entries 741
Mean 44.64
Std Dev 11.51
Turn on : 27.3956
Width : 2.756
Height : 19.963
Entry
ampl
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6
8
10
12
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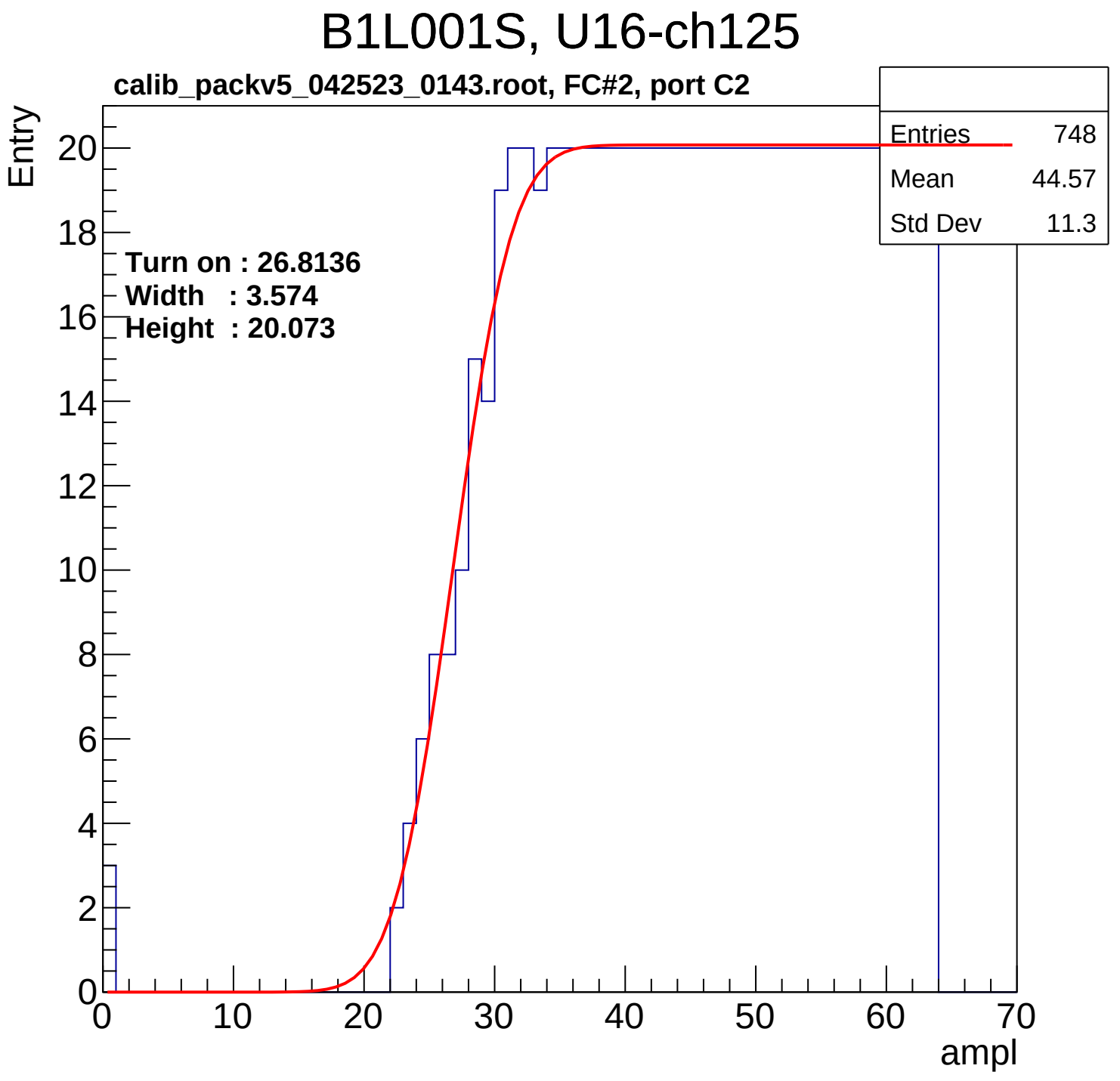
B1L001S, U16-ch125
calib_packv5_042523_0143.root, FC#2, port C2
Entries 748
Mean 44.57
Std Dev 11.3
Turn on : 26.8136
Width : 3.574
Height : 20.073
Entry
ampl
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6
8
10
12
14
16
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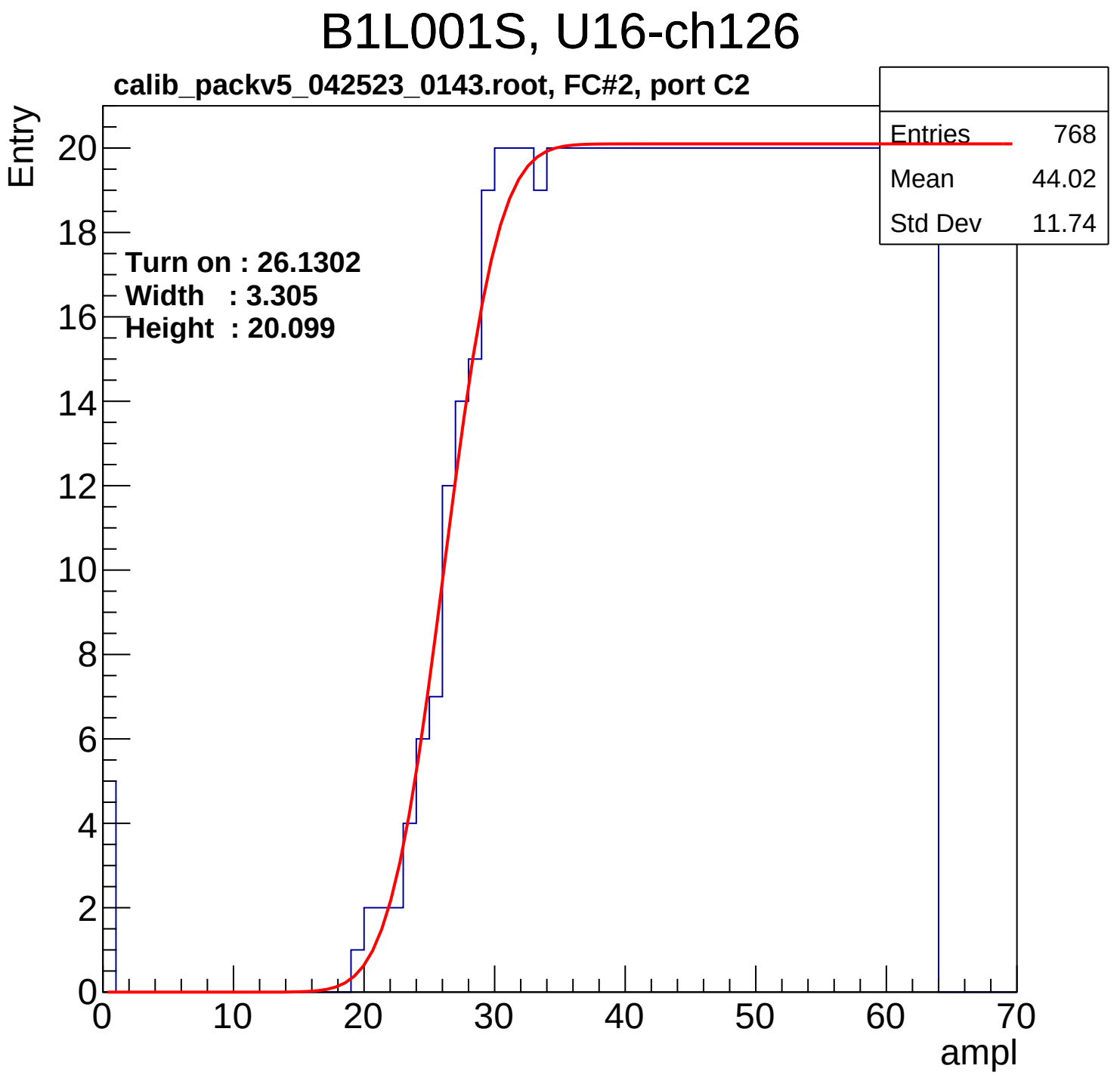
B1L001S, U16-ch126
calib_packv5_042523_0143.root, FC#2, port C2
Entries 768
Mean 44.02
Std Dev 11.74
Turn on : 26.1302
Width : 3.305
Height : 20.099
Entry
ampl
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8
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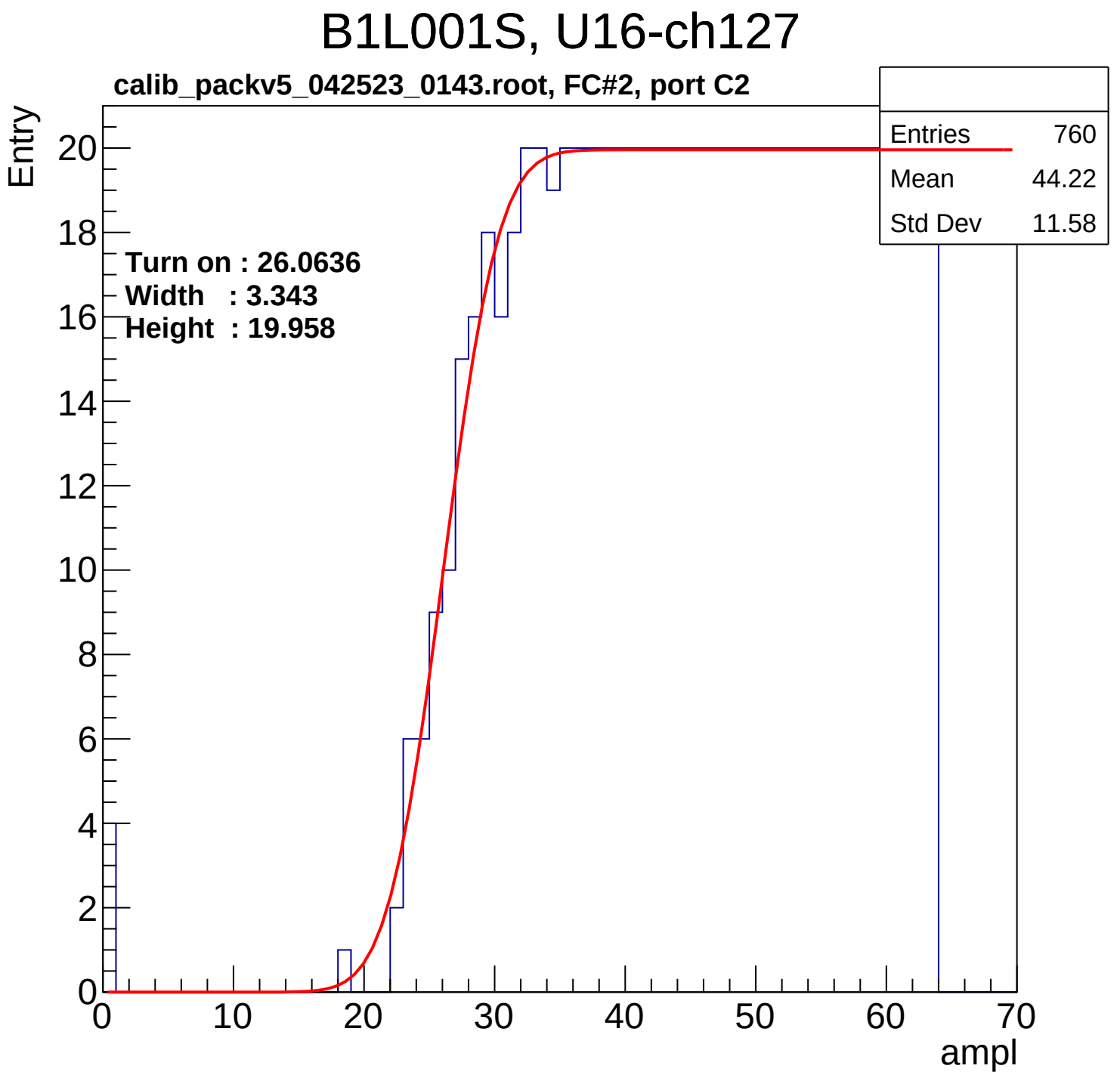
B1L001S, U16-ch127
calib_packv5_042523_0143.root, FC#2, port C2
Entries 760
Mean 44.22
Std Dev 11.58
Turn on : 26.0636
Width : 3.343
Height : 19.958
Entry
ampl
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8
10
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14
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0
10
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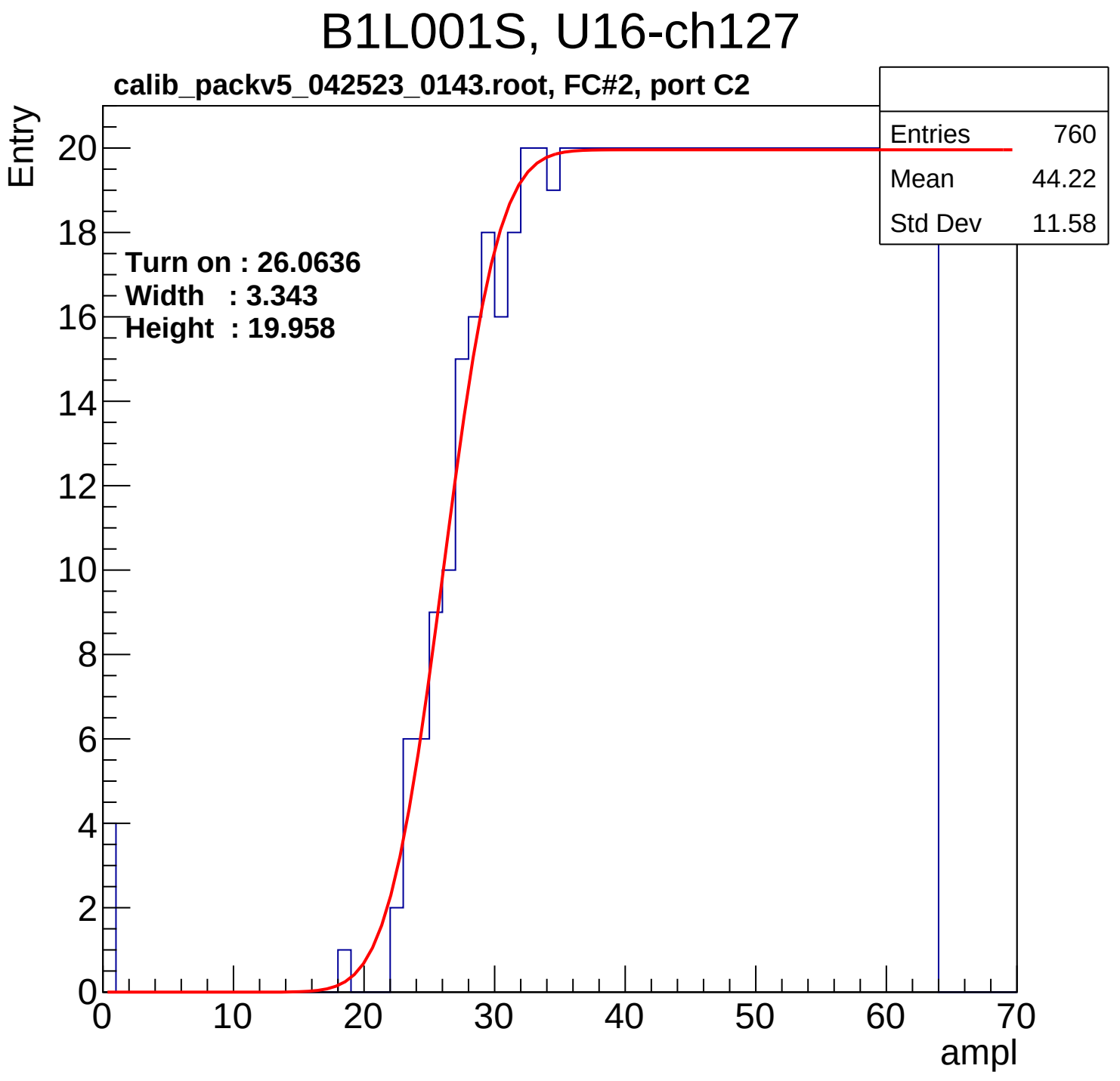
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calib_packv5_042523_0143.root, FC#2, port C2
Entries 760
Mean 44.22
Std Dev 11.58
Turn on : 26.0636
Width : 3.343
Height : 19.958
Entry
ampl
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