

B1L102S, U20-ch0

calib_packv5_042523_0143.root, FC#11, port A2

Entries	385
Mean	43.79
Std Dev	12.12

Turn on : 26.6071

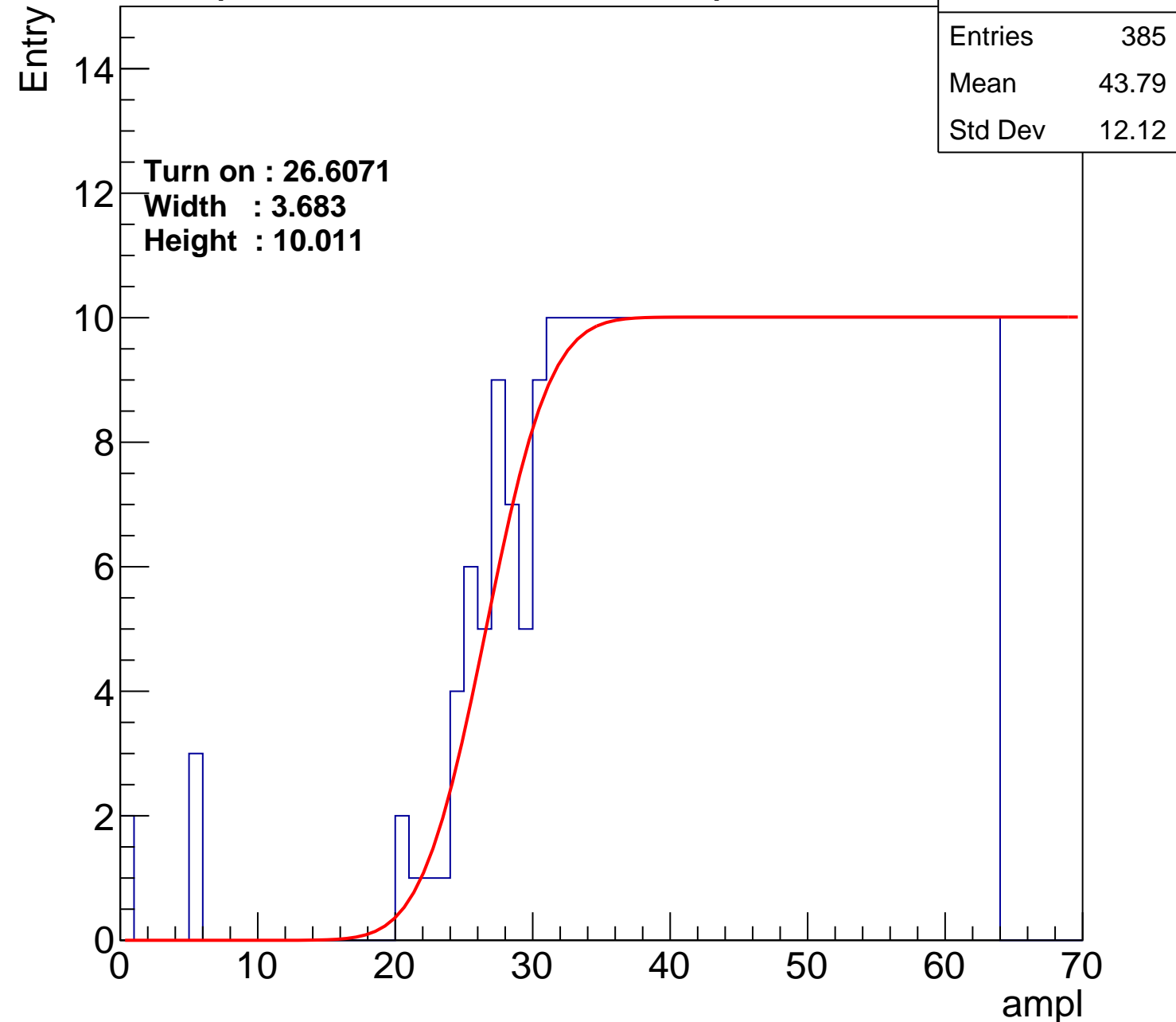
Width : 3.683

Height : 10.011

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U20-ch1

calib_packv5_042523_0143.root, FC#11, port A2

Entries	371
Mean	44.58
Std Dev	11.57

Turn on : 27.4509

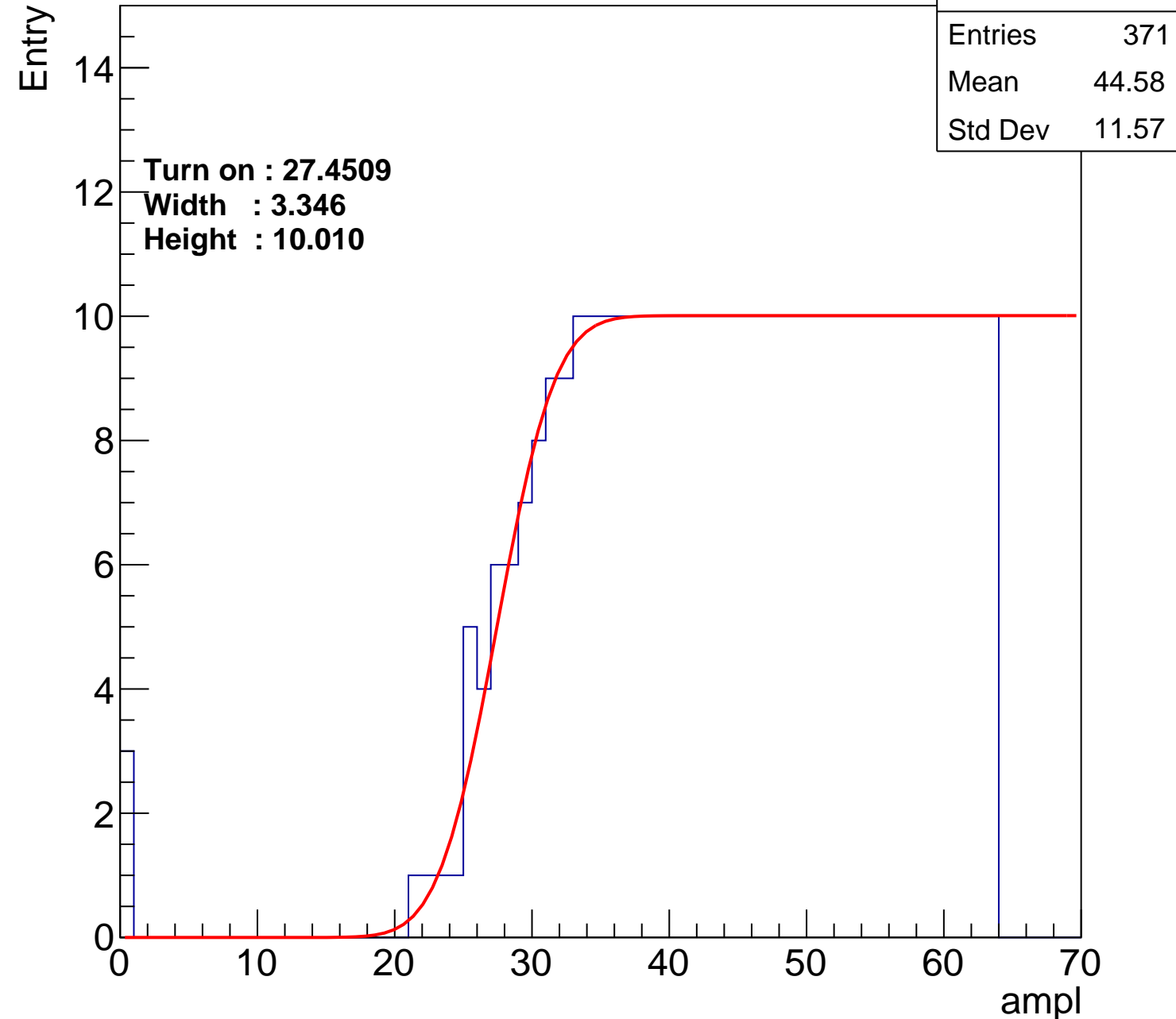
Width : 3.346

Height : 10.010

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U20-ch2

calib_packv5_042523_0143.root, FC#11, port A2

Entries	398
Mean	43.41
Std Dev	11.93

Turn on : 24.7384

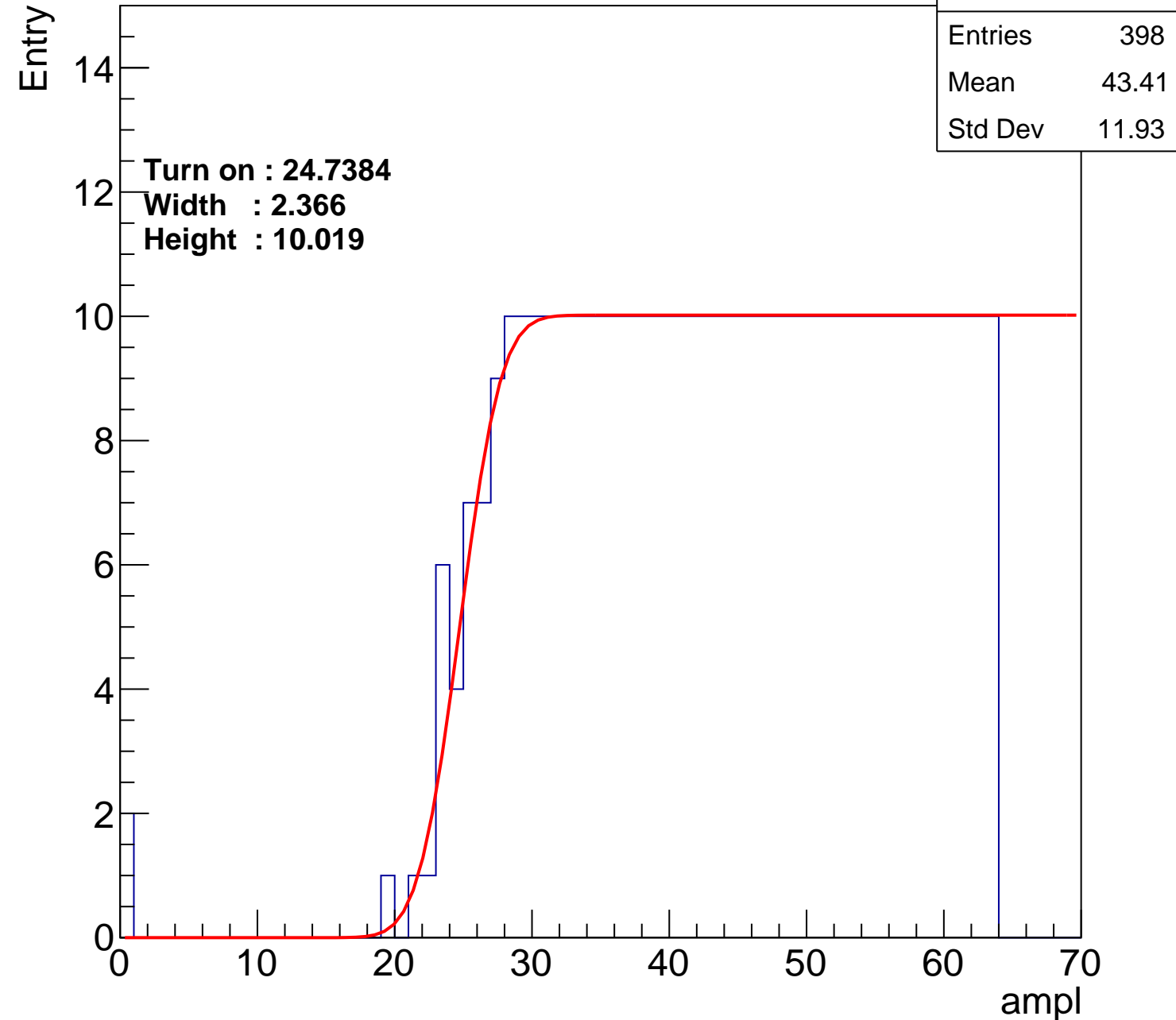
Width : 2.366

Height : 10.019

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U20-ch3

calib_packv5_042523_0143.root, FC#11, port A2

Entries	393
Mean	43.64
Std Dev	11.82

Turn on : 25.0896

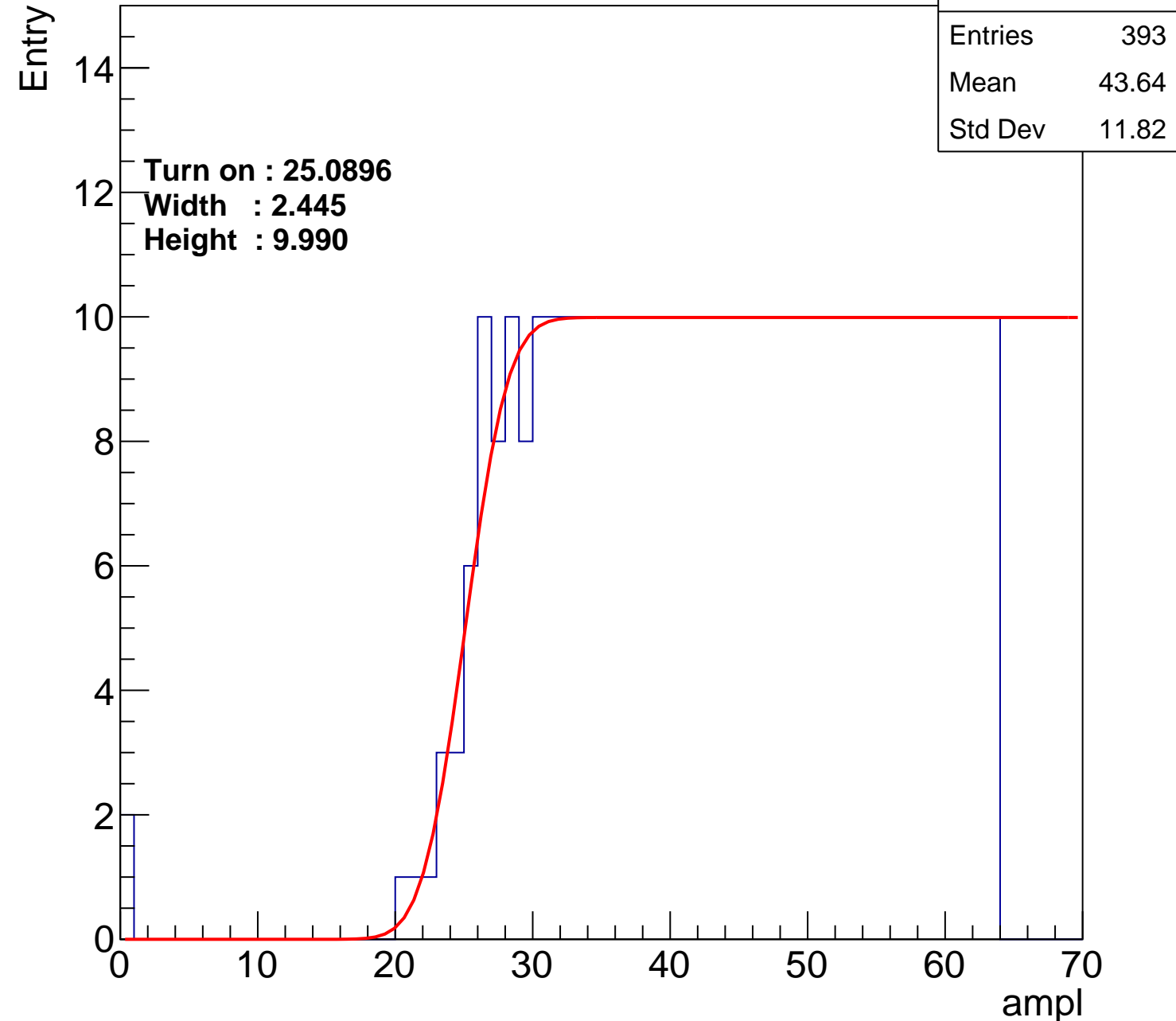
Width : 2.445

Height : 9.990

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U20-ch4

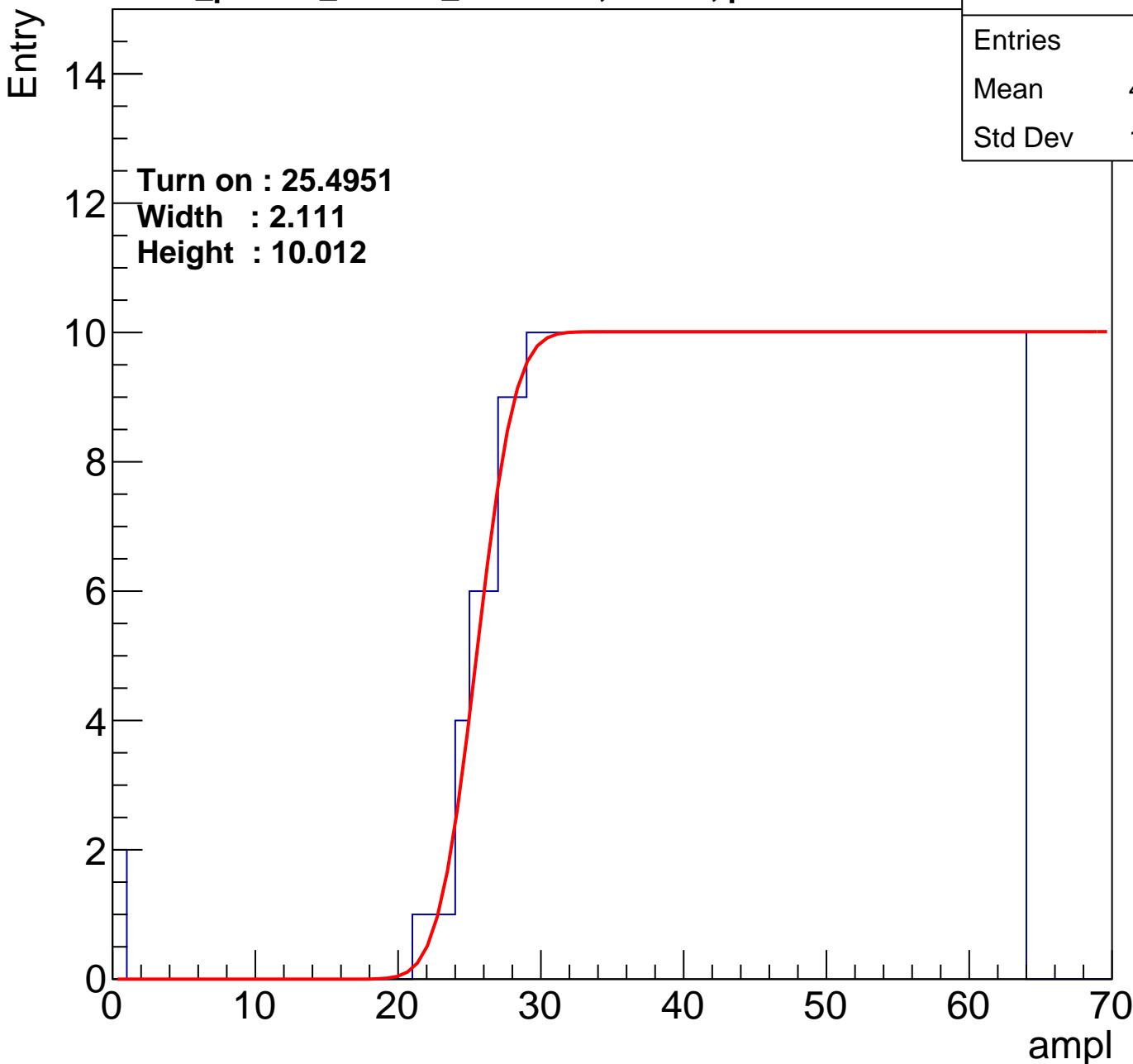
calib_packv5_042523_0143.root, FC#11, port A2

Turn on : 25.4951

Width : 2.111

Height : 10.012

Entries	389
Mean	43.86
Std Dev	11.68



B1L102S, U20-ch5

calib_packv5_042523_0143.root, FC#11, port A2

Entries	396
Mean	43.53
Std Dev	11.9

Turn on : 24.9016

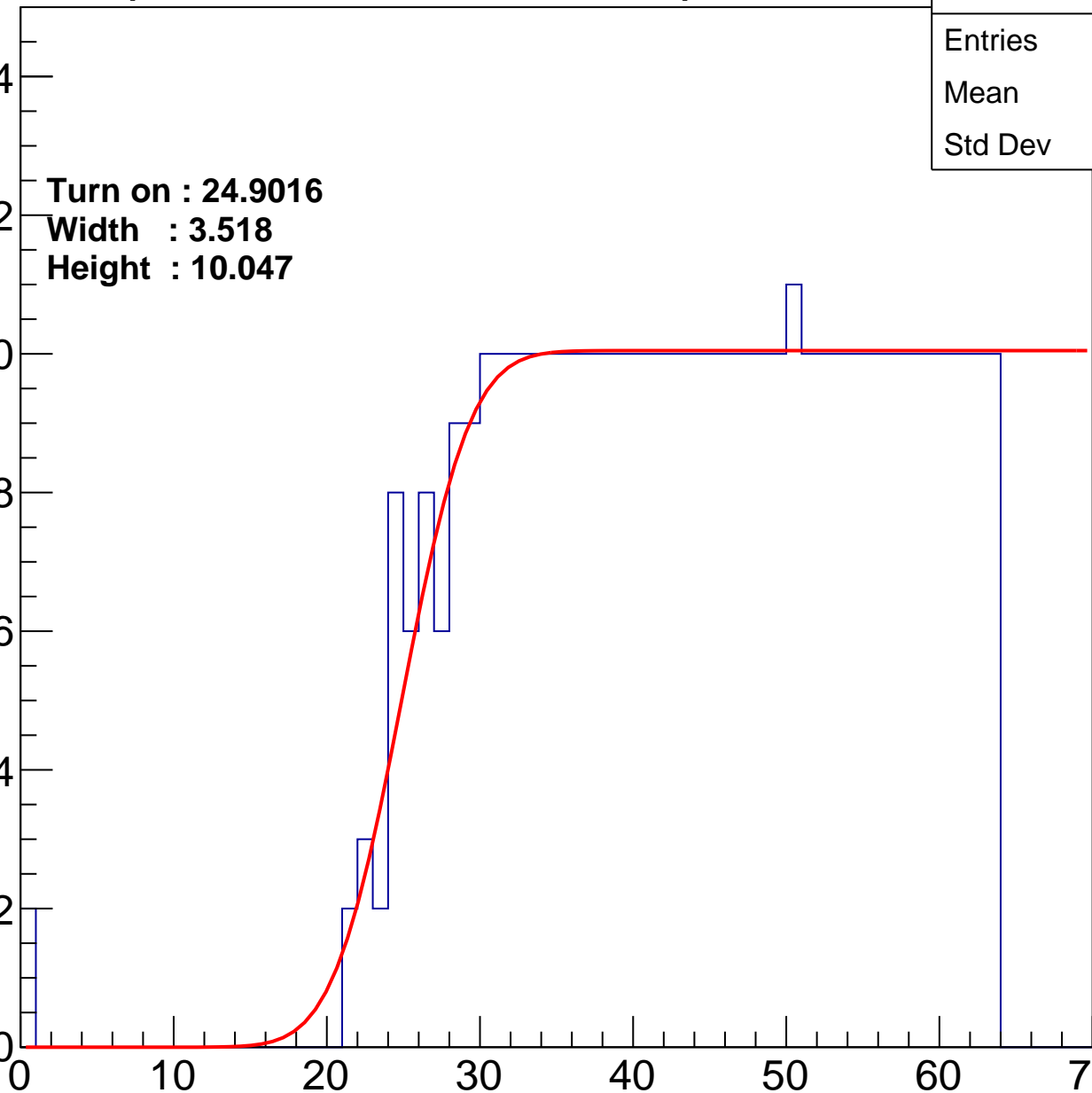
Width : 3.518

Height : 10.047

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U20-ch6

calib_packv5_042523_0143.root, FC#11, port A2

Entries	382
Mean	44.21
Std Dev	11.42

Turn on : 25.8874

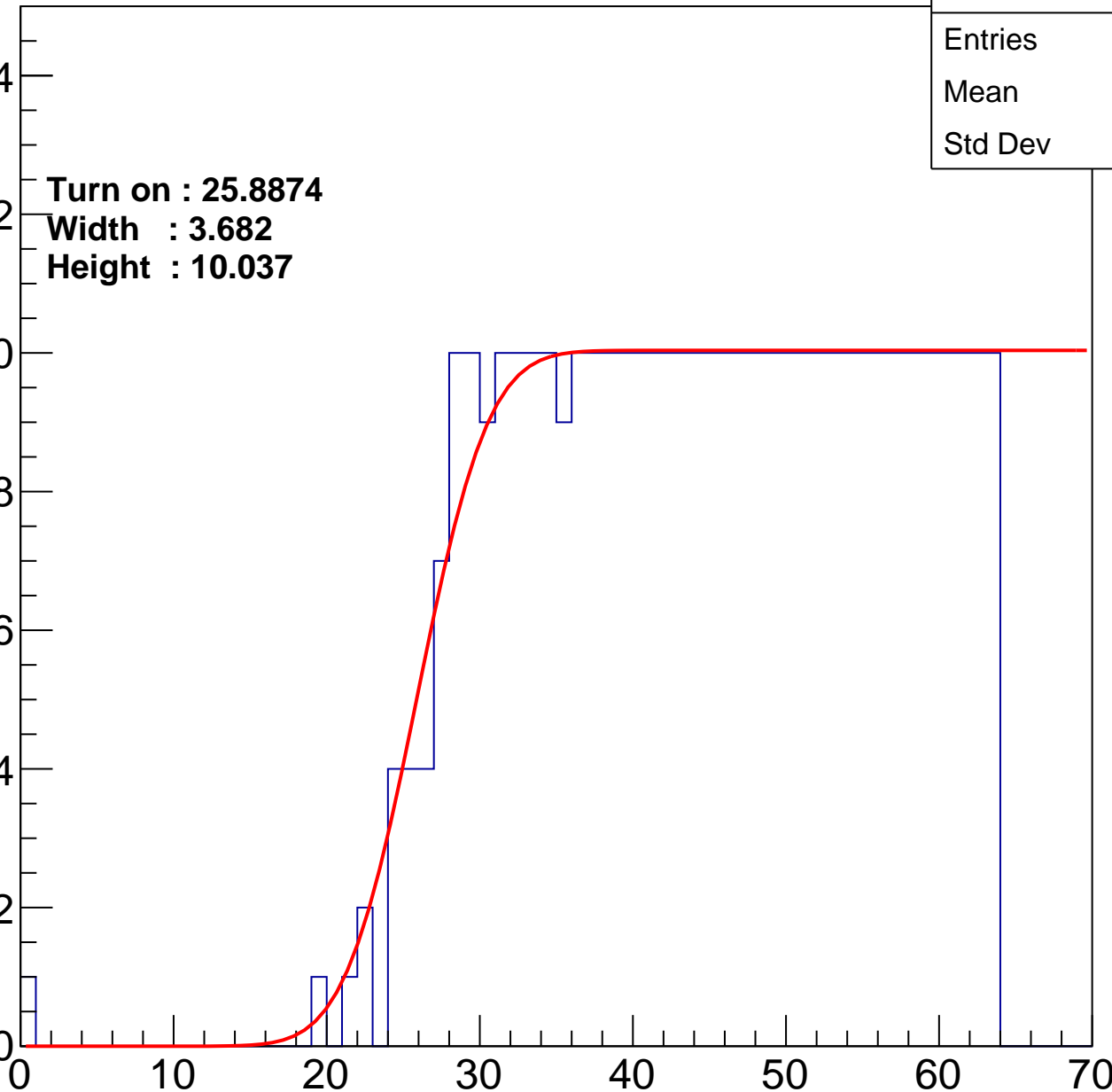
Width : 3.682

Height : 10.037

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U20-ch7

calib_packv5_042523_0143.root, FC#11, port A2

Entries	368
Mean	44.93
Std Dev	11.01

Turn on : 27.9430

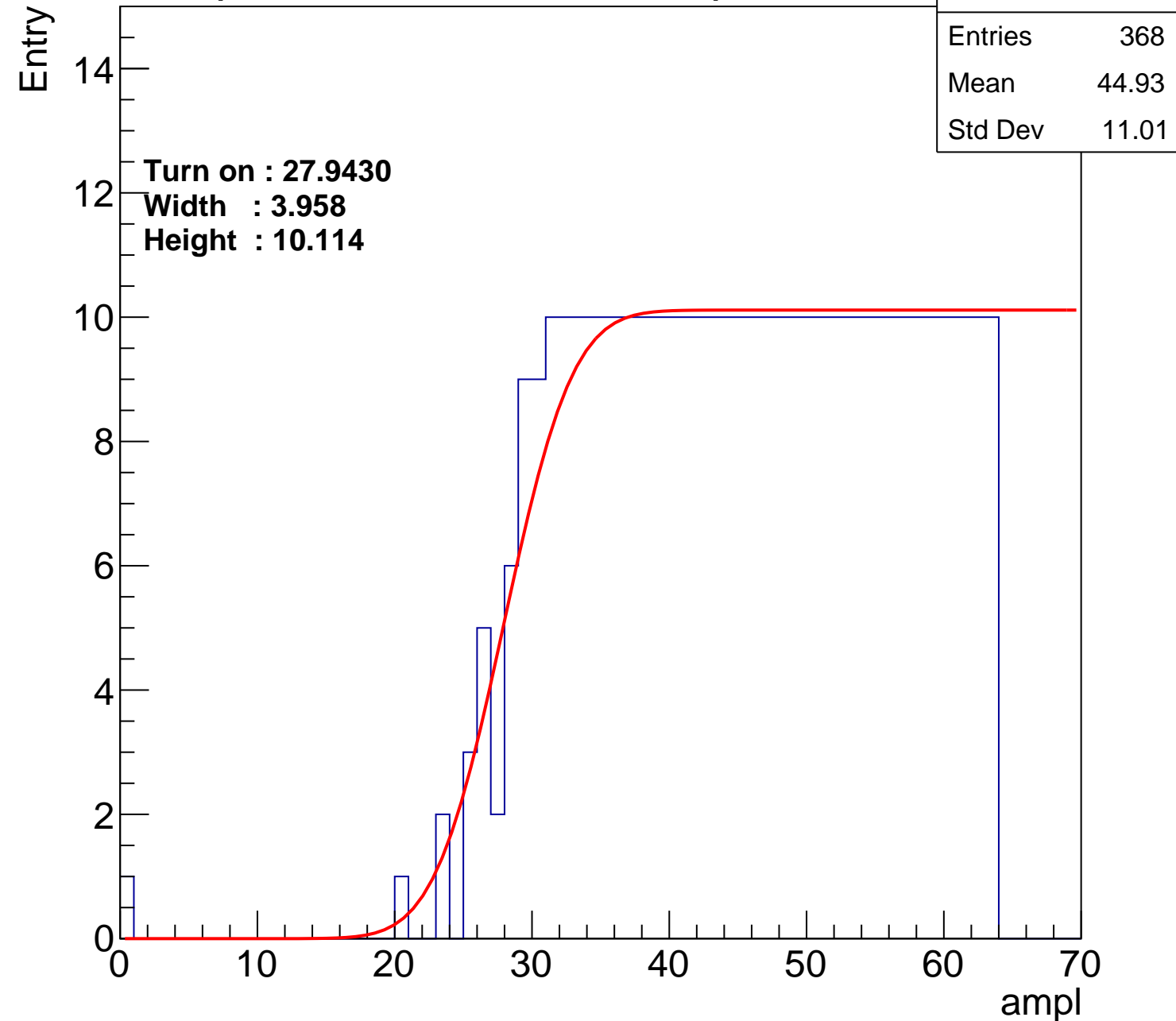
Width : 3.958

Height : 10.114

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U20-ch8

calib_packv5_042523_0143.root, FC#11, port A2

Entries	374
Mean	44.59
Std Dev	11.32

Turn on : 26.9996

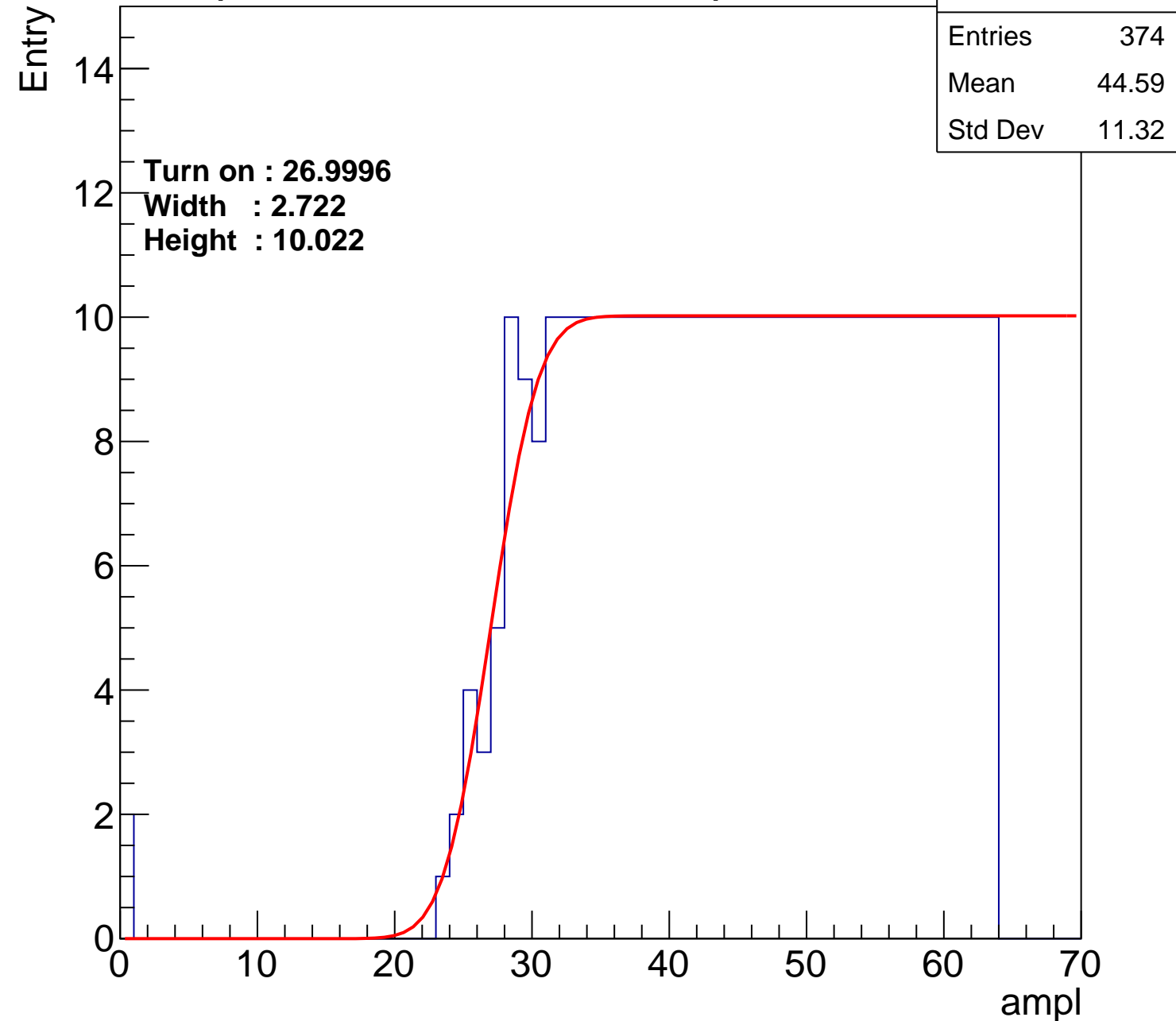
Width : 2.722

Height : 10.022

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U20-ch9

calib_packv5_042523_0143.root, FC#11, port A2

Entries	386
Mean	43.91
Std Dev	11.83

Turn on : 25.8127

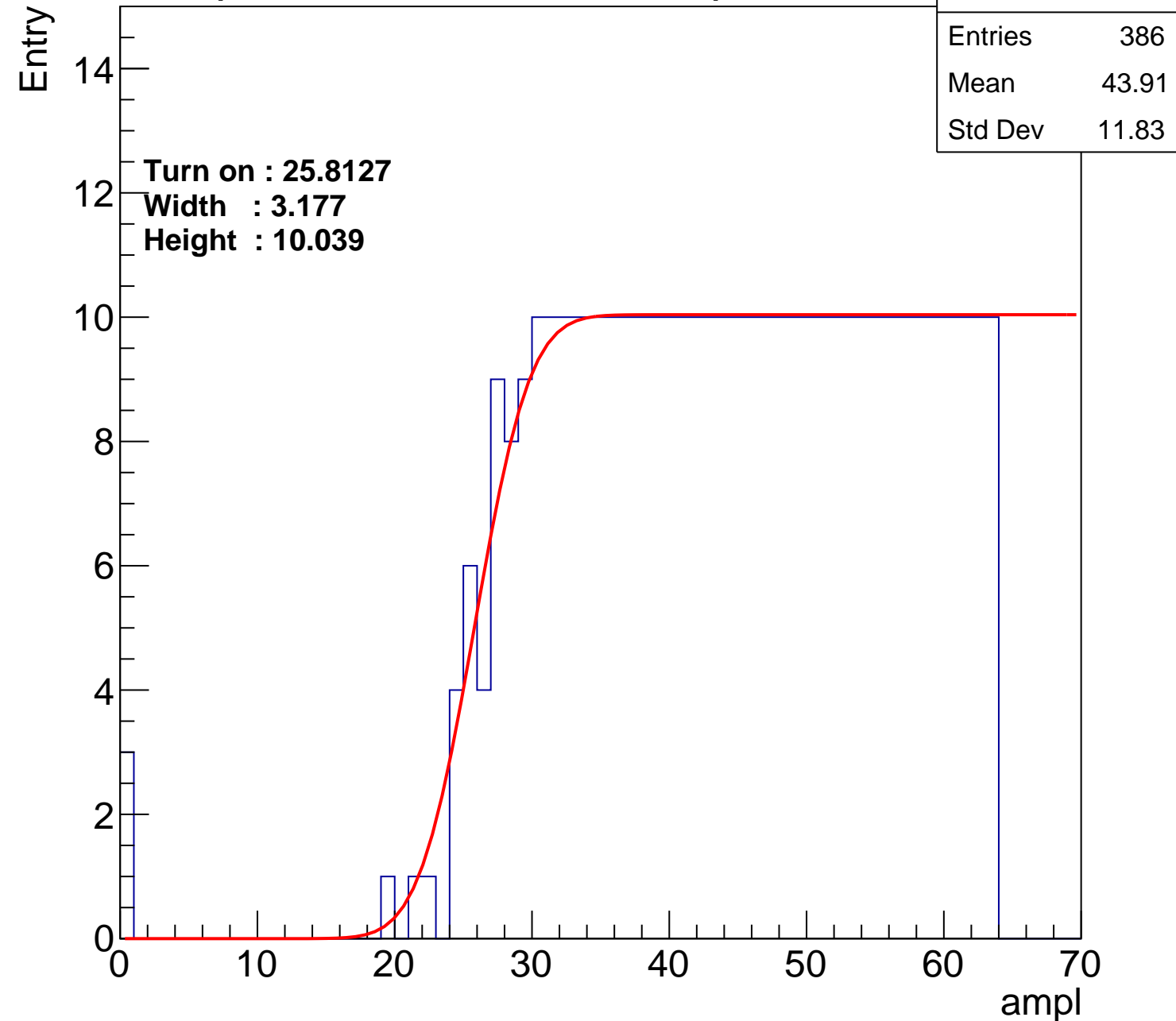
Width : 3.177

Height : 10.039

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U20-ch10

calib_packv5_042523_0143.root, FC#11, port A2

Entries	377
Mean	44.36
Std Dev	11.6

Turn on : 26.4536

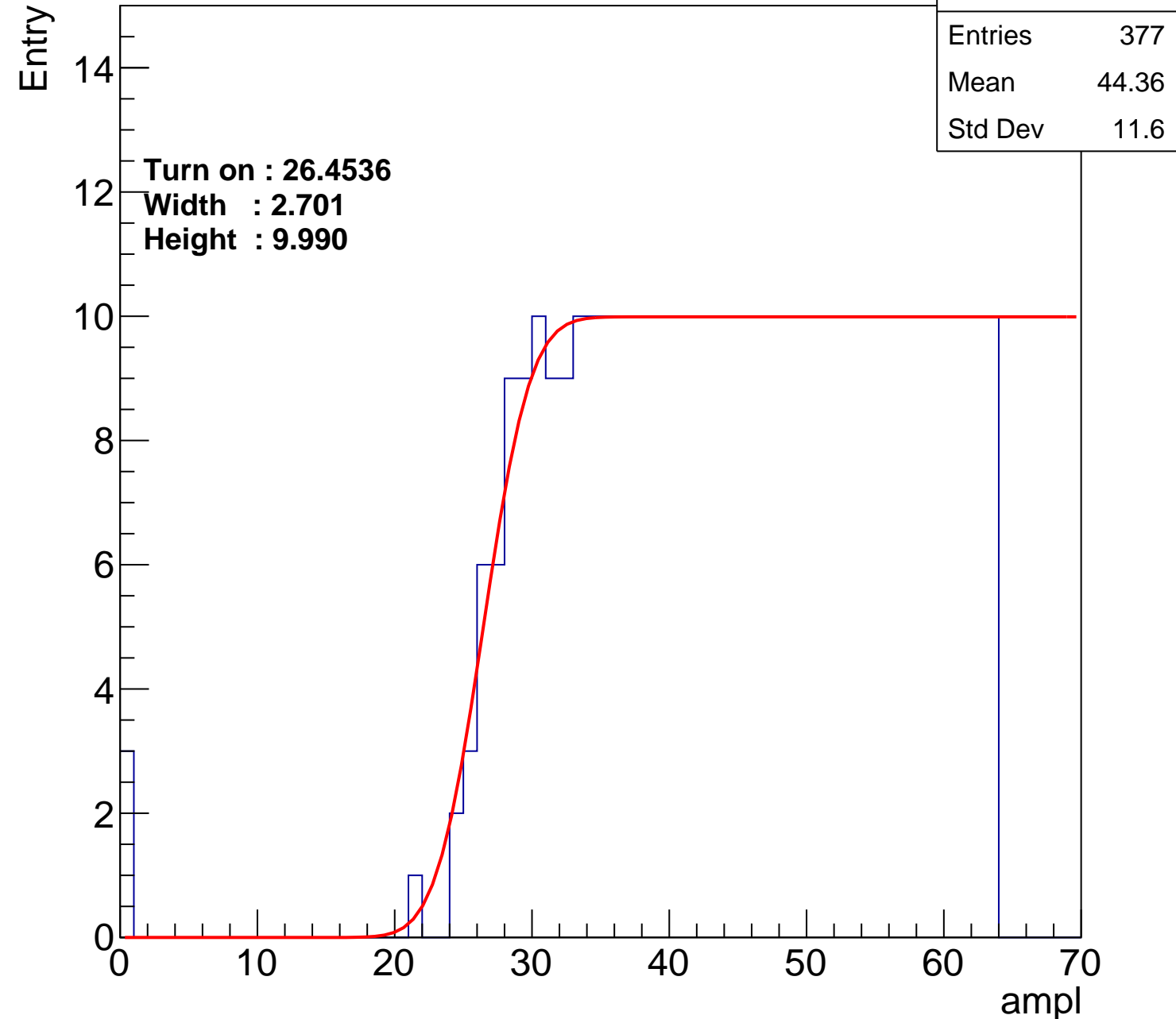
Width : 2.701

Height : 9.990

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U20-ch11

calib_packv5_042523_0143.root, FC#11, port A2

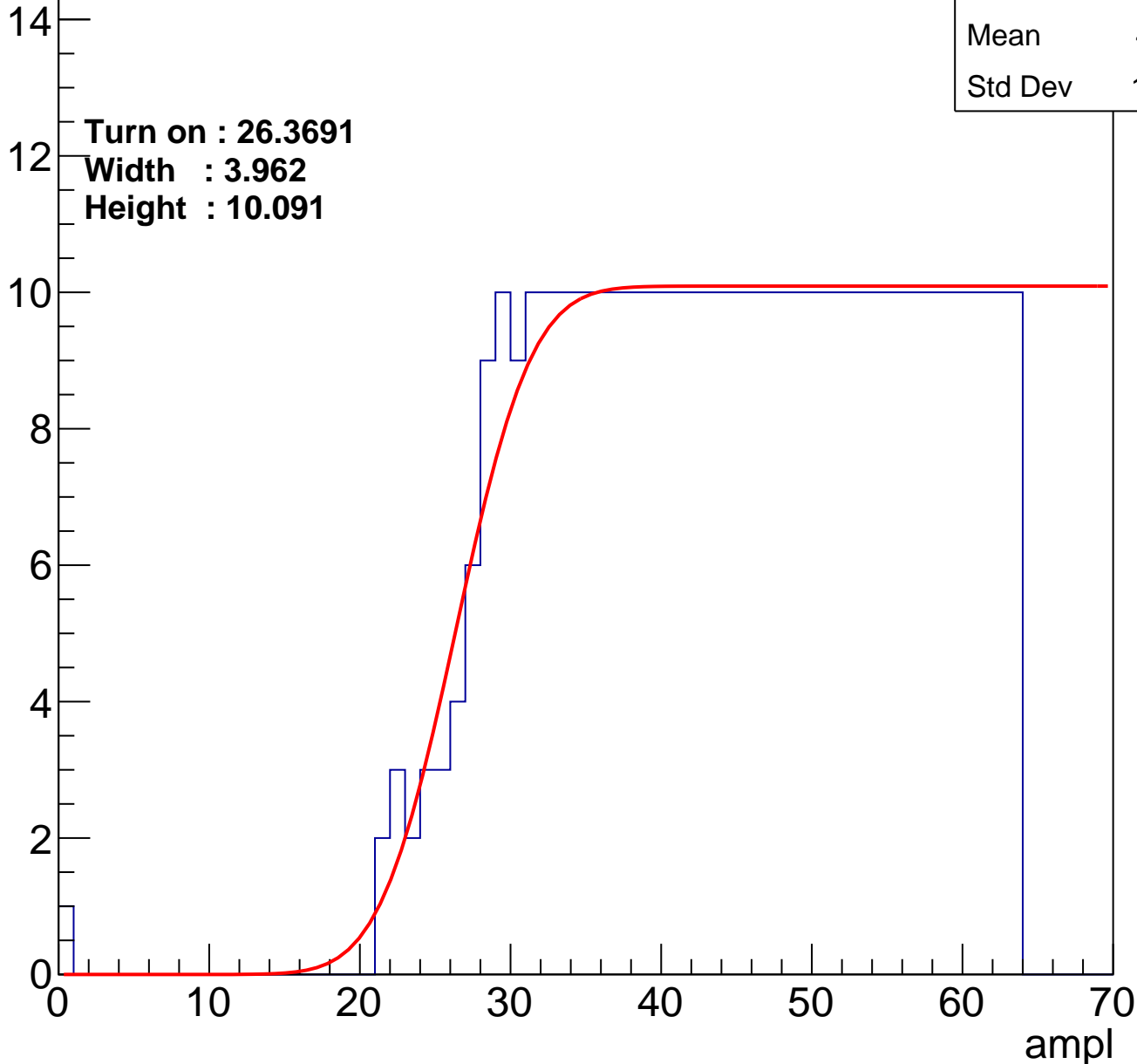
Entries	382
Mean	44.21
Std Dev	11.42

Turn on : 26.3691

Width : 3.962

Height : 10.091

Entry



B1L102S, U20-ch12

calib_packv5_042523_0143.root, FC#11, port A2

Entries	406
Mean	42.91
Std Dev	12.36

Turn on : 23.4915

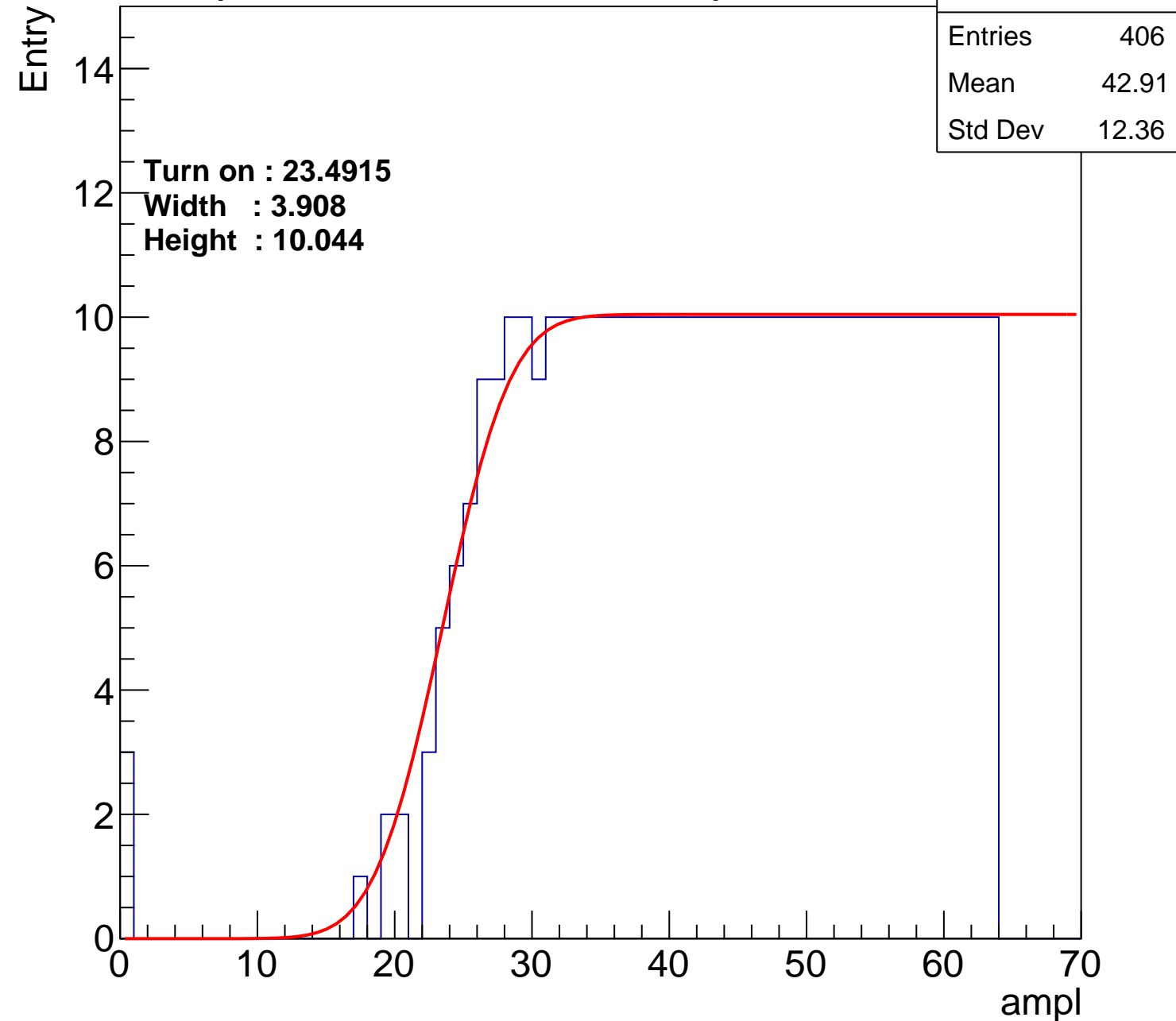
Width : 3.908

Height : 10.044

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U20-ch13

calib_packv5_042523_0143.root, FC#11, port A2

Entries	393
Mean	43.65
Std Dev	11.75

Turn on : 25.4475

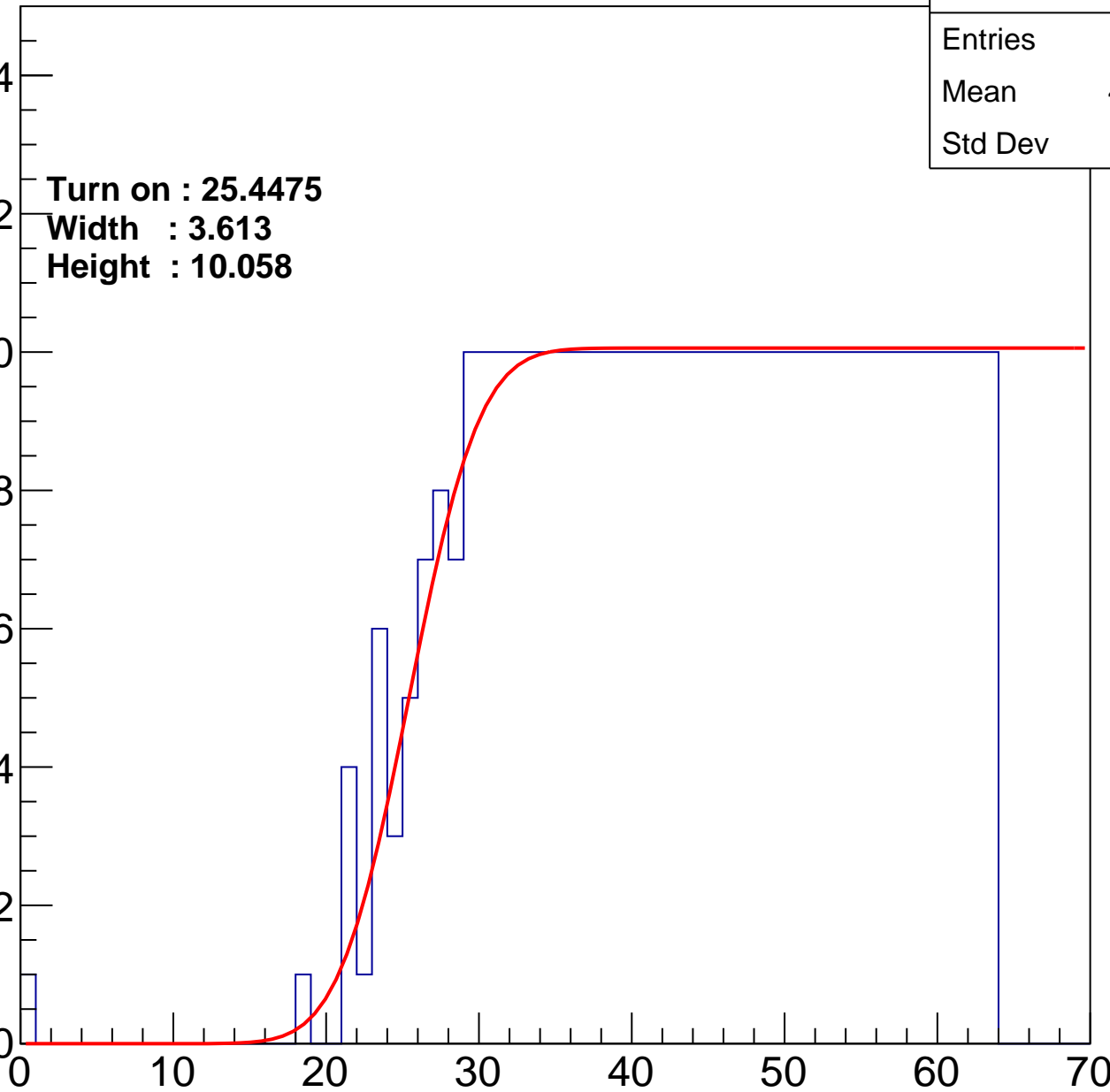
Width : 3.613

Height : 10.058

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U20-ch14

calib_packv5_042523_0143.root, FC#11, port A2

Entries	396
Mean	43.47
Std Dev	11.94

Turn on : 24.8289

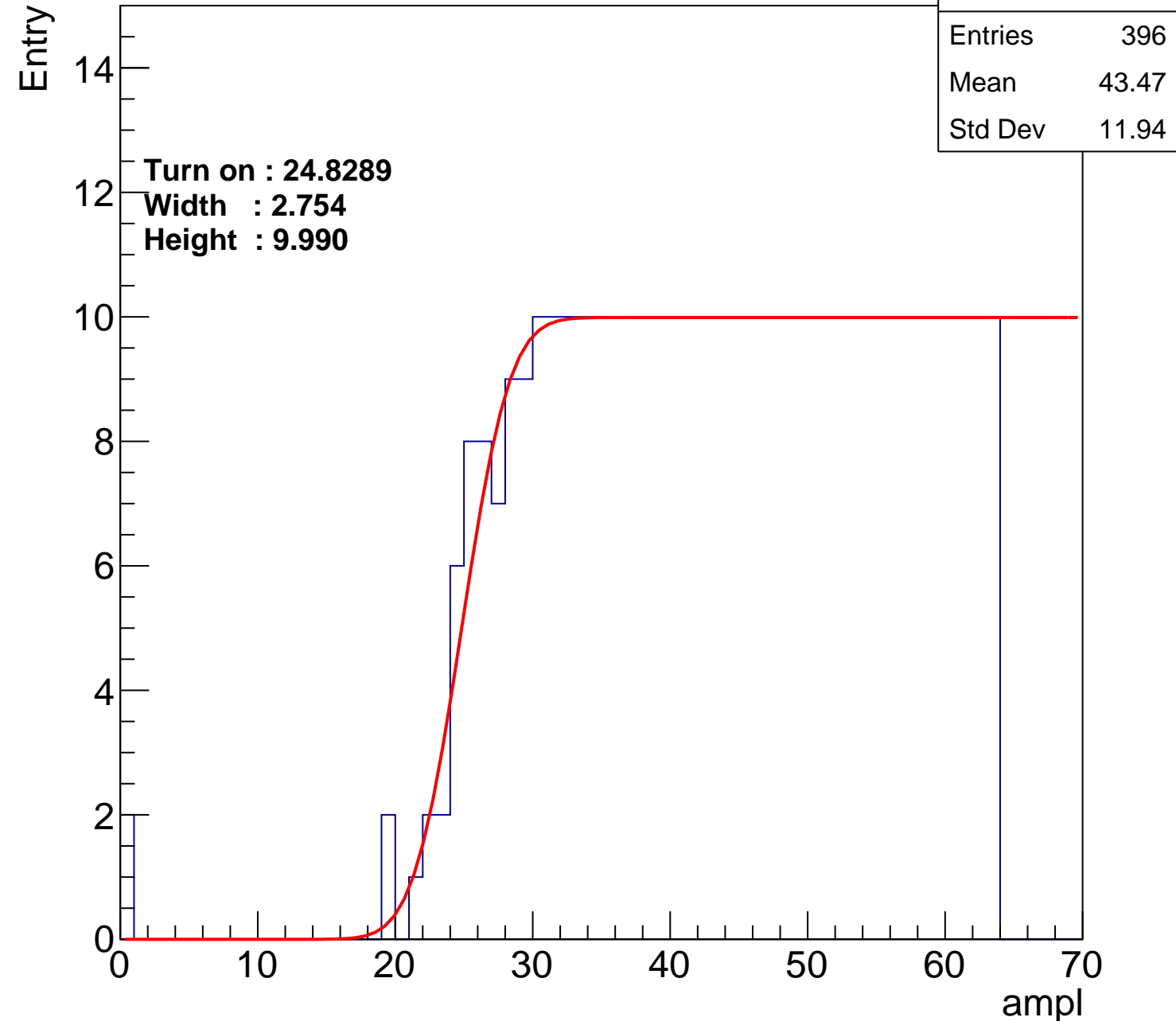
Width : 2.754

Height : 9.990

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U20-ch15

calib_packv5_042523_0143.root, FC#11, port A2

Entries	368
Mean	44.92
Std Dev	11.21

Turn on : 27.7491

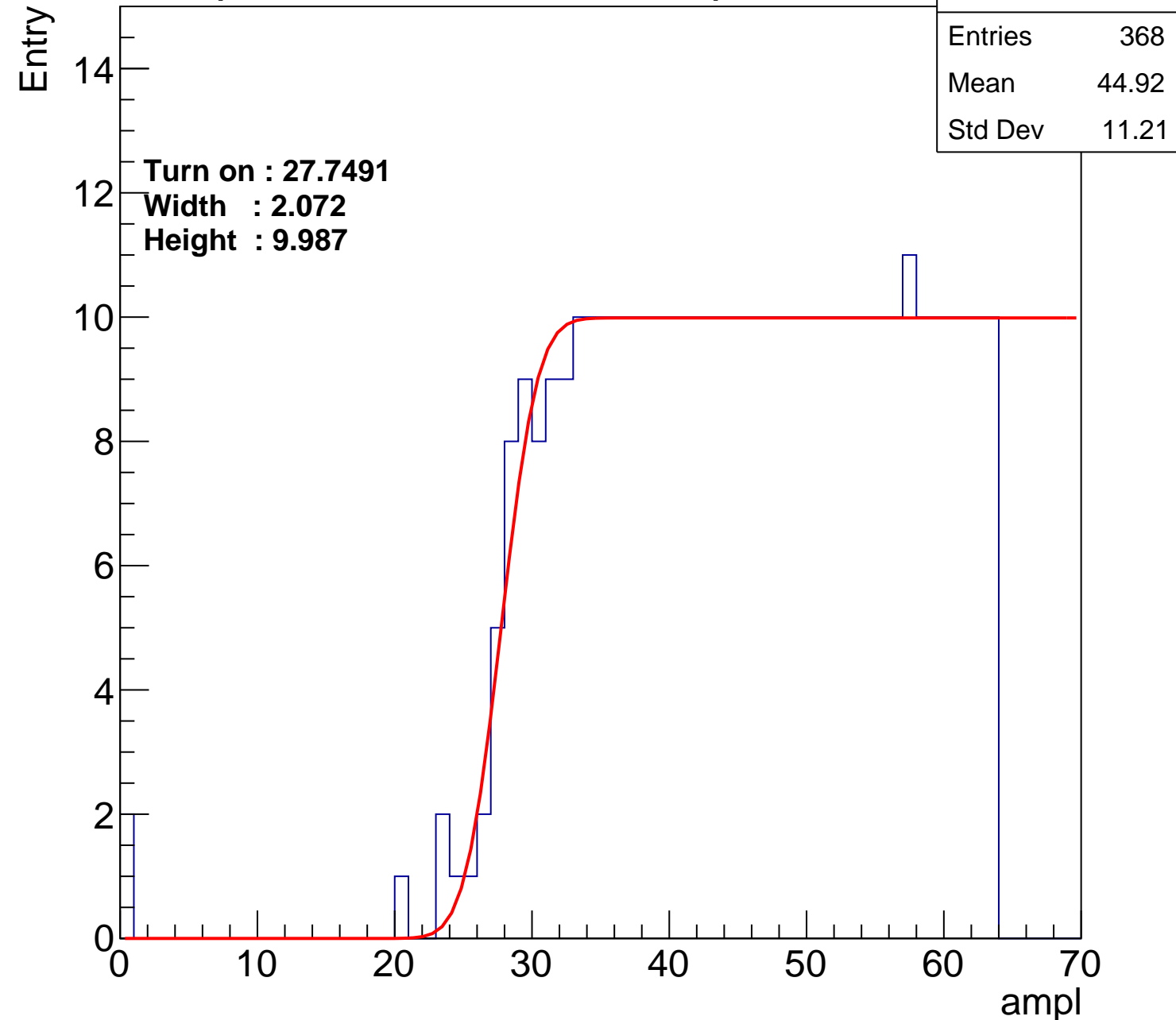
Width : 2.072

Height : 9.987

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U20-ch16

calib_packv5_042523_0143.root, FC#11, port A2

Entries	392
Mean	43.73
Std Dev	11.73

Turn on : 24.6794

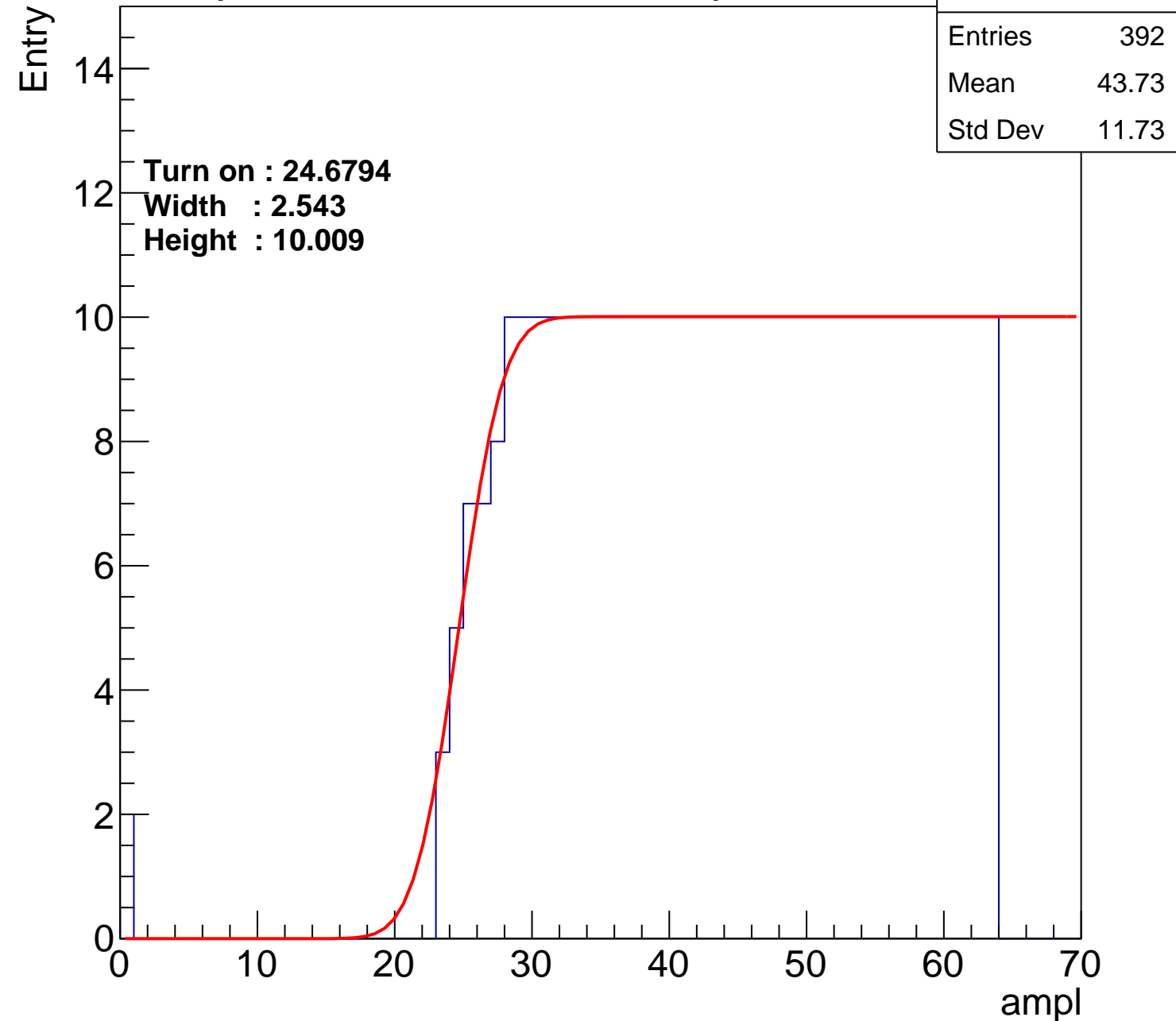
Width : 2.543

Height : 10.009

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U20-ch17

calib_packv5_042523_0143.root, FC#11, port A2

Entries	390
Mean	43.68
Std Dev	11.98

Turn on : 25.6115

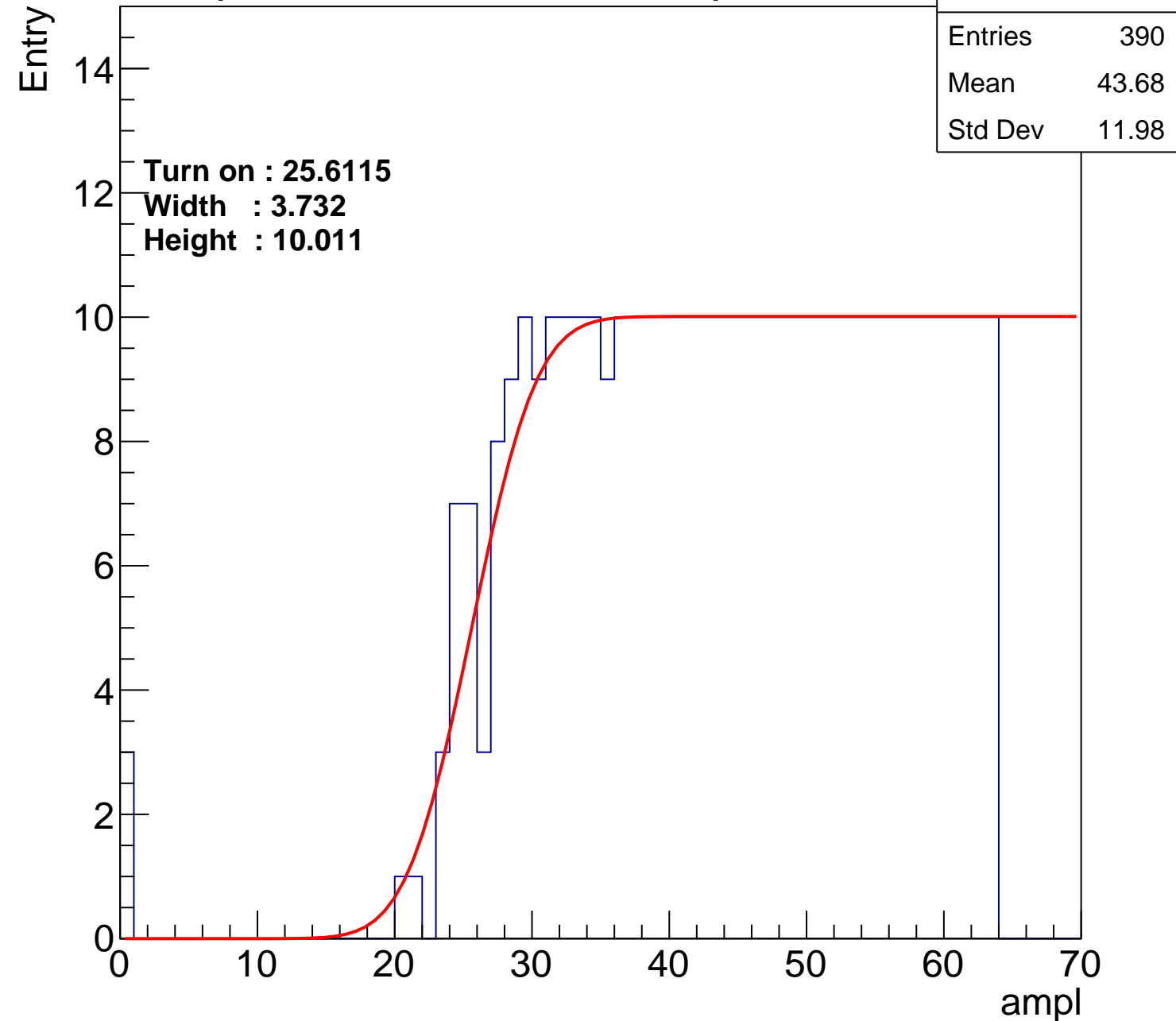
Width : 3.732

Height : 10.011

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U20-ch18

calib_packv5_042523_0143.root, FC#11, port A2

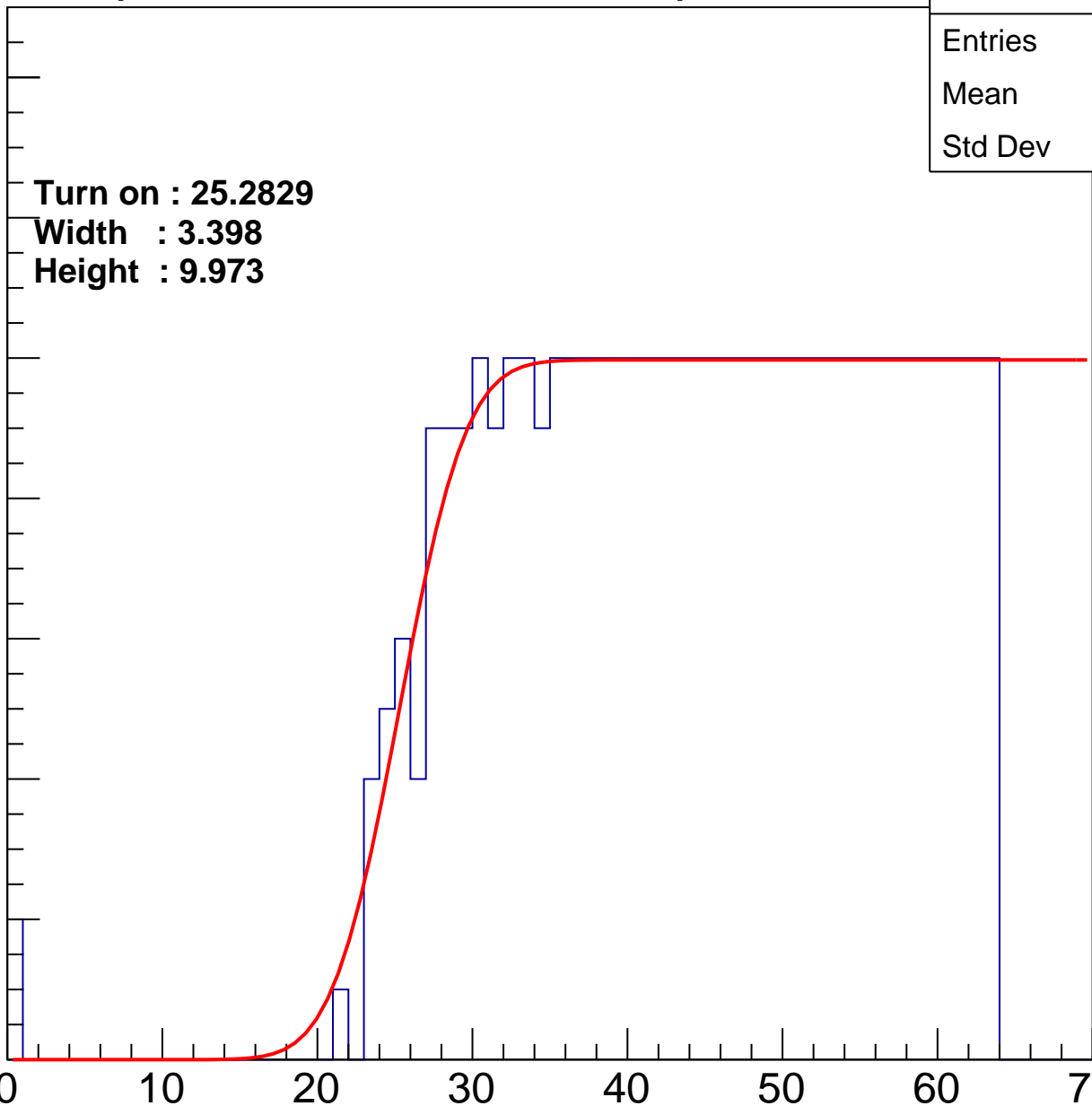
Entry

14
12
10
8
6
4
2
0

Turn on : 25.2829
Width : 3.398
Height : 9.973

Entries	387
Mean	43.9
Std Dev	11.72

ampl



B1L102S, U20-ch19

calib_packv5_042523_0143.root, FC#11, port A2

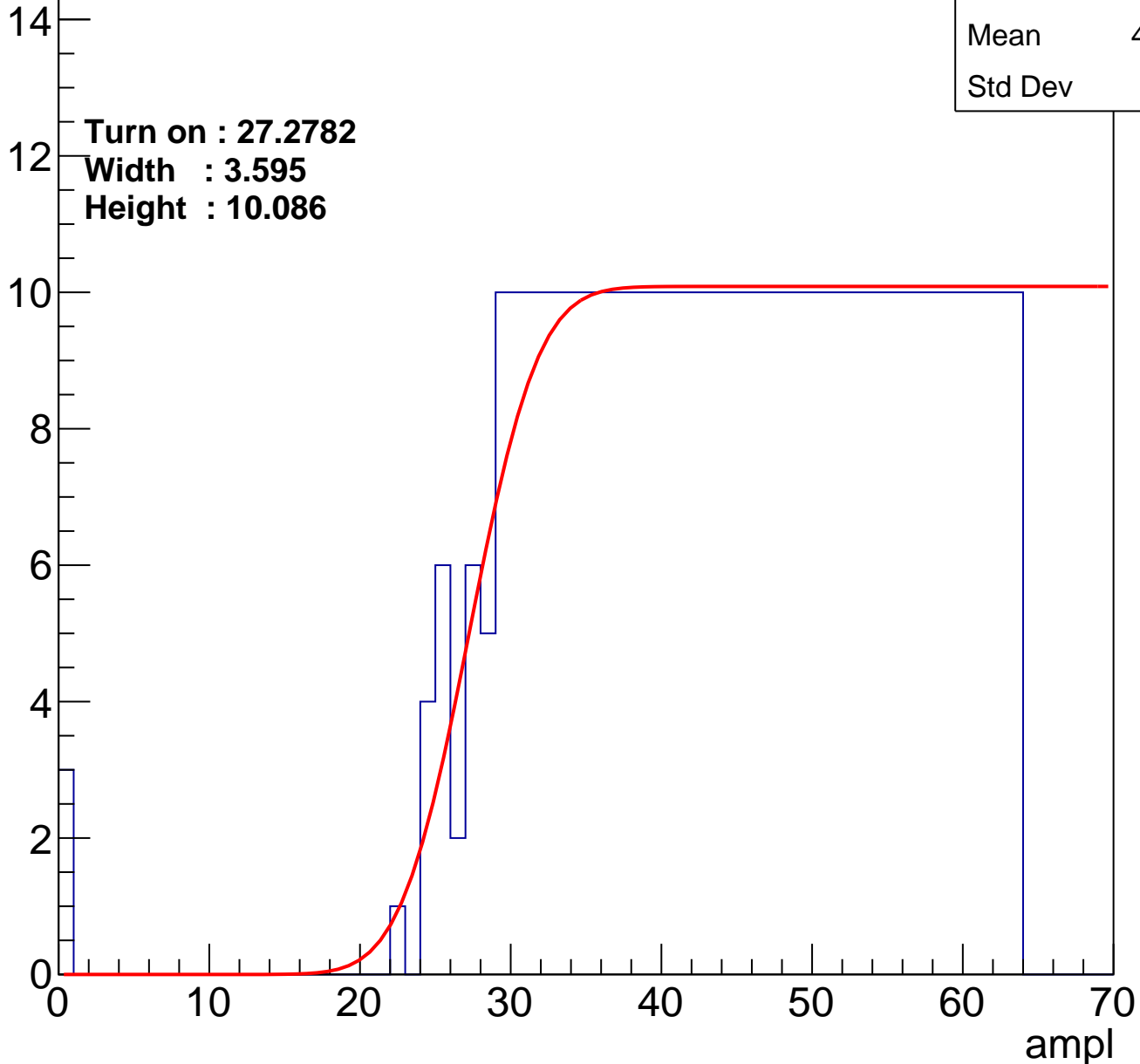
Entries	377
Mean	44.36
Std Dev	11.6

Turn on : 27.2782

Width : 3.595

Height : 10.086

Entry



B1L102S, U20-ch20

calib_packv5_042523_0143.root, FC#11, port A2

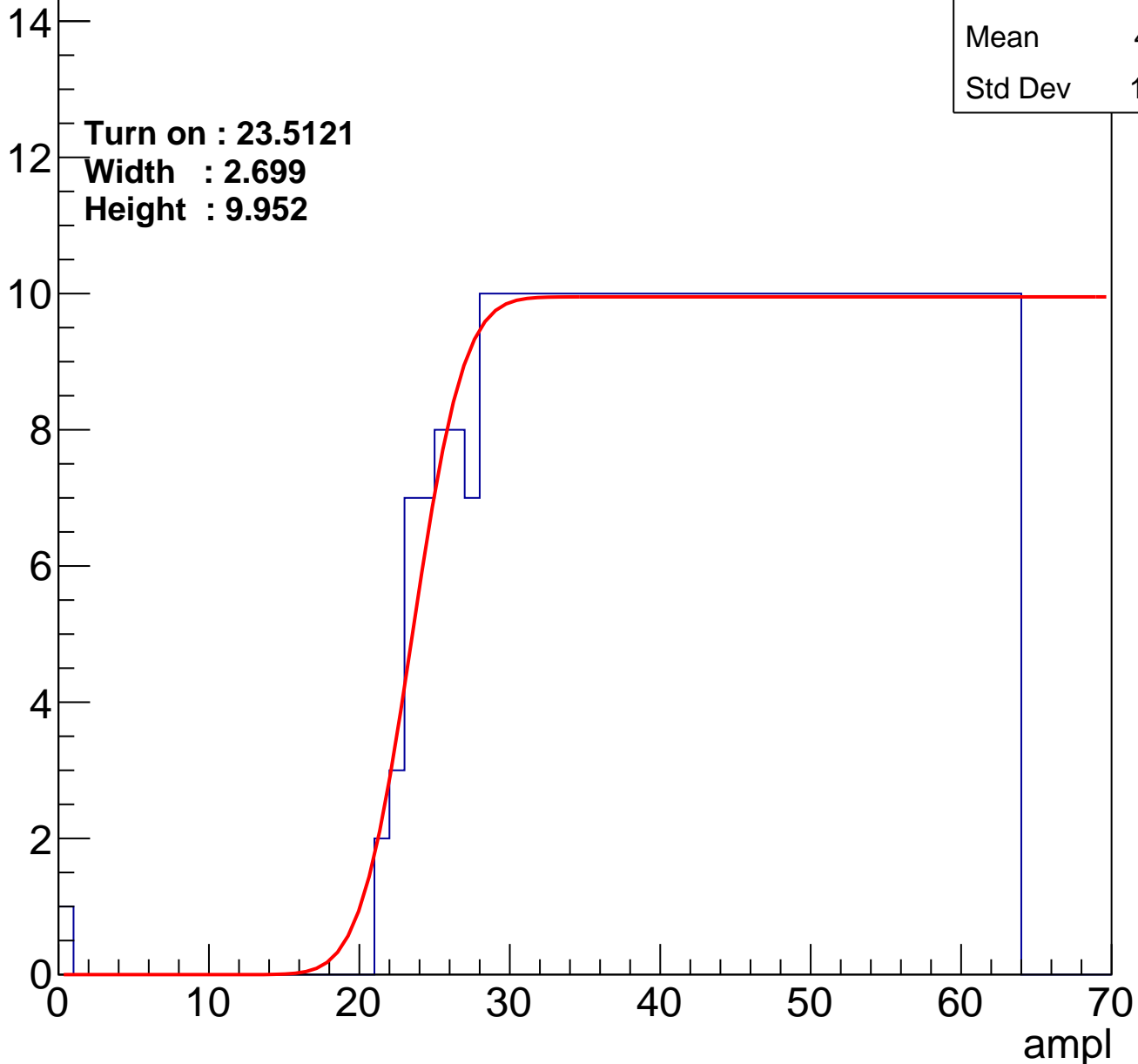
Entries	403
Mean	43.21
Std Dev	11.92

Turn on : 23.5121

Width : 2.699

Height : 9.952

Entry



B1L102S, U20-ch21

calib_packv5_042523_0143.root, FC#11, port A2

Entries	389
Mean	43.77
Std Dev	11.9

Turn on : 25.7447

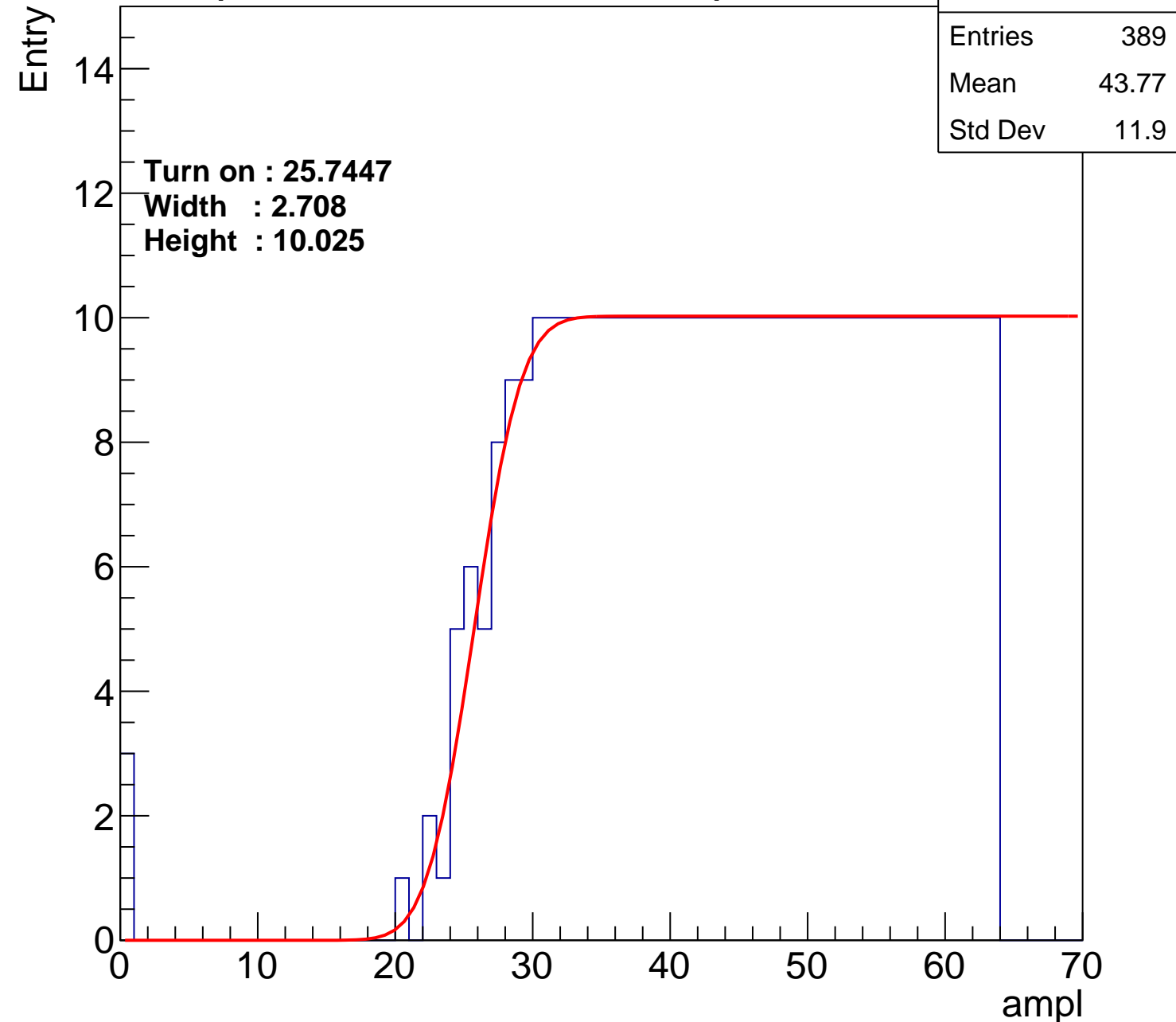
Width : 2.708

Height : 10.025

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U20-ch22

calib_packv5_042523_0143.root, FC#11, port A2

Entries	389
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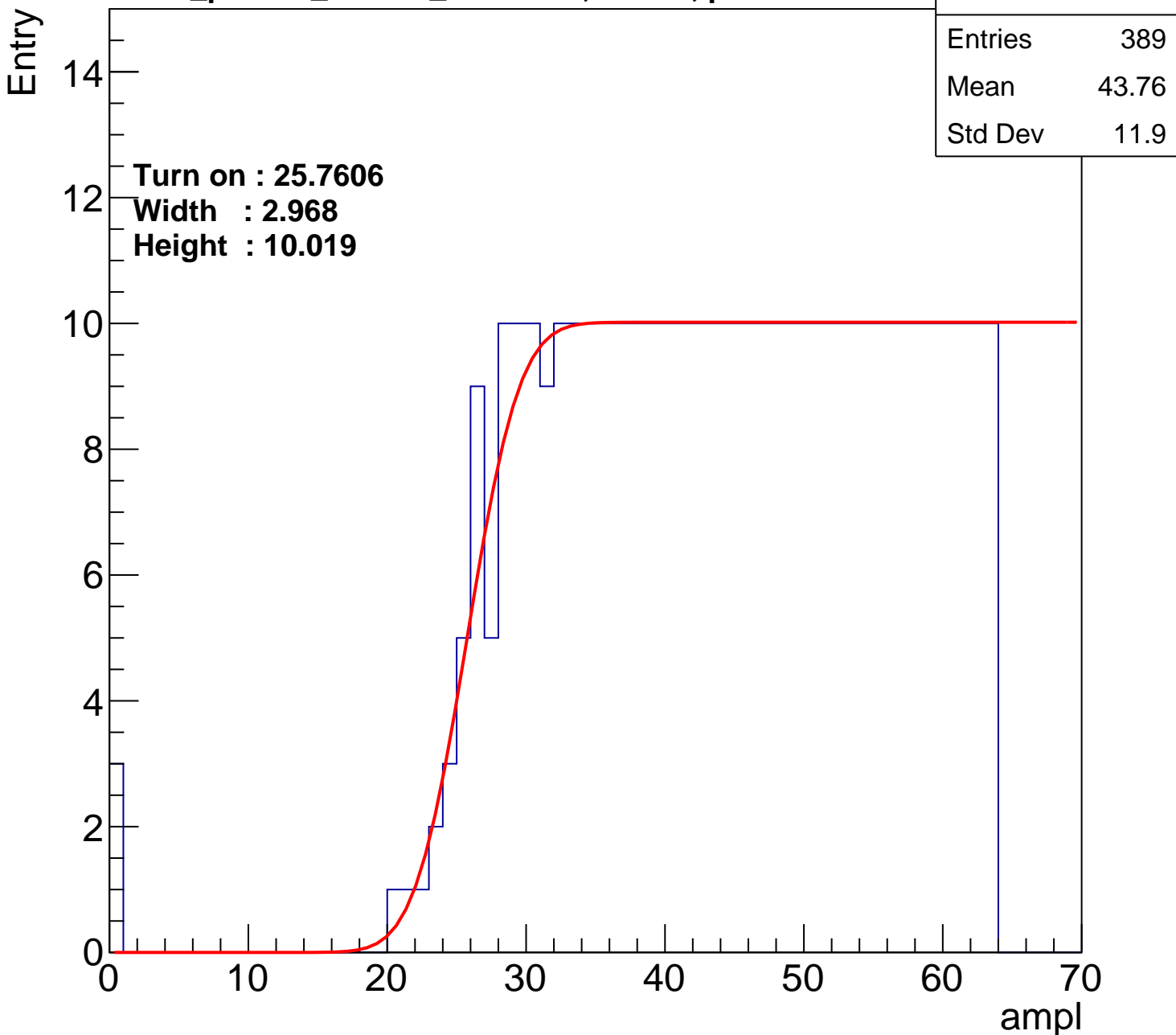
Mean	43.76
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Std Dev	11.9
---------	------

Turn on : 25.7606

Width : 2.968

Height : 10.019



B1L102S, U20-ch23

calib_packv5_042523_0143.root, FC#11, port A2

Entries	380
Mean	44.25
Std Dev	11.53

Turn on : 26.4149

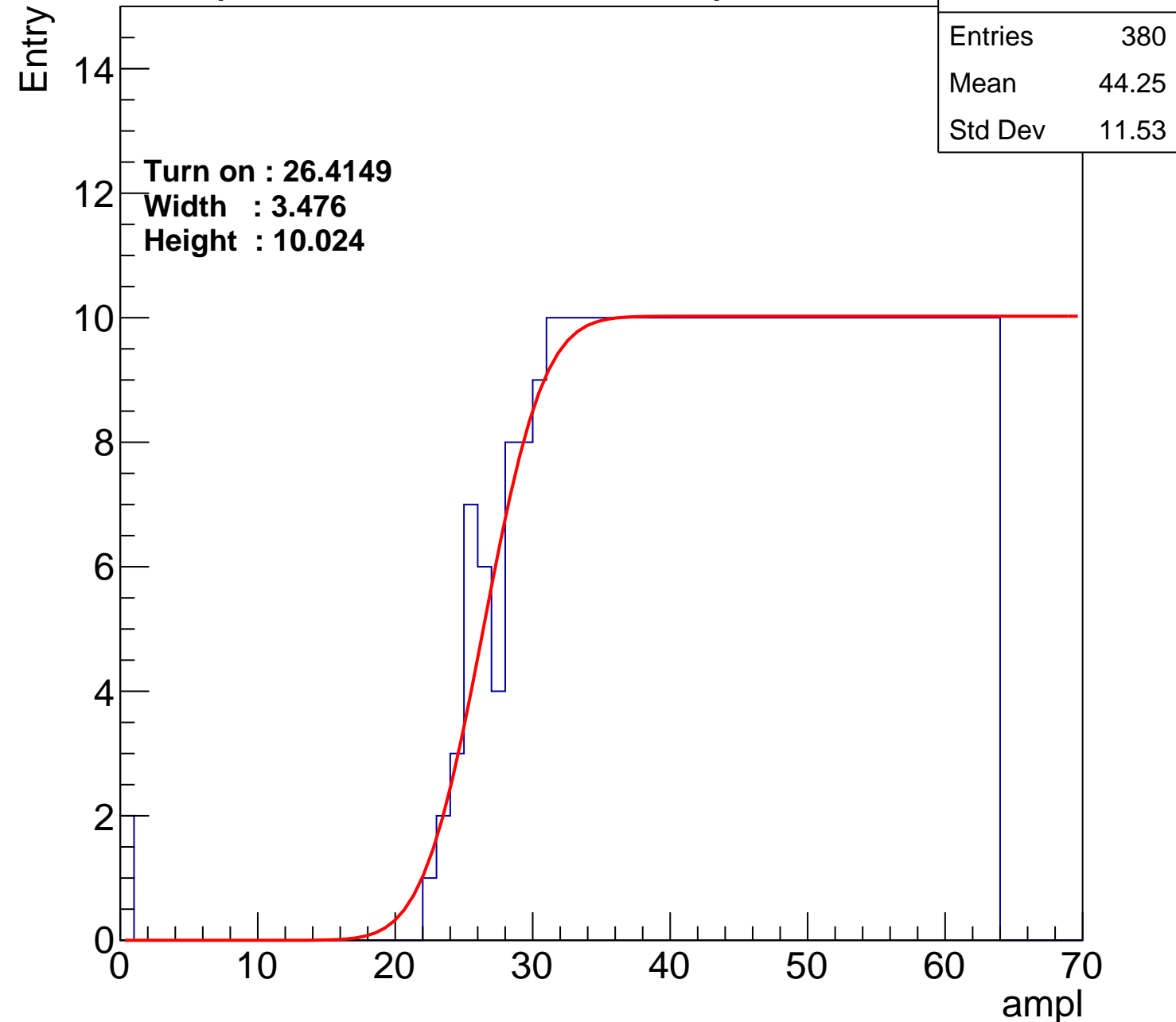
Width : 3.476

Height : 10.024

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U20-ch24

calib_packv5_042523_0143.root, FC#11, port A2

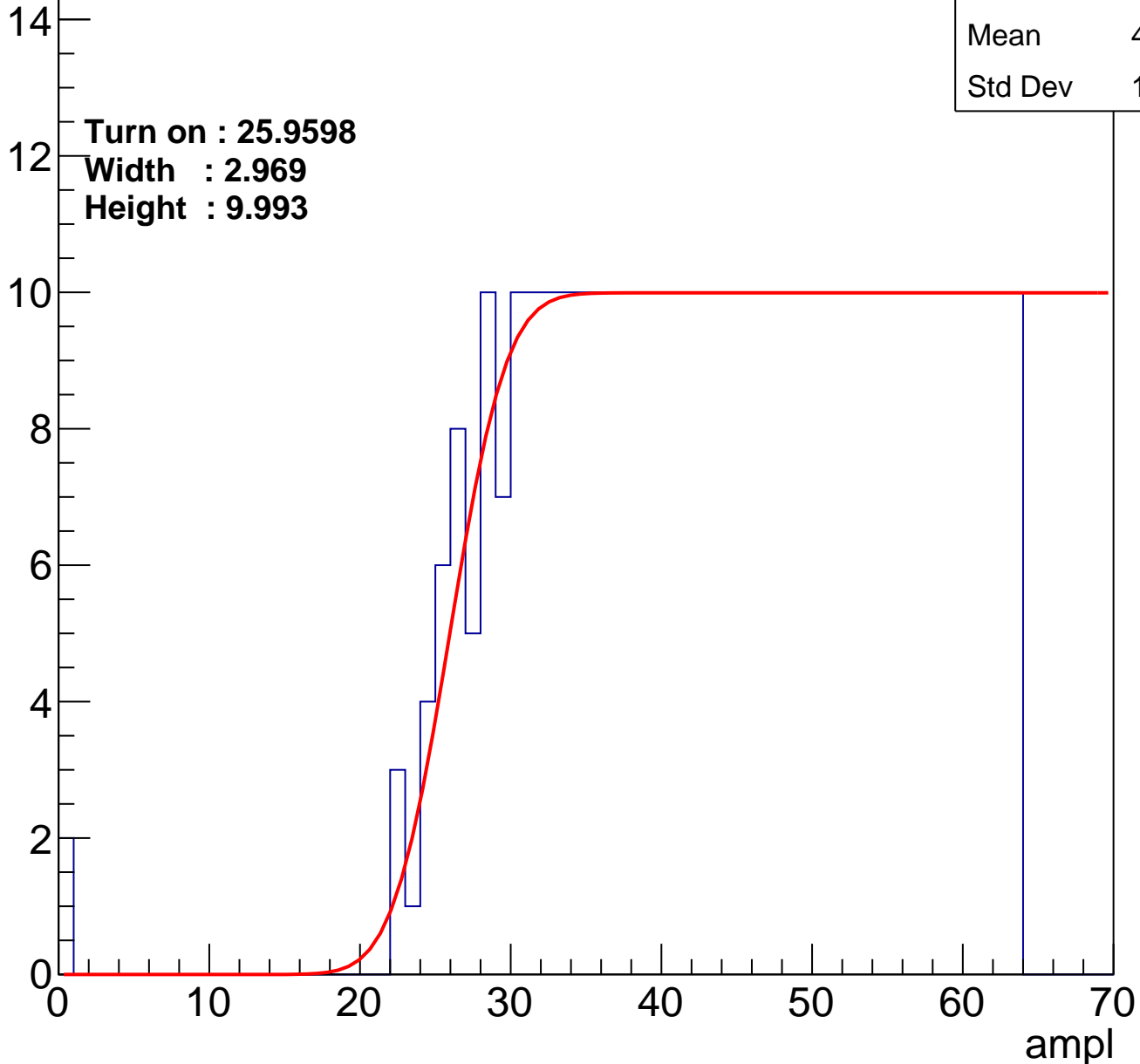
Entries	386
Mean	43.97
Std Dev	11.67

Turn on : 25.9598

Width : 2.969

Height : 9.993

Entry



B1L102S, U20-ch25

calib_packv5_042523_0143.root, FC#11, port A2

Entries	386
Mean	43.9
Std Dev	11.85

Turn on : 26.1118

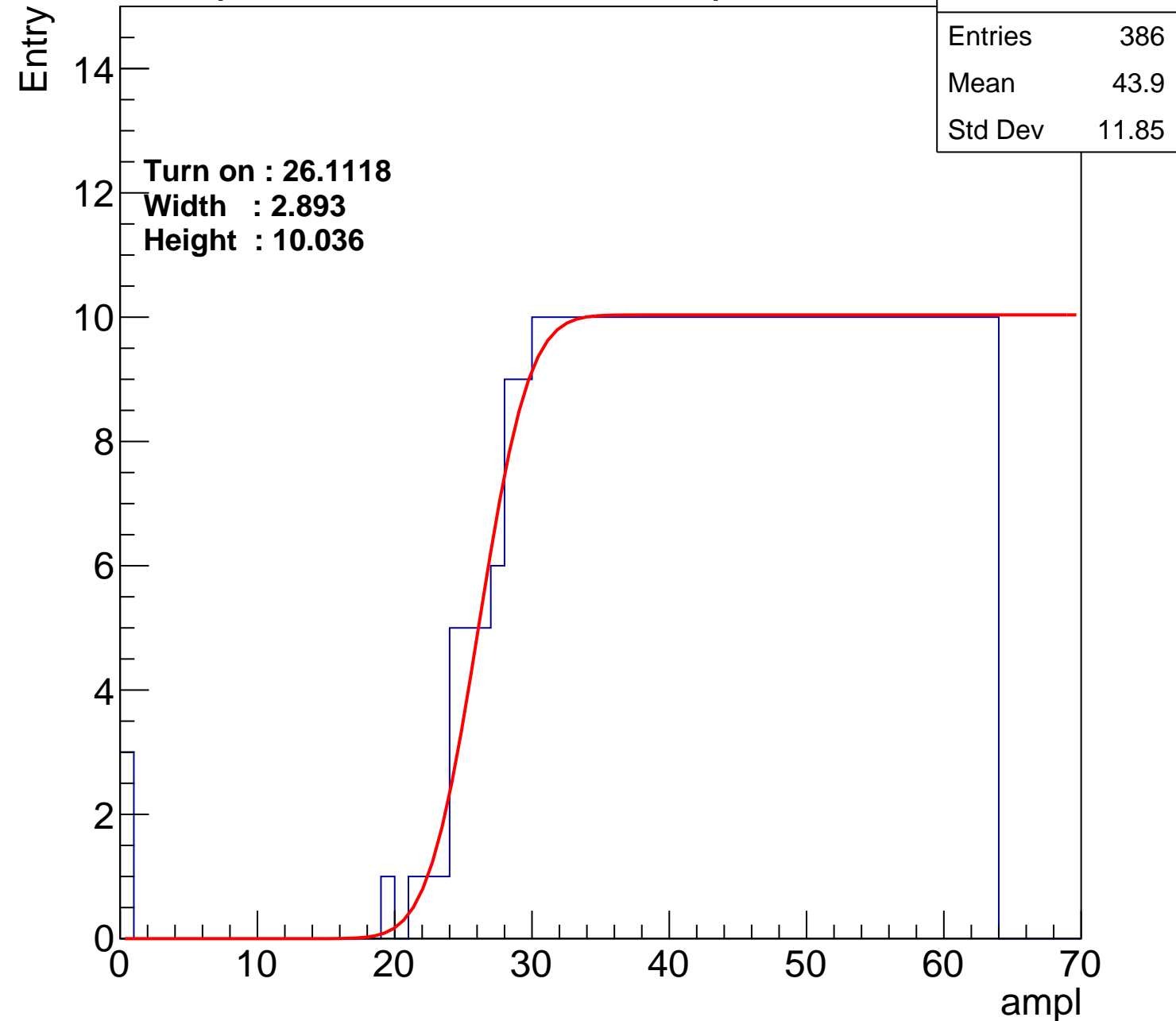
Width : 2.893

Height : 10.036

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U20-ch26

calib_packv5_042523_0143.root, FC#11, port A2

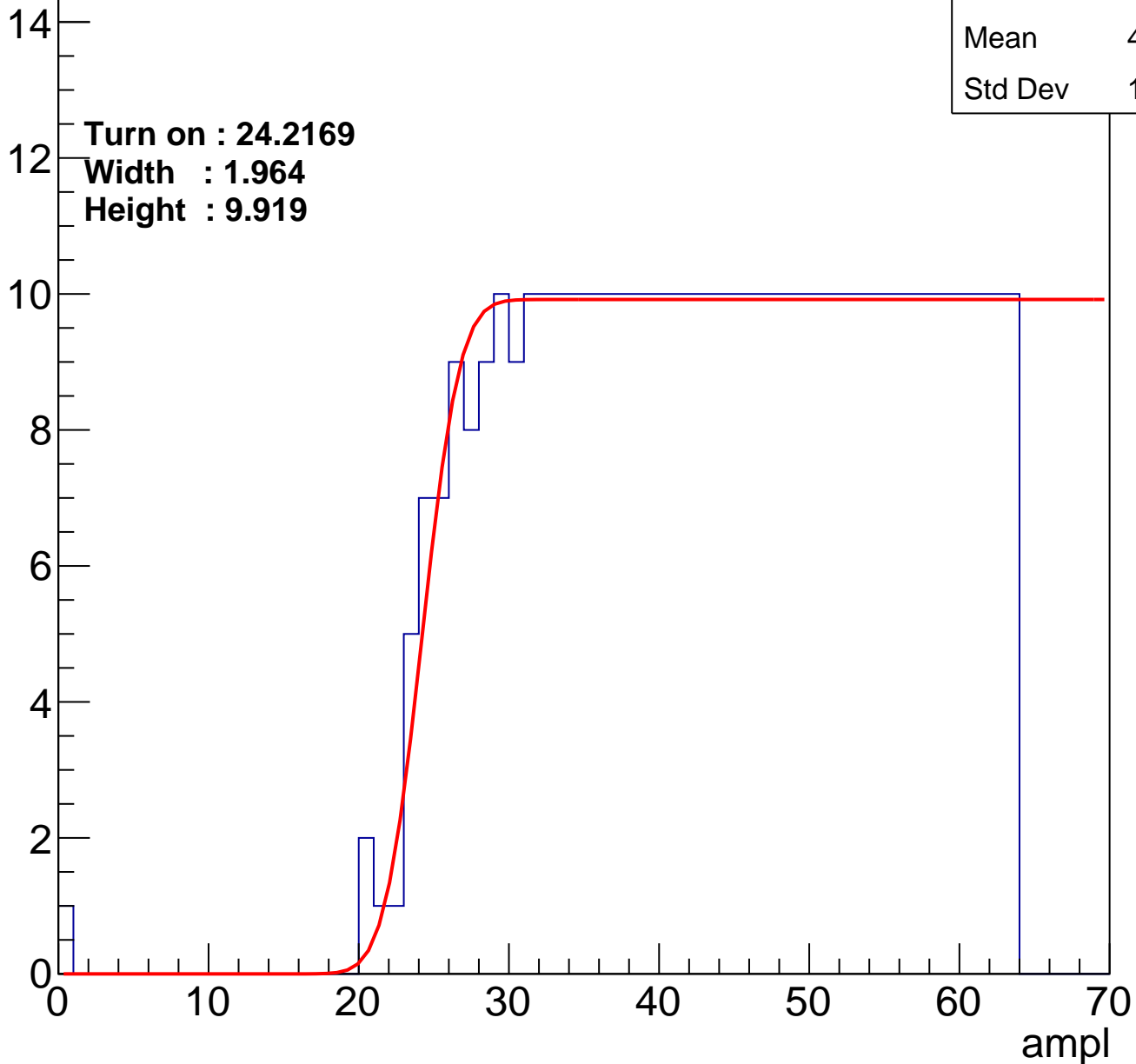
Entry

Entries	399
Mean	43.39
Std Dev	11.84

Turn on : 24.2169

Width : 1.964

Height : 9.919



B1L102S, U20-ch27

calib_packv5_042523_0143.root, FC#11, port A2

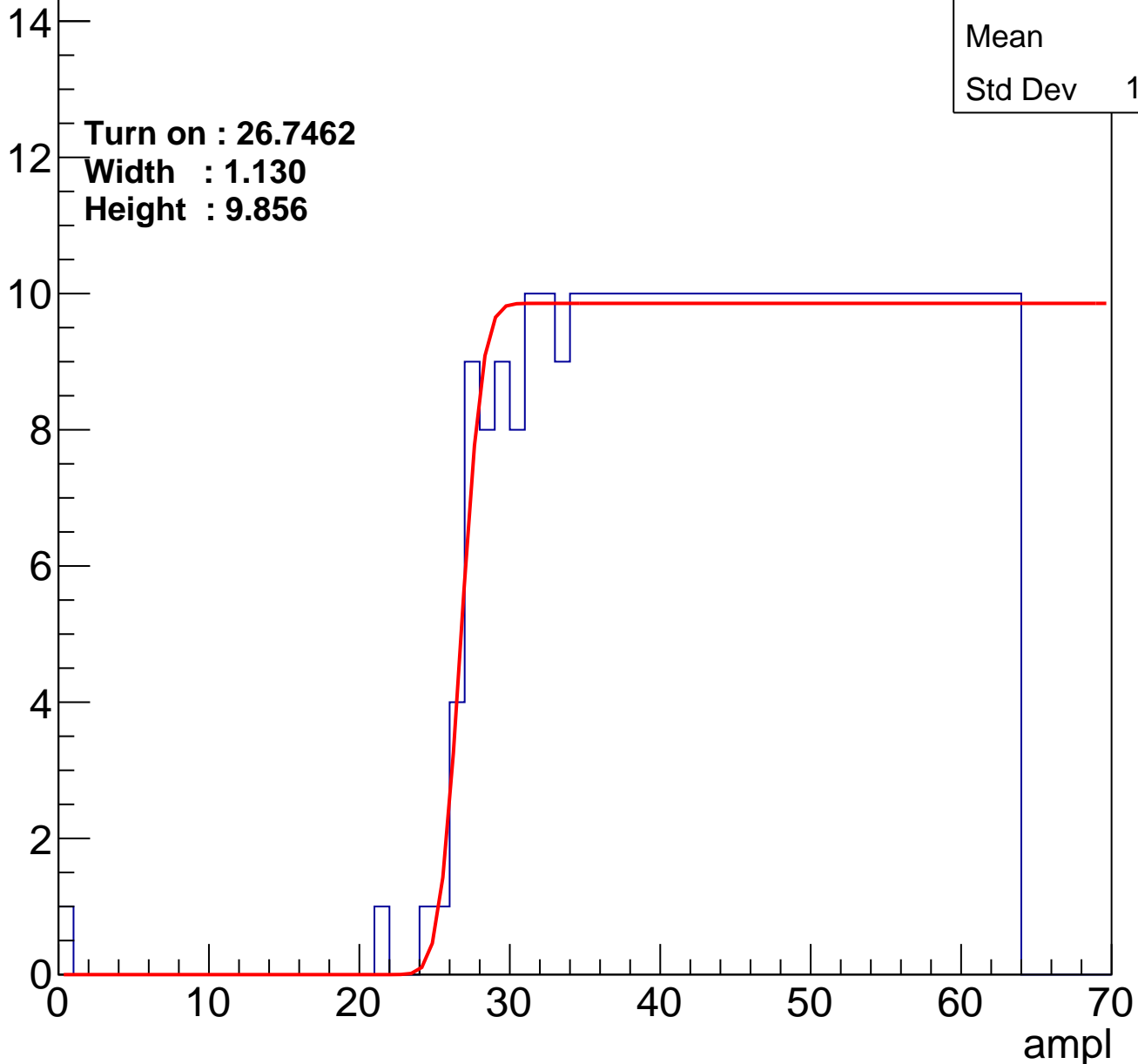
Entries	371
Mean	44.8
Std Dev	11.05

Turn on : 26.7462

Width : 1.130

Height : 9.856

Entry



B1L102S, U20-ch28

calib_packv5_042523_0143.root, FC#11, port A2

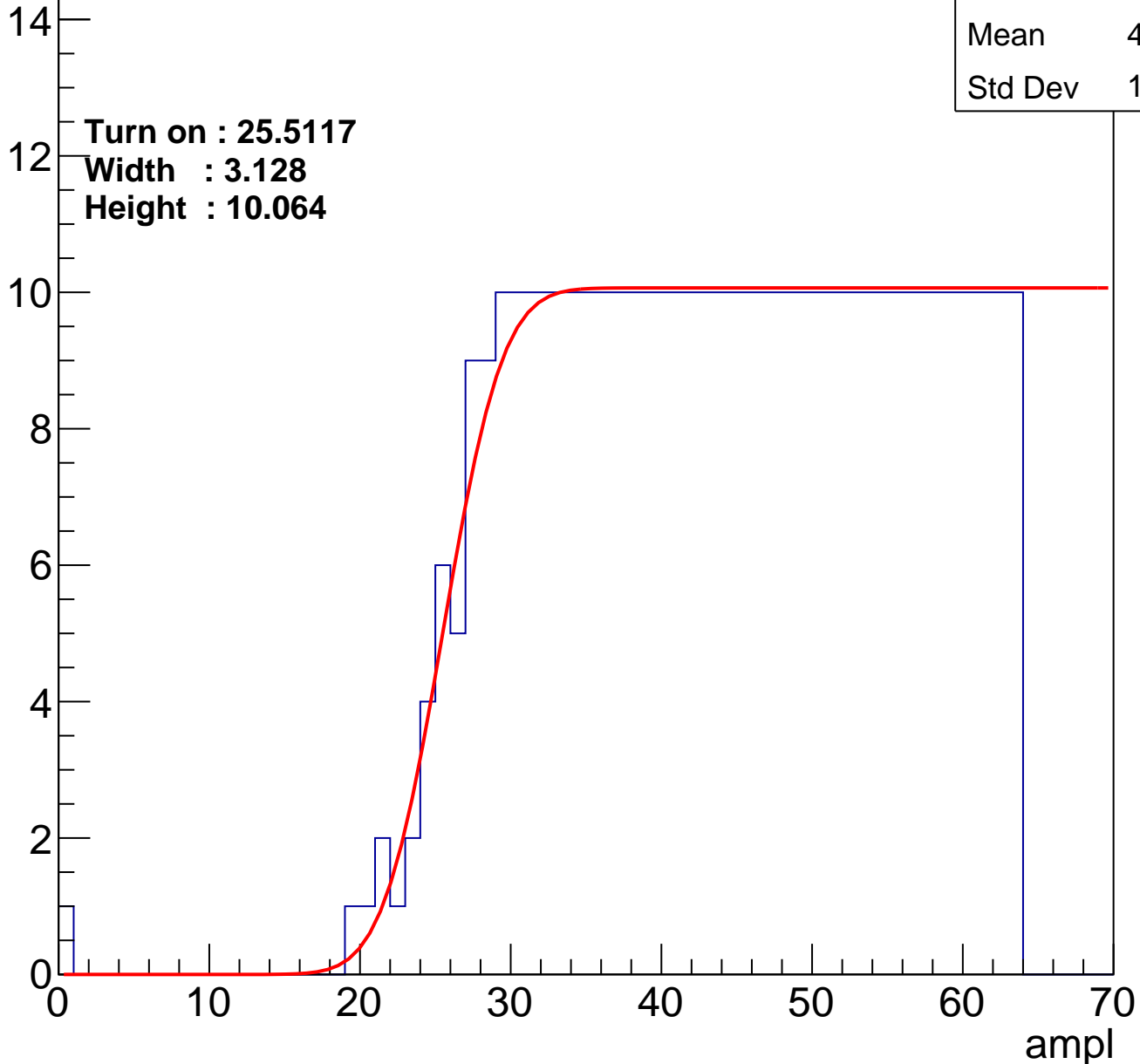
Entries	391
Mean	43.79
Std Dev	11.64

Turn on : 25.5117

Width : 3.128

Height : 10.064

Entry



B1L102S, U20-ch29

calib_packv5_042523_0143.root, FC#11, port A2

Entries	373
Mean	44.45
Std Dev	11.82

Turn on : 27.1009

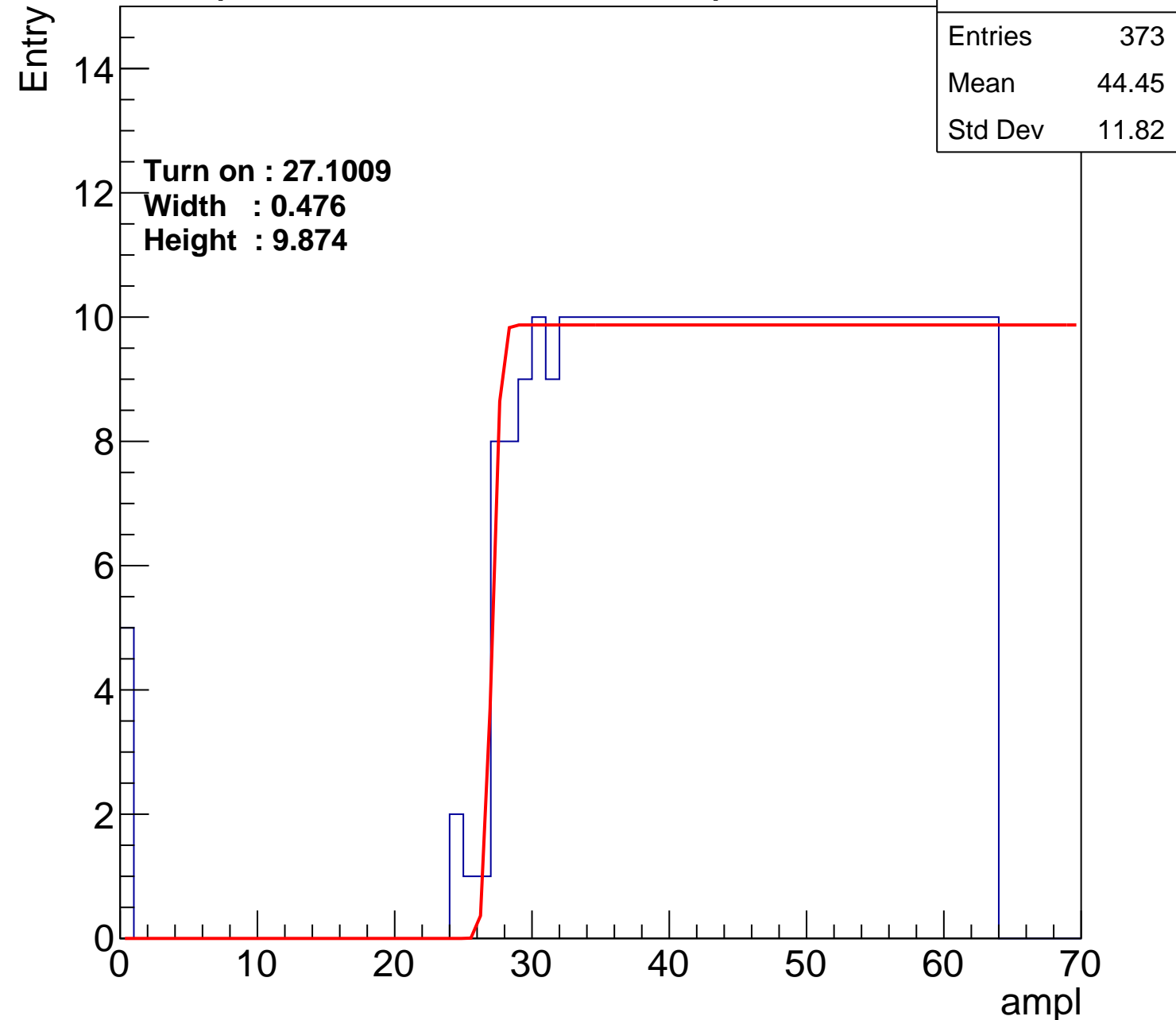
Width : 0.476

Height : 9.874

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U20-ch30

calib_packv5_042523_0143.root, FC#11, port A2

Entries	384
Mean	43.93
Std Dev	11.97

Turn on : 26.1964

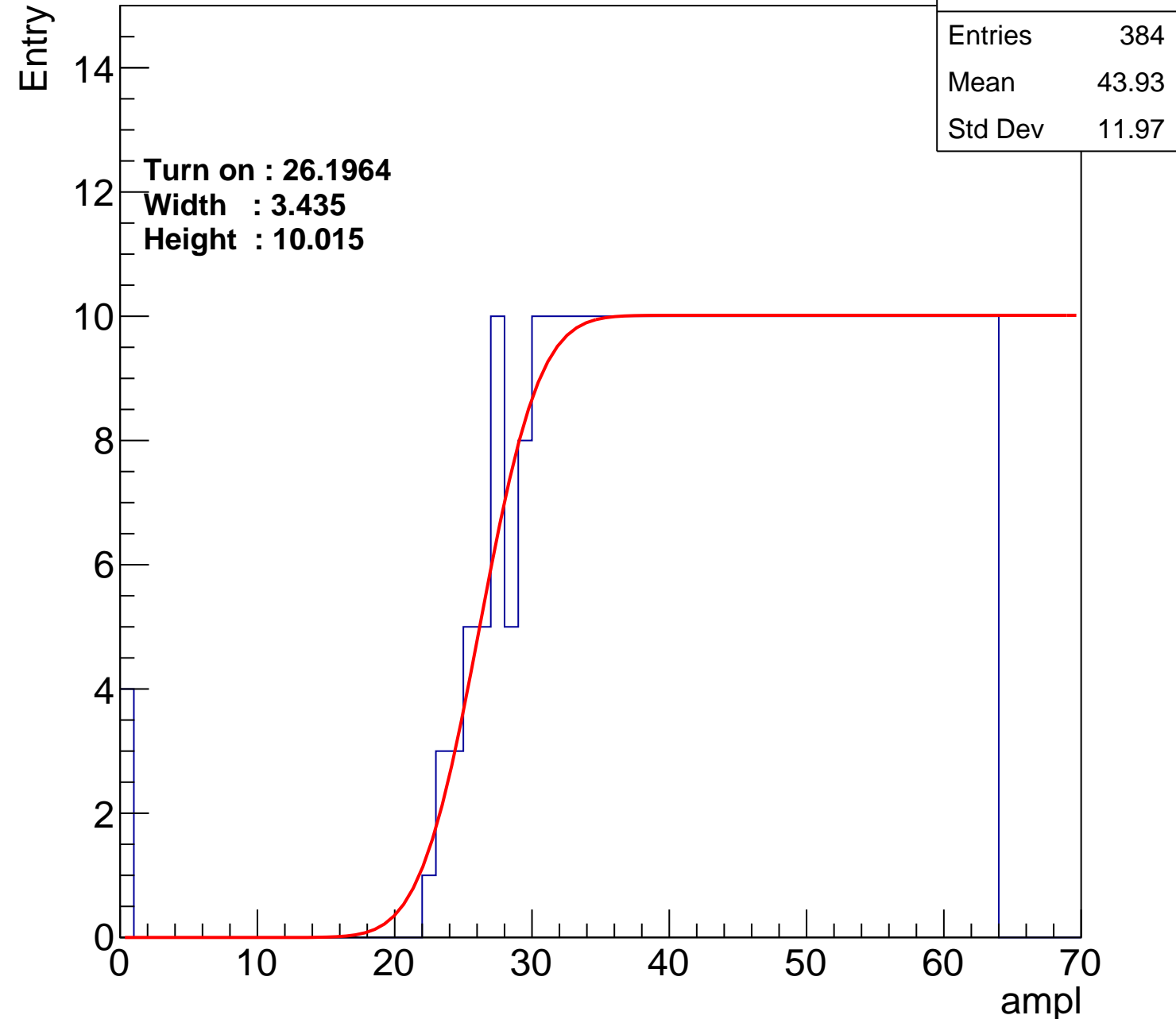
Width : 3.435

Height : 10.015

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U20-ch31

calib_packv5_042523_0143.root, FC#11, port A2

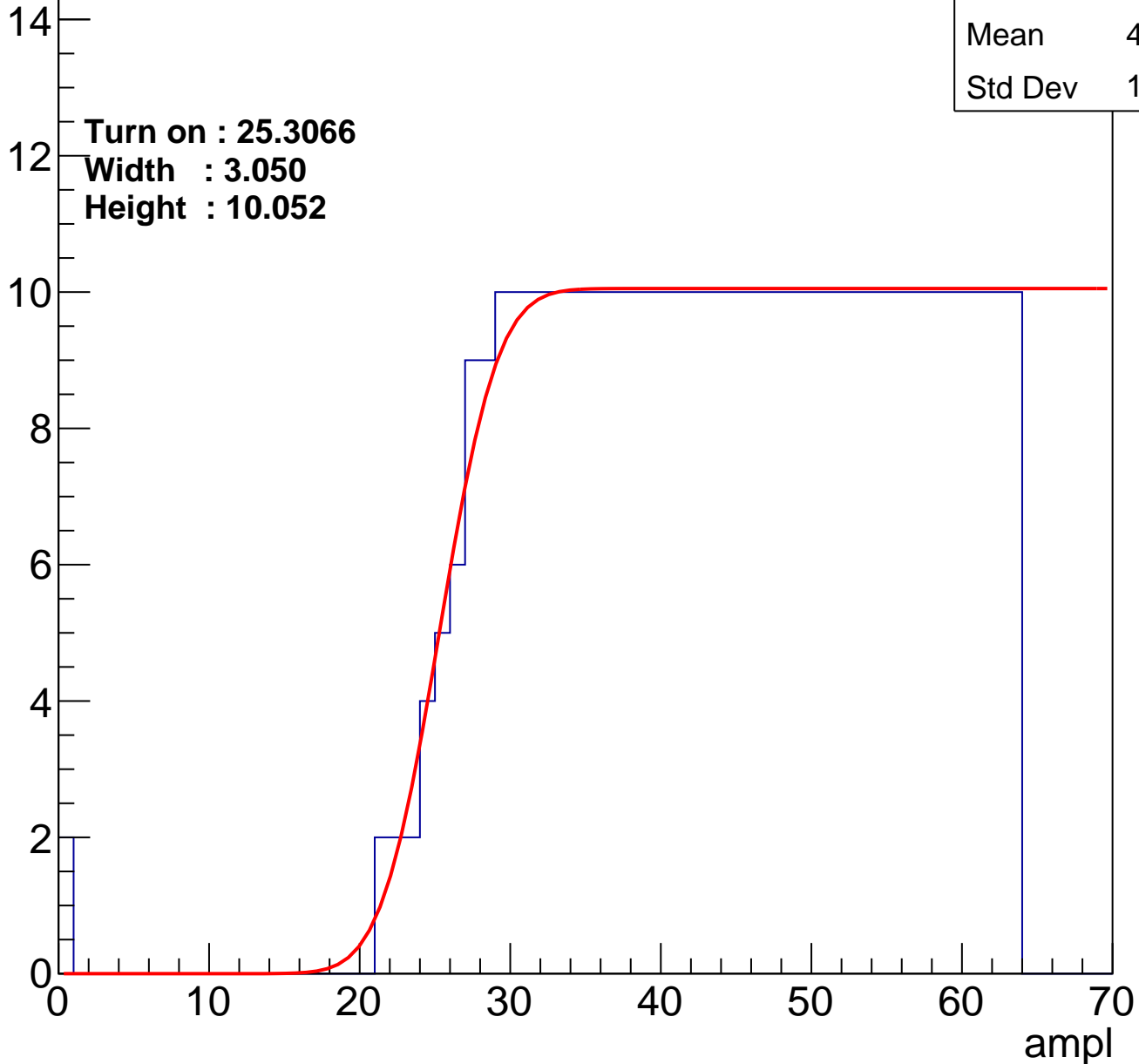
Entries	391
Mean	43.74
Std Dev	11.76

Turn on : 25.3066

Width : 3.050

Height : 10.052

Entry



B1L102S, U20-ch32

calib_packv5_042523_0143.root, FC#11, port A2

Entries	396
Mean	43.54
Std Dev	11.75

Turn on : 24.4452

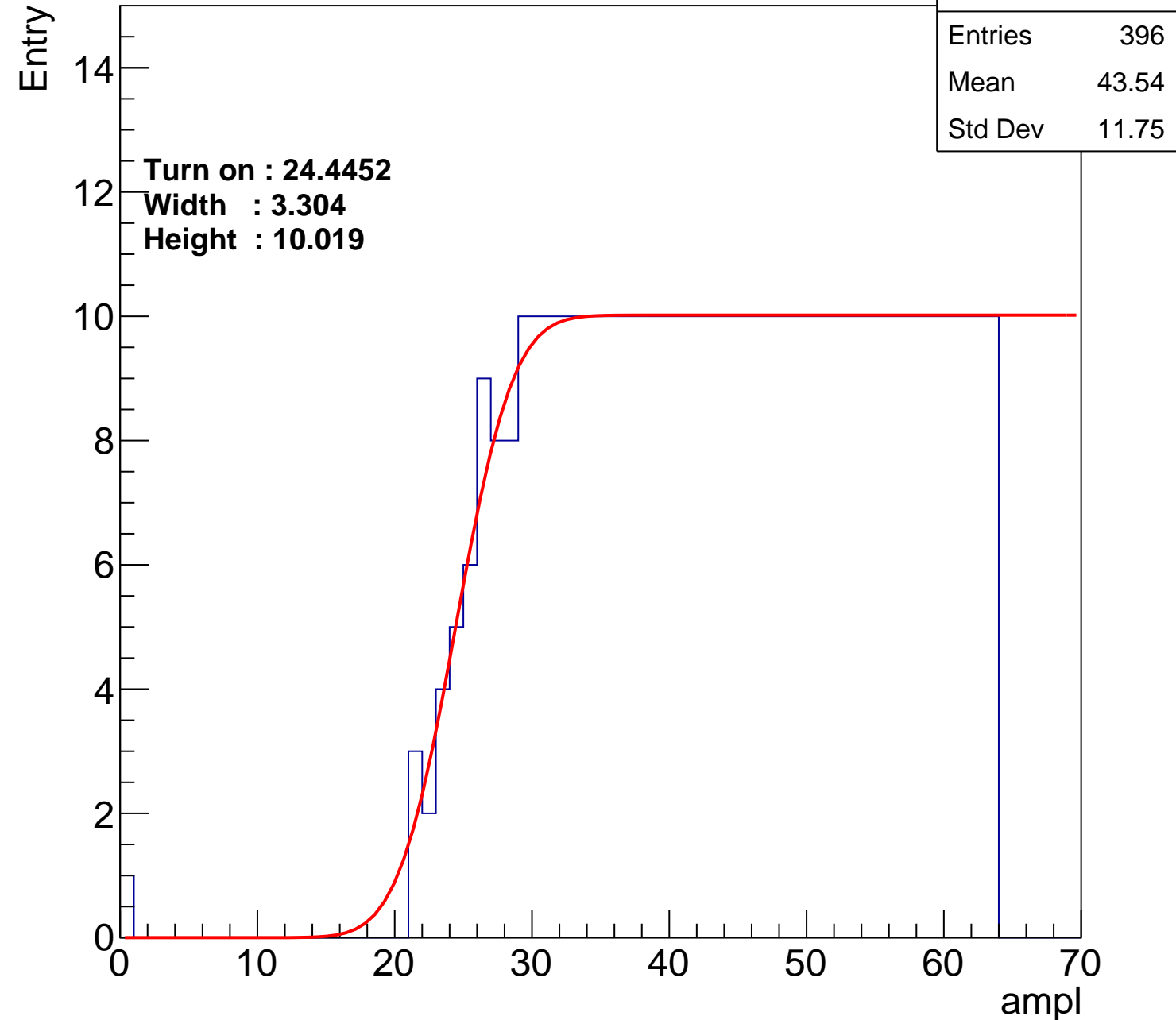
Width : 3.304

Height : 10.019

Entry

14
12
10
8
6
4
2
0

ampl

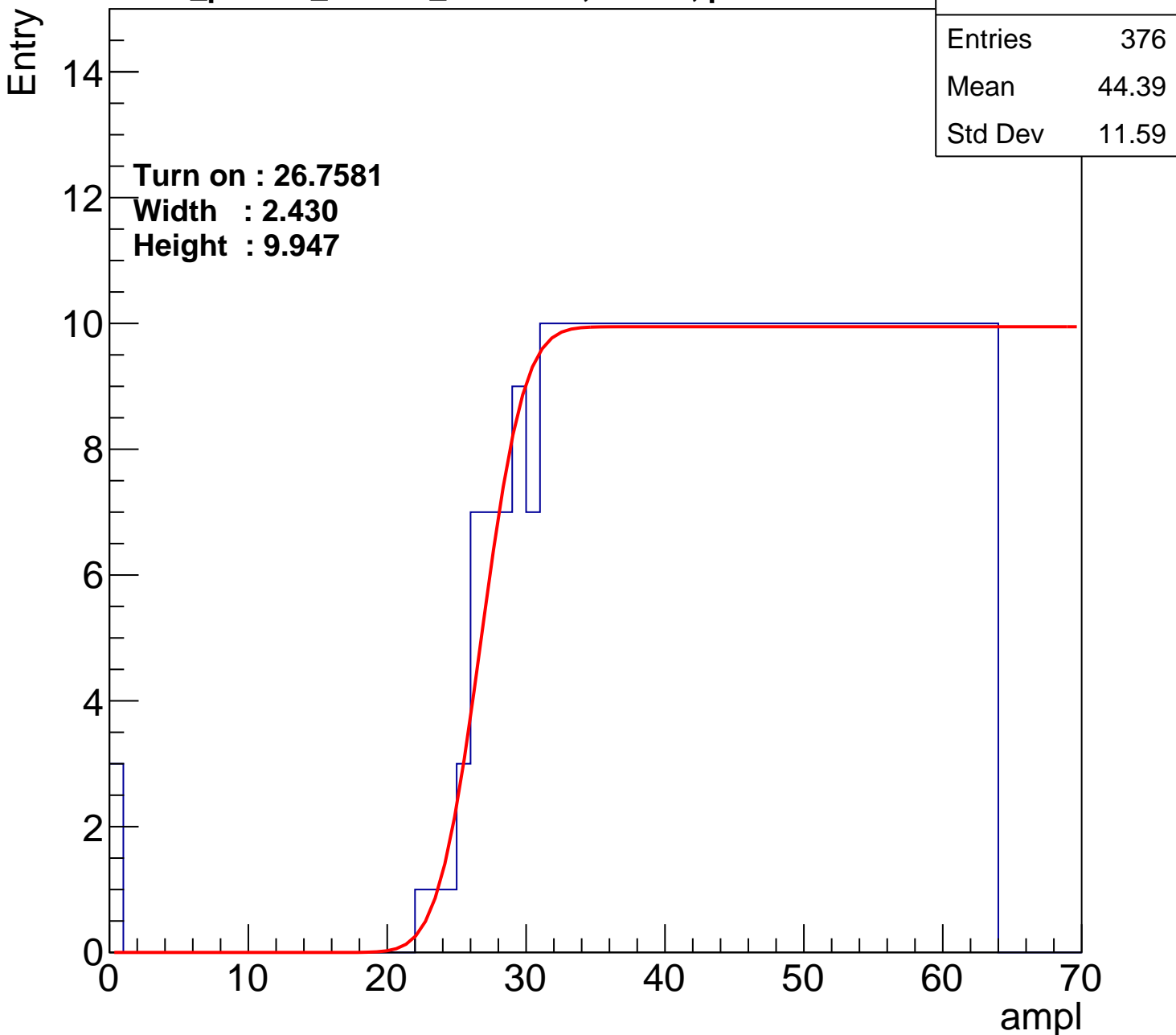


calib_packv5_042523_0143.root, FC#11, port A2

calib_packv5_042523_0143.root, FC#11, port A2

Entries	376
Mean	44.39
Std Dev	11.59

Height : 9.947



B1L102S, U20-ch34

calib_packv5_042523_0143.root, FC#11, port A2

Entries	375
Mean	44.58
Std Dev	11.19

Turn on : 26.6479

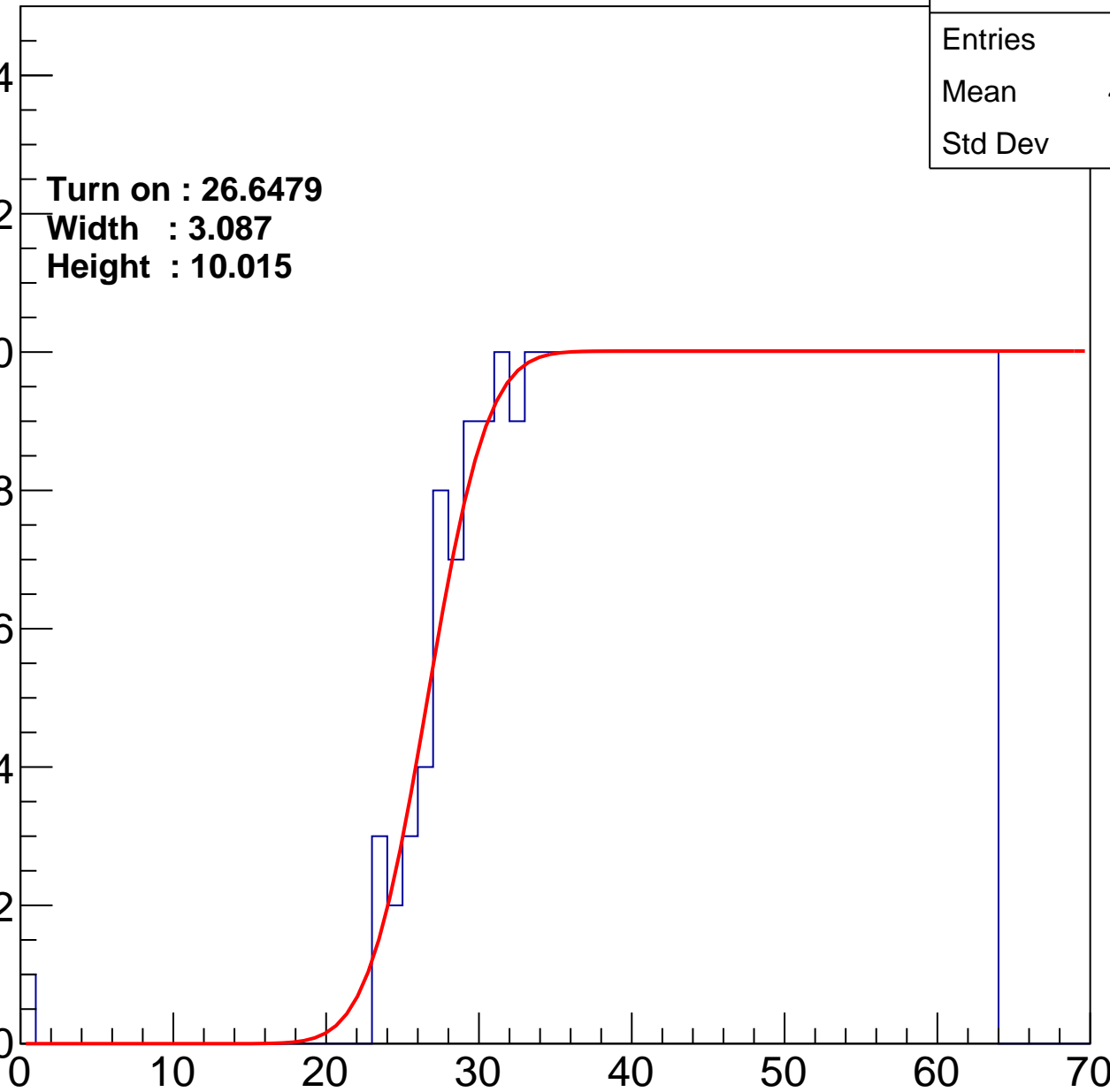
Width : 3.087

Height : 10.015

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U20-ch35

calib_packv5_042523_0143.root, FC#11, port A2

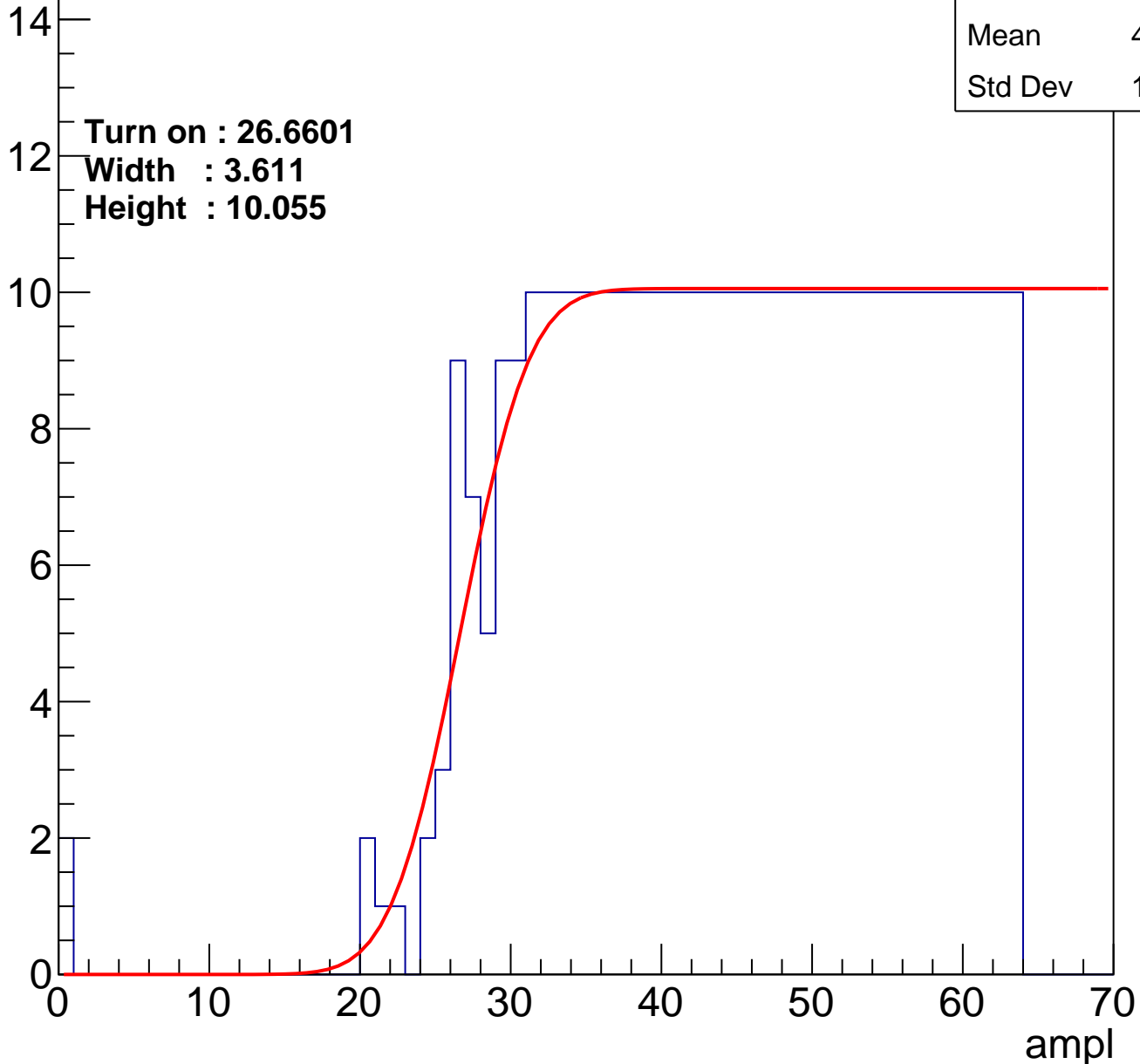
Entries	380
Mean	44.24
Std Dev	11.56

Turn on : 26.6601

Width : 3.611

Height : 10.055

Entry



B1L102S, U20-ch36

calib_packv5_042523_0143.root, FC#11, port A2

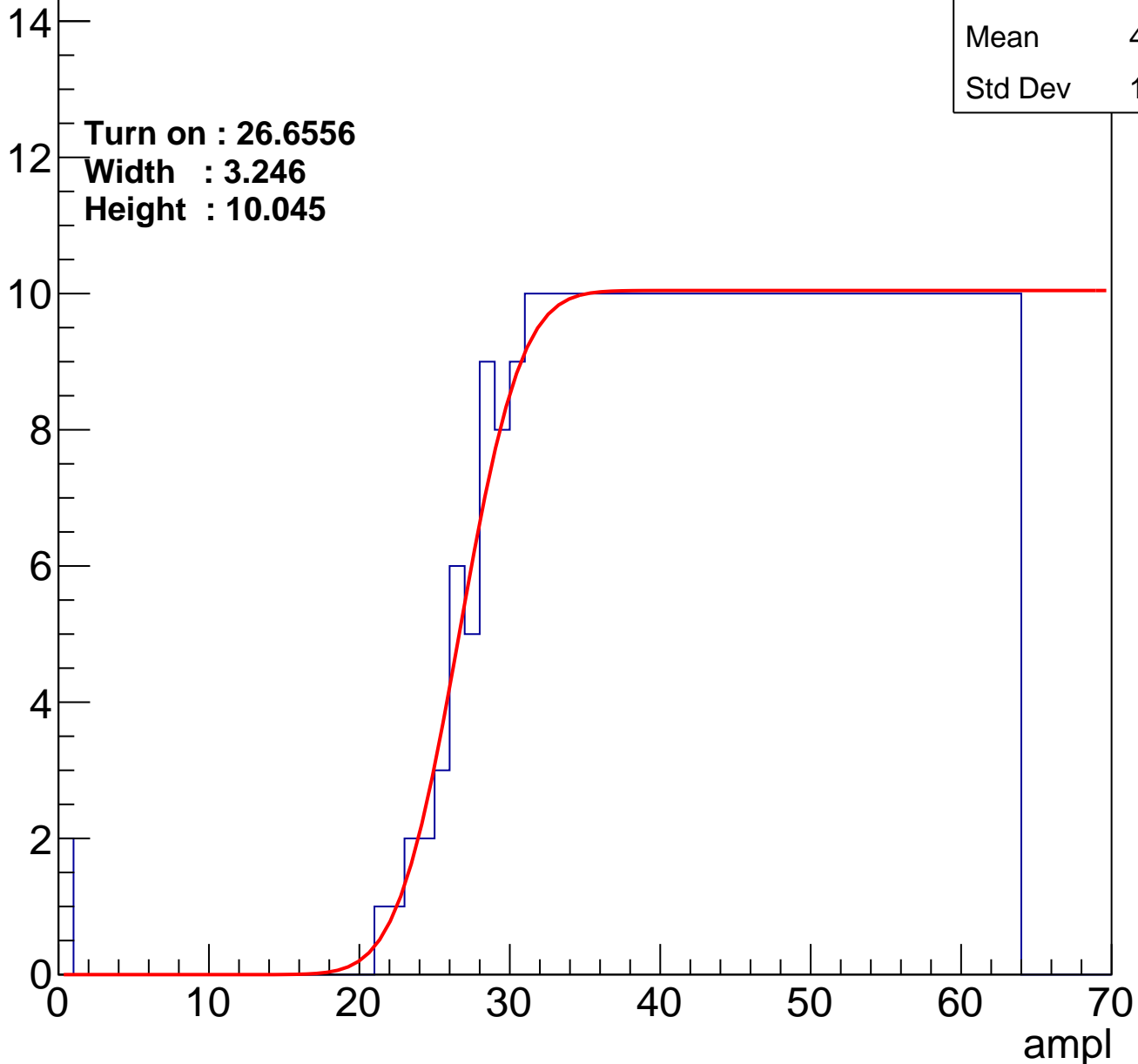
Entries	378
Mean	44.36
Std Dev	11.47

Turn on : 26.6556

Width : 3.246

Height : 10.045

Entry



B1L102S, U20-ch37

calib_packv5_042523_0143.root, FC#11, port A2

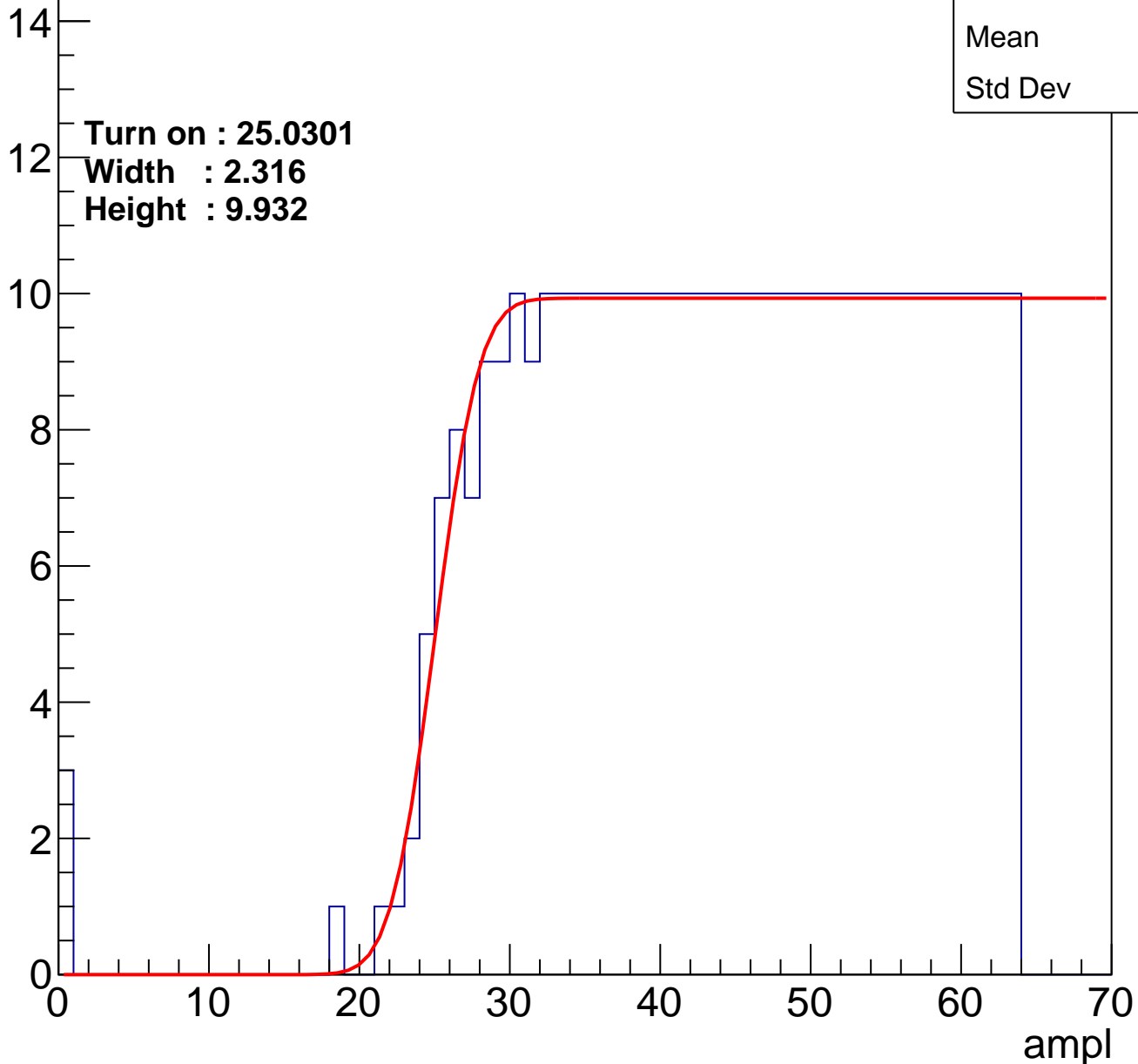
Entries	392
Mean	43.6
Std Dev	12

Turn on : 25.0301

Width : 2.316

Height : 9.932

Entry



B1L102S, U20-ch38

calib_packv5_042523_0143.root, FC#11, port A2

Entries	385
Mean	43.83
Std Dev	12.14

Turn on : 26.2825

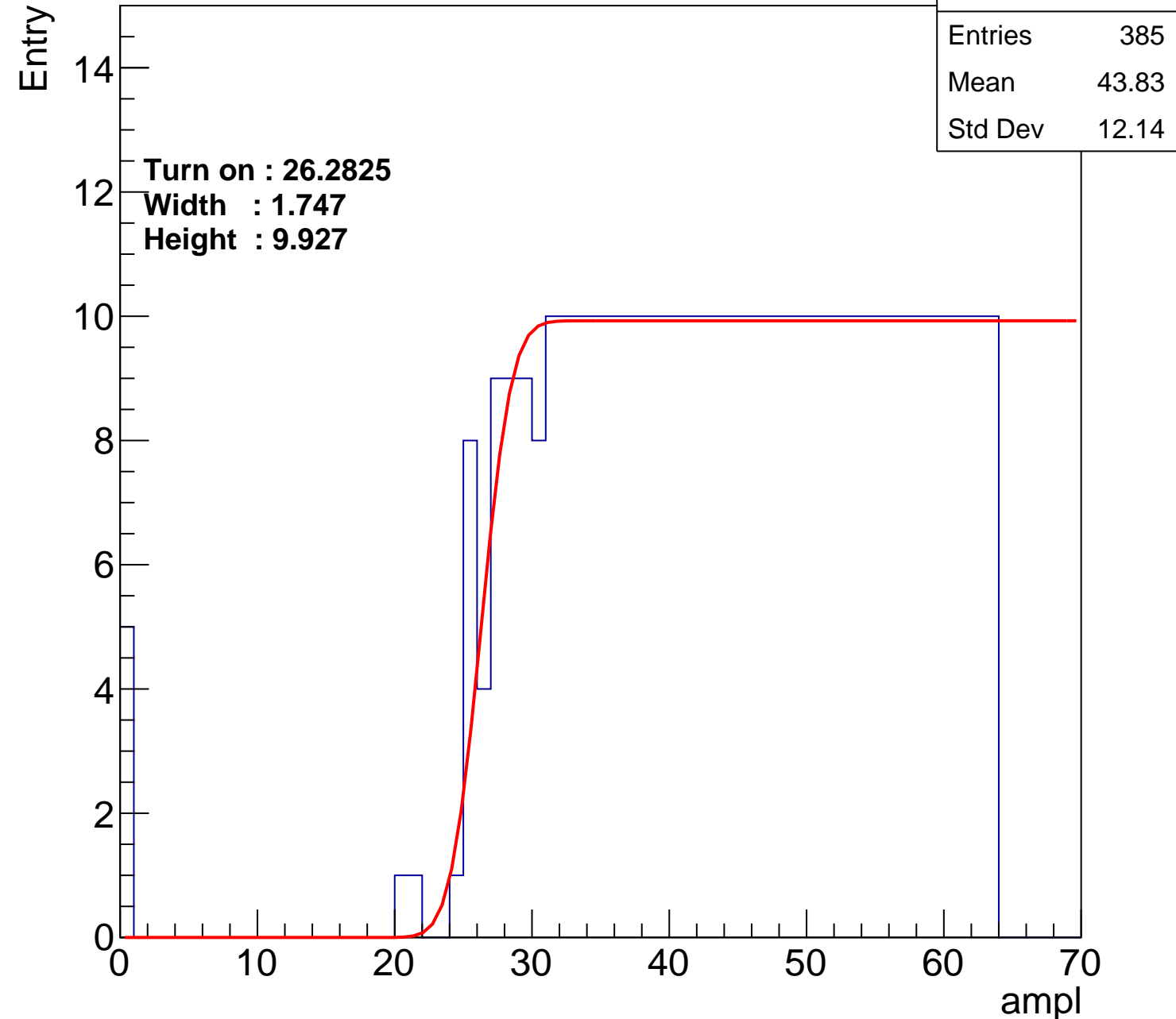
Width : 1.747

Height : 9.927

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U20-ch39

calib_packv5_042523_0143.root, FC#11, port A2

Entries	381
Mean	44.16
Std Dev	11.69

Turn on : 26.2119

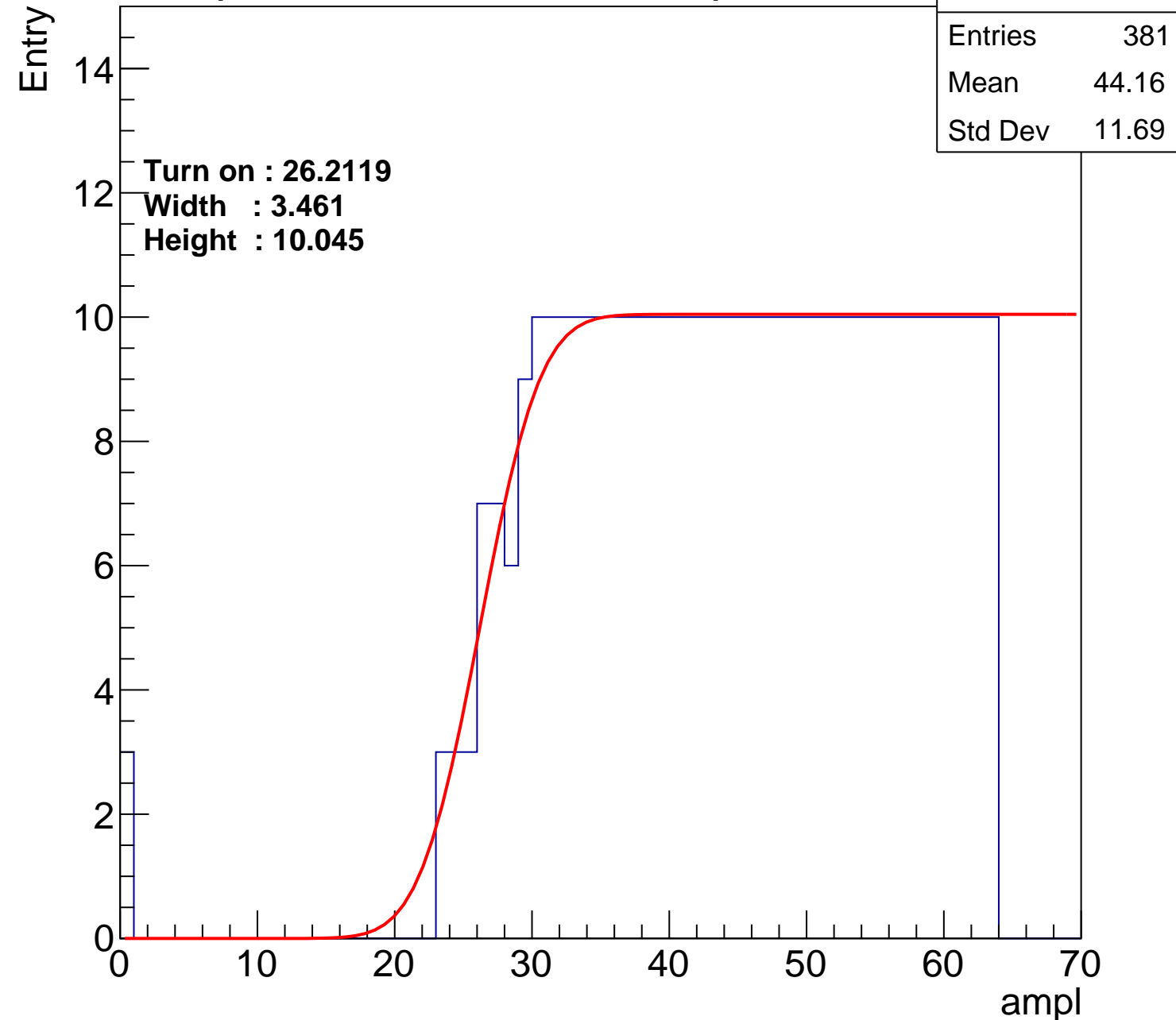
Width : 3.461

Height : 10.045

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U20-ch40

calib_packv5_042523_0143.root, FC#11, port A2

Entries	364
Mean	45.13
Std Dev	10.88

Turn on : 27.7742

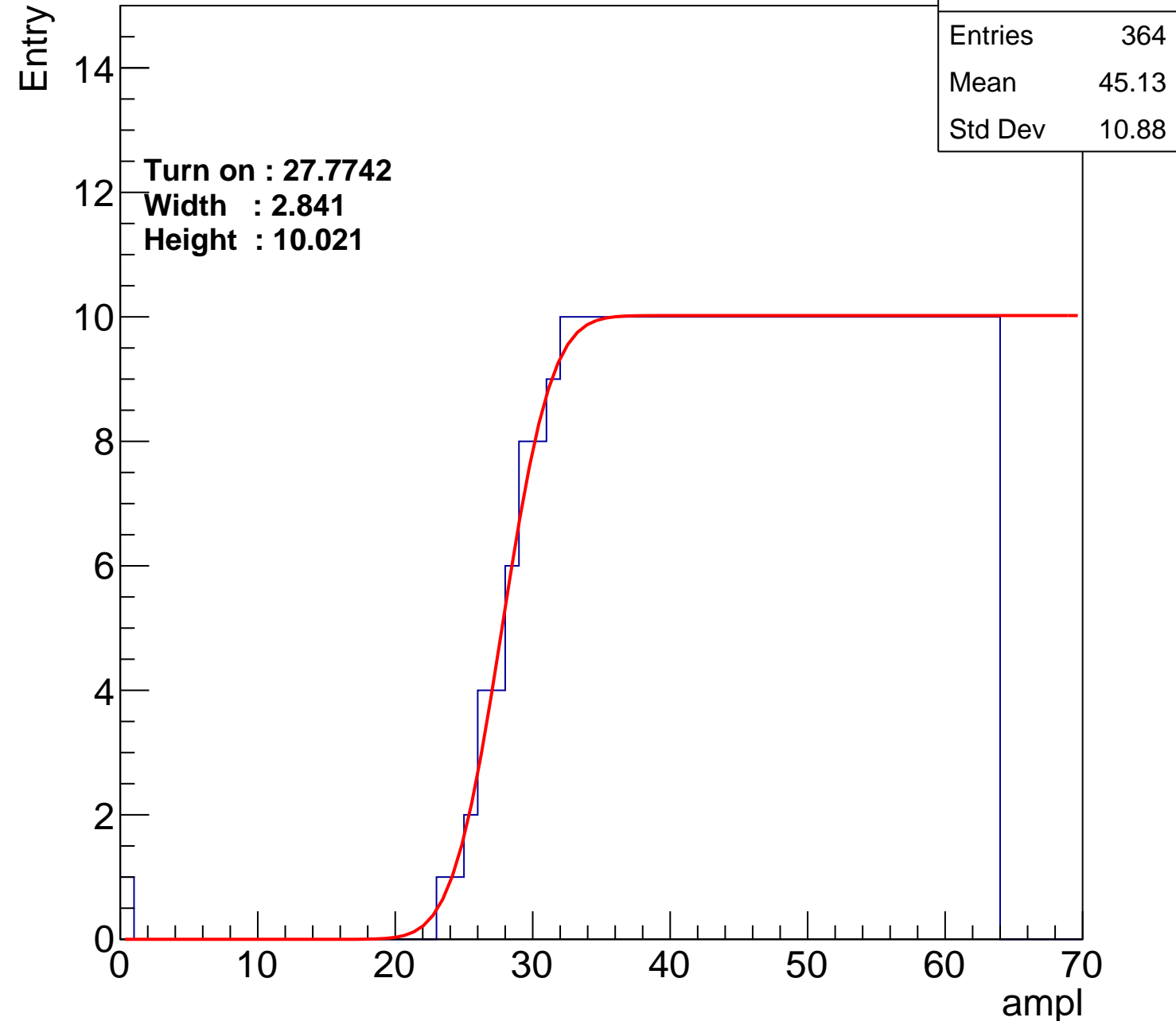
Width : 2.841

Height : 10.021

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U20-ch41

calib_packv5_042523_0143.root, FC#11, port A2

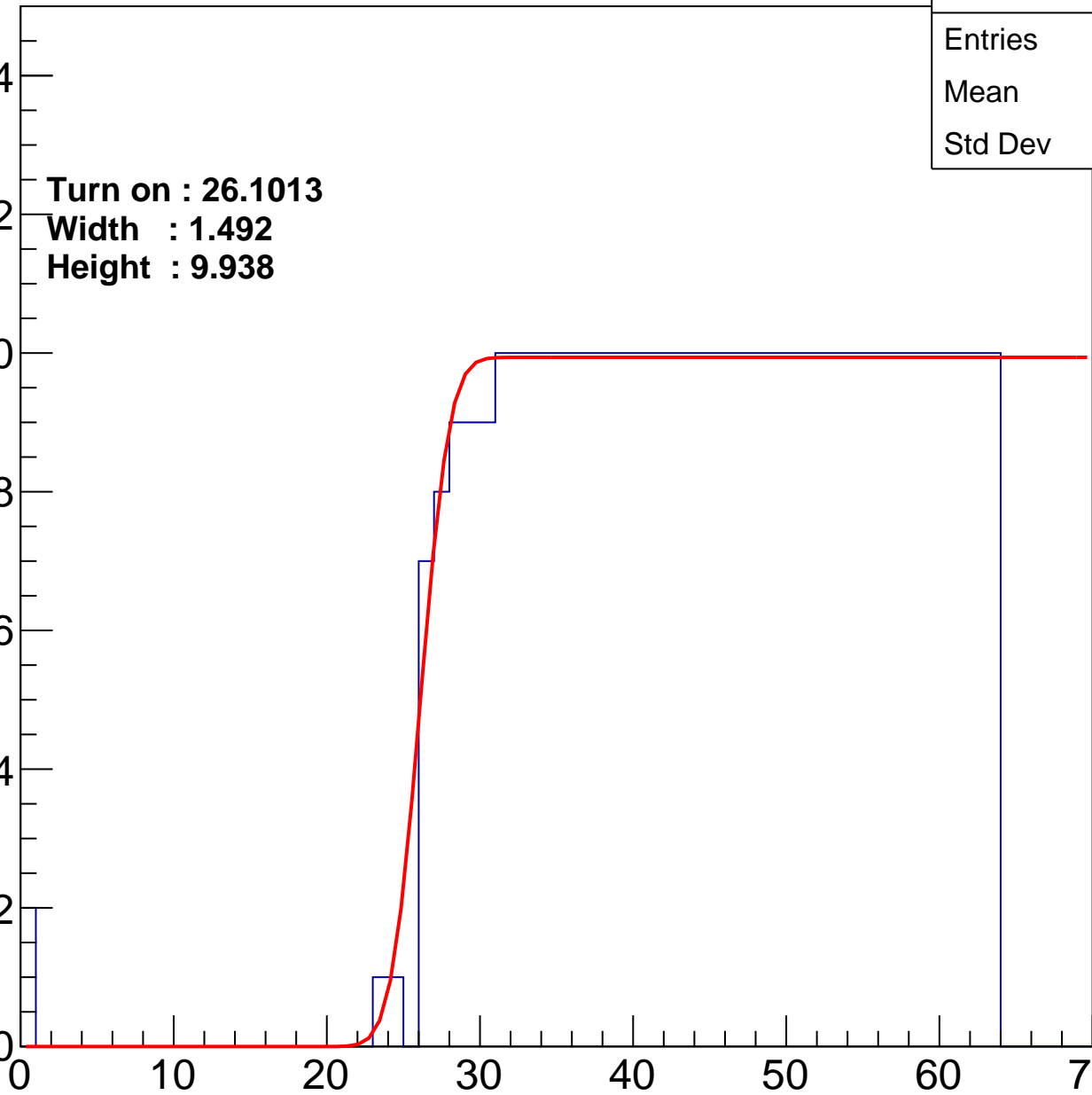
Entry

14
12
10
8
6
4
2
0

Turn on : 26.1013
Width : 1.492
Height : 9.938

Entries	376
Mean	44.52
Std Dev	11.32

ampl



B1L102S, U20-ch42

calib_packv5_042523_0143.root, FC#11, port A2

Entries	378
Mean	44.44
Std Dev	11.25

Turn on : 26.3845

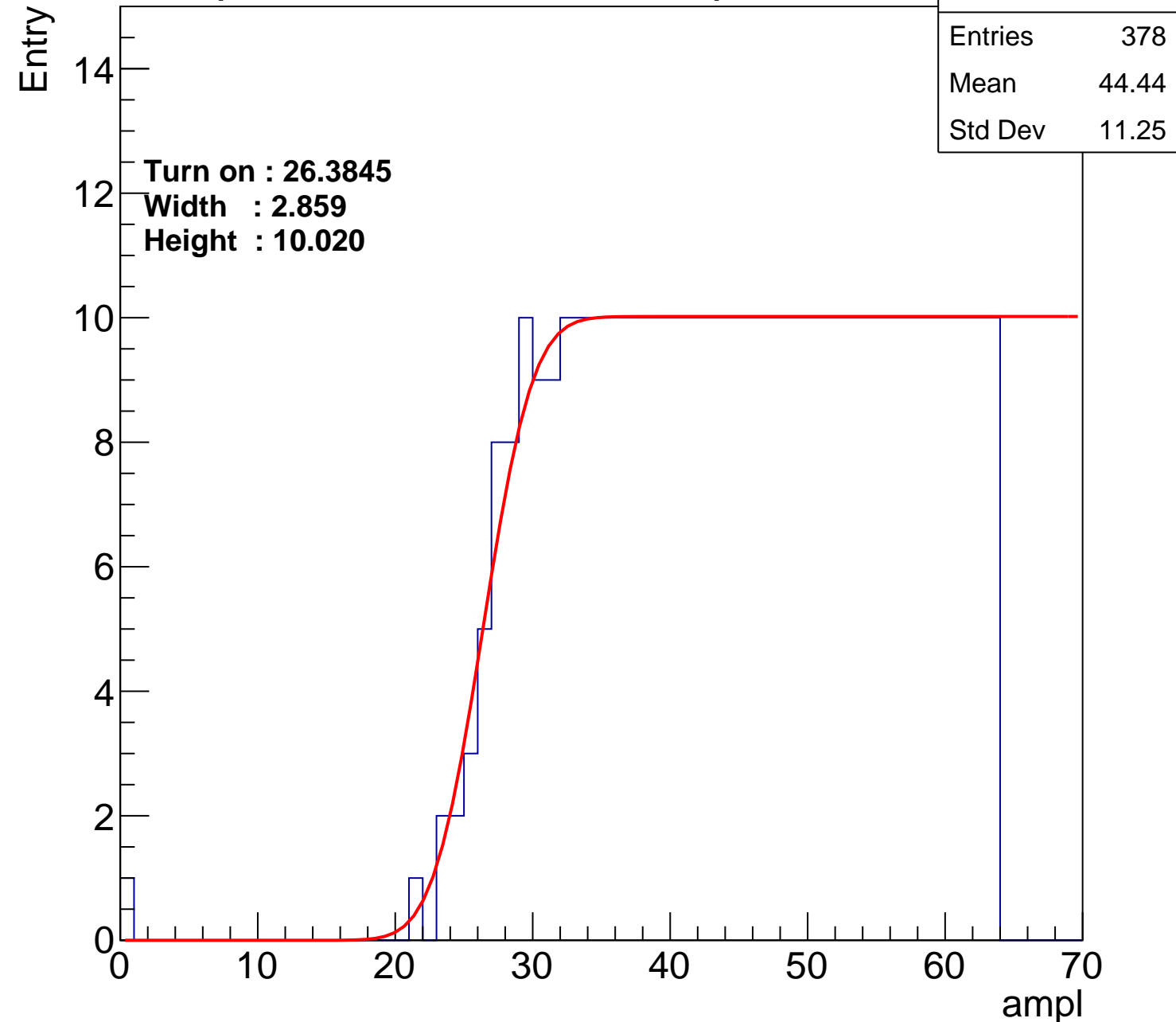
Width : 2.859

Height : 10.020

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U20-ch43

calib_packv5_042523_0143.root, FC#11, port A2

Entries	385
Mean	44.05
Std Dev	11.59

Turn on : 25.9448

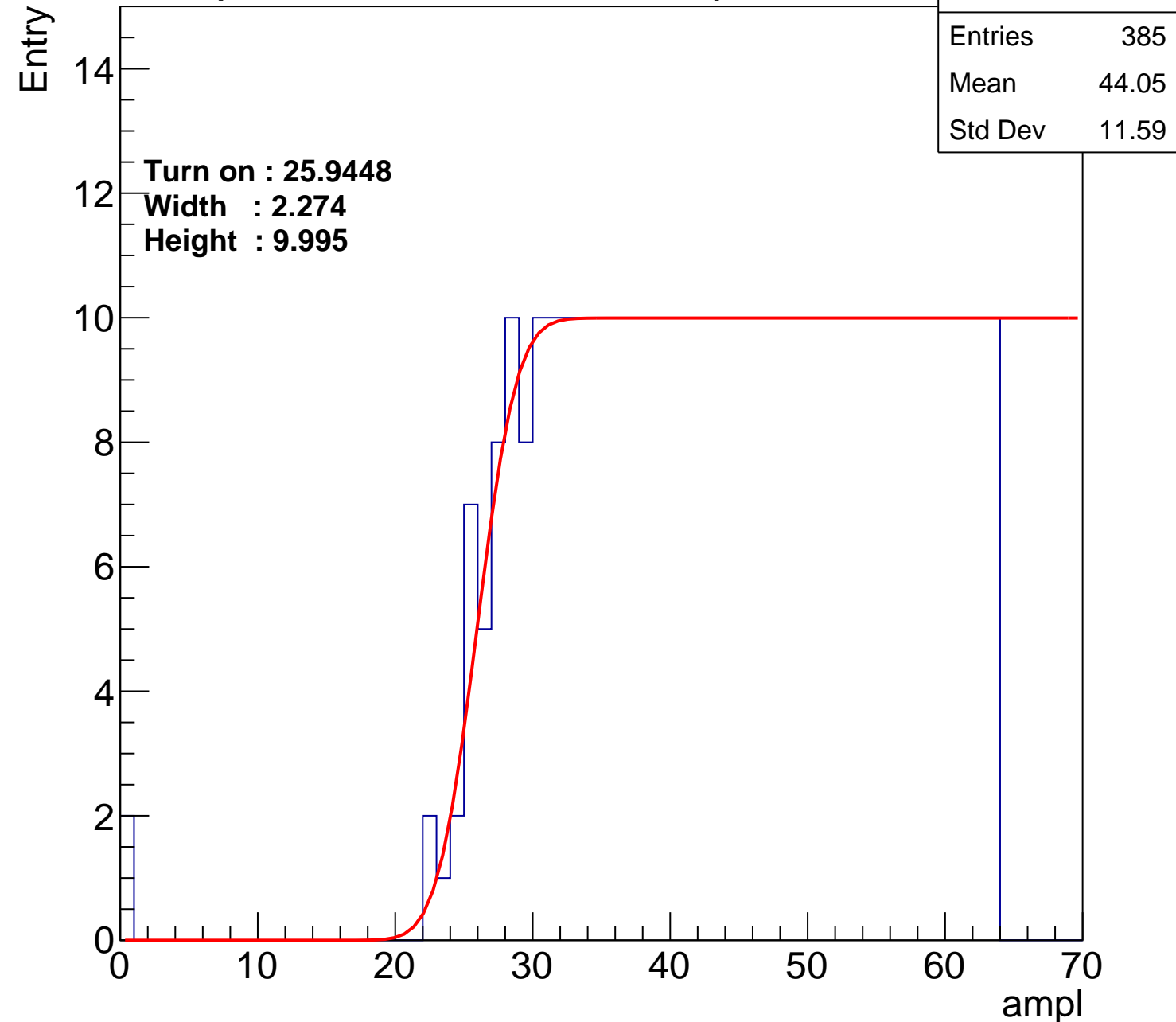
Width : 2.274

Height : 9.995

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U20-ch44

calib_packv5_042523_0143.root, FC#11, port A2

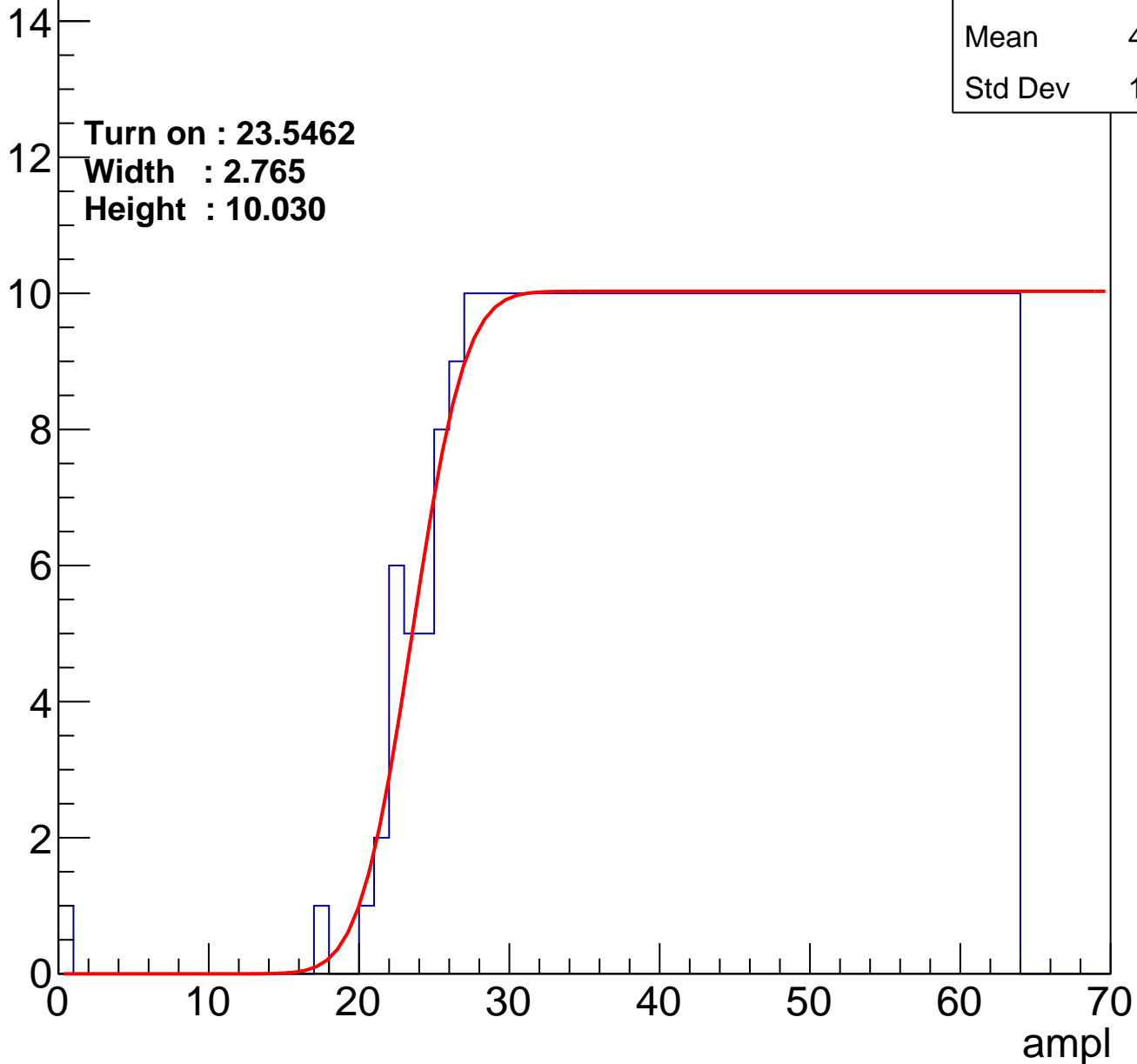
Entries	408
Mean	42.97
Std Dev	12.06

Turn on : 23.5462

Width : 2.765

Height : 10.030

Entry



B1L102S, U20-ch45

calib_packv5_042523_0143.root, FC#11, port A2

Entries	394
Mean	43.56
Std Dev	11.96

Turn on : 25.3705

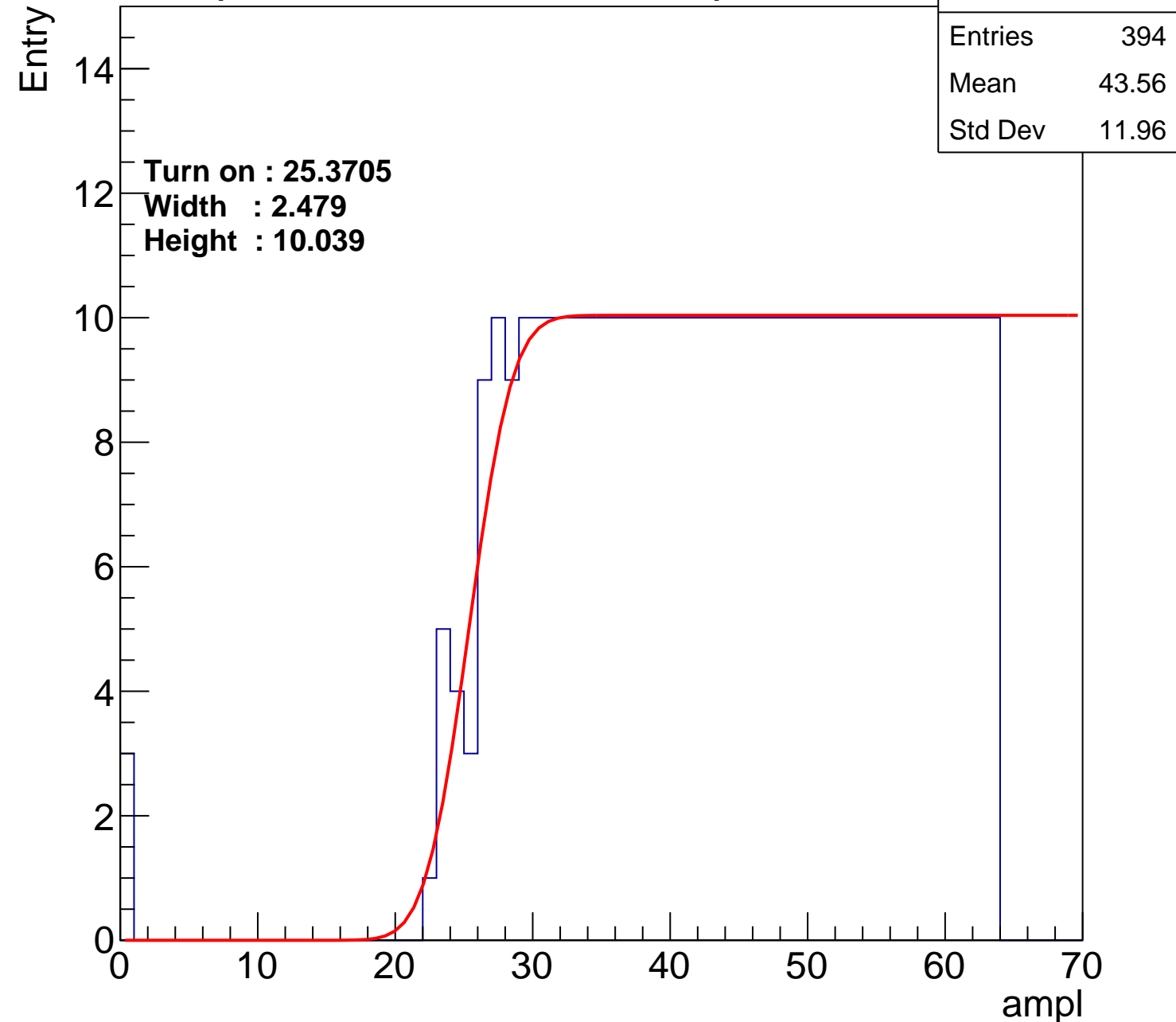
Width : 2.479

Height : 10.039

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U20-ch46

calib_packv5_042523_0143.root, FC#11, port A2

Entries	383
Mean	44.13
Std Dev	11.5

Turn on : 26.0532

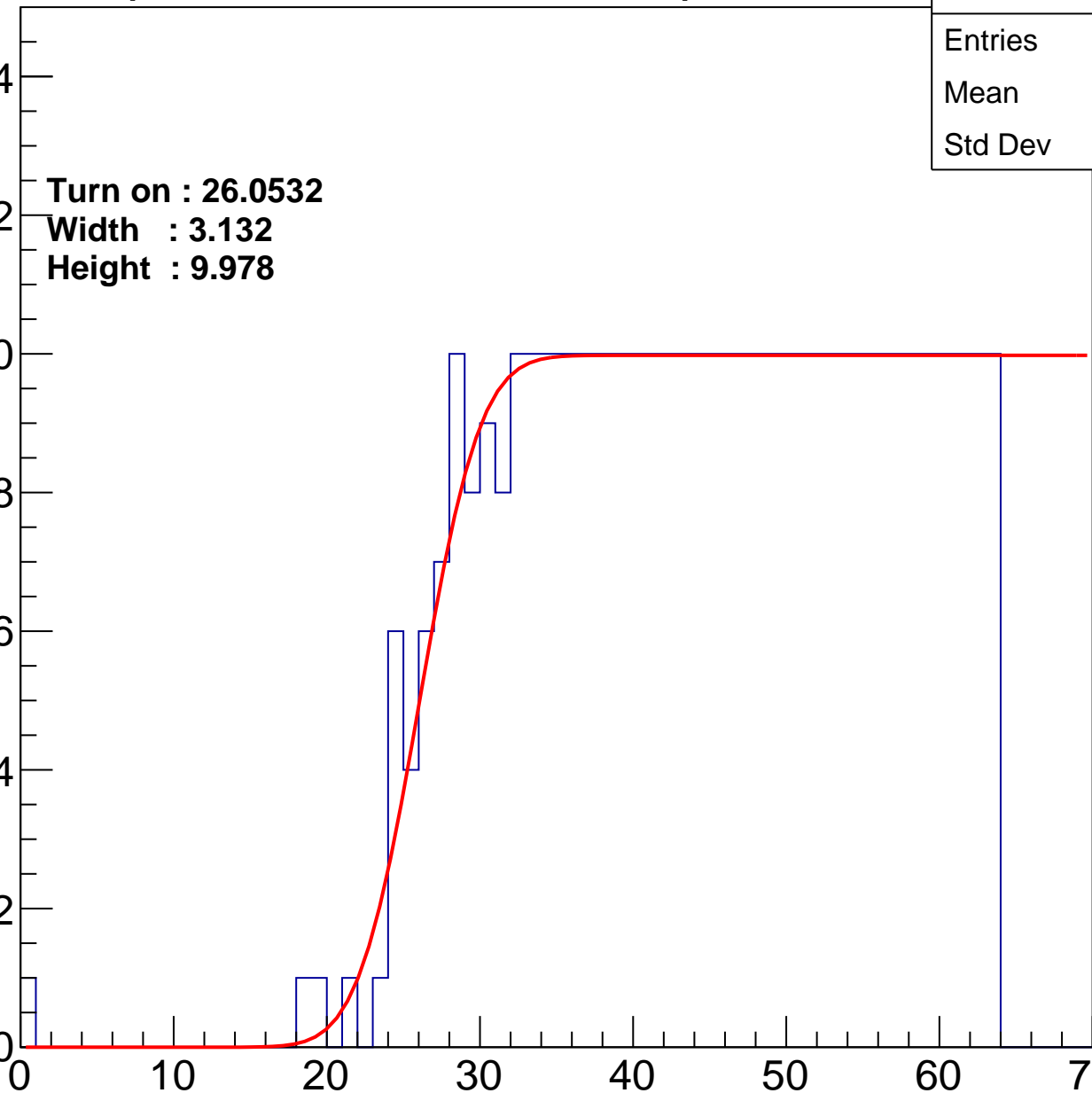
Width : 3.132

Height : 9.978

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U20-ch47

calib_packv5_042523_0143.root, FC#11, port A2

Entries	404
Mean	43.12
Std Dev	12.02

Turn on : 23.6211

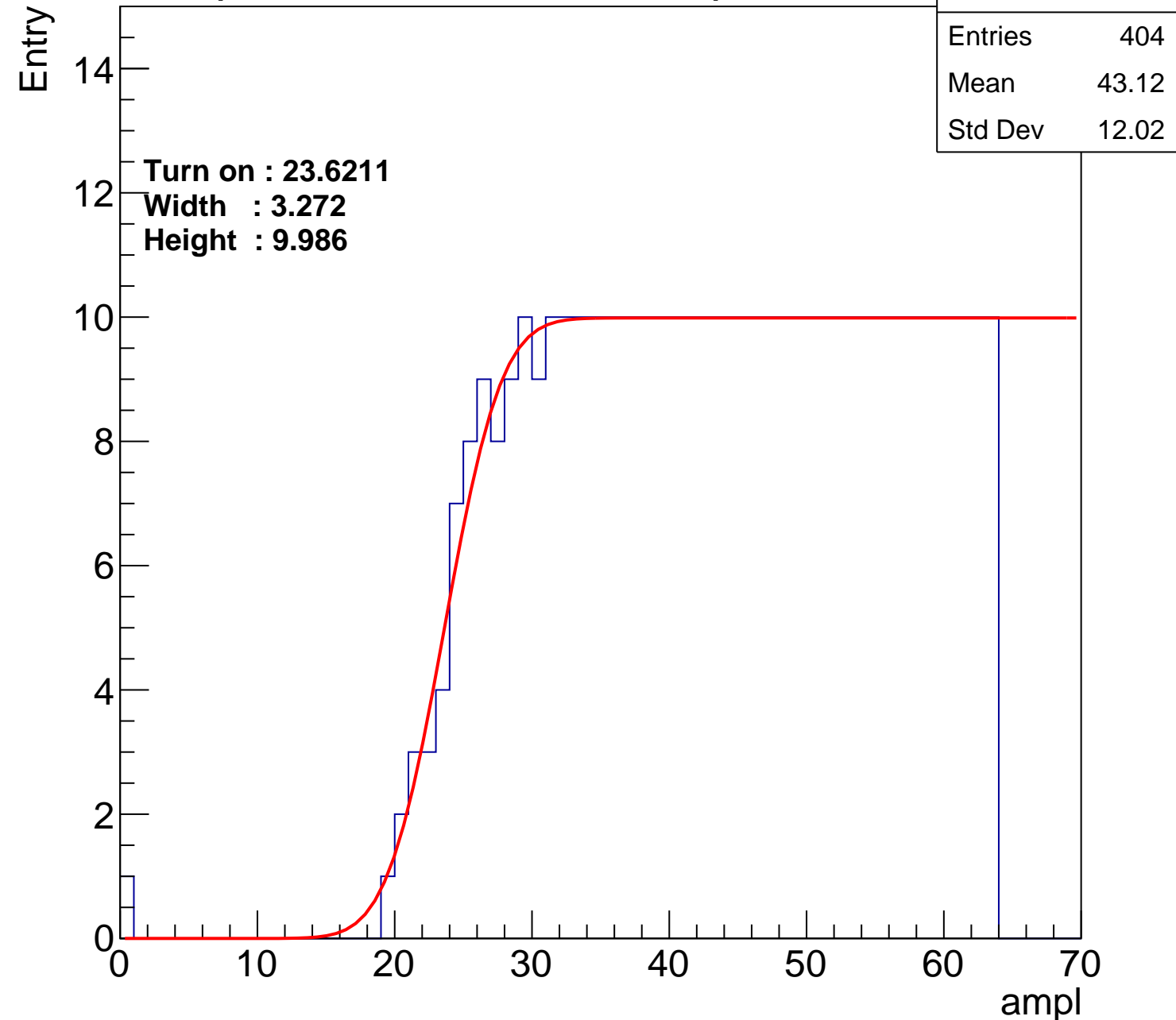
Width : 3.272

Height : 9.986

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U20-ch48

calib_packv5_042523_0143.root, FC#11, port A2

Entries	373
Mean	44.59
Std Dev	11.38

Turn on : 27.3138

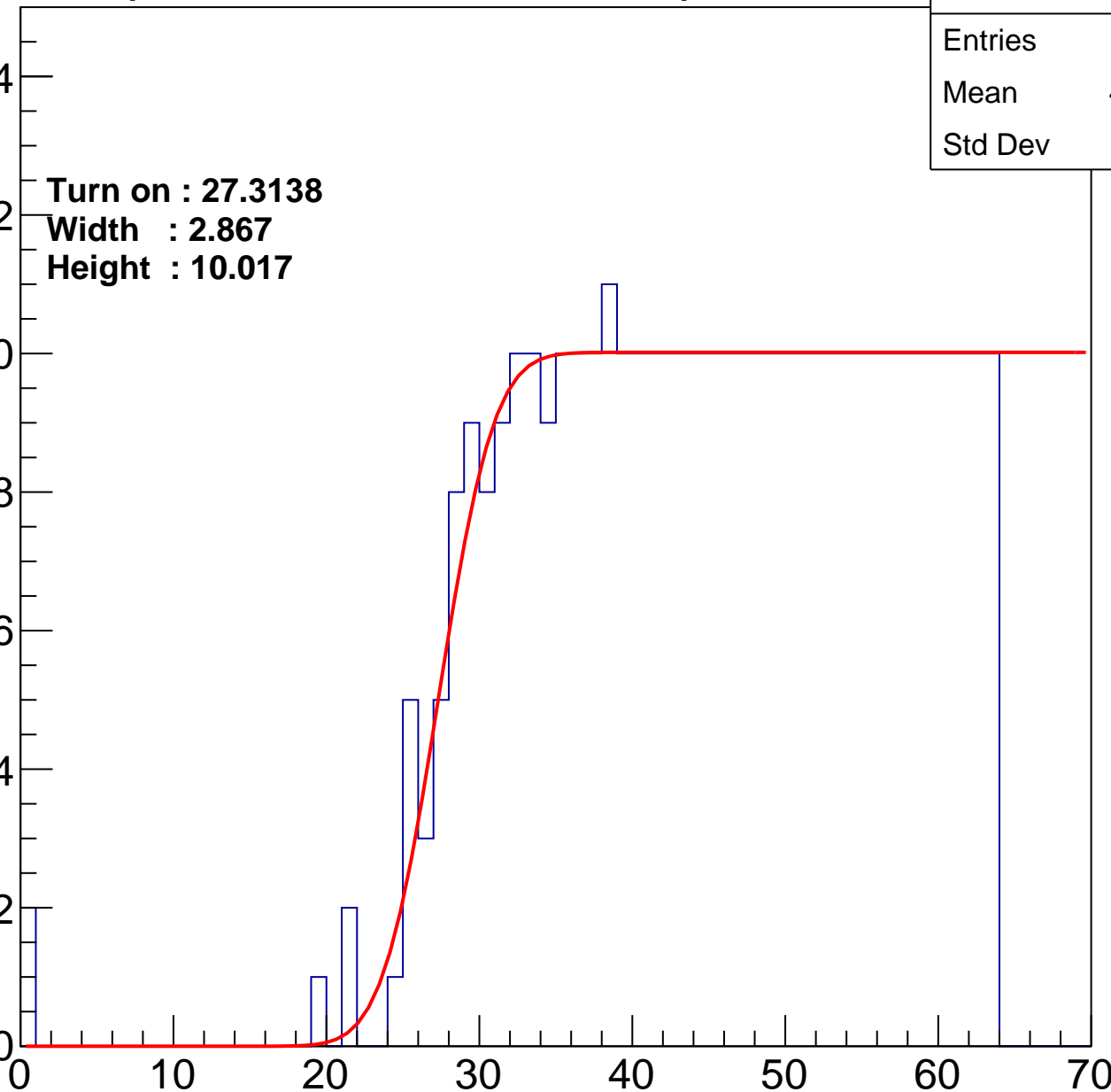
Width : 2.867

Height : 10.017

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U20-ch49

calib_packv5_042523_0143.root, FC#11, port A2

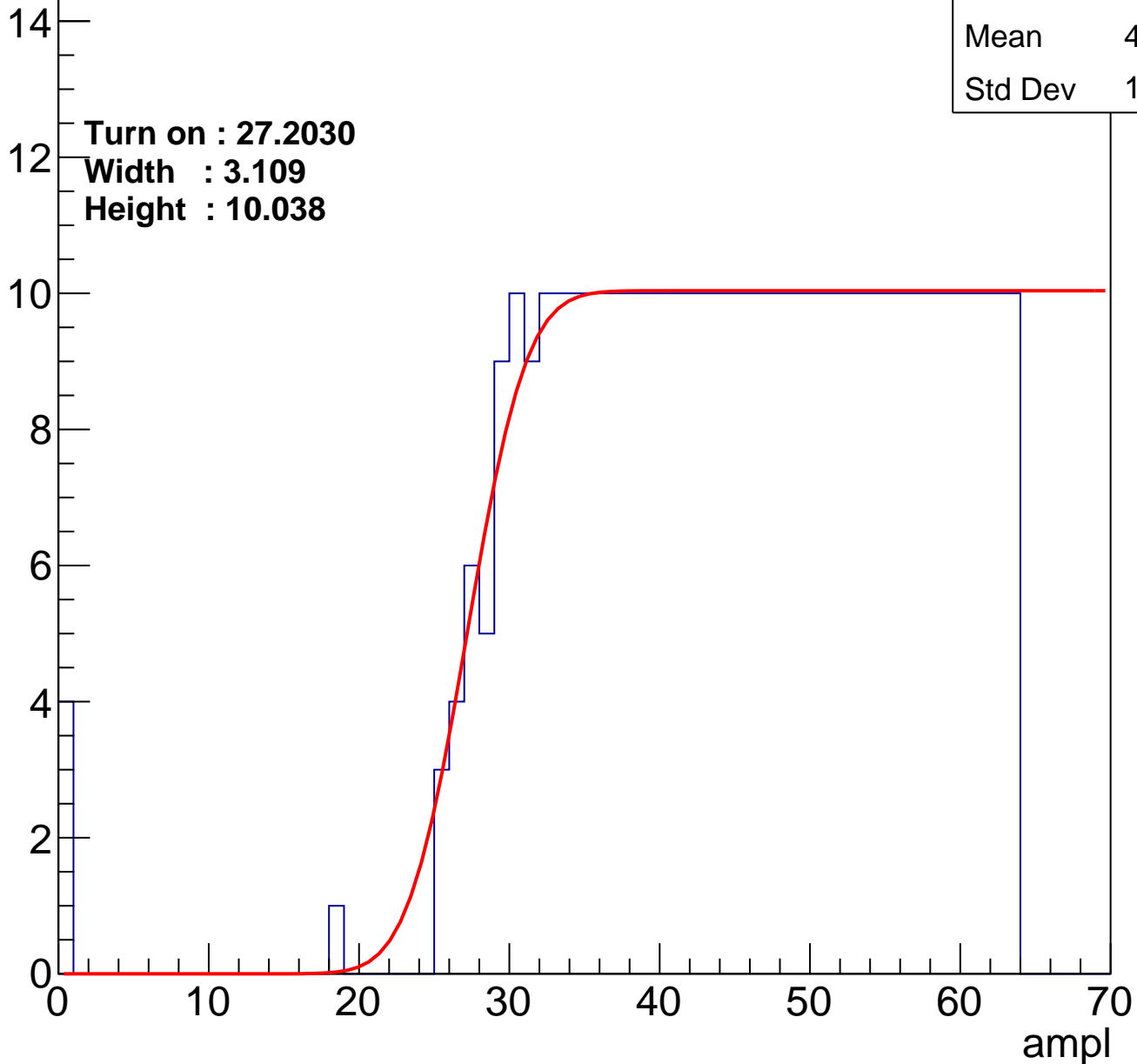
Entries	371
Mean	44.58
Std Dev	11.65

Turn on : 27.2030

Width : 3.109

Height : 10.038

Entry



B1L102S, U20-ch50

calib_packv5_042523_0143.root, FC#11, port A2

Entries	402
Mean	42.9
Std Dev	12.74

Turn on : 24.1360

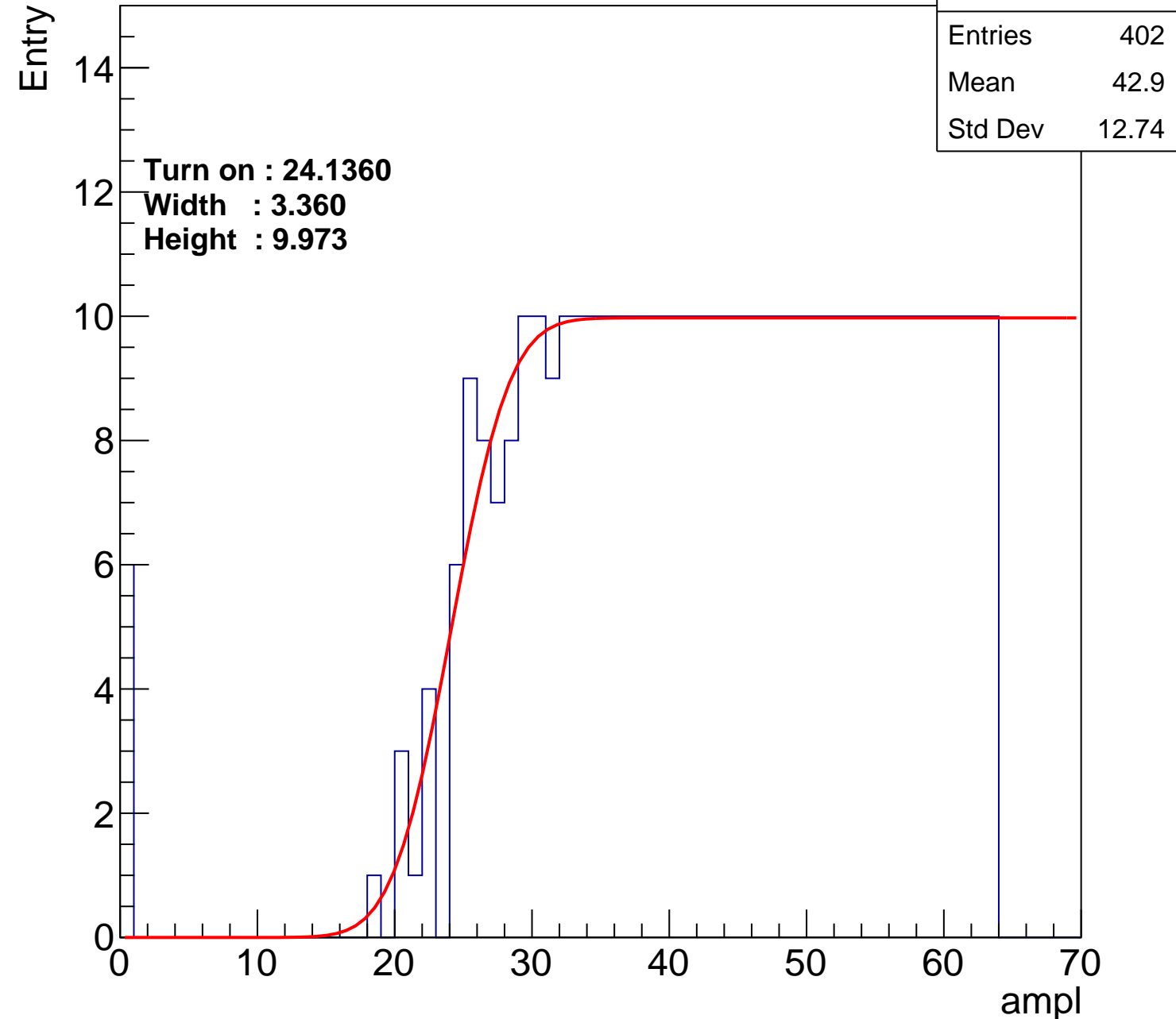
Width : 3.360

Height : 9.973

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U20-ch51

calib_packv5_042523_0143.root, FC#11, port A2

Entries	370
Mean	44.58
Std Dev	11.7

Turn on : 27.6899

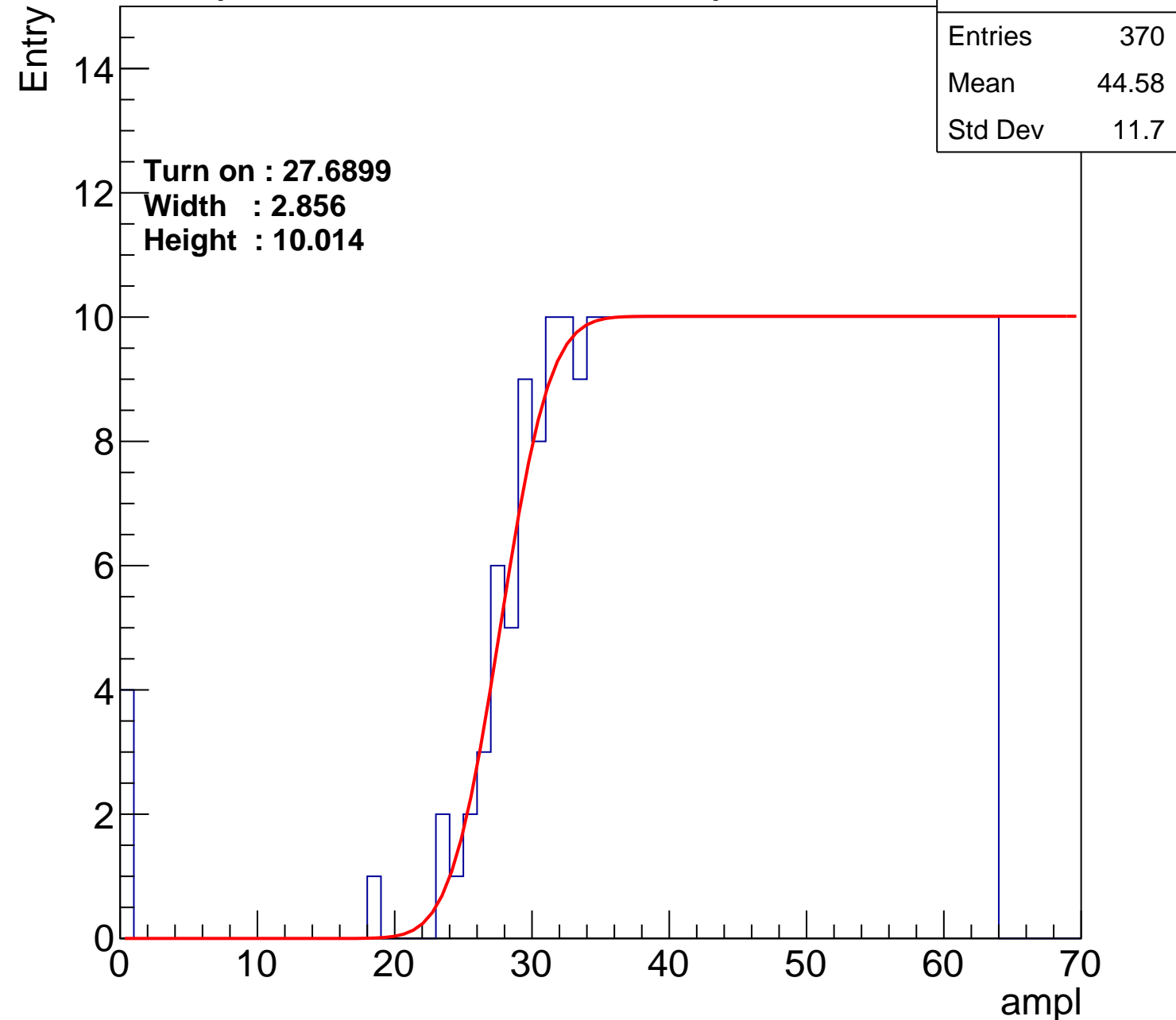
Width : 2.856

Height : 10.014

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U20-ch52

calib_packv5_042523_0143.root, FC#11, port A2

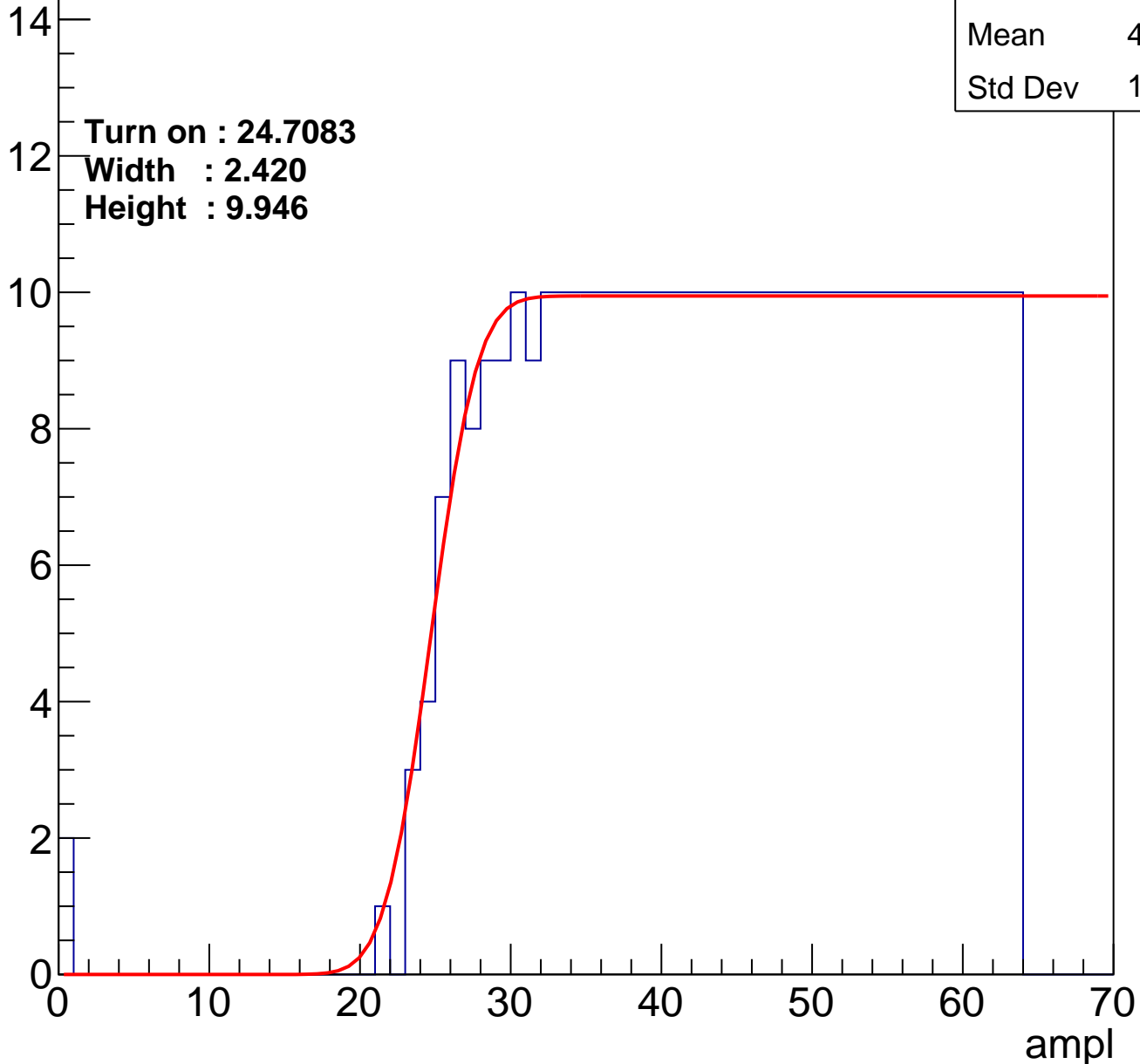
Entry

Entries	391
Mean	43.74
Std Dev	11.76

Turn on : 24.7083

Width : 2.420

Height : 9.946



B1L102S, U20-ch53

calib_packv5_042523_0143.root, FC#11, port A2

Entries	388
Mean	43.9
Std Dev	11.69

Turn on : 25.9781

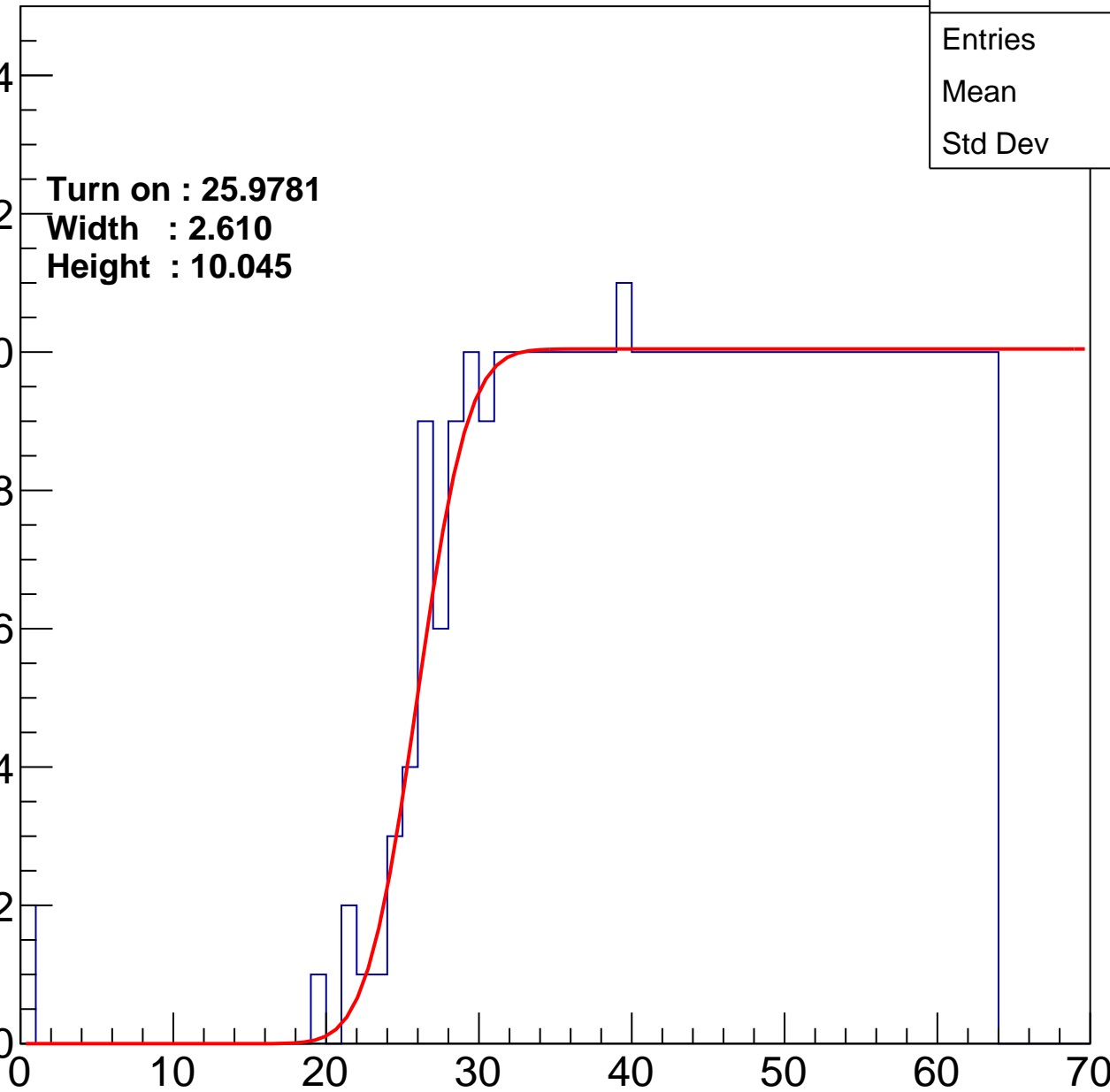
Width : 2.610

Height : 10.045

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U20-ch54

calib_packv5_042523_0143.root, FC#11, port A2

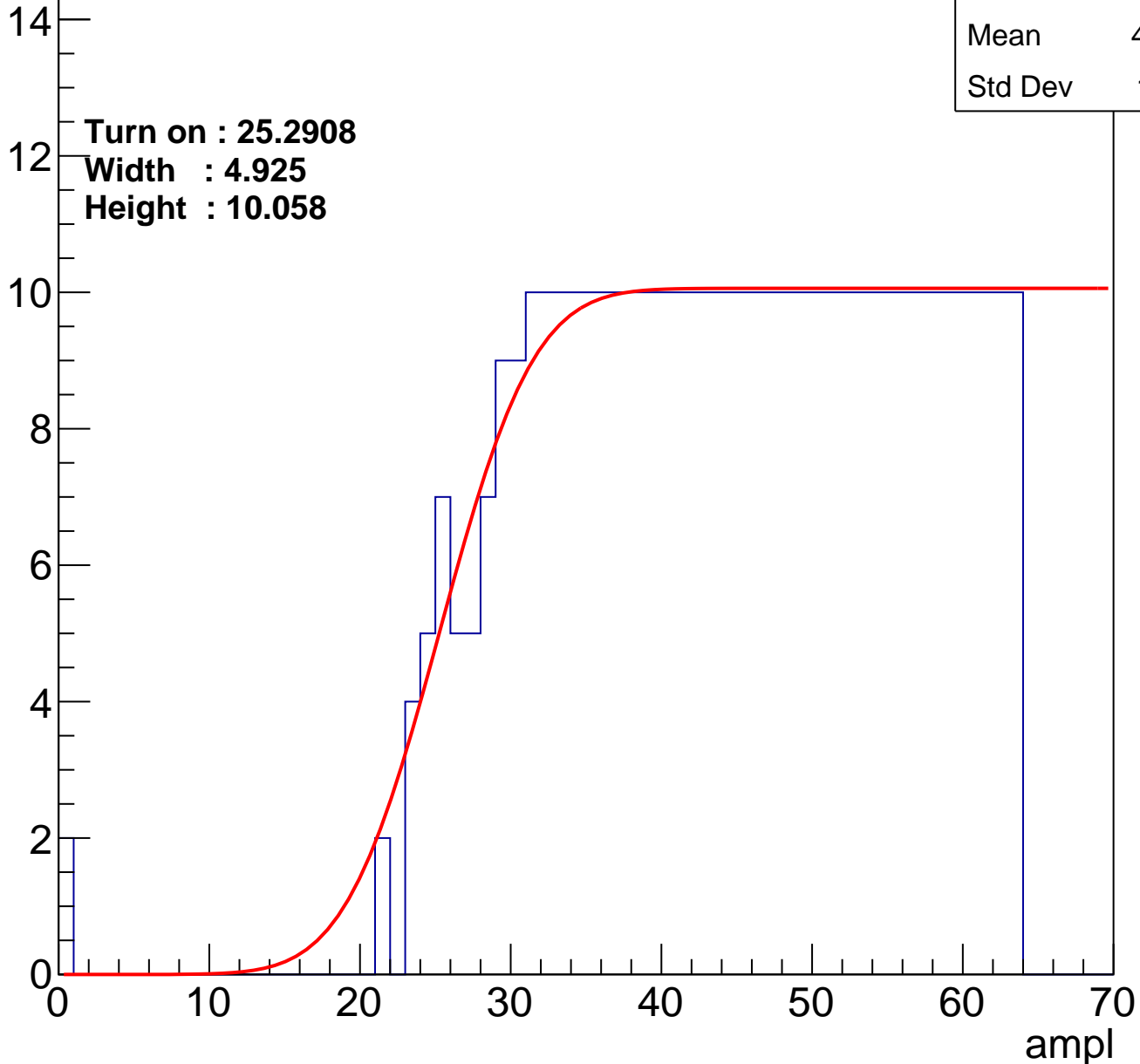
Entries	385
Mean	43.98
Std Dev	11.71

Turn on : 25.2908

Width : 4.925

Height : 10.058

Entry



B1L102S, U20-ch55

calib_packv5_042523_0143.root, FC#11, port A2

Entries	385
Mean	43.89
Std Dev	11.98

Turn on : 25.7851

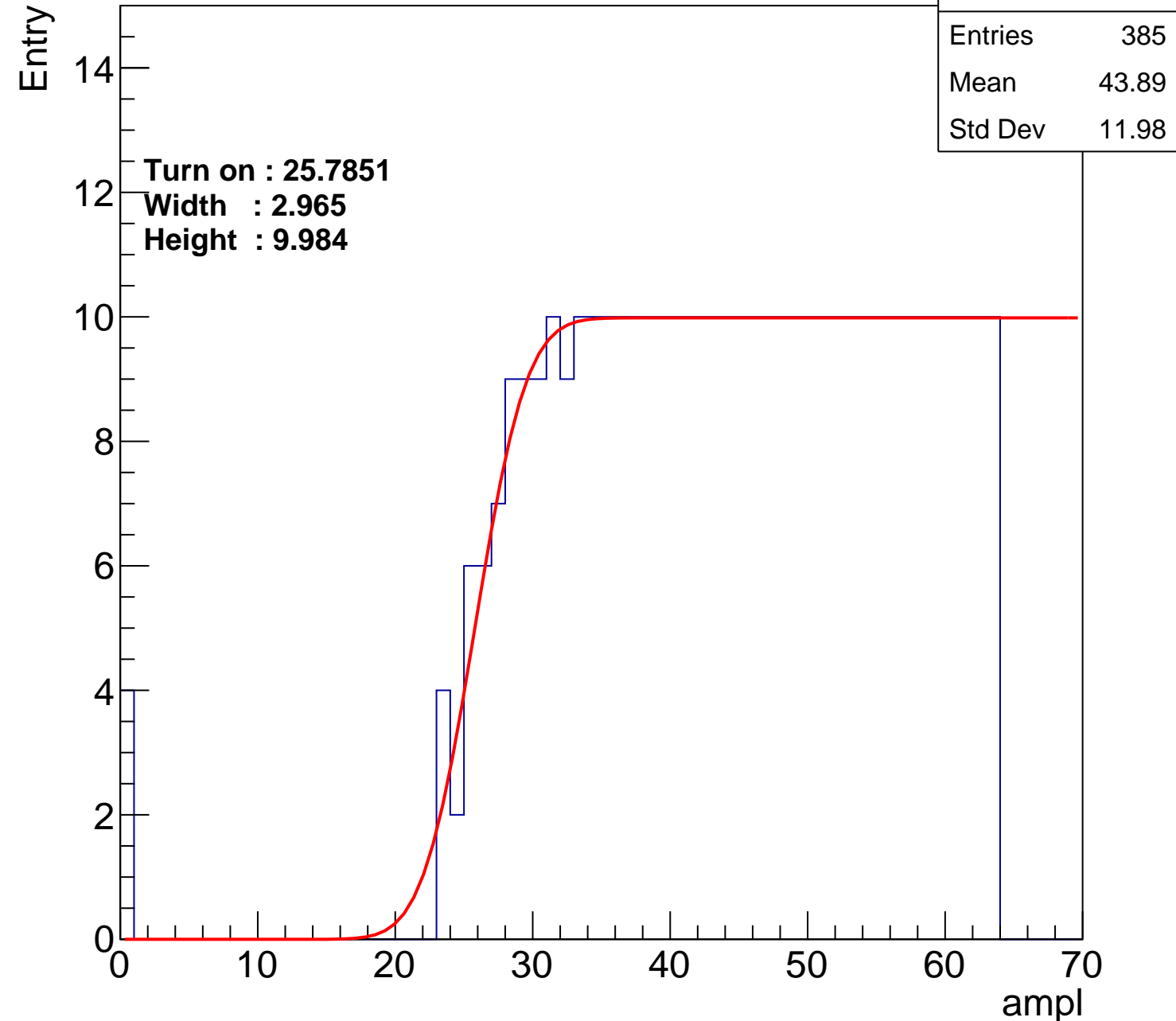
Width : 2.965

Height : 9.984

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U20-ch56

calib_packv5_042523_0143.root, FC#11, port A2

Entries	409
Mean	42.85
Std Dev	12.24

Turn on : 23.5100

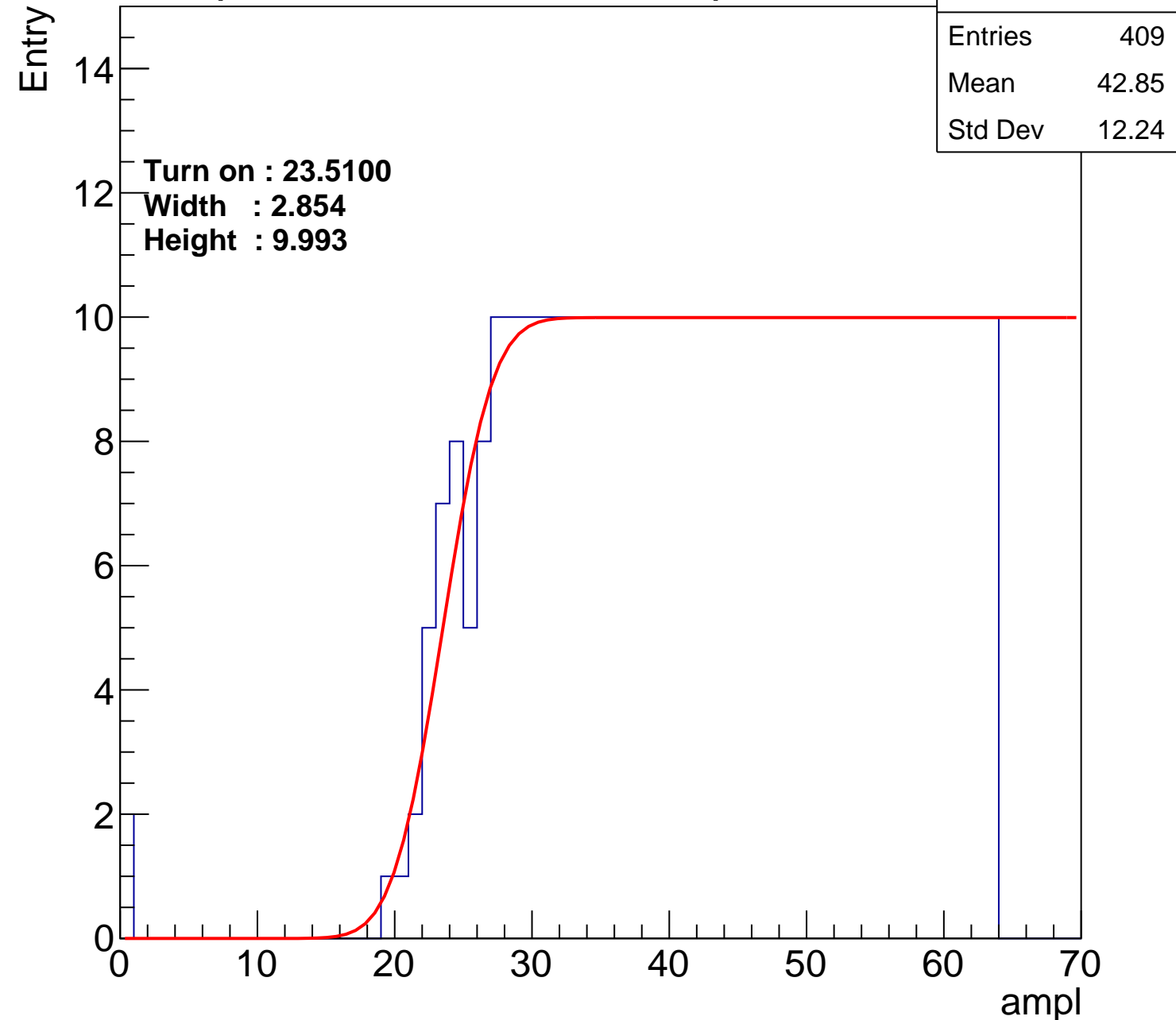
Width : 2.854

Height : 9.993

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U20-ch57

calib_packv5_042523_0143.root, FC#11, port A2

Entries	383
Mean	44.13
Std Dev	11.56

Turn on : 26.1477

Width : 2.965

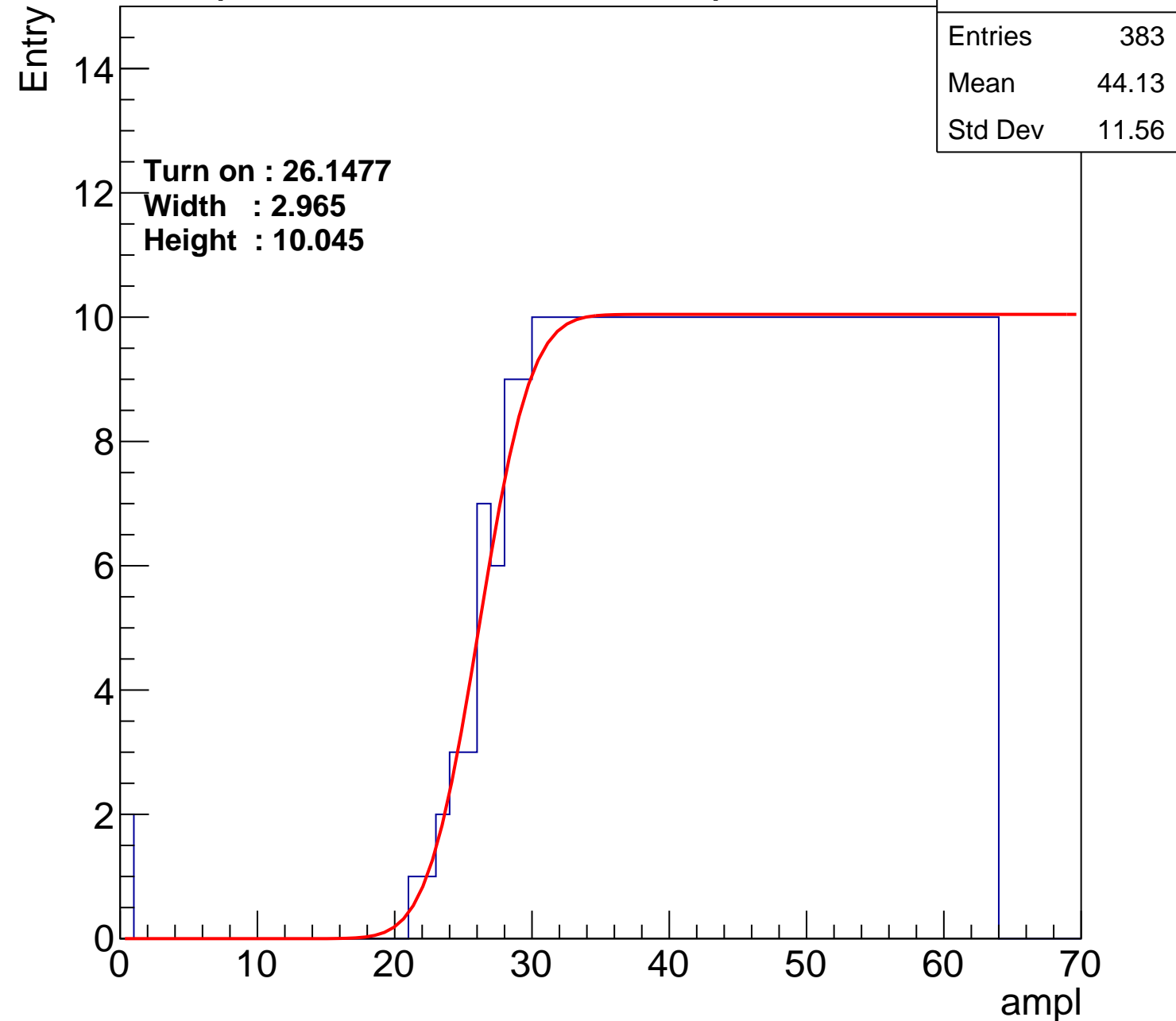
Height : 10.045

Entry

14
12
10
8
6
4
2
0

ampl

0 10 20 30 40 50 60 70



B1L102S, U20-ch58

calib_packv5_042523_0143.root, FC#11, port A2

Entries	384
Mean	44.1
Std Dev	11.5

Turn on : 26.5176

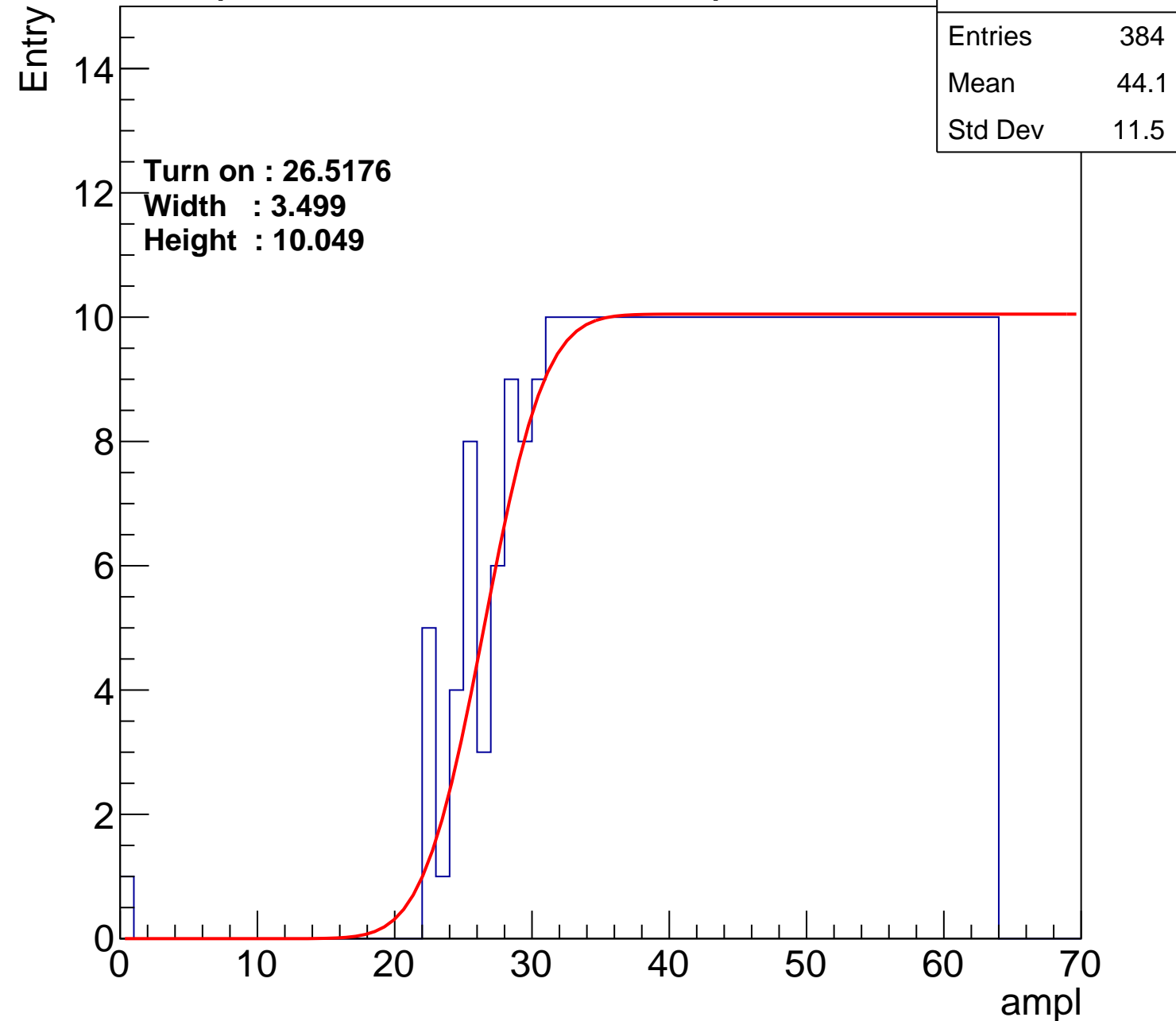
Width : 3.499

Height : 10.049

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U20-ch59

calib_packv5_042523_0143.root, FC#11, port A2

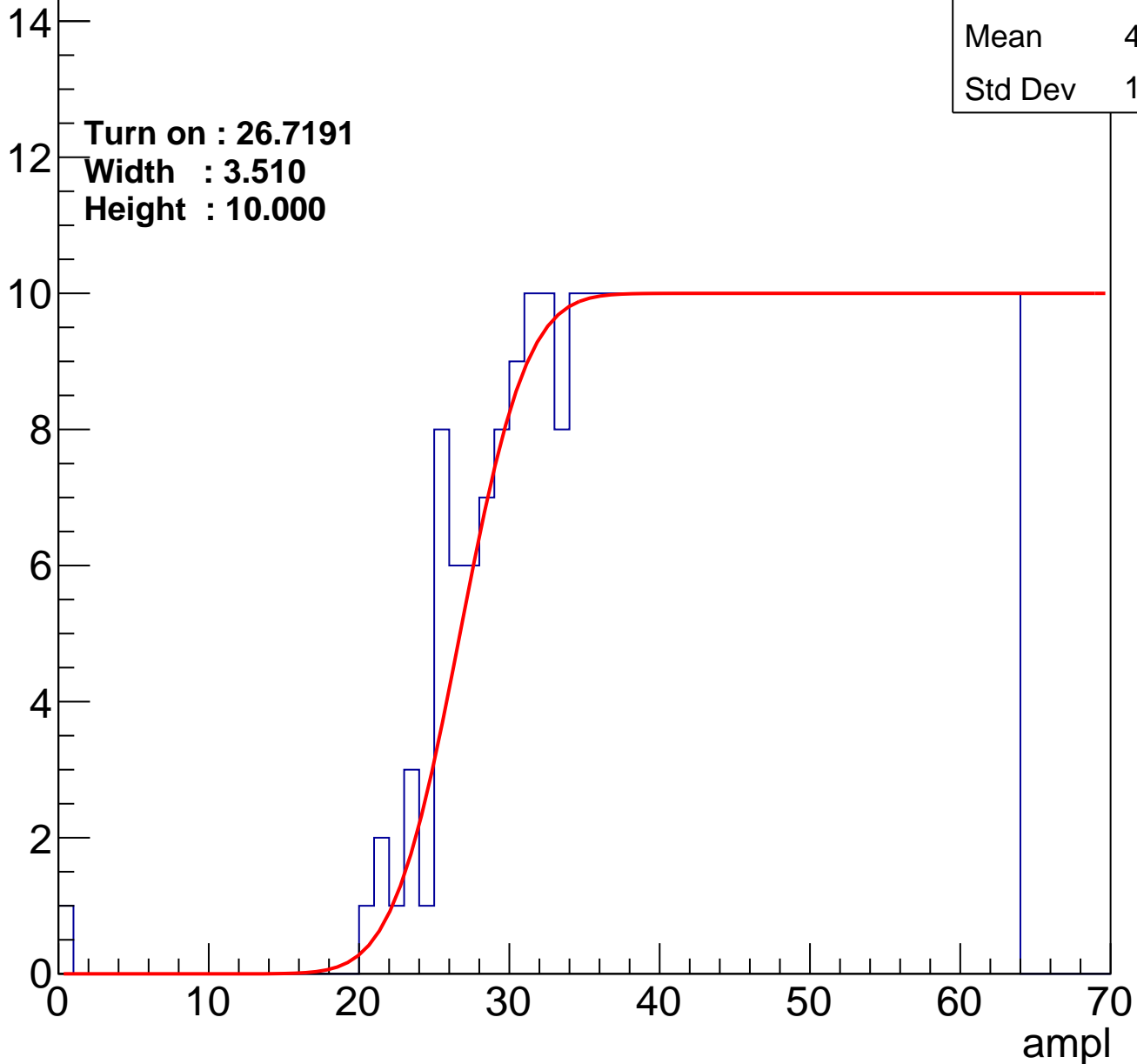
Entries	381
Mean	44.19
Std Dev	11.49

Turn on : 26.7191

Width : 3.510

Height : 10.000

Entry



B1L102S, U20-ch60

calib_packv5_042523_0143.root, FC#11, port A2

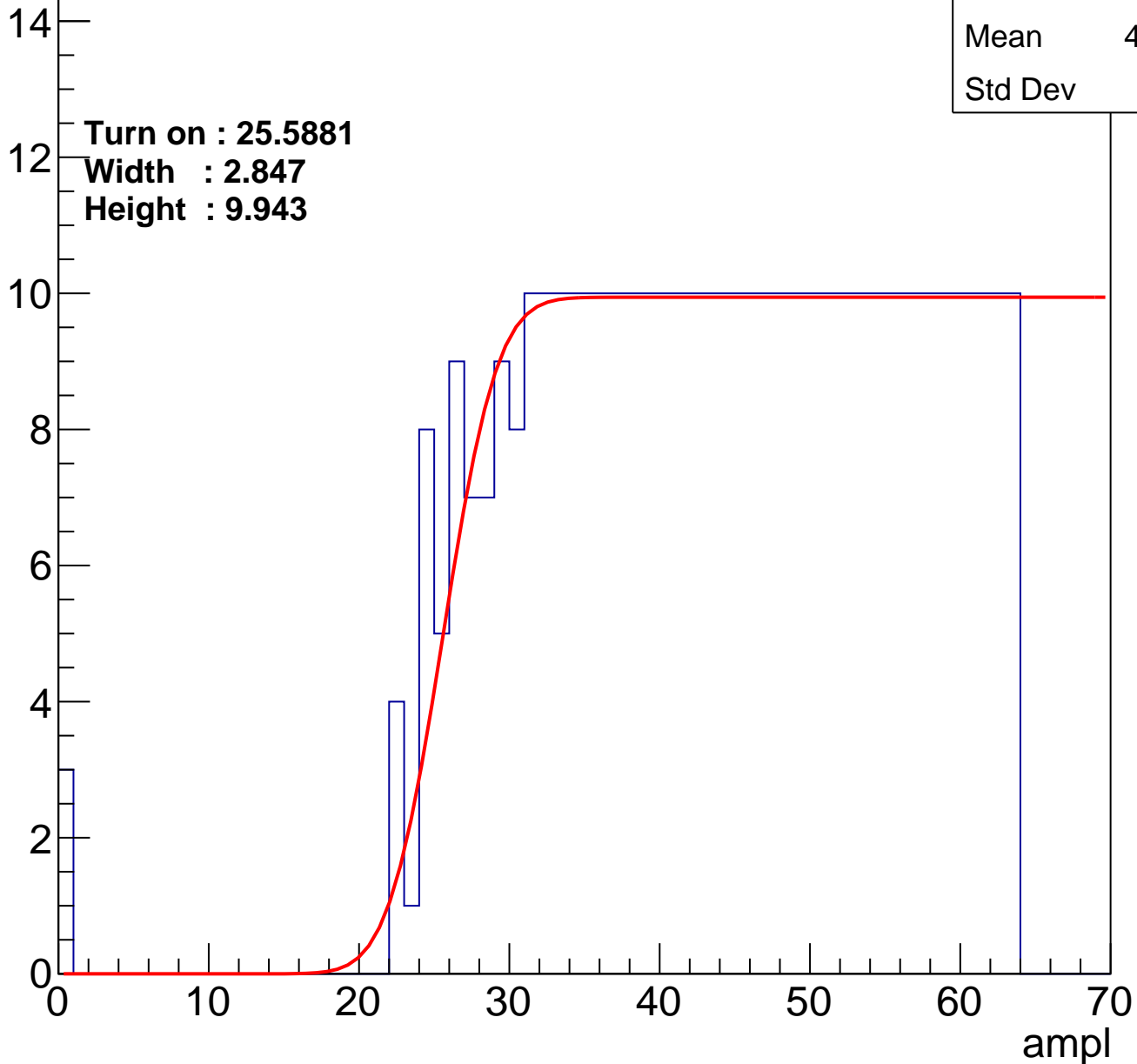
Entries	391
Mean	43.63
Std Dev	12

Turn on : 25.5881

Width : 2.847

Height : 9.943

Entry



B1L102S, U20-ch61

calib_packv5_042523_0143.root, FC#11, port A2

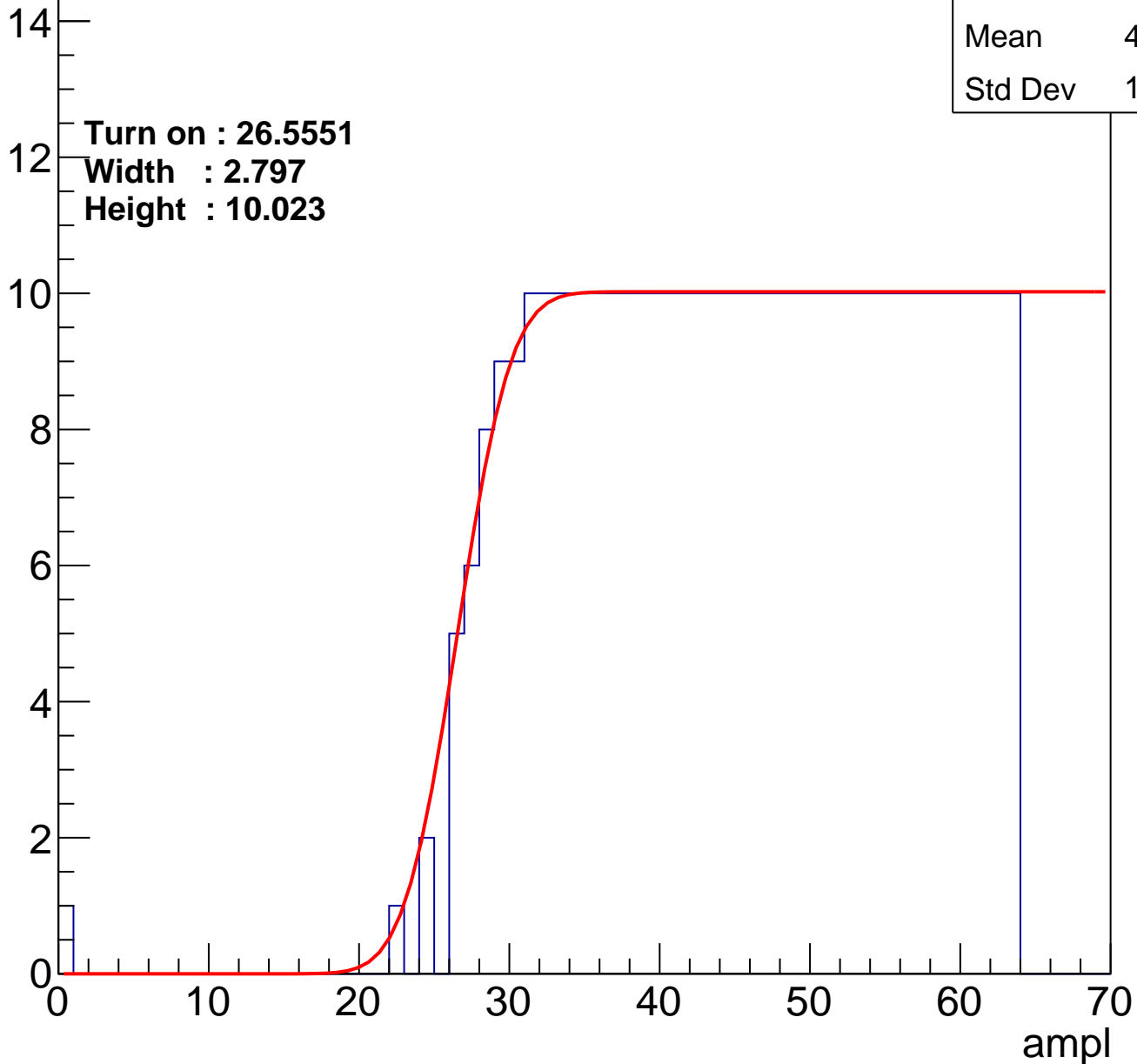
Entries	371
Mean	44.82
Std Dev	11.02

Turn on : 26.5551

Width : 2.797

Height : 10.023

Entry



B1L102S, U20-ch62

calib_packv5_042523_0143.root, FC#11, port A2

Entries	385
Mean	43.89
Std Dev	11.98

Turn on : 25.9338

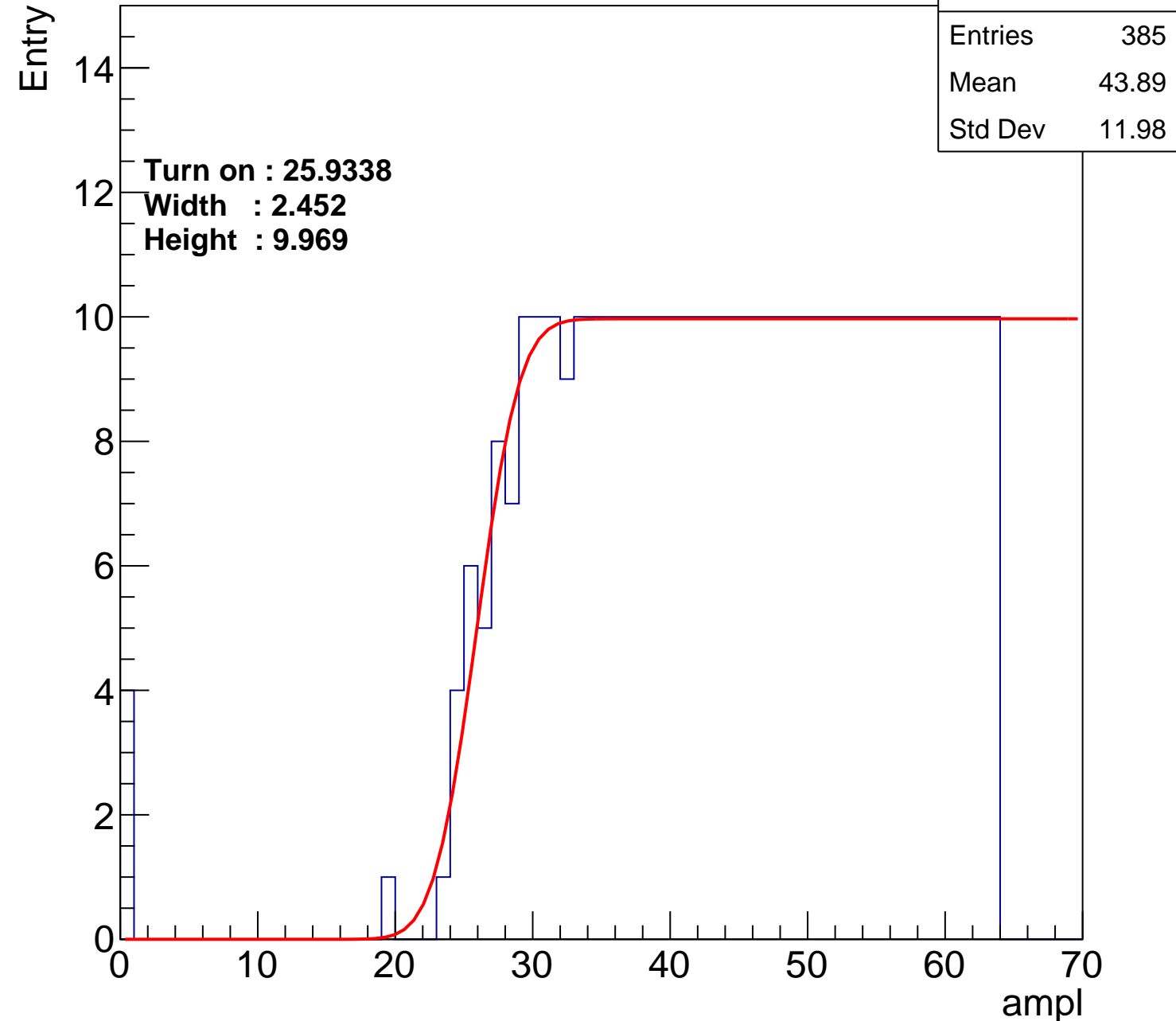
Width : 2.452

Height : 9.969

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U20-ch63

calib_packv5_042523_0143.root, FC#11, port A2

Entries	391
Mean	43.71
Std Dev	11.82

Turn on : 25.0388

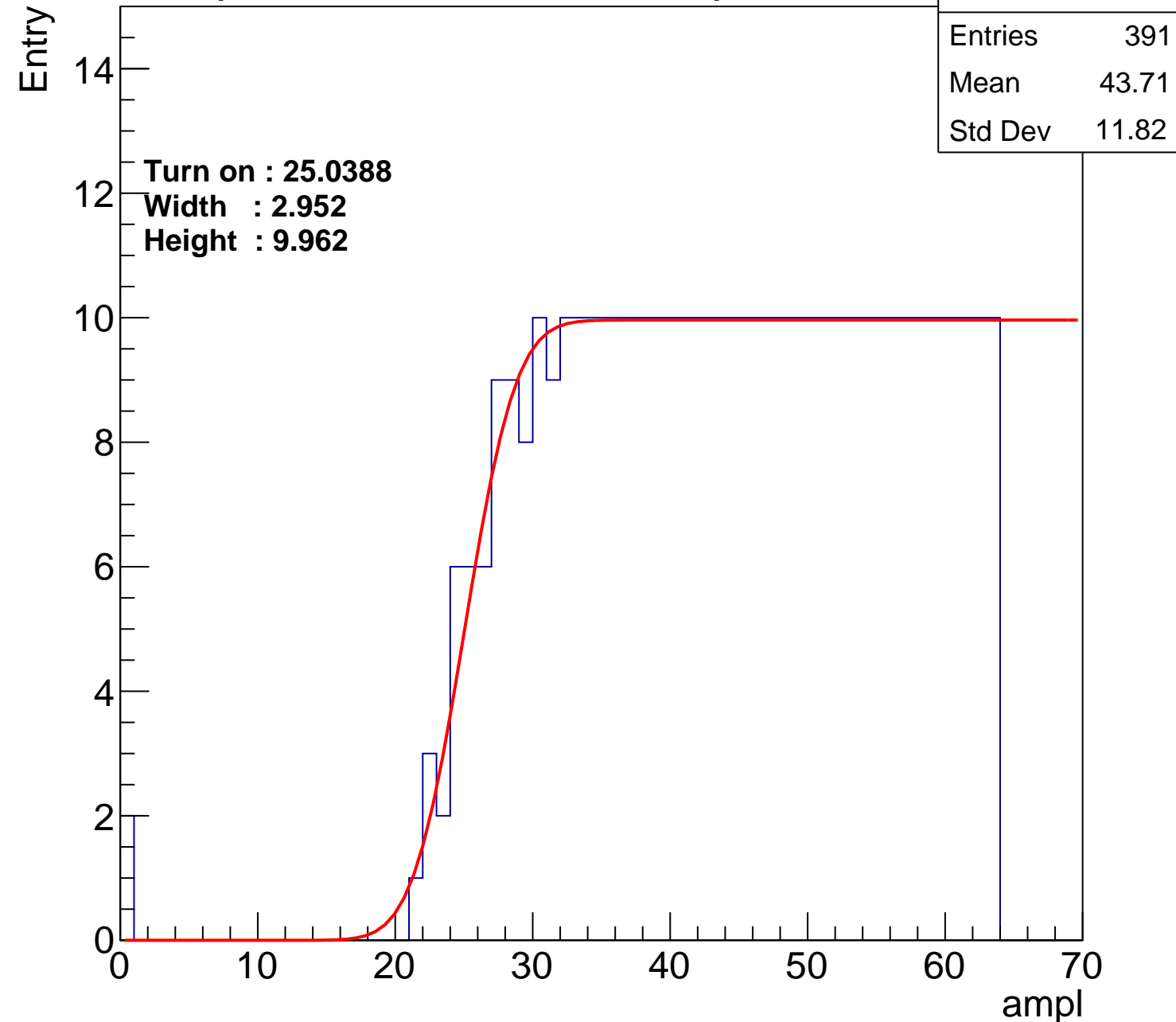
Width : 2.952

Height : 9.962

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U20-ch64

calib_packv5_042523_0143.root, FC#11, port A2

Entries	380
Mean	44.29
Std Dev	11.47

Turn on : 26.2475

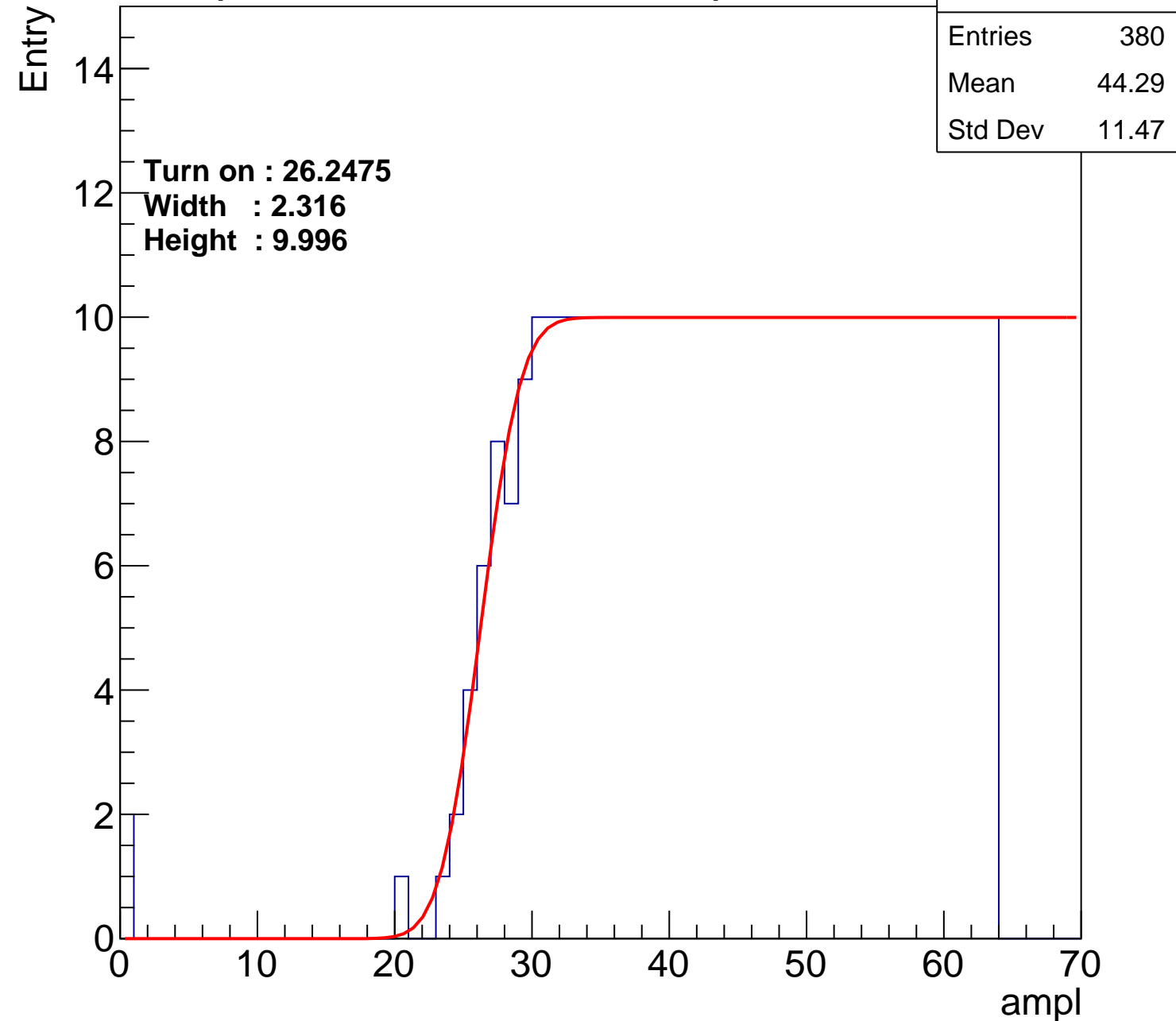
Width : 2.316

Height : 9.996

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U20-ch65

calib_packv5_042523_0143.root, FC#11, port A2

Entries	378
Mean	44.46
Std Dev	11.24

Turn on : 26.5416

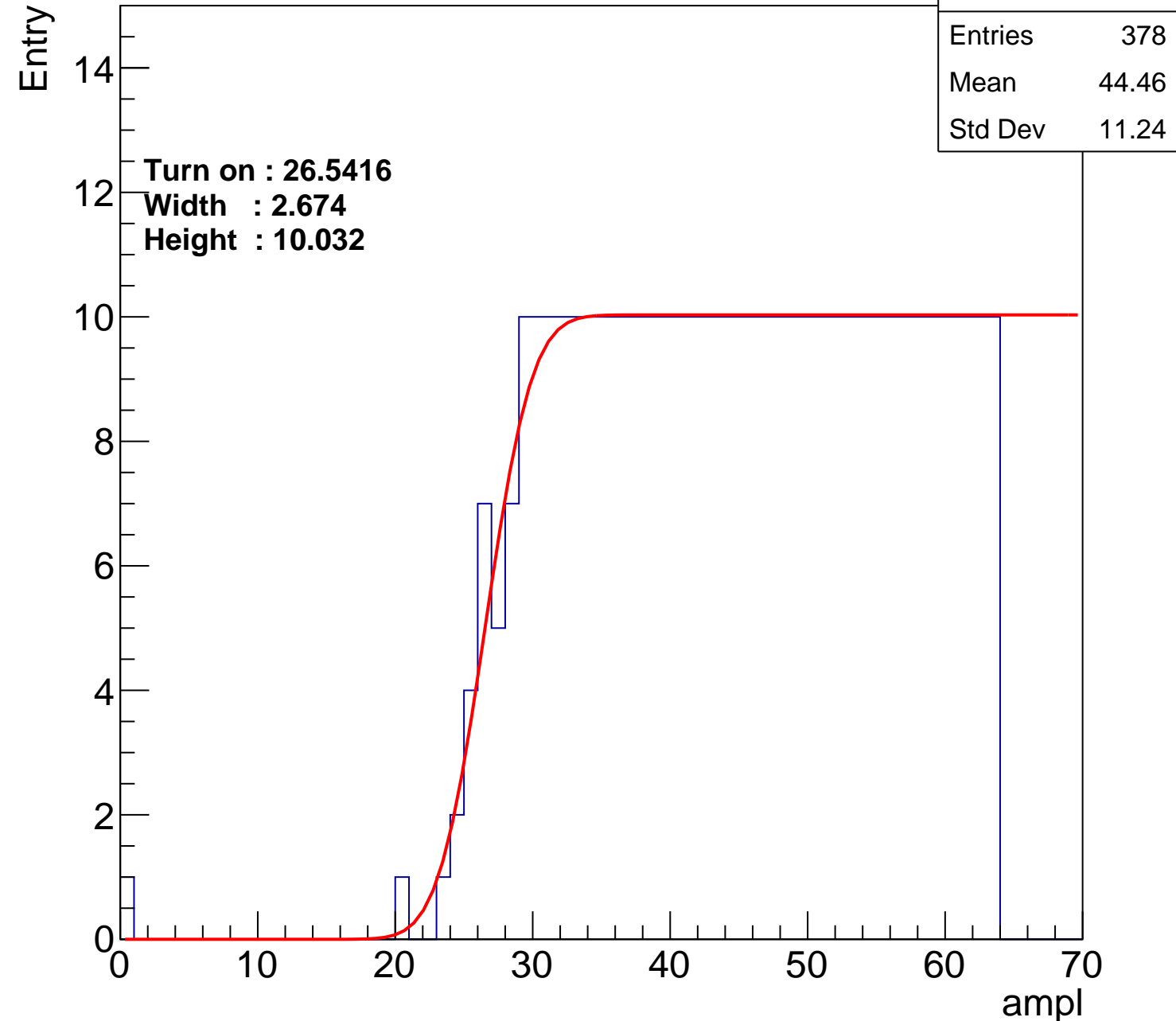
Width : 2.674

Height : 10.032

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U20-ch66

calib_packv5_042523_0143.root, FC#11, port A2

Entries	389
Mean	43.94
Std Dev	11.53

Turn on : 25.7885

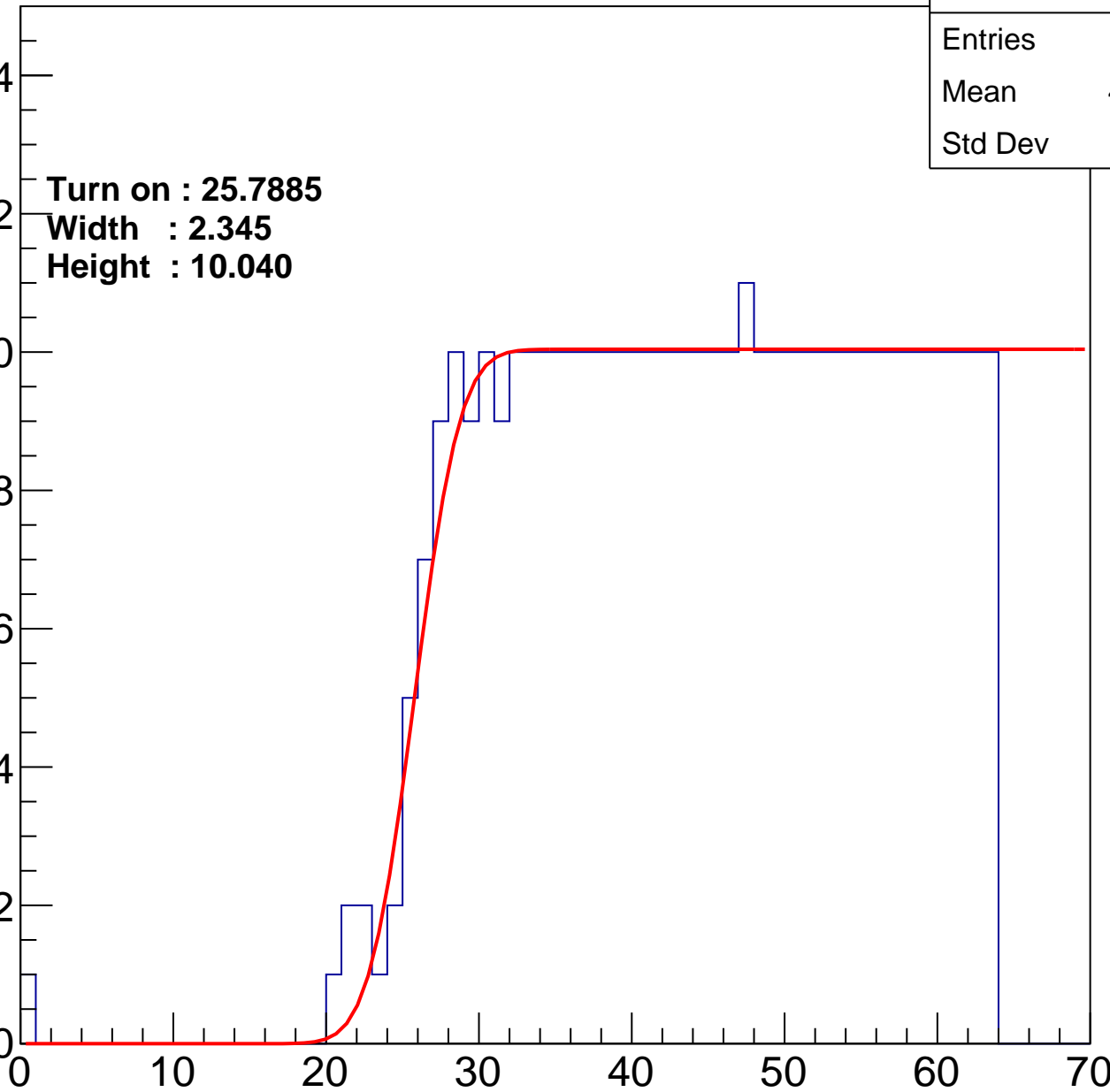
Width : 2.345

Height : 10.040

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U20-ch67

calib_packv5_042523_0143.root, FC#11, port A2

Entries	384
Mean	44.02
Std Dev	11.69

Turn on : 25.8124

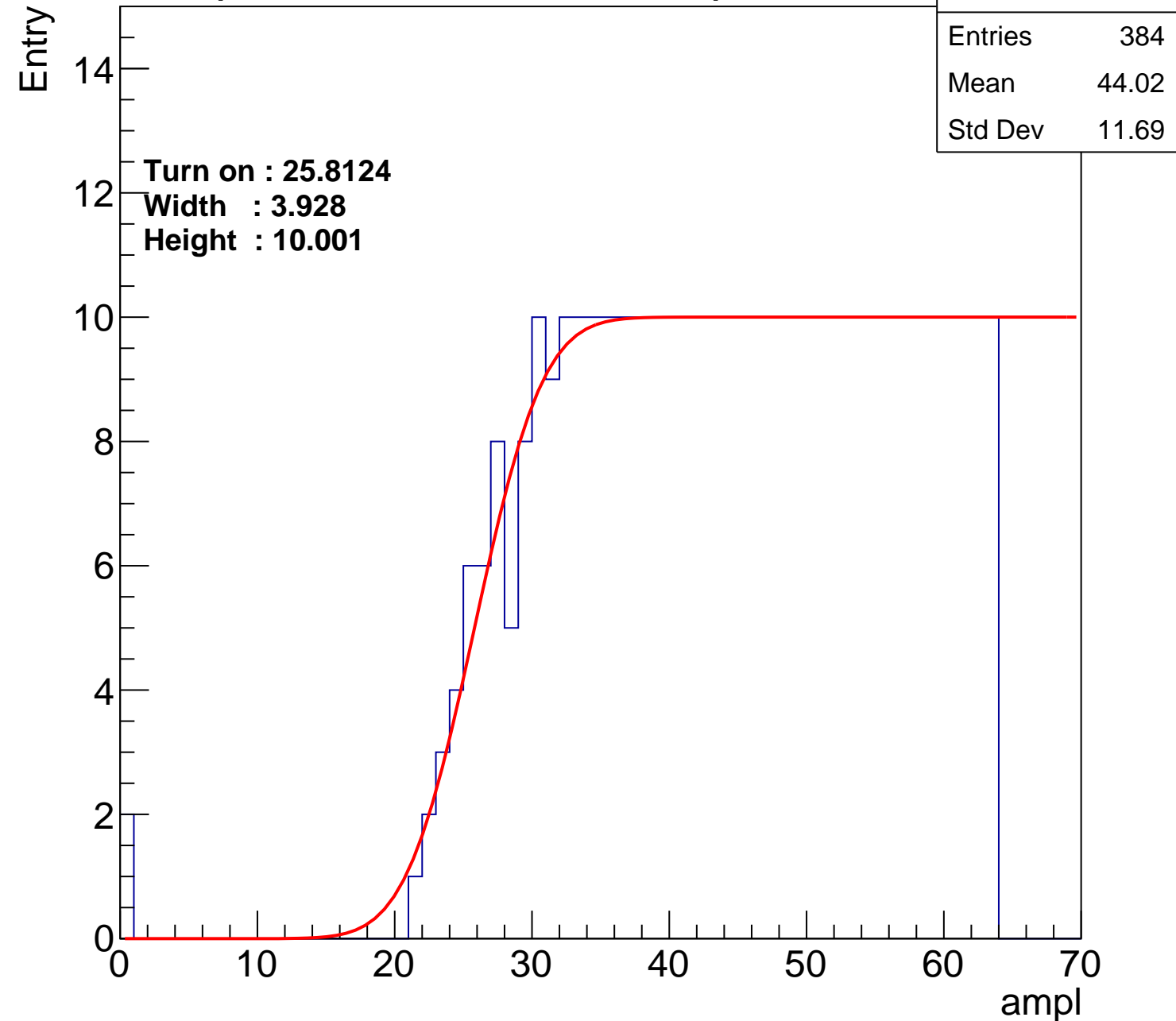
Width : 3.928

Height : 10.001

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U20-ch68

calib_packv5_042523_0143.root, FC#11, port A2

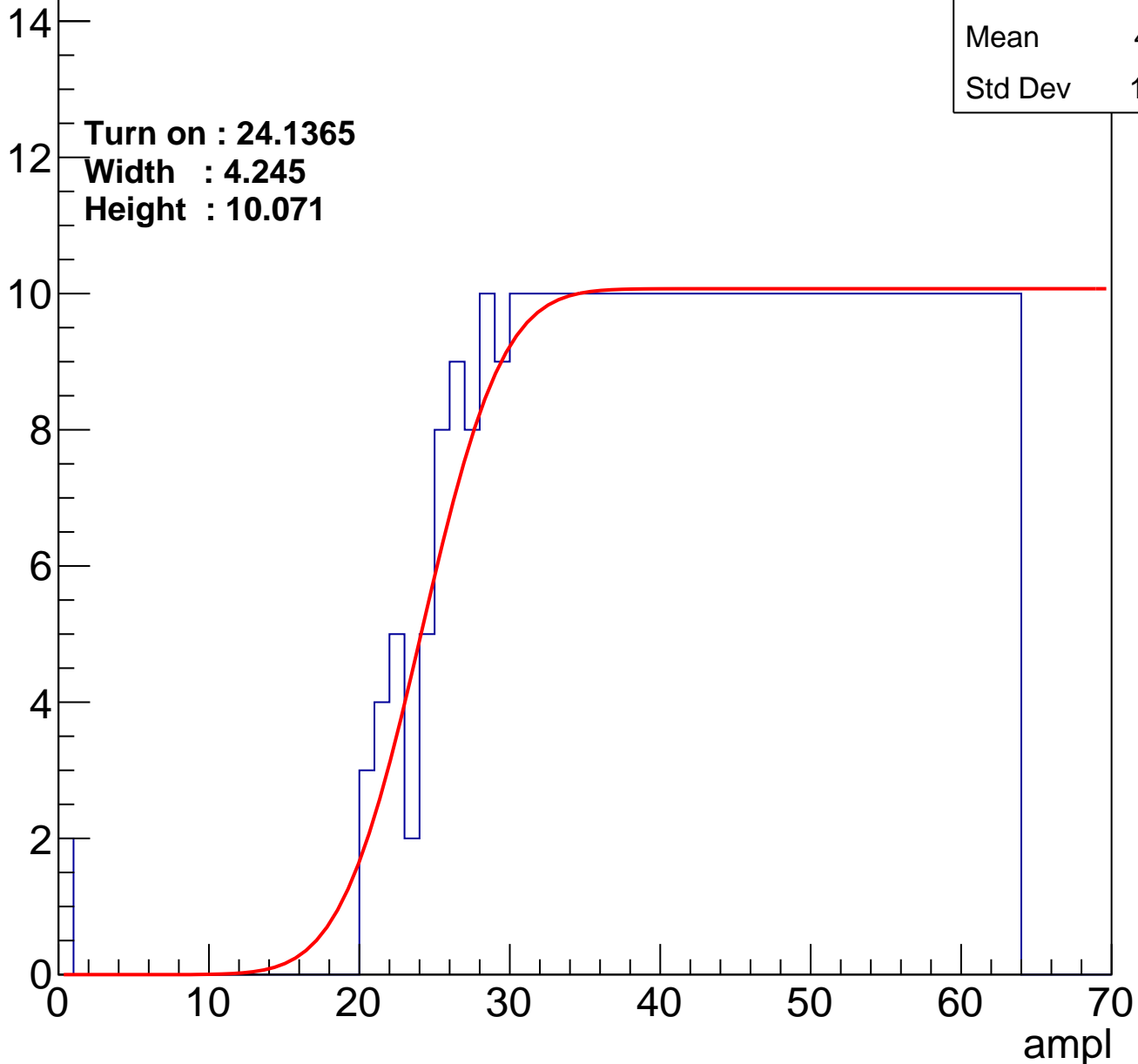
Entries	405
Mean	43.01
Std Dev	12.19

Turn on : 24.1365

Width : 4.245

Height : 10.071

Entry



B1L102S, U20-ch69

calib_packv5_042523_0143.root, FC#11, port A2

Entries	399
Mean	43.39
Std Dev	11.85

Turn on : 24.0450

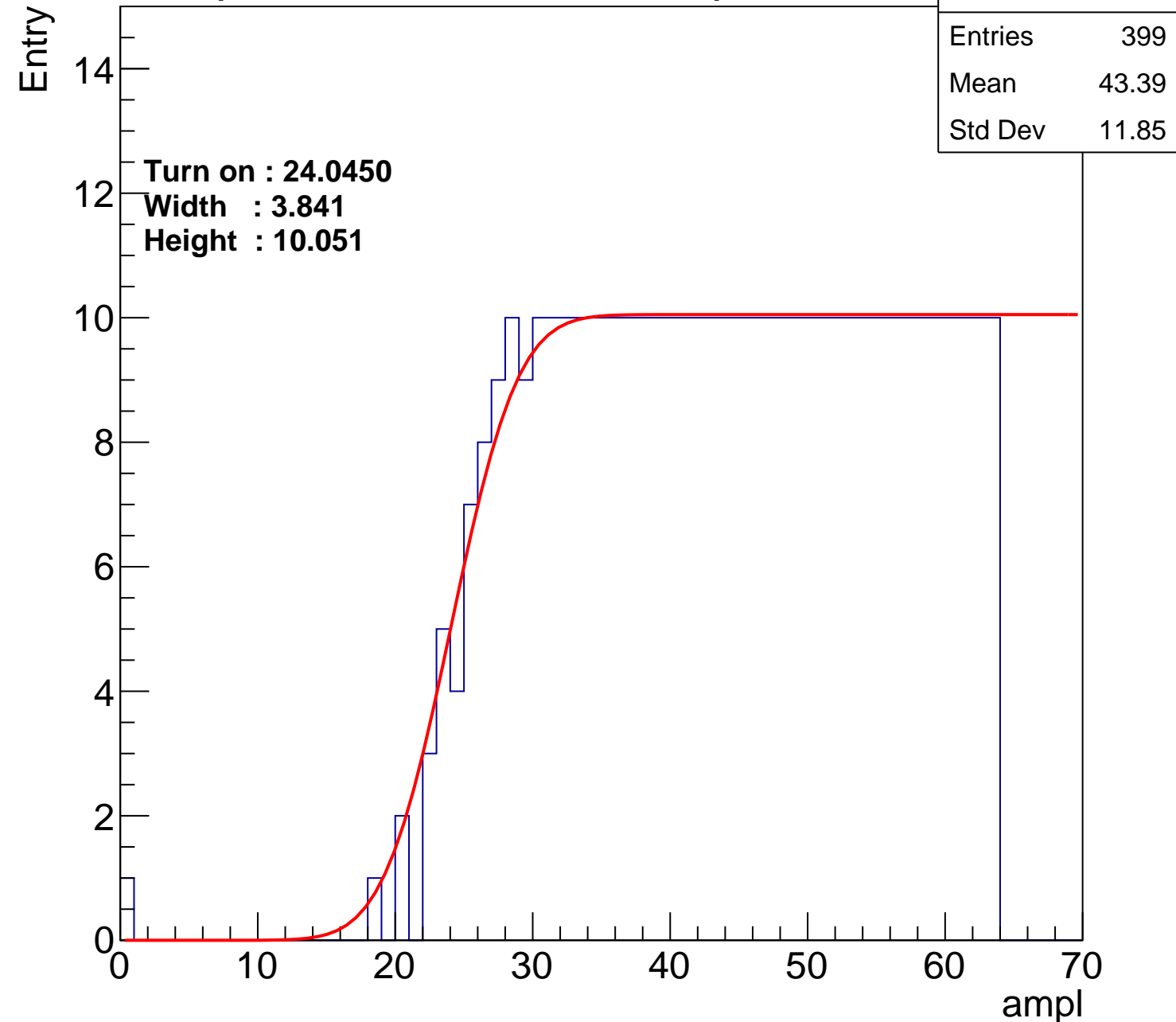
Width : 3.841

Height : 10.051

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U20-ch70

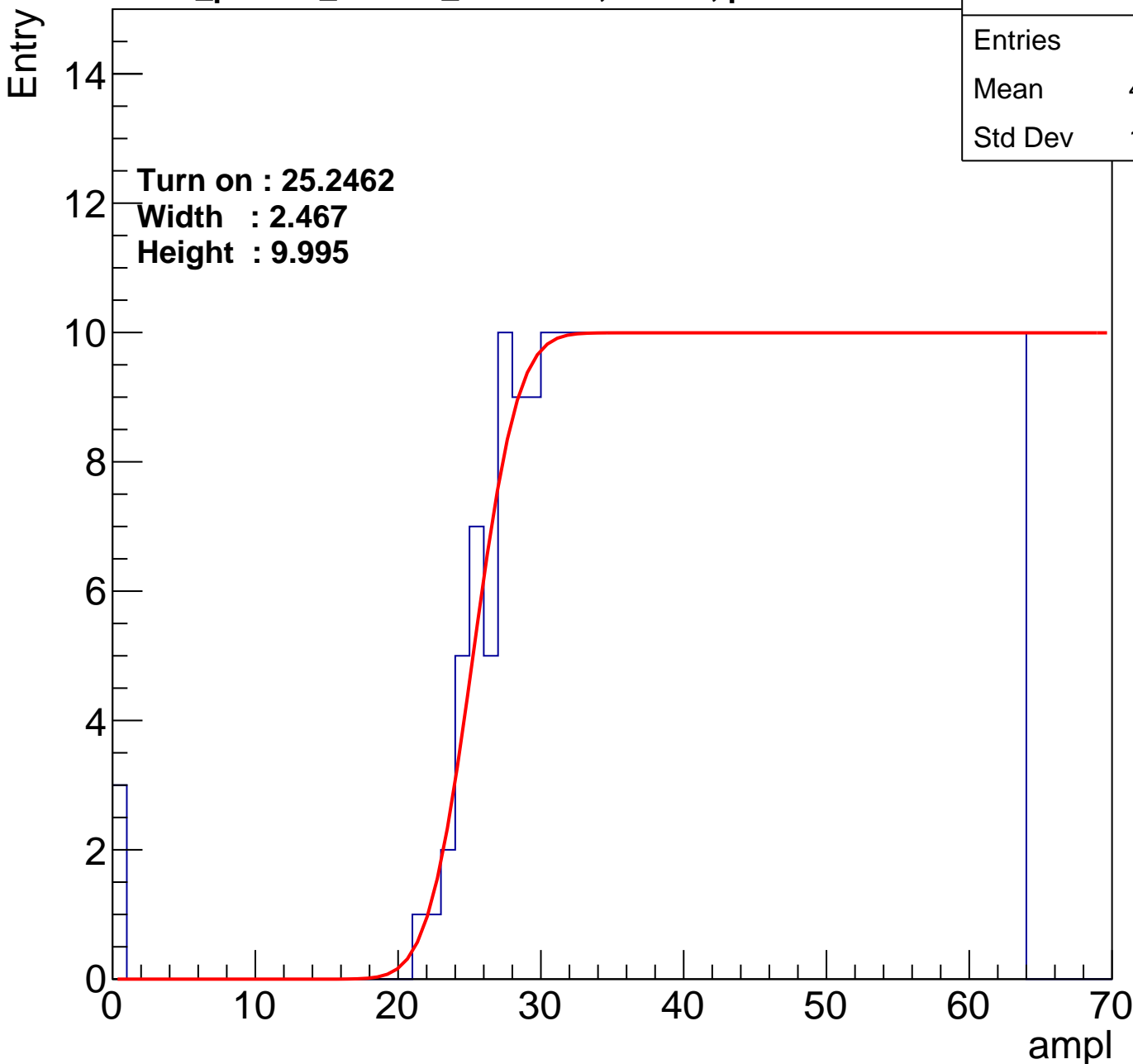
calib_packv5_042523_0143.root, FC#11, port A2

Entries	392
Mean	43.64
Std Dev	11.94

Turn on : 25.2462

Width : 2.467

Height : 9.995



B1L102S, U20-ch71

calib_packv5_042523_0143.root, FC#11, port A2

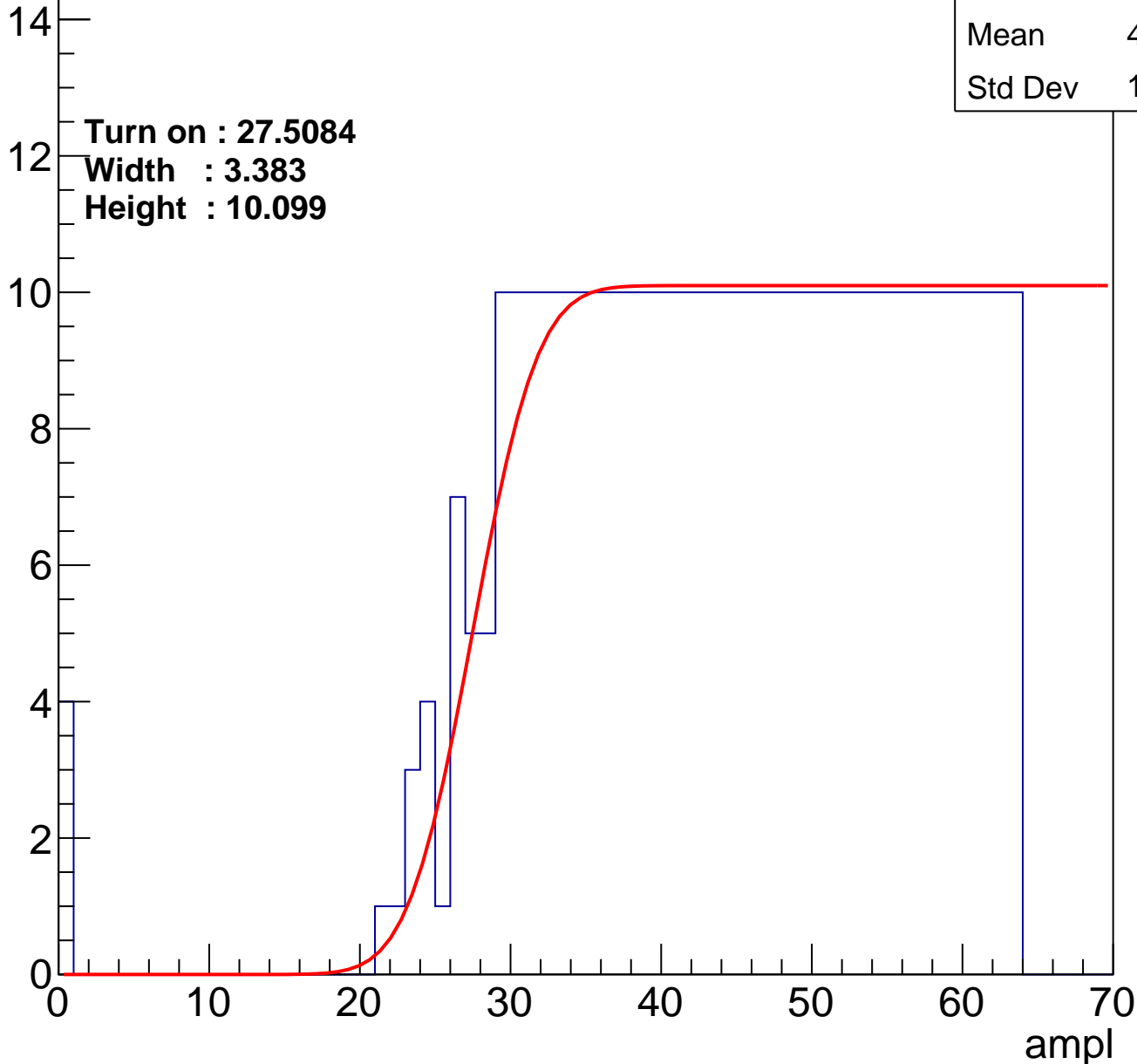
Entries	381
Mean	44.07
Std Dev	11.92

Turn on : 27.5084

Width : 3.383

Height : 10.099

Entry



B1L102S, U20-ch72

calib_packv5_042523_0143.root, FC#11, port A2

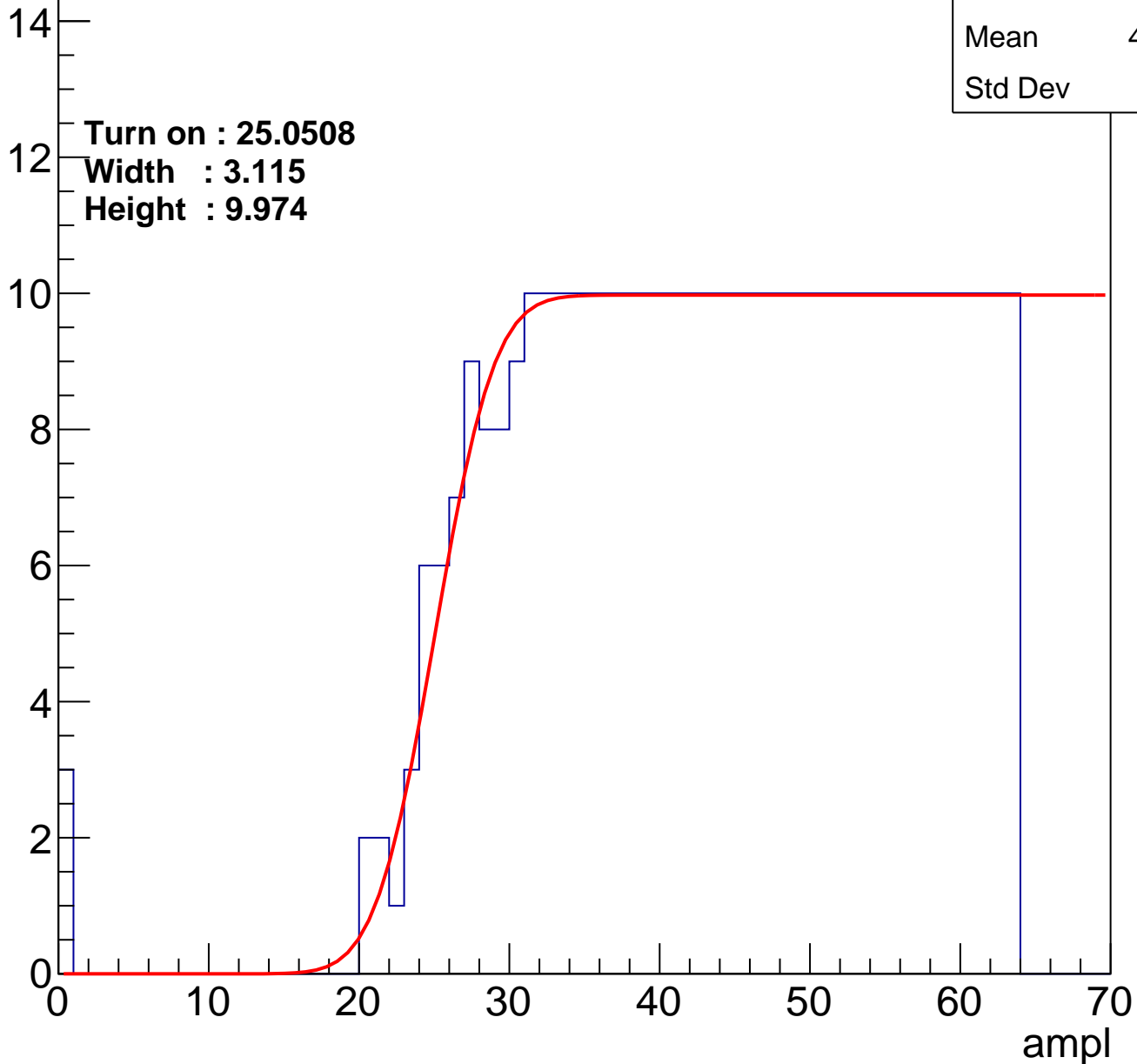
Entries	394
Mean	43.47
Std Dev	12.1

Turn on : 25.0508

Width : 3.115

Height : 9.974

Entry



B1L102S, U20-ch73

calib_packv5_042523_0143.root, FC#11, port A2

Entries	375
Mean	44.49
Std Dev	11.42

Turn on : 27.4980

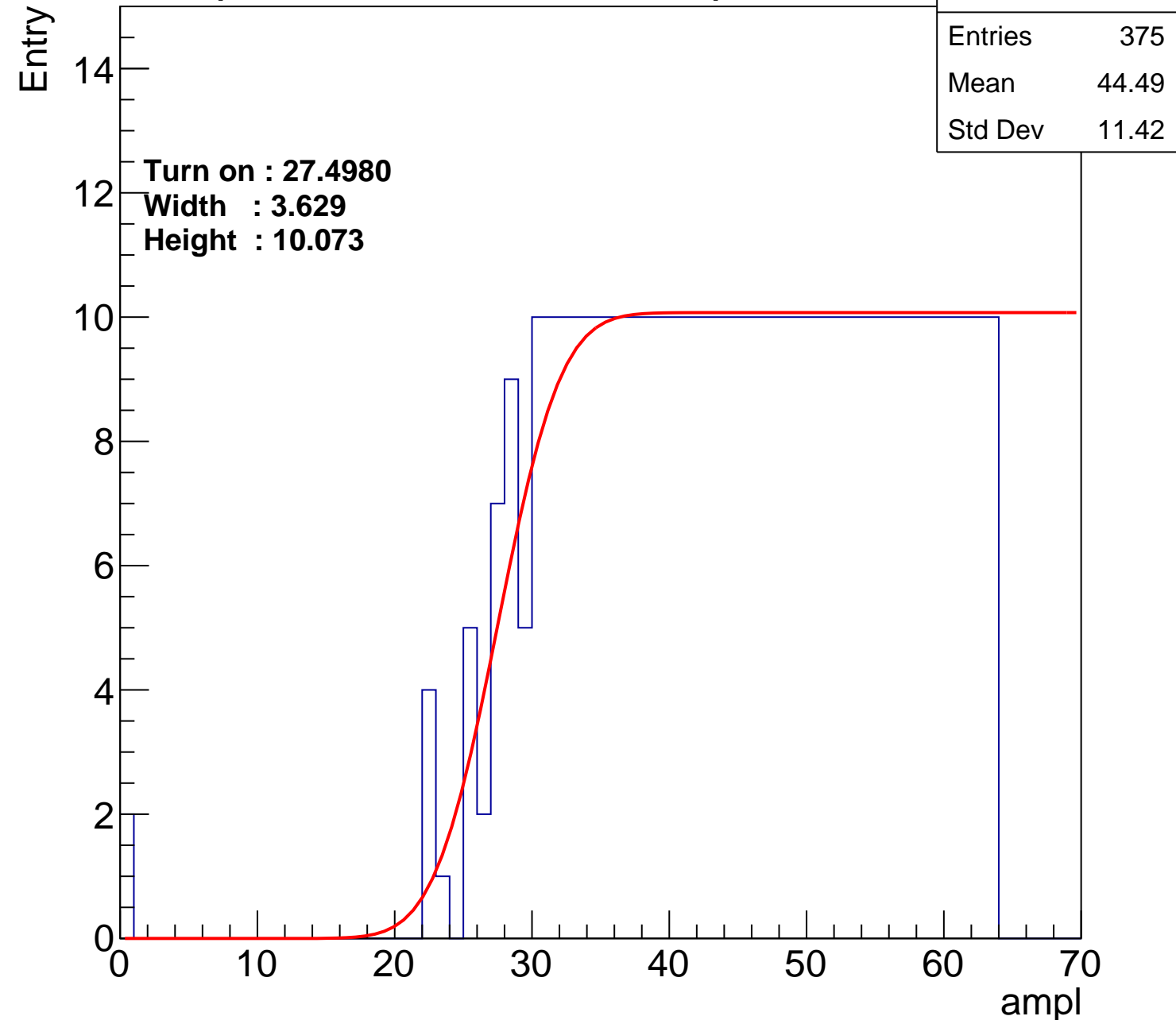
Width : 3.629

Height : 10.073

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U20-ch74

calib_packv5_042523_0143.root, FC#11, port A2

Entries	394
Mean	43.58
Std Dev	11.86

Turn on : 24.8870

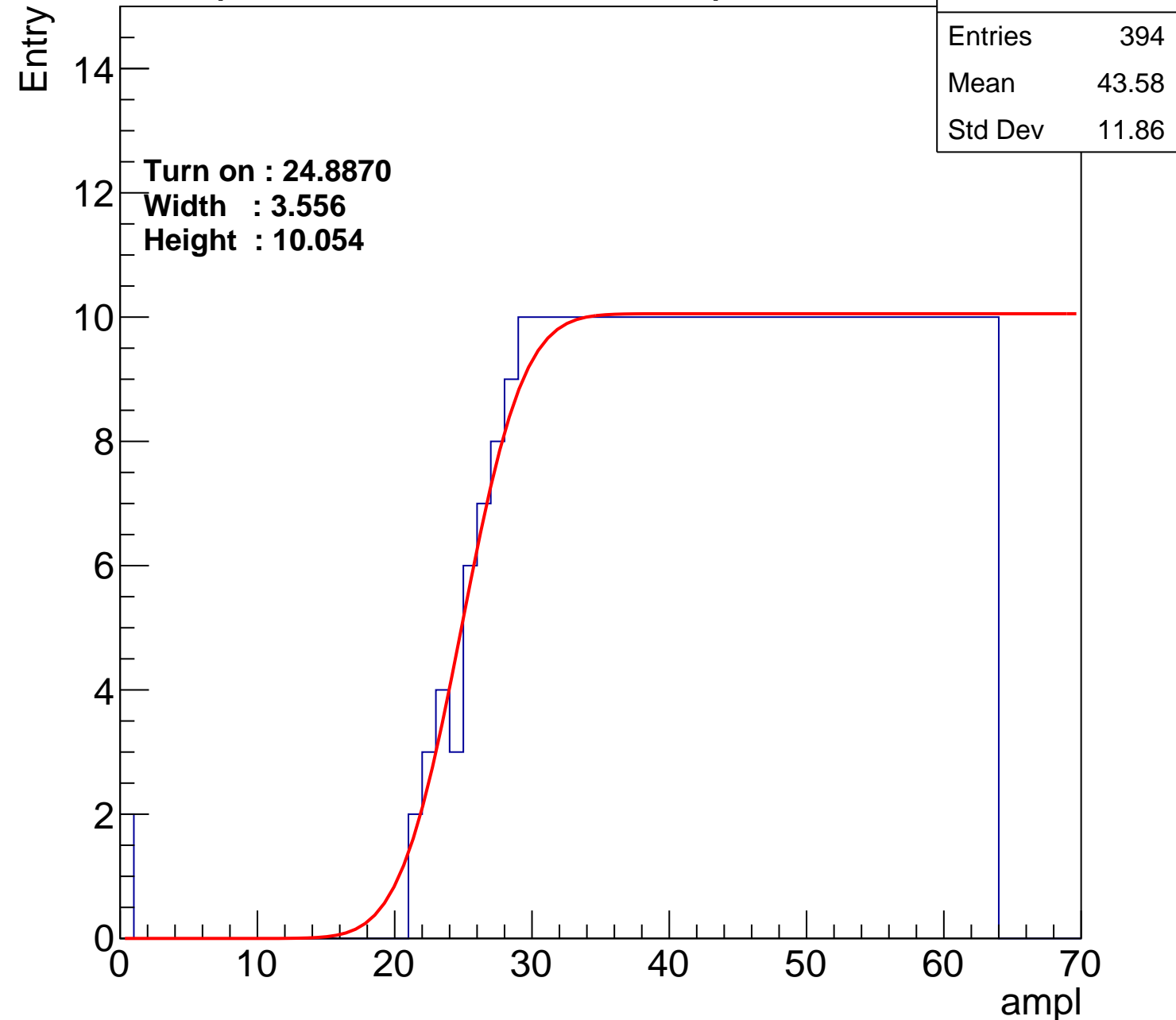
Width : 3.556

Height : 10.054

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U20-ch75

calib_packv5_042523_0143.root, FC#11, port A2

Entries	396
Mean	43.39
Std Dev	12.12

Turn on : 24.7445

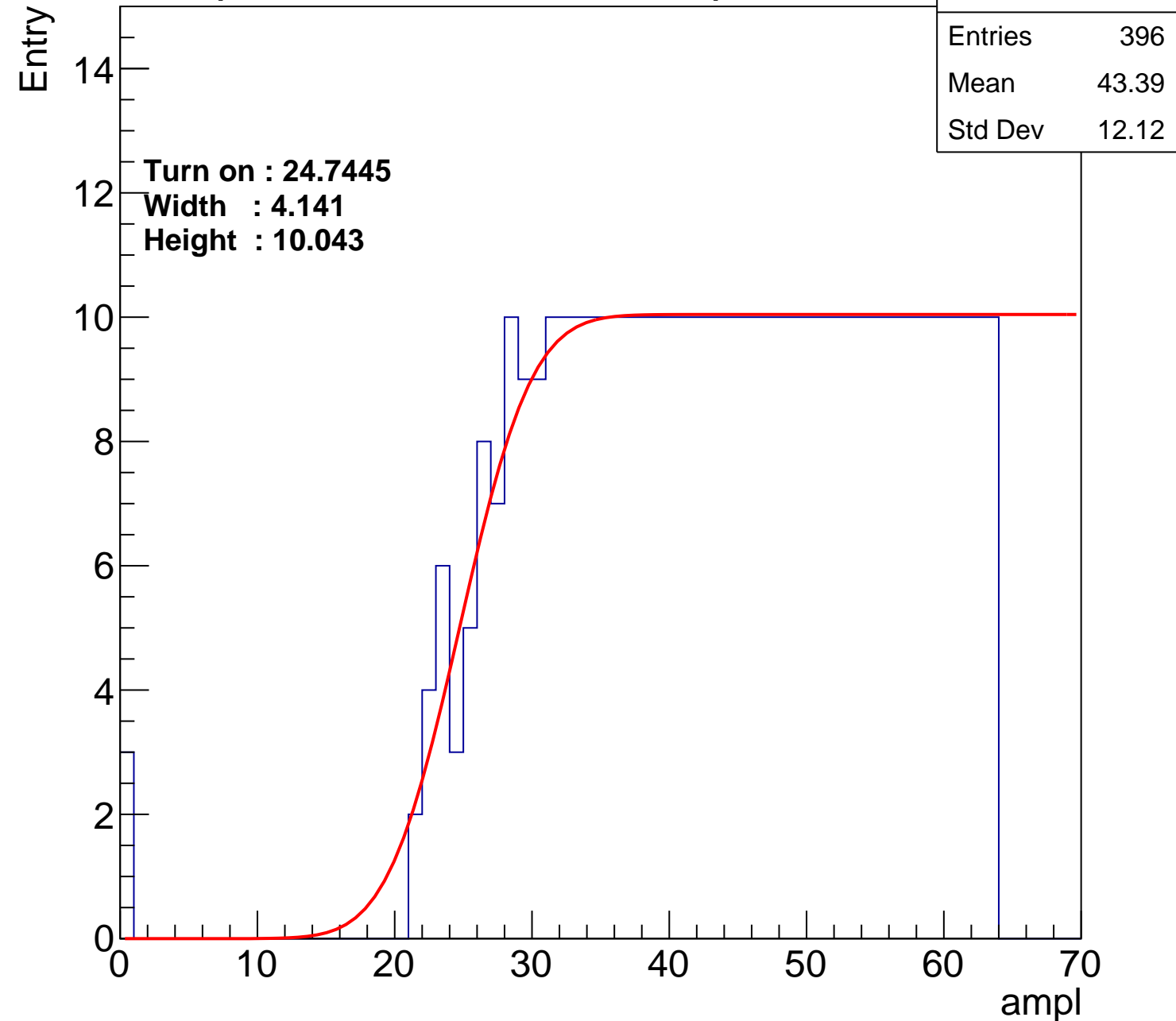
Width : 4.141

Height : 10.043

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U20-ch76

calib_packv5_042523_0143.root, FC#11, port A2

Entries	367
Mean	44.74
Std Dev	11.52

Turn on : 27.4409

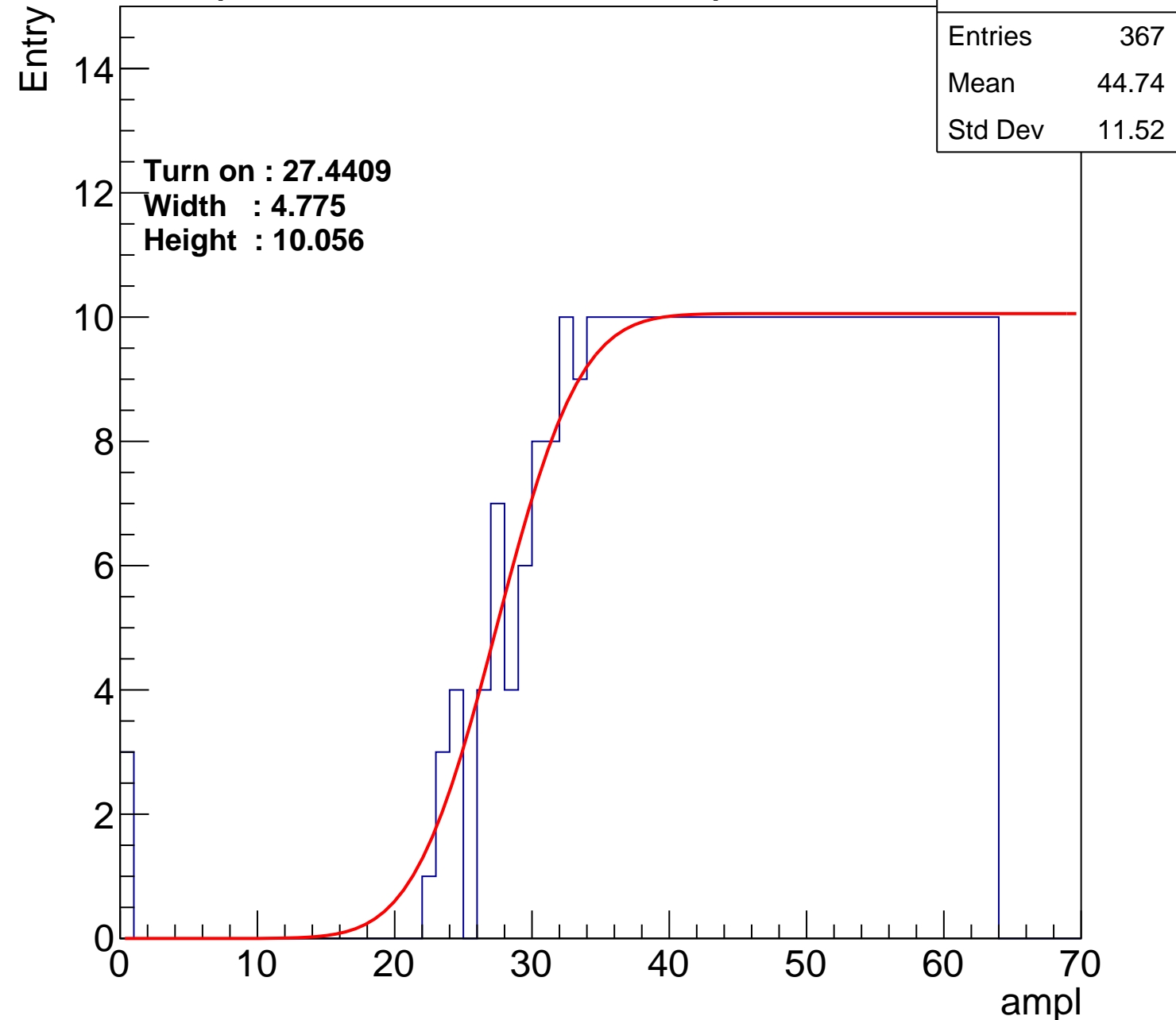
Width : 4.775

Height : 10.056

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U20-ch77

calib_packv5_042523_0143.root, FC#11, port A2

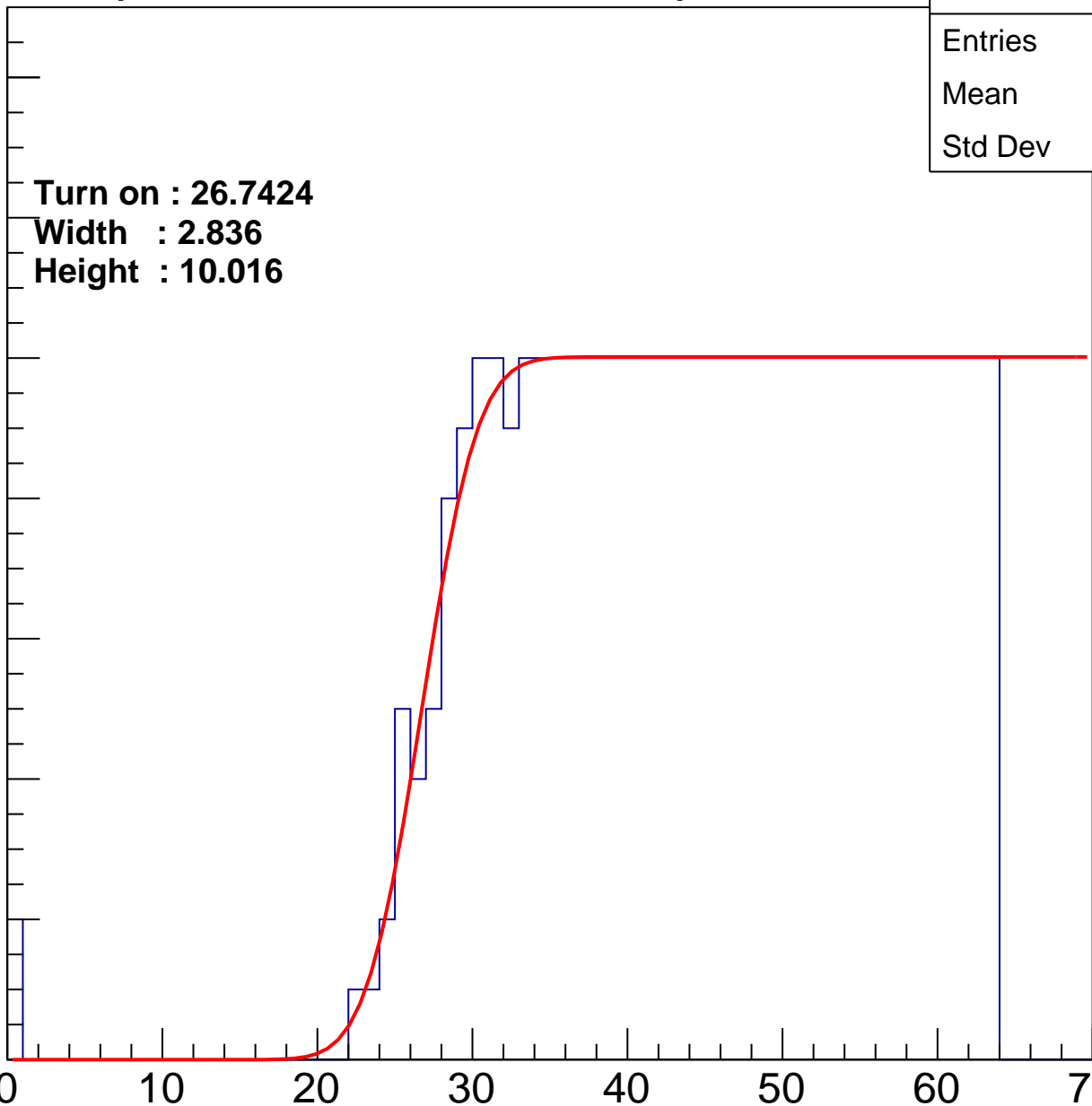
Entry

14
12
10
8
6
4
2
0

Turn on : 26.7424
Width : 2.836
Height : 10.016

Entries	376
Mean	44.47
Std Dev	11.4

ampl



B1L102S, U20-ch78

calib_packv5_042523_0143.root, FC#11, port A2

Entries	392
Mean	43.69
Std Dev	11.79

Turn on : 24.8686

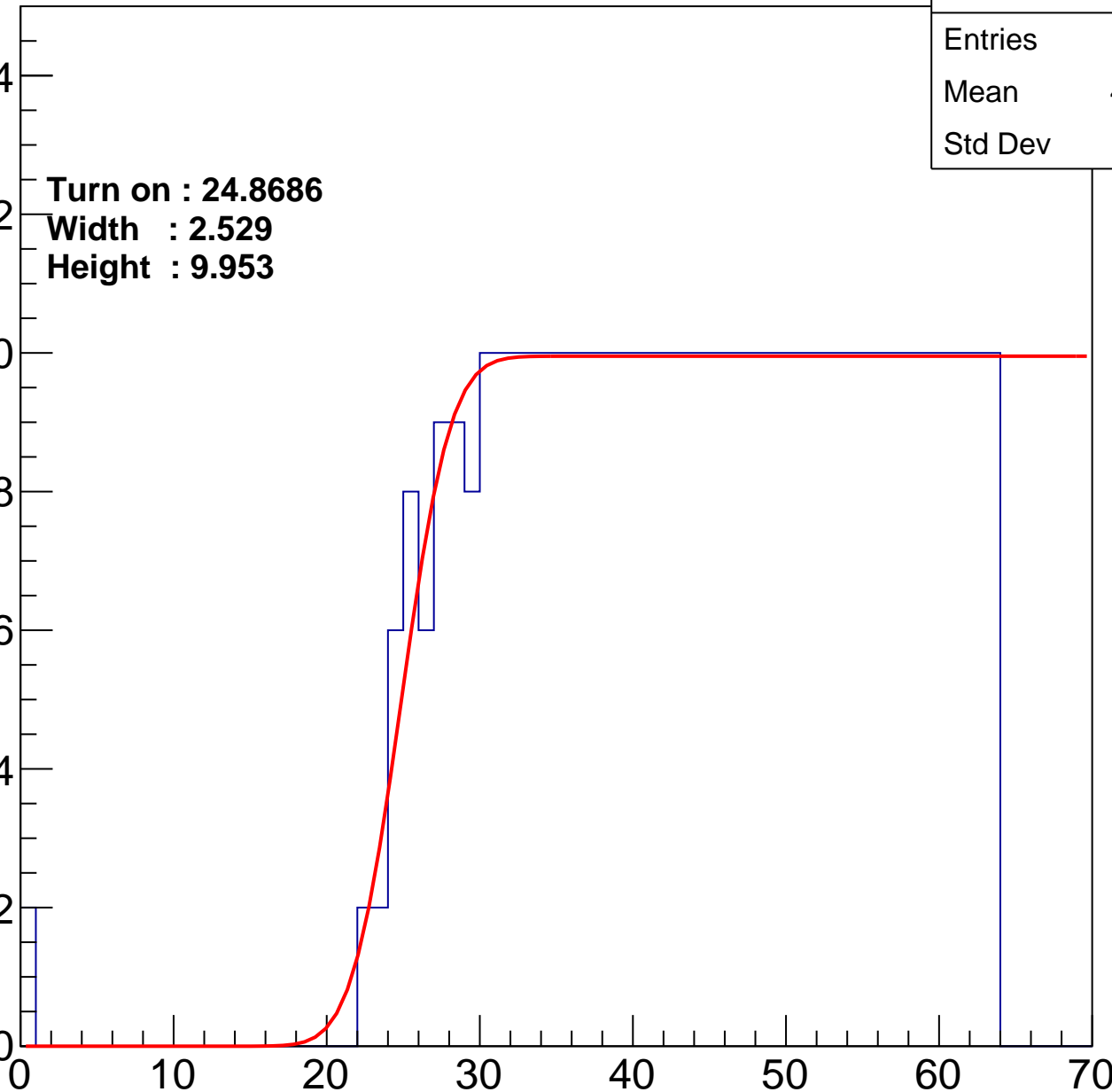
Width : 2.529

Height : 9.953

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U20-ch79

calib_packv5_042523_0143.root, FC#11, port A2

Entries	382
Mean	44.15
Std Dev	11.59

Turn on : 25.6764

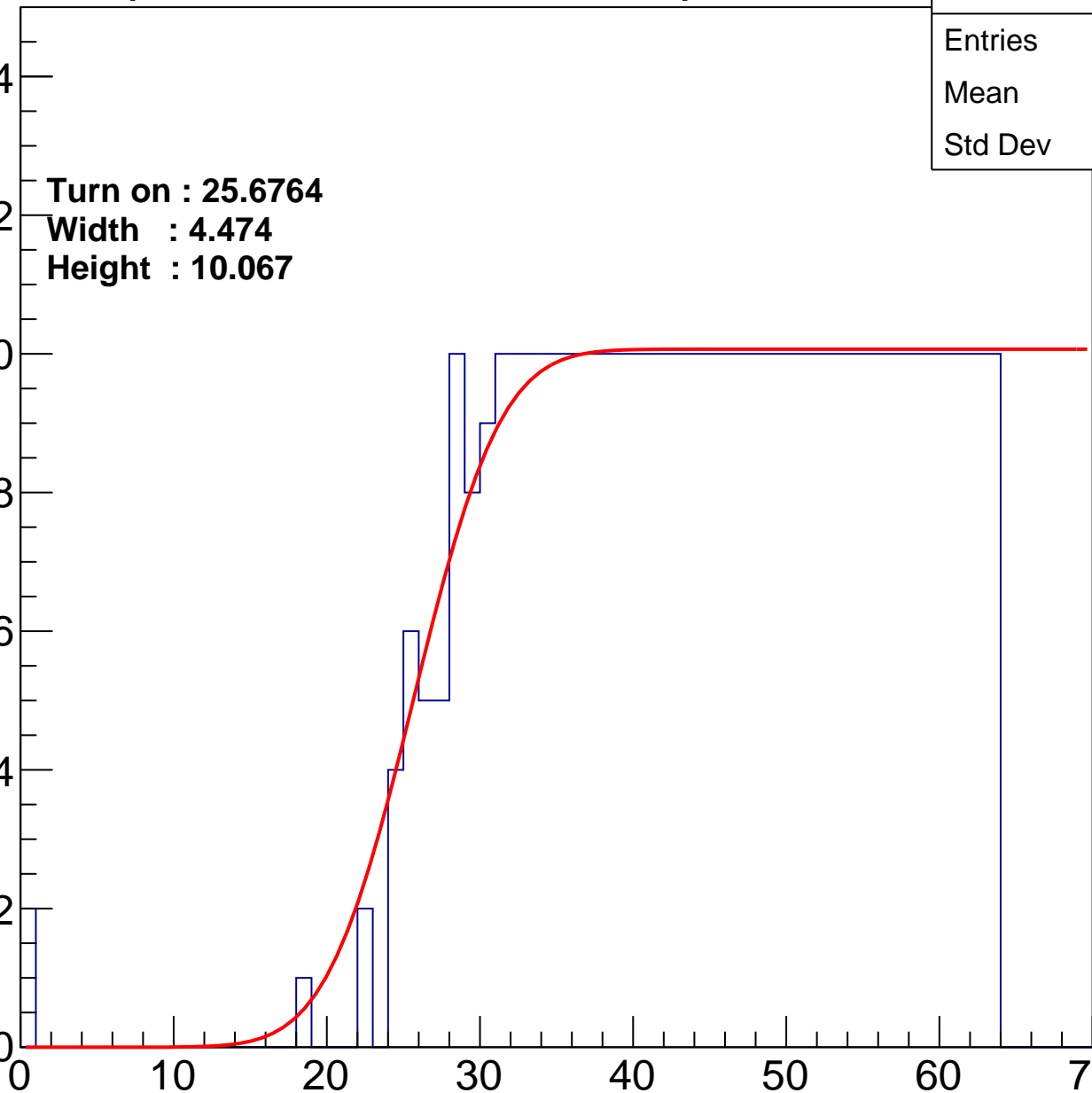
Width : 4.474

Height : 10.067

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U20-ch80

calib_packv5_042523_0143.root, FC#11, port A2

Entries	399
Mean	43.24
Std Dev	12.21

Turn on : 24.4235

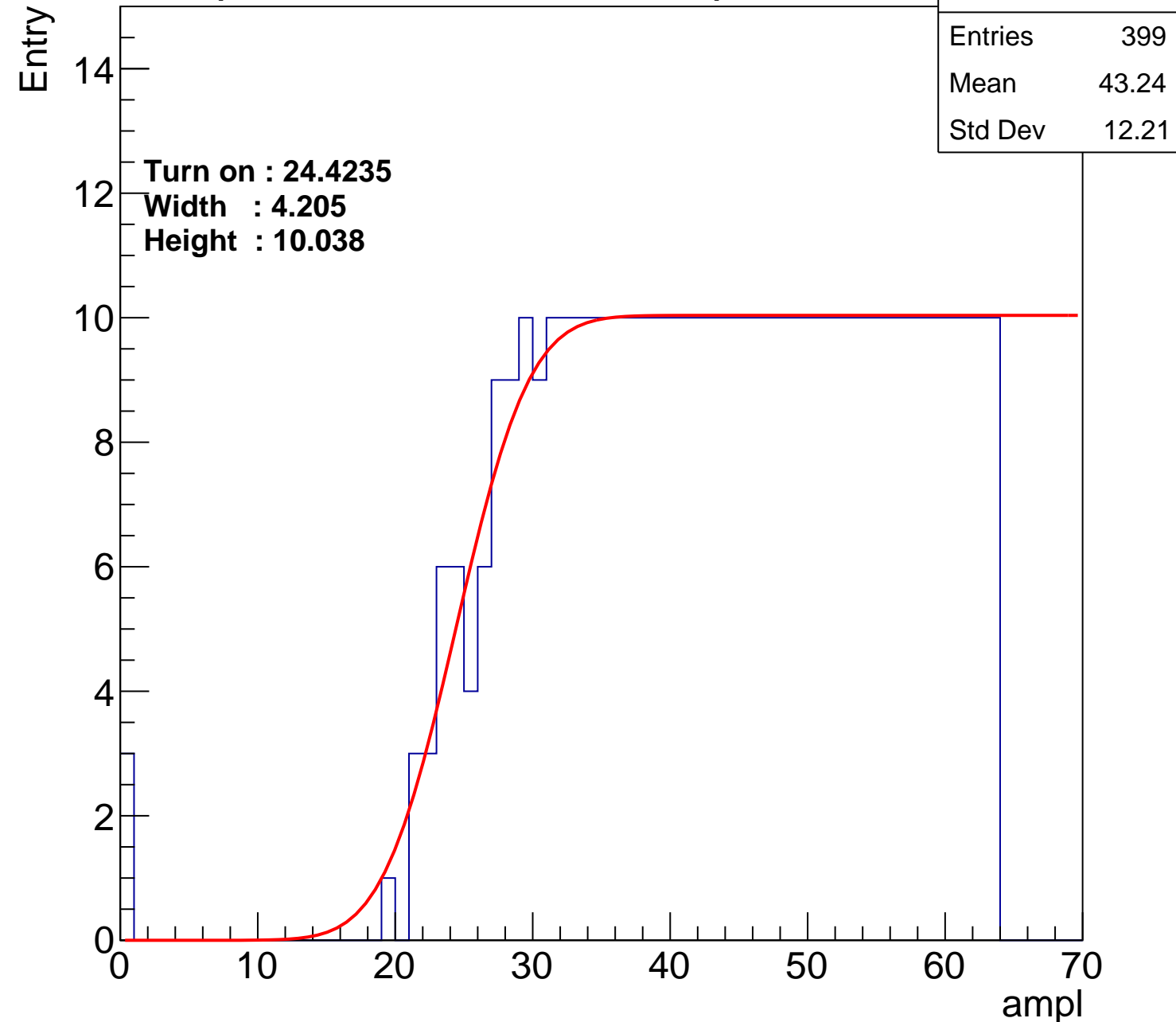
Width : 4.205

Height : 10.038

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U20-ch81

calib_packv5_042523_0143.root, FC#11, port A2

Entries	387
Mean	43.9
Std Dev	11.79

Turn on : 25.5164

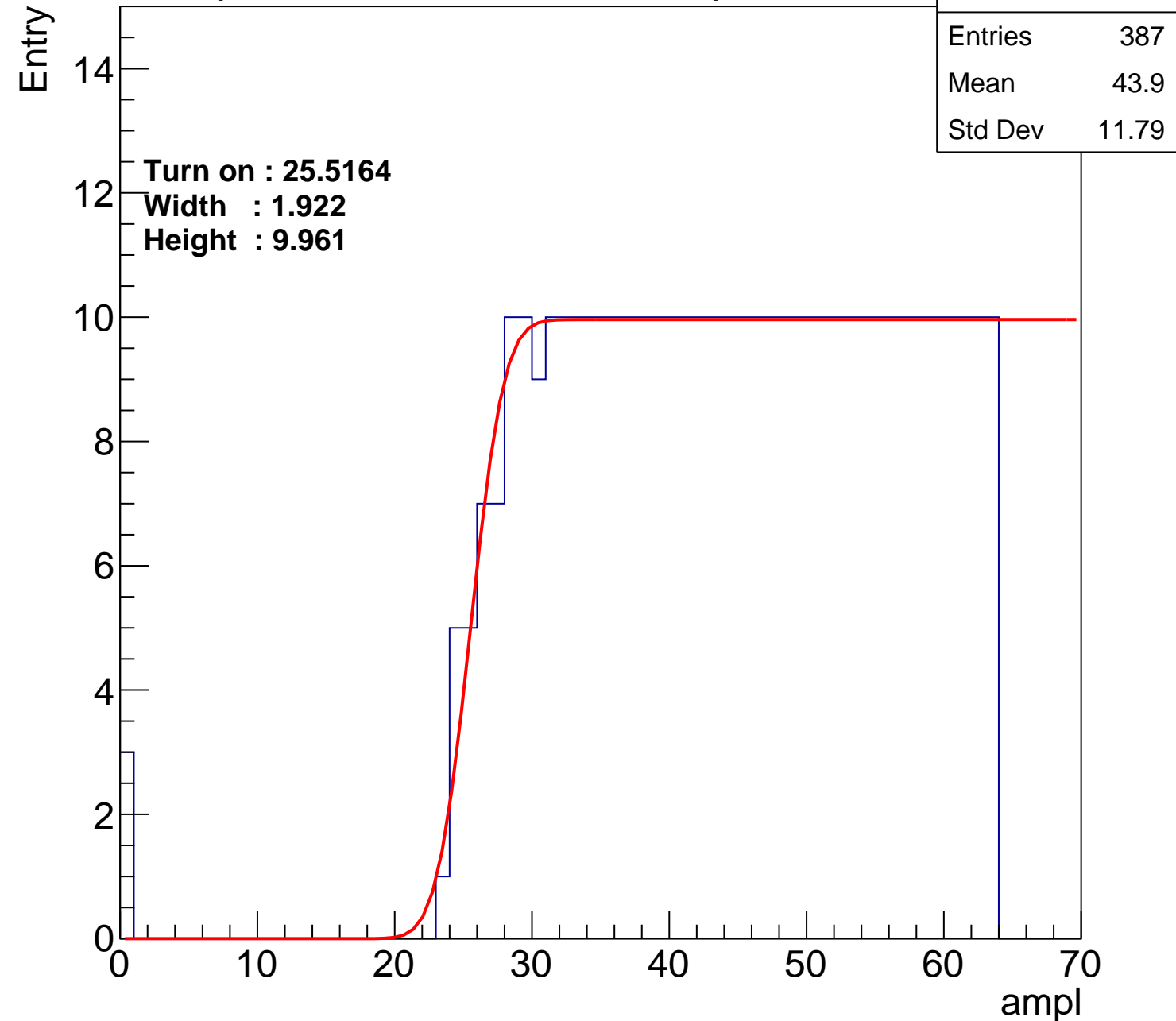
Width : 1.922

Height : 9.961

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U20-ch82

calib_packv5_042523_0143.root, FC#11, port A2

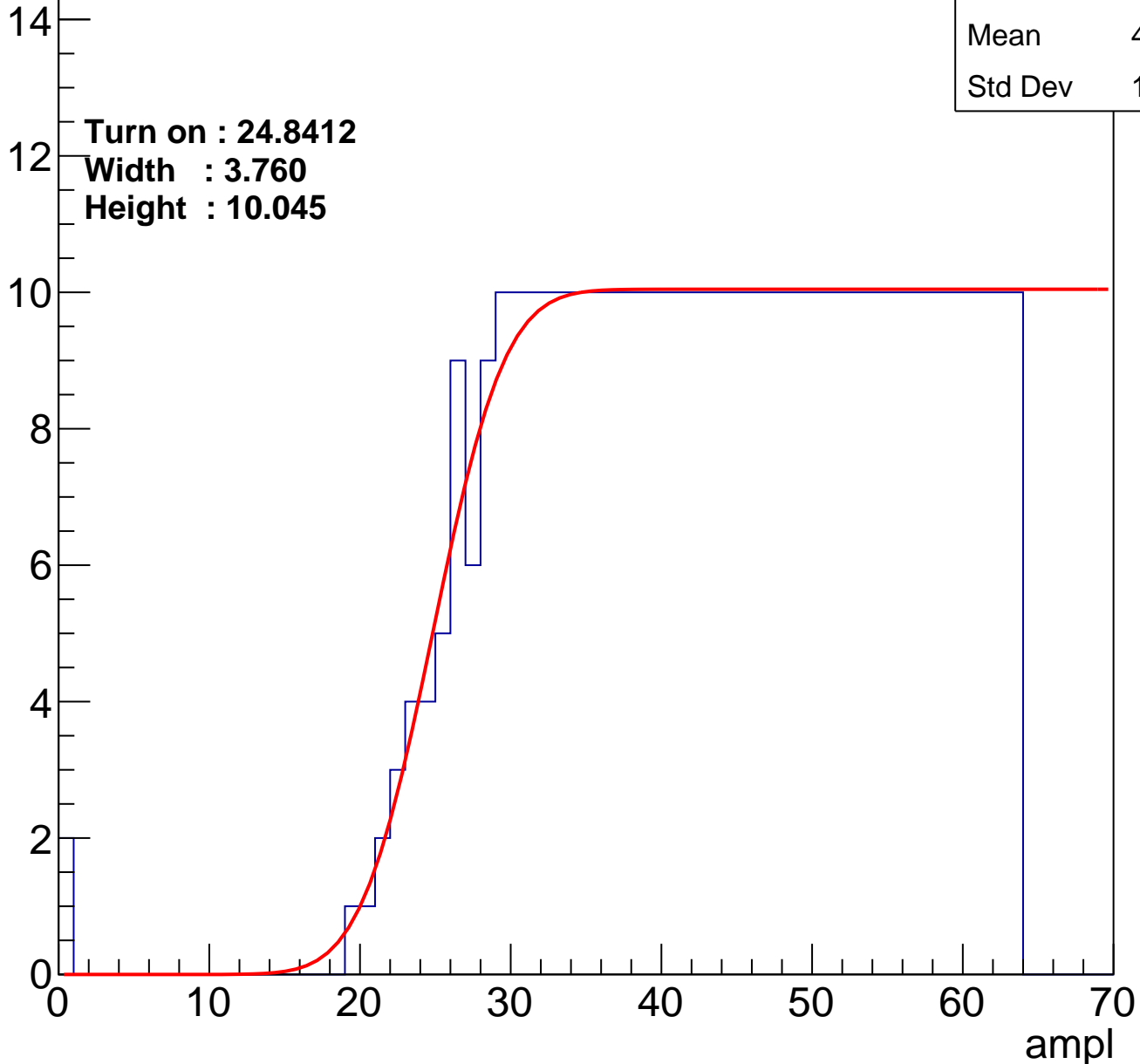
Entries	396
Mean	43.45
Std Dev	11.96

Turn on : 24.8412

Width : 3.760

Height : 10.045

Entry



B1L102S, U20-ch83

calib_packv5_042523_0143.root, FC#11, port A2

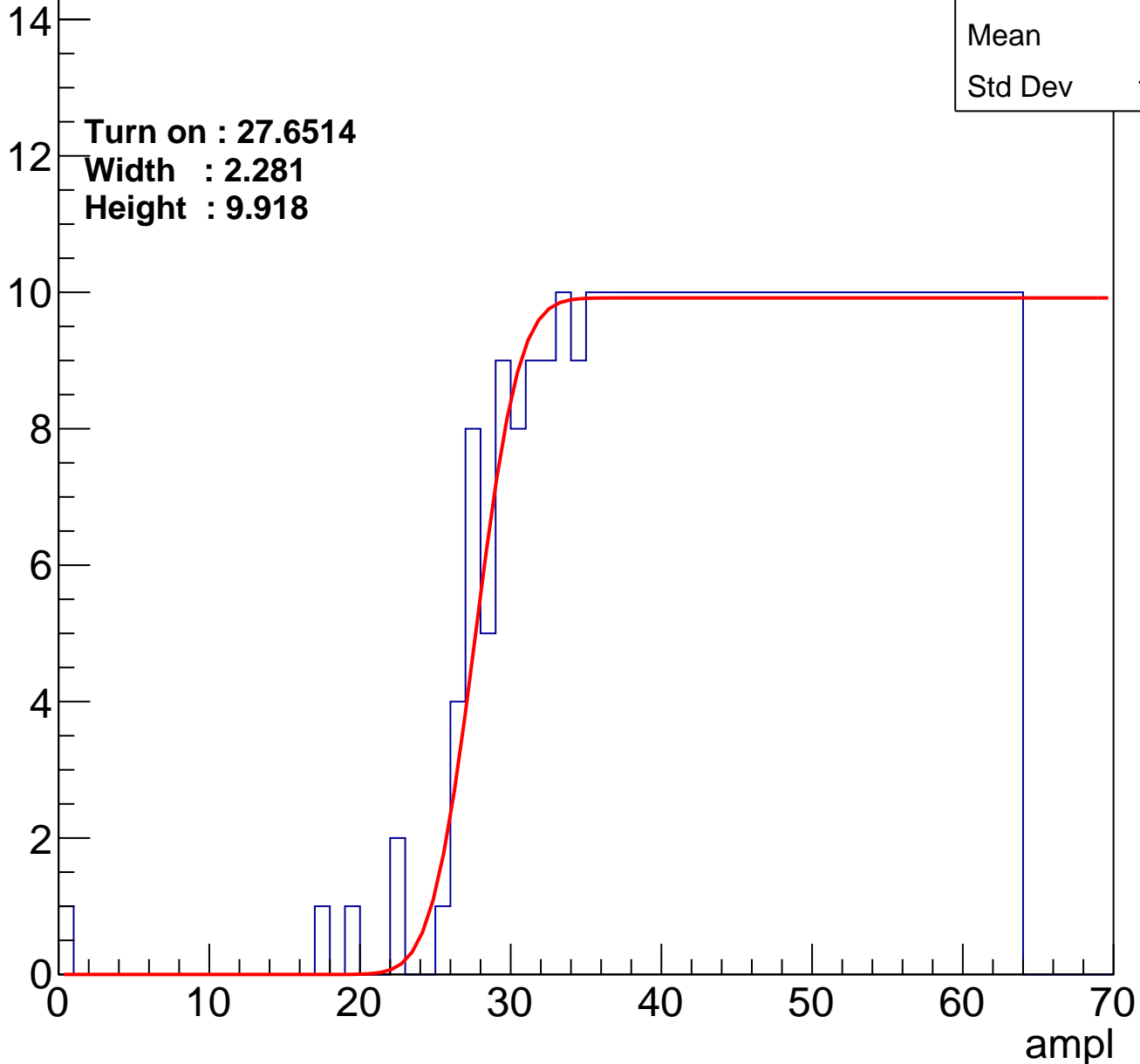
Entry

Entries	367
Mean	44.9
Std Dev	11.11

Turn on : 27.6514

Width : 2.281

Height : 9.918



B1L102S, U20-ch84

calib_packv5_042523_0143.root, FC#11, port A2

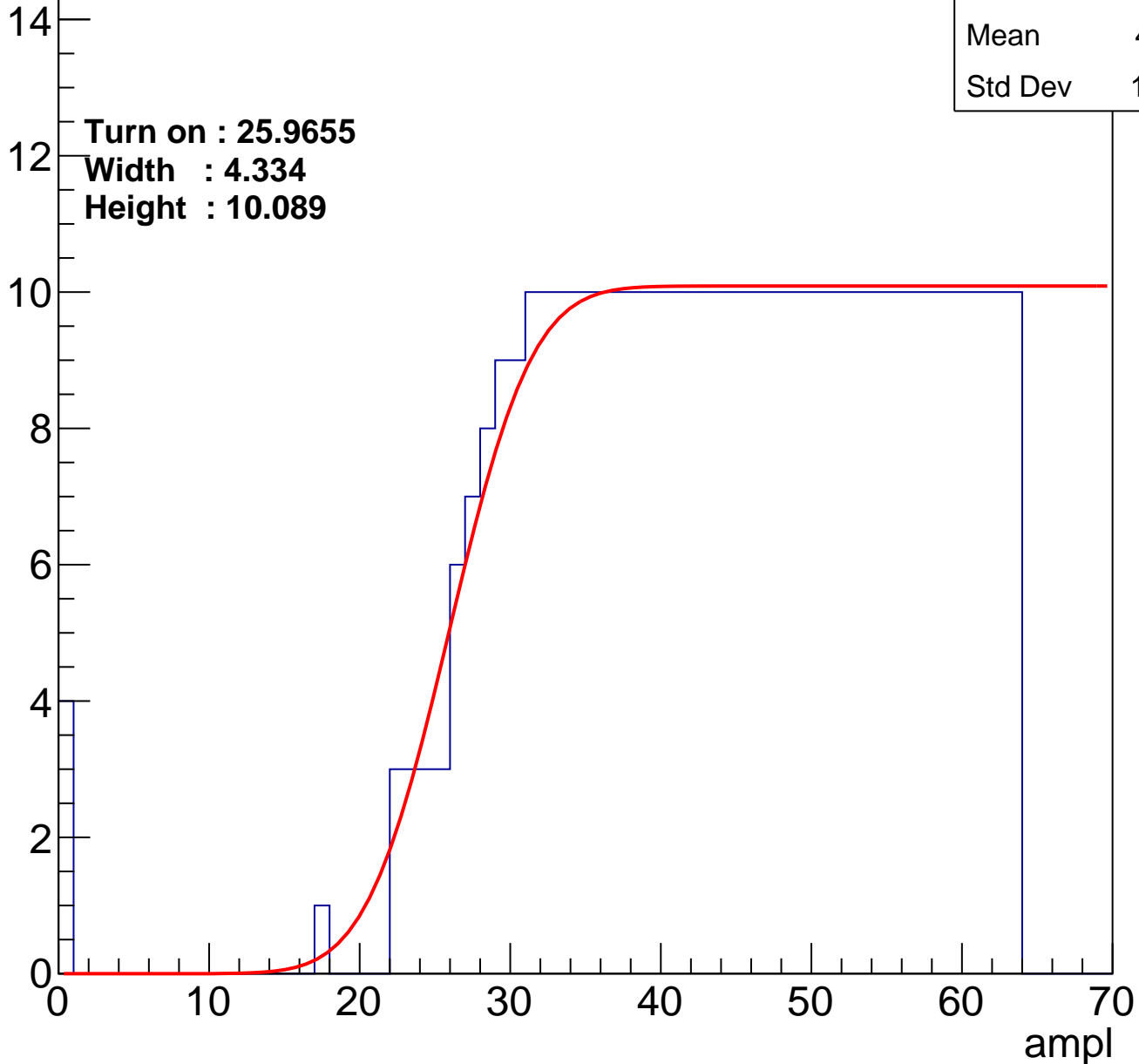
Entries	386
Mean	43.81
Std Dev	12.07

Turn on : 25.9655

Width : 4.334

Height : 10.089

Entry



B1L102S, U20-ch85

calib_packv5_042523_0143.root, FC#11, port A2

Entries	390
Mean	43.71
Std Dev	11.94

Turn on : 25.2330

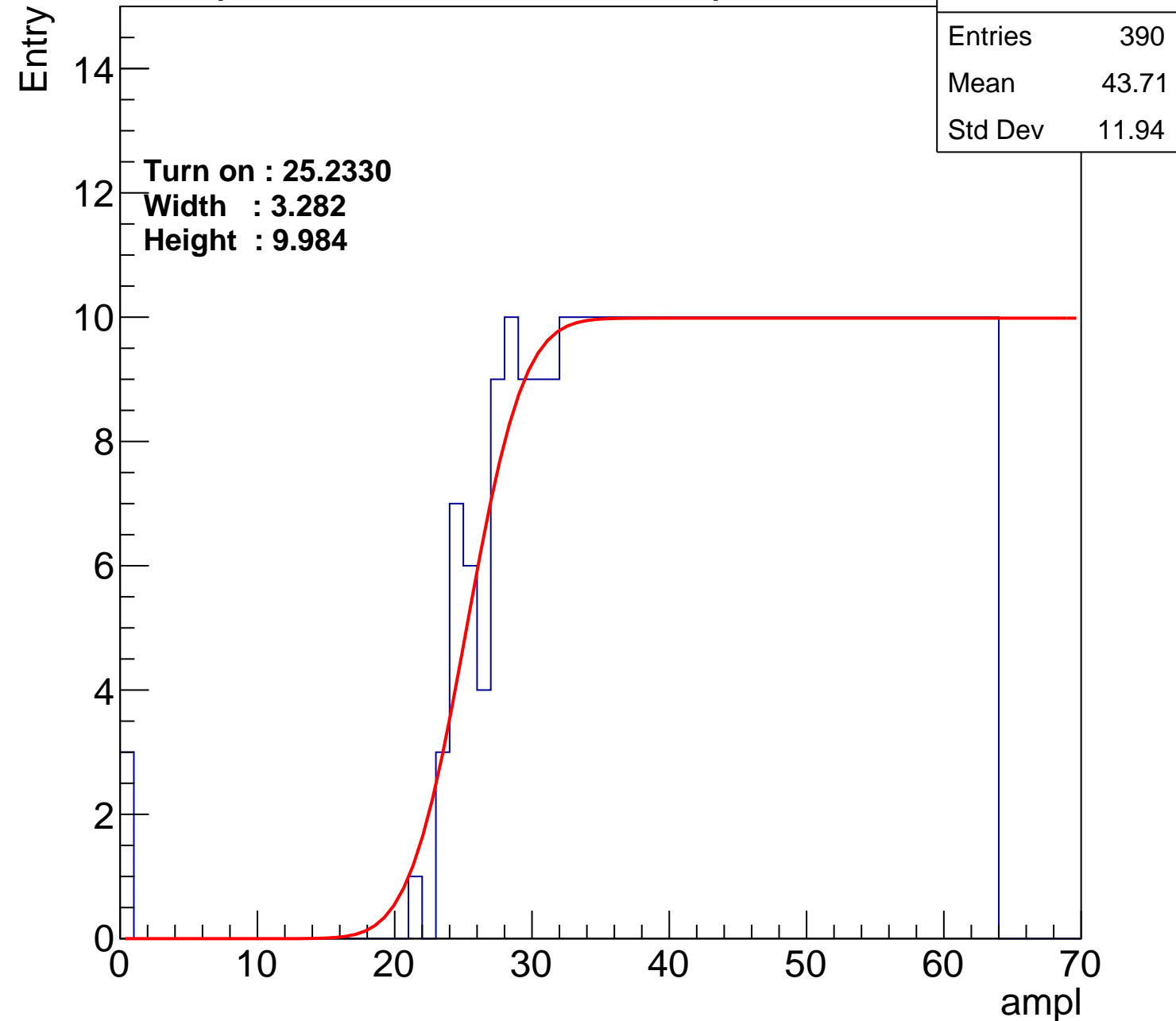
Width : 3.282

Height : 9.984

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U20-ch86

calib_packv5_042523_0143.root, FC#11, port A2

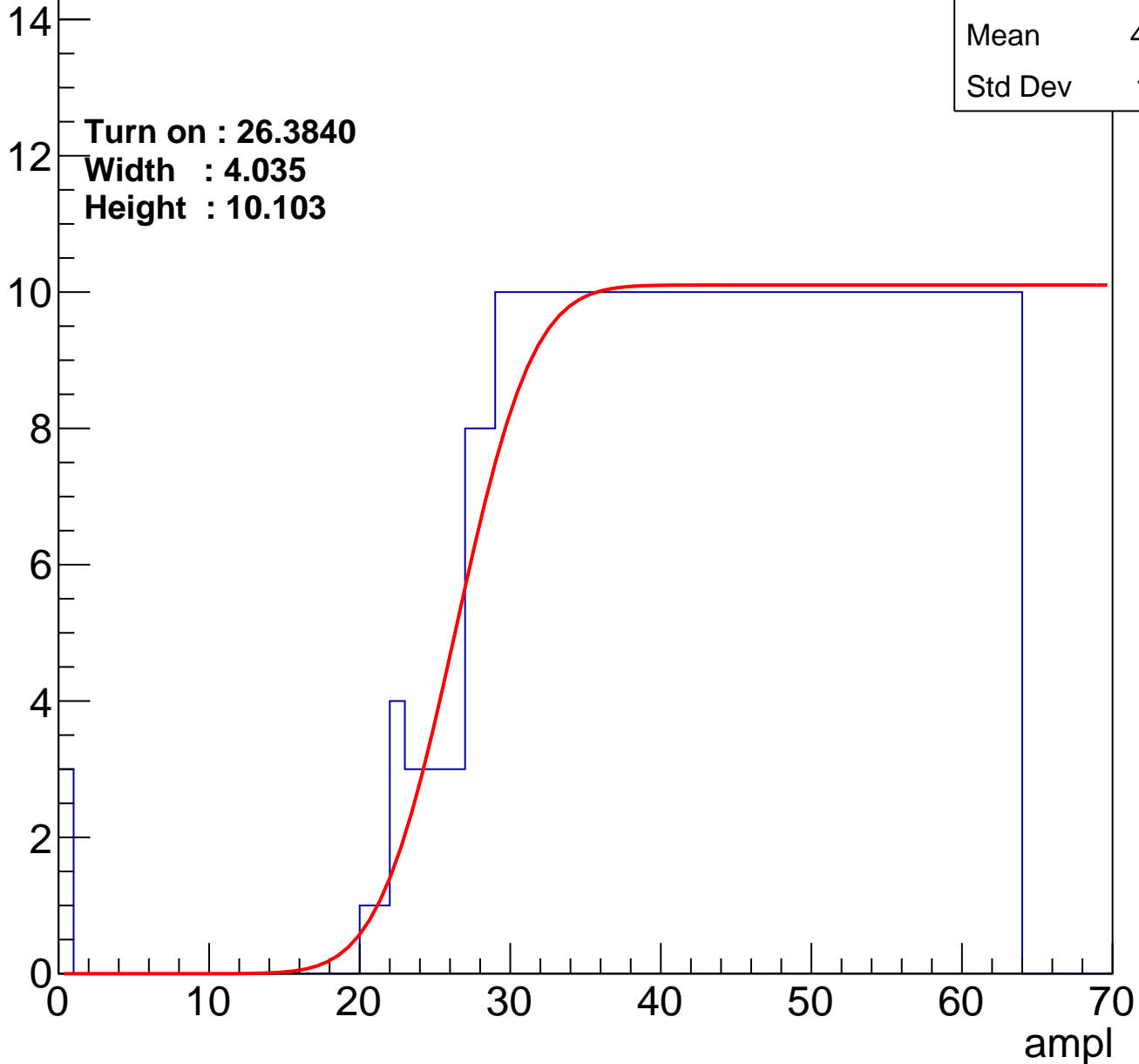
Entries	387
Mean	43.83
Std Dev	11.91

Turn on : 26.3840

Width : 4.035

Height : 10.103

Entry



B1L102S, U20-ch87

calib_packv5_042523_0143.root, FC#11, port A2

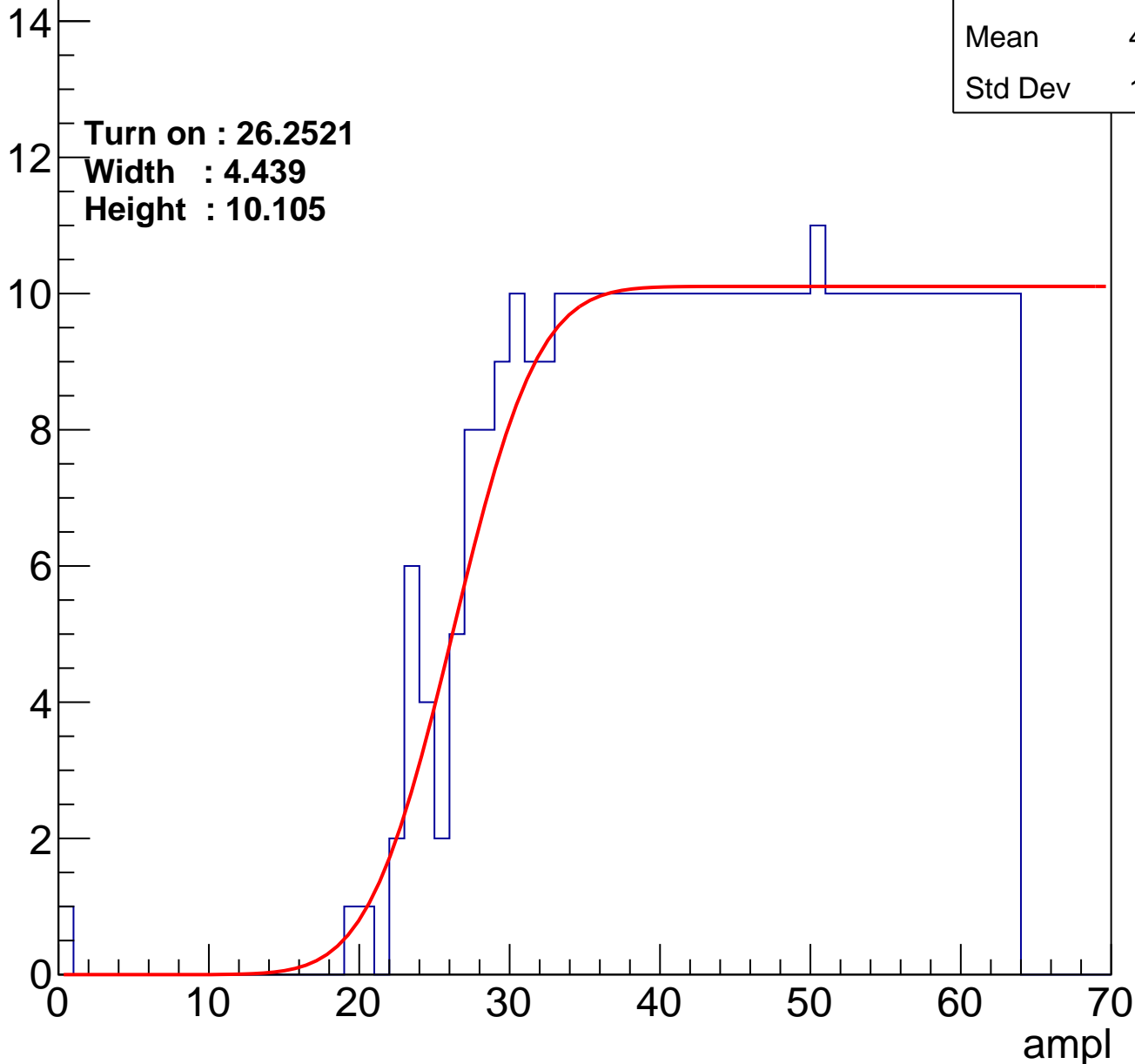
Entries	386
Mean	44.03
Std Dev	11.57

Turn on : 26.2521

Width : 4.439

Height : 10.105

Entry



B1L102S, U20-ch88

calib_packv5_042523_0143.root, FC#11, port A2

Entries	395
Mean	43.54
Std Dev	11.87

Turn on : 24.8324

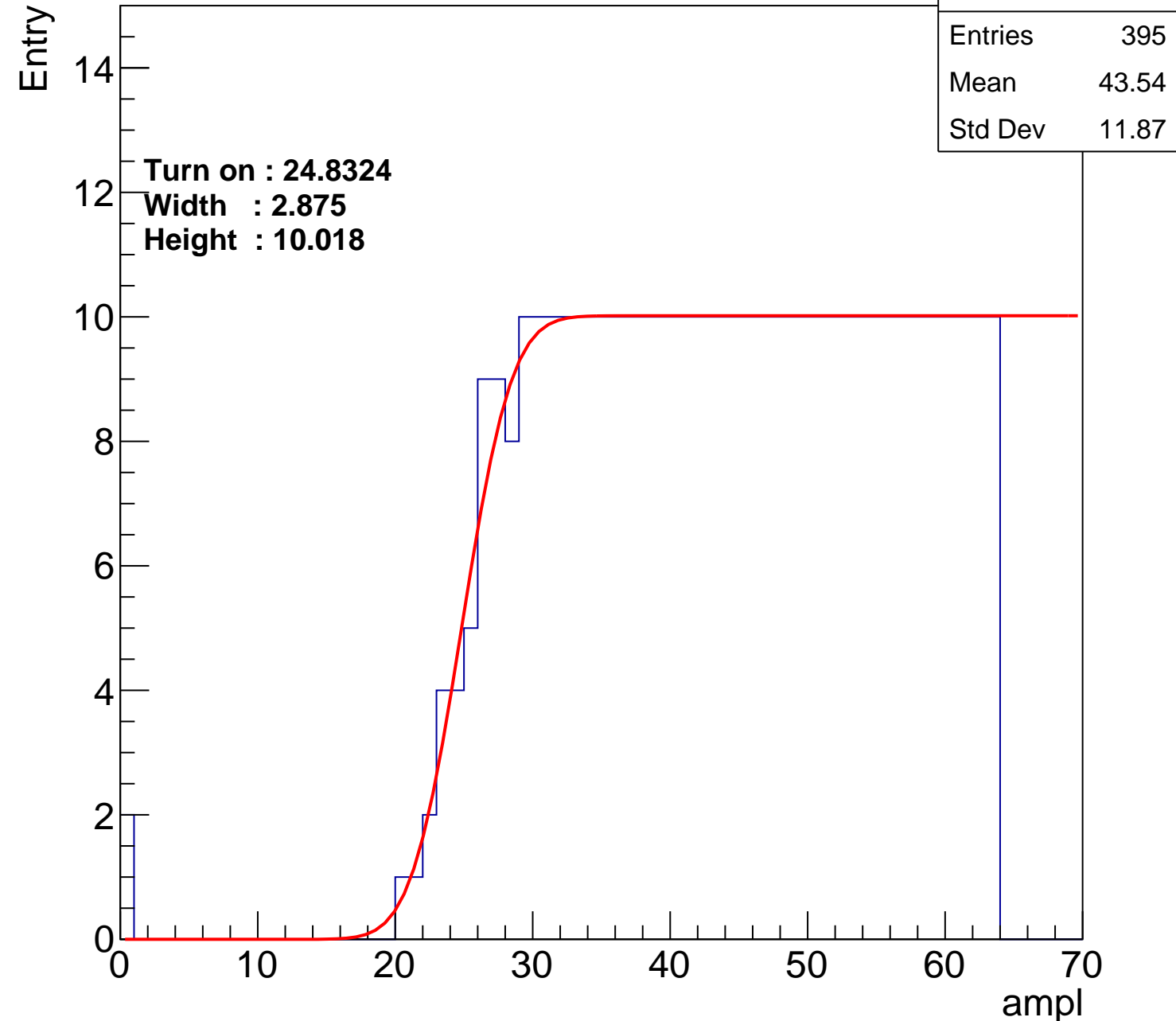
Width : 2.875

Height : 10.018

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U20-ch89

calib_packv5_042523_0143.root, FC#11, port A2

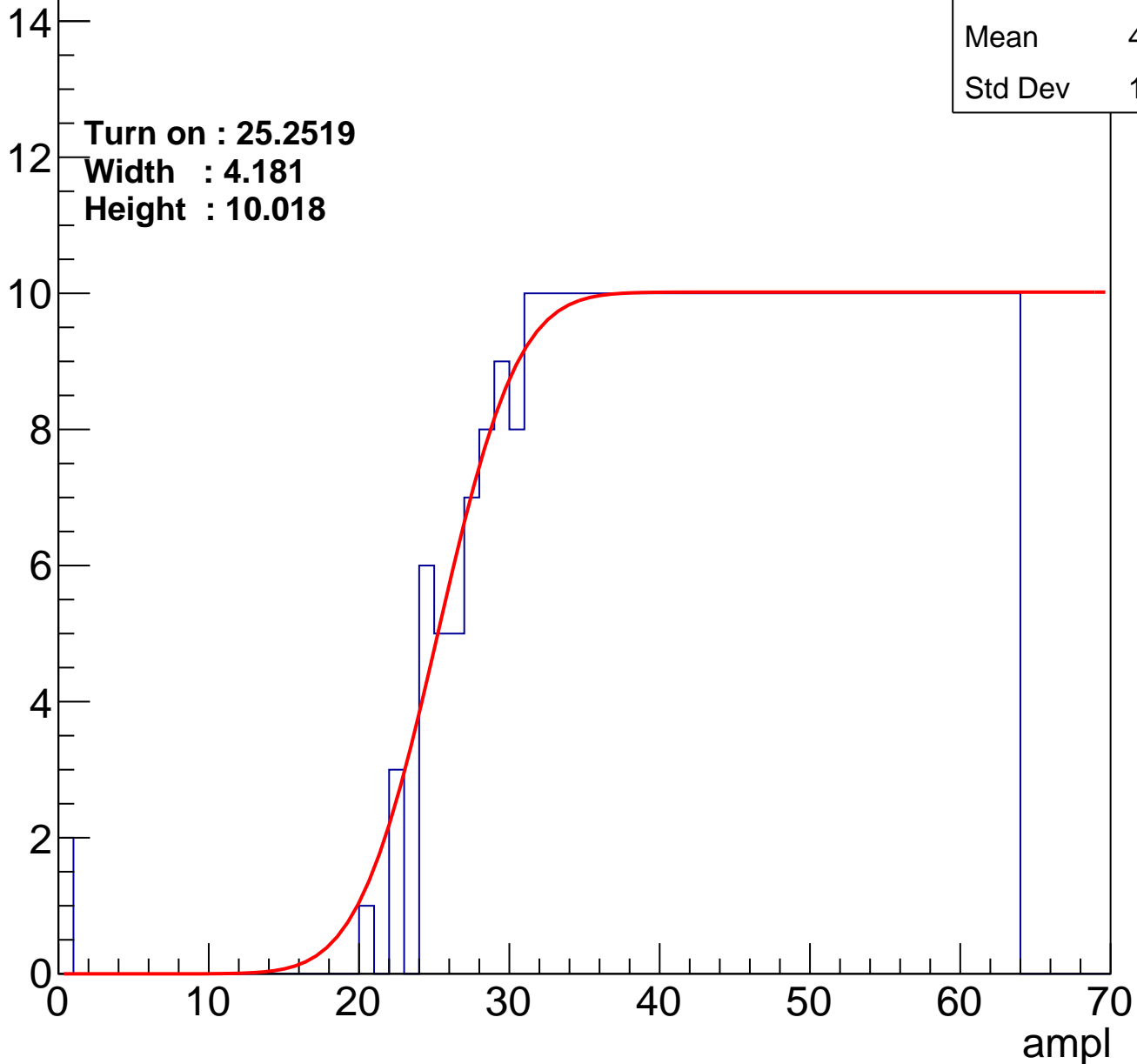
Entries	384
Mean	44.03
Std Dev	11.67

Turn on : 25.2519

Width : 4.181

Height : 10.018

Entry



B1L102S, U20-ch90

calib_packv5_042523_0143.root, FC#11, port A2

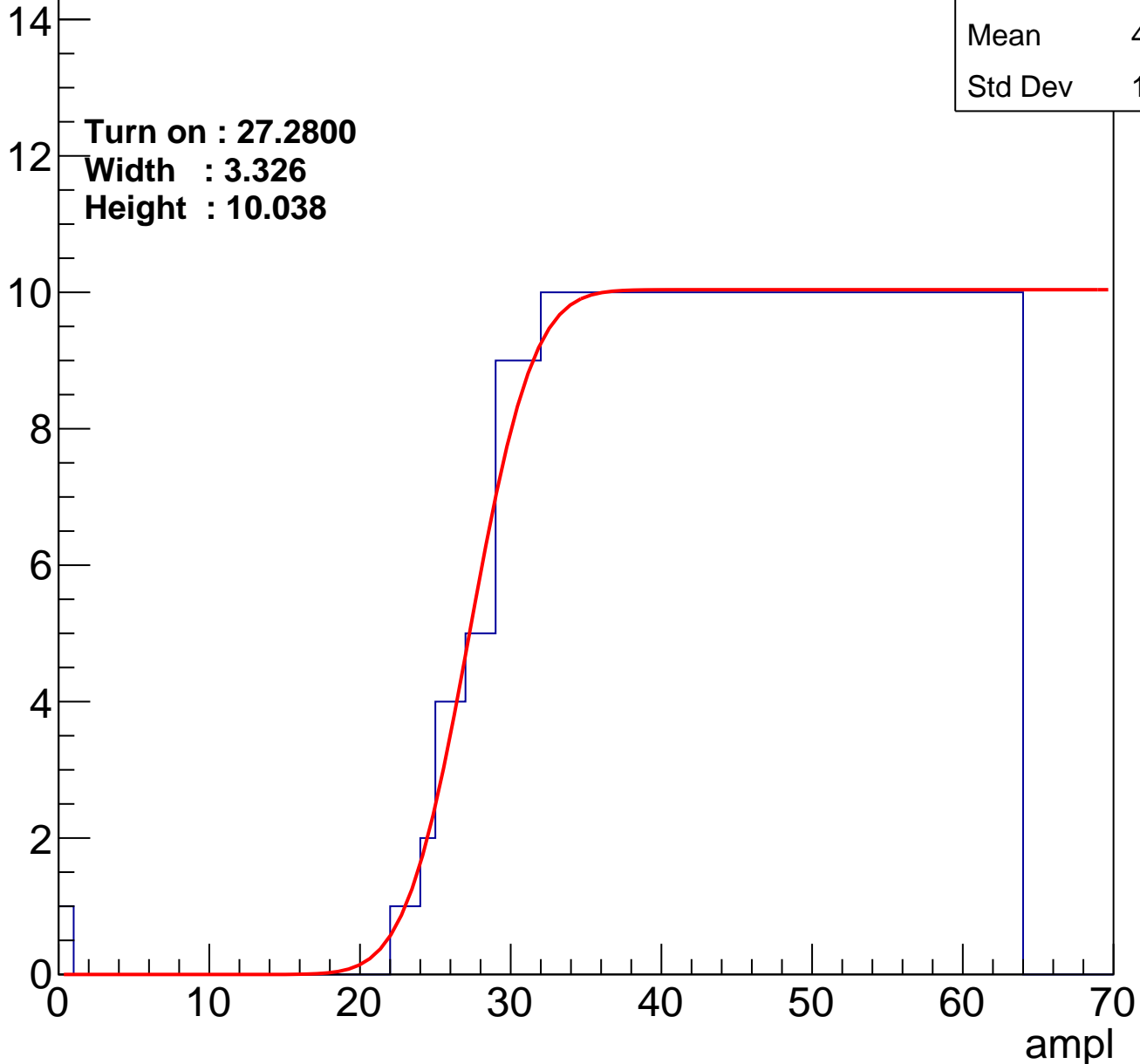
Entries	370
Mean	44.82
Std Dev	11.08

Turn on : 27.2800

Width : 3.326

Height : 10.038

Entry



B1L102S, U20-ch91

calib_packv5_042523_0143.root, FC#11, port A2

Entries	393
Mean	43.47
Std Dev	12.22

Turn on : 25.5404

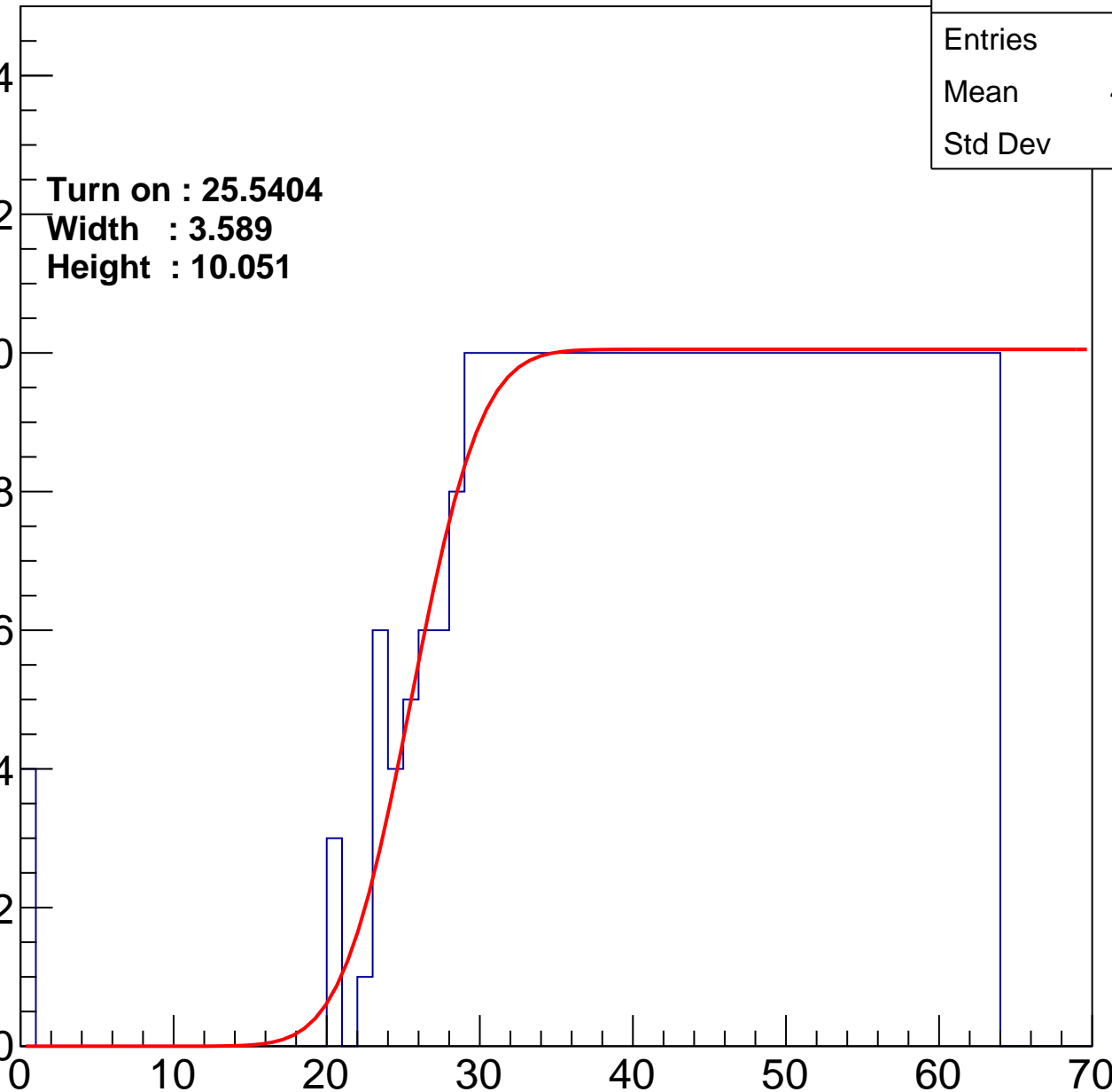
Width : 3.589

Height : 10.051

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U20-ch92

calib_packv5_042523_0143.root, FC#11, port A2

Entries	405
Mean	43.03
Std Dev	12.11

Turn on : 24.0750

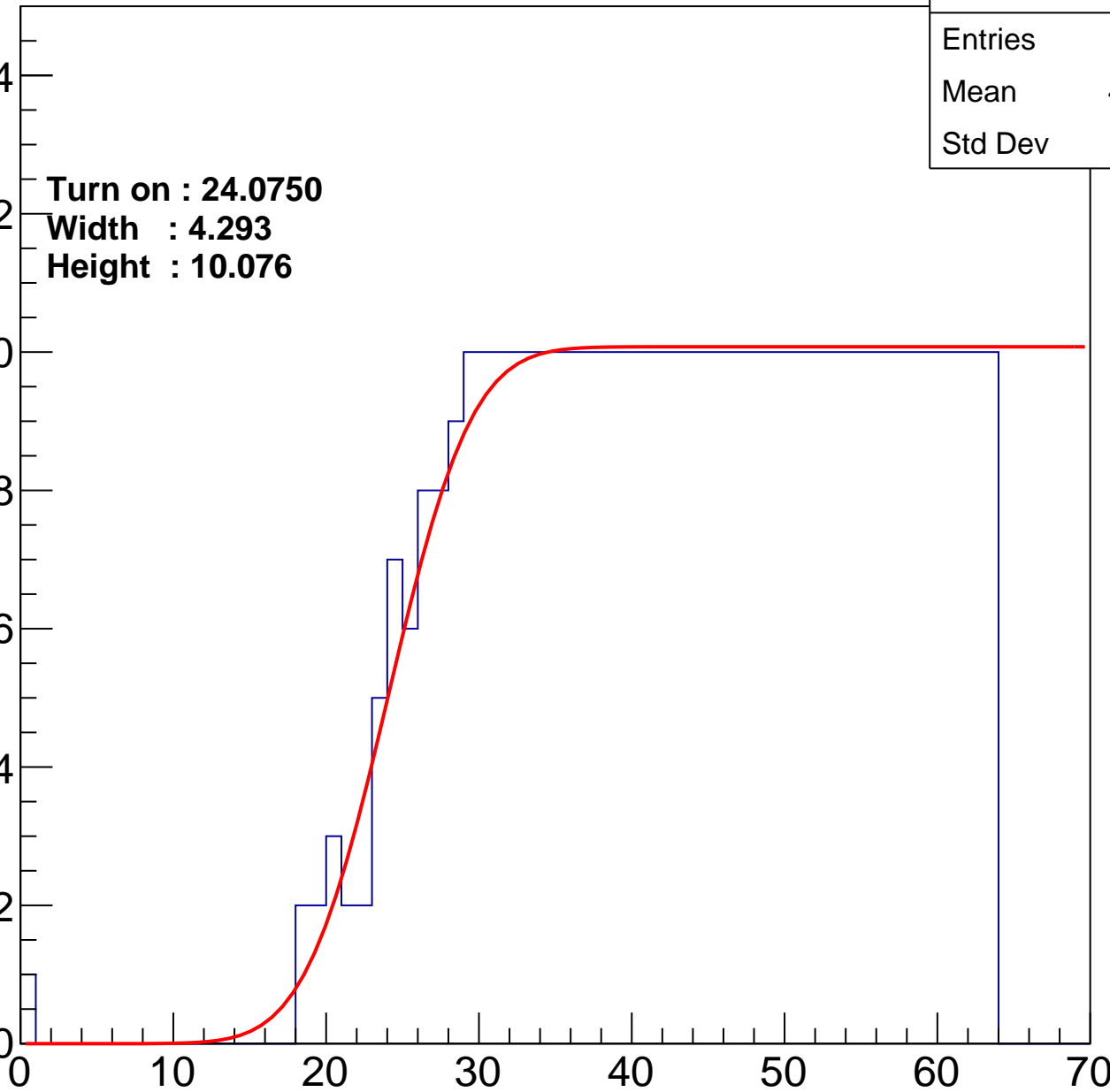
Width : 4.293

Height : 10.076

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U20-ch93

calib_packv5_042523_0143.root, FC#11, port A2

Entries	394
Mean	43.54
Std Dev	11.94

Turn on : 26.1820

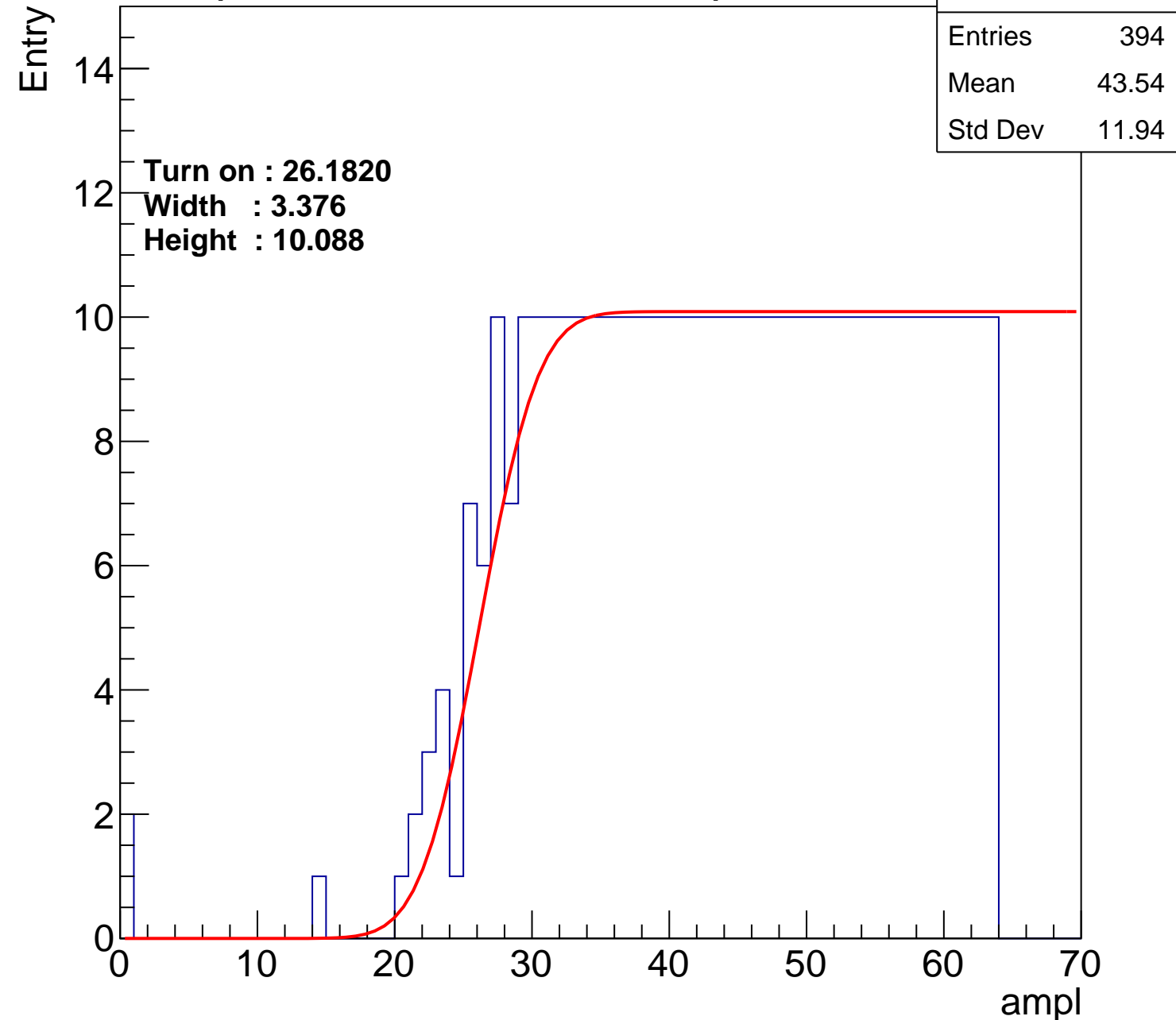
Width : 3.376

Height : 10.088

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U20-ch94

calib_packv5_042523_0143.root, FC#11, port A2

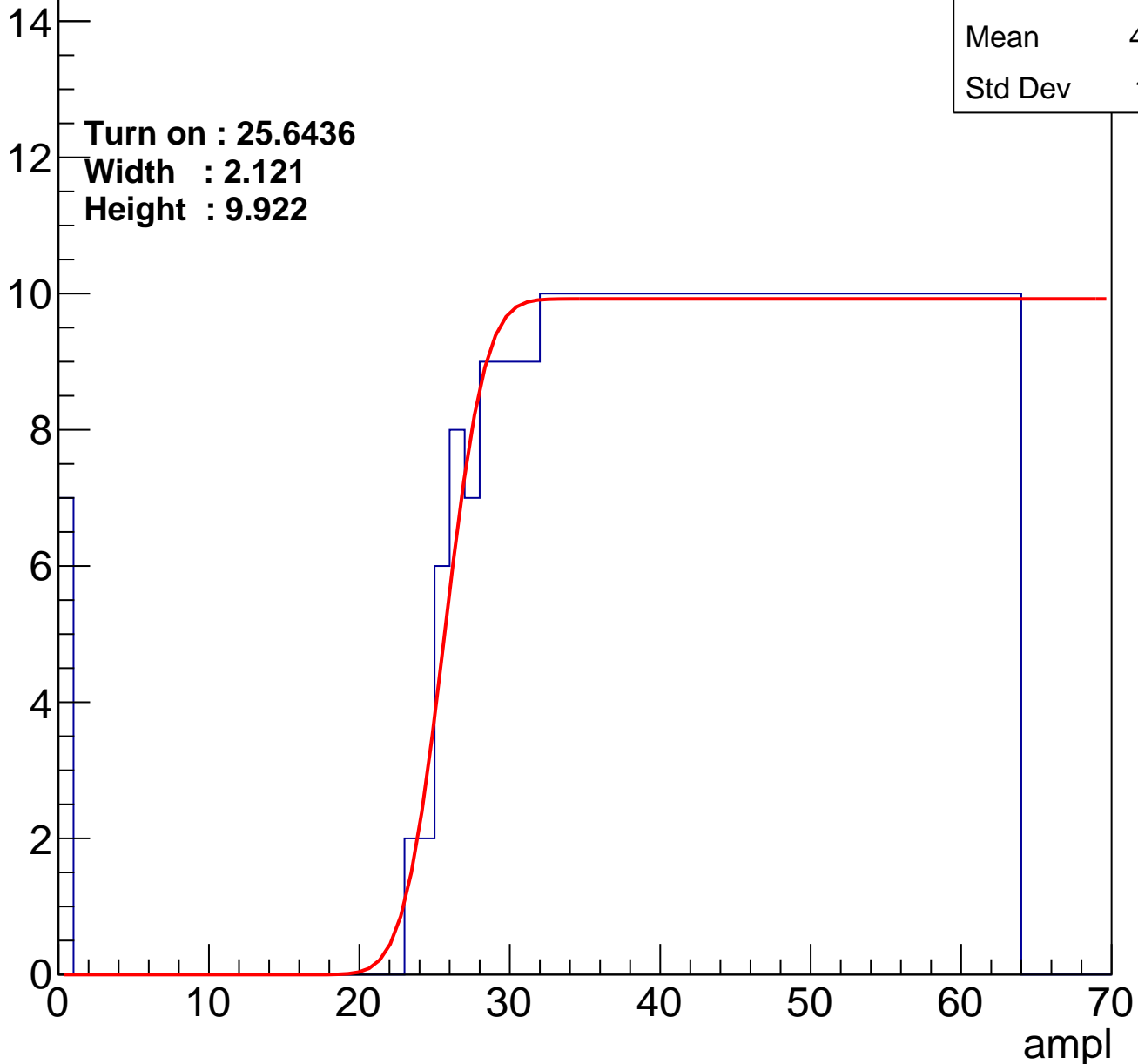
Entries	388
Mean	43.56
Std Dev	12.51

Turn on : 25.6436

Width : 2.121

Height : 9.922

Entry



B1L102S, U20-ch95

calib_packv5_042523_0143.root, FC#11, port A2

Entries	396
Mean	43.44
Std Dev	11.98

Turn on : 24.6477

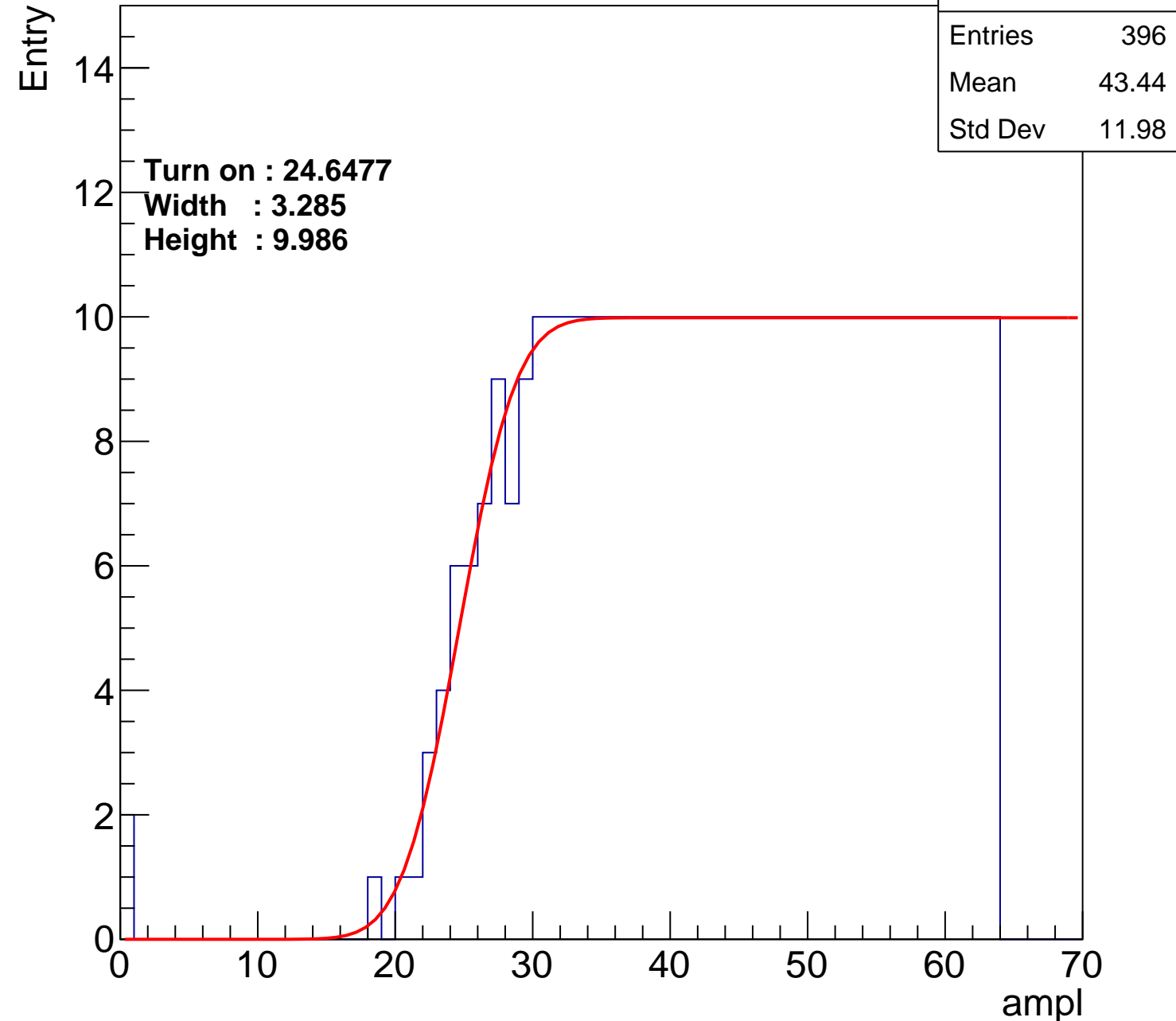
Width : 3.285

Height : 9.986

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U20-ch96

calib_packv5_042523_0143.root, FC#11, port A2

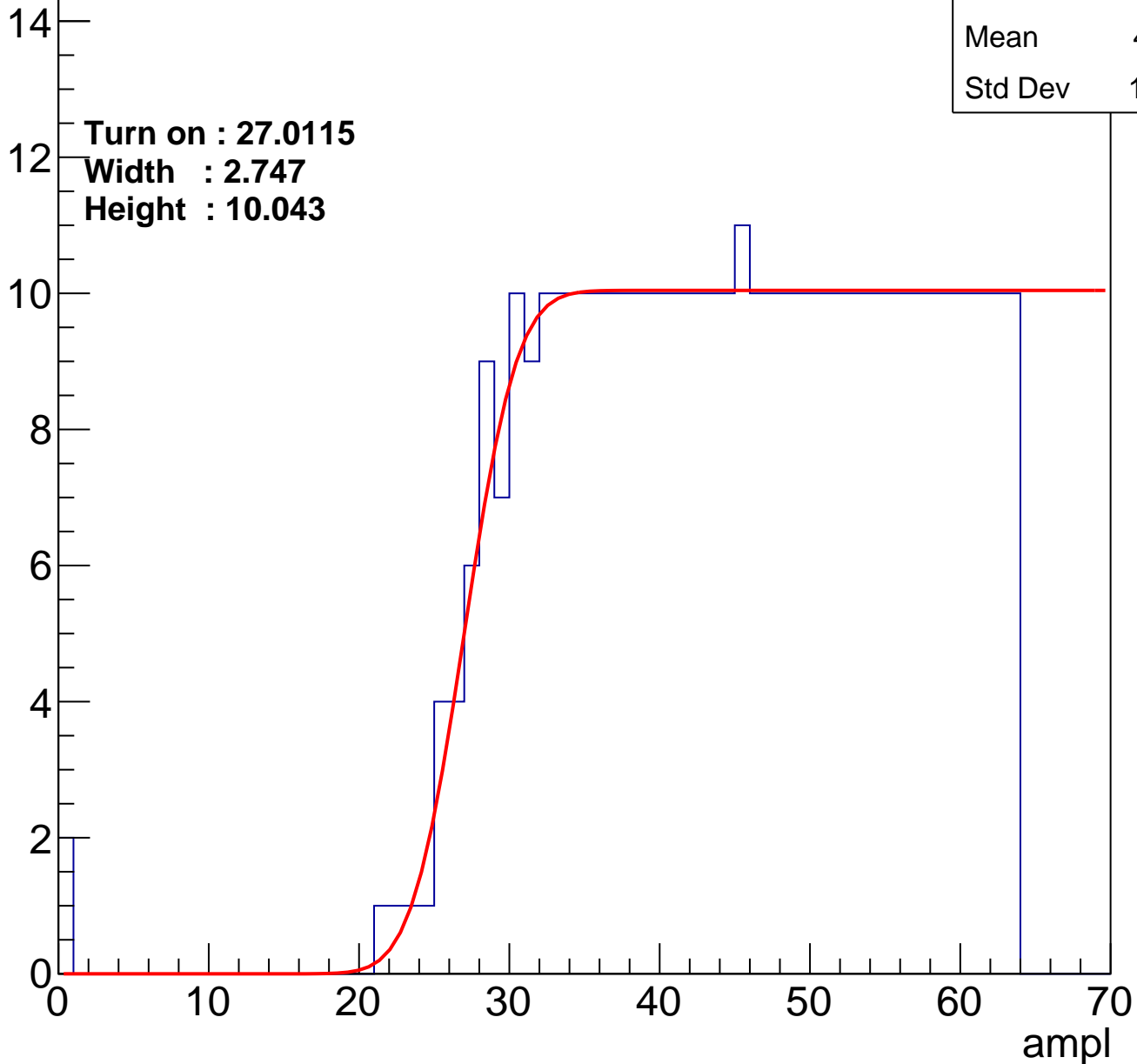
Entries	376
Mean	44.51
Std Dev	11.38

Turn on : 27.0115

Width : 2.747

Height : 10.043

Entry



B1L102S, U20-ch97

calib_packv5_042523_0143.root, FC#11, port A2

Entries	392
Mean	43.77
Std Dev	11.6

Turn on : 24.8527

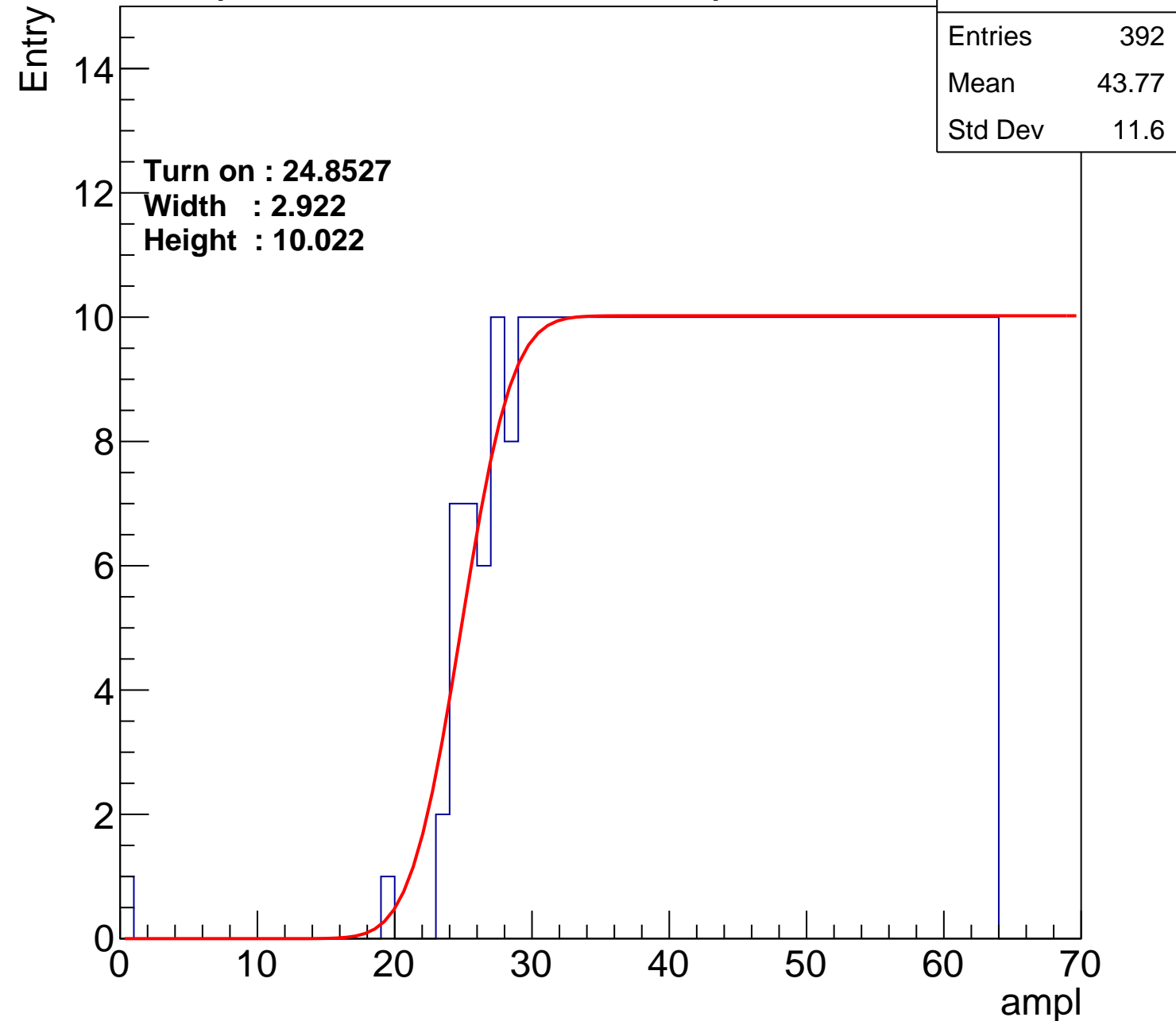
Width : 2.922

Height : 10.022

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U20-ch98

calib_packv5_042523_0143.root, FC#11, port A2

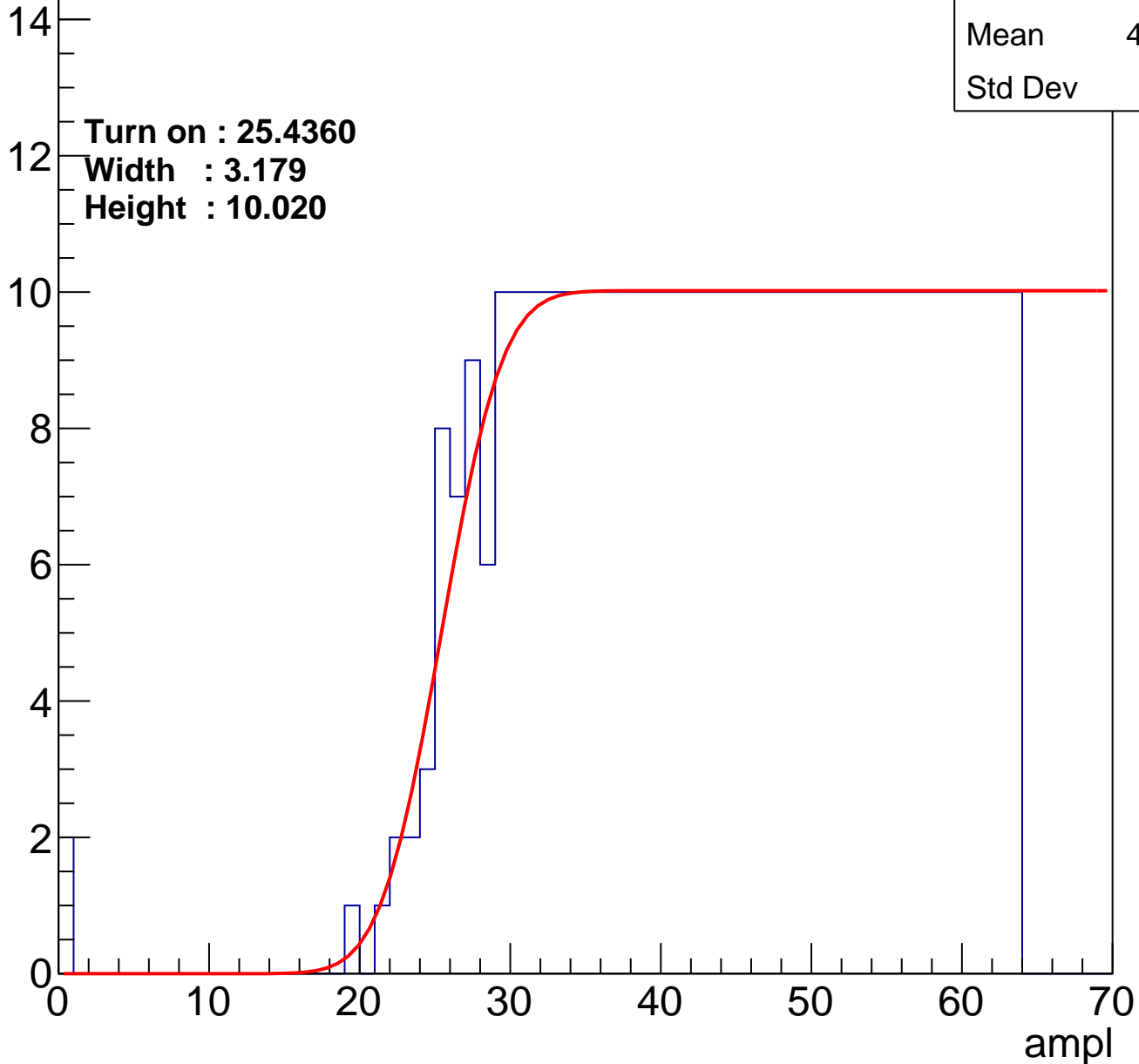
Entries	391
Mean	43.72
Std Dev	11.8

Turn on : 25.4360

Width : 3.179

Height : 10.020

Entry



B1L102S, U20-ch99

calib_packv5_042523_0143.root, FC#11, port A2

Entries	369
Mean	44.79
Std Dev	11.27

Turn on : 27.8899

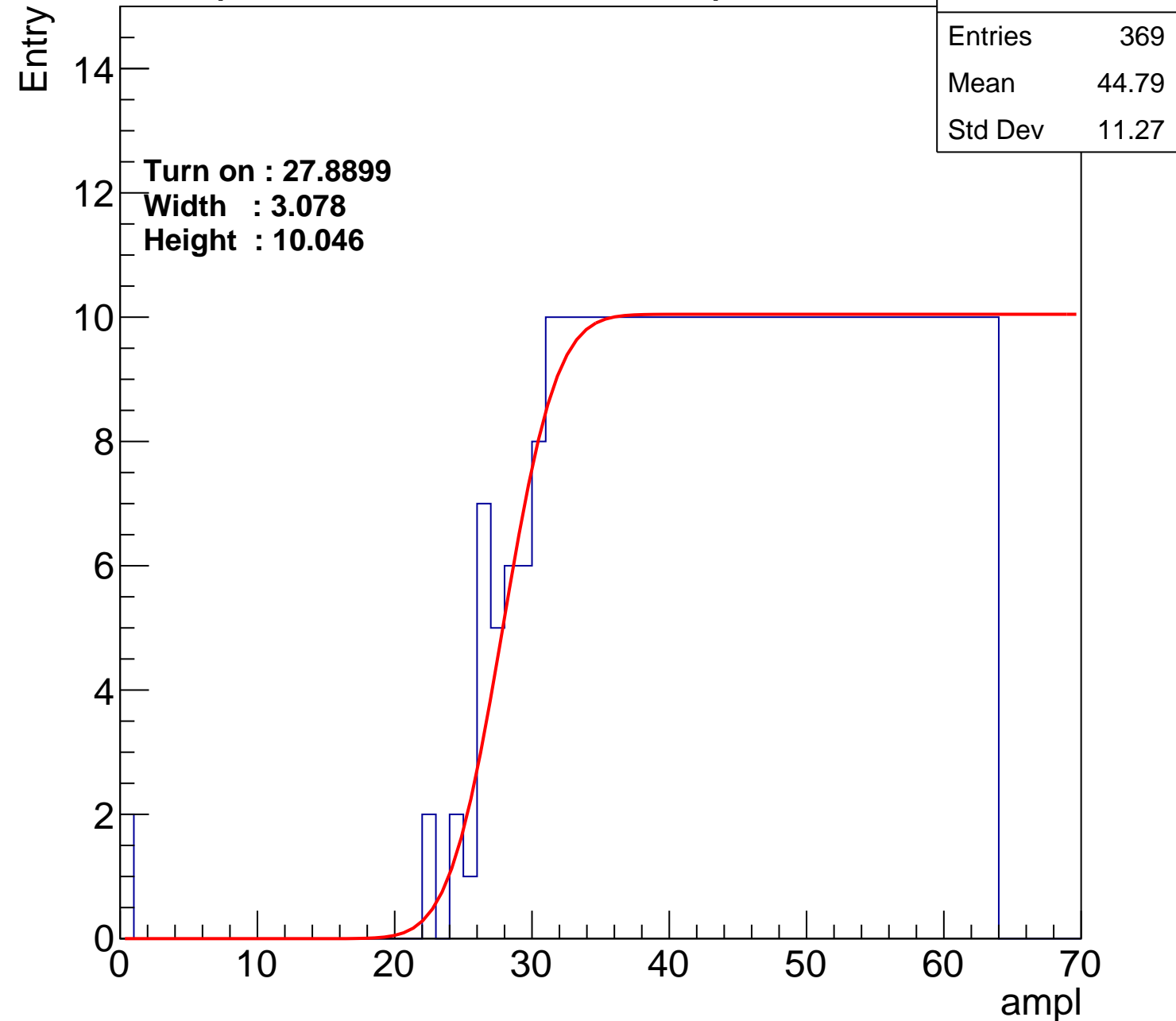
Width : 3.078

Height : 10.046

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U20-ch100

calib_packv5_042523_0143.root, FC#11, port A2

Entries	415
Mean	42.42
Std Dev	12.76

Turn on : 23.1576

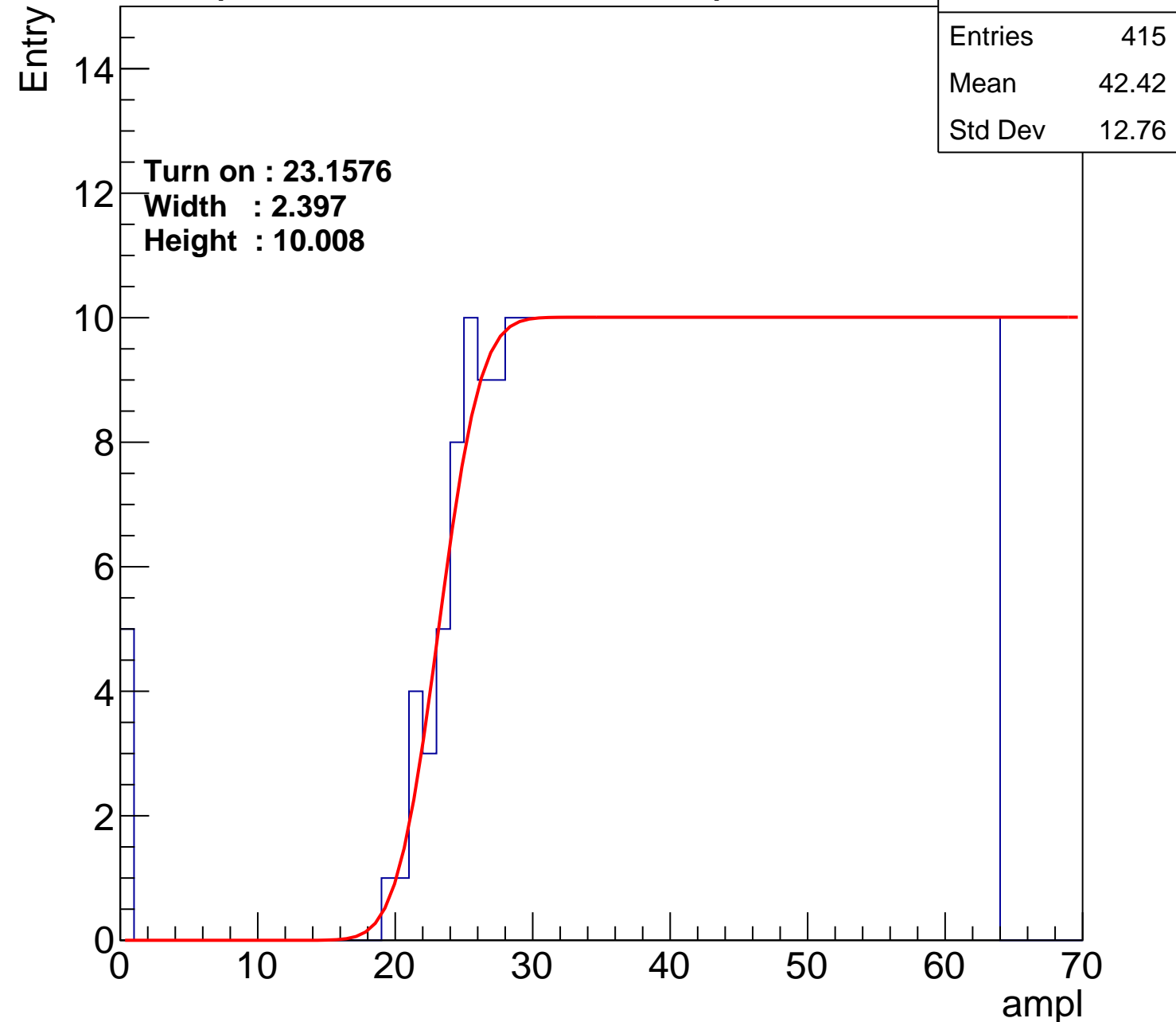
Width : 2.397

Height : 10.008

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U20-ch101

calib_packv5_042523_0143.root, FC#11, port A2

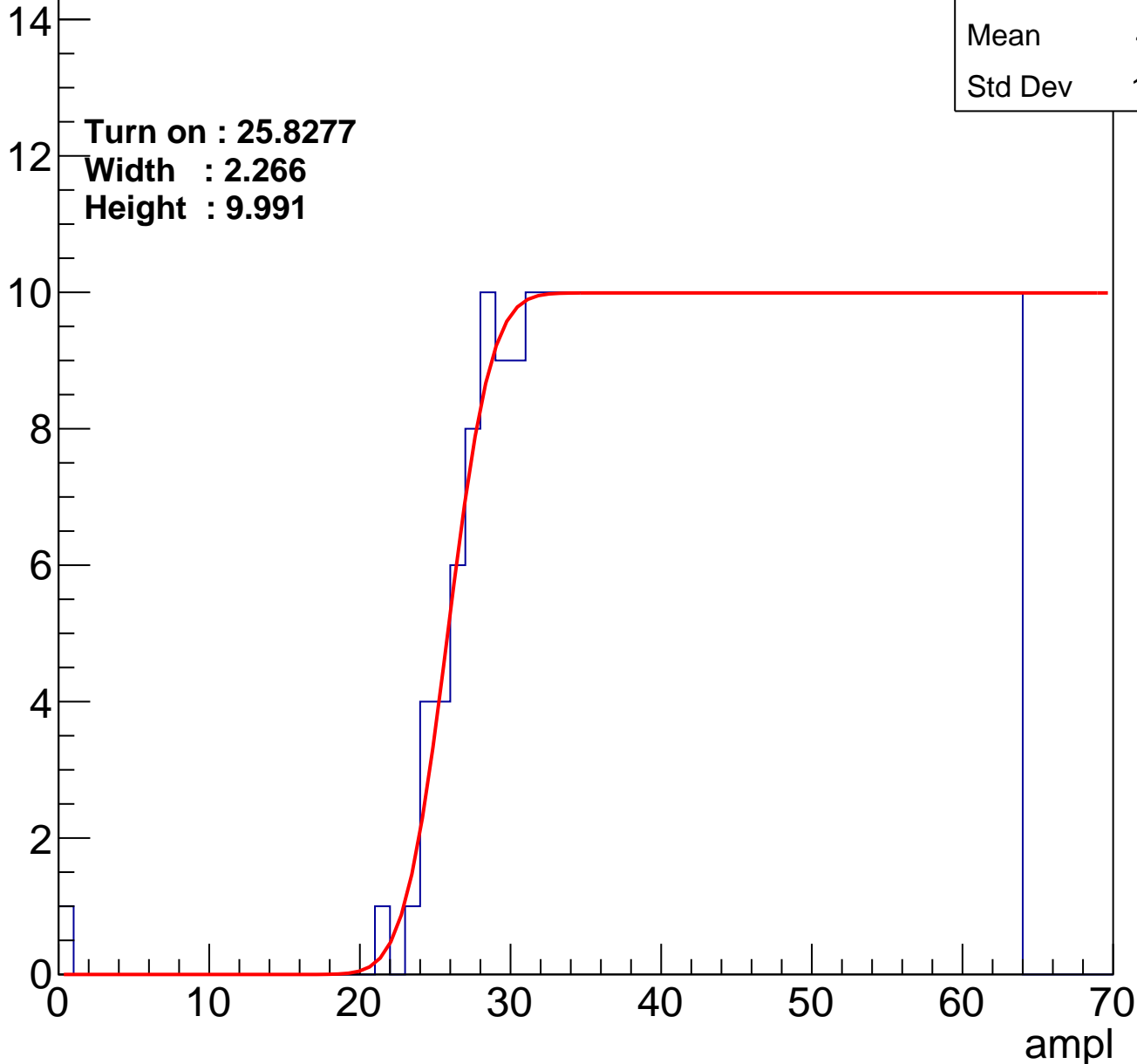
Entries	383
Mean	44.21
Std Dev	11.36

Turn on : 25.8277

Width : 2.266

Height : 9.991

Entry



B1L102S, U20-ch102

calib_packv5_042523_0143.root, FC#11, port A2

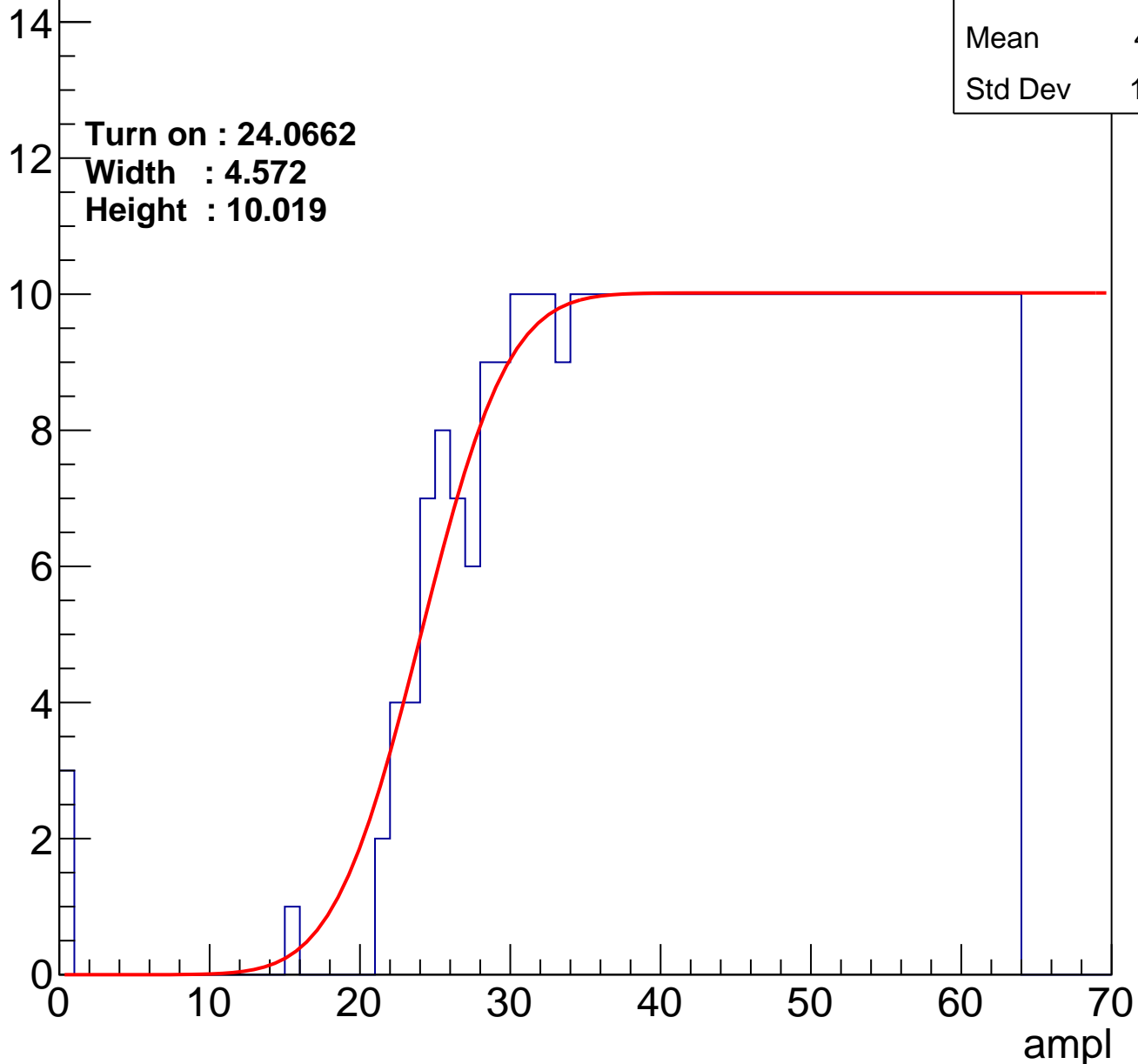
Entries	399
Mean	43.21
Std Dev	12.25

Turn on : 24.0662

Width : 4.572

Height : 10.019

Entry



B1L102S, U20-ch103

calib_packv5_042523_0143.root, FC#11, port A2

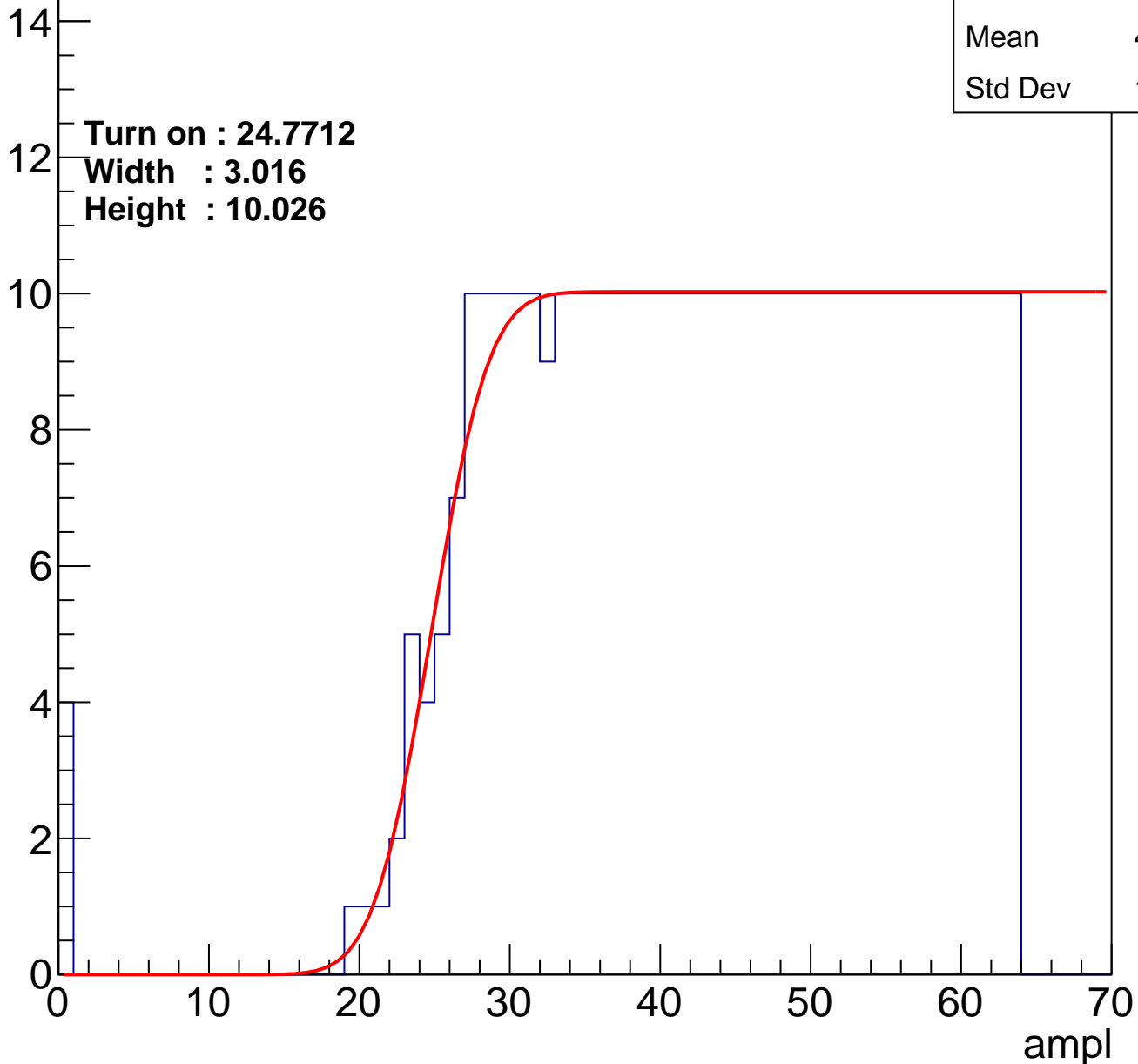
Entries	399
Mean	43.21
Std Dev	12.31

Turn on : 24.7712

Width : 3.016

Height : 10.026

Entry



B1L102S, U20-ch104

calib_packv5_042523_0143.root, FC#11, port A2

Entries	375
Mean	44.47
Std Dev	11.45

Turn on : 26.6578

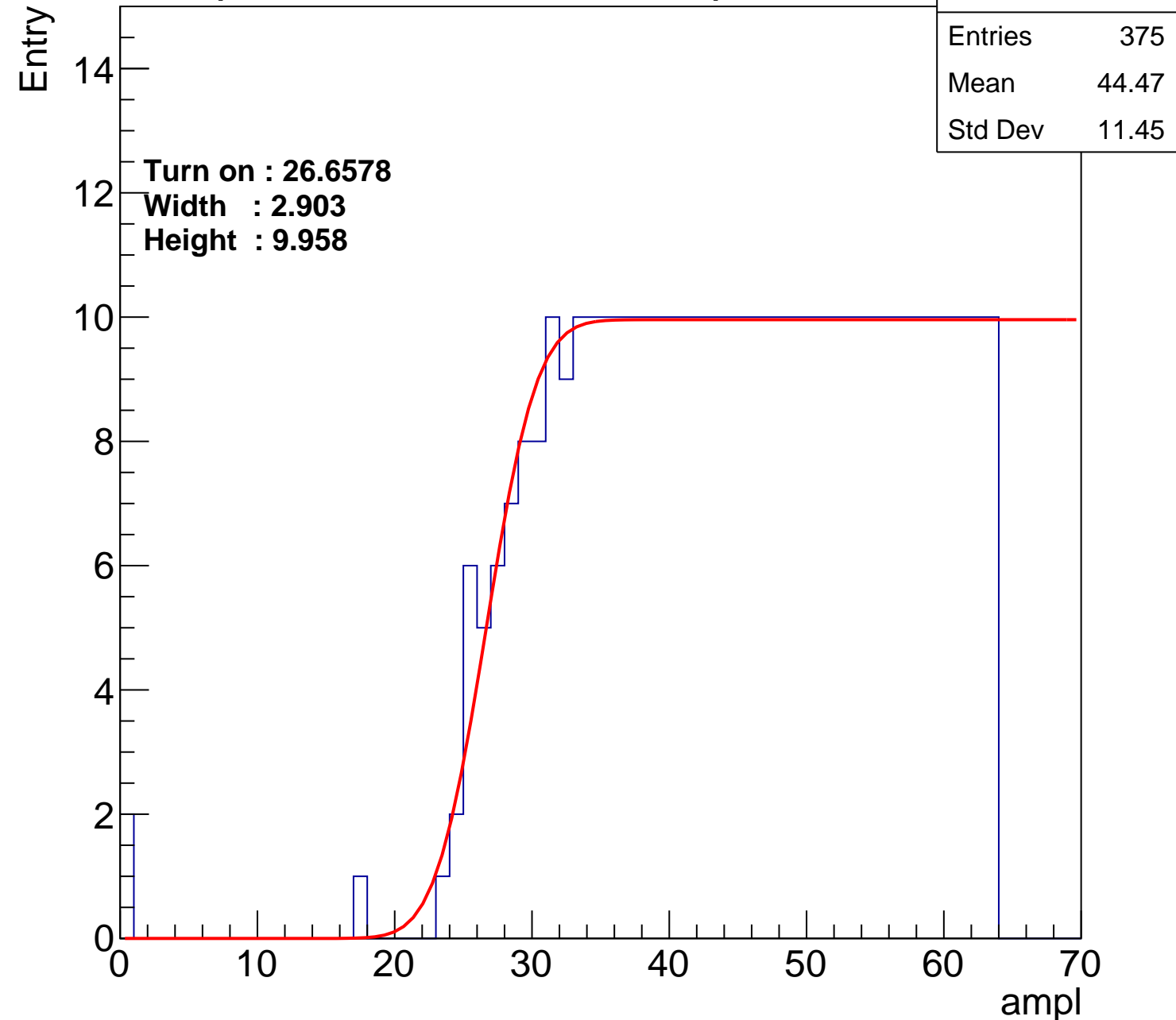
Width : 2.903

Height : 9.958

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U20-ch105

calib_packv5_042523_0143.root, FC#11, port A2

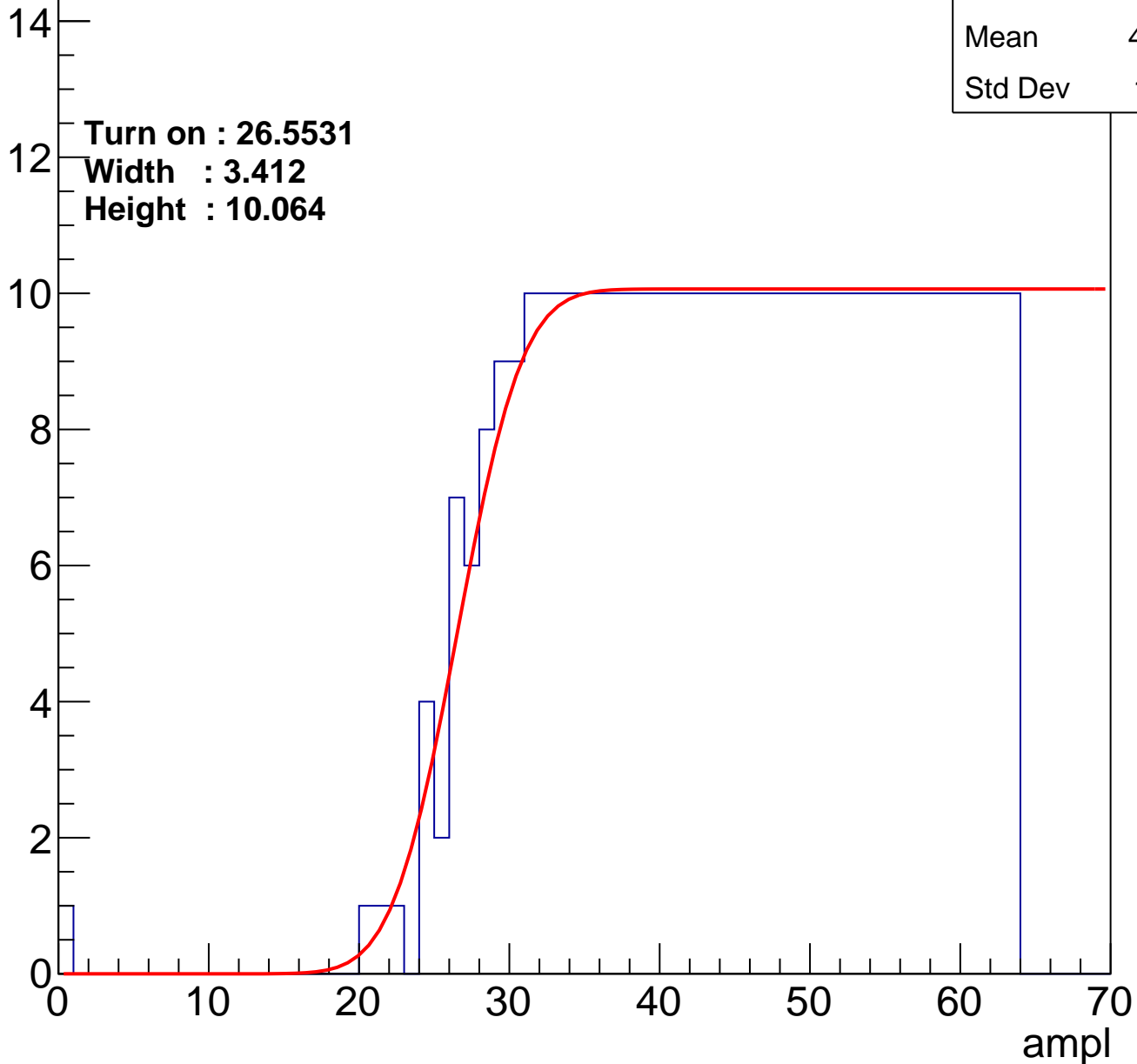
Entries	379
Mean	44.37
Std Dev	11.31

Turn on : 26.5531

Width : 3.412

Height : 10.064

Entry



B1L102S, U20-ch106

calib_packv5_042523_0143.root, FC#11, port A2

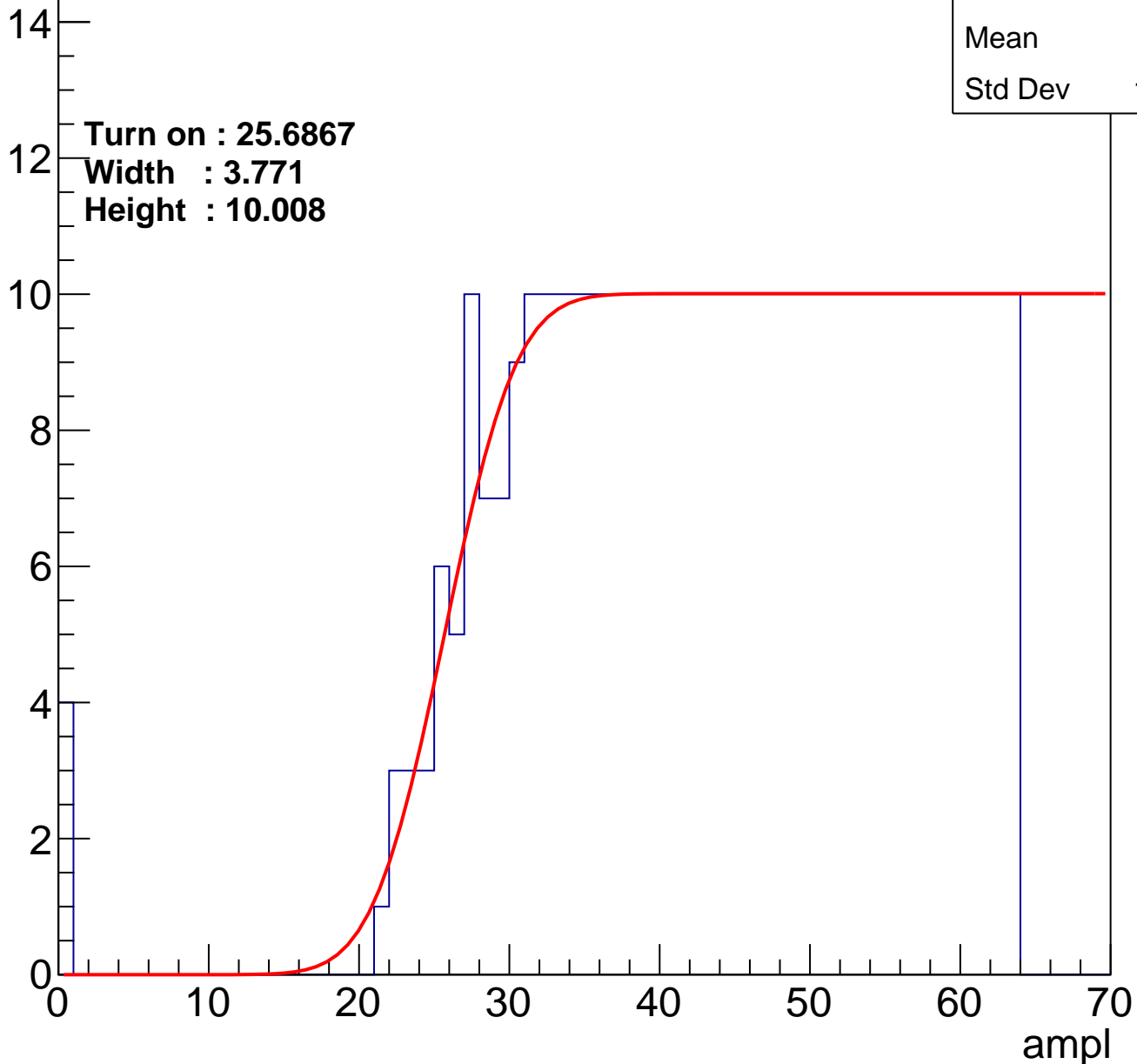
Entries	388
Mean	43.7
Std Dev	12.11

Turn on : 25.6867

Width : 3.771

Height : 10.008

Entry



B1L102S, U20-ch107

calib_packv5_042523_0143.root, FC#11, port A2

Entries	364
Mean	45.07
Std Dev	11.07

Turn on : 28.1800

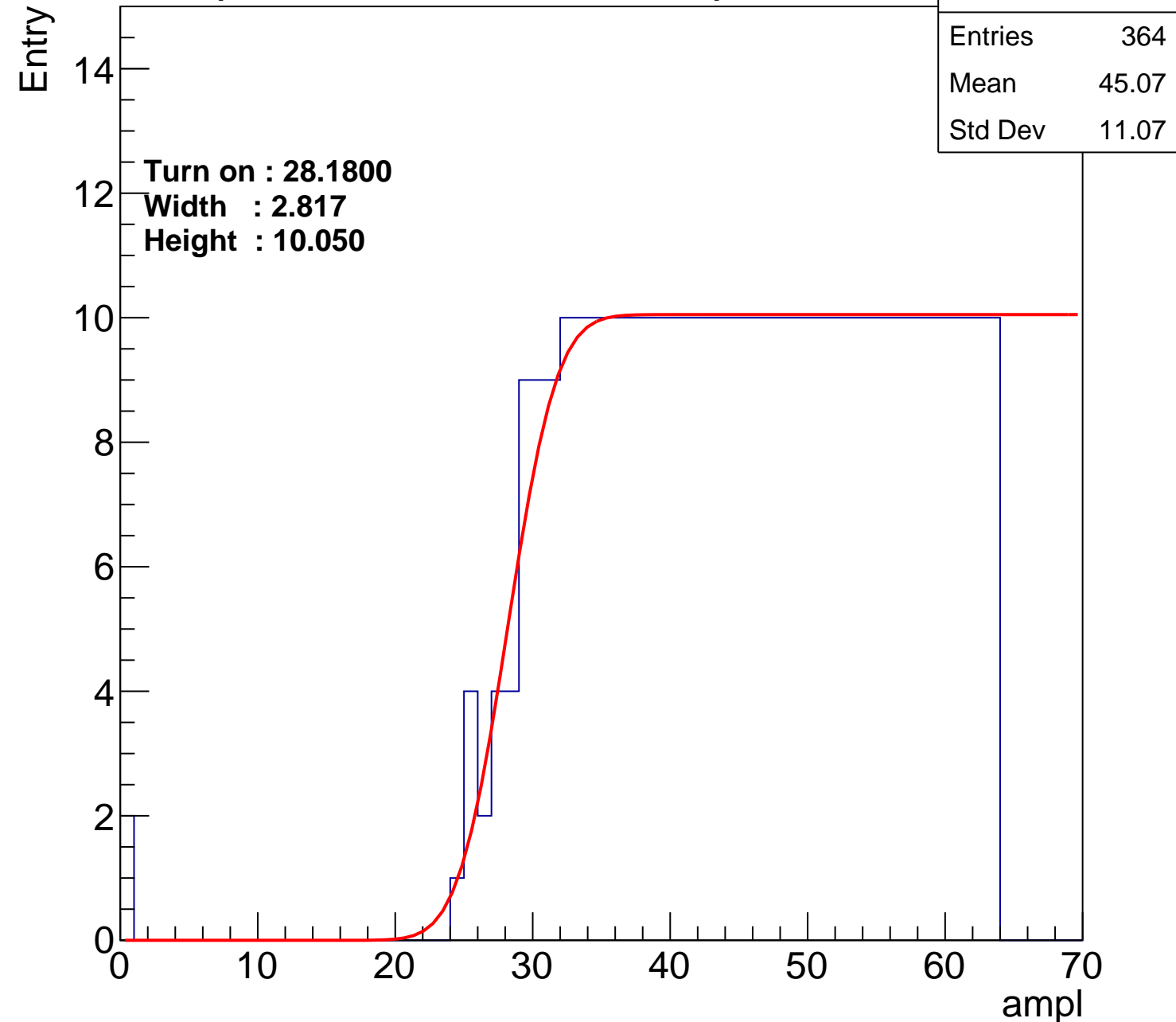
Width : 2.817

Height : 10.050

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U20-ch108

calib_packv5_042523_0143.root, FC#11, port A2

Entries	386
Mean	43.92
Std Dev	11.84

Turn on : 26.5883

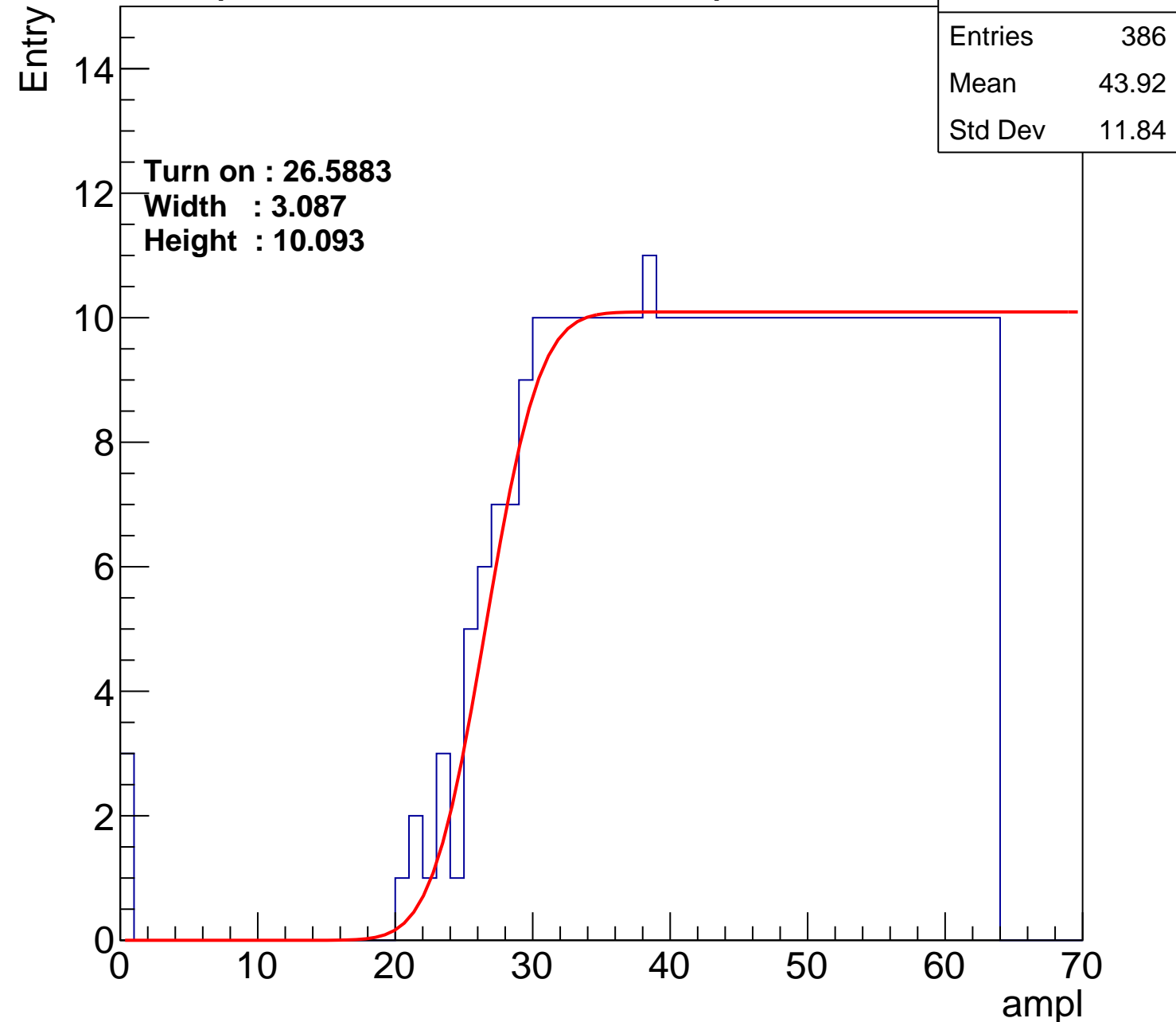
Width : 3.087

Height : 10.093

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U20-ch109

calib_packv5_042523_0143.root, FC#11, port A2

Entries	384
Mean	43.92
Std Dev	11.99

Turn on : 25.9927

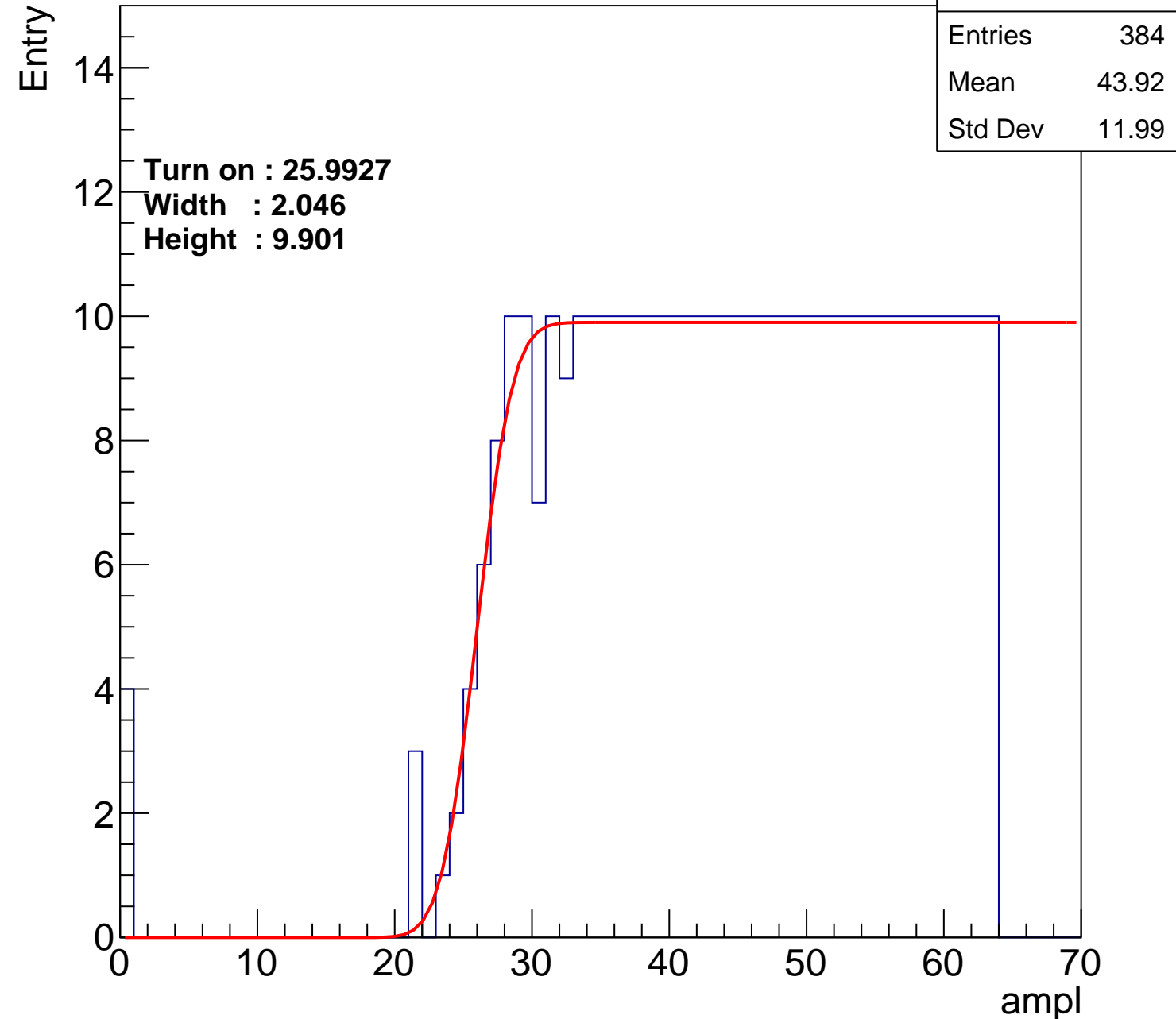
Width : 2.046

Height : 9.901

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U20-ch110

calib_packv5_042523_0143.root, FC#11, port A2

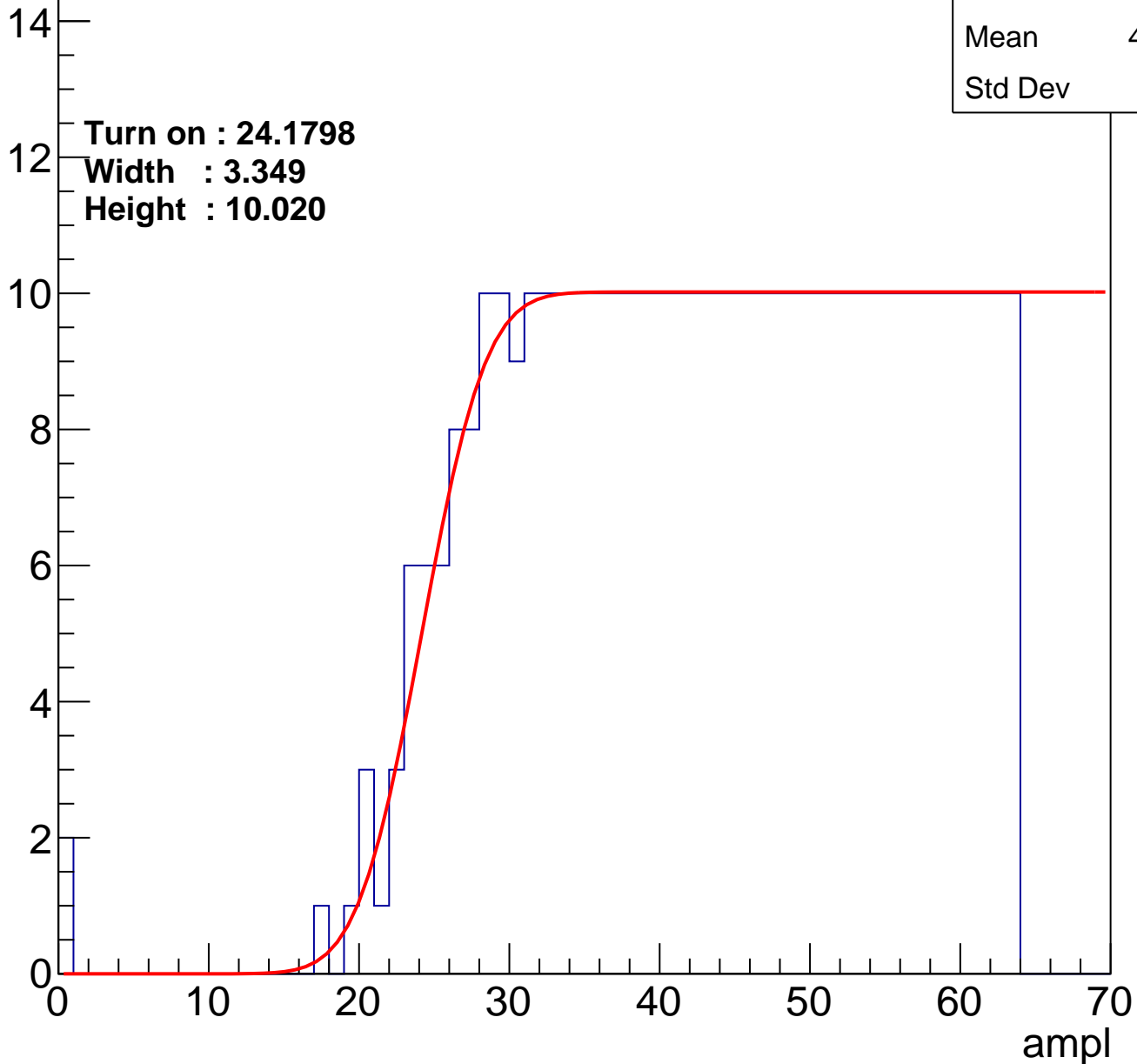
Entries	404
Mean	43.04
Std Dev	12.2

Turn on : 24.1798

Width : 3.349

Height : 10.020

Entry



B1L102S, U20-ch111

calib_packv5_042523_0143.root, FC#11, port A2

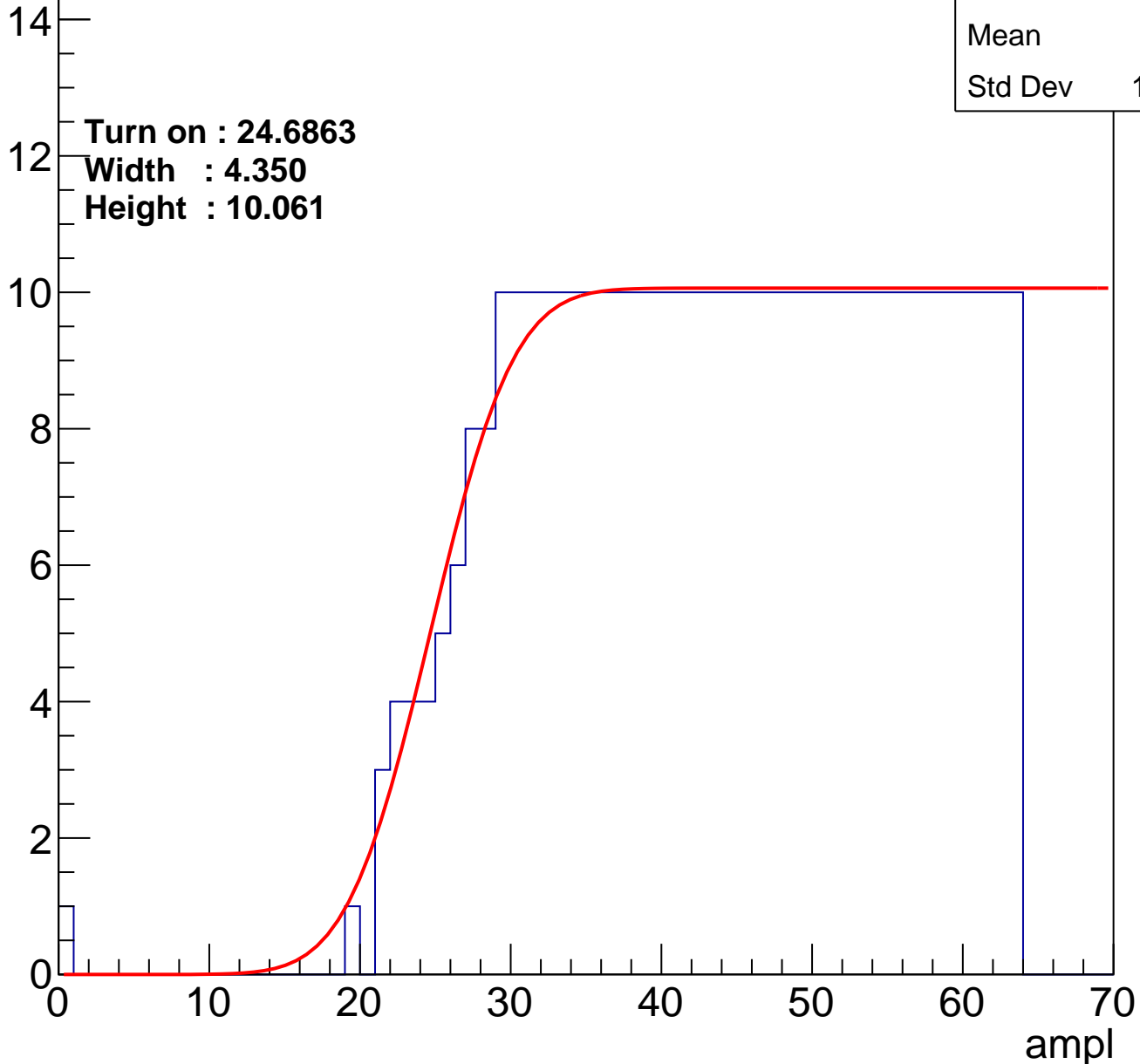
Entries	394
Mean	43.6
Std Dev	11.77

Turn on : 24.6863

Width : 4.350

Height : 10.061

Entry



B1L102S, U20-ch112

calib_packv5_042523_0143.root, FC#11, port A2

Entries	377
Mean	44.45
Std Dev	11.46

Turn on : 27.1369

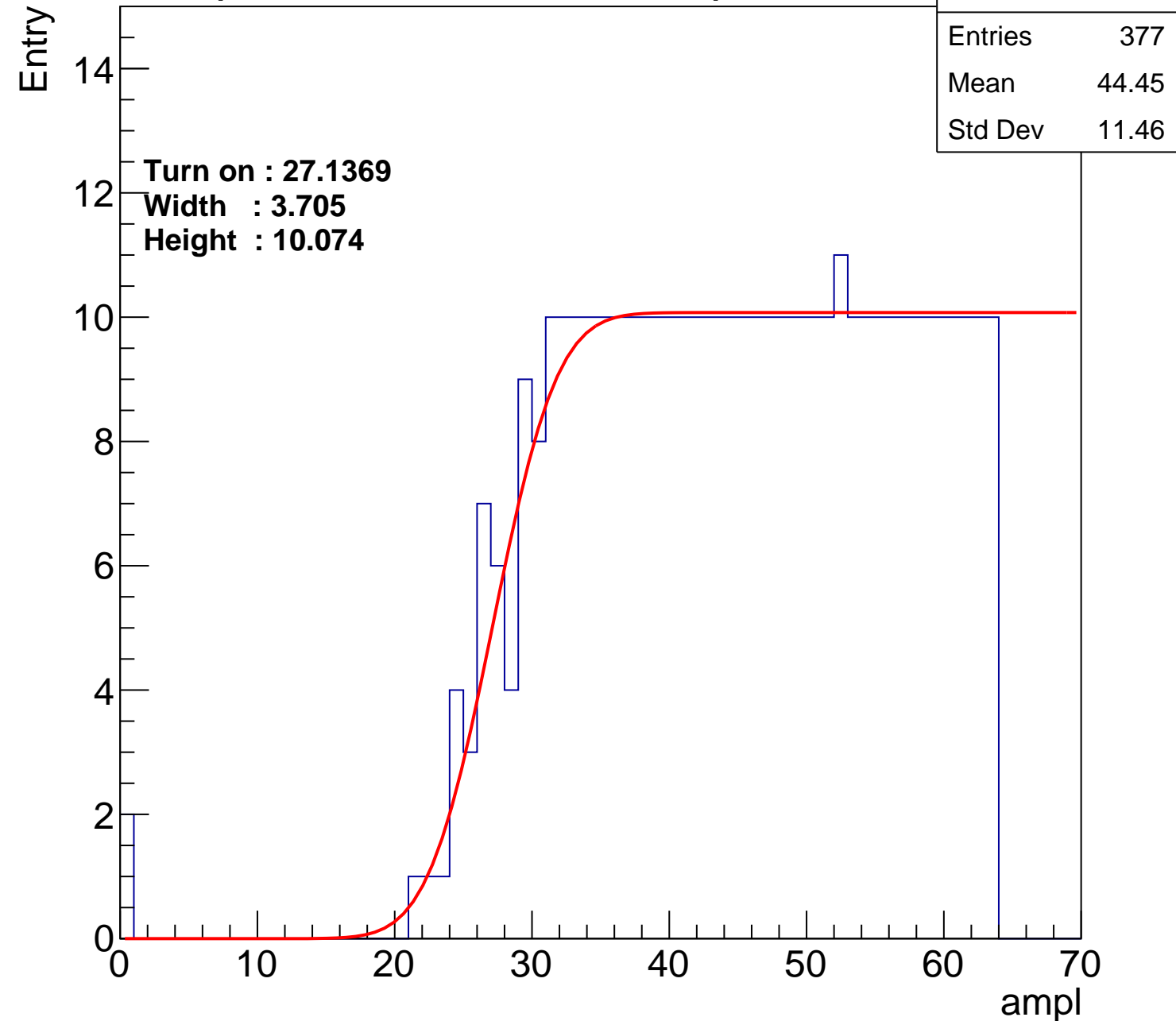
Width : 3.705

Height : 10.074

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U20-ch113

calib_packv5_042523_0143.root, FC#11, port A2

Entries	380
Mean	44.25
Std Dev	11.53

Turn on : 26.3260

Width : 2.701

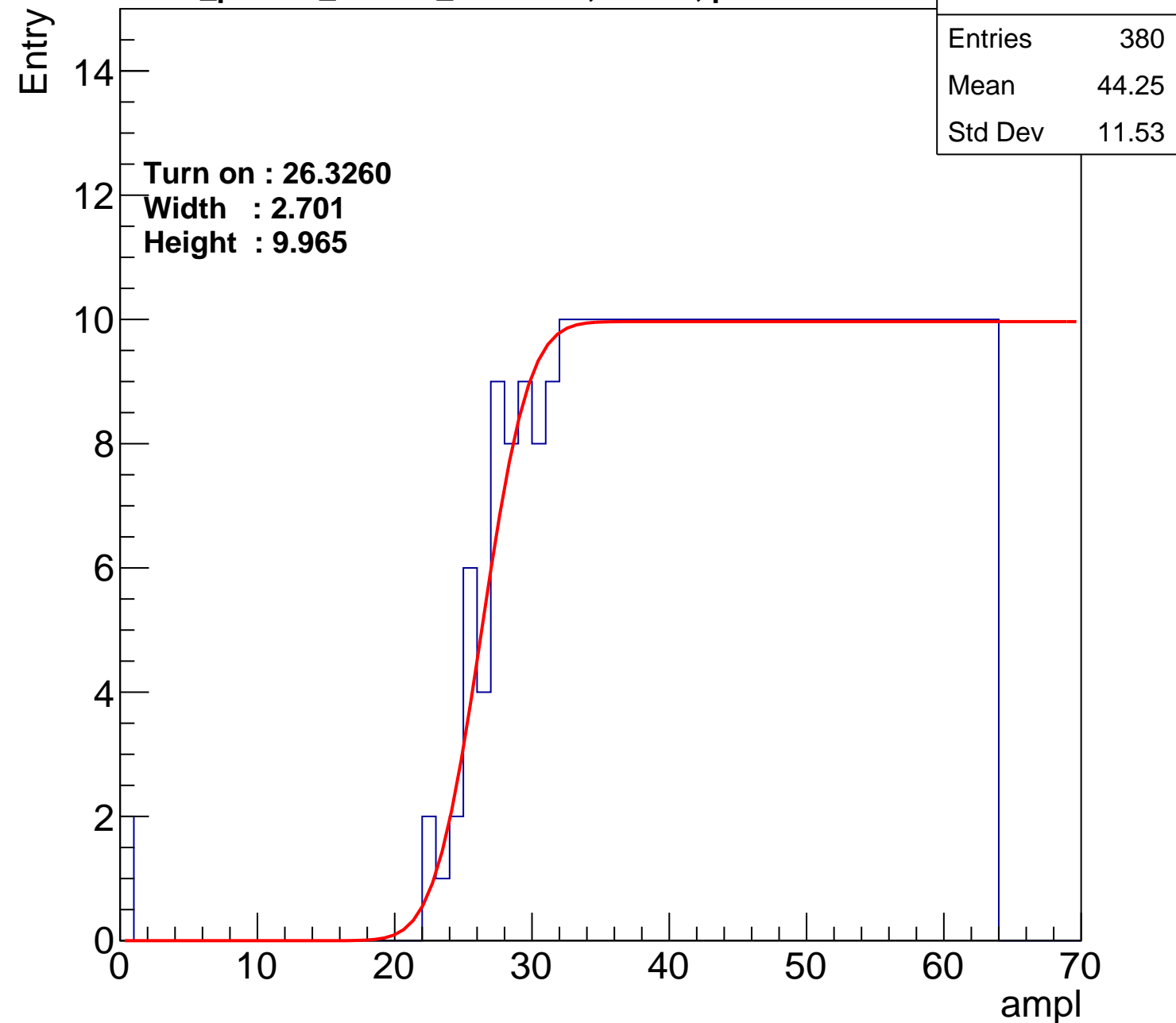
Height : 9.965

Entry

14
12
10
8
6
4
2
0

ampl

0 10 20 30 40 50 60 70



B1L102S, U20-ch114

calib_packv5_042523_0143.root, FC#11, port A2

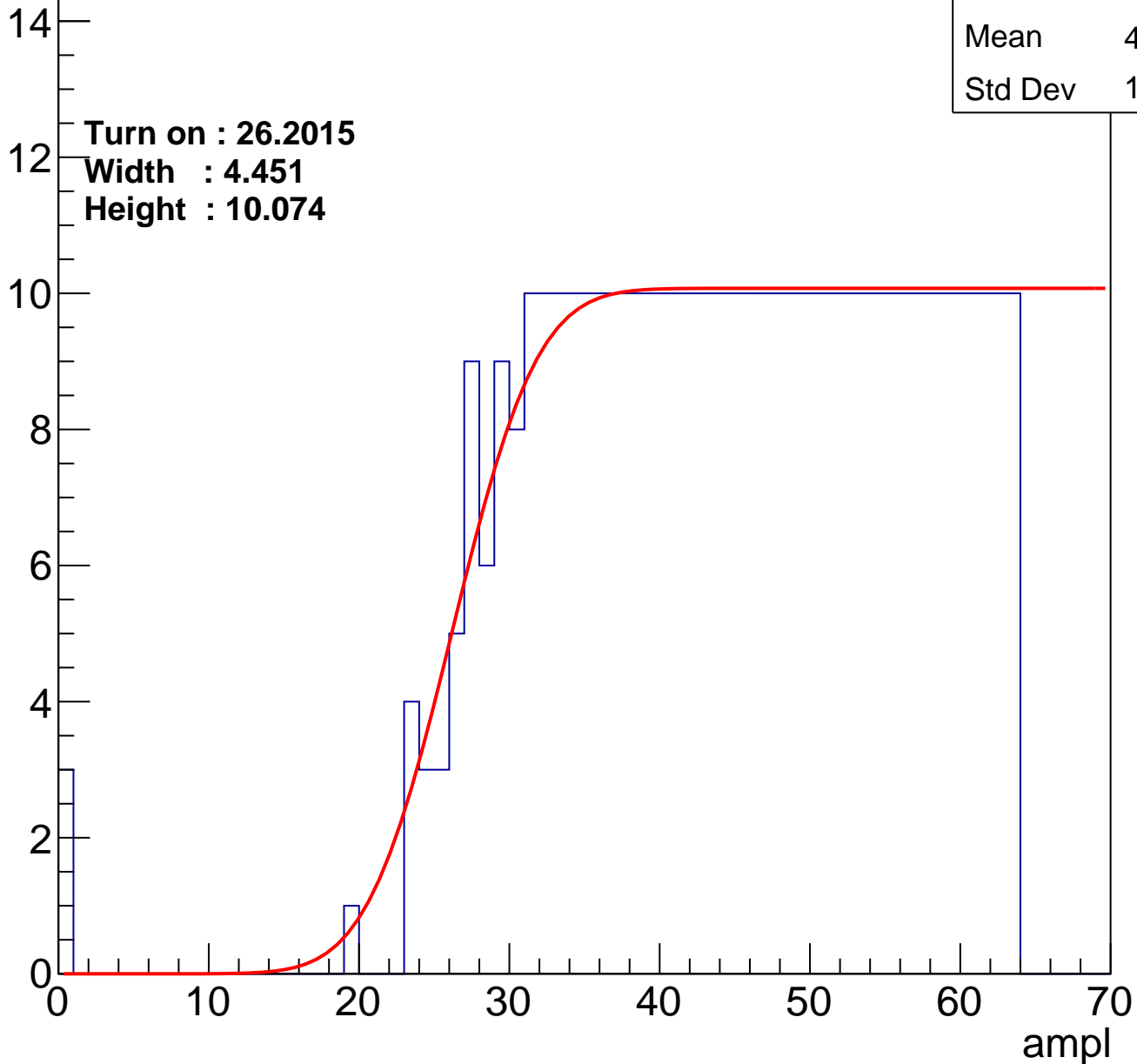
Entries	381
Mean	44.12
Std Dev	11.76

Turn on : 26.2015

Width : 4.451

Height : 10.074

Entry



B1L102S, U20-ch115

calib_packv5_042523_0143.root, FC#11, port A2

Entries	371
Mean	44.7
Std Dev	11.29

Turn on : 27.5061

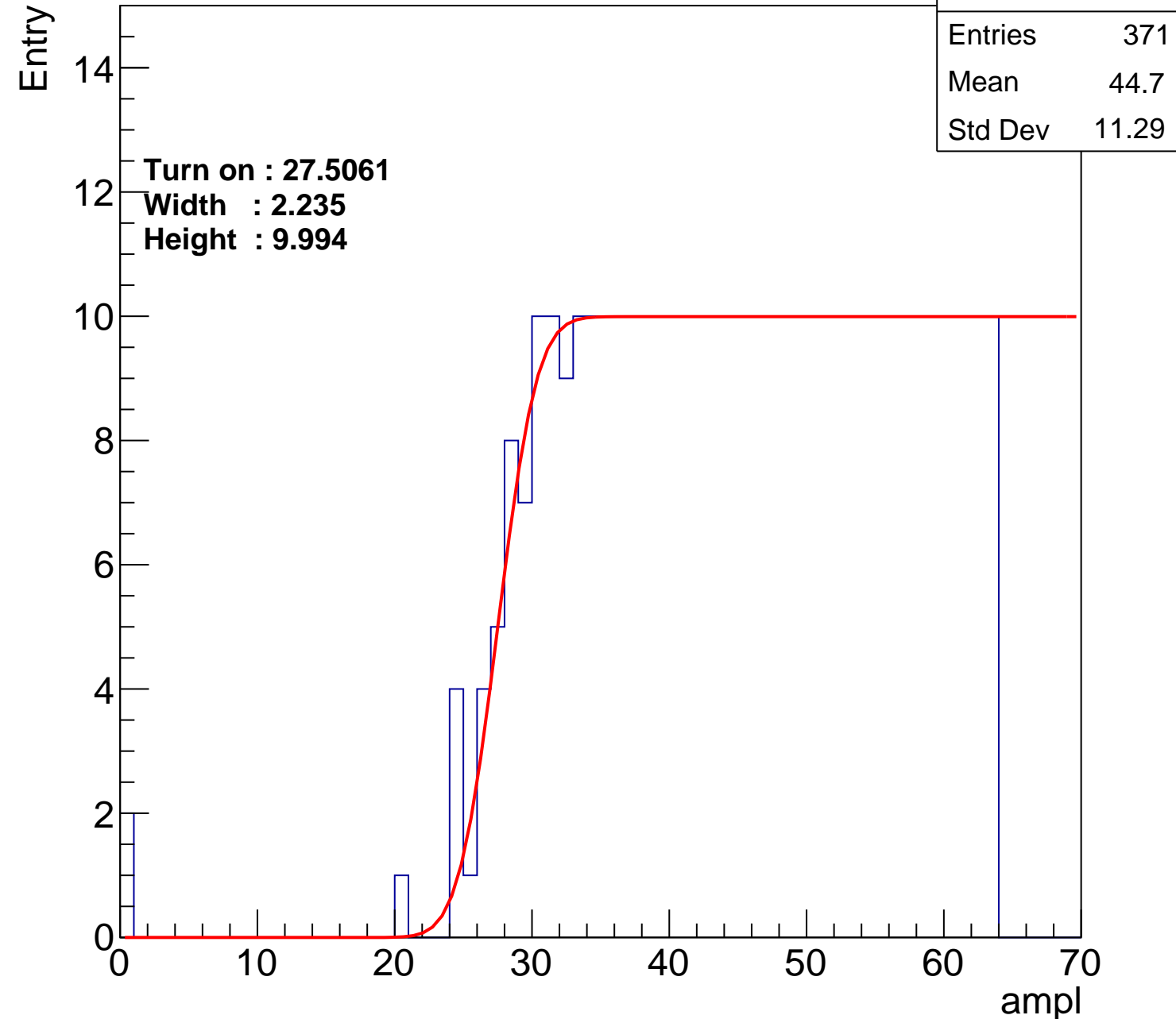
Width : 2.235

Height : 9.994

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U20-ch116

calib_packv5_042523_0143.root, FC#11, port A2

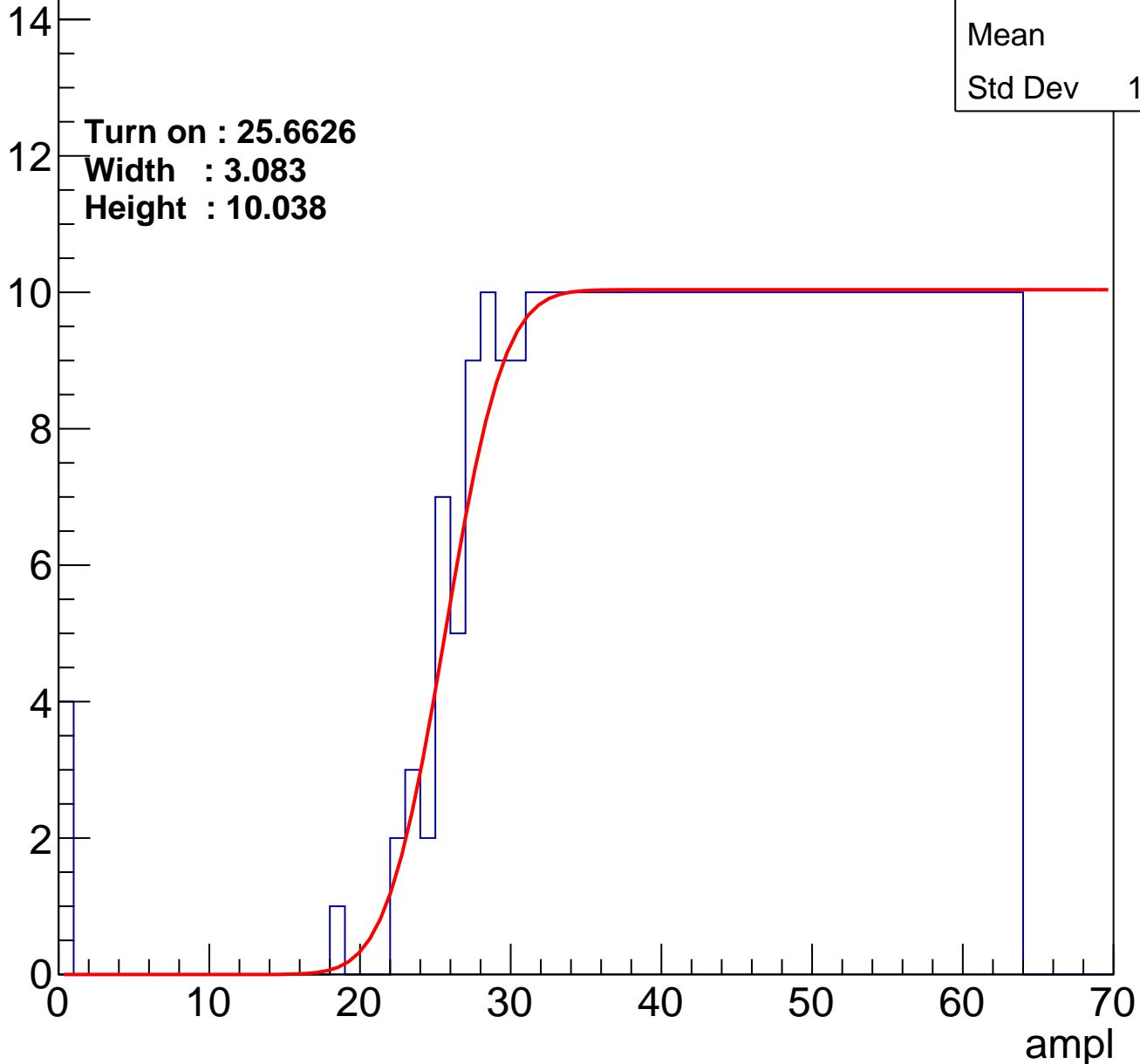
Entries	391
Mean	43.6
Std Dev	12.12

Turn on : 25.6626

Width : 3.083

Height : 10.038

Entry



B1L102S, U20-ch117

calib_packv5_042523_0143.root, FC#11, port A2

Entries	373
Mean	44.64
Std Dev	11.27

Turn on : 26.7259

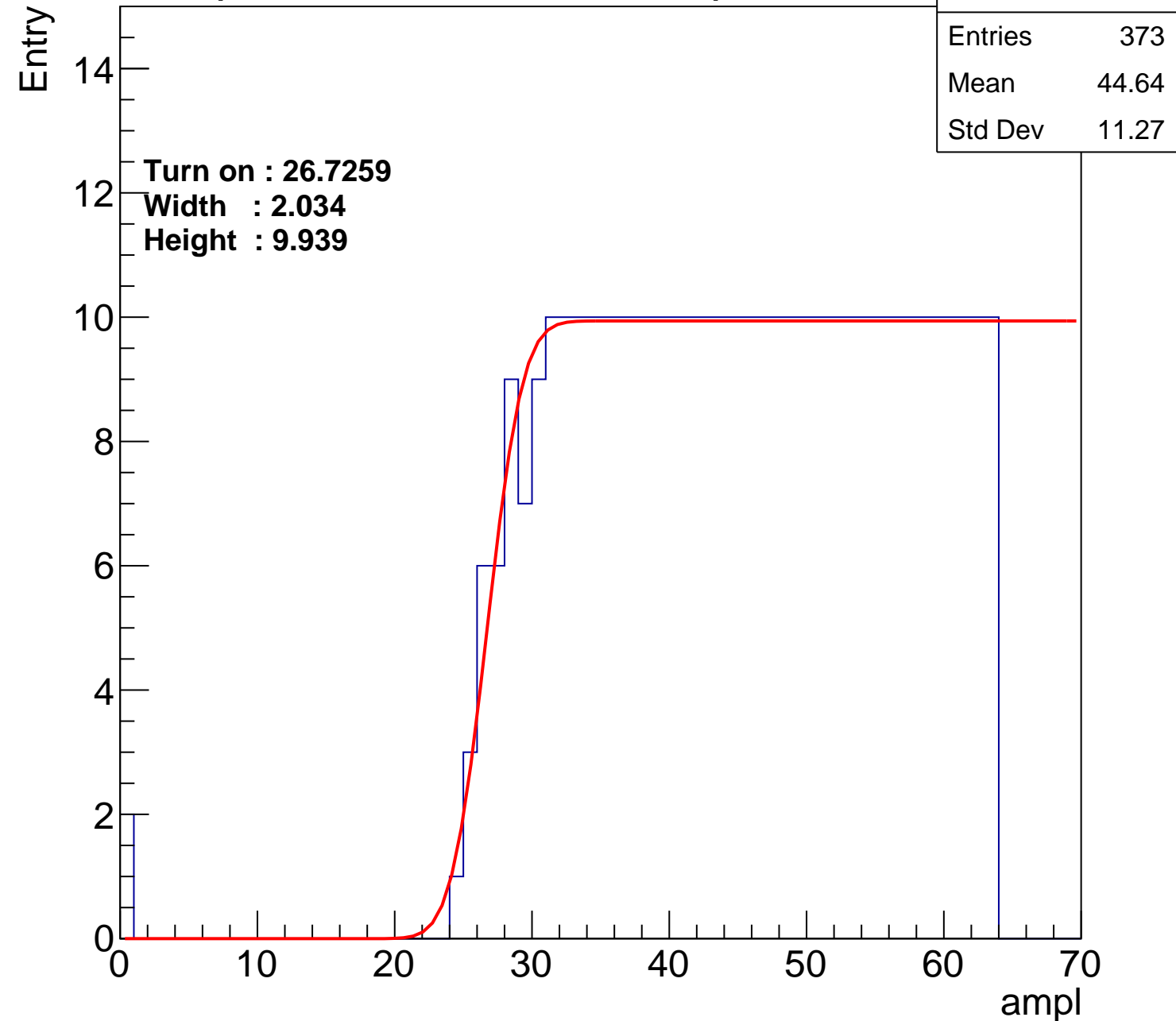
Width : 2.034

Height : 9.939

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U20-ch118

calib_packv5_042523_0143.root, FC#11, port A2

Entries	393
Mean	43.48
Std Dev	12.2

Turn on : 25.5765

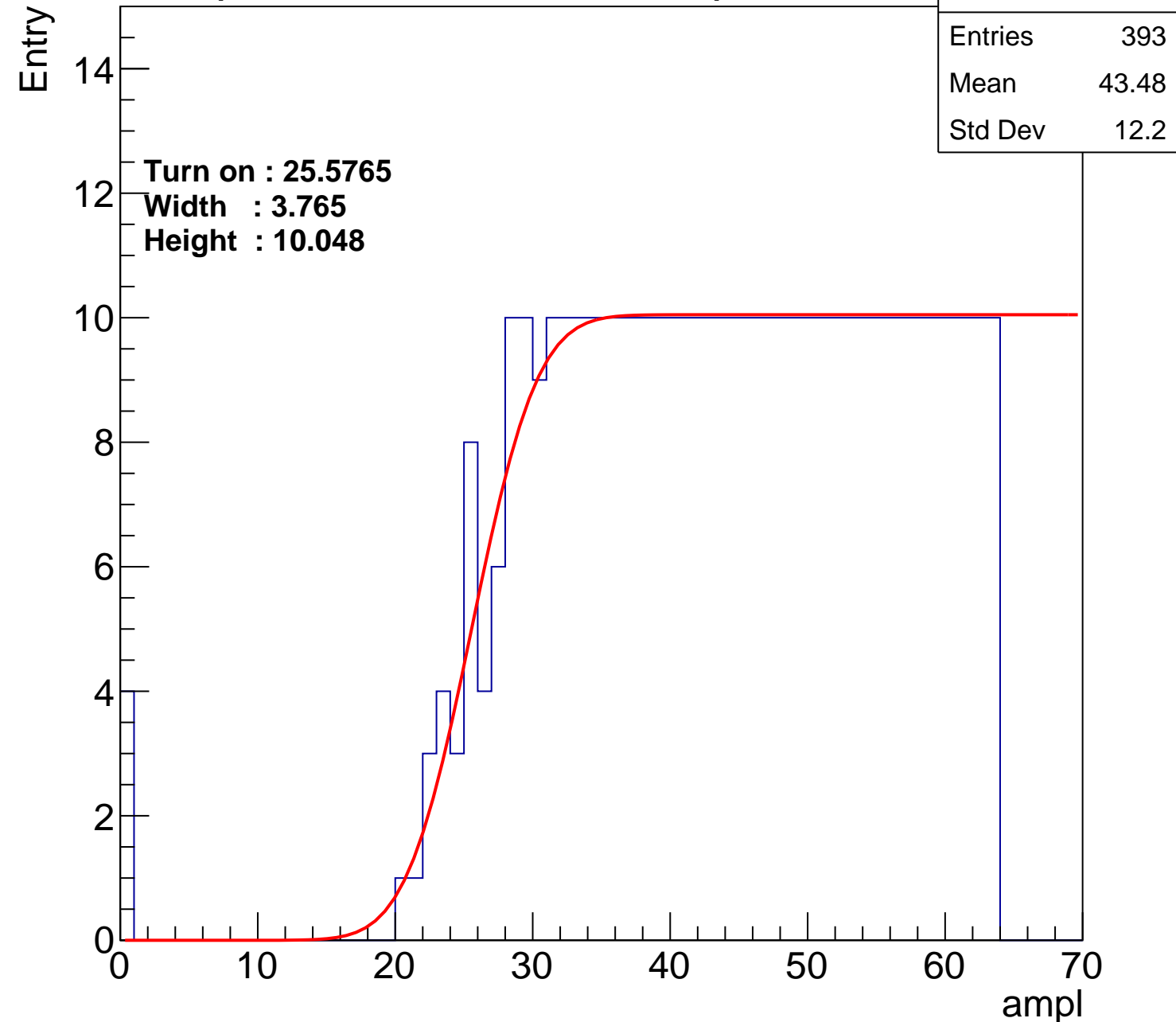
Width : 3.765

Height : 10.048

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U20-ch119

calib_packv5_042523_0143.root, FC#11, port A2

Entries	386
Mean	43.95
Std Dev	11.7

Turn on : 25.8382

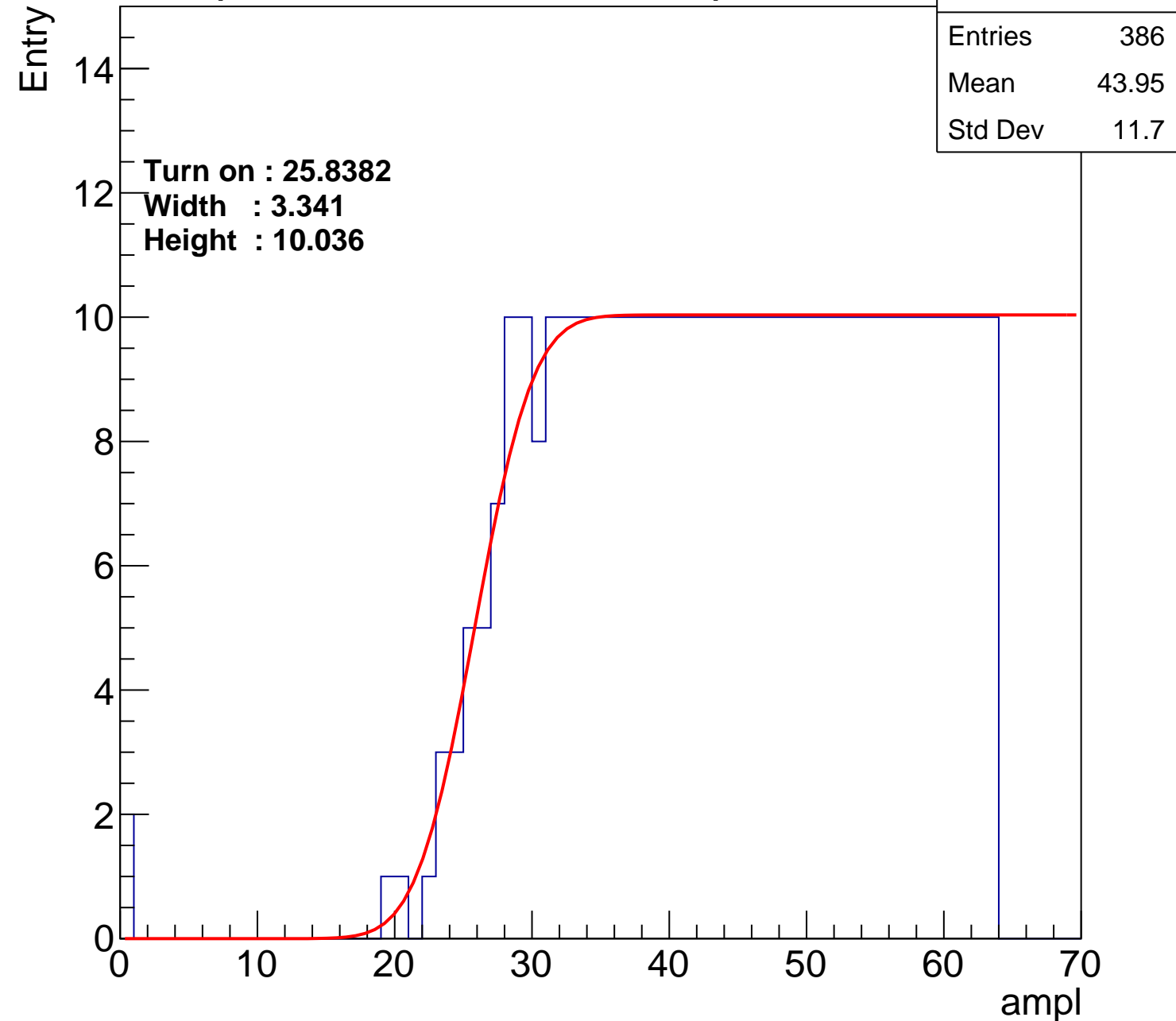
Width : 3.341

Height : 10.036

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U20-ch120

calib_packv5_042523_0143.root, FC#11, port A2

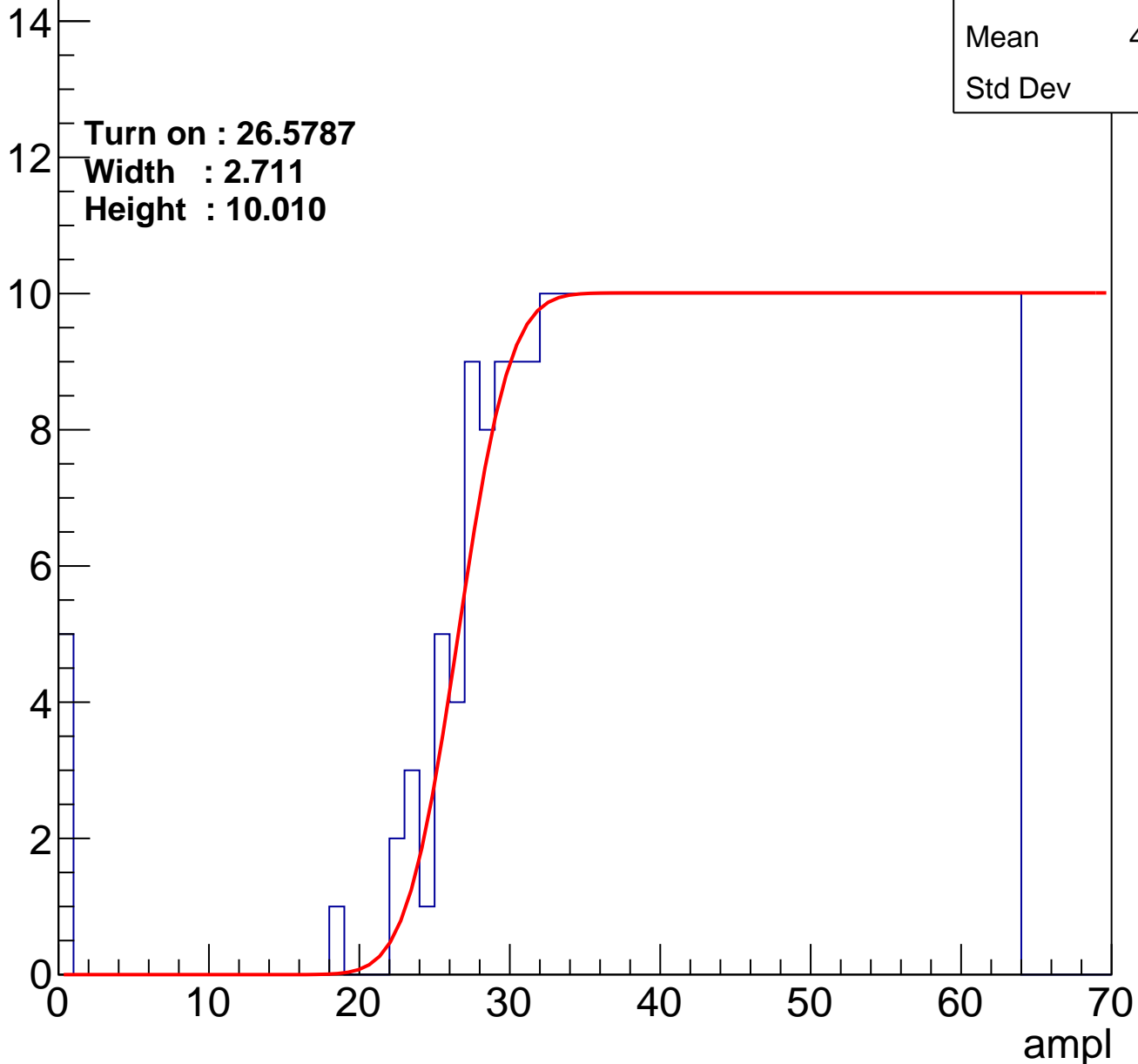
Entries	385
Mean	43.79
Std Dev	12.2

Turn on : 26.5787

Width : 2.711

Height : 10.010

Entry



B1L102S, U20-ch121

calib_packv5_042523_0143.root, FC#11, port A2

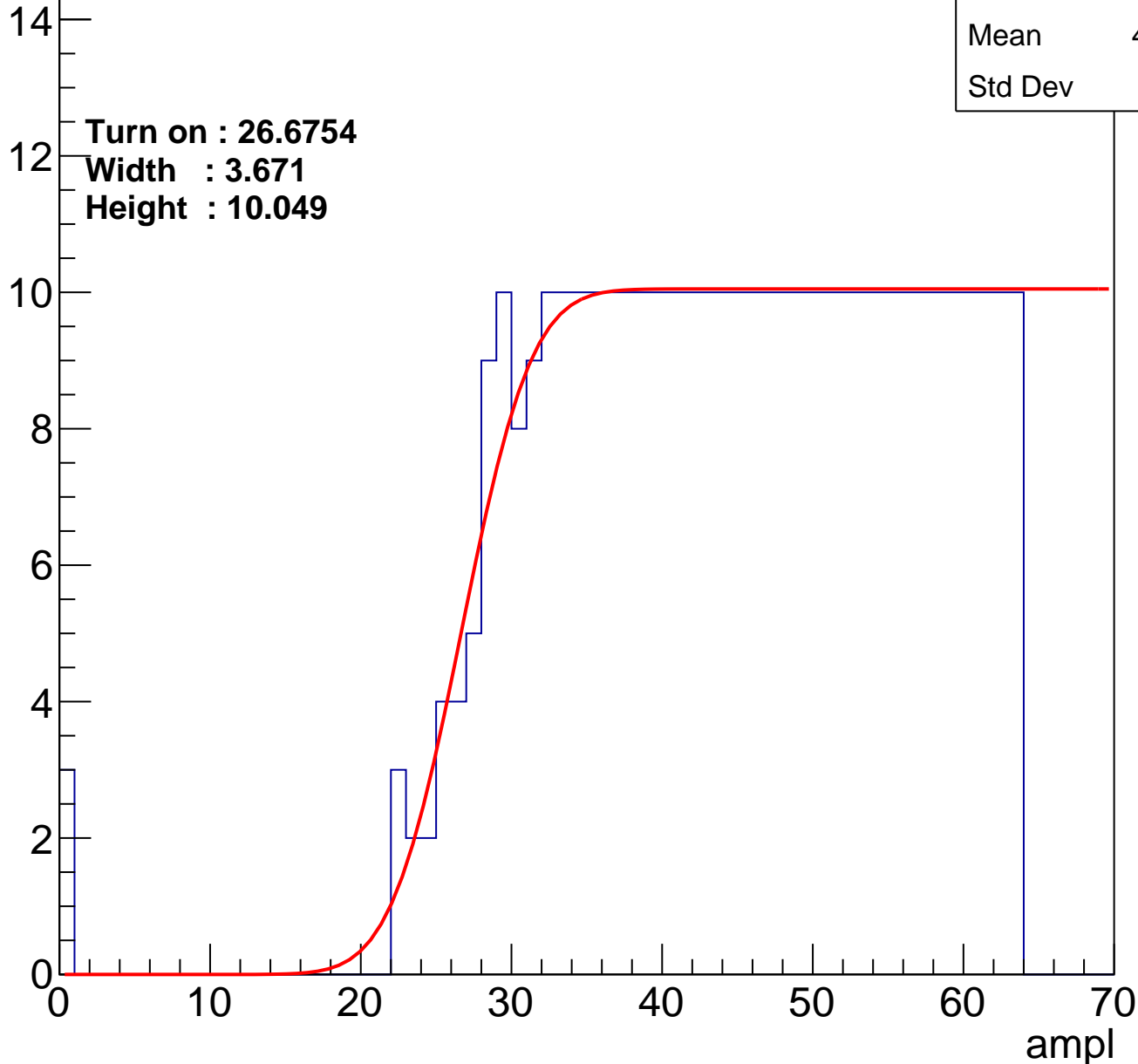
Entries	379
Mean	44.22
Std Dev	11.71

Turn on : 26.6754

Width : 3.671

Height : 10.049

Entry



B1L102S, U20-ch122

calib_packv5_042523_0143.root, FC#11, port A2

Entries	400
Mean	43.37
Std Dev	11.82

Turn on : 24.4779

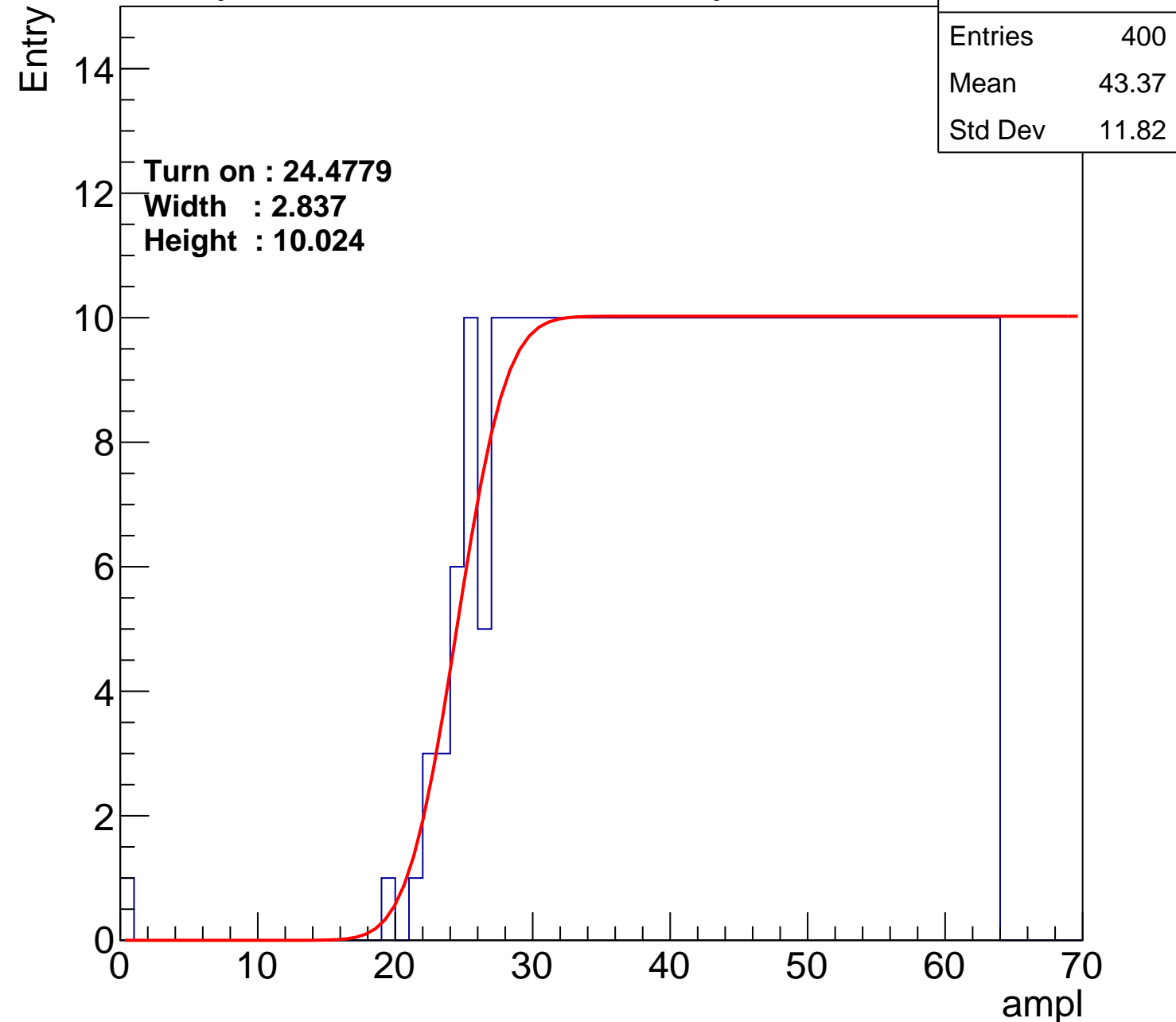
Width : 2.837

Height : 10.024

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U20-ch123

calib_packv5_042523_0143.root, FC#11, port A2

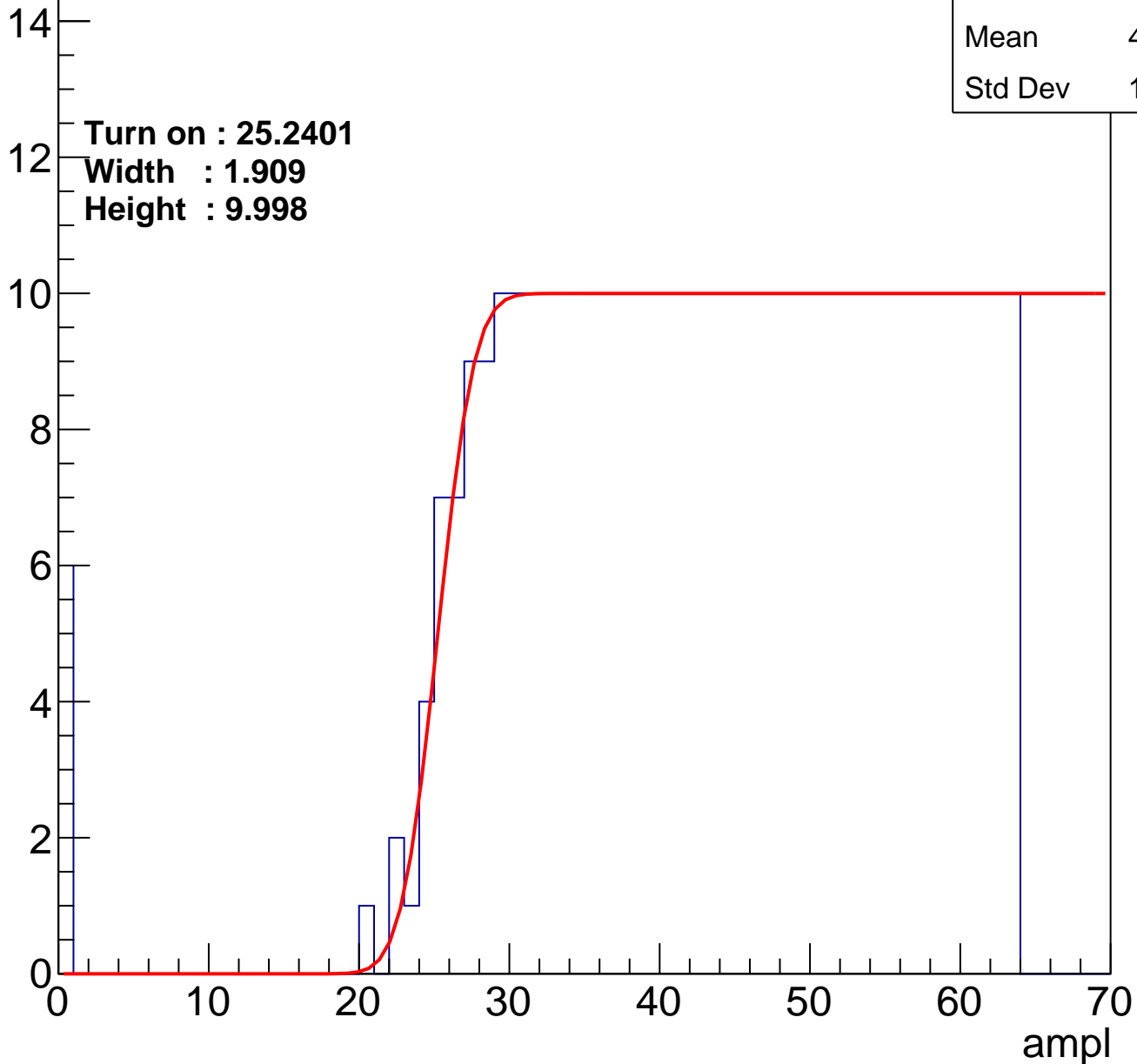
Entries	396
Mean	43.27
Std Dev	12.49

Turn on : 25.2401

Width : 1.909

Height : 9.998

Entry



B1L102S, U20-ch124

calib_packv5_042523_0143.root, FC#11, port A2

Entries	400
Mean	43.16
Std Dev	12.32

Turn on : 24.3309

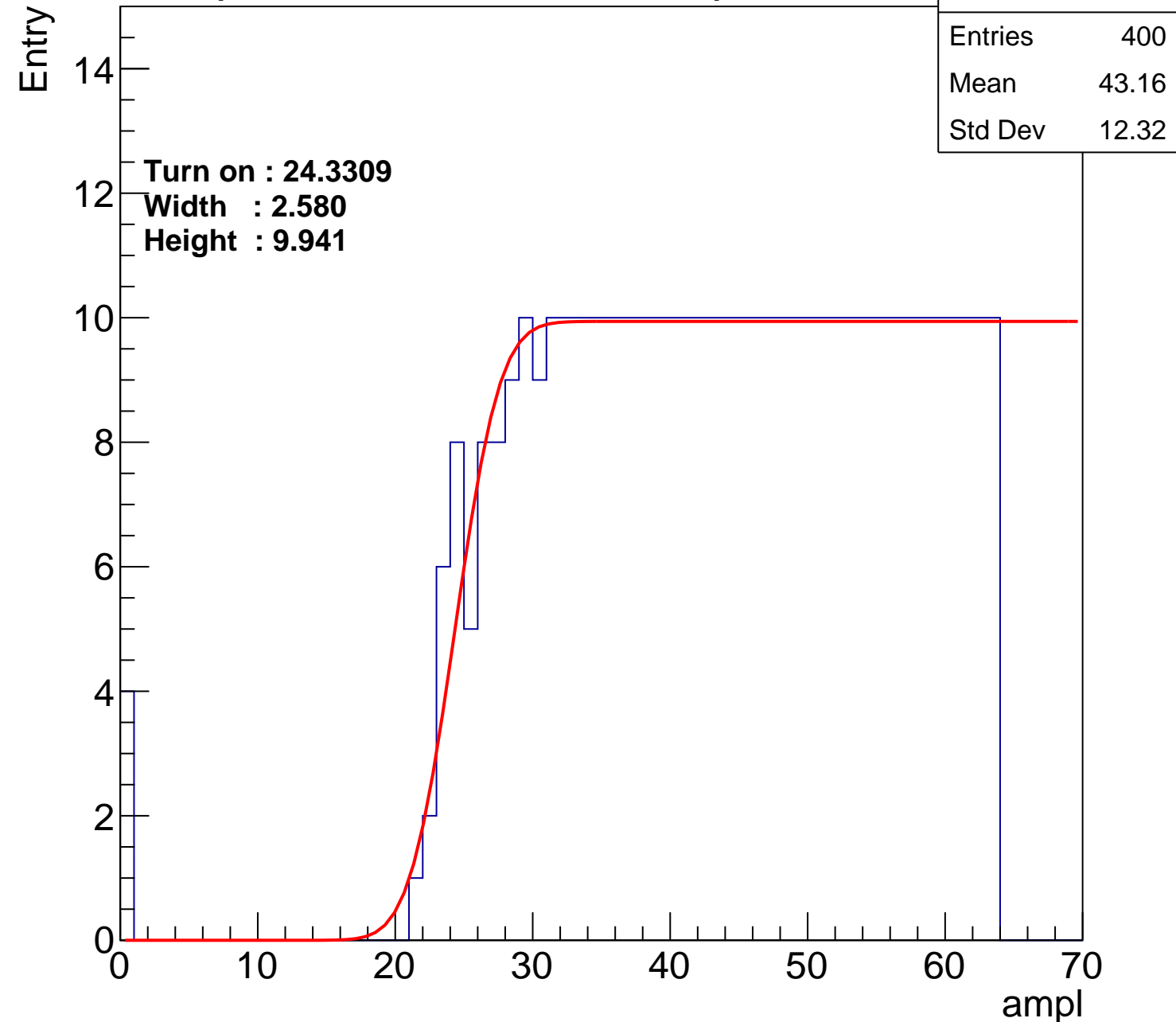
Width : 2.580

Height : 9.941

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U20-ch125

calib_packv5_042523_0143.root, FC#11, port A2

Entries	369
Mean	44.71
Std Dev	11.38

Turn on : 27.5297

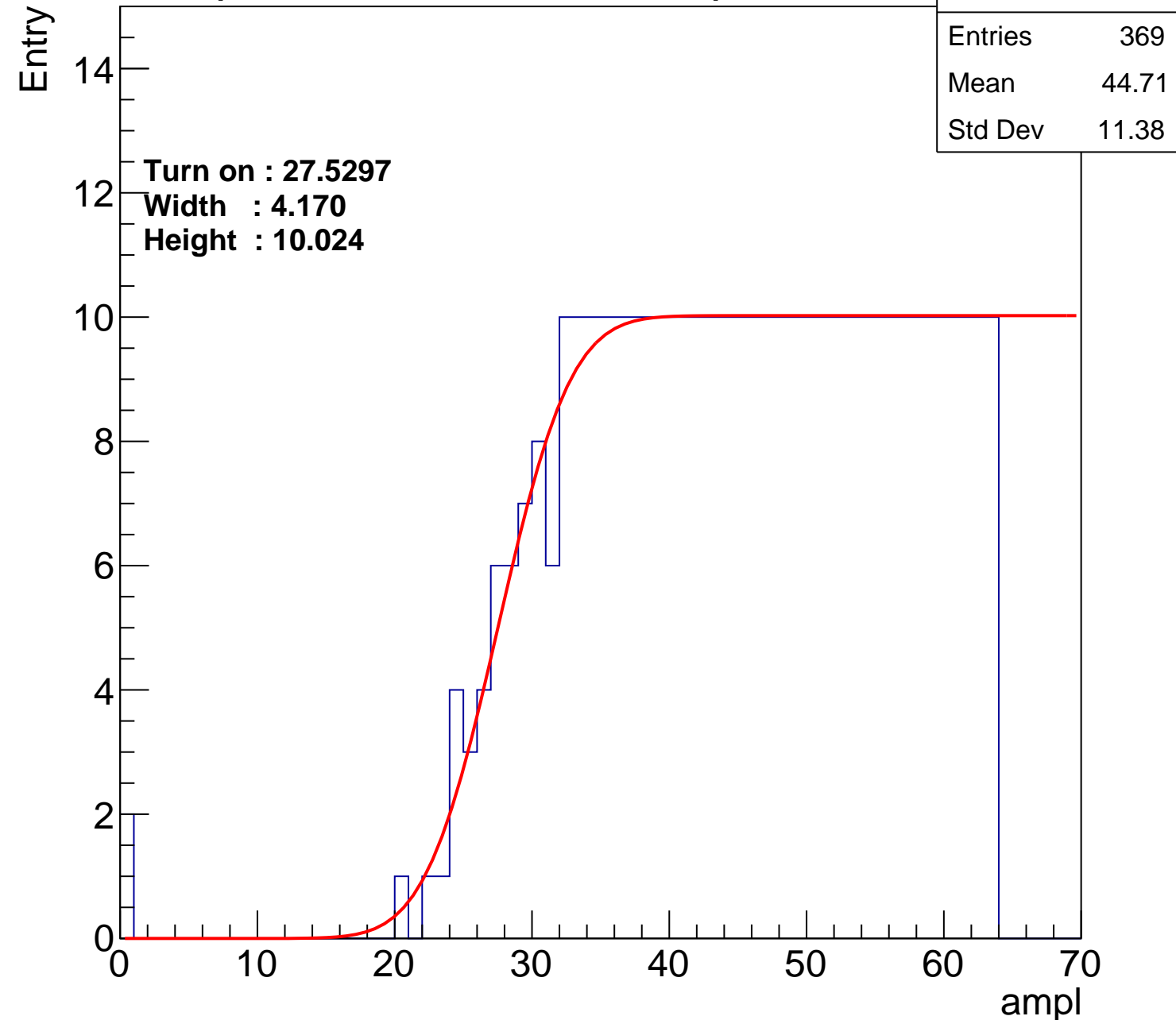
Width : 4.170

Height : 10.024

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U20-ch126

calib_packv5_042523_0143.root, FC#11, port A2

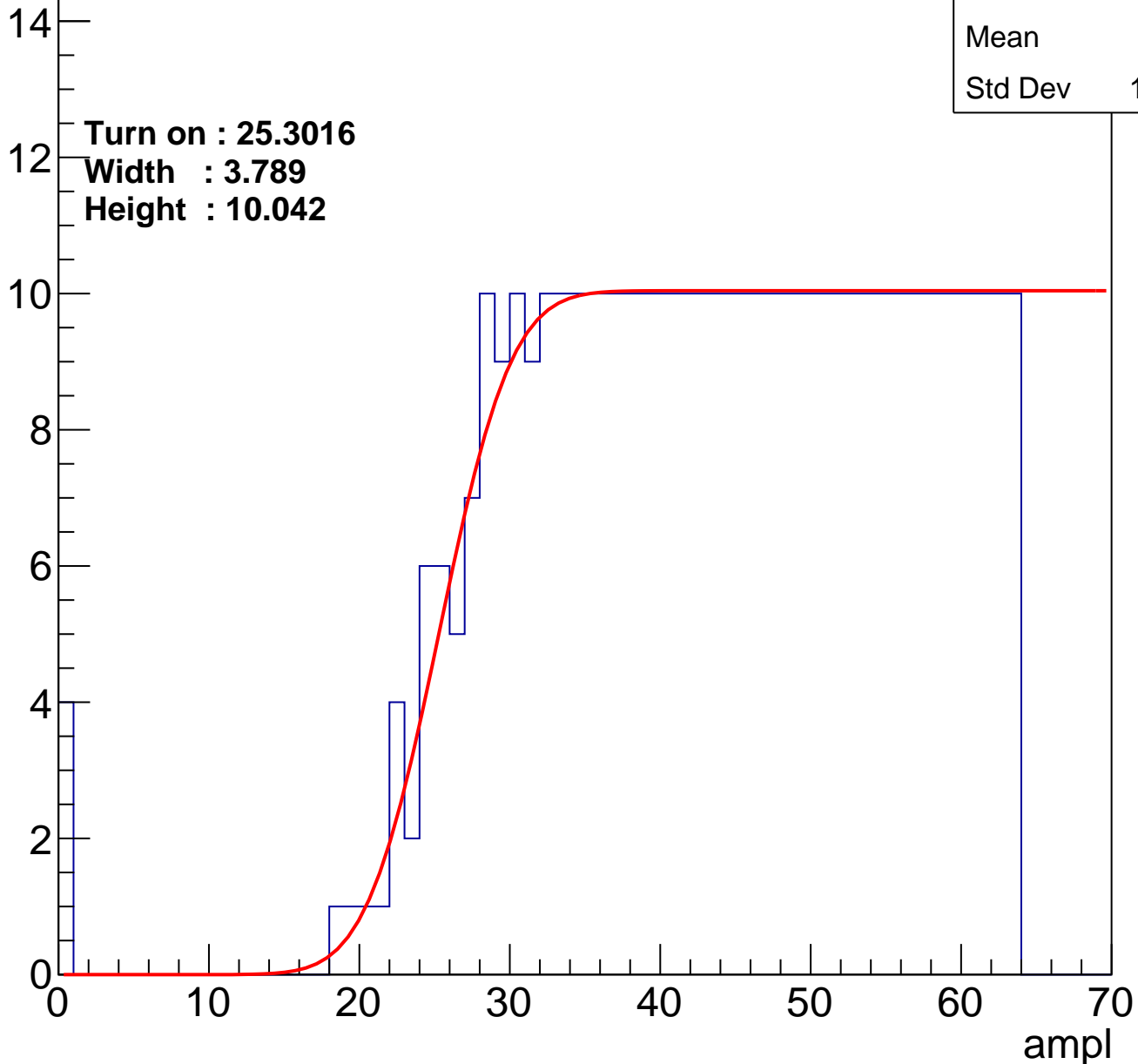
Entries	396
Mean	43.3
Std Dev	12.33

Turn on : 25.3016

Width : 3.789

Height : 10.042

Entry



B1L102S, U20-ch127

calib_packv5_042523_0143.root, FC#11, port A2

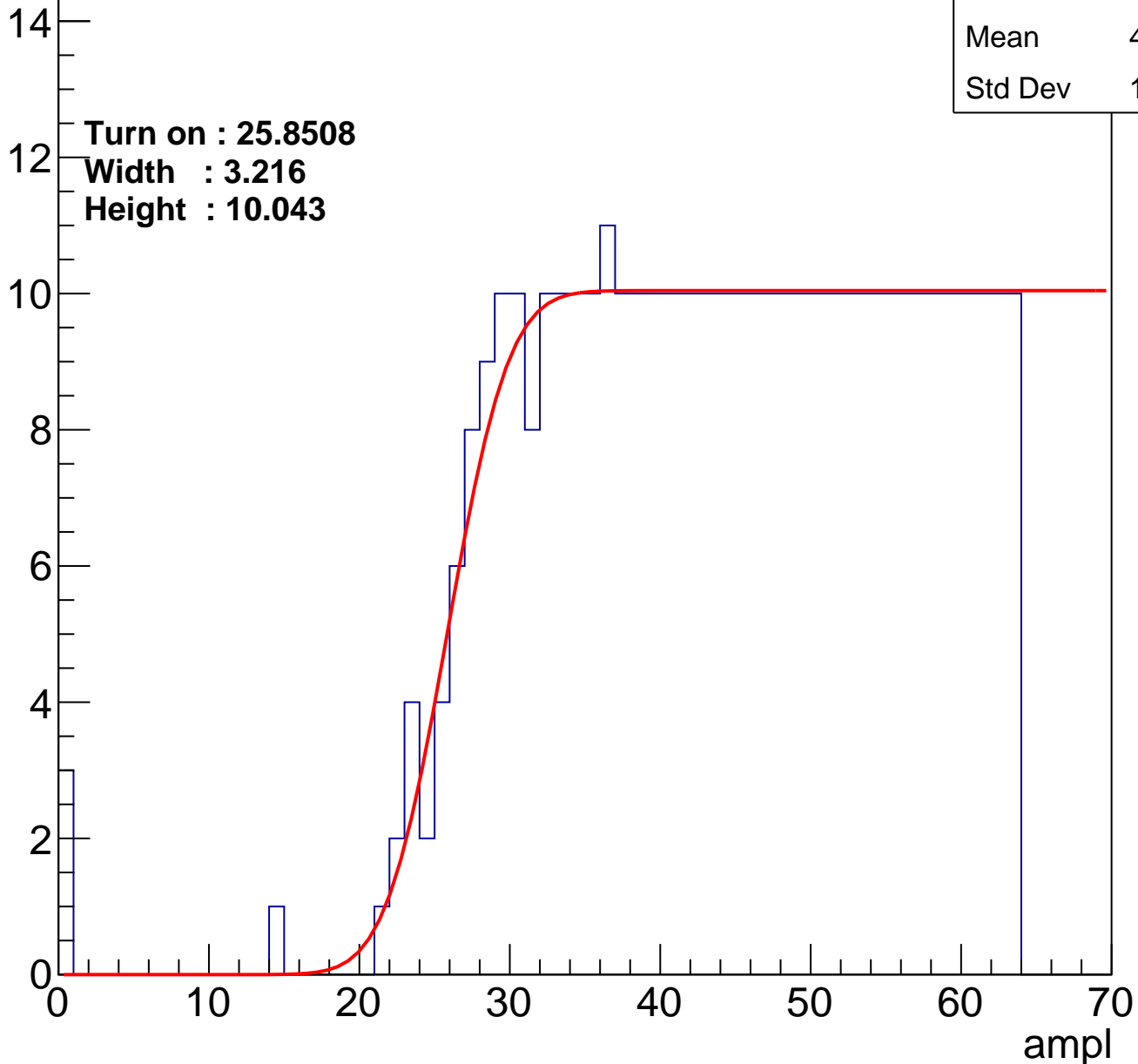
Entries	389
Mean	43.75
Std Dev	11.95

Turn on : 25.8508

Width : 3.216

Height : 10.043

Entry



B1L102S, U20-ch127

calib_packv5_042523_0143.root, FC#11, port A2

Entries	389
Mean	43.75
Std Dev	11.95

Turn on : 25.8508

Width : 3.216

Height : 10.043

Entry

14
12
10
8
6
4
2
0

ampl

