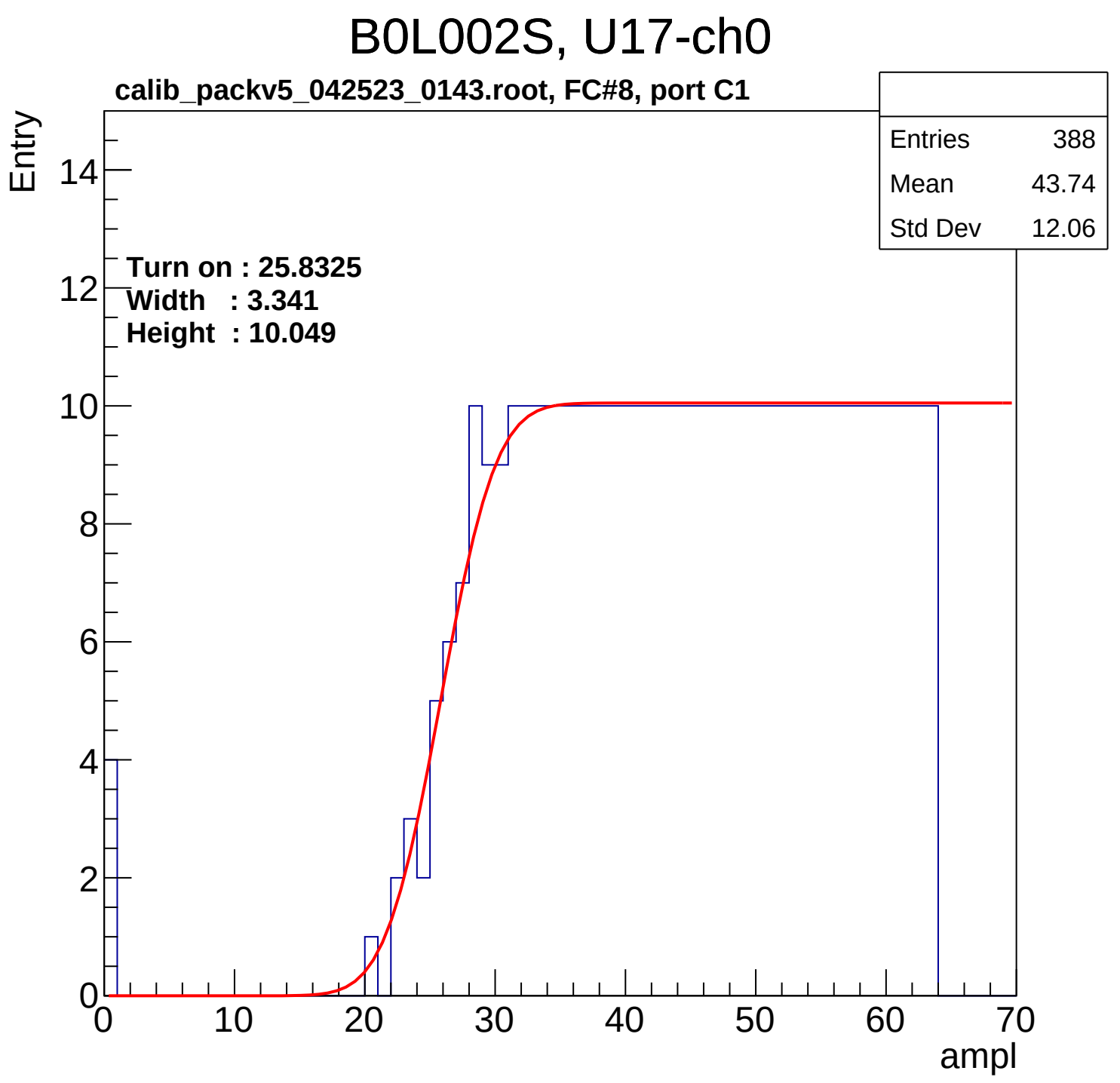
B0L002S, U17-ch0
calib_packv5_042523_0143.root, FC#8, port C1
Entries 388
Mean 43.74
Std Dev 12.06
Turn on : 25.8325
Width : 3.341
Height : 10.049
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ampl
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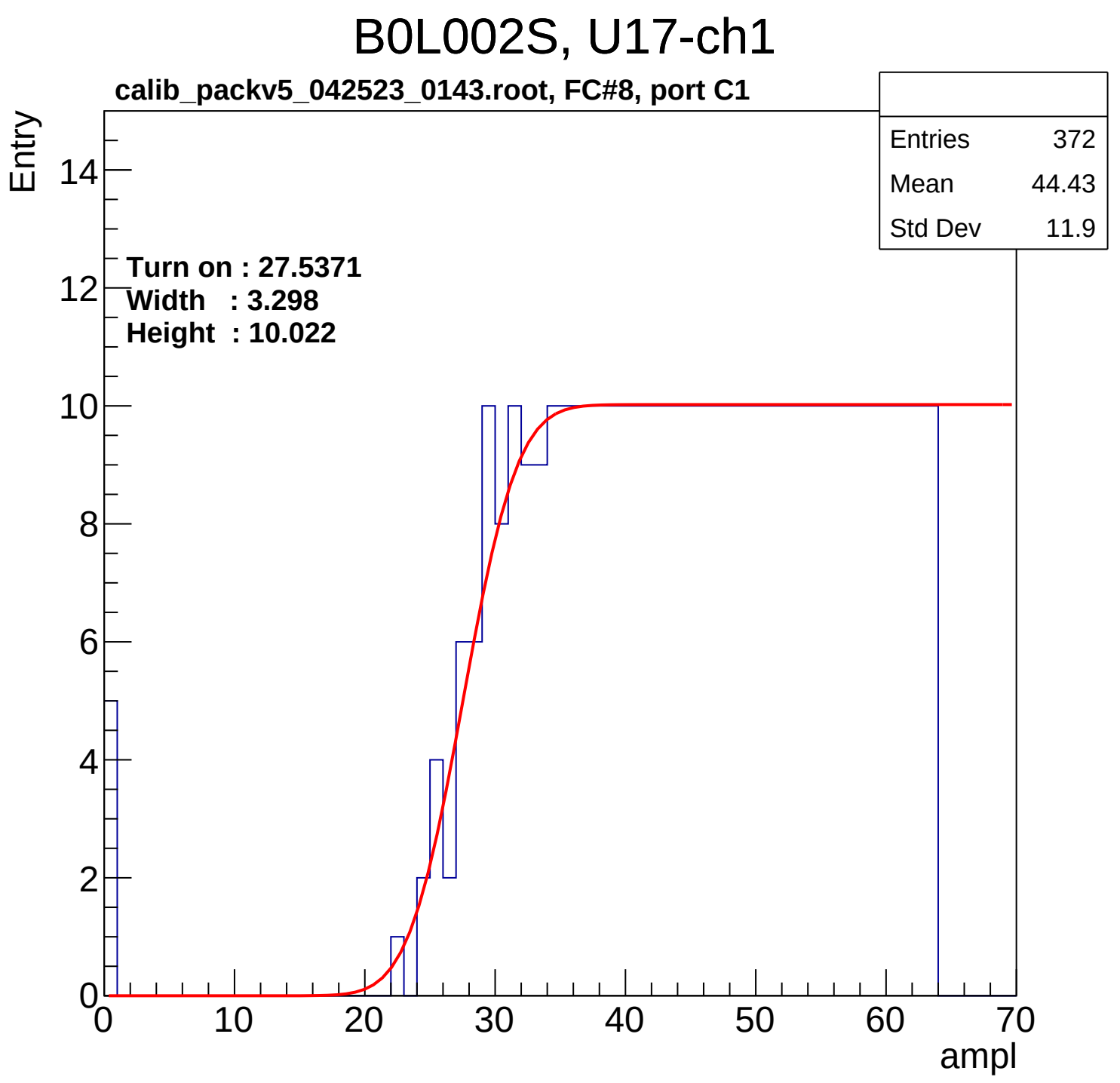
B0L002S, U17-ch1
calib_packv5_042523_0143.root, FC#8, port C1
Entries 372
Mean 44.43
Std Dev 11.9
Turn on : 27.5371
Width : 3.298
Height : 10.022
Entry
ampl
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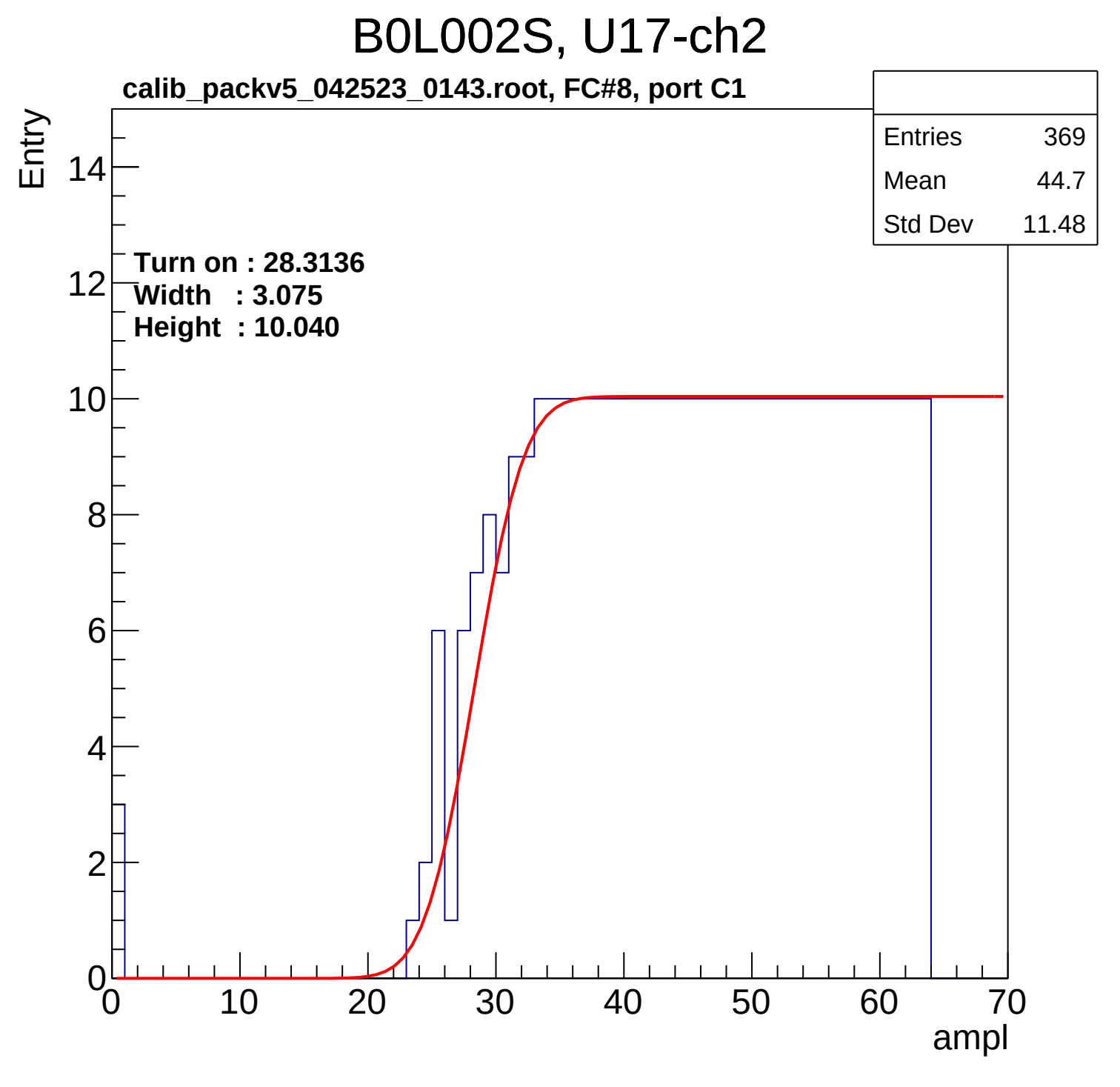
B0L002S, U17-ch2
calib_packv5_042523_0143.root, FC#8, port C1
Entries 369
Mean 44.7
Std Dev 11.48
Turn on : 28.3136
Width : 3.075
Height : 10.040
Entry
ampl
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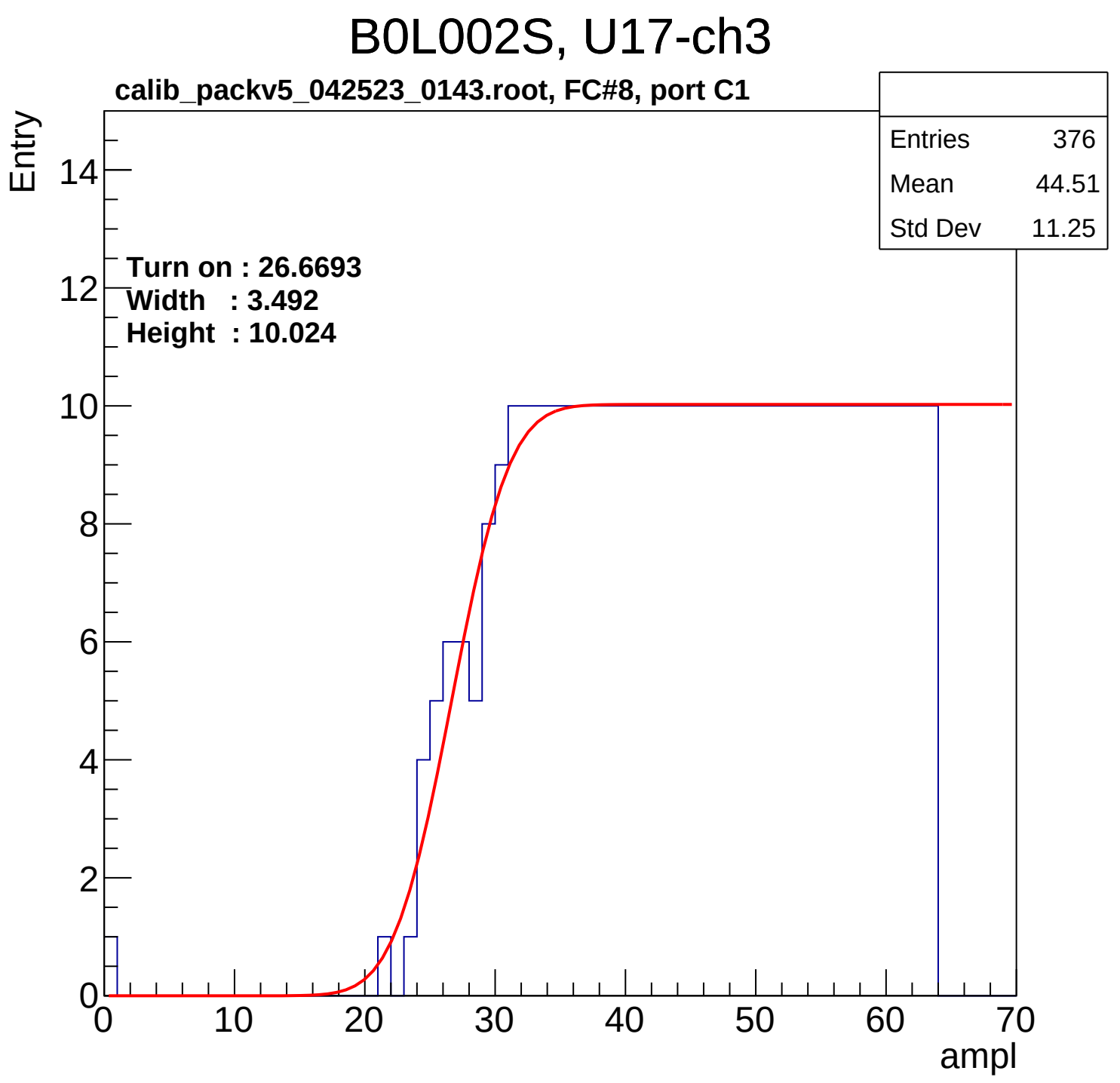
B0L002S, U17-ch3
calib_packv5_042523_0143.root, FC#8, port C1
Entries 376
Mean 44.51
Std Dev 11.25
Turn on : 26.6693
Width : 3.492
Height : 10.024
Entry
ampl
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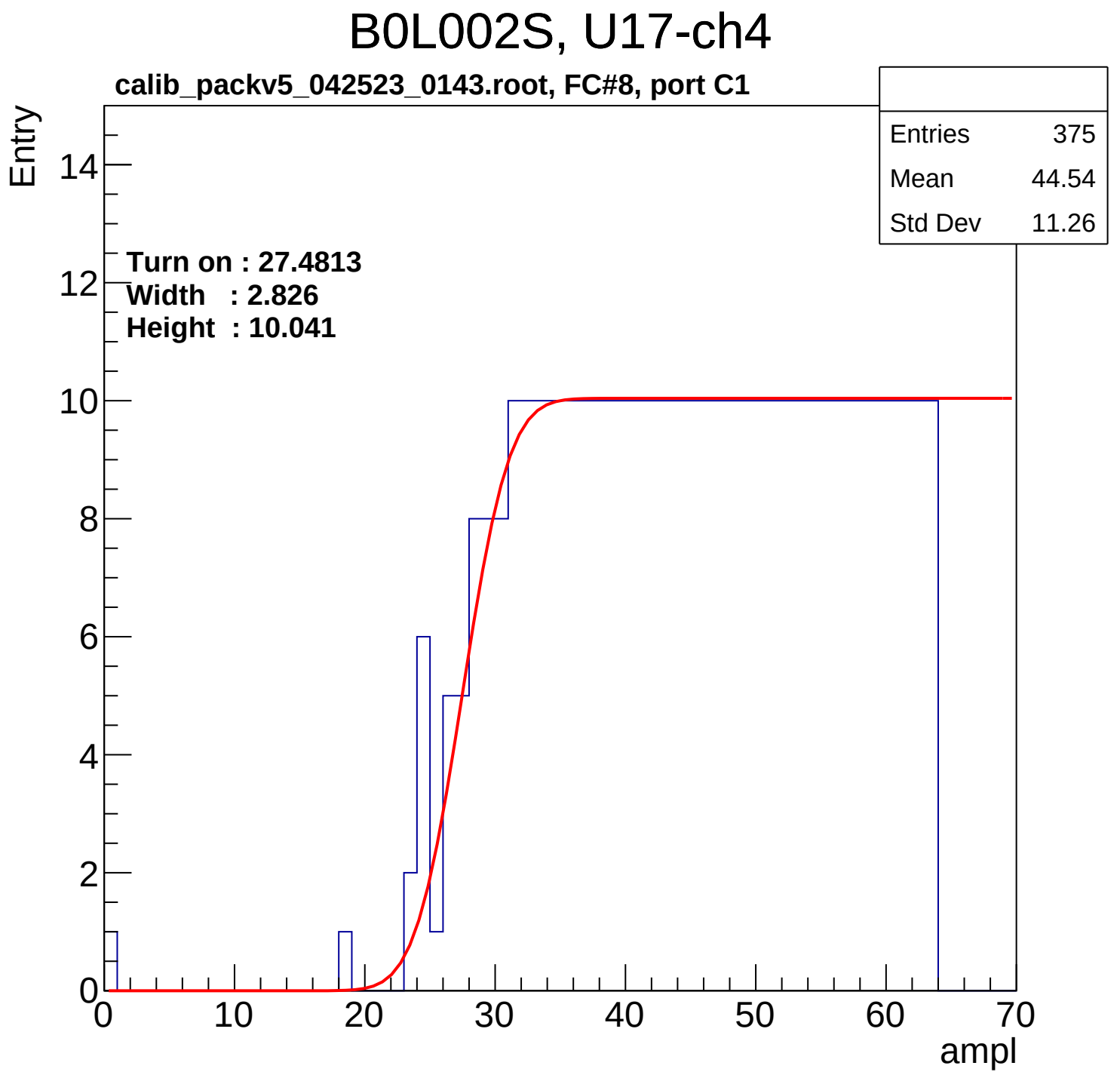
B0L002S, U17-ch4
calib_packv5_042523_0143.root, FC#8, port C1
Entries 375
Mean 44.54
Std Dev 11.26
Turn on : 27.4813
Width : 2.826
Height : 10.041
Entry
ampl
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2
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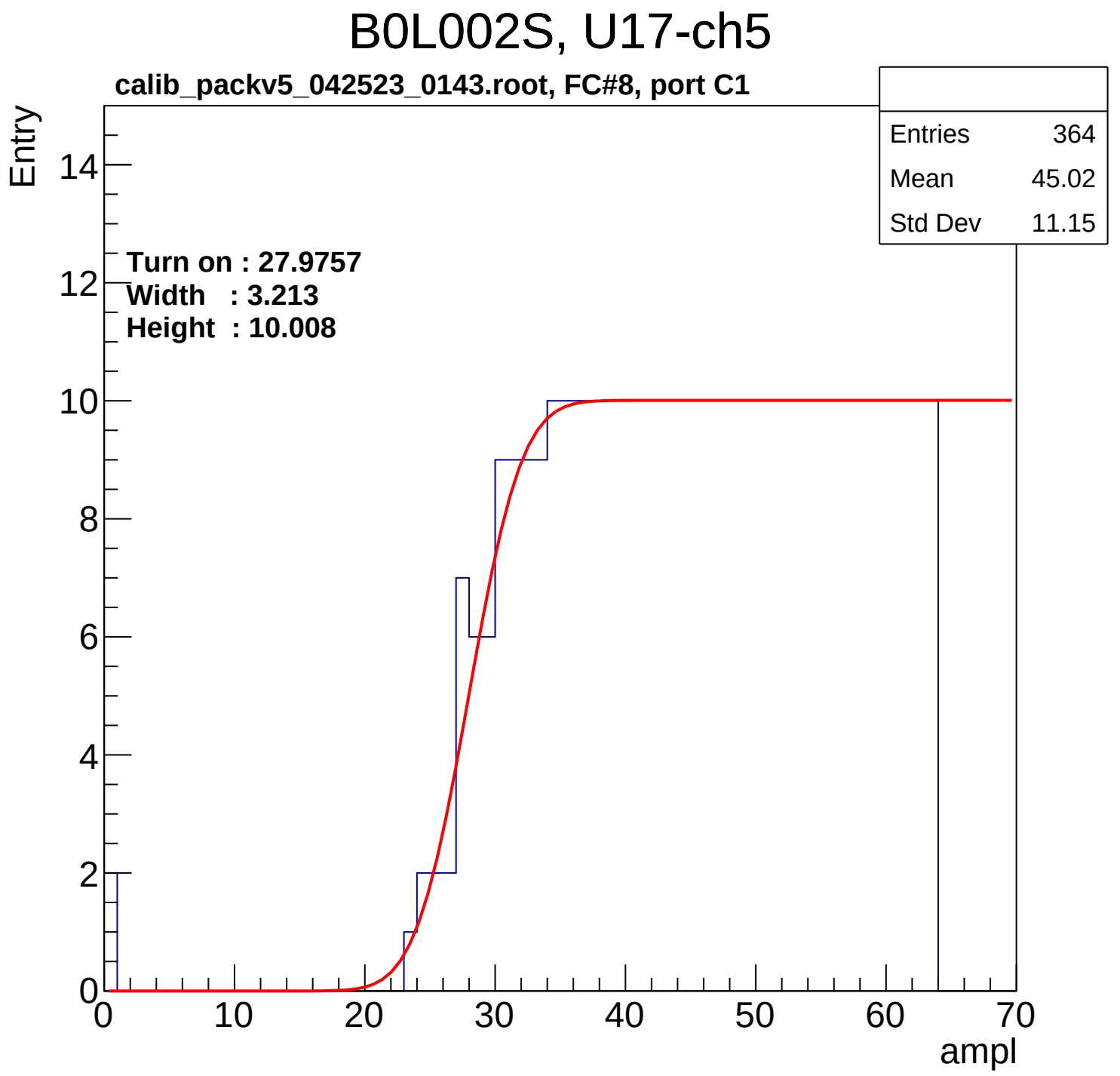
B0L002S, U17-ch5
calib_packv5_042523_0143.root, FC#8, port C1
Entries 364
Mean 45.02
Std Dev 11.15
Turn on : 27.9757
Width : 3.213
Height : 10.008
Entry
ampl
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6
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0
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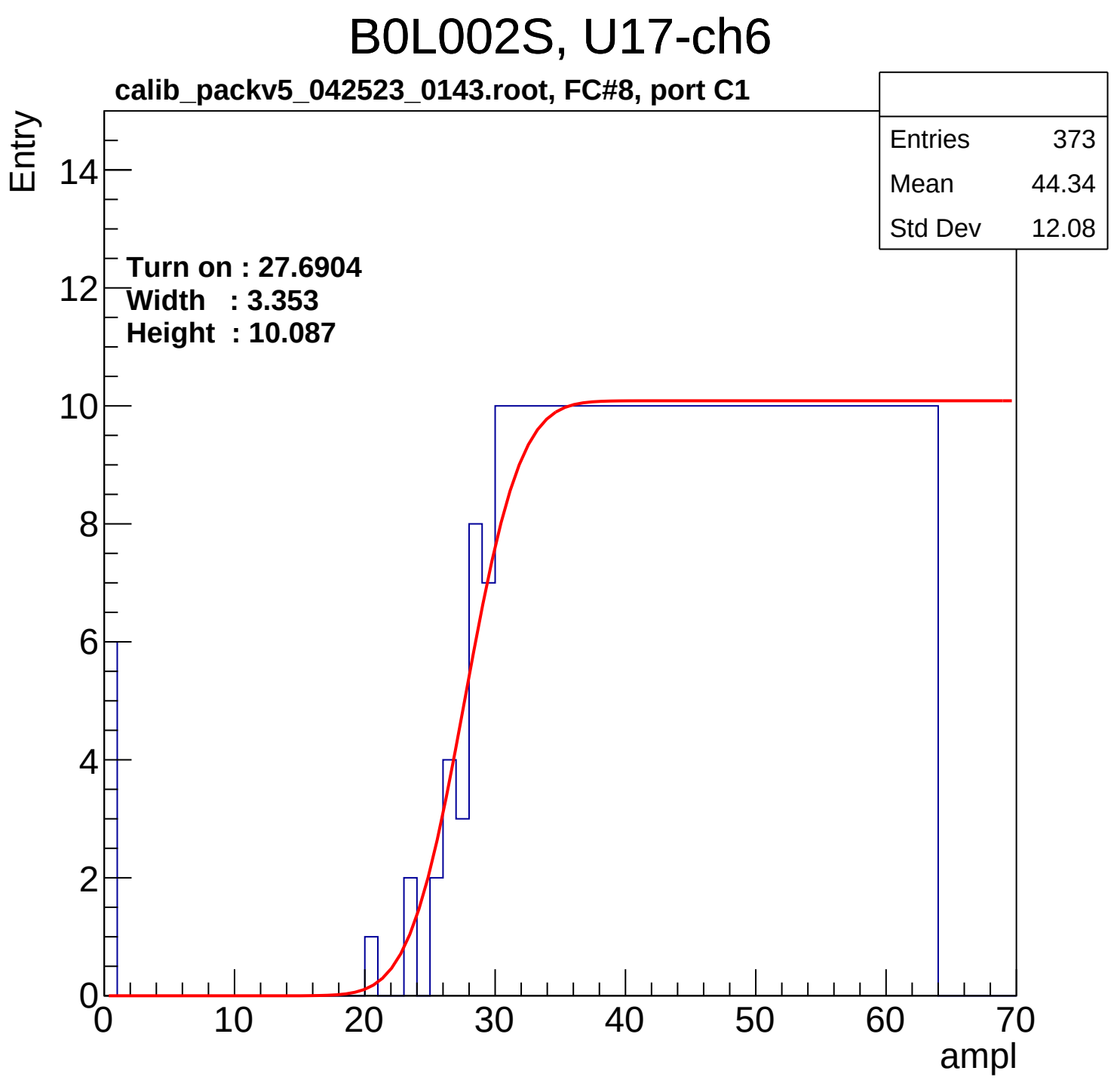
B0L002S, U17-ch6
calib_packv5_042523_0143.root, FC#8, port C1
Entries 373
Mean 44.34
Std Dev 12.08
Turn on : 27.6904
Width : 3.353
Height : 10.087
Entry
ampl
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2
4
6
8
10
12
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0
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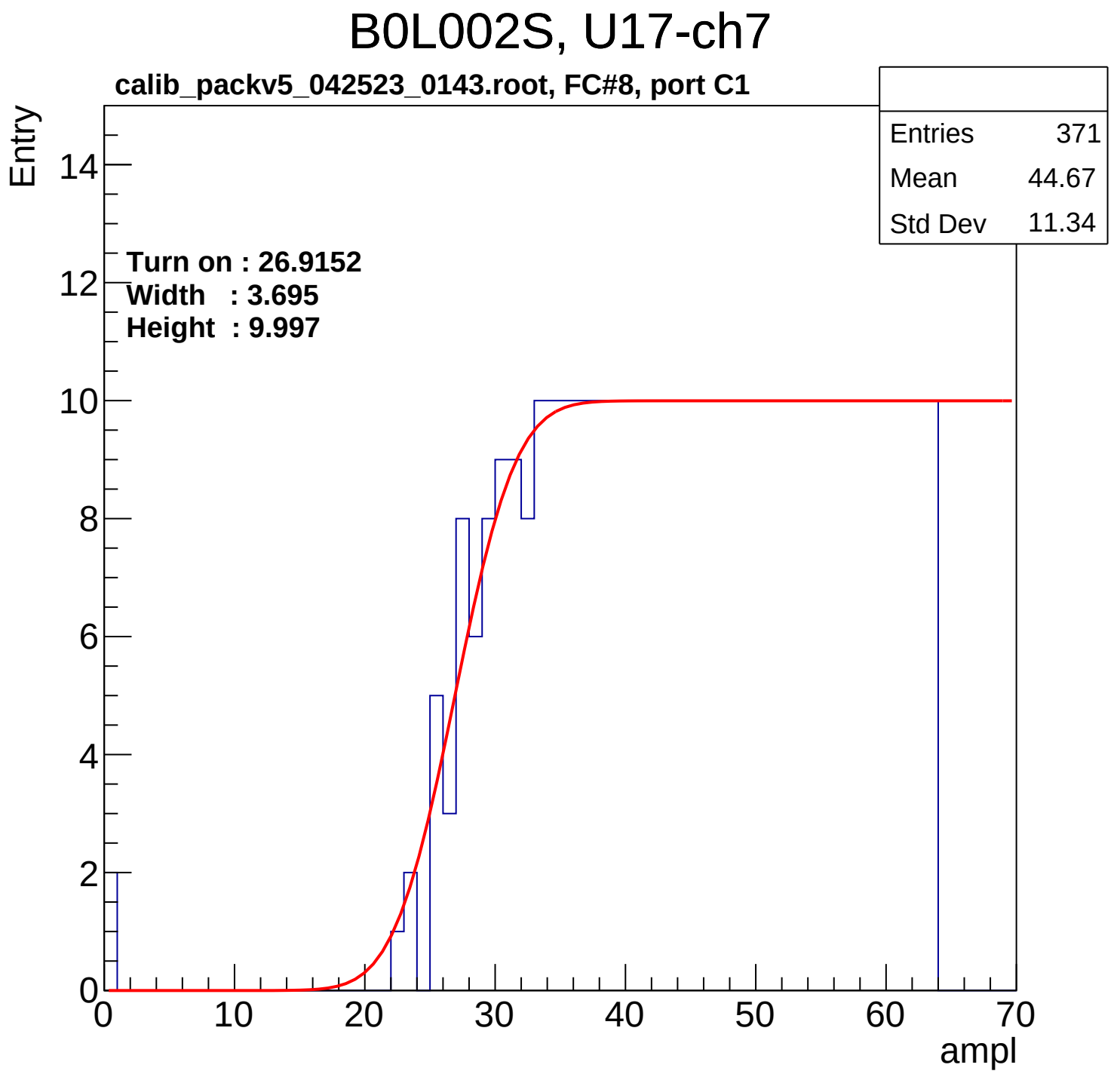
B0L002S, U17-ch7
calib_packv5_042523_0143.root, FC#8, port C1
Entries 371
Mean 44.67
Std Dev 11.34
Turn on : 26.9152
Width : 3.695
Height : 9.997
Entry
ampl
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2
4
6
8
10
12
14
0
10
20
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60
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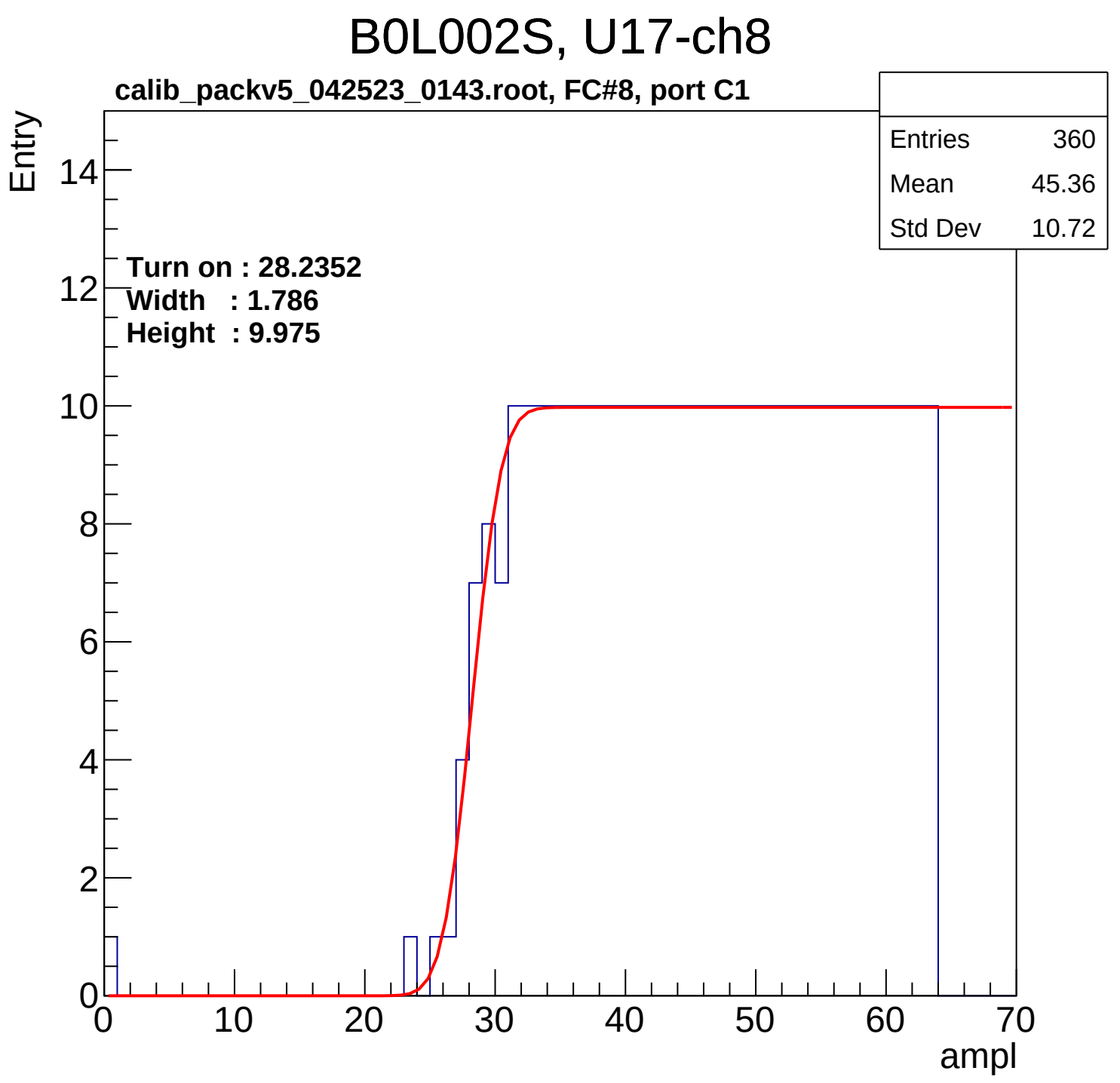
B0L002S, U17-ch8
calib_packv5_042523_0143.root, FC#8, port C1
Entries 360
Mean 45.36
Std Dev 10.72
Turn on : 28.2352
Width : 1.786
Height : 9.975
Entry
ampl
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6
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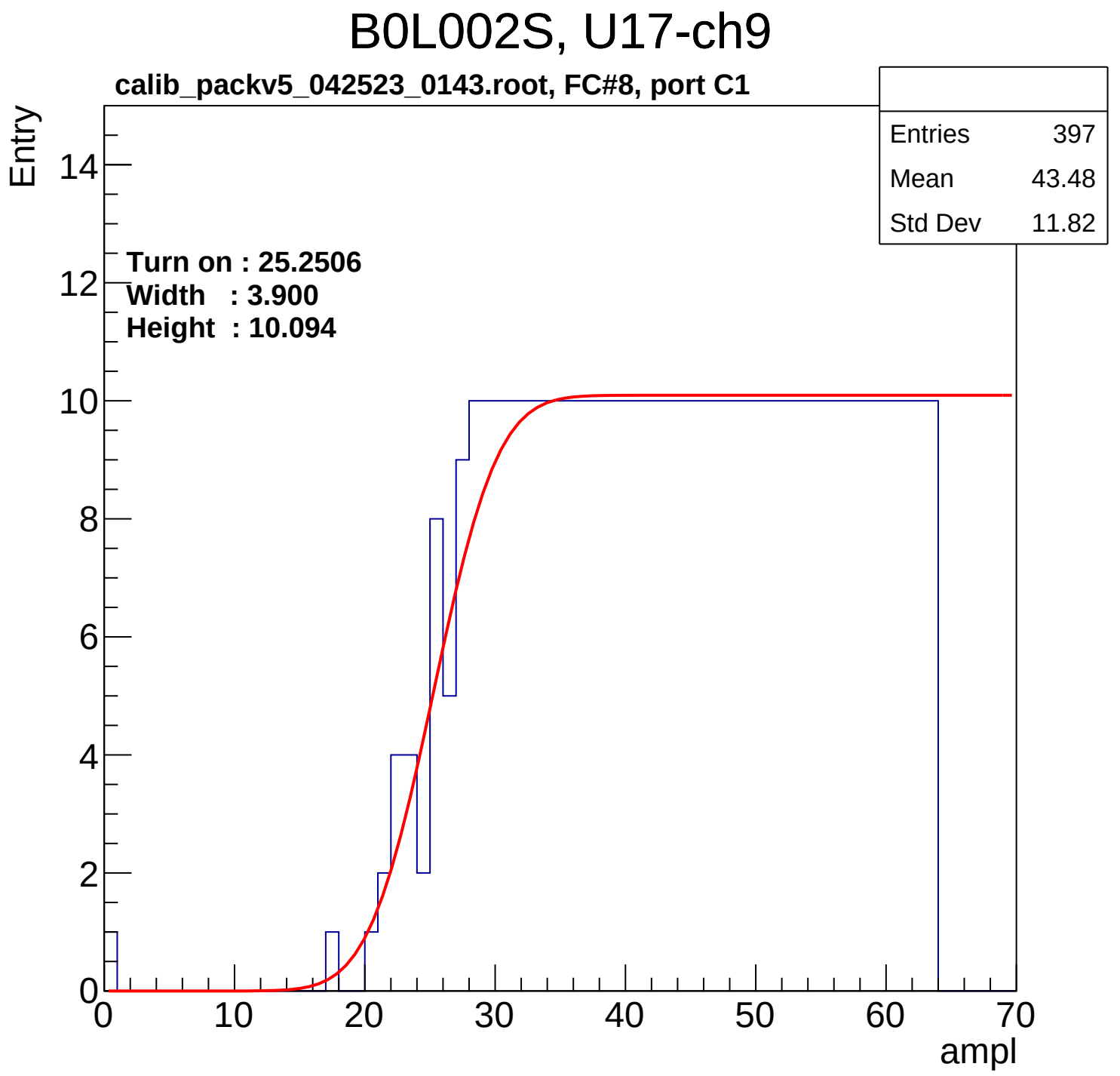
B0L002S, U17-ch9
calib_packv5_042523_0143.root, FC#8, port C1
Entries 397
Mean 43.48
Std Dev 11.82
Turn on : 25.2506
Width : 3.900
Height : 10.094
Entry
ampl
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2
4
6
8
10
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0
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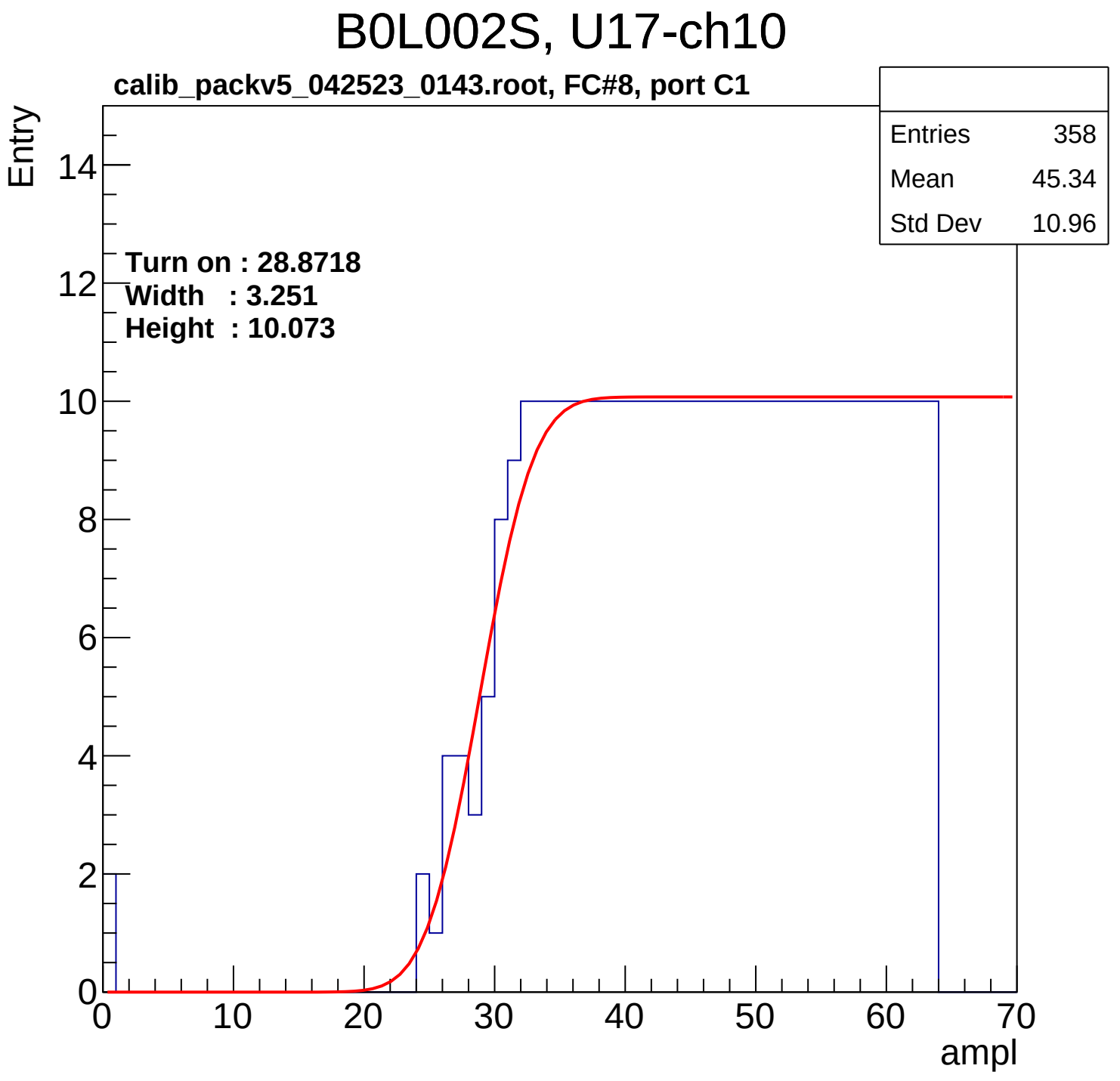
B0L002S, U17-ch10
calib_packv5_042523_0143.root, FC#8, port C1
Entries 358
Mean 45.34
Std Dev 10.96
Turn on : 28.8718
Width : 3.251
Height : 10.073
Entry
ampl
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4
6
8
10
12
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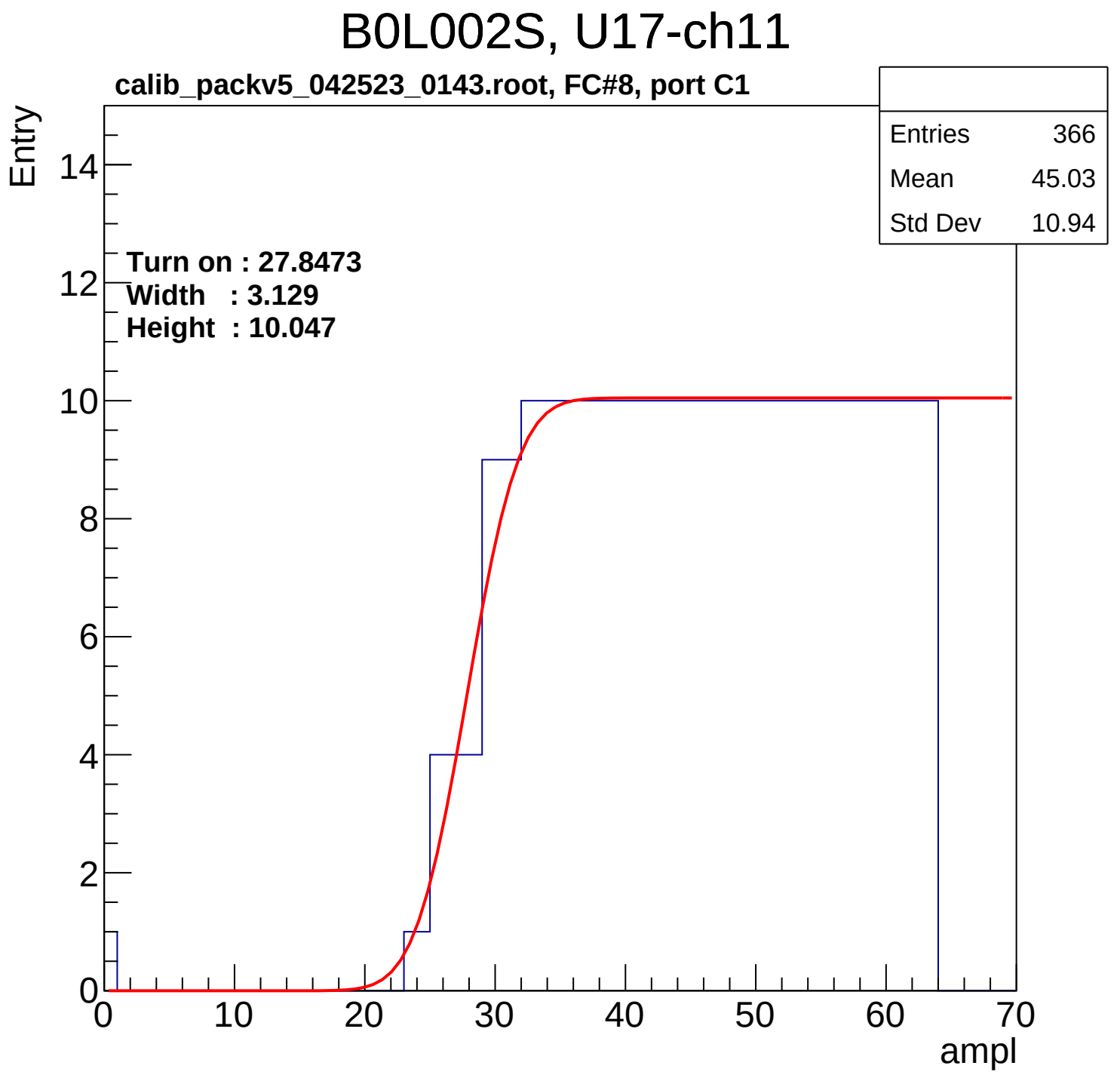
B0L002S, U17-ch11
calib_packv5_042523_0143.root, FC#8, port C1
Entries 366
Mean 45.03
Std Dev 10.94
Turn on : 27.8473
Width : 3.129
Height : 10.047
Entry
ampl
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6
8
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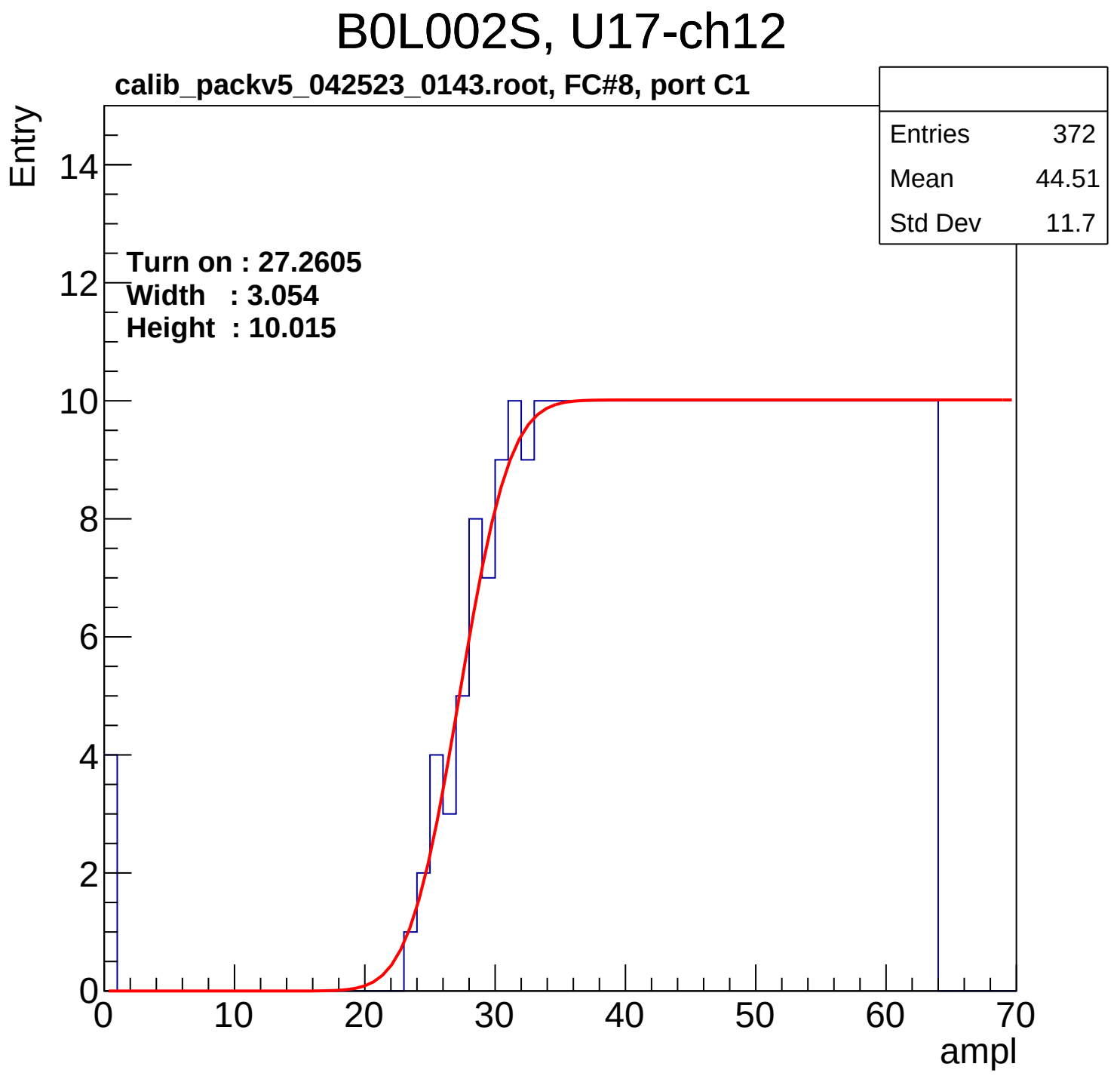
B0L002S, U17-ch12
calib_packv5_042523_0143.root, FC#8, port C1
Entries 372
Mean 44.51
Std Dev 11.7
Turn on : 27.2605
Width : 3.054
Height : 10.015
Entry
ampl
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6
8
10
12
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0
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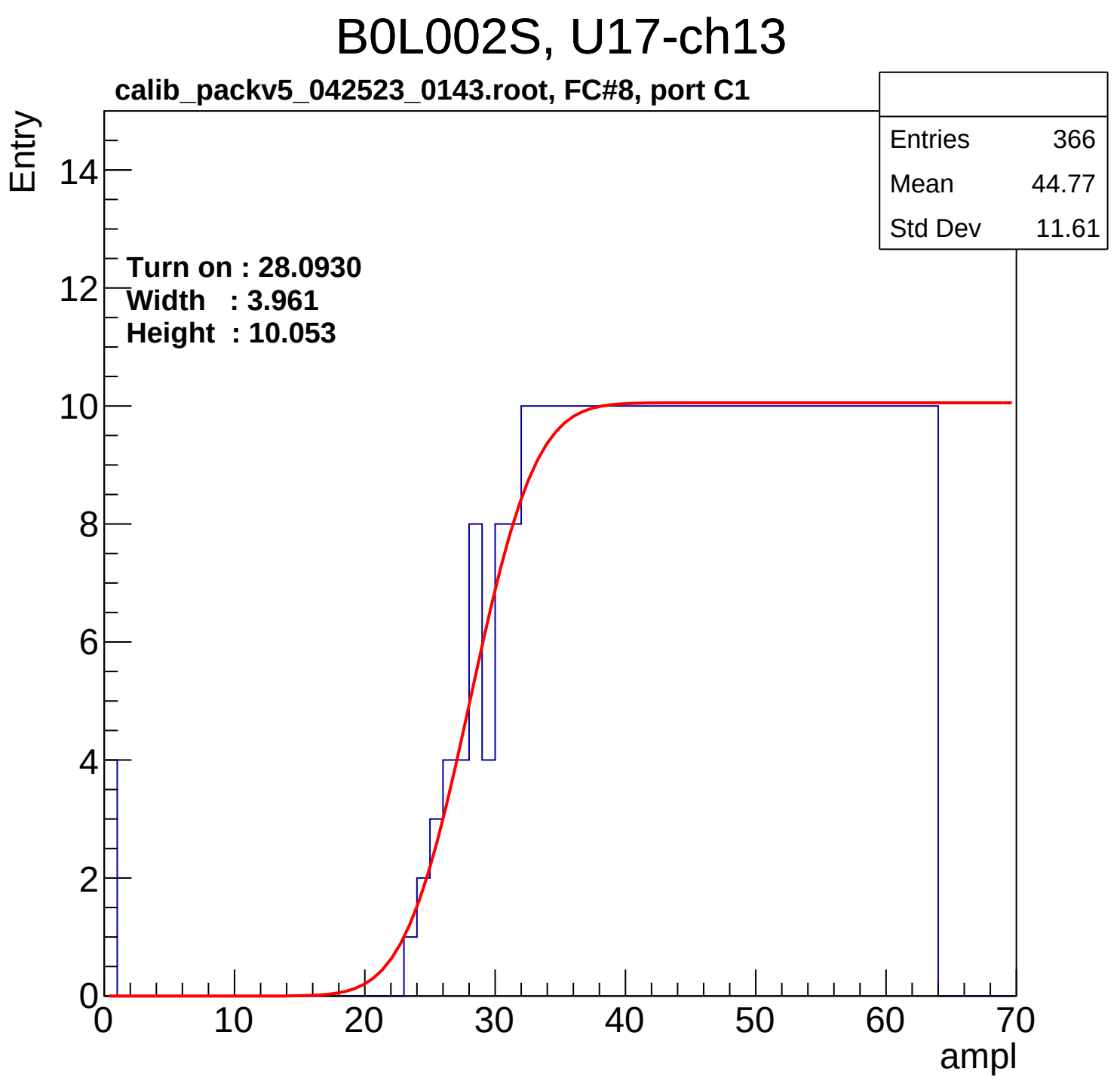
B0L002S, U17-ch13
calib_packv5_042523_0143.root, FC#8, port C1
Entries 366
Mean 44.77
Std Dev 11.61
Turn on : 28.0930
Width : 3.961
Height : 10.053
Entry
ampl
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6
8
10
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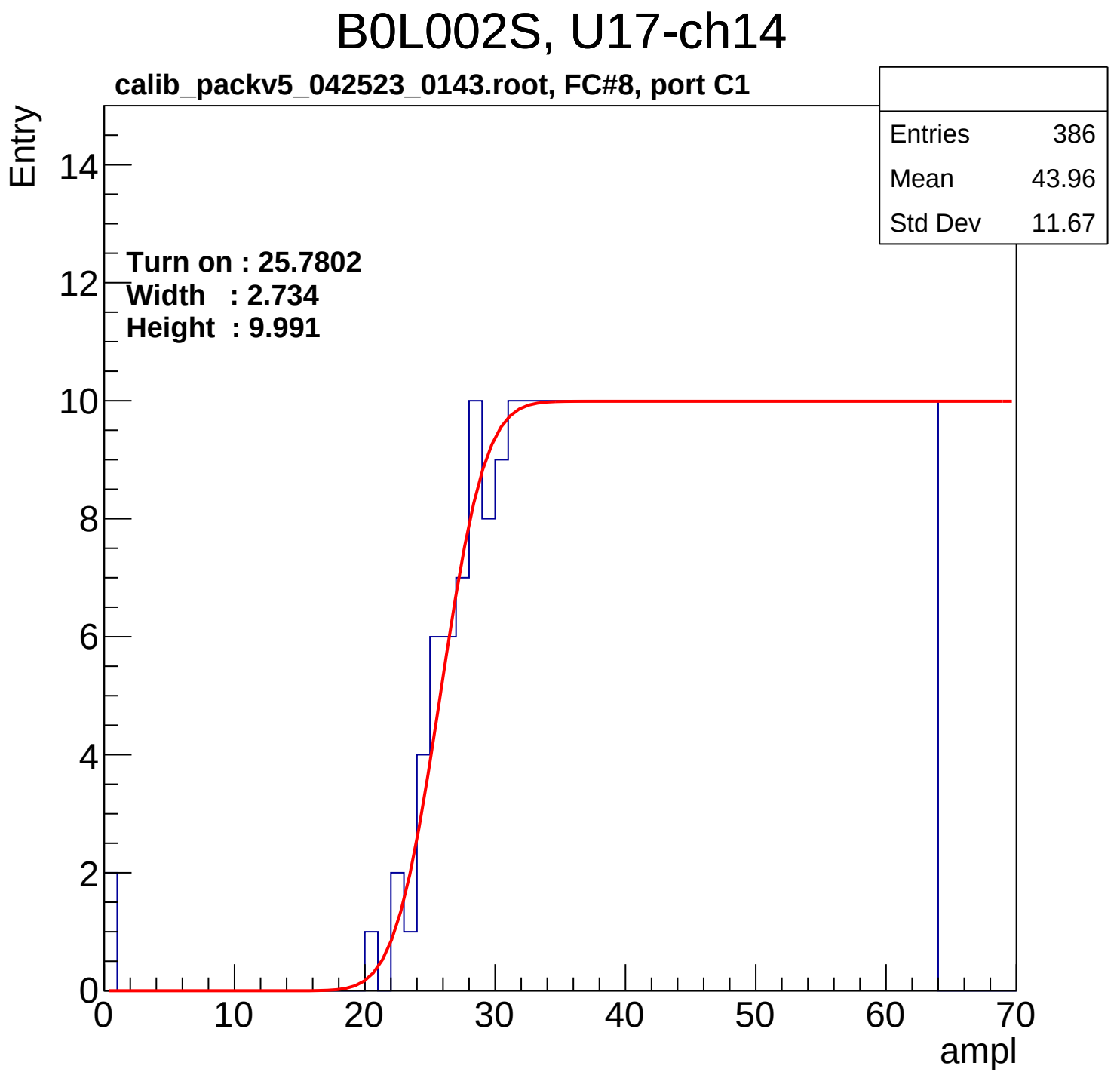
B0L002S, U17-ch14
calib_packv5_042523_0143.root, FC#8, port C1
Entries 386
Mean 43.96
Std Dev 11.67
Turn on : 25.7802
Width : 2.734
Height : 9.991
Entry
ampl
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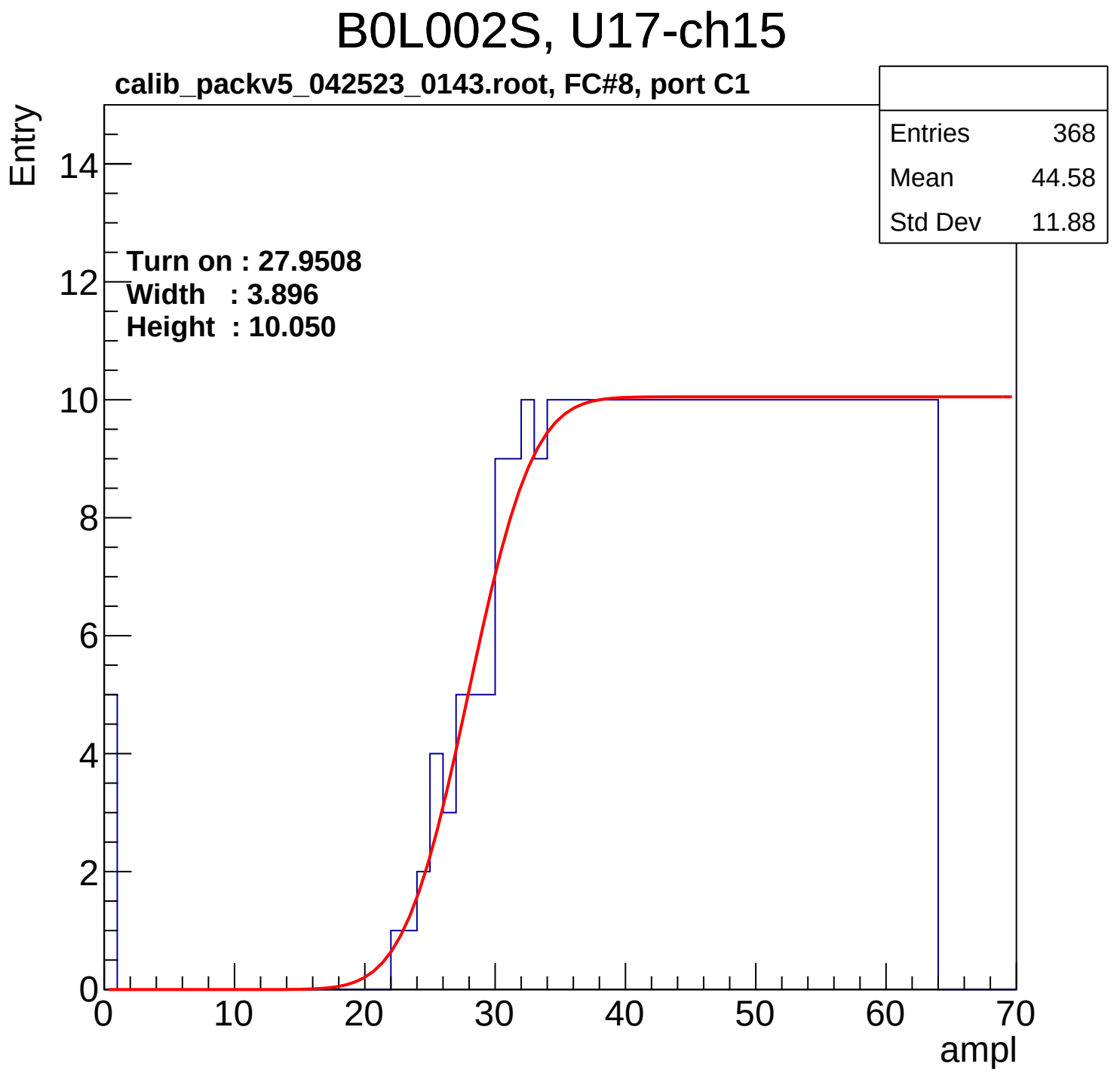
B0L002S, U17-ch15
calib_packv5_042523_0143.root, FC#8, port C1
Entries 368
Mean 44.58
Std Dev 11.88
Turn on : 27.9508
Width : 3.896
Height : 10.050
Entry
ampl
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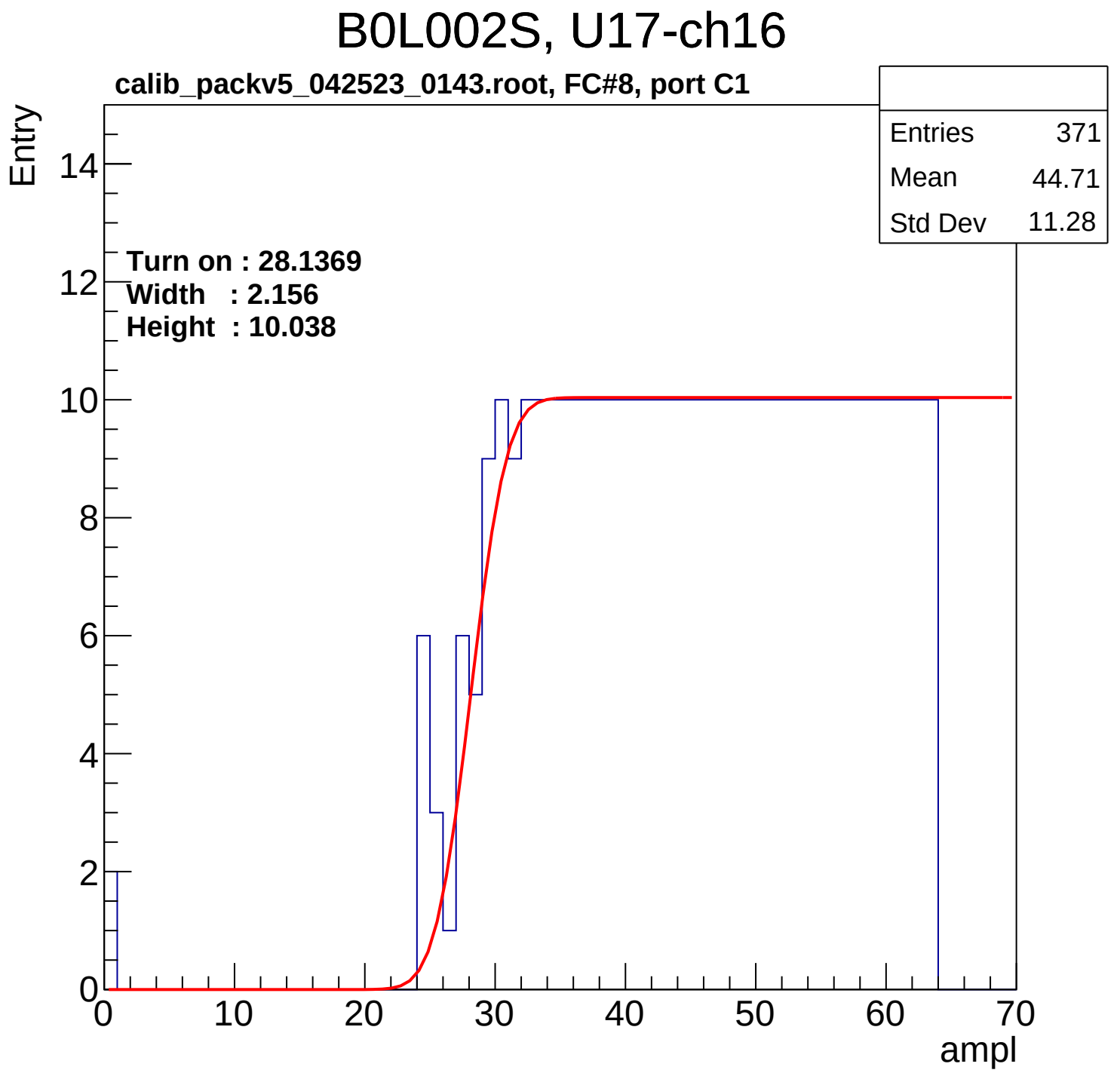
B0L002S, U17-ch16
calib_packv5_042523_0143.root, FC#8, port C1
Entries 371
Mean 44.71
Std Dev 11.28
Turn on : 28.1369
Width : 2.156
Height : 10.038
Entry
ampl
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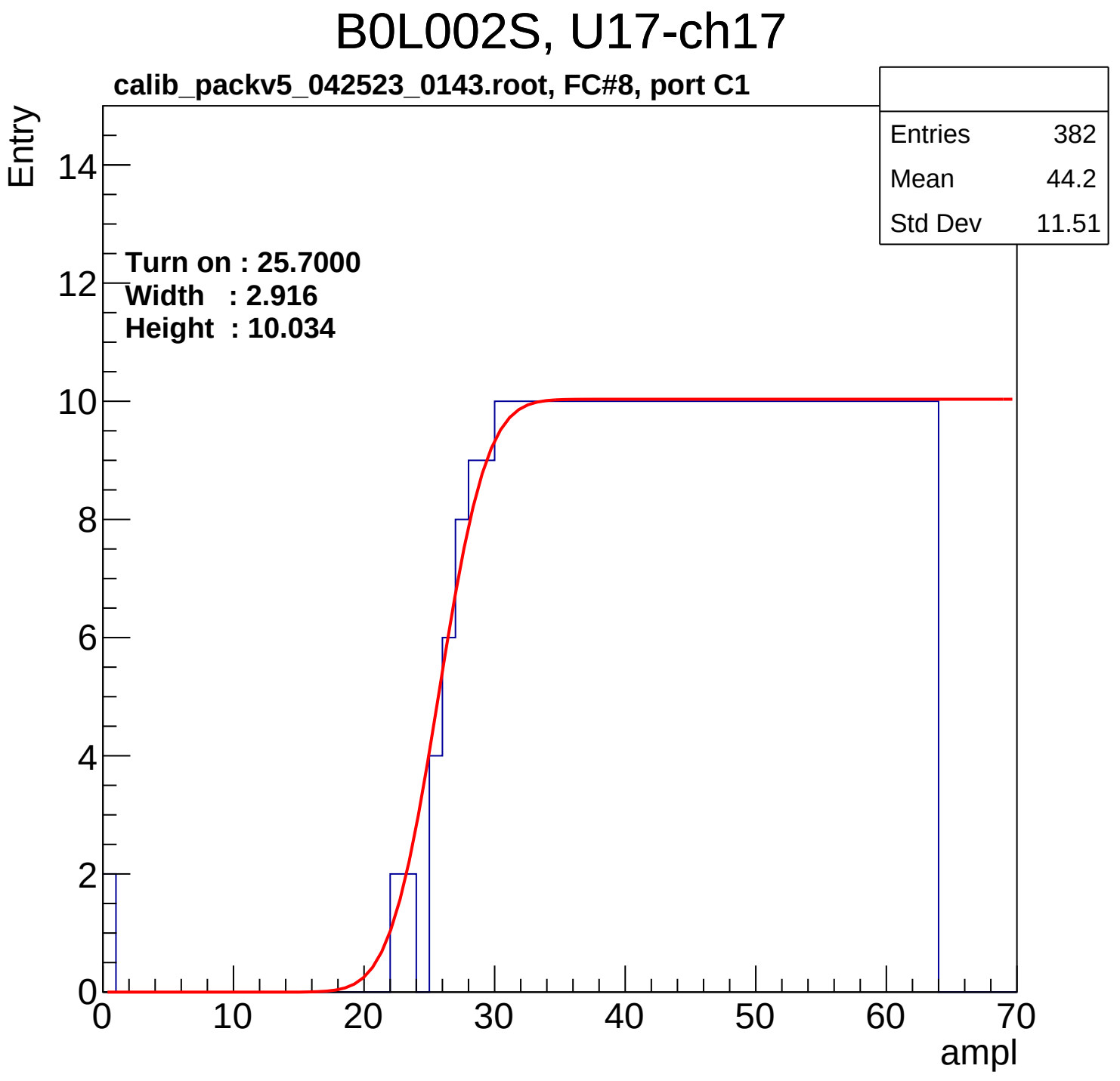
B0L002S, U17-ch17
calib_packv5_042523_0143.root, FC#8, port C1
Entries 382
Mean 44.2
Std Dev 11.51
Turn on : 25.7000
Width : 2.916
Height : 10.034
Entry
ampl
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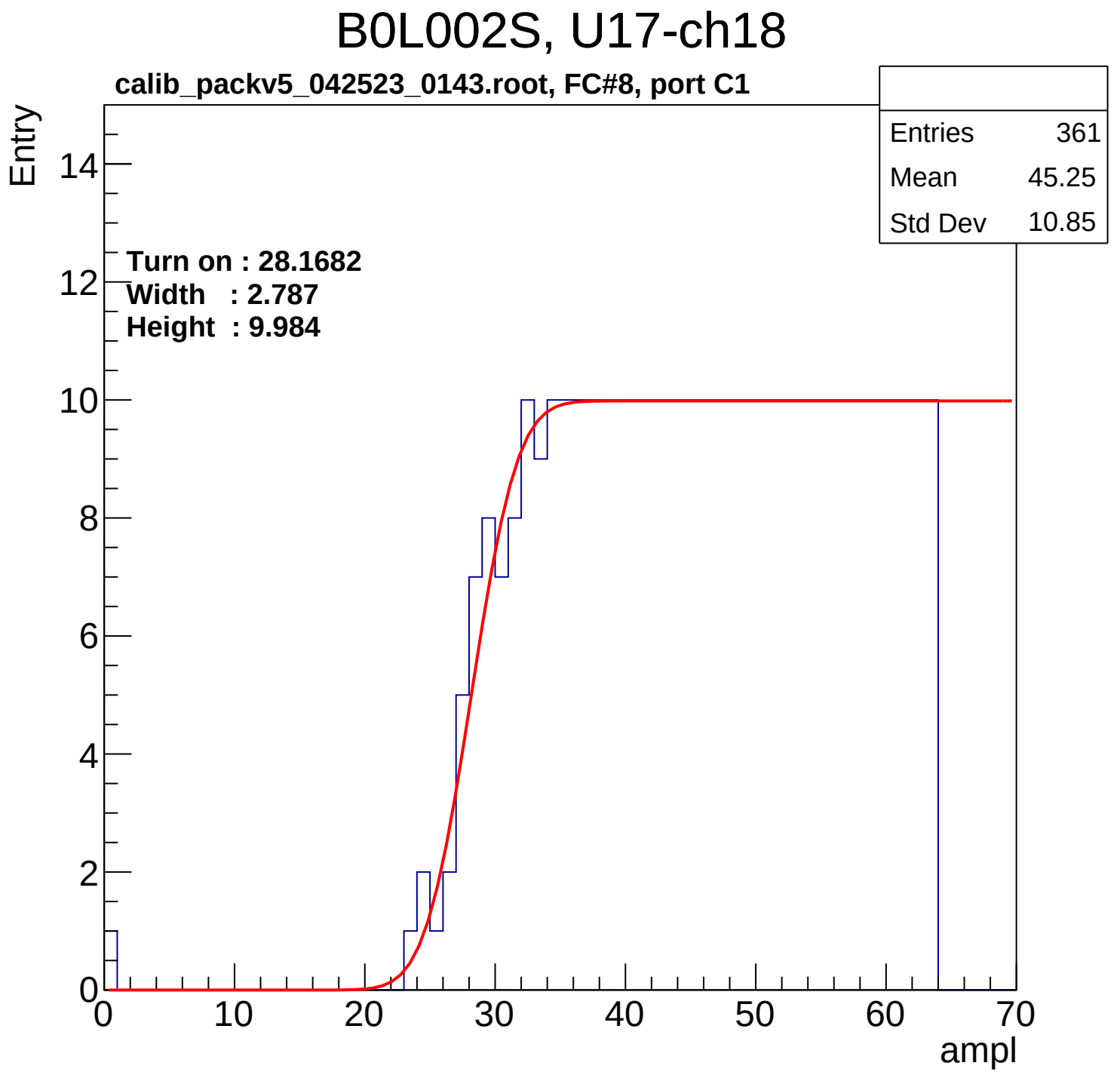
B0L002S, U17-ch18
calib_packv5_042523_0143.root, FC#8, port C1
Entries 361
Mean 45.25
Std Dev 10.85
Turn on : 28.1682
Width : 2.787
Height : 9.984
Entry
ampl
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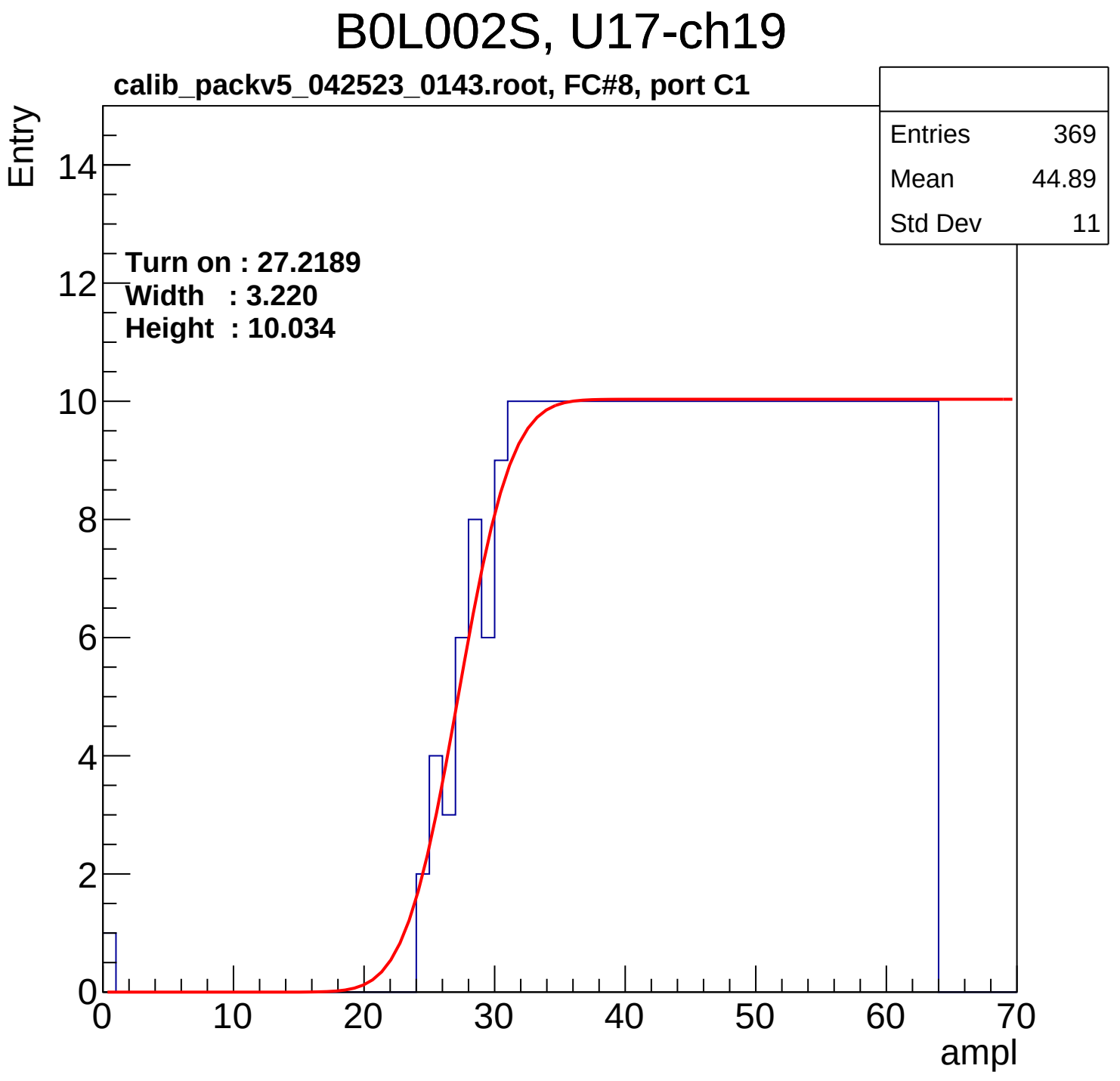
B0L002S, U17-ch19
calib_packv5_042523_0143.root, FC#8, port C1
Entries 369
Mean 44.89
Std Dev 11
Turn on : 27.2189
Width : 3.220
Height : 10.034
Entry
ampl
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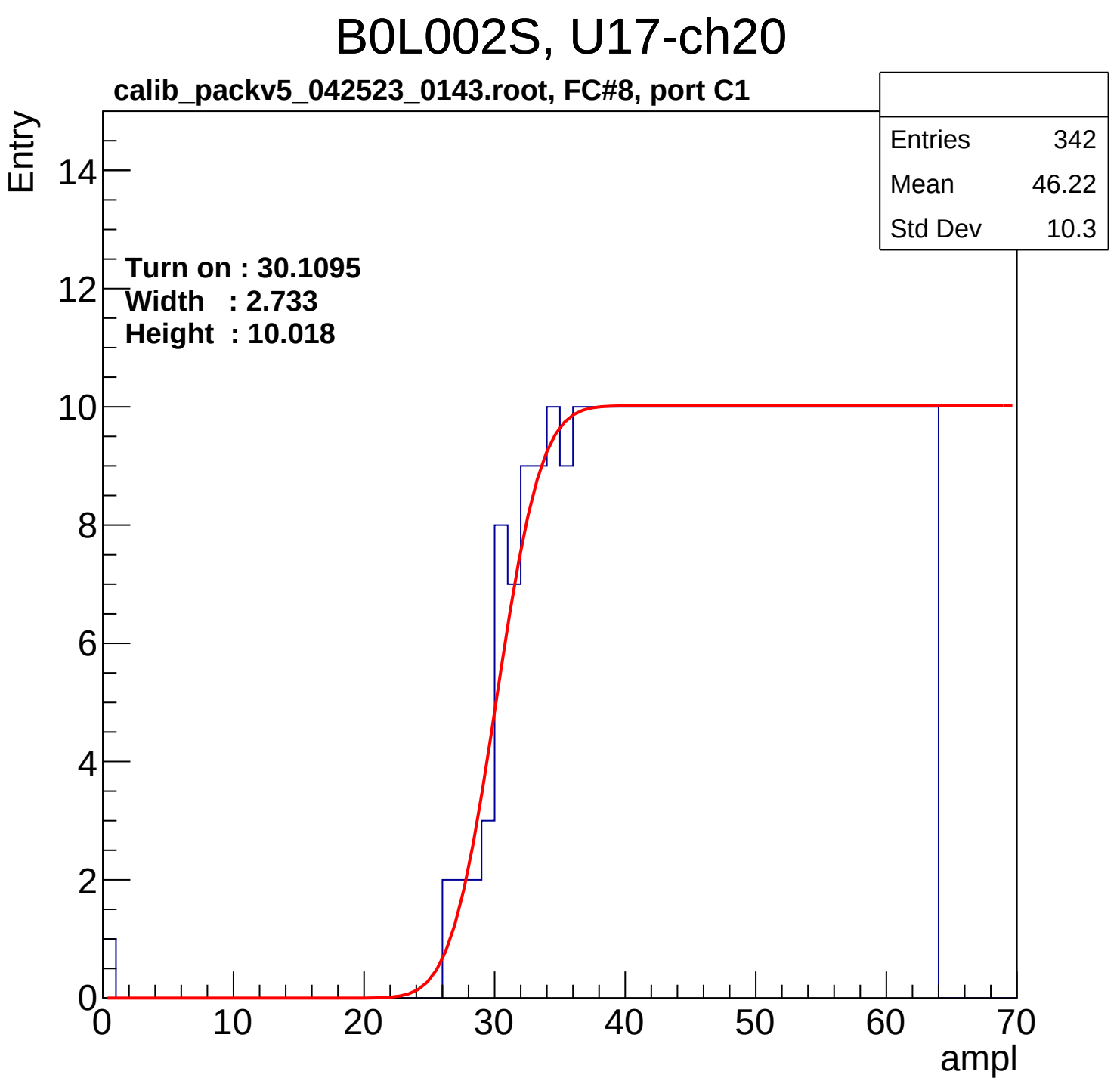
B0L002S, U17-ch20
calib_packv5_042523_0143.root, FC#8, port C1
Entries 342
Mean 46.22
Std Dev 10.3
Turn on : 30.1095
Width : 2.733
Height : 10.018
Entry
ampl
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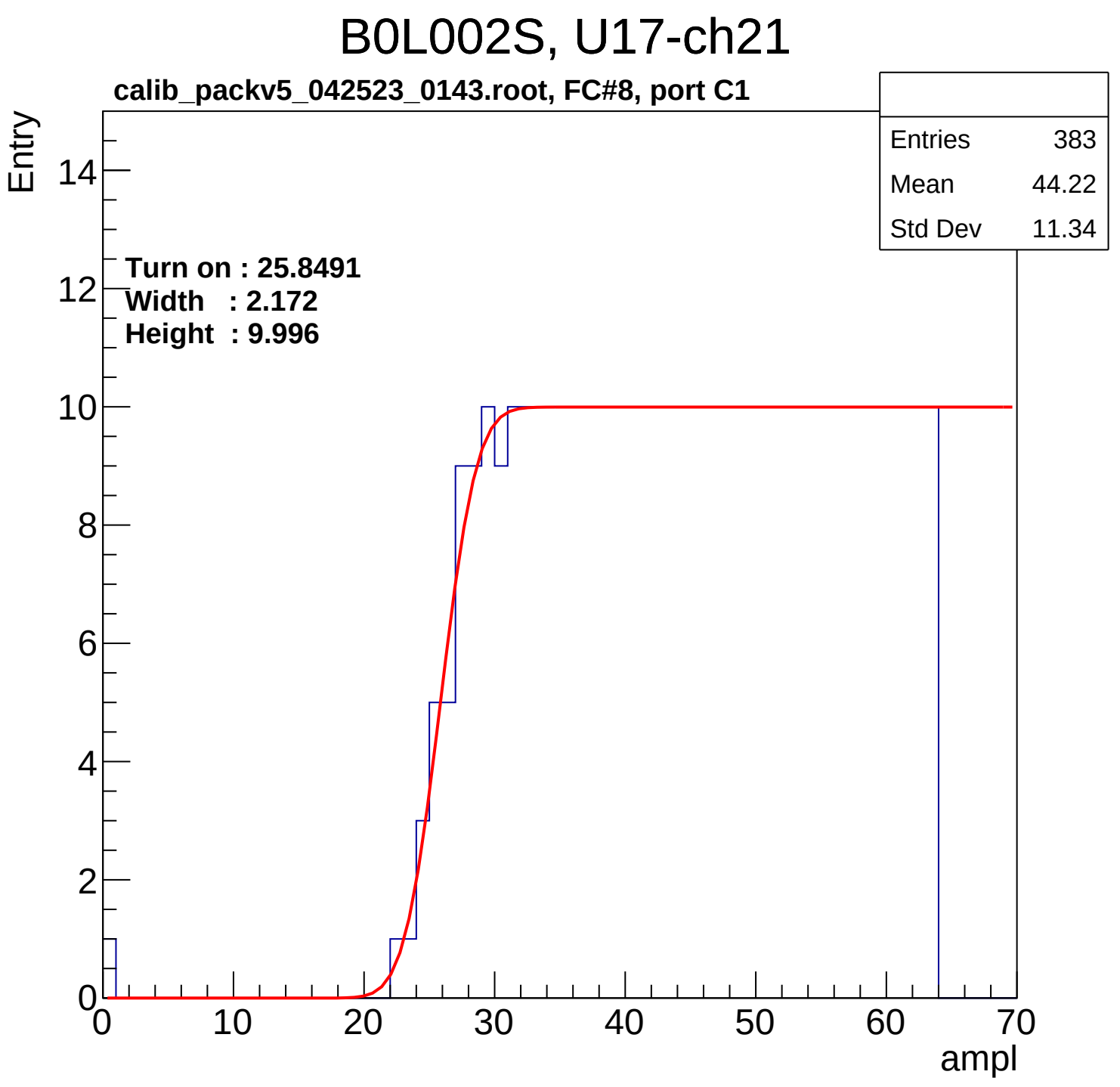
B0L002S, U17-ch21
calib_packv5_042523_0143.root, FC#8, port C1
Entries 383
Mean 44.22
Std Dev 11.34
Turn on : 25.8491
Width : 2.172
Height : 9.996
Entry
ampl
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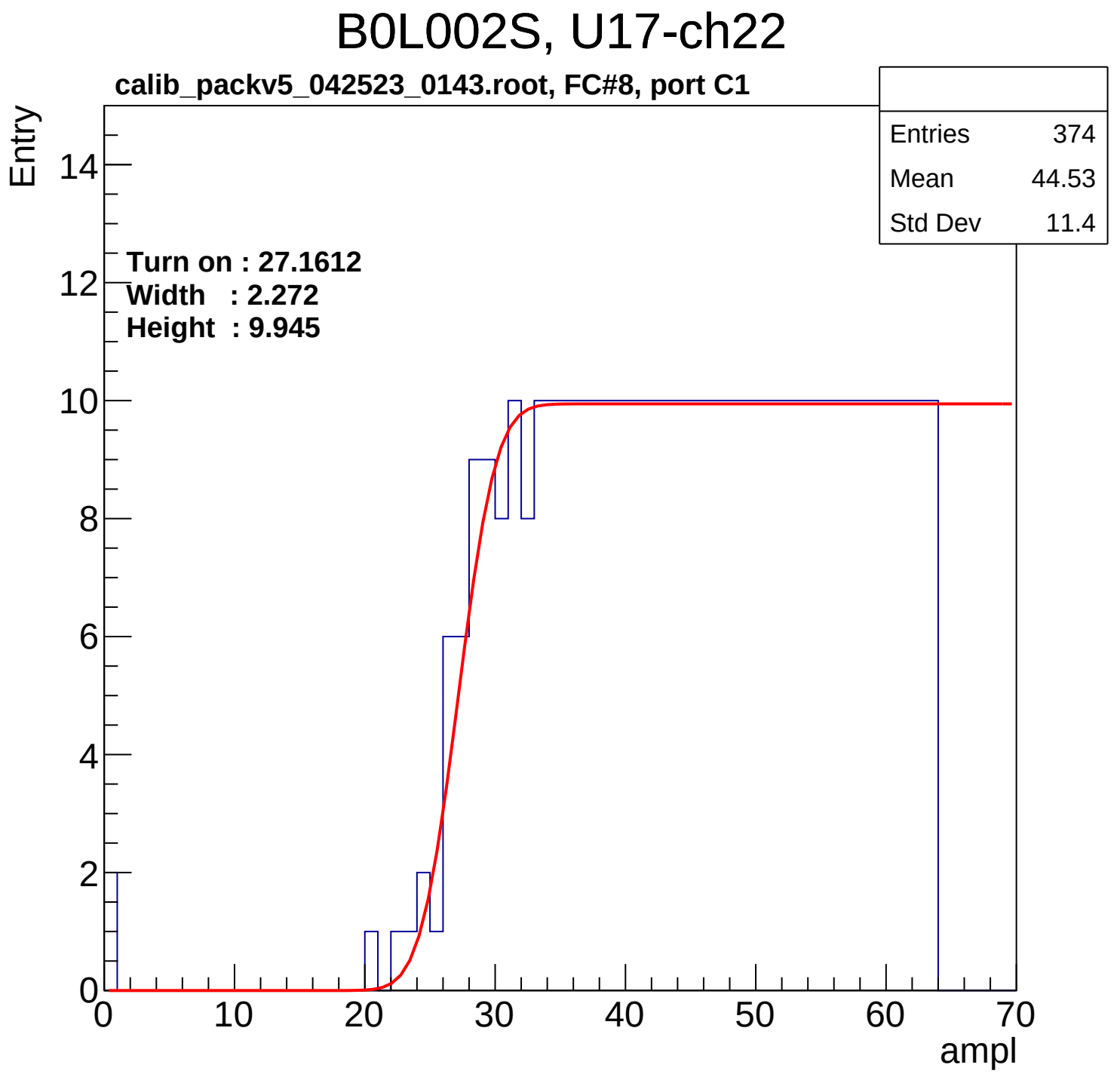
B0L002S, U17-ch22
calib_packv5_042523_0143.root, FC#8, port C1
Entries 374
Mean 44.53
Std Dev 11.4
Turn on : 27.1612
Width : 2.272
Height : 9.945
Entry
ampl
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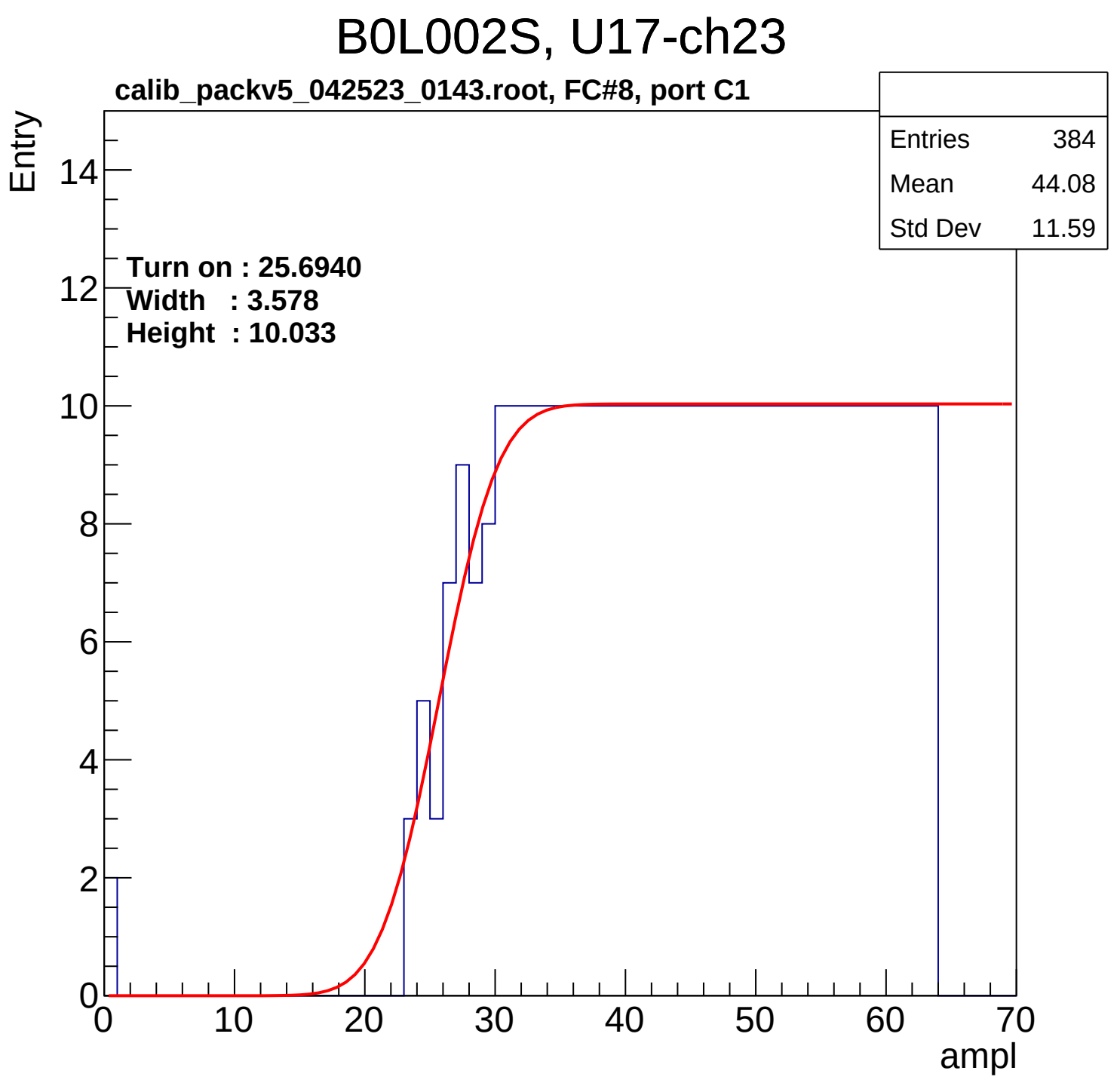
B0L002S, U17-ch23
calib_packv5_042523_0143.root, FC#8, port C1
Entries 384
Mean 44.08
Std Dev 11.59
Turn on : 25.6940
Width : 3.578
Height : 10.033
Entry
ampl
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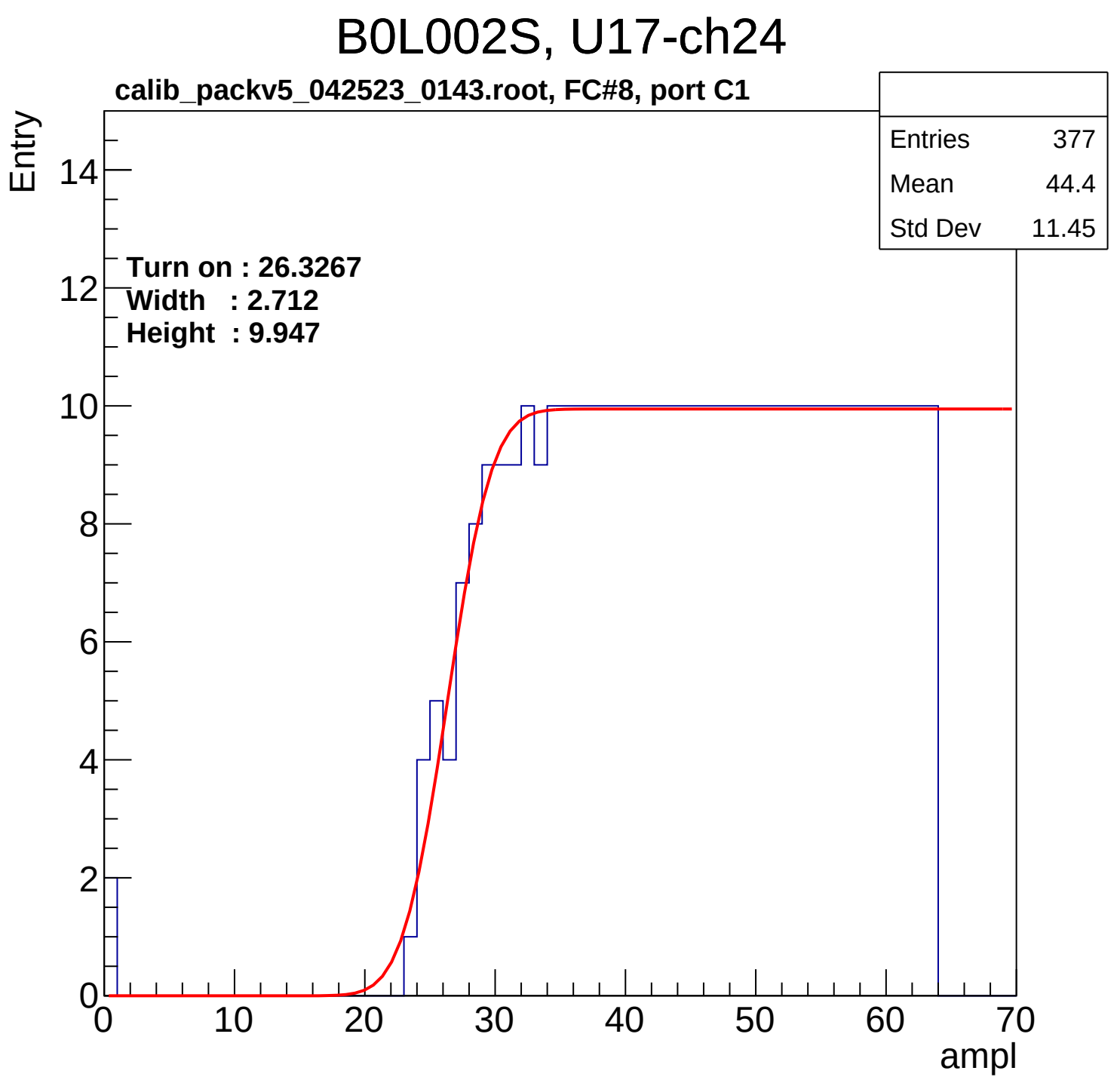
B0L002S, U17-ch24
calib_packv5_042523_0143.root, FC#8, port C1
Entries 377
Mean 44.4
Std Dev 11.45
Turn on : 26.3267
Width : 2.712
Height : 9.947
Entry
ampl
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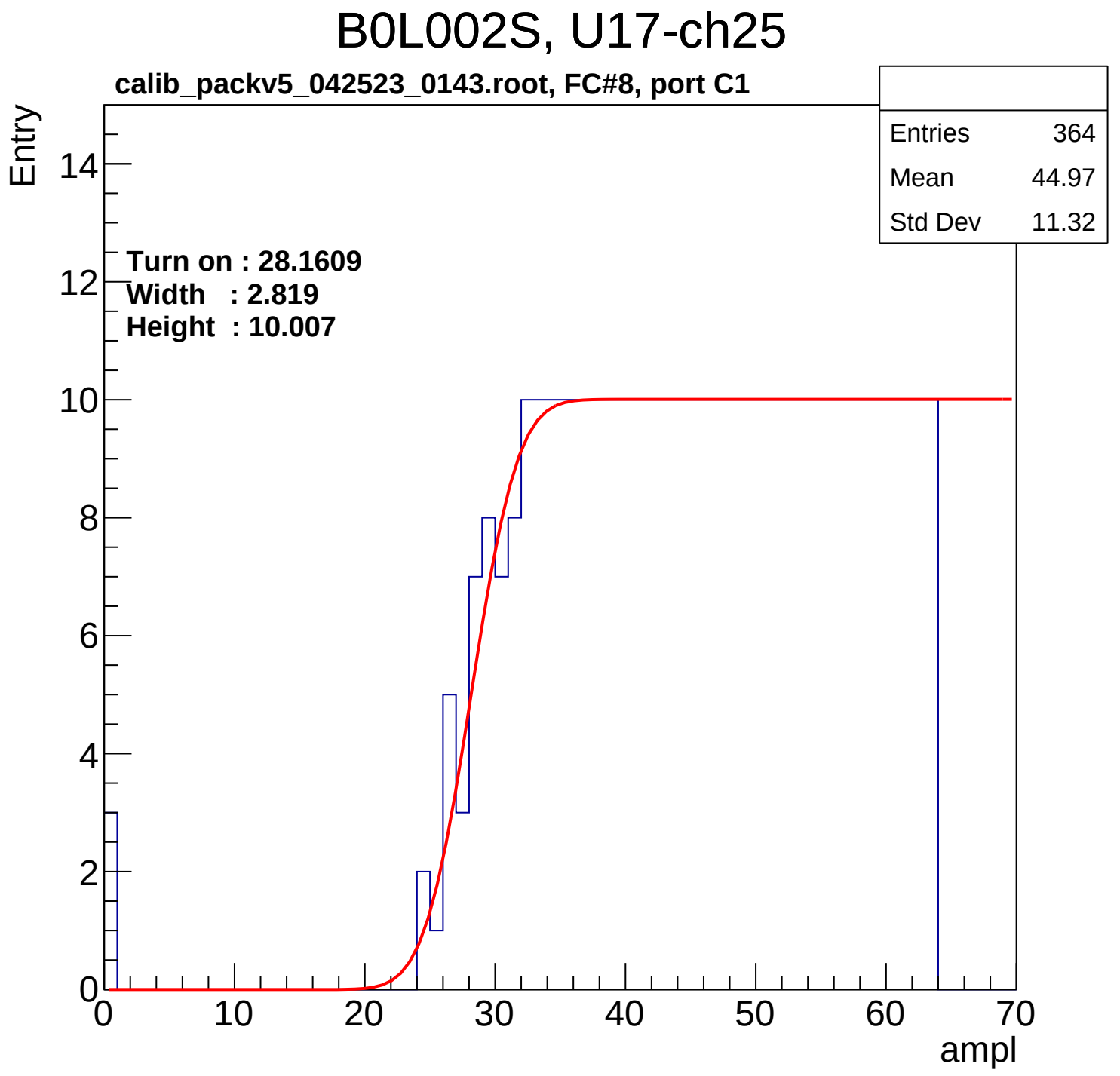
B0L002S, U17-ch25
calib_packv5_042523_0143.root, FC#8, port C1
Entries 364
Mean 44.97
Std Dev 11.32
Turn on : 28.1609
Width : 2.819
Height : 10.007
Entry
ampl
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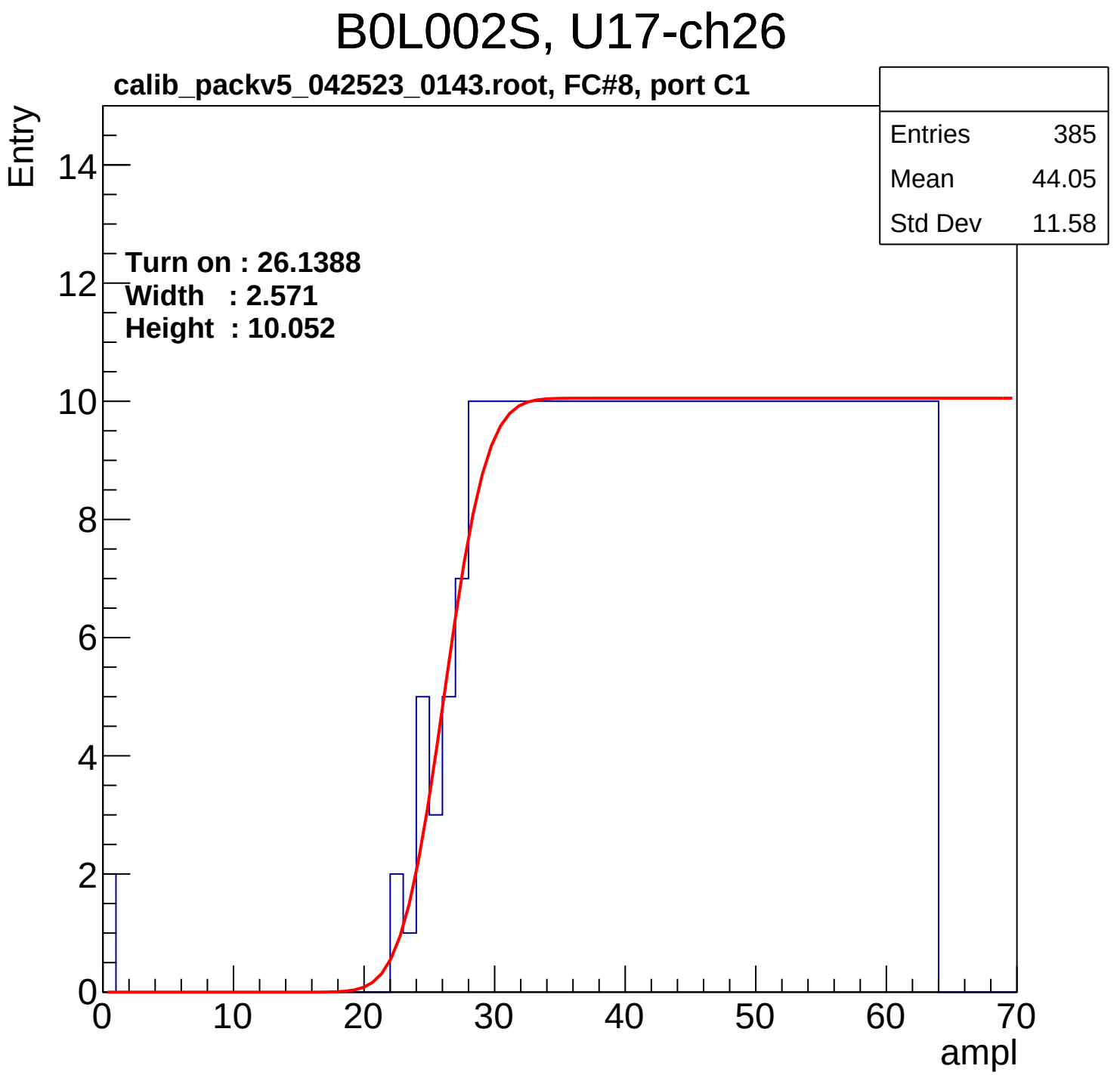
B0L002S, U17-ch26
calib_packv5_042523_0143.root, FC#8, port C1
Entries 385
Mean 44.05
Std Dev 11.58
Turn on : 26.1388
Width : 2.571
Height : 10.052
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ampl
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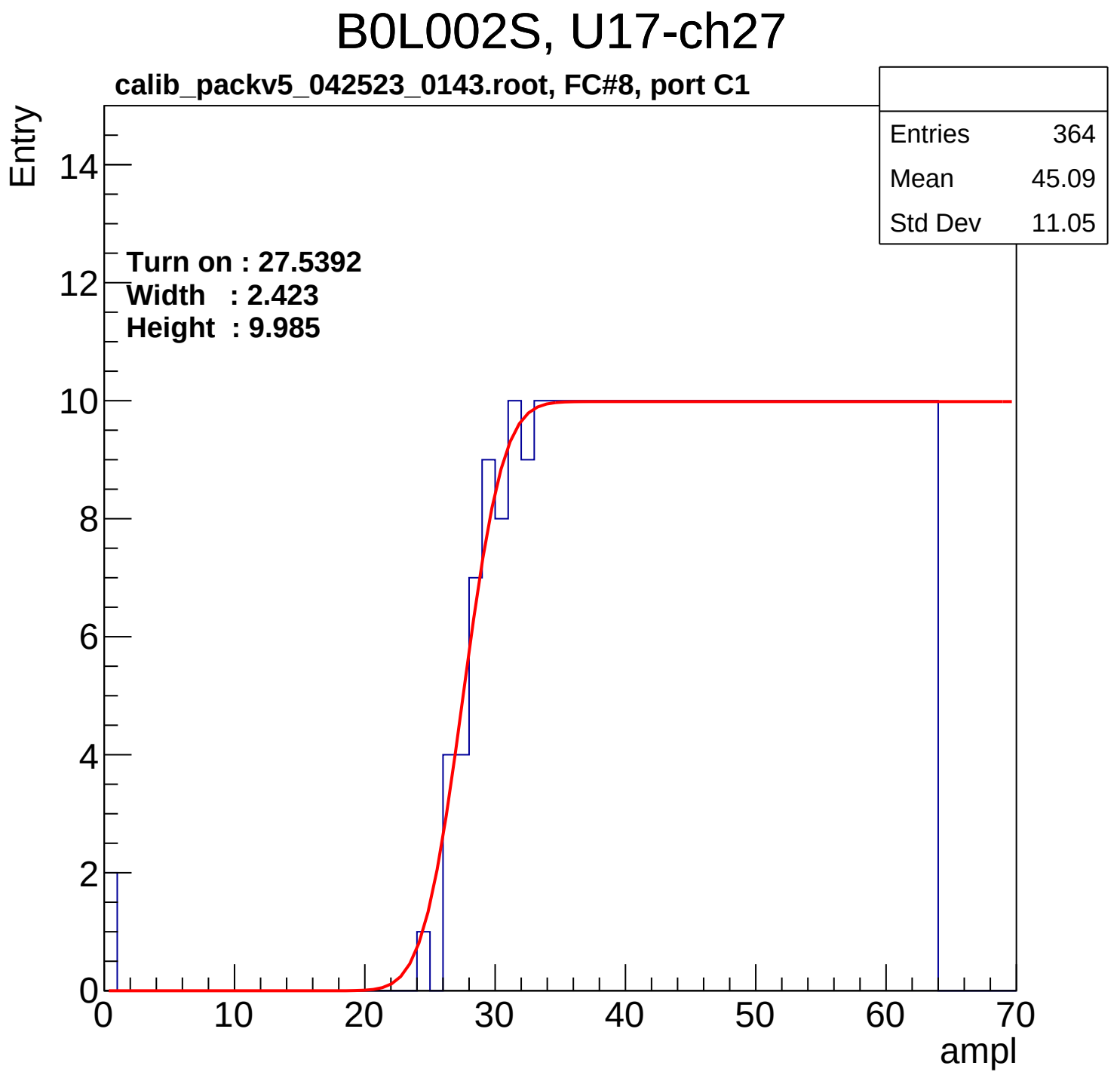
B0L002S, U17-ch27
calib_packv5_042523_0143.root, FC#8, port C1
Entries 364
Mean 45.09
Std Dev 11.05
Turn on : 27.5392
Width : 2.423
Height : 9.985
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ampl
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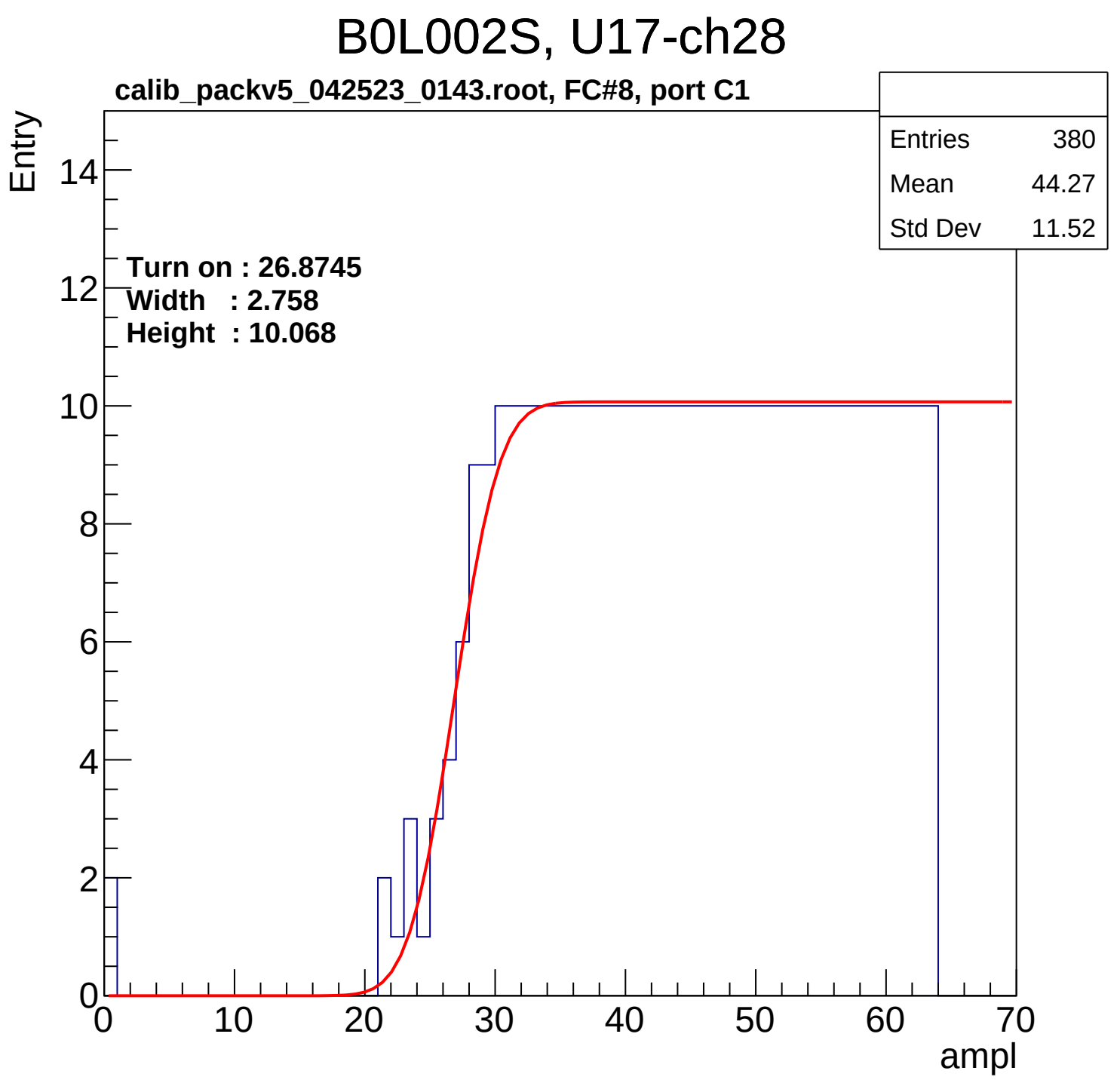
B0L002S, U17-ch28
calib_packv5_042523_0143.root, FC#8, port C1
Entries 380
Mean 44.27
Std Dev 11.52
Turn on : 26.8745
Width : 2.758
Height : 10.068
Entry
ampl
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4
6
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20
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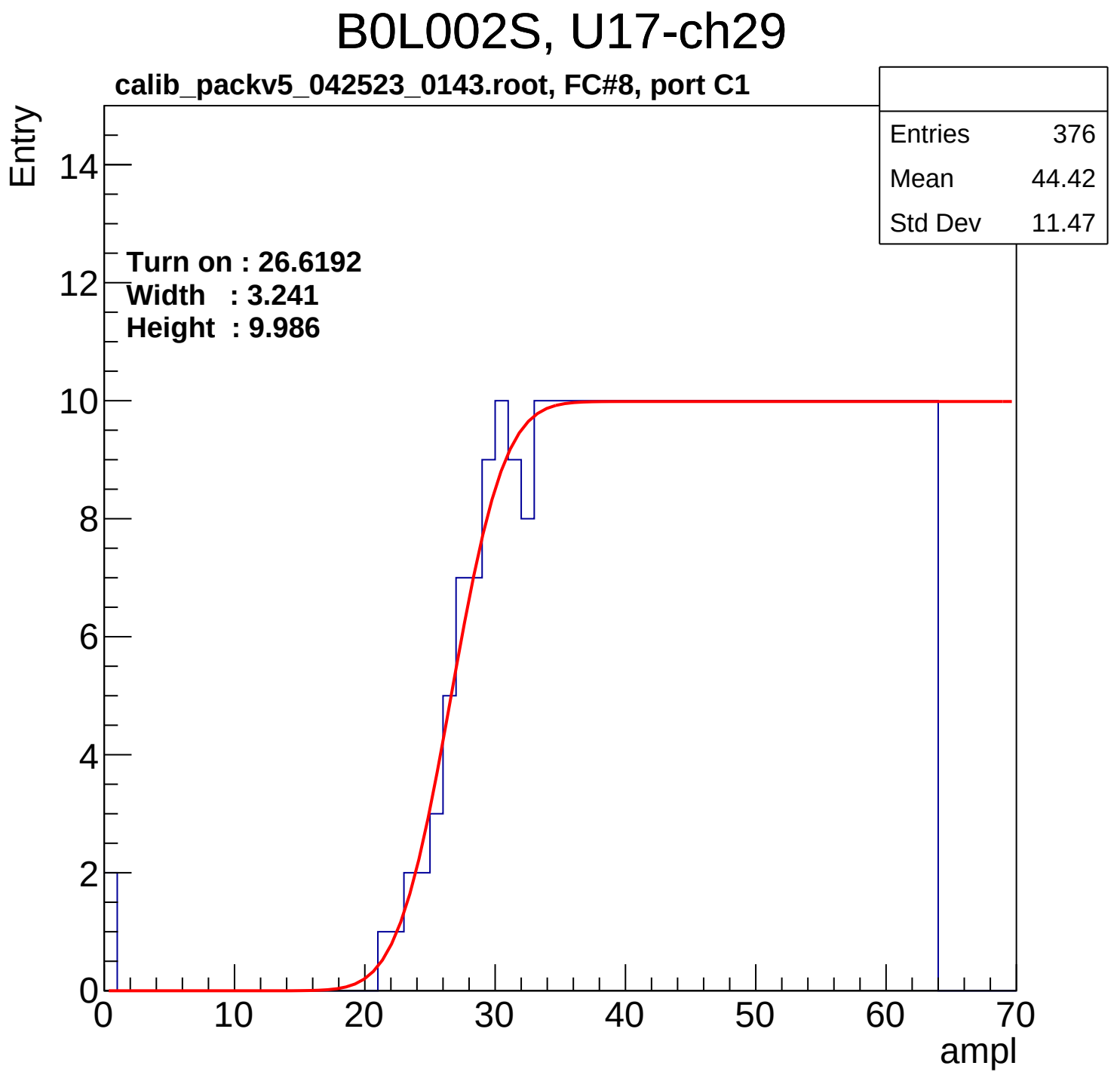
B0L002S, U17-ch29
calib_packv5_042523_0143.root, FC#8, port C1
Entries 376
Mean 44.42
Std Dev 11.47
Turn on : 26.6192
Width : 3.241
Height : 9.986
Entry
ampl
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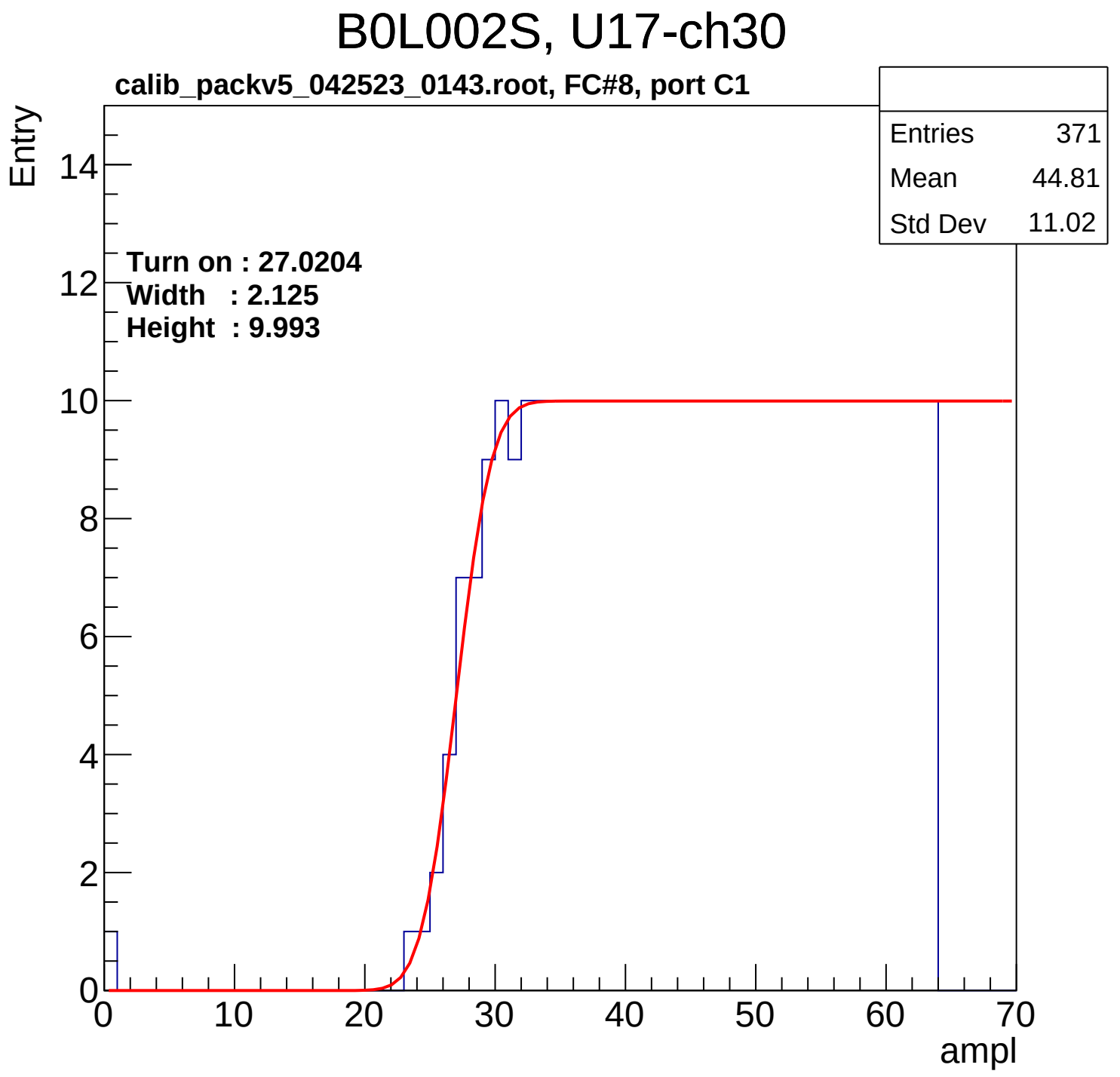
B0L002S, U17-ch30
calib_packv5_042523_0143.root, FC#8, port C1
Entries 371
Mean 44.81
Std Dev 11.02
Turn on : 27.0204
Width : 2.125
Height : 9.993
Entry
ampl
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2
4
6
8
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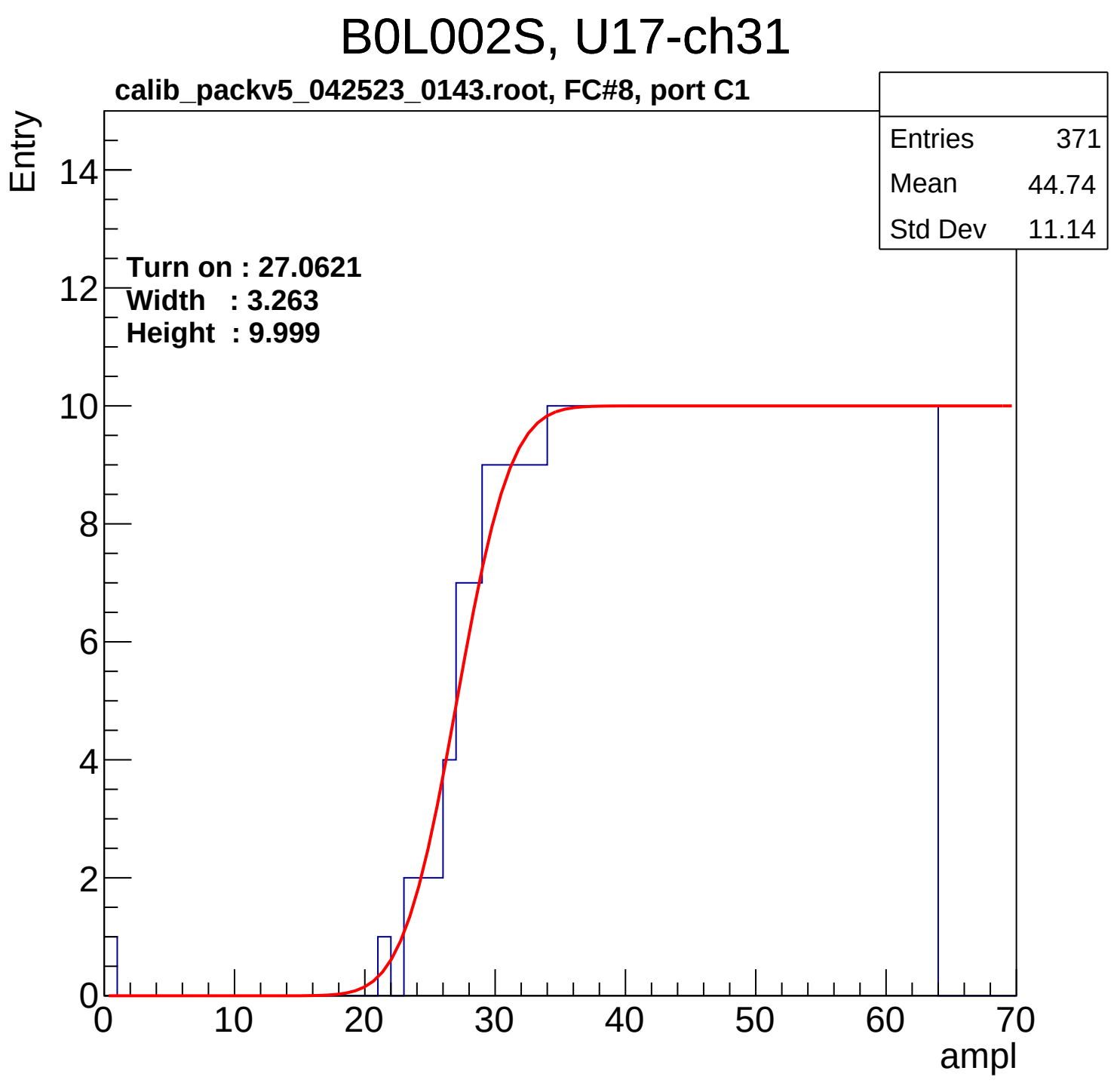
B0L002S, U17-ch31
calib_packv5_042523_0143.root, FC#8, port C1
Entries 371
Mean 44.74
Std Dev 11.14
Turn on : 27.0621
Width : 3.263
Height : 9.999
Entry
ampl
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2
4
6
8
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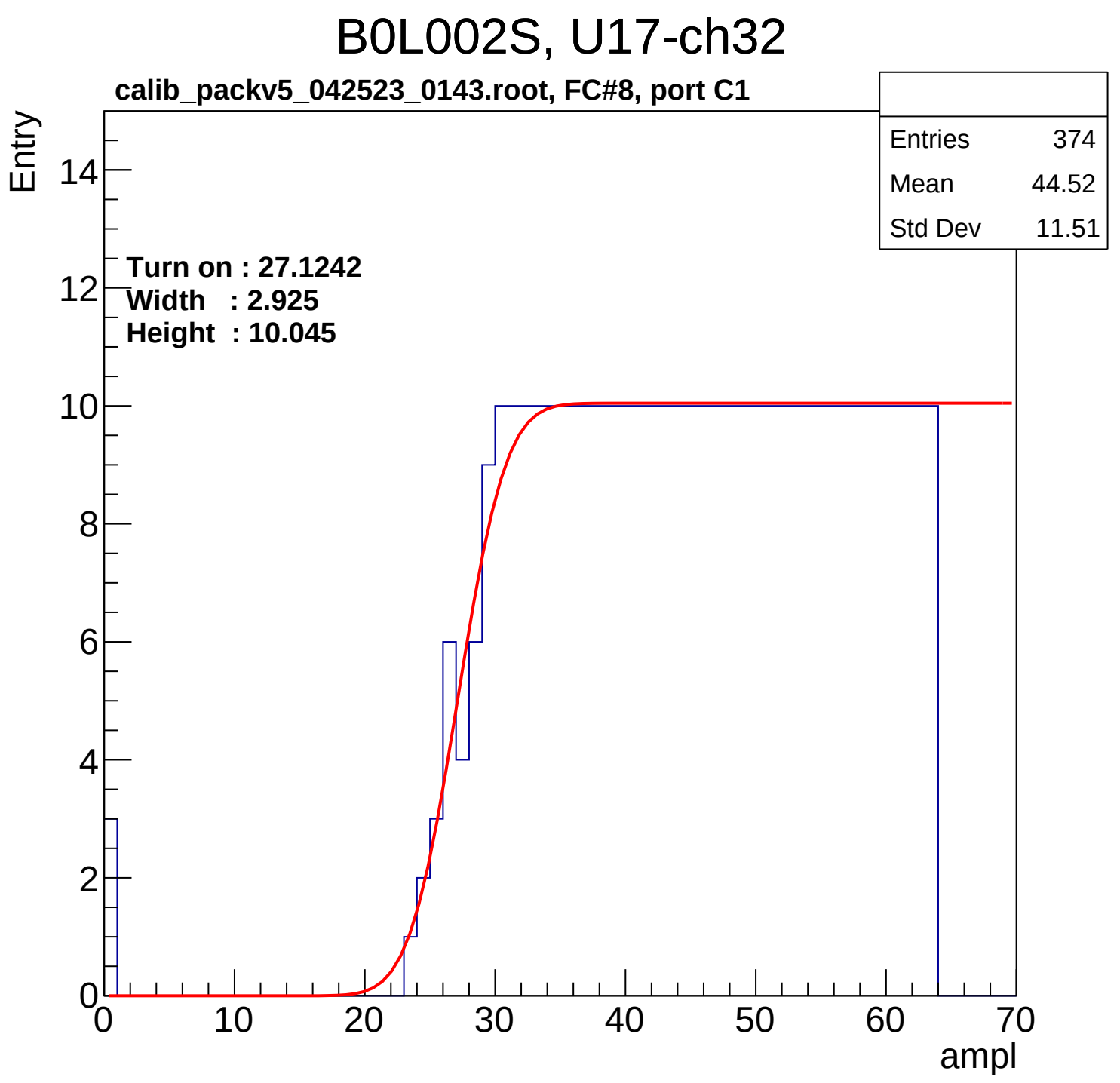
B0L002S, U17-ch32
calib_packv5_042523_0143.root, FC#8, port C1
Entries 374
Mean 44.52
Std Dev 11.51
Turn on : 27.1242
Width : 2.925
Height : 10.045
Entry
ampl
0
2
4
6
8
10
12
14
0
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60
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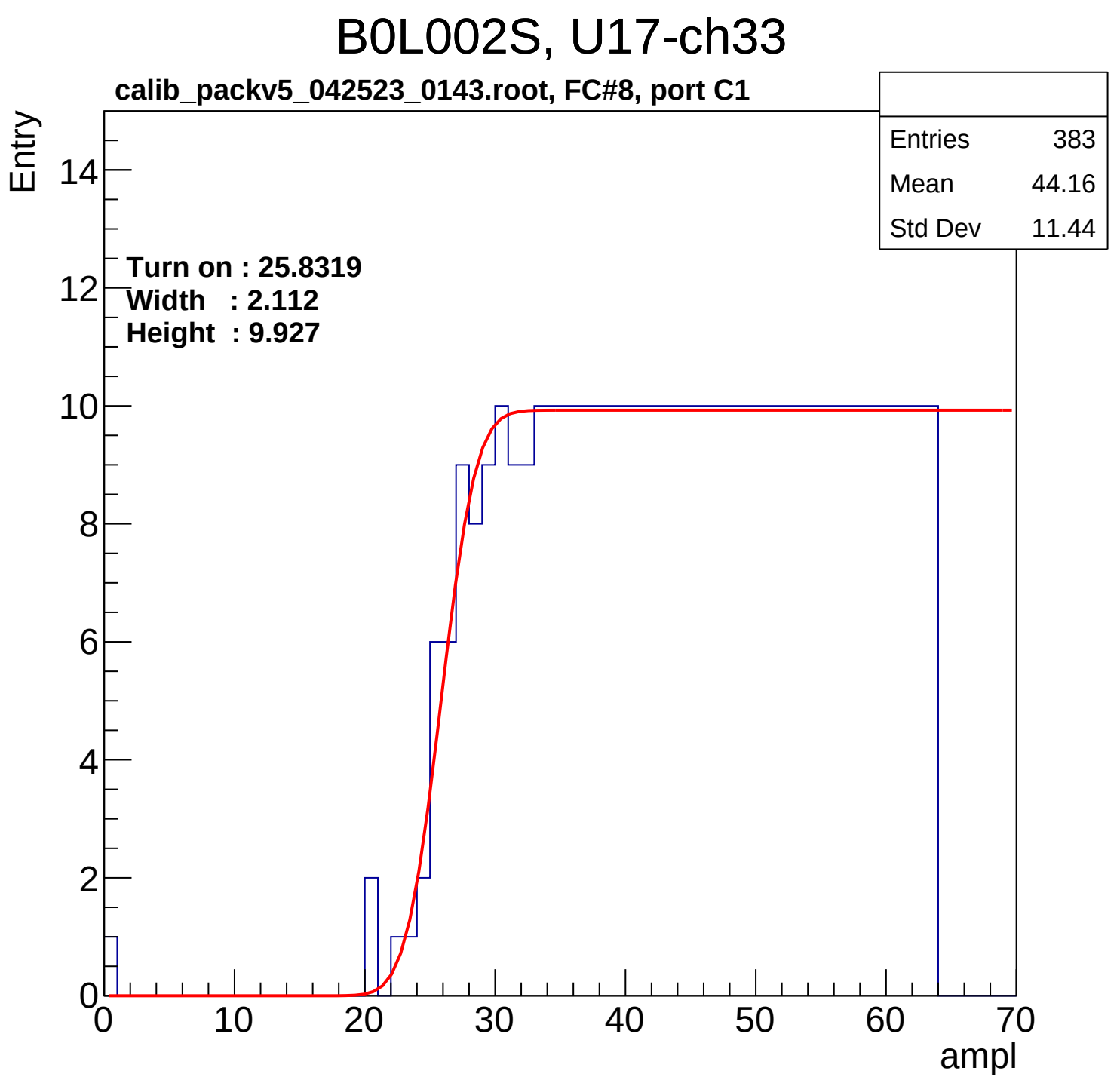
B0L002S, U17-ch33
calib_packv5_042523_0143.root, FC#8, port C1
Entries 383
Mean 44.16
Std Dev 11.44
Turn on : 25.8319
Width : 2.112
Height : 9.927
Entry
ampl
0
2
4
6
8
10
12
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0
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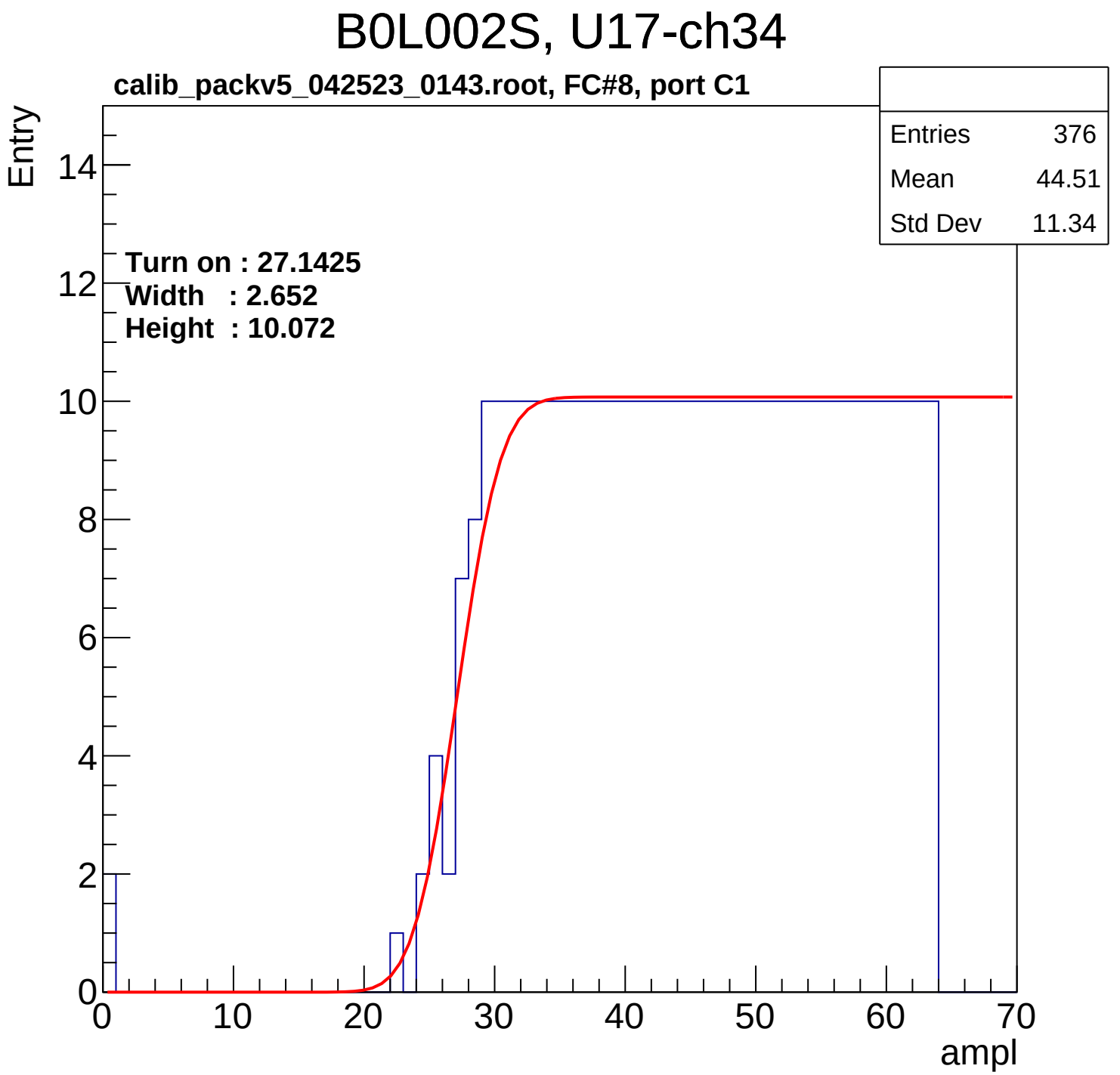
B0L002S, U17-ch34
calib_packv5_042523_0143.root, FC#8, port C1
Entries 376
Mean 44.51
Std Dev 11.34
Turn on : 27.1425
Width : 2.652
Height : 10.072
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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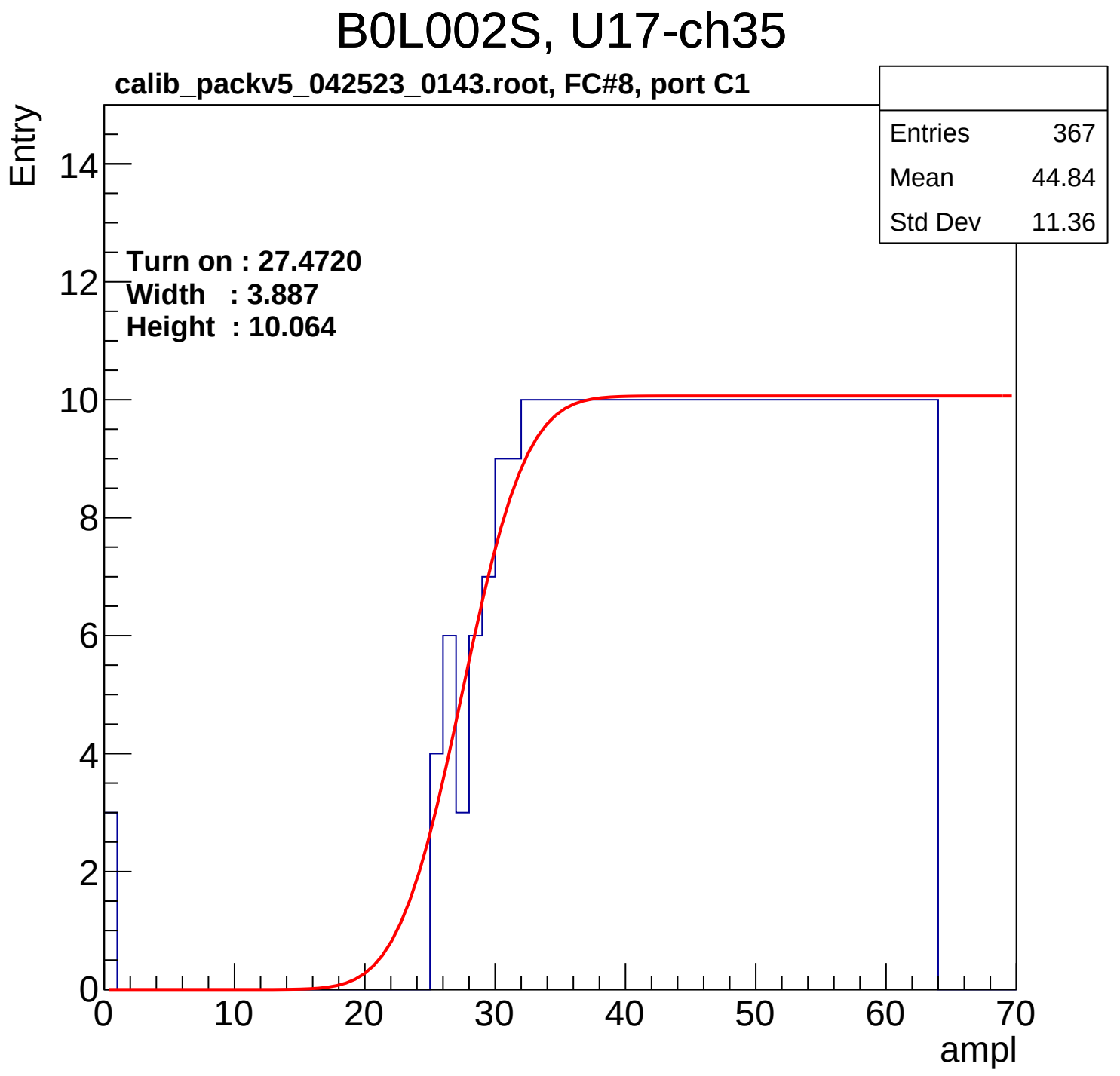
B0L002S, U17-ch35
calib_packv5_042523_0143.root, FC#8, port C1
Entries 367
Mean 44.84
Std Dev 11.36
Turn on : 27.4720
Width : 3.887
Height : 10.064
Entry
ampl
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2
4
6
8
10
12
14
0
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20
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40
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60
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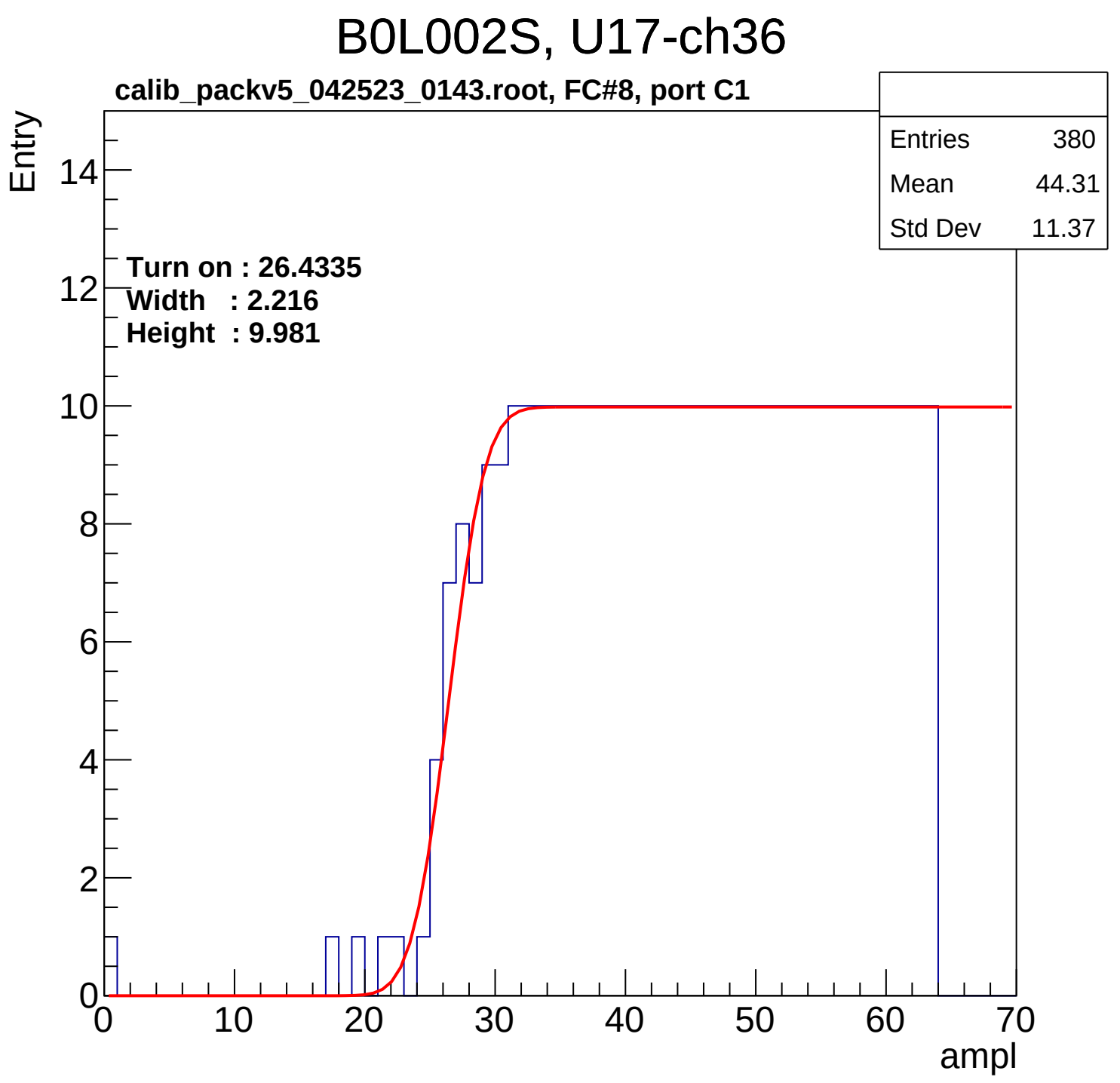
B0L002S, U17-ch36
calib_packv5_042523_0143.root, FC#8, port C1
Entries 380
Mean 44.31
Std Dev 11.37
Turn on : 26.4335
Width : 2.216
Height : 9.981
Entry
ampl
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2
4
6
8
10
12
14
0
10
20
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40
50
60
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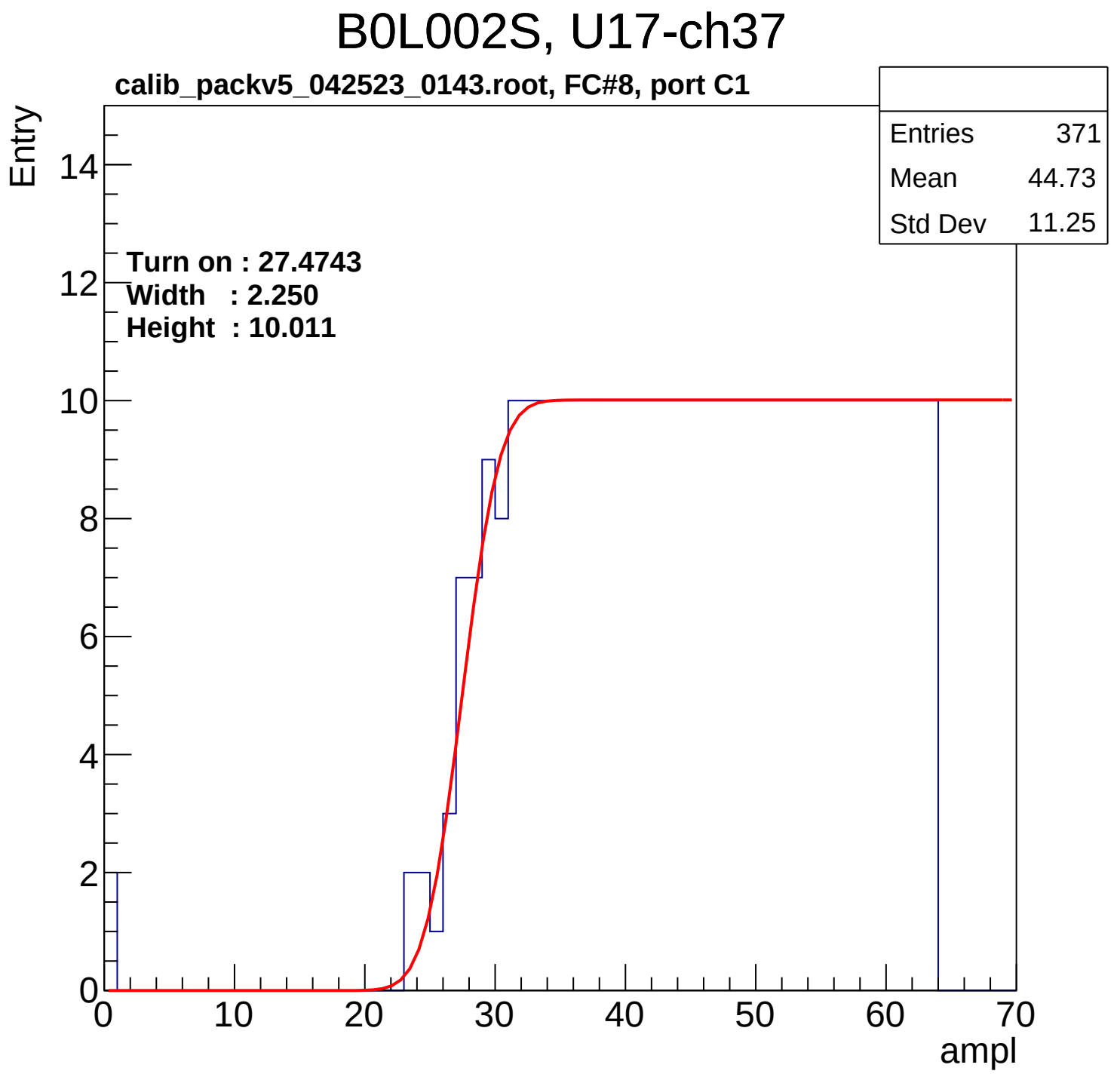
B0L002S, U17-ch37
calib_packv5_042523_0143.root, FC#8, port C1
Entries 371
Mean 44.73
Std Dev 11.25
Turn on : 27.4743
Width : 2.250
Height : 10.011
Entry
ampl
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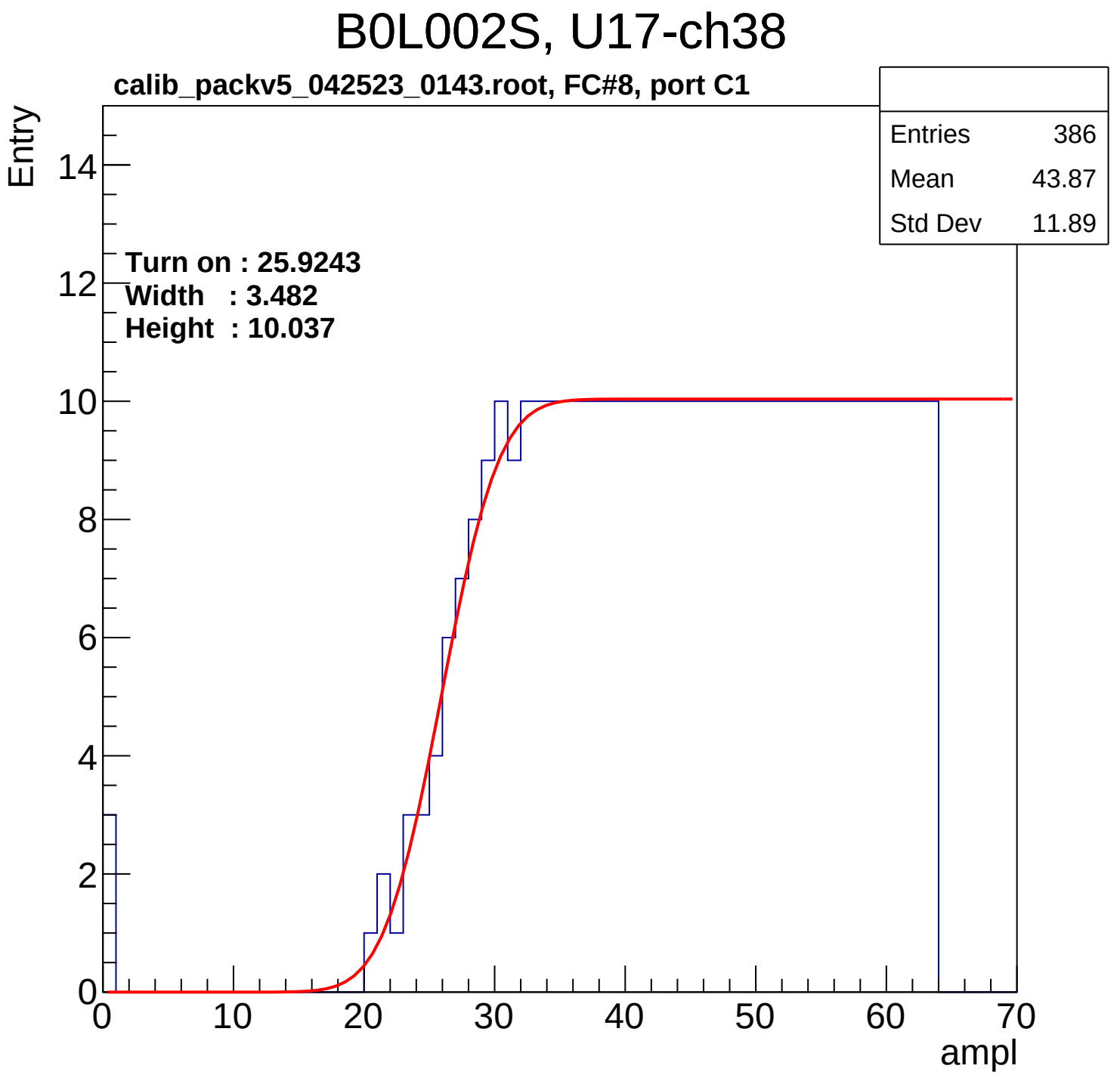
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L002S, U17-ch38
calib_packv5_042523_0143.root, FC#8, port C1
Entries 386
Mean 43.87
Std Dev 11.89
Turn on : 25.9243
Width : 3.482
Height : 10.037
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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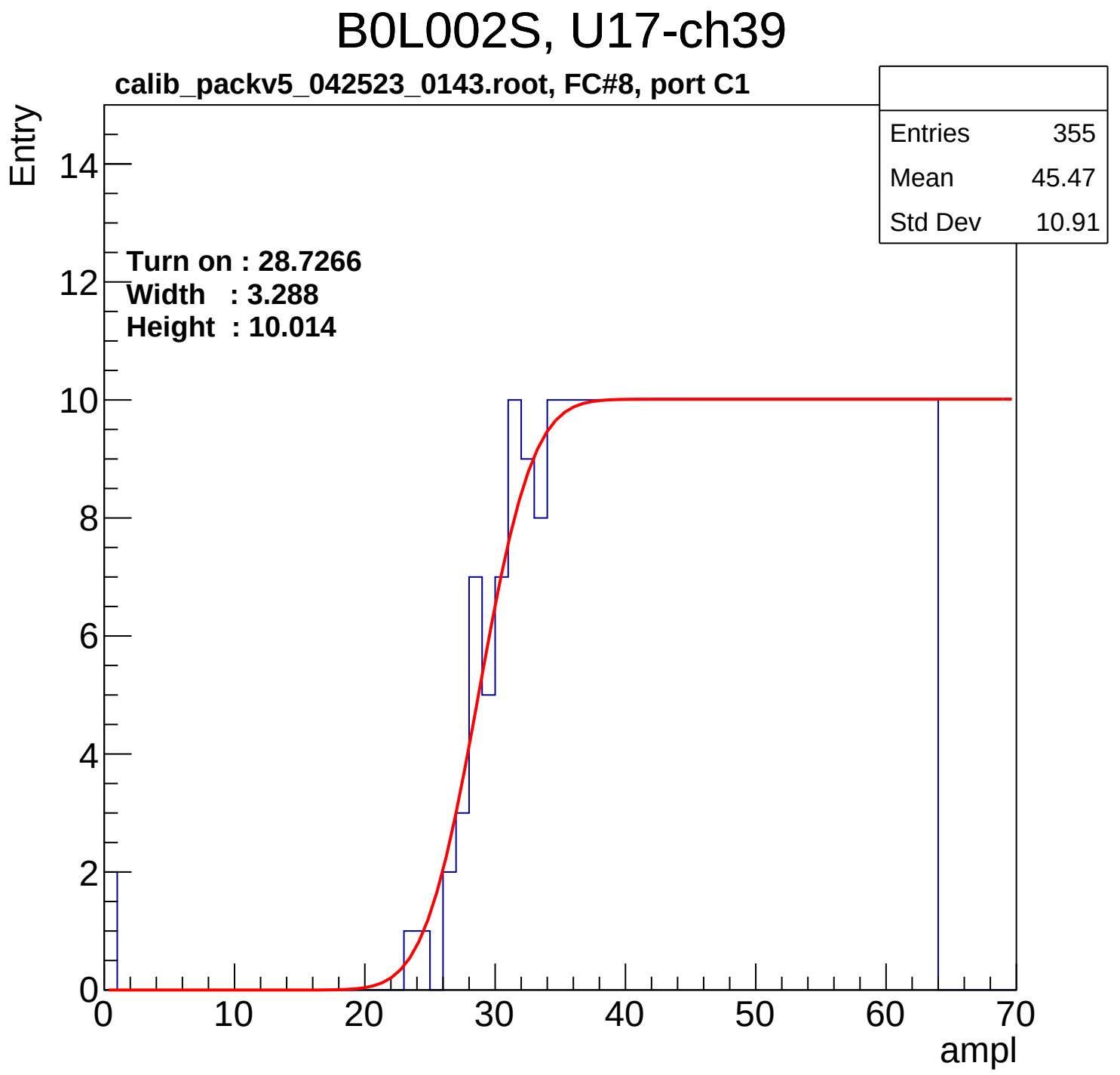
B0L002S, U17-ch39
calib_packv5_042523_0143.root, FC#8, port C1
Entries 355
Mean 45.47
Std Dev 10.91
Turn on : 28.7266
Width : 3.288
Height : 10.014
Entry
ampl
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2
4
6
8
10
12
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0
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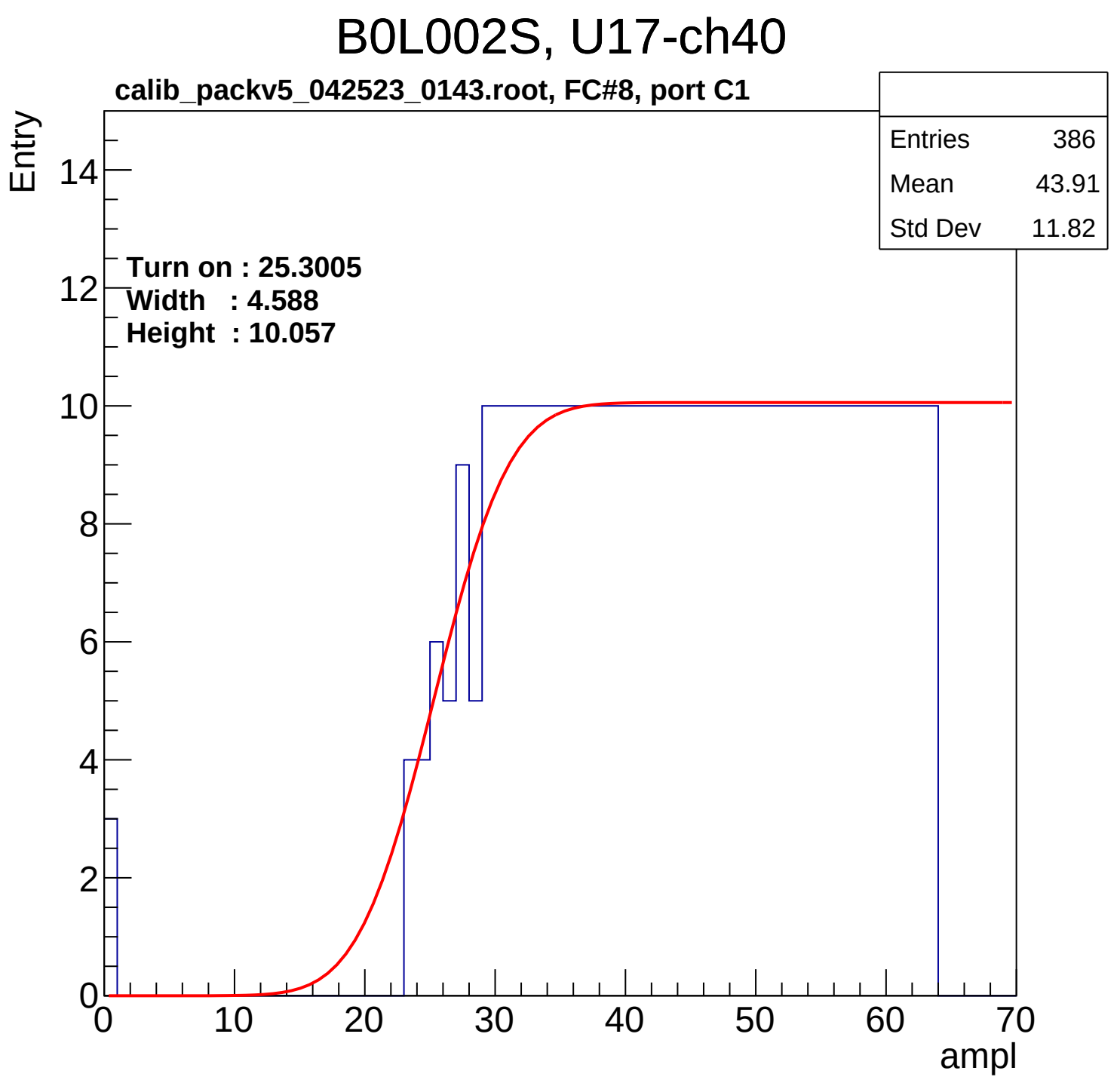
B0L002S, U17-ch40
calib_packv5_042523_0143.root, FC#8, port C1
Entries 386
Mean 43.91
Std Dev 11.82
Turn on : 25.3005
Width : 4.588
Height : 10.057
Entry
ampl
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6
8
10
12
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0
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20
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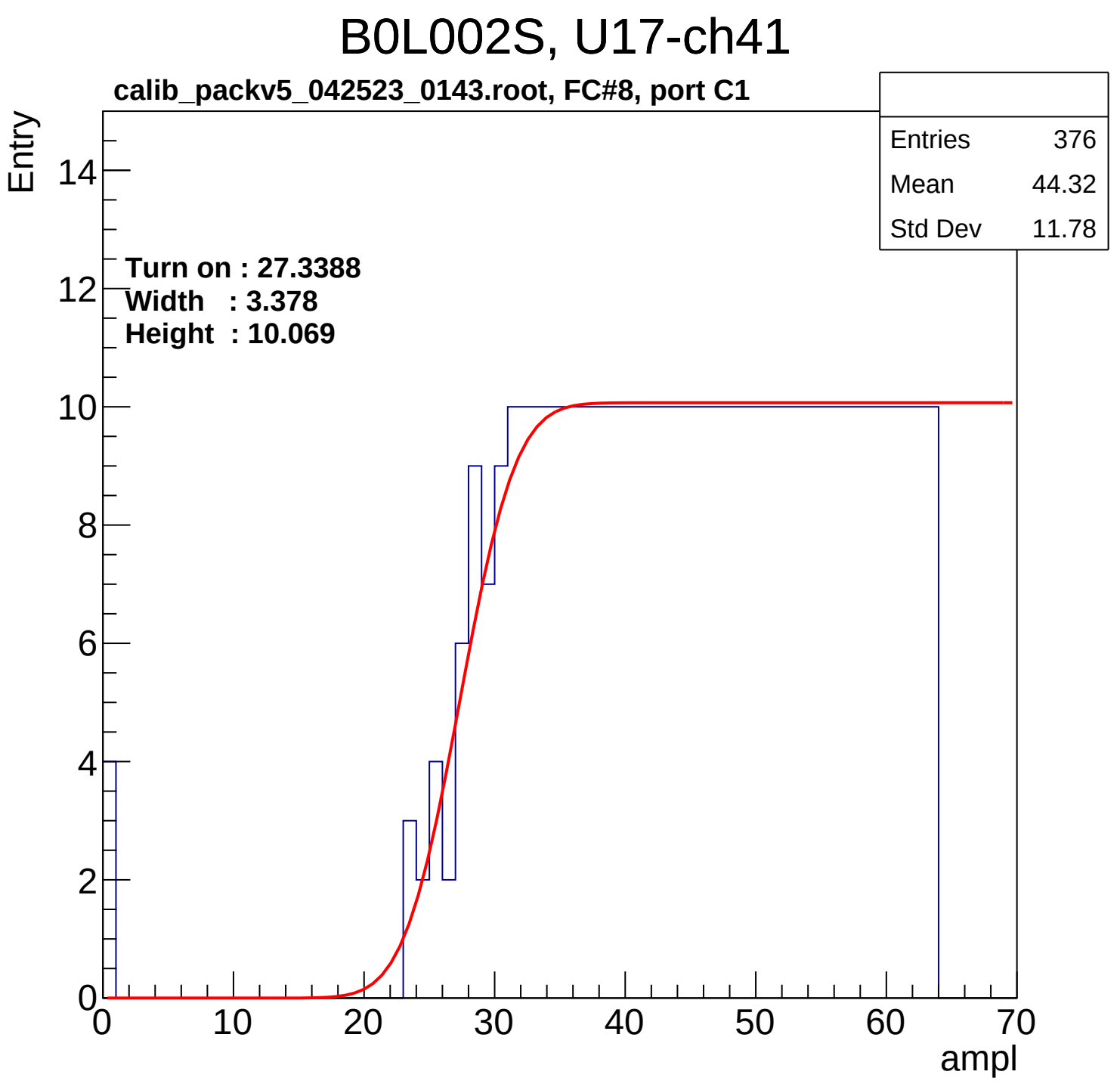
B0L002S, U17-ch41
calib_packv5_042523_0143.root, FC#8, port C1
Entries 376
Mean 44.32
Std Dev 11.78
Turn on : 27.3388
Width : 3.378
Height : 10.069
Entry
ampl
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2
4
6
8
10
12
14
0
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20
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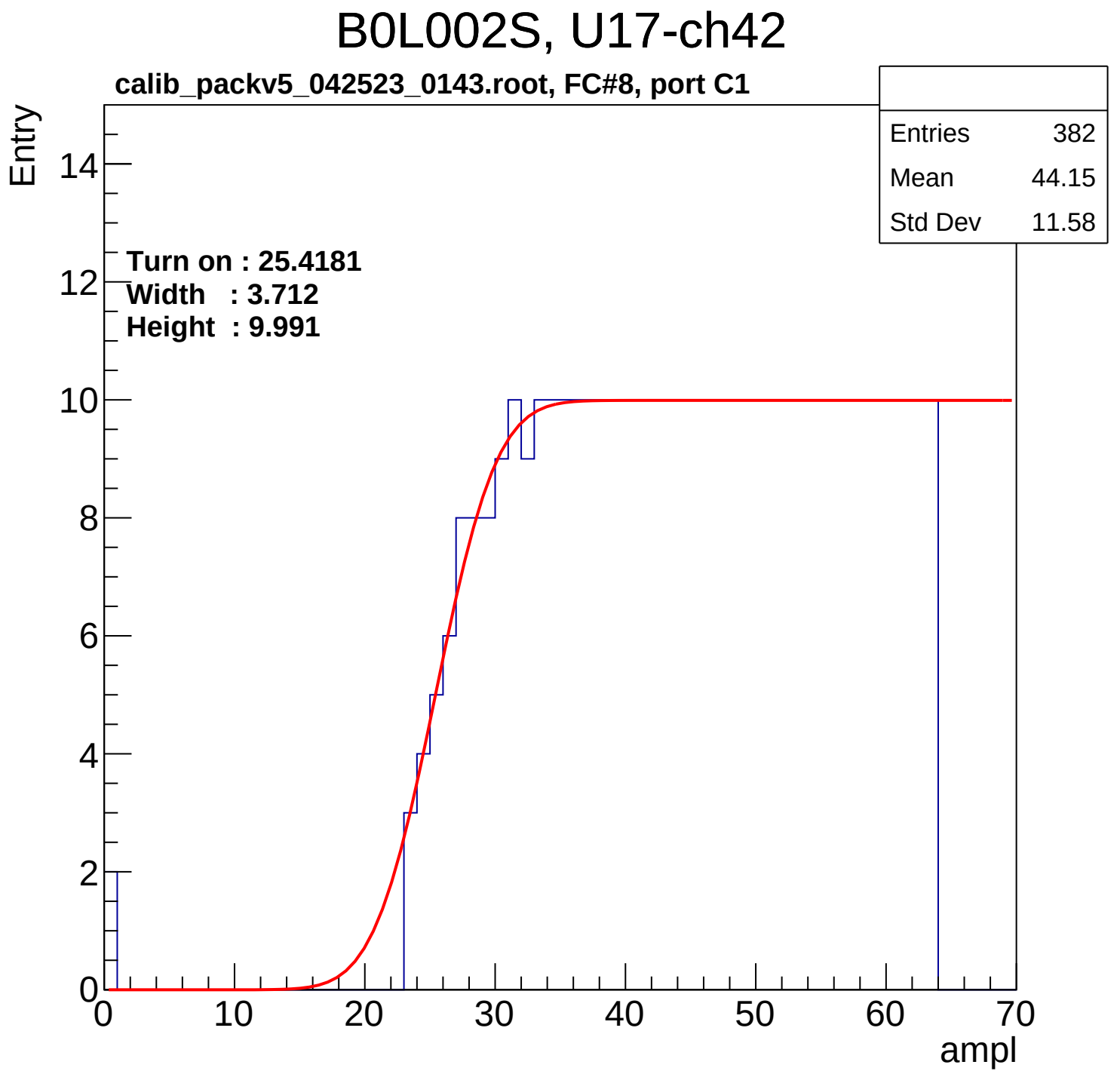
B0L002S, U17-ch42
calib_packv5_042523_0143.root, FC#8, port C1
Entries 382
Mean 44.15
Std Dev 11.58
Turn on : 25.4181
Width : 3.712
Height : 9.991
Entry
ampl
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2
4
6
8
10
12
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0
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20
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40
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60
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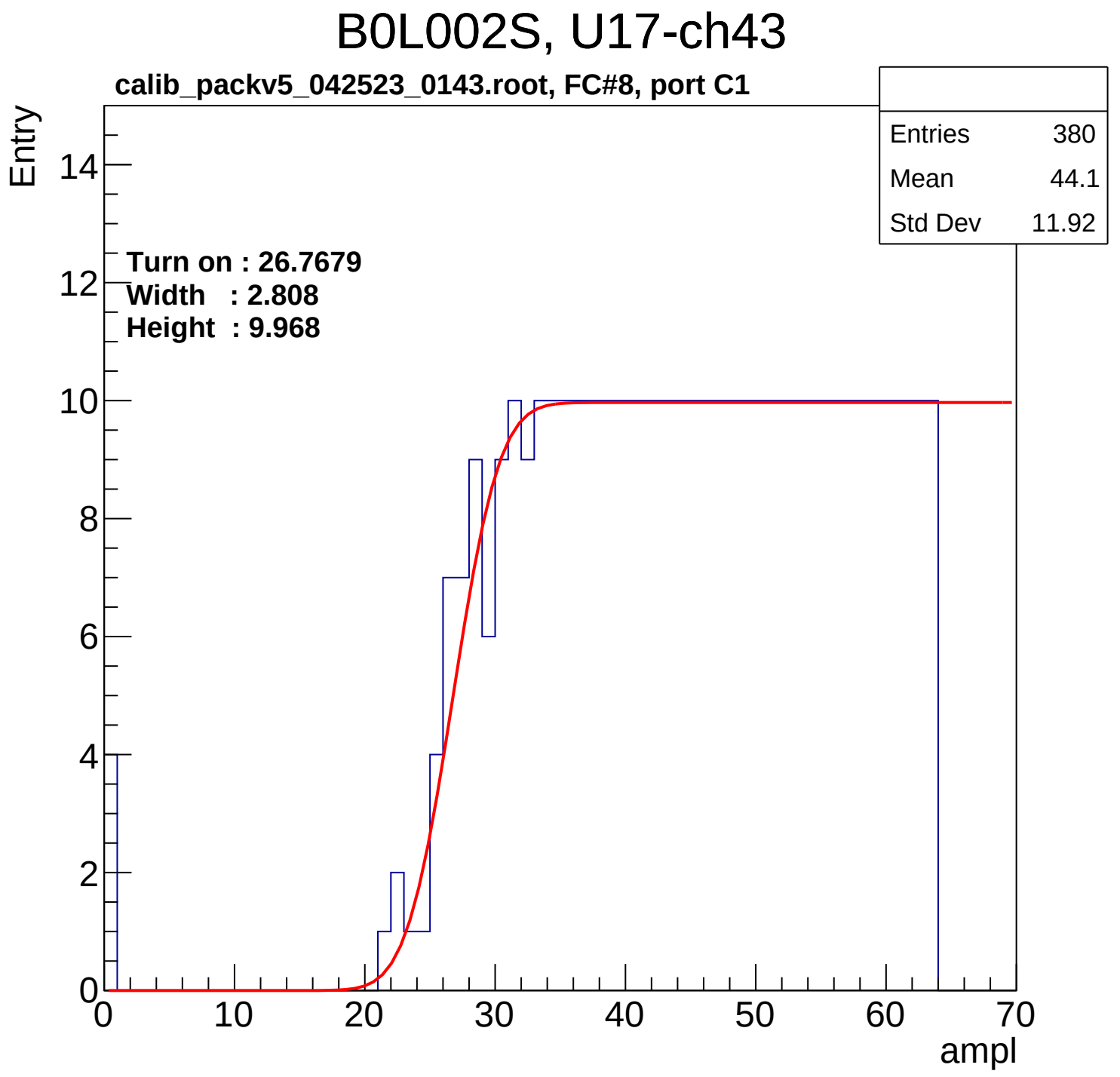
B0L002S, U17-ch43
calib_packv5_042523_0143.root, FC#8, port C1
Entries 380
Mean 44.1
Std Dev 11.92
Turn on : 26.7679
Width : 2.808
Height : 9.968
Entry
ampl
0
2
4
6
8
10
12
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0
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20
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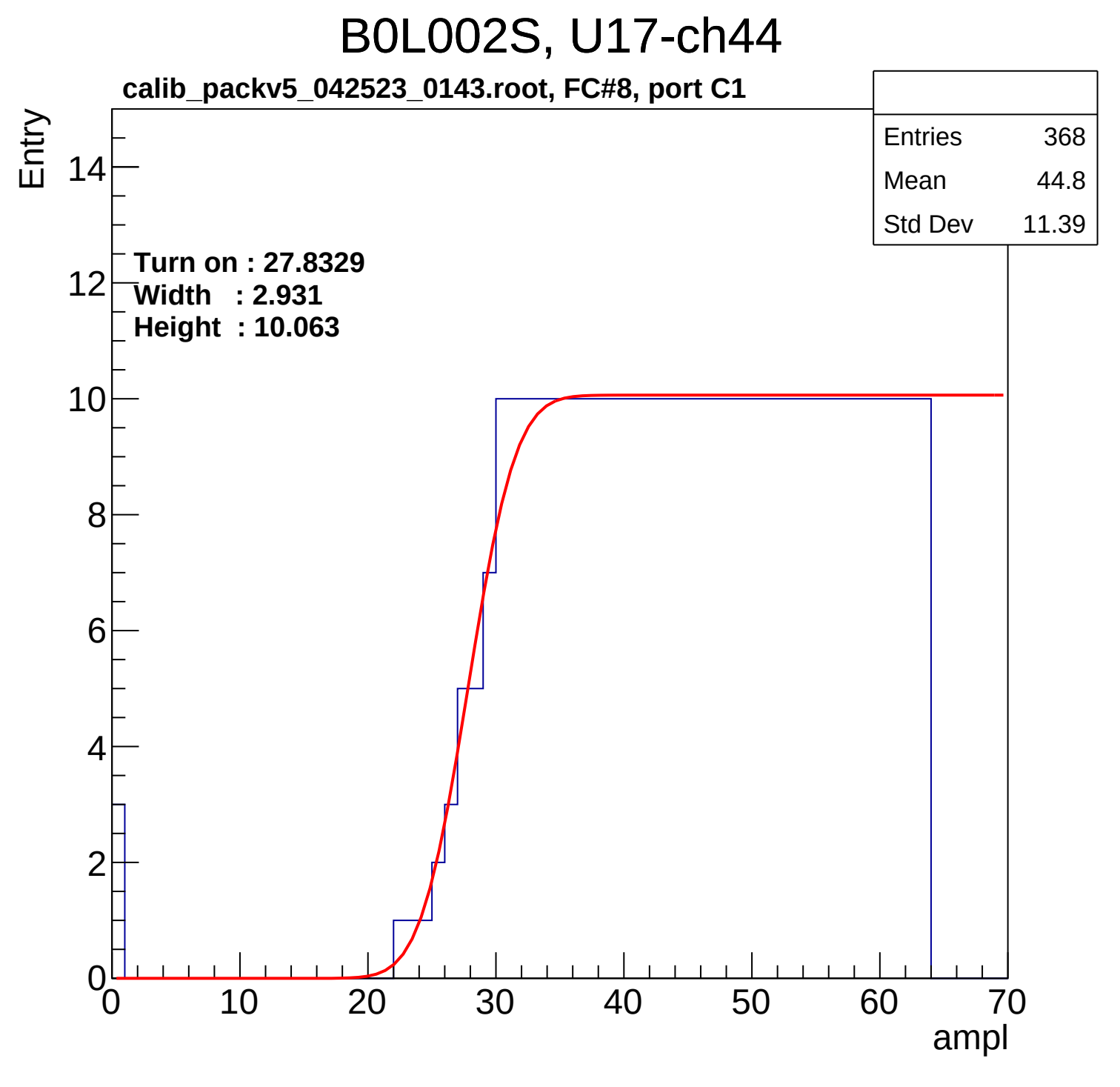
B0L002S, U17-ch44
calib_packv5_042523_0143.root, FC#8, port C1
Entries 368
Mean 44.8
Std Dev 11.39
Turn on : 27.8329
Width : 2.931
Height : 10.063
Entry
ampl
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2
4
6
8
10
12
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0
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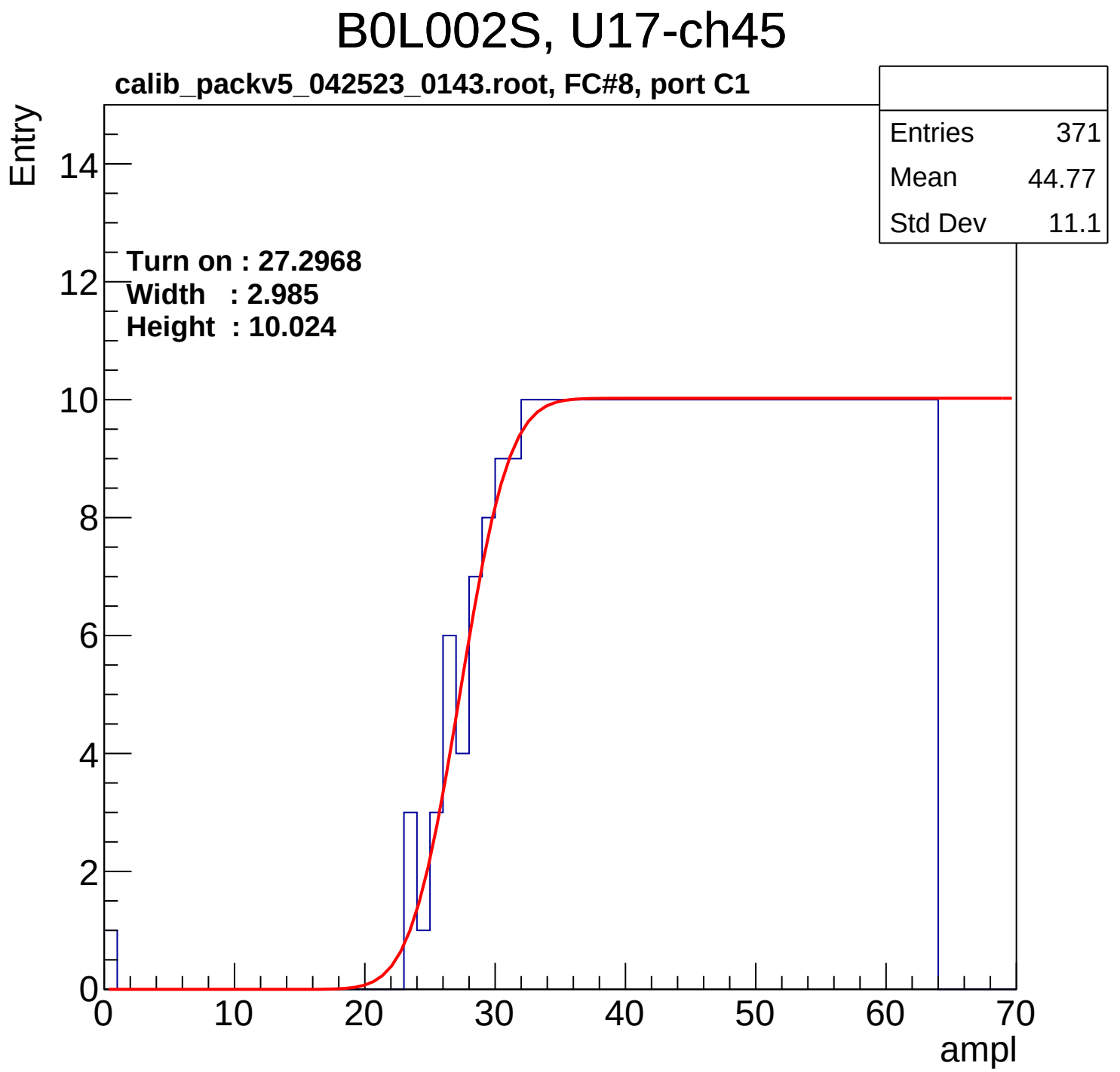
B0L002S, U17-ch45
calib_packv5_042523_0143.root, FC#8, port C1
Entries 371
Mean 44.77
Std Dev 11.1
Turn on : 27.2968
Width : 2.985
Height : 10.024
Entry
ampl
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2
4
6
8
10
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0
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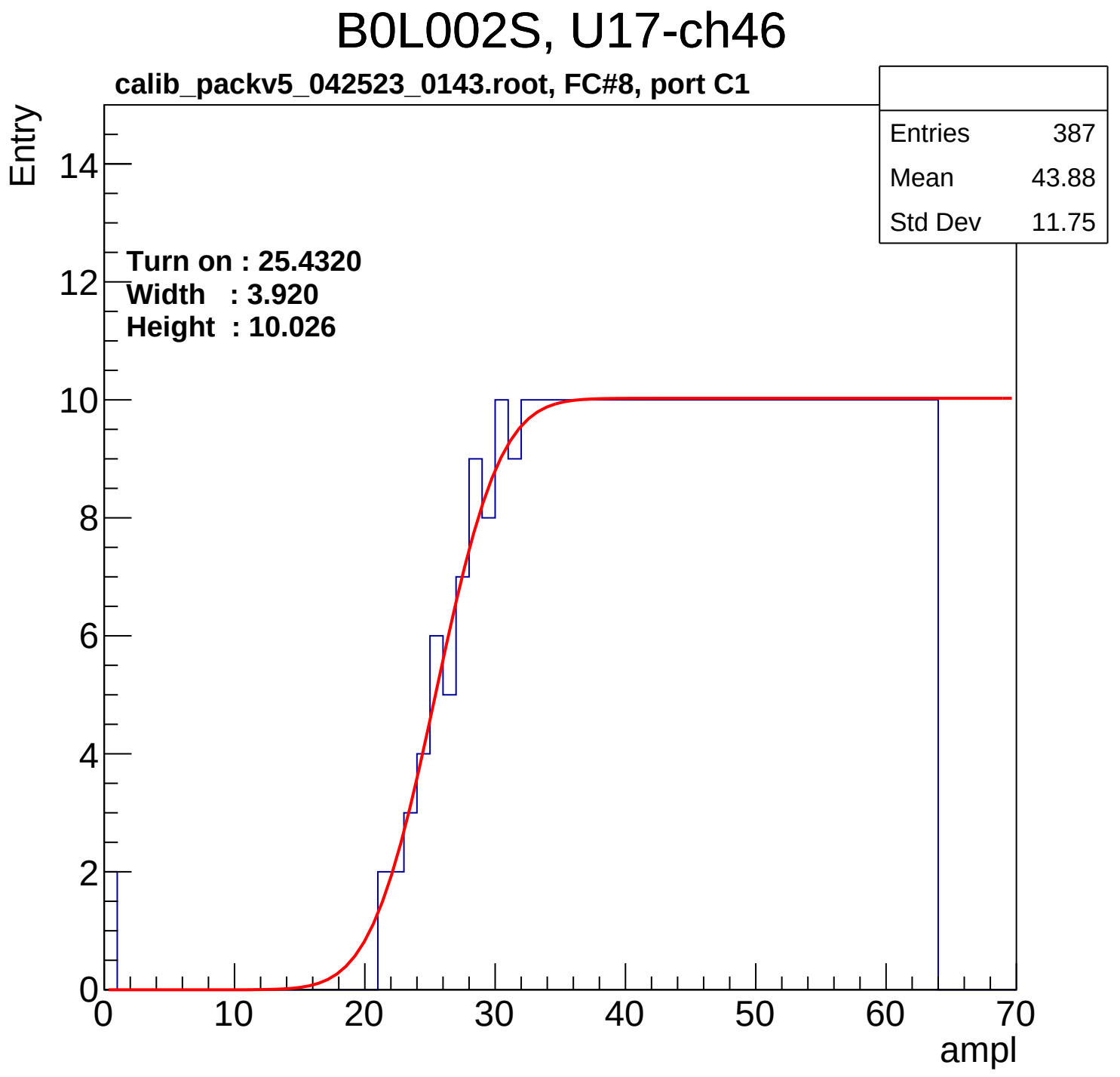
B0L002S, U17-ch46
calib_packv5_042523_0143.root, FC#8, port C1
Entries 387
Mean 43.88
Std Dev 11.75
Turn on : 25.4320
Width : 3.920
Height : 10.026
Entry
ampl
0
2
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6
8
10
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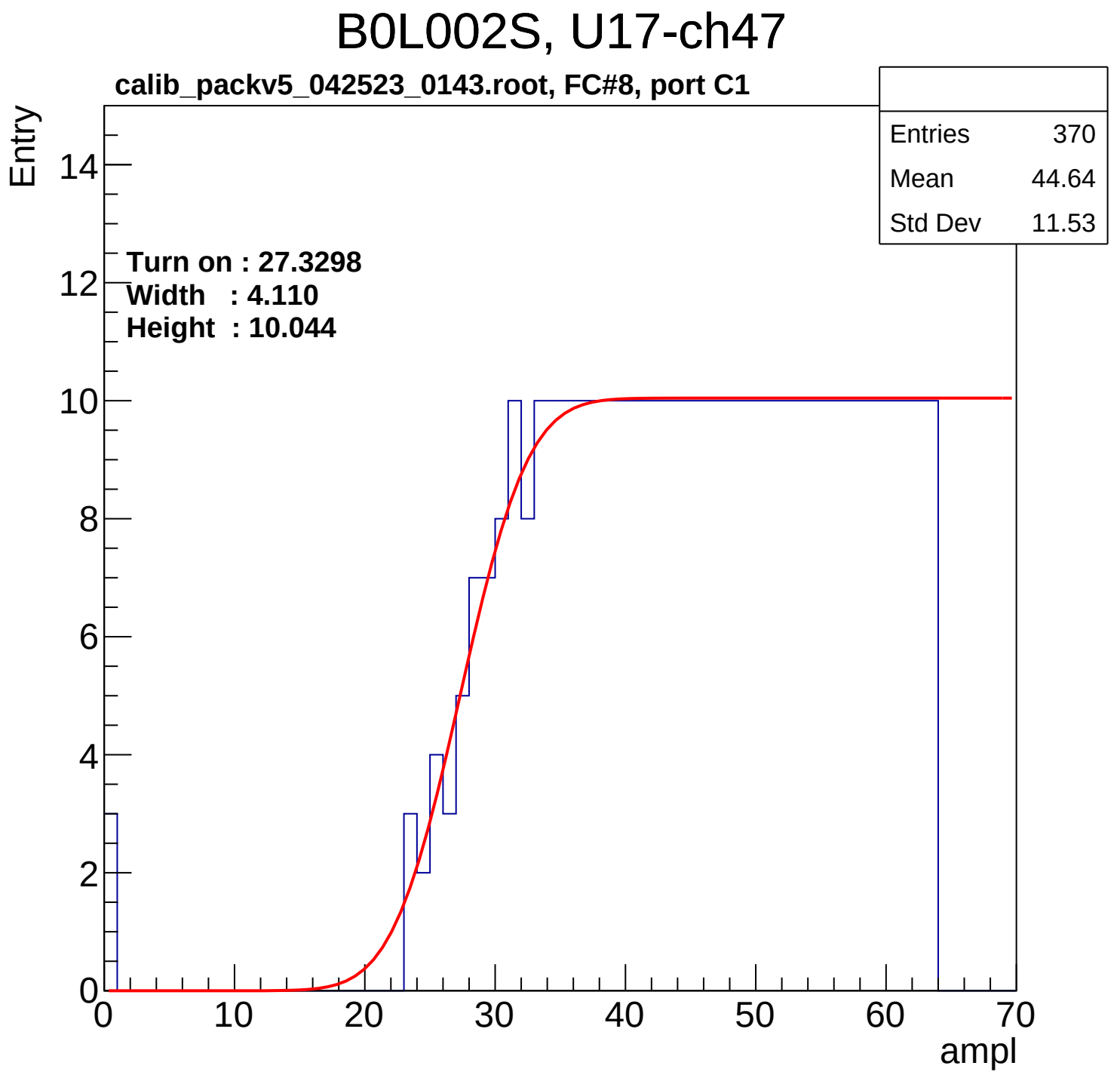
B0L002S, U17-ch47
calib_packv5_042523_0143.root, FC#8, port C1
Entries 370
Mean 44.64
Std Dev 11.53
Turn on : 27.3298
Width : 4.110
Height : 10.044
Entry
ampl
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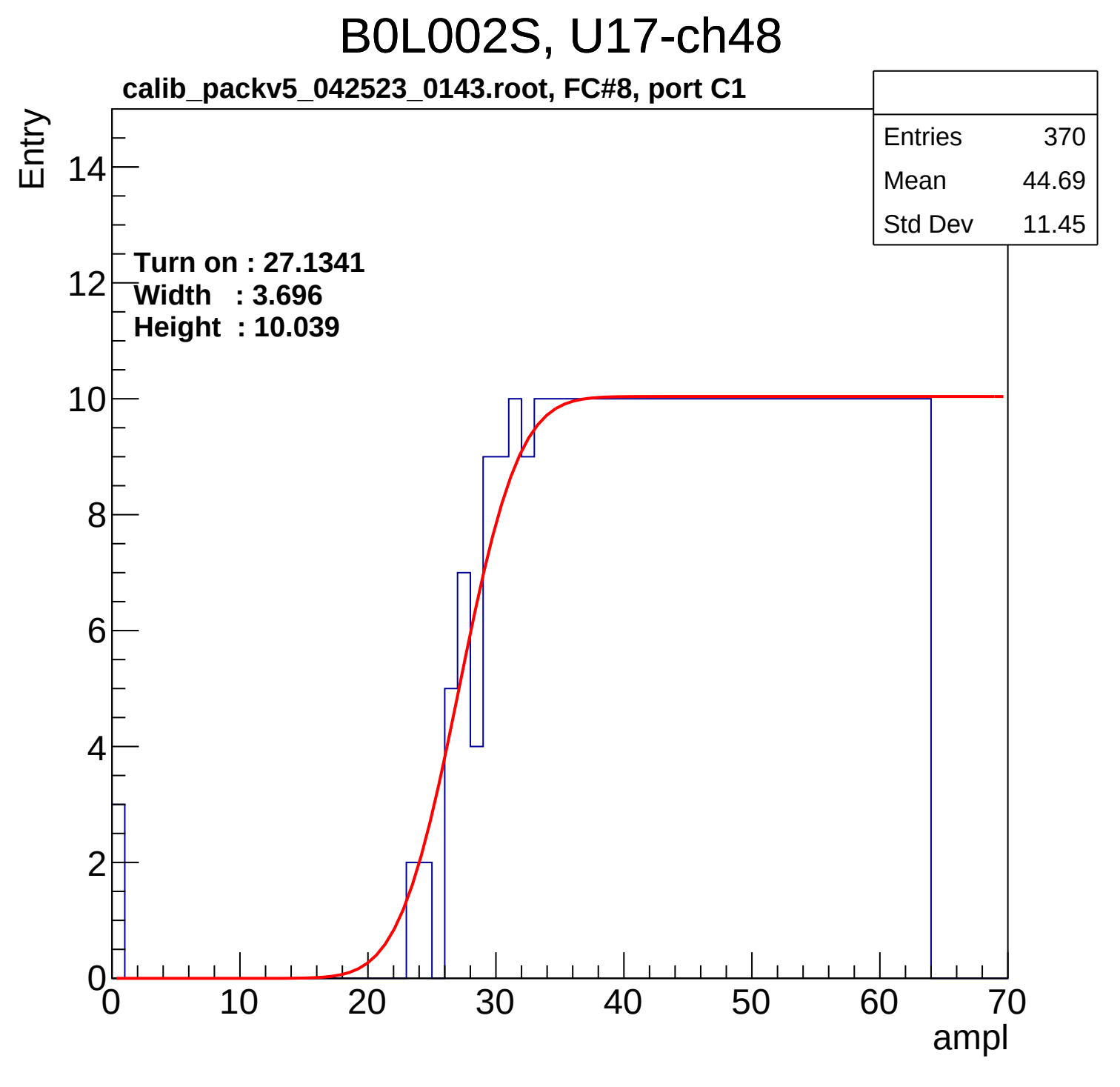
B0L002S, U17-ch48
calib_packv5_042523_0143.root, FC#8, port C1
Entries 370
Mean 44.69
Std Dev 11.45
Turn on : 27.1341
Width : 3.696
Height : 10.039
Entry
ampl
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2
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8
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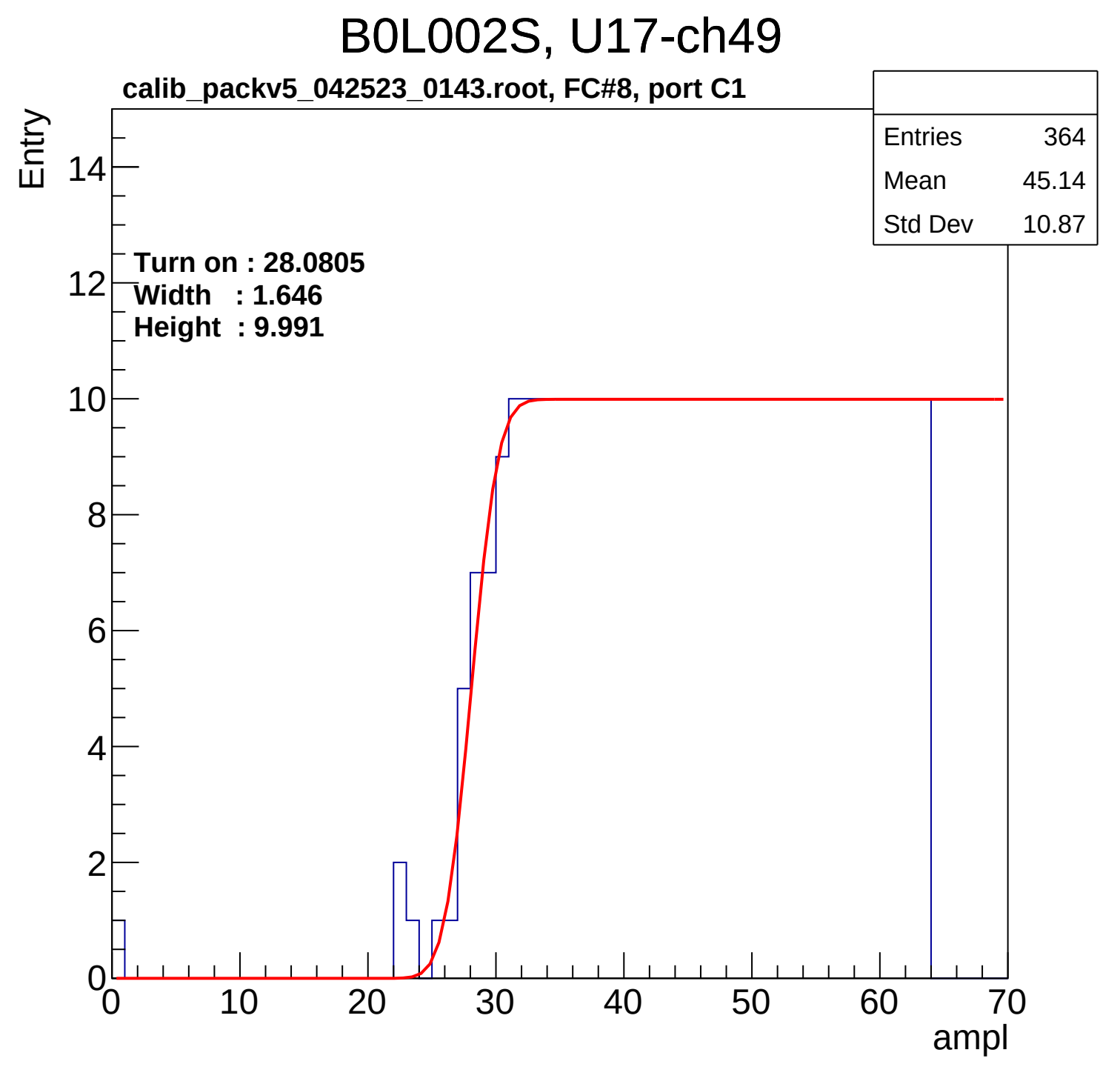
B0L002S, U17-ch49
calib_packv5_042523_0143.root, FC#8, port C1
Entries 364
Mean 45.14
Std Dev 10.87
Turn on : 28.0805
Width : 1.646
Height : 9.991
Entry
ampl
0
2
4
6
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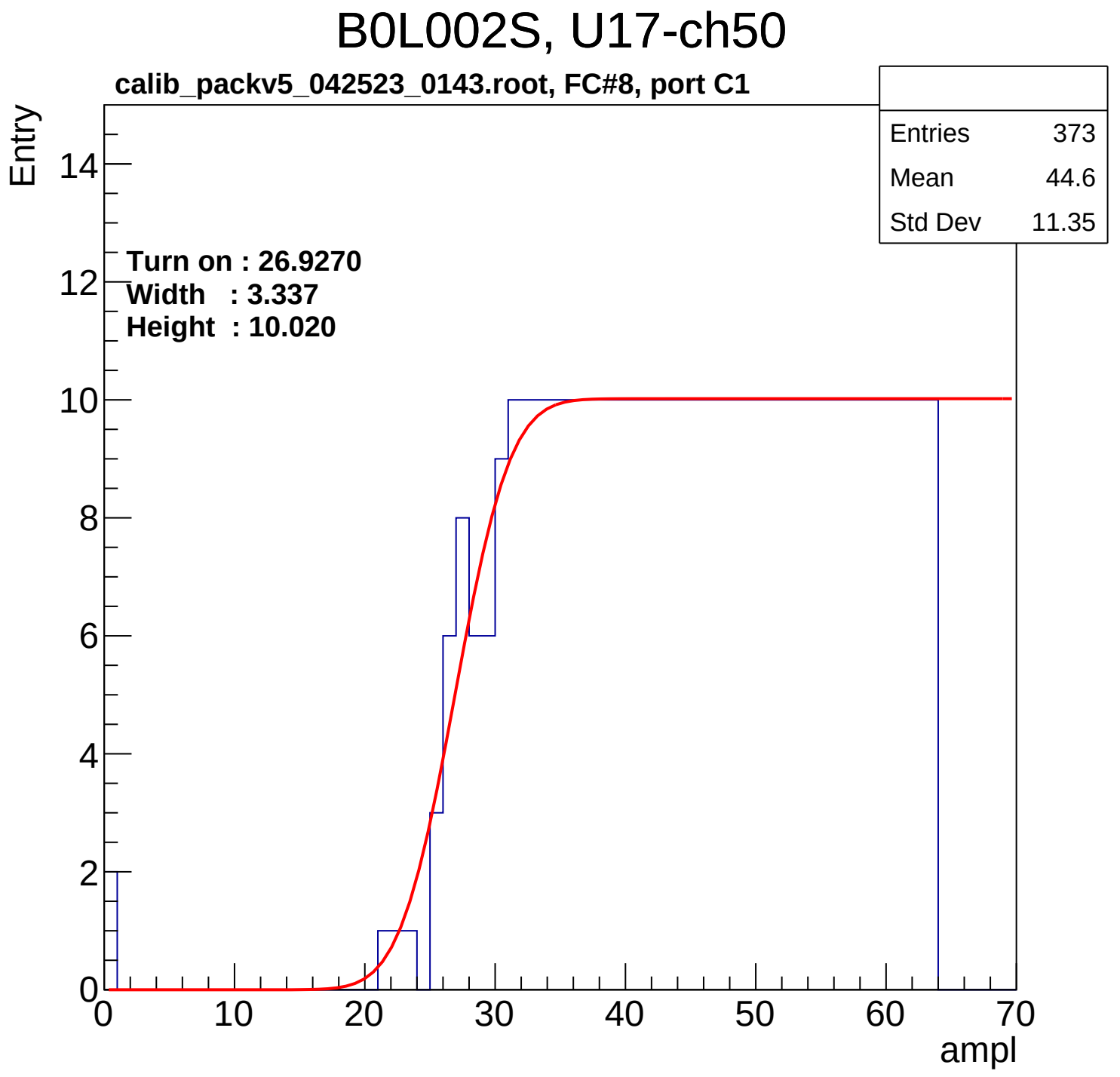
B0L002S, U17-ch50
calib_packv5_042523_0143.root, FC#8, port C1
Entries 373
Mean 44.6
Std Dev 11.35
Turn on : 26.9270
Width : 3.337
Height : 10.020
Entry
ampl
0
2
4
6
8
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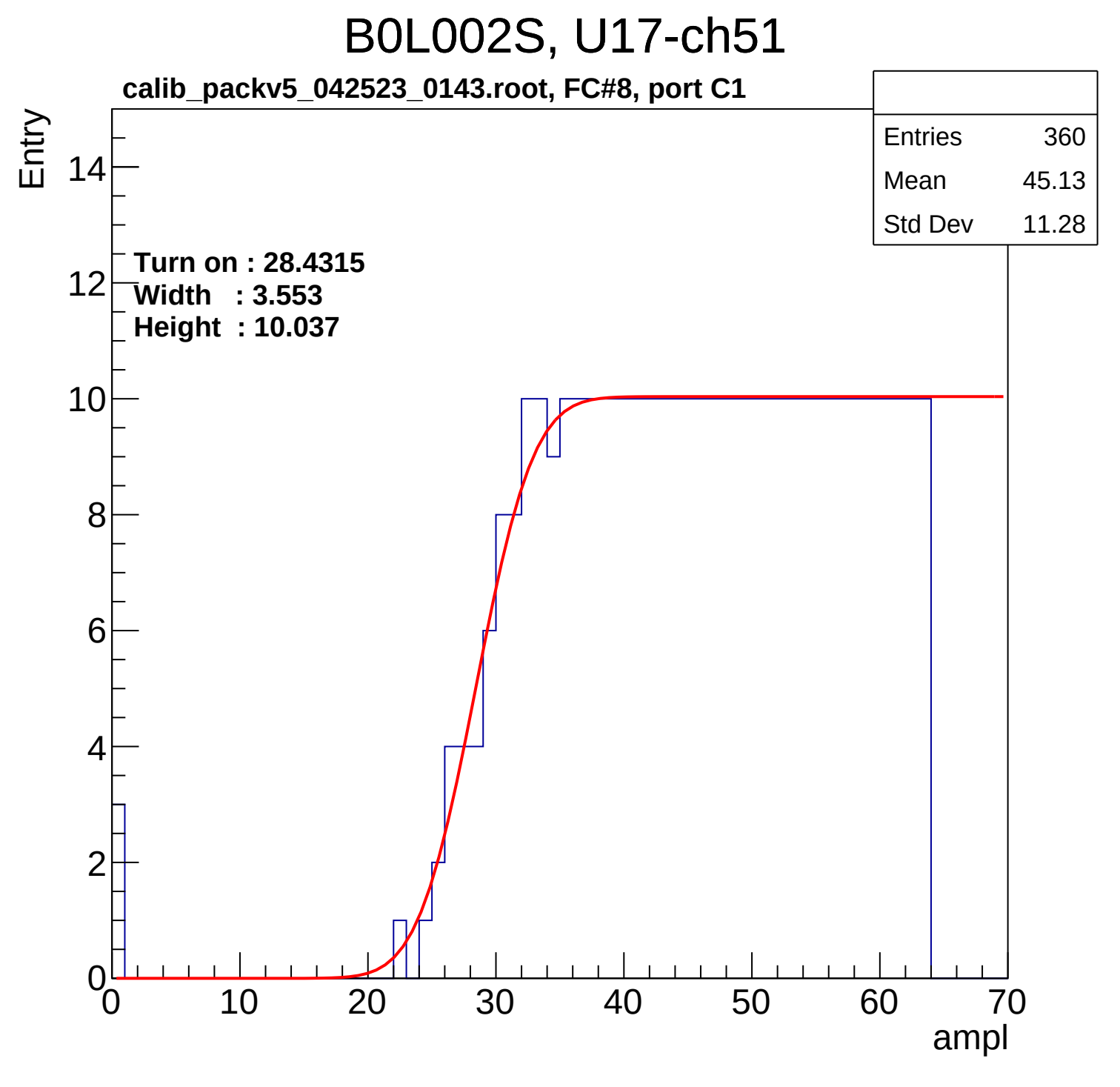
B0L002S, U17-ch51
calib_packv5_042523_0143.root, FC#8, port C1
Entries 360
Mean 45.13
Std Dev 11.28
Turn on : 28.4315
Width : 3.553
Height : 10.037
Entry
ampl
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2
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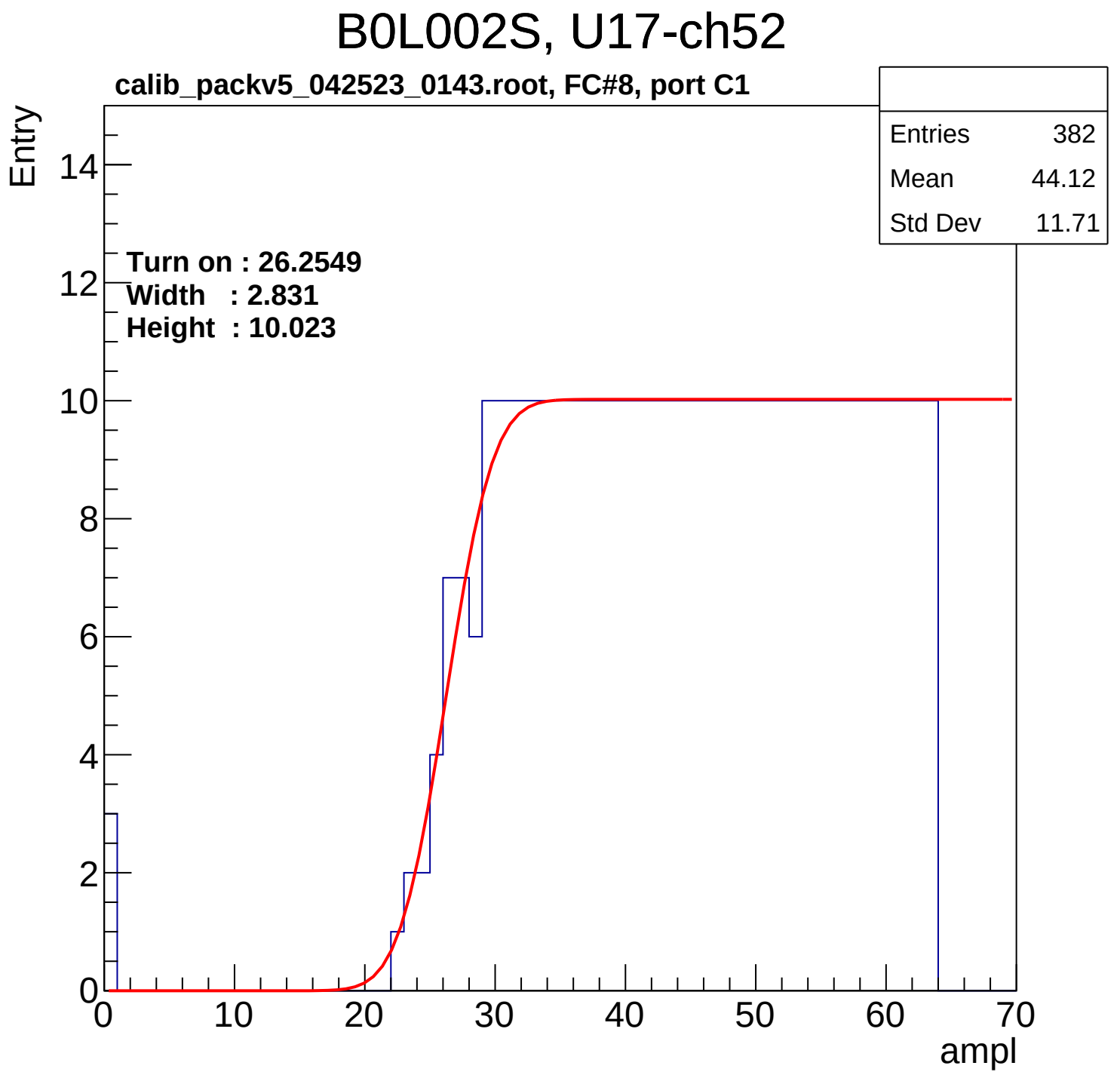
B0L002S, U17-ch52
calib_packv5_042523_0143.root, FC#8, port C1
Entries 382
Mean 44.12
Std Dev 11.71
Turn on : 26.2549
Width : 2.831
Height : 10.023
Entry
ampl
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2
4
6
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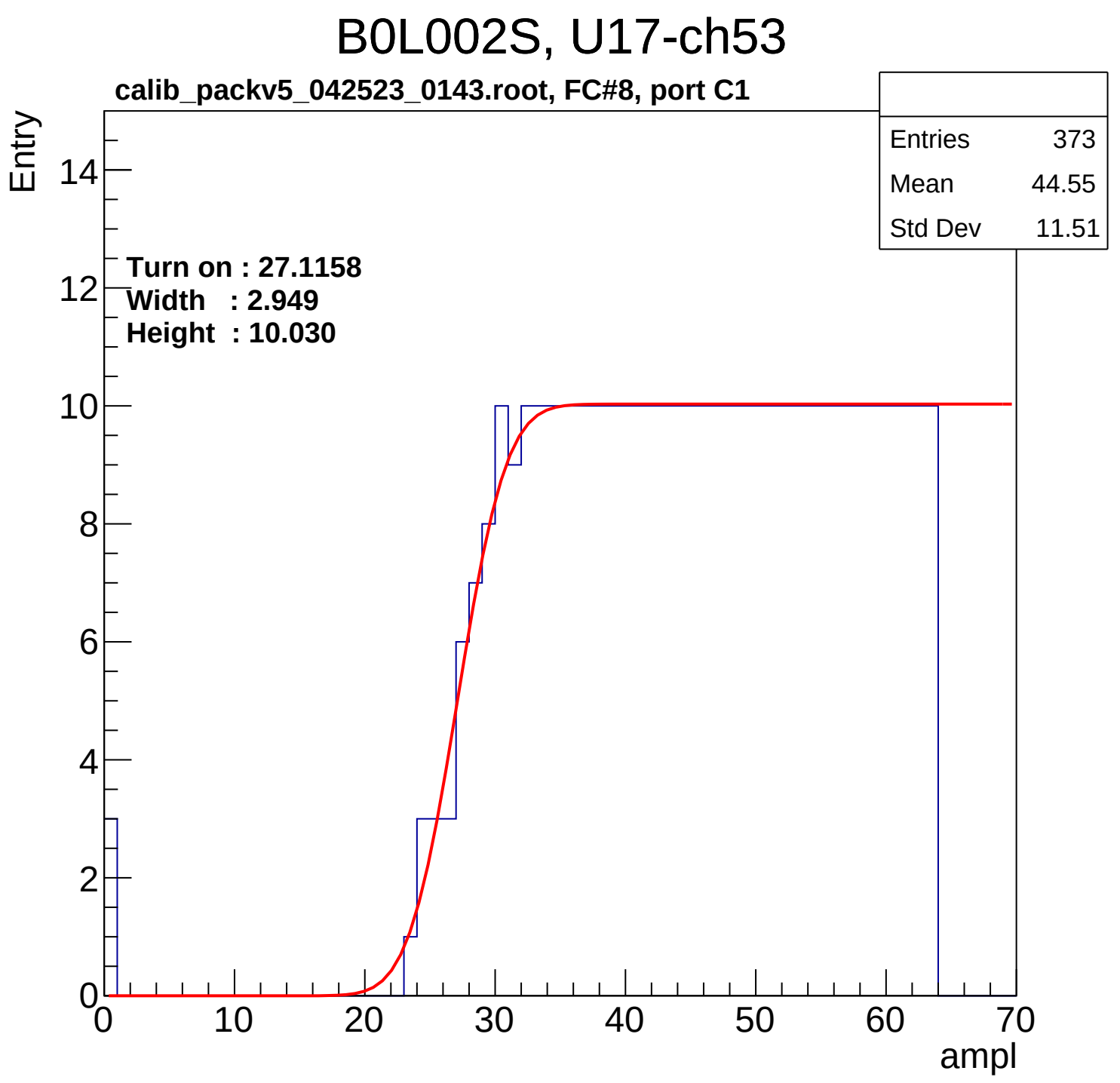
B0L002S, U17-ch53
calib_packv5_042523_0143.root, FC#8, port C1
Entries 373
Mean 44.55
Std Dev 11.51
Turn on : 27.1158
Width : 2.949
Height : 10.030
Entry
ampl
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2
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6
8
10
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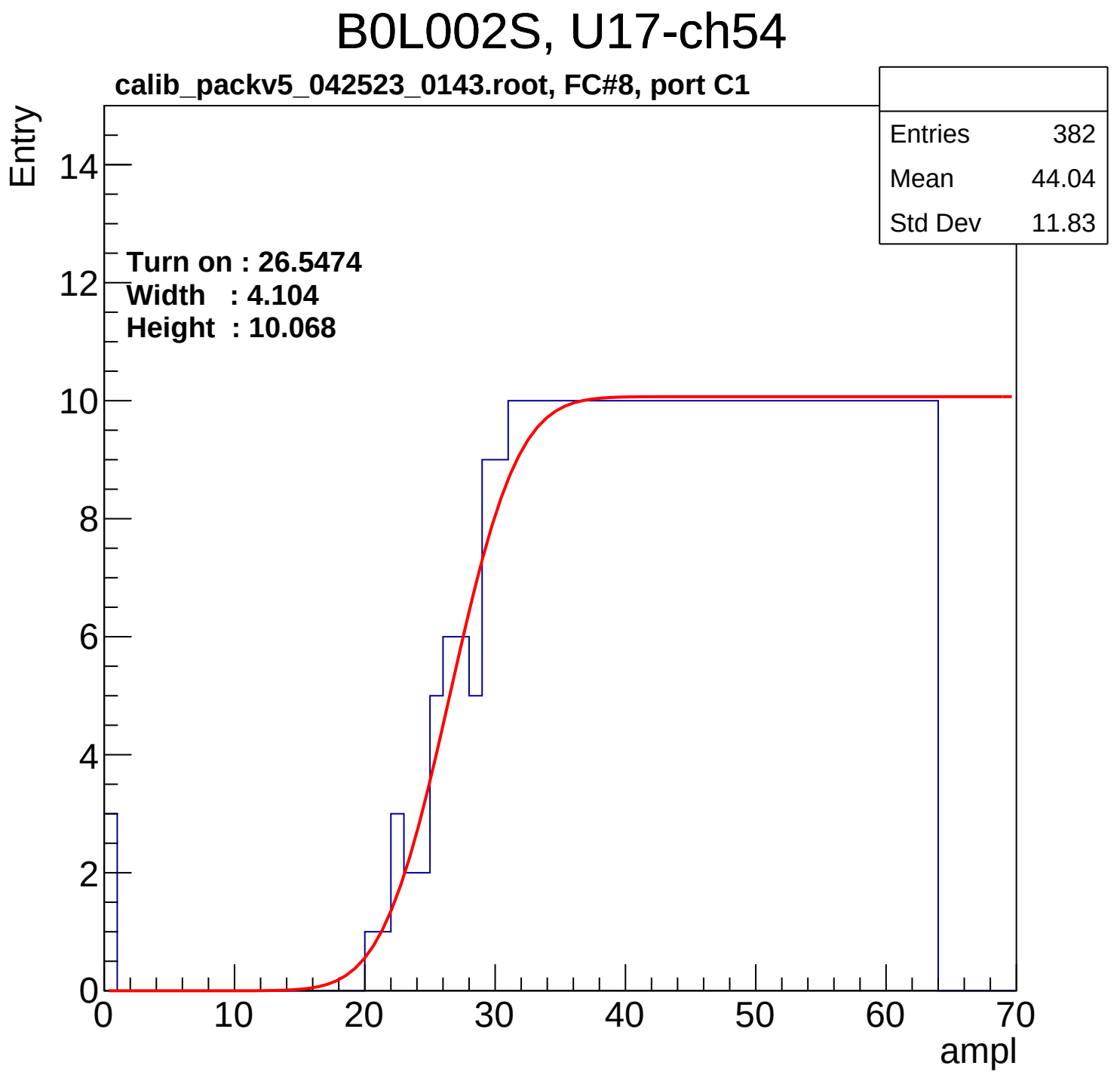
B0L002S, U17-ch54
calib_packv5_042523_0143.root, FC#8, port C1
Entries 382
Mean 44.04
Std Dev 11.83
Turn on : 26.5474
Width : 4.104
Height : 10.068
Entry
ampl
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2
4
6
8
10
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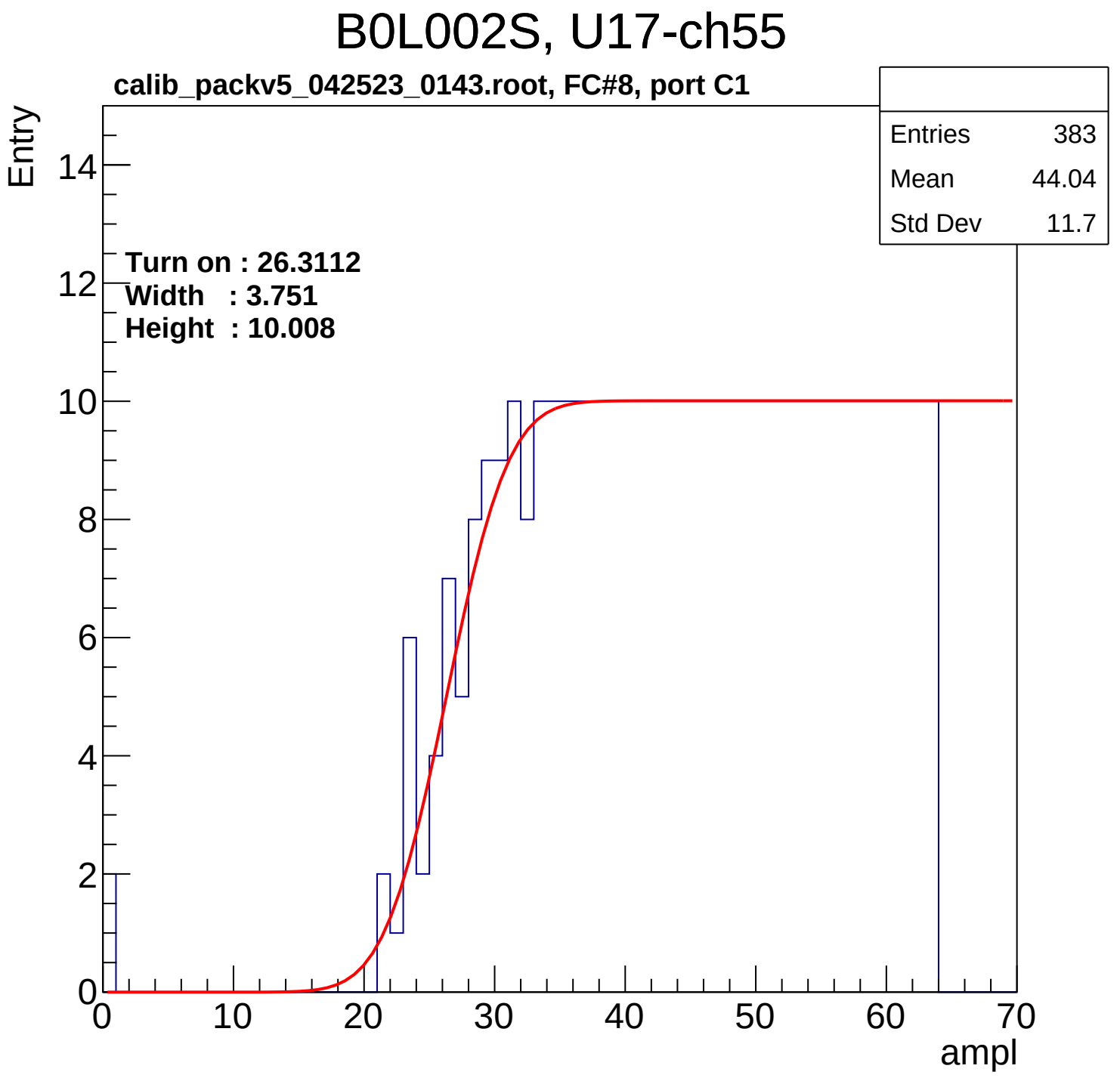
B0L002S, U17-ch55
calib_packv5_042523_0143.root, FC#8, port C1
Entries 383
Mean 44.04
Std Dev 11.7
Turn on : 26.3112
Width : 3.751
Height : 10.008
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ampl
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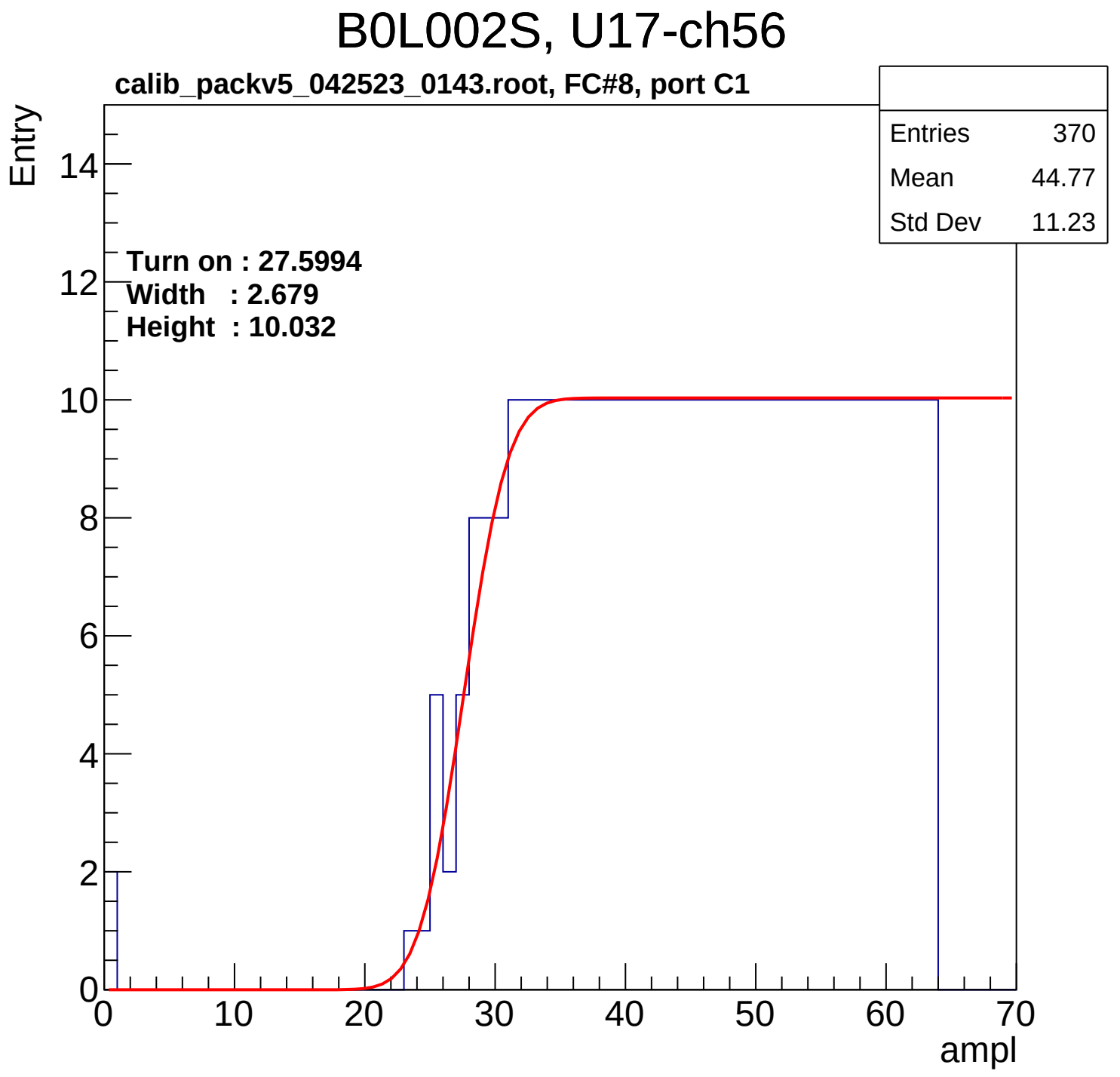
B0L002S, U17-ch56
calib_packv5_042523_0143.root, FC#8, port C1
Entries 370
Mean 44.77
Std Dev 11.23
Turn on : 27.5994
Width : 2.679
Height : 10.032
Entry
ampl
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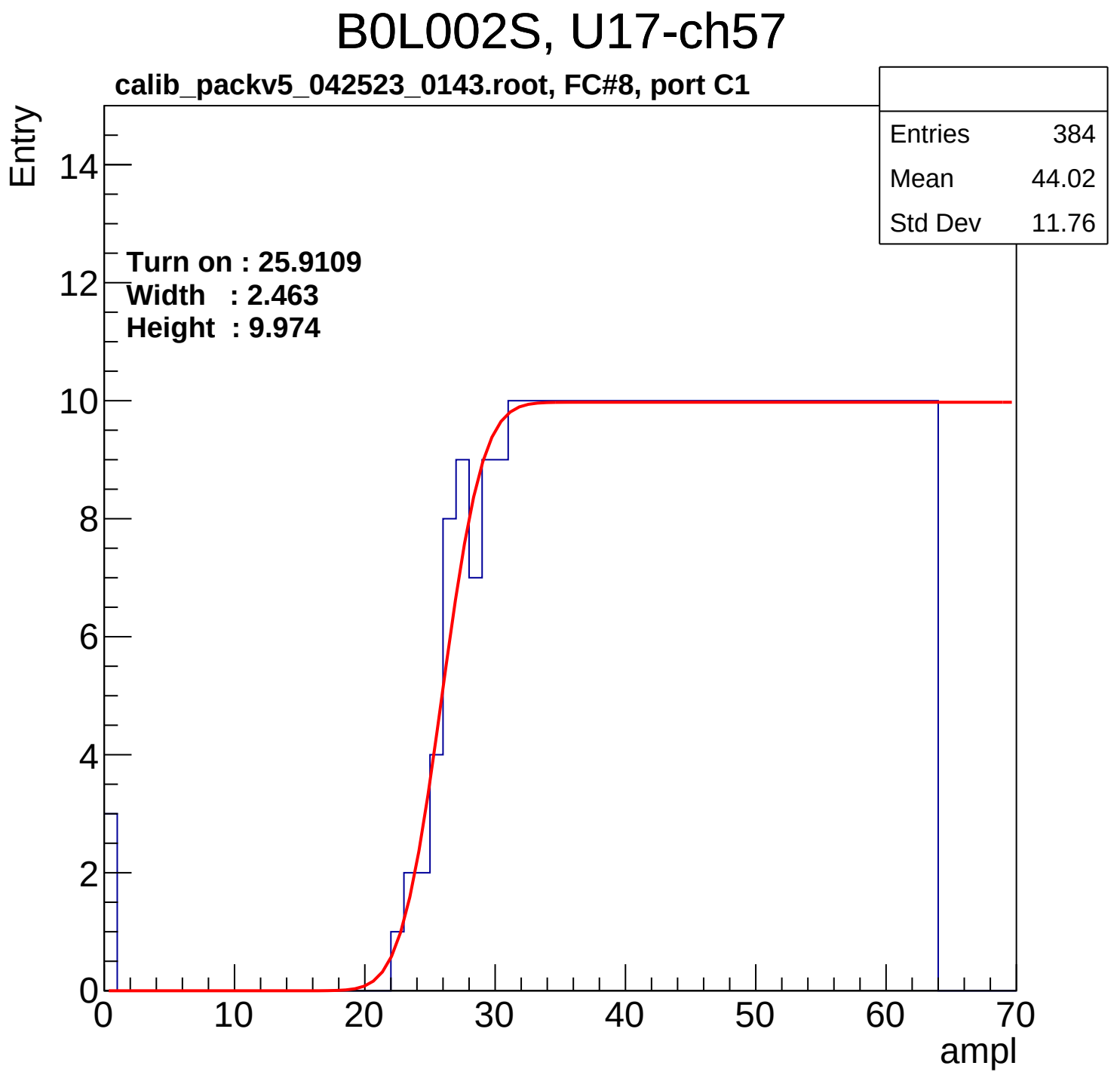
B0L002S, U17-ch57
calib_packv5_042523_0143.root, FC#8, port C1
Entries 384
Mean 44.02
Std Dev 11.76
Turn on : 25.9109
Width : 2.463
Height : 9.974
Entry
ampl
0
2
4
6
8
10
12
14
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10
20
30
40
50
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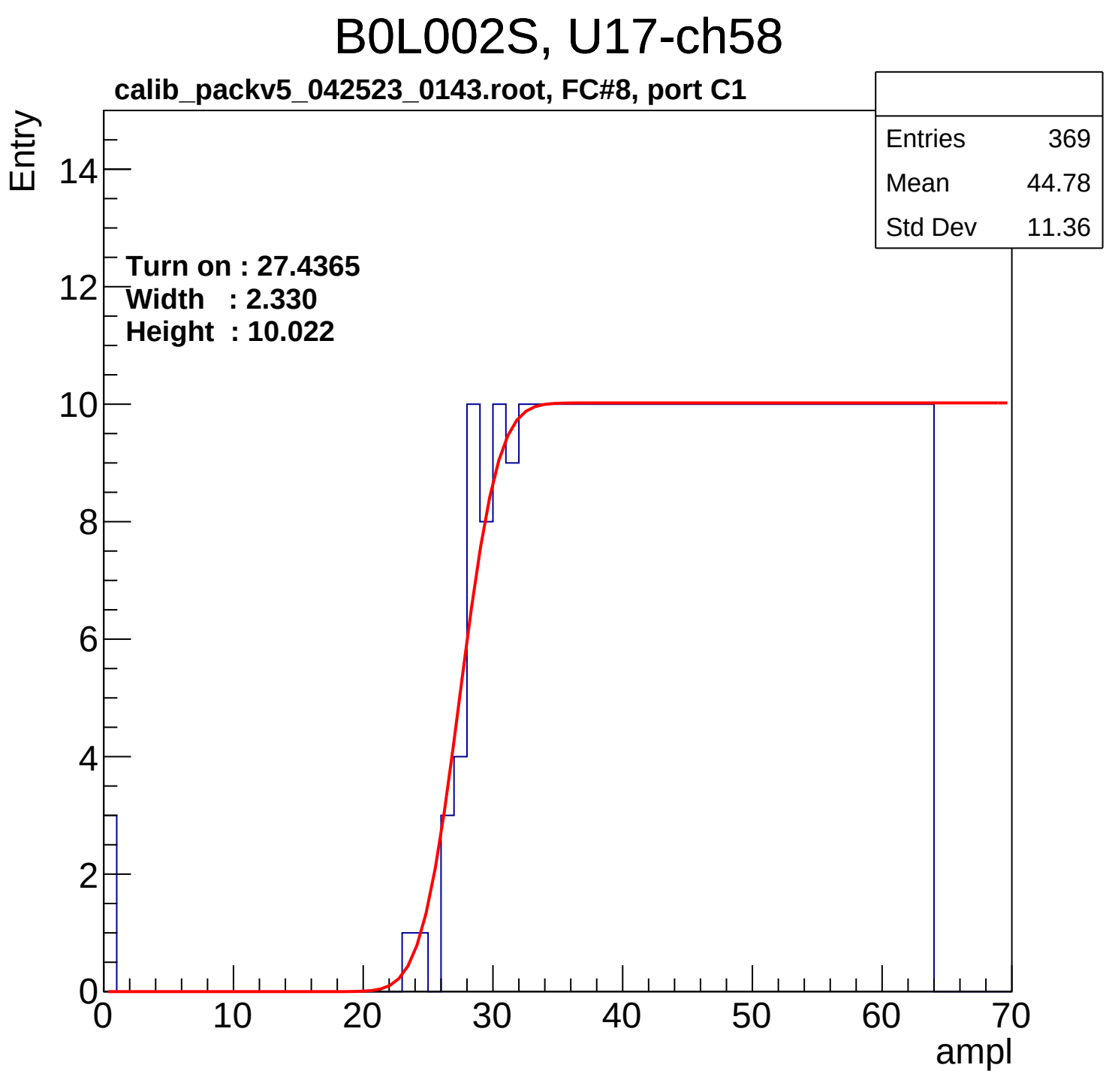
B0L002S, U17-ch58
calib_packv5_042523_0143.root, FC#8, port C1
Entries 369
Mean 44.78
Std Dev 11.36
Turn on : 27.4365
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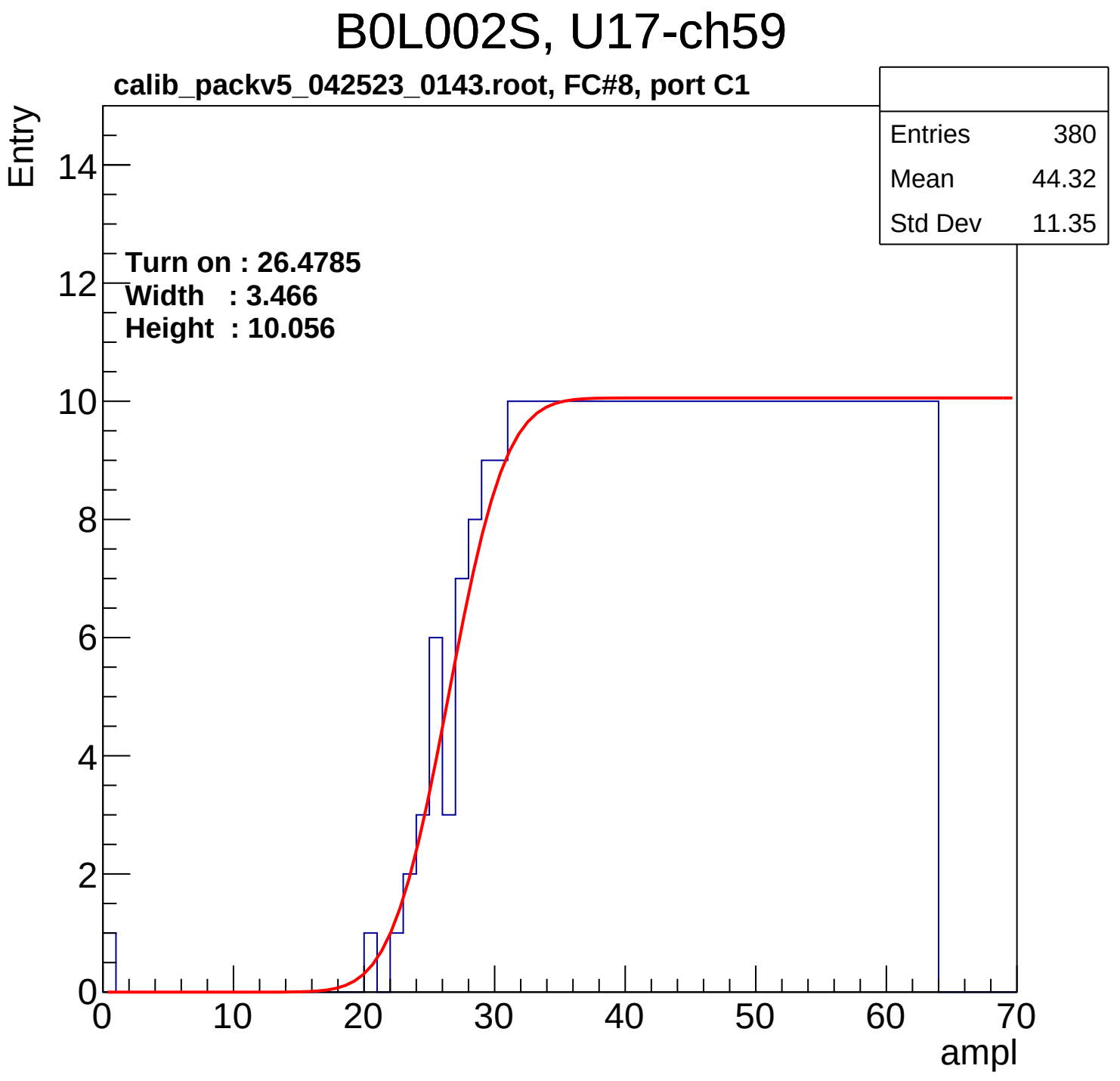
B0L002S, U17-ch59
calib_packv5_042523_0143.root, FC#8, port C1
Entries 380
Mean 44.32
Std Dev 11.35
Turn on : 26.4785
Width : 3.466
Height : 10.056
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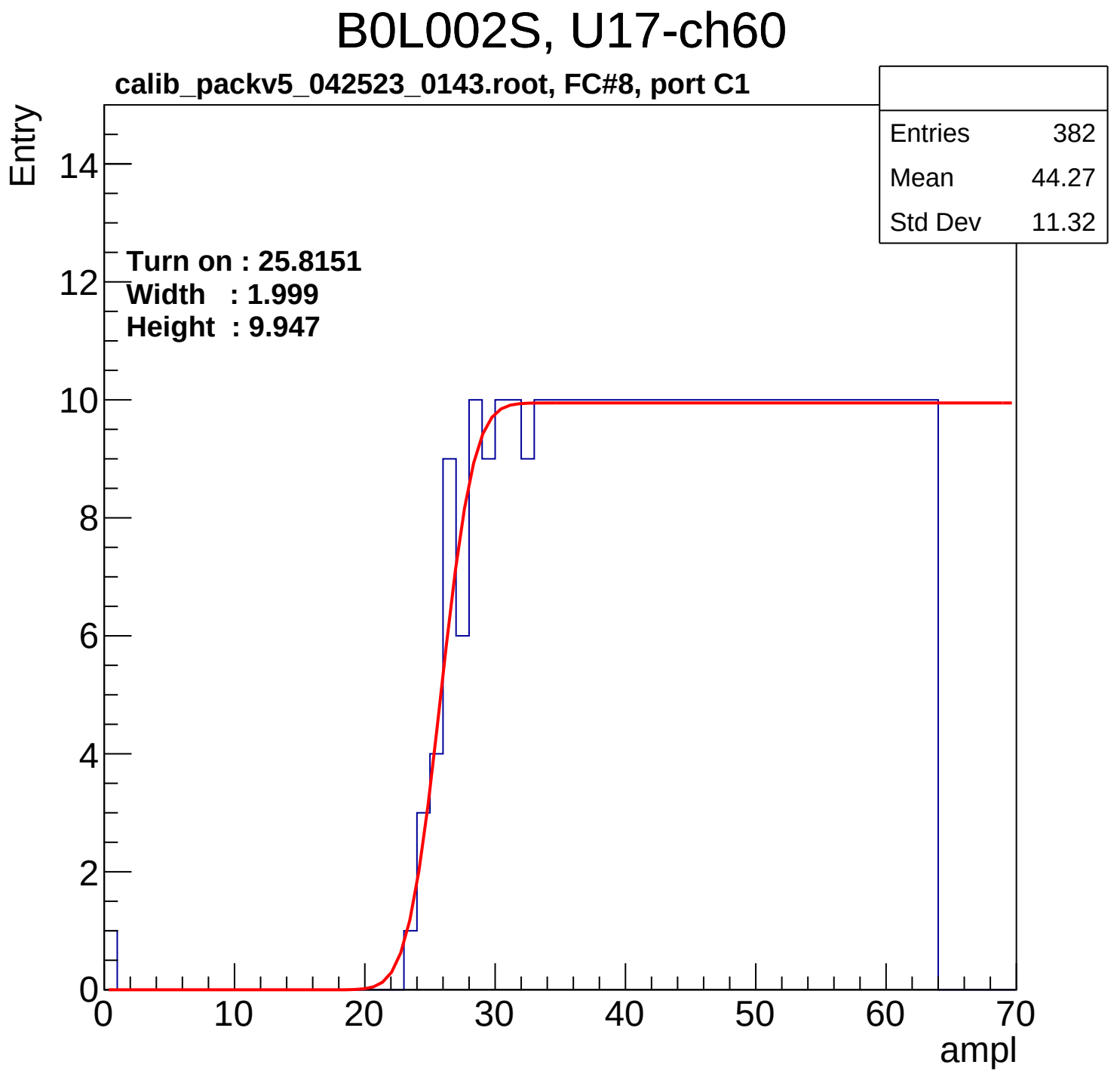
B0L002S, U17-ch60
calib_packv5_042523_0143.root, FC#8, port C1
Entries 382
Mean 44.27
Std Dev 11.32
Turn on : 25.8151
Width : 1.999
Height : 9.947
Entry
ampl
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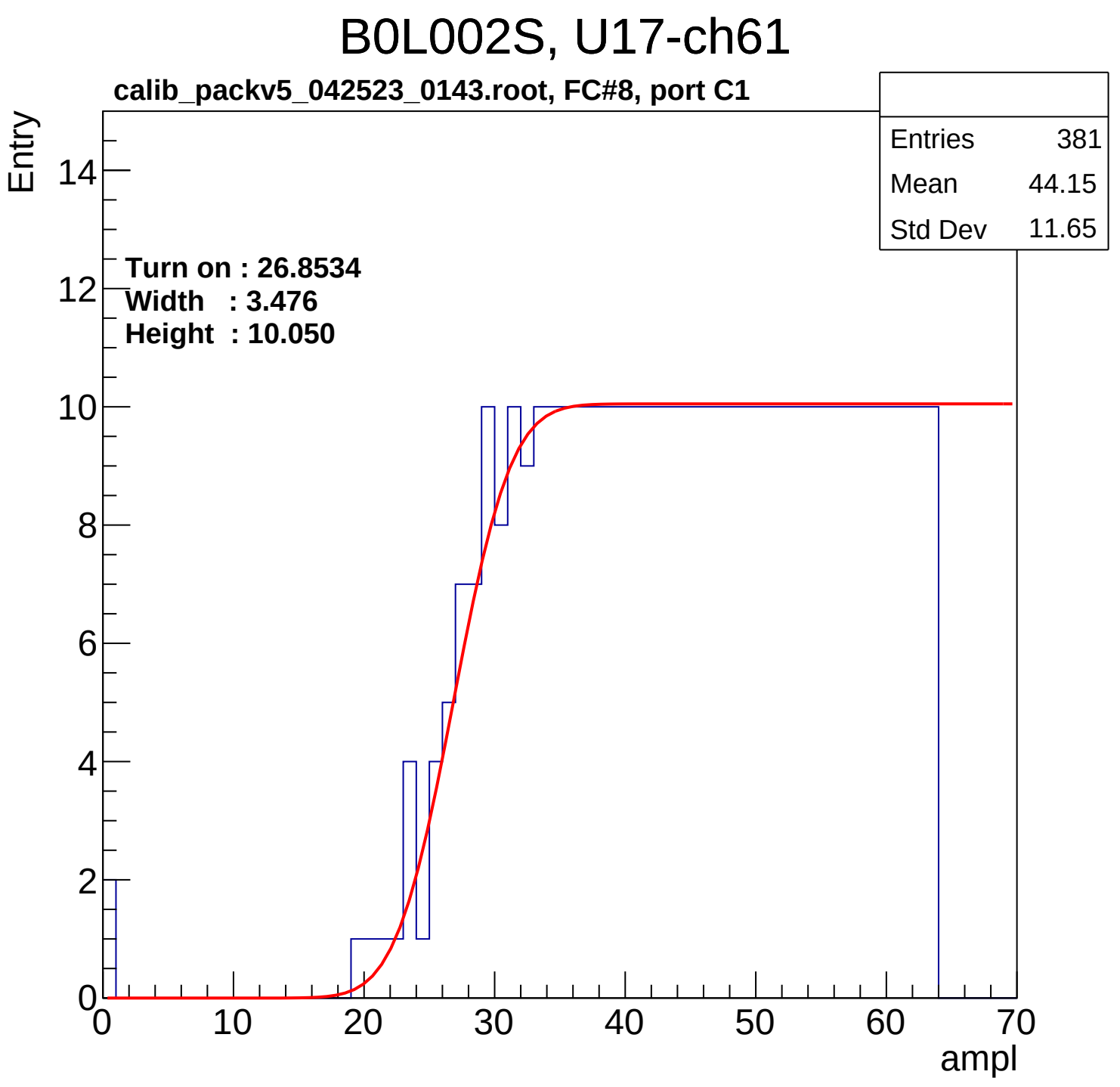
B0L002S, U17-ch61
calib_packv5_042523_0143.root, FC#8, port C1
Entries 381
Mean 44.15
Std Dev 11.65
Turn on : 26.8534
Width : 3.476
Height : 10.050
Entry
ampl
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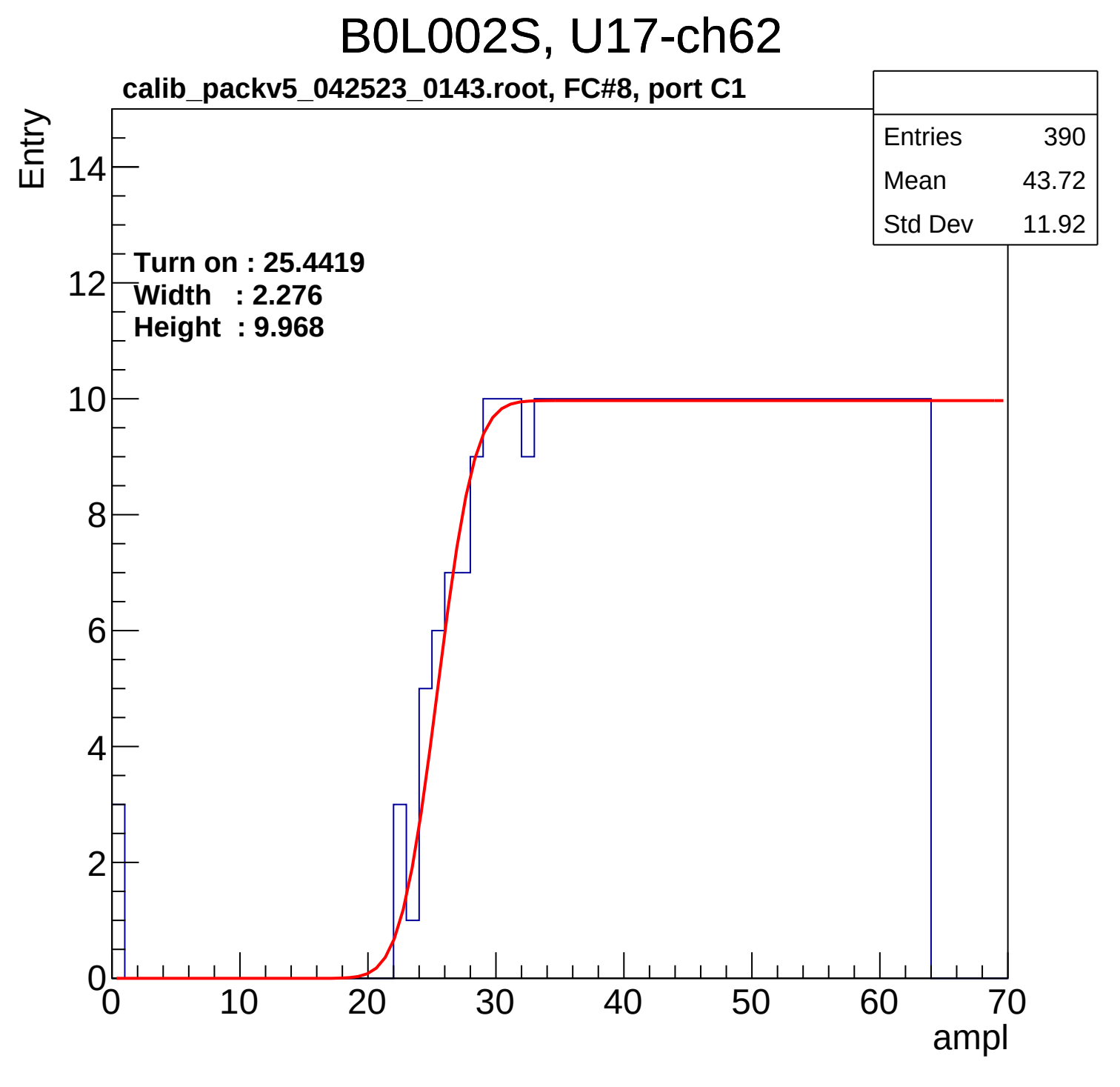
B0L002S, U17-ch62
calib_packv5_042523_0143.root, FC#8, port C1
Entries 390
Mean 43.72
Std Dev 11.92
Turn on : 25.4419
Width : 2.276
Height : 9.968
Entry
ampl
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2
4
6
8
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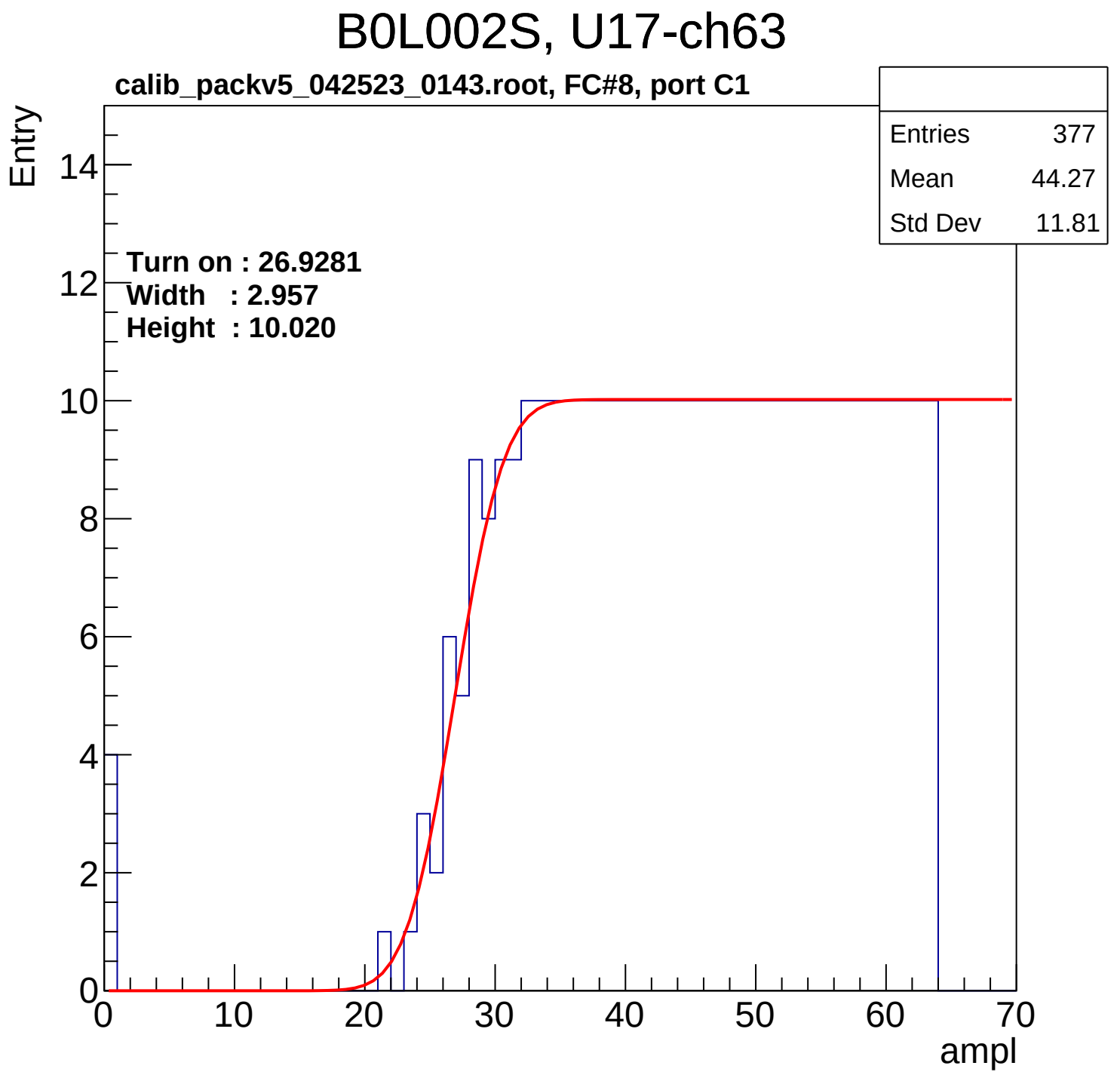
B0L002S, U17-ch63
calib_packv5_042523_0143.root, FC#8, port C1
Entries 377
Mean 44.27
Std Dev 11.81
Turn on : 26.9281
Width : 2.957
Height : 10.020
Entry
ampl
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4
6
8
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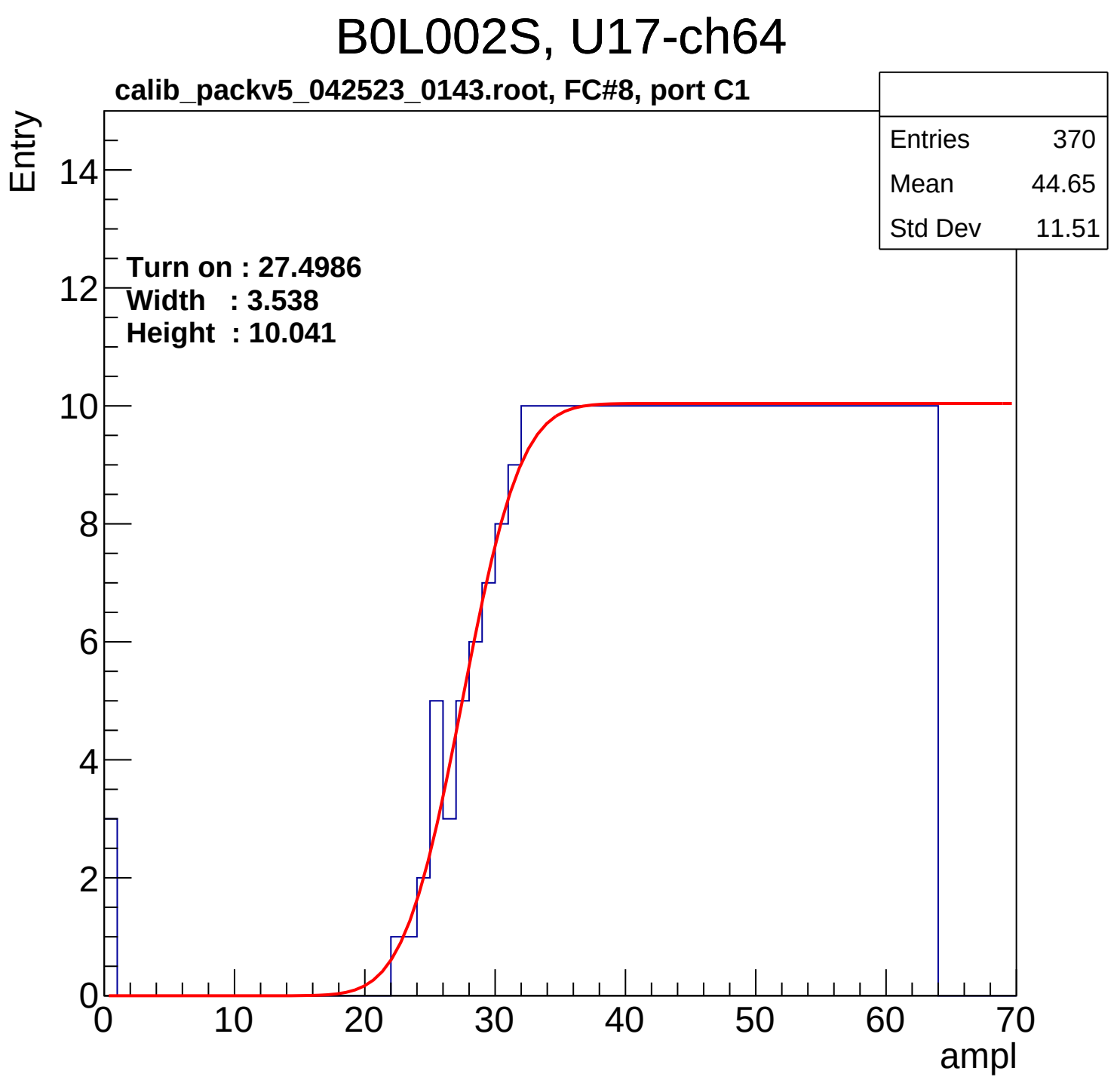
B0L002S, U17-ch64
calib_packv5_042523_0143.root, FC#8, port C1
Entries 370
Mean 44.65
Std Dev 11.51
Turn on : 27.4986
Width : 3.538
Height : 10.041
Entry
ampl
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2
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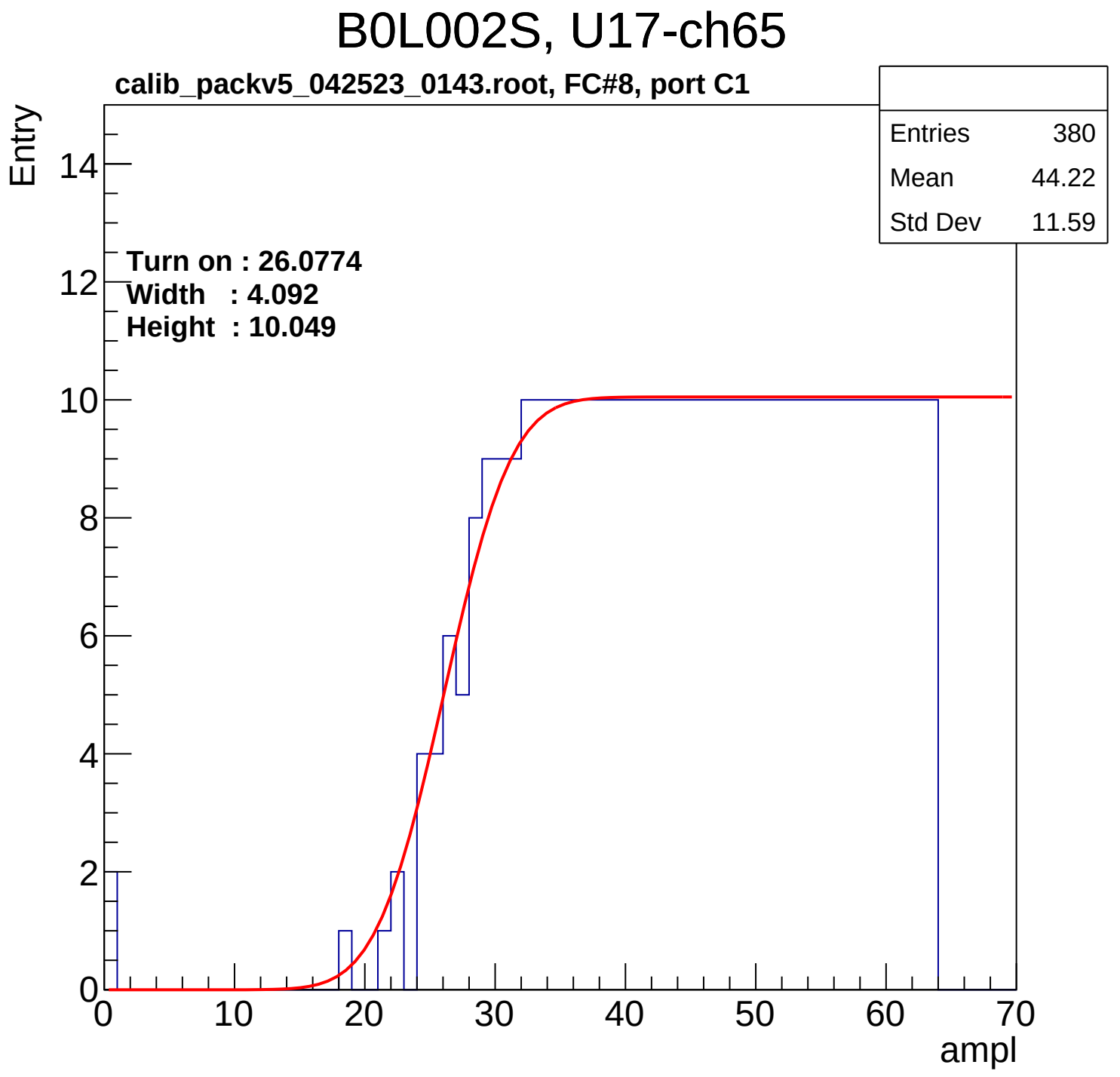
B0L002S, U17-ch65
calib_packv5_042523_0143.root, FC#8, port C1
Entries 380
Mean 44.22
Std Dev 11.59
Turn on : 26.0774
Width : 4.092
Height : 10.049
Entry
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2
4
6
8
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12
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60
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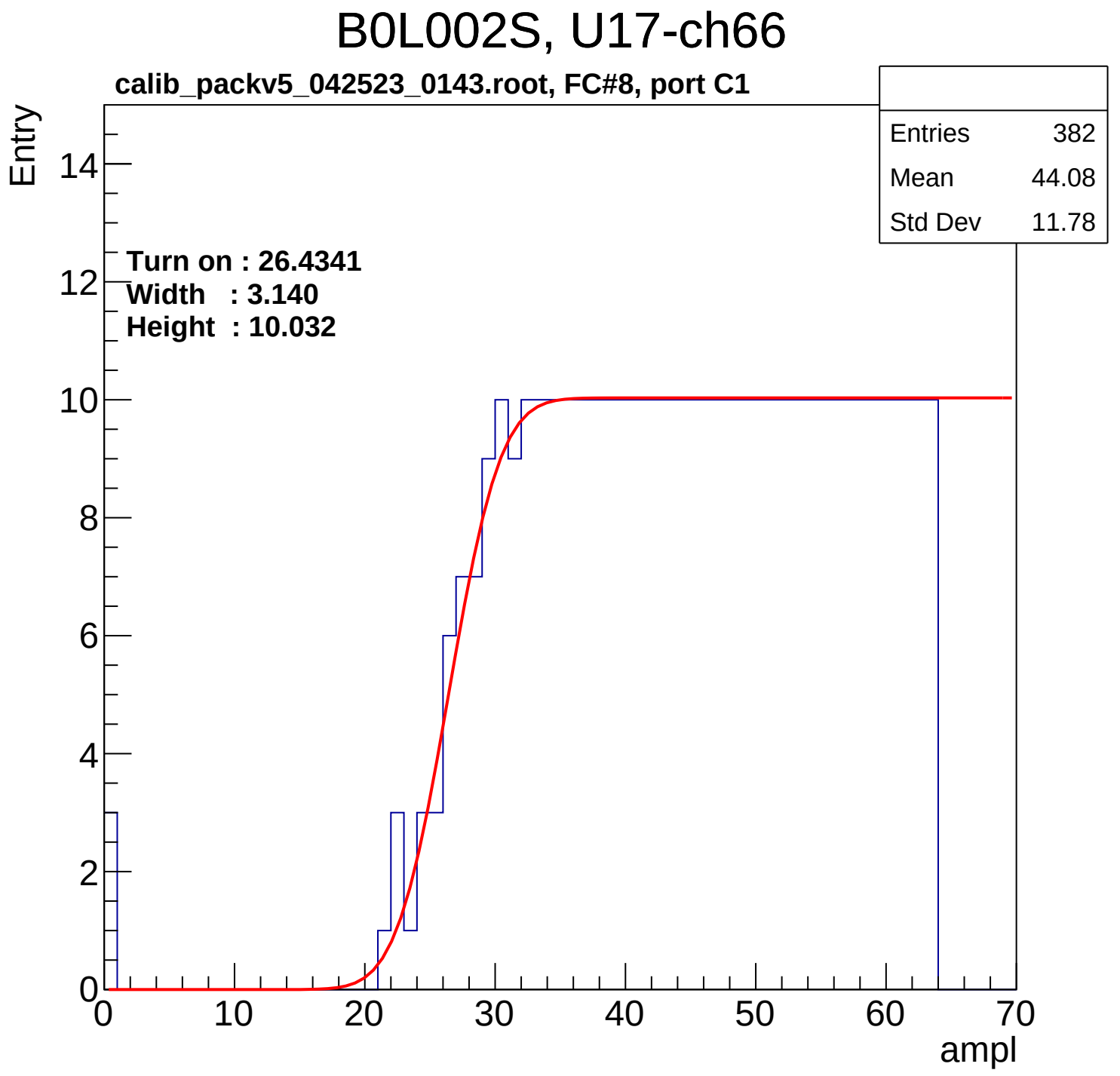
B0L002S, U17-ch66
calib_packv5_042523_0143.root, FC#8, port C1
Entries 382
Mean 44.08
Std Dev 11.78
Turn on : 26.4341
Width : 3.140
Height : 10.032
Entry
ampl
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6
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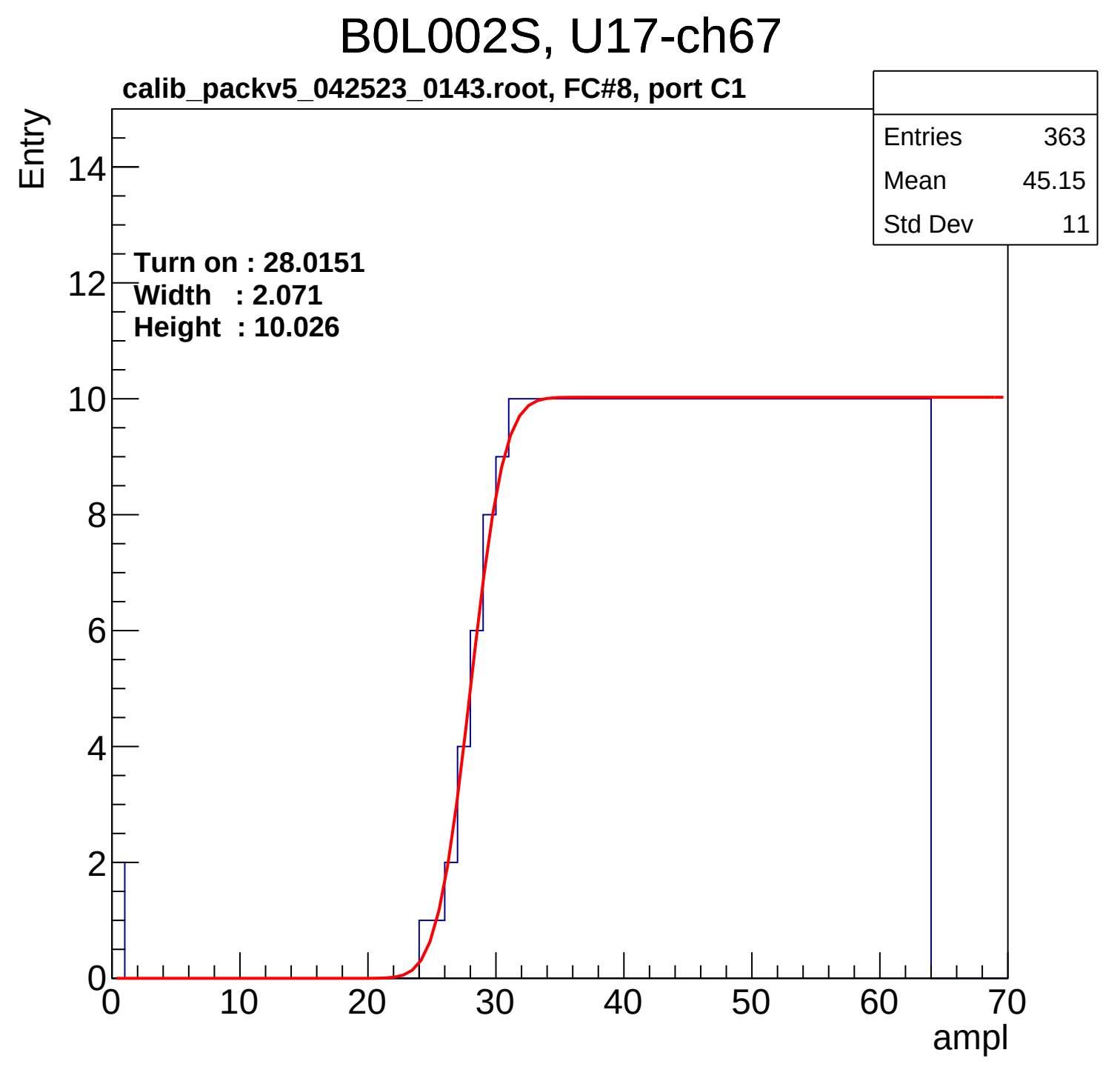
B0L002S, U17-ch67
calib_packv5_042523_0143.root, FC#8, port C1
Entries 363
Mean 45.15
Std Dev 11
Turn on : 28.0151
Width : 2.071
Height : 10.026
Entry
ampl
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6
8
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20
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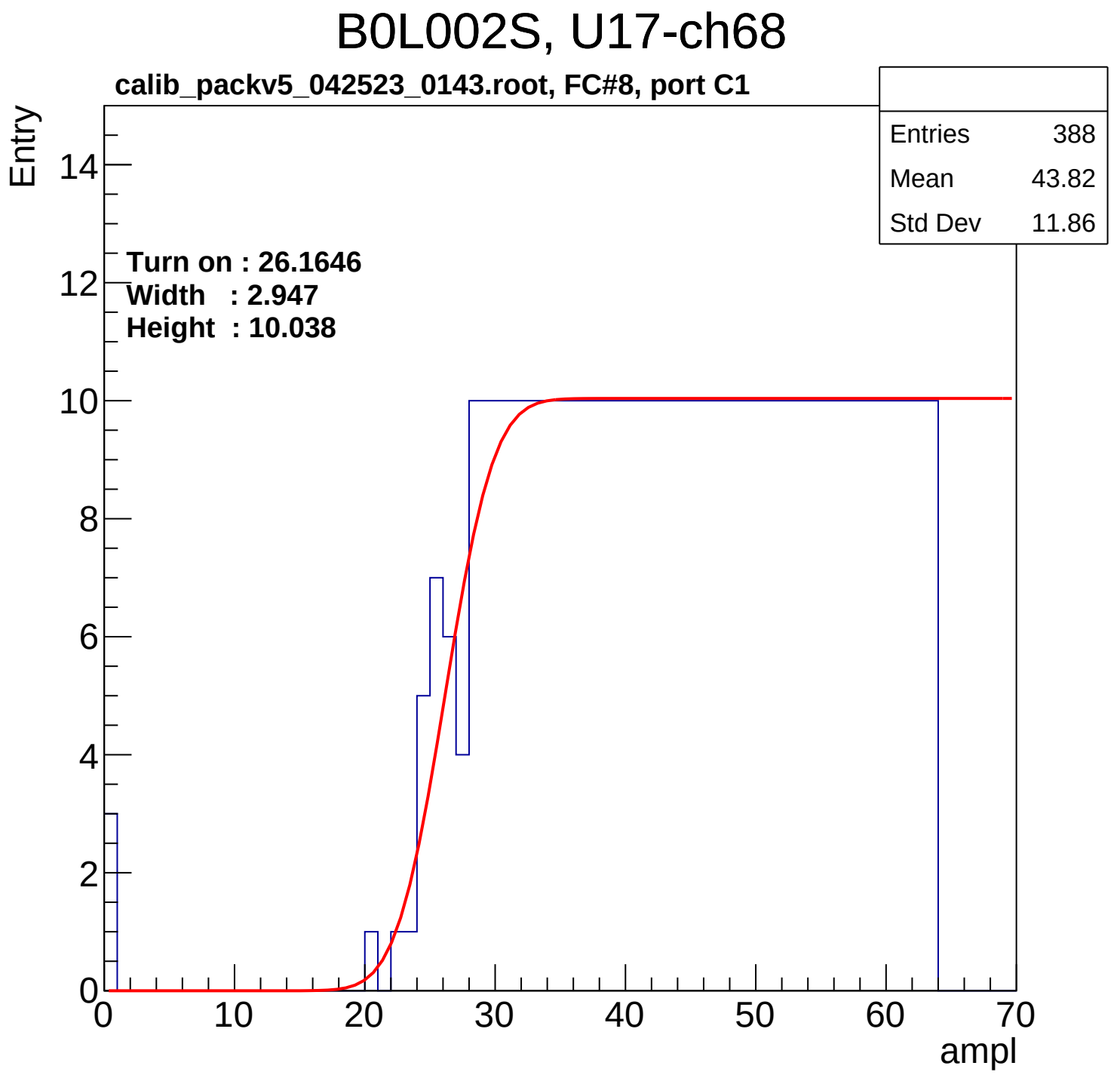
B0L002S, U17-ch68
calib_packv5_042523_0143.root, FC#8, port C1
Entries 388
Mean 43.82
Std Dev 11.86
Turn on : 26.1646
Width : 2.947
Height : 10.038
Entry
ampl
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6
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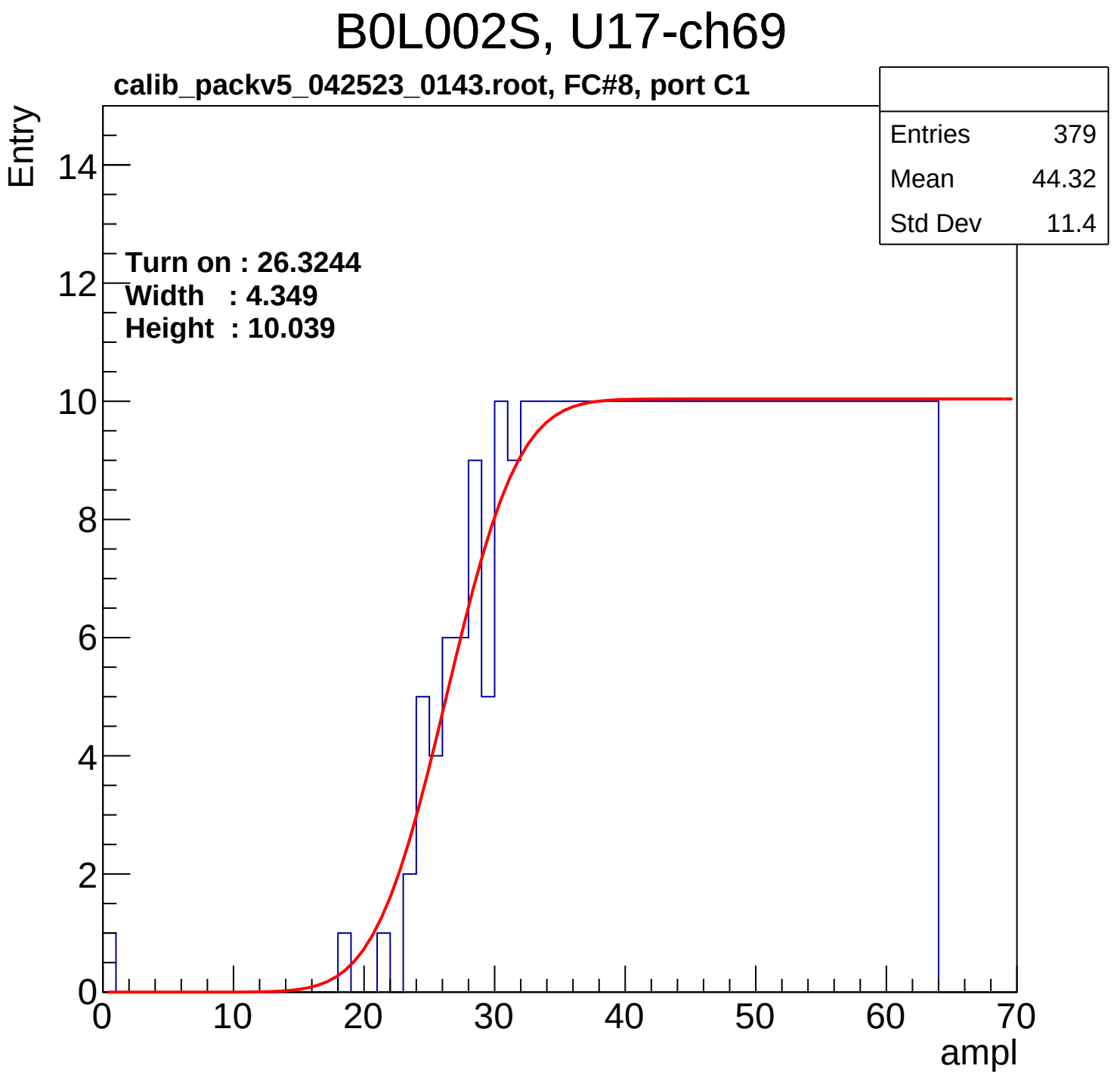
B0L002S, U17-ch69
calib_packv5_042523_0143.root, FC#8, port C1
Entries 379
Mean 44.32
Std Dev 11.4
Turn on : 26.3244
Width : 4.349
Height : 10.039
Entry
ampl
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4
6
8
10
12
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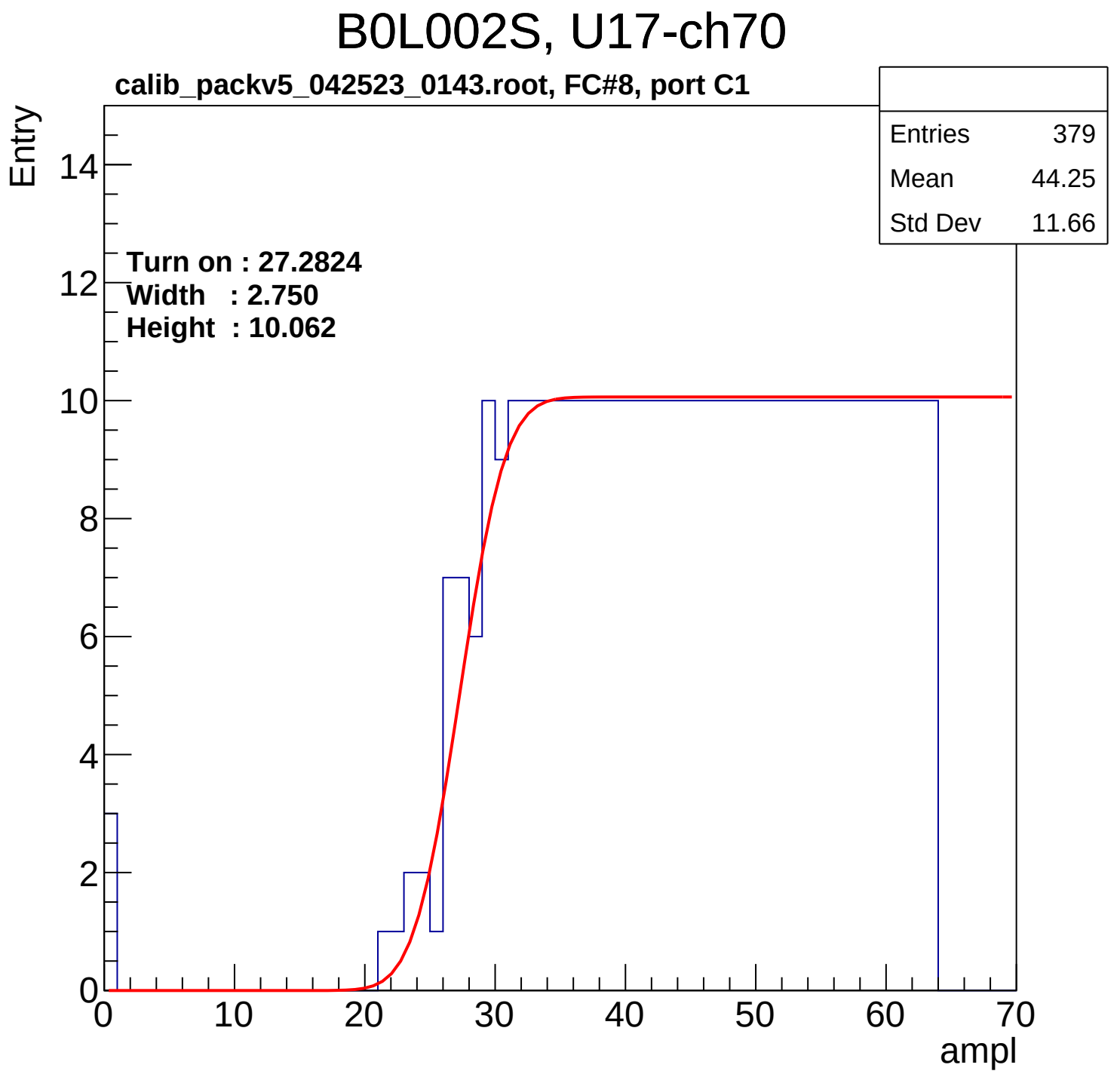
B0L002S, U17-ch70
calib_packv5_042523_0143.root, FC#8, port C1
Entries 379
Mean 44.25
Std Dev 11.66
Turn on : 27.2824
Width : 2.750
Height : 10.062
Entry
ampl
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6
8
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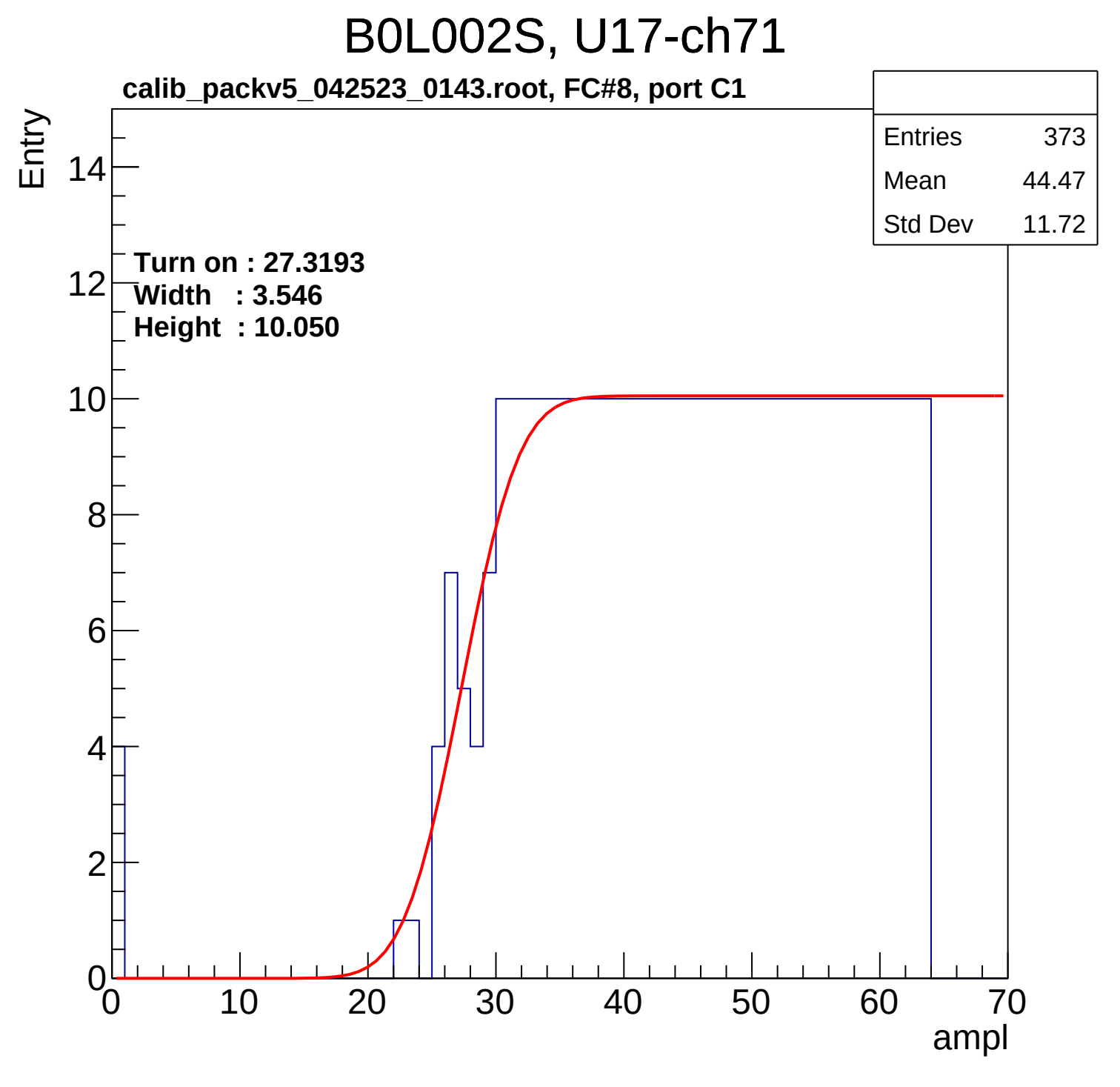
B0L002S, U17-ch71
calib_packv5_042523_0143.root, FC#8, port C1
Entries 373
Mean 44.47
Std Dev 11.72
Turn on : 27.3193
Width : 3.546
Height : 10.050
Entry
ampl
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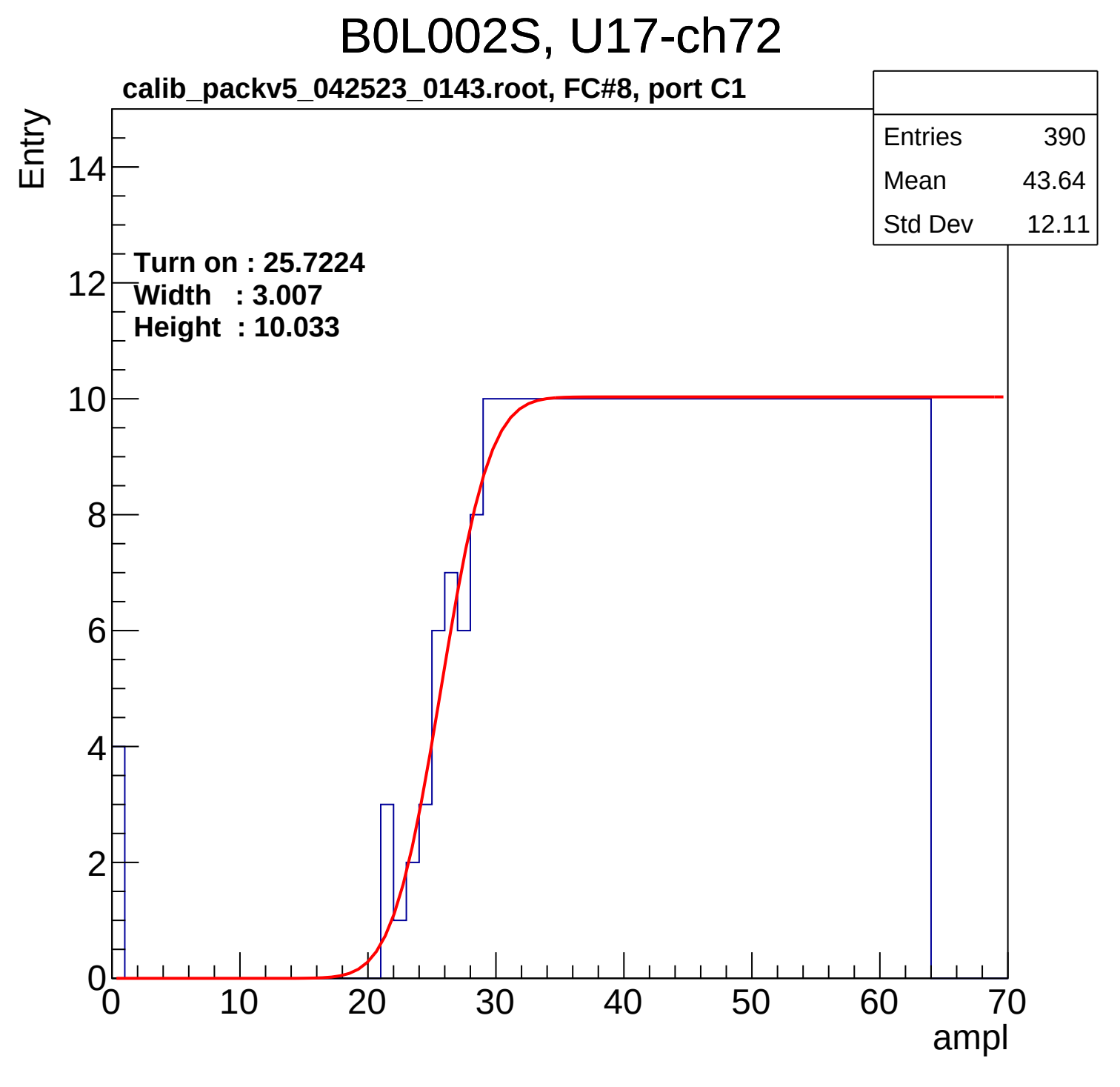
B0L002S, U17-ch72
calib_packv5_042523_0143.root, FC#8, port C1
Entries 390
Mean 43.64
Std Dev 12.11
Turn on : 25.7224
Width : 3.007
Height : 10.033
Entry
ampl
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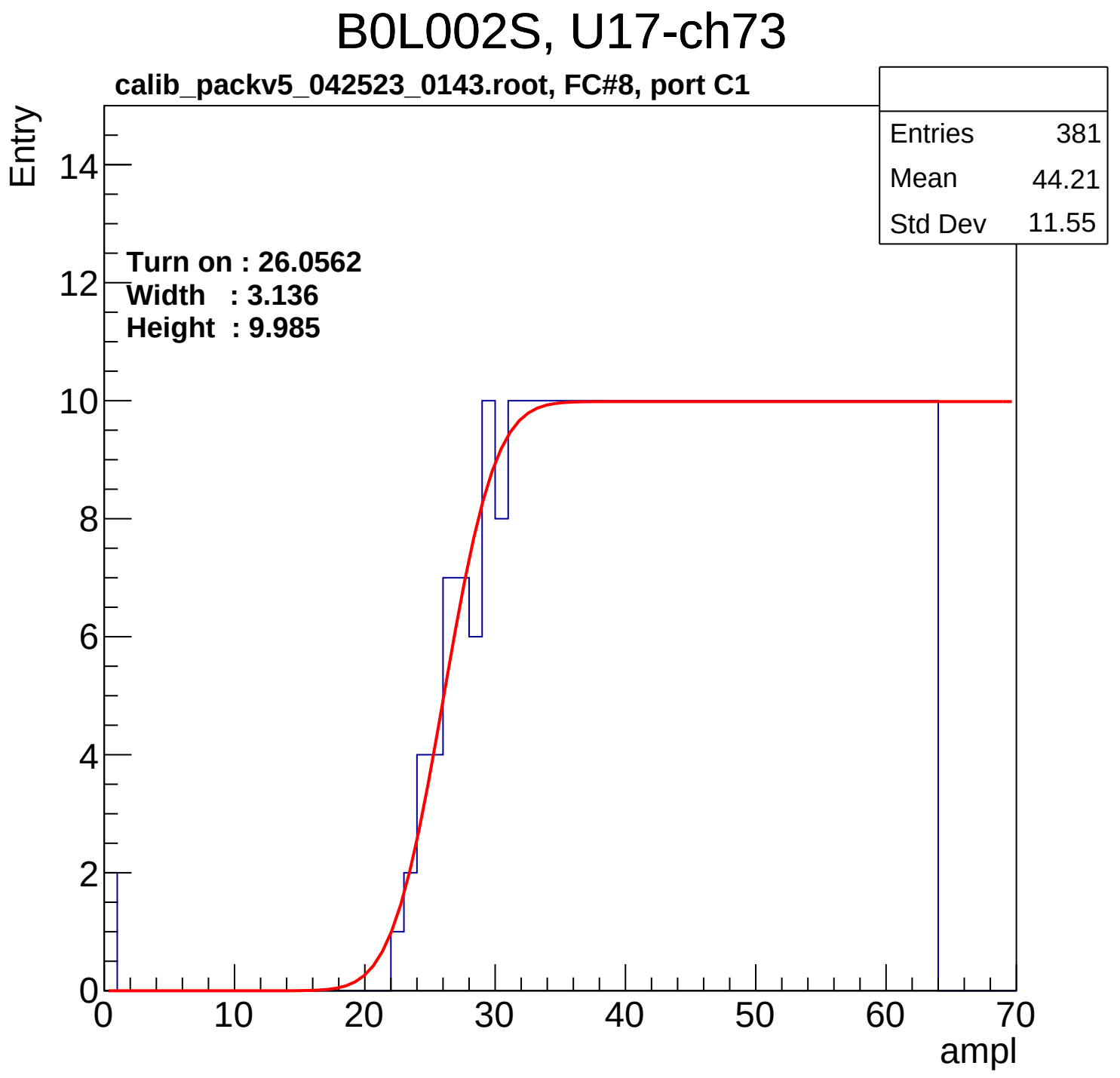
B0L002S, U17-ch73
calib_packv5_042523_0143.root, FC#8, port C1
Entries 381
Mean 44.21
Std Dev 11.55
Turn on : 26.0562
Width : 3.136
Height : 9.985
Entry
ampl
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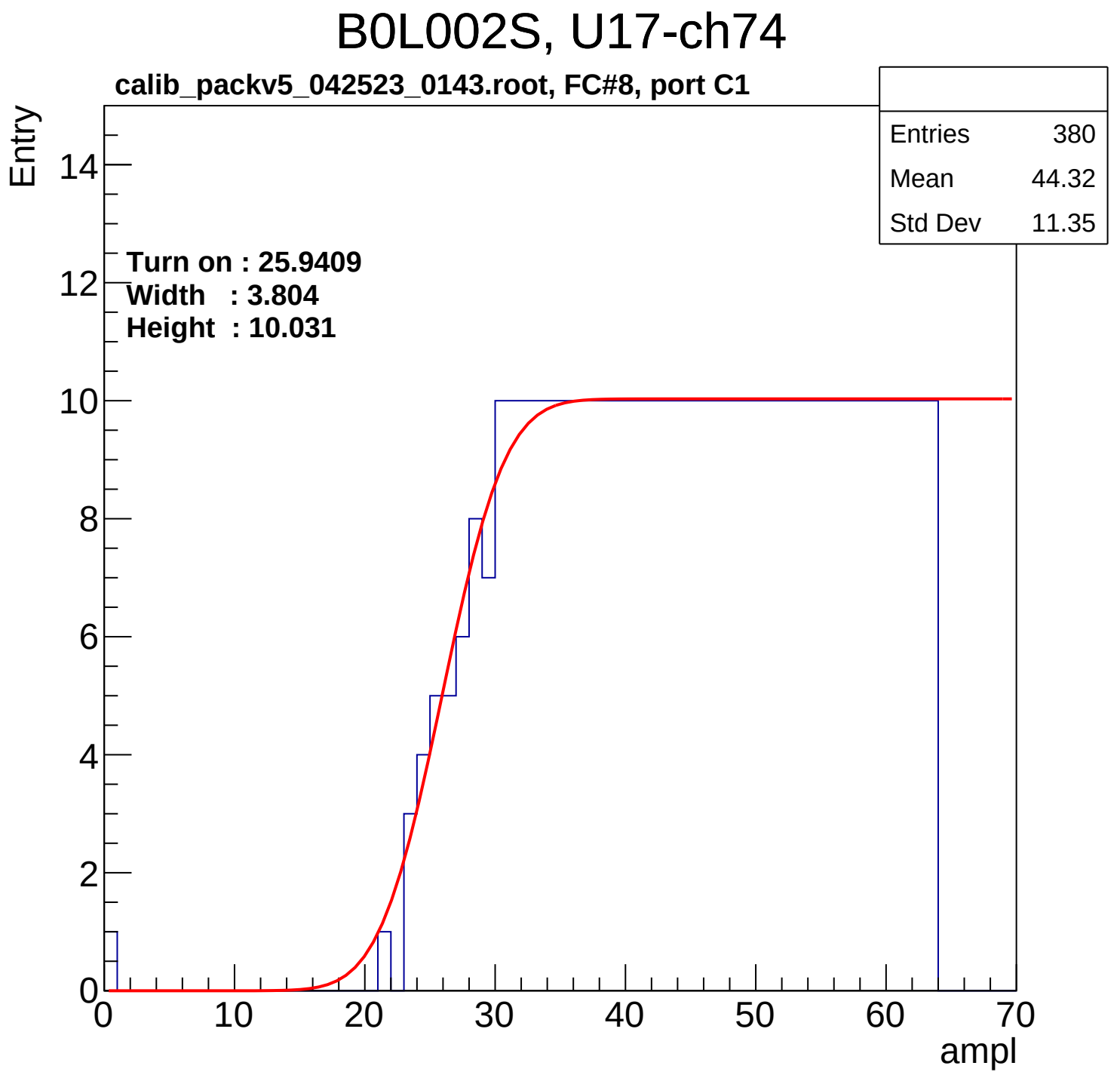
B0L002S, U17-ch74
calib_packv5_042523_0143.root, FC#8, port C1
Entries 380
Mean 44.32
Std Dev 11.35
Turn on : 25.9409
Width : 3.804
Height : 10.031
Entry
ampl
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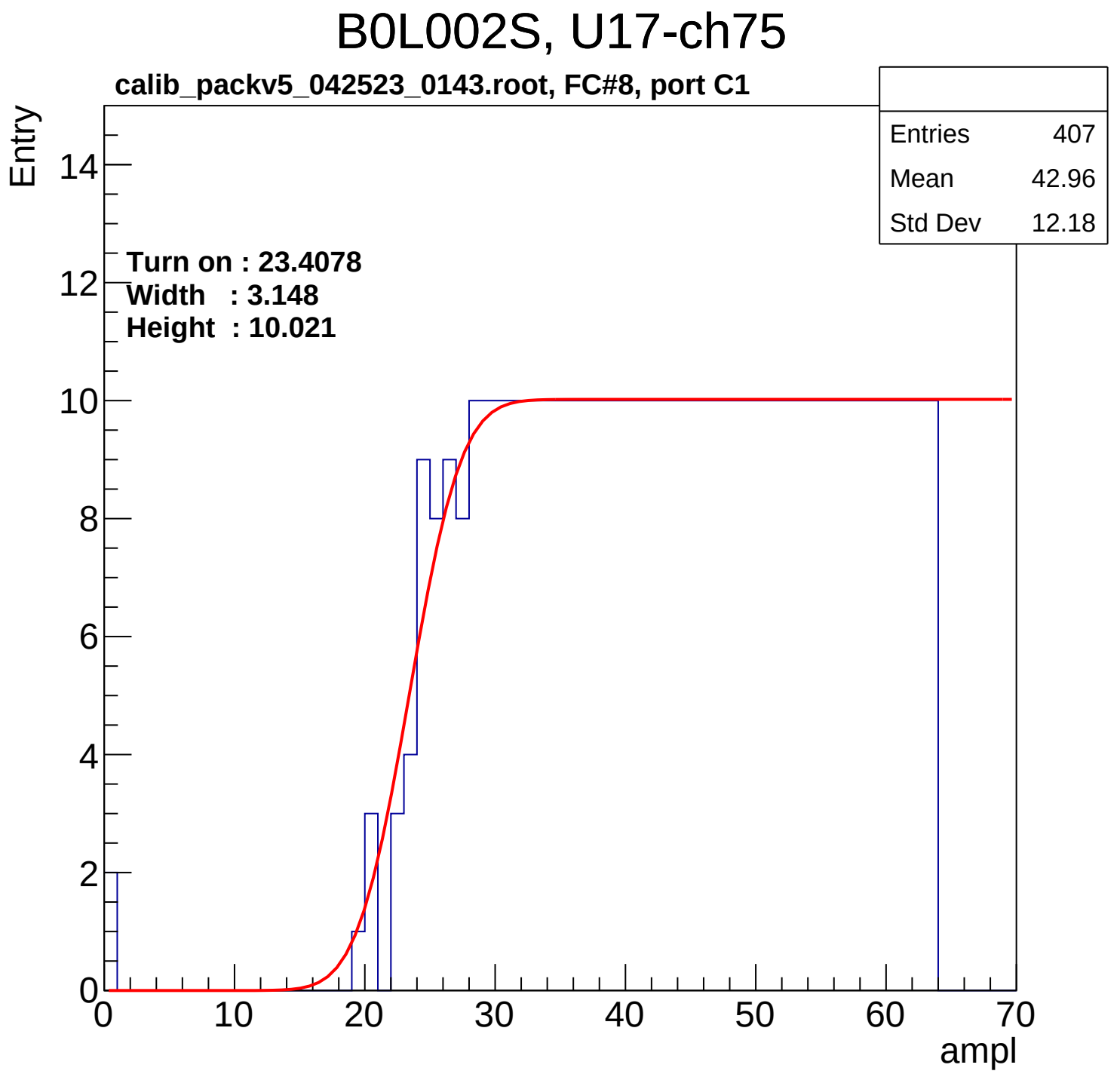
B0L002S, U17-ch75
calib_packv5_042523_0143.root, FC#8, port C1
Entries 407
Mean 42.96
Std Dev 12.18
Turn on : 23.4078
Width : 3.148
Height : 10.021
Entry
ampl
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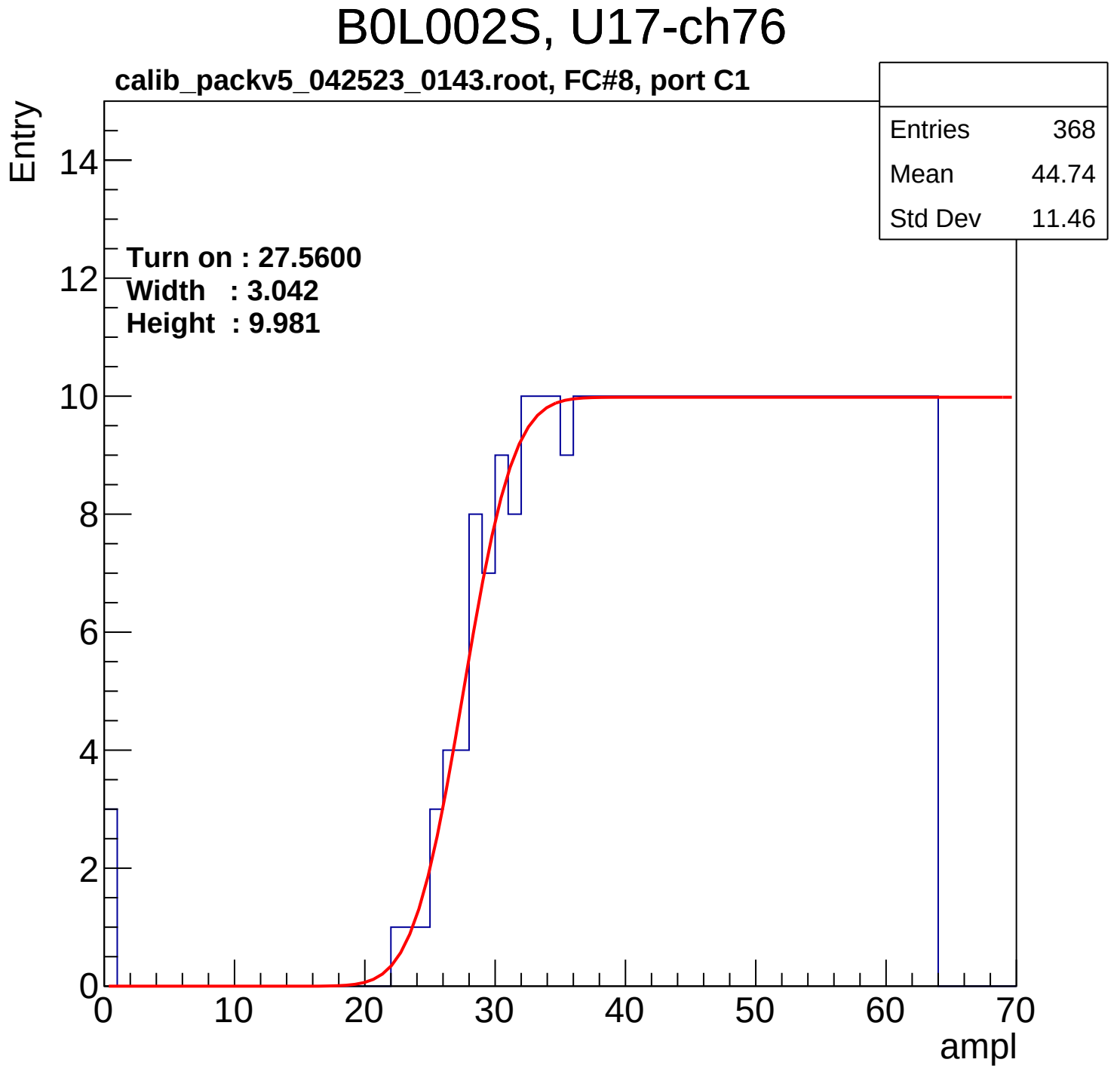
B0L002S, U17-ch76
calib_packv5_042523_0143.root, FC#8, port C1
Entries 368
Mean 44.74
Std Dev 11.46
Turn on : 27.5600
Width : 3.042
Height : 9.981
Entry
ampl
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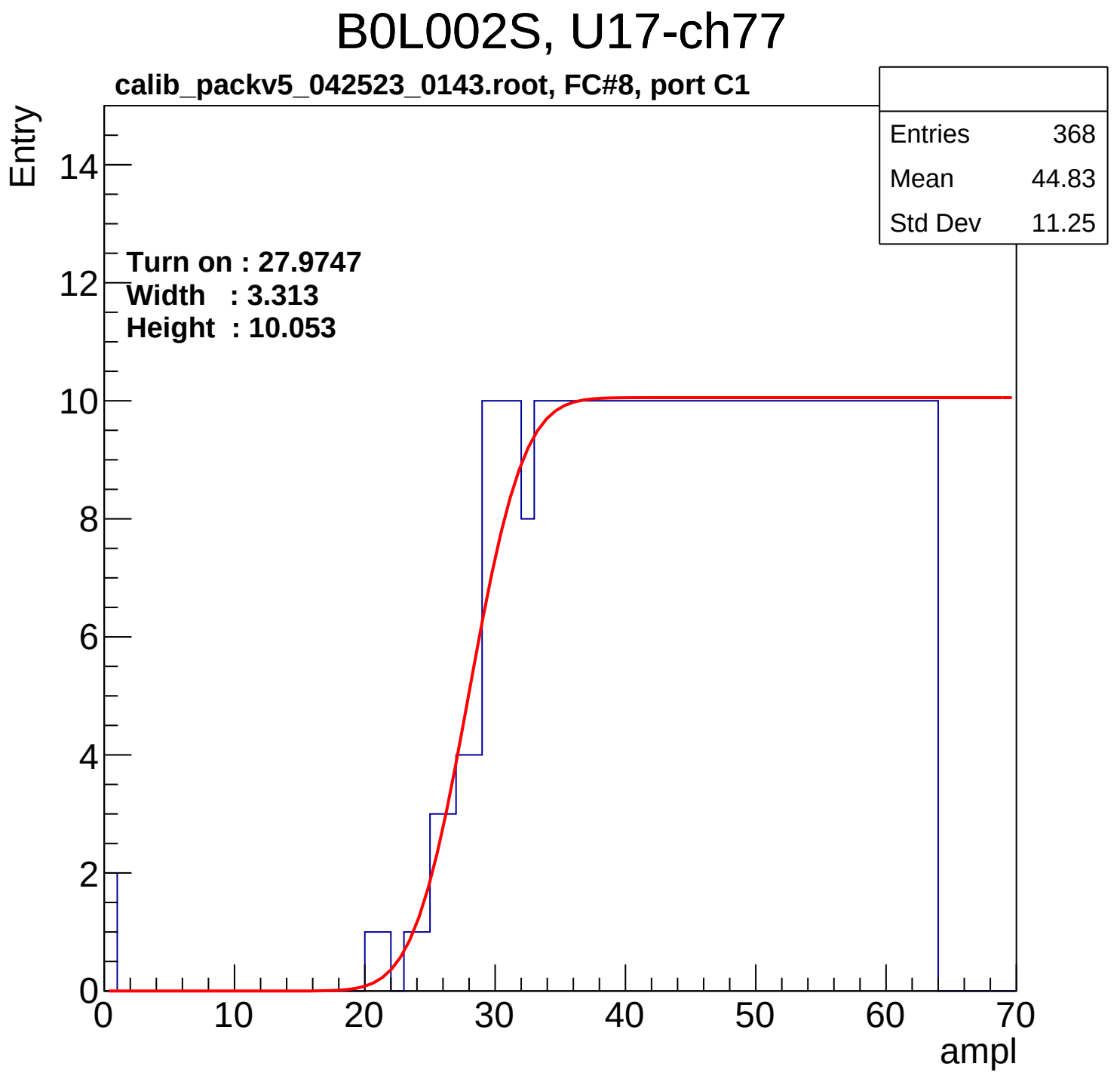
B0L002S, U17-ch77
calib_packv5_042523_0143.root, FC#8, port C1
Entries 368
Mean 44.83
Std Dev 11.25
Turn on : 27.9747
Width : 3.313
Height : 10.053
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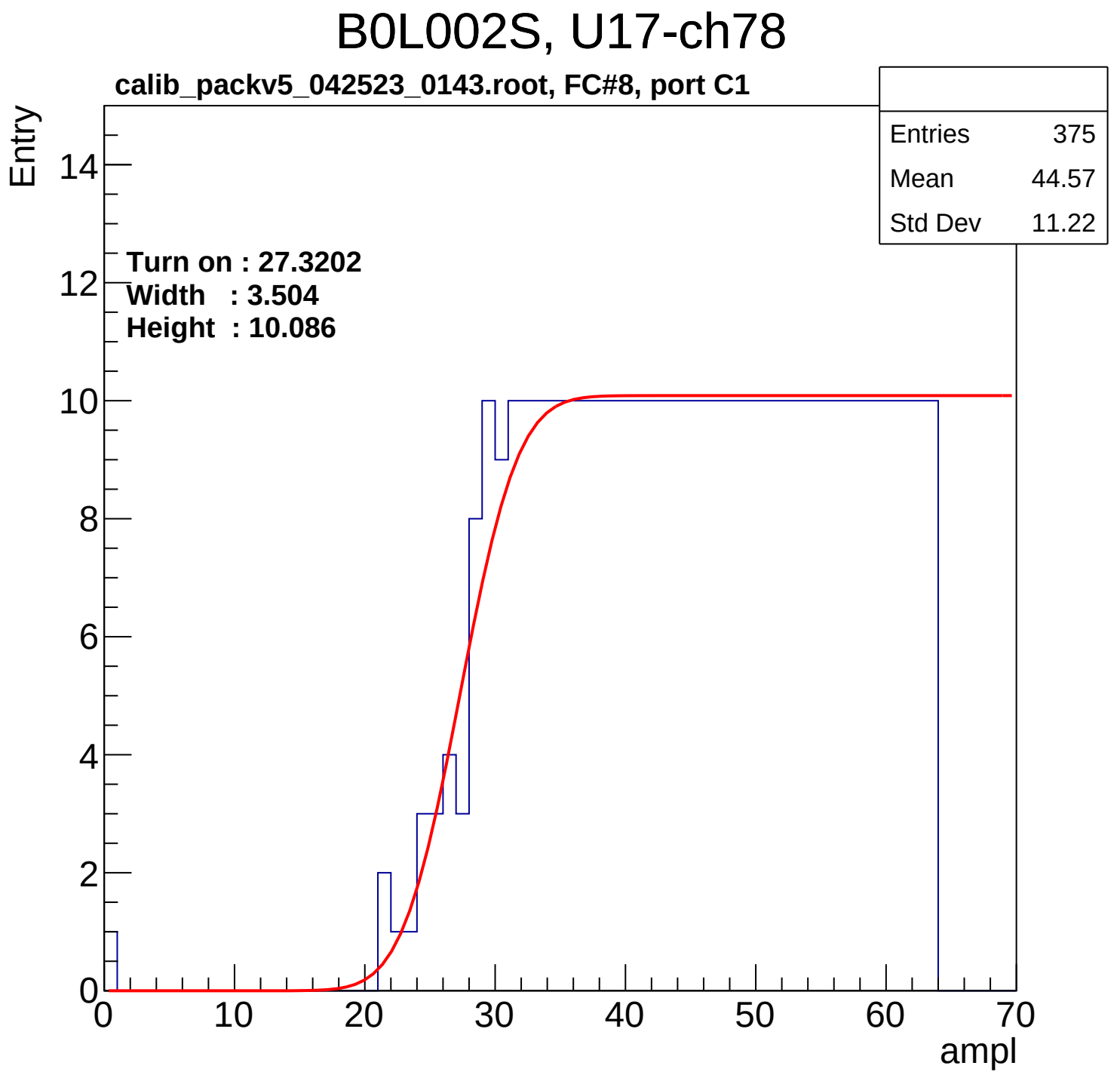
B0L002S, U17-ch78
calib_packv5_042523_0143.root, FC#8, port C1
Entries 375
Mean 44.57
Std Dev 11.22
Turn on : 27.3202
Width : 3.504
Height : 10.086
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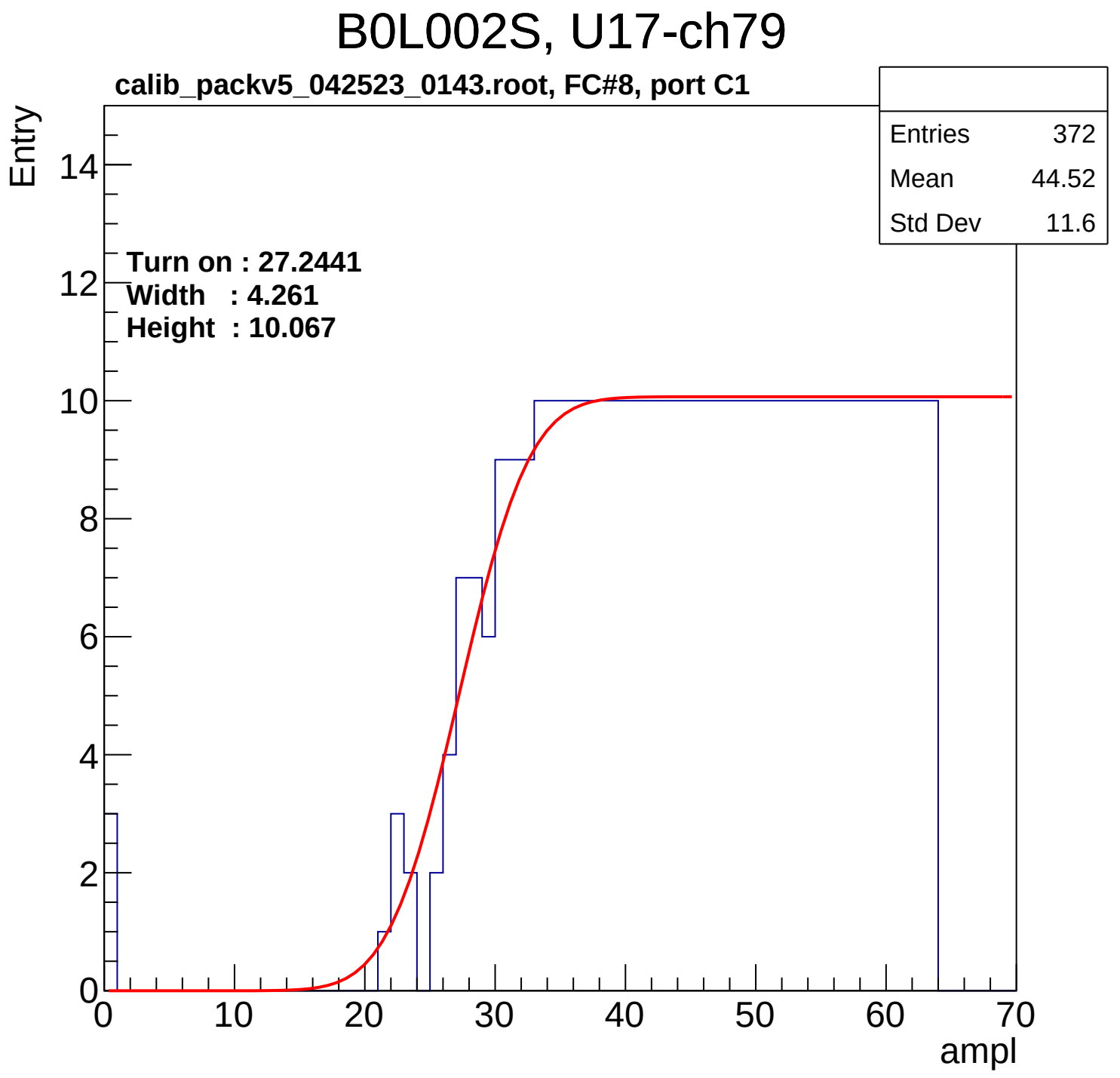
B0L002S, U17-ch79
calib_packv5_042523_0143.root, FC#8, port C1
Entries 372
Mean 44.52
Std Dev 11.6
Turn on : 27.2441
Width : 4.261
Height : 10.067
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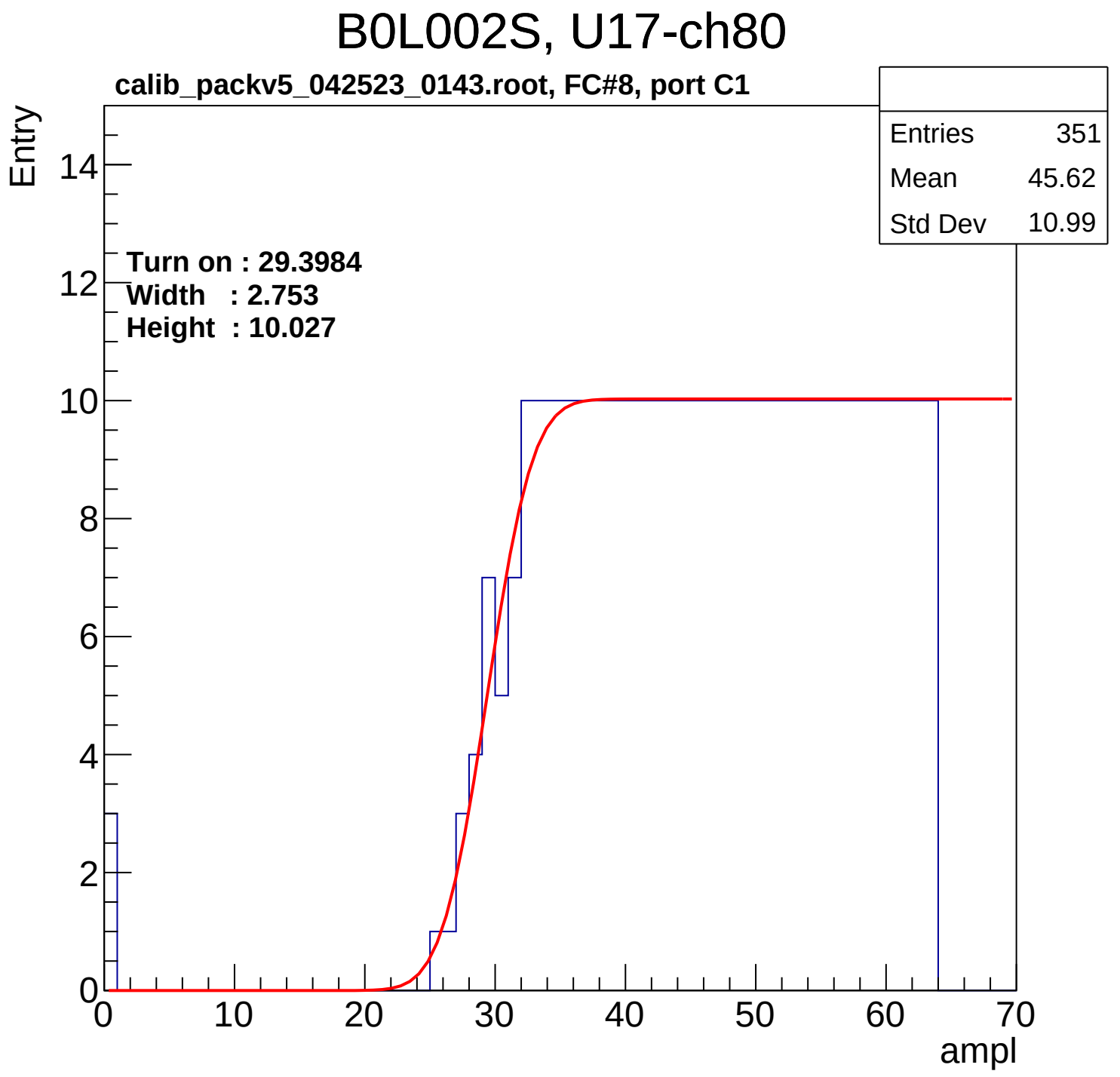
B0L002S, U17-ch80
calib_packv5_042523_0143.root, FC#8, port C1
Entries 351
Mean 45.62
Std Dev 10.99
Turn on : 29.3984
Width : 2.753
Height : 10.027
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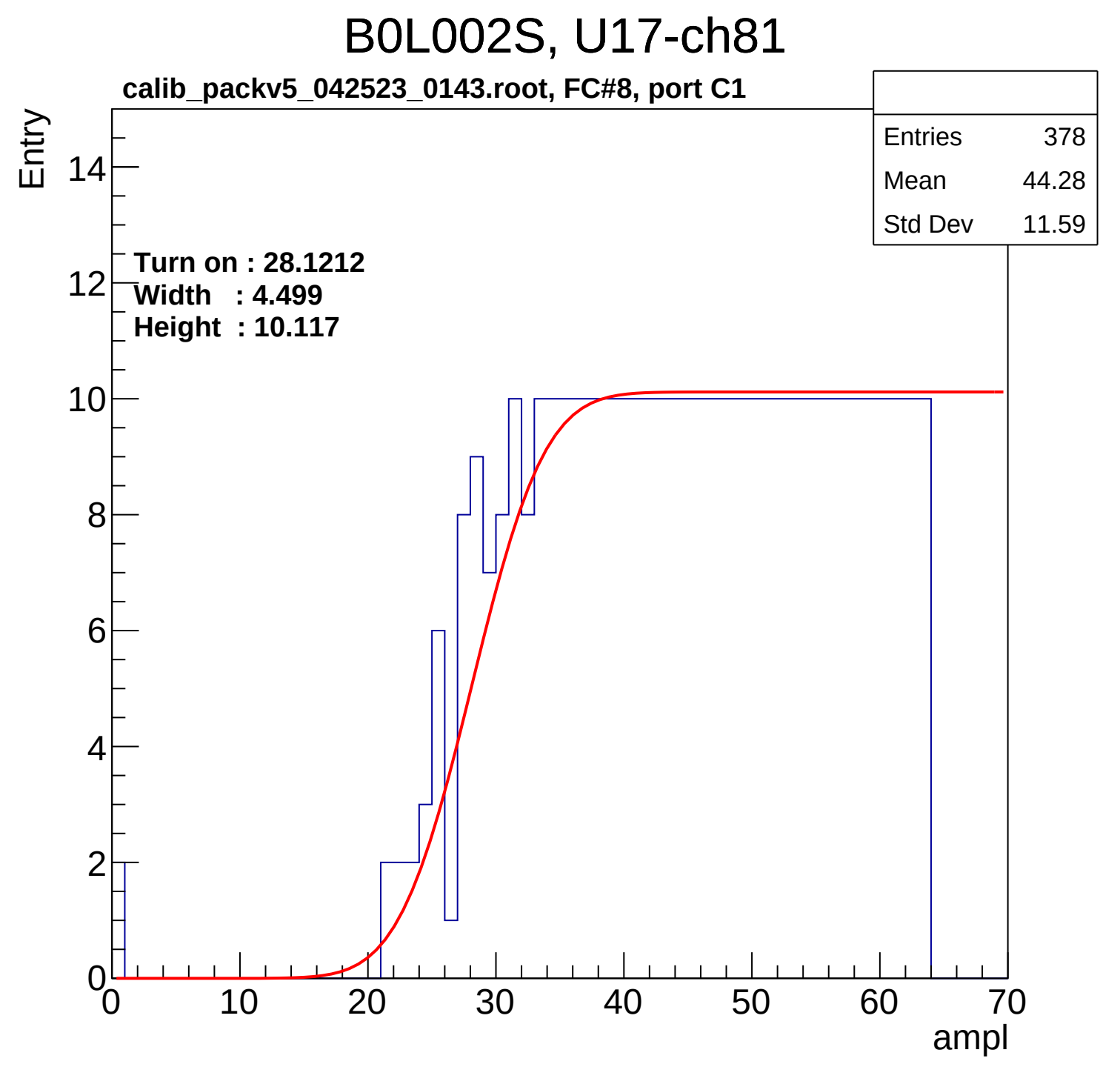
B0L002S, U17-ch81
calib_packv5_042523_0143.root, FC#8, port C1
Entries 378
Mean 44.28
Std Dev 11.59
Turn on : 28.1212
Width : 4.499
Height : 10.117
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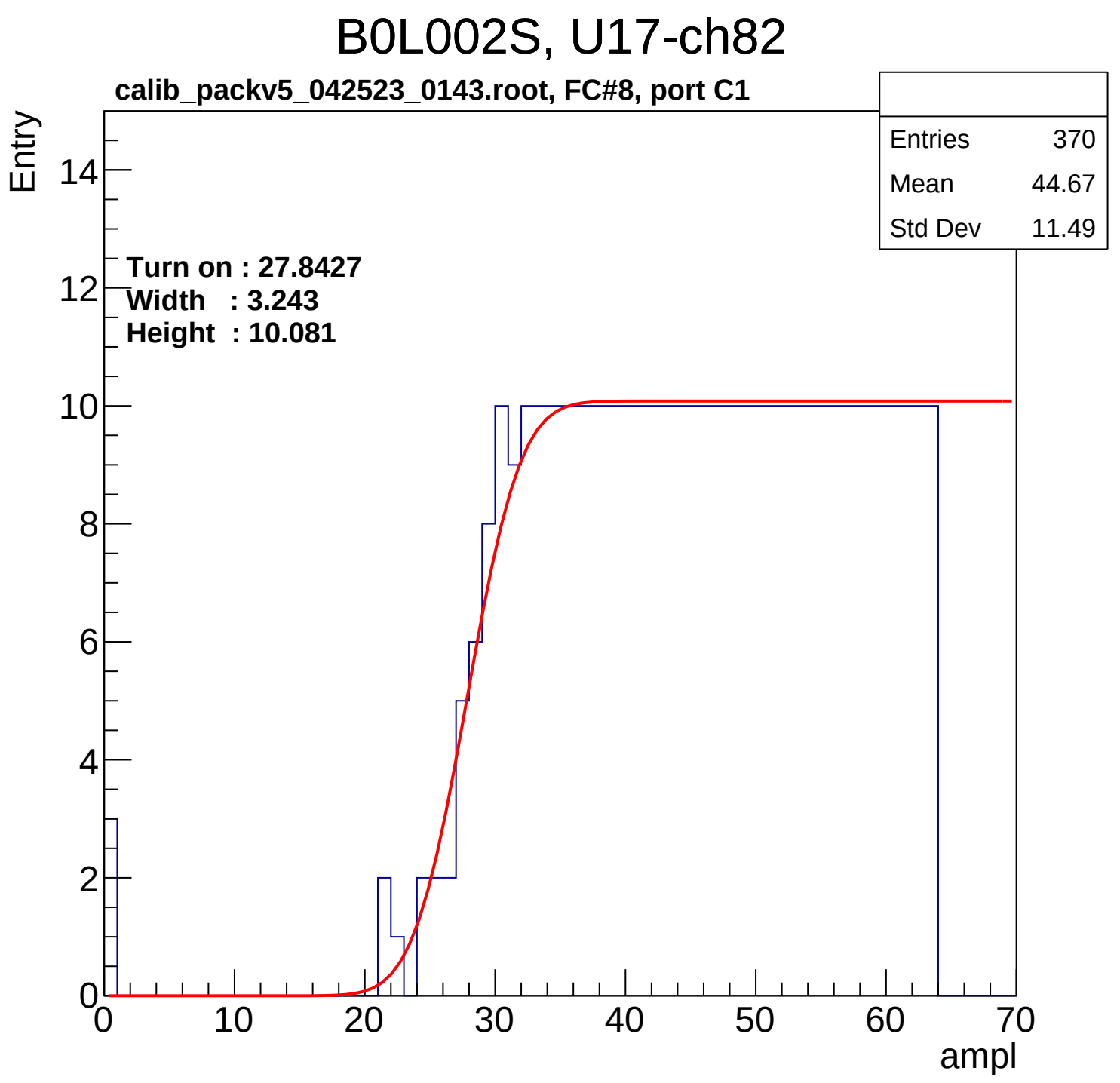
B0L002S, U17-ch82
calib_packv5_042523_0143.root, FC#8, port C1
Entries 370
Mean 44.67
Std Dev 11.49
Turn on : 27.8427
Width : 3.243
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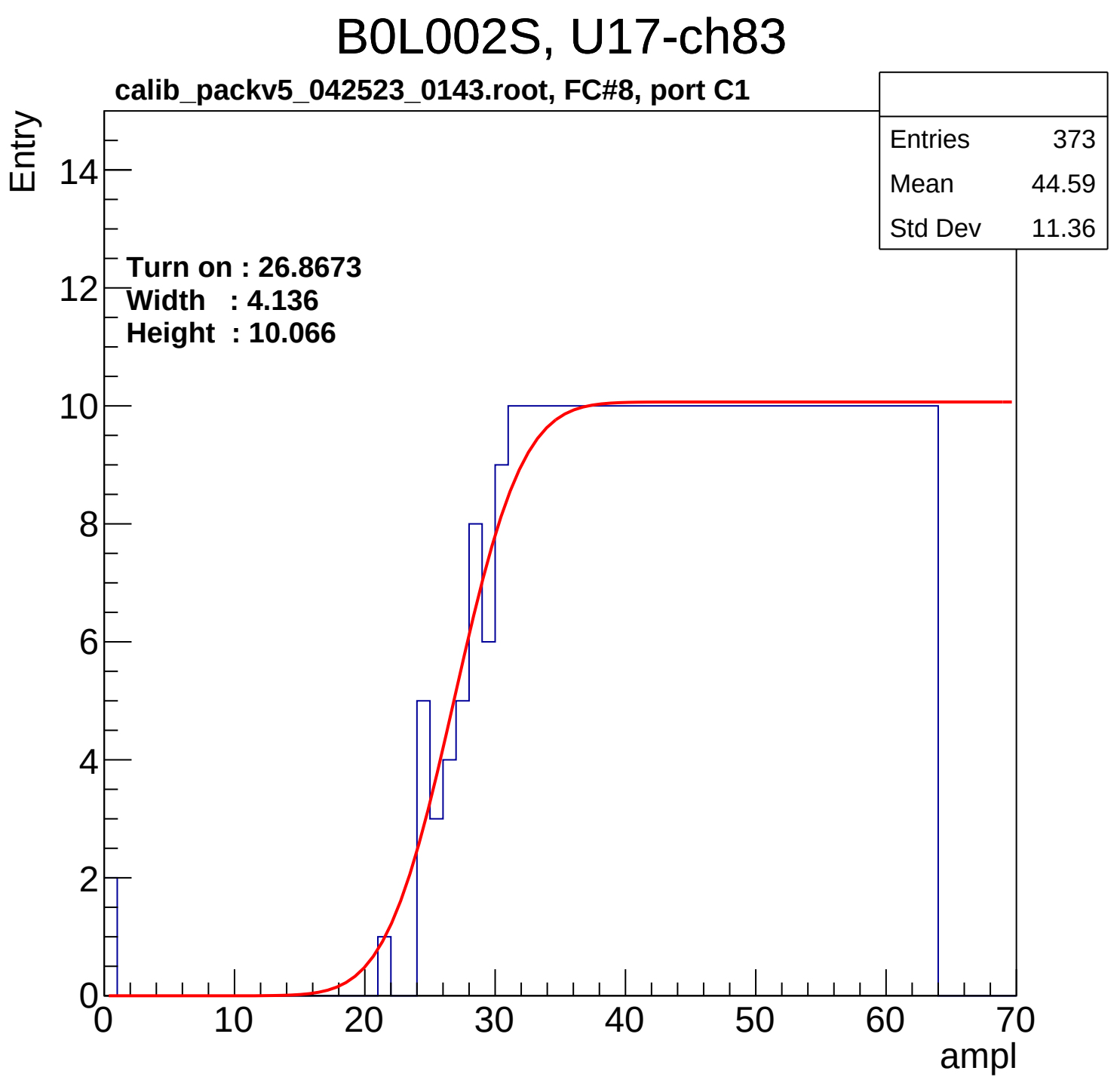
B0L002S, U17-ch83
calib_packv5_042523_0143.root, FC#8, port C1
Entries 373
Mean 44.59
Std Dev 11.36
Turn on : 26.8673
Width : 4.136
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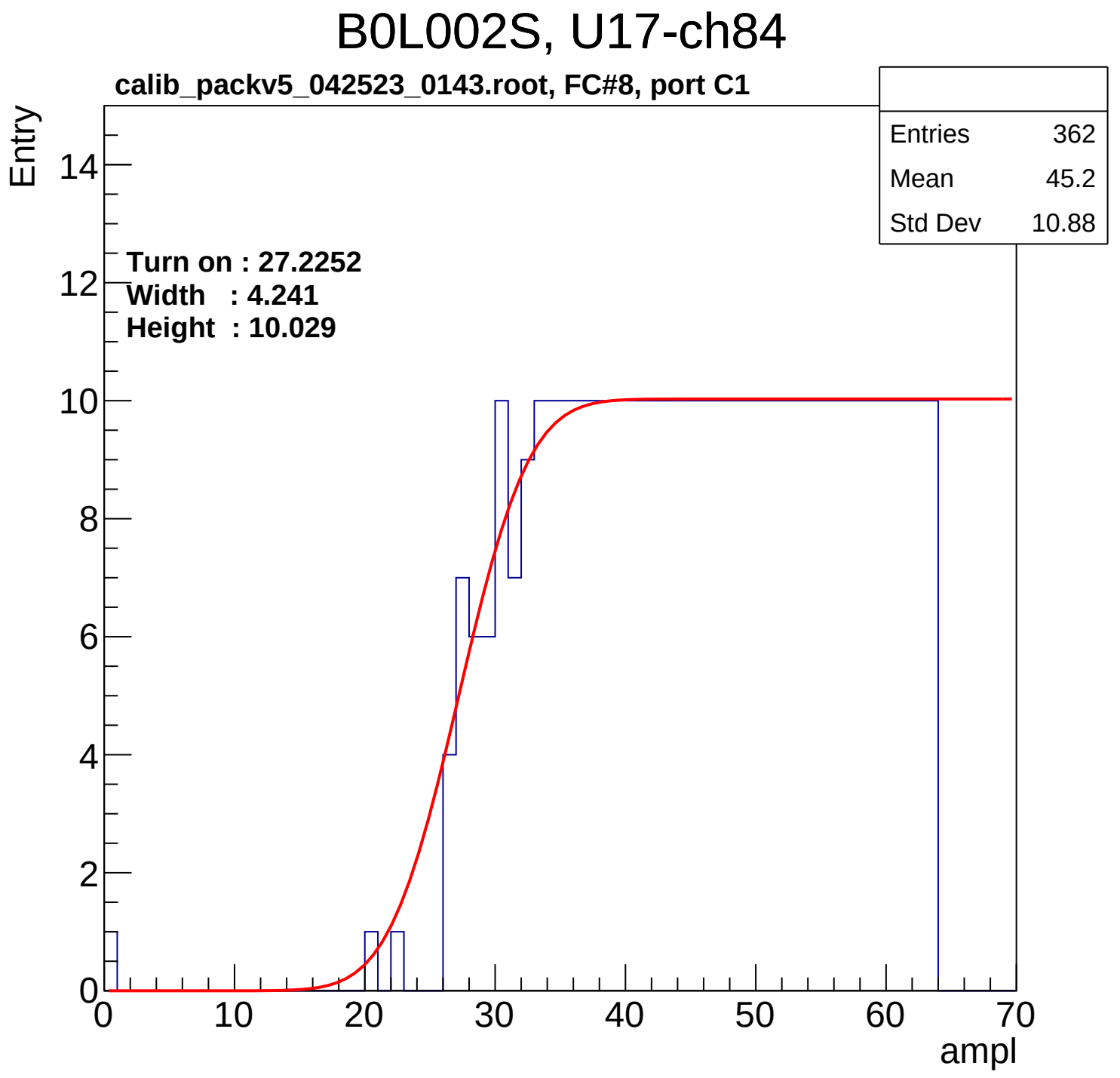
B0L002S, U17-ch84
calib_packv5_042523_0143.root, FC#8, port C1
Entries 362
Mean 45.2
Std Dev 10.88
Turn on : 27.2252
Width : 4.241
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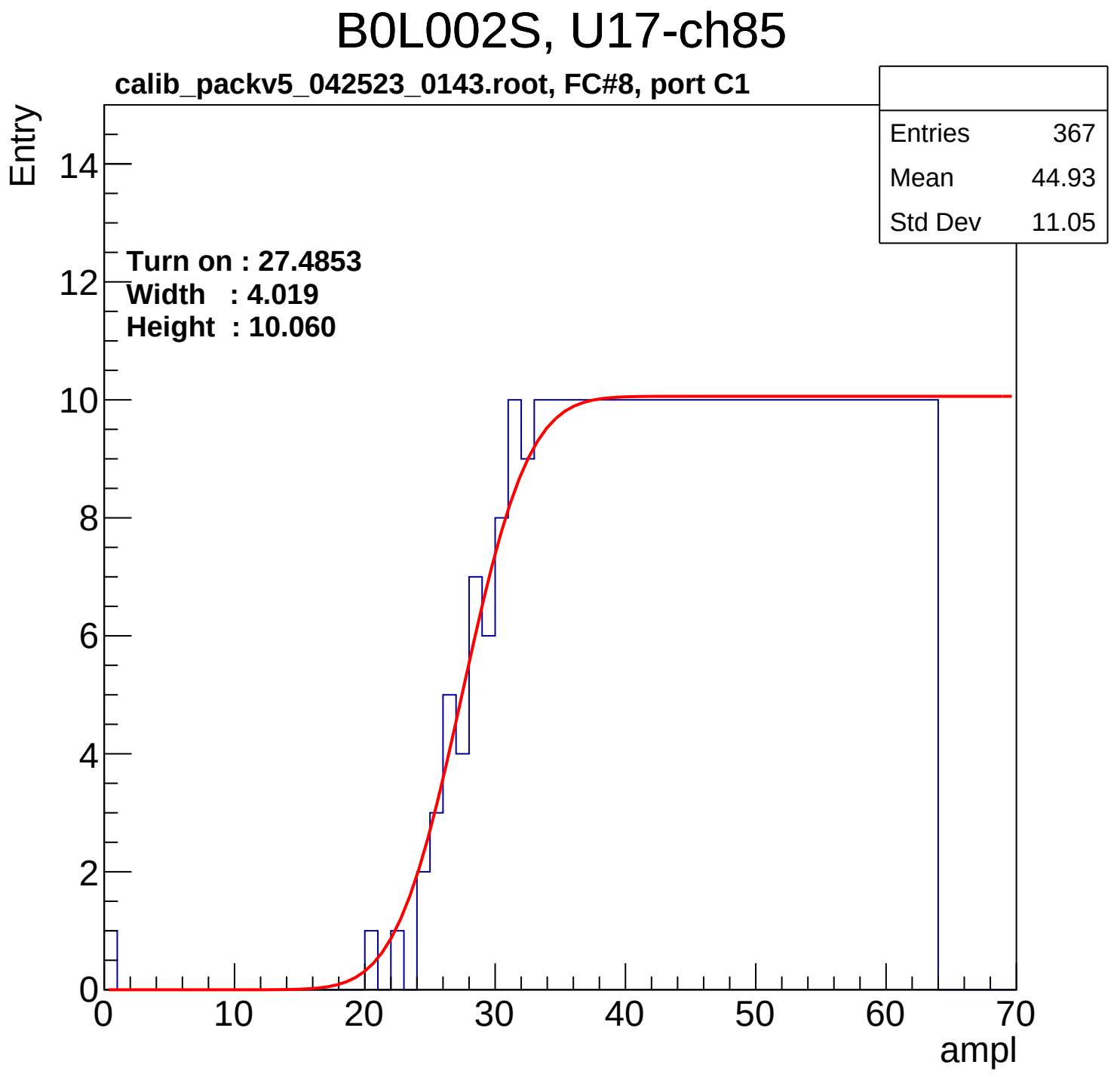
B0L002S, U17-ch85
calib_packv5_042523_0143.root, FC#8, port C1
Entries 367
Mean 44.93
Std Dev 11.05
Turn on : 27.4853
Width : 4.019
Height : 10.060
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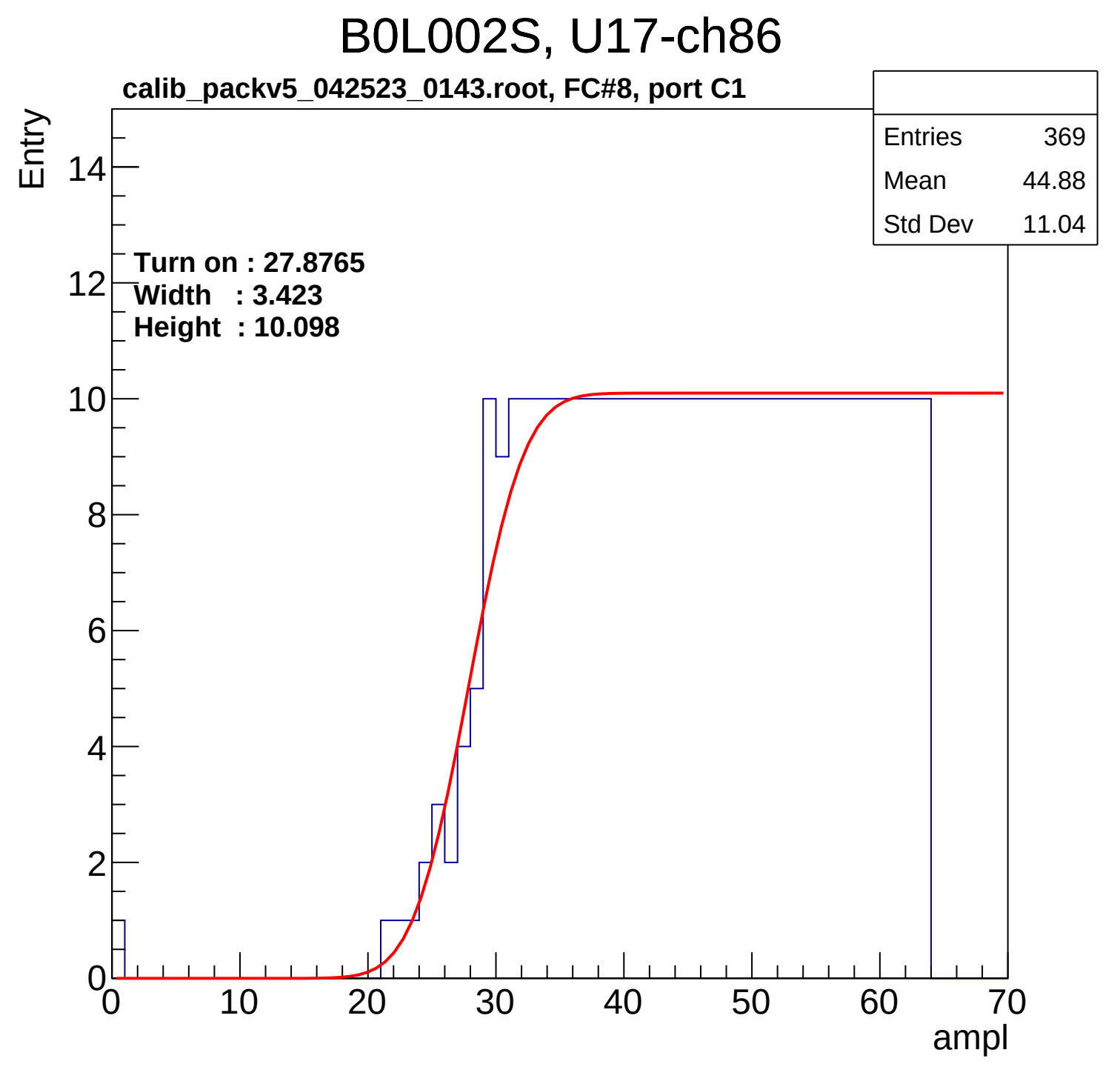
B0L002S, U17-ch86
calib_packv5_042523_0143.root, FC#8, port C1
Entries 369
Mean 44.88
Std Dev 11.04
Turn on : 27.8765
Width : 3.423
Height : 10.098
Entry
ampl
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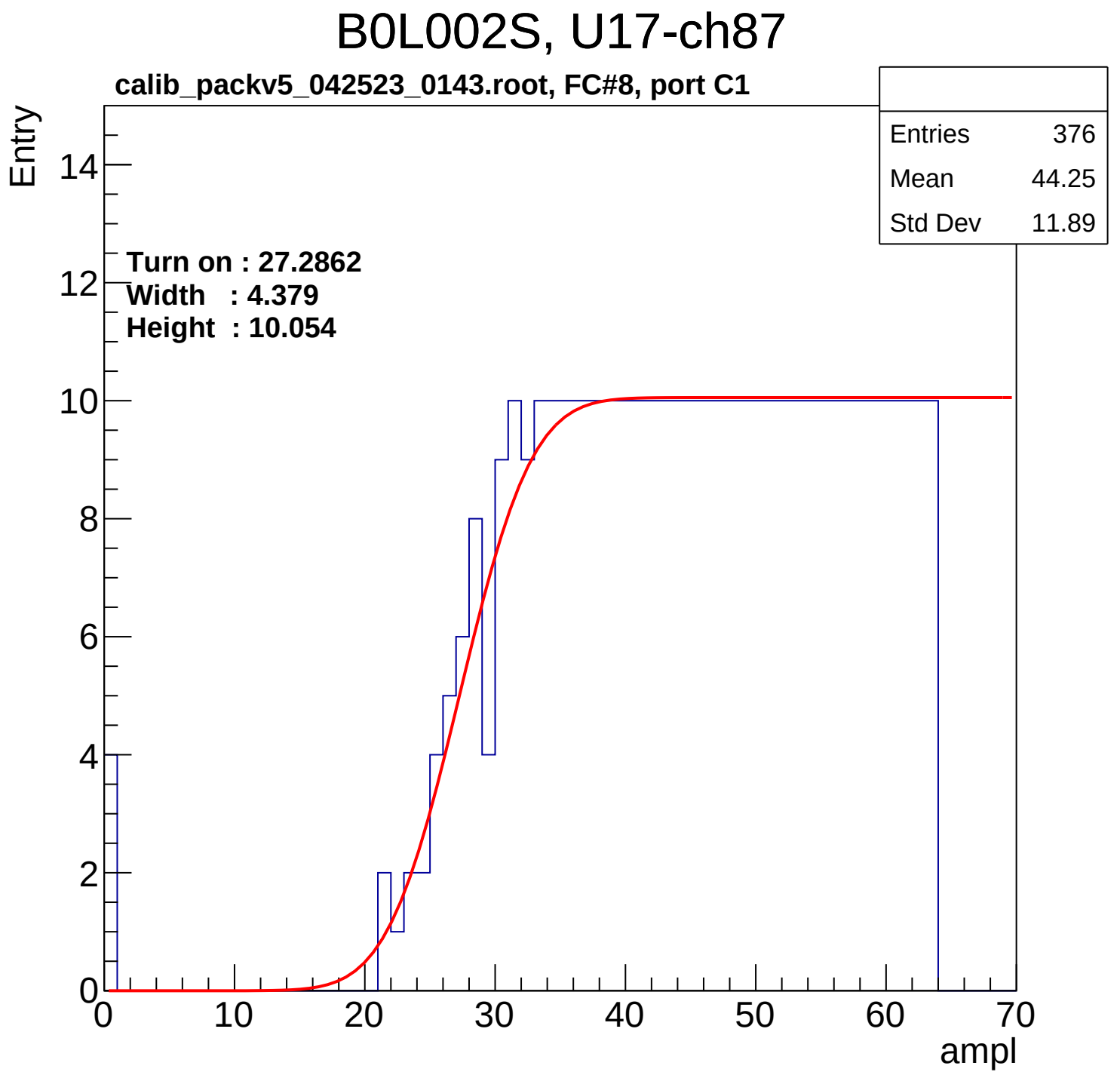
B0L002S, U17-ch87
calib_packv5_042523_0143.root, FC#8, port C1
Entries 376
Mean 44.25
Std Dev 11.89
Turn on : 27.2862
Width : 4.379
Height : 10.054
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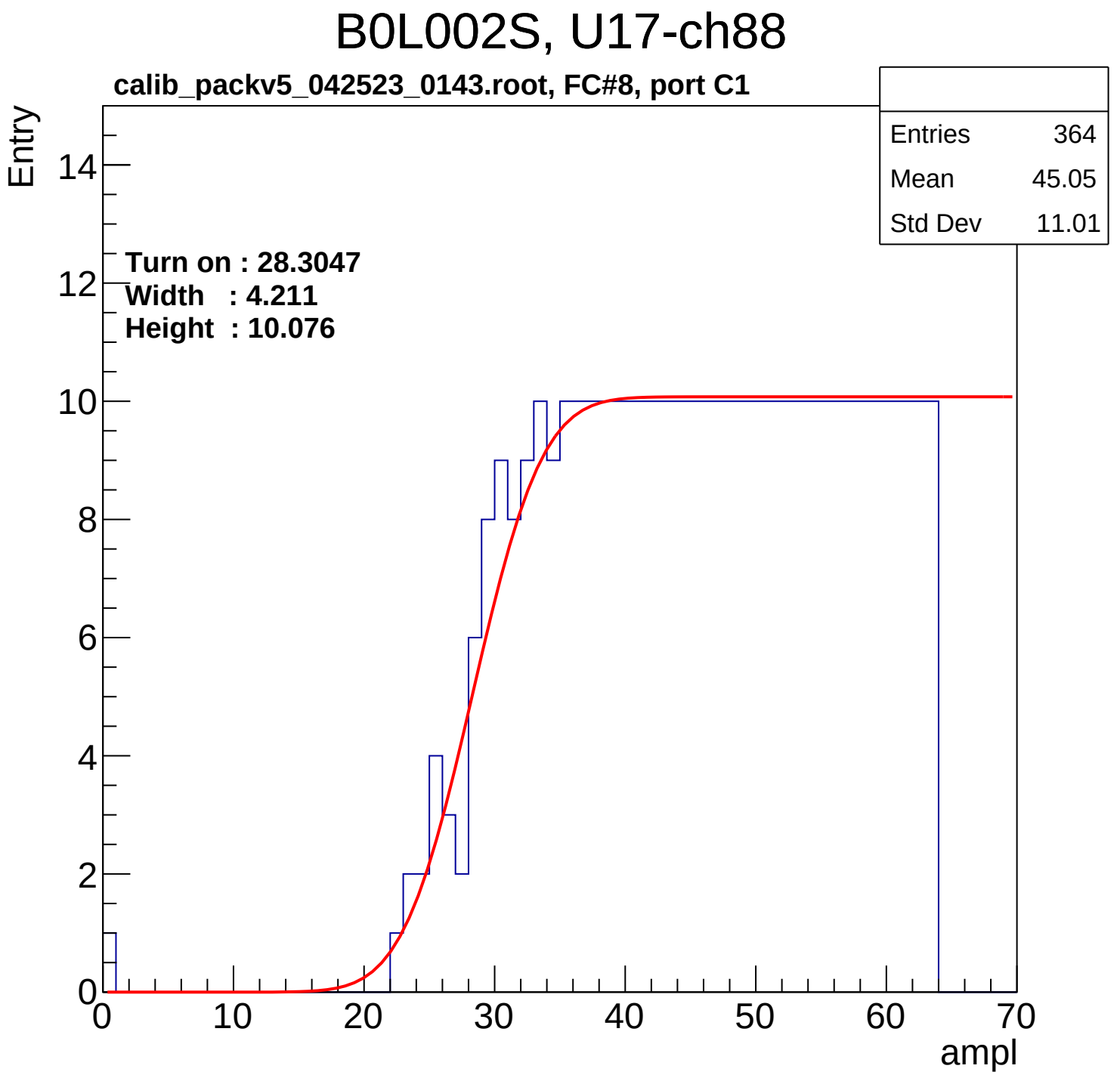
B0L002S, U17-ch88
calib_packv5_042523_0143.root, FC#8, port C1
Entries 364
Mean 45.05
Std Dev 11.01
Turn on : 28.3047
Width : 4.211
Height : 10.076
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ampl
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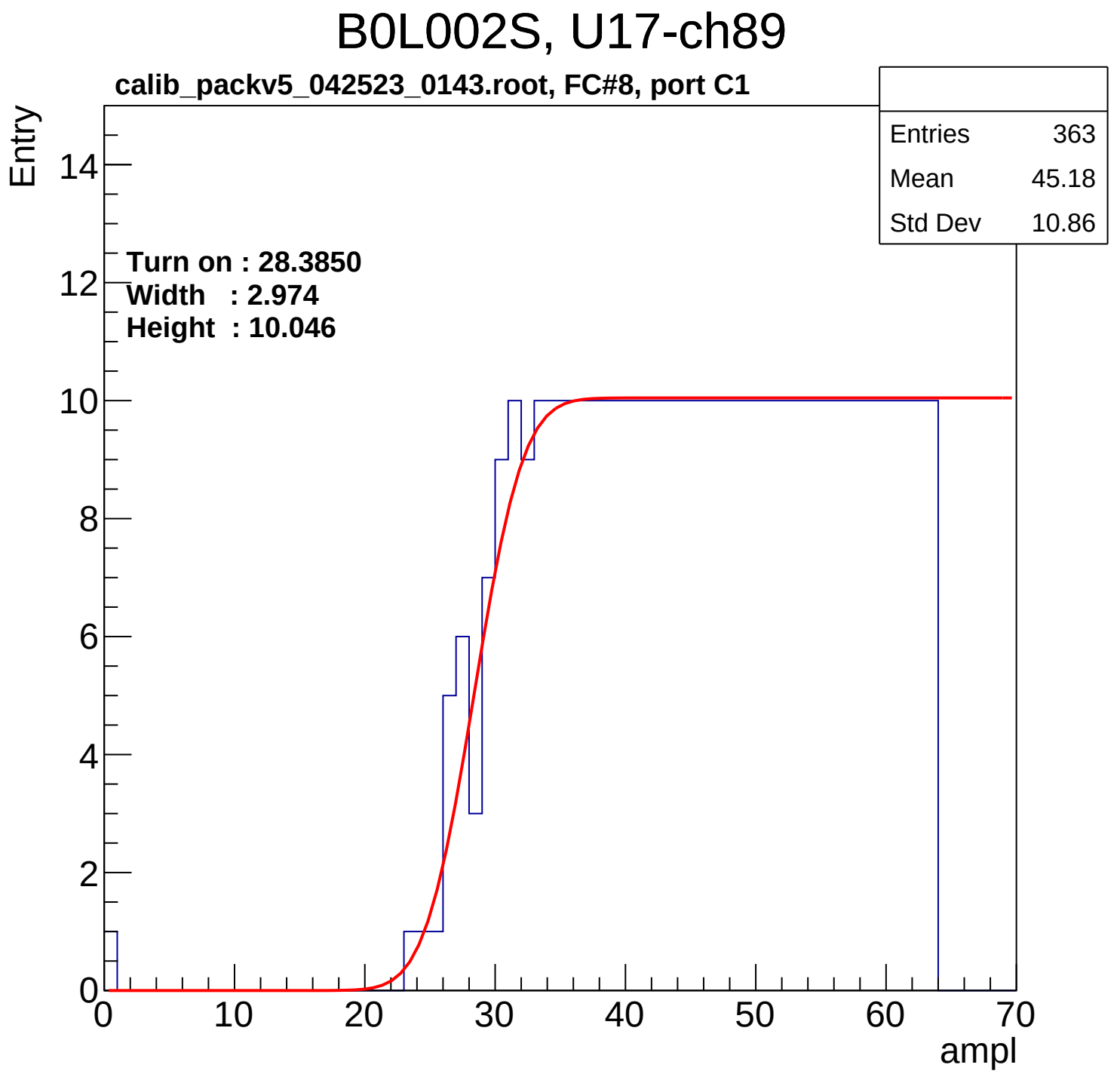
B0L002S, U17-ch89
calib_packv5_042523_0143.root, FC#8, port C1
Entries 363
Mean 45.18
Std Dev 10.86
Turn on : 28.3850
Width : 2.974
Height : 10.046
Entry
ampl
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2
4
6
8
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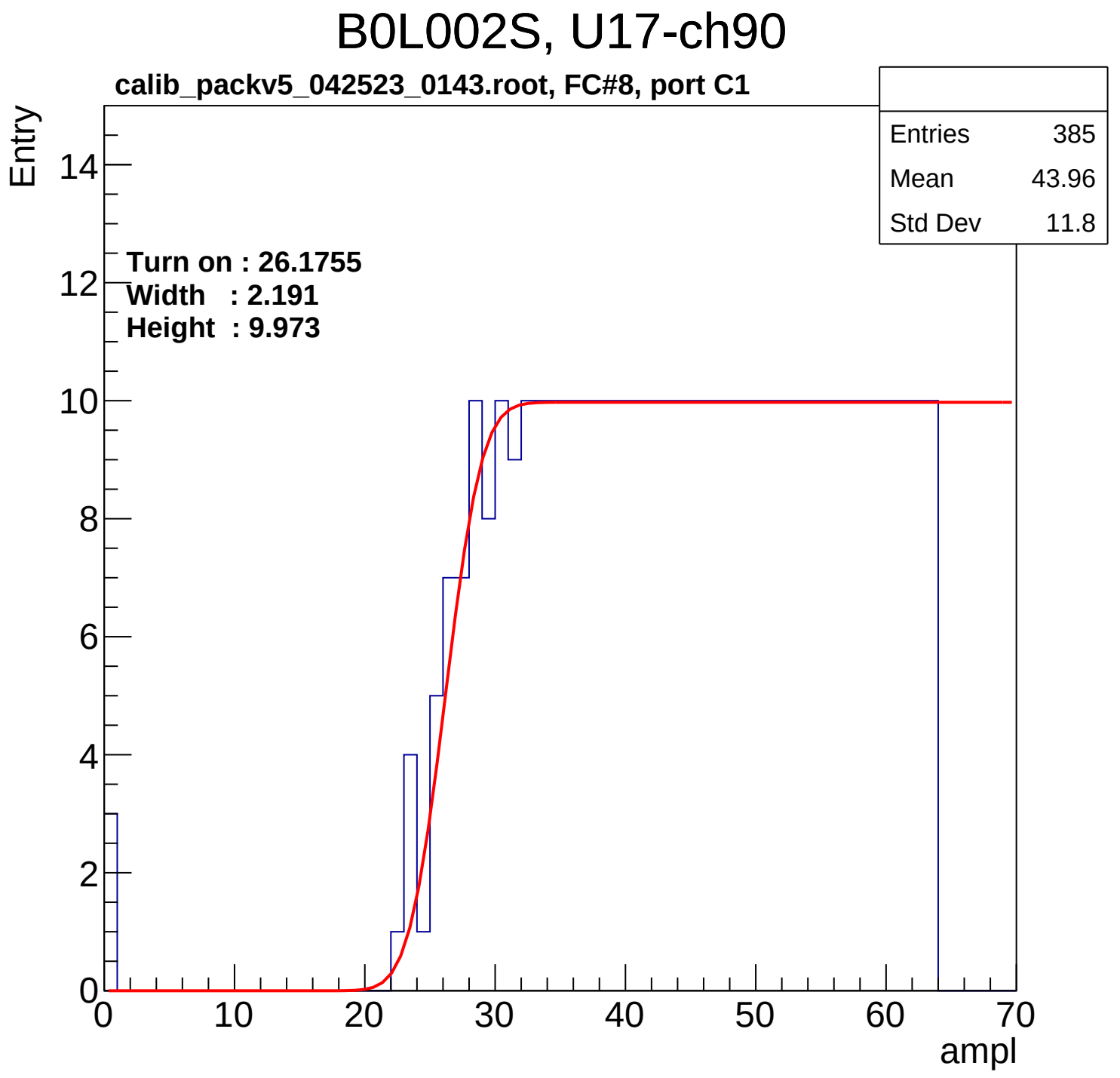
B0L002S, U17-ch90
calib_packv5_042523_0143.root, FC#8, port C1
Entries 385
Mean 43.96
Std Dev 11.8
Turn on : 26.1755
Width : 2.191
Height : 9.973
Entry
ampl
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2
4
6
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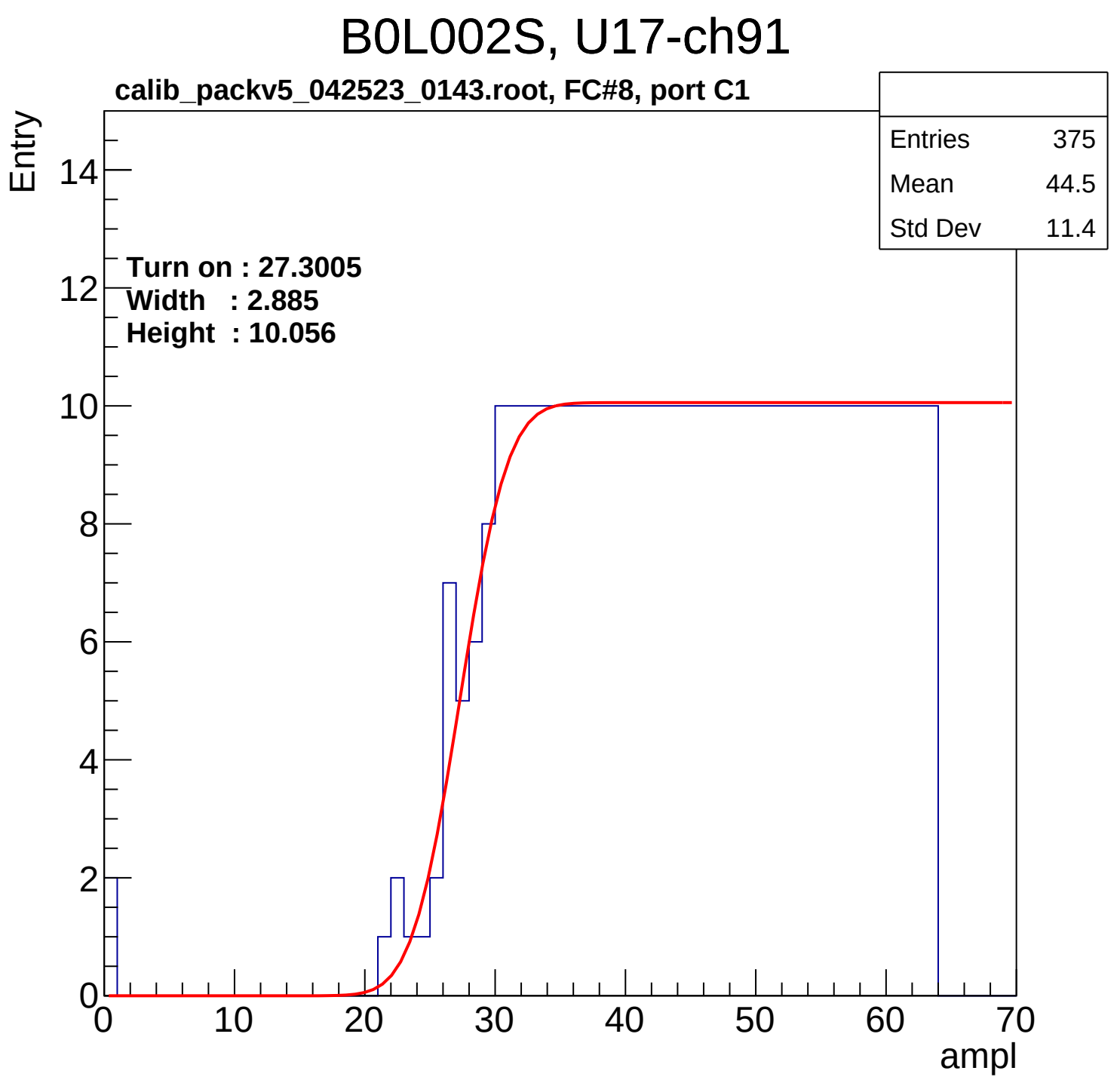
B0L002S, U17-ch91
calib_packv5_042523_0143.root, FC#8, port C1
Entries 375
Mean 44.5
Std Dev 11.4
Turn on : 27.3005
Width : 2.885
Height : 10.056
Entry
ampl
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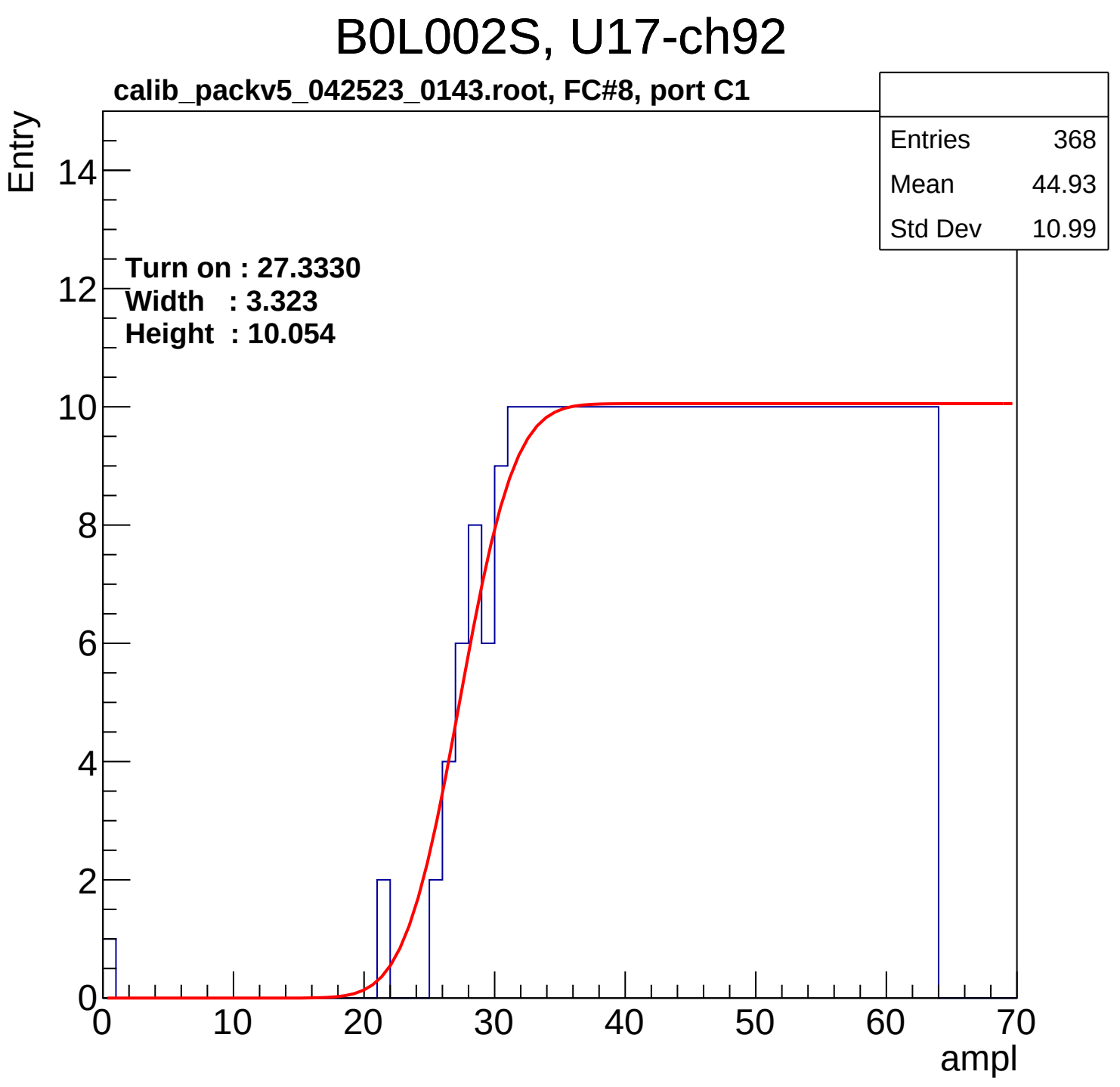
B0L002S, U17-ch92
calib_packv5_042523_0143.root, FC#8, port C1
Entries 368
Mean 44.93
Std Dev 10.99
Turn on : 27.3330
Width : 3.323
Height : 10.054
Entry
ampl
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2
4
6
8
10
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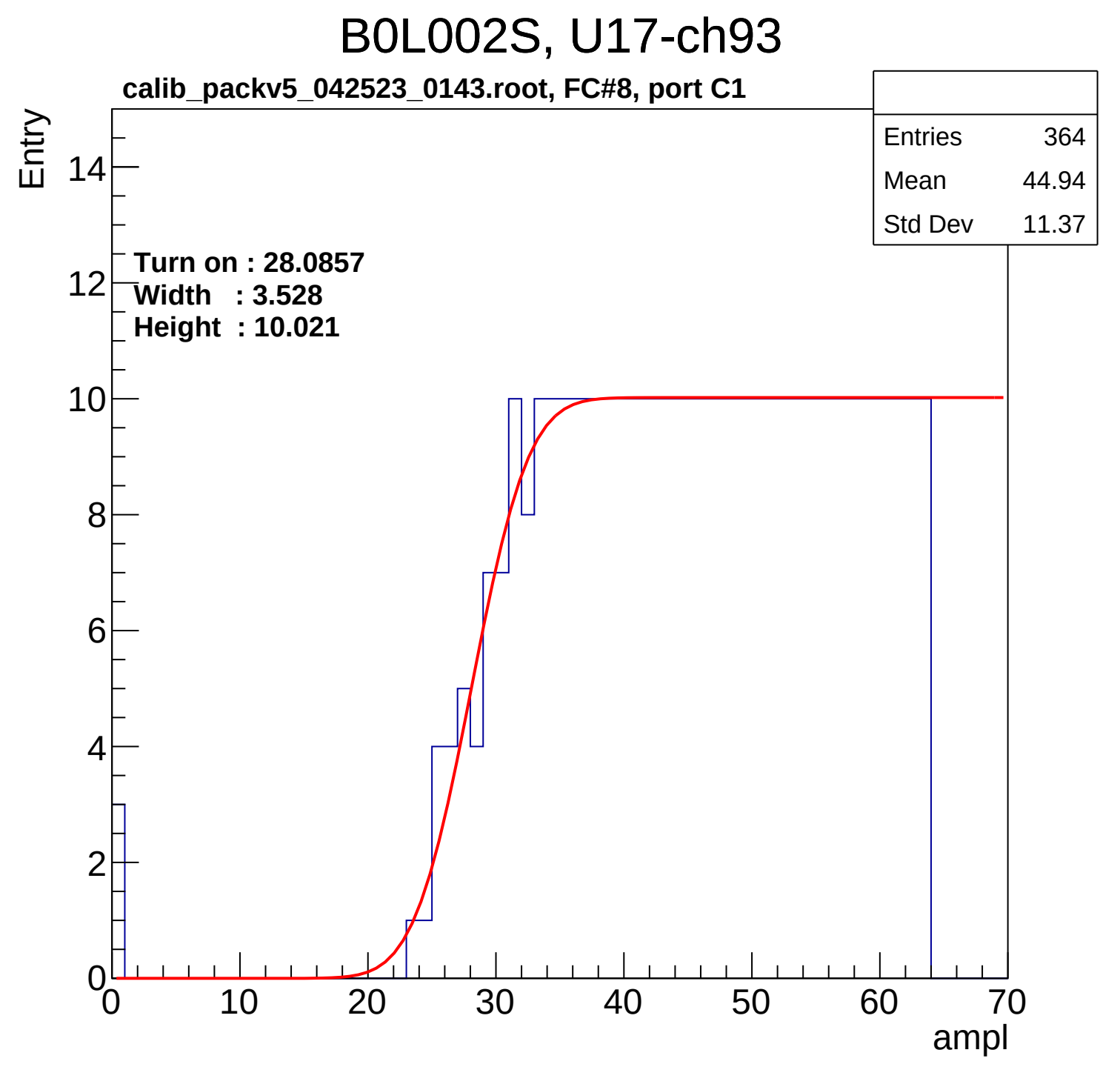
B0L002S, U17-ch93
calib_packv5_042523_0143.root, FC#8, port C1
Entries 364
Mean 44.94
Std Dev 11.37
Turn on : 28.0857
Width : 3.528
Height : 10.021
Entry
ampl
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6
8
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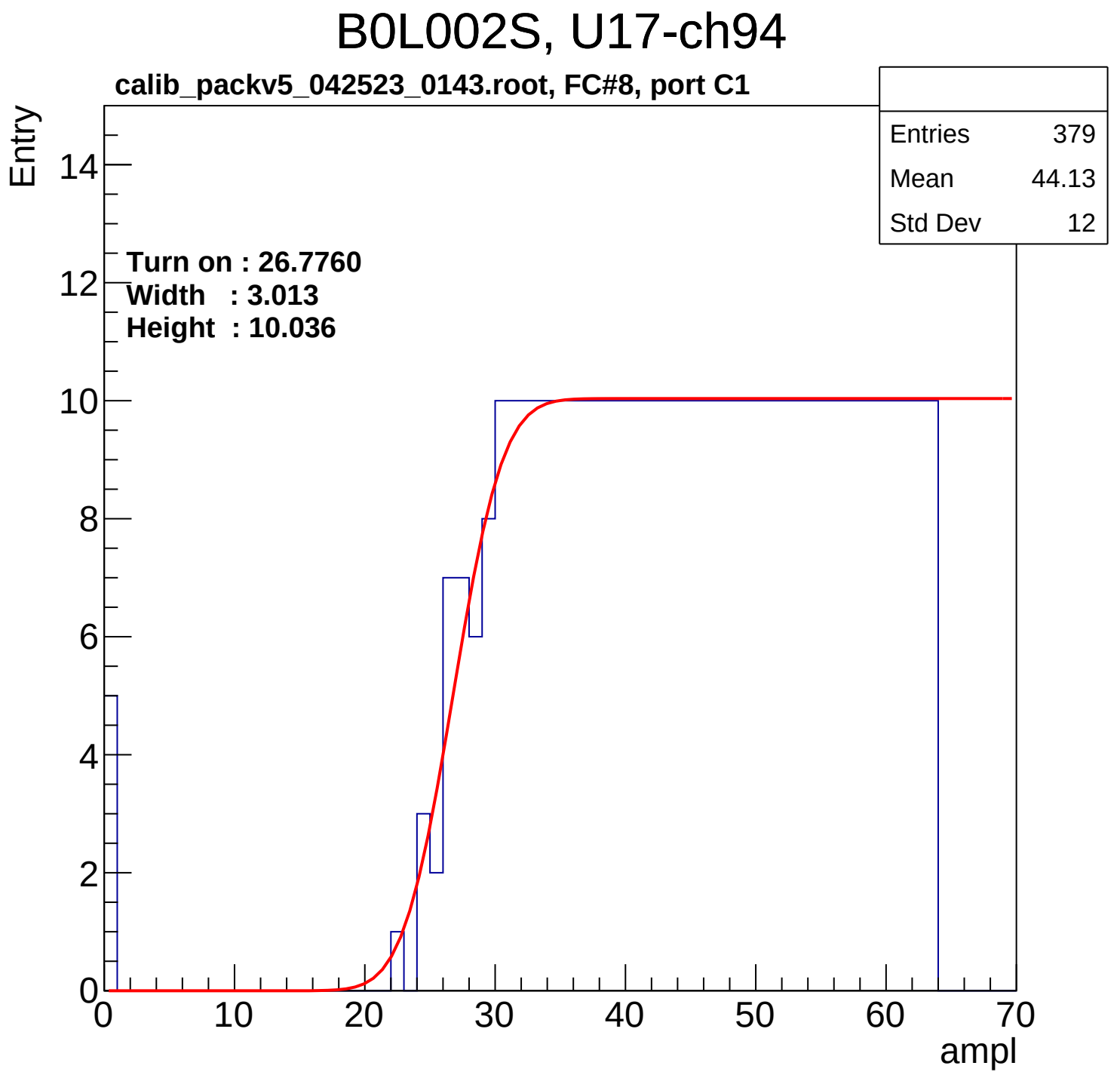
B0L002S, U17-ch94
calib_packv5_042523_0143.root, FC#8, port C1
Entries 379
Mean 44.13
Std Dev 12
Turn on : 26.7760
Width : 3.013
Height : 10.036
Entry
ampl
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2
4
6
8
10
12
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0
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60
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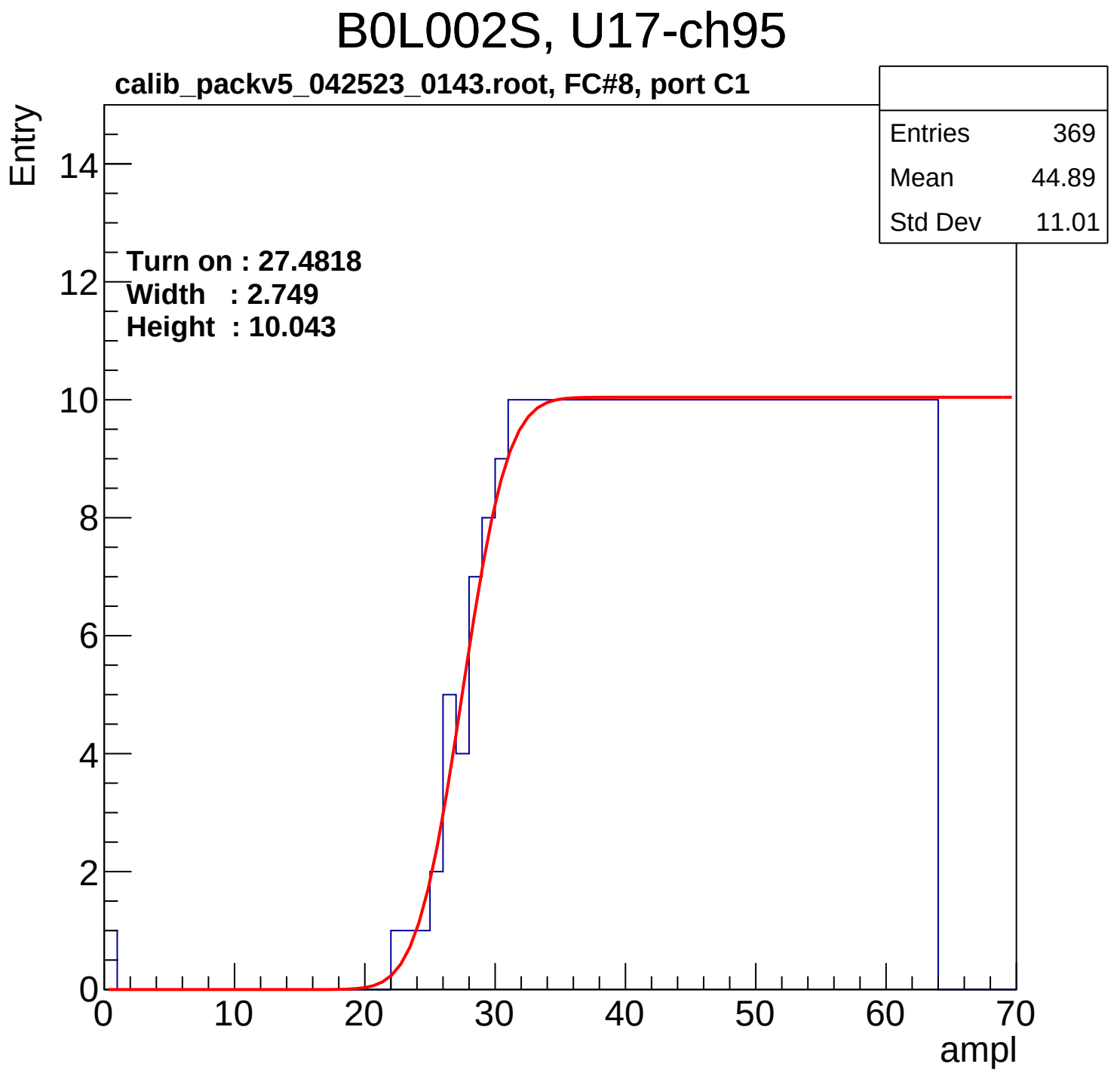
B0L002S, U17-ch95
calib_packv5_042523_0143.root, FC#8, port C1
Entries 369
Mean 44.89
Std Dev 11.01
Turn on : 27.4818
Width : 2.749
Height : 10.043
Entry
ampl
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4
6
8
10
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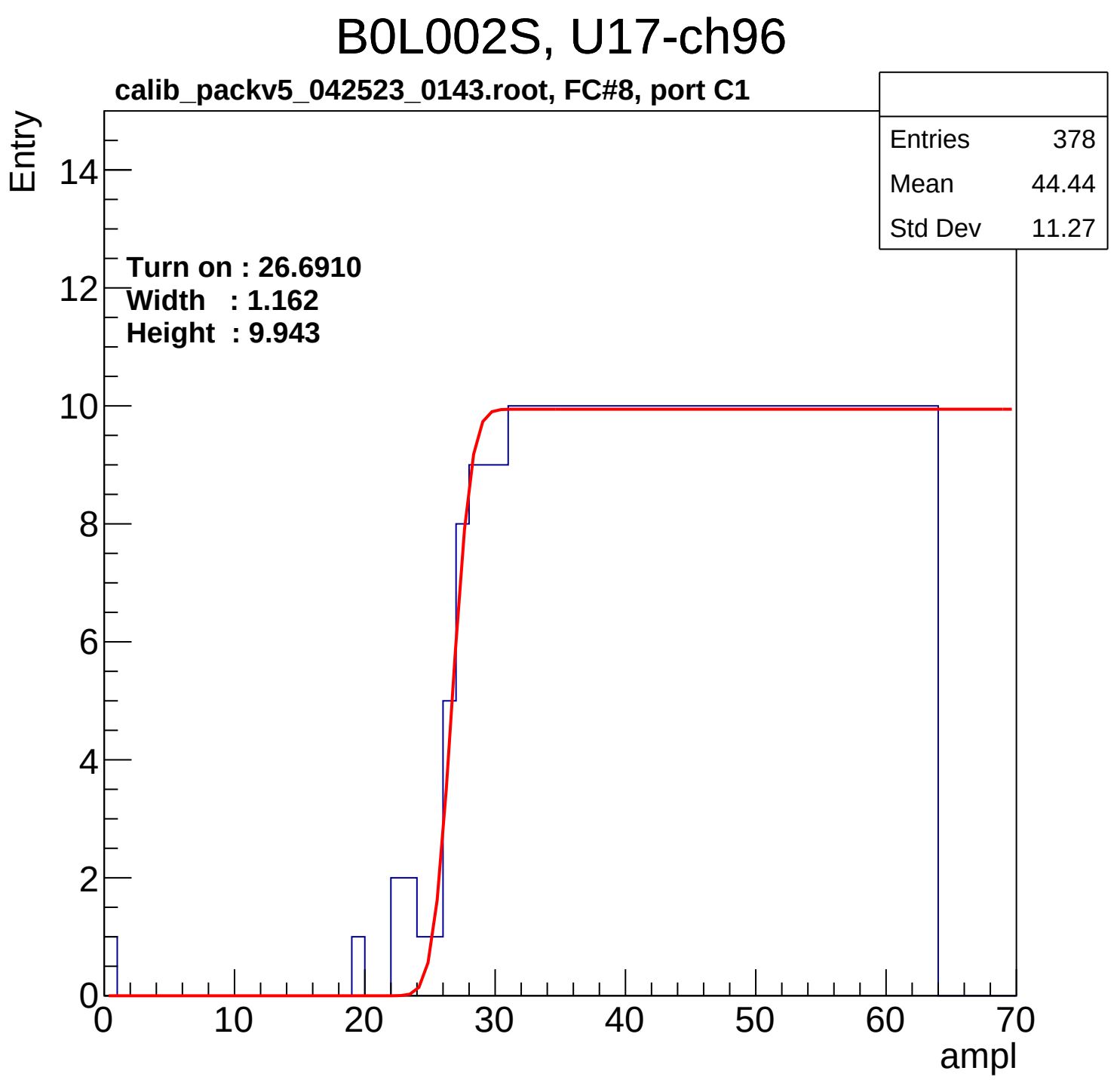
B0L002S, U17-ch96
calib_packv5_042523_0143.root, FC#8, port C1
Entries 378
Mean 44.44
Std Dev 11.27
Turn on : 26.6910
Width : 1.162
Height : 9.943
Entry
ampl
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2
4
6
8
10
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0
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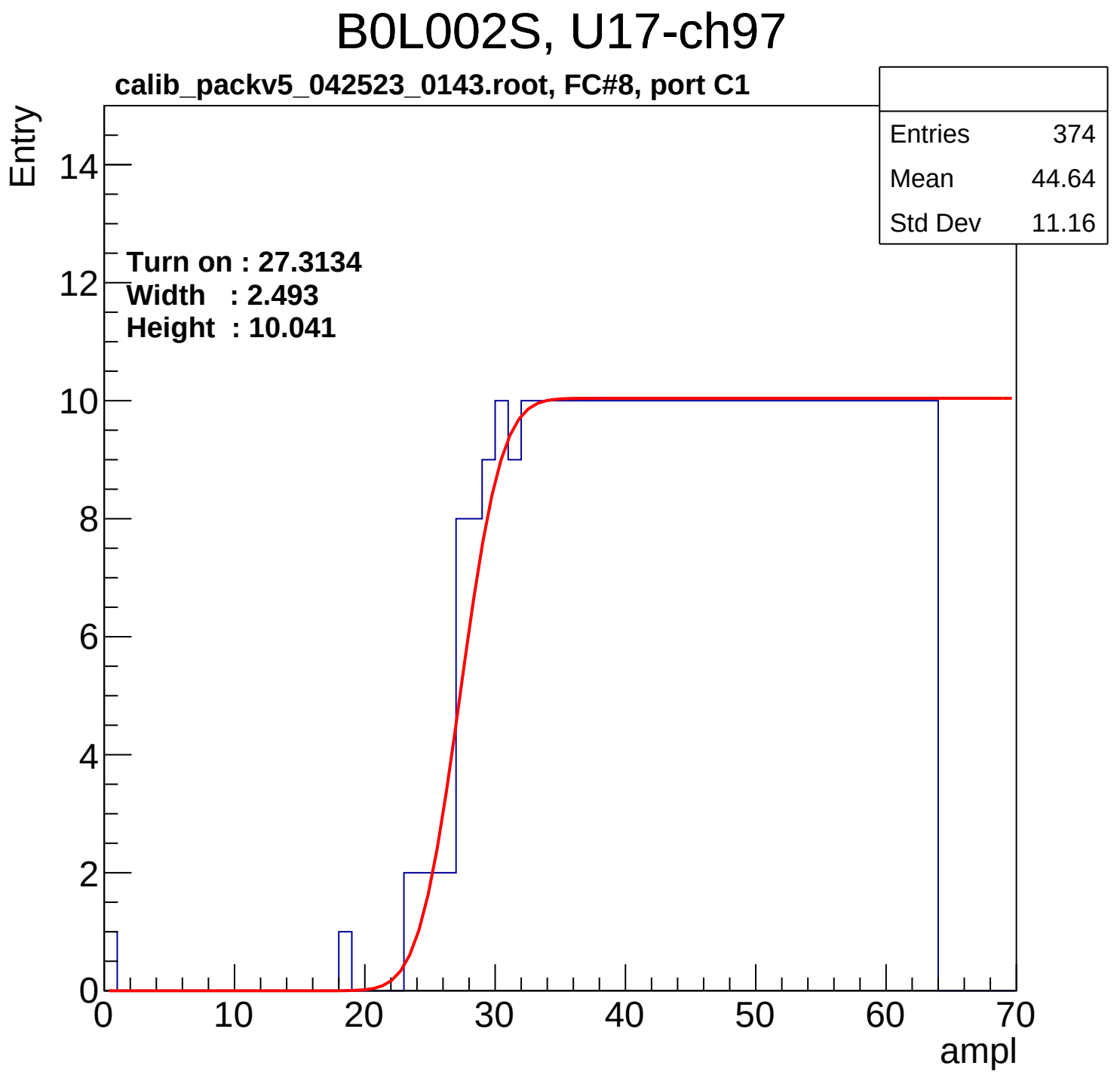
B0L002S, U17-ch97
calib_packv5_042523_0143.root, FC#8, port C1
Entries 374
Mean 44.64
Std Dev 11.16
Turn on : 27.3134
Width : 2.493
Height : 10.041
Entry
ampl
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2
4
6
8
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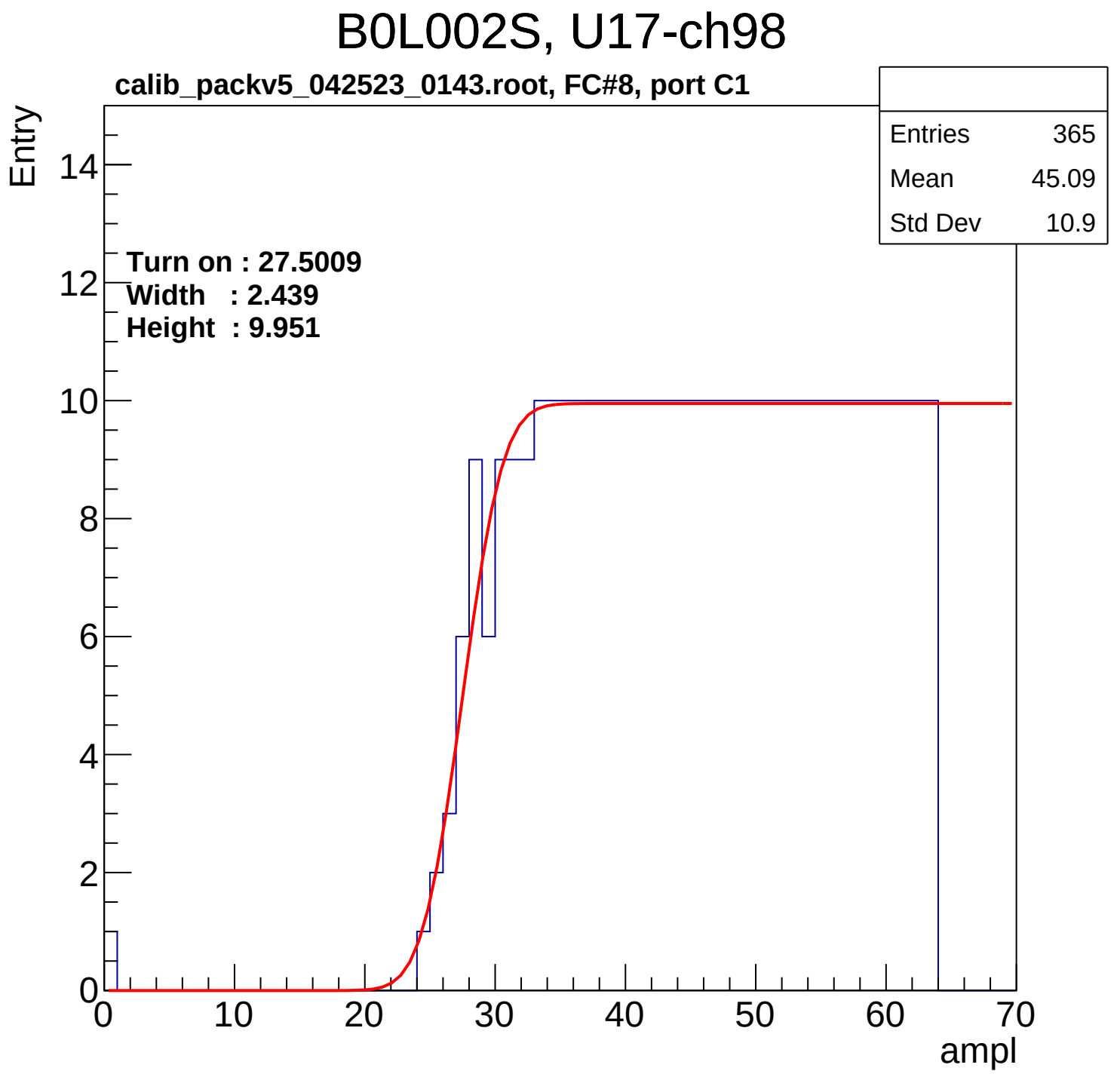
B0L002S, U17-ch98
calib_packv5_042523_0143.root, FC#8, port C1
Entries 365
Mean 45.09
Std Dev 10.9
Turn on : 27.5009
Width : 2.439
Height : 9.951
Entry
ampl
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6
8
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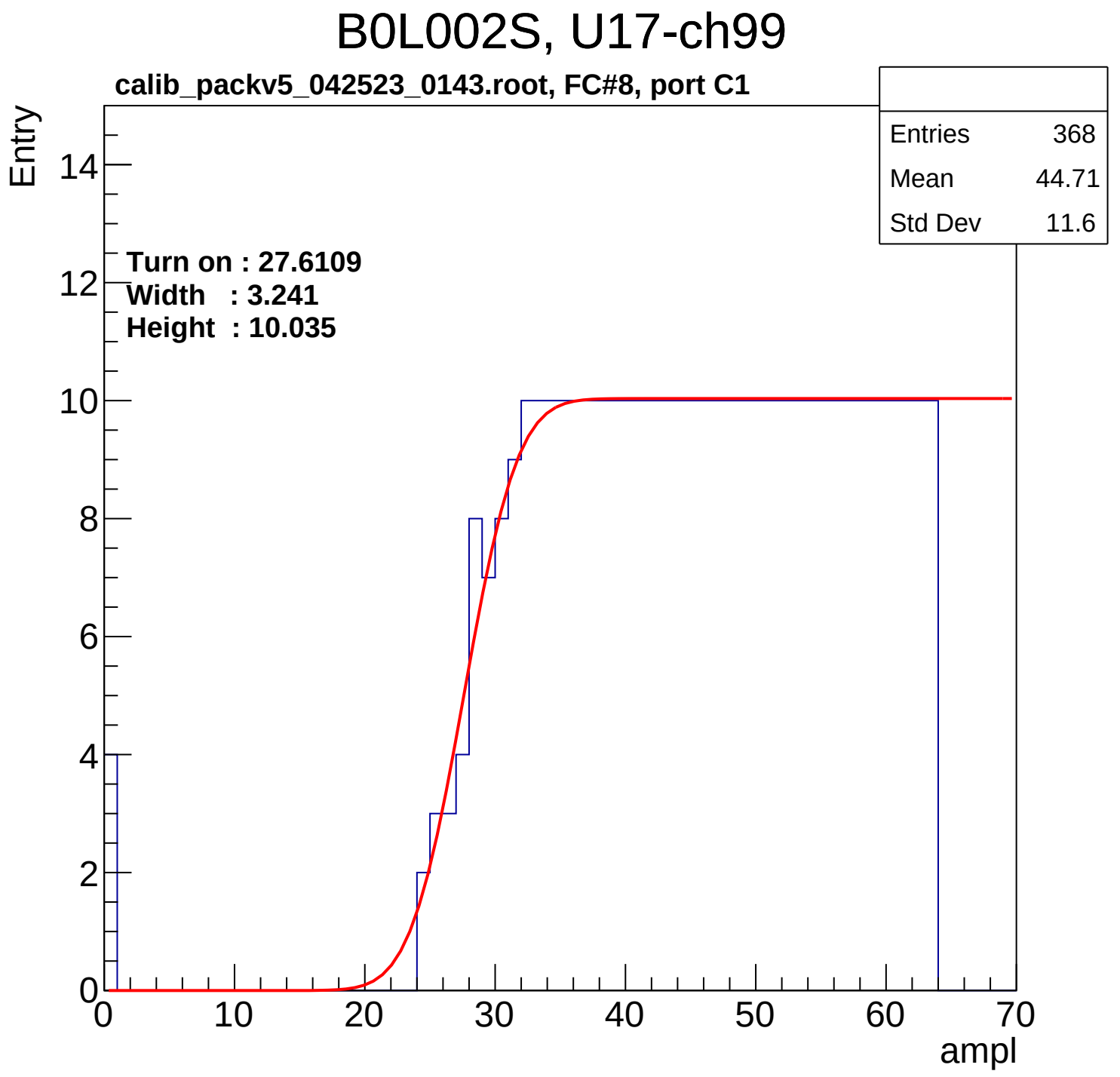
B0L002S, U17-ch99
calib_packv5_042523_0143.root, FC#8, port C1
Entries 368
Mean 44.71
Std Dev 11.6
Turn on : 27.6109
Width : 3.241
Height : 10.035
Entry
ampl
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6
8
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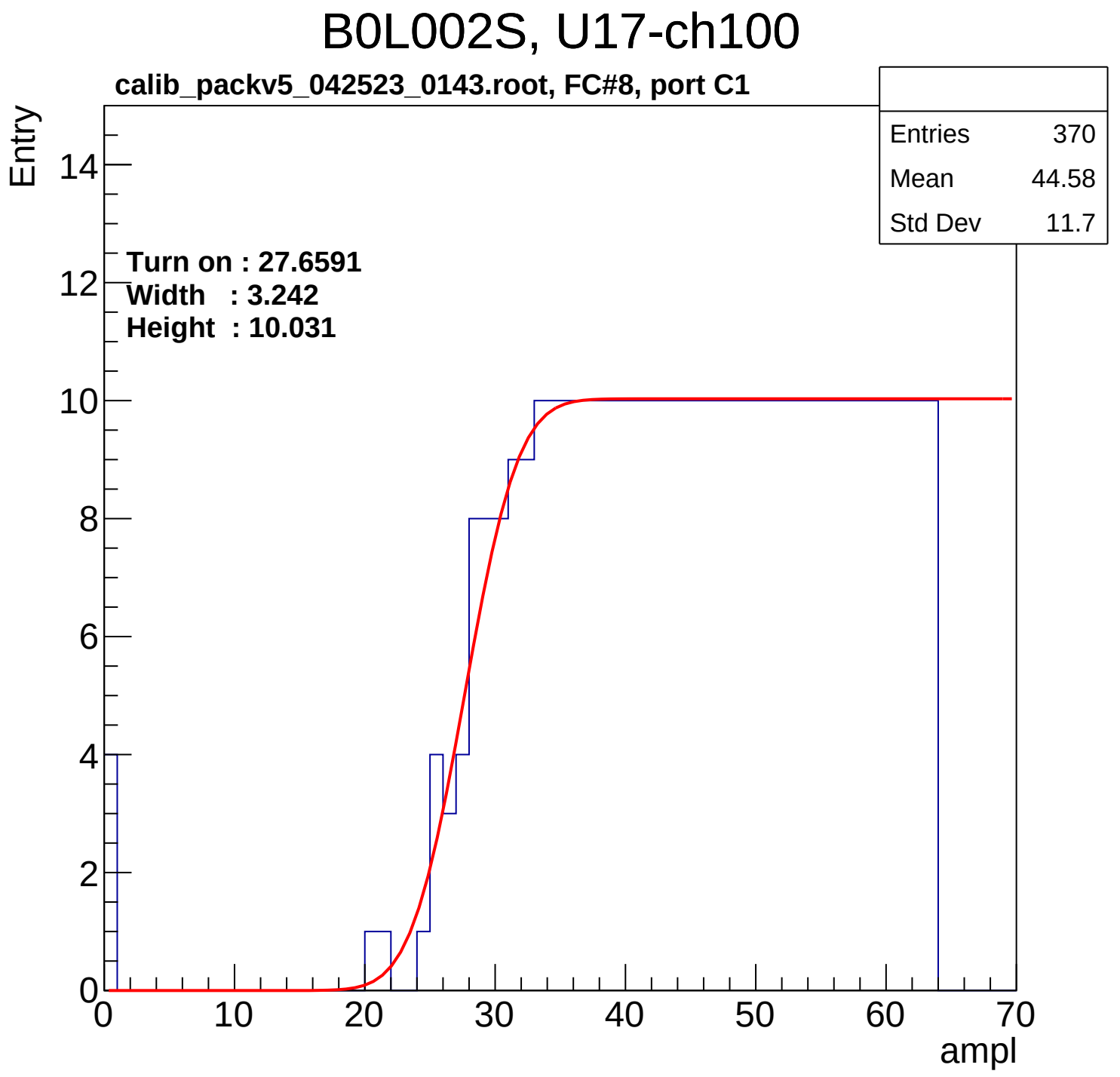
B0L002S, U17-ch100
calib_packv5_042523_0143.root, FC#8, port C1
Entries 370
Mean 44.58
Std Dev 11.7
Turn on : 27.6591
Width : 3.242
Height : 10.031
Entry
ampl
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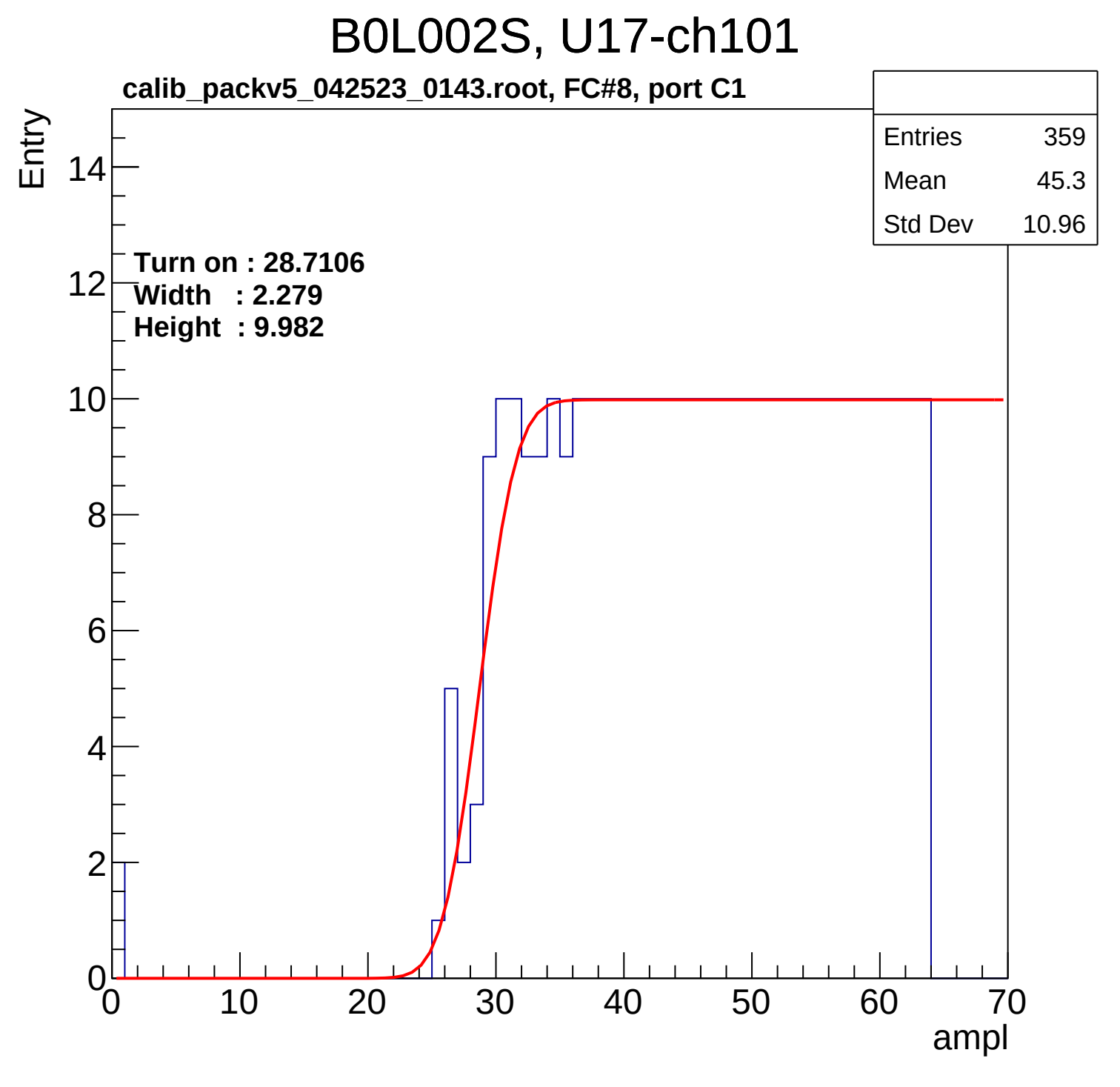
B0L002S, U17-ch101
calib_packv5_042523_0143.root, FC#8, port C1
Entries 359
Mean 45.3
Std Dev 10.96
Turn on : 28.7106
Width : 2.279
Height : 9.982
Entry
ampl
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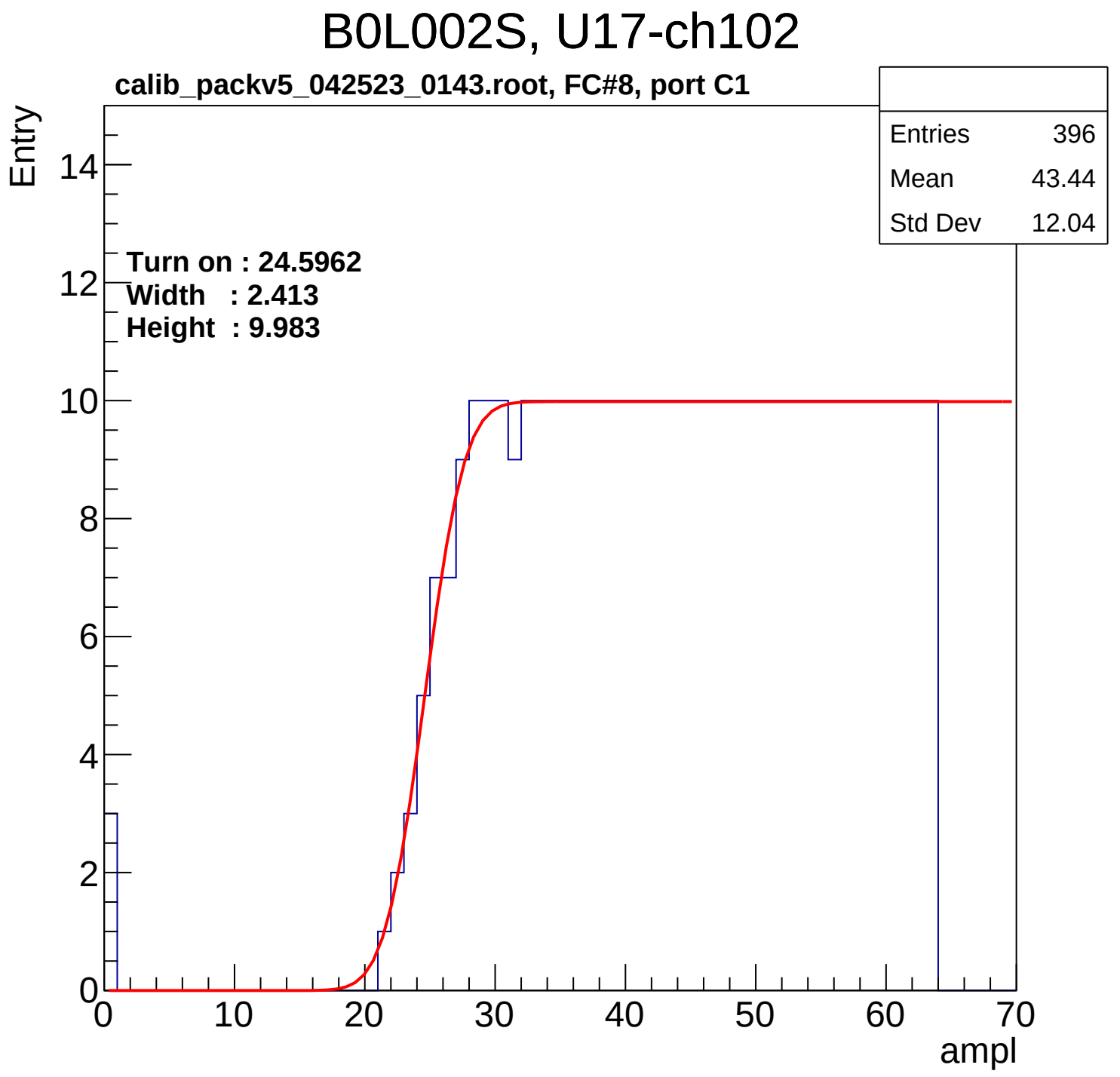
B0L002S, U17-ch102
calib_packv5_042523_0143.root, FC#8, port C1
Entries 396
Mean 43.44
Std Dev 12.04
Turn on : 24.5962
Width : 2.413
Height : 9.983
Entry
ampl
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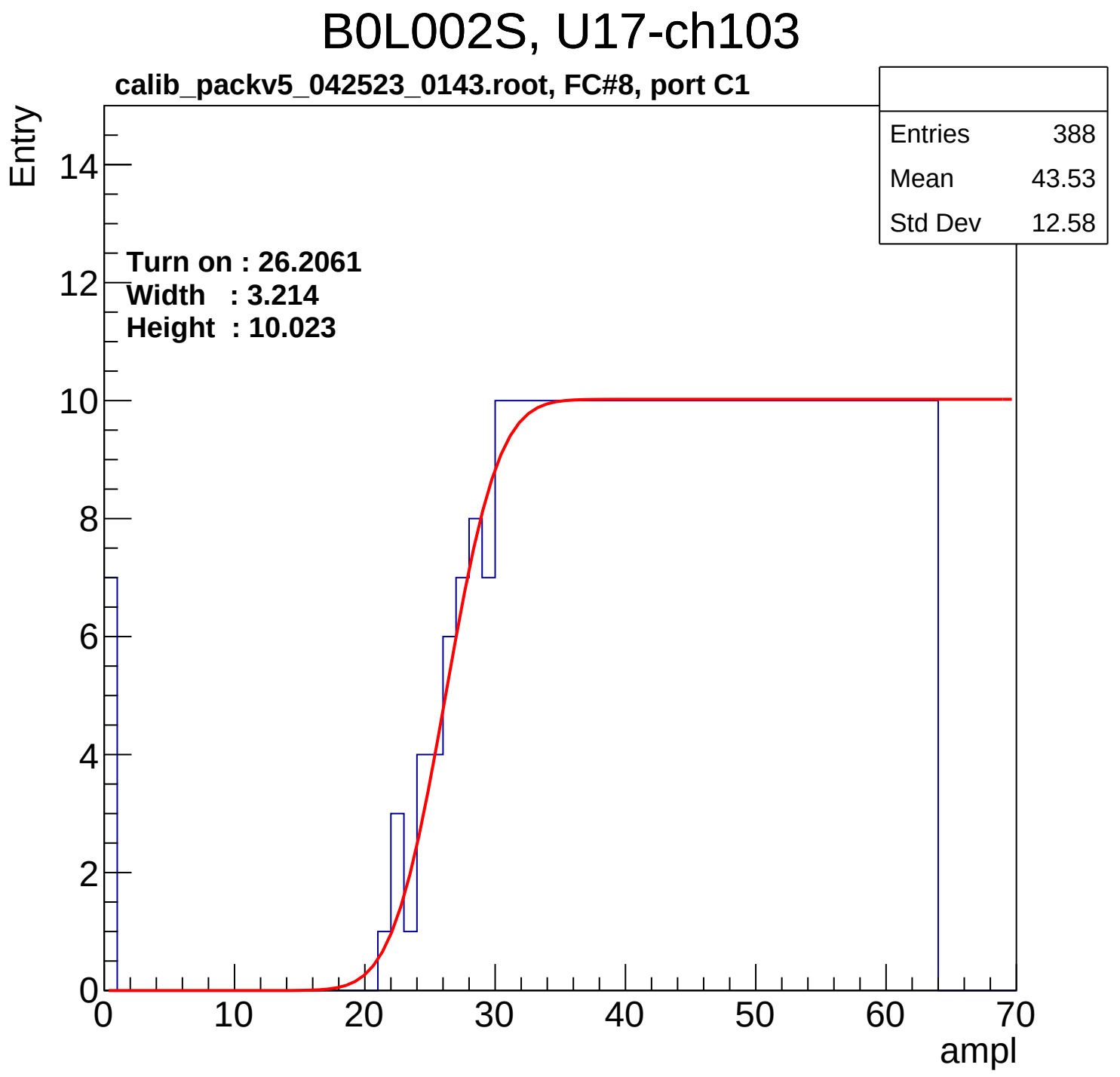
B0L002S, U17-ch103
calib_packv5_042523_0143.root, FC#8, port C1
Entries 388
Mean 43.53
Std Dev 12.58
Turn on : 26.2061
Width : 3.214
Height : 10.023
Entry
ampl
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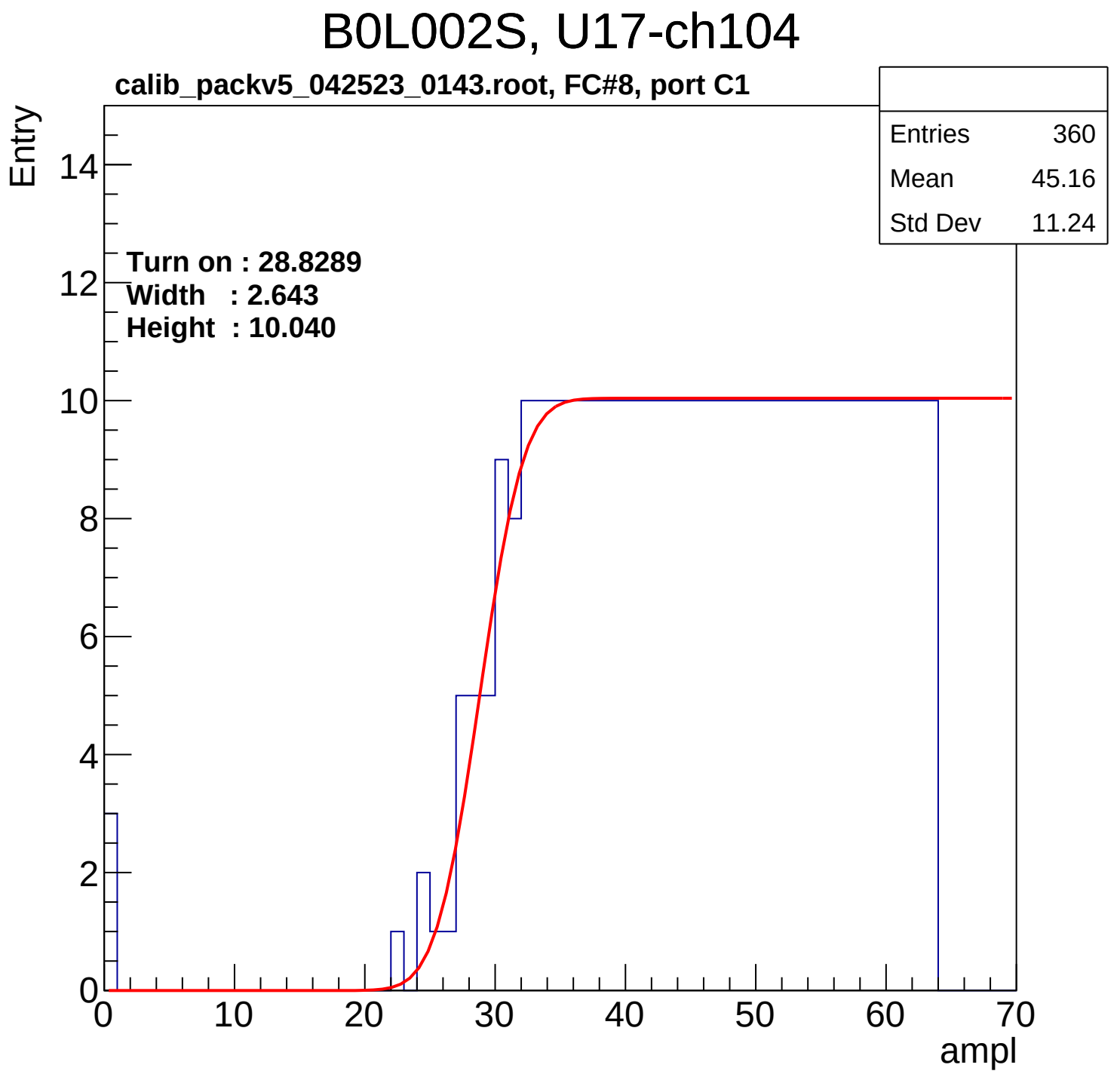
B0L002S, U17-ch104
calib_packv5_042523_0143.root, FC#8, port C1
Entries 360
Mean 45.16
Std Dev 11.24
Turn on : 28.8289
Width : 2.643
Height : 10.040
Entry
ampl
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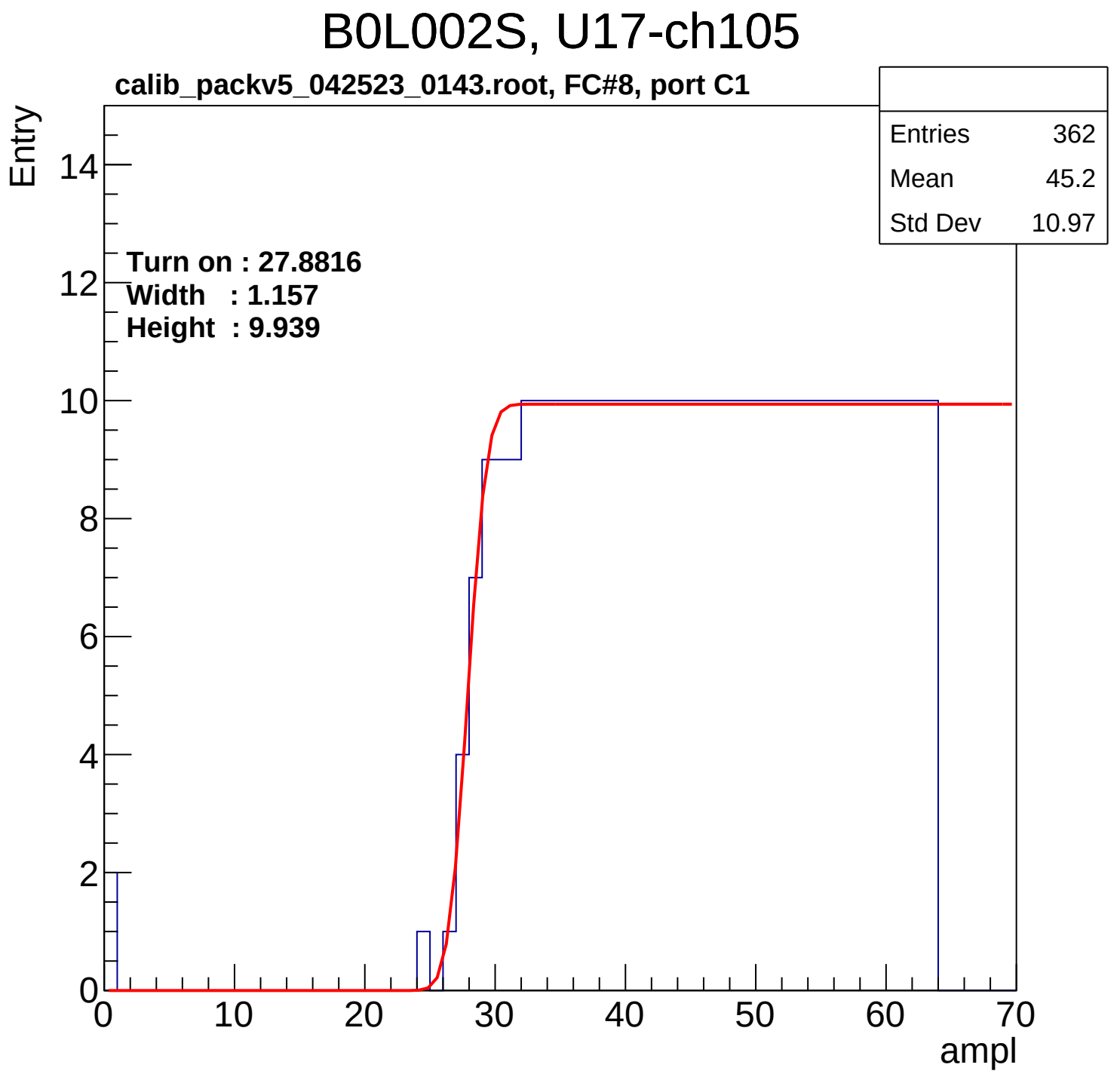
B0L002S, U17-ch105
calib_packv5_042523_0143.root, FC#8, port C1
Entries 362
Mean 45.2
Std Dev 10.97
Turn on : 27.8816
Width : 1.157
Height : 9.939
Entry
ampl
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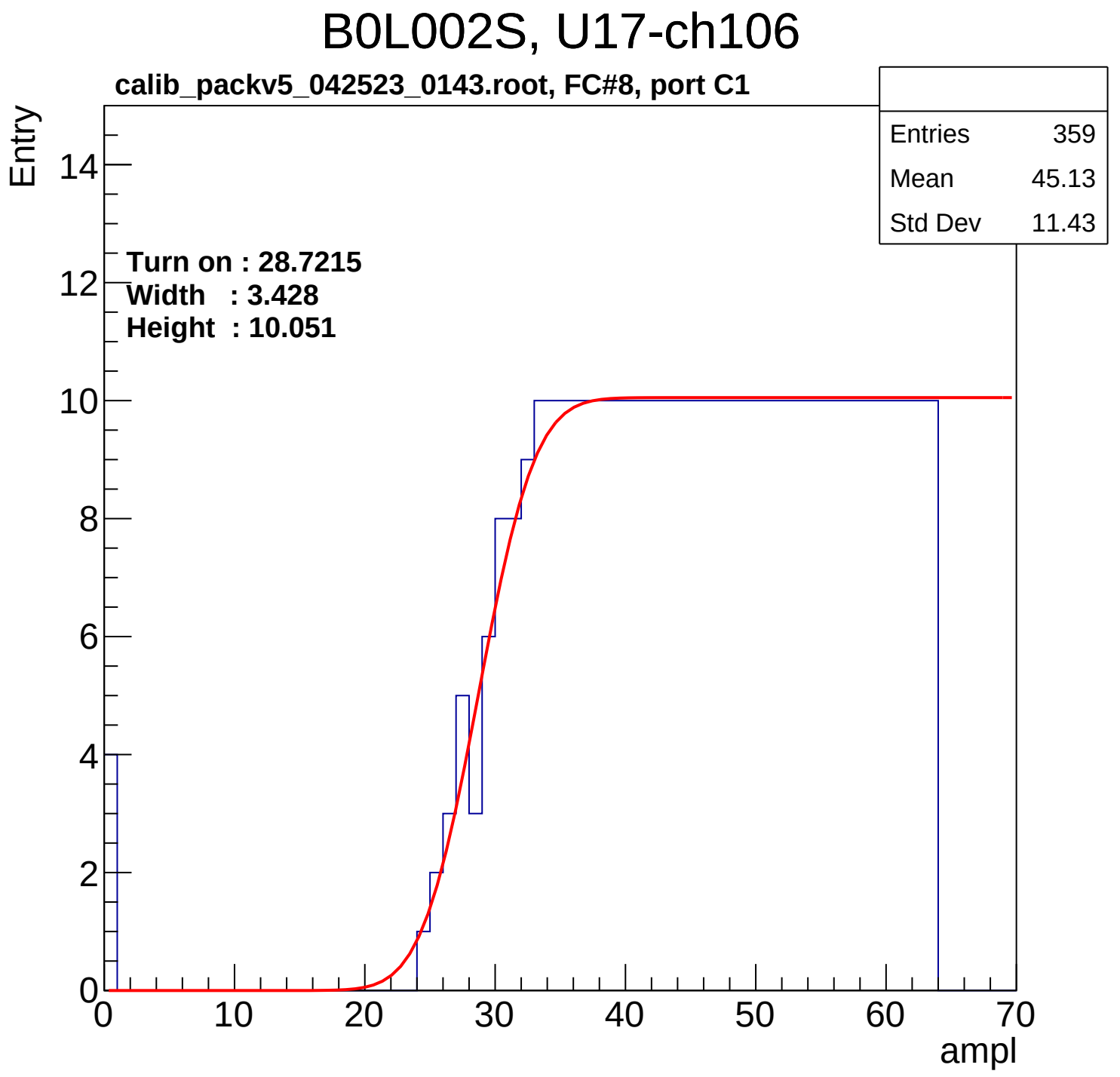
B0L002S, U17-ch106
calib_packv5_042523_0143.root, FC#8, port C1
Entries 359
Mean 45.13
Std Dev 11.43
Turn on : 28.7215
Width : 3.428
Height : 10.051
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ampl
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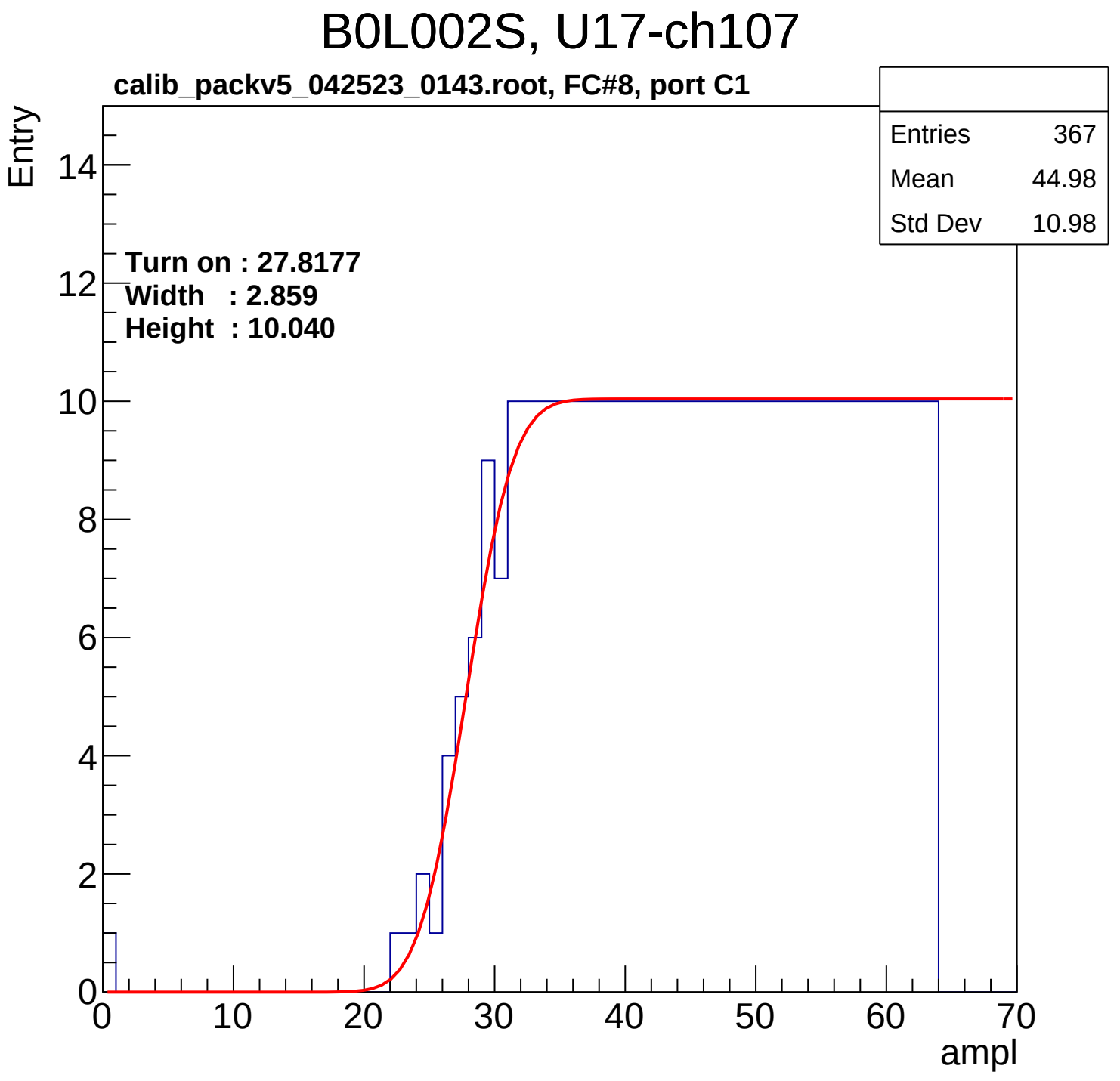
B0L002S, U17-ch107
calib_packv5_042523_0143.root, FC#8, port C1
Entries 367
Mean 44.98
Std Dev 10.98
Turn on : 27.8177
Width : 2.859
Height : 10.040
Entry
ampl
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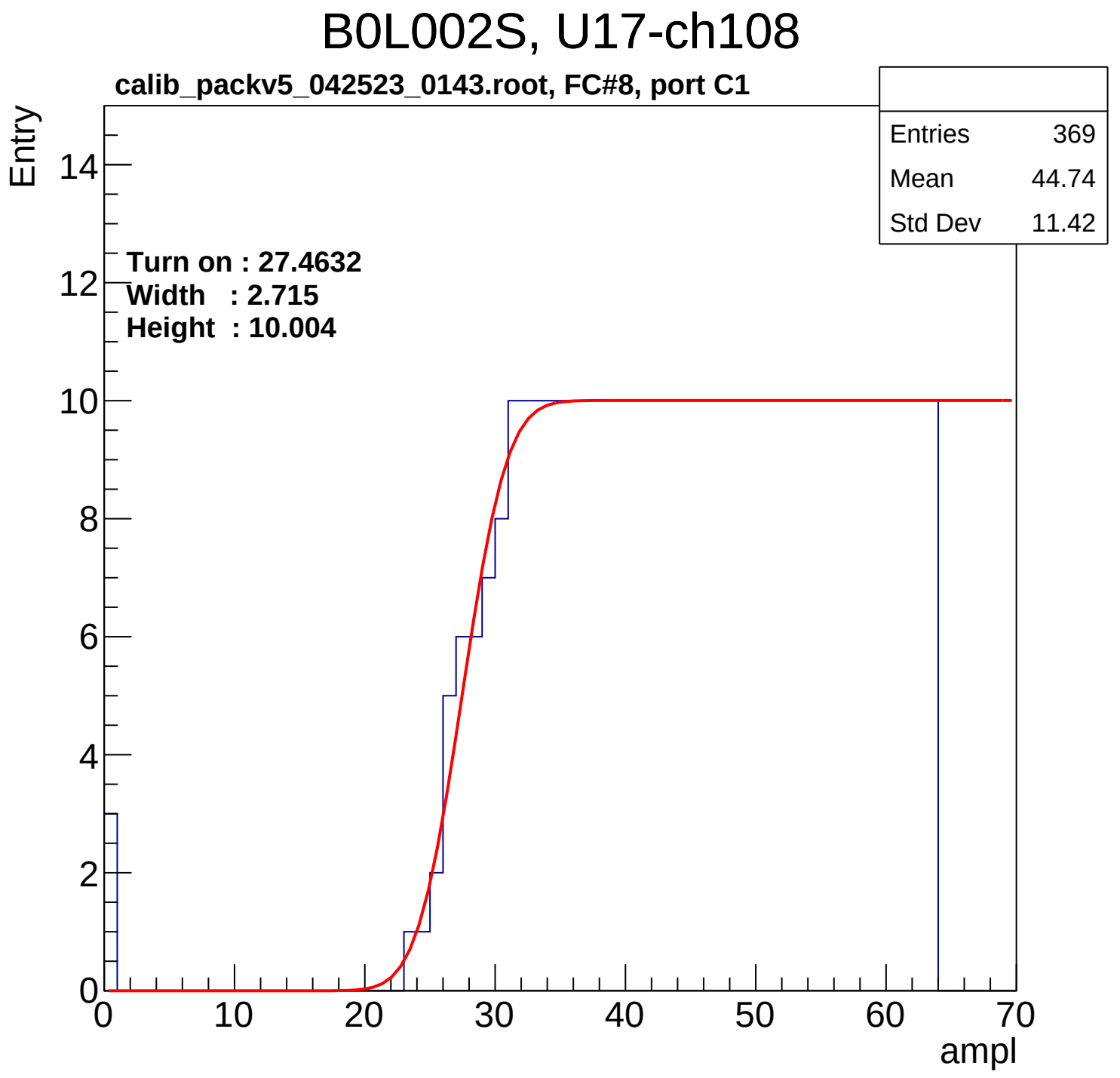
B0L002S, U17-ch108
calib_packv5_042523_0143.root, FC#8, port C1
Entries 369
Mean 44.74
Std Dev 11.42
Turn on : 27.4632
Width : 2.715
Height : 10.004
Entry
ampl
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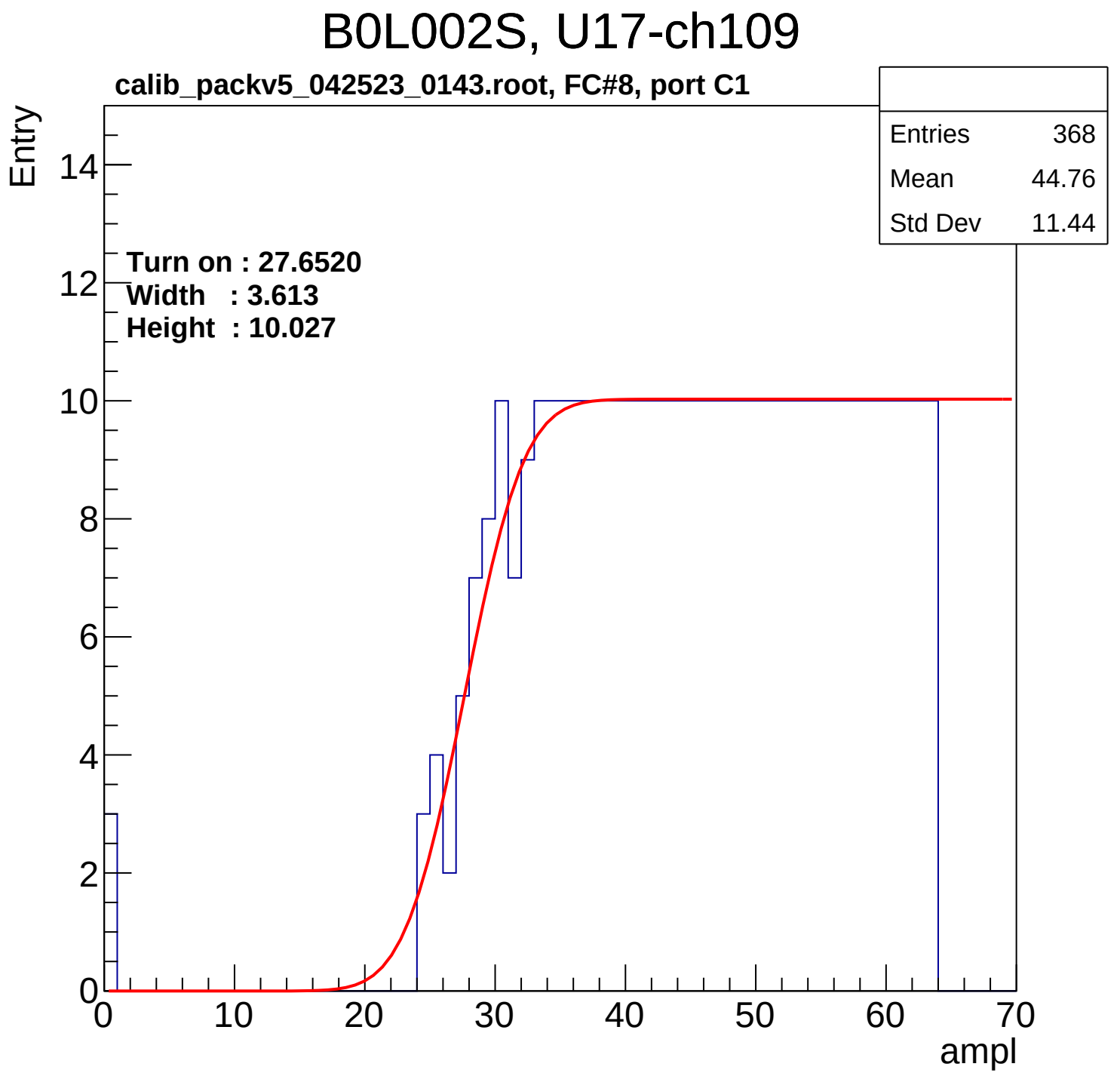
B0L002S, U17-ch109
calib_packv5_042523_0143.root, FC#8, port C1
Entries 368
Mean 44.76
Std Dev 11.44
Turn on : 27.6520
Width : 3.613
Height : 10.027
Entry
ampl
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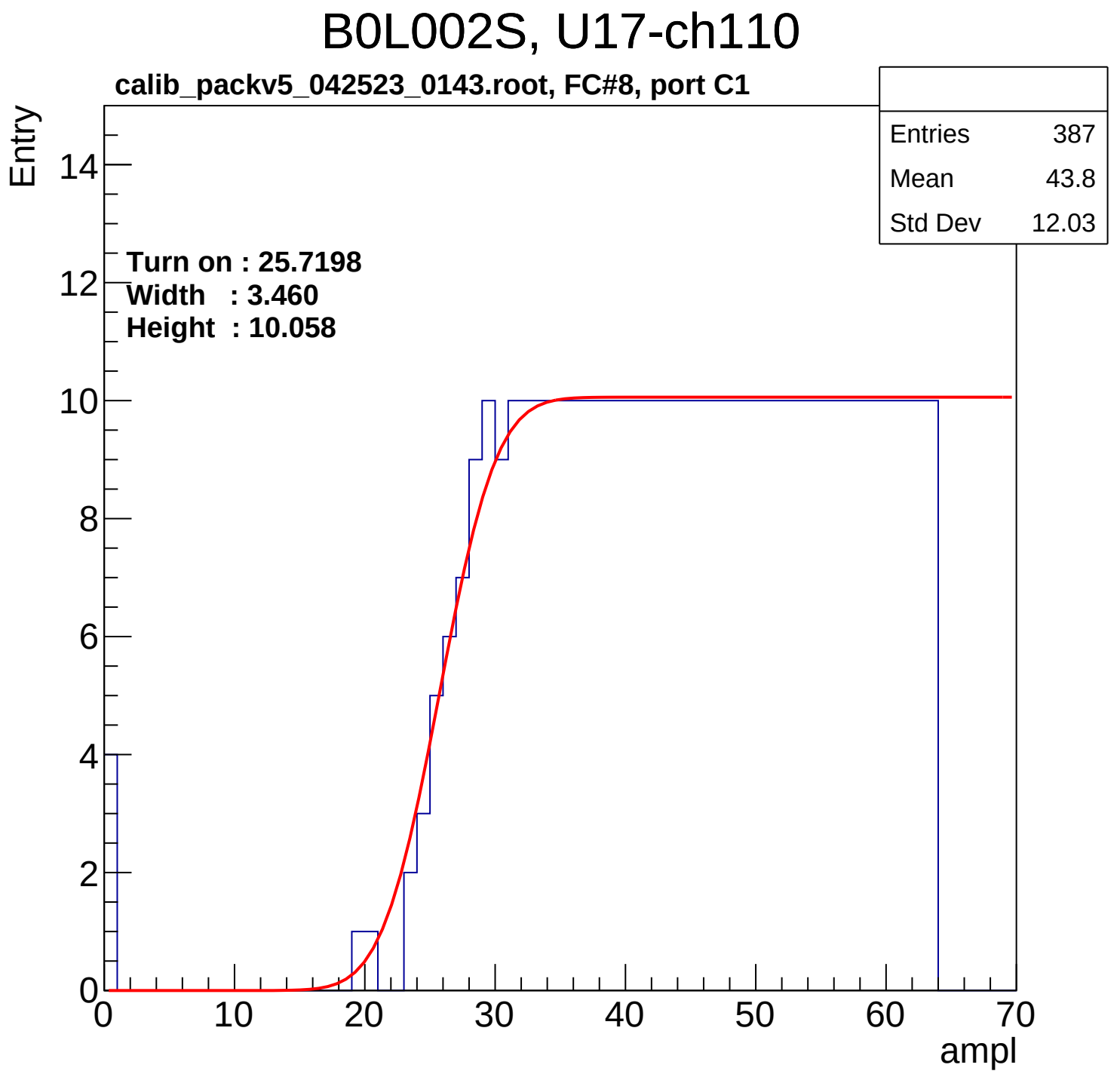
B0L002S, U17-ch110
calib_packv5_042523_0143.root, FC#8, port C1
Entries 387
Mean 43.8
Std Dev 12.03
Turn on : 25.7198
Width : 3.460
Height : 10.058
Entry
ampl
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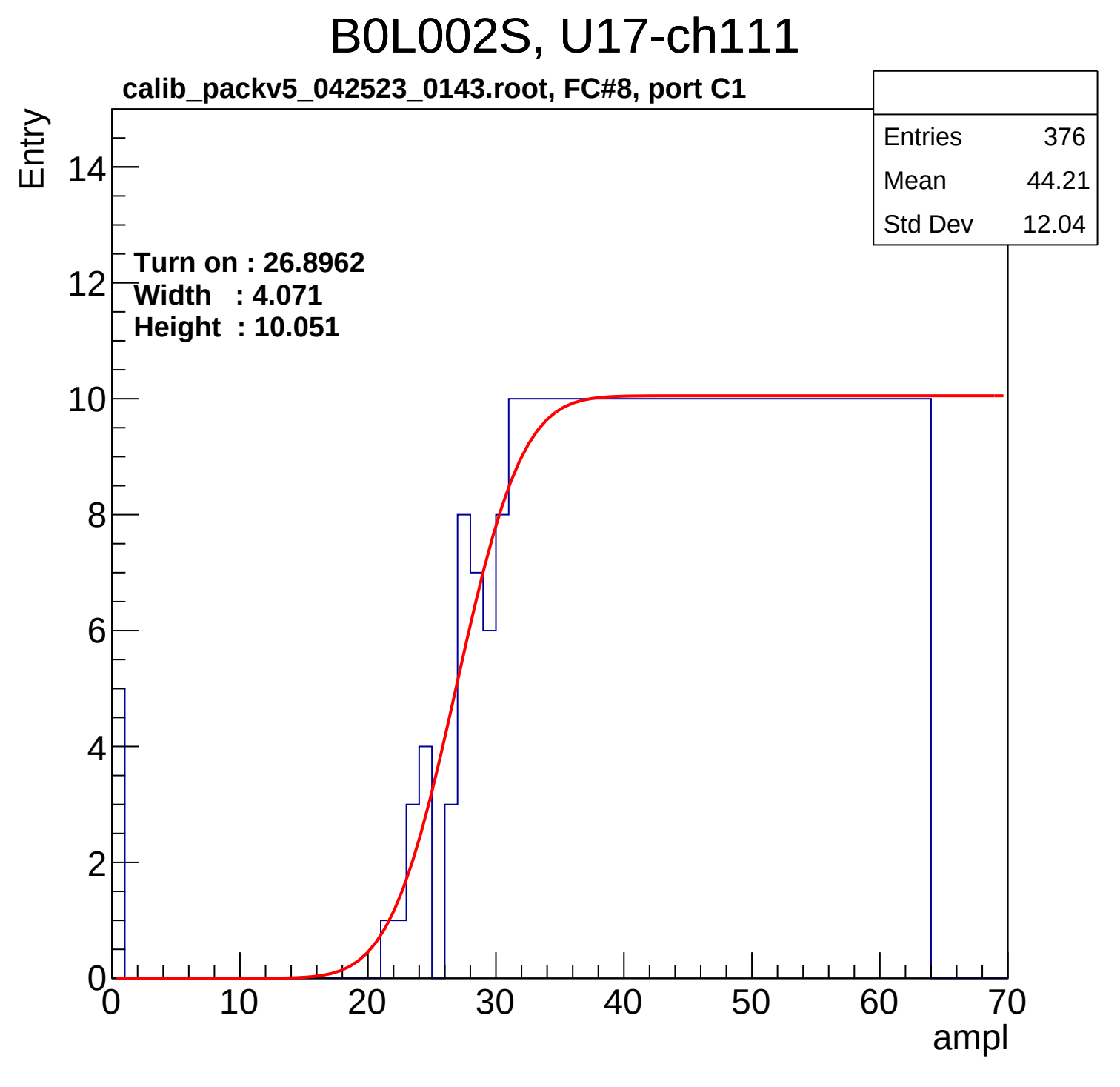
B0L002S, U17-ch111
calib_packv5_042523_0143.root, FC#8, port C1
Entries 376
Mean 44.21
Std Dev 12.04
Turn on : 26.8962
Width : 4.071
Height : 10.051
Entry
ampl
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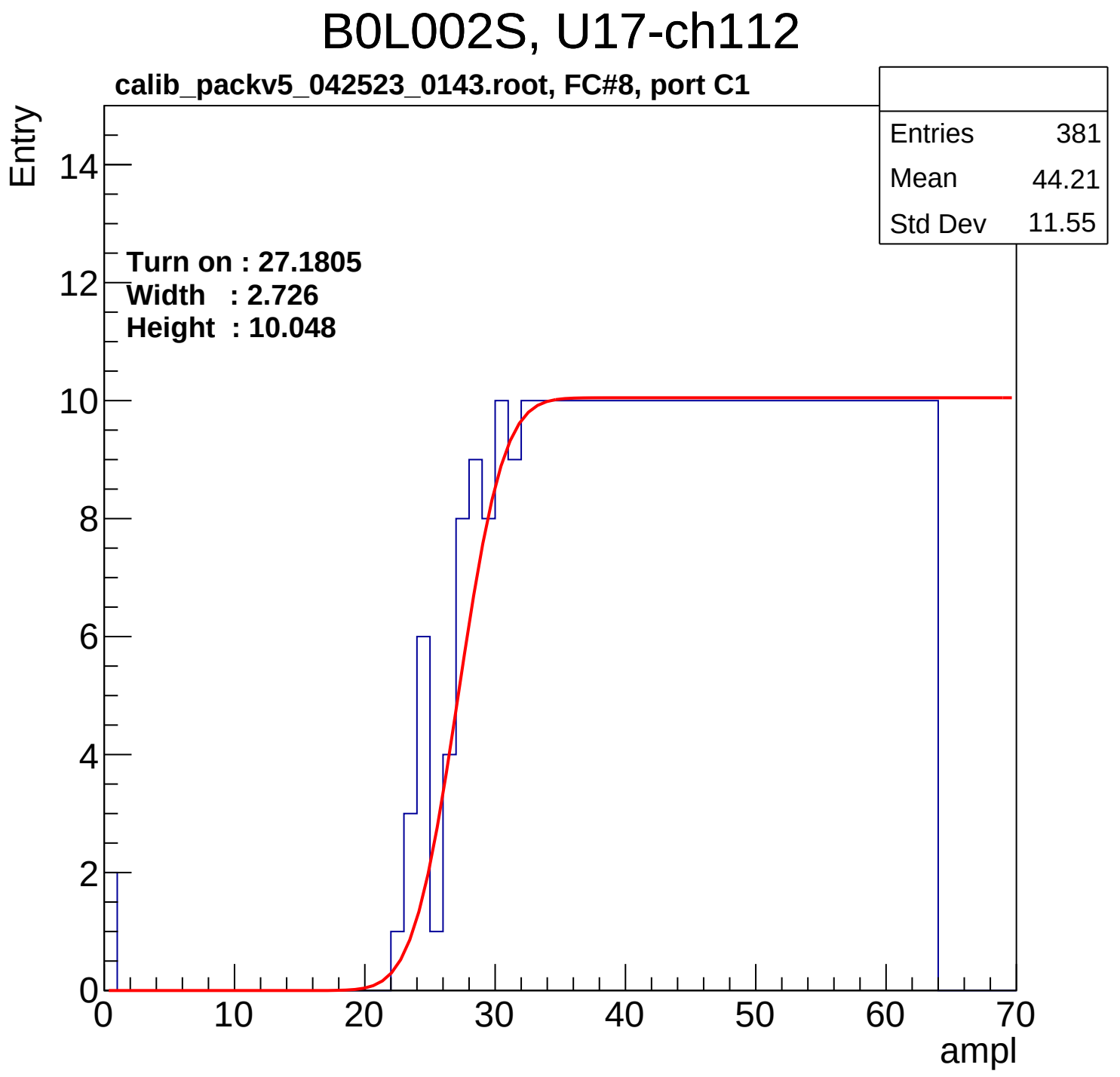
B0L002S, U17-ch112
calib_packv5_042523_0143.root, FC#8, port C1
Entries 381
Mean 44.21
Std Dev 11.55
Turn on : 27.1805
Width : 2.726
Height : 10.048
Entry
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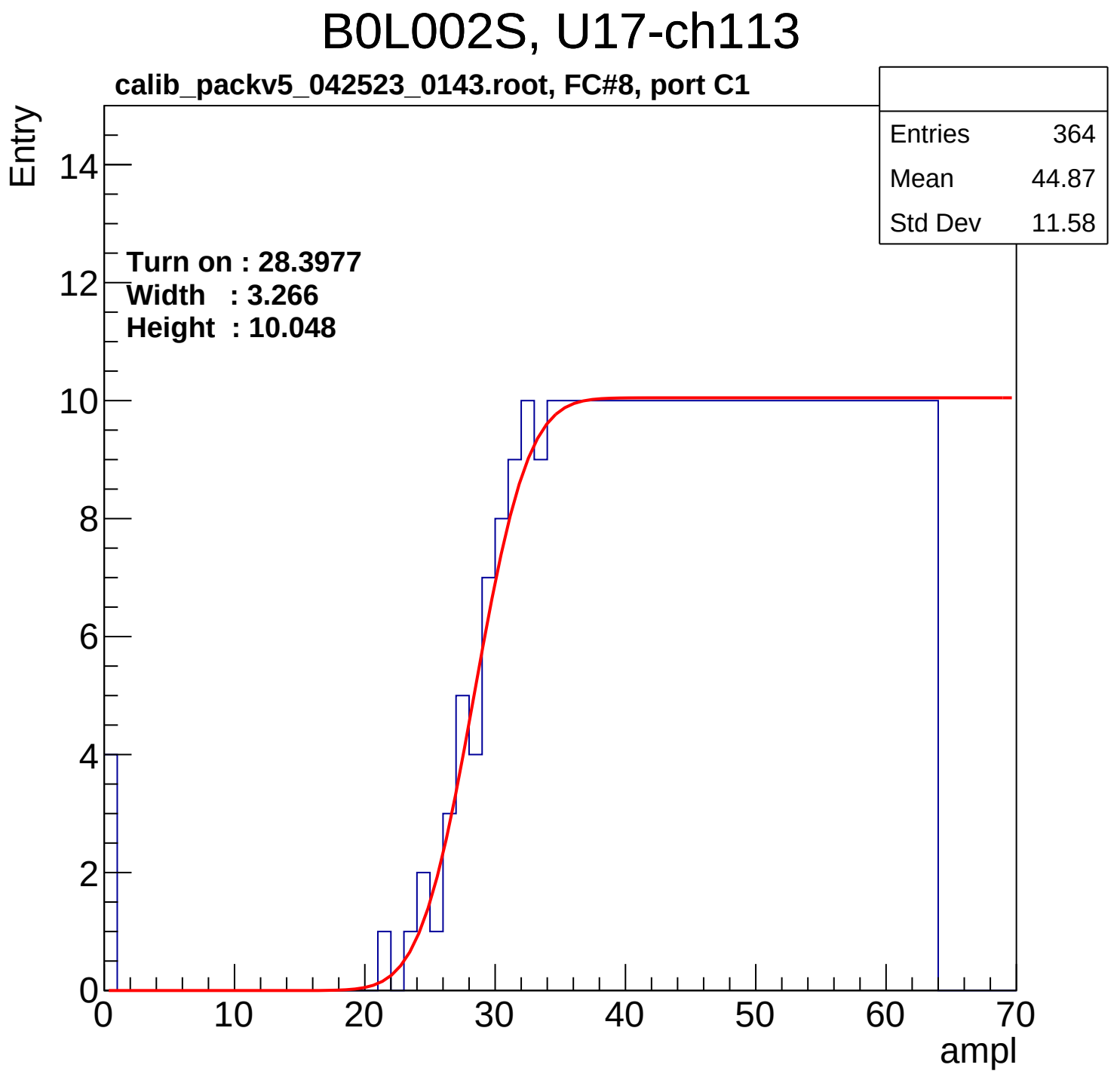
B0L002S, U17-ch113
calib_packv5_042523_0143.root, FC#8, port C1
Entries 364
Mean 44.87
Std Dev 11.58
Turn on : 28.3977
Width : 3.266
Height : 10.048
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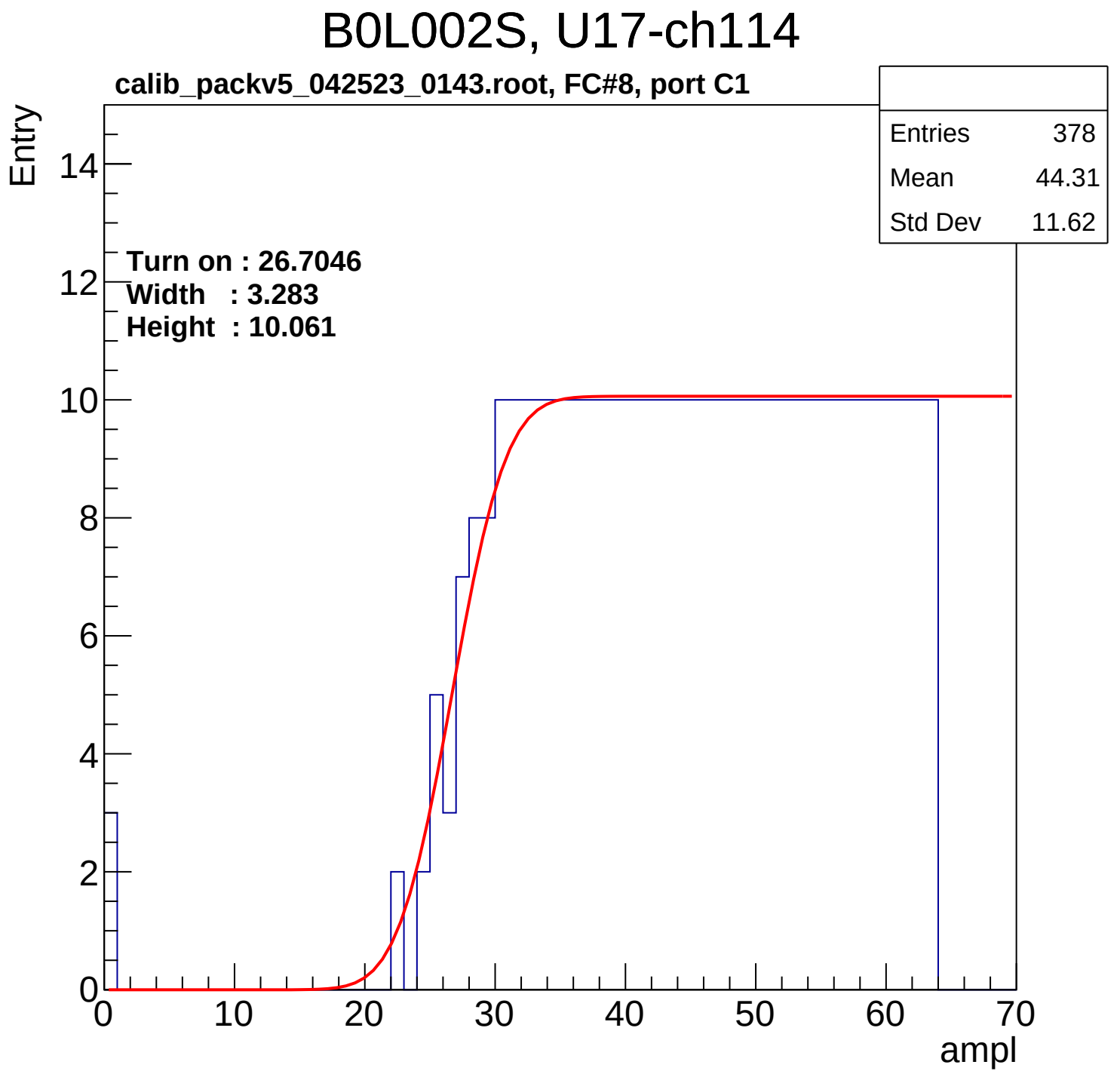
B0L002S, U17-ch114
calib_packv5_042523_0143.root, FC#8, port C1
Entries 378
Mean 44.31
Std Dev 11.62
Turn on : 26.7046
Width : 3.283
Height : 10.061
Entry
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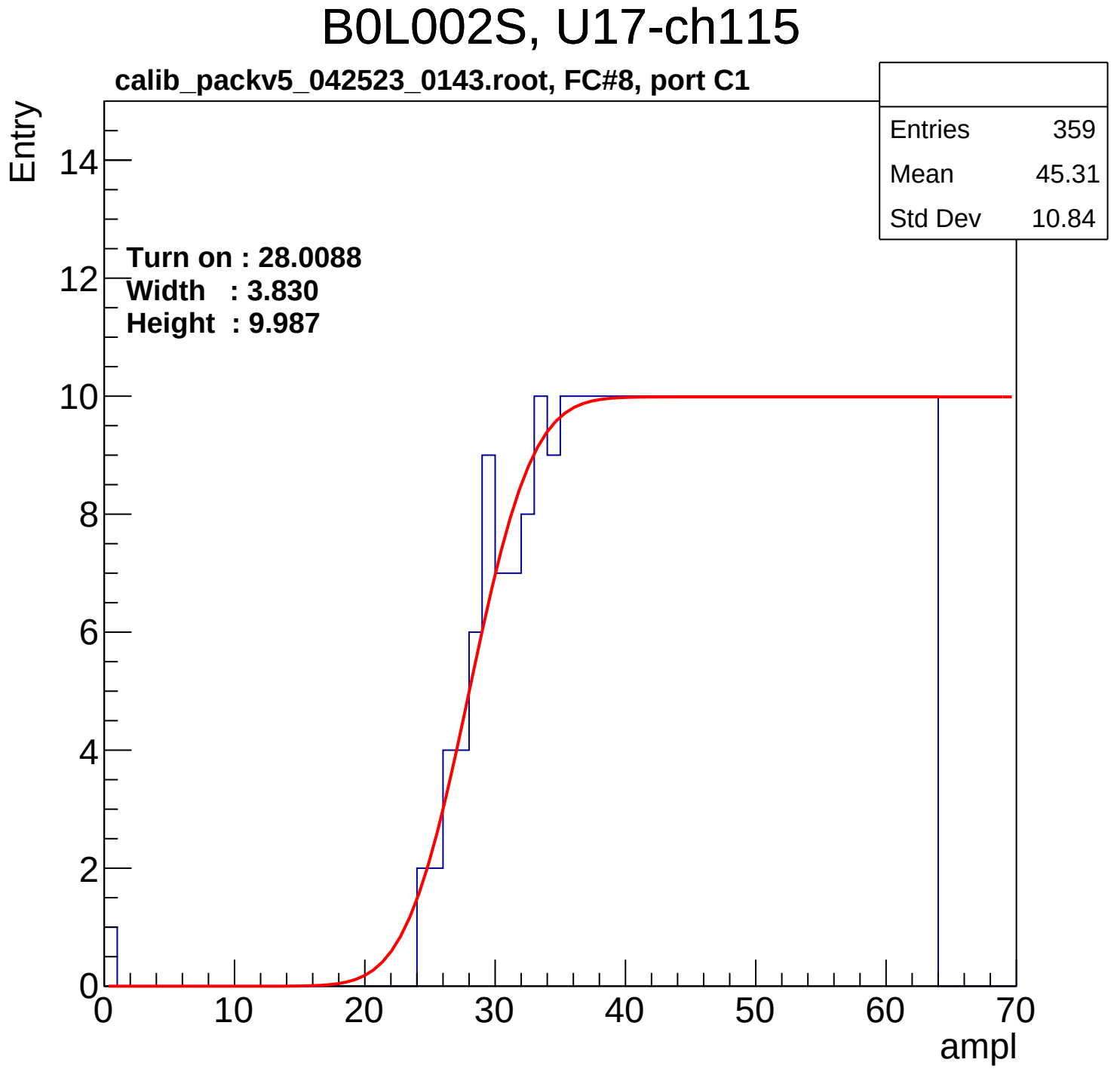
B0L002S, U17-ch115
calib_packv5_042523_0143.root, FC#8, port C1
Entries 359
Mean 45.31
Std Dev 10.84
Turn on : 28.0088
Width : 3.830
Height : 9.987
Entry
ampl
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6
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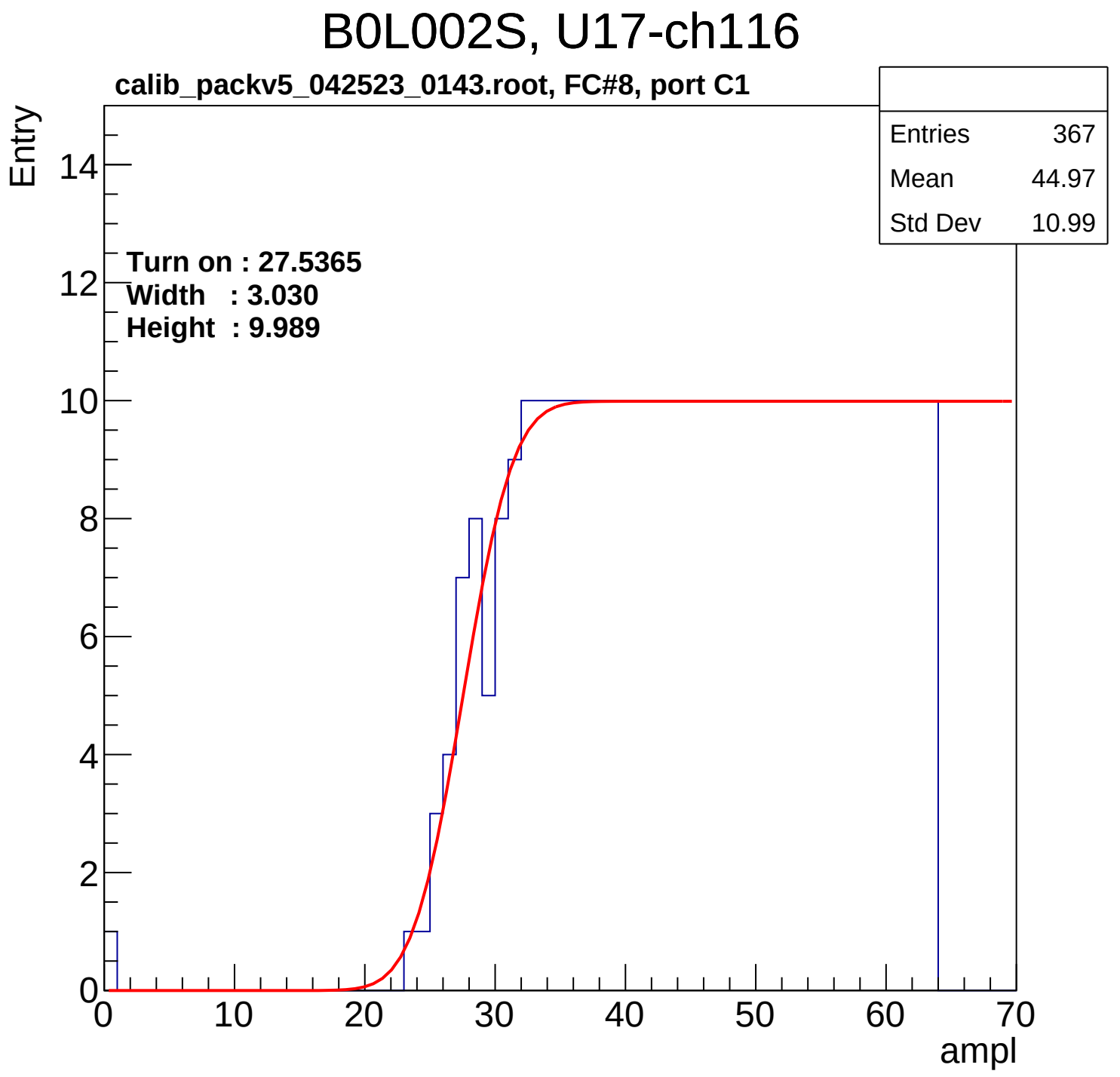
B0L002S, U17-ch116
calib_packv5_042523_0143.root, FC#8, port C1
Entries 367
Mean 44.97
Std Dev 10.99
Turn on : 27.5365
Width : 3.030
Height : 9.989
Entry
ampl
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2
4
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8
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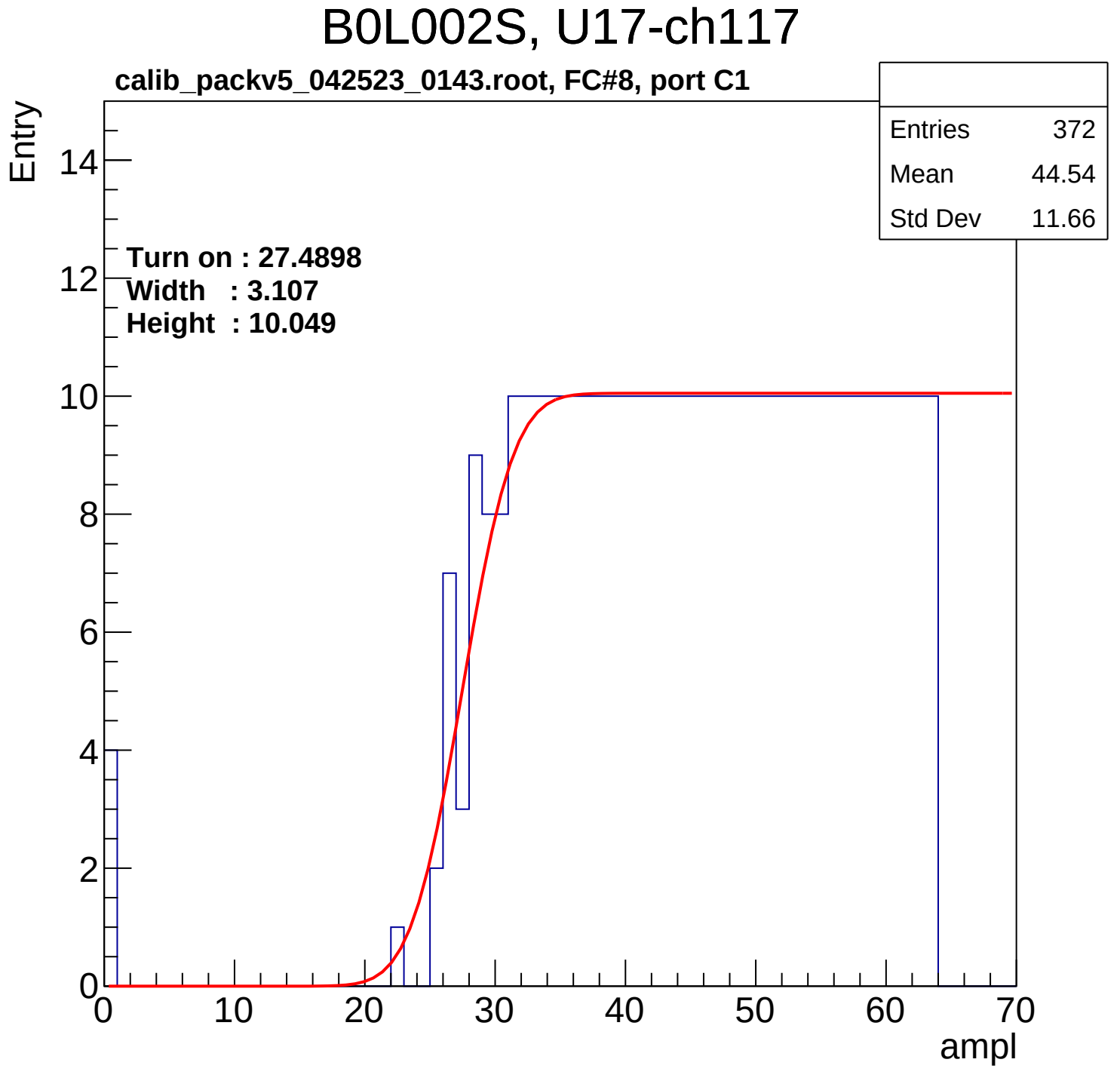
B0L002S, U17-ch117
calib_packv5_042523_0143.root, FC#8, port C1
Entries 372
Mean 44.54
Std Dev 11.66
Turn on : 27.4898
Width : 3.107
Height : 10.049
Entry
ampl
0
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4
6
8
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12
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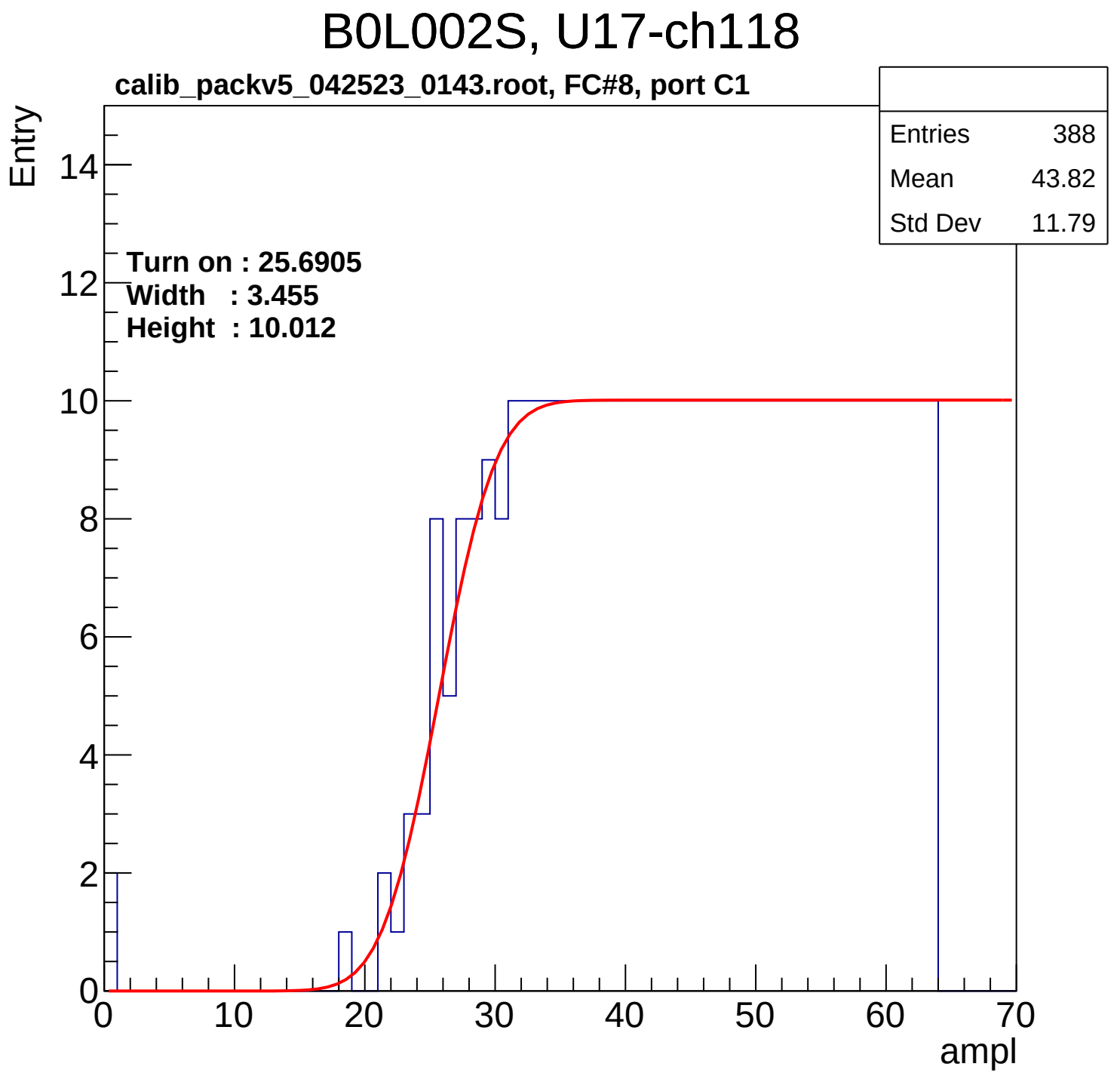
B0L002S, U17-ch118
calib_packv5_042523_0143.root, FC#8, port C1
Entries 388
Mean 43.82
Std Dev 11.79
Turn on : 25.6905
Width : 3.455
Height : 10.012
Entry
ampl
0
2
4
6
8
10
12
14
0
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20
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40
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60
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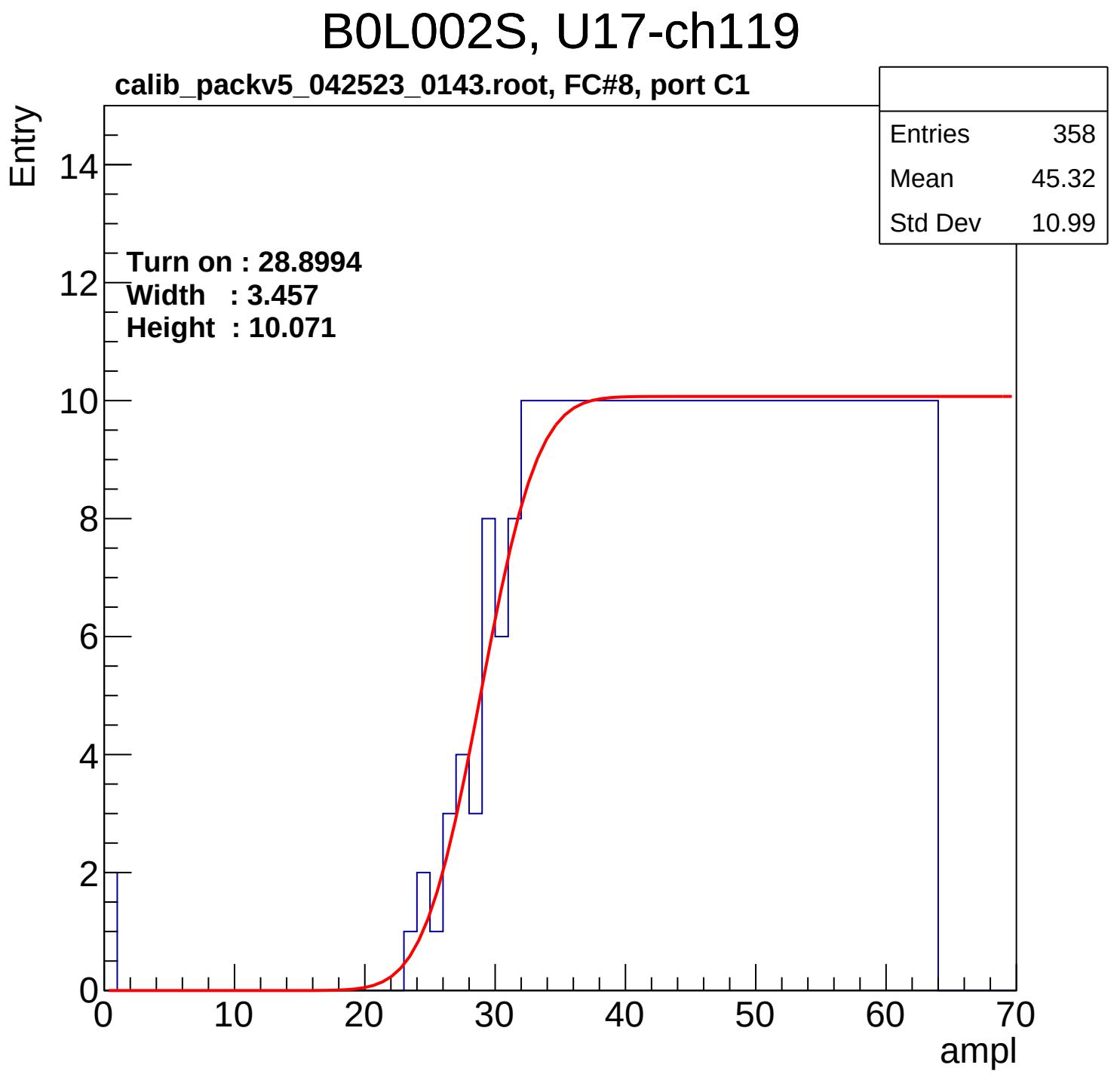
B0L002S, U17-ch119
calib_packv5_042523_0143.root, FC#8, port C1
Entries 358
Mean 45.32
Std Dev 10.99
Turn on : 28.8994
Width : 3.457
Height : 10.071
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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40
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60
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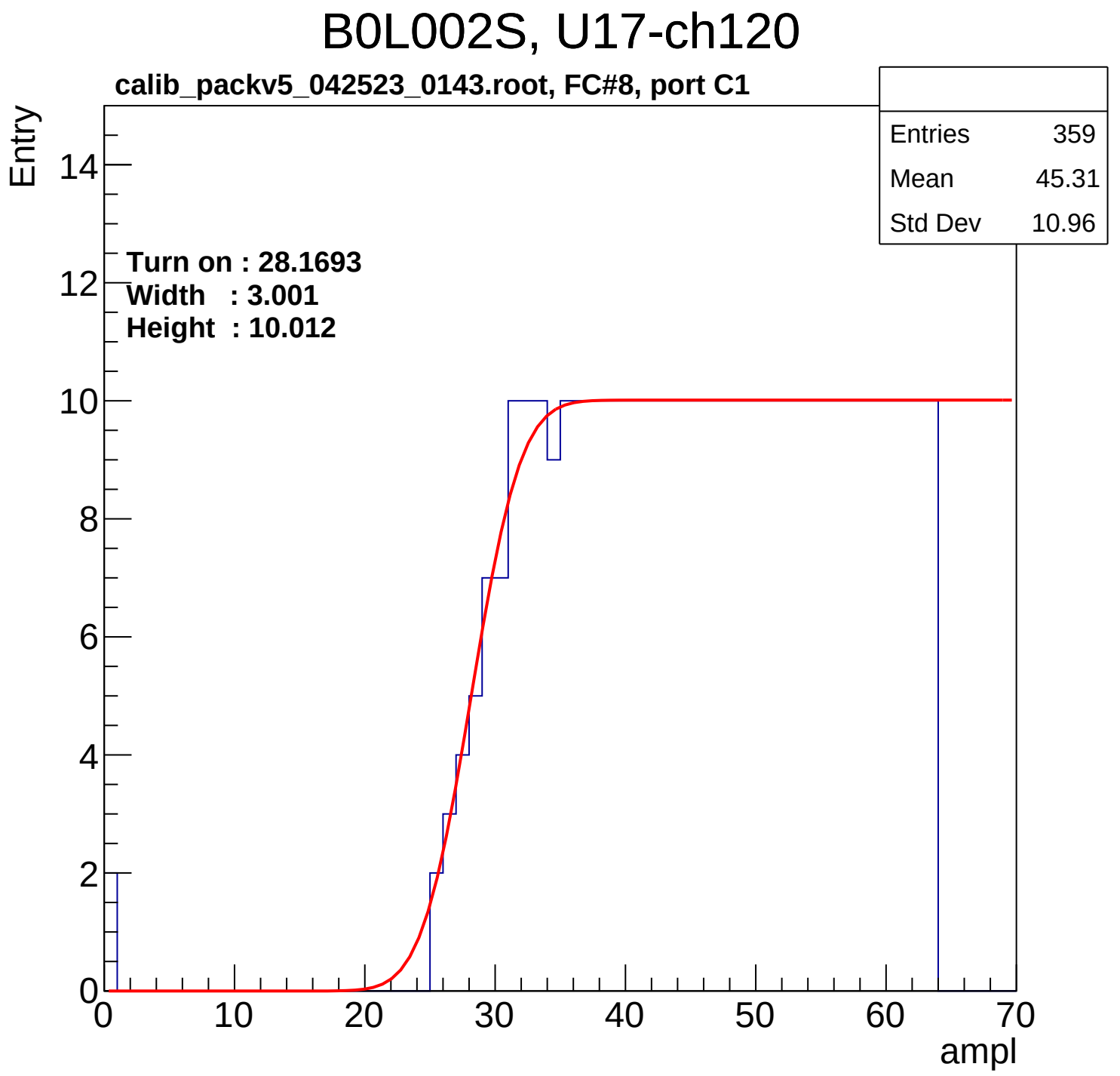
B0L002S, U17-ch120
calib_packv5_042523_0143.root, FC#8, port C1
Entries 359
Mean 45.31
Std Dev 10.96
Turn on : 28.1693
Width : 3.001
Height : 10.012
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
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60
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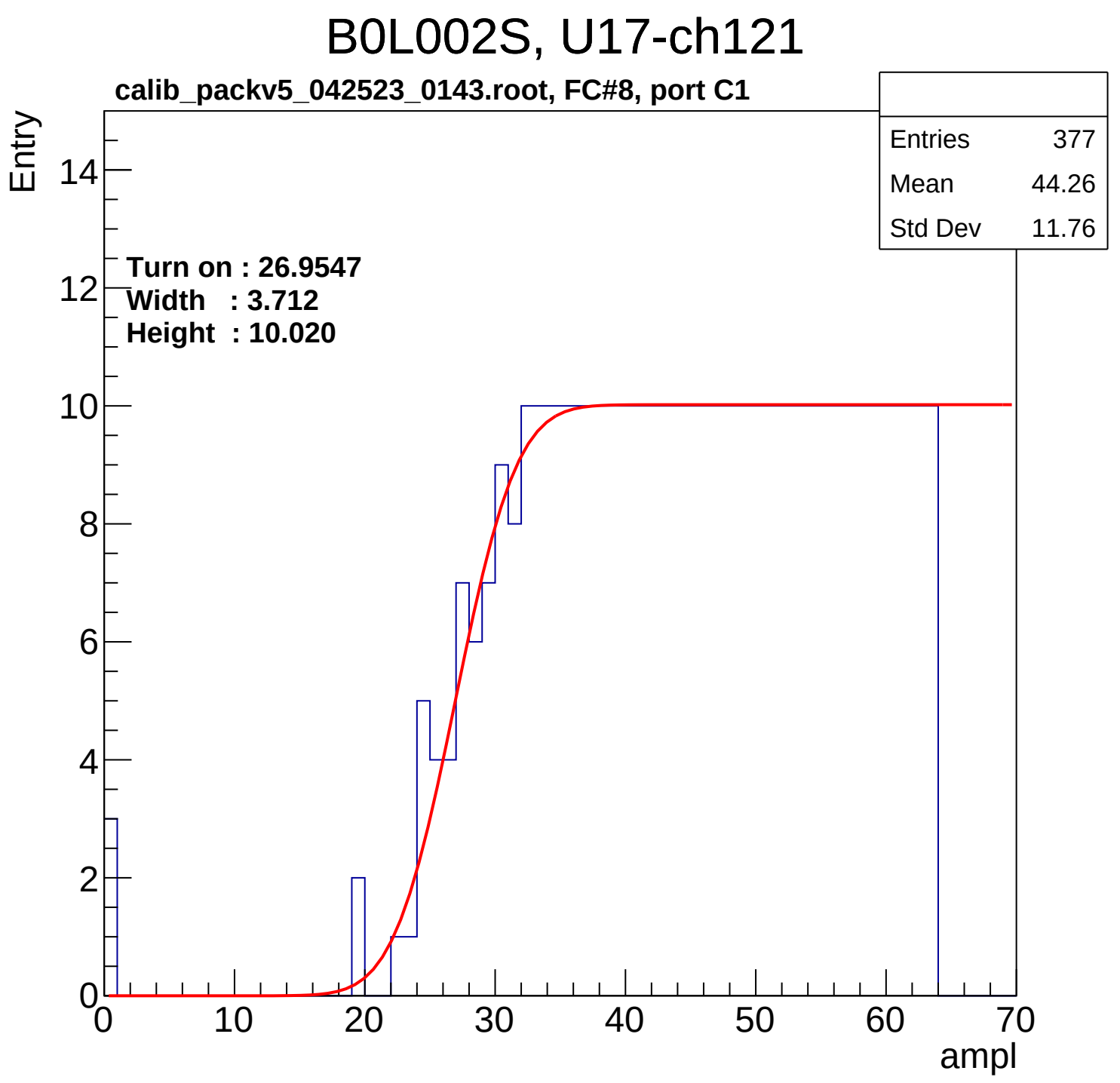
B0L002S, U17-ch121
calib_packv5_042523_0143.root, FC#8, port C1
Entries 377
Mean 44.26
Std Dev 11.76
Turn on : 26.9547
Width : 3.712
Height : 10.020
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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40
50
60
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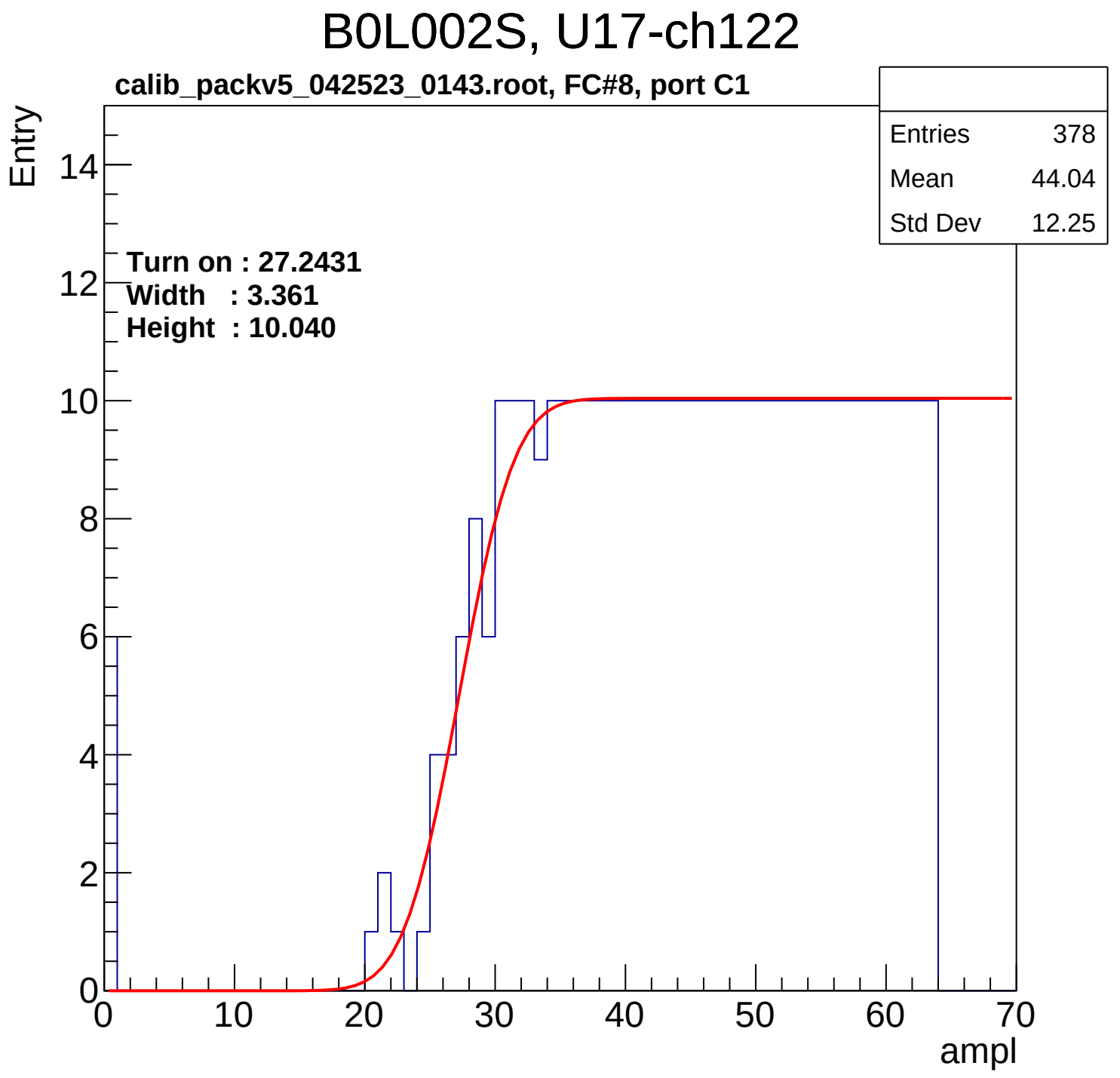
B0L002S, U17-ch122
calib_packv5_042523_0143.root, FC#8, port C1
Entries 378
Mean 44.04
Std Dev 12.25
Turn on : 27.2431
Width : 3.361
Height : 10.040
Entry
ampl
0
2
4
6
8
10
12
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20
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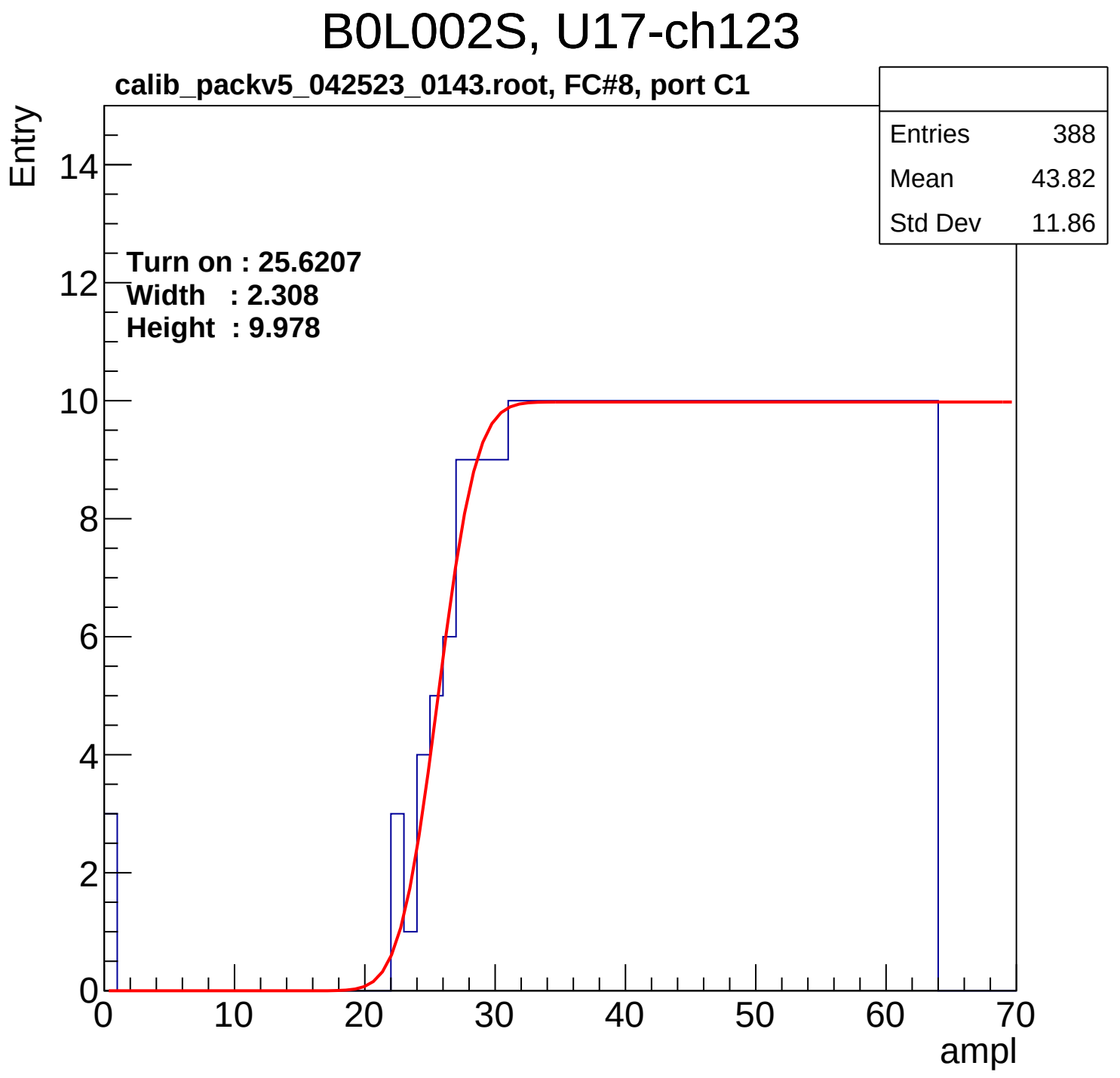
B0L002S, U17-ch123
calib_packv5_042523_0143.root, FC#8, port C1
Entries 388
Mean 43.82
Std Dev 11.86
Turn on : 25.6207
Width : 2.308
Height : 9.978
Entry
ampl
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2
4
6
8
10
12
14
0
10
20
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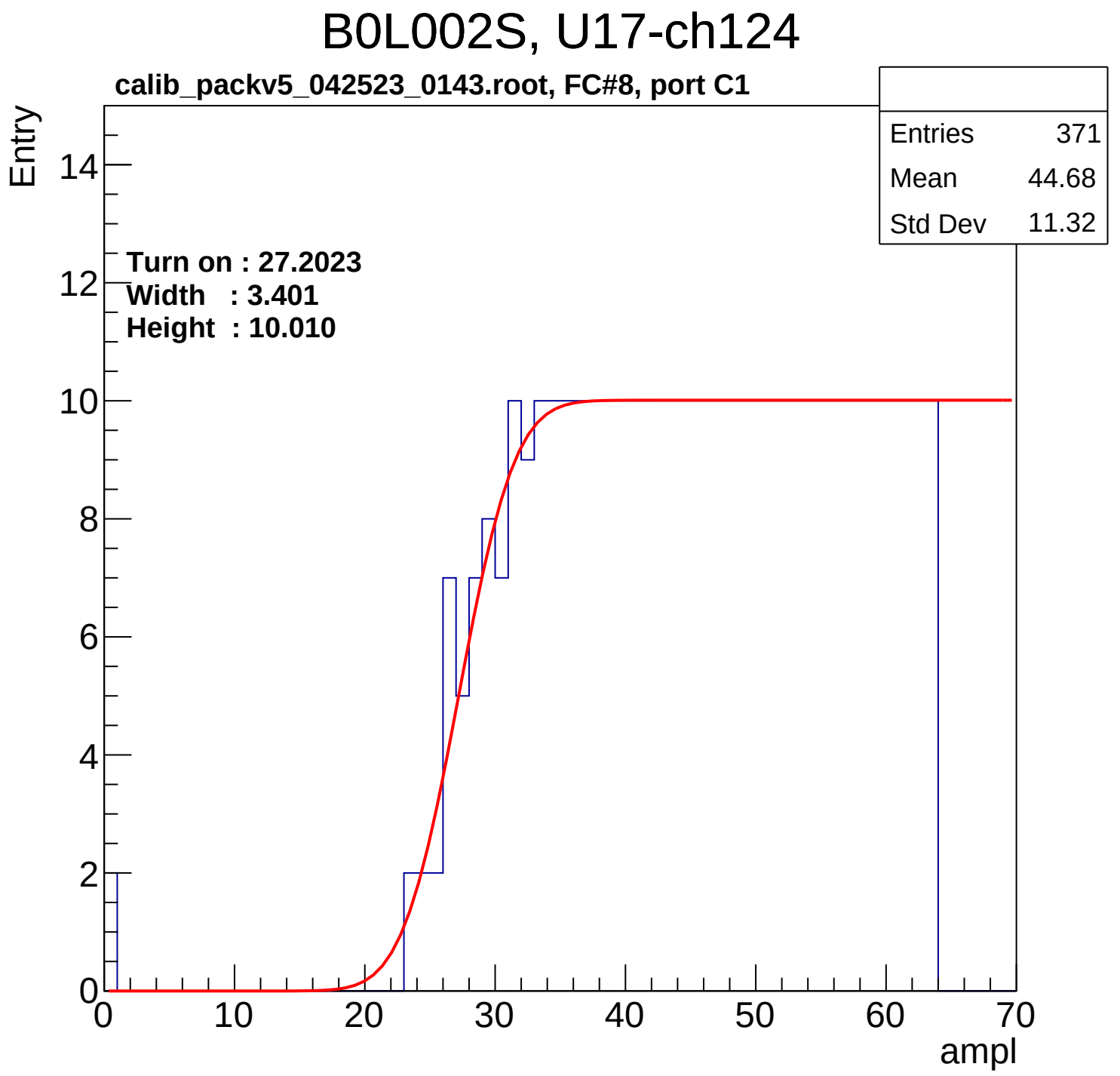
40
50
60
70


B0L002S, U17-ch124
calib_packv5_042523_0143.root, FC#8, port C1
Entries 371
Mean 44.68
Std Dev 11.32
Turn on : 27.2023
Width : 3.401
Height : 10.010
Entry
ampl
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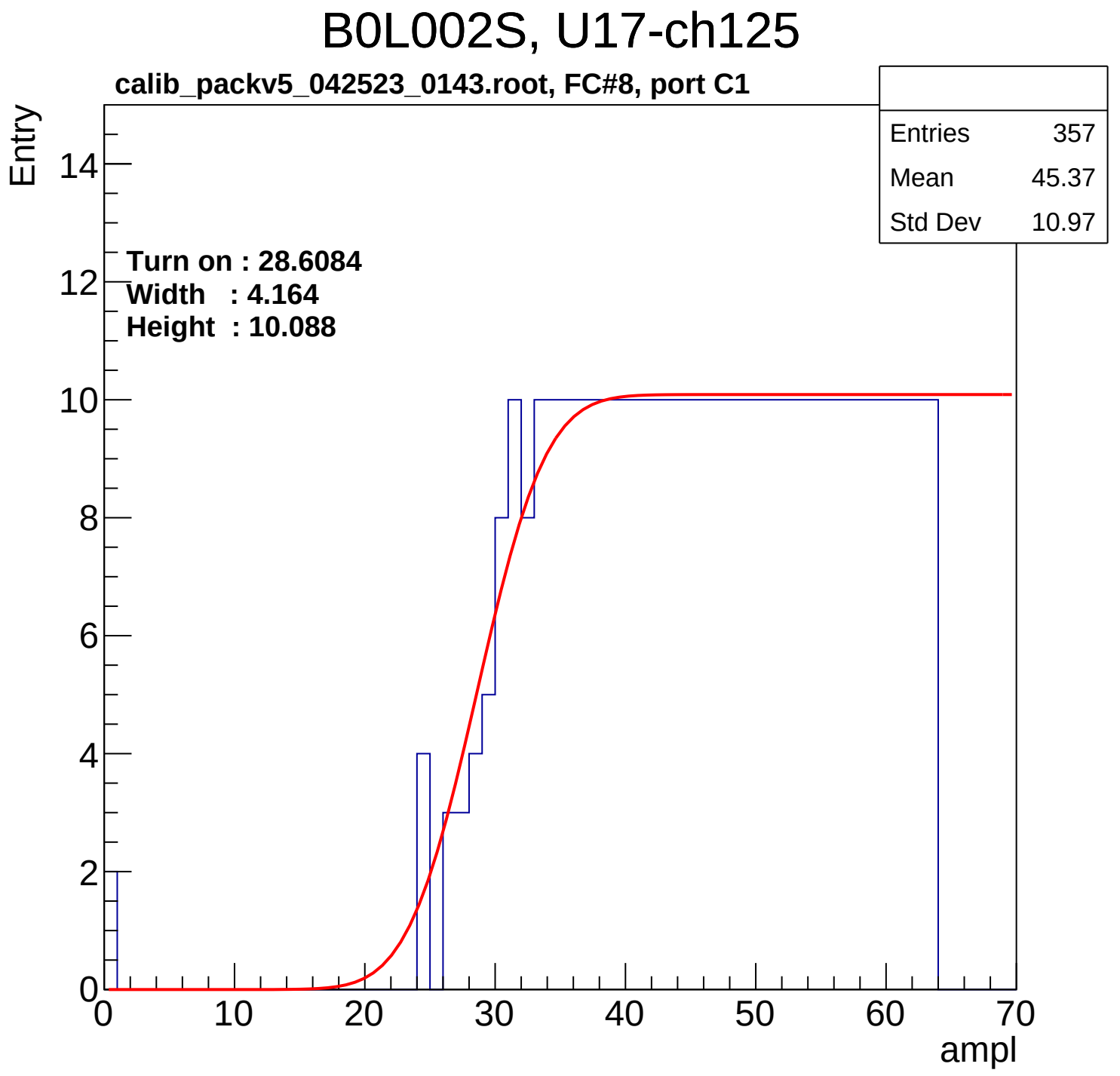
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L002S, U17-ch125
calib_packv5_042523_0143.root, FC#8, port C1
Entries 357
Mean 45.37
Std Dev 10.97
Turn on : 28.6084
Width : 4.164
Height : 10.088
Entry
ampl
0
2
4
6
8
10
12
14
0
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20
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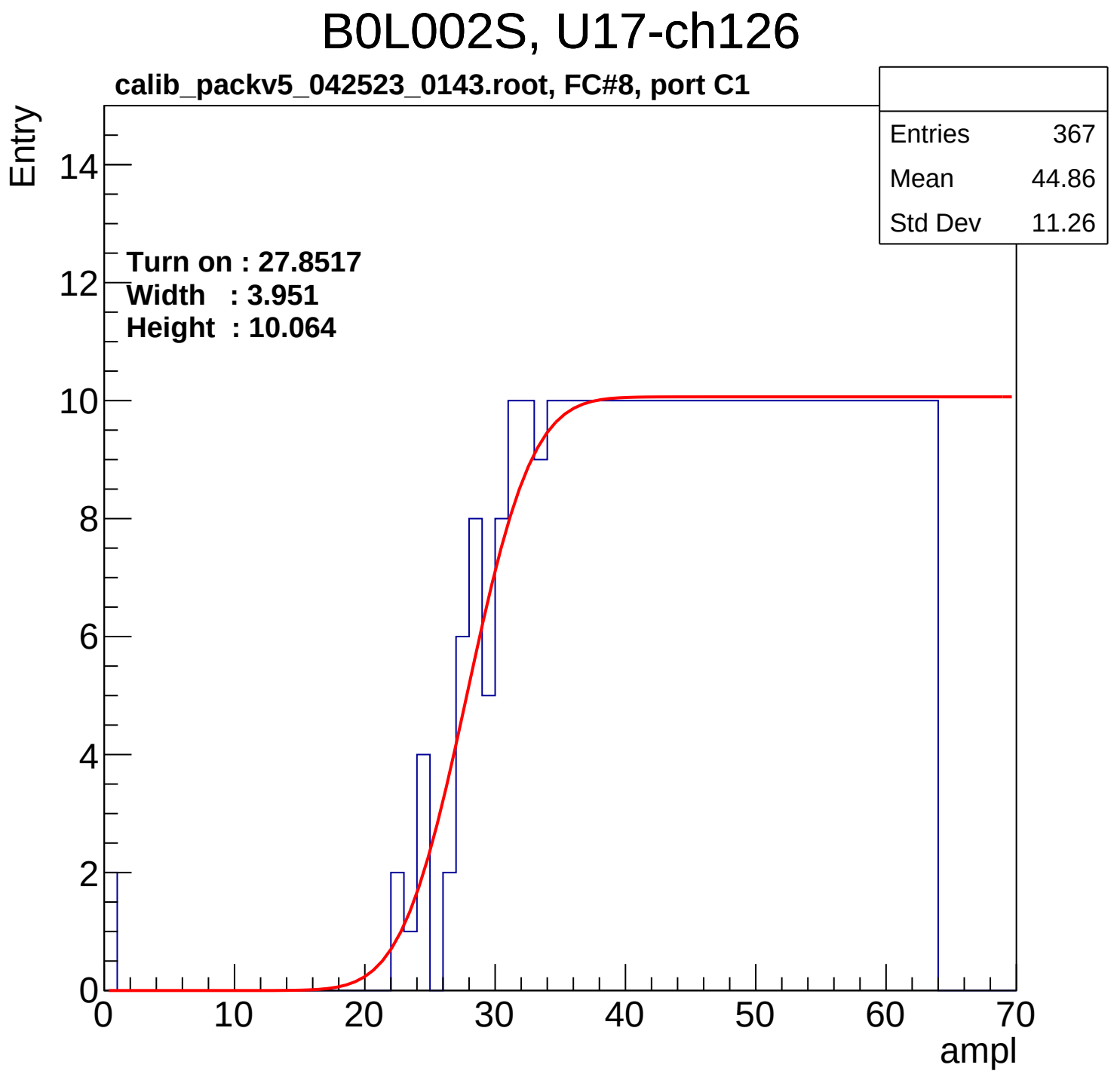
40
50
60
70


B0L002S, U17-ch126
calib_packv5_042523_0143.root, FC#8, port C1
Entries 367
Mean 44.86
Std Dev 11.26
Turn on : 27.8517
Width : 3.951
Height : 10.064
Entry
ampl
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4
6
8
10
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0
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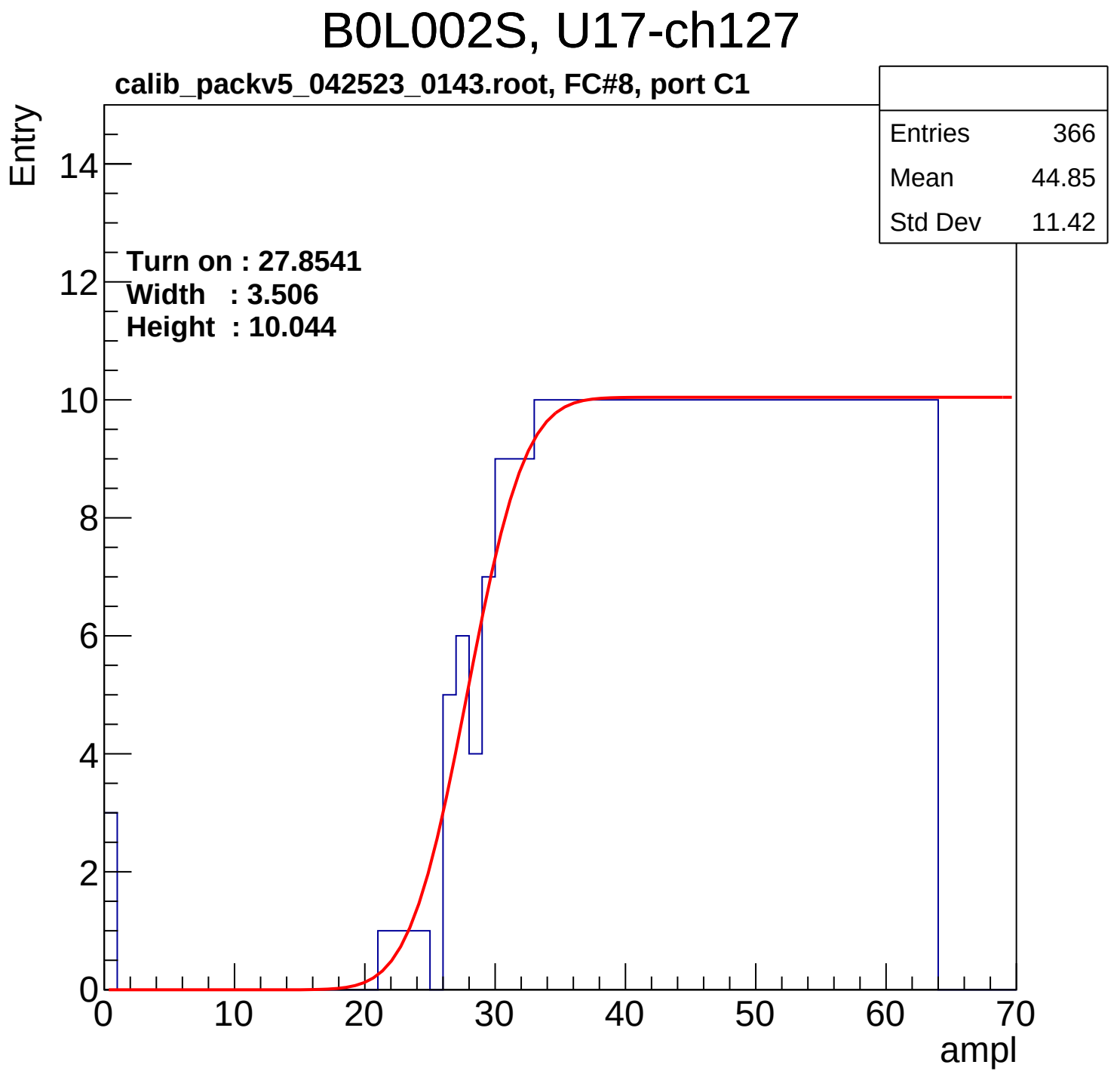
B0L002S, U17-ch127
calib_packv5_042523_0143.root, FC#8, port C1
Entries 366
Mean 44.85
Std Dev 11.42
Turn on : 27.8541
Width : 3.506
Height : 10.044
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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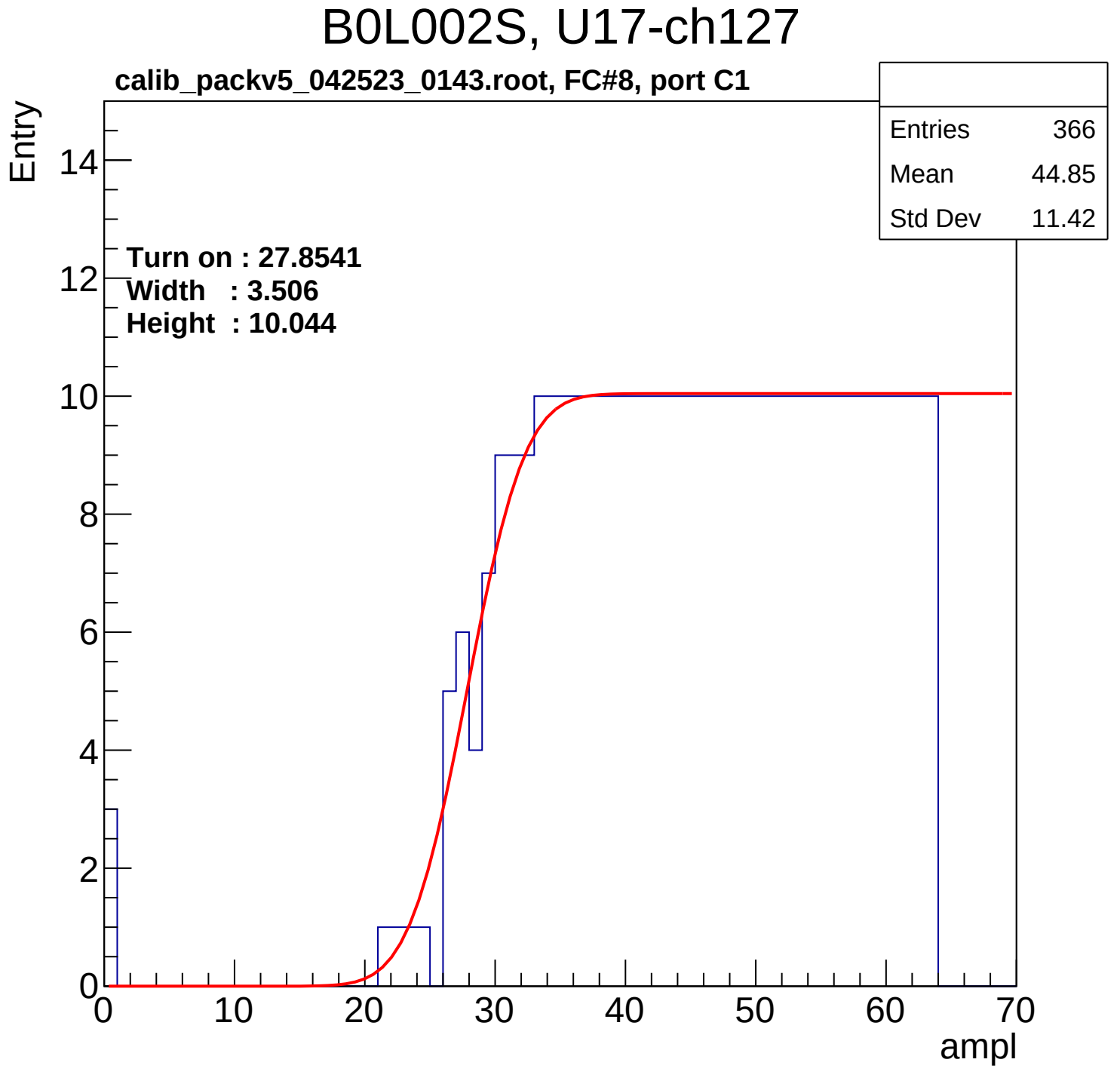
40
50
60
70


B0L002S, U17-ch127
calib_packv5_042523_0143.root, FC#8, port C1
Entries 366
Mean 44.85
Std Dev 11.42
Turn on : 27.8541
Width : 3.506
Height : 10.044
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70