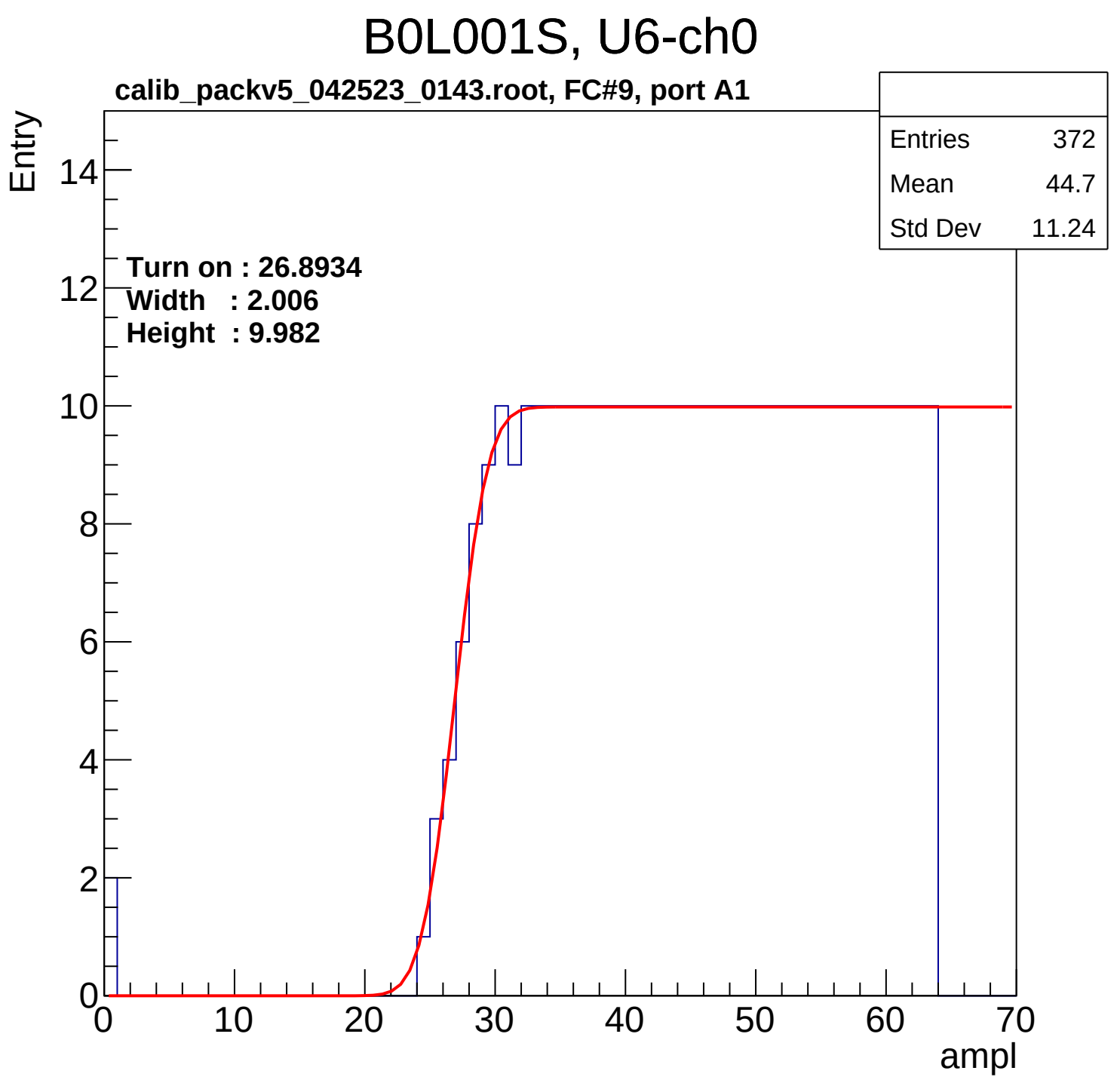
B0L001S, U6-ch0
calib_packv5_042523_0143.root, FC#9, port A1
Entries 372
Mean 44.7
Std Dev 11.24
Turn on : 26.8934
Width : 2.006
Height : 9.982
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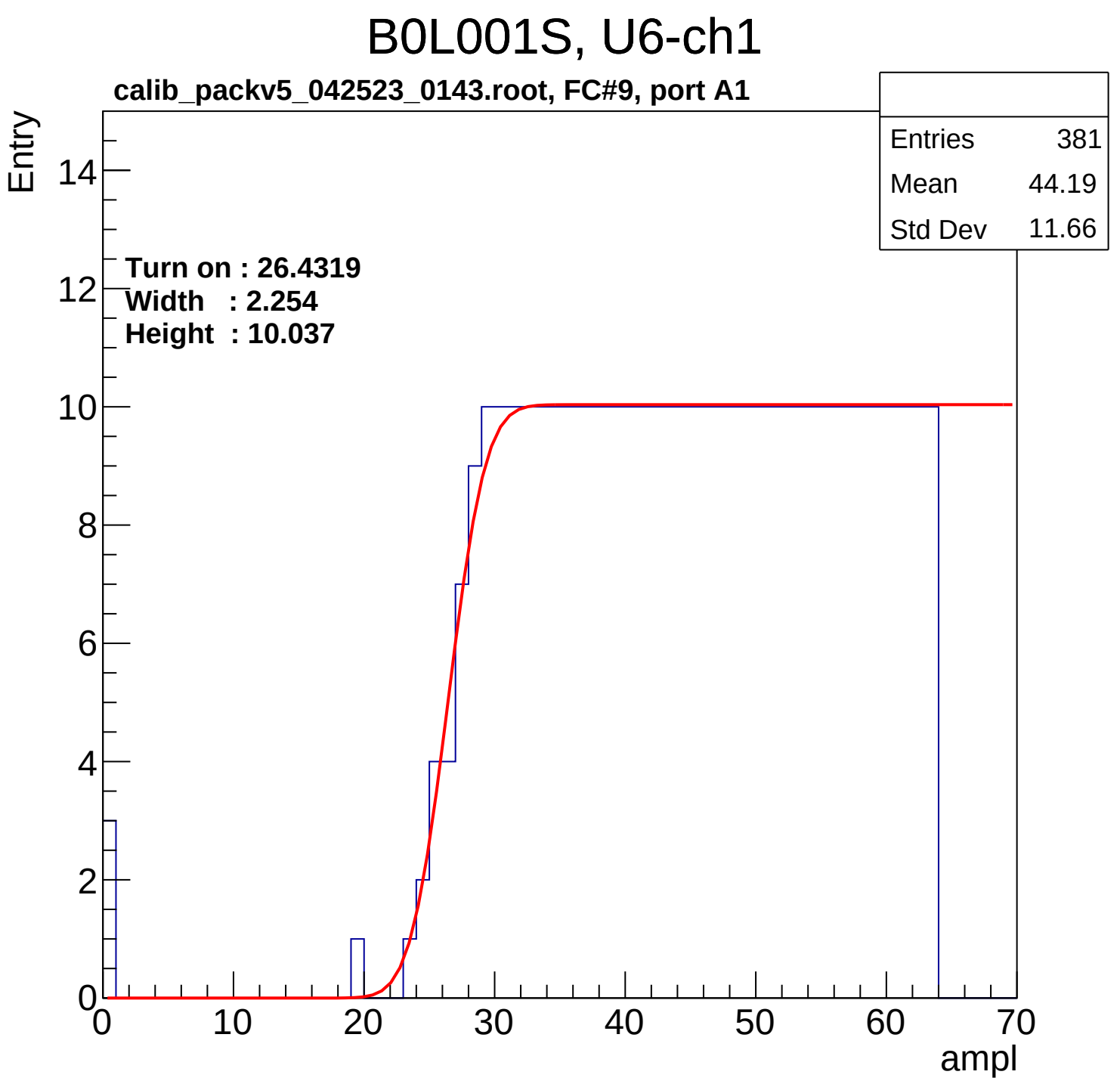
B0L001S, U6-ch1
calib_packv5_042523_0143.root, FC#9, port A1
Entries 381
Mean 44.19
Std Dev 11.66
Turn on : 26.4319
Width : 2.254
Height : 10.037
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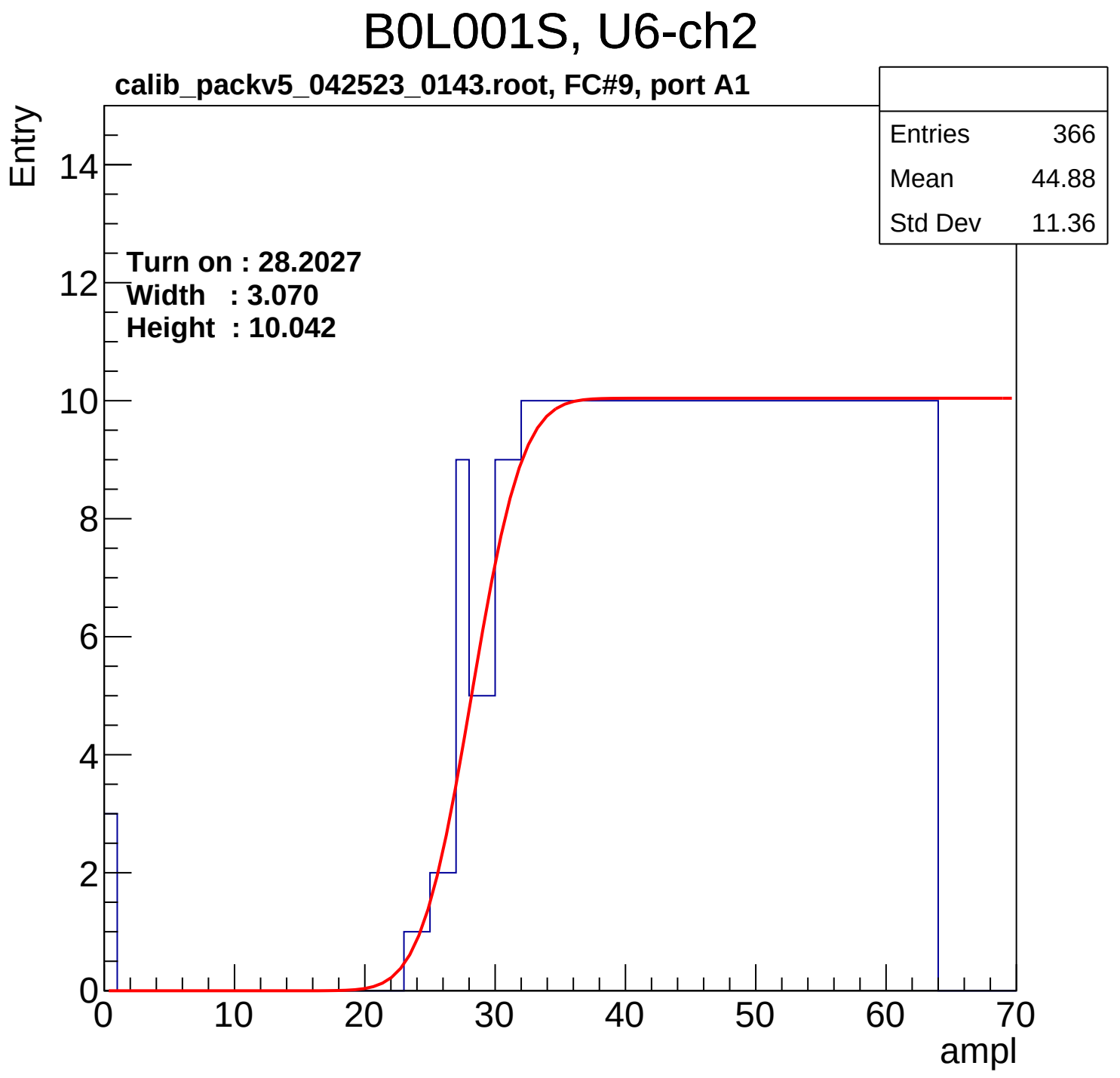
B0L001S, U6-ch2
calib_packv5_042523_0143.root, FC#9, port A1
Entries 366
Mean 44.88
Std Dev 11.36
Turn on : 28.2027
Width : 3.070
Height : 10.042
Entry
ampl
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4
6
8
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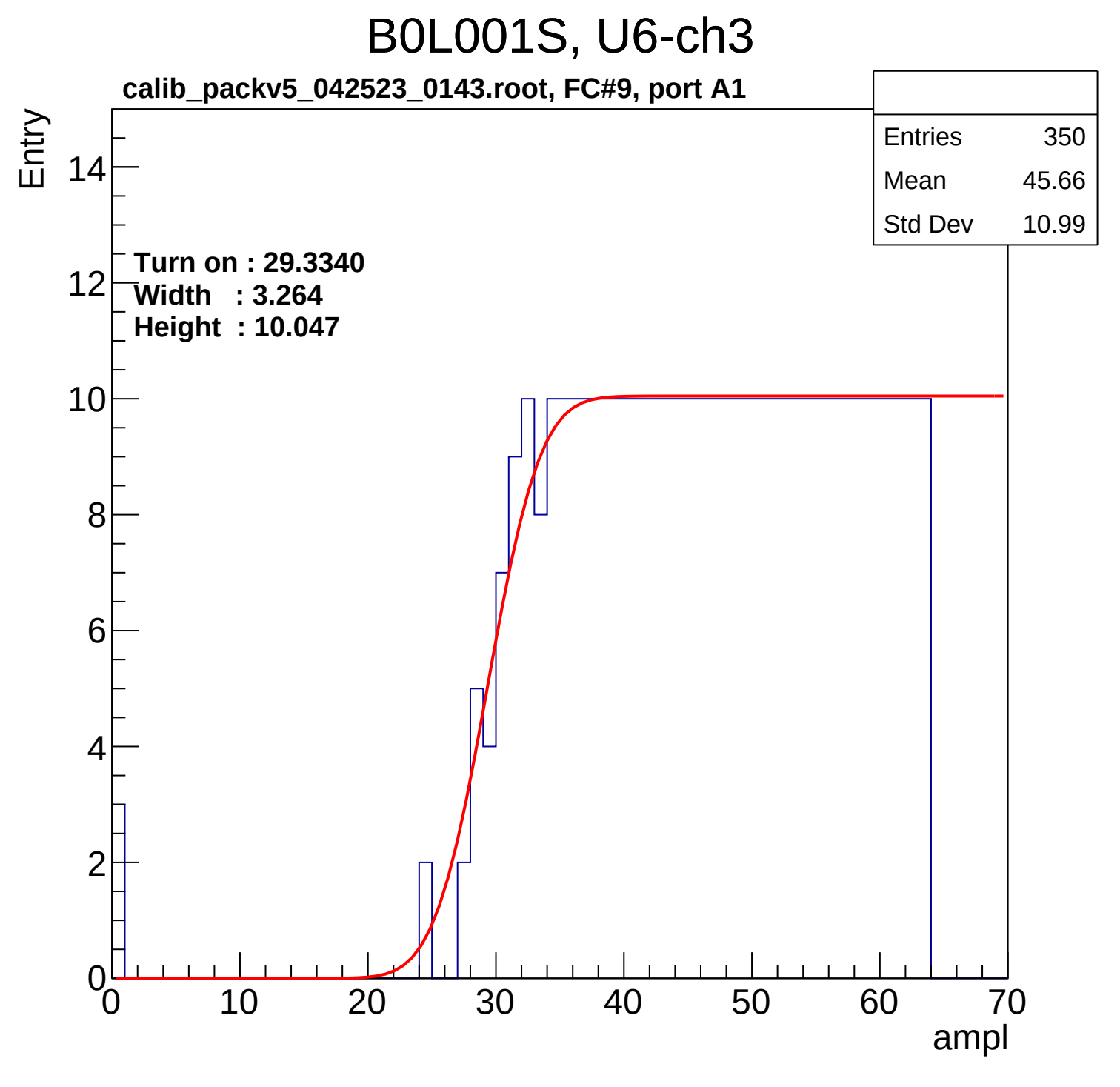
B0L001S, U6-ch3
calib_packv5_042523_0143.root, FC#9, port A1
Entries 350
Mean 45.66
Std Dev 10.99
Turn on : 29.3340
Width : 3.264
Height : 10.047
Entry
ampl
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2
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6
8
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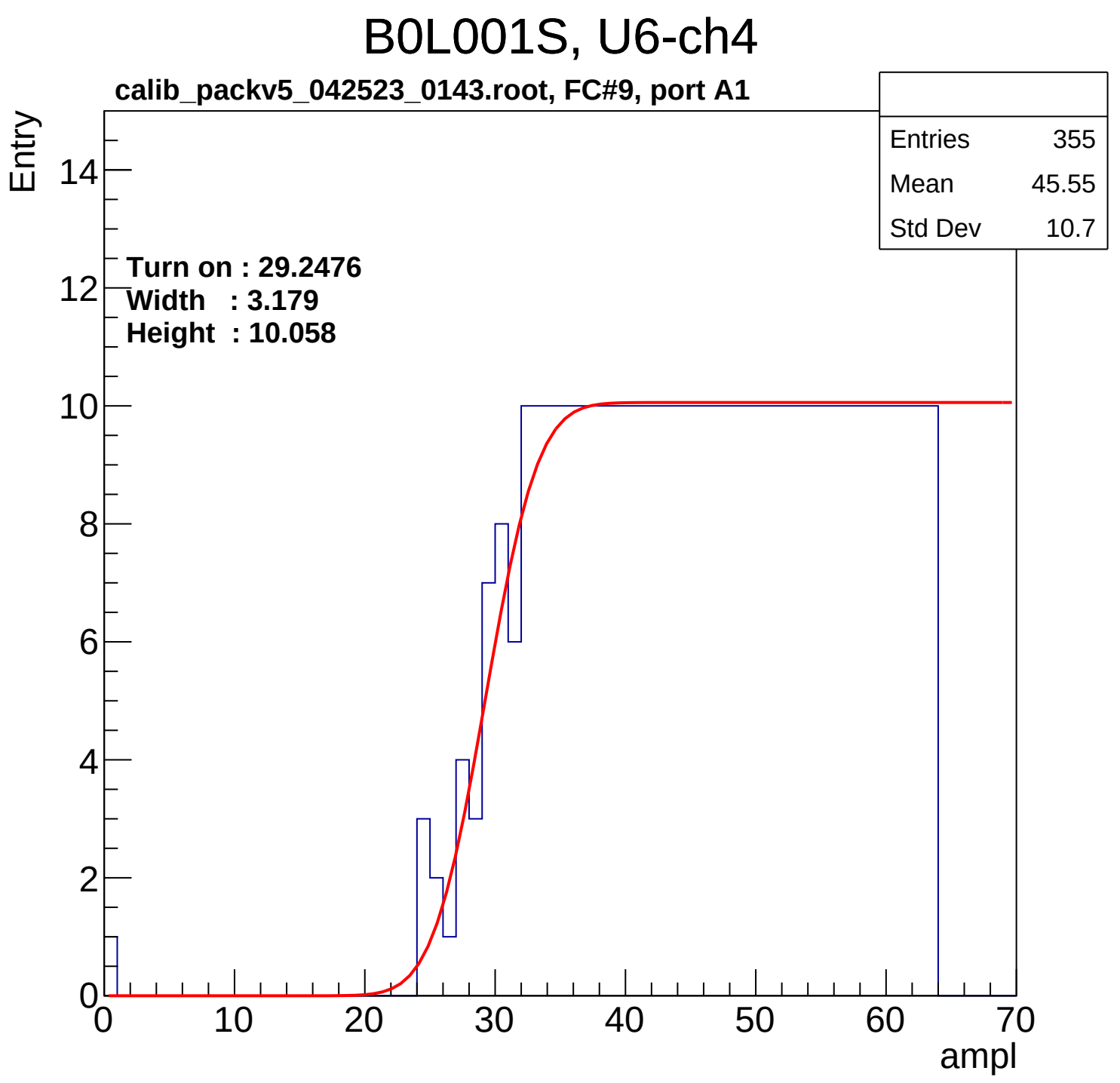
B0L001S, U6-ch4
calib_packv5_042523_0143.root, FC#9, port A1
Entries 355
Mean 45.55
Std Dev 10.7
Turn on : 29.2476
Width : 3.179
Height : 10.058
Entry
ampl
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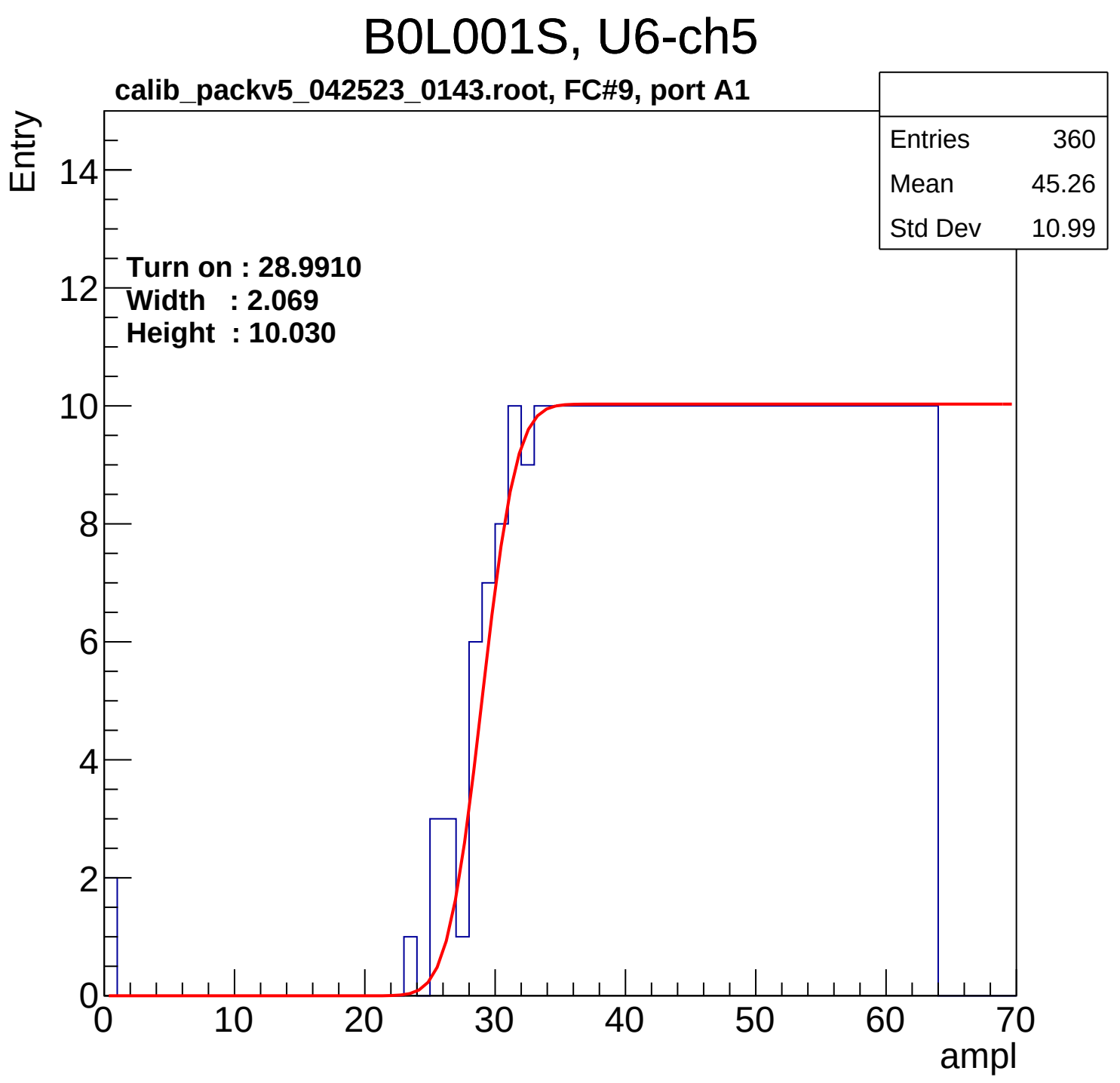
B0L001S, U6-ch5
calib_packv5_042523_0143.root, FC#9, port A1
Entries 360
Mean 45.26
Std Dev 10.99
Turn on : 28.9910
Width : 2.069
Height : 10.030
Entry
ampl
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4
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8
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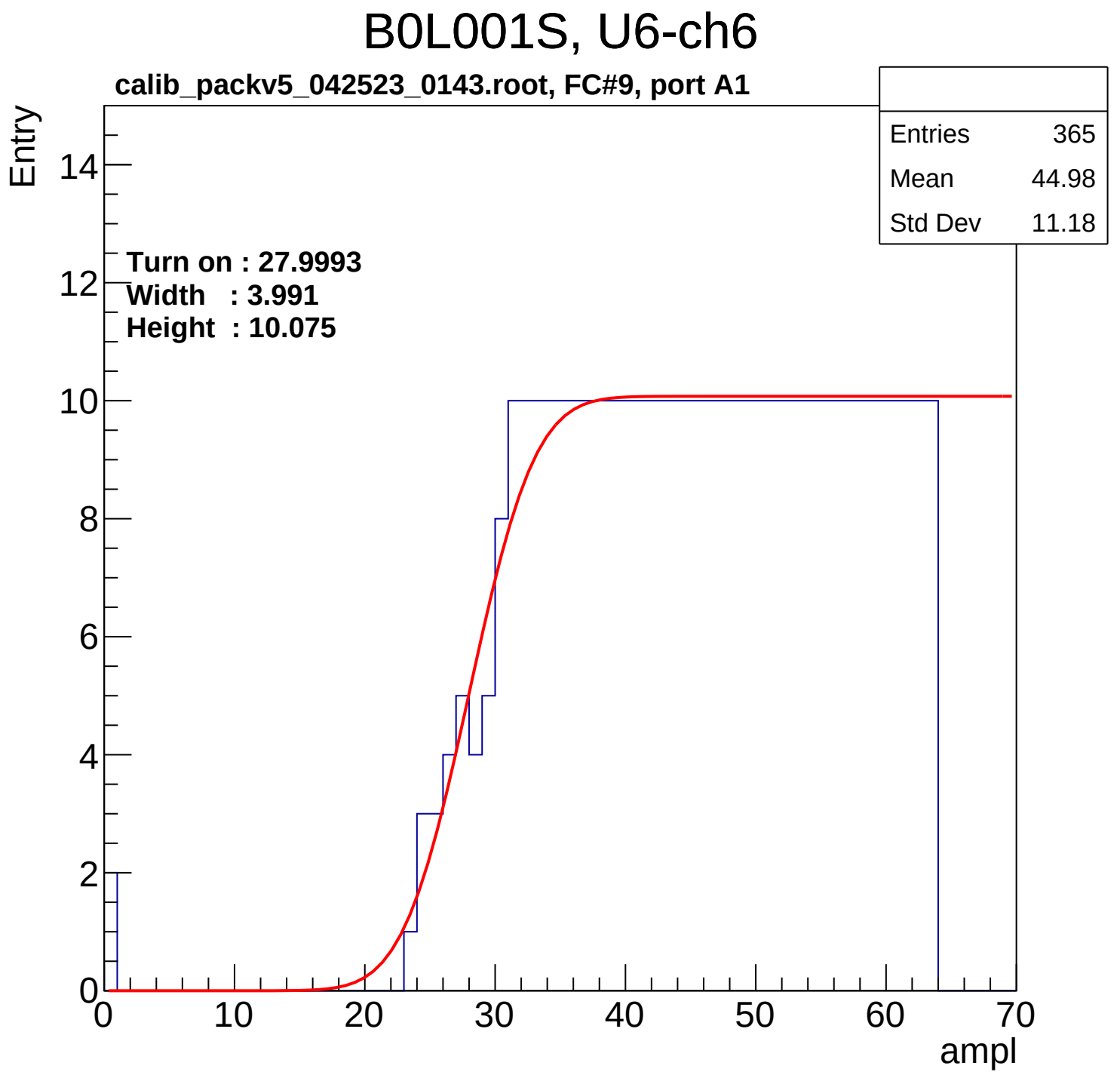
B0L001S, U6-ch6
calib_packv5_042523_0143.root, FC#9, port A1
Entries 365
Mean 44.98
Std Dev 11.18
Turn on : 27.9993
Width : 3.991
Height : 10.075
Entry
ampl
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2
4
6
8
10
12
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0
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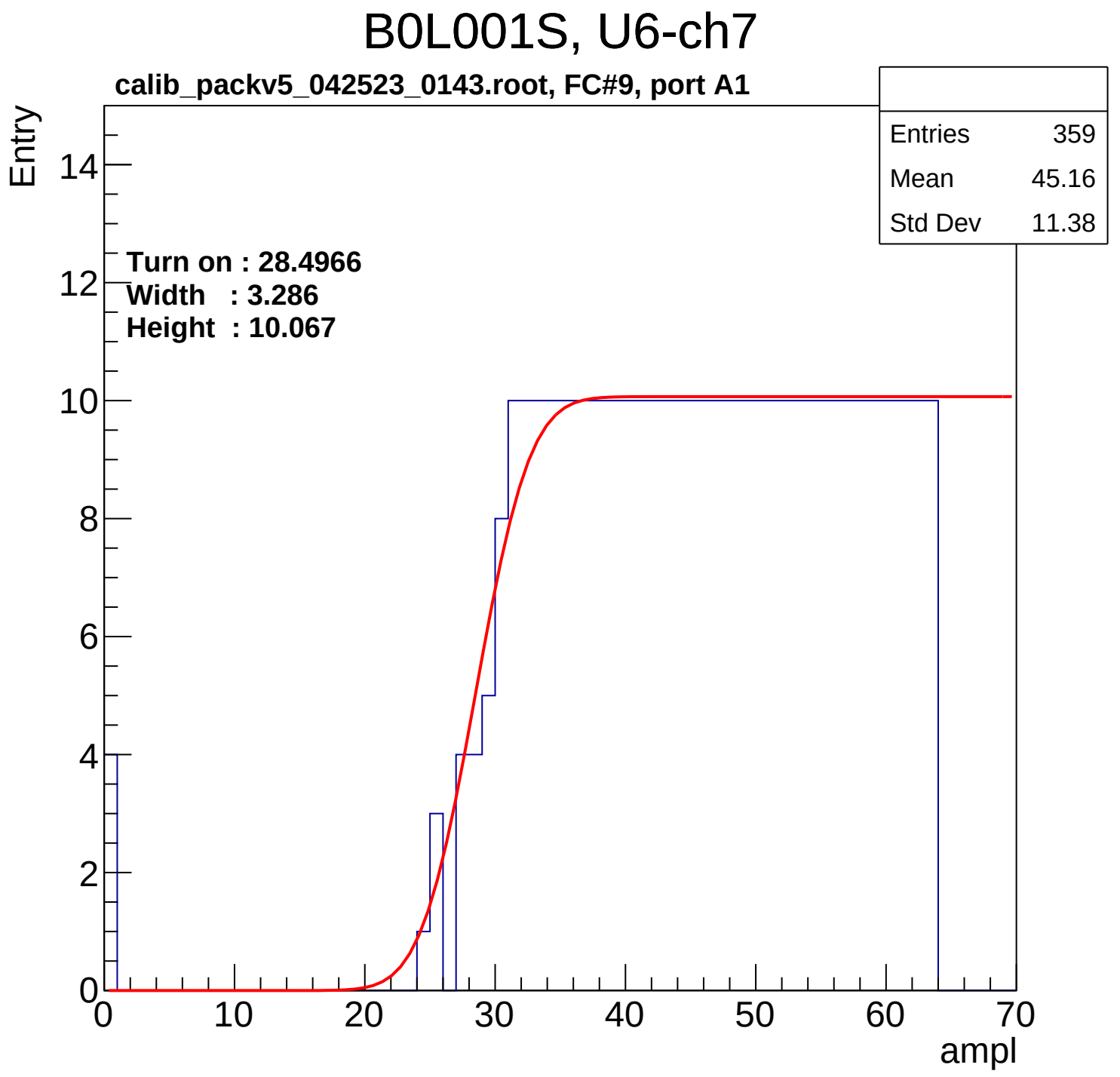
B0L001S, U6-ch7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 359
Mean 45.16
Std Dev 11.38
Turn on : 28.4966
Width : 3.286
Height : 10.067
Entry
ampl
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6
8
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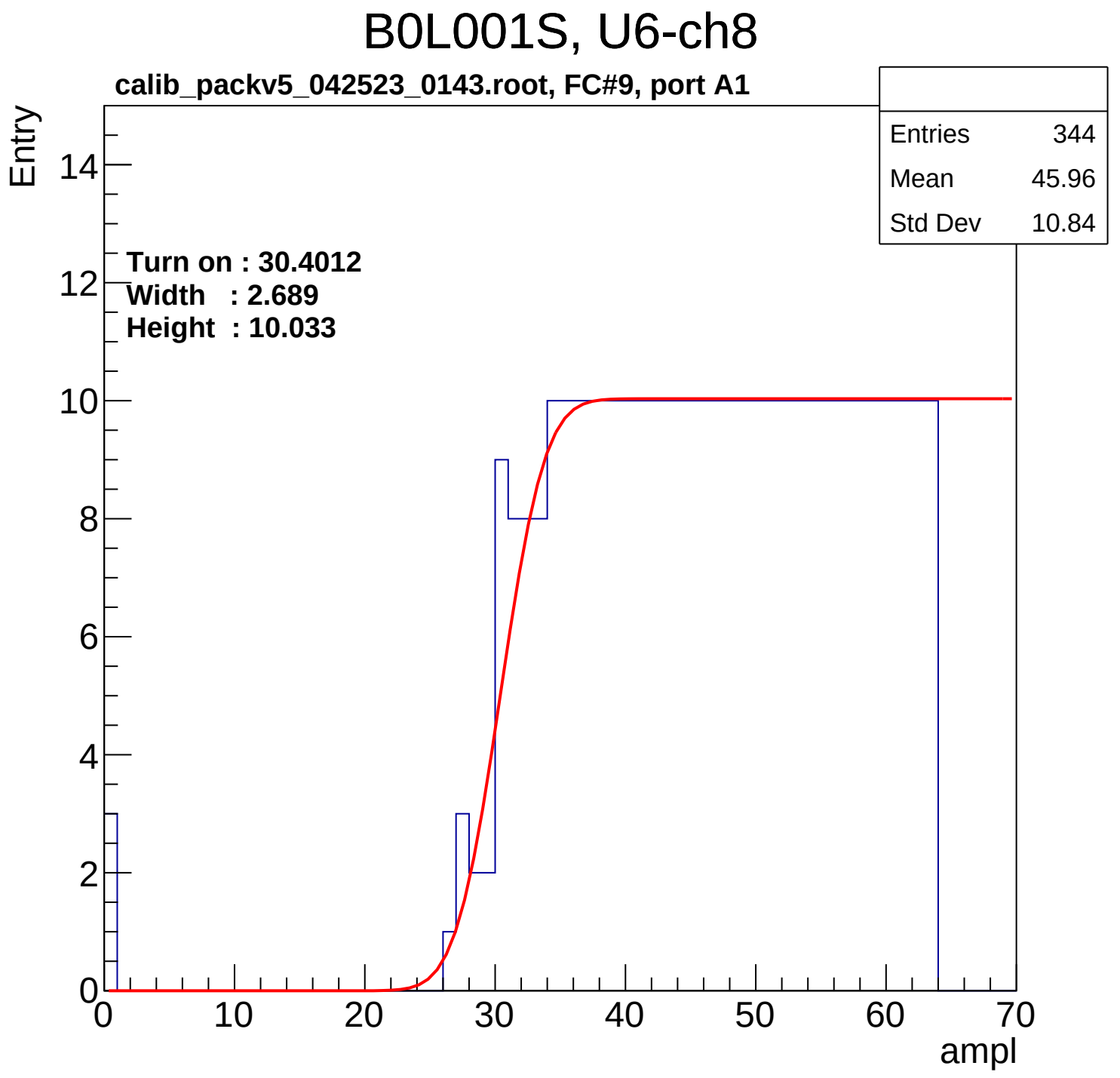
B0L001S, U6-ch8
calib_packv5_042523_0143.root, FC#9, port A1
Entries 344
Mean 45.96
Std Dev 10.84
Turn on : 30.4012
Width : 2.689
Height : 10.033
Entry
ampl
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6
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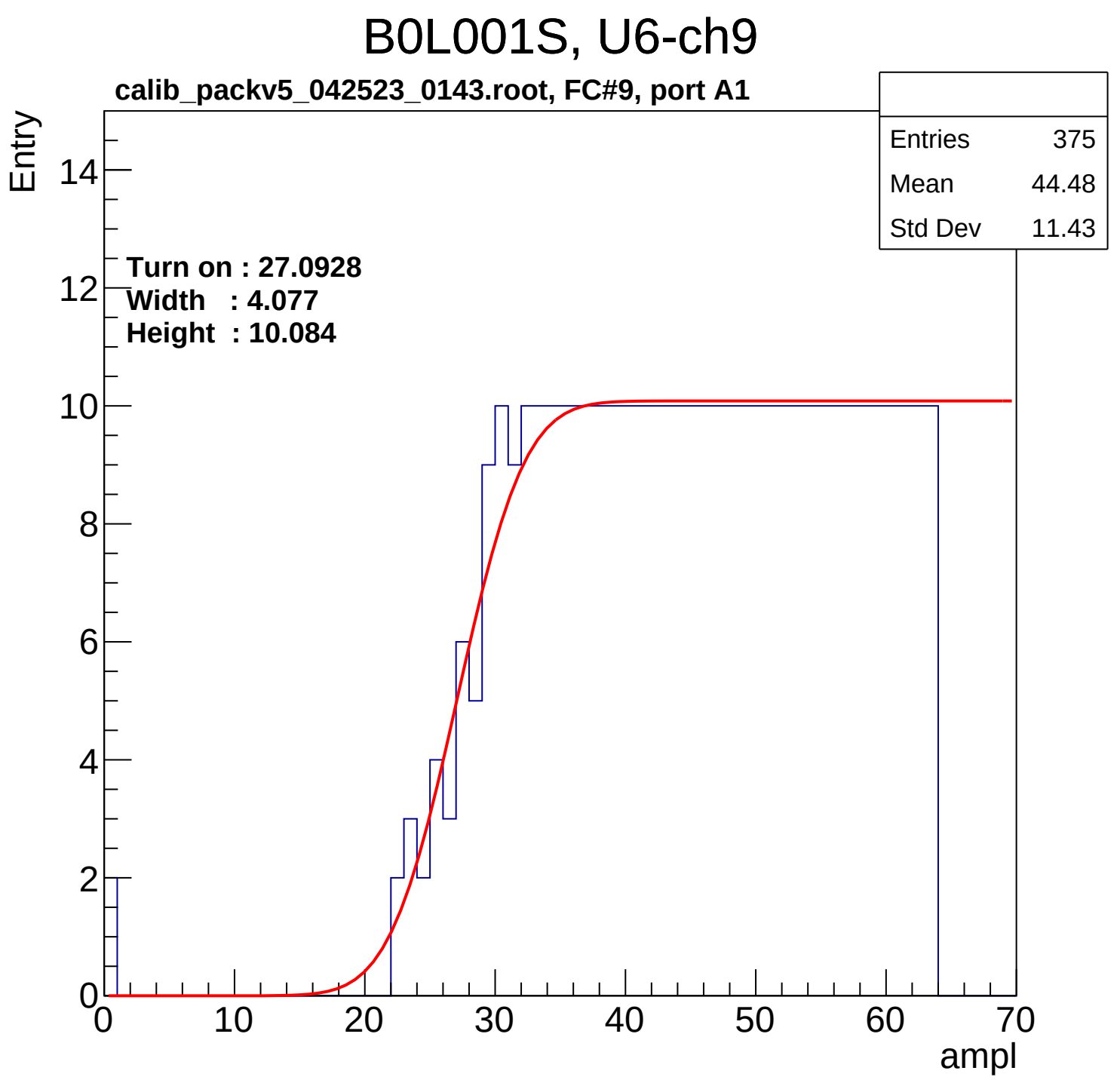
B0L001S, U6-ch9
calib_packv5_042523_0143.root, FC#9, port A1
Entries 375
Mean 44.48
Std Dev 11.43
Turn on : 27.0928
Width : 4.077
Height : 10.084
Entry
ampl
0
2
4
6
8
10
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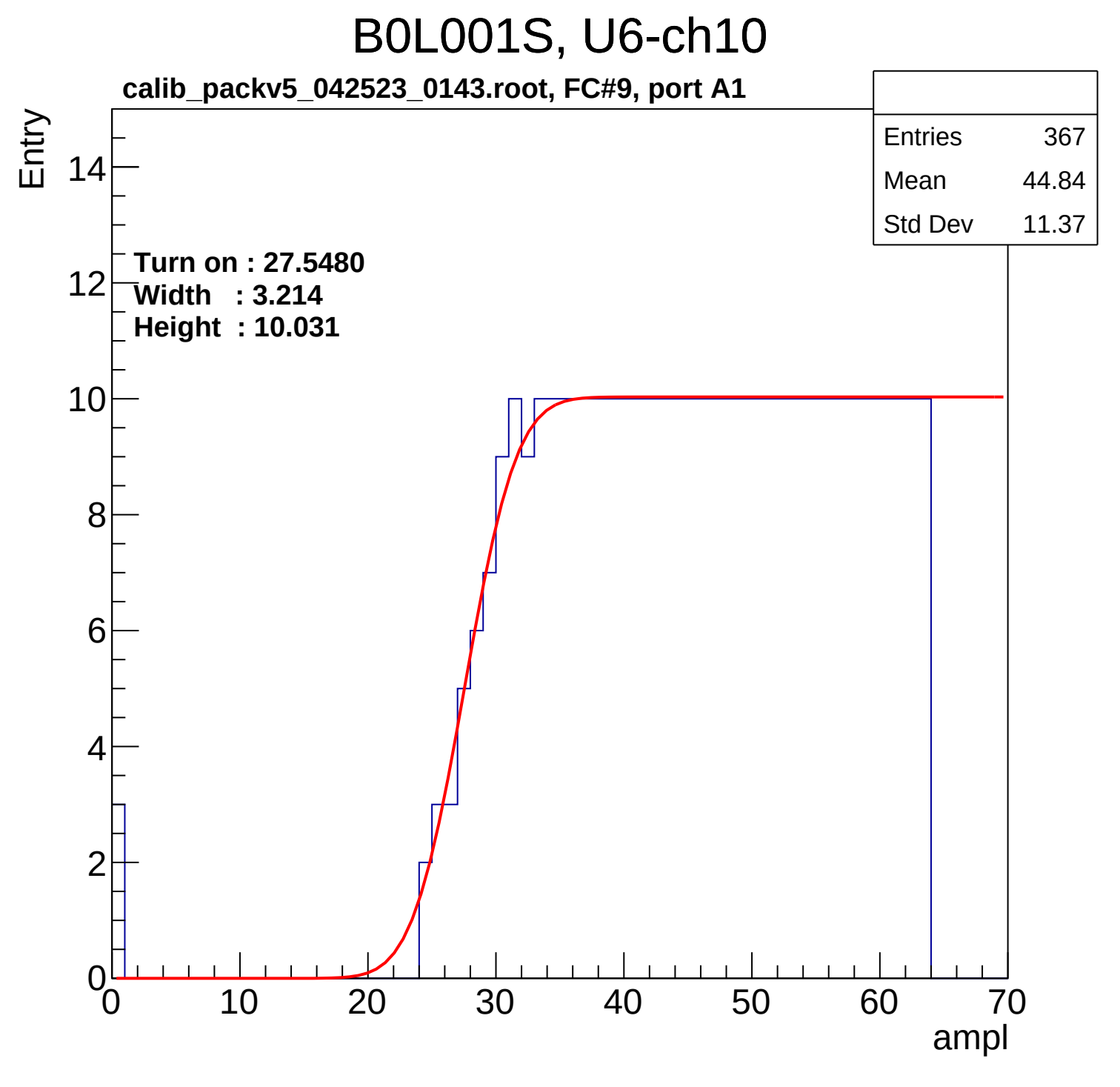
B0L001S, U6-ch10
calib_packv5_042523_0143.root, FC#9, port A1
Entries 367
Mean 44.84
Std Dev 11.37
Turn on : 27.5480
Width : 3.214
Height : 10.031
Entry
ampl
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6
8
10
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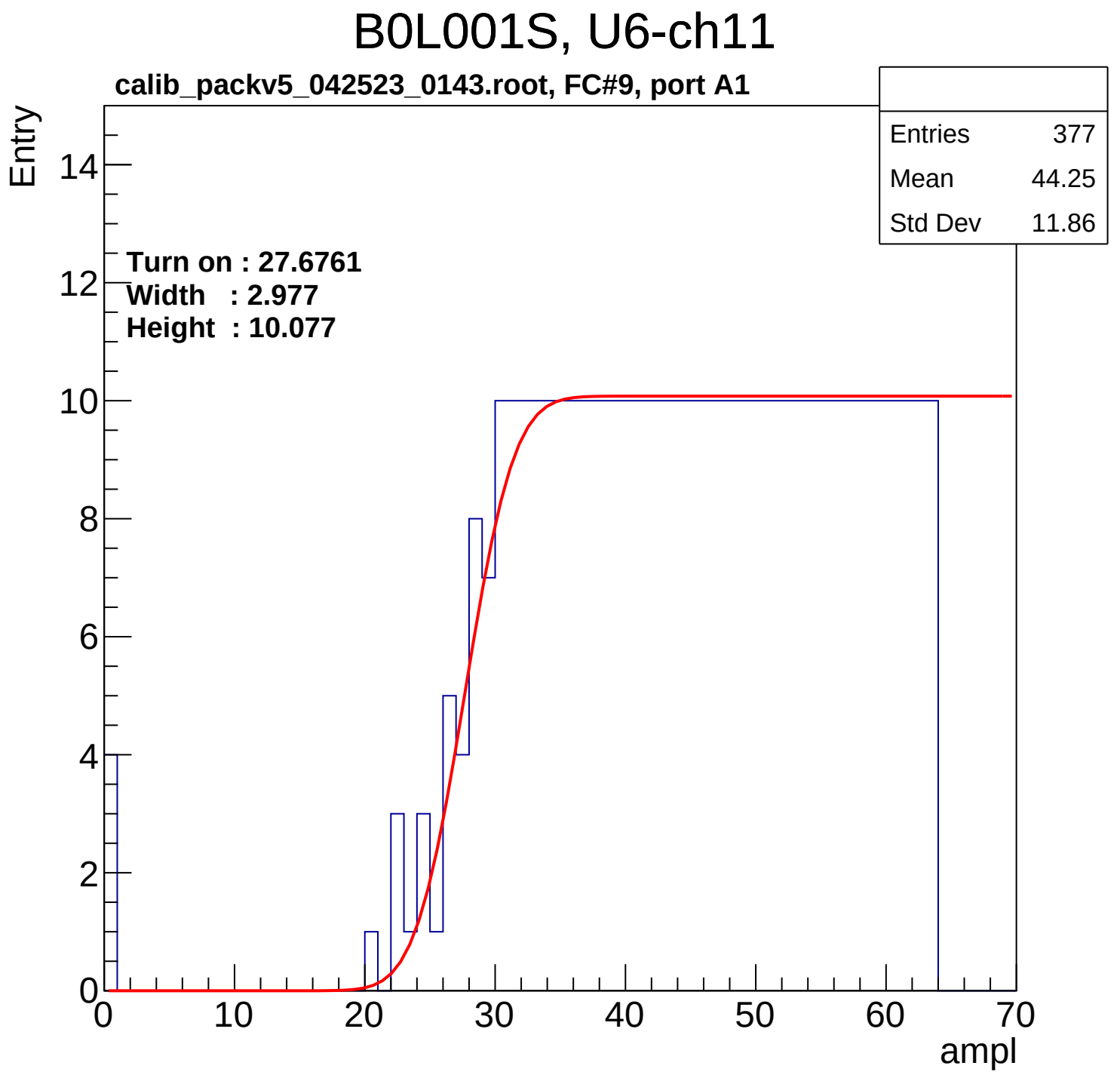
B0L001S, U6-ch11
calib_packv5_042523_0143.root, FC#9, port A1
Entries 377
Mean 44.25
Std Dev 11.86
Turn on : 27.6761
Width : 2.977
Height : 10.077
Entry
ampl
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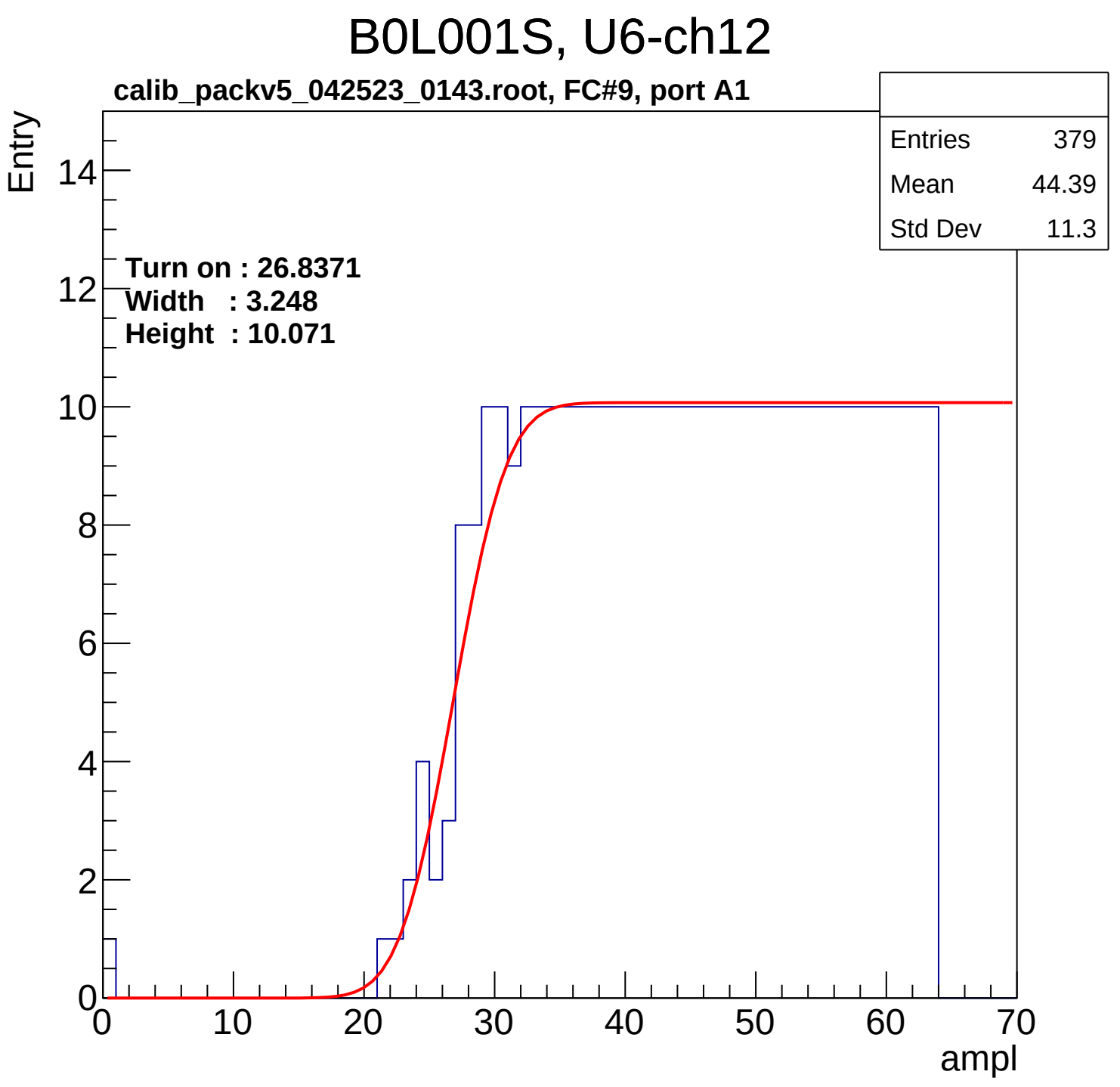
B0L001S, U6-ch12
calib_packv5_042523_0143.root, FC#9, port A1
Entries 379
Mean 44.39
Std Dev 11.3
Turn on : 26.8371
Width : 3.248
Height : 10.071
Entry
ampl
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6
8
10
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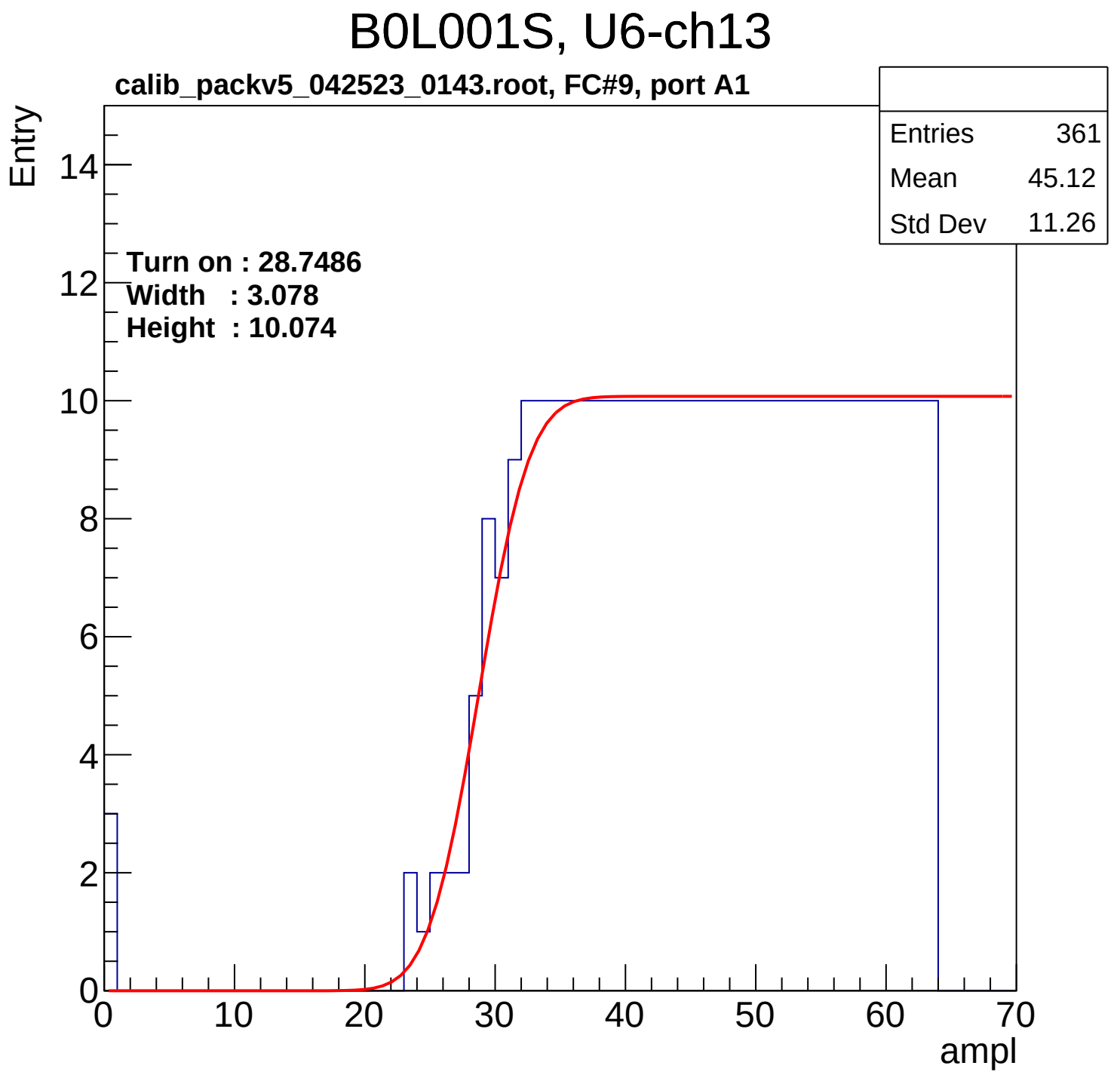
B0L001S, U6-ch13
calib_packv5_042523_0143.root, FC#9, port A1
Entries 361
Mean 45.12
Std Dev 11.26
Turn on : 28.7486
Width : 3.078
Height : 10.074
Entry
ampl
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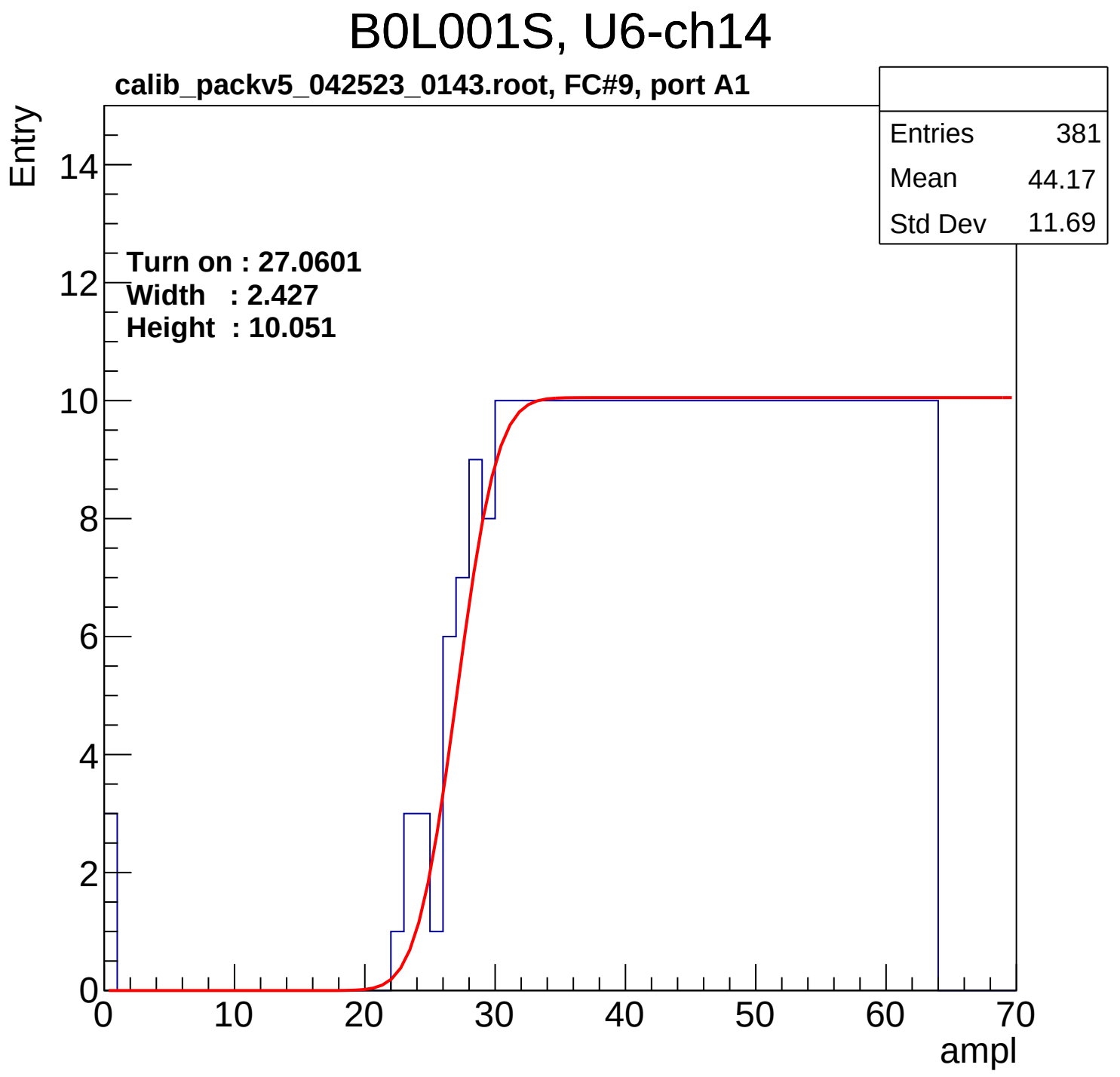
B0L001S, U6-ch14
calib_packv5_042523_0143.root, FC#9, port A1
Entries 381
Mean 44.17
Std Dev 11.69
Turn on : 27.0601
Width : 2.427
Height : 10.051
Entry
ampl
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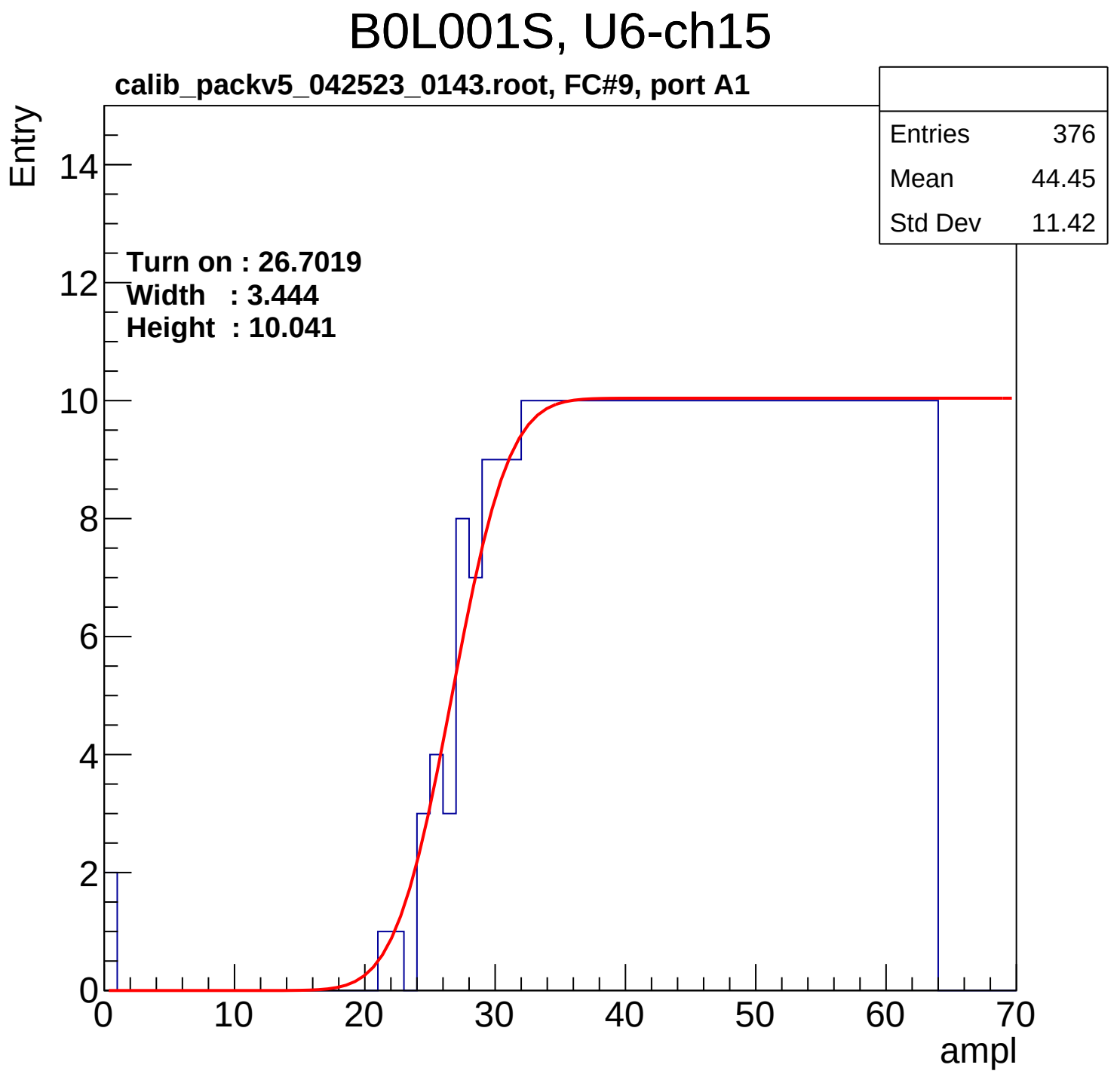
B0L001S, U6-ch15
calib_packv5_042523_0143.root, FC#9, port A1
Entries 376
Mean 44.45
Std Dev 11.42
Turn on : 26.7019
Width : 3.444
Height : 10.041
Entry
ampl
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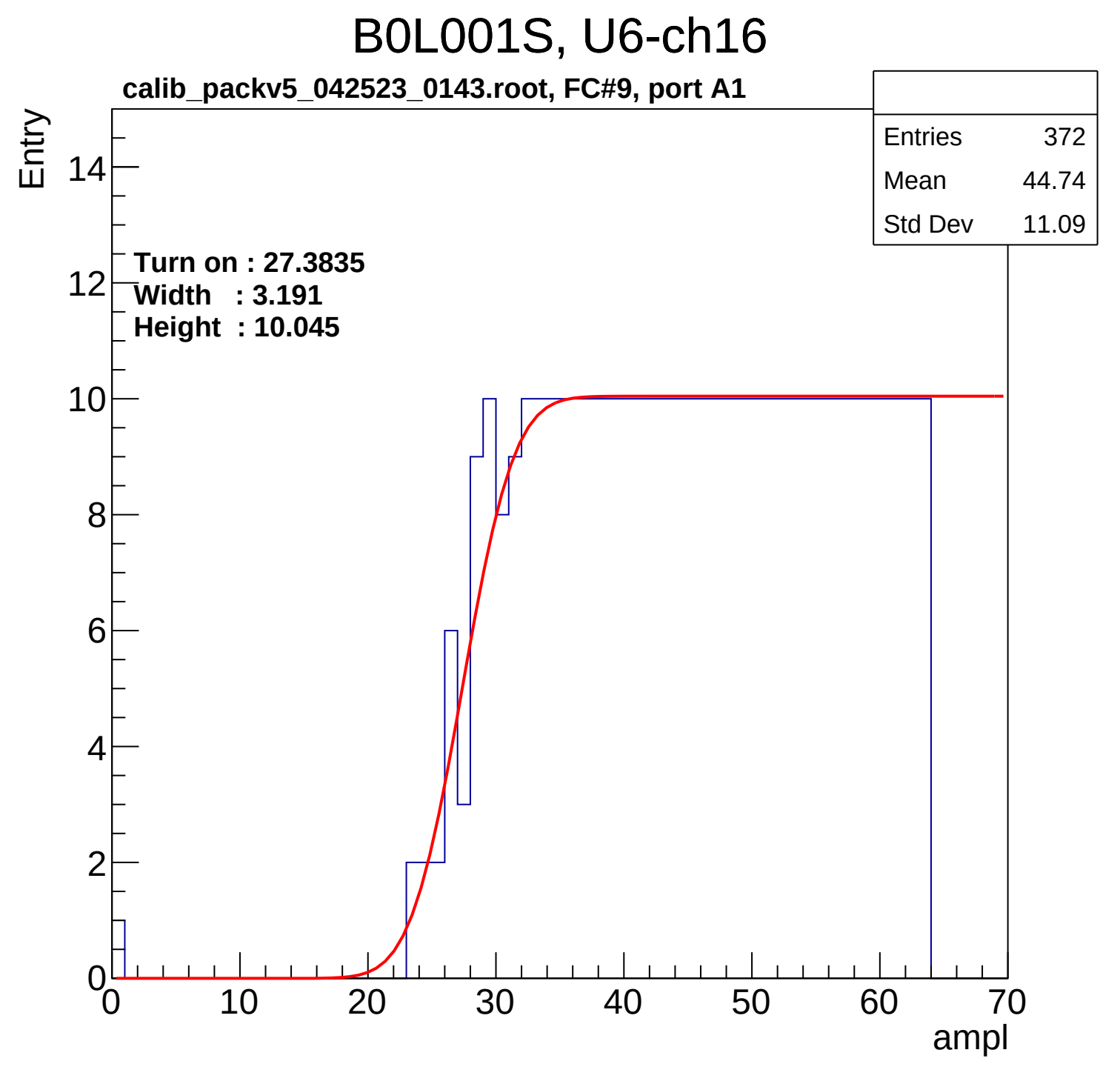
B0L001S, U6-ch16
calib_packv5_042523_0143.root, FC#9, port A1
Entries 372
Mean 44.74
Std Dev 11.09
Turn on : 27.3835
Width : 3.191
Height : 10.045
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ampl
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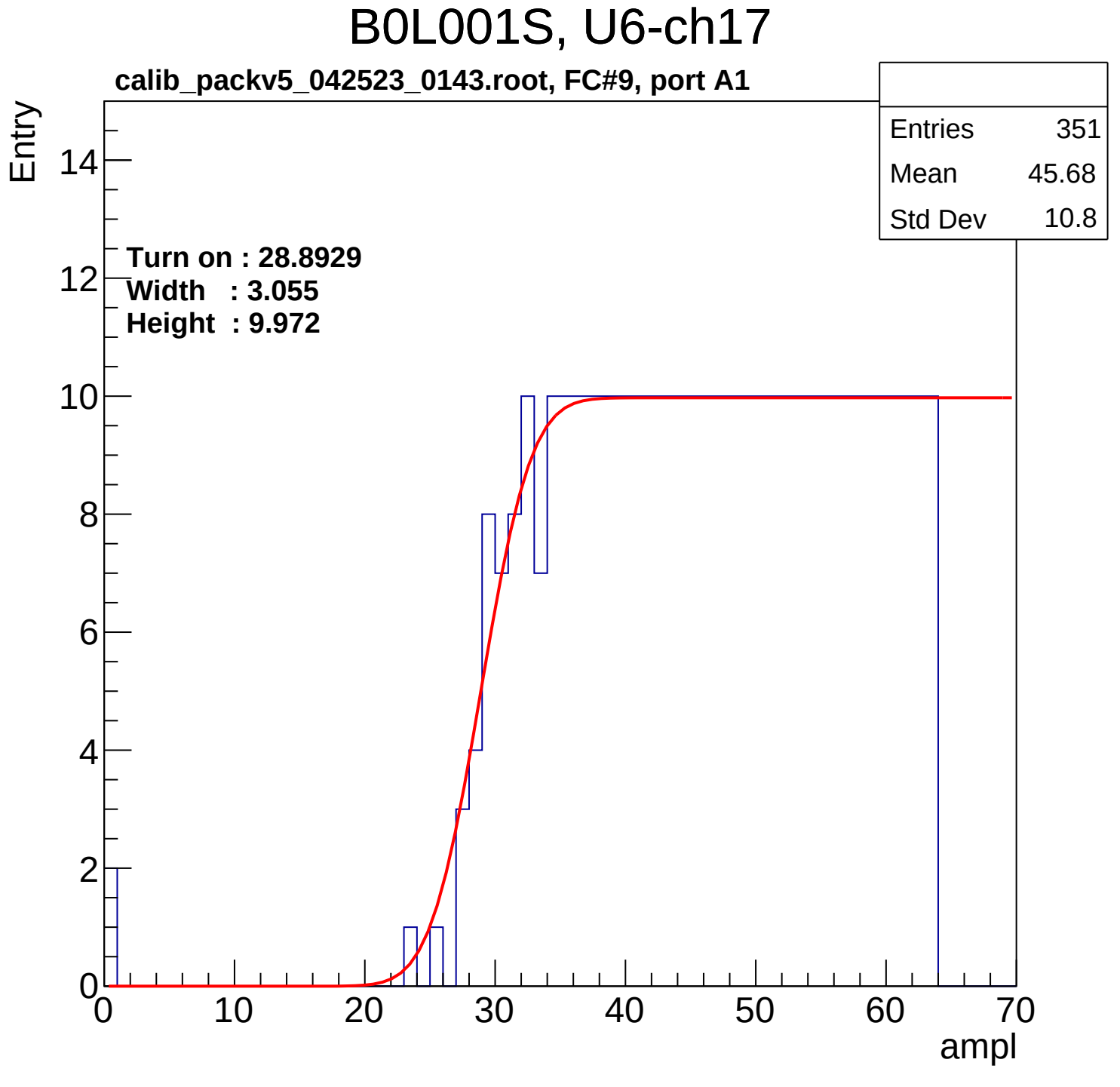
B0L001S, U6-ch17
calib_packv5_042523_0143.root, FC#9, port A1
Entries 351
Mean 45.68
Std Dev 10.8
Turn on : 28.8929
Width : 3.055
Height : 9.972
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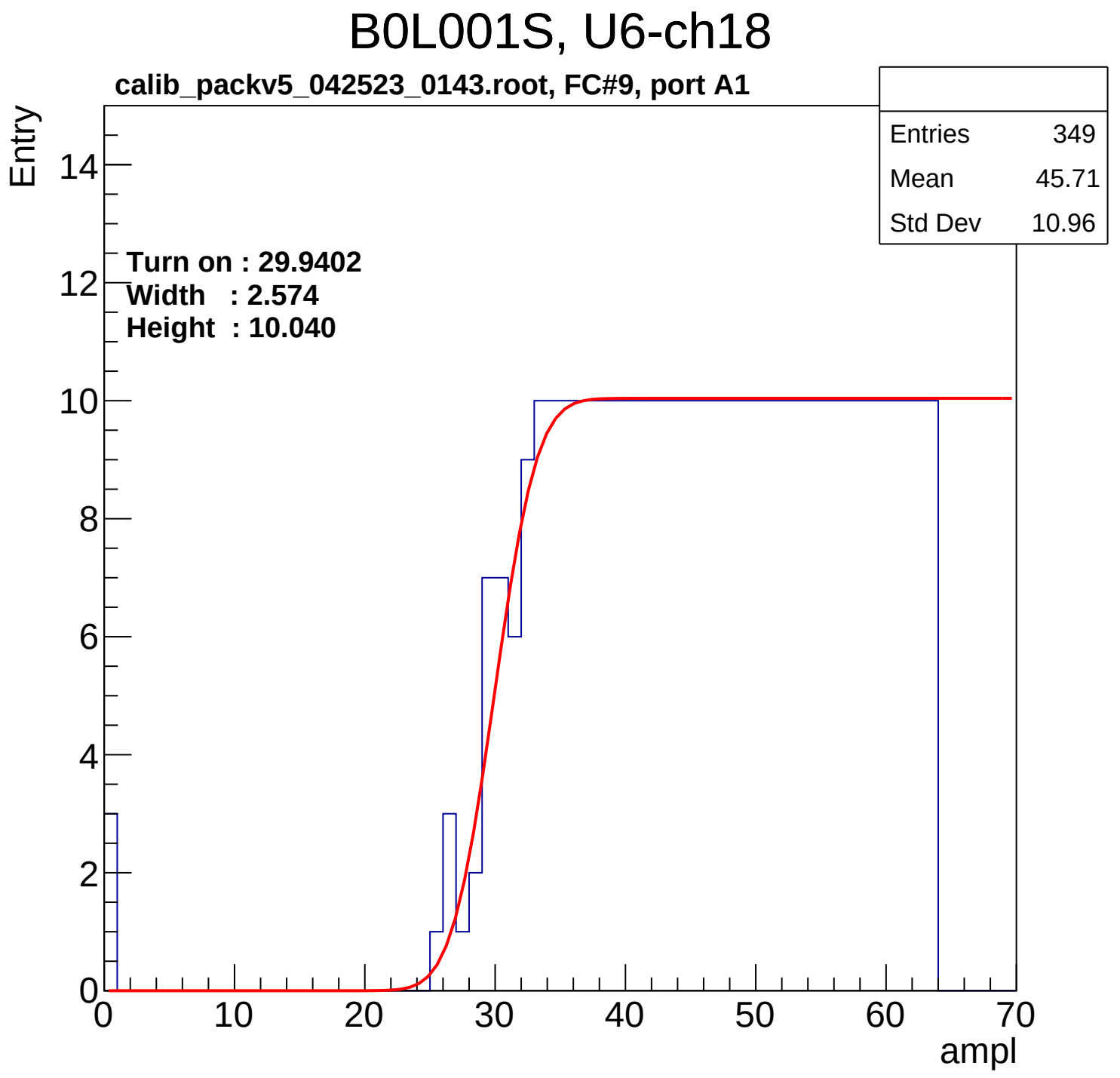
B0L001S, U6-ch18
calib_packv5_042523_0143.root, FC#9, port A1
Entries 349
Mean 45.71
Std Dev 10.96
Turn on : 29.9402
Width : 2.574
Height : 10.040
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ampl
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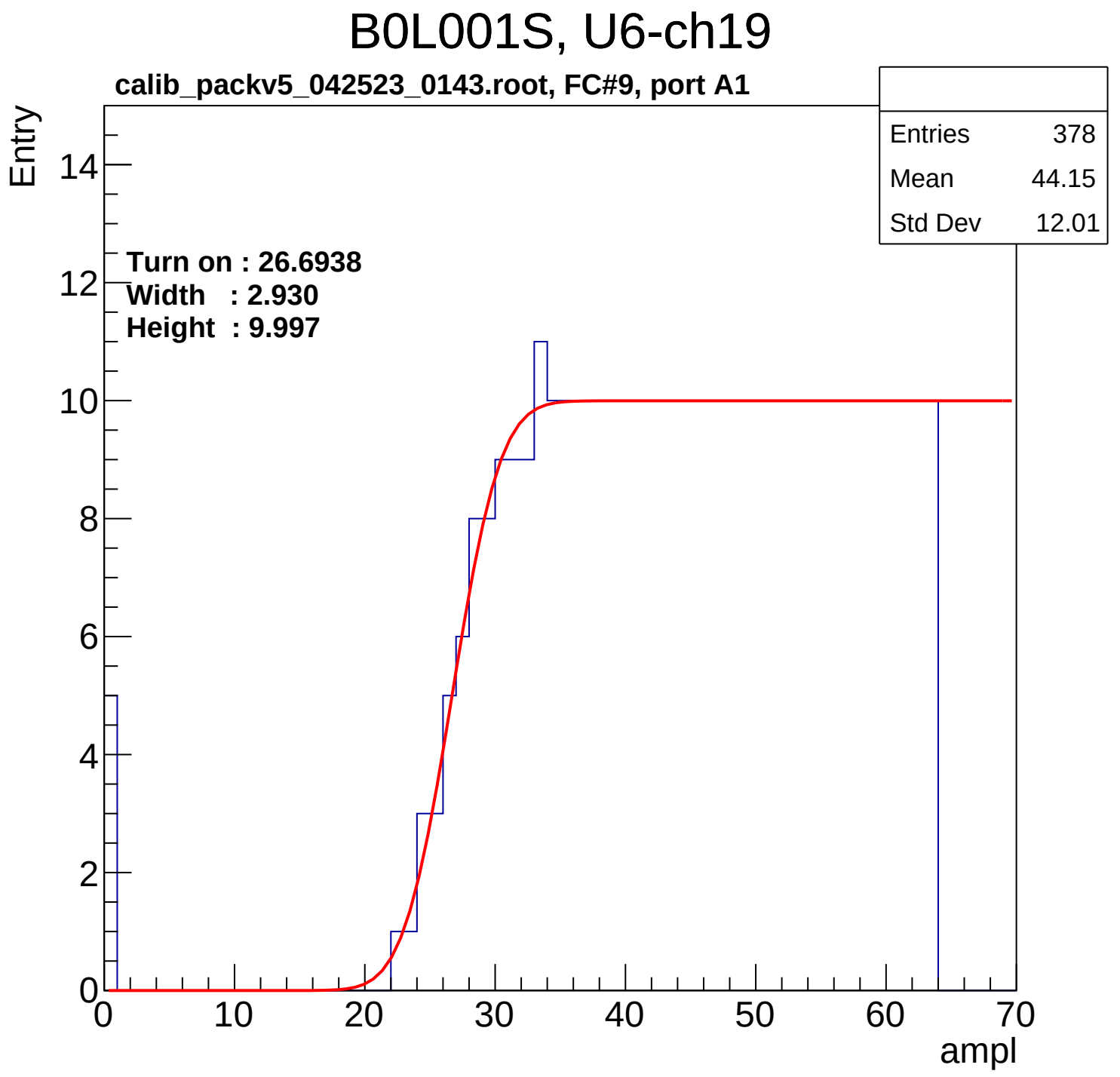
B0L001S, U6-ch19
calib_packv5_042523_0143.root, FC#9, port A1
Entries 378
Mean 44.15
Std Dev 12.01
Turn on : 26.6938
Width : 2.930
Height : 9.997
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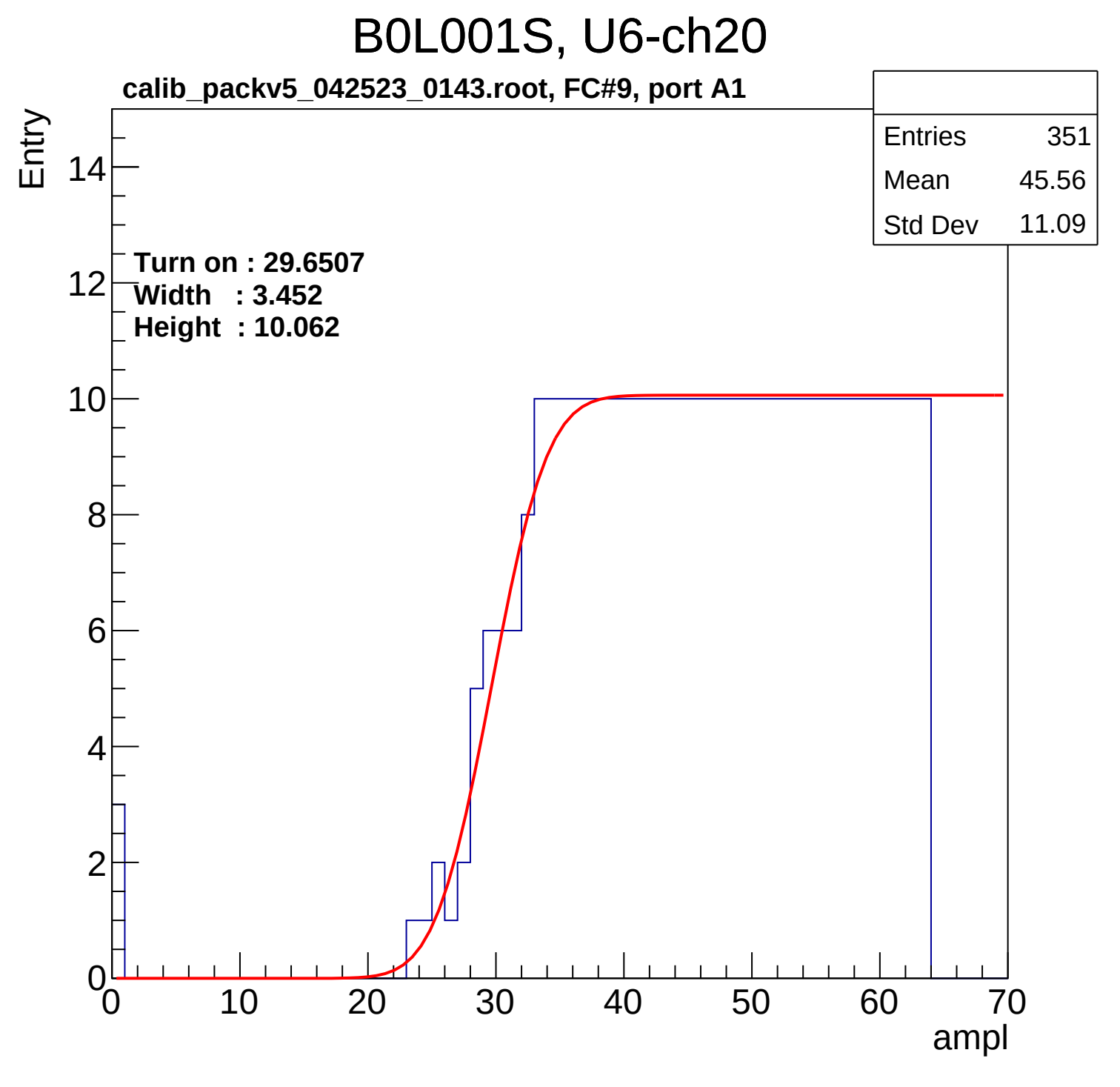
B0L001S, U6-ch20
calib_packv5_042523_0143.root, FC#9, port A1
Entries 351
Mean 45.56
Std Dev 11.09
Turn on : 29.6507
Width : 3.452
Height : 10.062
Entry
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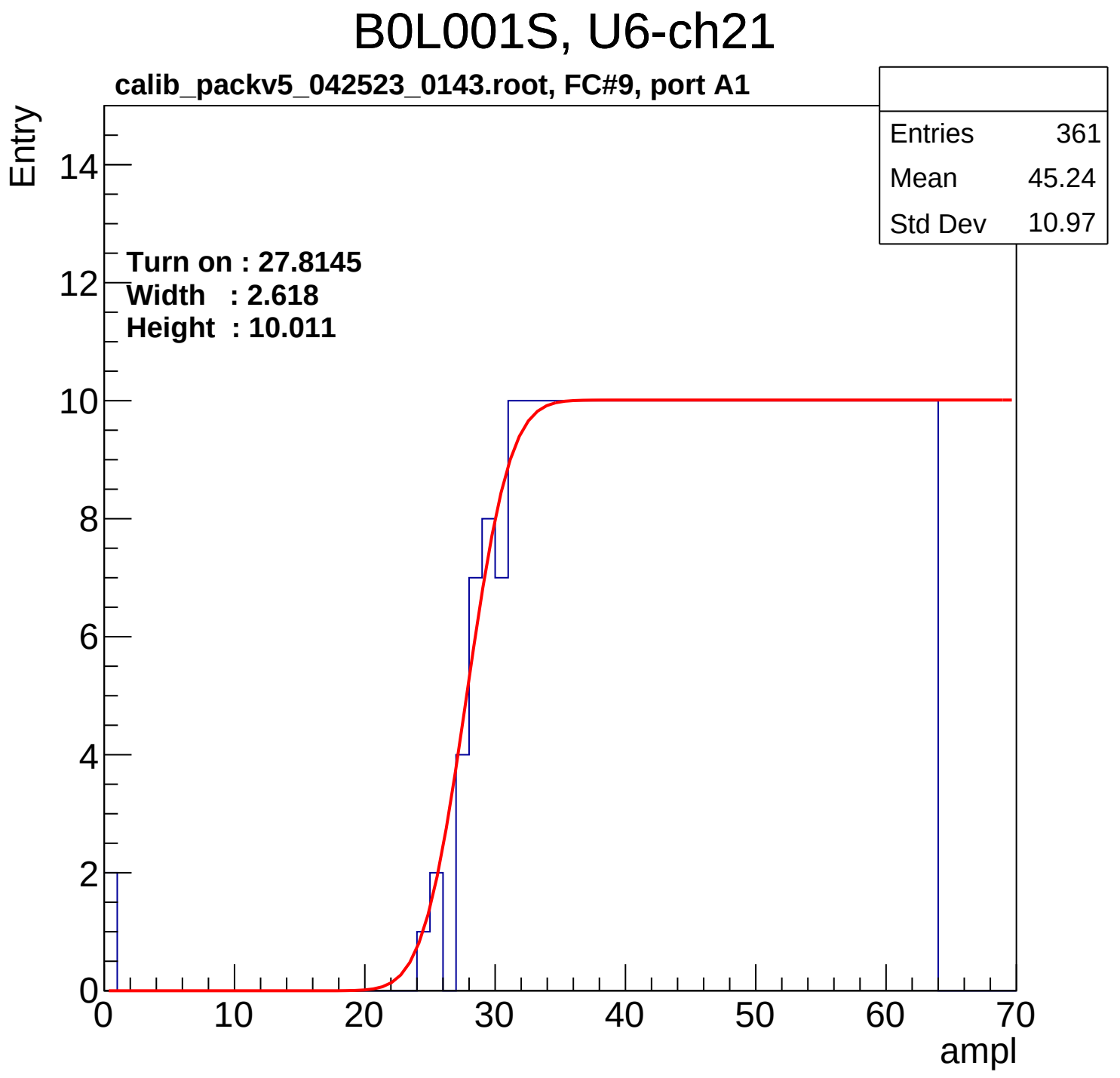
B0L001S, U6-ch21
calib_packv5_042523_0143.root, FC#9, port A1
Entries 361
Mean 45.24
Std Dev 10.97
Turn on : 27.8145
Width : 2.618
Height : 10.011
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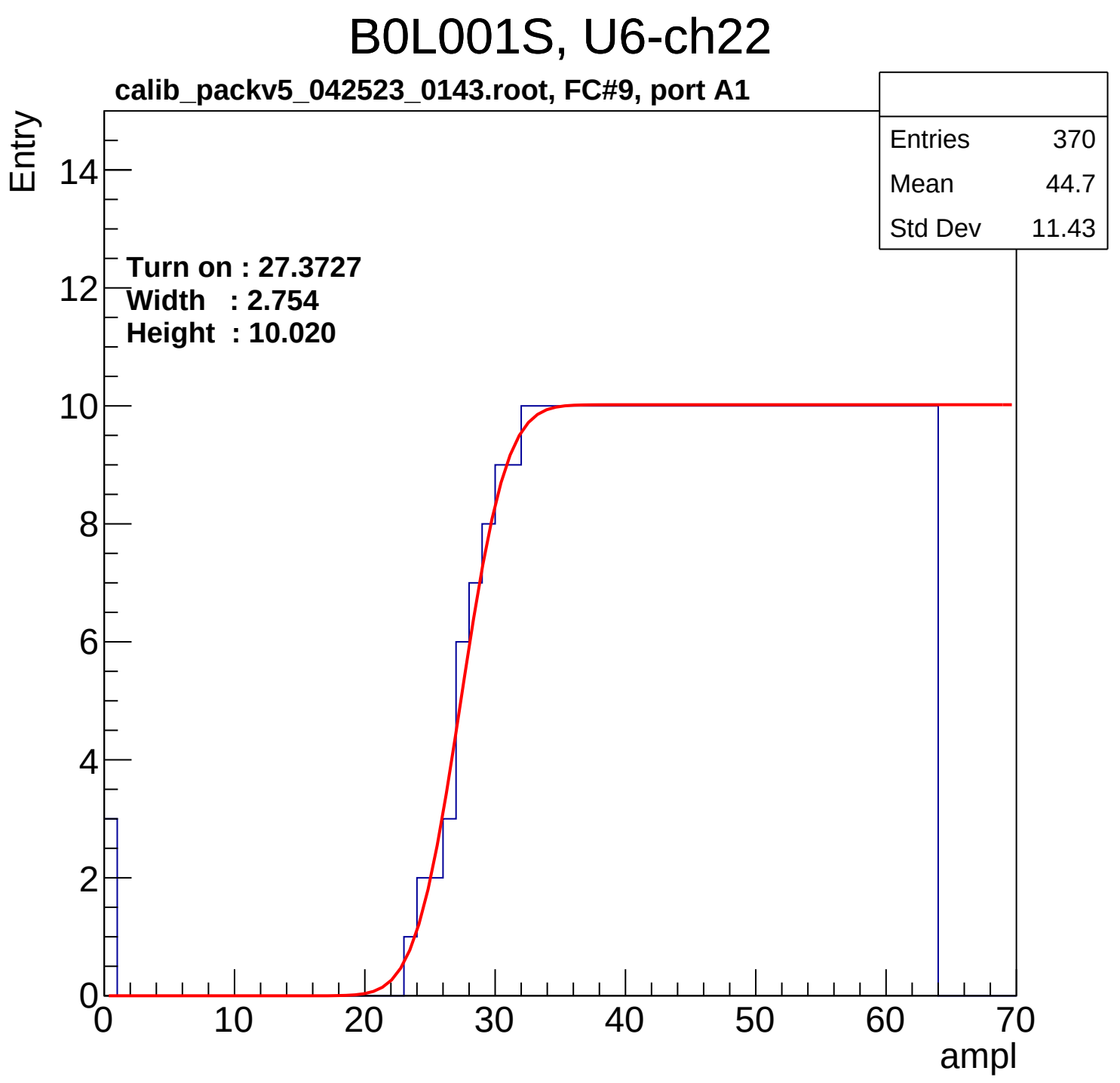
B0L001S, U6-ch22
calib_packv5_042523_0143.root, FC#9, port A1
Entries 370
Mean 44.7
Std Dev 11.43
Turn on : 27.3727
Width : 2.754
Height : 10.020
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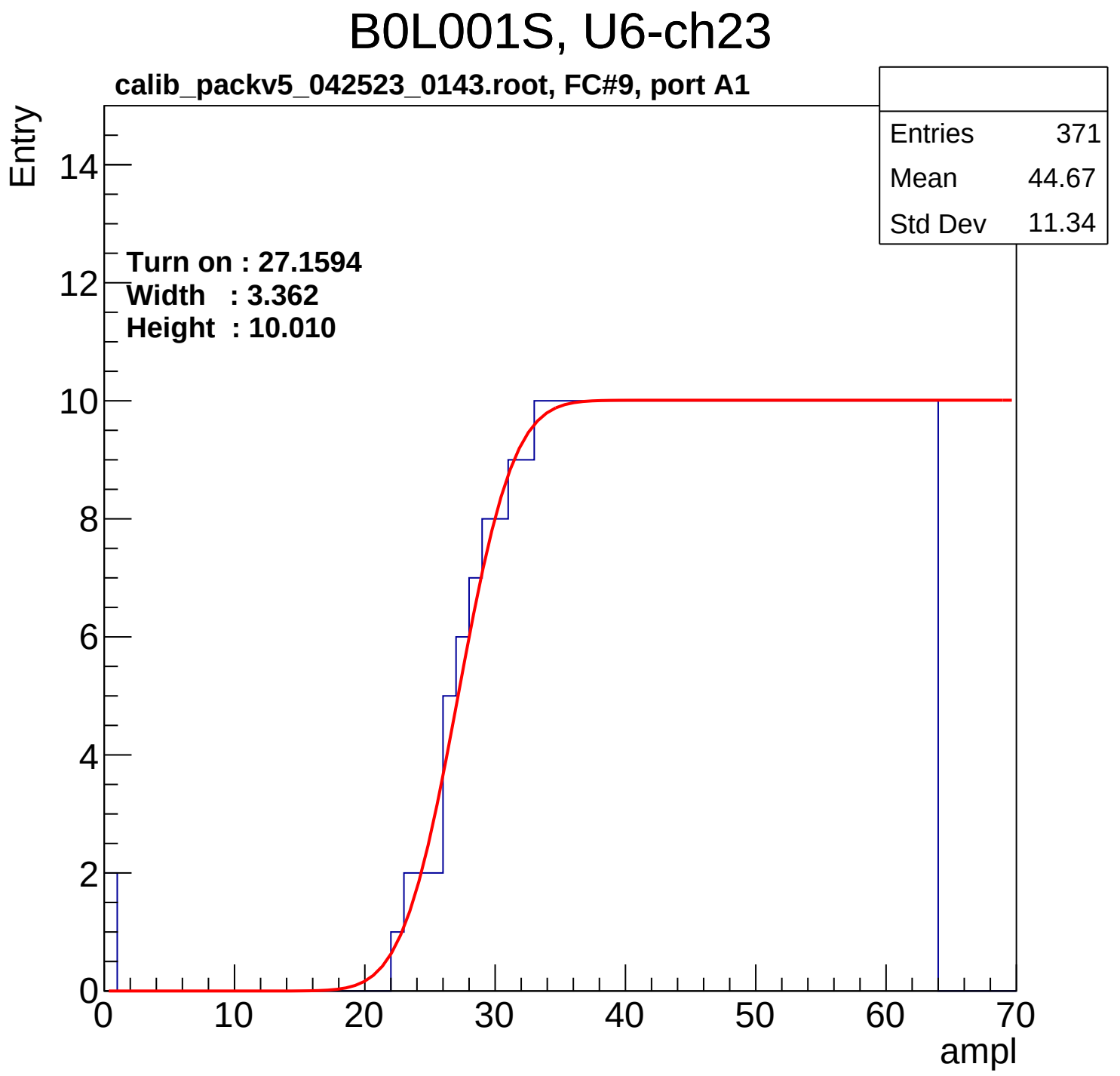
B0L001S, U6-ch23
calib_packv5_042523_0143.root, FC#9, port A1
Entries 371
Mean 44.67
Std Dev 11.34
Turn on : 27.1594
Width : 3.362
Height : 10.010
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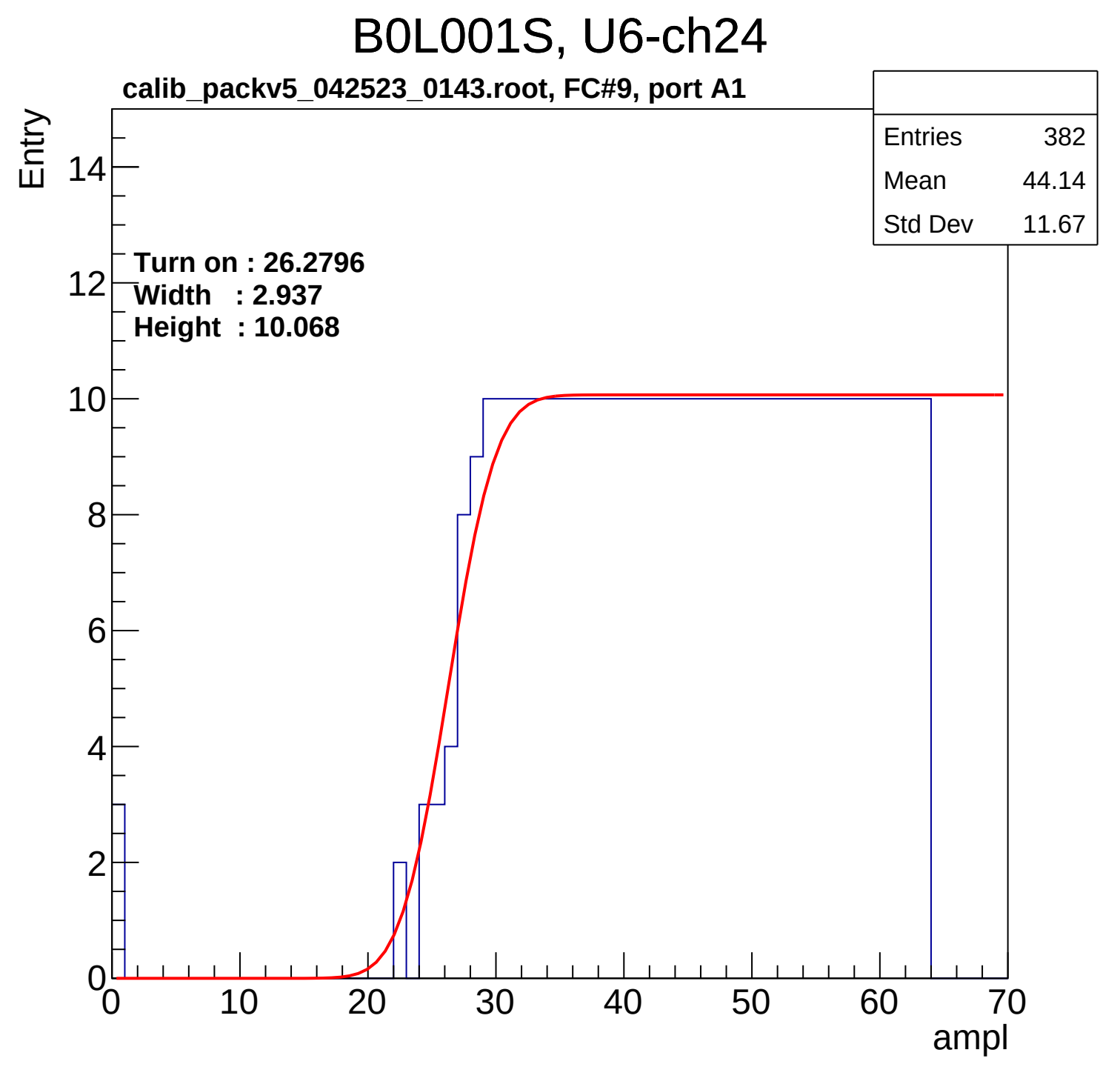
B0L001S, U6-ch24
calib_packv5_042523_0143.root, FC#9, port A1
Entries 382
Mean 44.14
Std Dev 11.67
Turn on : 26.2796
Width : 2.937
Height : 10.068
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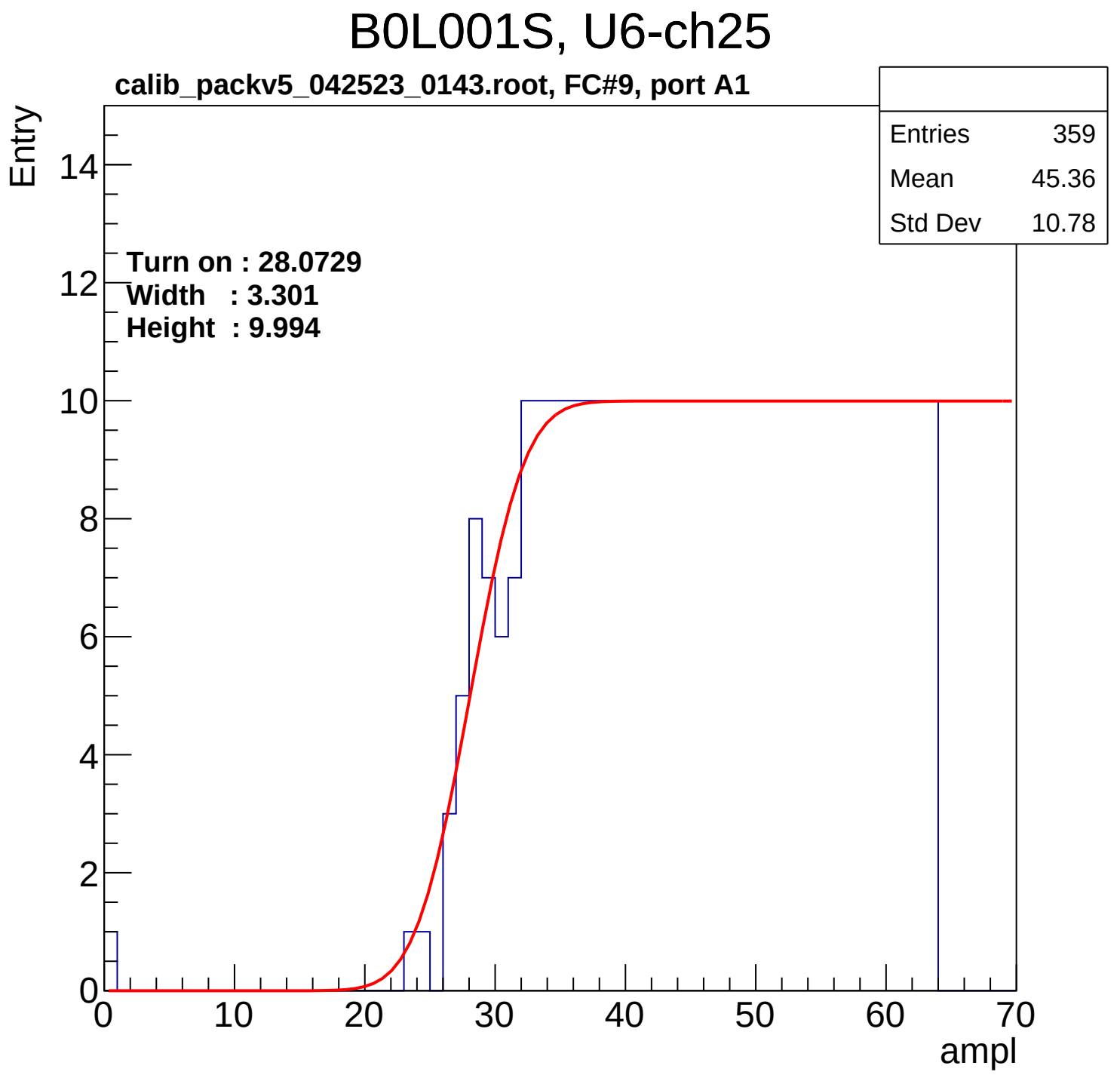
B0L001S, U6-ch25
calib_packv5_042523_0143.root, FC#9, port A1
Entries 359
Mean 45.36
Std Dev 10.78
Turn on : 28.0729
Width : 3.301
Height : 9.994
Entry
ampl
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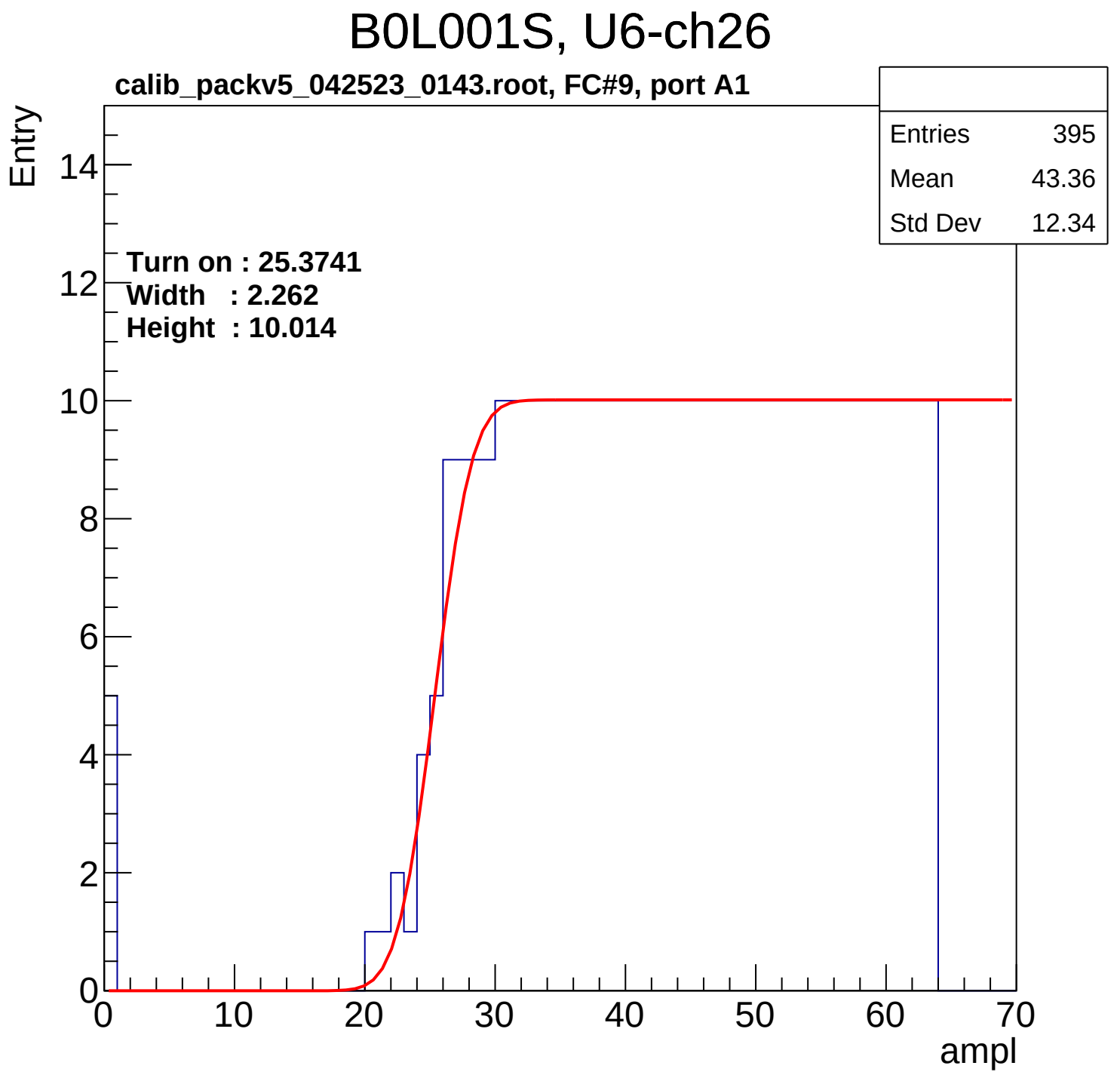
B0L001S, U6-ch26
calib_packv5_042523_0143.root, FC#9, port A1
Entries 395
Mean 43.36
Std Dev 12.34
Turn on : 25.3741
Width : 2.262
Height : 10.014
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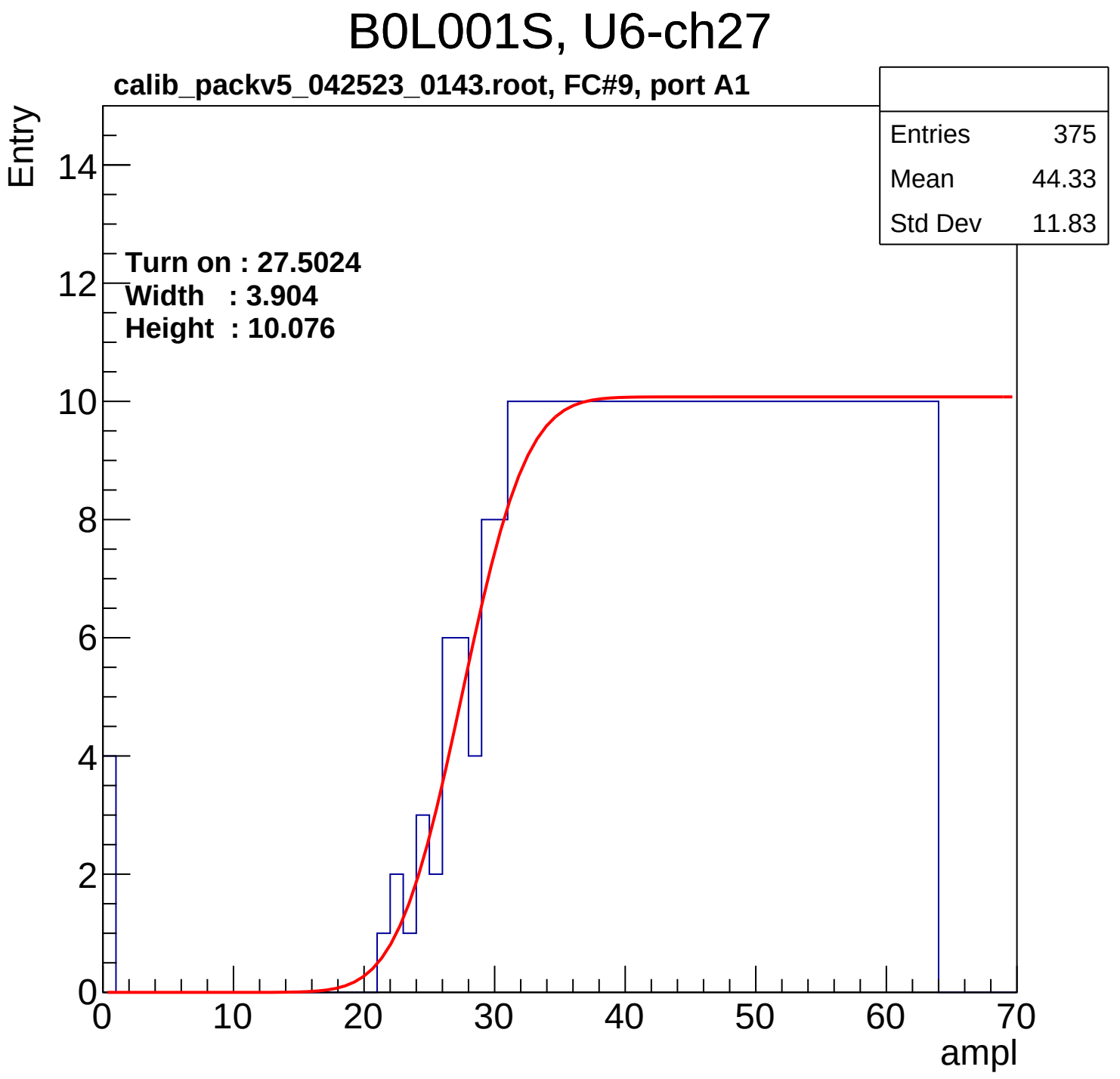
B0L001S, U6-ch27
calib_packv5_042523_0143.root, FC#9, port A1
Entries 375
Mean 44.33
Std Dev 11.83
Turn on : 27.5024
Width : 3.904
Height : 10.076
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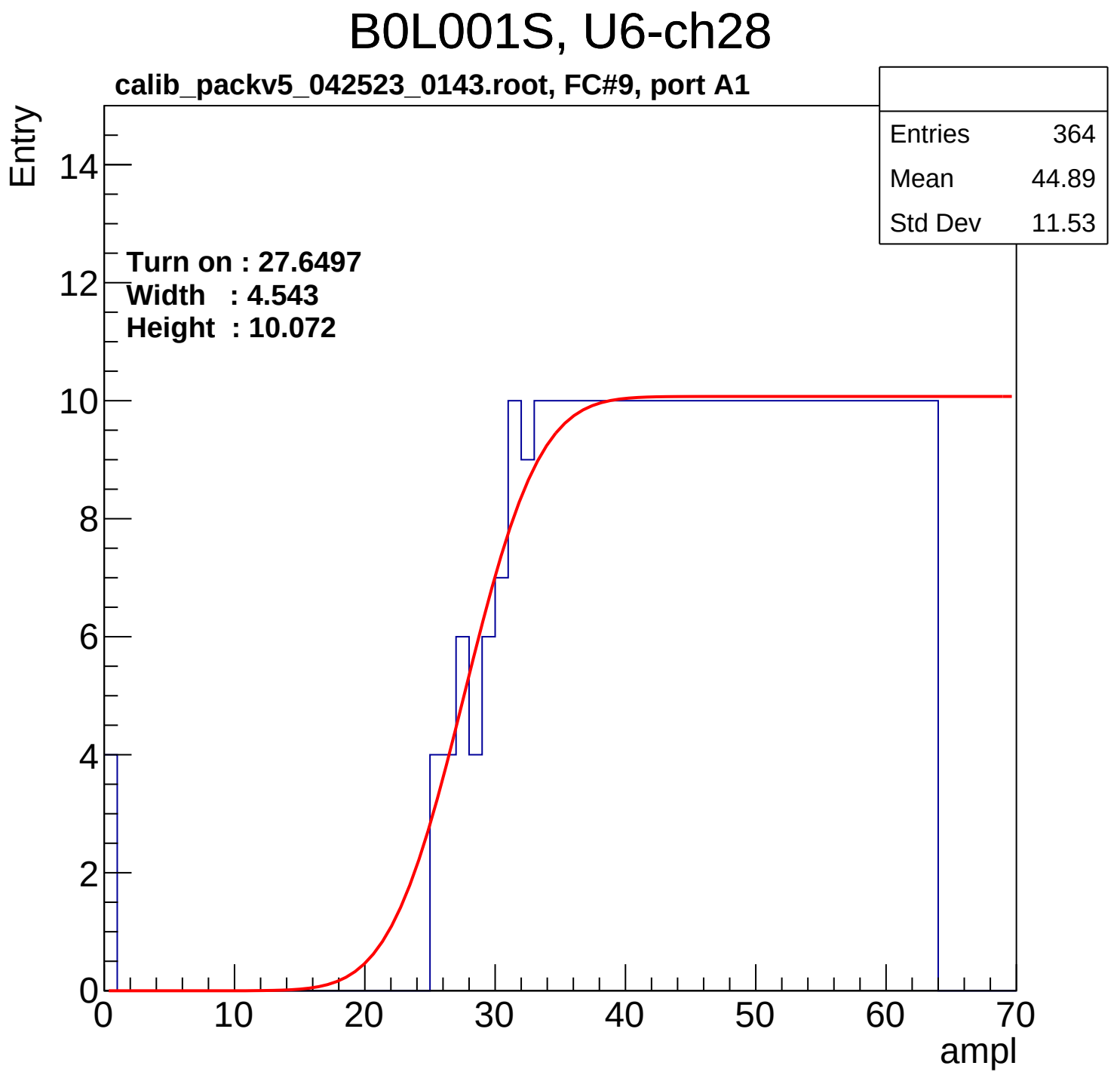
B0L001S, U6-ch28
calib_packv5_042523_0143.root, FC#9, port A1
Entries 364
Mean 44.89
Std Dev 11.53
Turn on : 27.6497
Width : 4.543
Height : 10.072
Entry
ampl
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20
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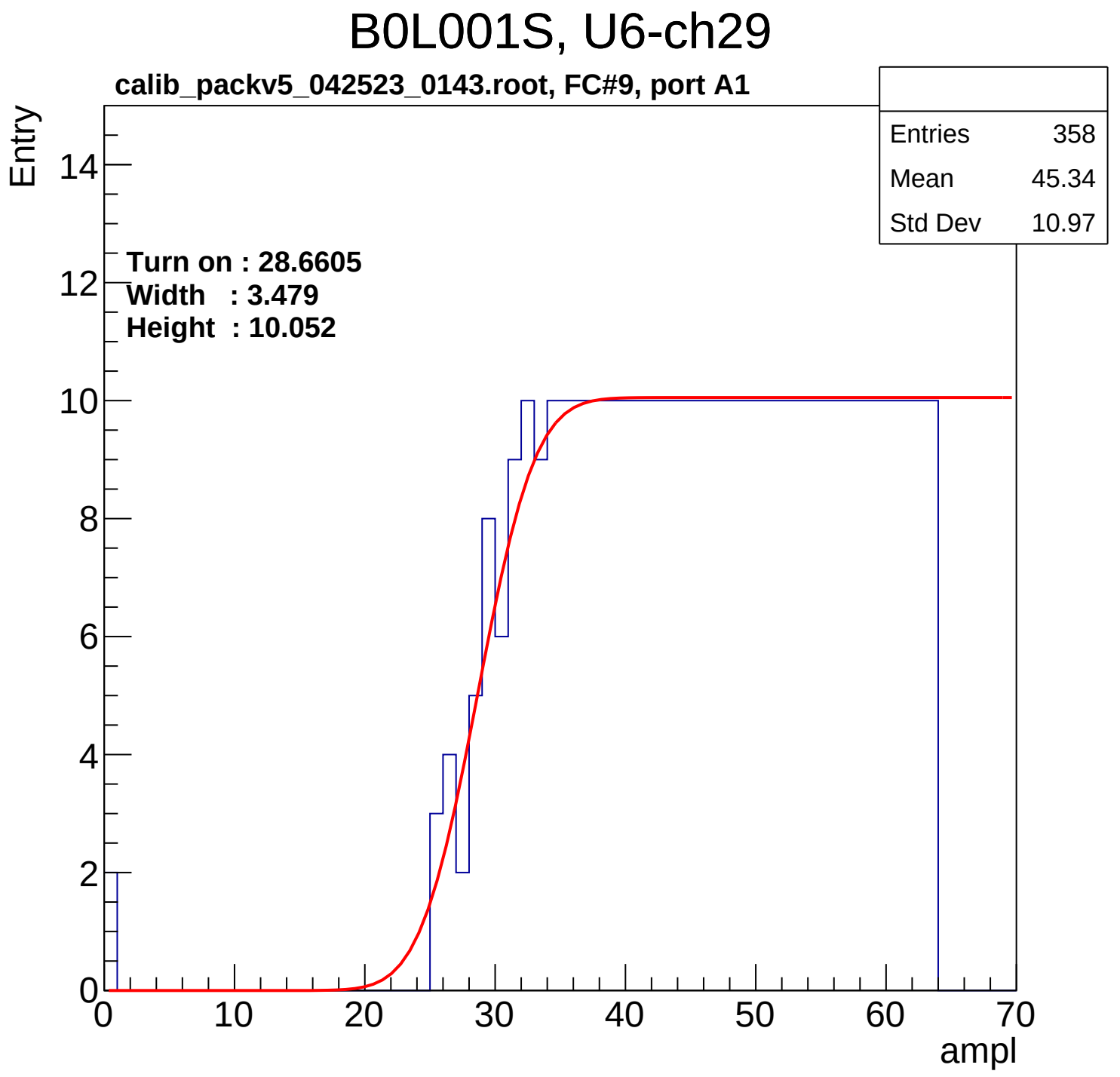
B0L001S, U6-ch29
calib_packv5_042523_0143.root, FC#9, port A1
Entries 358
Mean 45.34
Std Dev 10.97
Turn on : 28.6605
Width : 3.479
Height : 10.052
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ampl
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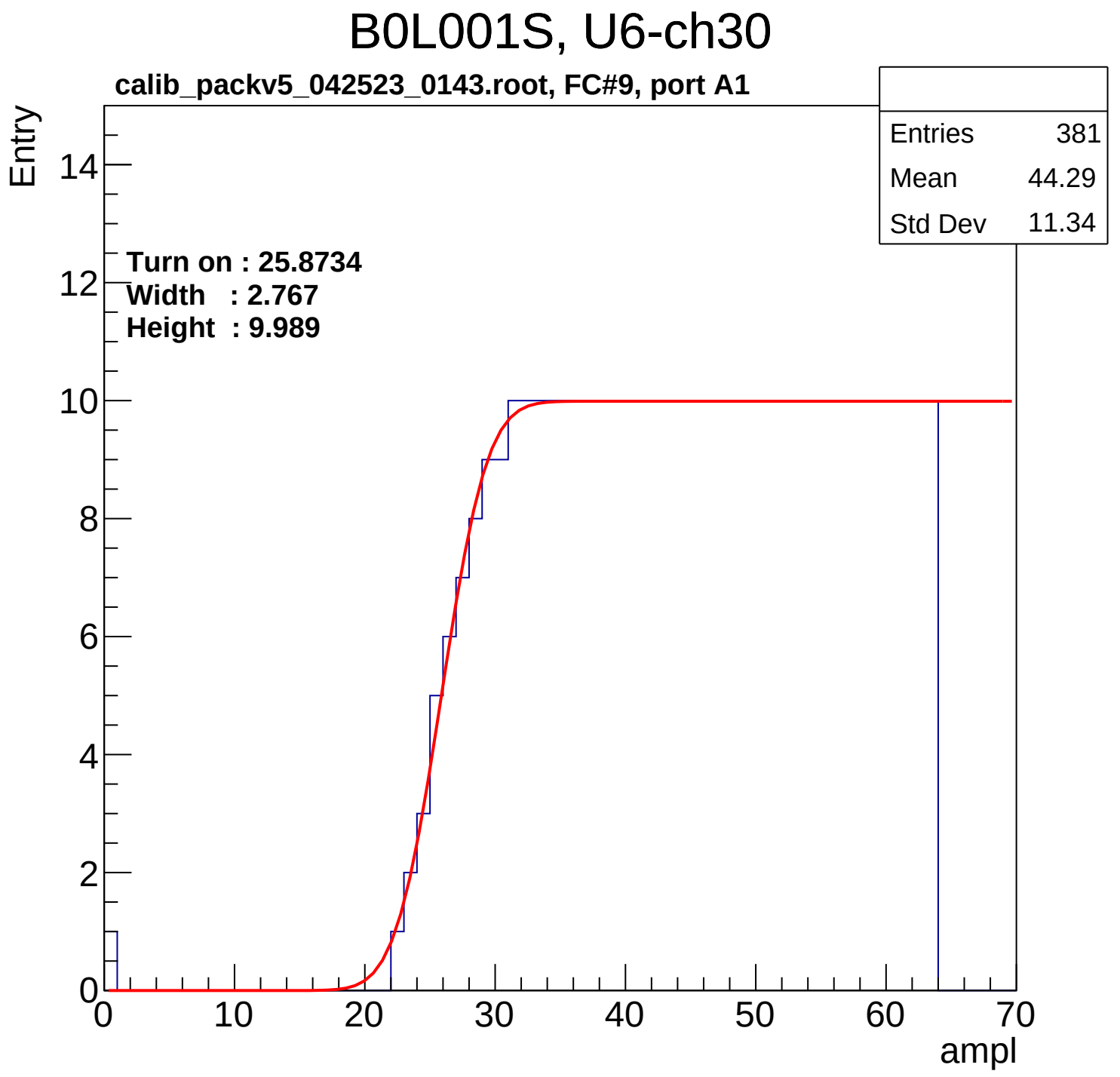
B0L001S, U6-ch30
calib_packv5_042523_0143.root, FC#9, port A1
Entries 381
Mean 44.29
Std Dev 11.34
Turn on : 25.8734
Width : 2.767
Height : 9.989
Entry
ampl
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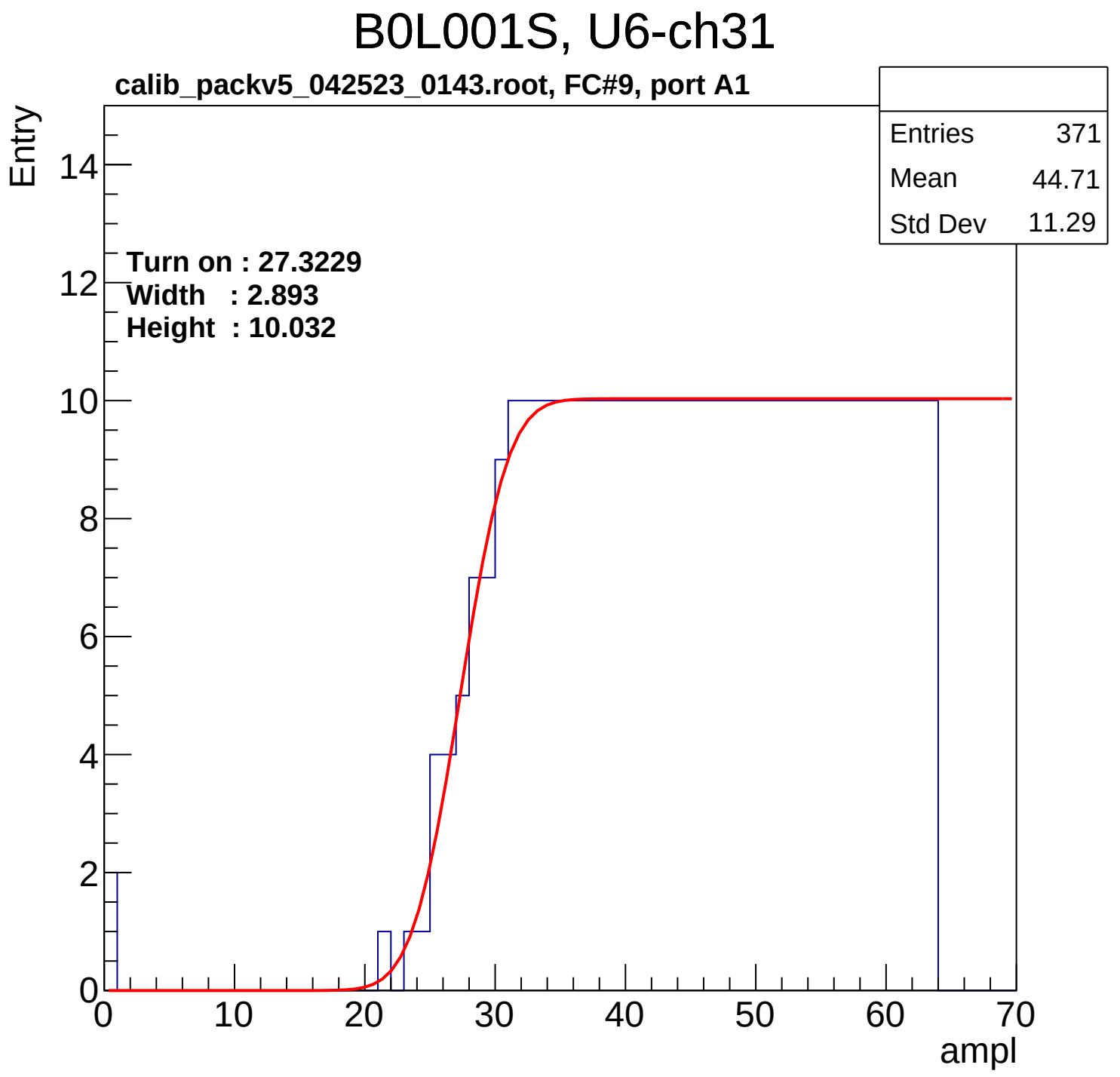
B0L001S, U6-ch31
calib_packv5_042523_0143.root, FC#9, port A1
Entries 371
Mean 44.71
Std Dev 11.29
Turn on : 27.3229
Width : 2.893
Height : 10.032
Entry
ampl
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2
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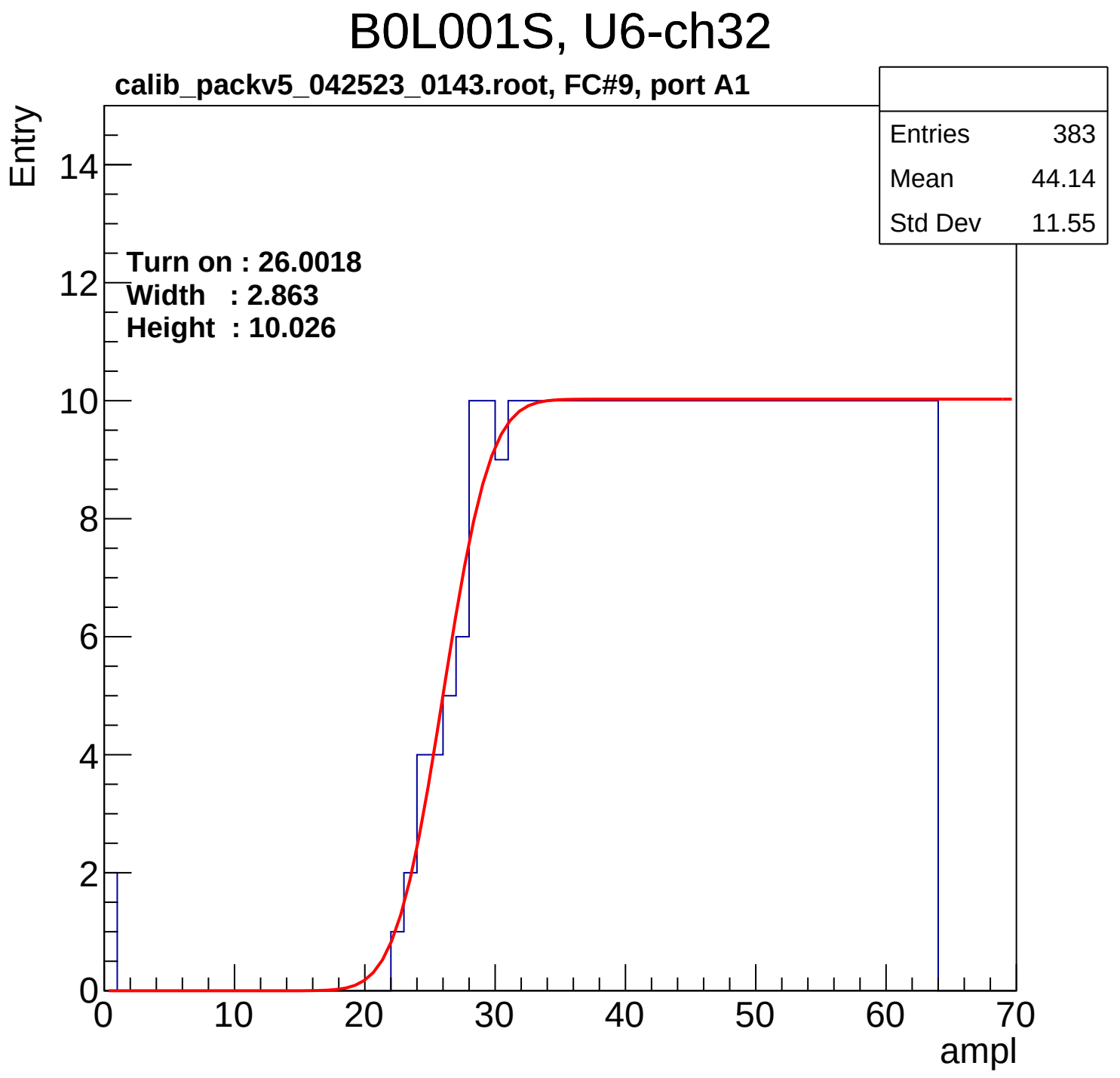
B0L001S, U6-ch32
calib_packv5_042523_0143.root, FC#9, port A1
Entries 383
Mean 44.14
Std Dev 11.55
Turn on : 26.0018
Width : 2.863
Height : 10.026
Entry
ampl
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2
4
6
8
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12
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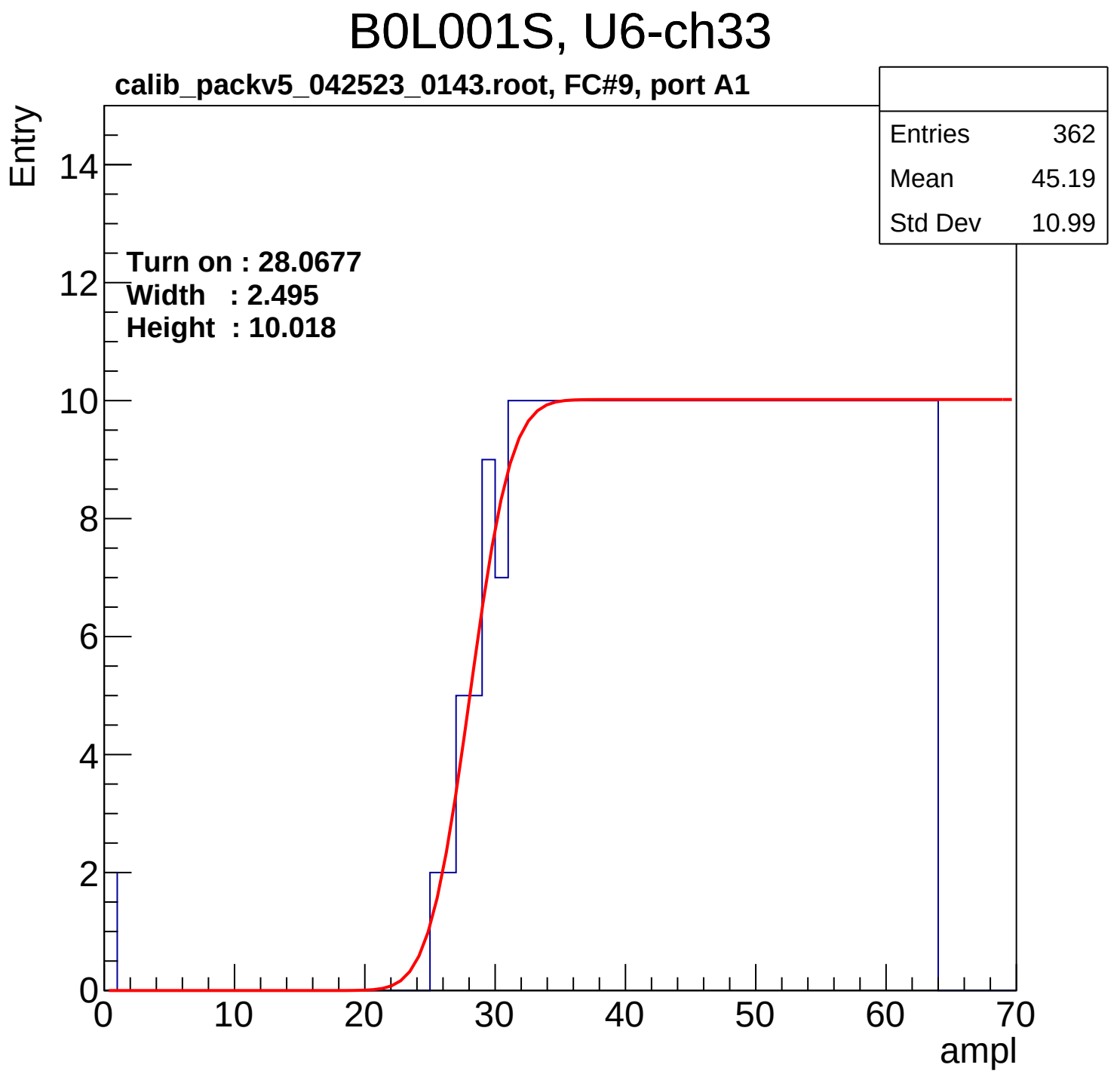
B0L001S, U6-ch33
calib_packv5_042523_0143.root, FC#9, port A1
Entries 362
Mean 45.19
Std Dev 10.99
Turn on : 28.0677
Width : 2.495
Height : 10.018
Entry
ampl
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2
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6
8
10
12
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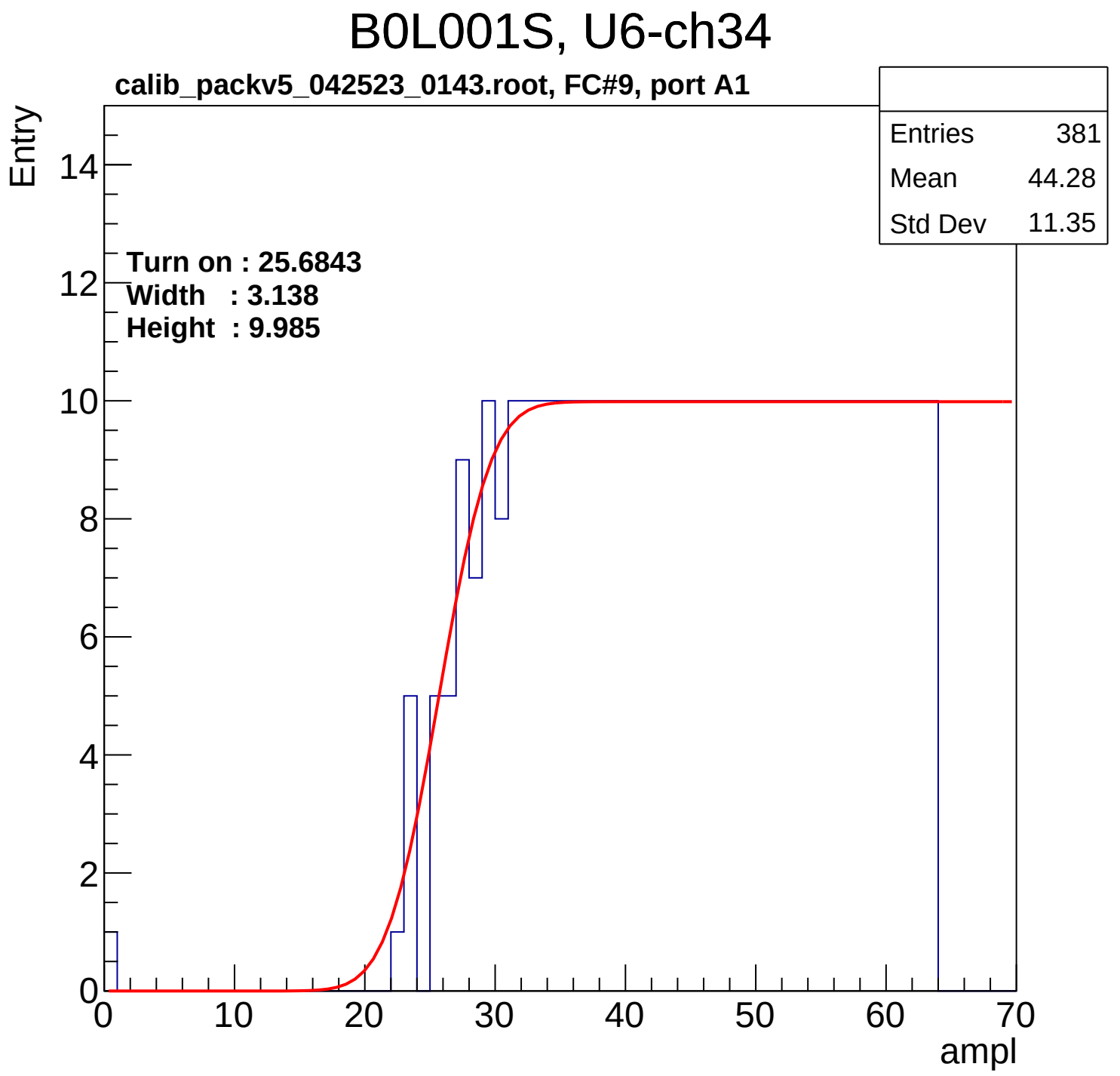
B0L001S, U6-ch34
calib_packv5_042523_0143.root, FC#9, port A1
Entries 381
Mean 44.28
Std Dev 11.35
Turn on : 25.6843
Width : 3.138
Height : 9.985
Entry
ampl
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2
4
6
8
10
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0
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60
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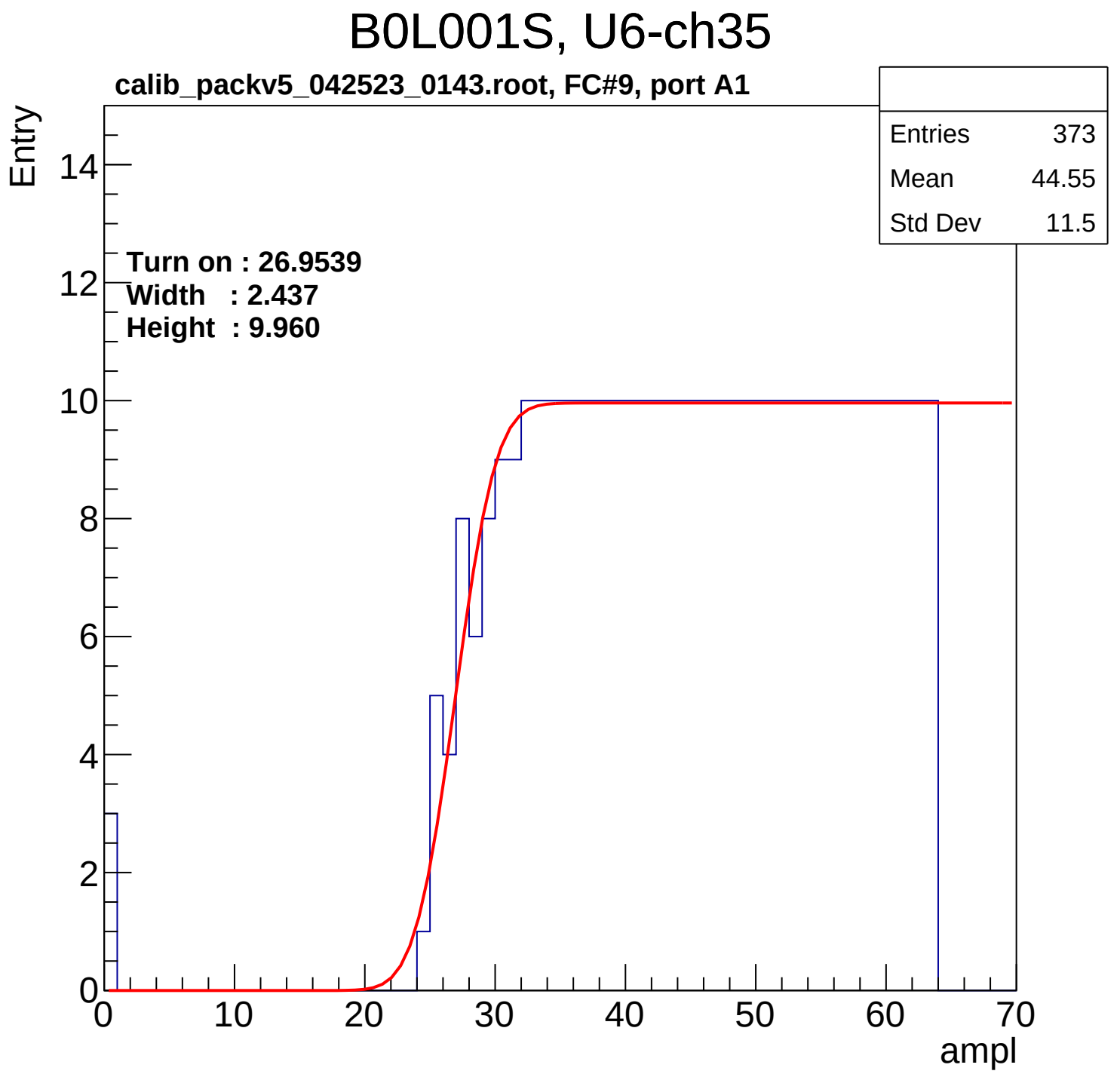
B0L001S, U6-ch35
calib_packv5_042523_0143.root, FC#9, port A1
Entries 373
Mean 44.55
Std Dev 11.5
Turn on : 26.9539
Width : 2.437
Height : 9.960
Entry
ampl
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4
6
8
10
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0
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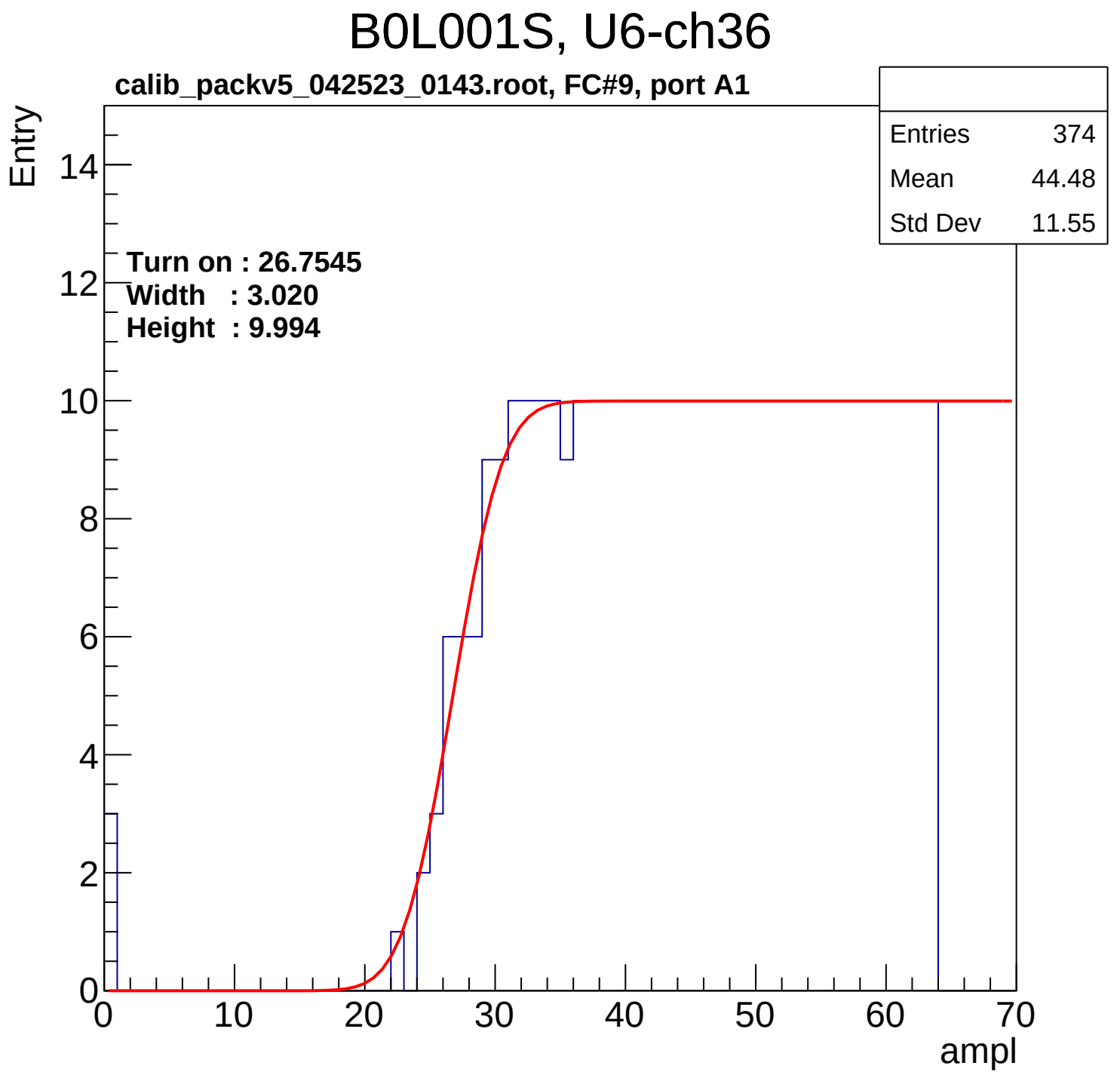
B0L001S, U6-ch36
calib_packv5_042523_0143.root, FC#9, port A1
Entries 374
Mean 44.48
Std Dev 11.55
Turn on : 26.7545
Width : 3.020
Height : 9.994
Entry
ampl
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2
4
6
8
10
12
14
0
10
20
30
40
50
60
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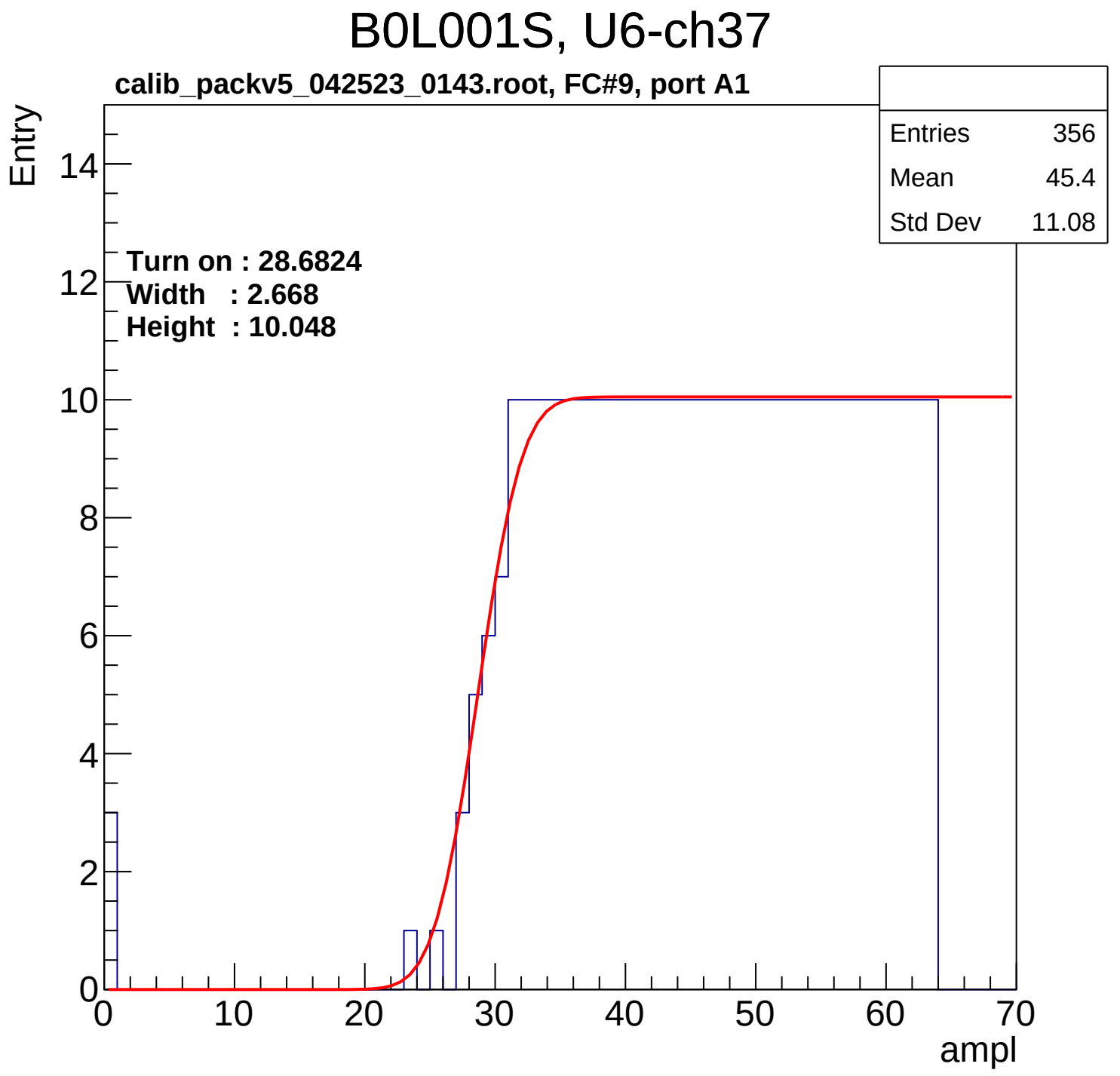
B0L001S, U6-ch37
calib_packv5_042523_0143.root, FC#9, port A1
Entries 356
Mean 45.4
Std Dev 11.08
Turn on : 28.6824
Width : 2.668
Height : 10.048
Entry
ampl
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2
4
6
8
10
12
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0
10
20
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60
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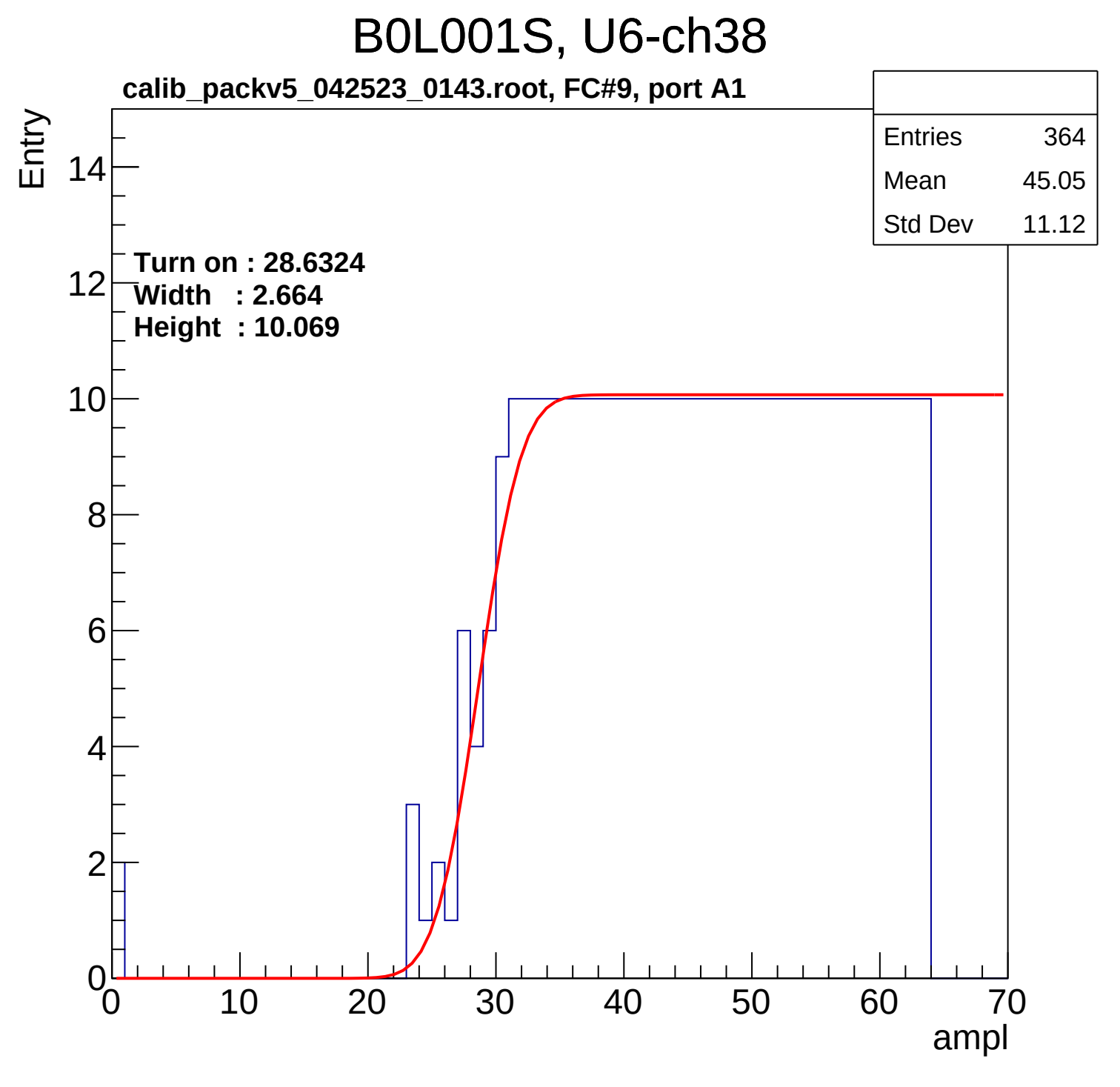
B0L001S, U6-ch38
calib_packv5_042523_0143.root, FC#9, port A1
Entries 364
Mean 45.05
Std Dev 11.12
Turn on : 28.6324
Width : 2.664
Height : 10.069
Entry
ampl
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2
4
6
8
10
12
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60
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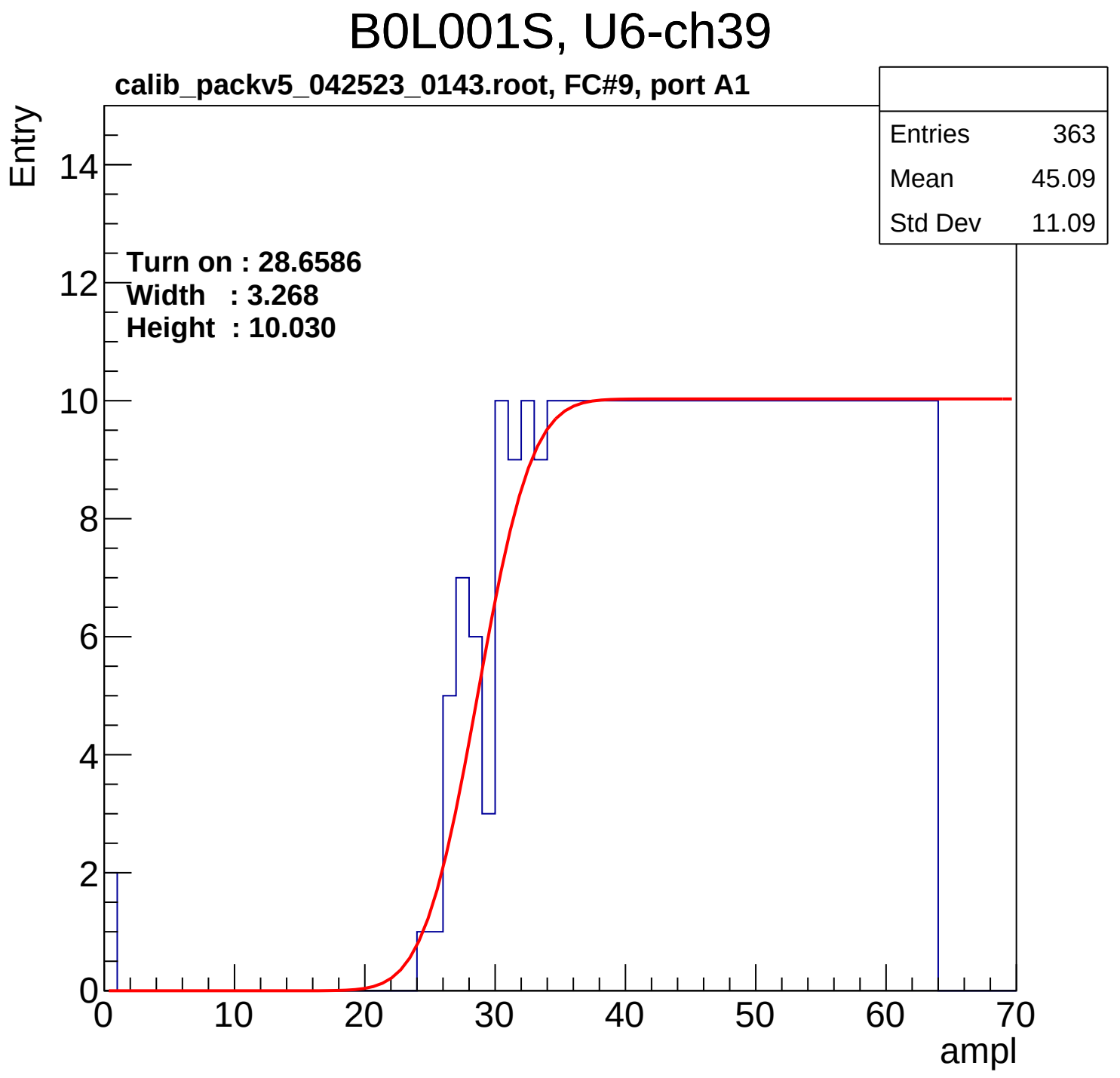
B0L001S, U6-ch39
calib_packv5_042523_0143.root, FC#9, port A1
Entries 363
Mean 45.09
Std Dev 11.09
Turn on : 28.6586
Width : 3.268
Height : 10.030
Entry
ampl
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4
6
8
10
12
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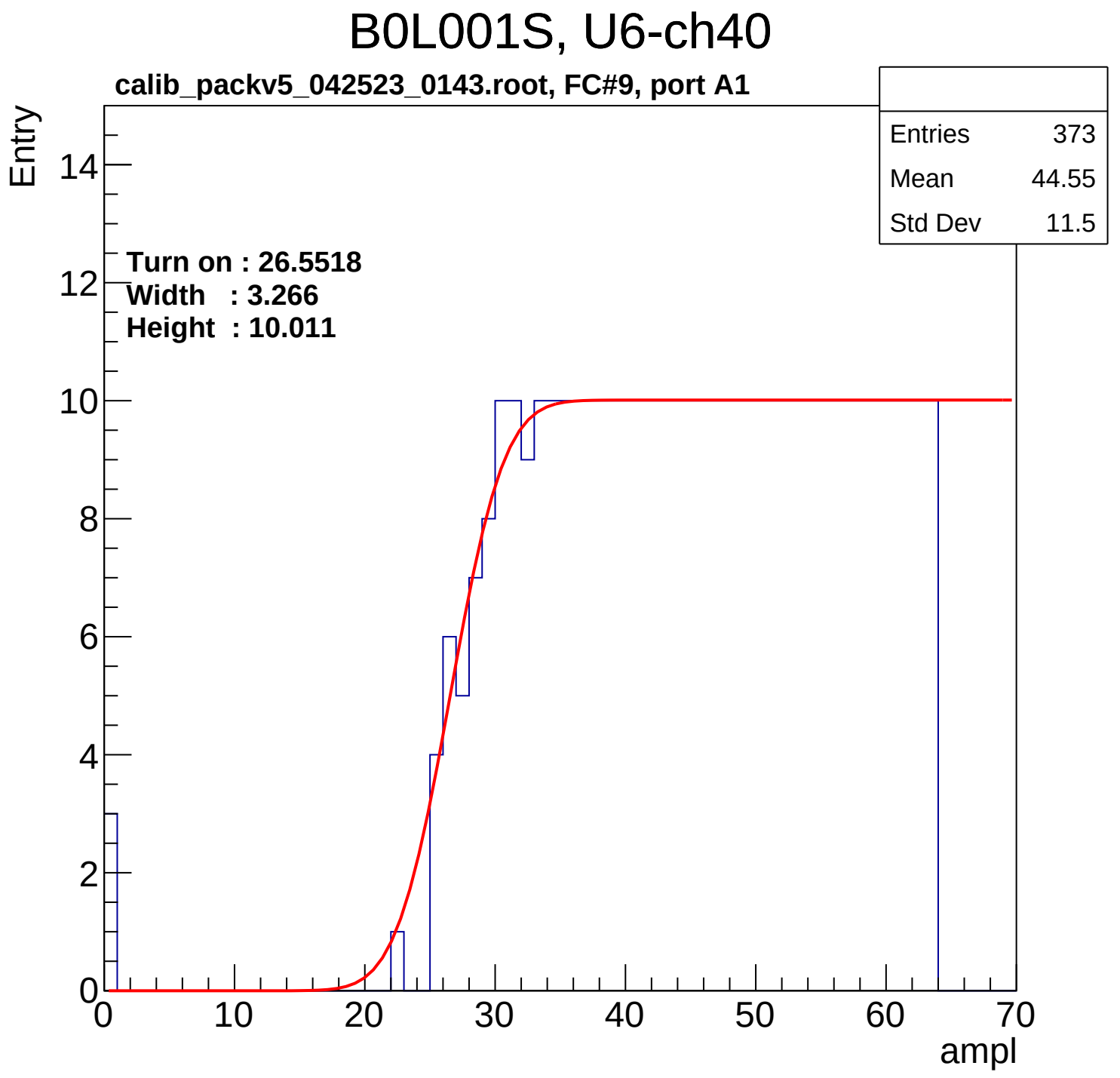
B0L001S, U6-ch40
calib_packv5_042523_0143.root, FC#9, port A1
Entries 373
Mean 44.55
Std Dev 11.5
Turn on : 26.5518
Width : 3.266
Height : 10.011
Entry
ampl
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6
8
10
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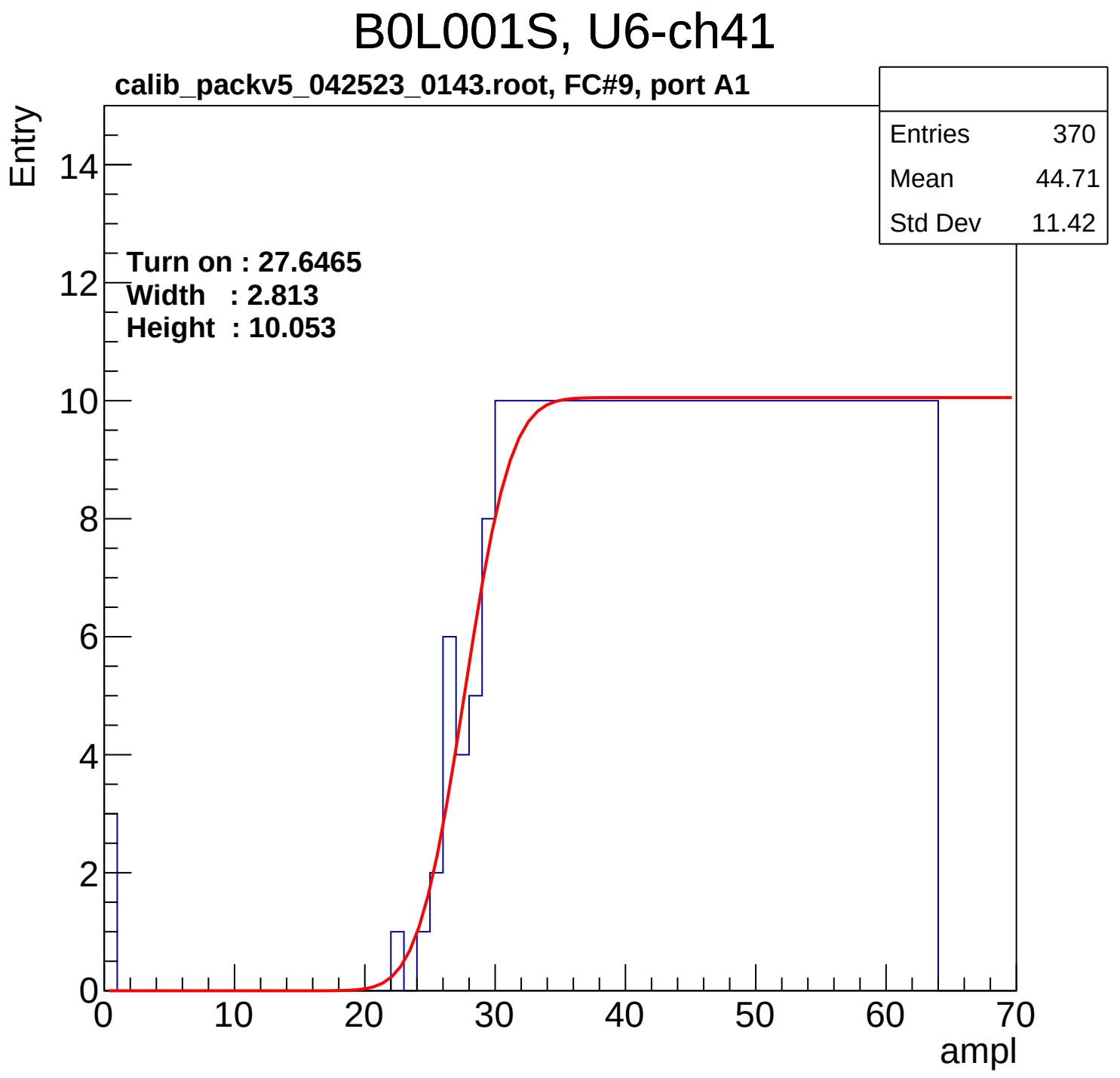
B0L001S, U6-ch41
calib_packv5_042523_0143.root, FC#9, port A1
Entries 370
Mean 44.71
Std Dev 11.42
Turn on : 27.6465
Width : 2.813
Height : 10.053
Entry
ampl
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6
8
10
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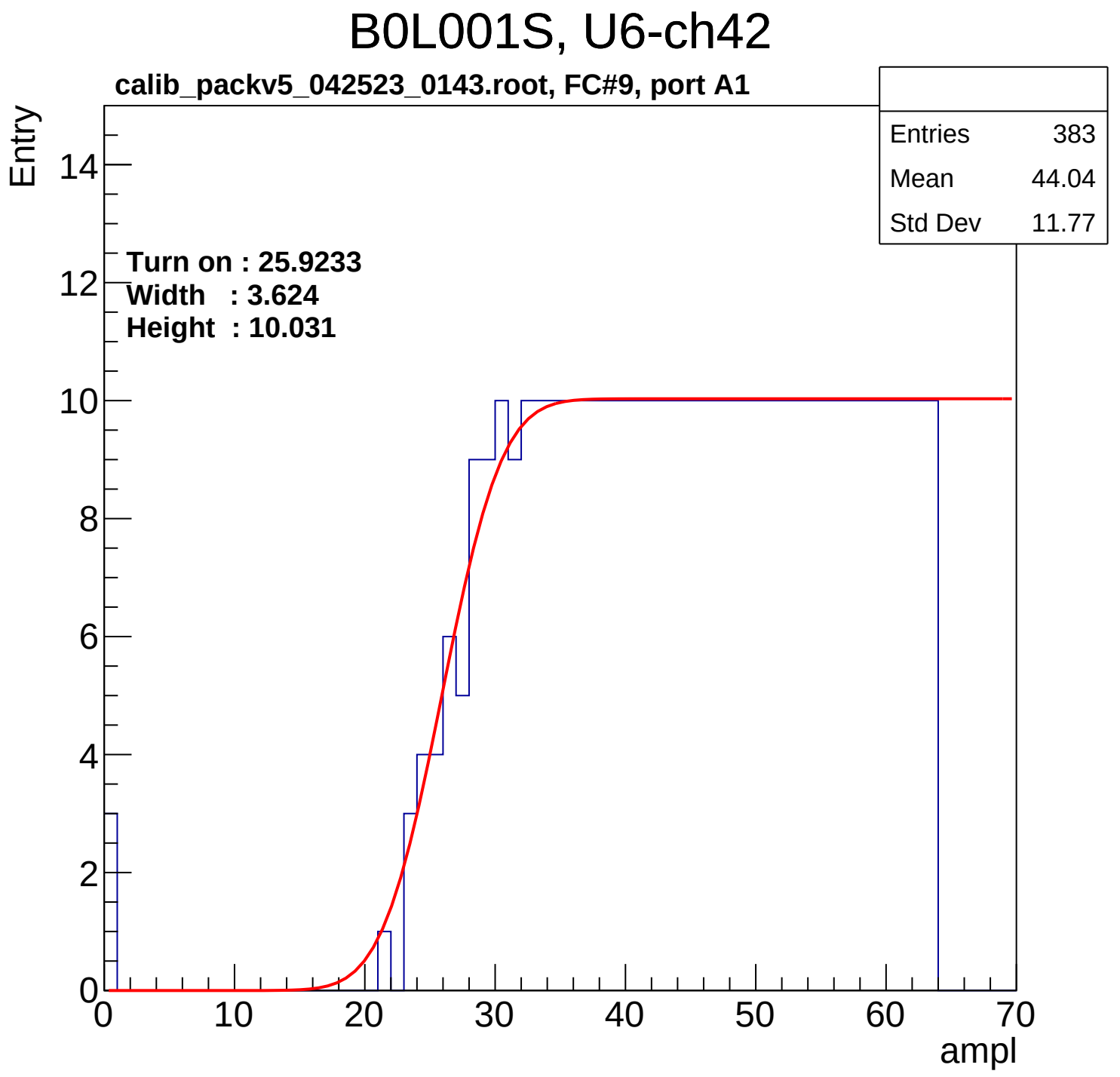
B0L001S, U6-ch42
calib_packv5_042523_0143.root, FC#9, port A1
Entries 383
Mean 44.04
Std Dev 11.77
Turn on : 25.9233
Width : 3.624
Height : 10.031
Entry
ampl
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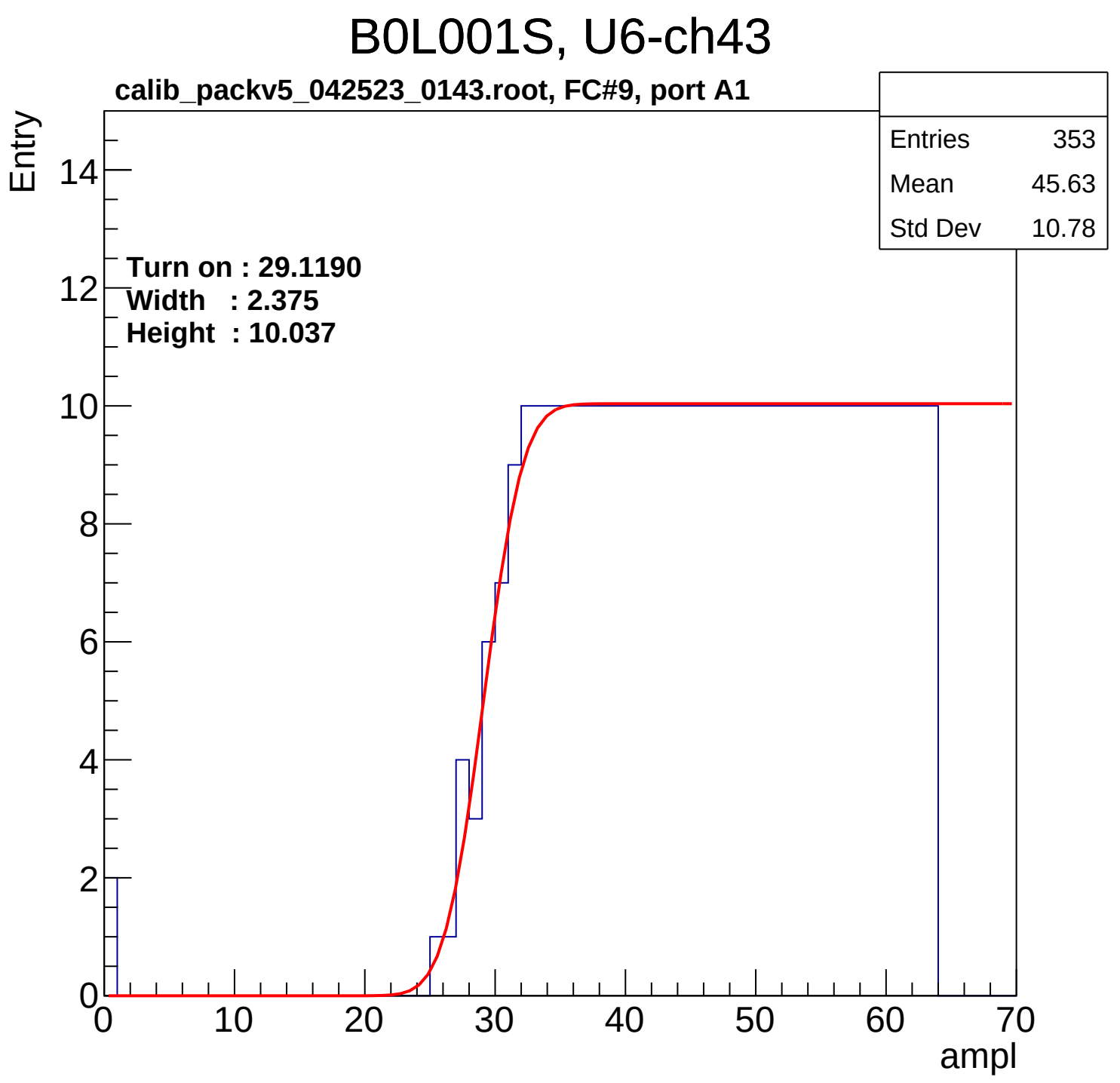
B0L001S, U6-ch43
calib_packv5_042523_0143.root, FC#9, port A1
Entries 353
Mean 45.63
Std Dev 10.78
Turn on : 29.1190
Width : 2.375
Height : 10.037
Entry
ampl
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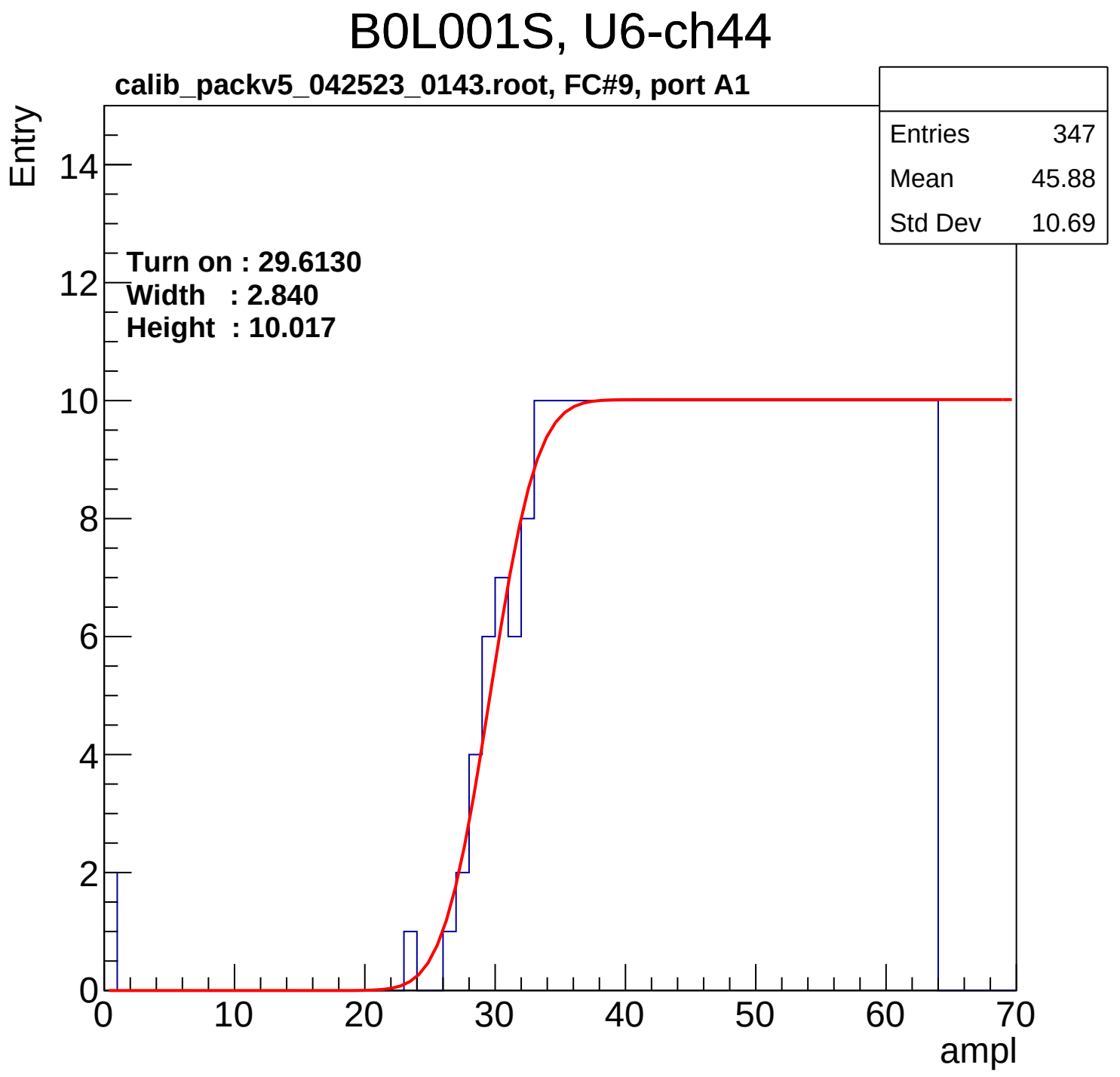
B0L001S, U6-ch44
calib_packv5_042523_0143.root, FC#9, port A1
Entries 347
Mean 45.88
Std Dev 10.69
Turn on : 29.6130
Width : 2.840
Height : 10.017
Entry
ampl
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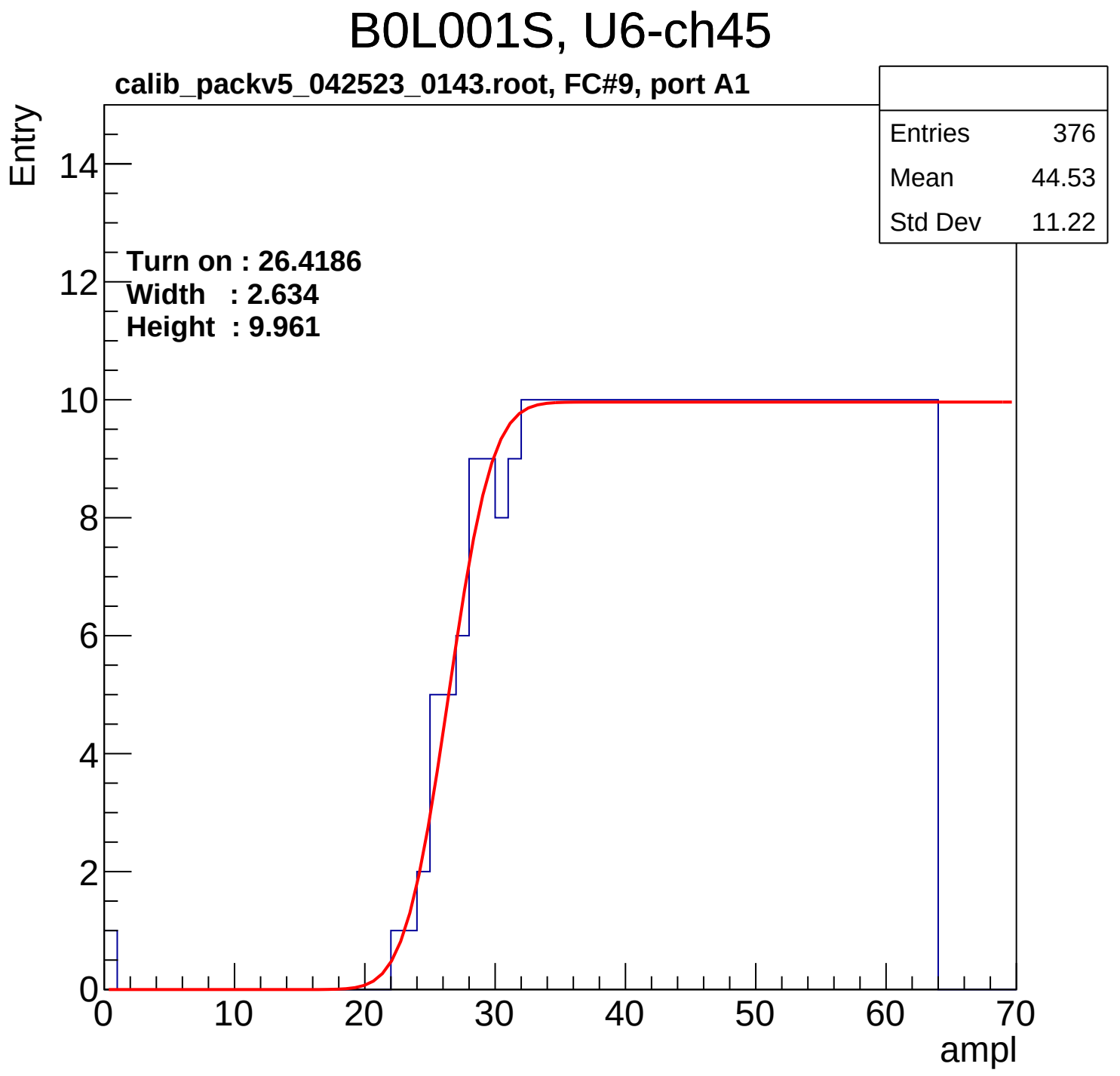
B0L001S, U6-ch45
calib_packv5_042523_0143.root, FC#9, port A1
Entries 376
Mean 44.53
Std Dev 11.22
Turn on : 26.4186
Width : 2.634
Height : 9.961
Entry
ampl
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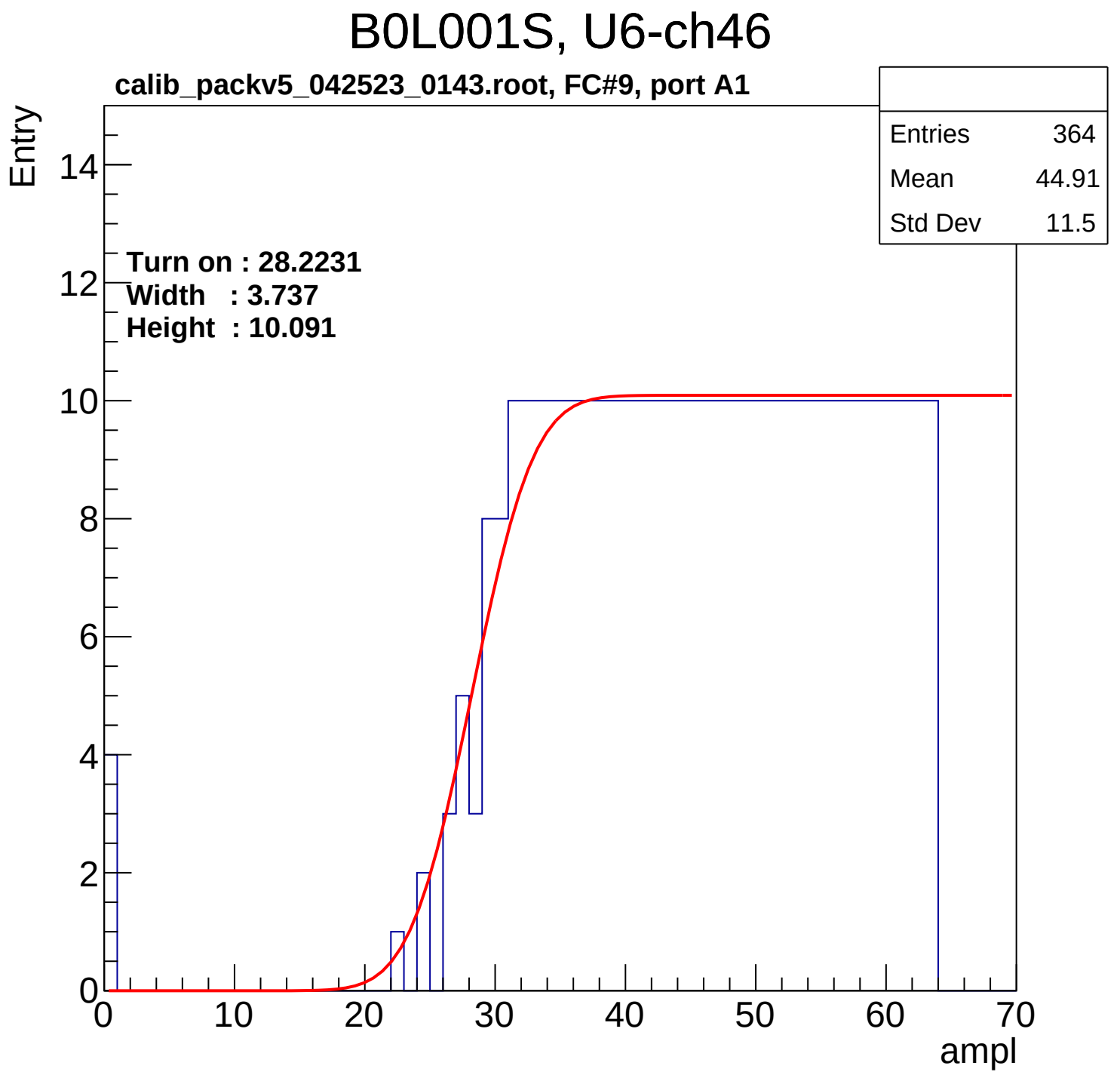
B0L001S, U6-ch46
calib_packv5_042523_0143.root, FC#9, port A1
Entries 364
Mean 44.91
Std Dev 11.5
Turn on : 28.2231
Width : 3.737
Height : 10.091
Entry
ampl
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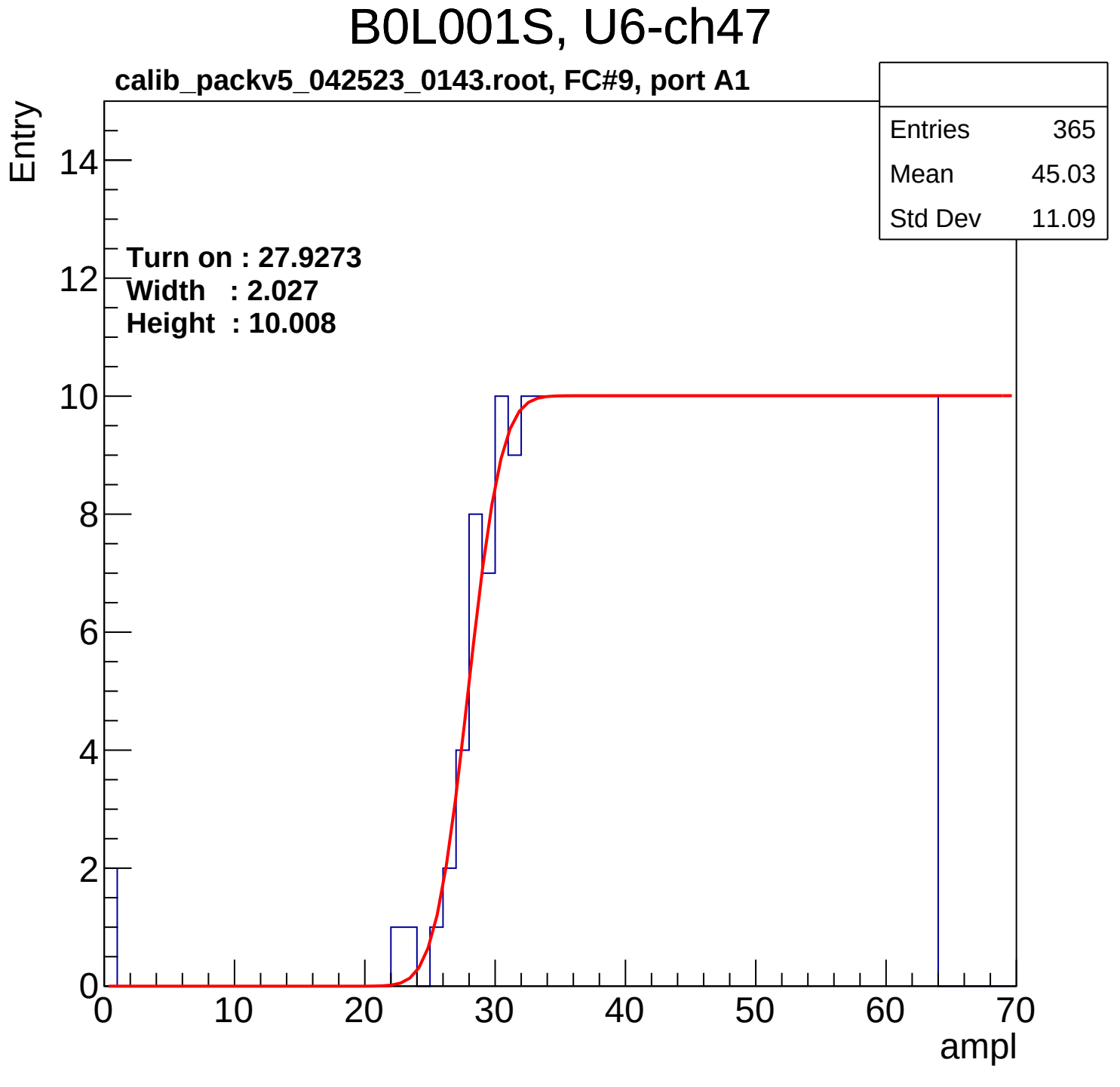
B0L001S, U6-ch47
calib_packv5_042523_0143.root, FC#9, port A1
Entries 365
Mean 45.03
Std Dev 11.09
Turn on : 27.9273
Width : 2.027
Height : 10.008
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ampl
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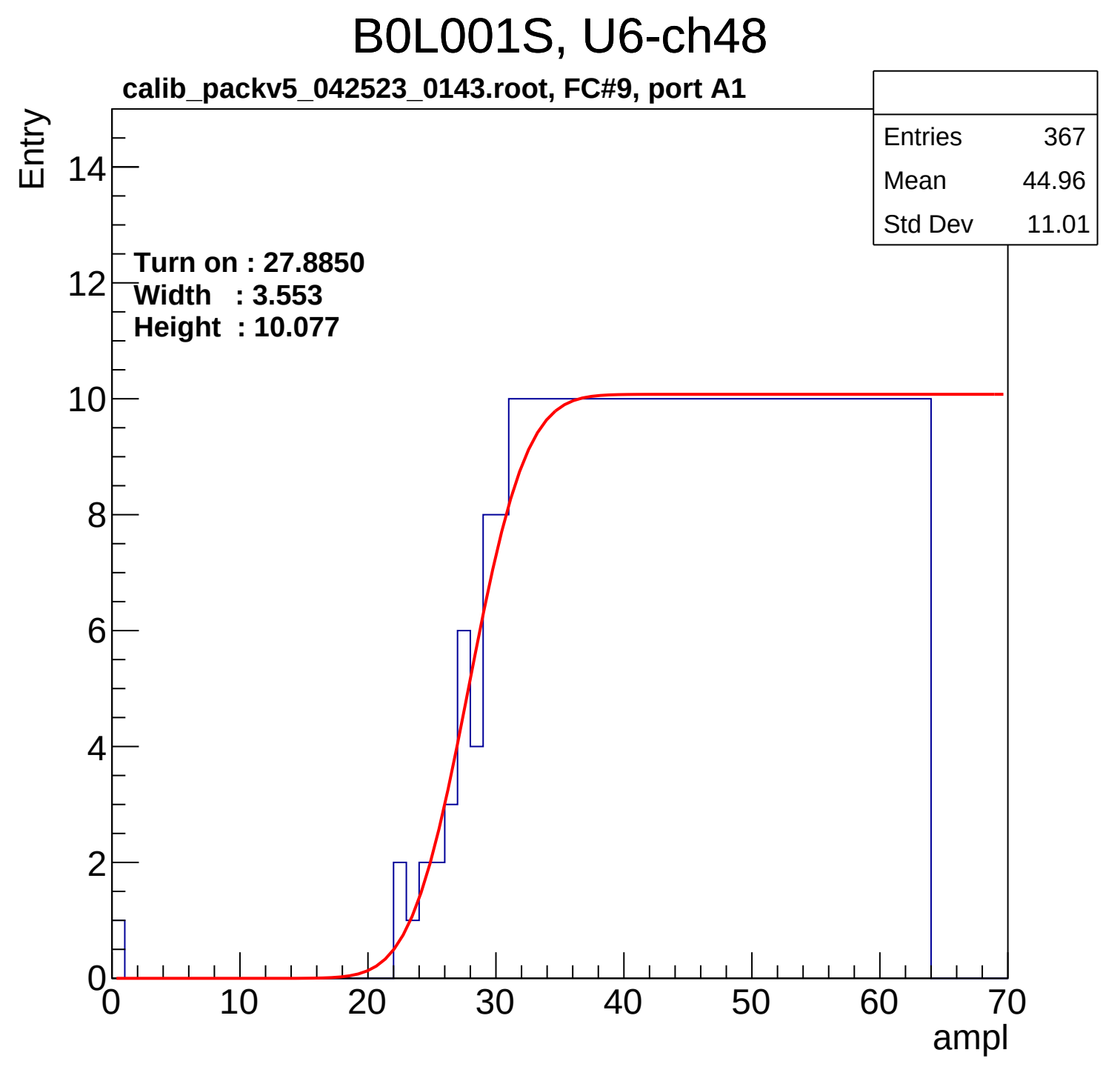
B0L001S, U6-ch48
calib_packv5_042523_0143.root, FC#9, port A1
Entries 367
Mean 44.96
Std Dev 11.01
Turn on : 27.8850
Width : 3.553
Height : 10.077
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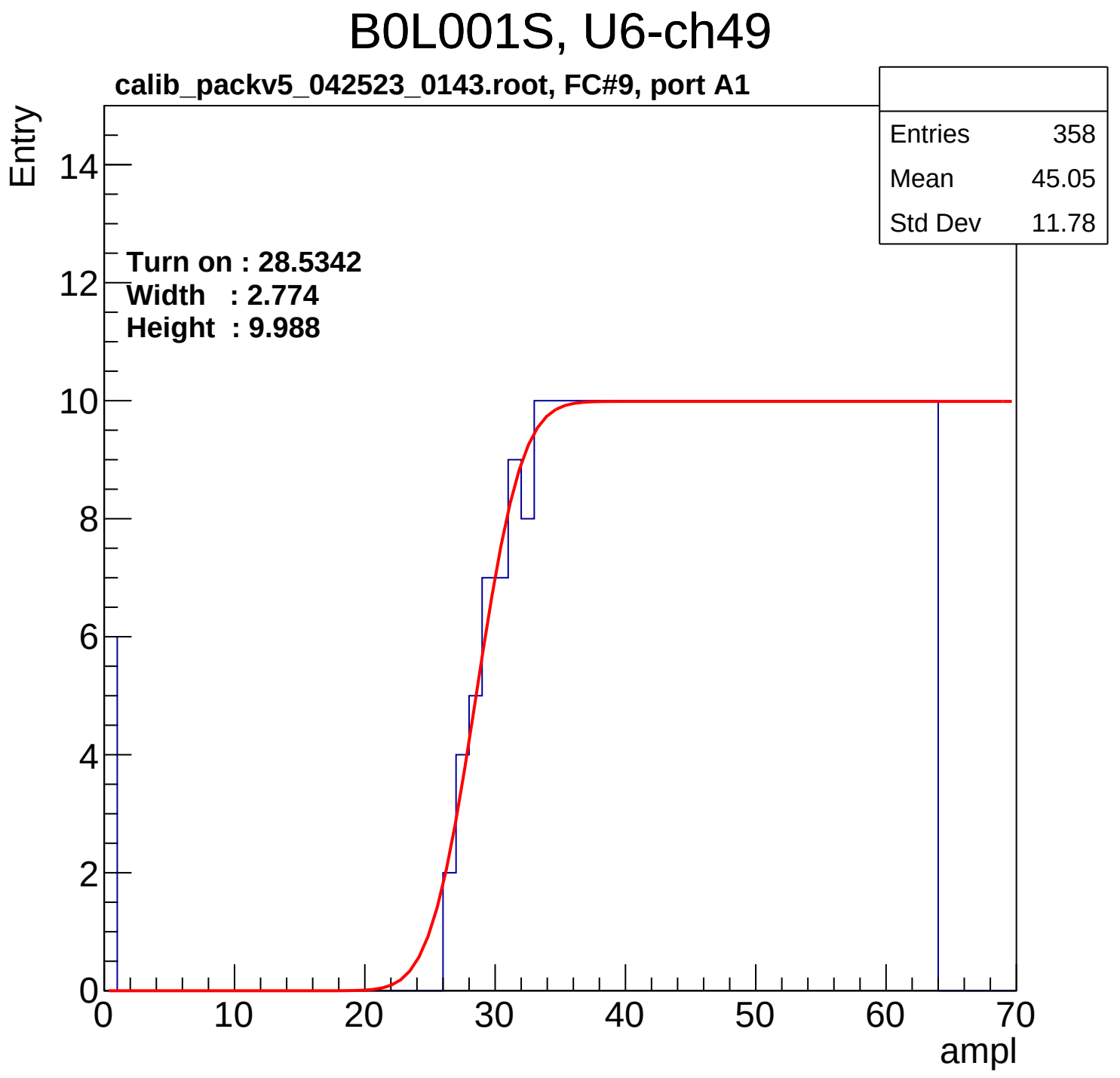
B0L001S, U6-ch49
calib_packv5_042523_0143.root, FC#9, port A1
Entries 358
Mean 45.05
Std Dev 11.78
Turn on : 28.5342
Width : 2.774
Height : 9.988
Entry
ampl
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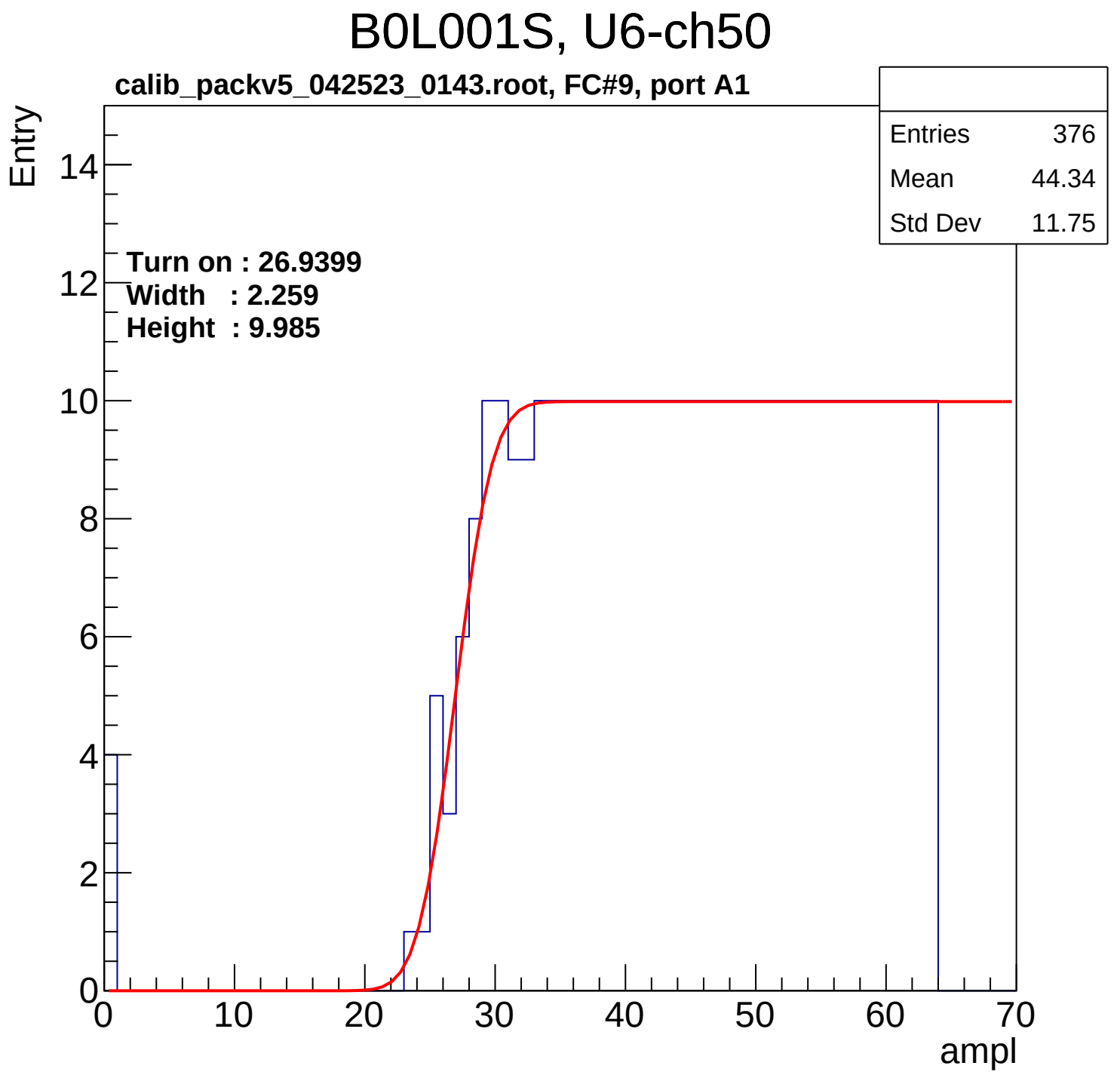
B0L001S, U6-ch50
calib_packv5_042523_0143.root, FC#9, port A1
Entries 376
Mean 44.34
Std Dev 11.75
Turn on : 26.9399
Width : 2.259
Height : 9.985
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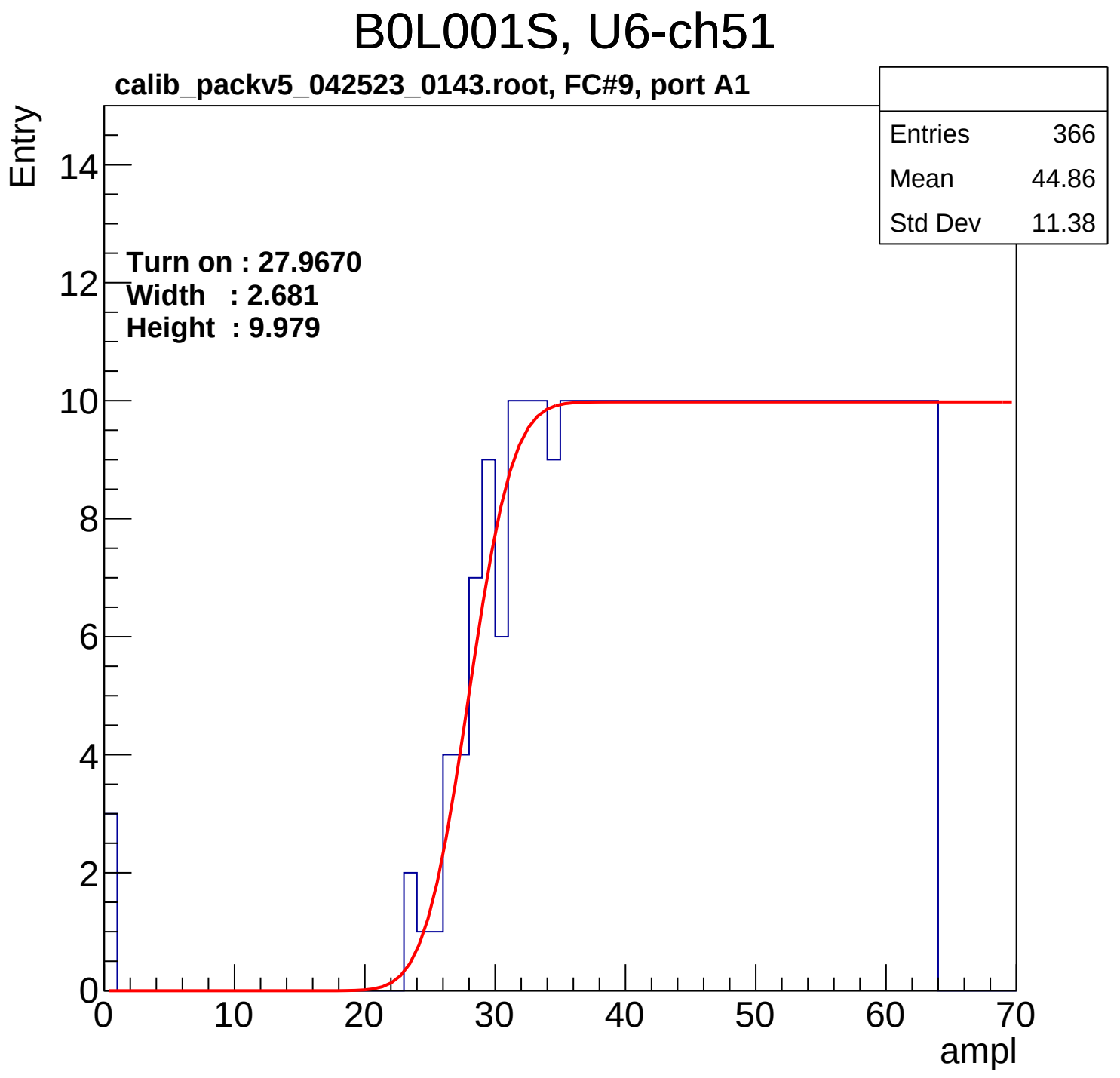
B0L001S, U6-ch51
calib_packv5_042523_0143.root, FC#9, port A1
Entries 366
Mean 44.86
Std Dev 11.38
Turn on : 27.9670
Width : 2.681
Height : 9.979
Entry
ampl
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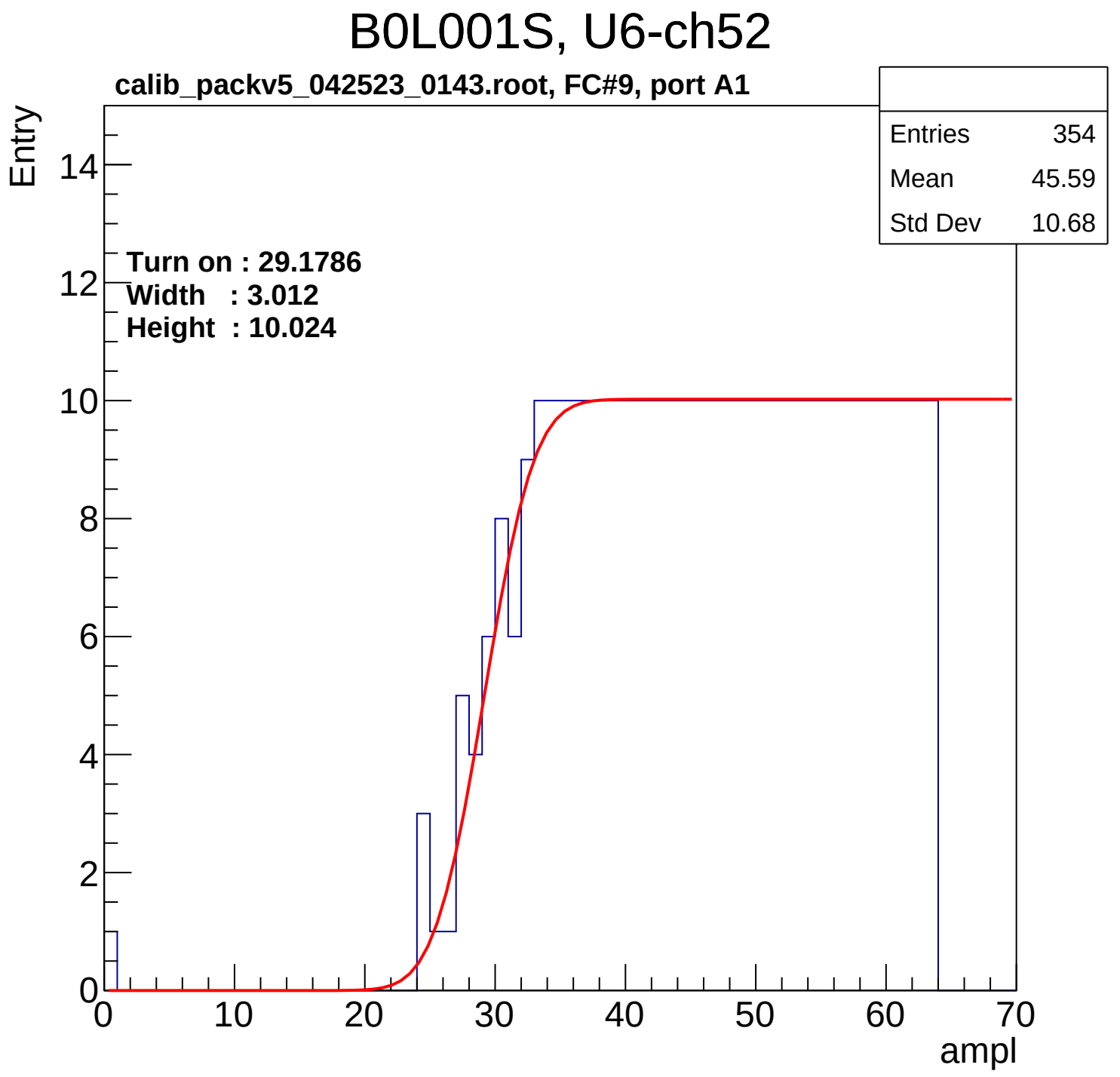
B0L001S, U6-ch52
calib_packv5_042523_0143.root, FC#9, port A1
Entries 354
Mean 45.59
Std Dev 10.68
Turn on : 29.1786
Width : 3.012
Height : 10.024
Entry
ampl
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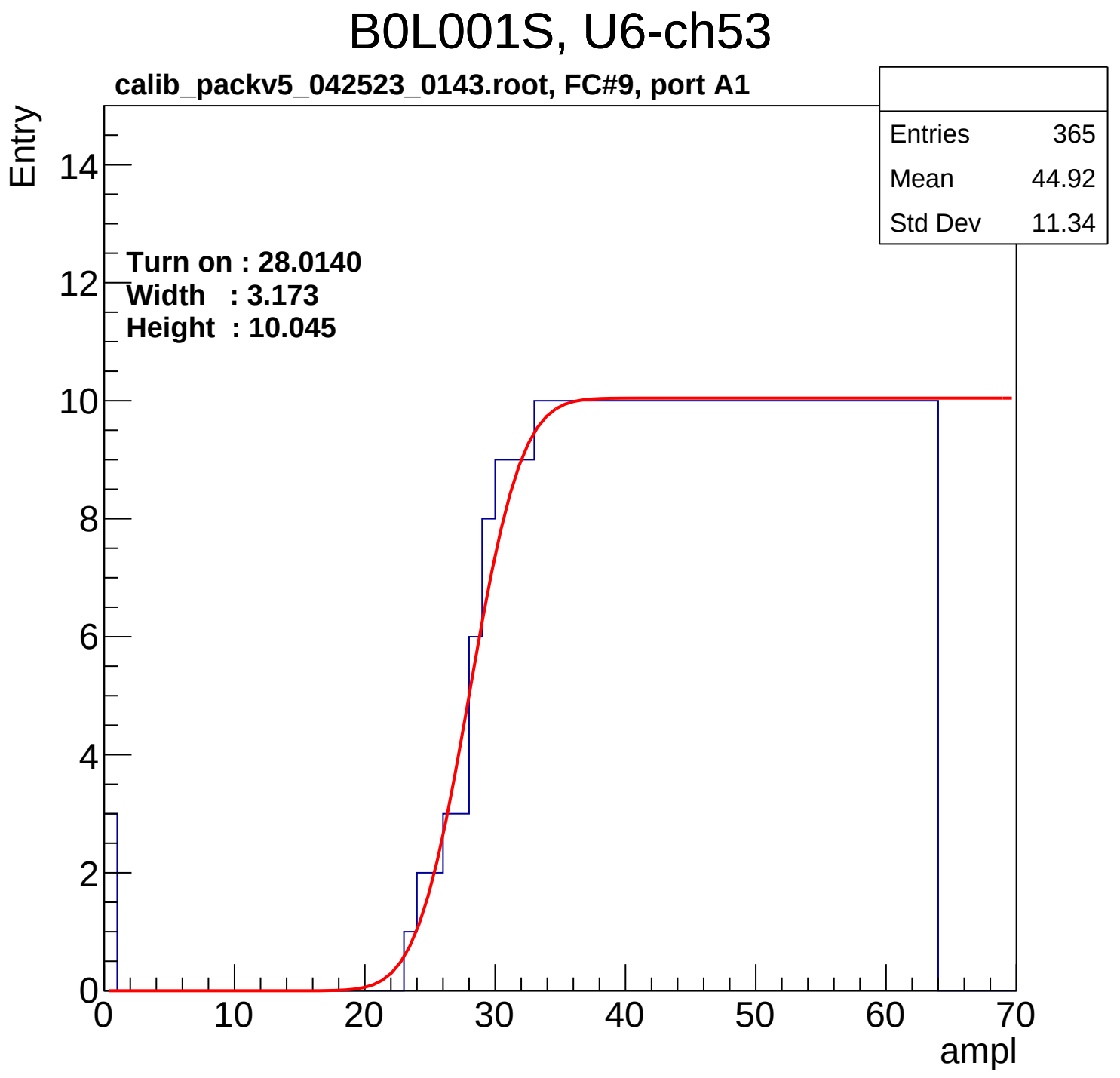
B0L001S, U6-ch53
calib_packv5_042523_0143.root, FC#9, port A1
Entries 365
Mean 44.92
Std Dev 11.34
Turn on : 28.0140
Width : 3.173
Height : 10.045
Entry
ampl
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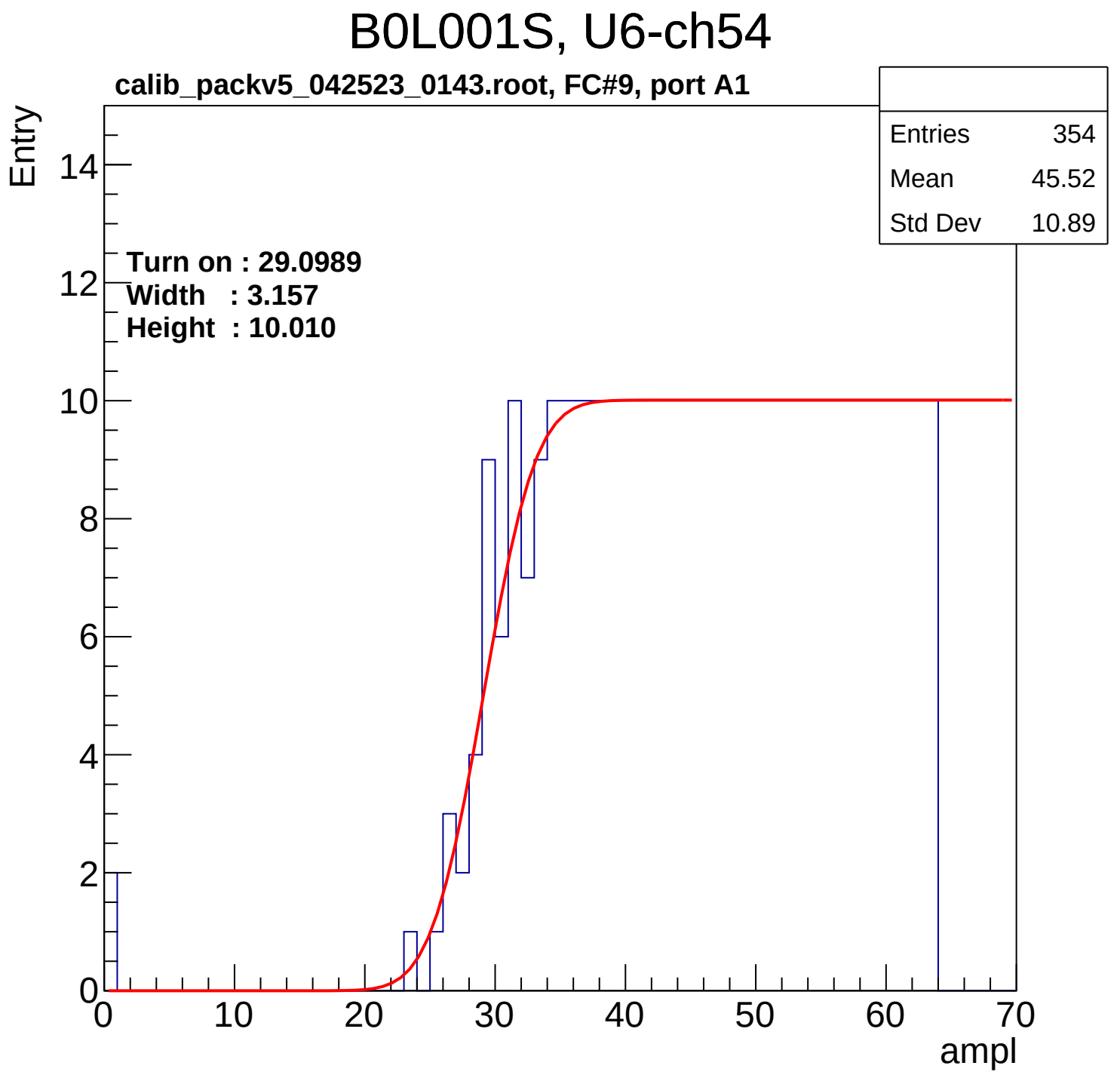
B0L001S, U6-ch54
calib_packv5_042523_0143.root, FC#9, port A1
Entries 354
Mean 45.52
Std Dev 10.89
Turn on : 29.0989
Width : 3.157
Height : 10.010
Entry
ampl
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6
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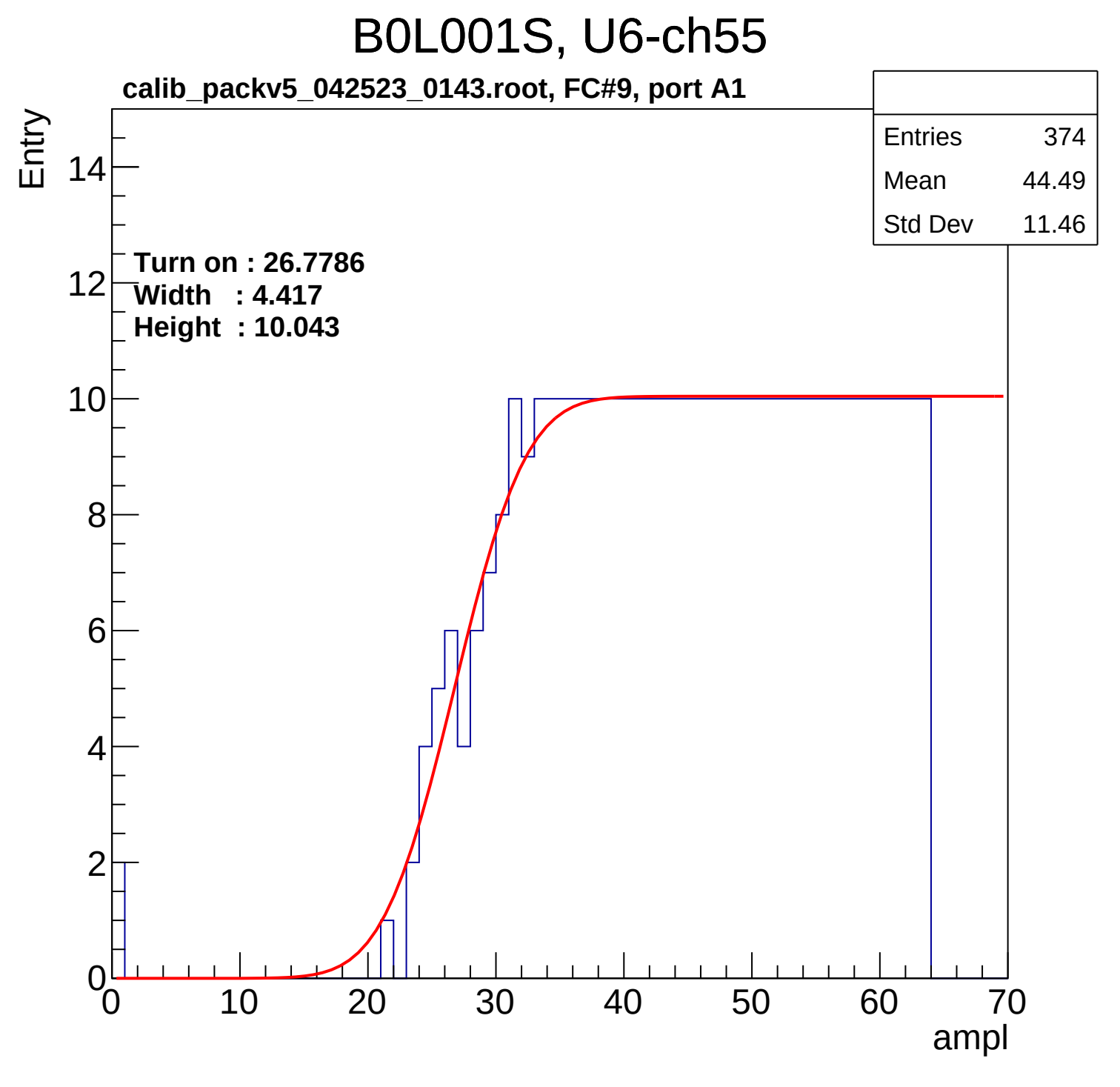
B0L001S, U6-ch55
calib_packv5_042523_0143.root, FC#9, port A1
Entries 374
Mean 44.49
Std Dev 11.46
Turn on : 26.7786
Width : 4.417
Height : 10.043
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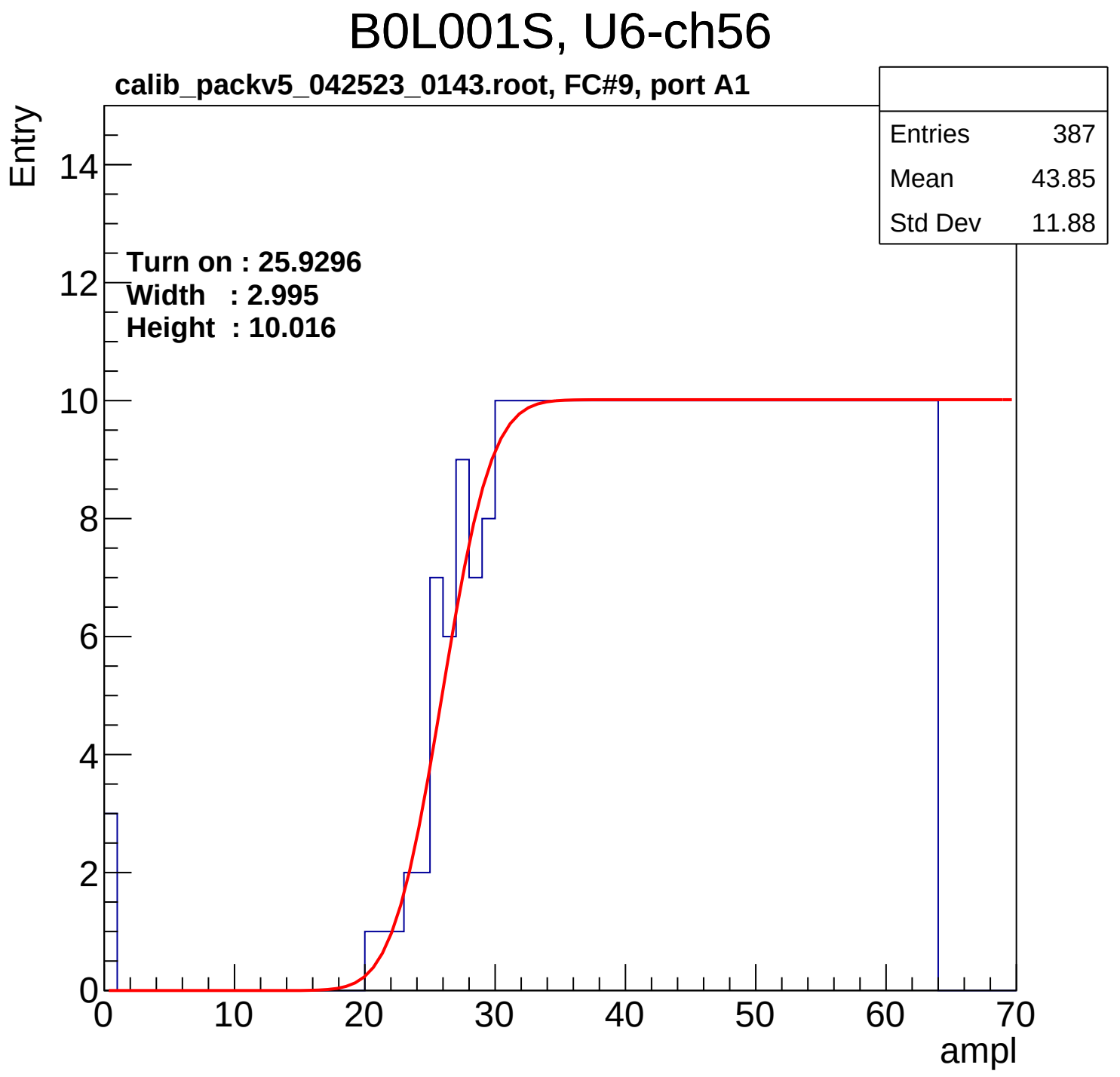
B0L001S, U6-ch56
calib_packv5_042523_0143.root, FC#9, port A1
Entries 387
Mean 43.85
Std Dev 11.88
Turn on : 25.9296
Width : 2.995
Height : 10.016
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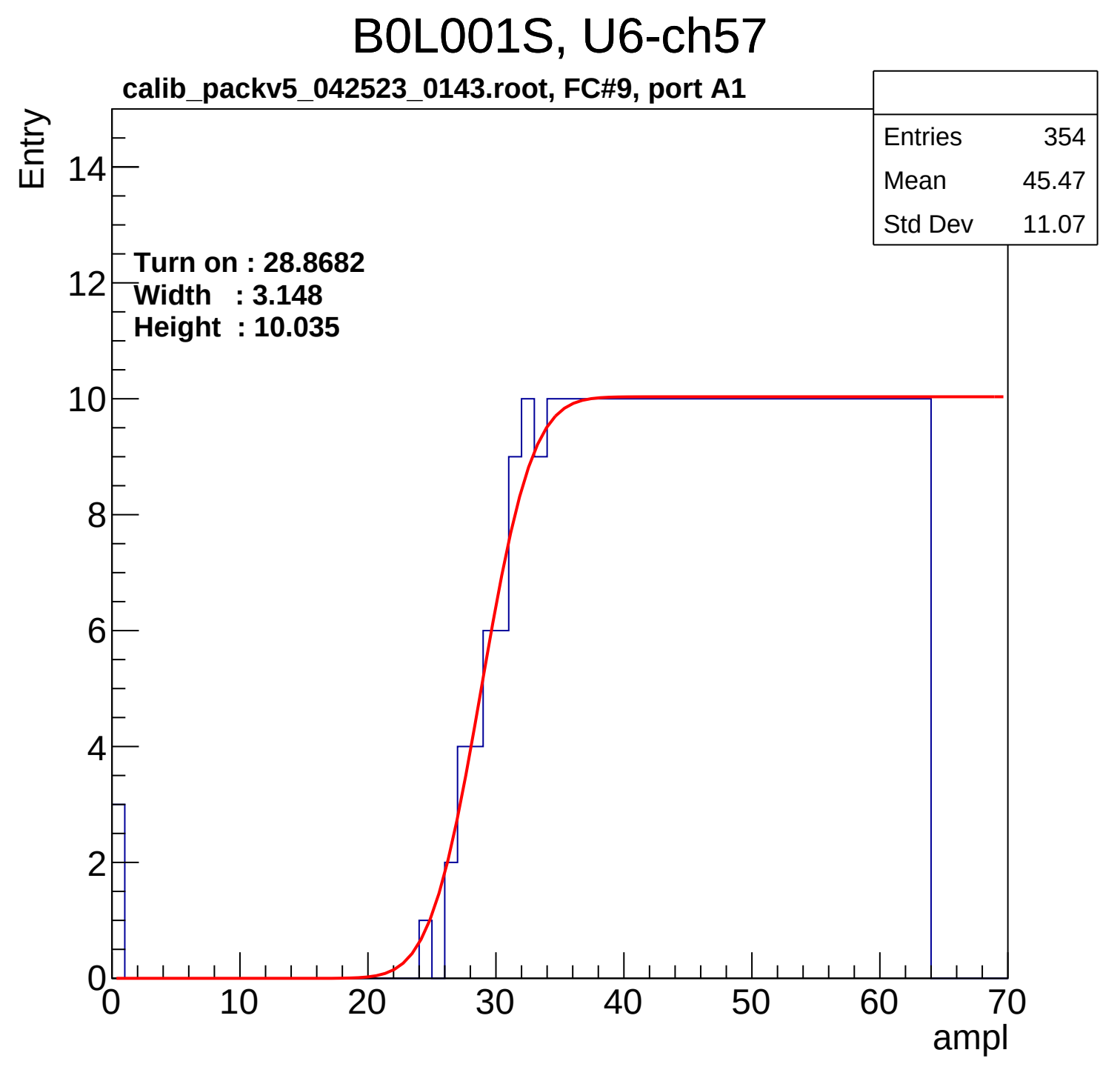
B0L001S, U6-ch57
calib_packv5_042523_0143.root, FC#9, port A1
Entries 354
Mean 45.47
Std Dev 11.07
Turn on : 28.8682
Width : 3.148
Height : 10.035
Entry
ampl
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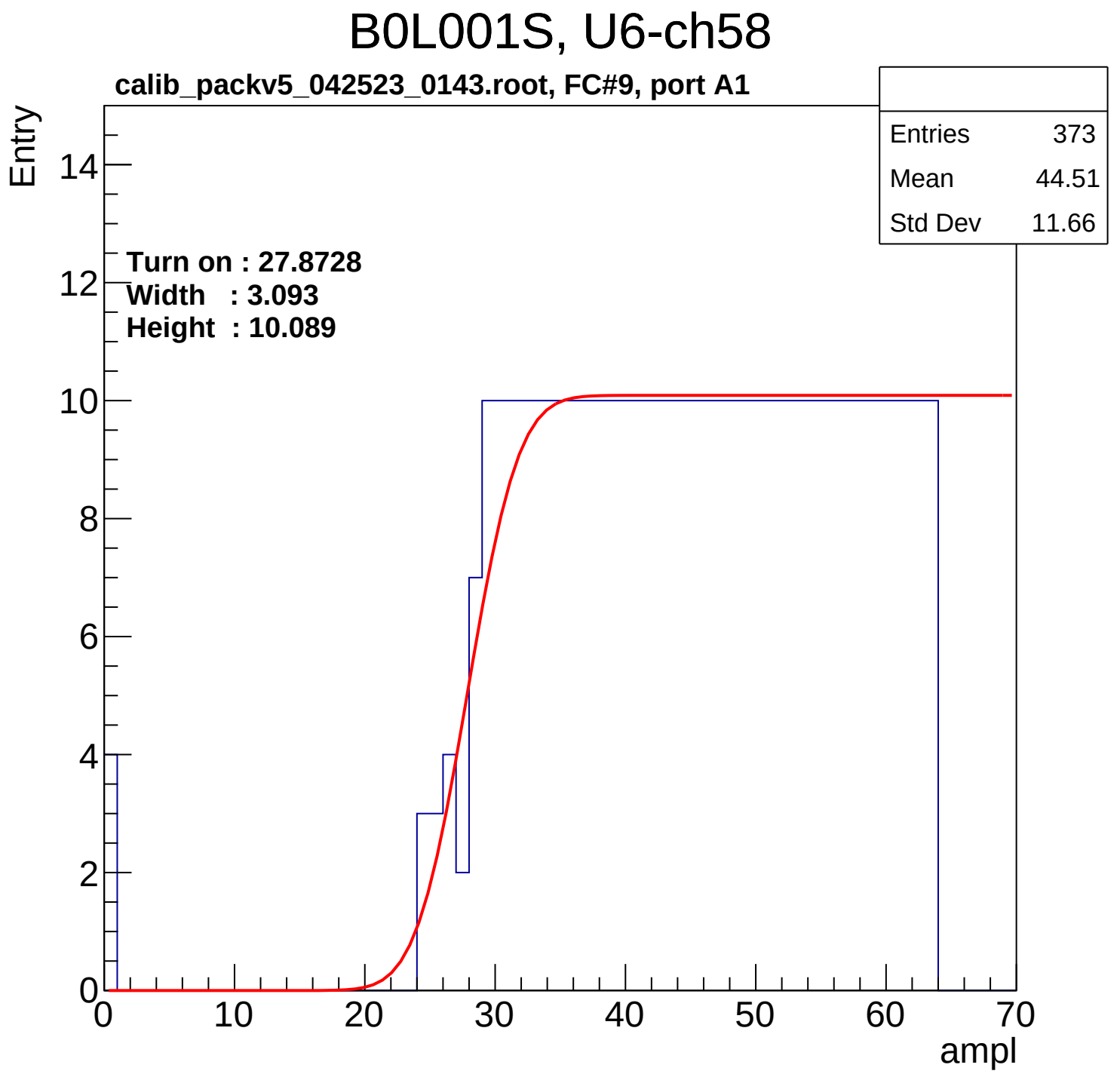
B0L001S, U6-ch58
calib_packv5_042523_0143.root, FC#9, port A1
Entries 373
Mean 44.51
Std Dev 11.66
Turn on : 27.8728
Width : 3.093
Height : 10.089
Entry
ampl
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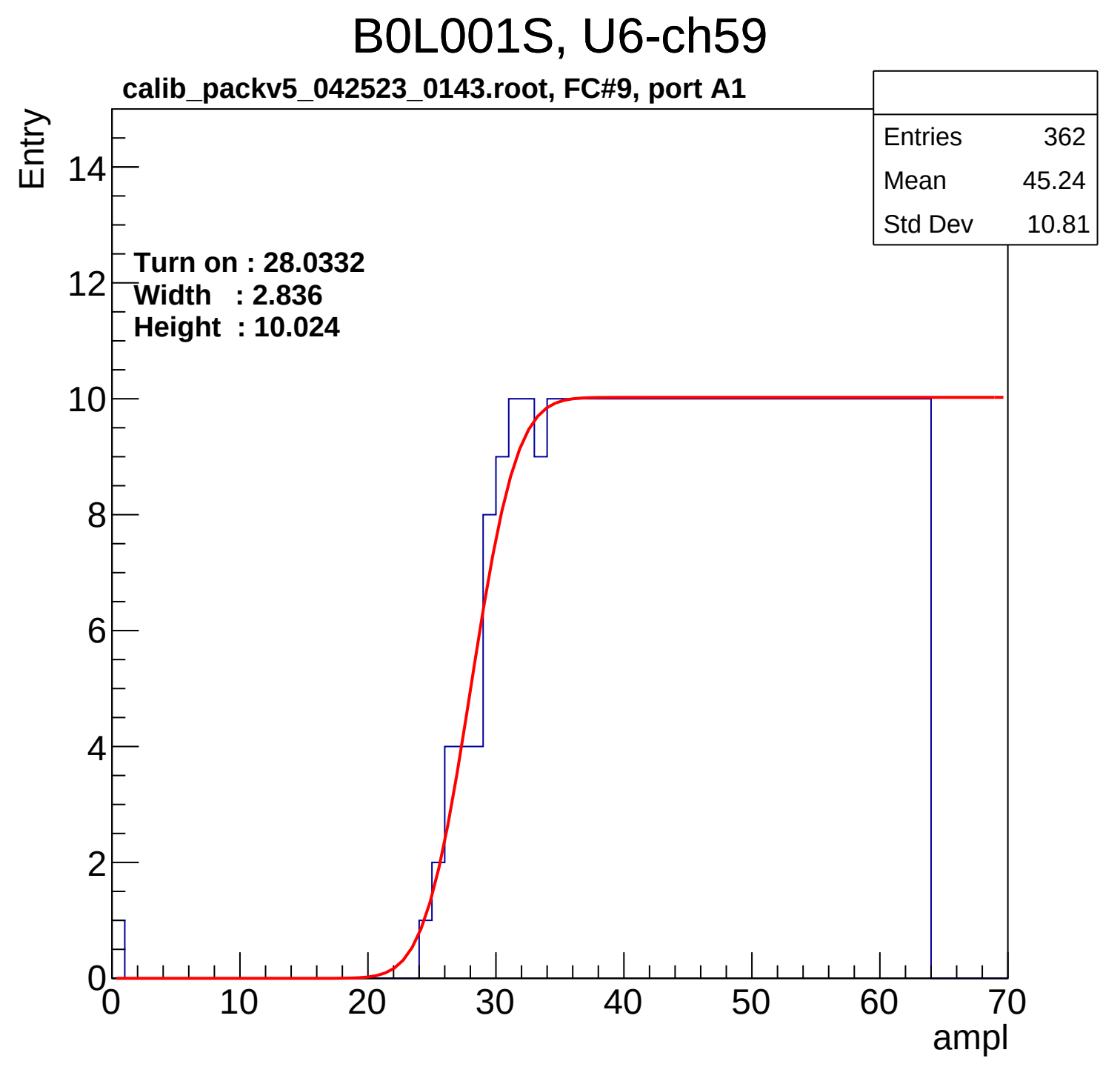
B0L001S, U6-ch59
calib_packv5_042523_0143.root, FC#9, port A1
Entries 362
Mean 45.24
Std Dev 10.81
Turn on : 28.0332
Width : 2.836
Height : 10.024
Entry
ampl
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4
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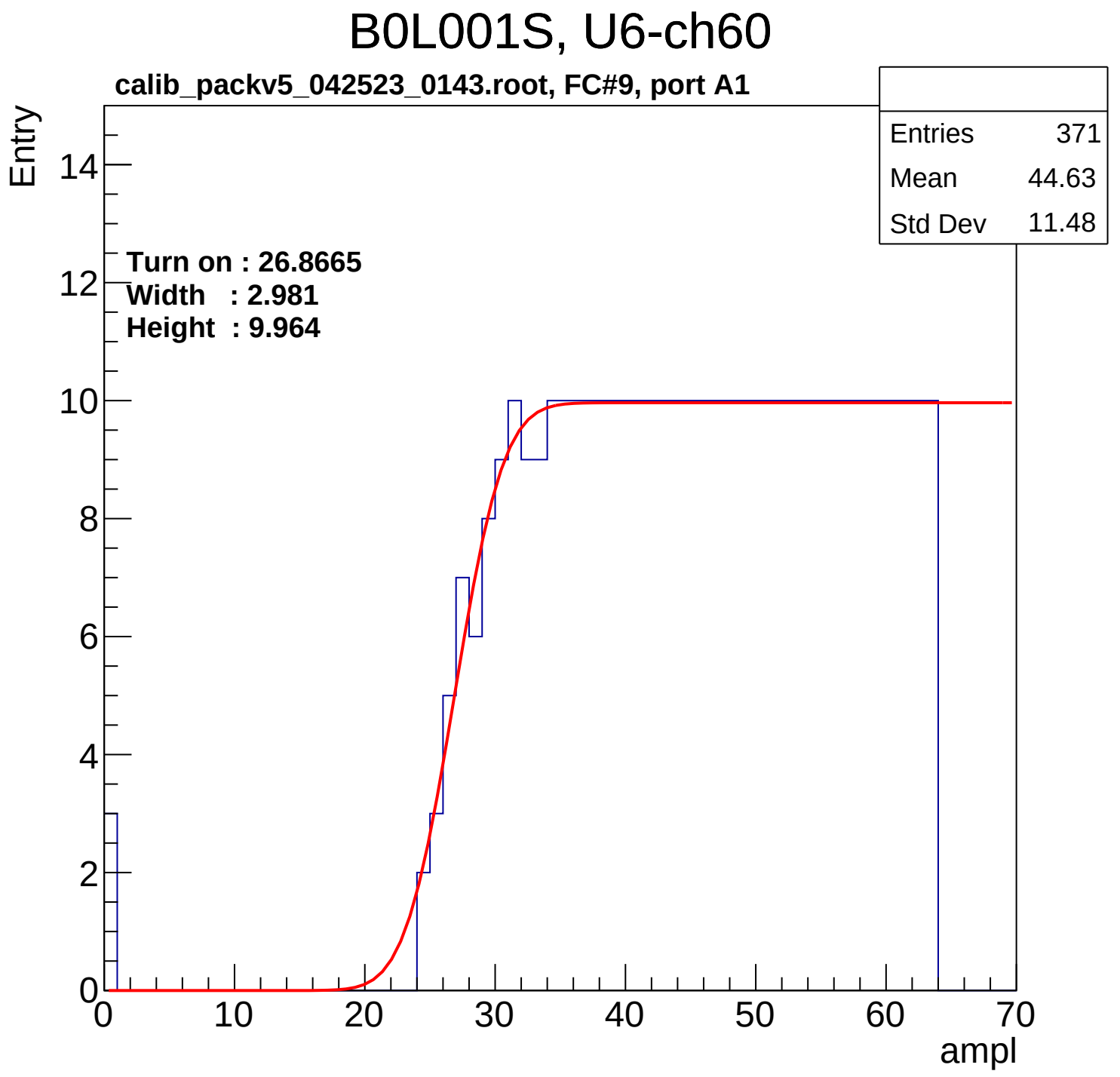
B0L001S, U6-ch60
calib_packv5_042523_0143.root, FC#9, port A1
Entries 371
Mean 44.63
Std Dev 11.48
Turn on : 26.8665
Width : 2.981
Height : 9.964
Entry
ampl
0
2
4
6
8
10
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0
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40
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60
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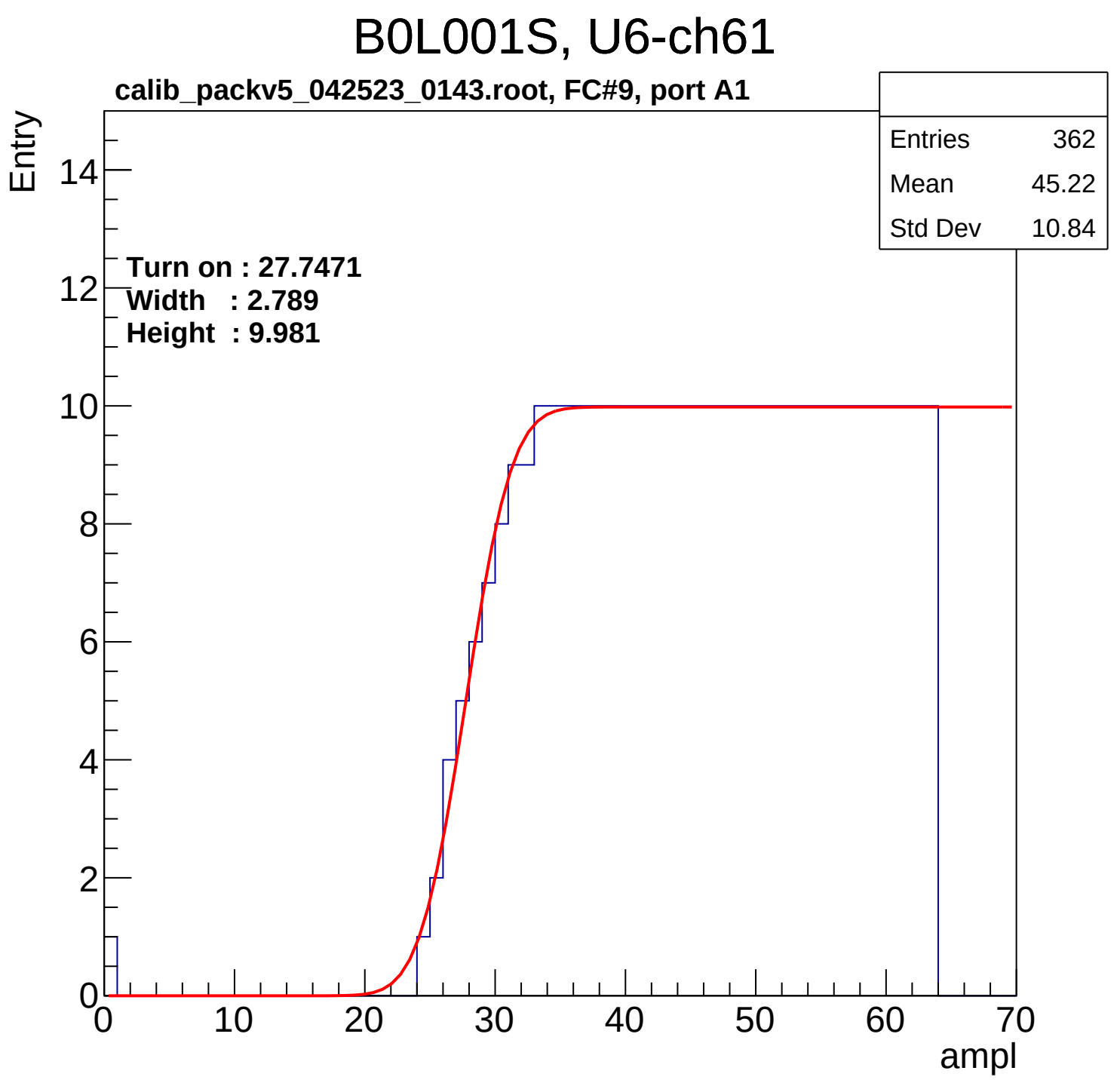
B0L001S, U6-ch61
calib_packv5_042523_0143.root, FC#9, port A1
Entries 362
Mean 45.22
Std Dev 10.84
Turn on : 27.7471
Width : 2.789
Height : 9.981
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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40
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60
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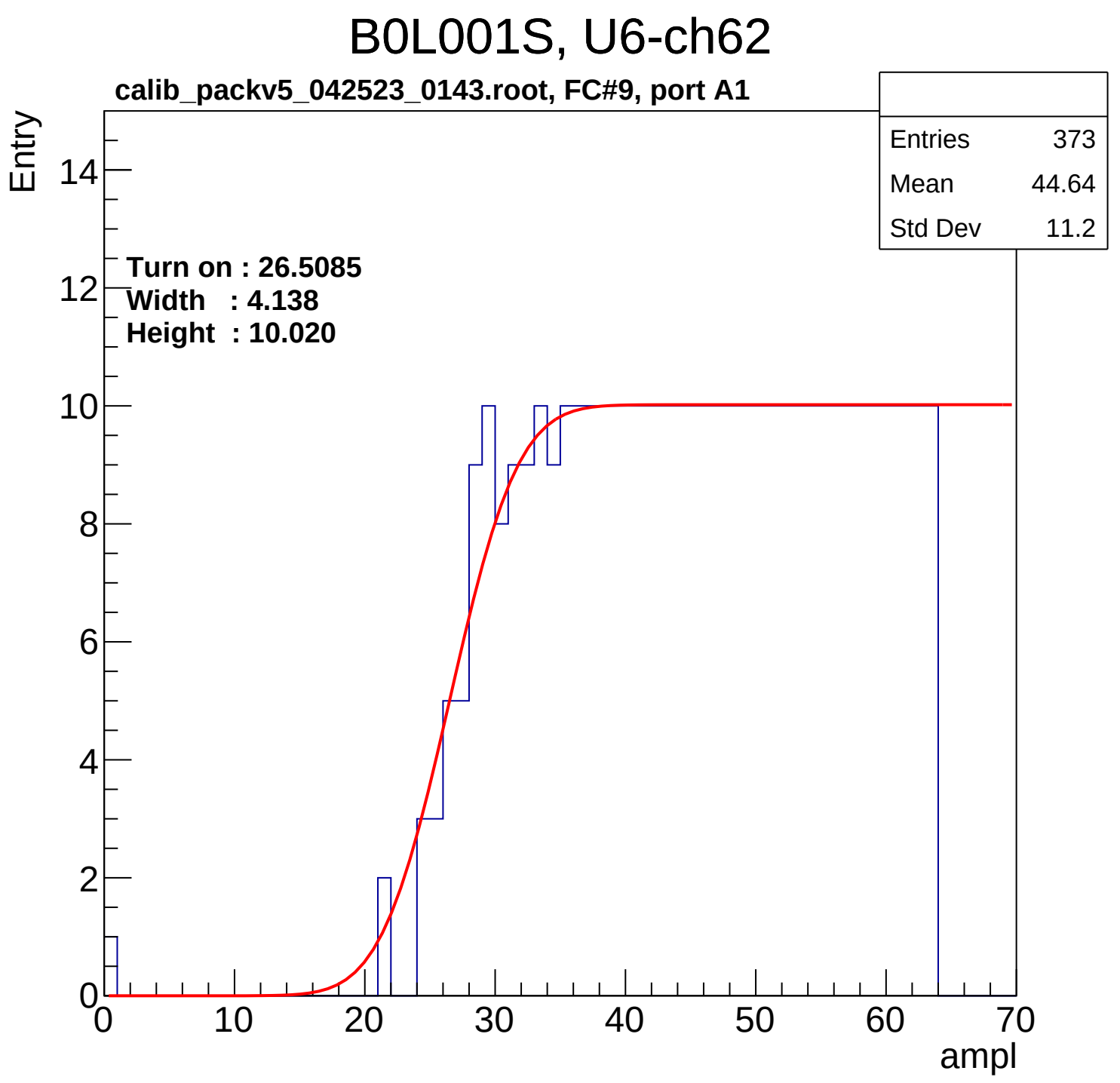
B0L001S, U6-ch62
calib_packv5_042523_0143.root, FC#9, port A1
Entries 373
Mean 44.64
Std Dev 11.2
Turn on : 26.5085
Width : 4.138
Height : 10.020
Entry
ampl
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2
4
6
8
10
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0
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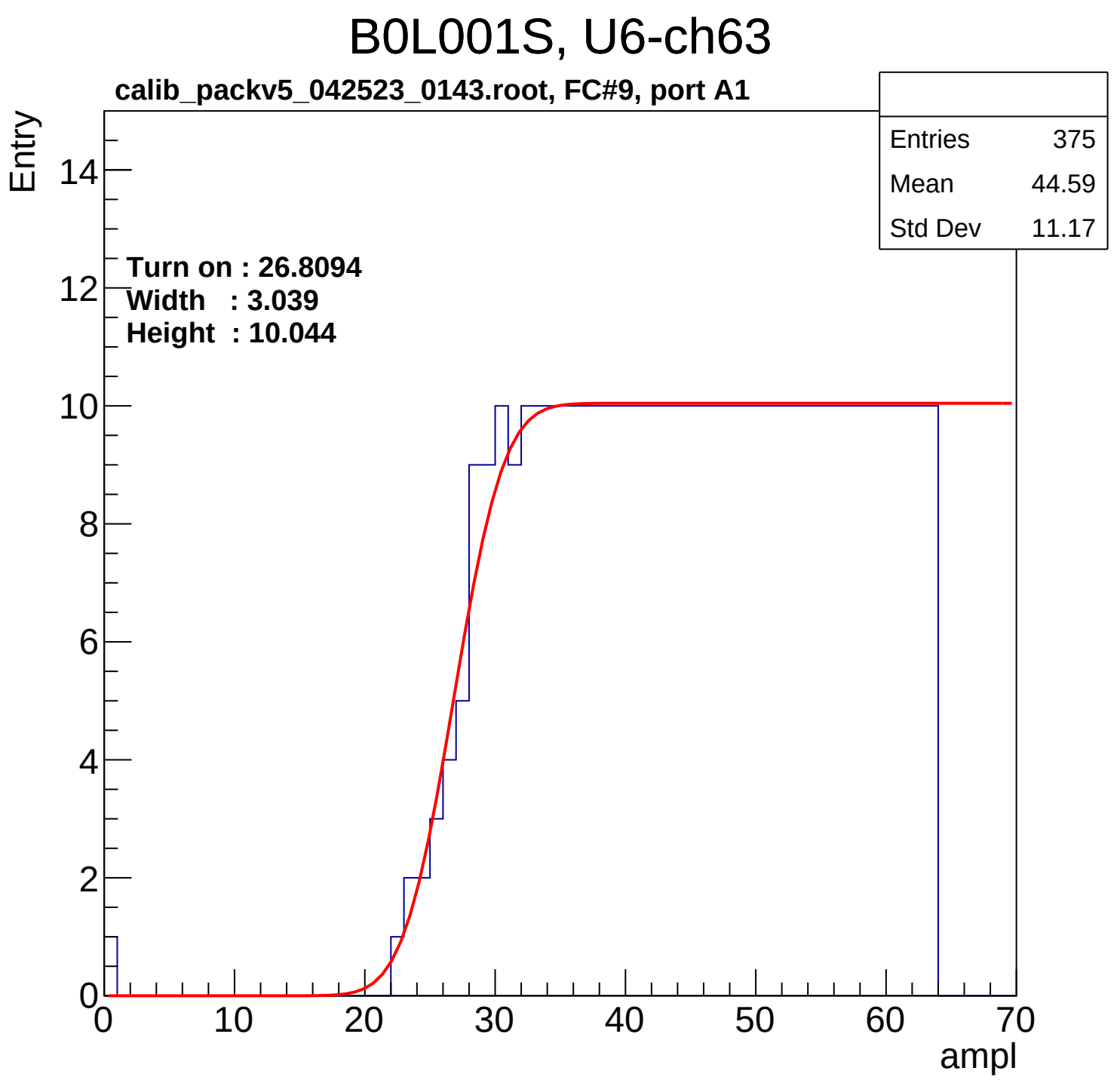
B0L001S, U6-ch63
calib_packv5_042523_0143.root, FC#9, port A1
Entries 375
Mean 44.59
Std Dev 11.17
Turn on : 26.8094
Width : 3.039
Height : 10.044
Entry
ampl
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2
4
6
8
10
12
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0
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60
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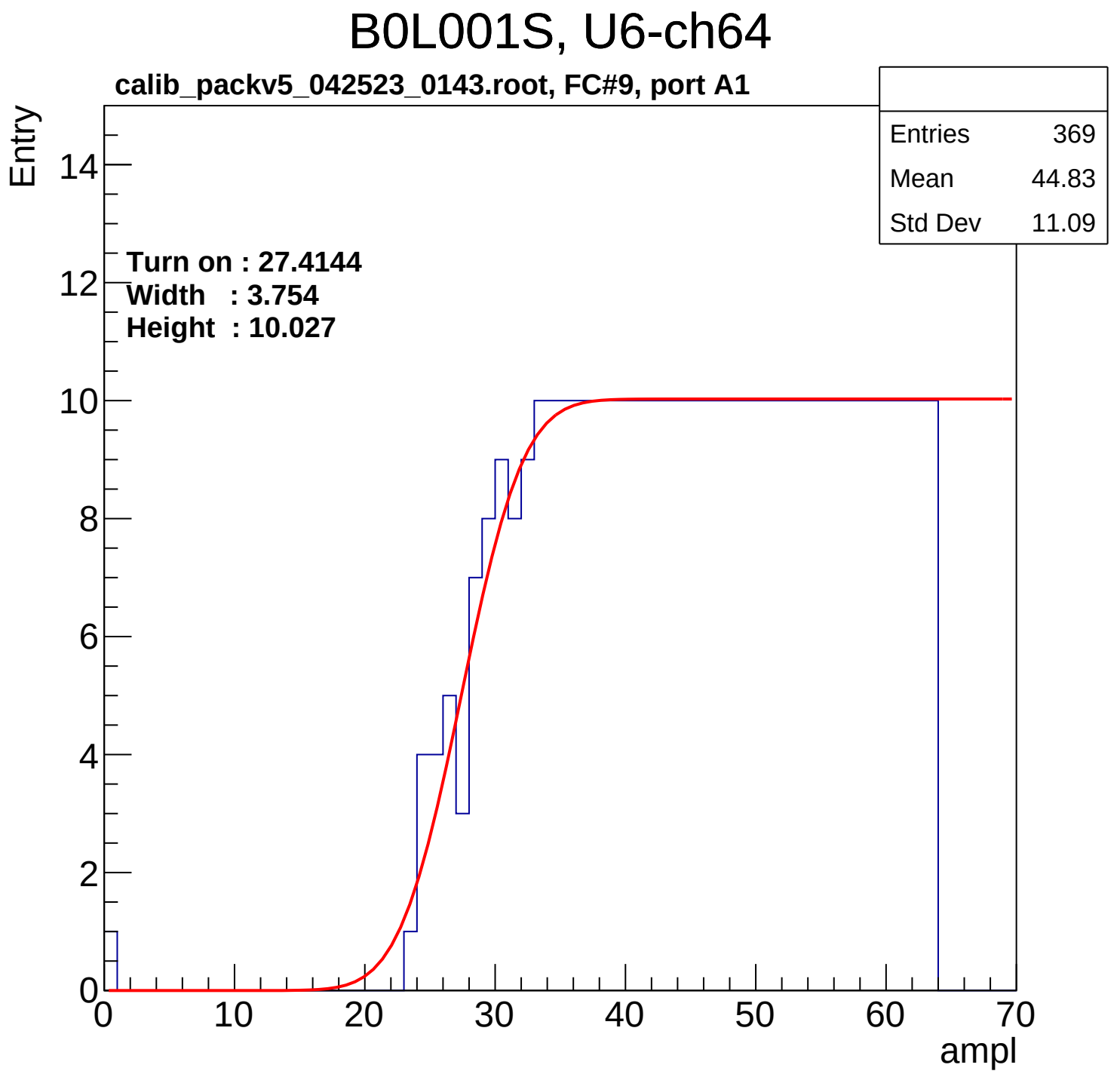
B0L001S, U6-ch64
calib_packv5_042523_0143.root, FC#9, port A1
Entries 369
Mean 44.83
Std Dev 11.09
Turn on : 27.4144
Width : 3.754
Height : 10.027
Entry
ampl
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4
6
8
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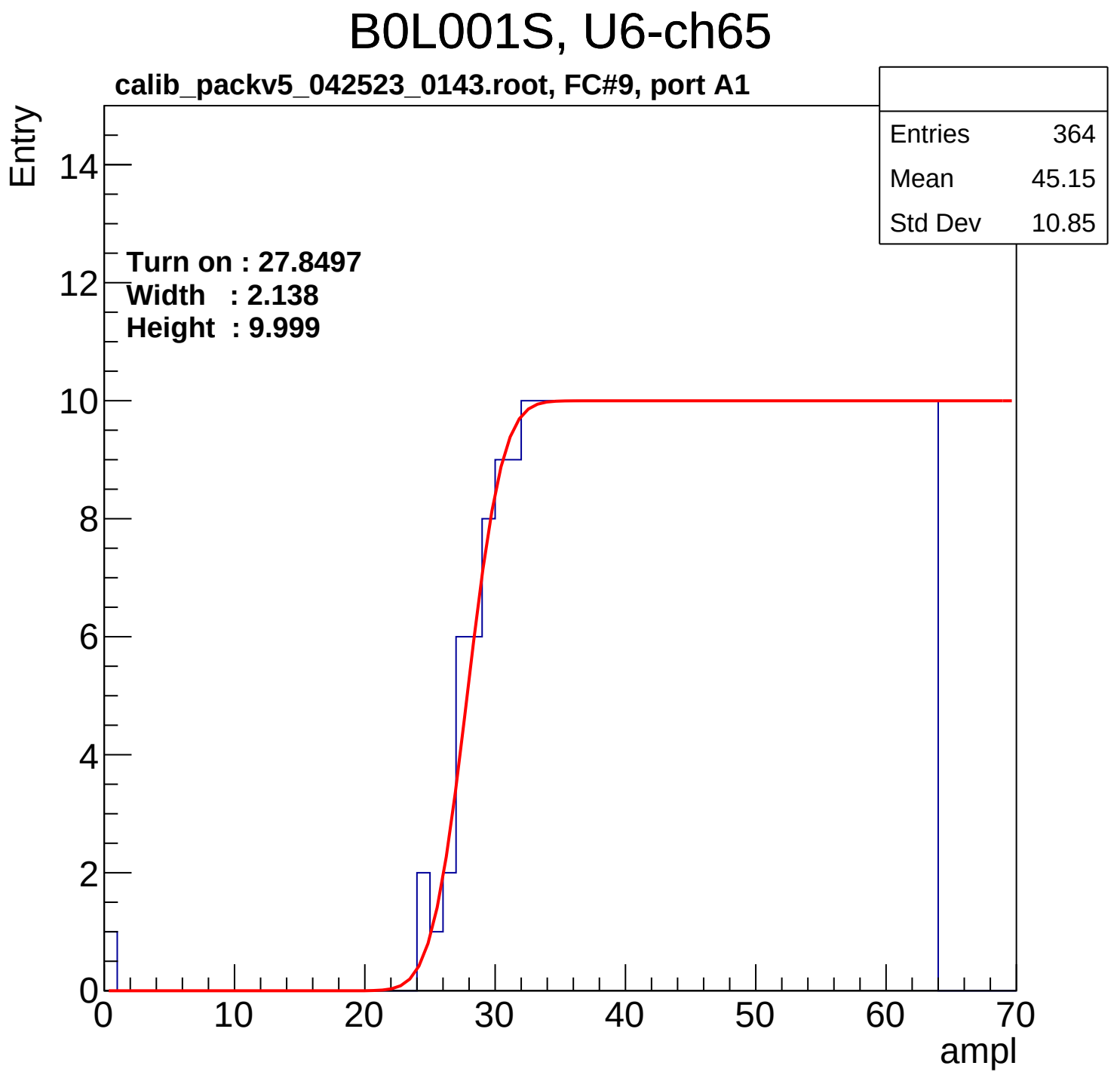
B0L001S, U6-ch65
calib_packv5_042523_0143.root, FC#9, port A1
Entries 364
Mean 45.15
Std Dev 10.85
Turn on : 27.8497
Width : 2.138
Height : 9.999
Entry
ampl
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2
4
6
8
10
12
14
0
10
20
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40
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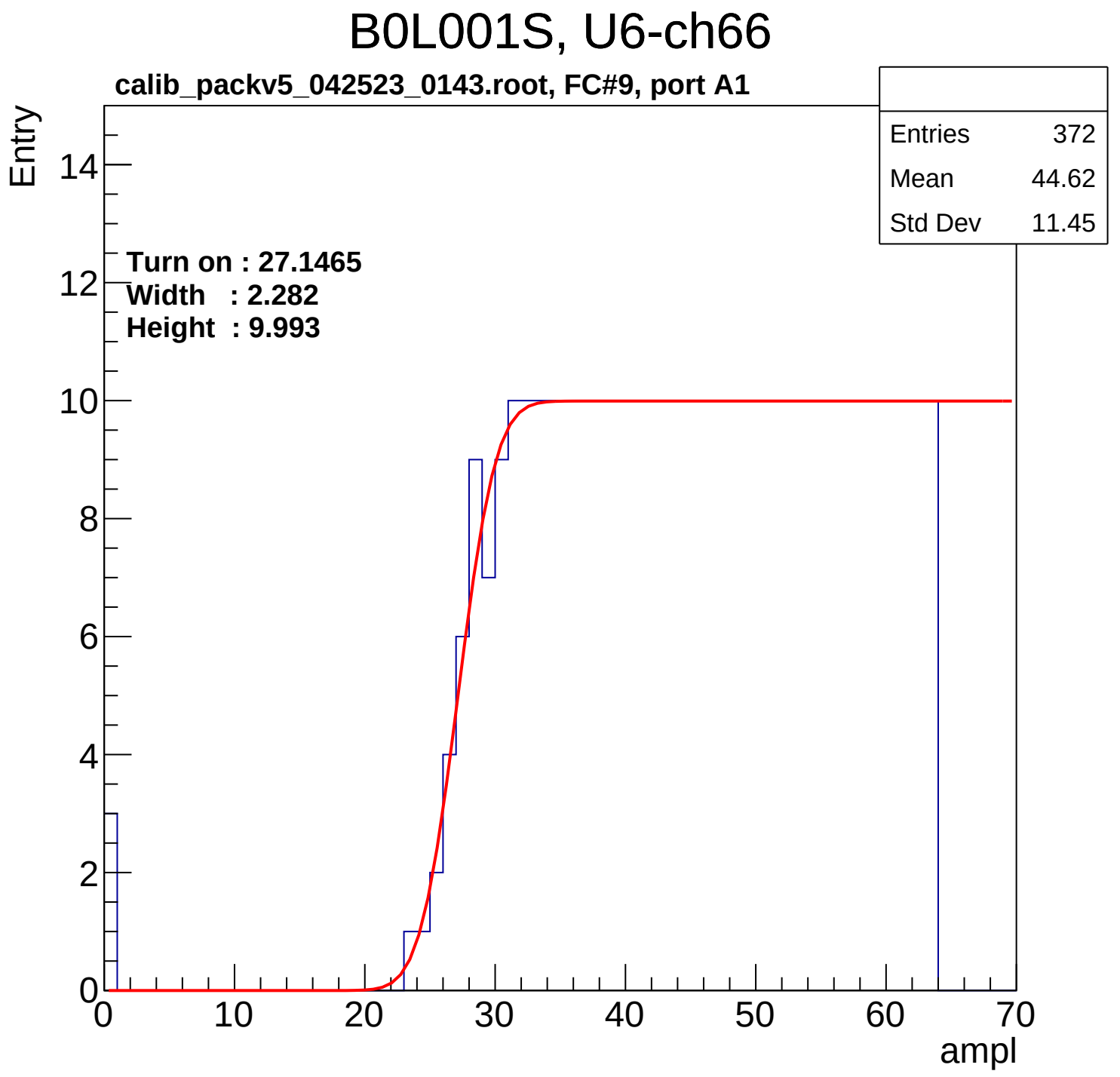
60
70


B0L001S, U6-ch66
calib_packv5_042523_0143.root, FC#9, port A1
Entries 372
Mean 44.62
Std Dev 11.45
Turn on : 27.1465
Width : 2.282
Height : 9.993
Entry
ampl
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2
4
6
8
10
12
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0
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60
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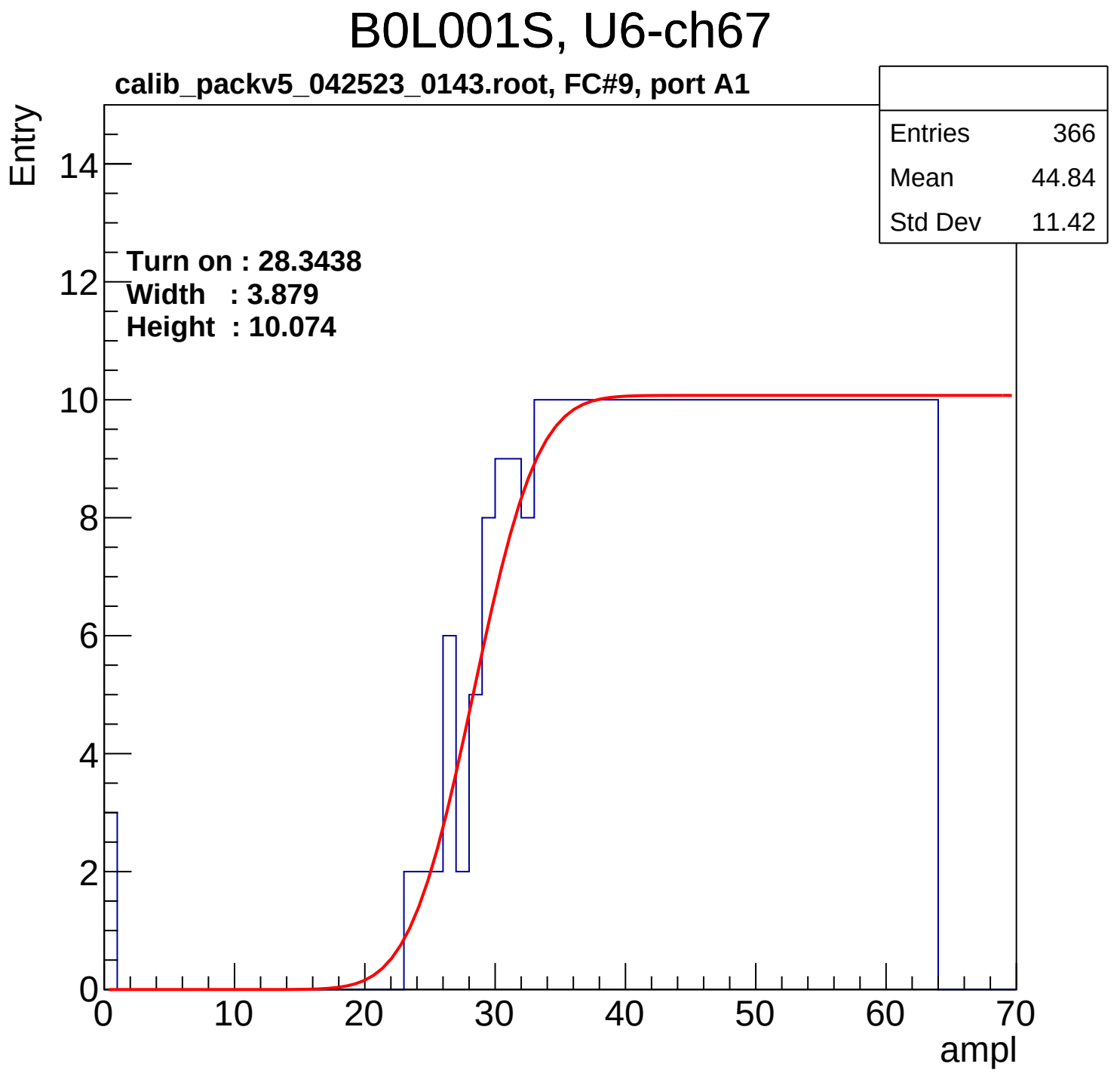
B0L001S, U6-ch67
calib_packv5_042523_0143.root, FC#9, port A1
Entries 366
Mean 44.84
Std Dev 11.42
Turn on : 28.3438
Width : 3.879
Height : 10.074
Entry
ampl
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2
4
6
8
10
12
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60
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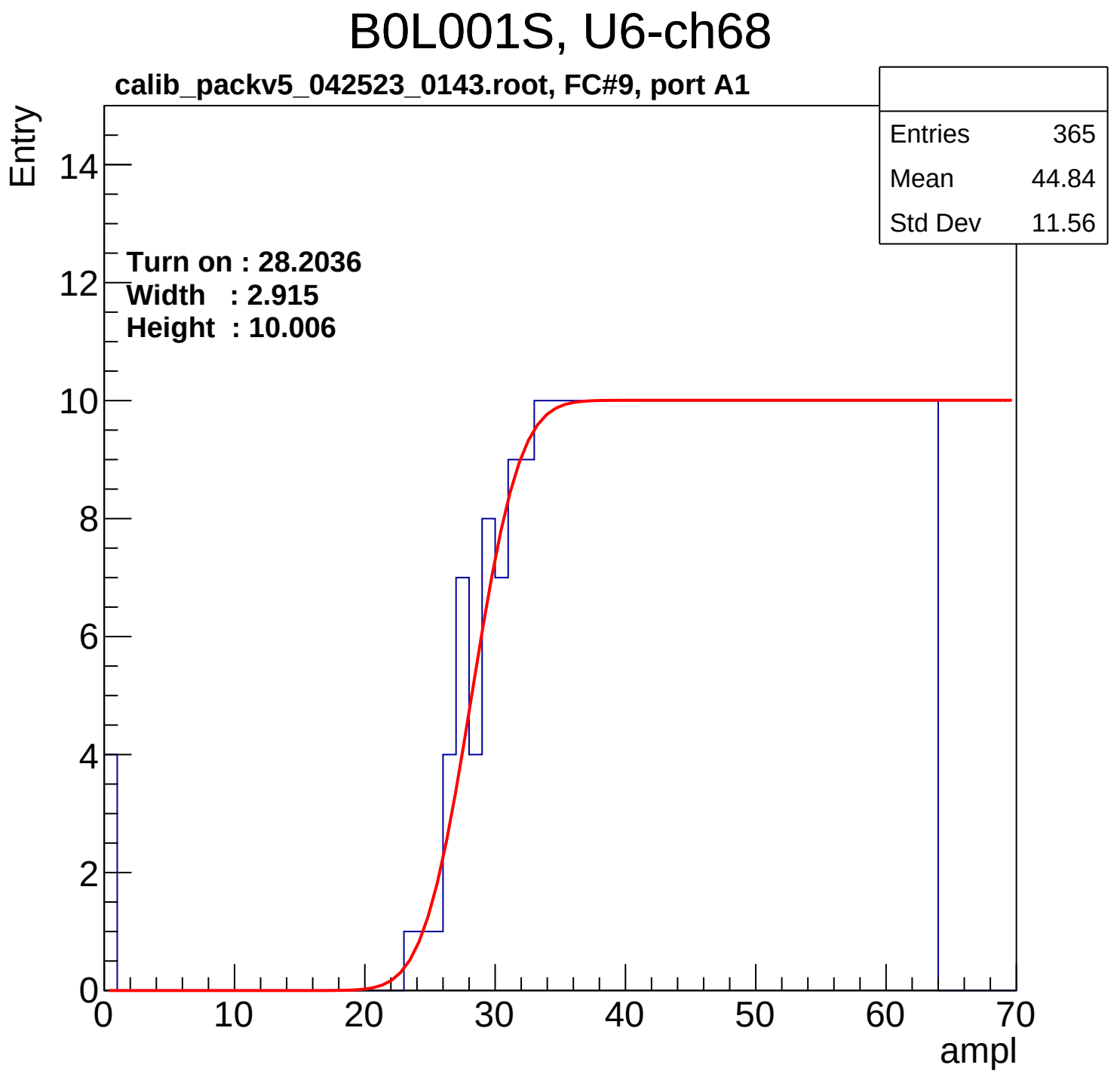
B0L001S, U6-ch68
calib_packv5_042523_0143.root, FC#9, port A1
Entries 365
Mean 44.84
Std Dev 11.56
Turn on : 28.2036
Width : 2.915
Height : 10.006
Entry
ampl
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2
4
6
8
10
12
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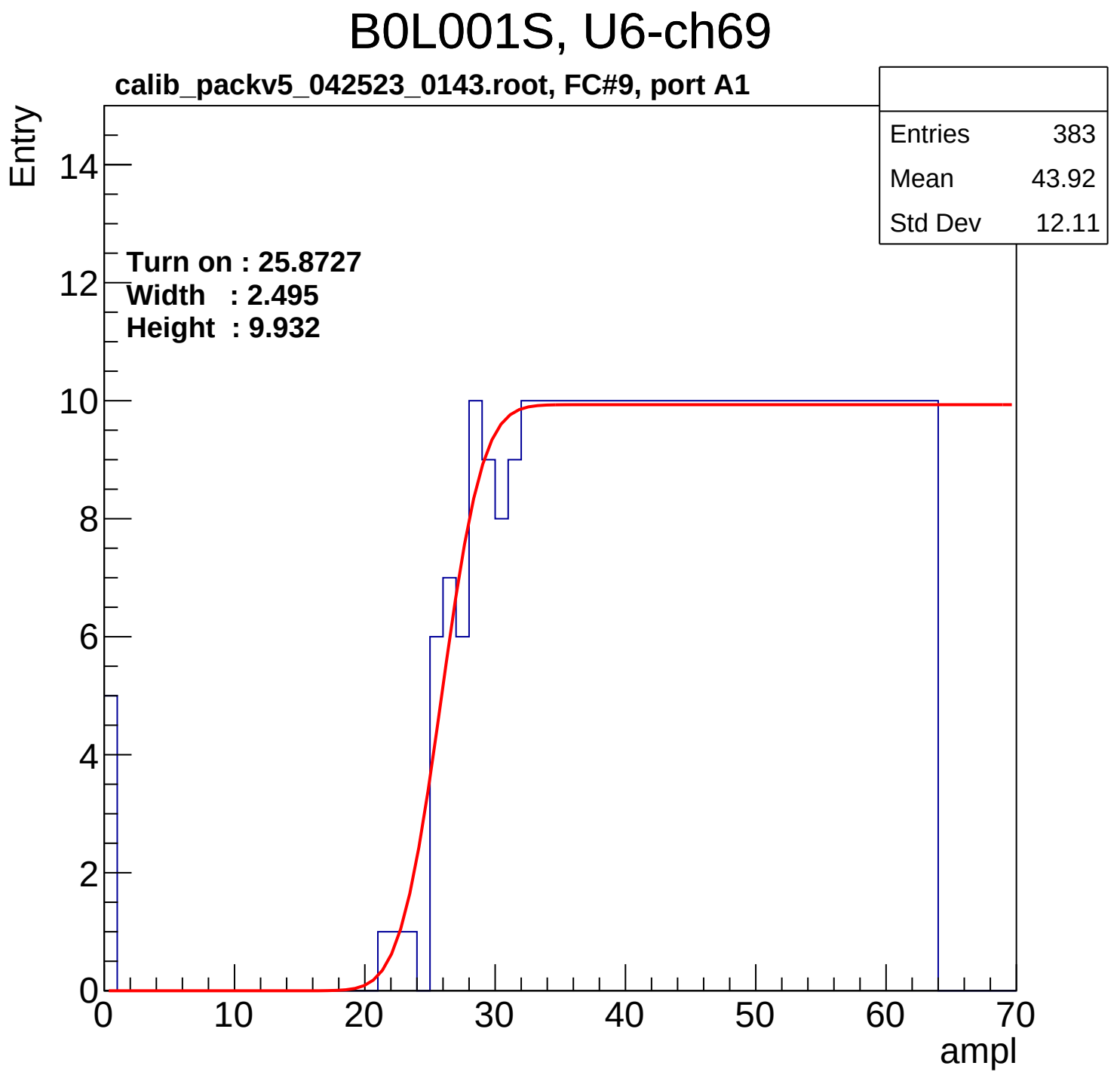
B0L001S, U6-ch69
calib_packv5_042523_0143.root, FC#9, port A1
Entries 383
Mean 43.92
Std Dev 12.11
Turn on : 25.8727
Width : 2.495
Height : 9.932
Entry
ampl
0
2
4
6
8
10
12
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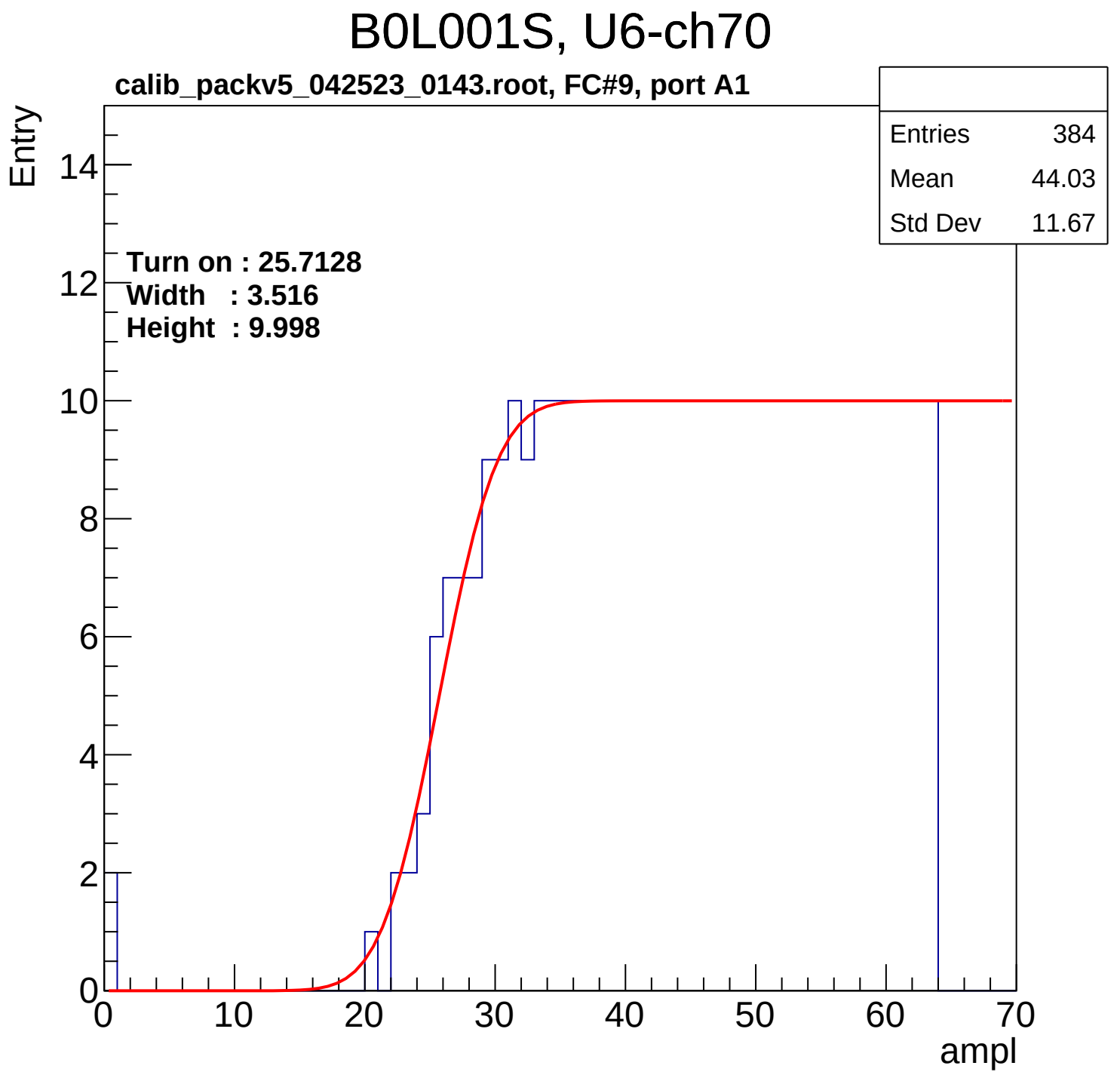
B0L001S, U6-ch70
calib_packv5_042523_0143.root, FC#9, port A1
Entries 384
Mean 44.03
Std Dev 11.67
Turn on : 25.7128
Width : 3.516
Height : 9.998
Entry
ampl
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2
4
6
8
10
12
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0
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20
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60
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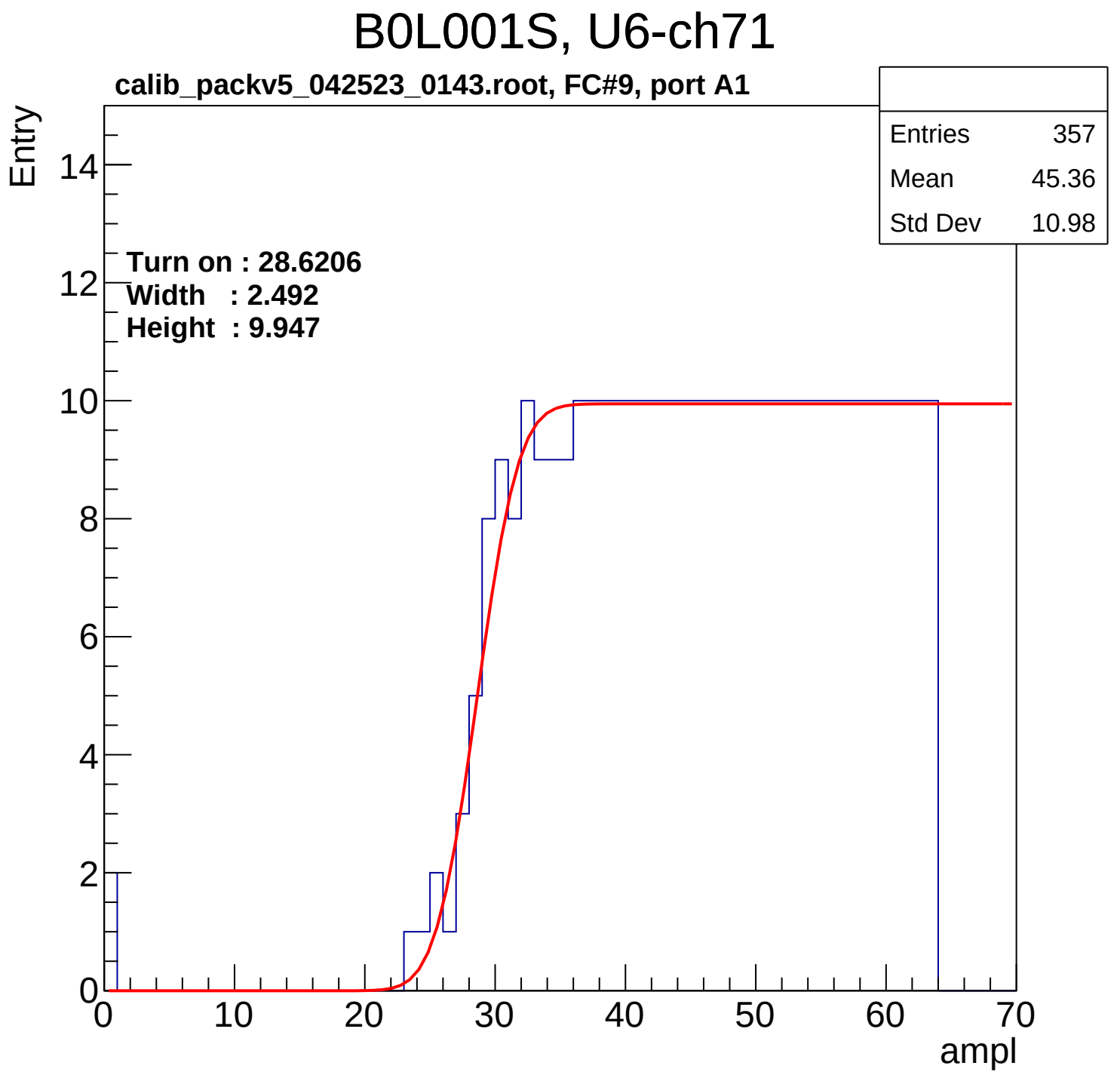
B0L001S, U6-ch71
calib_packv5_042523_0143.root, FC#9, port A1
Entries 357
Mean 45.36
Std Dev 10.98
Turn on : 28.6206
Width : 2.492
Height : 9.947
Entry
ampl
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8
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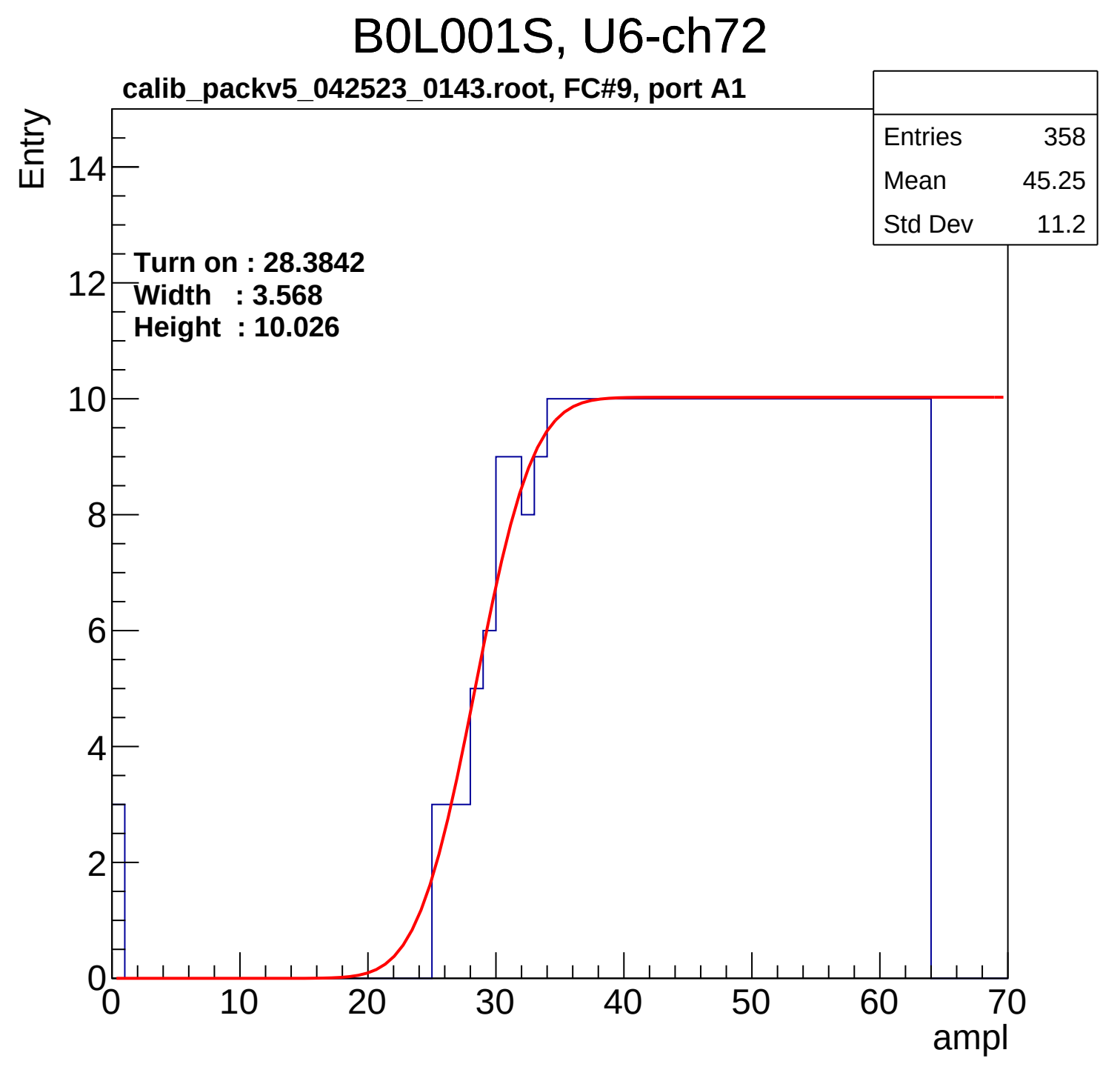
B0L001S, U6-ch72
calib_packv5_042523_0143.root, FC#9, port A1
Entries 358
Mean 45.25
Std Dev 11.2
Turn on : 28.3842
Width : 3.568
Height : 10.026
Entry
ampl
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8
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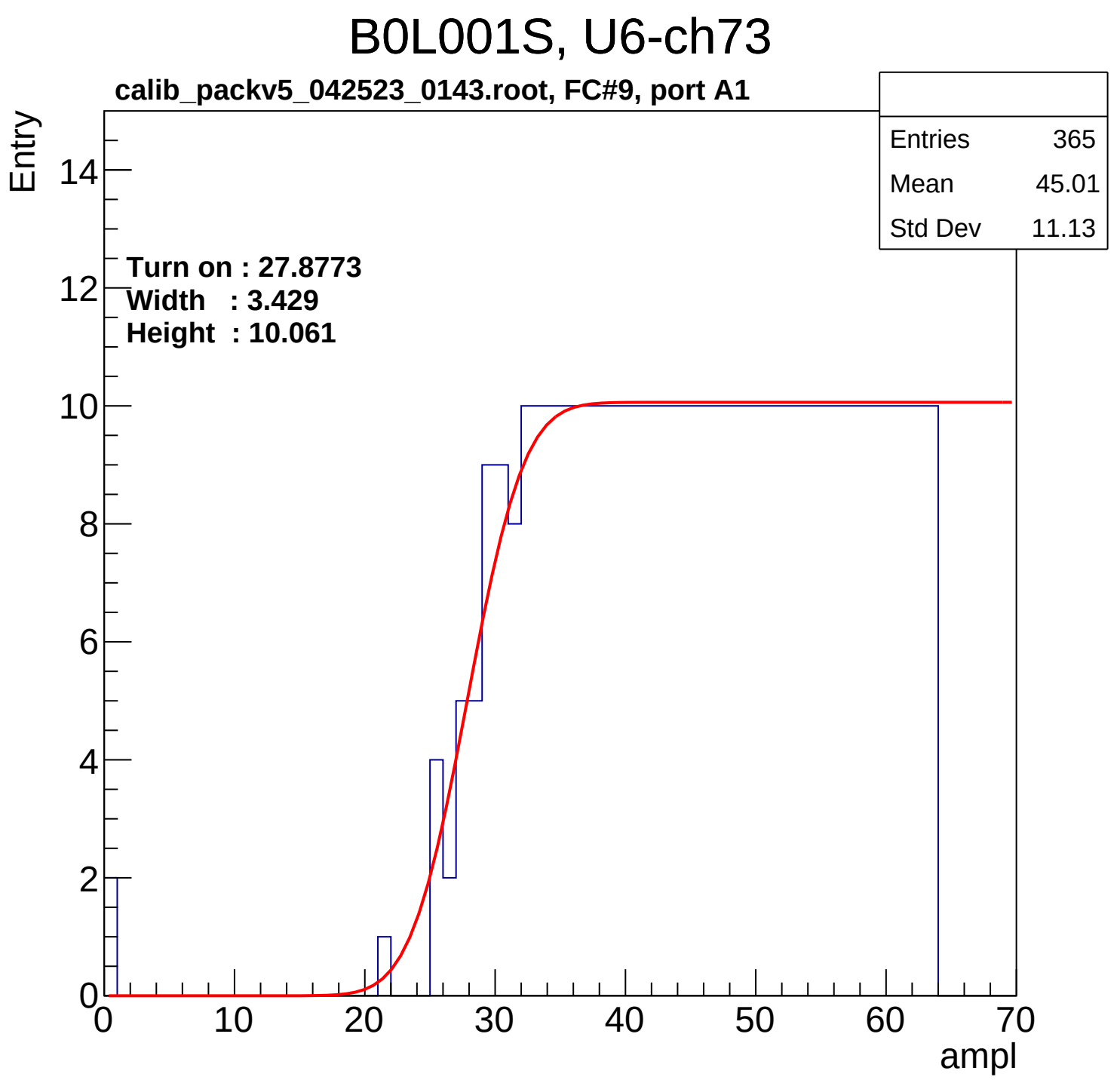
B0L001S, U6-ch73
calib_packv5_042523_0143.root, FC#9, port A1
Entries 365
Mean 45.01
Std Dev 11.13
Turn on : 27.8773
Width : 3.429
Height : 10.061
Entry
ampl
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6
8
10
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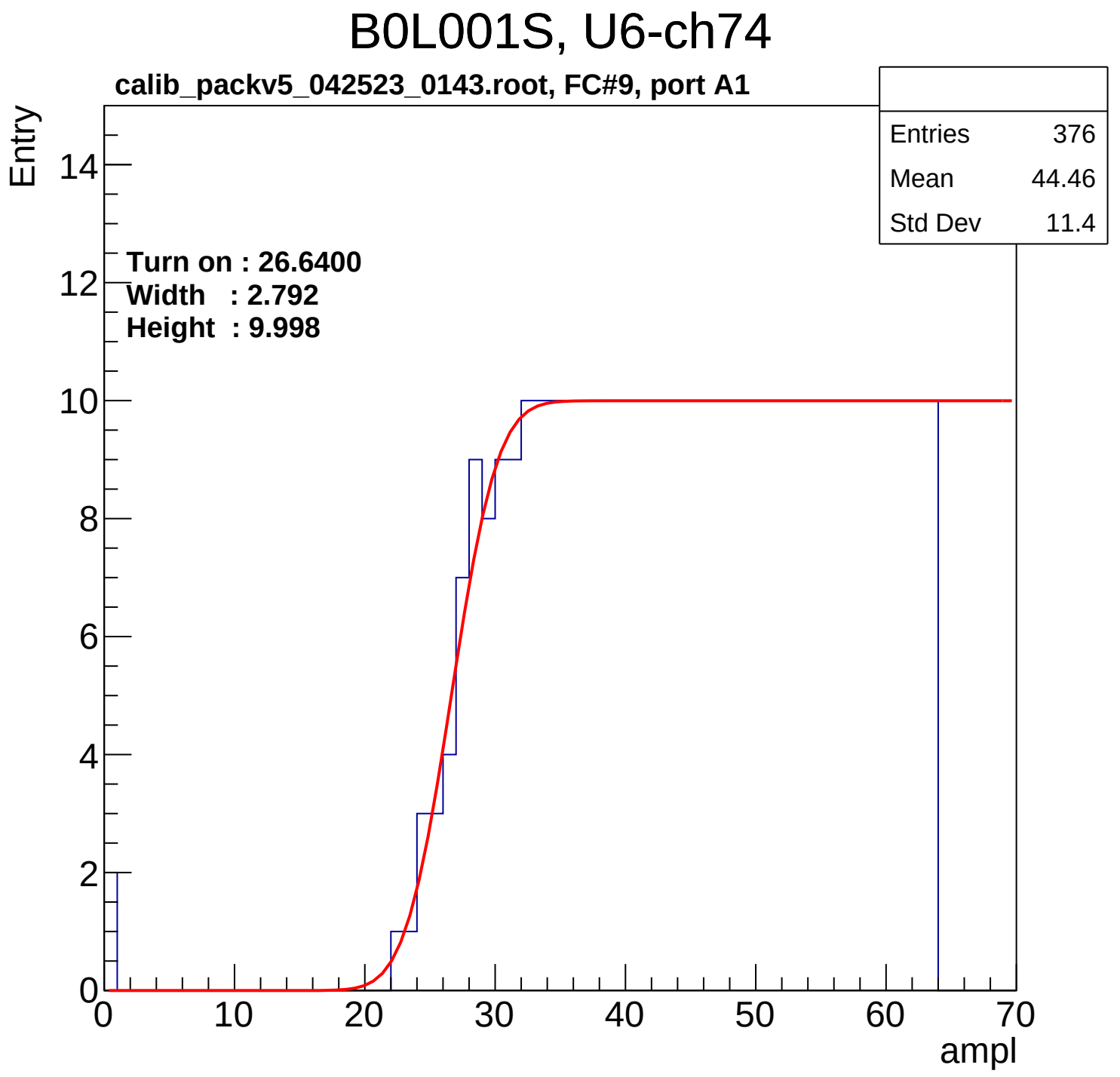
B0L001S, U6-ch74
calib_packv5_042523_0143.root, FC#9, port A1
Entries 376
Mean 44.46
Std Dev 11.4
Turn on : 26.6400
Width : 2.792
Height : 9.998
Entry
ampl
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6
8
10
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0
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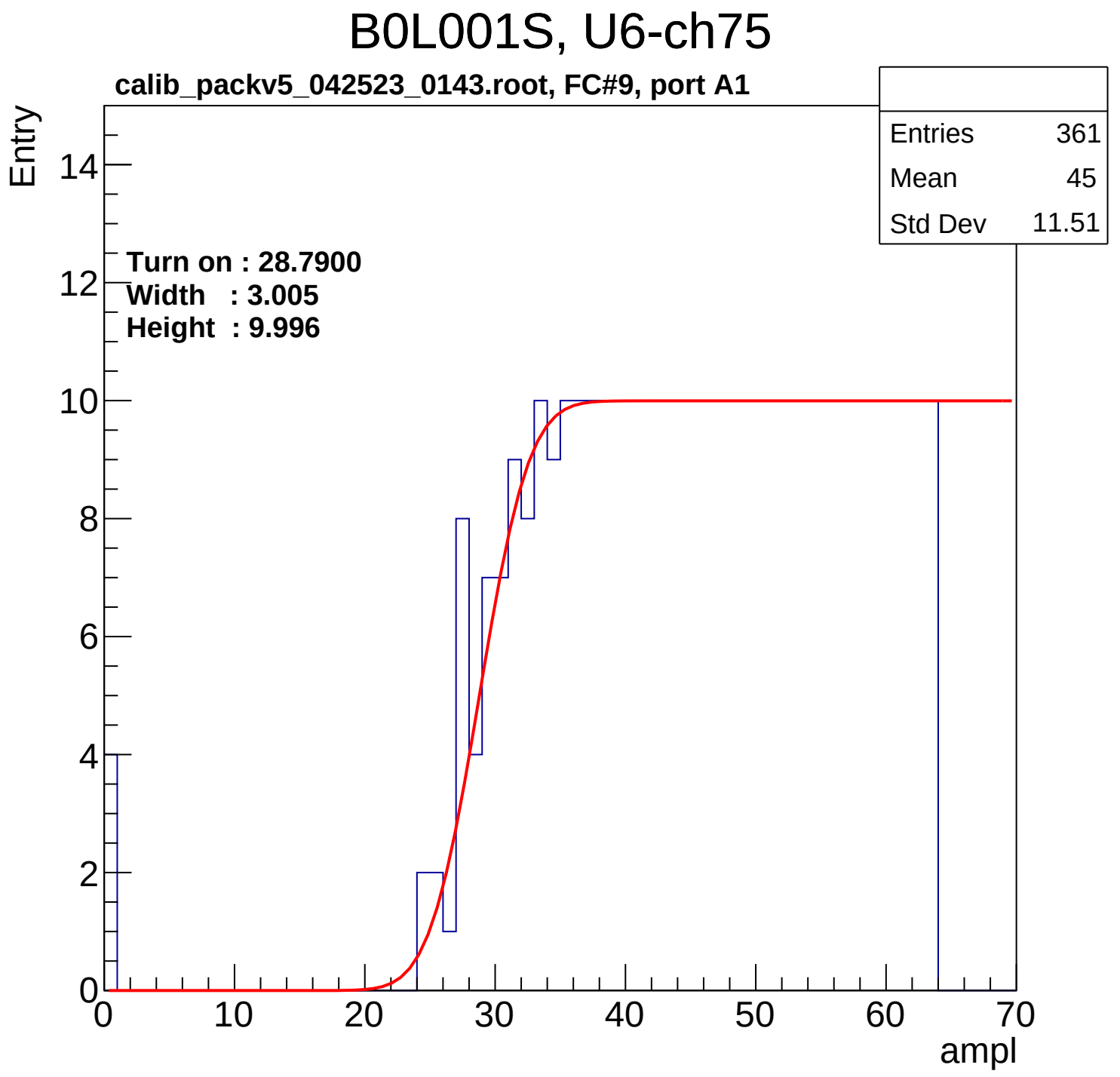
B0L001S, U6-ch75
calib_packv5_042523_0143.root, FC#9, port A1
Entries 361
Mean 45
Std Dev 11.51
Turn on : 28.7900
Width : 3.005
Height : 9.996
Entry
ampl
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10
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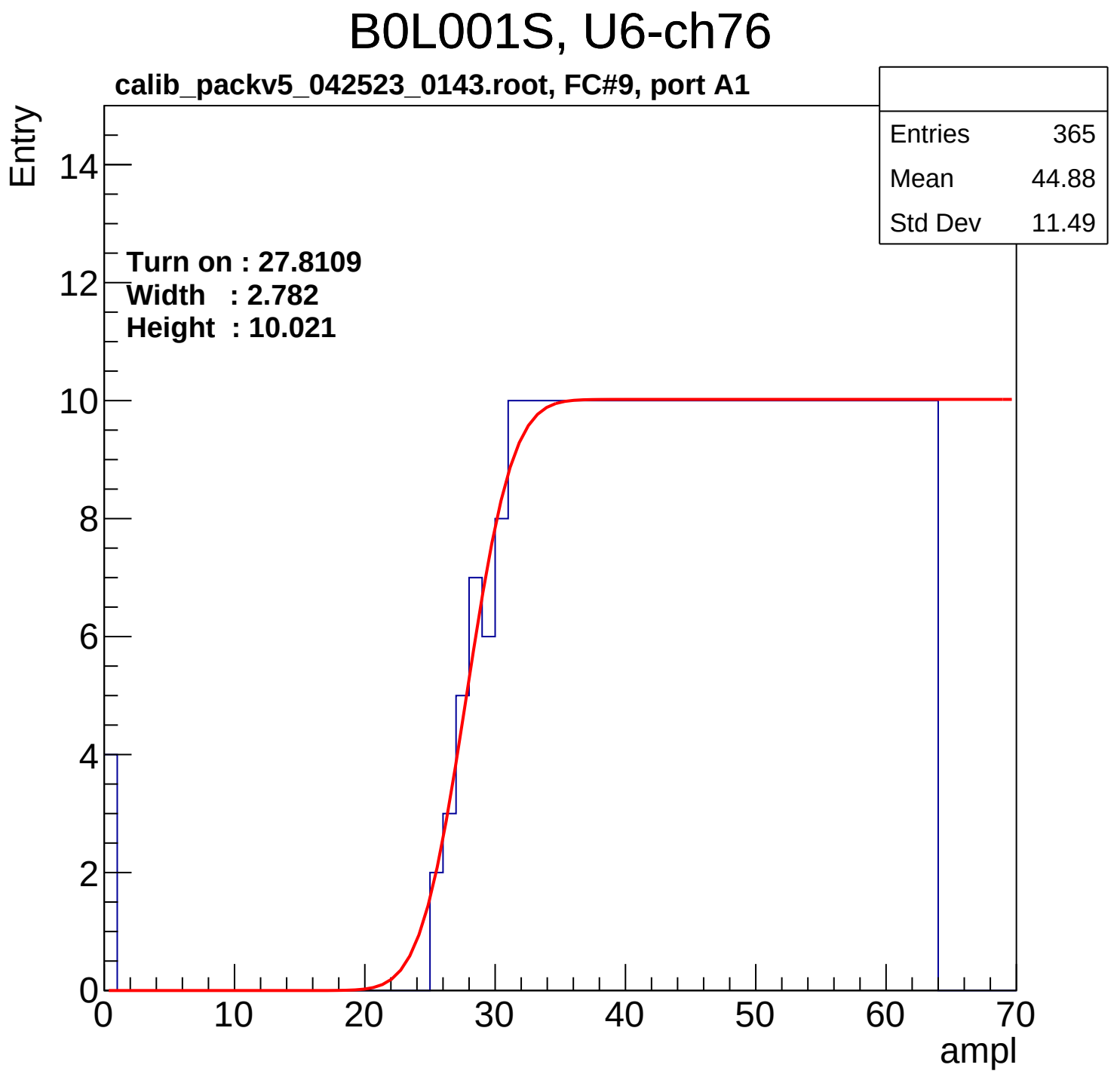
B0L001S, U6-ch76
calib_packv5_042523_0143.root, FC#9, port A1
Entries 365
Mean 44.88
Std Dev 11.49
Turn on : 27.8109
Width : 2.782
Height : 10.021
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ampl
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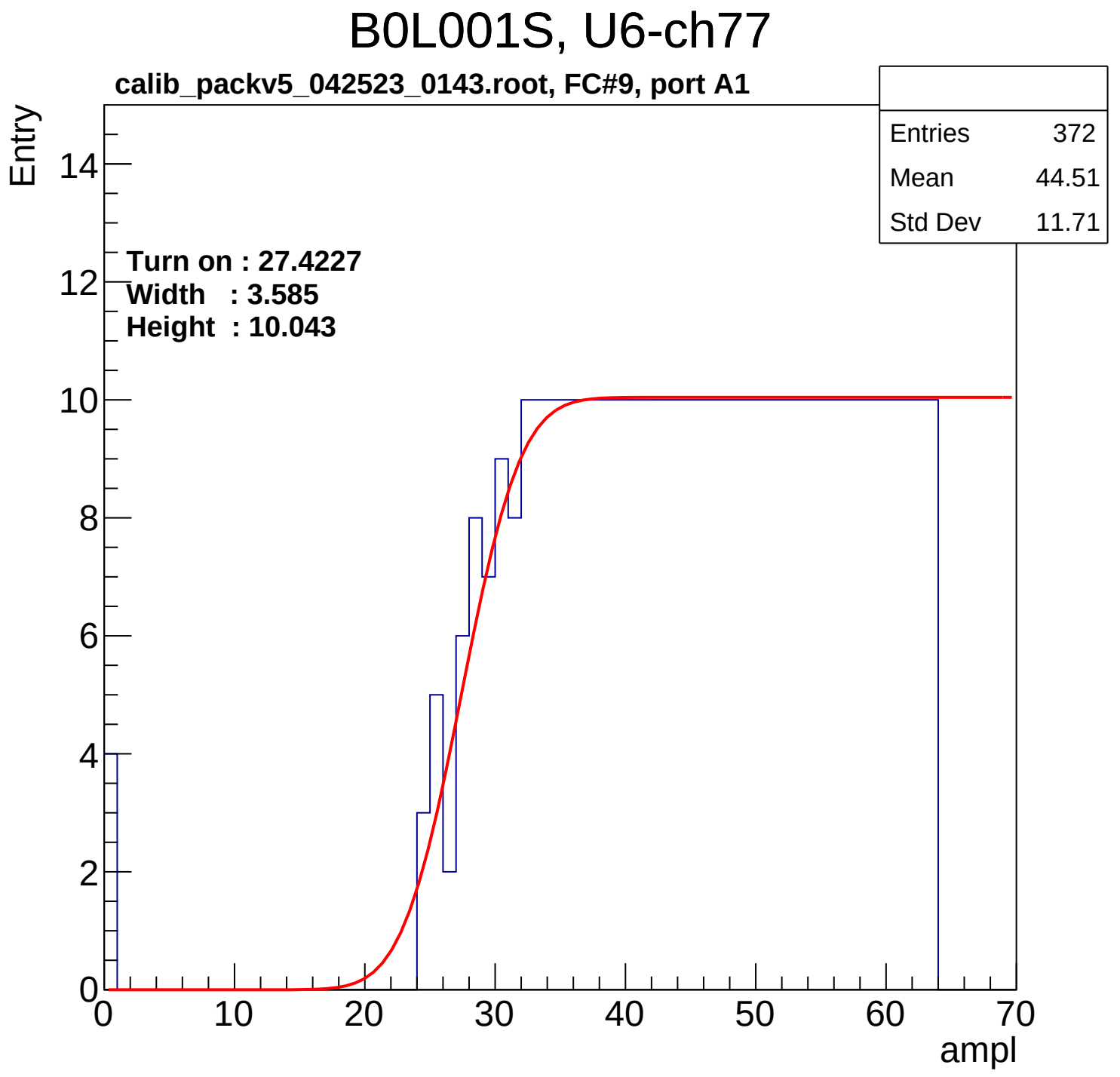
B0L001S, U6-ch77
calib_packv5_042523_0143.root, FC#9, port A1
Entries 372
Mean 44.51
Std Dev 11.71
Turn on : 27.4227
Width : 3.585
Height : 10.043
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ampl
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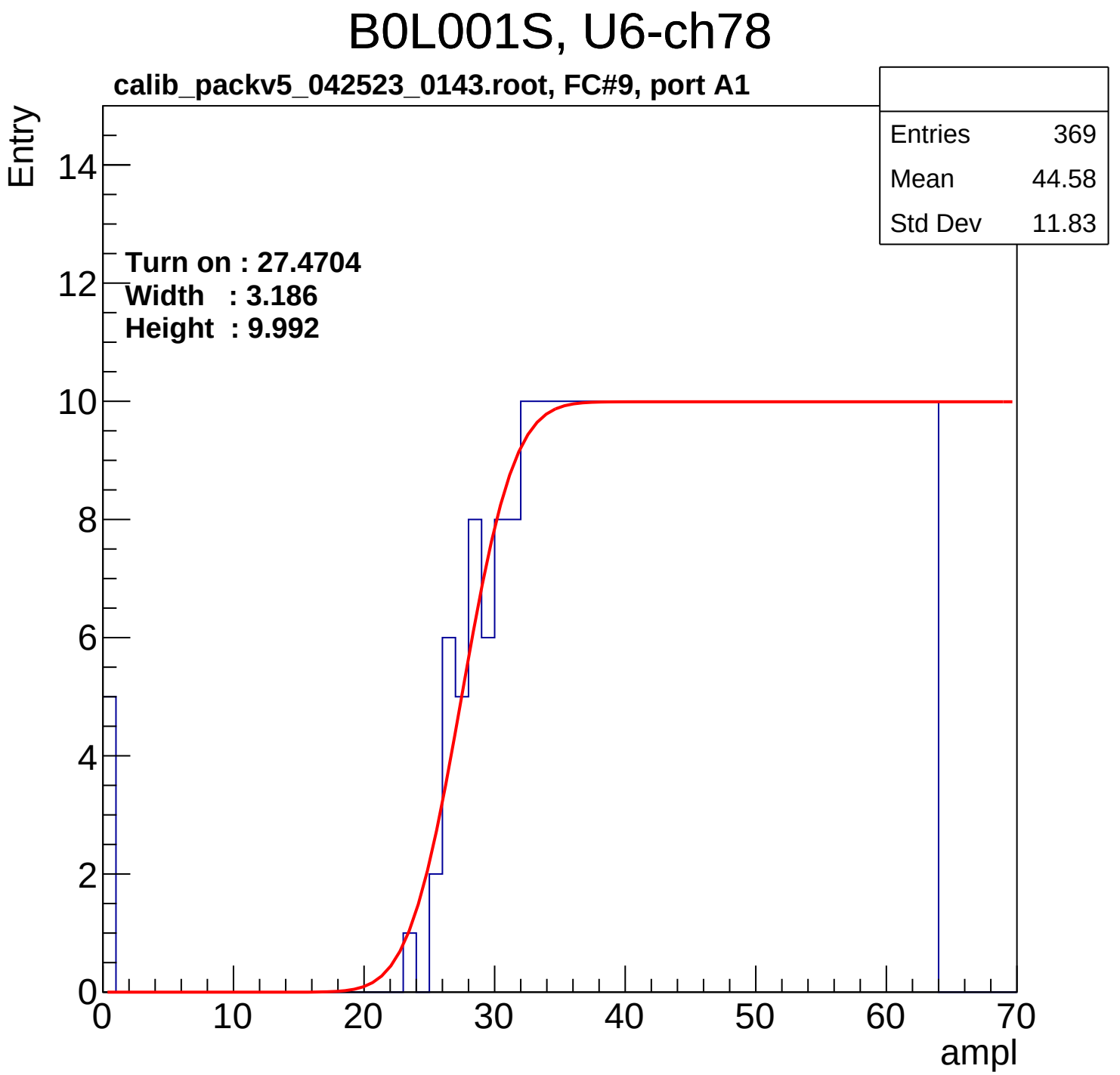
B0L001S, U6-ch78
calib_packv5_042523_0143.root, FC#9, port A1
Entries 369
Mean 44.58
Std Dev 11.83
Turn on : 27.4704
Width : 3.186
Height : 9.992
Entry
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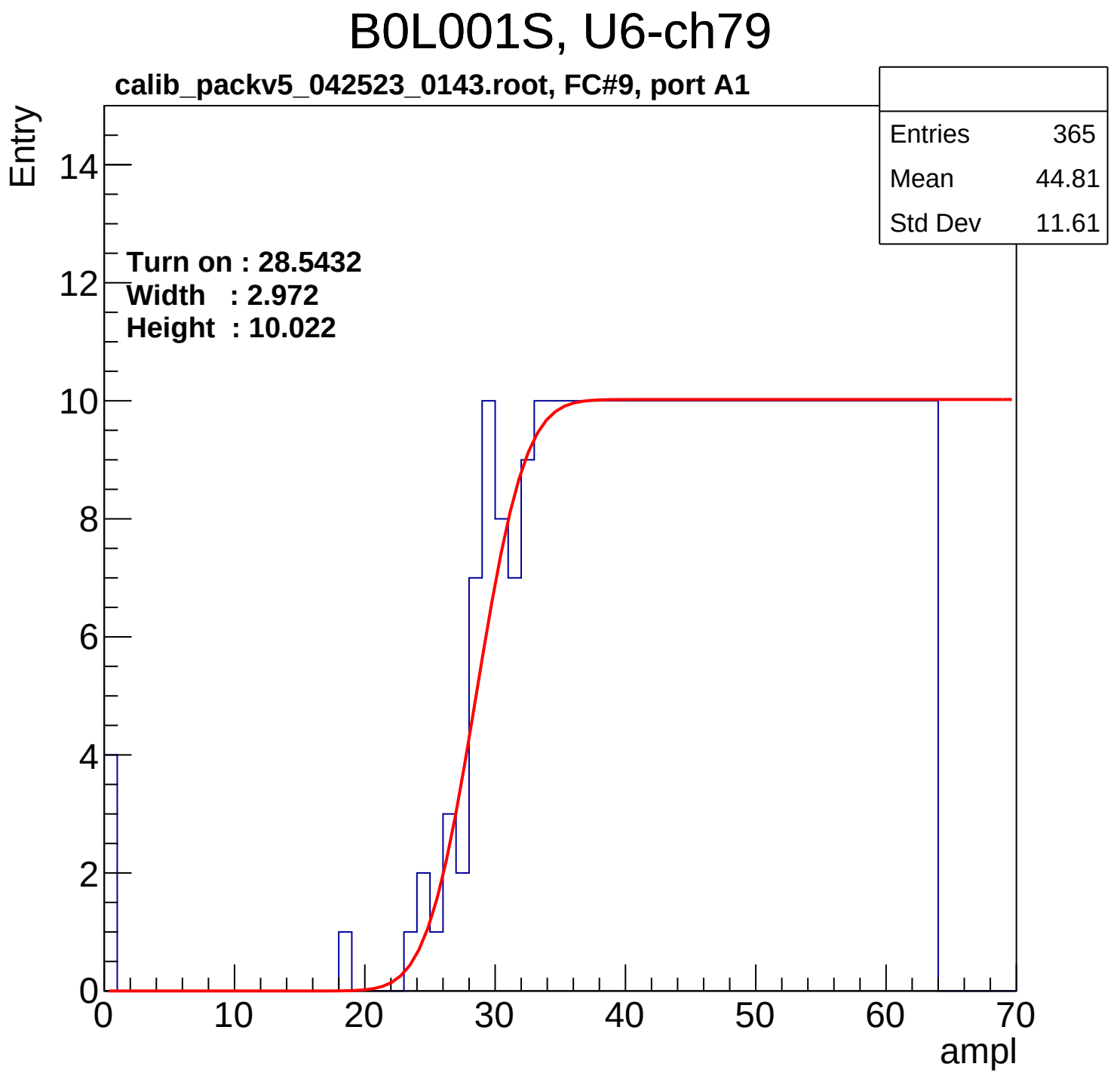
B0L001S, U6-ch79
calib_packv5_042523_0143.root, FC#9, port A1
Entries 365
Mean 44.81
Std Dev 11.61
Turn on : 28.5432
Width : 2.972
Height : 10.022
Entry
ampl
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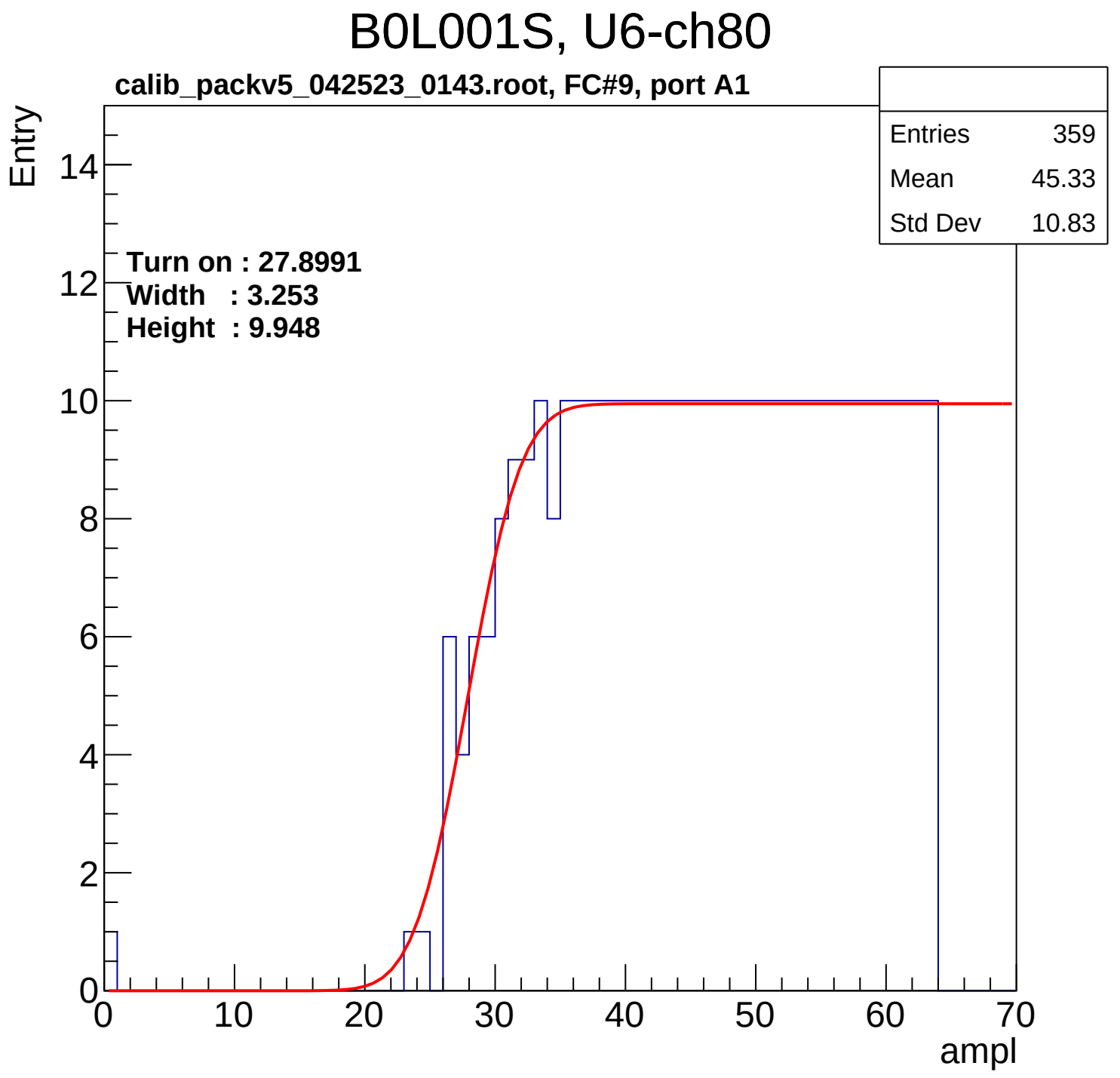
B0L001S, U6-ch80
calib_packv5_042523_0143.root, FC#9, port A1
Entries 359
Mean 45.33
Std Dev 10.83
Turn on : 27.8991
Width : 3.253
Height : 9.948
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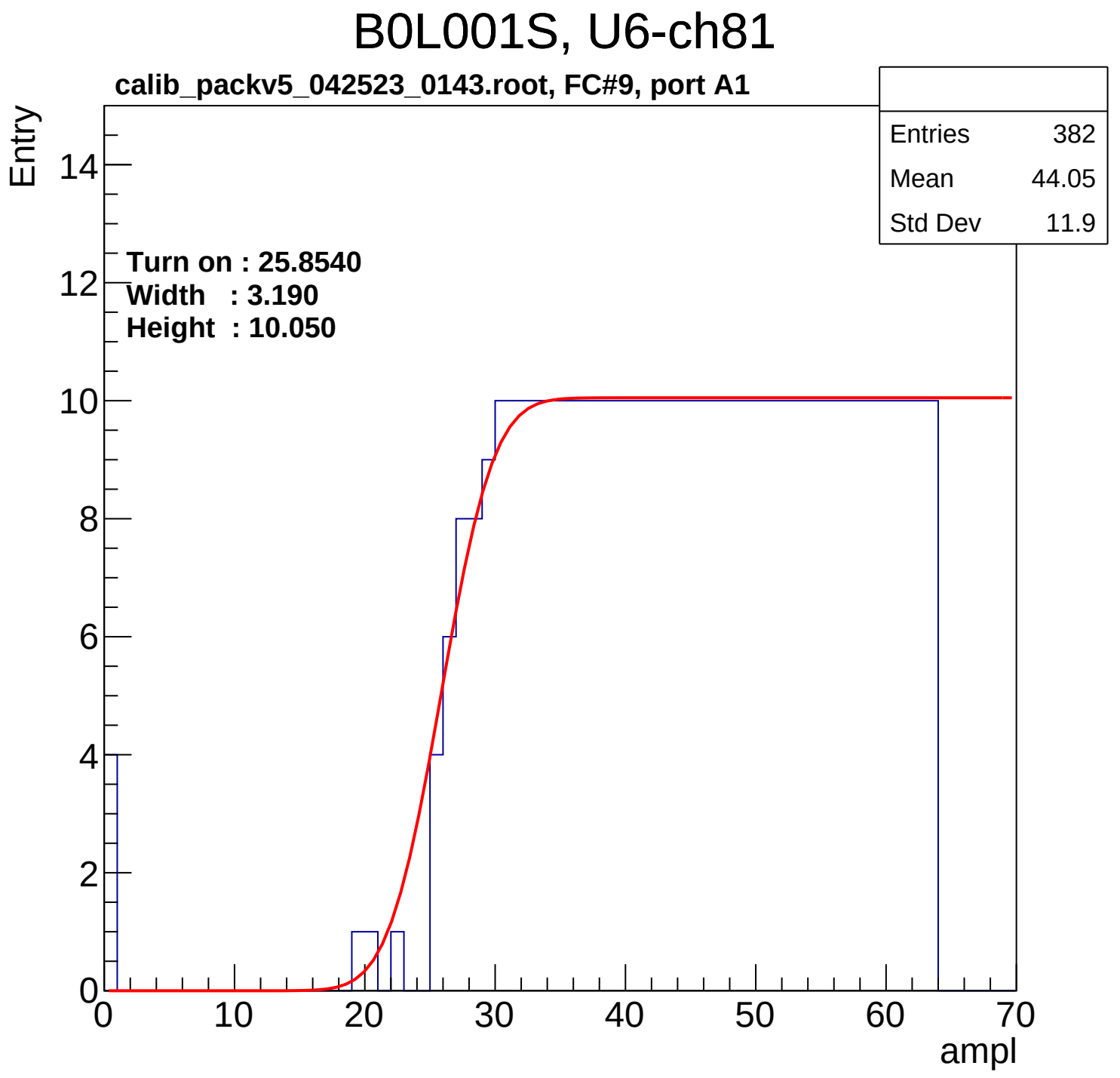
B0L001S, U6-ch81
calib_packv5_042523_0143.root, FC#9, port A1
Entries 382
Mean 44.05
Std Dev 11.9
Turn on : 25.8540
Width : 3.190
Height : 10.050
Entry
ampl
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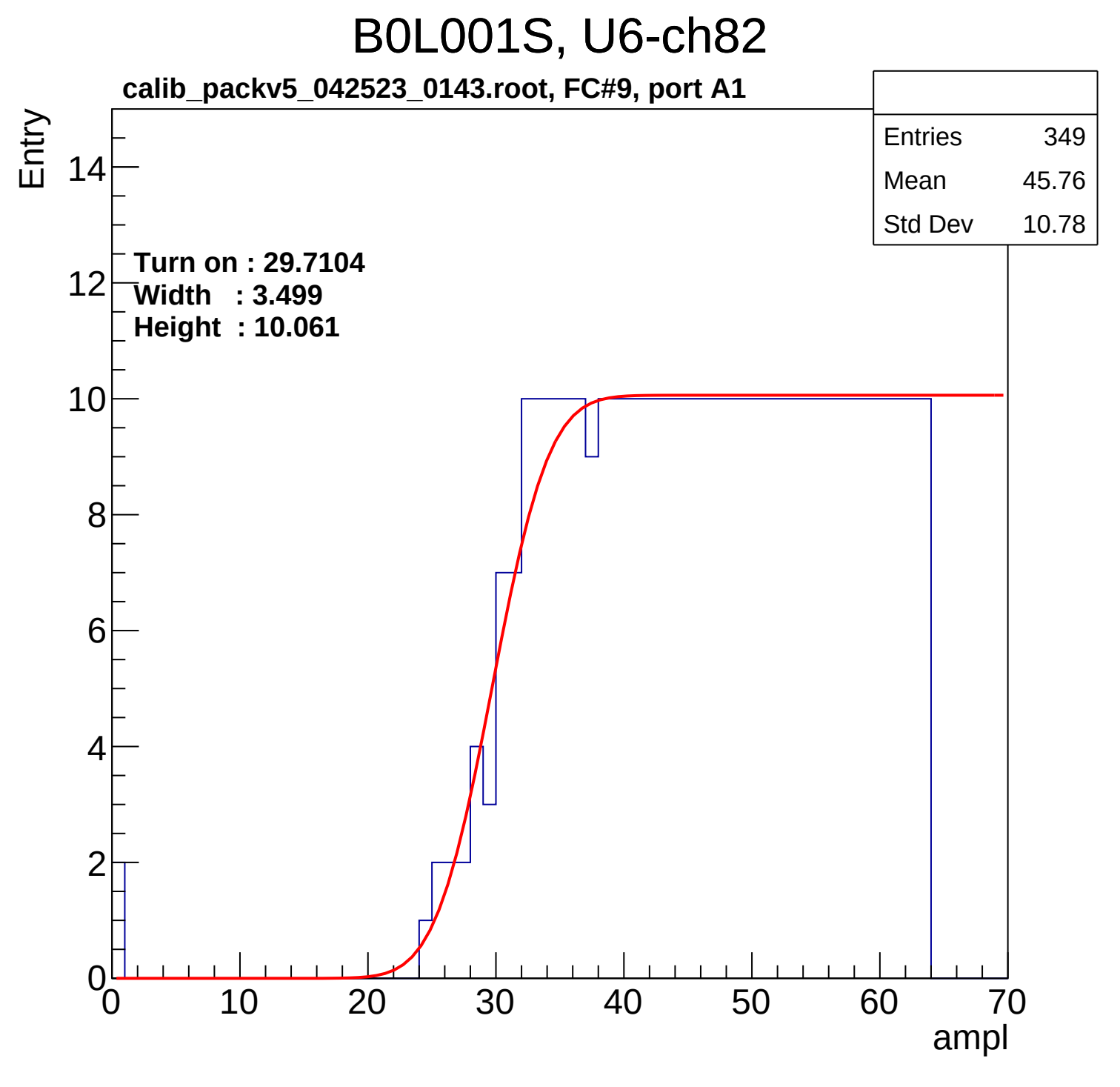
B0L001S, U6-ch82
calib_packv5_042523_0143.root, FC#9, port A1
Entries 349
Mean 45.76
Std Dev 10.78
Turn on : 29.7104
Width : 3.499
Height : 10.061
Entry
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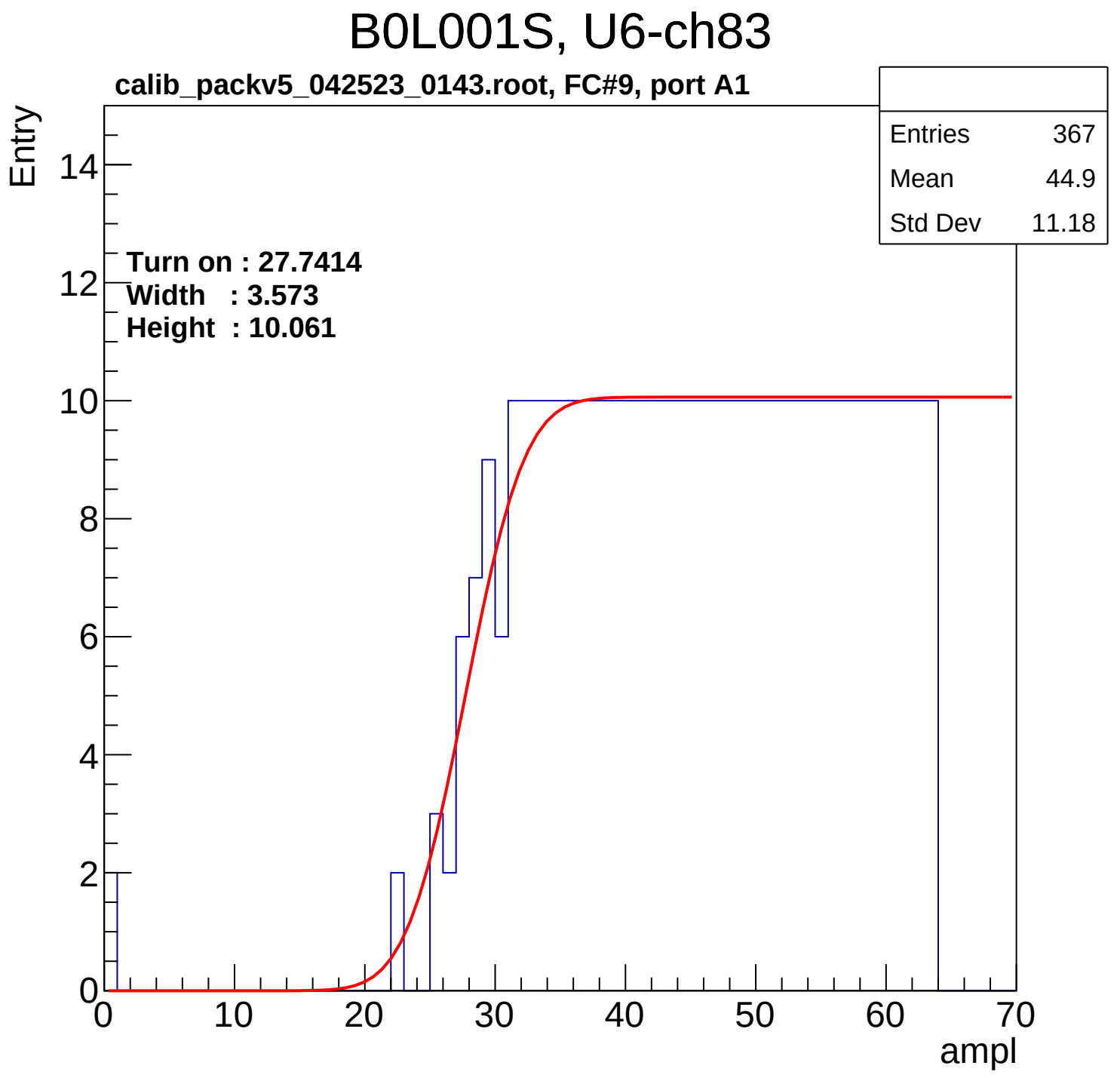
B0L001S, U6-ch83
calib_packv5_042523_0143.root, FC#9, port A1
Entries 367
Mean 44.9
Std Dev 11.18
Turn on : 27.7414
Width : 3.573
Height : 10.061
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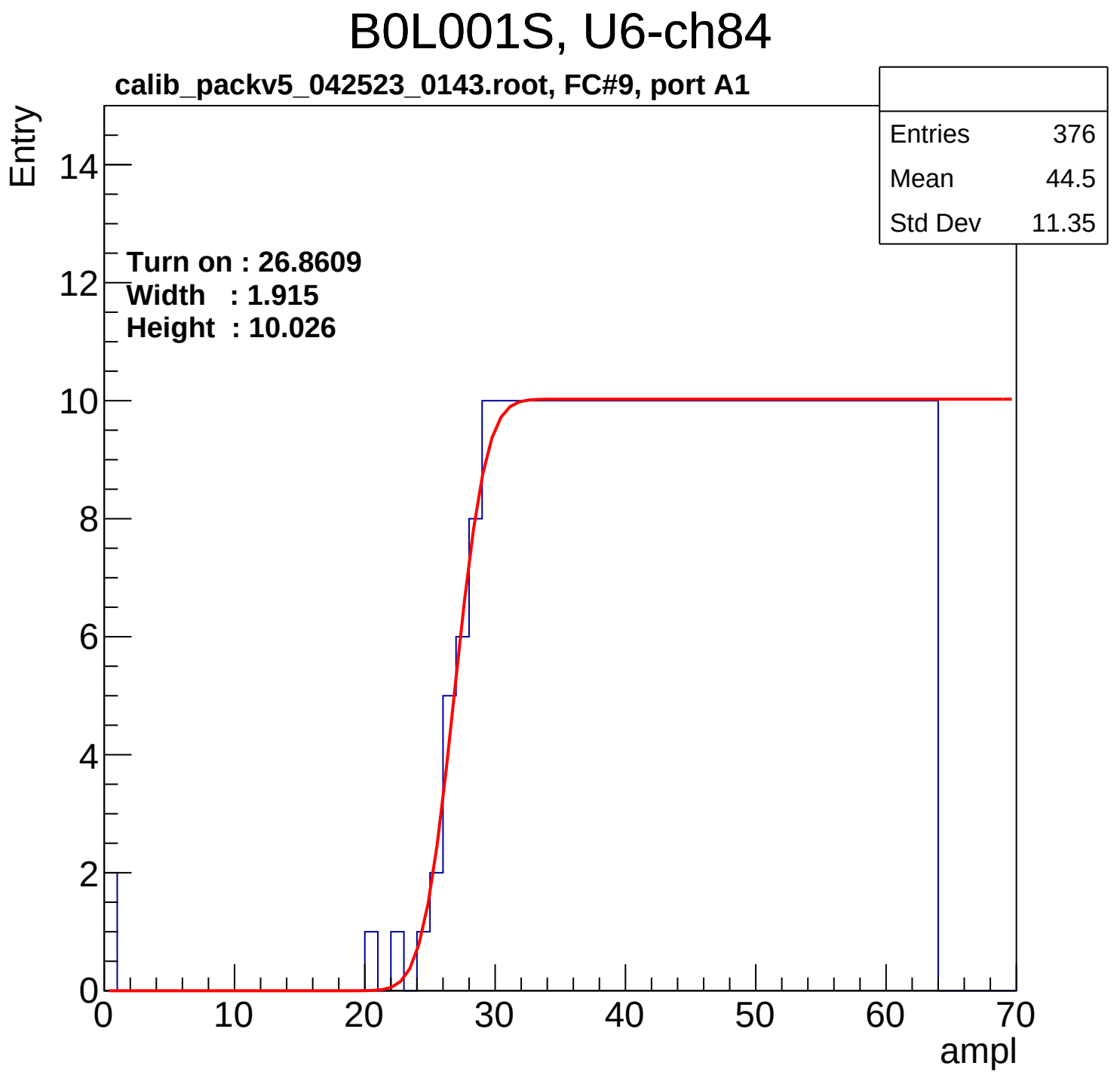
B0L001S, U6-ch84
calib_packv5_042523_0143.root, FC#9, port A1
Entries 376
Mean 44.5
Std Dev 11.35
Turn on : 26.8609
Width : 1.915
Height : 10.026
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ampl
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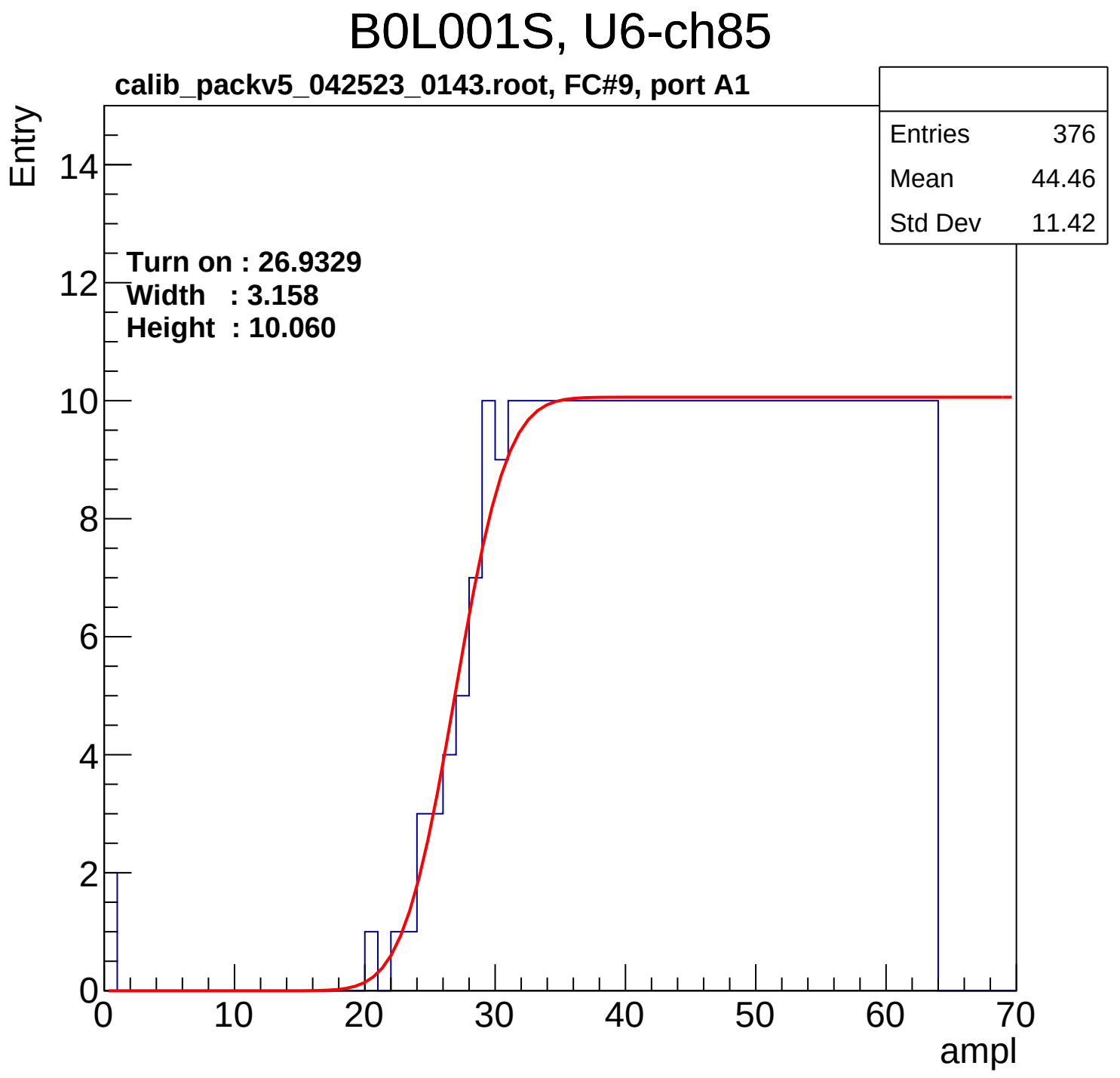
B0L001S, U6-ch85
calib_packv5_042523_0143.root, FC#9, port A1
Entries 376
Mean 44.46
Std Dev 11.42
Turn on : 26.9329
Width : 3.158
Height : 10.060
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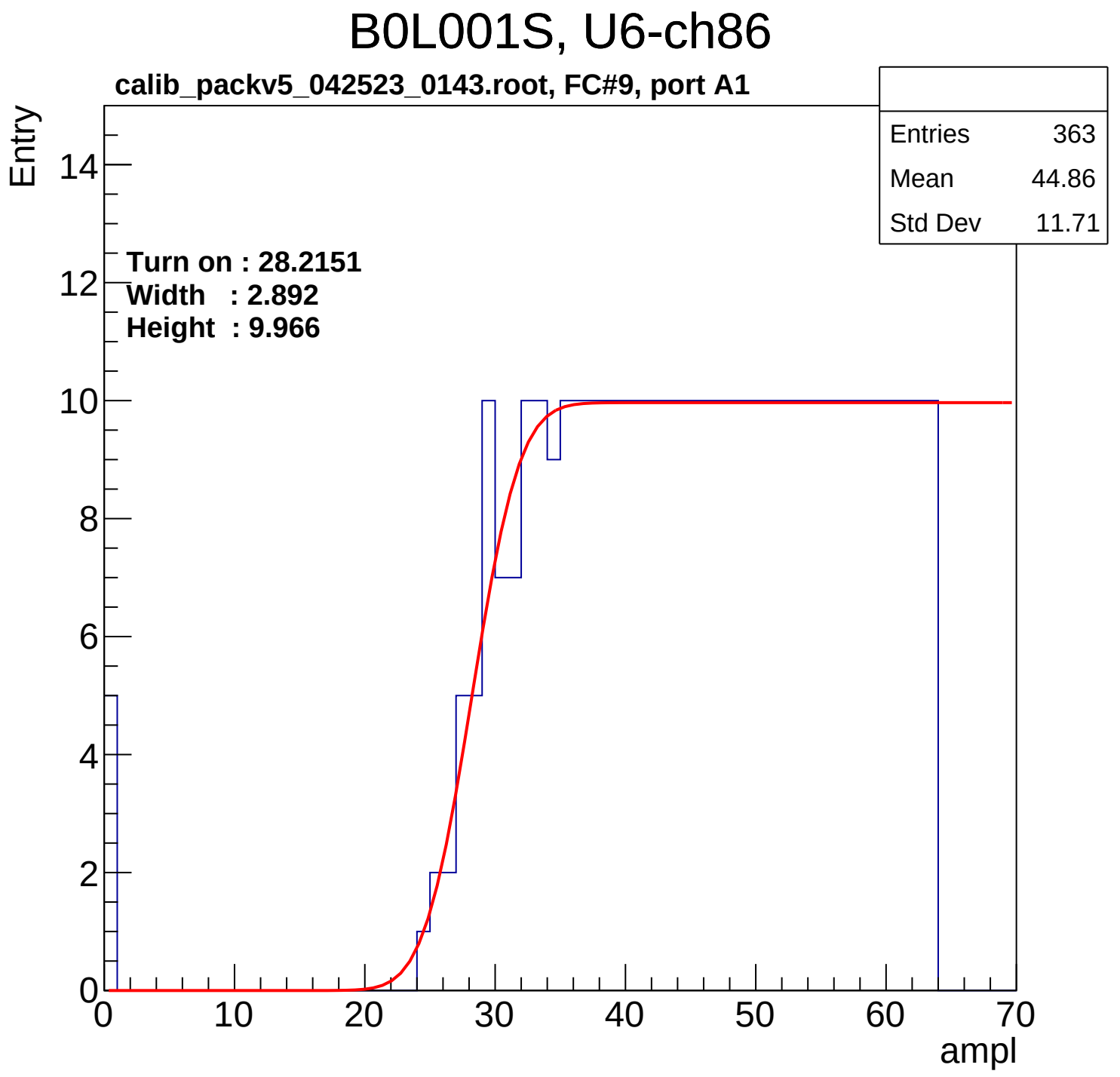
B0L001S, U6-ch86
calib_packv5_042523_0143.root, FC#9, port A1
Entries 363
Mean 44.86
Std Dev 11.71
Turn on : 28.2151
Width : 2.892
Height : 9.966
Entry
ampl
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4
6
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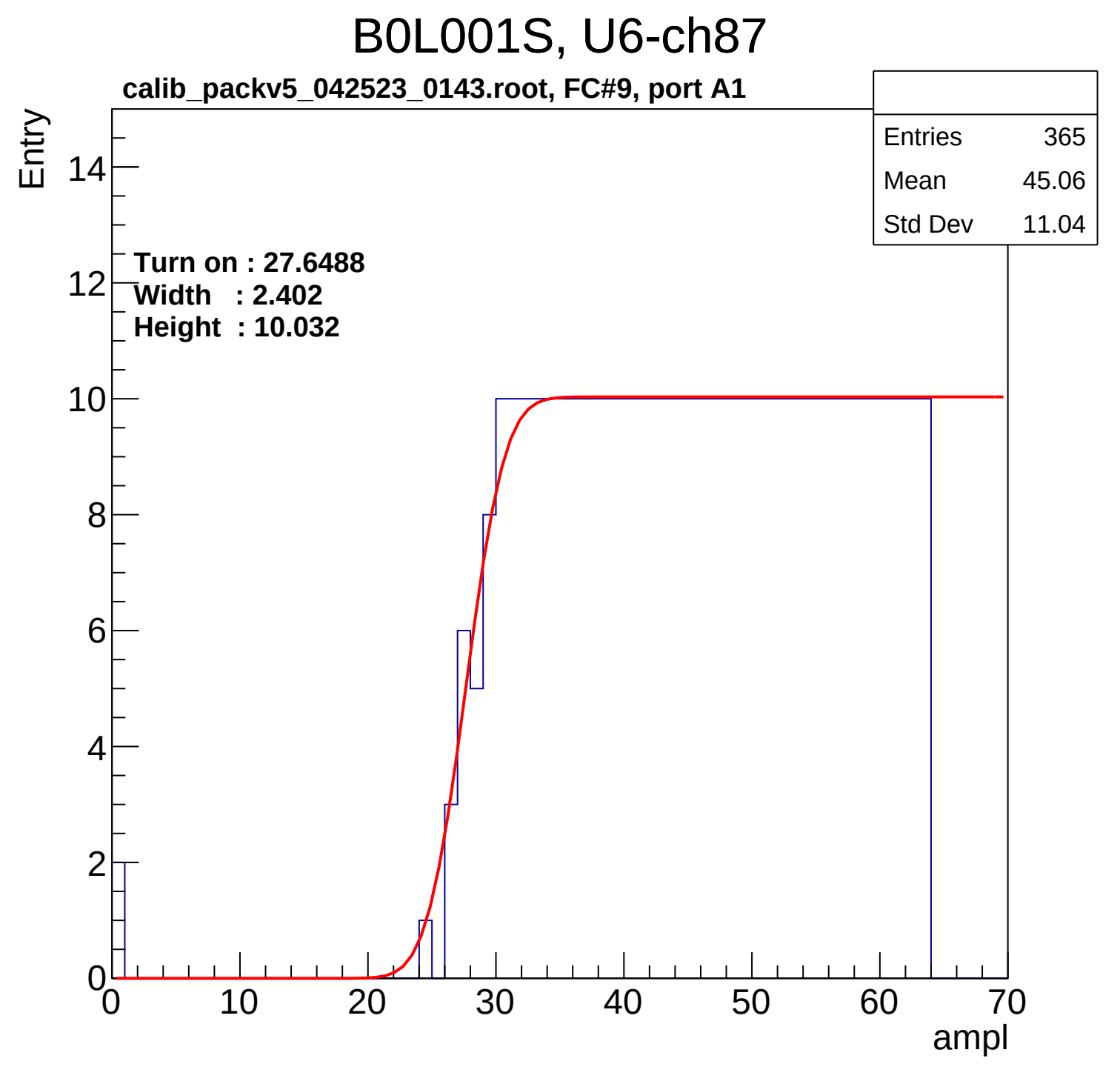
B0L001S, U6-ch87
calib_packv5_042523_0143.root, FC#9, port A1
Entries 365
Mean 45.06
Std Dev 11.04
Turn on : 27.6488
Width : 2.402
Height : 10.032
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ampl
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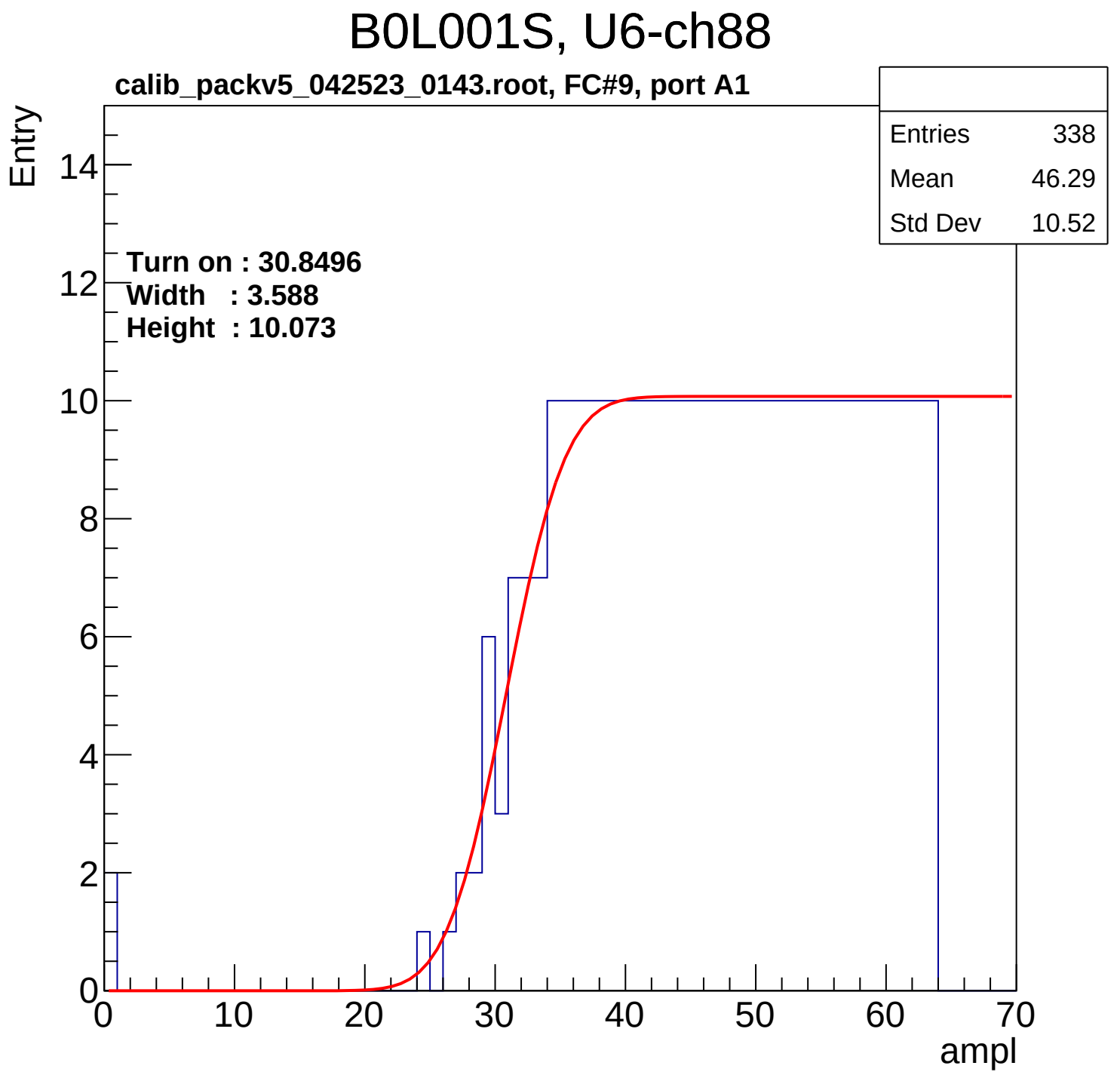
B0L001S, U6-ch88
calib_packv5_042523_0143.root, FC#9, port A1
Entries 338
Mean 46.29
Std Dev 10.52
Turn on : 30.8496
Width : 3.588
Height : 10.073
Entry
ampl
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2
4
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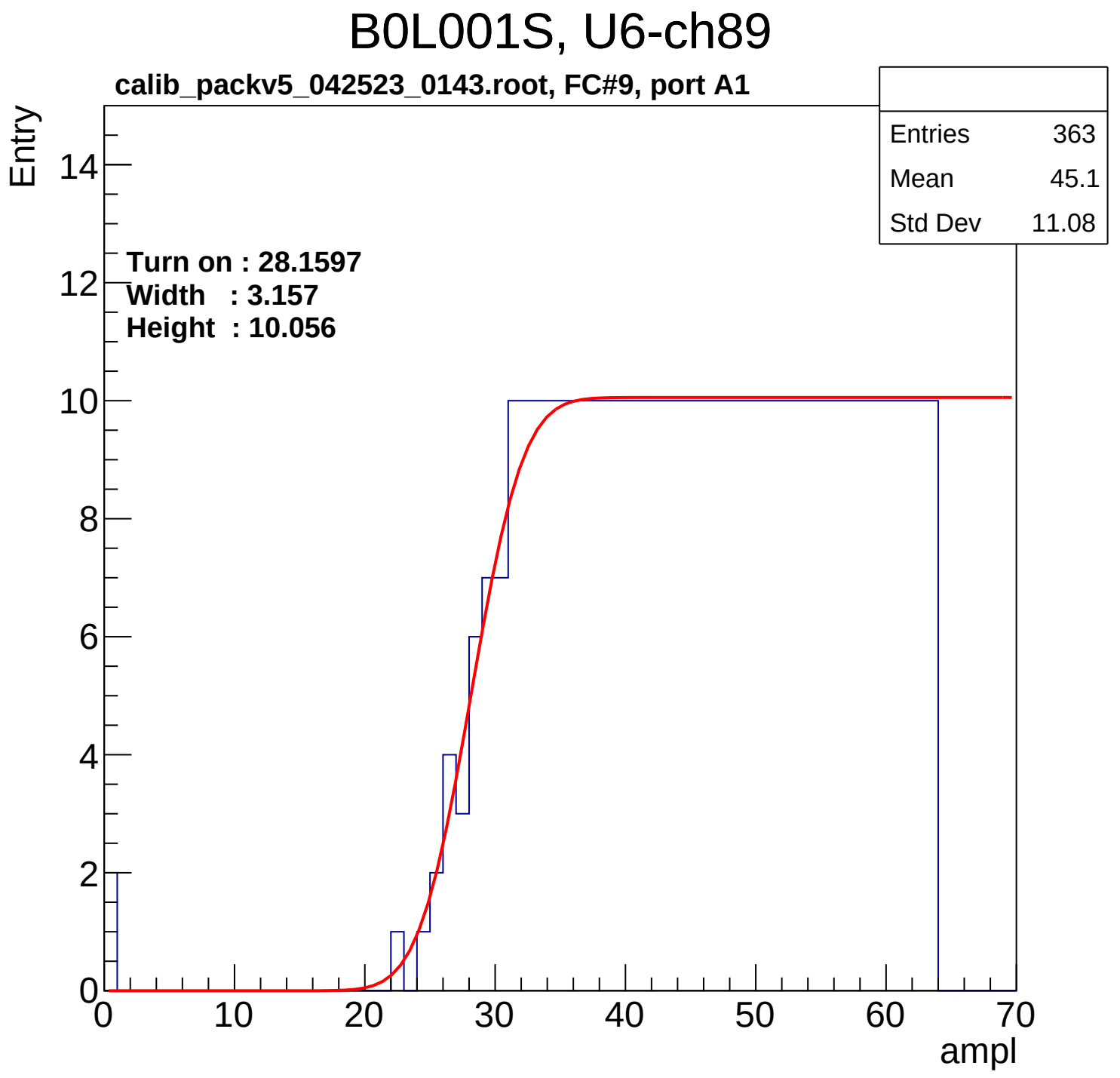
B0L001S, U6-ch89
calib_packv5_042523_0143.root, FC#9, port A1
Entries 363
Mean 45.1
Std Dev 11.08
Turn on : 28.1597
Width : 3.157
Height : 10.056
Entry
ampl
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2
4
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8
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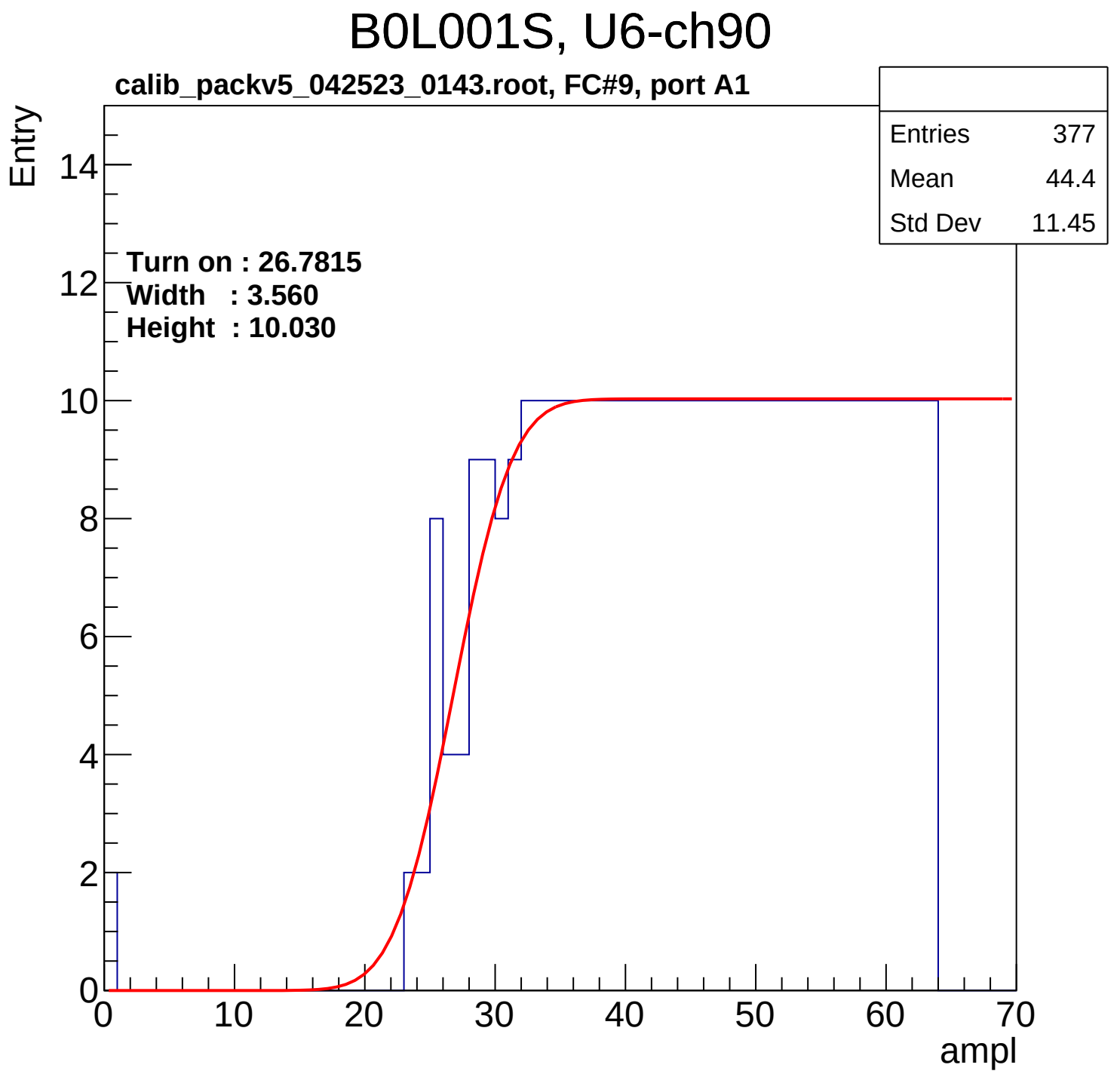
B0L001S, U6-ch90
calib_packv5_042523_0143.root, FC#9, port A1
Entries 377
Mean 44.4
Std Dev 11.45
Turn on : 26.7815
Width : 3.560
Height : 10.030
Entry
ampl
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2
4
6
8
10
12
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0
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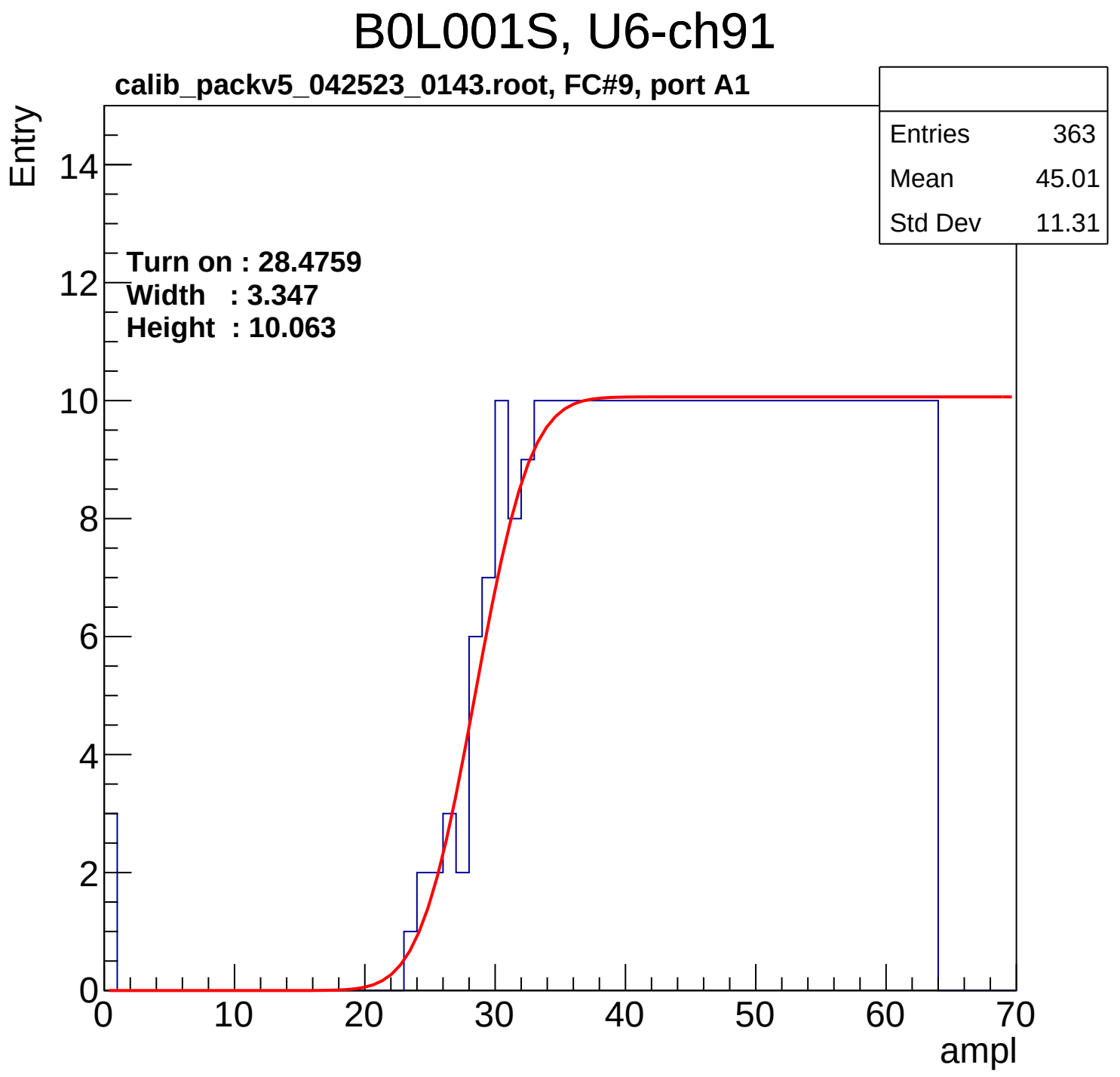
B0L001S, U6-ch91
calib_packv5_042523_0143.root, FC#9, port A1
Entries 363
Mean 45.01
Std Dev 11.31
Turn on : 28.4759
Width : 3.347
Height : 10.063
Entry
ampl
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2
4
6
8
10
12
14
0
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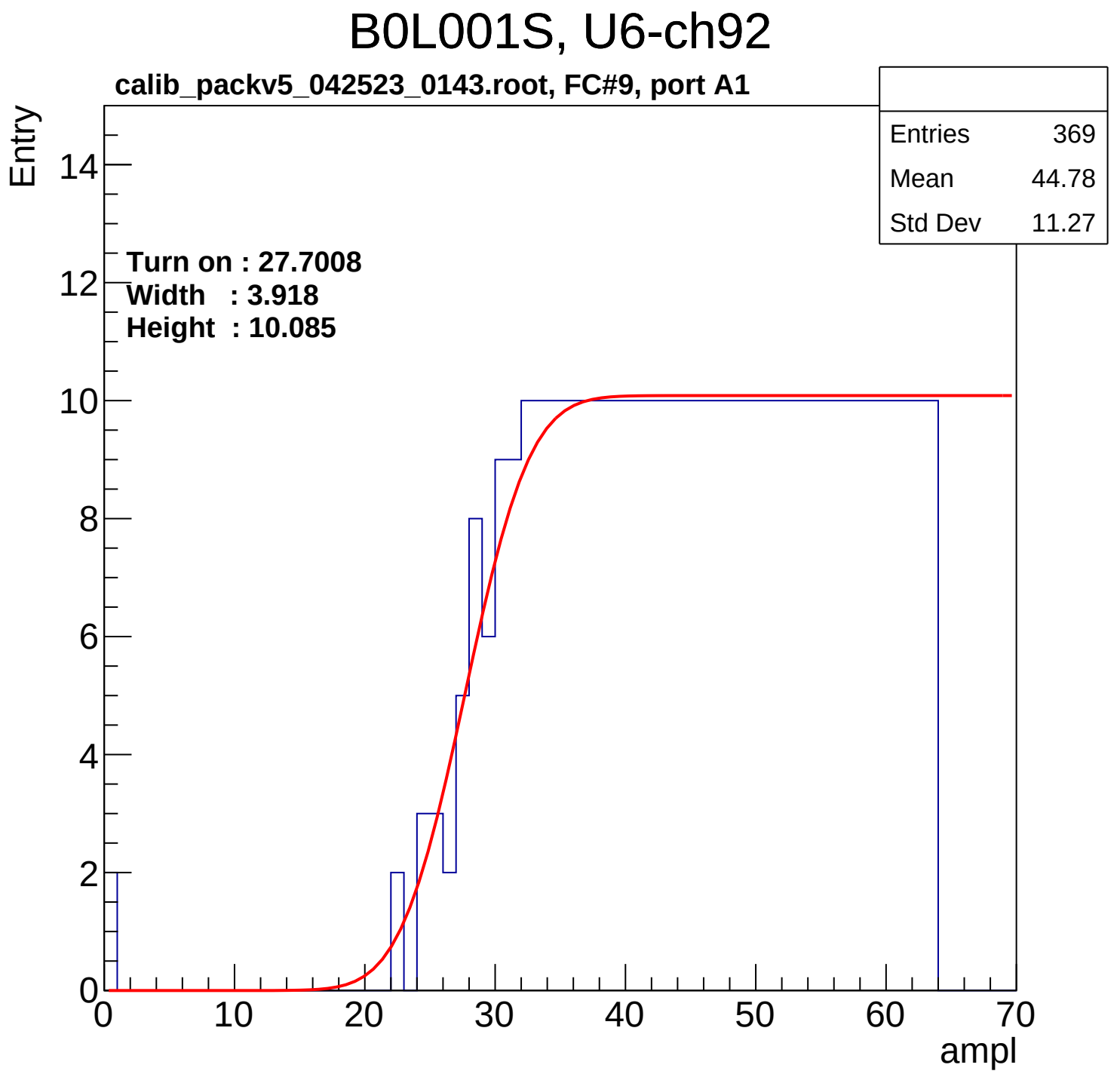
B0L001S, U6-ch92
calib_packv5_042523_0143.root, FC#9, port A1
Entries 369
Mean 44.78
Std Dev 11.27
Turn on : 27.7008
Width : 3.918
Height : 10.085
Entry
ampl
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2
4
6
8
10
12
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0
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60
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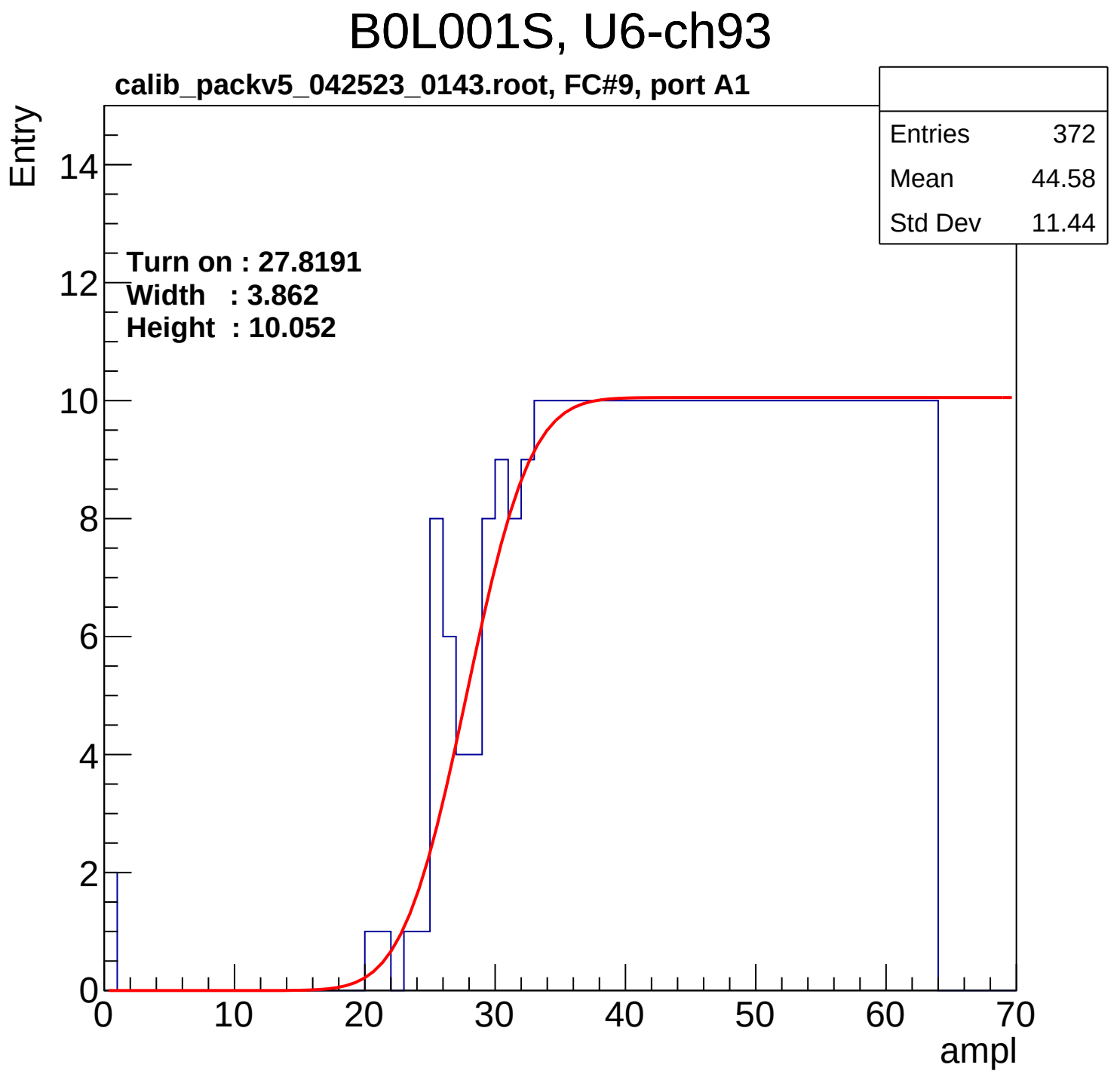
B0L001S, U6-ch93
calib_packv5_042523_0143.root, FC#9, port A1
Entries 372
Mean 44.58
Std Dev 11.44
Turn on : 27.8191
Width : 3.862
Height : 10.052
Entry
ampl
0
2
4
6
8
10
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0
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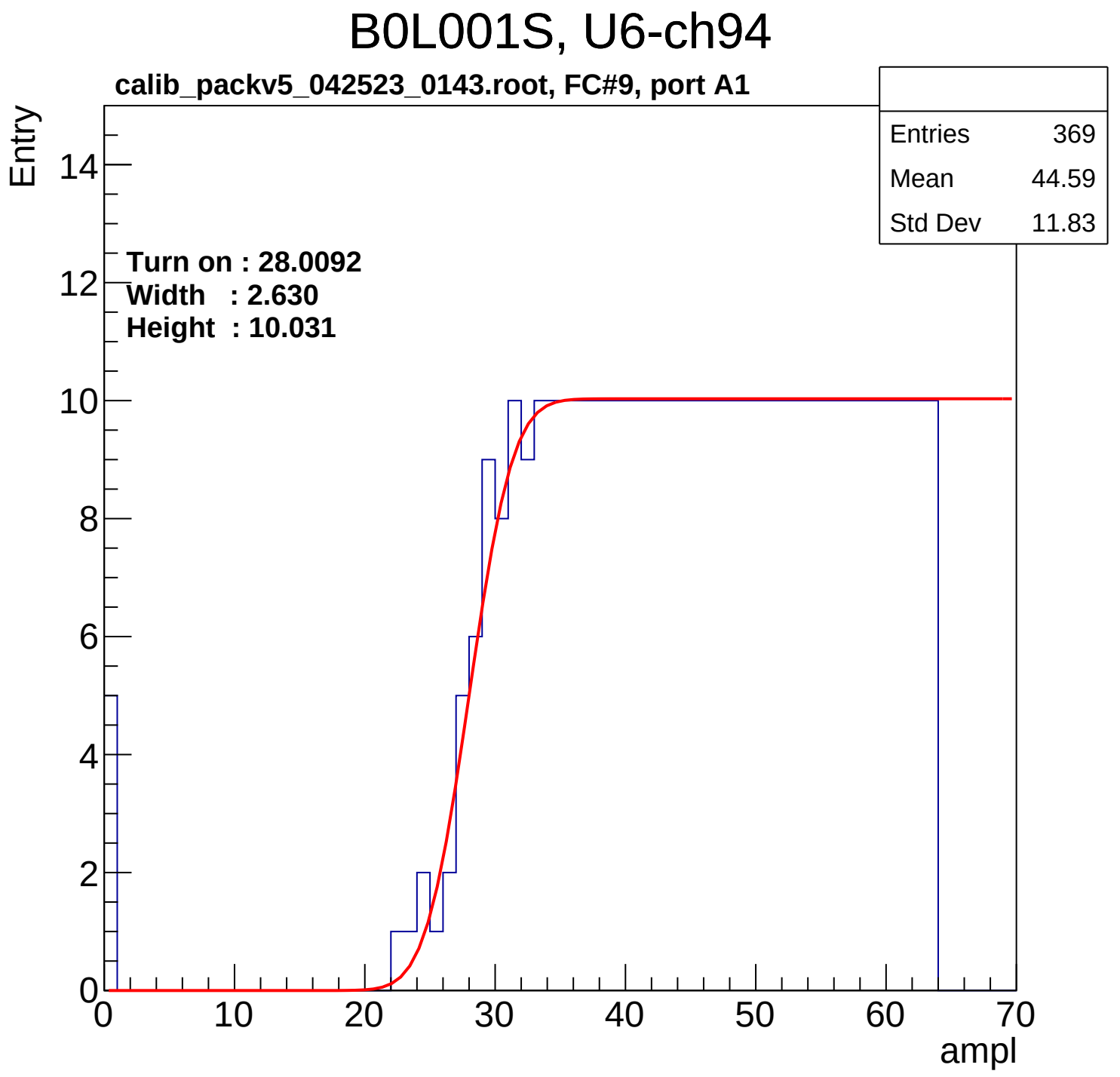
B0L001S, U6-ch94
calib_packv5_042523_0143.root, FC#9, port A1
Entries 369
Mean 44.59
Std Dev 11.83
Turn on : 28.0092
Width : 2.630
Height : 10.031
Entry
ampl
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2
4
6
8
10
12
14
0
10
20
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40
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60
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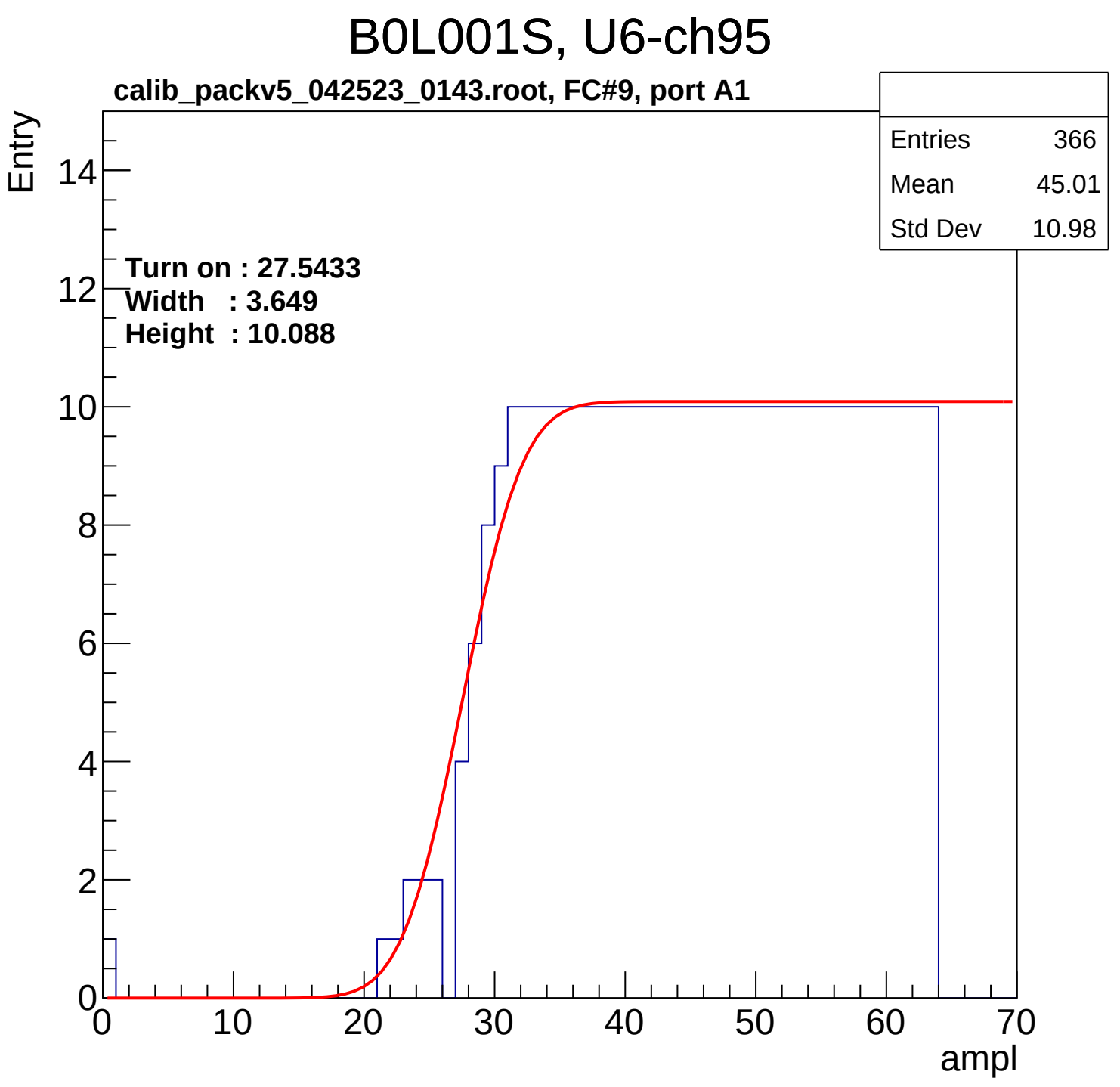
B0L001S, U6-ch95
calib_packv5_042523_0143.root, FC#9, port A1
Entries 366
Mean 45.01
Std Dev 10.98
Turn on : 27.5433
Width : 3.649
Height : 10.088
Entry
ampl
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2
4
6
8
10
12
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0
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20
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40
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60
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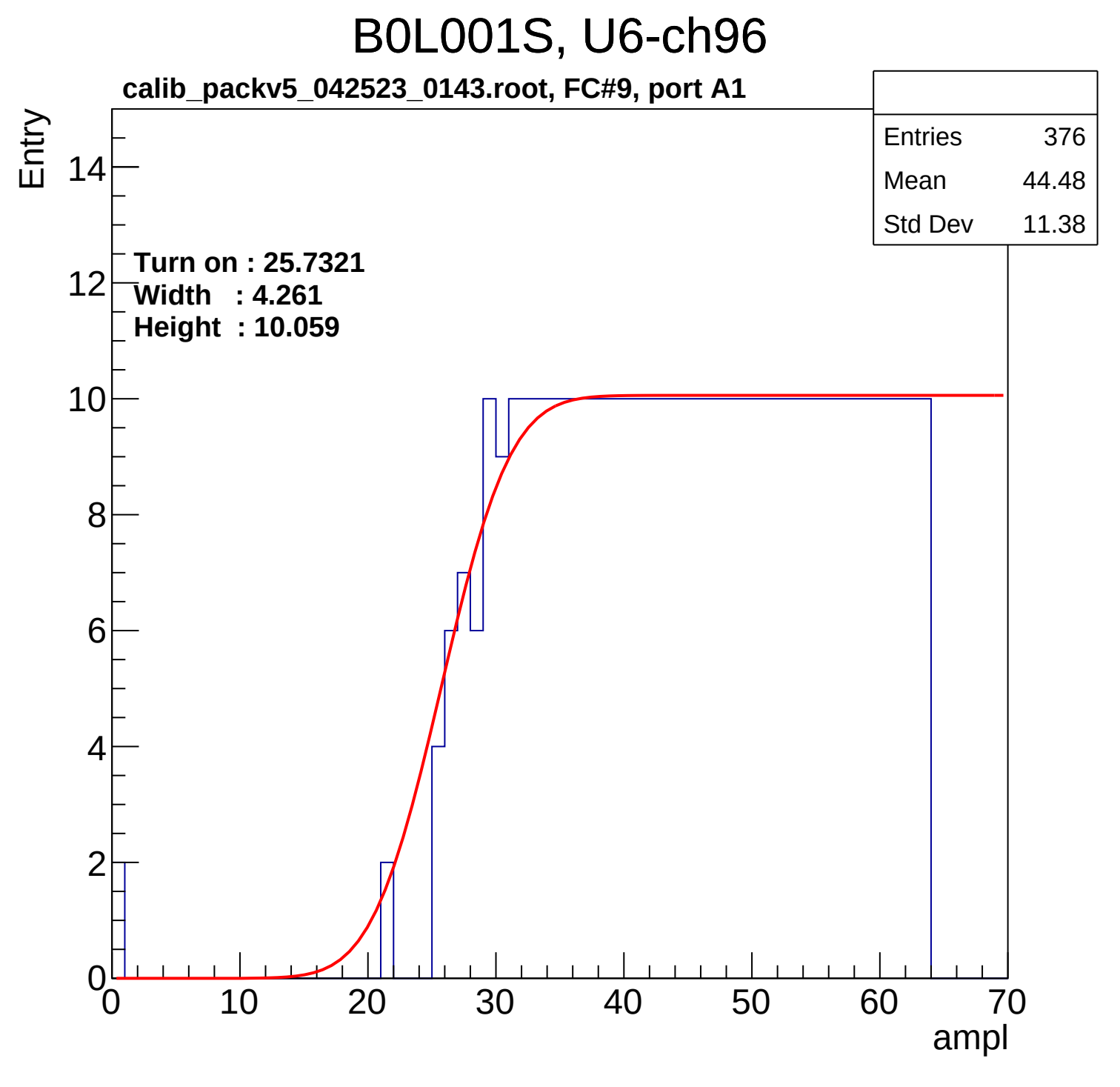
B0L001S, U6-ch96
calib_packv5_042523_0143.root, FC#9, port A1
Entries 376
Mean 44.48
Std Dev 11.38
Turn on : 25.7321
Width : 4.261
Height : 10.059
Entry
ampl
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2
4
6
8
10
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0
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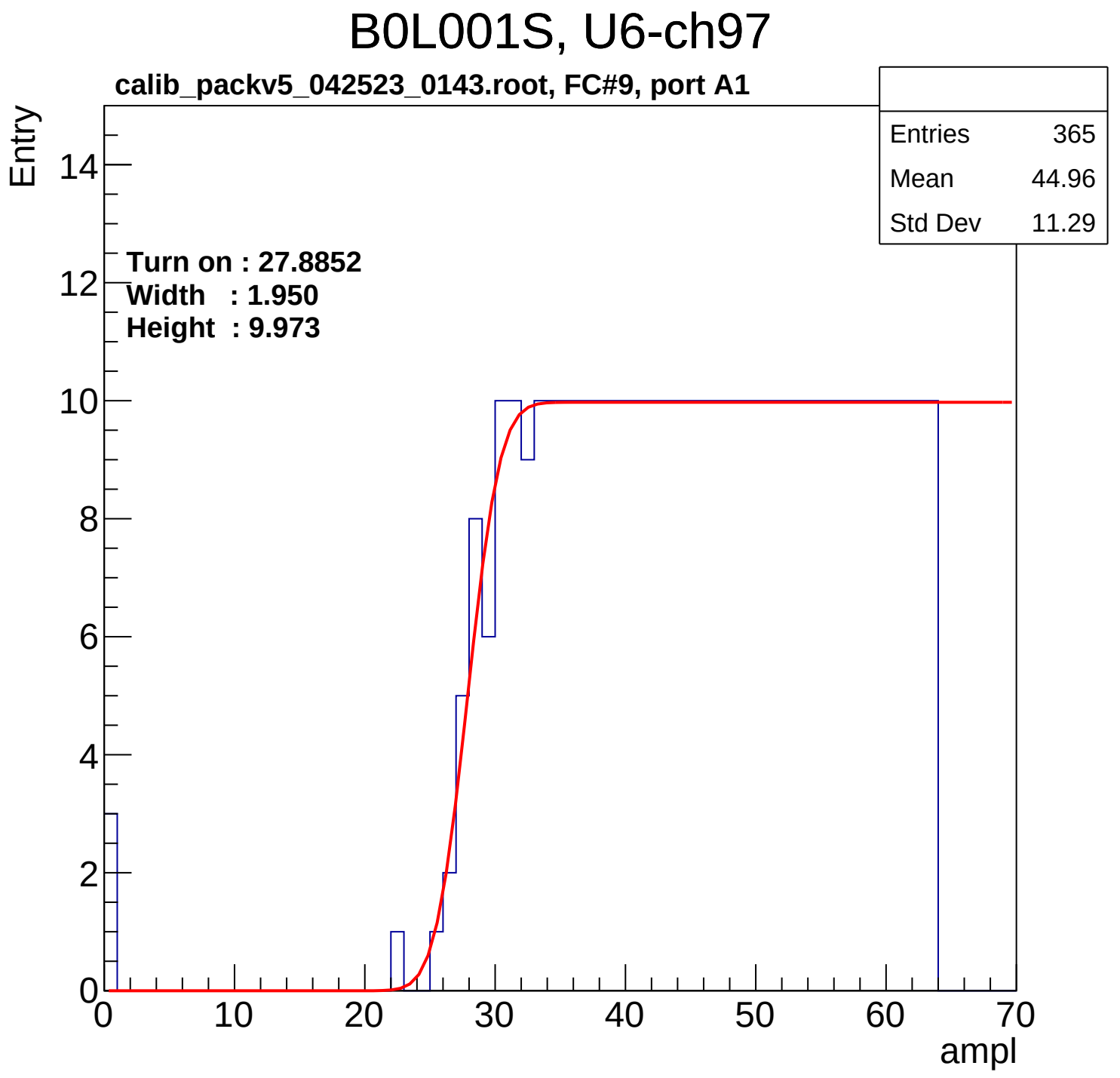
B0L001S, U6-ch97
calib_packv5_042523_0143.root, FC#9, port A1
Entries 365
Mean 44.96
Std Dev 11.29
Turn on : 27.8852
Width : 1.950
Height : 9.973
Entry
ampl
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4
6
8
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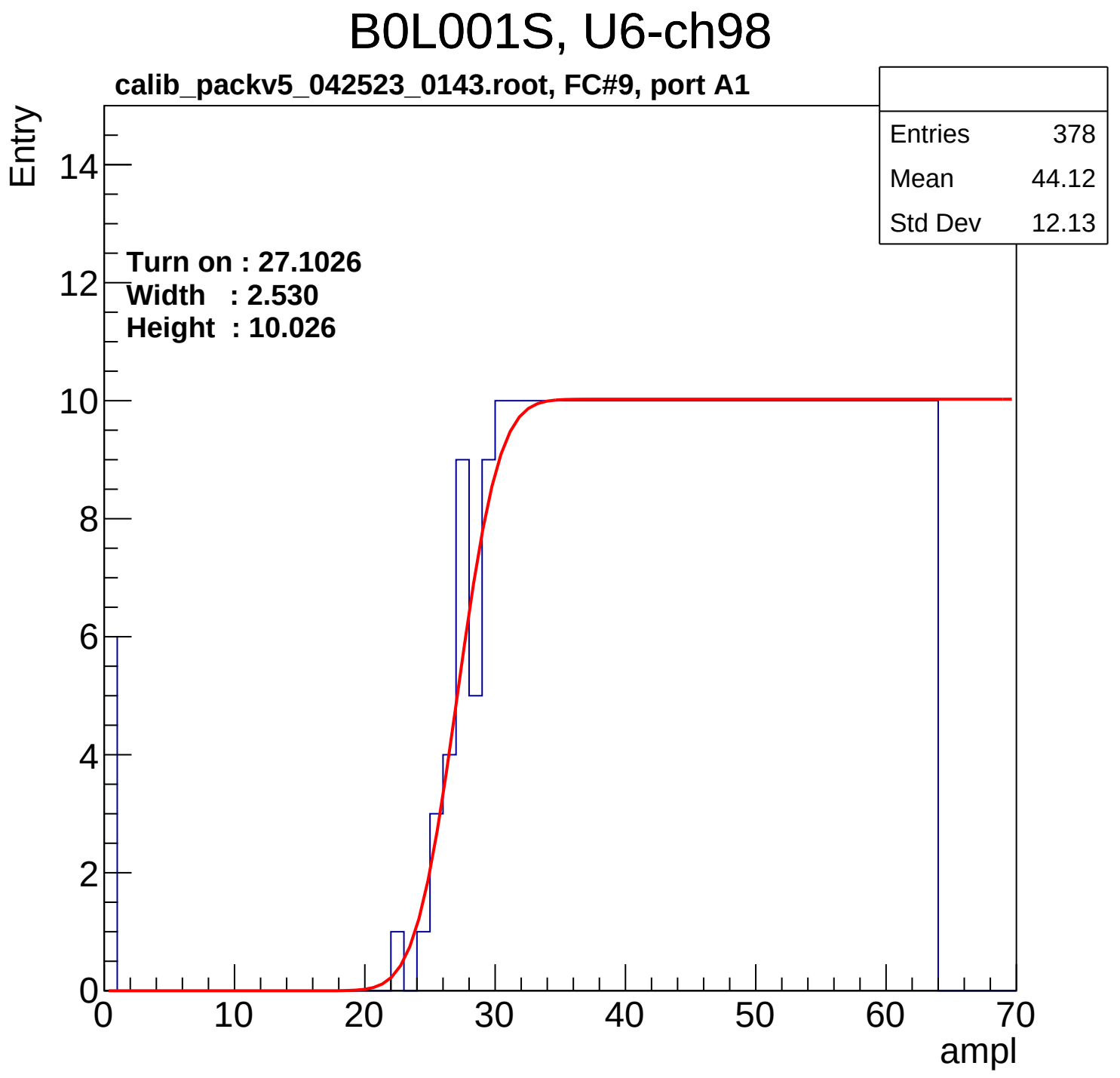
B0L001S, U6-ch98
calib_packv5_042523_0143.root, FC#9, port A1
Entries 378
Mean 44.12
Std Dev 12.13
Turn on : 27.1026
Width : 2.530
Height : 10.026
Entry
ampl
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2
4
6
8
10
12
14
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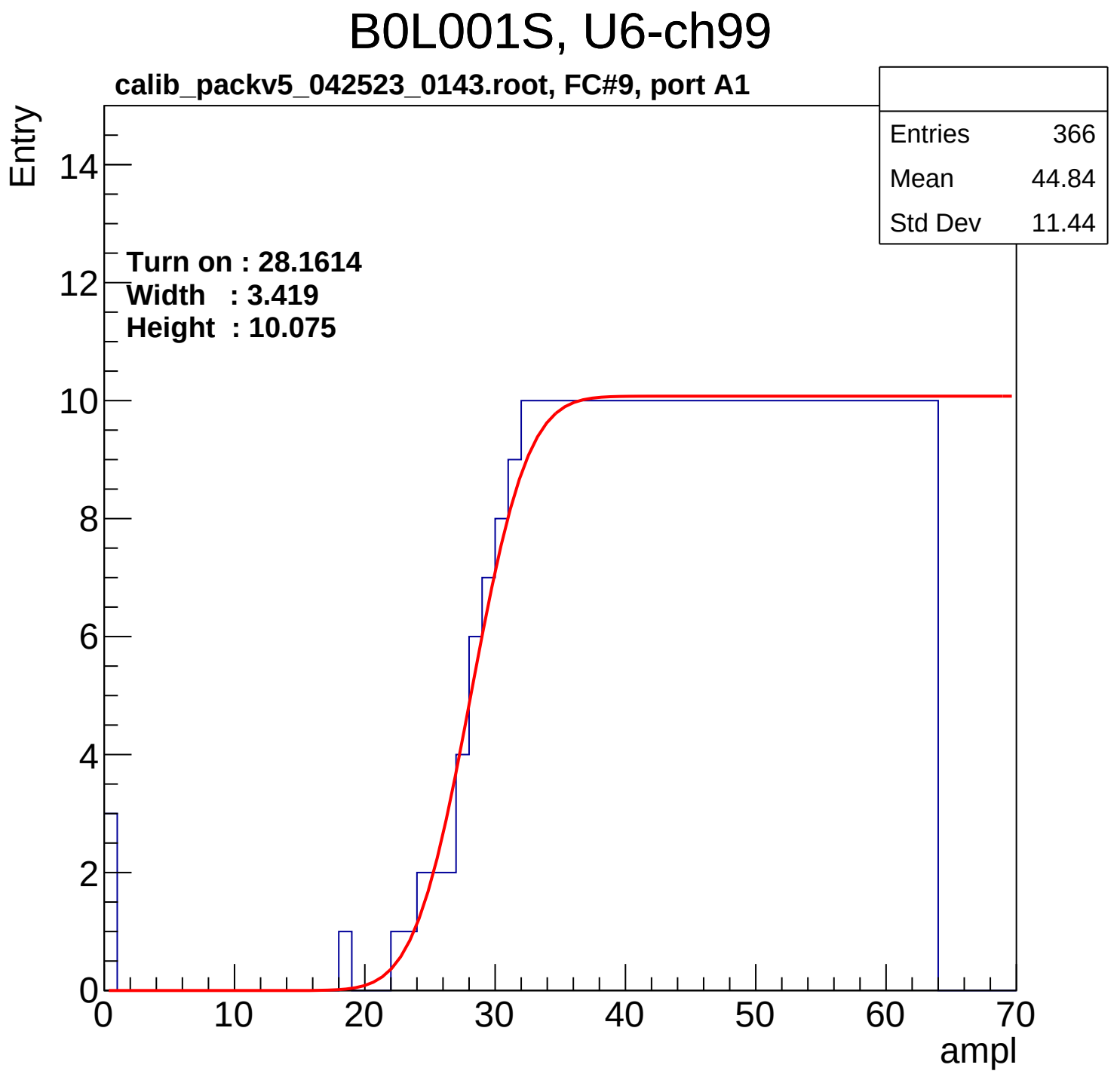
B0L001S, U6-ch99
calib_packv5_042523_0143.root, FC#9, port A1
Entries 366
Mean 44.84
Std Dev 11.44
Turn on : 28.1614
Width : 3.419
Height : 10.075
Entry
ampl
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6
8
10
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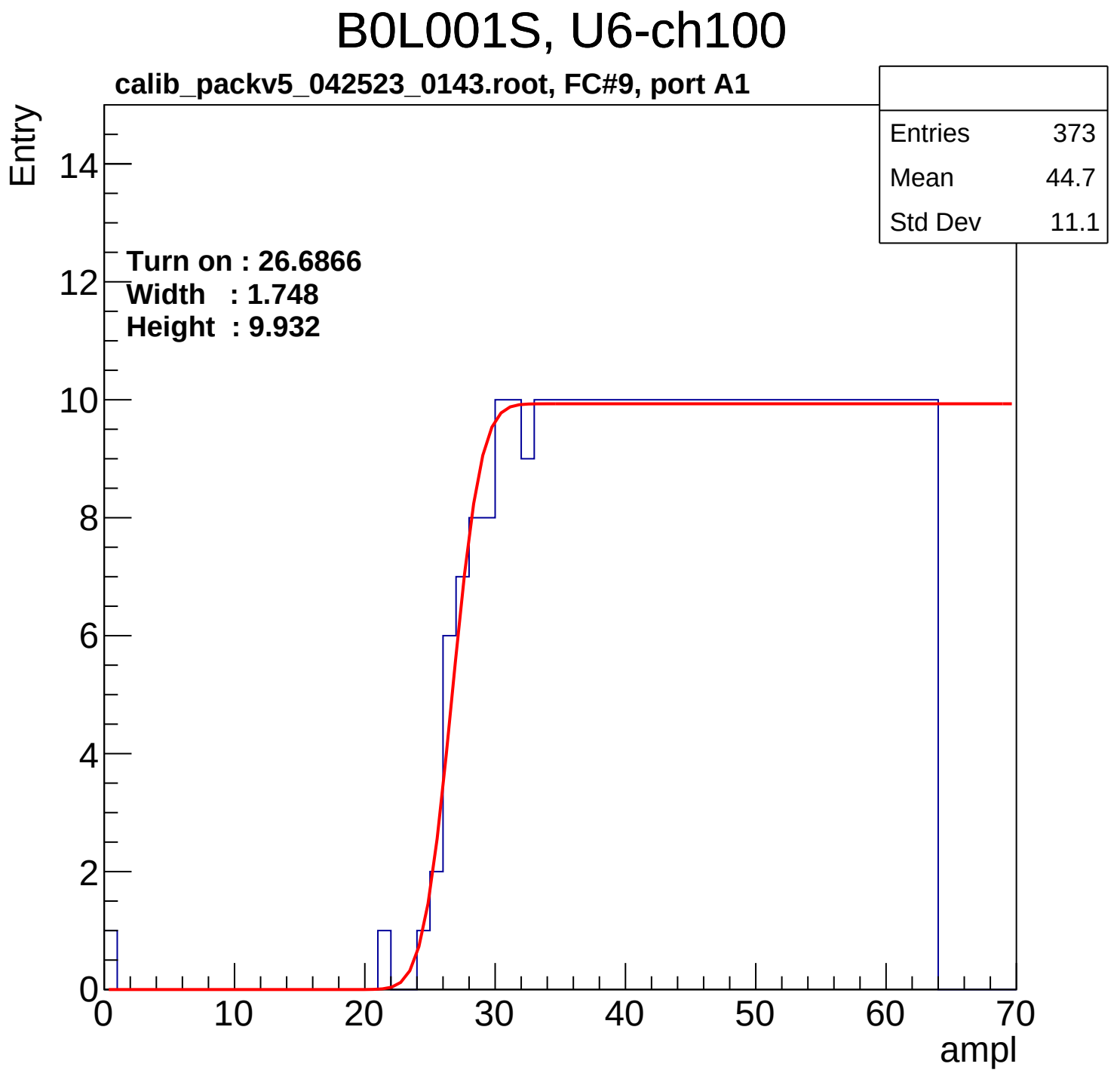
B0L001S, U6-ch100
calib_packv5_042523_0143.root, FC#9, port A1
Entries 373
Mean 44.7
Std Dev 11.1
Turn on : 26.6866
Width : 1.748
Height : 9.932
Entry
ampl
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6
8
10
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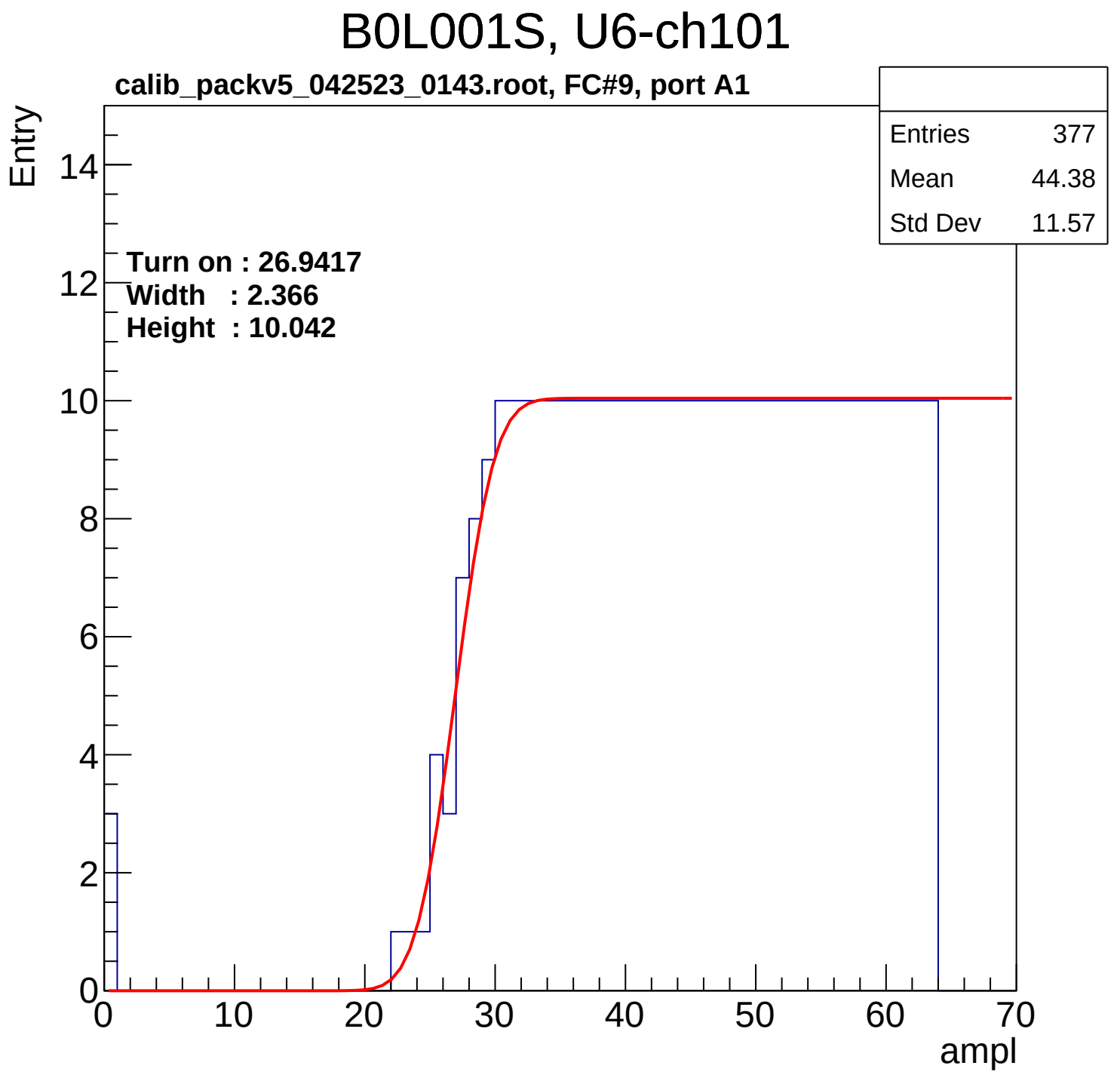
B0L001S, U6-ch101
calib_packv5_042523_0143.root, FC#9, port A1
Entries 377
Mean 44.38
Std Dev 11.57
Turn on : 26.9417
Width : 2.366
Height : 10.042
Entry
ampl
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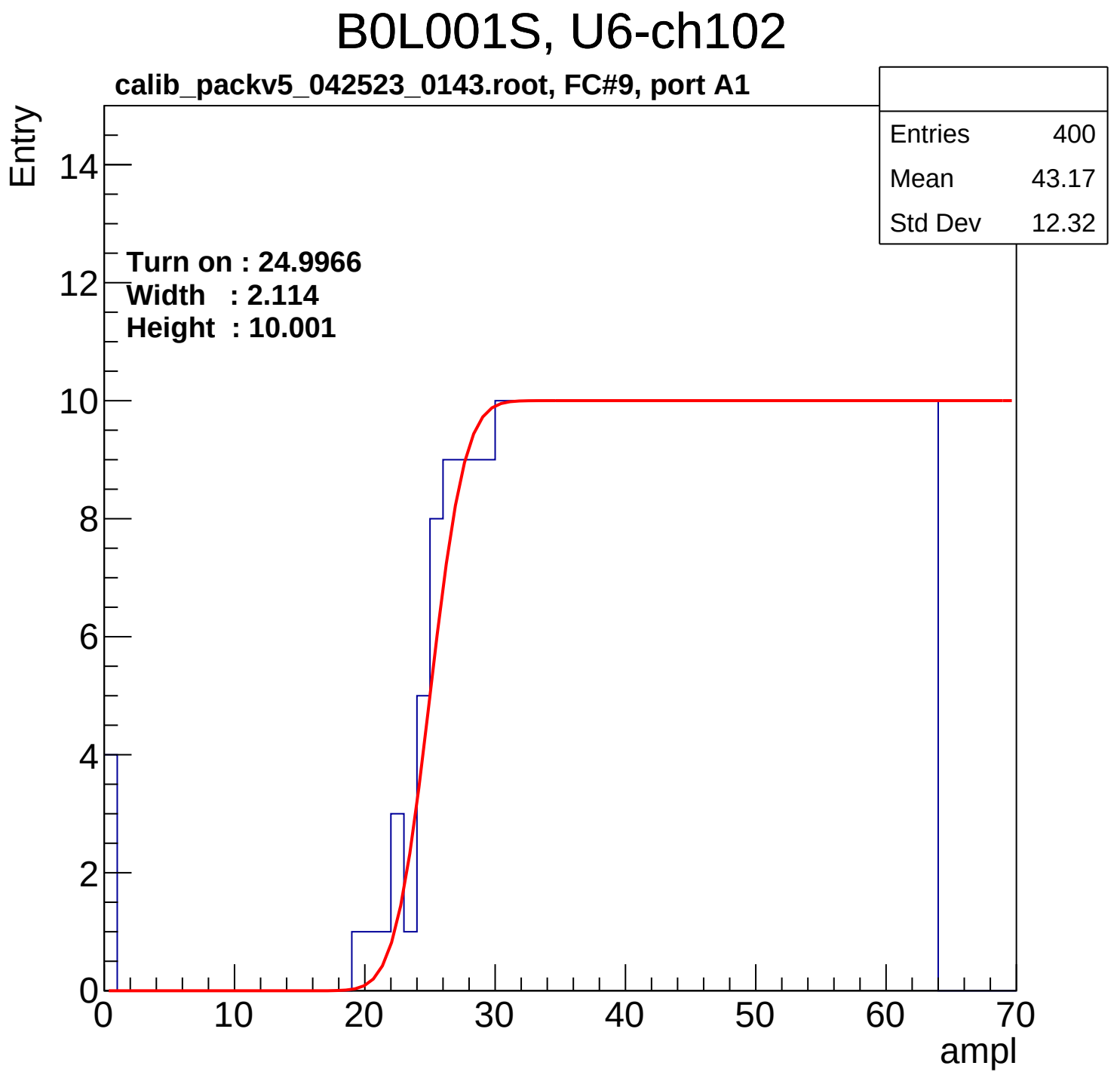
B0L001S, U6-ch102
calib_packv5_042523_0143.root, FC#9, port A1
Entries 400
Mean 43.17
Std Dev 12.32
Turn on : 24.9966
Width : 2.114
Height : 10.001
Entry
ampl
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8
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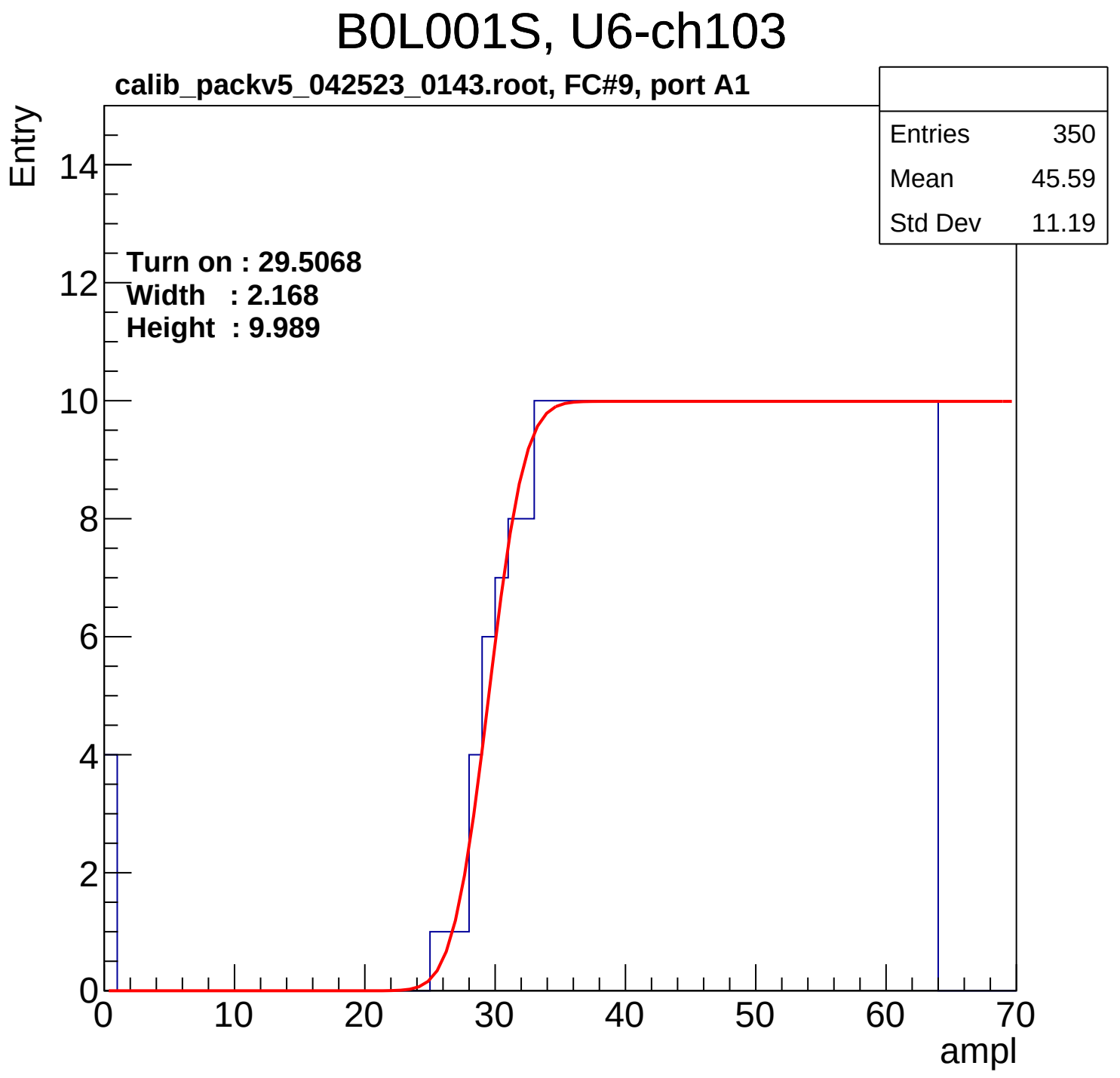
B0L001S, U6-ch103
calib_packv5_042523_0143.root, FC#9, port A1
Entries 350
Mean 45.59
Std Dev 11.19
Turn on : 29.5068
Width : 2.168
Height : 9.989
Entry
ampl
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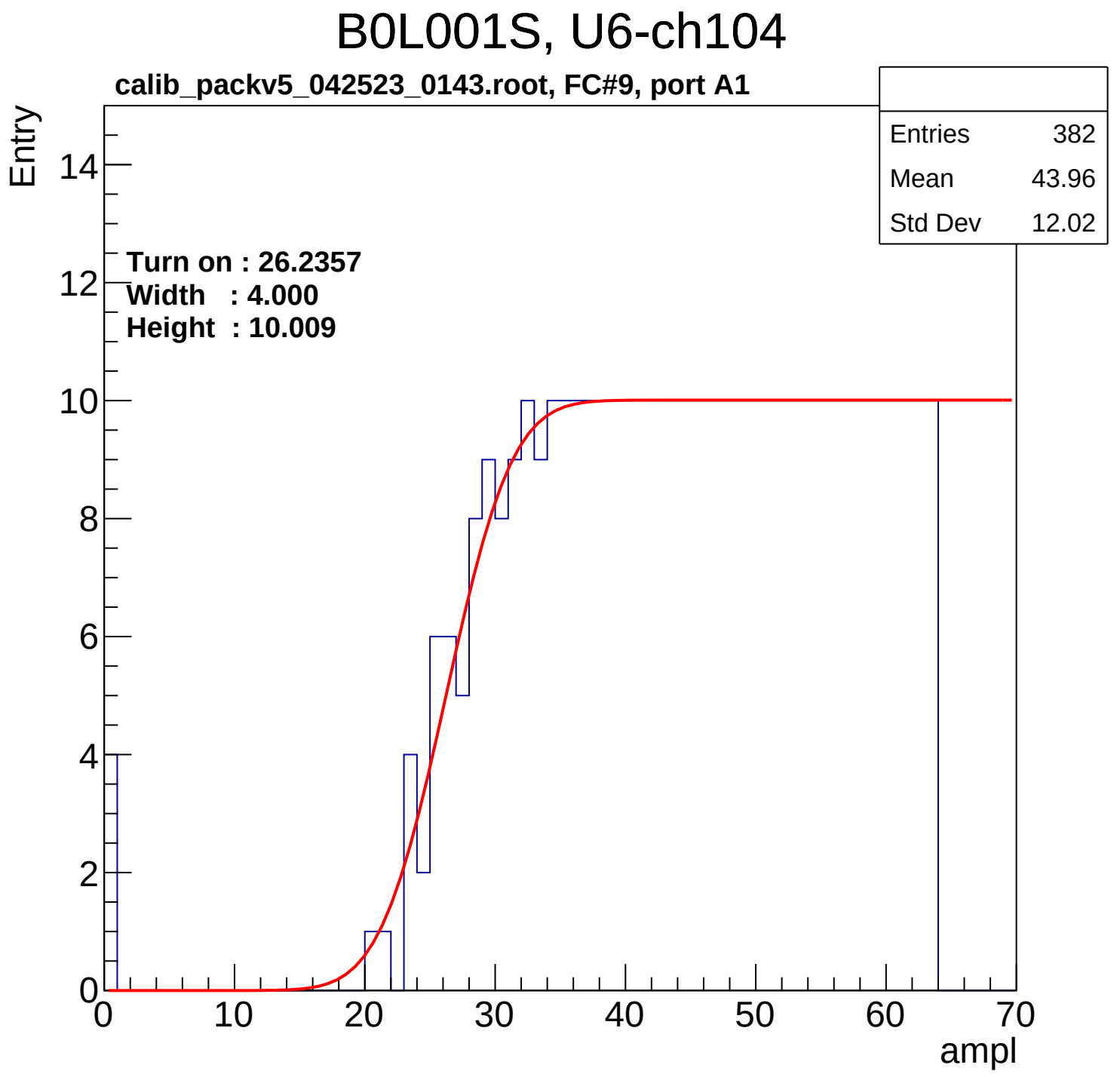
B0L001S, U6-ch104
calib_packv5_042523_0143.root, FC#9, port A1
Entries 382
Mean 43.96
Std Dev 12.02
Turn on : 26.2357
Width : 4.000
Height : 10.009
Entry
ampl
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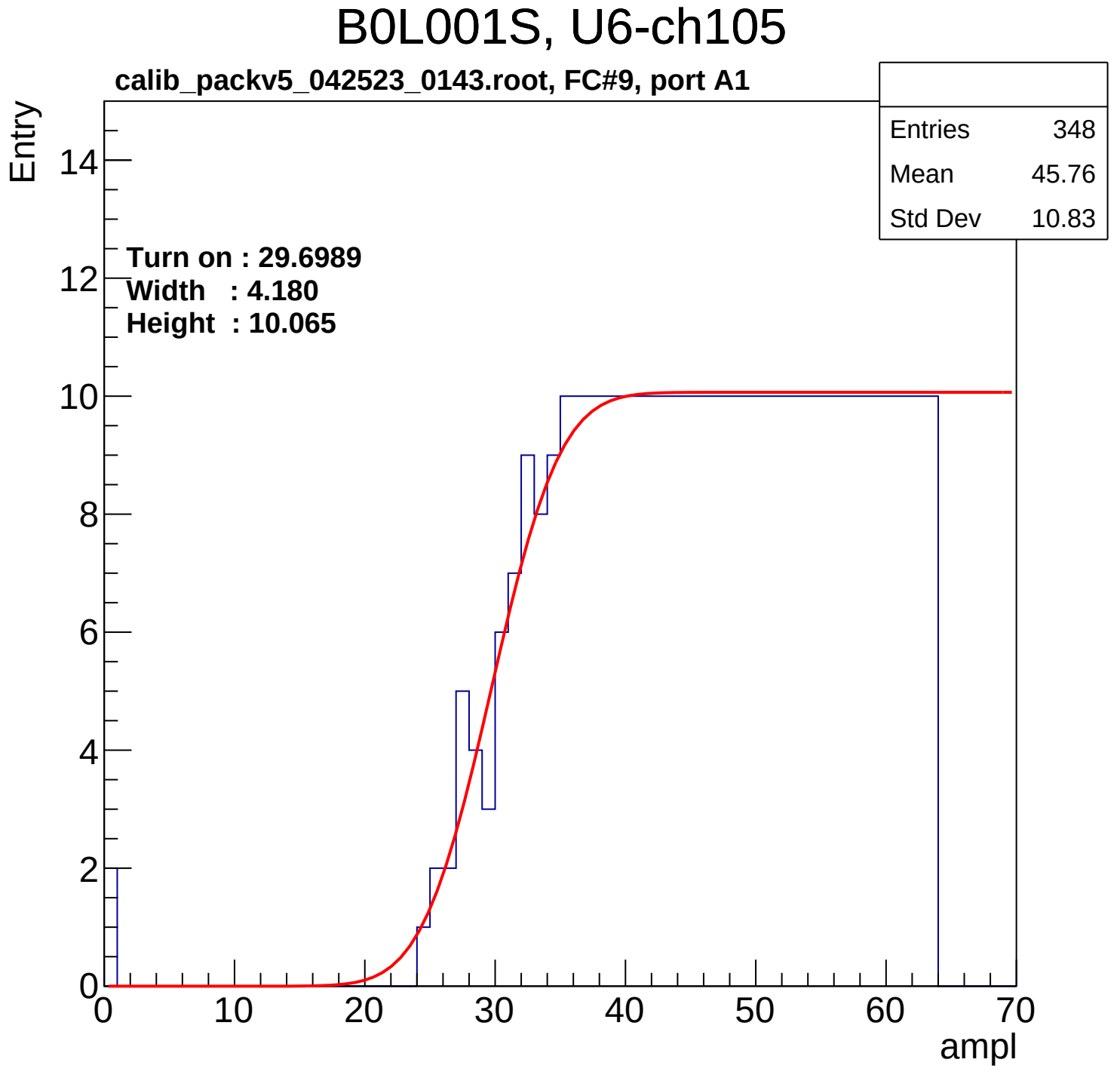
B0L001S, U6-ch105
calib_packv5_042523_0143.root, FC#9, port A1
Entries 348
Mean 45.76
Std Dev 10.83
Turn on : 29.6989
Width : 4.180
Height : 10.065
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ampl
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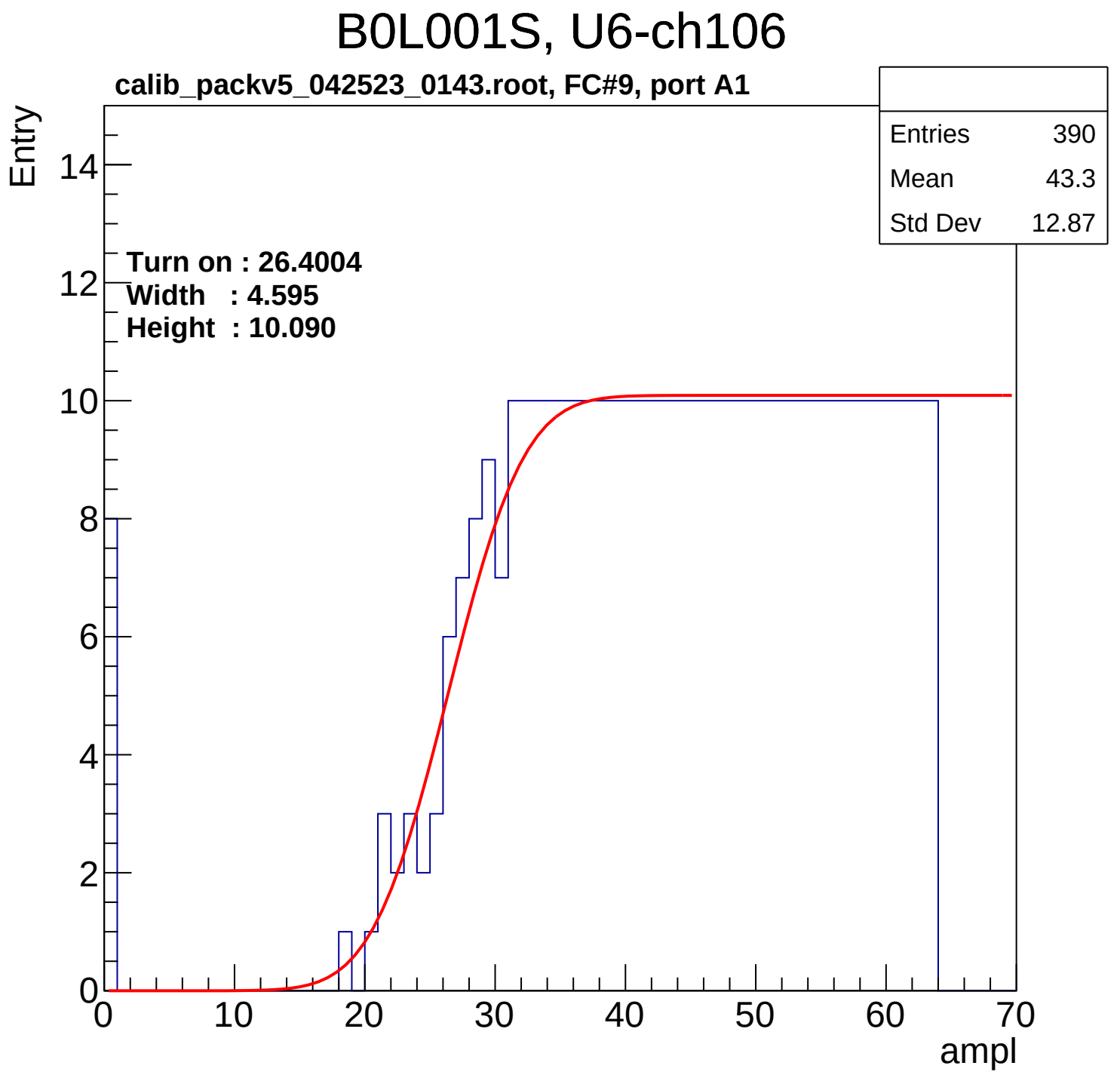
B0L001S, U6-ch106
calib_packv5_042523_0143.root, FC#9, port A1
Entries 390
Mean 43.3
Std Dev 12.87
Turn on : 26.4004
Width : 4.595
Height : 10.090
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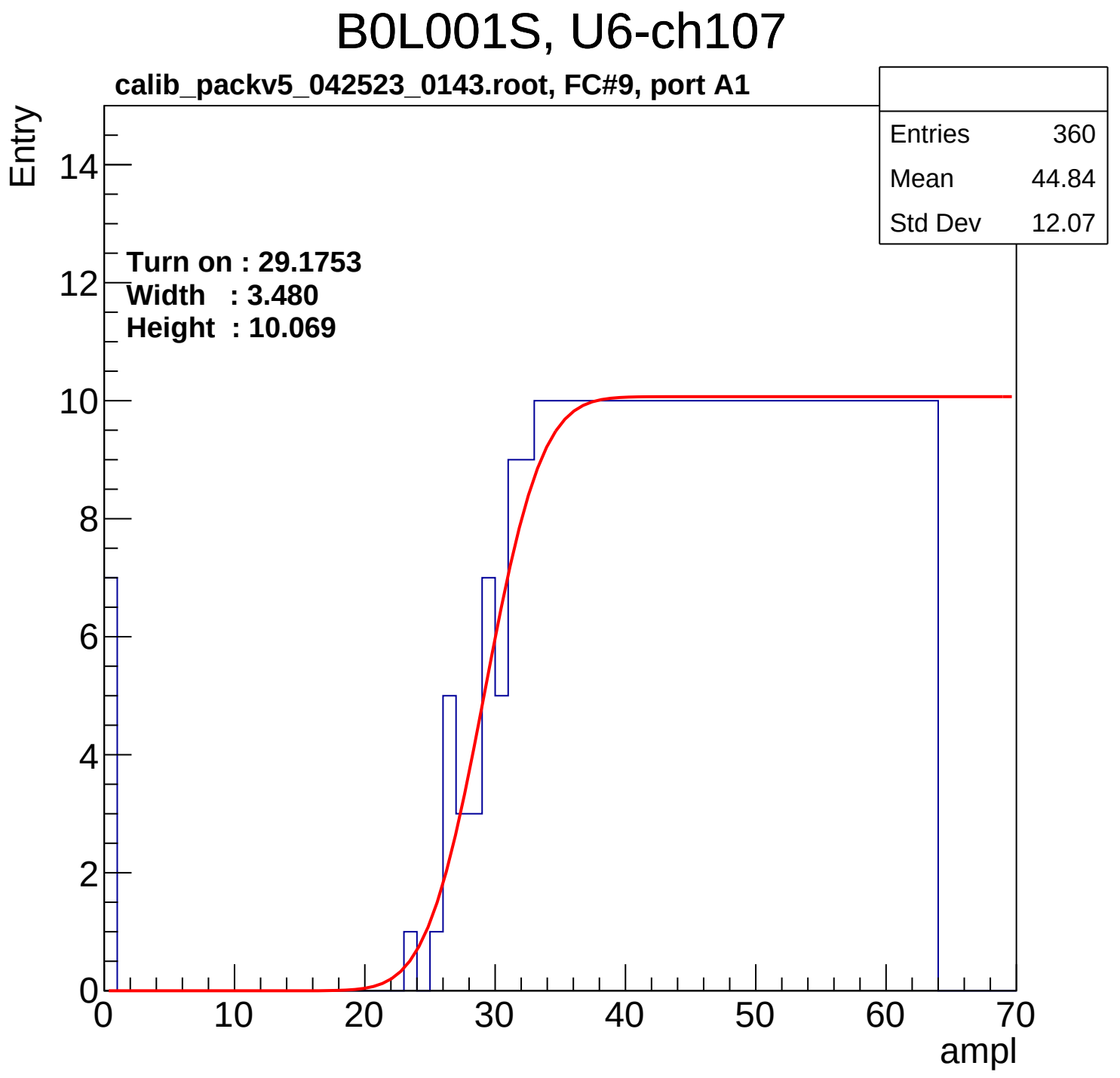
B0L001S, U6-ch107
calib_packv5_042523_0143.root, FC#9, port A1
Entries 360
Mean 44.84
Std Dev 12.07
Turn on : 29.1753
Width : 3.480
Height : 10.069
Entry
ampl
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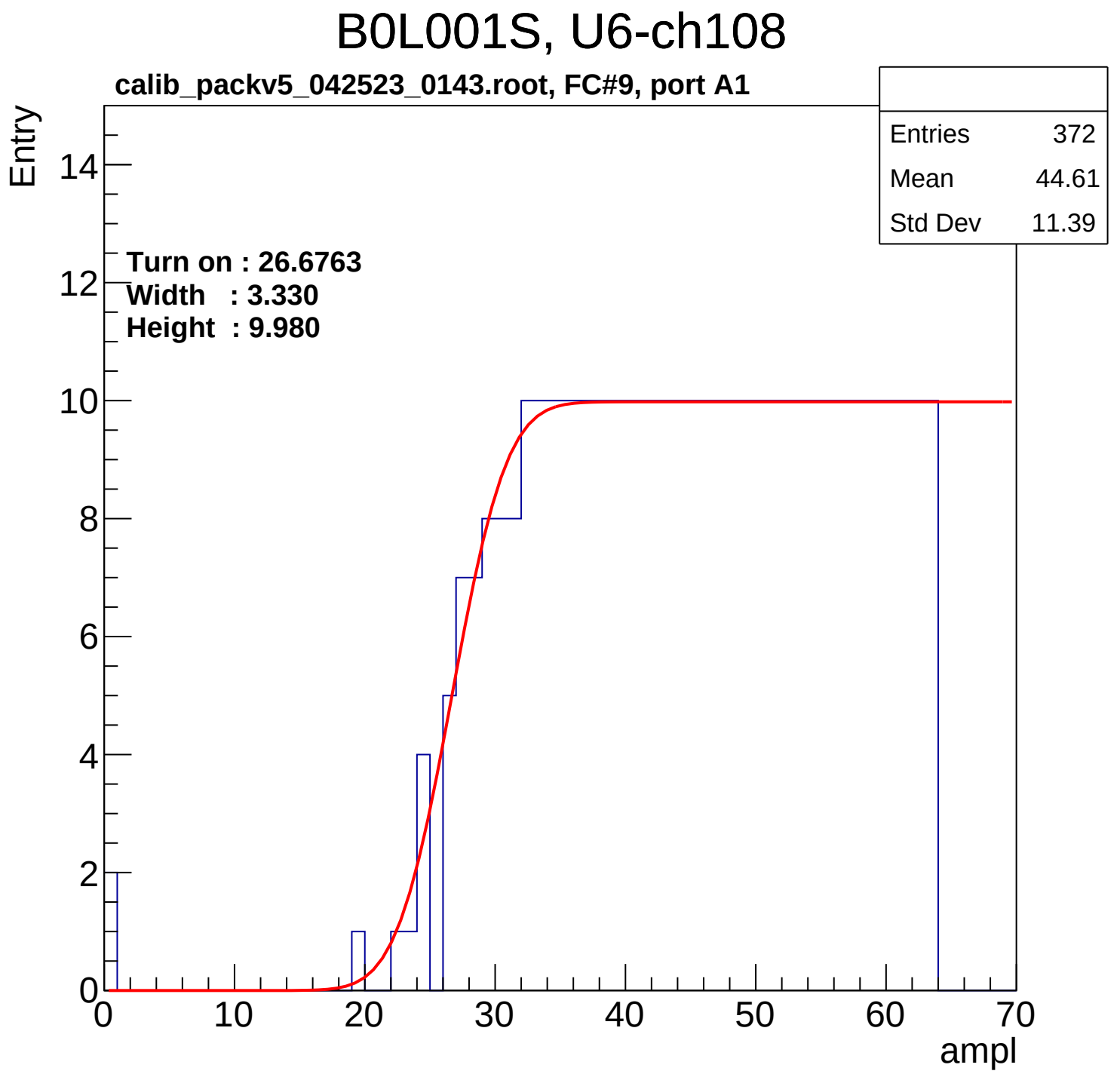
B0L001S, U6-ch108
calib_packv5_042523_0143.root, FC#9, port A1
Entries 372
Mean 44.61
Std Dev 11.39
Turn on : 26.6763
Width : 3.330
Height : 9.980
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ampl
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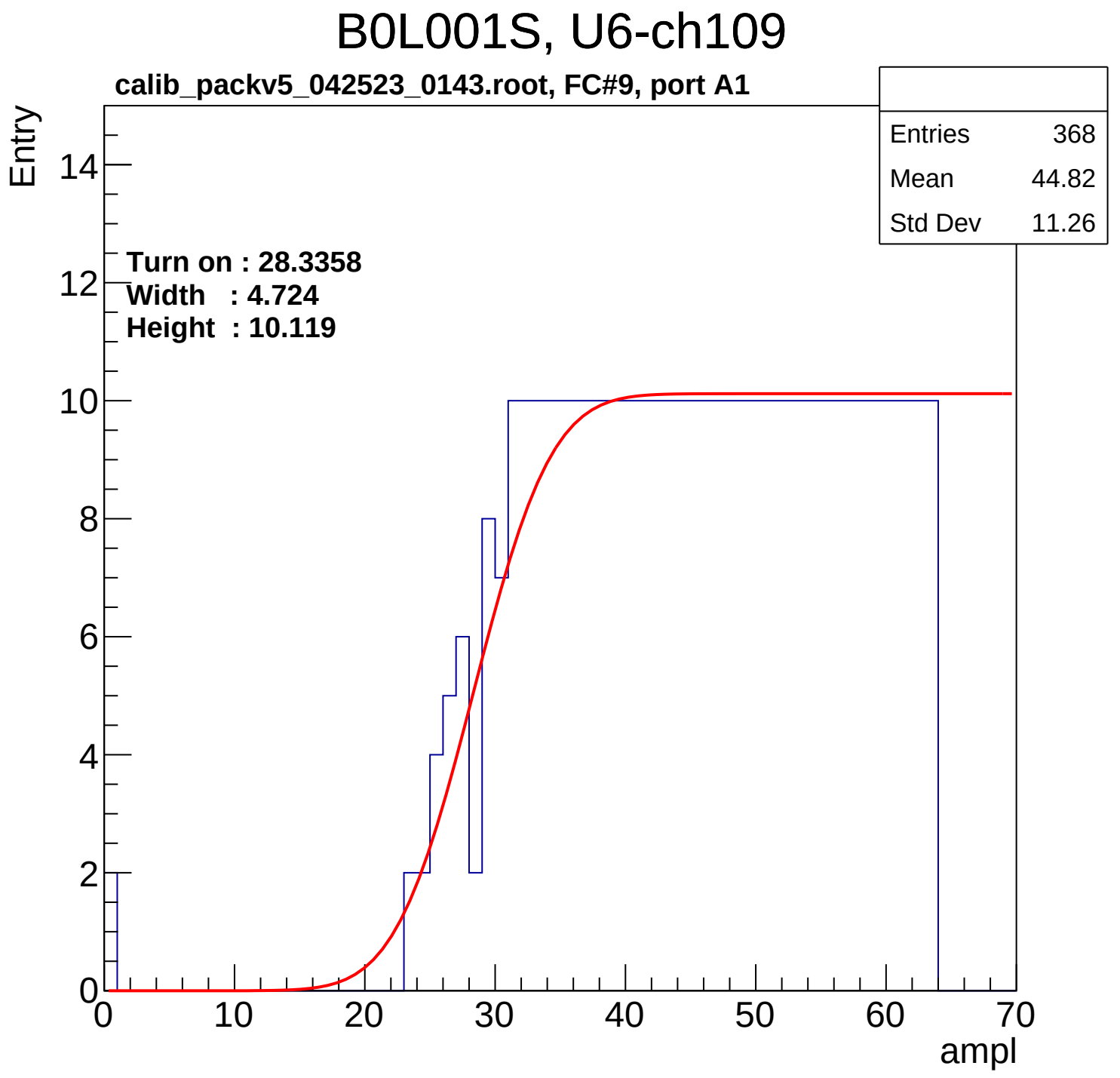
B0L001S, U6-ch109
calib_packv5_042523_0143.root, FC#9, port A1
Entries 368
Mean 44.82
Std Dev 11.26
Turn on : 28.3358
Width : 4.724
Height : 10.119
Entry
ampl
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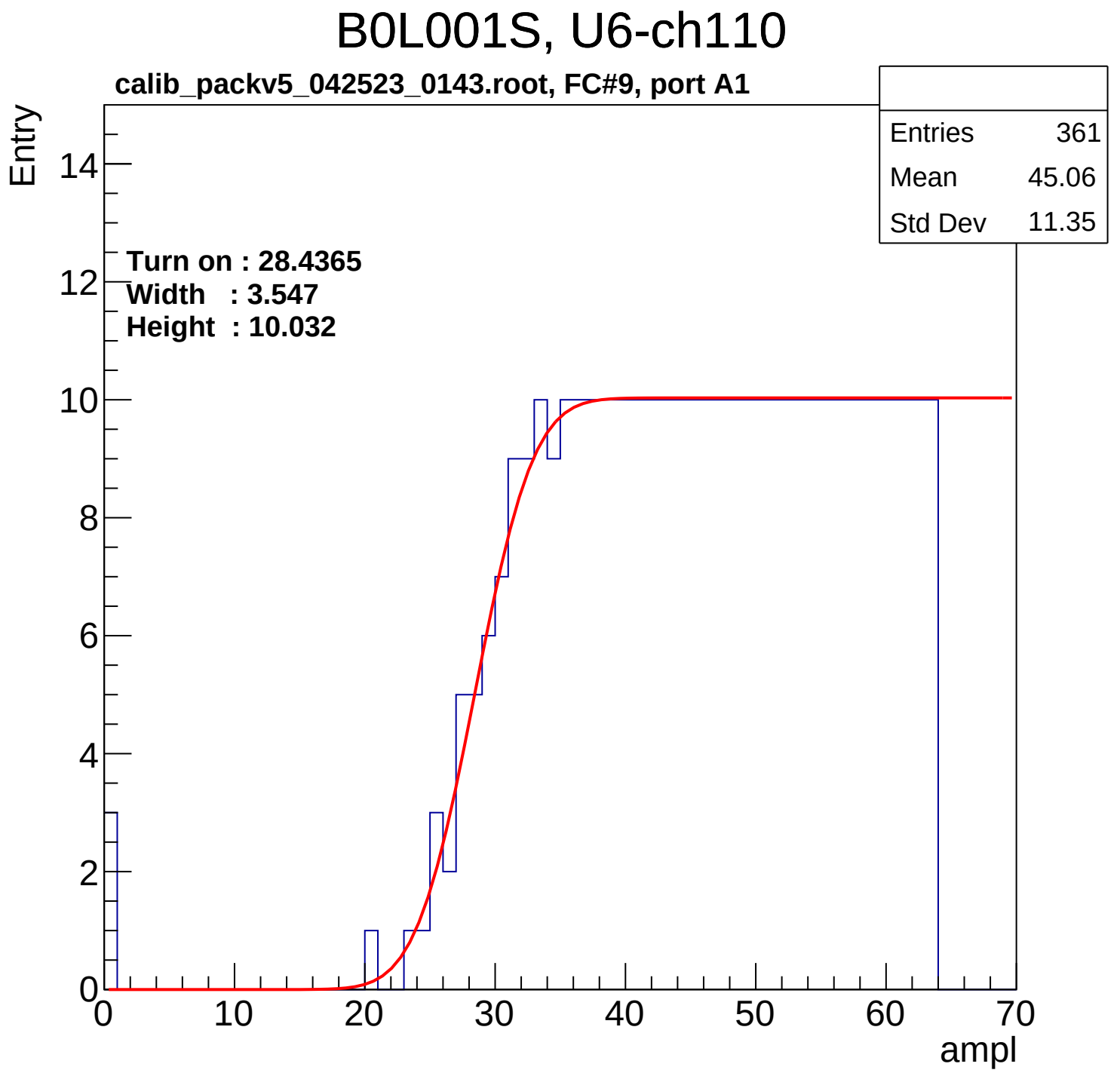
B0L001S, U6-ch110
calib_packv5_042523_0143.root, FC#9, port A1
Entries 361
Mean 45.06
Std Dev 11.35
Turn on : 28.4365
Width : 3.547
Height : 10.032
Entry
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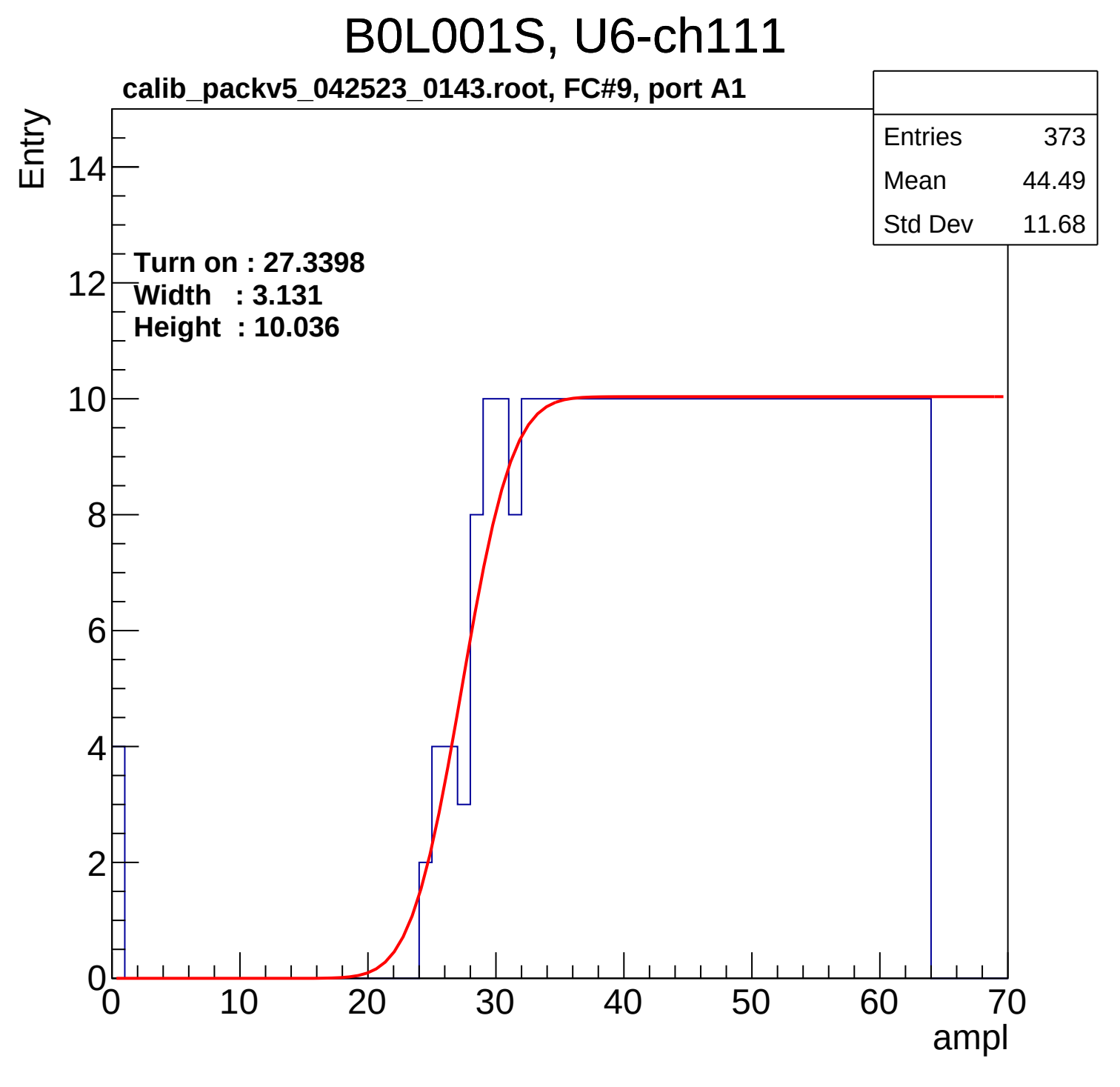
B0L001S, U6-ch111
calib_packv5_042523_0143.root, FC#9, port A1
Entries 373
Mean 44.49
Std Dev 11.68
Turn on : 27.3398
Width : 3.131
Height : 10.036
Entry
ampl
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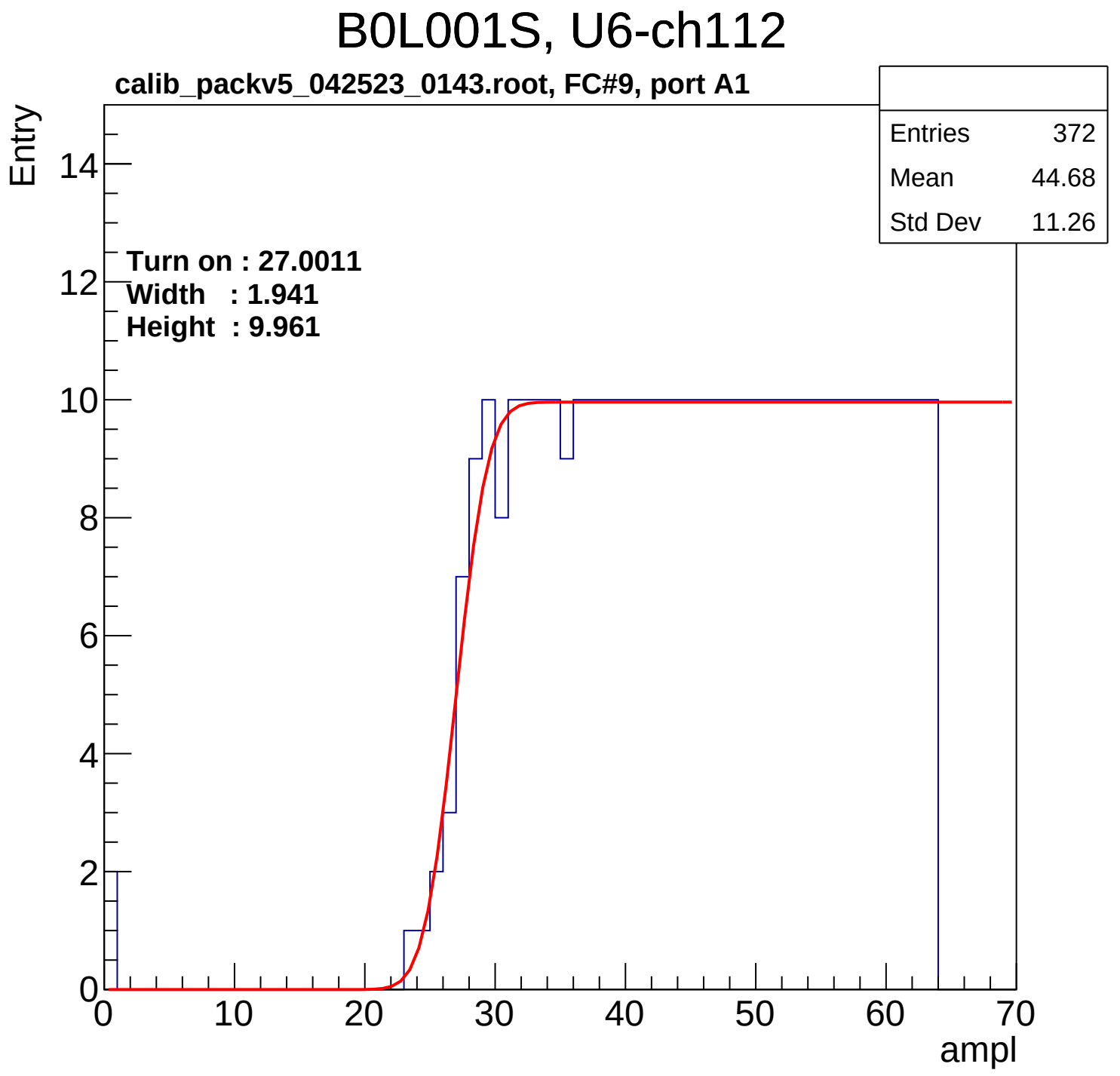
B0L001S, U6-ch112
calib_packv5_042523_0143.root, FC#9, port A1
Entries 372
Mean 44.68
Std Dev 11.26
Turn on : 27.0011
Width : 1.941
Height : 9.961
Entry
ampl
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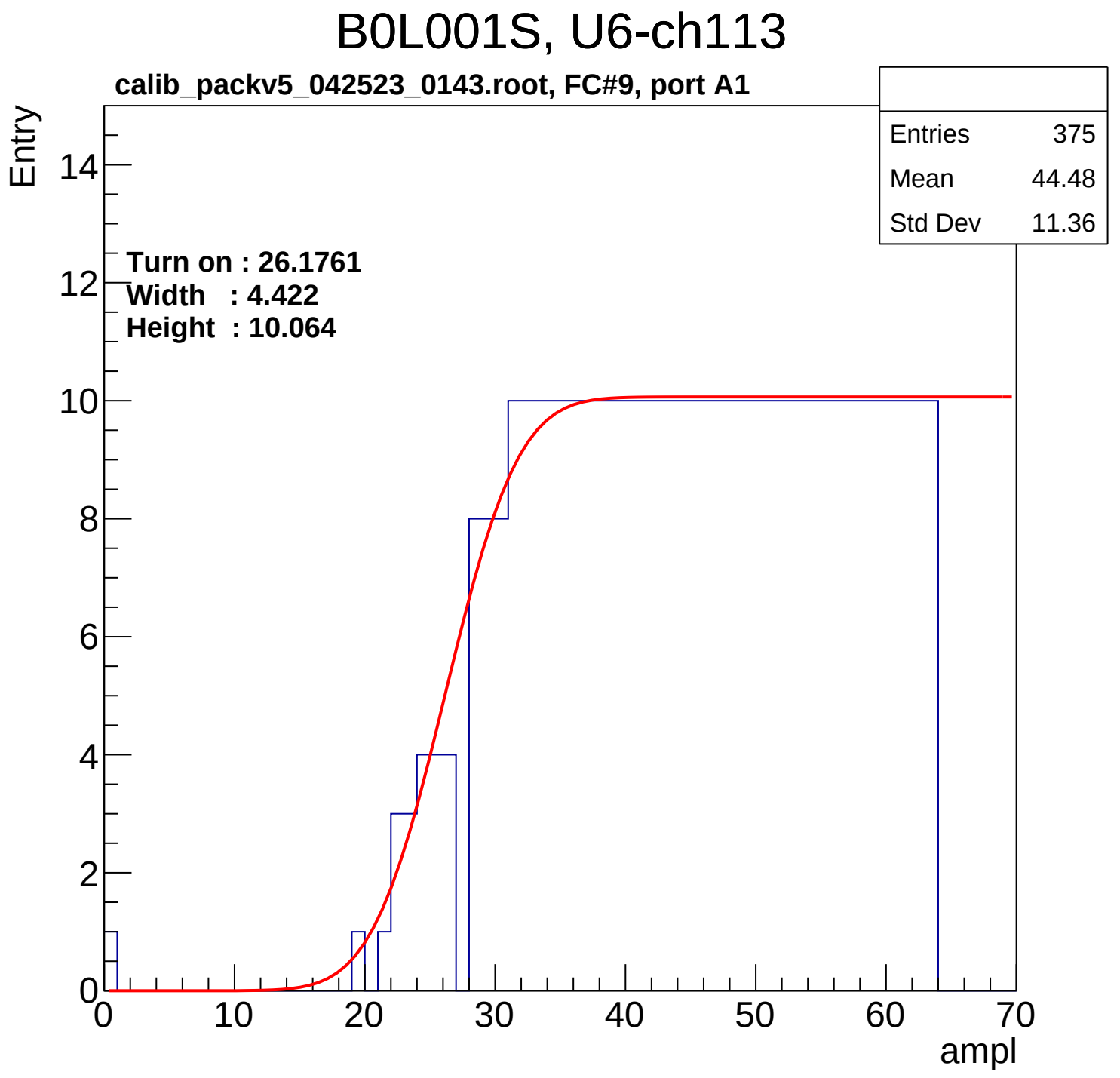
B0L001S, U6-ch113
calib_packv5_042523_0143.root, FC#9, port A1
Entries 375
Mean 44.48
Std Dev 11.36
Turn on : 26.1761
Width : 4.422
Height : 10.064
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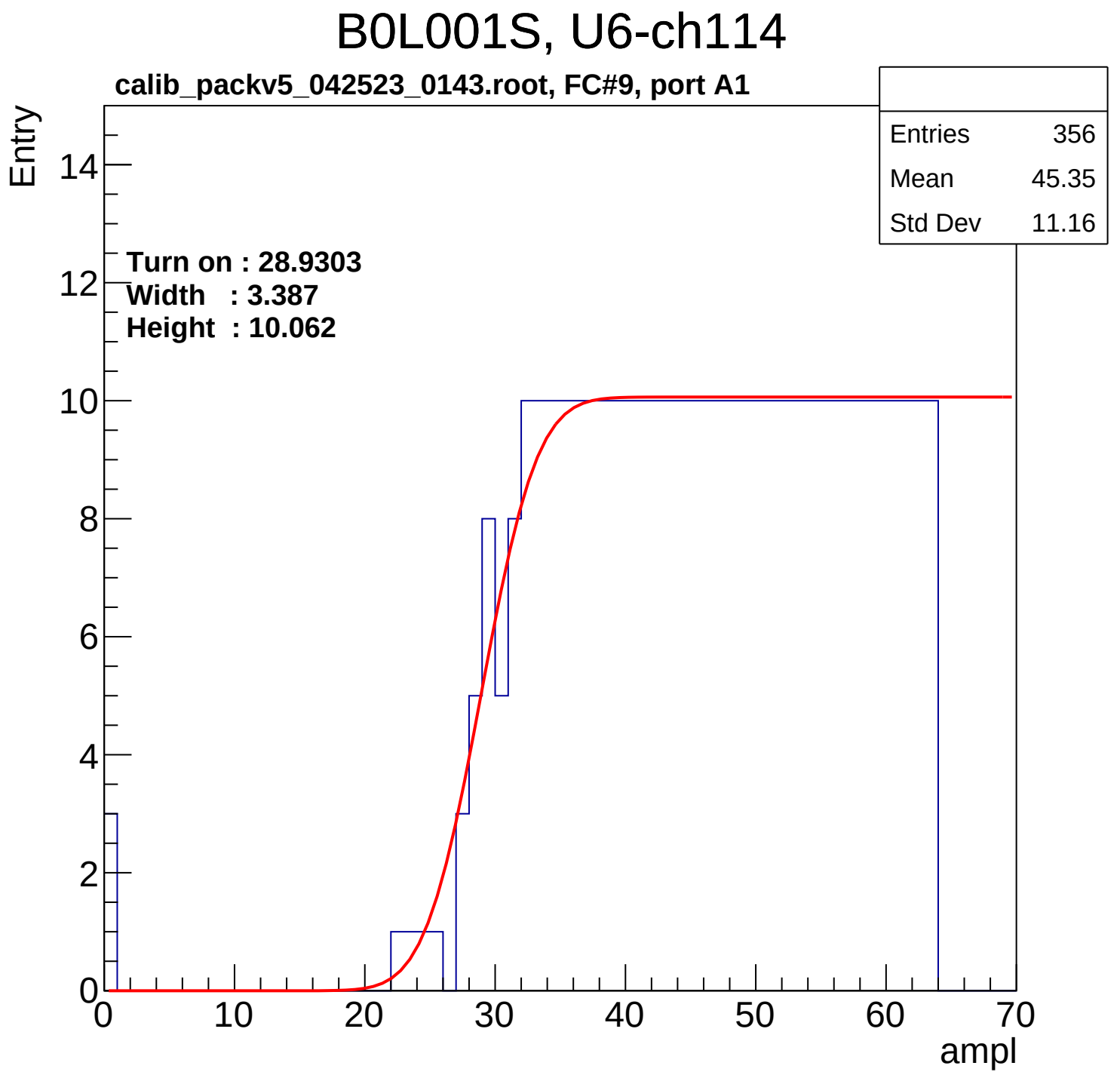
B0L001S, U6-ch114
calib_packv5_042523_0143.root, FC#9, port A1
Entries 356
Mean 45.35
Std Dev 11.16
Turn on : 28.9303
Width : 3.387
Height : 10.062
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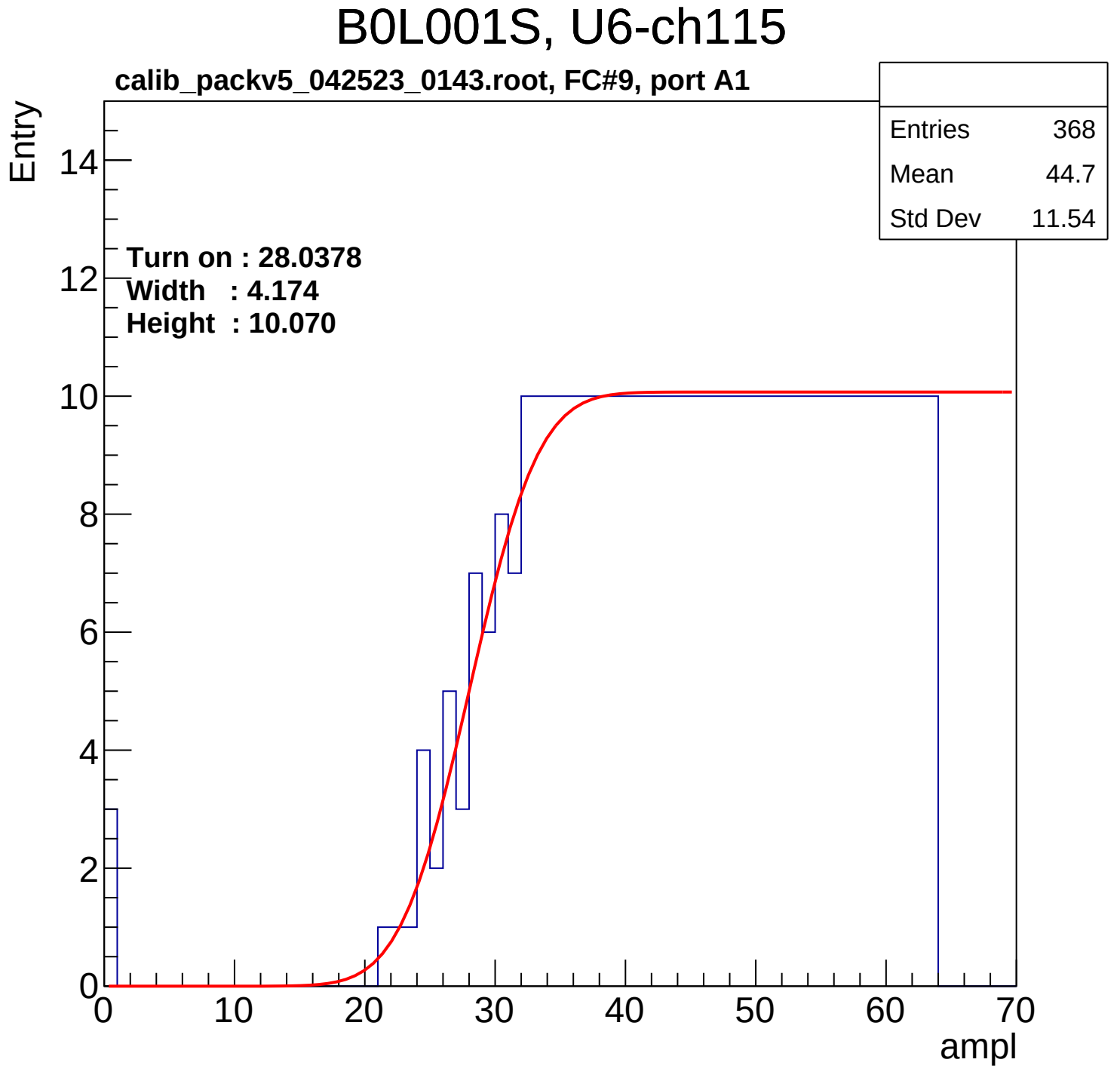
B0L001S, U6-ch115
calib_packv5_042523_0143.root, FC#9, port A1
Entries 368
Mean 44.7
Std Dev 11.54
Turn on : 28.0378
Width : 4.174
Height : 10.070
Entry
ampl
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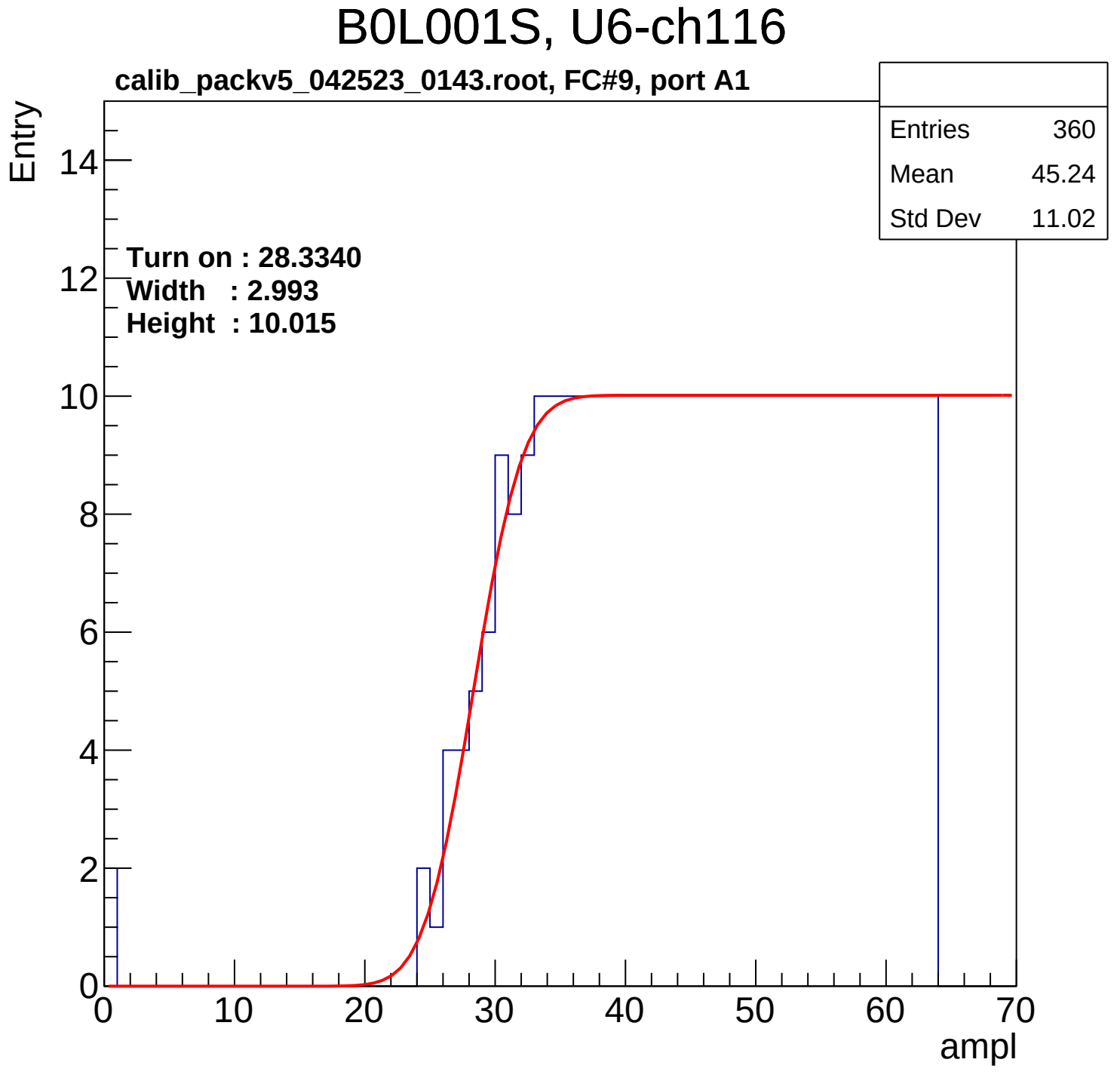
B0L001S, U6-ch116
calib_packv5_042523_0143.root, FC#9, port A1
Entries 360
Mean 45.24
Std Dev 11.02
Turn on : 28.3340
Width : 2.993
Height : 10.015
Entry
ampl
0
2
4
6
8
10
12
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0
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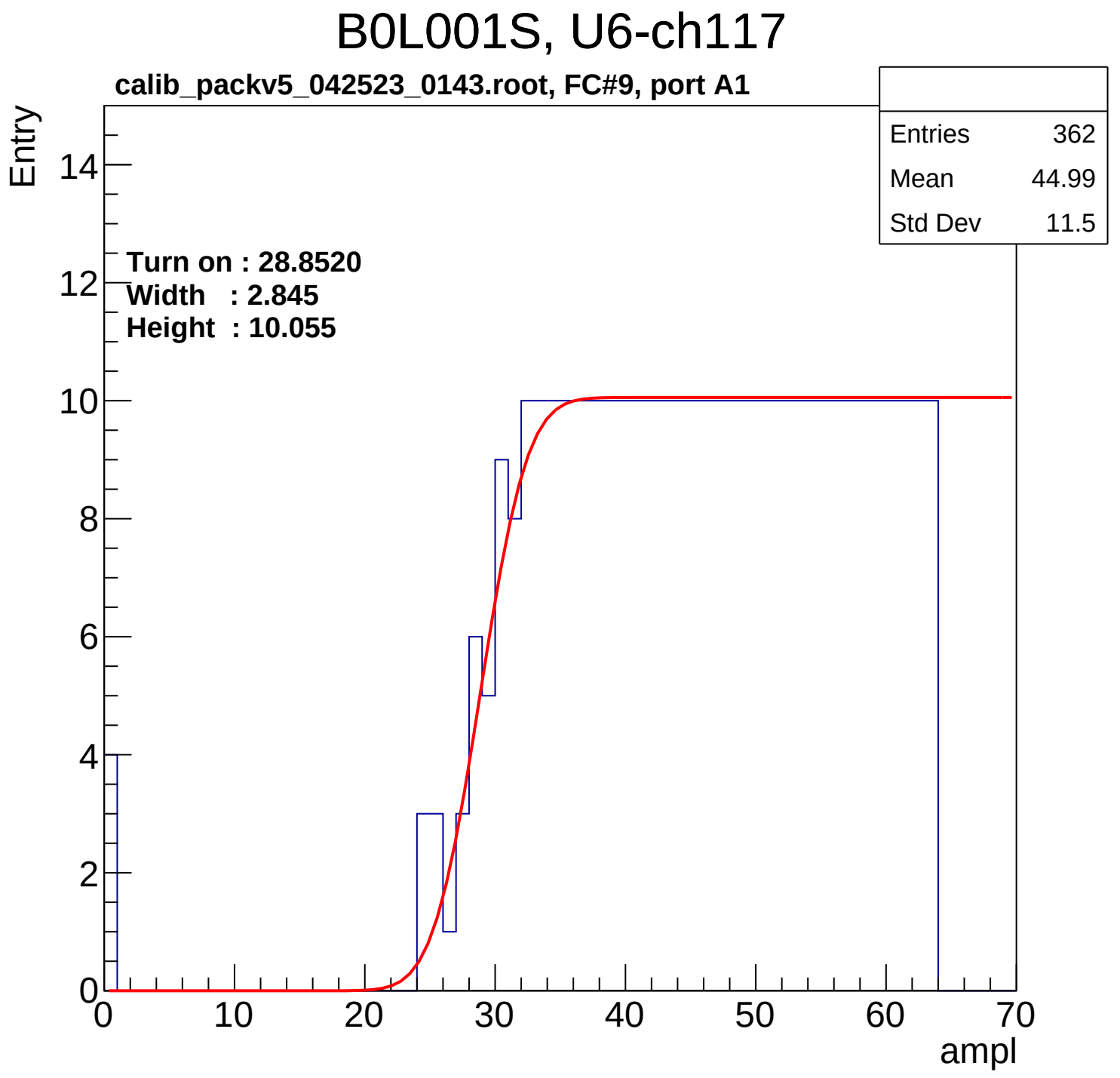
B0L001S, U6-ch117
calib_packv5_042523_0143.root, FC#9, port A1
Entries 362
Mean 44.99
Std Dev 11.5
Turn on : 28.8520
Width : 2.845
Height : 10.055
Entry
ampl
0
2
4
6
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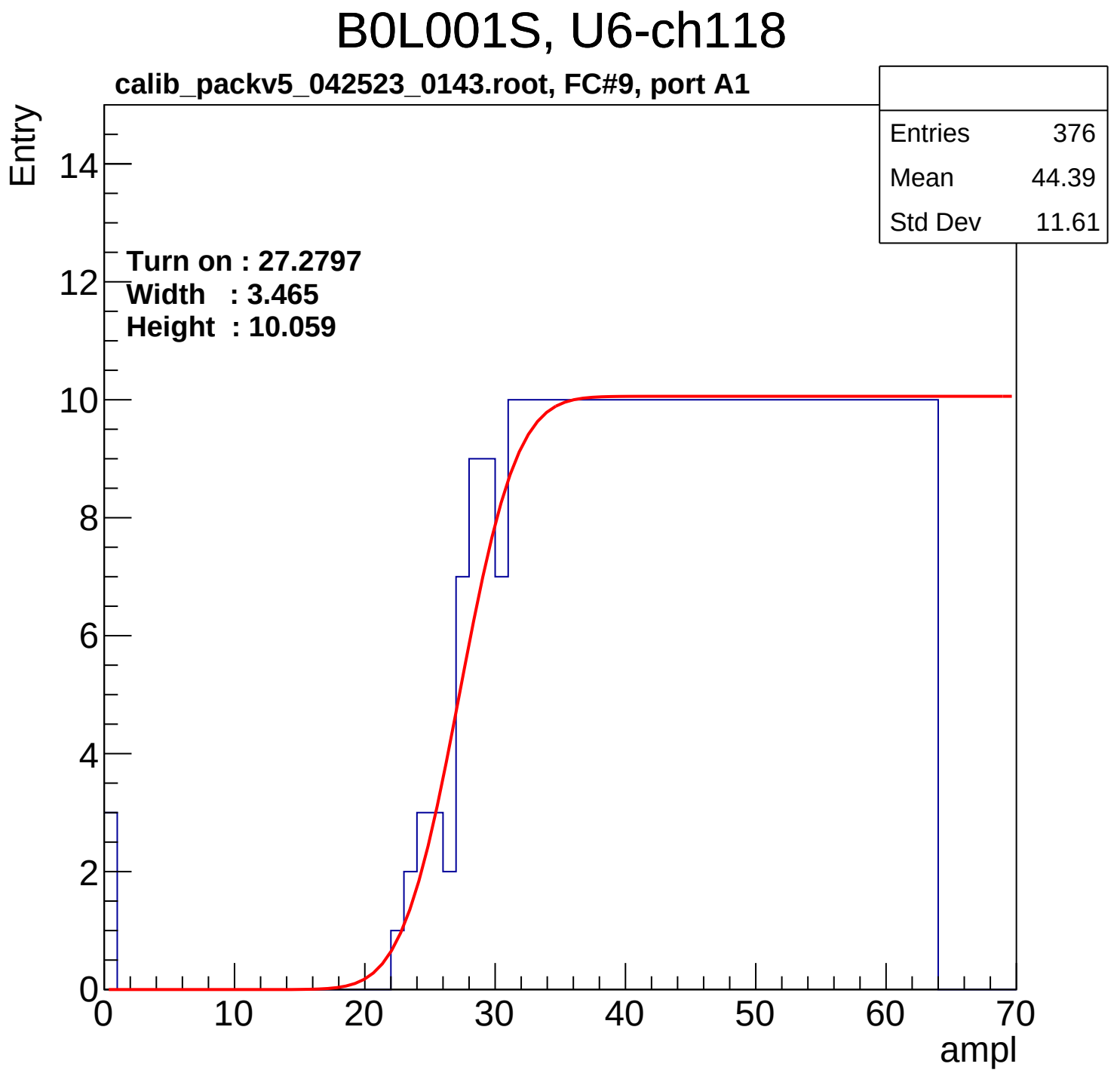
B0L001S, U6-ch118
calib_packv5_042523_0143.root, FC#9, port A1
Entries 376
Mean 44.39
Std Dev 11.61
Turn on : 27.2797
Width : 3.465
Height : 10.059
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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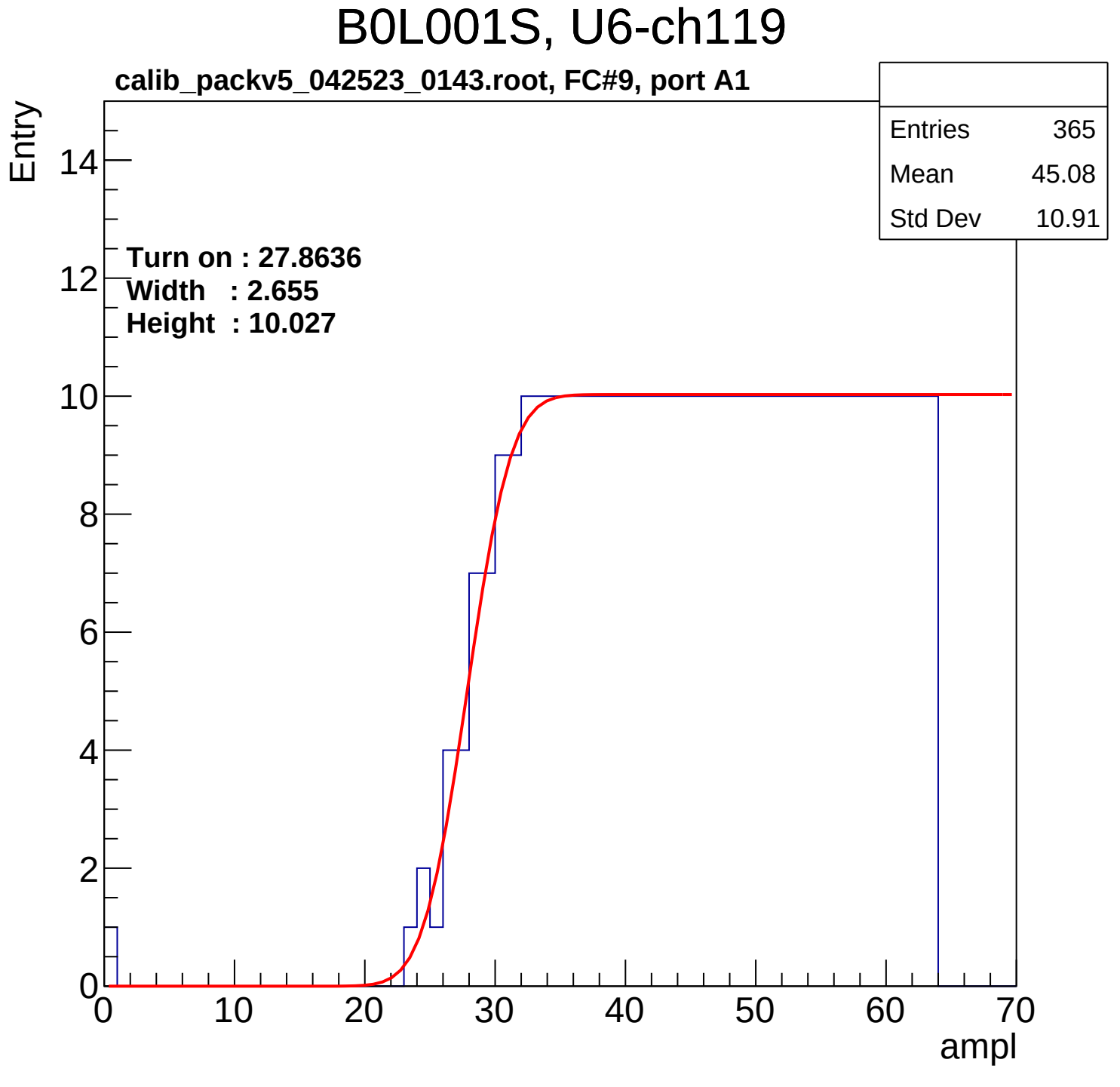
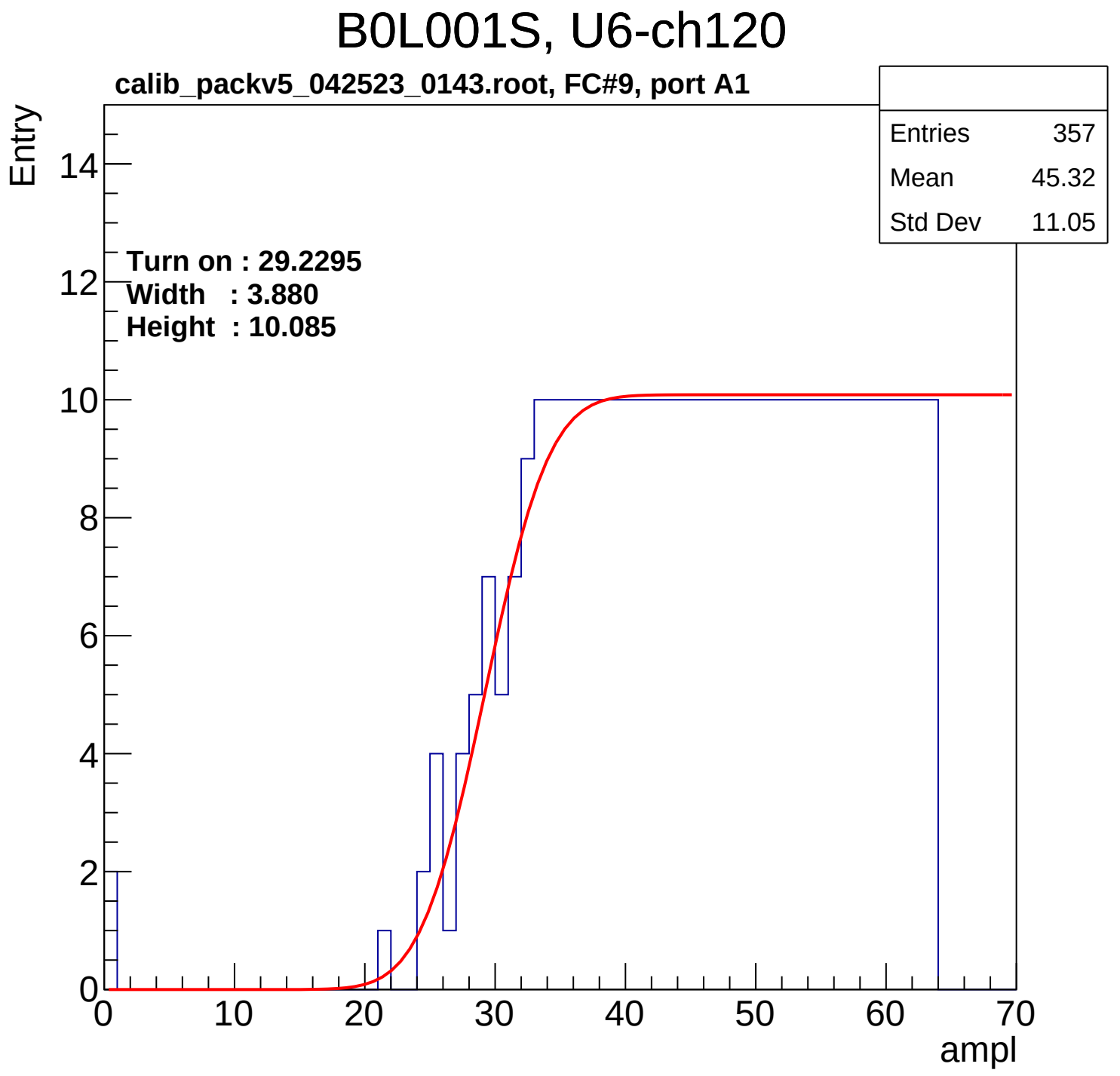

B0L001S, U6-ch119
calib_packv5_042523_0143.root, FC#9, port A1
Entries 365
Mean 45.08
Std Dev 10.91
Turn on : 27.8636
Width : 2.655
Height : 10.027
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L001S, U6-ch120
calib_packv5_042523_0143.root, FC#9, port A1
Entries 357
Mean 45.32
Std Dev 11.05
Turn on : 29.2295
Width : 3.880
Height : 10.085
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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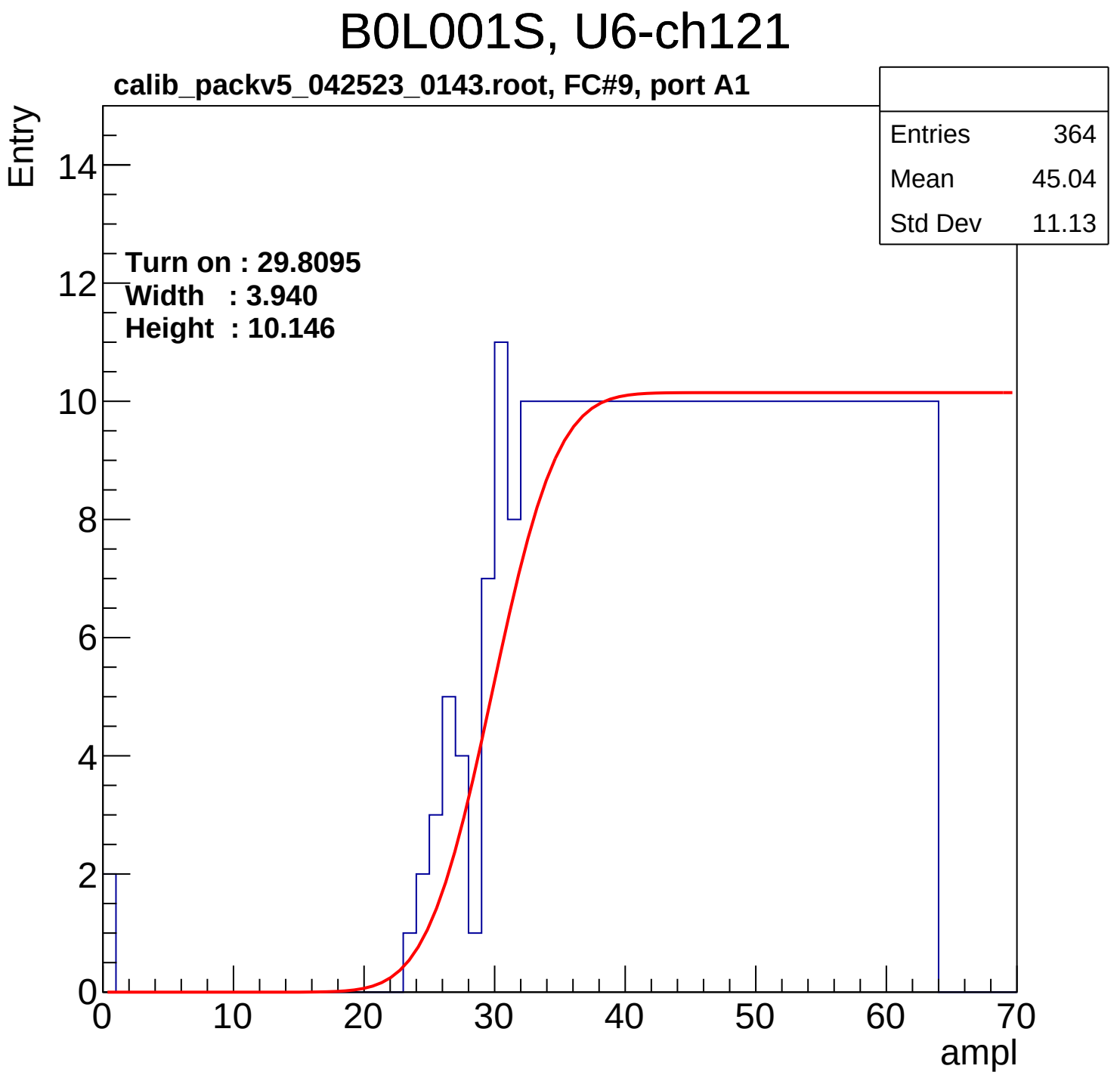
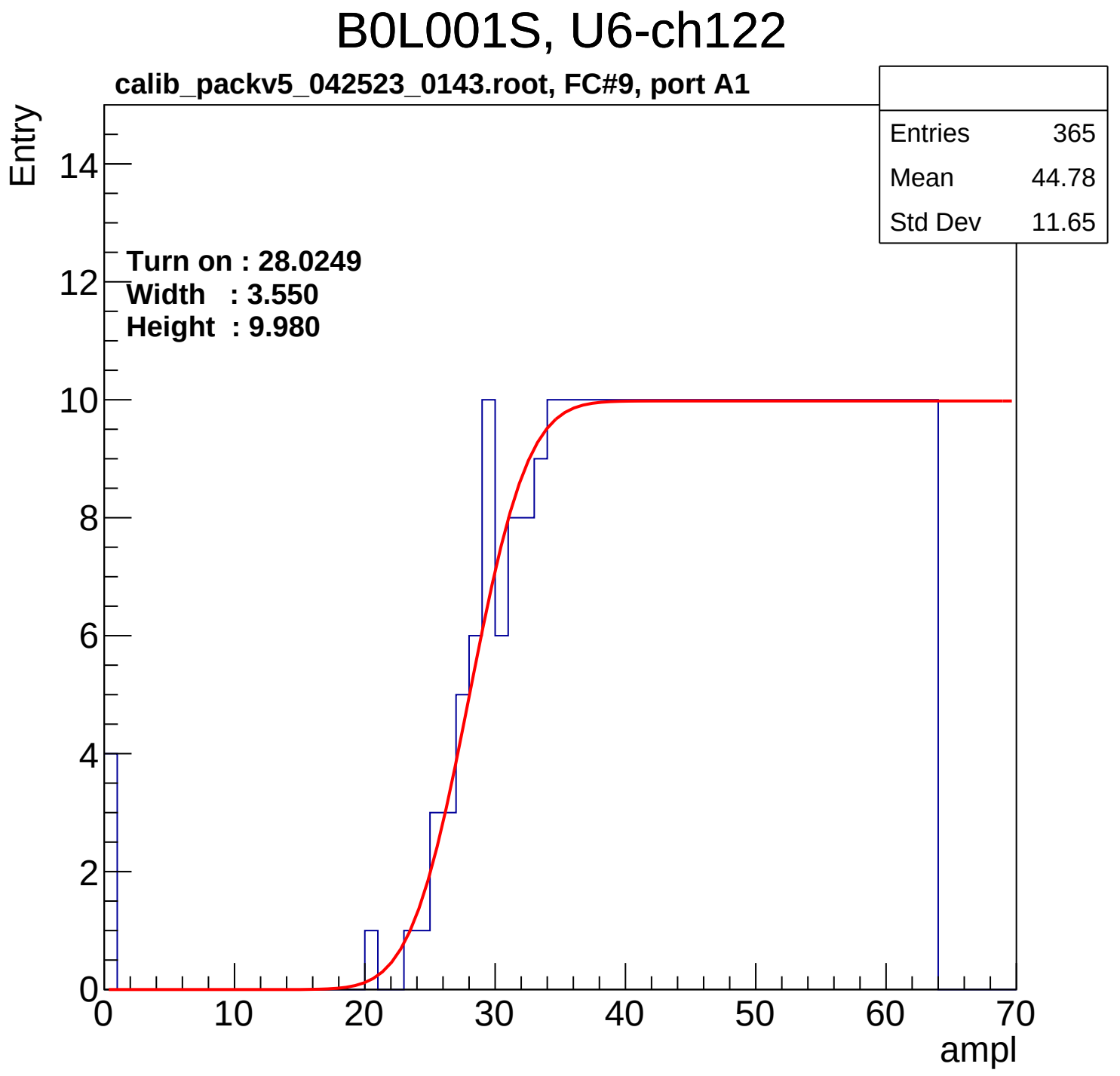

B0L001S, U6-ch121
calib_packv5_042523_0143.root, FC#9, port A1
Entries 364
Mean 45.04
Std Dev 11.13
Turn on : 29.8095
Width : 3.940
Height : 10.146
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L001S, U6-ch122
calib_packv5_042523_0143.root, FC#9, port A1
Entries 365
Mean 44.78
Std Dev 11.65
Turn on : 28.0249
Width : 3.550
Height : 9.980
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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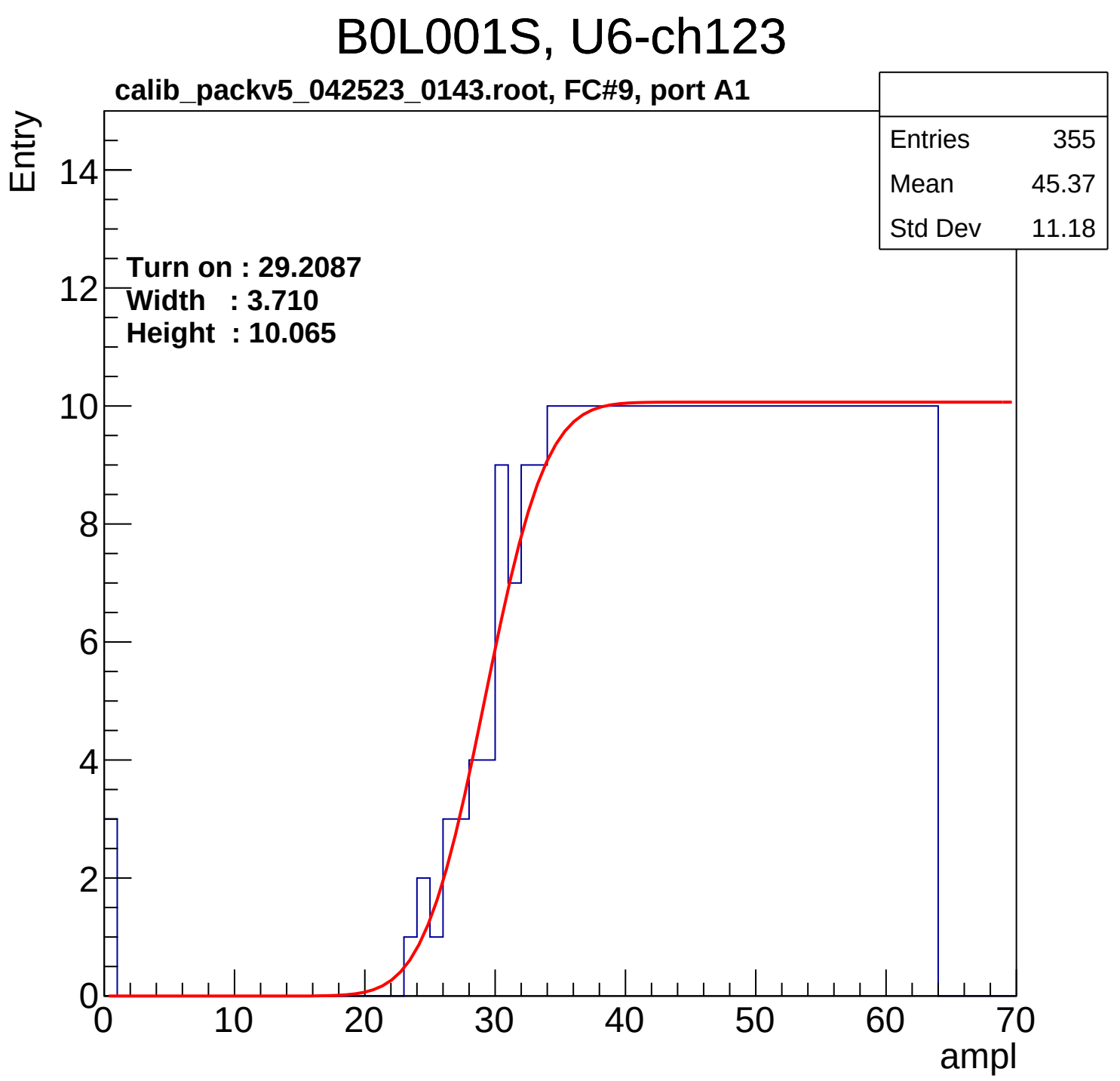
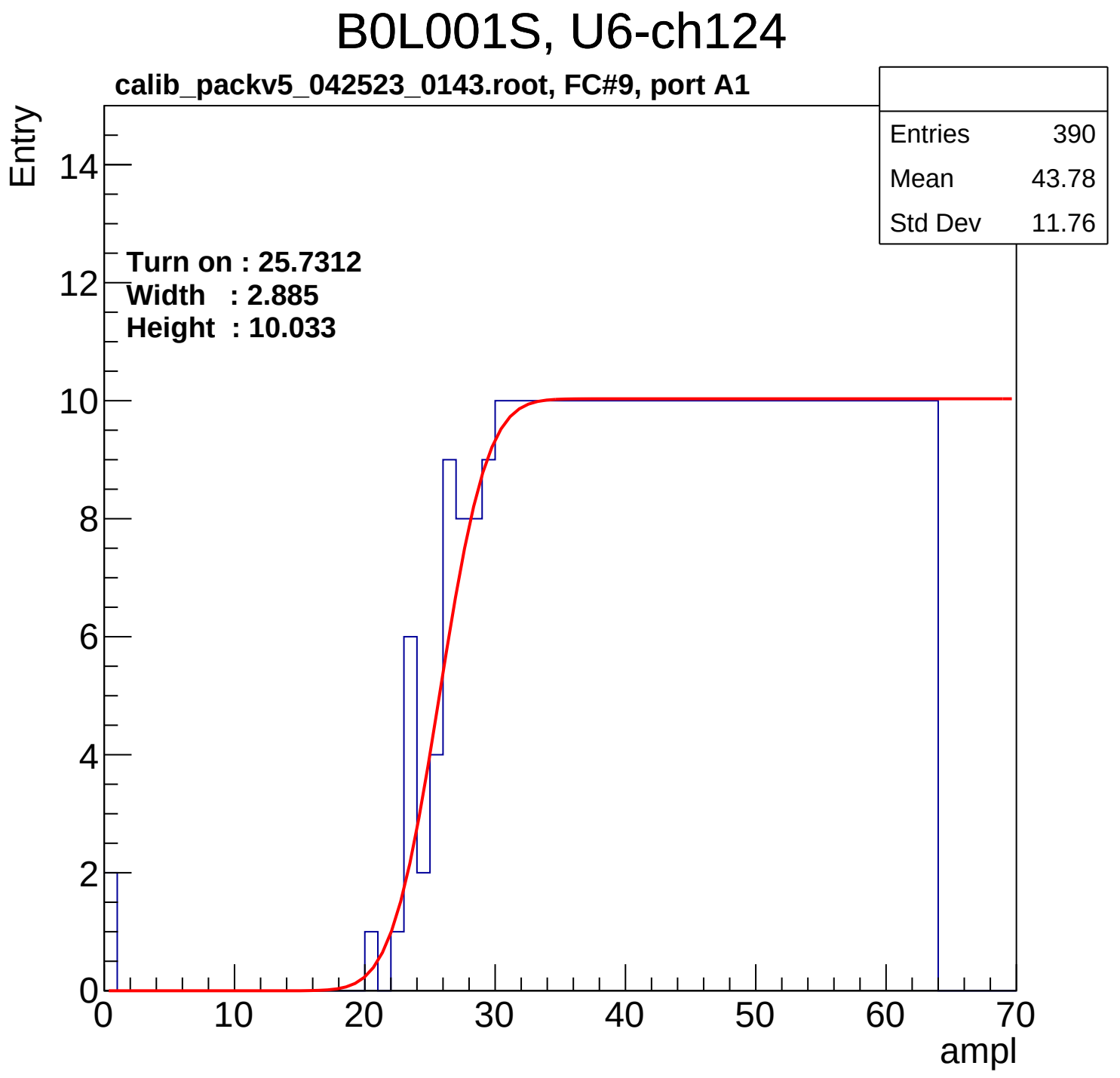
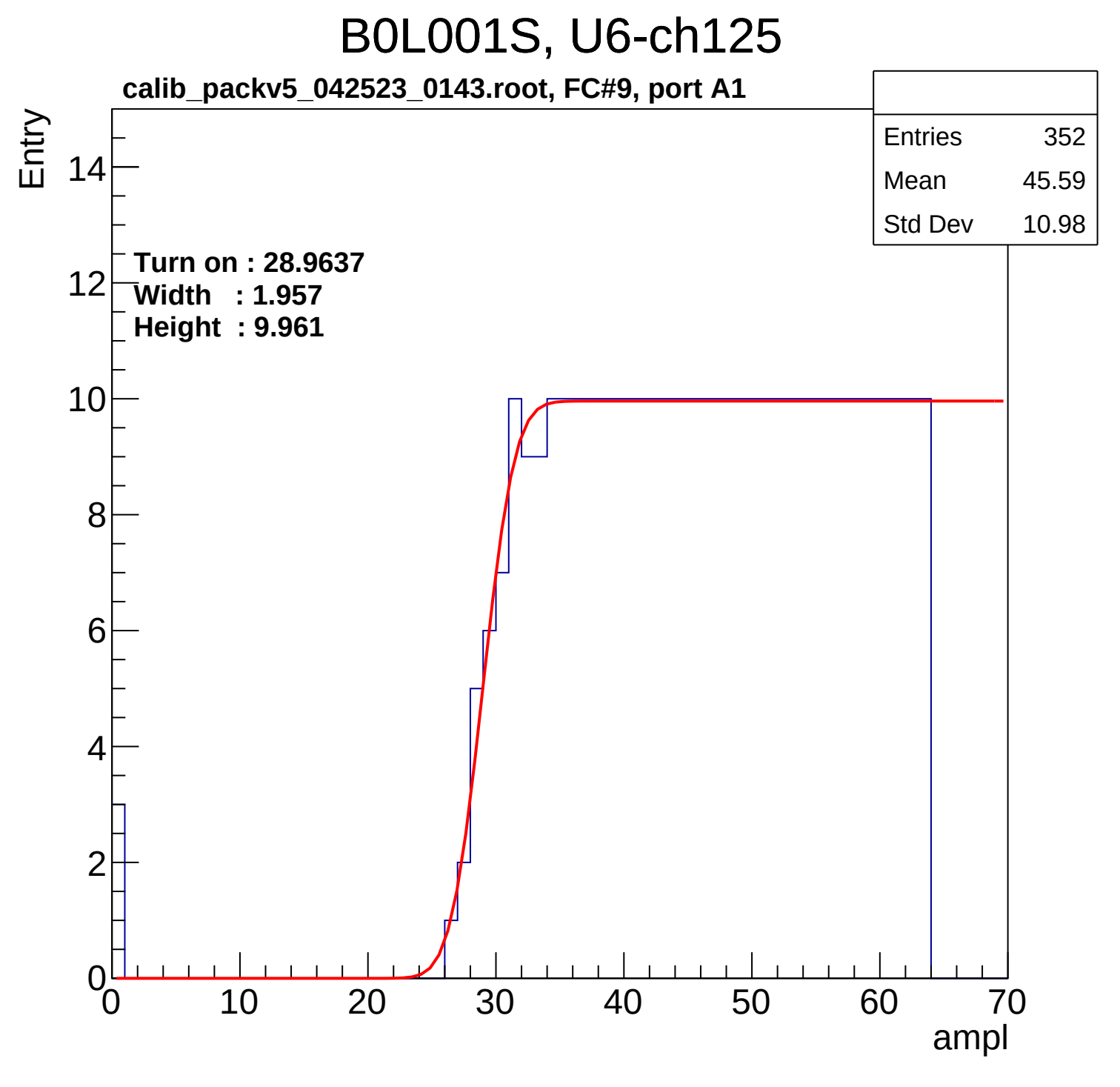
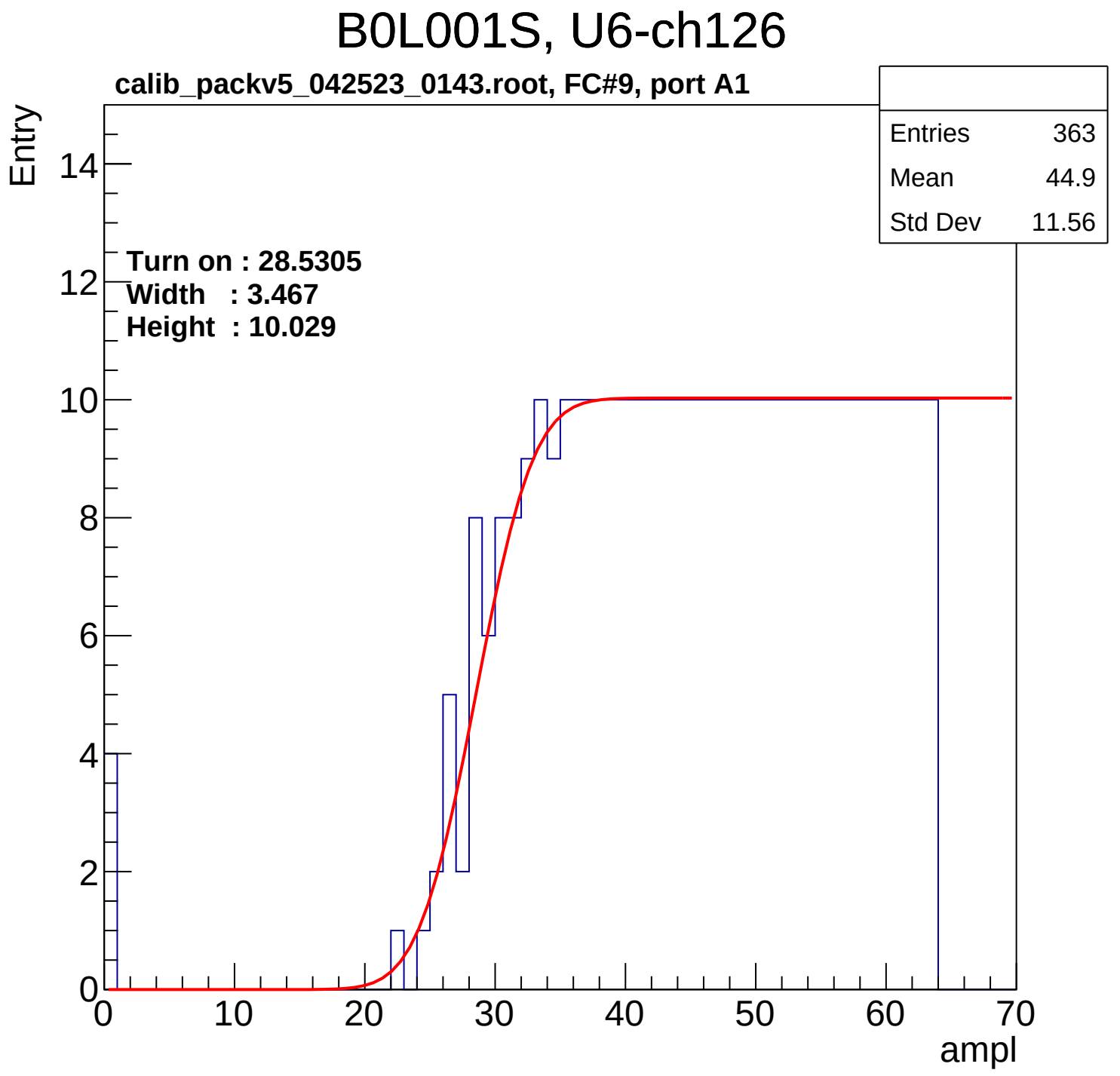

B0L001S, U6-ch123
calib_packv5_042523_0143.root, FC#9, port A1
Entries 355
Mean 45.37
Std Dev 11.18
Turn on : 29.2087
Width : 3.710
Height : 10.065
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L001S, U6-ch124
calib_packv5_042523_0143.root, FC#9, port A1
Entries 390
Mean 43.78
Std Dev 11.76
Turn on : 25.7312
Width : 2.885
Height : 10.033
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L001S, U6-ch125
calib_packv5_042523_0143.root, FC#9, port A1
Entries 352
Mean 45.59
Std Dev 10.98
Turn on : 28.9637
Width : 1.957
Height : 9.961
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L001S, U6-ch126
calib_packv5_042523_0143.root, FC#9, port A1
Entries 363
Mean 44.9
Std Dev 11.56
Turn on : 28.5305
Width : 3.467
Height : 10.029
Entry
ampl
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2
4
6
8
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0
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60
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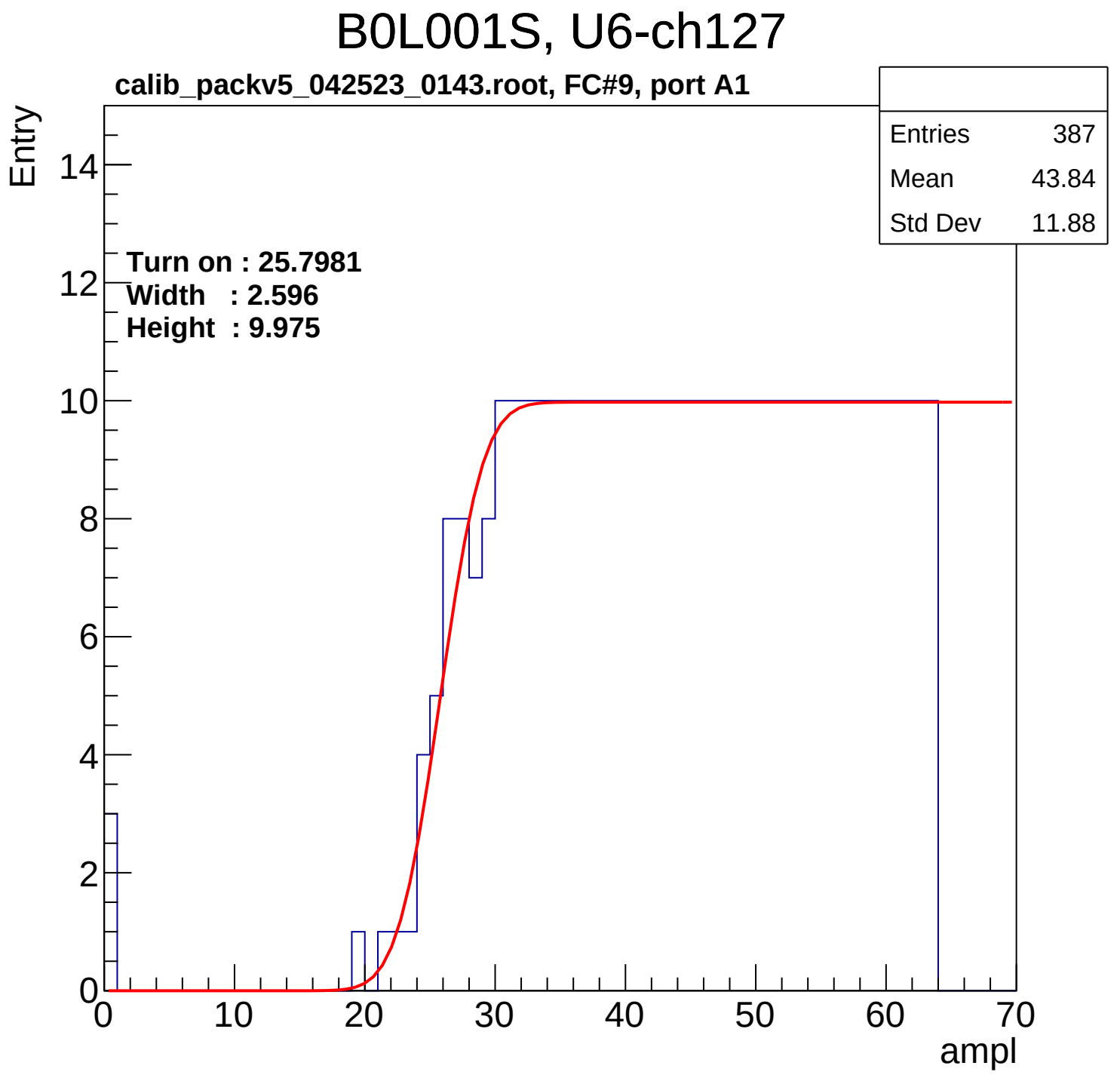
B0L001S, U6-ch127
calib_packv5_042523_0143.root, FC#9, port A1
Entries 387
Mean 43.84
Std Dev 11.88
Turn on : 25.7981
Width : 2.596
Height : 9.975
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
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60
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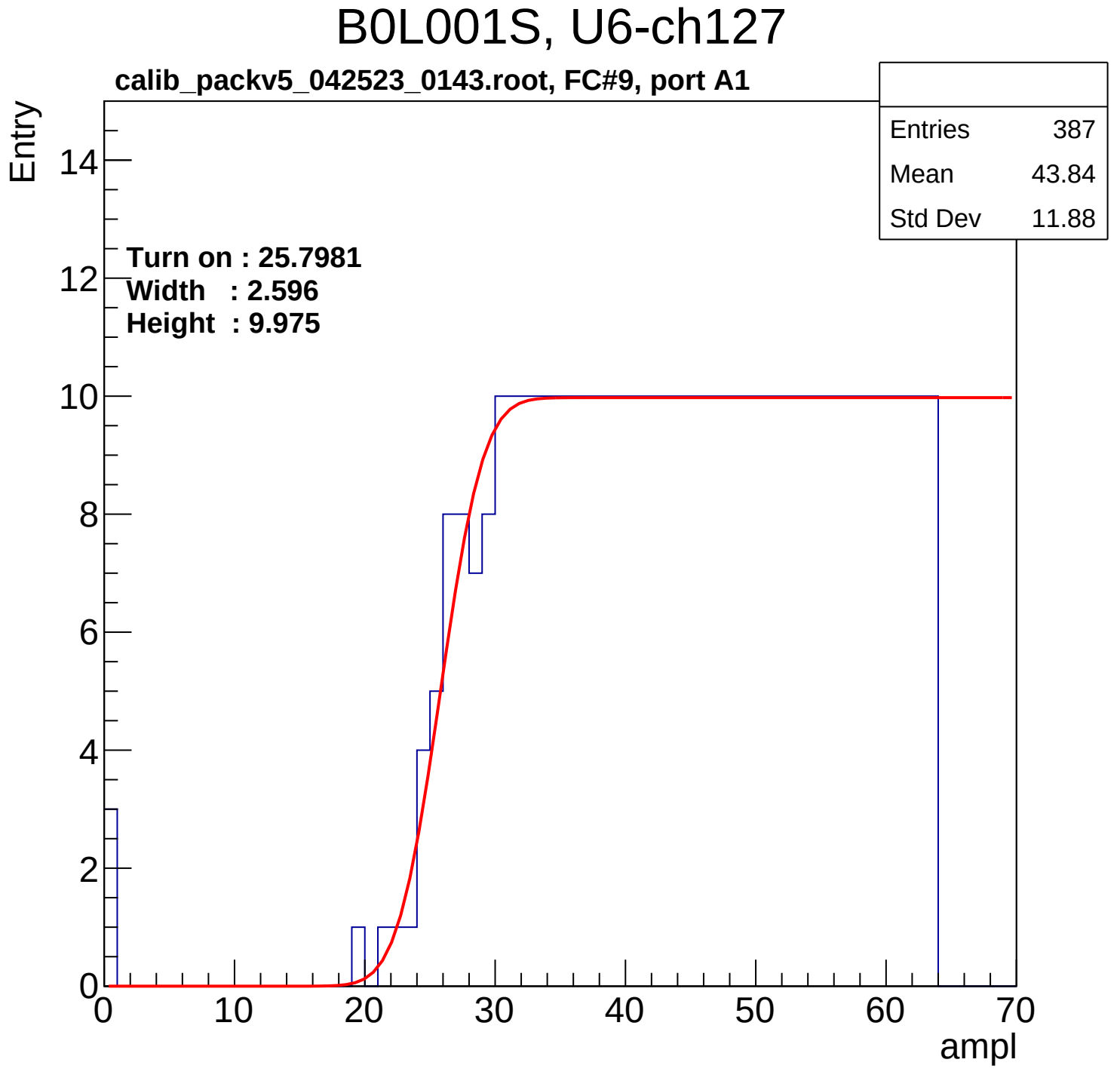
B0L001S, U6-ch127
calib_packv5_042523_0143.root, FC#9, port A1
Entries 387
Mean 43.84
Std Dev 11.88
Turn on : 25.7981
Width : 2.596
Height : 9.975
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70