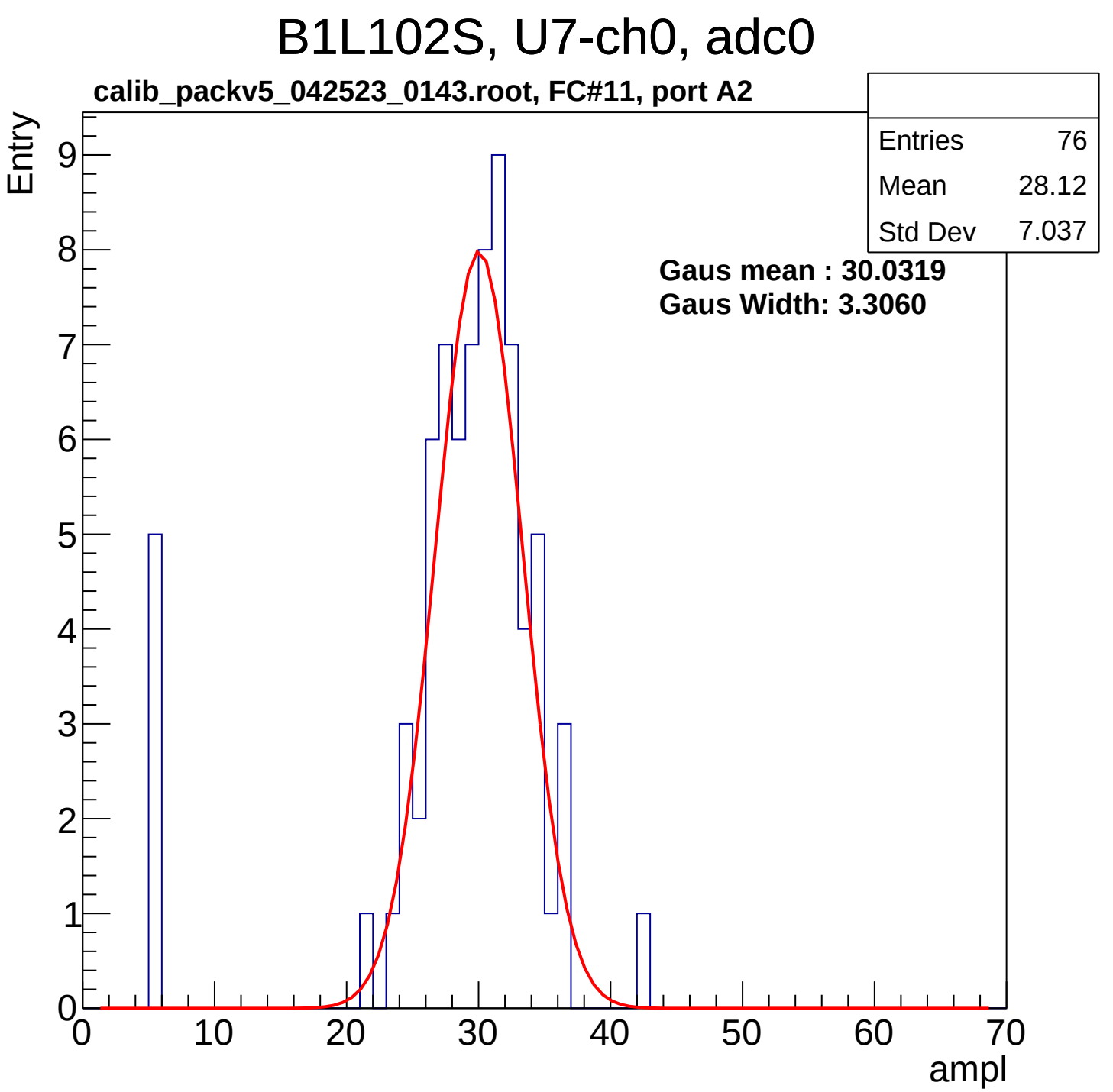
B1L102S, U7-ch0, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 76
Mean 28.12
Std Dev 7.037
Gaus mean : 30.0319
Gaus Width: 3.3060
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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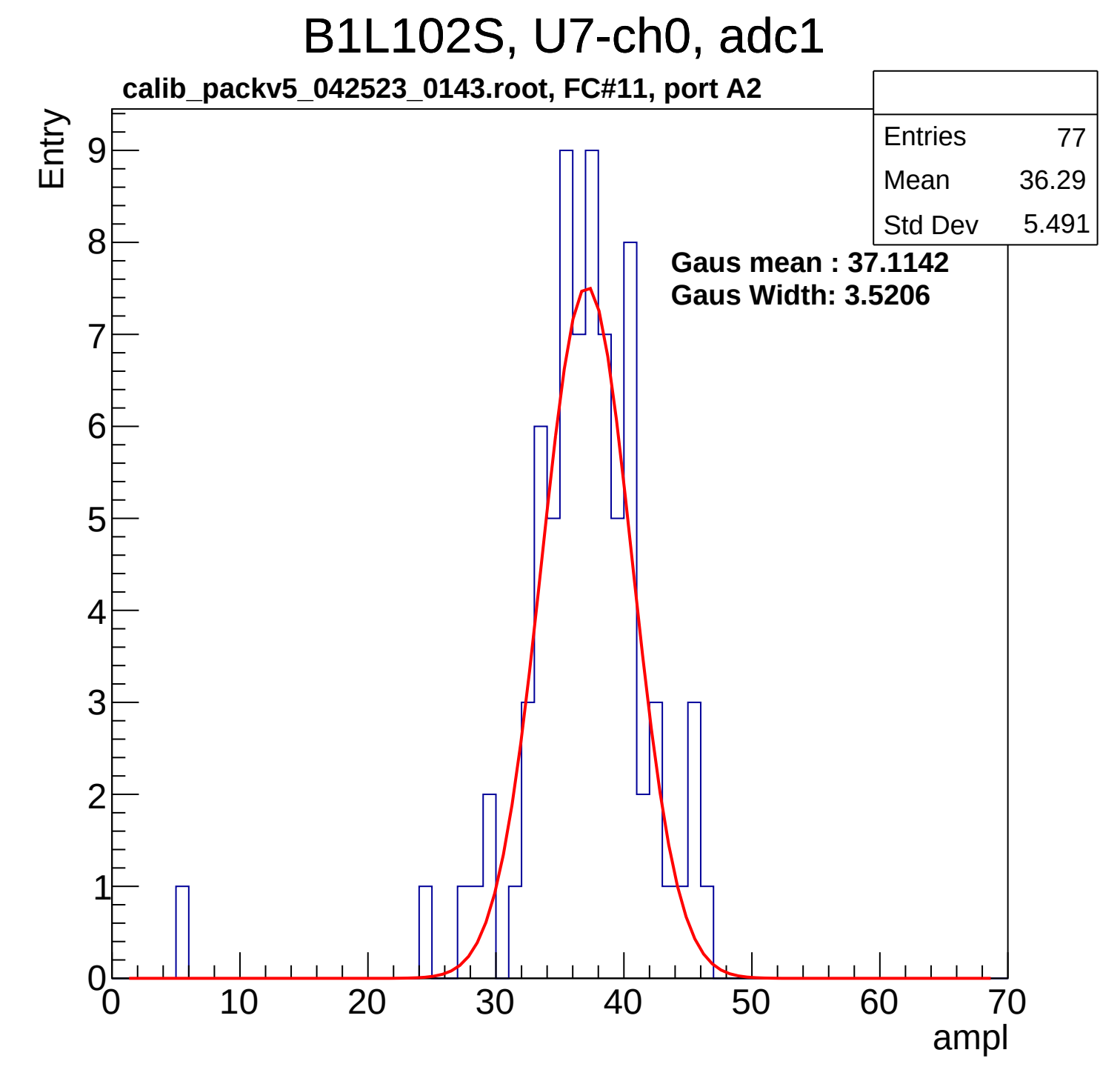
B1L102S, U7-ch0, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 77
Mean 36.29
Std Dev 5.491
Gaus mean : 37.1142
Gaus Width: 3.5206
Entry
ampl
0
1
2
3
4
5
6
7
8
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0
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40
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60
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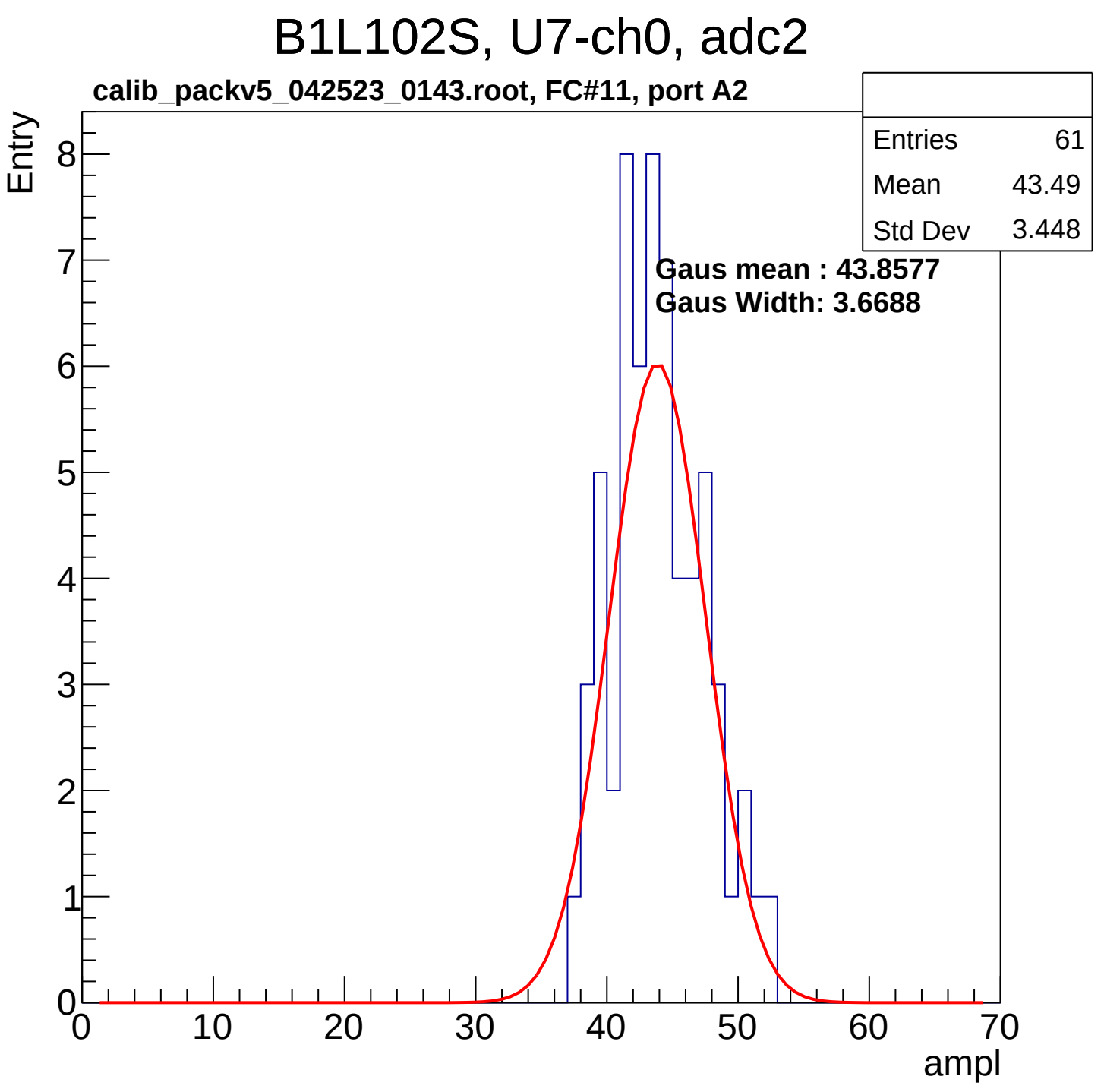
B1L102S, U7-ch0, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 61
Mean 43.49
Std Dev 3.448
Gaus mean : 43.8577
Gaus Width: 3.6688
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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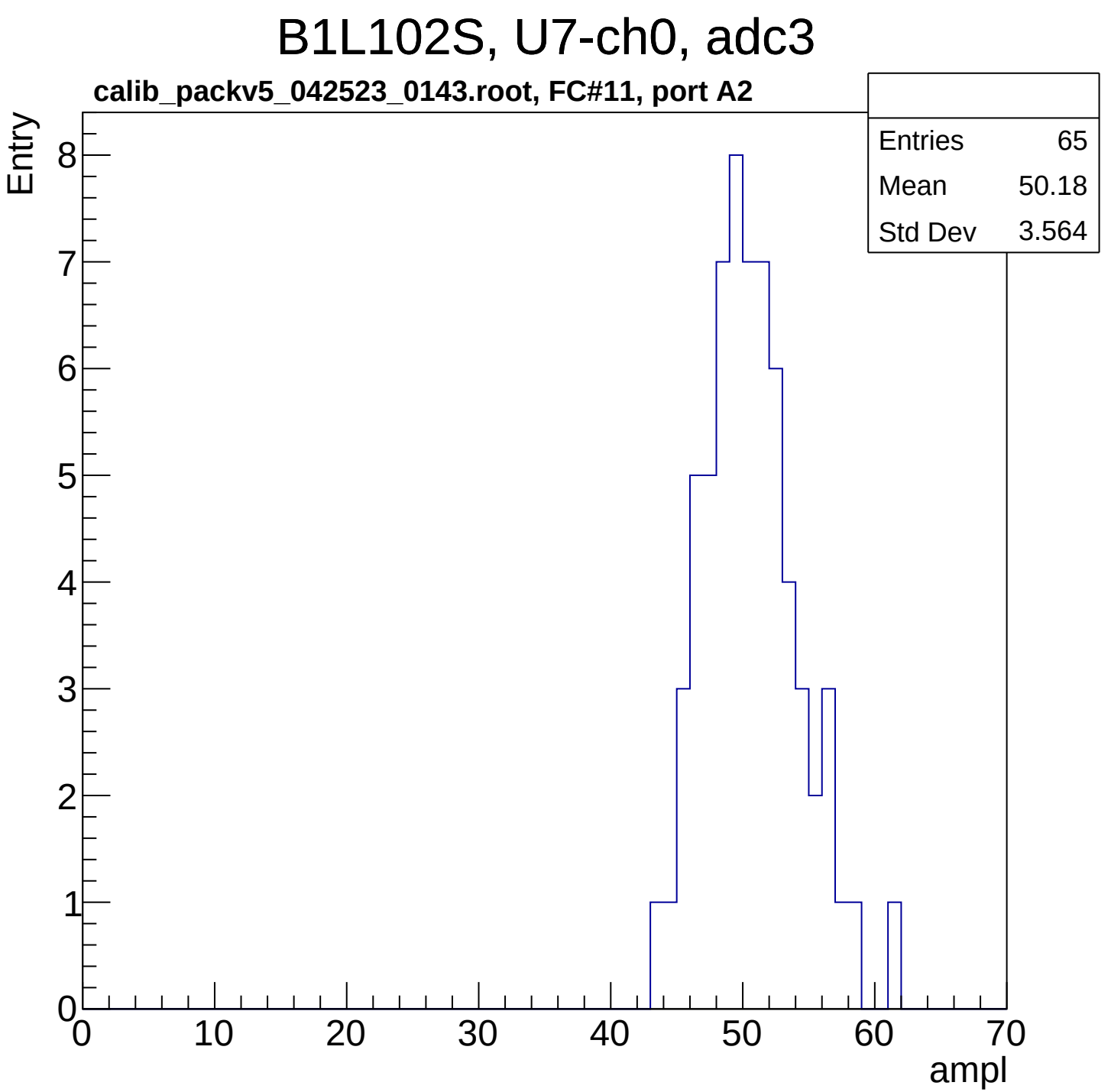
B1L102S, U7-ch0, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 65
Mean 50.18
Std Dev 3.564
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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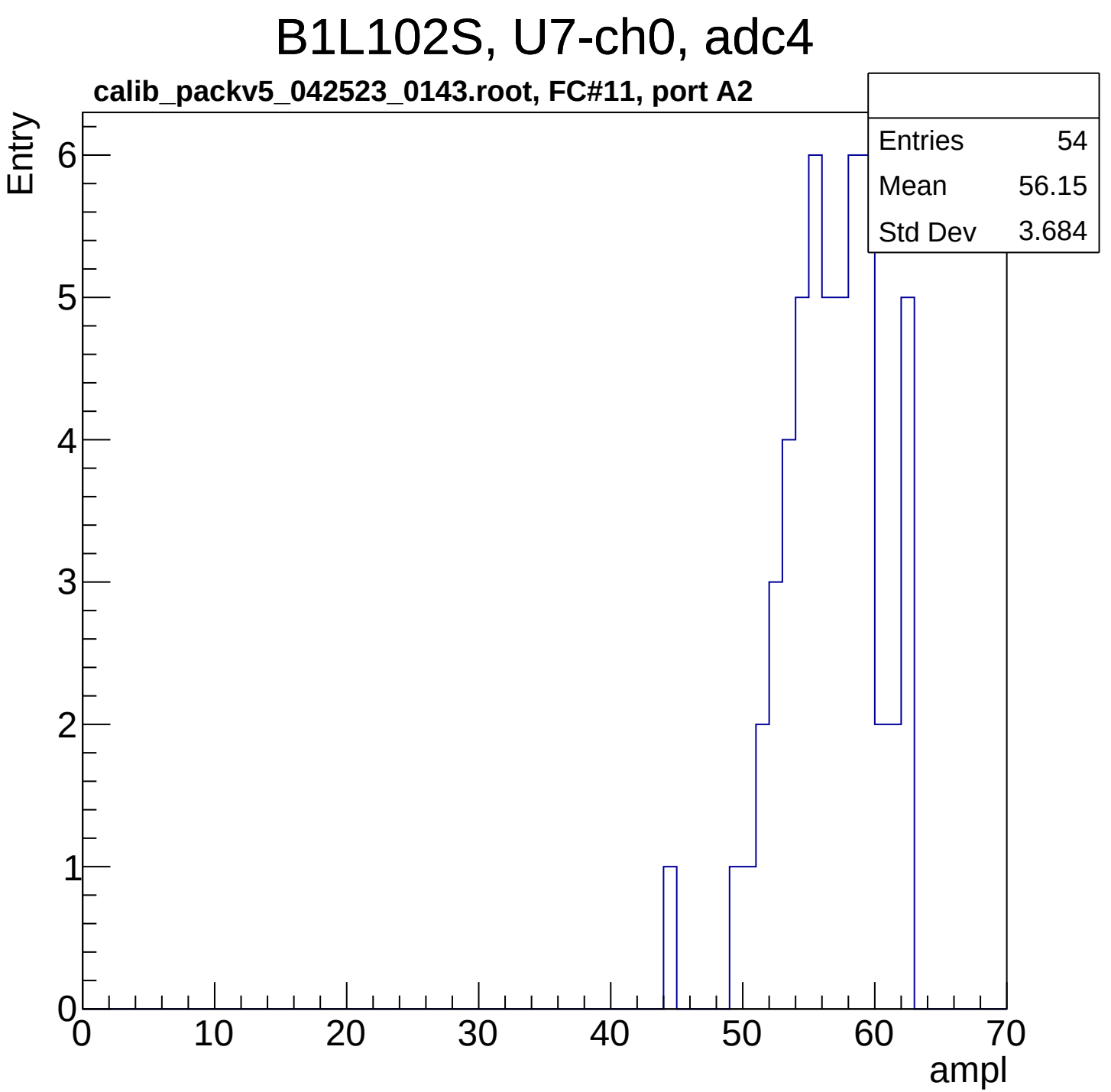
B1L102S, U7-ch0, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 54
Mean 56.15
Std Dev 3.684
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
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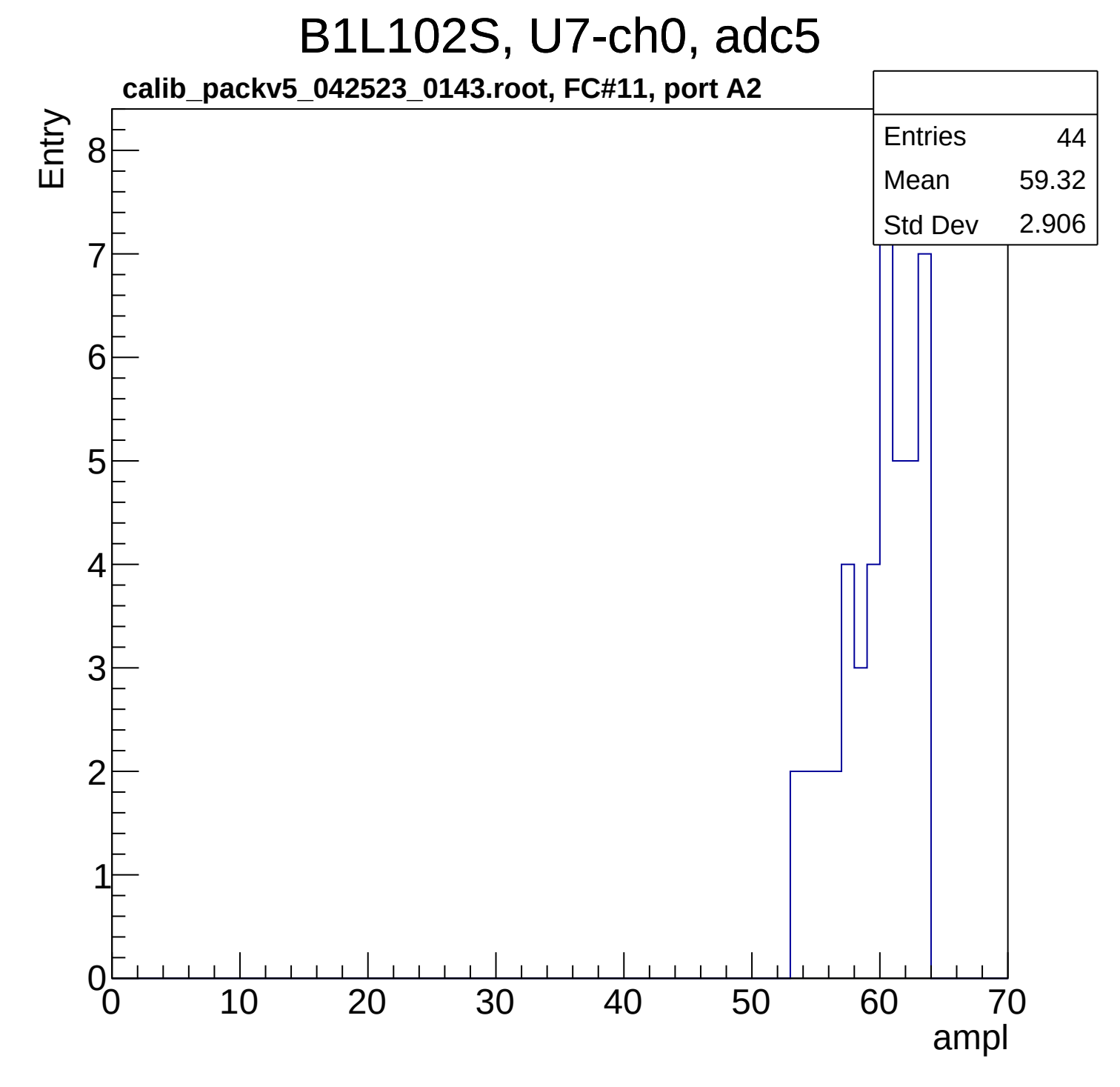
B1L102S, U7-ch0, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 44
Mean 59.32
Std Dev 2.906
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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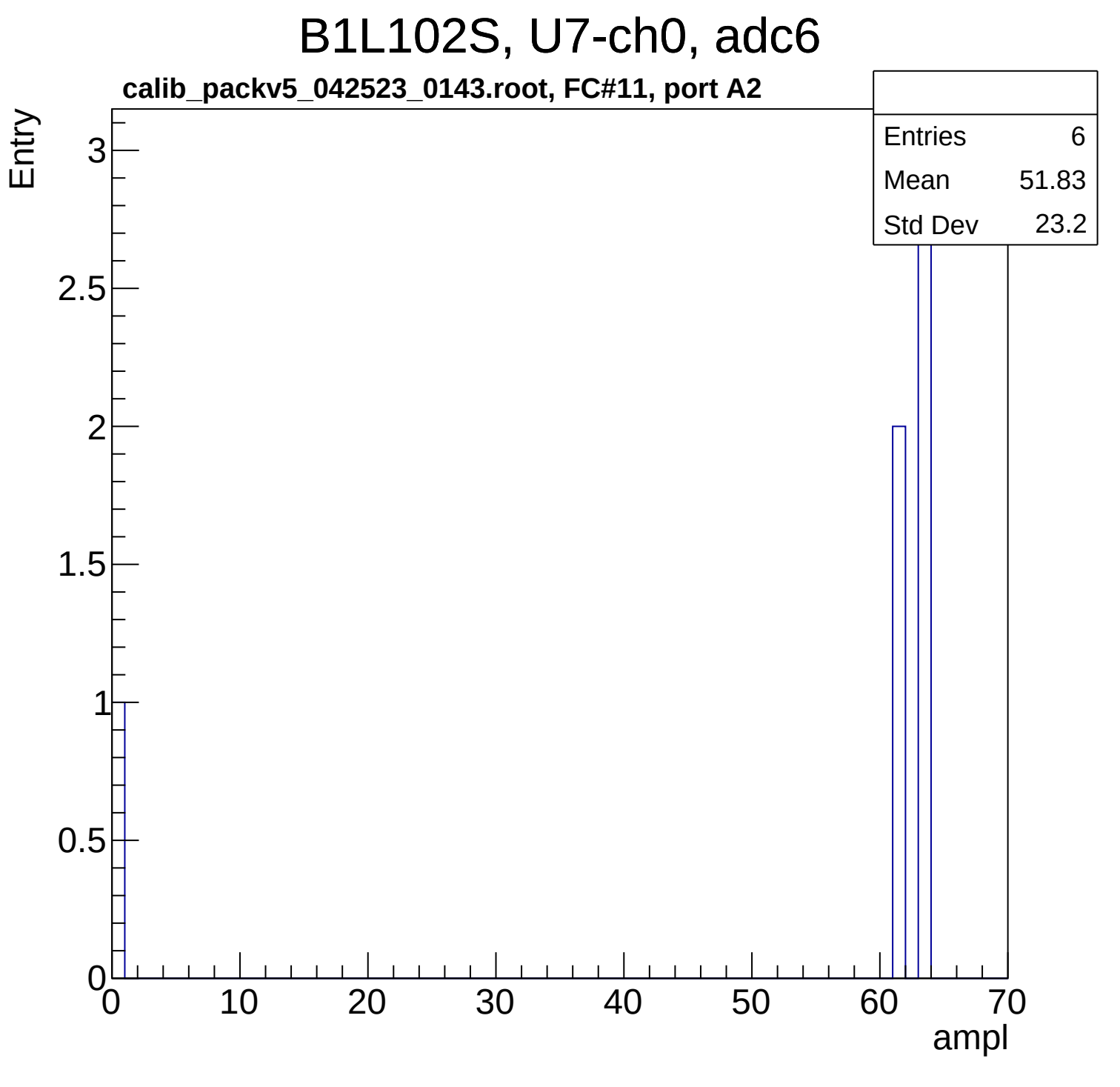
B1L102S, U7-ch0, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 6
Mean 51.83
Std Dev 23.2
Entry
ampl
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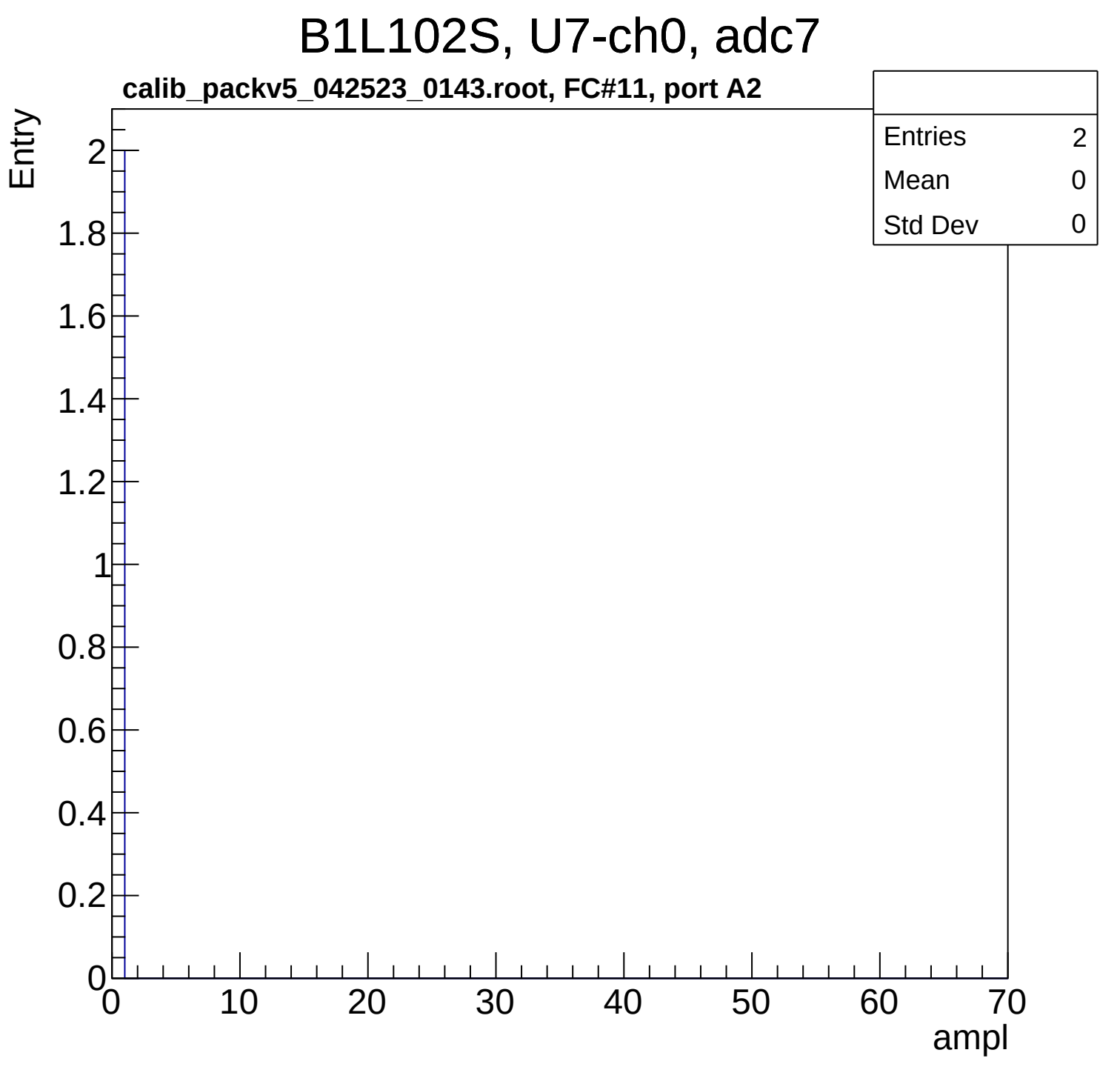
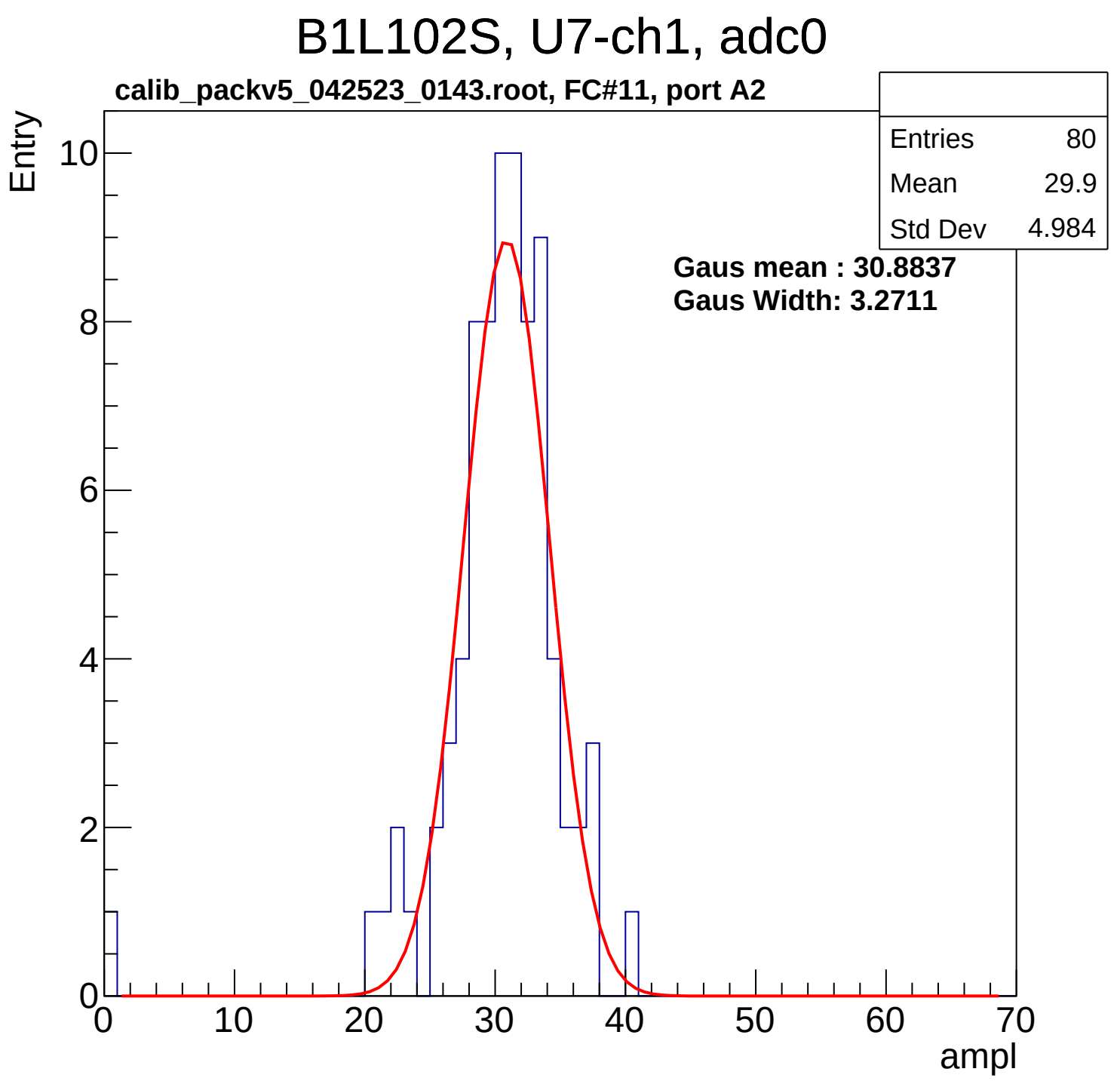
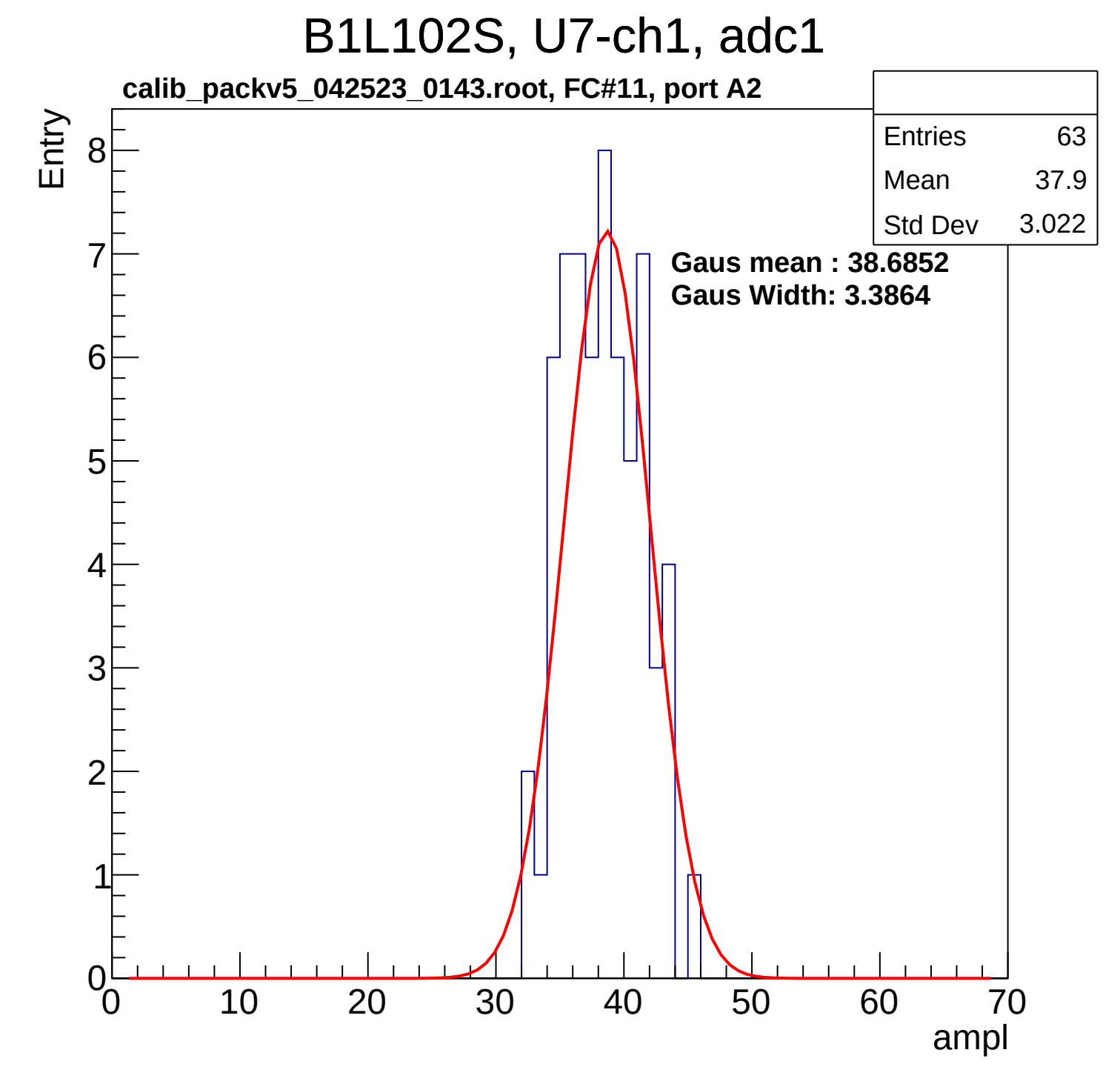
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L102S, U7-ch0, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 2
Mean 0
Std Dev 0
Entry
2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U7-ch1, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 80
Mean 29.9
Std Dev 4.984
Gaus mean : 30.8837
Gaus Width: 3.2711
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L102S, U7-ch1, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 63
Mean 37.9
Std Dev 3.022
Gaus mean : 38.6852
Gaus Width: 3.3864
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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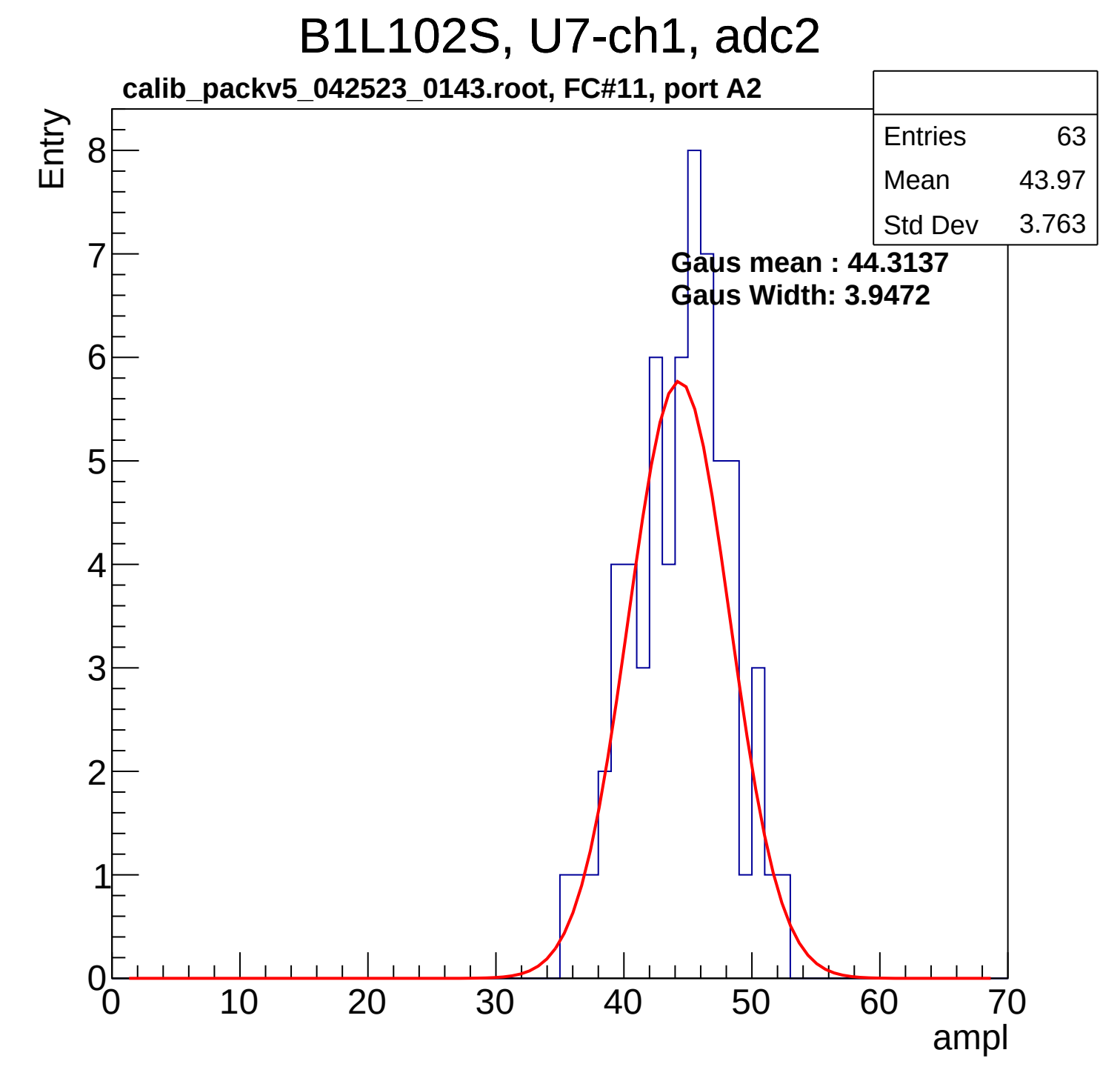
B1L102S, U7-ch1, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 63
Mean 43.97
Std Dev 3.763
Gaus mean : 44.3137
Gaus Width: 3.9472
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
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60
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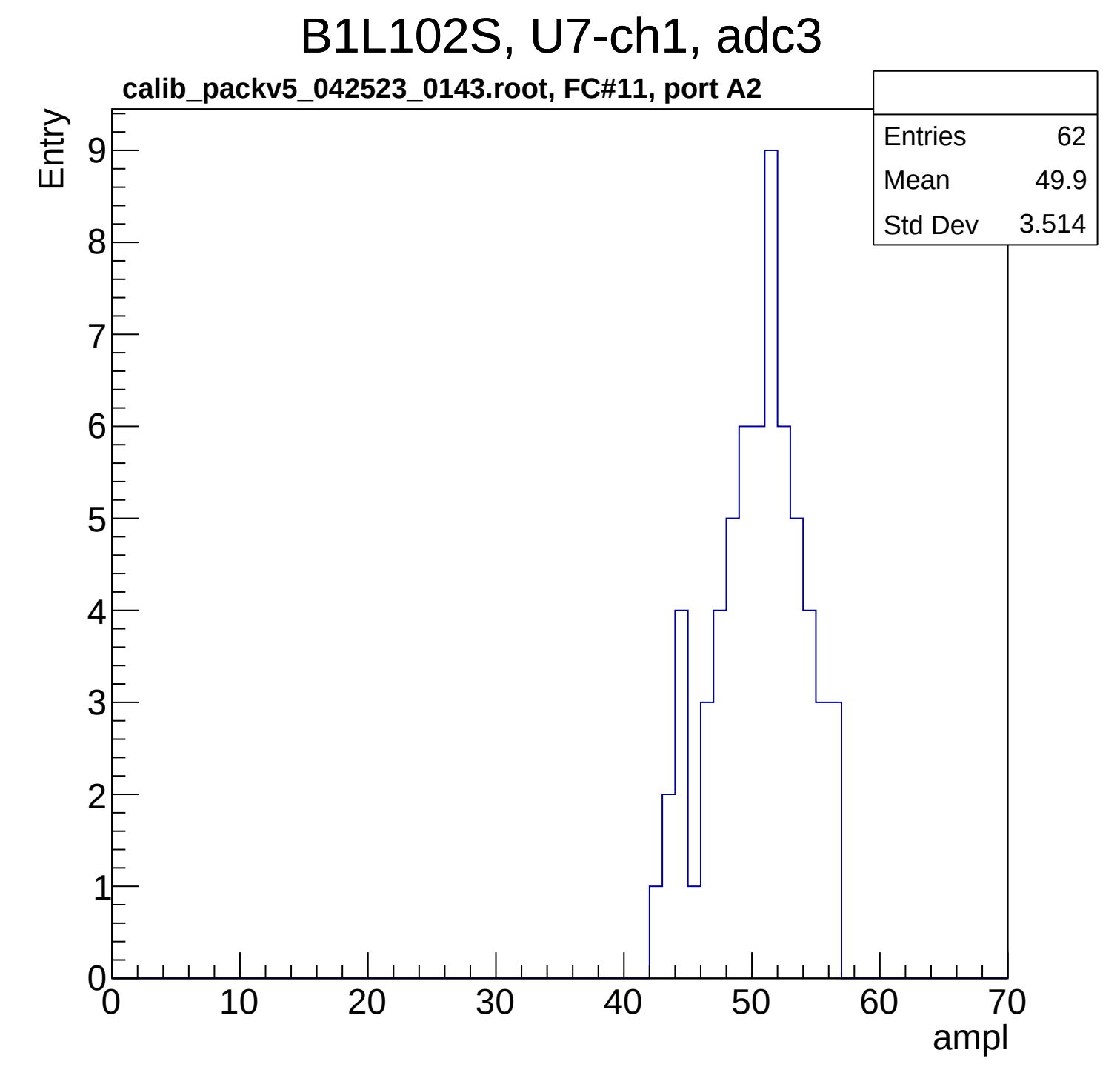
B1L102S, U7-ch1, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 62
Mean 49.9
Std Dev 3.514
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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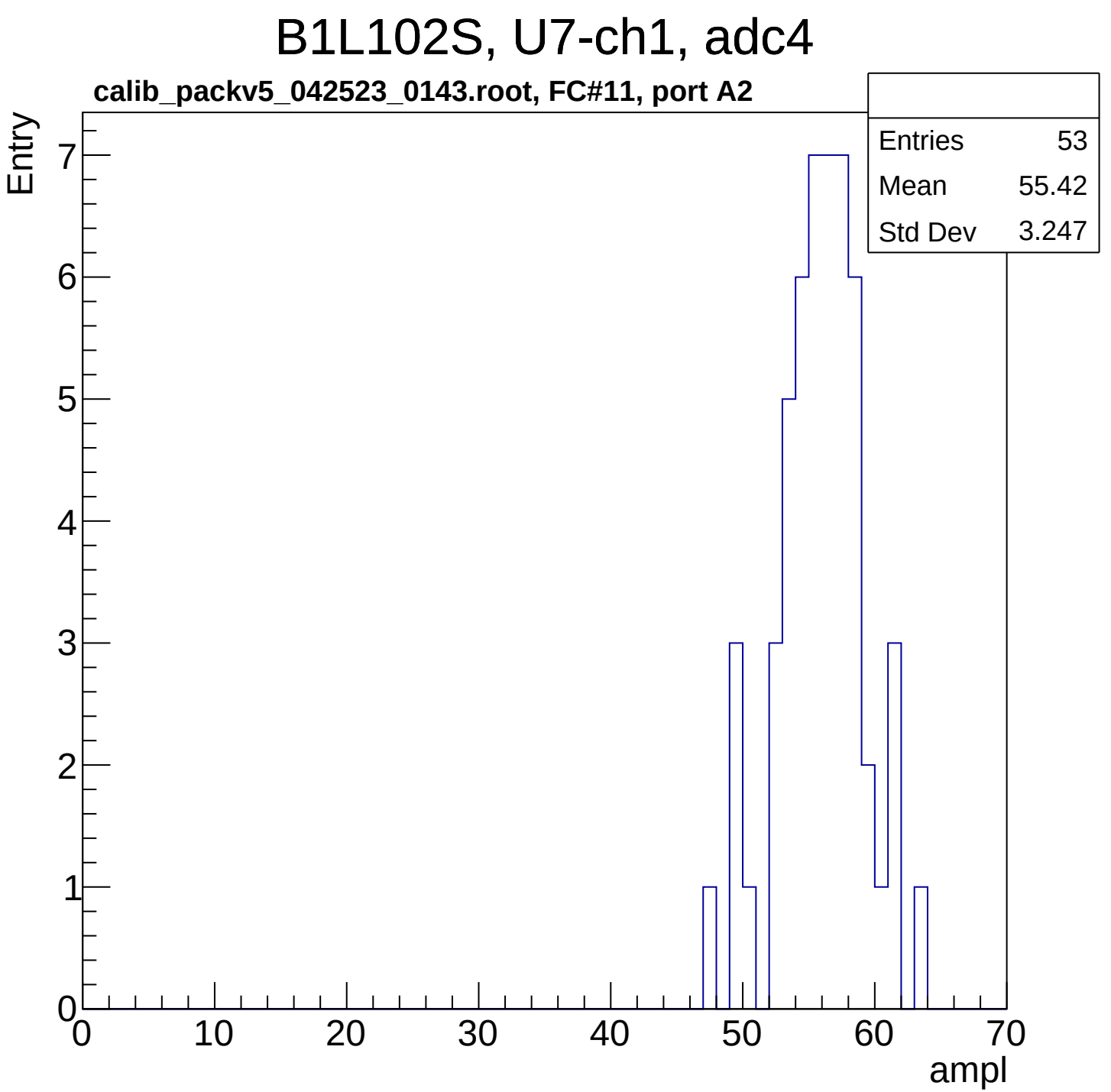
B1L102S, U7-ch1, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 53
Mean 55.42
Std Dev 3.247
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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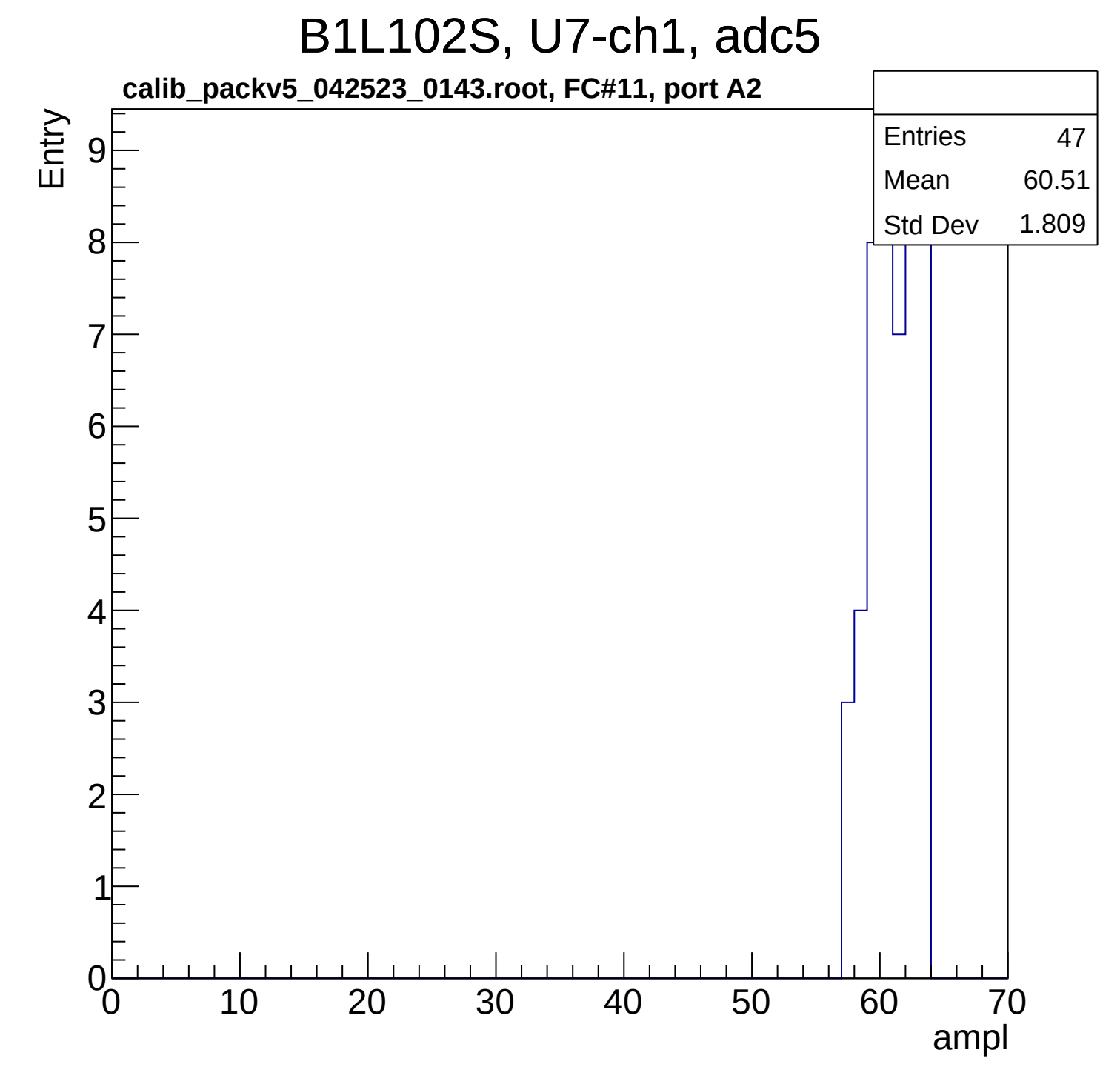
B1L102S, U7-ch1, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 47
Mean 60.51
Std Dev 1.809
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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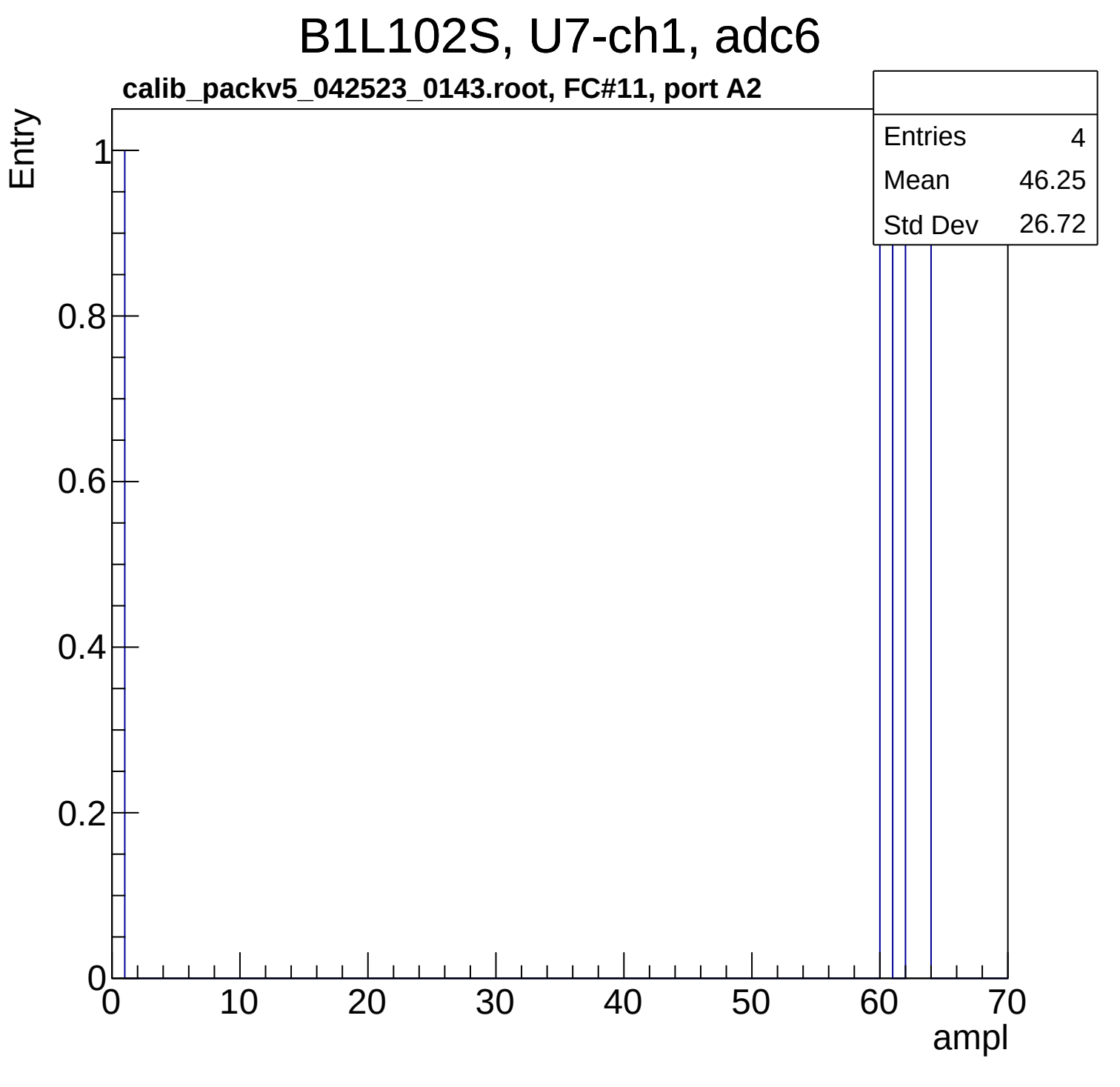
B1L102S, U7-ch1, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 4
Mean 46.25
Std Dev 26.72
Entry
ampl
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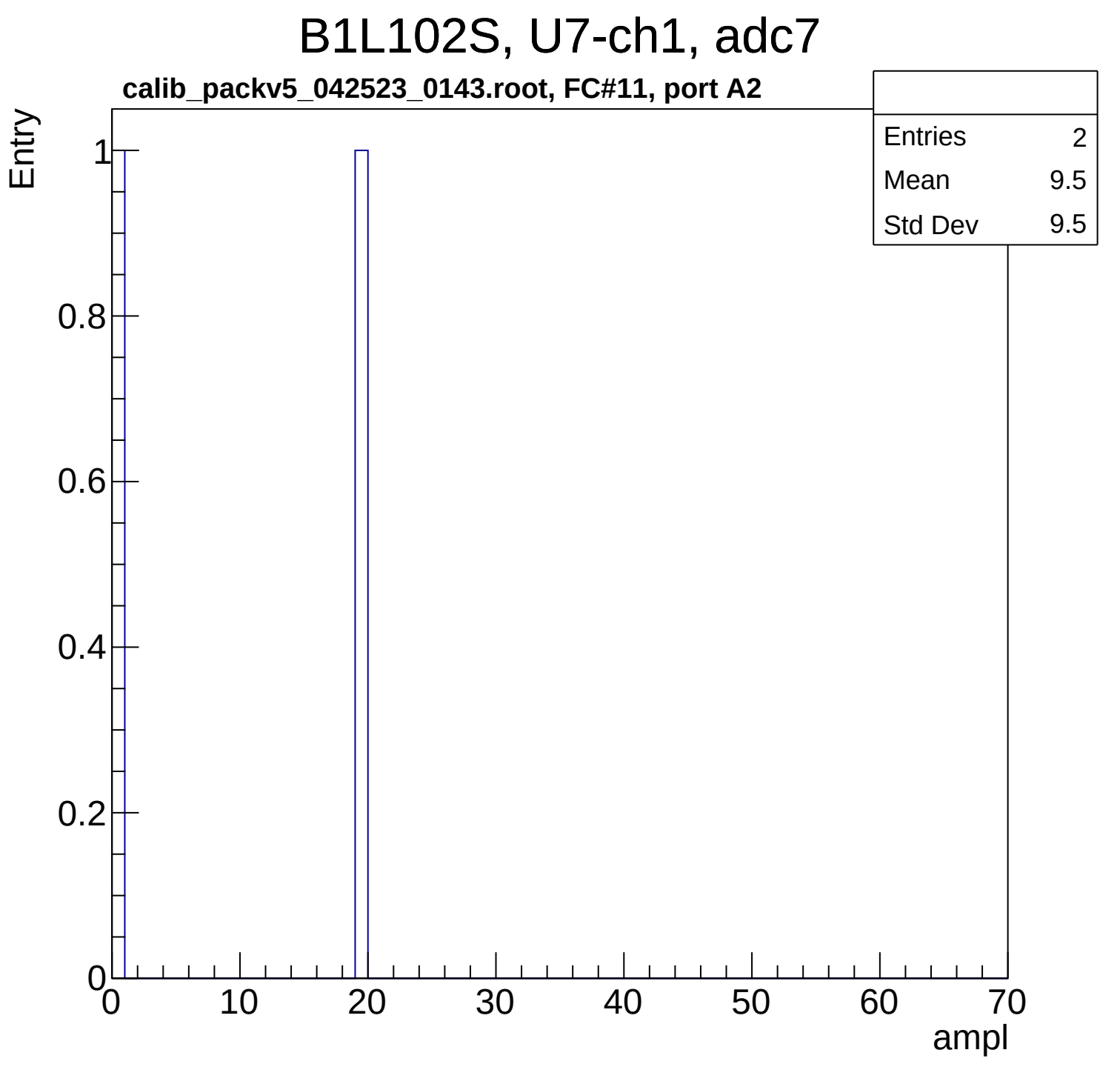
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70


B1L102S, U7-ch1, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 2
Mean 9.5
Std Dev 9.5
Entry
ampl
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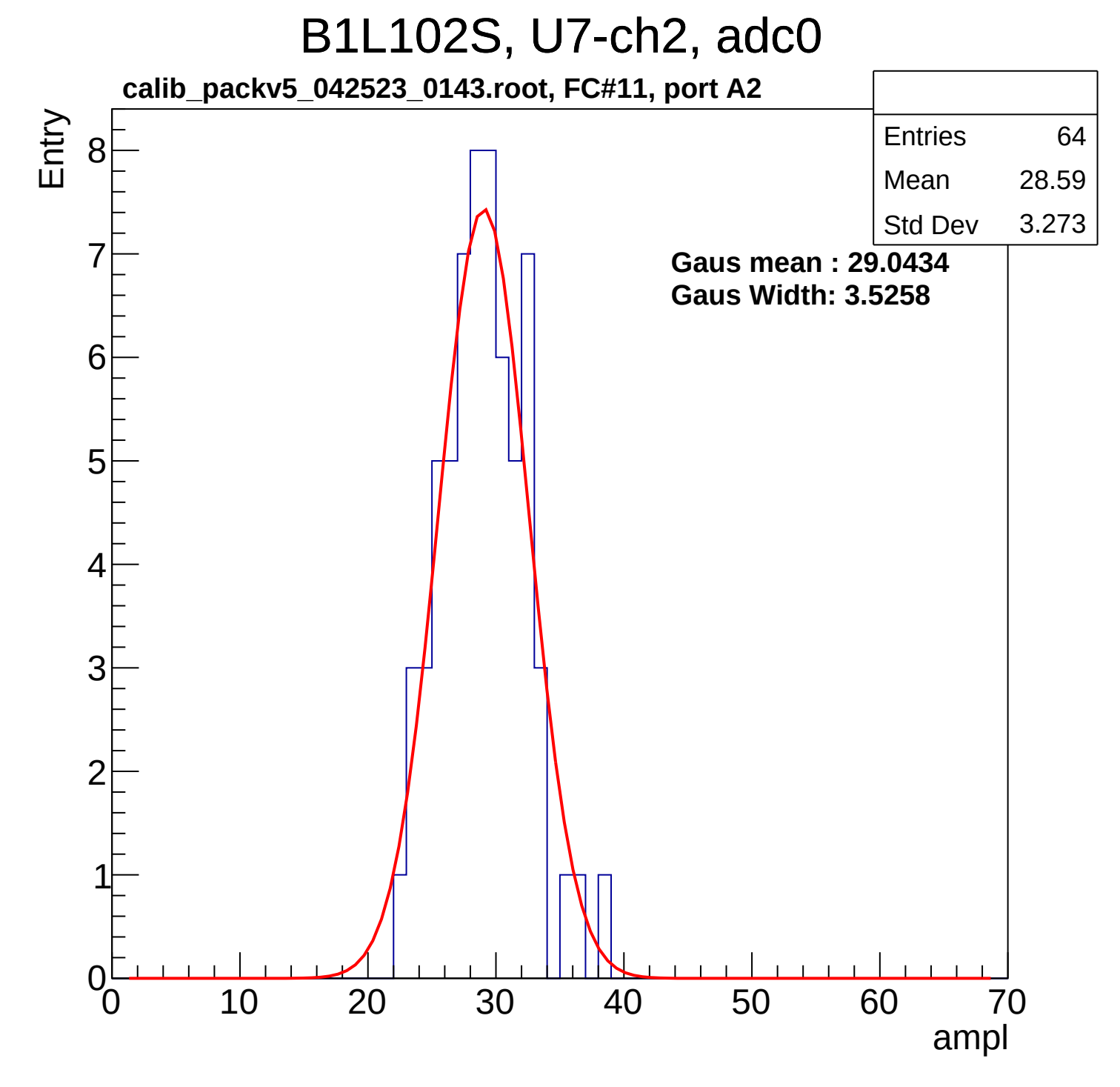
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70


B1L102S, U7-ch2, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 64
Mean 28.59
Std Dev 3.273
Gaus mean : 29.0434
Gaus Width: 3.5258
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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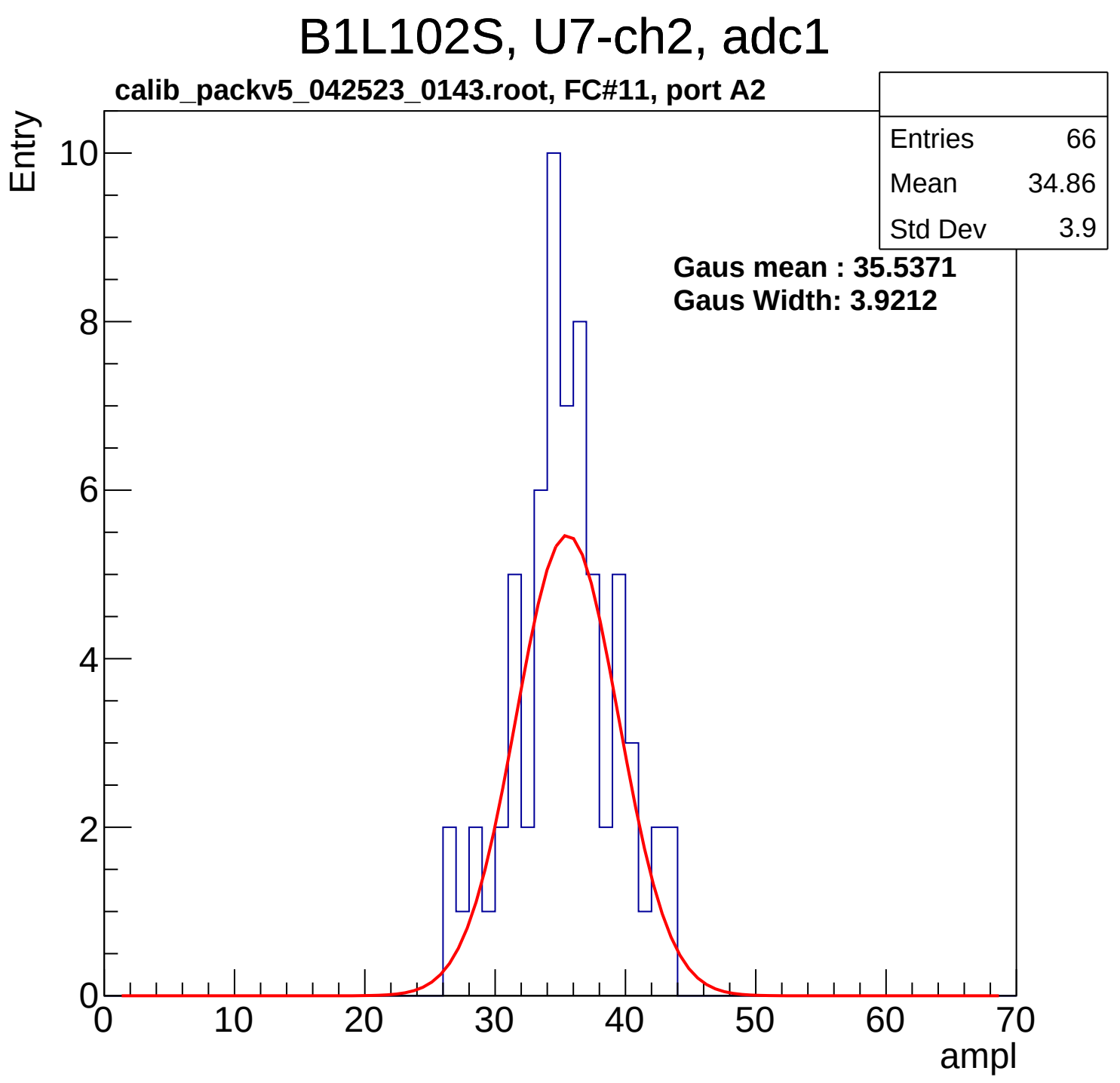
B1L102S, U7-ch2, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 66
Mean 34.86
Std Dev 3.9
Gaus mean : 35.5371
Gaus Width: 3.9212
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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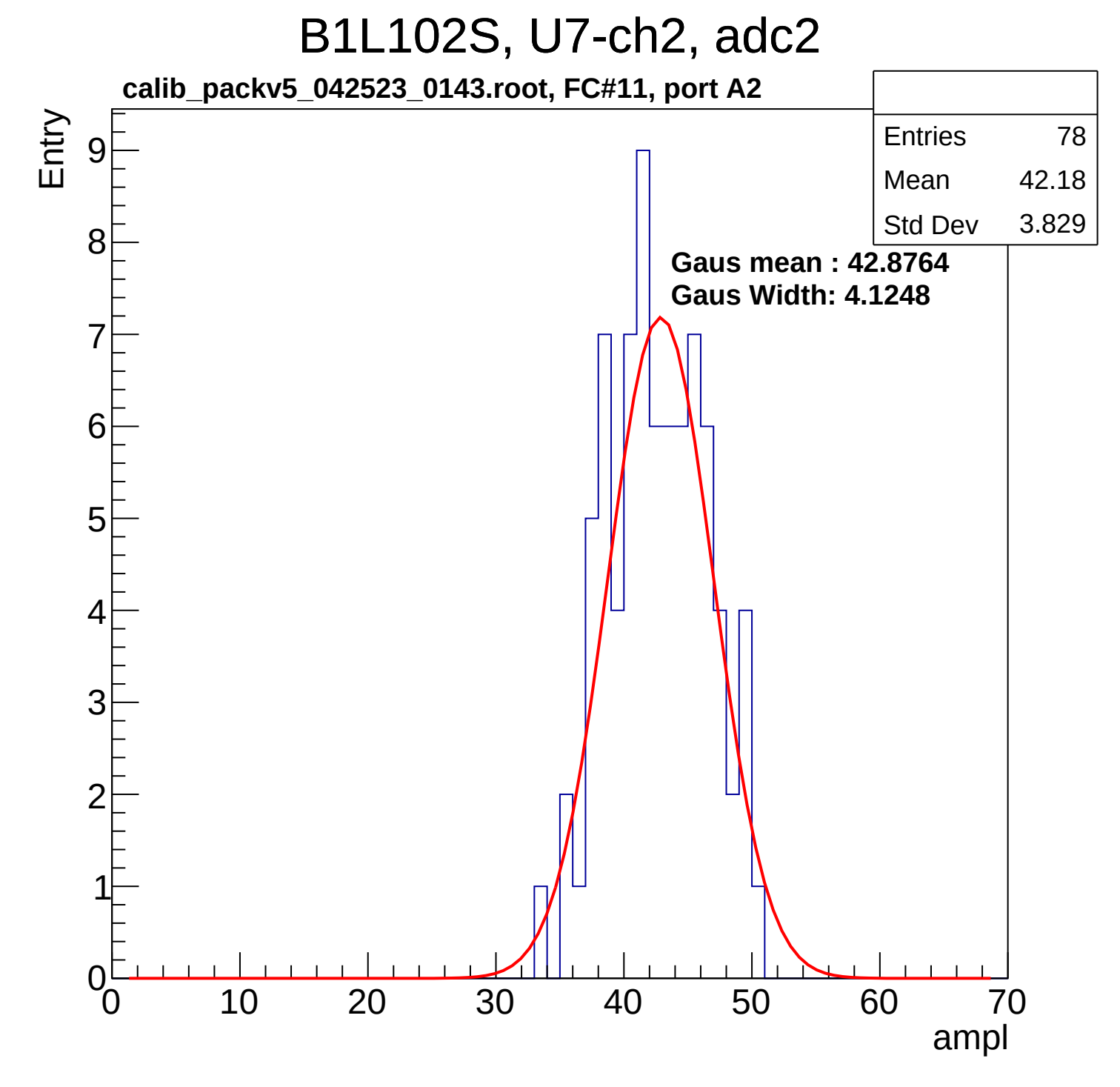
B1L102S, U7-ch2, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 78
Mean 42.18
Std Dev 3.829
Gaus mean : 42.8764
Gaus Width: 4.1248
Entry
ampl
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2
3
4
5
6
7
8
9
0
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60
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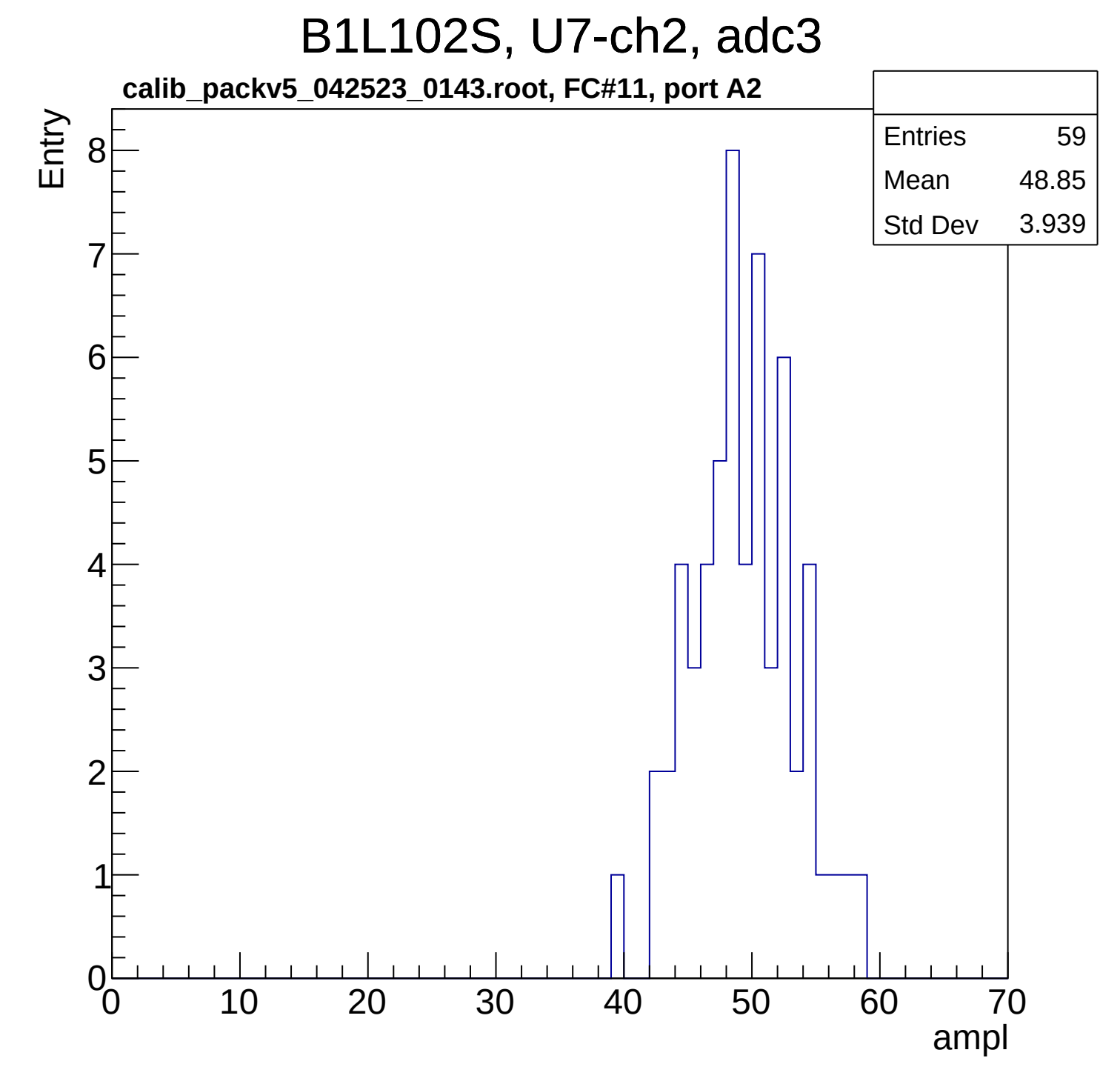
B1L102S, U7-ch2, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 59
Mean 48.85
Std Dev 3.939
Entry
ampl
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0
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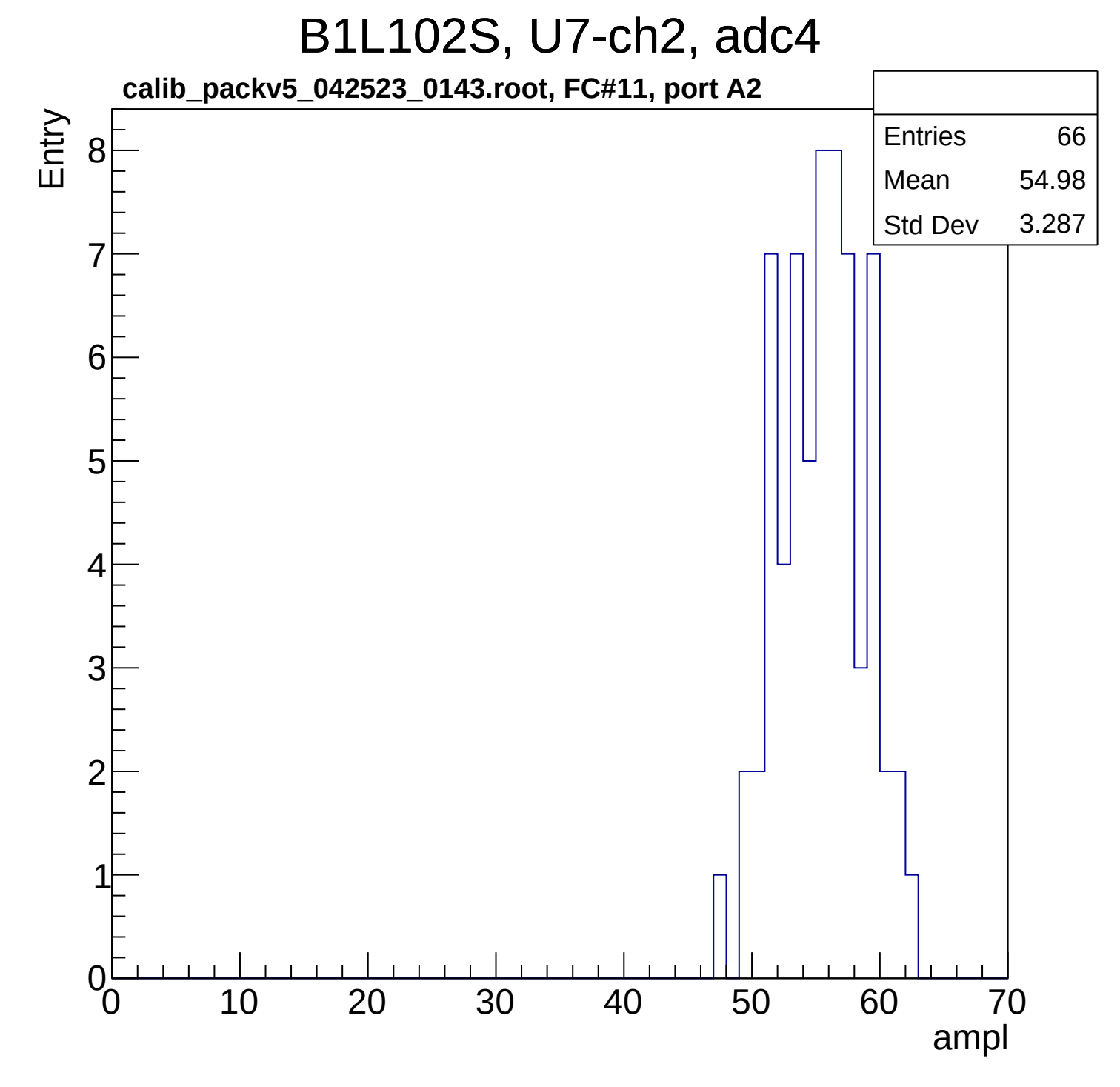
B1L102S, U7-ch2, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 66
Mean 54.98
Std Dev 3.287
Entry
ampl
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5
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0
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60
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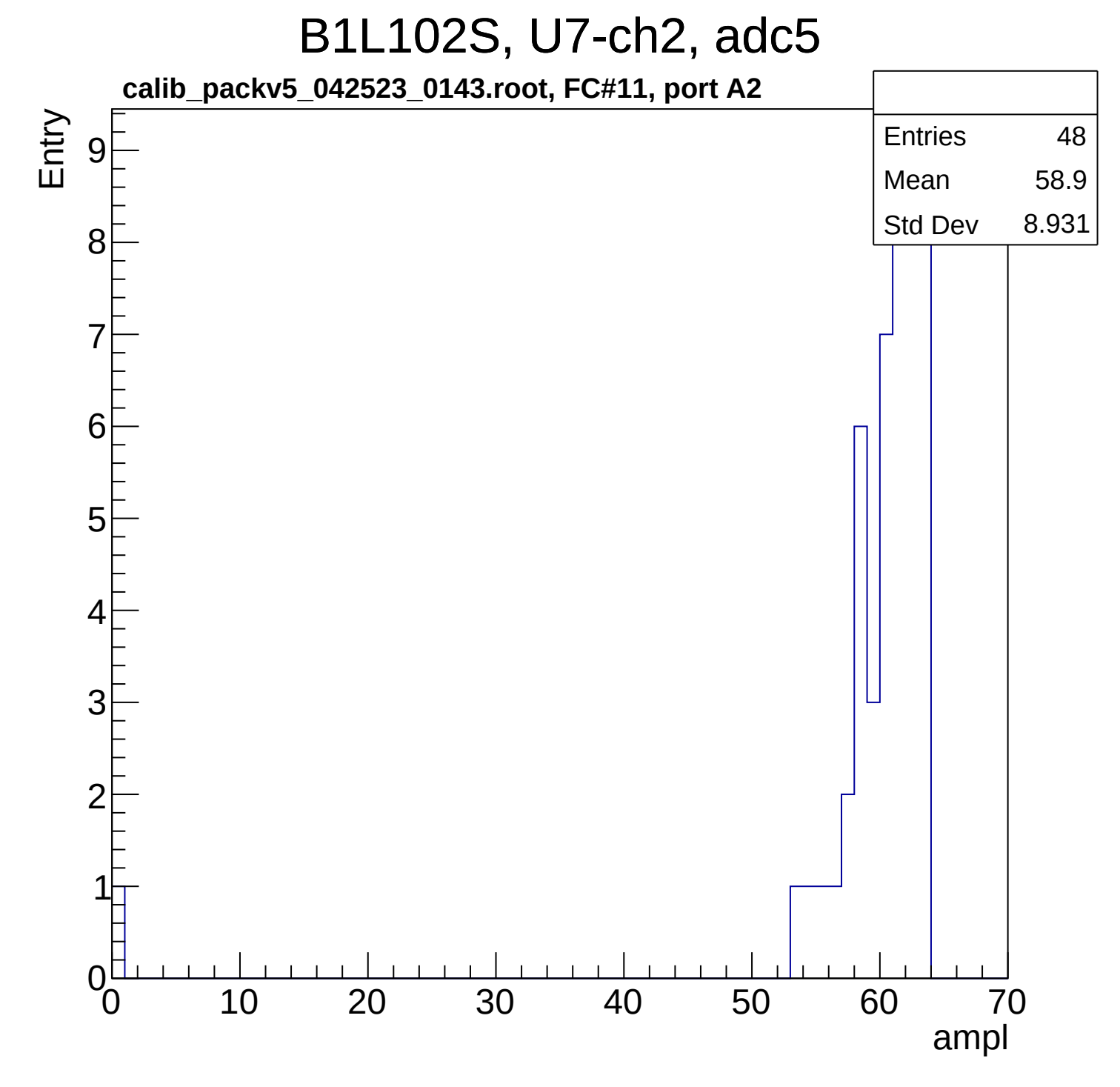
B1L102S, U7-ch2, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 48
Mean 58.9
Std Dev 8.931
Entry
ampl
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4
5
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0
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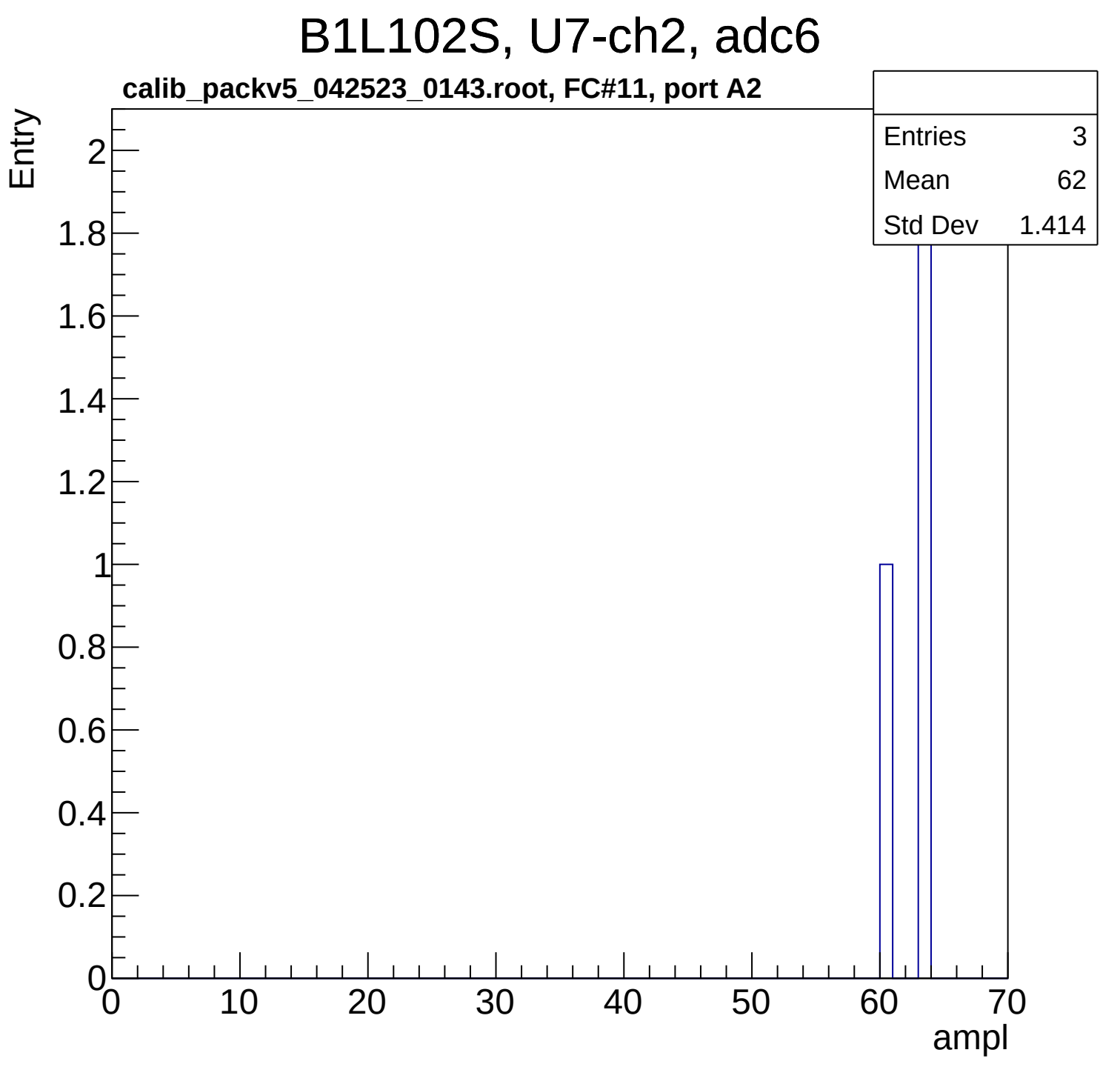
B1L102S, U7-ch2, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 3
Mean 62
Std Dev 1.414
Entry
ampl
0
0.2
0.4
0.6
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1
1.2
1.4
1.6
1.8
2
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40
50
60
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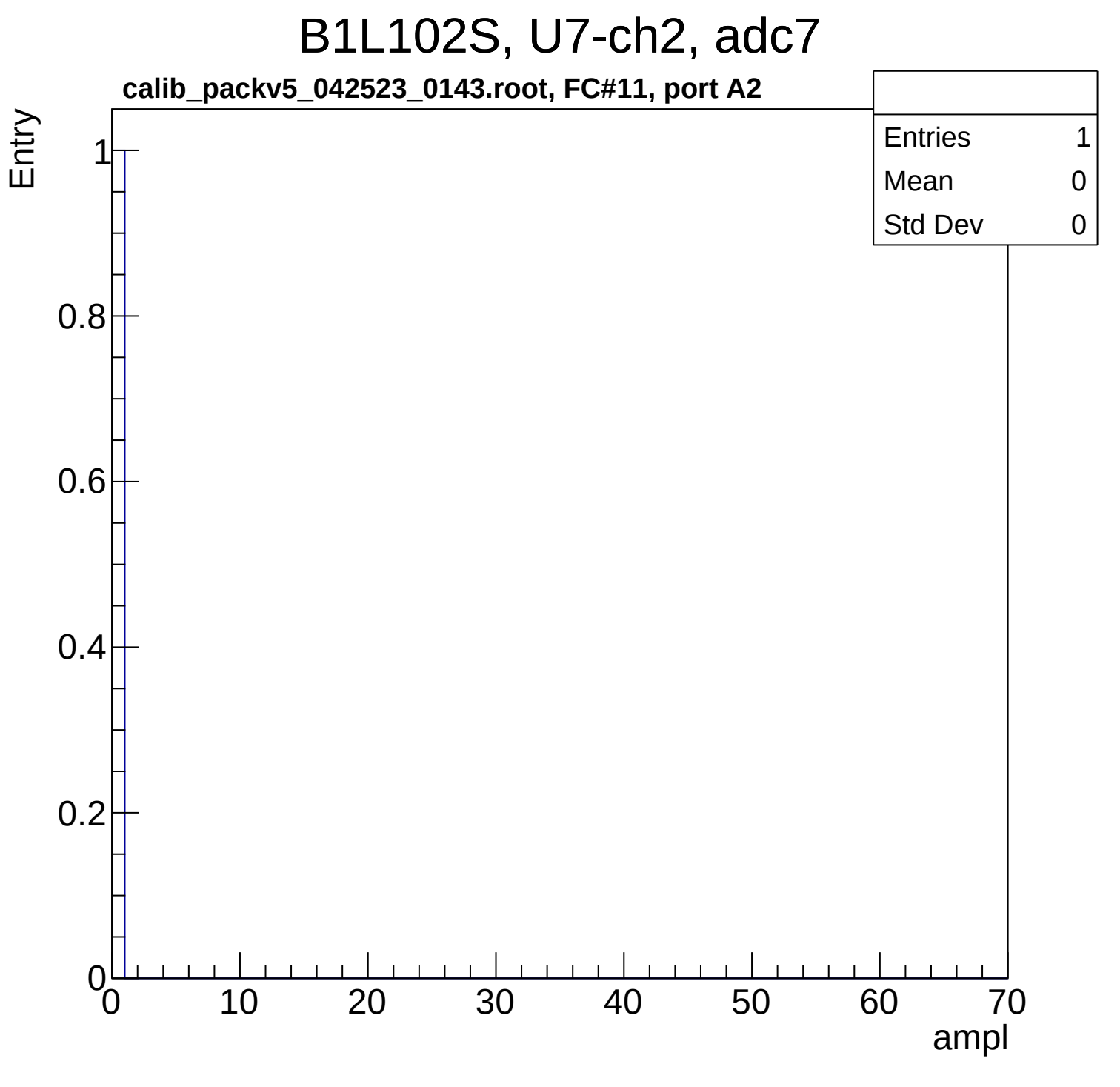
B1L102S, U7-ch2, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 1
Mean 0
Std Dev 0
Entry
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0.8
0.6
0.4
0.2
0
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10
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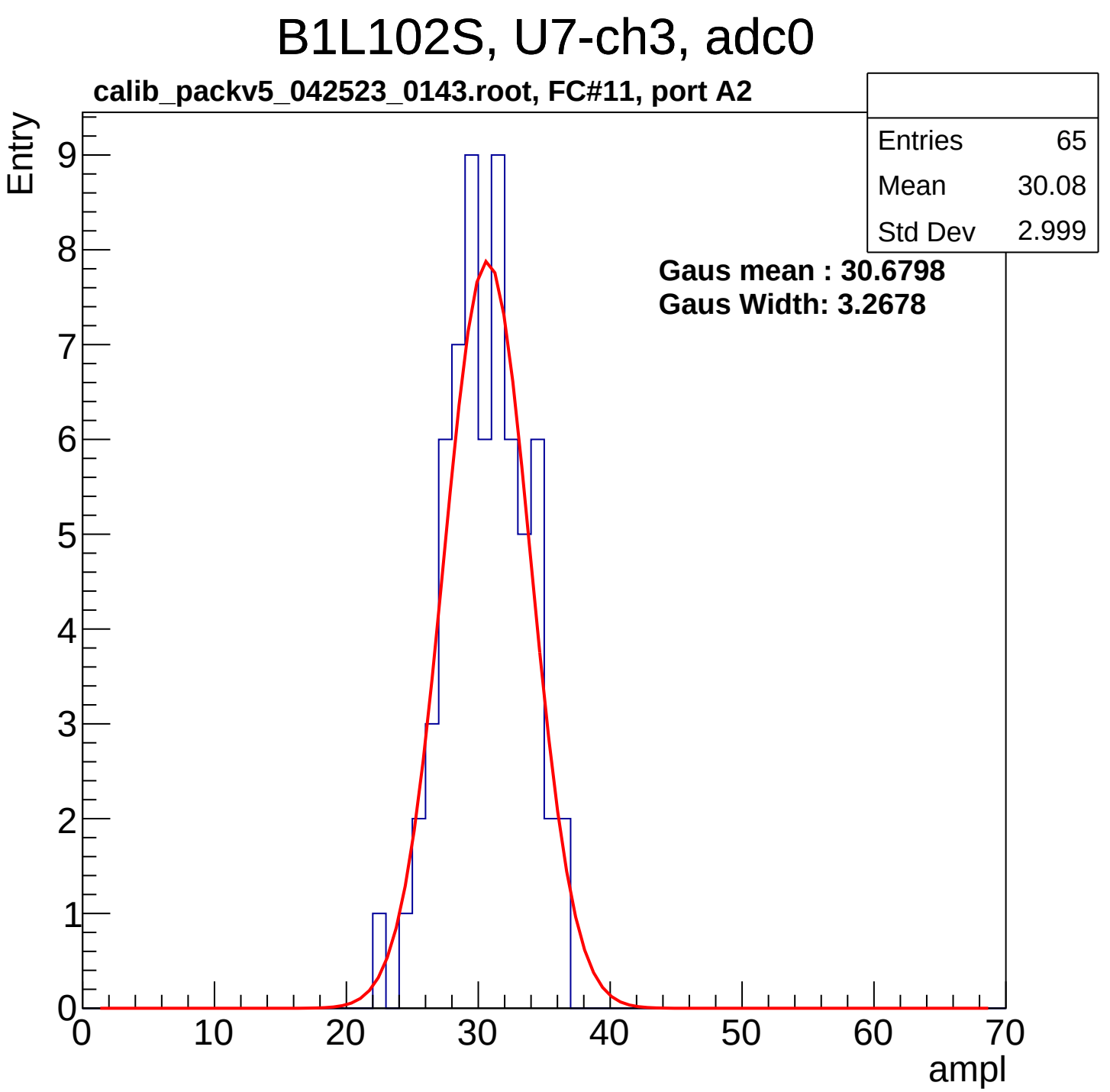
50
60
70
ampl


B1L102S, U7-ch3, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 65
Mean 30.08
Std Dev 2.999
Gaus mean : 30.6798
Gaus Width: 3.2678
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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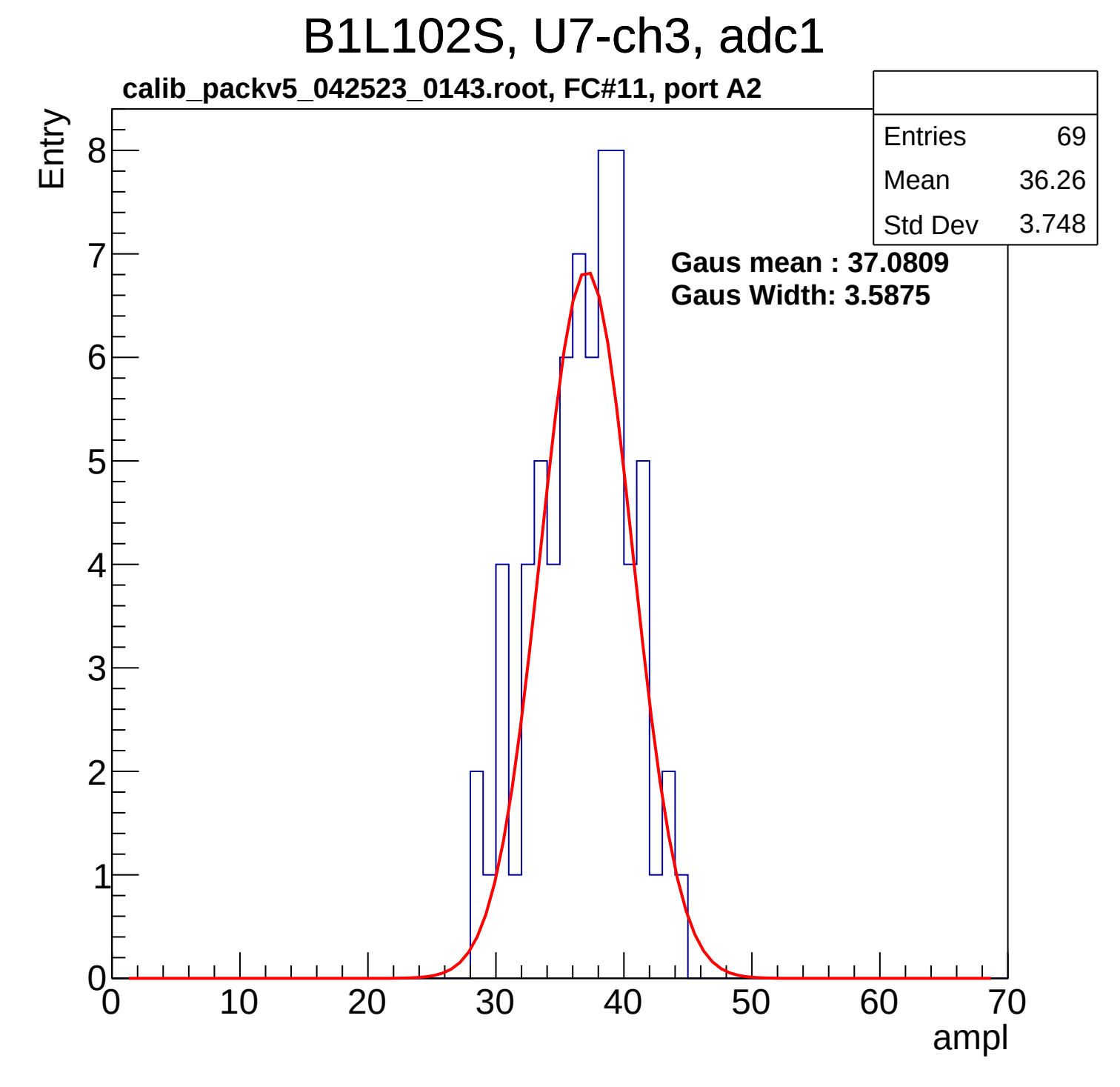
B1L102S, U7-ch3, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 69
Mean 36.26
Std Dev 3.748
Gaus mean : 37.0809
Gaus Width: 3.5875
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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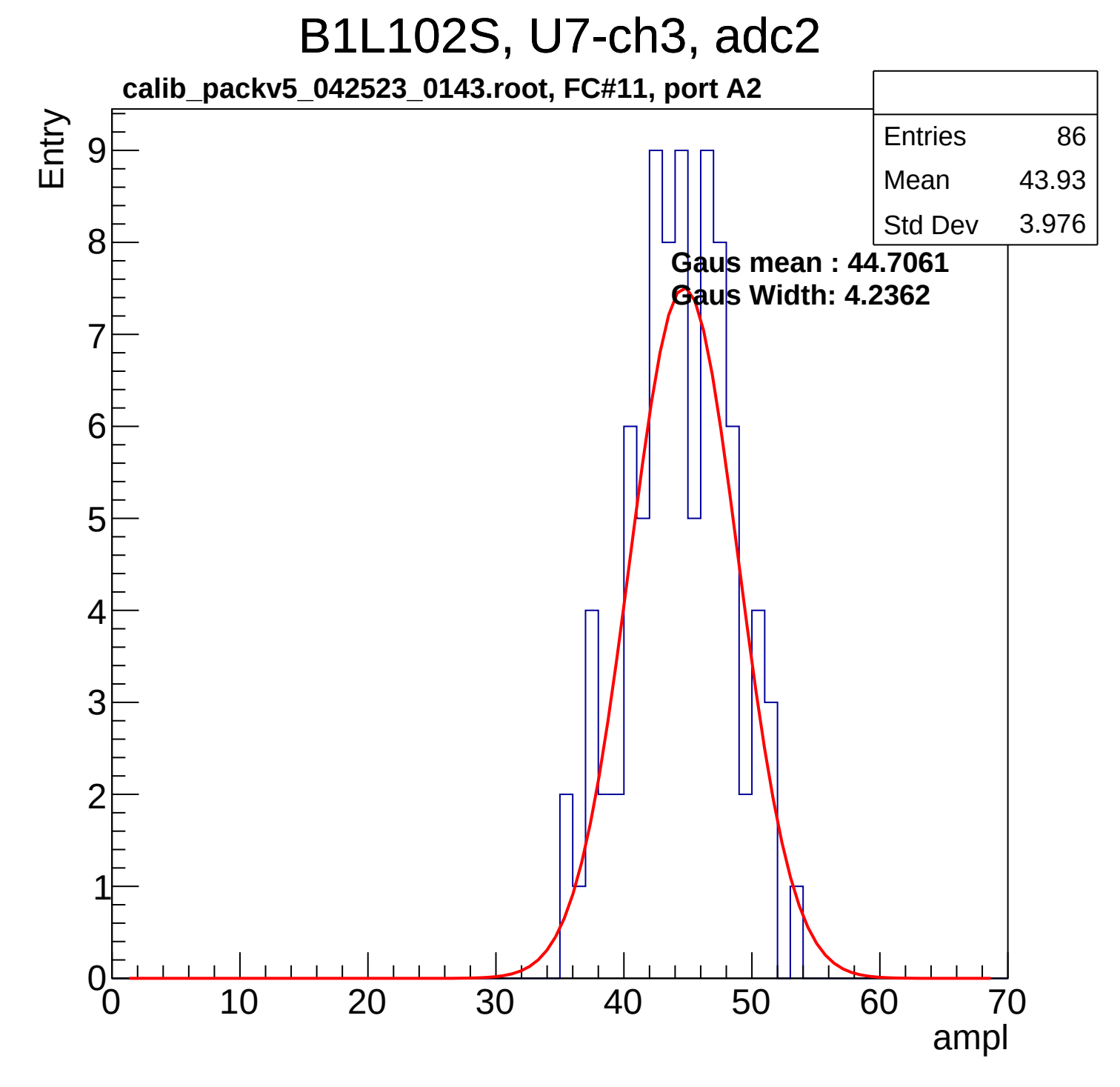
B1L102S, U7-ch3, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 86
Mean 43.93
Std Dev 3.976
Gaus mean : 44.7061
Gaus Width: 4.2362
Entry
ampl
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2
3
4
5
6
7
8
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0
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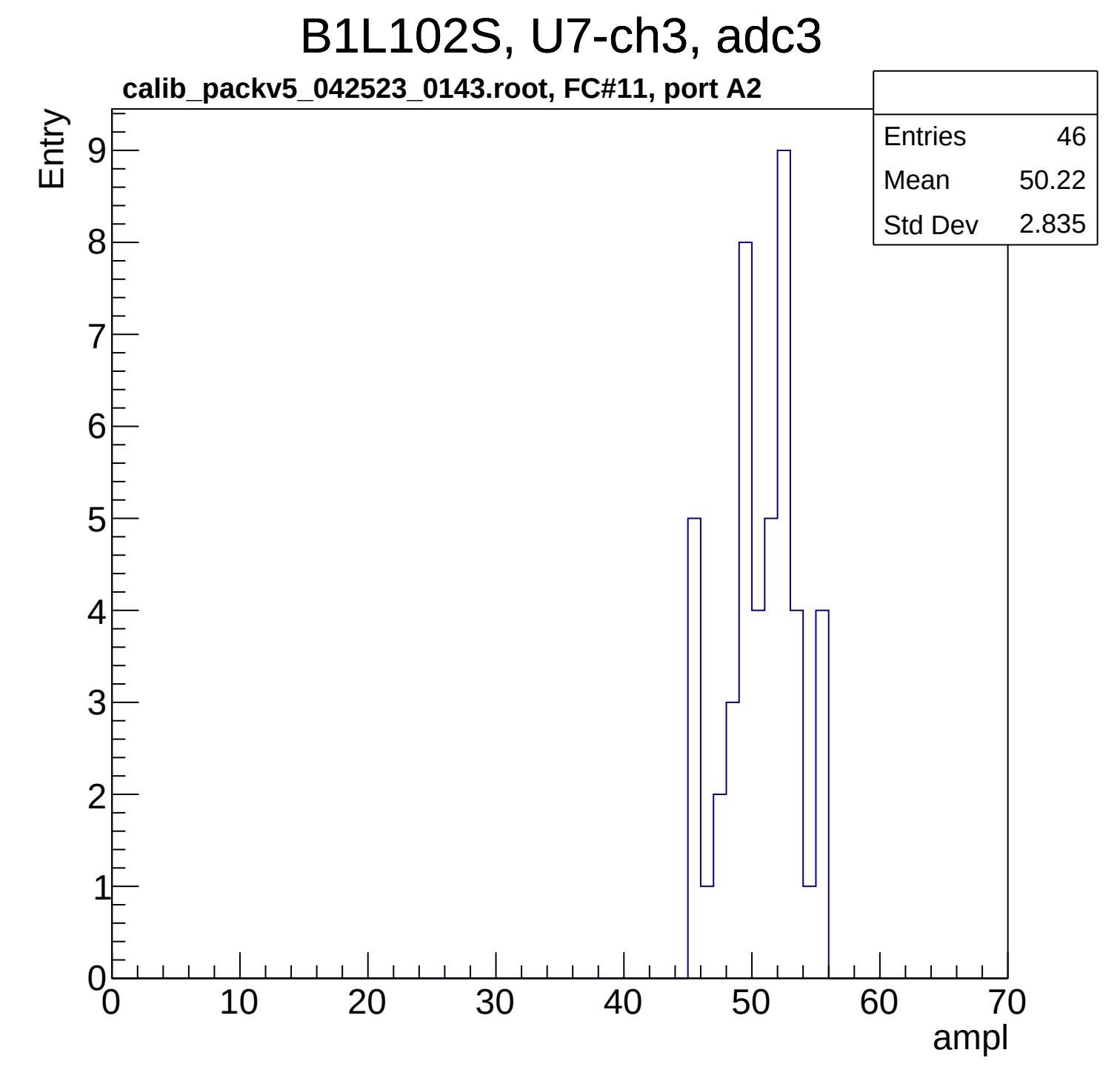
B1L102S, U7-ch3, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 46
Mean 50.22
Std Dev 2.835
Entry
ampl
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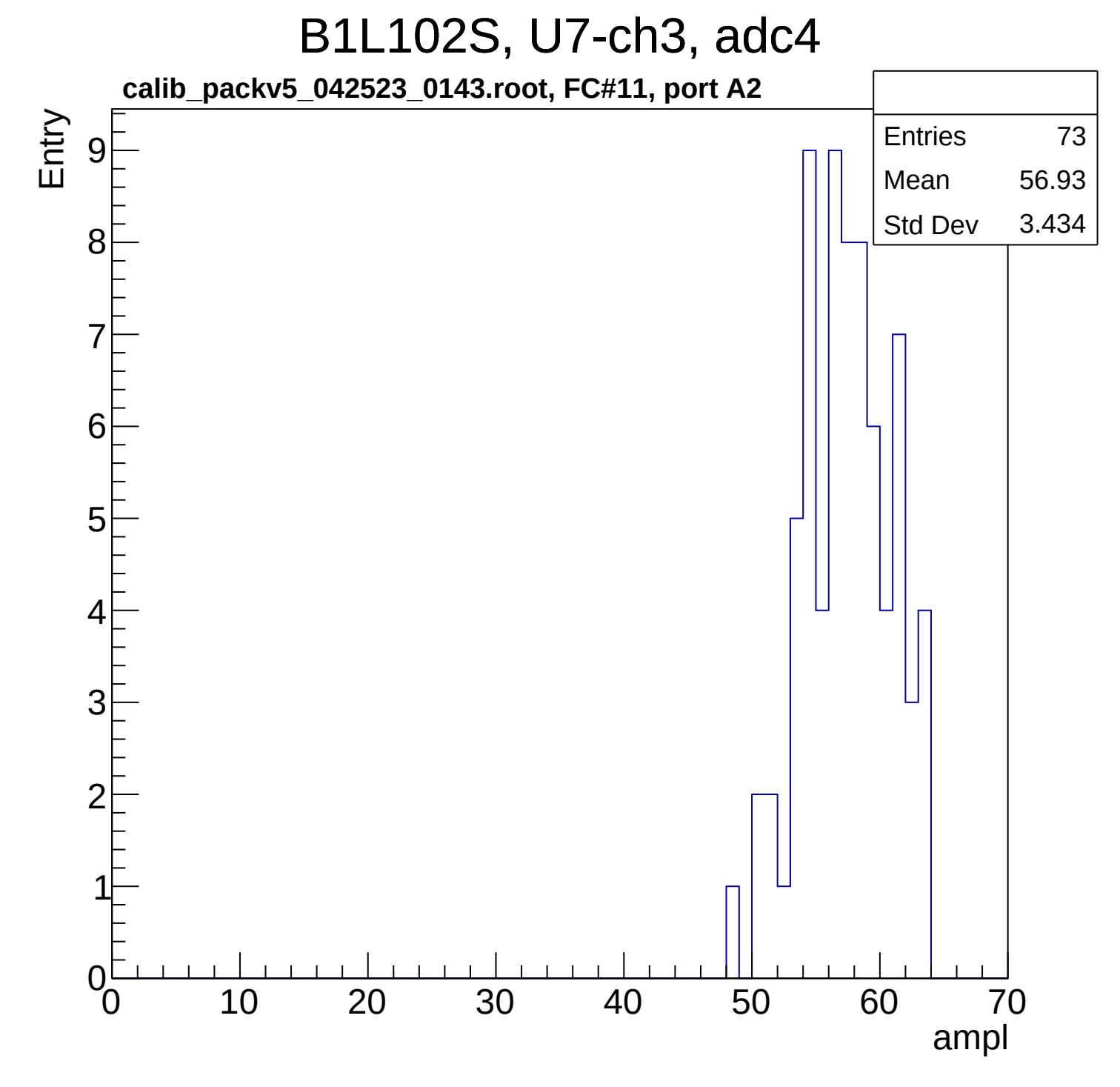
B1L102S, U7-ch3, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 73
Mean 56.93
Std Dev 3.434
Entry
ampl
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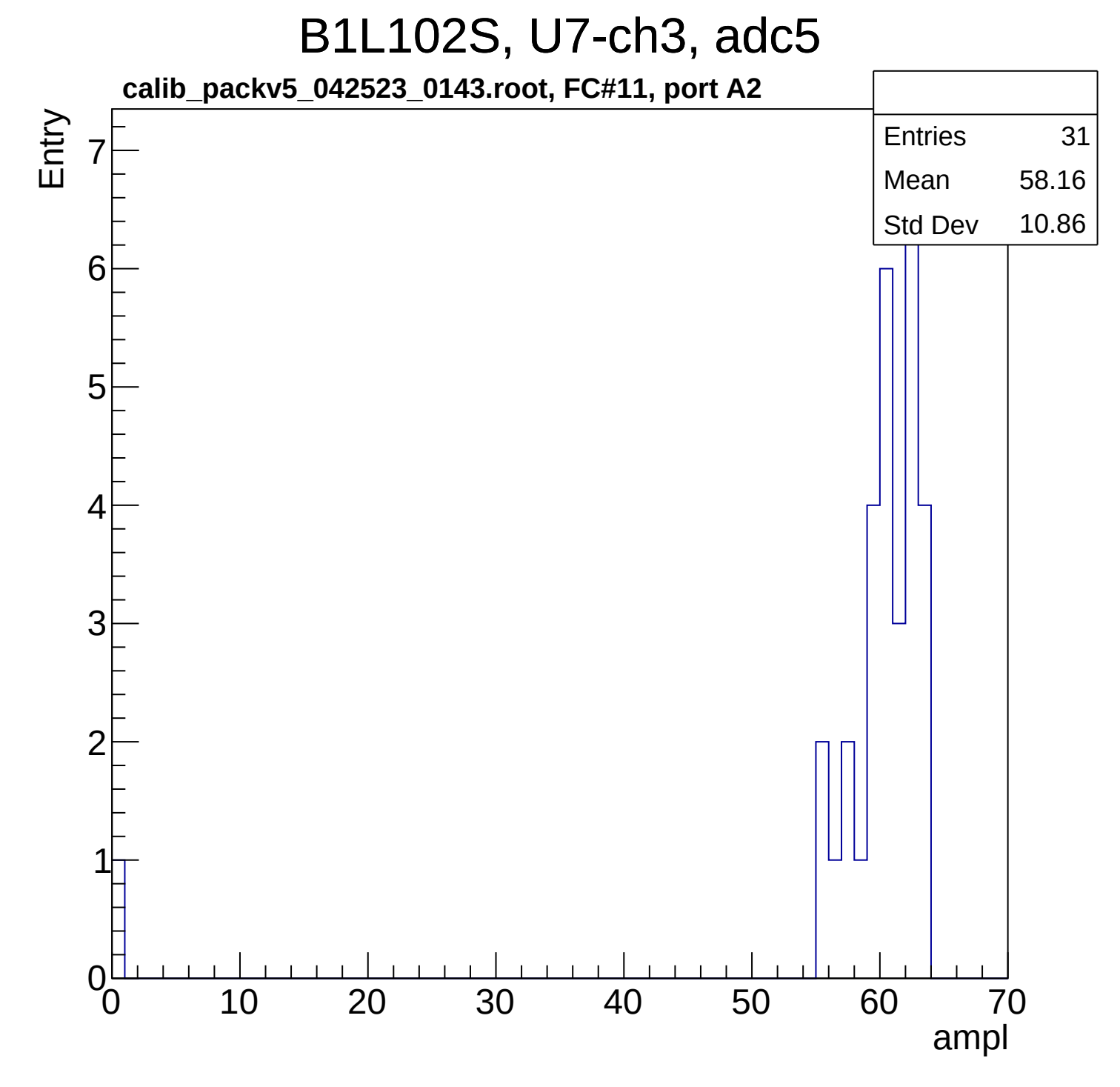
B1L102S, U7-ch3, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 31
Mean 58.16
Std Dev 10.86
Entry
ampl
0
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0
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20
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40
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60
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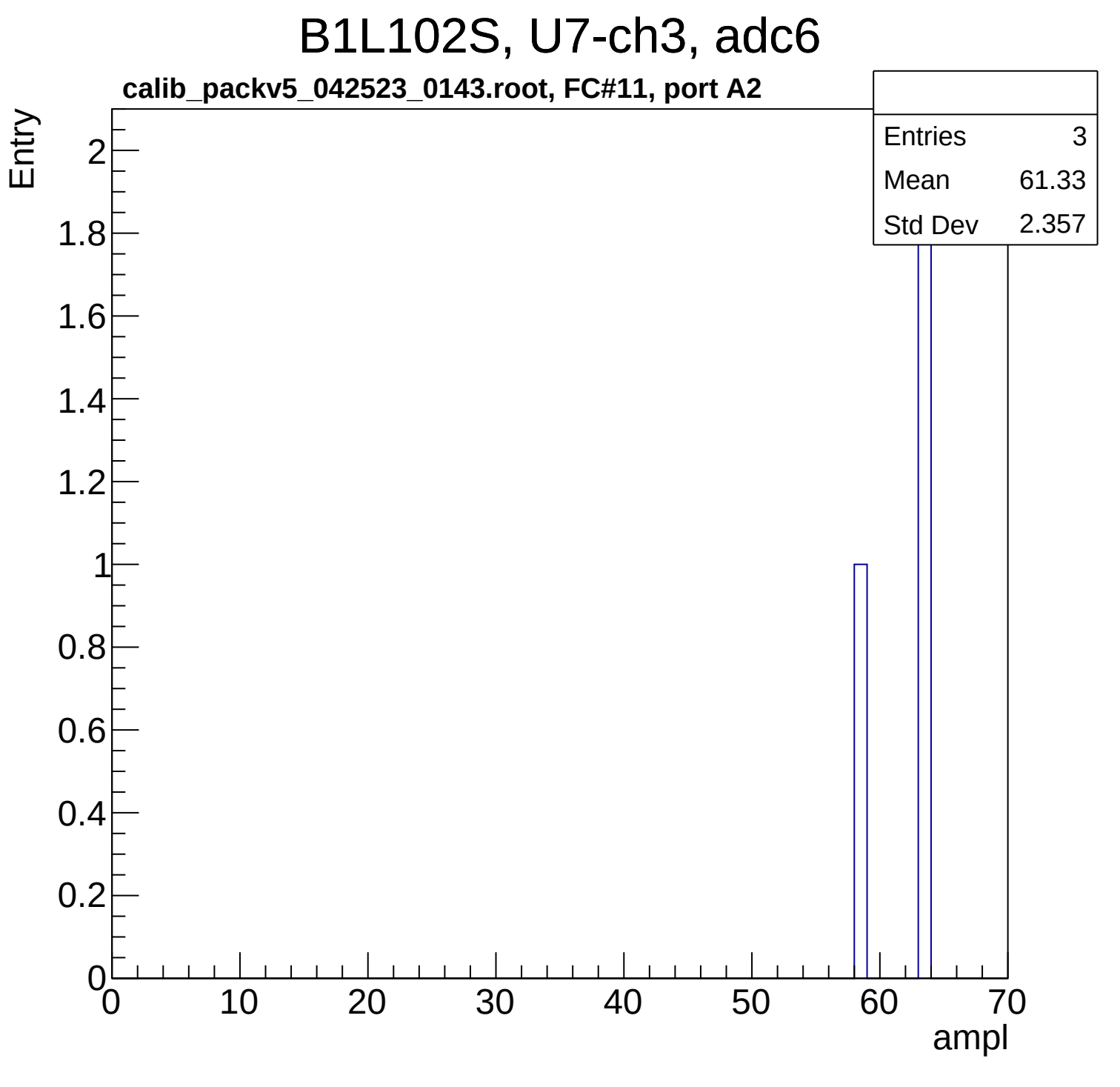
B1L102S, U7-ch3, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 3
Mean 61.33
Std Dev 2.357
Entry
ampl
0
0.2
0.4
0.6
0.8
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1.2
1.4
1.6
1.8
2
0
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20
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60
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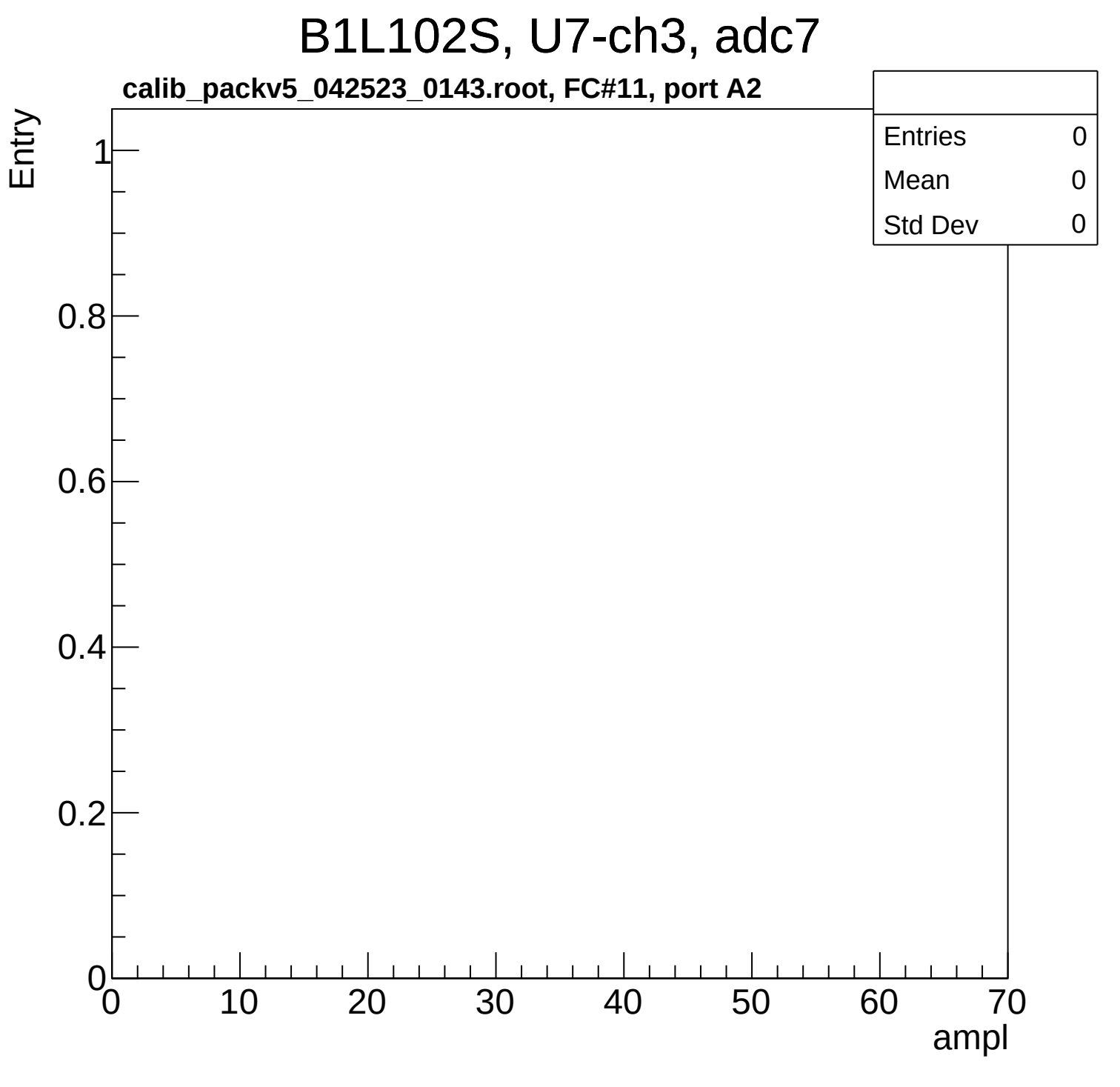
B1L102S, U7-ch3, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 0
Mean 0
Std Dev 0
Entry
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0.6
0.4
0.2
0
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10
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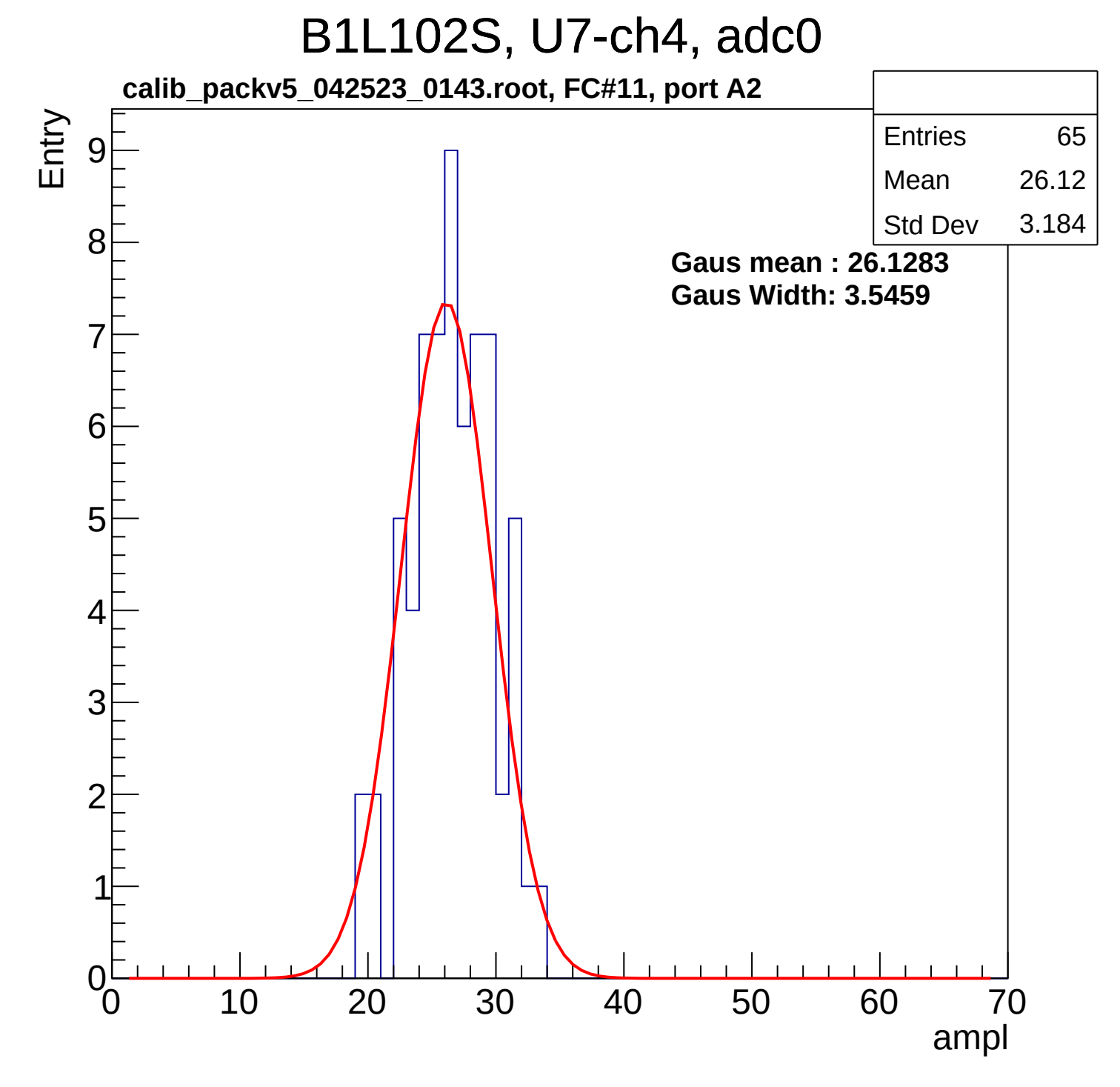
50
60
70
ampl


B1L102S, U7-ch4, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 65
Mean 26.12
Std Dev 3.184
Gaus mean : 26.1283
Gaus Width: 3.5459
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
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40
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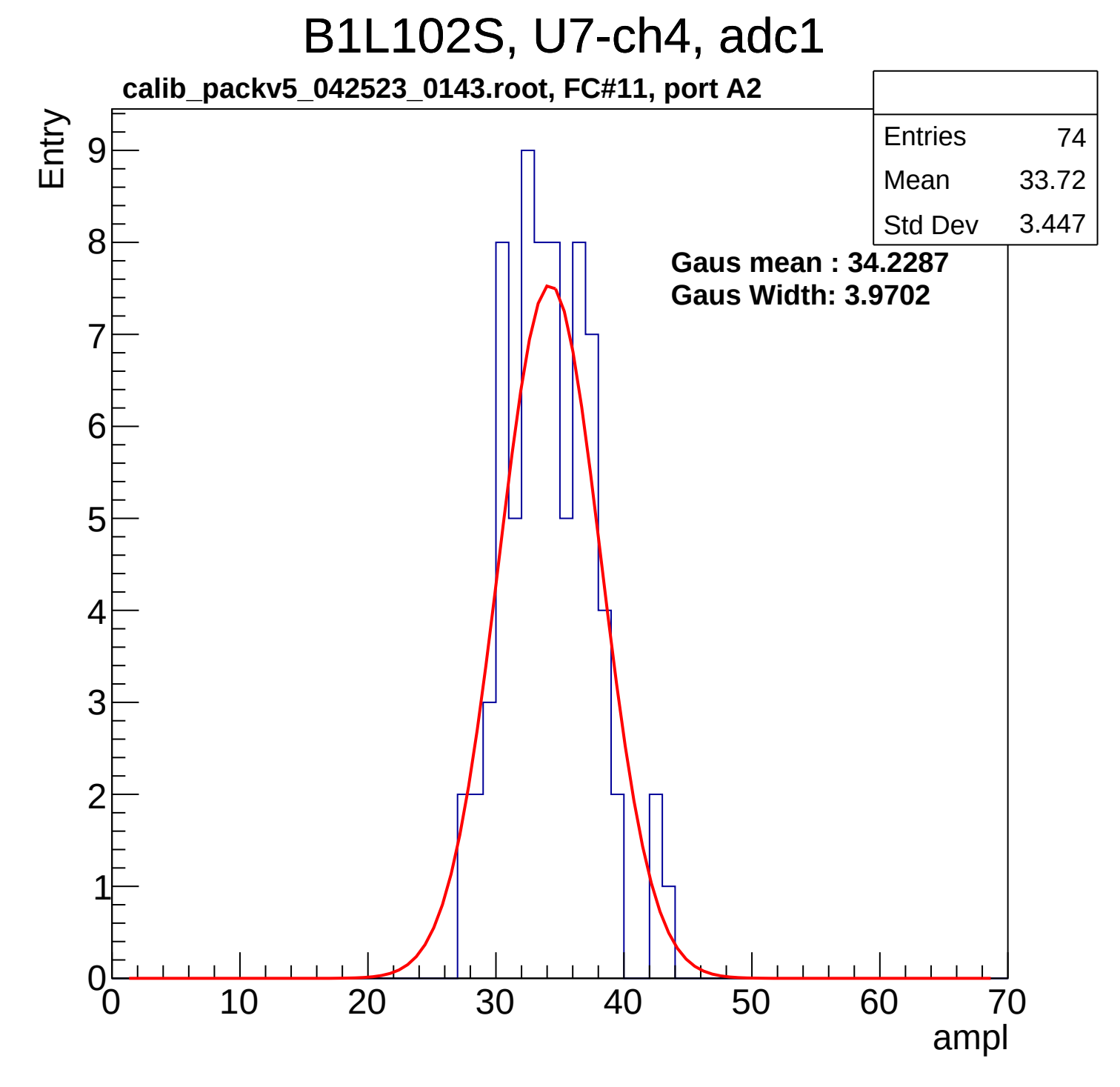
B1L102S, U7-ch4, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 74
Mean 33.72
Std Dev 3.447
Gaus mean : 34.2287
Gaus Width: 3.9702
Entry
ampl
0
1
2
3
4
5
6
7
8
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0
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20
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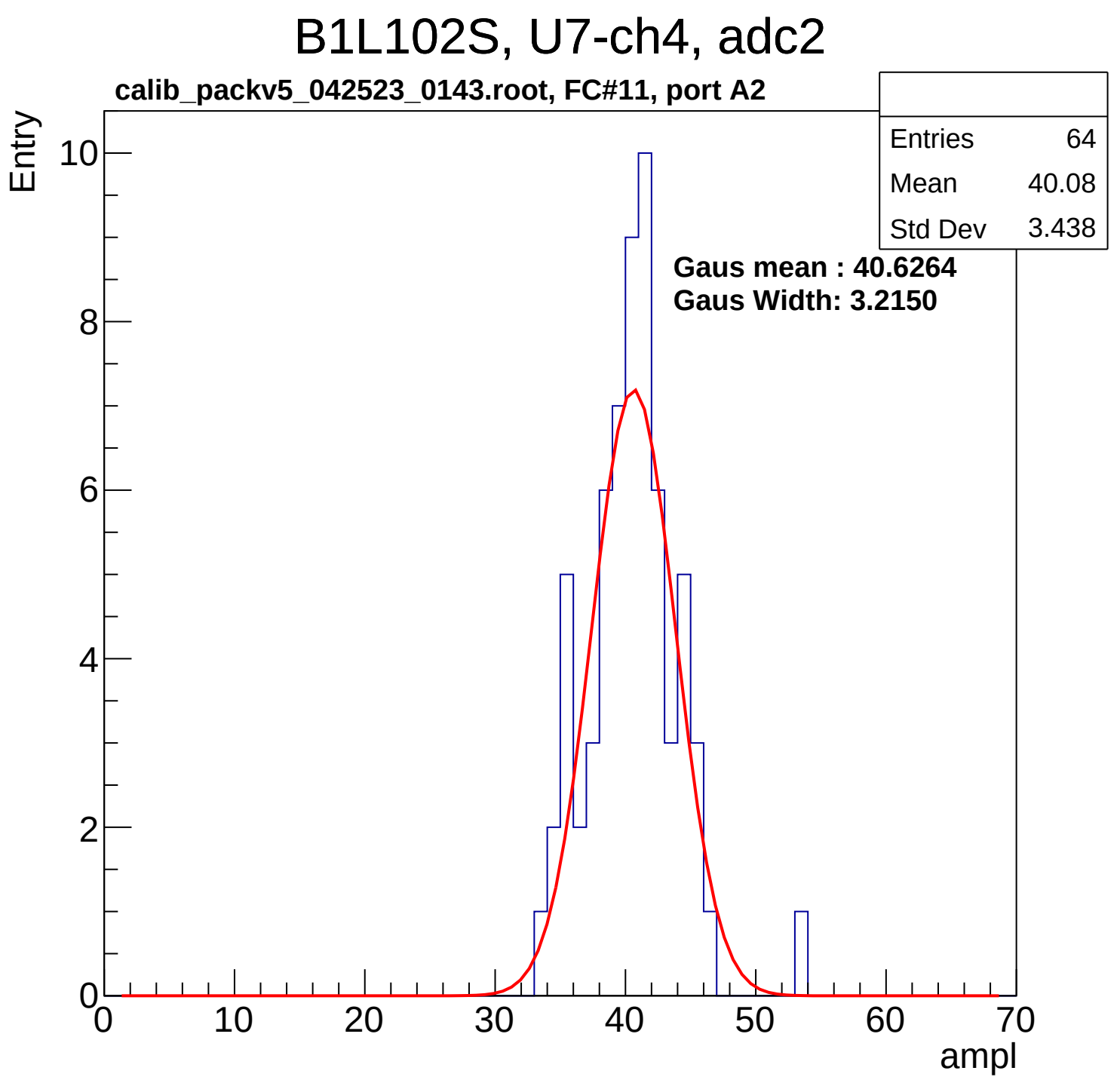
B1L102S, U7-ch4, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 64
Mean 40.08
Std Dev 3.438
Gaus mean : 40.6264
Gaus Width: 3.2150
Entry
ampl
0
2
4
6
8
10
0
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60
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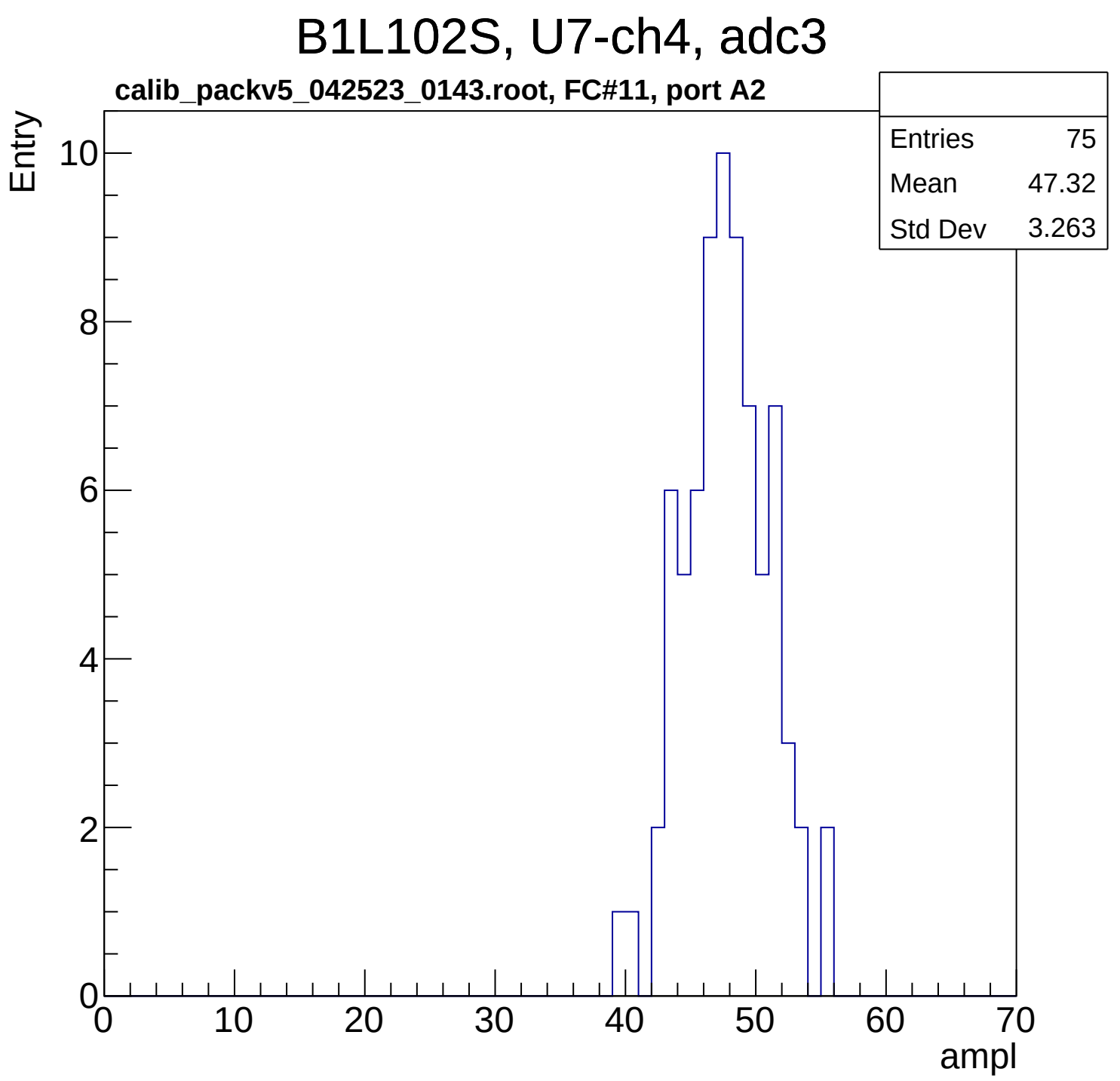
B1L102S, U7-ch4, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 75
Mean 47.32
Std Dev 3.263
Entry
ampl
0
2
4
6
8
10
0
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20
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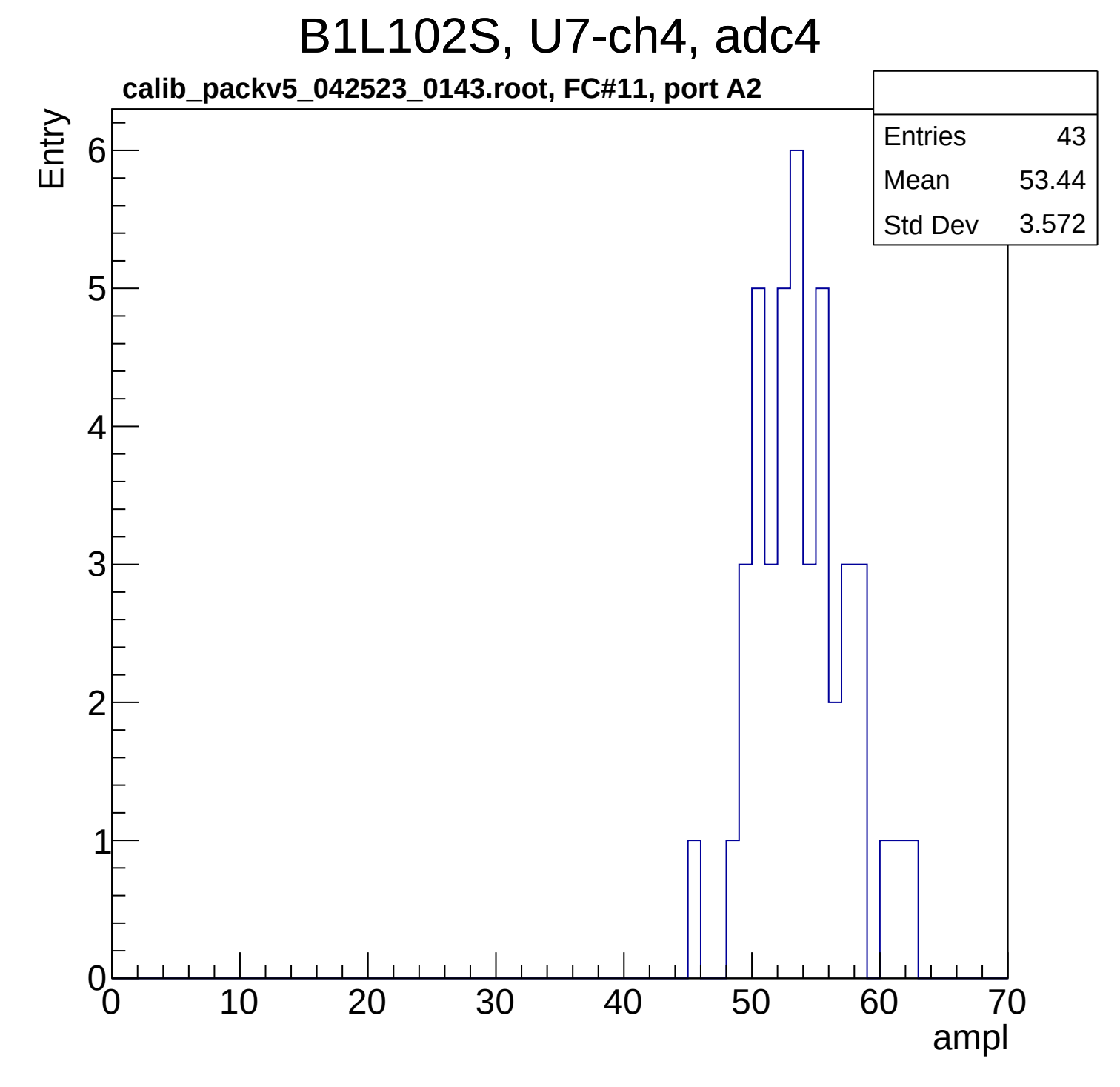
B1L102S, U7-ch4, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 43
Mean 53.44
Std Dev 3.572
Entry
ampl
0
1
2
3
4
5
6
0
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20
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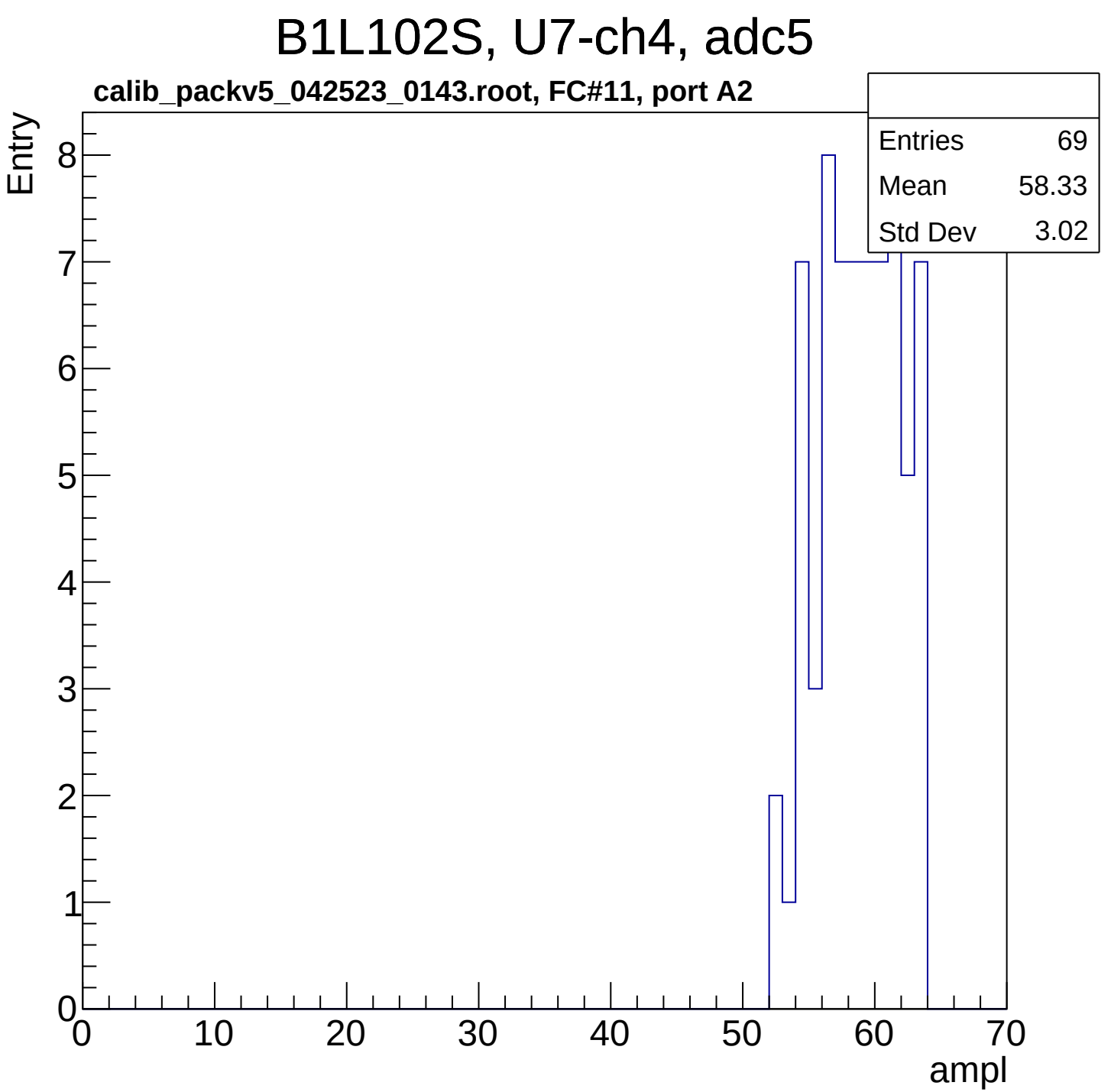
B1L102S, U7-ch4, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 69
Mean 58.33
Std Dev 3.02
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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40
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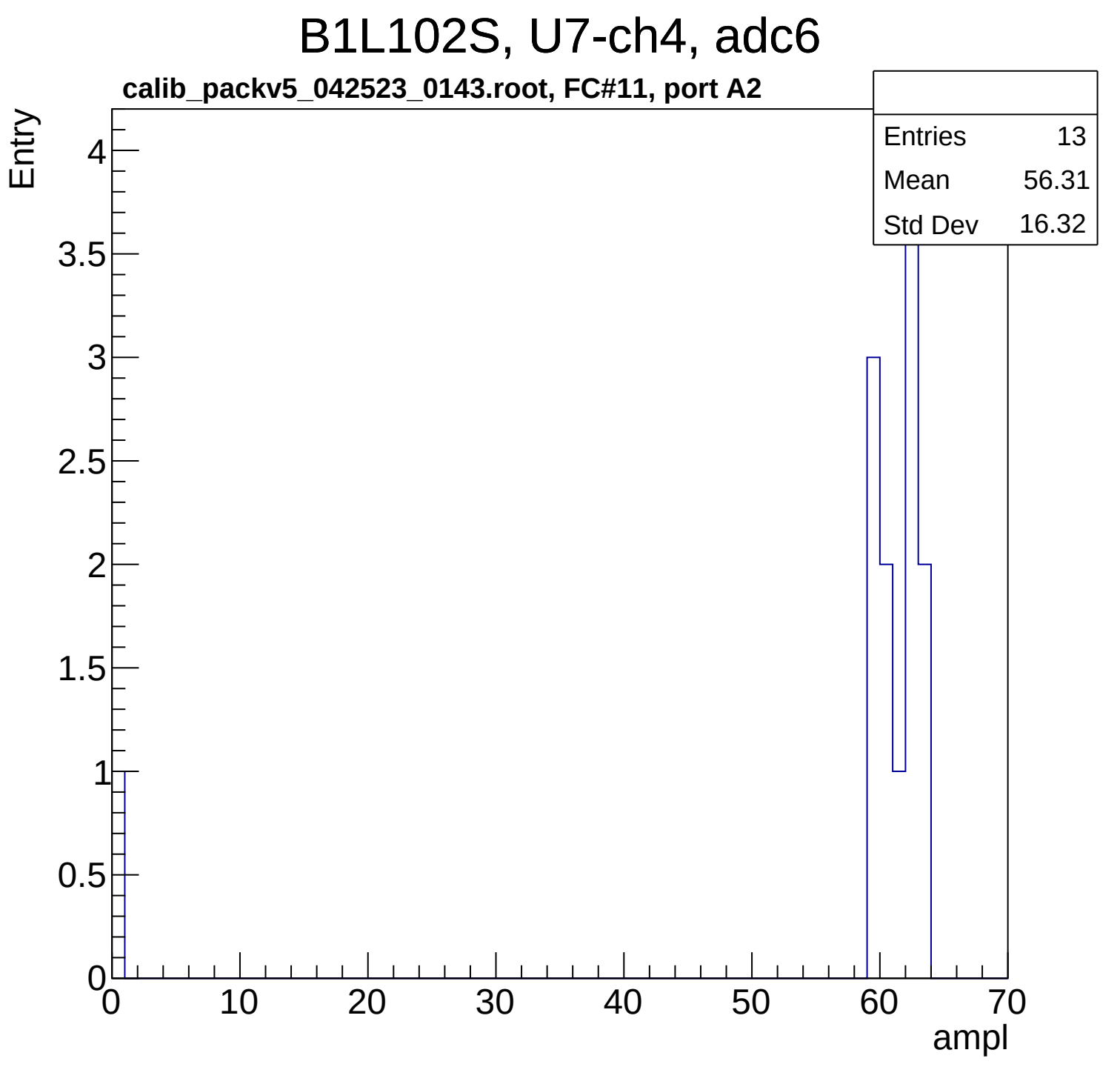
B1L102S, U7-ch4, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 13
Mean 56.31
Std Dev 16.32
Entry
ampl
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1.5
2
2.5
3
3.5
4
0
10
20
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40
50
60
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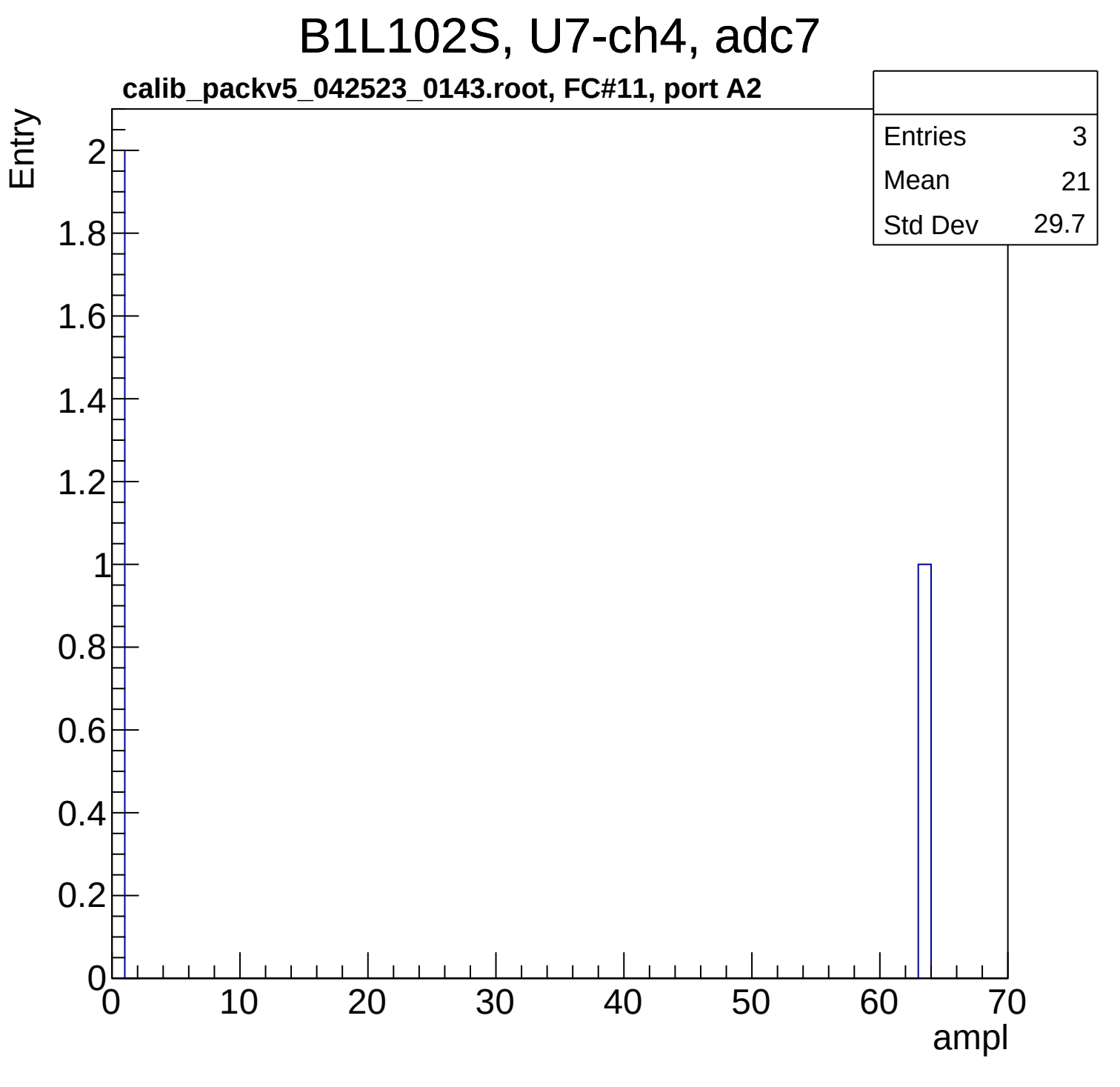
B1L102S, U7-ch4, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 3
Mean 21
Std Dev 29.7
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
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40
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60
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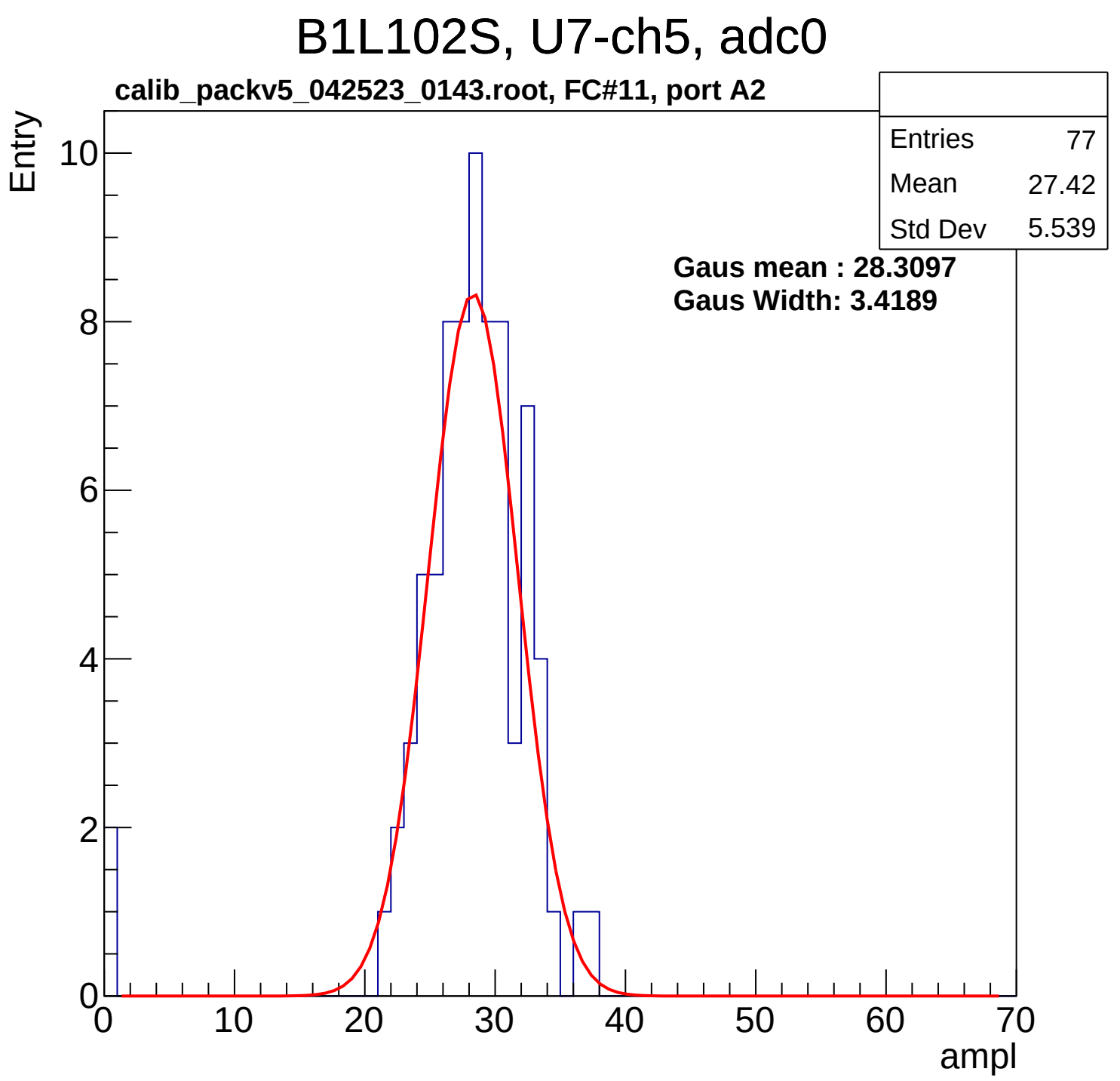
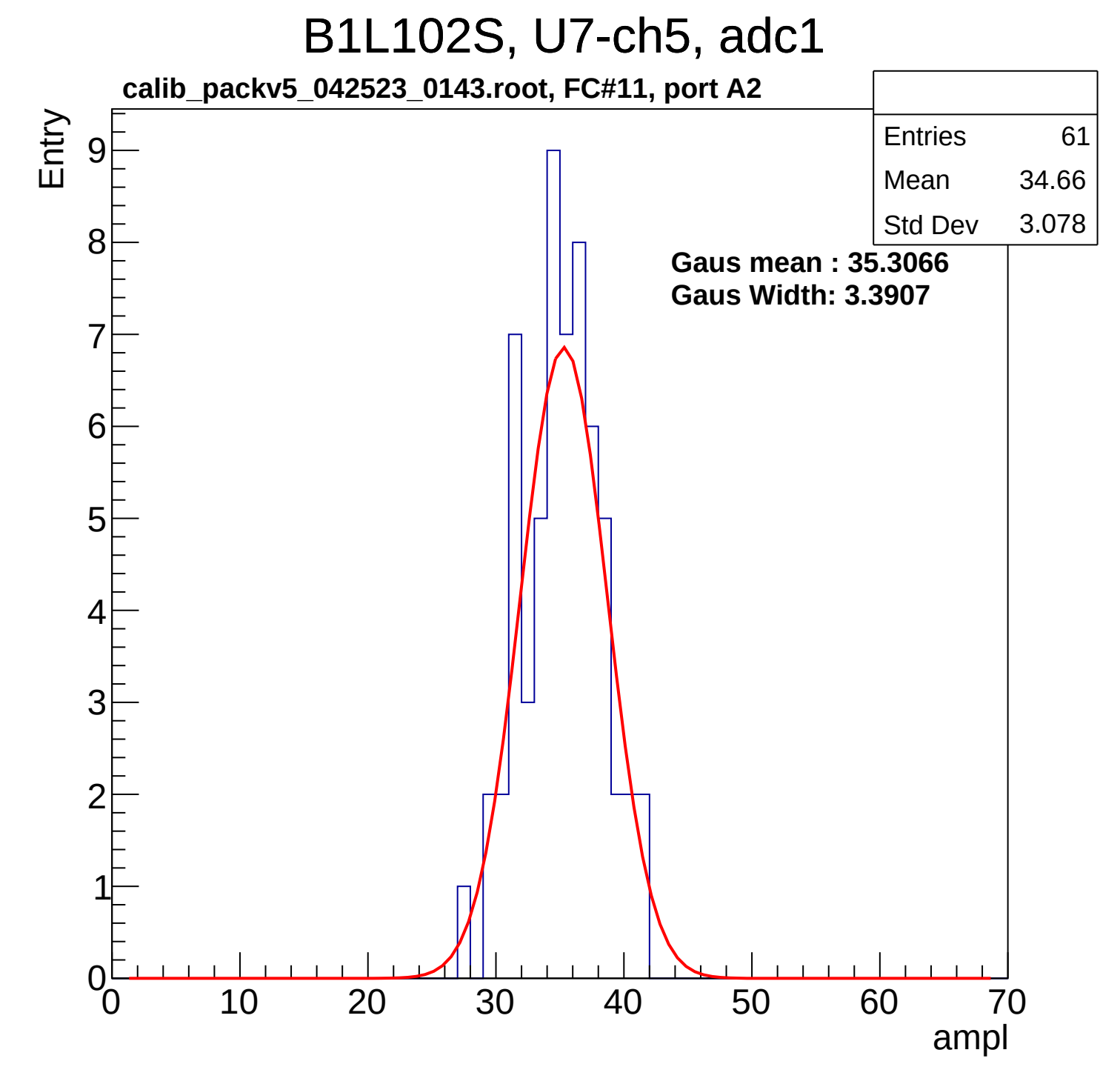

B1L102S, U7-ch5, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 77
Mean 27.42
Std Dev 5.539
Gaus mean : 28.3097
Gaus Width: 3.4189
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L102S, U7-ch5, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 61
Mean 34.66
Std Dev 3.078
Gaus mean : 35.3066
Gaus Width: 3.3907
Entry
ampl
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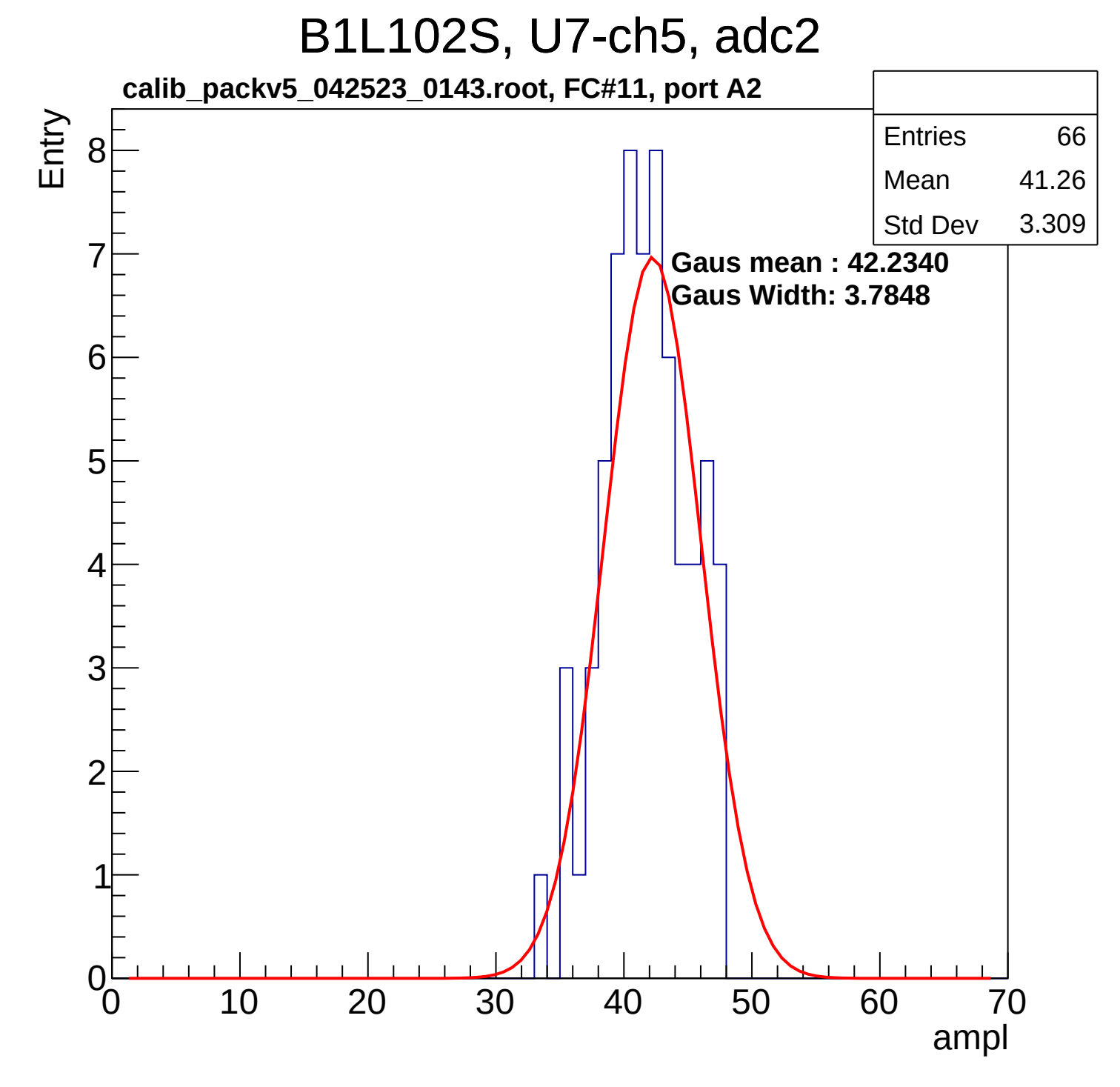
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9


B1L102S, U7-ch5, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 66
Mean 41.26
Std Dev 3.309
Gaus mean : 42.2340
Gaus Width: 3.7848
Entry
ampl
0
1
2
3
4
5
6
7
8
0
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20
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40
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60
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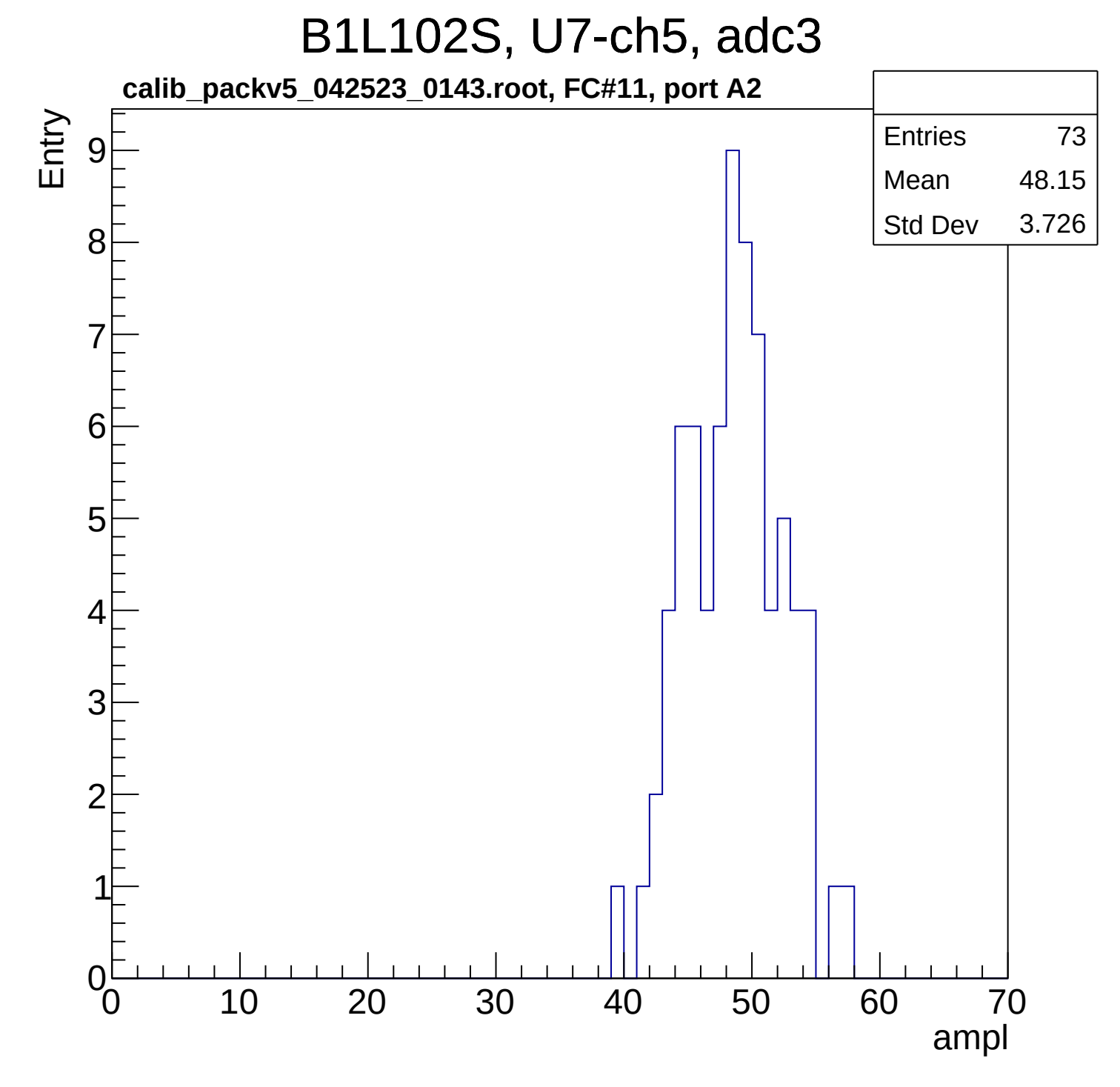
B1L102S, U7-ch5, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 73
Mean 48.15
Std Dev 3.726
Entry
ampl
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2
3
4
5
6
7
8
9
0
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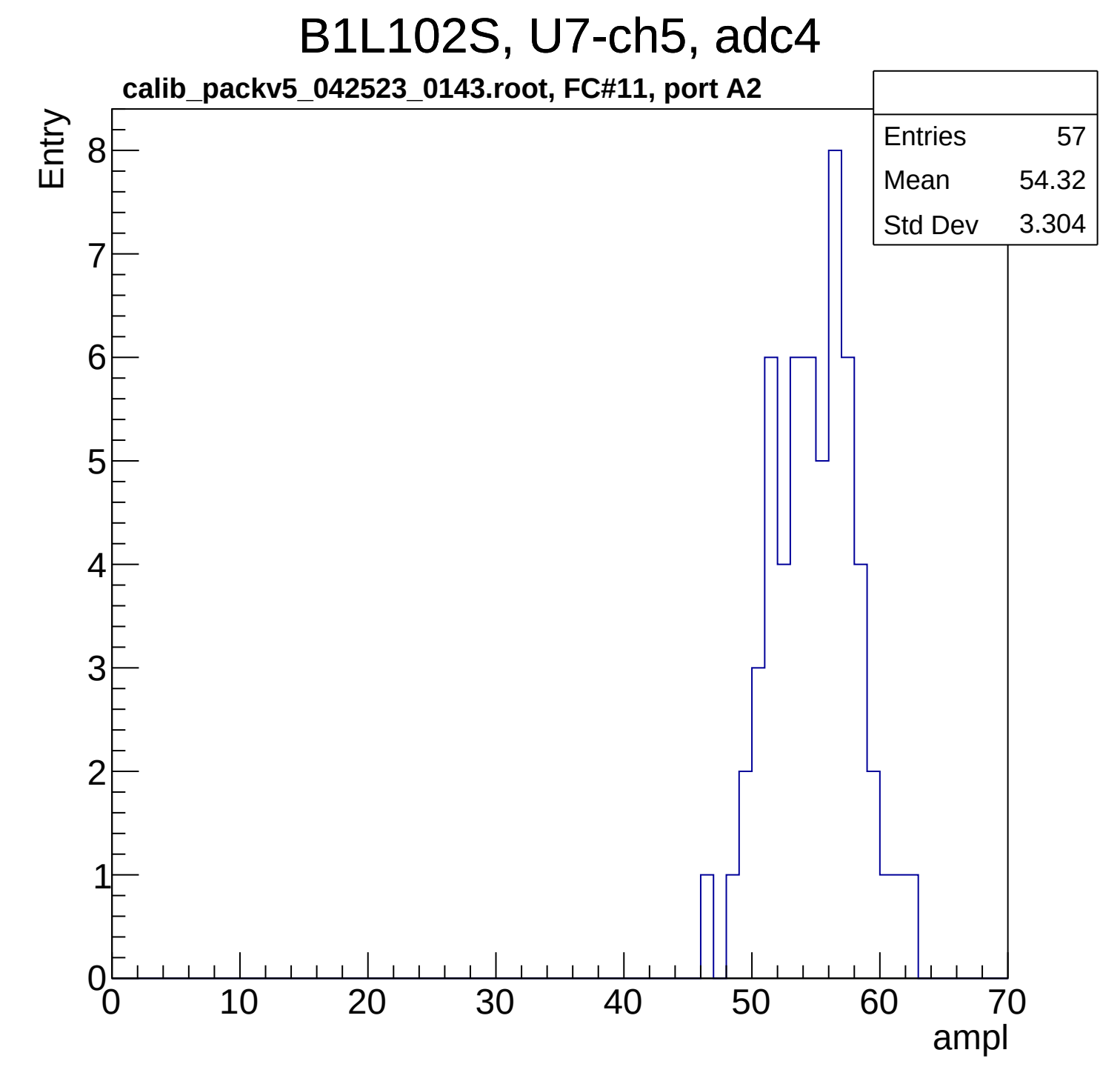
B1L102S, U7-ch5, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 57
Mean 54.32
Std Dev 3.304
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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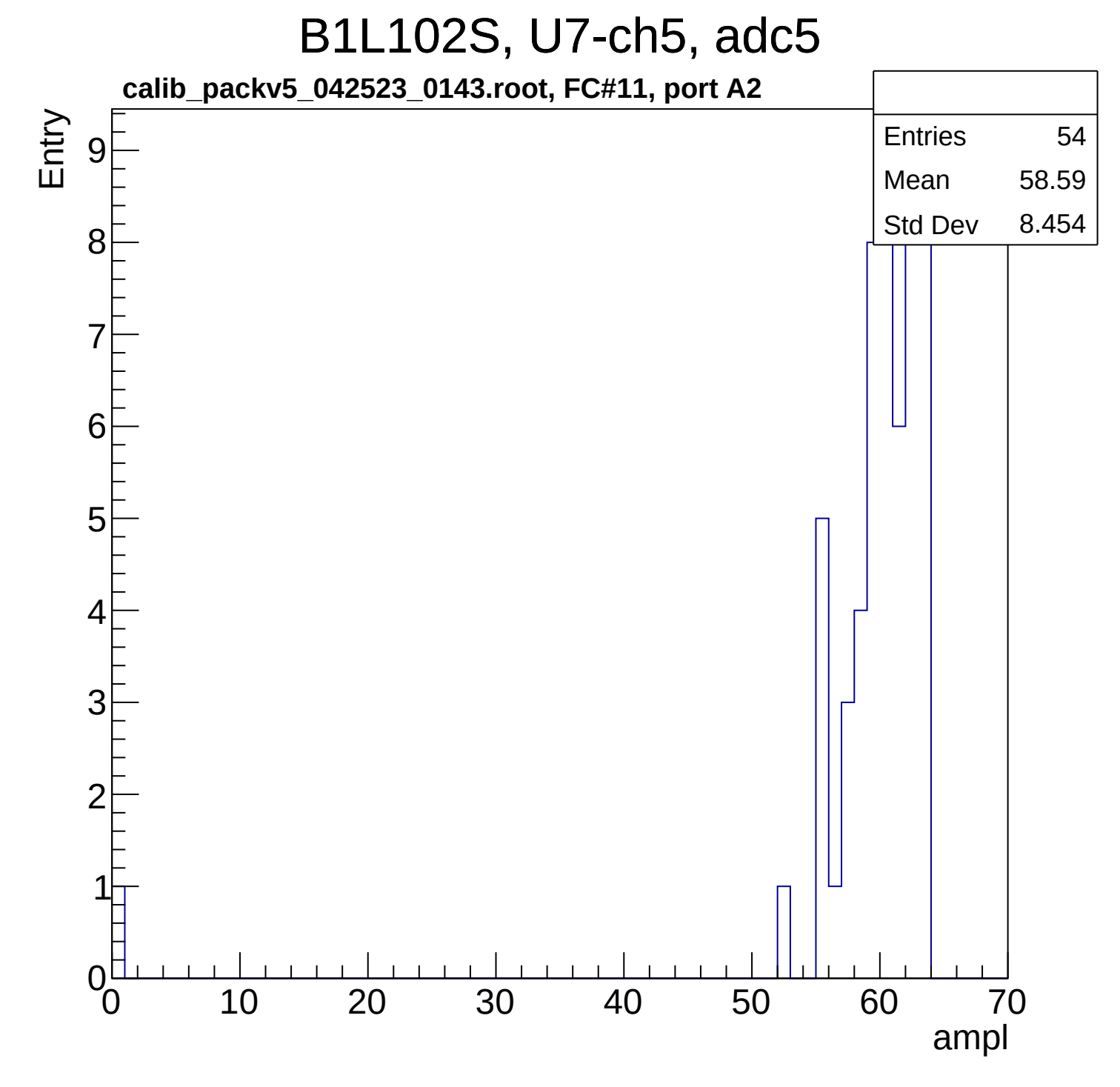
B1L102S, U7-ch5, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 54
Mean 58.59
Std Dev 8.454
Entry
ampl
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10
20
30
40
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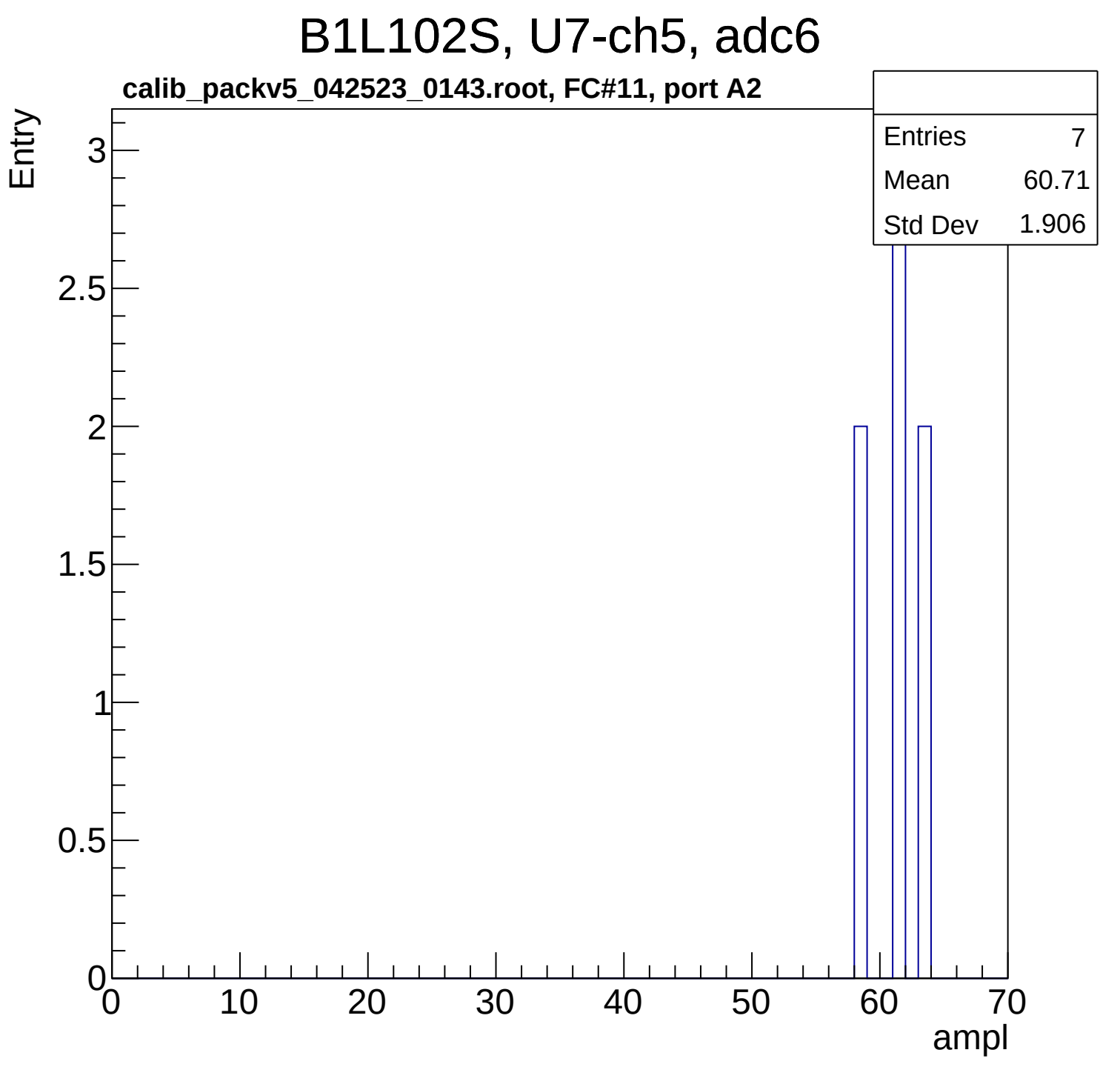
60
70
1
2
3
4
5
6
7
8
9


B1L102S, U7-ch5, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 7
Mean 60.71
Std Dev 1.906
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
10
20
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40
50
60
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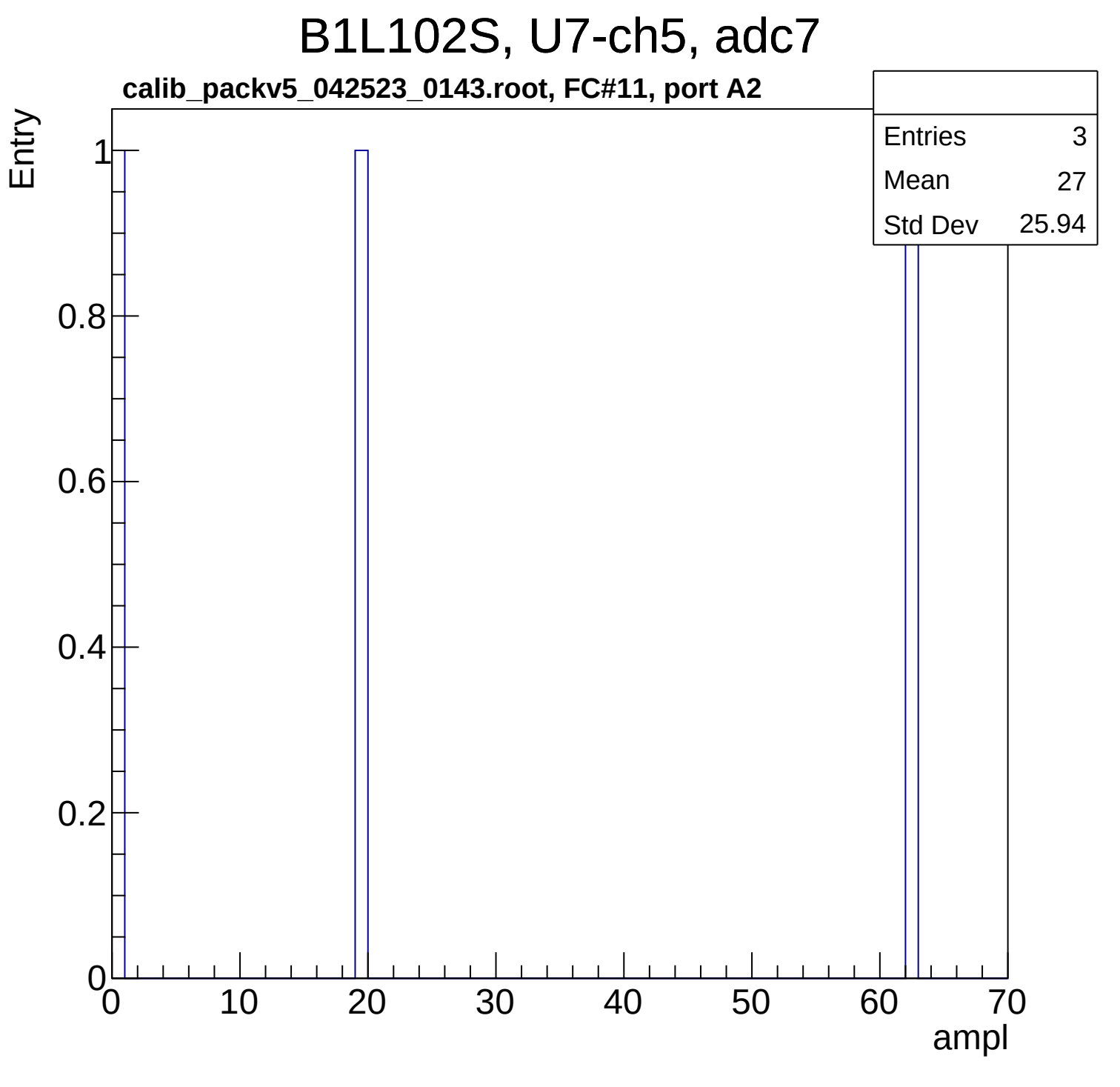
B1L102S, U7-ch5, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 3
Mean 27
Std Dev 25.94
Entry
ampl
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0.4
0.6
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1
0
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40
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60
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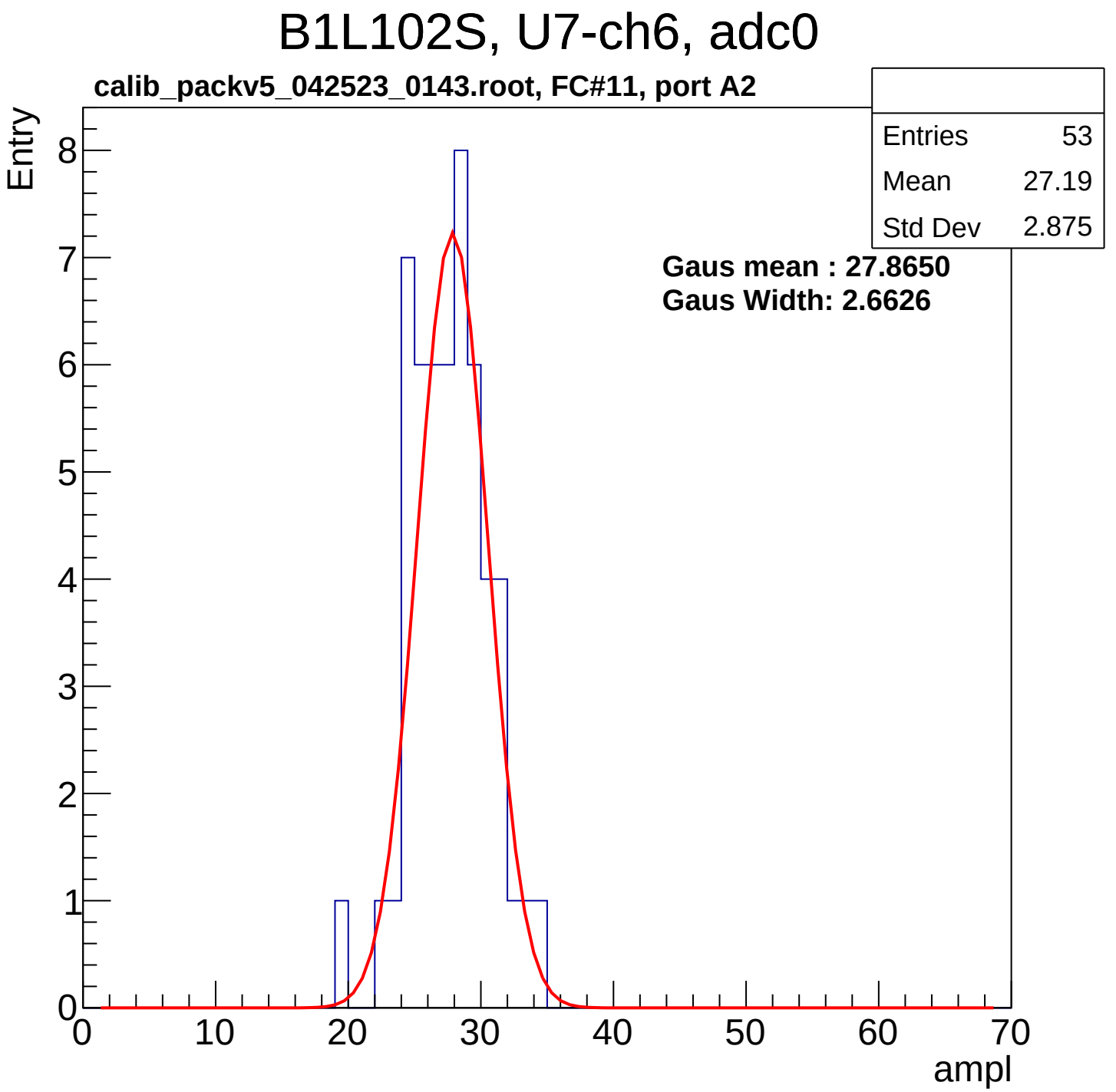
B1L102S, U7-ch6, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 53
Mean 27.19
Std Dev 2.875
Gaus mean : 27.8650
Gaus Width: 2.6626
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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60
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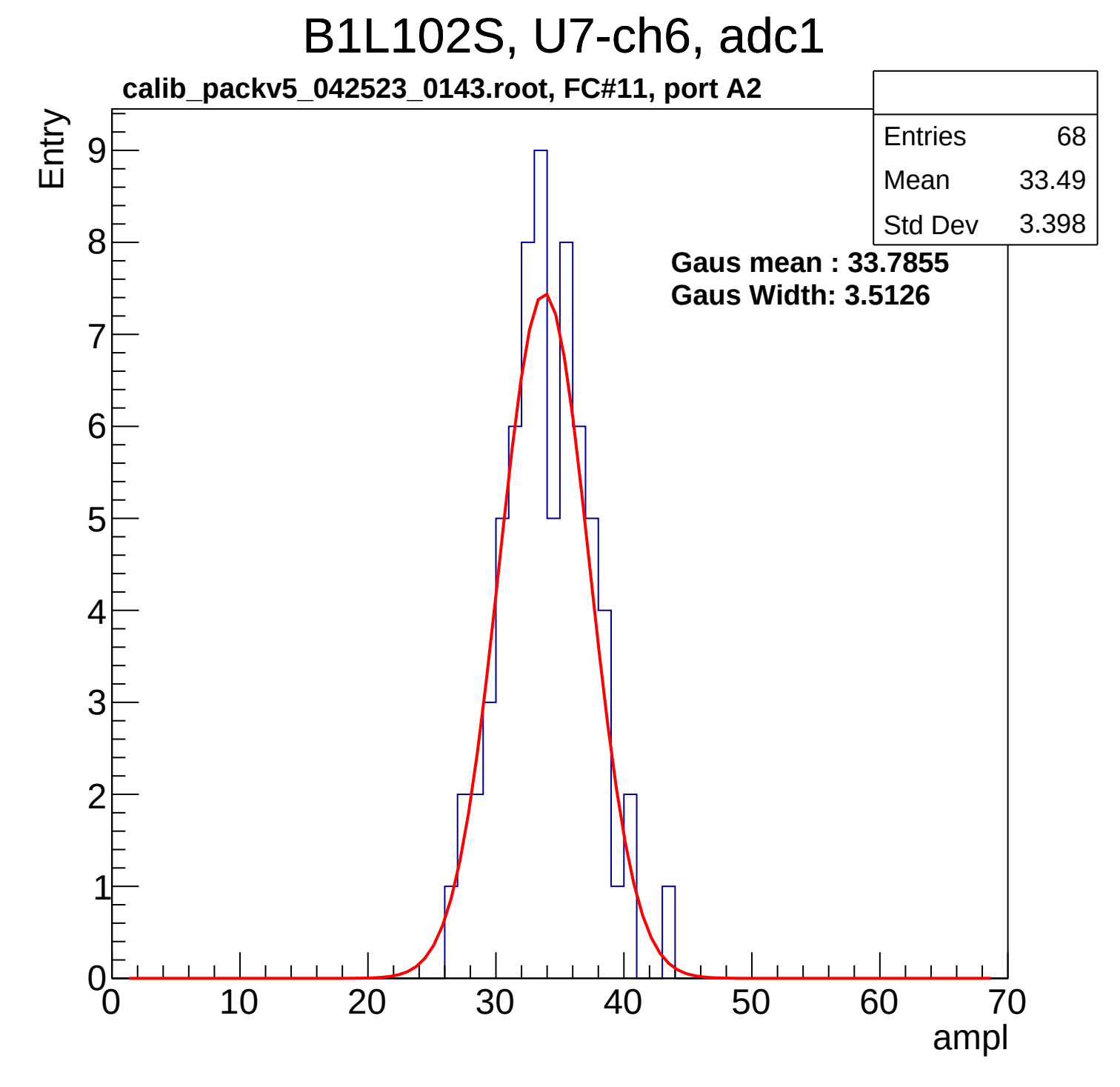
B1L102S, U7-ch6, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 68
Mean 33.49
Std Dev 3.398
Gaus mean : 33.7855
Gaus Width: 3.5126
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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60
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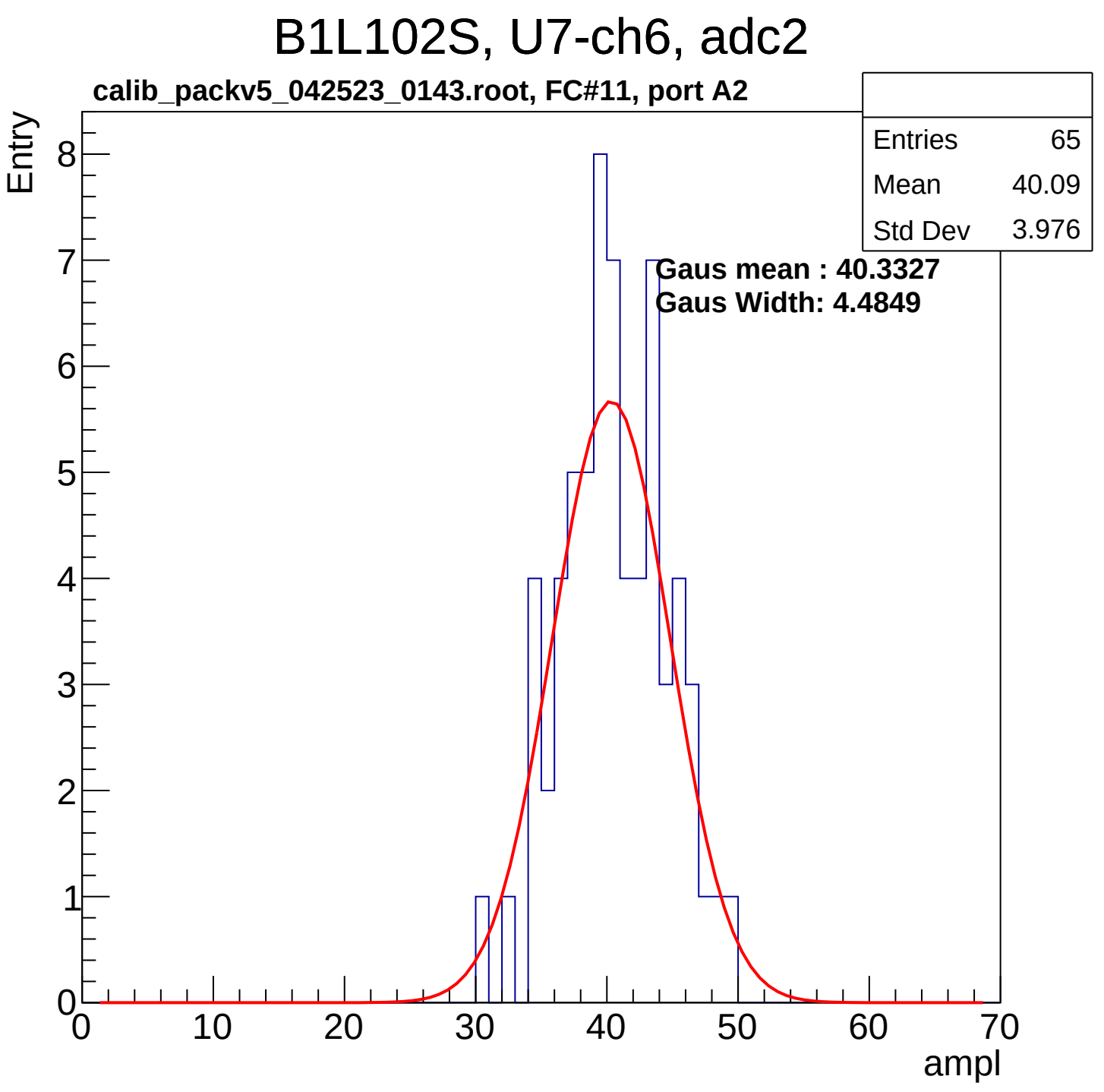
B1L102S, U7-ch6, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 65
Mean 40.09
Std Dev 3.976
Gaus mean : 40.3327
Gaus Width: 4.4849
Entry
ampl
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2
3
4
5
6
7
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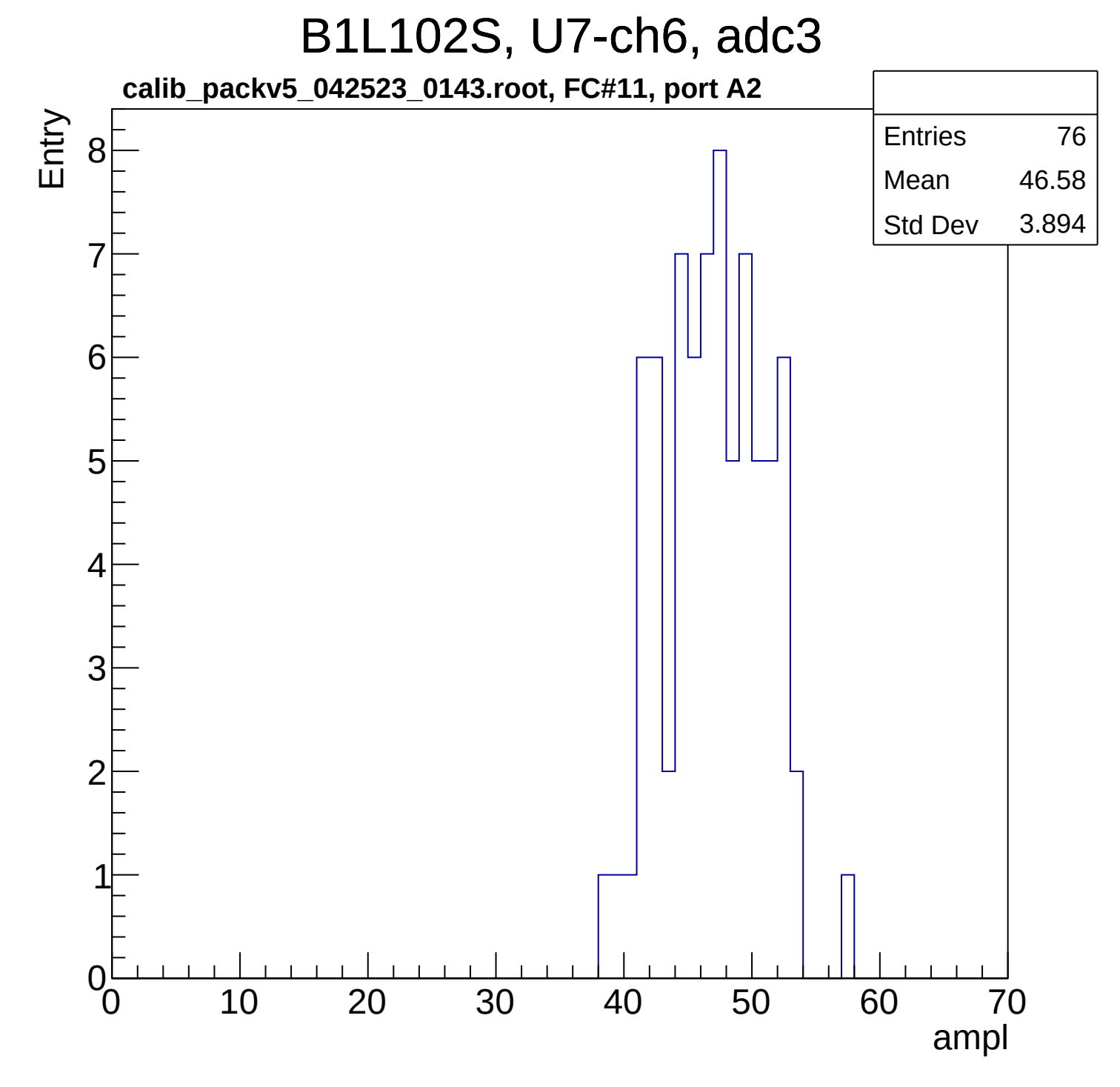
B1L102S, U7-ch6, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 76
Mean 46.58
Std Dev 3.894
Entry
ampl
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6
7
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0
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20
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60
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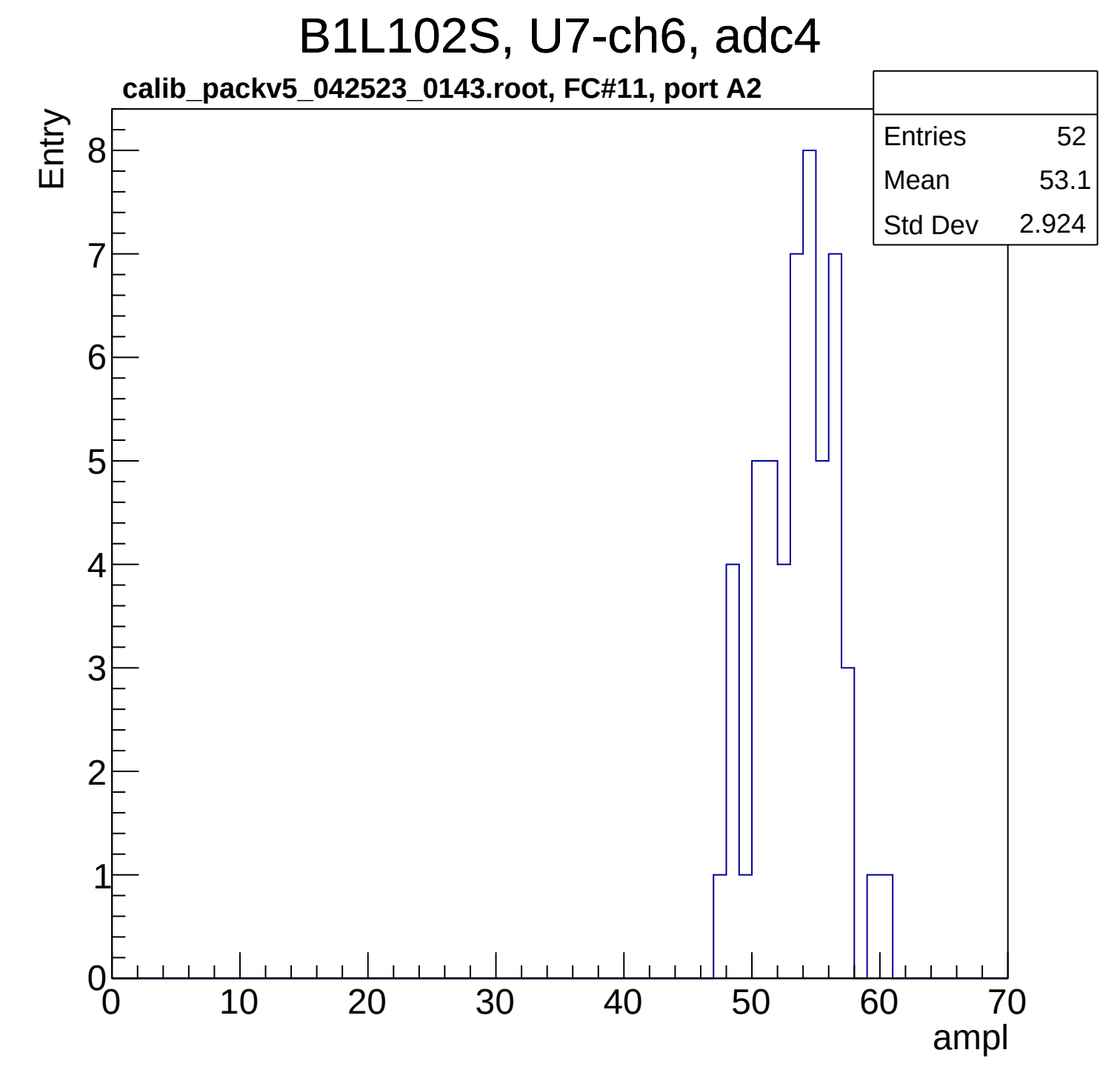
B1L102S, U7-ch6, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 52
Mean 53.1
Std Dev 2.924
Entry
ampl
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4
5
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7
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20
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40
50
60
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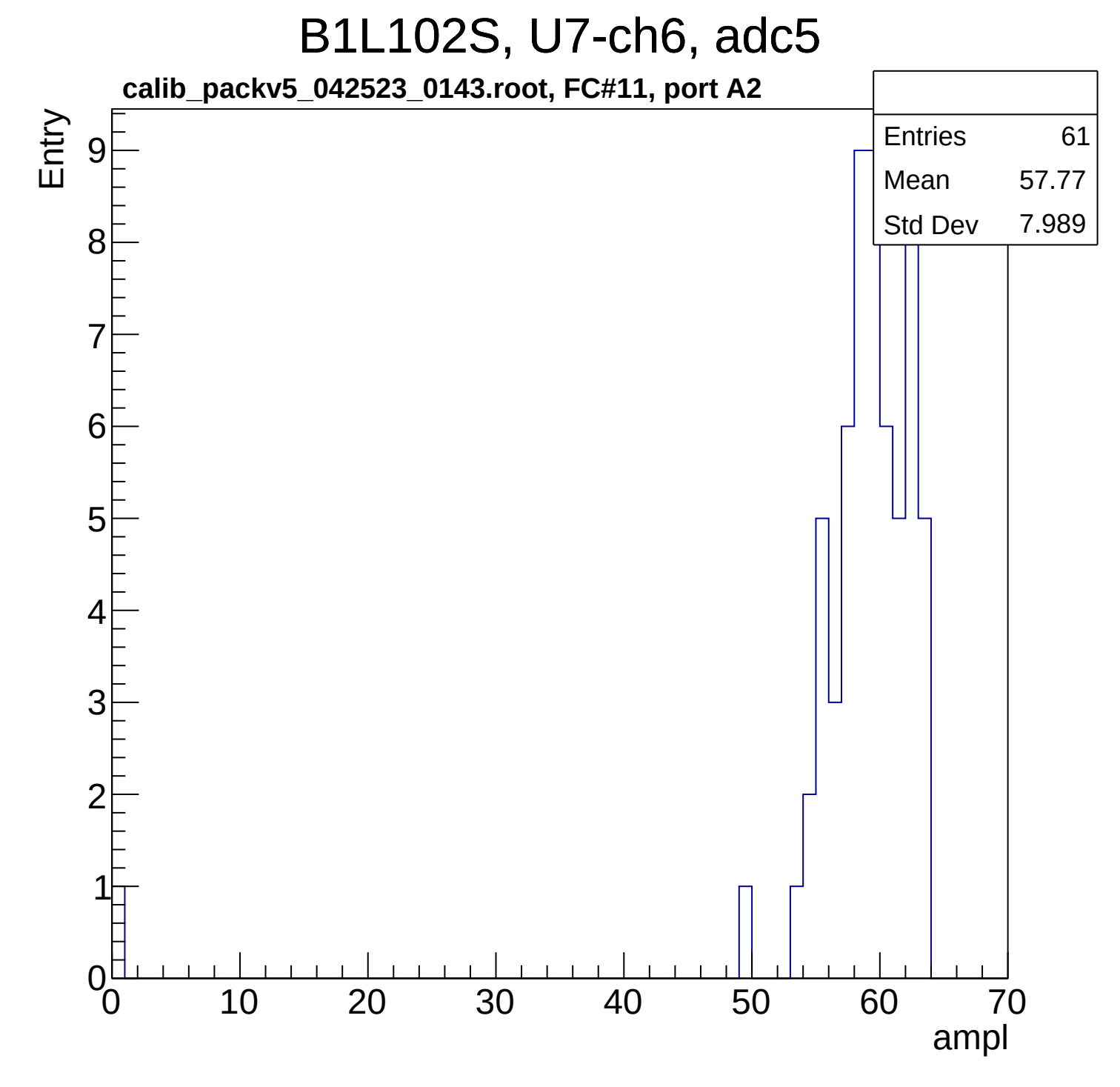
B1L102S, U7-ch6, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 61
Mean 57.77
Std Dev 7.989
Entry
ampl
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3
4
5
6
7
8
9
0
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20
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40
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60
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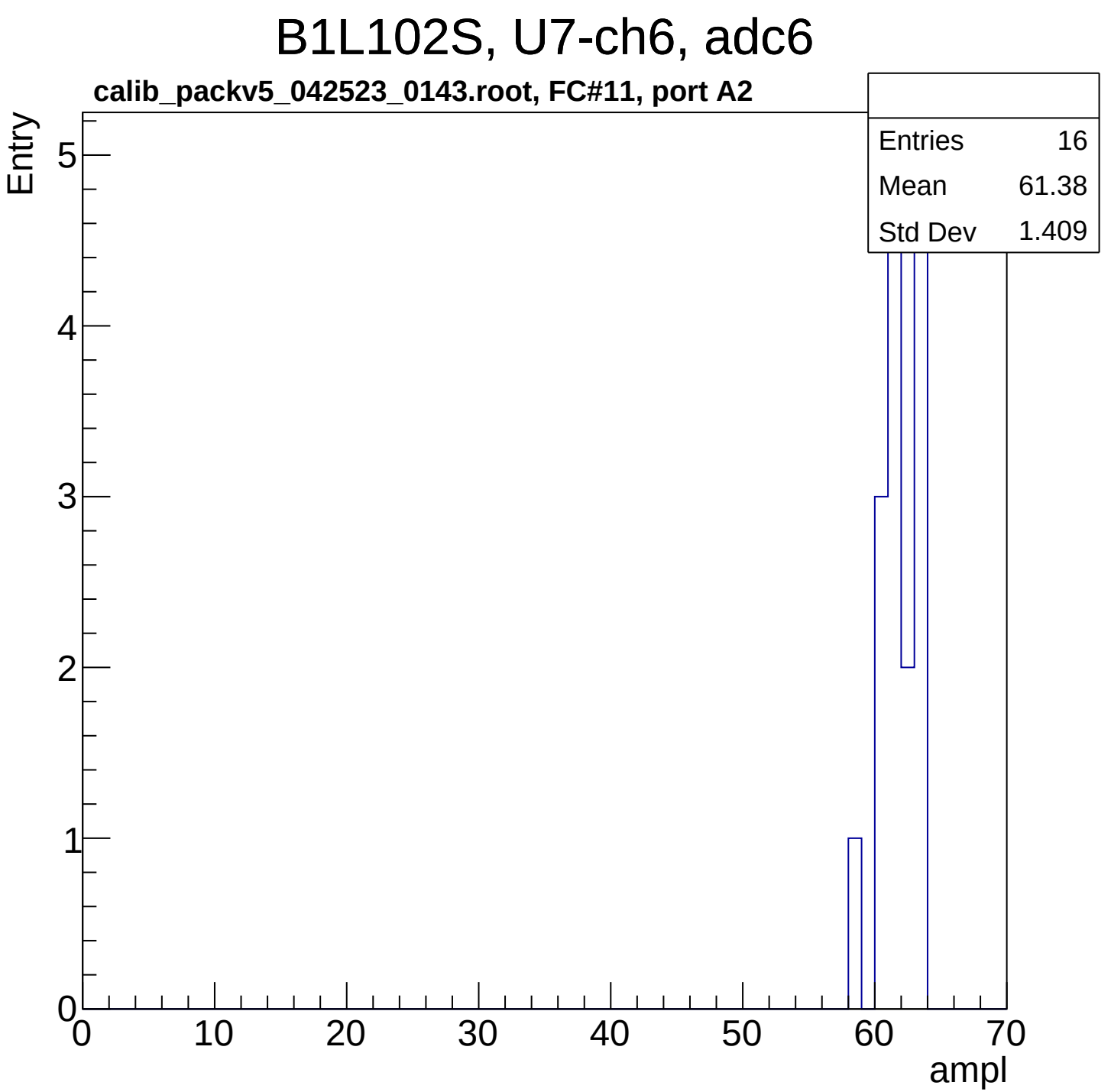
B1L102S, U7-ch6, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 16
Mean 61.38
Std Dev 1.409
Entry
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3
4
5
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10
20
30
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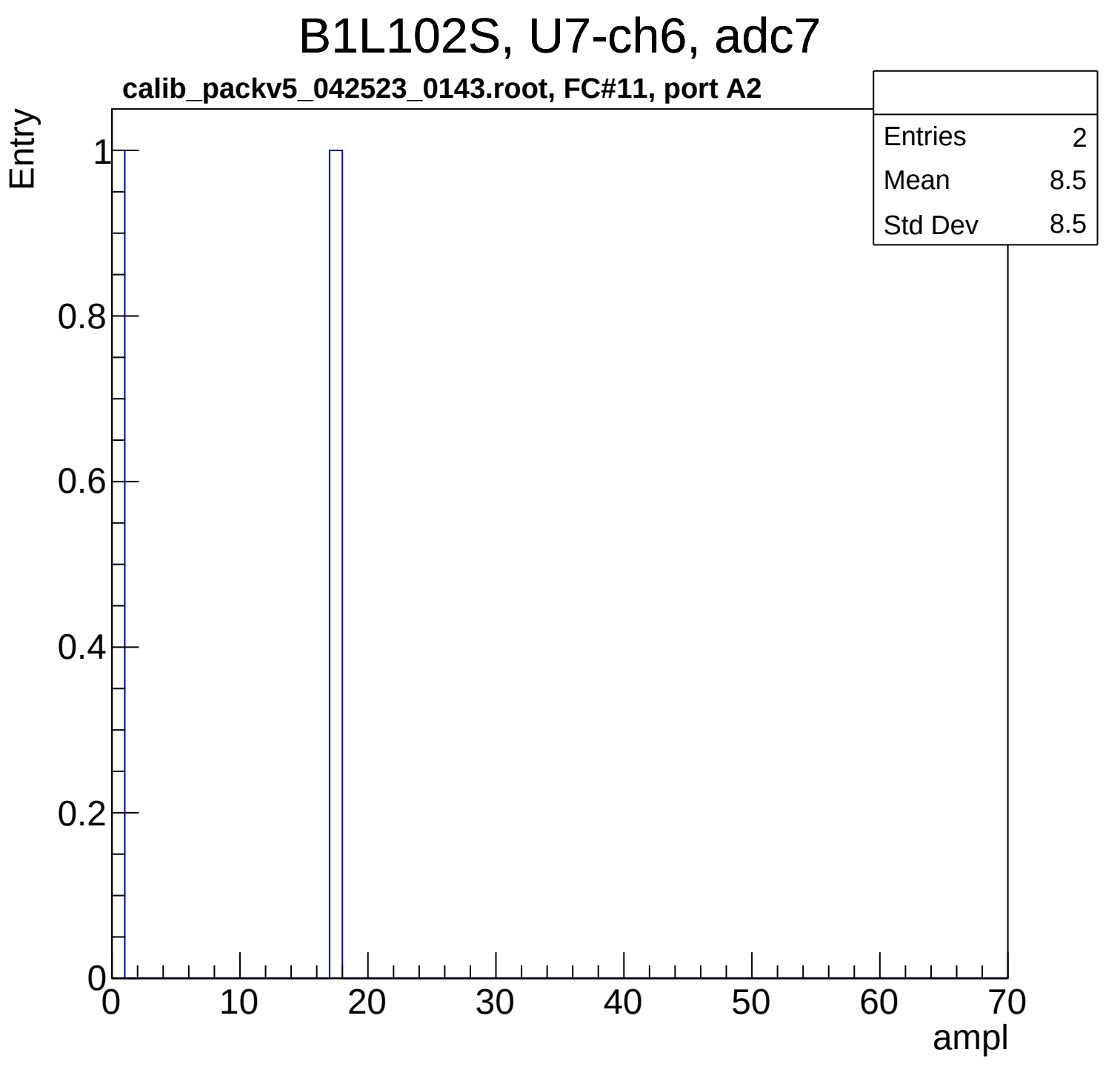
50
60
70
ampl


B1L102S, U7-ch6, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 2
Mean 8.5
Std Dev 8.5
Entry
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0.6
0.4
0.2
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10
20
30
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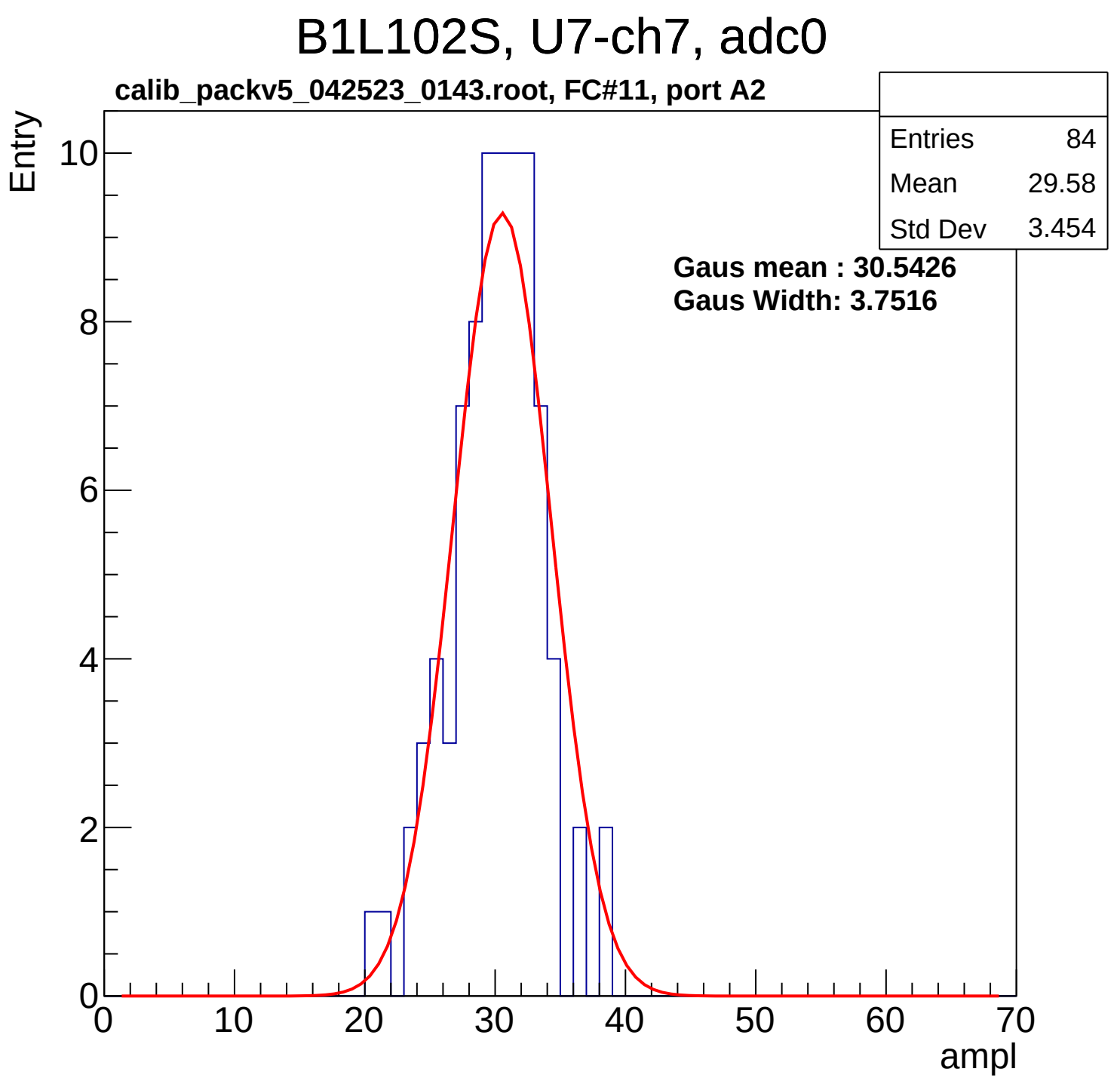
50
60
70
ampl


B1L102S, U7-ch7, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 84
Mean 29.58
Std Dev 3.454
Gaus mean : 30.5426
Gaus Width: 3.7516
Entry
ampl
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0
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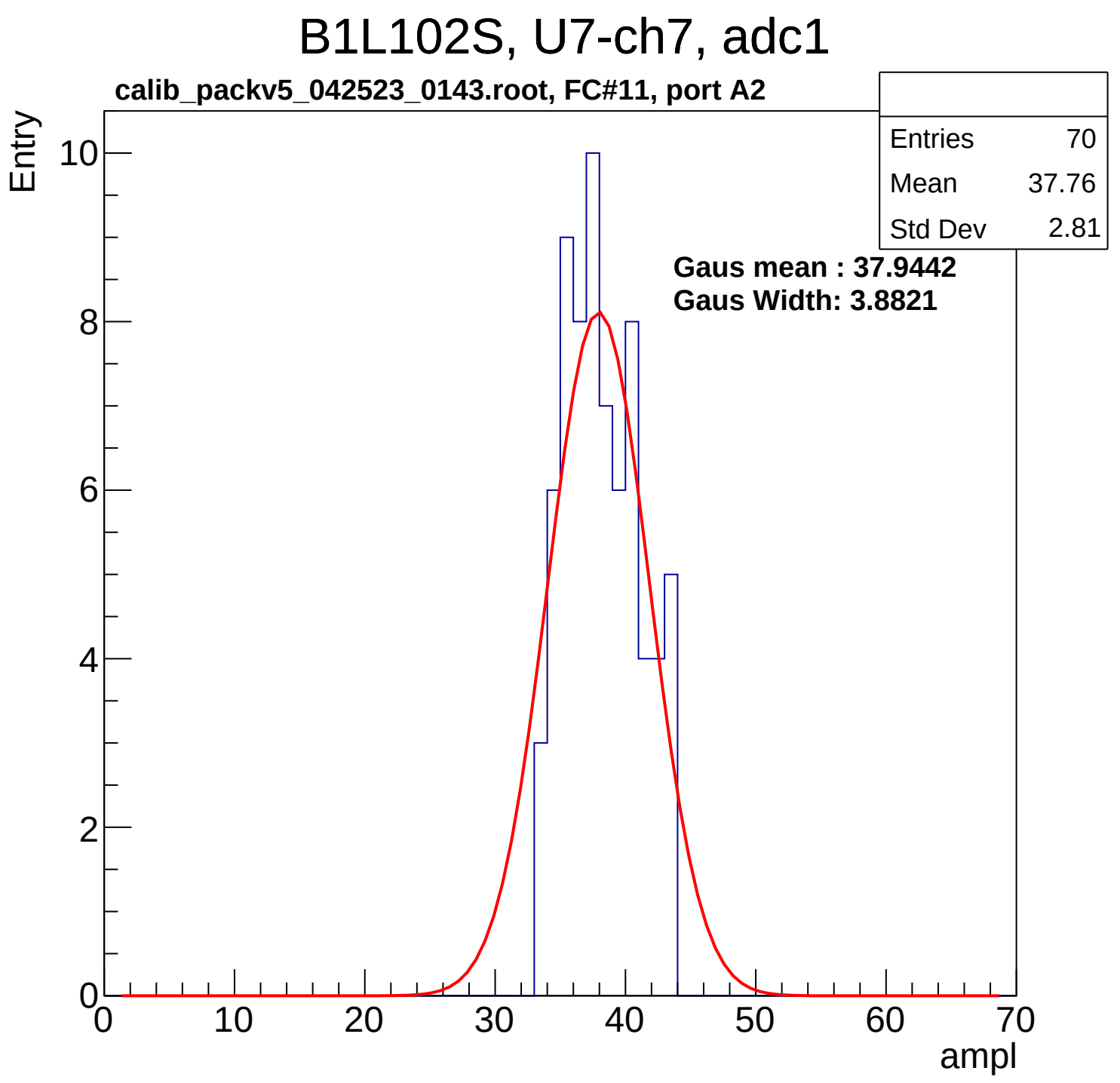
B1L102S, U7-ch7, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 70
Mean 37.76
Std Dev 2.81
Gaus mean : 37.9442
Gaus Width: 3.8821
Entry
ampl
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4
6
8
10
0
10
20
30
40
50
60
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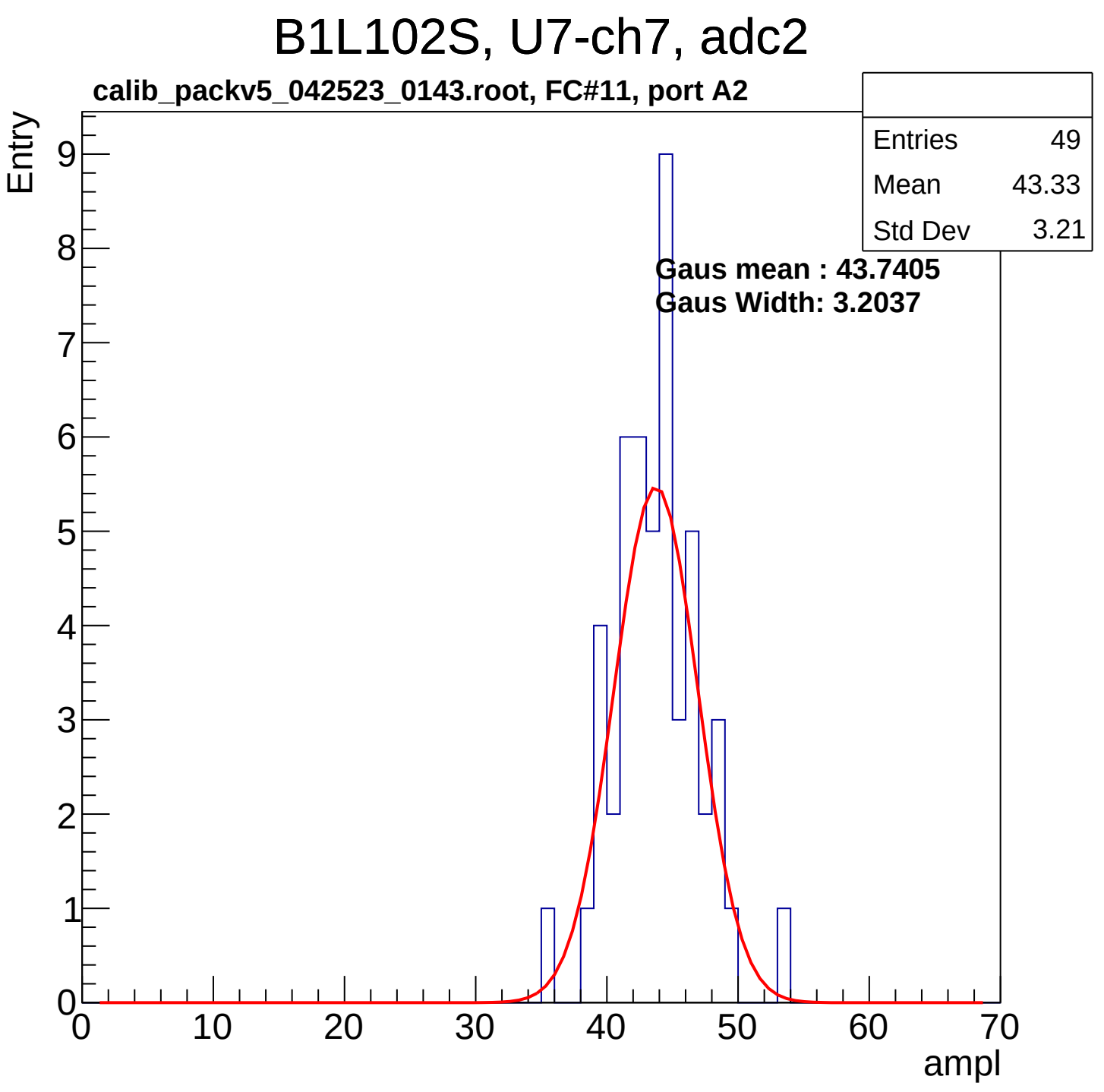
B1L102S, U7-ch7, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 49
Mean 43.33
Std Dev 3.21
Gaus mean : 43.7405
Gaus Width: 3.2037
Entry
ampl
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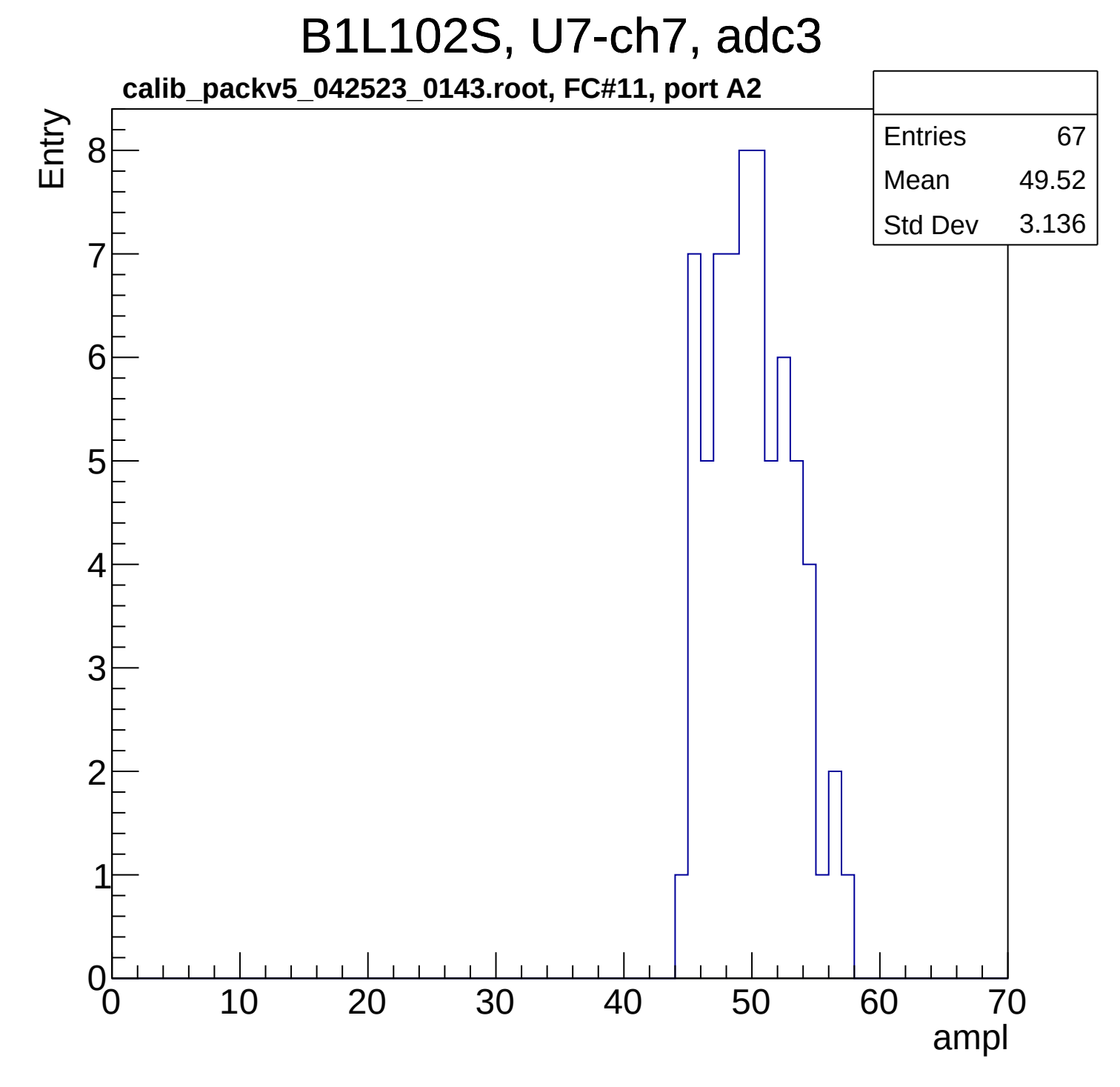
B1L102S, U7-ch7, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 67
Mean 49.52
Std Dev 3.136
Entry
ampl
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3
4
5
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7
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60
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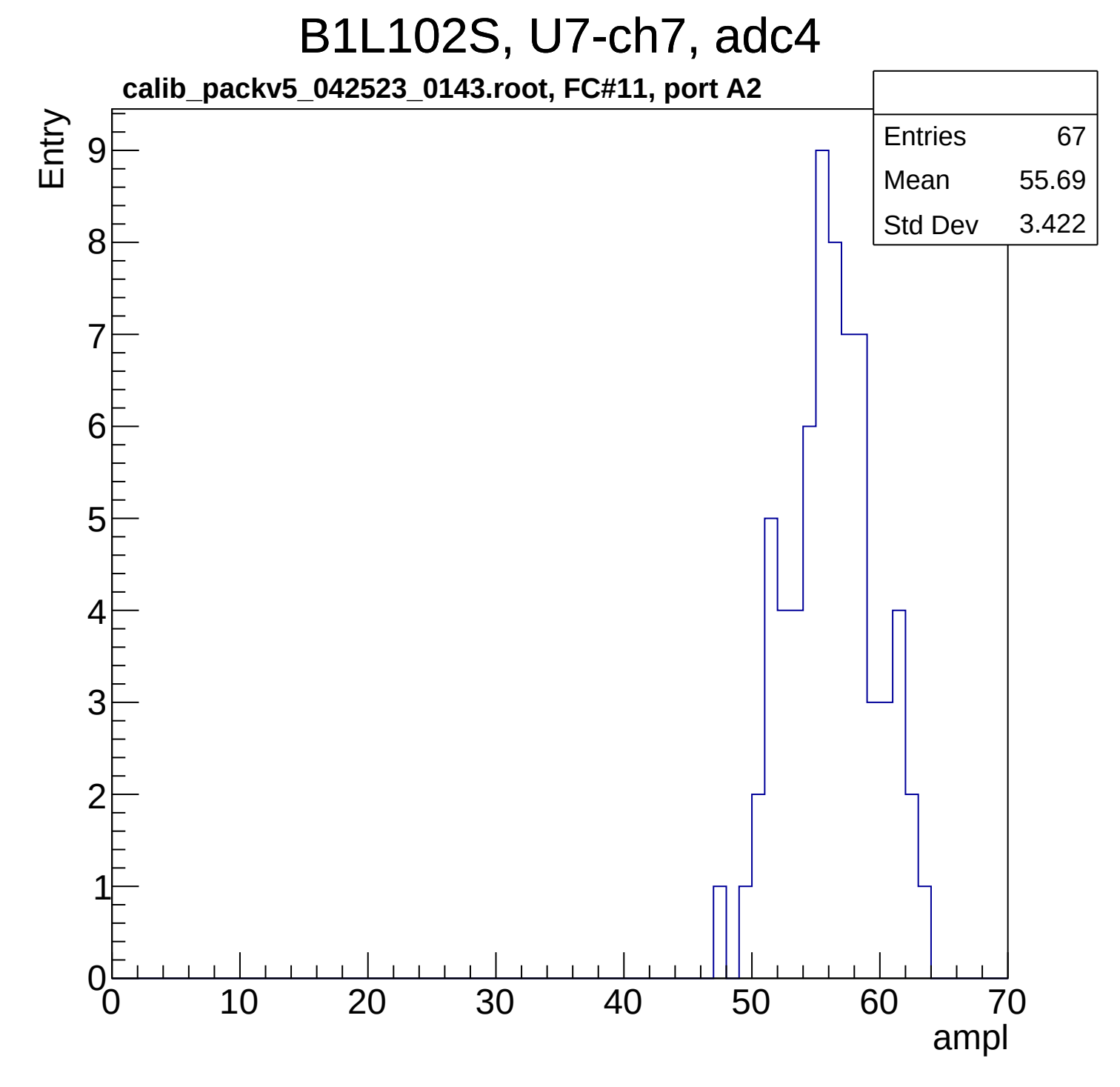
B1L102S, U7-ch7, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 67
Mean 55.69
Std Dev 3.422
Entry
ampl
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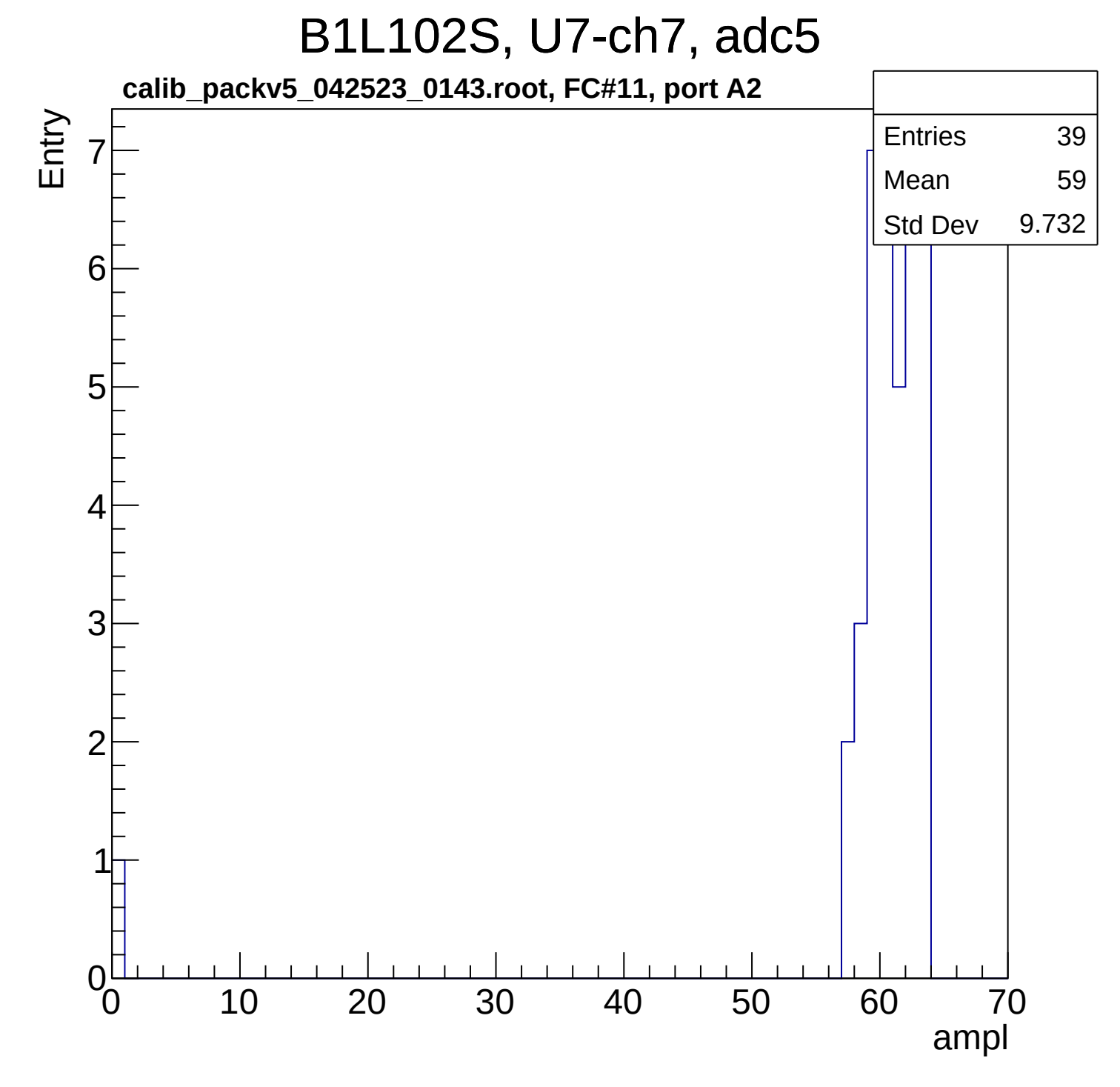
B1L102S, U7-ch7, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 39
Mean 59
Std Dev 9.732
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
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60
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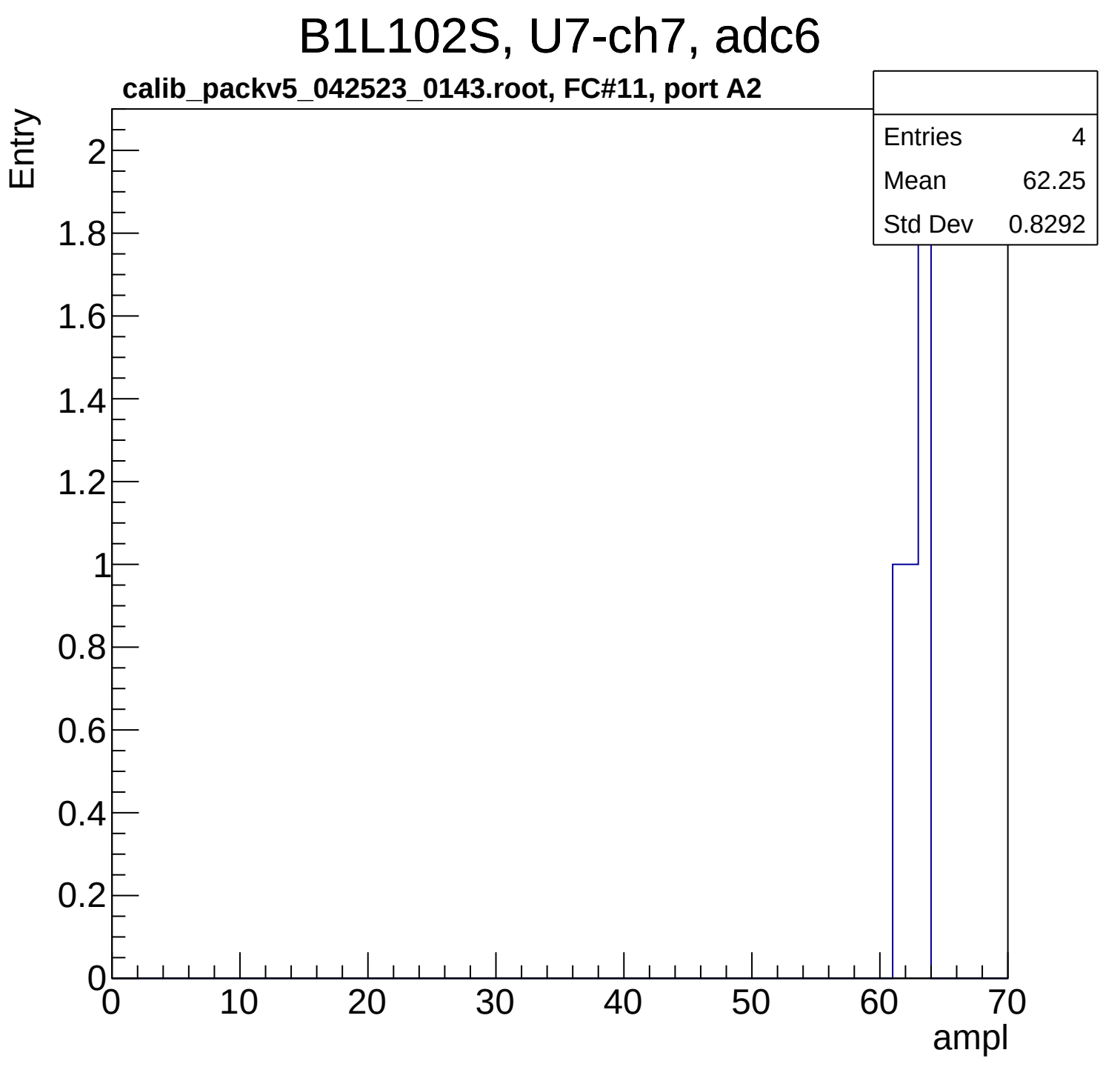
B1L102S, U7-ch7, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 4
Mean 62.25
Std Dev 0.8292
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
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40
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60
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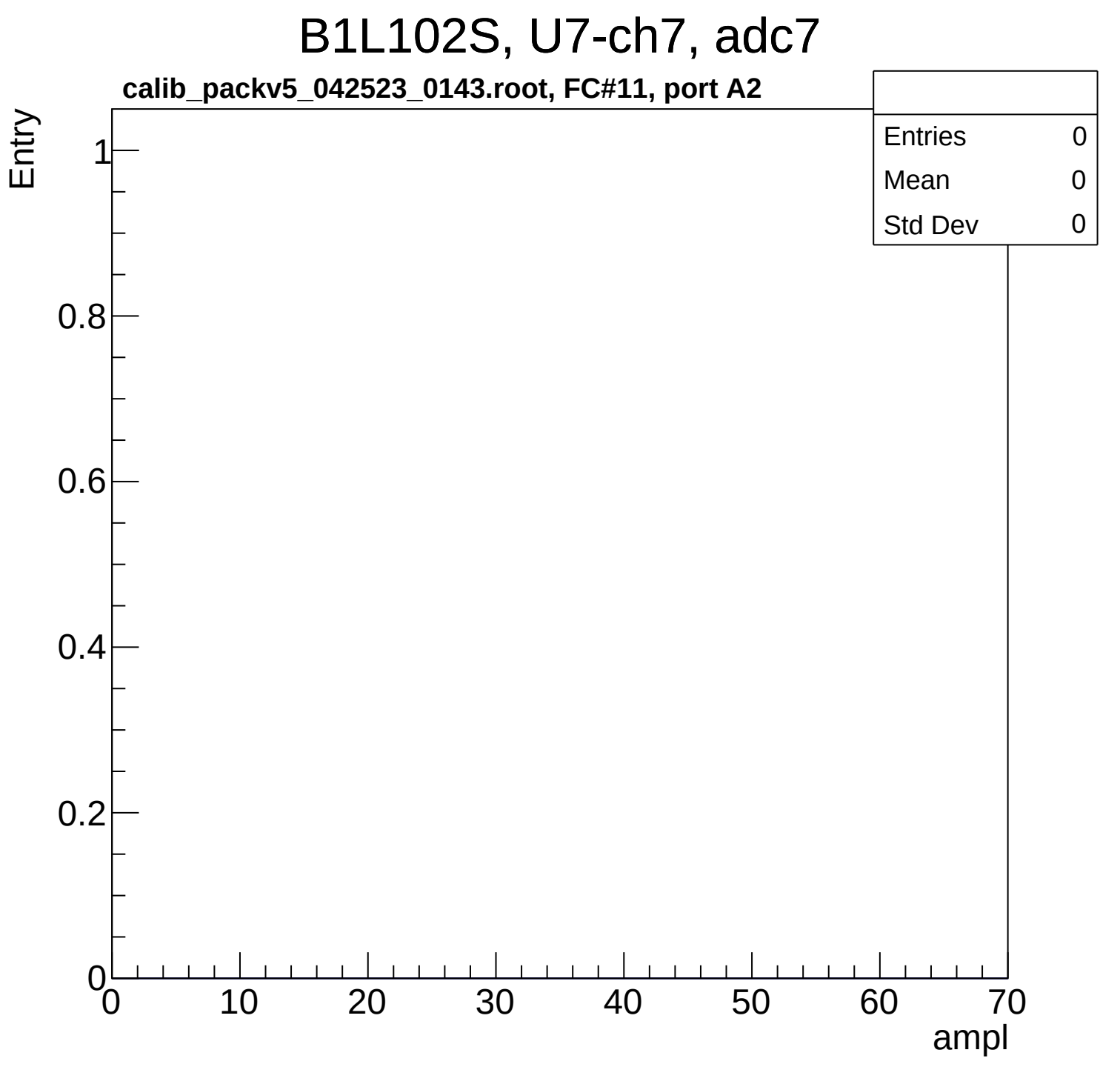
B1L102S, U7-ch7, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 0
Mean 0
Std Dev 0
Entry
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0.8
0.6
0.4
0.2
0
0
10
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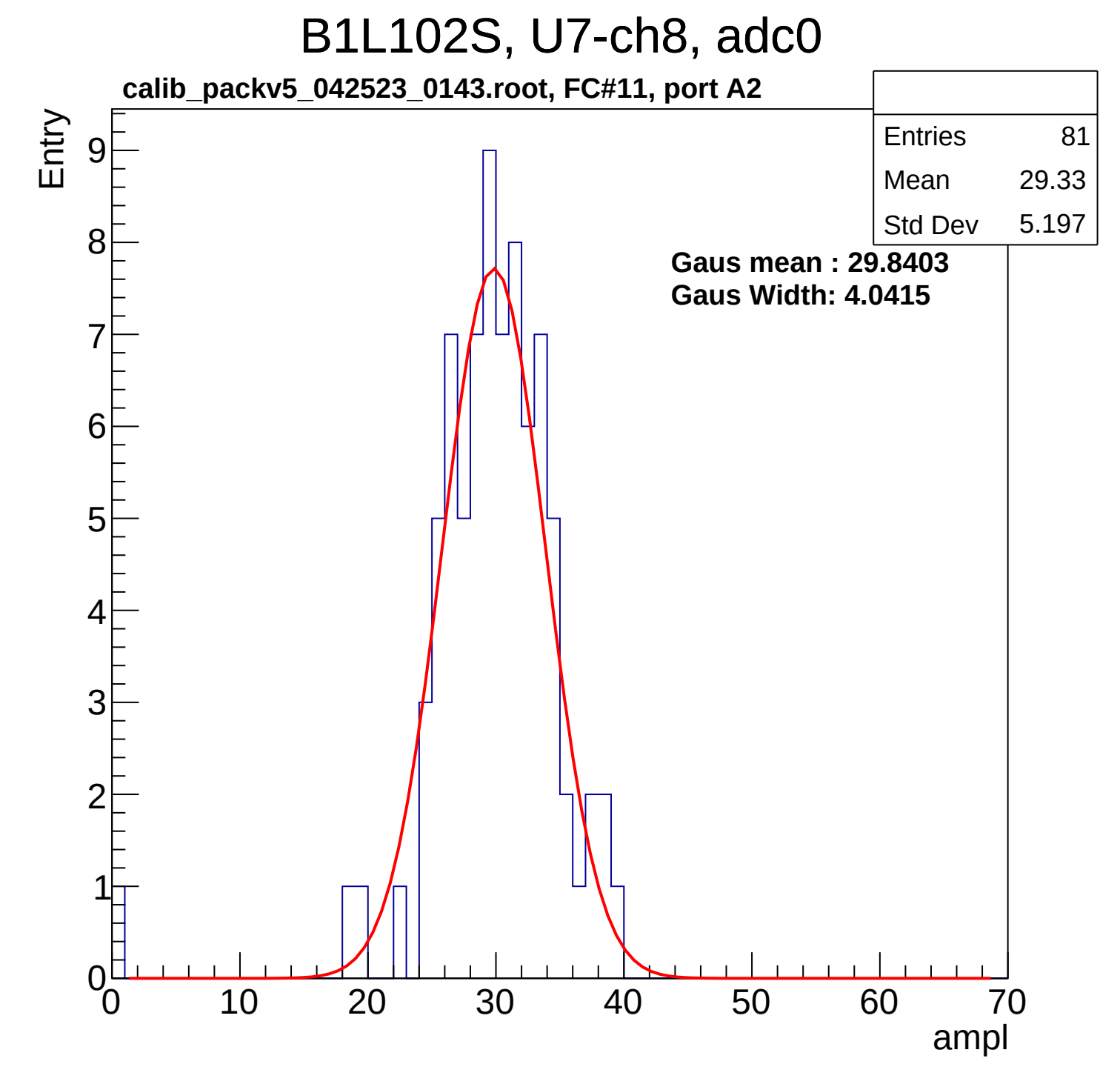
30
40
50
60
70
ampl


B1L102S, U7-ch8, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 81
Mean 29.33
Std Dev 5.197
Gaus mean : 29.8403
Gaus Width: 4.0415
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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40
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60
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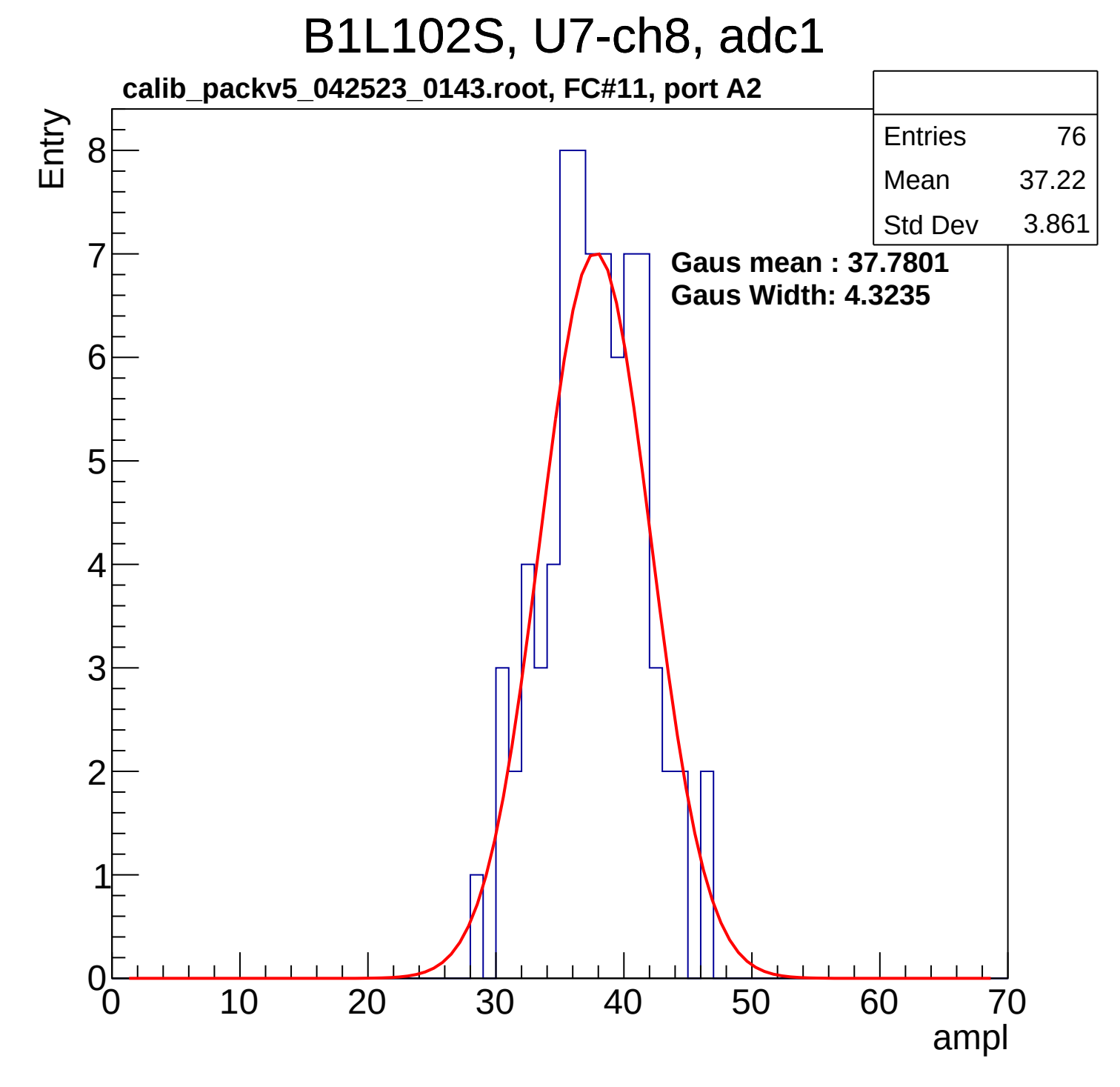
B1L102S, U7-ch8, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 76
Mean 37.22
Std Dev 3.861
Gaus mean : 37.7801
Gaus Width: 4.3235
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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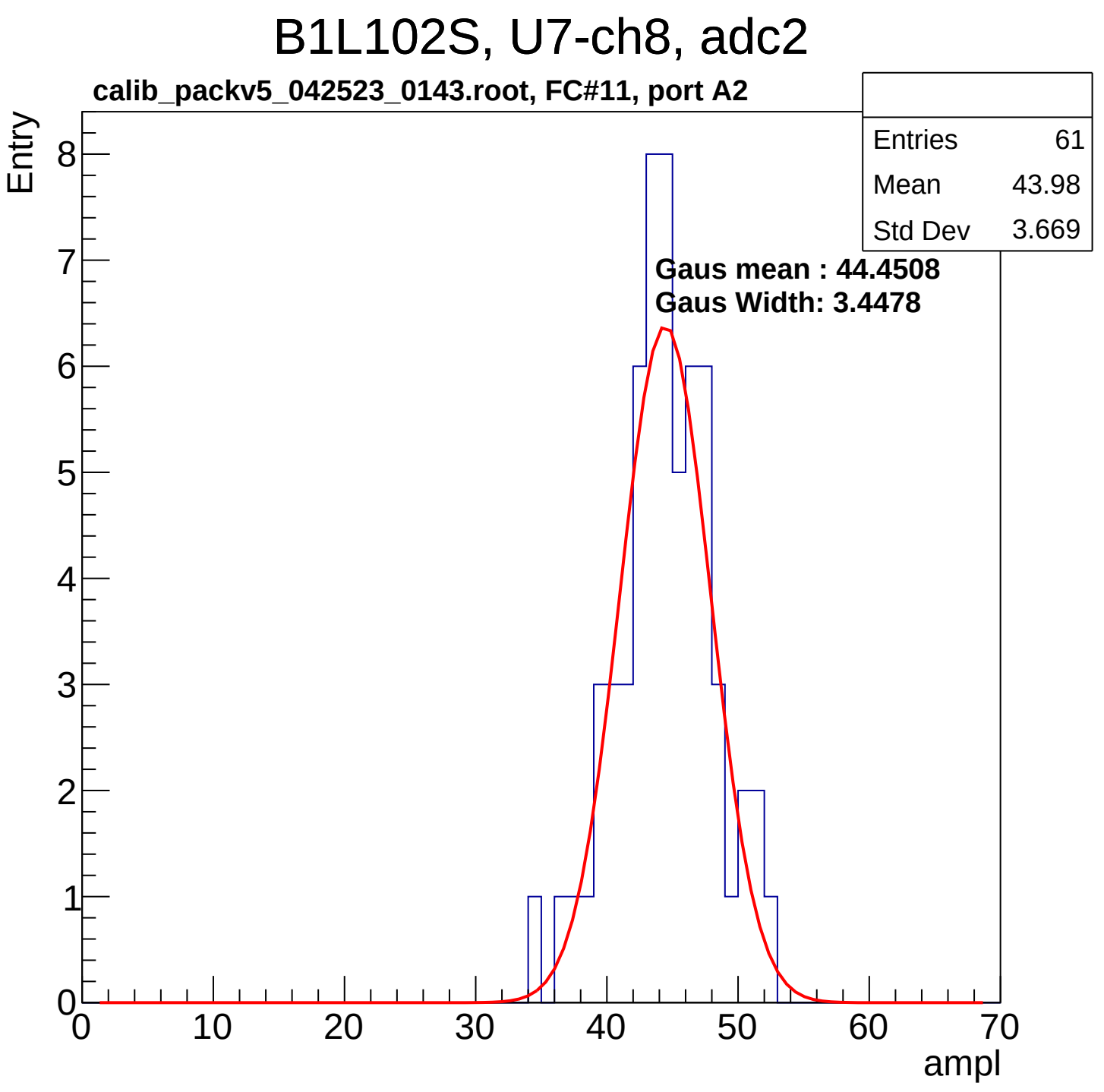
B1L102S, U7-ch8, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 61
Mean 43.98
Std Dev 3.669
Gaus mean : 44.4508
Gaus Width: 3.4478
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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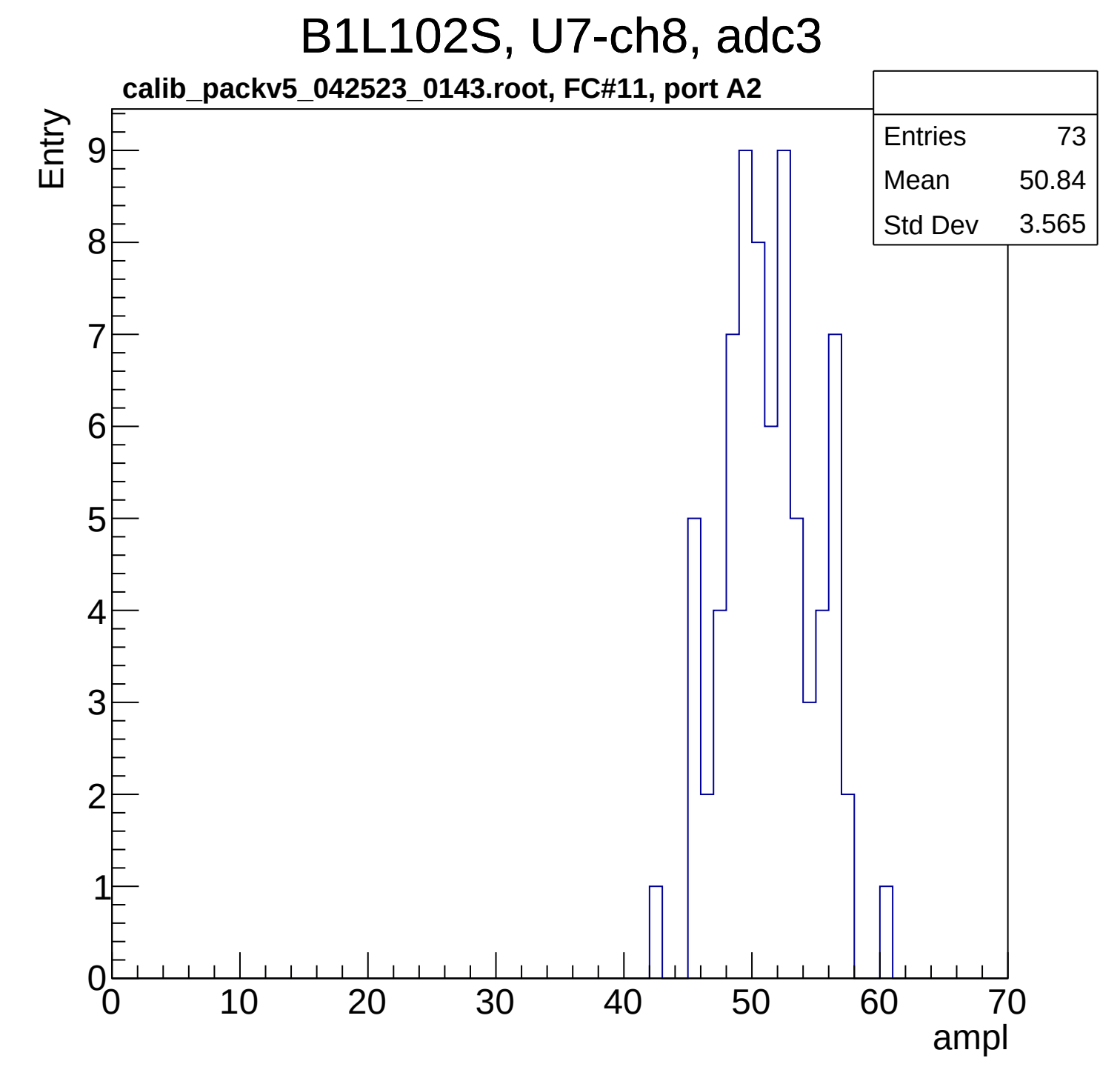
B1L102S, U7-ch8, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 73
Mean 50.84
Std Dev 3.565
Entry
ampl
0
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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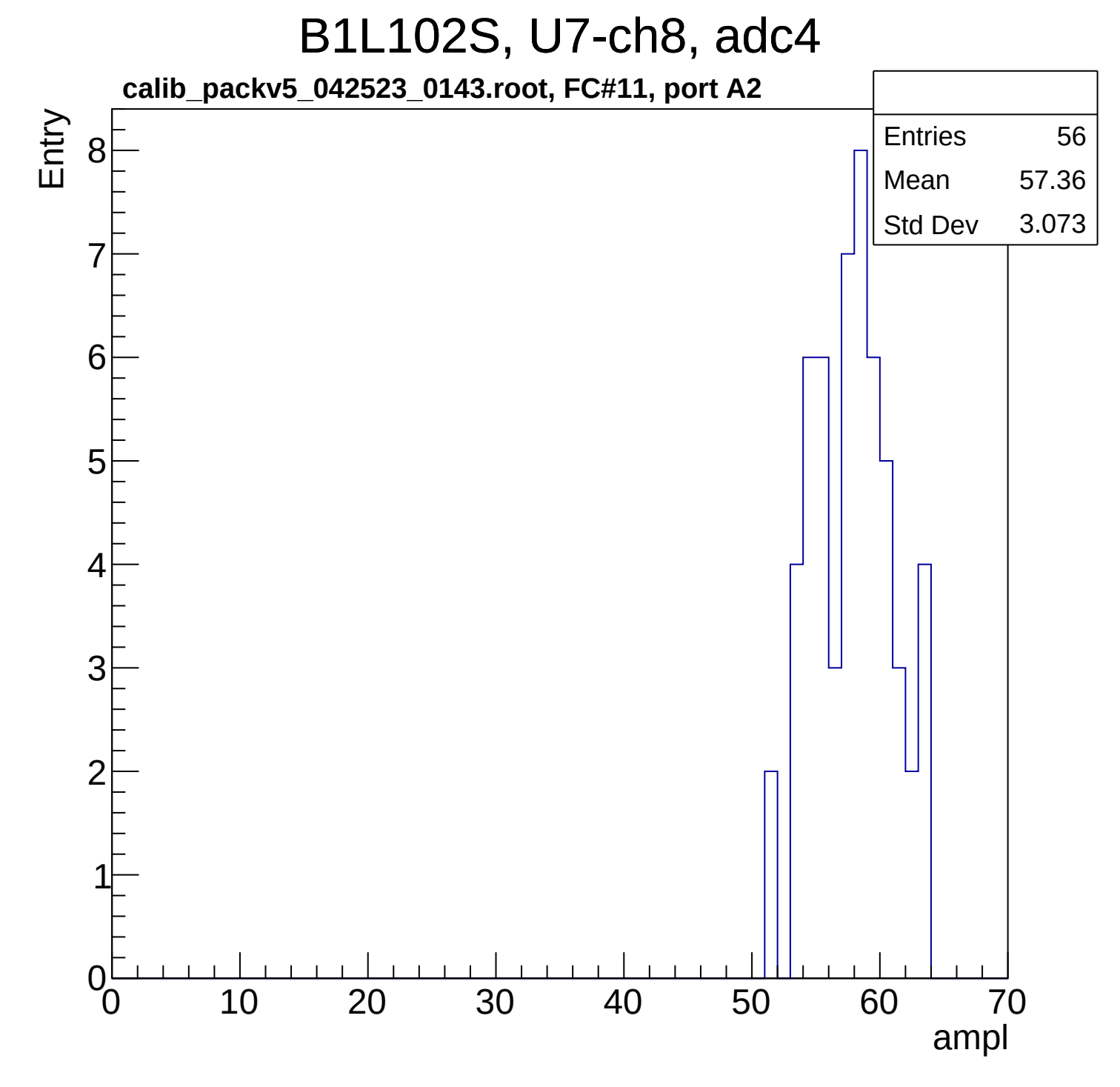
B1L102S, U7-ch8, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 56
Mean 57.36
Std Dev 3.073
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
30
40
50
60
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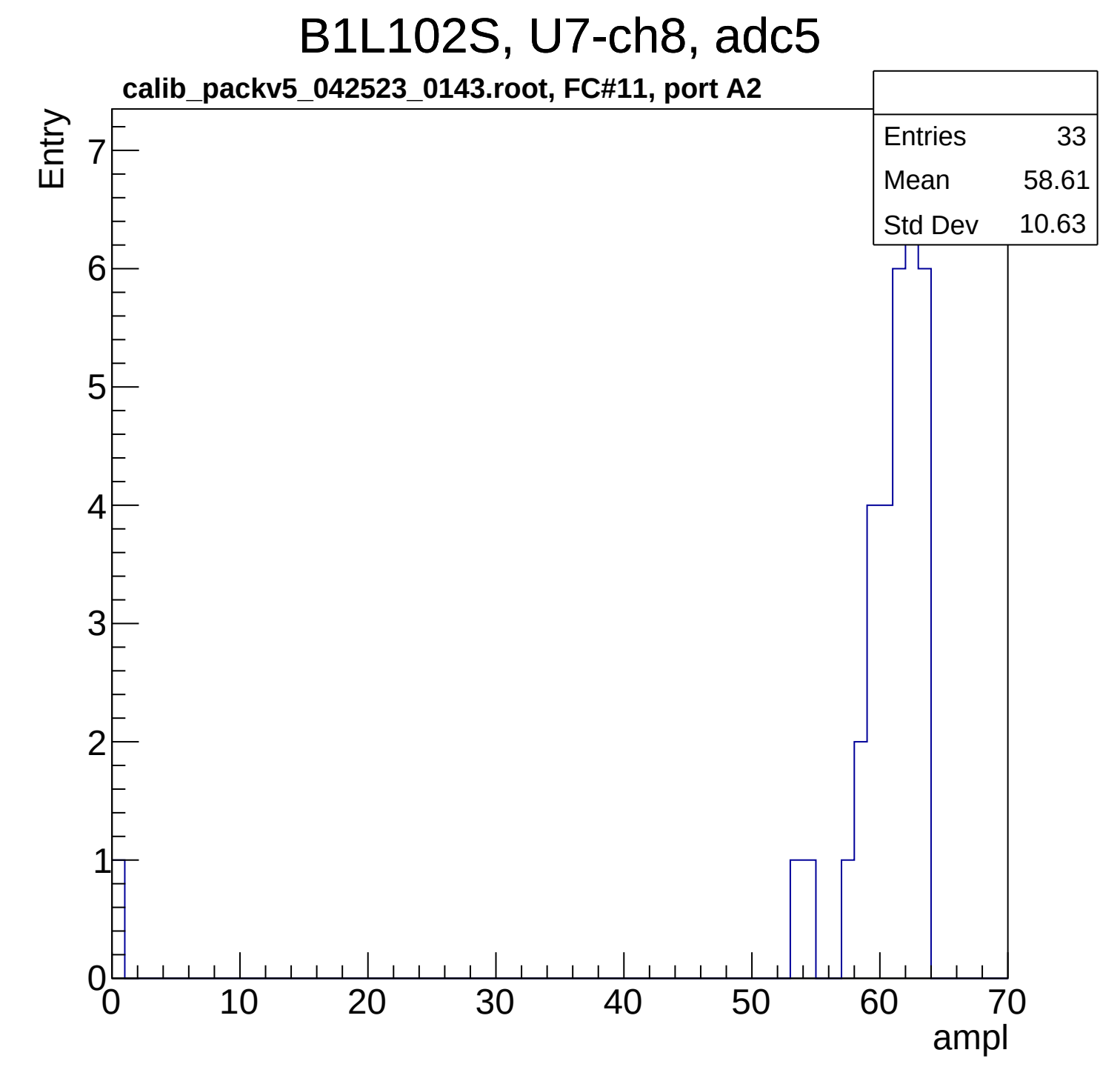
B1L102S, U7-ch8, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 33
Mean 58.61
Std Dev 10.63
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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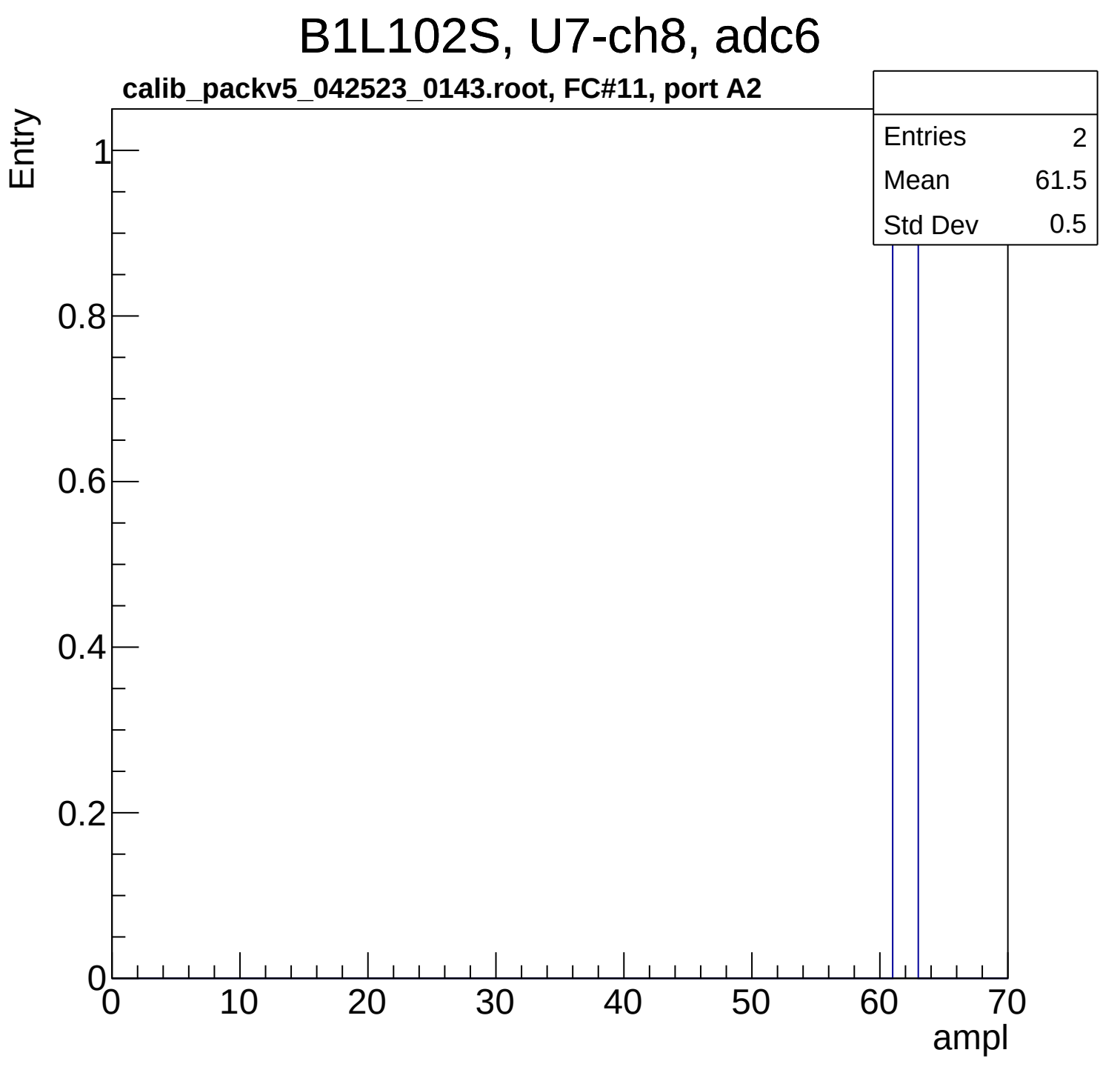
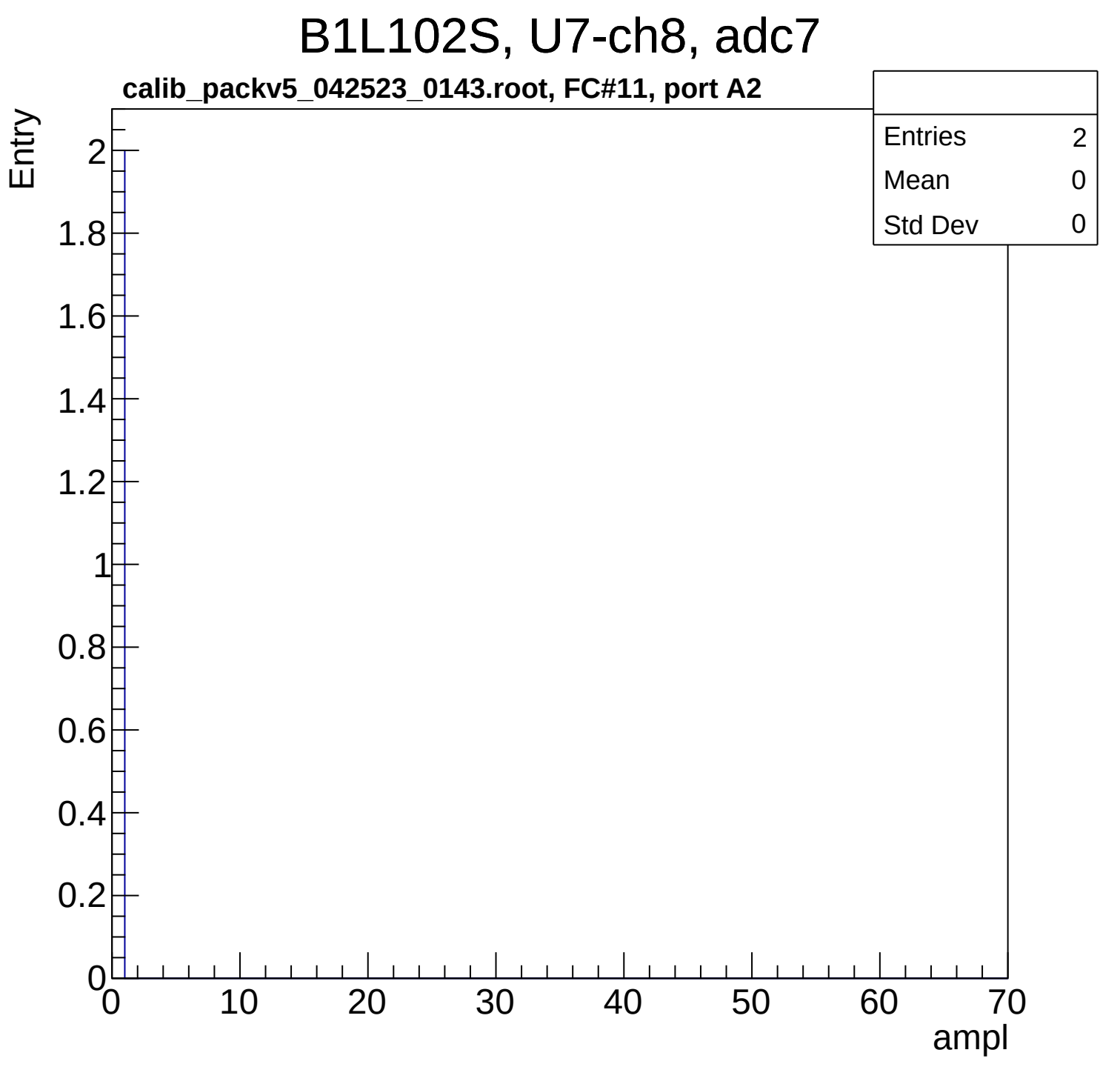

B1L102S, U7-ch8, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 2
Mean 61.5
Std Dev 0.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U7-ch8, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 2
Mean 0
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
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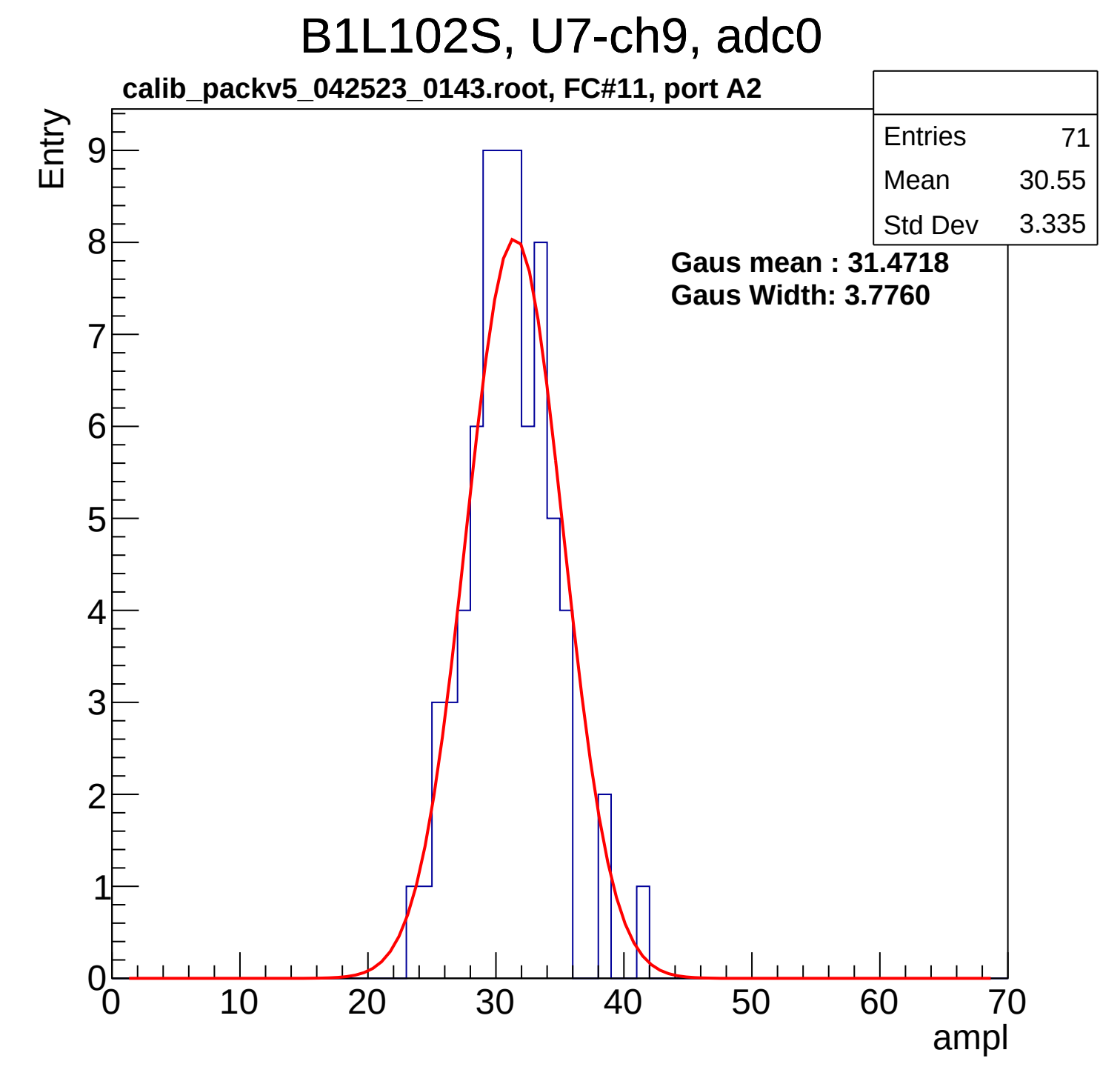
B1L102S, U7-ch9, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 71
Mean 30.55
Std Dev 3.335
Gaus mean : 31.4718
Gaus Width: 3.7760
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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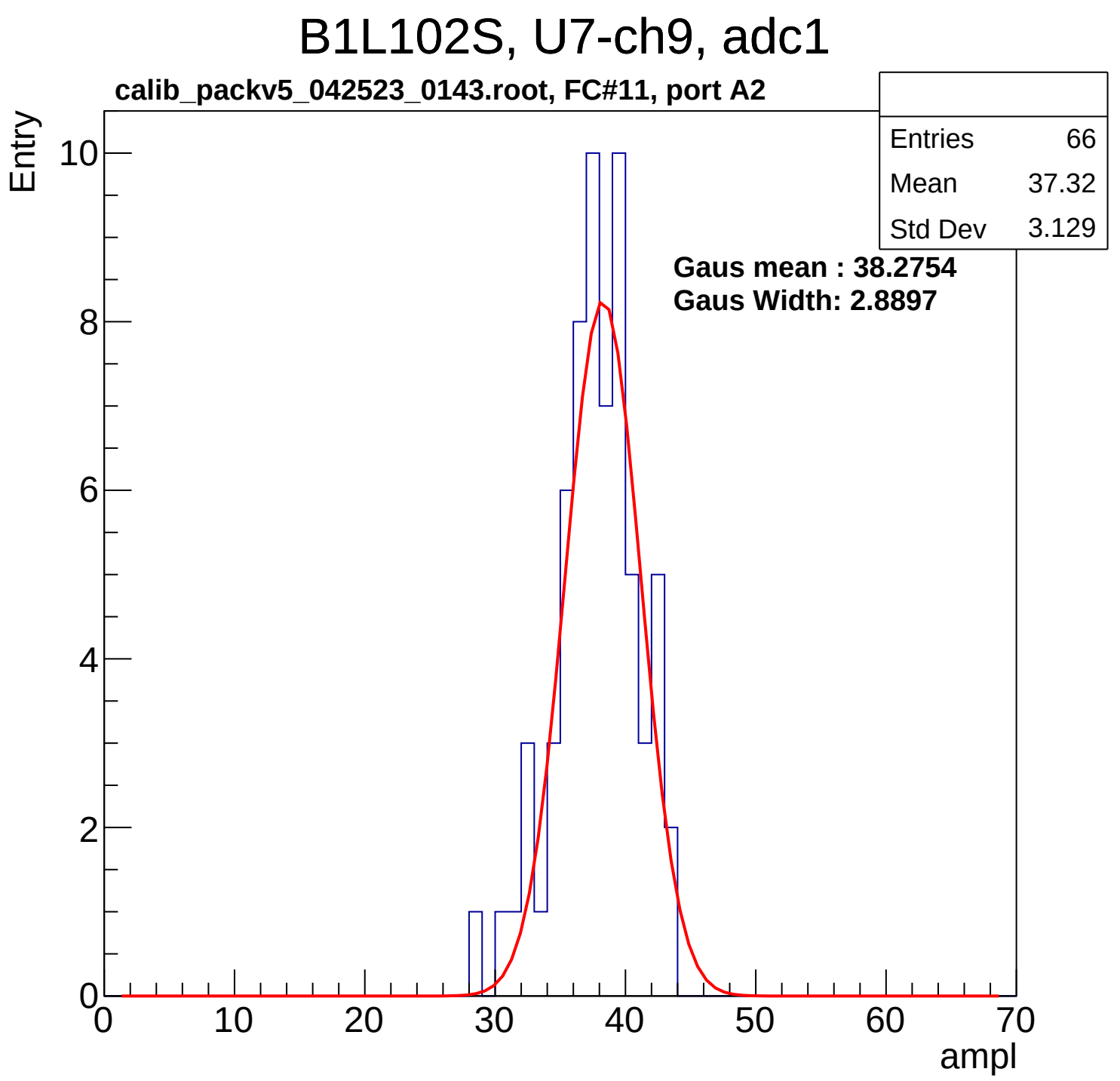
B1L102S, U7-ch9, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 66
Mean 37.32
Std Dev 3.129
Gaus mean : 38.2754
Gaus Width: 2.8897
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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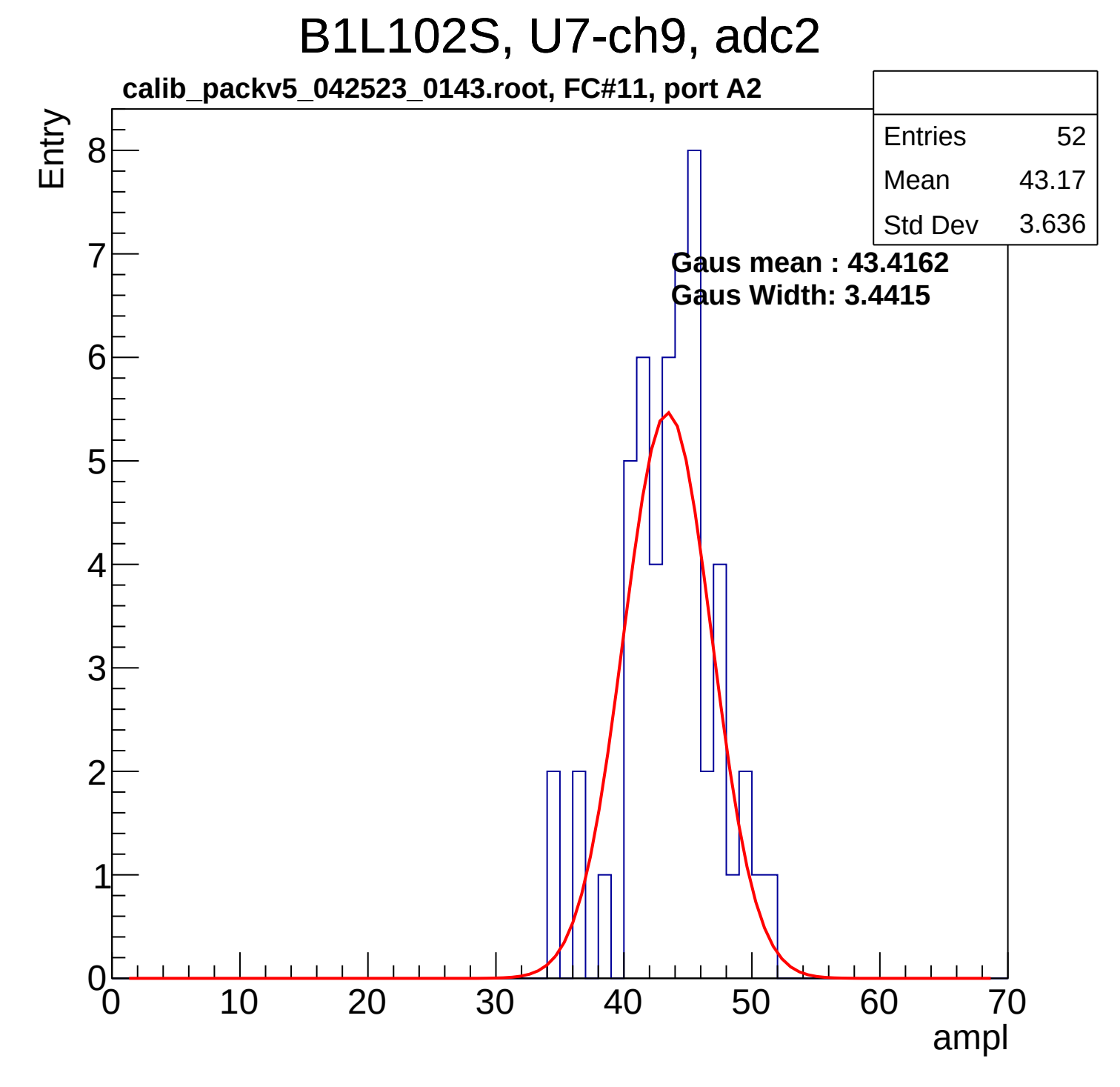
B1L102S, U7-ch9, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 52
Mean 43.17
Std Dev 3.636
Gaus mean : 43.4162
Gaus Width: 3.4415
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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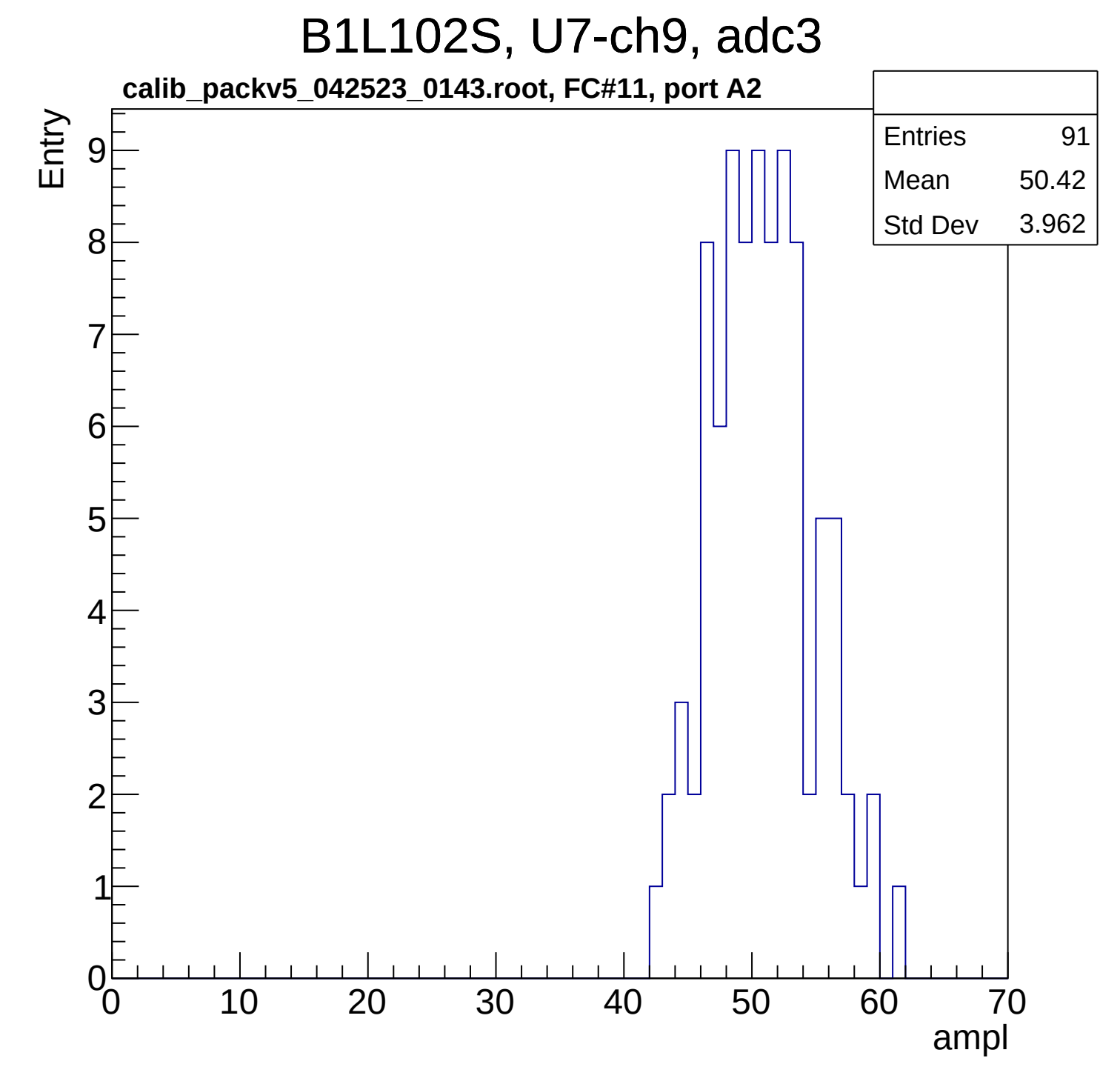
B1L102S, U7-ch9, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 91
Mean 50.42
Std Dev 3.962
Entry
ampl
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10
20
30
40
50
60
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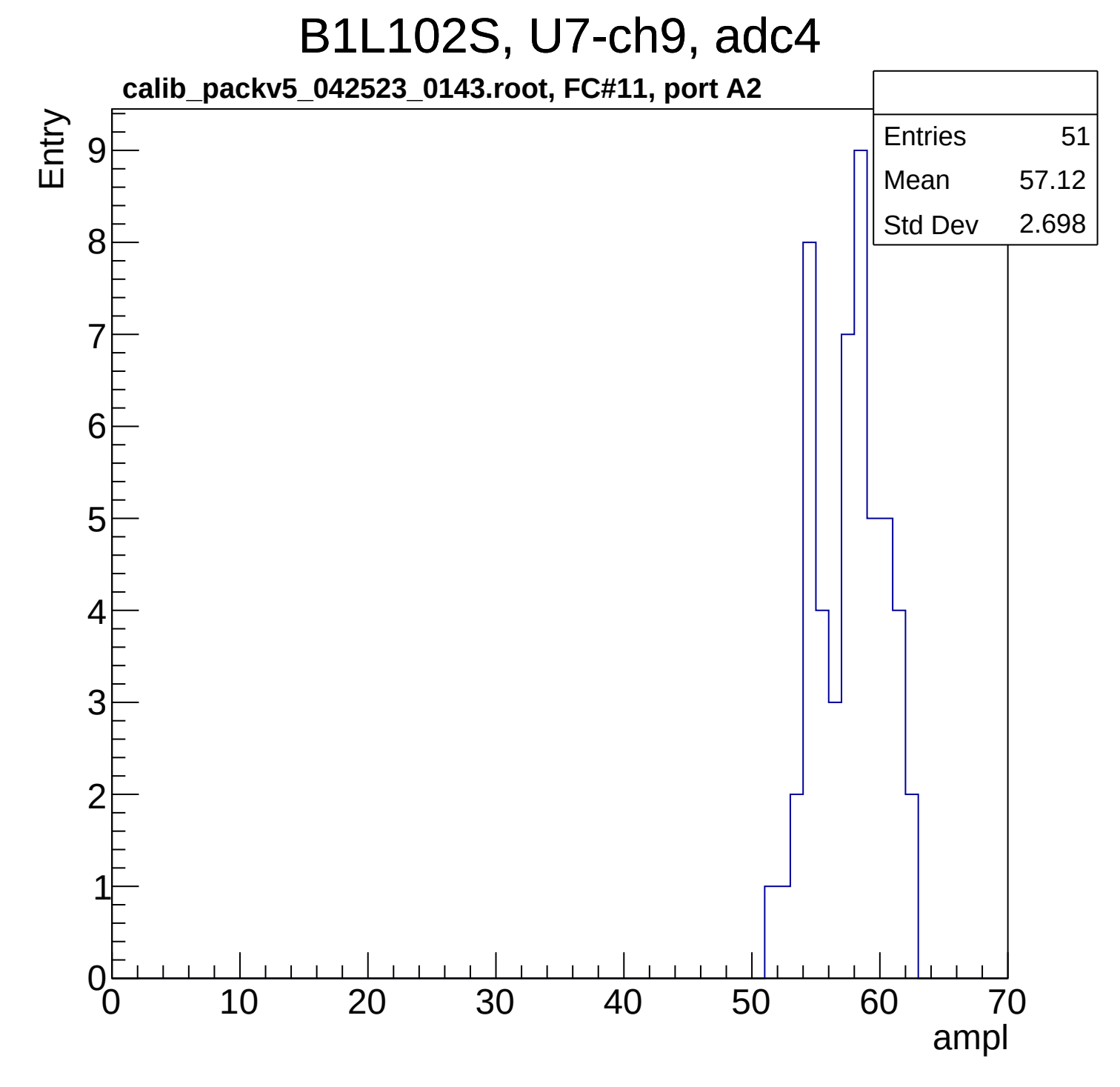
1
2
3
4
5
6
7
8
9


B1L102S, U7-ch9, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 51
Mean 57.12
Std Dev 2.698
Entry
ampl
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2
3
4
5
6
7
8
9
0
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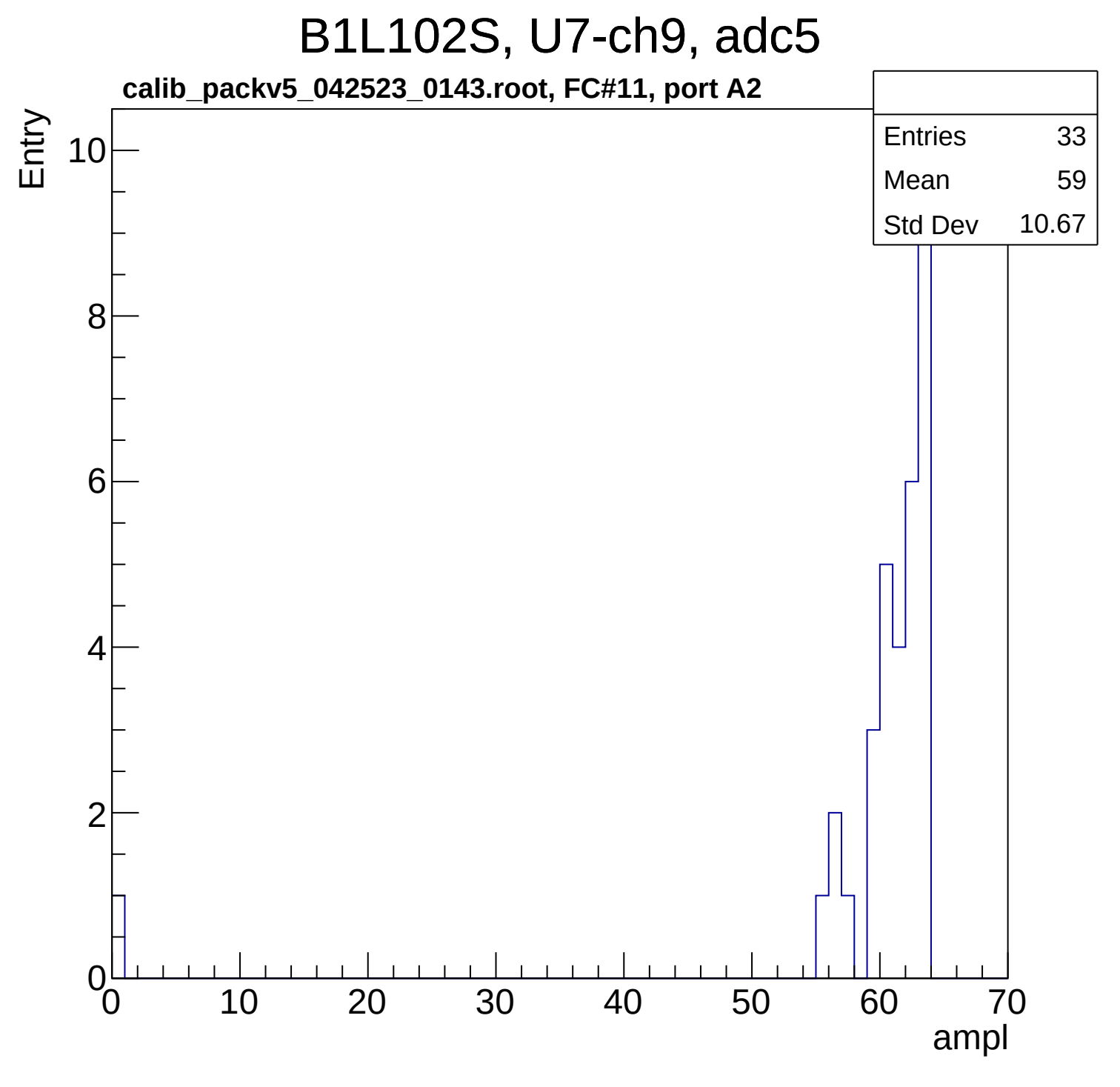
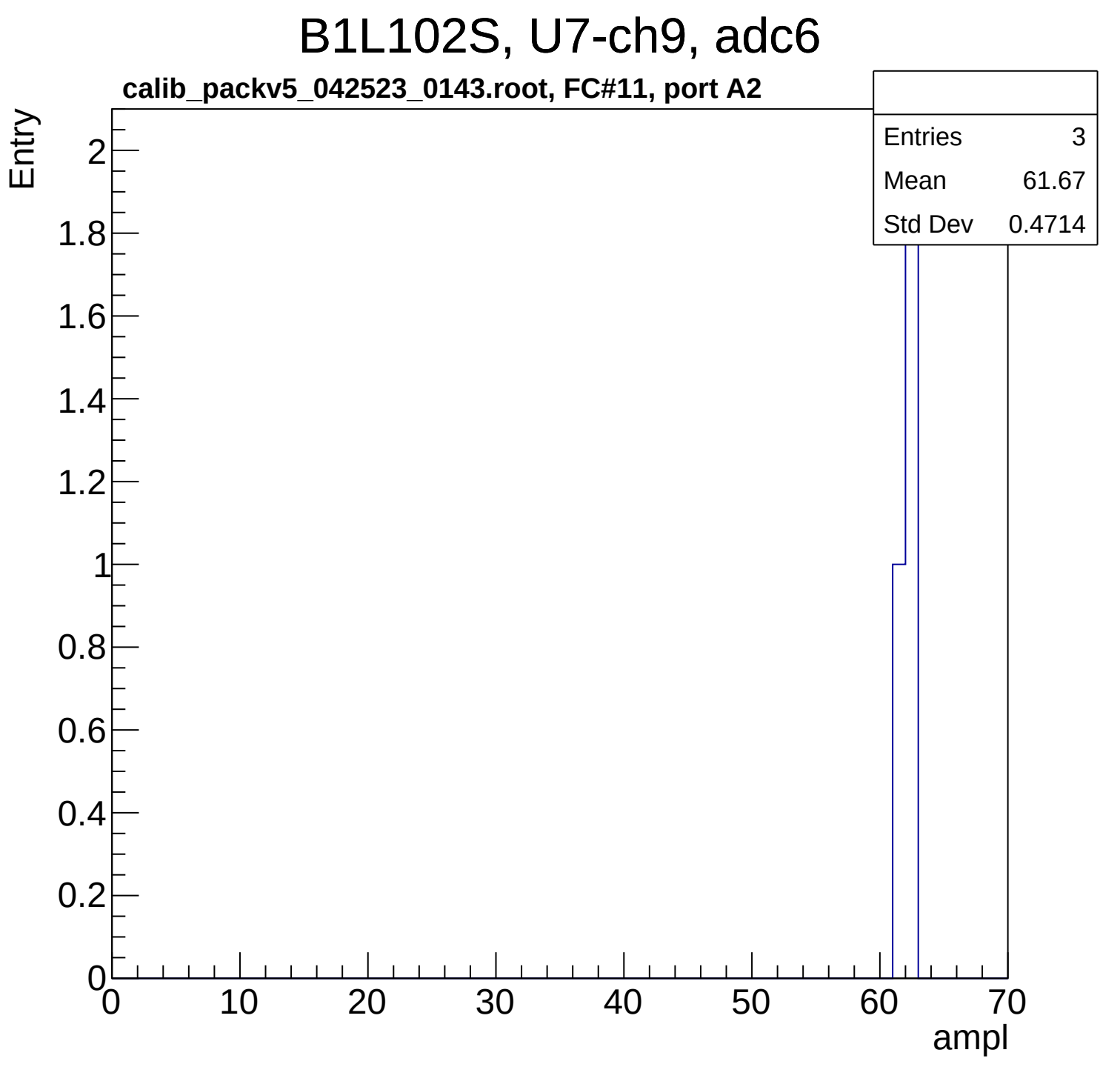
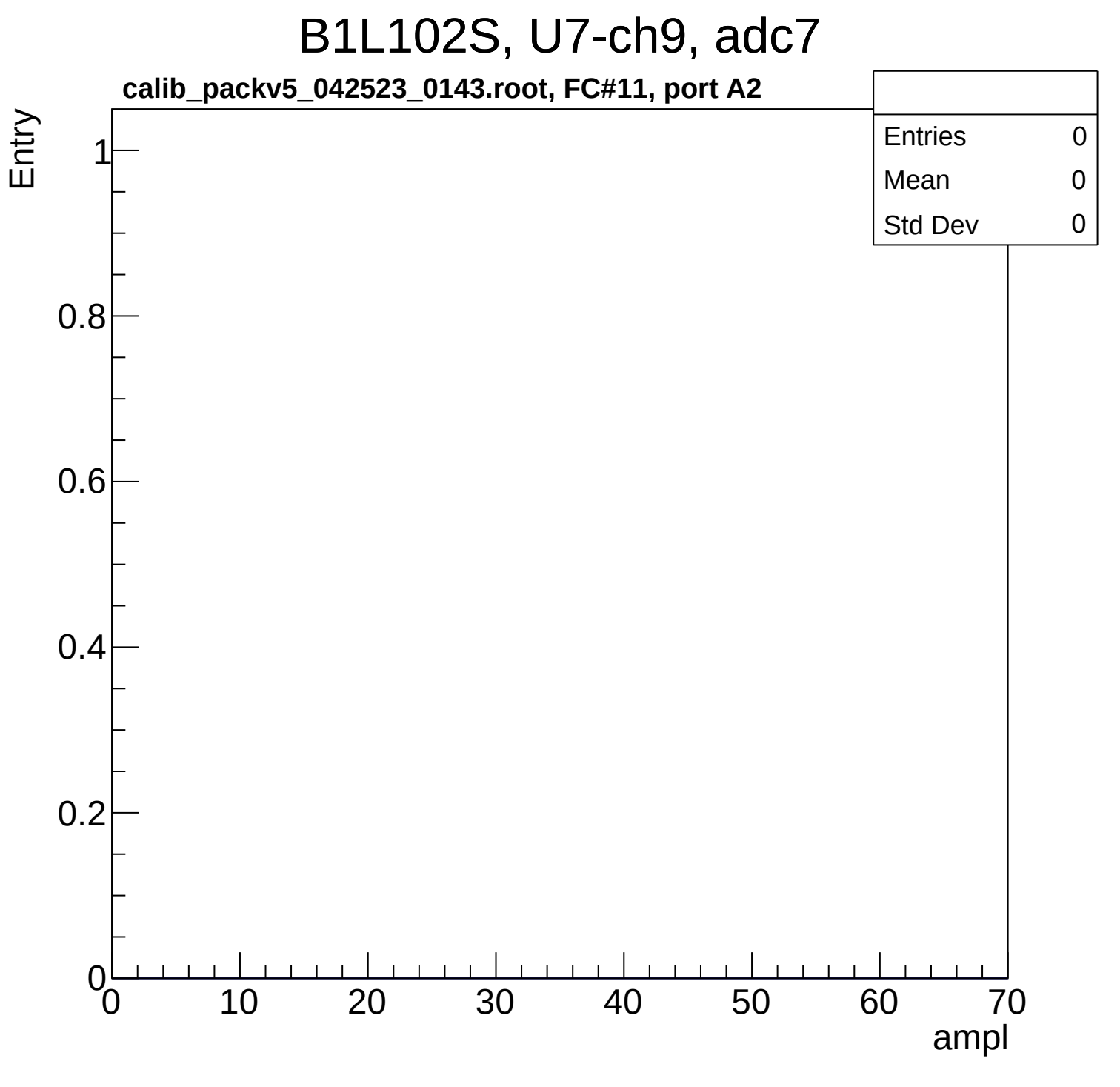

B1L102S, U7-ch9, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 33
Mean 59
Std Dev 10.67
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L102S, U7-ch9, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 3
Mean 61.67
Std Dev 0.4714
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L102S, U7-ch9, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 0
Mean 0
Std Dev 0
Entry
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0.8
0.6
0.4
0.2
0
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10
20
30
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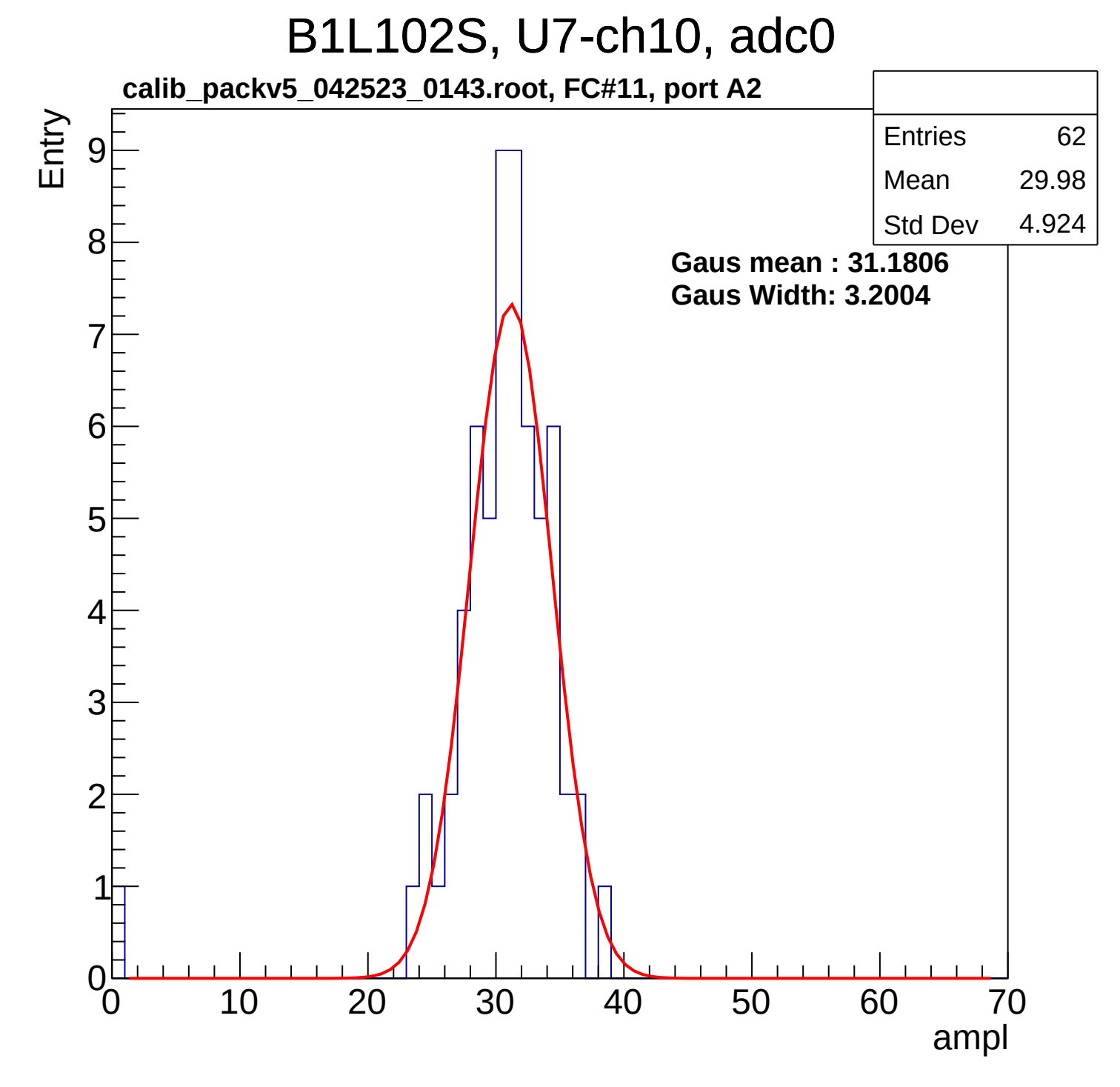
50
60
70
ampl


B1L102S, U7-ch10, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 62
Mean 29.98
Std Dev 4.924
Gaus mean : 31.1806
Gaus Width: 3.2004
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
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40
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60
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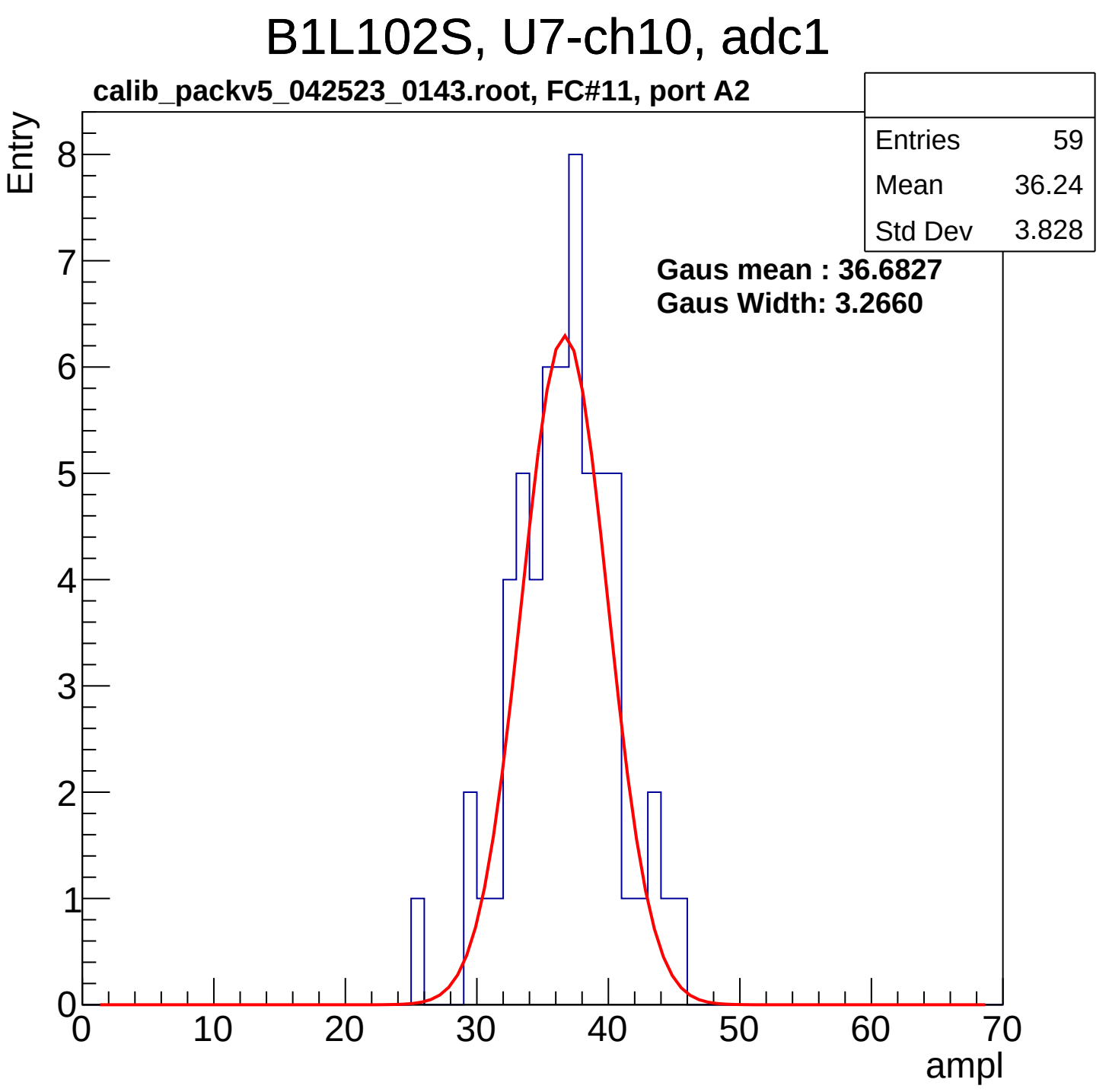
B1L102S, U7-ch10, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 59
Mean 36.24
Std Dev 3.828
Gaus mean : 36.6827
Gaus Width: 3.2660
Entry
ampl
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1
2
3
4
5
6
7
8
0
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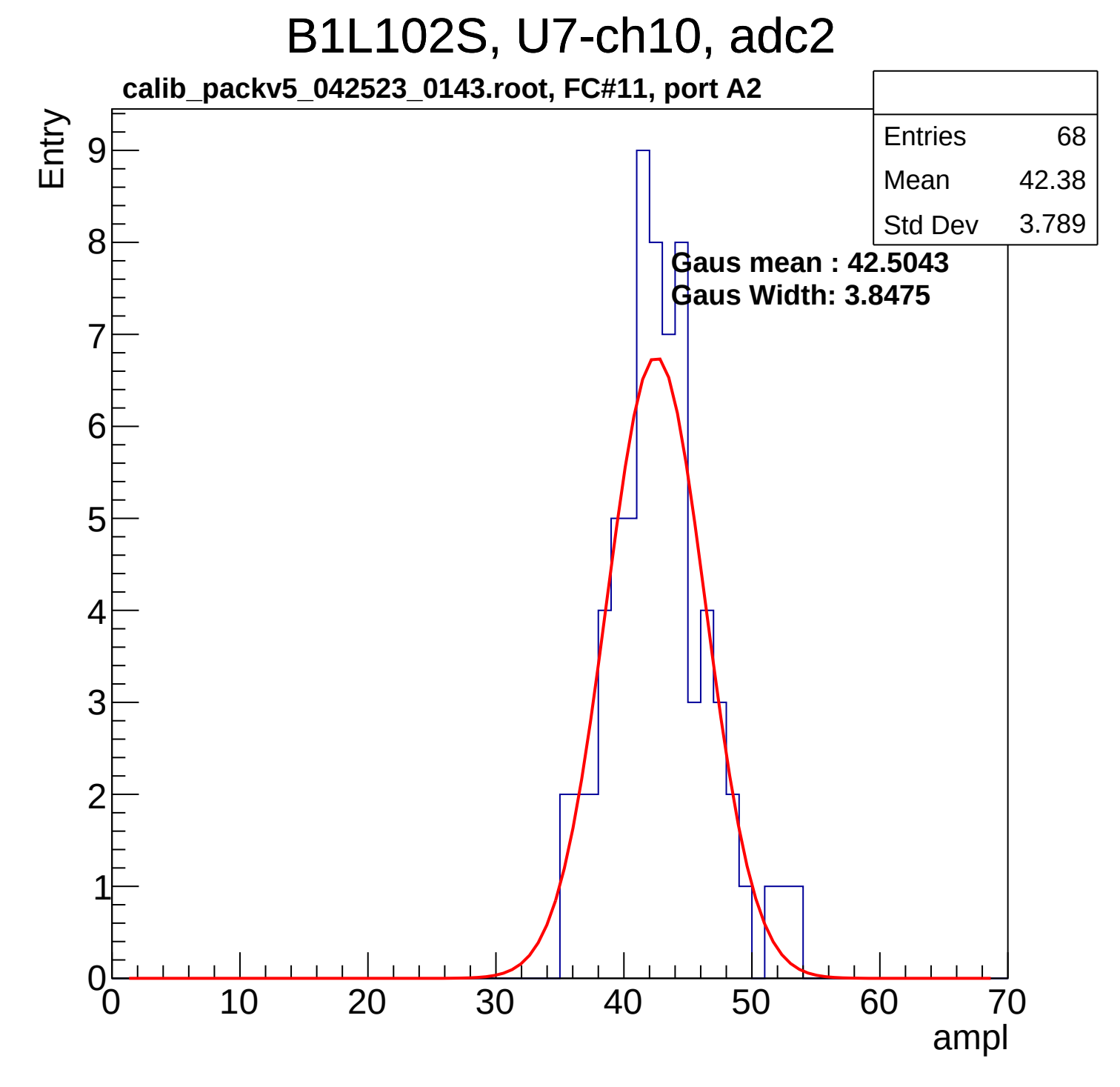
20
30
40
50
60
70


B1L102S, U7-ch10, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 68
Mean 42.38
Std Dev 3.789
Gaus mean : 42.5043
Gaus Width: 3.8475
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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60
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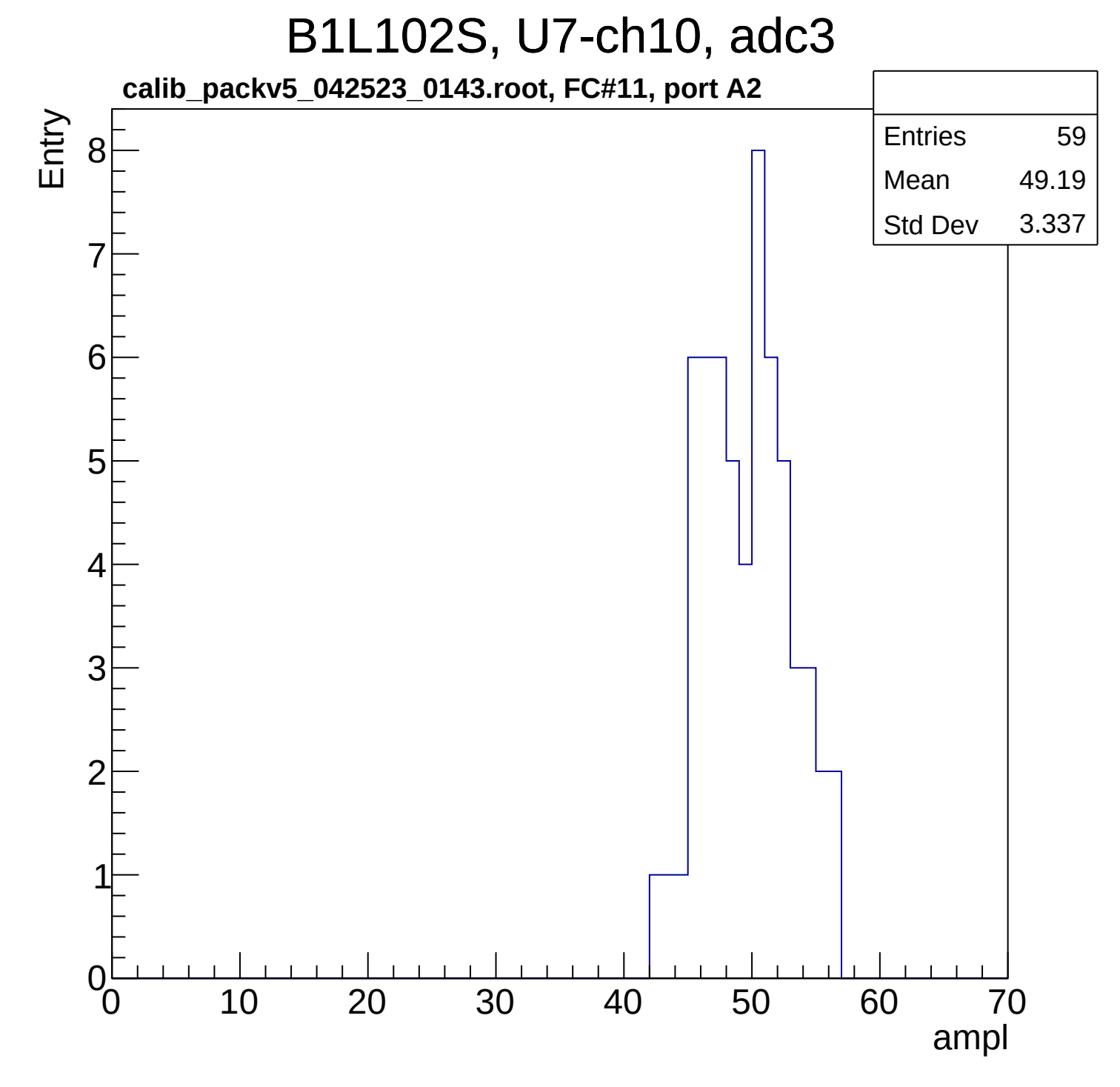
B1L102S, U7-ch10, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 59
Mean 49.19
Std Dev 3.337
Entry
ampl
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4
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7
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0
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40
50
60
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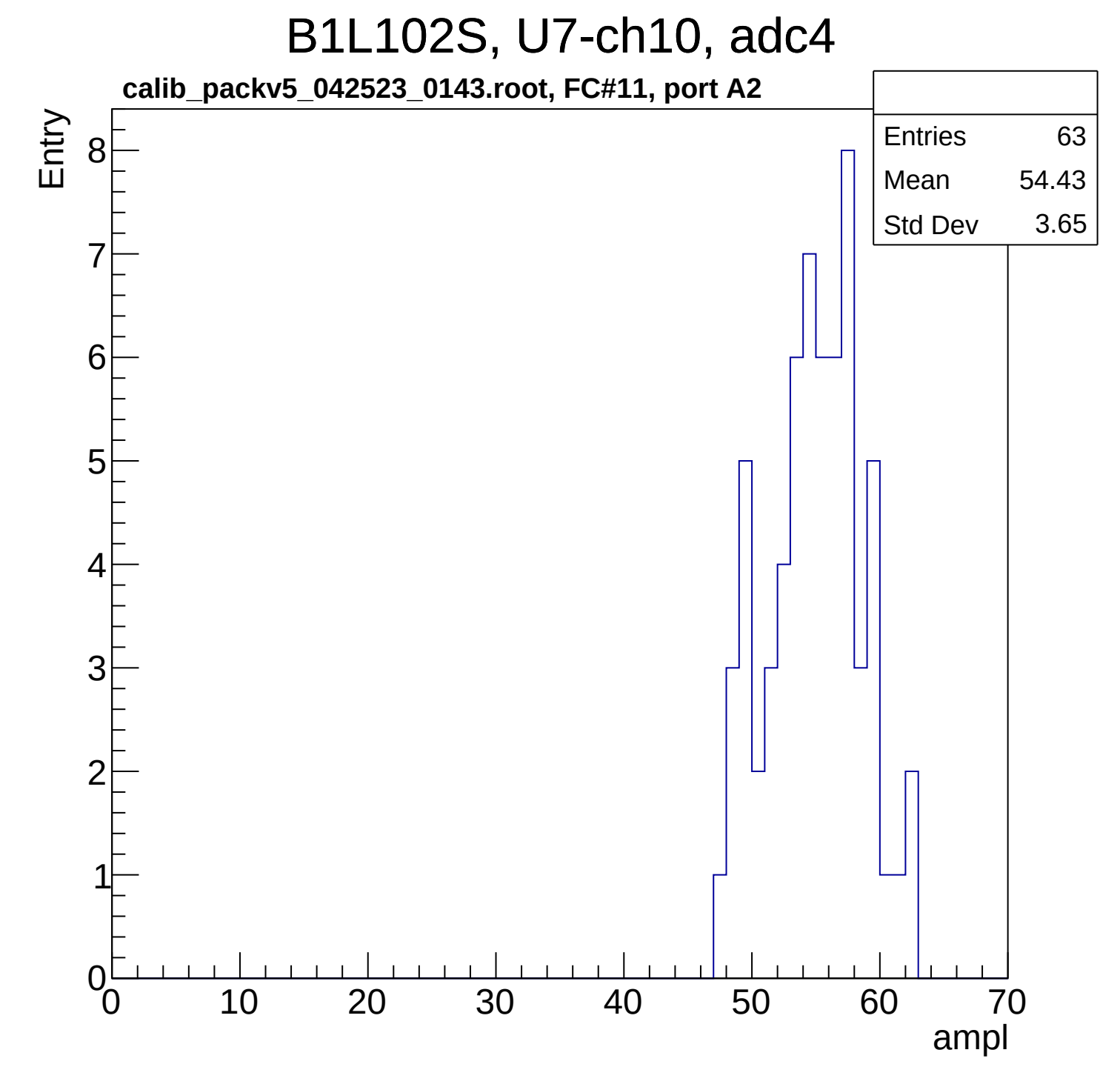
B1L102S, U7-ch10, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 63
Mean 54.43
Std Dev 3.65
Entry
ampl
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5
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60
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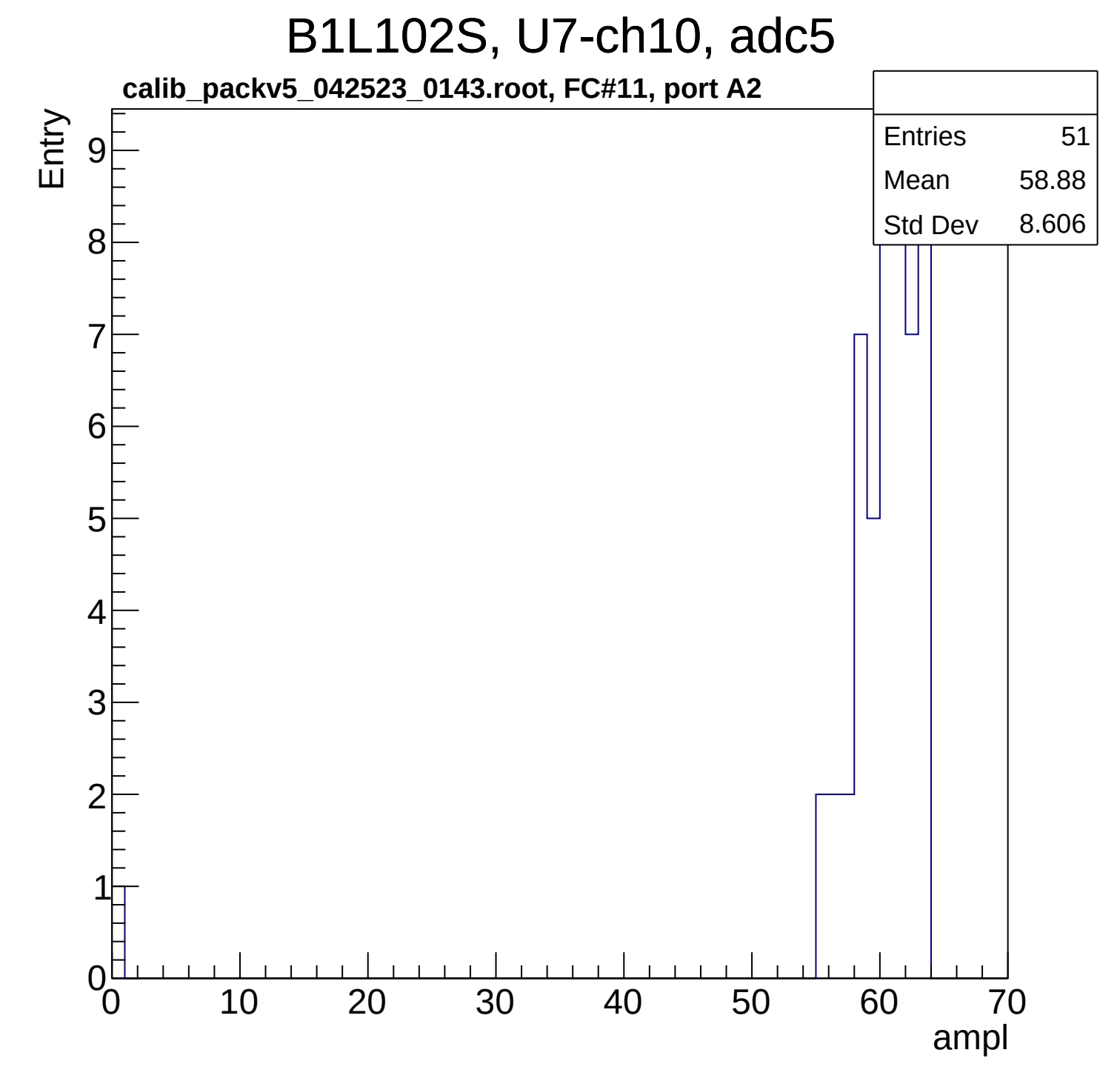
B1L102S, U7-ch10, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 51
Mean 58.88
Std Dev 8.606
Entry
ampl
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3
4
5
6
7
8
9
0
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20
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40
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60
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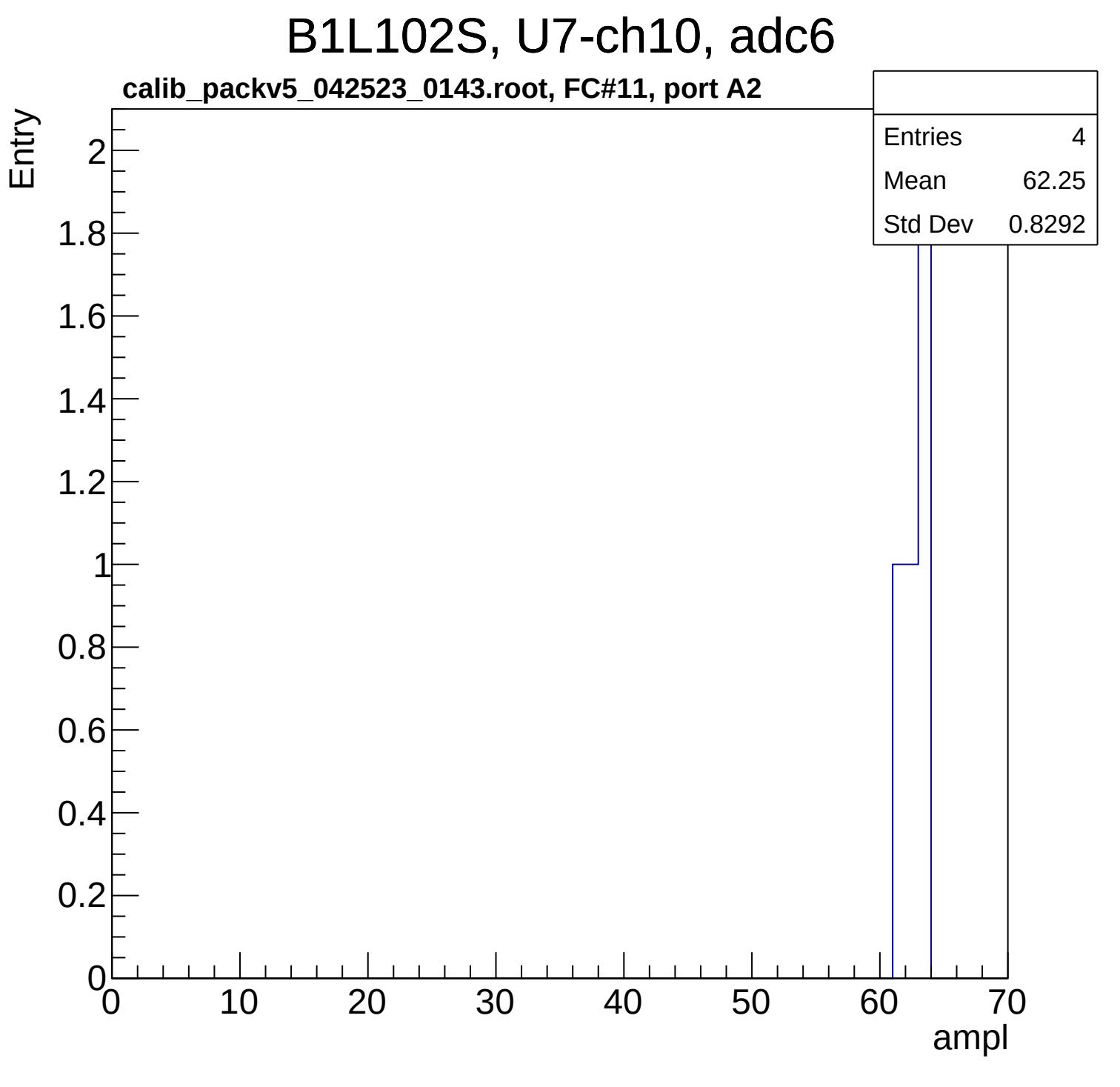
B1L102S, U7-ch10, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 4
Mean 62.25
Std Dev 0.8292
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
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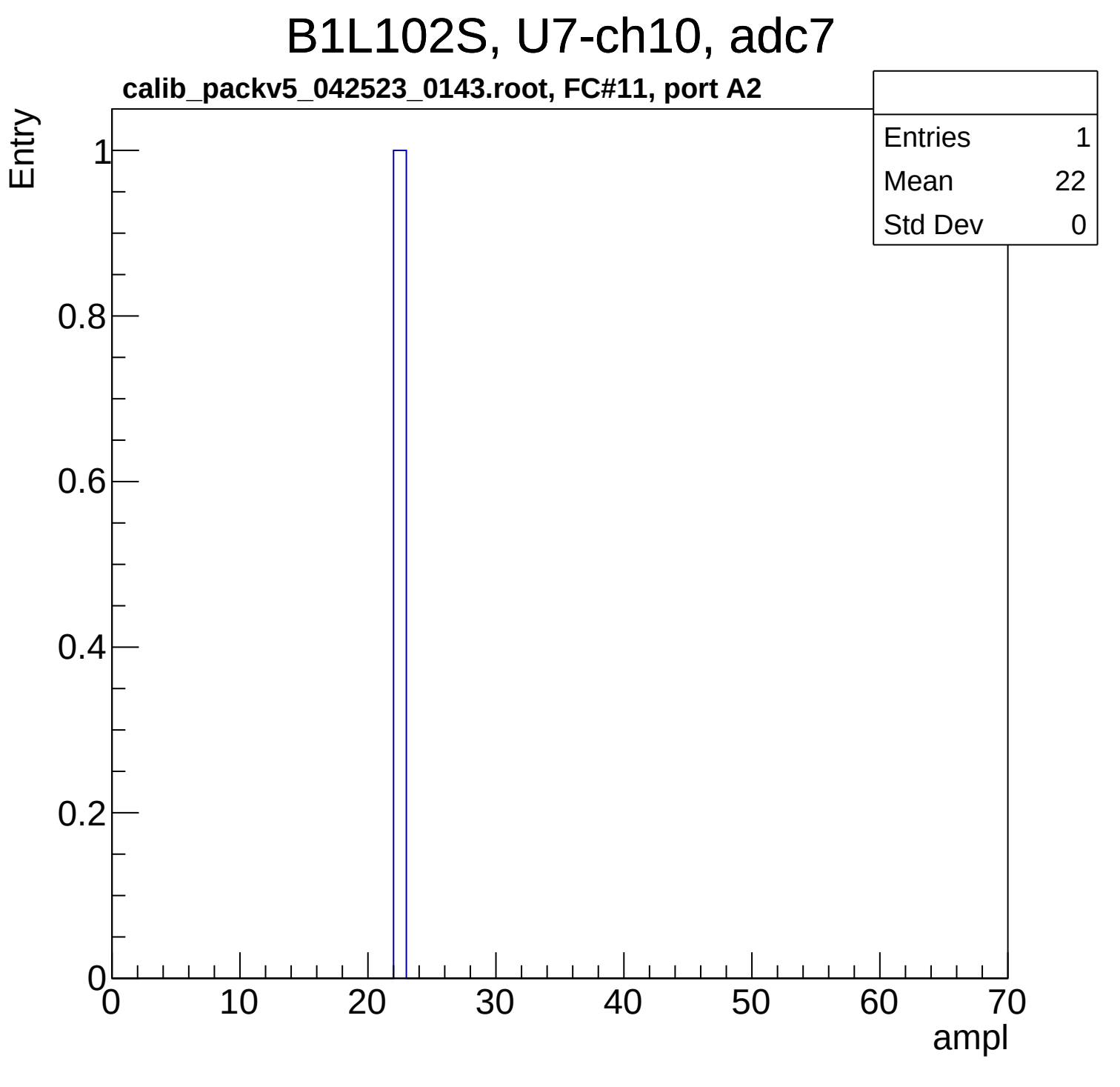
B1L102S, U7-ch10, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 1
Mean 22
Std Dev 0
Entry
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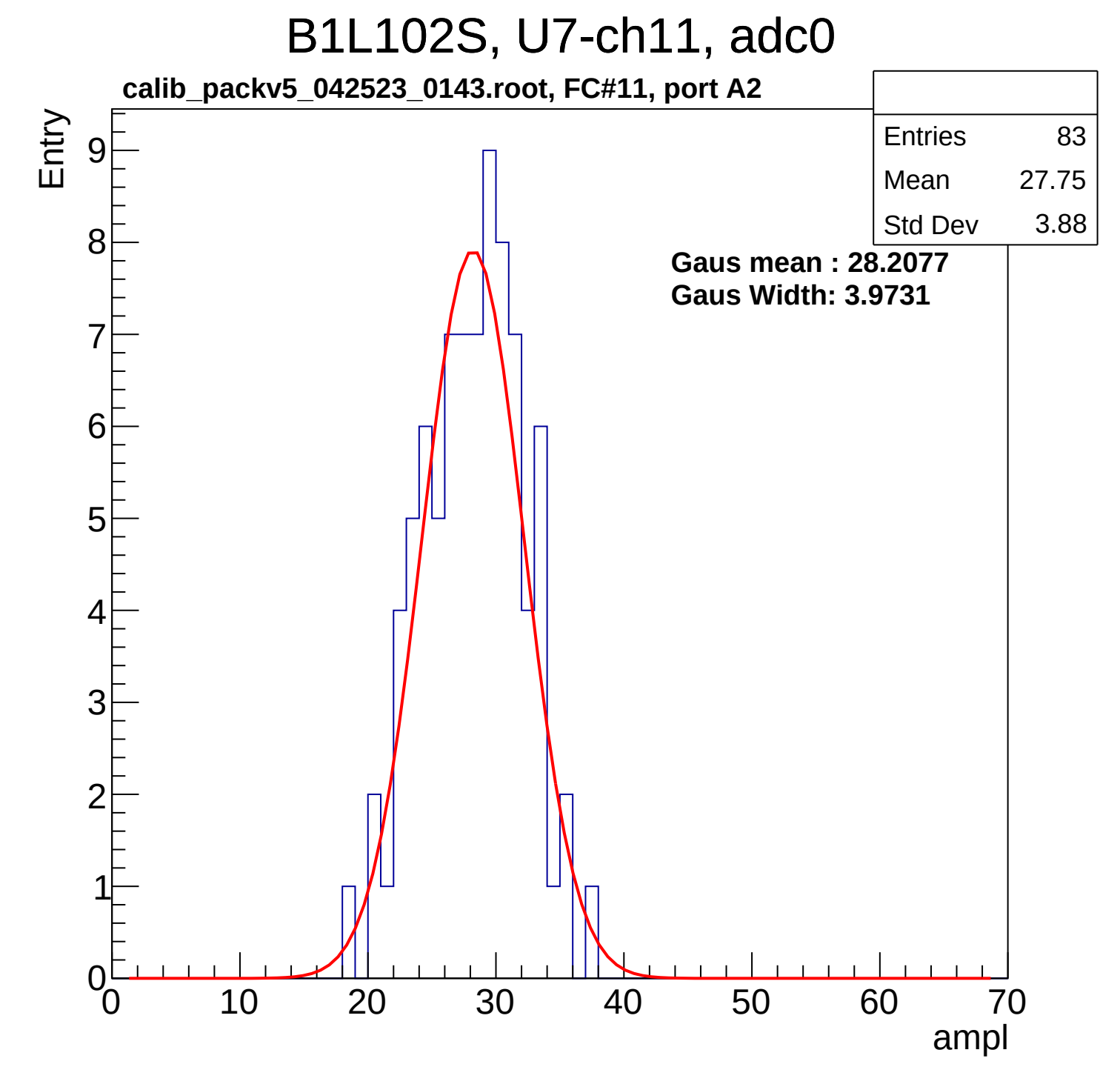
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U7-ch11, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 83
Mean 27.75
Std Dev 3.88
Gaus mean : 28.2077
Gaus Width: 3.9731
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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60
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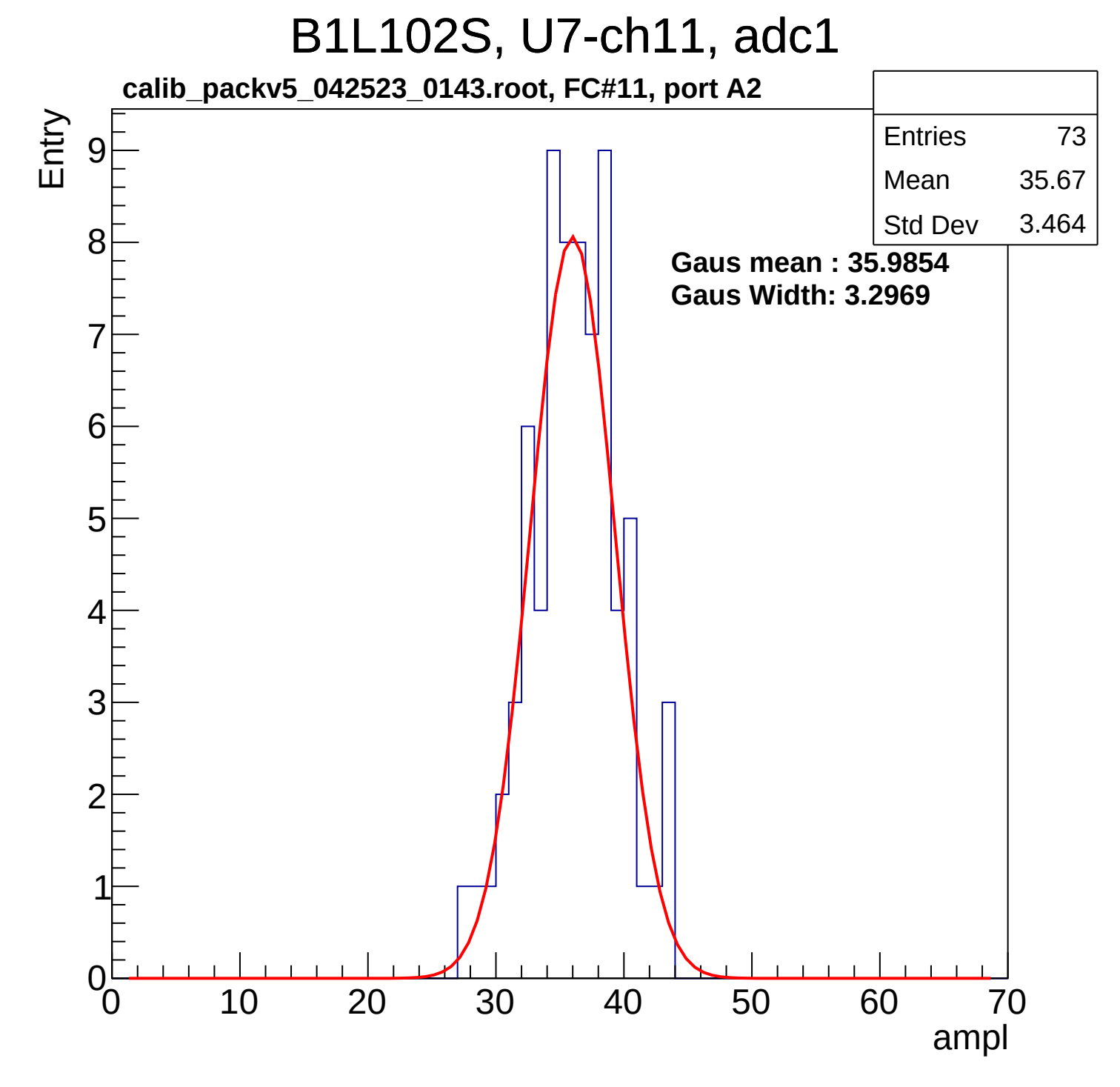
B1L102S, U7-ch11, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 73
Mean 35.67
Std Dev 3.464
Gaus mean : 35.9854
Gaus Width: 3.2969
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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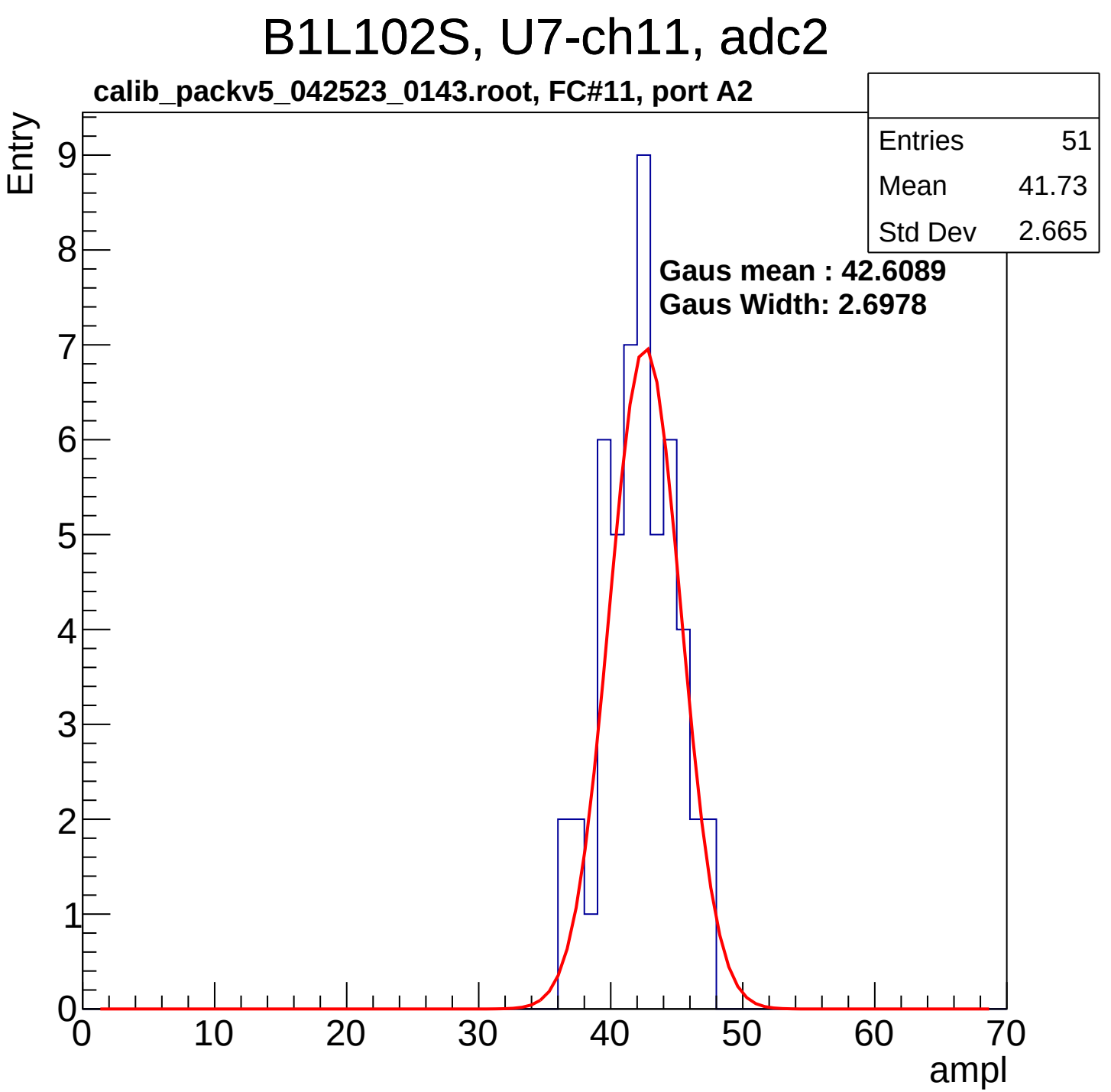
B1L102S, U7-ch11, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 51
Mean 41.73
Std Dev 2.665
Gaus mean : 42.6089
Gaus Width: 2.6978
Entry
ampl
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3
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5
6
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0
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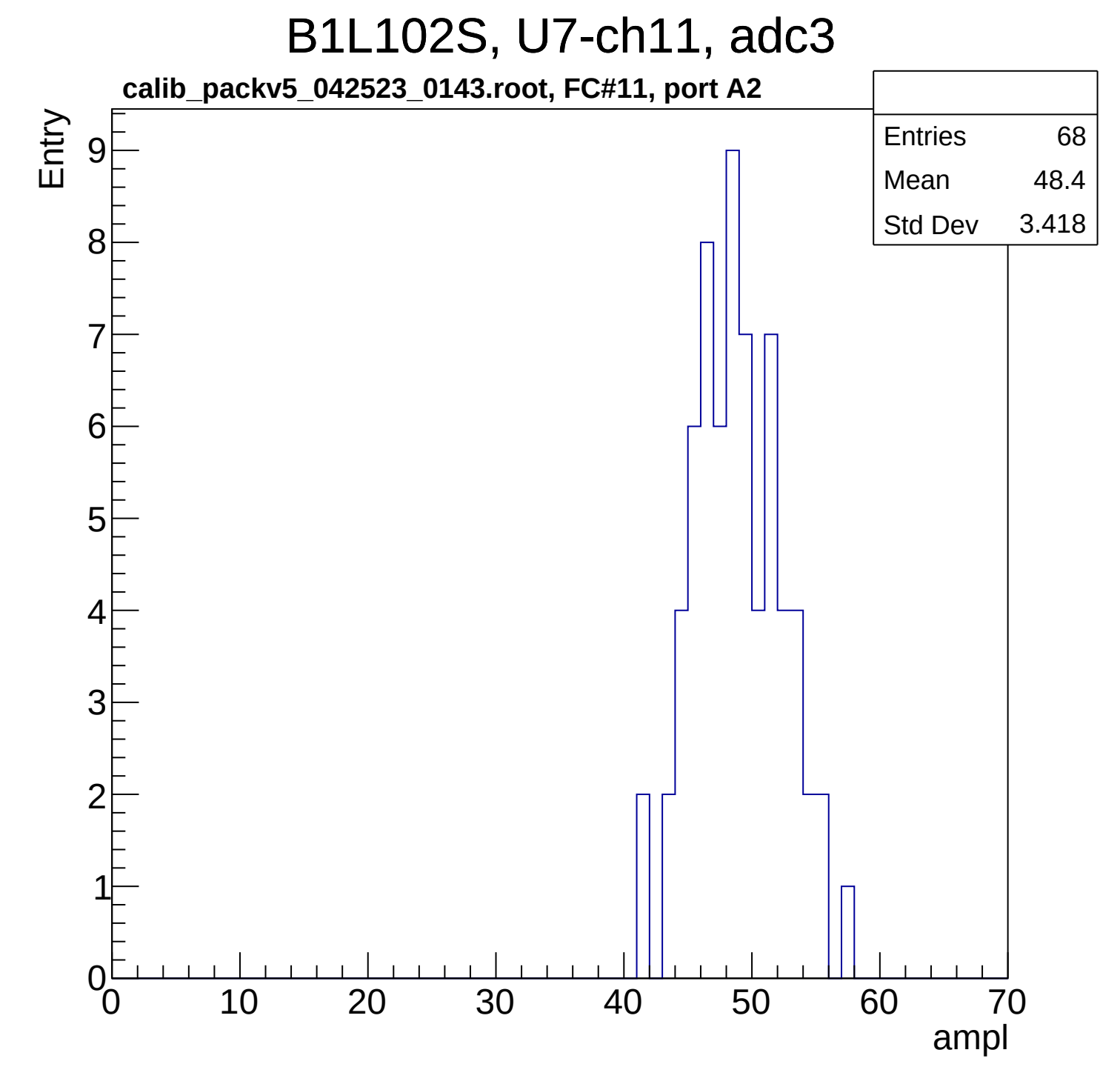
B1L102S, U7-ch11, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 68
Mean 48.4
Std Dev 3.418
Entry
ampl
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1
2
3
4
5
6
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0
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60
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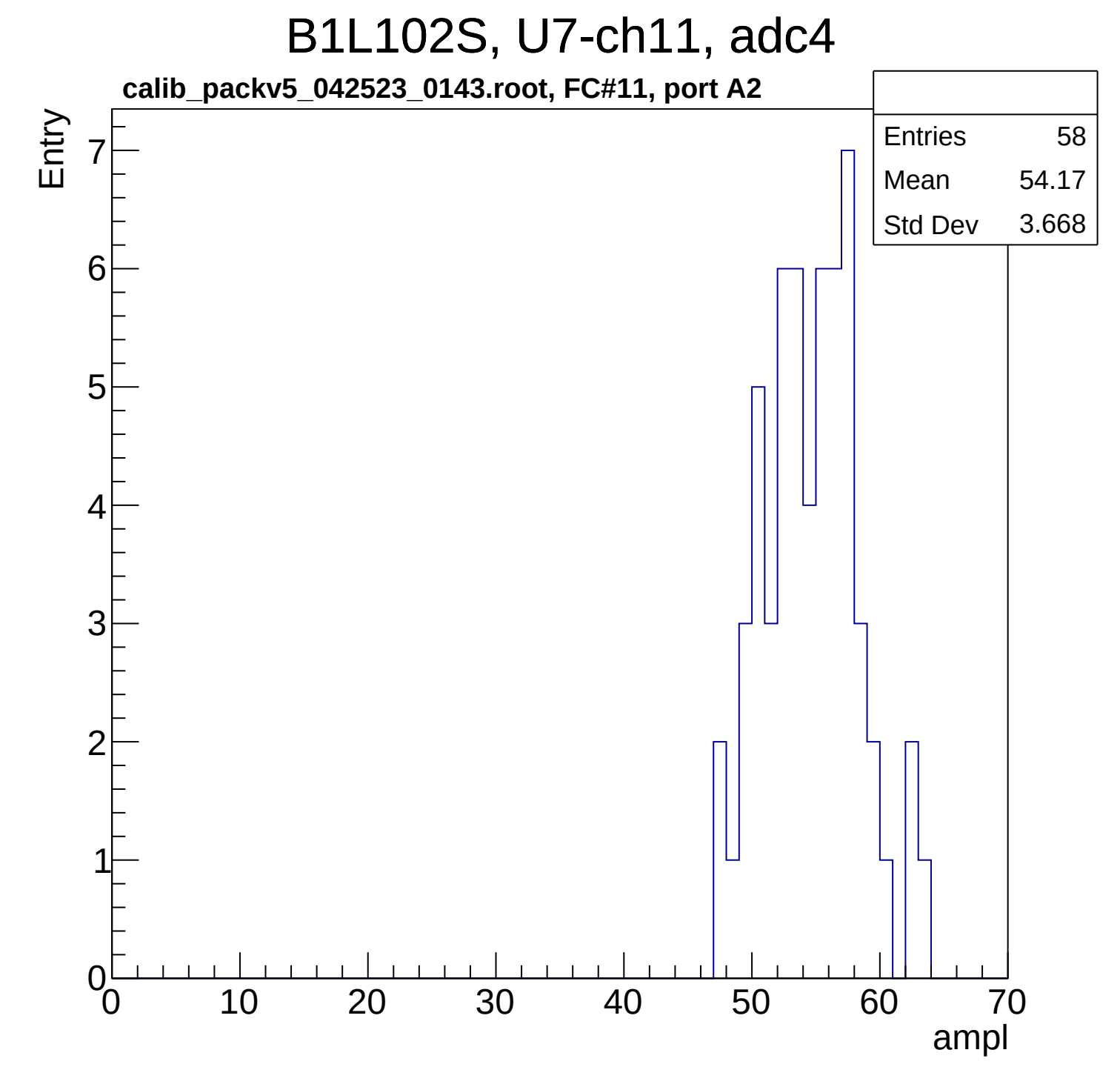
B1L102S, U7-ch11, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 58
Mean 54.17
Std Dev 3.668
Entry
ampl
0
1
2
3
4
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0
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60
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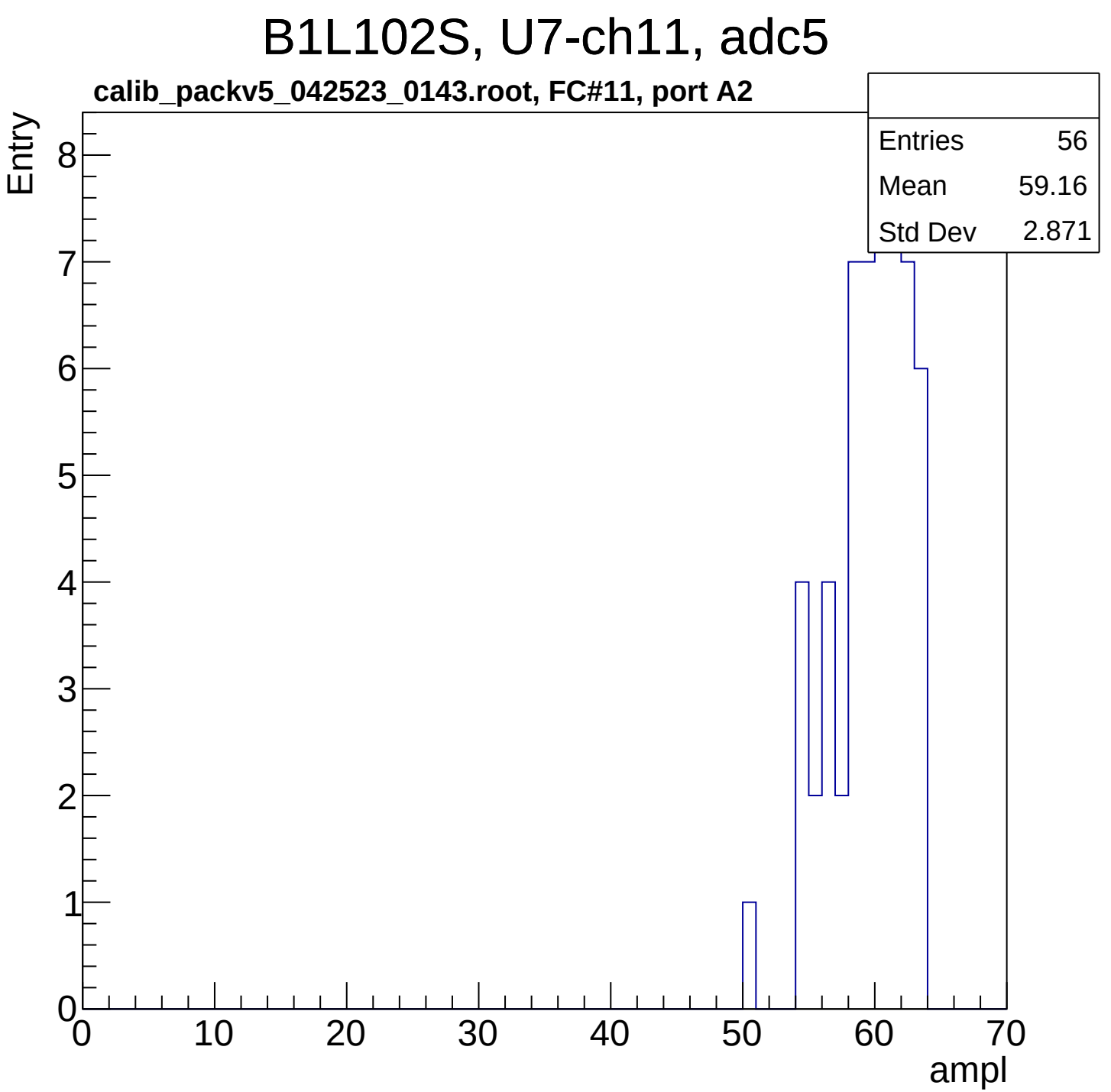
B1L102S, U7-ch11, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 56
Mean 59.16
Std Dev 2.871
Entry
ampl
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1
2
3
4
5
6
7
8
0
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60
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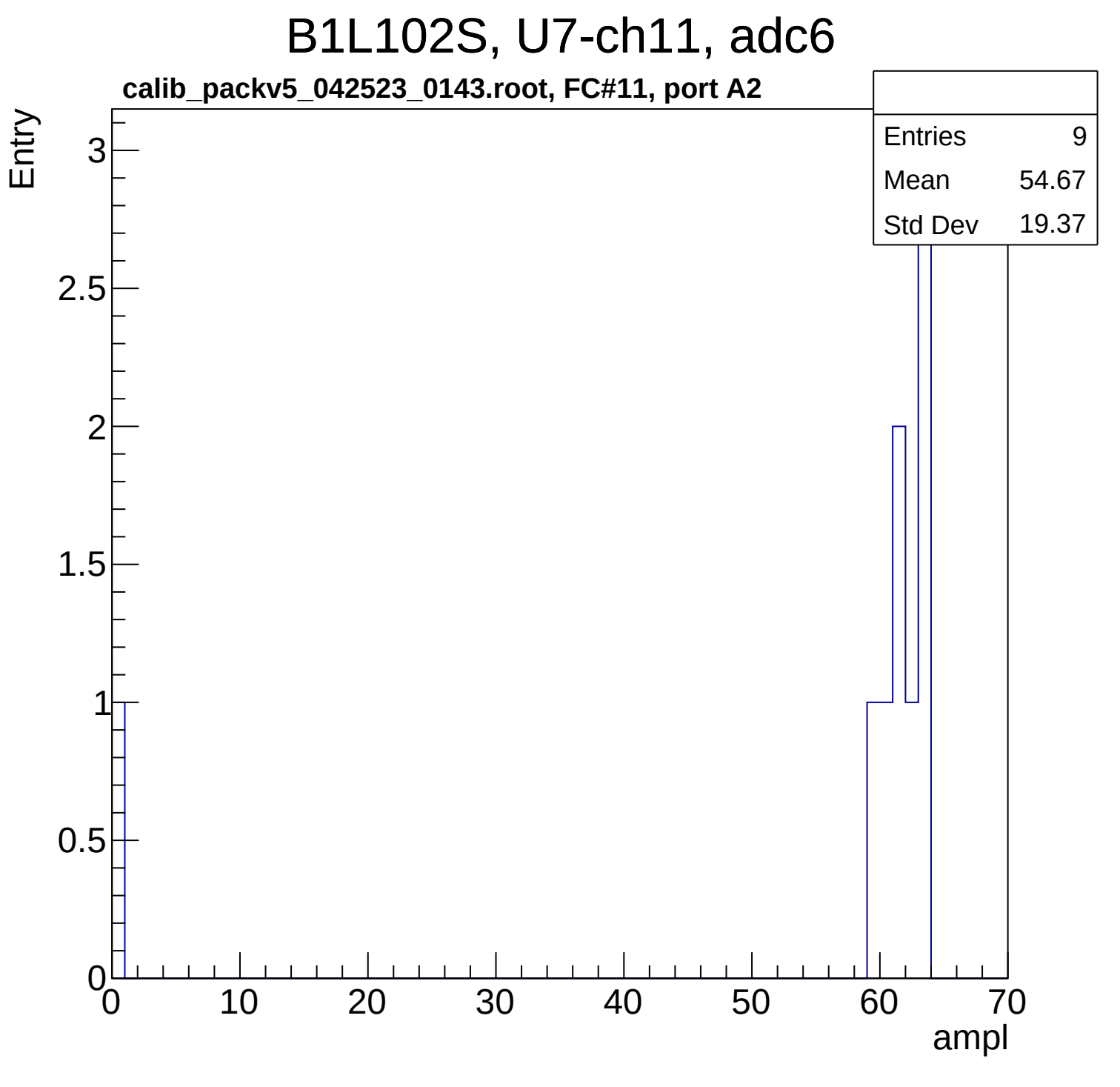
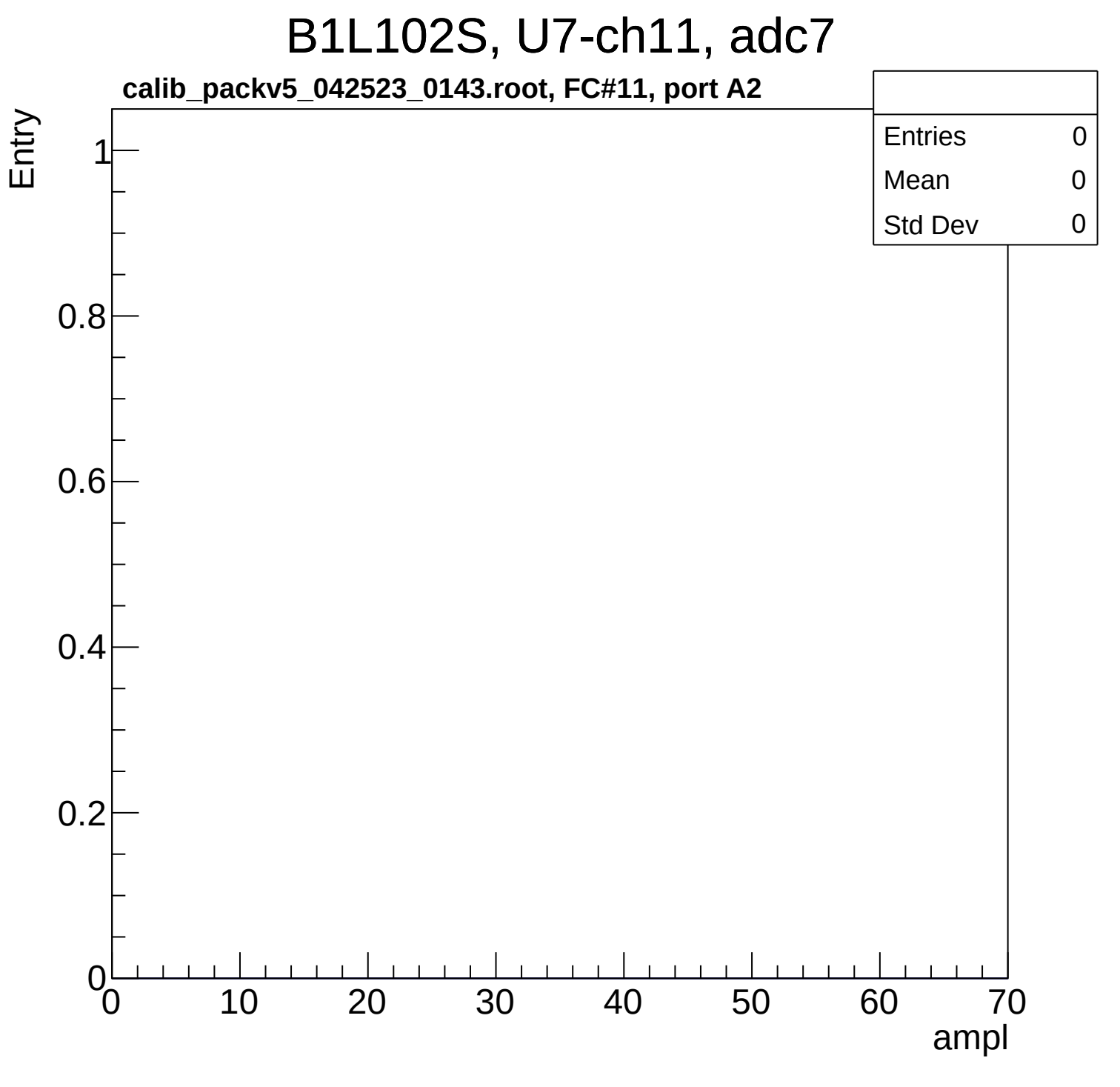
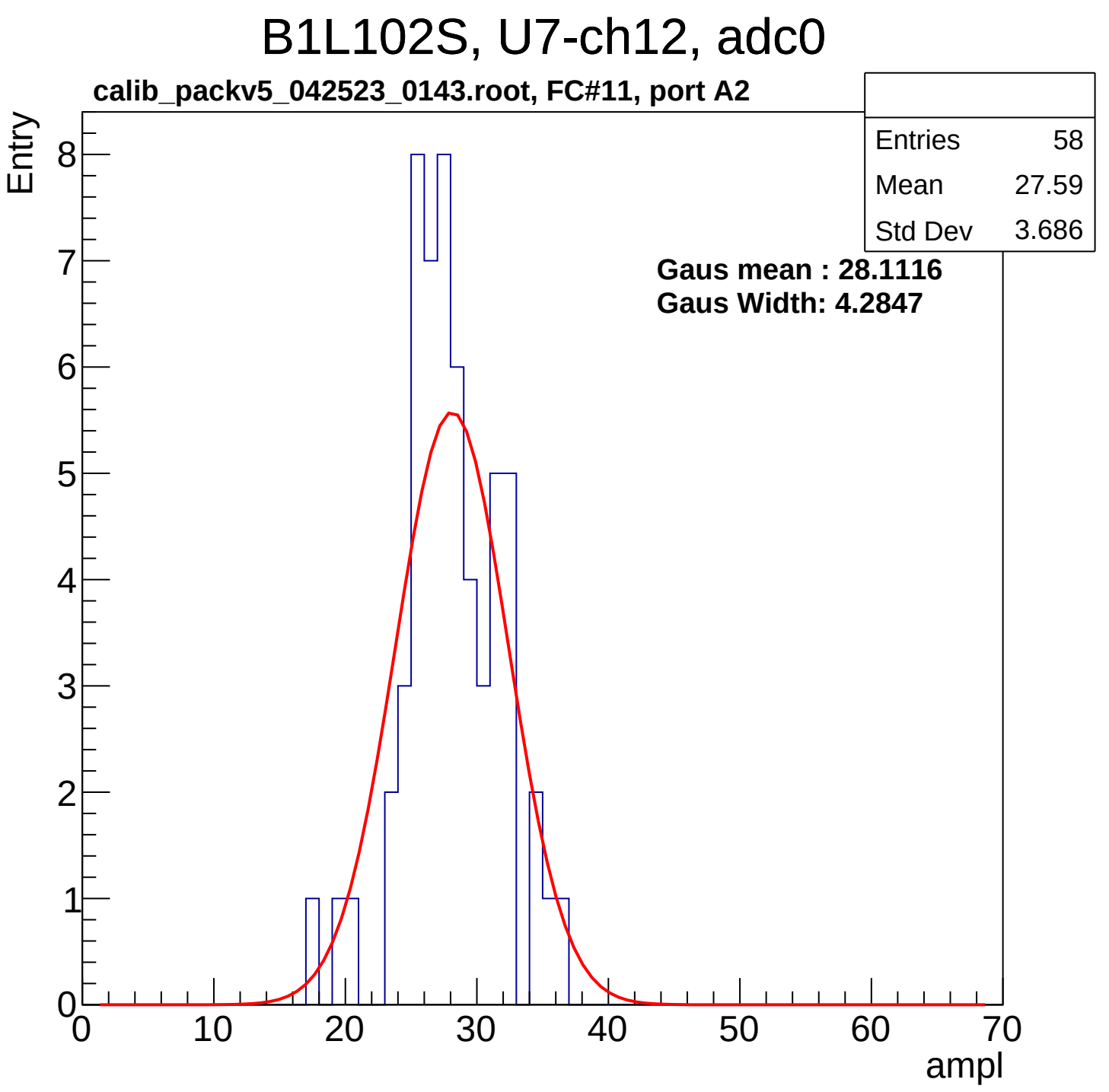

B1L102S, U7-ch11, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 9
Mean 54.67
Std Dev 19.37
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L102S, U7-ch11, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U7-ch12, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 58
Mean 27.59
Std Dev 3.686
Gaus mean : 28.1116
Gaus Width: 4.2847
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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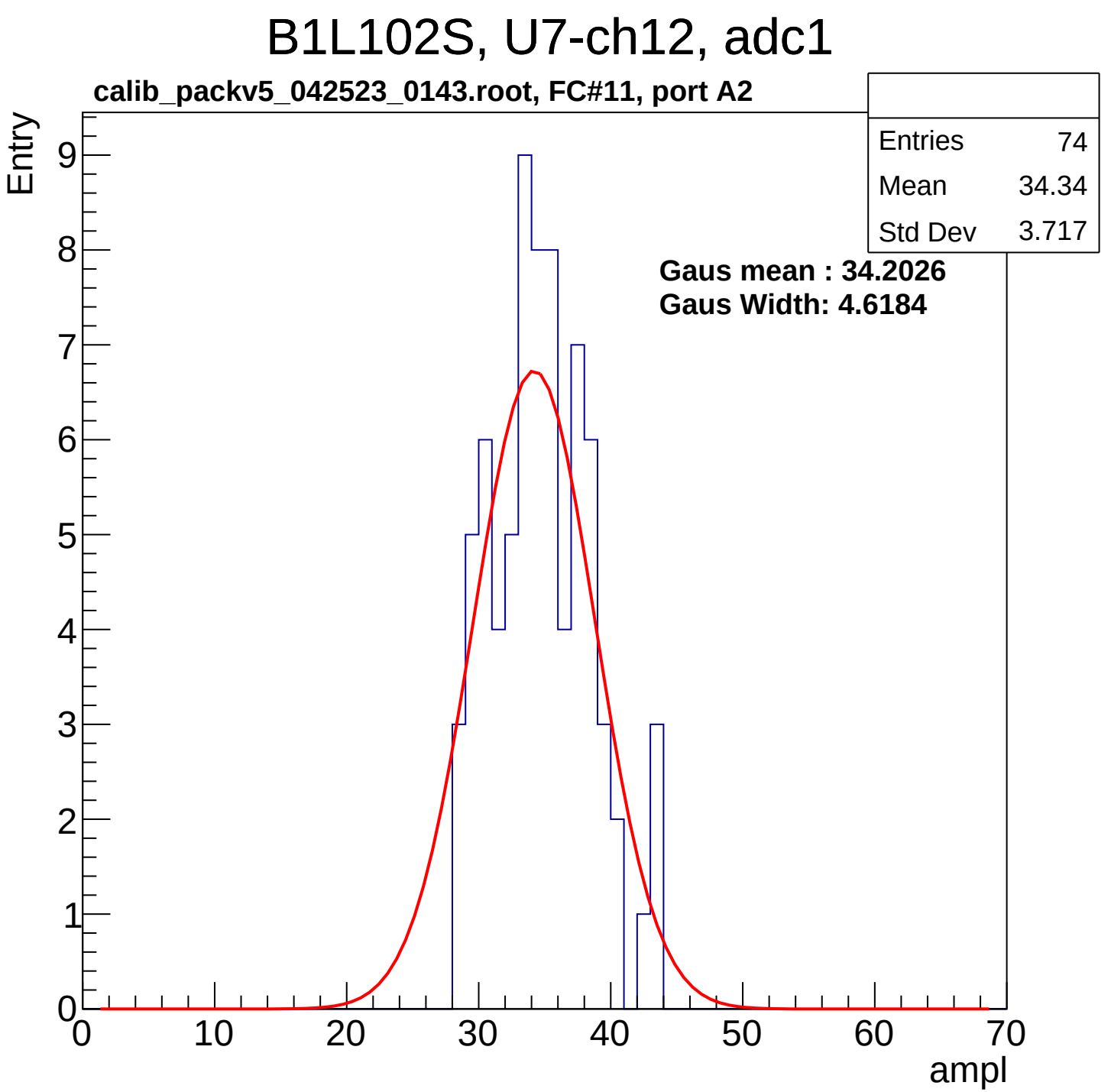
B1L102S, U7-ch12, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 74
Mean 34.34
Std Dev 3.717
Gaus mean : 34.2026
Gaus Width: 4.6184
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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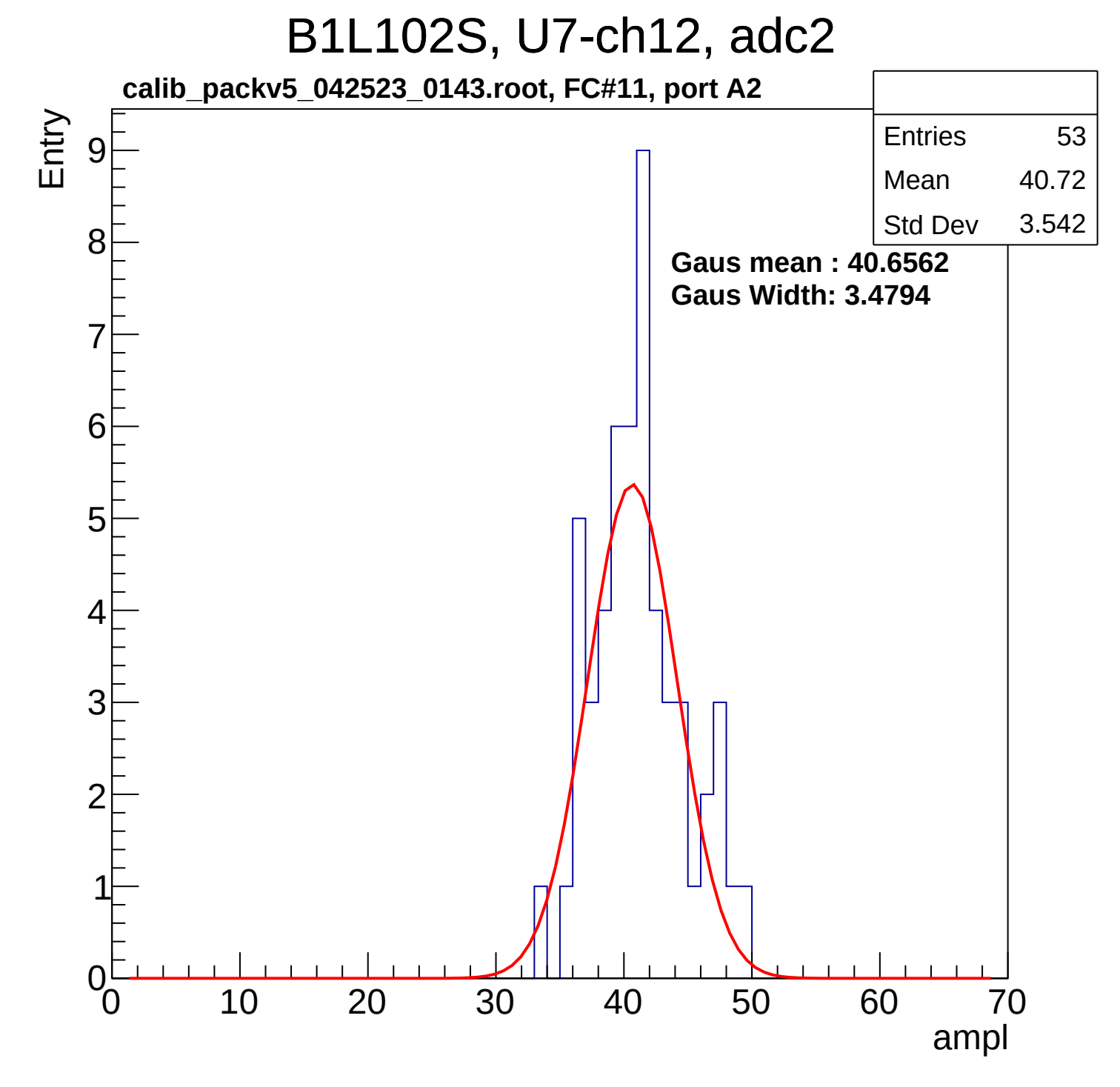
B1L102S, U7-ch12, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 53
Mean 40.72
Std Dev 3.542
Gaus mean : 40.6562
Gaus Width: 3.4794
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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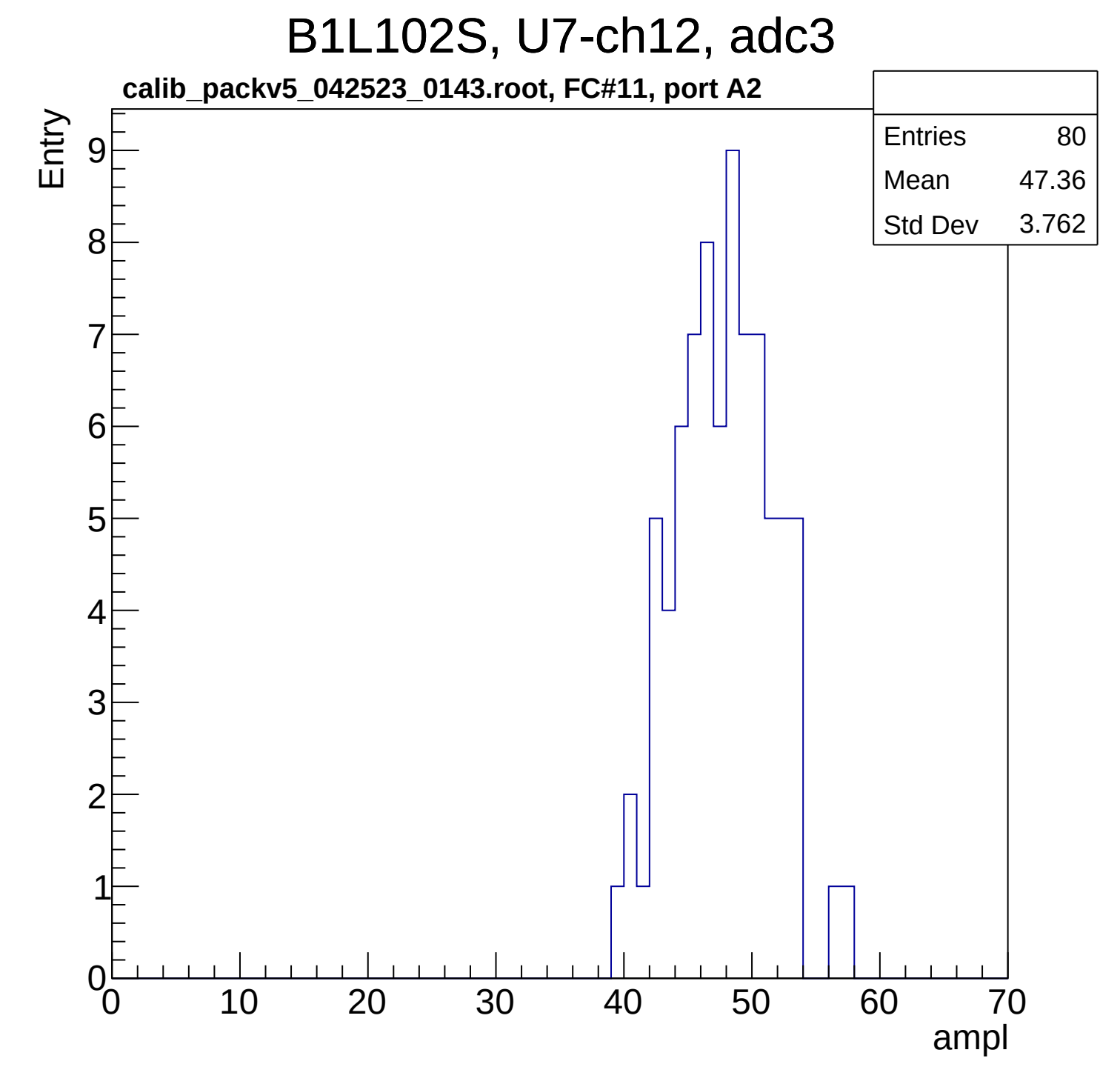
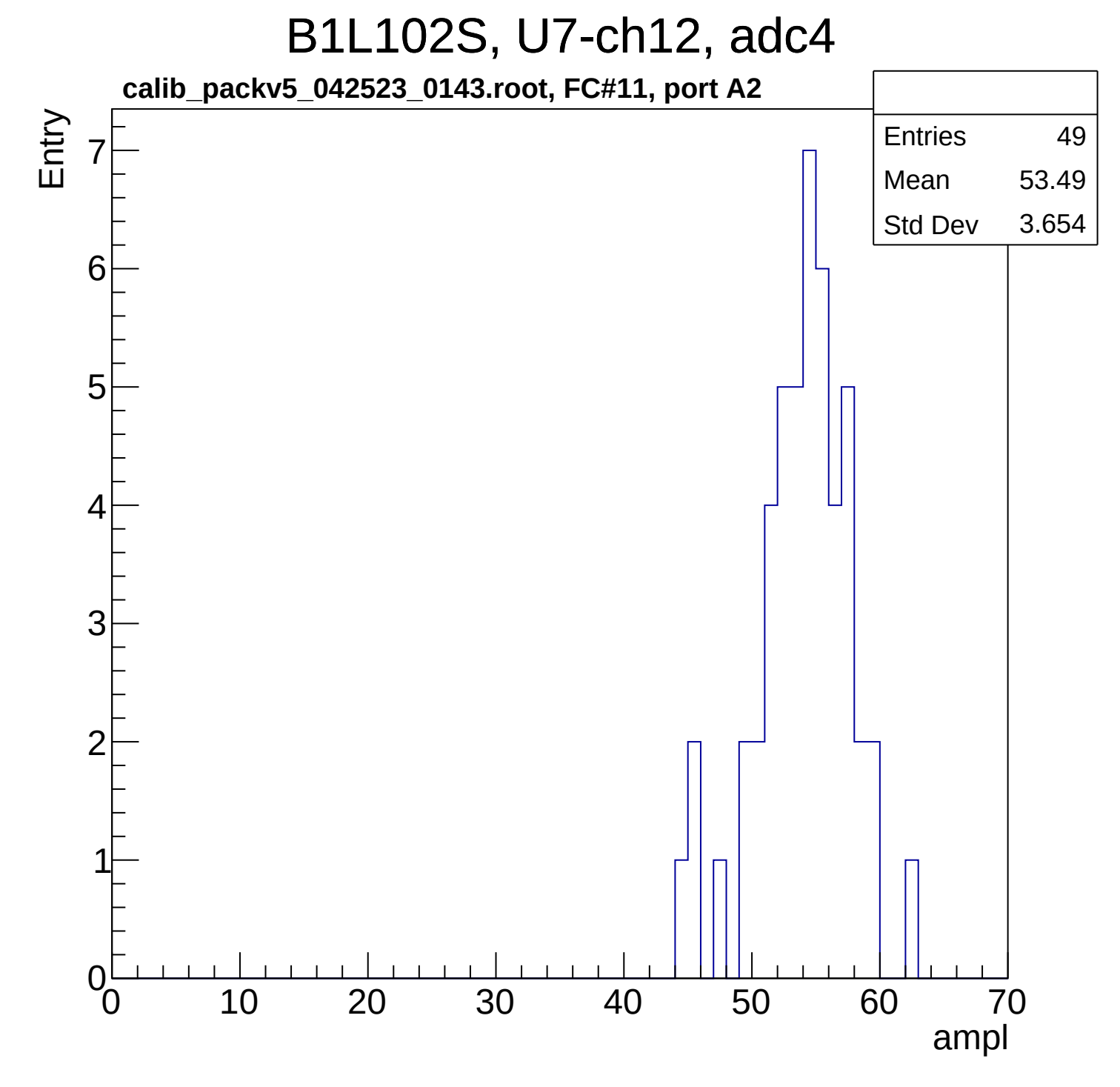
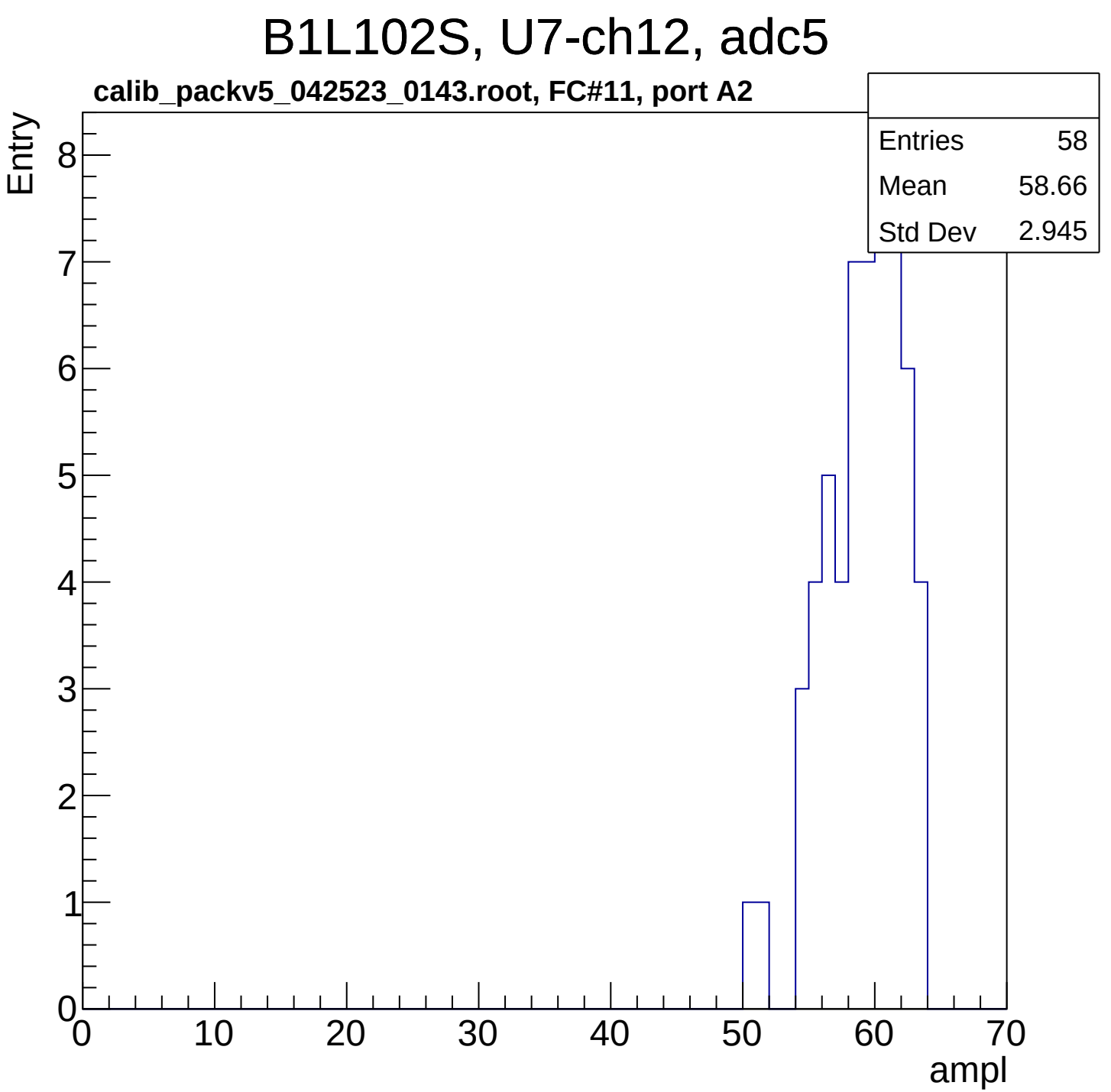
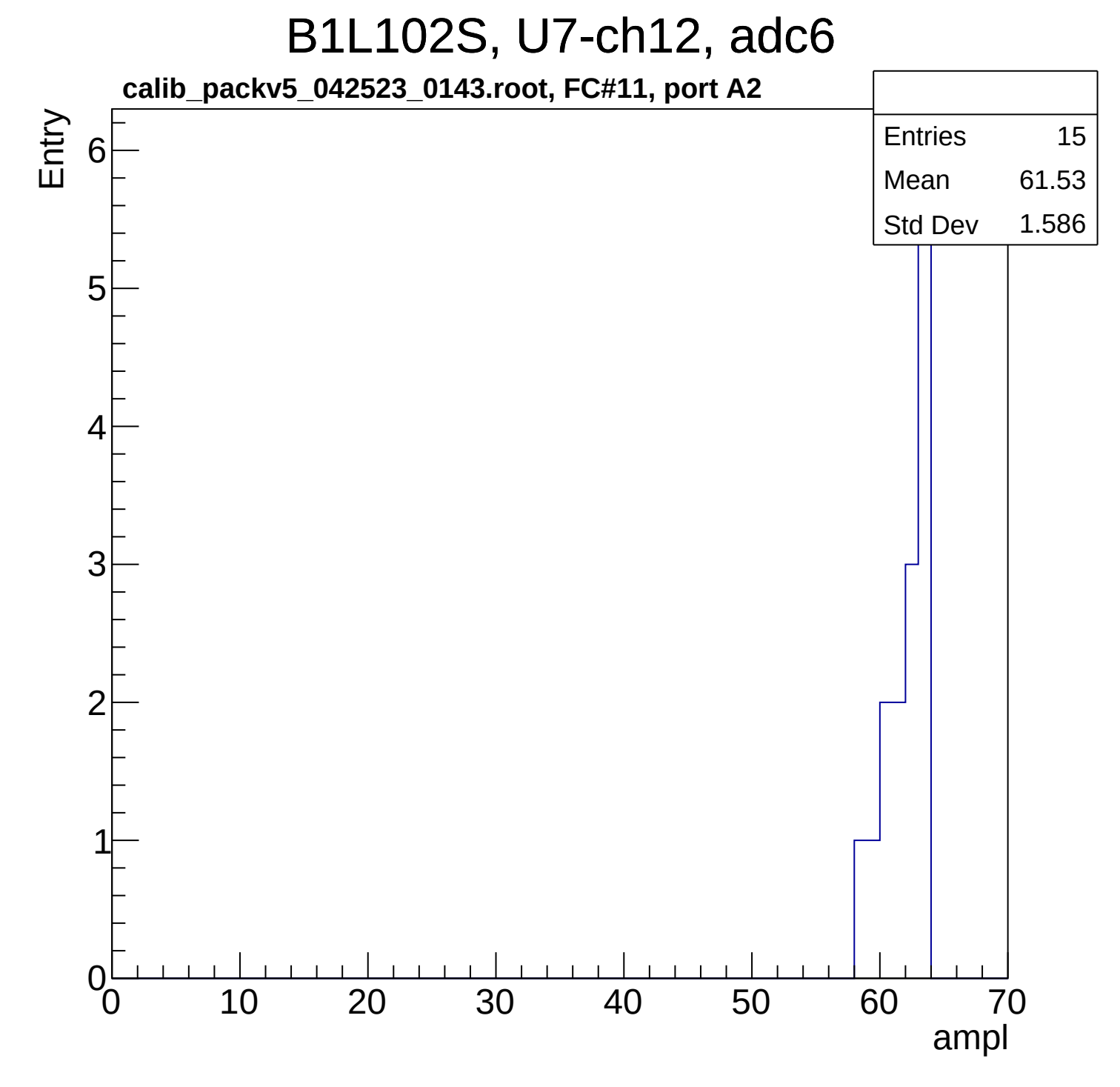
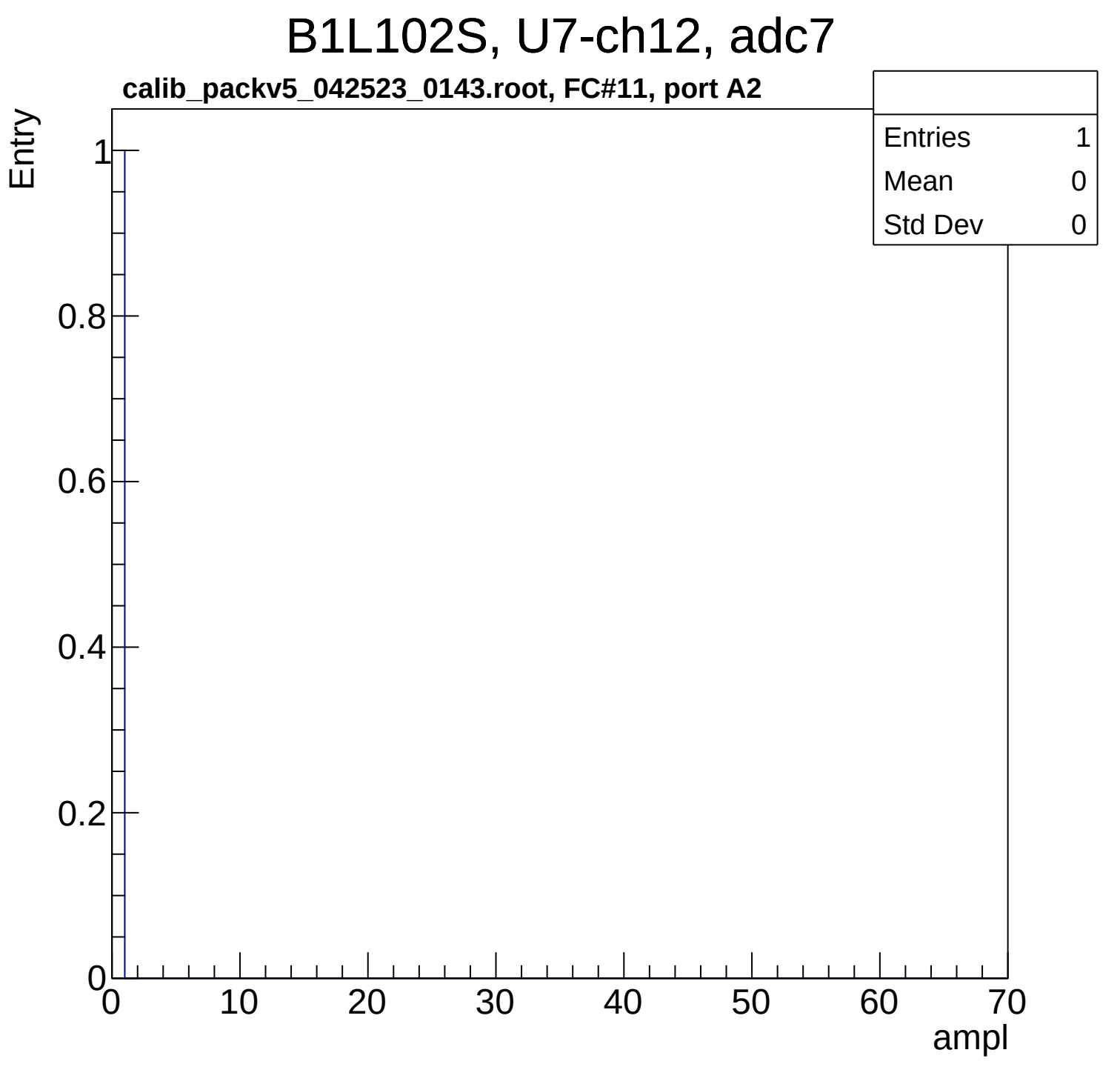
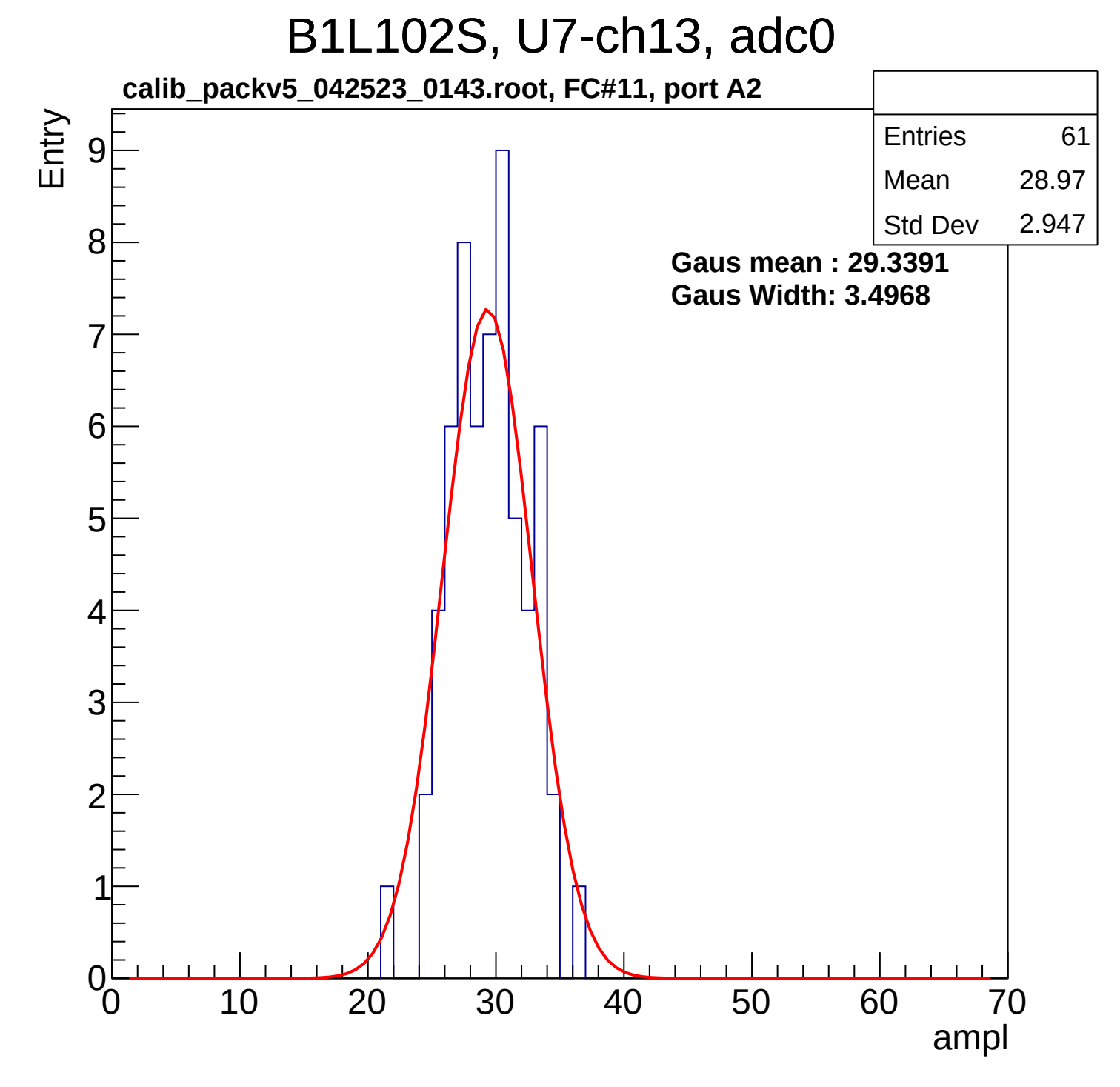

B1L102S, U7-ch12, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 80
Mean 47.36
Std Dev 3.762
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

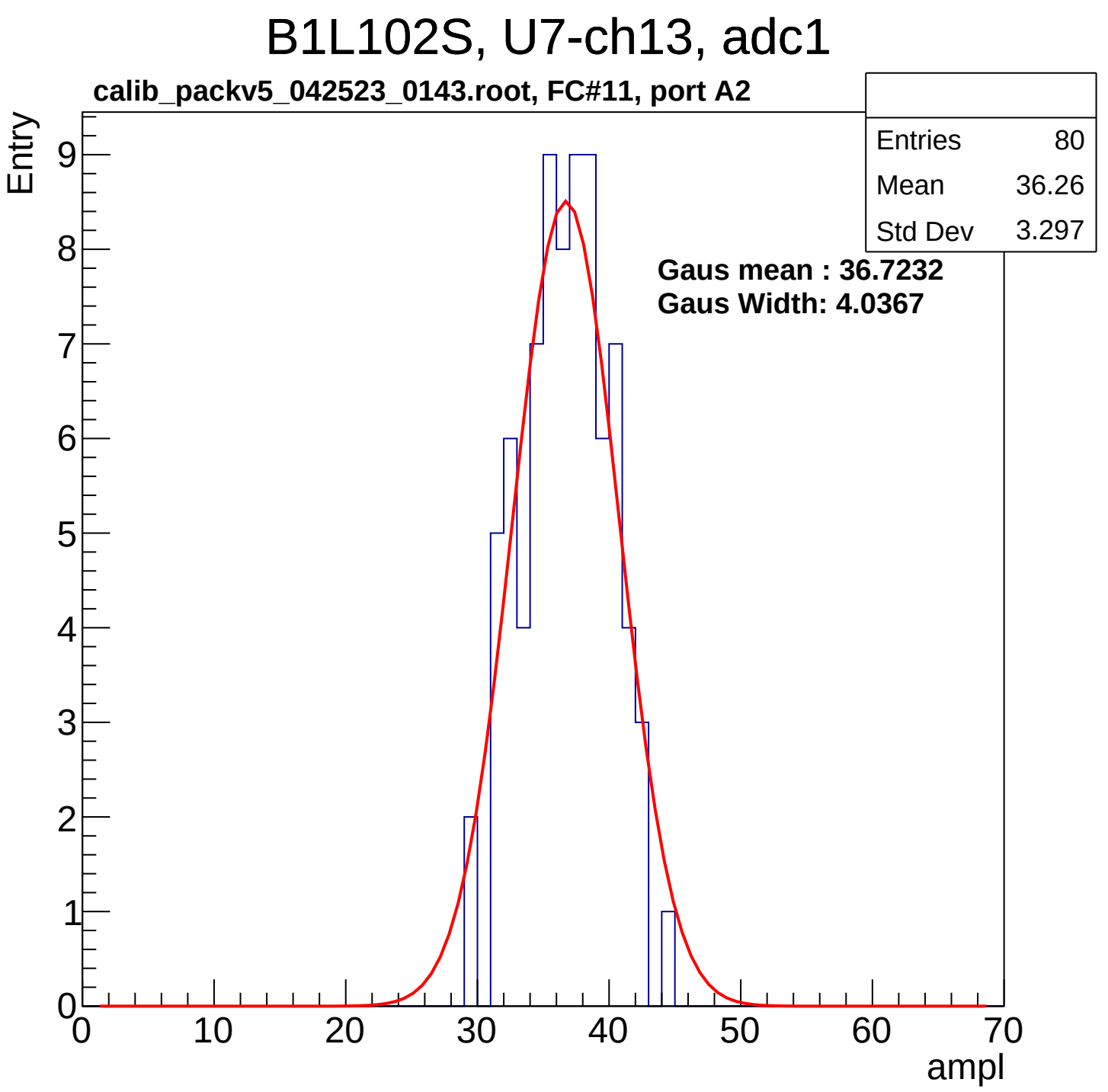

B1L102S, U7-ch12, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 49
Mean 53.49
Std Dev 3.654
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L102S, U7-ch12, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 58
Mean 58.66
Std Dev 2.945
Entry
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L102S, U7-ch12, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 15
Mean 61.53
Std Dev 1.586
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L102S, U7-ch12, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U7-ch13, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 61
Mean 28.97
Std Dev 2.947
Gaus mean : 29.3391
Gaus Width: 3.4968
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L102S, U7-ch13, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 80
Mean 36.26
Std Dev 3.297
Gaus mean : 36.7232
Gaus Width: 4.0367
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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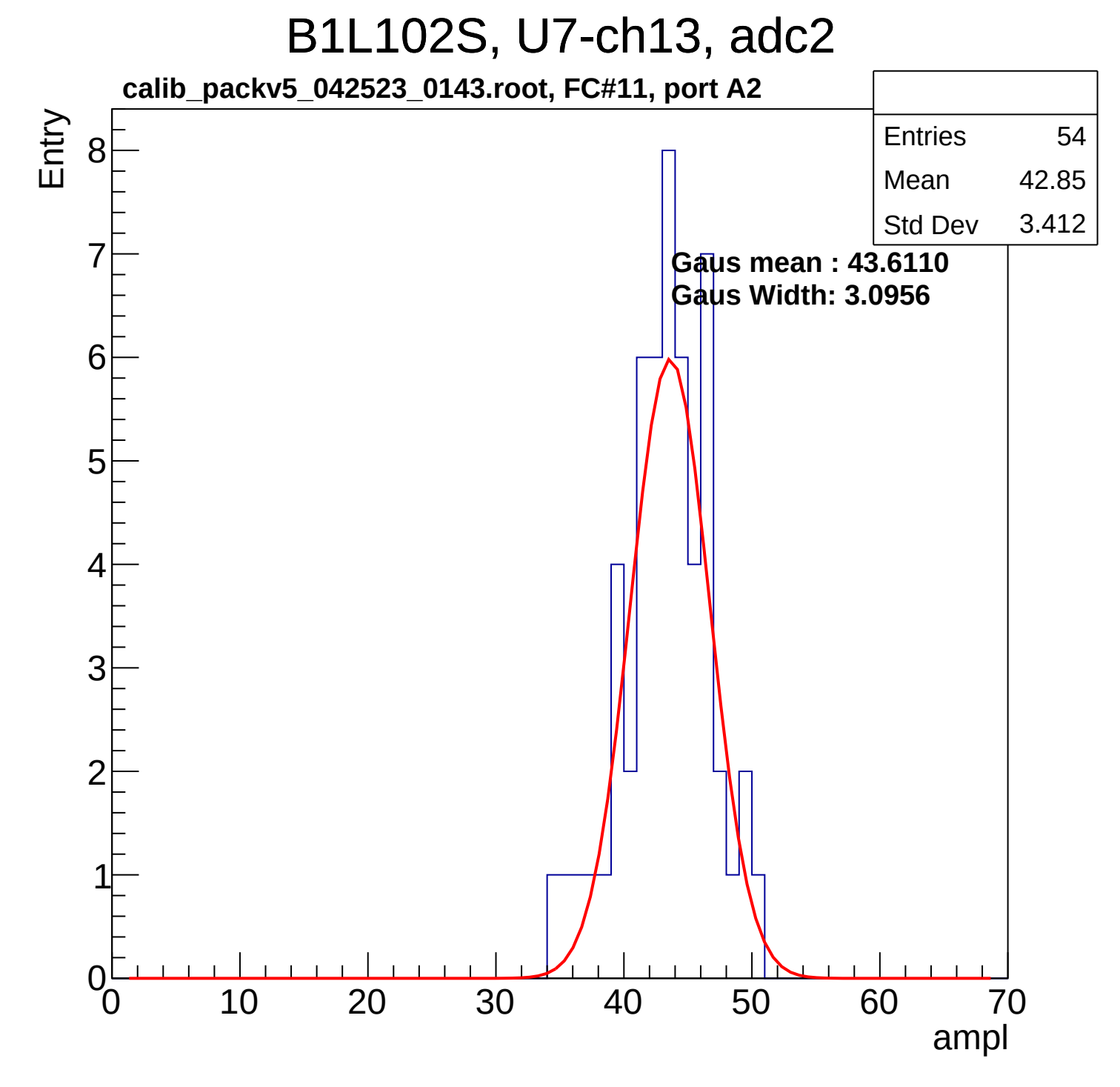
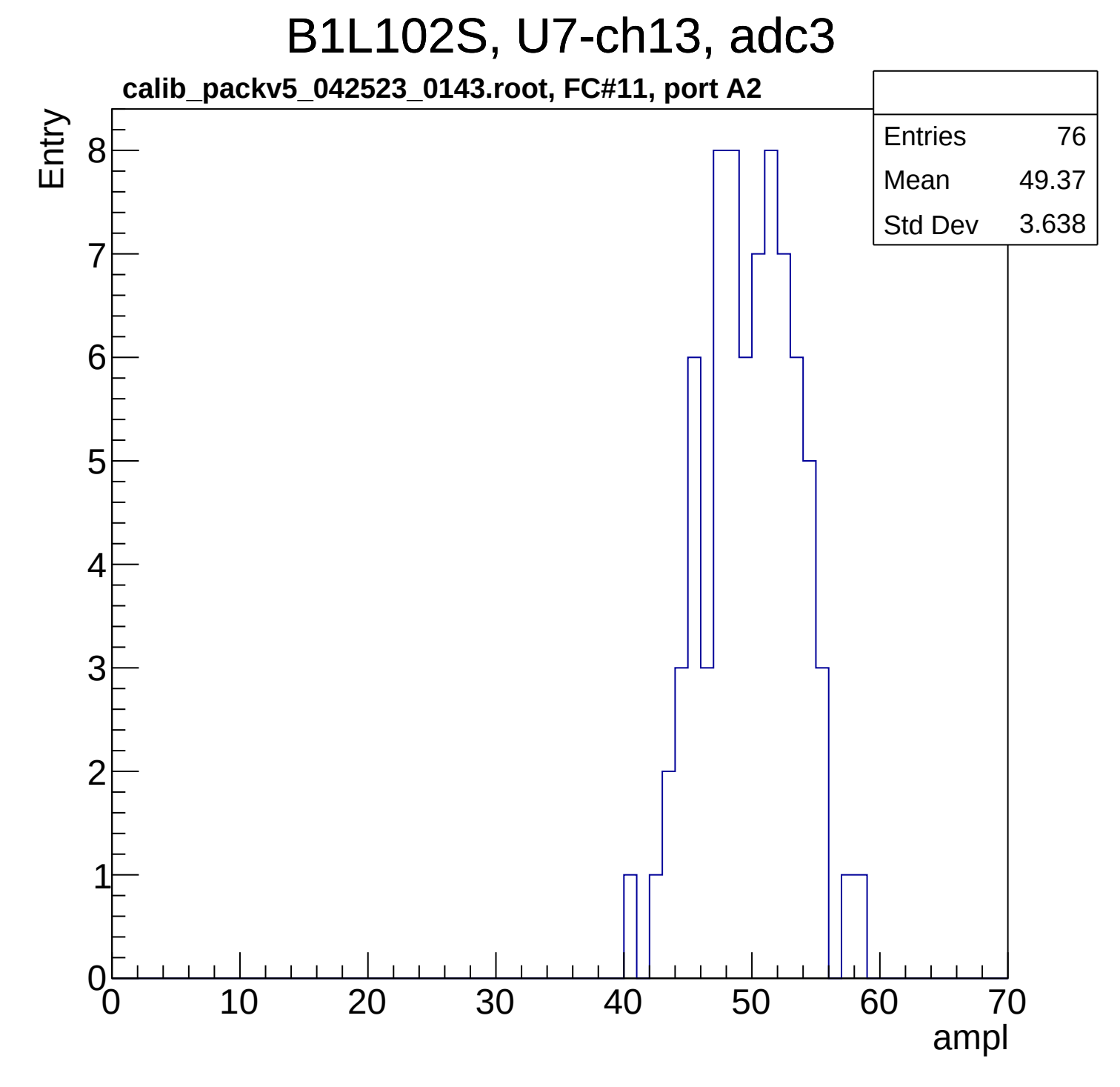
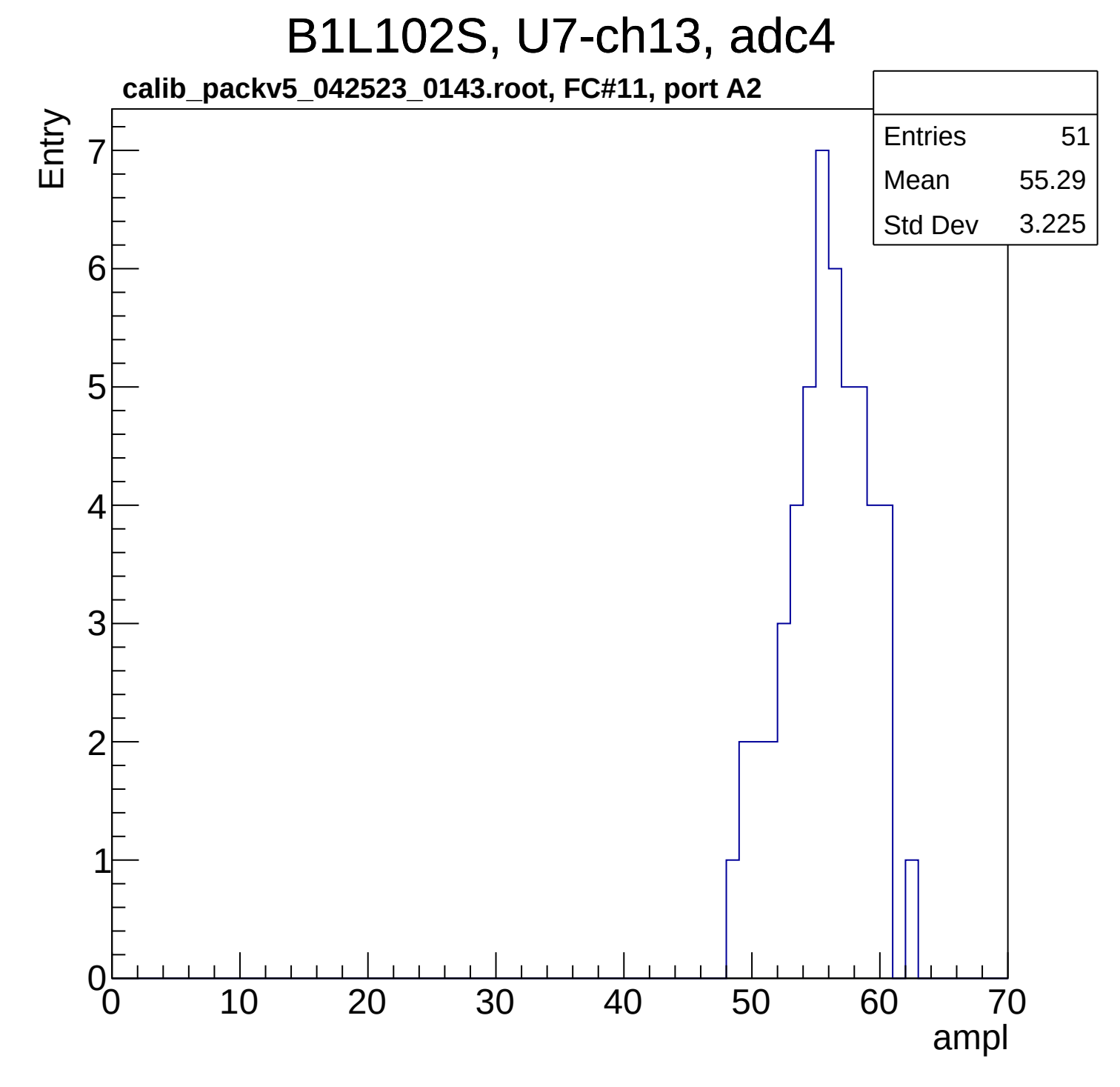
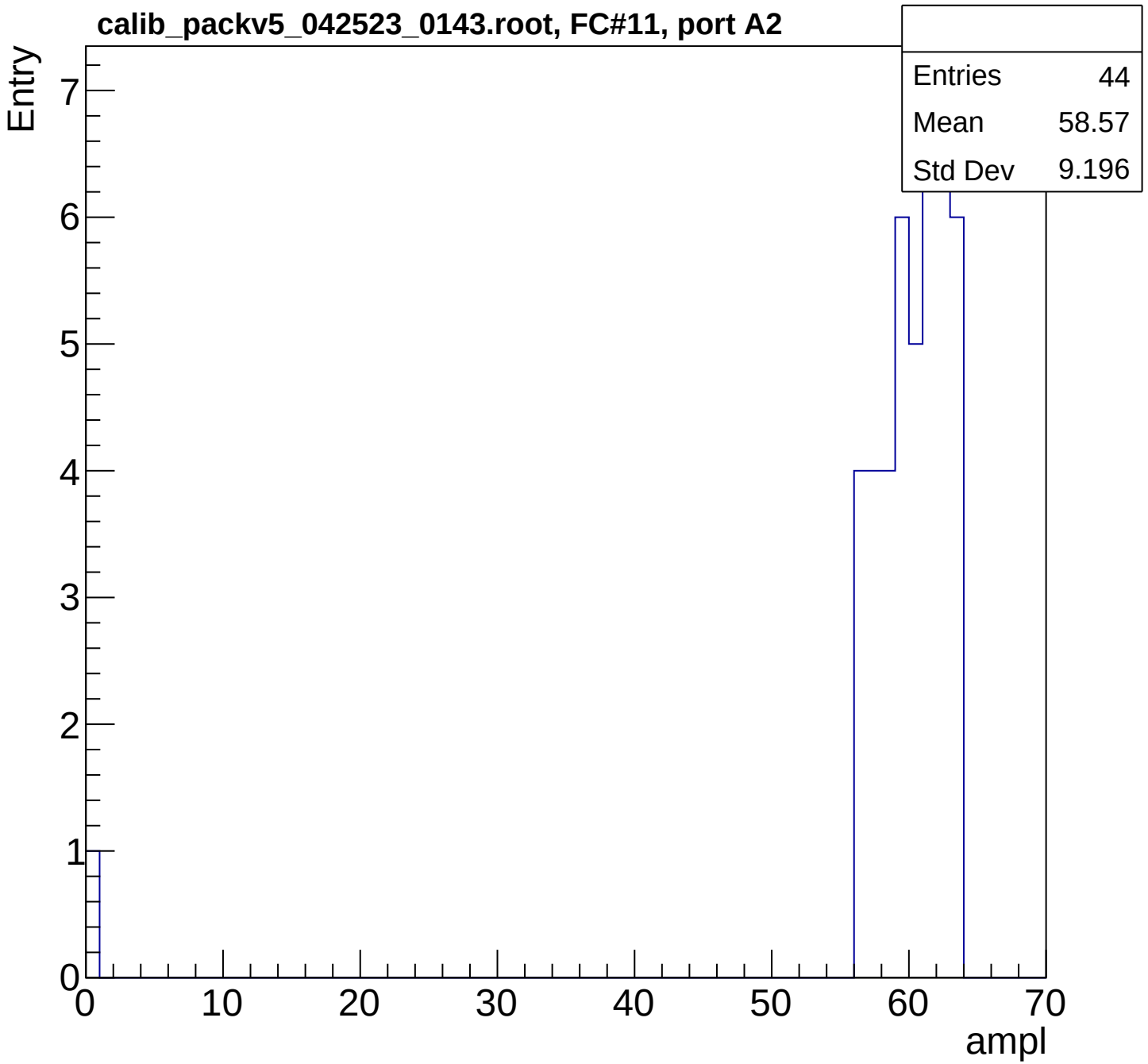
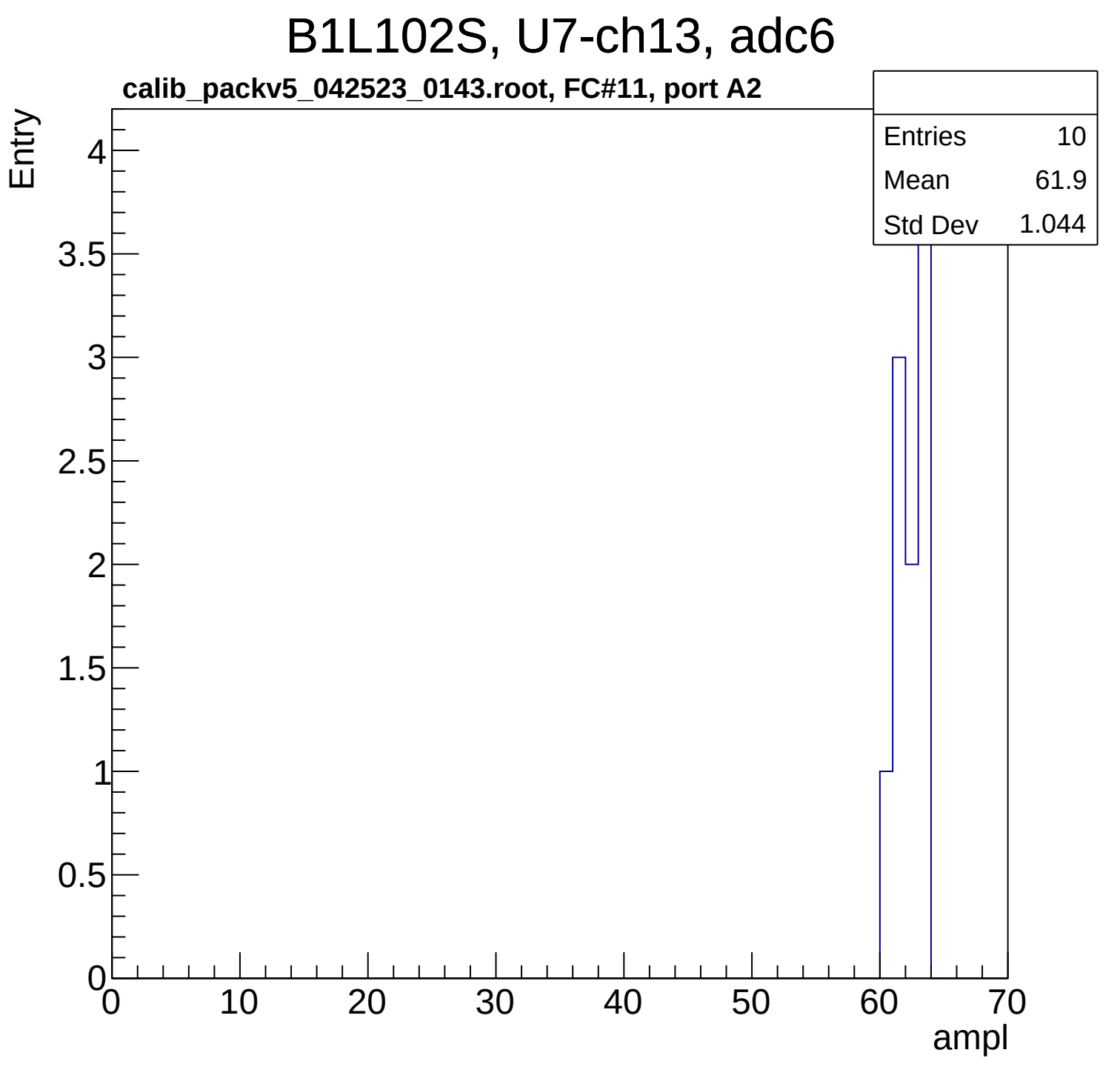

B1L102S, U7-ch13, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 54
Mean 42.85
Std Dev 3.412
Gaus mean : 43.6110
Gaus Width: 3.0956
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L102S, U7-ch13, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 76
Mean 49.37
Std Dev 3.638
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L102S, U7-ch13, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 51
Mean 55.29
Std Dev 3.225
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L102S, U7-ch13, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 44
Mean 58.57
Std Dev 9.196
Entry
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70
ampl


B1L102S, U7-ch13, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 10
Mean 61.9
Std Dev 1.044
Entry
ampl
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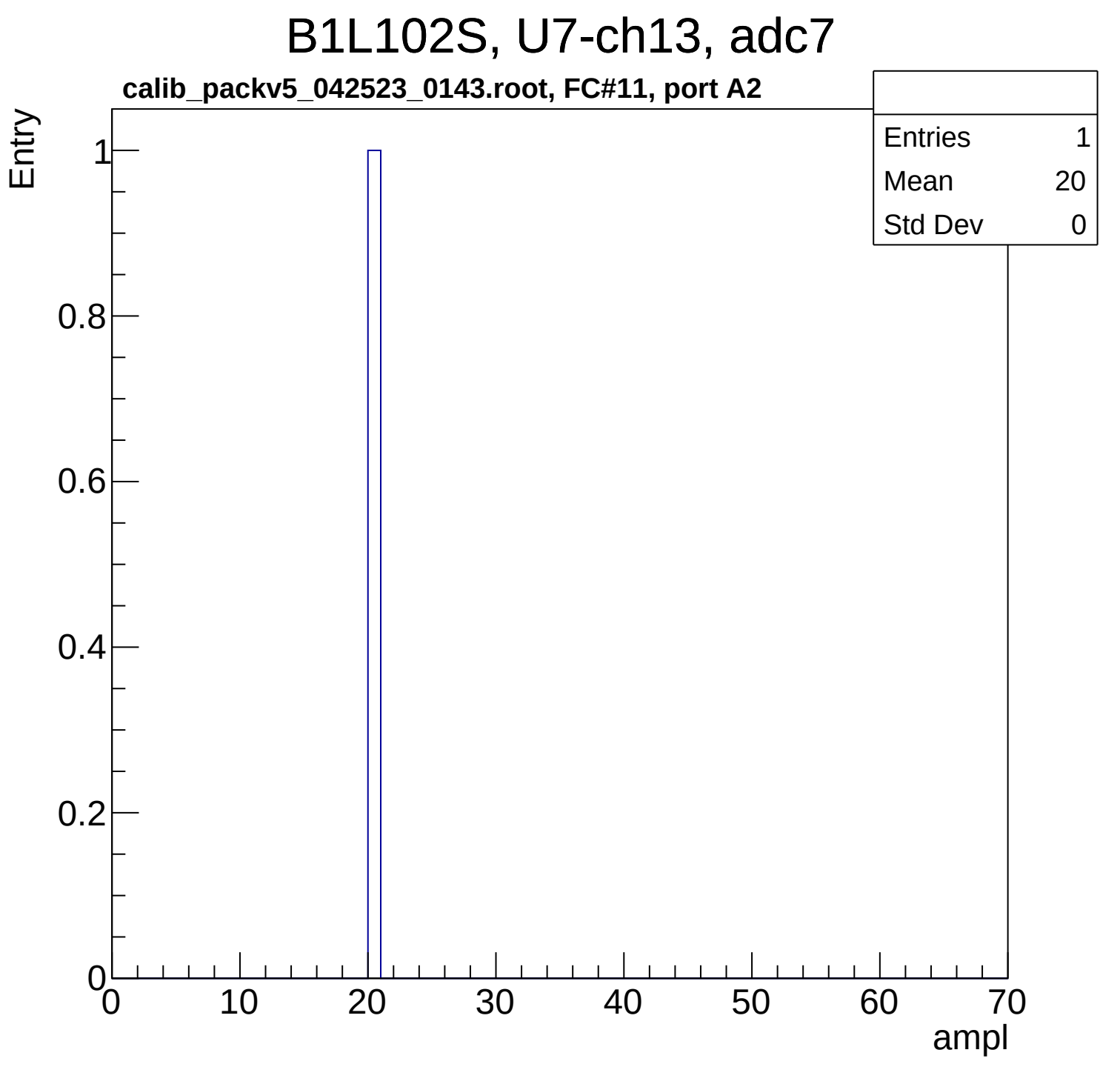
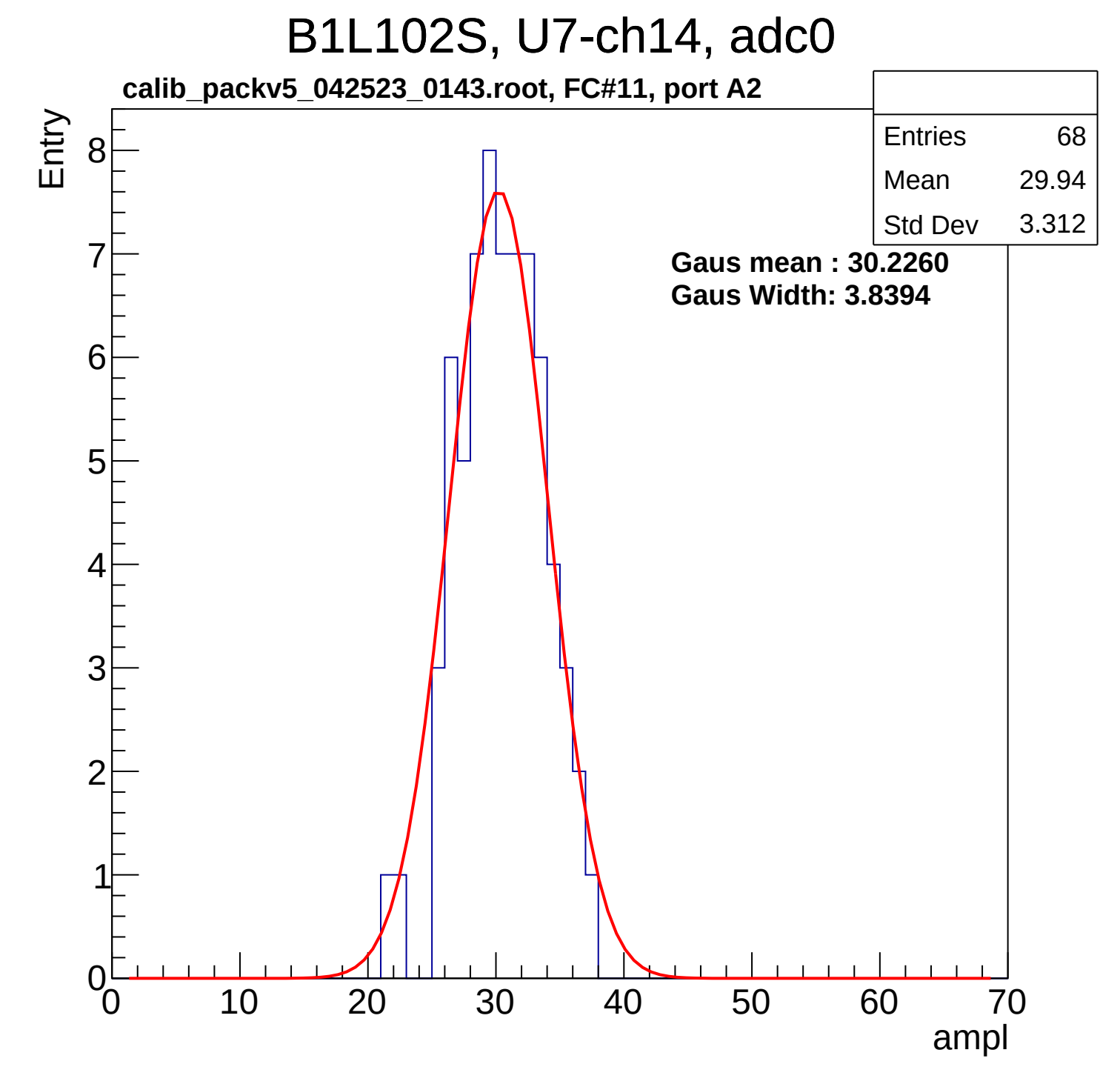
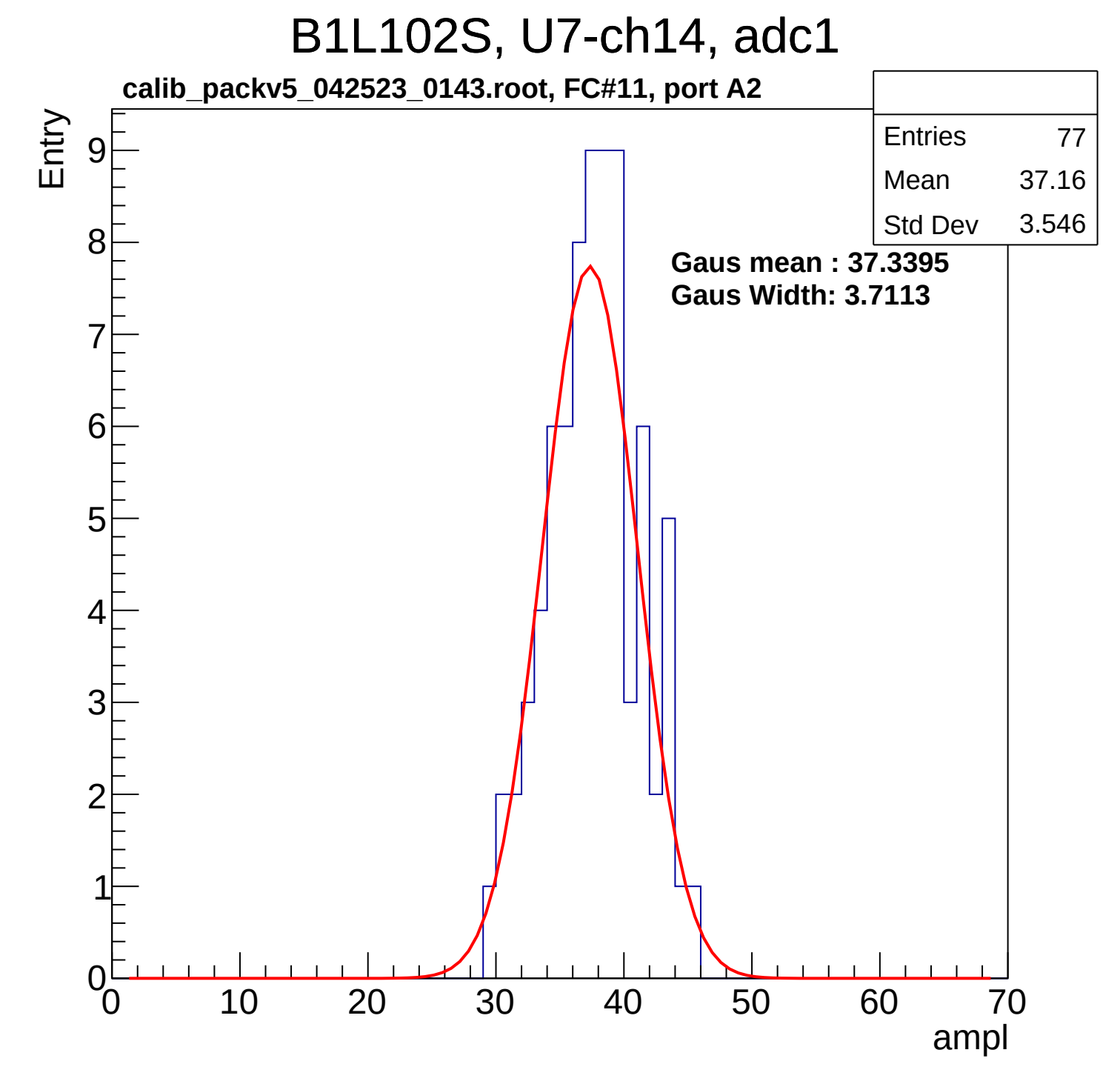
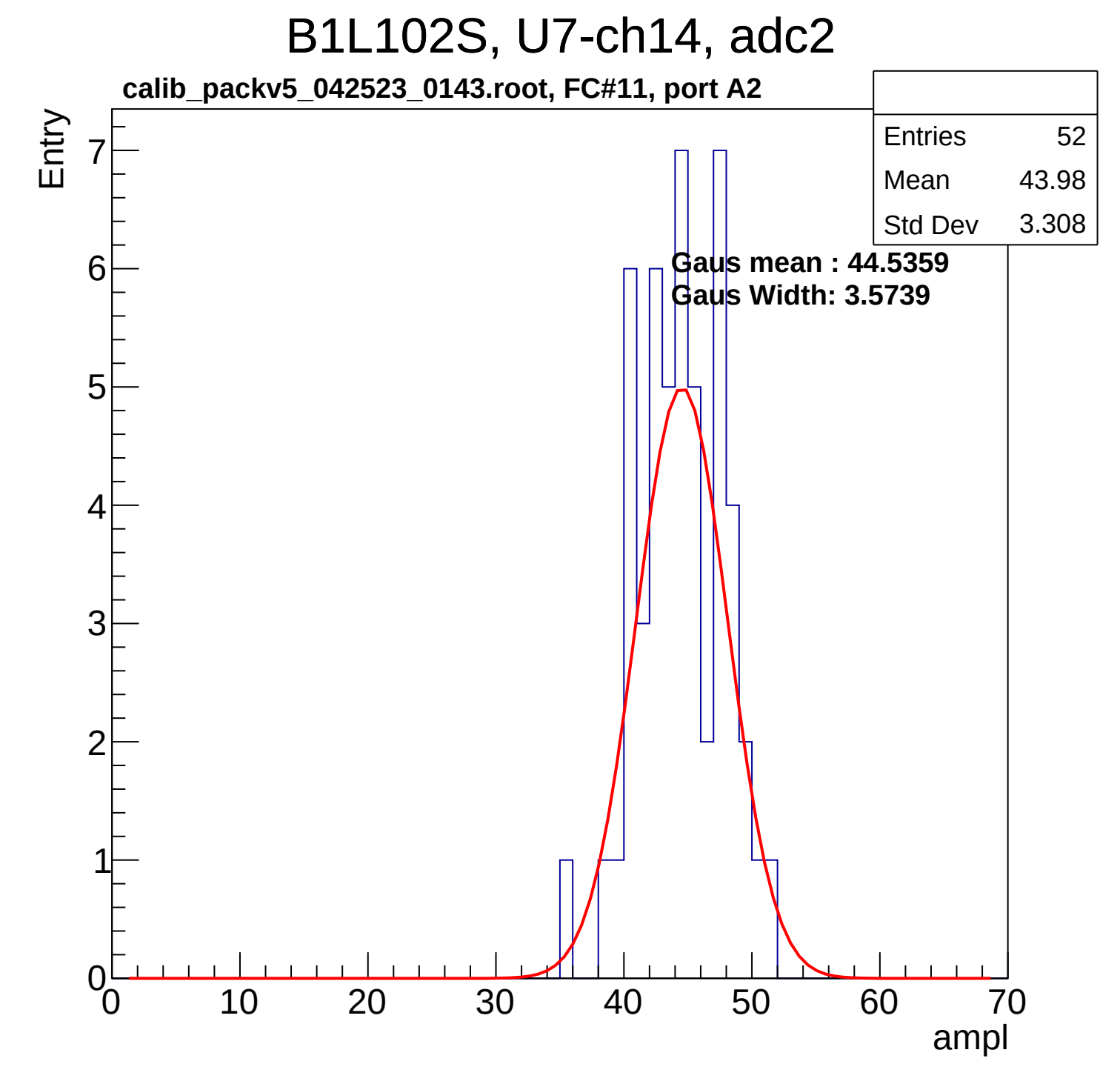
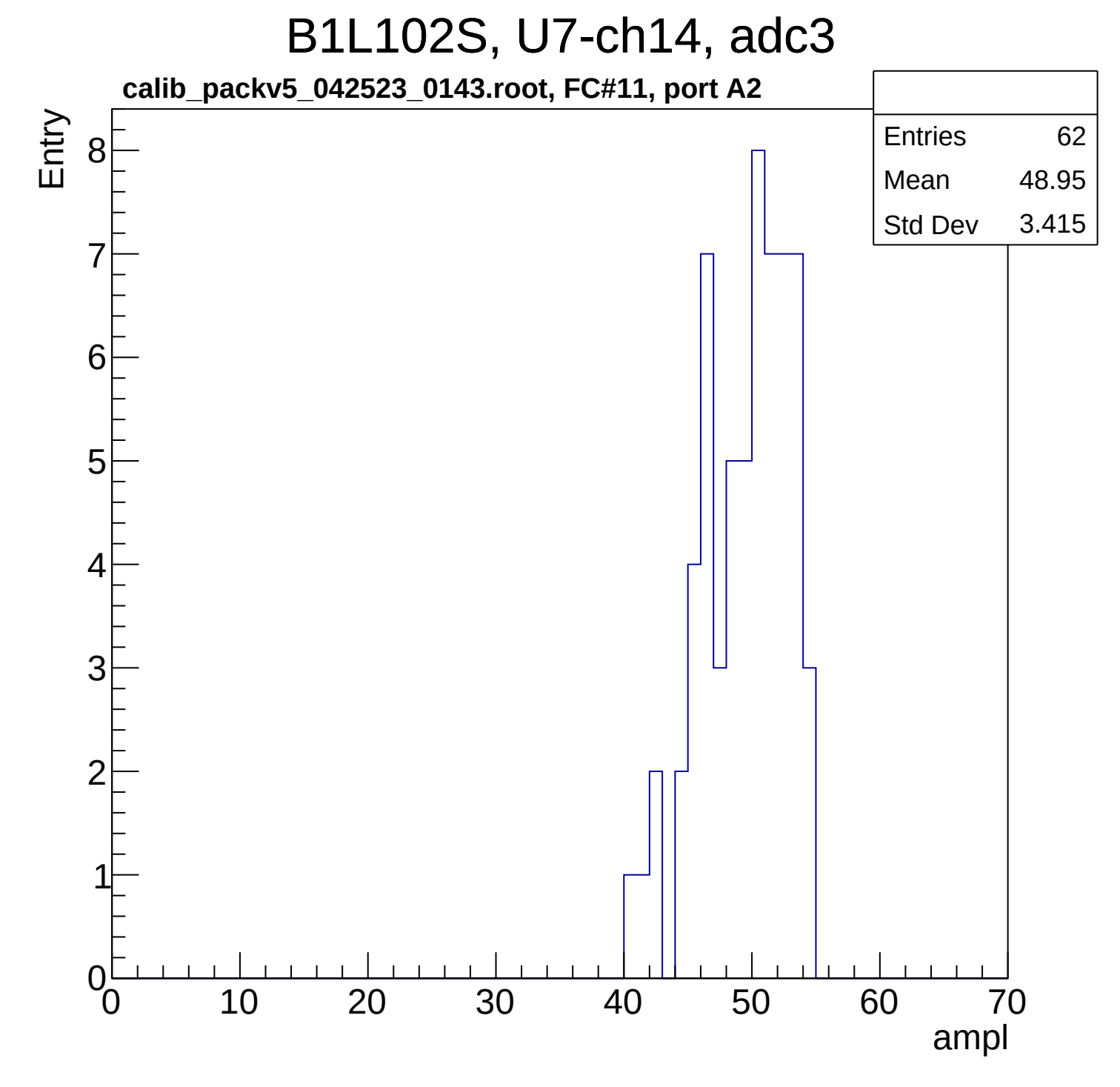
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L102S, U7-ch13, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 1
Mean 20
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70


B1L102S, U7-ch14, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 68
Mean 29.94
Std Dev 3.312
Gaus mean : 30.2260
Gaus Width: 3.8394
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L102S, U7-ch14, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 77
Mean 37.16
Std Dev 3.546
Gaus mean : 37.3395
Gaus Width: 3.7113
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L102S, U7-ch14, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 52
Mean 43.98
Std Dev 3.308
Gaus mean : 44.5359
Gaus Width: 3.5739
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L102S, U7-ch14, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 62
Mean 48.95
Std Dev 3.415
Entry
ampl
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3
4
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7
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0
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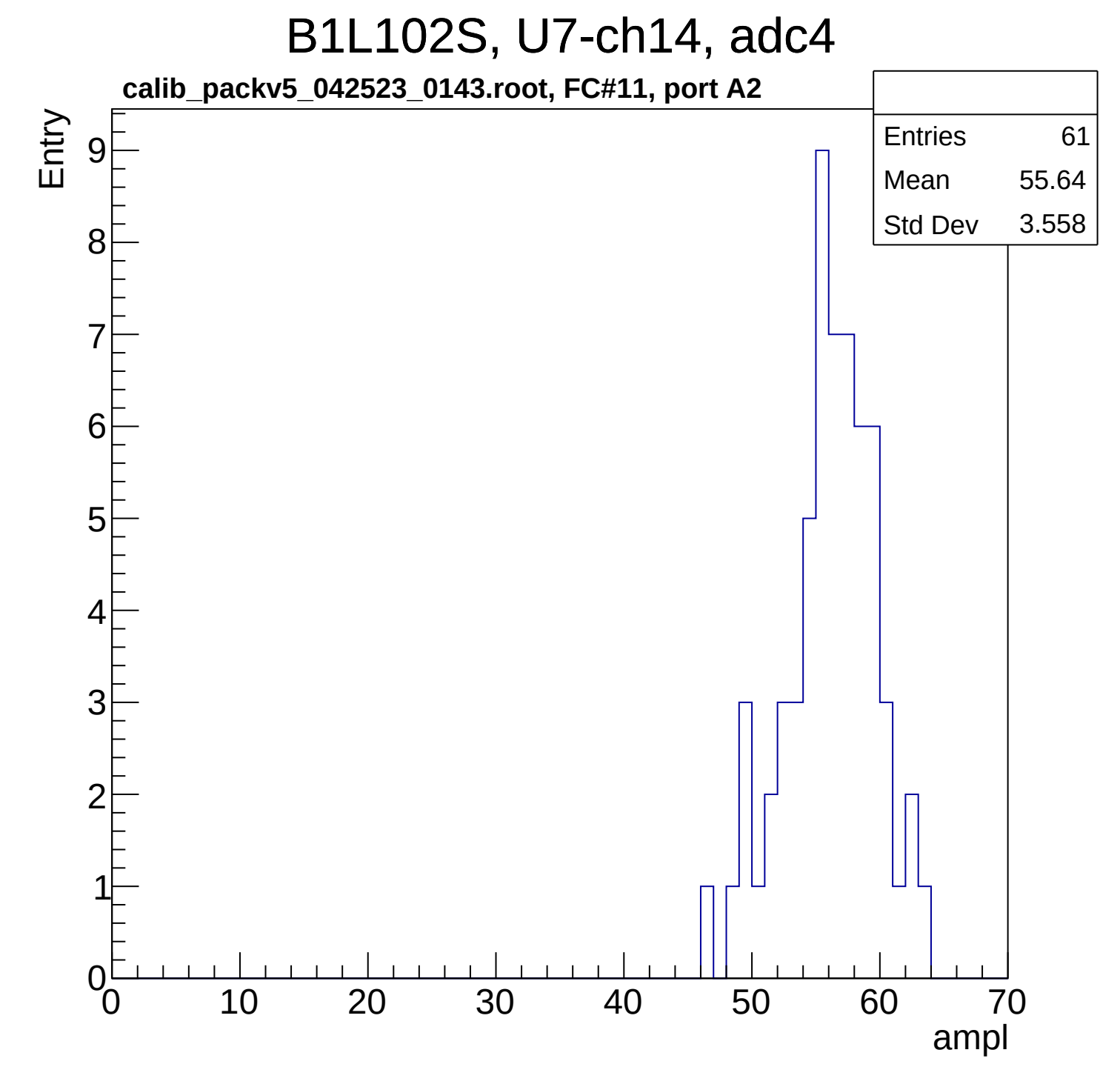
B1L102S, U7-ch14, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 61
Mean 55.64
Std Dev 3.558
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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60
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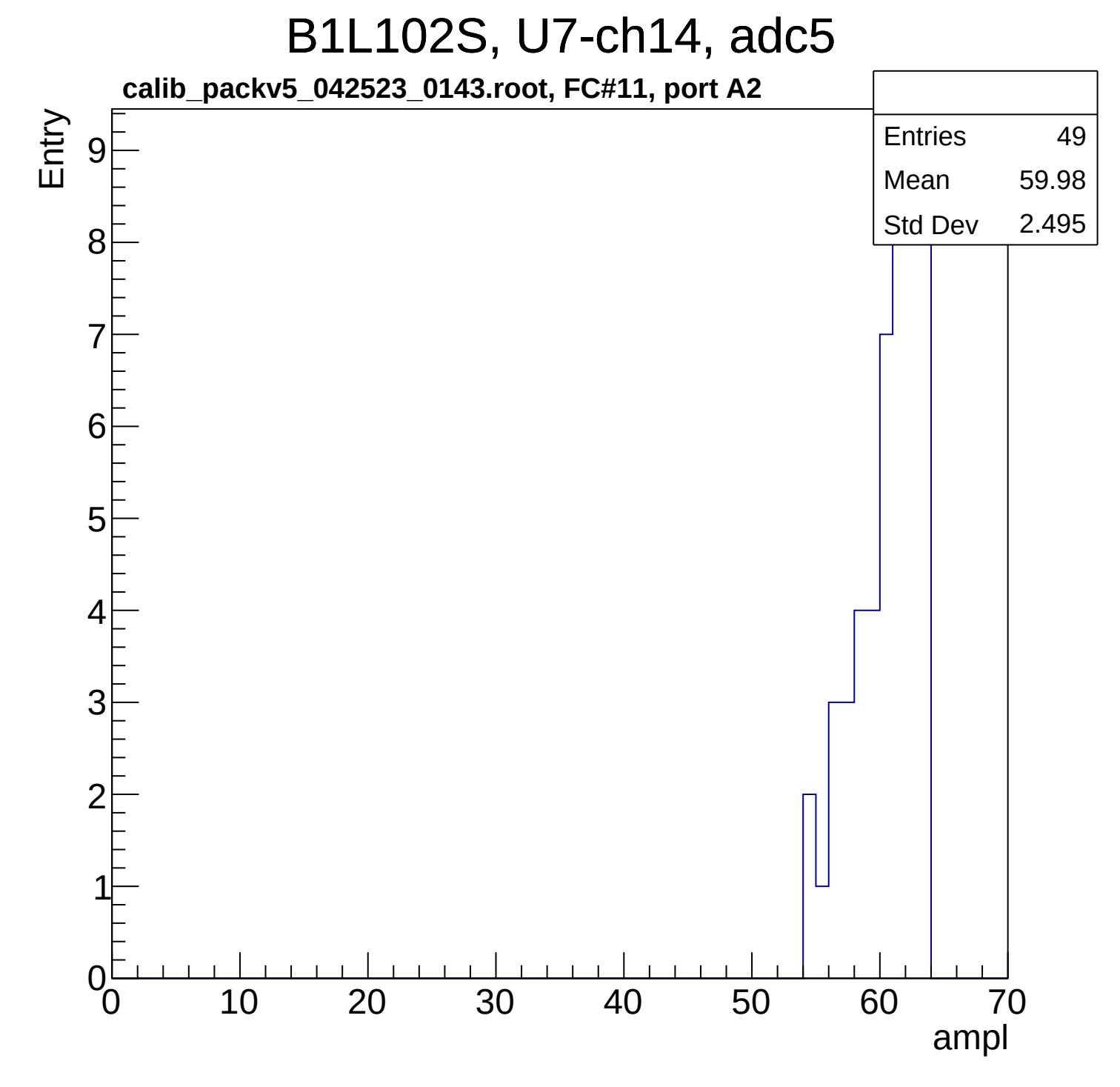
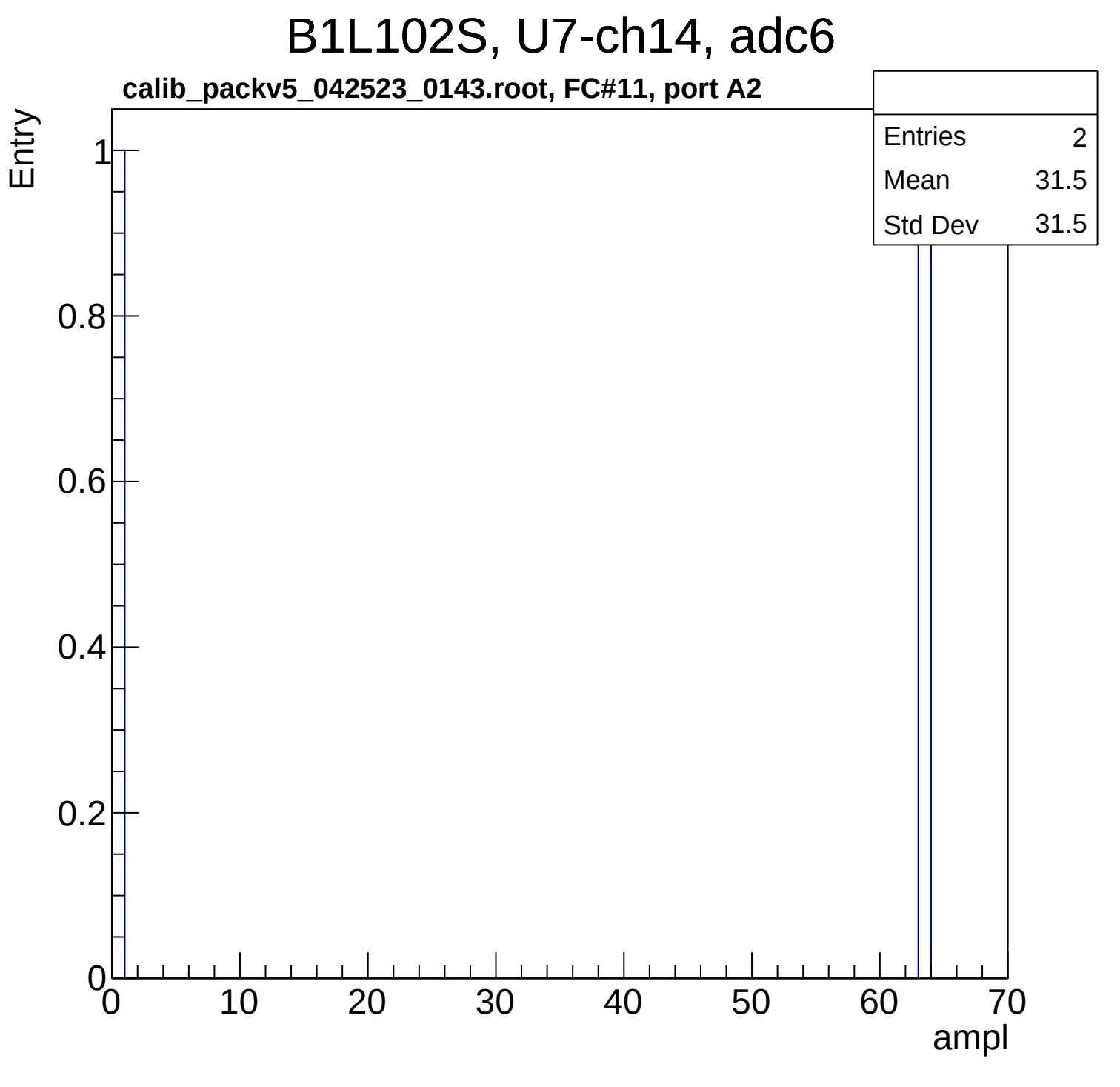
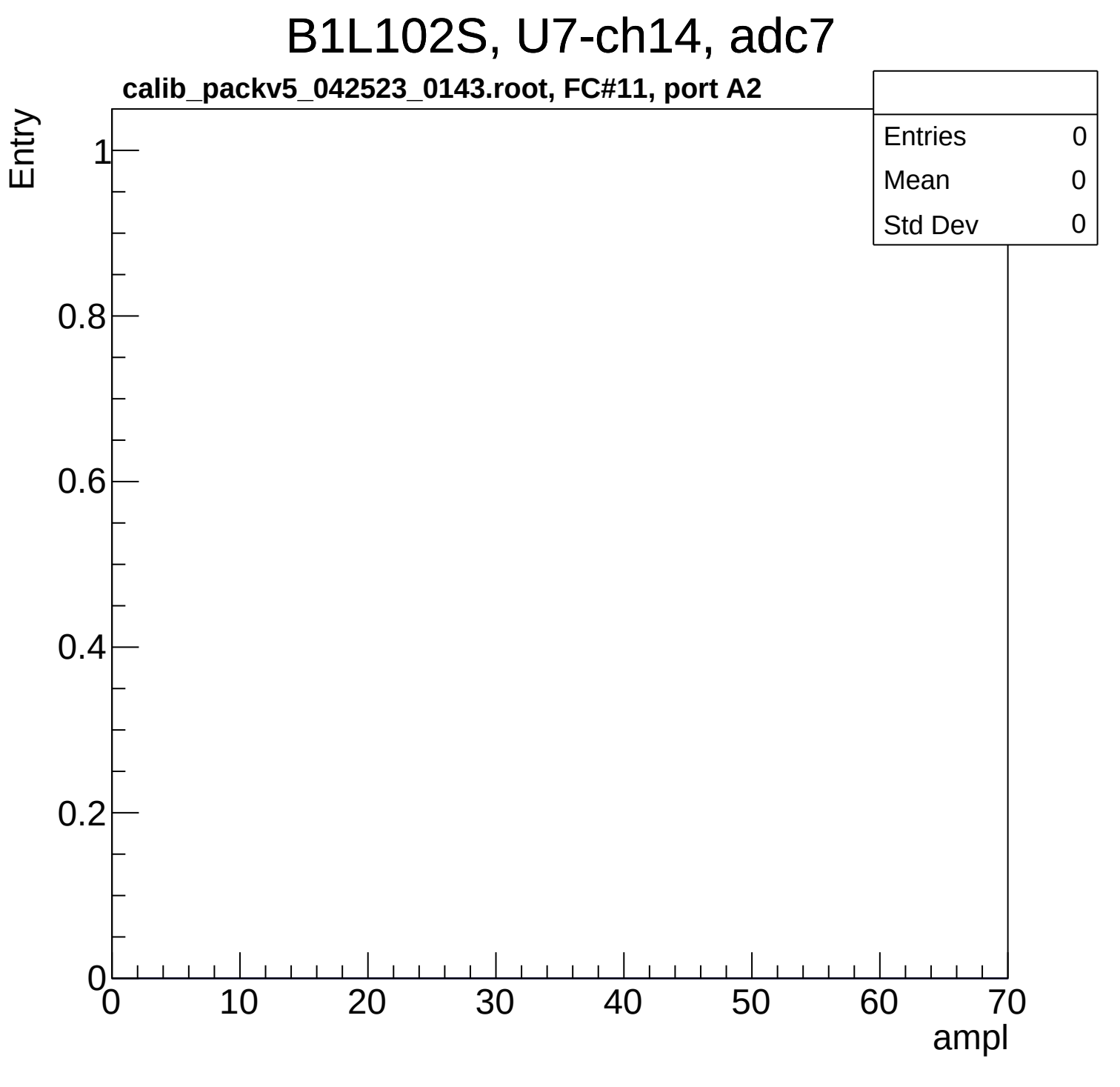

B1L102S, U7-ch14, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 49
Mean 59.98
Std Dev 2.495
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L102S, U7-ch14, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 2
Mean 31.5
Std Dev 31.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U7-ch14, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 0
Mean 0
Std Dev 0
Entry
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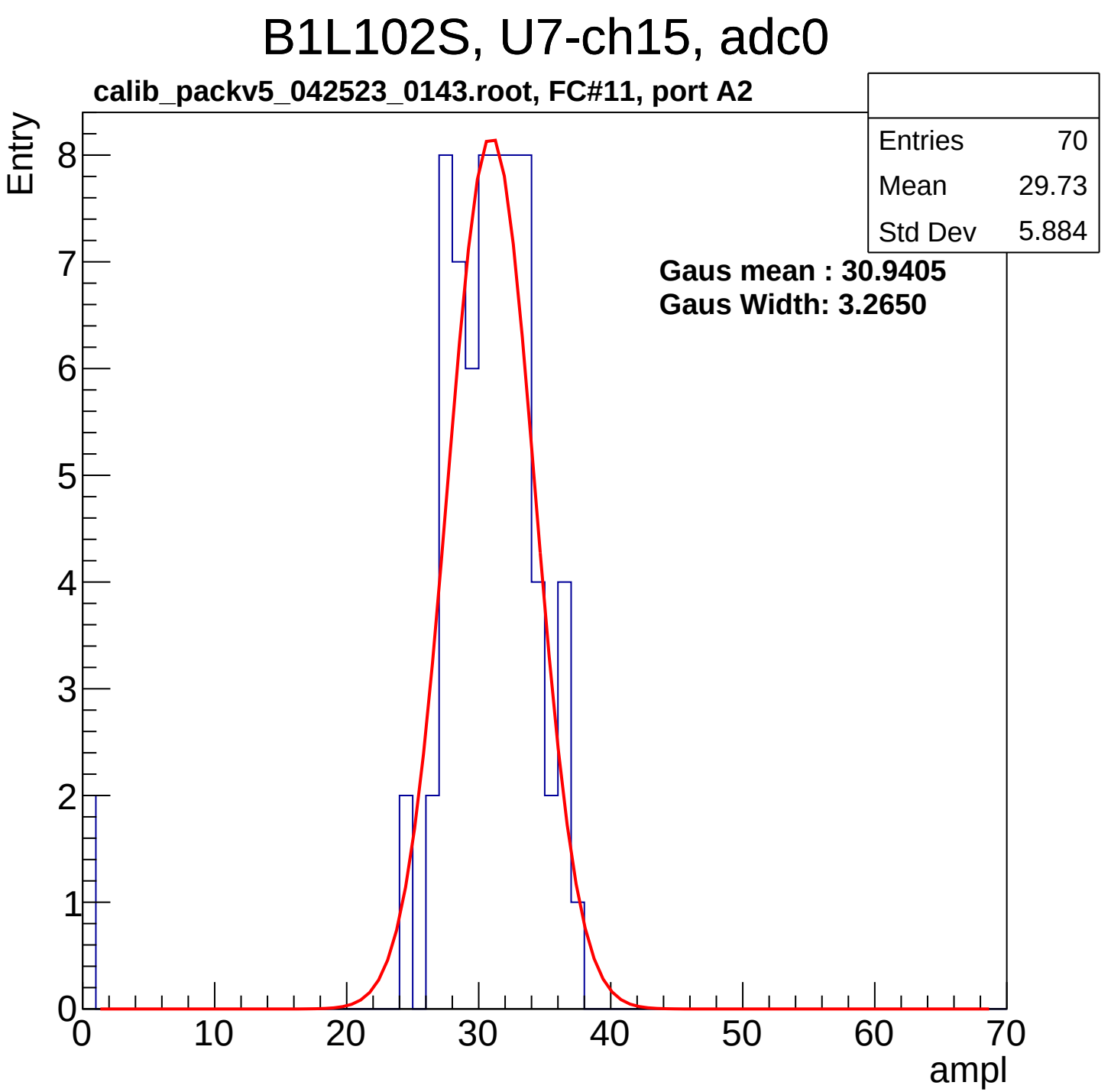
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U7-ch15, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 70
Mean 29.73
Std Dev 5.884
Gaus mean : 30.9405
Gaus Width: 3.2650
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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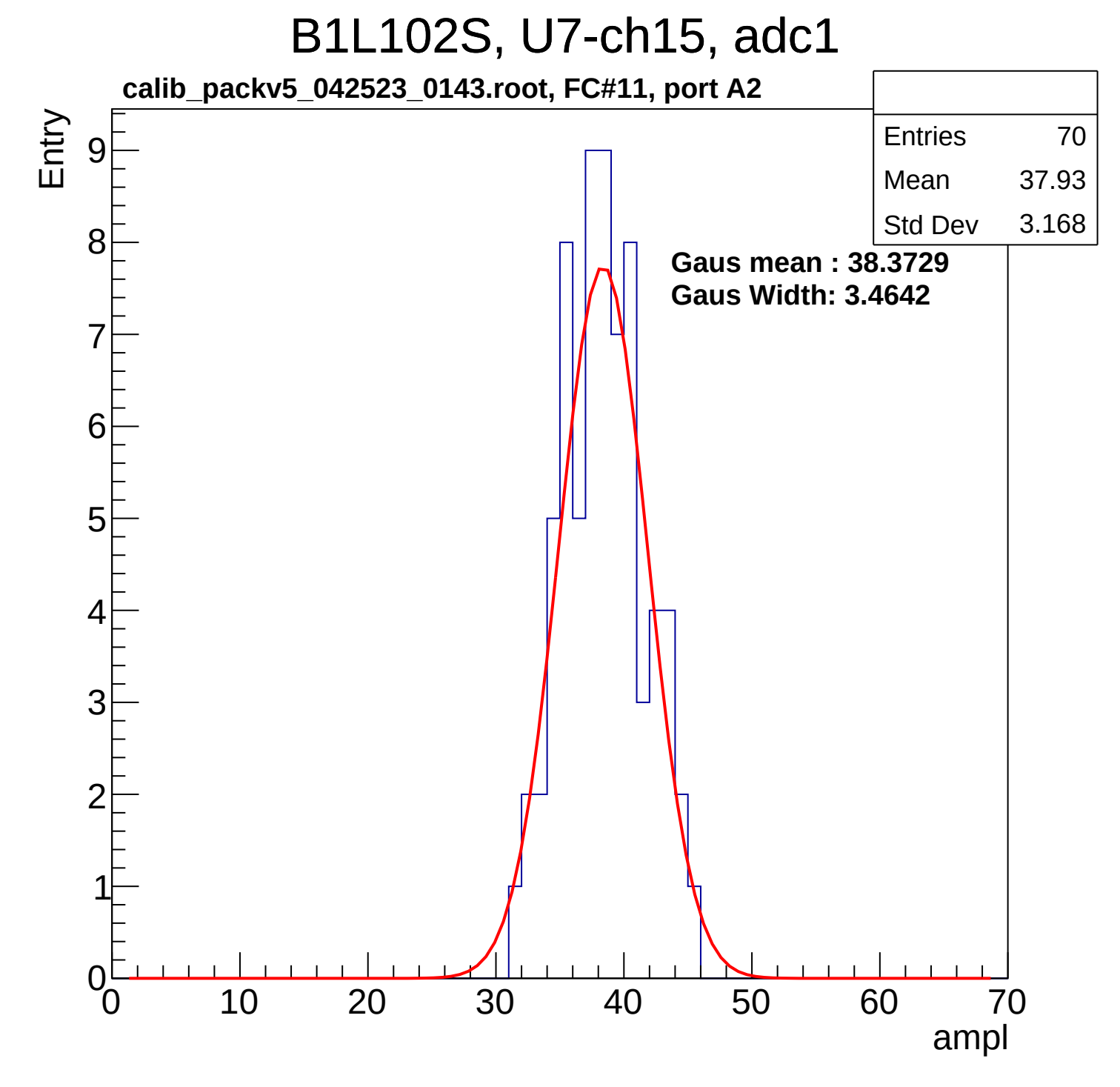
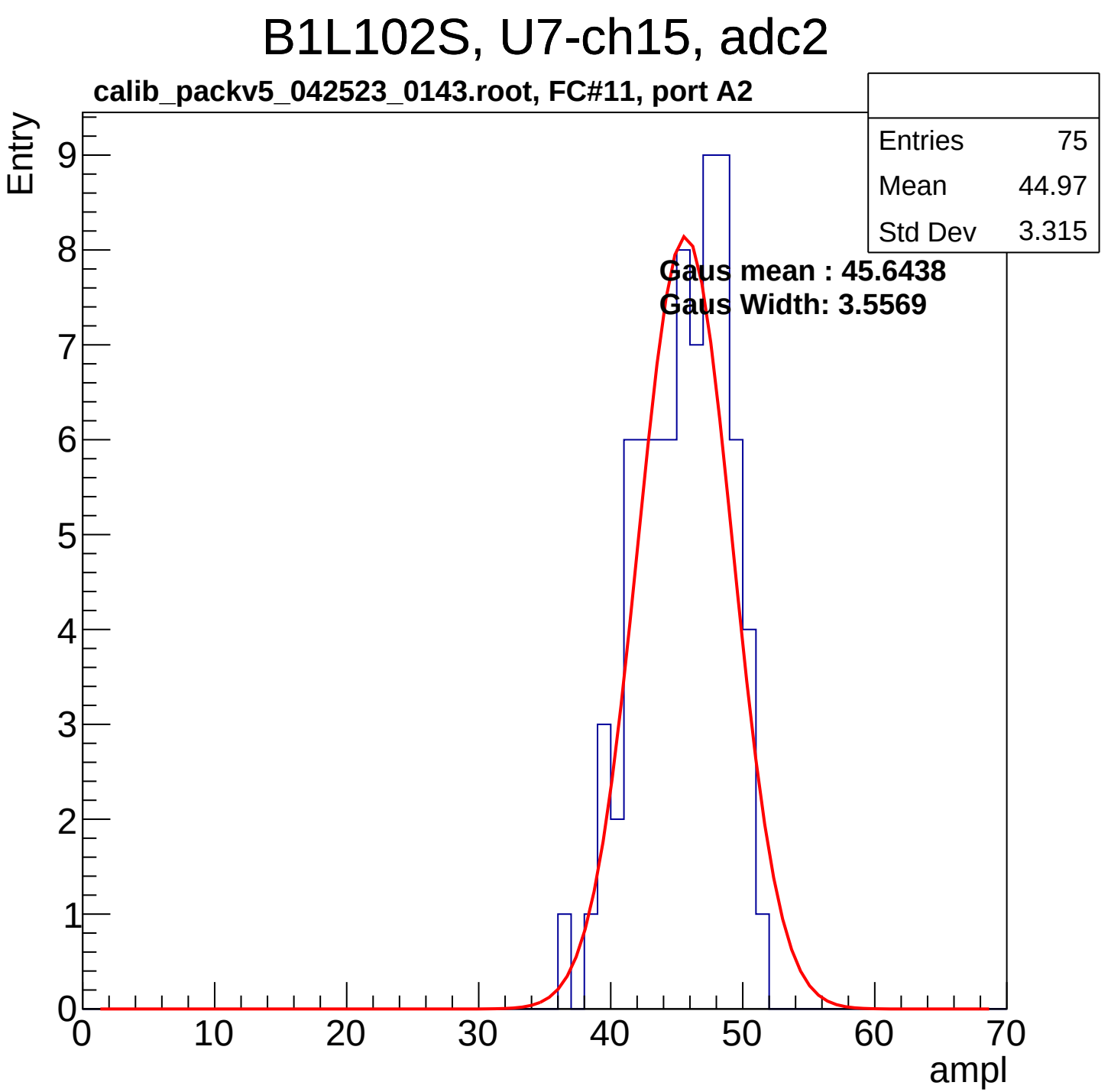

B1L102S, U7-ch15, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 70
Mean 37.93
Std Dev 3.168
Gaus mean : 38.3729
Gaus Width: 3.4642
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L102S, U7-ch15, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 75
Mean 44.97
Std Dev 3.315
Gaus mean : 45.6438
Gaus Width: 3.5569
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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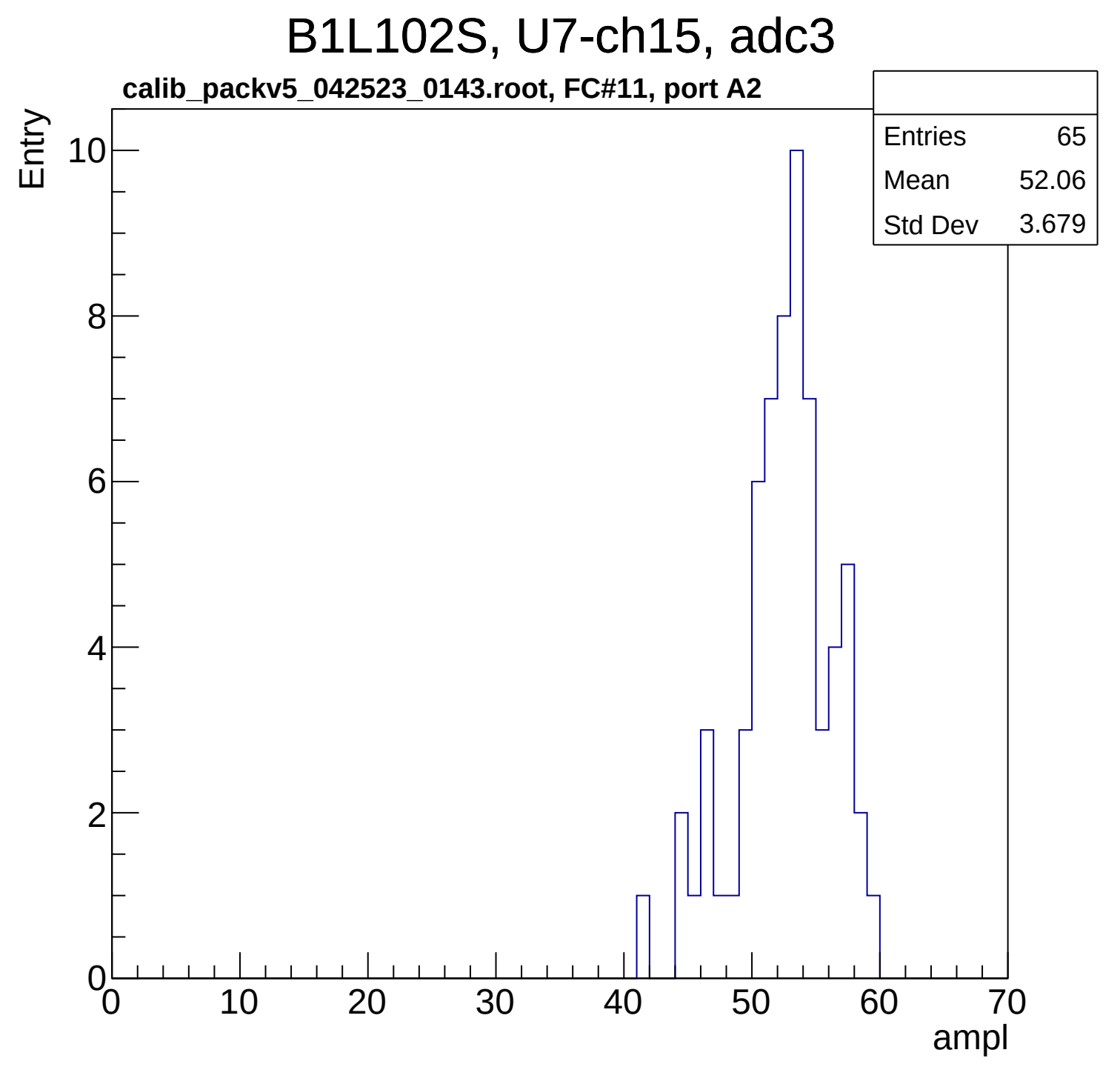
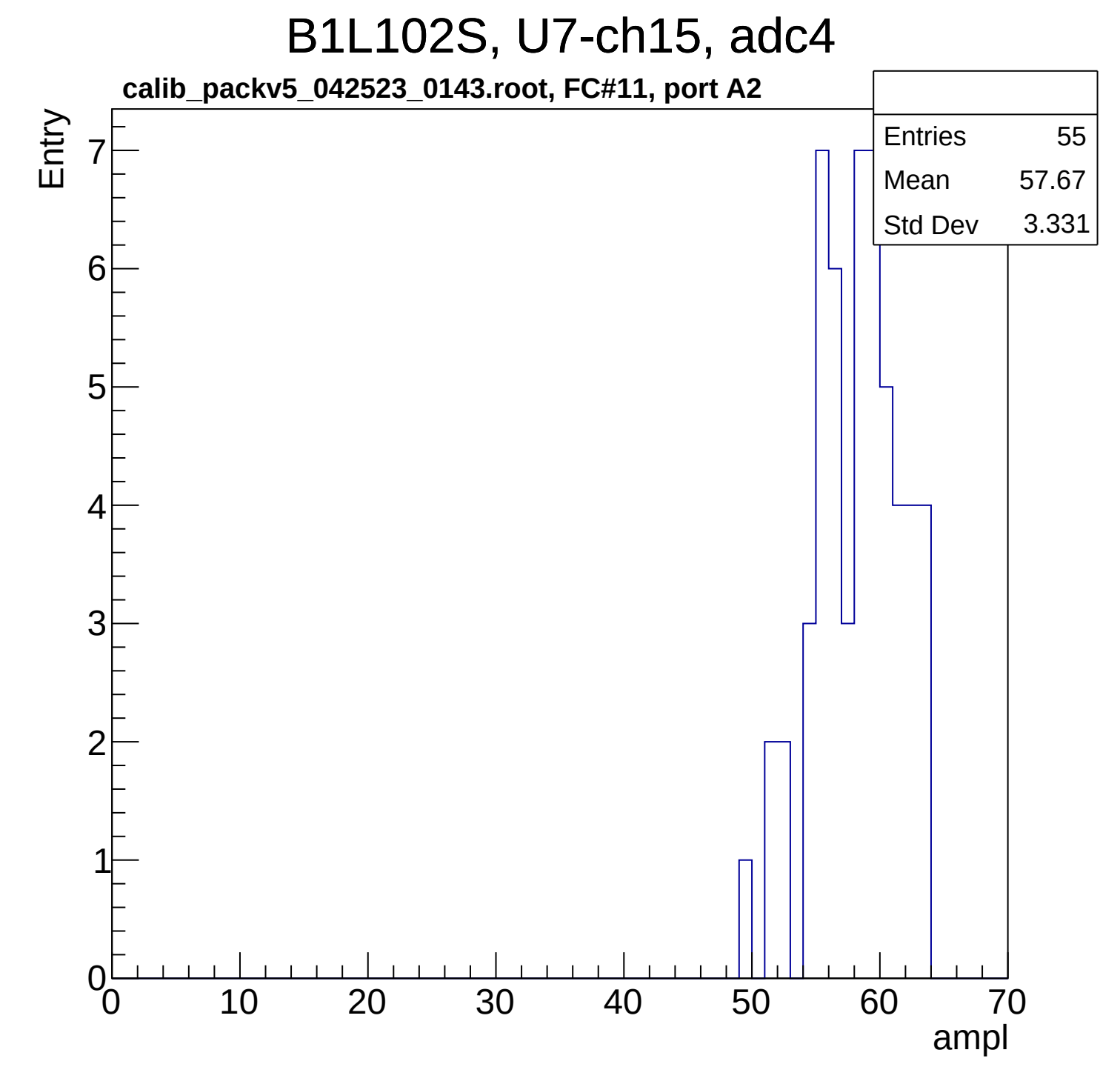
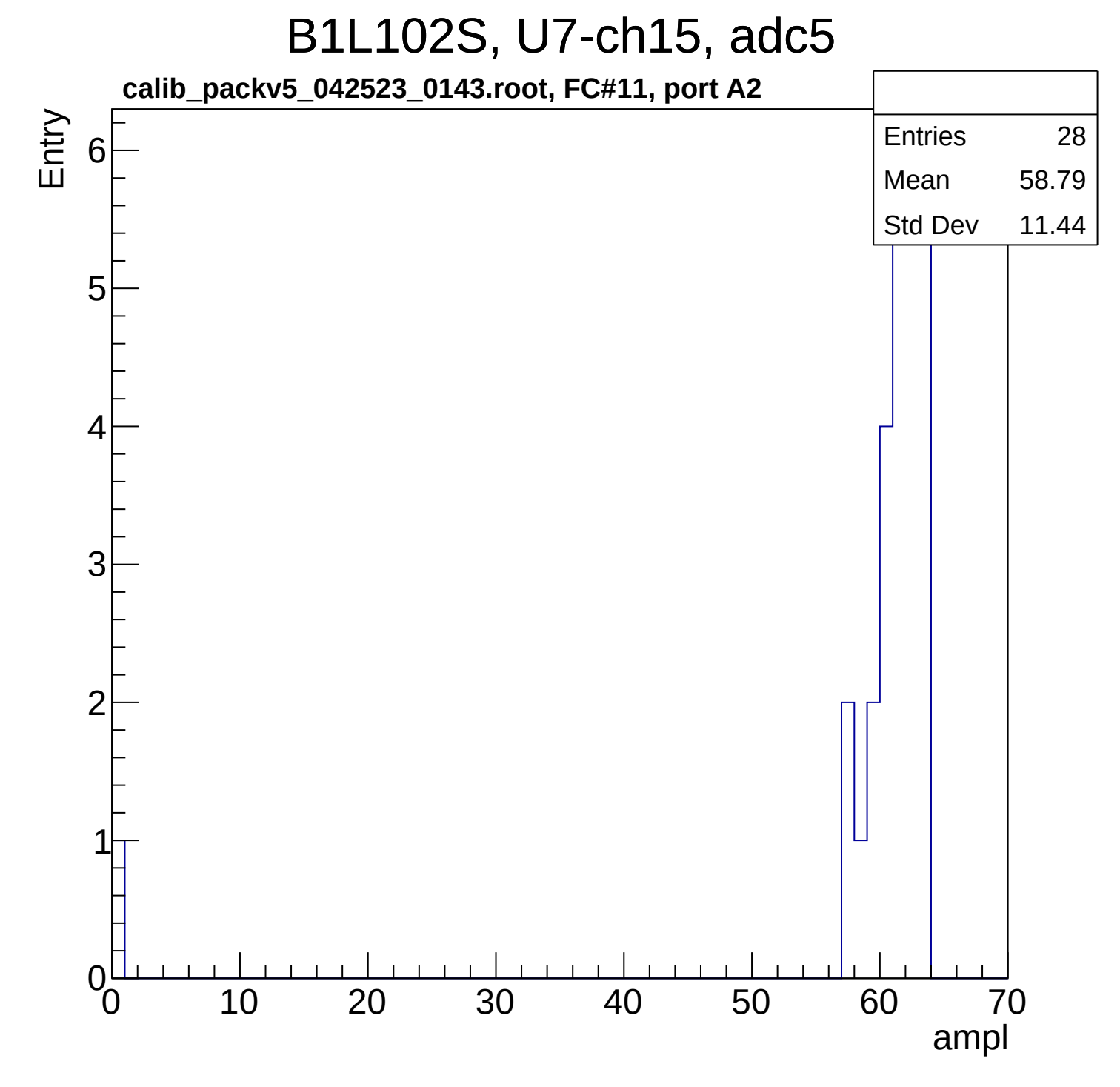

B1L102S, U7-ch15, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 65
Mean 52.06
Std Dev 3.679
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L102S, U7-ch15, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 55
Mean 57.67
Std Dev 3.331
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L102S, U7-ch15, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 28
Mean 58.79
Std Dev 11.44
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
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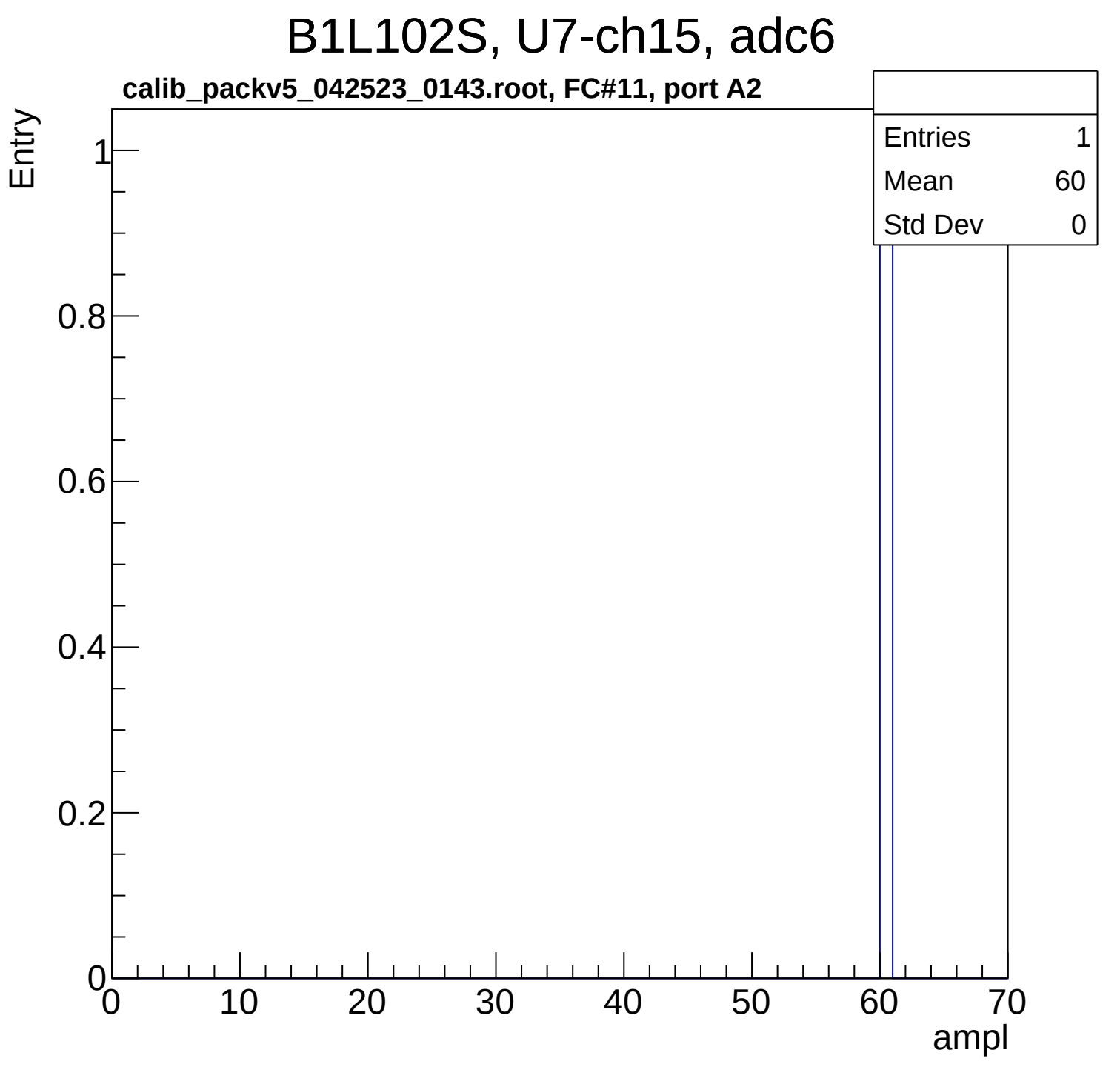
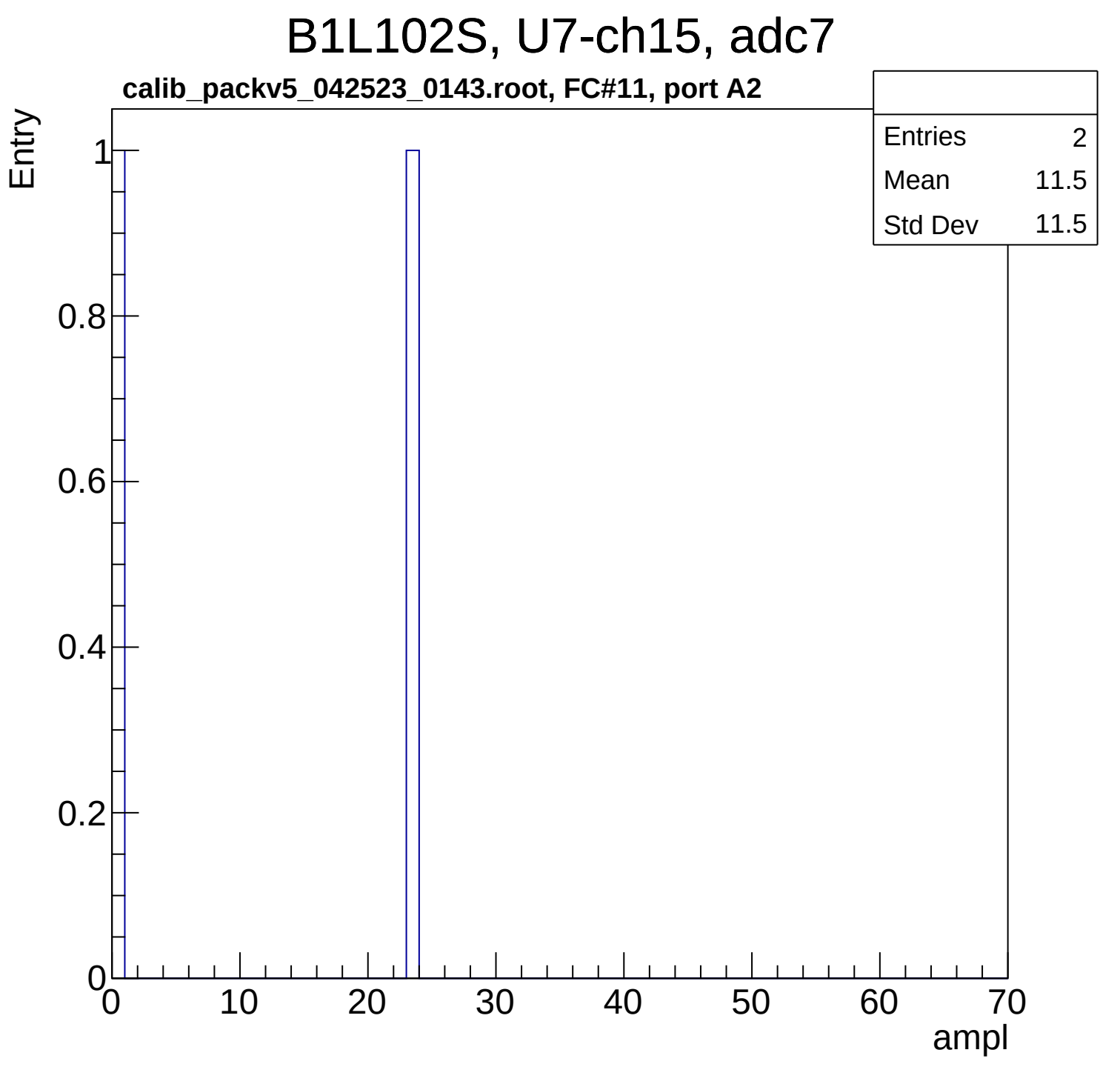
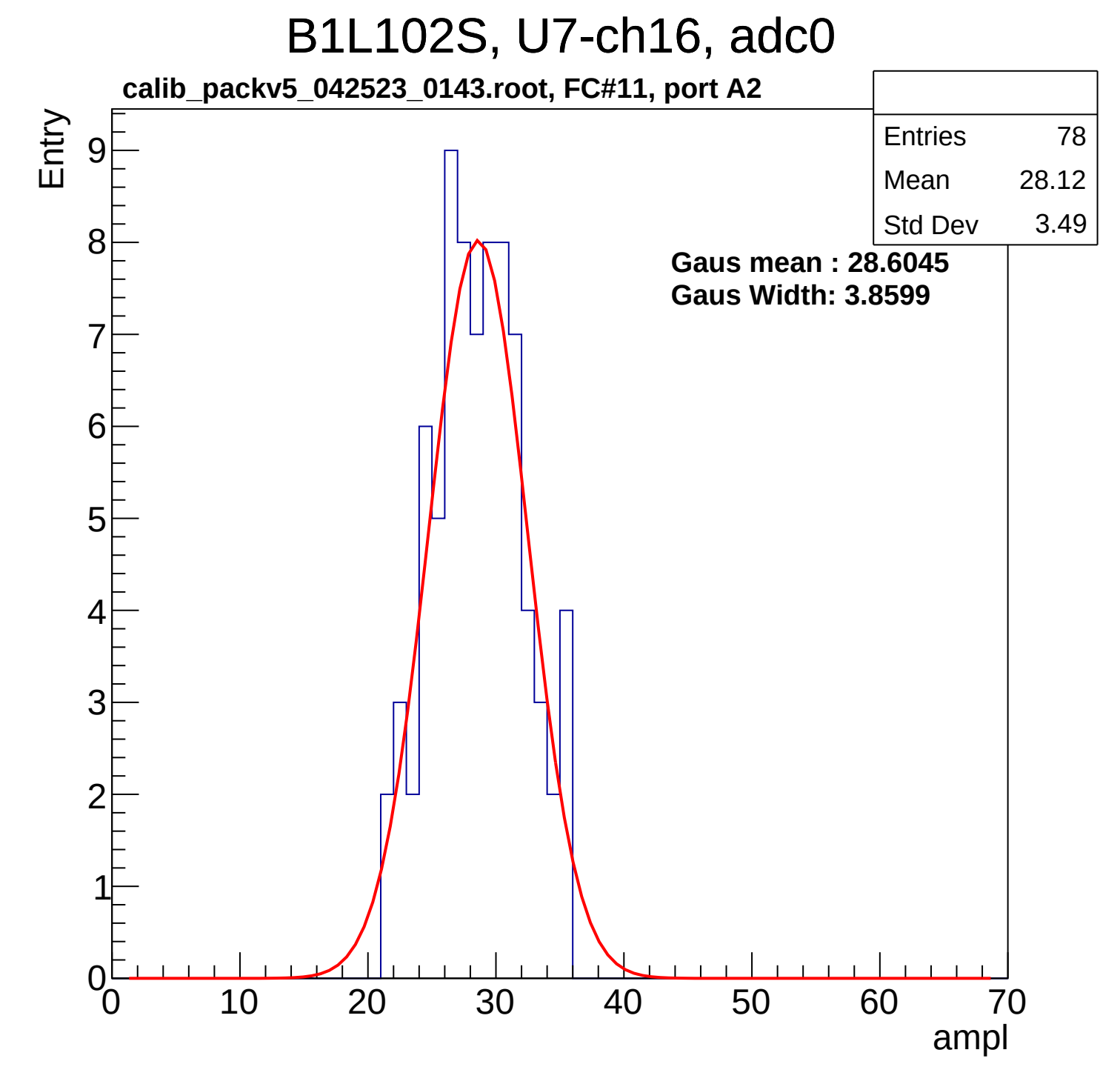
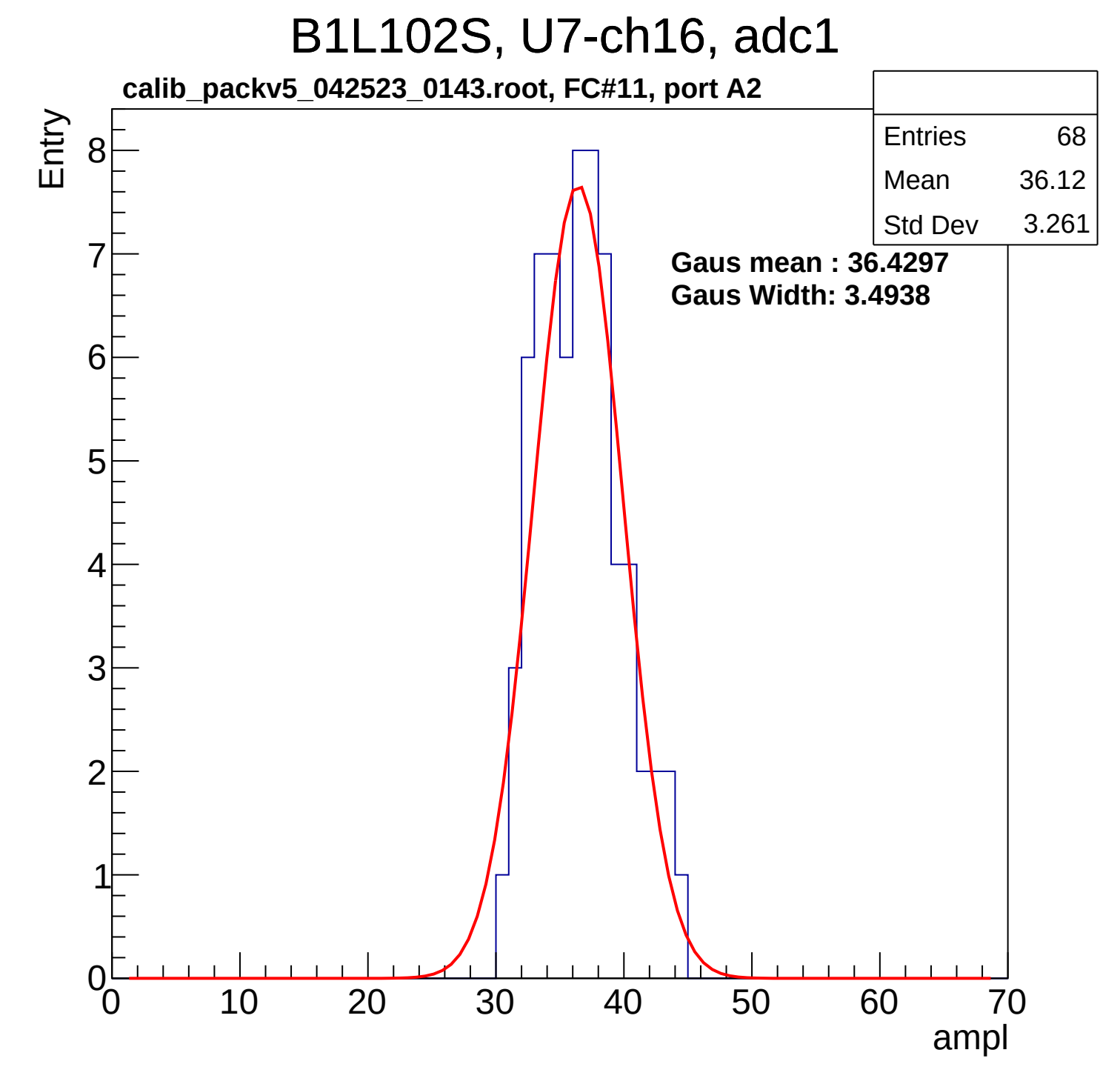

B1L102S, U7-ch15, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 1
Mean 60
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U7-ch15, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 2
Mean 11.5
Std Dev 11.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U7-ch16, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 78
Mean 28.12
Std Dev 3.49
Gaus mean : 28.6045
Gaus Width: 3.8599
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L102S, U7-ch16, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 68
Mean 36.12
Std Dev 3.261
Gaus mean : 36.4297
Gaus Width: 3.4938
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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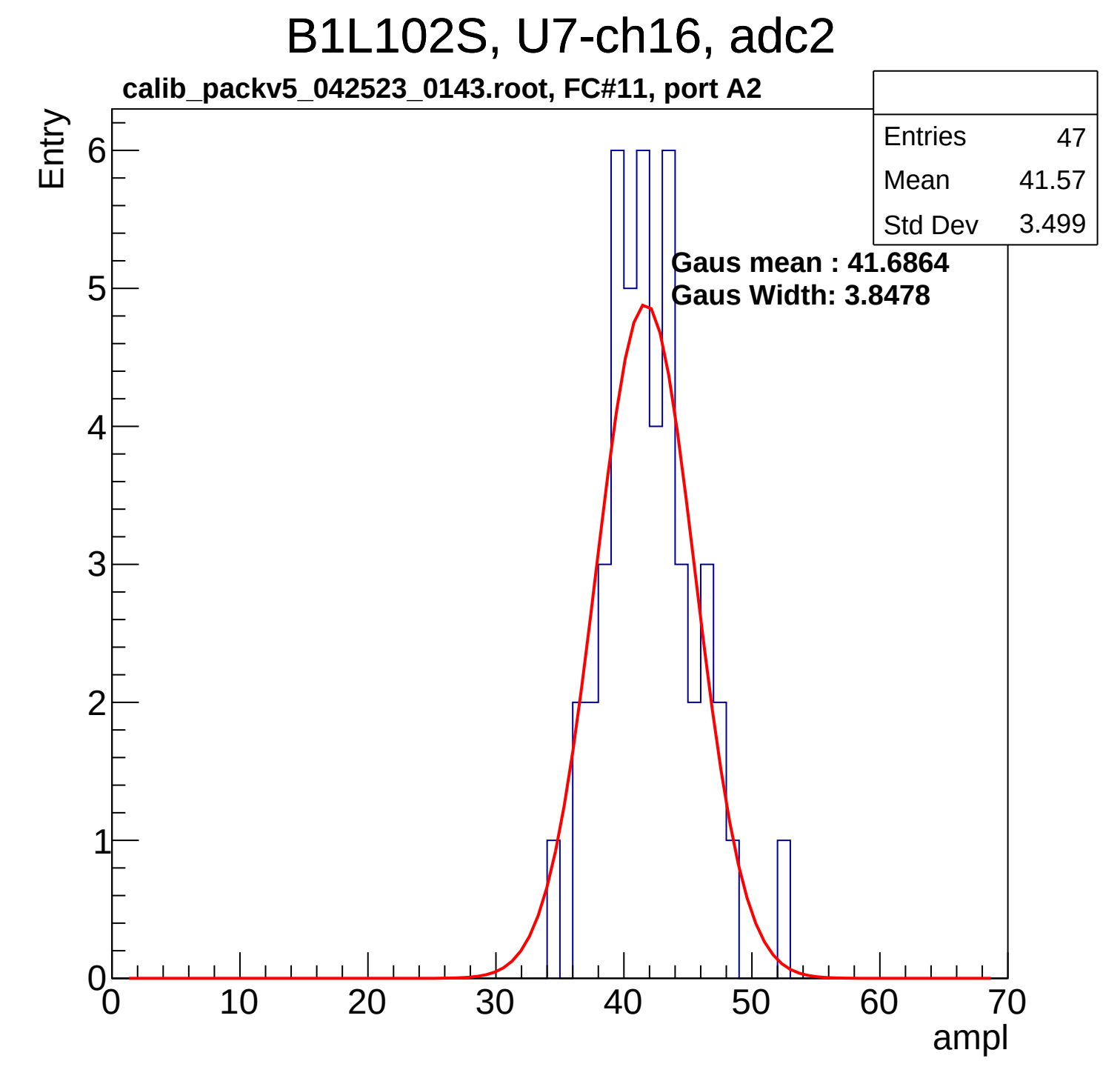
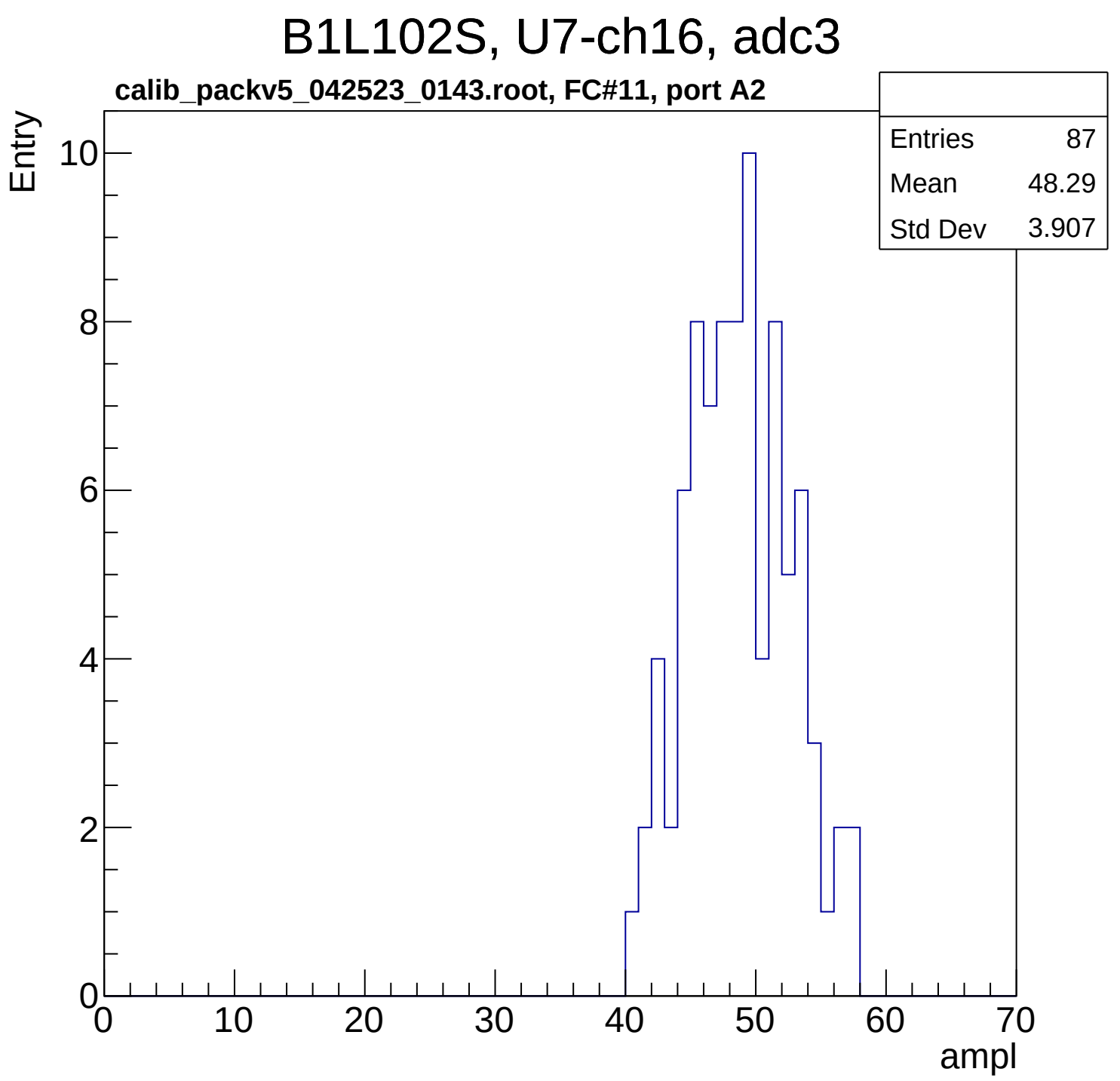
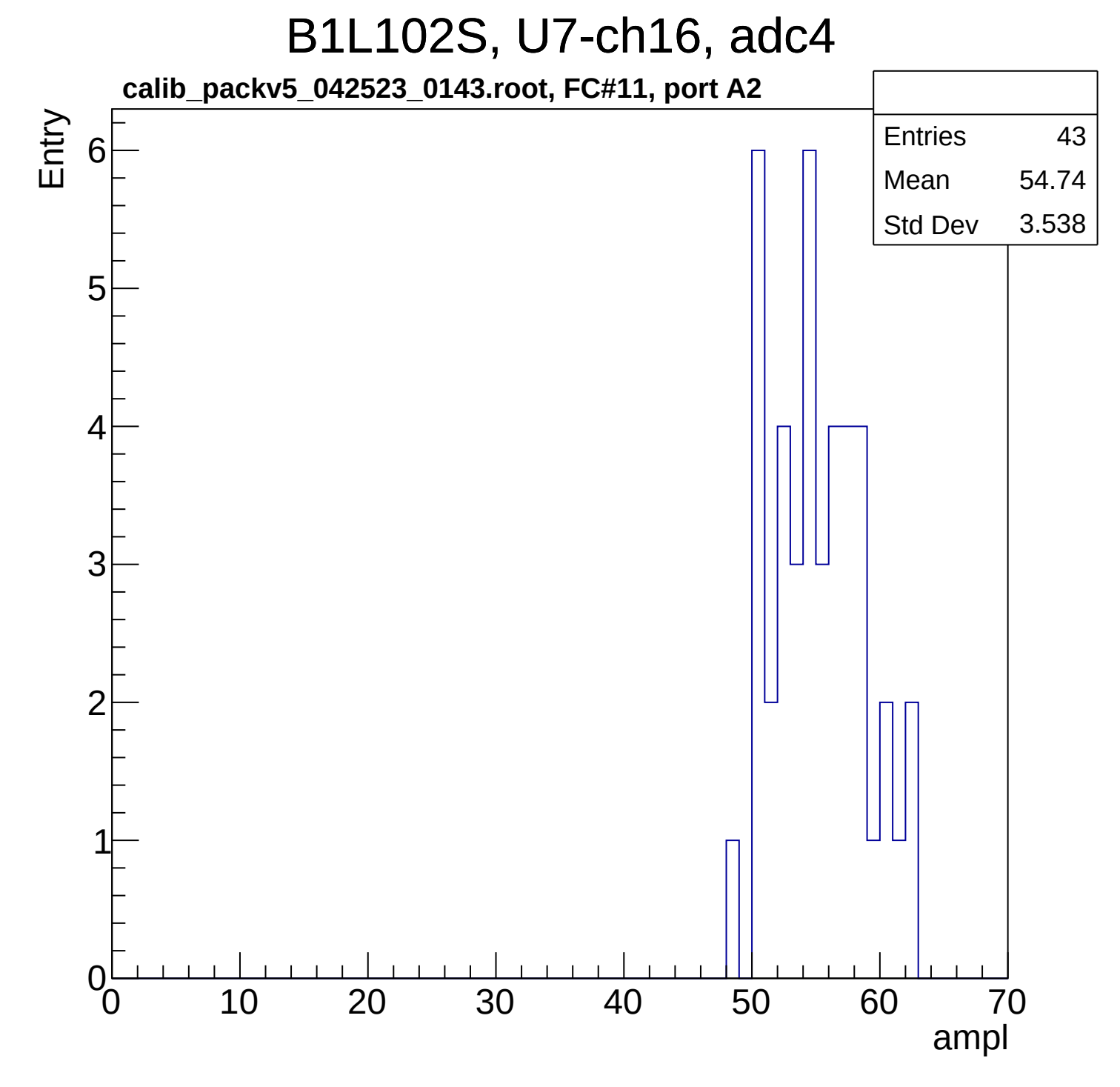
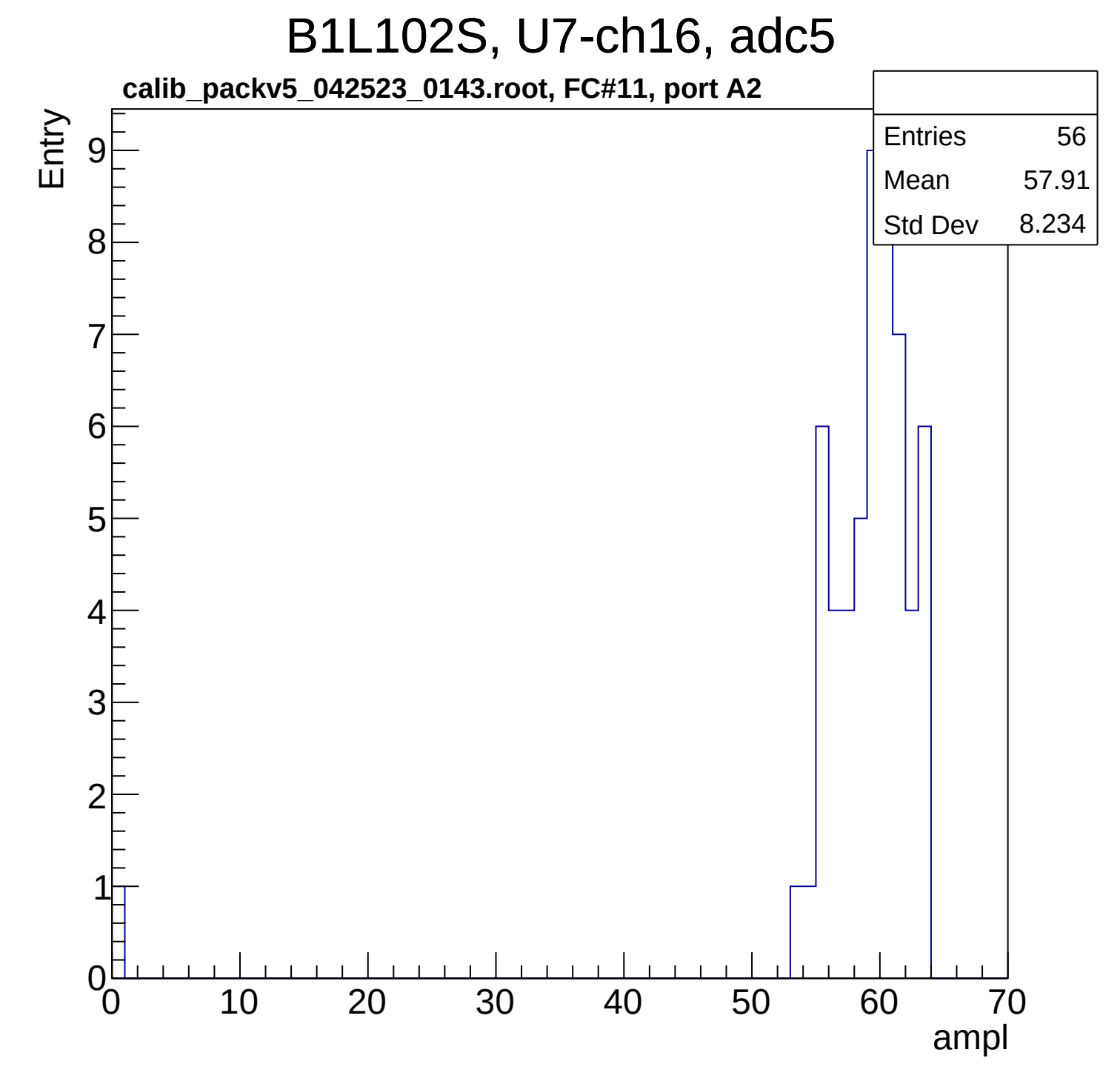

B1L102S, U7-ch16, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 47
Mean 41.57
Std Dev 3.499
Gaus mean : 41.6864
Gaus Width: 3.8478
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L102S, U7-ch16, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 87
Mean 48.29
Std Dev 3.907
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L102S, U7-ch16, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 43
Mean 54.74
Std Dev 3.538
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L102S, U7-ch16, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 56
Mean 57.91
Std Dev 8.234
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
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20
30
40
50
60
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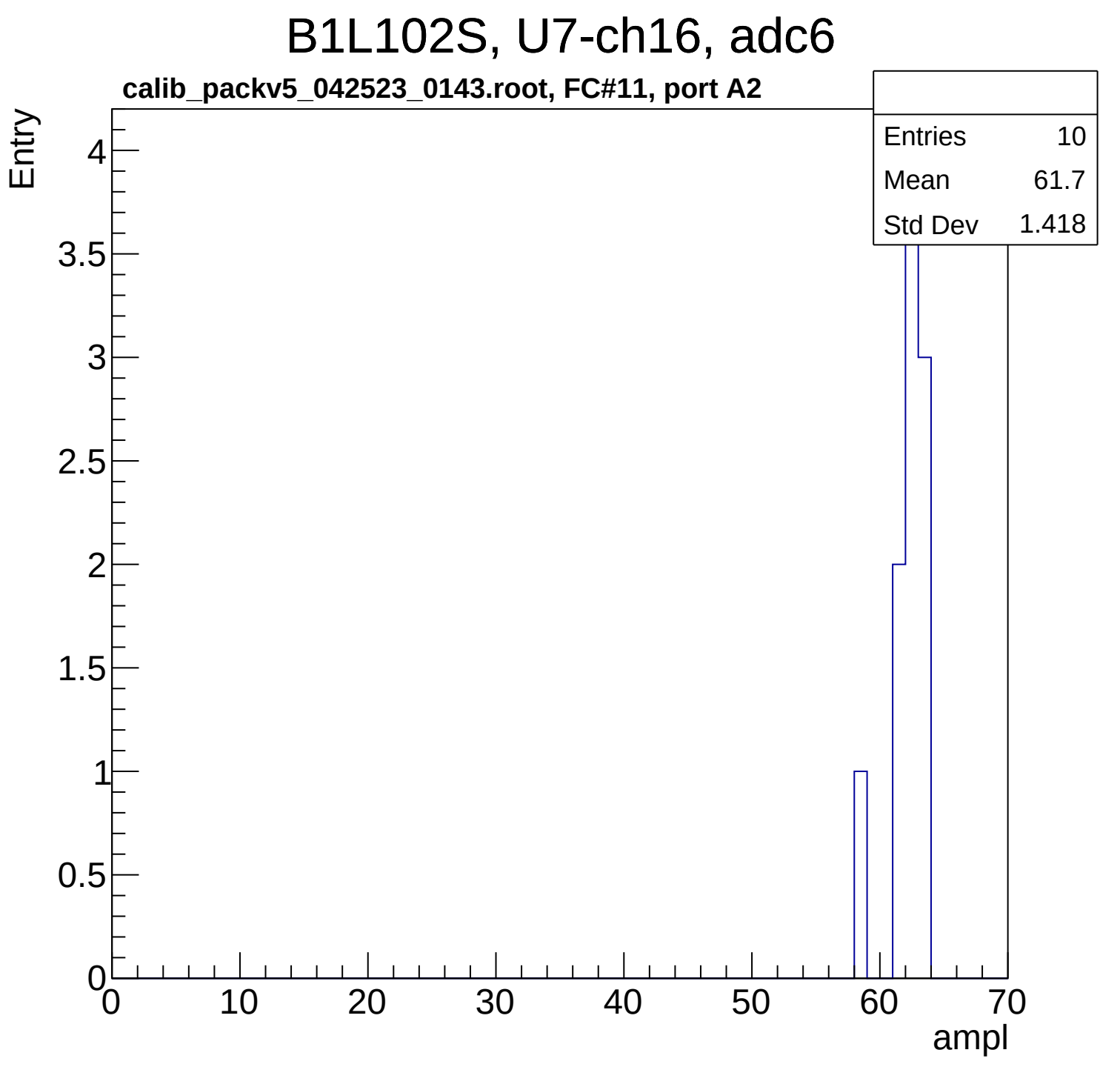
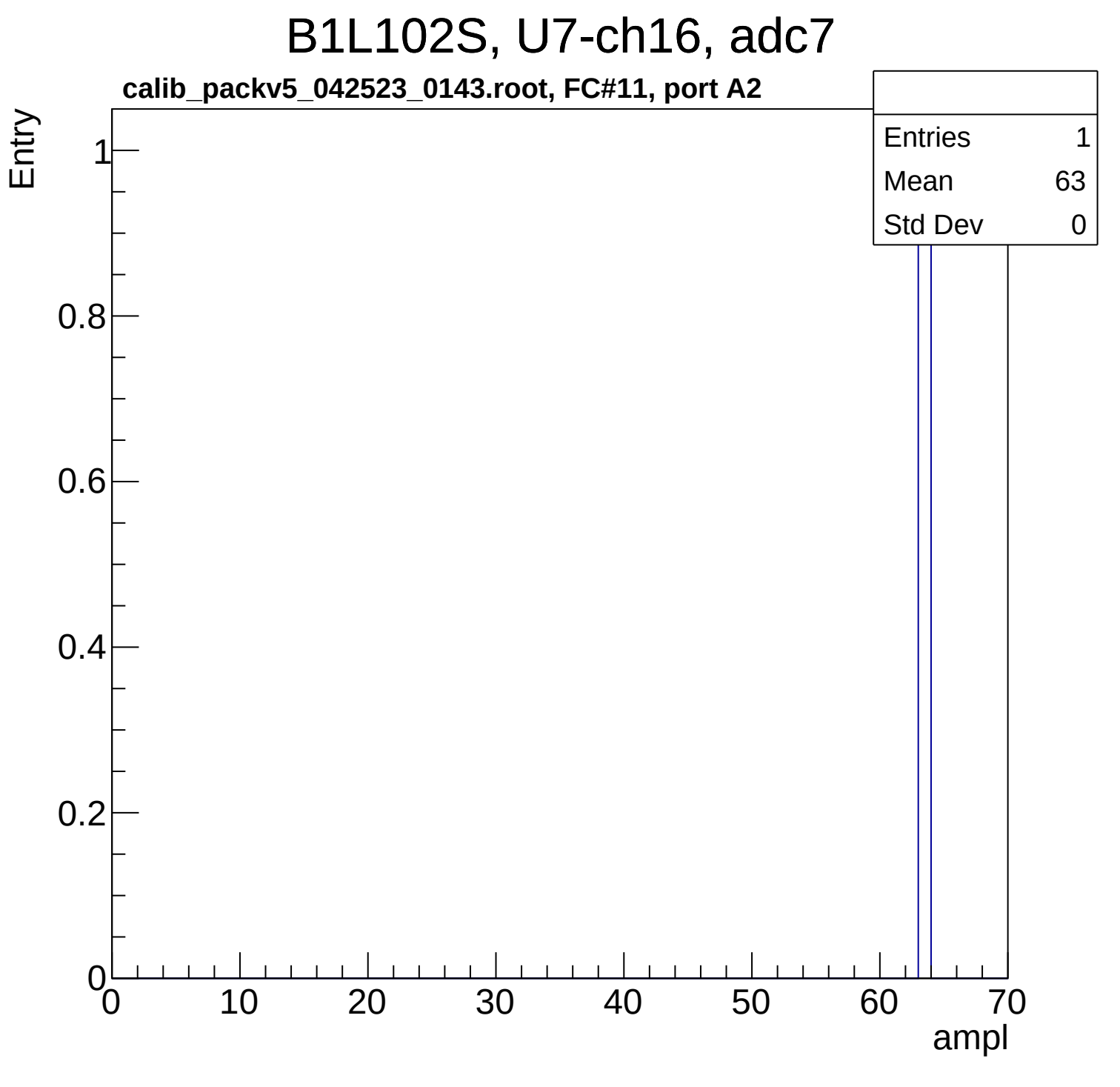
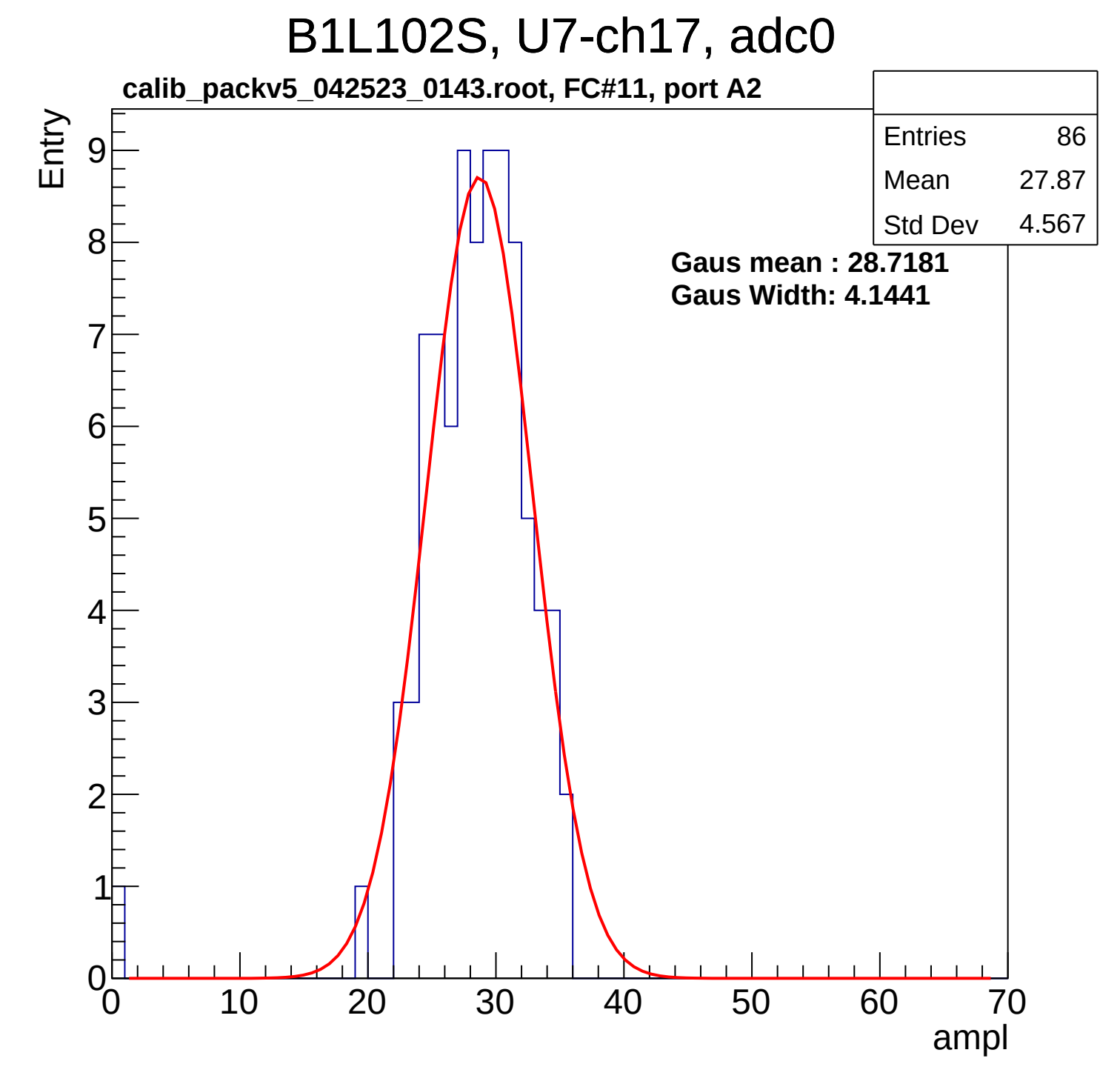
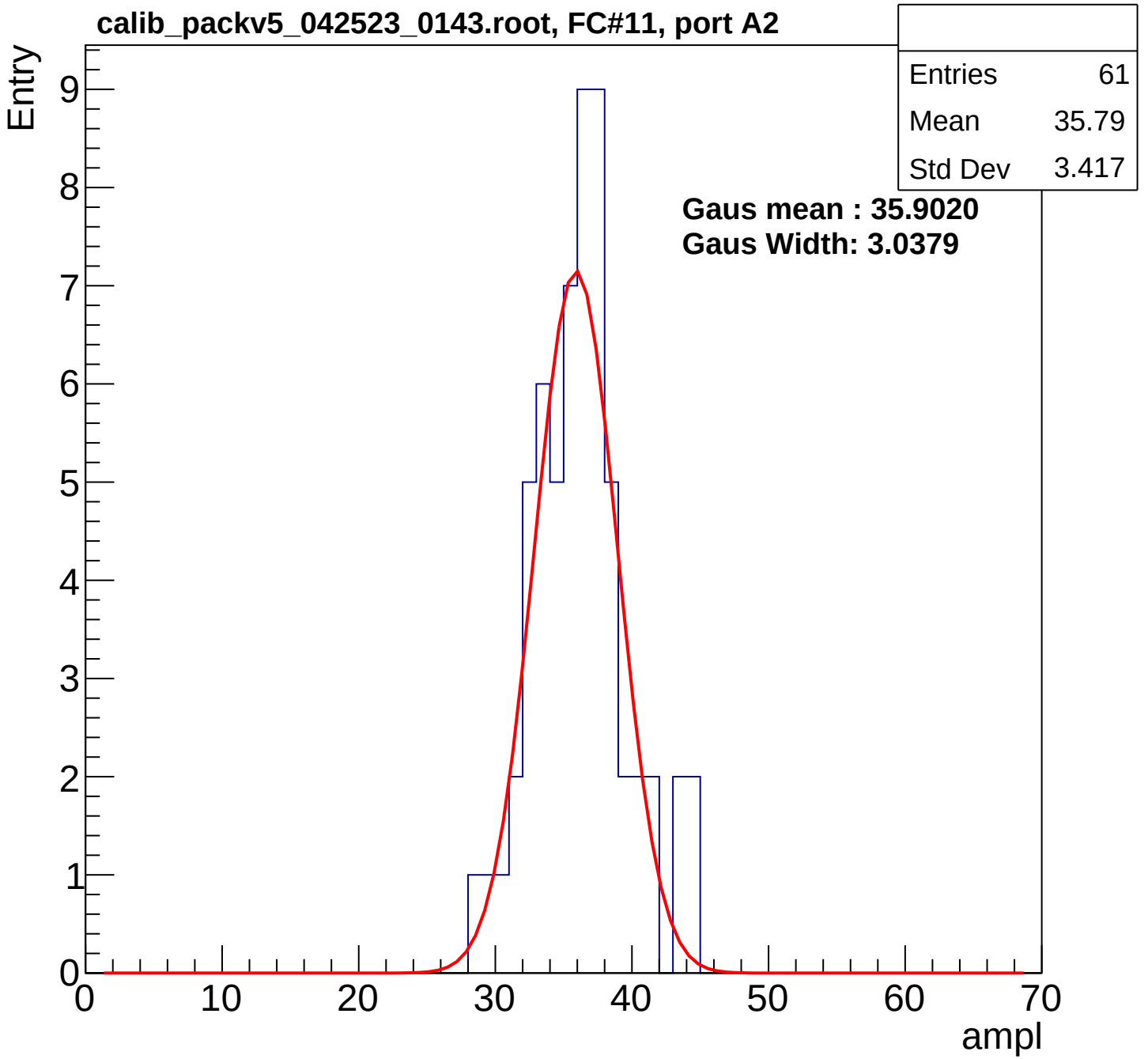
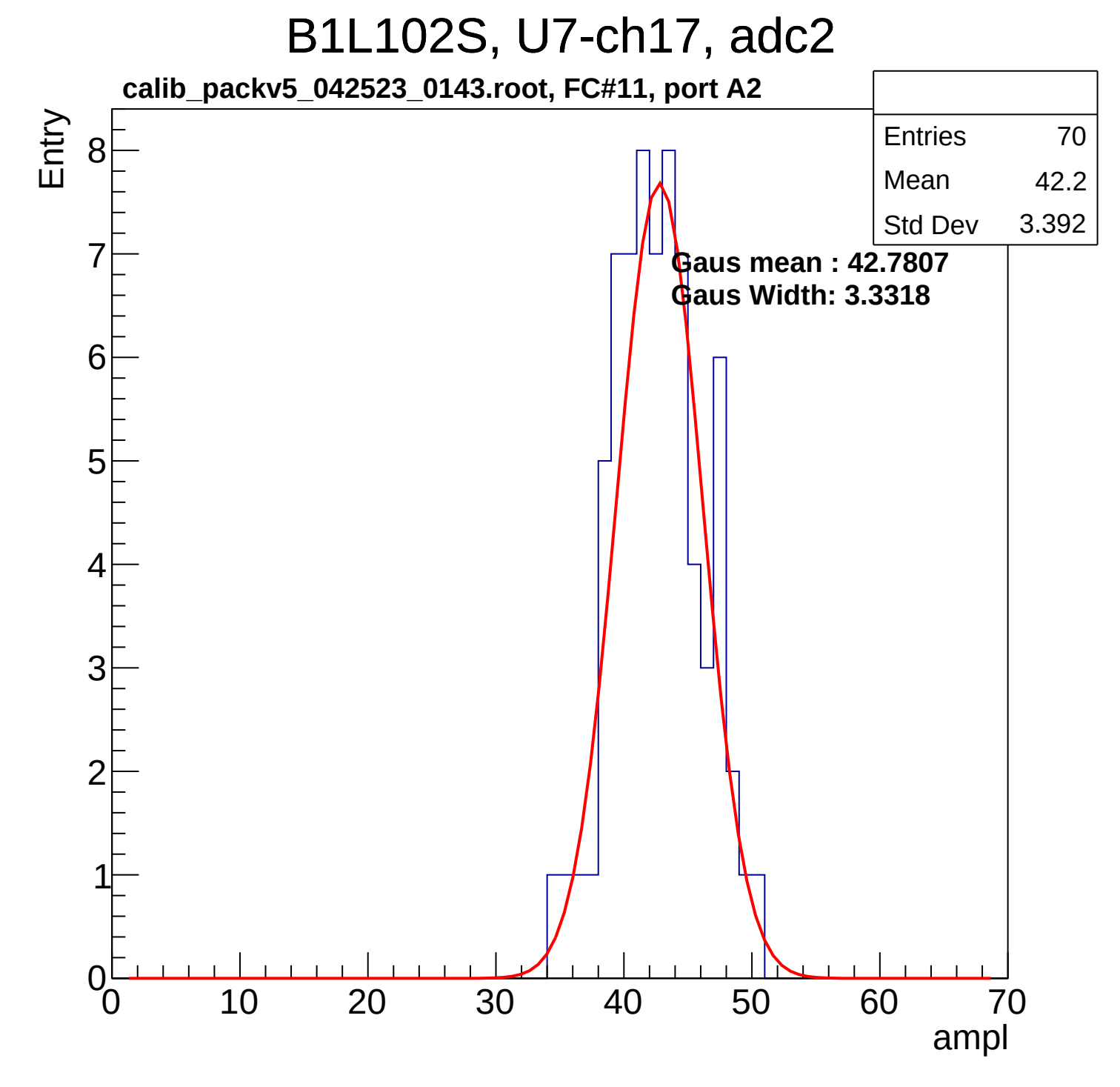
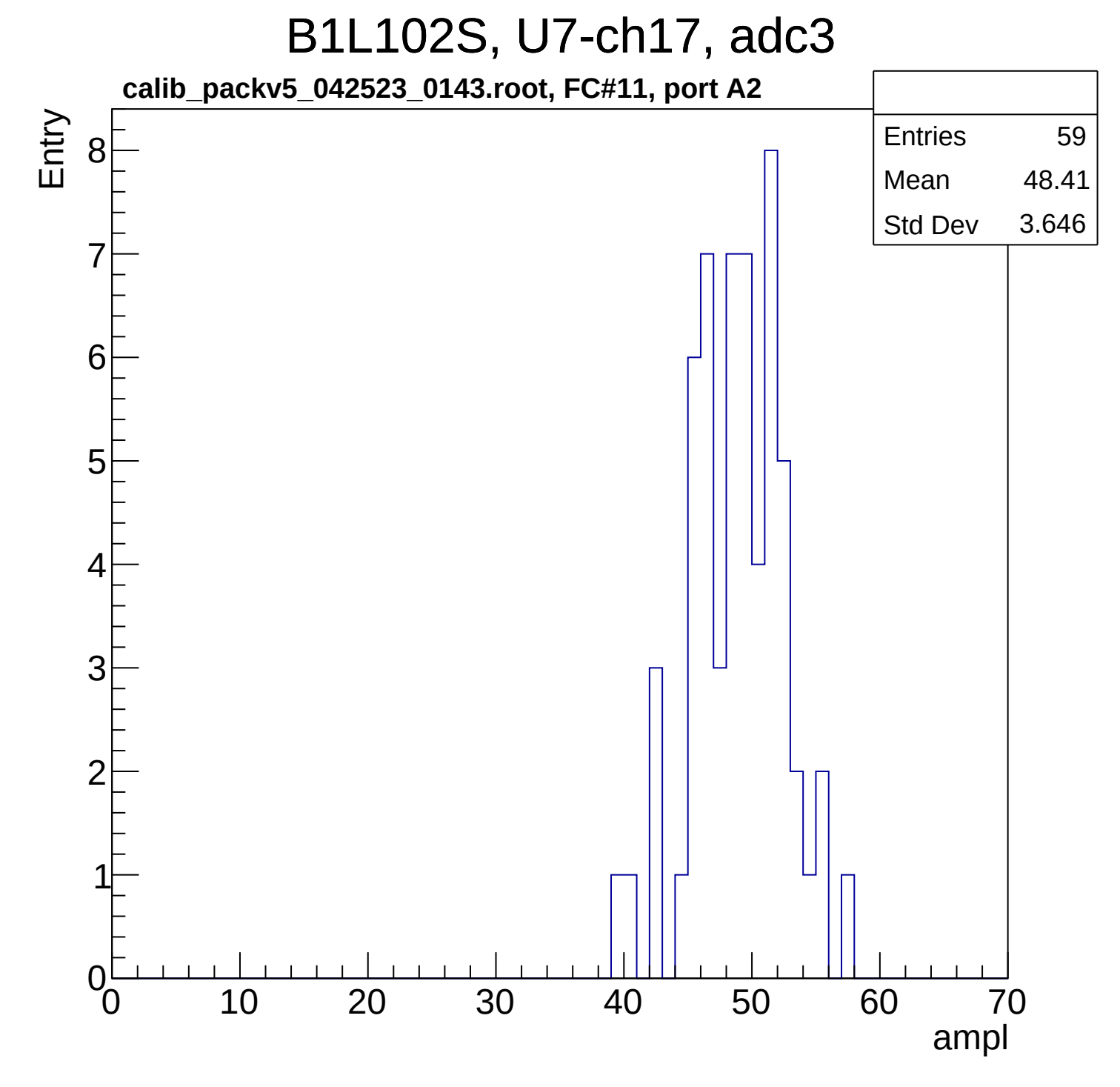

B1L102S, U7-ch16, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 10
Mean 61.7
Std Dev 1.418
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

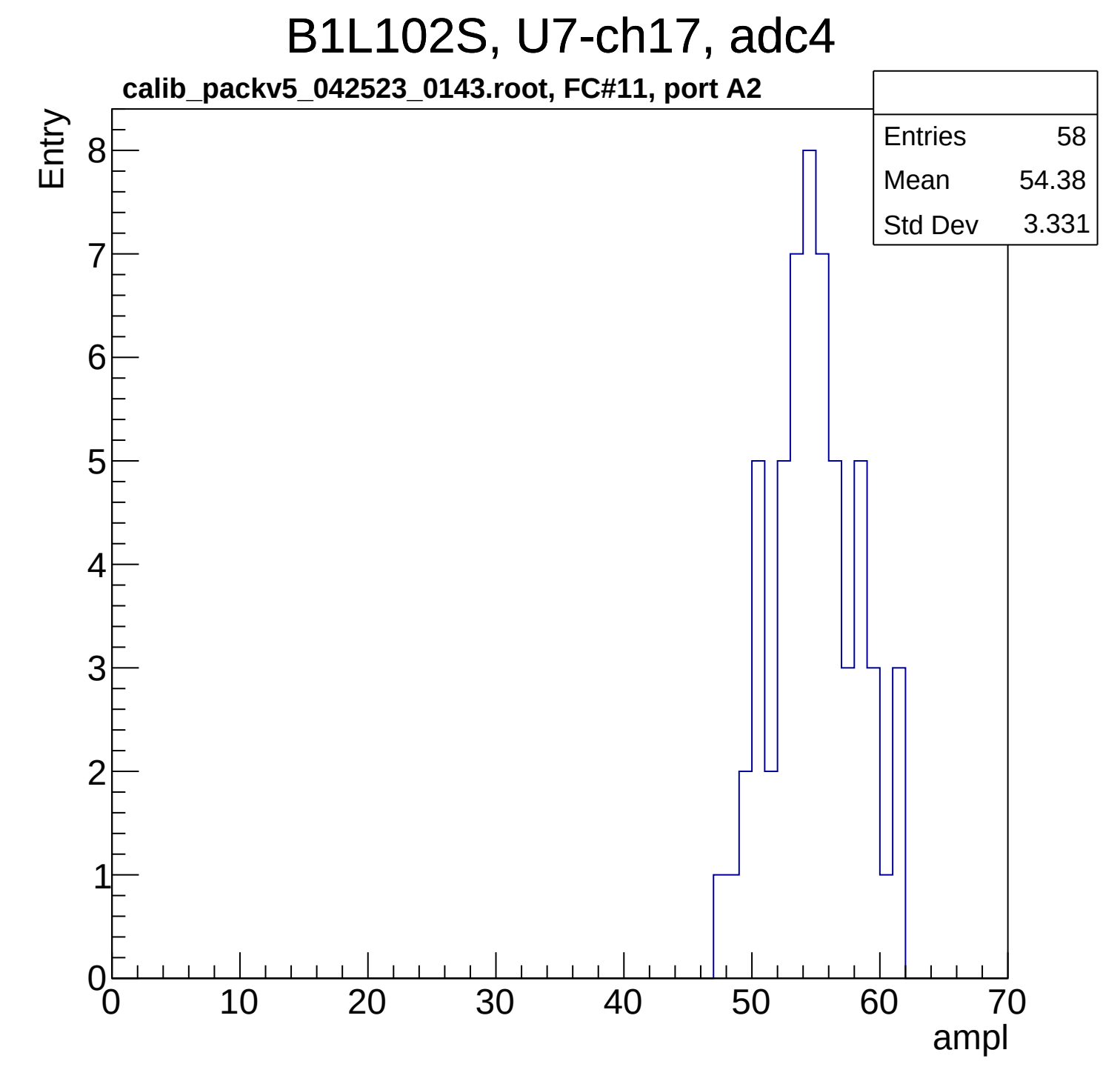

B1L102S, U7-ch16, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 1
Mean 63
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

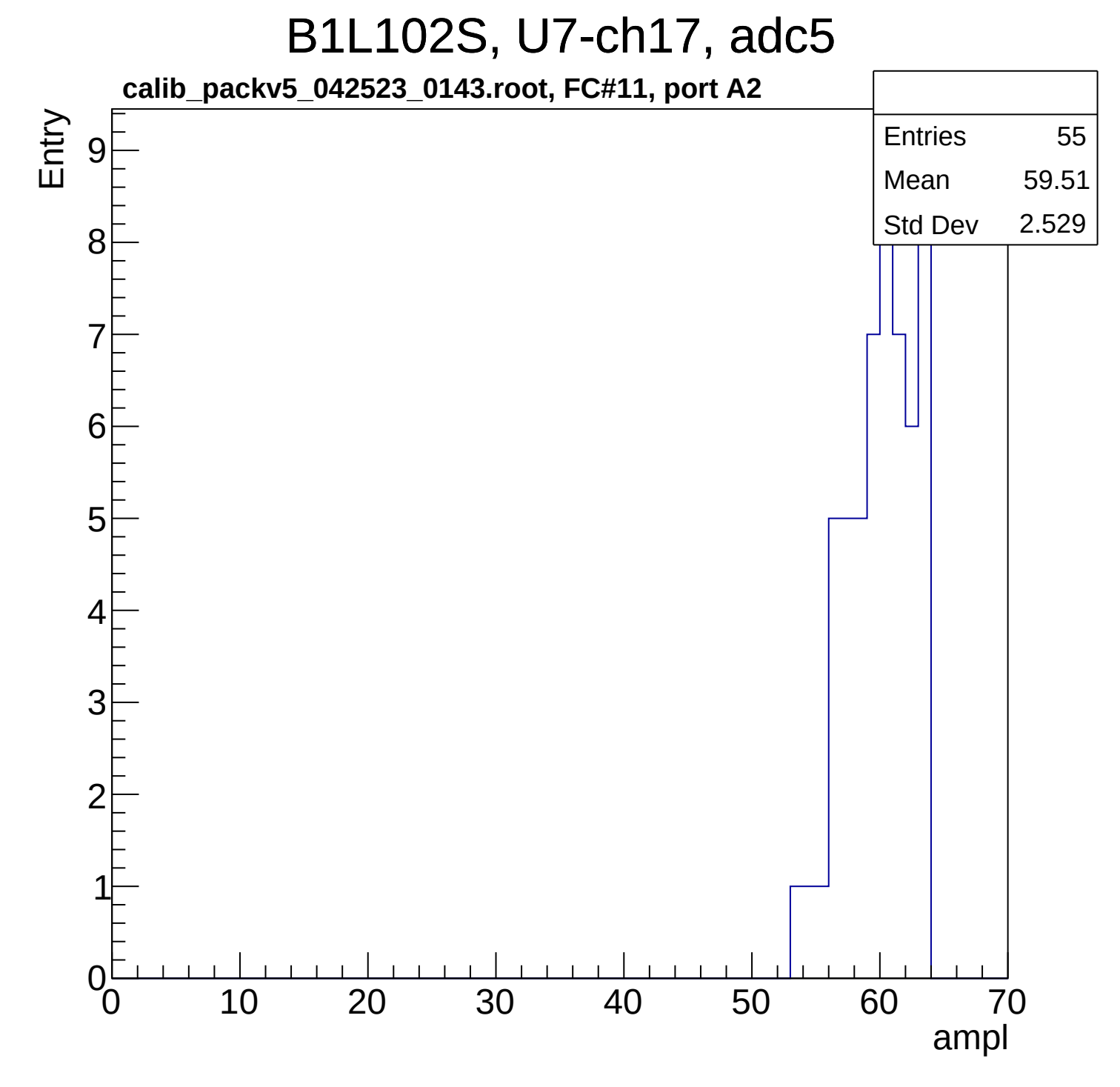

B1L102S, U7-ch17, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 86
Mean 27.87
Std Dev 4.567
Gaus mean : 28.7181
Gaus Width: 4.1441
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L102S, U7-ch17, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 61
Mean 35.79
Std Dev 3.417
Gaus mean : 35.9020
Gaus Width: 3.0379
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L102S, U7-ch17, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 70
Mean 42.2
Std Dev 3.392
Gaus mean : 42.7807
Gaus Width: 3.3318
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L102S, U7-ch17, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 59
Mean 48.41
Std Dev 3.646
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L102S, U7-ch17, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 58
Mean 54.38
Std Dev 3.331
Entry
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L102S, U7-ch17, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 55
Mean 59.51
Std Dev 2.529
Entry
ampl
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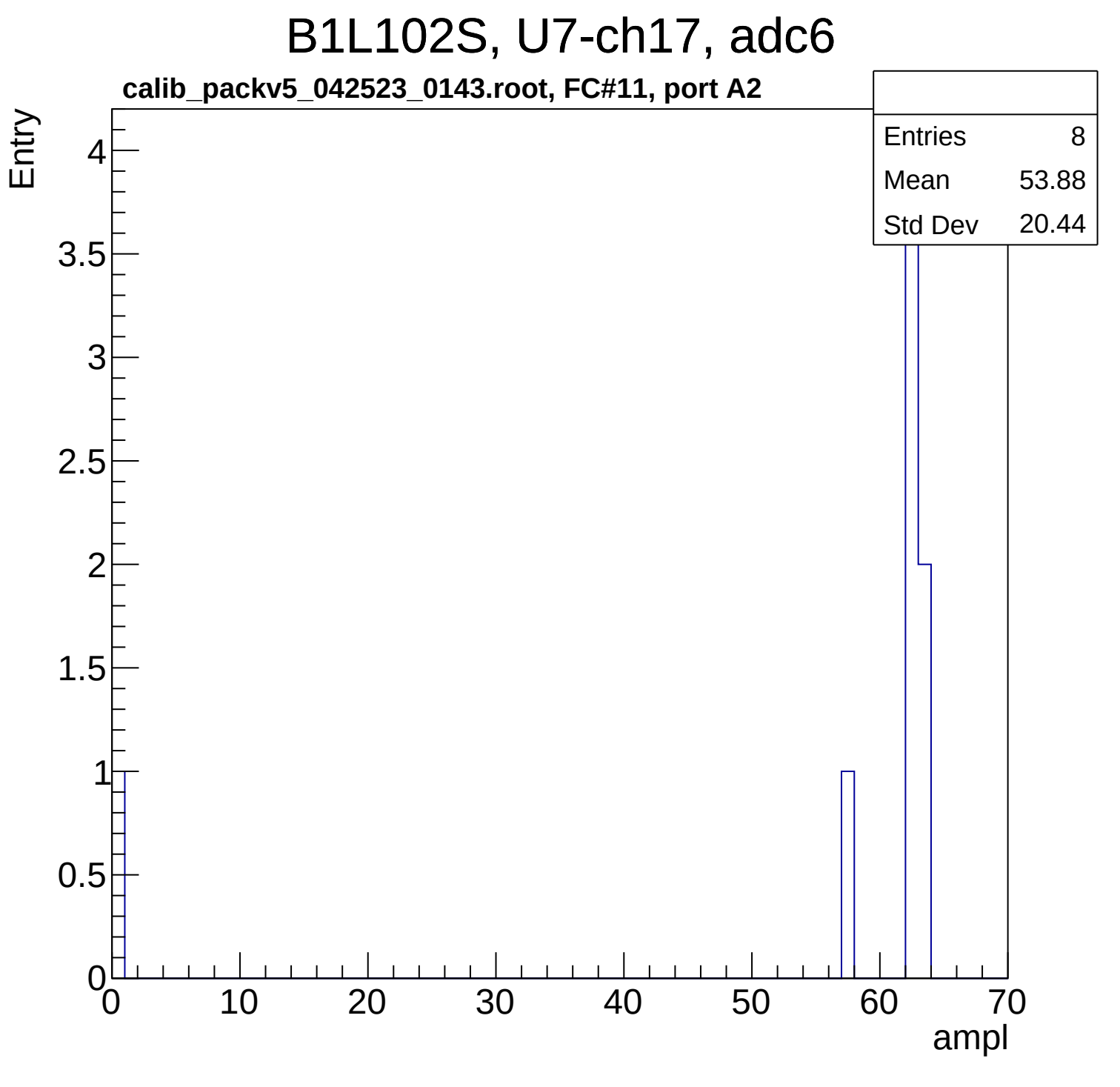
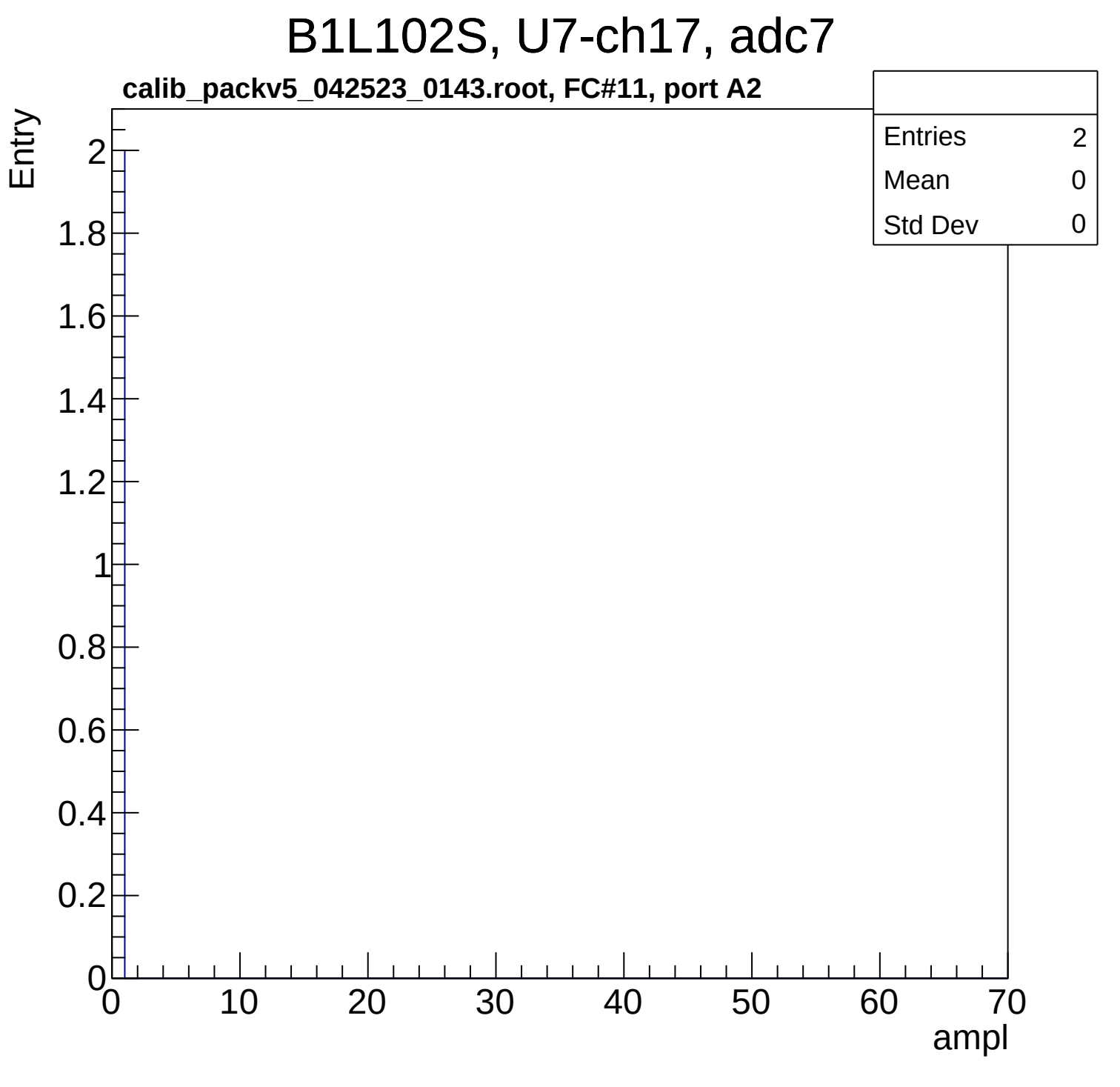
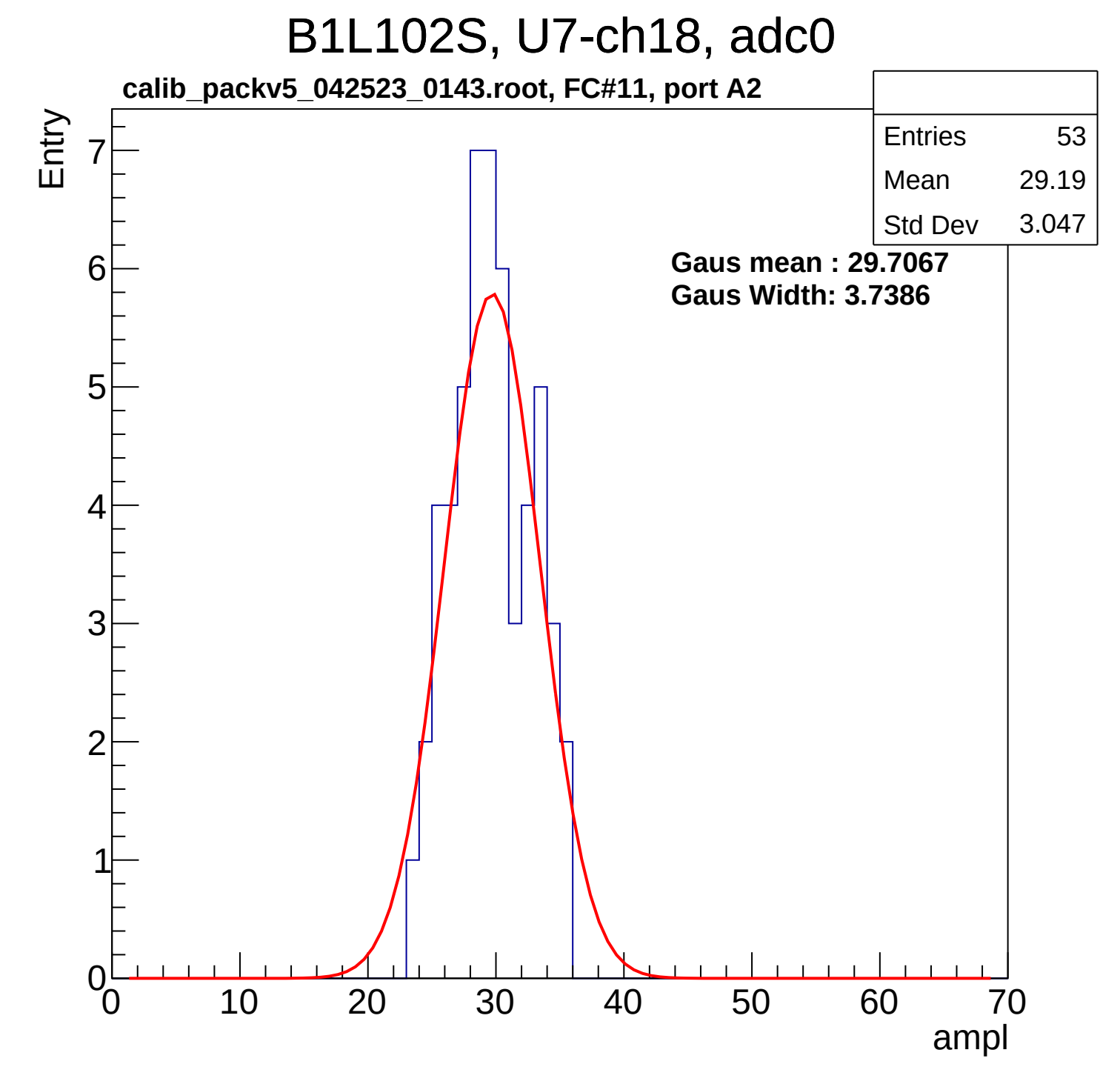
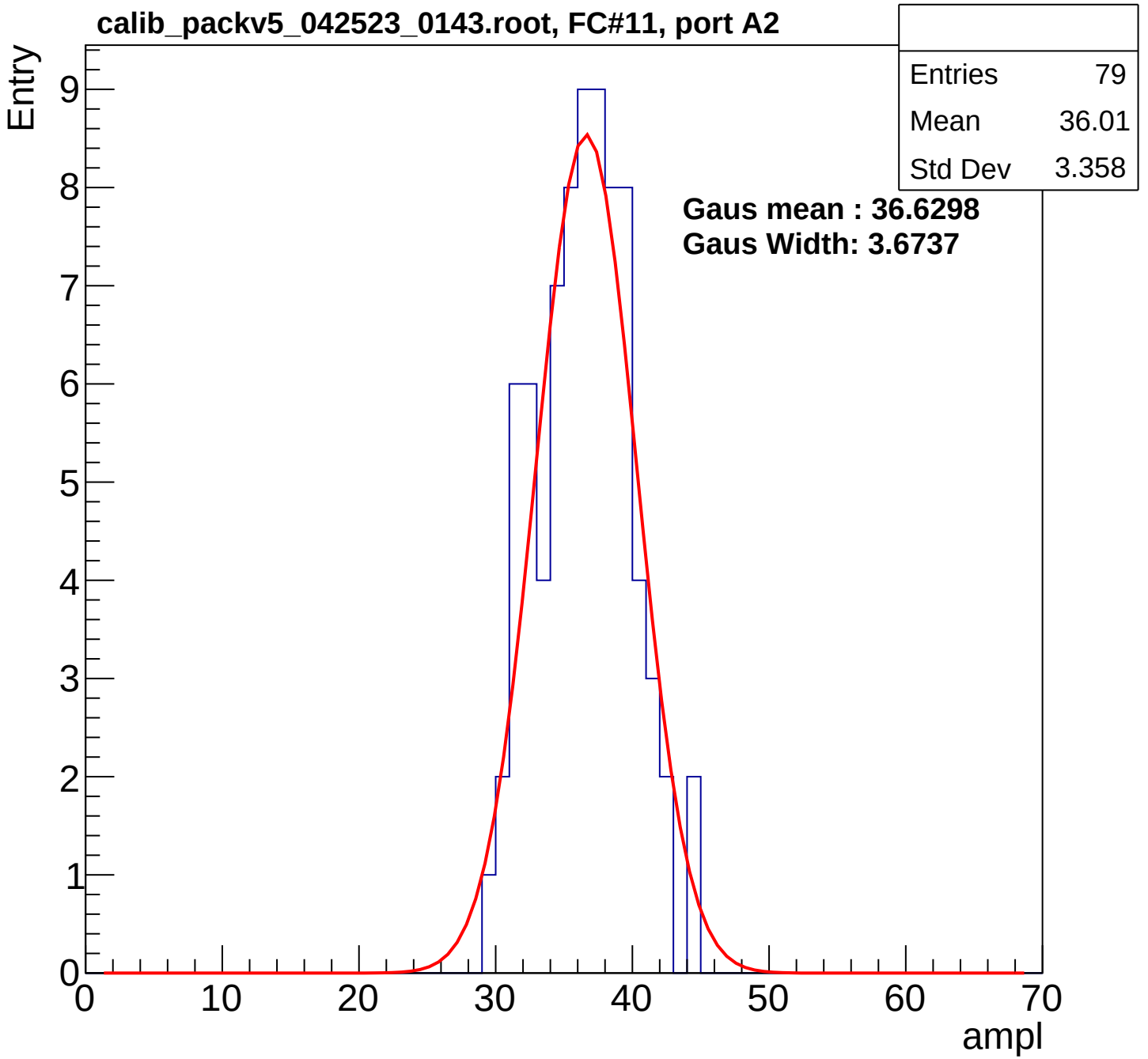
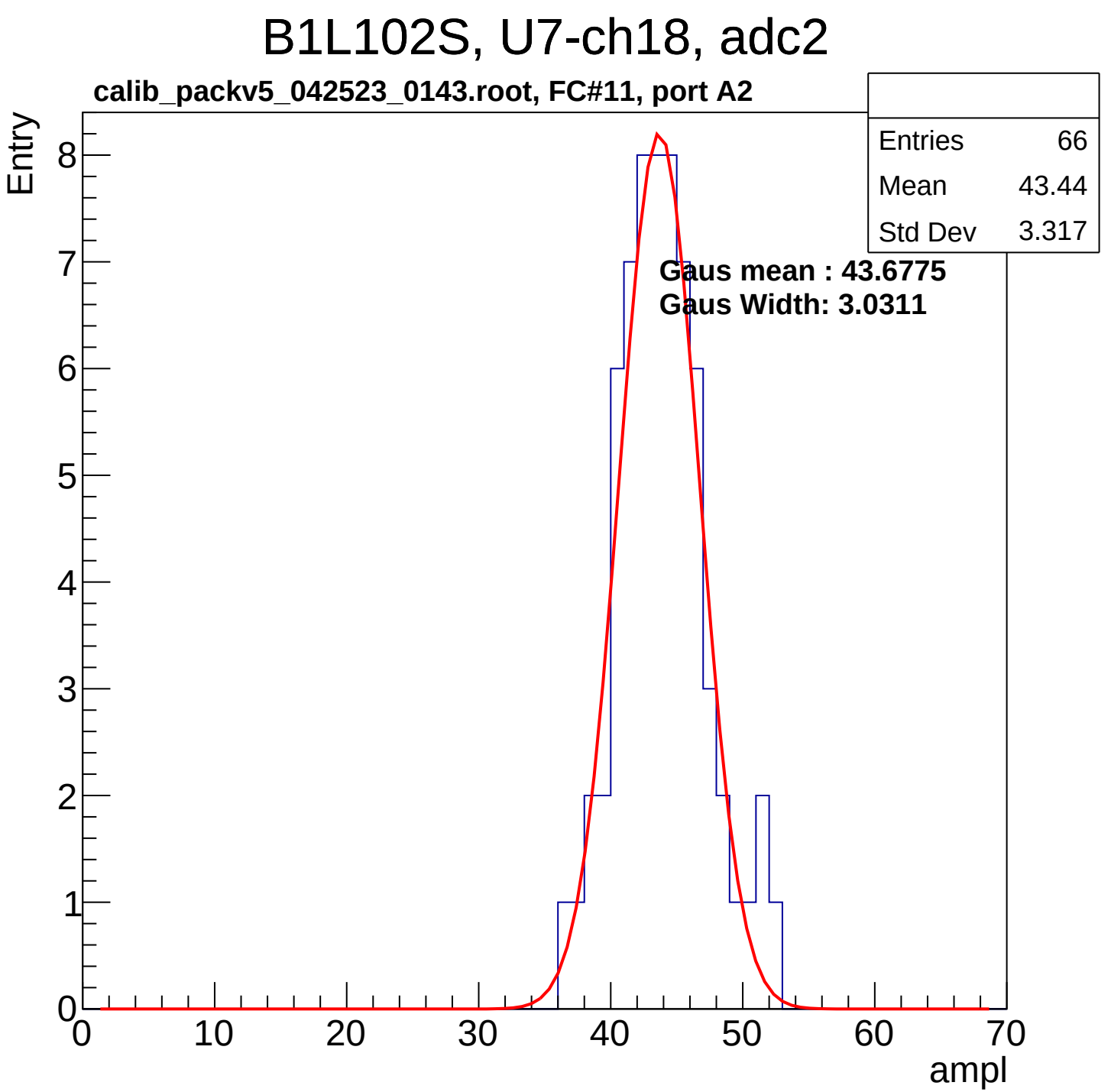
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L102S, U7-ch17, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 8
Mean 53.88
Std Dev 20.44
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L102S, U7-ch17, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 2
Mean 0
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L102S, U7-ch18, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 53
Mean 29.19
Std Dev 3.047
Gaus mean : 29.7067
Gaus Width: 3.7386
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L102S, U7-ch18, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 79
Mean 36.01
Std Dev 3.358
Gaus mean : 36.6298
Gaus Width: 3.6737
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L102S, U7-ch18, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 66
Mean 43.44
Std Dev 3.317
Gaus mean : 43.6775
Gaus Width: 3.0311
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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40
50
60
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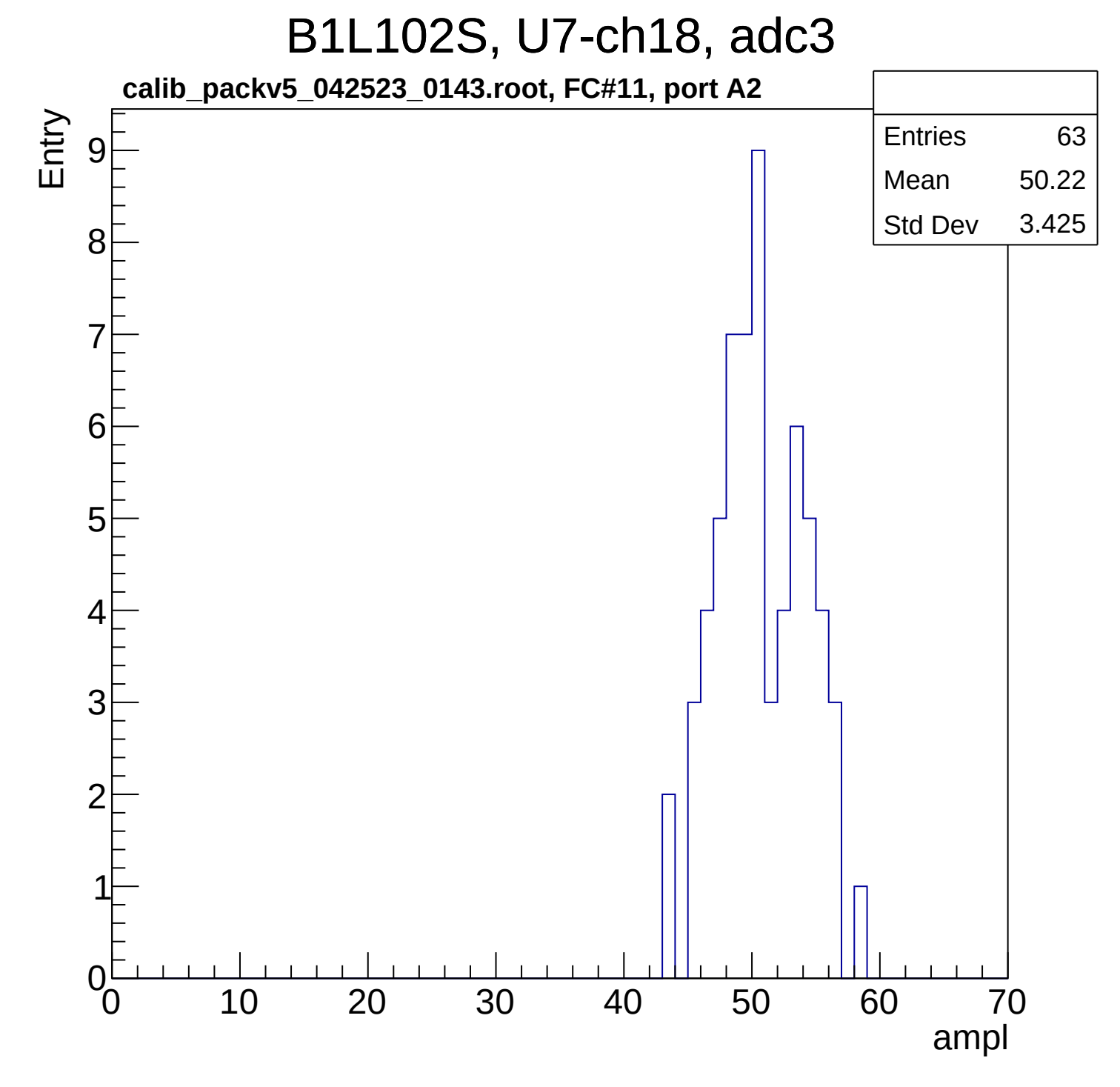
B1L102S, U7-ch18, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 63
Mean 50.22
Std Dev 3.425
Entry
ampl
0
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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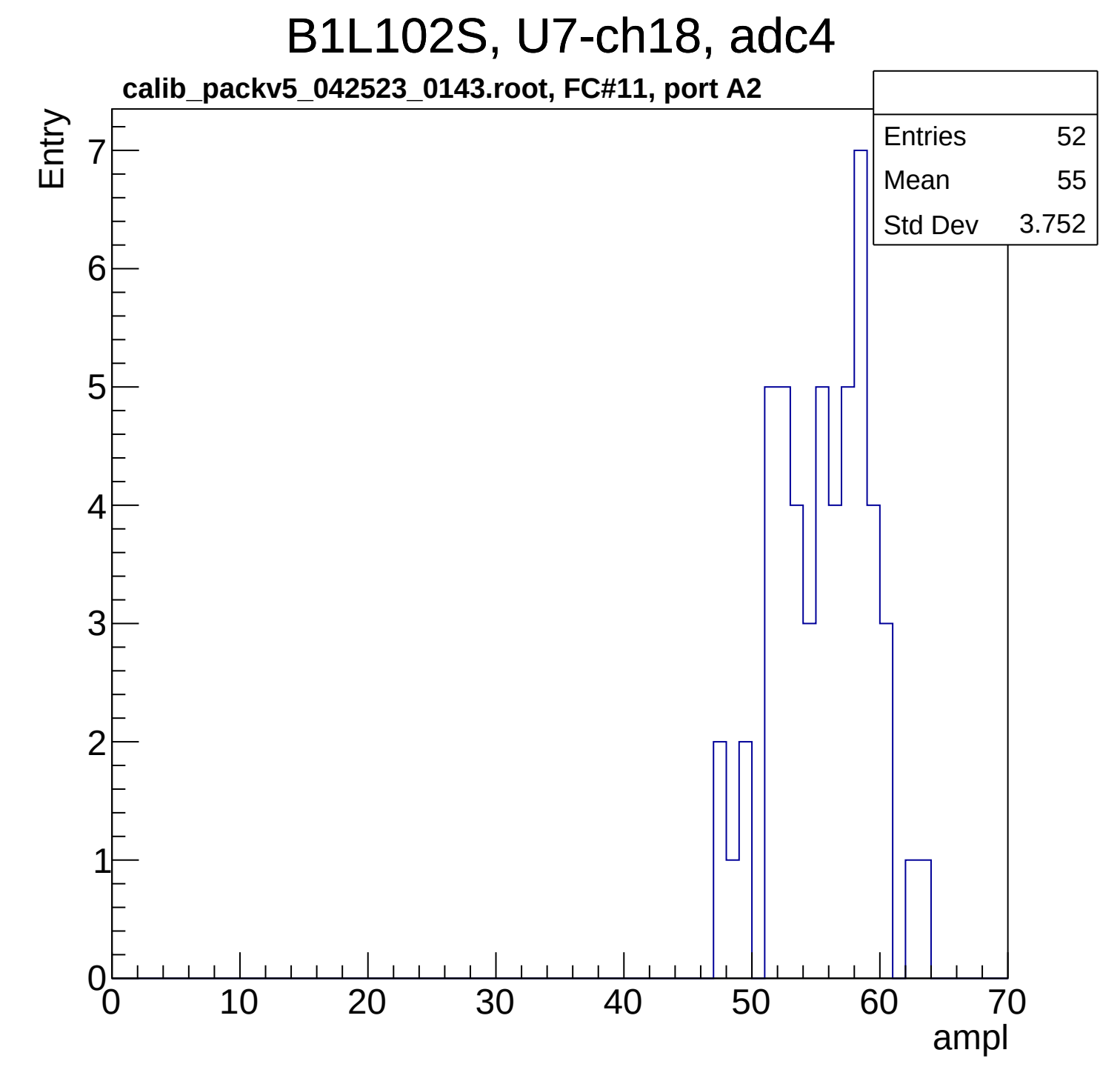
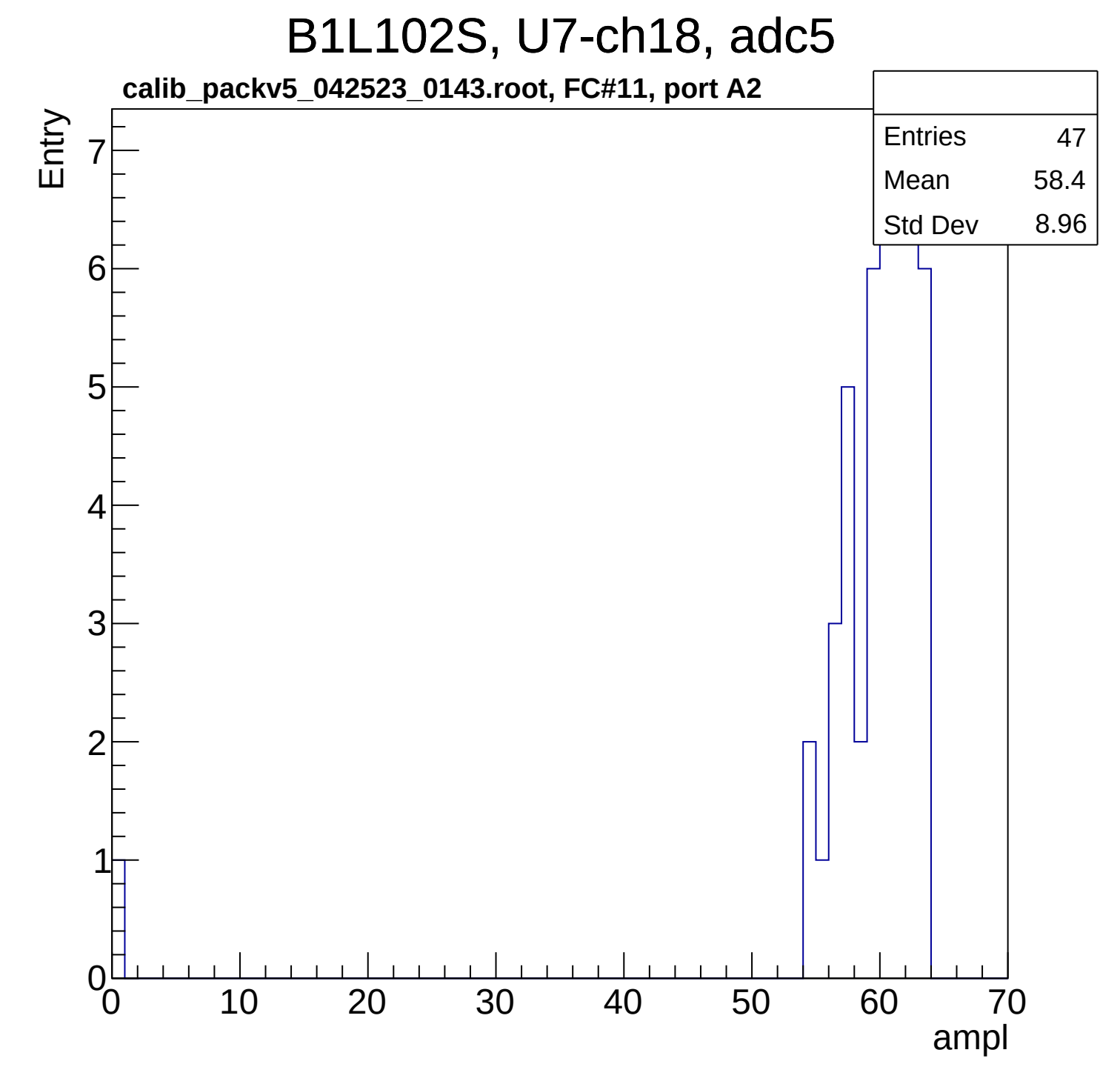
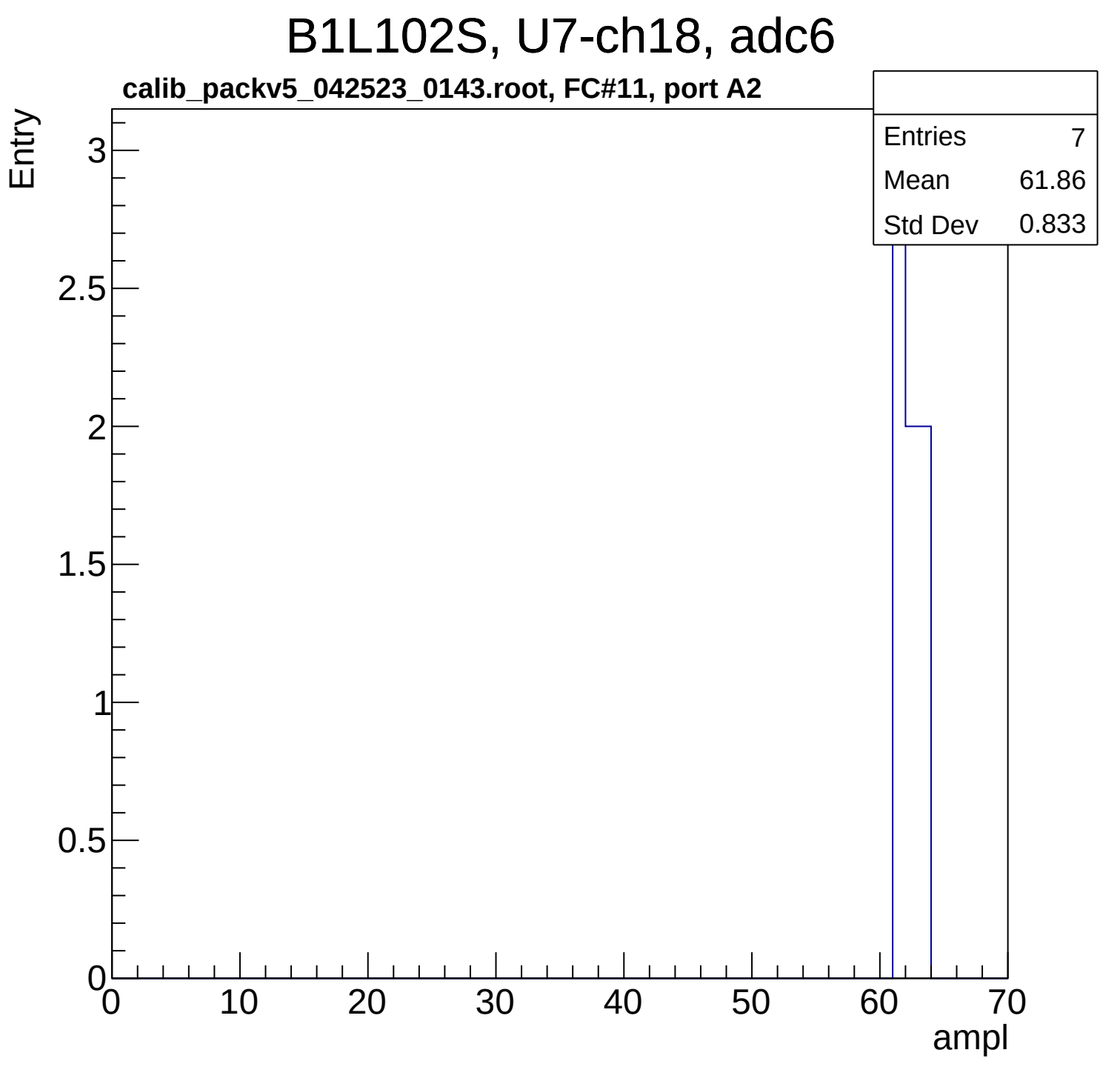
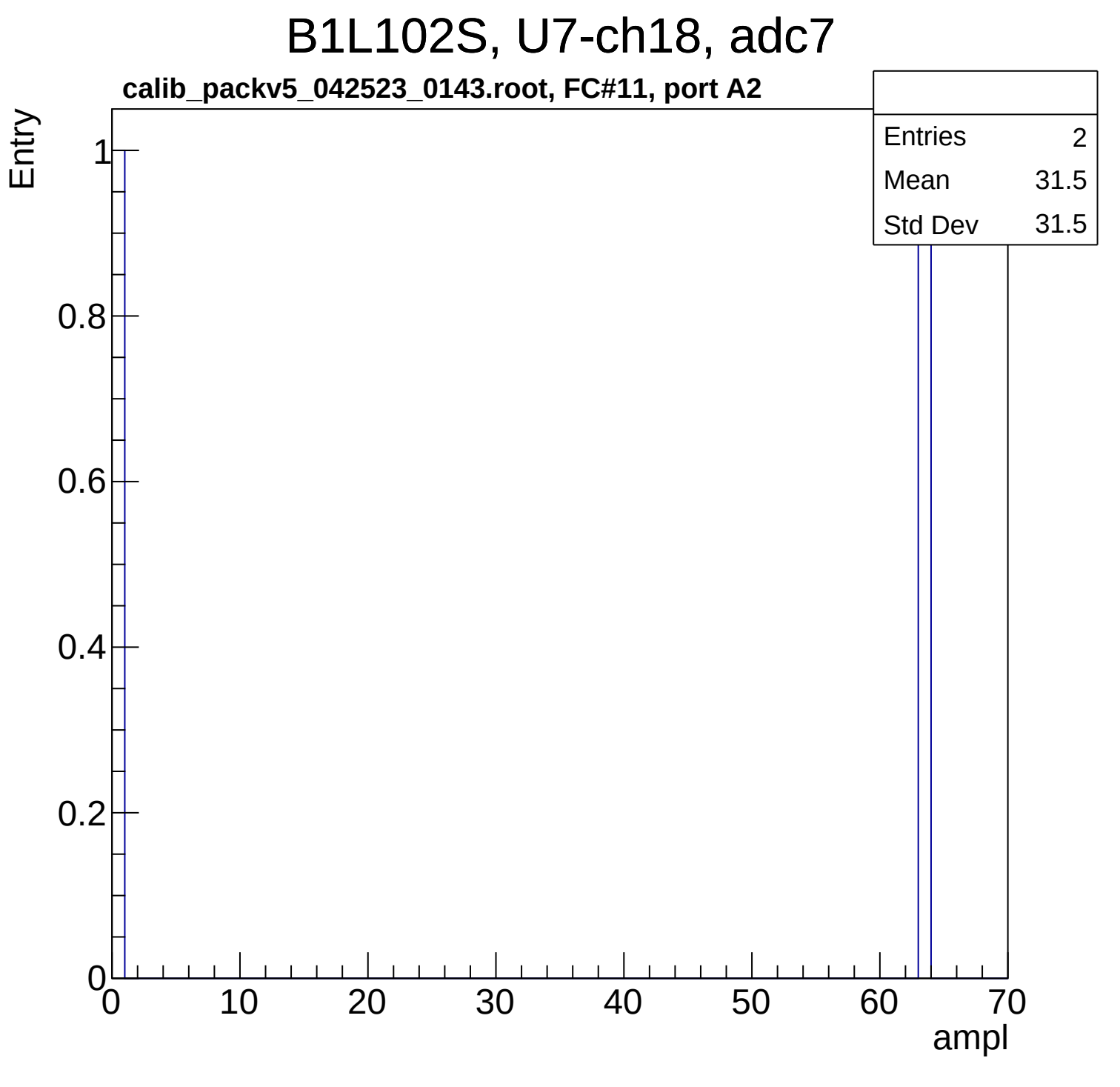
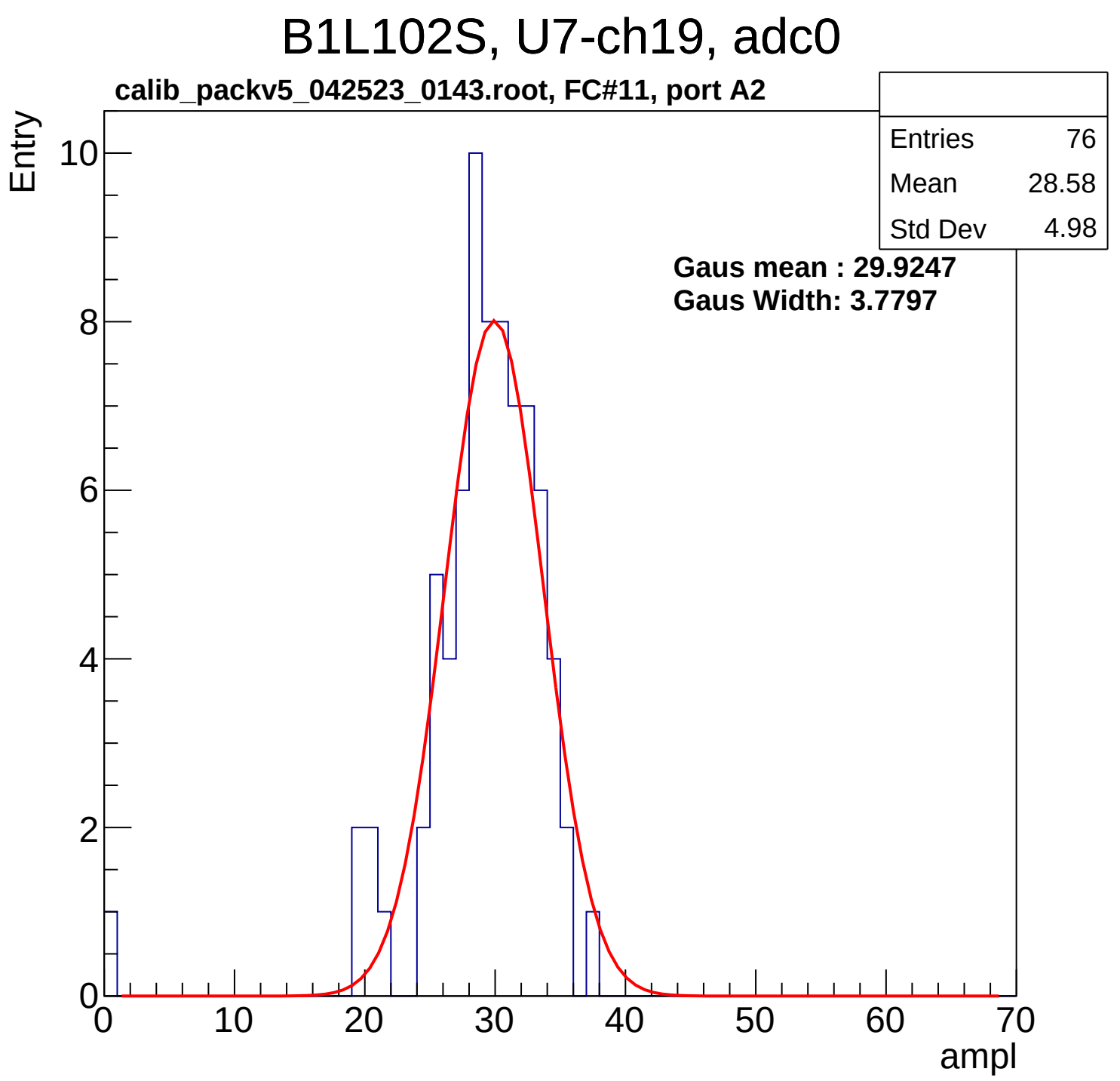
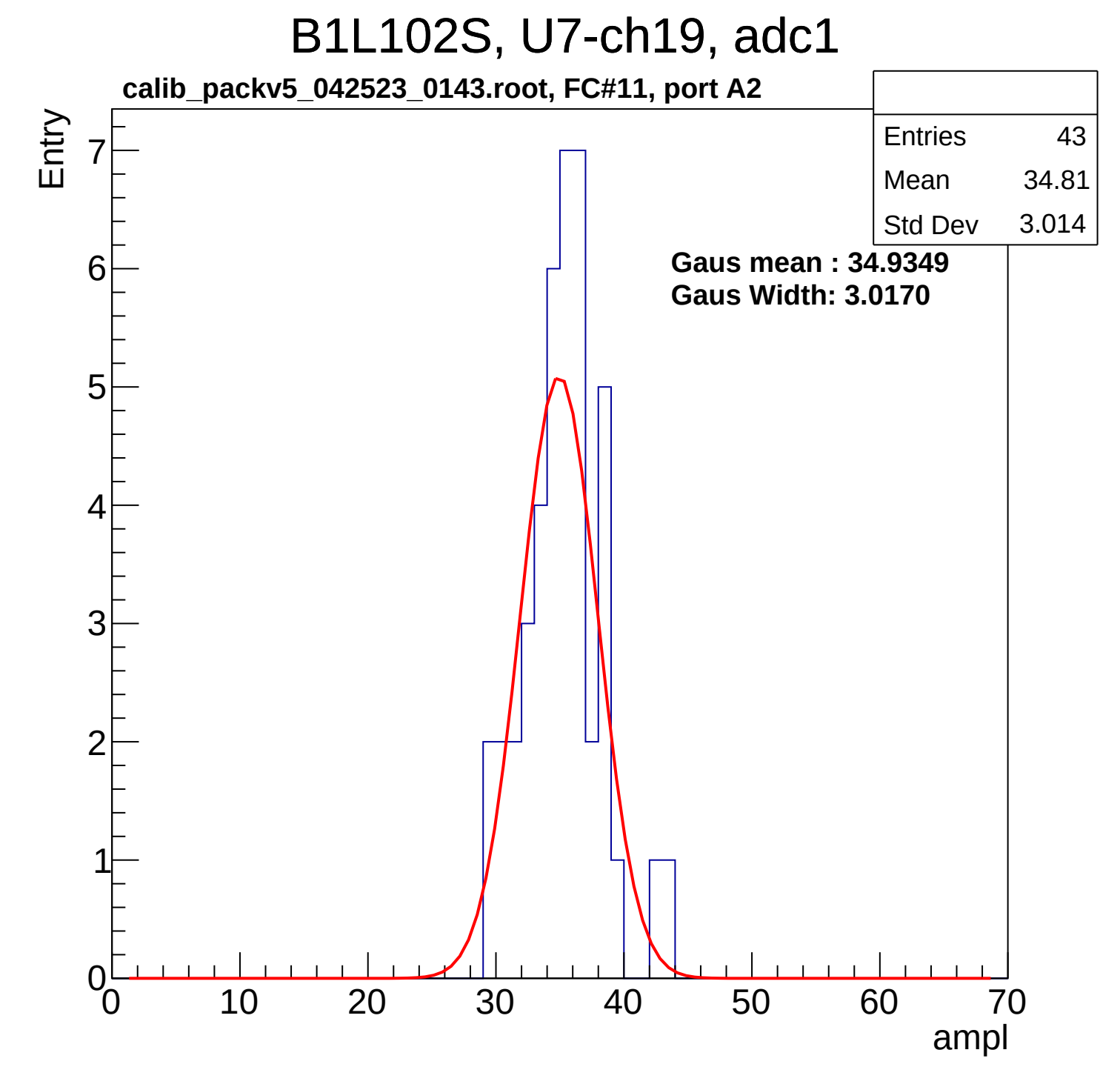

B1L102S, U7-ch18, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 52
Mean 55
Std Dev 3.752
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L102S, U7-ch18, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 47
Mean 58.4
Std Dev 8.96
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L102S, U7-ch18, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 7
Mean 61.86
Std Dev 0.833
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L102S, U7-ch18, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 2
Mean 31.5
Std Dev 31.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U7-ch19, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 76
Mean 28.58
Std Dev 4.98
Gaus mean : 29.9247
Gaus Width: 3.7797
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L102S, U7-ch19, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 43
Mean 34.81
Std Dev 3.014
Gaus mean : 34.9349
Gaus Width: 3.0170
Entry
ampl
0
1
2
3
4
5
6
7
0
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40
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60
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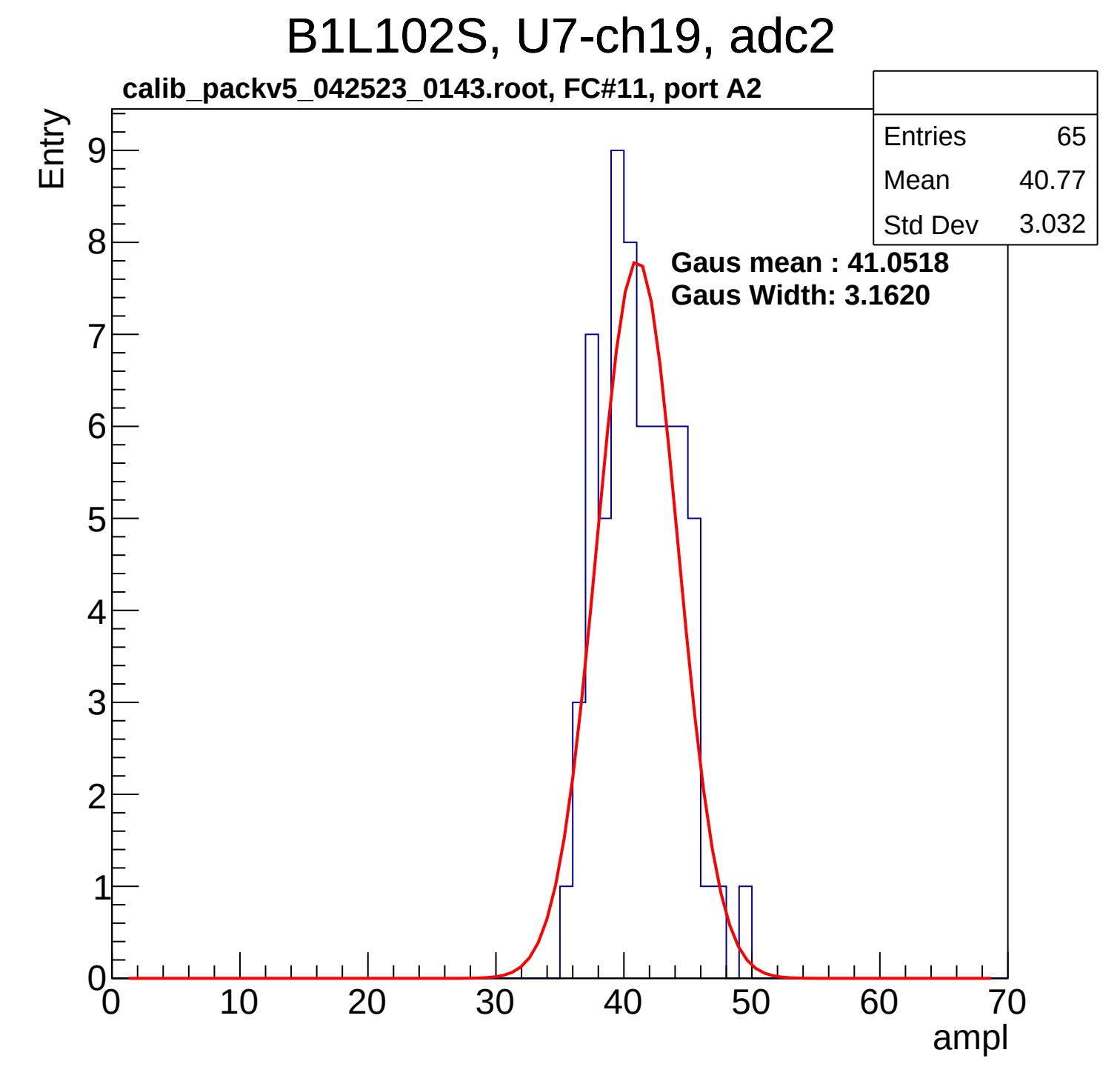
B1L102S, U7-ch19, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 65
Mean 40.77
Std Dev 3.032
Gaus mean : 41.0518
Gaus Width: 3.1620
Entry
ampl
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3
4
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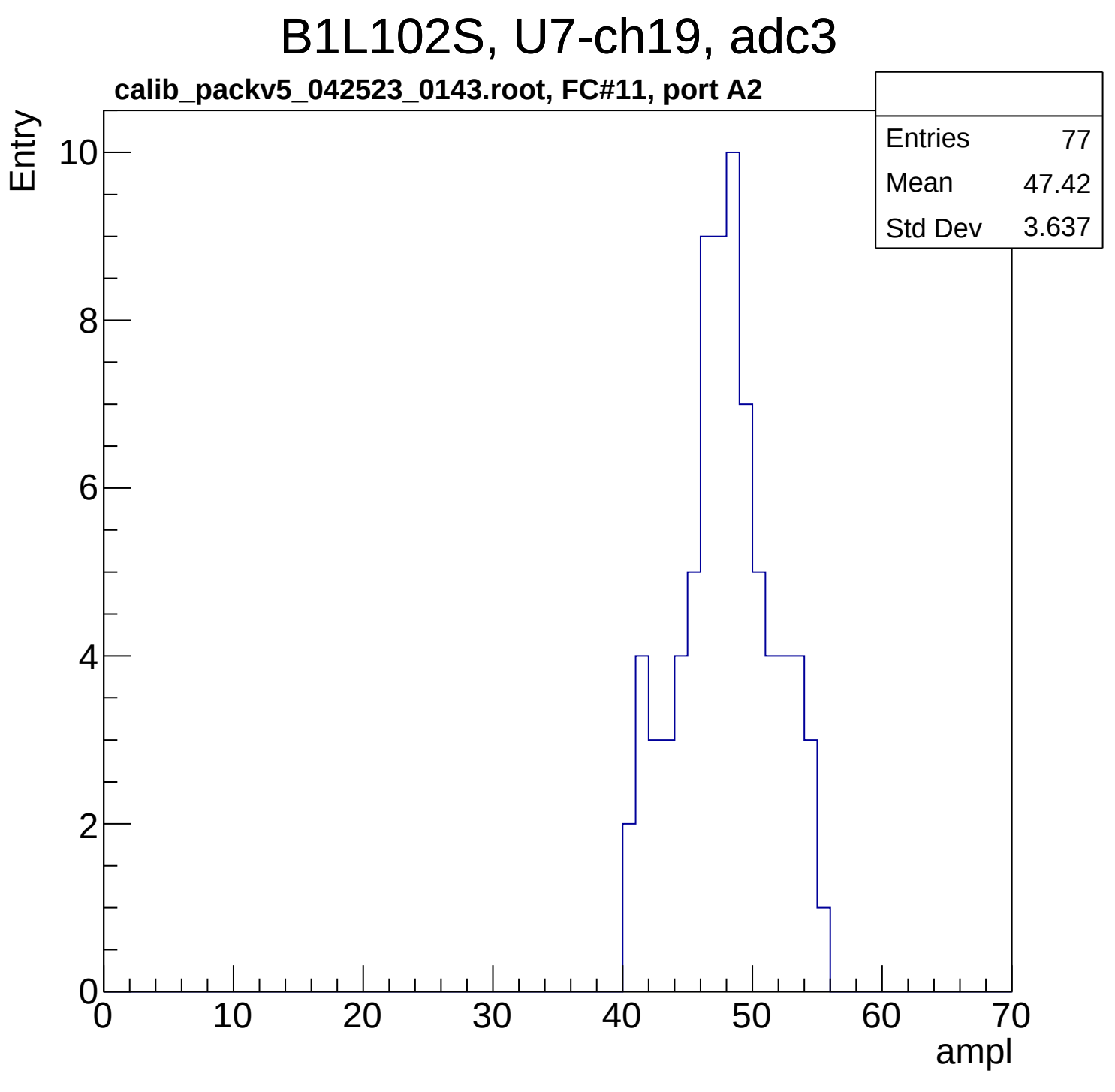
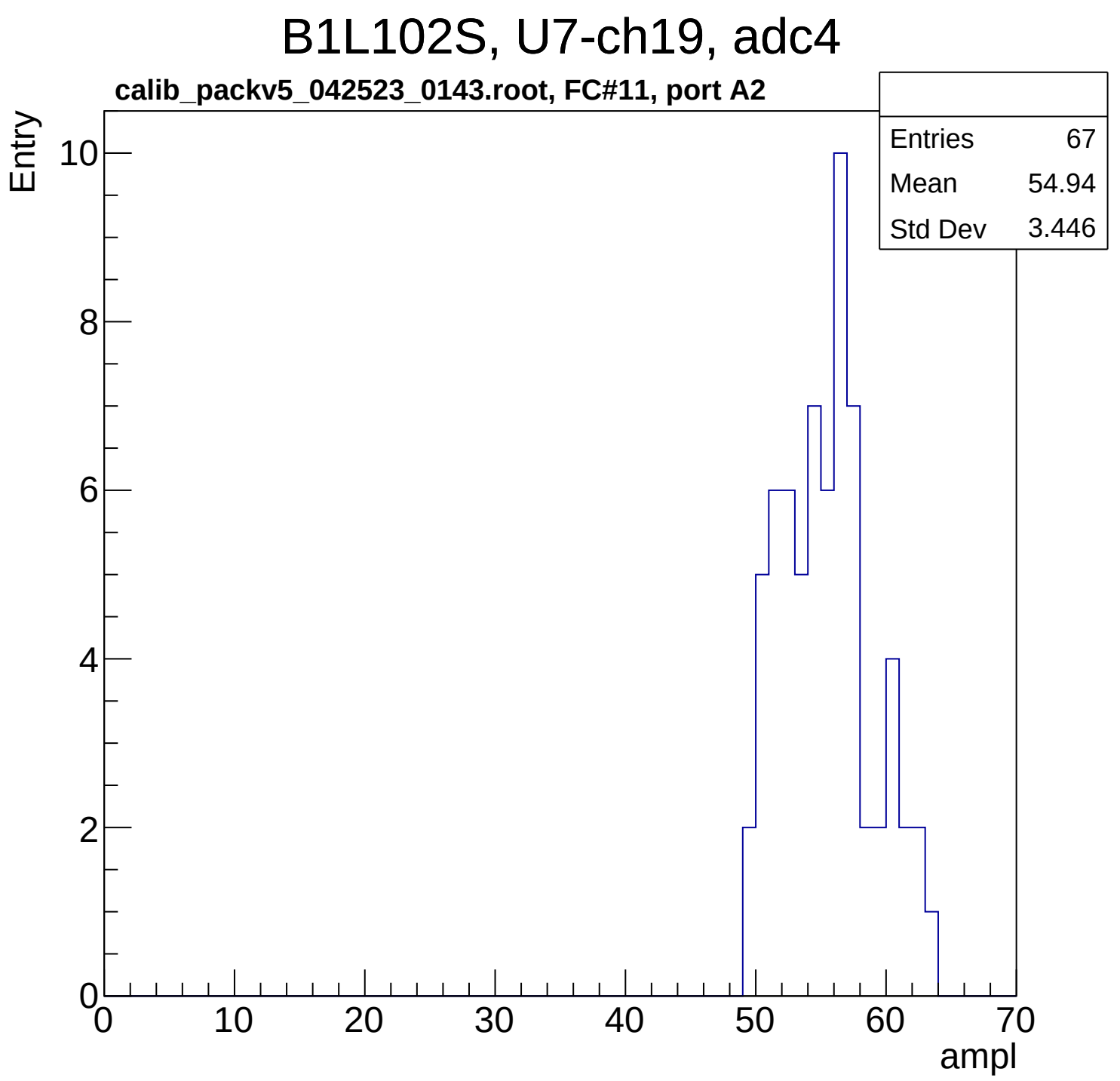

B1L102S, U7-ch19, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 77
Mean 47.42
Std Dev 3.637
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L102S, U7-ch19, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 67
Mean 54.94
Std Dev 3.446
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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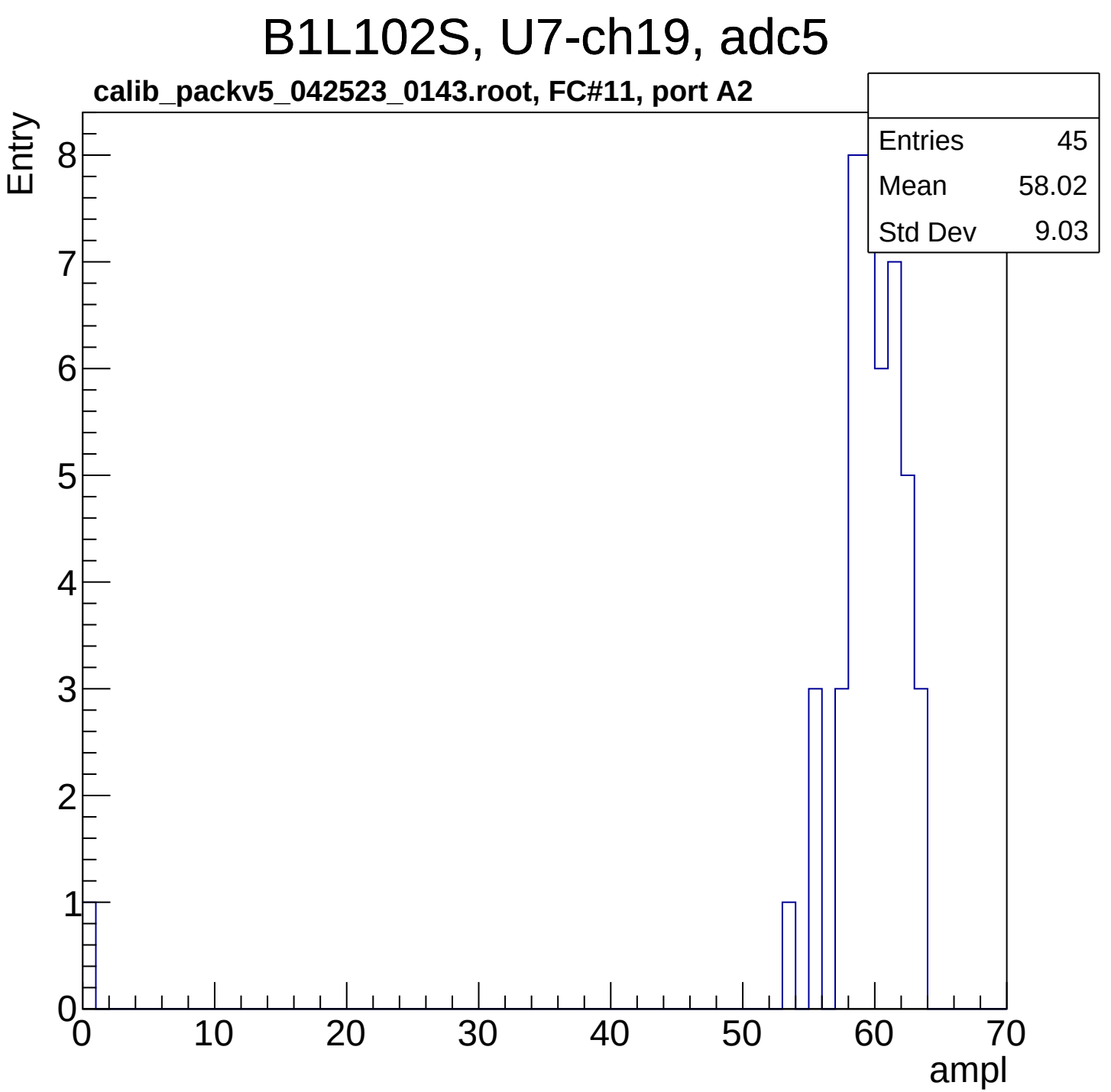
B1L102S, U7-ch19, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 45
Mean 58.02
Std Dev 9.03
Entry
ampl
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1
2
3
4
5
6
7
8
0
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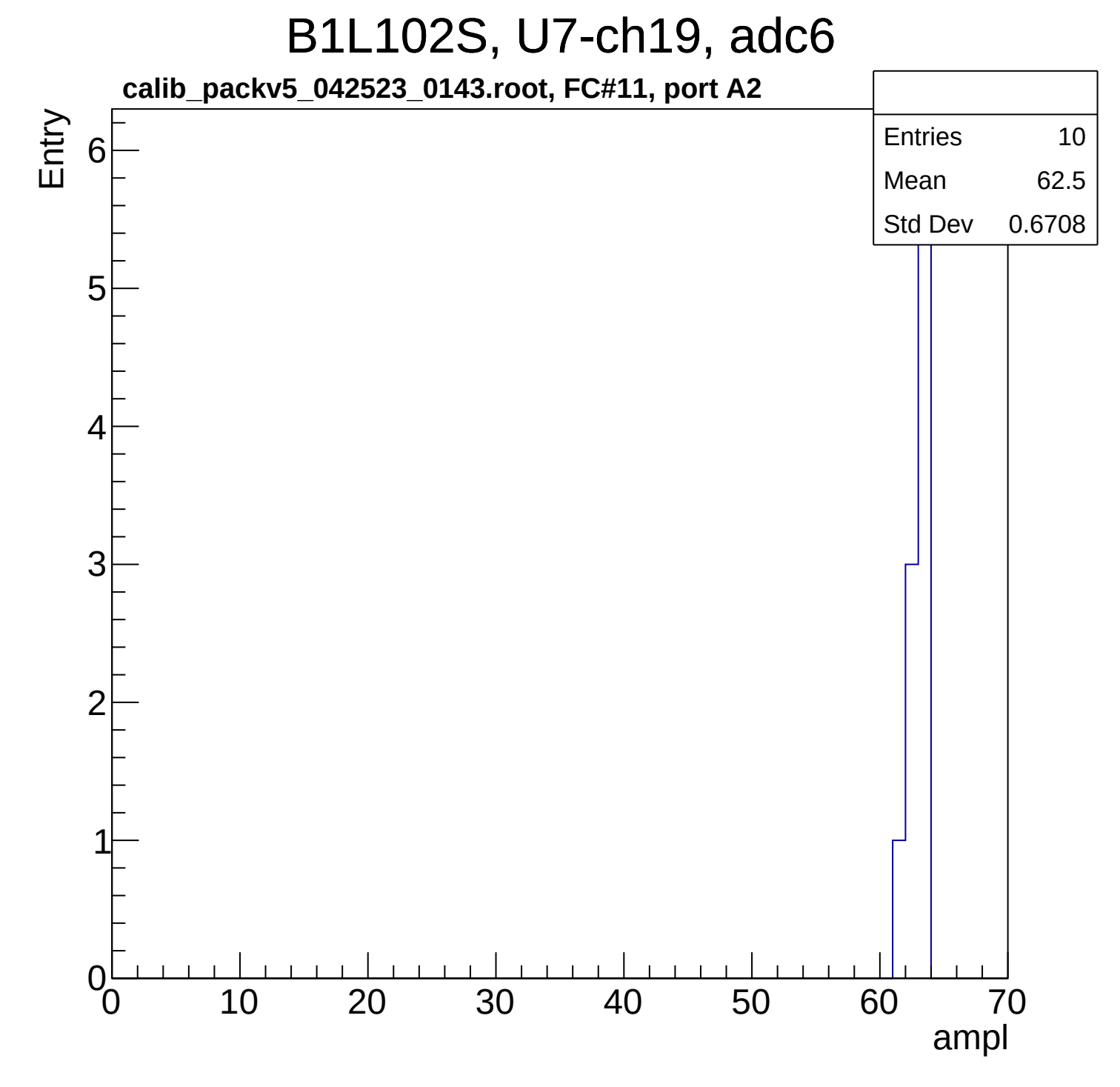
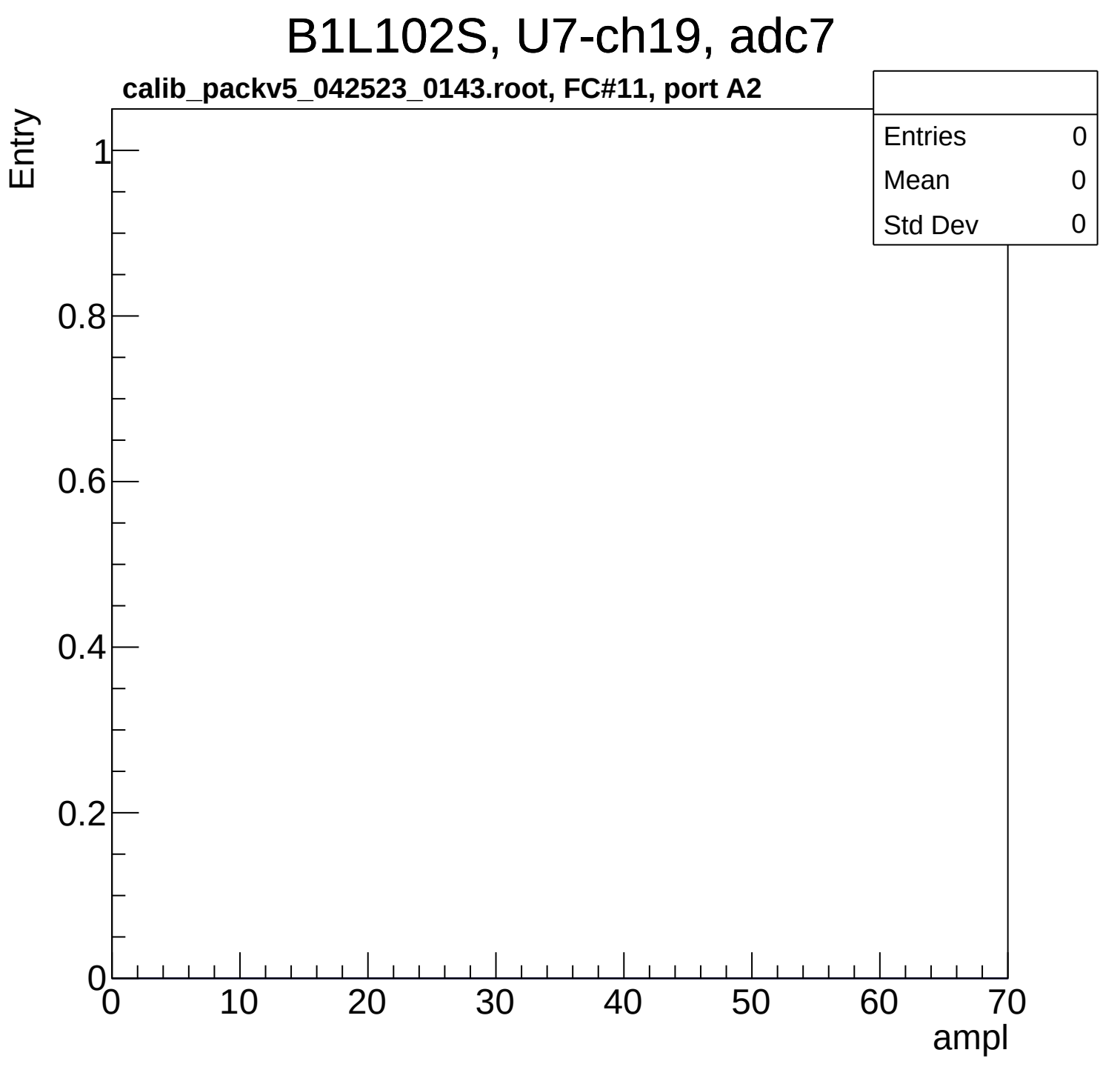
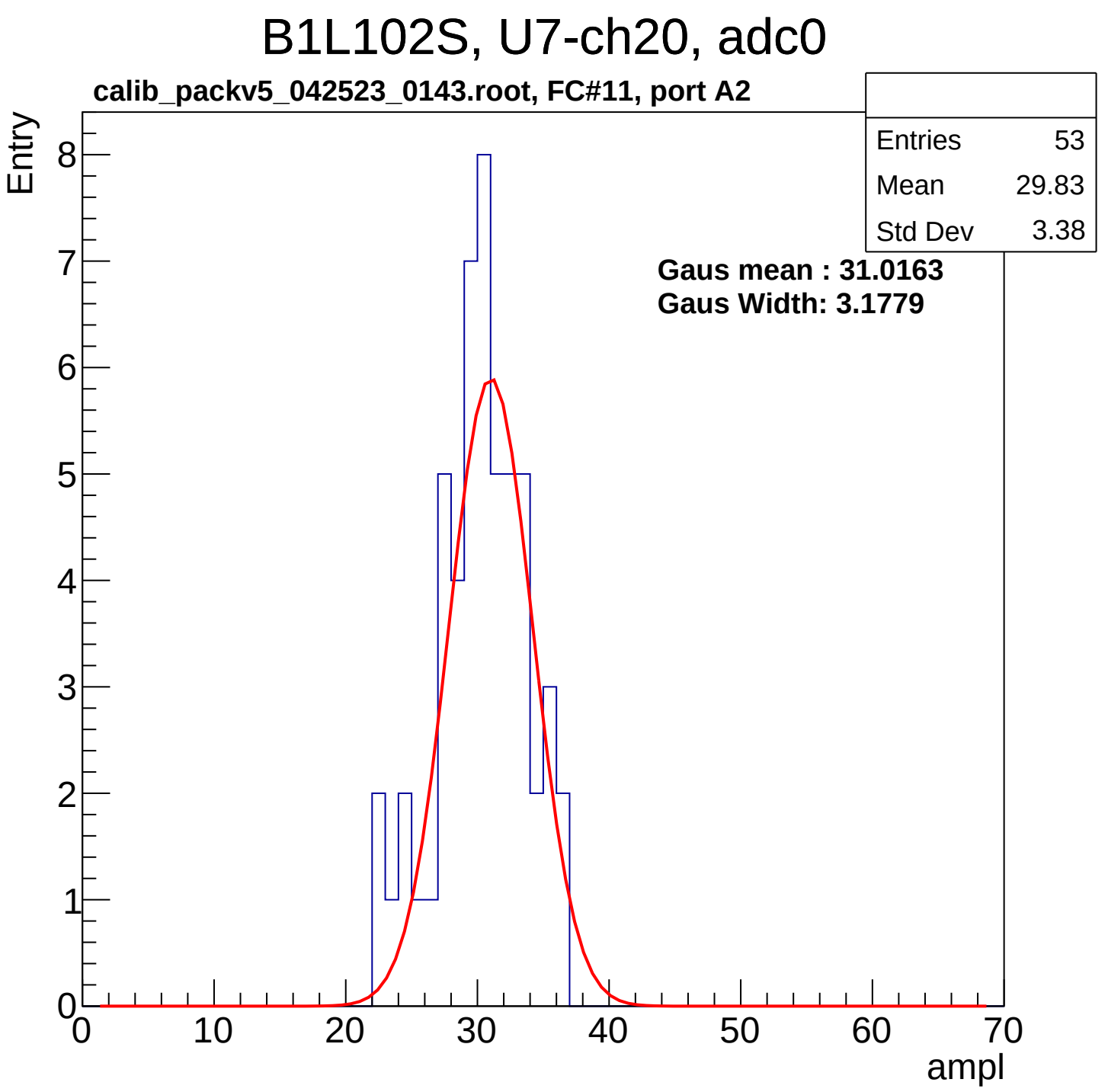

B1L102S, U7-ch19, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 10
Mean 62.5
Std Dev 0.6708
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L102S, U7-ch19, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U7-ch20, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 53
Mean 29.83
Std Dev 3.38
Gaus mean : 31.0163
Gaus Width: 3.1779
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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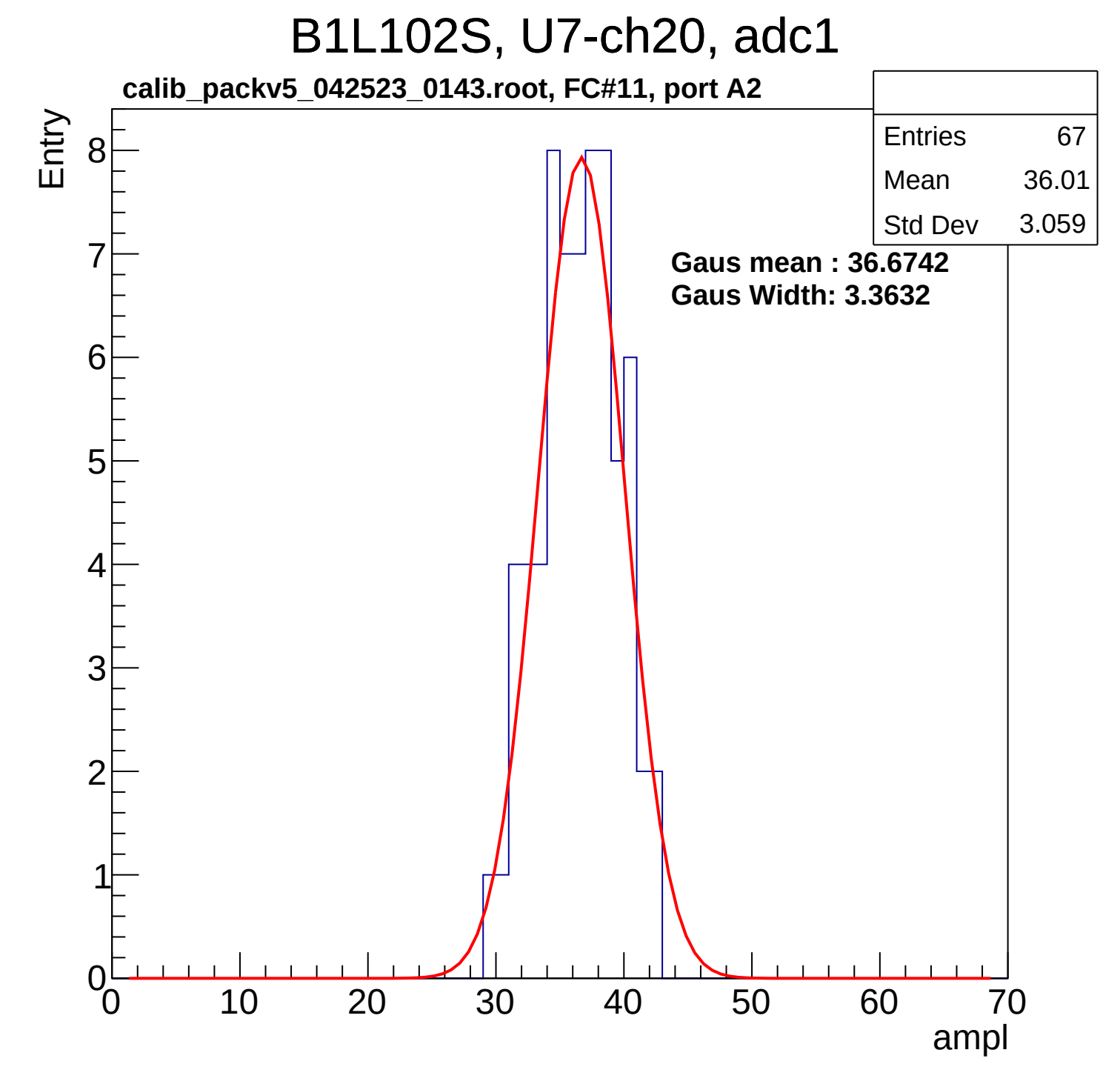
B1L102S, U7-ch20, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 67
Mean 36.01
Std Dev 3.059
Gaus mean : 36.6742
Gaus Width: 3.3632
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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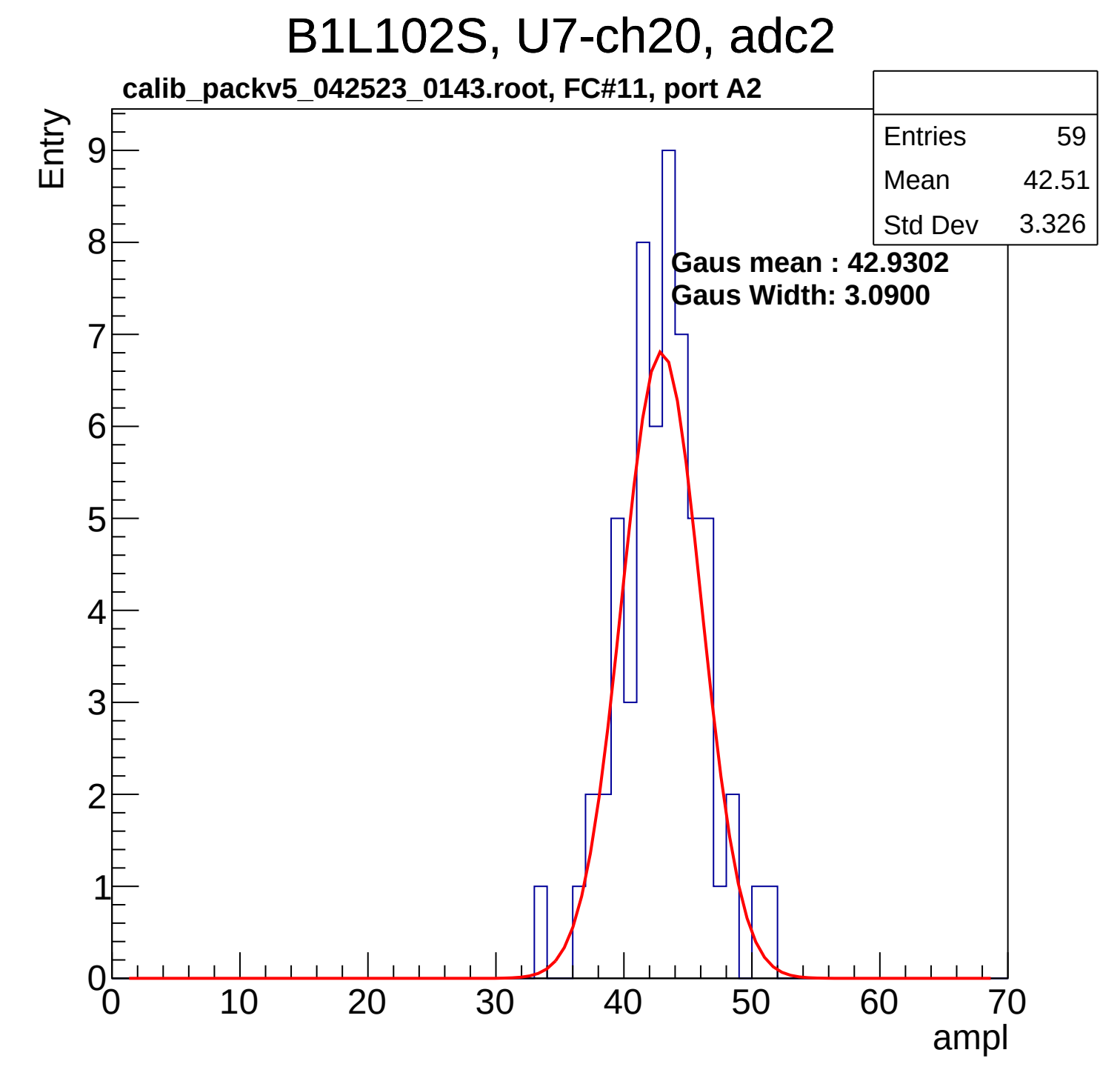
B1L102S, U7-ch20, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 59
Mean 42.51
Std Dev 3.326
Gaus mean : 42.9302
Gaus Width: 3.0900
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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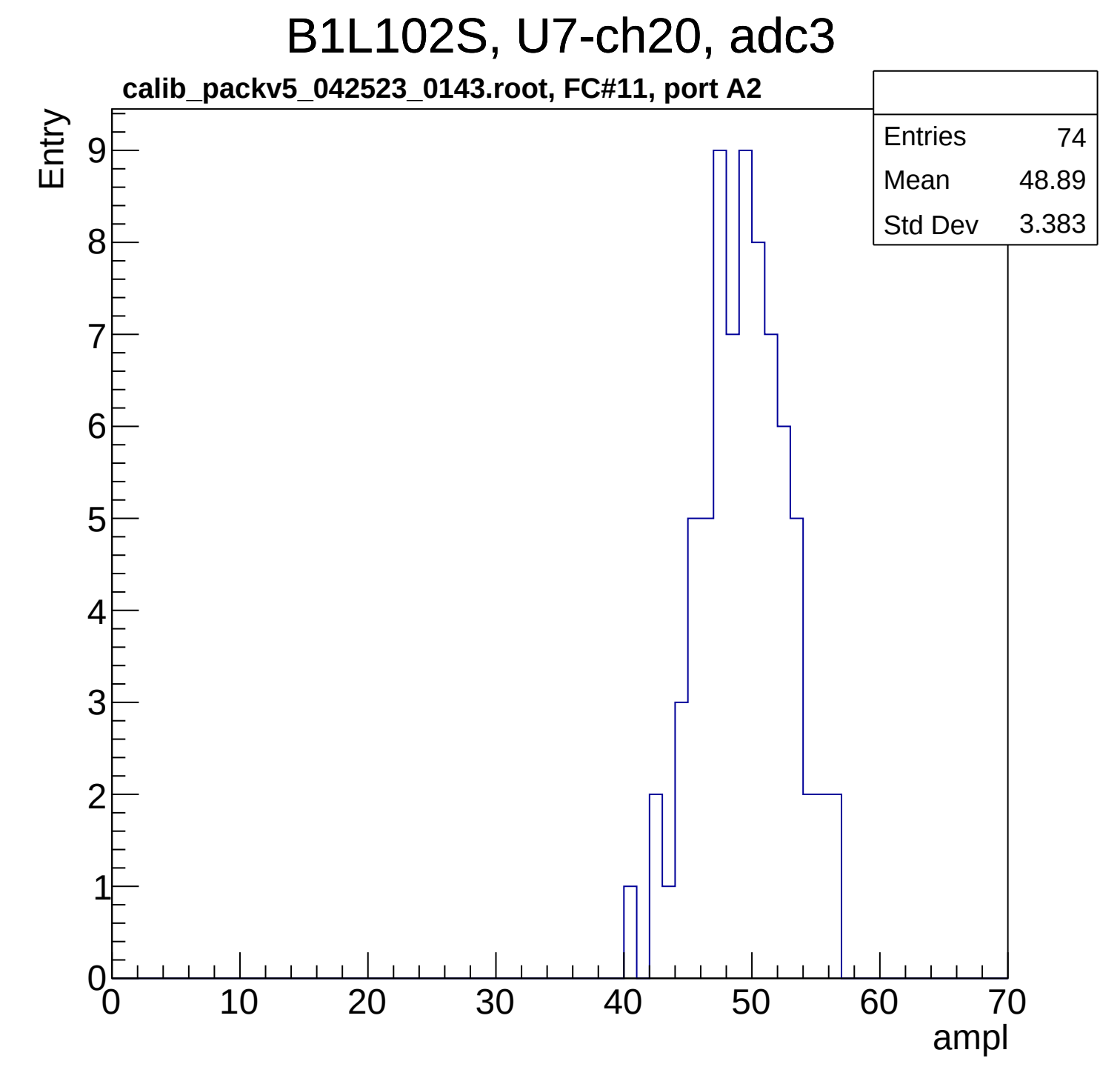
B1L102S, U7-ch20, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 74
Mean 48.89
Std Dev 3.383
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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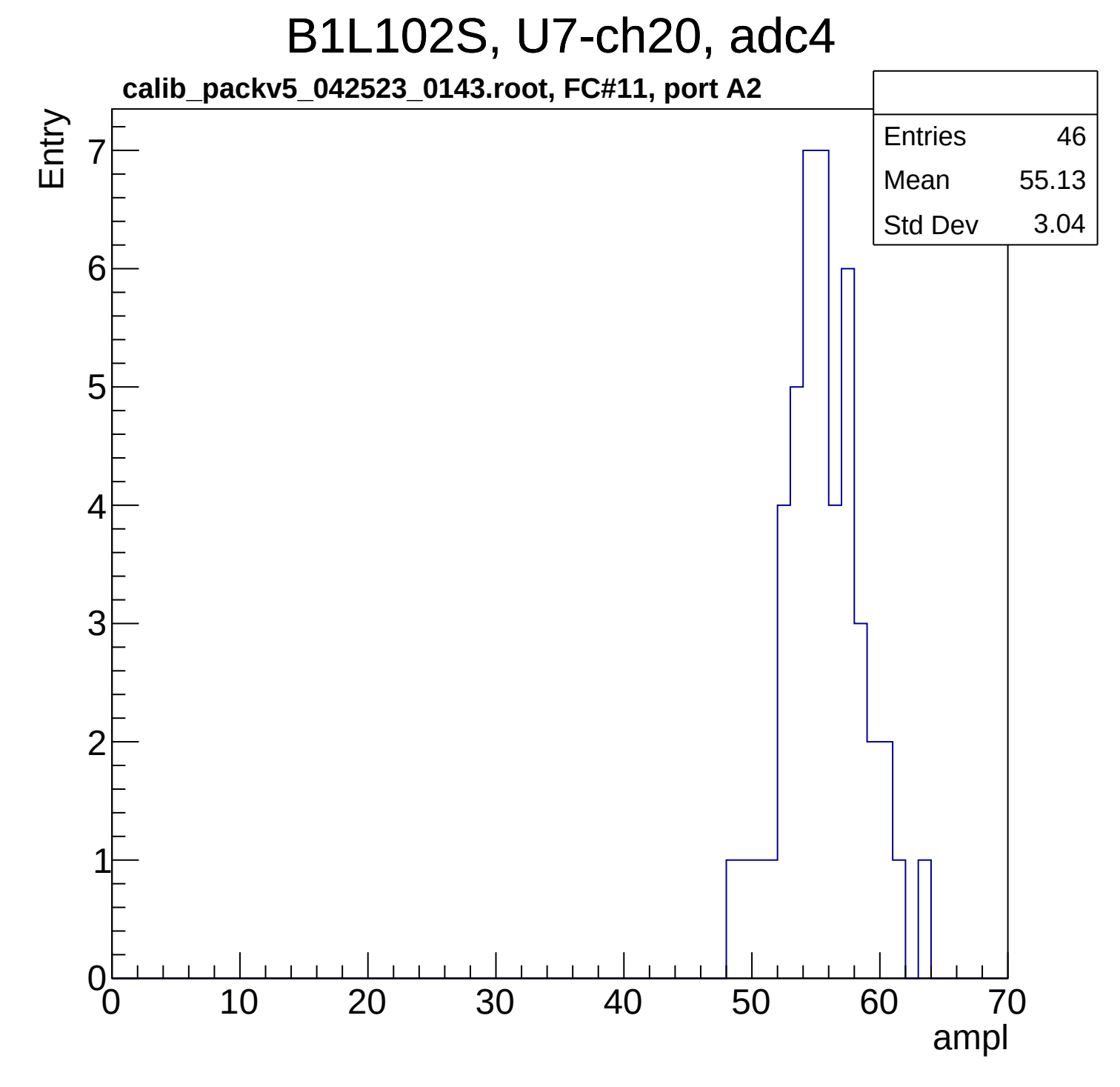
B1L102S, U7-ch20, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 46
Mean 55.13
Std Dev 3.04
Entry
ampl
0
1
2
3
4
5
6
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0
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20
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40
50
60
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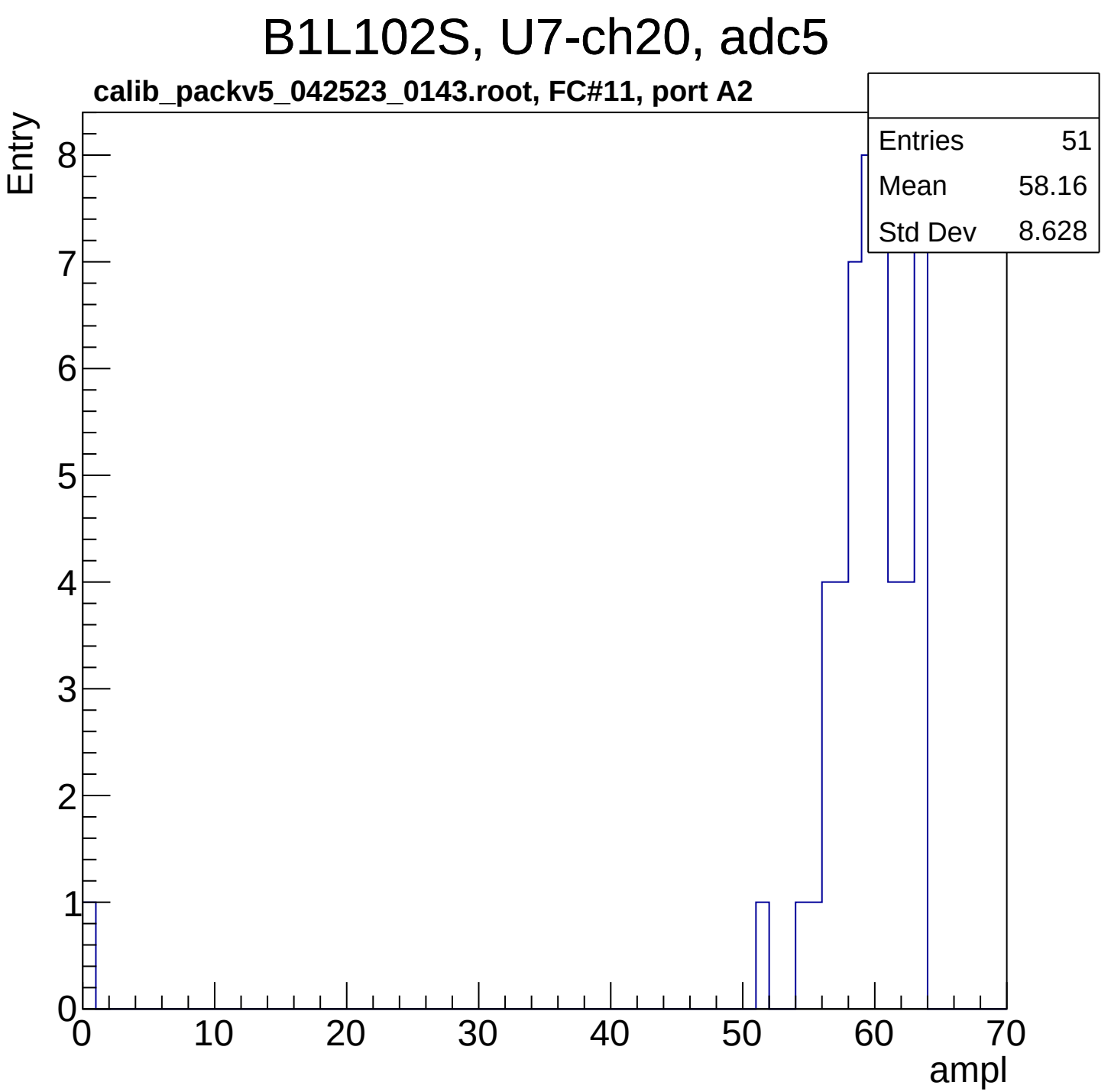
B1L102S, U7-ch20, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 51
Mean 58.16
Std Dev 8.628
Entry
ampl
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2
3
4
5
6
7
8
0
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20
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40
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60
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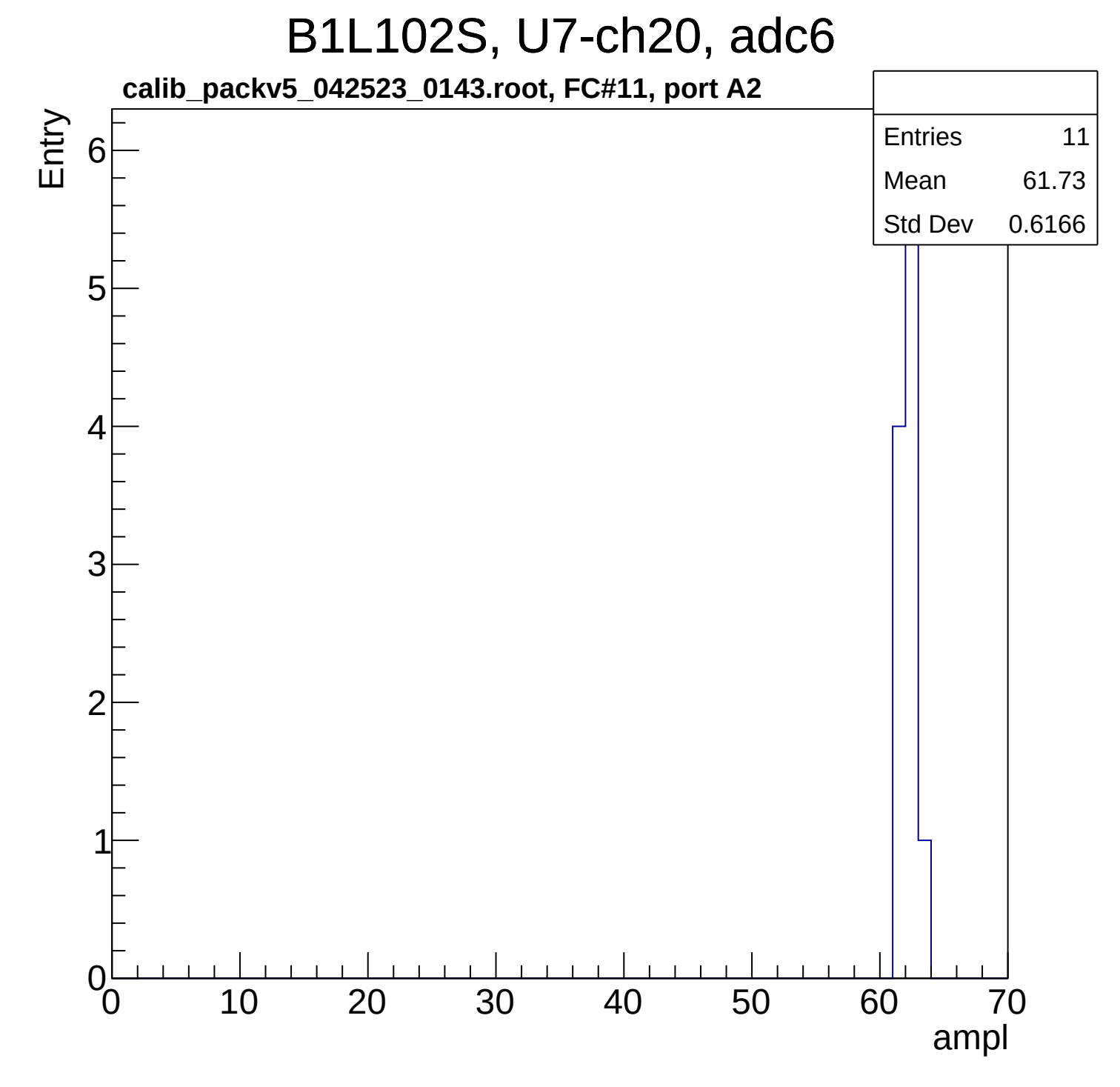
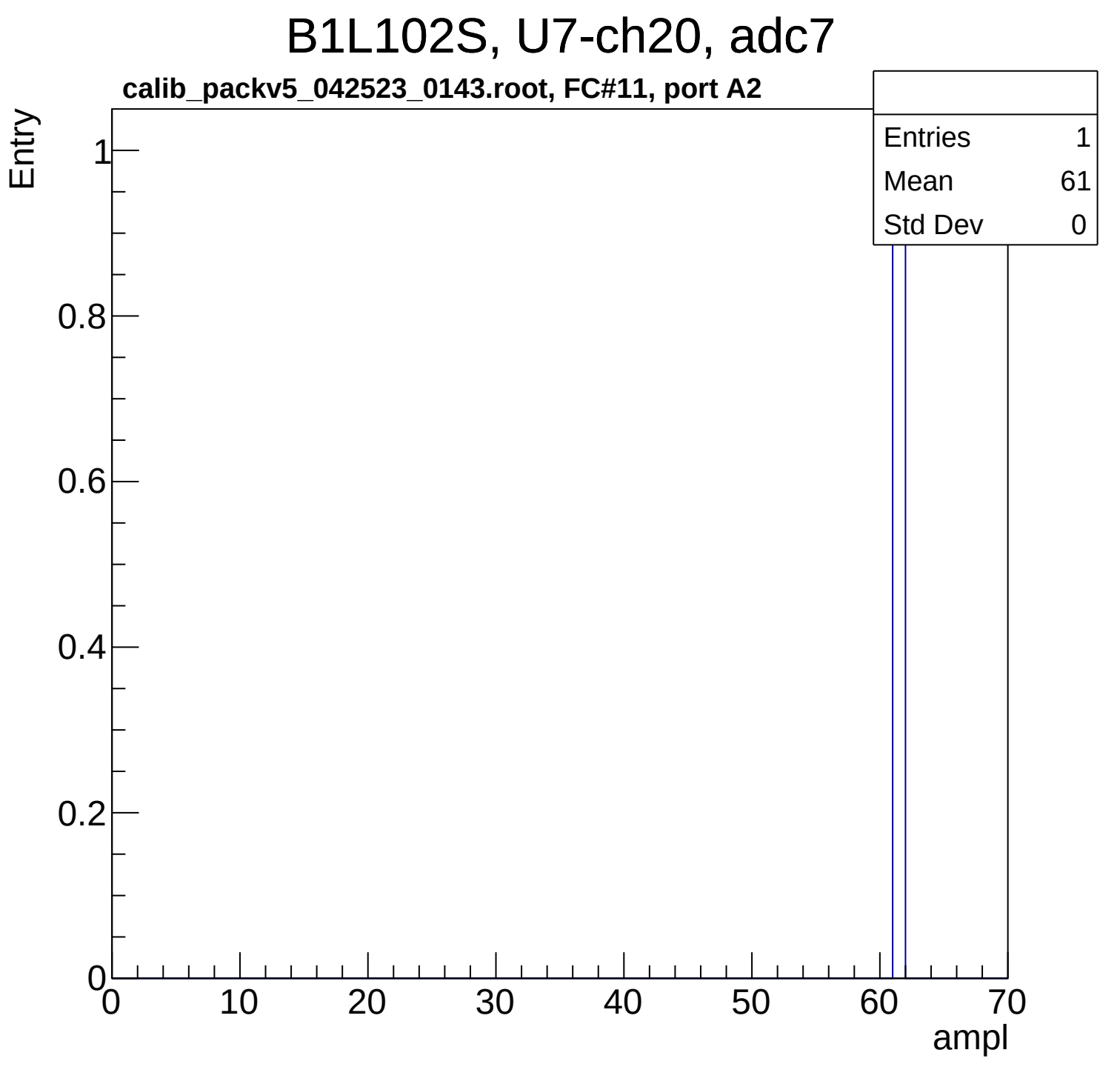

B1L102S, U7-ch20, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 11
Mean 61.73
Std Dev 0.6166
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L102S, U7-ch20, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 1
Mean 61
Std Dev 0
Entry
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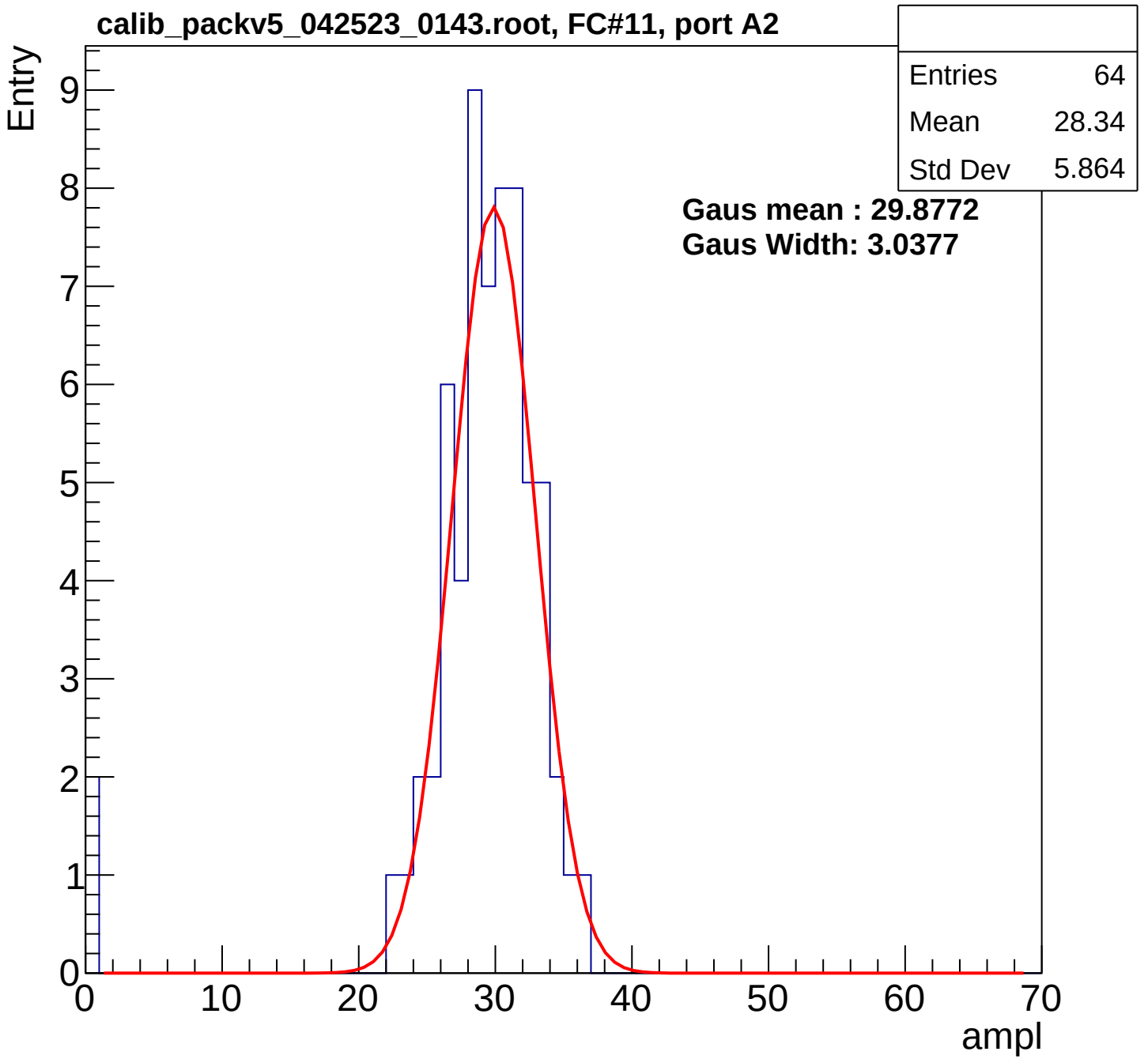
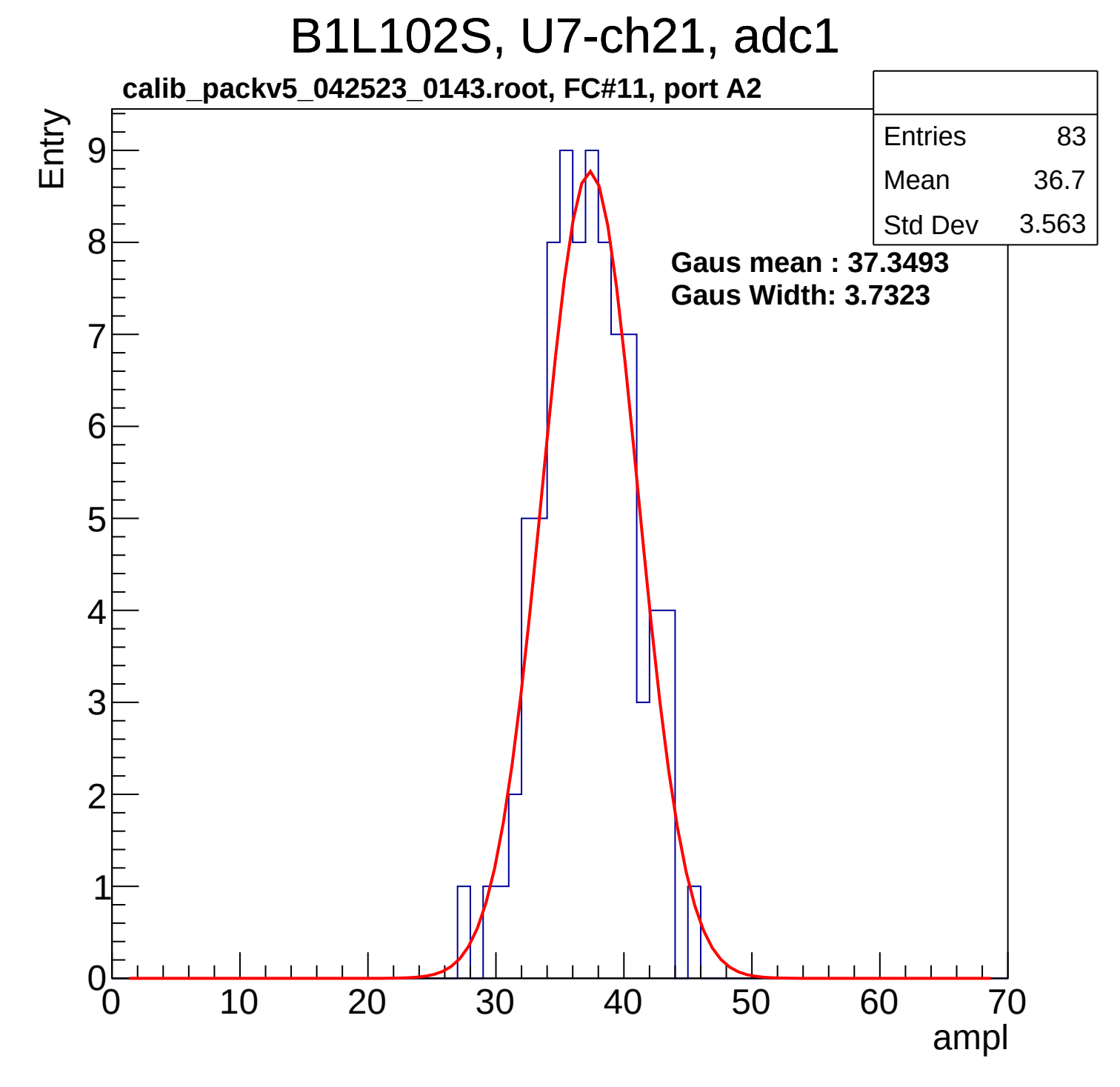
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U7-ch21, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 64
Mean 28.34
Std Dev 5.864
Gaus mean : 29.8772
Gaus Width: 3.0377
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L102S, U7-ch21, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 83
Mean 36.7
Std Dev 3.563
Gaus mean : 37.3493
Gaus Width: 3.7323
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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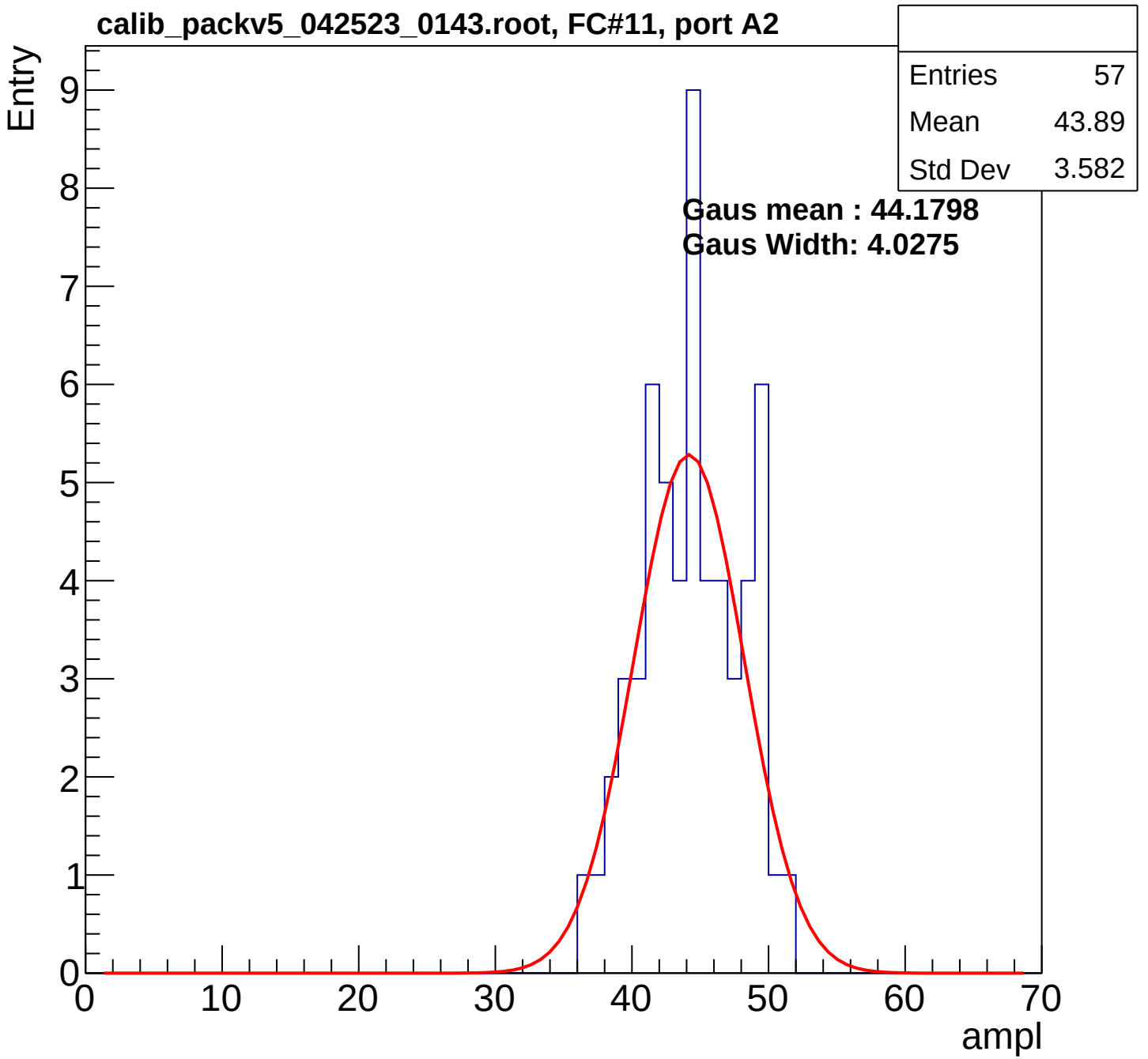
B1L102S, U7-ch21, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 57
Mean 43.89
Std Dev 3.582
Gaus mean : 44.1798
Gaus Width: 4.0275
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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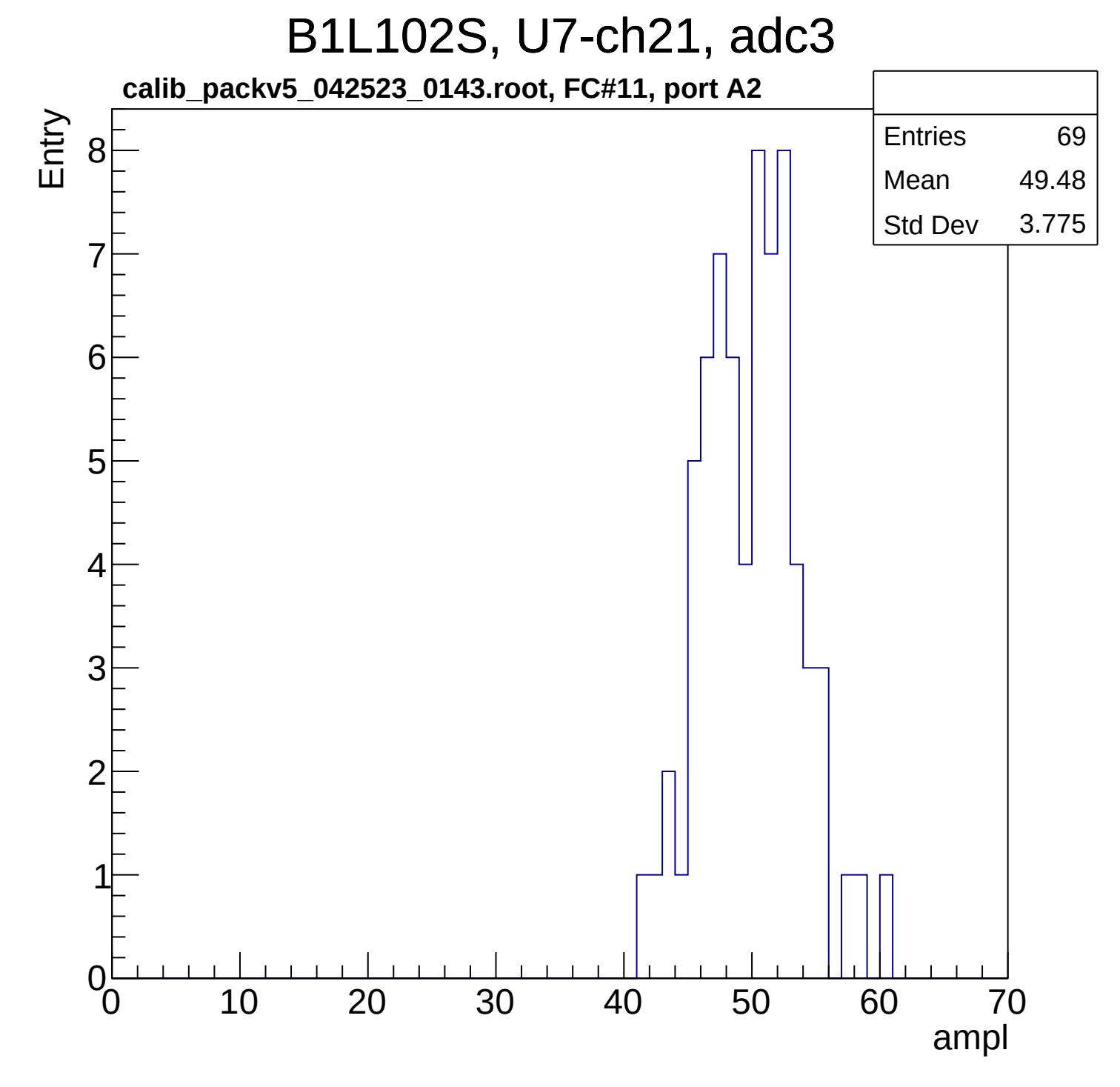
B1L102S, U7-ch21, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 69
Mean 49.48
Std Dev 3.775
Entry
ampl
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2
3
4
5
6
7
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0
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20
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40
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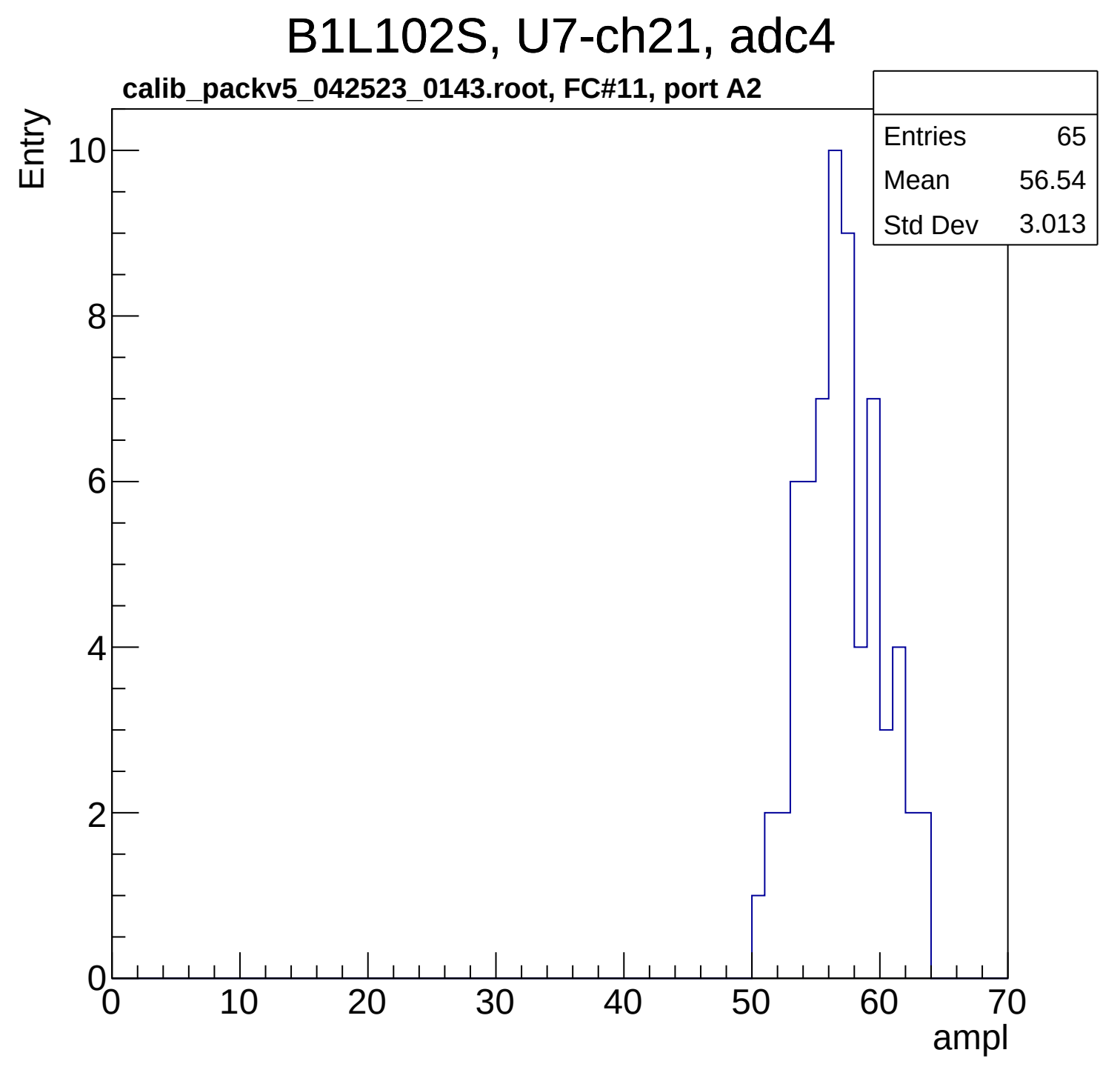
B1L102S, U7-ch21, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 65
Mean 56.54
Std Dev 3.013
Entry
ampl
0
2
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6
8
10
0
10
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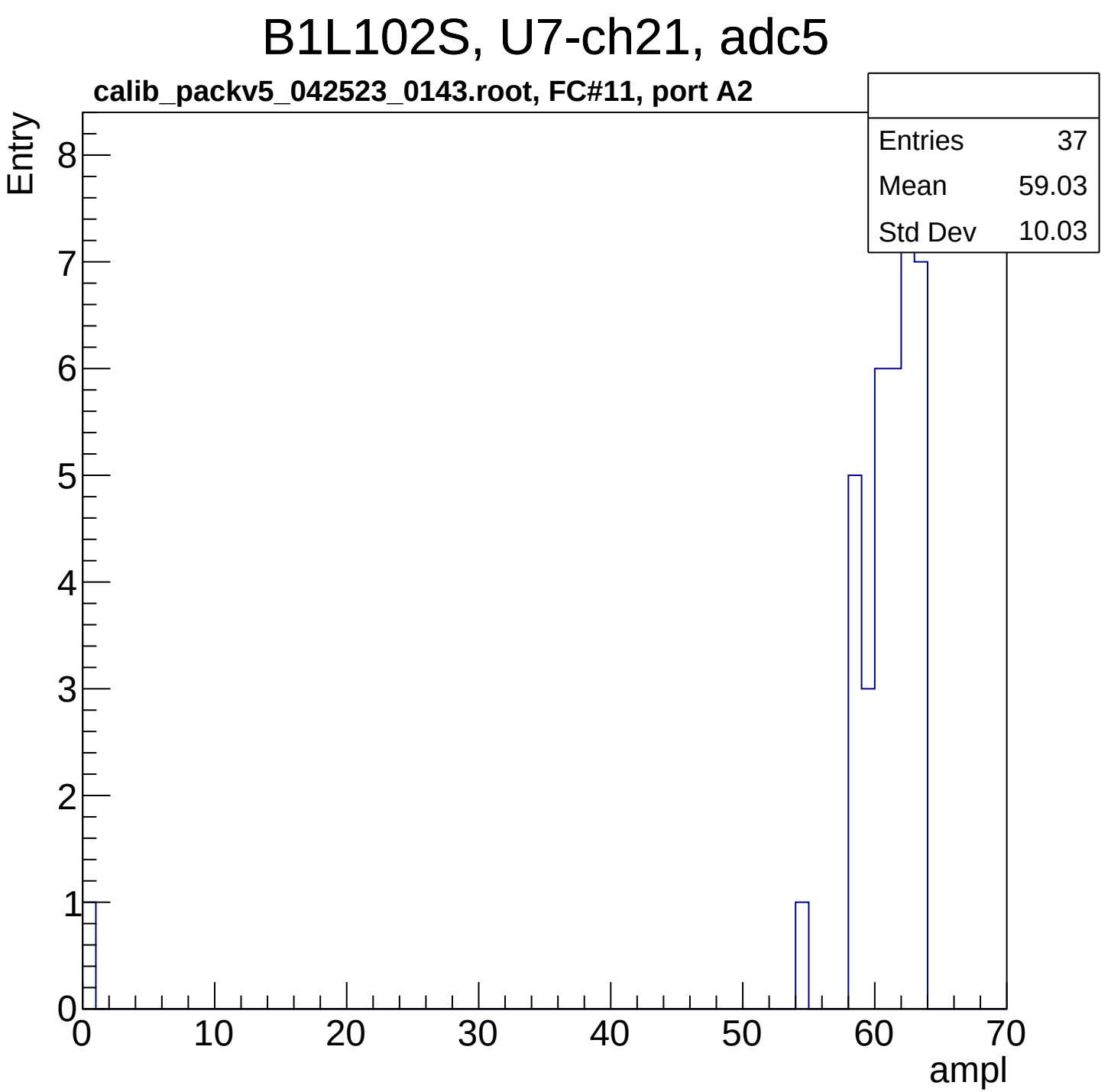
30
40
50
60
70


B1L102S, U7-ch21, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 37
Mean 59.03
Std Dev 10.03
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
30
40
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60
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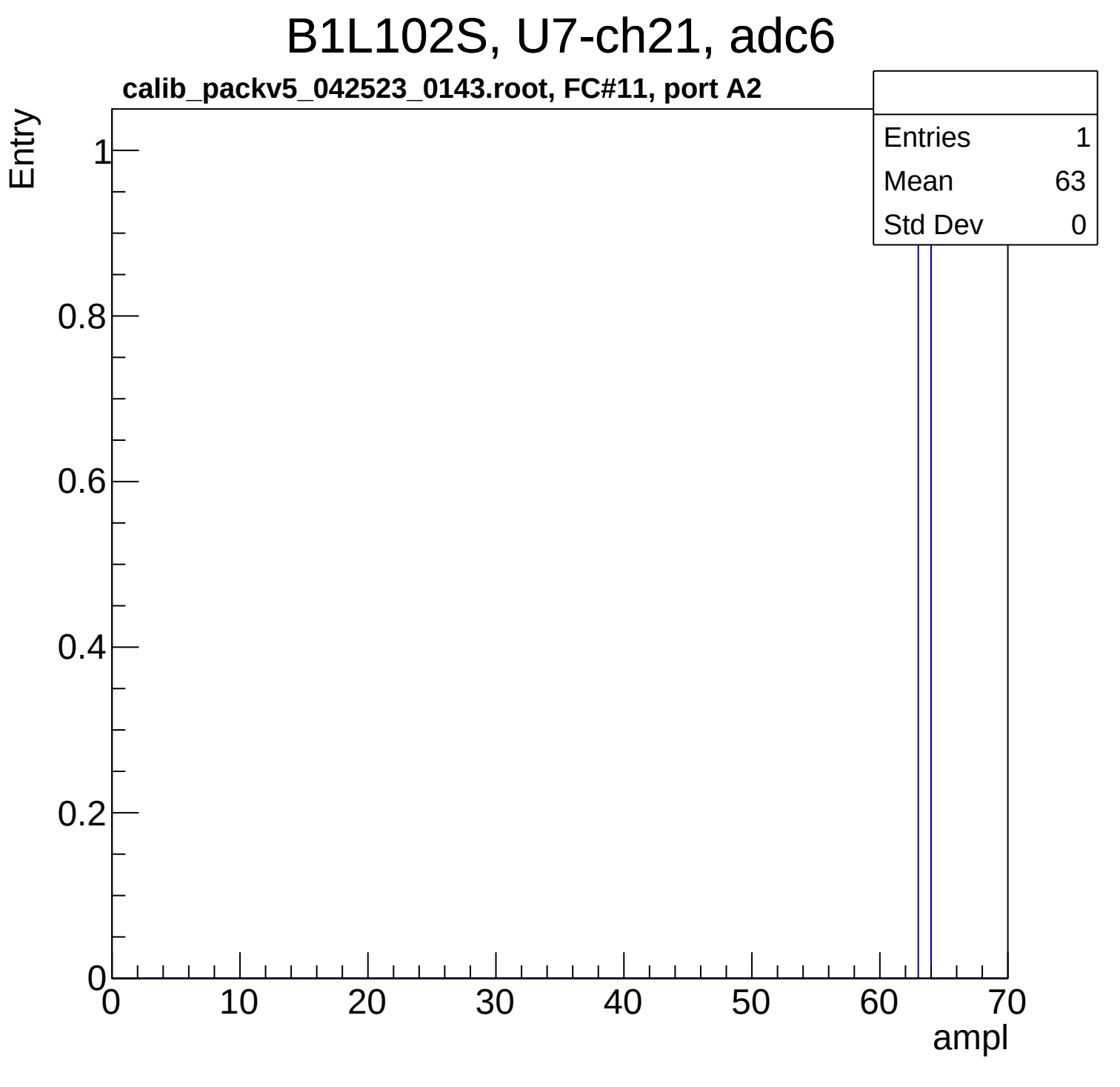
B1L102S, U7-ch21, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 1
Mean 63
Std Dev 0
Entry
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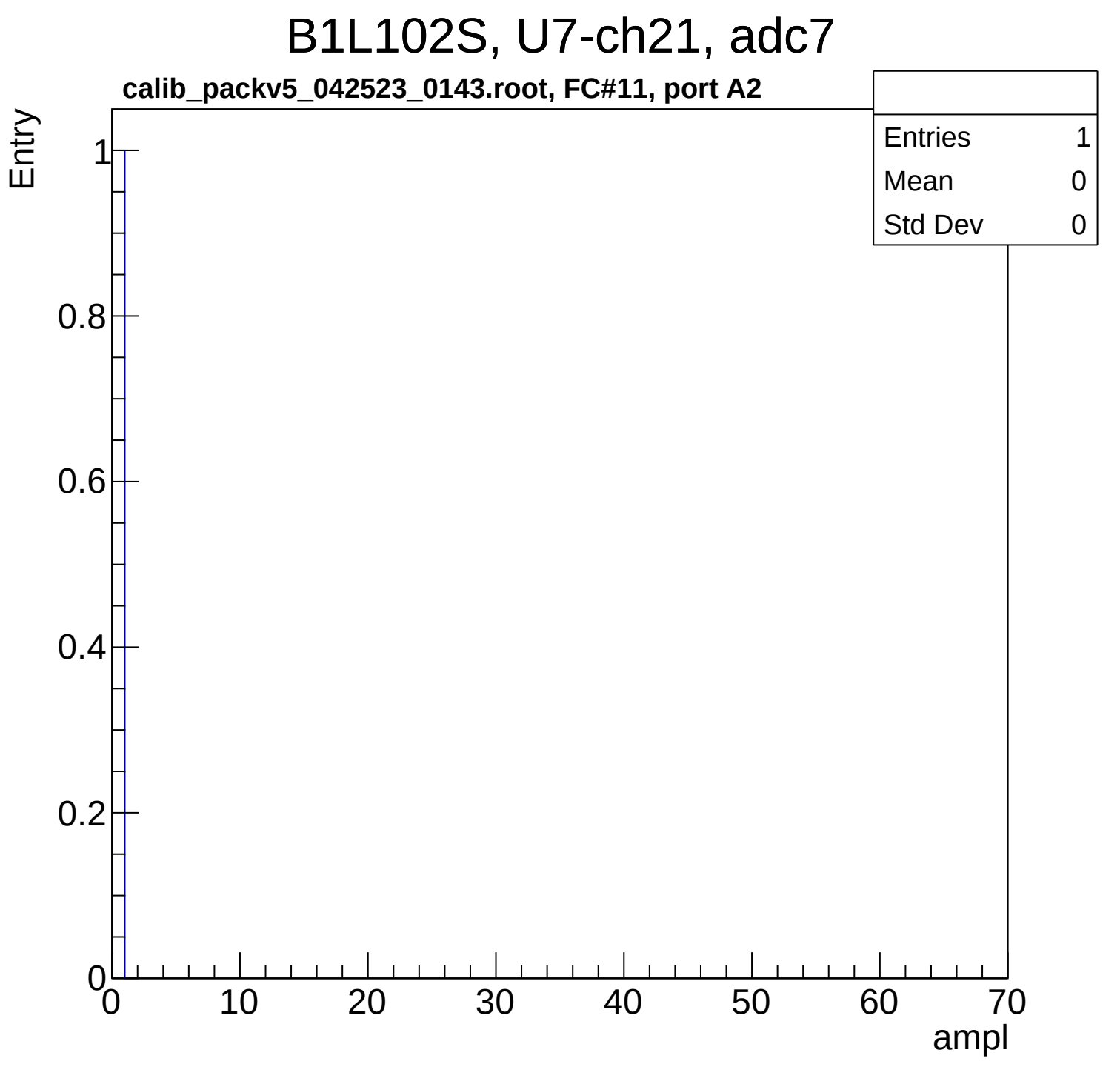
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U7-ch21, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 1
Mean 0
Std Dev 0
Entry
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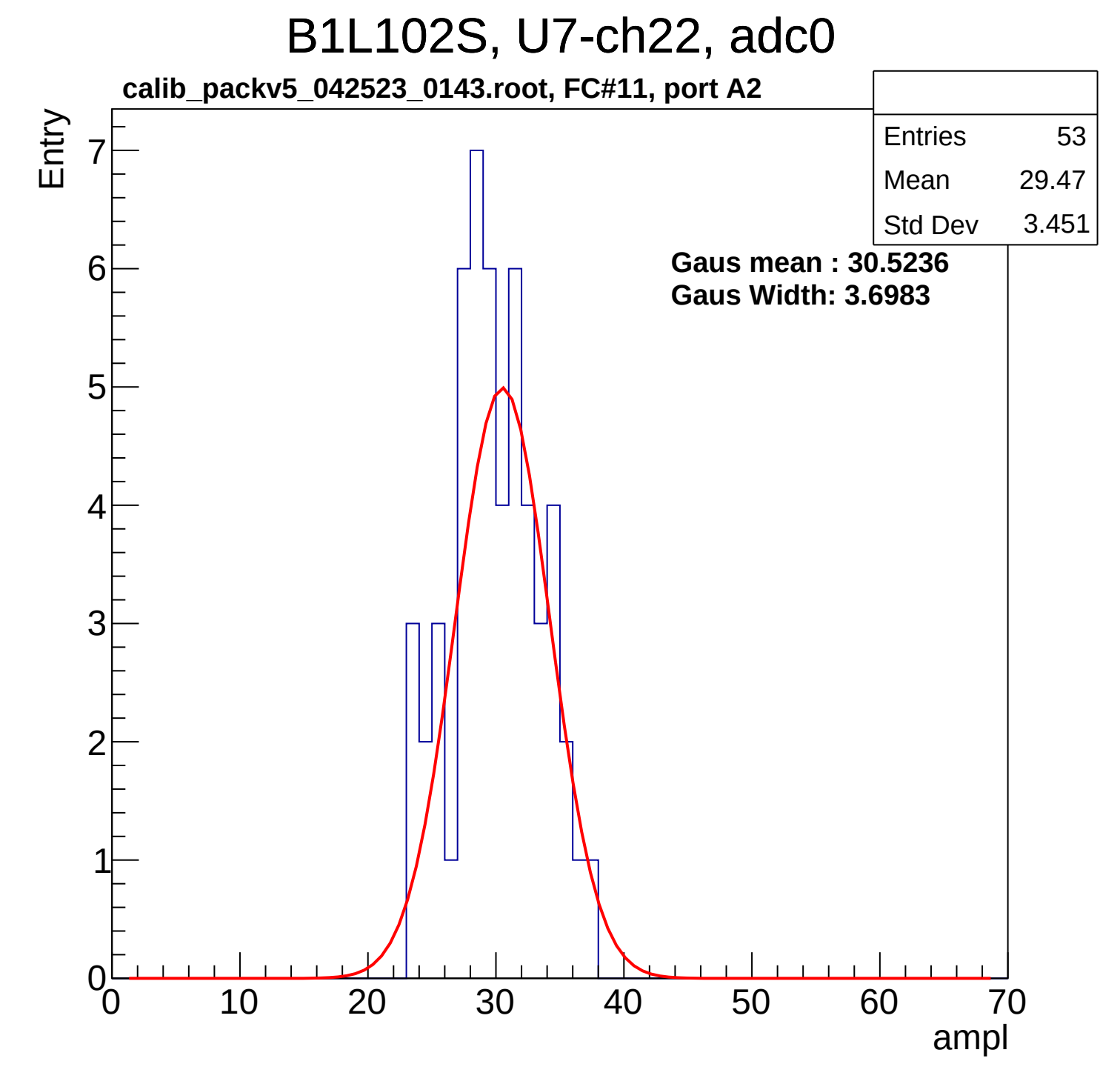
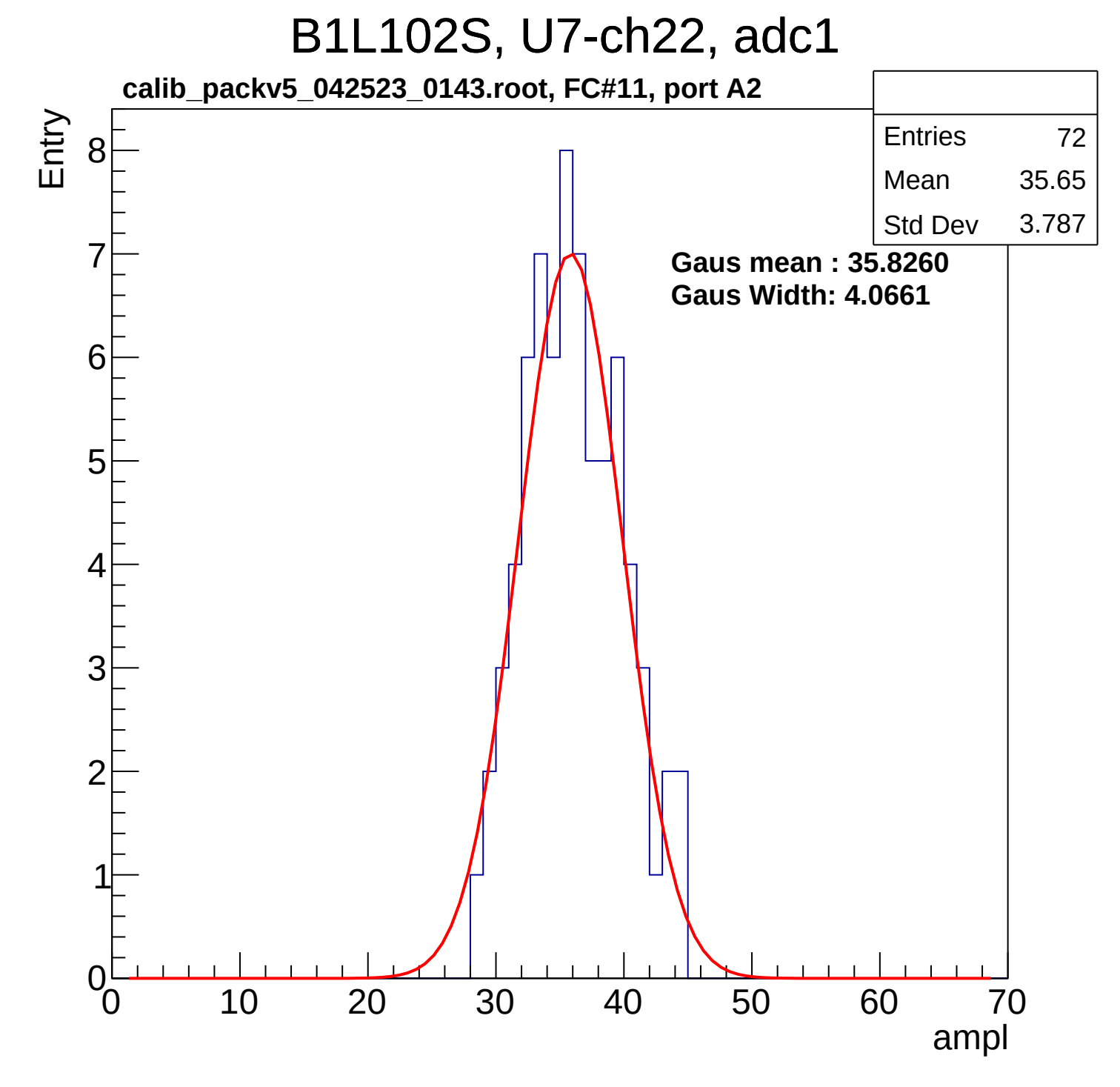
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U7-ch22, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 53
Mean 29.47
Std Dev 3.451
Gaus mean : 30.5236
Gaus Width: 3.6983
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L102S, U7-ch22, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 72
Mean 35.65
Std Dev 3.787
Gaus mean : 35.8260
Gaus Width: 4.0661
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
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60
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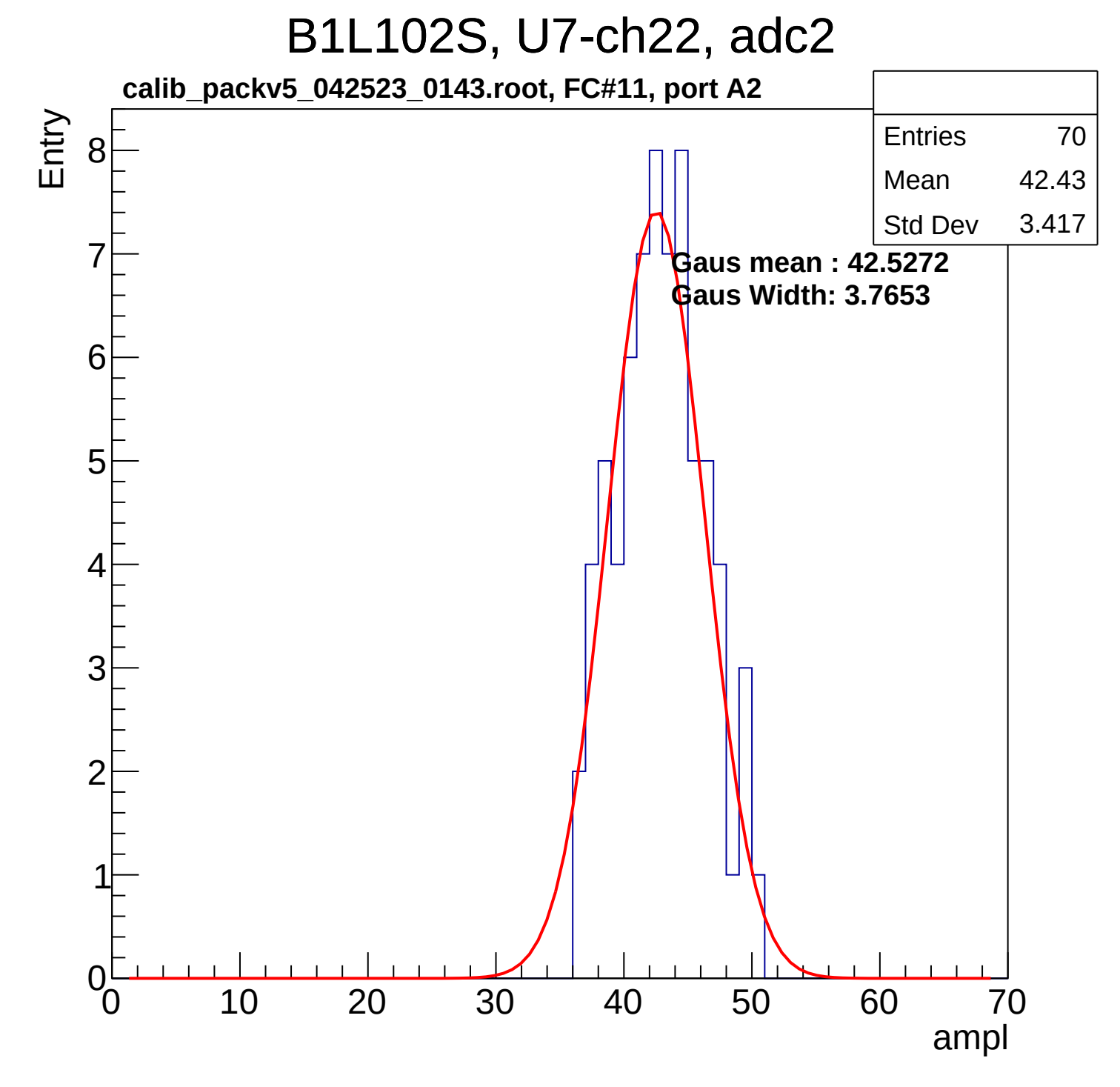
B1L102S, U7-ch22, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 70
Mean 42.43
Std Dev 3.417
Gaus mean : 42.5272
Gaus Width: 3.7653
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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60
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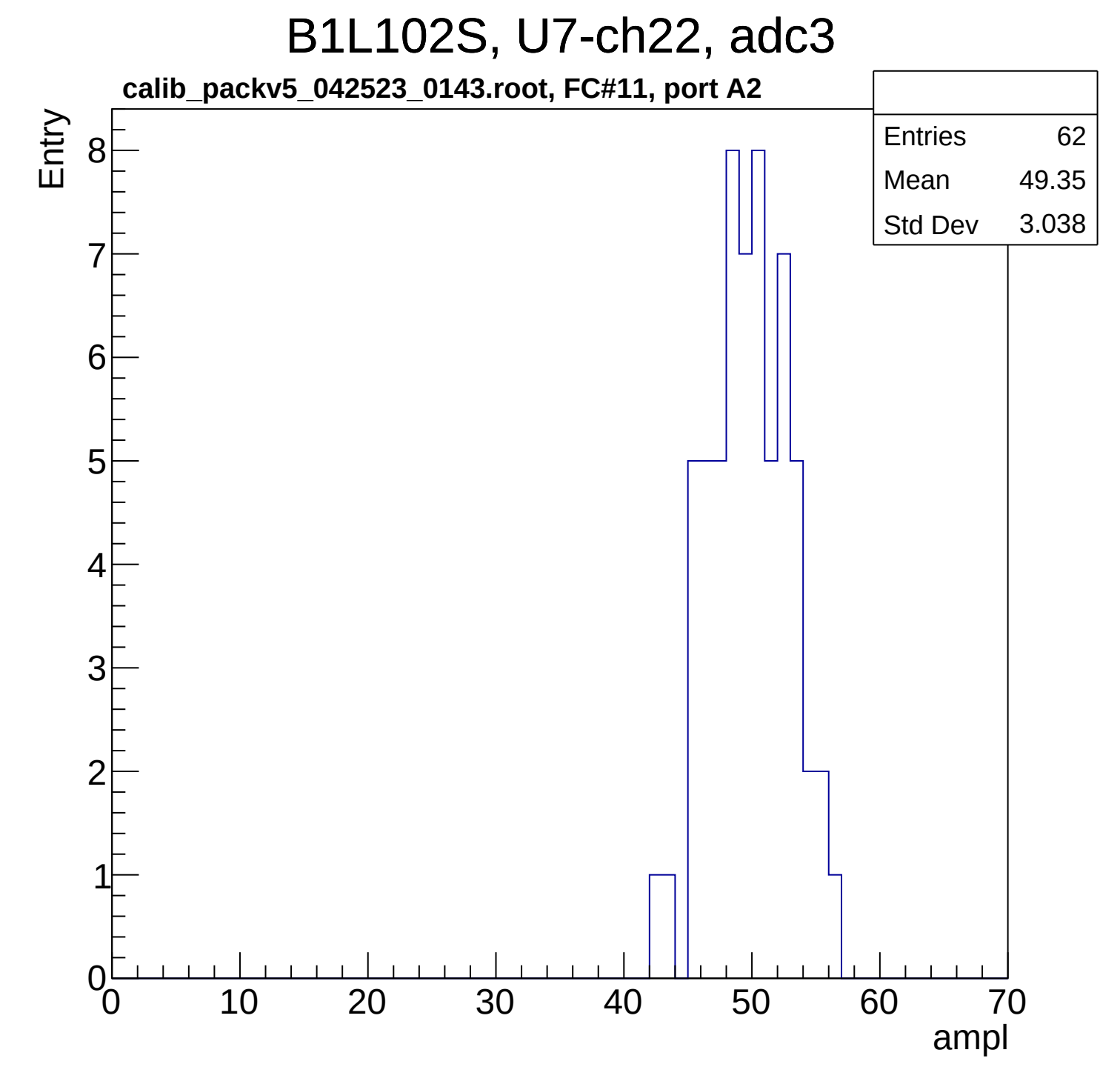
B1L102S, U7-ch22, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 62
Mean 49.35
Std Dev 3.038
Entry
ampl
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3
4
5
6
7
8
0
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20
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40
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60
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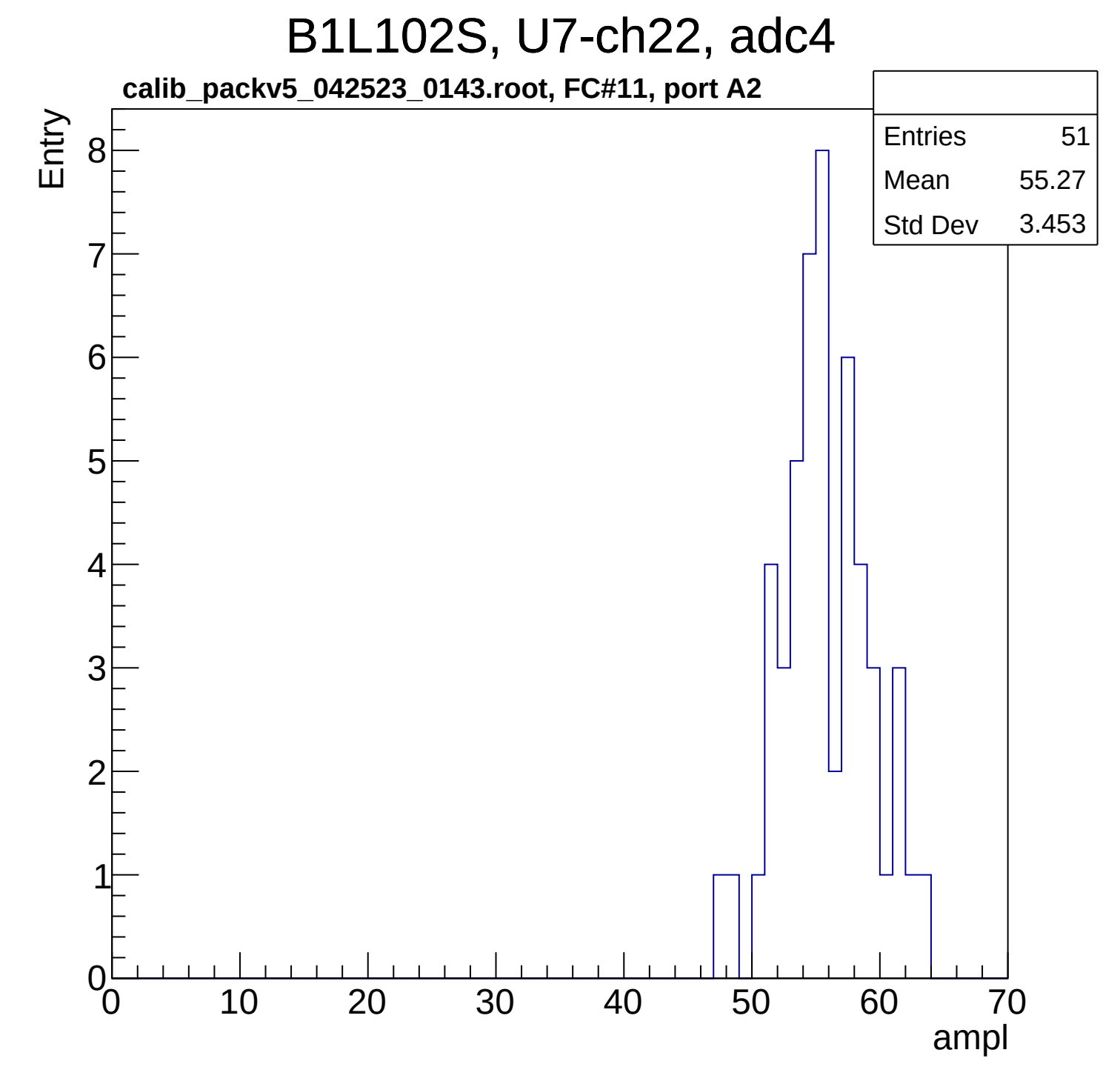
B1L102S, U7-ch22, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 51
Mean 55.27
Std Dev 3.453
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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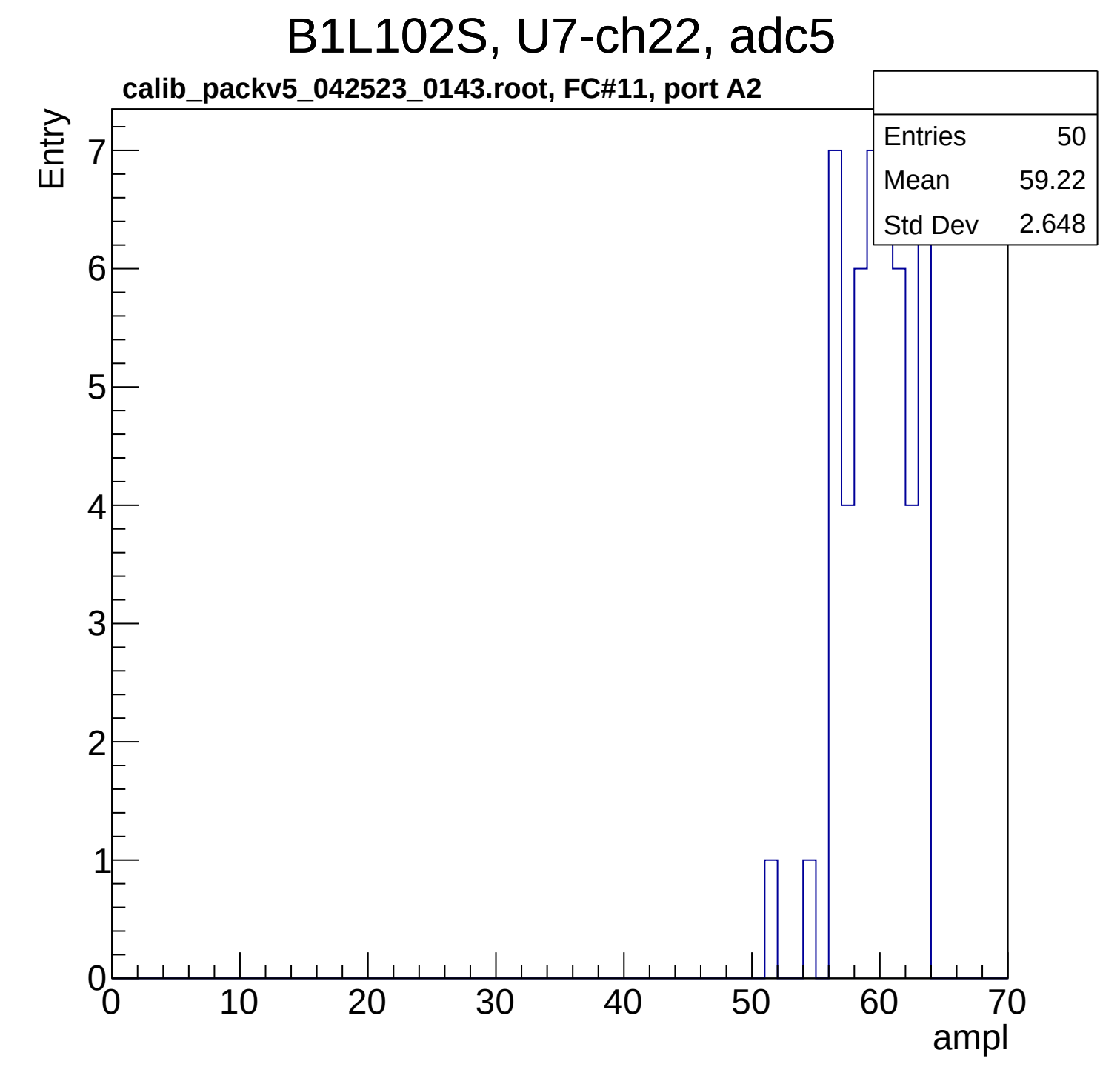
B1L102S, U7-ch22, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 50
Mean 59.22
Std Dev 2.648
Entry
ampl
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4
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7
0
10
20
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40
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60
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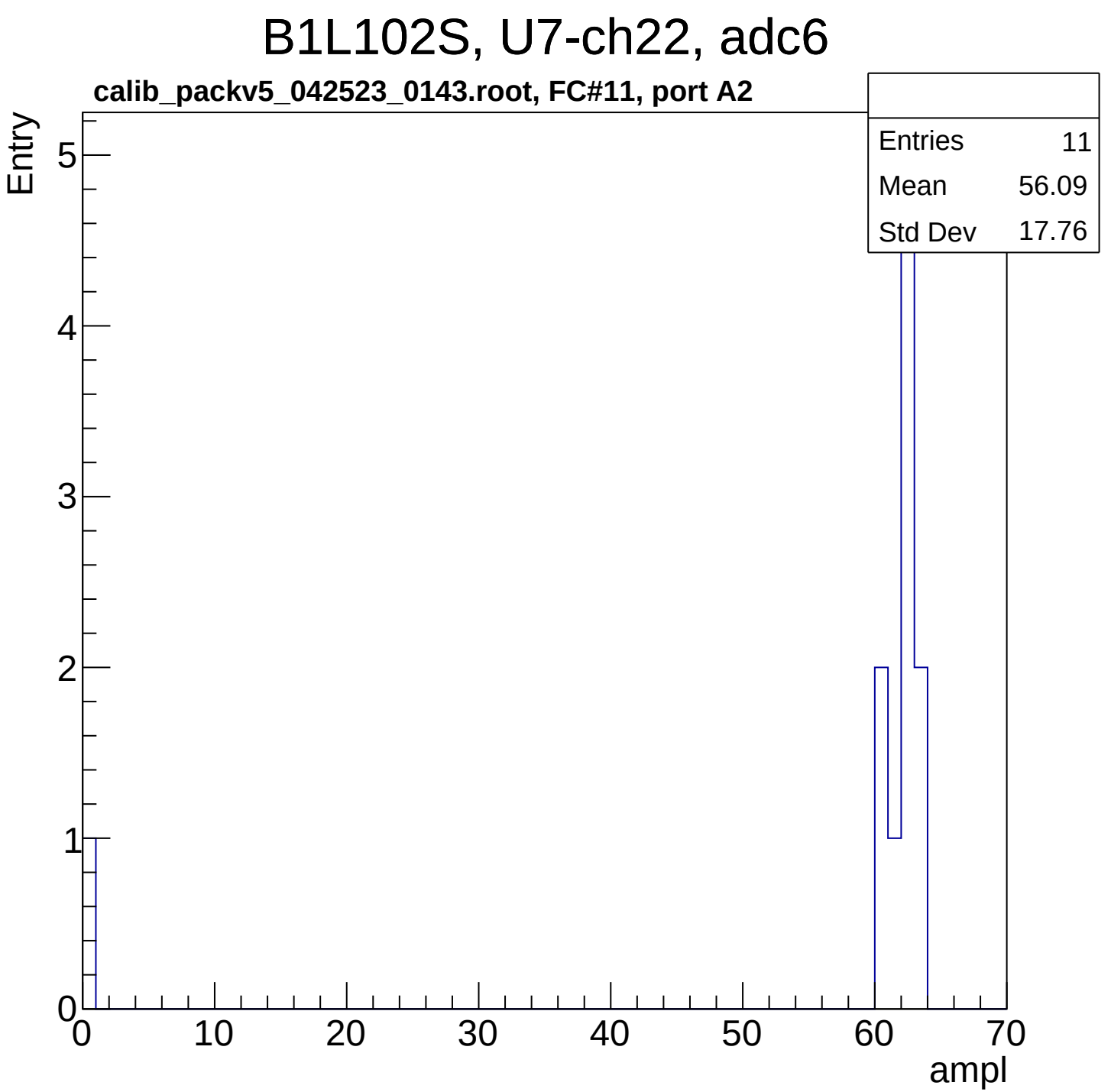
B1L102S, U7-ch22, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 11
Mean 56.09
Std Dev 17.76
Entry
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4
5
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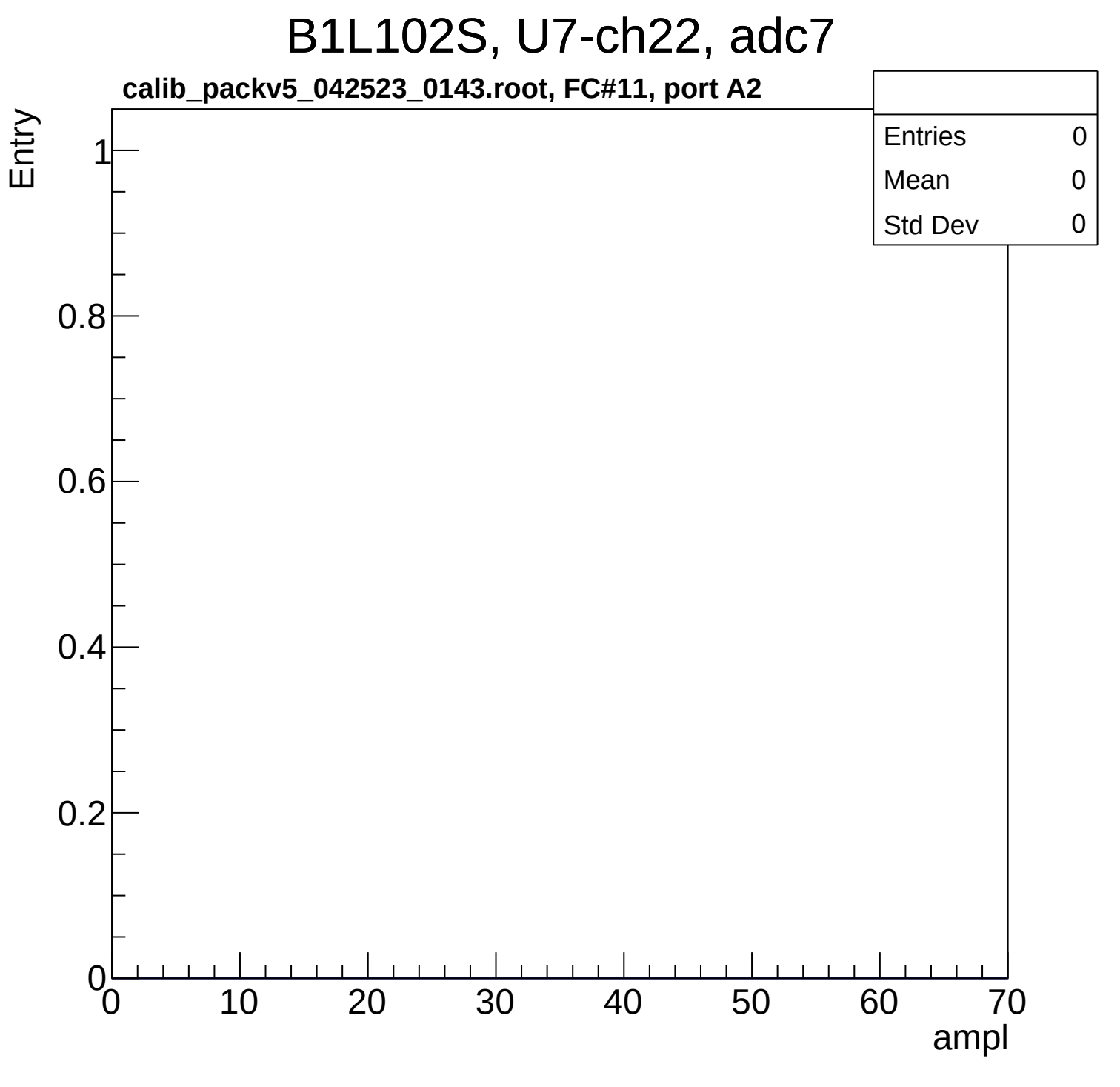
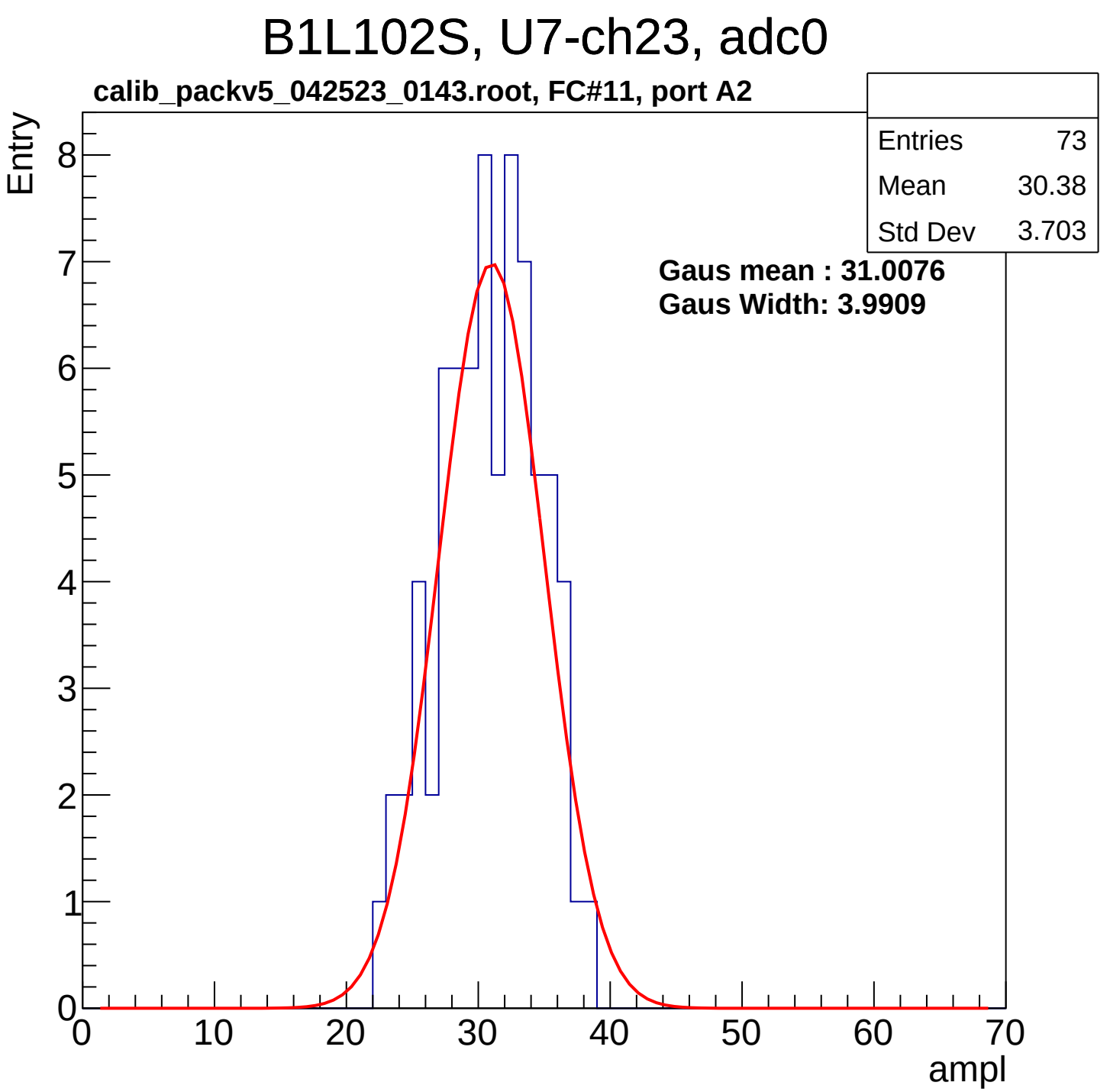
10
20
30
40
50
60
70
ampl


B1L102S, U7-ch22, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U7-ch23, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 73
Mean 30.38
Std Dev 3.703
Gaus mean : 31.0076
Gaus Width: 3.9909
Entry
ampl
0
1
2
3
4
5
6
7
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0
10
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60
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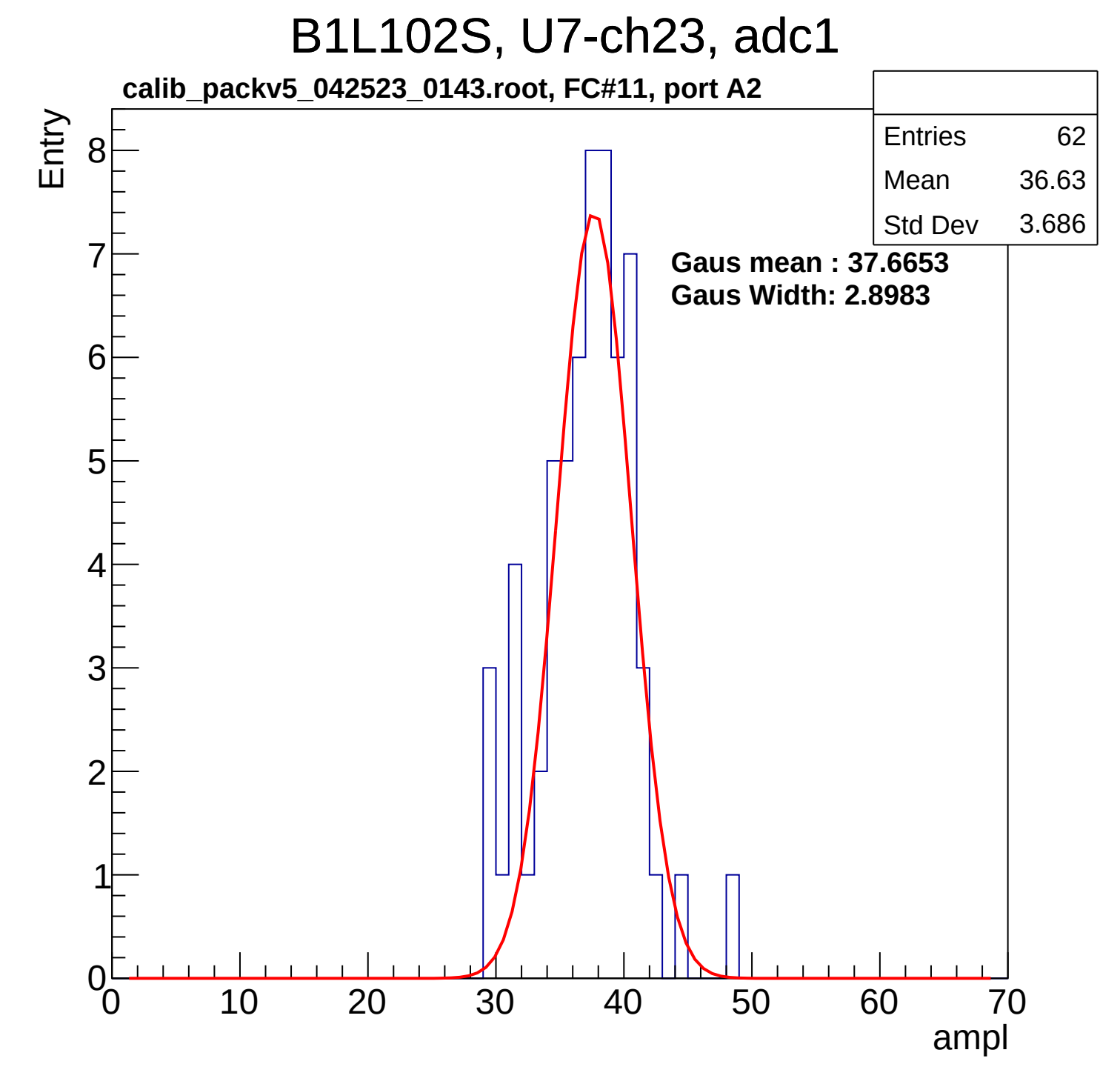
B1L102S, U7-ch23, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 62
Mean 36.63
Std Dev 3.686
Gaus mean : 37.6653
Gaus Width: 2.8983
Entry
ampl
0
1
2
3
4
5
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0
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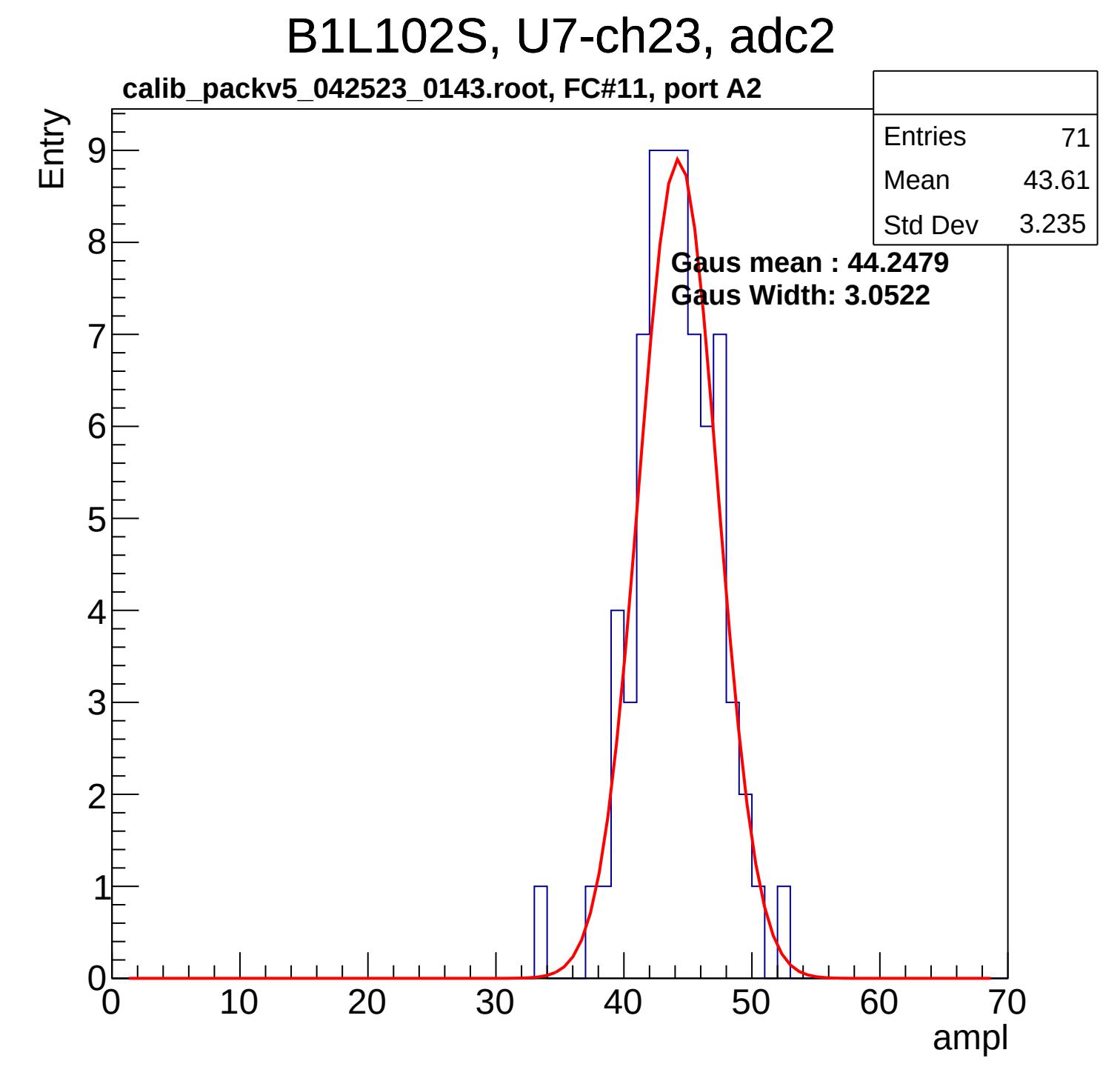
B1L102S, U7-ch23, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 71
Mean 43.61
Std Dev 3.235
Gaus mean : 44.2479
Gaus Width: 3.0522
Entry
ampl
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2
3
4
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6
7
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0
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60
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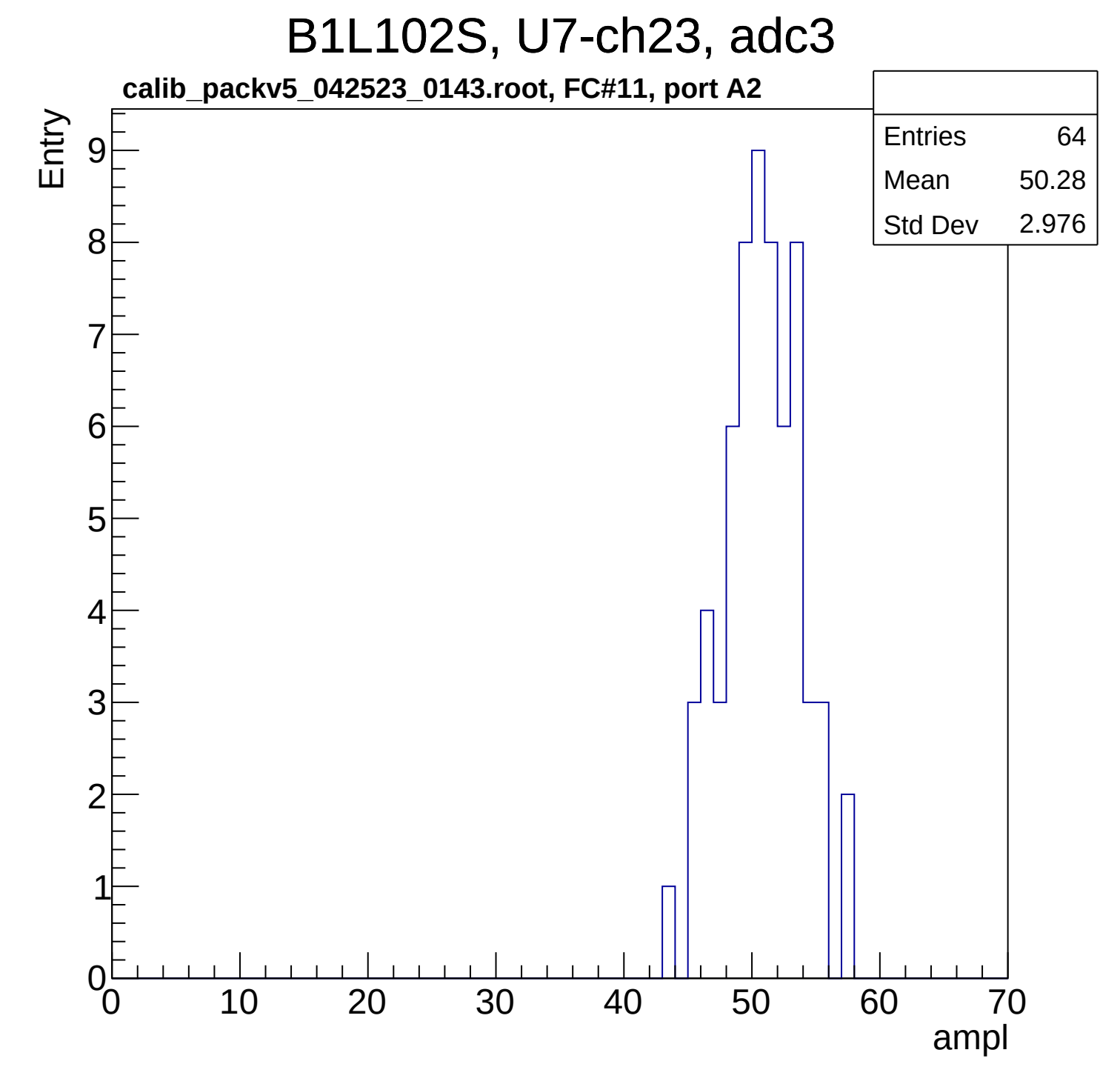
B1L102S, U7-ch23, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 64
Mean 50.28
Std Dev 2.976
Entry
ampl
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2
3
4
5
6
7
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0
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50
60
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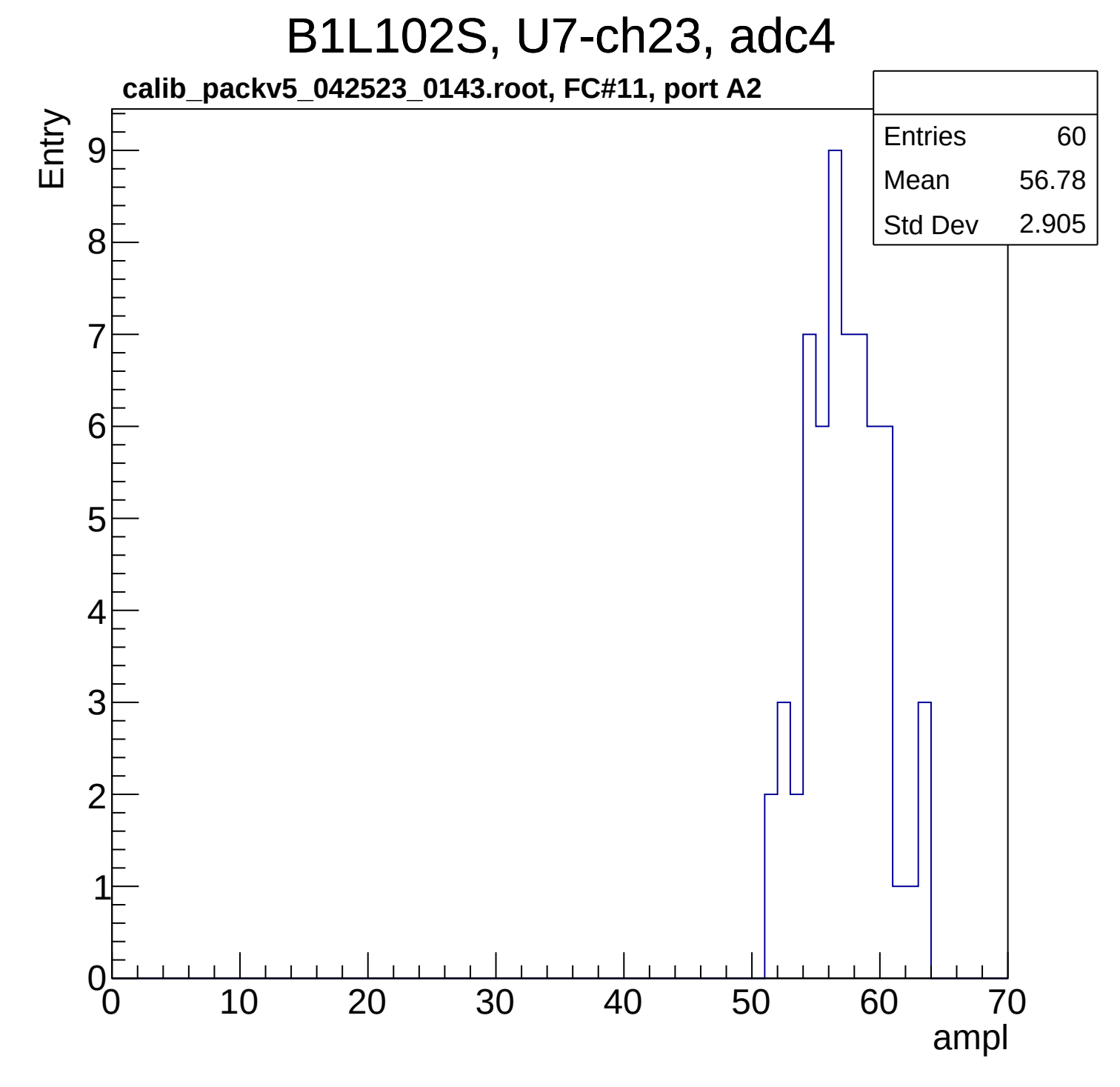
B1L102S, U7-ch23, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 60
Mean 56.78
Std Dev 2.905
Entry
ampl
0
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2
3
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5
6
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0
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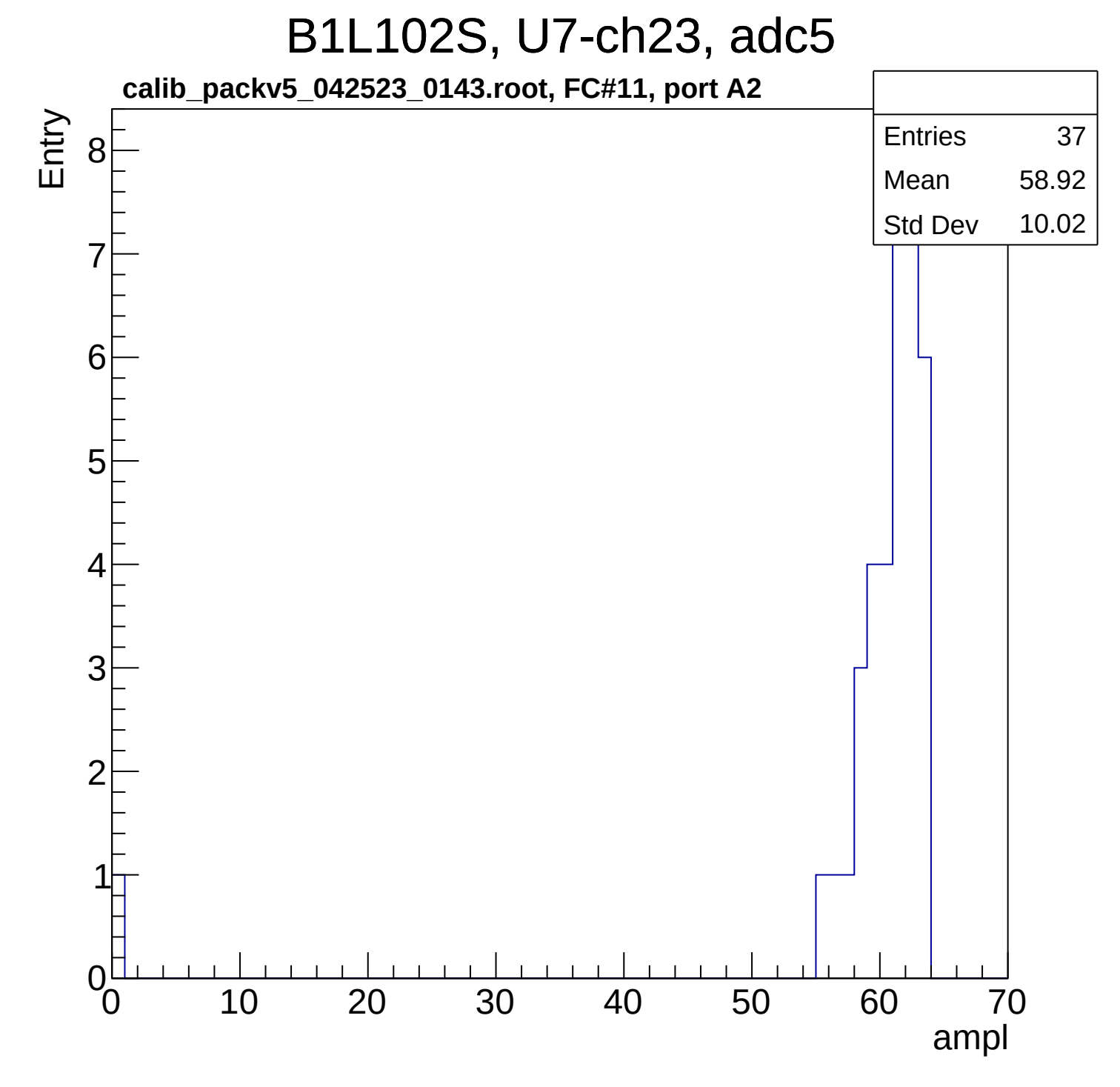
B1L102S, U7-ch23, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 37
Mean 58.92
Std Dev 10.02
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
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40
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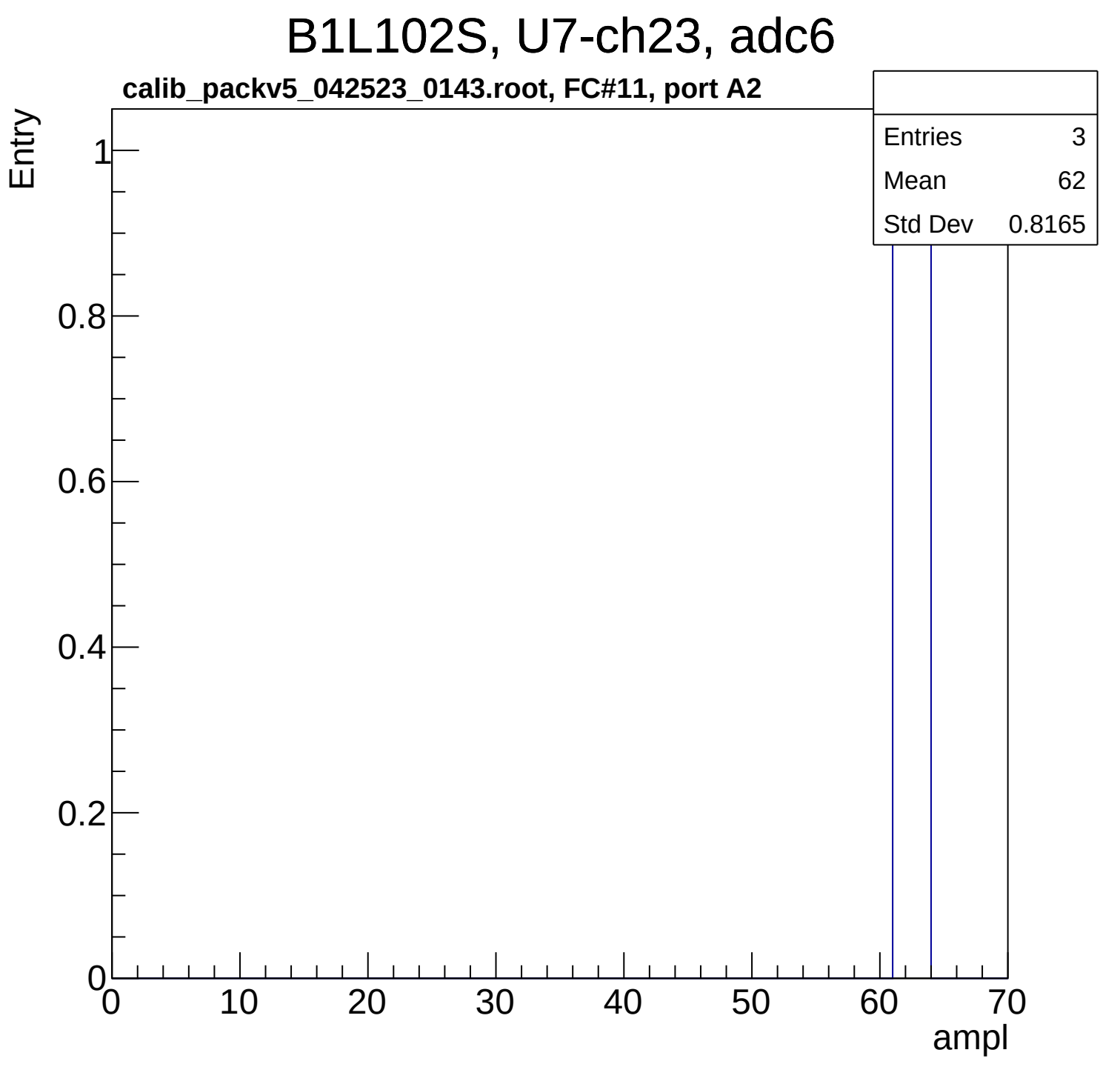
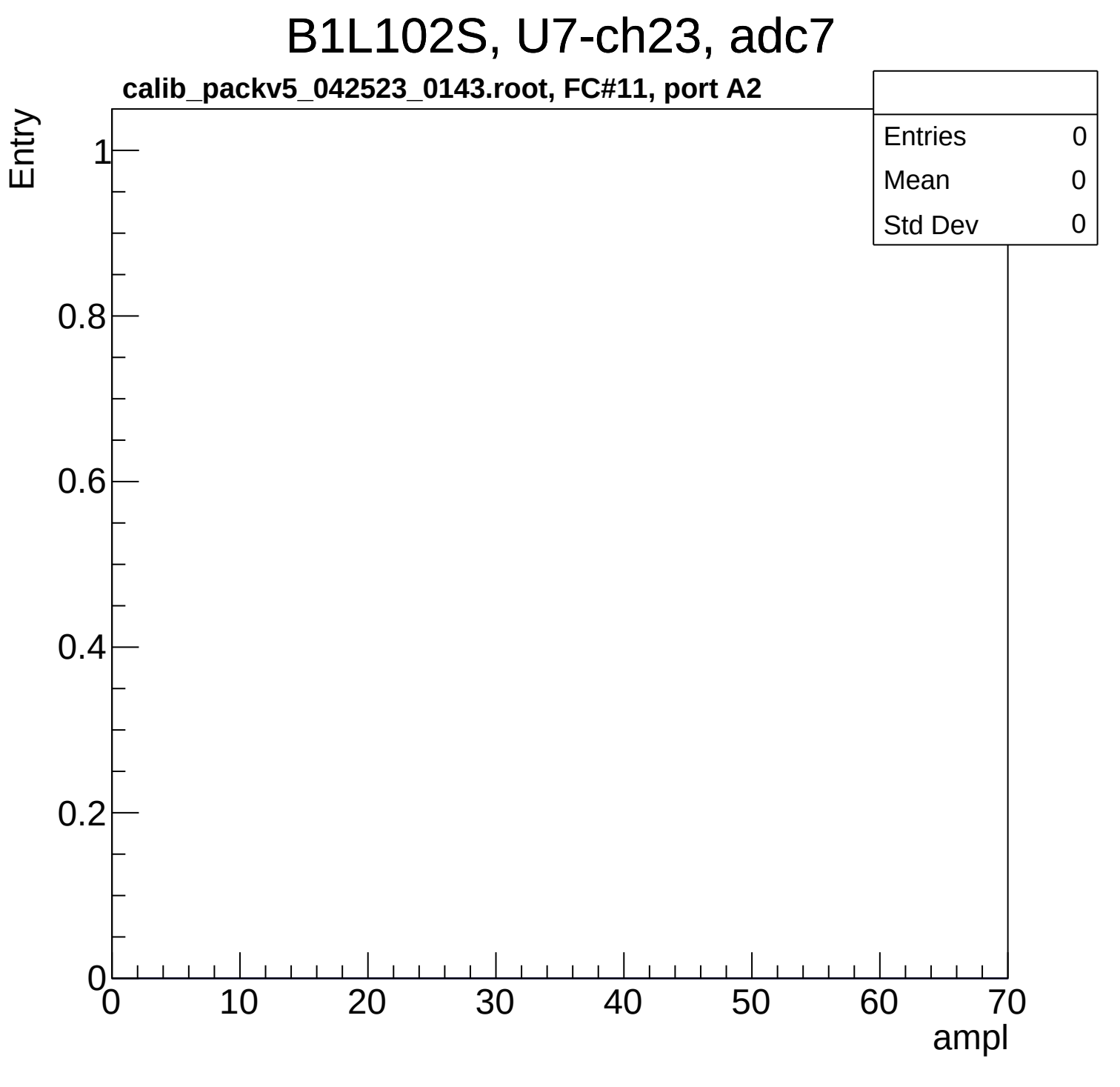
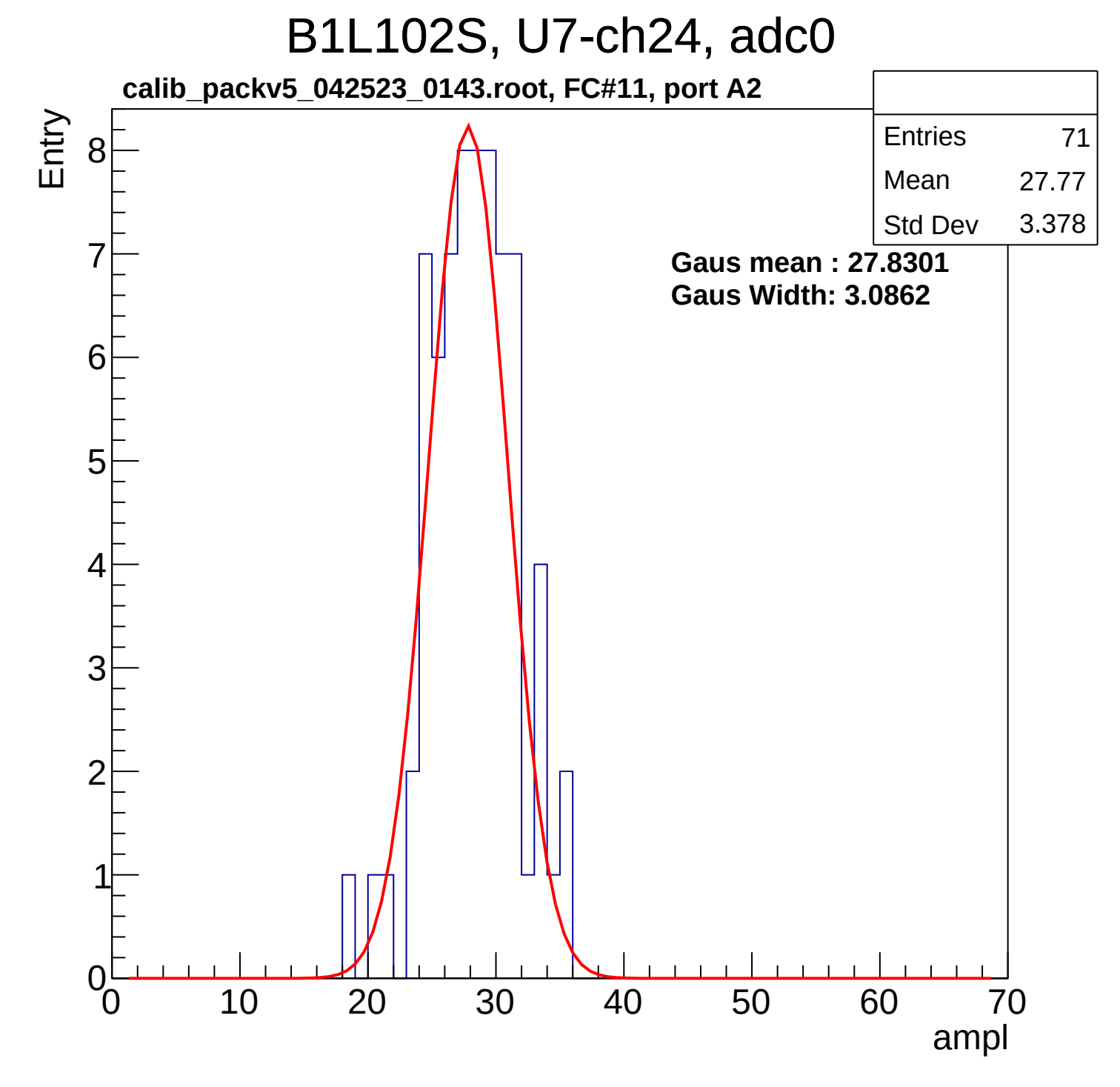
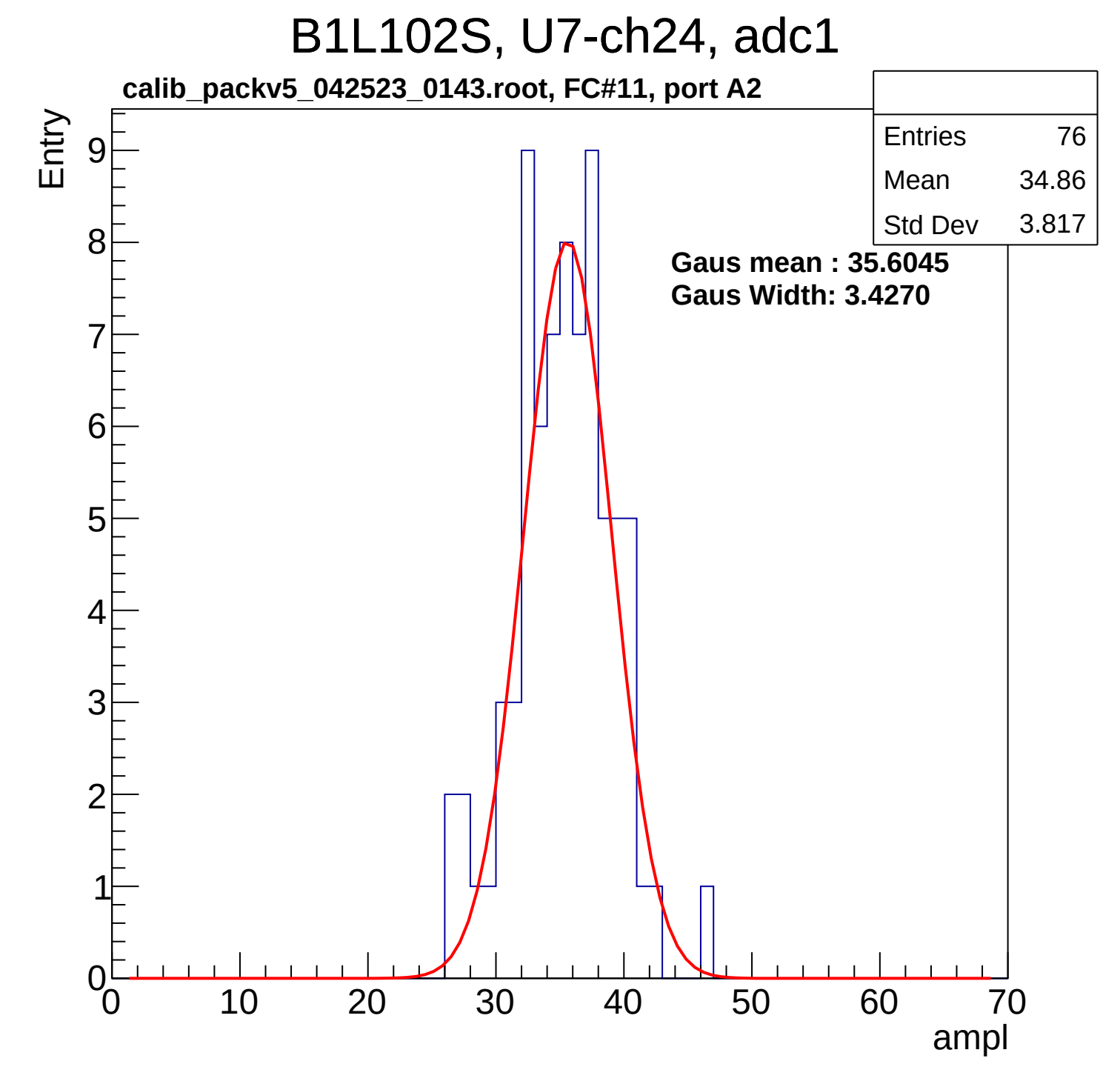

B1L102S, U7-ch23, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 3
Mean 62
Std Dev 0.8165
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U7-ch23, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U7-ch24, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 71
Mean 27.77
Std Dev 3.378
Gaus mean : 27.8301
Gaus Width: 3.0862
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L102S, U7-ch24, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 76
Mean 34.86
Std Dev 3.817
Gaus mean : 35.6045
Gaus Width: 3.4270
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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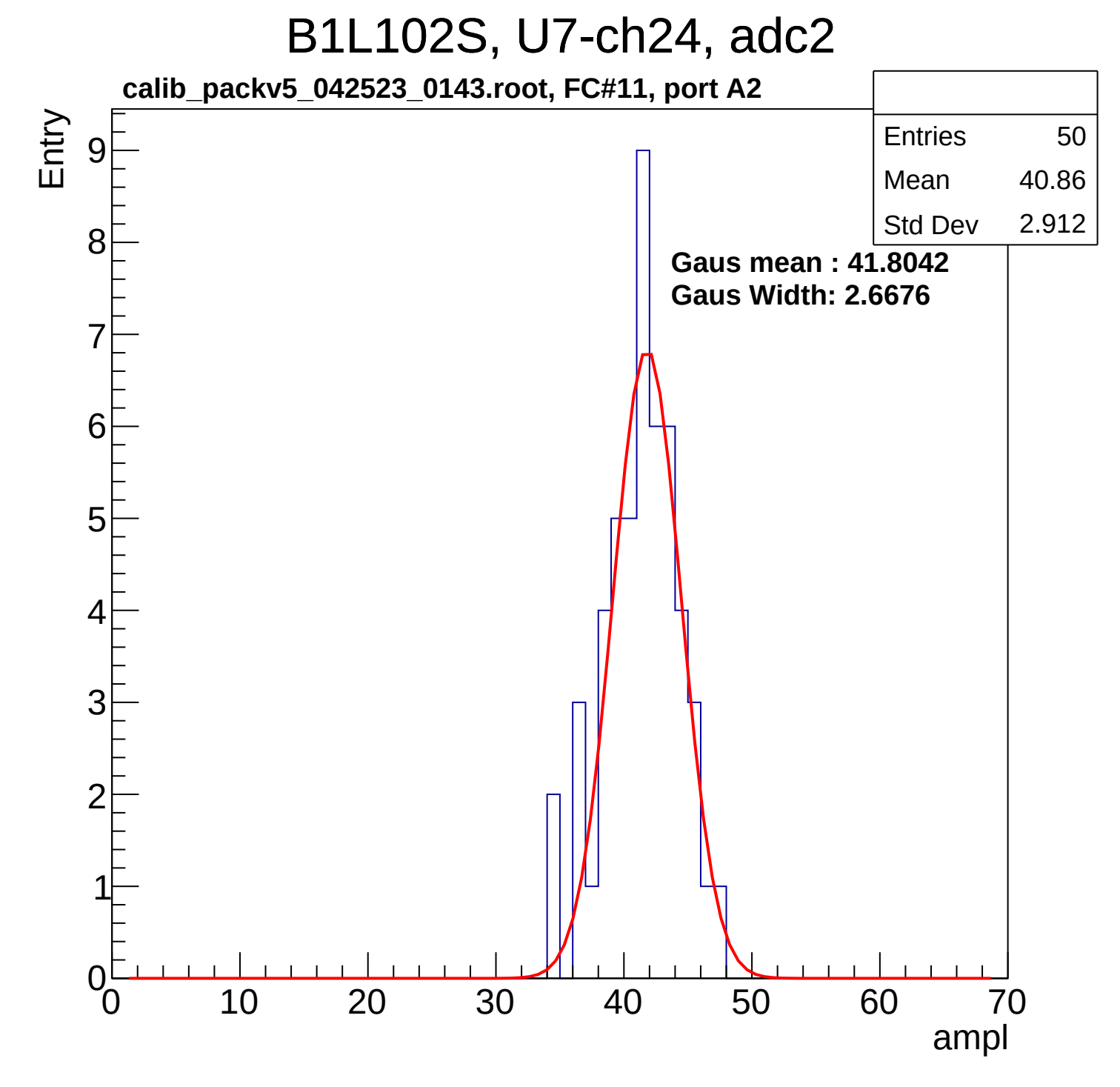
B1L102S, U7-ch24, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 50
Mean 40.86
Std Dev 2.912
Gaus mean : 41.8042
Gaus Width: 2.6676
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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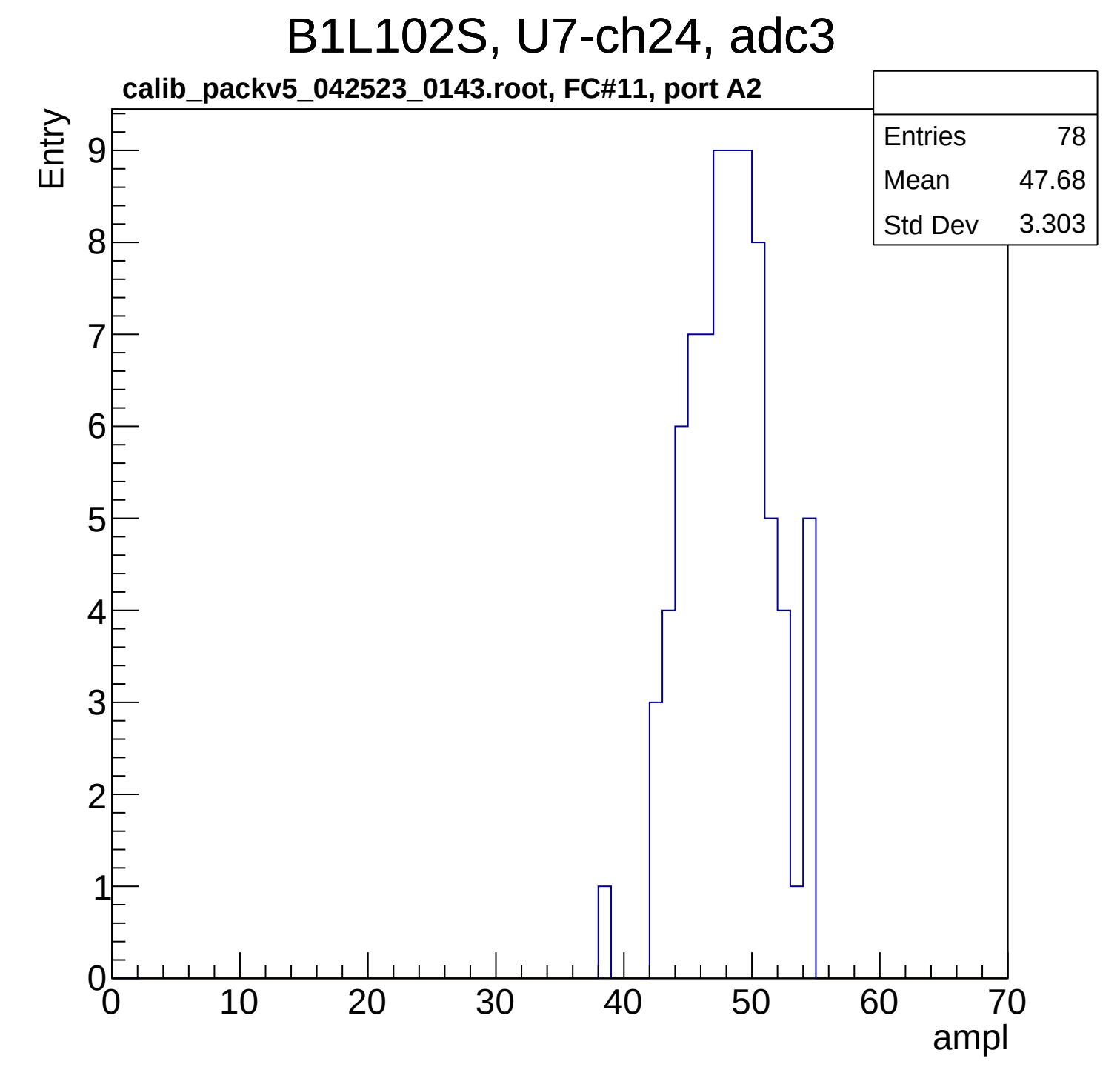
B1L102S, U7-ch24, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 78
Mean 47.68
Std Dev 3.303
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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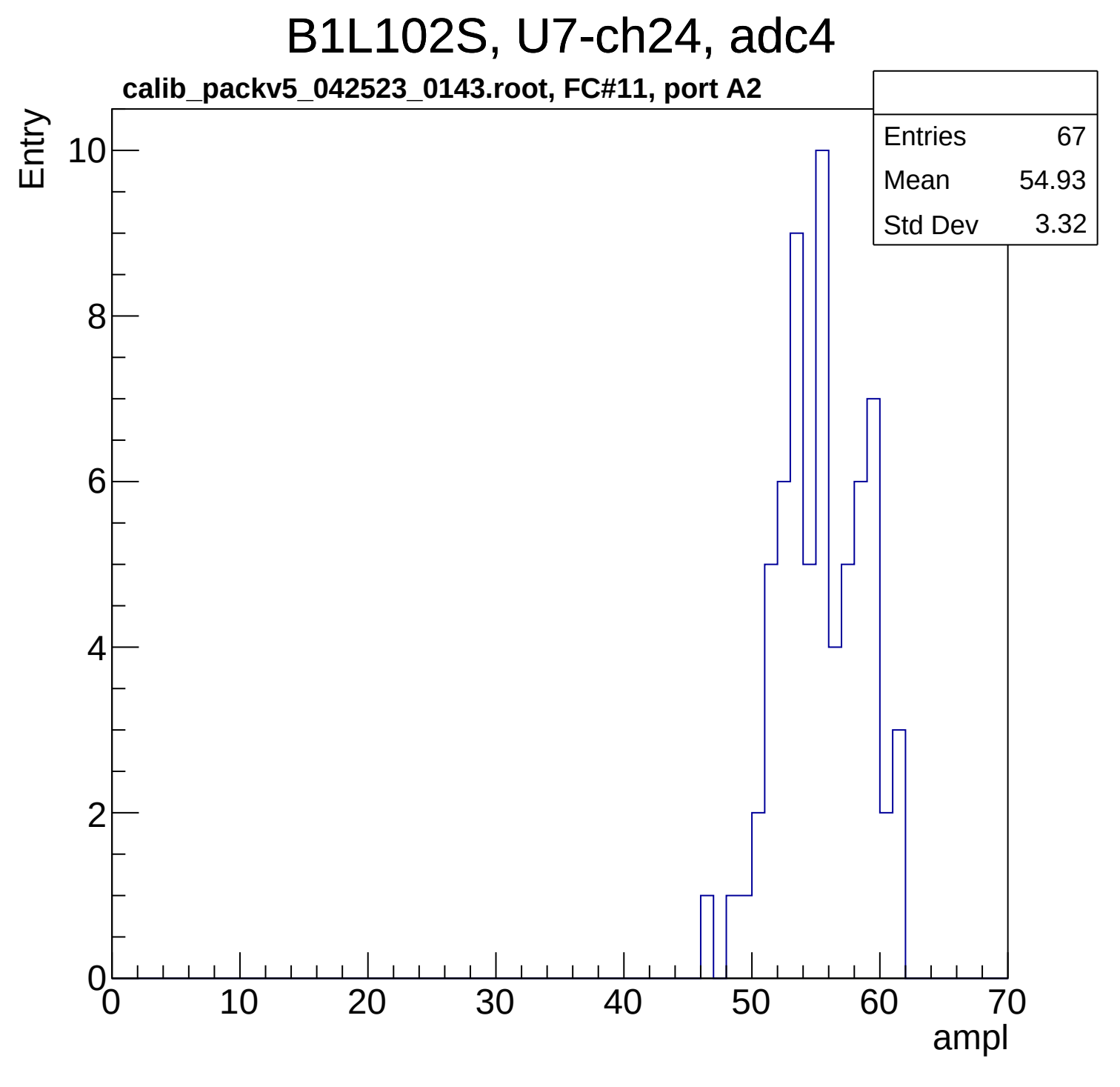
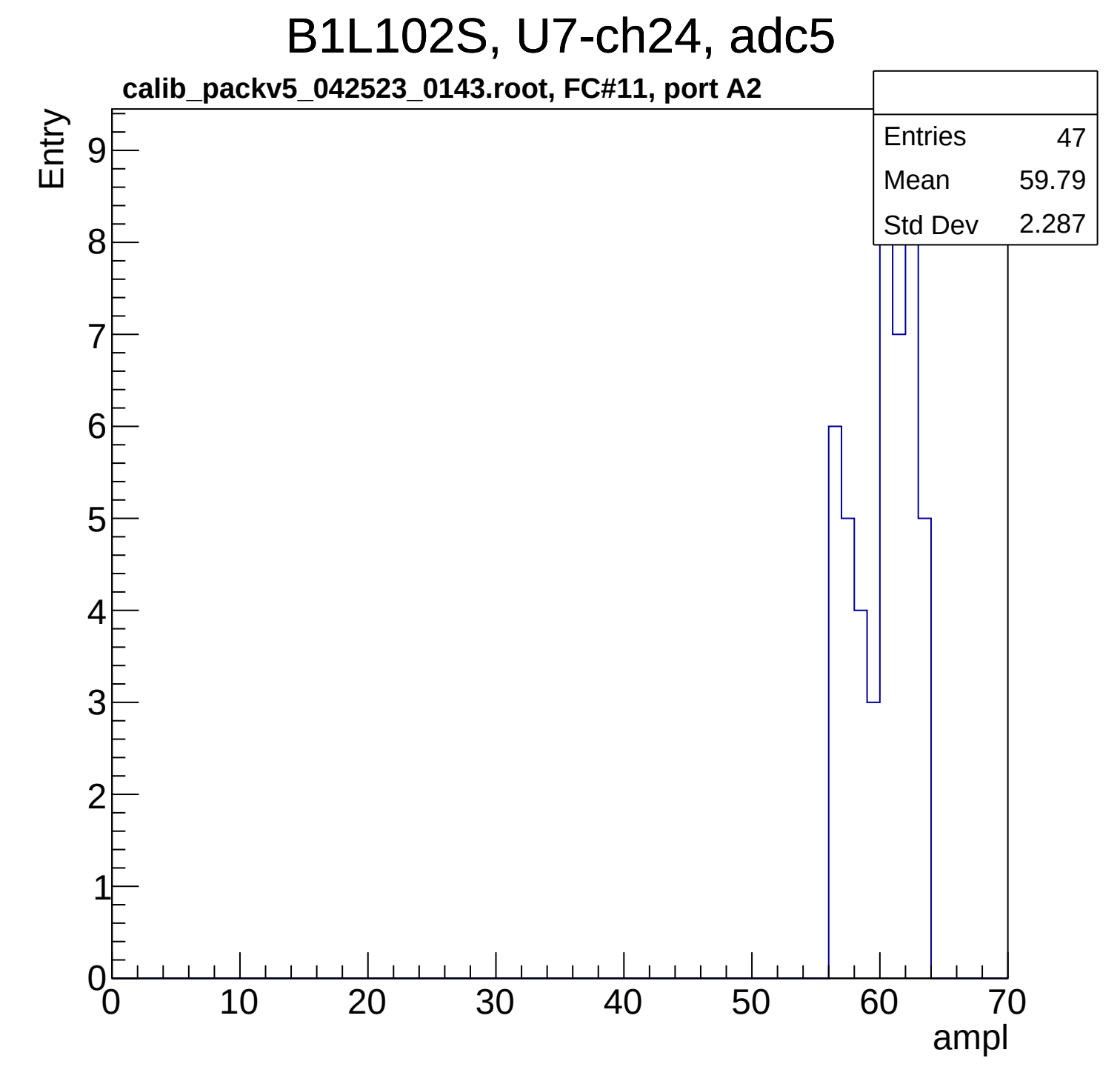
40
50
60
70


B1L102S, U7-ch24, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 67
Mean 54.93
Std Dev 3.32
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L102S, U7-ch24, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 47
Mean 59.79
Std Dev 2.287
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
50
60
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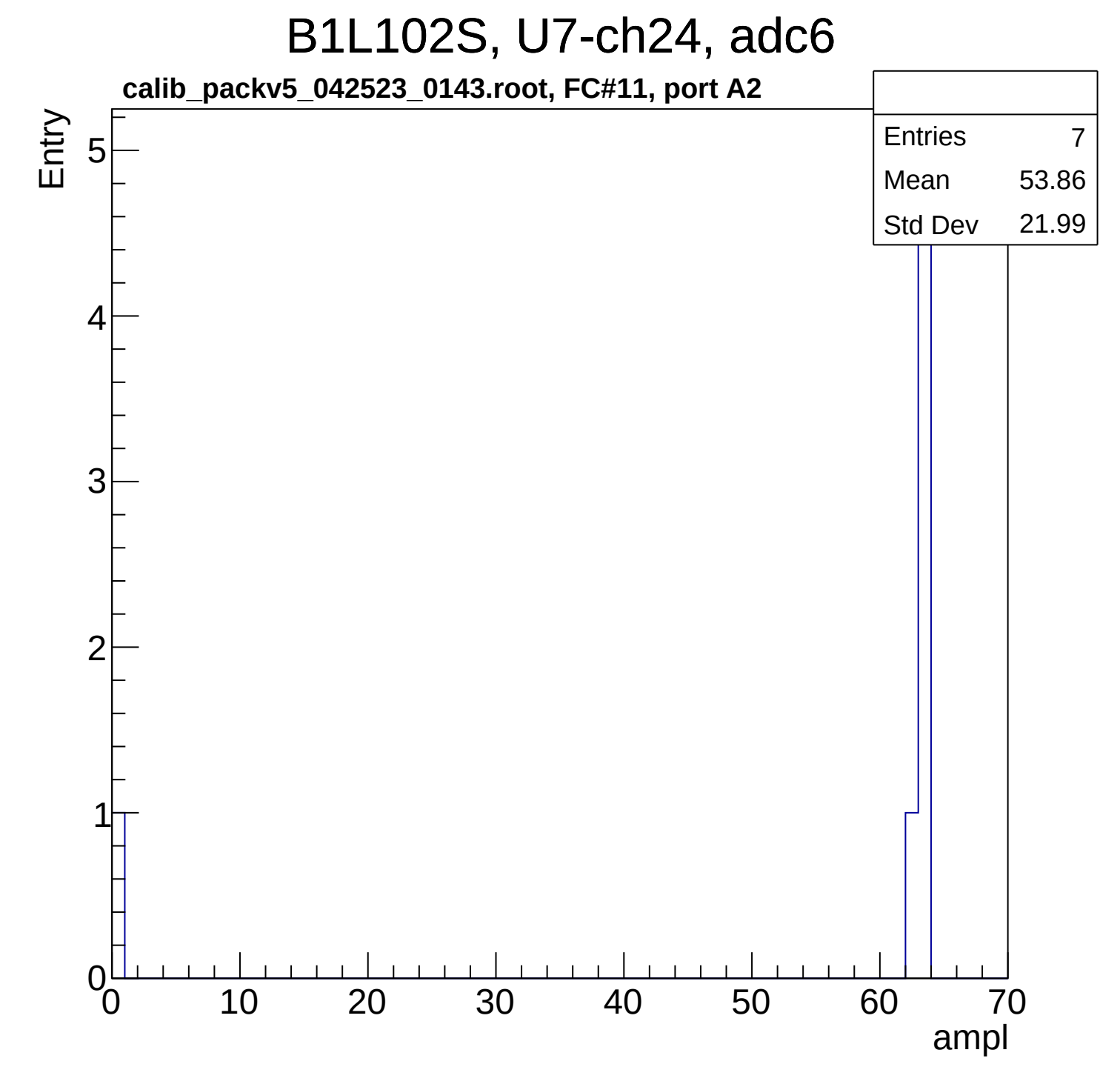
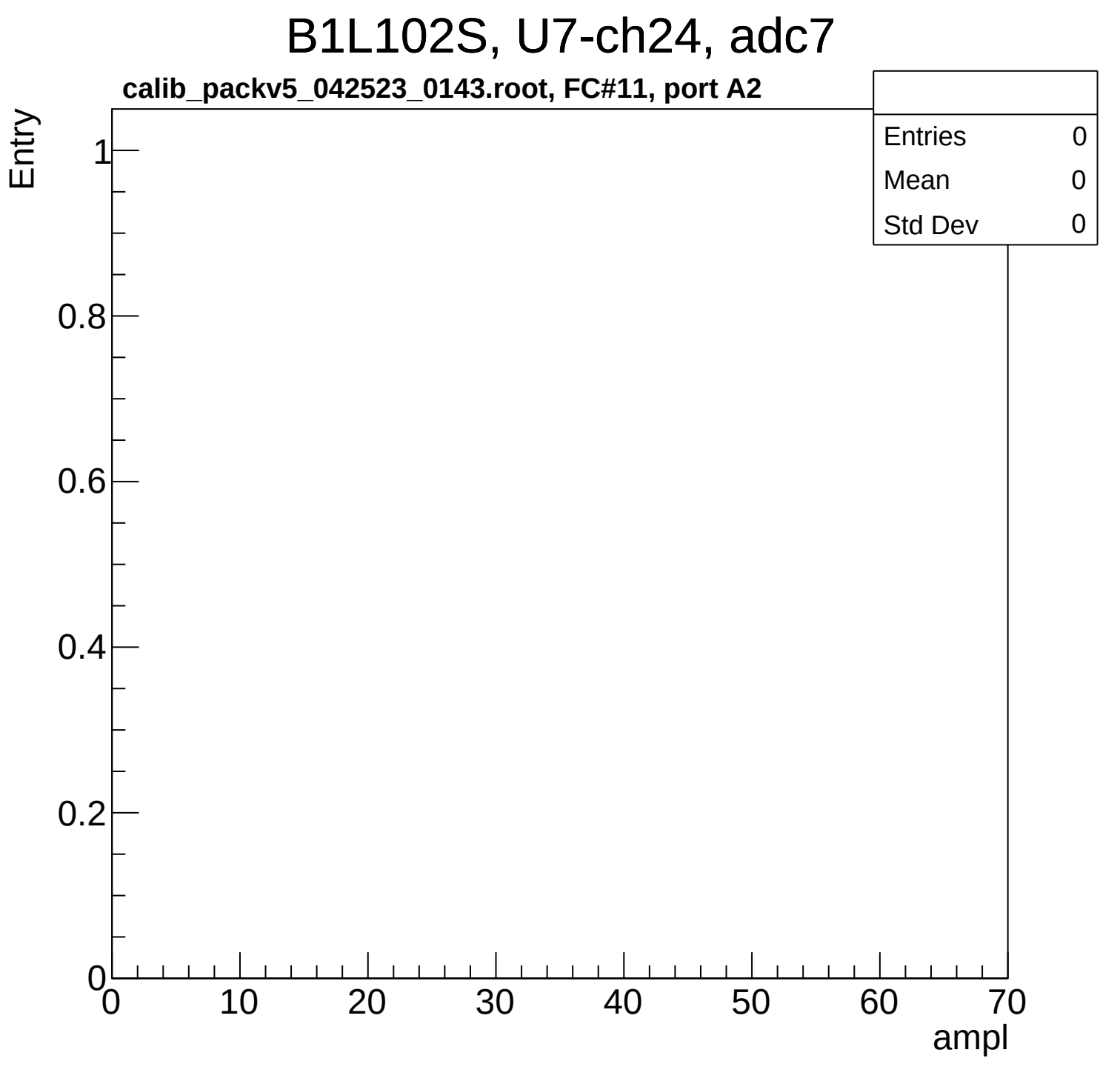
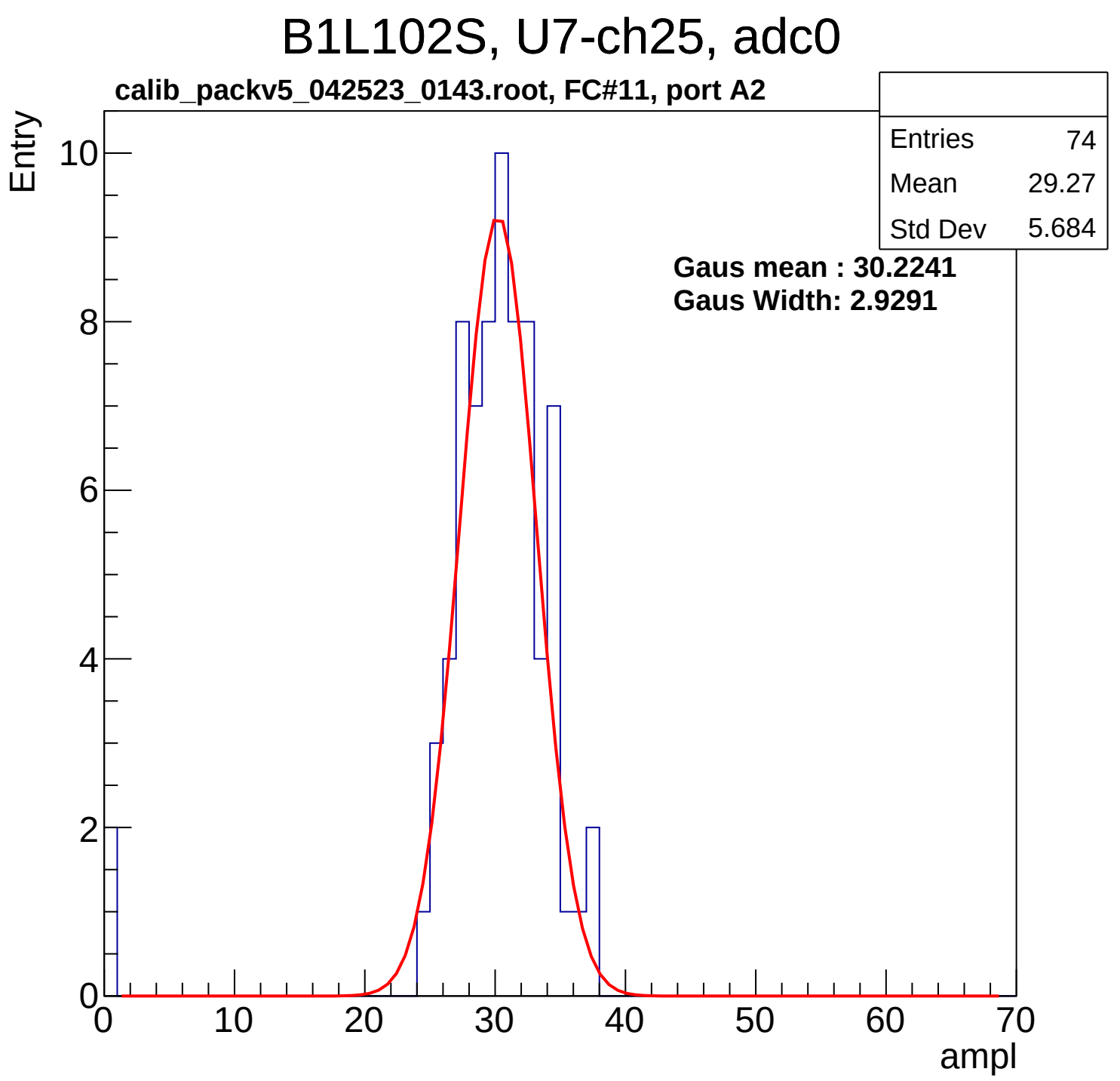
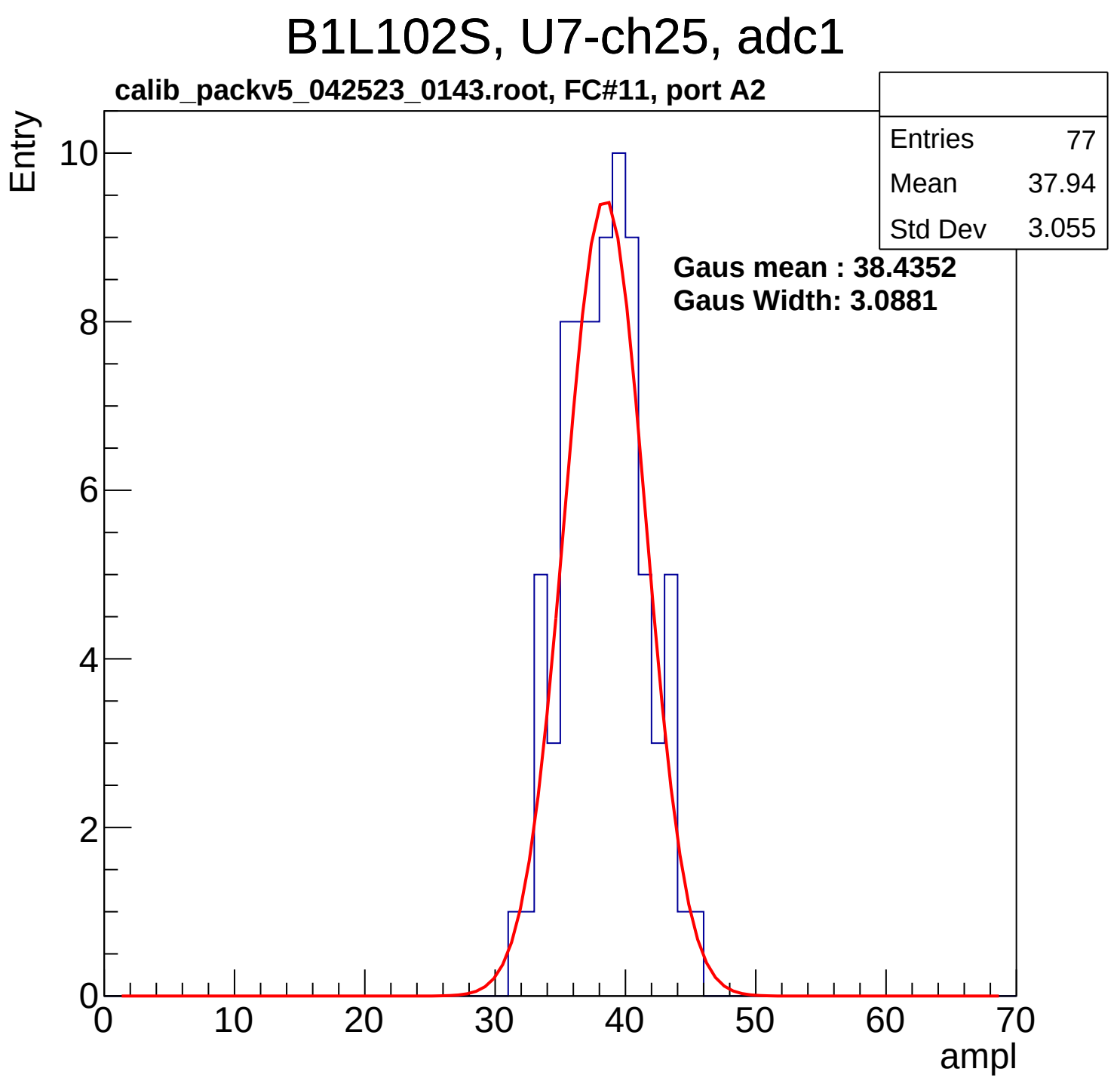
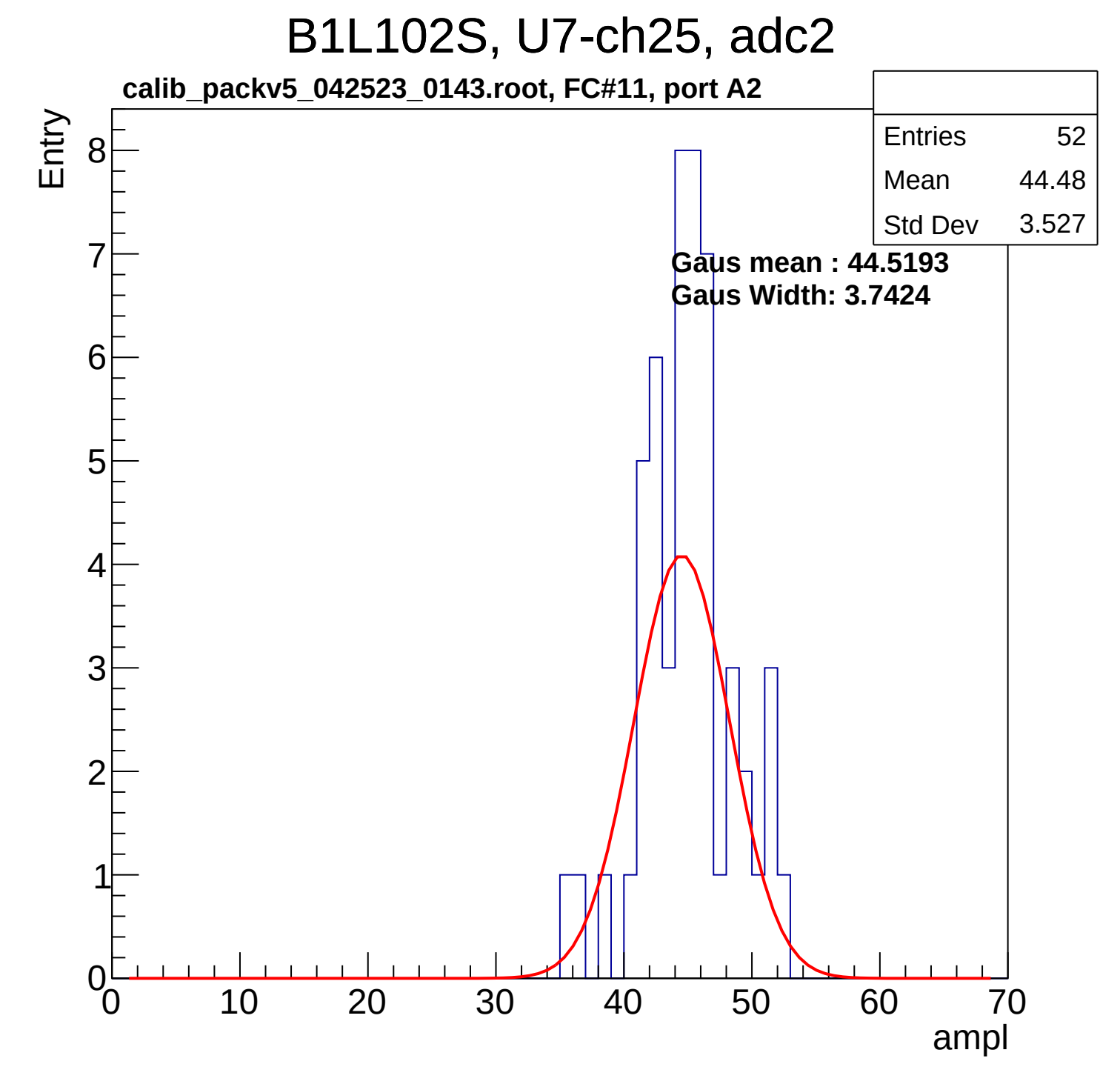

B1L102S, U7-ch24, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 7
Mean 53.86
Std Dev 21.99
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L102S, U7-ch24, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U7-ch25, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 74
Mean 29.27
Std Dev 5.684
Gaus mean : 30.2241
Gaus Width: 2.9291
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L102S, U7-ch25, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 77
Mean 37.94
Std Dev 3.055
Gaus mean : 38.4352
Gaus Width: 3.0881
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L102S, U7-ch25, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 52
Mean 44.48
Std Dev 3.527
Gaus mean : 44.5193
Gaus Width: 3.7424
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
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60
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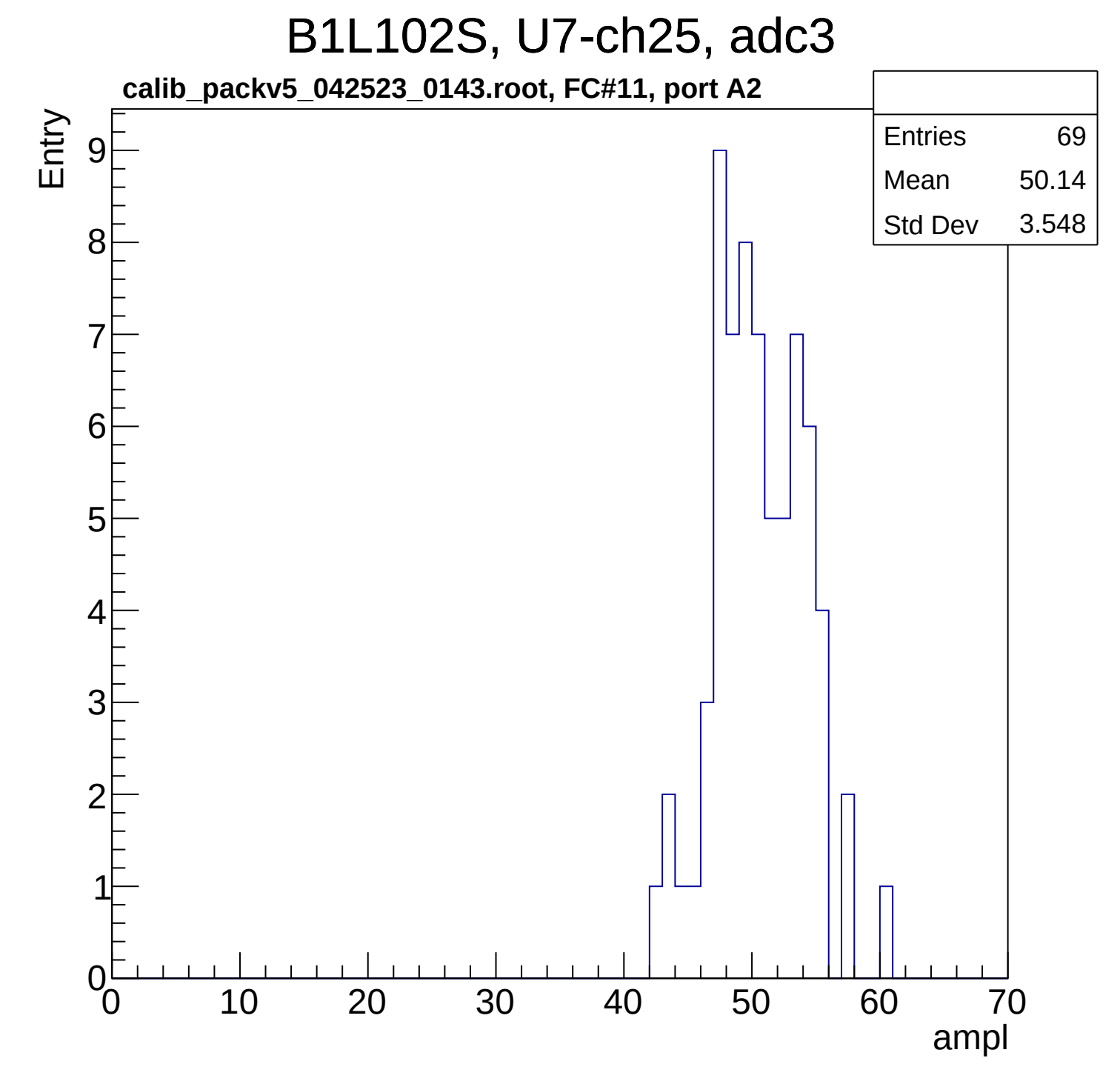
B1L102S, U7-ch25, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 69
Mean 50.14
Std Dev 3.548
Entry
ampl
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3
4
5
6
7
8
9
0
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60
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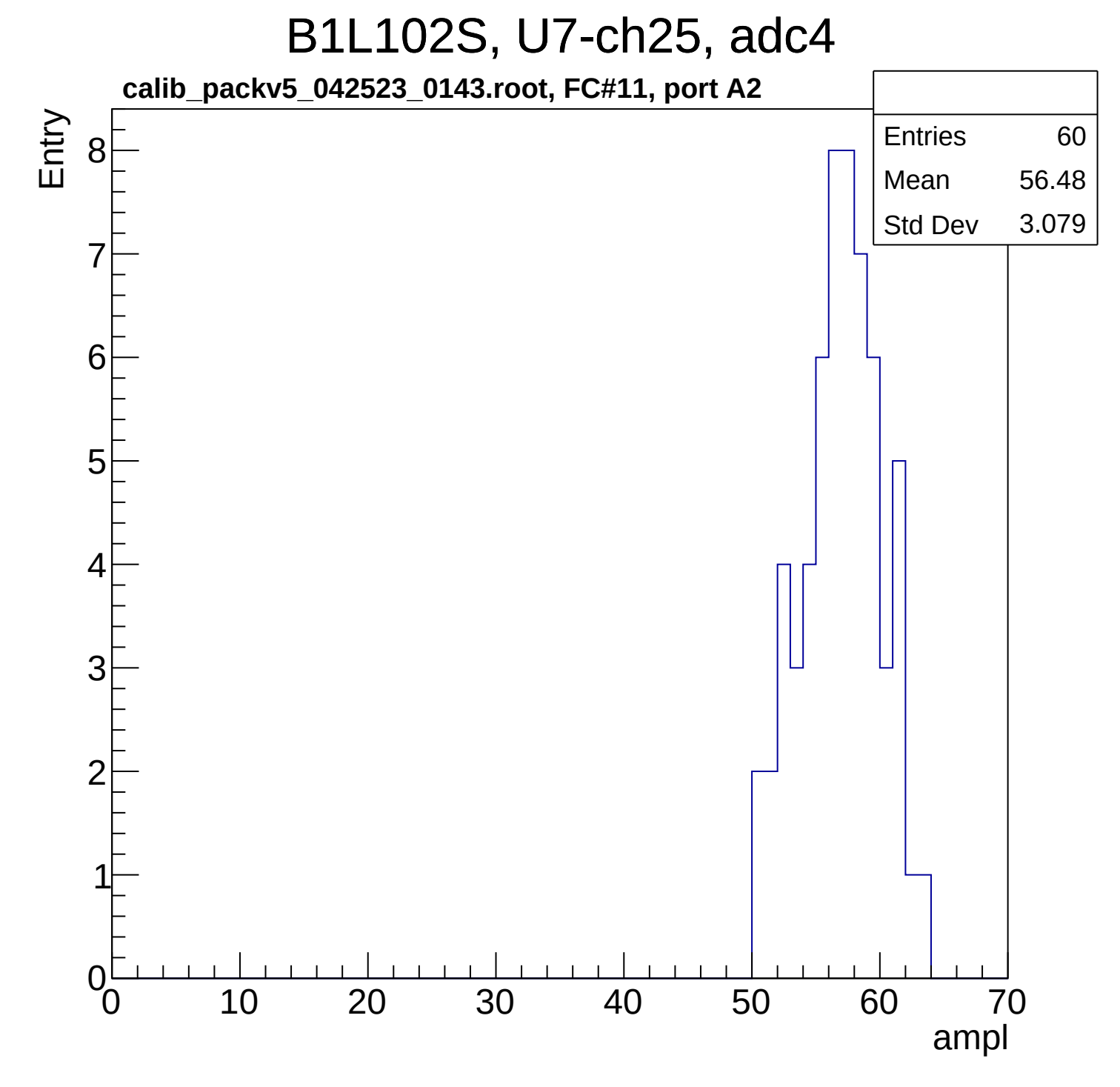
B1L102S, U7-ch25, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 60
Mean 56.48
Std Dev 3.079
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
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60
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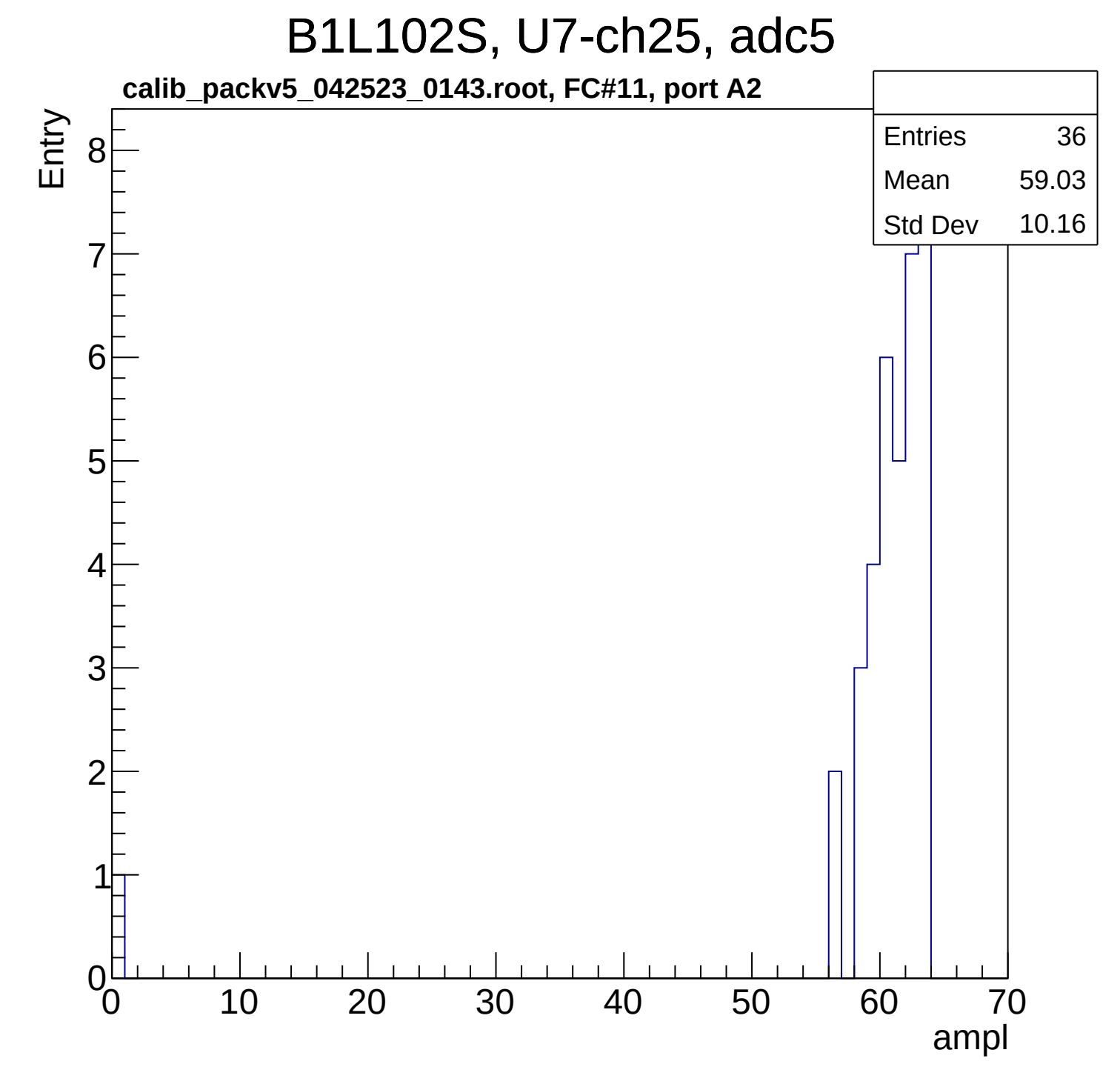
B1L102S, U7-ch25, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 36
Mean 59.03
Std Dev 10.16
Entry
ampl
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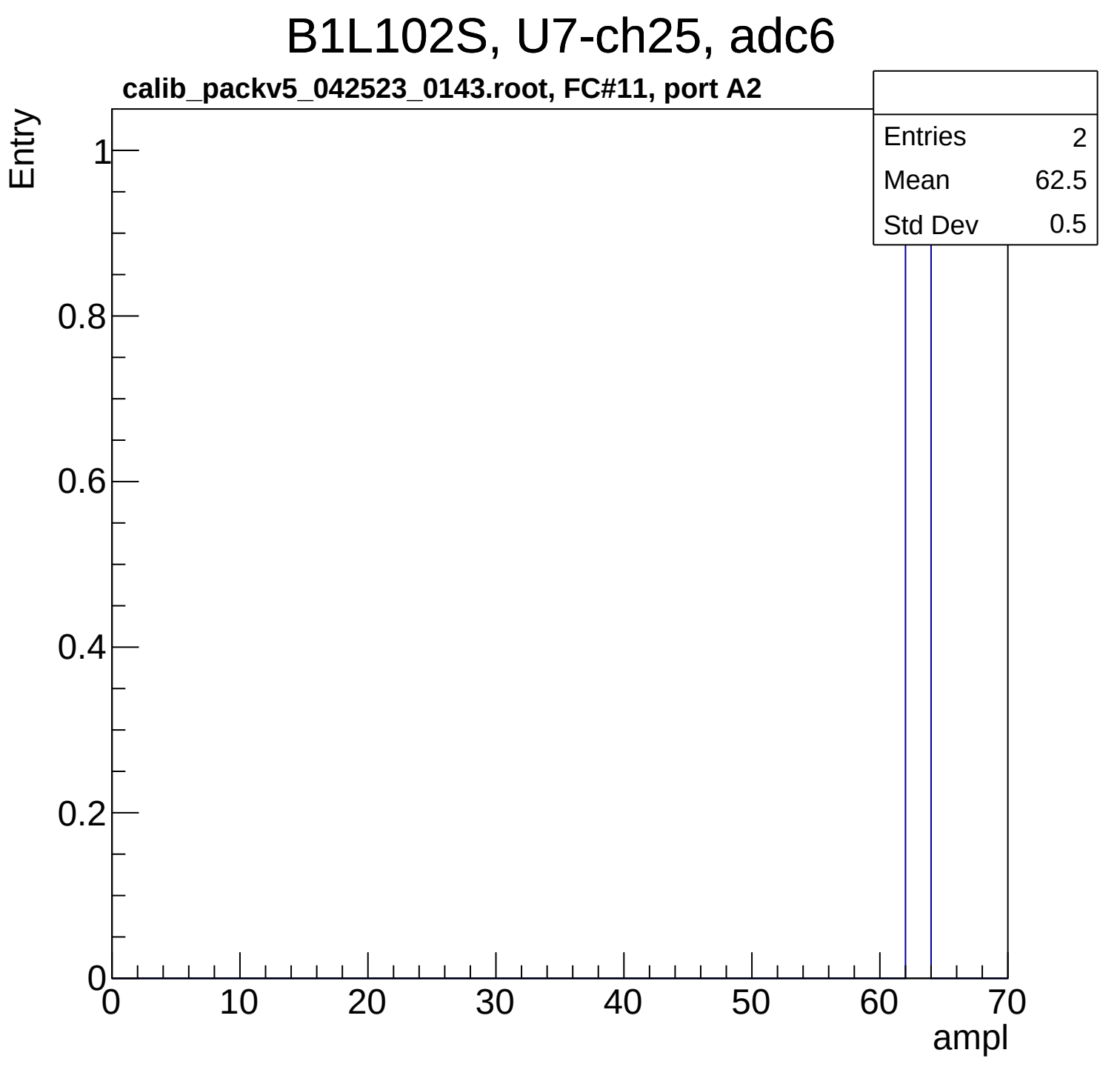
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L102S, U7-ch25, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 2
Mean 62.5
Std Dev 0.5
Entry
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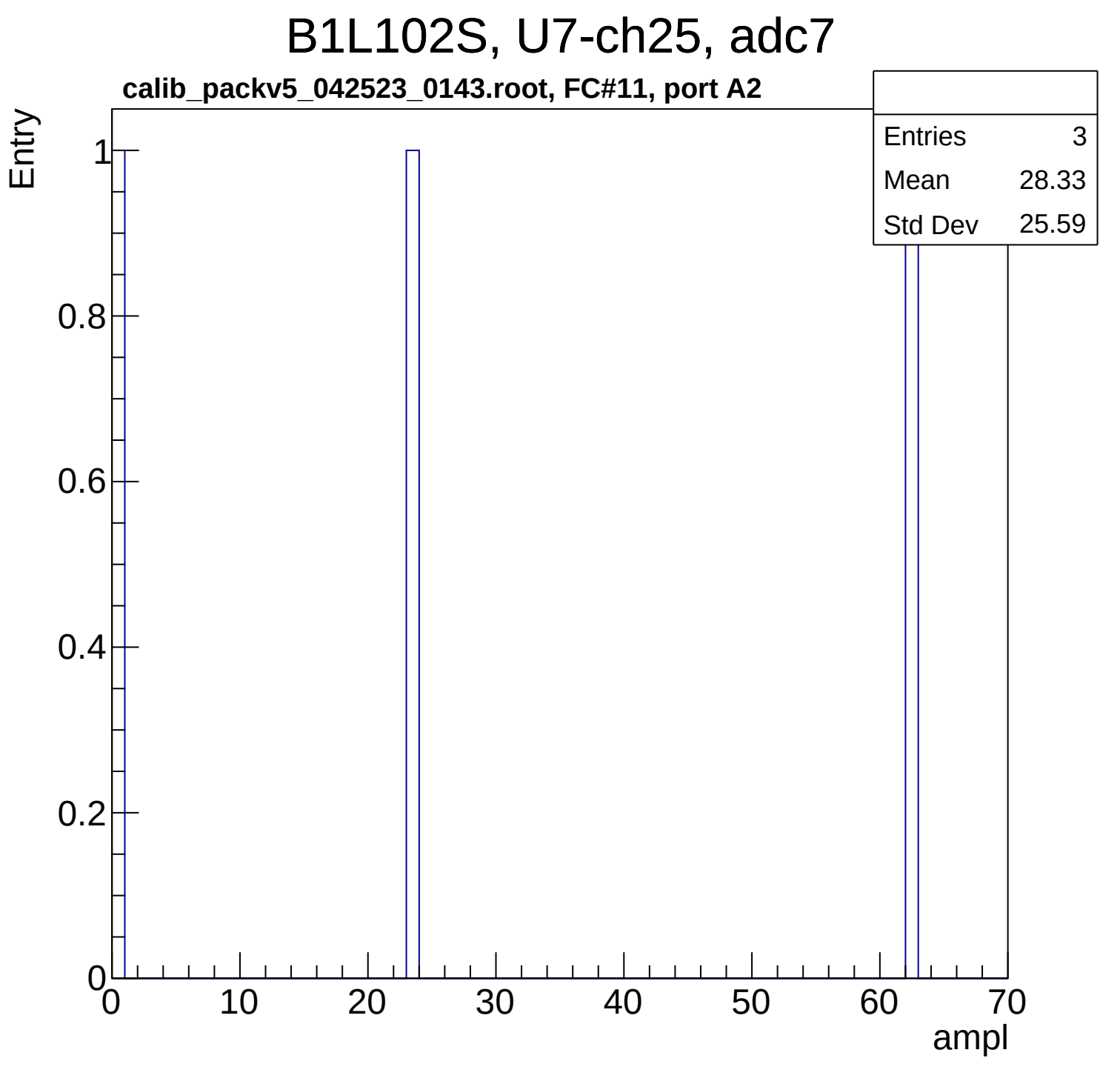
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U7-ch25, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 3
Mean 28.33
Std Dev 25.59
Entry
ampl
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0.2
0.4
0.6
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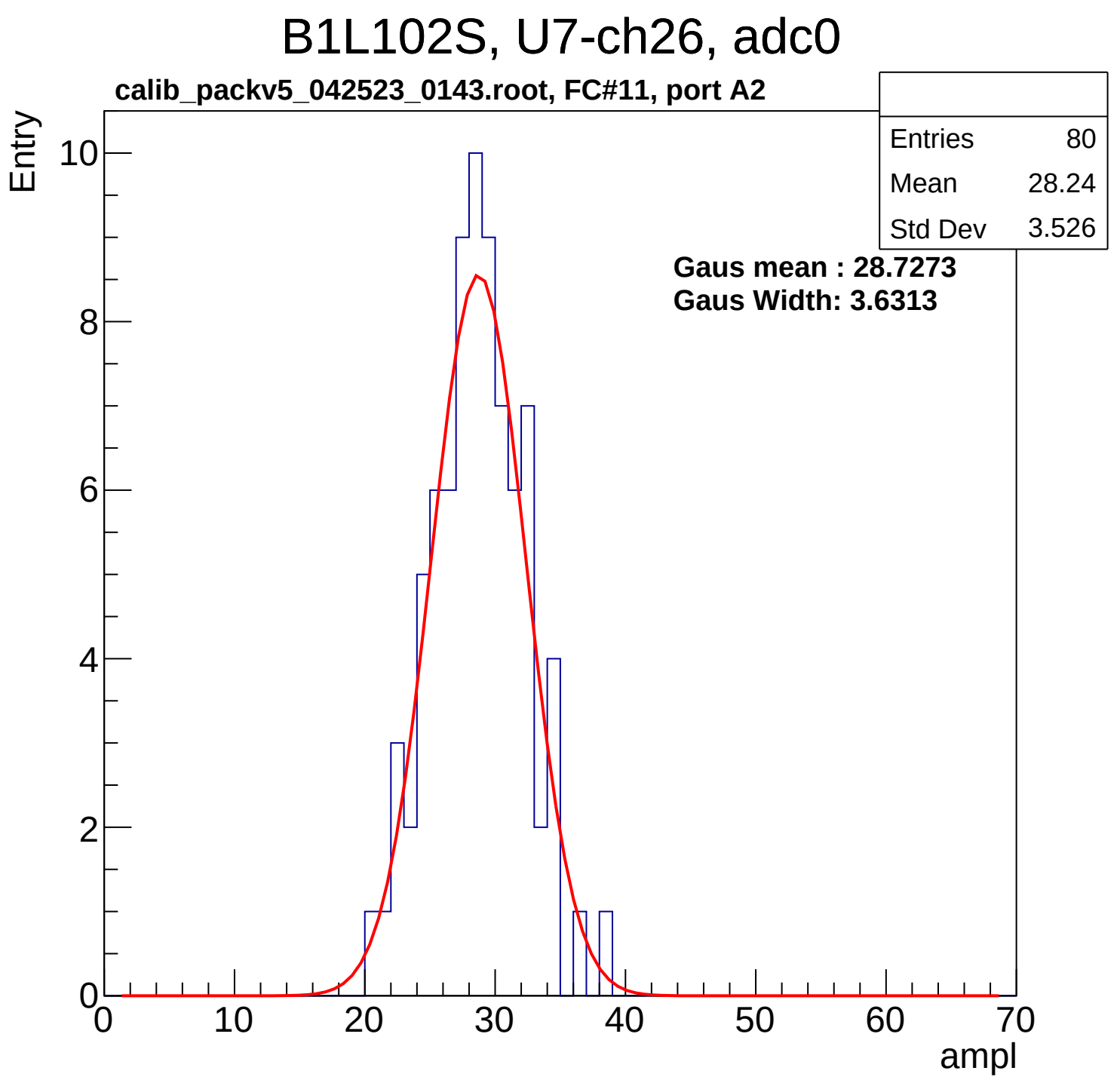
1
0
10
20
30
40
50
60
70


B1L102S, U7-ch26, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 80
Mean 28.24
Std Dev 3.526
Gaus mean : 28.7273
Gaus Width: 3.6313
Entry
ampl
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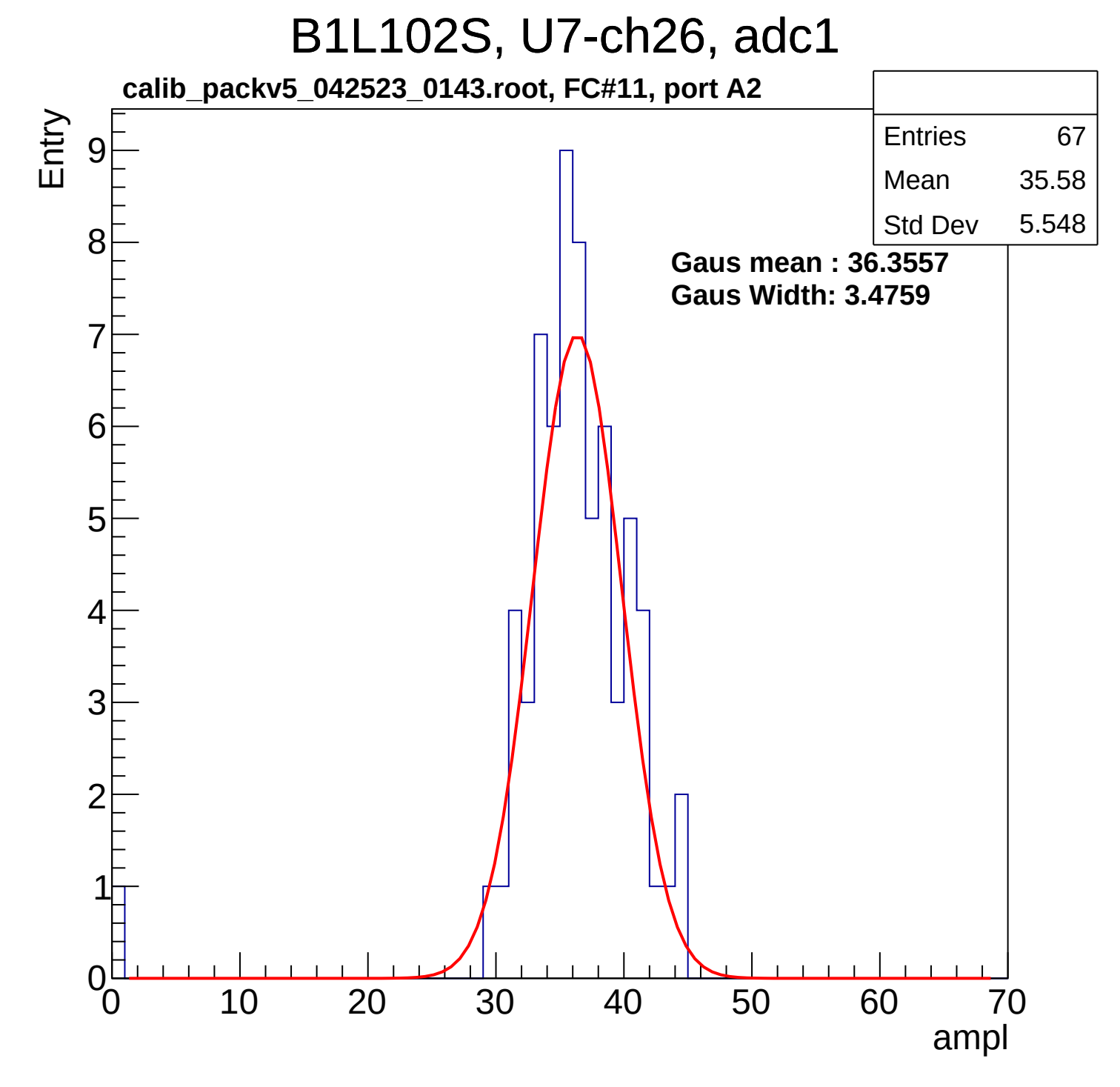
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L102S, U7-ch26, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 67
Mean 35.58
Std Dev 5.548
Gaus mean : 36.3557
Gaus Width: 3.4759
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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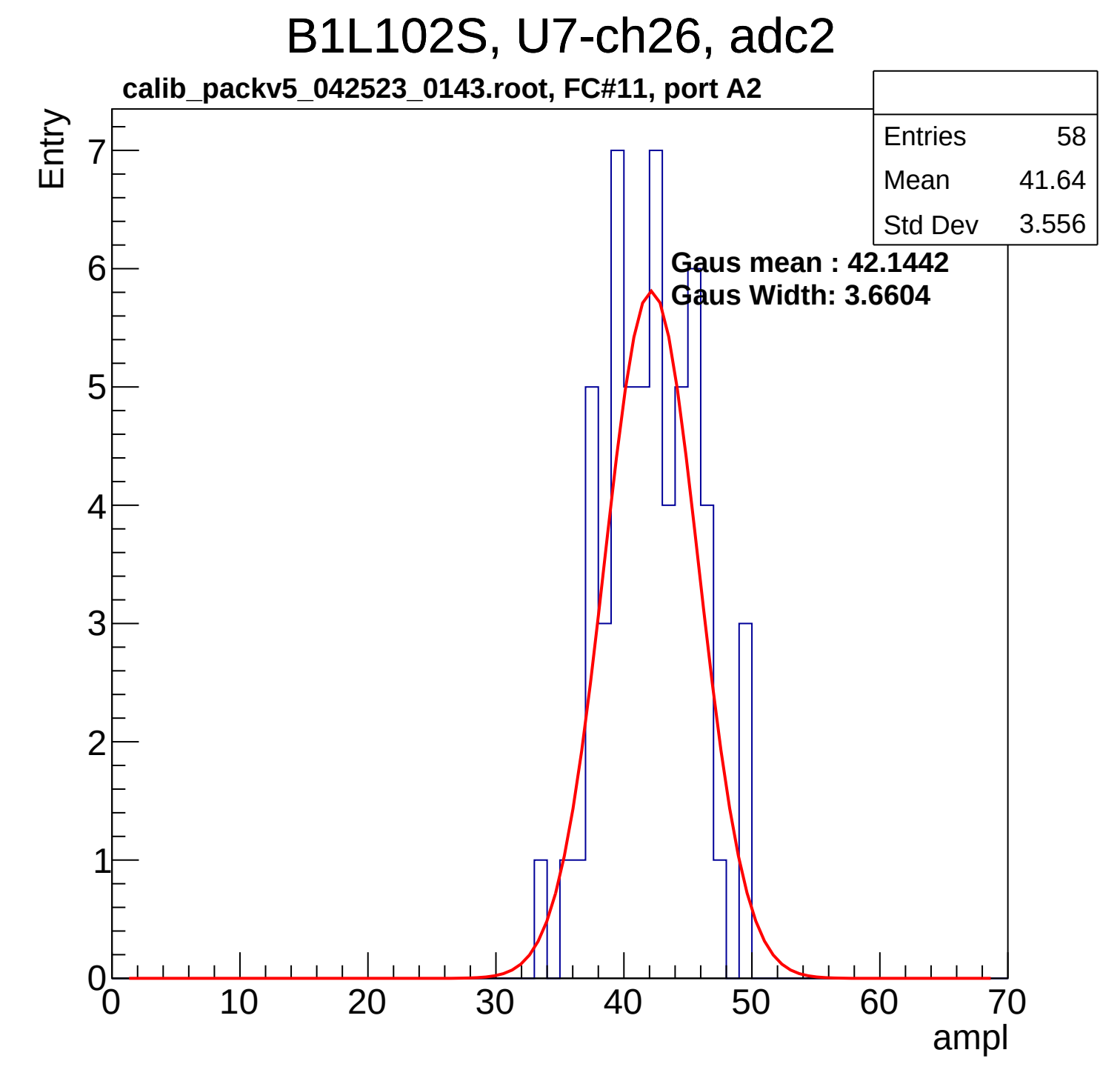
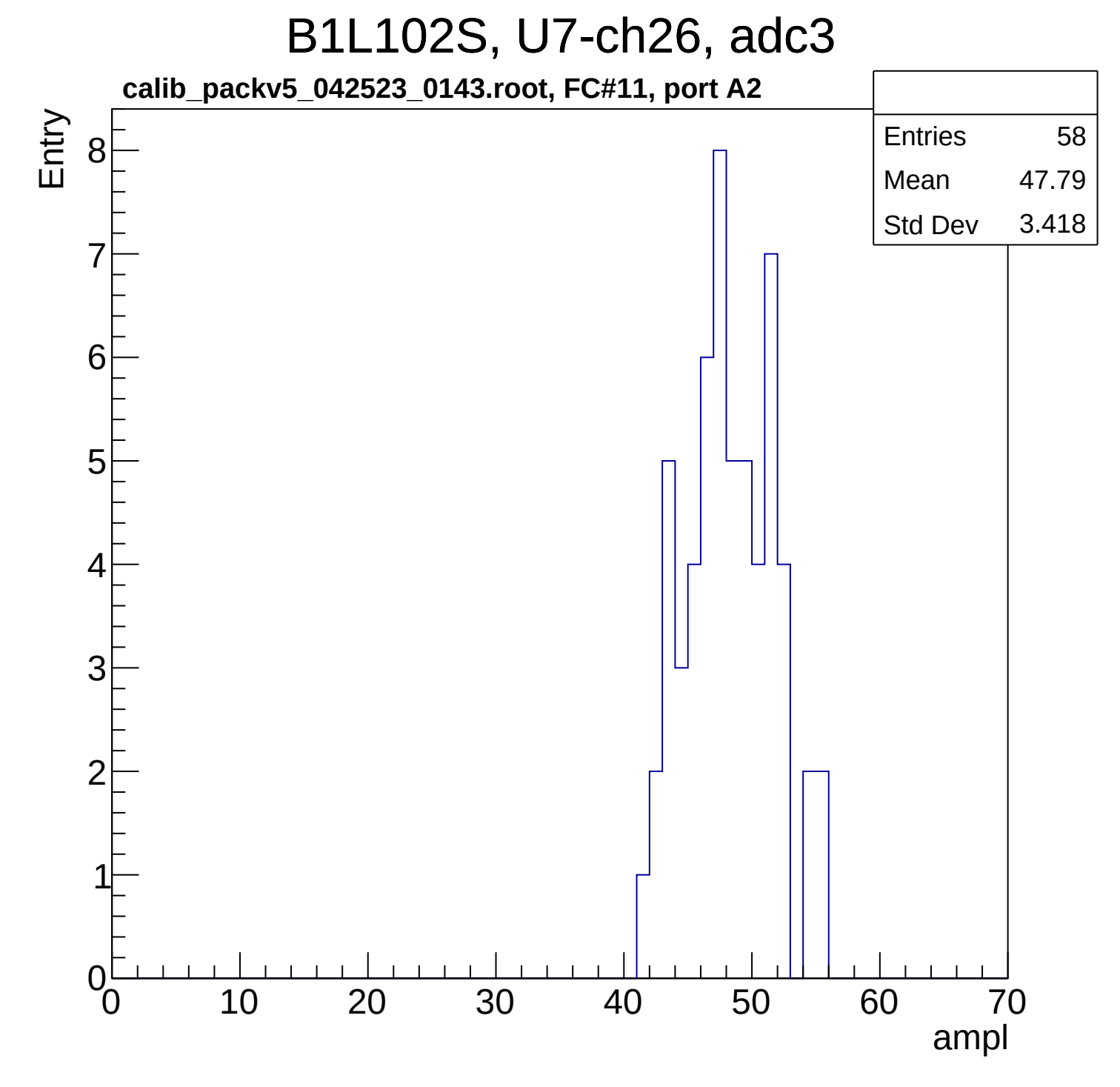

B1L102S, U7-ch26, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 58
Mean 41.64
Std Dev 3.556
Gaus mean : 42.1442
Gaus Width: 3.6604
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L102S, U7-ch26, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 58
Mean 47.79
Std Dev 3.418
Entry
ampl
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2
3
4
5
6
7
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10
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50
60
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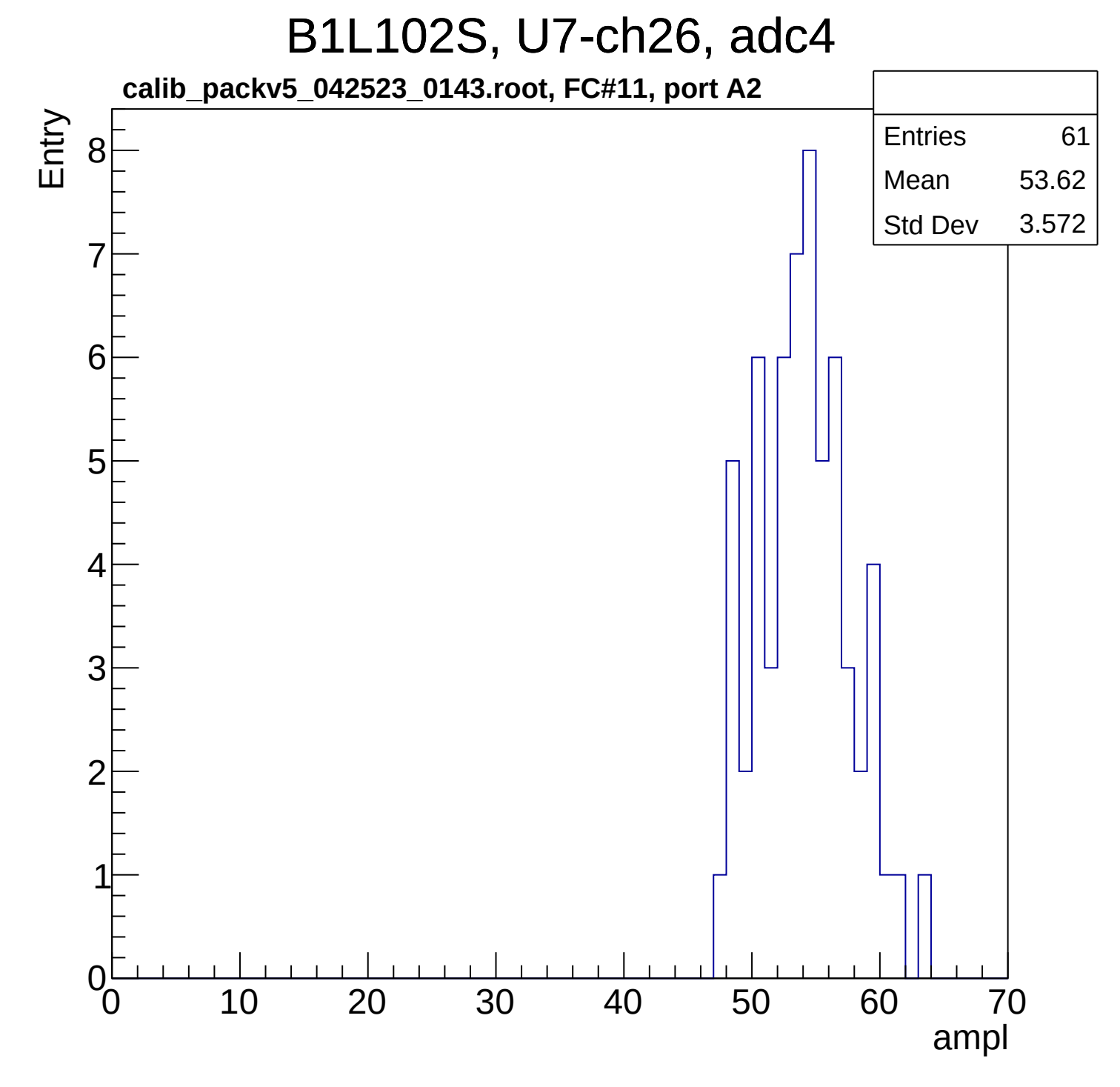
B1L102S, U7-ch26, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 61
Mean 53.62
Std Dev 3.572
Entry
ampl
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2
3
4
5
6
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8
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10
20
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40
50
60
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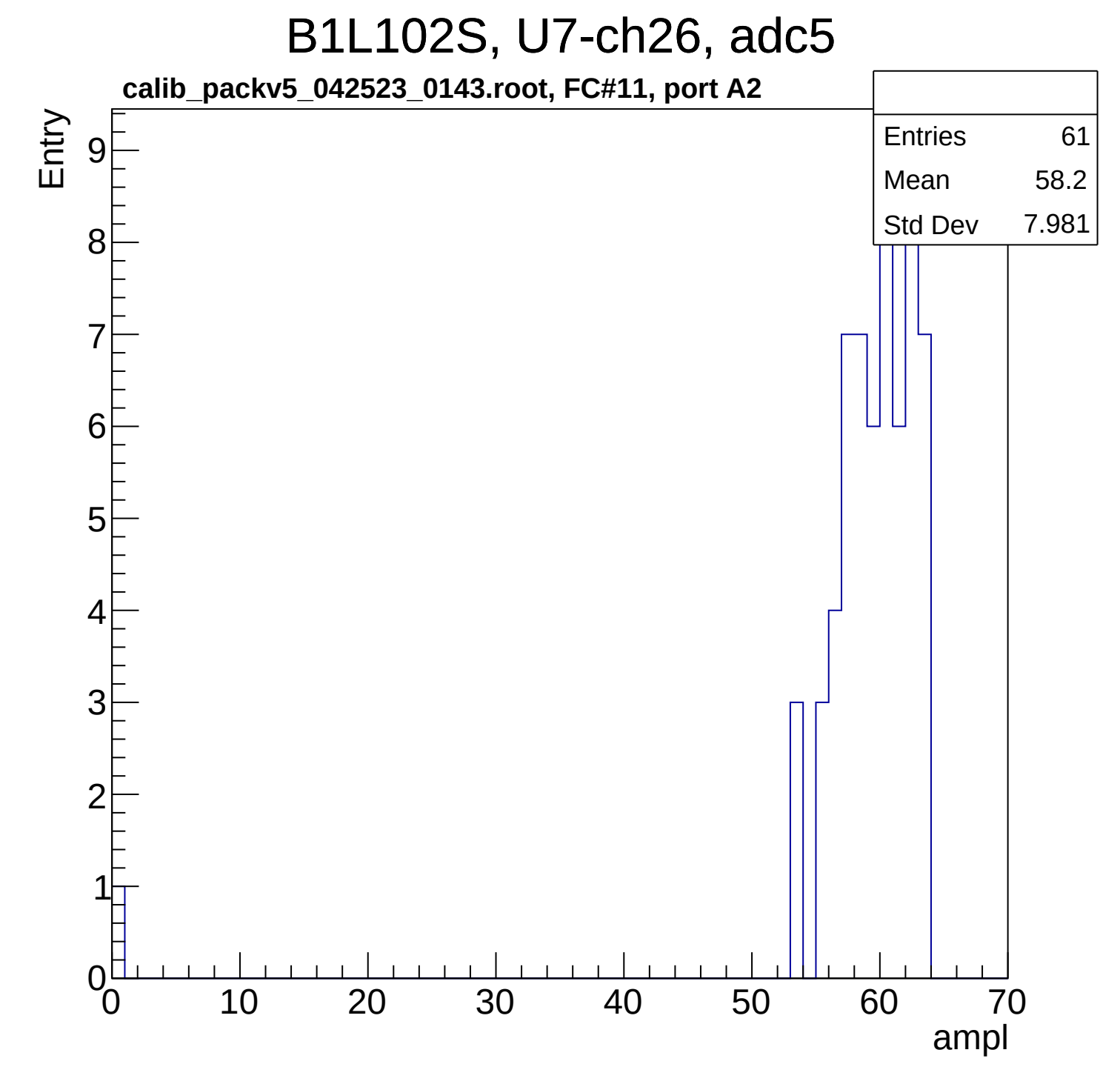
B1L102S, U7-ch26, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 61
Mean 58.2
Std Dev 7.981
Entry
ampl
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2
3
4
5
6
7
8
9
0
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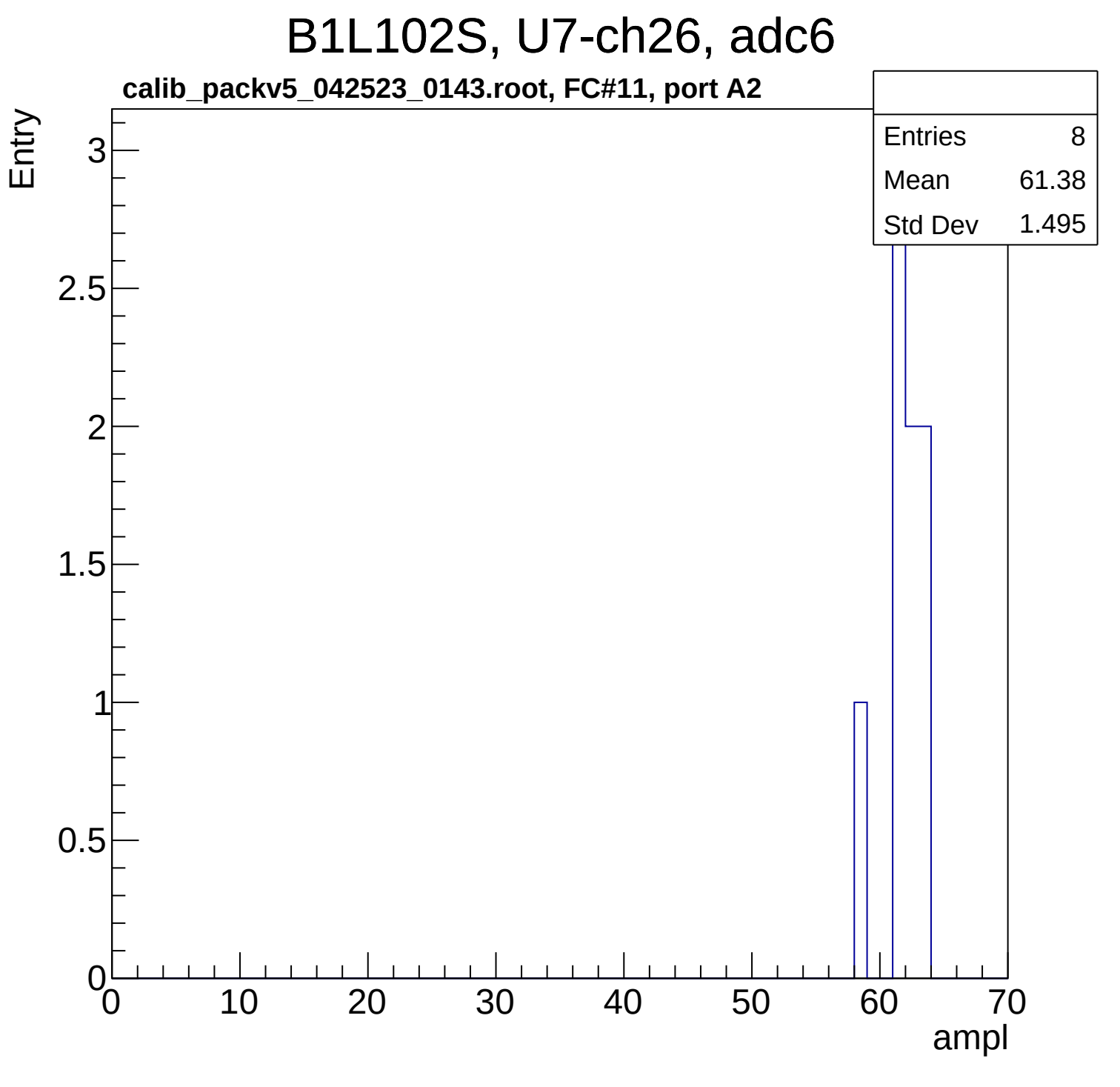
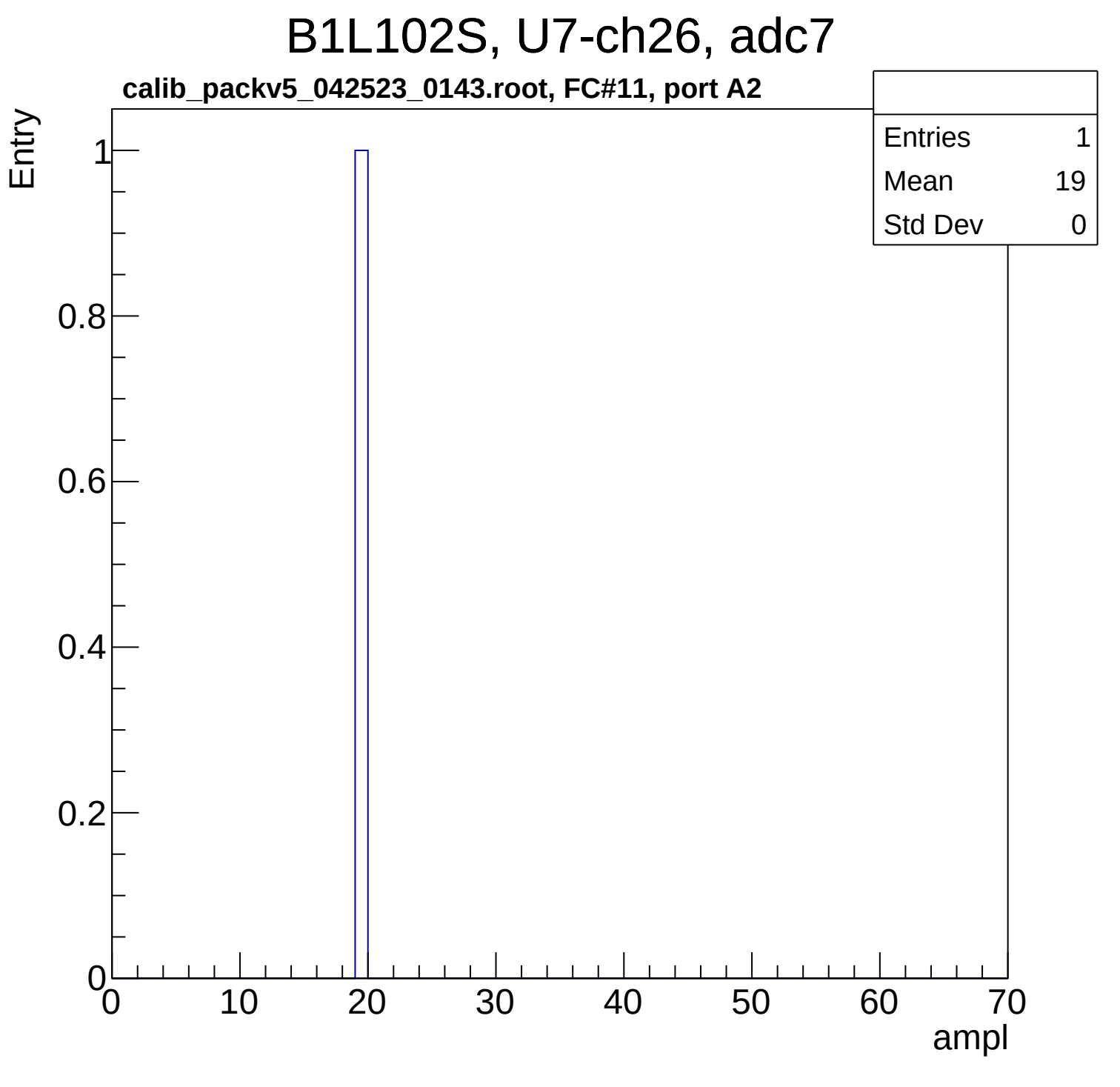

B1L102S, U7-ch26, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 8
Mean 61.38
Std Dev 1.495
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L102S, U7-ch26, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 1
Mean 19
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
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60
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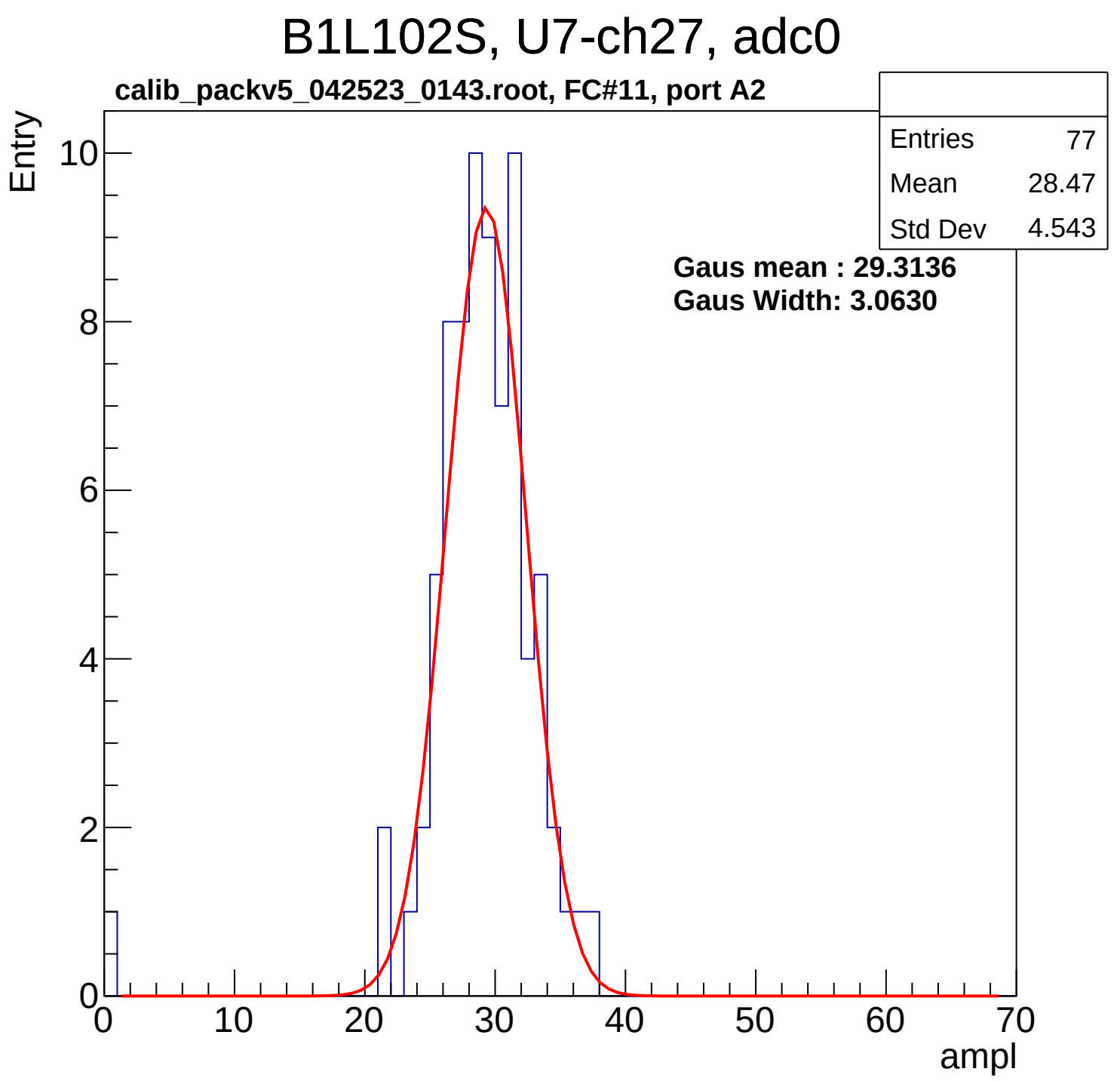
B1L102S, U7-ch27, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 77
Mean 28.47
Std Dev 4.543
Gaus mean : 29.3136
Gaus Width: 3.0630
Entry
ampl
0
2
4
6
8
10
0
10
20
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40
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60
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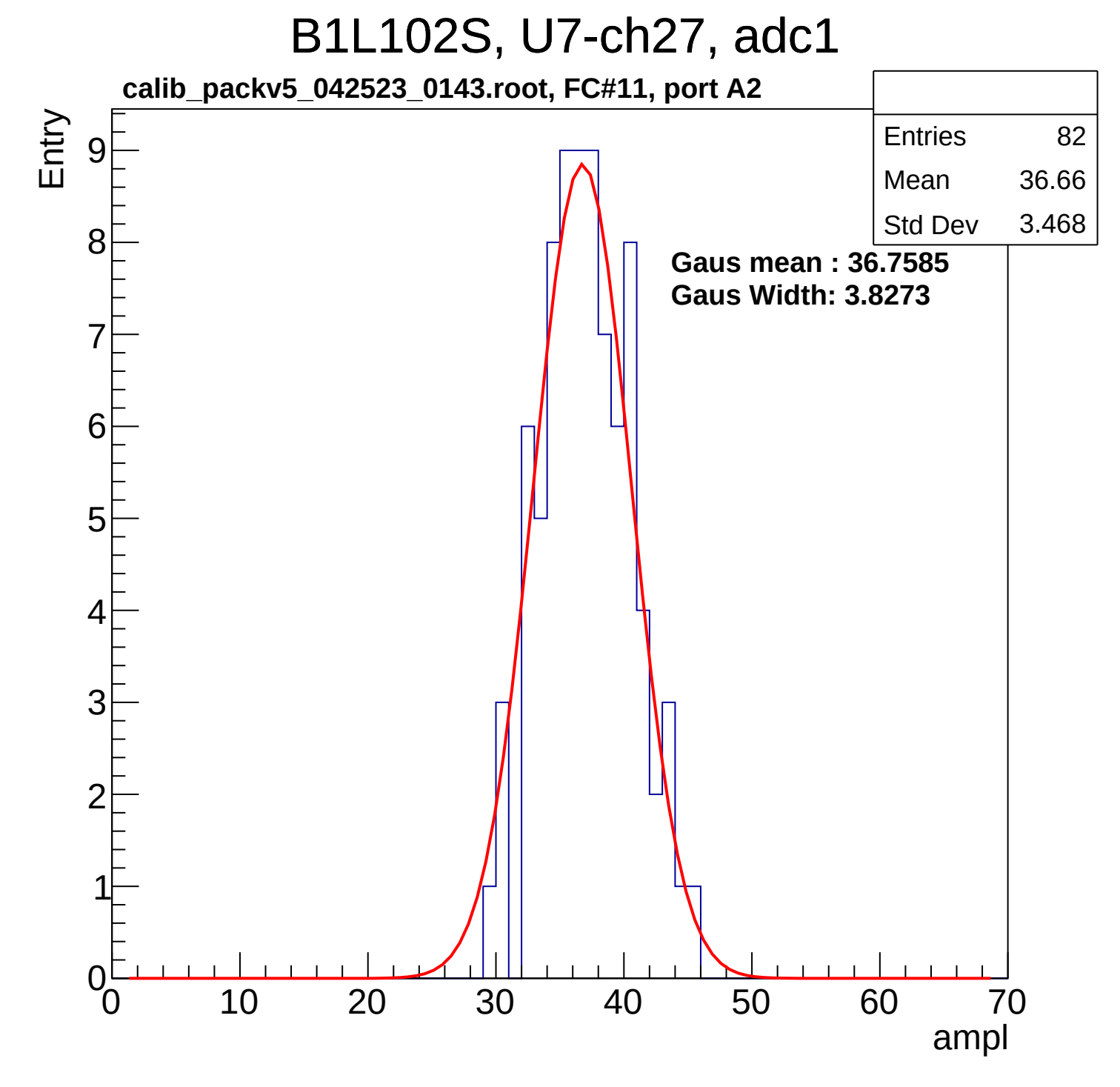
B1L102S, U7-ch27, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 82
Mean 36.66
Std Dev 3.468
Gaus mean : 36.7585
Gaus Width: 3.8273
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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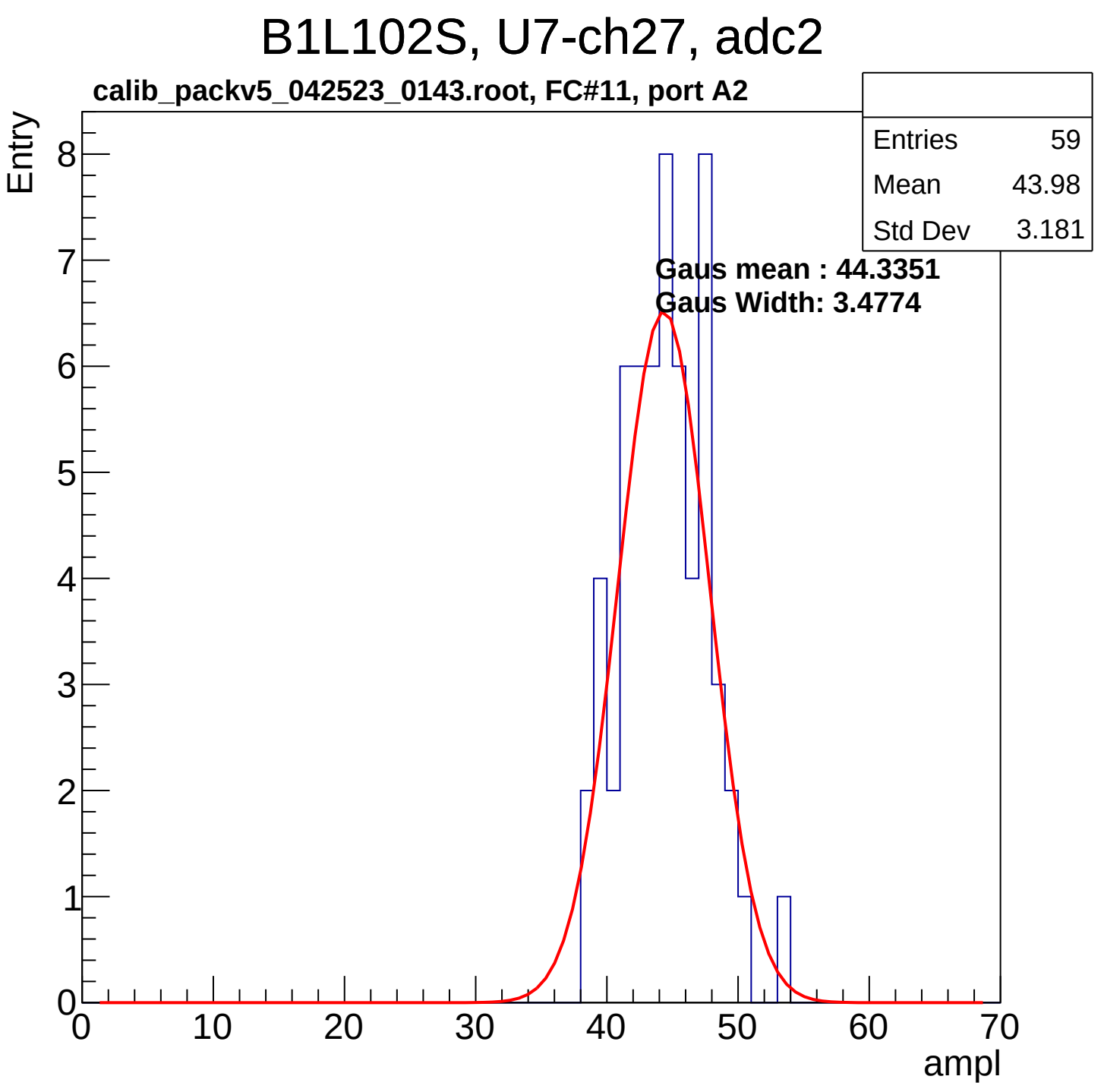
B1L102S, U7-ch27, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 59
Mean 43.98
Std Dev 3.181
Gaus mean : 44.3351
Gaus Width: 3.4774
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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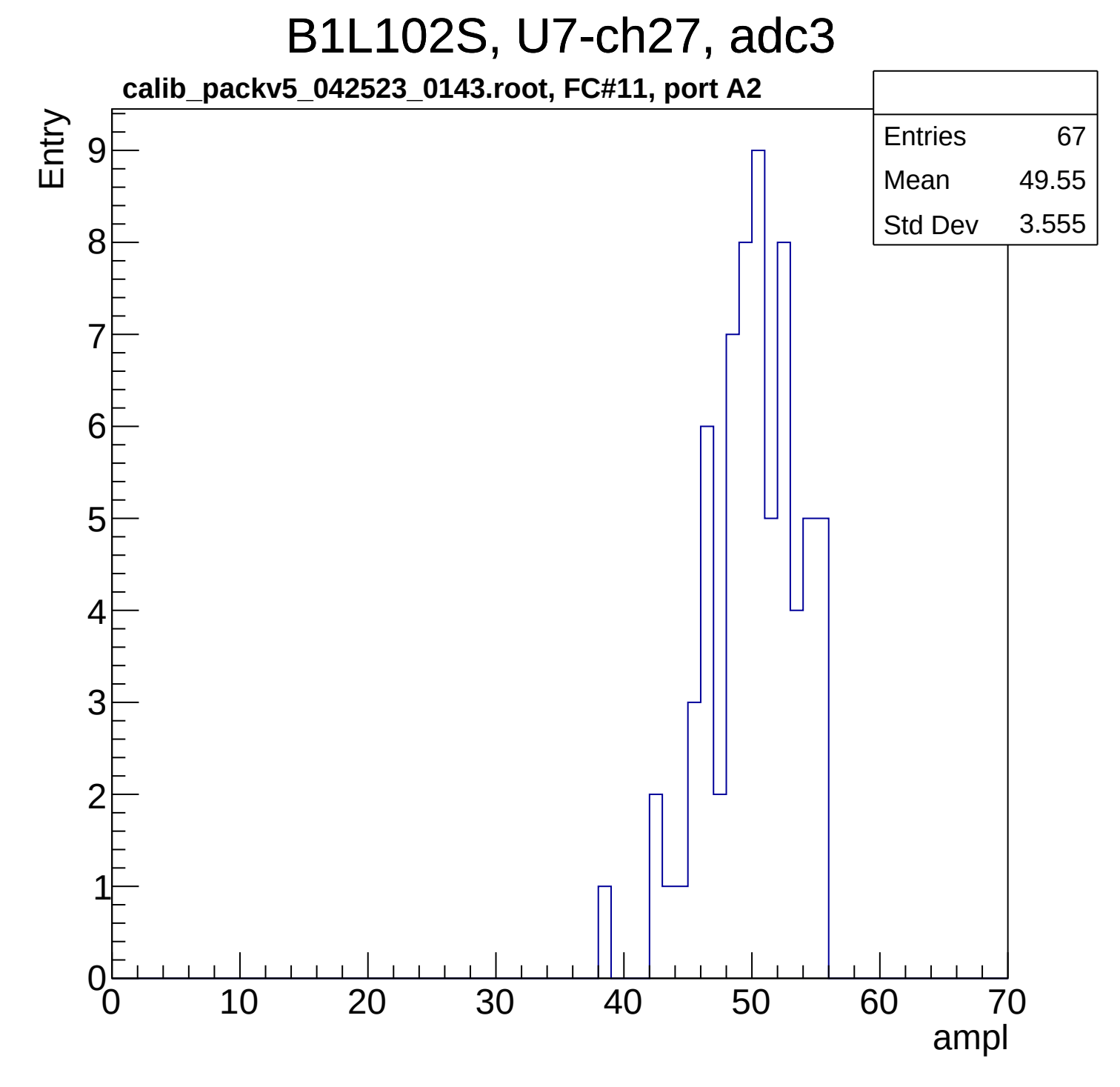
B1L102S, U7-ch27, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 67
Mean 49.55
Std Dev 3.555
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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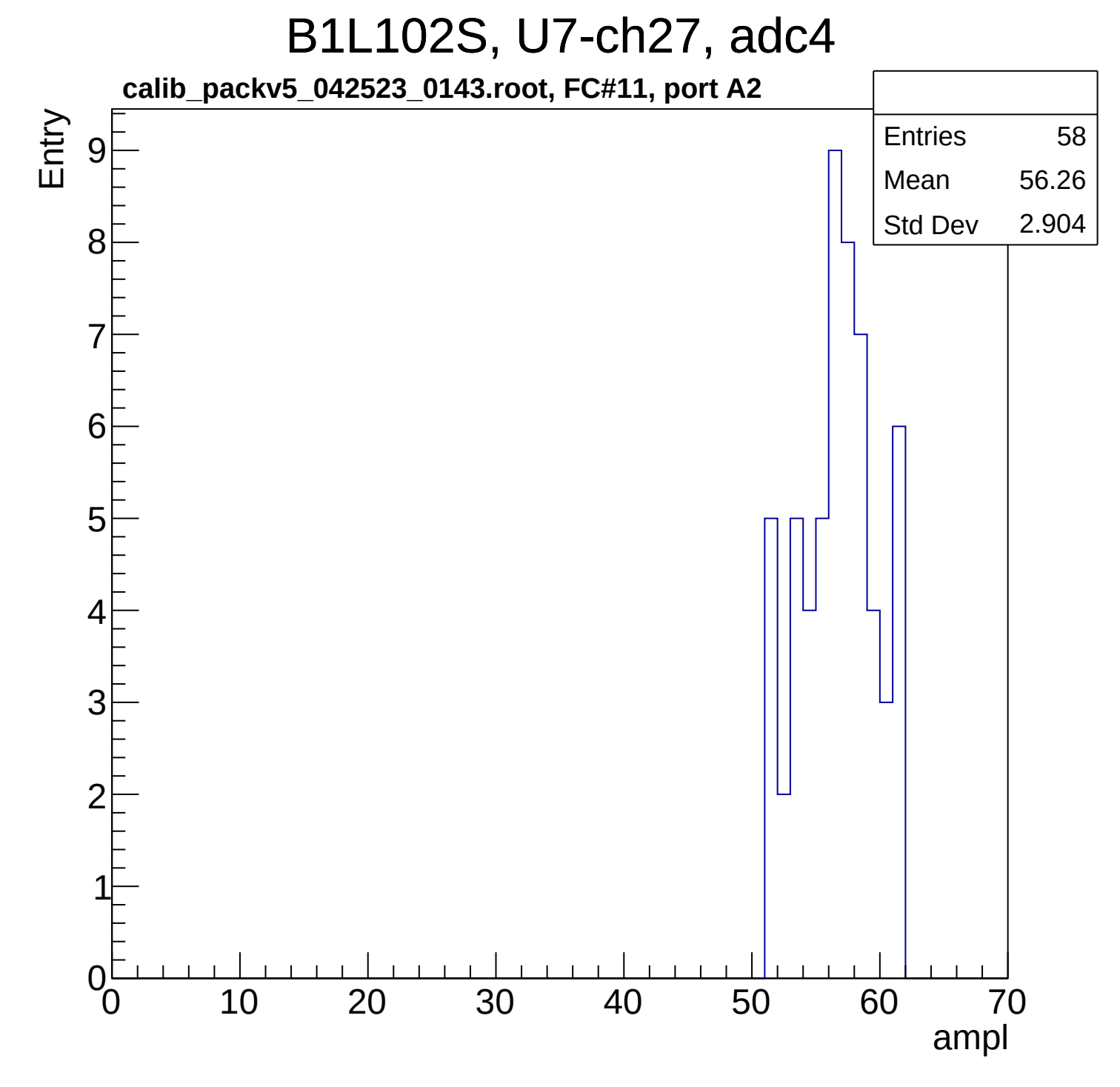
B1L102S, U7-ch27, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 58
Mean 56.26
Std Dev 2.904
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
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60
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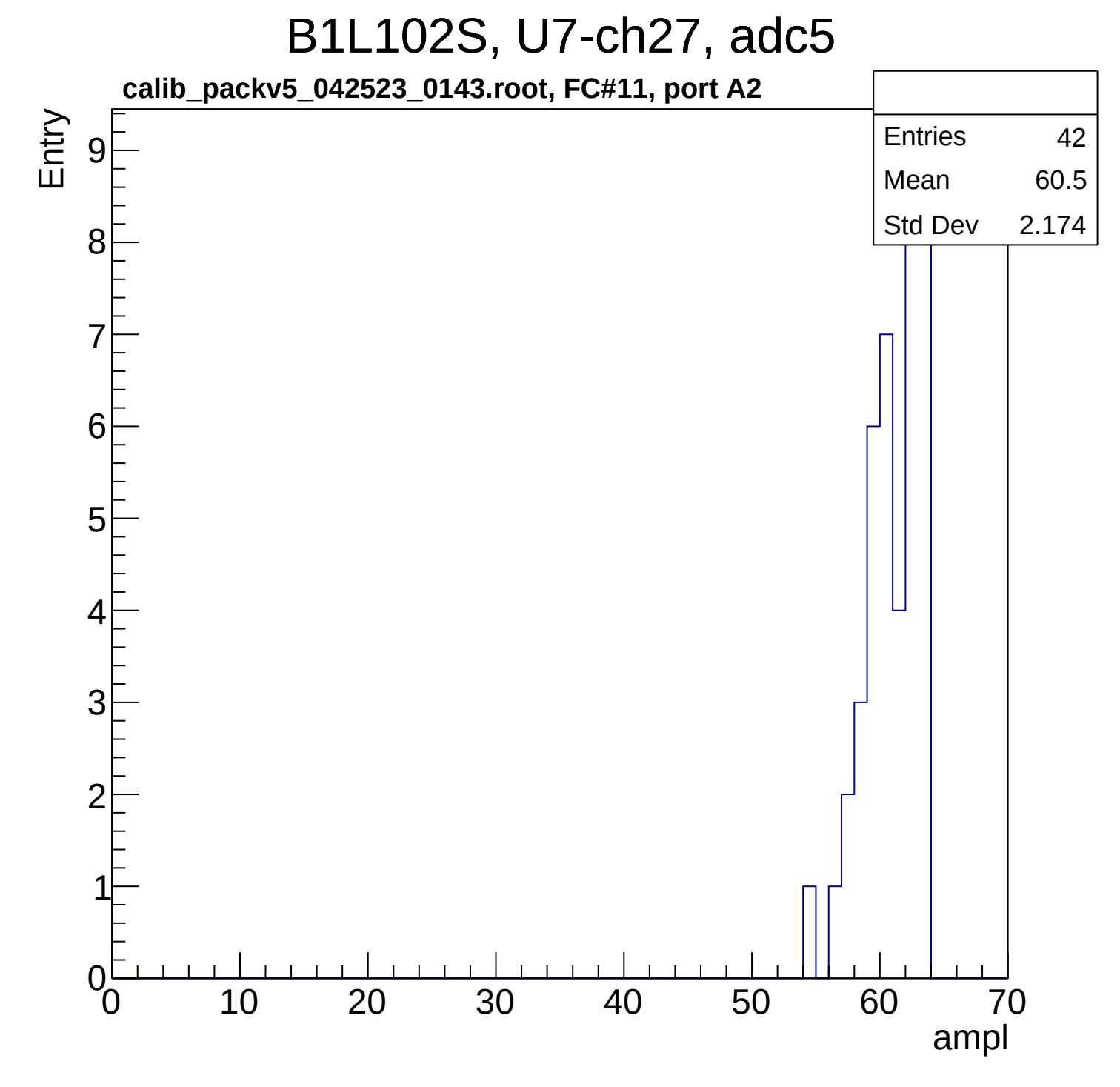
B1L102S, U7-ch27, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 42
Mean 60.5
Std Dev 2.174
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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40
50
60
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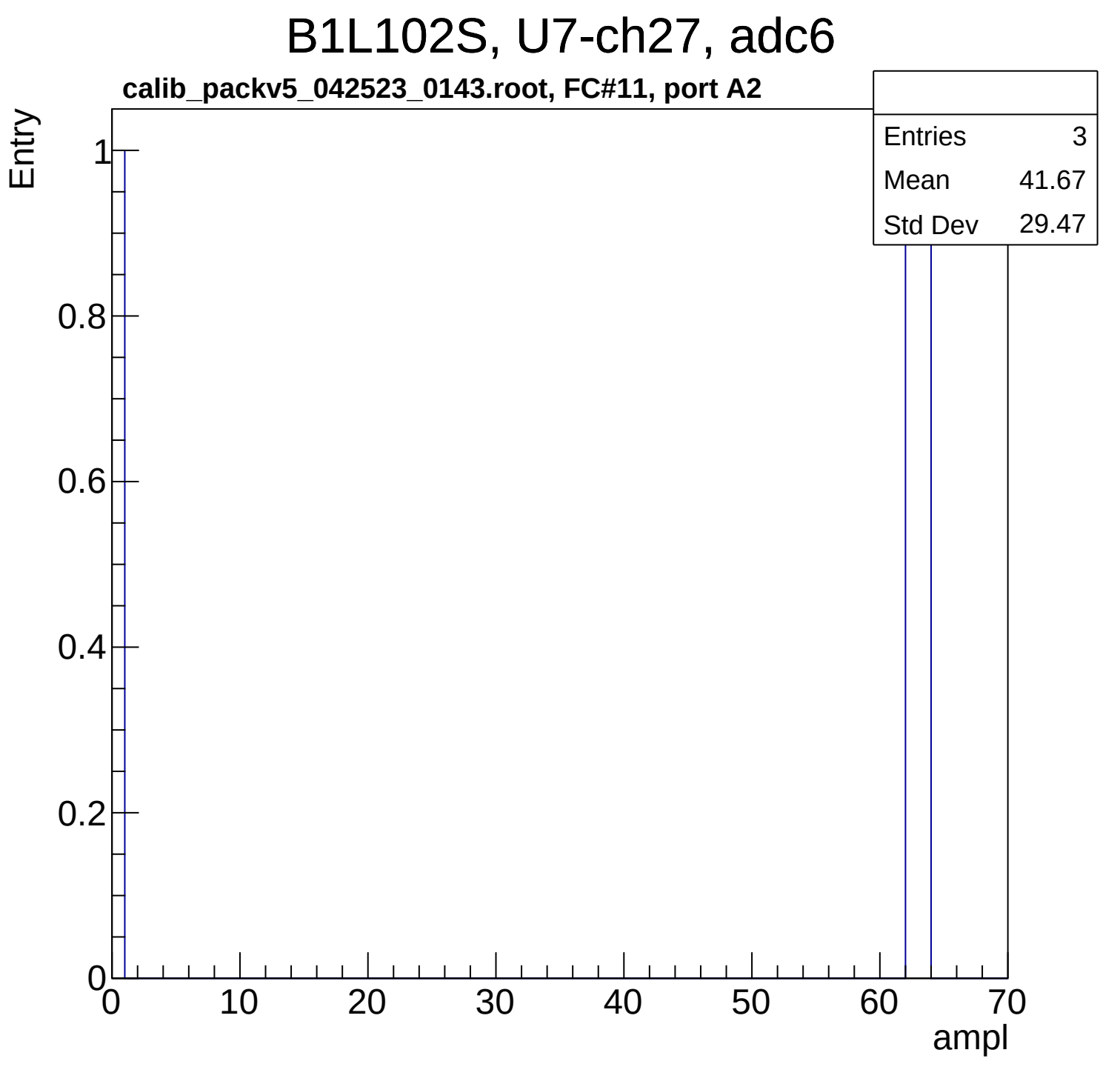
B1L102S, U7-ch27, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 3
Mean 41.67
Std Dev 29.47
Entry
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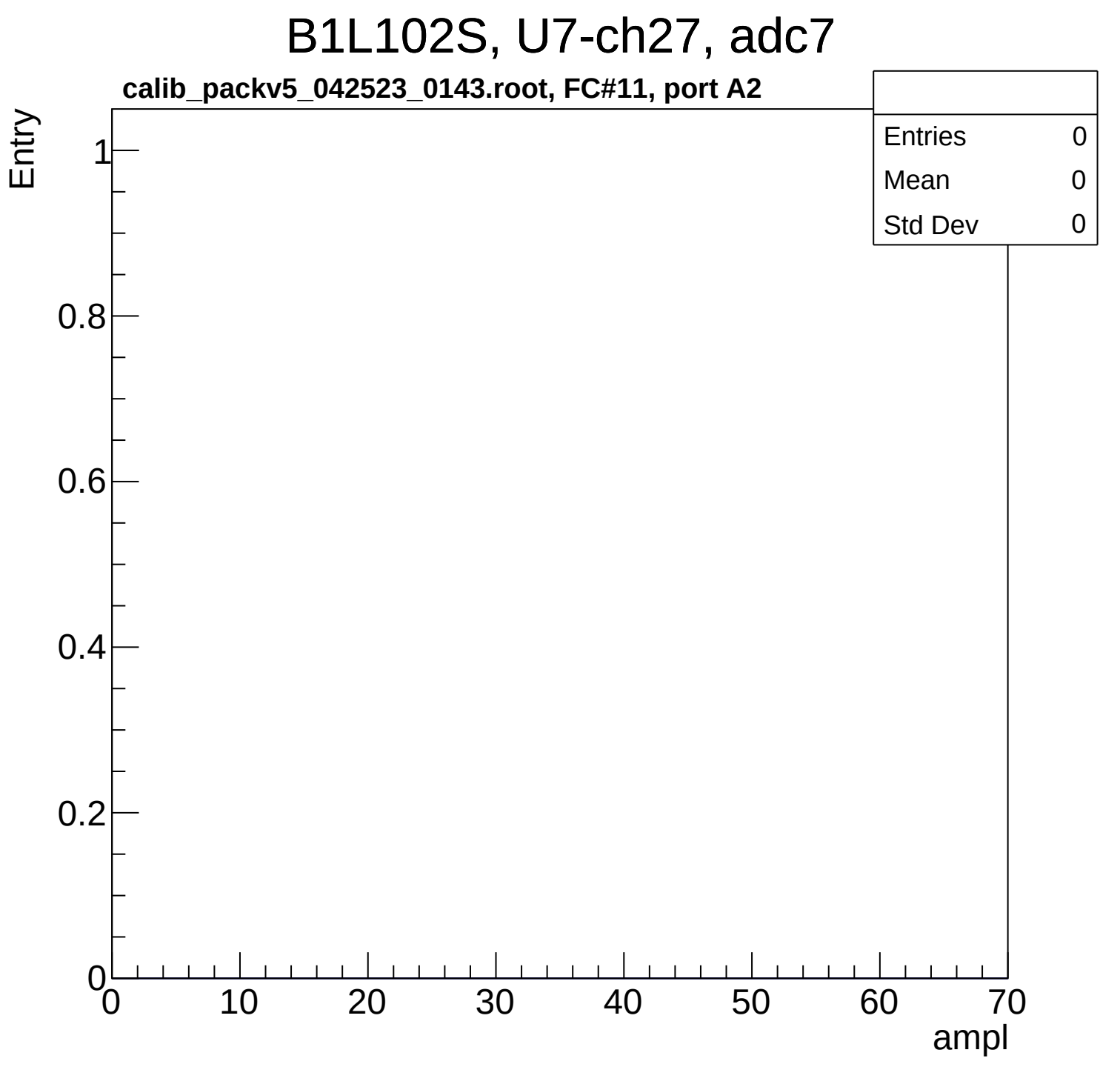
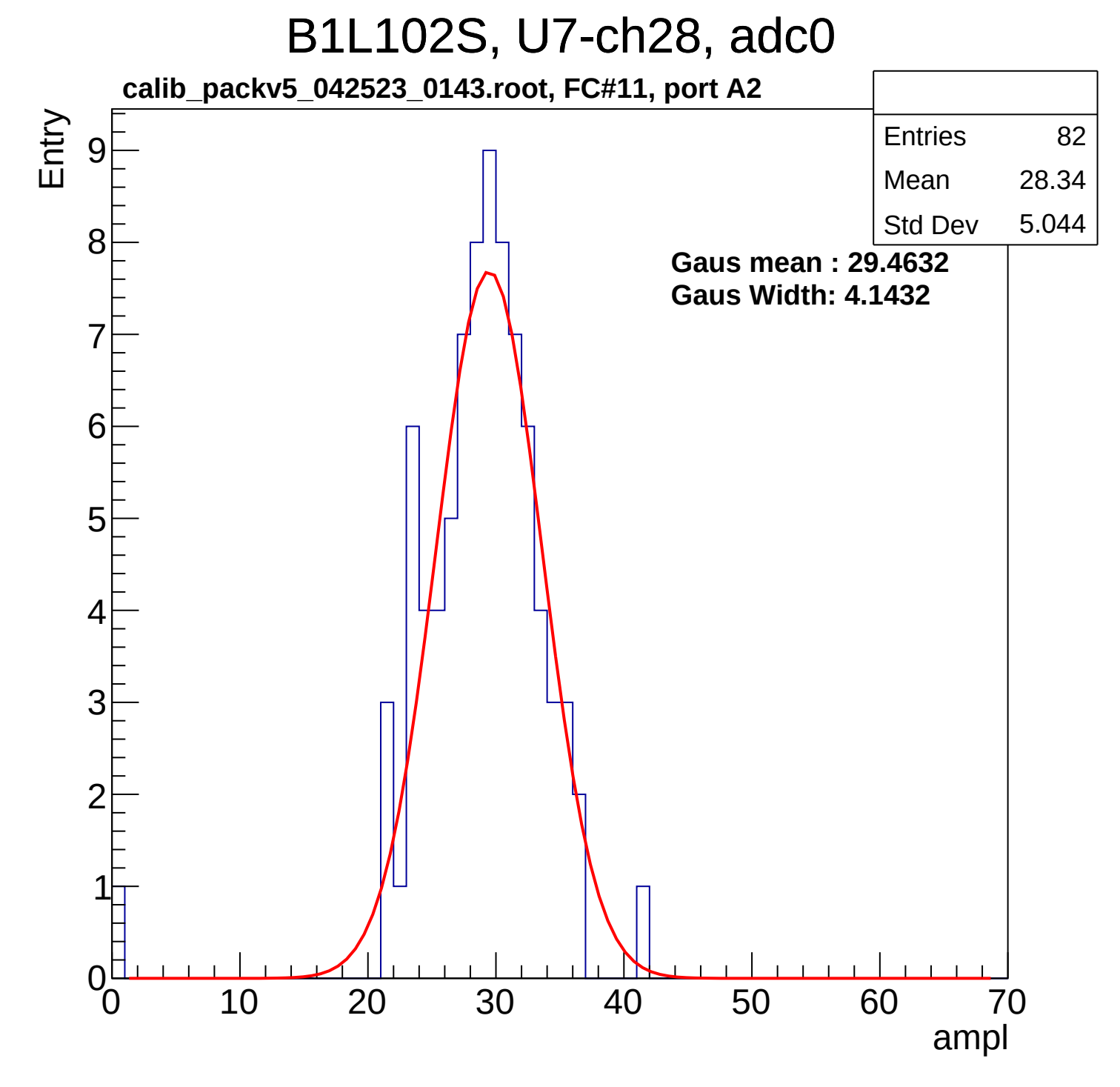
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U7-ch27, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U7-ch28, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 82
Mean 28.34
Std Dev 5.044
Gaus mean : 29.4632
Gaus Width: 4.1432
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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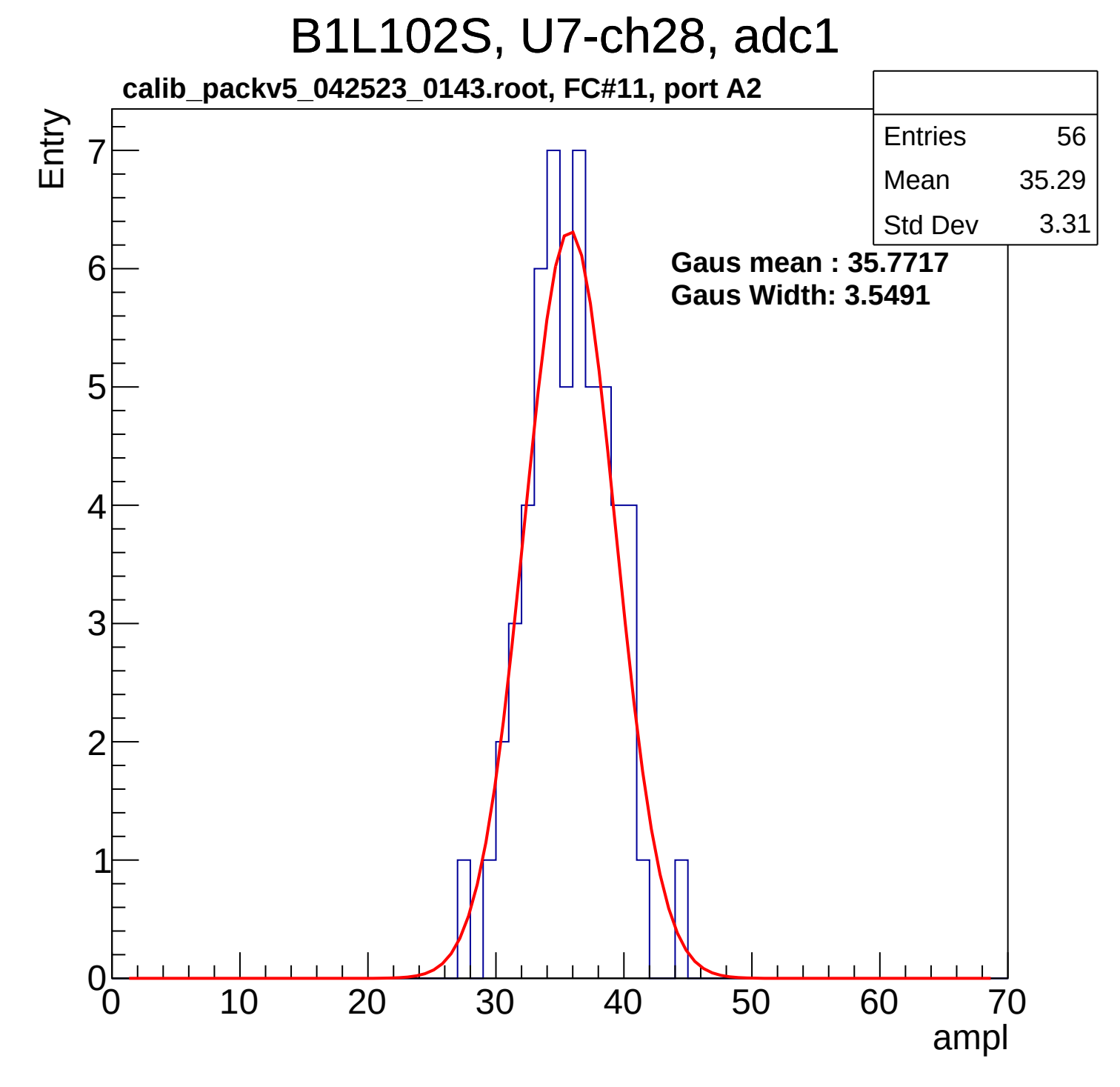
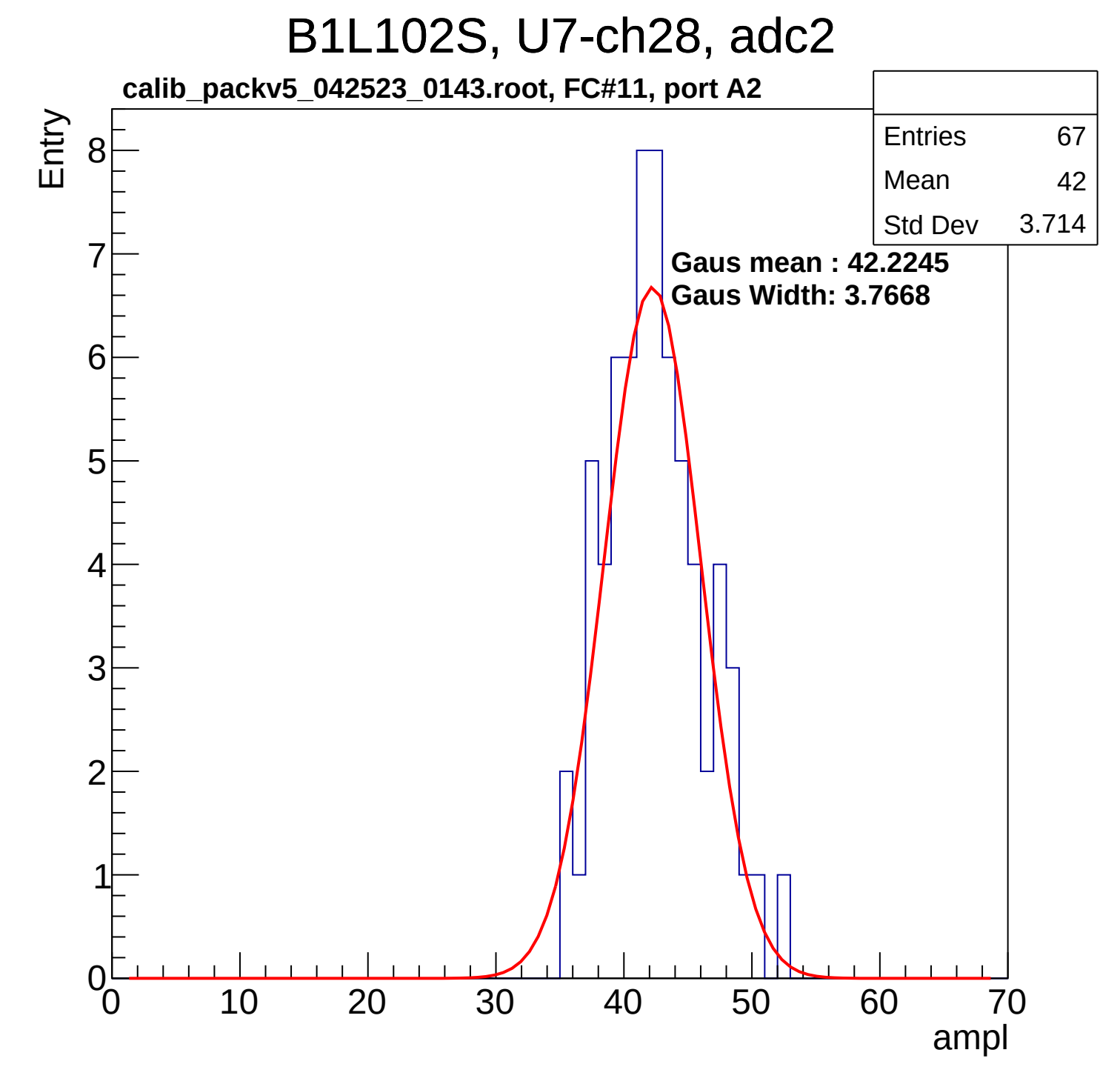

B1L102S, U7-ch28, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 56
Mean 35.29
Std Dev 3.31
Gaus mean : 35.7717
Gaus Width: 3.5491
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L102S, U7-ch28, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 67
Mean 42
Std Dev 3.714
Gaus mean : 42.2245
Gaus Width: 3.7668
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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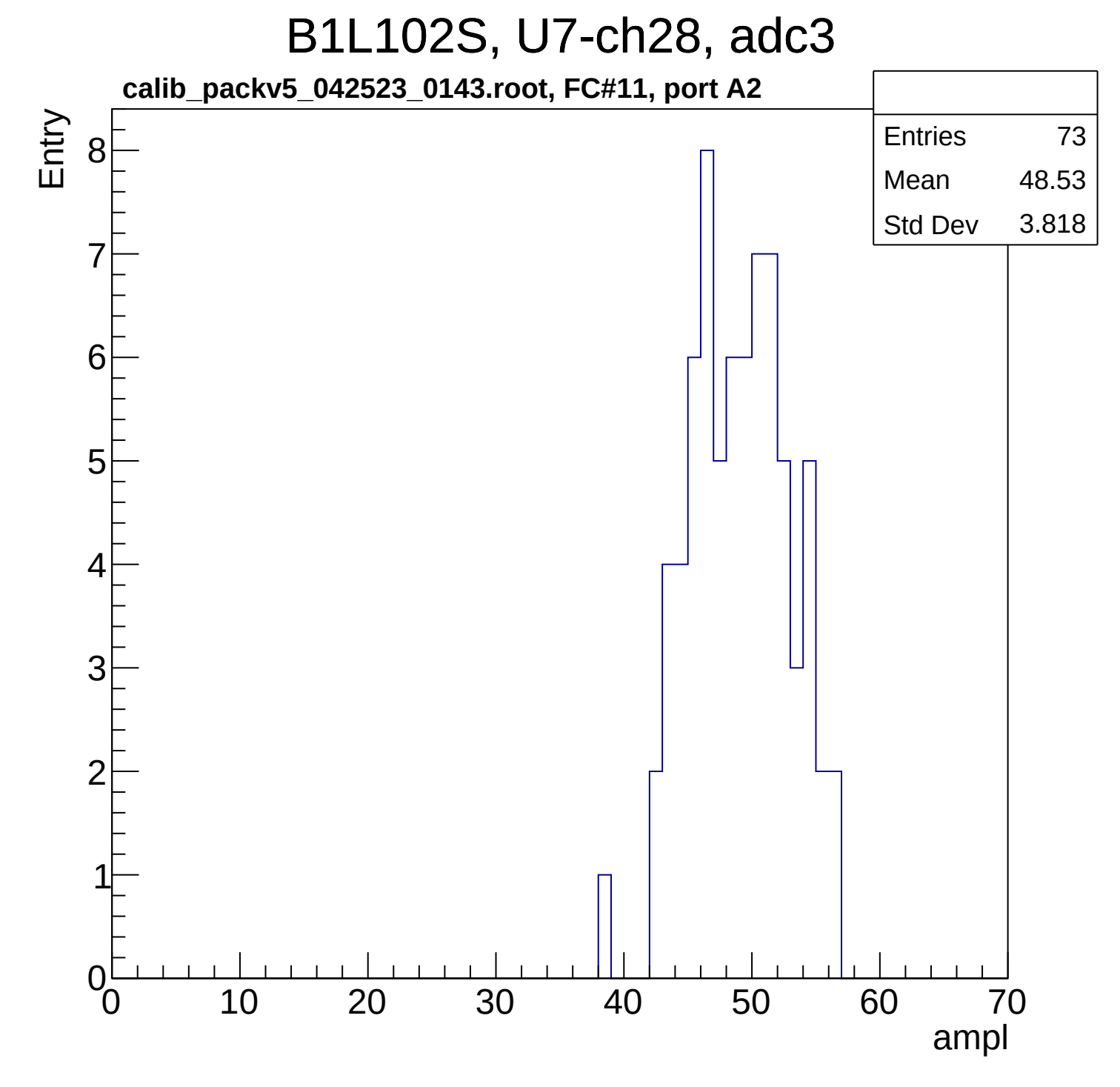
B1L102S, U7-ch28, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 73
Mean 48.53
Std Dev 3.818
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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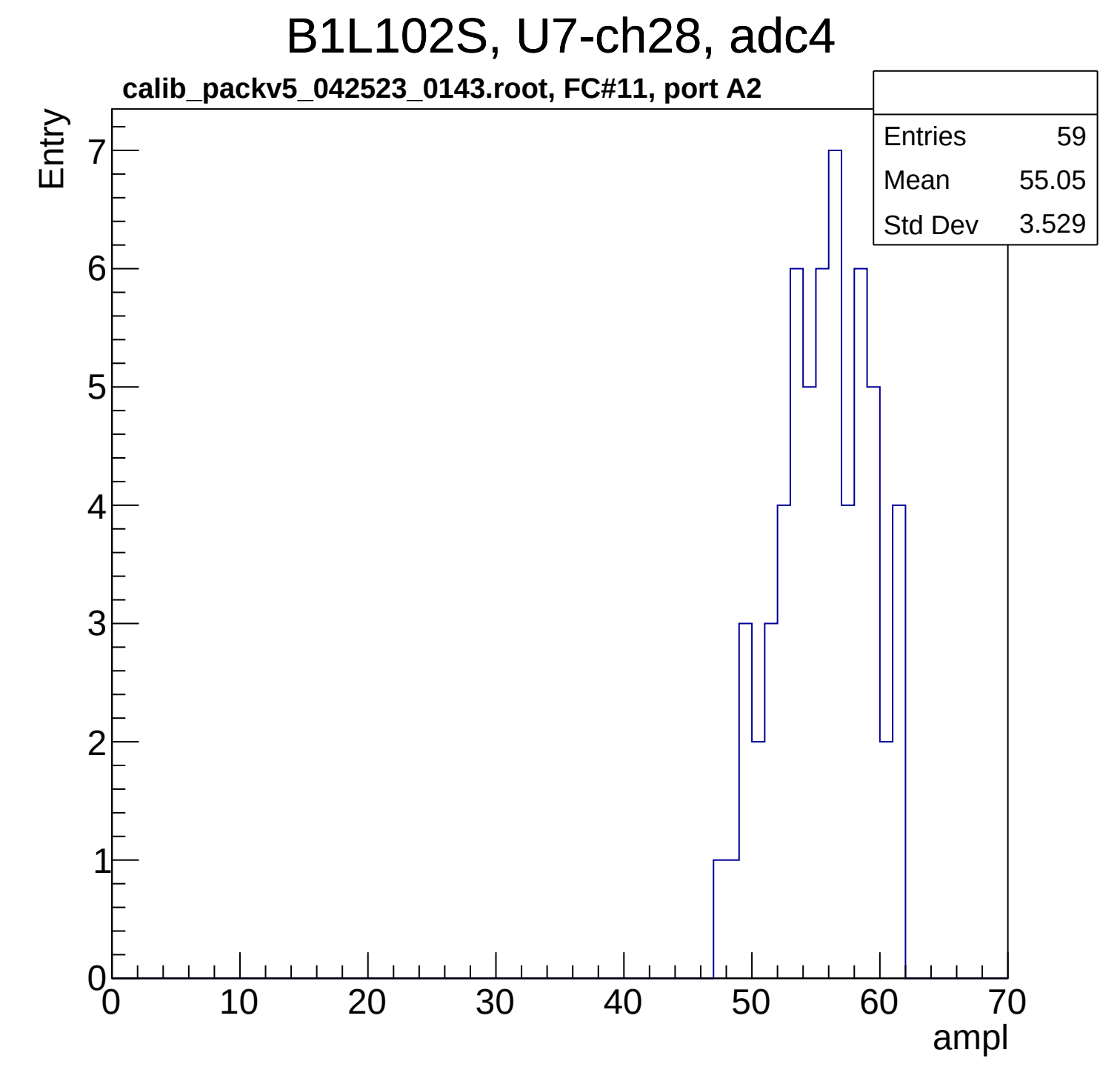
40
50
60
70


B1L102S, U7-ch28, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 59
Mean 55.05
Std Dev 3.529
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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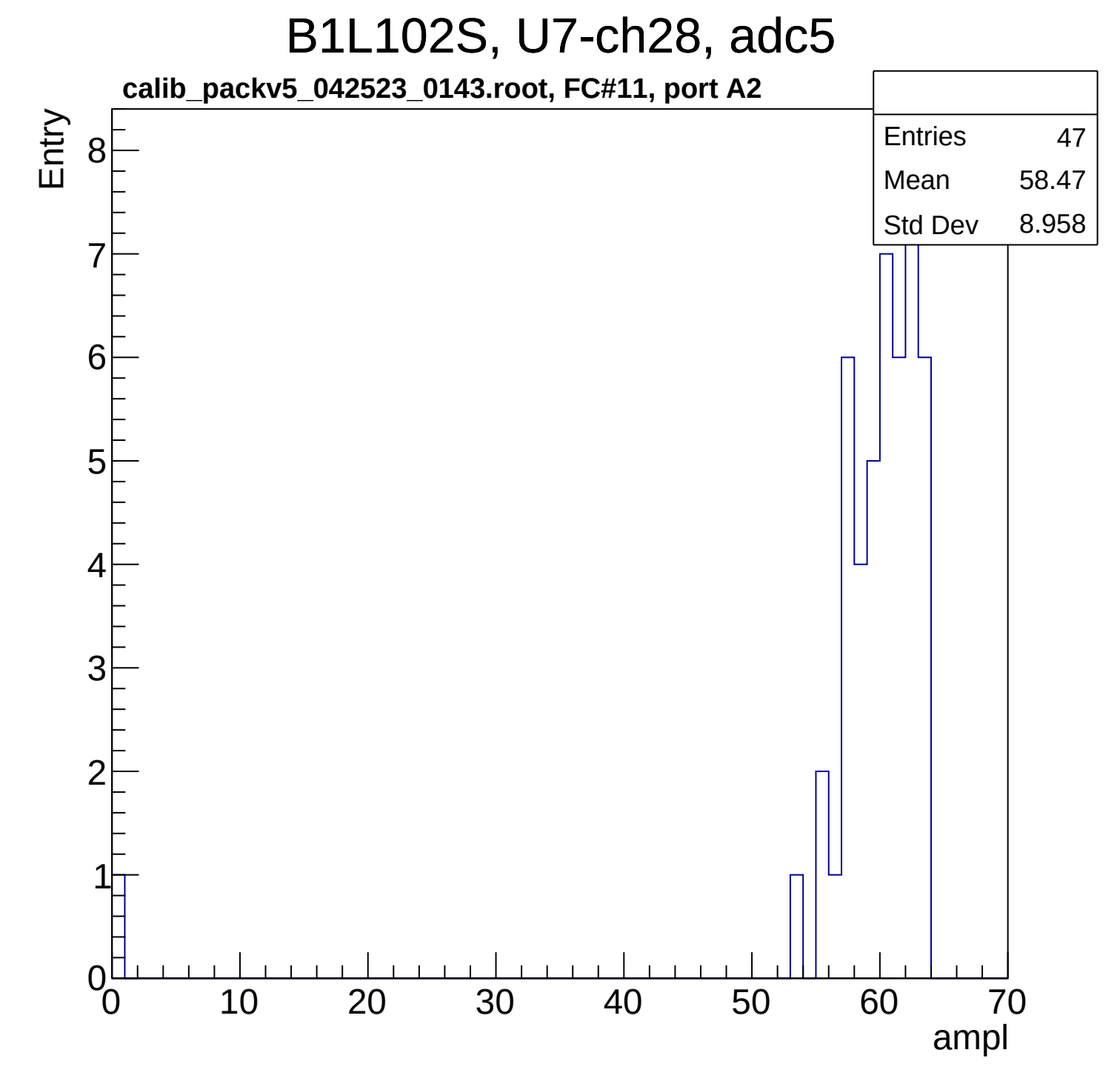
B1L102S, U7-ch28, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 47
Mean 58.47
Std Dev 8.958
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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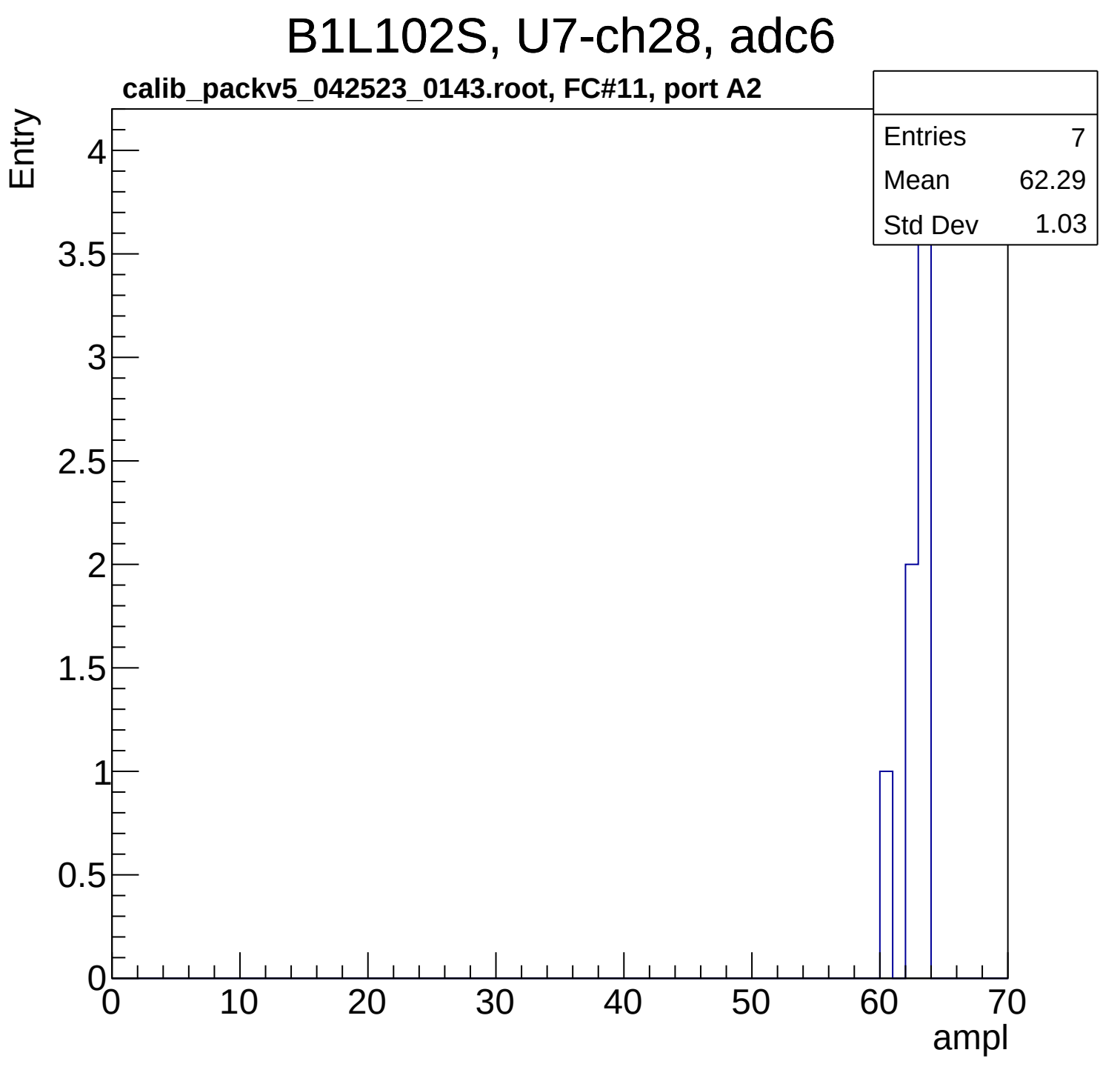
B1L102S, U7-ch28, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 7
Mean 62.29
Std Dev 1.03
Entry
ampl
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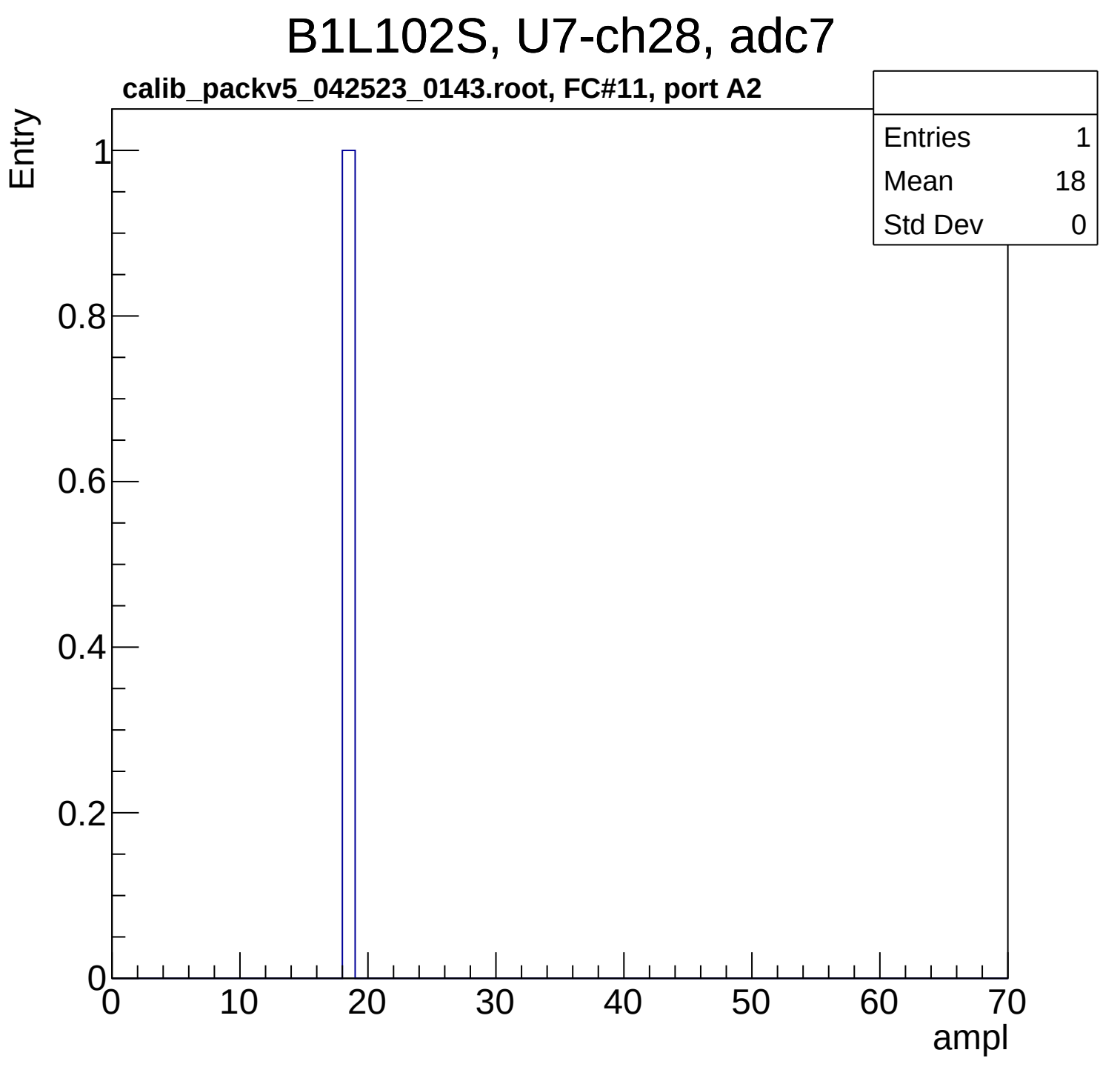
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L102S, U7-ch28, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 1
Mean 18
Std Dev 0
Entry
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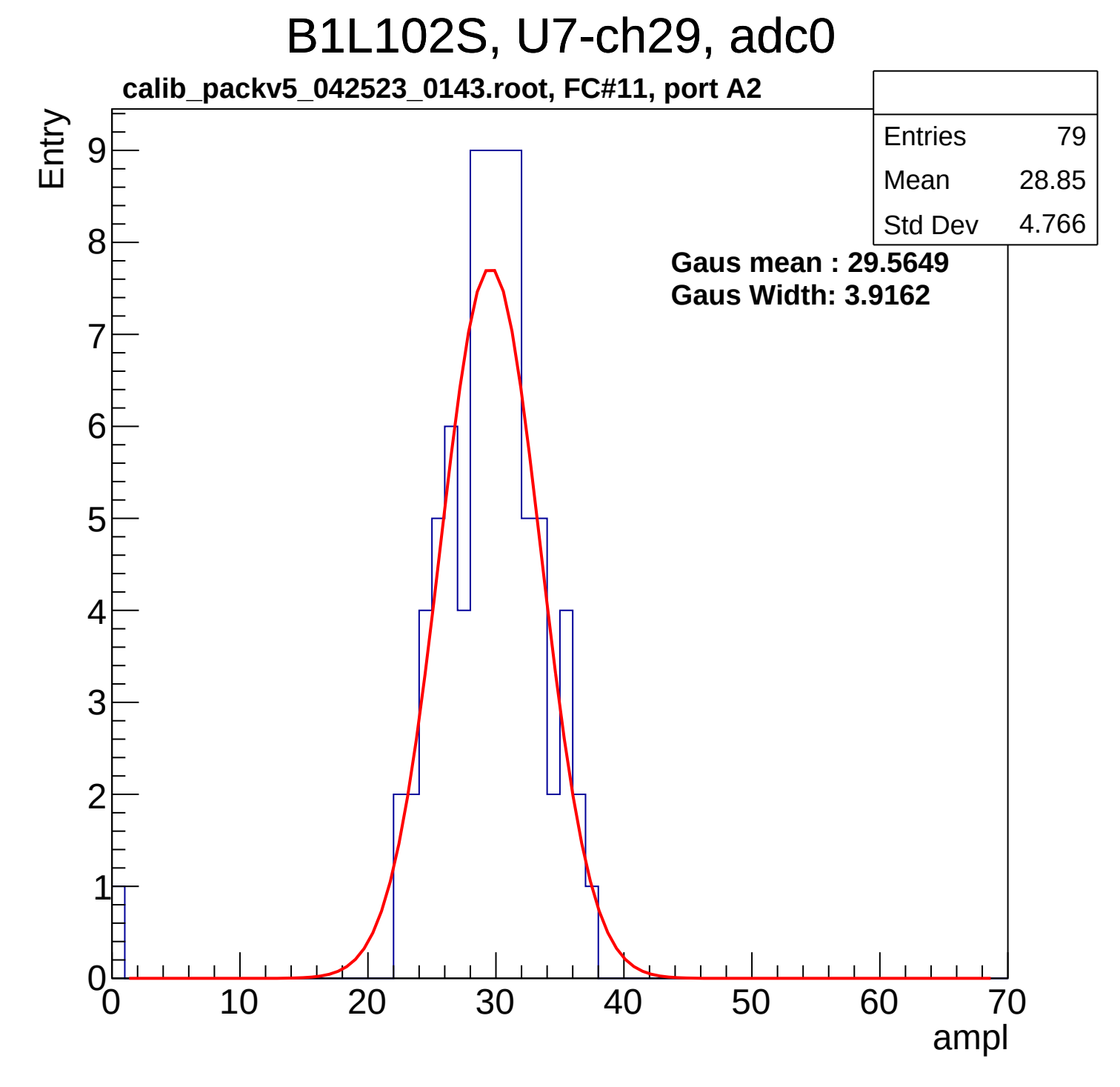
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U7-ch29, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 79
Mean 28.85
Std Dev 4.766
Gaus mean : 29.5649
Gaus Width: 3.9162
Entry
ampl
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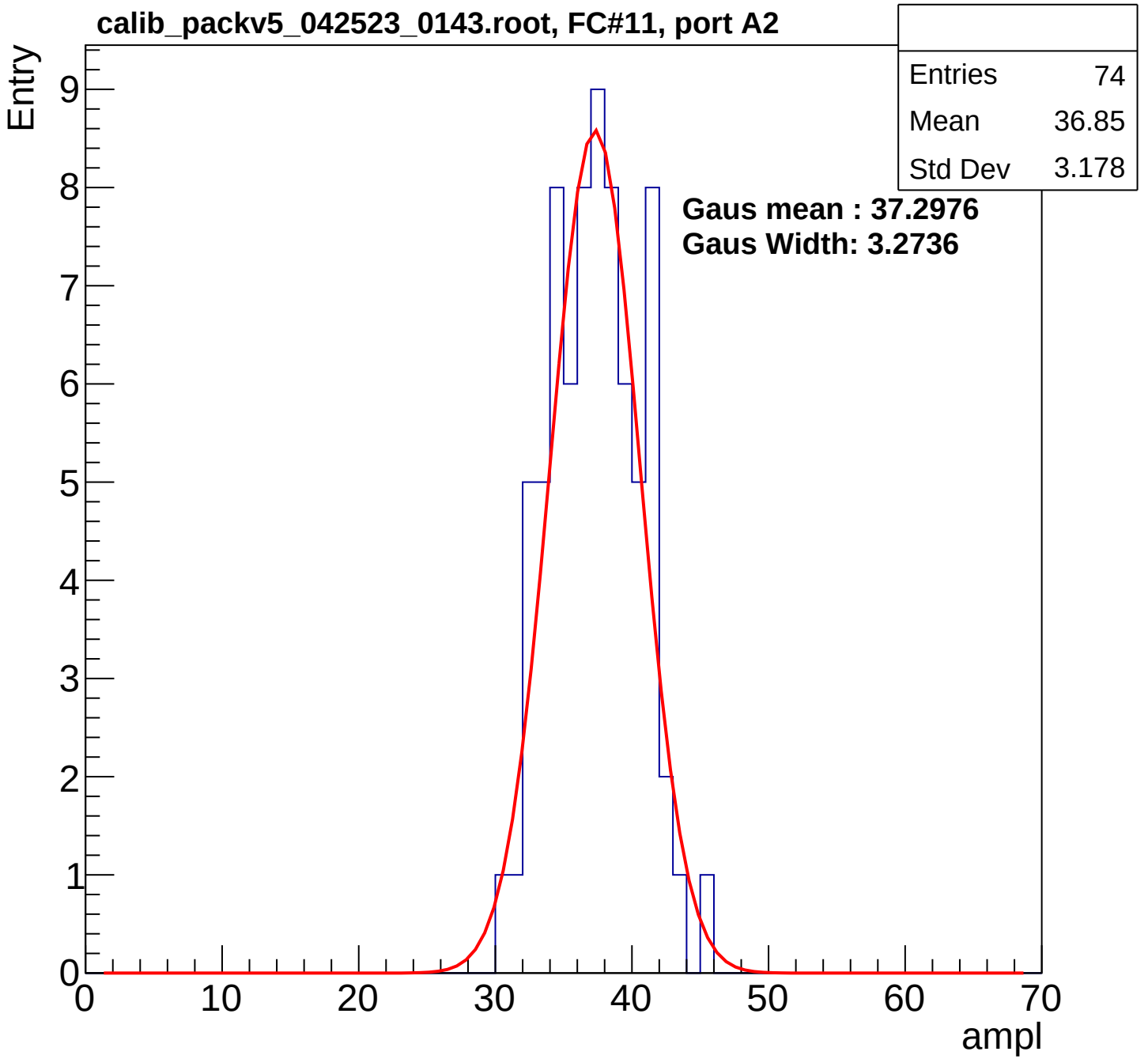
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L102S, U7-ch29, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 74
Mean 36.85
Std Dev 3.178
Gaus mean : 37.2976
Gaus Width: 3.2736
Entry
ampl
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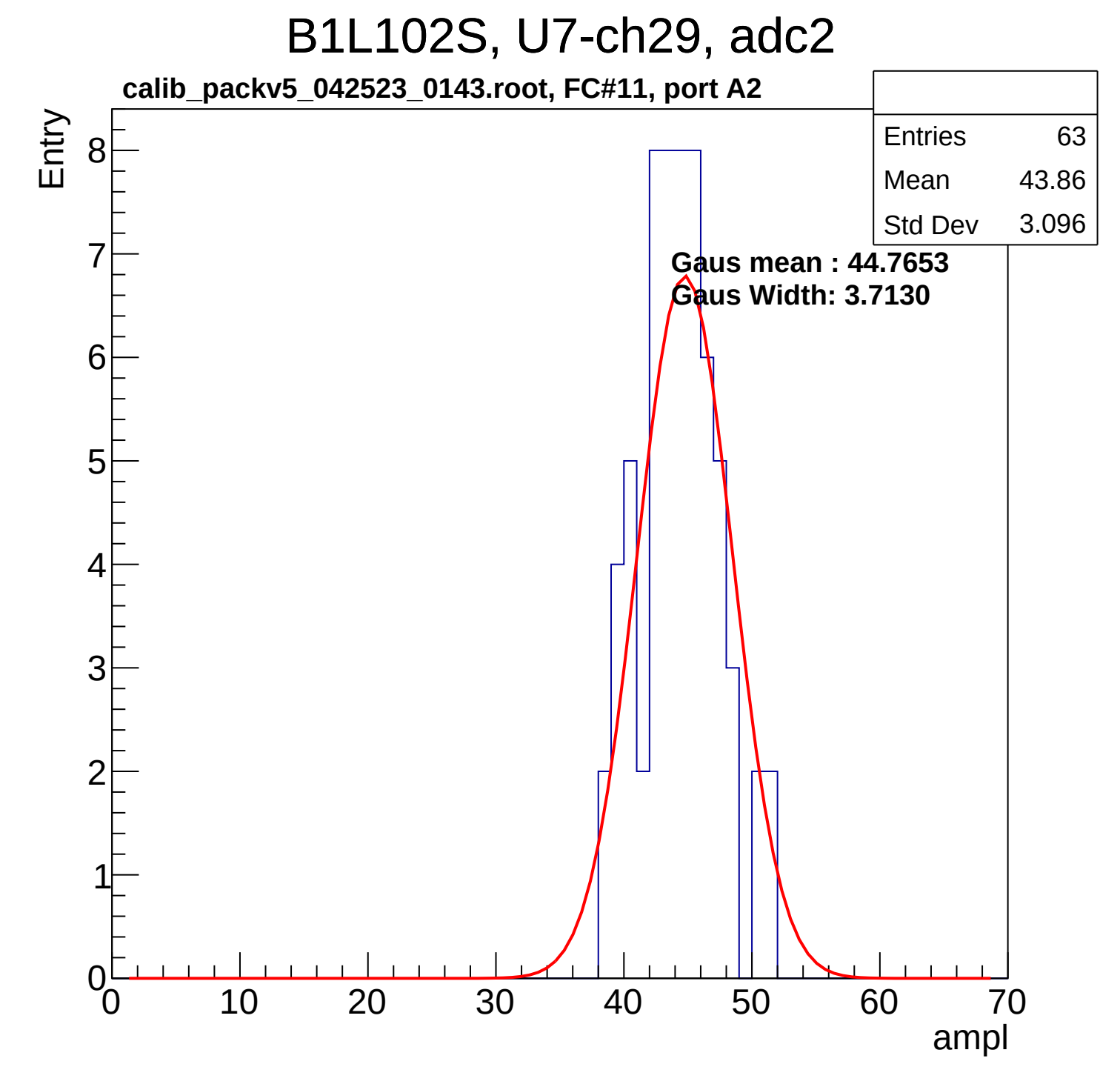
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L102S, U7-ch29, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 63
Mean 43.86
Std Dev 3.096
Gaus mean : 44.7653
Gaus Width: 3.7130
Entry
ampl
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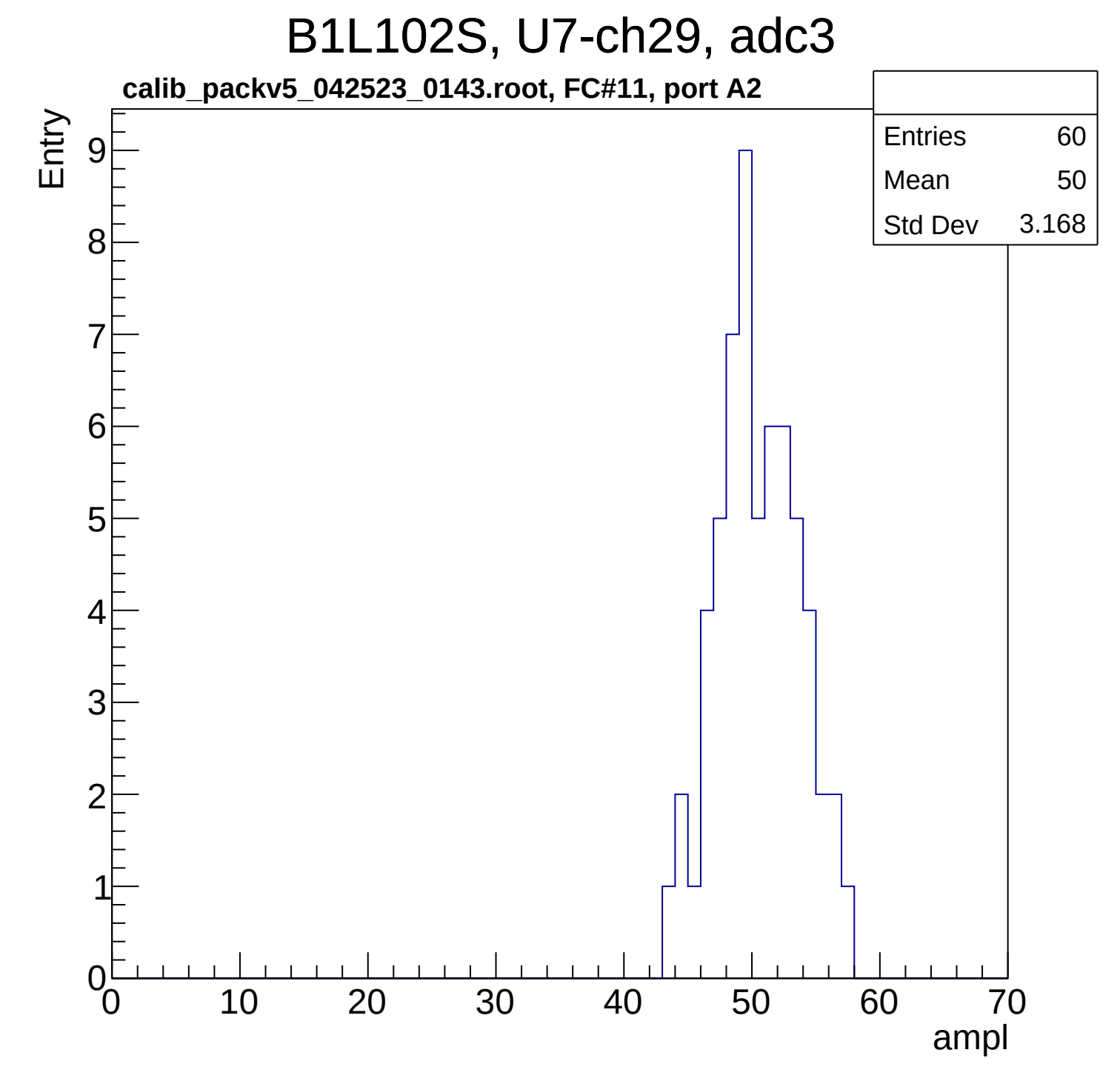
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L102S, U7-ch29, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 60
Mean 50
Std Dev 3.168
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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40
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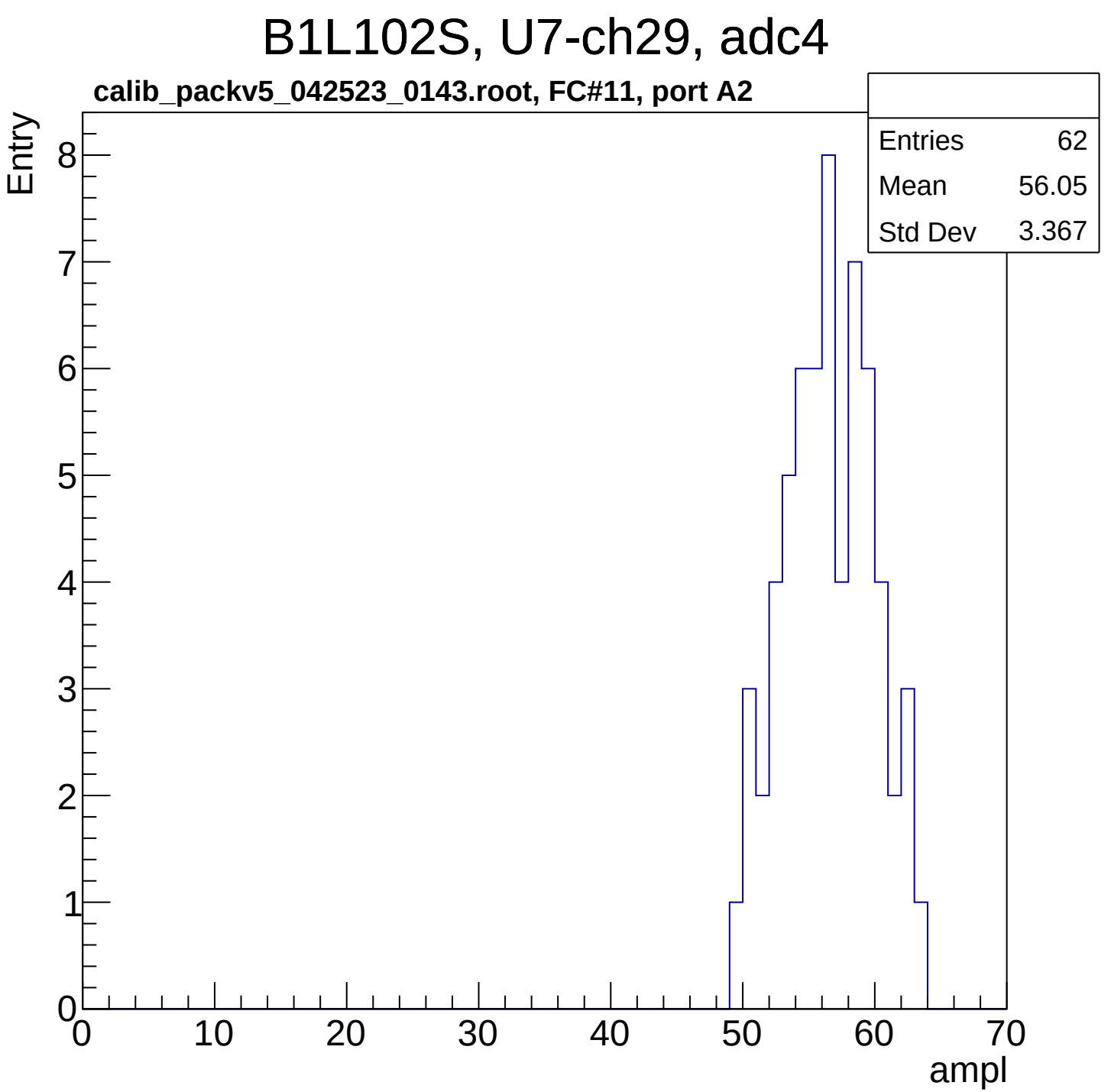
60
70


B1L102S, U7-ch29, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 62
Mean 56.05
Std Dev 3.367
Entry
ampl
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2
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4
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60
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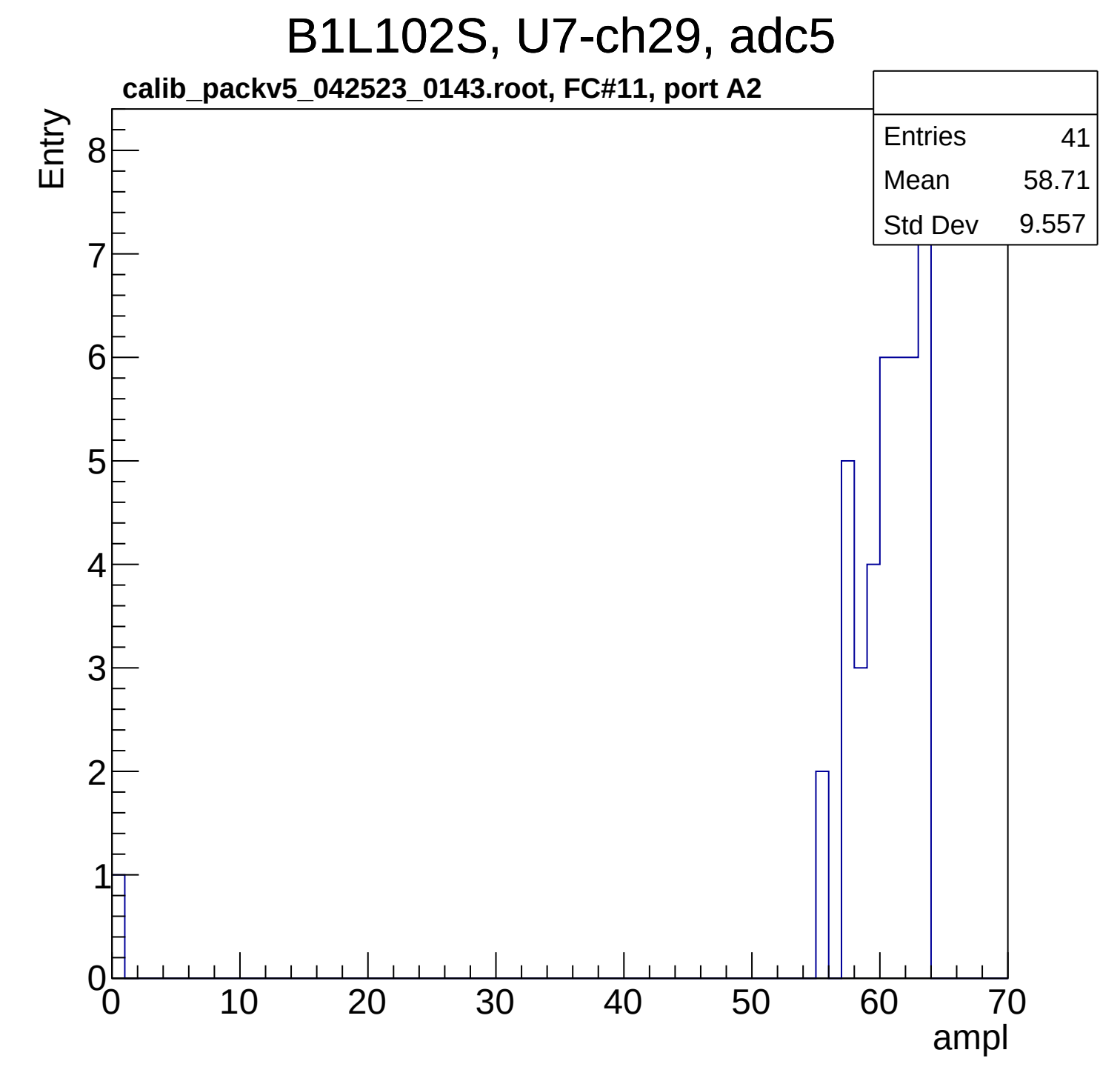
B1L102S, U7-ch29, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 41
Mean 58.71
Std Dev 9.557
Entry
ampl
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1
2
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4
5
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7
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0
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60
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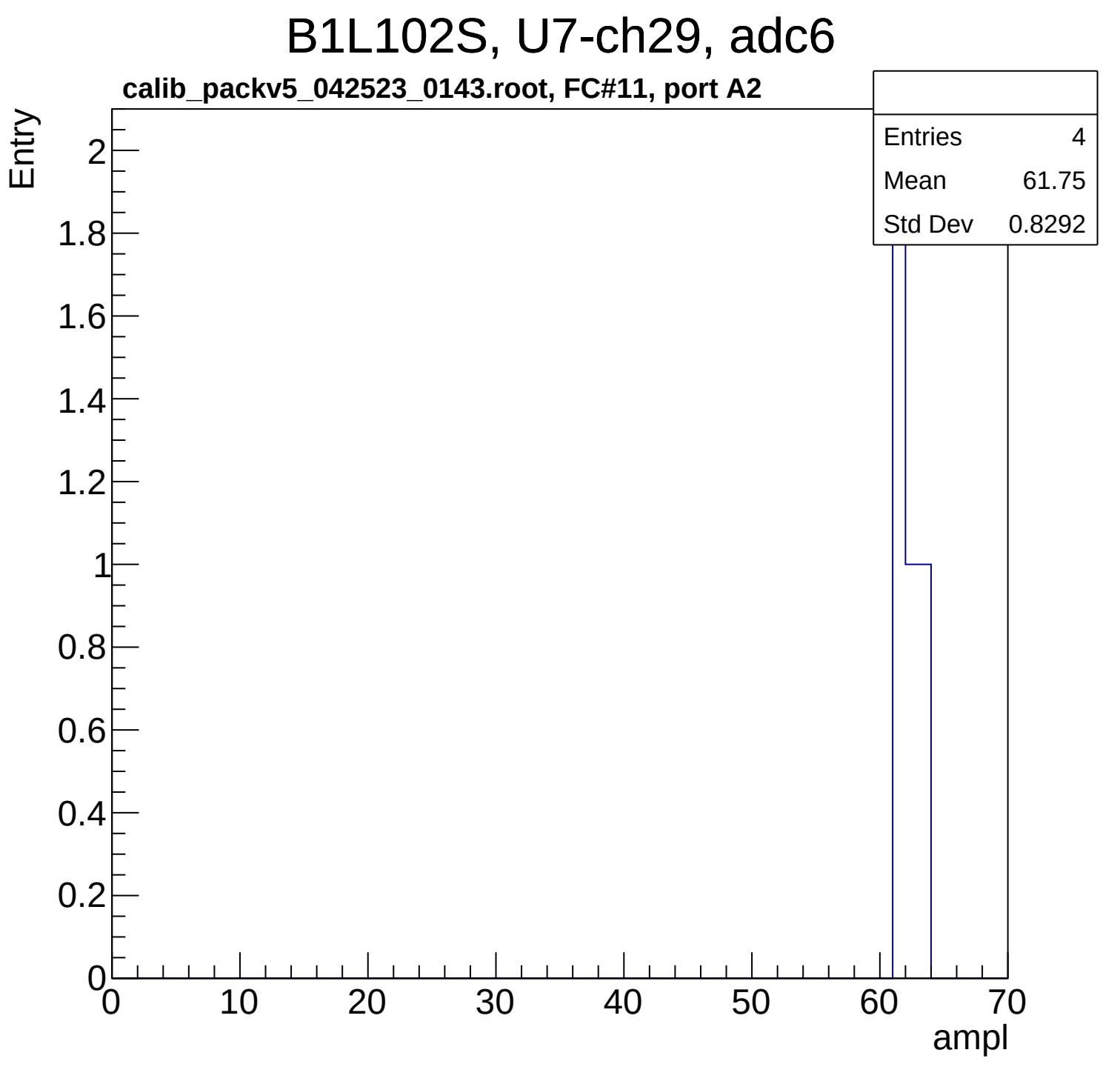
B1L102S, U7-ch29, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 4
Mean 61.75
Std Dev 0.8292
Entry
ampl
0
0.2
0.4
0.6
0.8
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1.2
1.4
1.6
1.8
2
0
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40
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60
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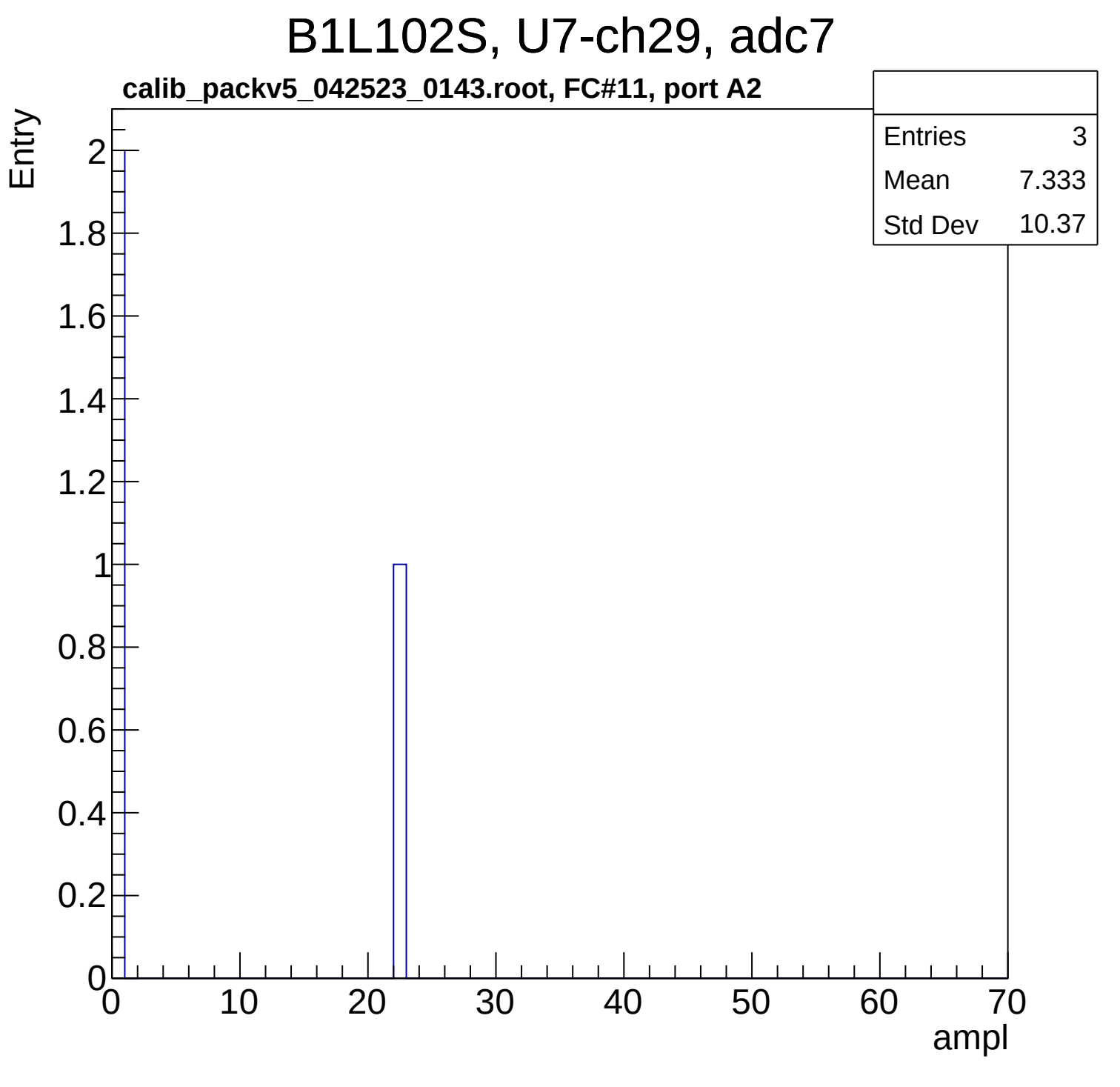
B1L102S, U7-ch29, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 3
Mean 7.333
Std Dev 10.37
Entry
ampl
0
0.2
0.4
0.6
0.8
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1.2
1.4
1.6
1.8
2
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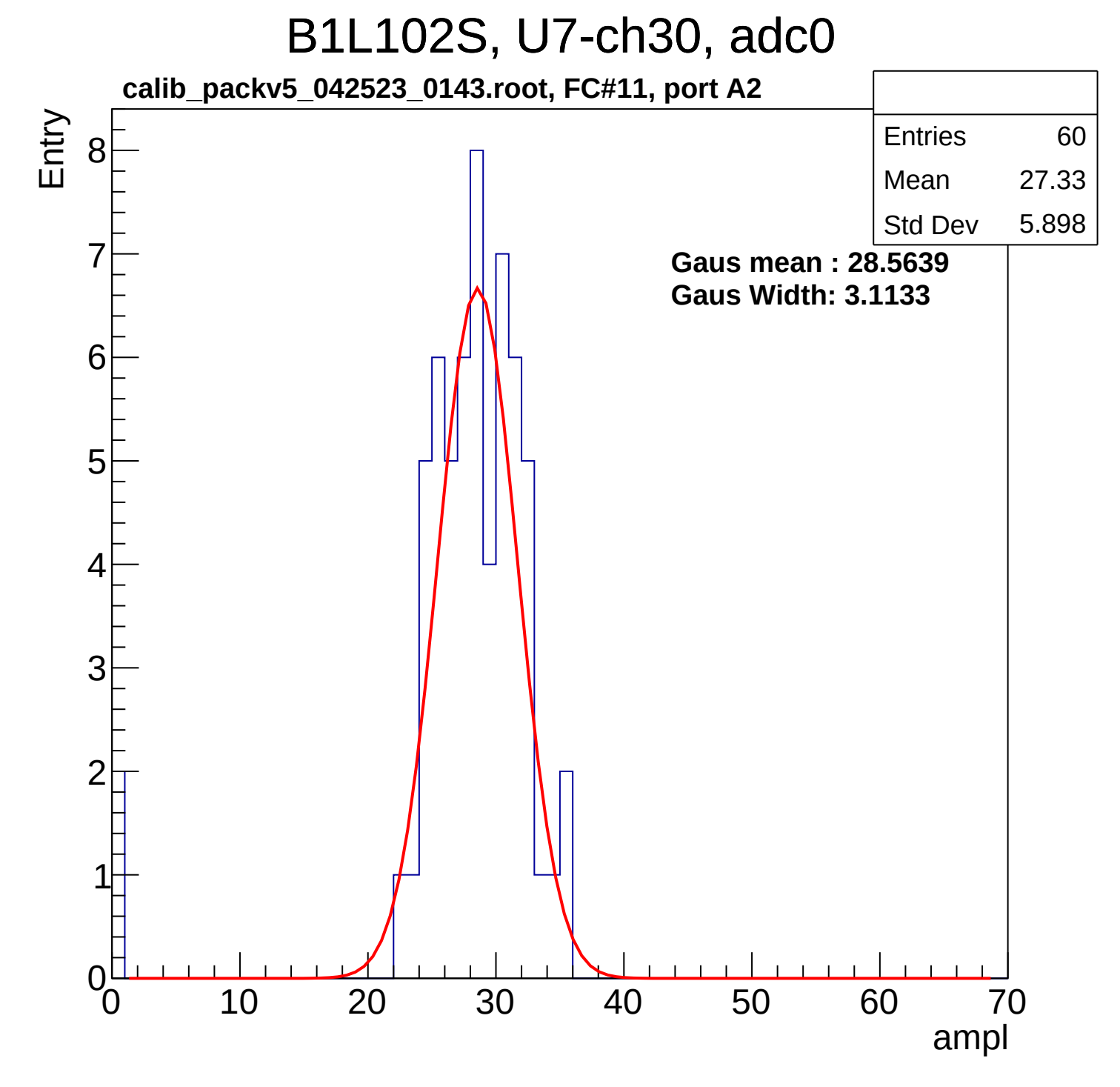
B1L102S, U7-ch30, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 60
Mean 27.33
Std Dev 5.898
Gaus mean : 28.5639
Gaus Width: 3.1133
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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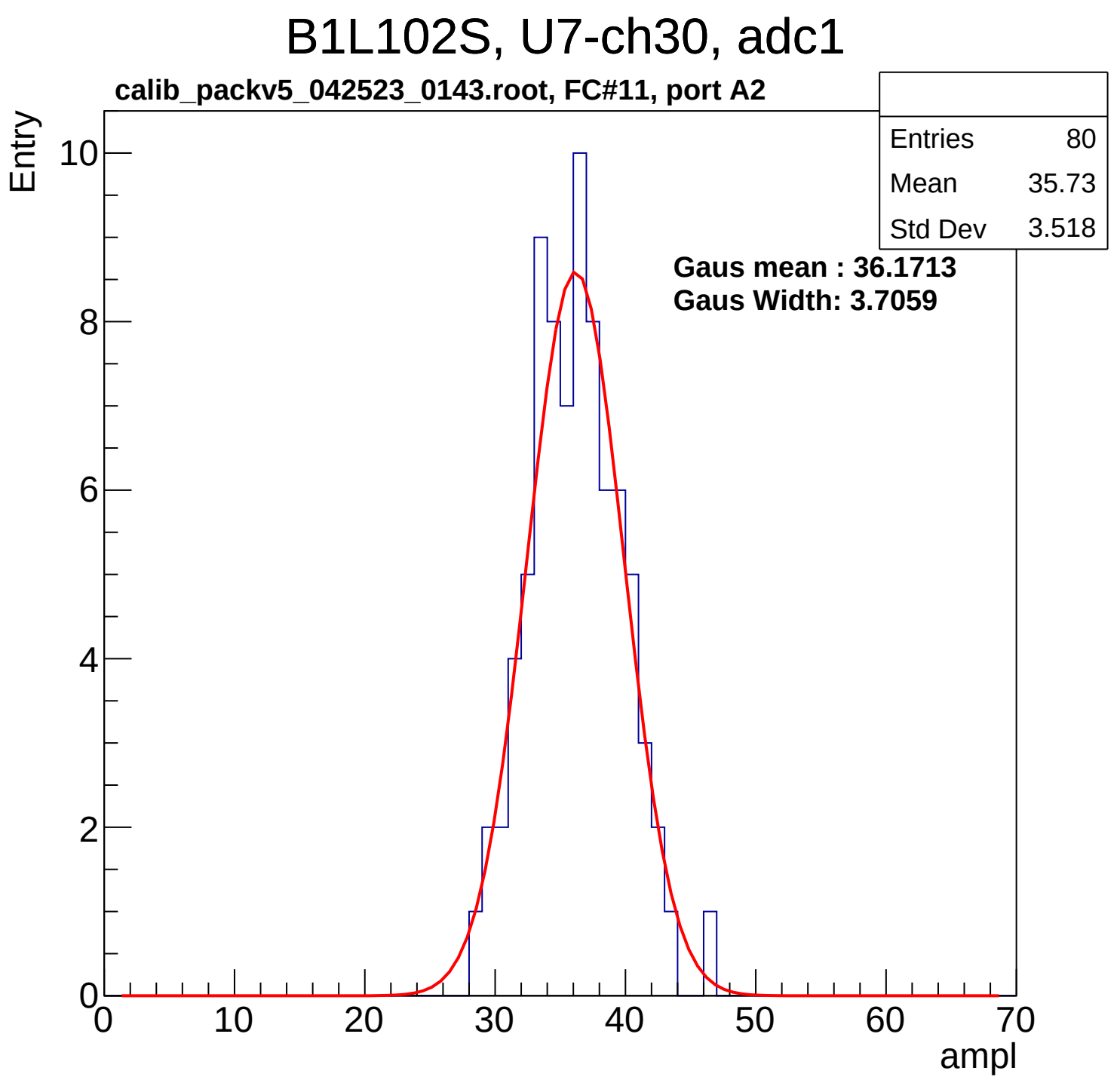
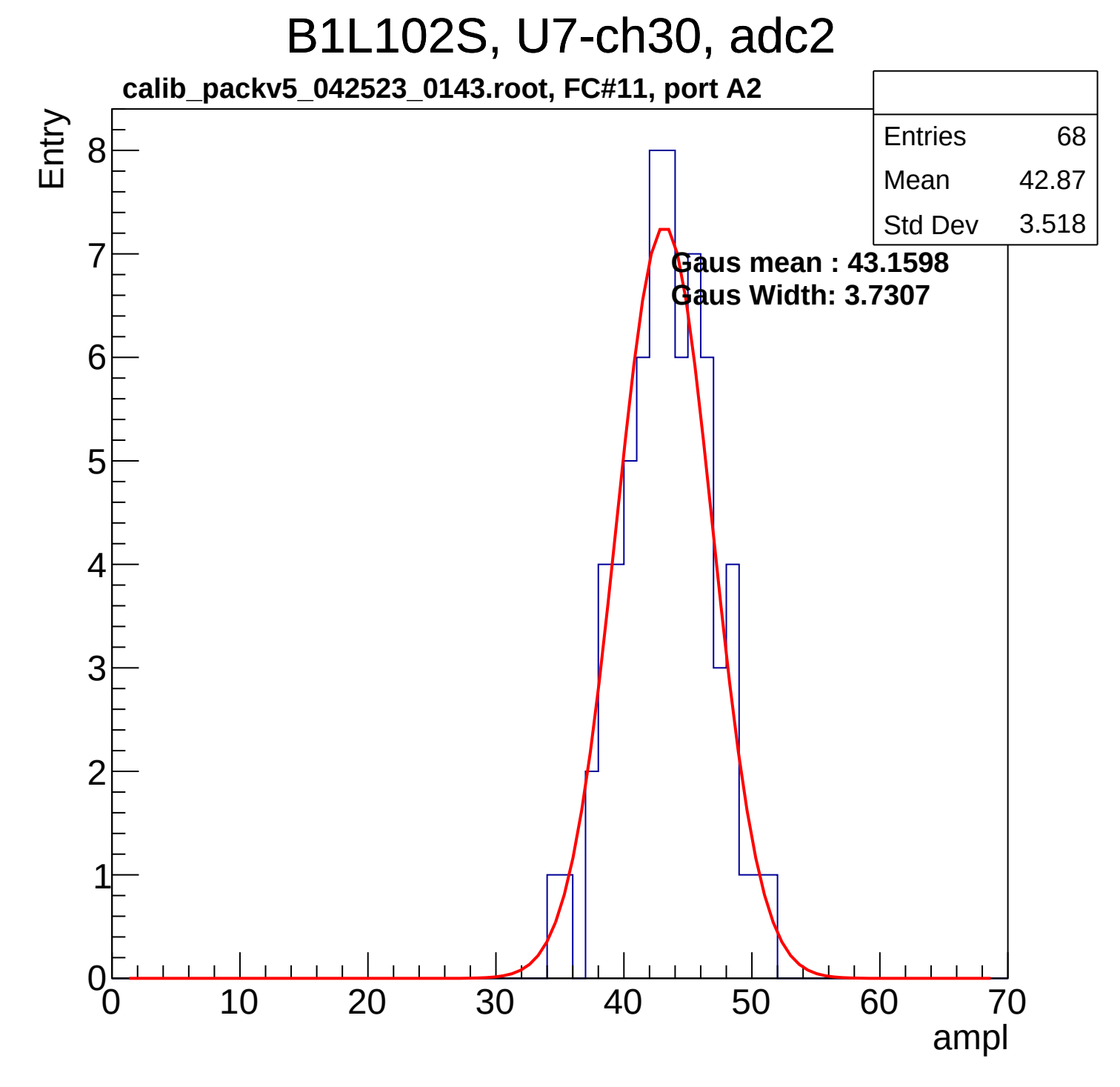
40
50
60
70


B1L102S, U7-ch30, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 80
Mean 35.73
Std Dev 3.518
Gaus mean : 36.1713
Gaus Width: 3.7059
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L102S, U7-ch30, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 68
Mean 42.87
Std Dev 3.518
Gaus mean : 43.1598
Gaus Width: 3.7307
Entry
ampl
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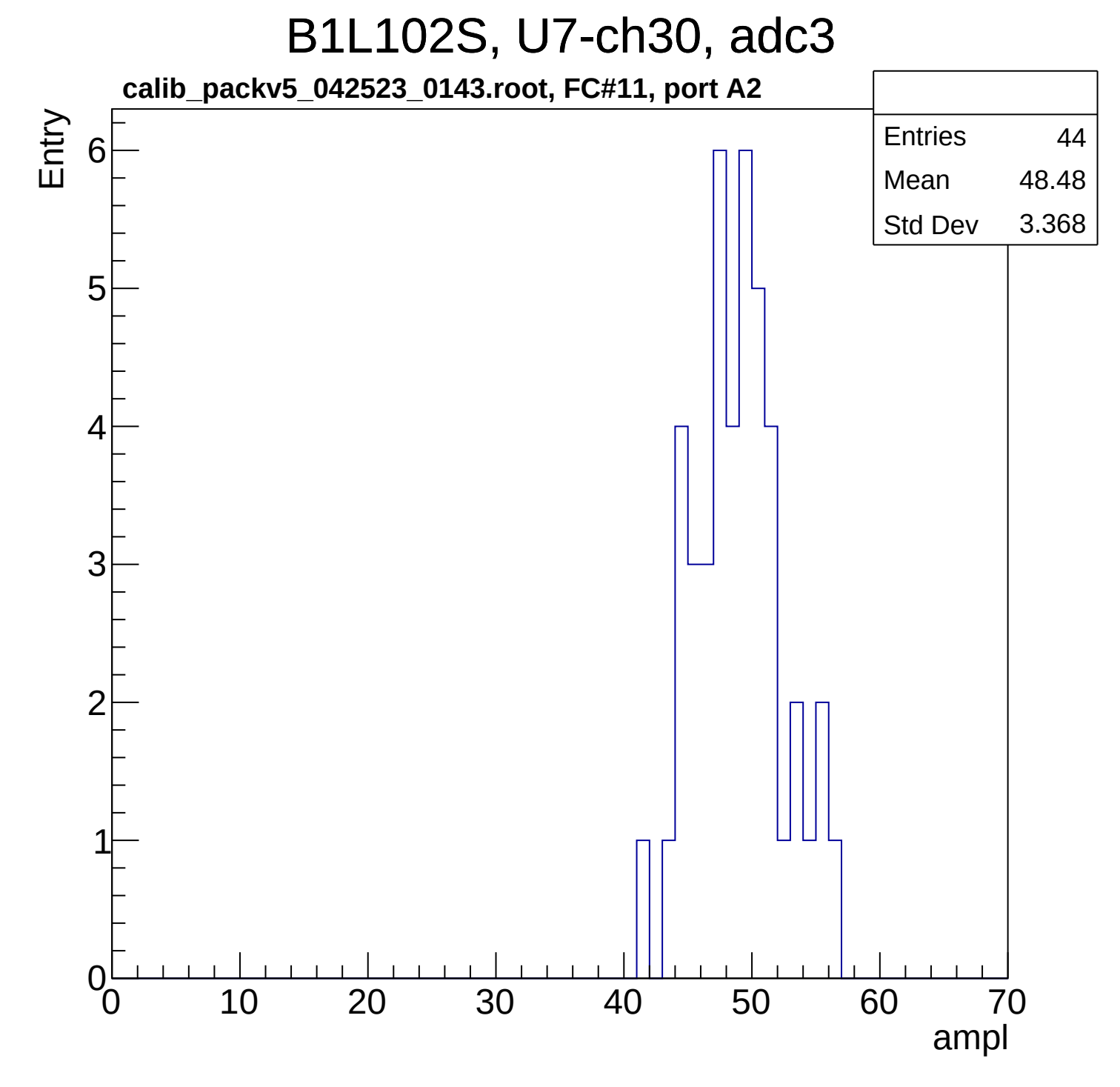
B1L102S, U7-ch30, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 44
Mean 48.48
Std Dev 3.368
Entry
ampl
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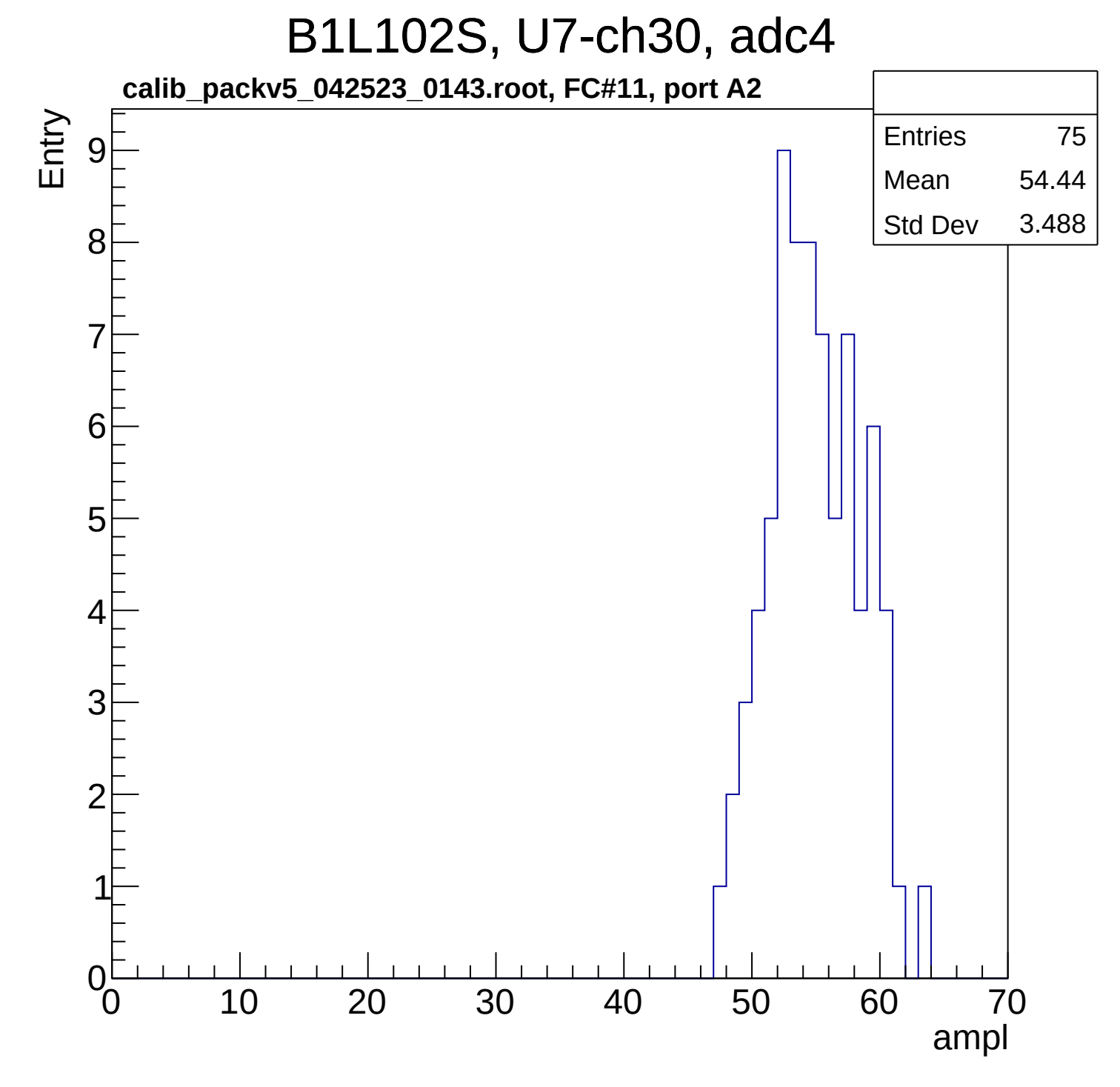
B1L102S, U7-ch30, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 75
Mean 54.44
Std Dev 3.488
Entry
ampl
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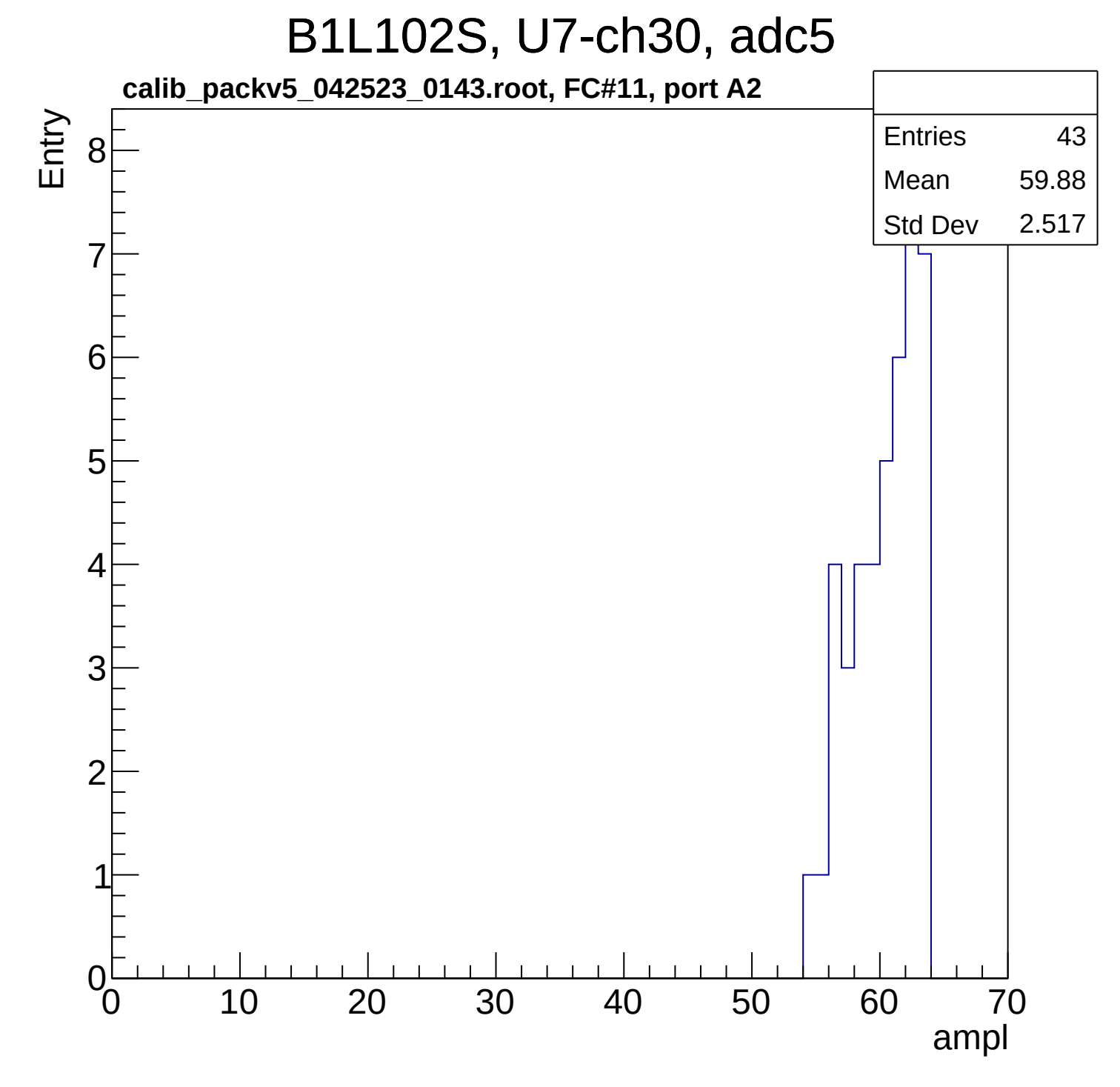
B1L102S, U7-ch30, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 43
Mean 59.88
Std Dev 2.517
Entry
ampl
0
1
2
3
4
5
6
7
8
0
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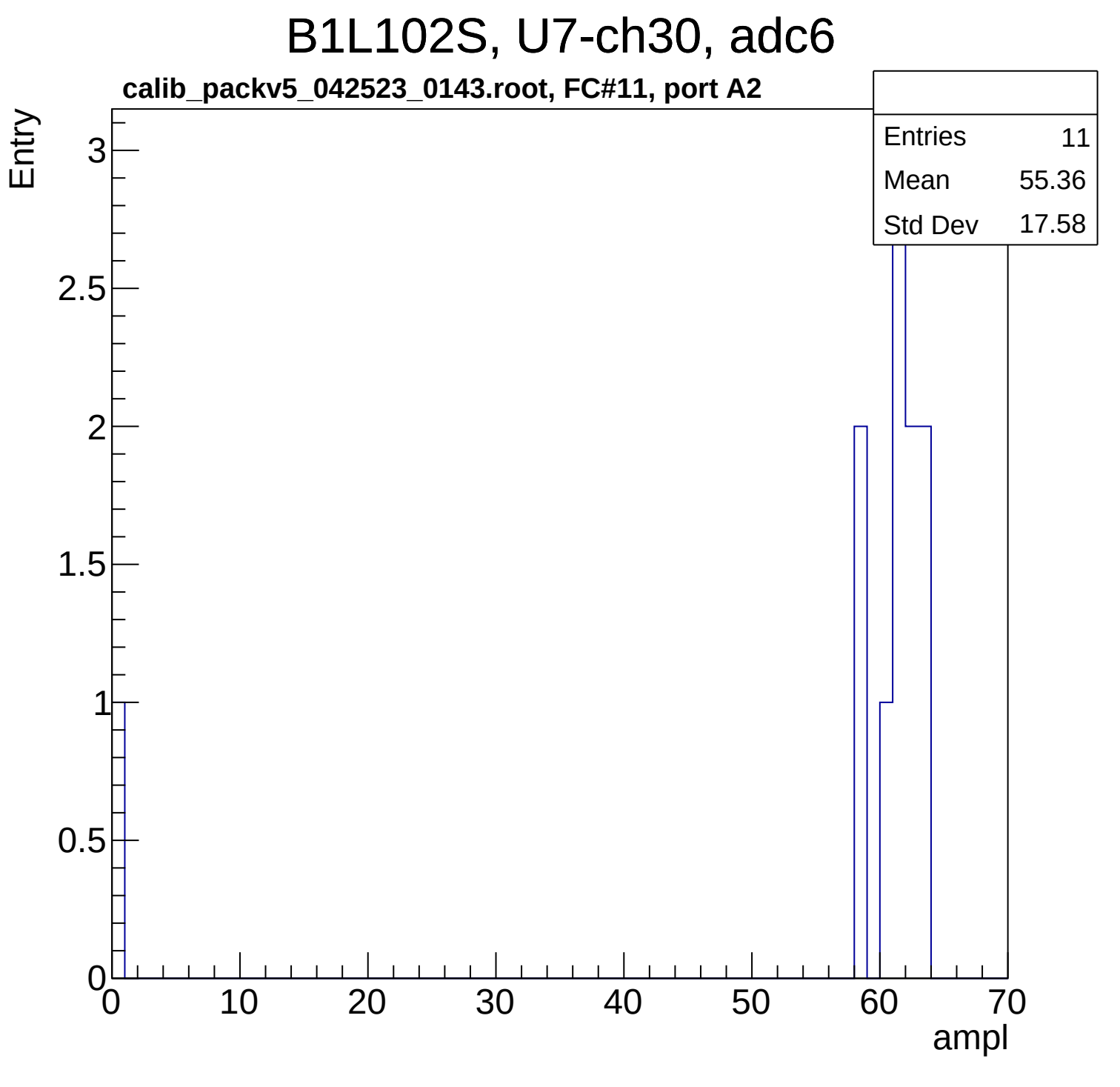
40
50
60
70


B1L102S, U7-ch30, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 11
Mean 55.36
Std Dev 17.58
Entry
ampl
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0.5
1
1.5
2
2.5
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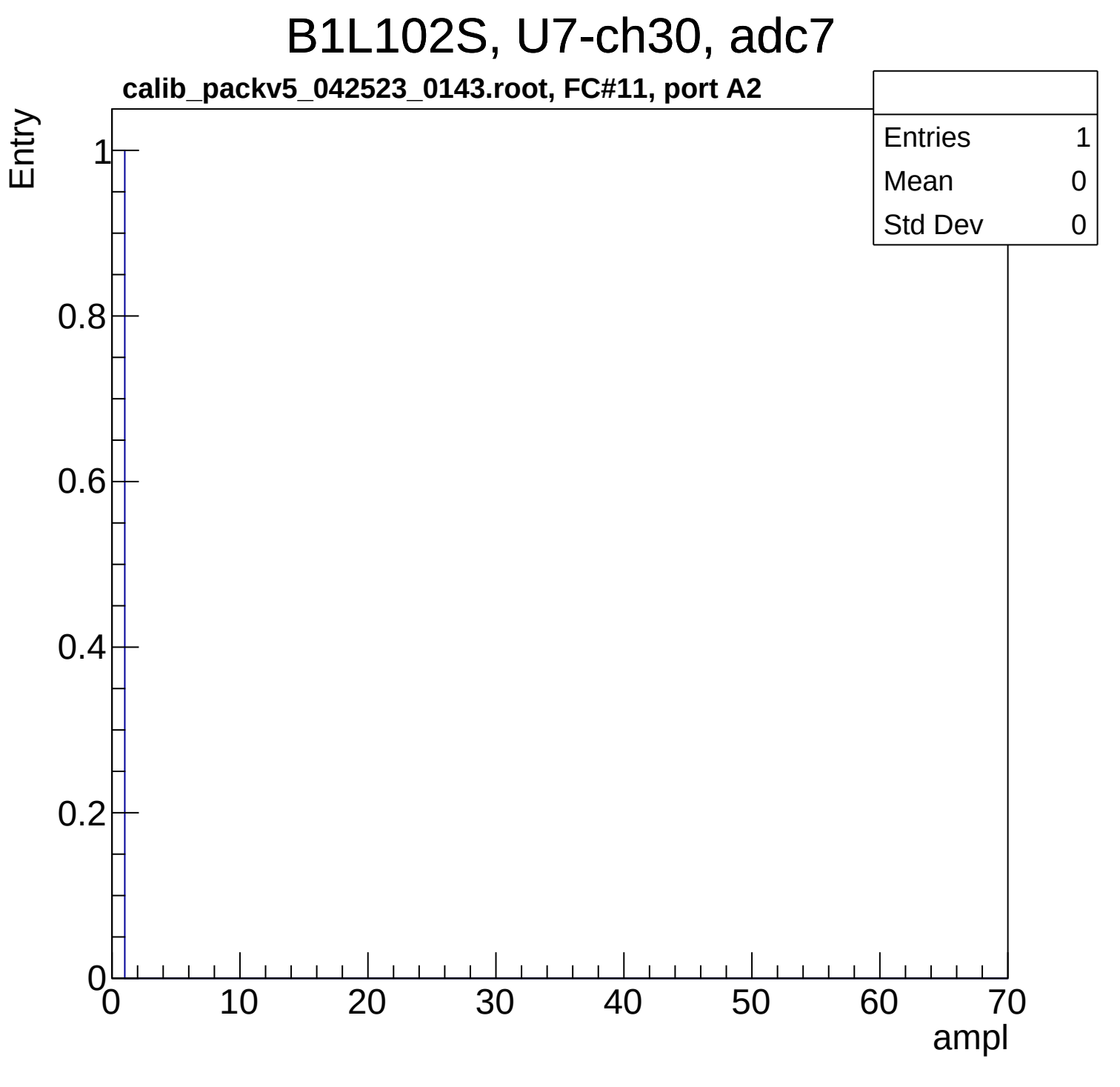
B1L102S, U7-ch30, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
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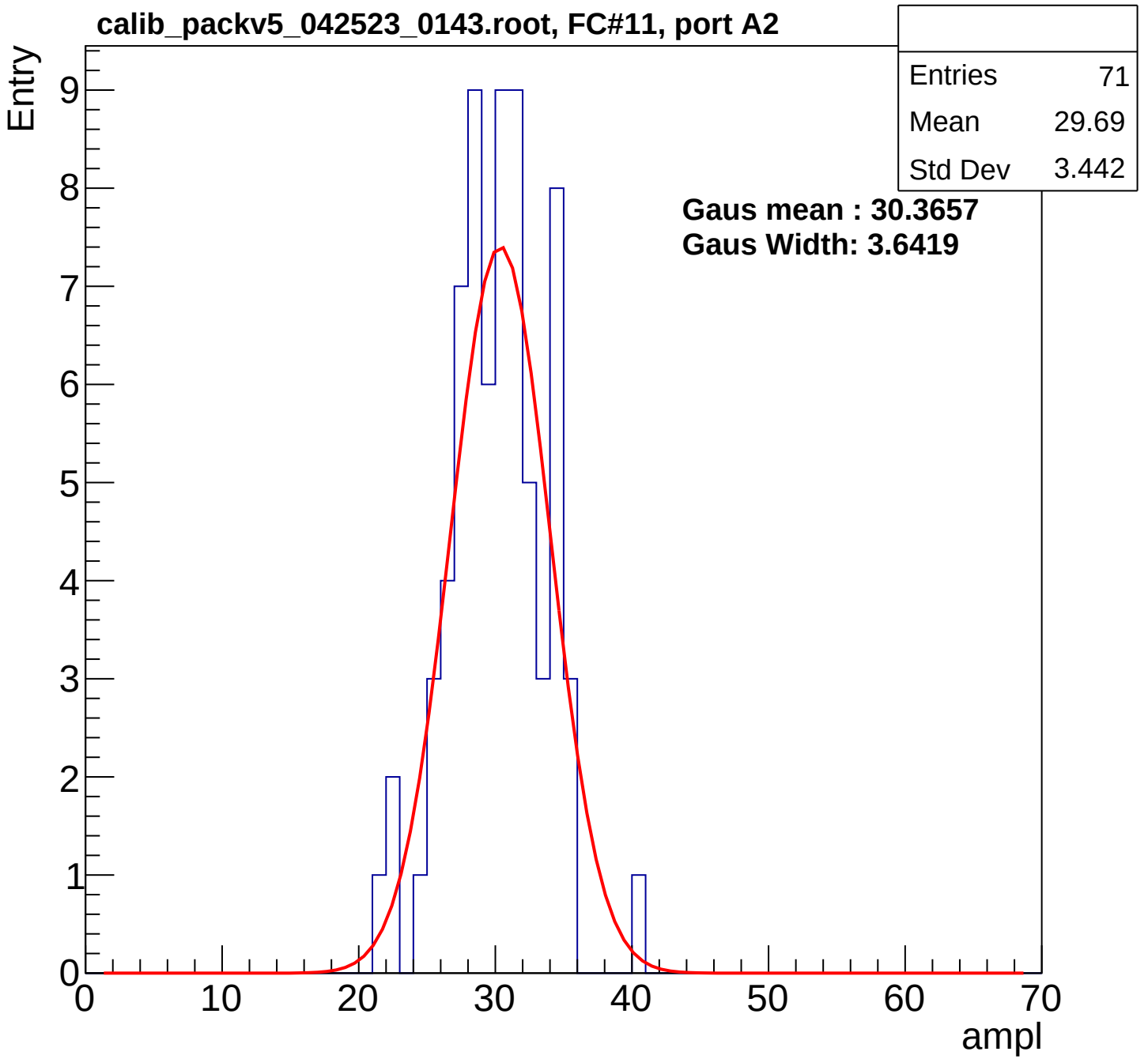
30
40
50
60
70
ampl


B1L102S, U7-ch31, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 71
Mean 29.69
Std Dev 3.442
Gaus mean : 30.3657
Gaus Width: 3.6419
Entry
ampl
0
10
20
30
40
50
60
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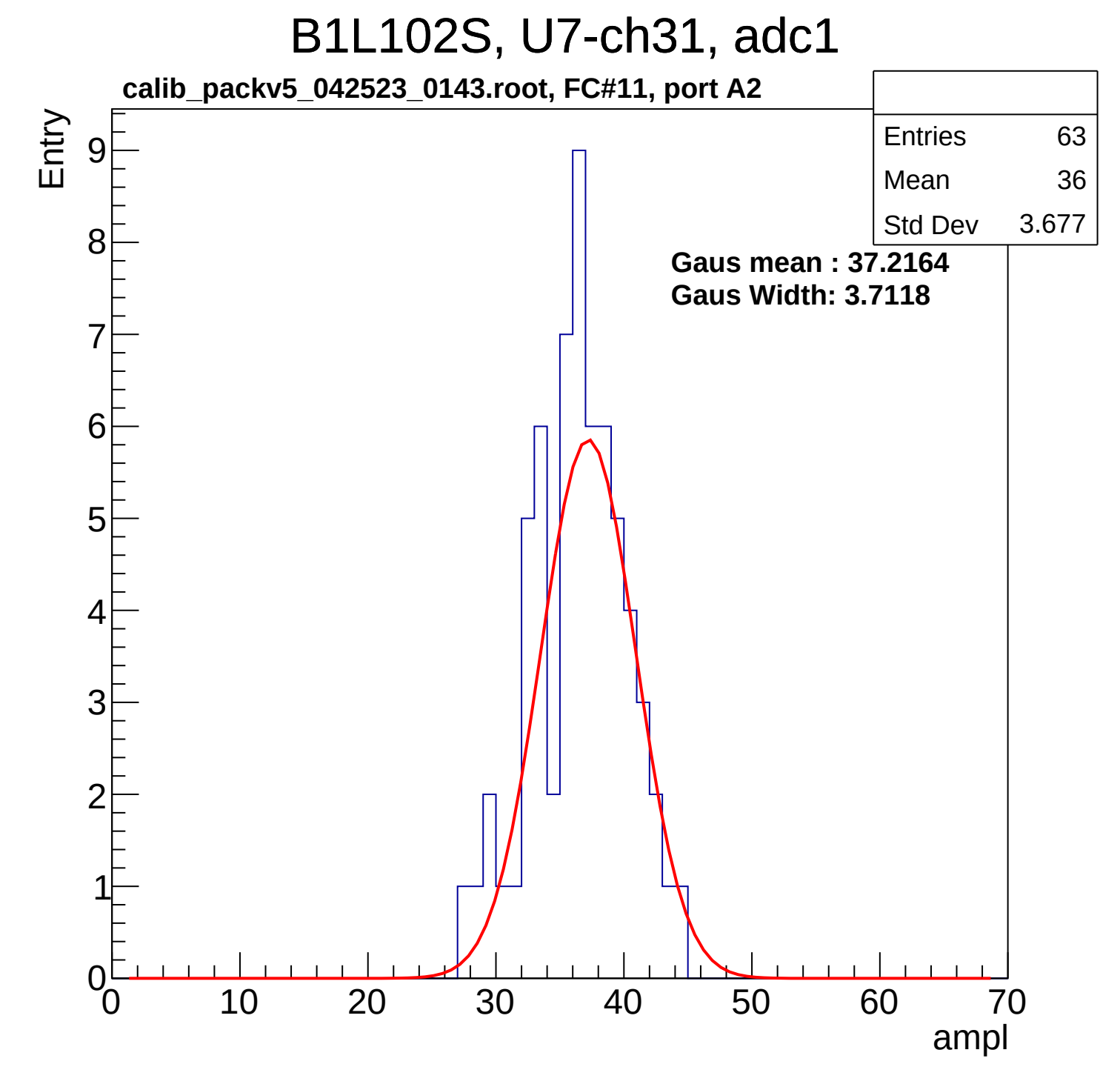
1
2
3
4
5
6
7
8
9


B1L102S, U7-ch31, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 63
Mean 36
Std Dev 3.677
Gaus mean : 37.2164
Gaus Width: 3.7118
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
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40
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60
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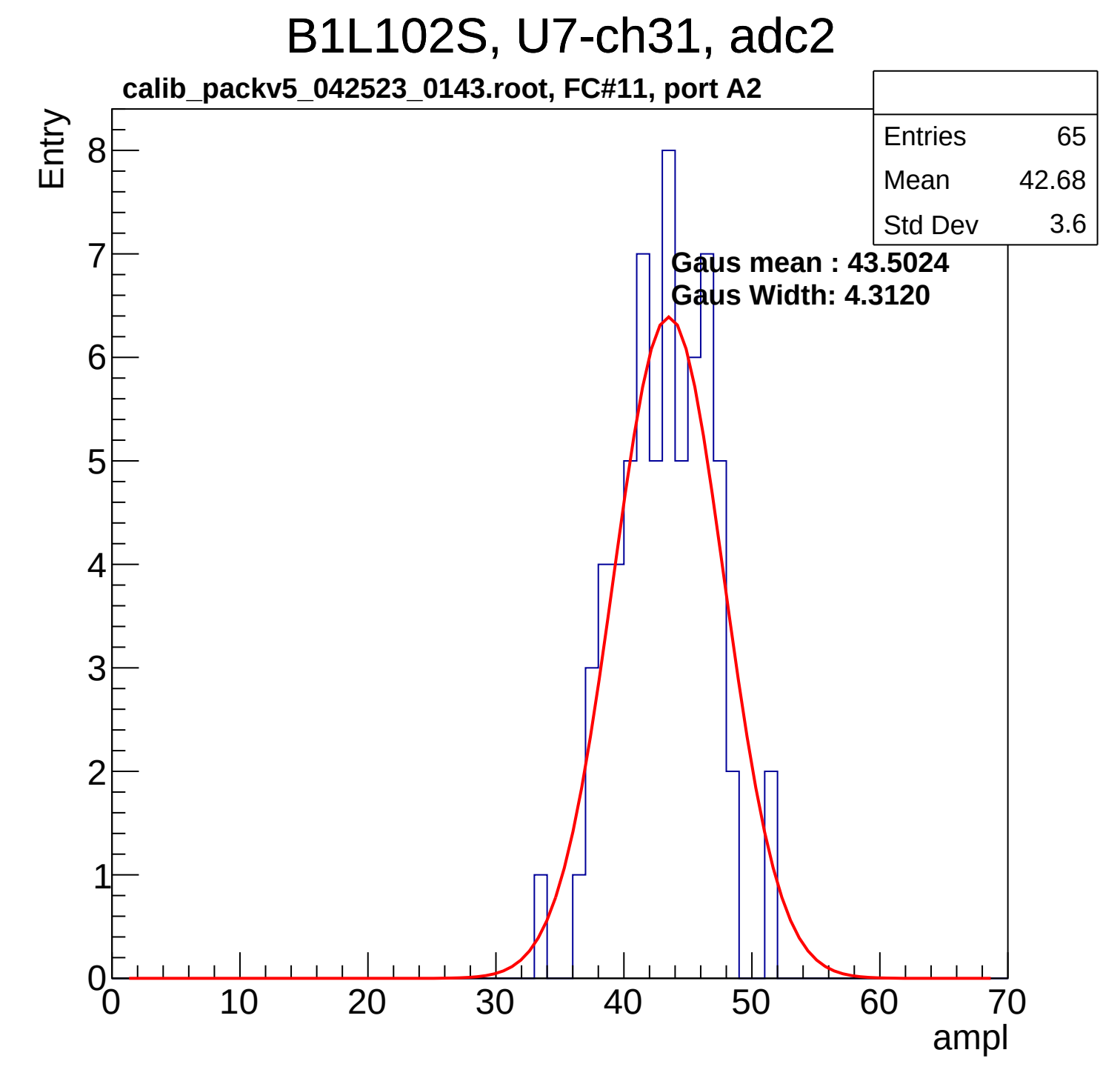
B1L102S, U7-ch31, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 65
Mean 42.68
Std Dev 3.6
Gaus mean : 43.5024
Gaus Width: 4.3120
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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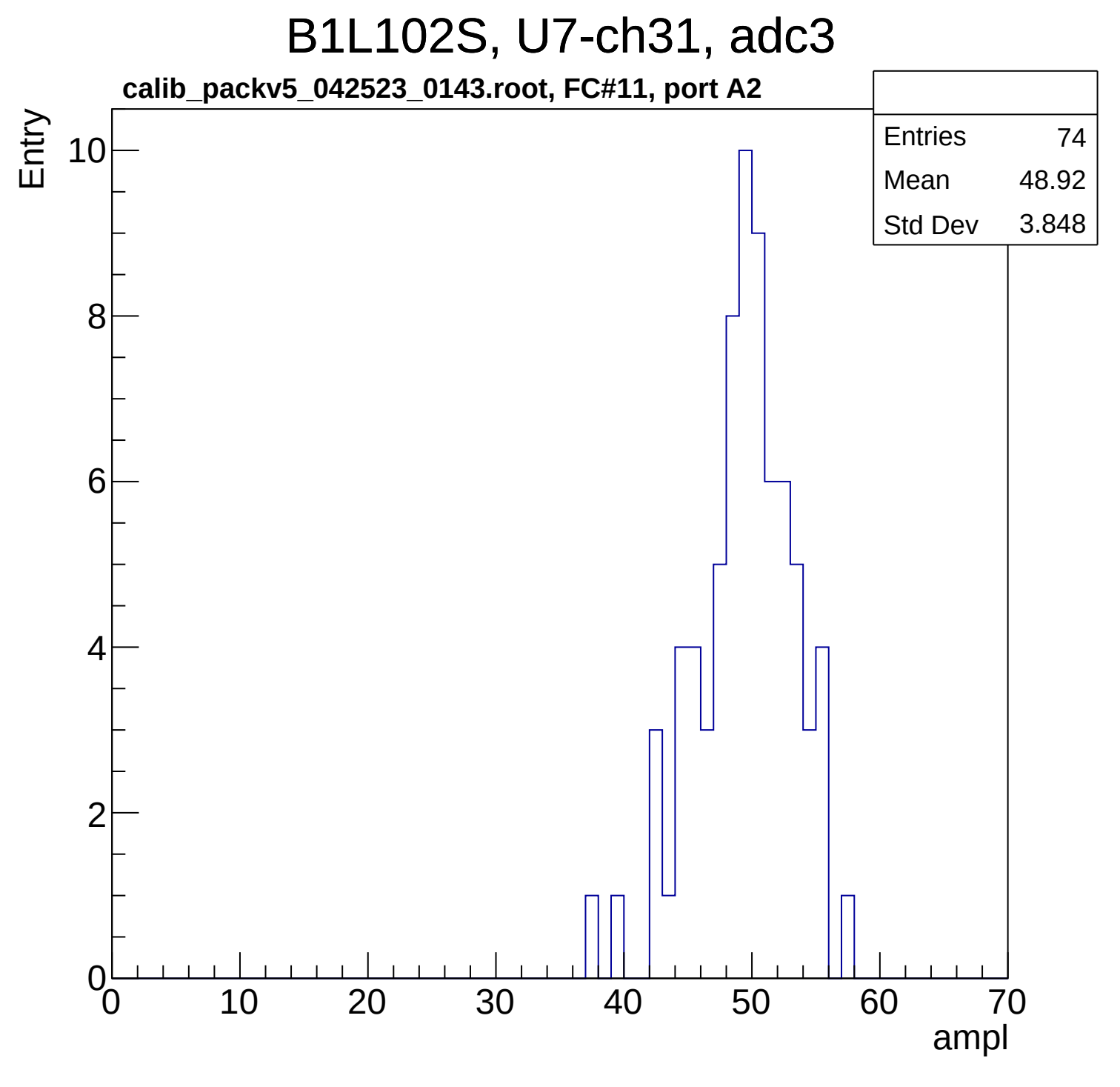
B1L102S, U7-ch31, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 74
Mean 48.92
Std Dev 3.848
Entry
ampl
0
2
4
6
8
10
0
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40
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60
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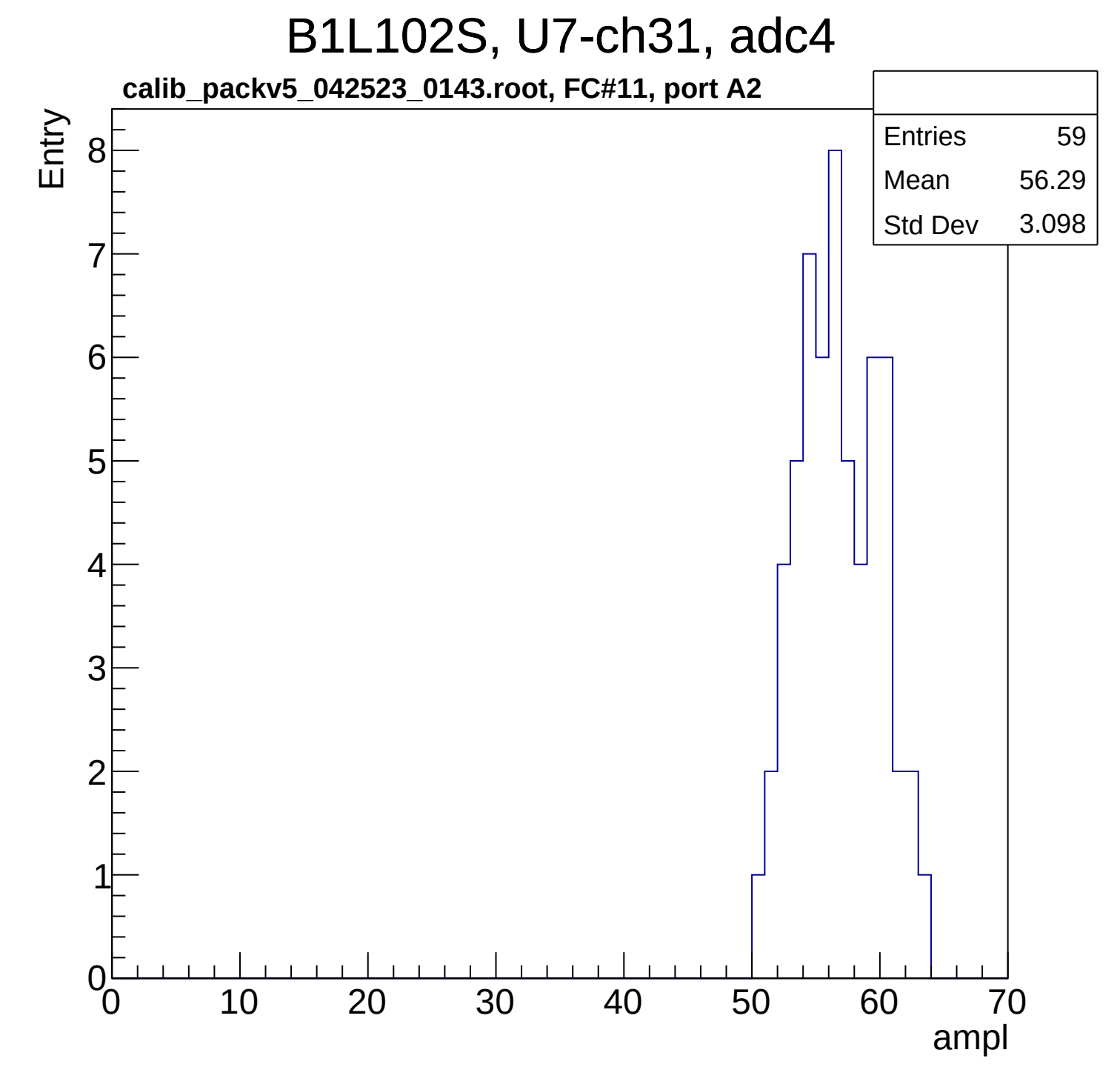
B1L102S, U7-ch31, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 59
Mean 56.29
Std Dev 3.098
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
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40
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60
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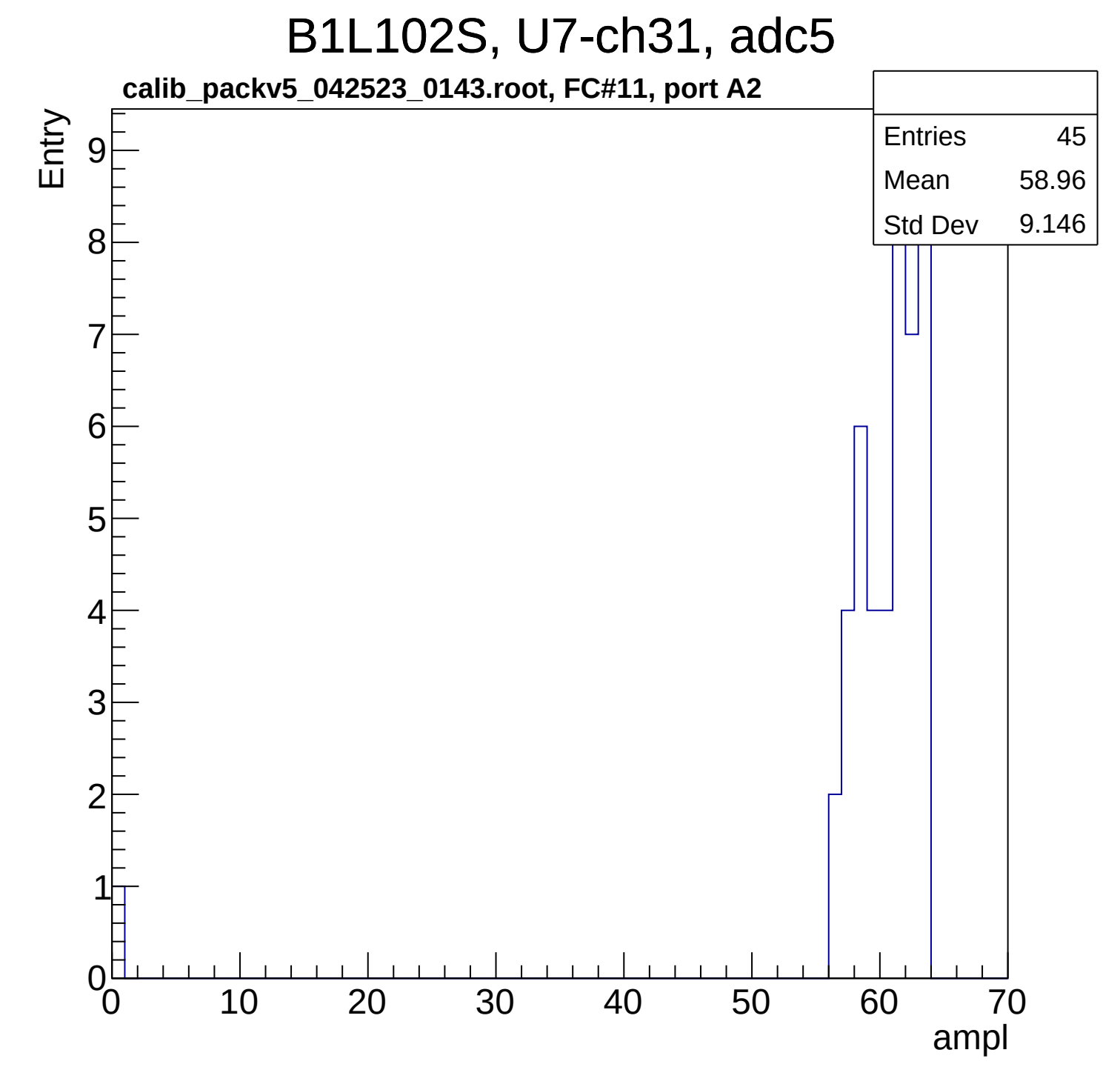
B1L102S, U7-ch31, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 45
Mean 58.96
Std Dev 9.146
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
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40
50
60
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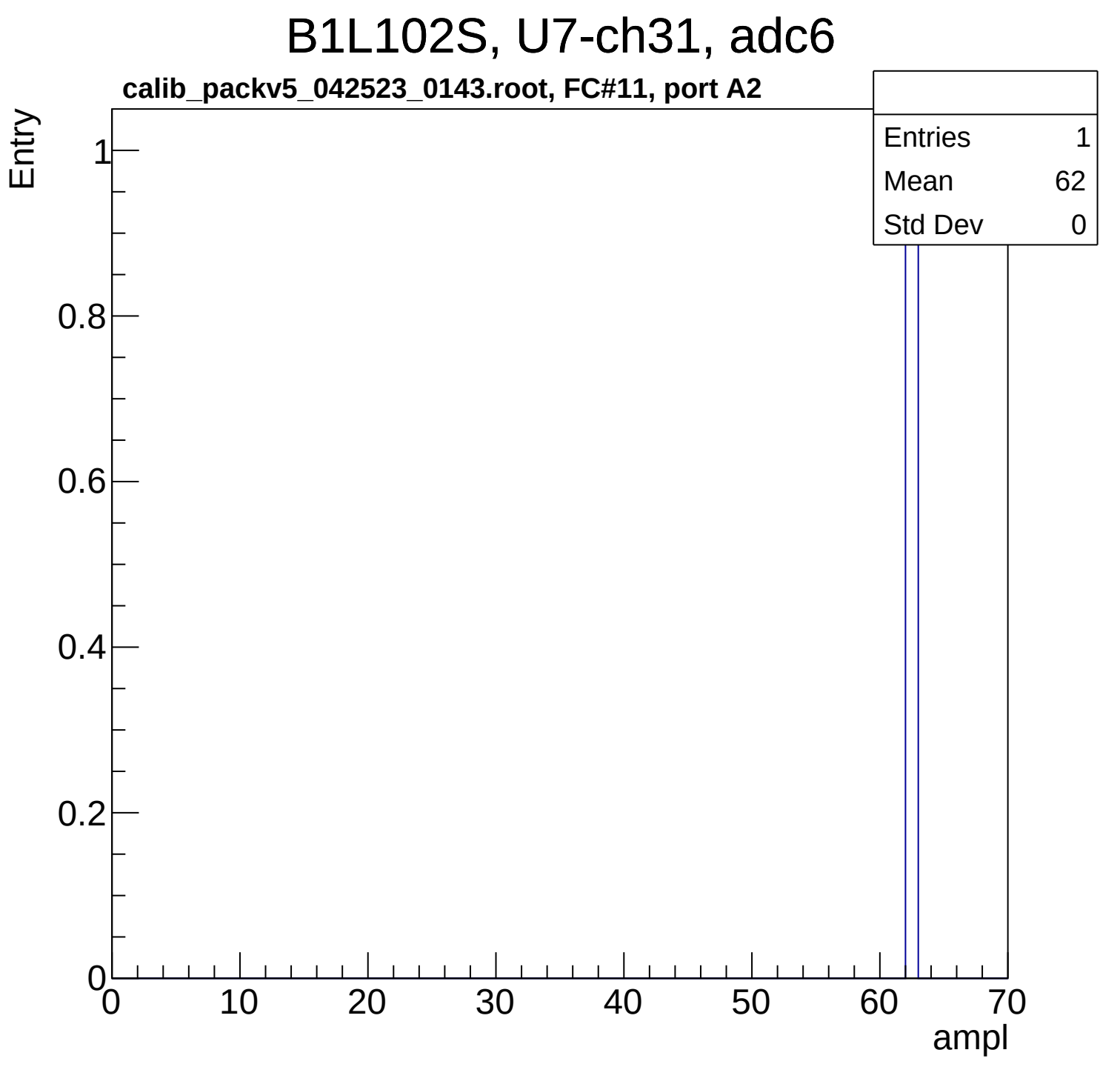
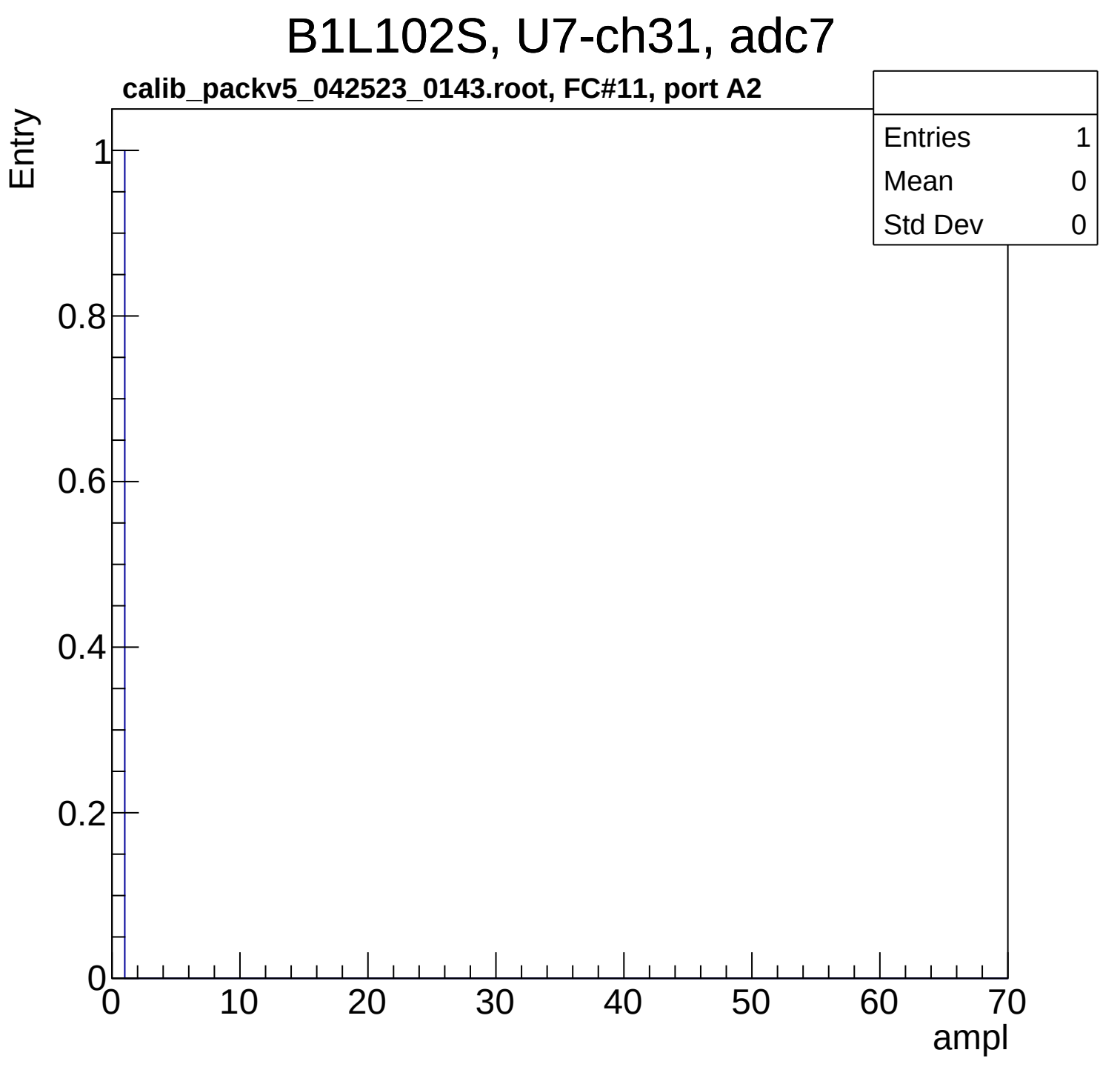
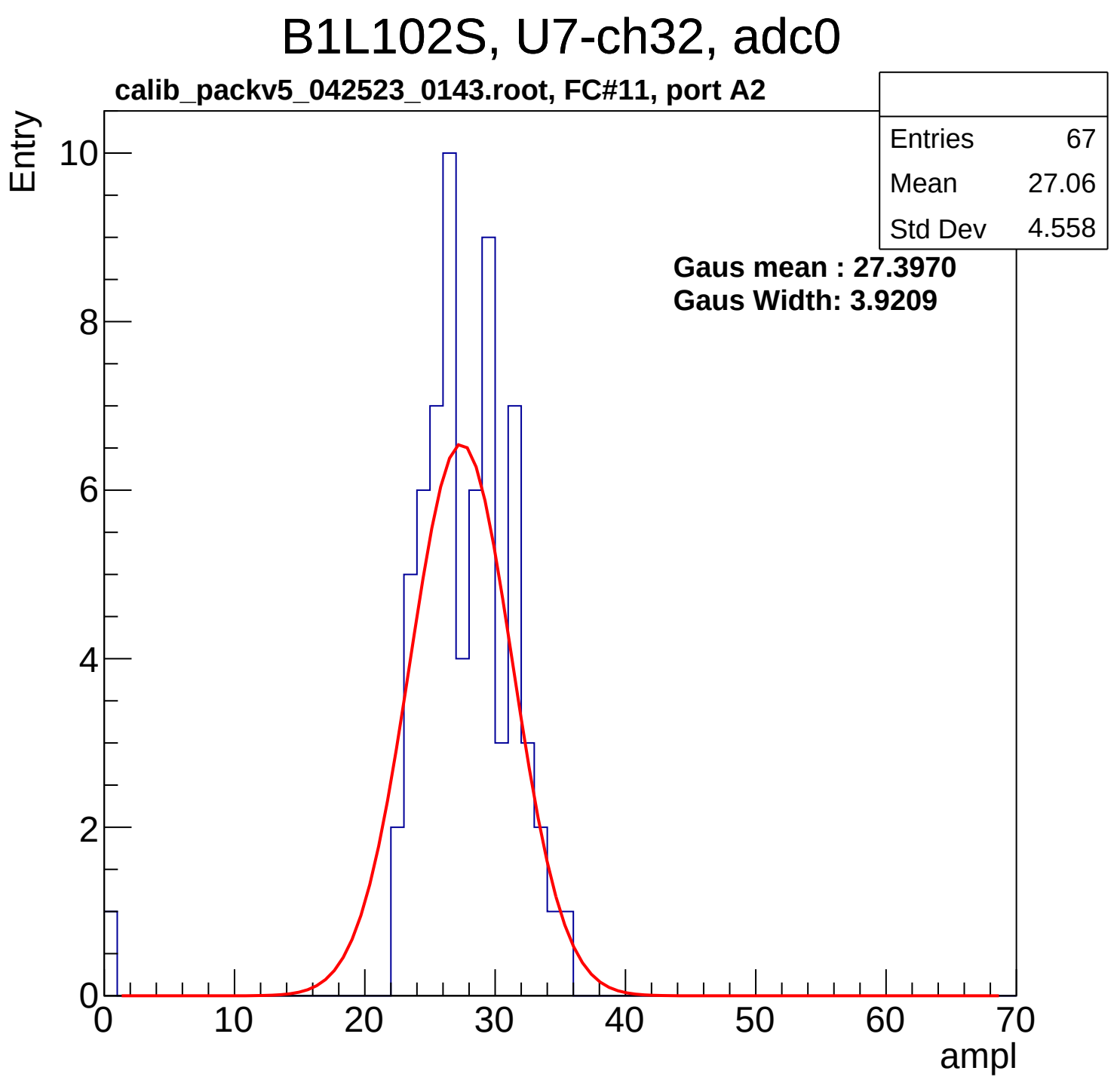

B1L102S, U7-ch31, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 1
Mean 62
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U7-ch31, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U7-ch32, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 67
Mean 27.06
Std Dev 4.558
Gaus mean : 27.3970
Gaus Width: 3.9209
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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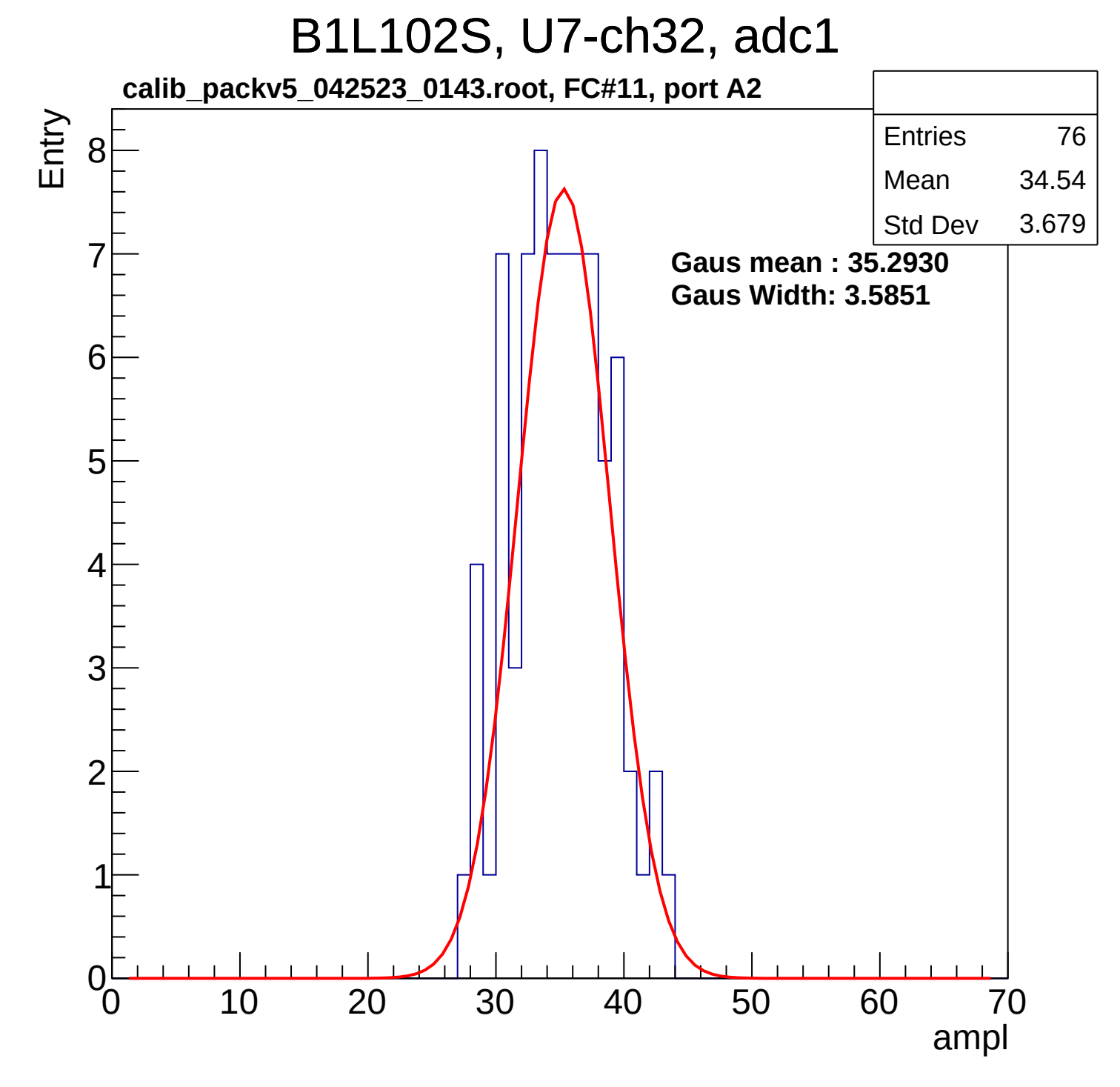
B1L102S, U7-ch32, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 76
Mean 34.54
Std Dev 3.679
Gaus mean : 35.2930
Gaus Width: 3.5851
Entry
ampl
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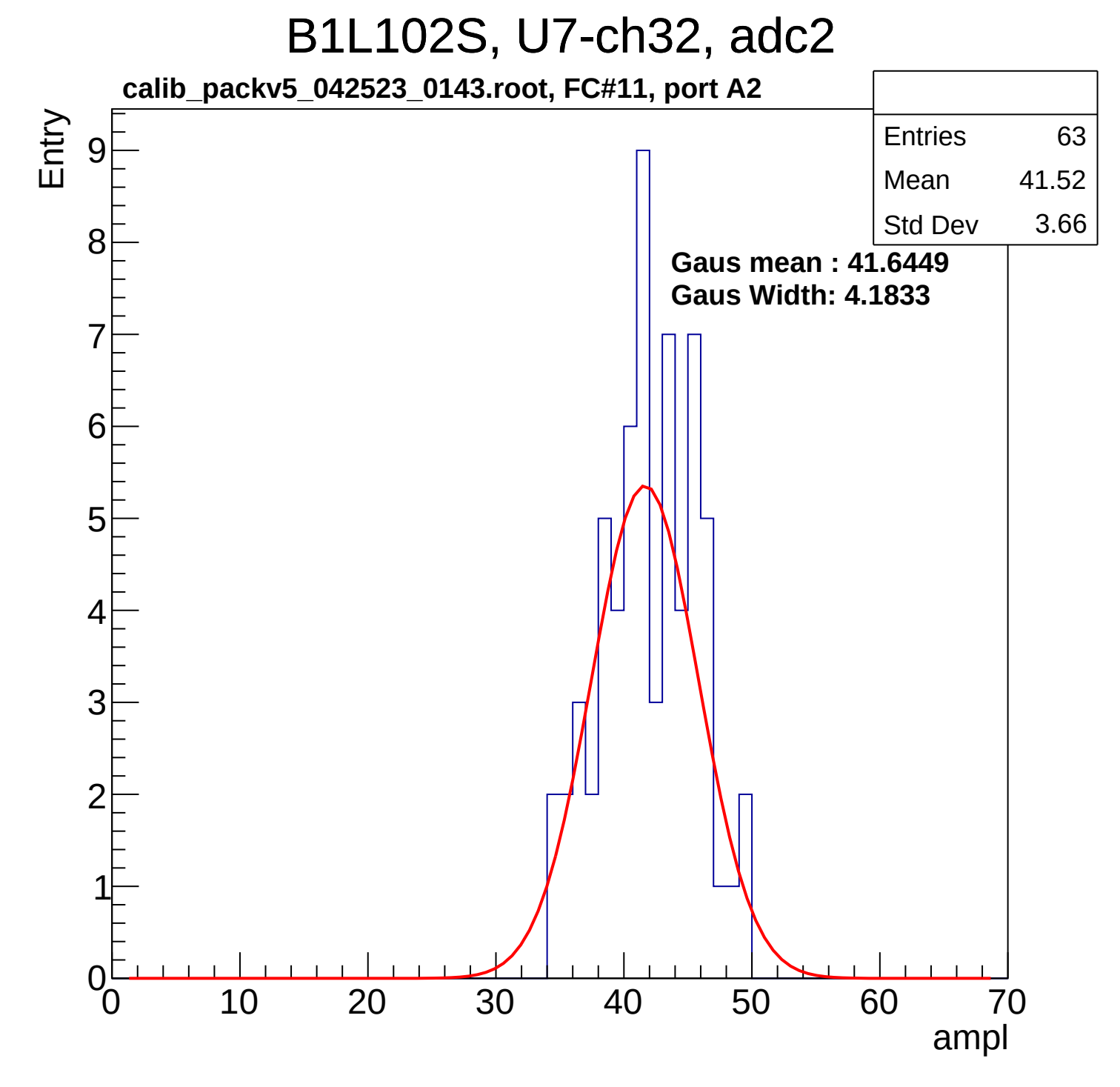
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L102S, U7-ch32, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 63
Mean 41.52
Std Dev 3.66
Gaus mean : 41.6449
Gaus Width: 4.1833
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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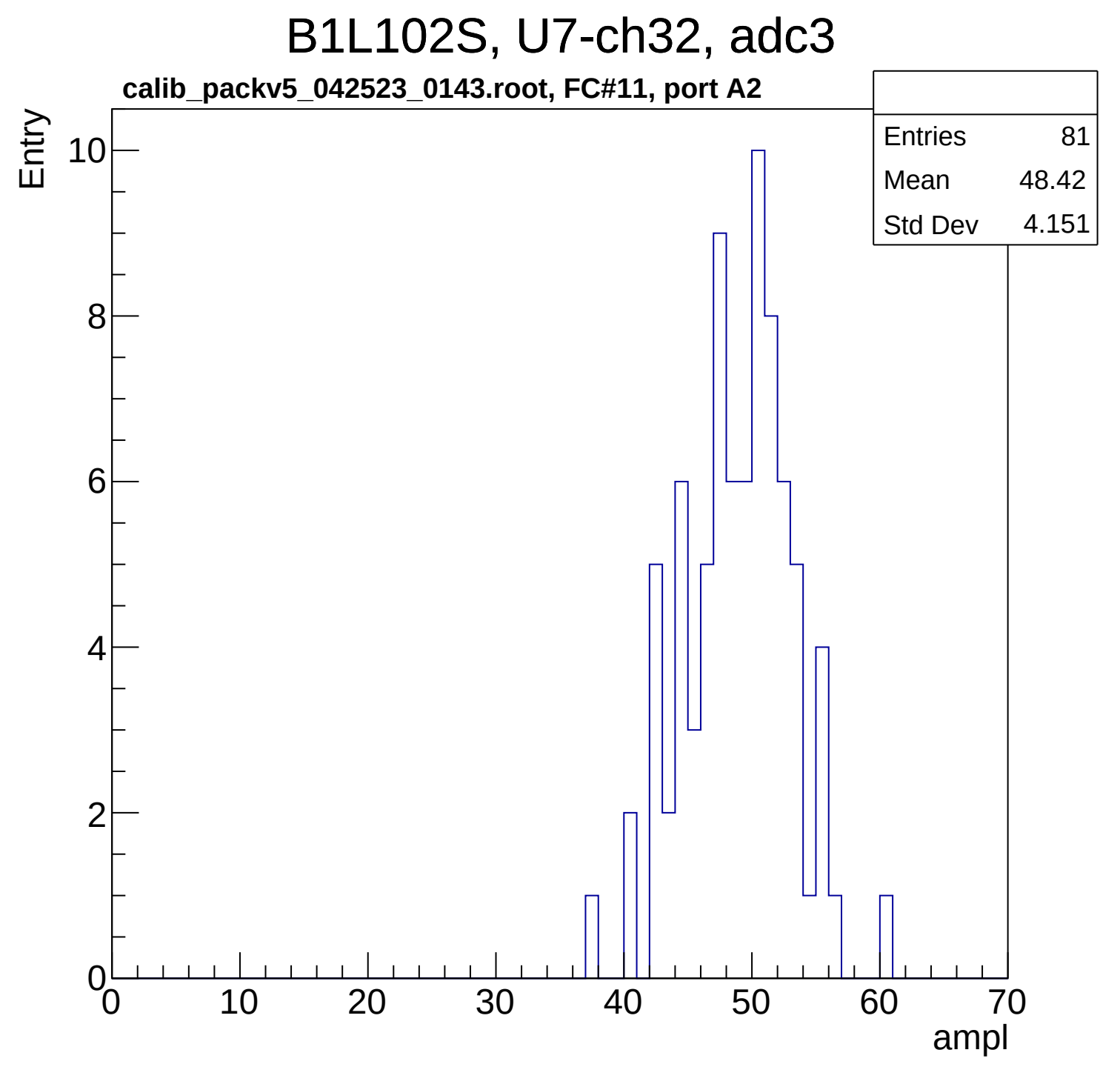
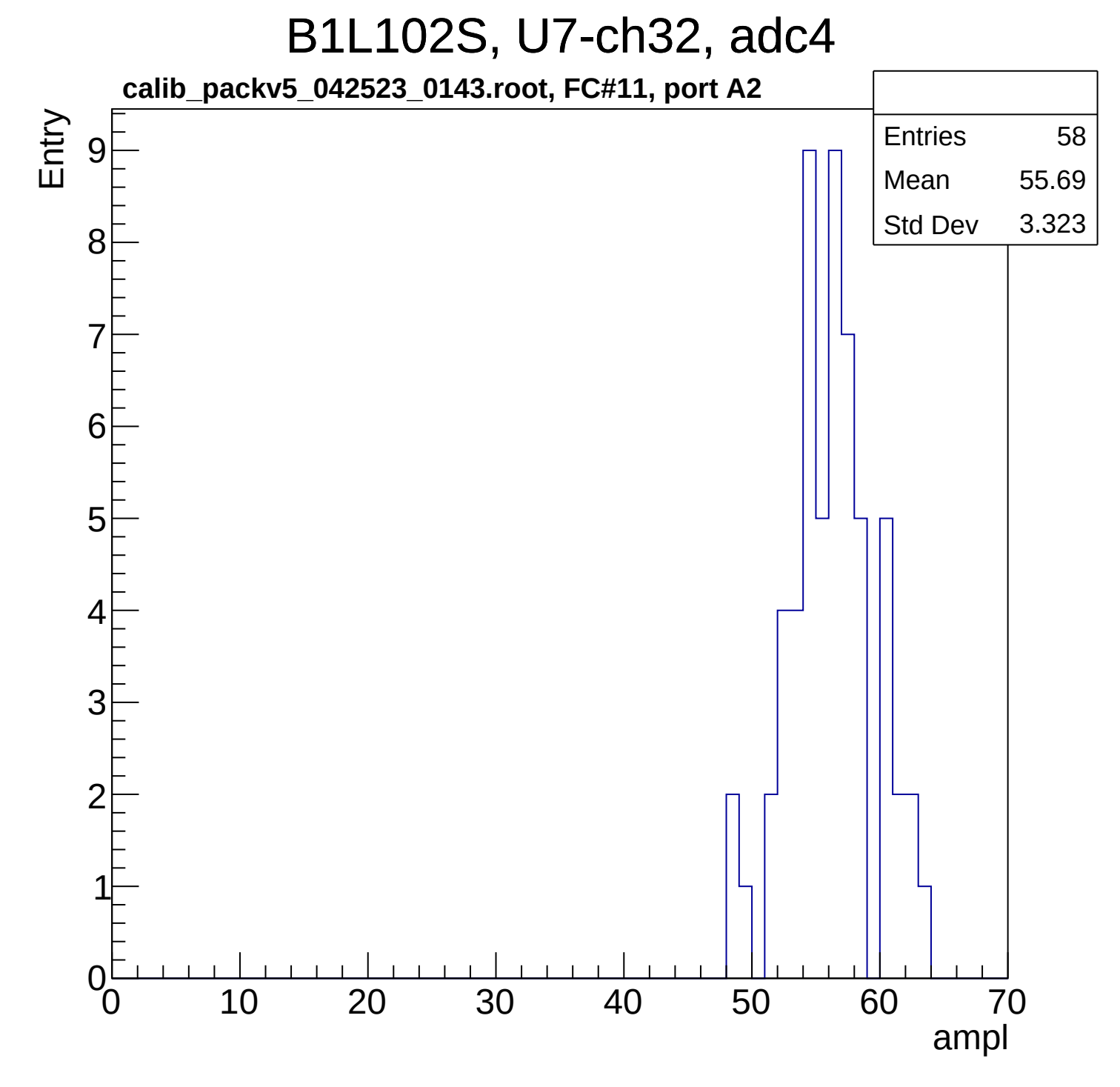

B1L102S, U7-ch32, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 81
Mean 48.42
Std Dev 4.151
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L102S, U7-ch32, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 58
Mean 55.69
Std Dev 3.323
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
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40
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60
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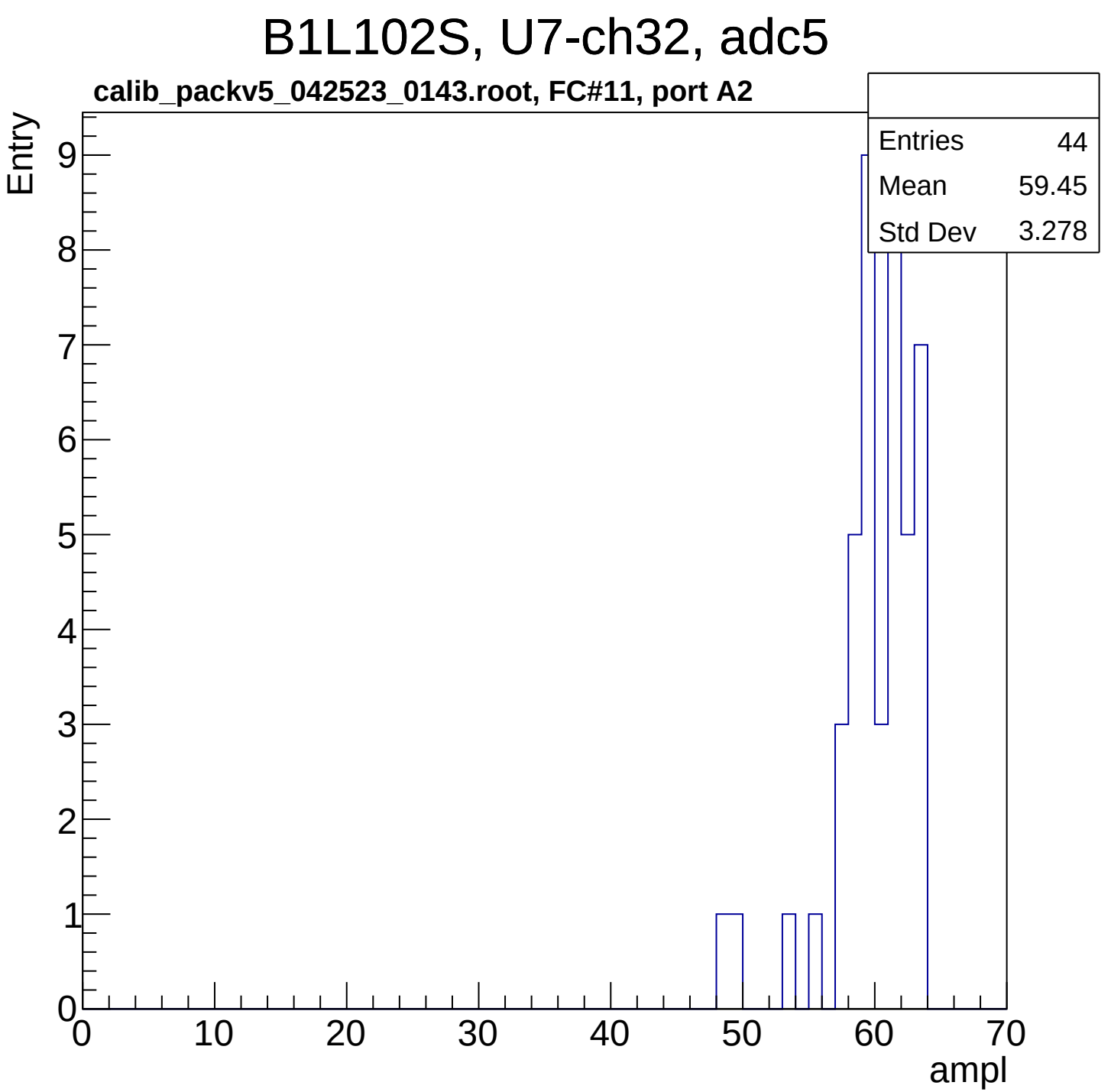
B1L102S, U7-ch32, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 44
Mean 59.45
Std Dev 3.278
Entry
ampl
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2
3
4
5
6
7
8
9
0
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60
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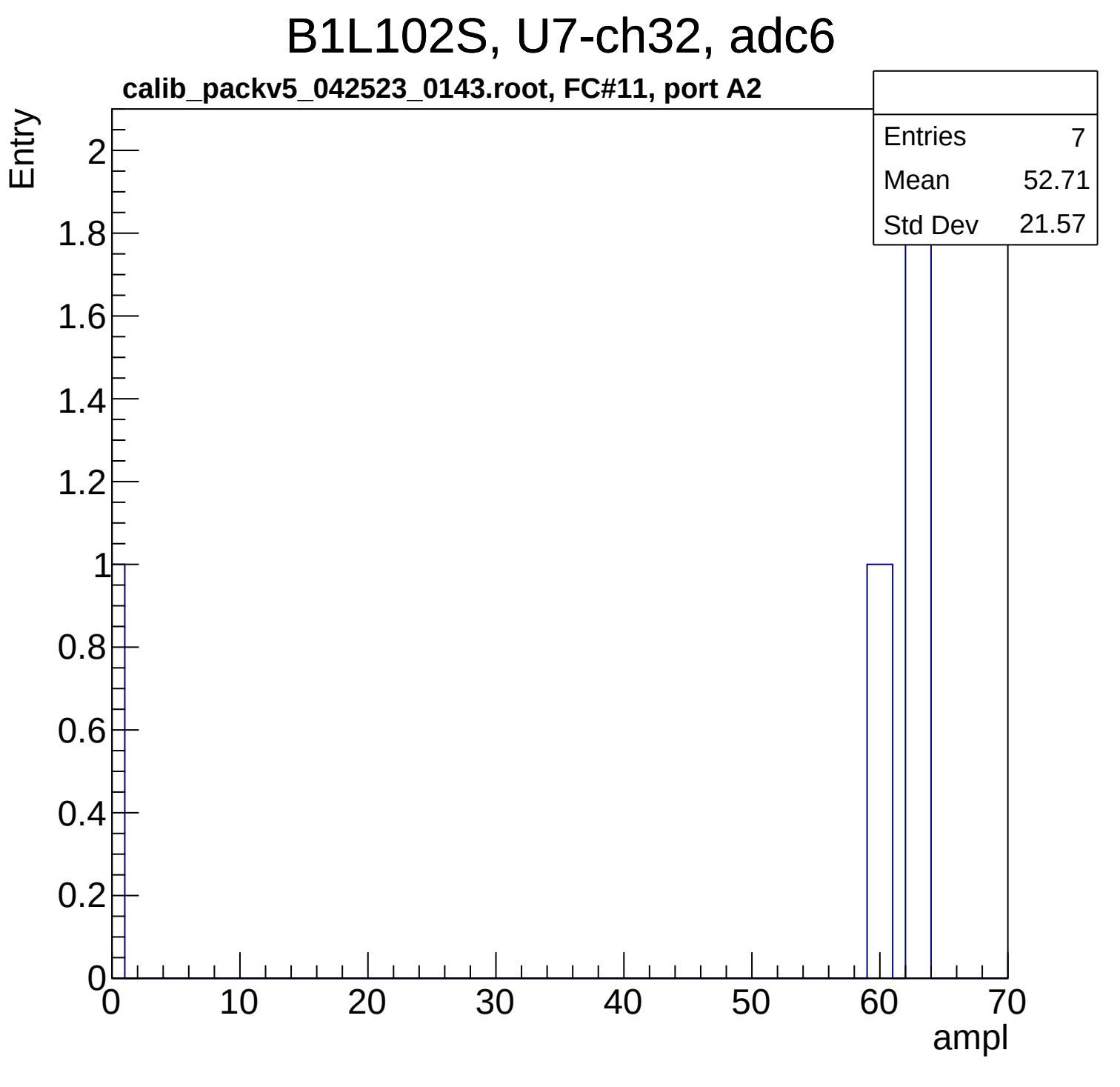
B1L102S, U7-ch32, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 7
Mean 52.71
Std Dev 21.57
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
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60
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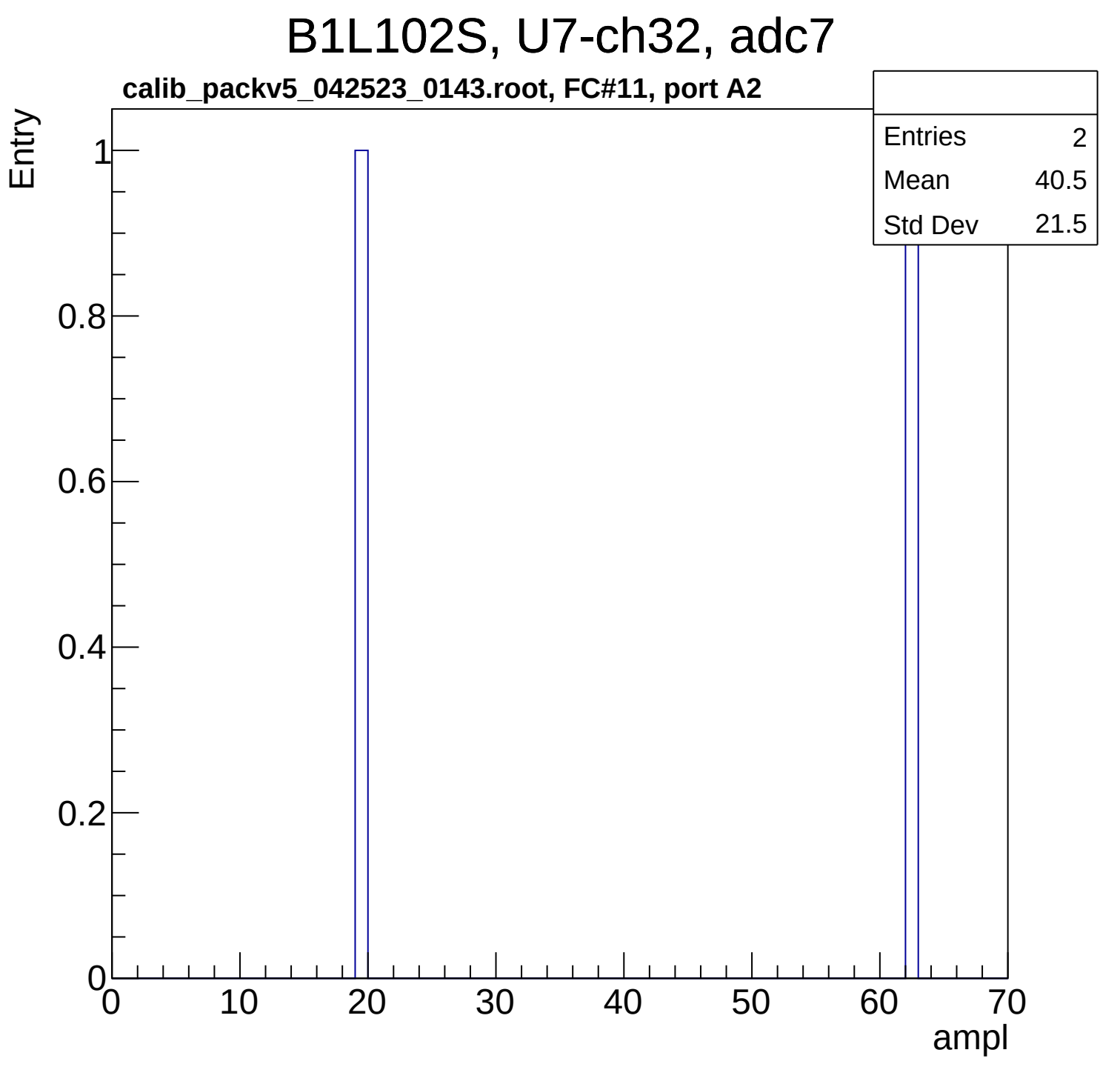
B1L102S, U7-ch32, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 2
Mean 40.5
Std Dev 21.5
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
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40
50
60
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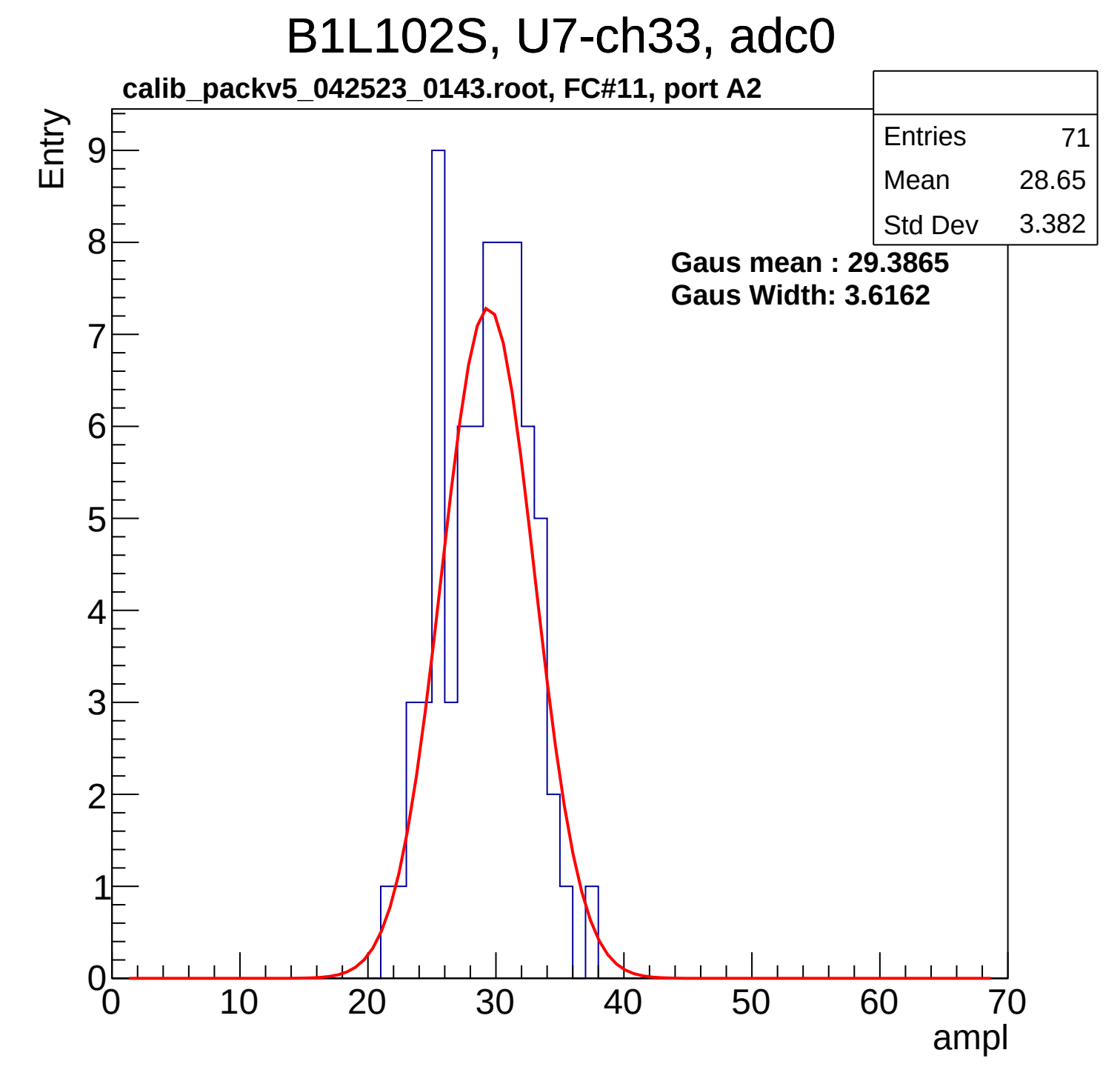
B1L102S, U7-ch33, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 71
Mean 28.65
Std Dev 3.382
Gaus mean : 29.3865
Gaus Width: 3.6162
Entry
ampl
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2
3
4
5
6
7
8
9
0
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40
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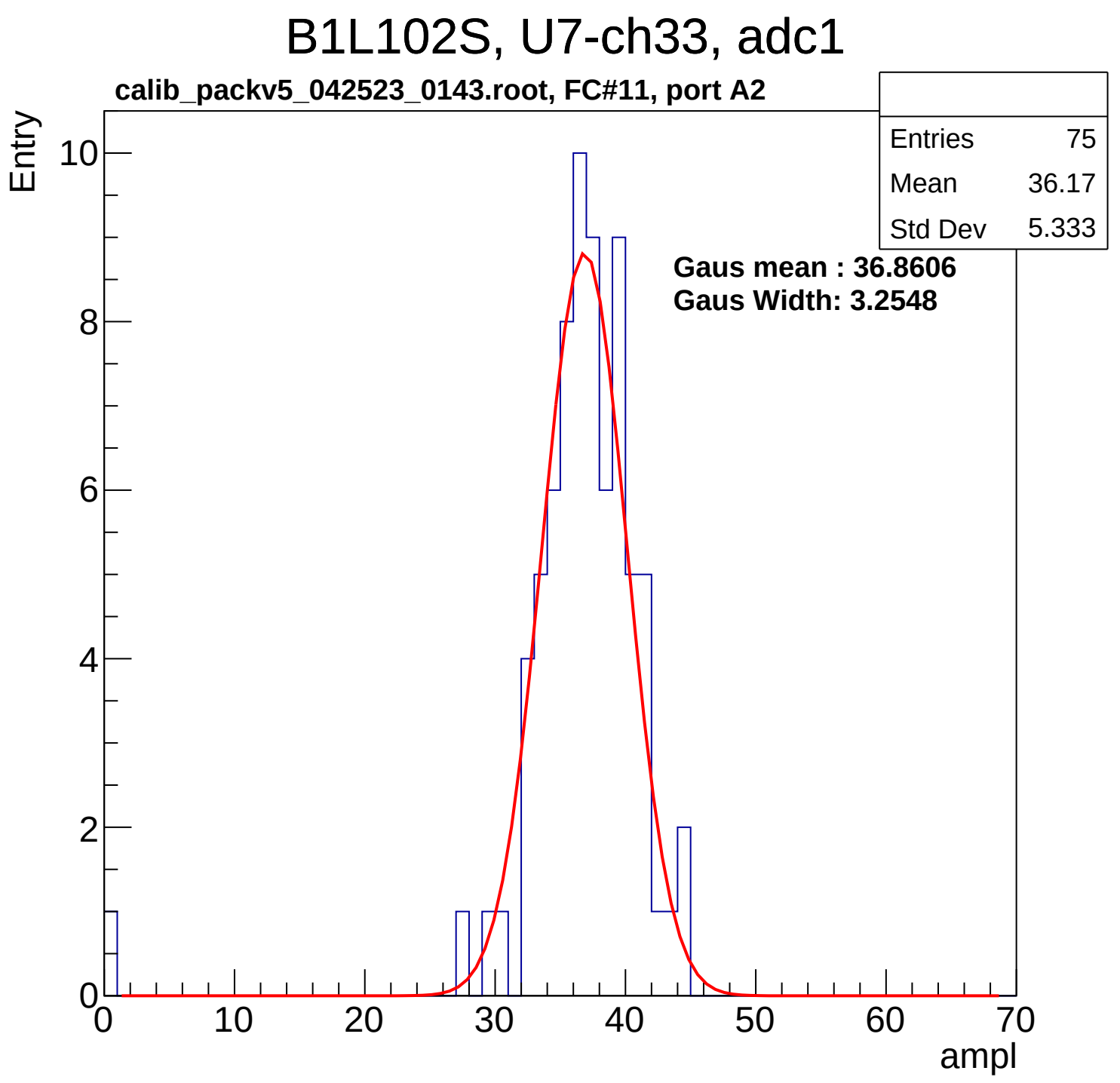
60
70


B1L102S, U7-ch33, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 75
Mean 36.17
Std Dev 5.333
Gaus mean : 36.8606
Gaus Width: 3.2548
Entry
ampl
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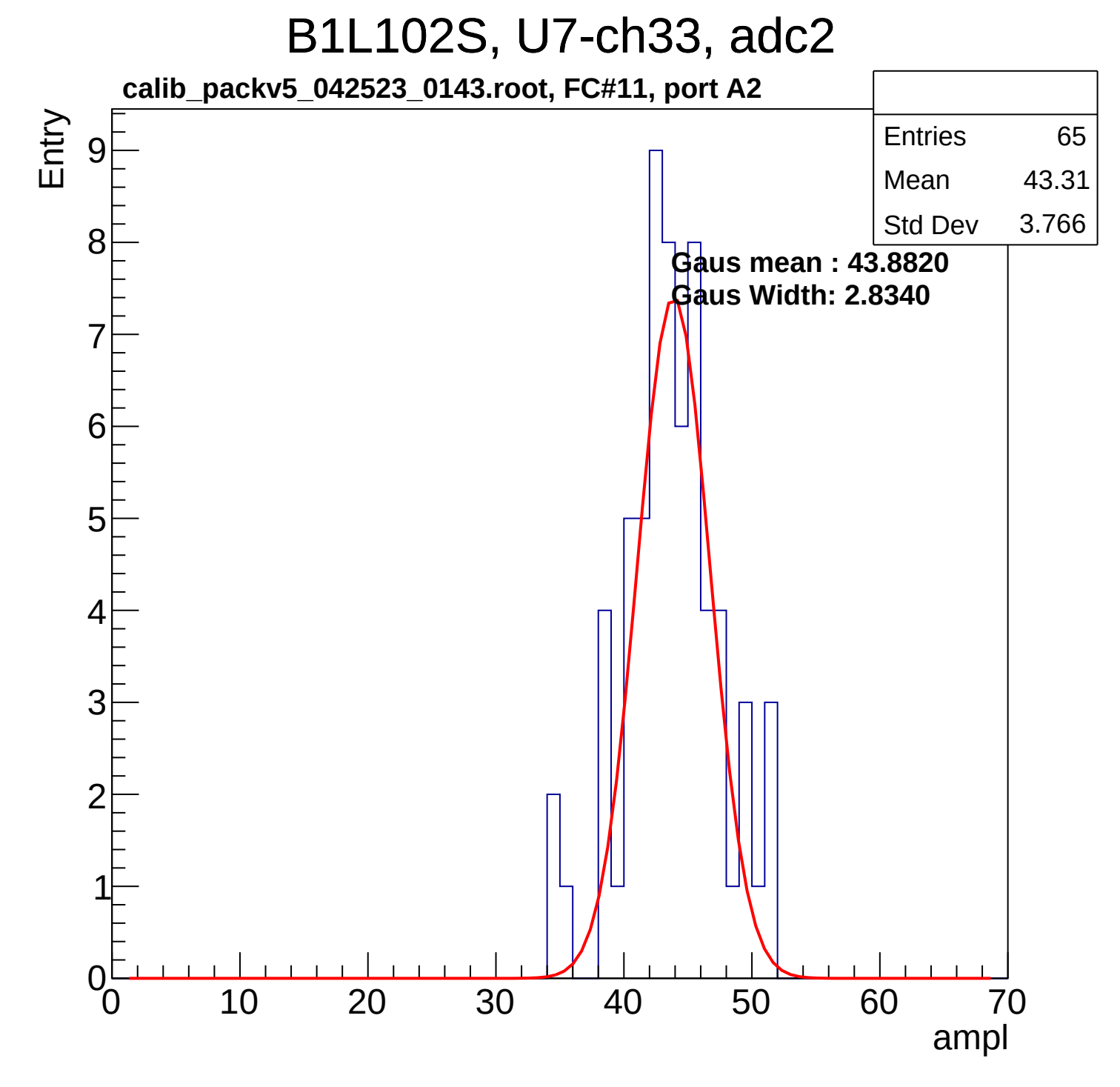
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L102S, U7-ch33, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 65
Mean 43.31
Std Dev 3.766
Gaus mean : 43.8820
Gaus Width: 2.8340
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
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20
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40
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60
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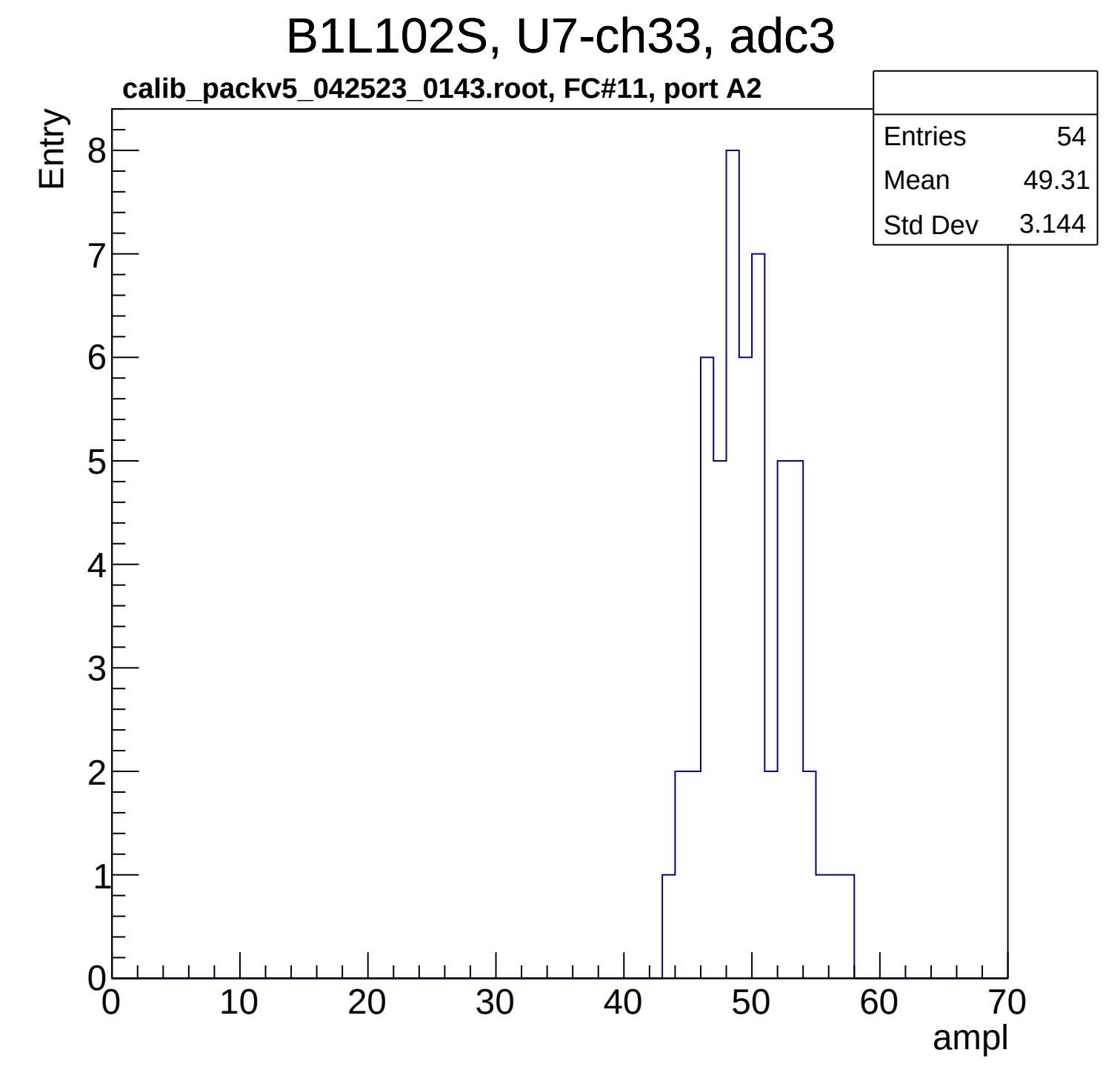
B1L102S, U7-ch33, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 54
Mean 49.31
Std Dev 3.144
Entry
ampl
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1
2
3
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5
6
7
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0
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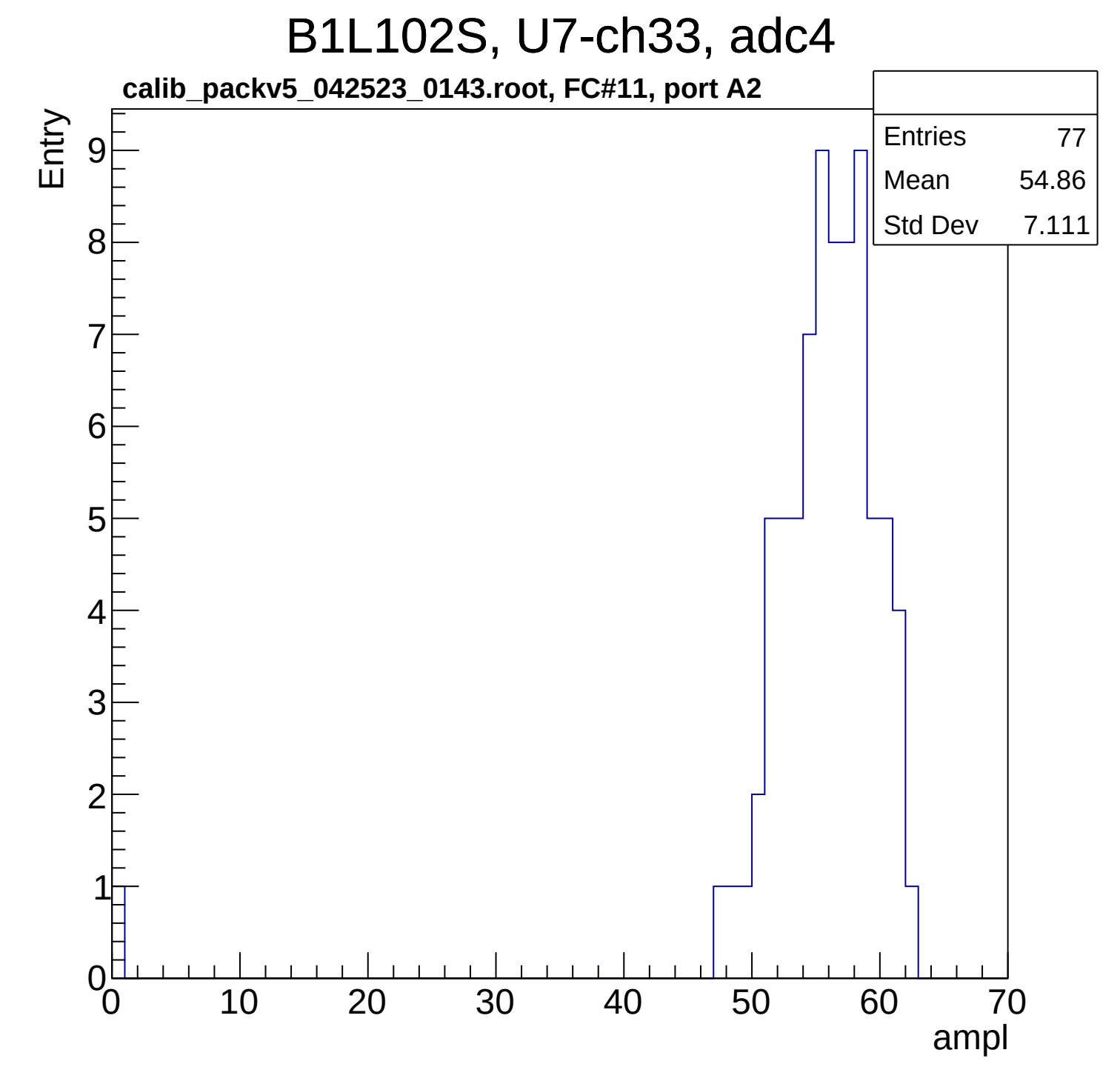
40
50
60
70


B1L102S, U7-ch33, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 77
Mean 54.86
Std Dev 7.111
Entry
ampl
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3
4
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6
7
8
9
0
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60
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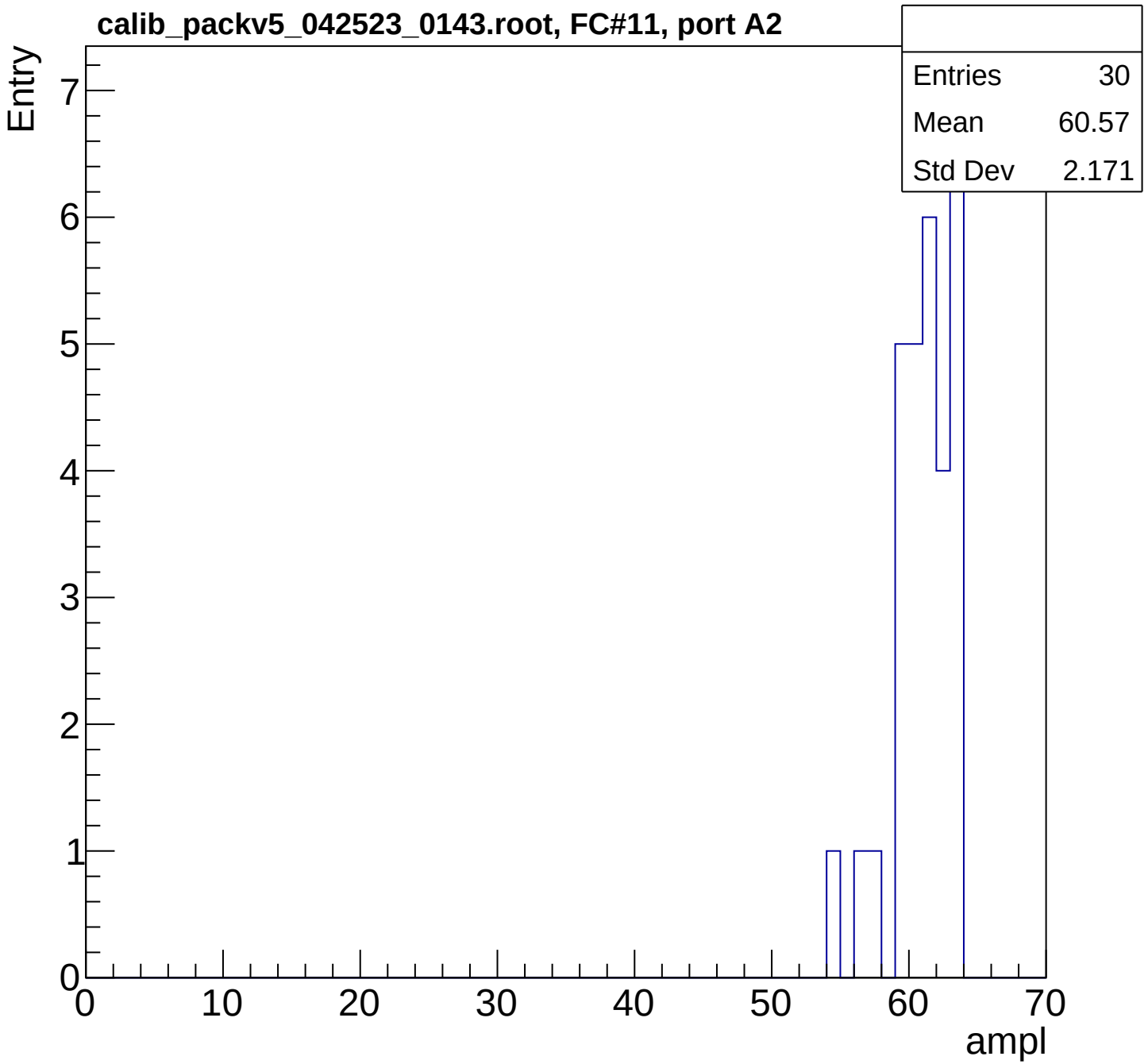
B1L102S, U7-ch33, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 30
Mean 60.57
Std Dev 2.171
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
30
40
50
60
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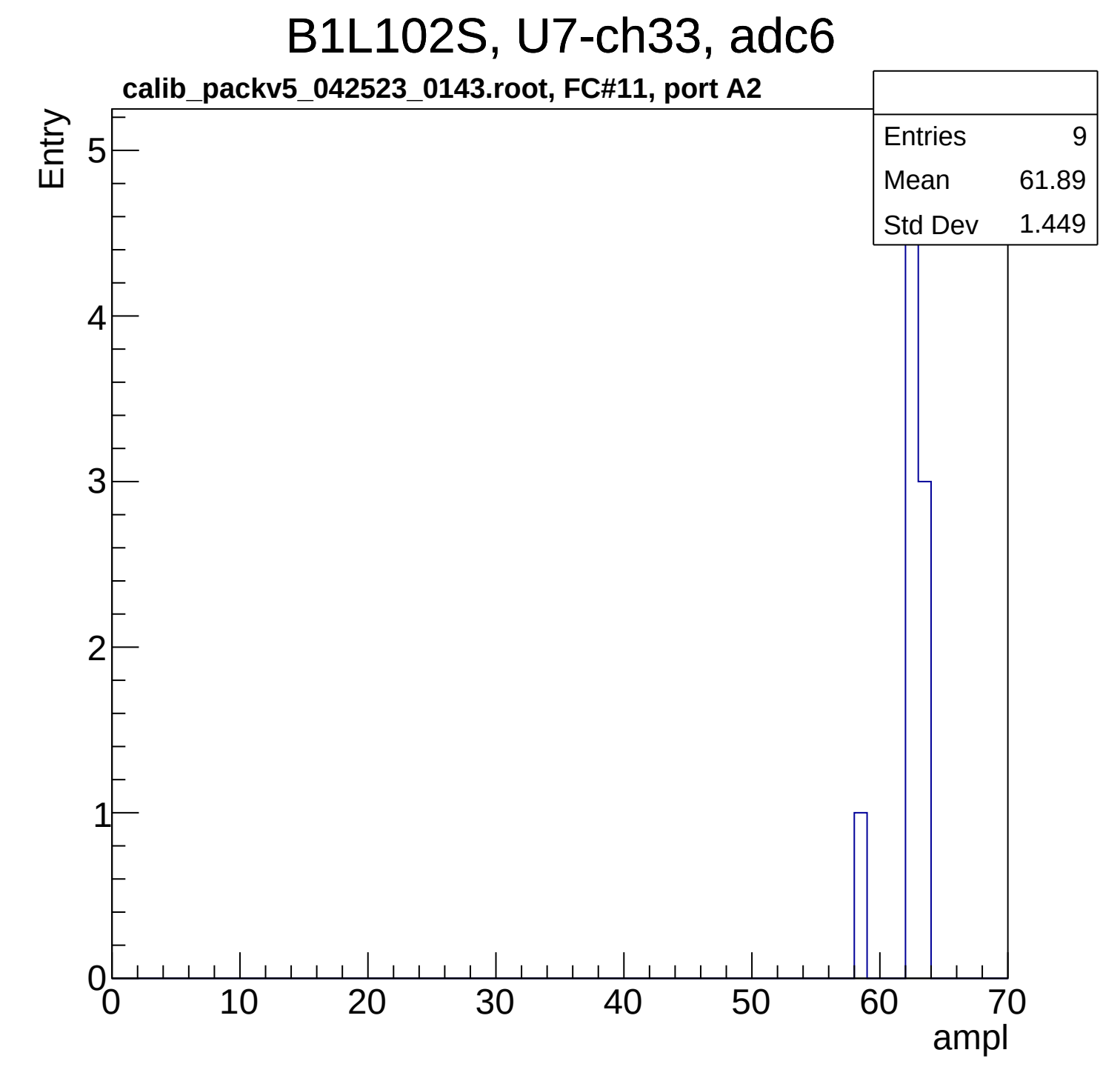
B1L102S, U7-ch33, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 9
Mean 61.89
Std Dev 1.449
Entry
ampl
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3
4
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0
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20
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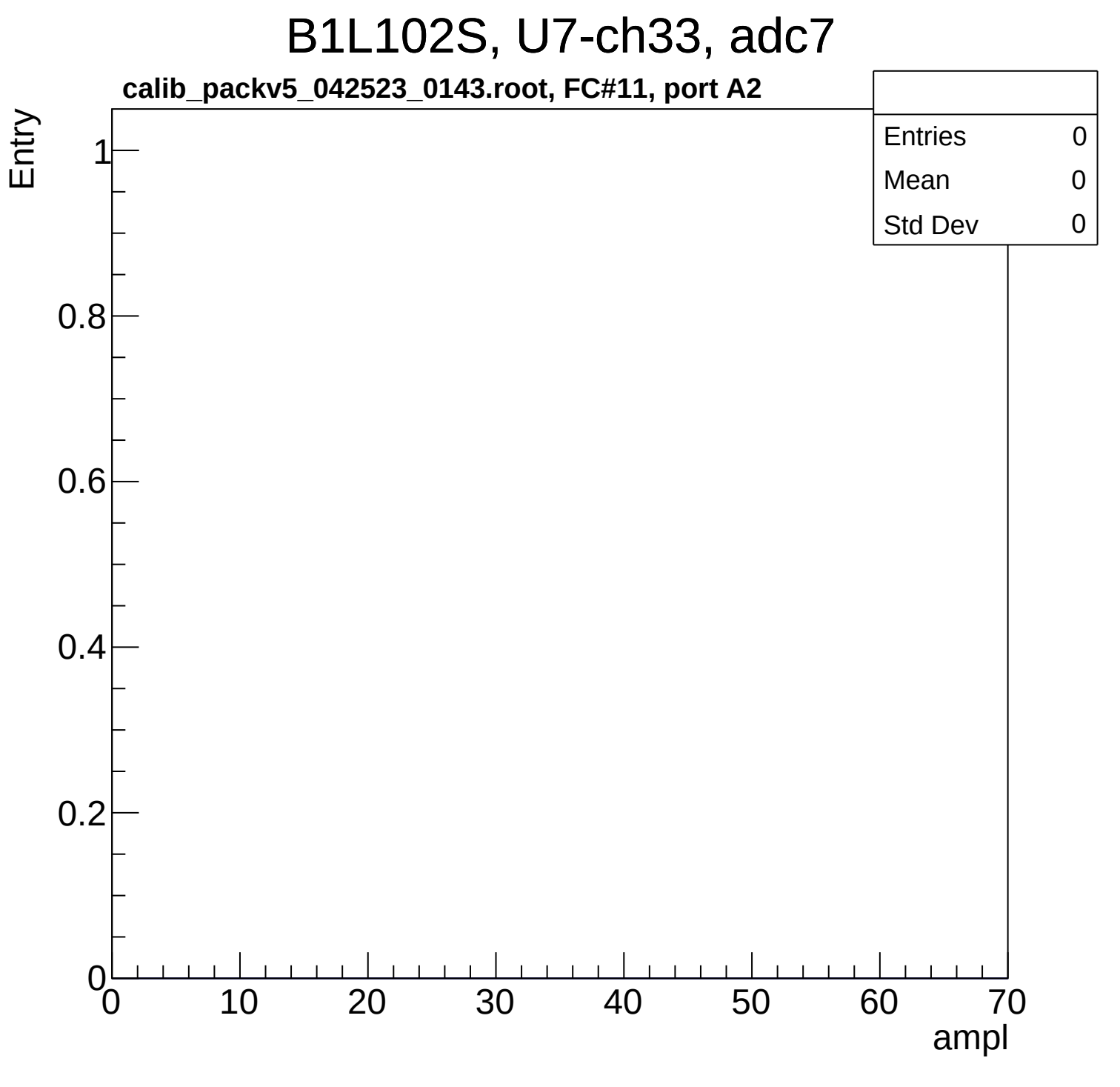
40
50
60
70


B1L102S, U7-ch33, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 0
Mean 0
Std Dev 0
Entry
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0.6
0.4
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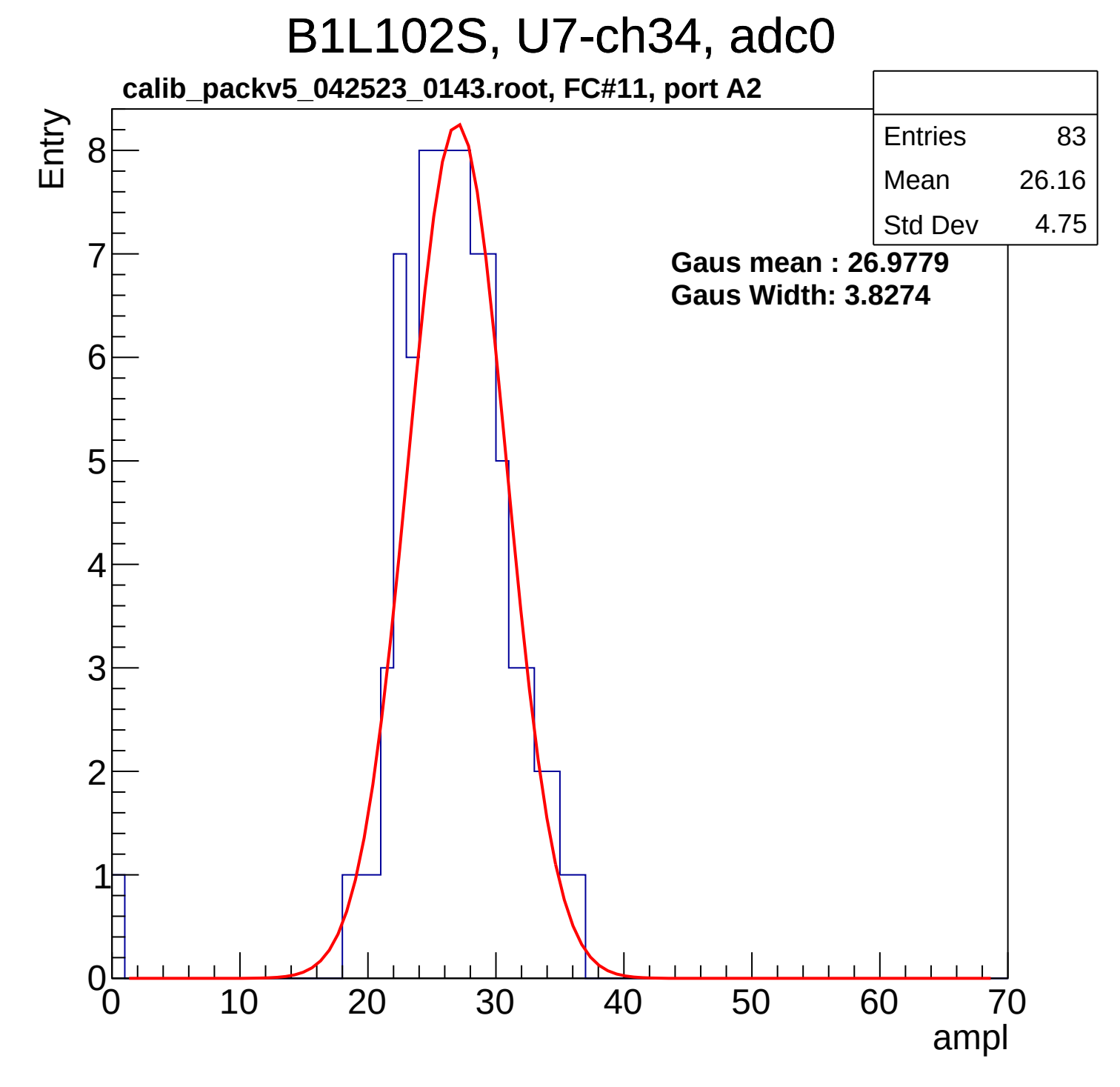
0
10
20
30
40
50
60
70
ampl


B1L102S, U7-ch34, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 83
Mean 26.16
Std Dev 4.75
Gaus mean : 26.9779
Gaus Width: 3.8274
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
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60
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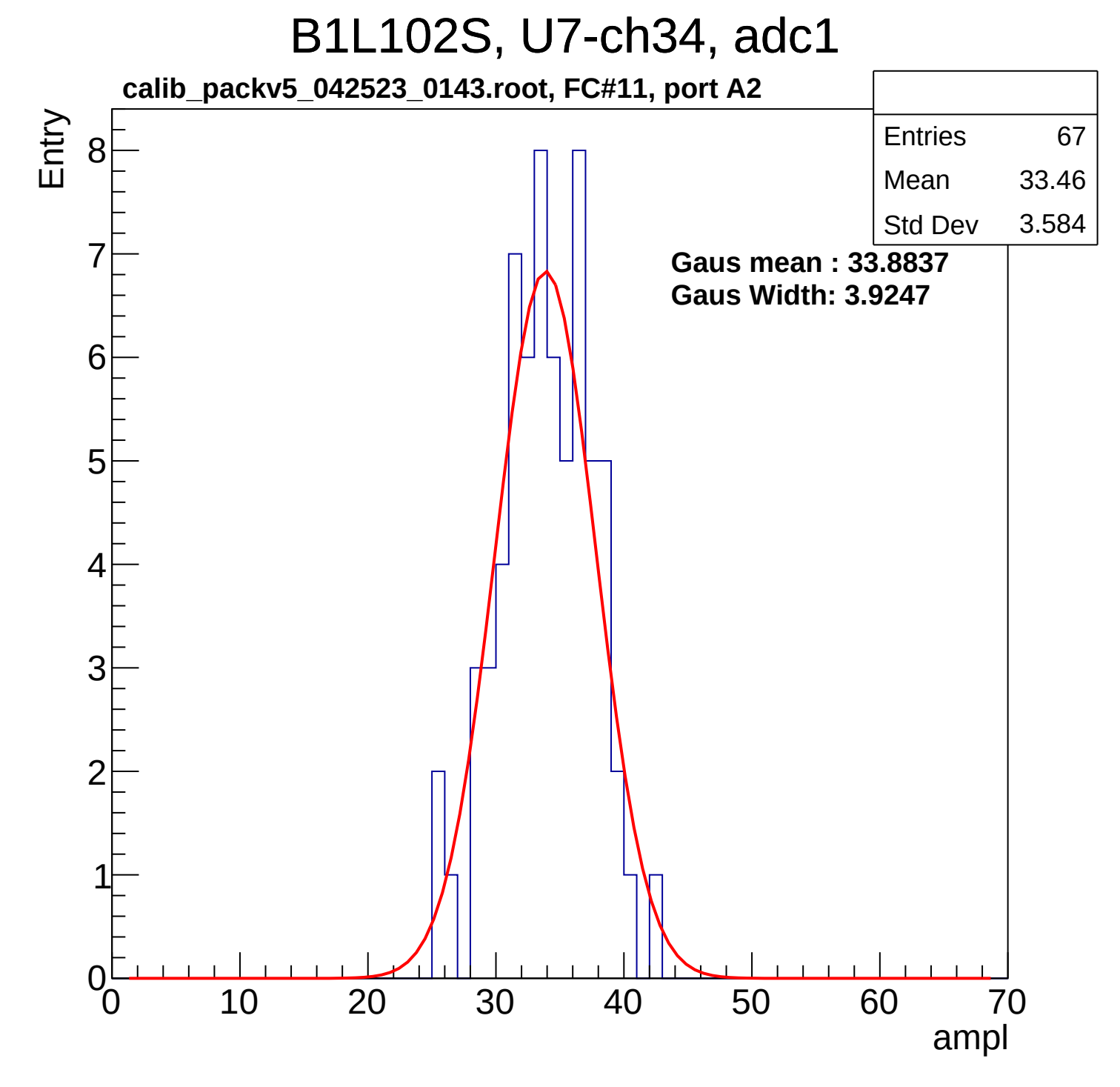
B1L102S, U7-ch34, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 67
Mean 33.46
Std Dev 3.584
Gaus mean : 33.8837
Gaus Width: 3.9247
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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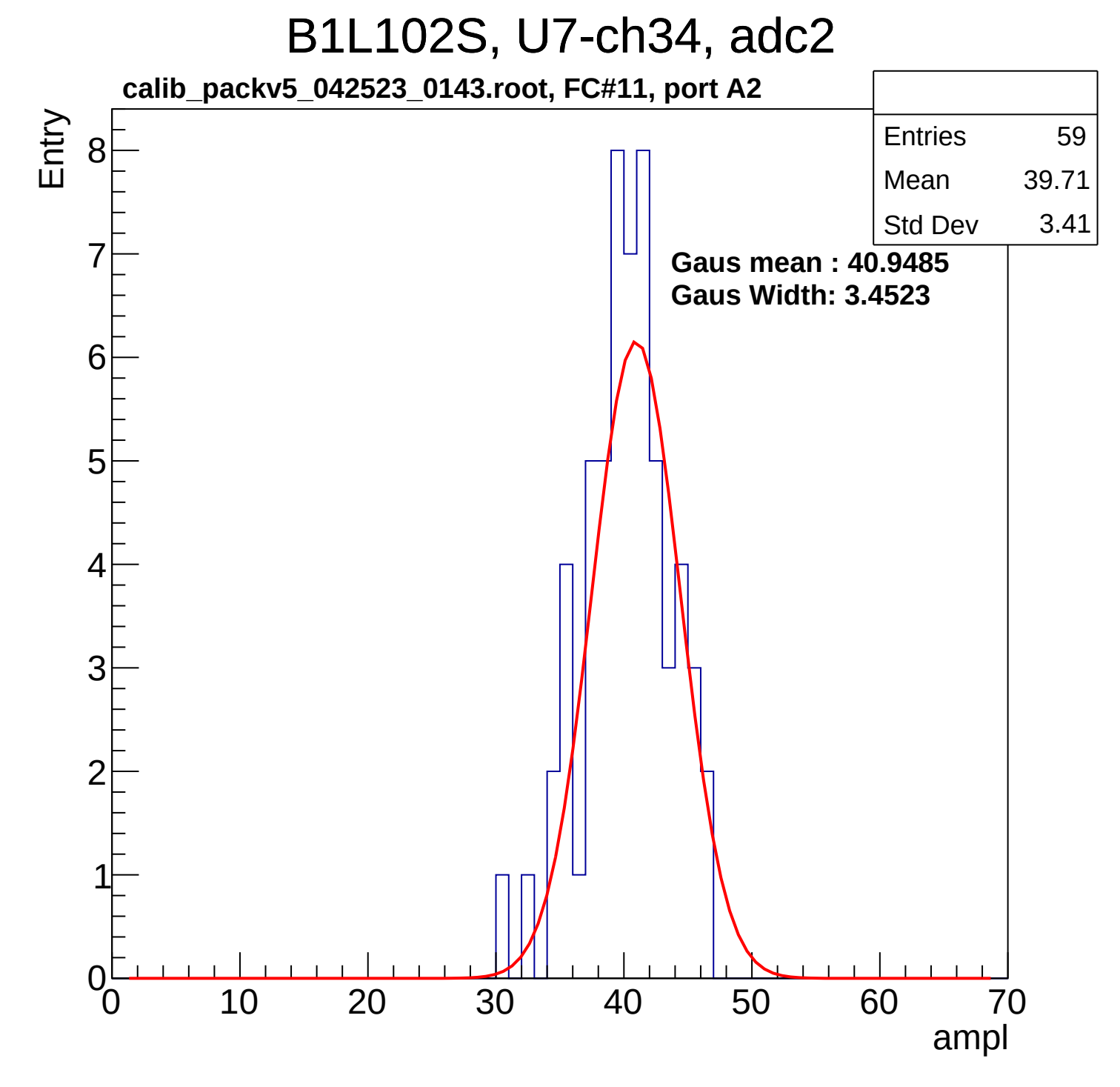
B1L102S, U7-ch34, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 59
Mean 39.71
Std Dev 3.41
Gaus mean : 40.9485
Gaus Width: 3.4523
Entry
ampl
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2
3
4
5
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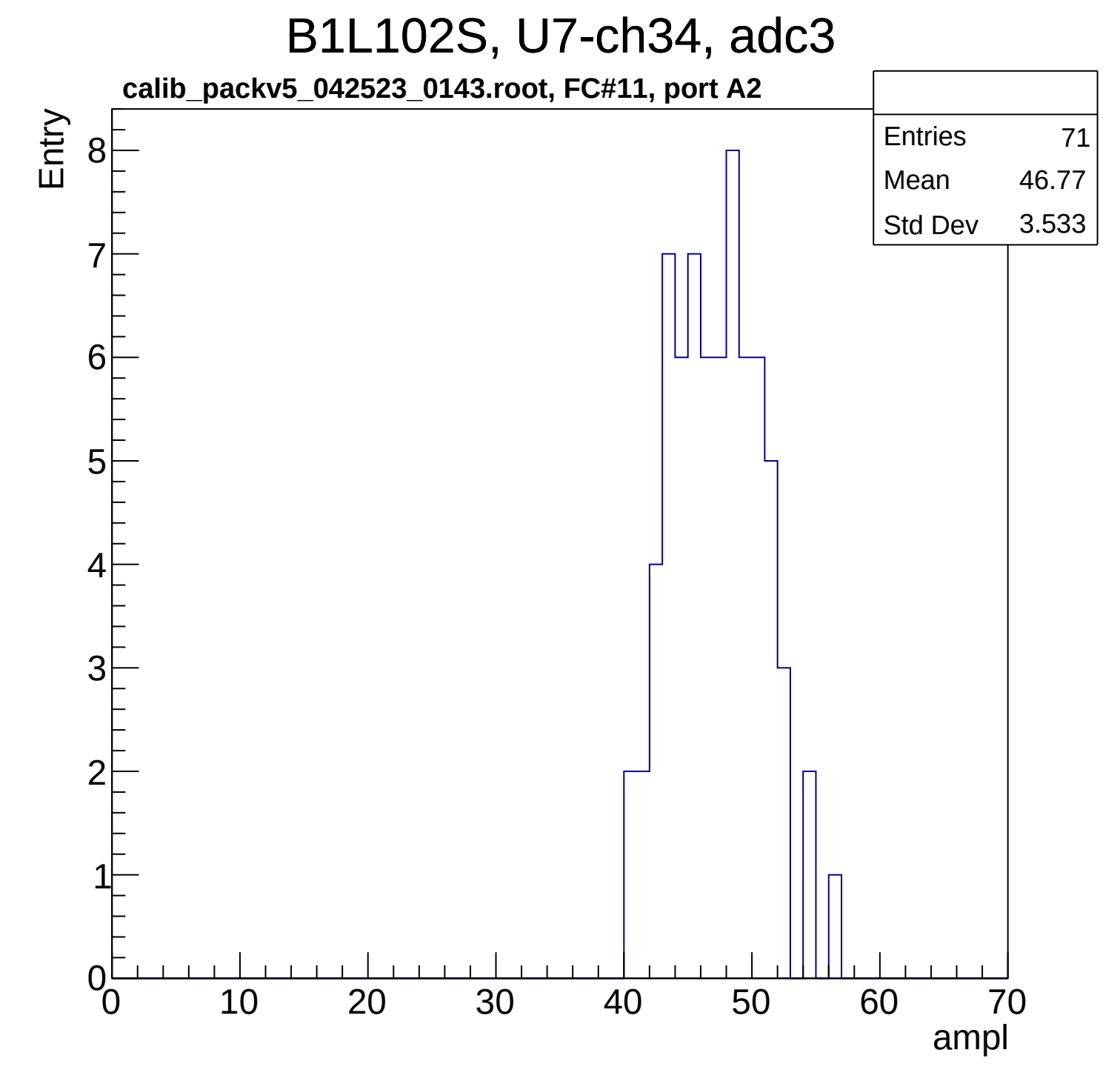
B1L102S, U7-ch34, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 71
Mean 46.77
Std Dev 3.533
Entry
ampl
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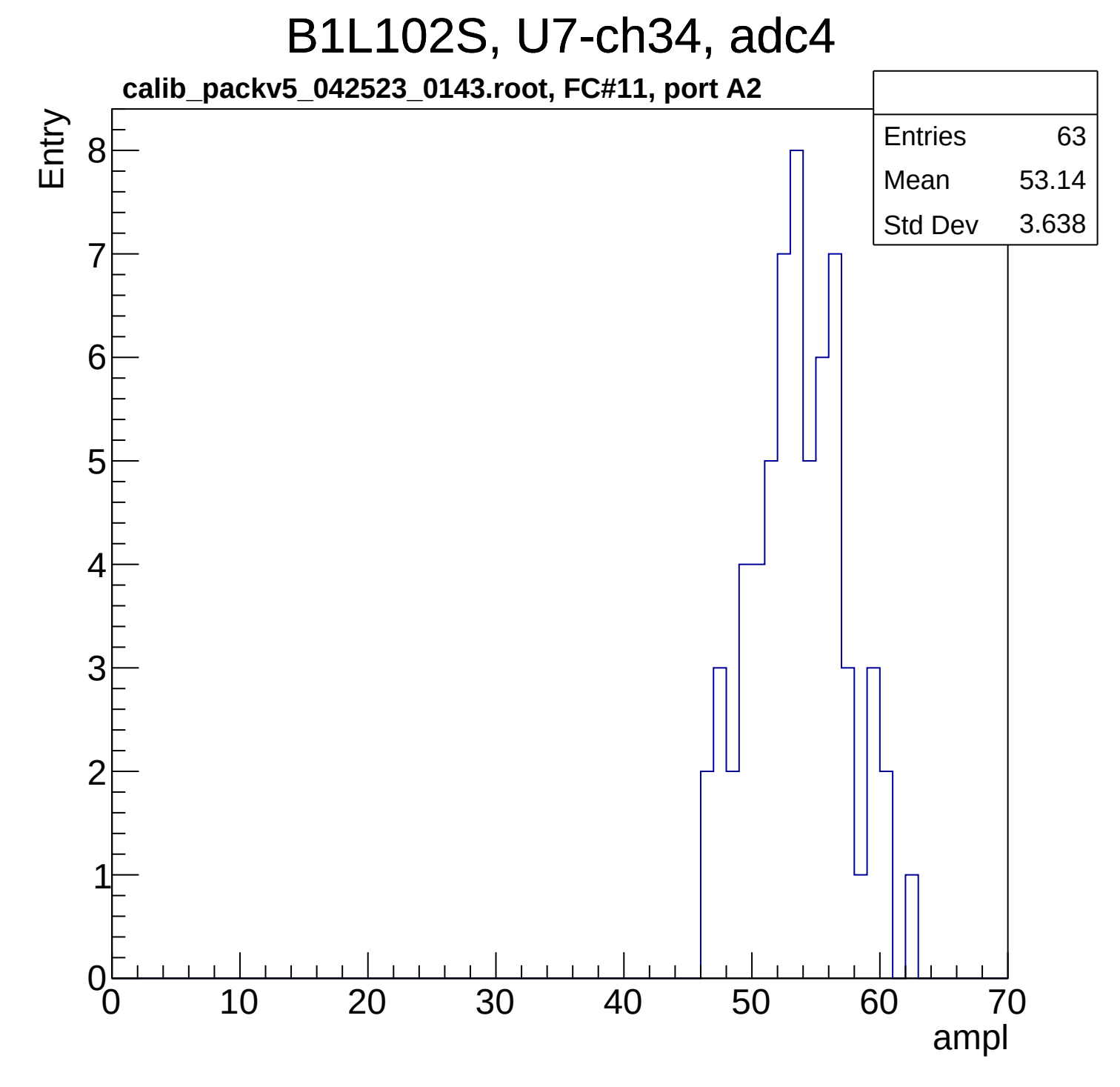
B1L102S, U7-ch34, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 63
Mean 53.14
Std Dev 3.638
Entry
ampl
0
1
2
3
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5
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7
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0
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60
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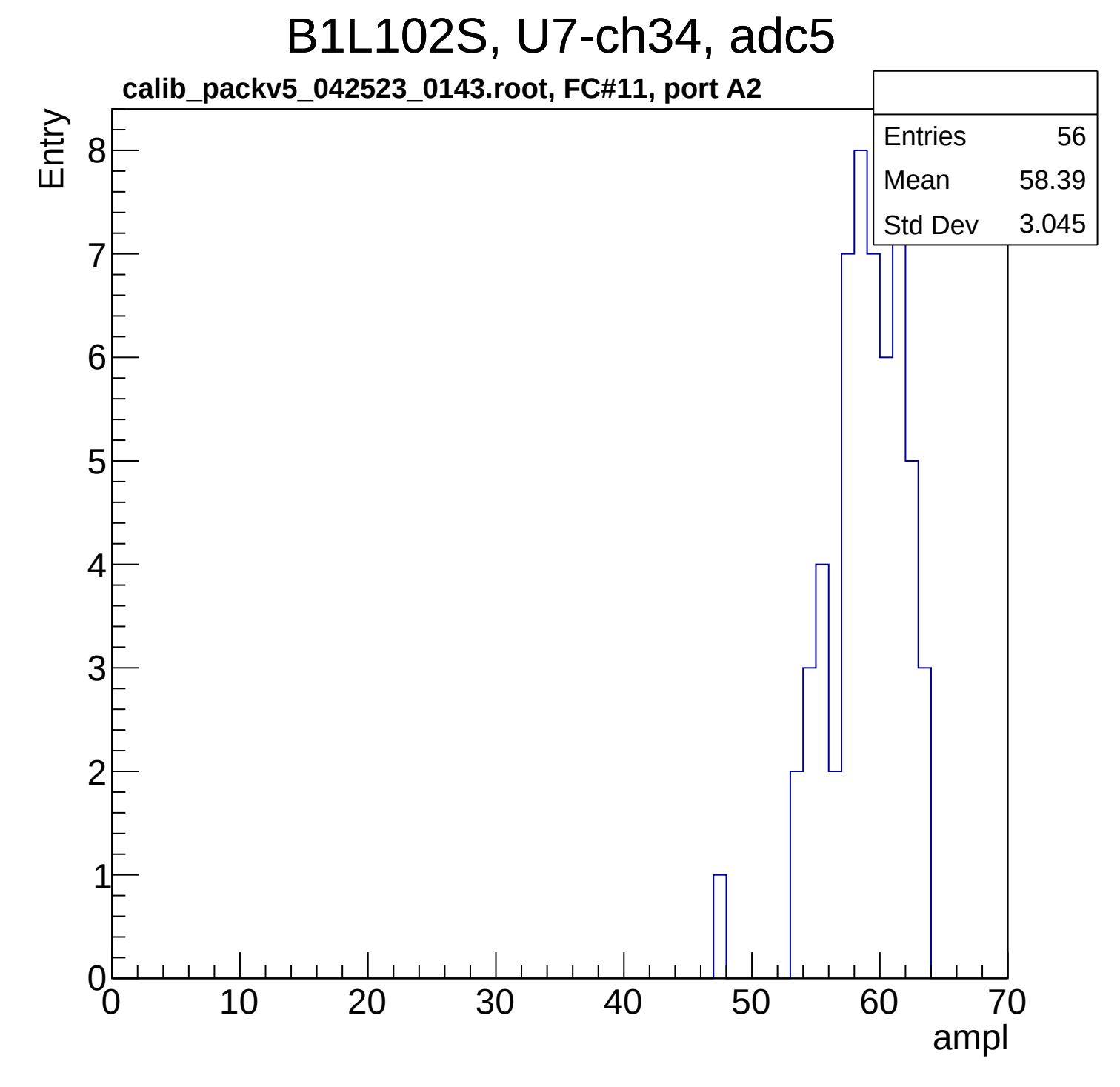
B1L102S, U7-ch34, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 56
Mean 58.39
Std Dev 3.045
Entry
ampl
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1
2
3
4
5
6
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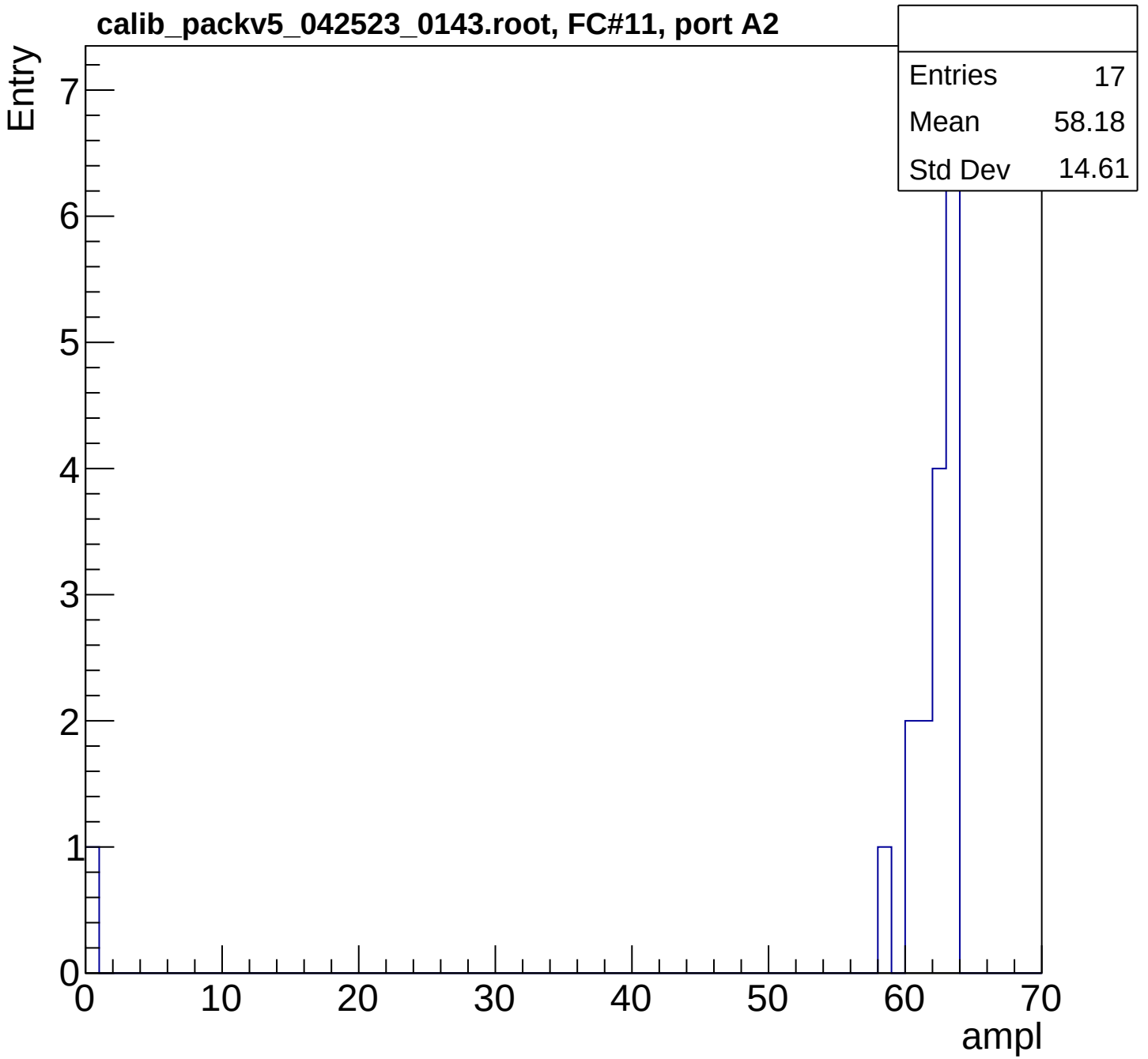
B1L102S, U7-ch34, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 17
Mean 58.18
Std Dev 14.61
Entry
ampl
0
1
2
3
4
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0
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60
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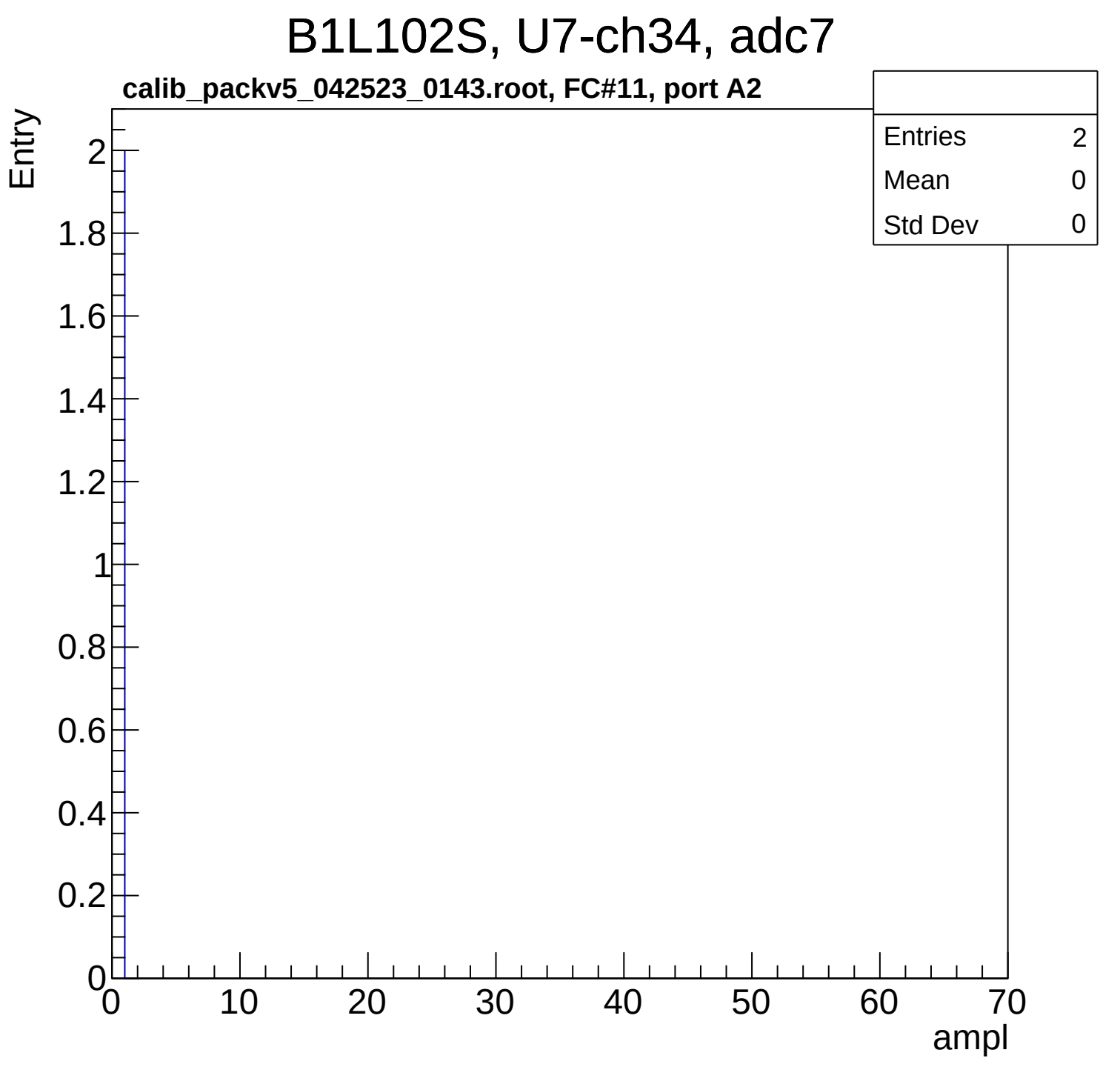
B1L102S, U7-ch34, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 2
Mean 0
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
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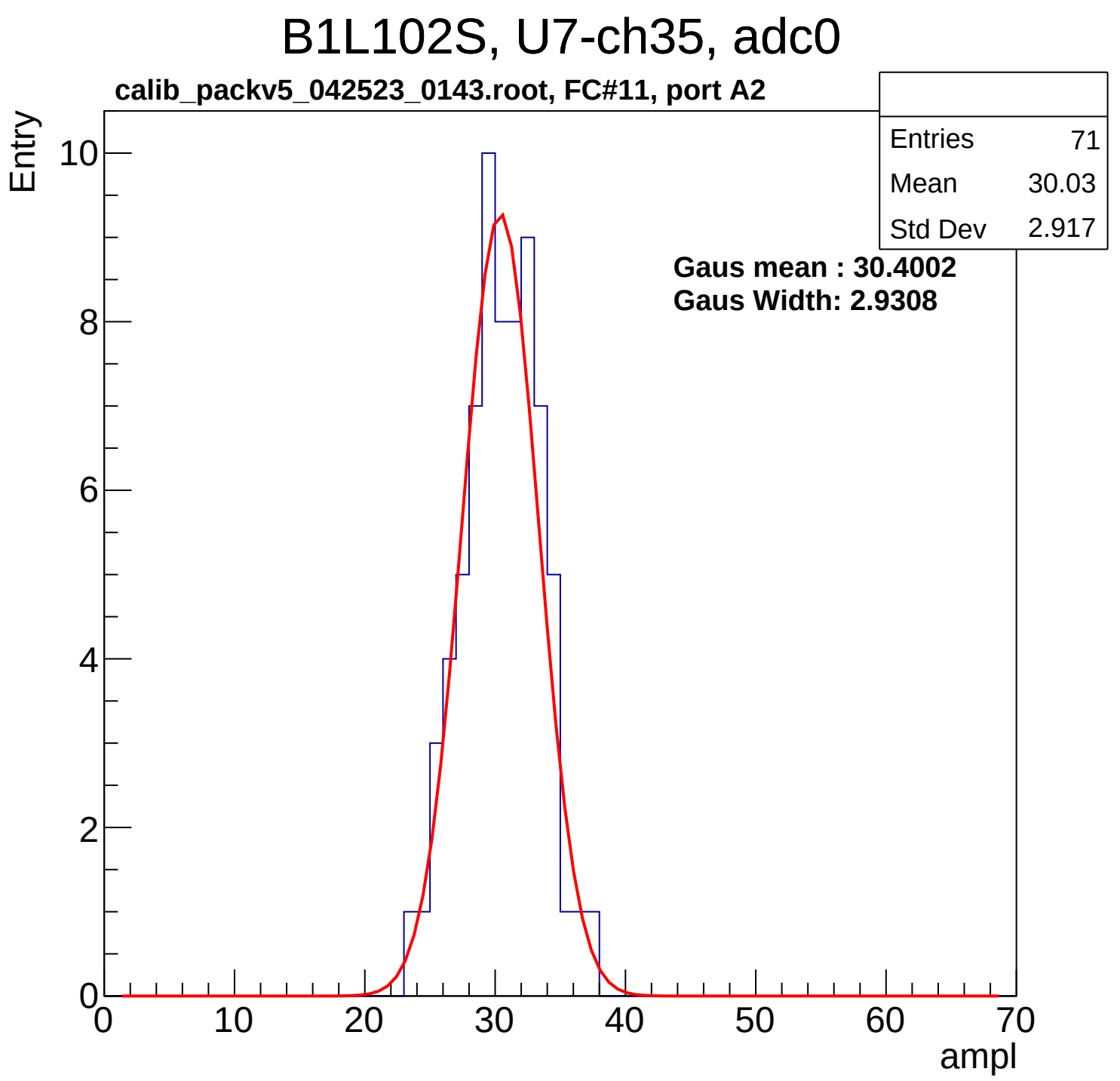
B1L102S, U7-ch35, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 71
Mean 30.03
Std Dev 2.917
Gaus mean : 30.4002
Gaus Width: 2.9308
Entry
ampl
0
2
4
6
8
10
0
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40
50
60
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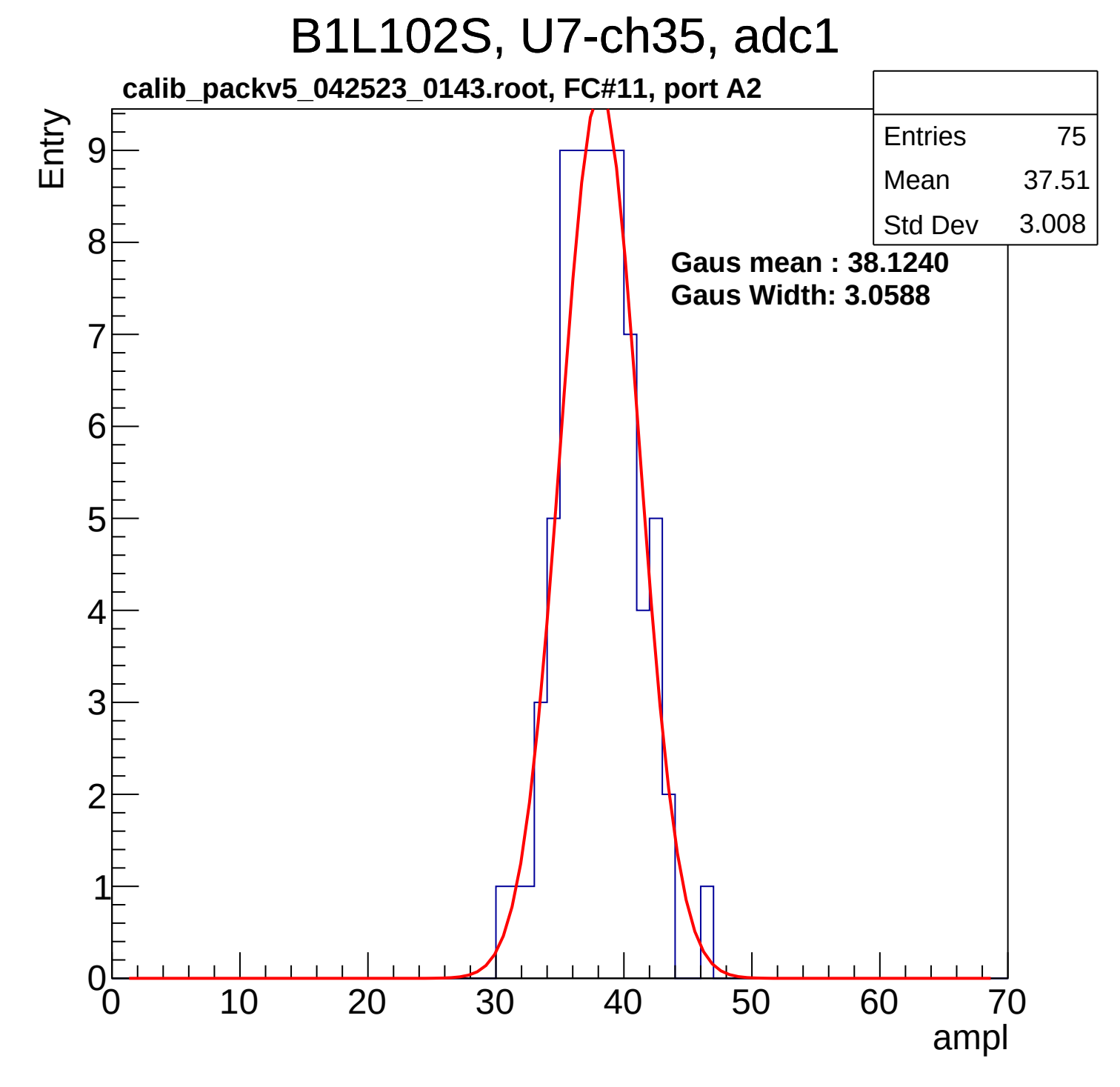
B1L102S, U7-ch35, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 75
Mean 37.51
Std Dev 3.008
Gaus mean : 38.1240
Gaus Width: 3.0588
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
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40
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60
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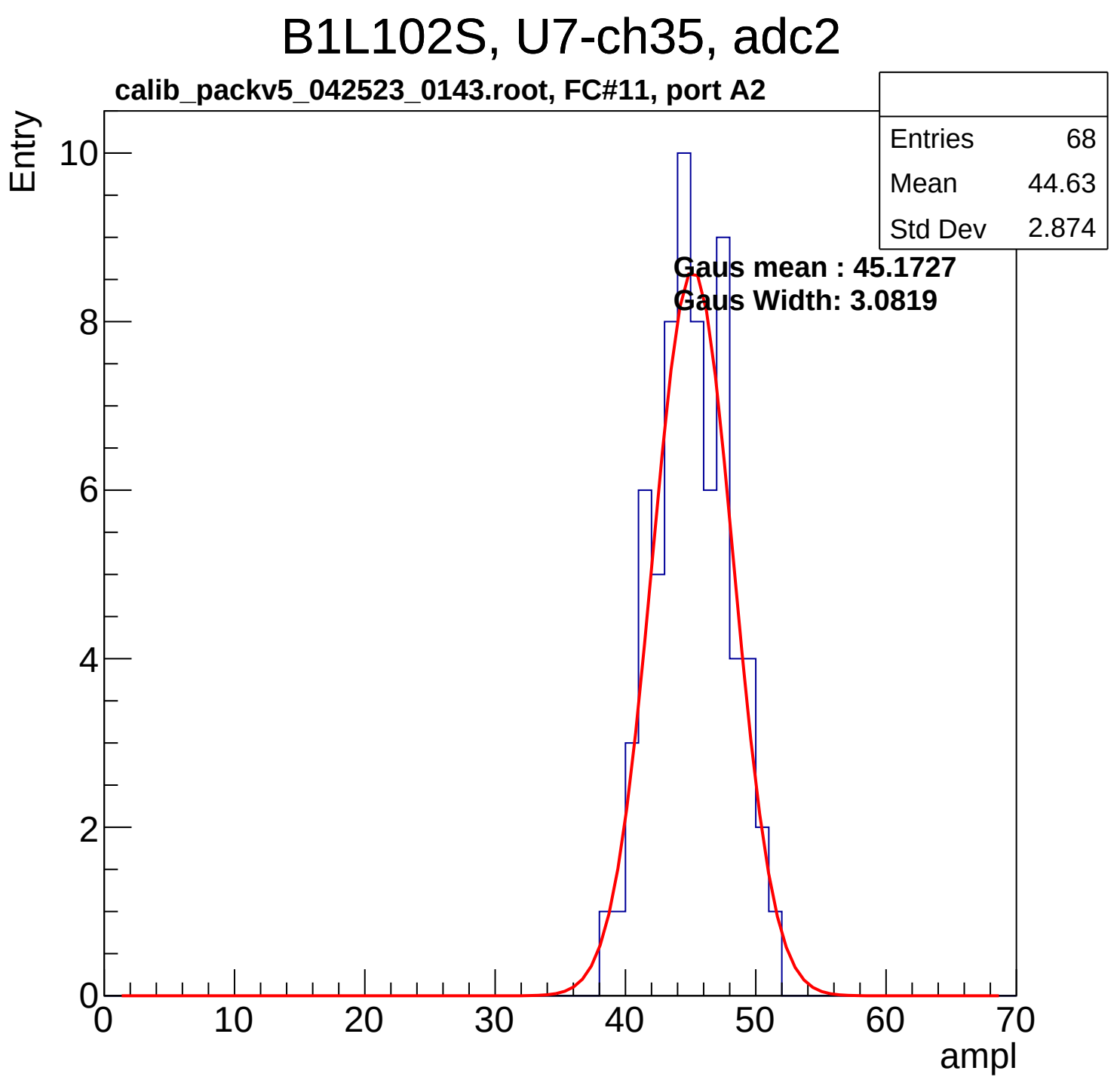
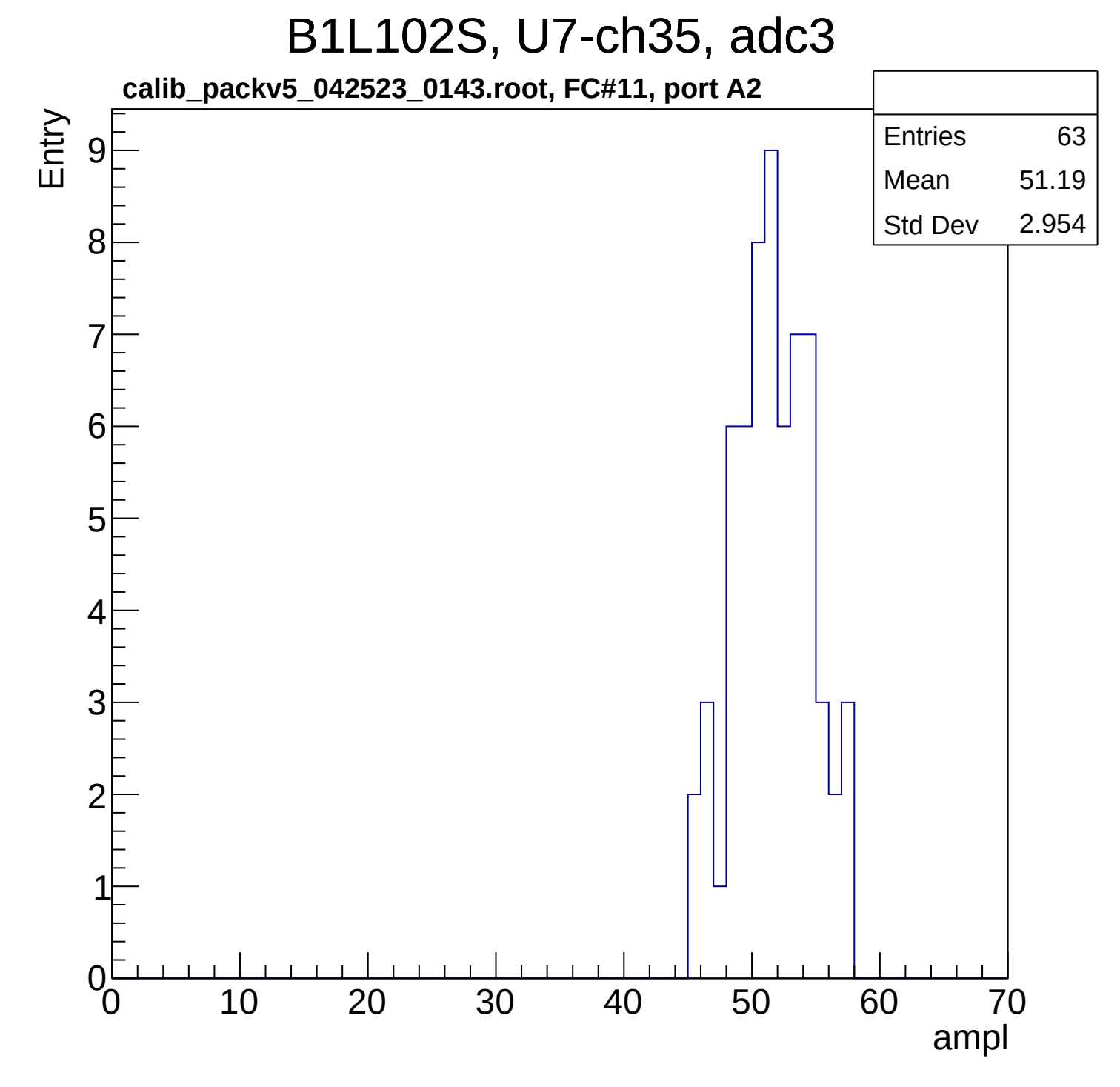

B1L102S, U7-ch35, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 68
Mean 44.63
Std Dev 2.874
Gaus mean : 45.1727
Gaus Width: 3.0819
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L102S, U7-ch35, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 63
Mean 51.19
Std Dev 2.954
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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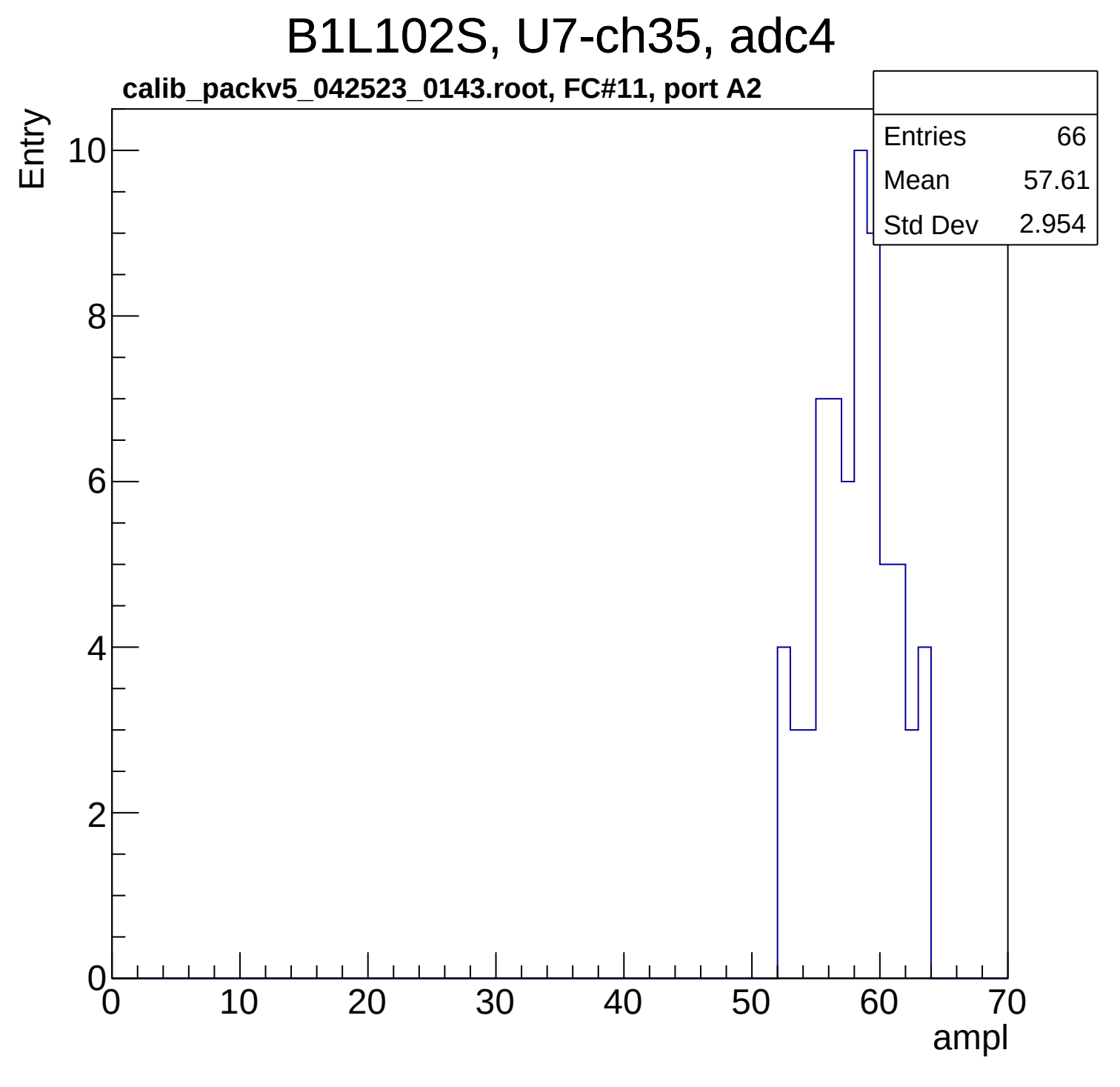
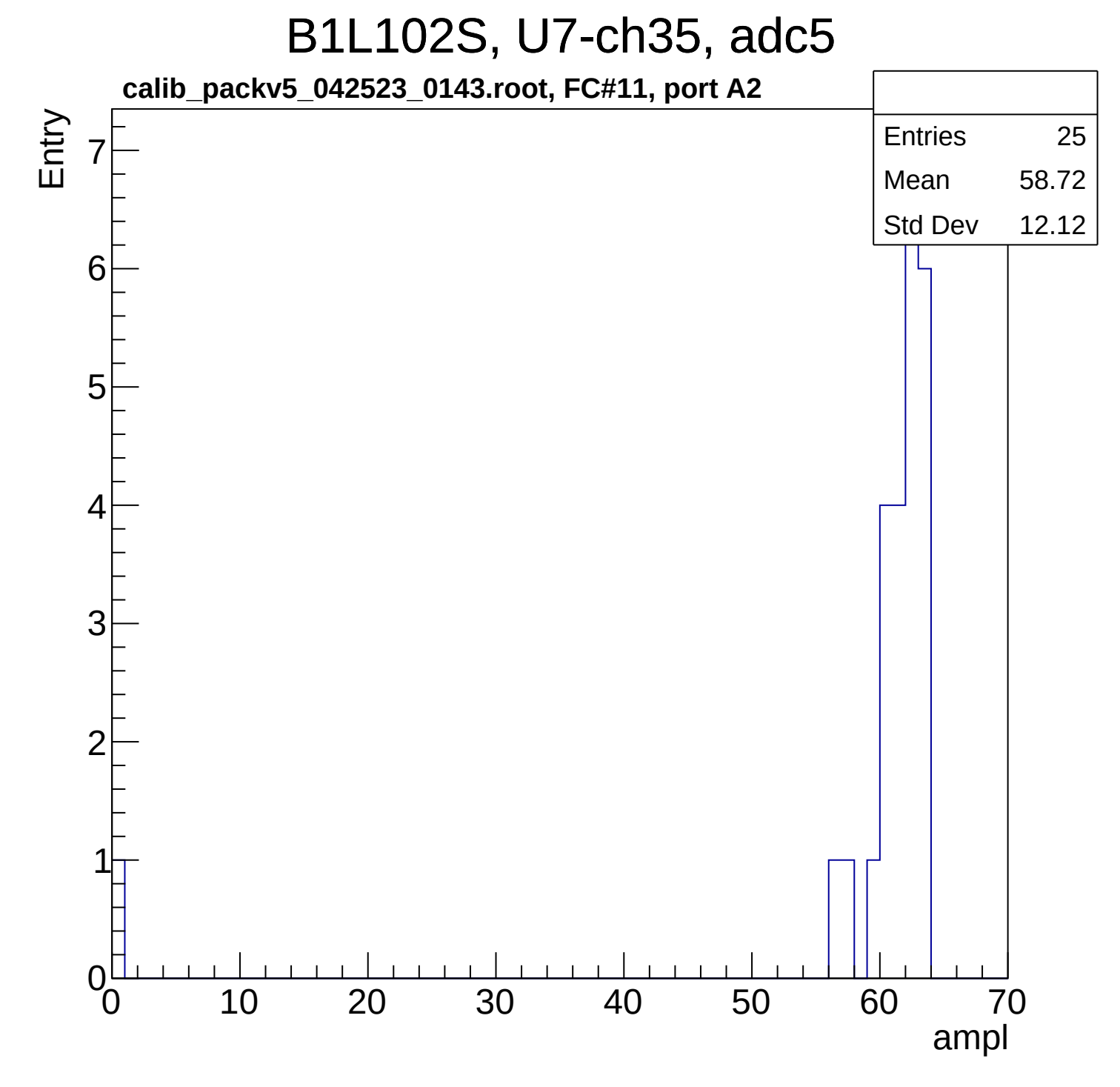
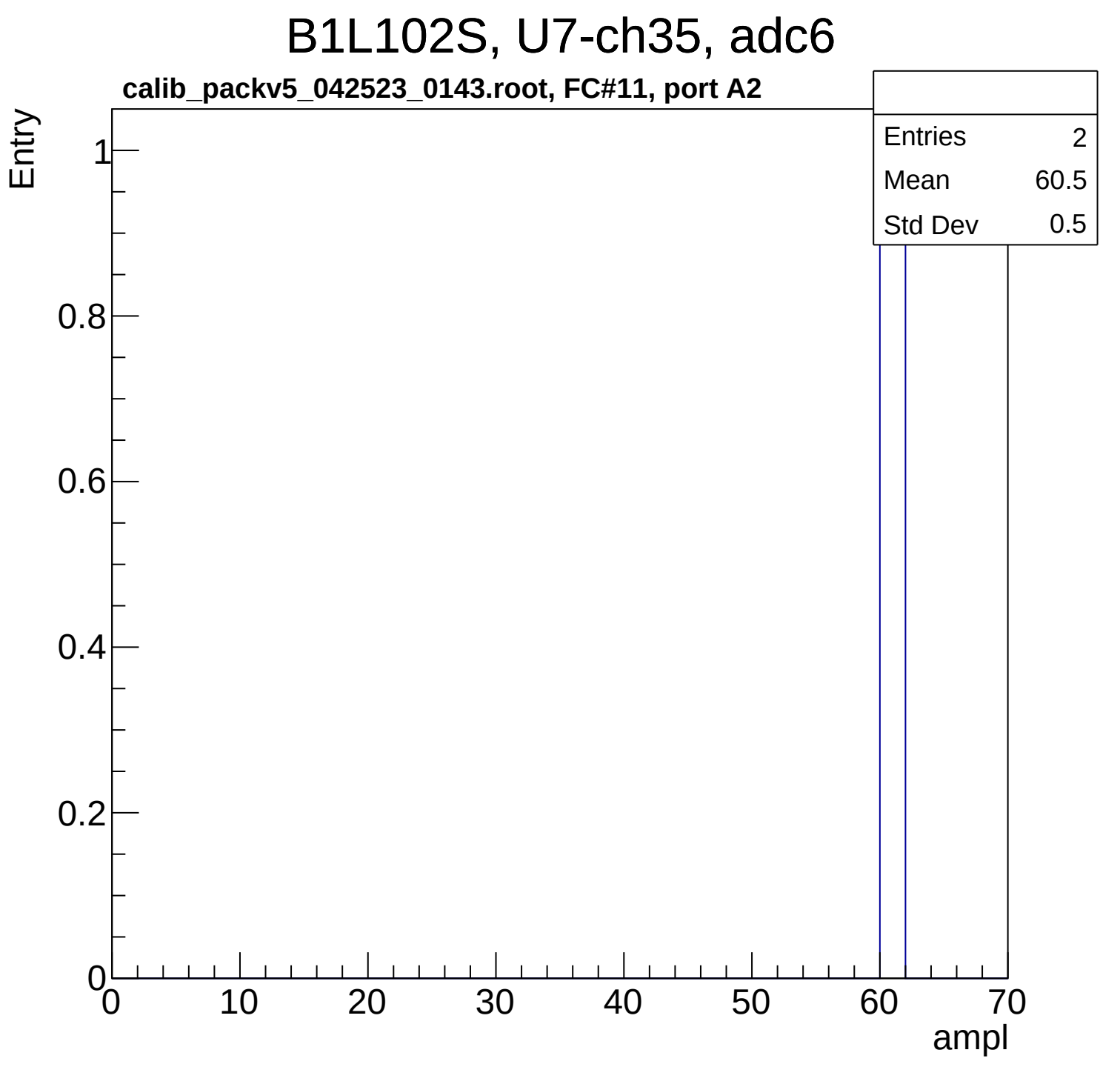
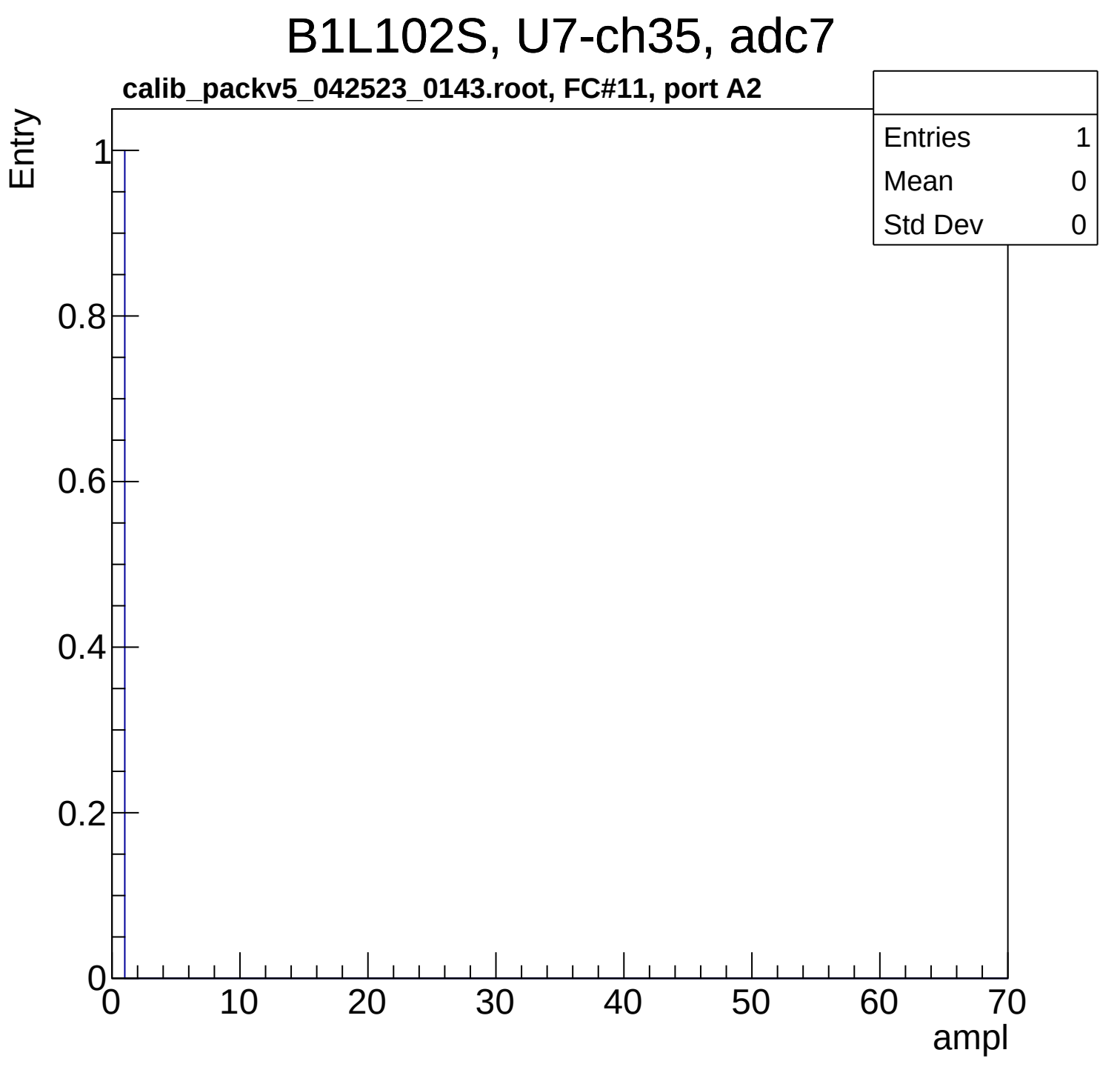
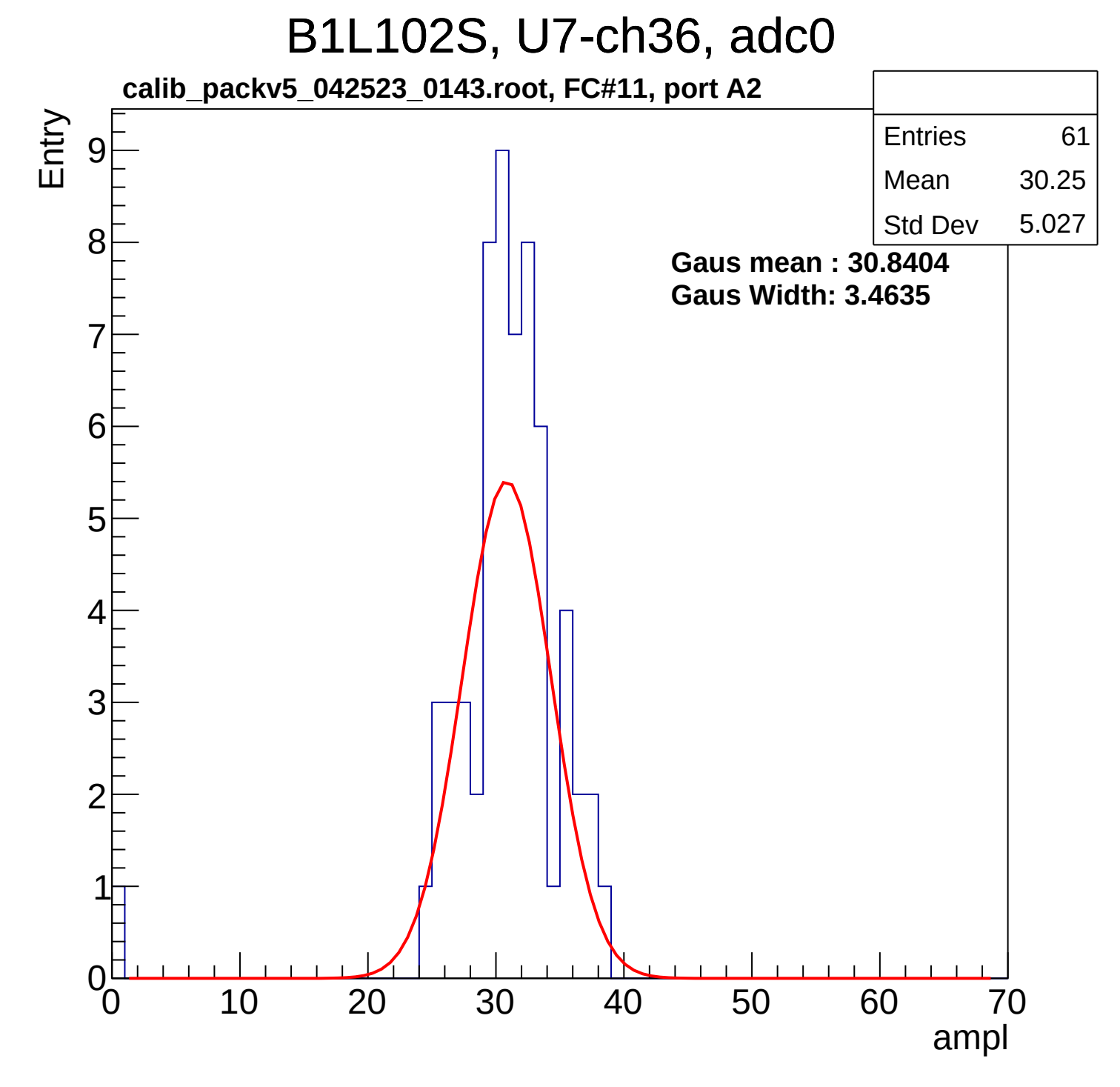

B1L102S, U7-ch35, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 66
Mean 57.61
Std Dev 2.954
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L102S, U7-ch35, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 25
Mean 58.72
Std Dev 12.12
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L102S, U7-ch35, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 2
Mean 60.5
Std Dev 0.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U7-ch35, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U7-ch36, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 61
Mean 30.25
Std Dev 5.027
Gaus mean : 30.8404
Gaus Width: 3.4635
Entry
ampl
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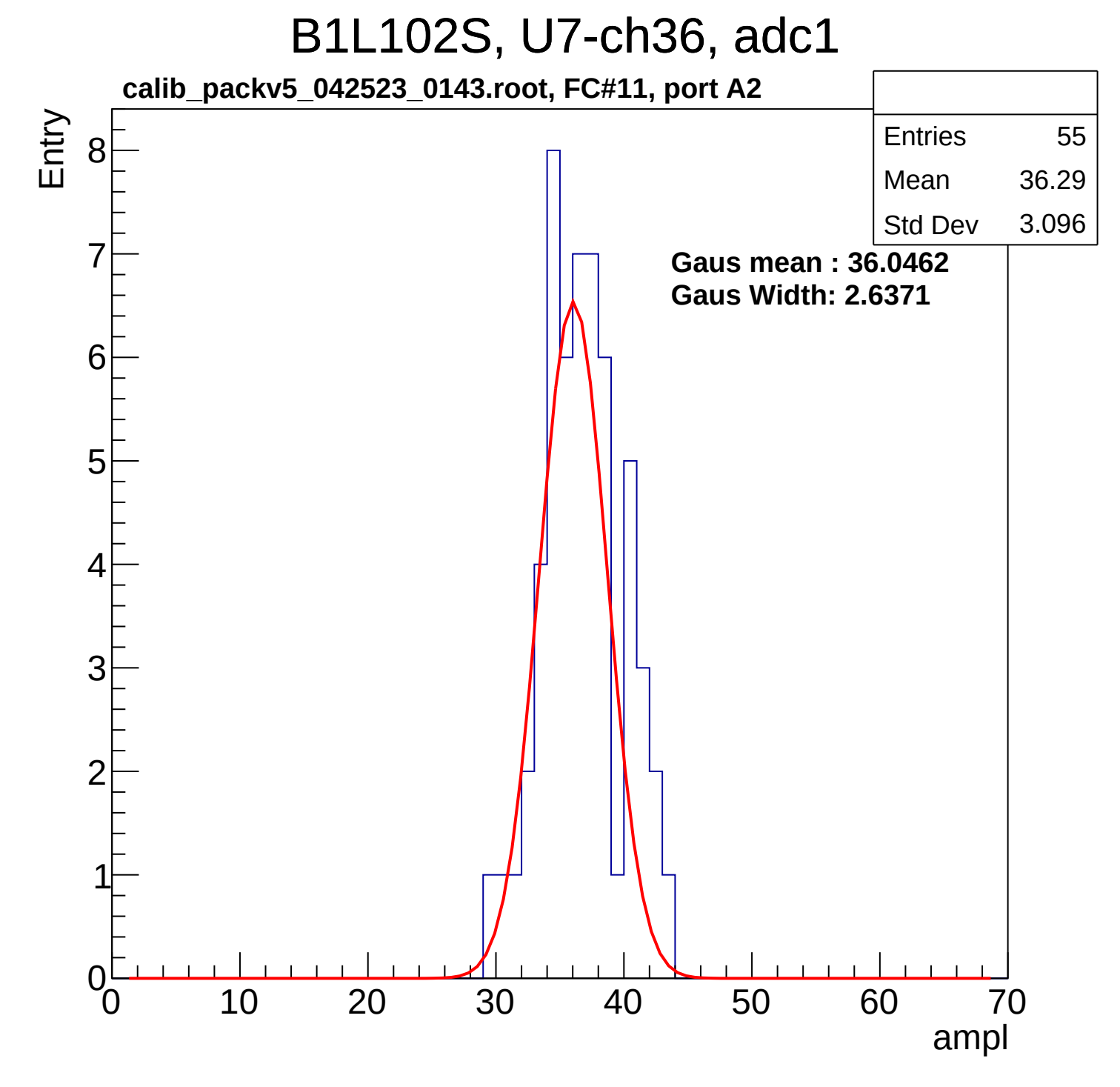
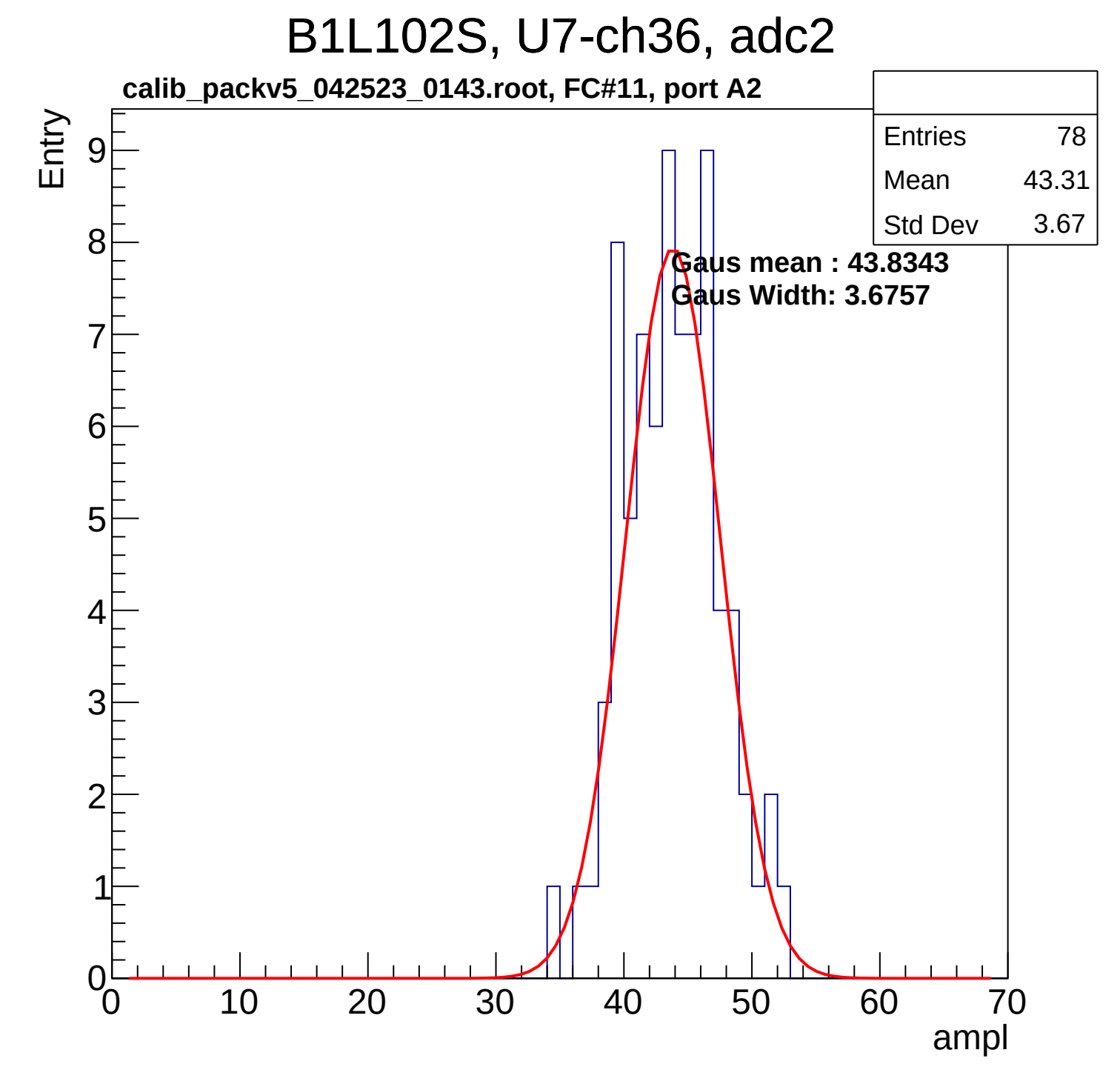
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L102S, U7-ch36, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 55
Mean 36.29
Std Dev 3.096
Gaus mean : 36.0462
Gaus Width: 2.6371
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L102S, U7-ch36, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 78
Mean 43.31
Std Dev 3.67
Gaus mean : 43.8343
Gaus Width: 3.6757
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
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60
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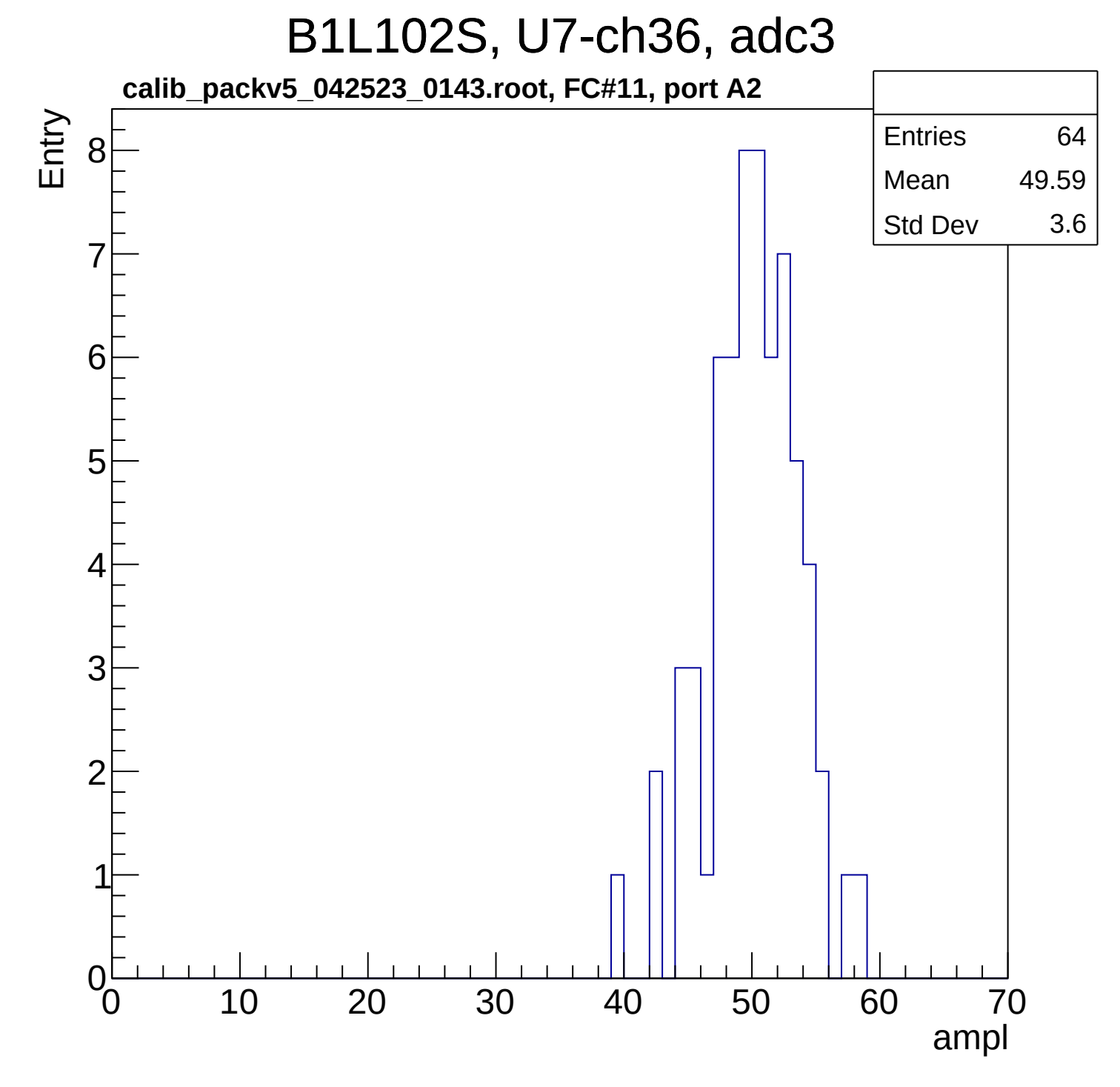
B1L102S, U7-ch36, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 64
Mean 49.59
Std Dev 3.6
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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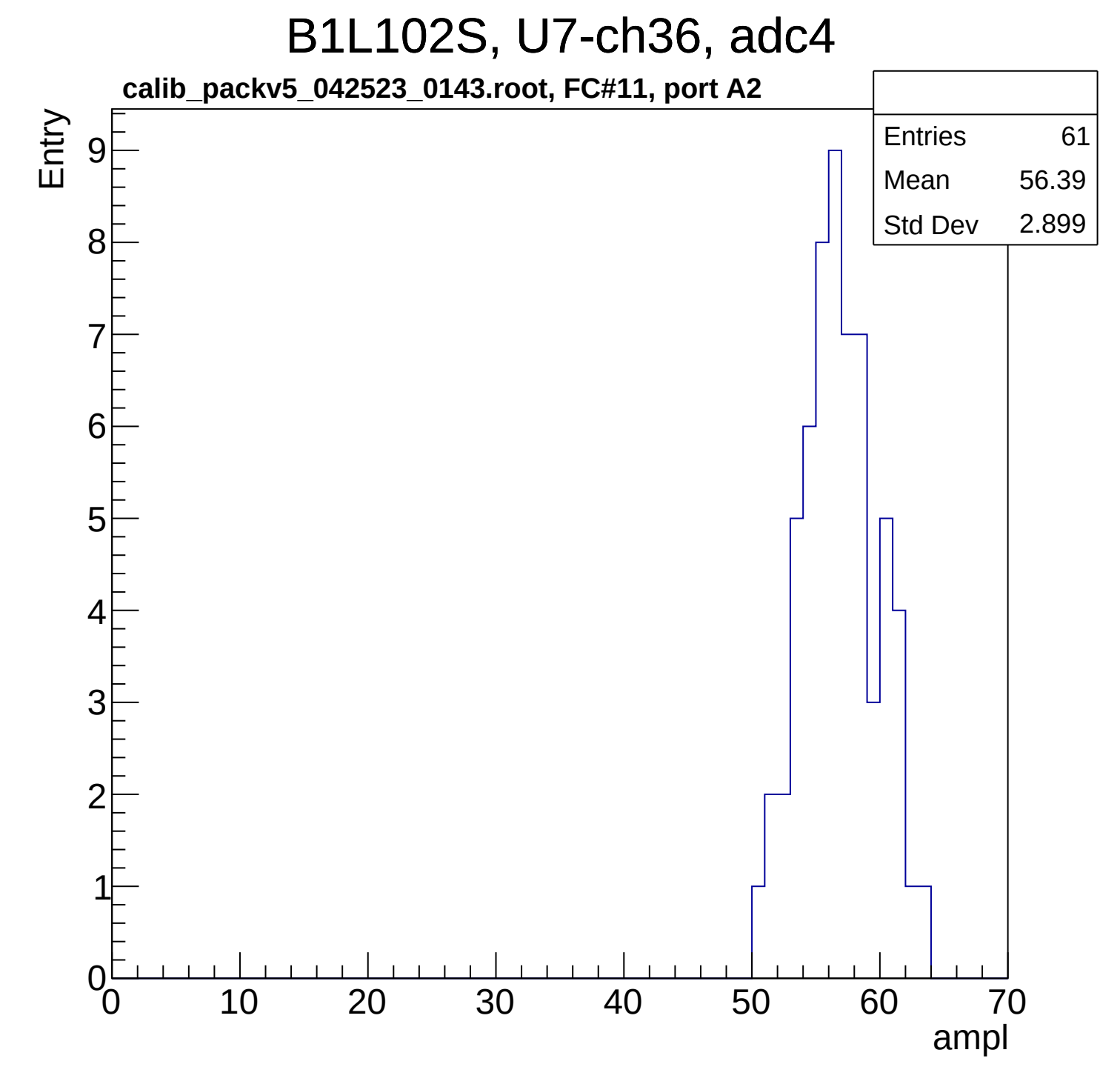
B1L102S, U7-ch36, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 61
Mean 56.39
Std Dev 2.899
Entry
ampl
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2
3
4
5
6
7
8
9
0
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60
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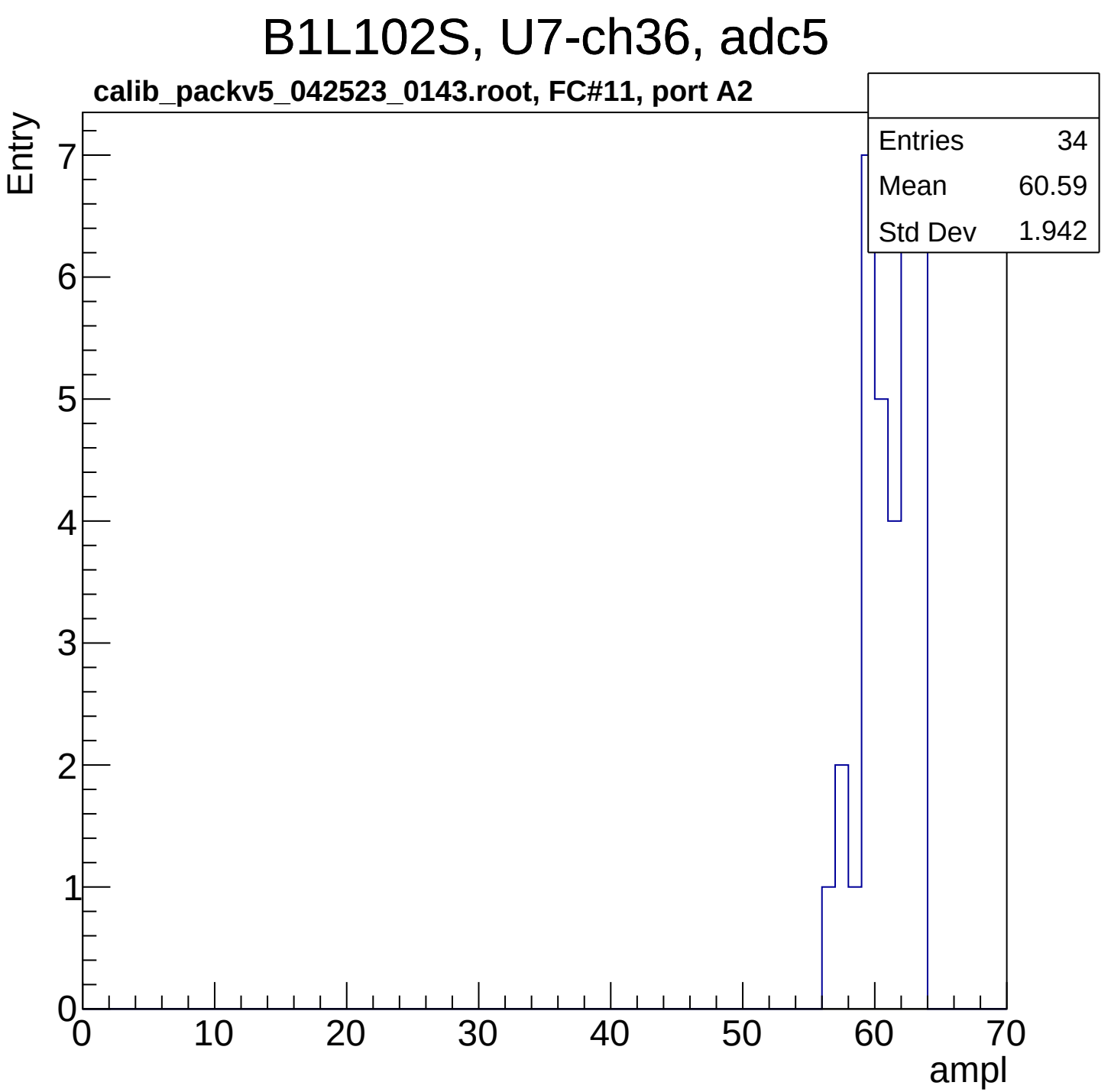
B1L102S, U7-ch36, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 34
Mean 60.59
Std Dev 1.942
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
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40
50
60
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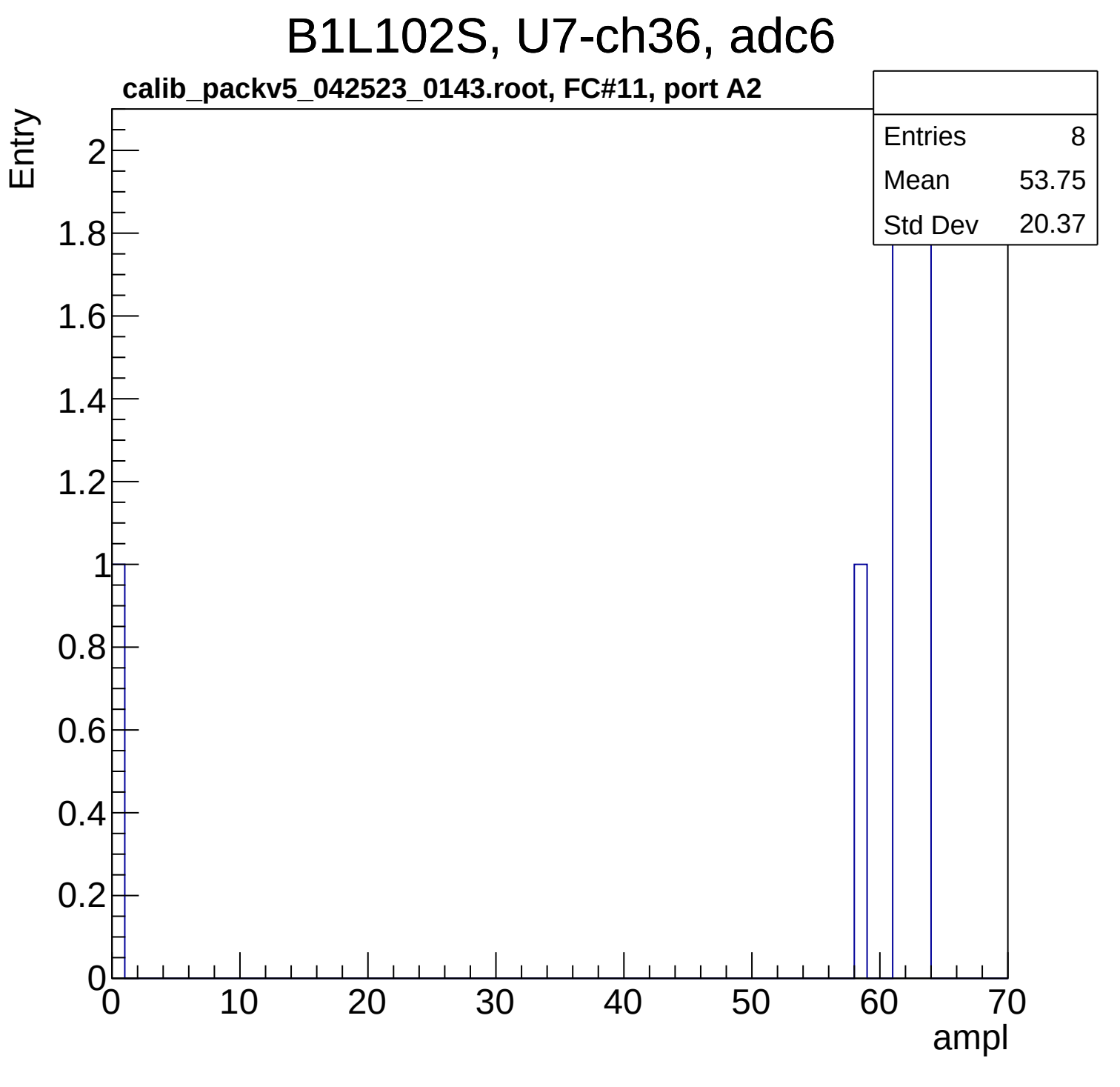
B1L102S, U7-ch36, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 8
Mean 53.75
Std Dev 20.37
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
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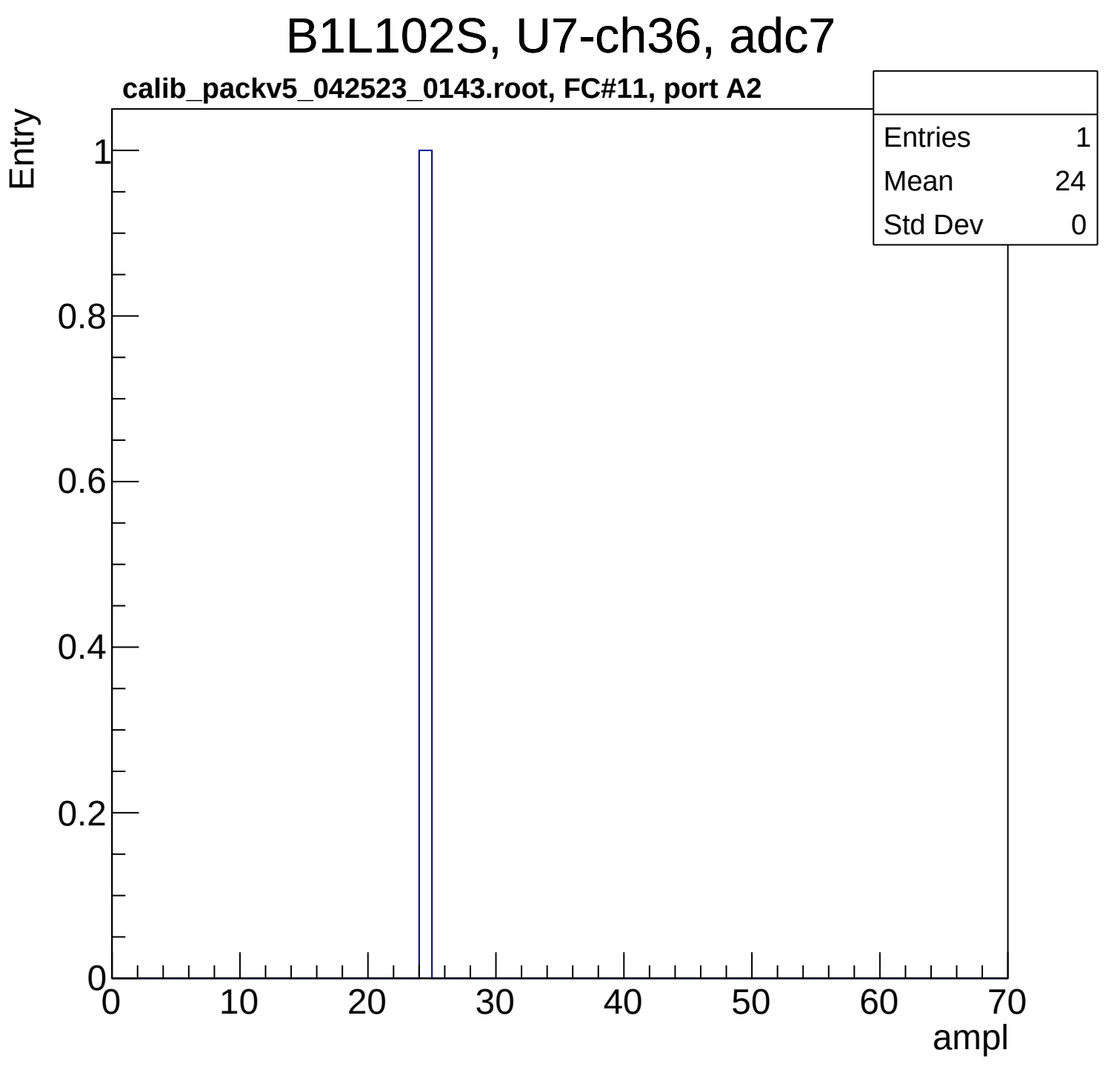
40
50
60
70


B1L102S, U7-ch36, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 1
Mean 24
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
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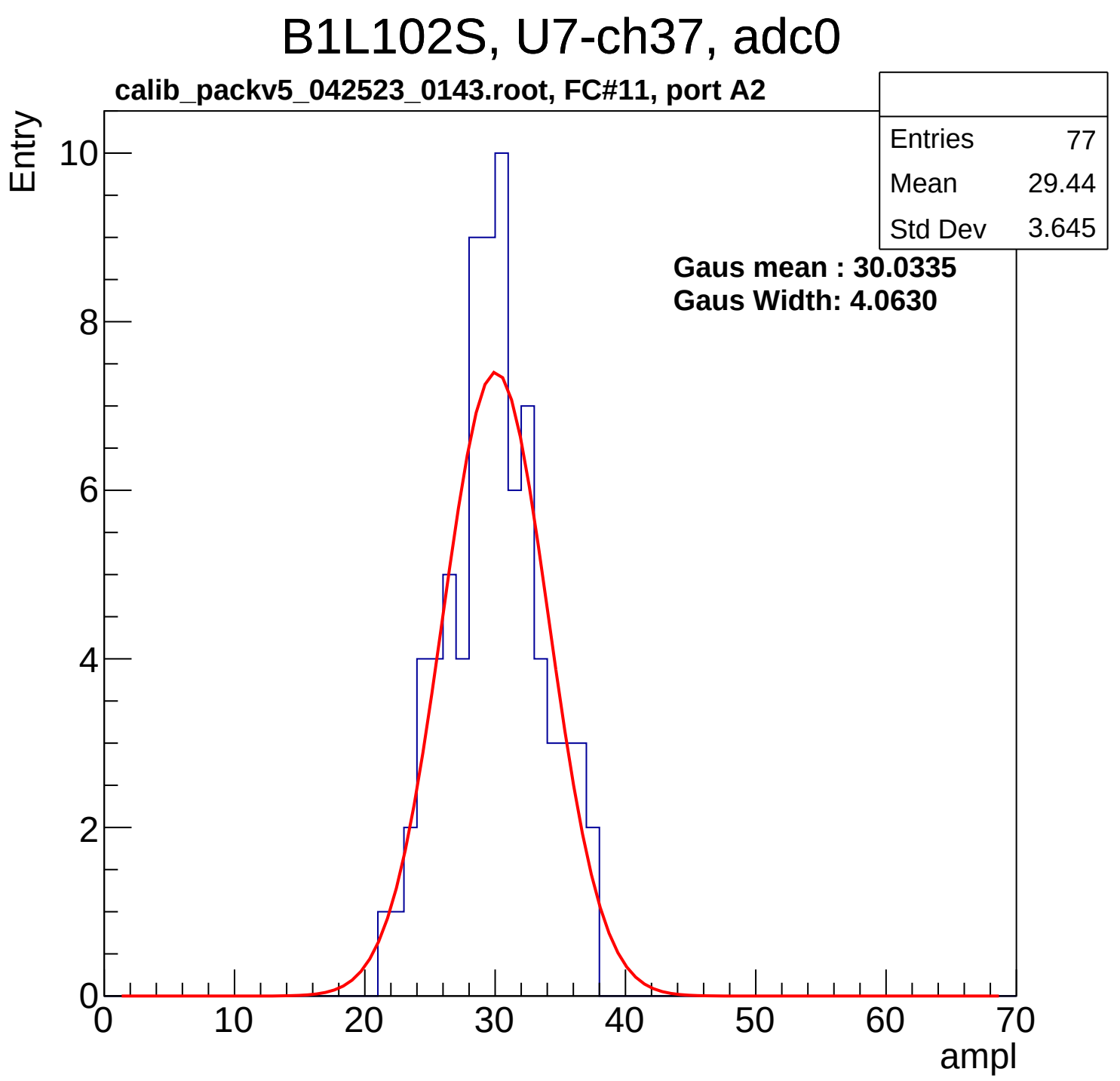
50
60
70
ampl


B1L102S, U7-ch37, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 77
Mean 29.44
Std Dev 3.645
Gaus mean : 30.0335
Gaus Width: 4.0630
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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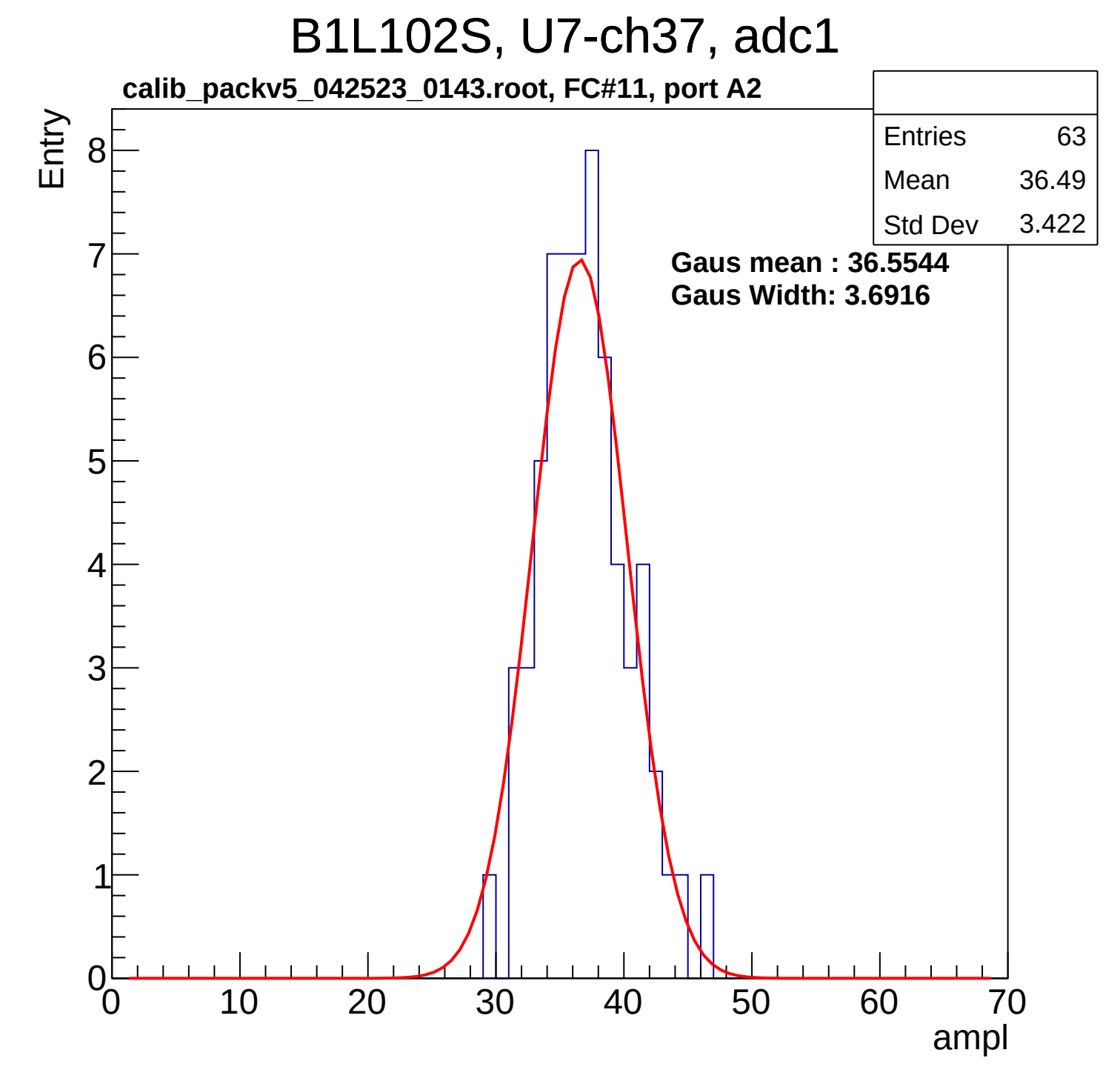
B1L102S, U7-ch37, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 63
Mean 36.49
Std Dev 3.422
Gaus mean : 36.5544
Gaus Width: 3.6916
Entry
ampl
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1
2
3
4
5
6
7
8
0
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40
50
60
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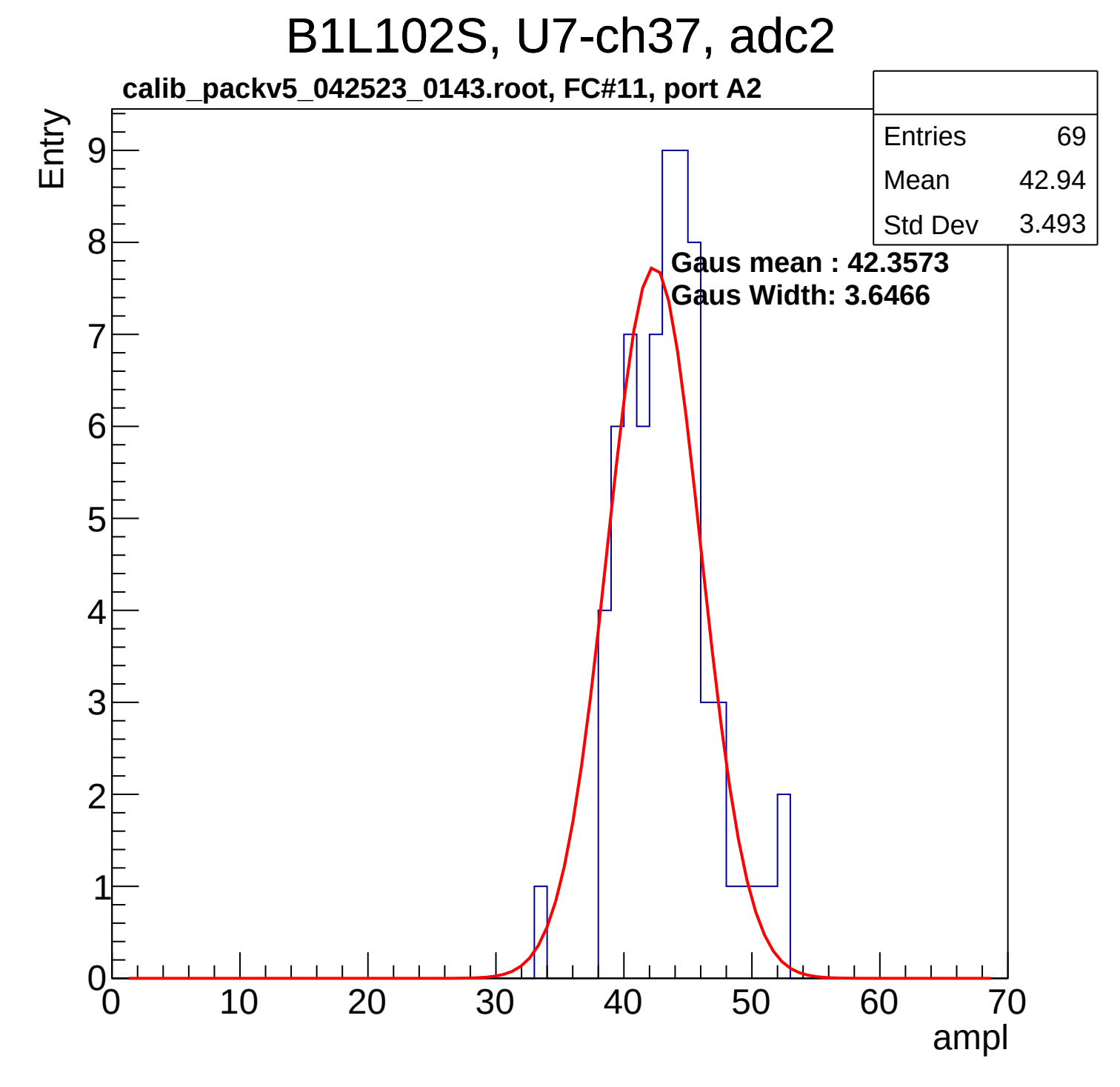
B1L102S, U7-ch37, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 69
Mean 42.94
Std Dev 3.493
Gaus mean : 42.3573
Gaus Width: 3.6466
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
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20
30
40
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60
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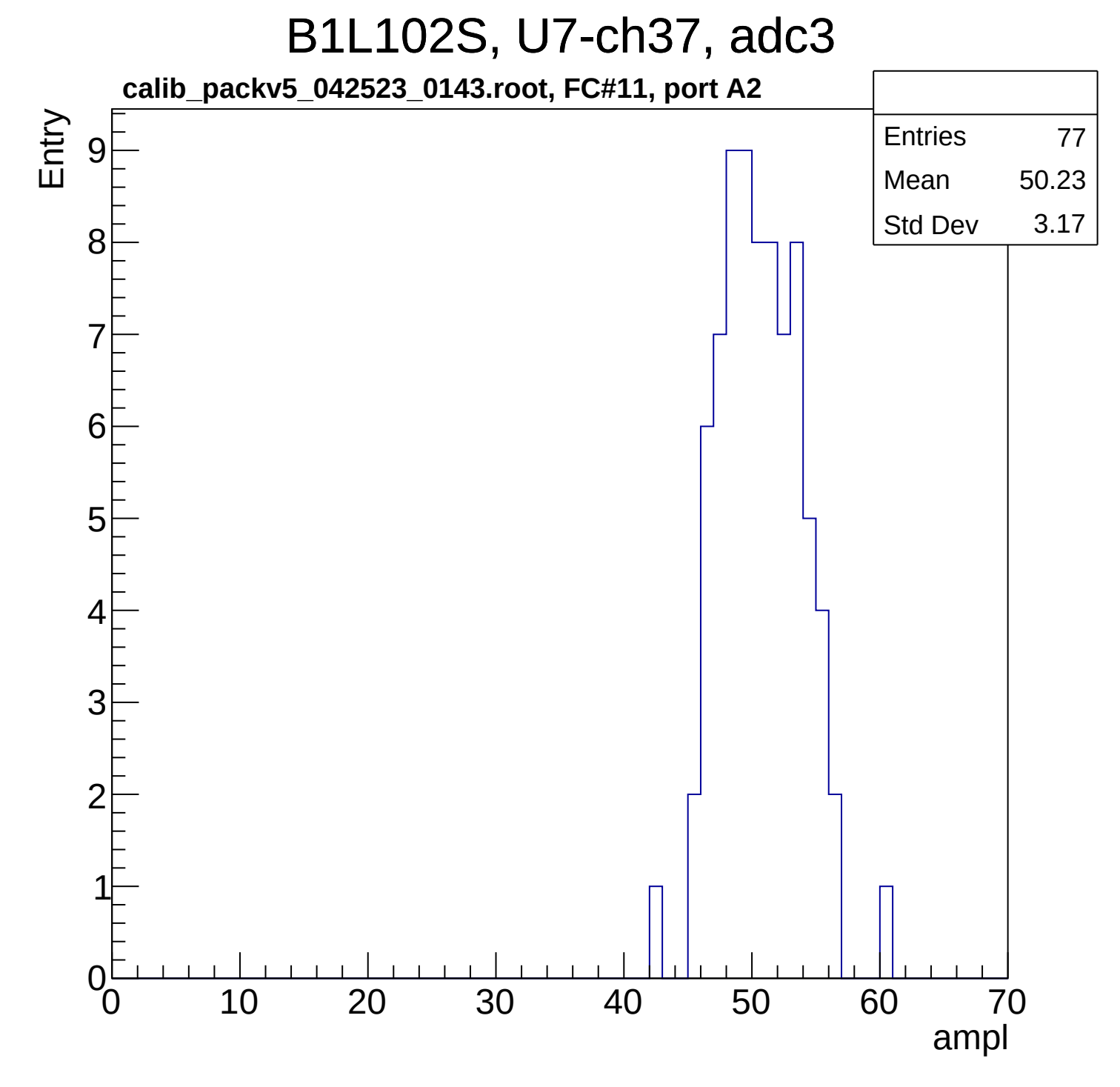
B1L102S, U7-ch37, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 77
Mean 50.23
Std Dev 3.17
Entry
ampl
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3
4
5
6
7
8
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0
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20
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40
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60
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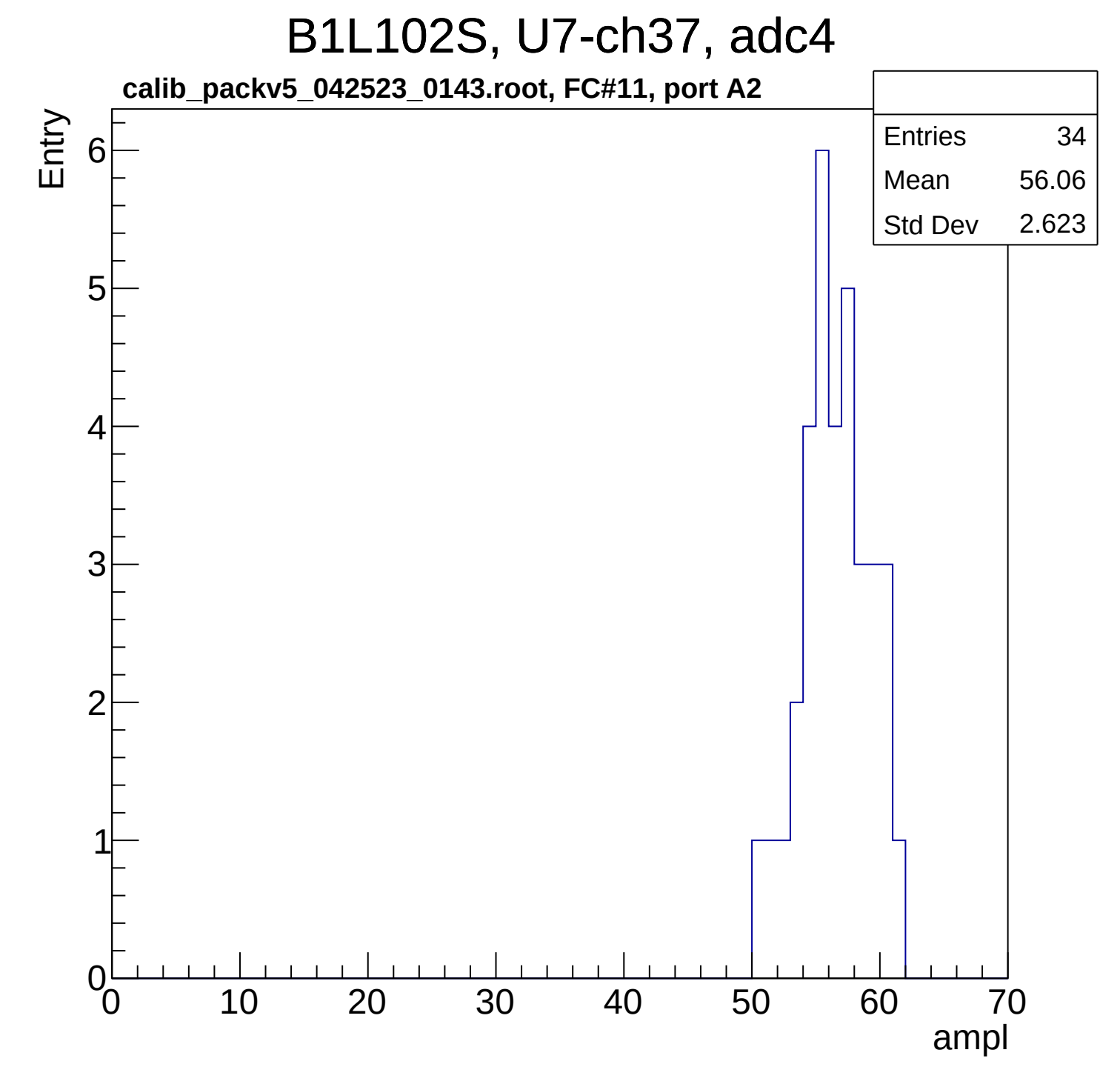
B1L102S, U7-ch37, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 34
Mean 56.06
Std Dev 2.623
Entry
ampl
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2
3
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0
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20
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40
50
60
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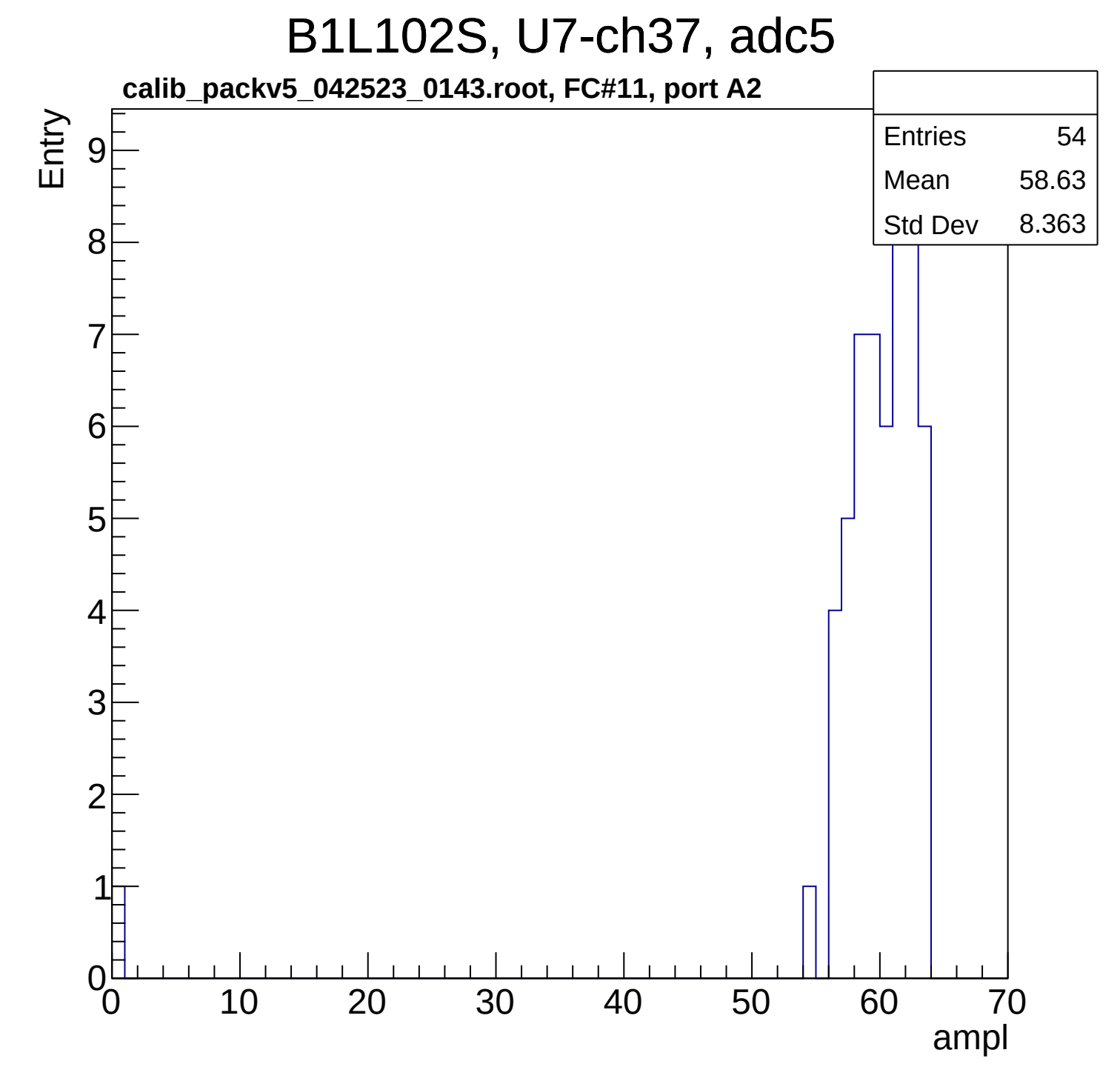
B1L102S, U7-ch37, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 54
Mean 58.63
Std Dev 8.363
Entry
ampl
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2
3
4
5
6
7
8
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0
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20
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40
50
60
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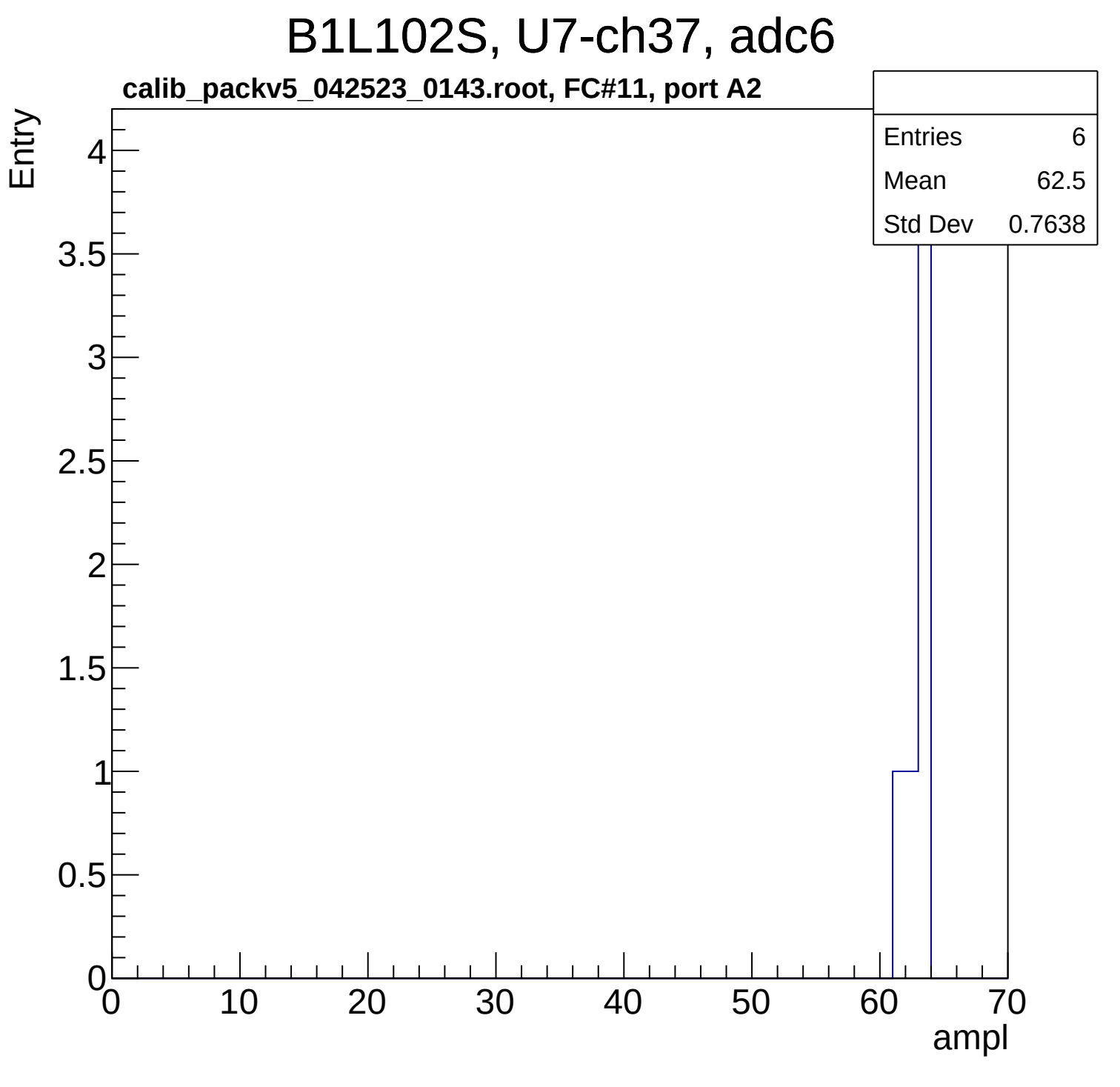
B1L102S, U7-ch37, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 6
Mean 62.5
Std Dev 0.7638
Entry
ampl
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0.5
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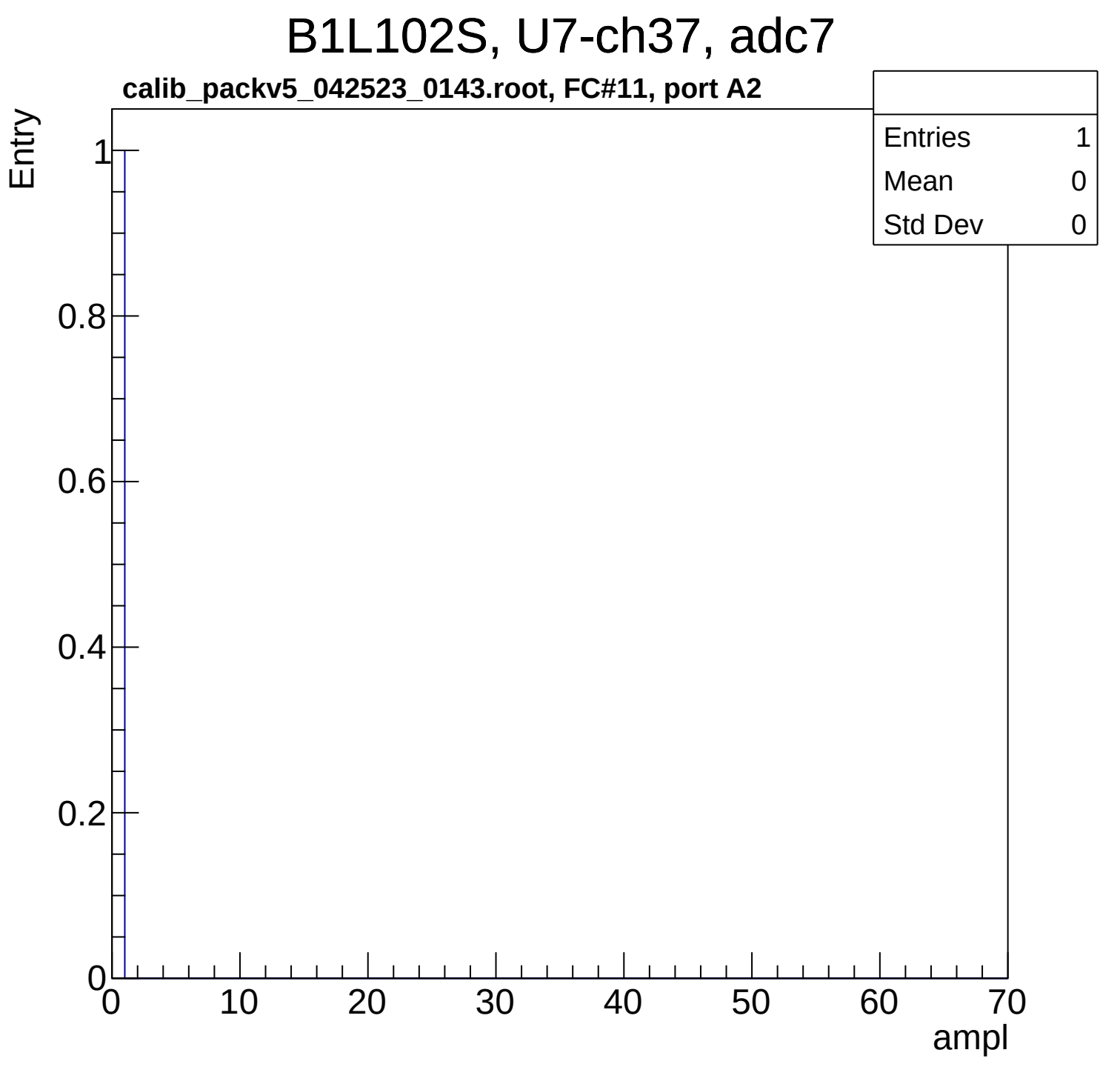
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L102S, U7-ch37, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 1
Mean 0
Std Dev 0
Entry
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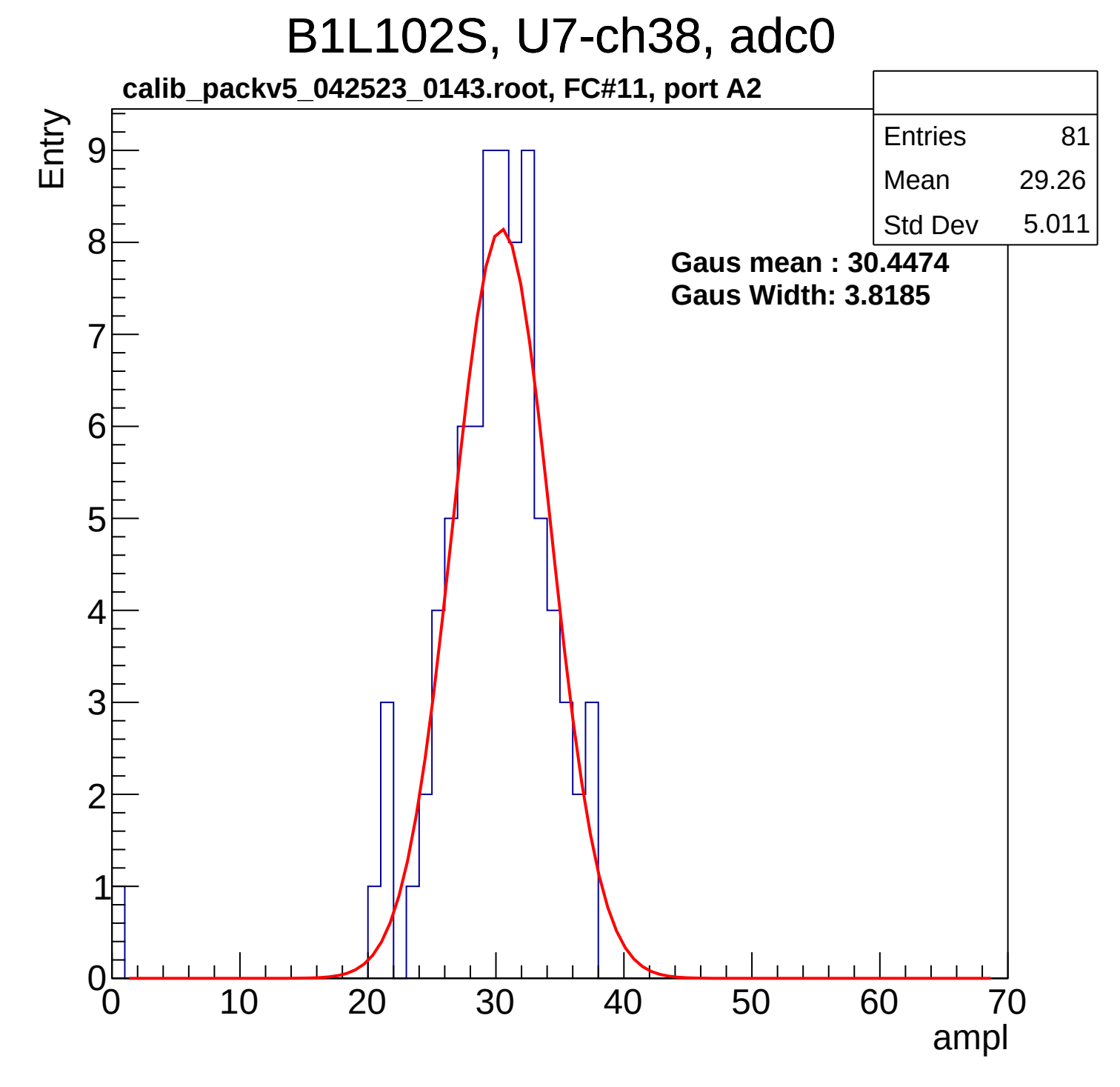
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U7-ch38, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 81
Mean 29.26
Std Dev 5.011
Gaus mean : 30.4474
Gaus Width: 3.8185
Entry
ampl
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1
2
3
4
5
6
7
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0
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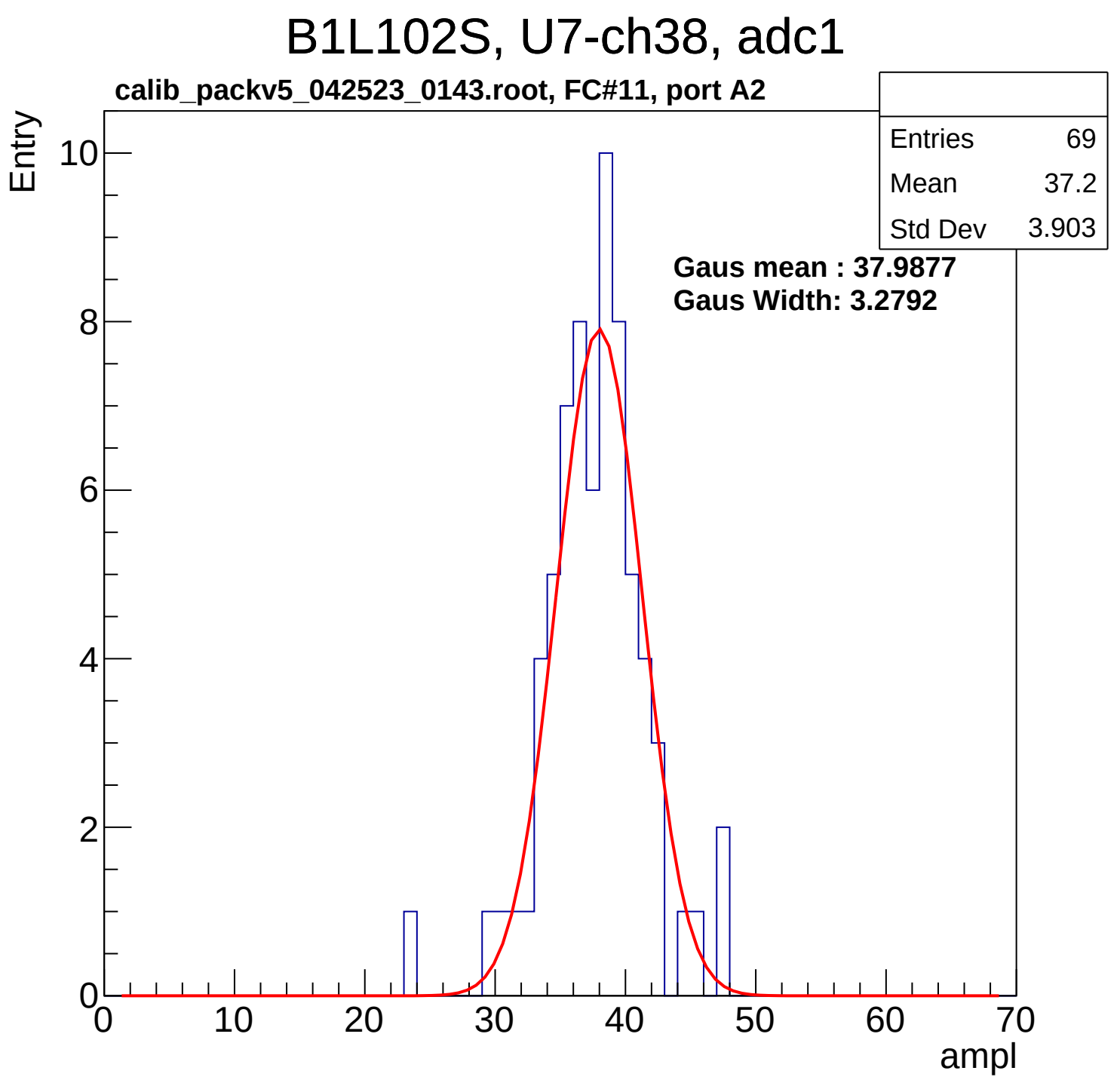
B1L102S, U7-ch38, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 69
Mean 37.2
Std Dev 3.903
Gaus mean : 37.9877
Gaus Width: 3.2792
Entry
ampl
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4
6
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0
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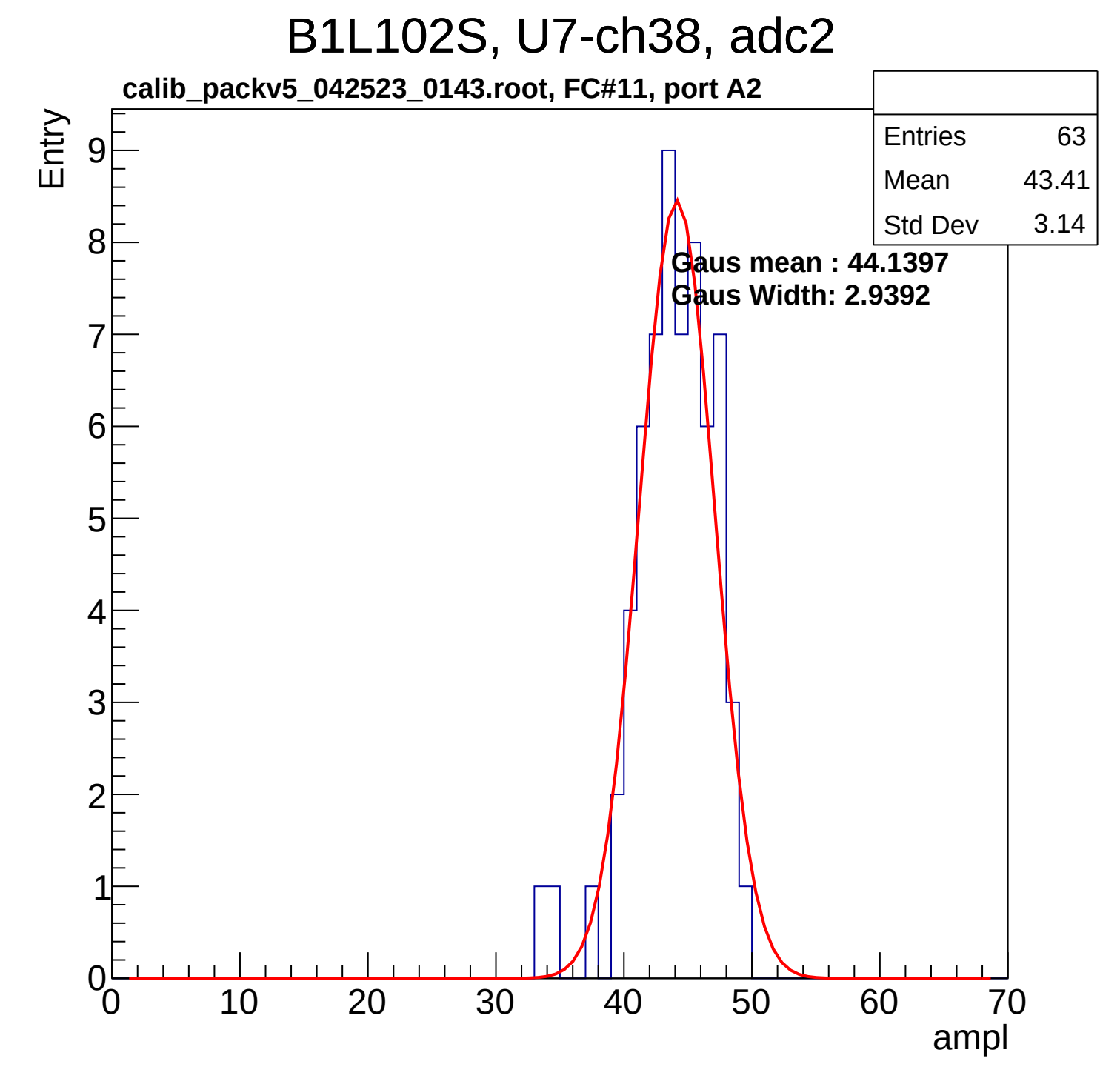
B1L102S, U7-ch38, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 63
Mean 43.41
Std Dev 3.14
Gaus mean : 44.1397
Gaus Width: 2.9392
Entry
ampl
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2
3
4
5
6
7
8
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0
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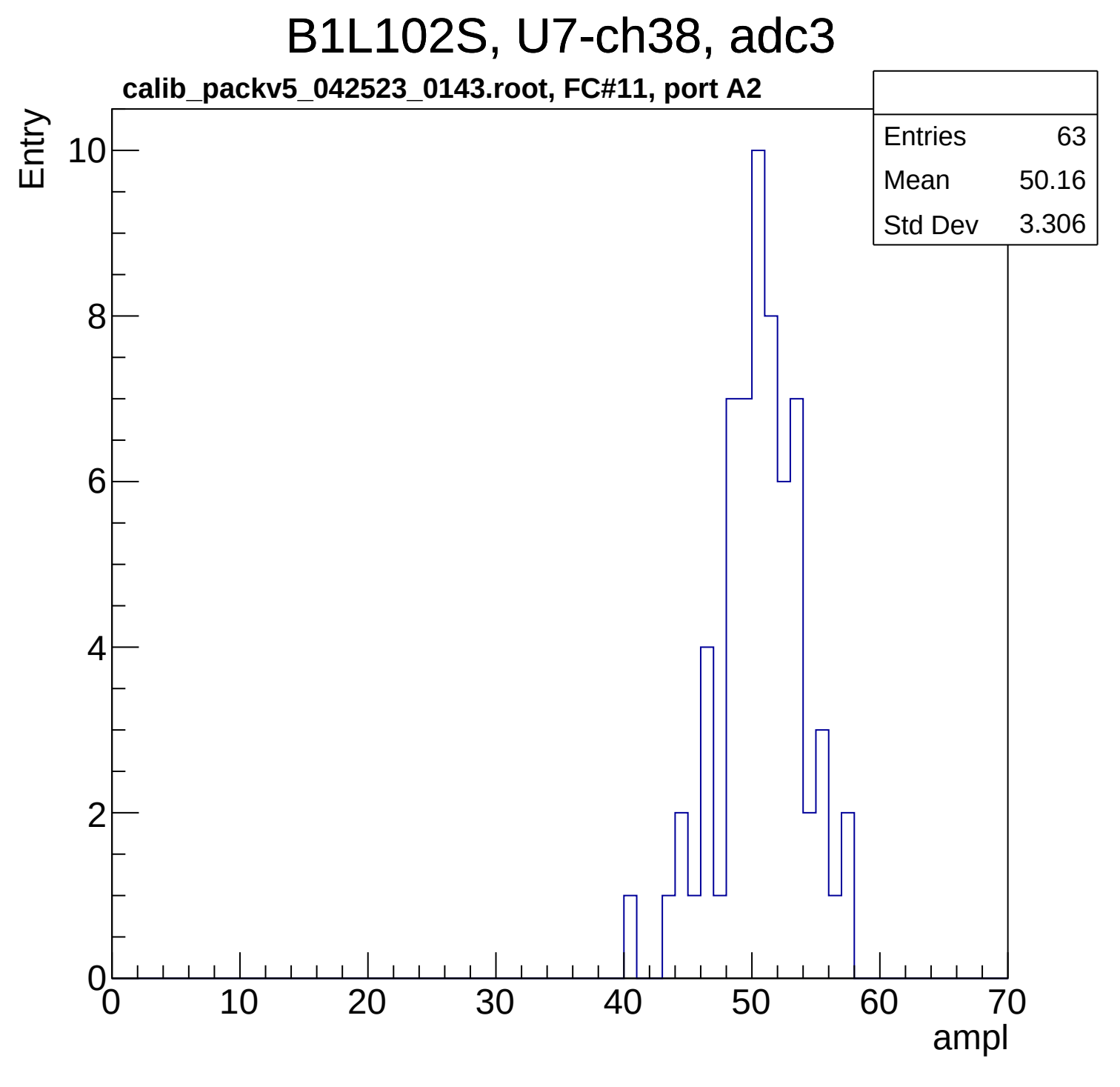
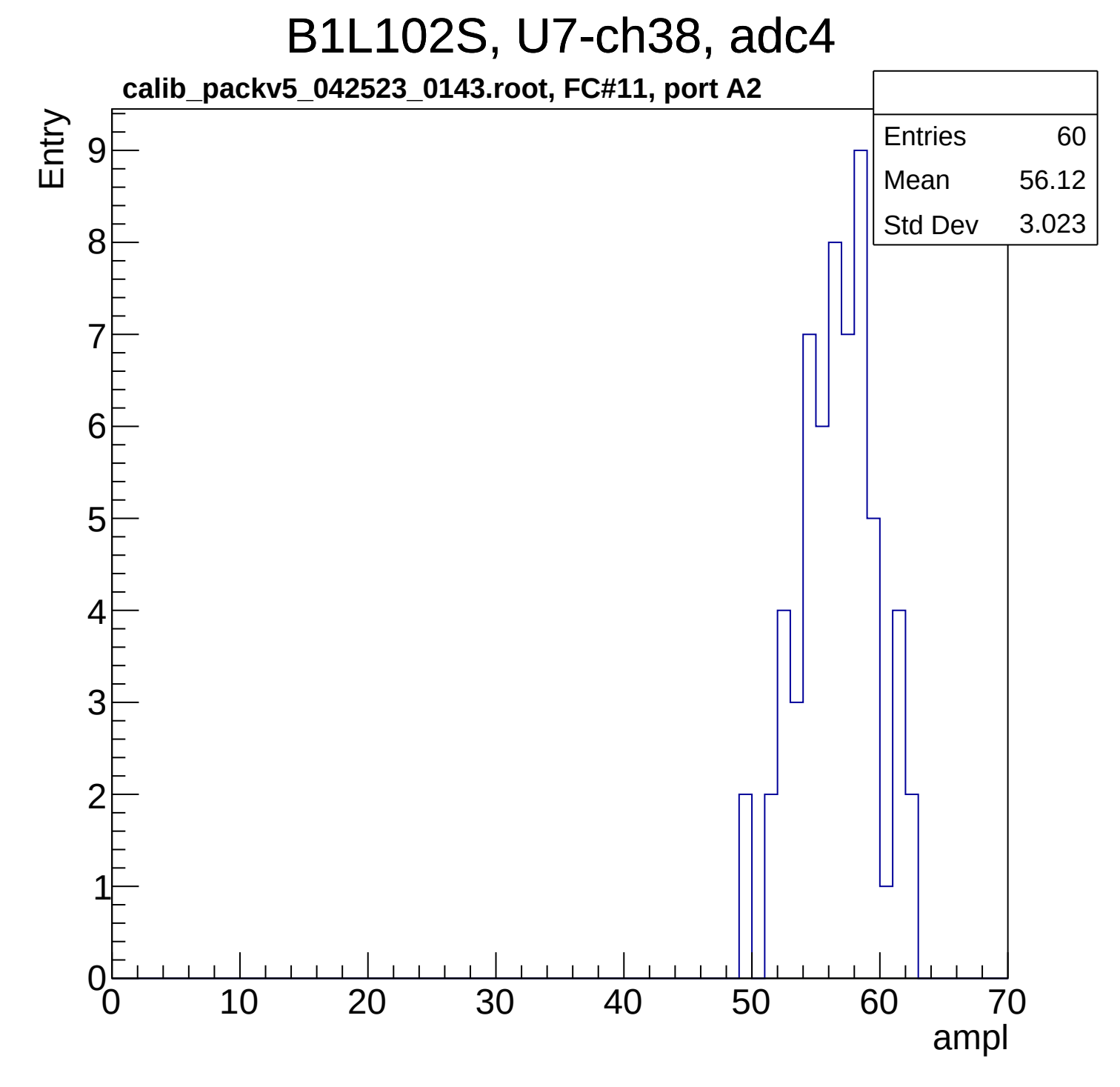

B1L102S, U7-ch38, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 63
Mean 50.16
Std Dev 3.306
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L102S, U7-ch38, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 60
Mean 56.12
Std Dev 3.023
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
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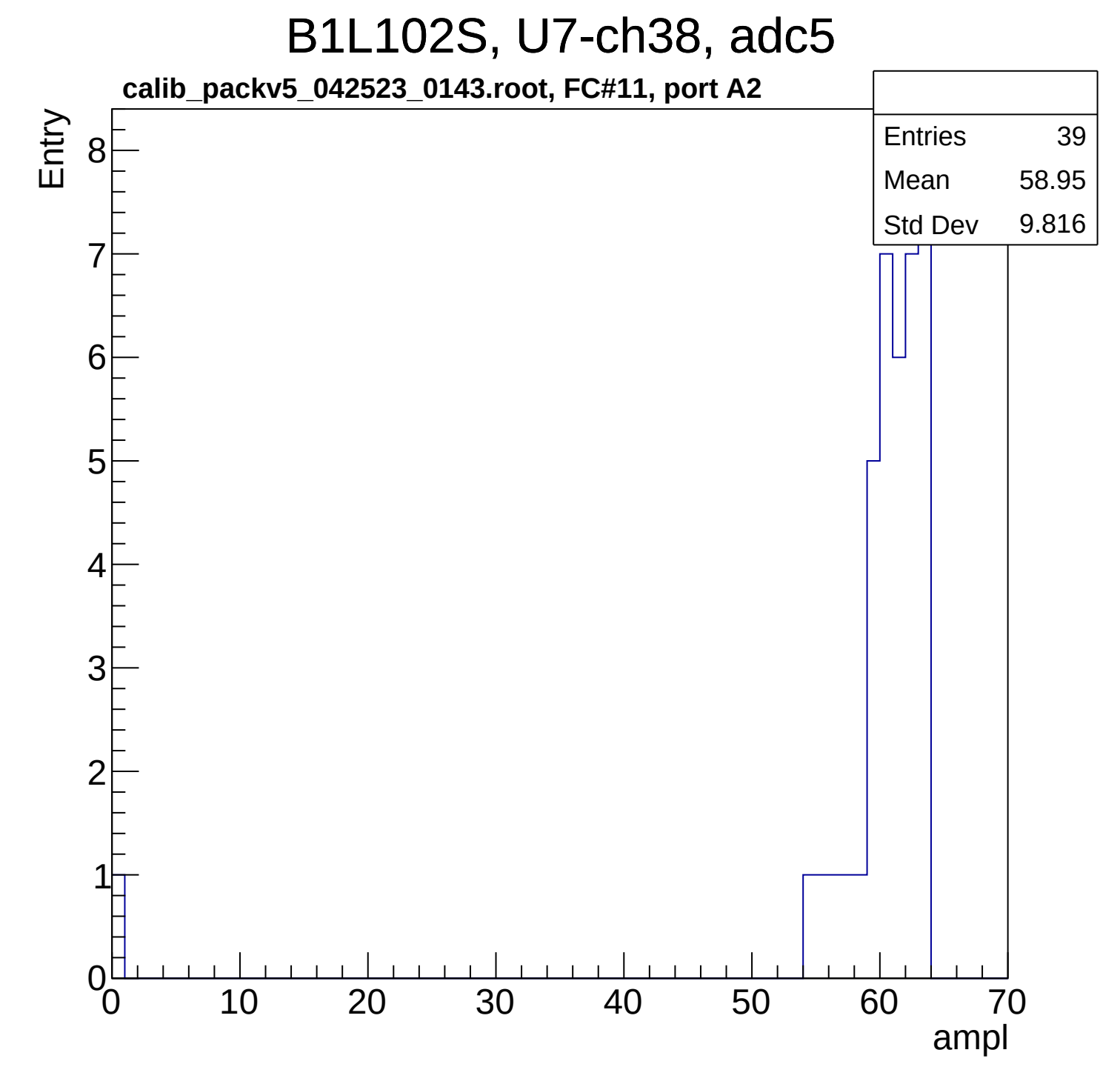
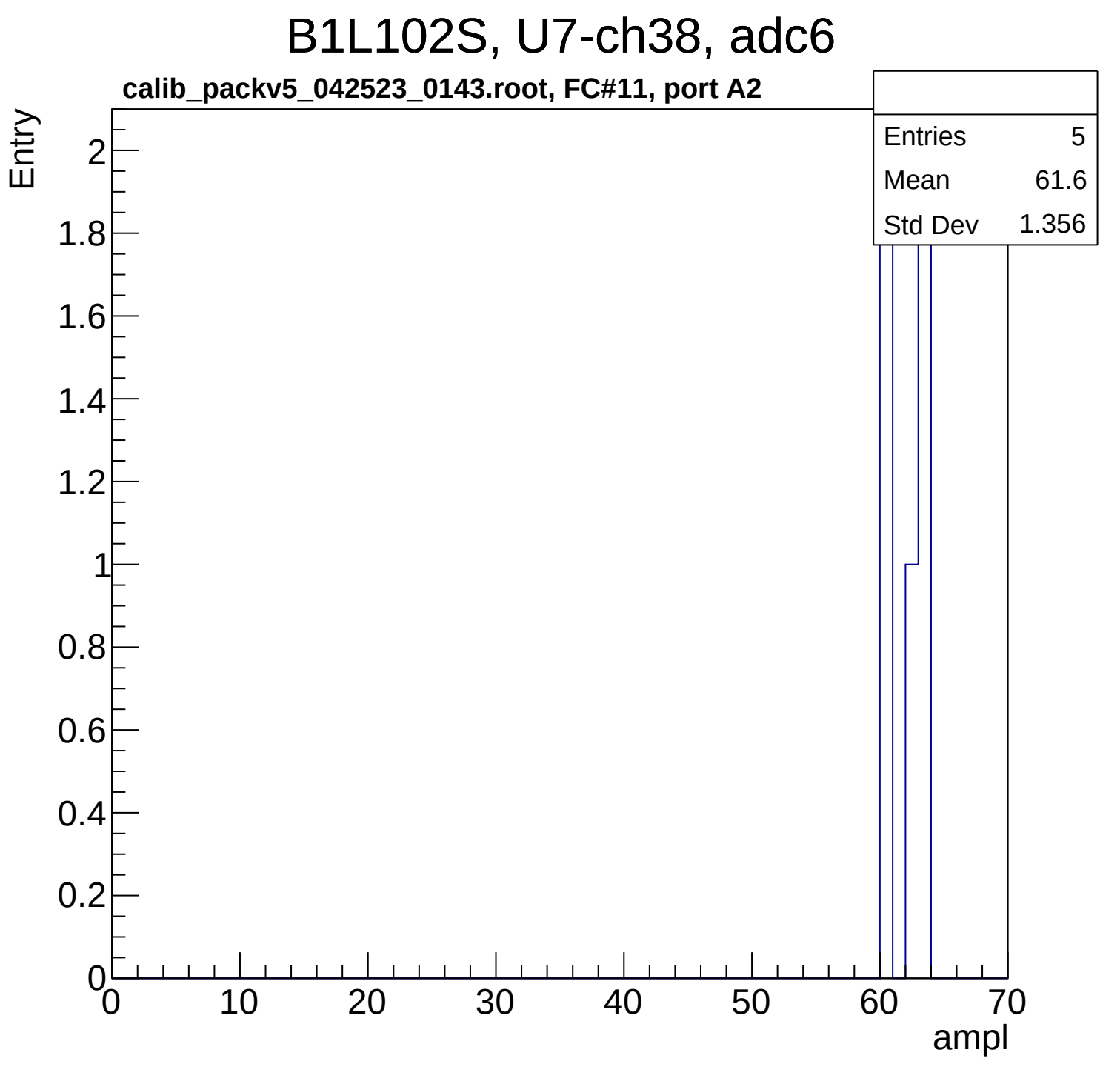
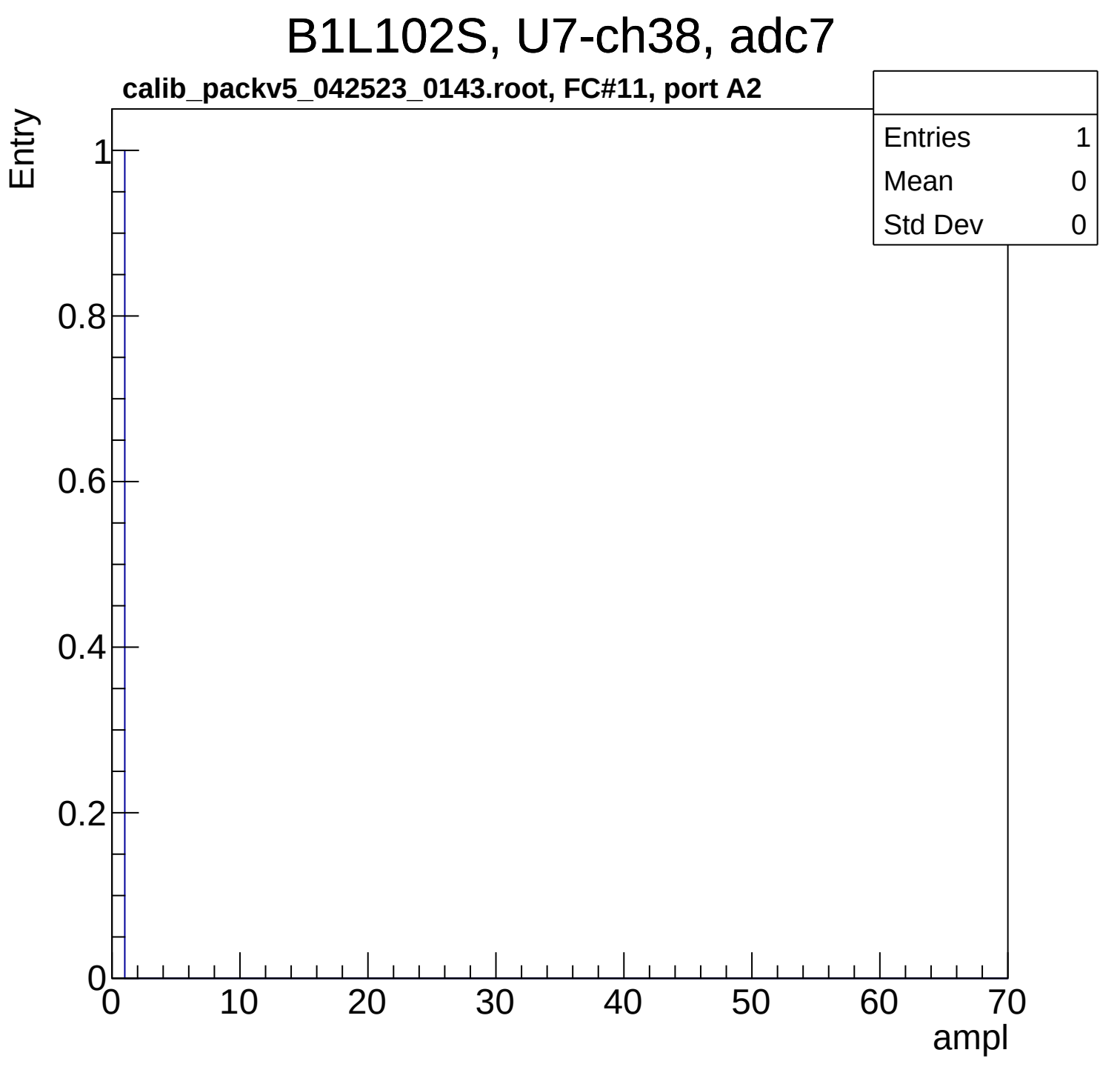
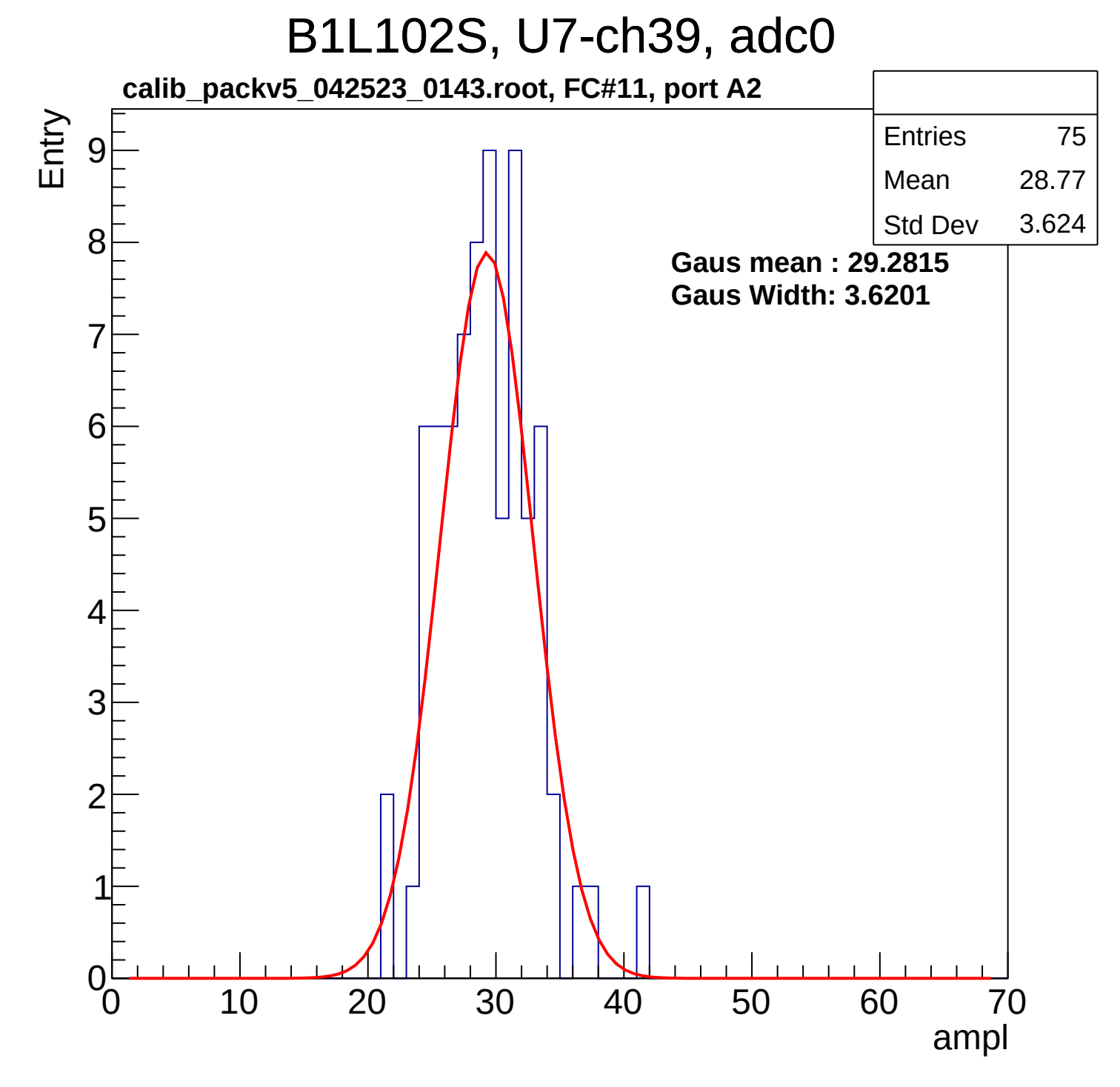
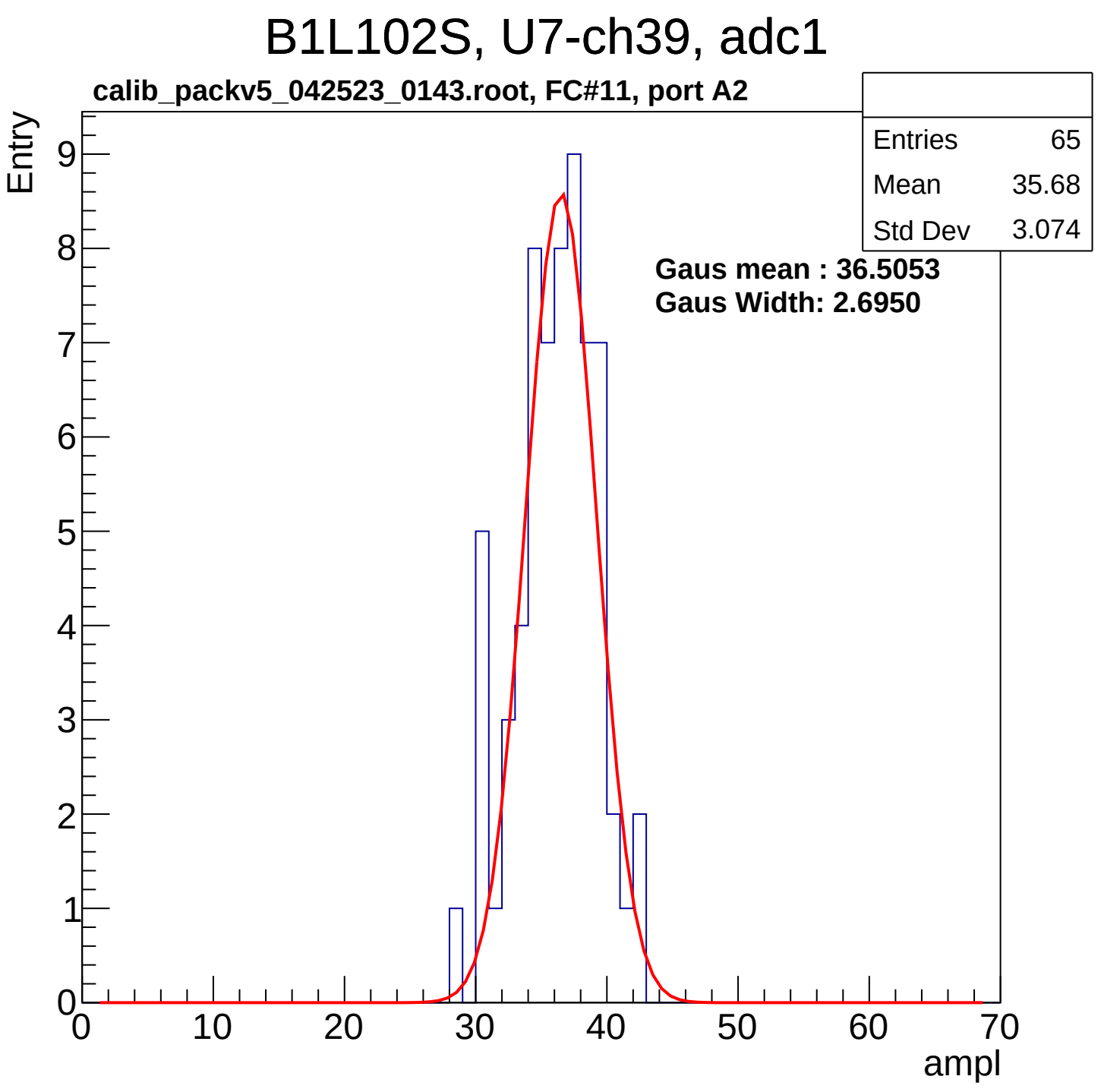
40
50
60
70

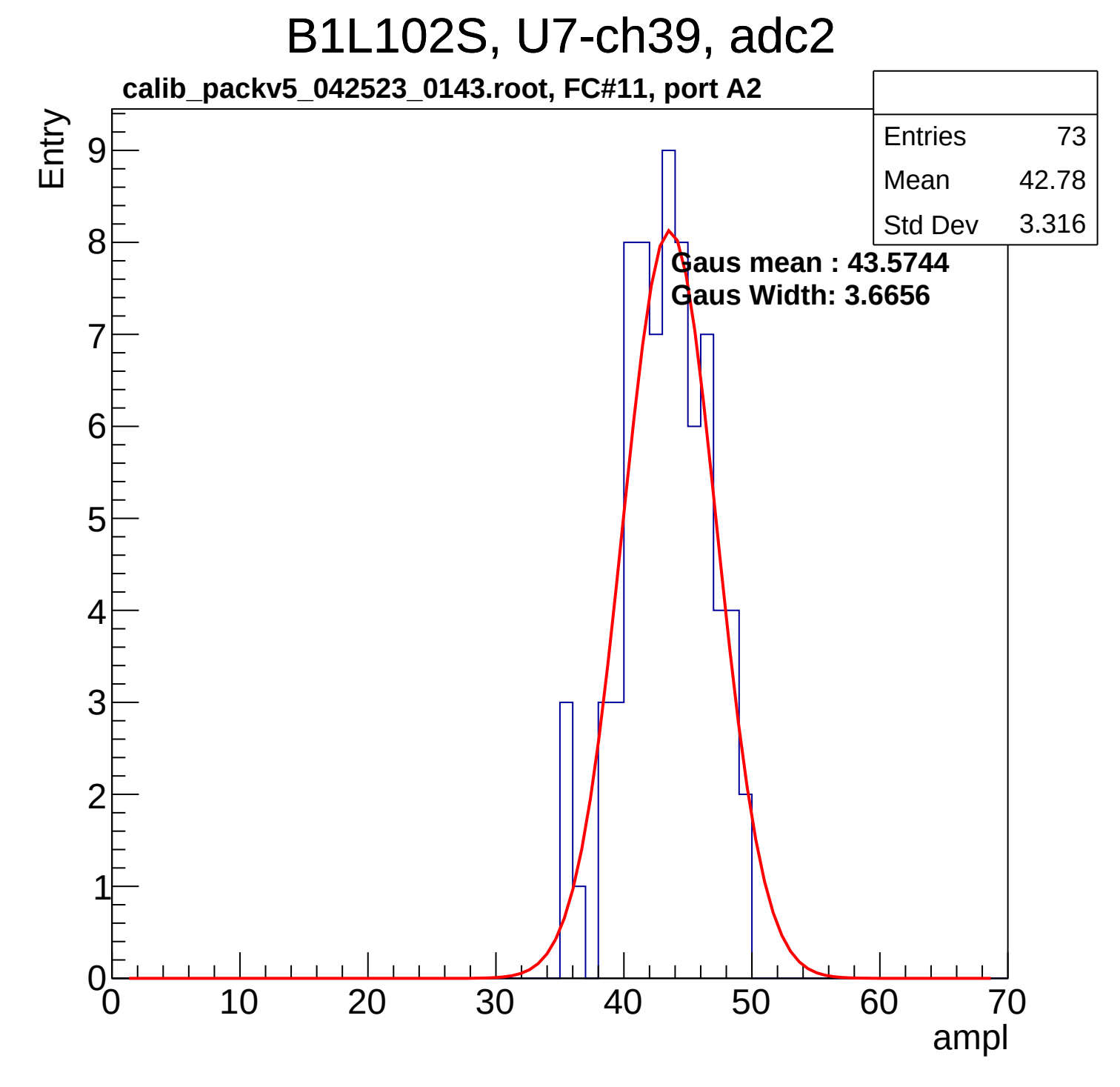

B1L102S, U7-ch38, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 39
Mean 58.95
Std Dev 9.816
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

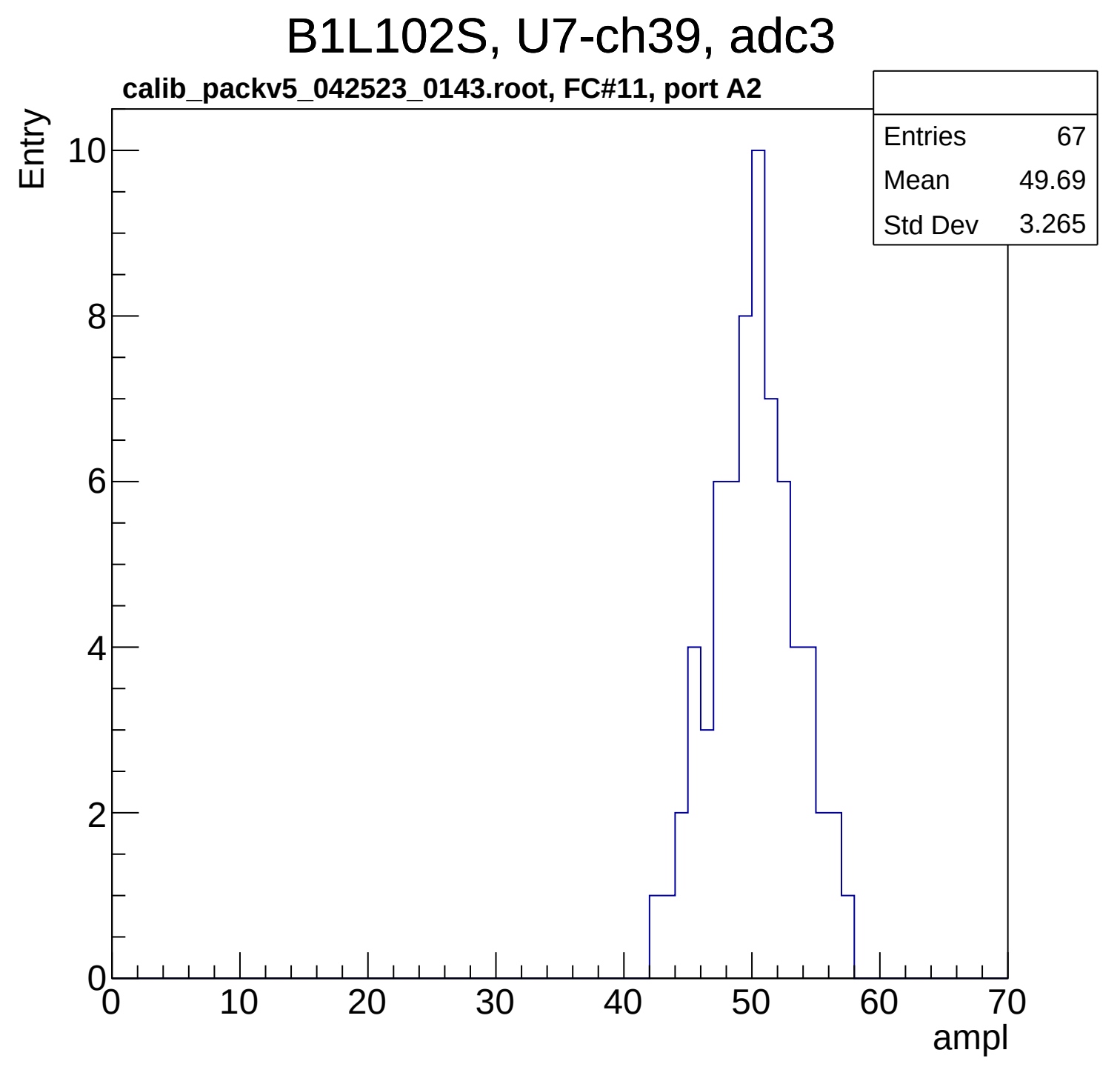

B1L102S, U7-ch38, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 5
Mean 61.6
Std Dev 1.356
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

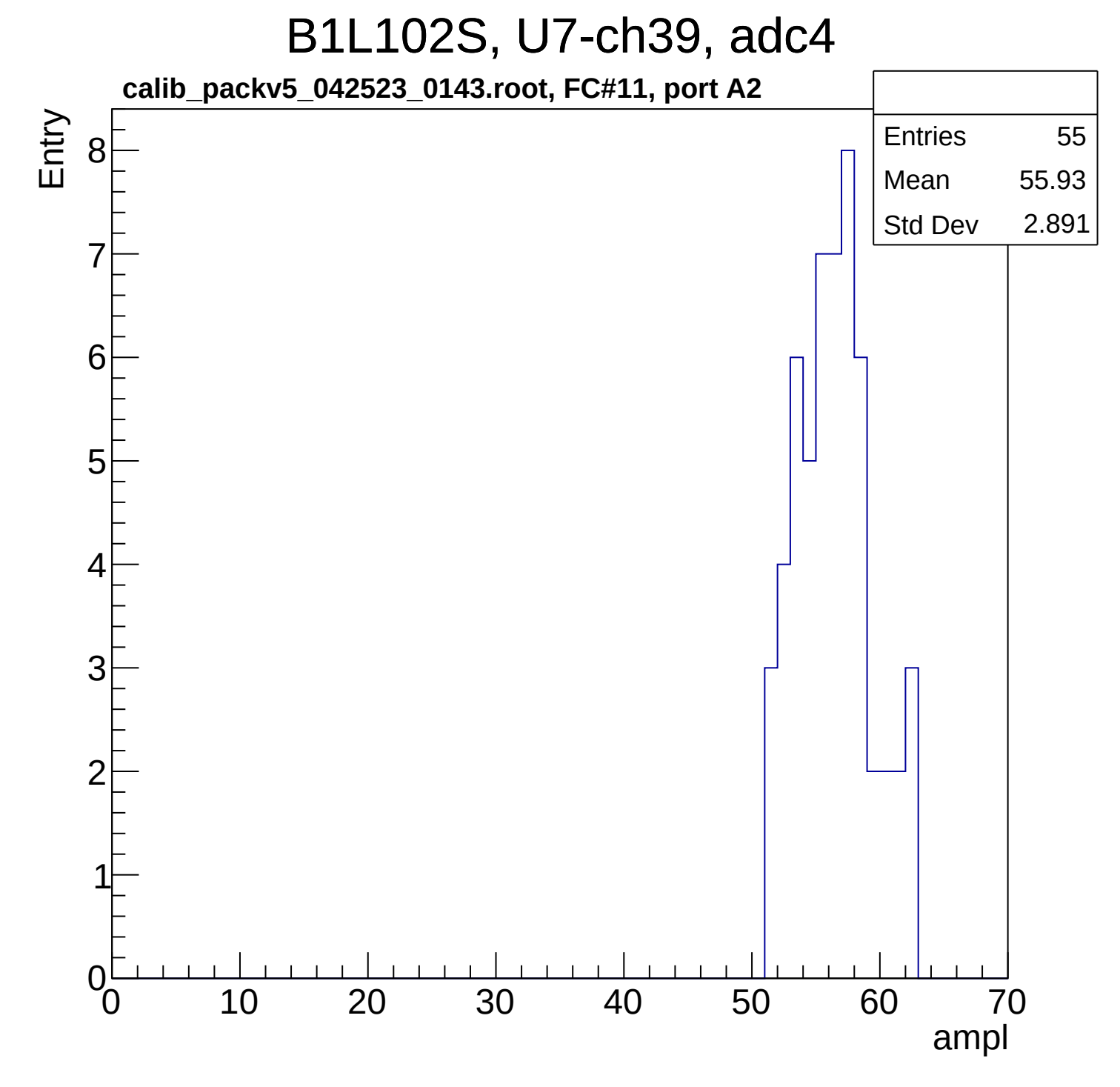

B1L102S, U7-ch38, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

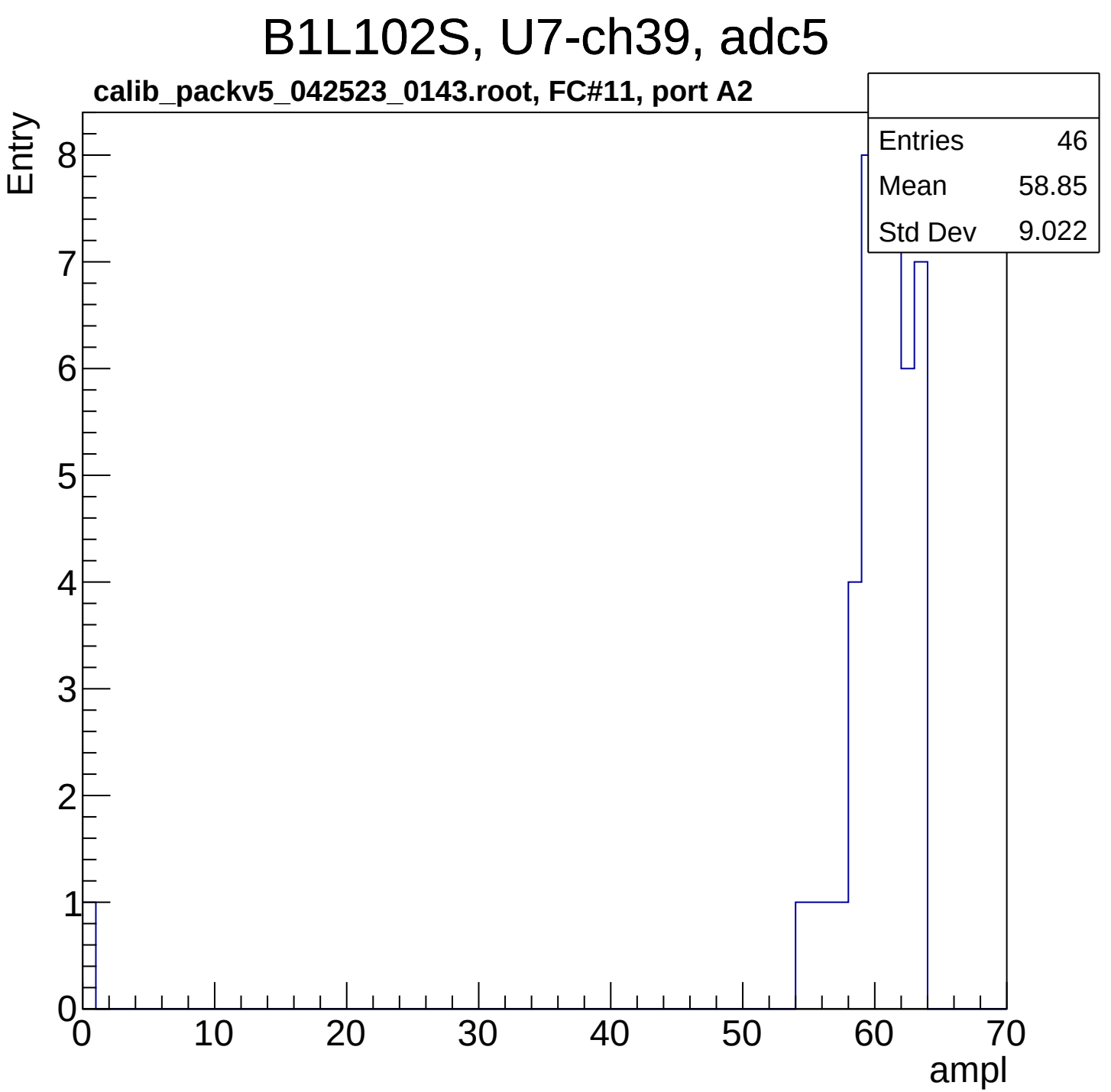

B1L102S, U7-ch39, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 75
Mean 28.77
Std Dev 3.624
Gaus mean : 29.2815
Gaus Width: 3.6201
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

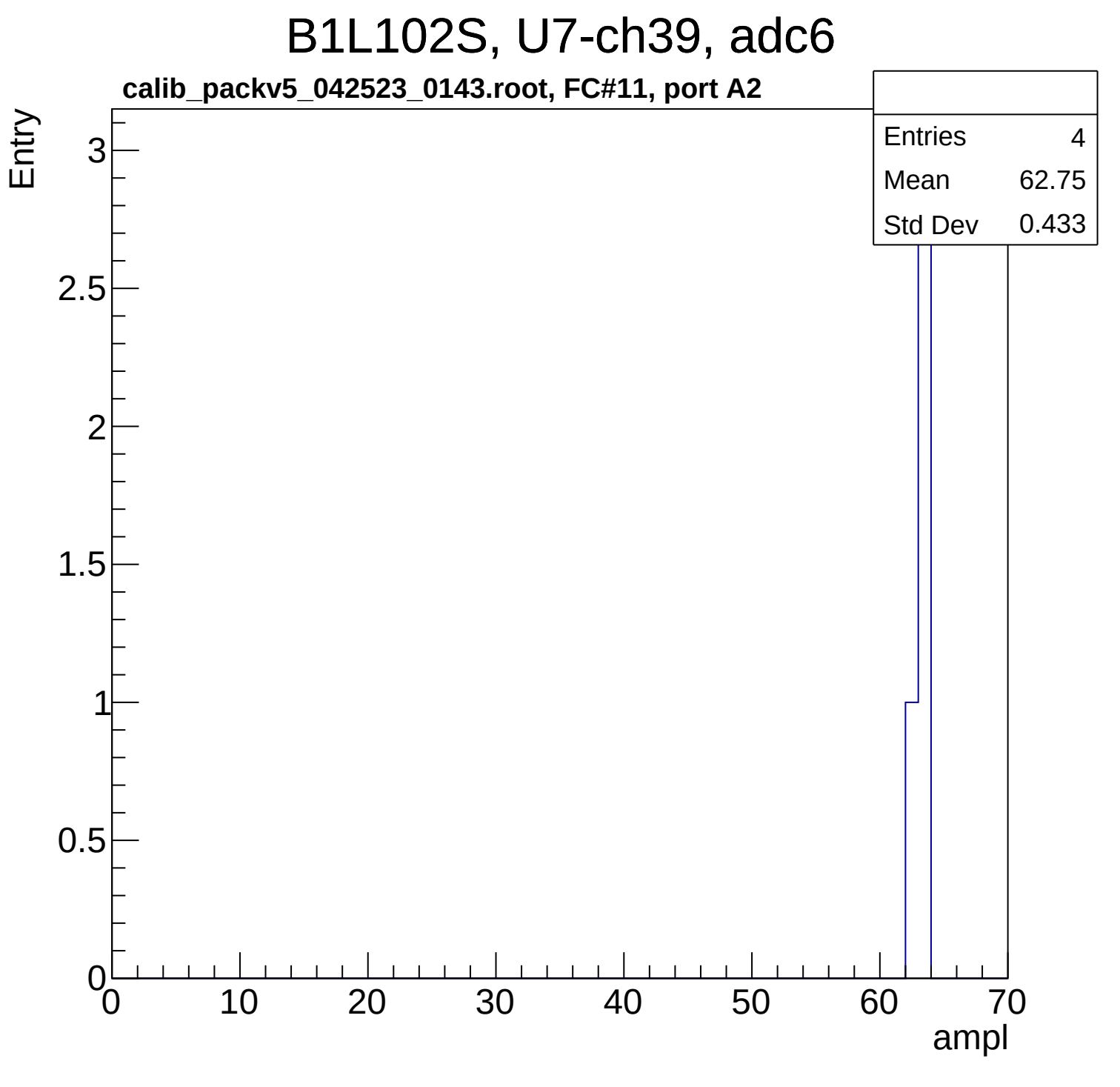

B1L102S, U7-ch39, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 65
Mean 35.68
Std Dev 3.074
Gaus mean : 36.5053
Gaus Width: 2.6950
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

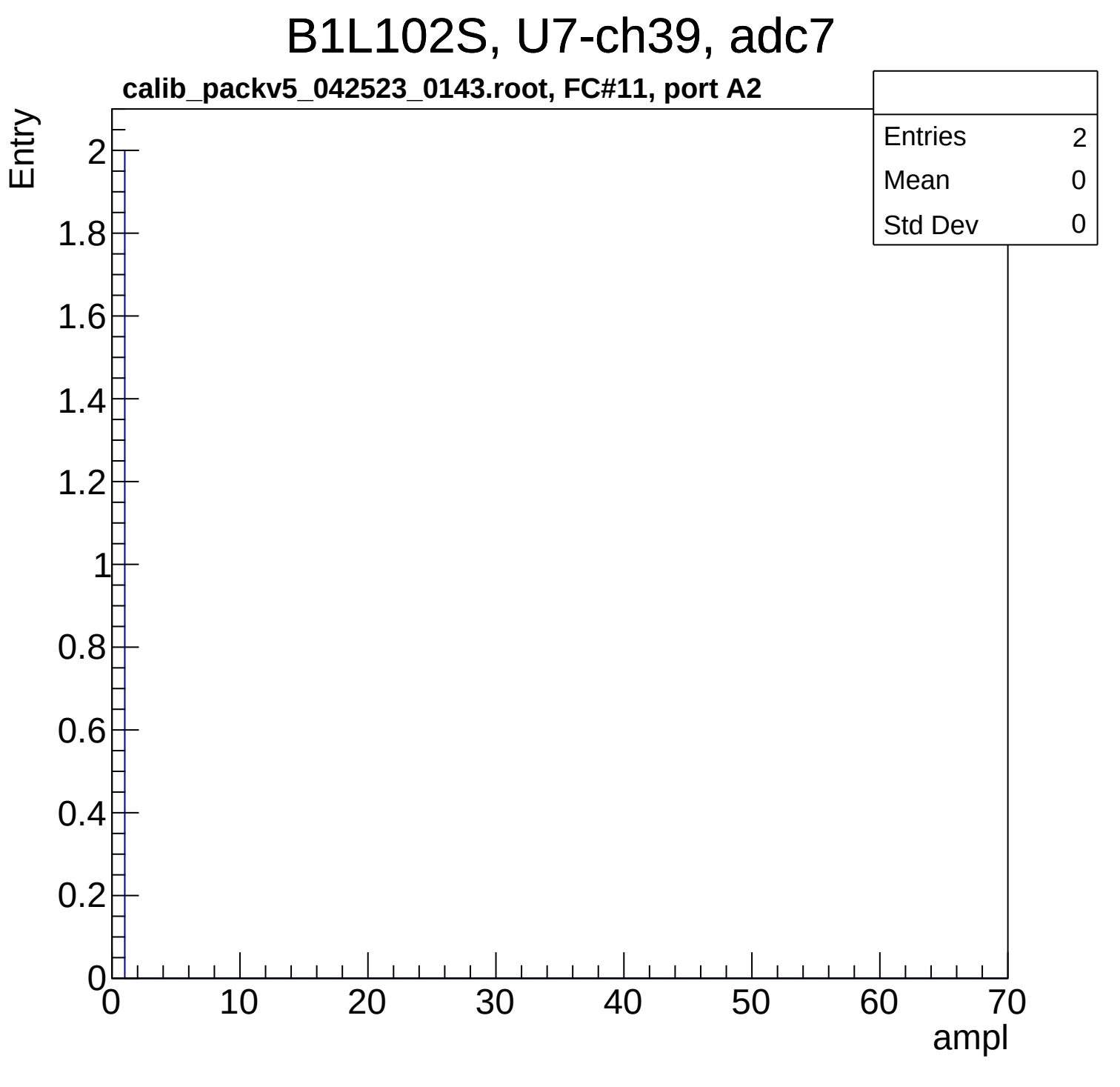

B1L102S, U7-ch39, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 73
Mean 42.78
Std Dev 3.316
Gaus mean : 43.5744
Gaus Width: 3.6656
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

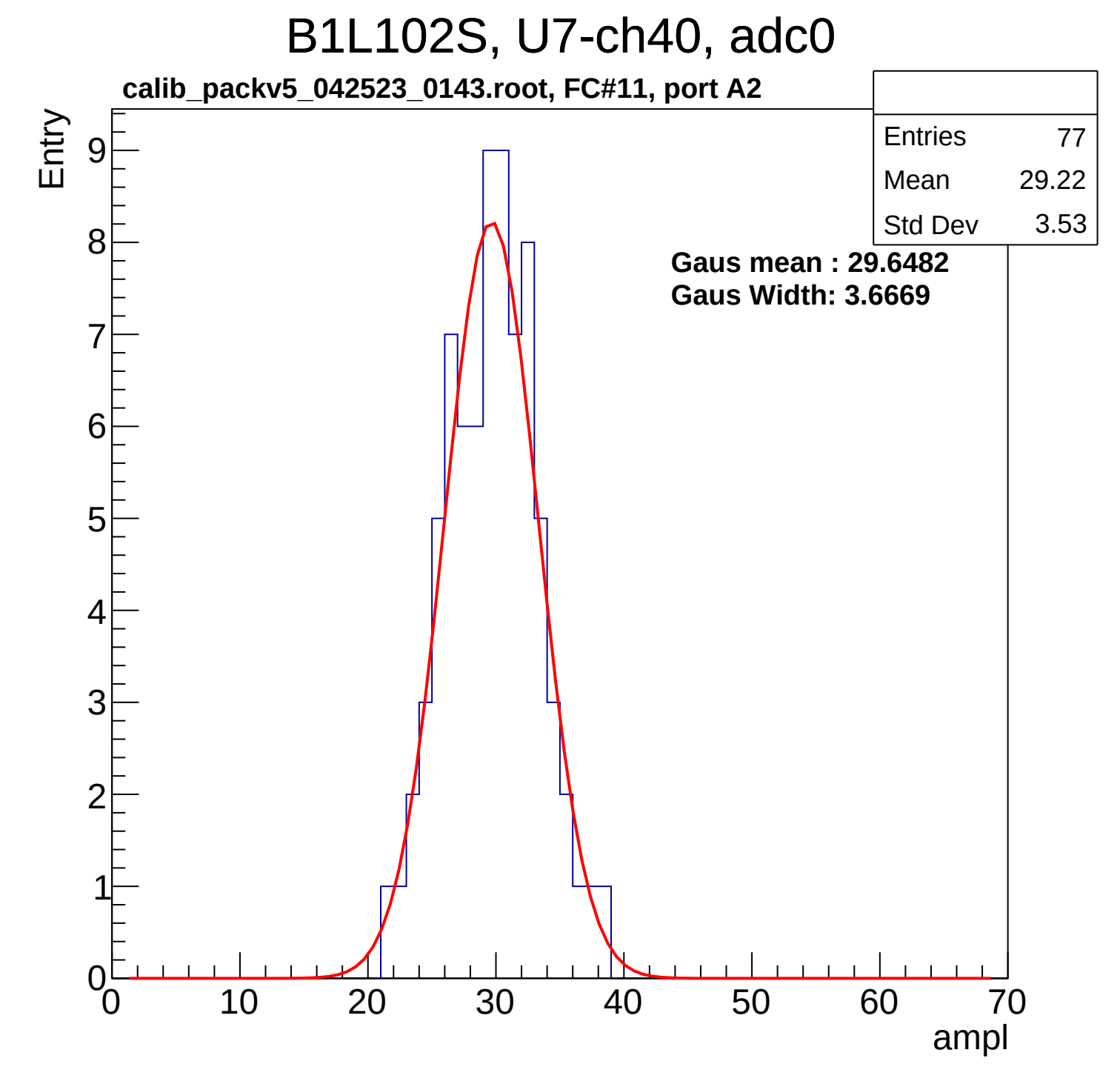

B1L102S, U7-ch39, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 67
Mean 49.69
Std Dev 3.265
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

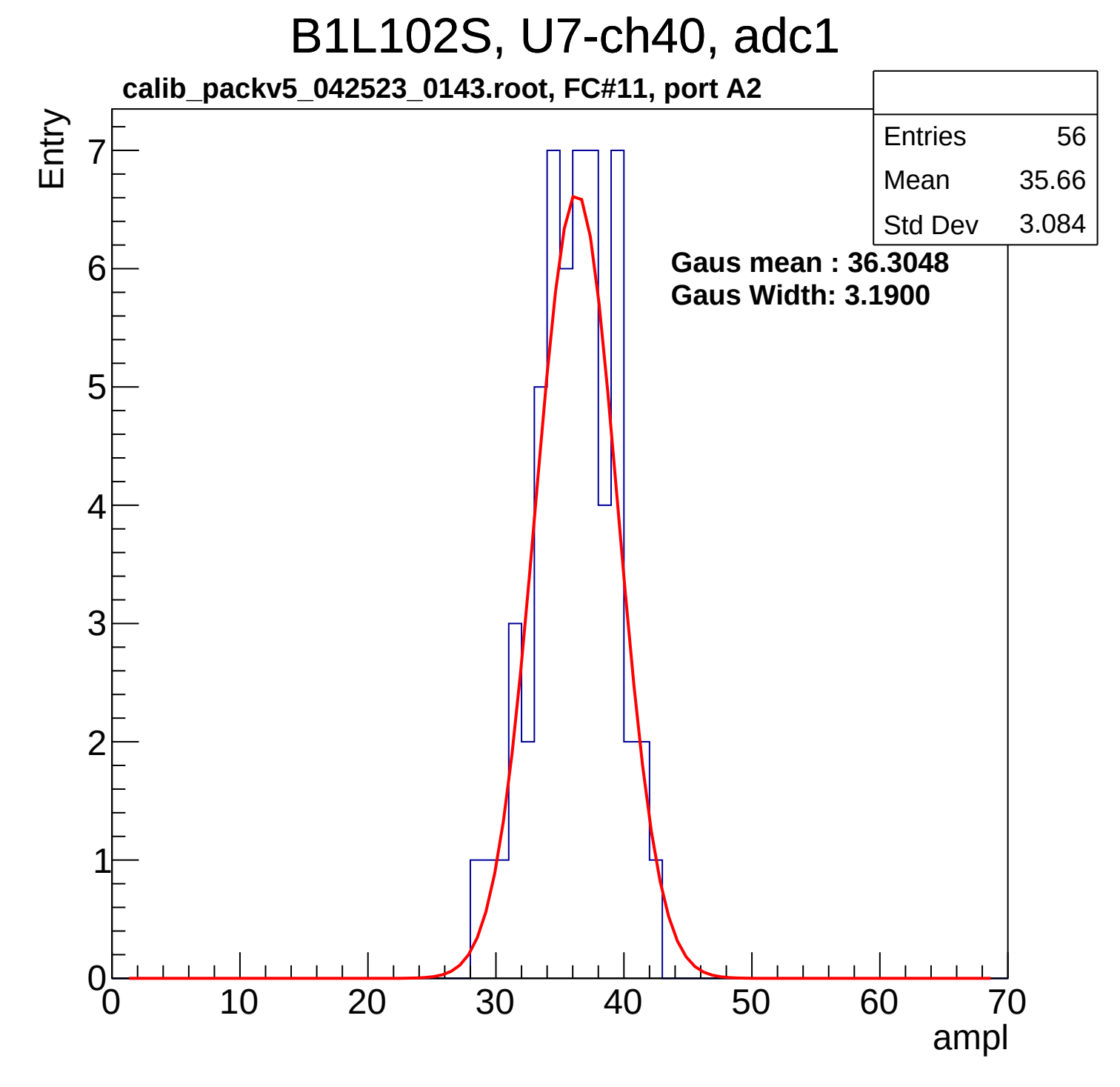

B1L102S, U7-ch39, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 55
Mean 55.93
Std Dev 2.891
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

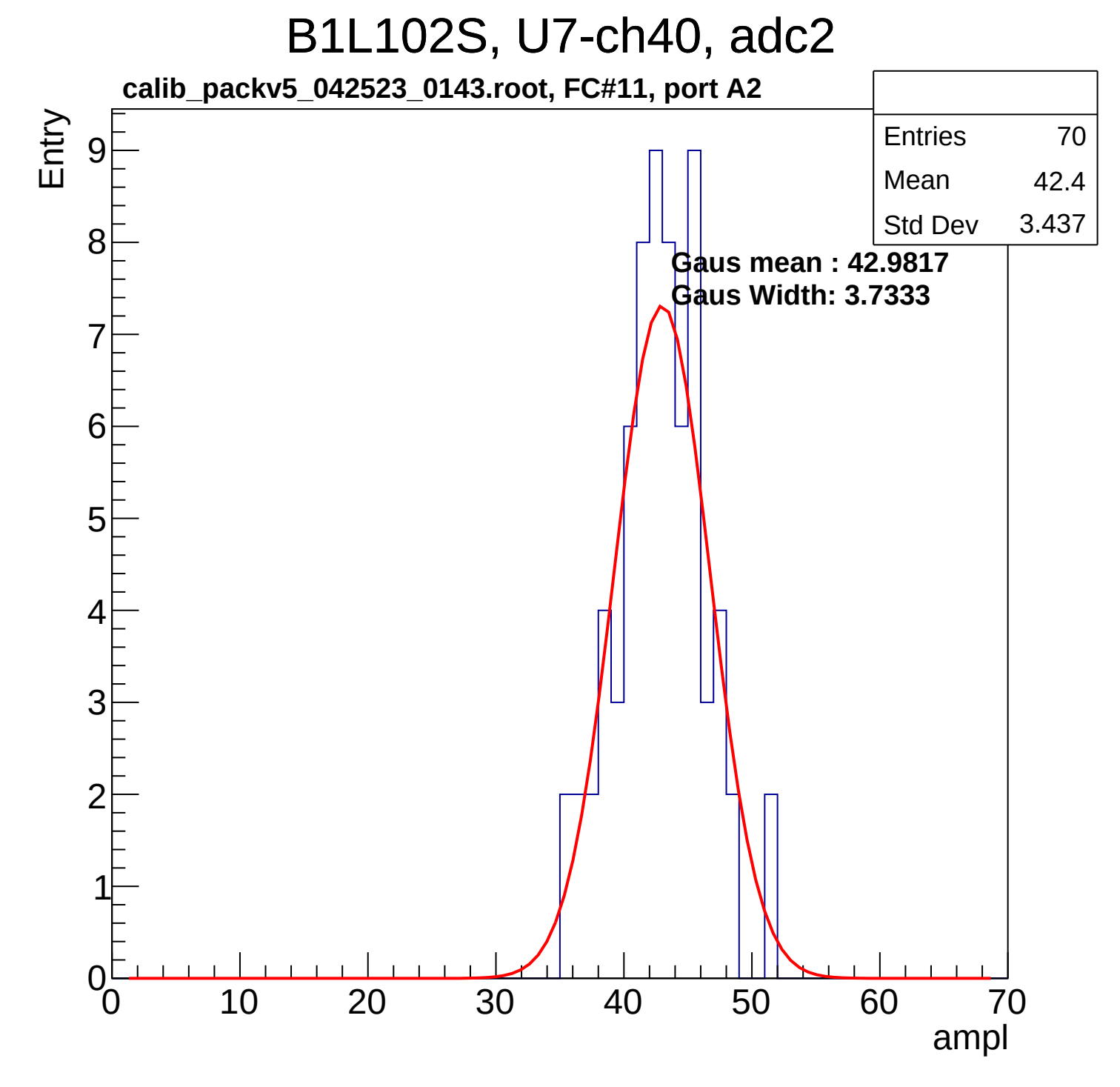

B1L102S, U7-ch39, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 46
Mean 58.85
Std Dev 9.022
Entry
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl

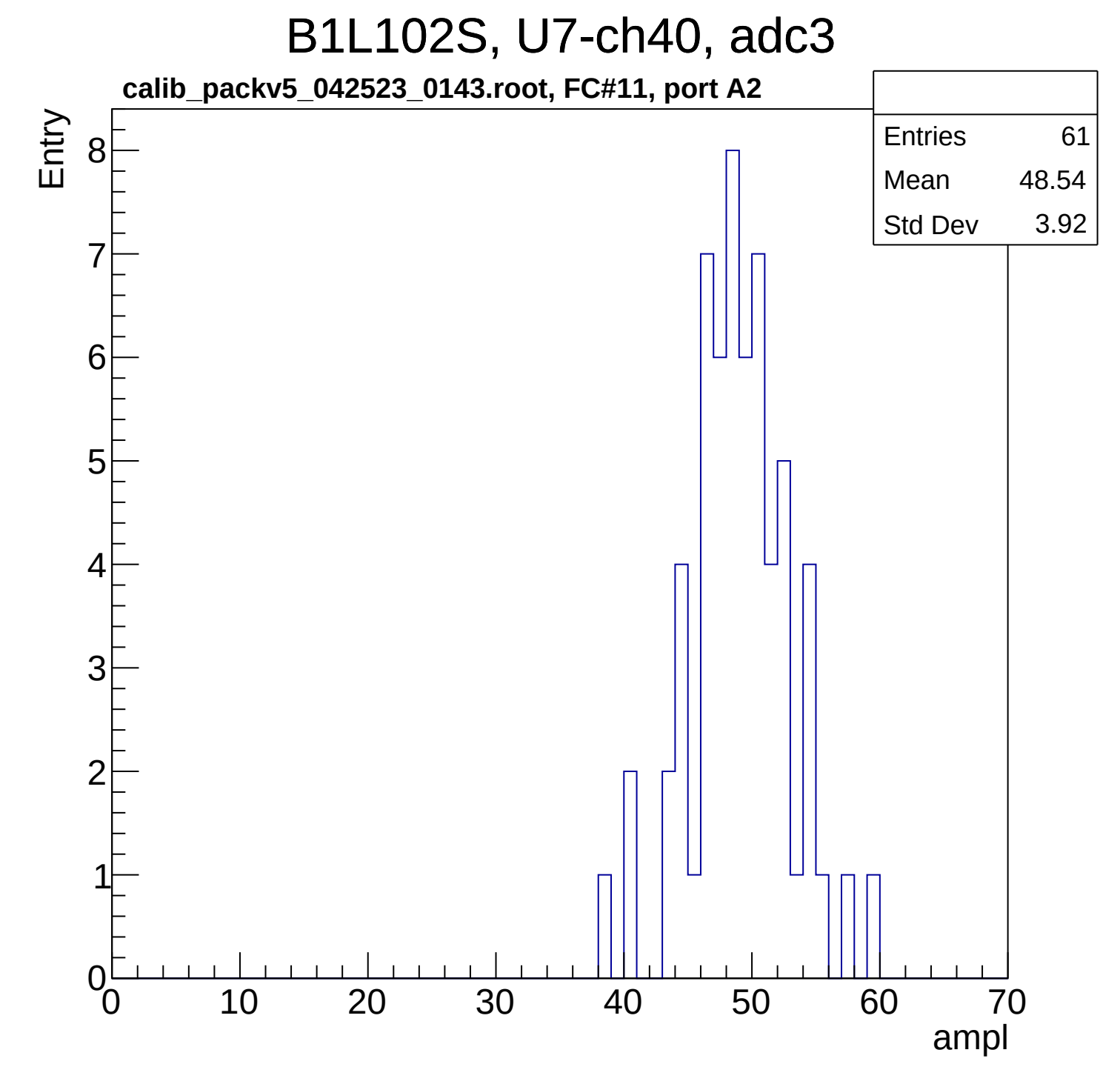

B1L102S, U7-ch39, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 4
Mean 62.75
Std Dev 0.433
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L102S, U7-ch39, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 2
Mean 0
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L102S, U7-ch40, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 77
Mean 29.22
Std Dev 3.53
Gaus mean : 29.6482
Gaus Width: 3.6669
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L102S, U7-ch40, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 56
Mean 35.66
Std Dev 3.084
Gaus mean : 36.3048
Gaus Width: 3.1900
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L102S, U7-ch40, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 70
Mean 42.4
Std Dev 3.437
Gaus mean : 42.9817
Gaus Width: 3.7333
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L102S, U7-ch40, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 61
Mean 48.54
Std Dev 3.92
Entry
ampl
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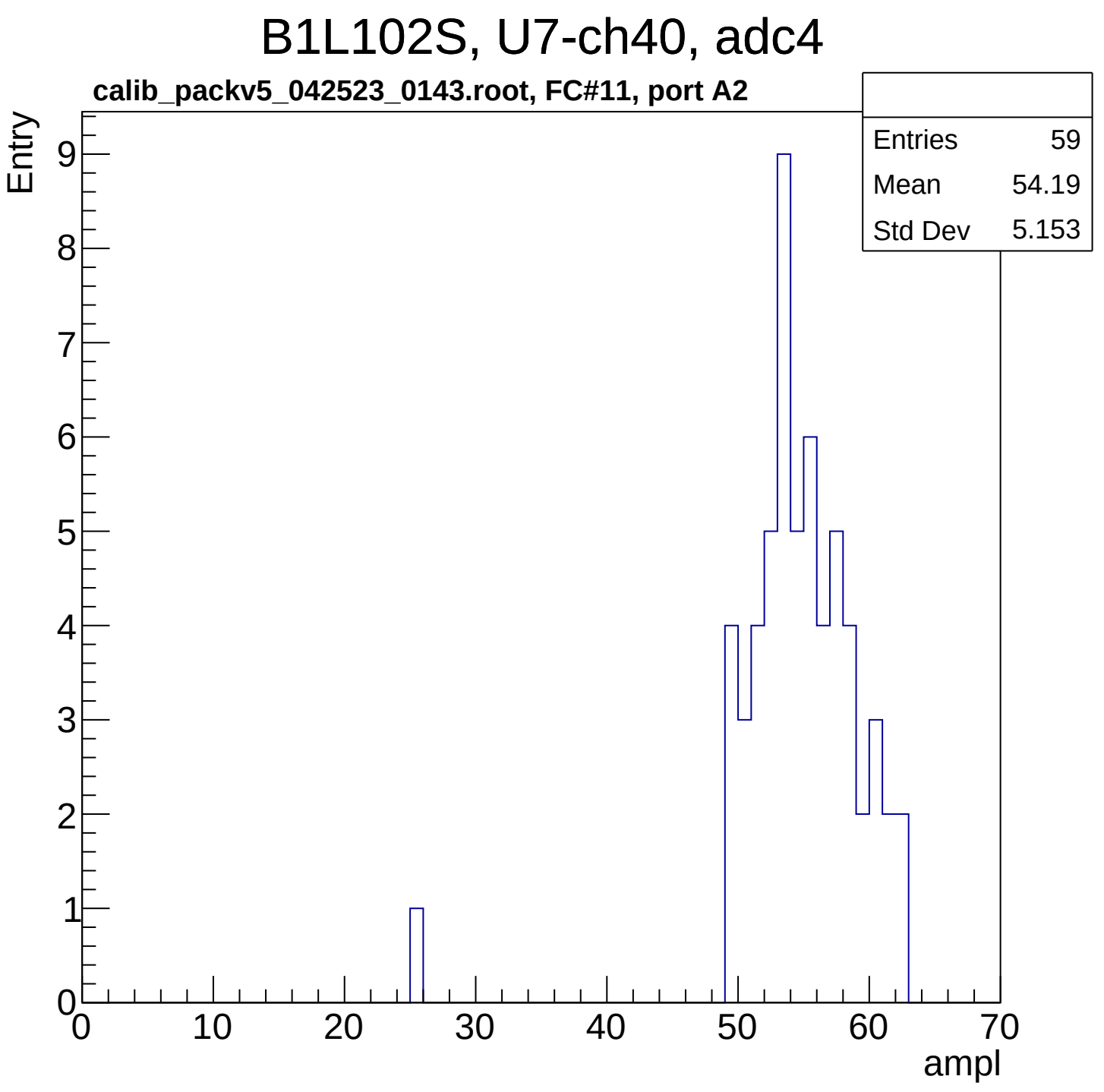
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L102S, U7-ch40, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 59
Mean 54.19
Std Dev 5.153
Entry
ampl
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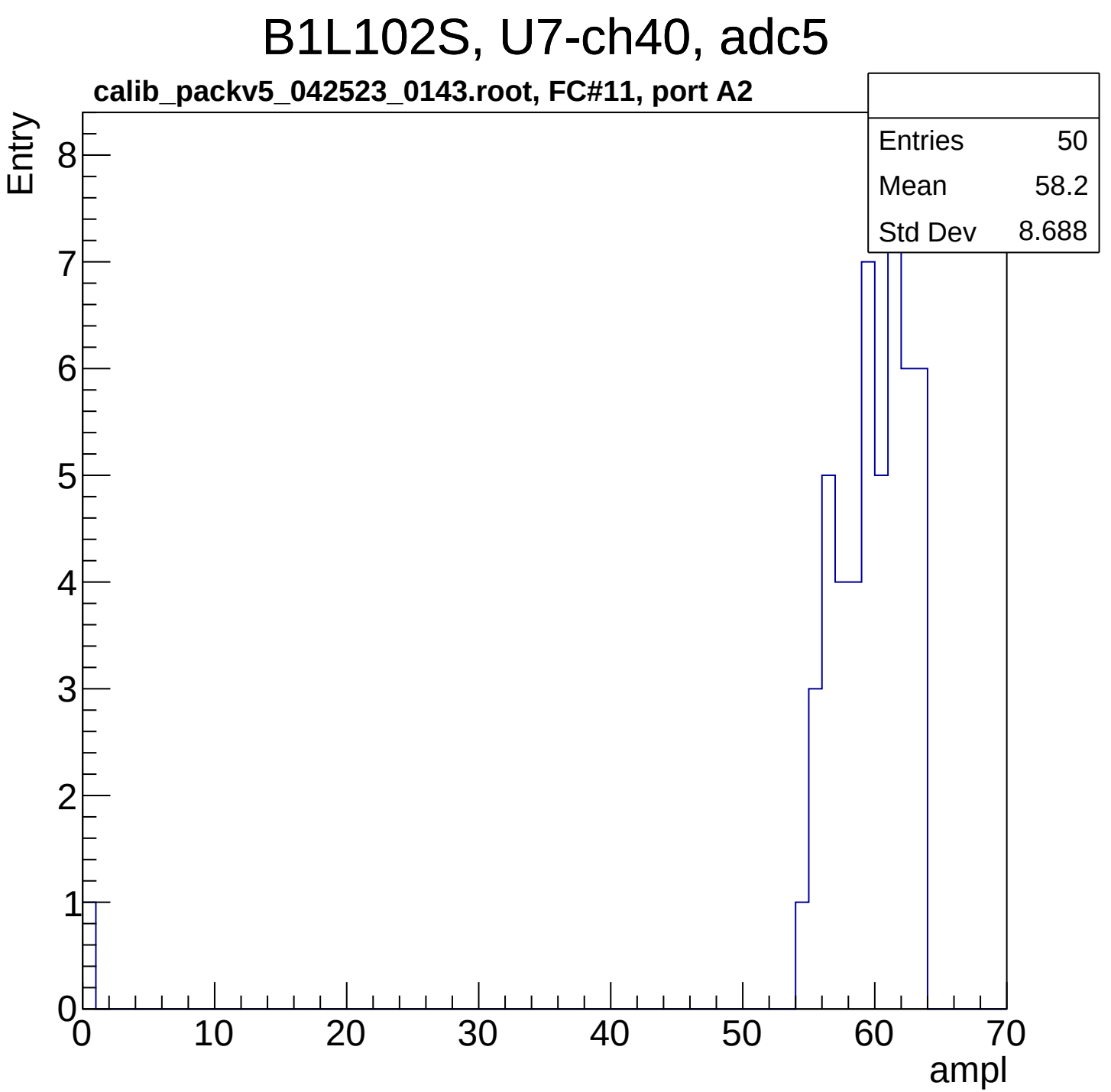
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L102S, U7-ch40, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 50
Mean 58.2
Std Dev 8.688
Entry
0
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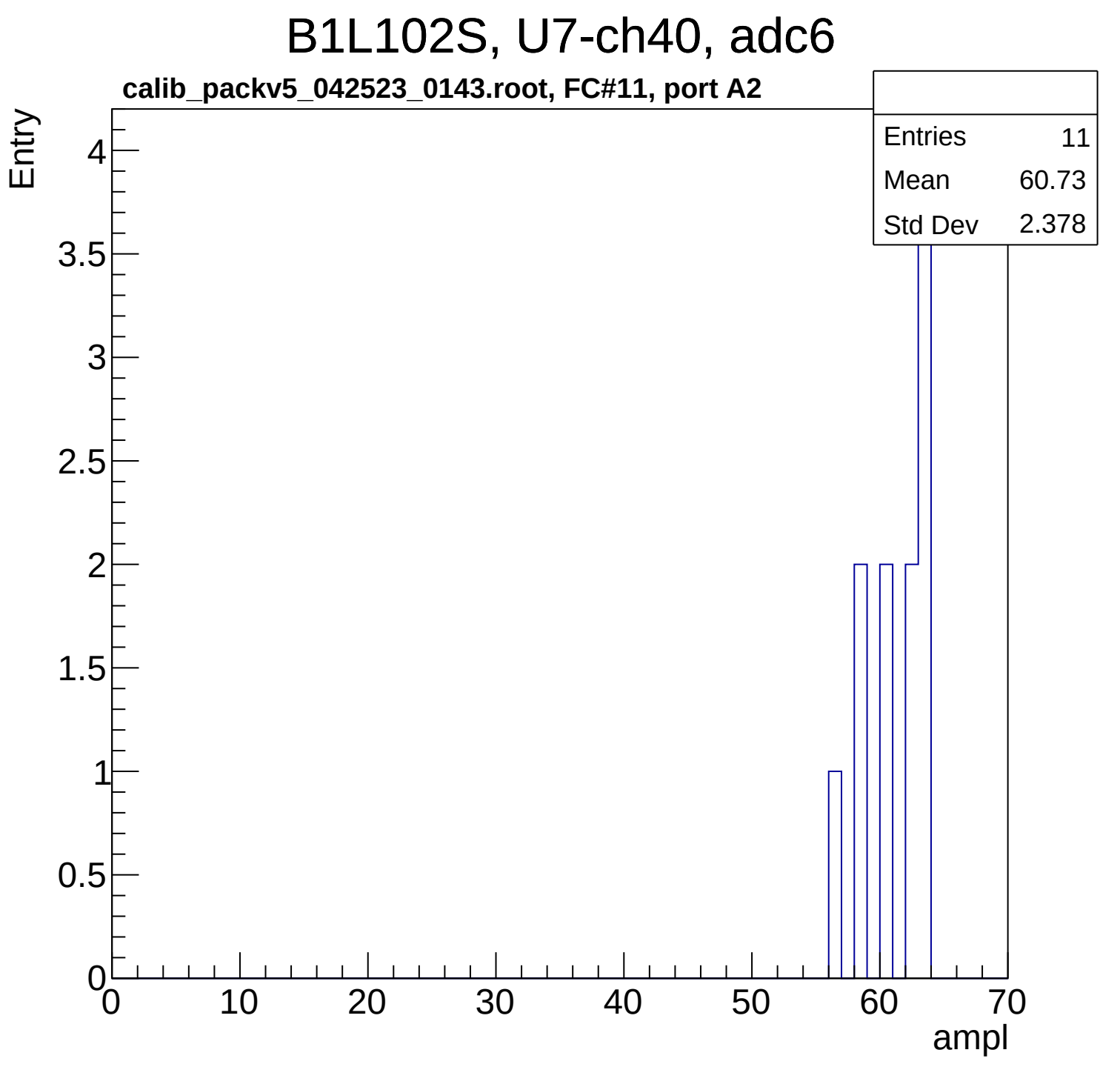
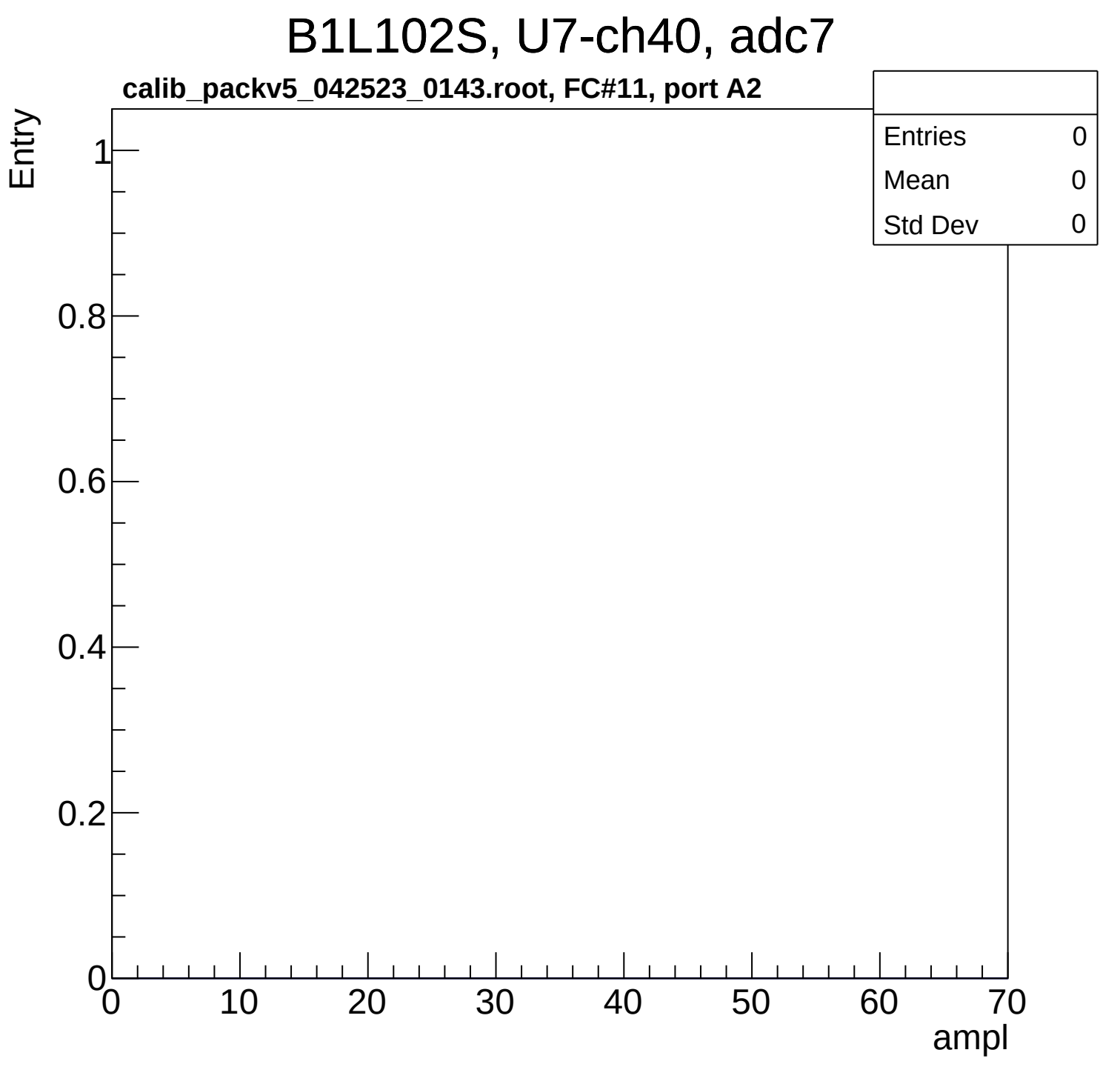
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L102S, U7-ch40, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 11
Mean 60.73
Std Dev 2.378
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L102S, U7-ch40, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 0
Mean 0
Std Dev 0
Entry
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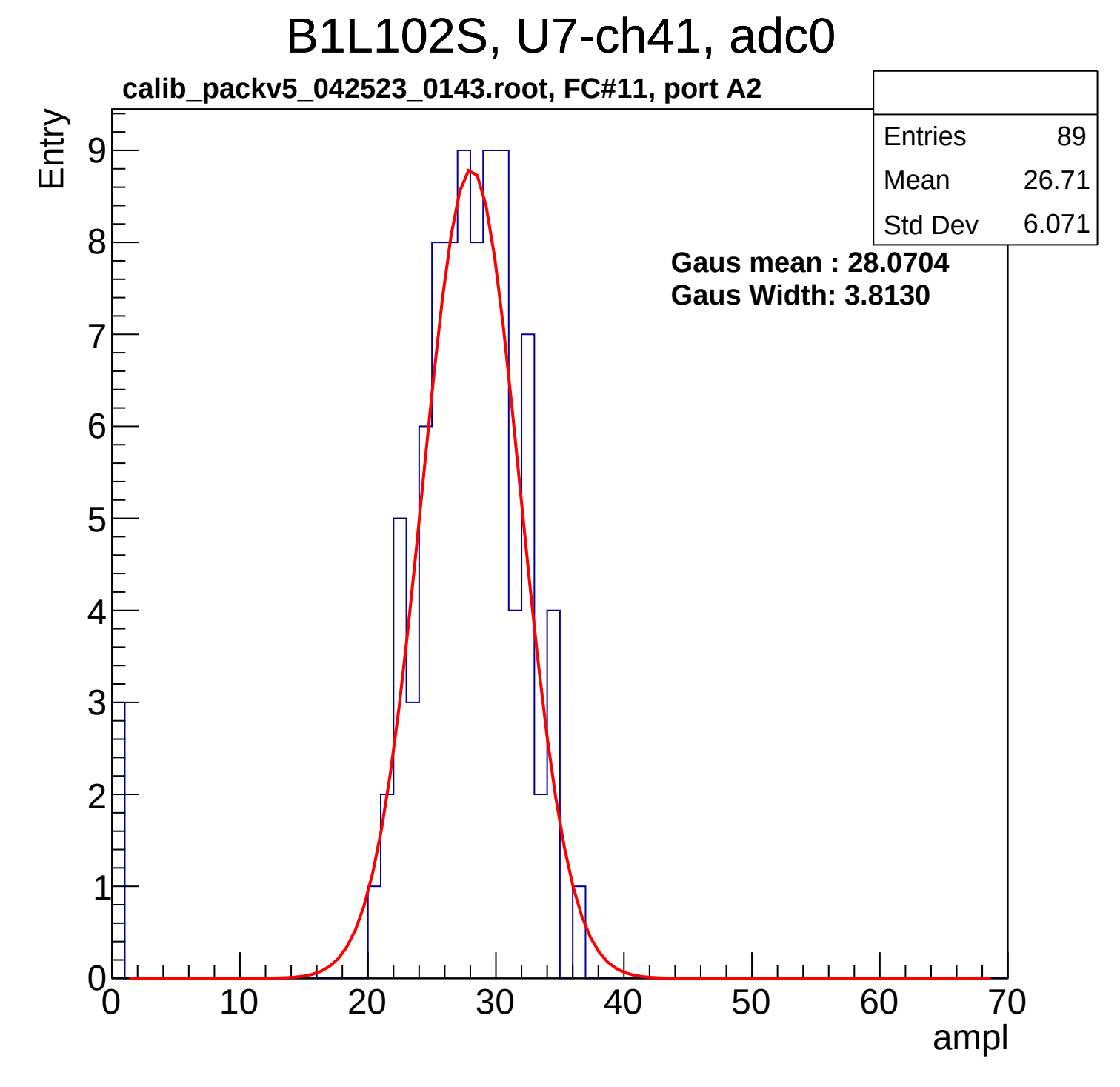
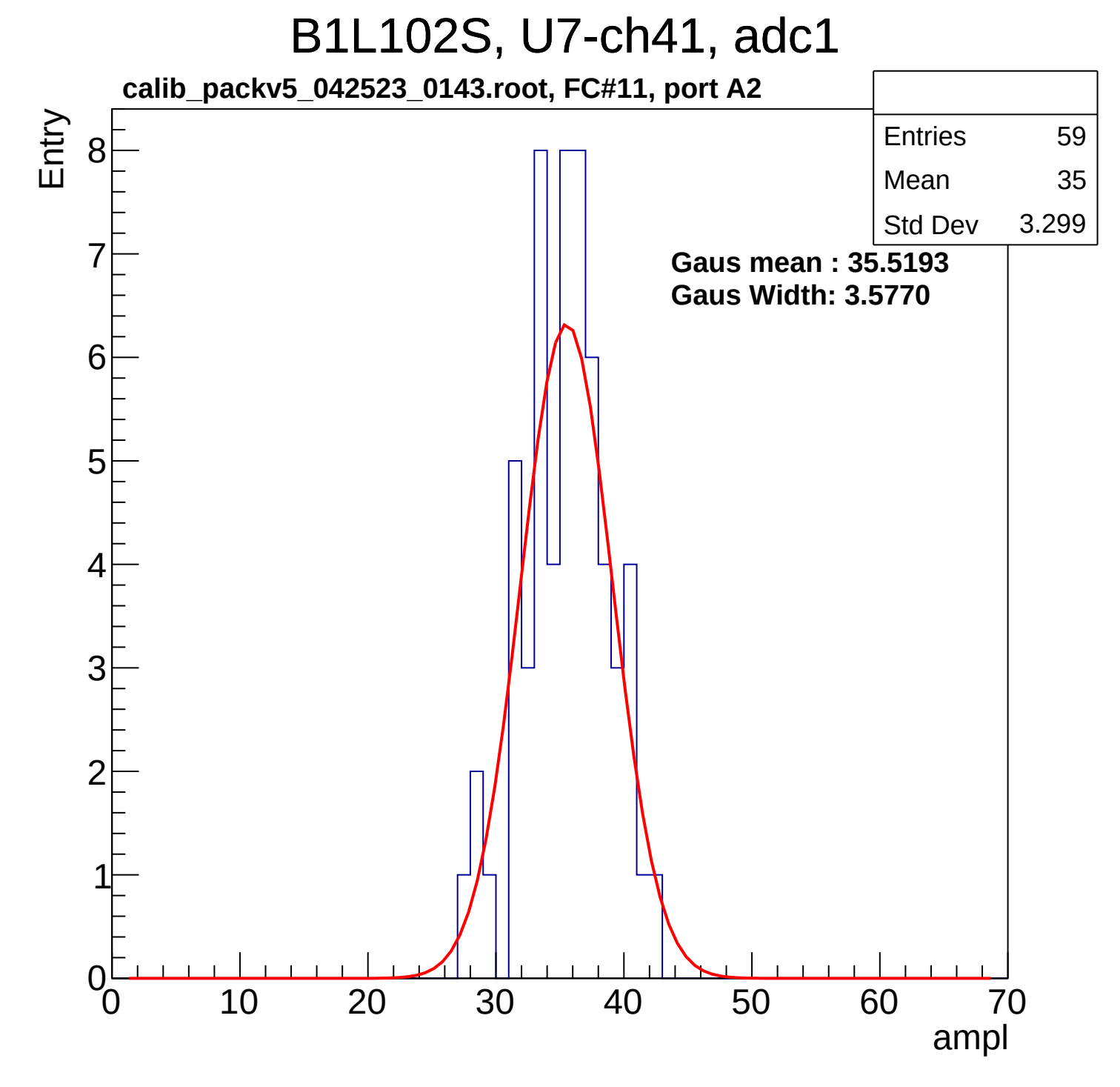
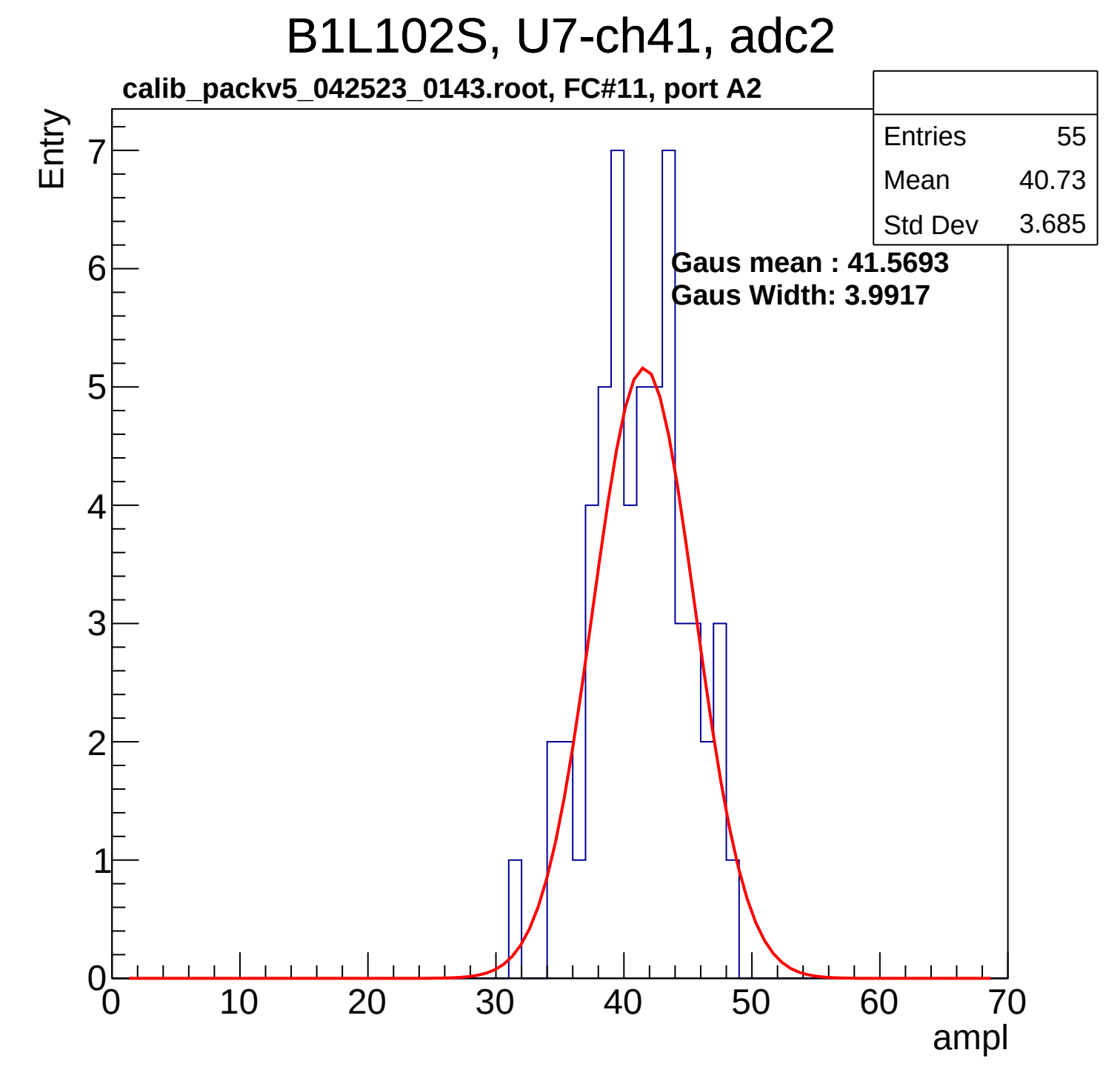
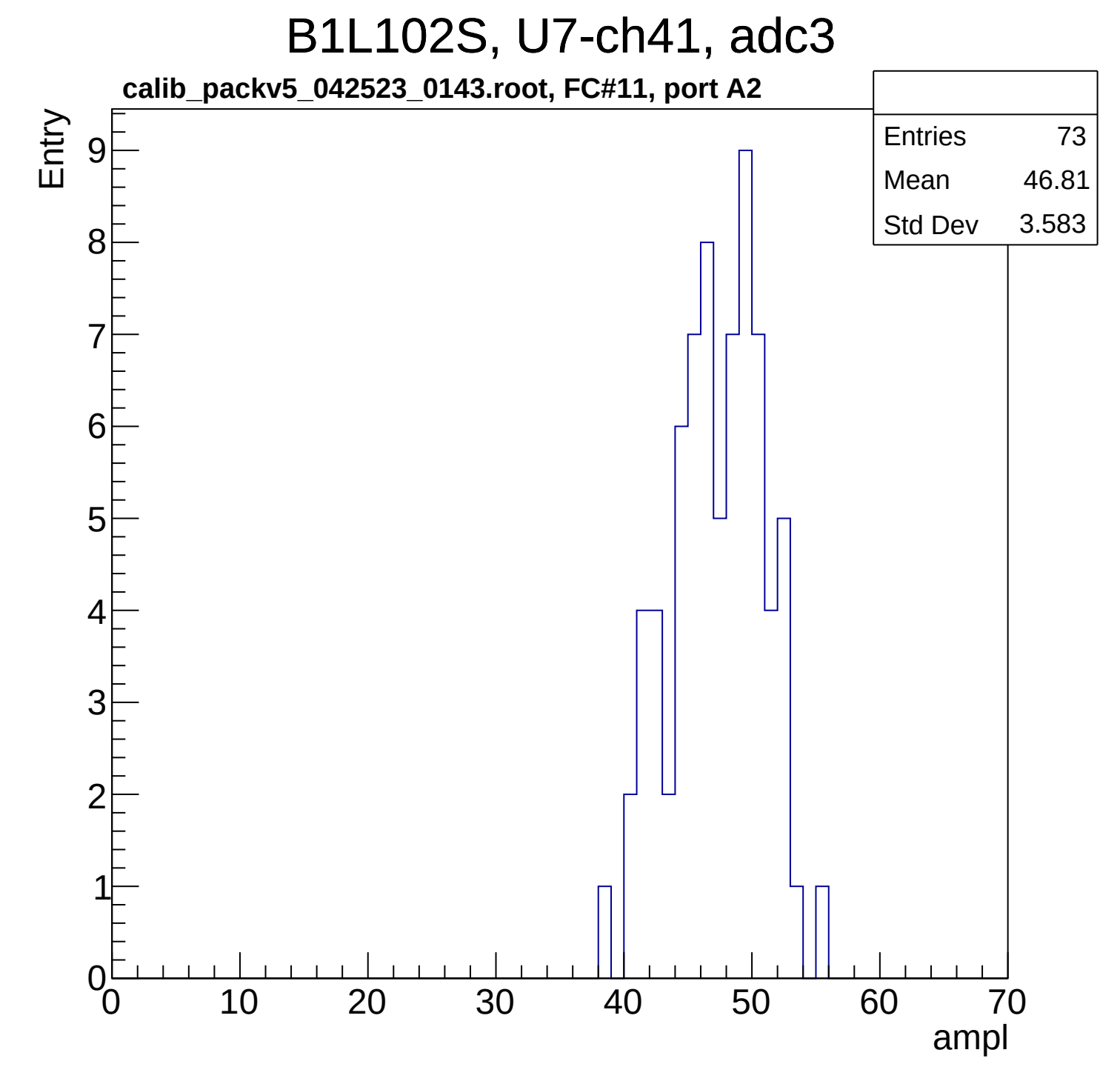
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U7-ch41, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 89
Mean 26.71
Std Dev 6.071
Gaus mean : 28.0704
Gaus Width: 3.8130
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L102S, U7-ch41, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 59
Mean 35
Std Dev 3.299
Gaus mean : 35.5193
Gaus Width: 3.5770
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L102S, U7-ch41, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 55
Mean 40.73
Std Dev 3.685
Gaus mean : 41.5693
Gaus Width: 3.9917
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L102S, U7-ch41, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 73
Mean 46.81
Std Dev 3.583
Entry
ampl
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3
4
5
6
7
8
9
0
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20
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40
50
60
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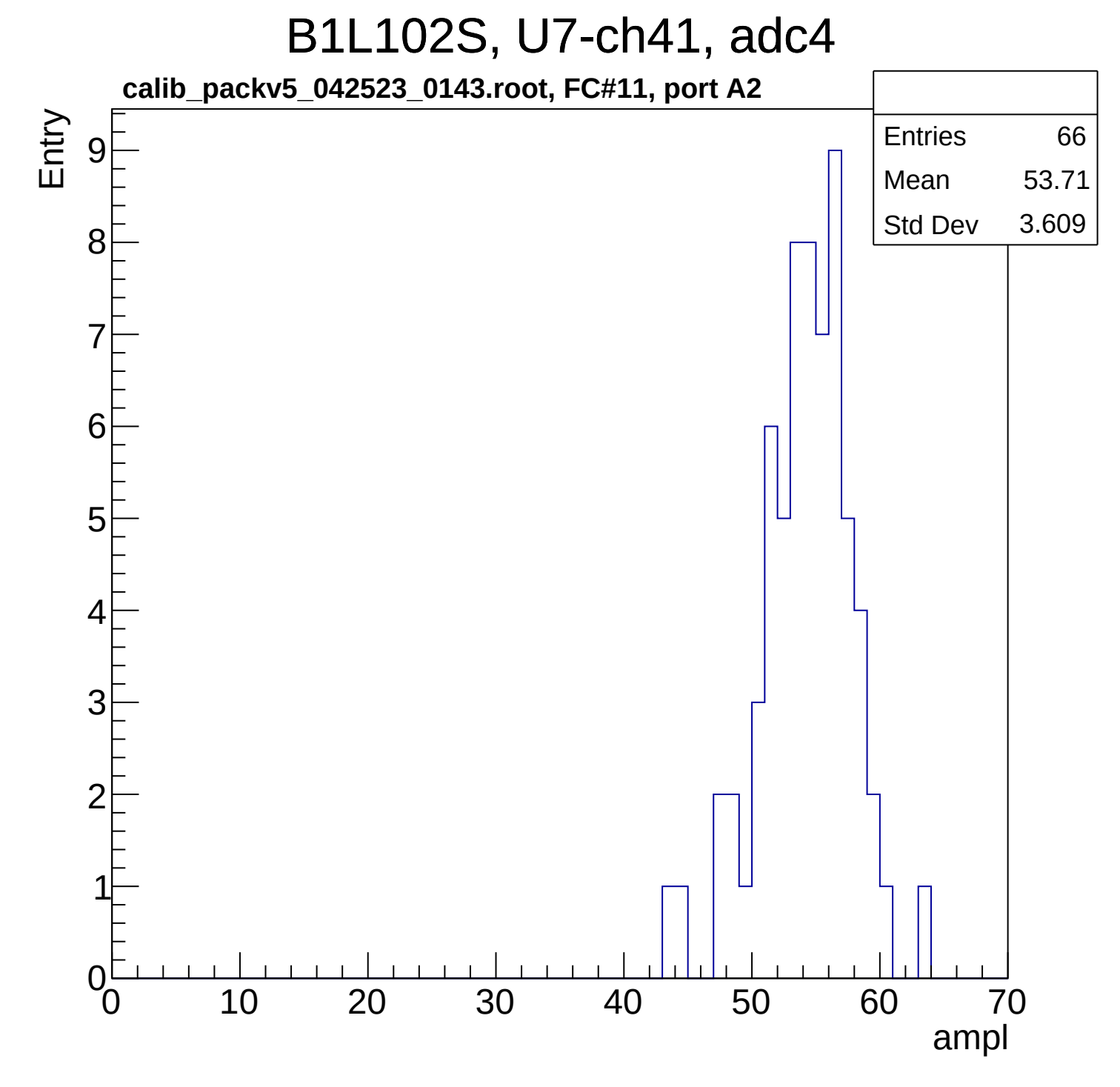
B1L102S, U7-ch41, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 66
Mean 53.71
Std Dev 3.609
Entry
ampl
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2
3
4
5
6
7
8
9
0
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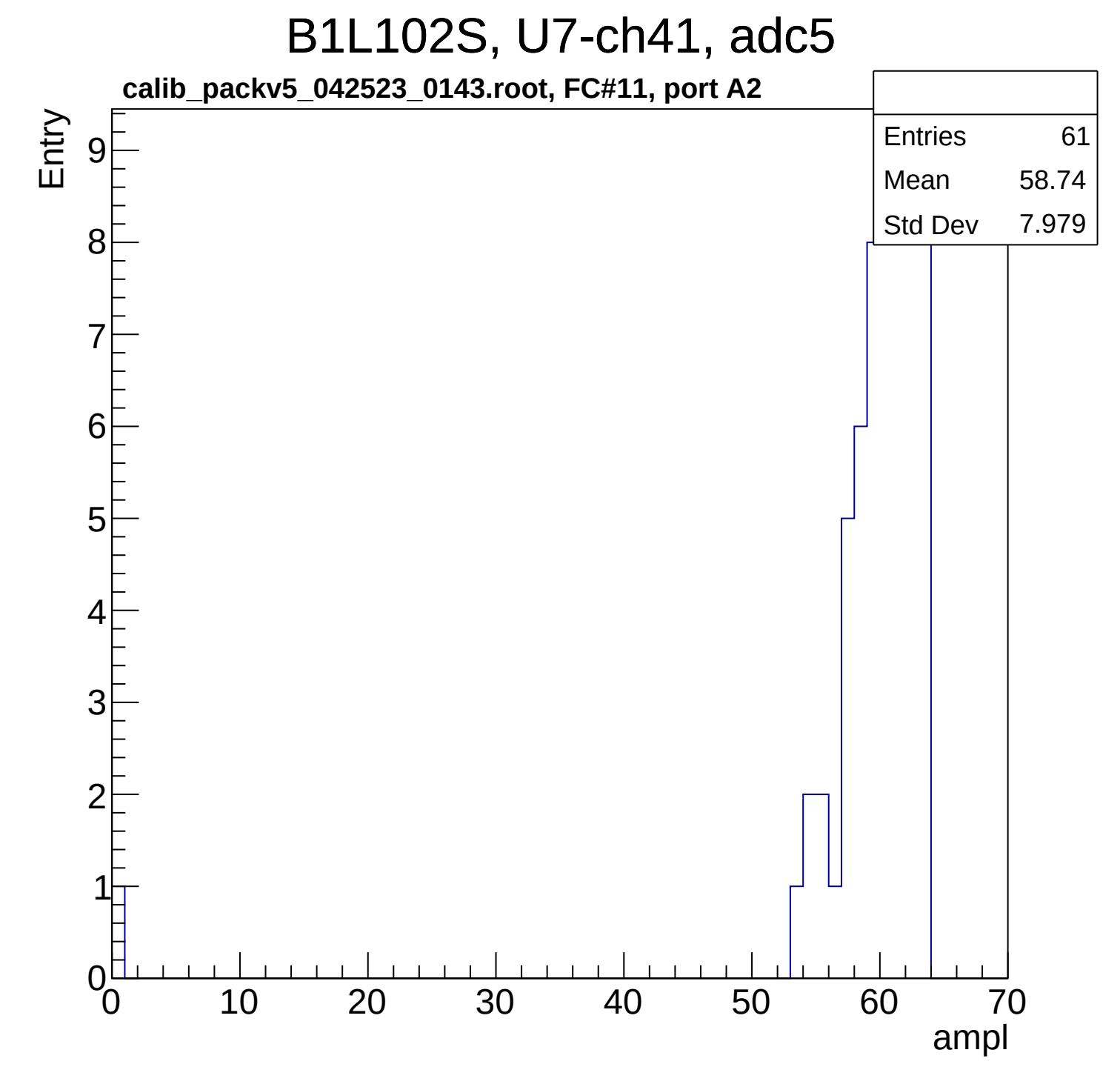
20
30
40
50
60
70


B1L102S, U7-ch41, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 61
Mean 58.74
Std Dev 7.979
Entry
ampl
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2
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6
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8
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0
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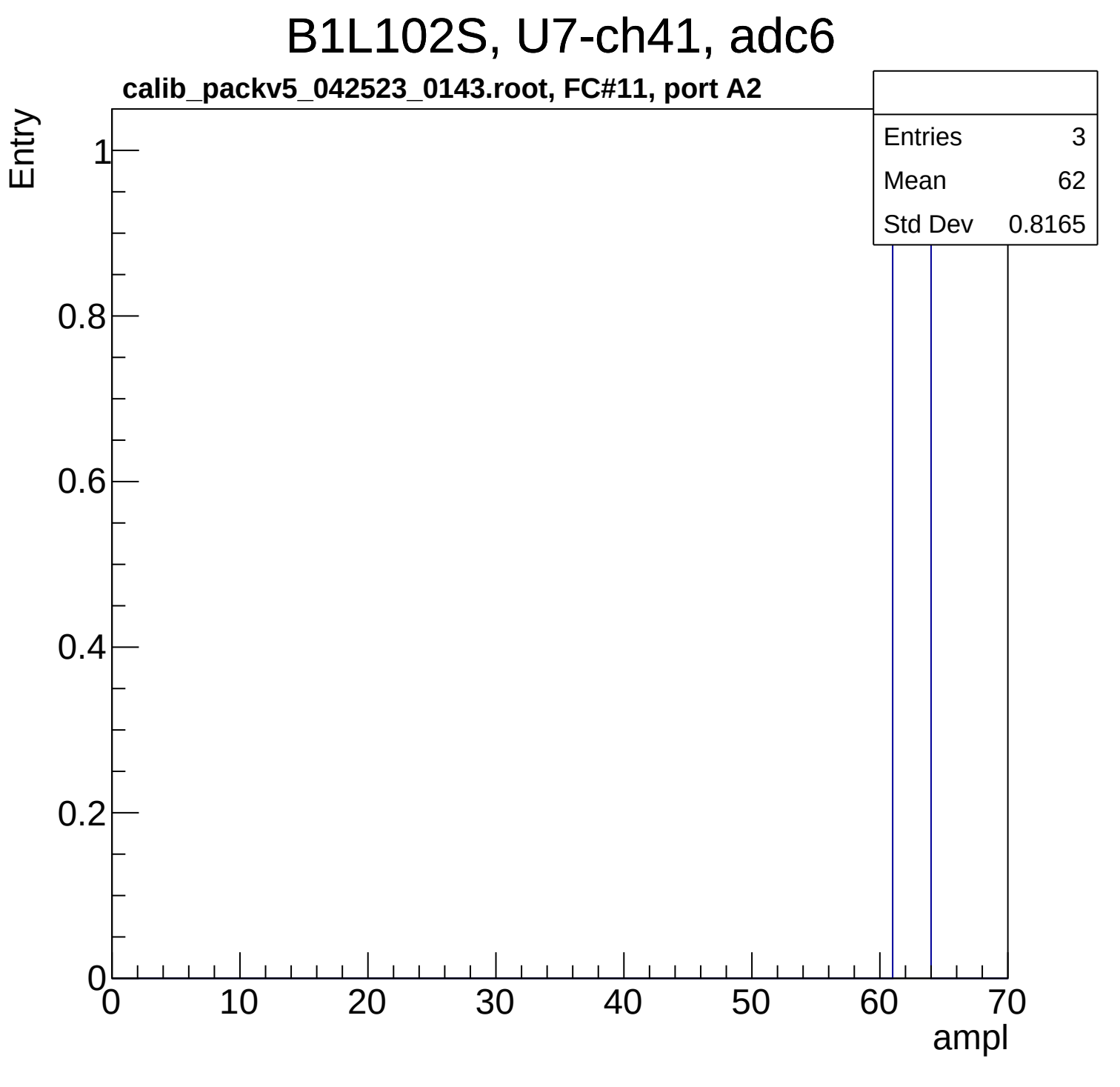
60
70


B1L102S, U7-ch41, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 3
Mean 62
Std Dev 0.8165
Entry
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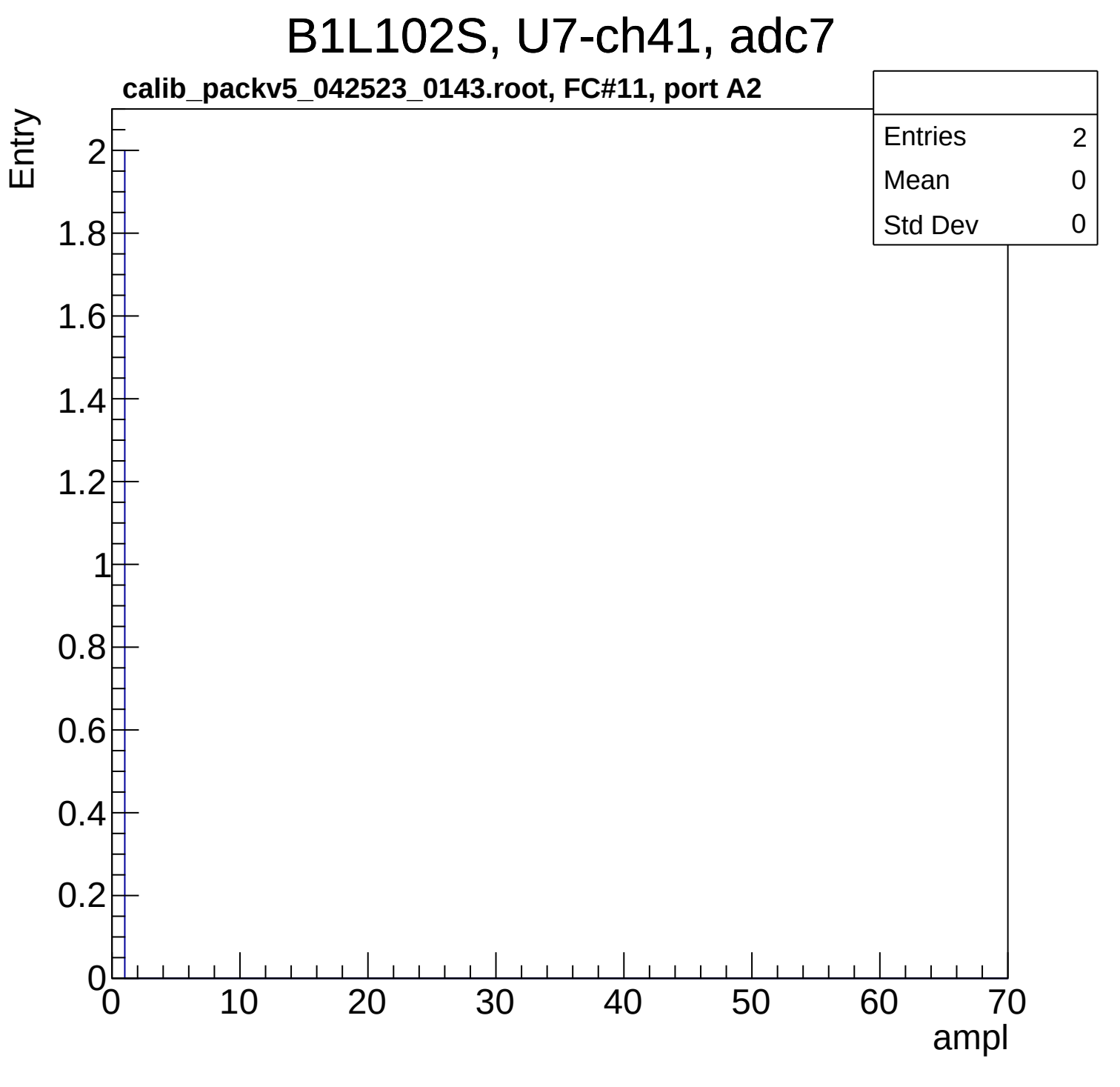
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U7-ch41, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 2
Mean 0
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
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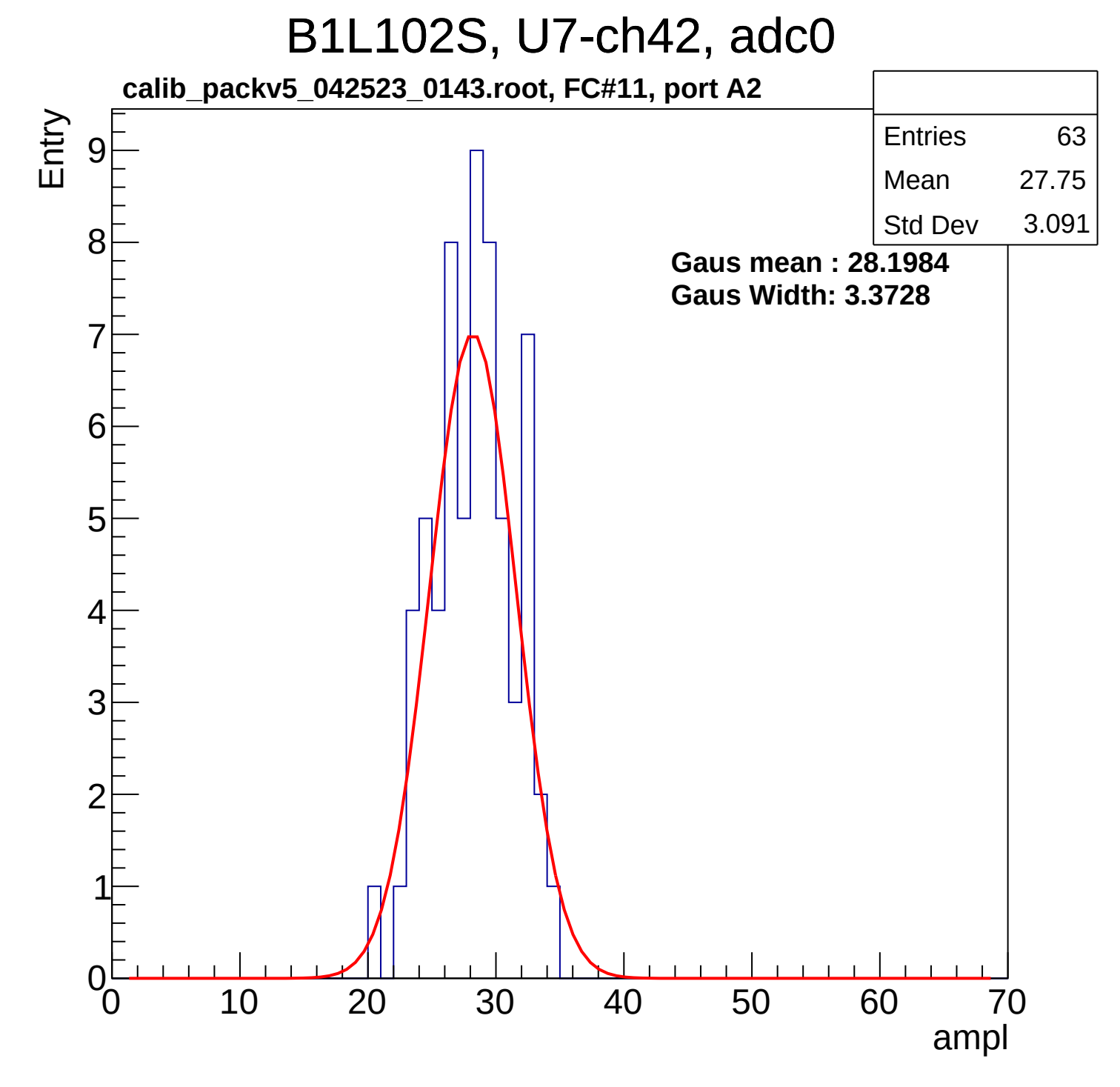
40
50
60
70


B1L102S, U7-ch42, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 63
Mean 27.75
Std Dev 3.091
Gaus mean : 28.1984
Gaus Width: 3.3728
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
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60
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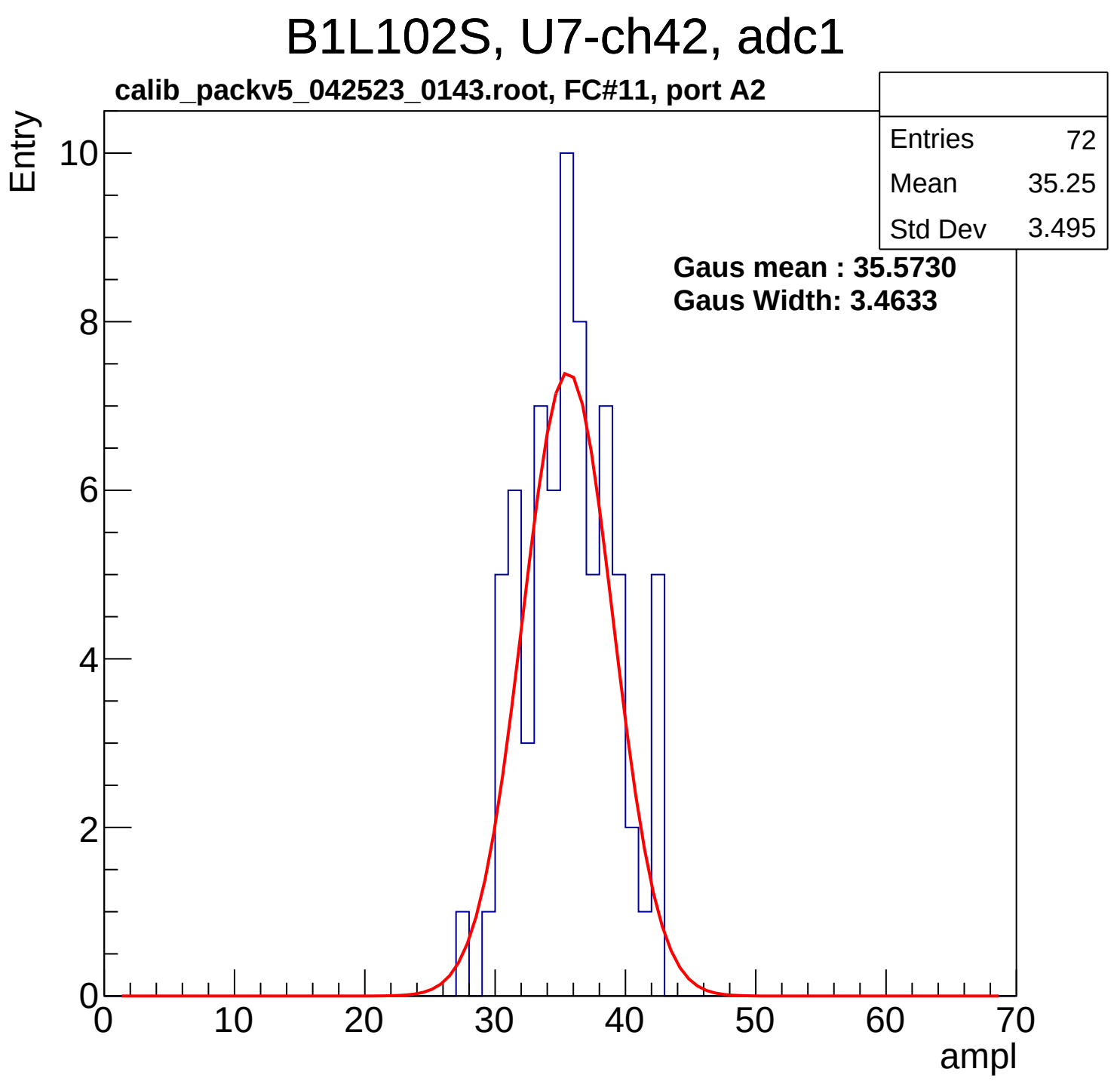
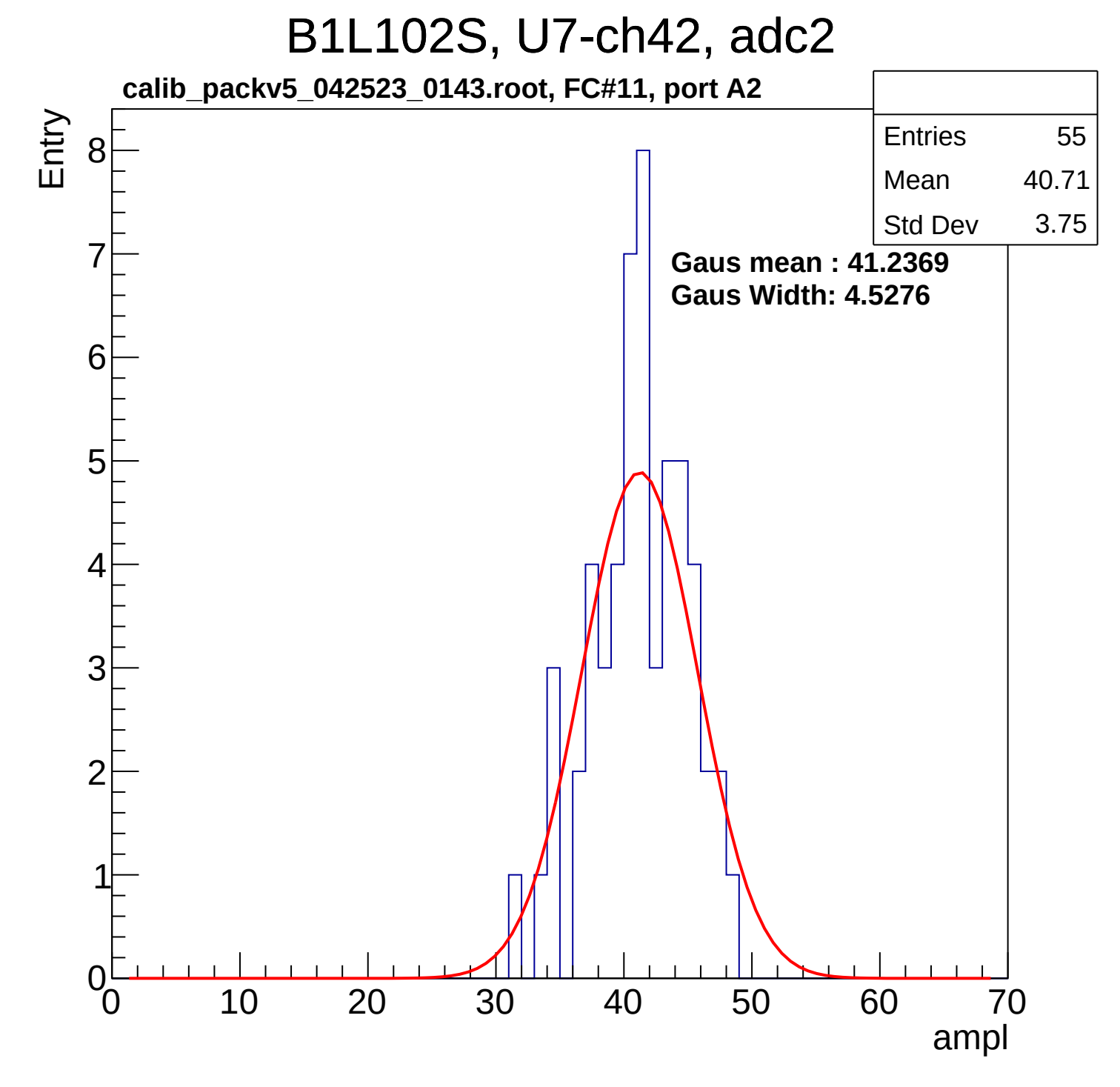

B1L102S, U7-ch42, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 72
Mean 35.25
Std Dev 3.495
Gaus mean : 35.5730
Gaus Width: 3.4633
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L102S, U7-ch42, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 55
Mean 40.71
Std Dev 3.75
Gaus mean : 41.2369
Gaus Width: 4.5276
Entry
ampl
0
1
2
3
4
5
6
7
8
0
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20
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40
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60
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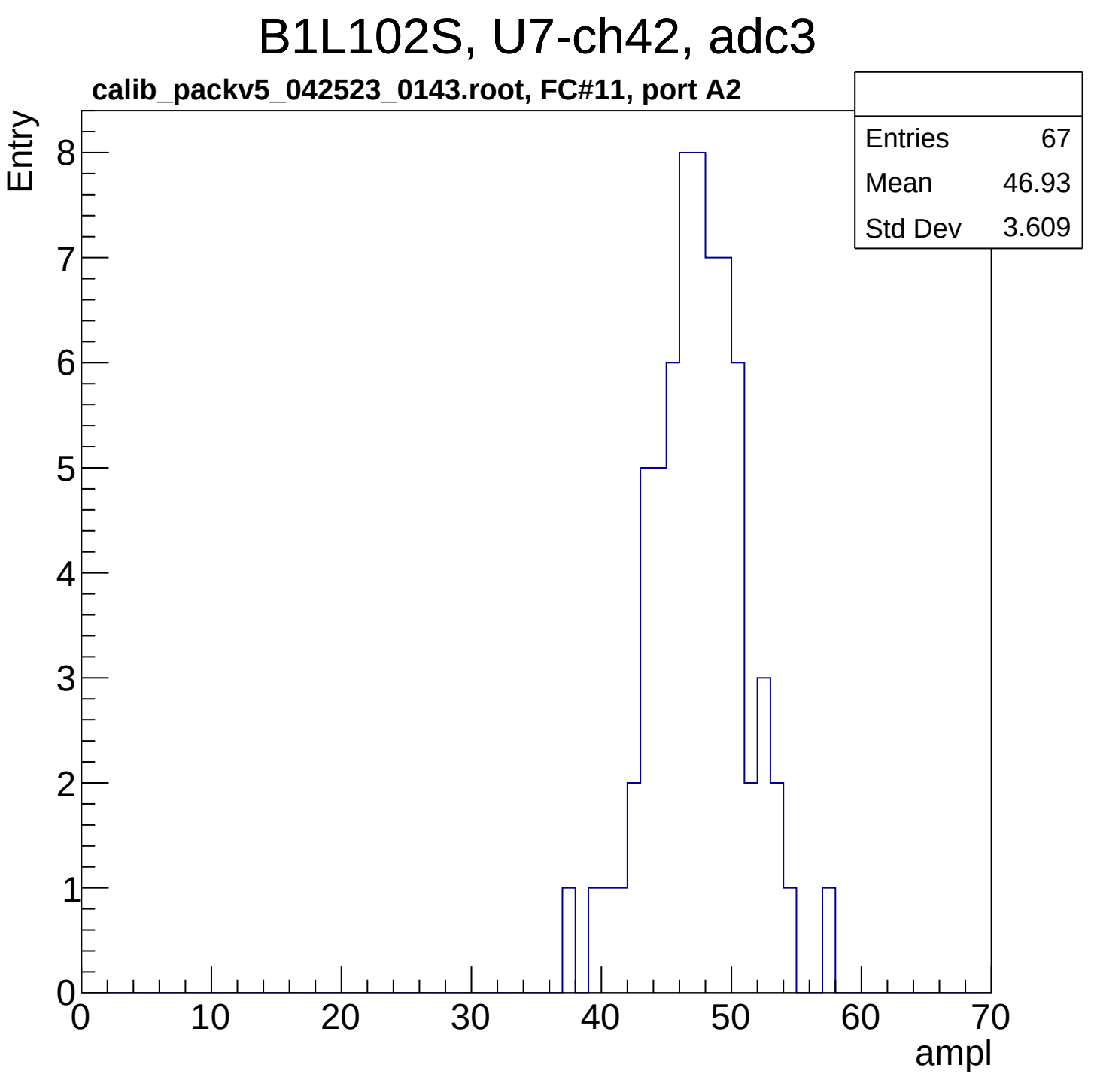
B1L102S, U7-ch42, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 67
Mean 46.93
Std Dev 3.609
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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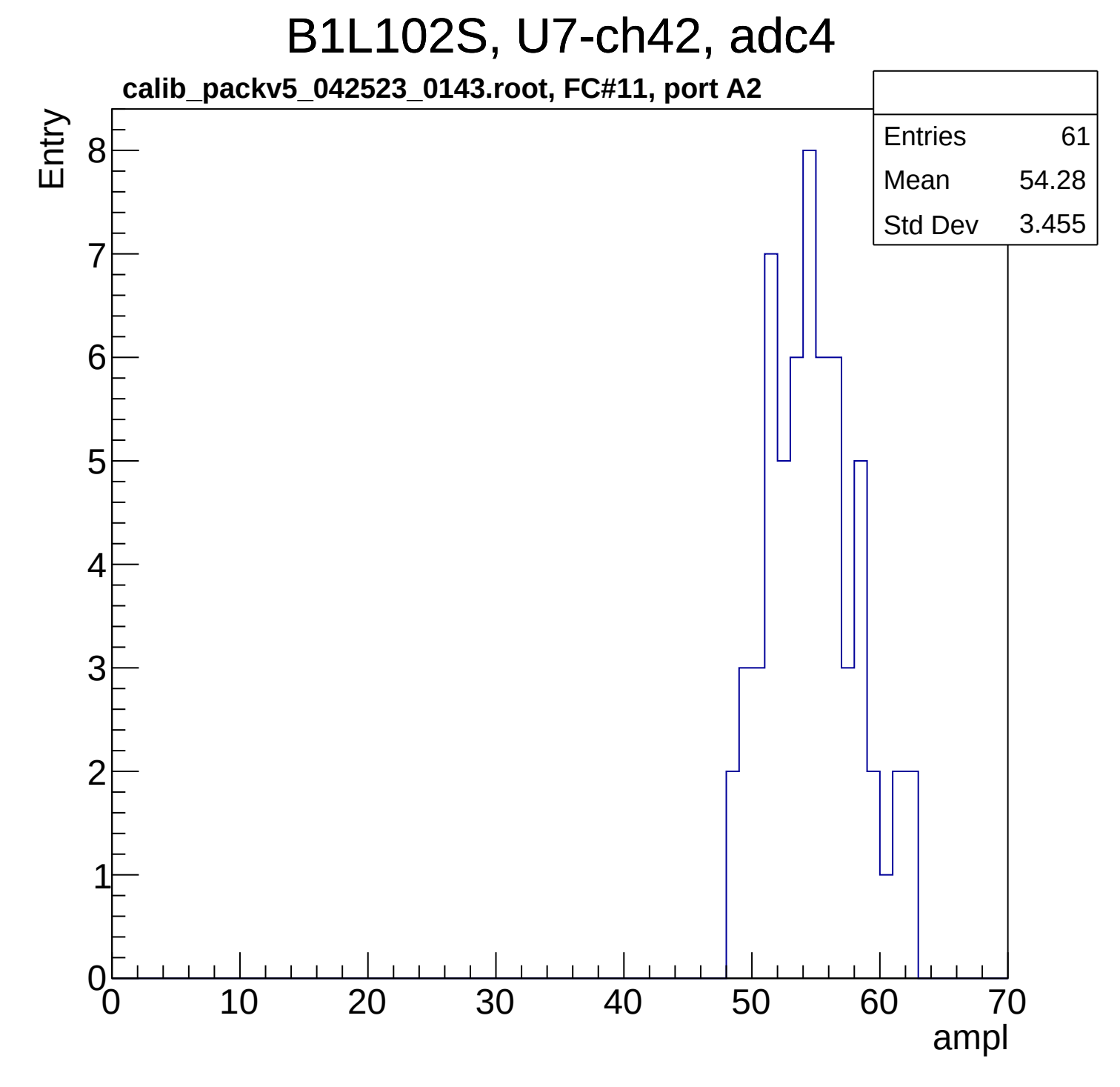
B1L102S, U7-ch42, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 61
Mean 54.28
Std Dev 3.455
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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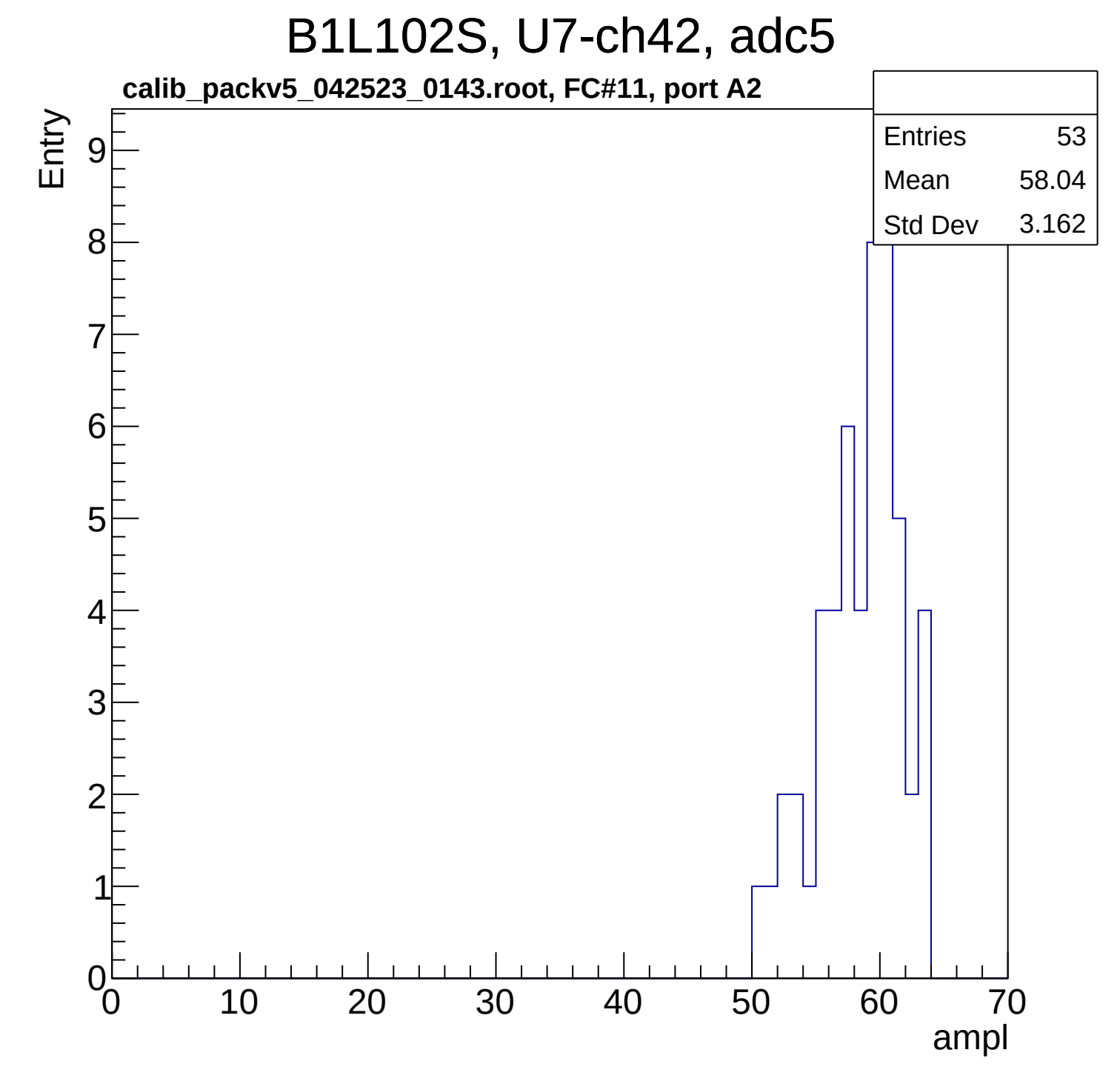
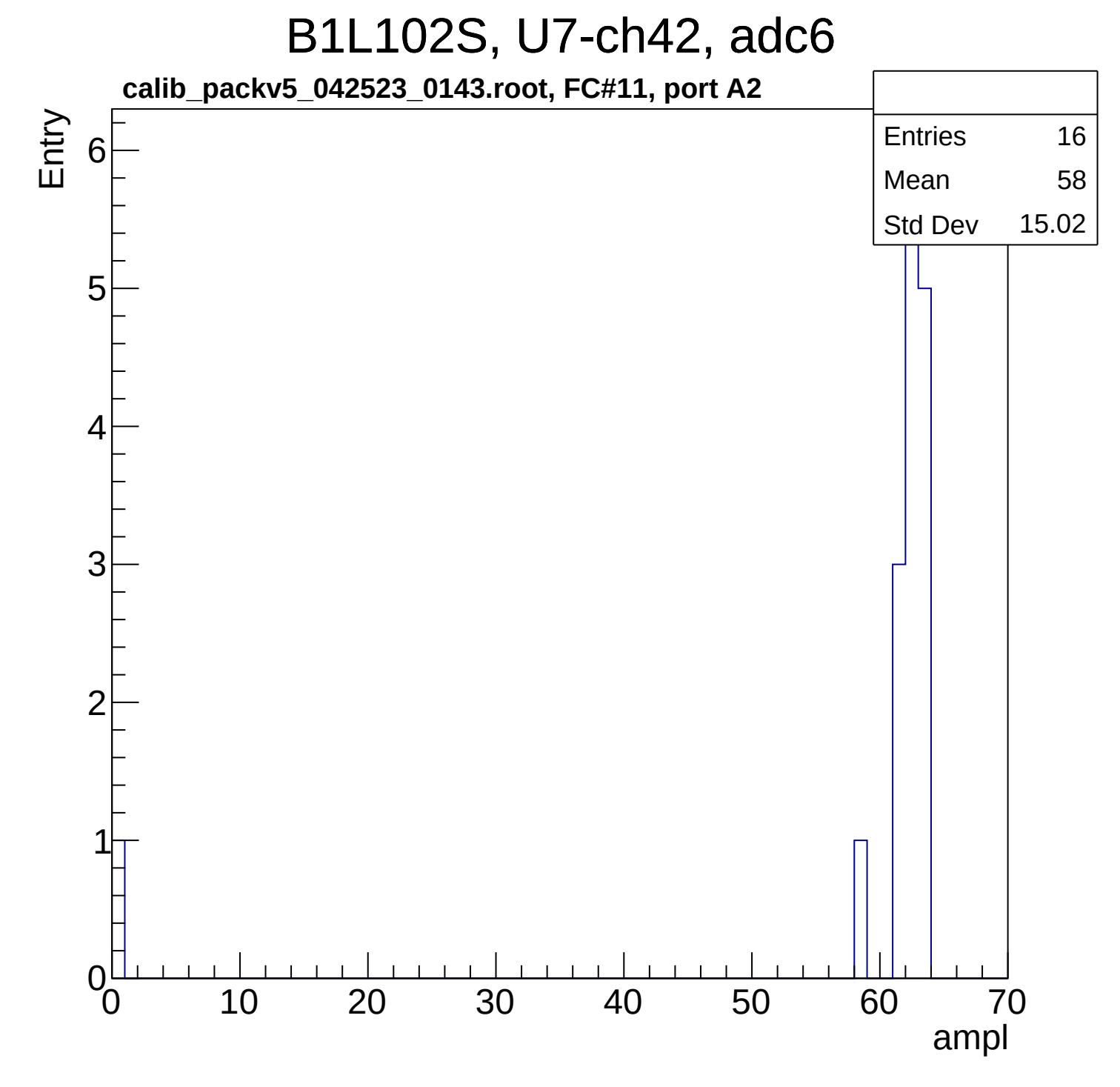
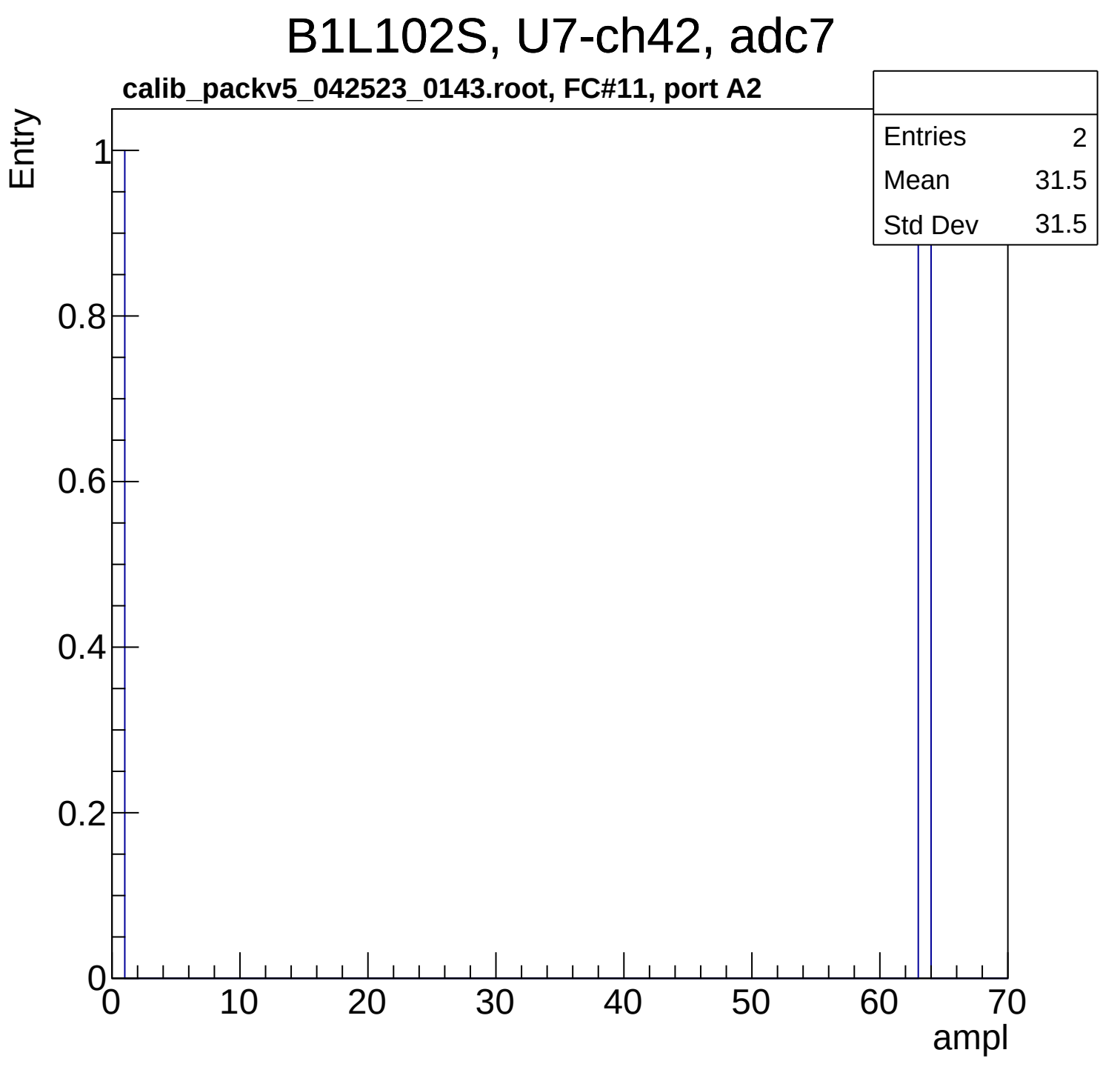
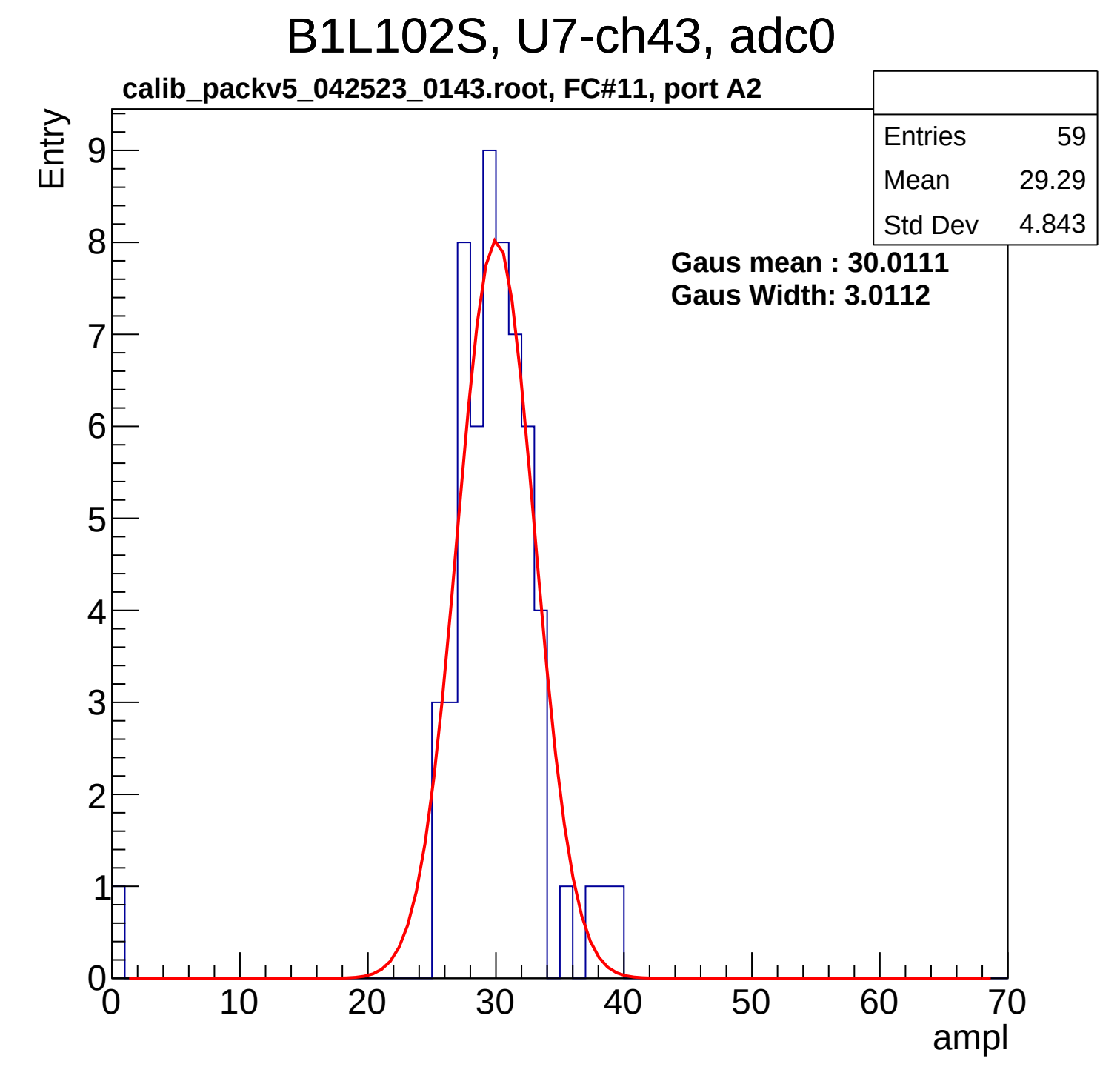
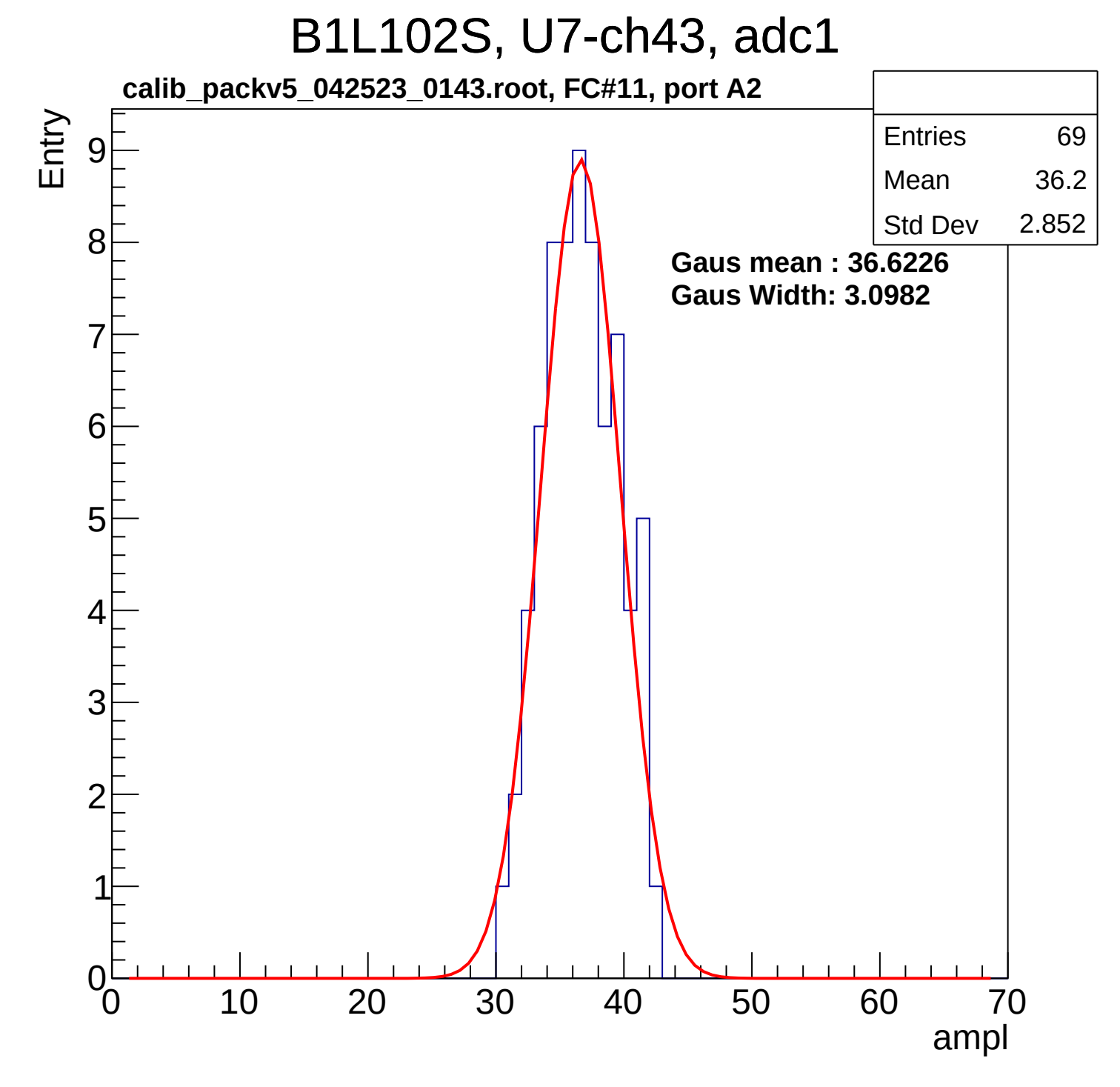

B1L102S, U7-ch42, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 53
Mean 58.04
Std Dev 3.162
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L102S, U7-ch42, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 16
Mean 58
Std Dev 15.02
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L102S, U7-ch42, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 2
Mean 31.5
Std Dev 31.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U7-ch43, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 59
Mean 29.29
Std Dev 4.843
Gaus mean : 30.0111
Gaus Width: 3.0112
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L102S, U7-ch43, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 69
Mean 36.2
Std Dev 2.852
Gaus mean : 36.6226
Gaus Width: 3.0982
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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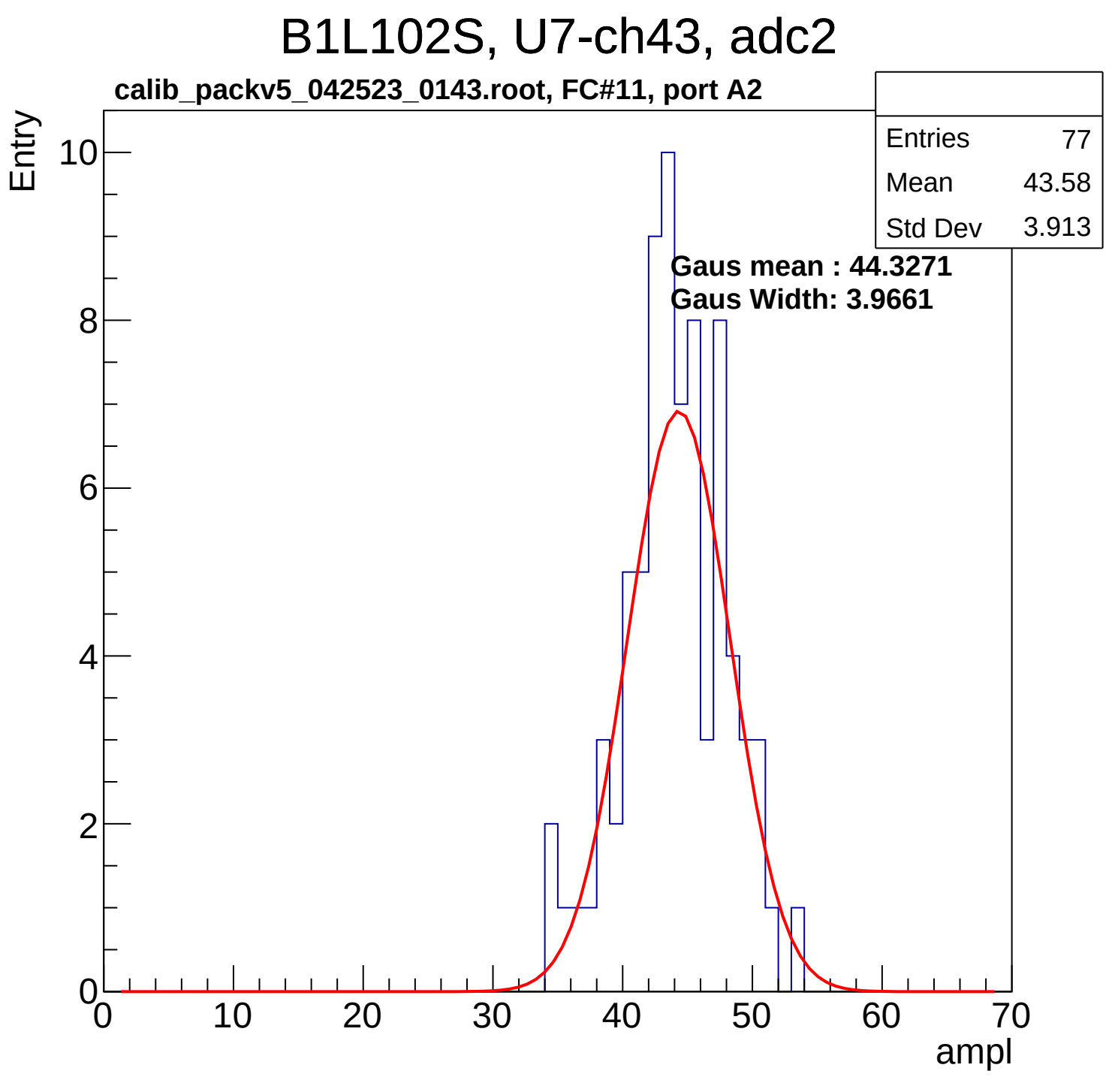
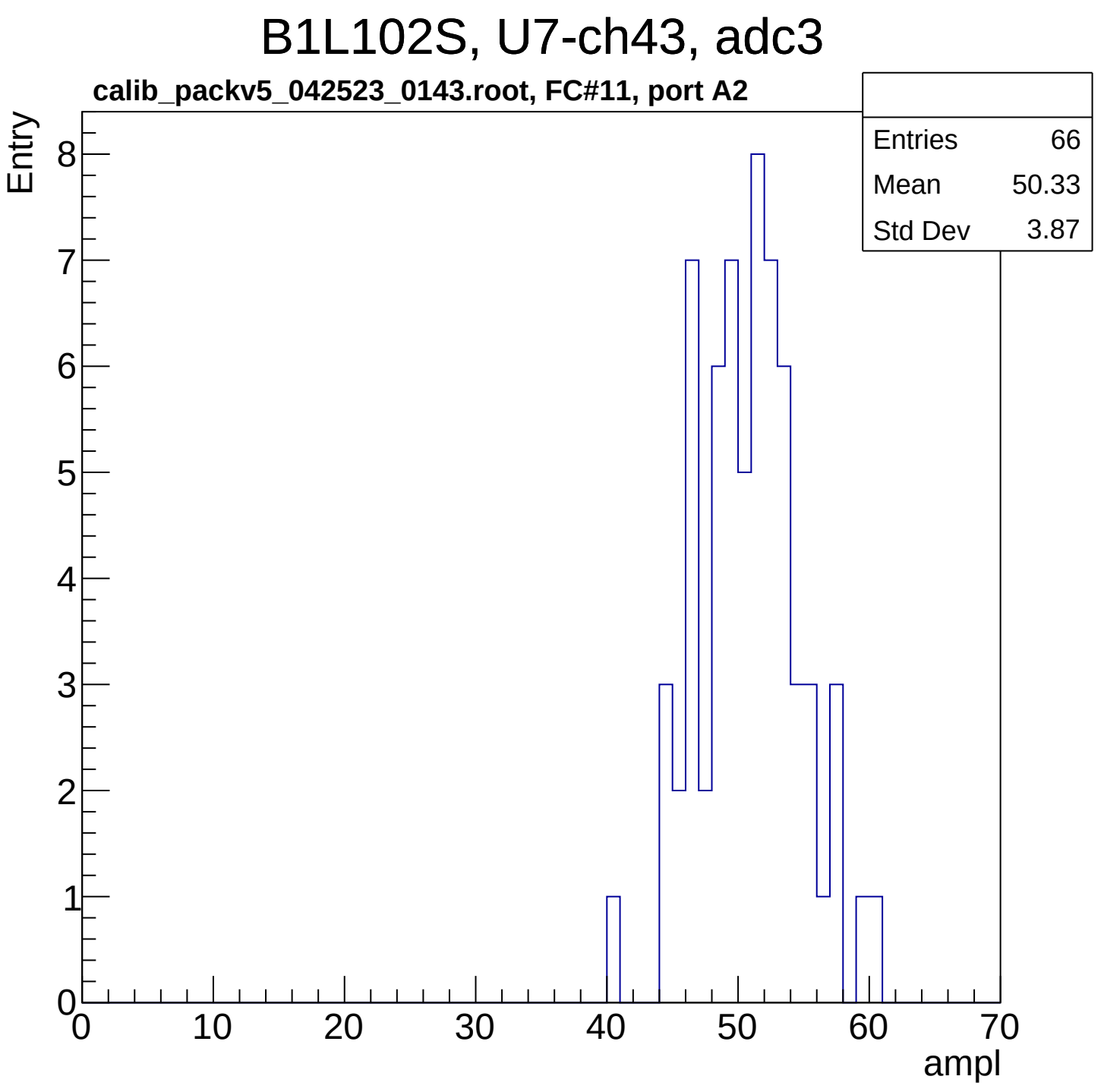
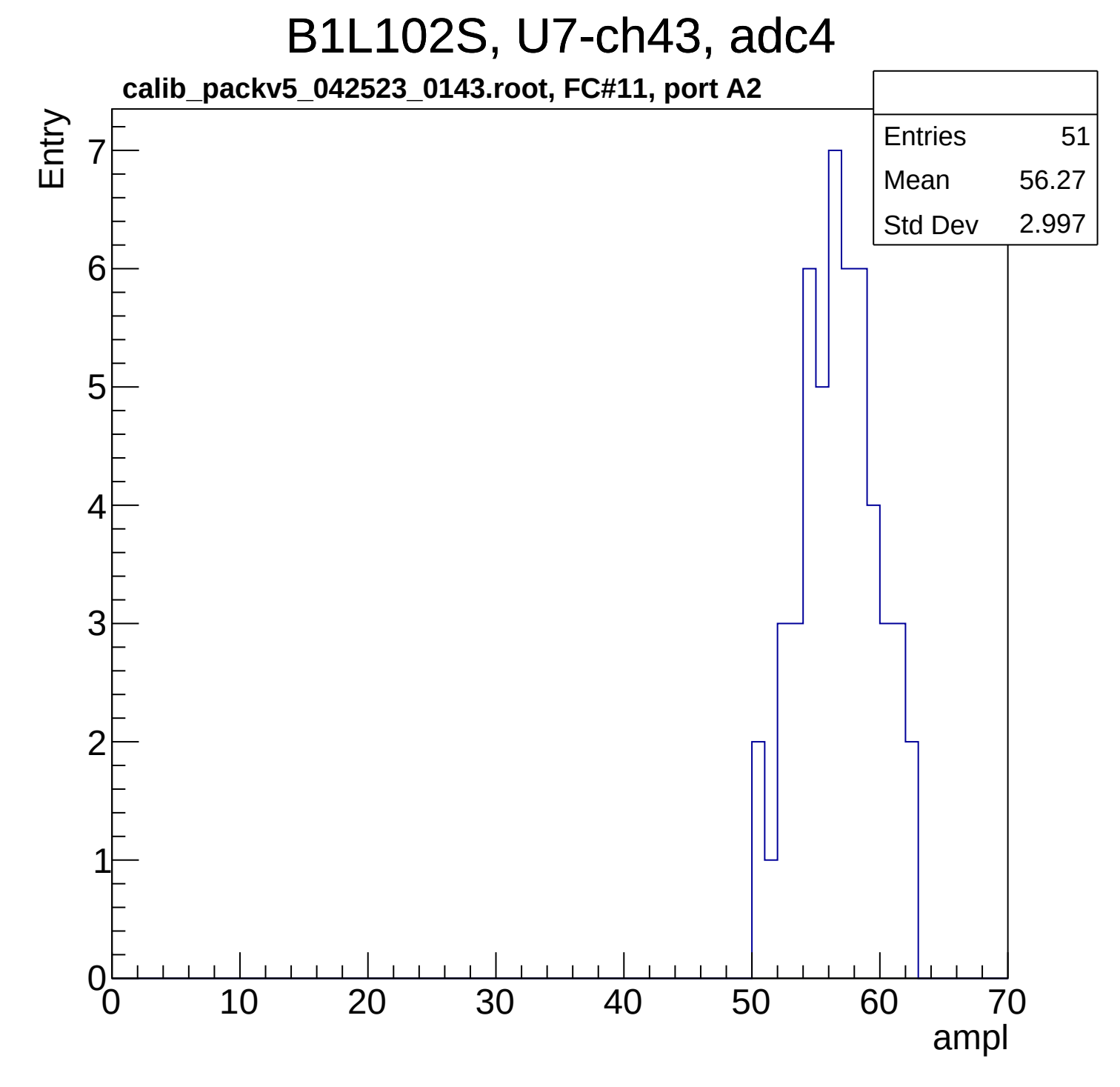
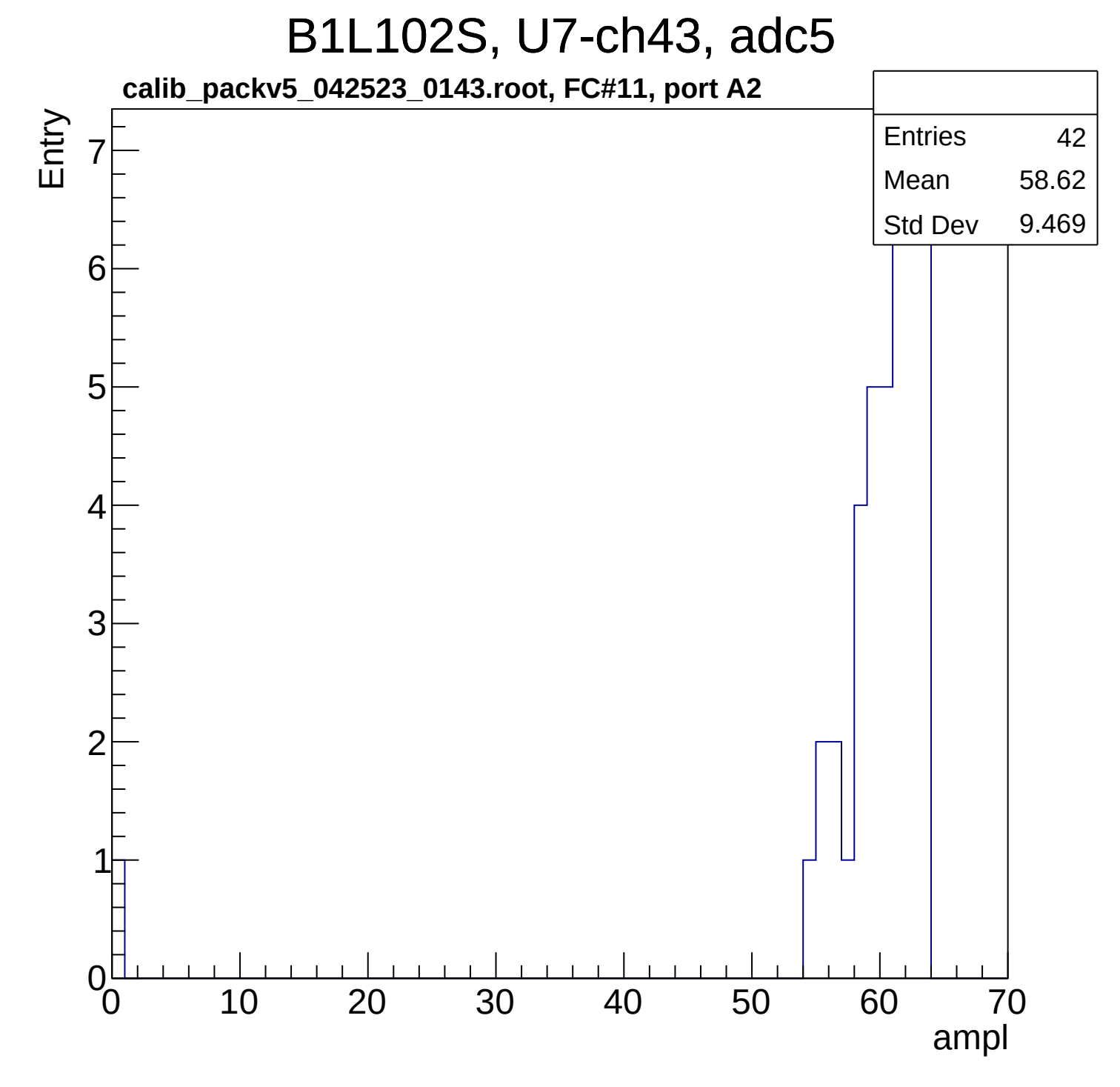
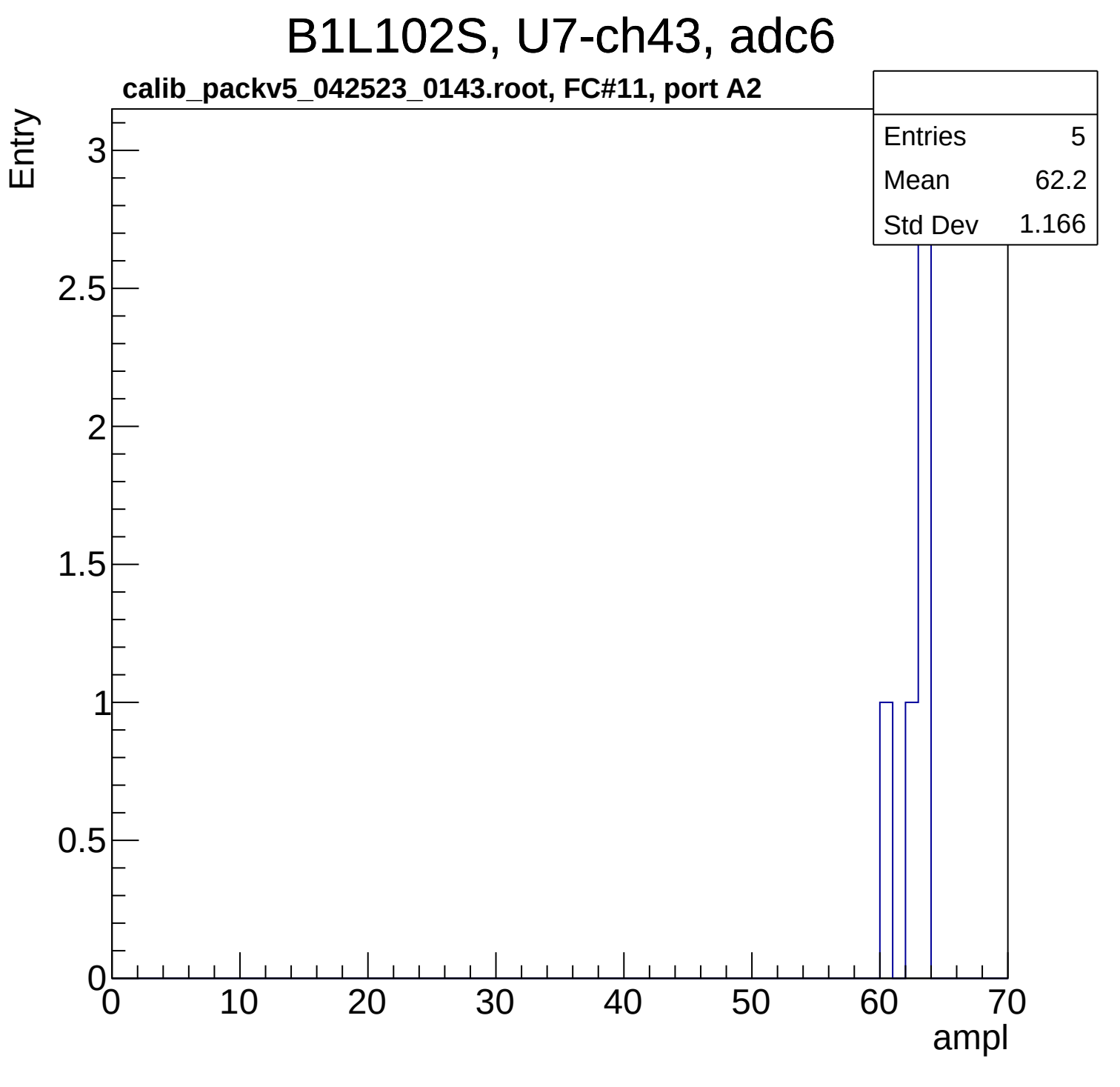
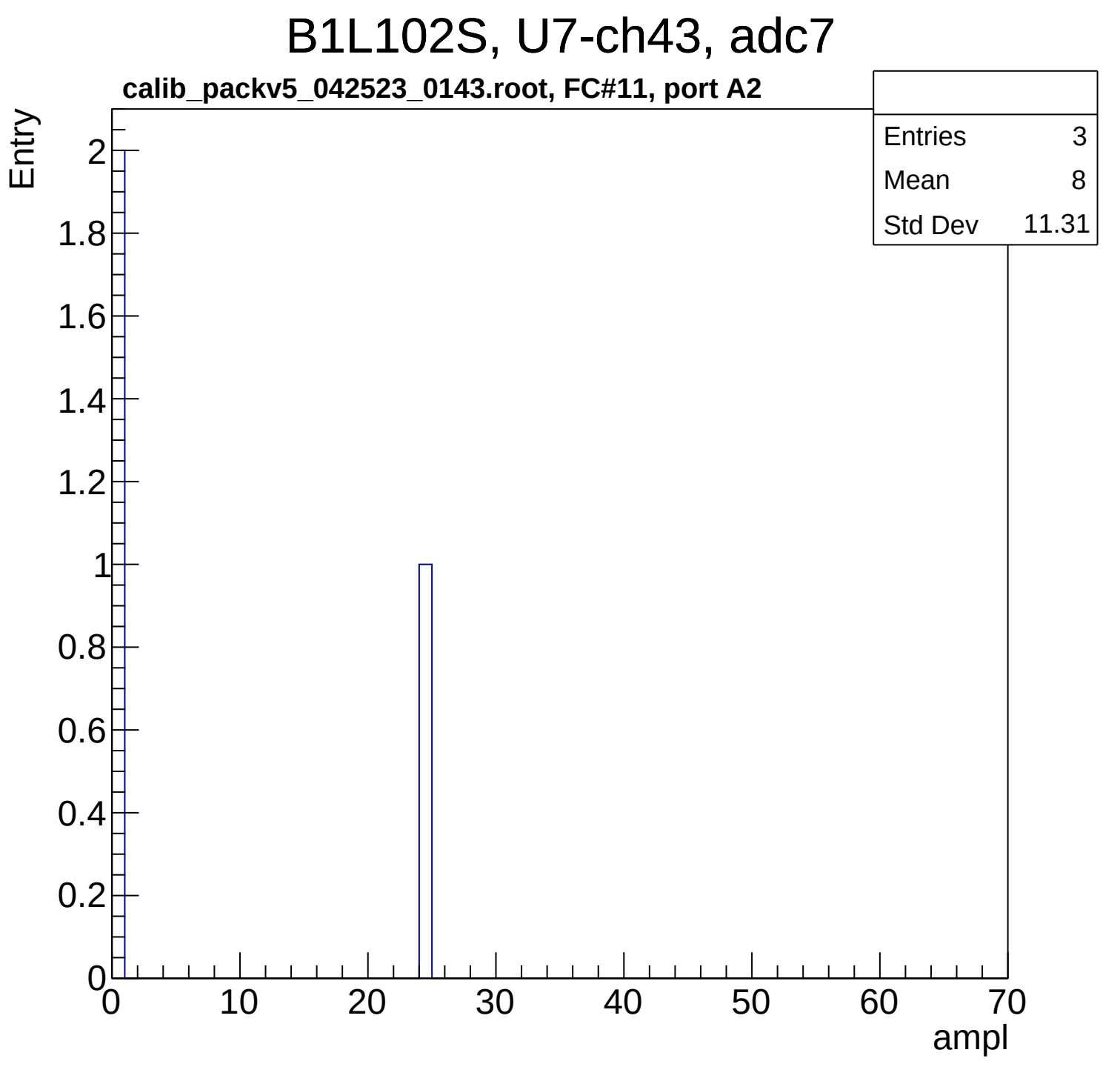

B1L102S, U7-ch43, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 77
Mean 43.58
Std Dev 3.913
Gaus mean : 44.3271
Gaus Width: 3.9661
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

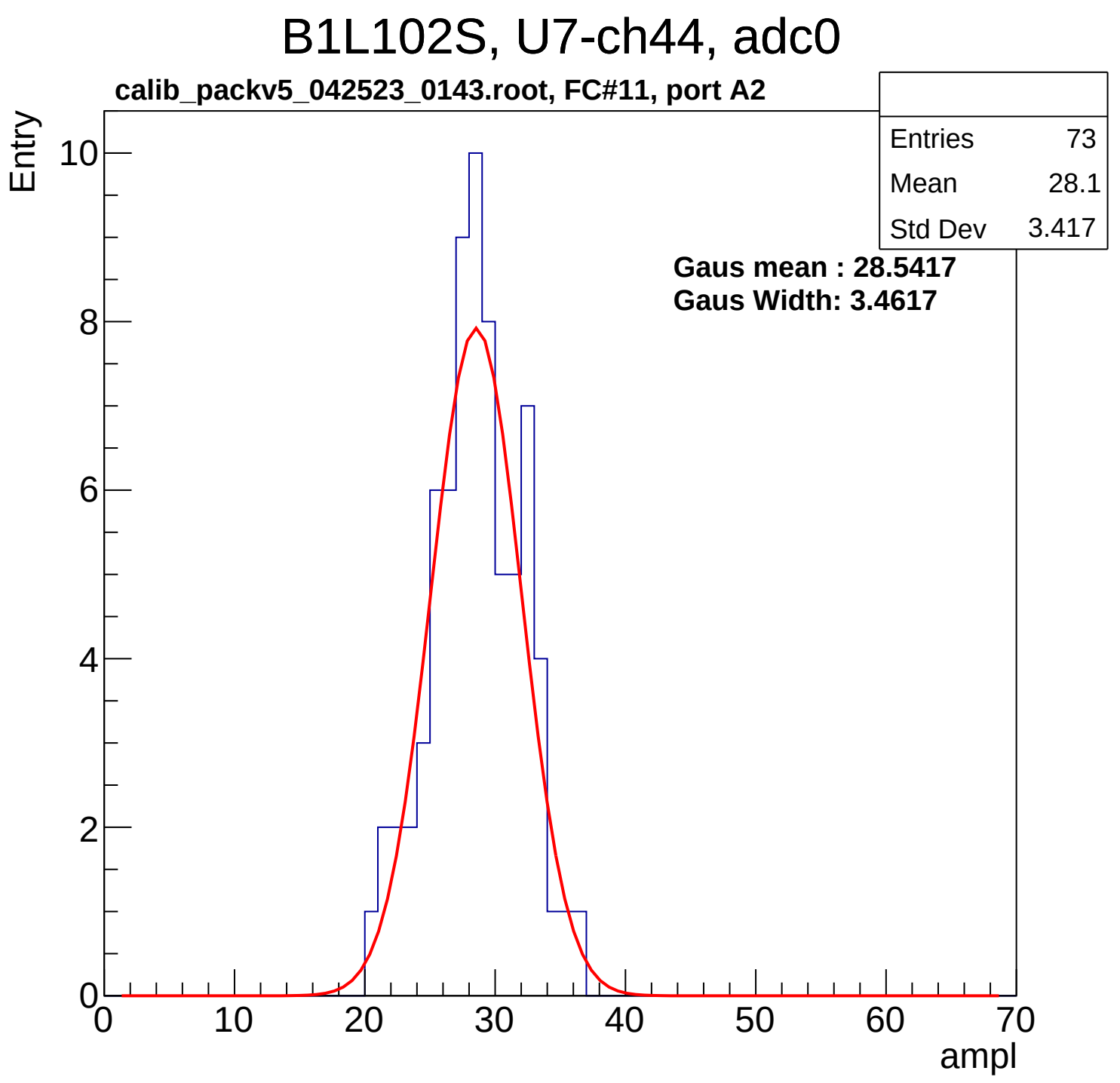

B1L102S, U7-ch43, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 66
Mean 50.33
Std Dev 3.87
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

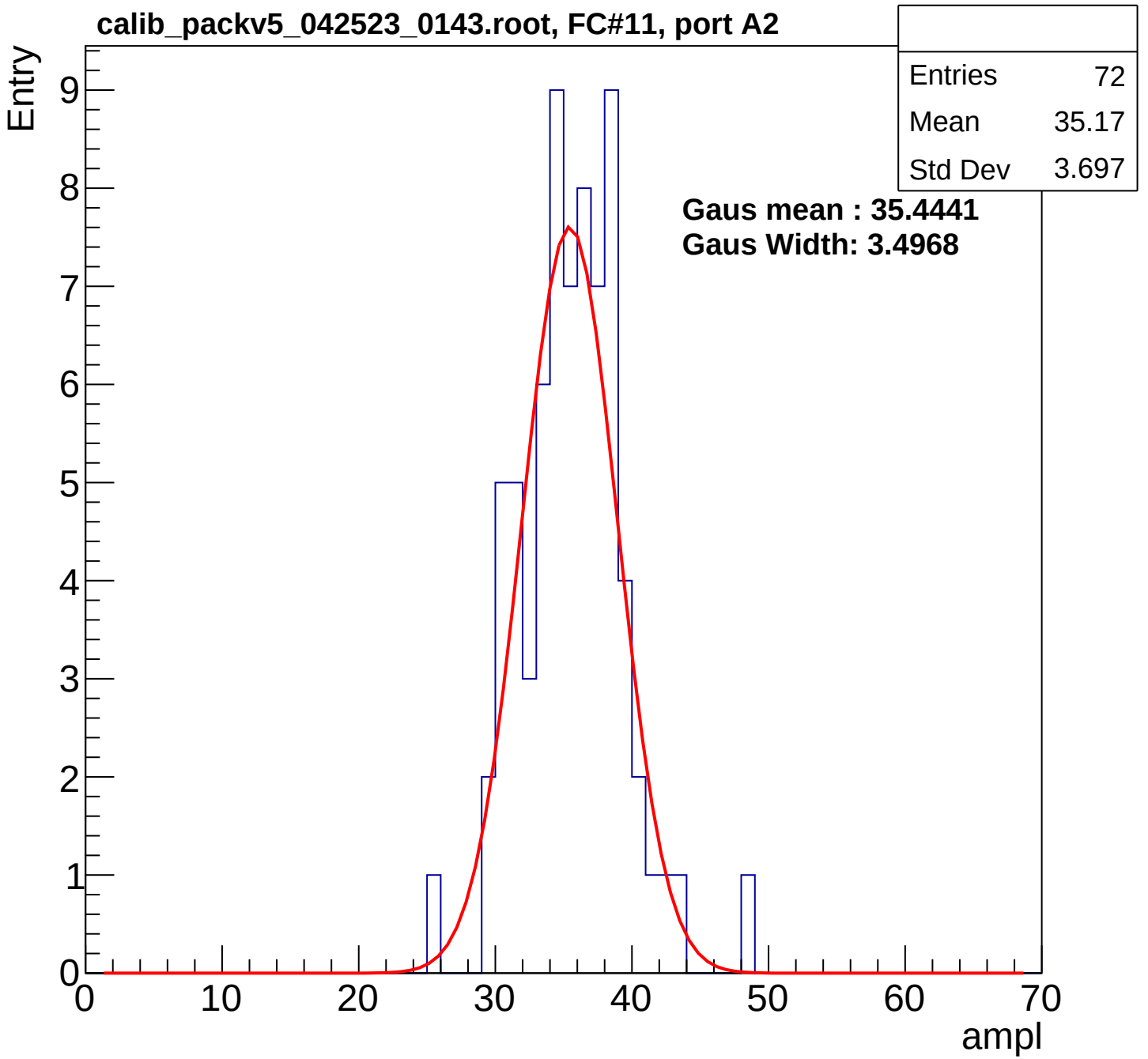

B1L102S, U7-ch43, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 51
Mean 56.27
Std Dev 2.997
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

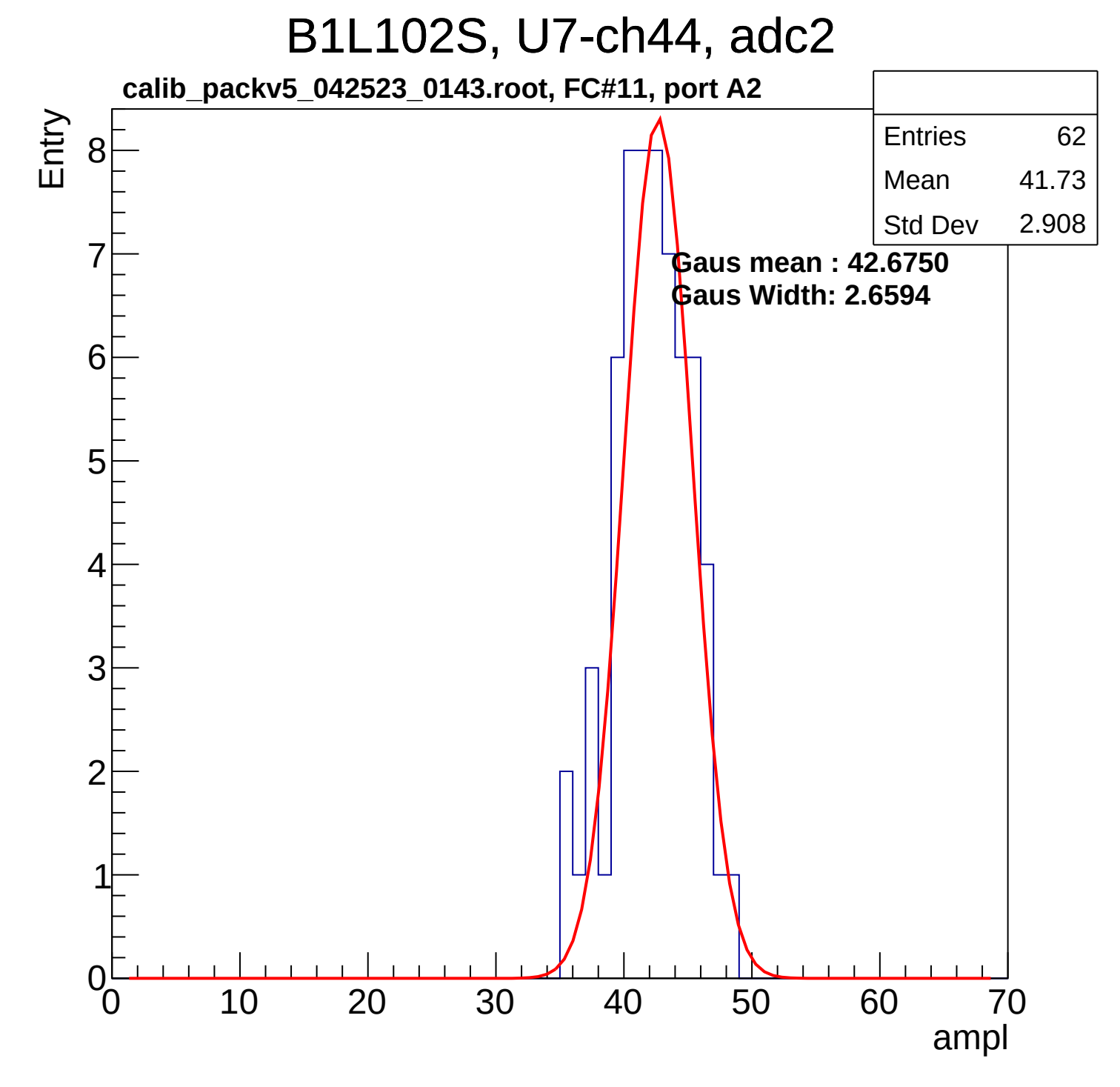

B1L102S, U7-ch43, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 42
Mean 58.62
Std Dev 9.469
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

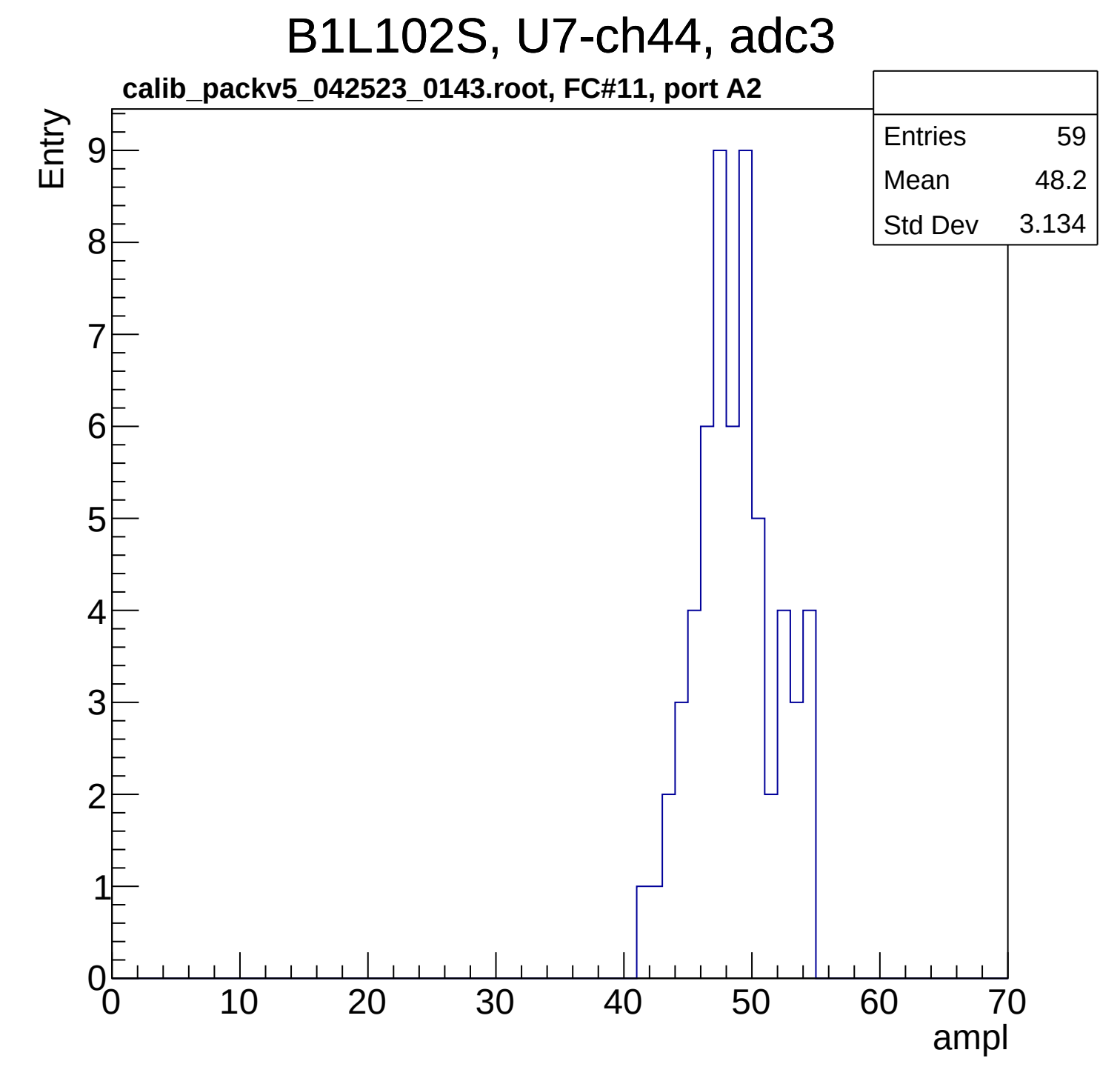

B1L102S, U7-ch43, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 5
Mean 62.2
Std Dev 1.166
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L102S, U7-ch43, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 3
Mean 8
Std Dev 11.31
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L102S, U7-ch44, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 73
Mean 28.1
Std Dev 3.417
Gaus mean : 28.5417
Gaus Width: 3.4617
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L102S, U7-ch44, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 72
Mean 35.17
Std Dev 3.697
Gaus mean : 35.4441
Gaus Width: 3.4968
Entry
ampl
0
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9


B1L102S, U7-ch44, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 62
Mean 41.73
Std Dev 2.908
Gaus mean : 42.6750
Gaus Width: 2.6594
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L102S, U7-ch44, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 59
Mean 48.2
Std Dev 3.134
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
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20
30
40
50
60
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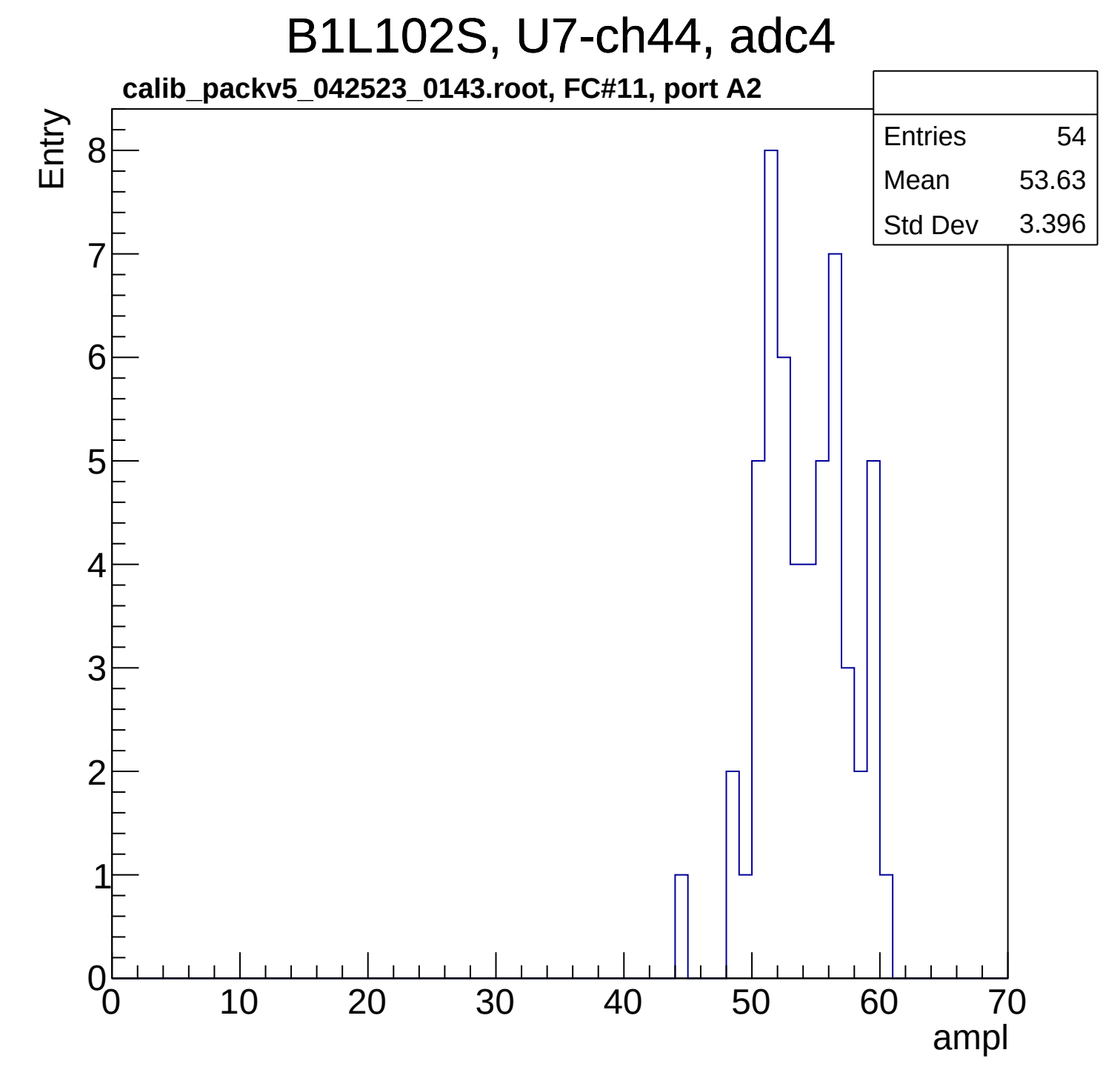
B1L102S, U7-ch44, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 54
Mean 53.63
Std Dev 3.396
Entry
ampl
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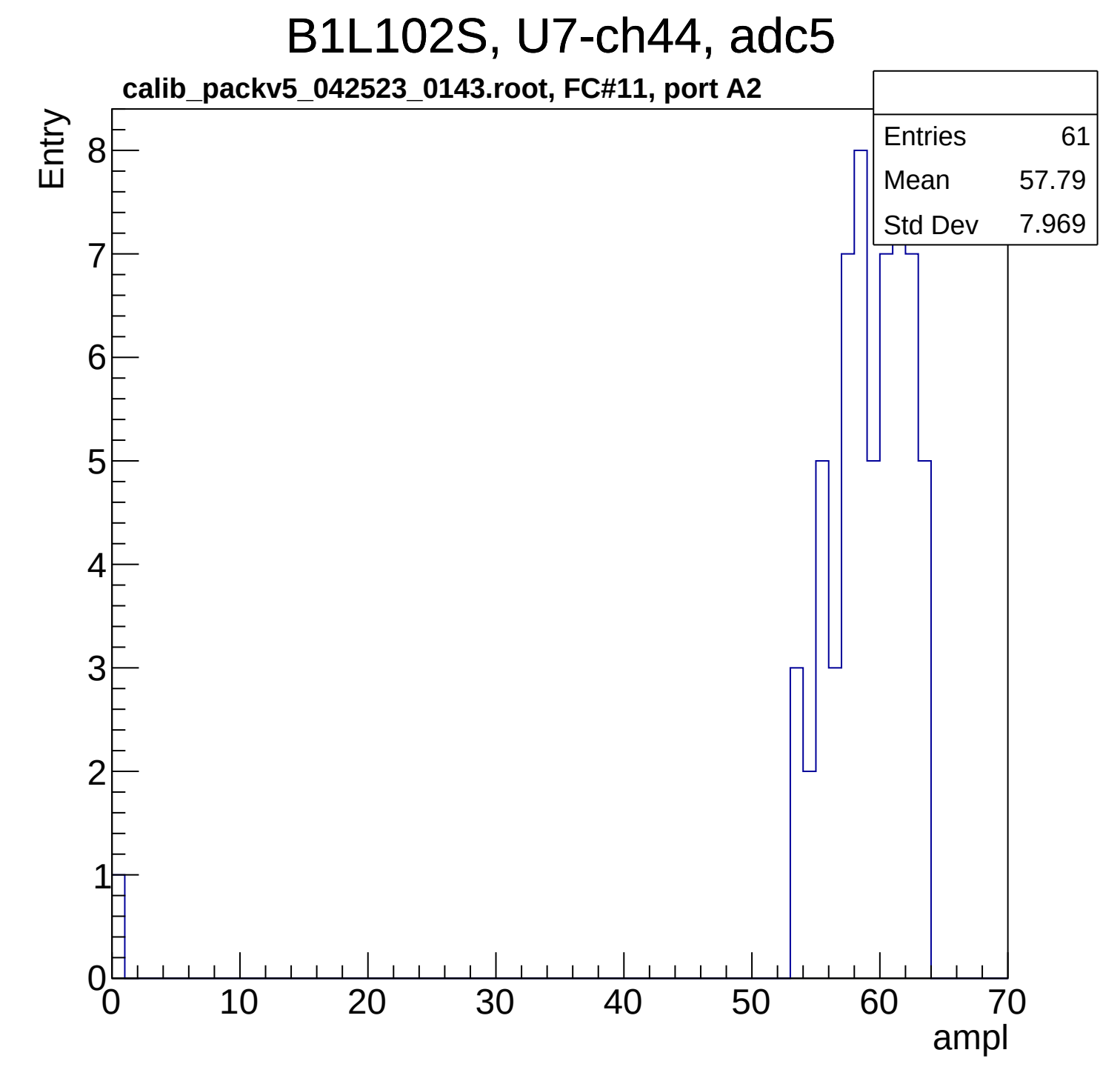
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L102S, U7-ch44, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 61
Mean 57.79
Std Dev 7.969
Entry
ampl
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1
2
3
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5
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7
8
0
10
20
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40
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60
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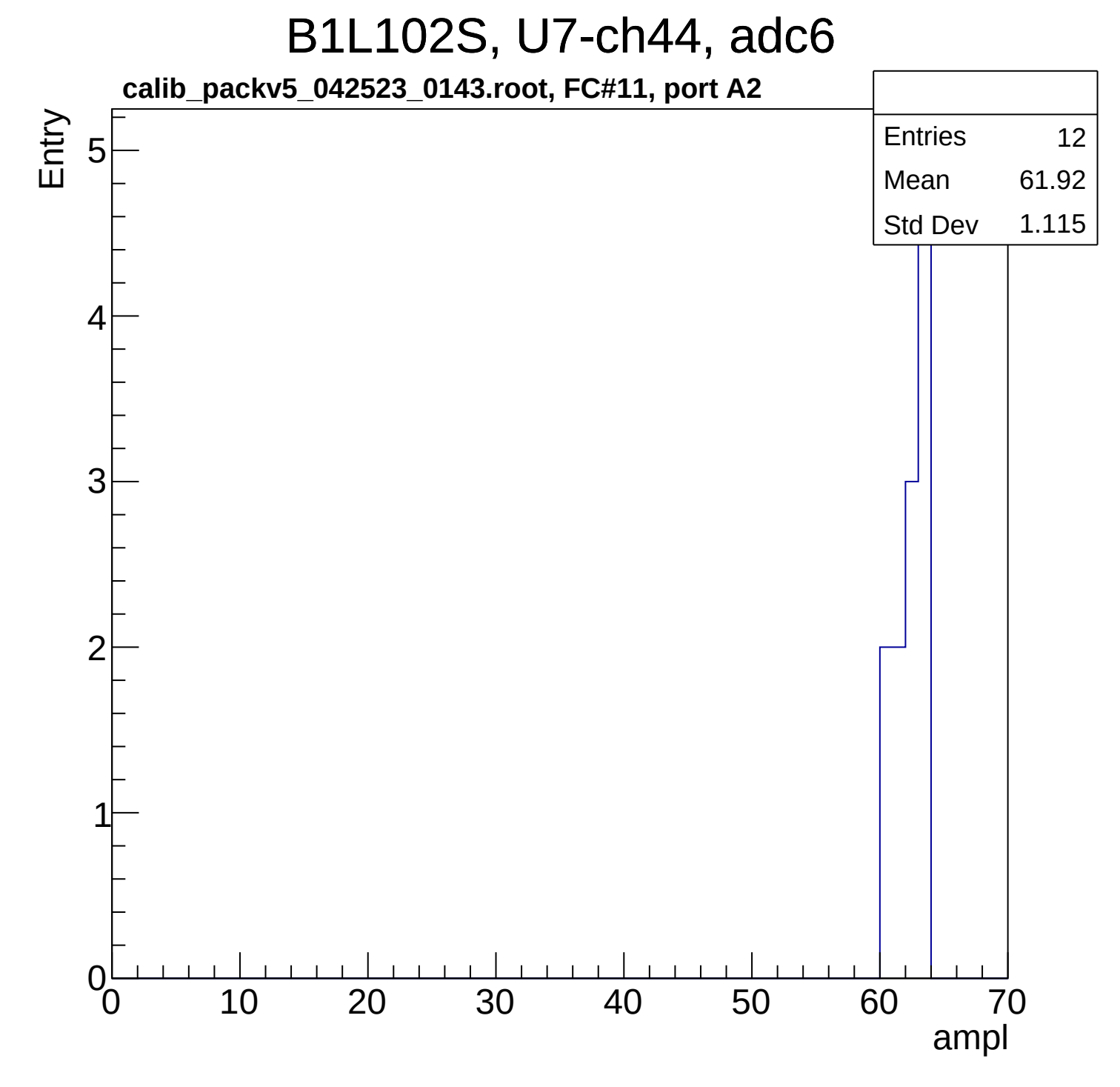
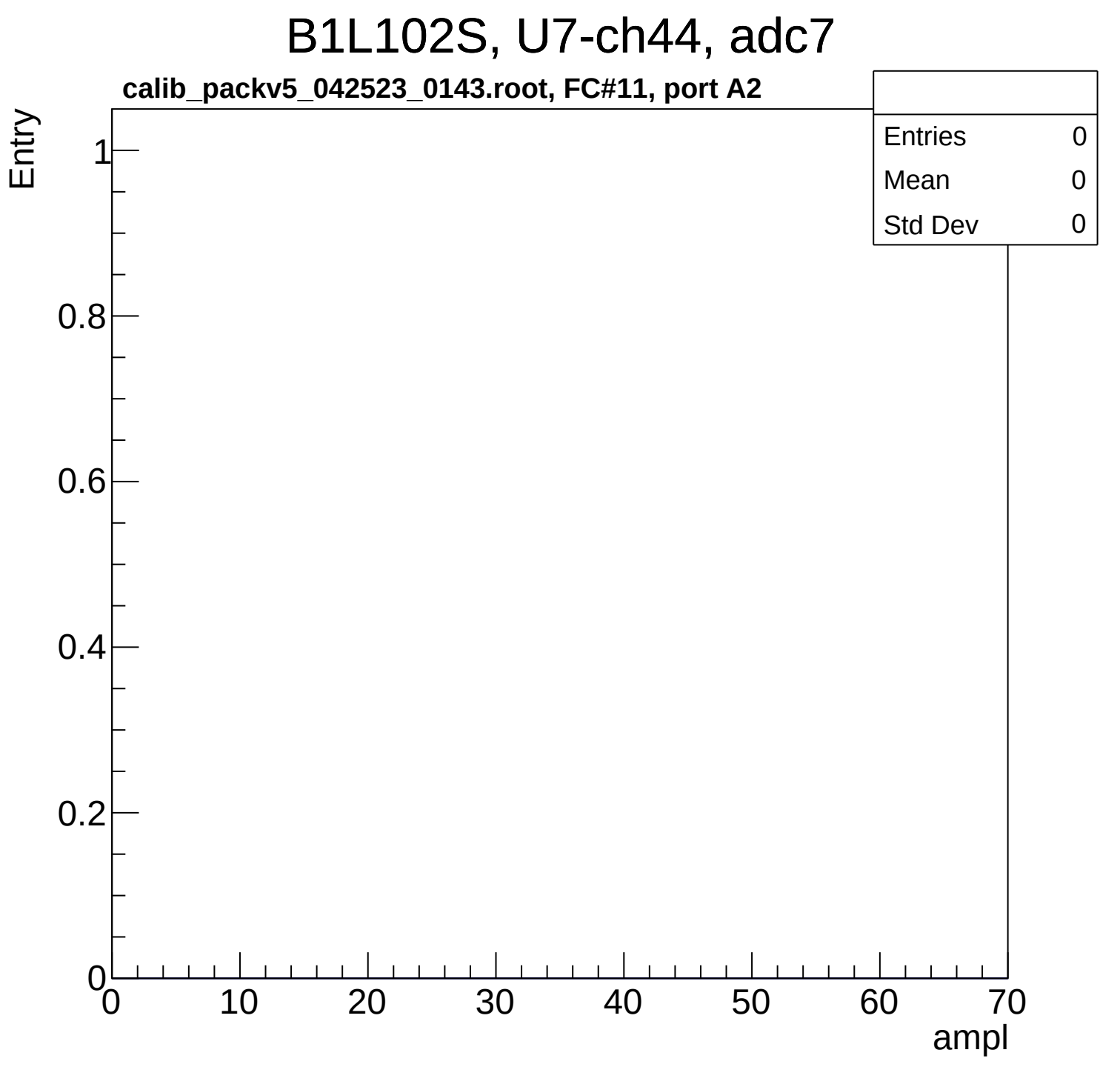
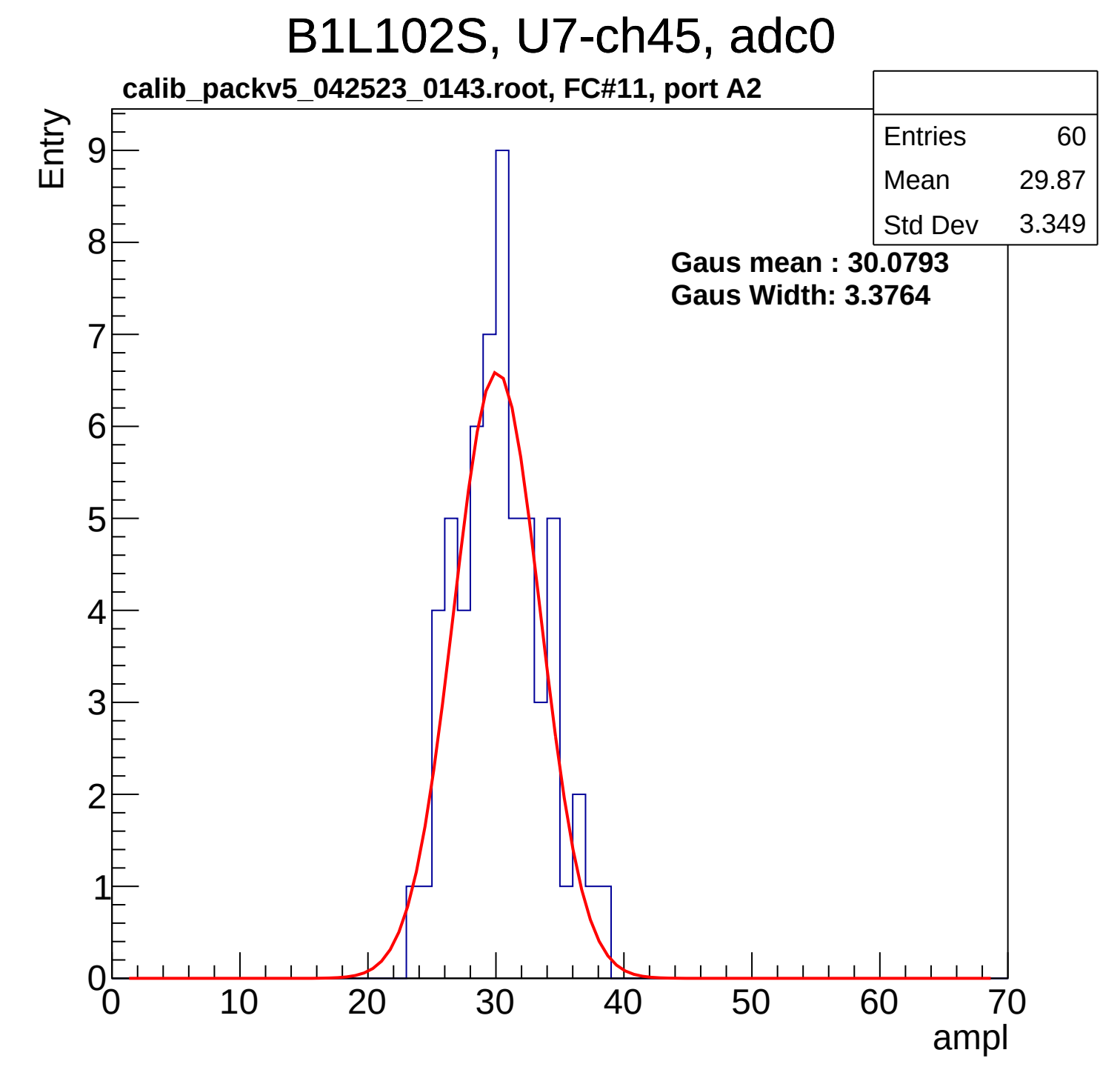
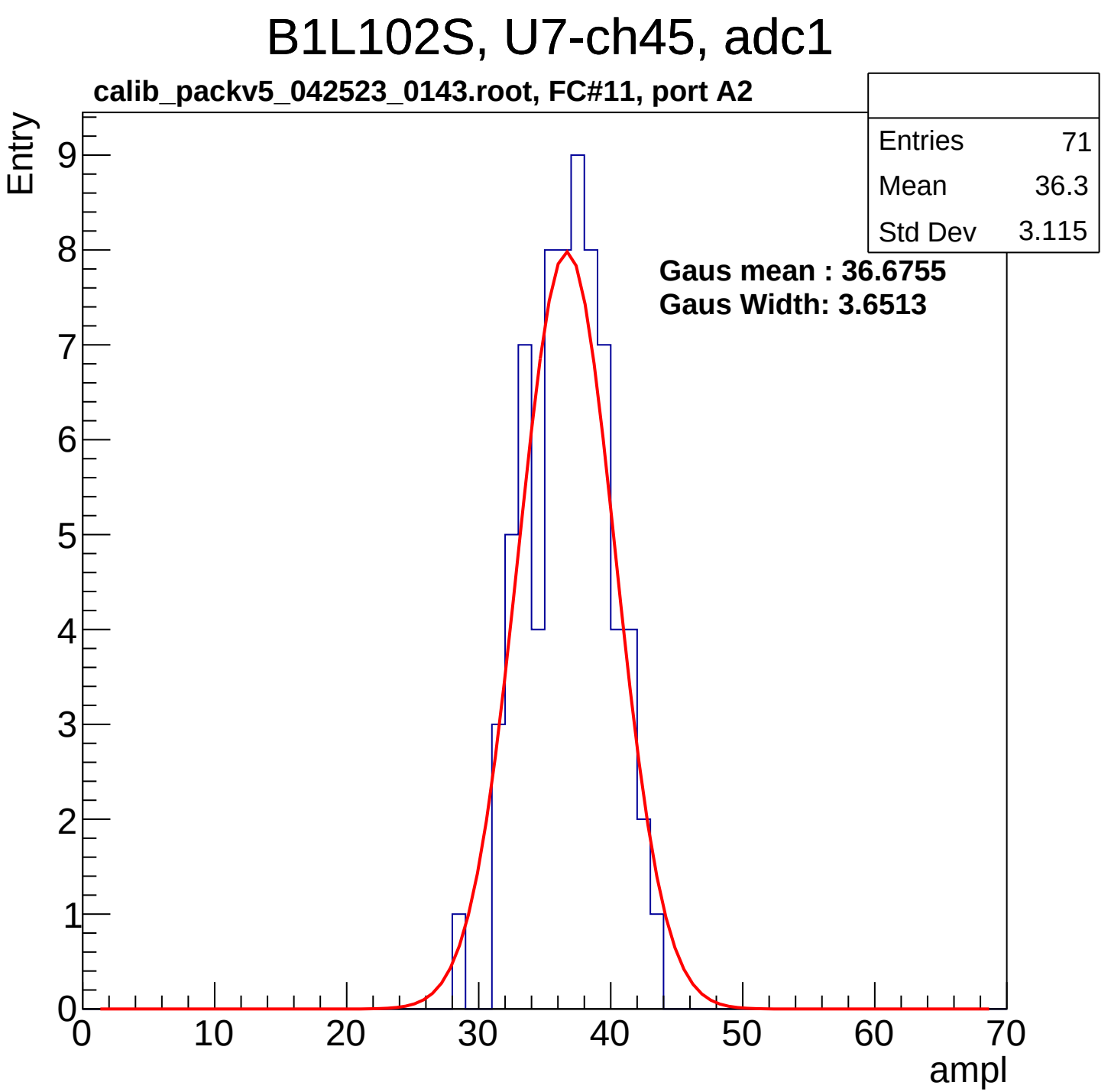
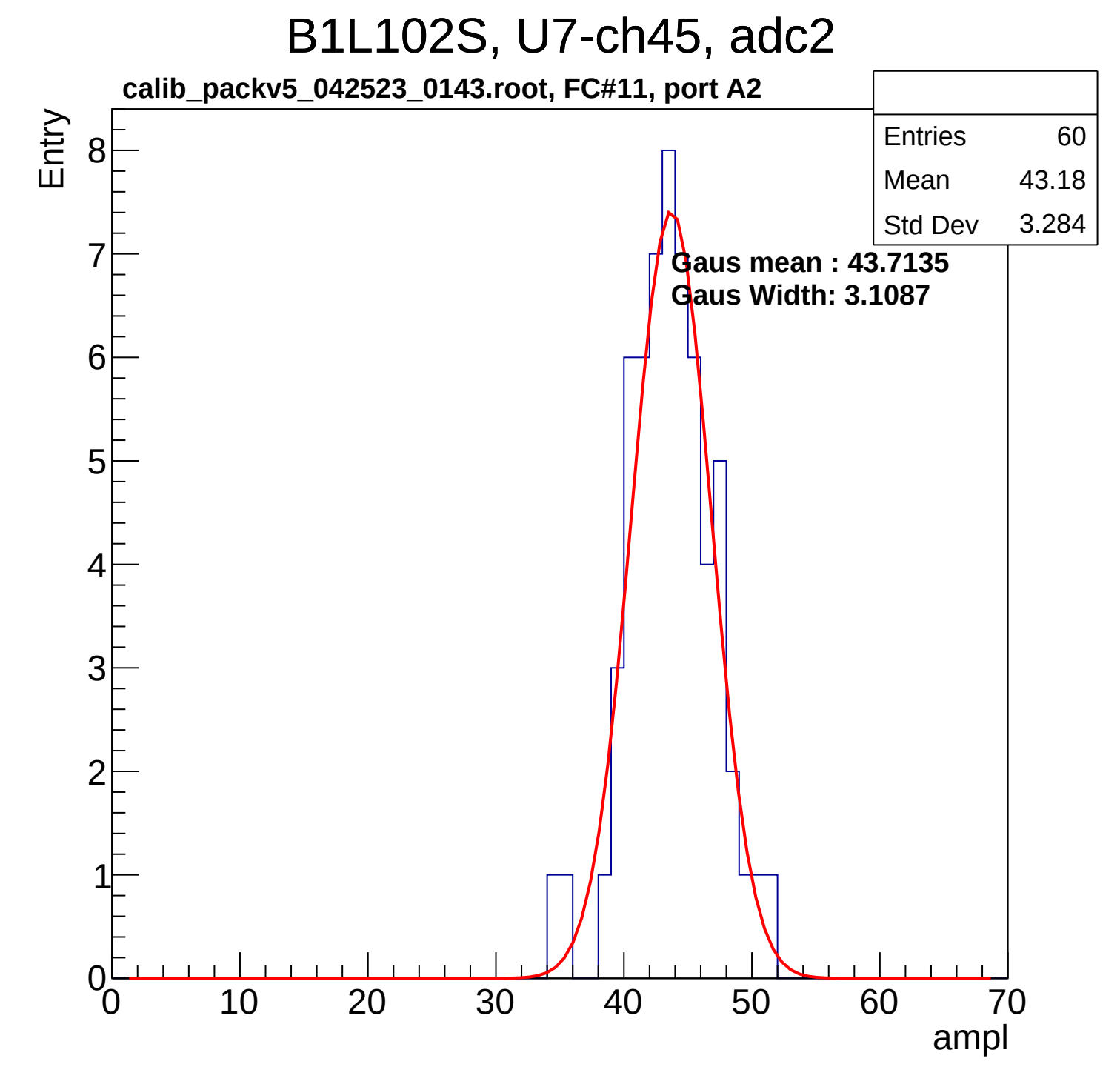

B1L102S, U7-ch44, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 12
Mean 61.92
Std Dev 1.115
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L102S, U7-ch44, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U7-ch45, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 60
Mean 29.87
Std Dev 3.349
Gaus mean : 30.0793
Gaus Width: 3.3764
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L102S, U7-ch45, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 71
Mean 36.3
Std Dev 3.115
Gaus mean : 36.6755
Gaus Width: 3.6513
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L102S, U7-ch45, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 60
Mean 43.18
Std Dev 3.284
Gaus mean : 43.7135
Gaus Width: 3.1087
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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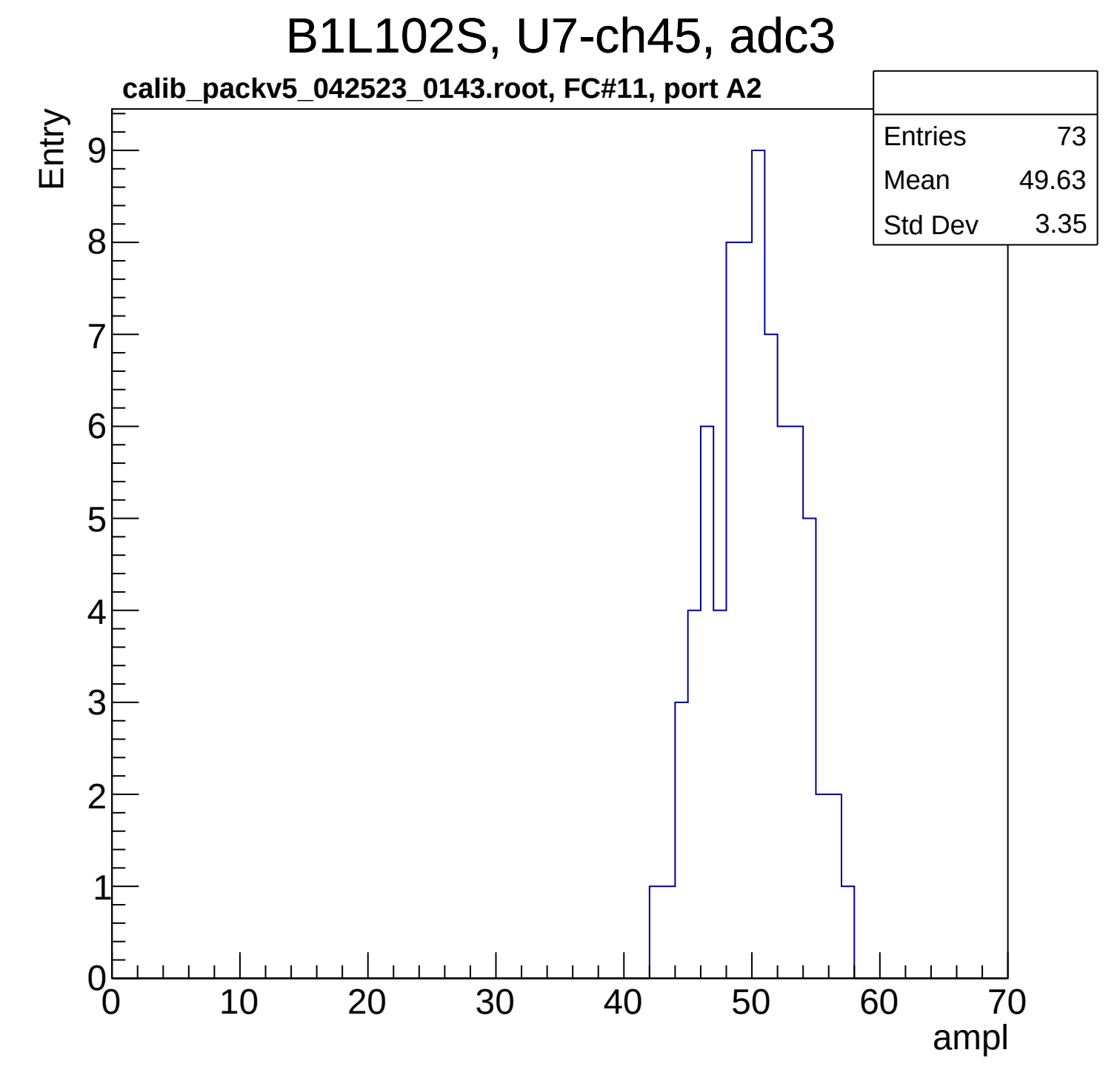
B1L102S, U7-ch45, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 73
Mean 49.63
Std Dev 3.35
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
30
40
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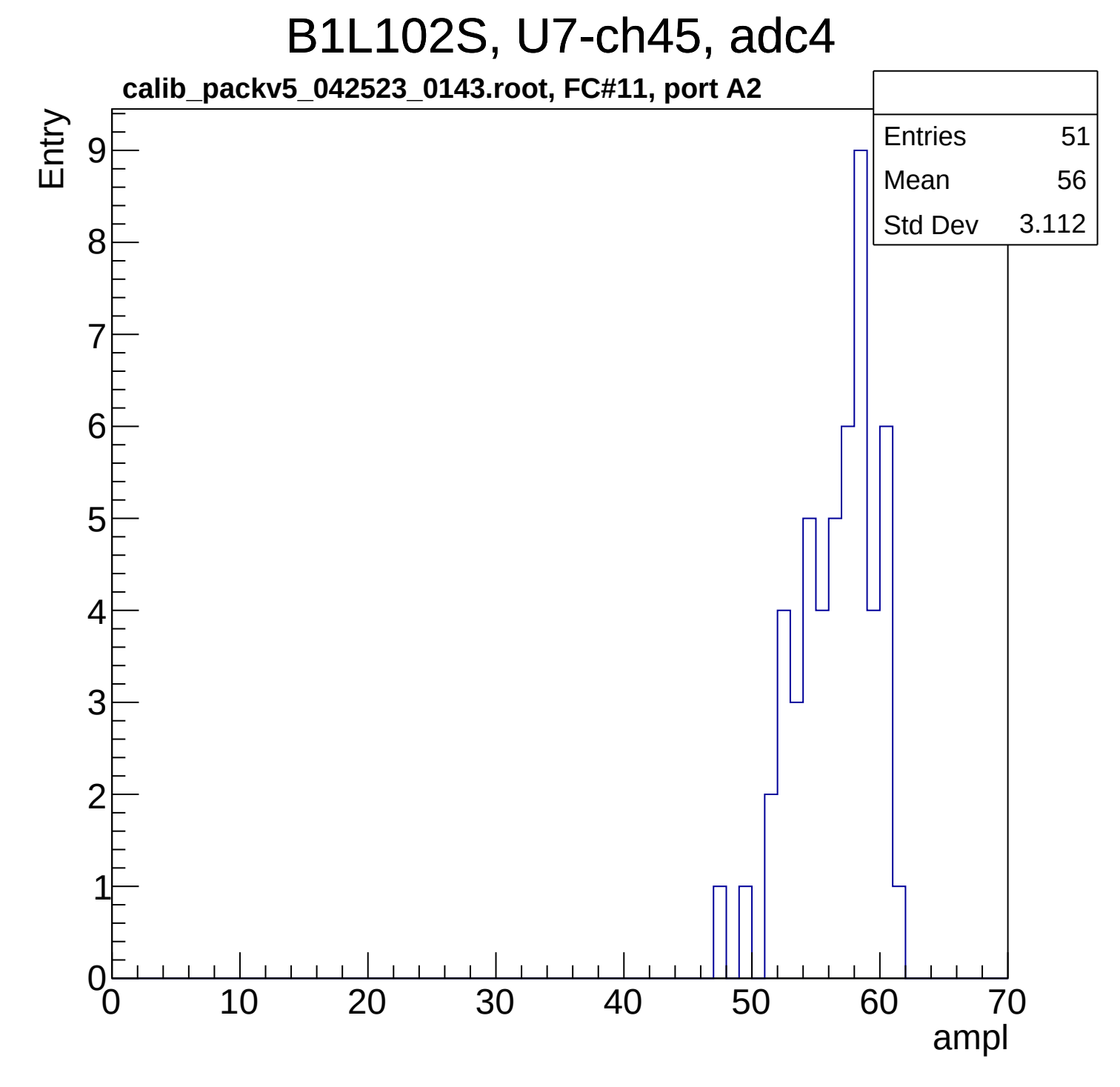
60
70


B1L102S, U7-ch45, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 51
Mean 56
Std Dev 3.112
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
50
60
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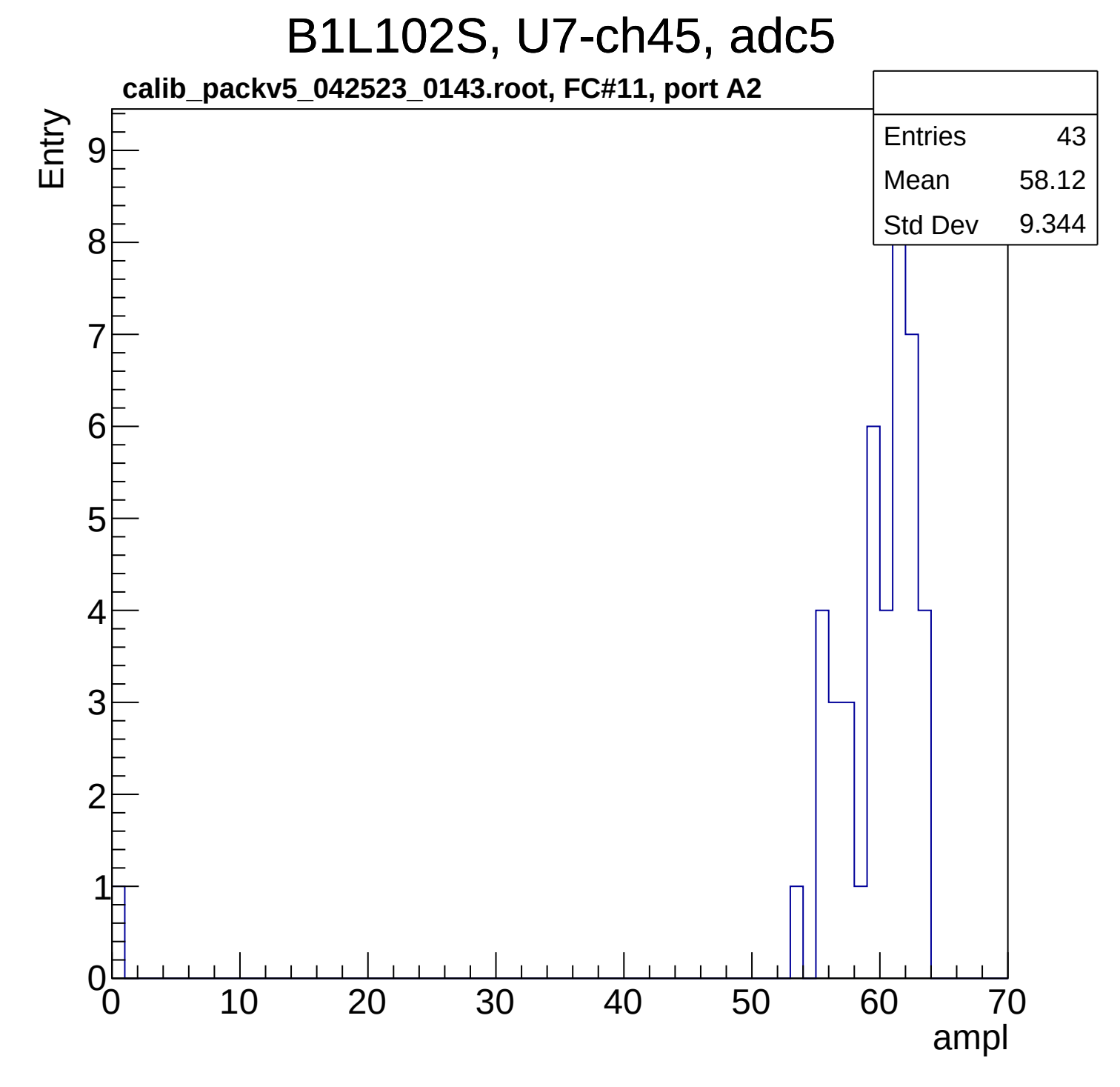
B1L102S, U7-ch45, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 43
Mean 58.12
Std Dev 9.344
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
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20
30
40
50
60
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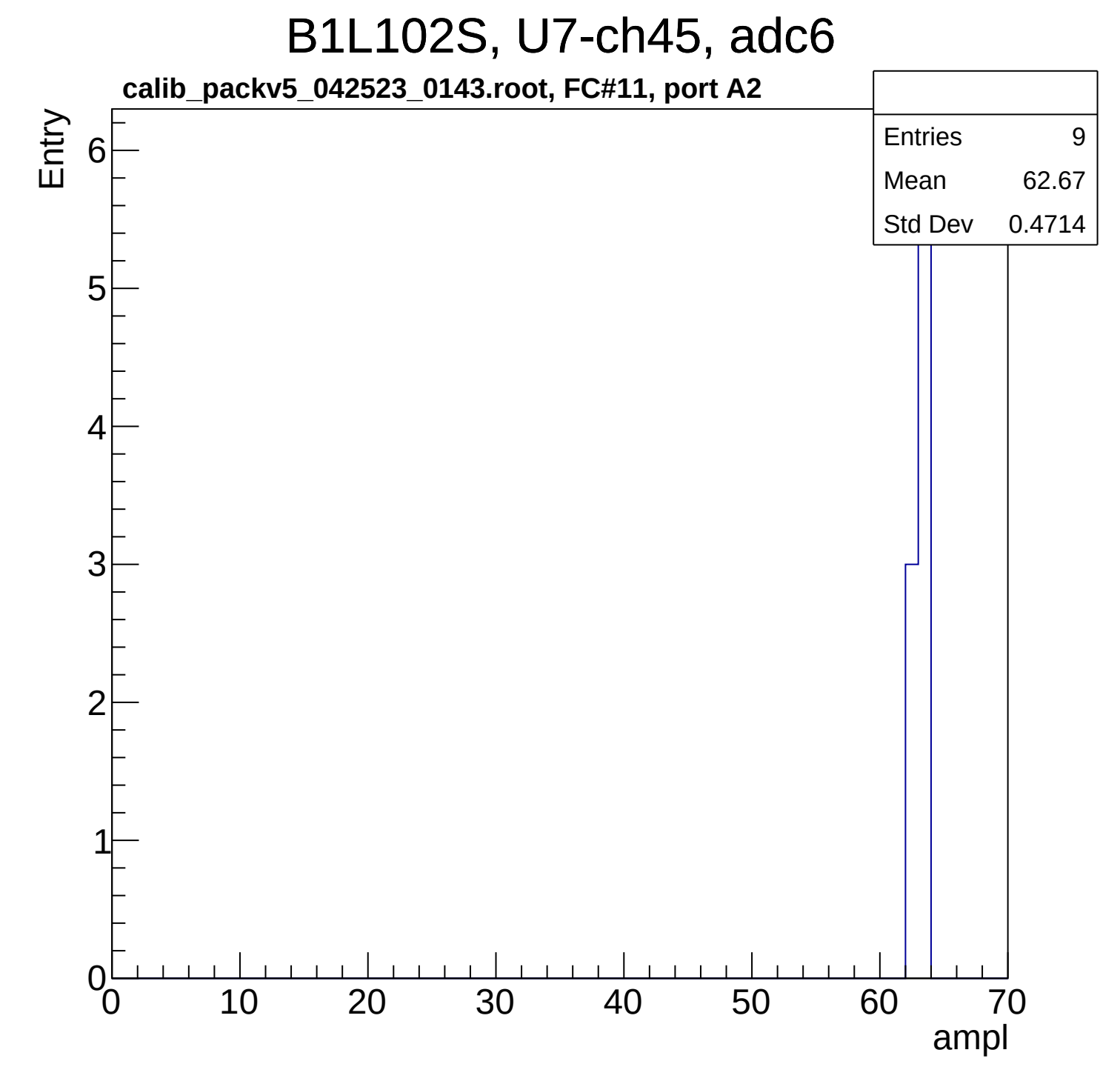
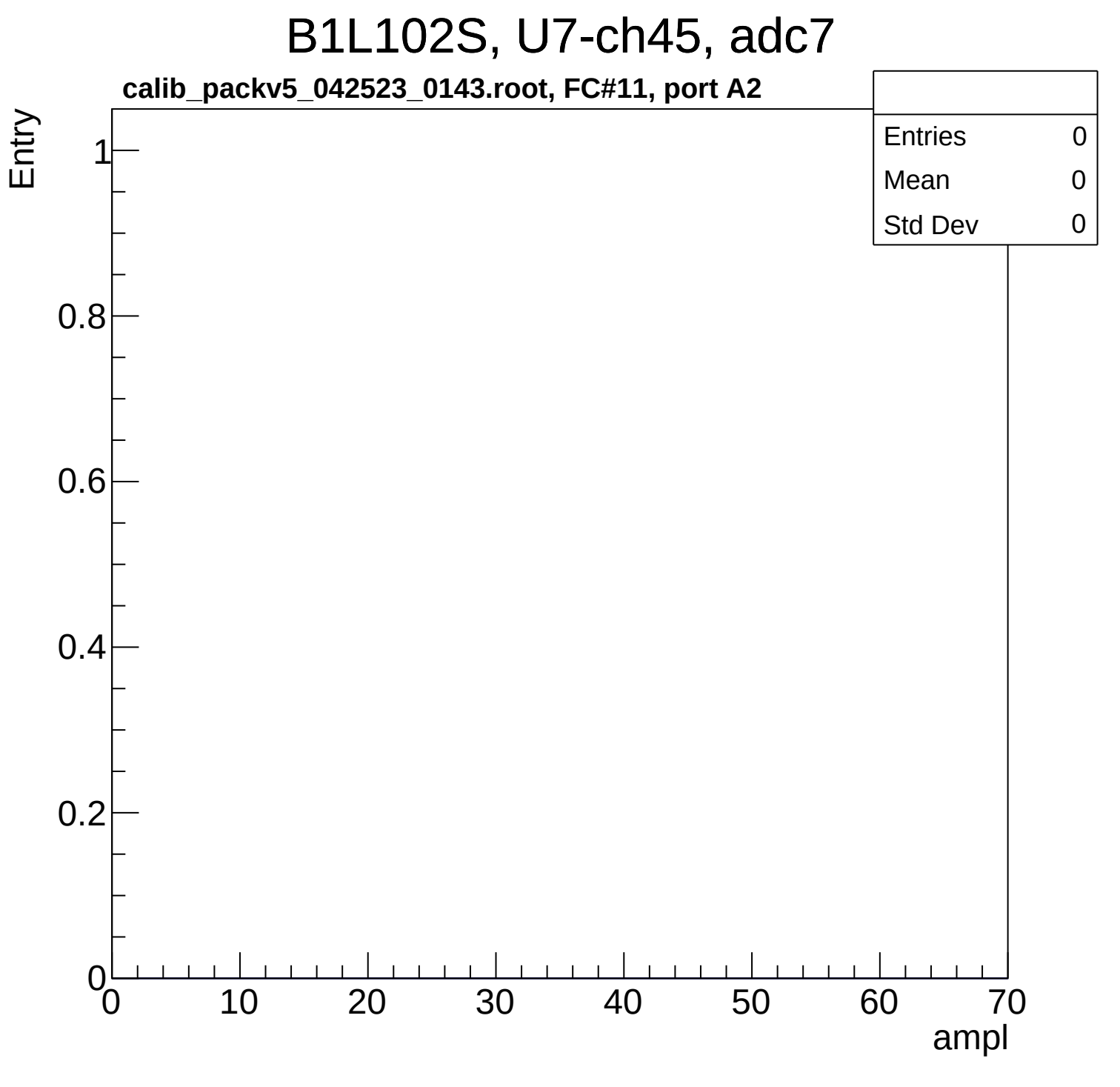
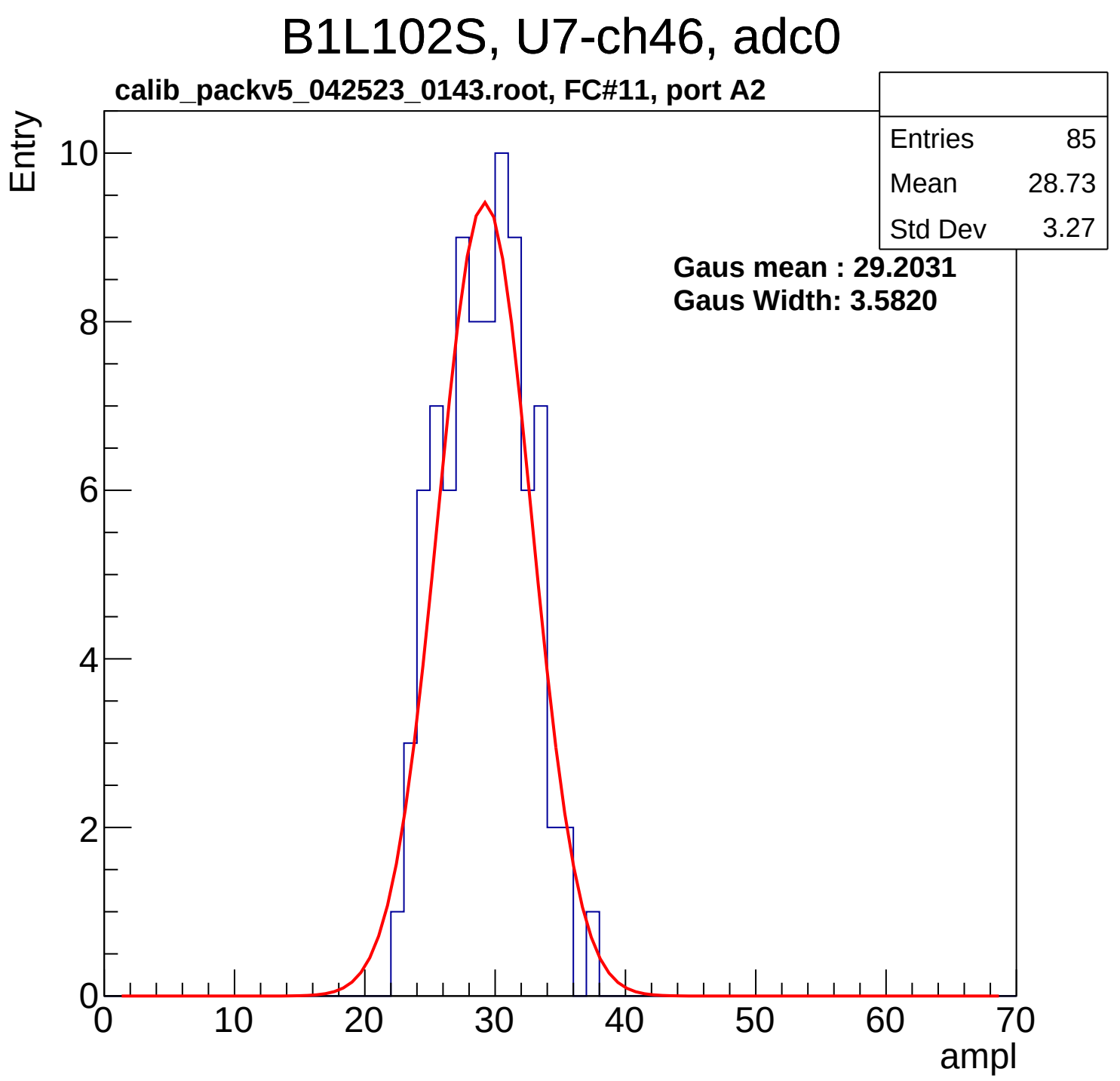
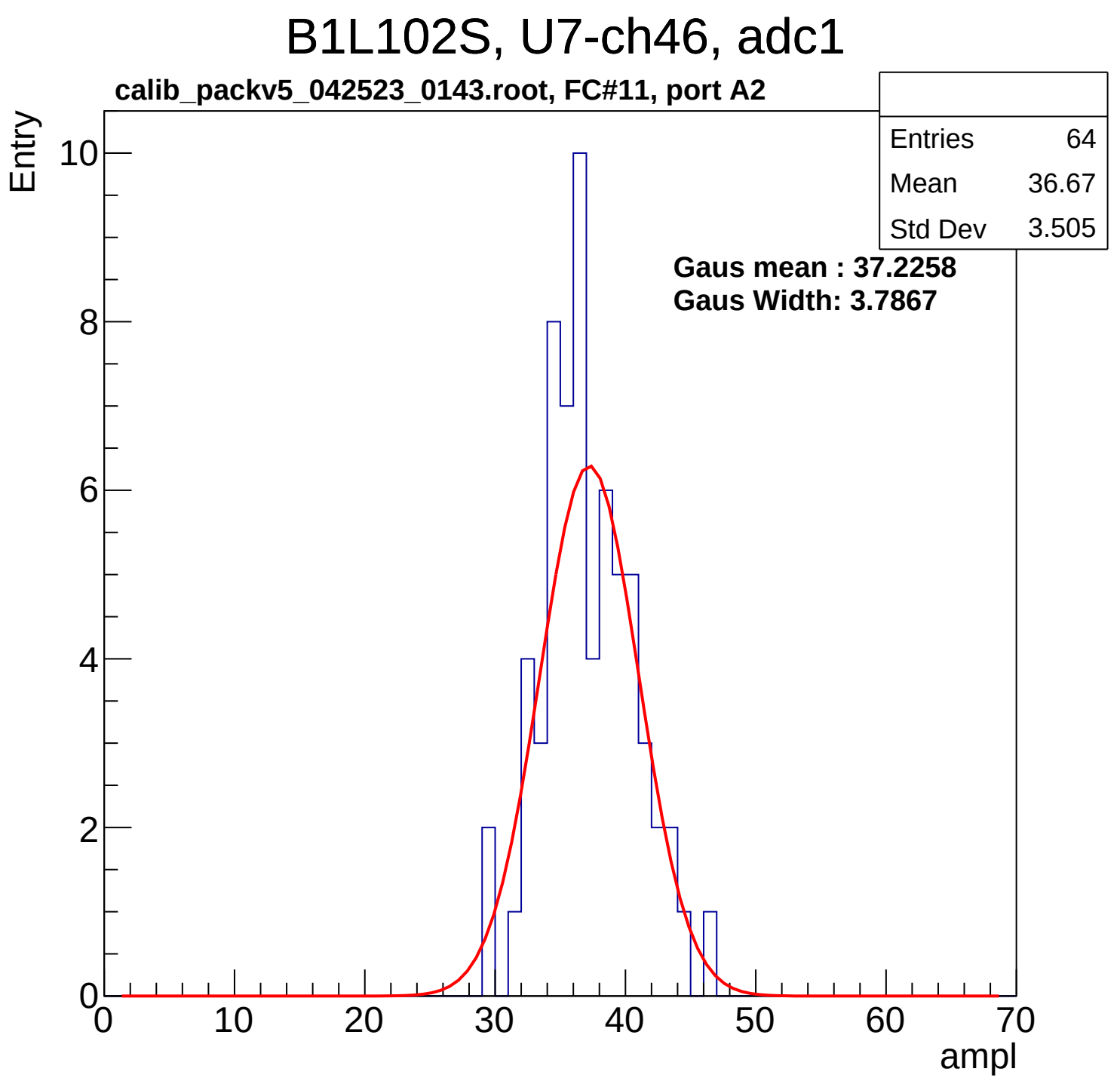
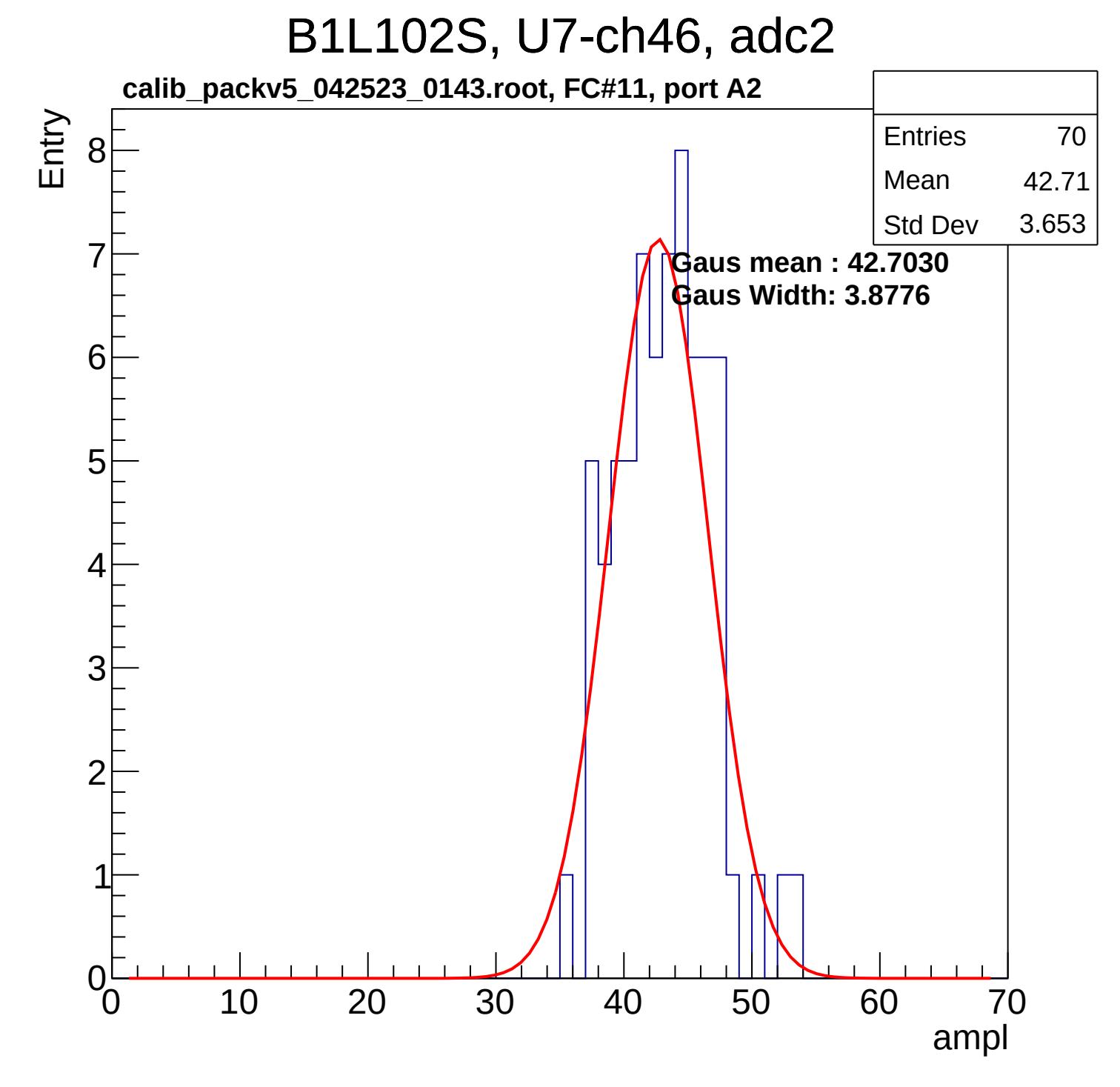

B1L102S, U7-ch45, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 9
Mean 62.67
Std Dev 0.4714
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L102S, U7-ch45, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U7-ch46, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 85
Mean 28.73
Std Dev 3.27
Gaus mean : 29.2031
Gaus Width: 3.5820
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L102S, U7-ch46, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 64
Mean 36.67
Std Dev 3.505
Gaus mean : 37.2258
Gaus Width: 3.7867
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L102S, U7-ch46, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 70
Mean 42.71
Std Dev 3.653
Gaus mean : 42.7030
Gaus Width: 3.8776
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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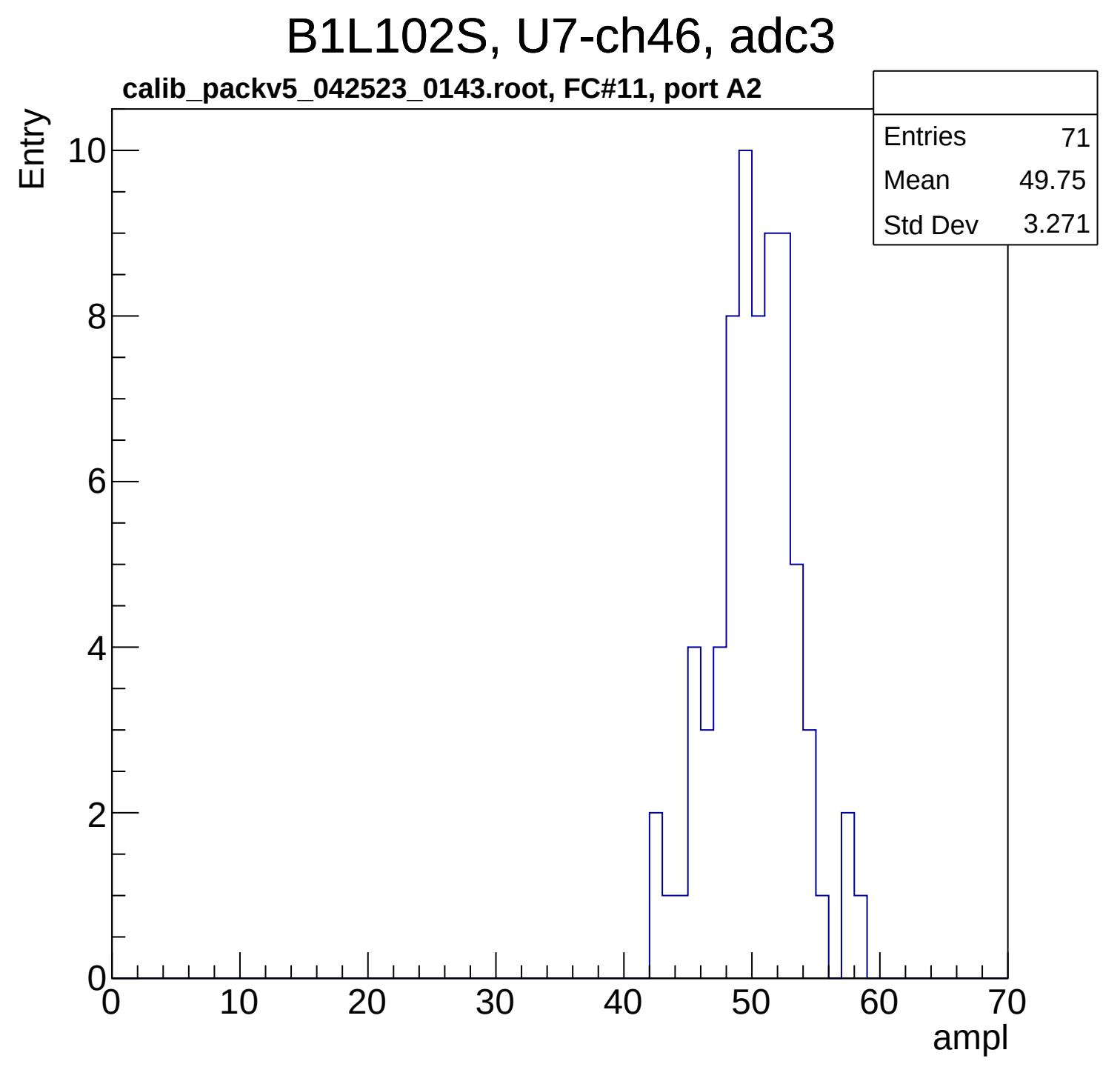
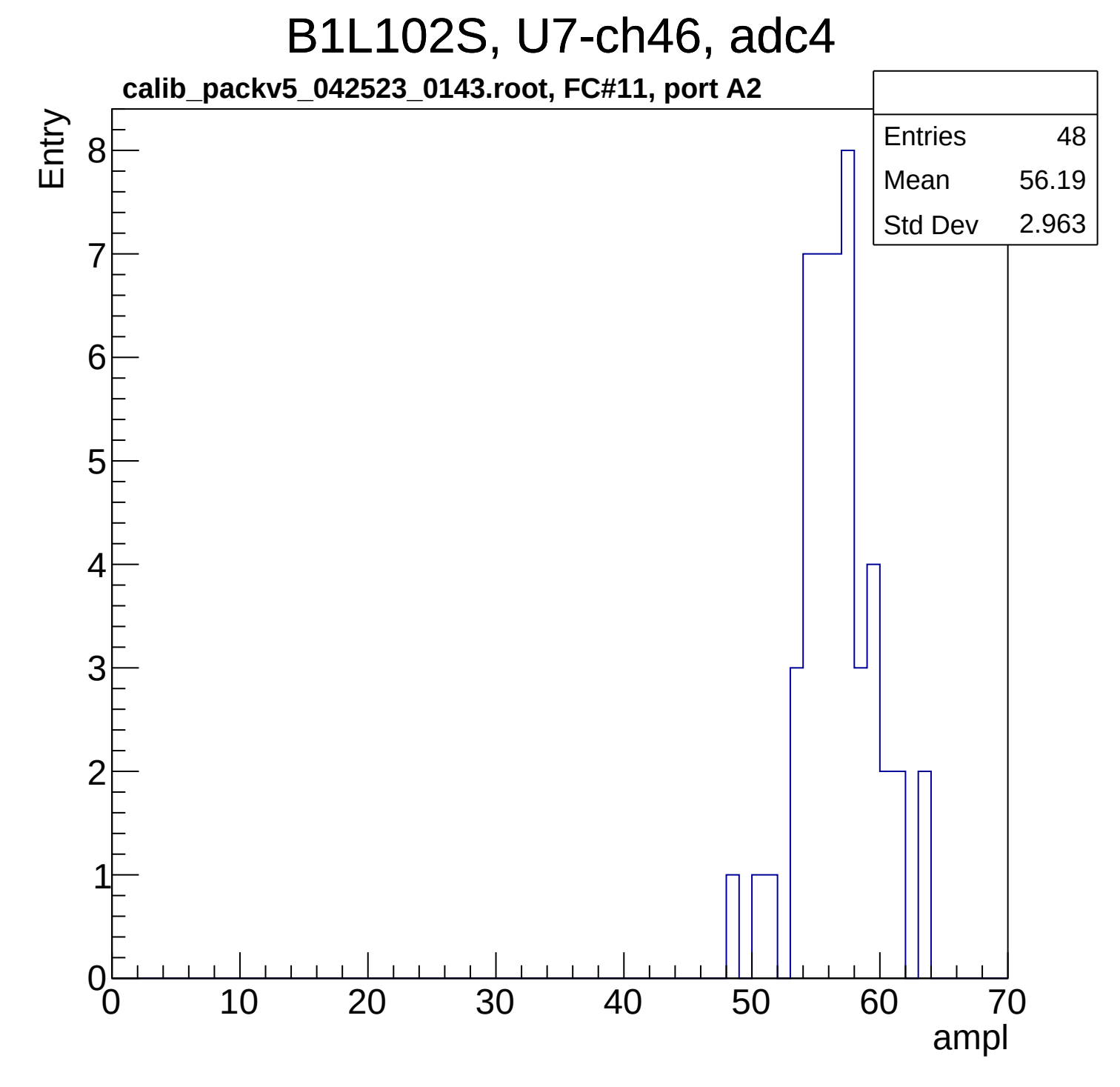
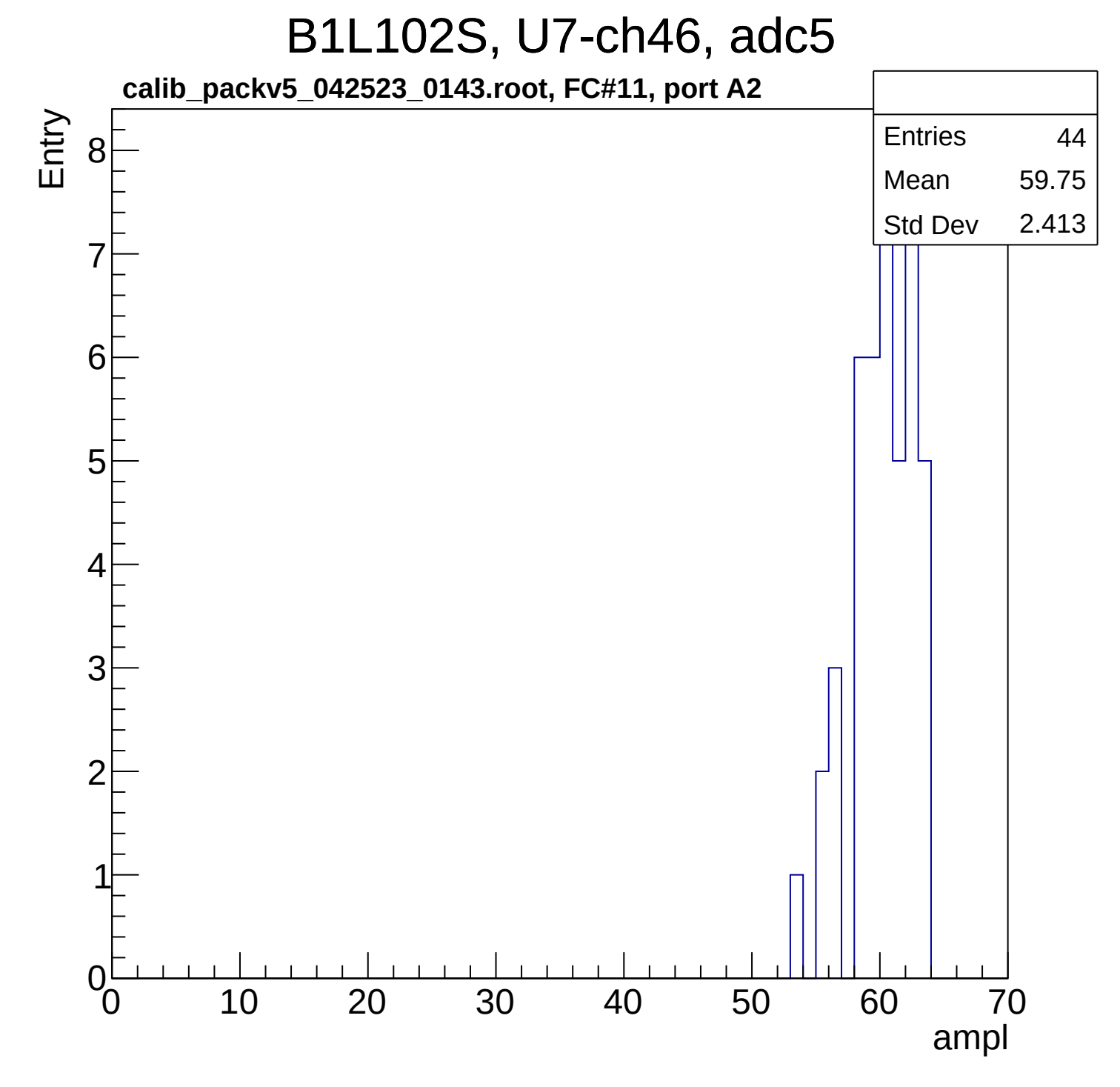
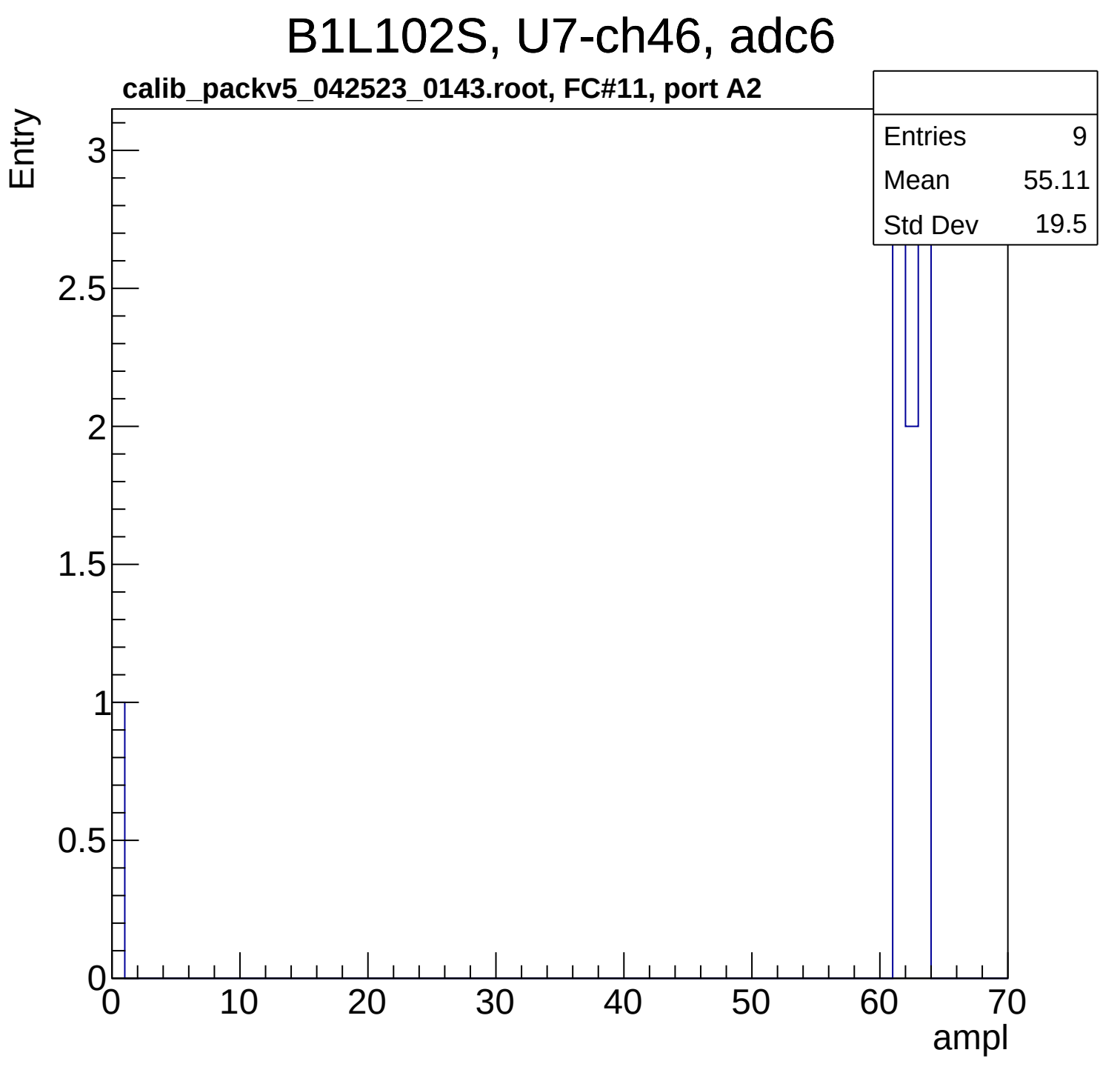
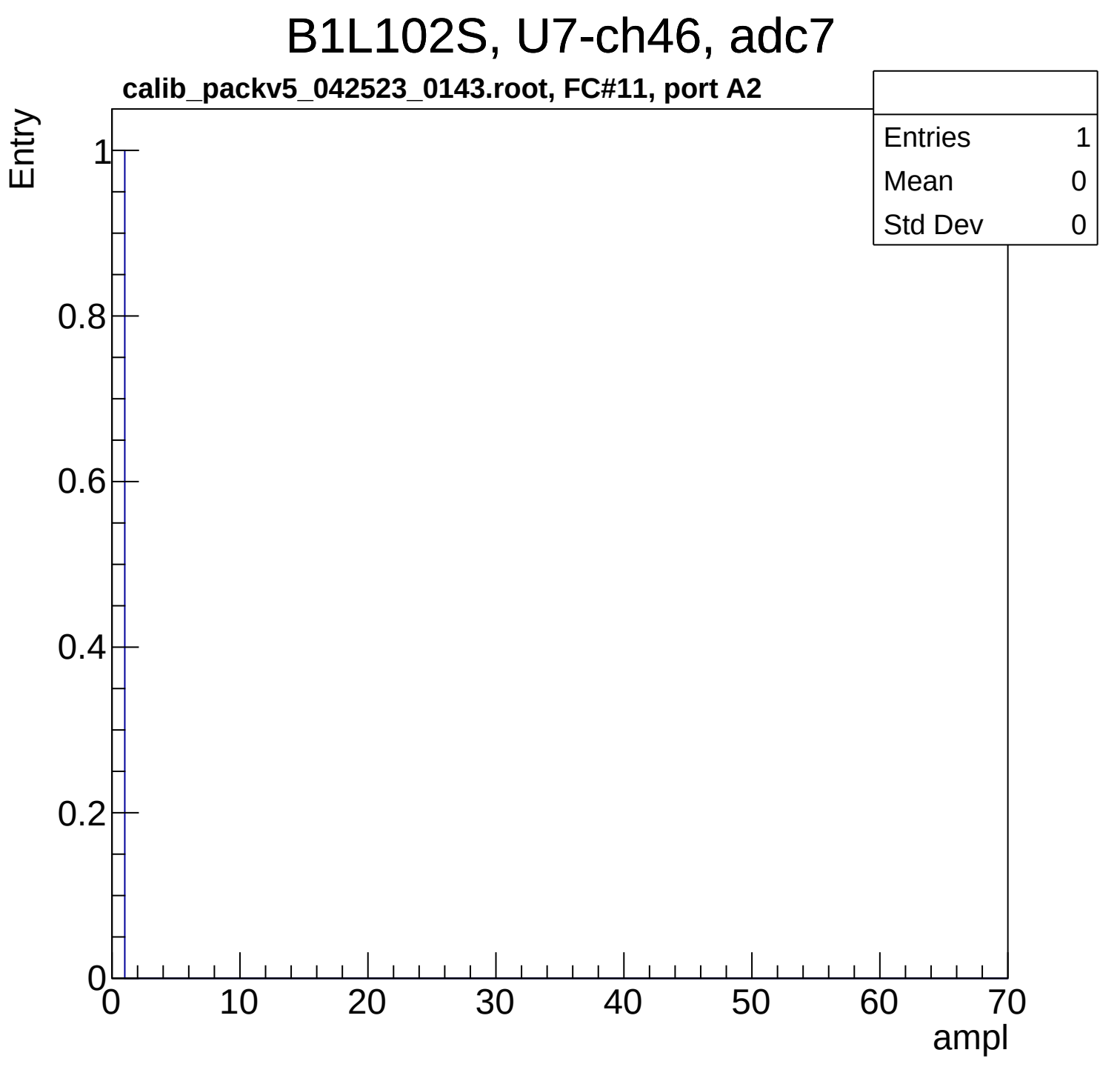
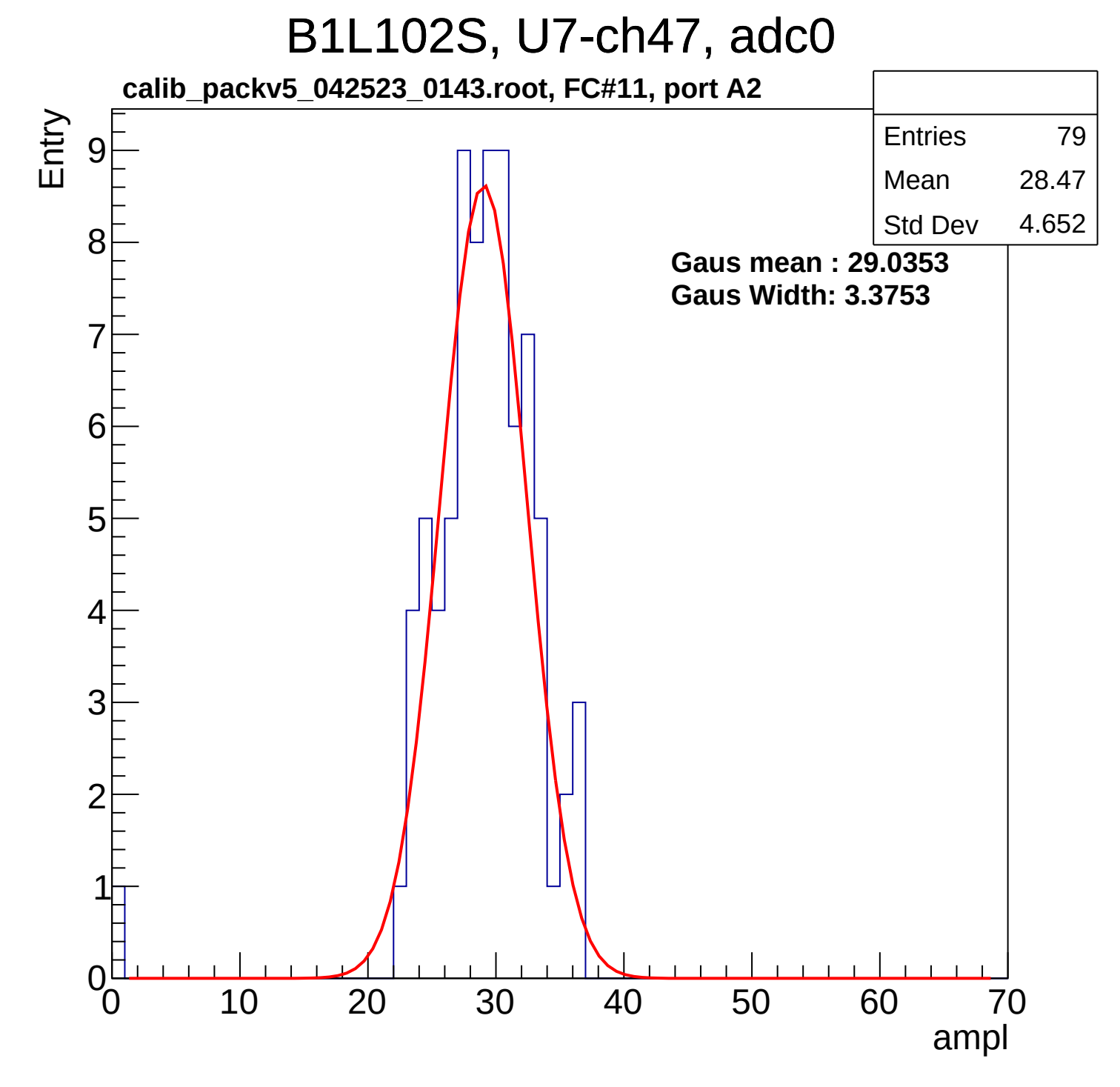

B1L102S, U7-ch46, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 71
Mean 49.75
Std Dev 3.271
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

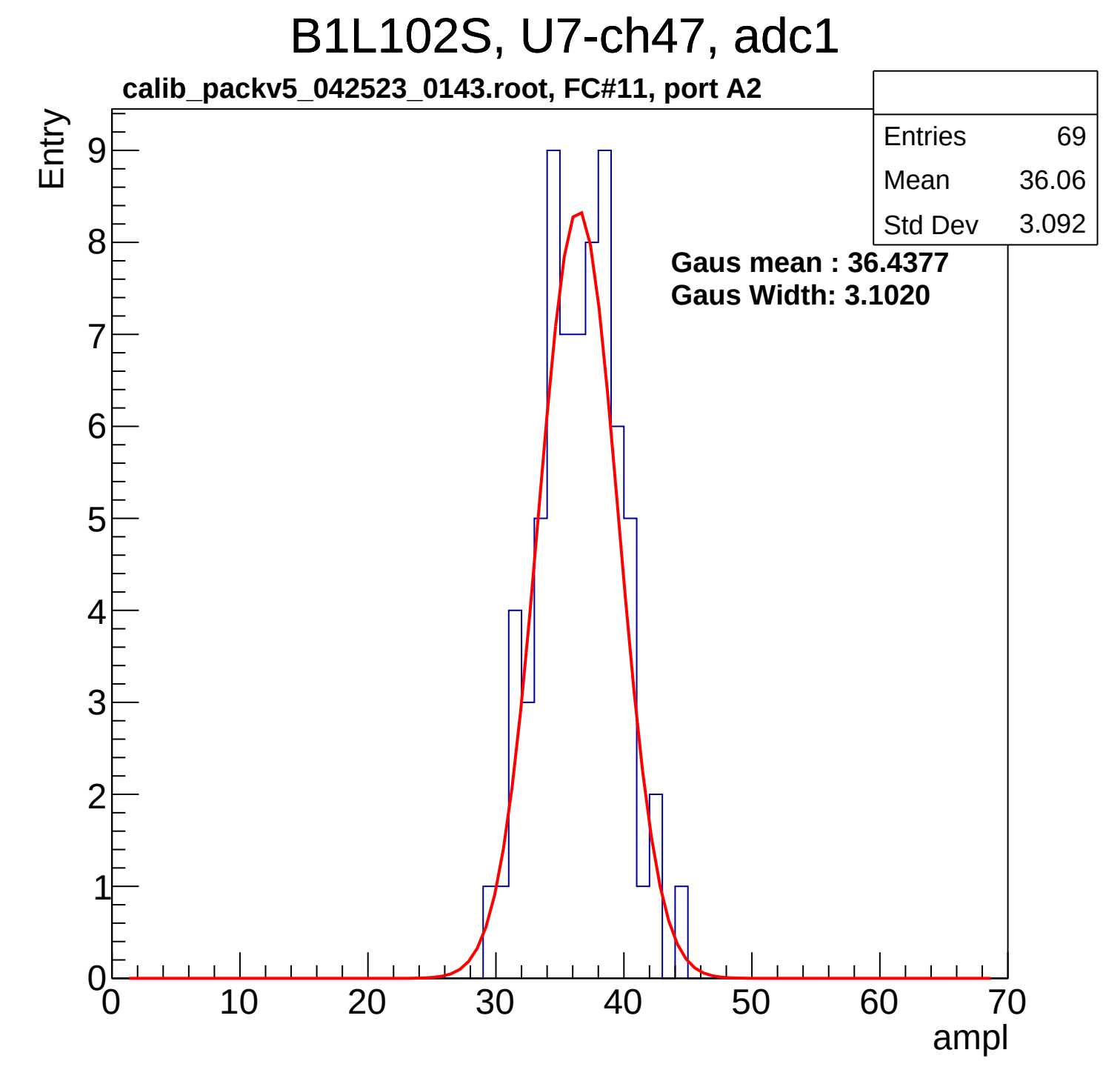

B1L102S, U7-ch46, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 48
Mean 56.19
Std Dev 2.963
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

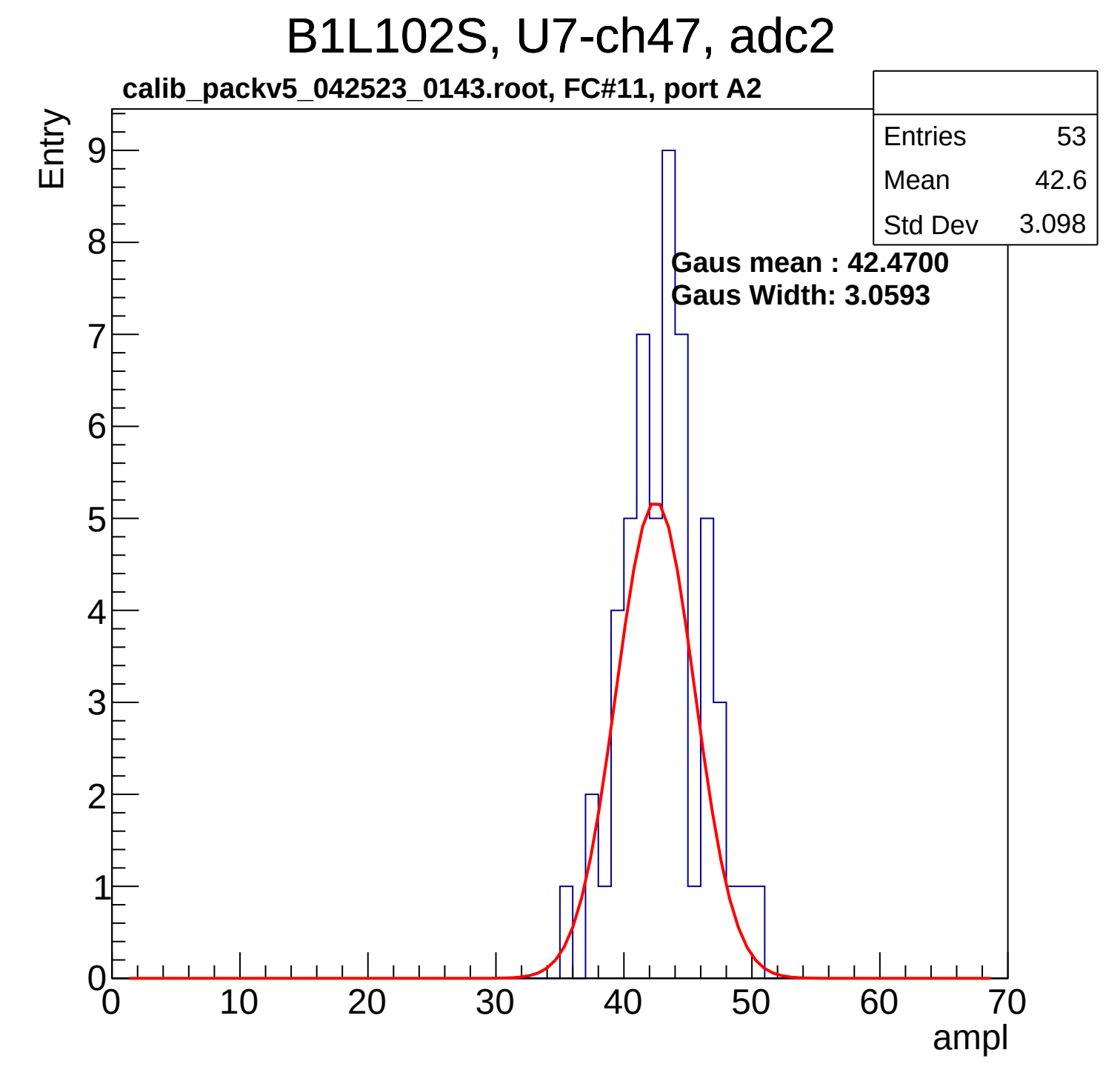

B1L102S, U7-ch46, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 44
Mean 59.75
Std Dev 2.413
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

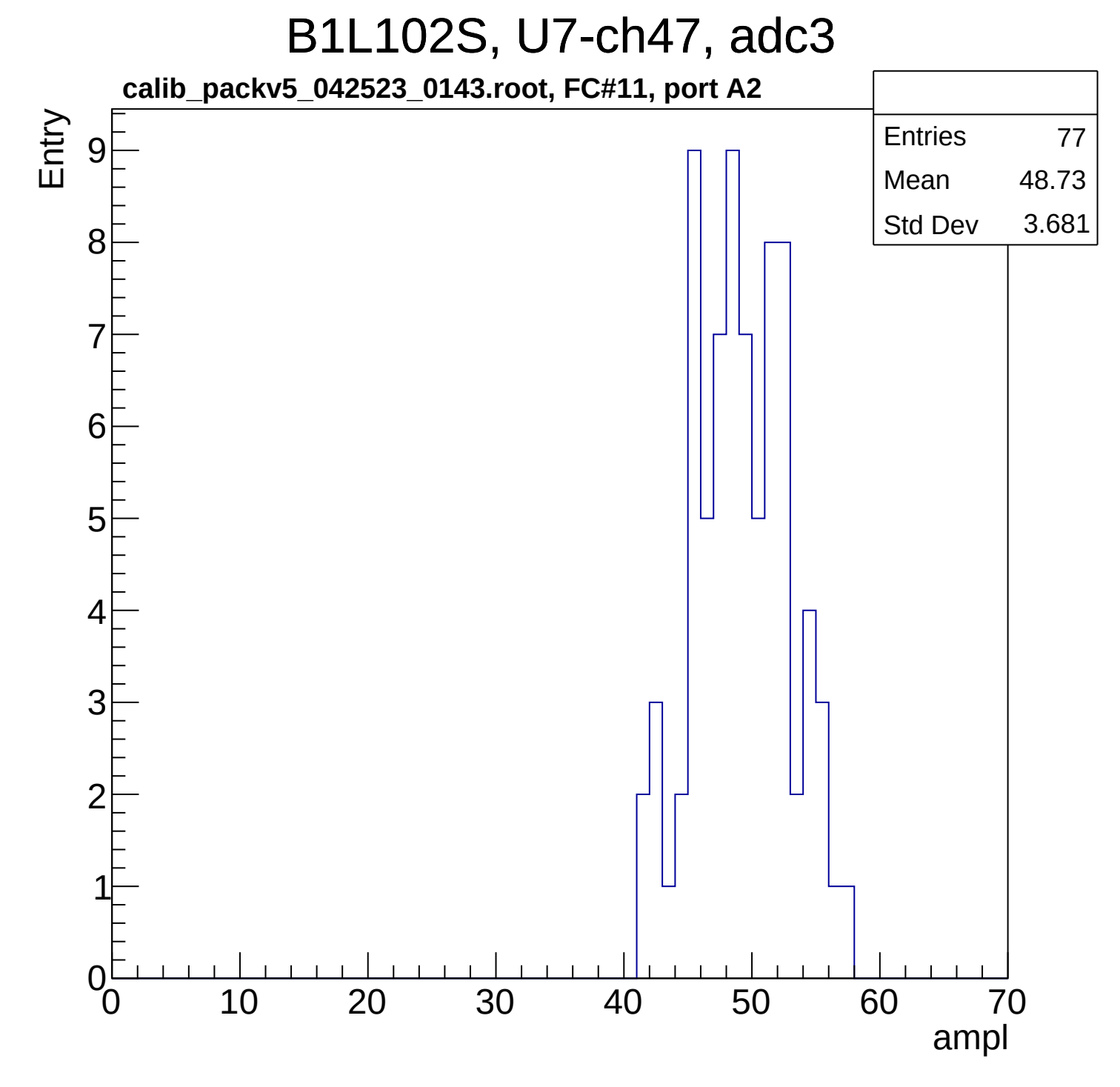

B1L102S, U7-ch46, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 9
Mean 55.11
Std Dev 19.5
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

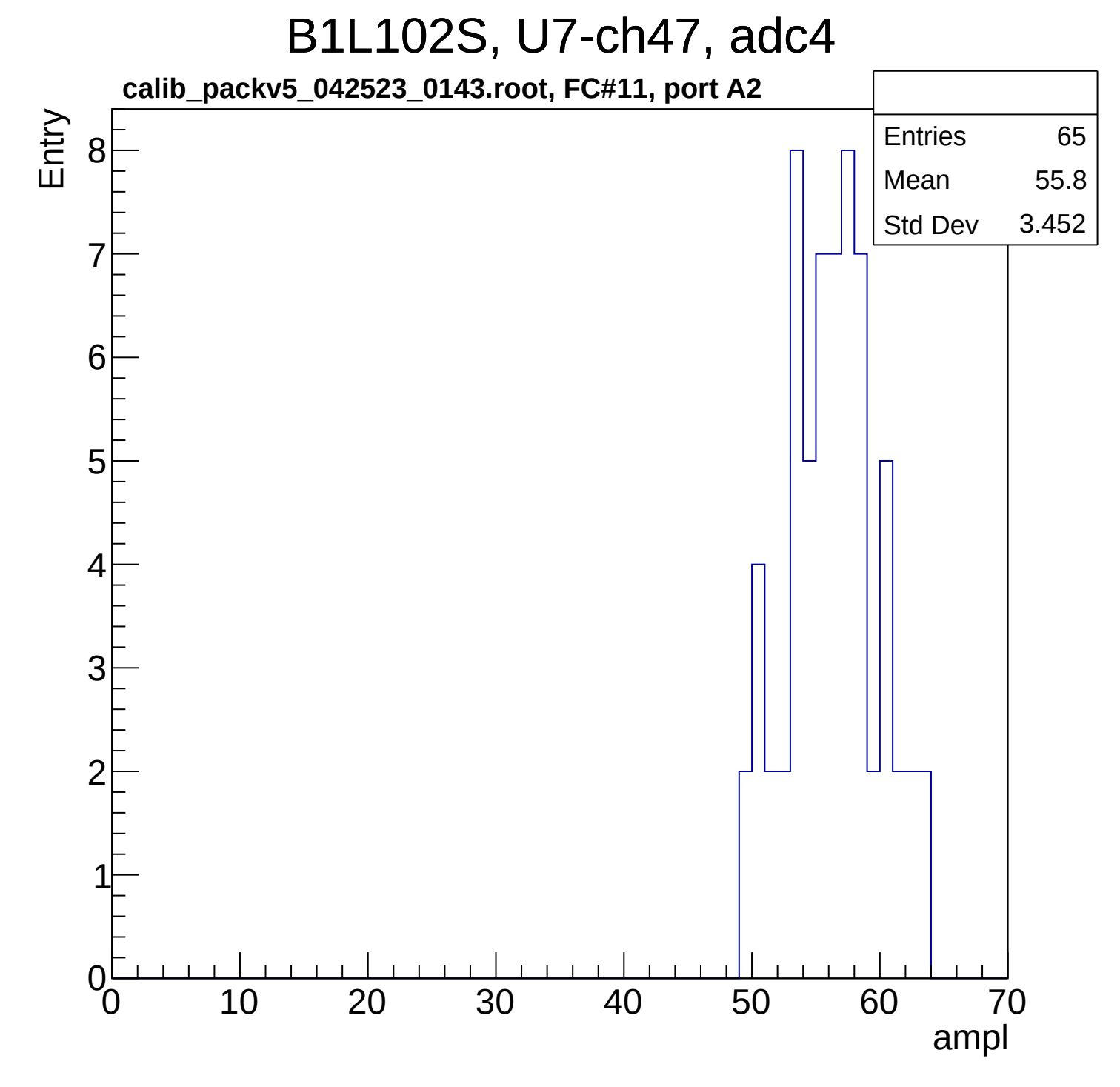

B1L102S, U7-ch46, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

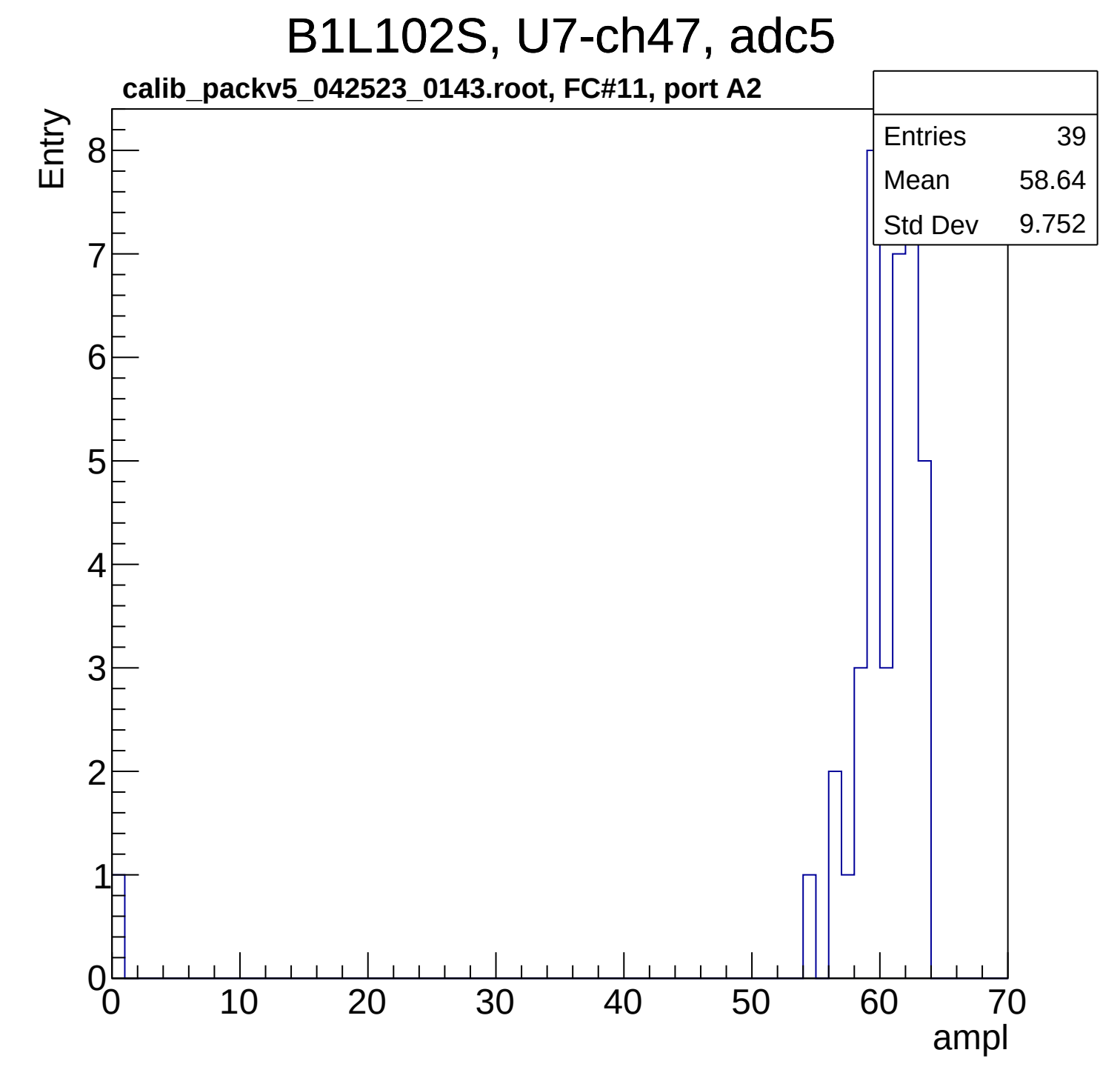

B1L102S, U7-ch47, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 79
Mean 28.47
Std Dev 4.652
Gaus mean : 29.0353
Gaus Width: 3.3753
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

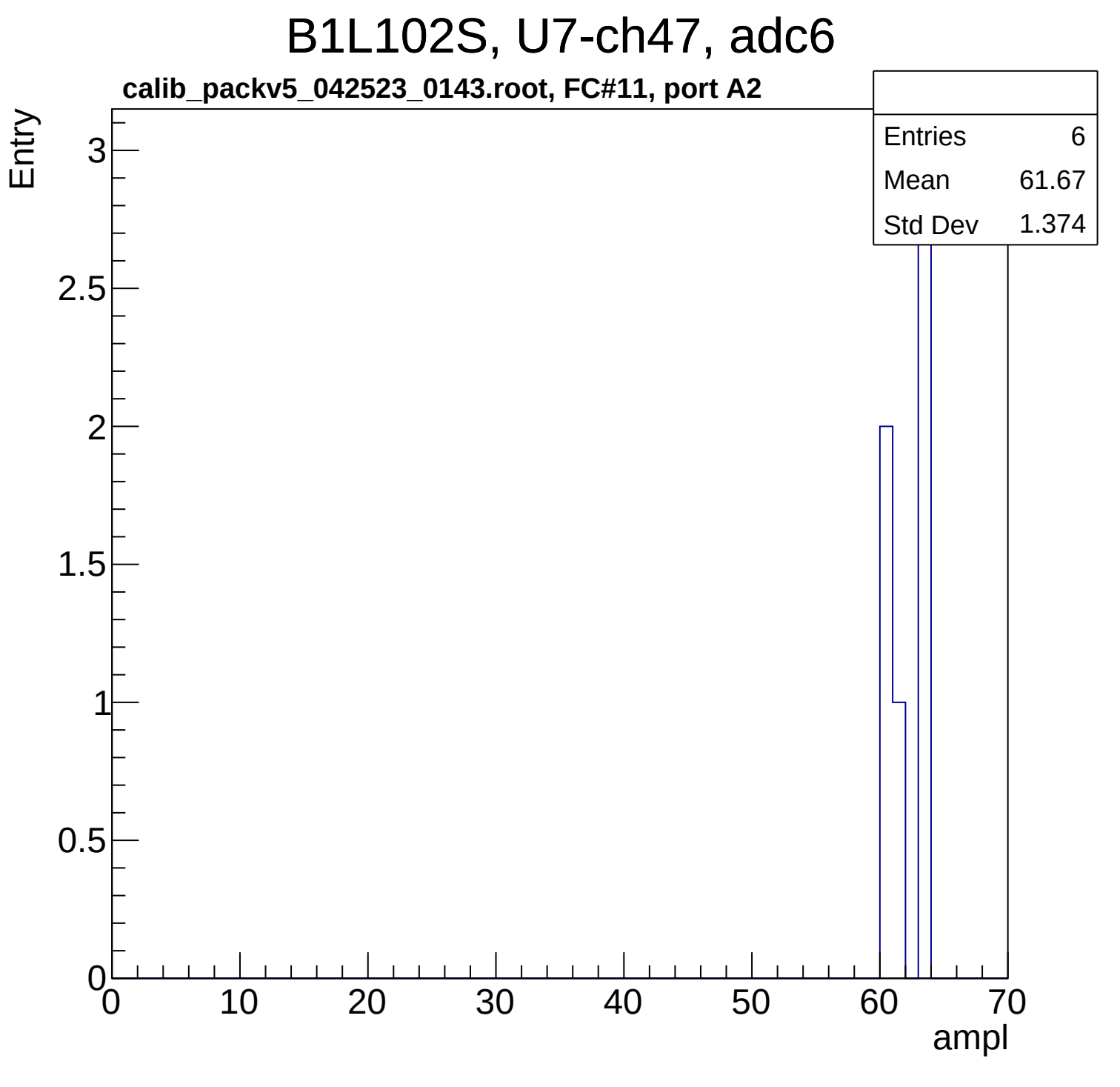

B1L102S, U7-ch47, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 69
Mean 36.06
Std Dev 3.092
Gaus mean : 36.4377
Gaus Width: 3.1020
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

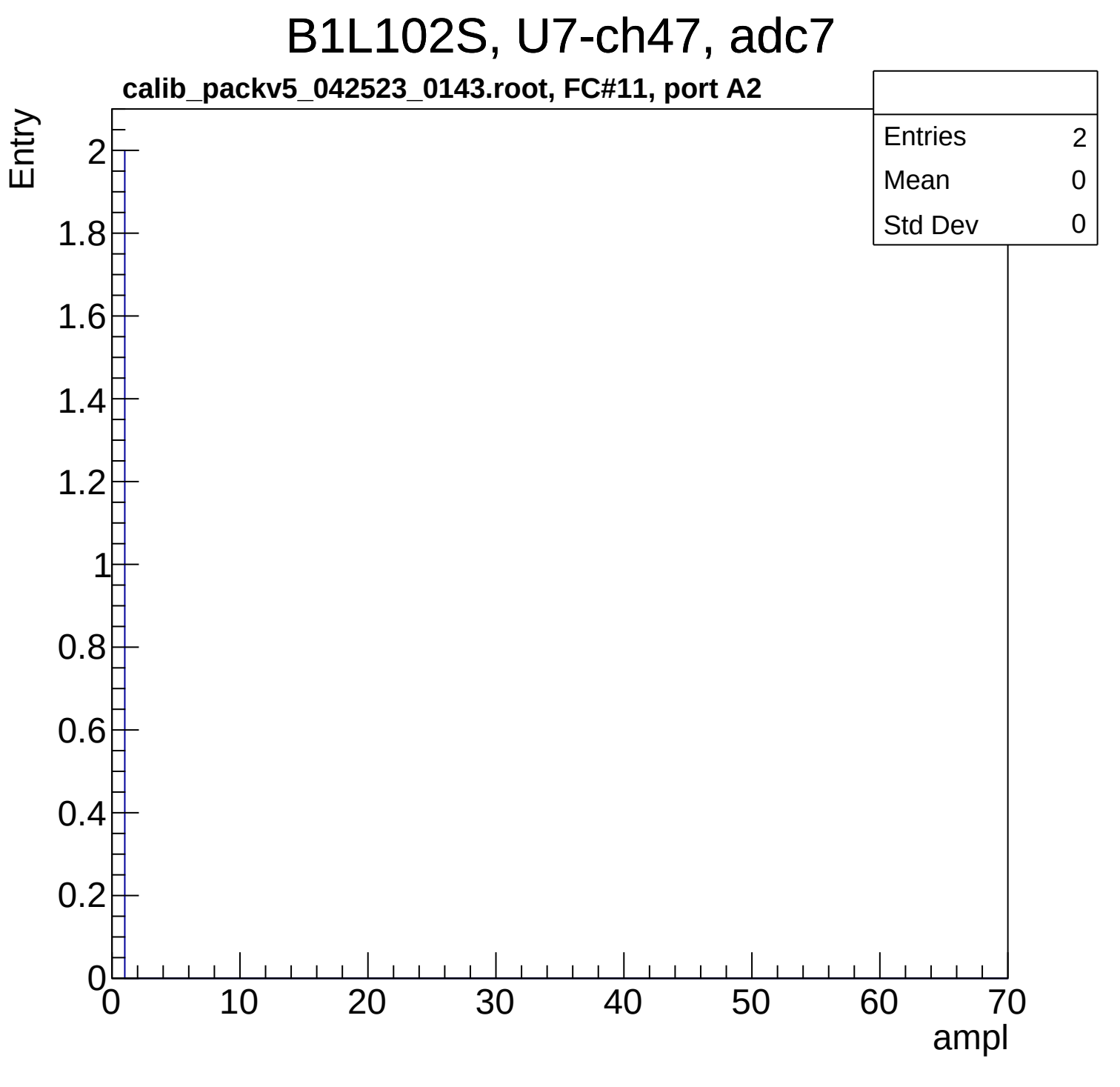

B1L102S, U7-ch47, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 53
Mean 42.6
Std Dev 3.098
Gaus mean : 42.4700
Gaus Width: 3.0593
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

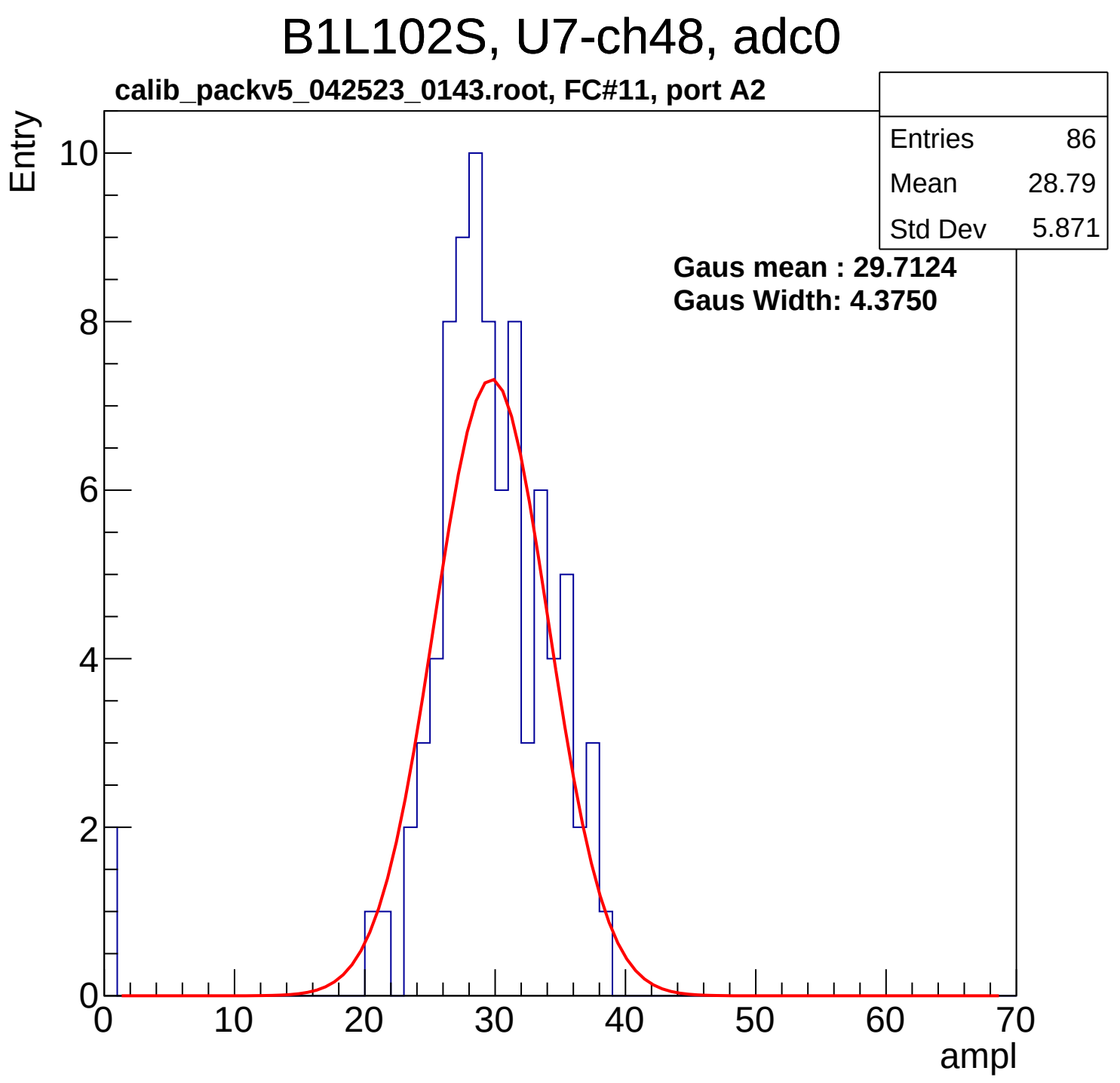

B1L102S, U7-ch47, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 77
Mean 48.73
Std Dev 3.681
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

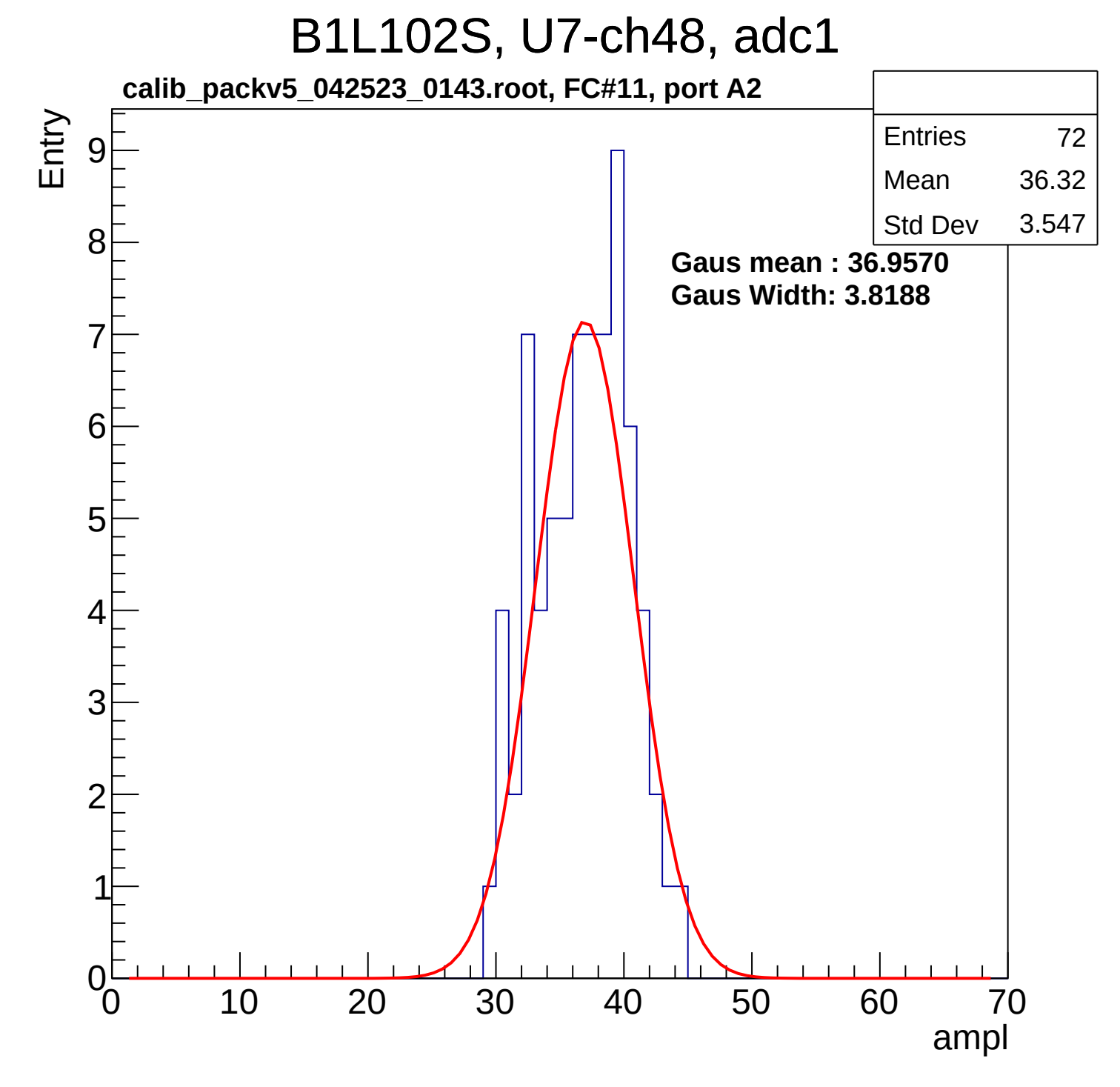

B1L102S, U7-ch47, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 65
Mean 55.8
Std Dev 3.452
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

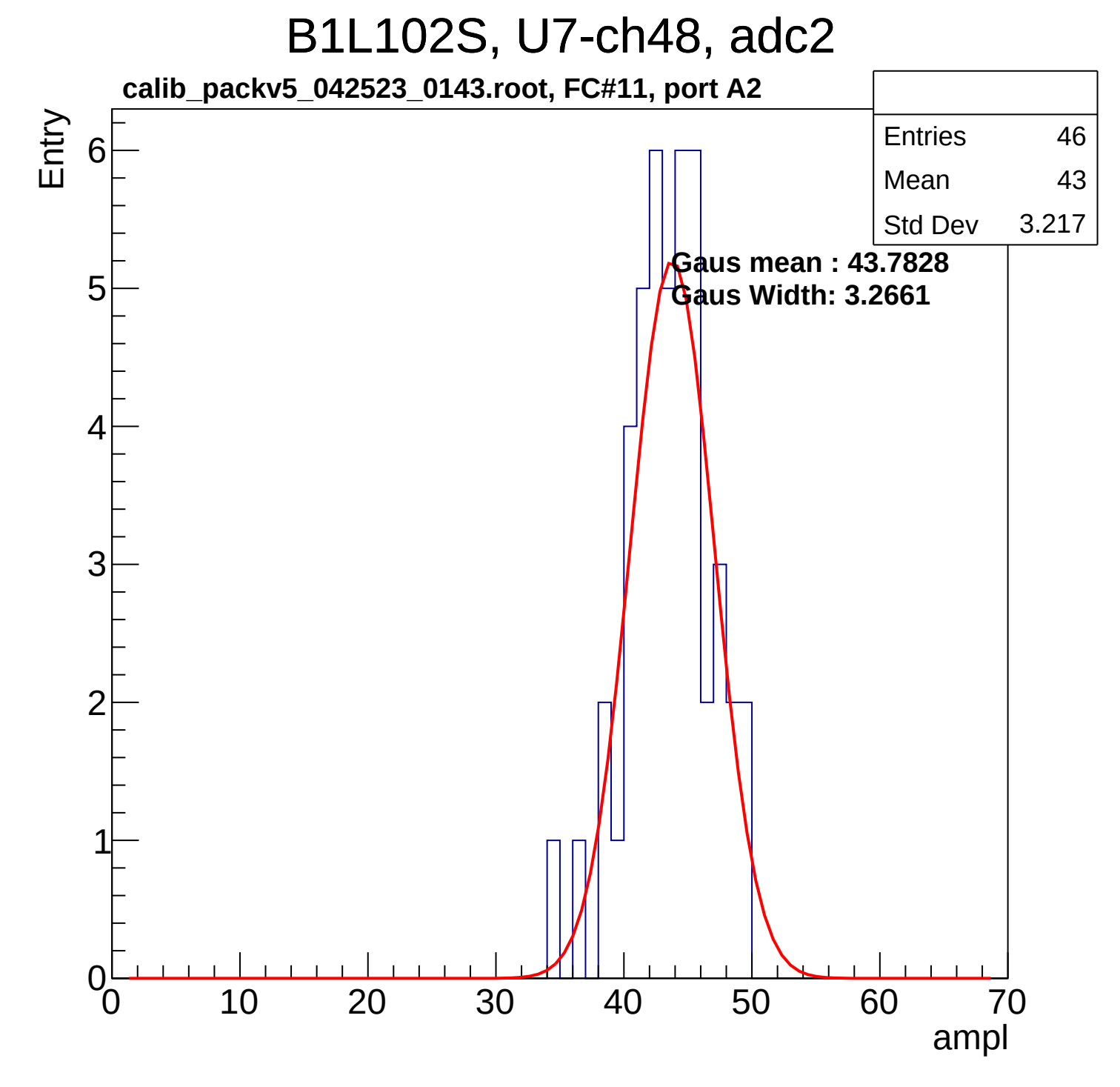

B1L102S, U7-ch47, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 39
Mean 58.64
Std Dev 9.752
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

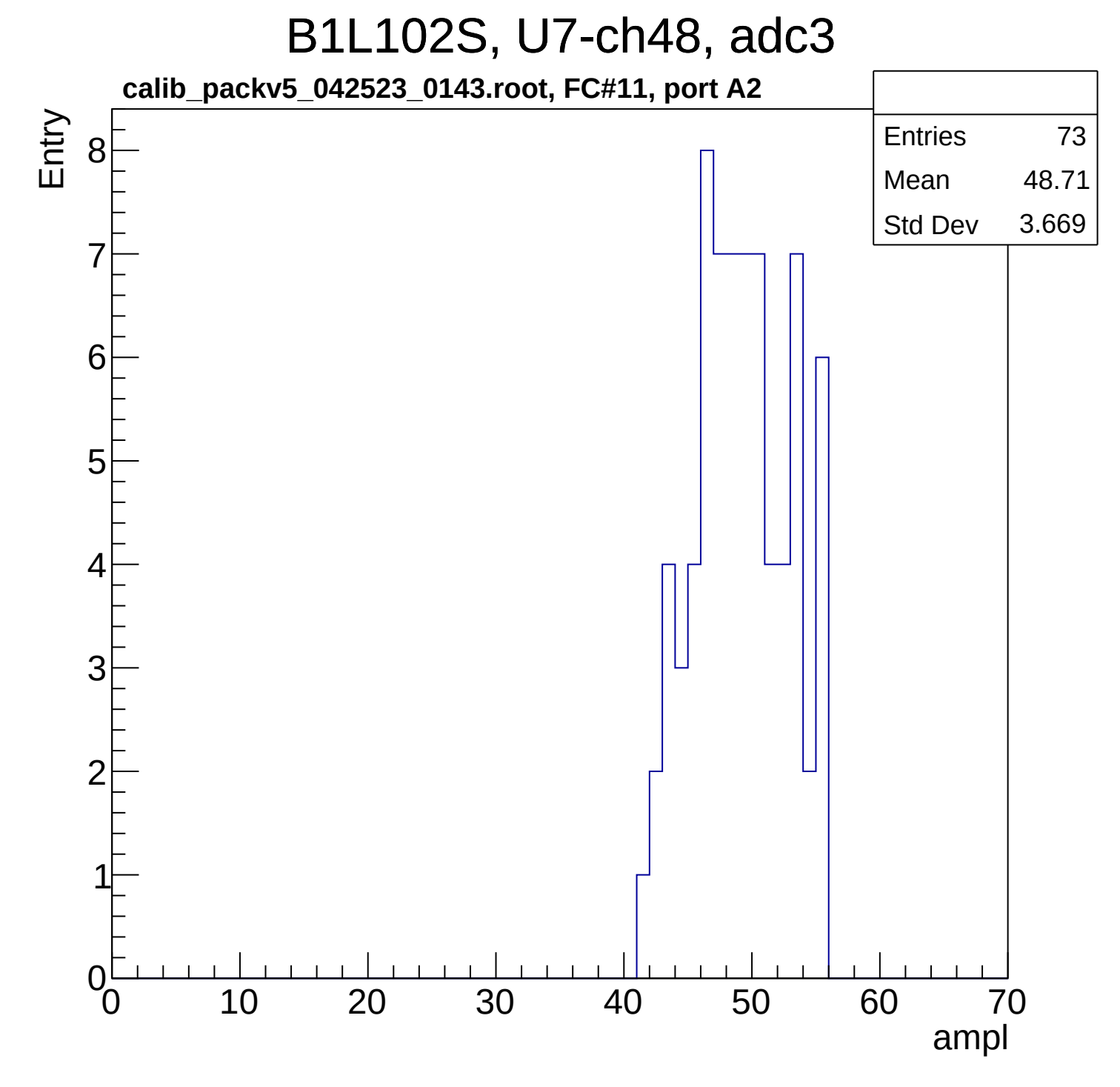

B1L102S, U7-ch47, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 6
Mean 61.67
Std Dev 1.374
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L102S, U7-ch47, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 2
Mean 0
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L102S, U7-ch48, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 86
Mean 28.79
Std Dev 5.871
Gaus mean : 29.7124
Gaus Width: 4.3750
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L102S, U7-ch48, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 72
Mean 36.32
Std Dev 3.547
Gaus mean : 36.9570
Gaus Width: 3.8188
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L102S, U7-ch48, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 46
Mean 43
Std Dev 3.217
Gaus mean : 43.7828
Gaus Width: 3.2661
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L102S, U7-ch48, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 73
Mean 48.71
Std Dev 3.669
Entry
ampl
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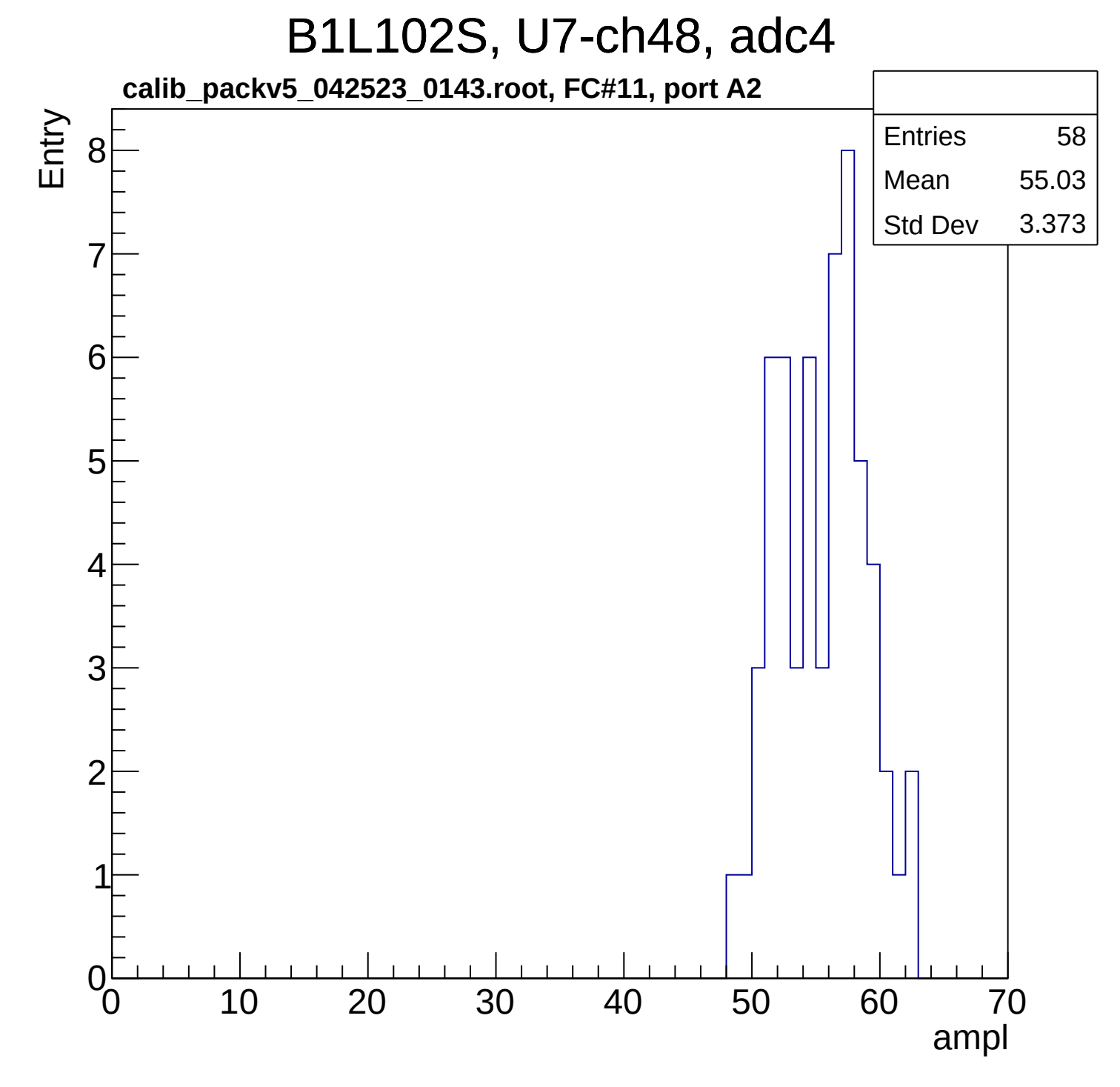
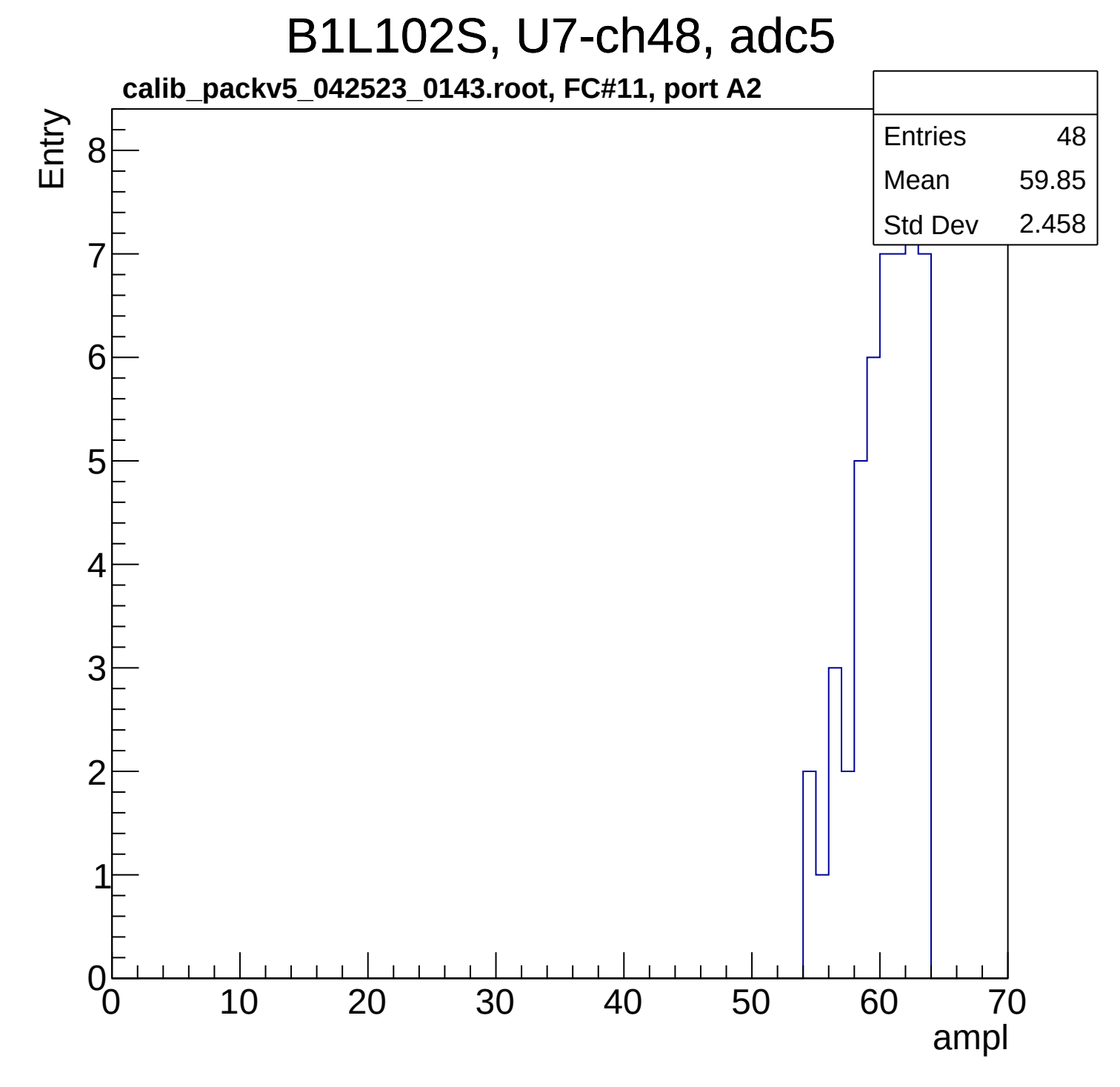
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L102S, U7-ch48, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 58
Mean 55.03
Std Dev 3.373
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L102S, U7-ch48, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 48
Mean 59.85
Std Dev 2.458
Entry
ampl
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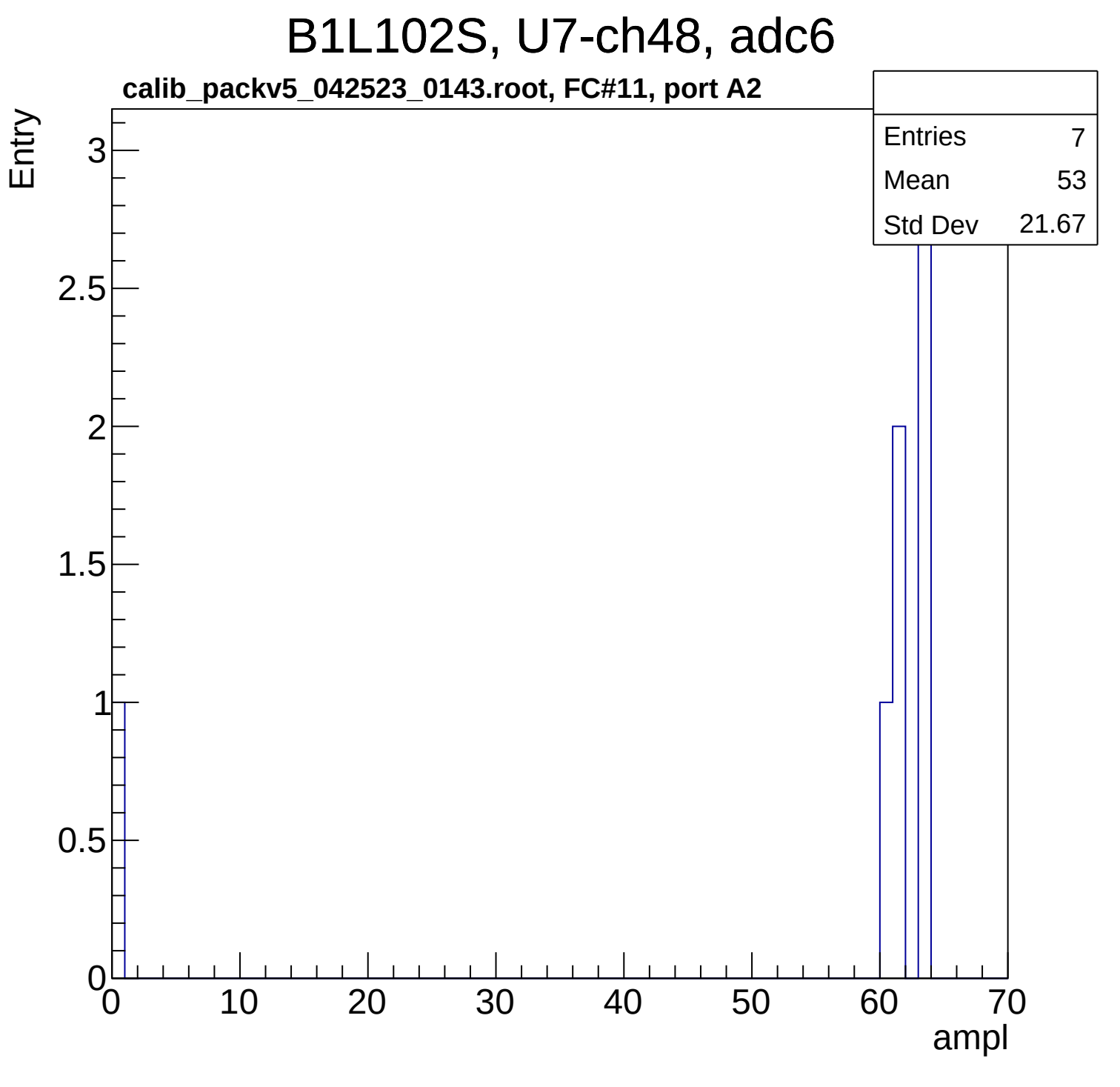
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L102S, U7-ch48, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 7
Mean 53
Std Dev 21.67
Entry
ampl
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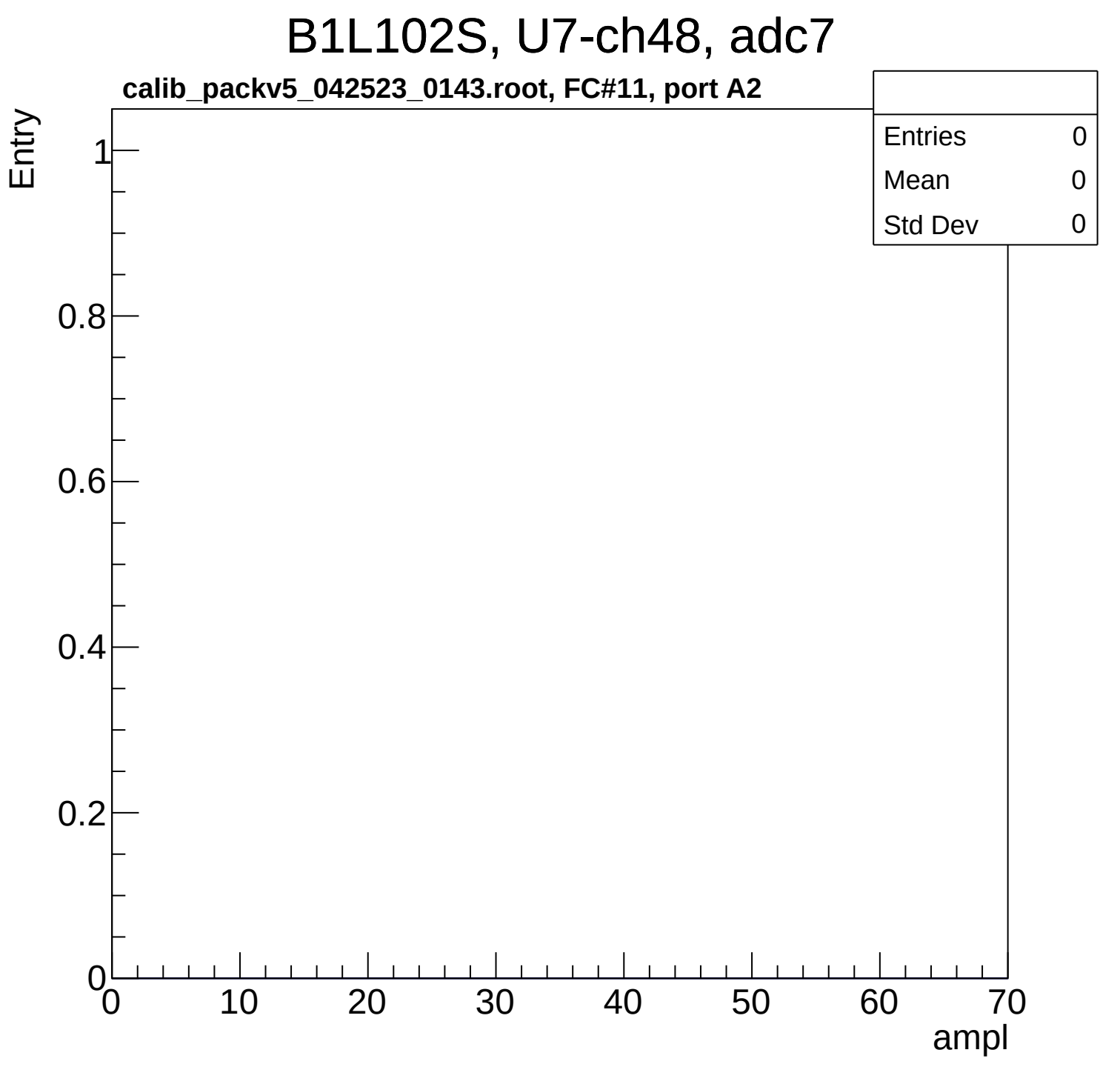
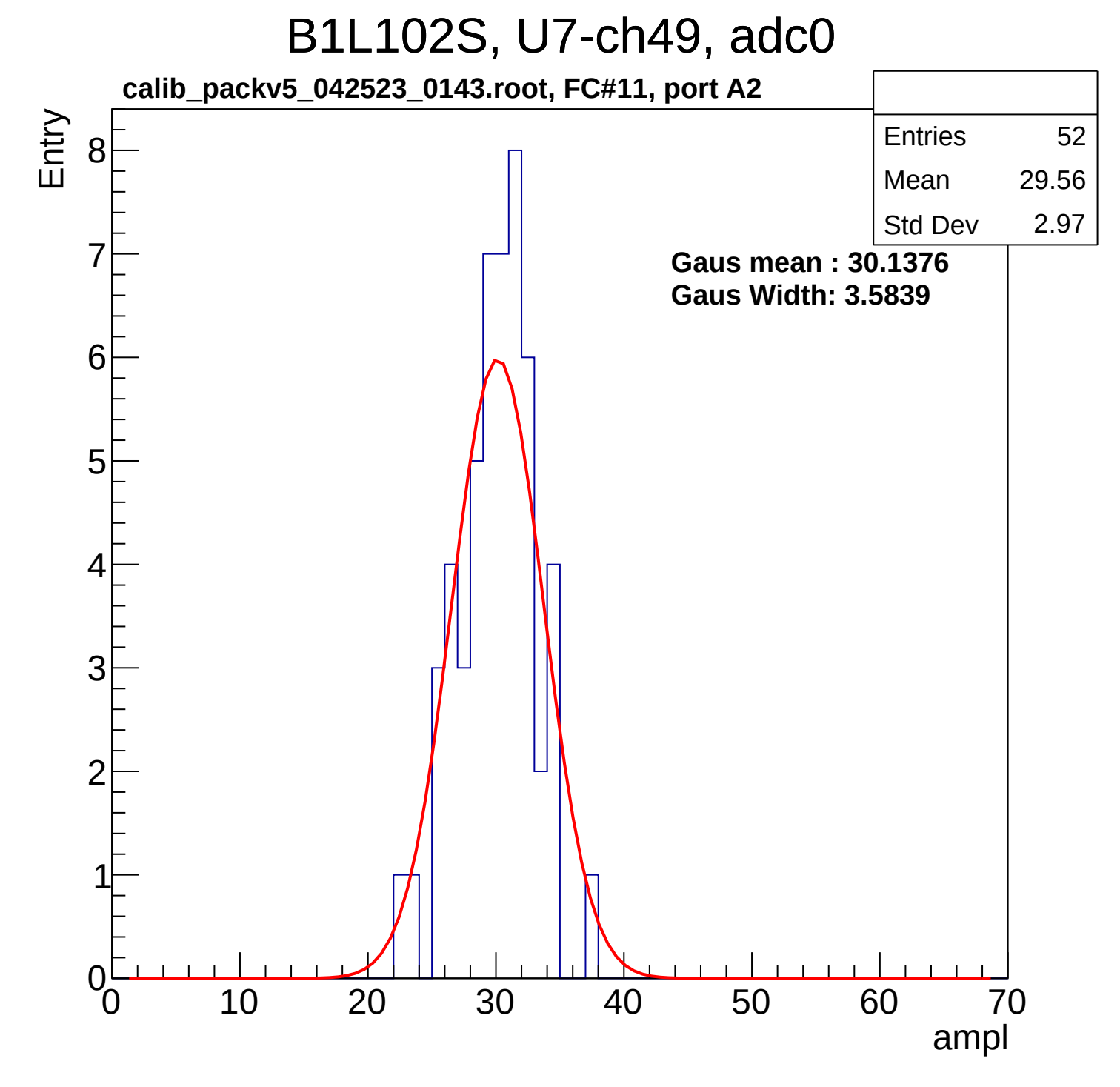
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L102S, U7-ch48, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U7-ch49, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 52
Mean 29.56
Std Dev 2.97
Gaus mean : 30.1376
Gaus Width: 3.5839
Entry
ampl
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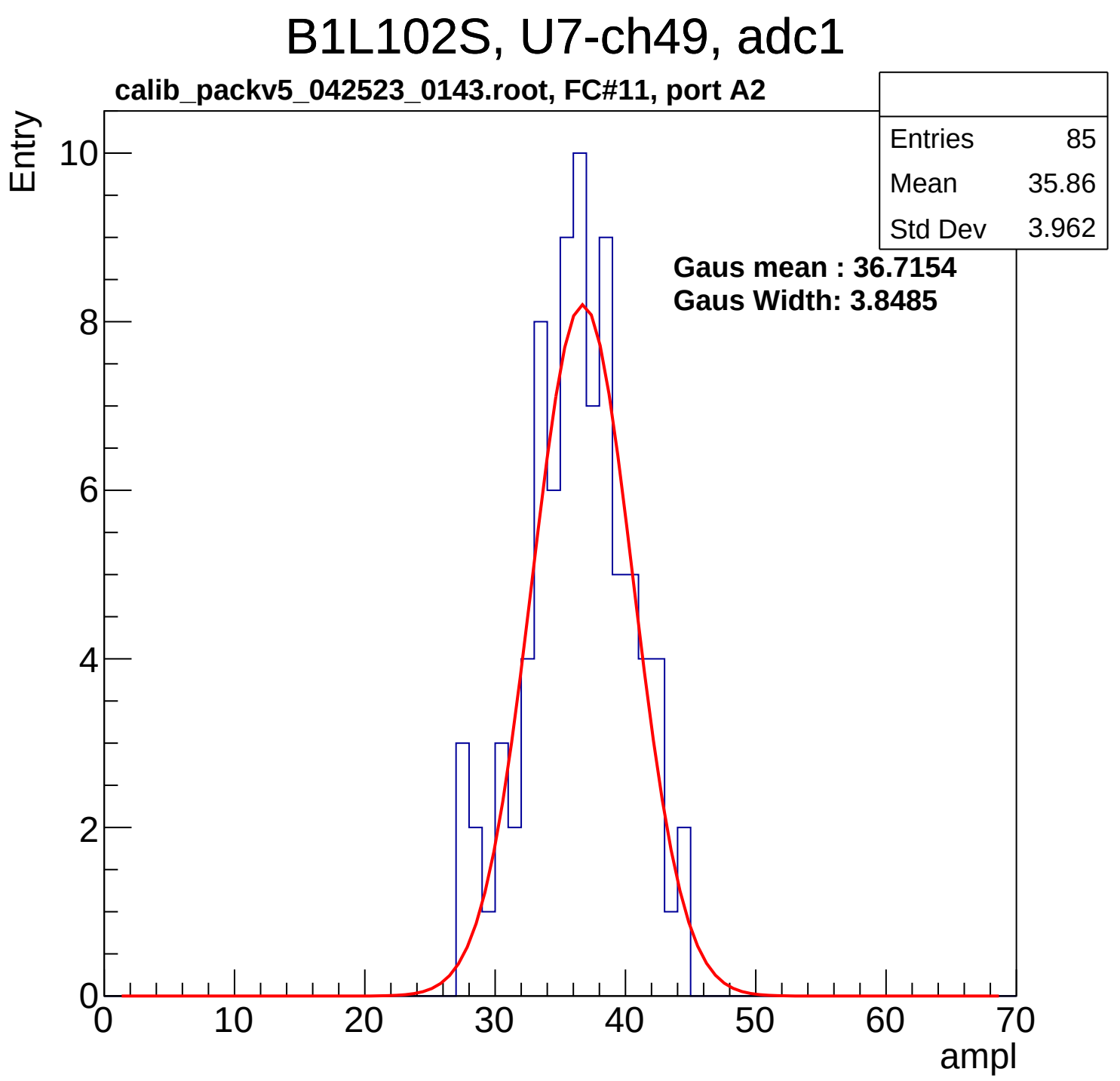
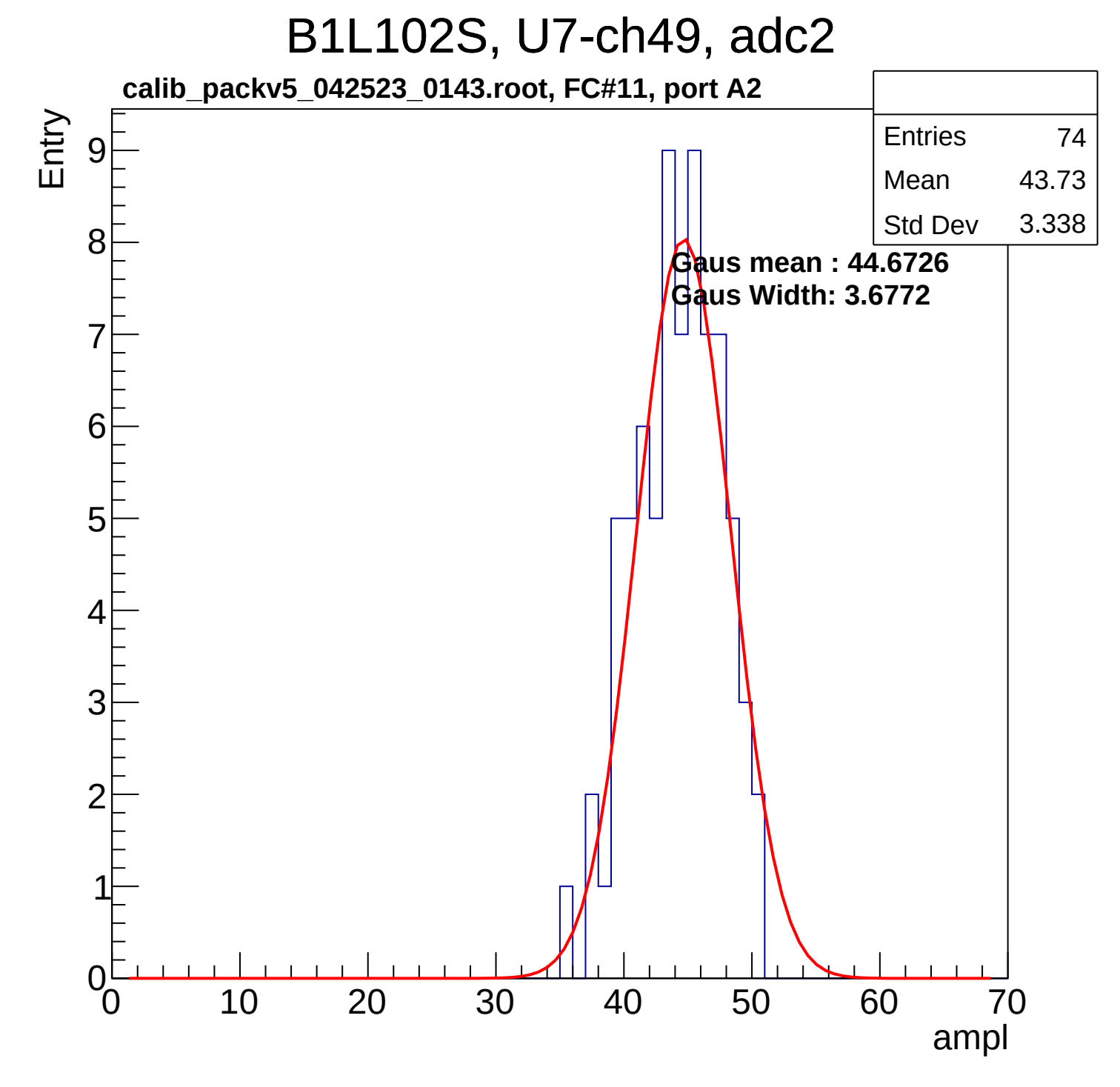
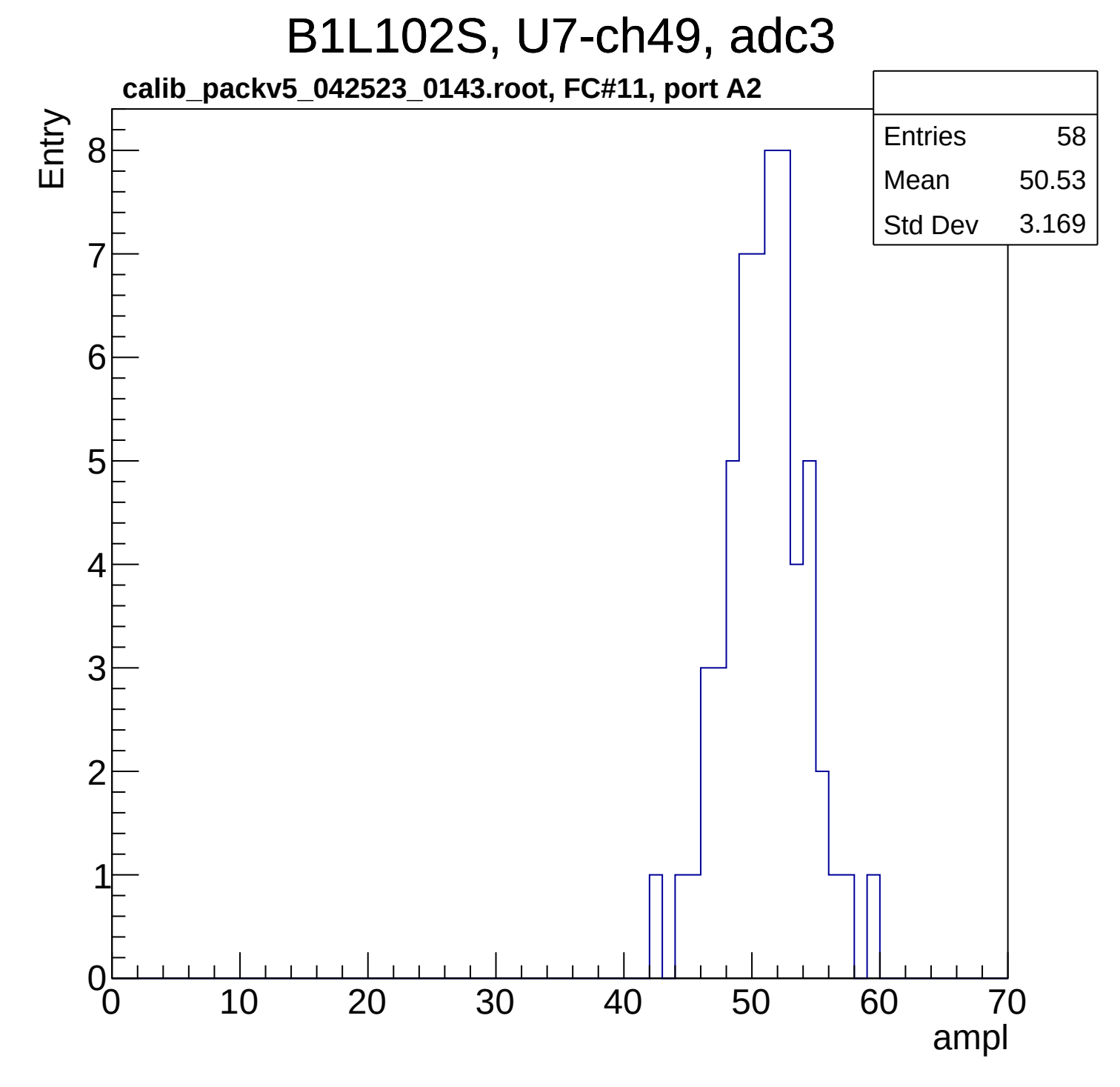
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L102S, U7-ch49, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 85
Mean 35.86
Std Dev 3.962
Gaus mean : 36.7154
Gaus Width: 3.8485
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L102S, U7-ch49, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 74
Mean 43.73
Std Dev 3.338
Gaus mean : 44.6726
Gaus Width: 3.6772
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L102S, U7-ch49, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 58
Mean 50.53
Std Dev 3.169
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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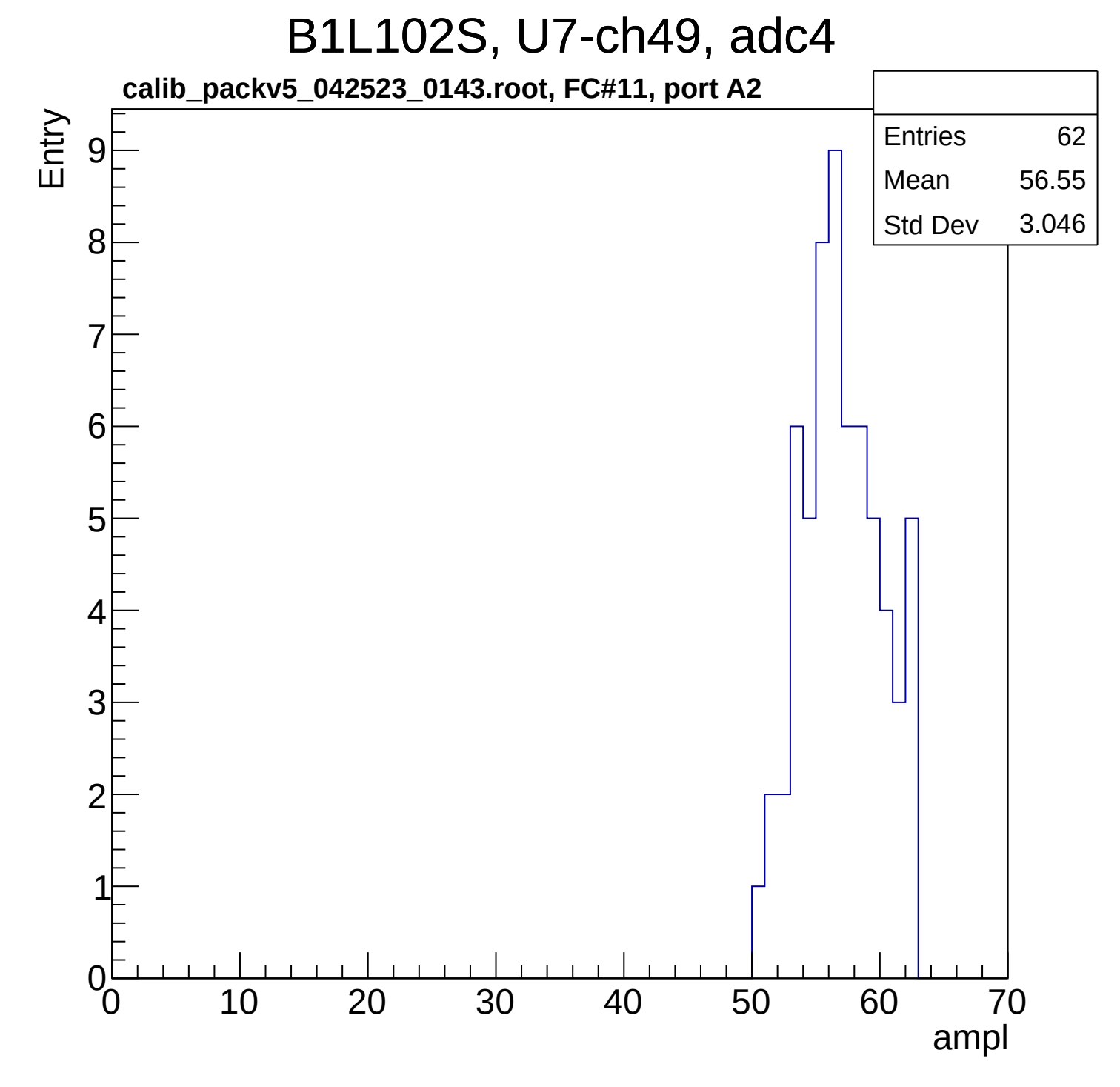
B1L102S, U7-ch49, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 62
Mean 56.55
Std Dev 3.046
Entry
ampl
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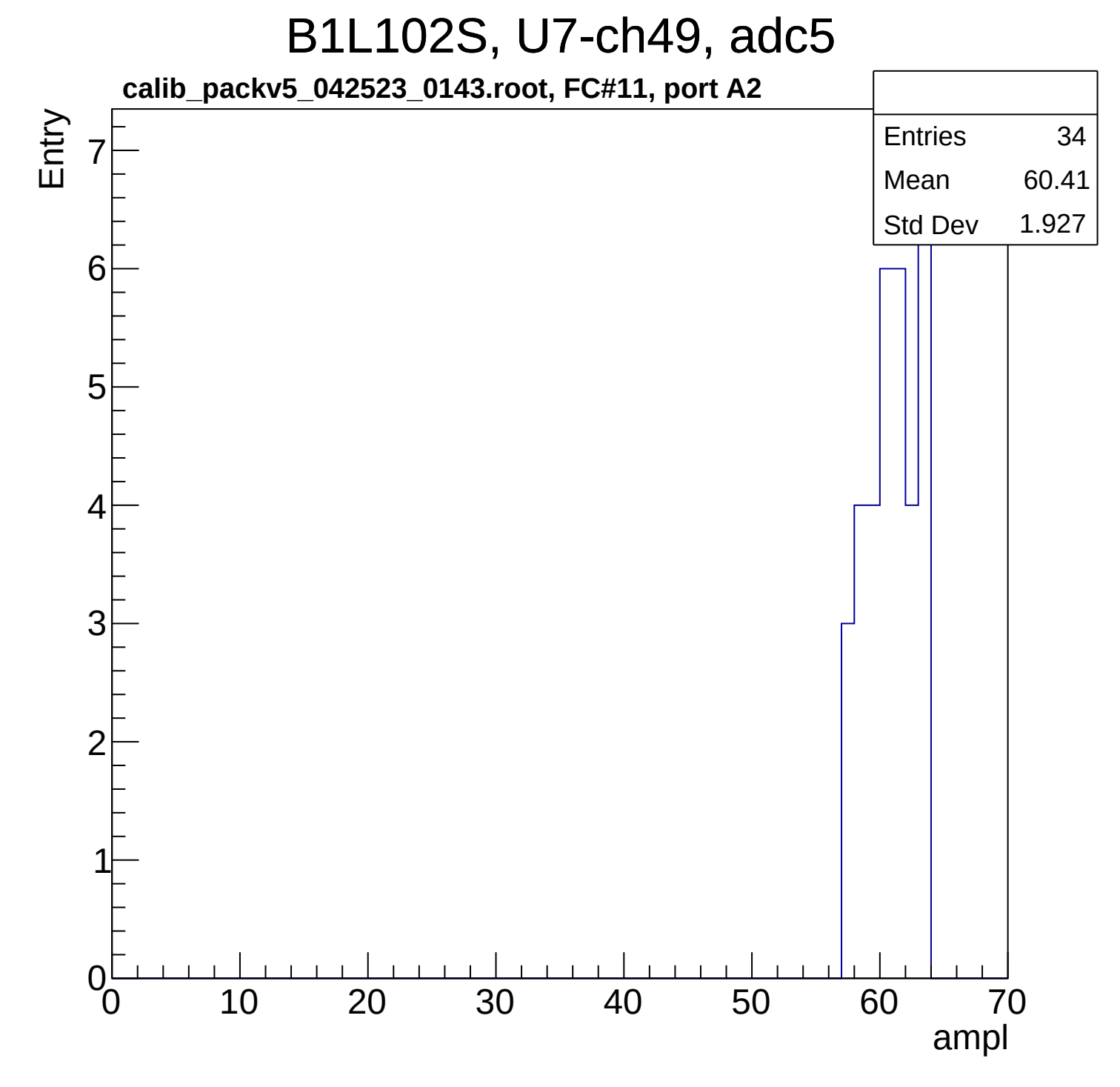
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L102S, U7-ch49, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 34
Mean 60.41
Std Dev 1.927
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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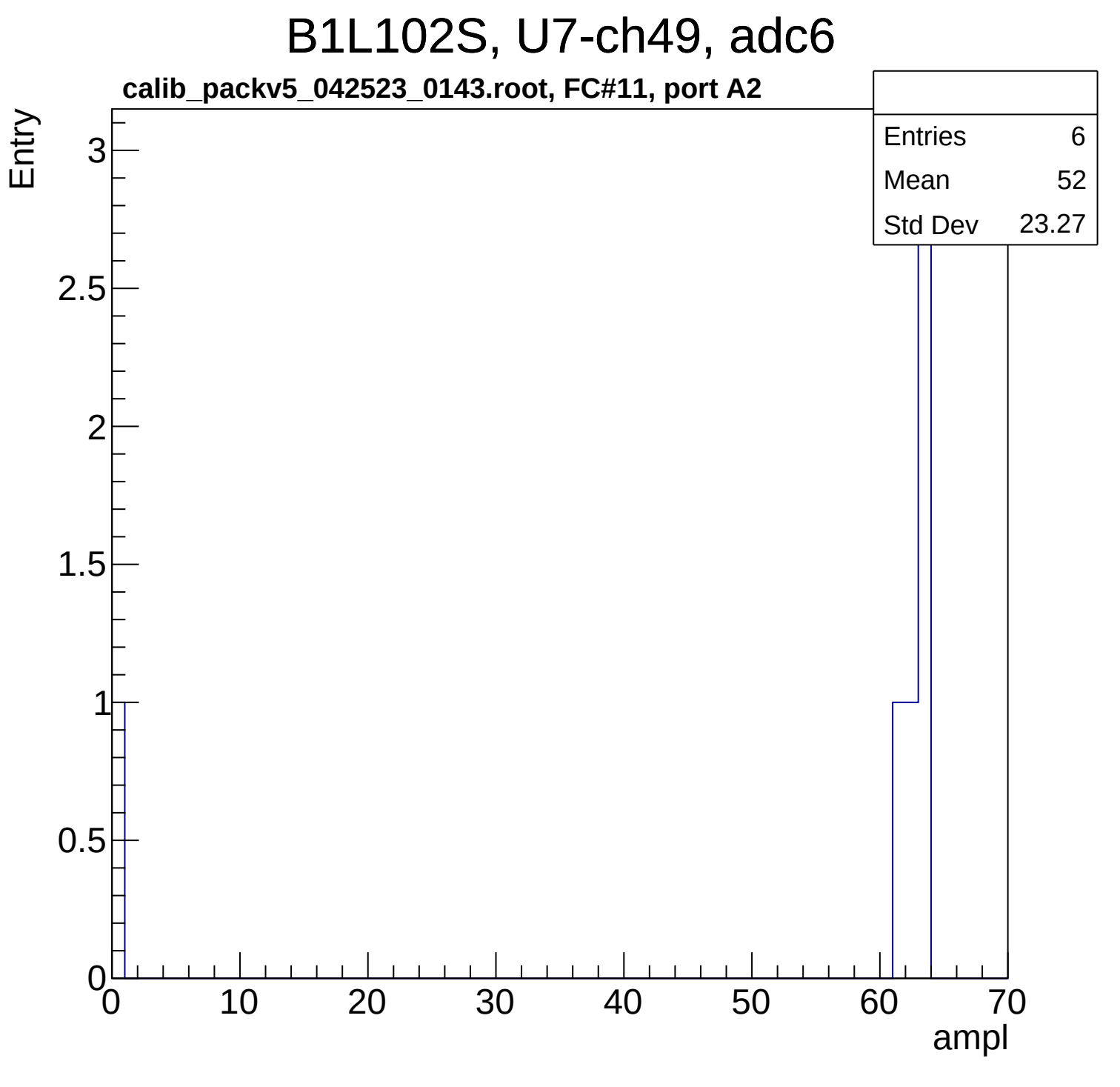
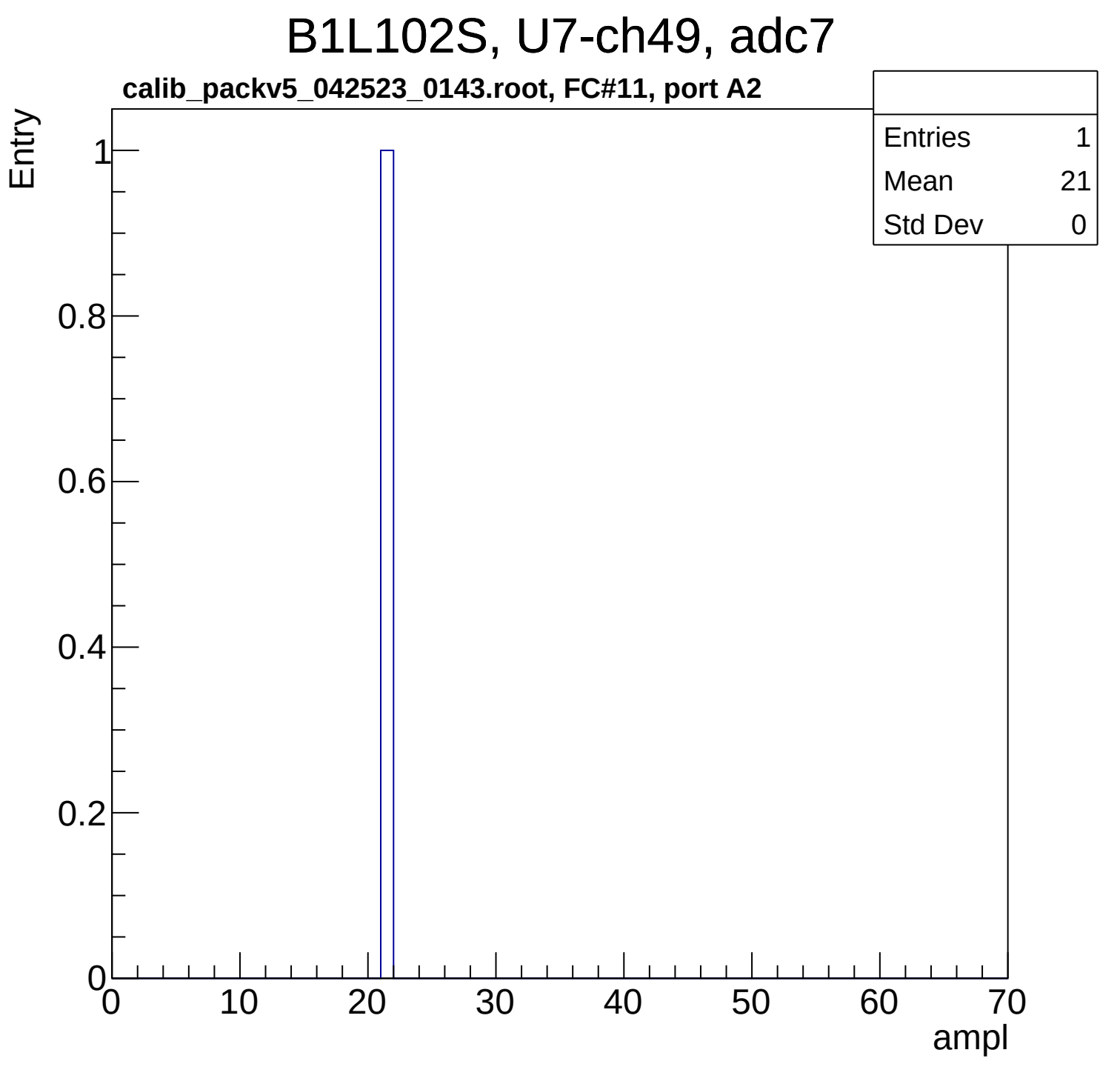
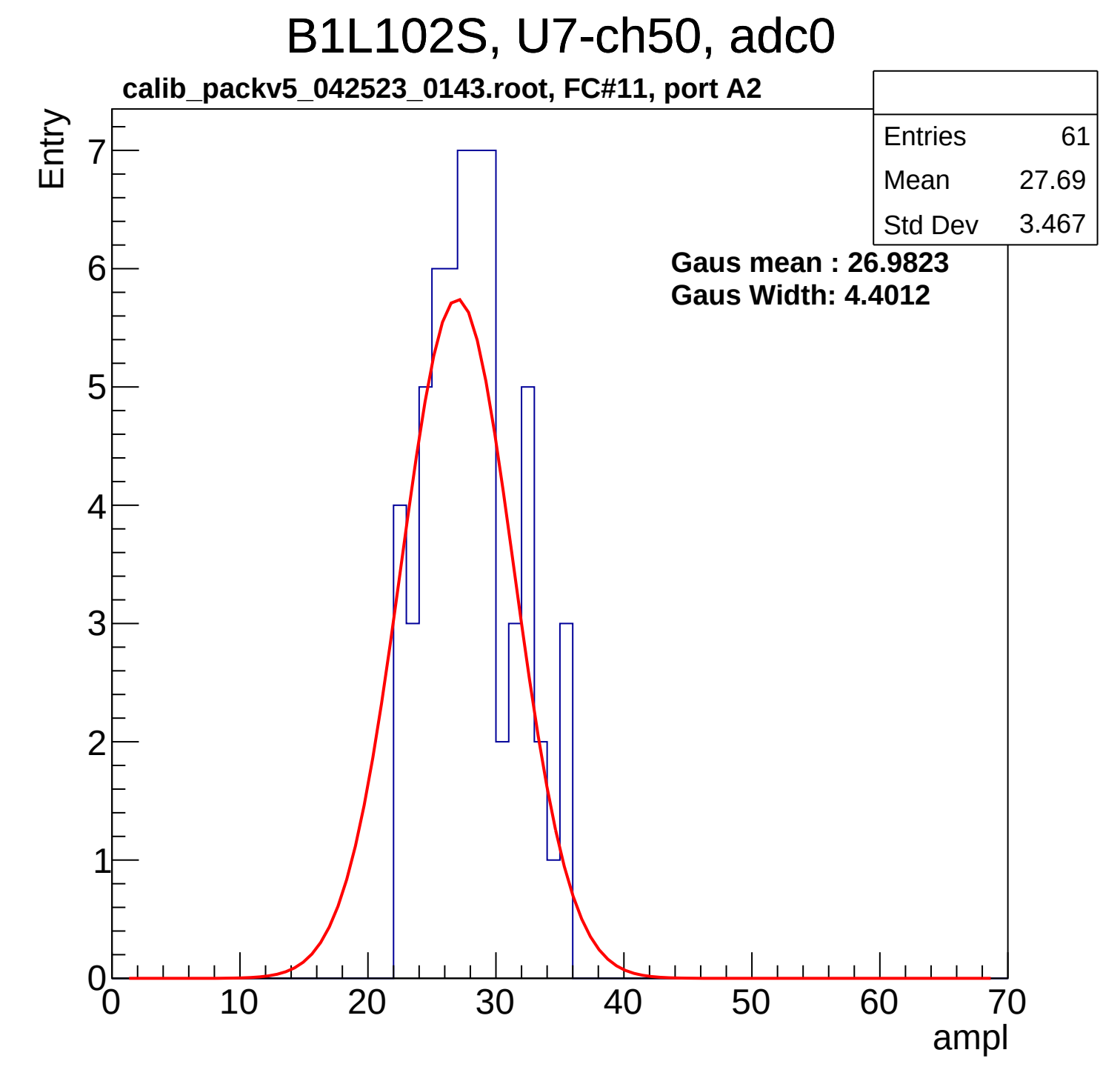

B1L102S, U7-ch49, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 6
Mean 52
Std Dev 23.27
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L102S, U7-ch49, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 1
Mean 21
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U7-ch50, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 61
Mean 27.69
Std Dev 3.467
Gaus mean : 26.9823
Gaus Width: 4.4012
Entry
ampl
0
1
2
3
4
5
6
7
0
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20
30
40
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60
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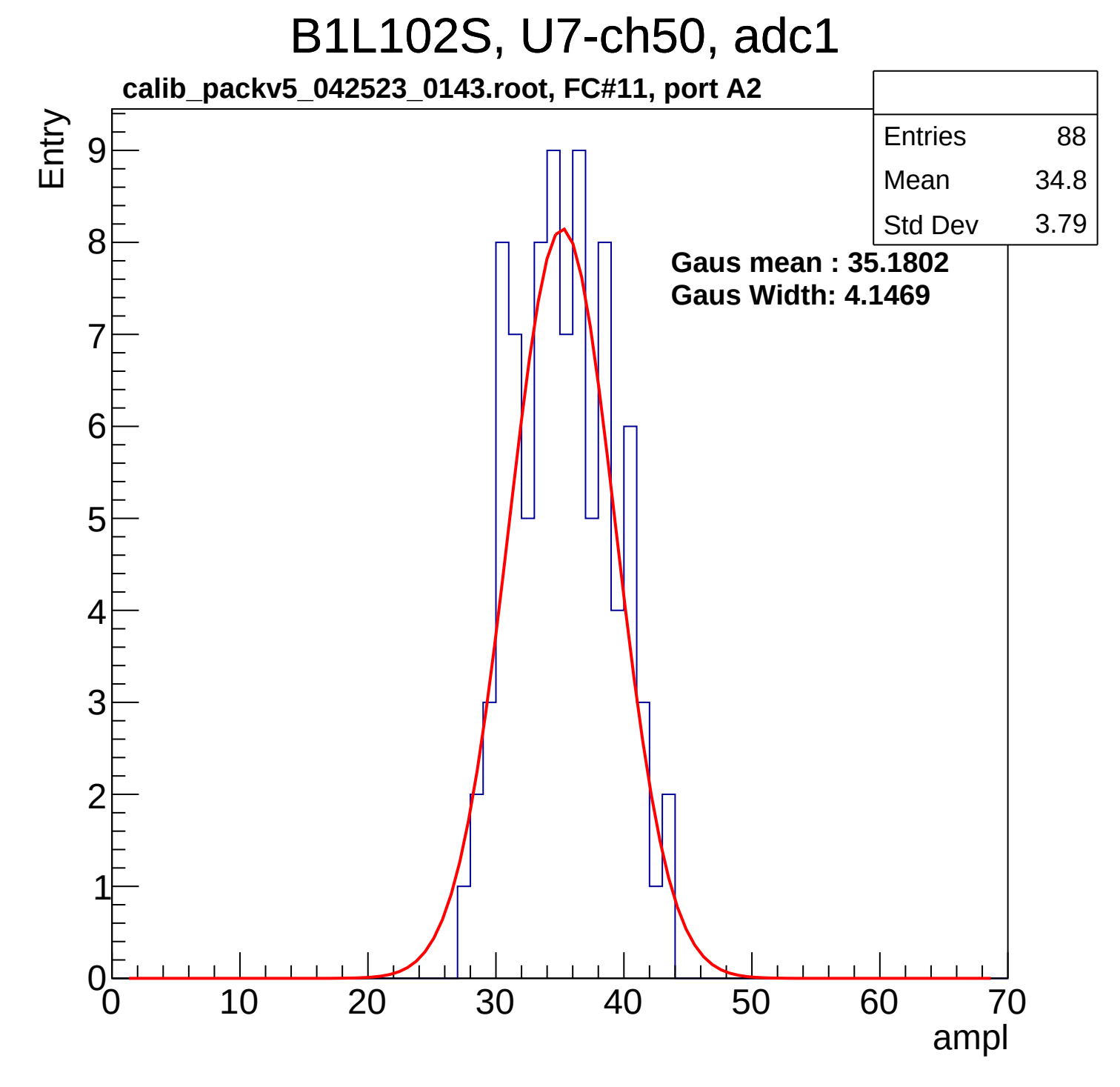
B1L102S, U7-ch50, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 88
Mean 34.8
Std Dev 3.79
Gaus mean : 35.1802
Gaus Width: 4.1469
Entry
ampl
0
1
2
3
4
5
6
7
8
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0
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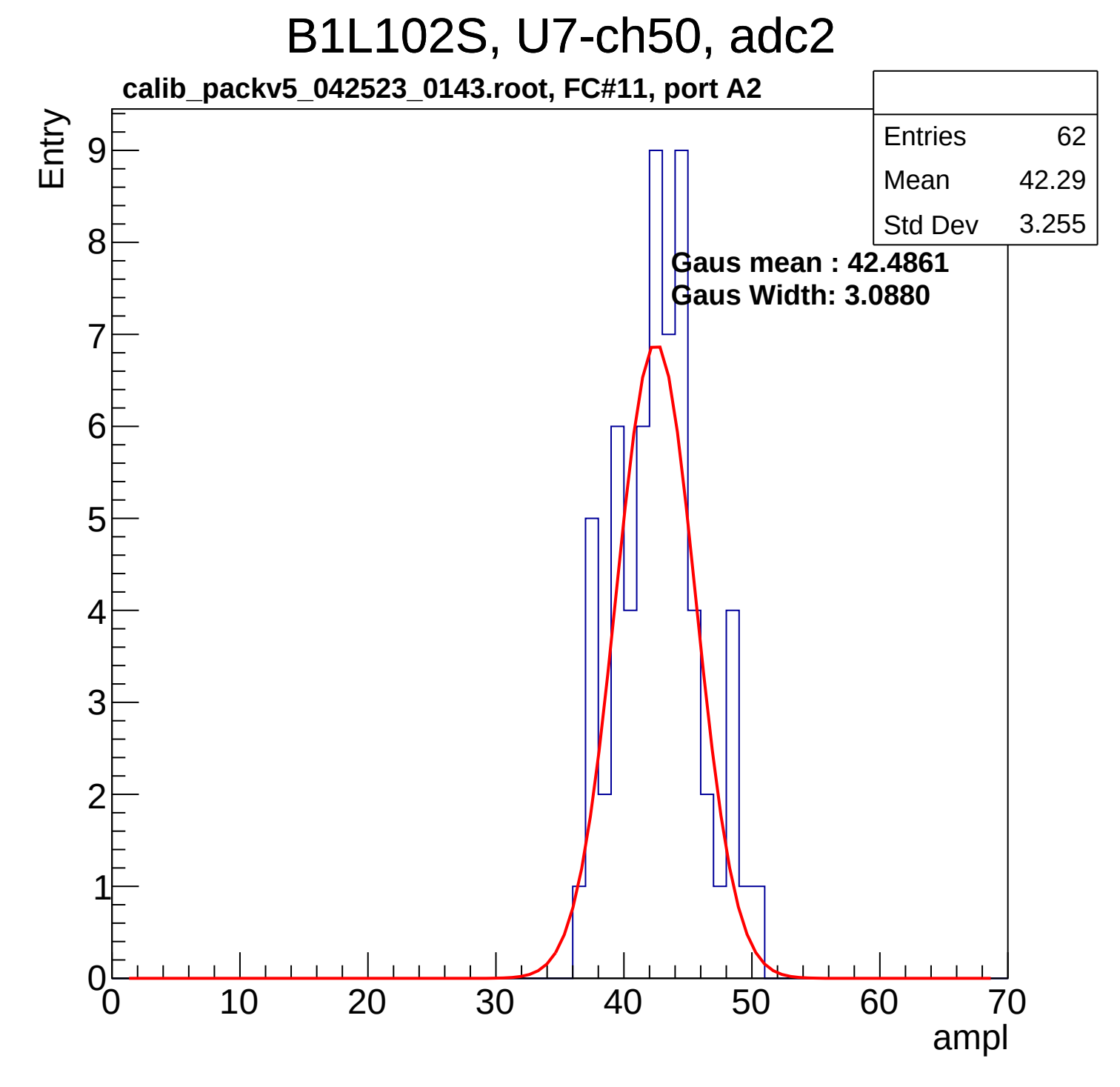
B1L102S, U7-ch50, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 62
Mean 42.29
Std Dev 3.255
Gaus mean : 42.4861
Gaus Width: 3.0880
Entry
ampl
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2
3
4
5
6
7
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0
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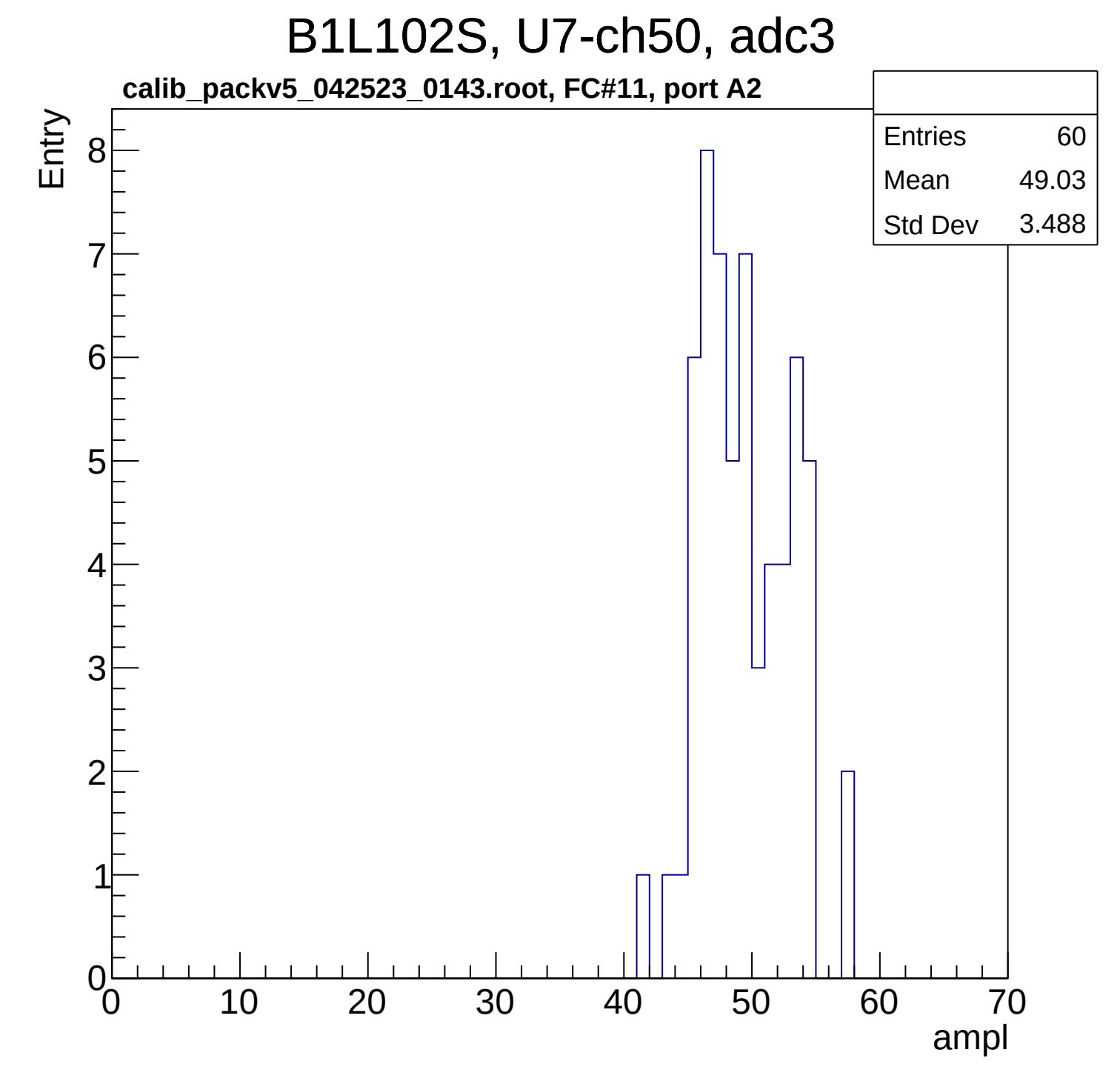
B1L102S, U7-ch50, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 60
Mean 49.03
Std Dev 3.488
Entry
ampl
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1
2
3
4
5
6
7
8
0
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40
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60
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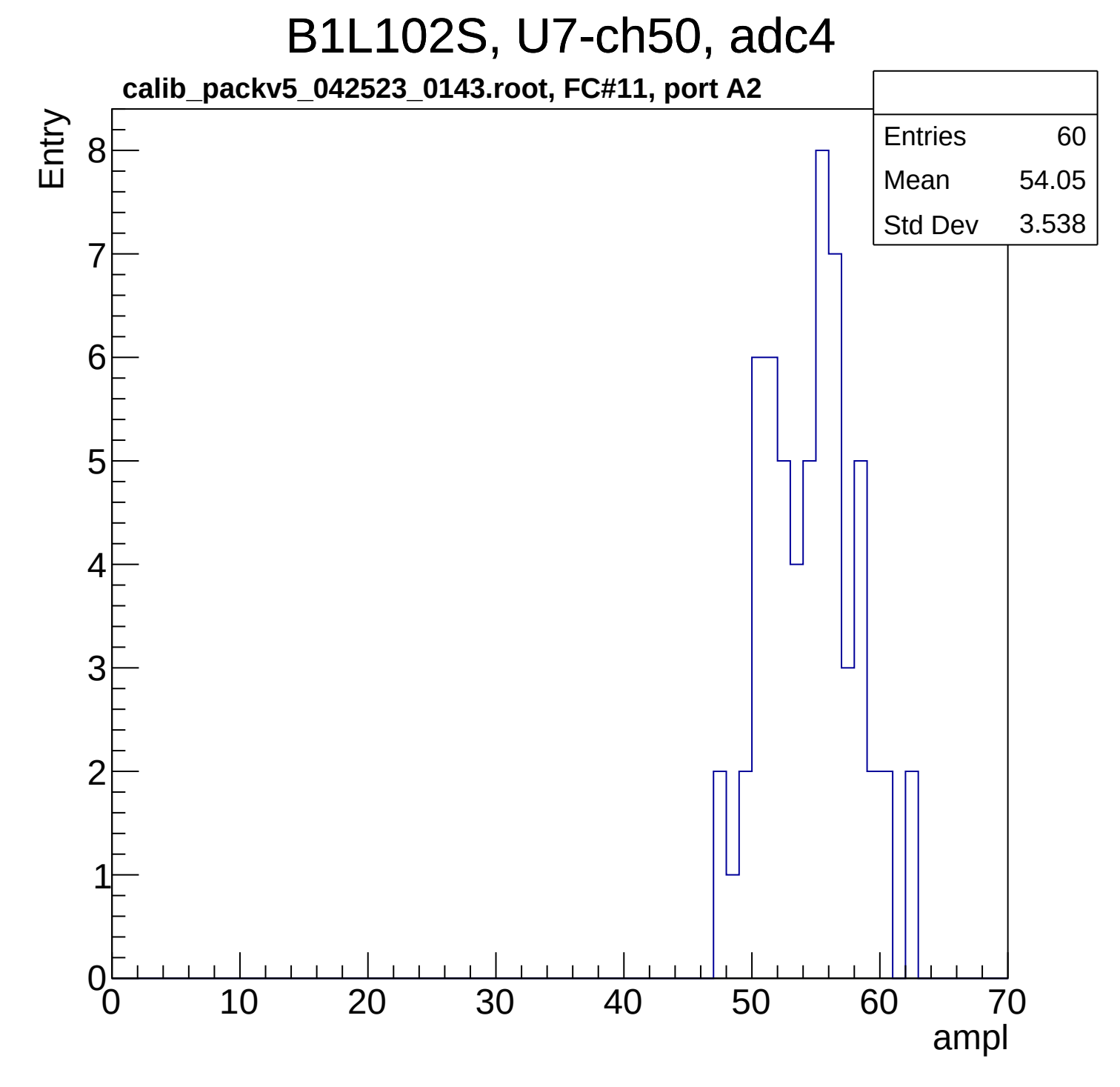
B1L102S, U7-ch50, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 60
Mean 54.05
Std Dev 3.538
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
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60
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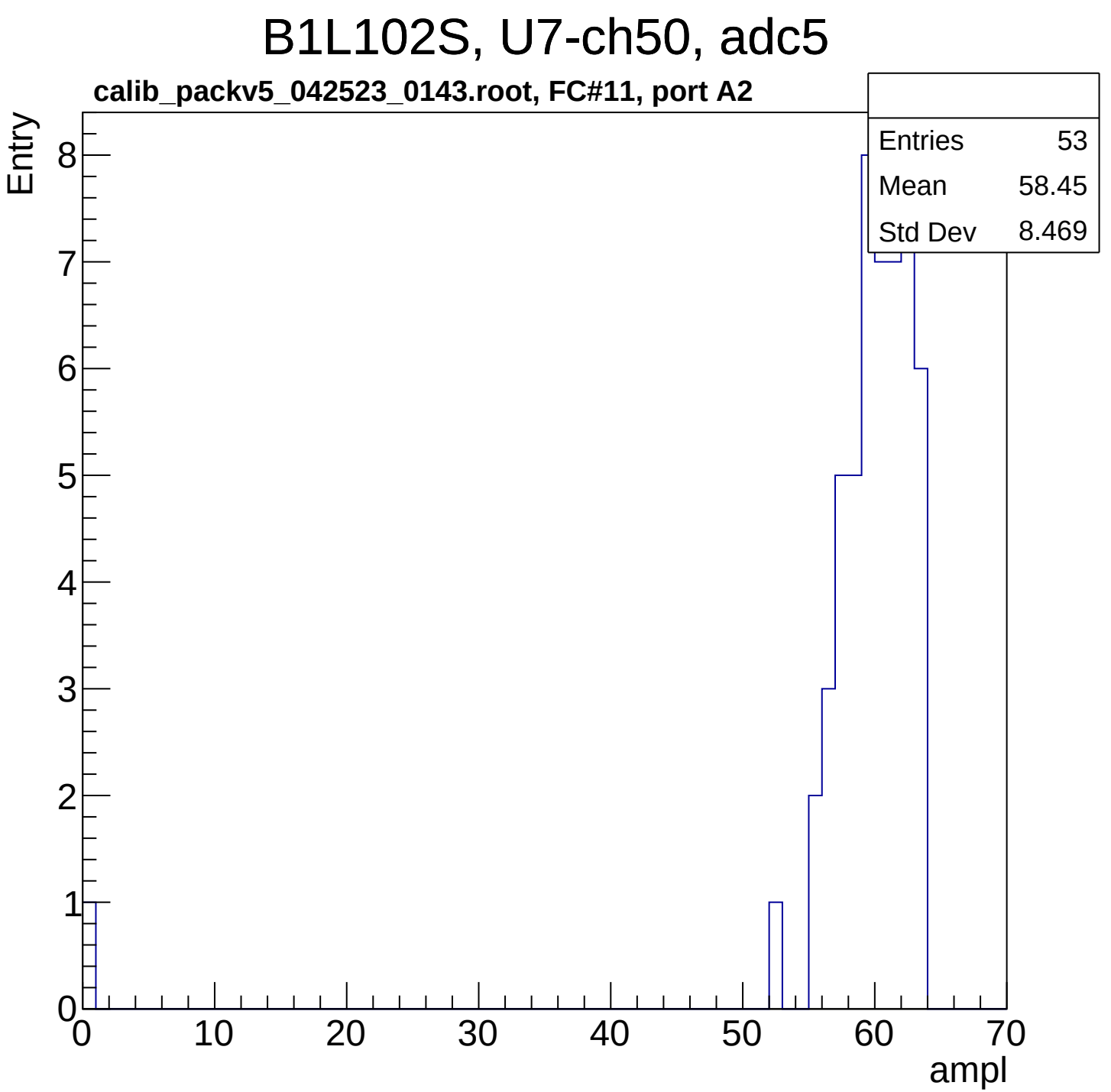
B1L102S, U7-ch50, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 53
Mean 58.45
Std Dev 8.469
Entry
0
1
2
3
4
5
6
7
8
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10
20
30
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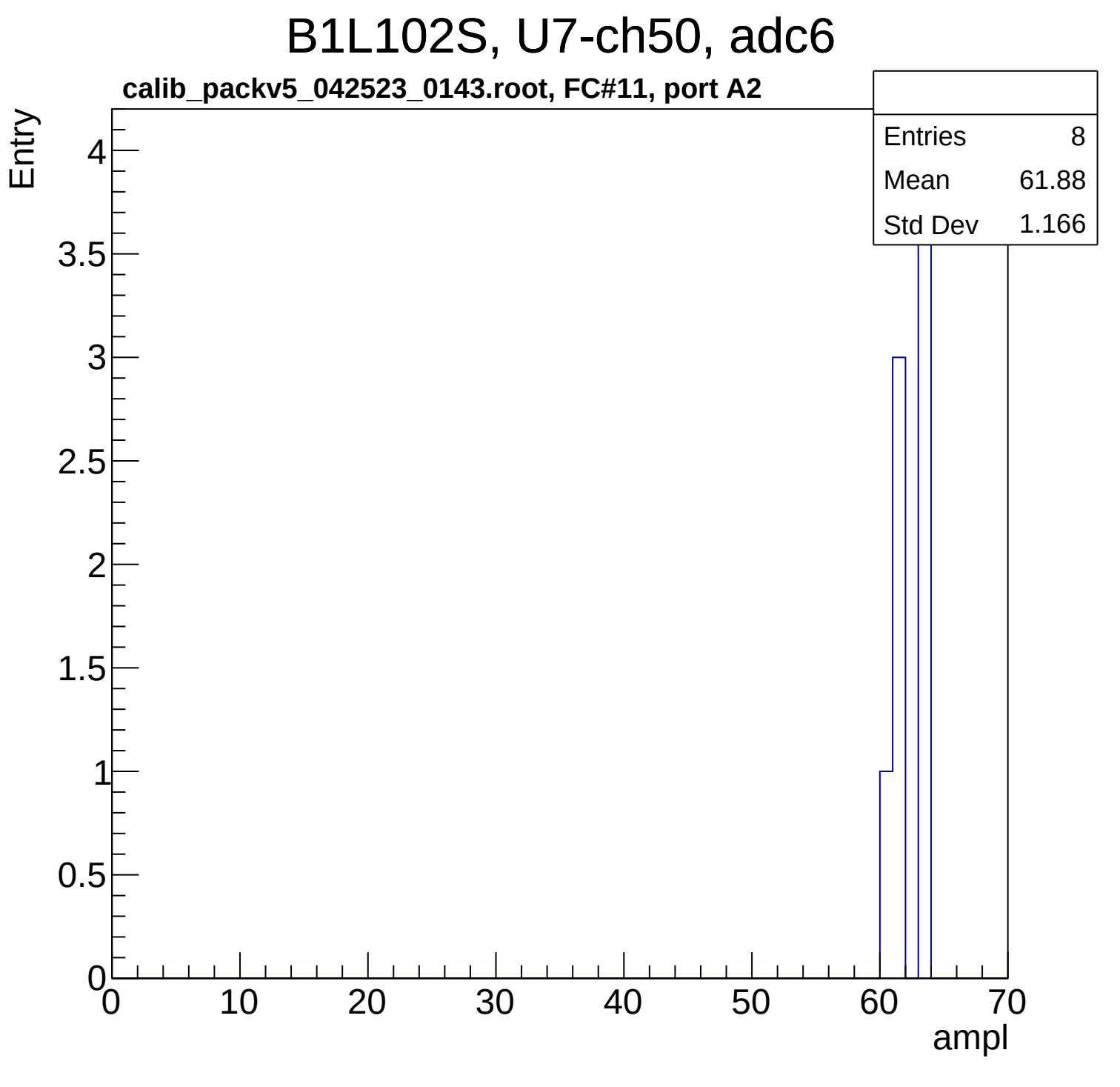
50
60
70
ampl


B1L102S, U7-ch50, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 8
Mean 61.88
Std Dev 1.166
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
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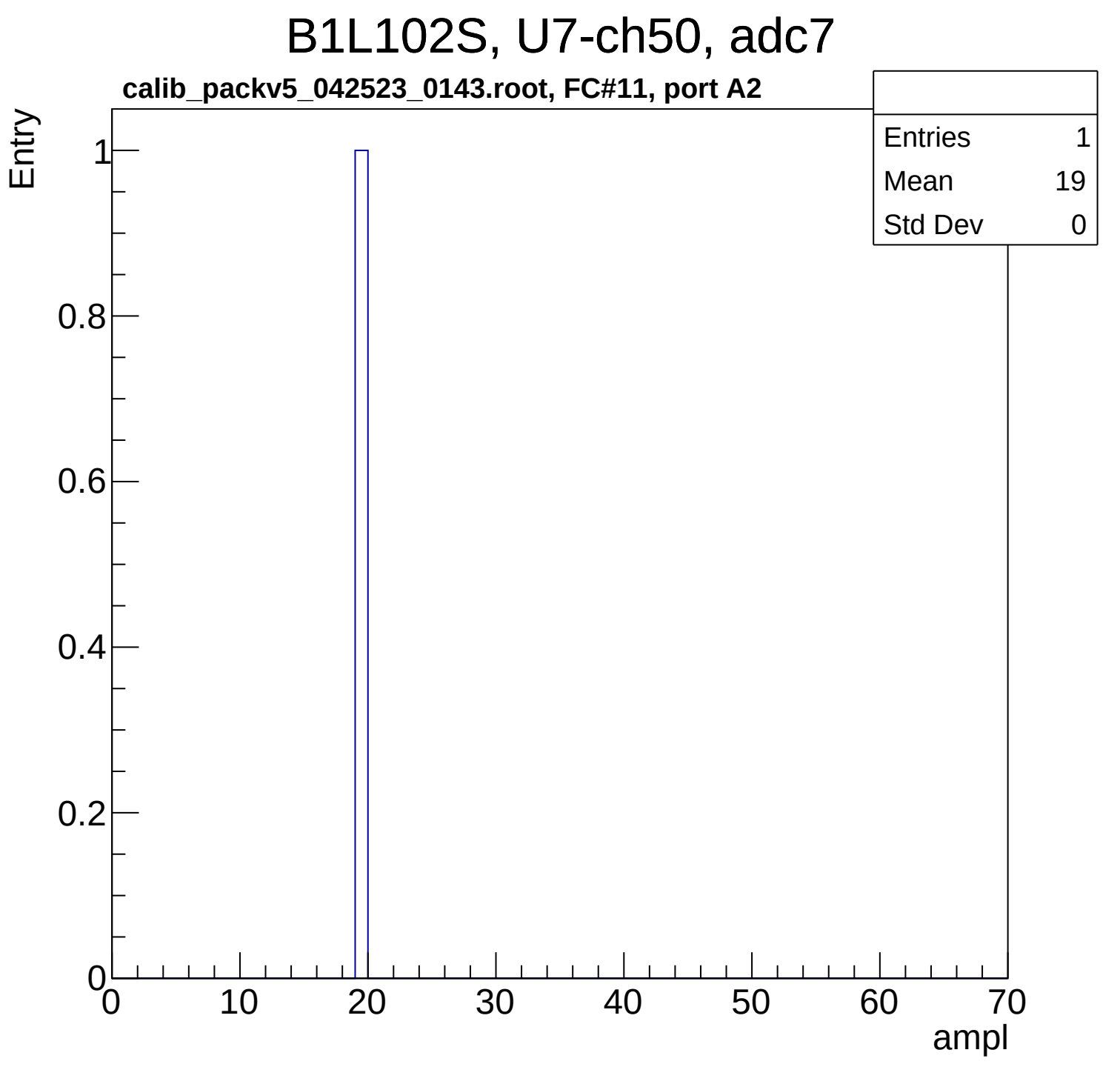
B1L102S, U7-ch50, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 1
Mean 19
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
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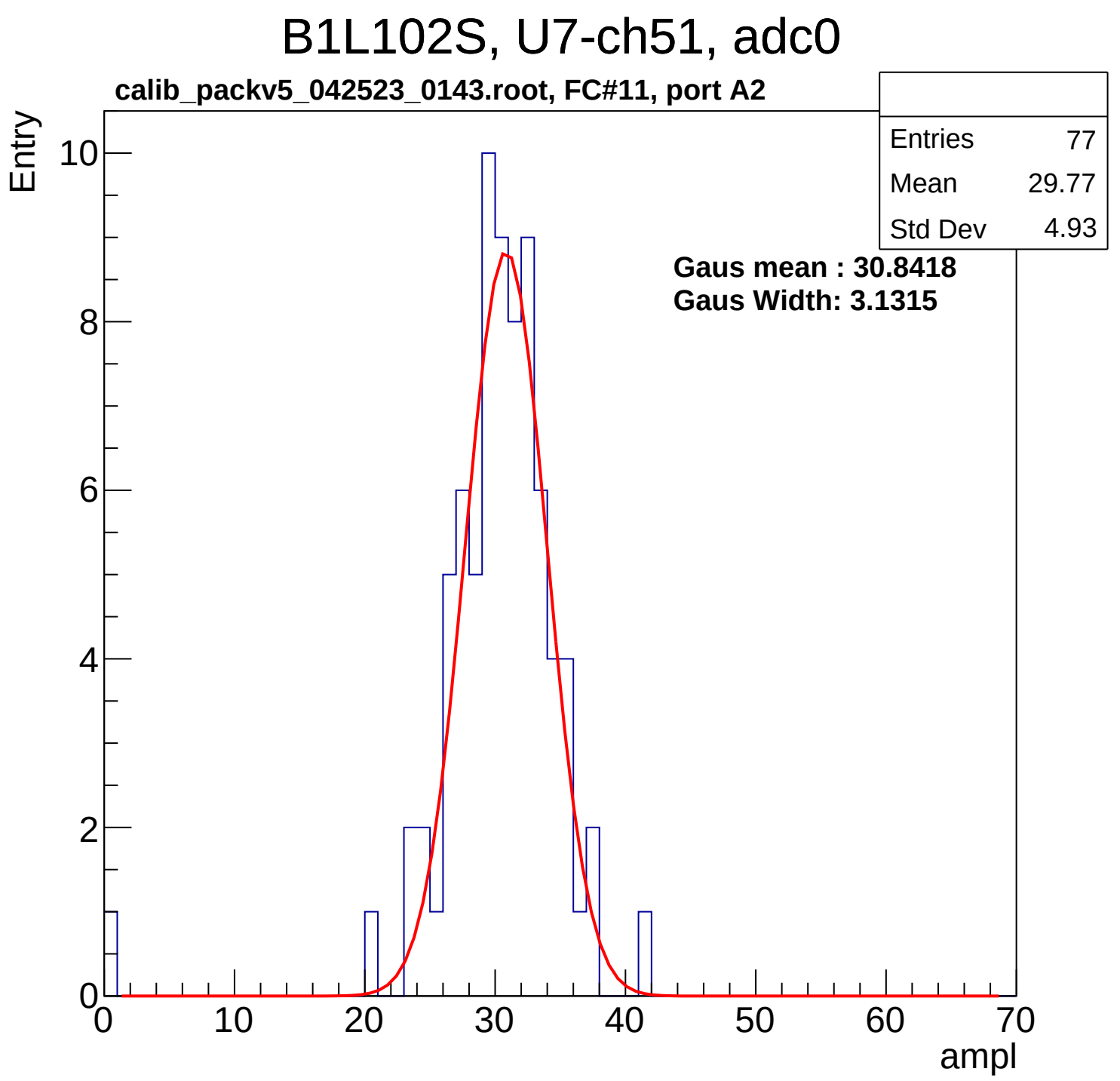
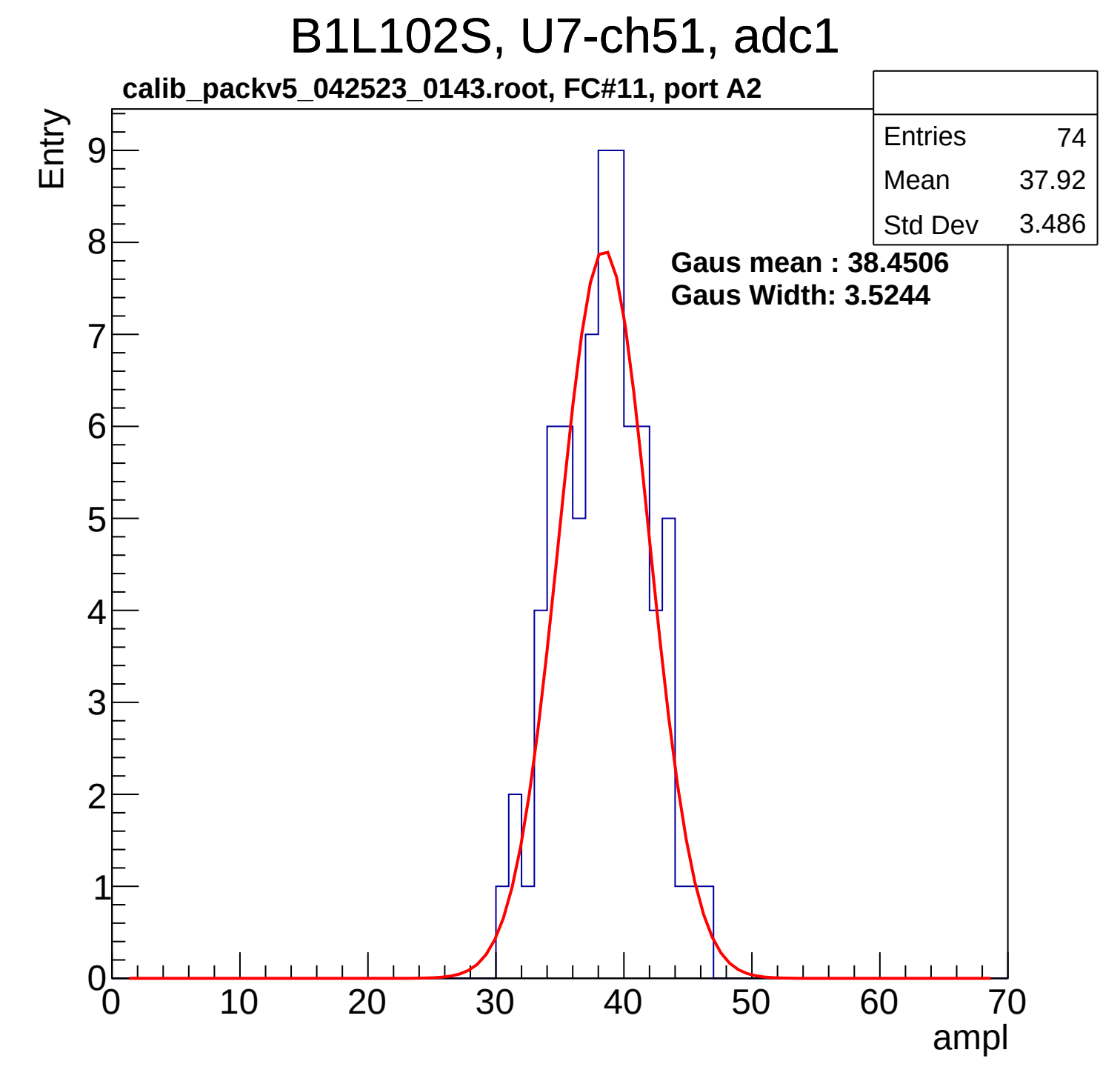
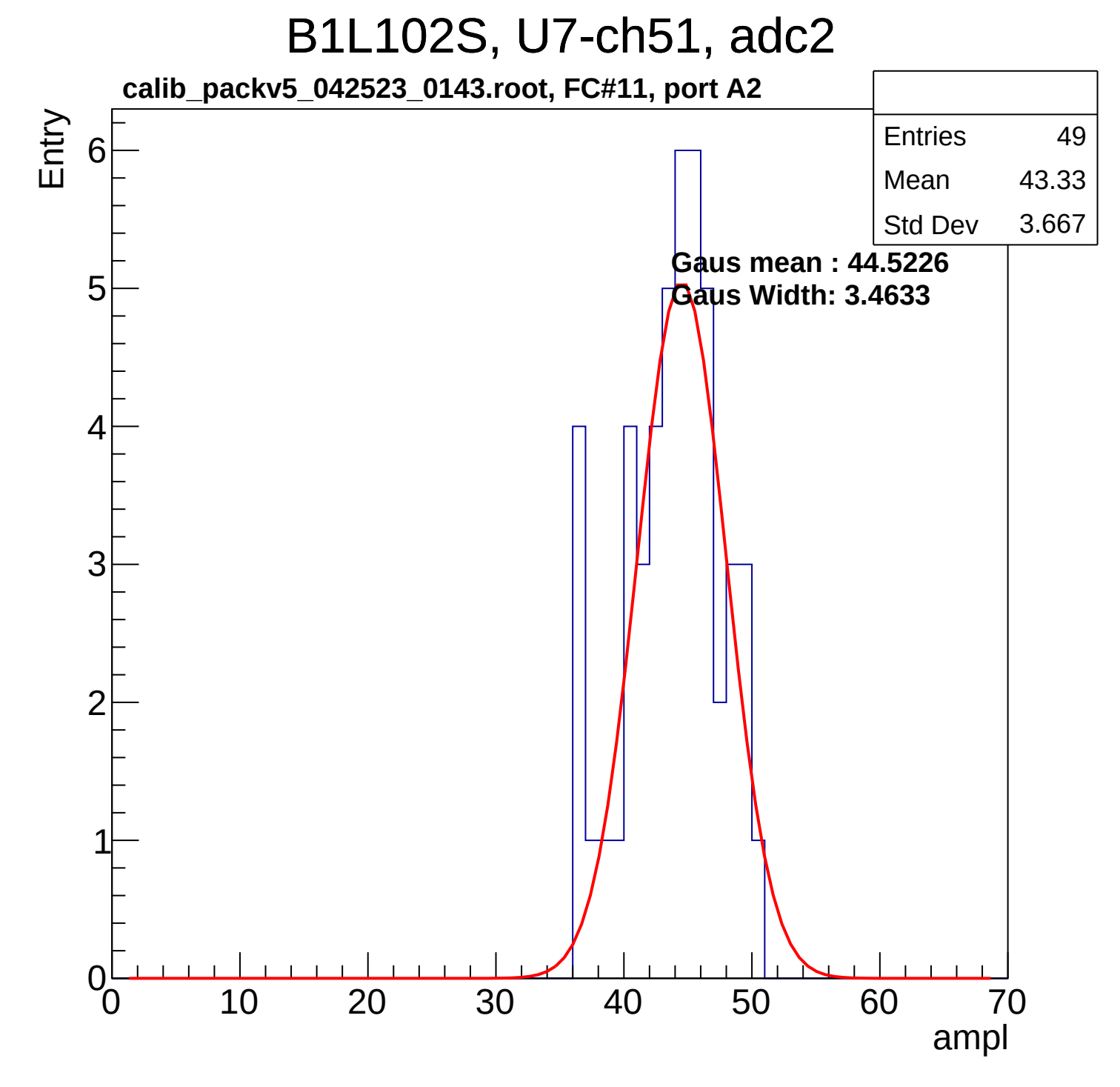
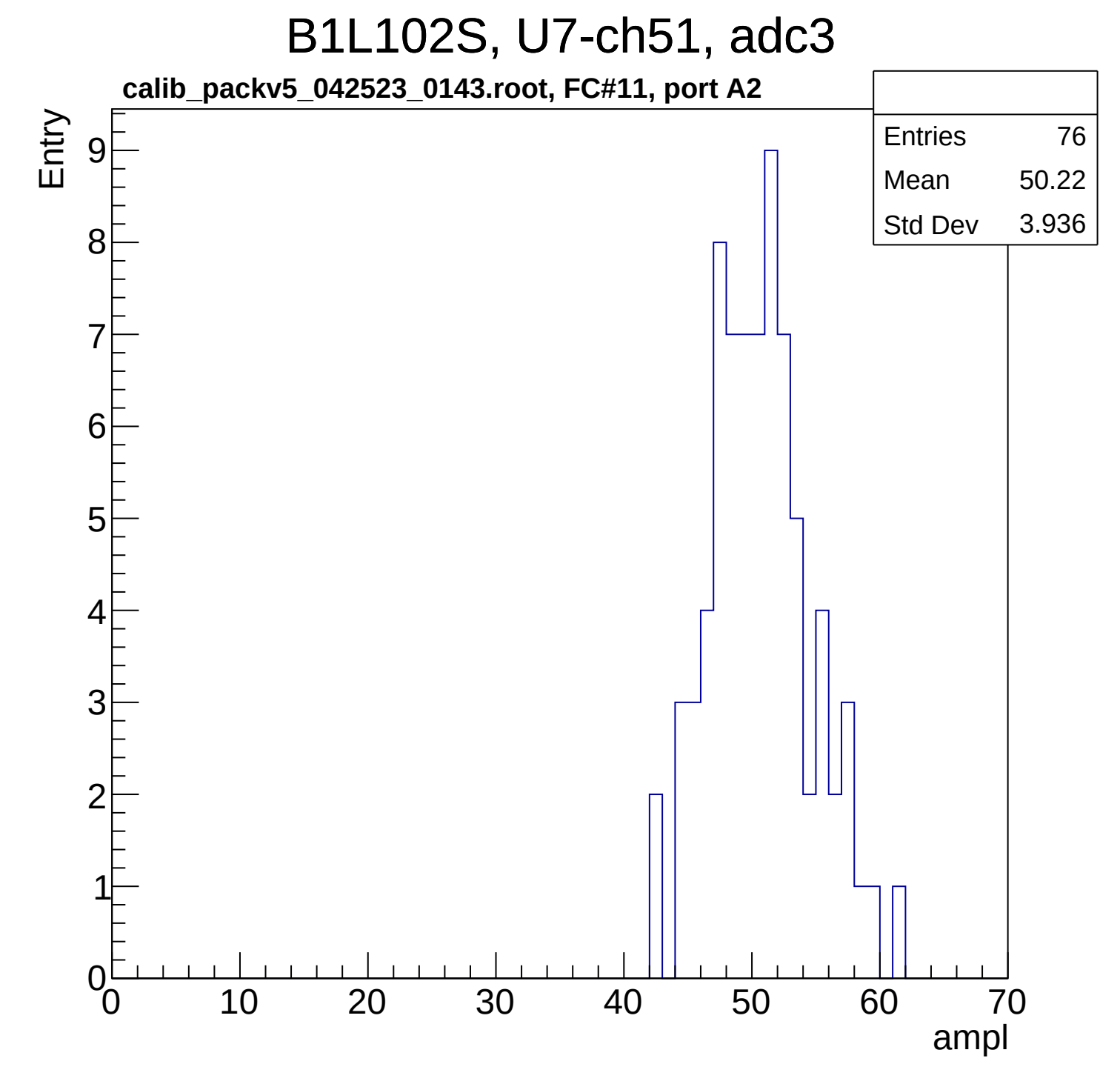
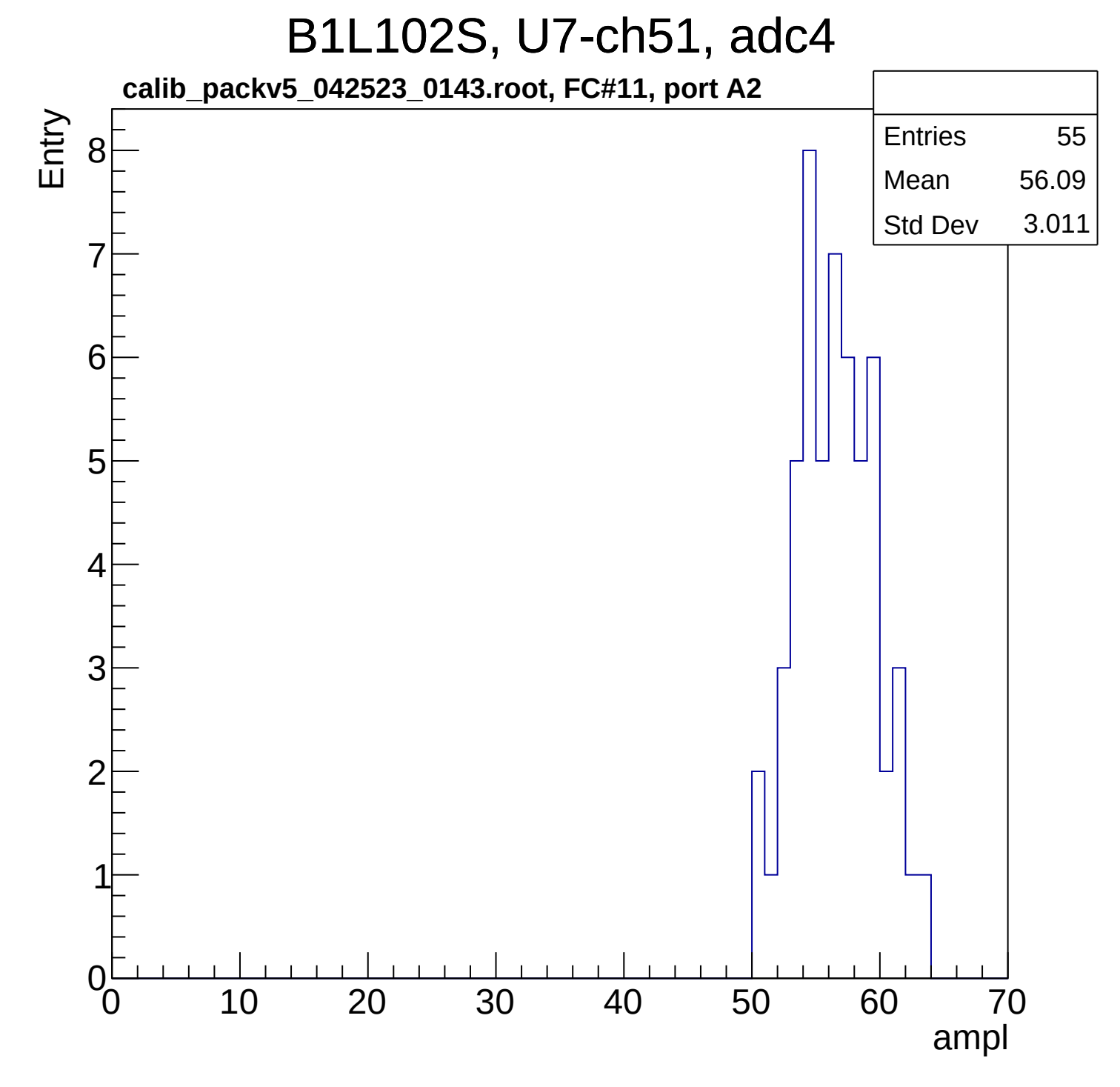

B1L102S, U7-ch51, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 77
Mean 29.77
Std Dev 4.93
Gaus mean : 30.8418
Gaus Width: 3.1315
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L102S, U7-ch51, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 74
Mean 37.92
Std Dev 3.486
Gaus mean : 38.4506
Gaus Width: 3.5244
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L102S, U7-ch51, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 49
Mean 43.33
Std Dev 3.667
Gaus mean : 44.5226
Gaus Width: 3.4633
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L102S, U7-ch51, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 76
Mean 50.22
Std Dev 3.936
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L102S, U7-ch51, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 55
Mean 56.09
Std Dev 3.011
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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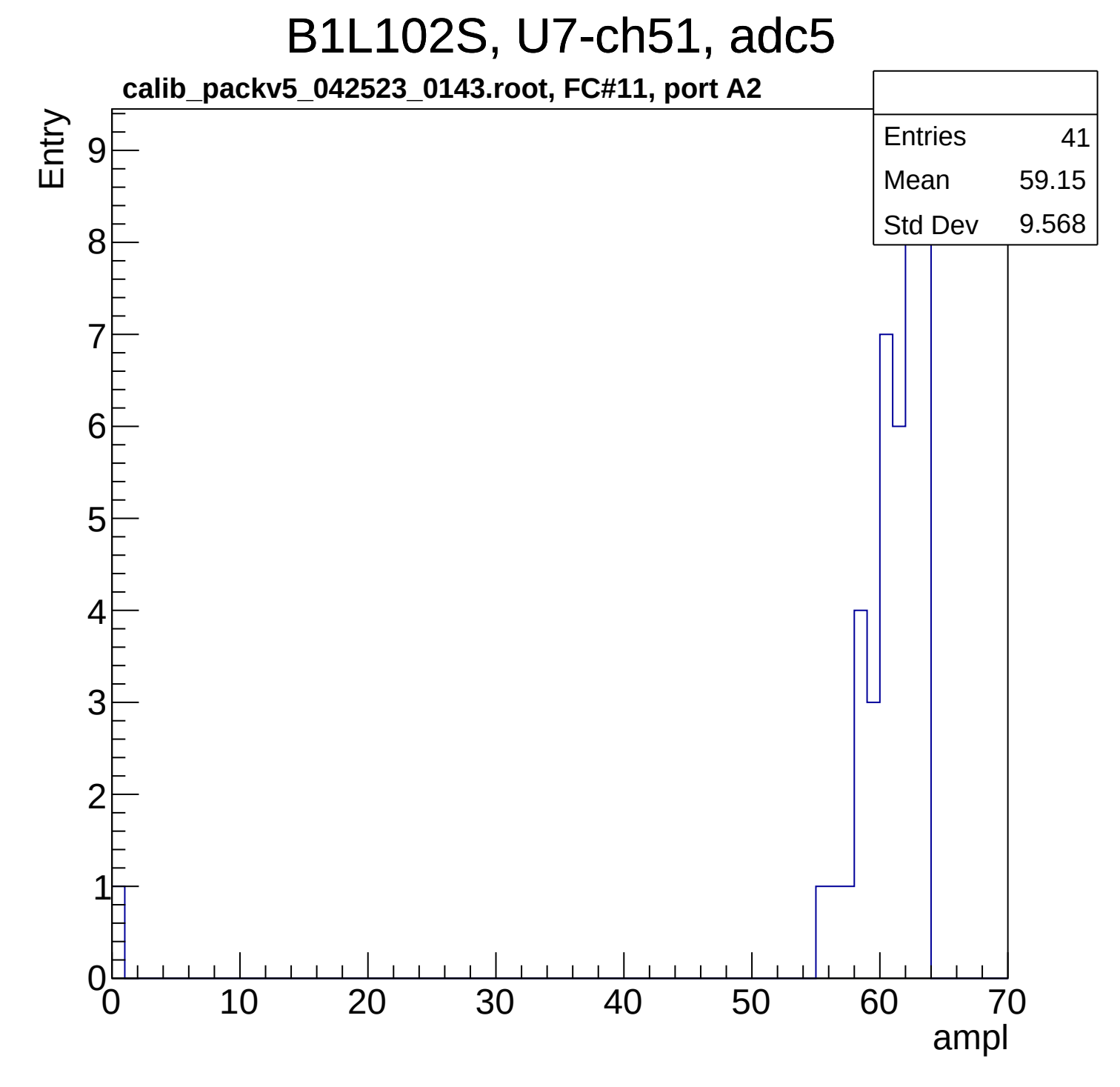
B1L102S, U7-ch51, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 41
Mean 59.15
Std Dev 9.568
Entry
ampl
0
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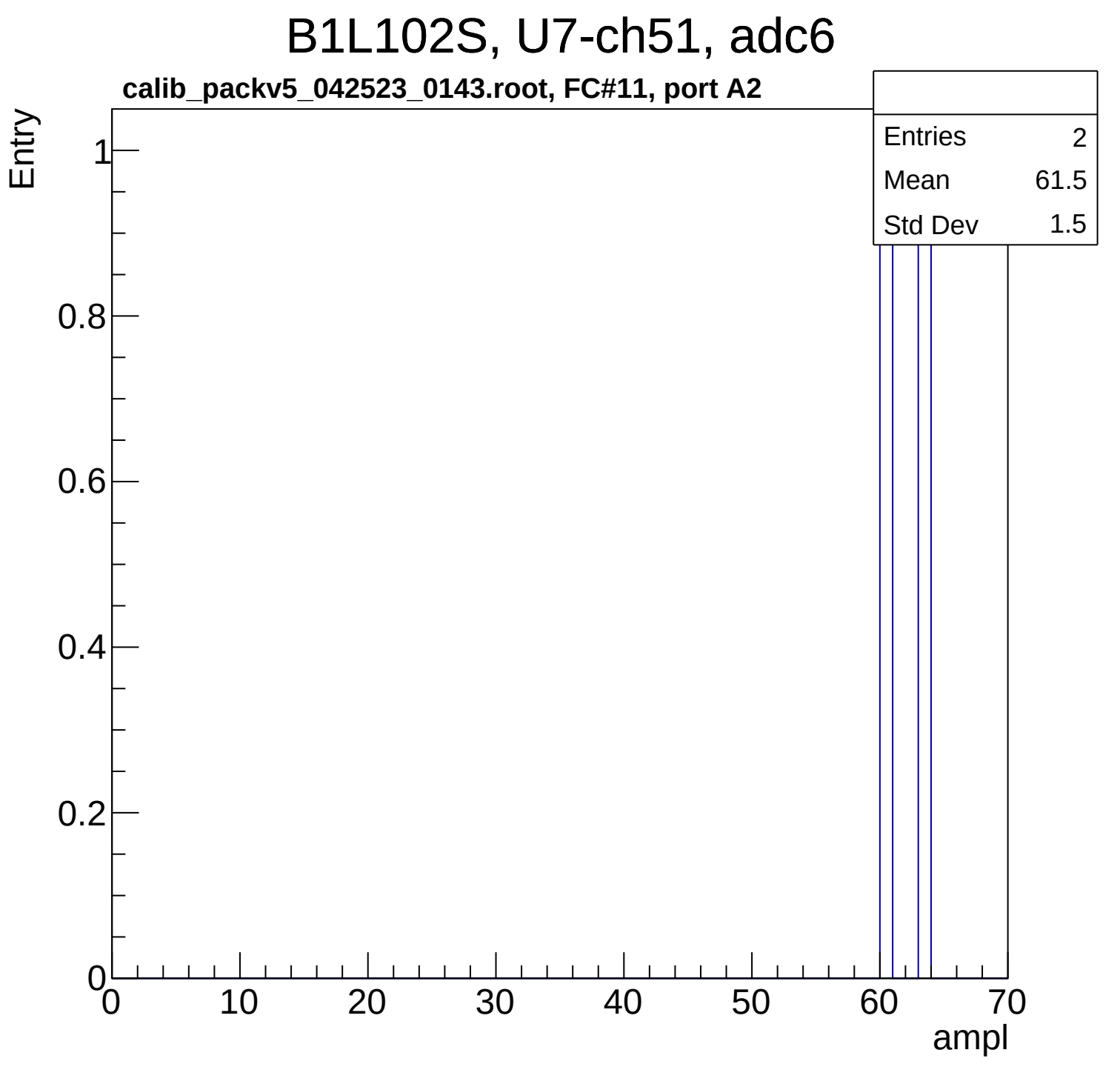
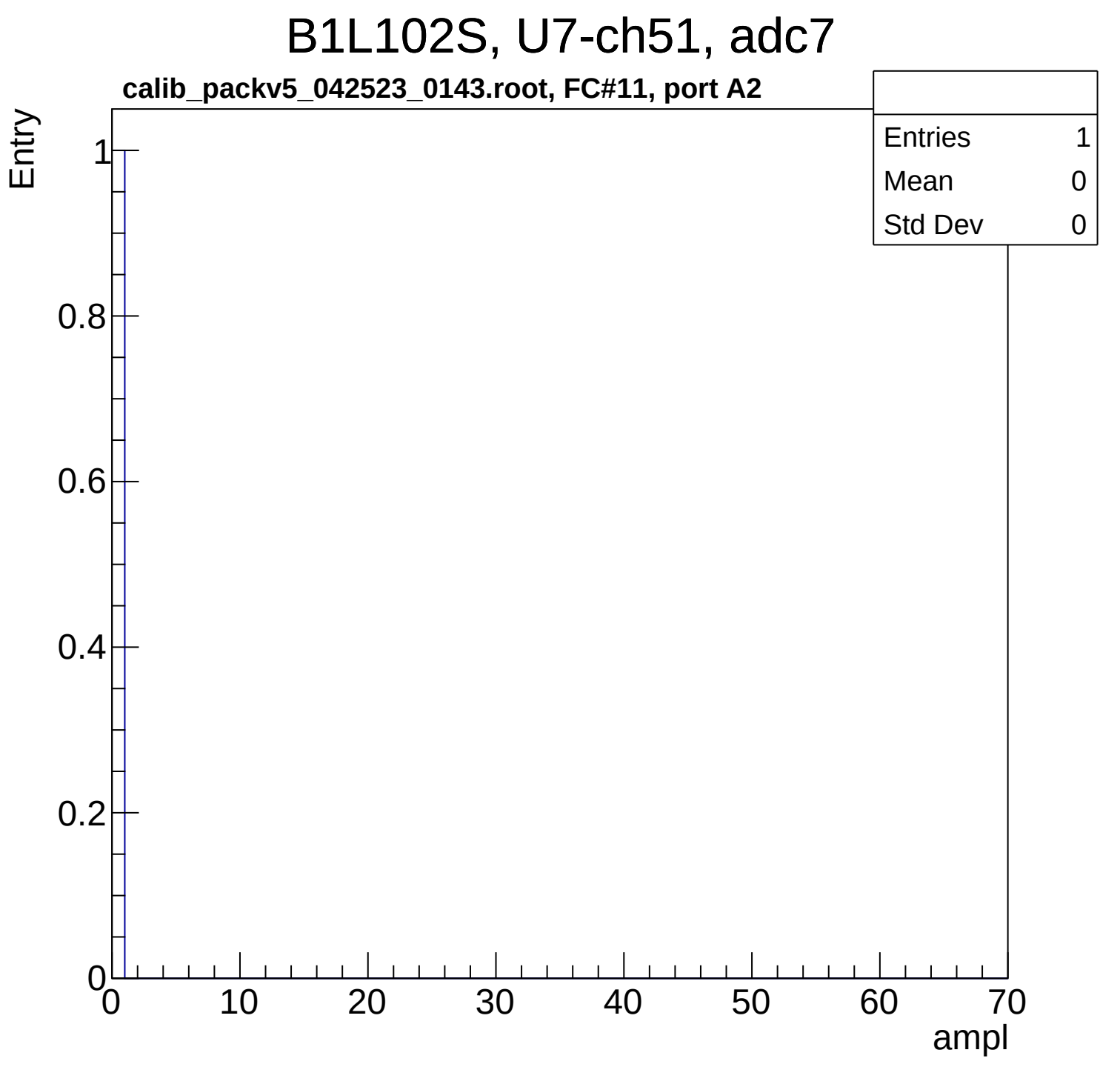
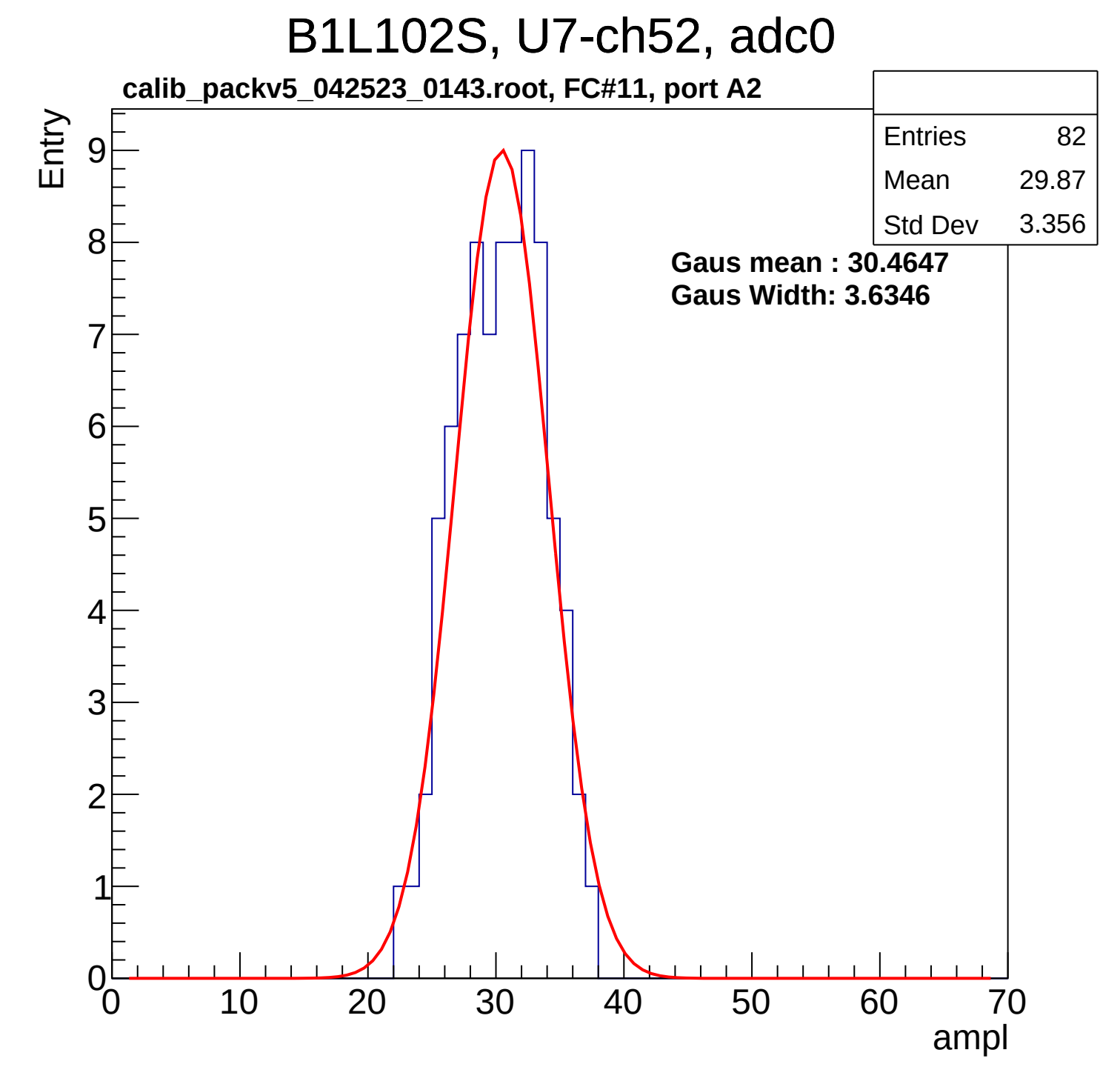
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L102S, U7-ch51, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 2
Mean 61.5
Std Dev 1.5
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70


B1L102S, U7-ch51, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U7-ch52, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 82
Mean 29.87
Std Dev 3.356
Gaus mean : 30.4647
Gaus Width: 3.6346
Entry
ampl
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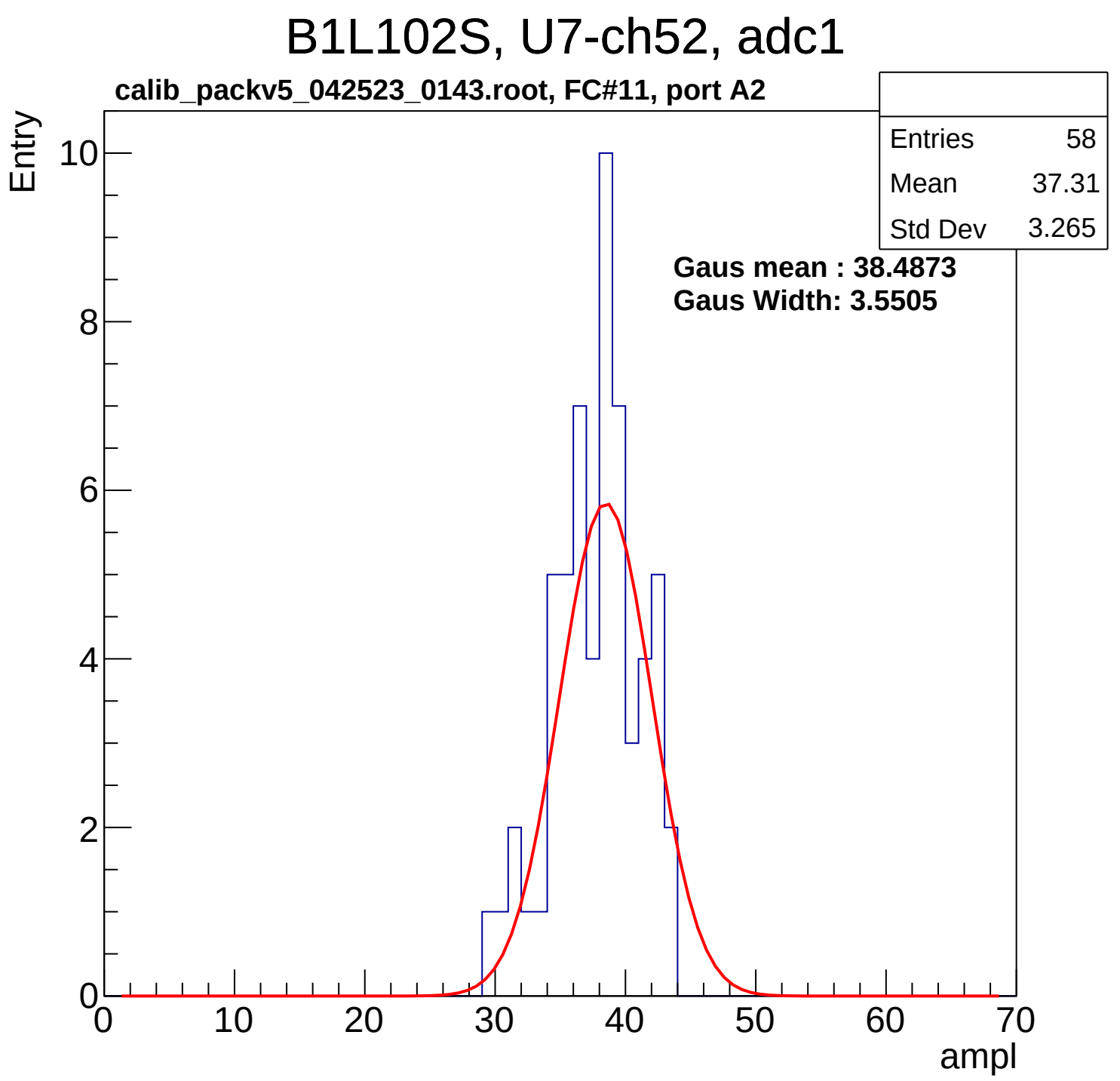
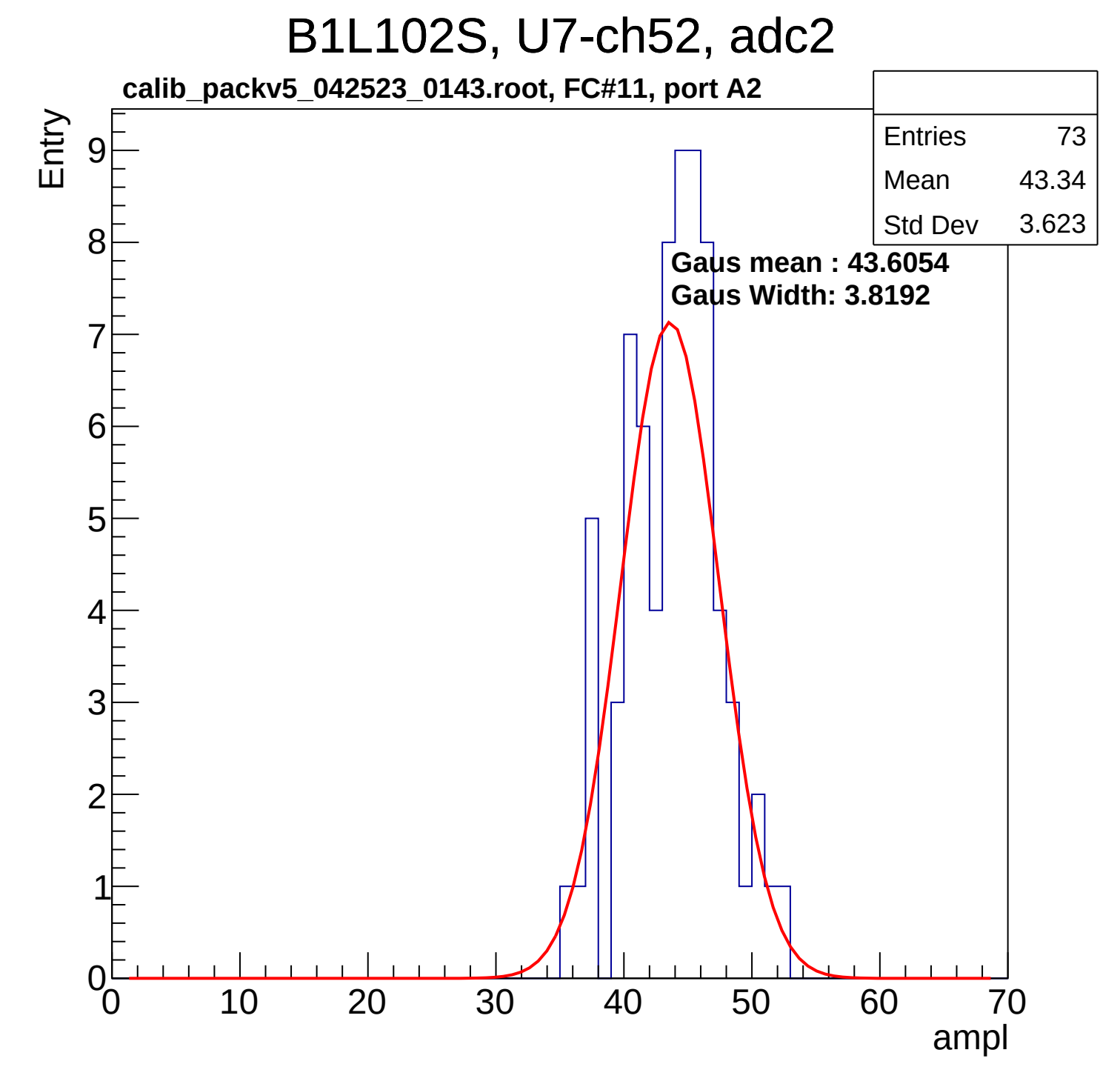
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L102S, U7-ch52, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 58
Mean 37.31
Std Dev 3.265
Gaus mean : 38.4873
Gaus Width: 3.5505
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L102S, U7-ch52, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 73
Mean 43.34
Std Dev 3.623
Gaus mean : 43.6054
Gaus Width: 3.8192
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
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20
30
40
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60
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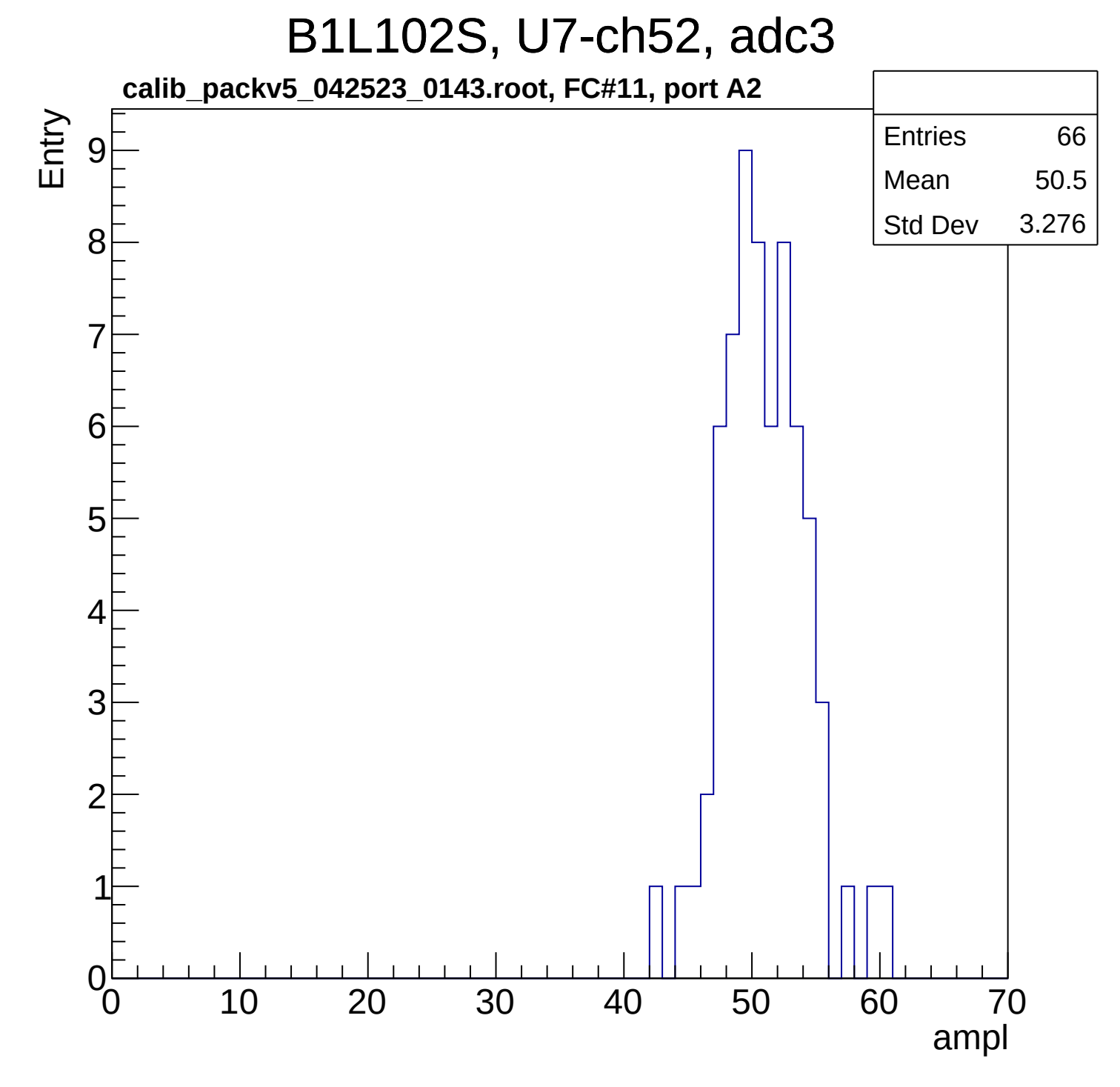
B1L102S, U7-ch52, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 66
Mean 50.5
Std Dev 3.276
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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40
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60
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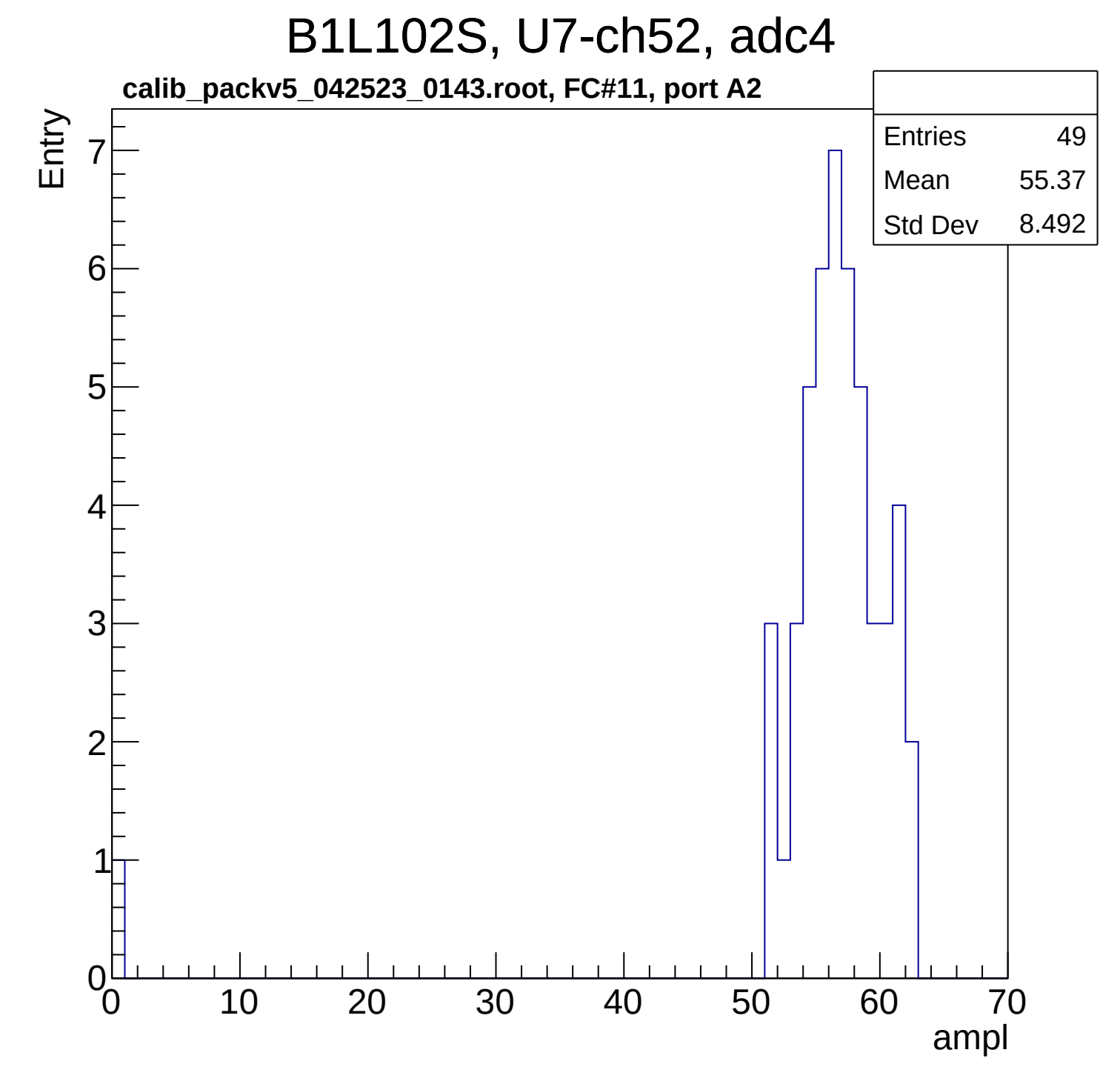
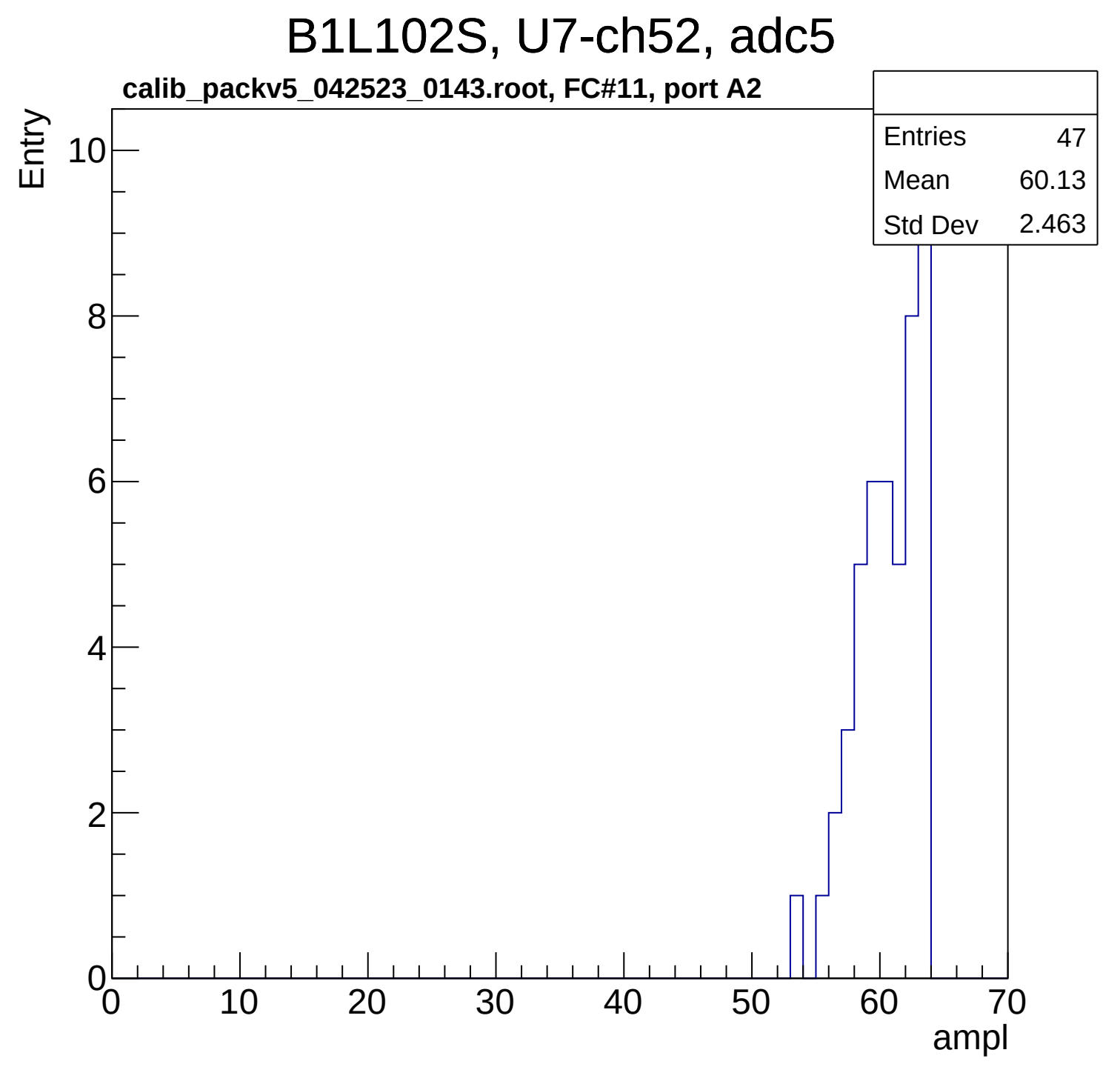

B1L102S, U7-ch52, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 49
Mean 55.37
Std Dev 8.492
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L102S, U7-ch52, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 47
Mean 60.13
Std Dev 2.463
Entry
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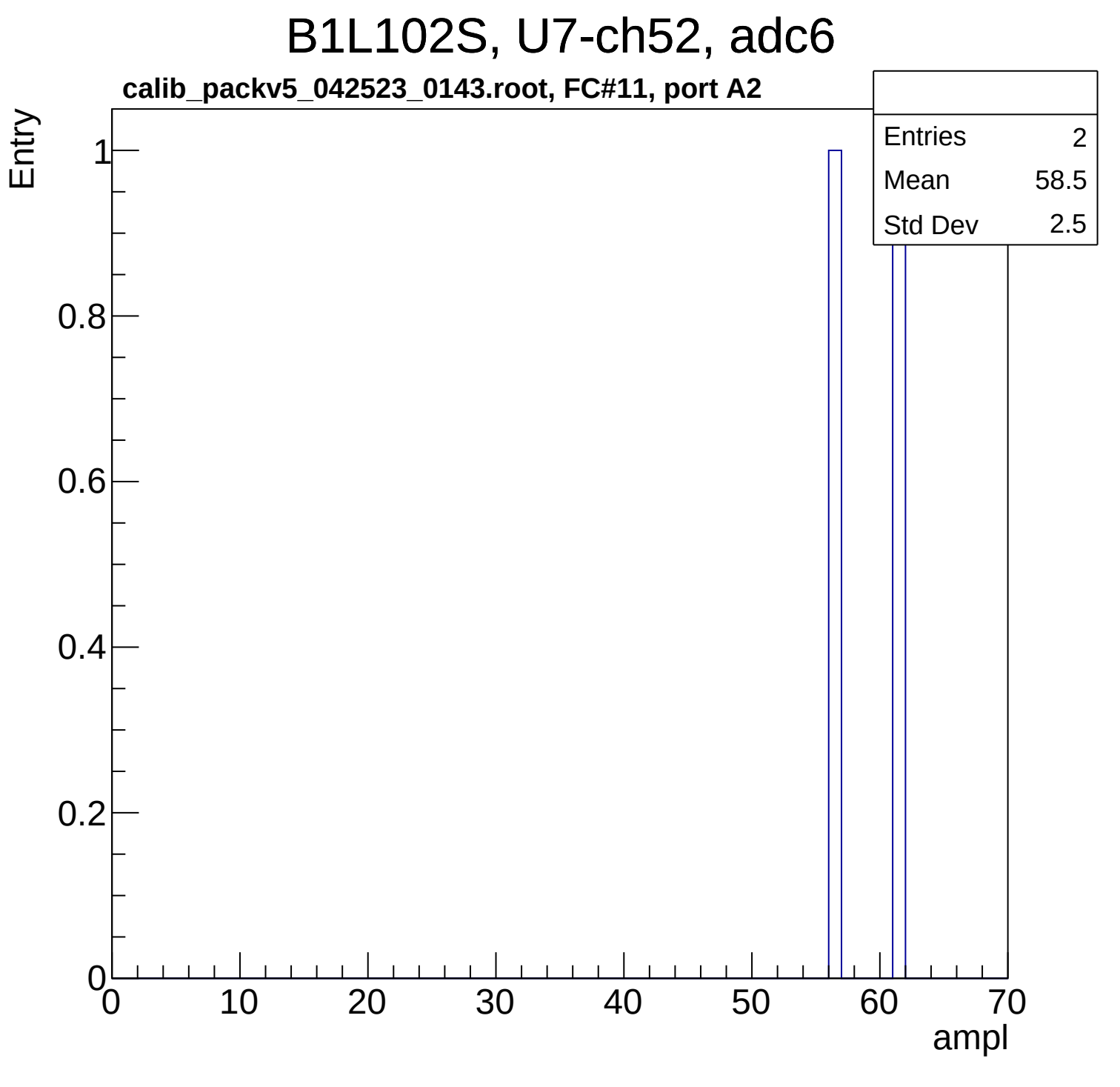
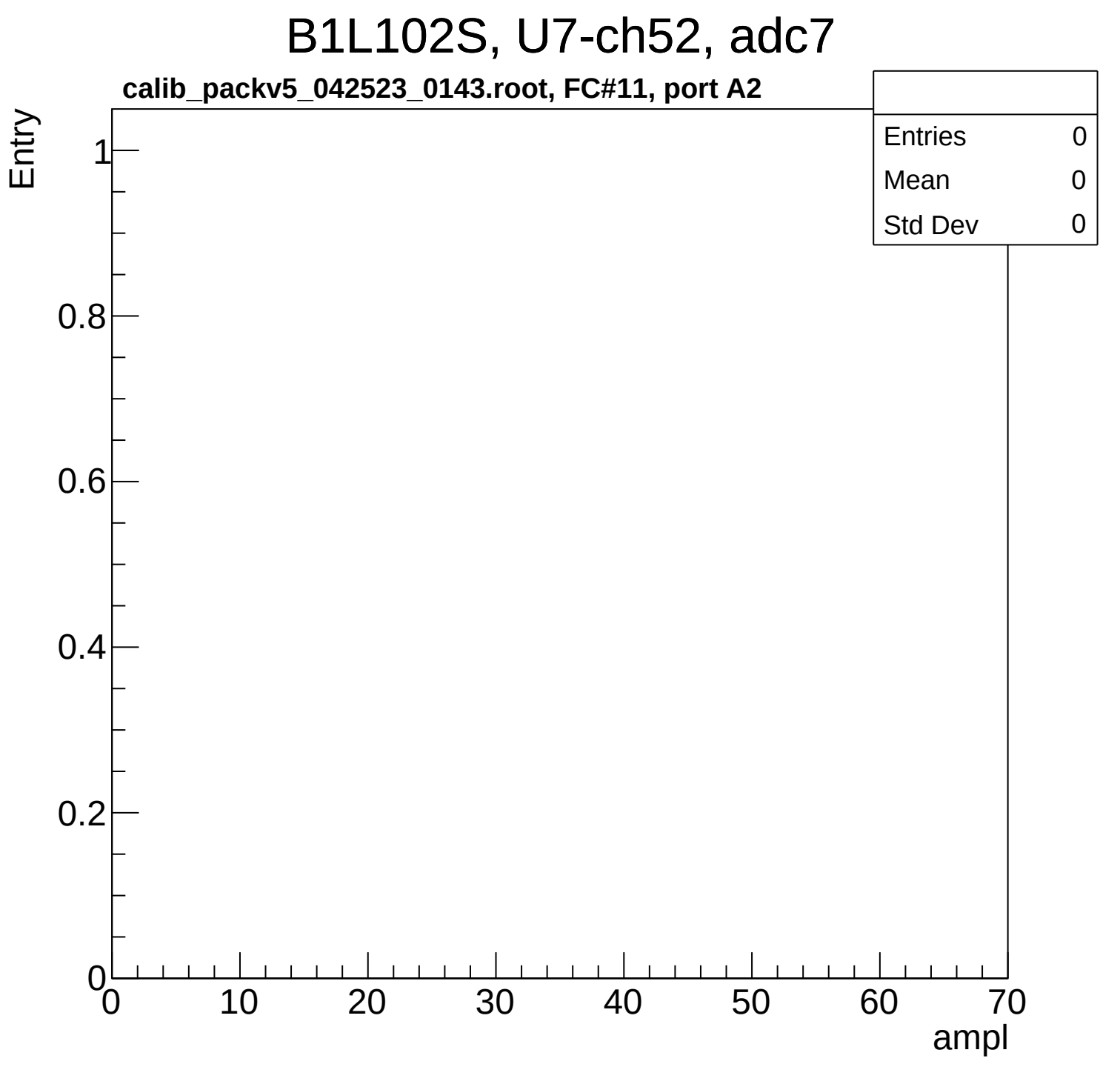
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L102S, U7-ch52, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 2
Mean 58.5
Std Dev 2.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U7-ch52, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 0
Mean 0
Std Dev 0
Entry
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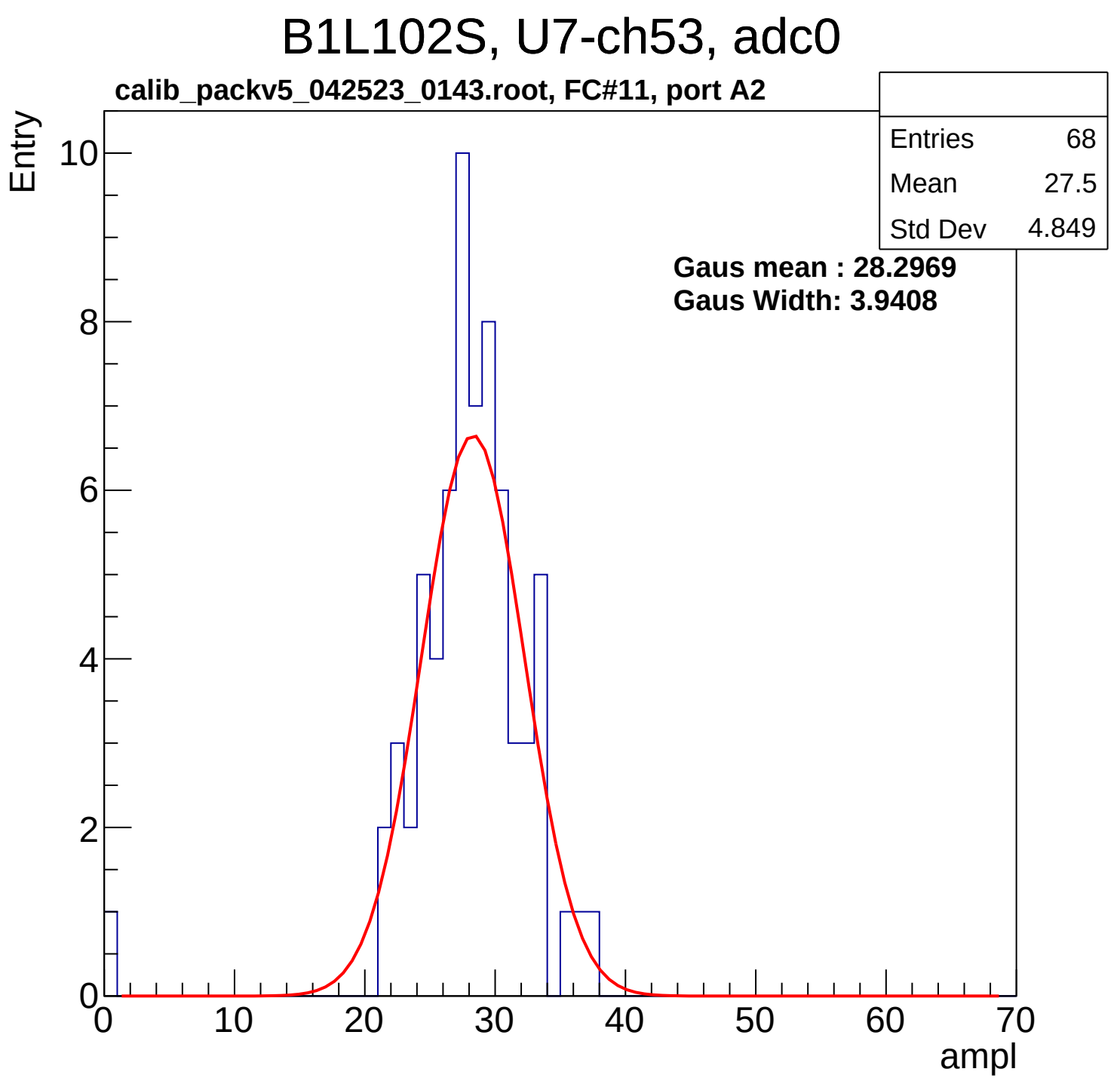
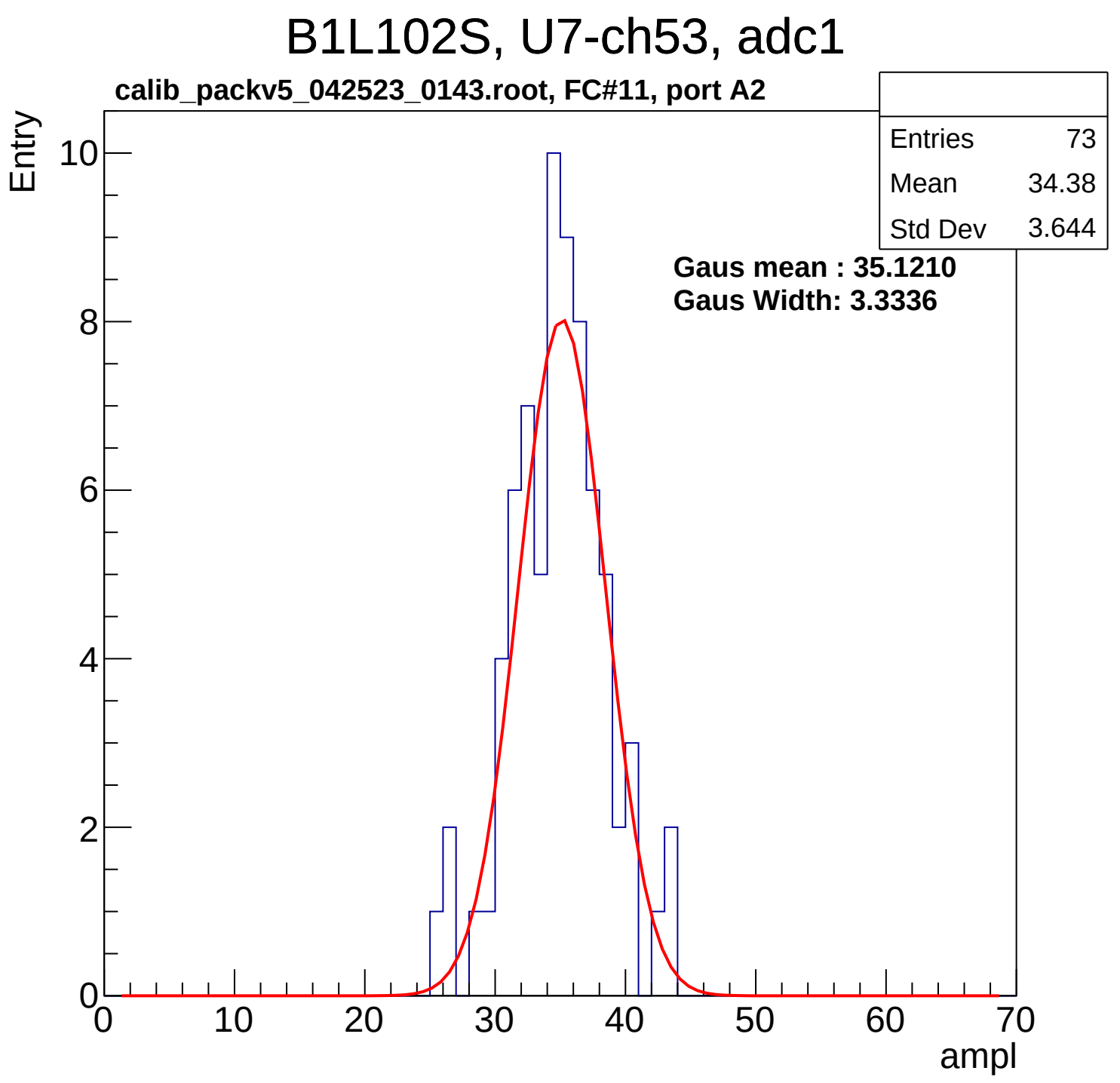
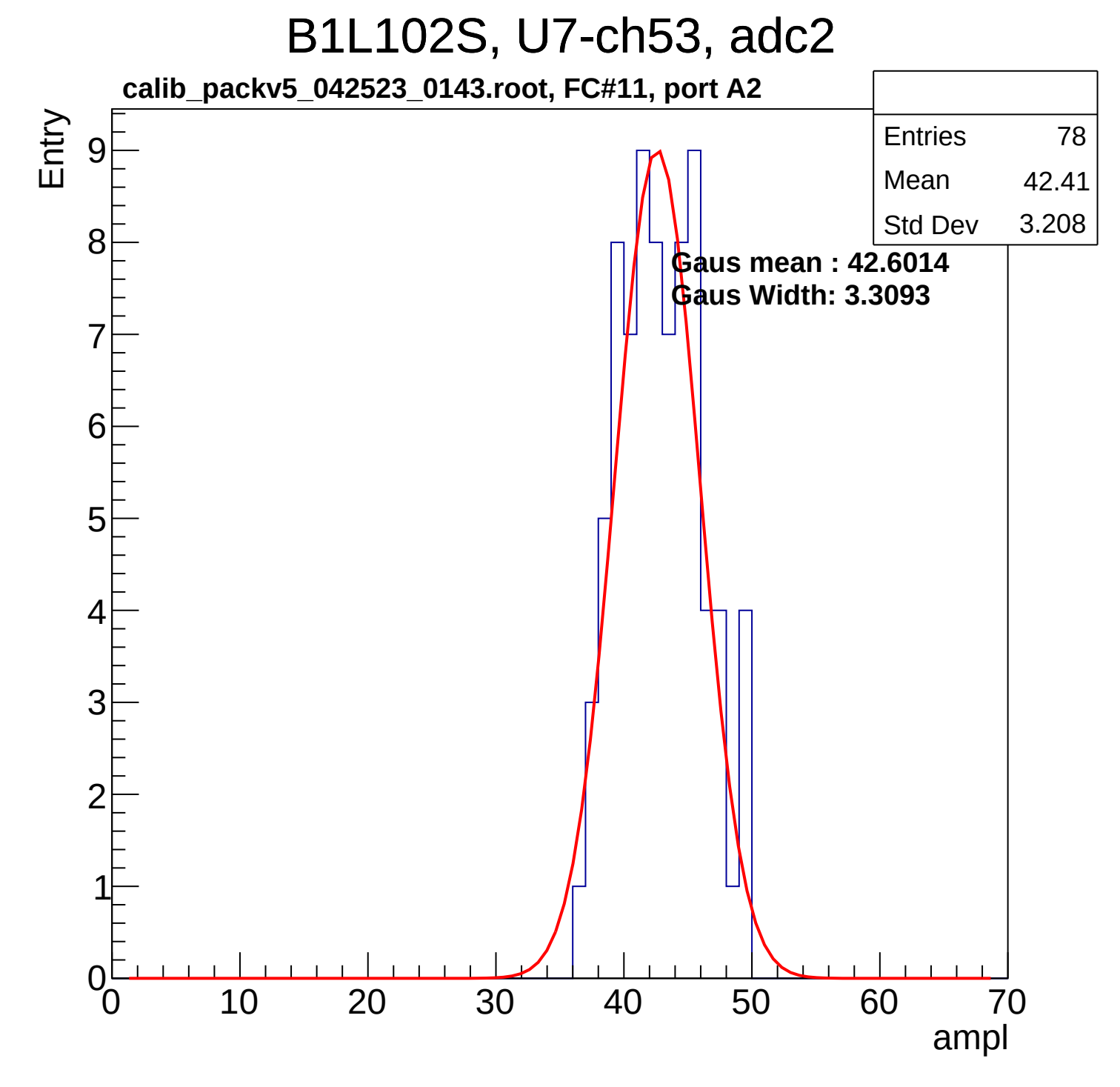
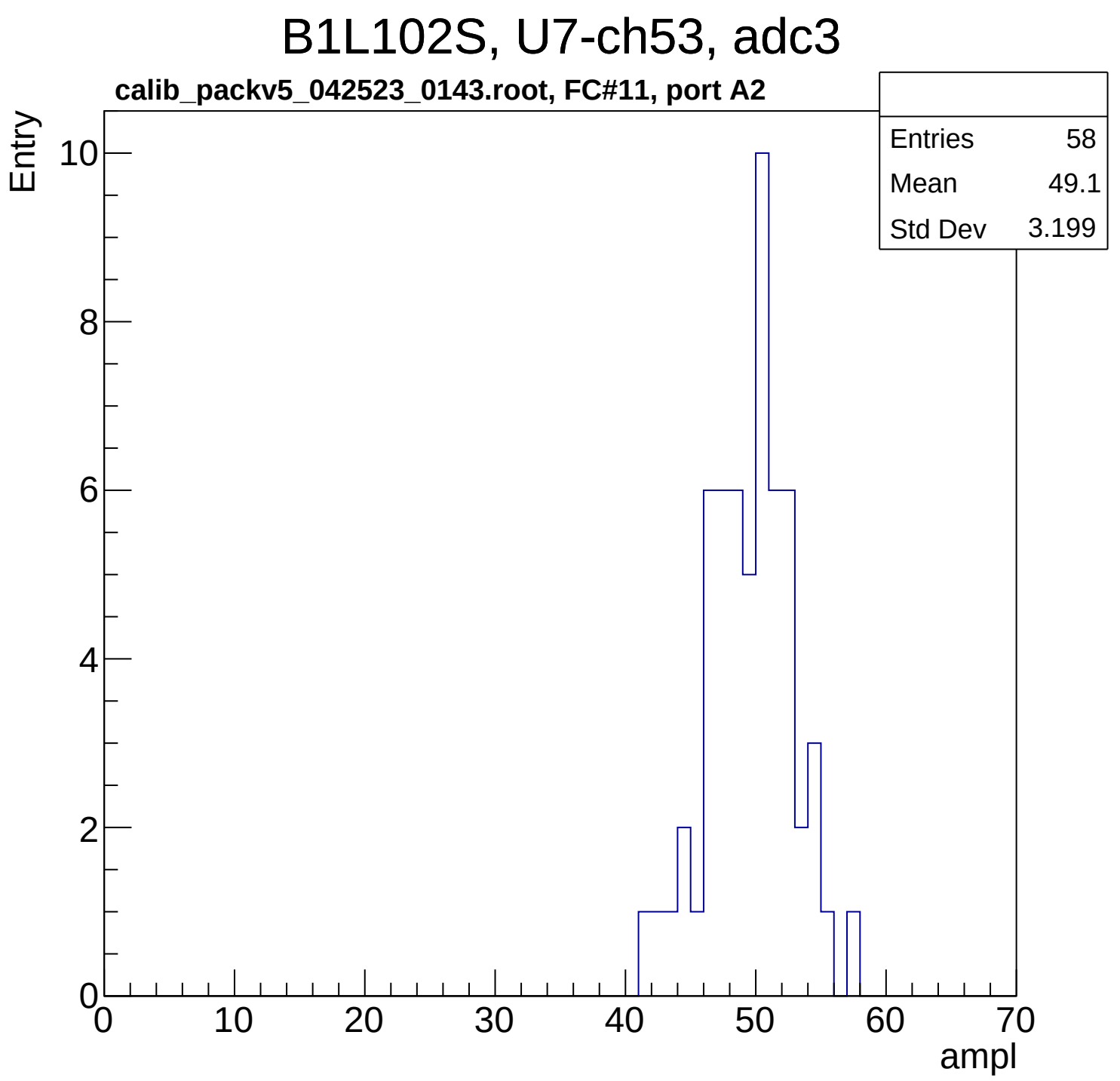
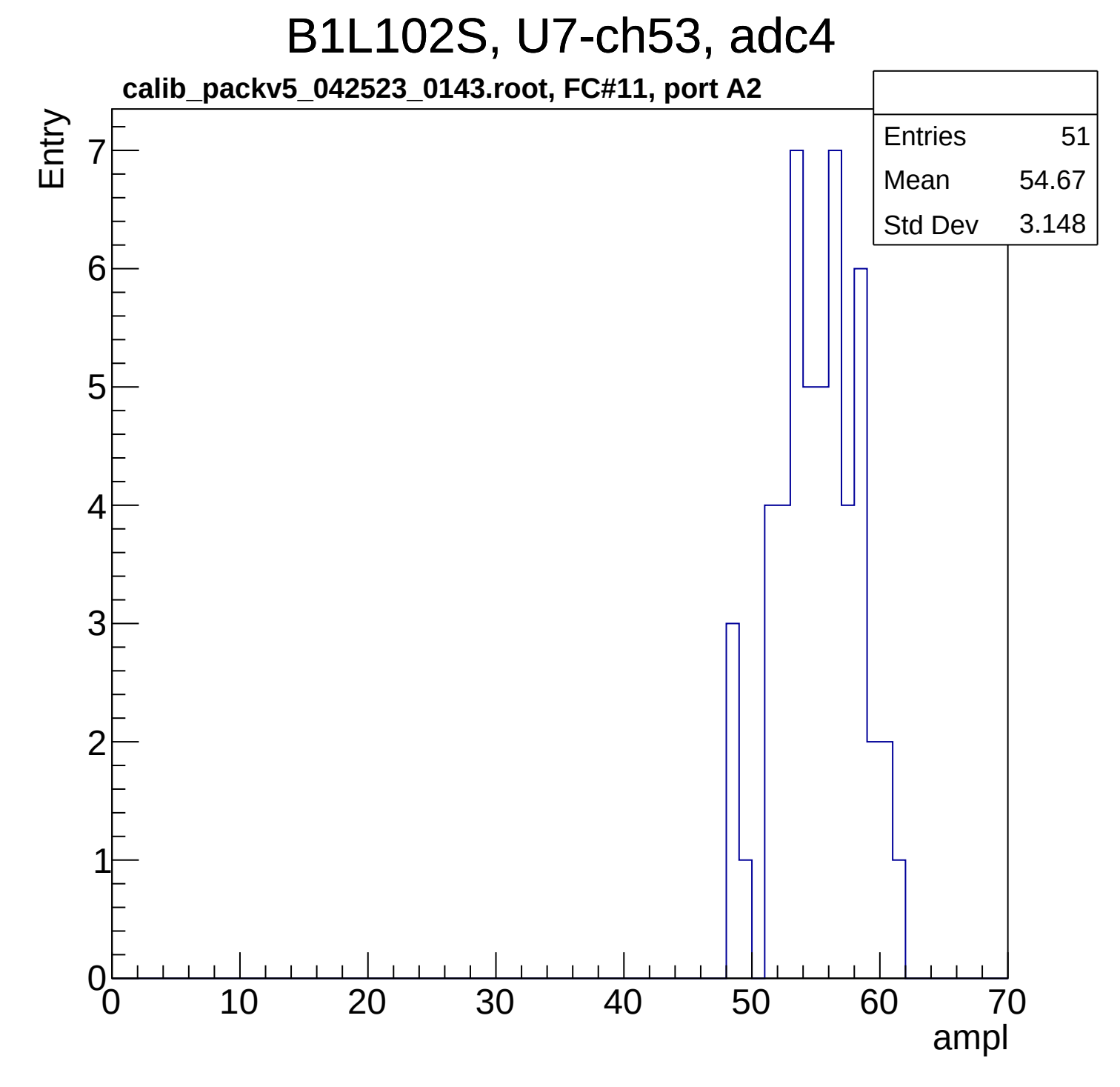
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U7-ch53, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 68
Mean 27.5
Std Dev 4.849
Gaus mean : 28.2969
Gaus Width: 3.9408
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L102S, U7-ch53, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 73
Mean 34.38
Std Dev 3.644
Gaus mean : 35.1210
Gaus Width: 3.3336
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L102S, U7-ch53, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 78
Mean 42.41
Std Dev 3.208
Gaus mean : 42.6014
Gaus Width: 3.3093
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L102S, U7-ch53, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 58
Mean 49.1
Std Dev 3.199
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L102S, U7-ch53, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 51
Mean 54.67
Std Dev 3.148
Entry
ampl
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3
4
5
6
7
0
10
20
30
40
50
60
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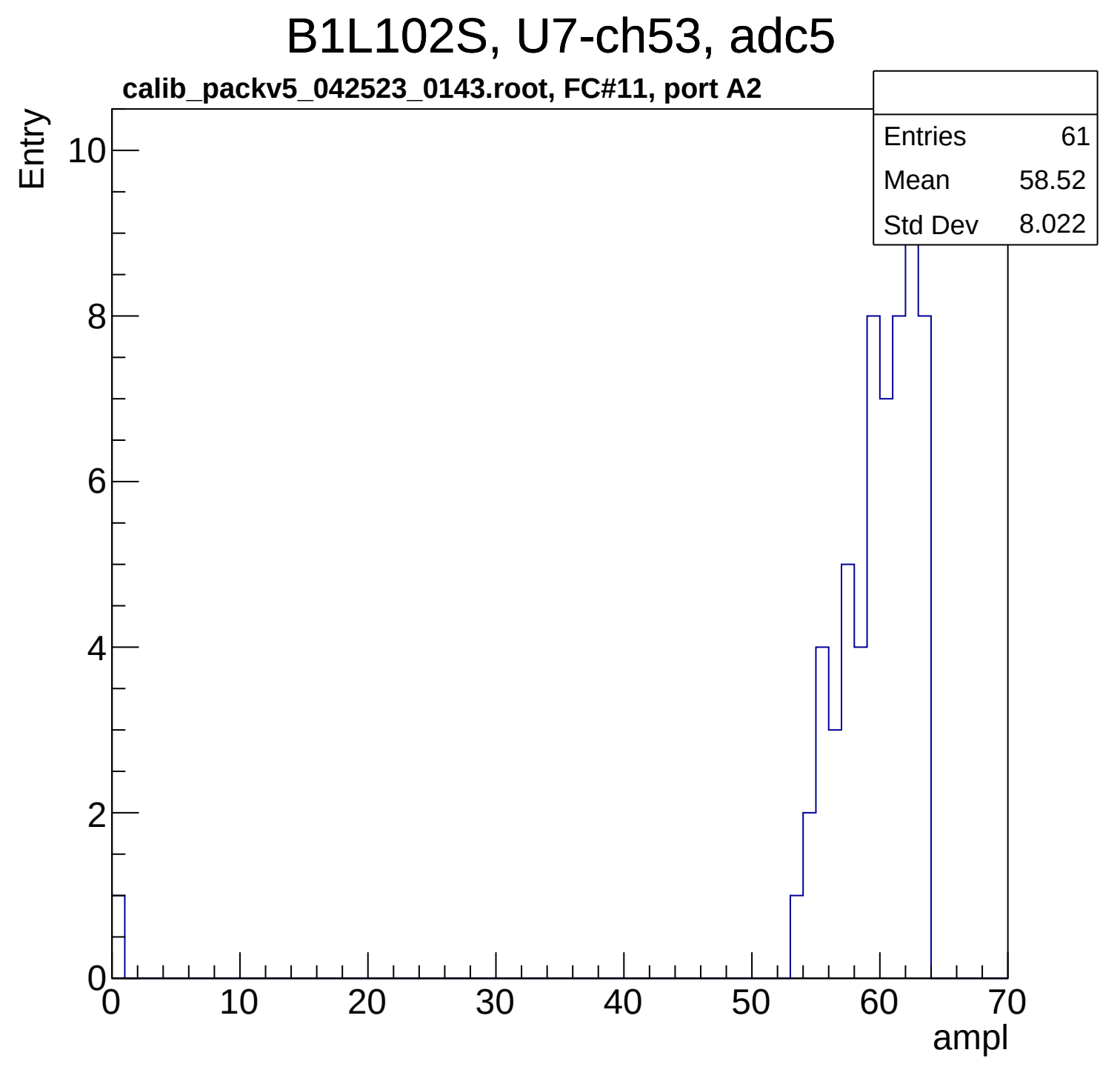
B1L102S, U7-ch53, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 61
Mean 58.52
Std Dev 8.022
Entry
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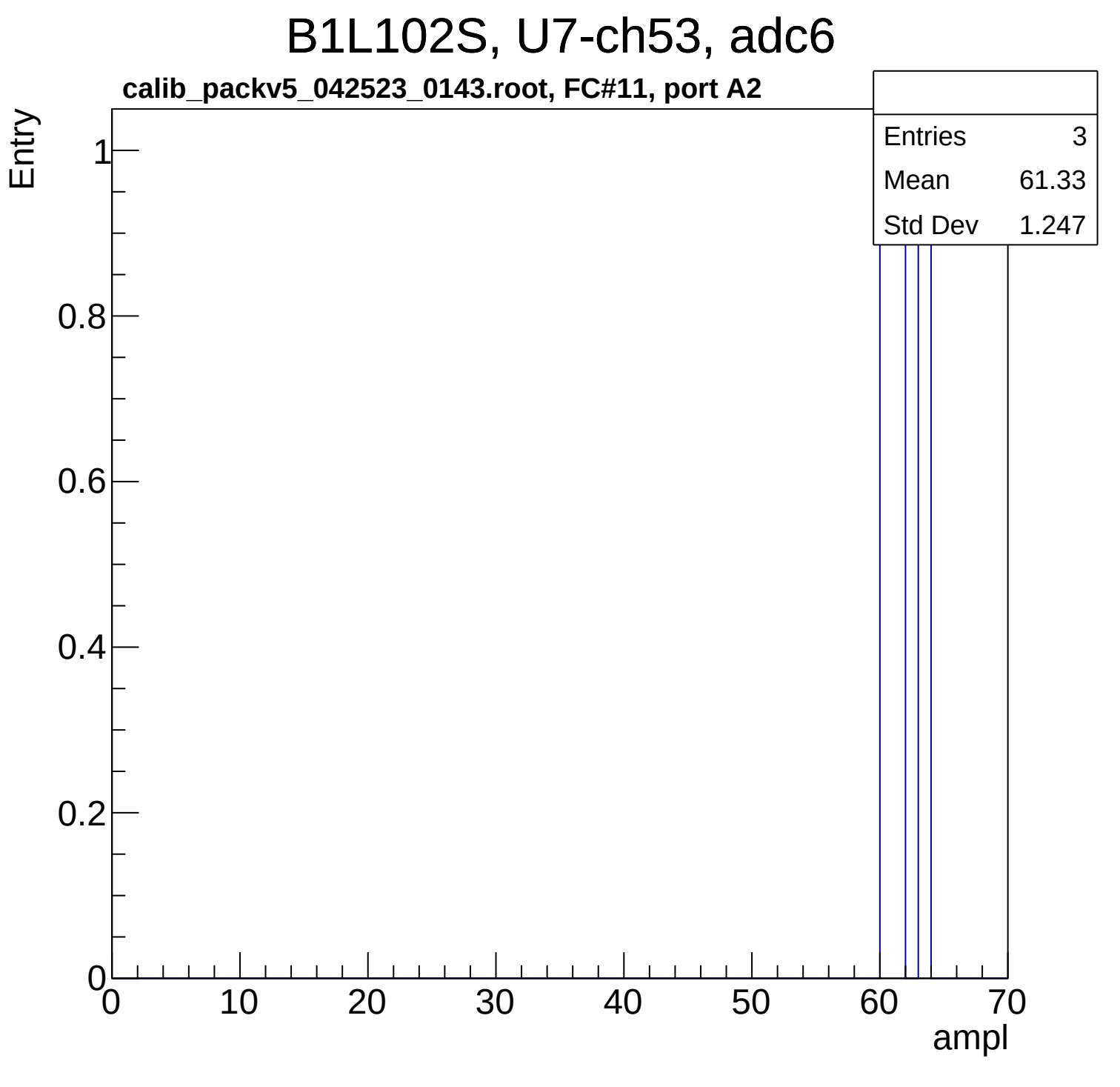
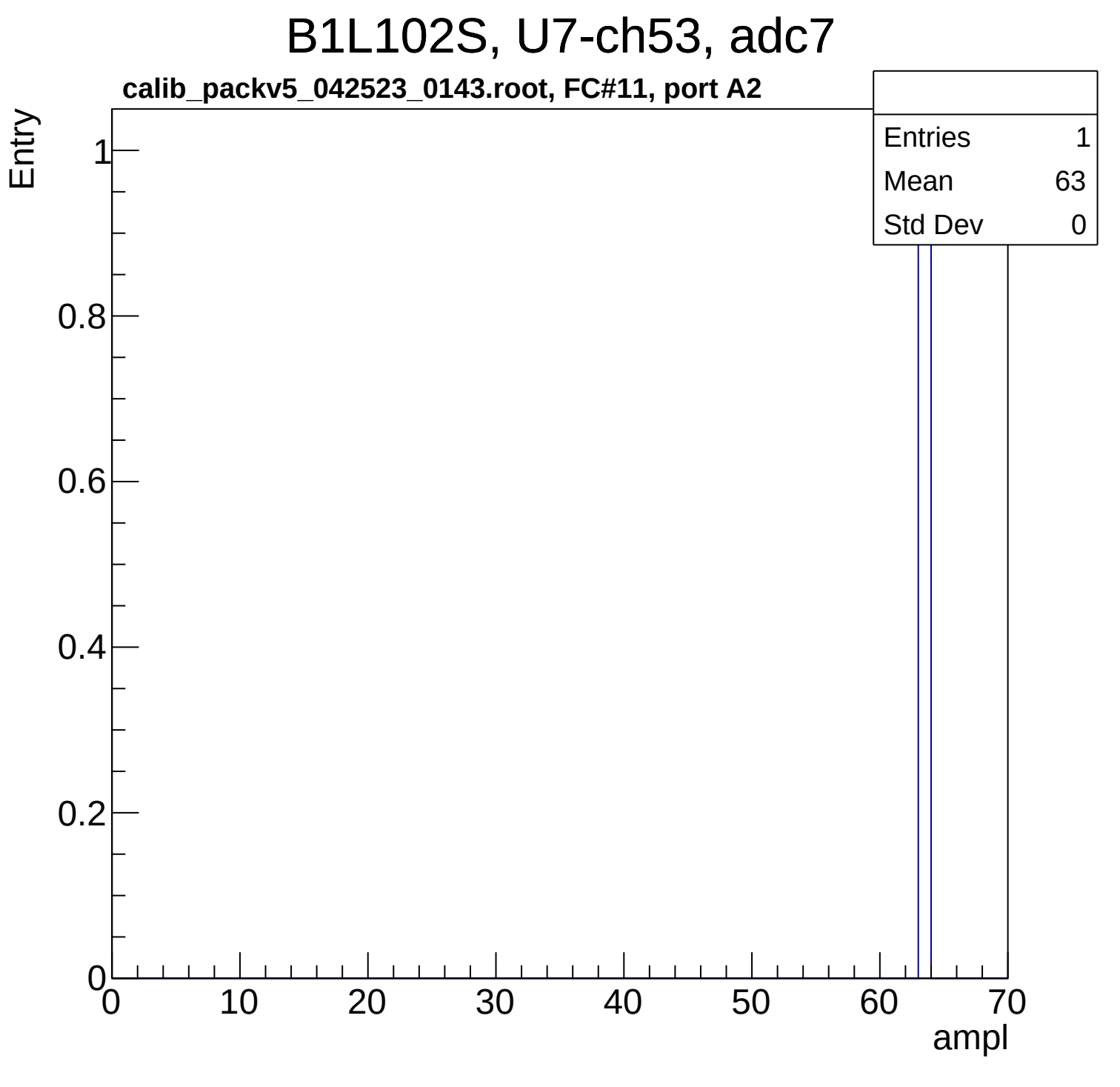
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L102S, U7-ch53, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 3
Mean 61.33
Std Dev 1.247
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70


B1L102S, U7-ch53, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 1
Mean 63
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
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10
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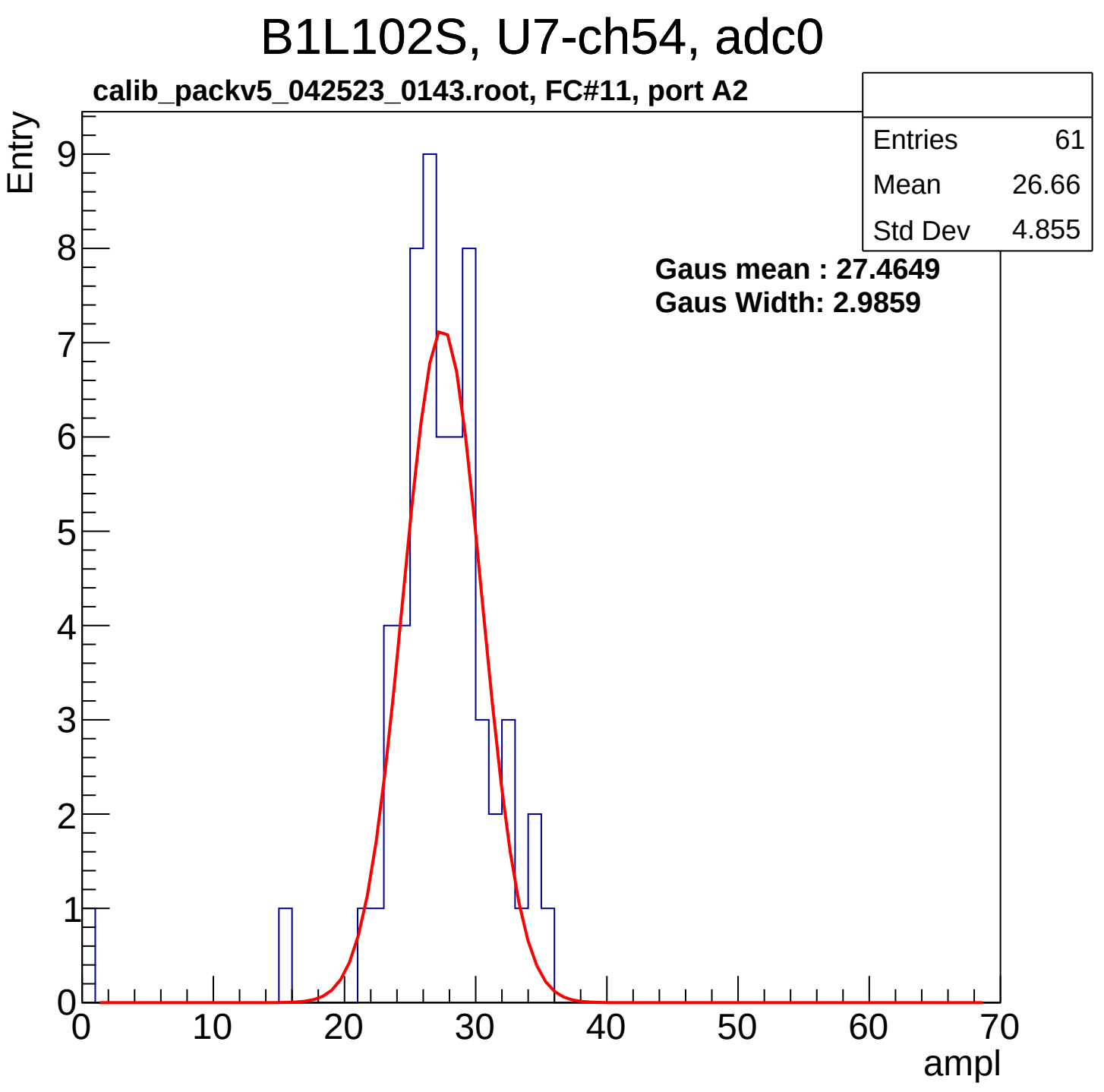
70
ampl


B1L102S, U7-ch54, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 61
Mean 26.66
Std Dev 4.855
Gaus mean : 27.4649
Gaus Width: 2.9859
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
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40
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60
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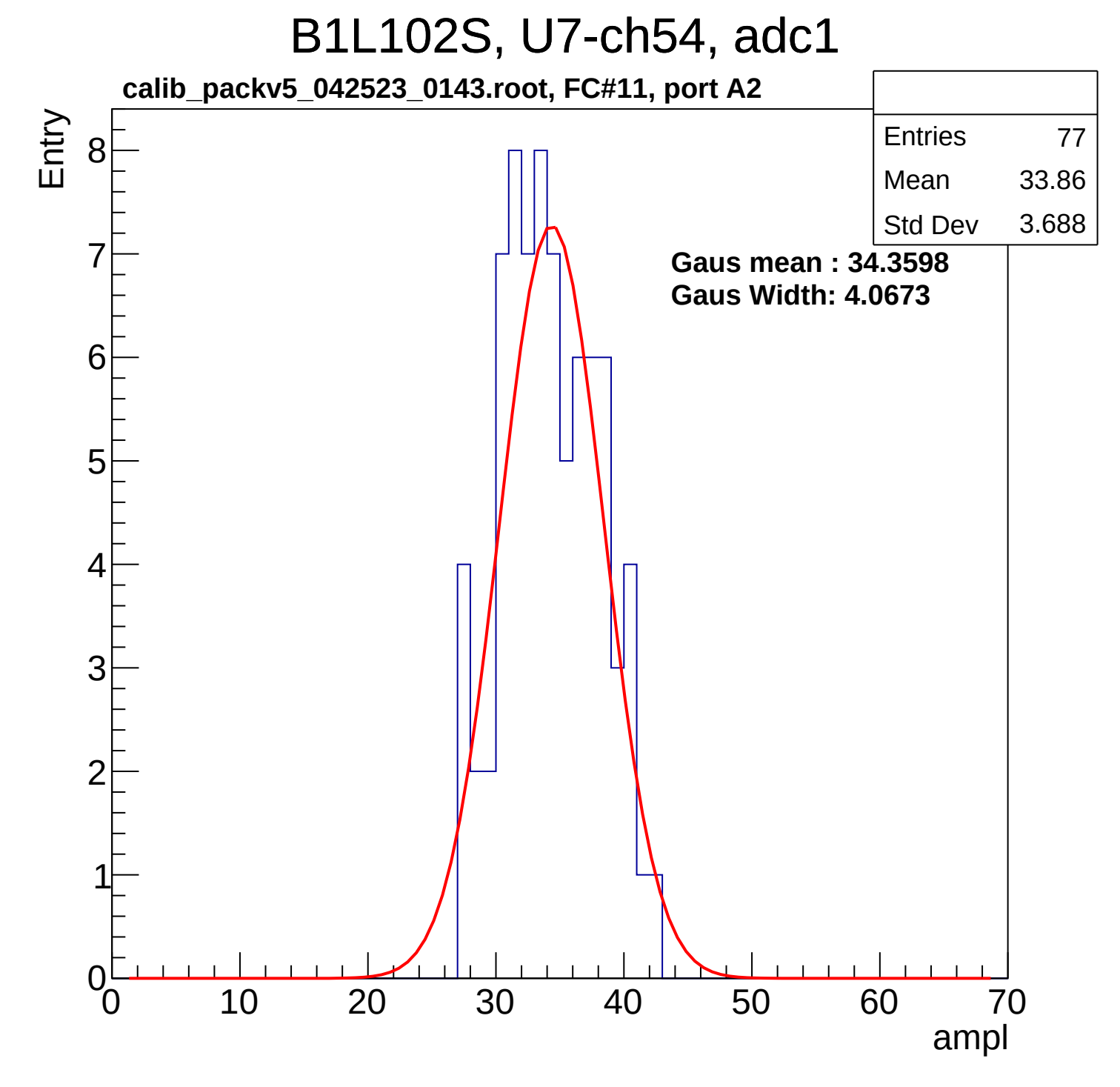
B1L102S, U7-ch54, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 77
Mean 33.86
Std Dev 3.688
Gaus mean : 34.3598
Gaus Width: 4.0673
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
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40
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60
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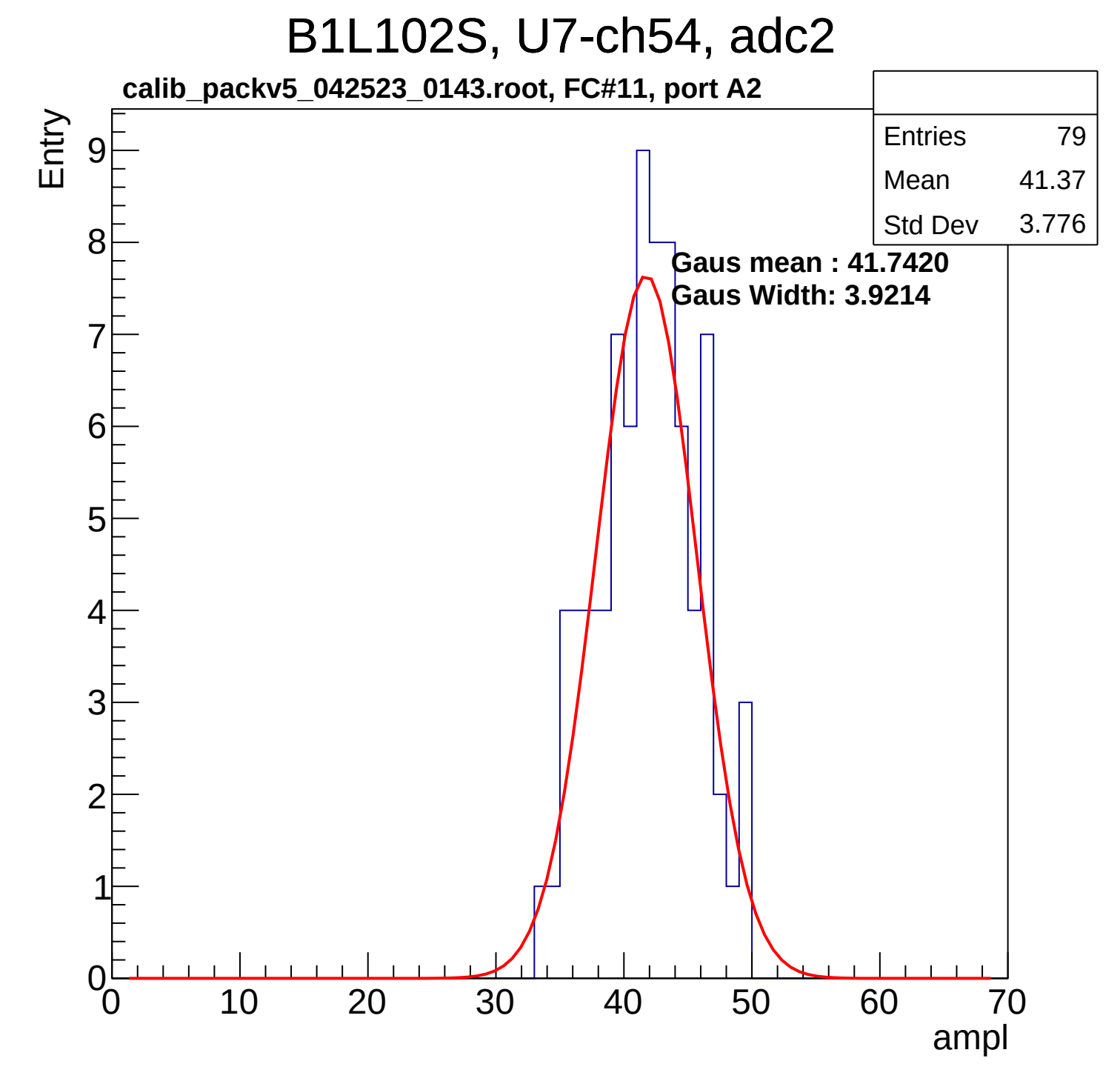
B1L102S, U7-ch54, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 79
Mean 41.37
Std Dev 3.776
Gaus mean : 41.7420
Gaus Width: 3.9214
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
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20
30
40
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60
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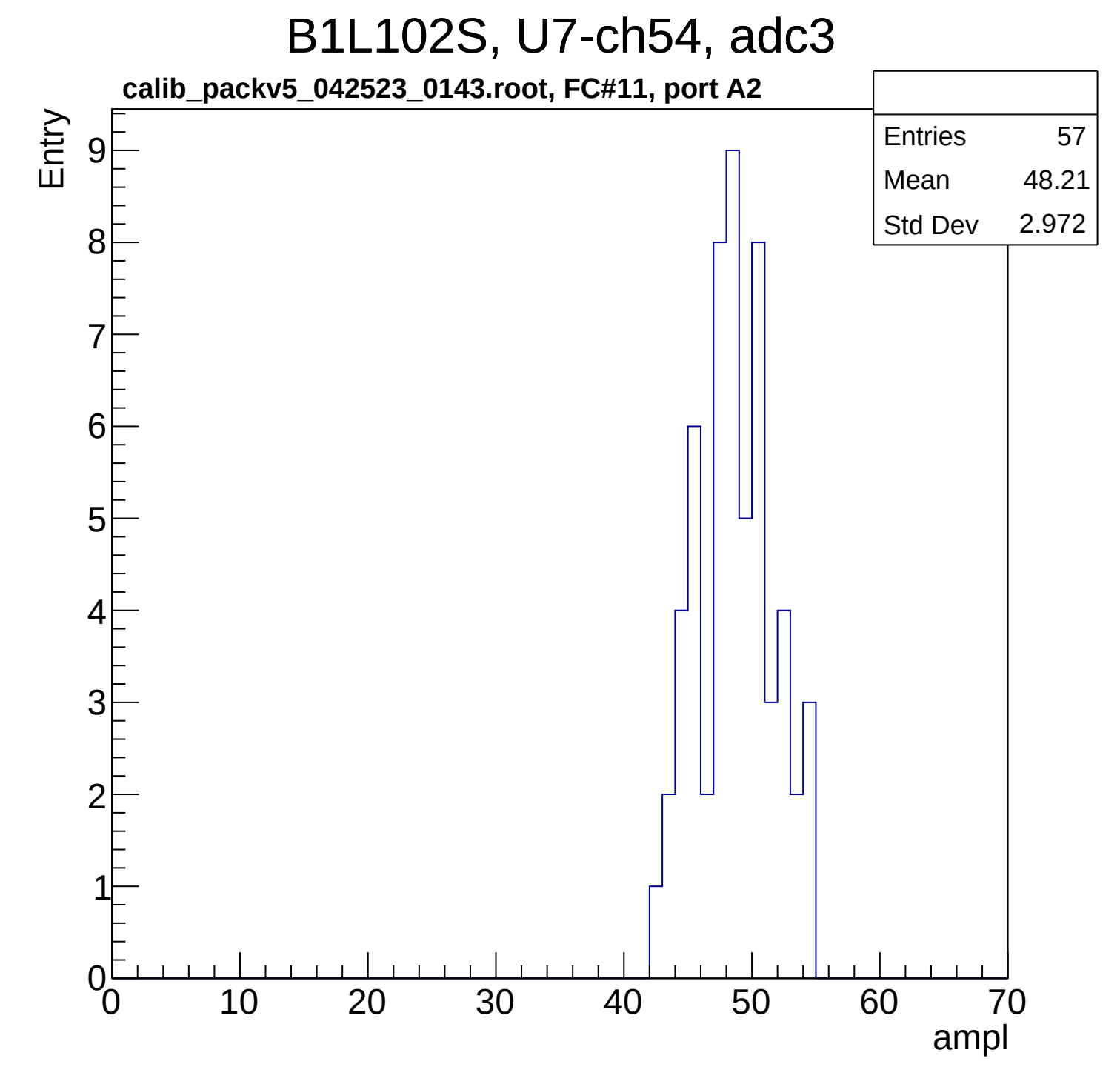
B1L102S, U7-ch54, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 57
Mean 48.21
Std Dev 2.972
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
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60
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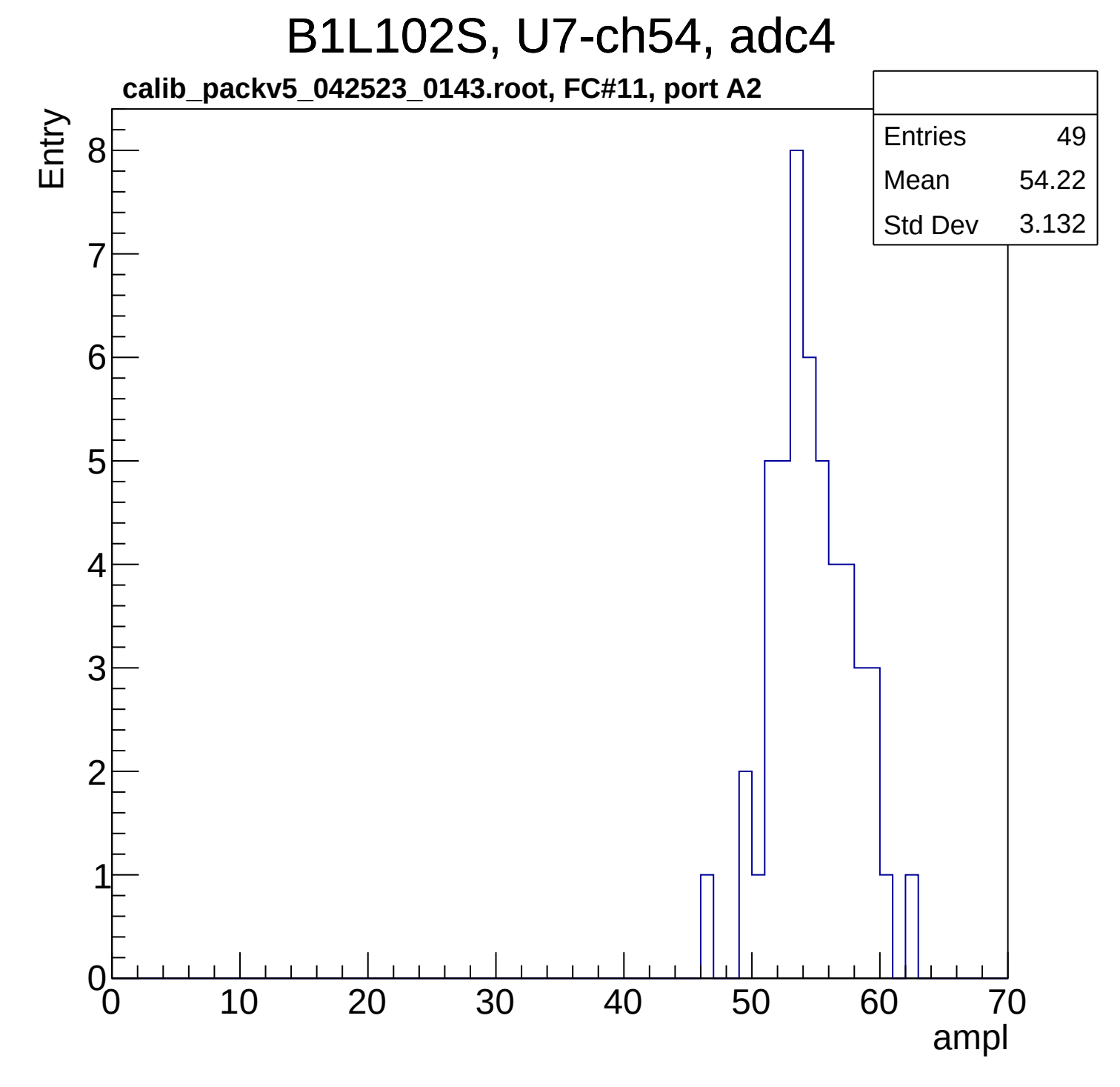
B1L102S, U7-ch54, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 49
Mean 54.22
Std Dev 3.132
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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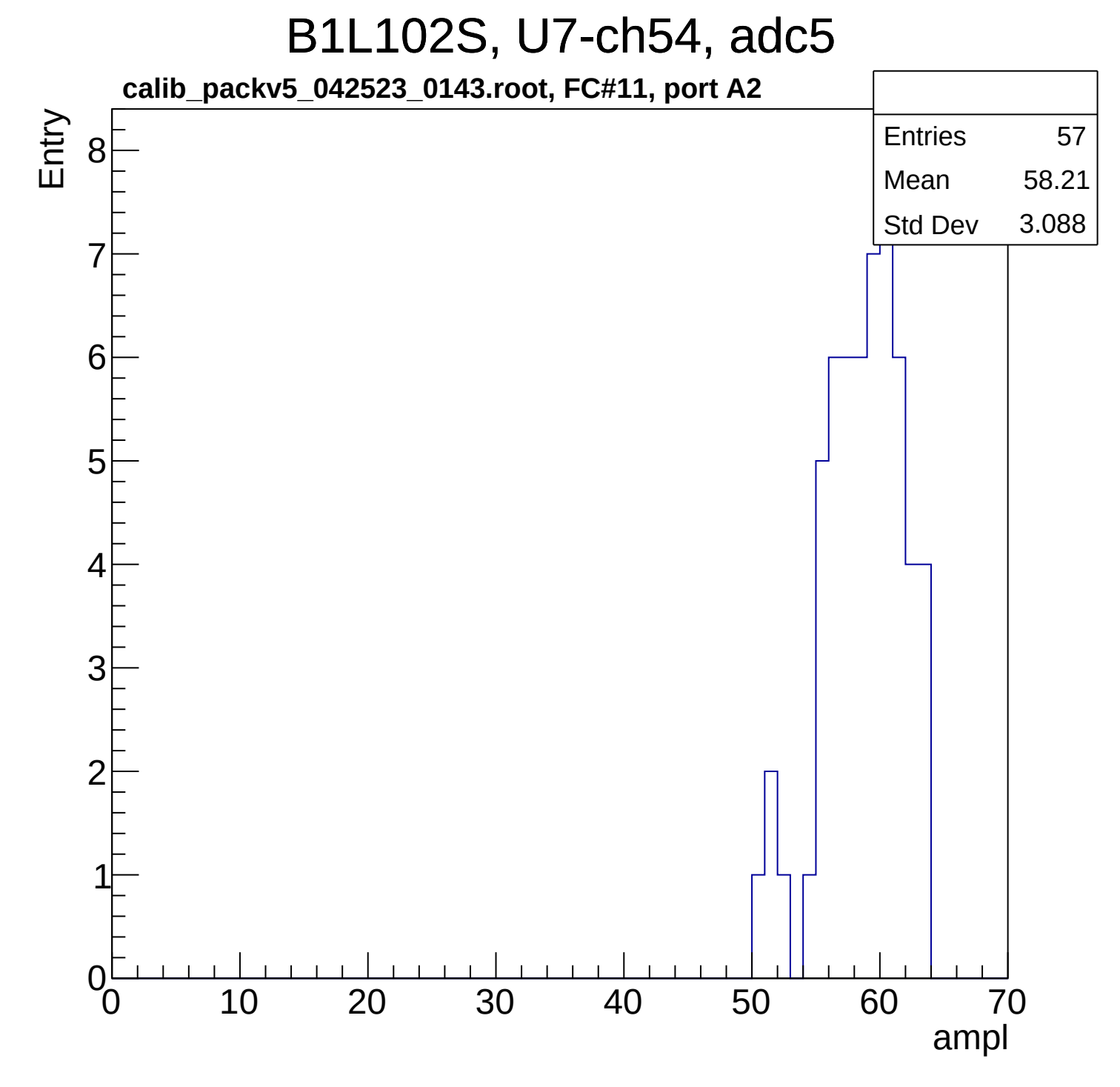
B1L102S, U7-ch54, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 57
Mean 58.21
Std Dev 3.088
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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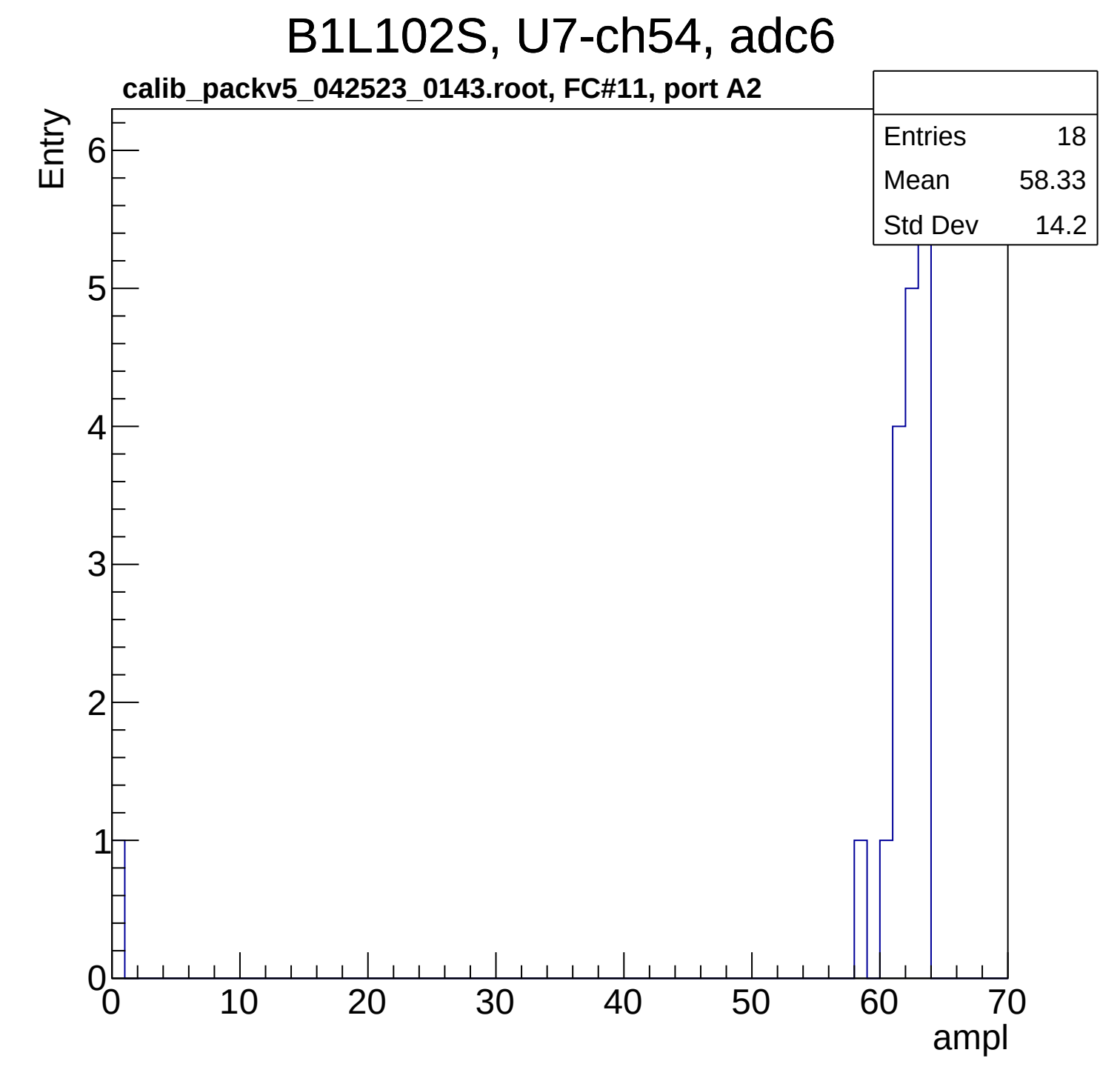
B1L102S, U7-ch54, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 18
Mean 58.33
Std Dev 14.2
Entry
ampl
0
1
2
3
4
5
6
0
10
20
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60
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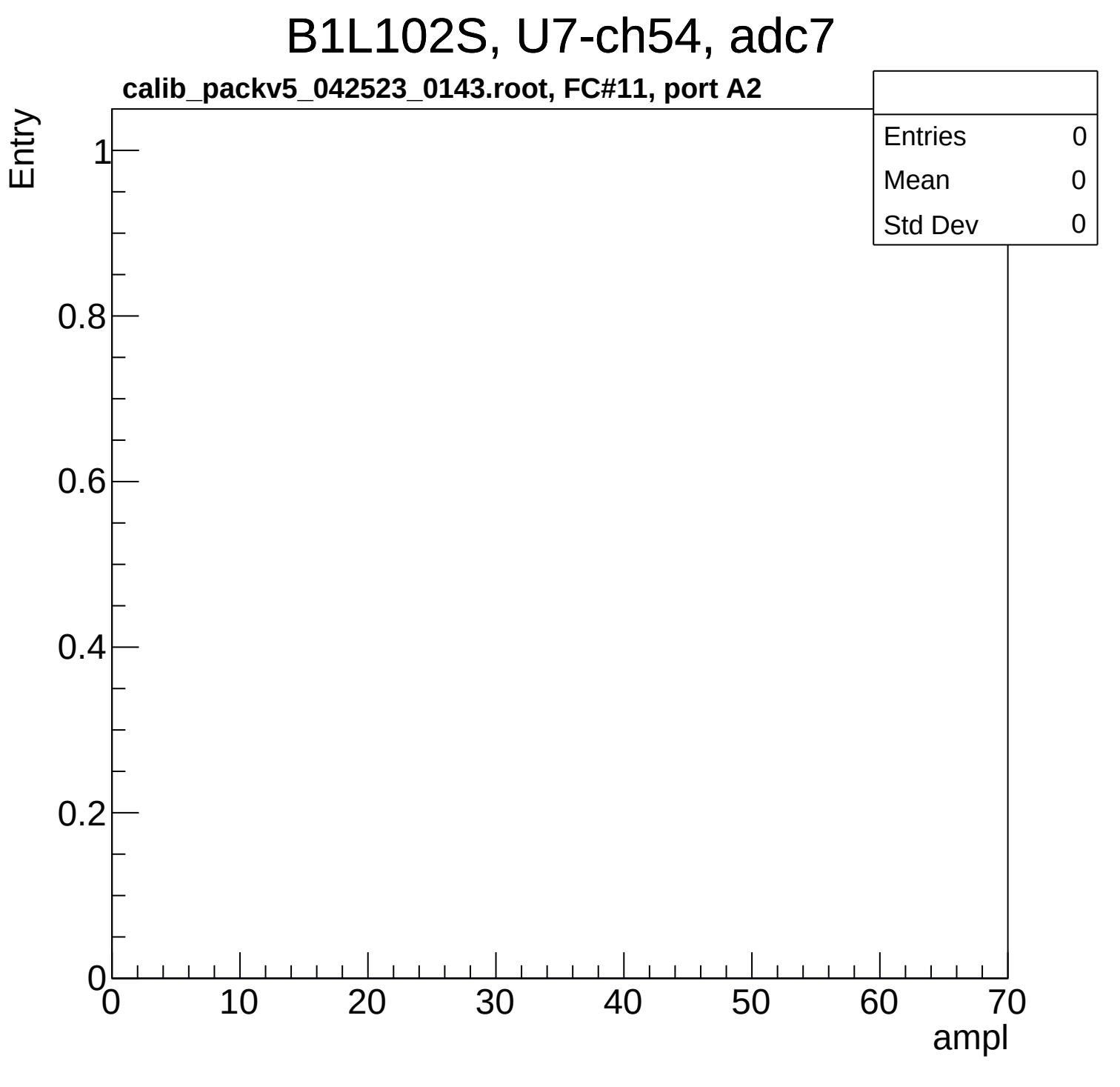
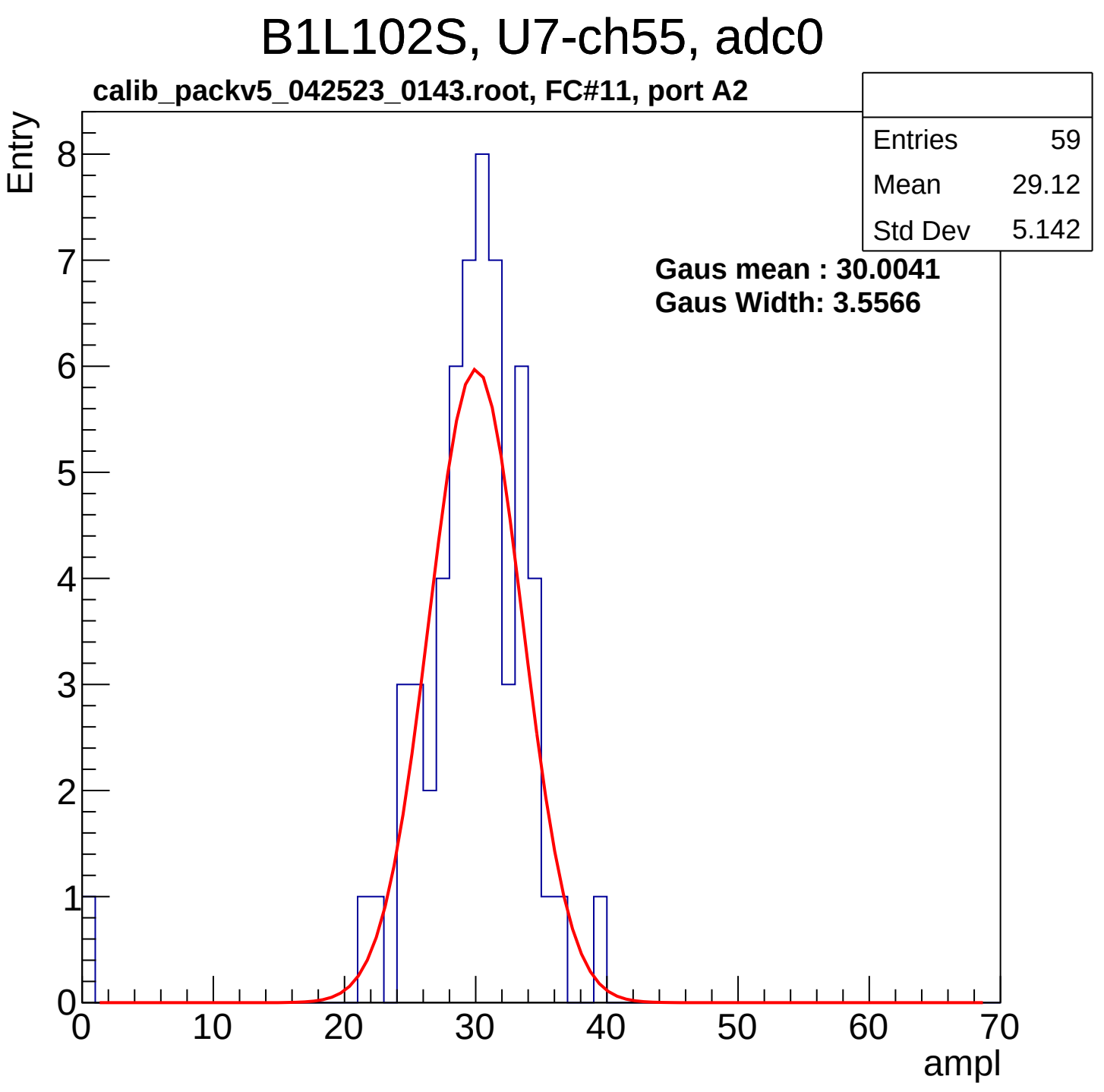
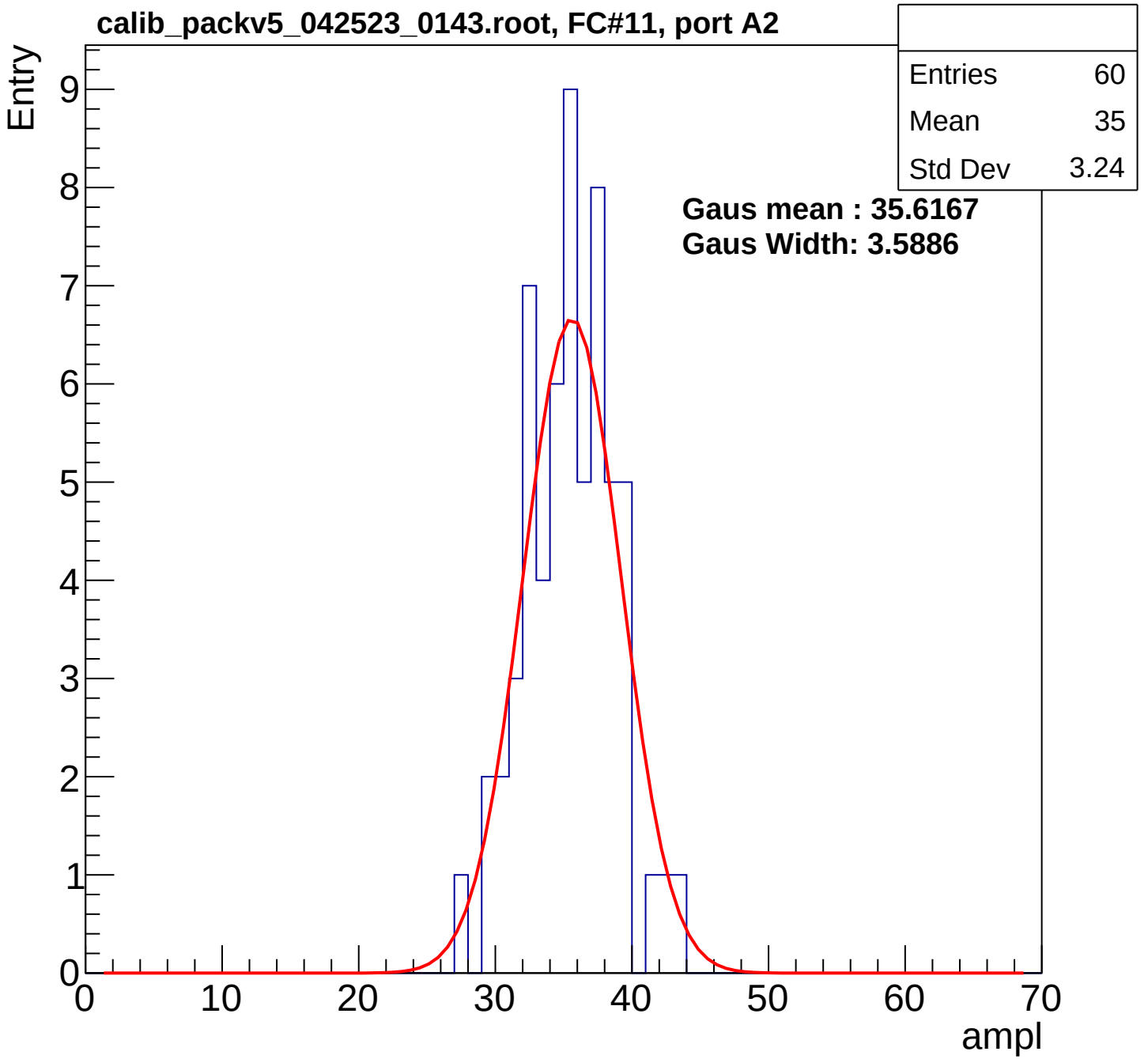

B1L102S, U7-ch54, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U7-ch55, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 59
Mean 29.12
Std Dev 5.142
Gaus mean : 30.0041
Gaus Width: 3.5566
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L102S, U7-ch55, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 60
Mean 35
Std Dev 3.24
Gaus mean : 35.6167
Gaus Width: 3.5886
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
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40
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60
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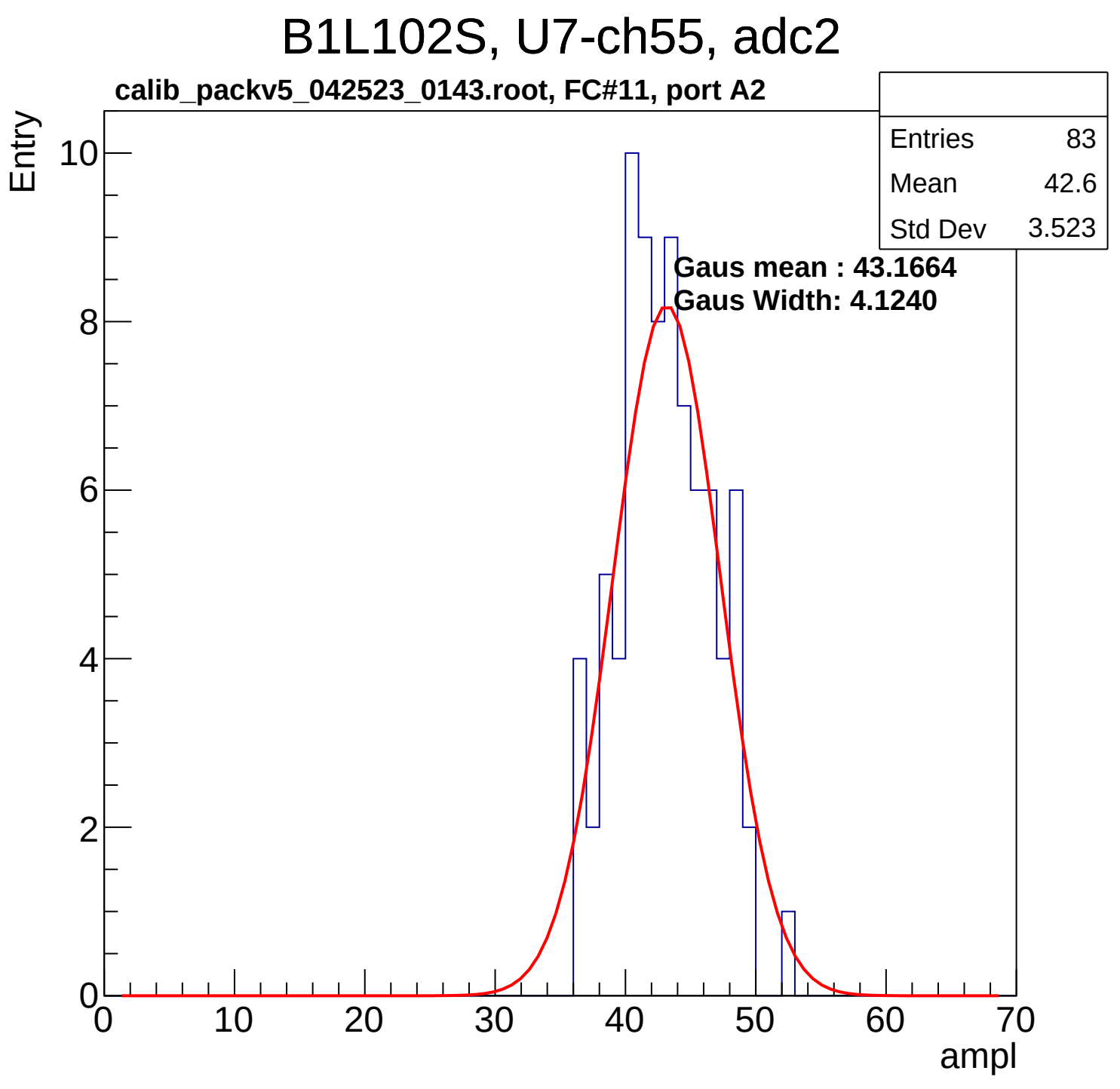
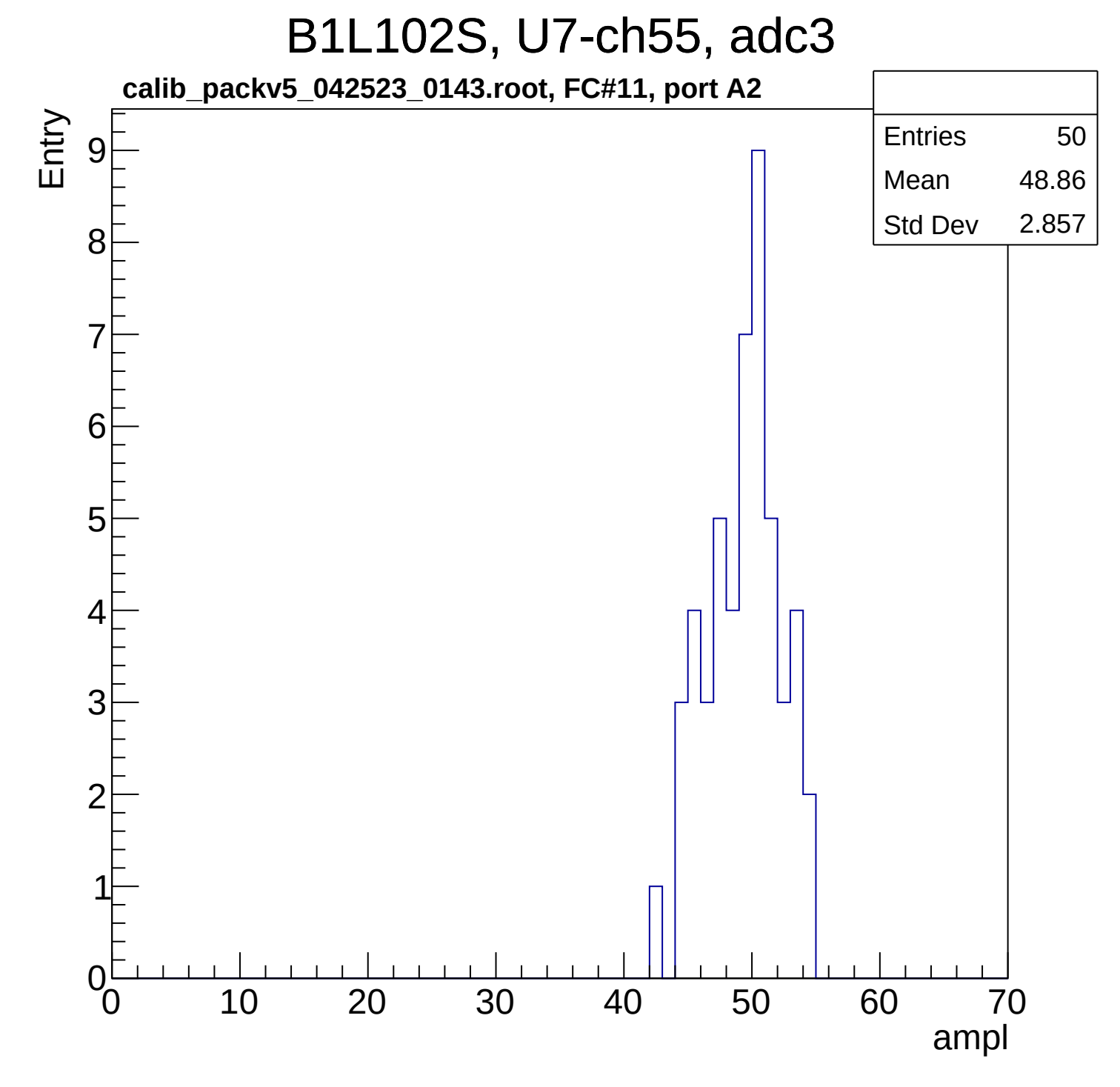

B1L102S, U7-ch55, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 83
Mean 42.6
Std Dev 3.523
Gaus mean : 43.1664
Gaus Width: 4.1240
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L102S, U7-ch55, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 50
Mean 48.86
Std Dev 2.857
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
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20
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40
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60
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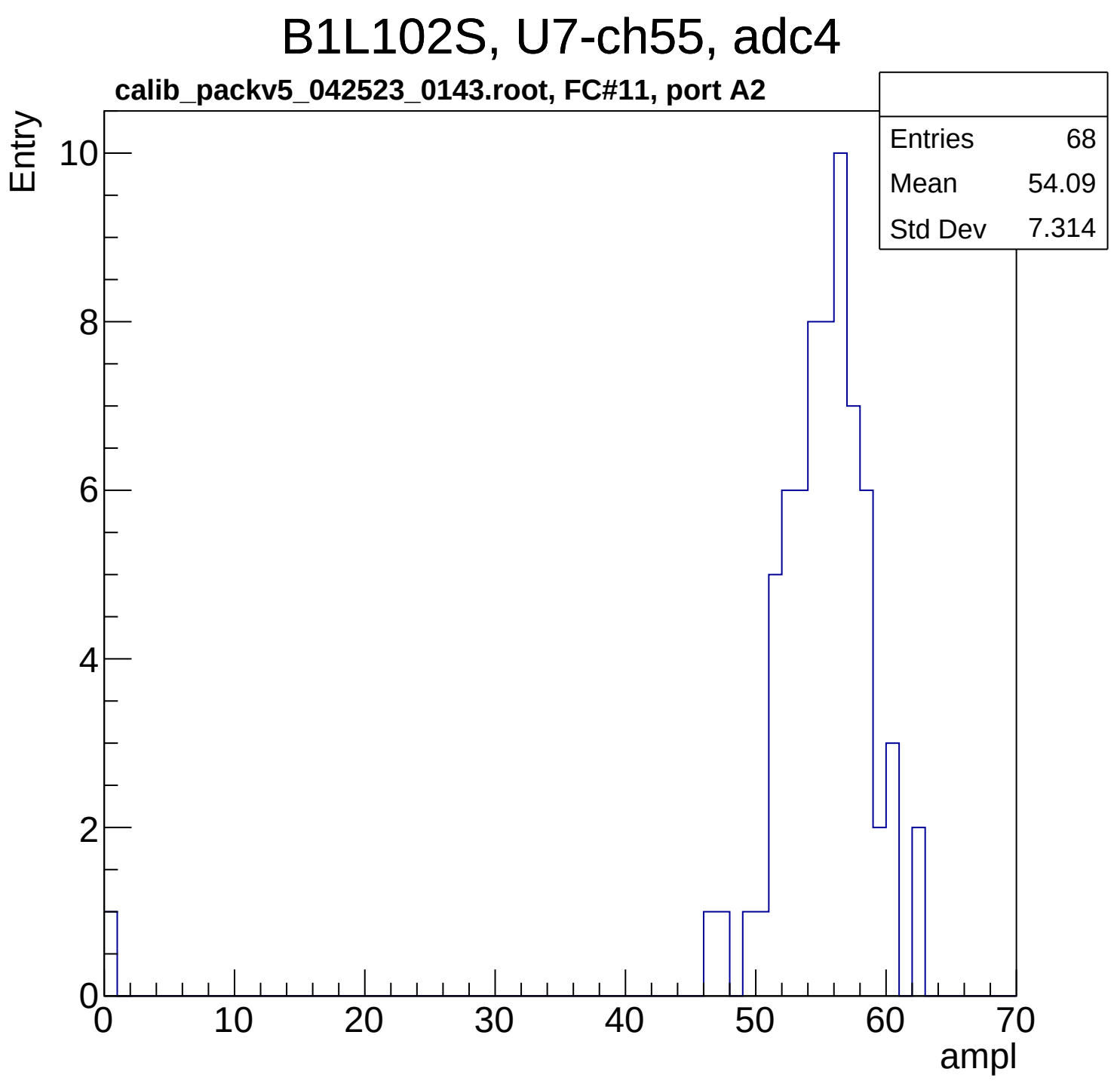
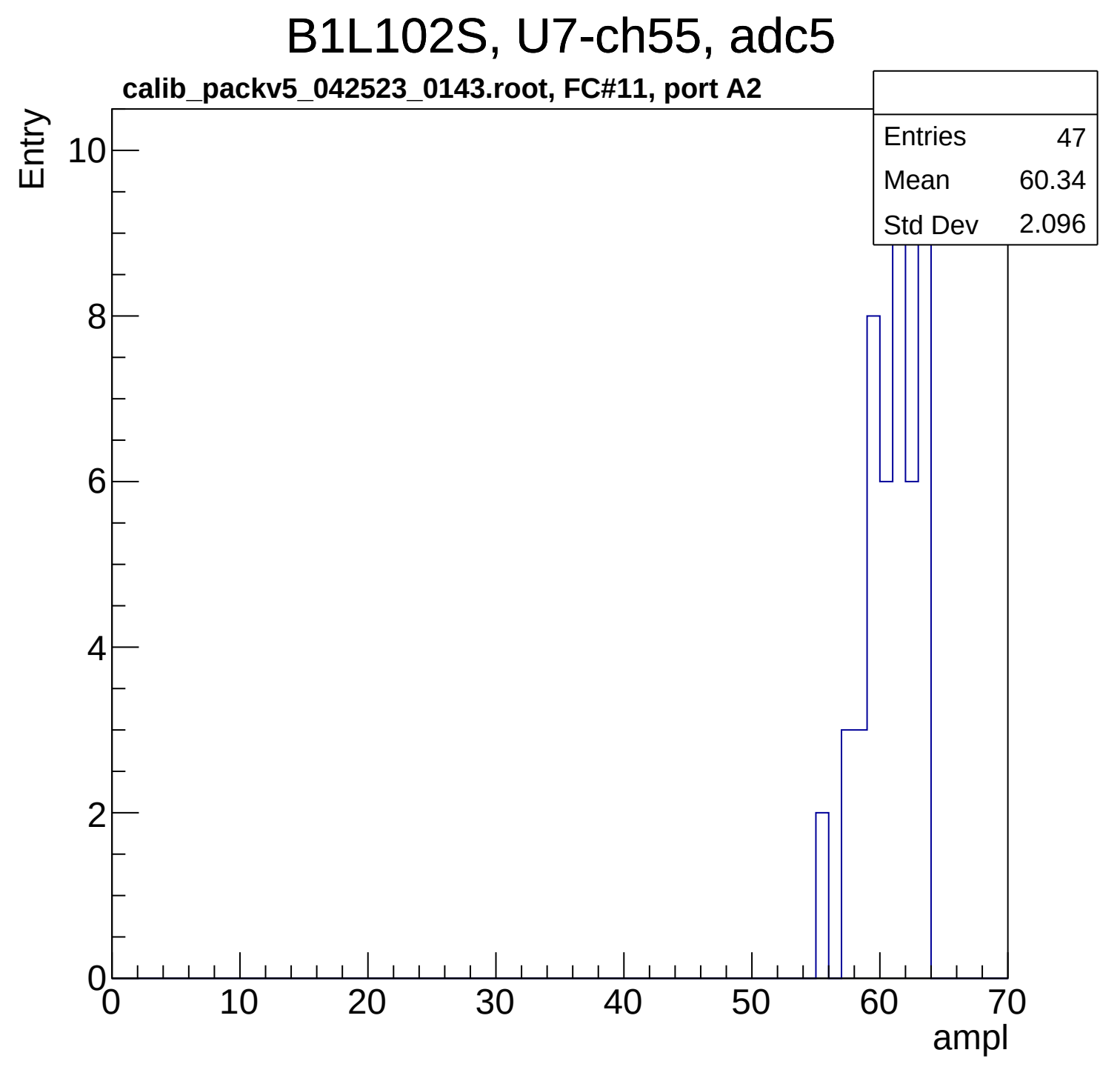
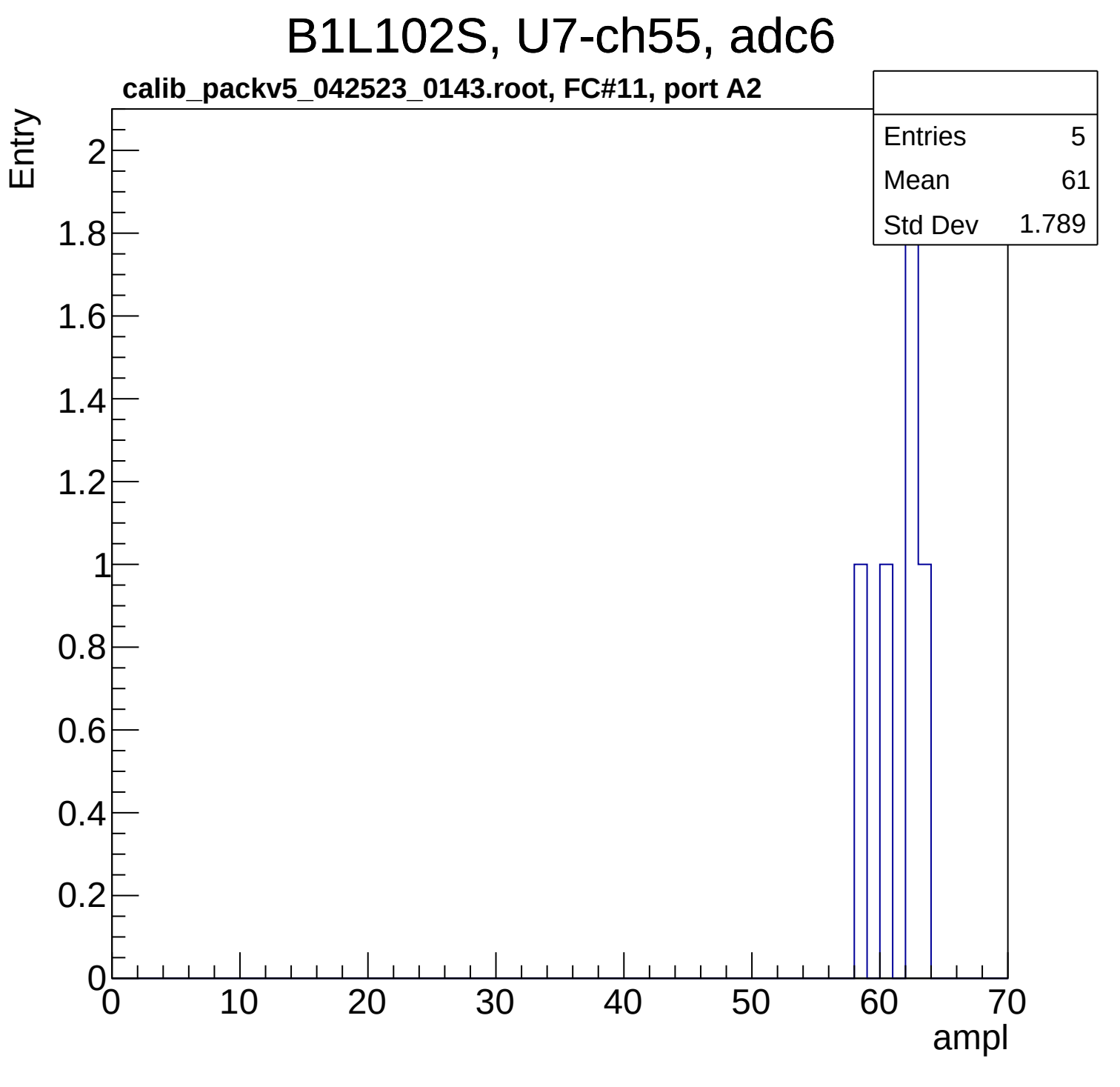
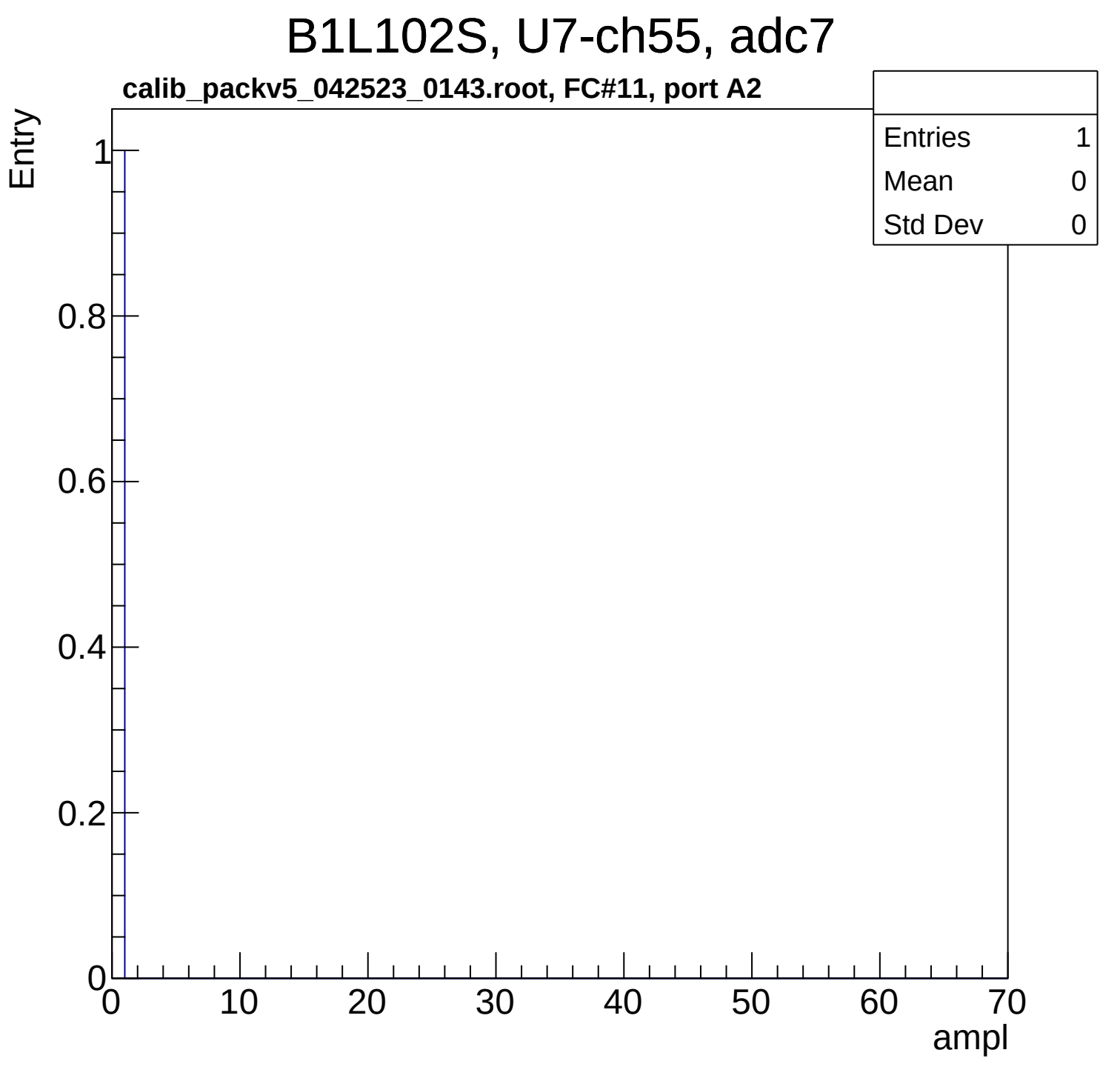

B1L102S, U7-ch55, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 68
Mean 54.09
Std Dev 7.314
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L102S, U7-ch55, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 47
Mean 60.34
Std Dev 2.096
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L102S, U7-ch55, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 5
Mean 61
Std Dev 1.789
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L102S, U7-ch55, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 1
Mean 0
Std Dev 0
Entry
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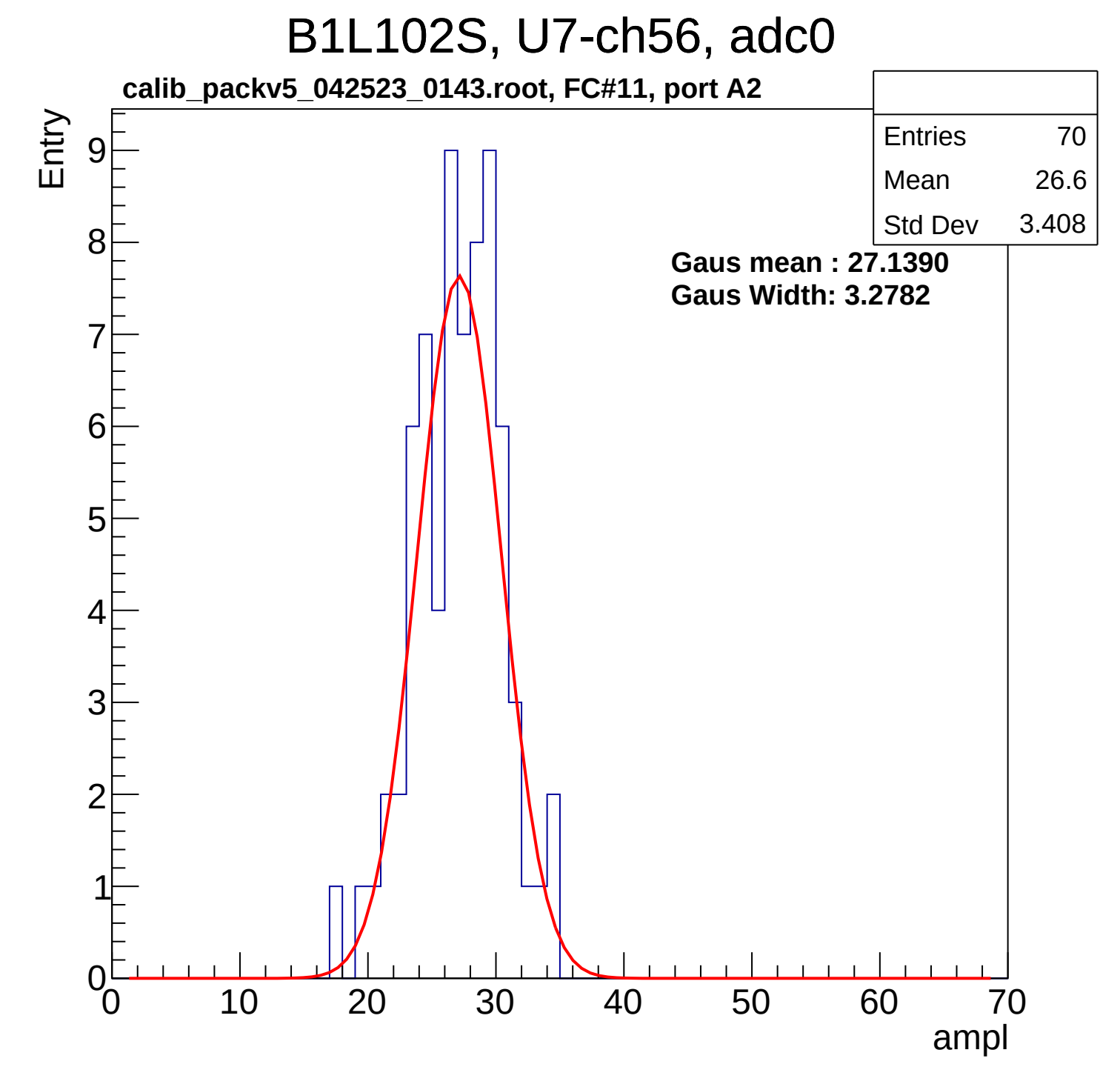
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U7-ch56, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 70
Mean 26.6
Std Dev 3.408
Gaus mean : 27.1390
Gaus Width: 3.2782
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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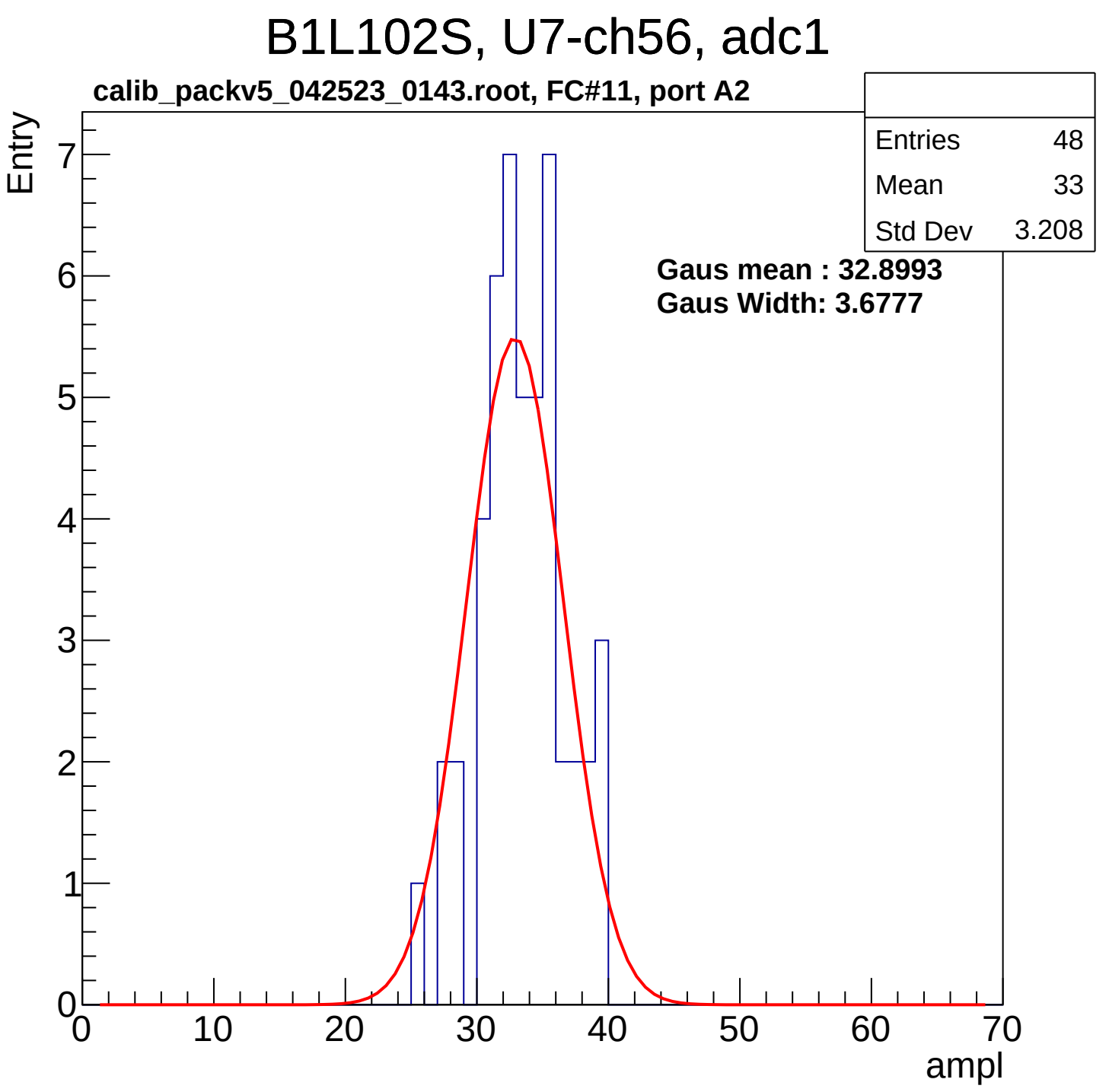
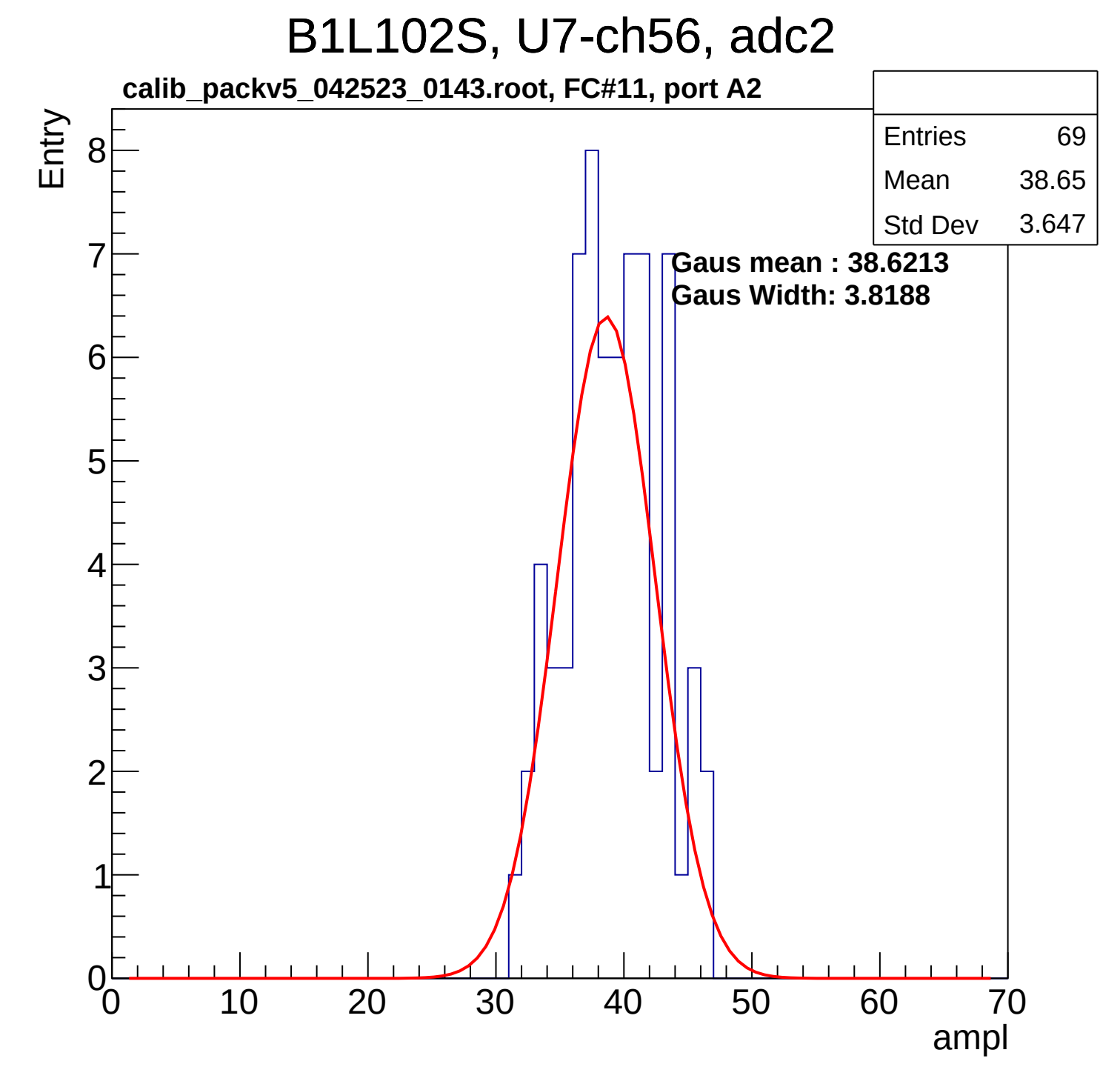
60
70


B1L102S, U7-ch56, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 48
Mean 33
Std Dev 3.208
Gaus mean : 32.8993
Gaus Width: 3.6777
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L102S, U7-ch56, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 69
Mean 38.65
Std Dev 3.647
Gaus mean : 38.6213
Gaus Width: 3.8188
Entry
ampl
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1
2
3
4
5
6
7
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0
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20
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60
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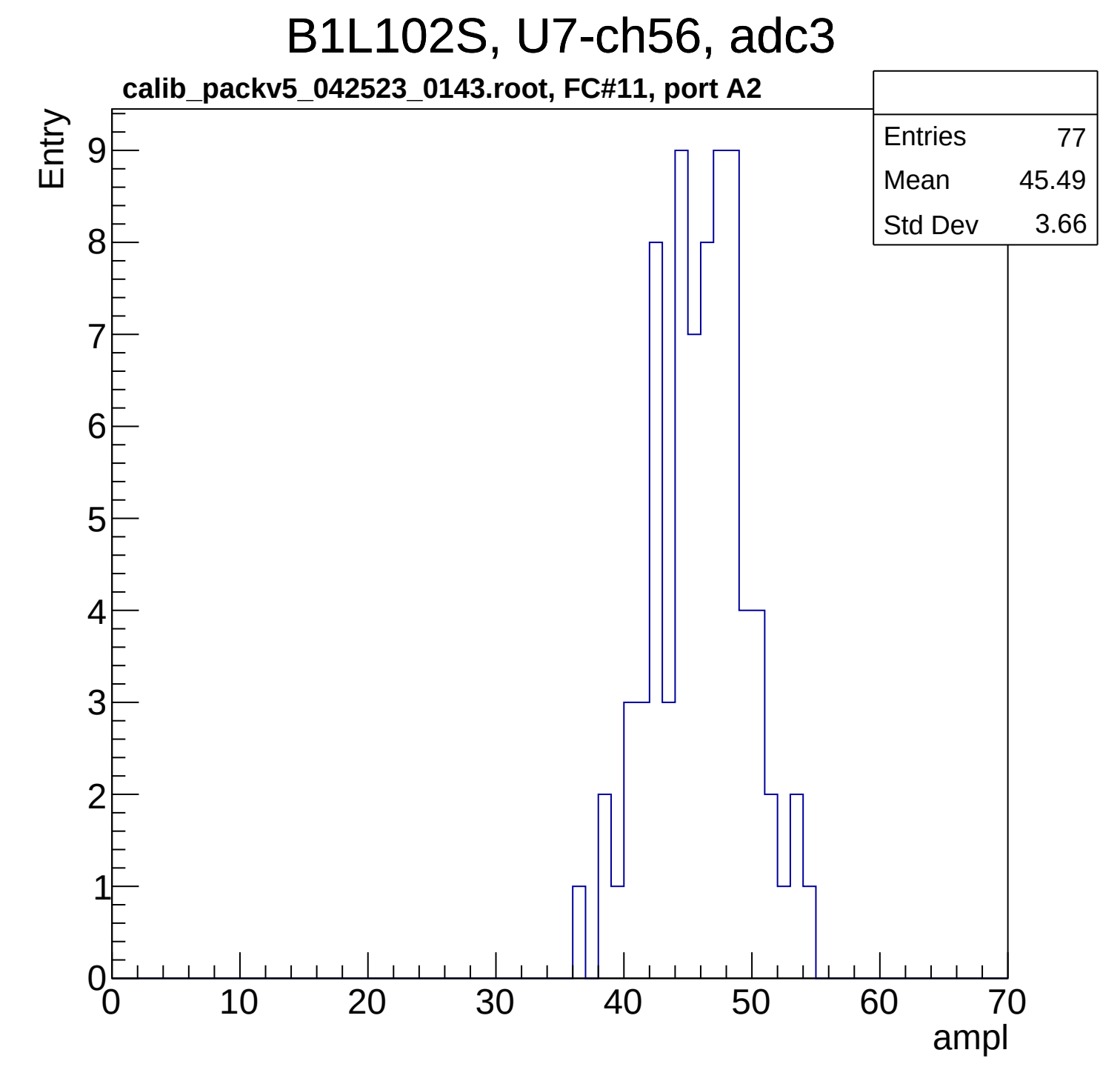
B1L102S, U7-ch56, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 77
Mean 45.49
Std Dev 3.66
Entry
ampl
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5
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8
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0
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60
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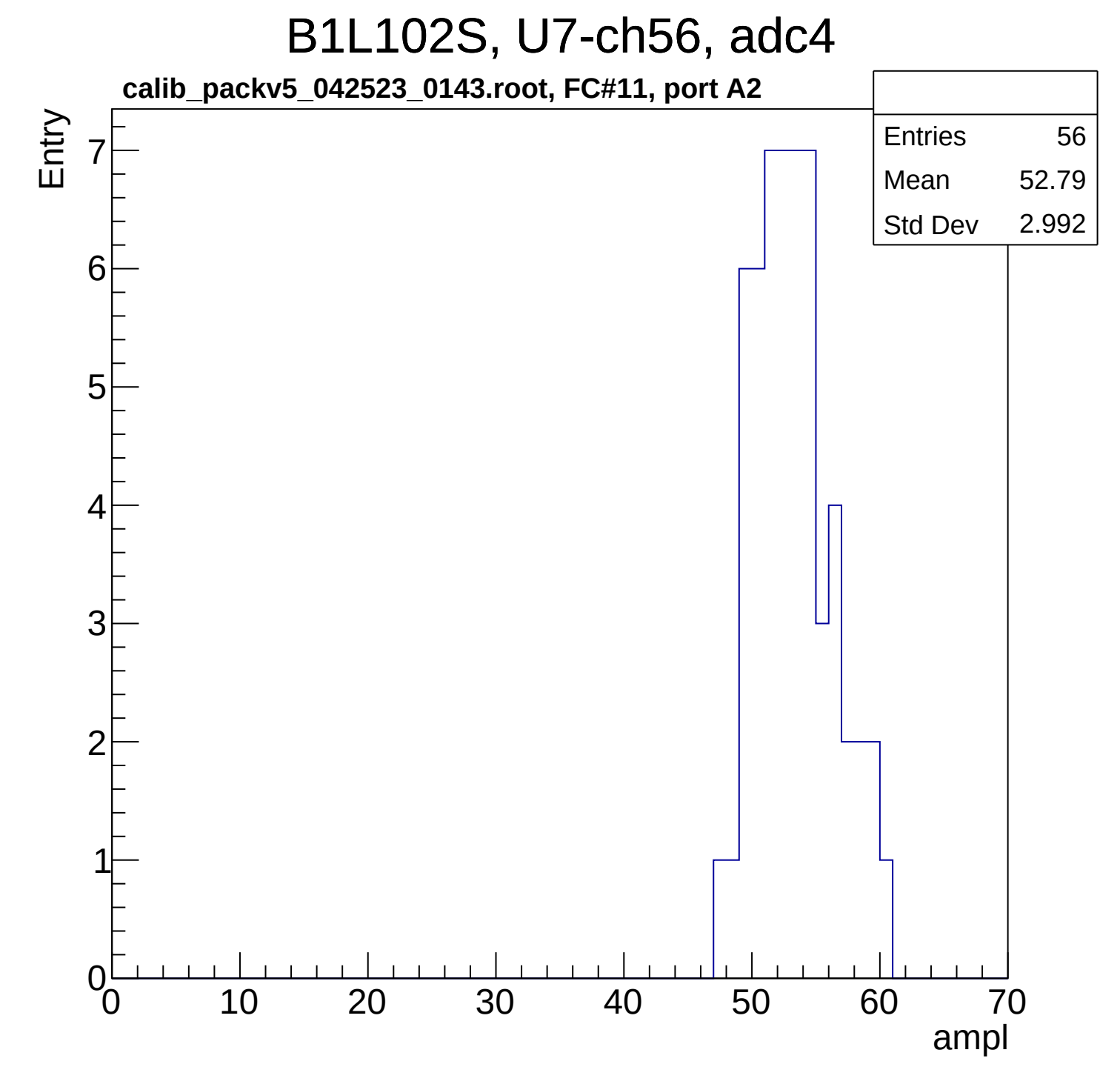
B1L102S, U7-ch56, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 56
Mean 52.79
Std Dev 2.992
Entry
ampl
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4
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6
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0
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40
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60
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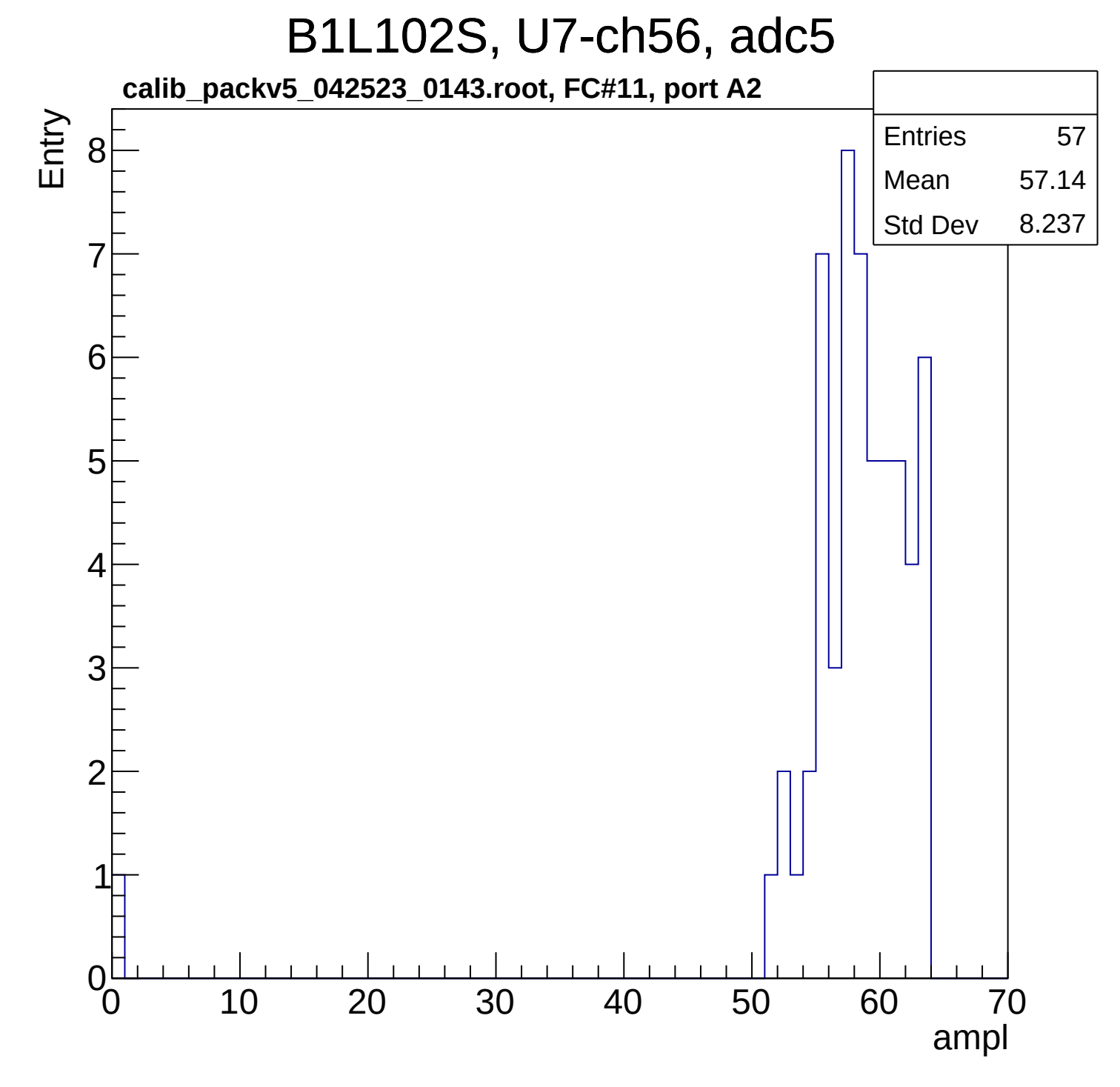
B1L102S, U7-ch56, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 57
Mean 57.14
Std Dev 8.237
Entry
ampl
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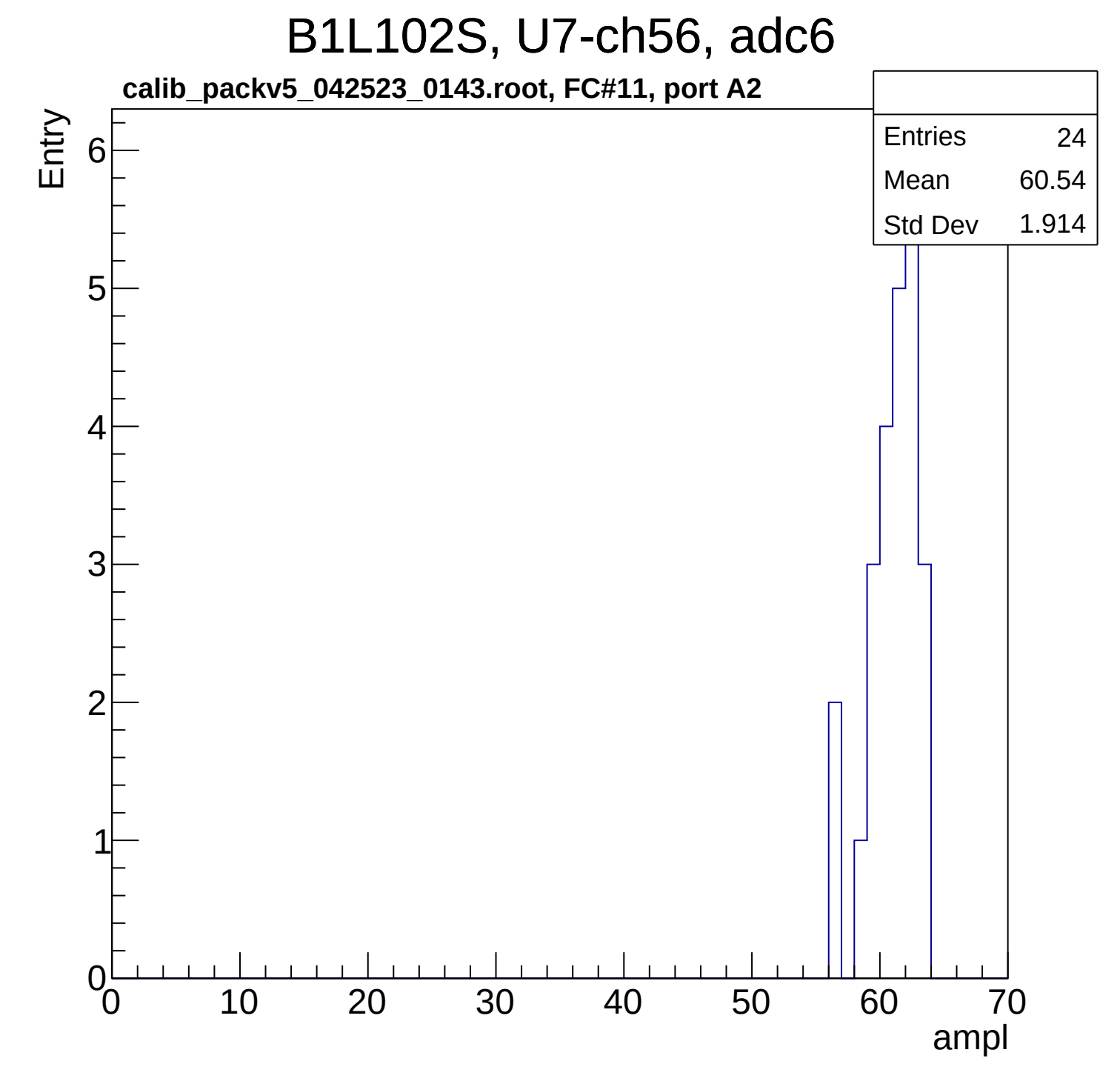
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L102S, U7-ch56, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 24
Mean 60.54
Std Dev 1.914
Entry
ampl
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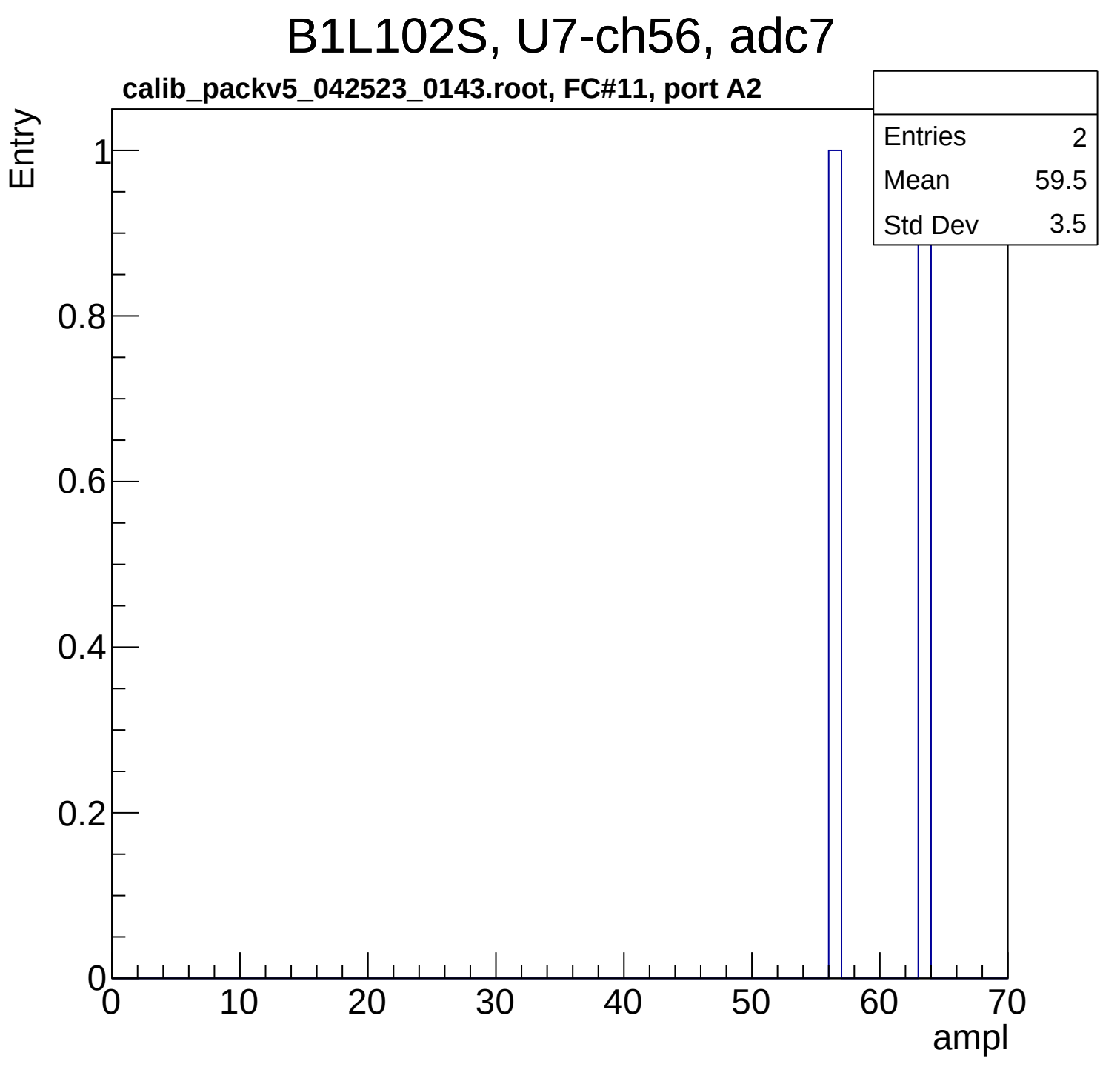
3
4
5
6
0
10
20
30
40
50
60
70


B1L102S, U7-ch56, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 2
Mean 59.5
Std Dev 3.5
Entry
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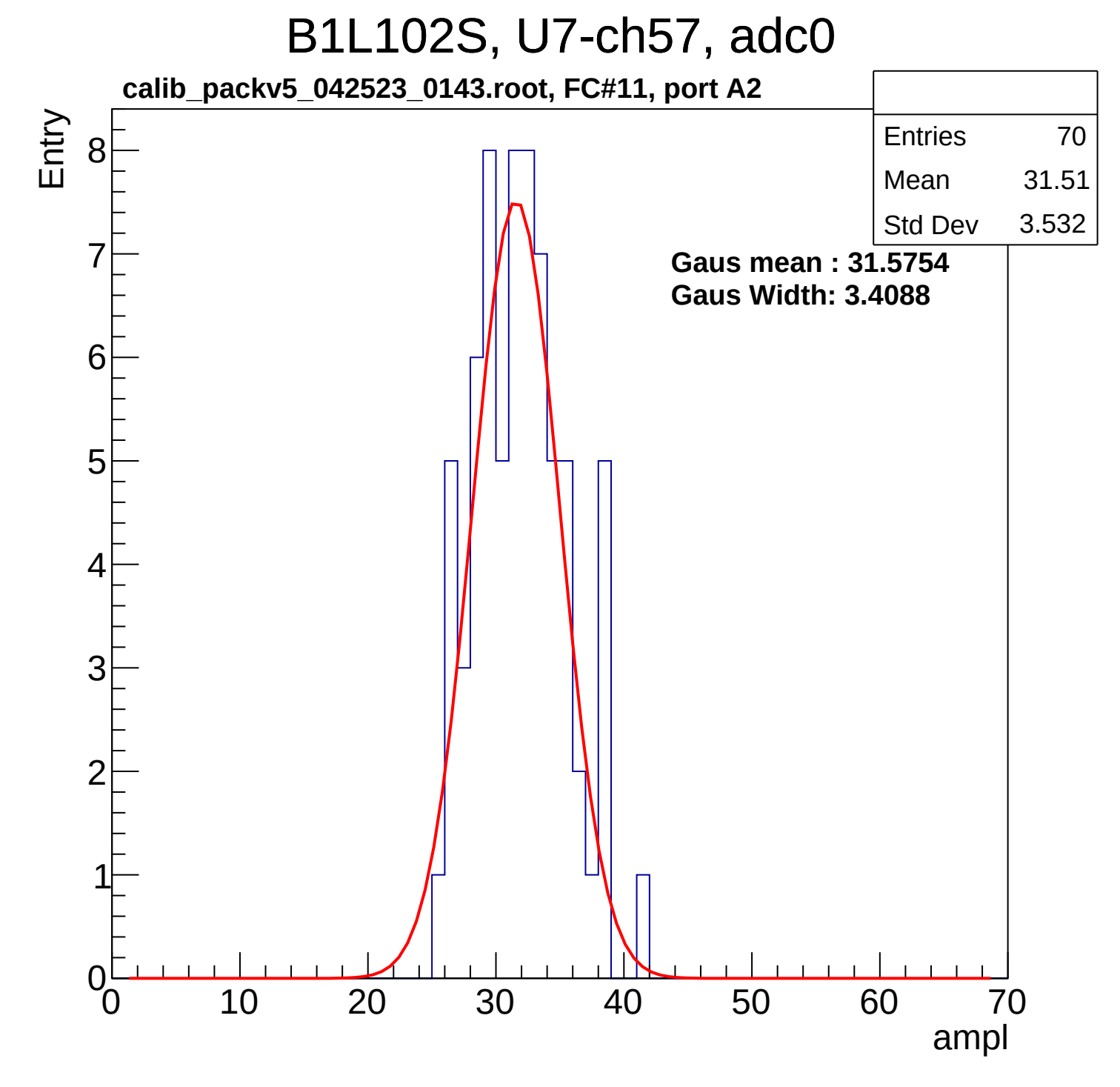
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U7-ch57, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 70
Mean 31.51
Std Dev 3.532
Gaus mean : 31.5754
Gaus Width: 3.4088
Entry
ampl
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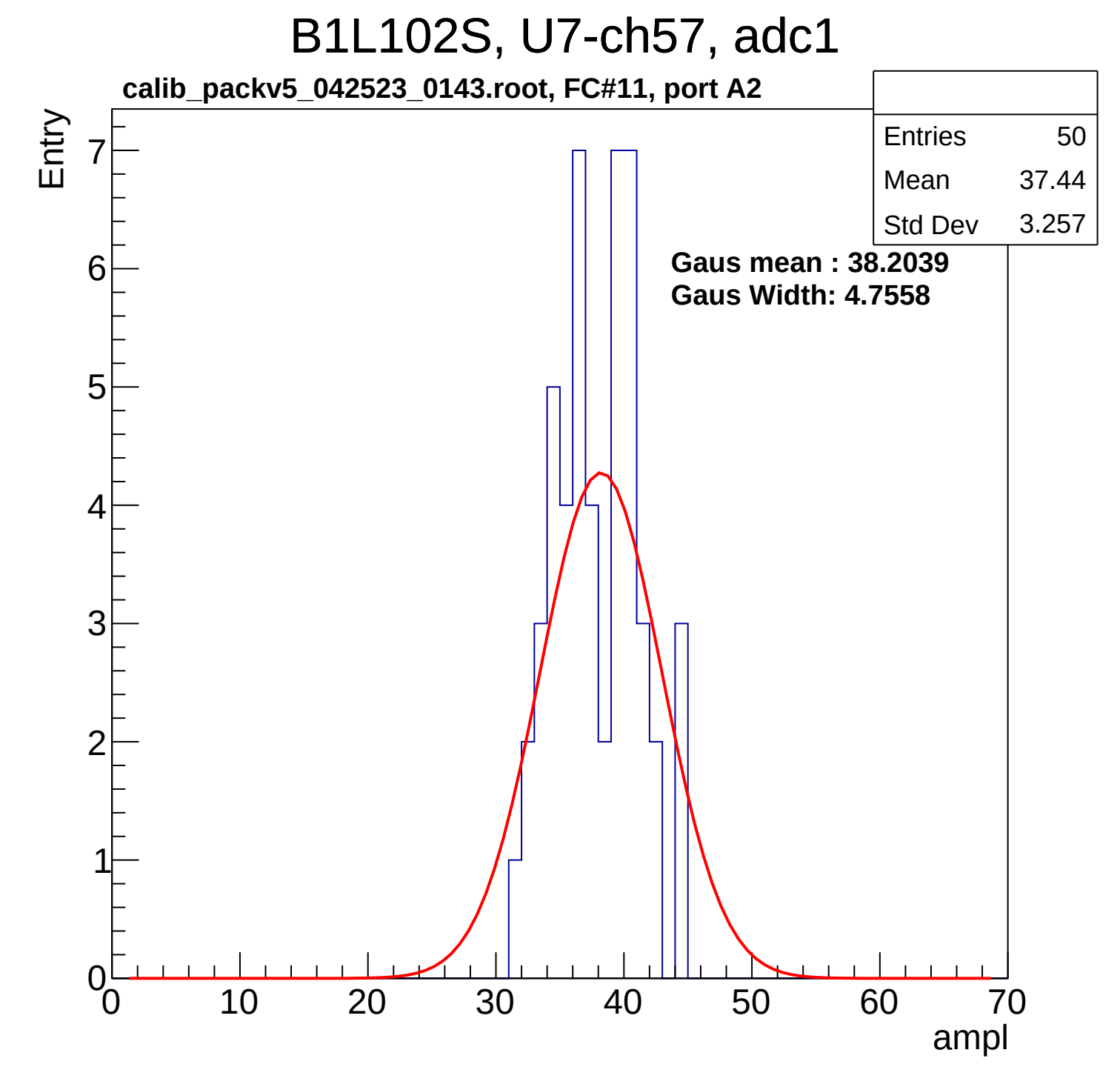
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L102S, U7-ch57, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 50
Mean 37.44
Std Dev 3.257
Gaus mean : 38.2039
Gaus Width: 4.7558
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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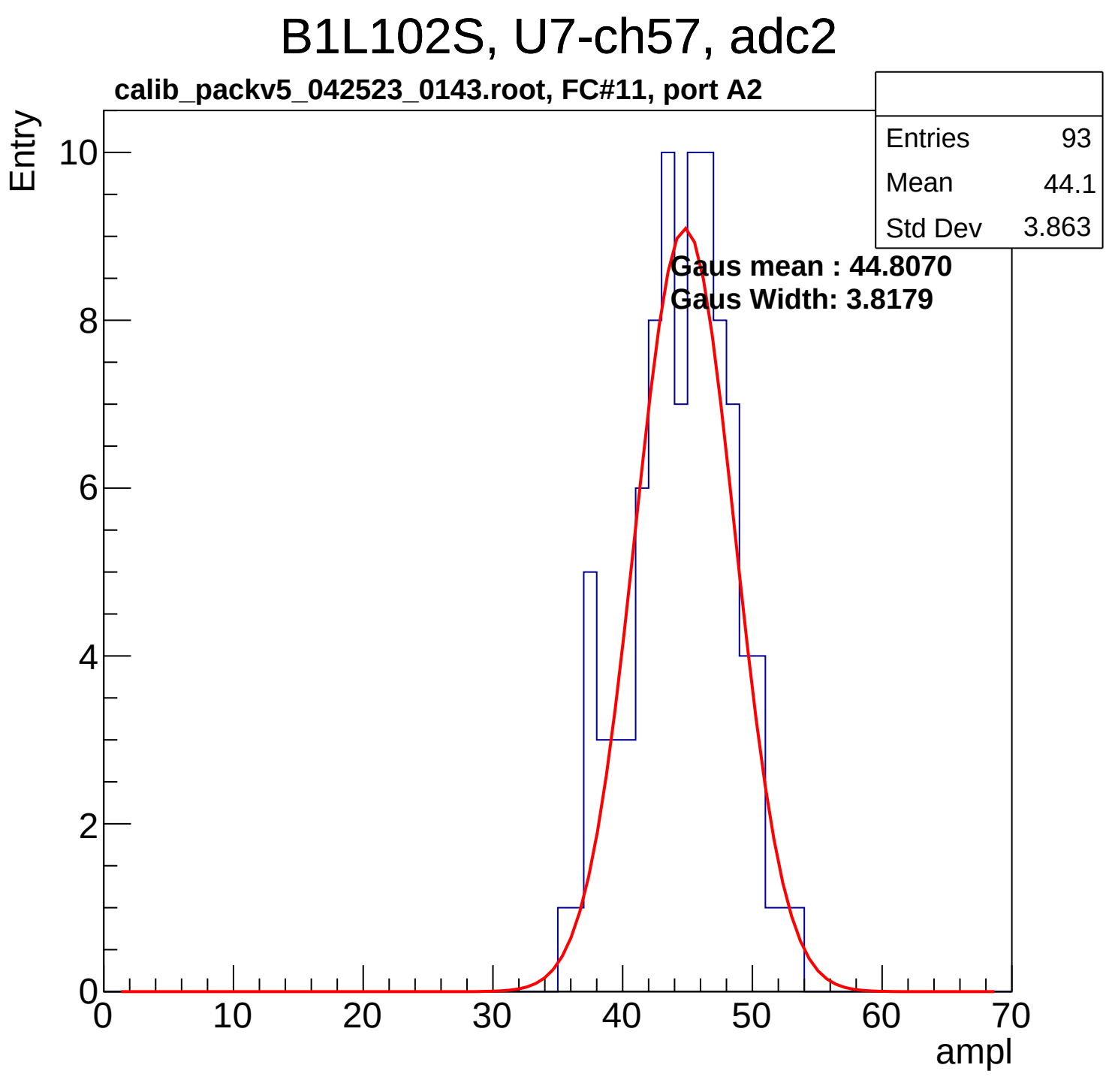
B1L102S, U7-ch57, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 93
Mean 44.1
Std Dev 3.863
Gaus mean : 44.8070
Gaus Width: 3.8179
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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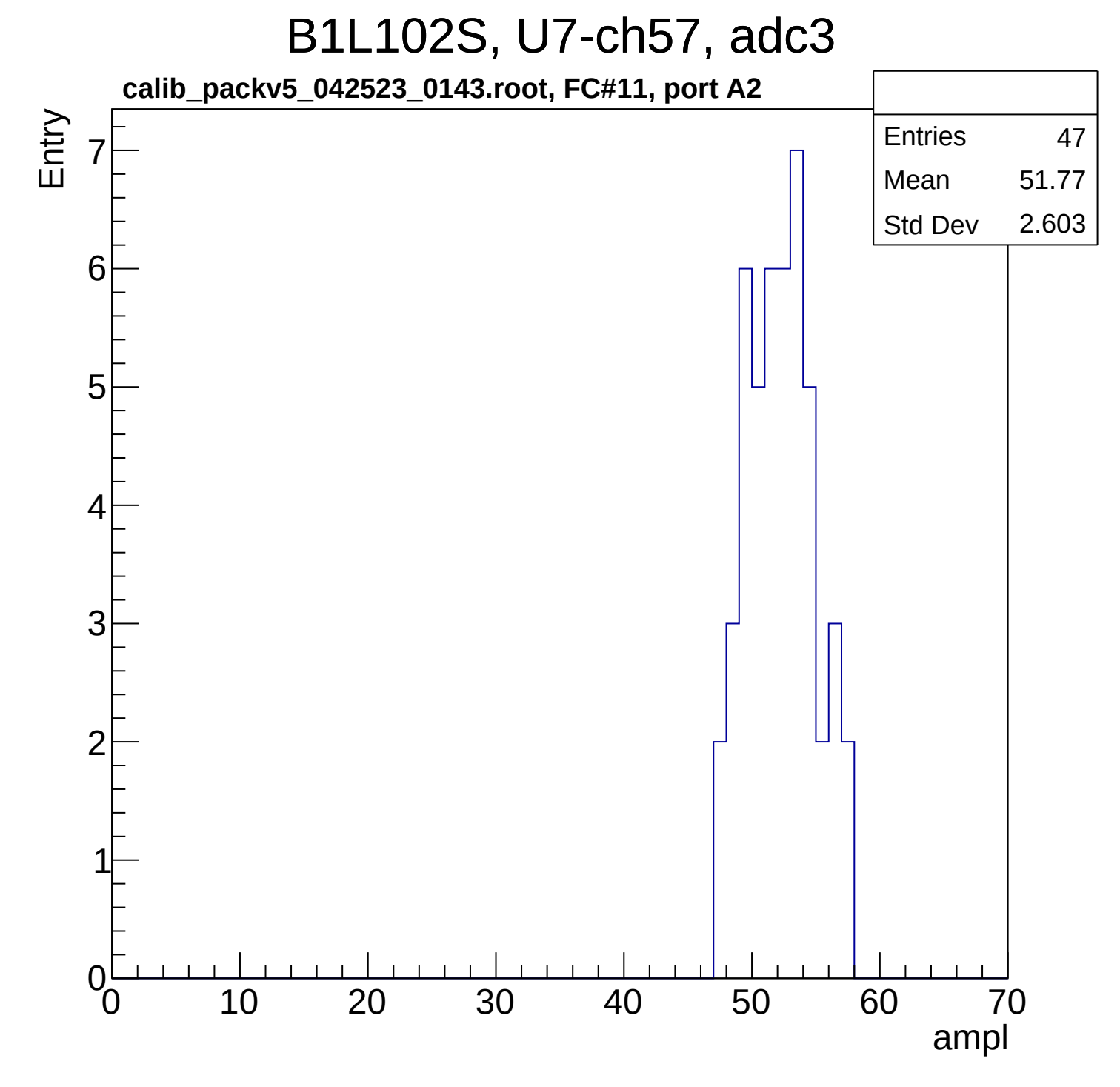
B1L102S, U7-ch57, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 47
Mean 51.77
Std Dev 2.603
Entry
ampl
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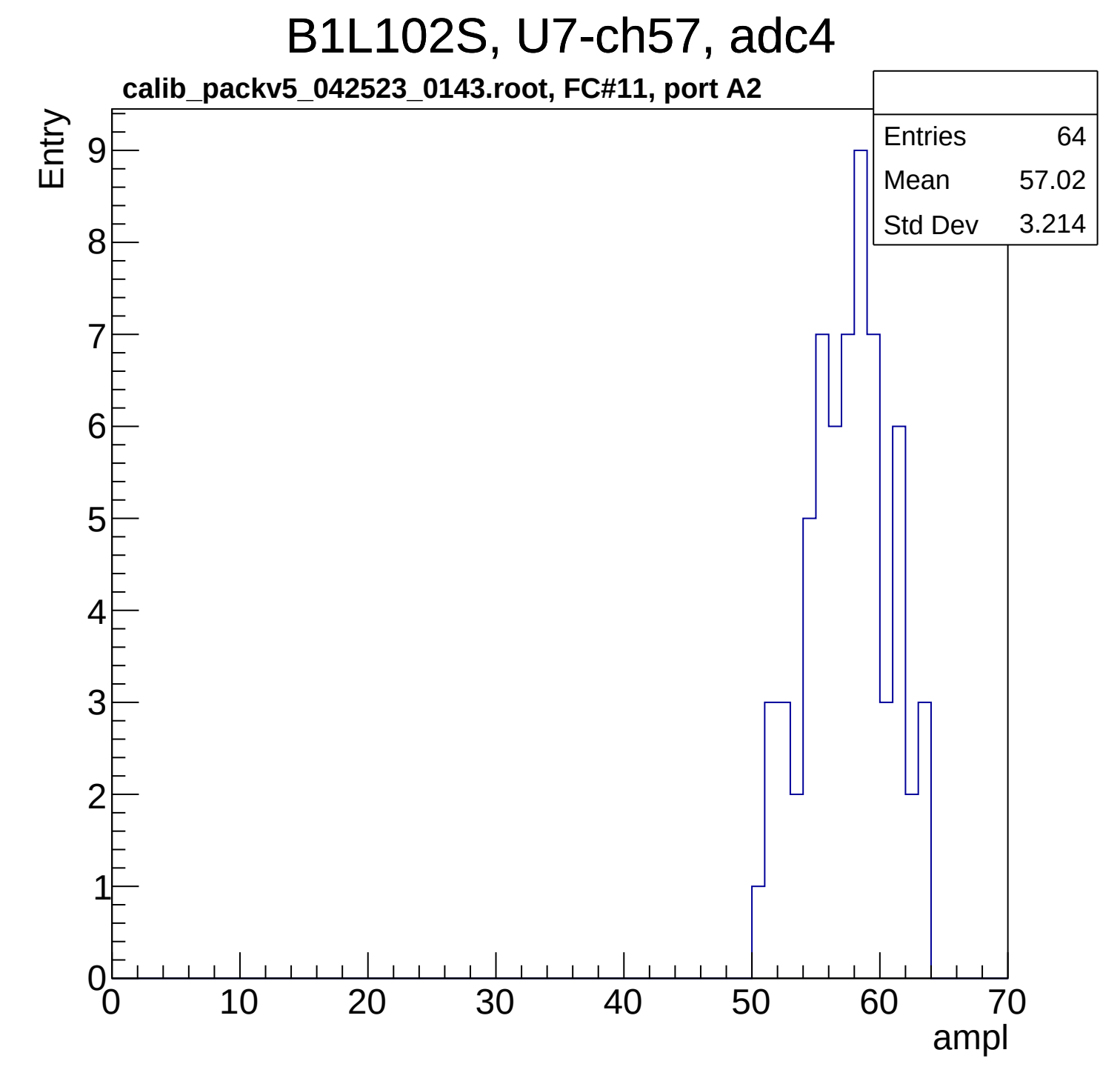
B1L102S, U7-ch57, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 64
Mean 57.02
Std Dev 3.214
Entry
ampl
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3
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0
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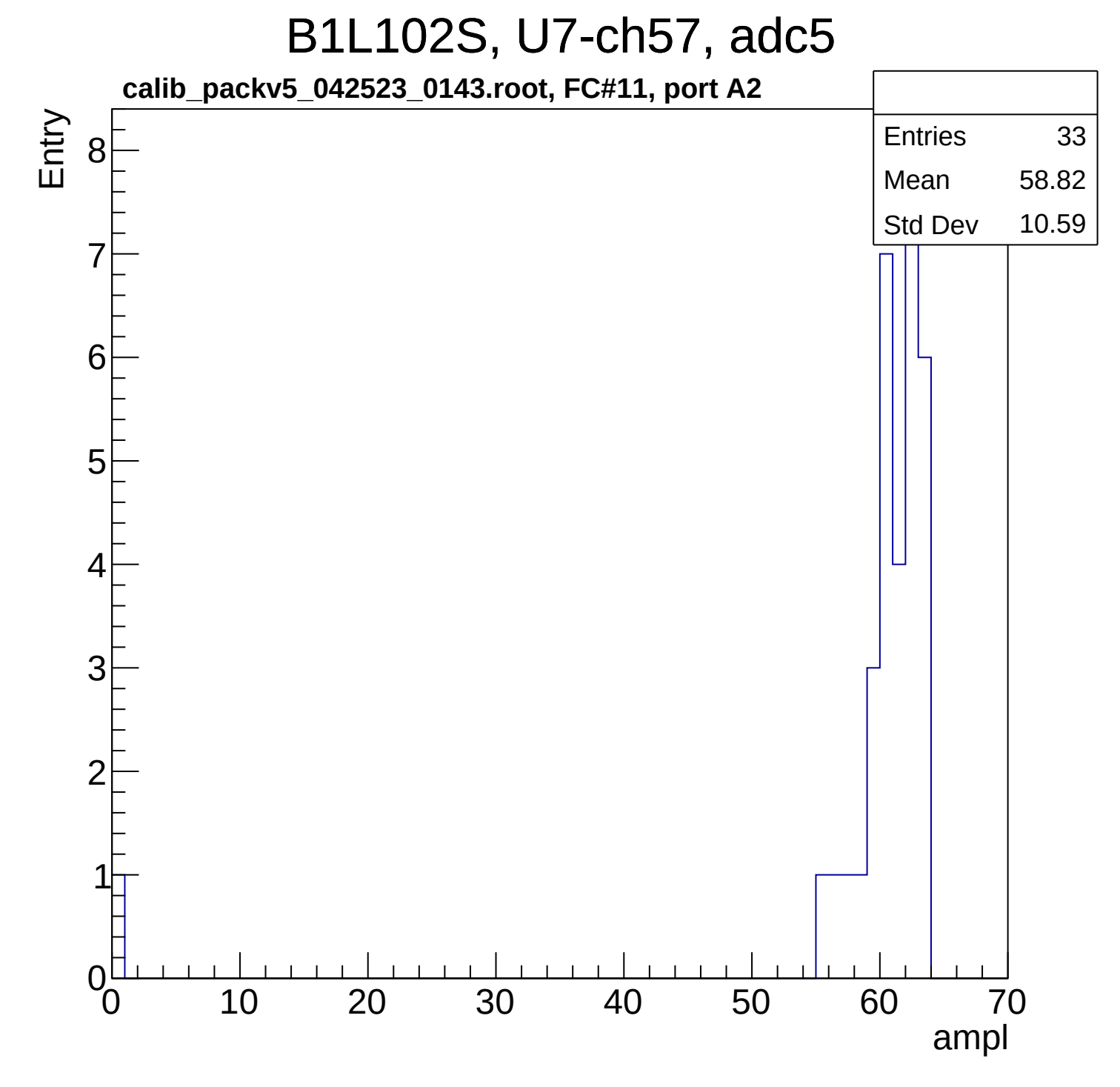
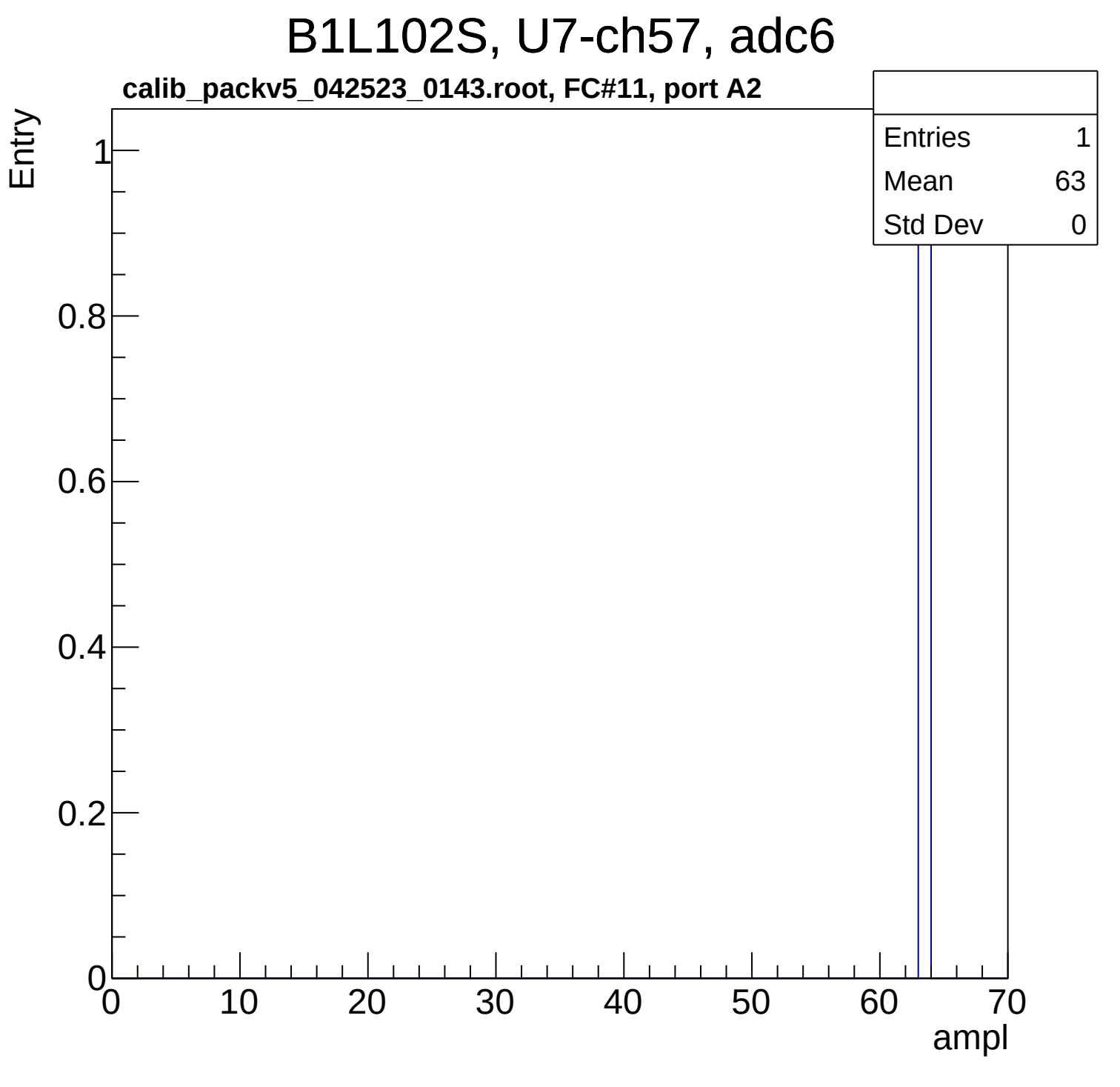

B1L102S, U7-ch57, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 33
Mean 58.82
Std Dev 10.59
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L102S, U7-ch57, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 1
Mean 63
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
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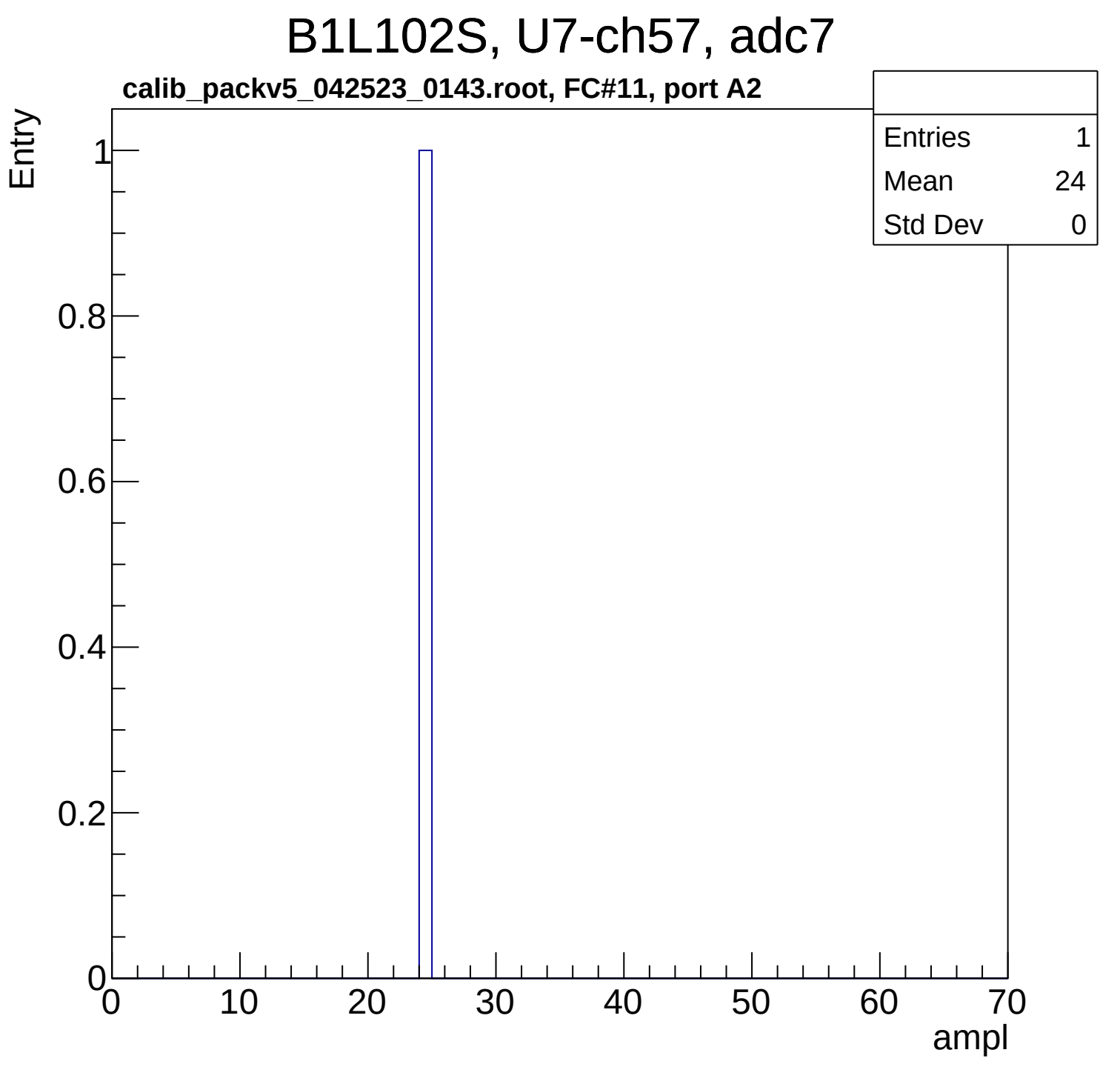
50
60
70
ampl


B1L102S, U7-ch57, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 1
Mean 24
Std Dev 0
Entry
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0.8
0.6
0.4
0.2
0
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10
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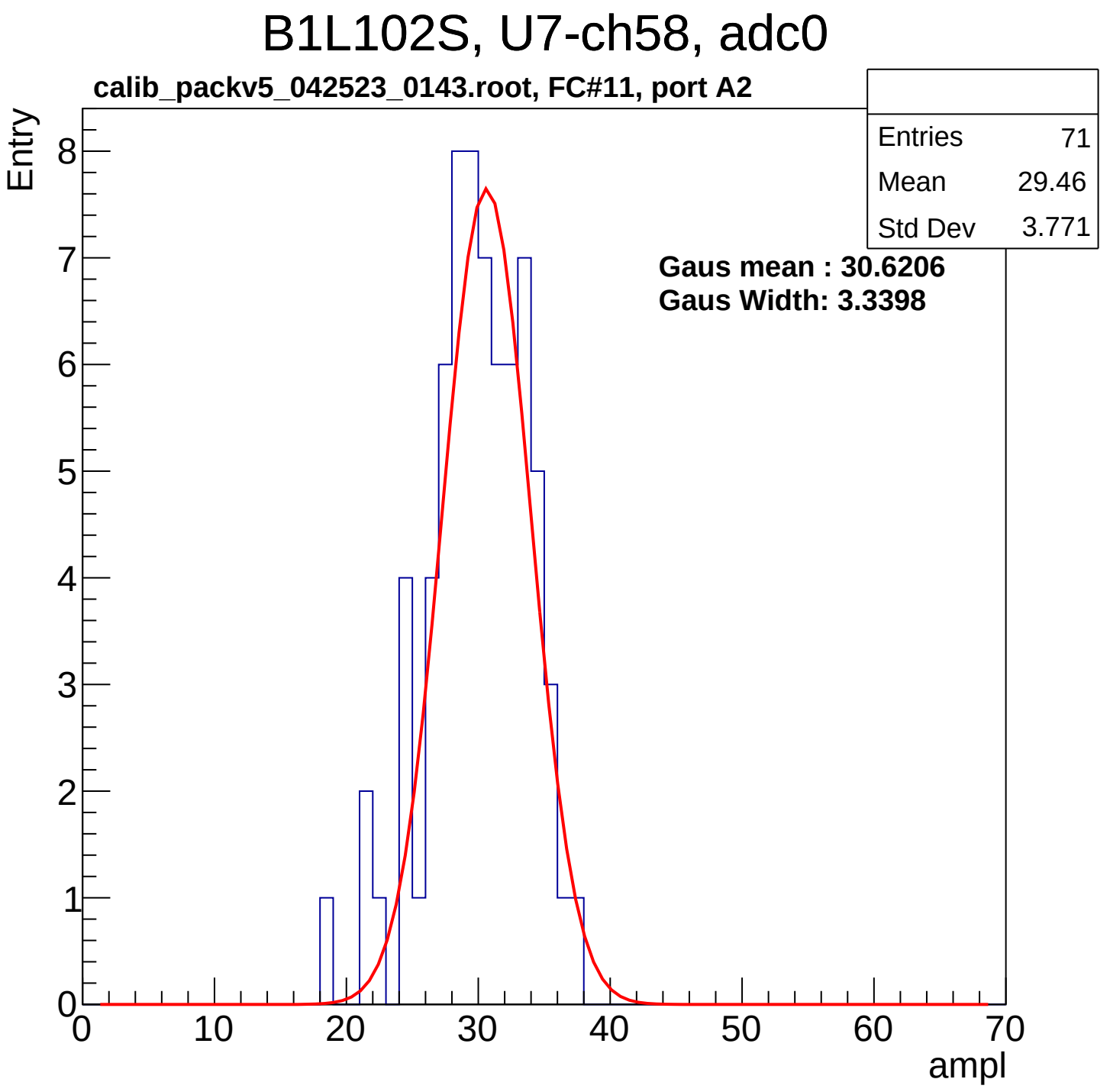
50
60
70
ampl


B1L102S, U7-ch58, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 71
Mean 29.46
Std Dev 3.771
Gaus mean : 30.6206
Gaus Width: 3.3398
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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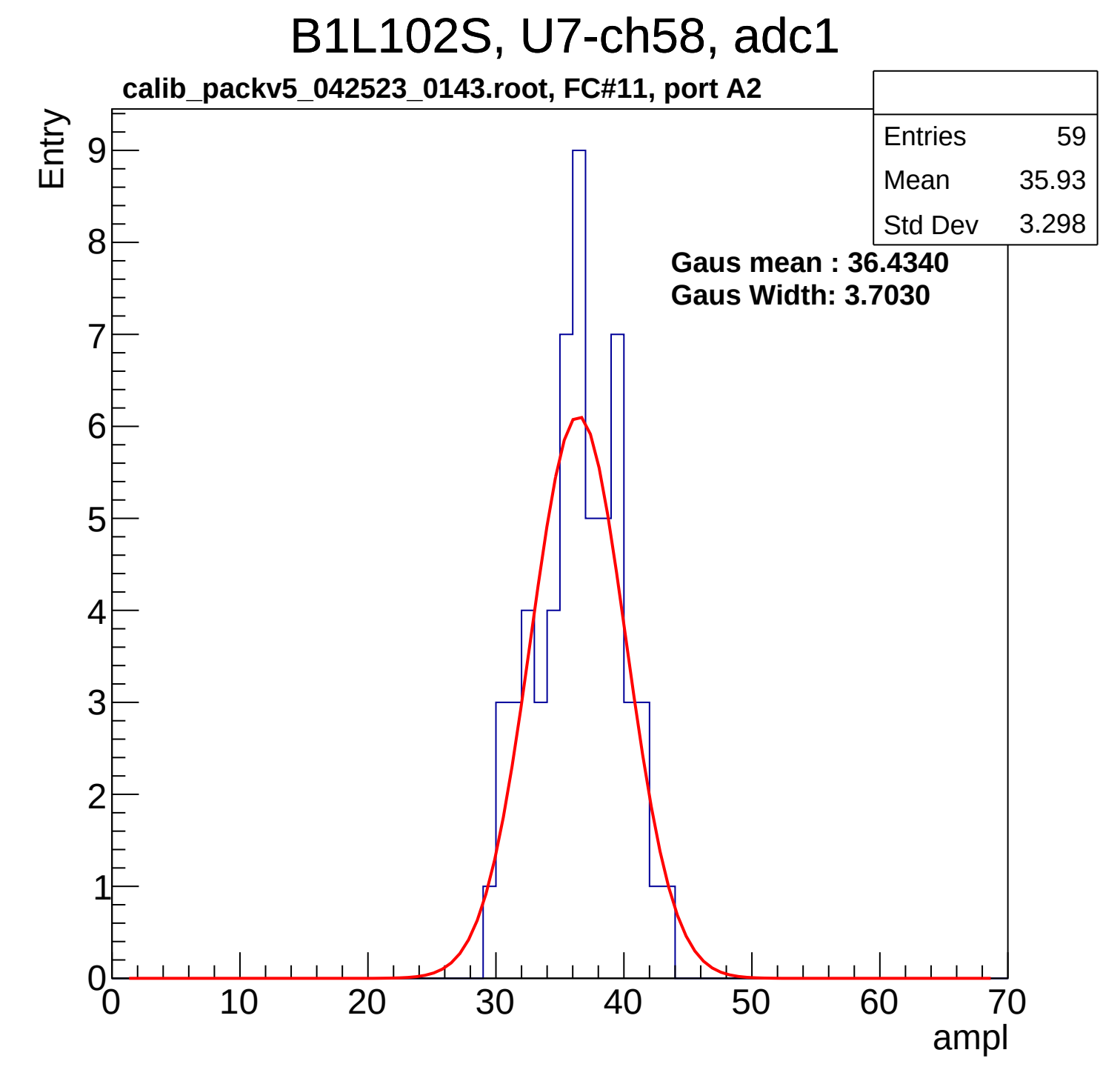
B1L102S, U7-ch58, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 59
Mean 35.93
Std Dev 3.298
Gaus mean : 36.4340
Gaus Width: 3.7030
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
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20
30
40
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60
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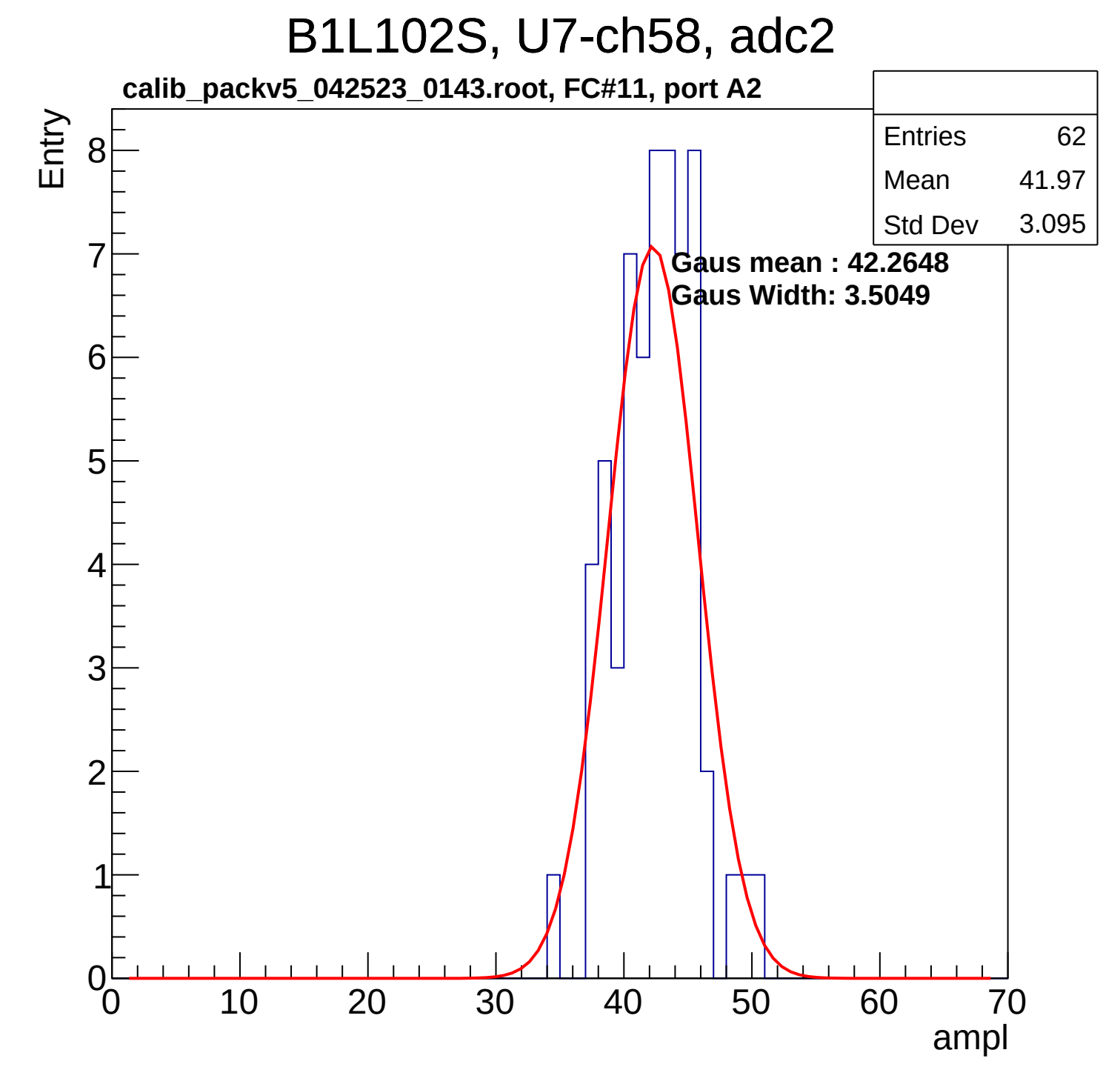
B1L102S, U7-ch58, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 62
Mean 41.97
Std Dev 3.095
Gaus mean : 42.2648
Gaus Width: 3.5049
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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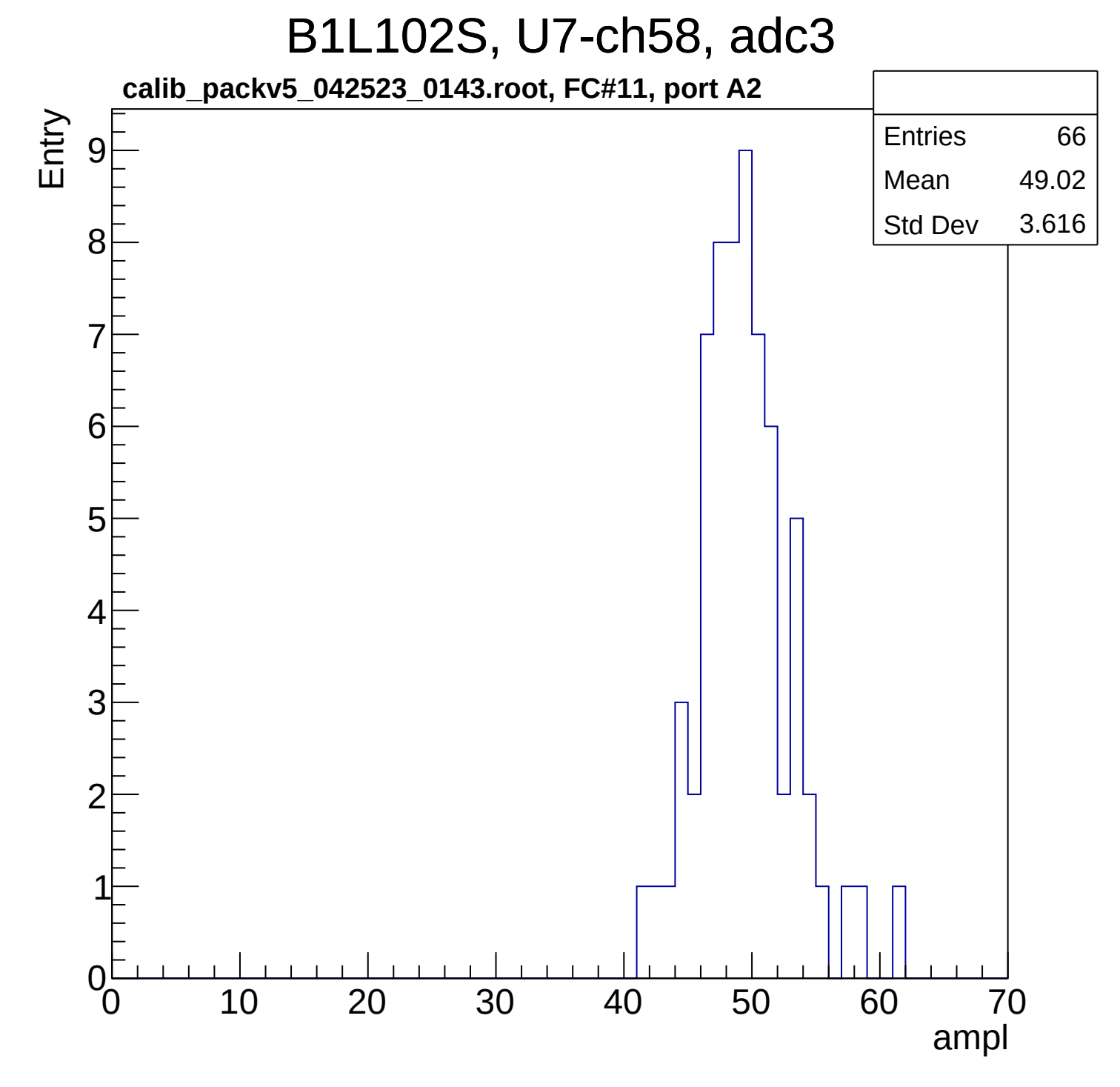
B1L102S, U7-ch58, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 66
Mean 49.02
Std Dev 3.616
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
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20
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40
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60
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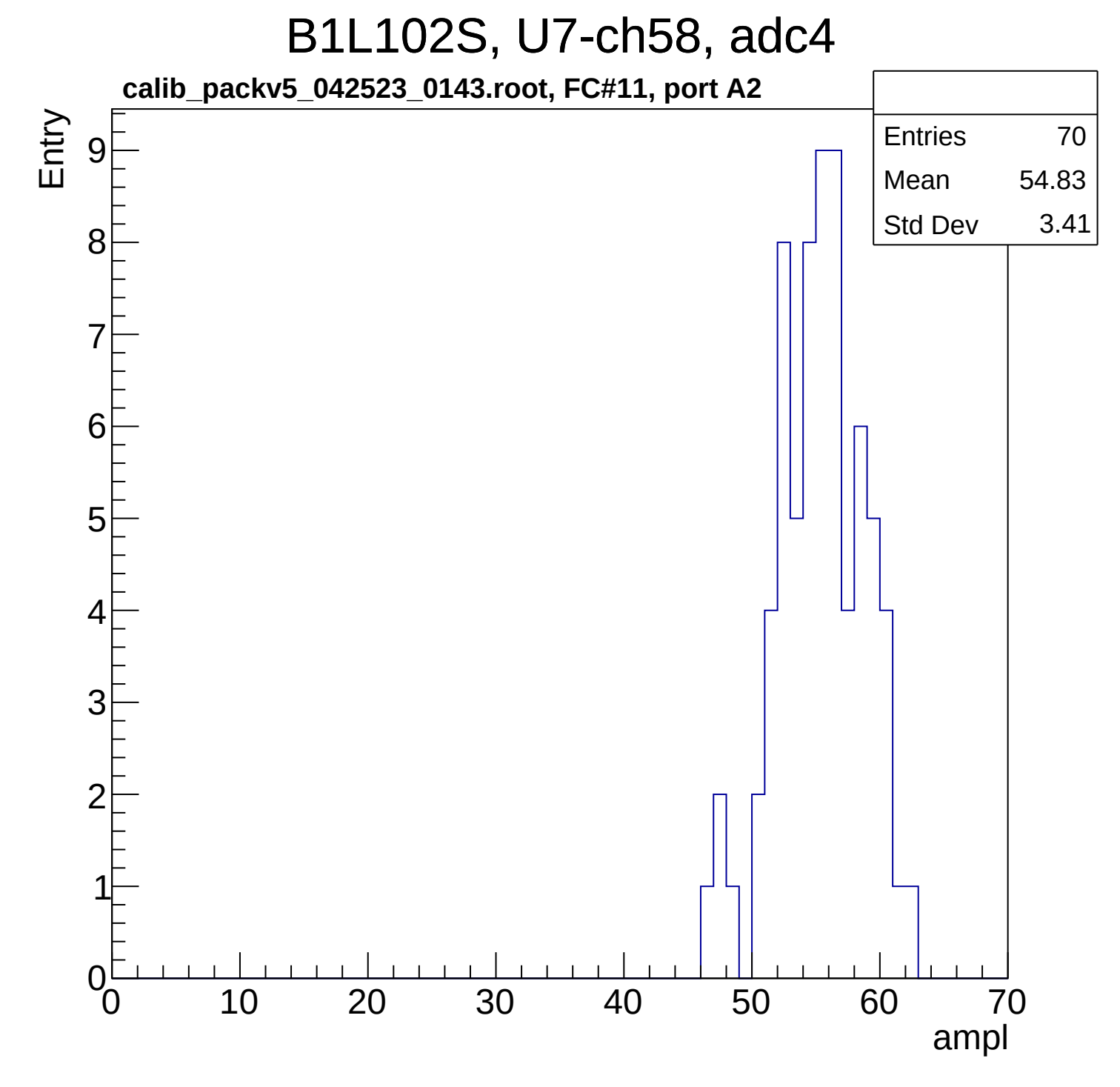
B1L102S, U7-ch58, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 70
Mean 54.83
Std Dev 3.41
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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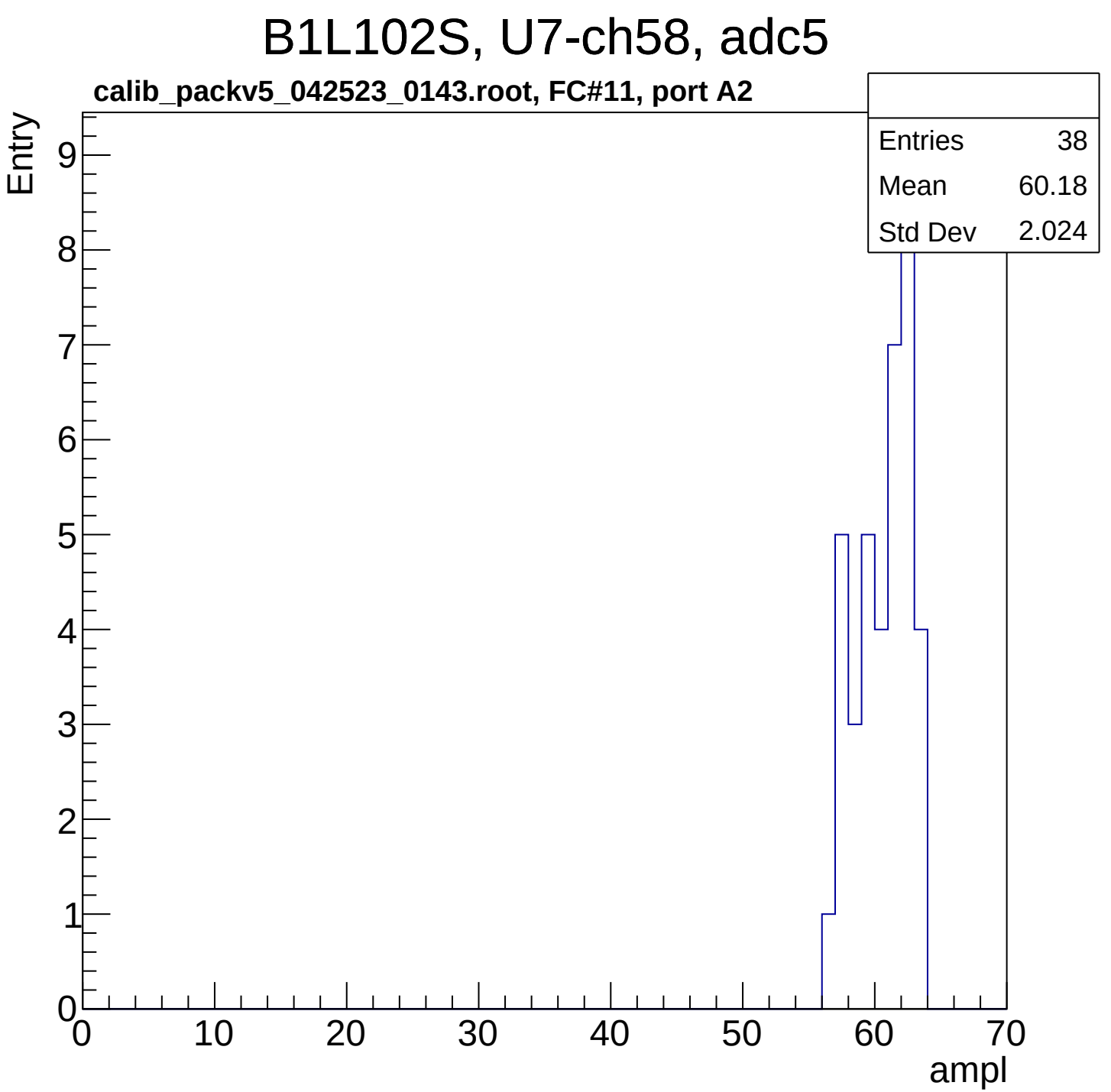
B1L102S, U7-ch58, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 38
Mean 60.18
Std Dev 2.024
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
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40
50
60
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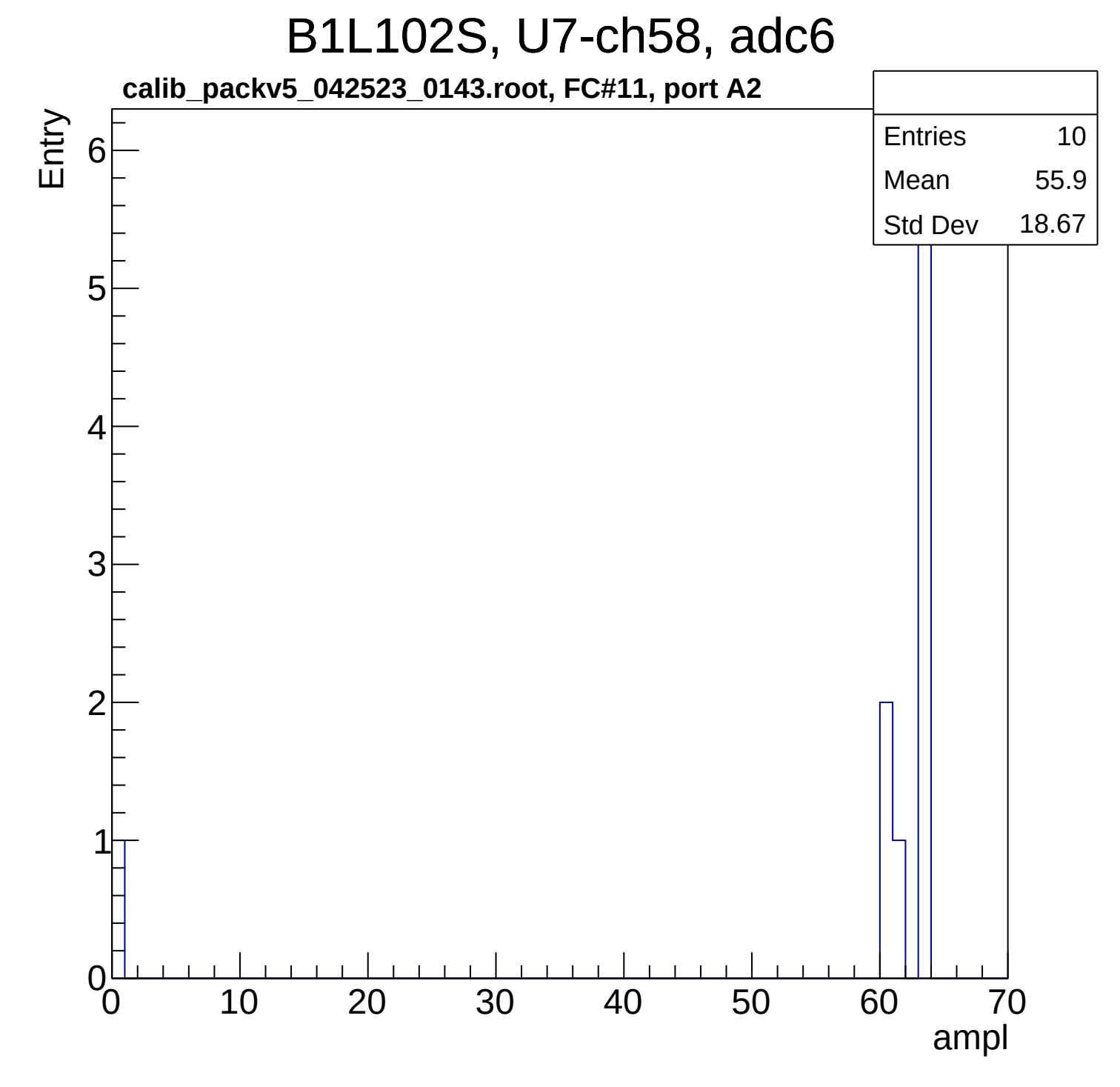
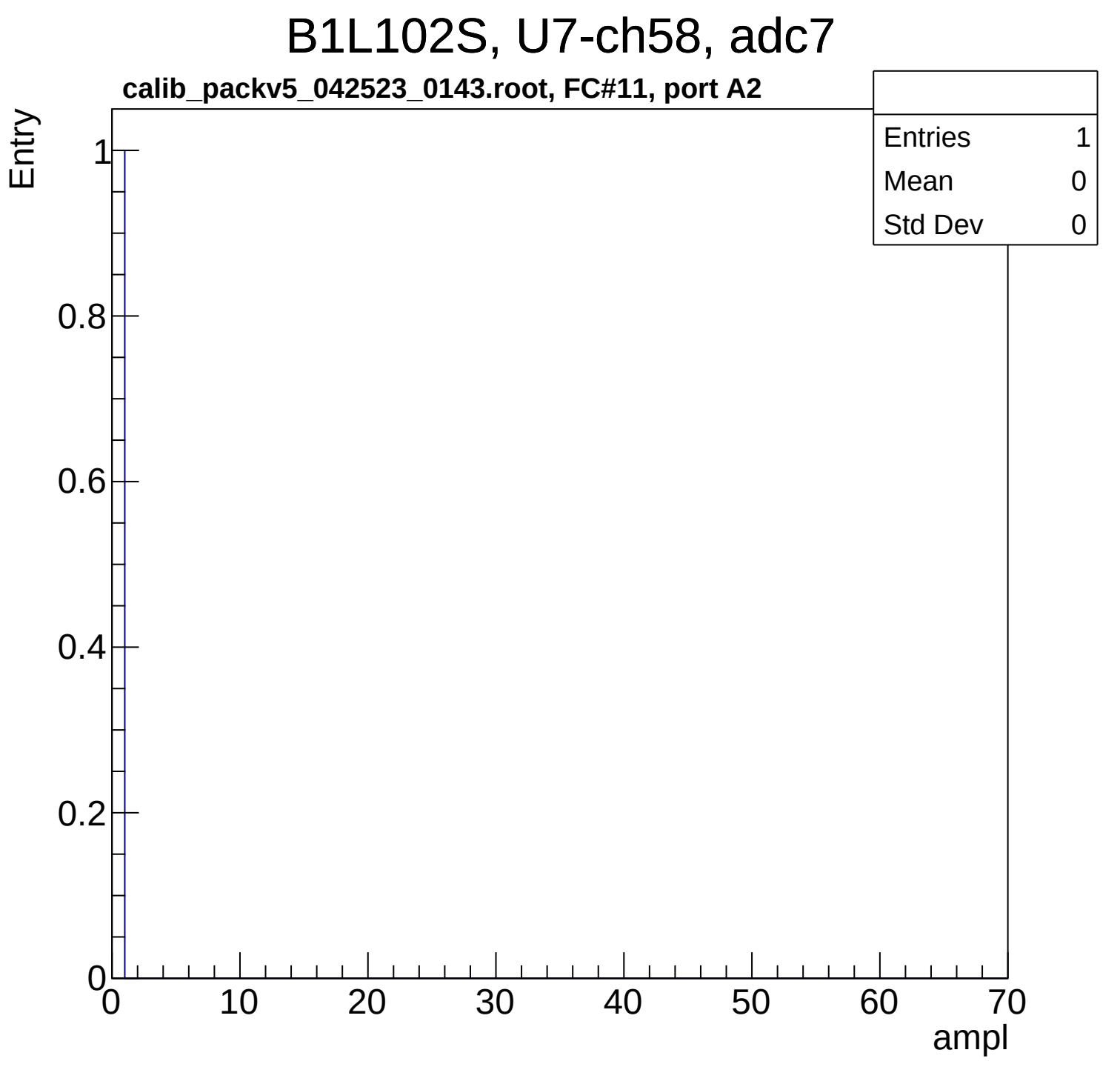
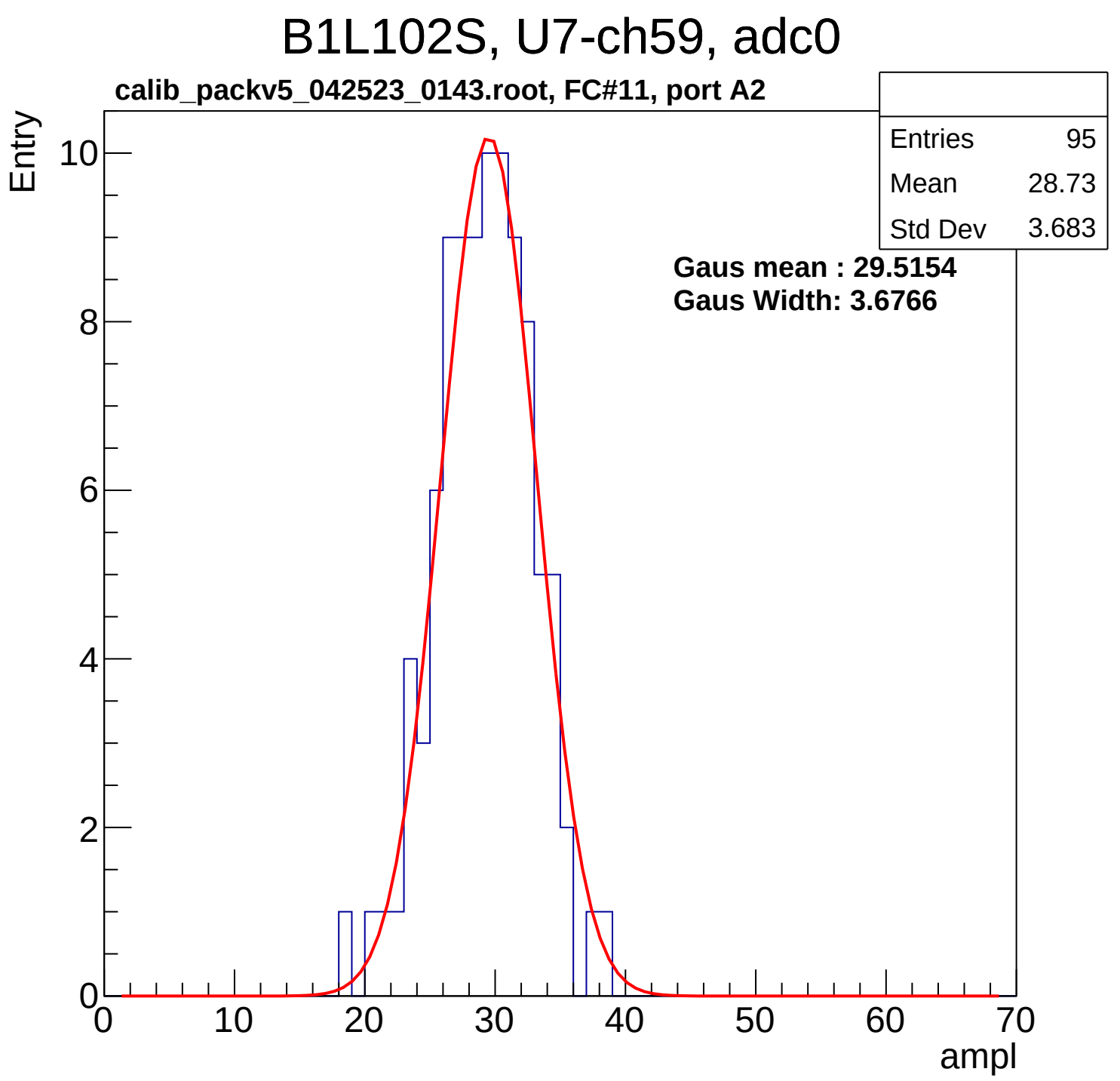
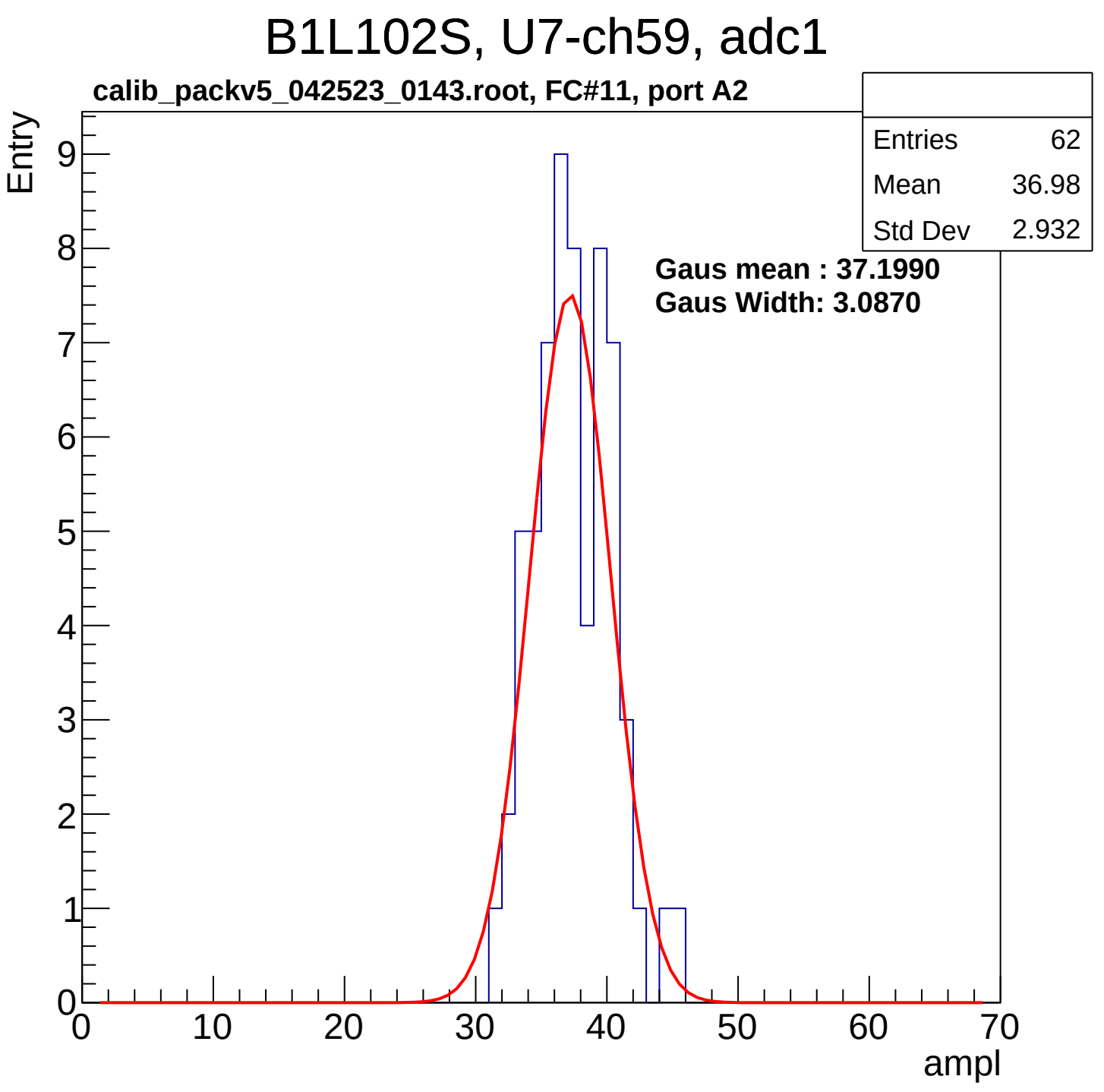
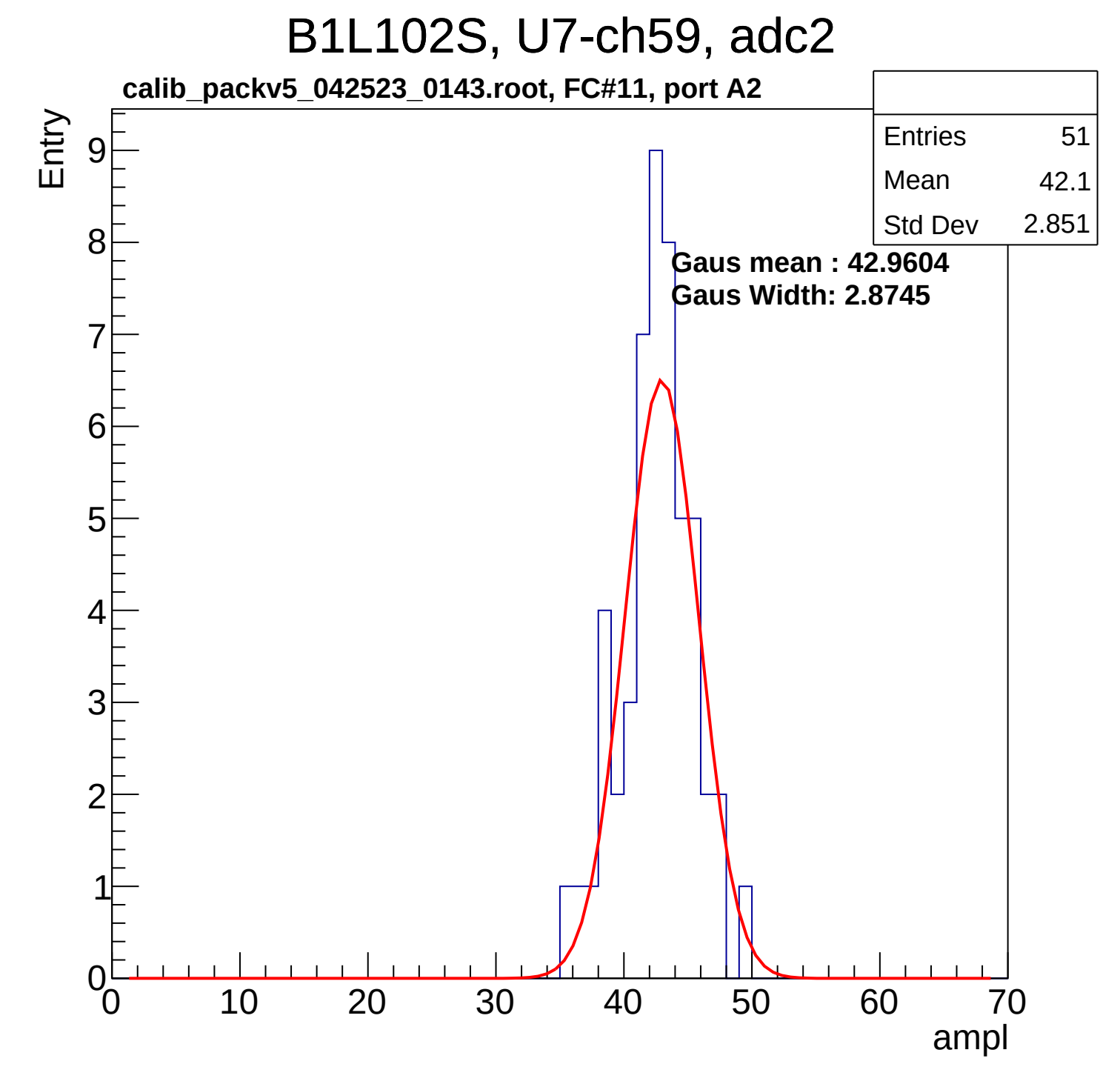

B1L102S, U7-ch58, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 10
Mean 55.9
Std Dev 18.67
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L102S, U7-ch58, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U7-ch59, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 95
Mean 28.73
Std Dev 3.683
Gaus mean : 29.5154
Gaus Width: 3.6766
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L102S, U7-ch59, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 62
Mean 36.98
Std Dev 2.932
Gaus mean : 37.1990
Gaus Width: 3.0870
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L102S, U7-ch59, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 51
Mean 42.1
Std Dev 2.851
Gaus mean : 42.9604
Gaus Width: 2.8745
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
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40
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60
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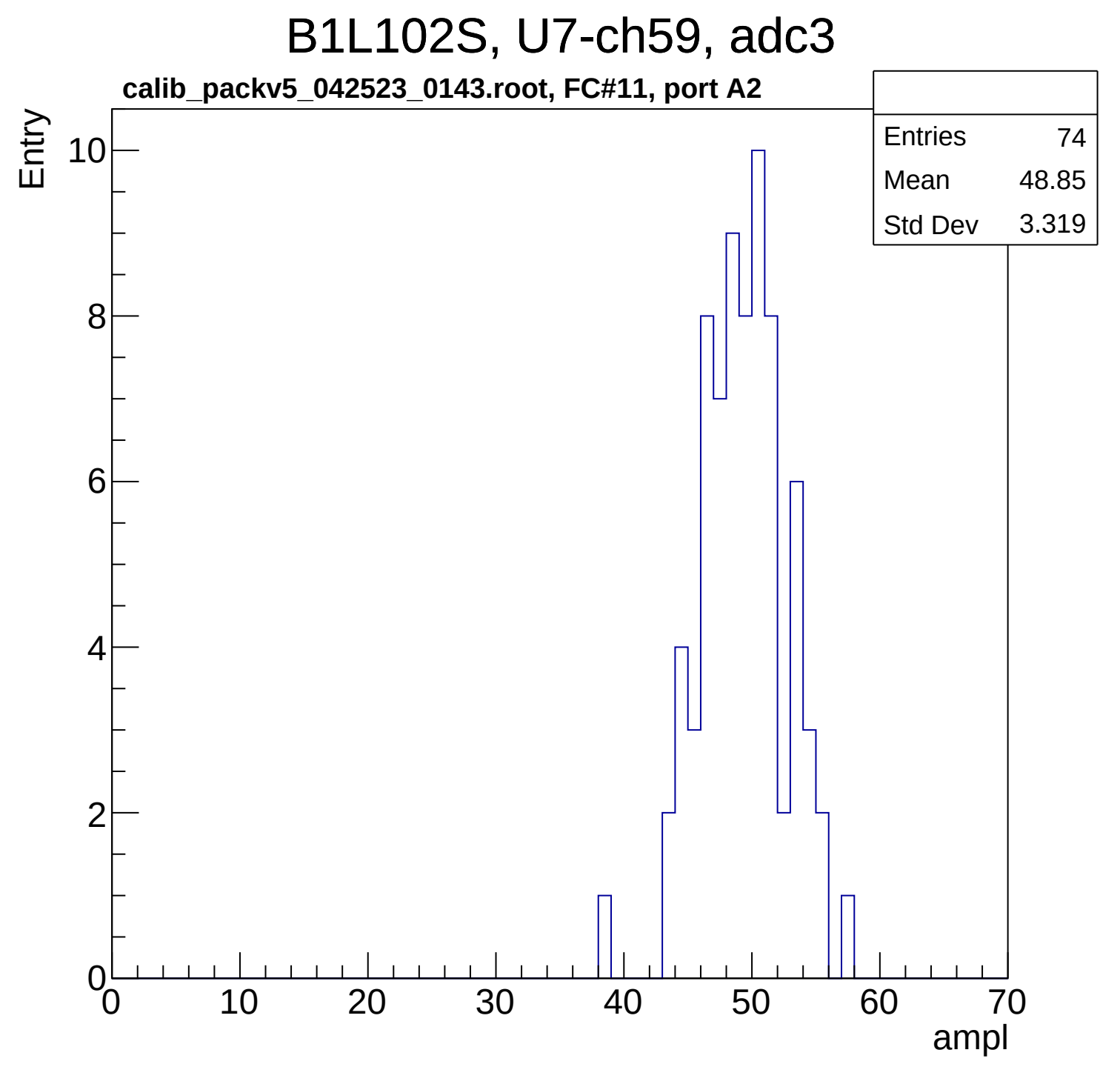
B1L102S, U7-ch59, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 74
Mean 48.85
Std Dev 3.319
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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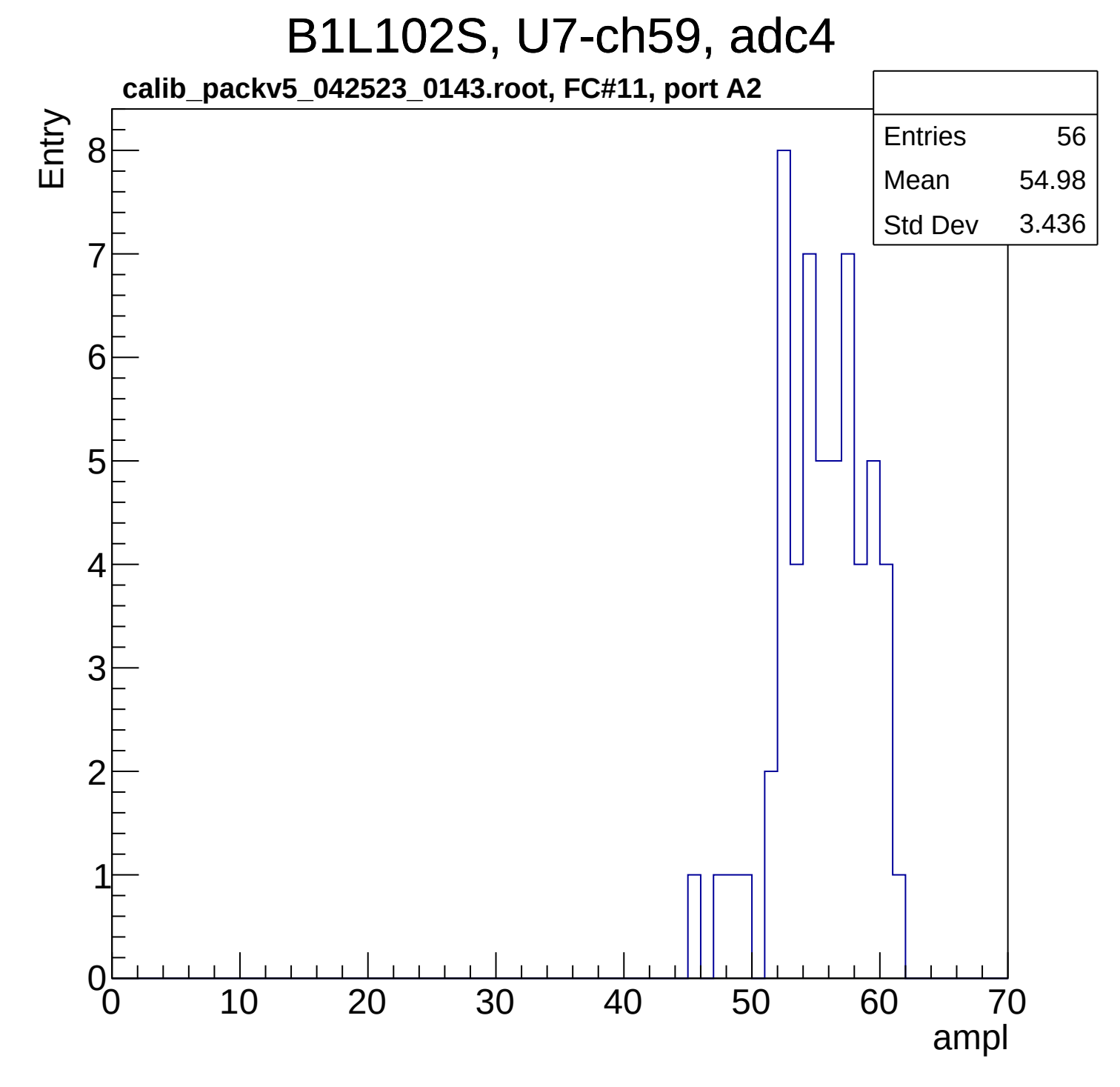
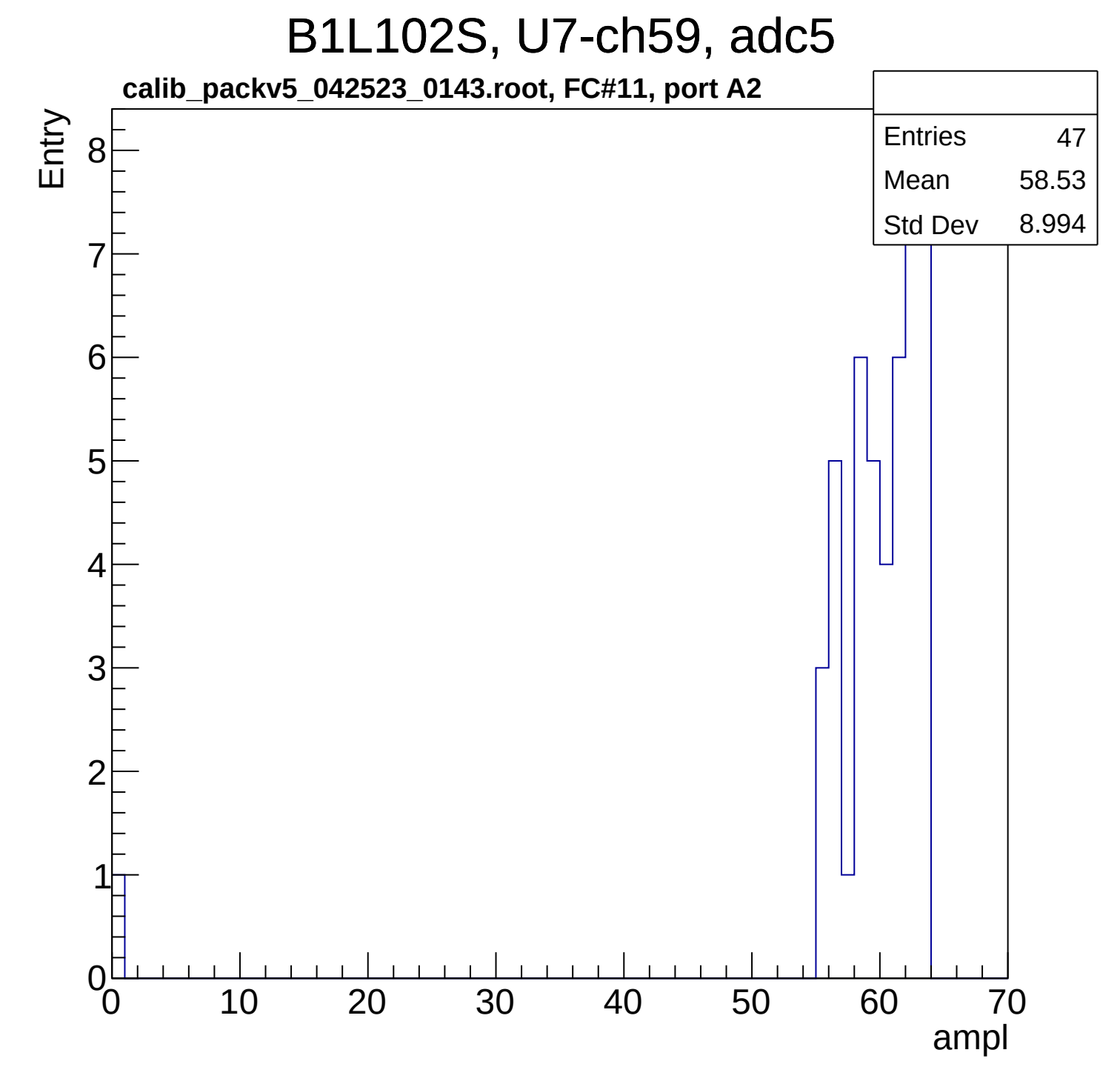
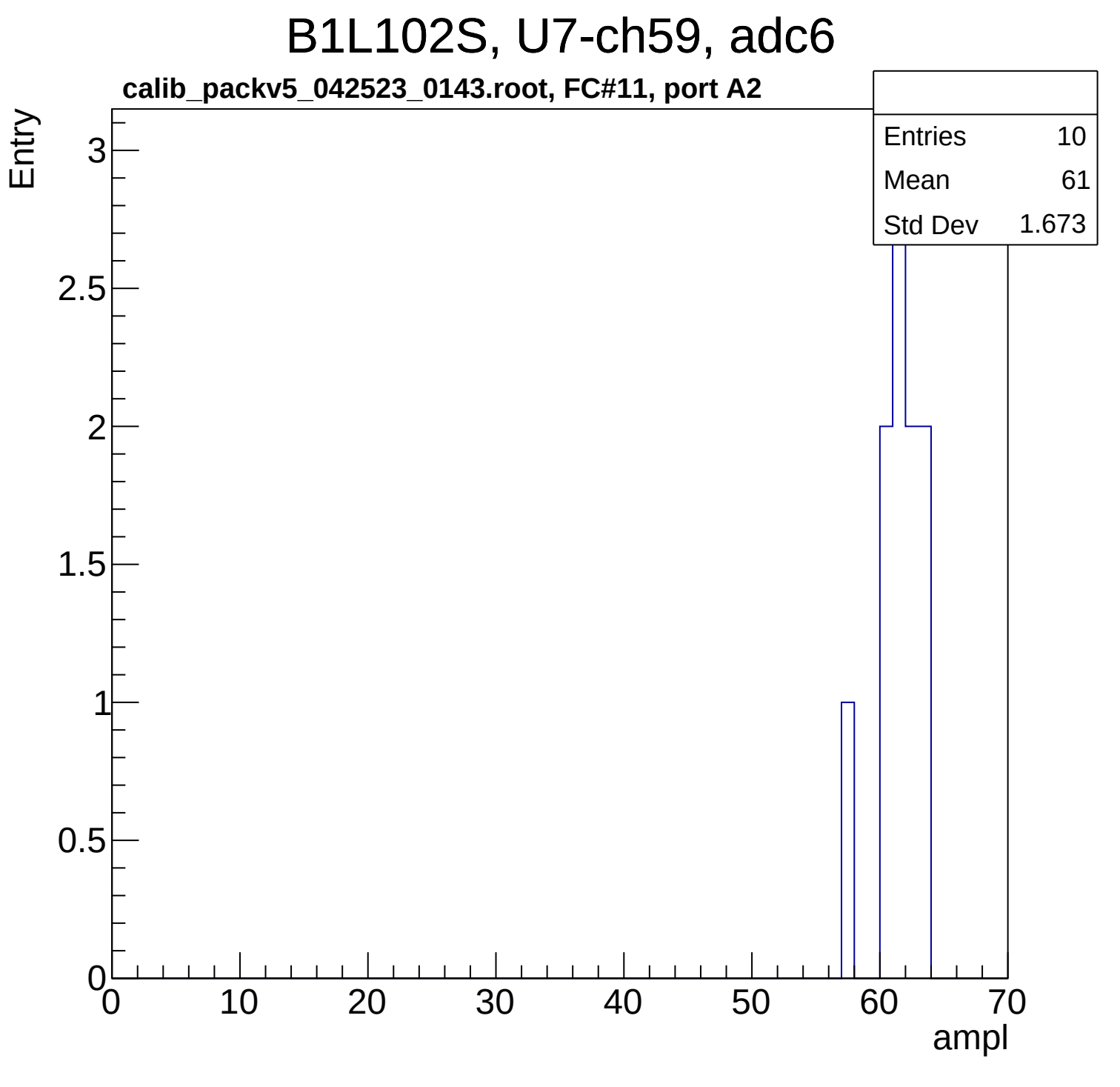

B1L102S, U7-ch59, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 56
Mean 54.98
Std Dev 3.436
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L102S, U7-ch59, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 47
Mean 58.53
Std Dev 8.994
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L102S, U7-ch59, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 10
Mean 61
Std Dev 1.673
Entry
ampl
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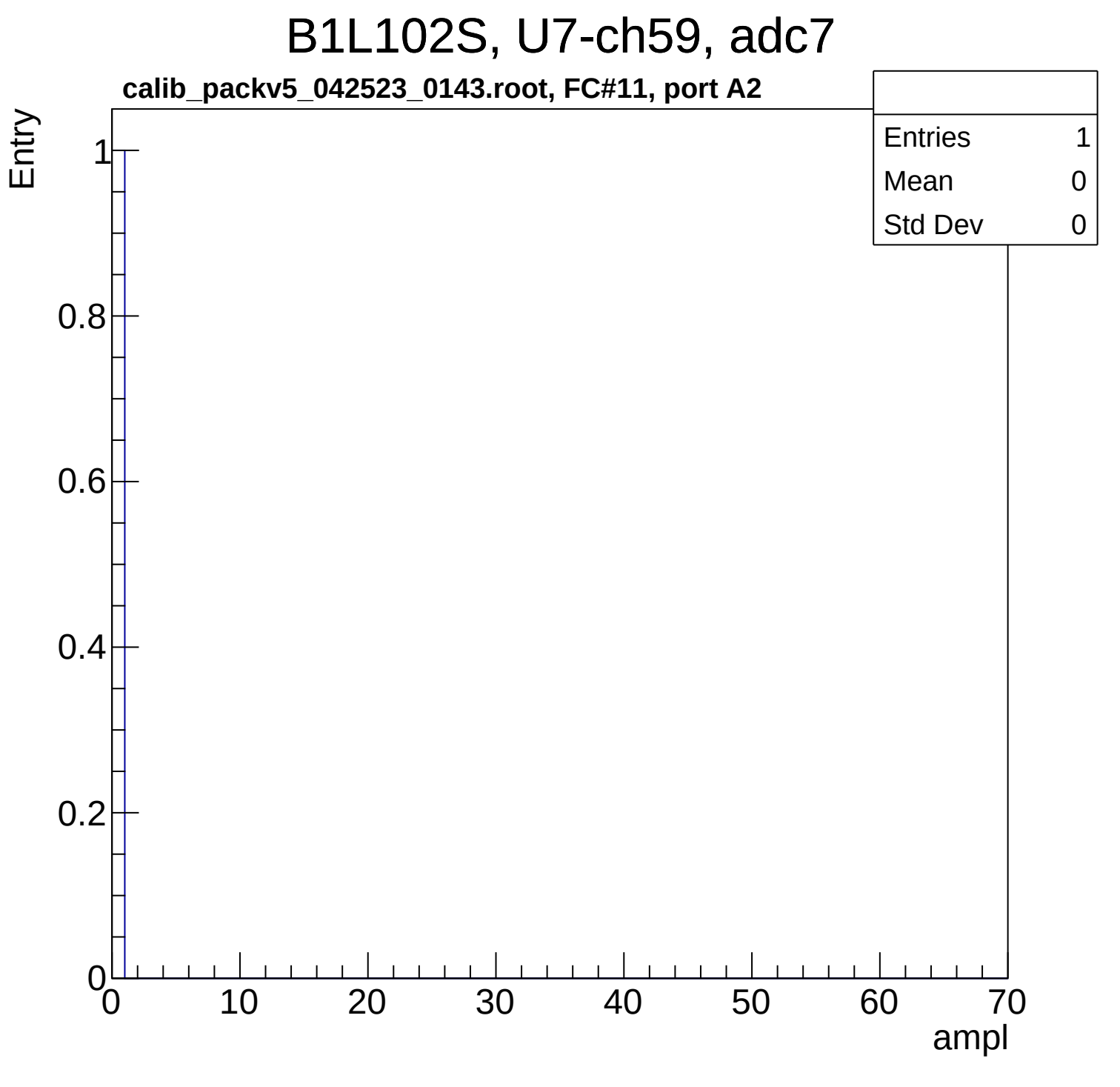
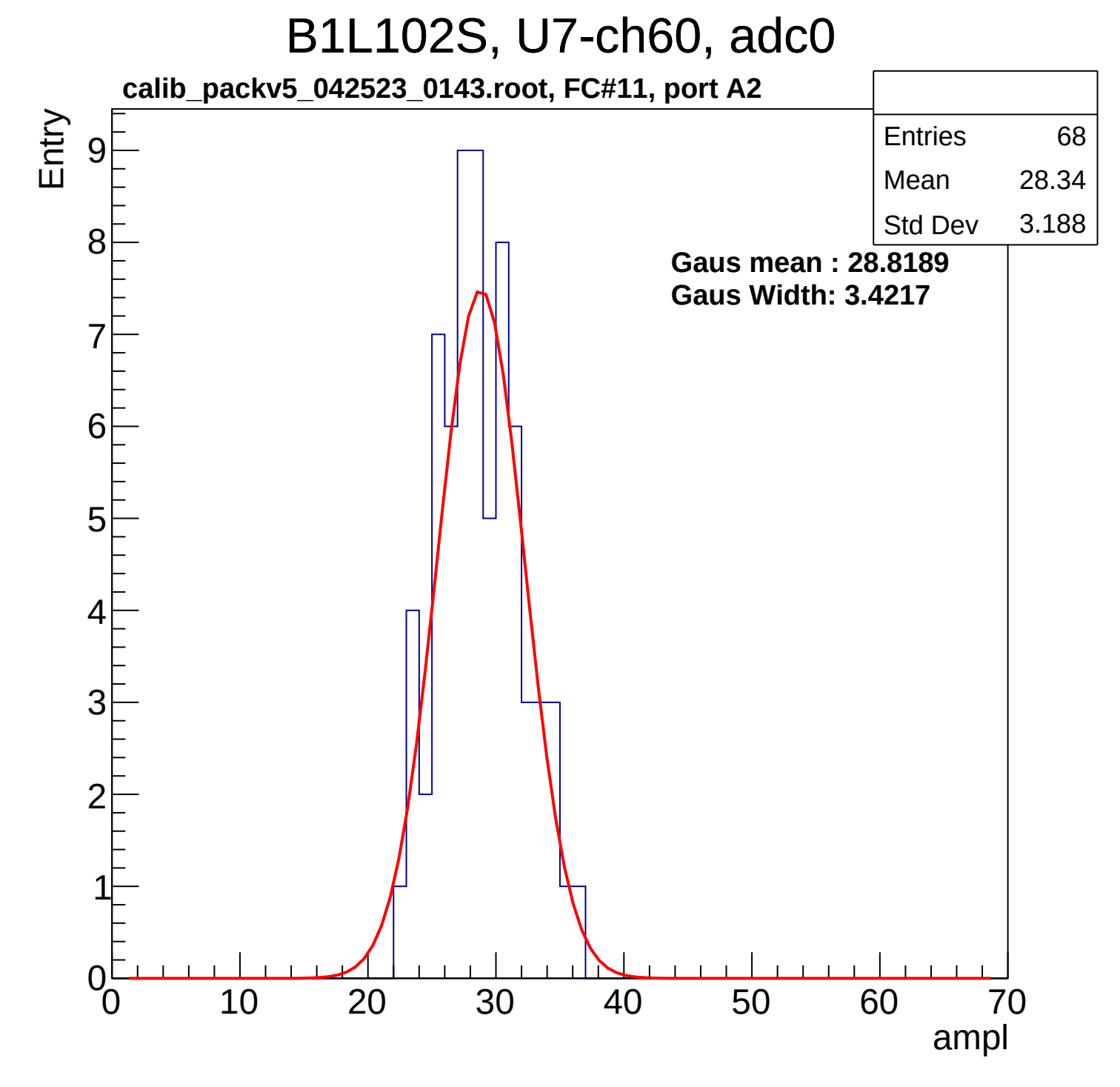
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L102S, U7-ch59, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U7-ch60, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 68
Mean 28.34
Std Dev 3.188
Gaus mean : 28.8189
Gaus Width: 3.4217
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
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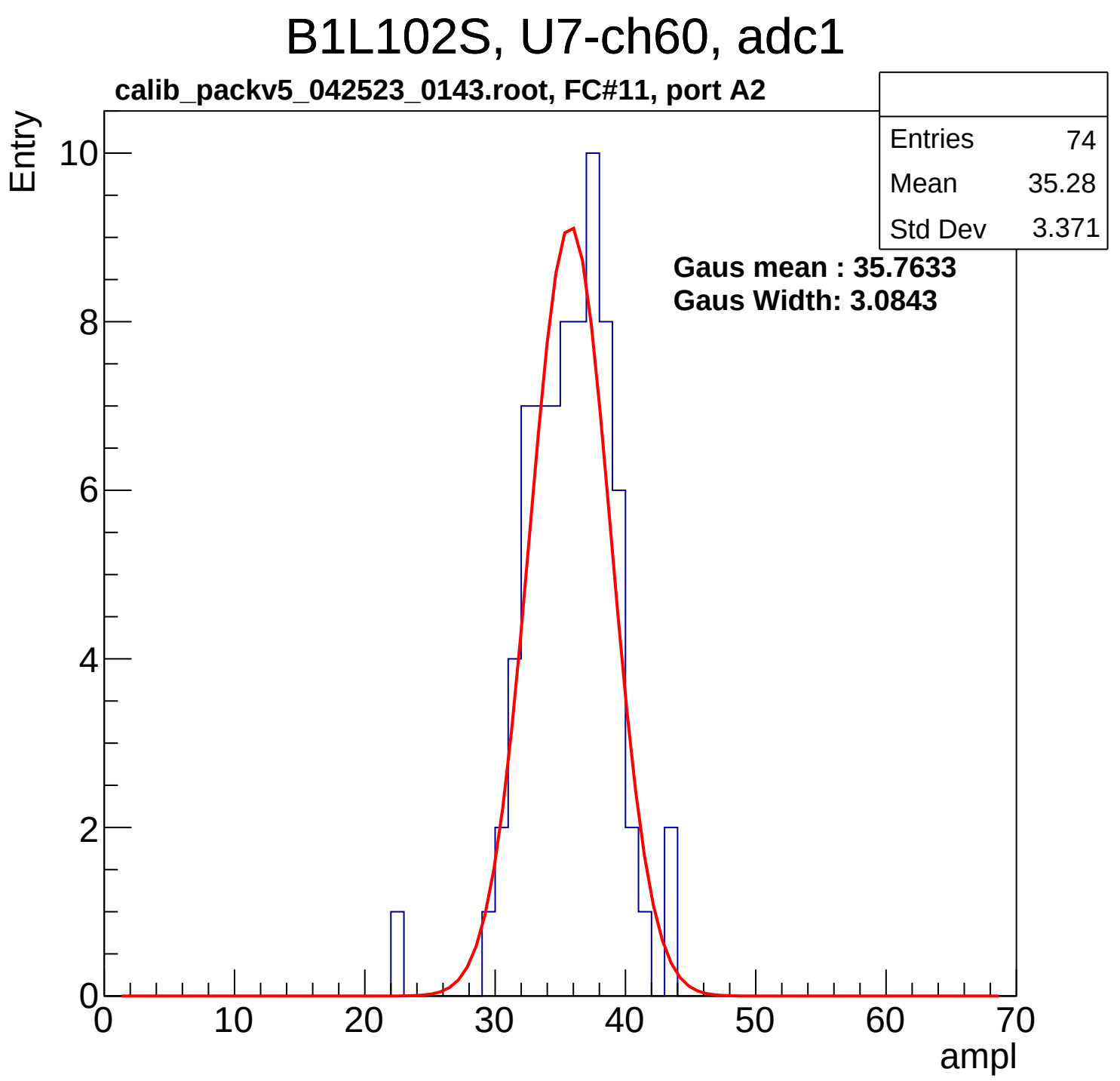
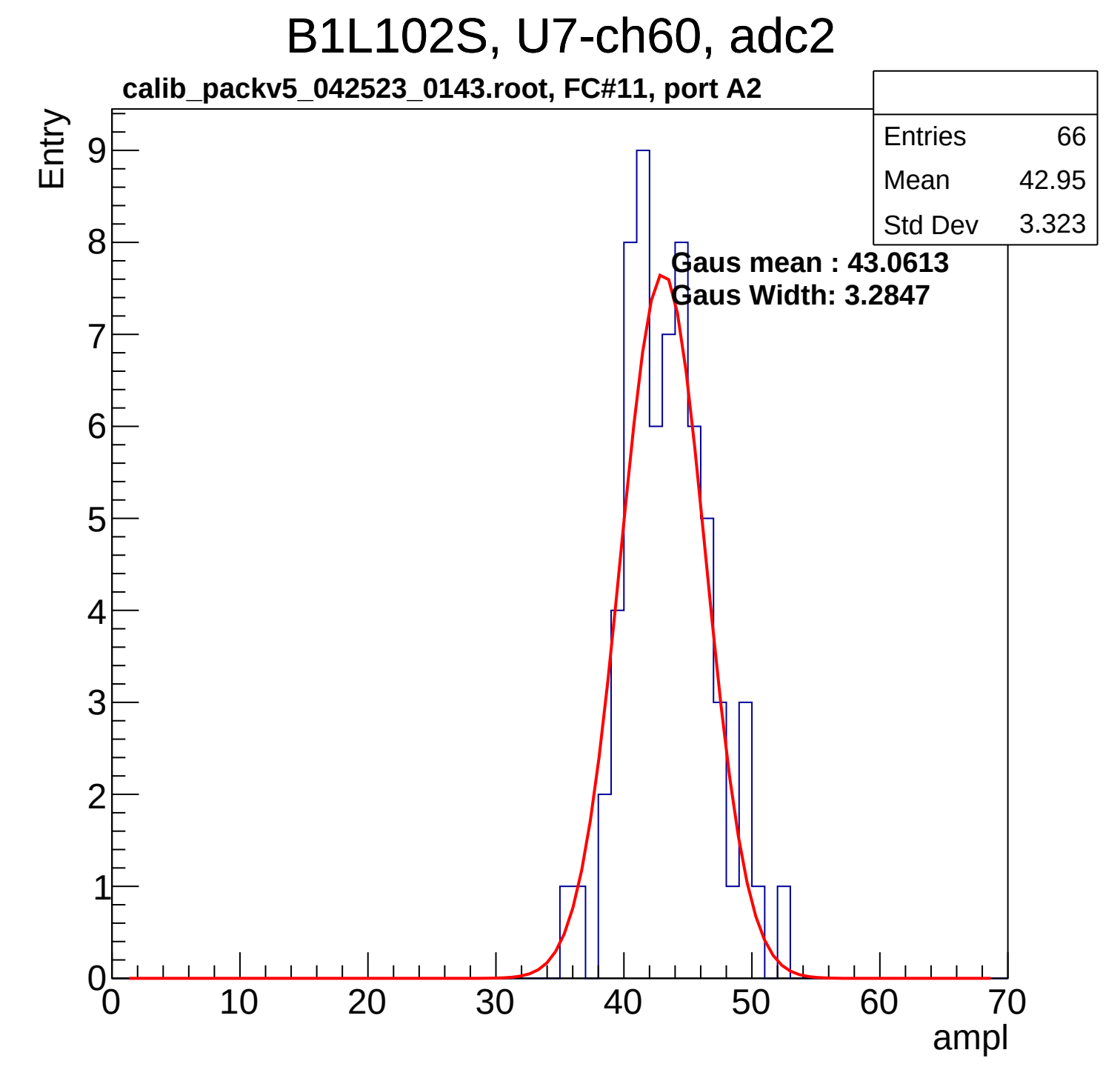
60
70


B1L102S, U7-ch60, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 74
Mean 35.28
Std Dev 3.371
Gaus mean : 35.7633
Gaus Width: 3.0843
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L102S, U7-ch60, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 66
Mean 42.95
Std Dev 3.323
Gaus mean : 43.0613
Gaus Width: 3.2847
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
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40
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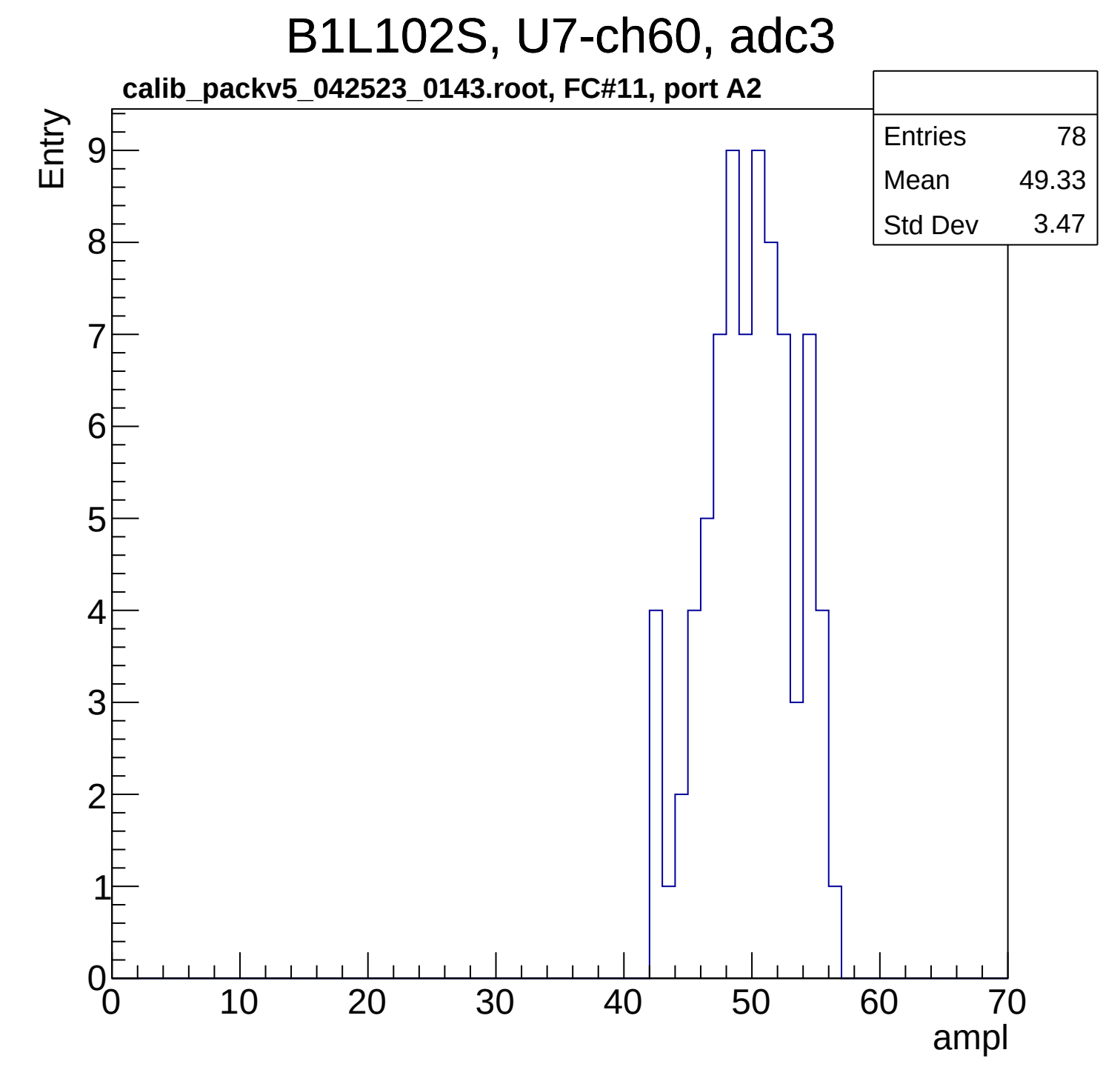
60
70


B1L102S, U7-ch60, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 78
Mean 49.33
Std Dev 3.47
Entry
ampl
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3
4
5
6
7
8
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0
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60
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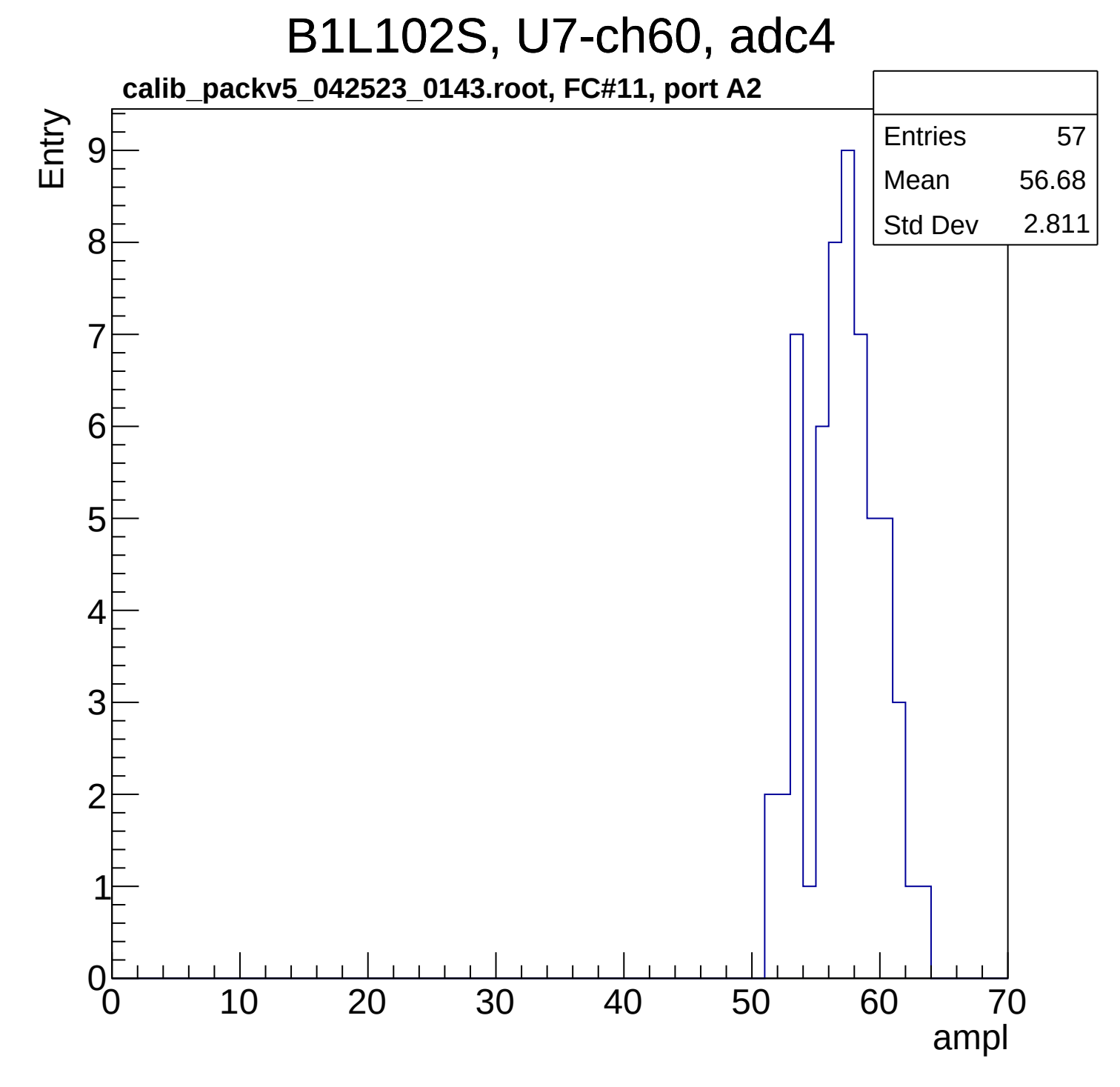
B1L102S, U7-ch60, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 57
Mean 56.68
Std Dev 2.811
Entry
ampl
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2
3
4
5
6
7
8
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0
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40
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60
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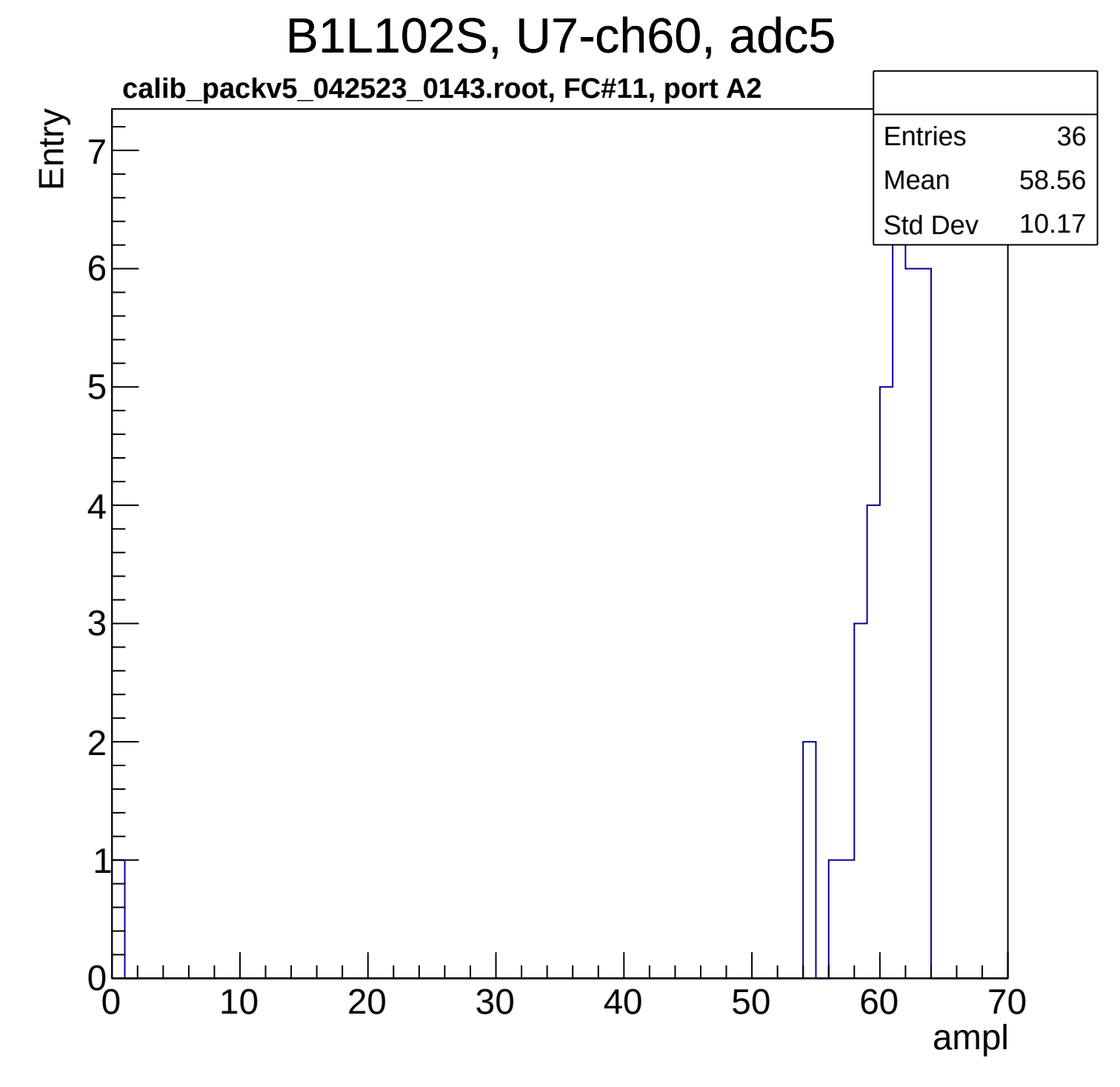
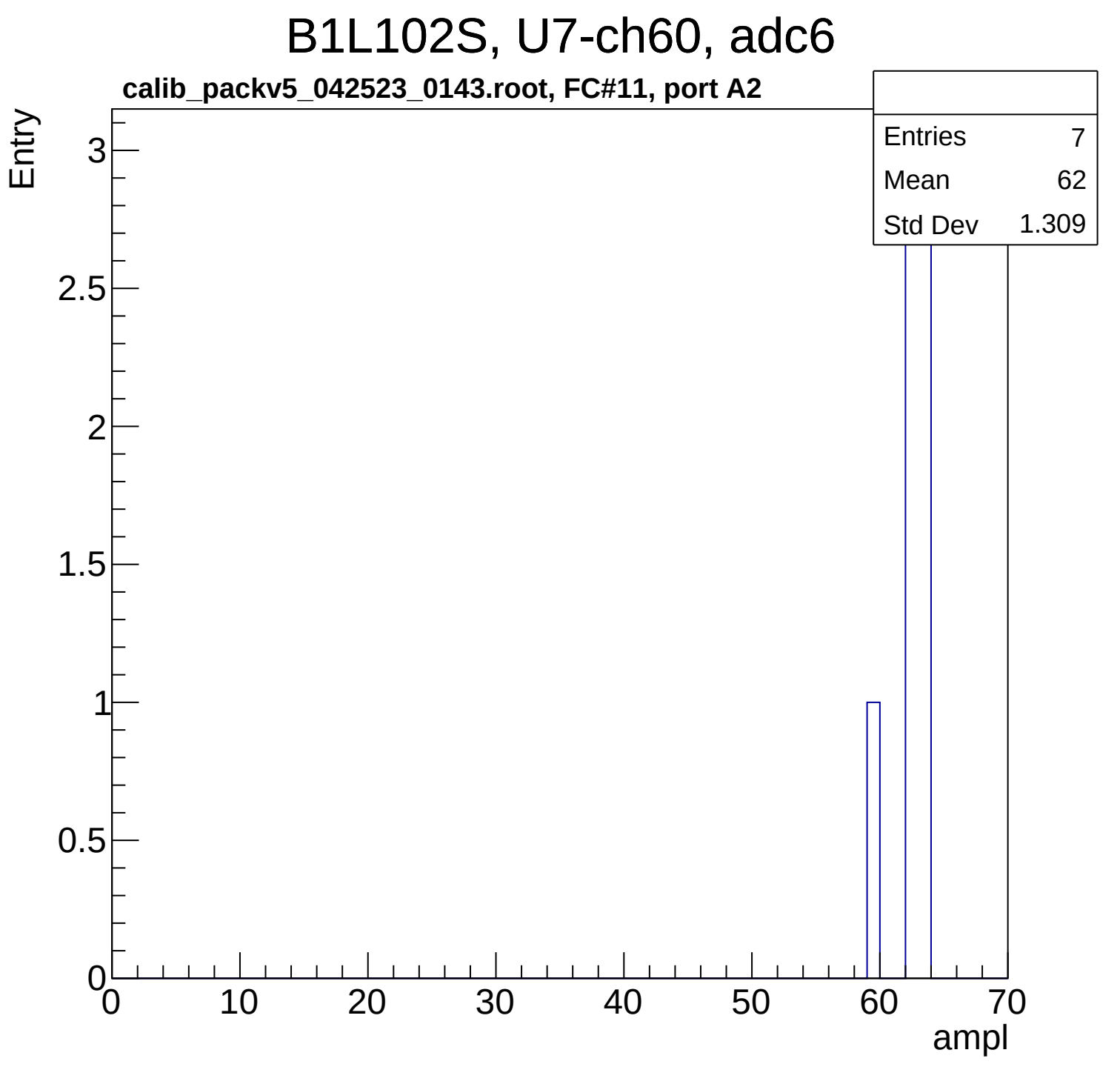

B1L102S, U7-ch60, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 36
Mean 58.56
Std Dev 10.17
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L102S, U7-ch60, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 7
Mean 62
Std Dev 1.309
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
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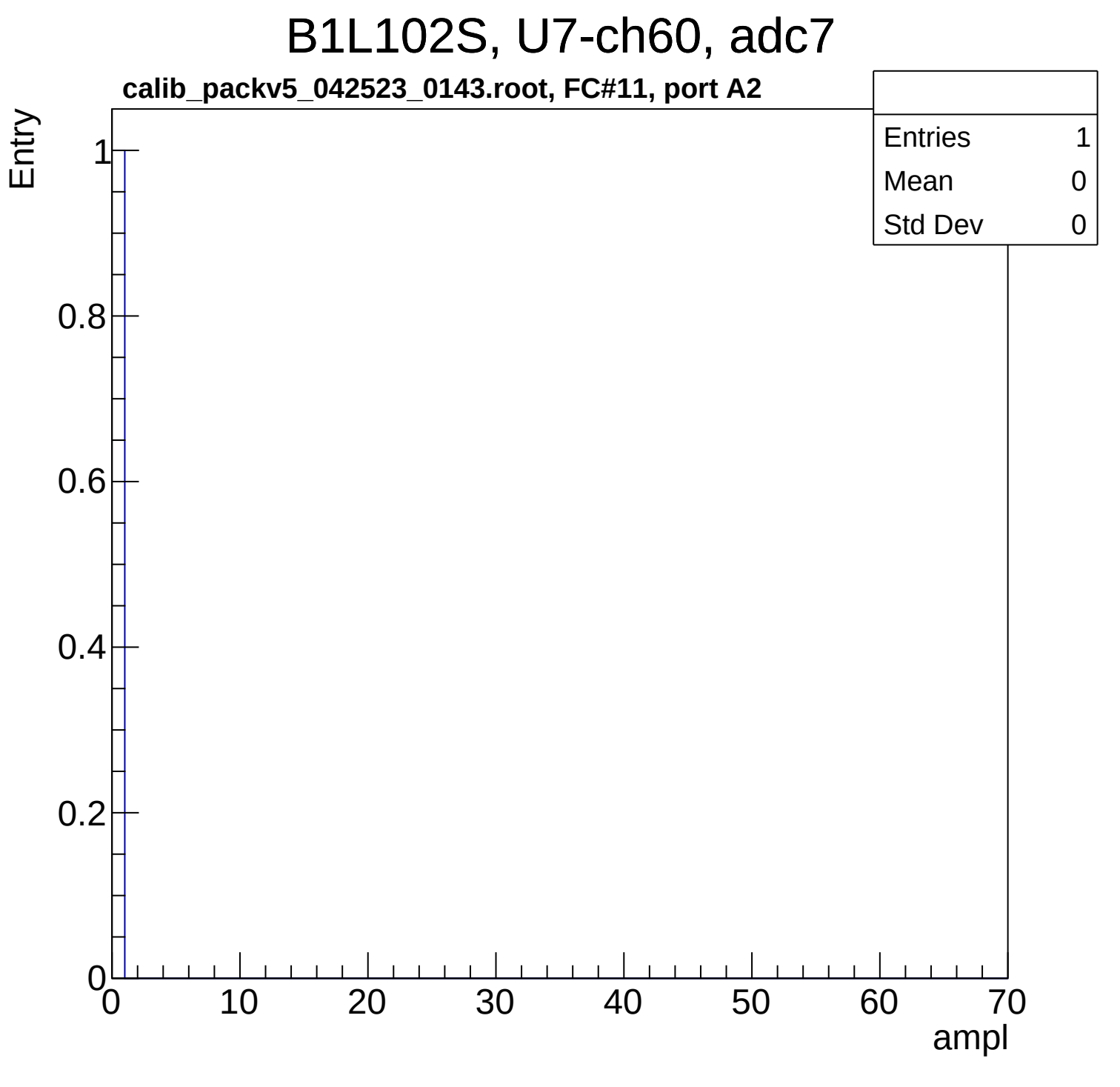
20
30
40
50
60
70


B1L102S, U7-ch60, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 1
Mean 0
Std Dev 0
Entry
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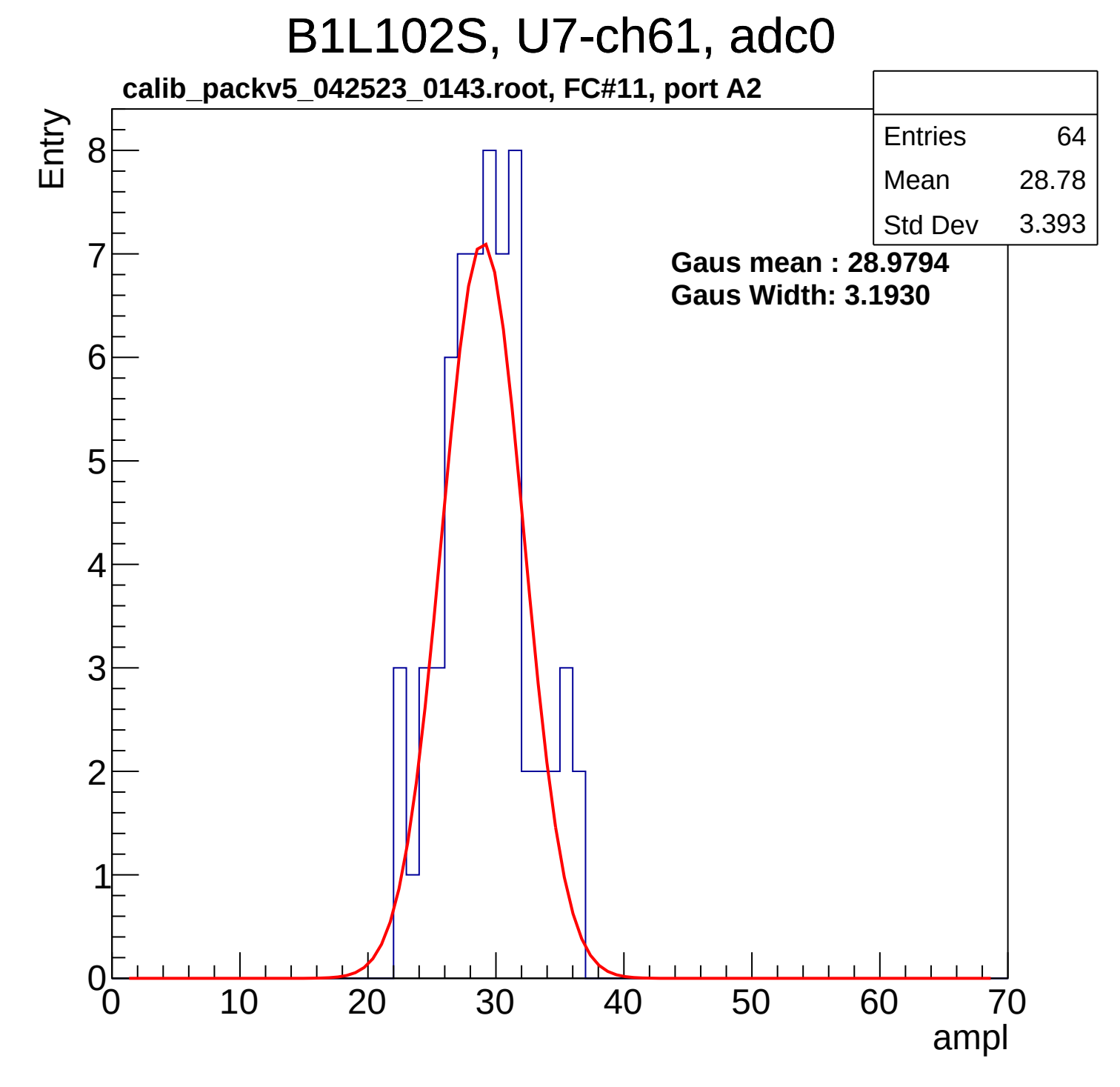
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U7-ch61, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 64
Mean 28.78
Std Dev 3.393
Gaus mean : 28.9794
Gaus Width: 3.1930
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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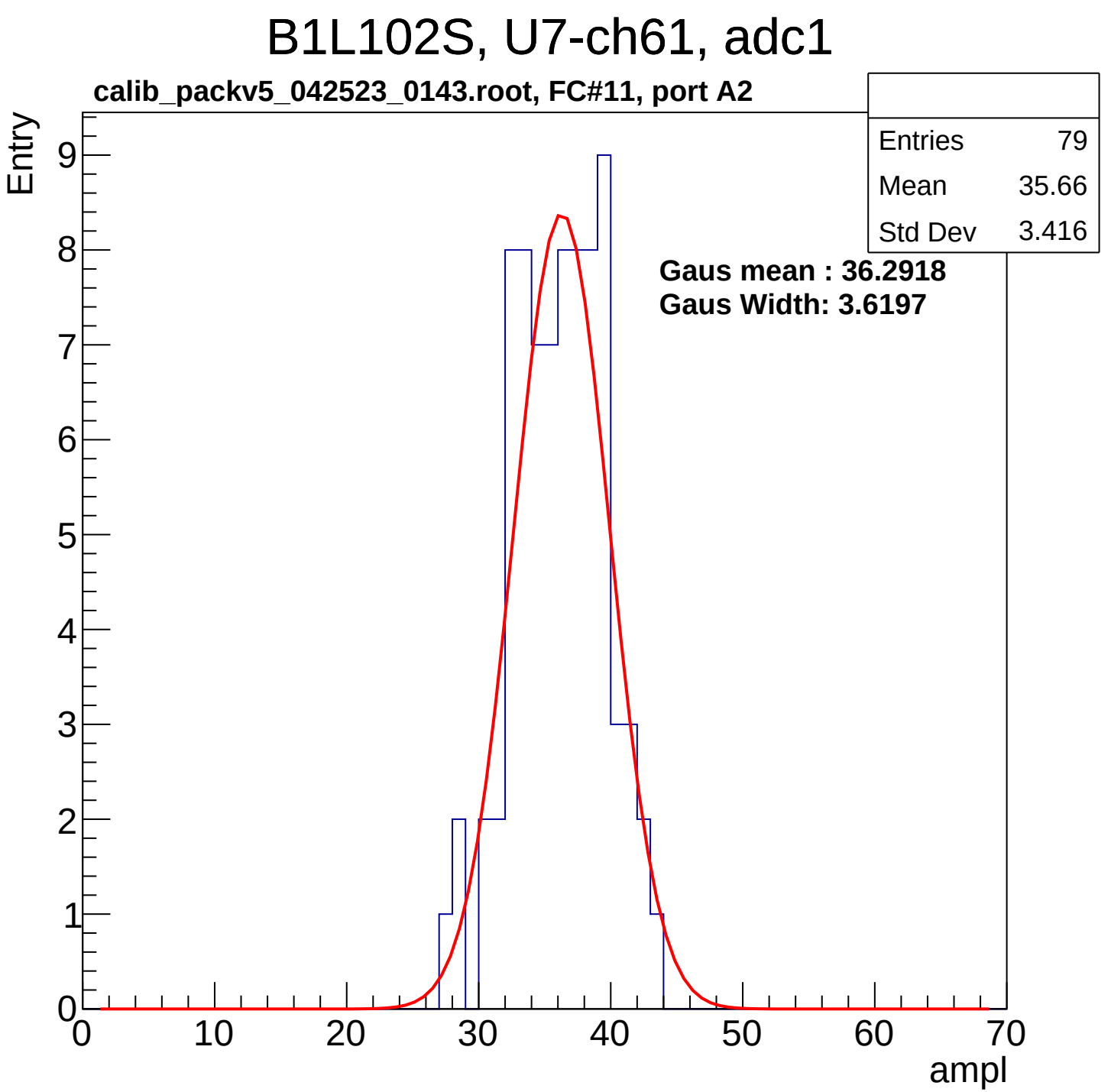
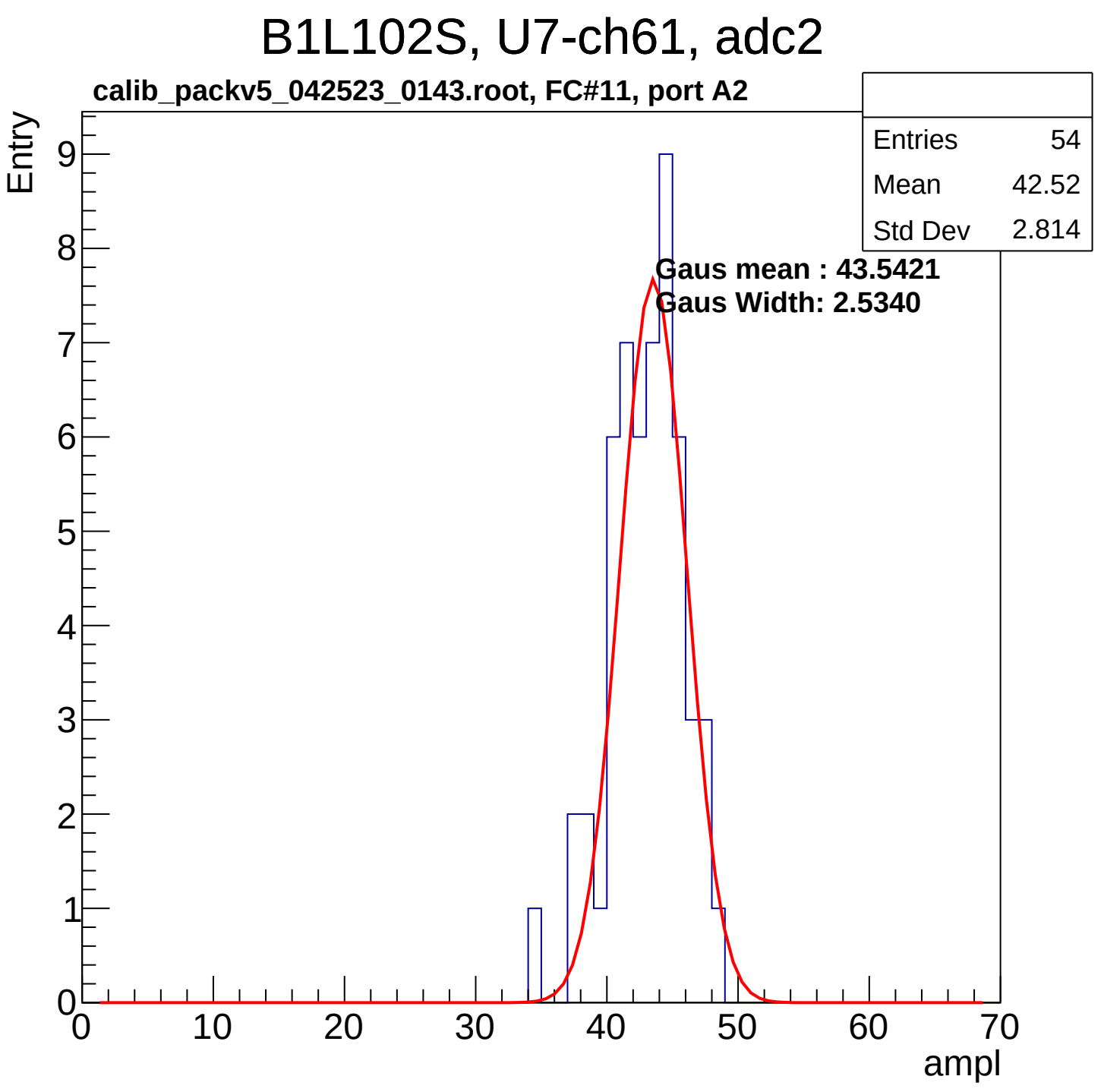

B1L102S, U7-ch61, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 79
Mean 35.66
Std Dev 3.416
Gaus mean : 36.2918
Gaus Width: 3.6197
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L102S, U7-ch61, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 54
Mean 42.52
Std Dev 2.814
Gaus mean : 43.5421
Gaus Width: 2.5340
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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60
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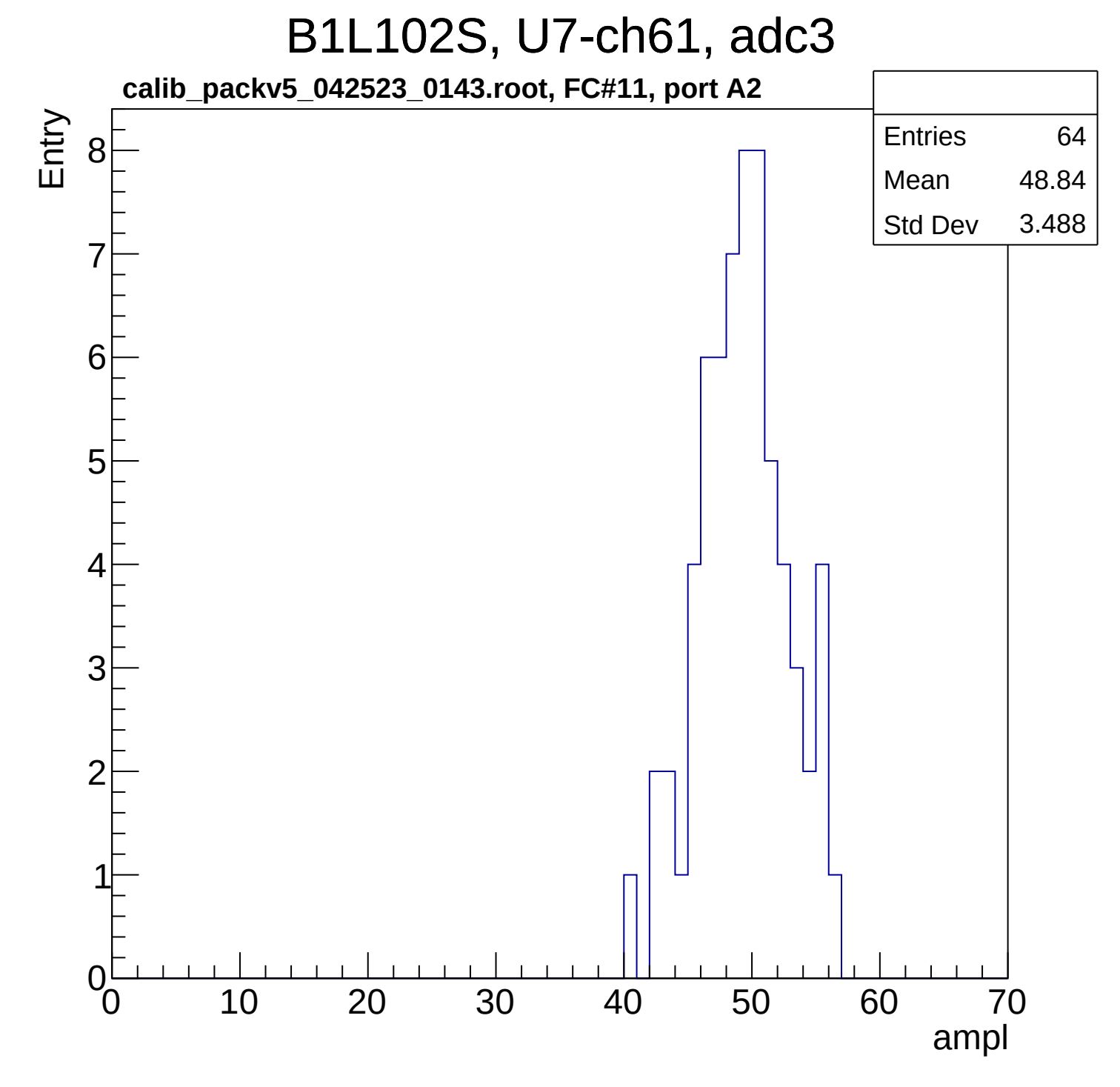
B1L102S, U7-ch61, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 64
Mean 48.84
Std Dev 3.488
Entry
ampl
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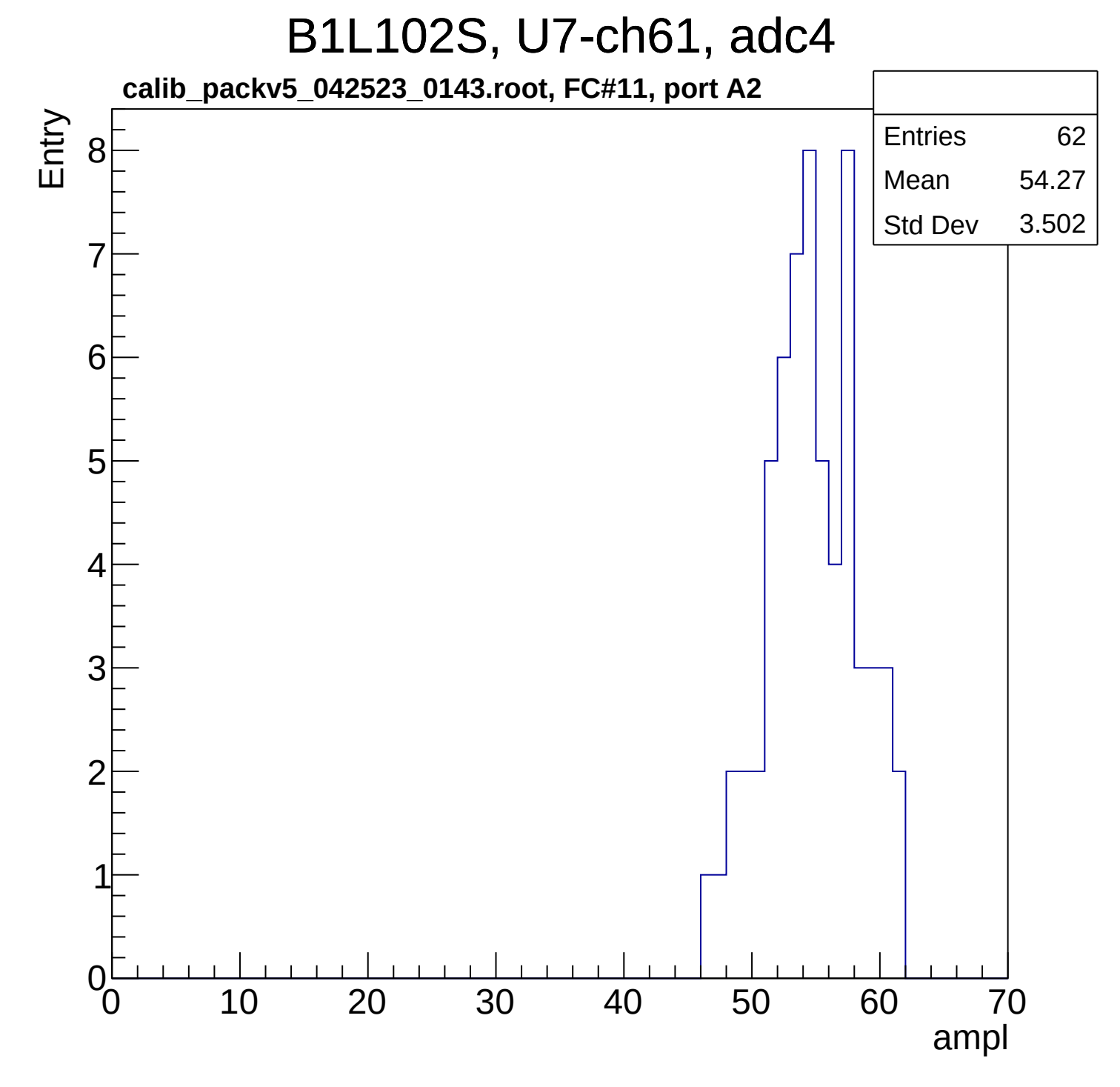
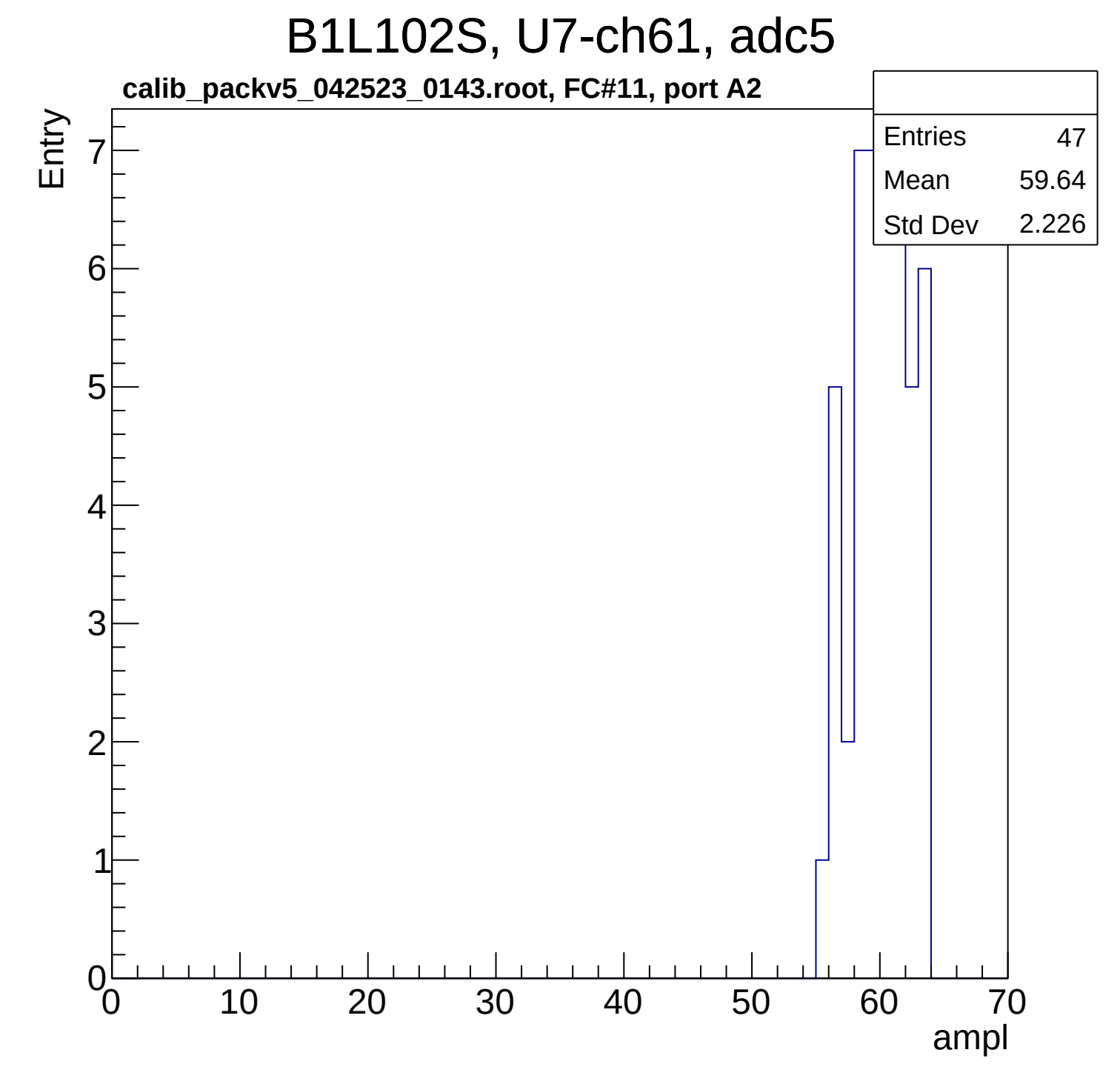

B1L102S, U7-ch61, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 62
Mean 54.27
Std Dev 3.502
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L102S, U7-ch61, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 47
Mean 59.64
Std Dev 2.226
Entry
ampl
0
1
2
3
4
5
6
7
0
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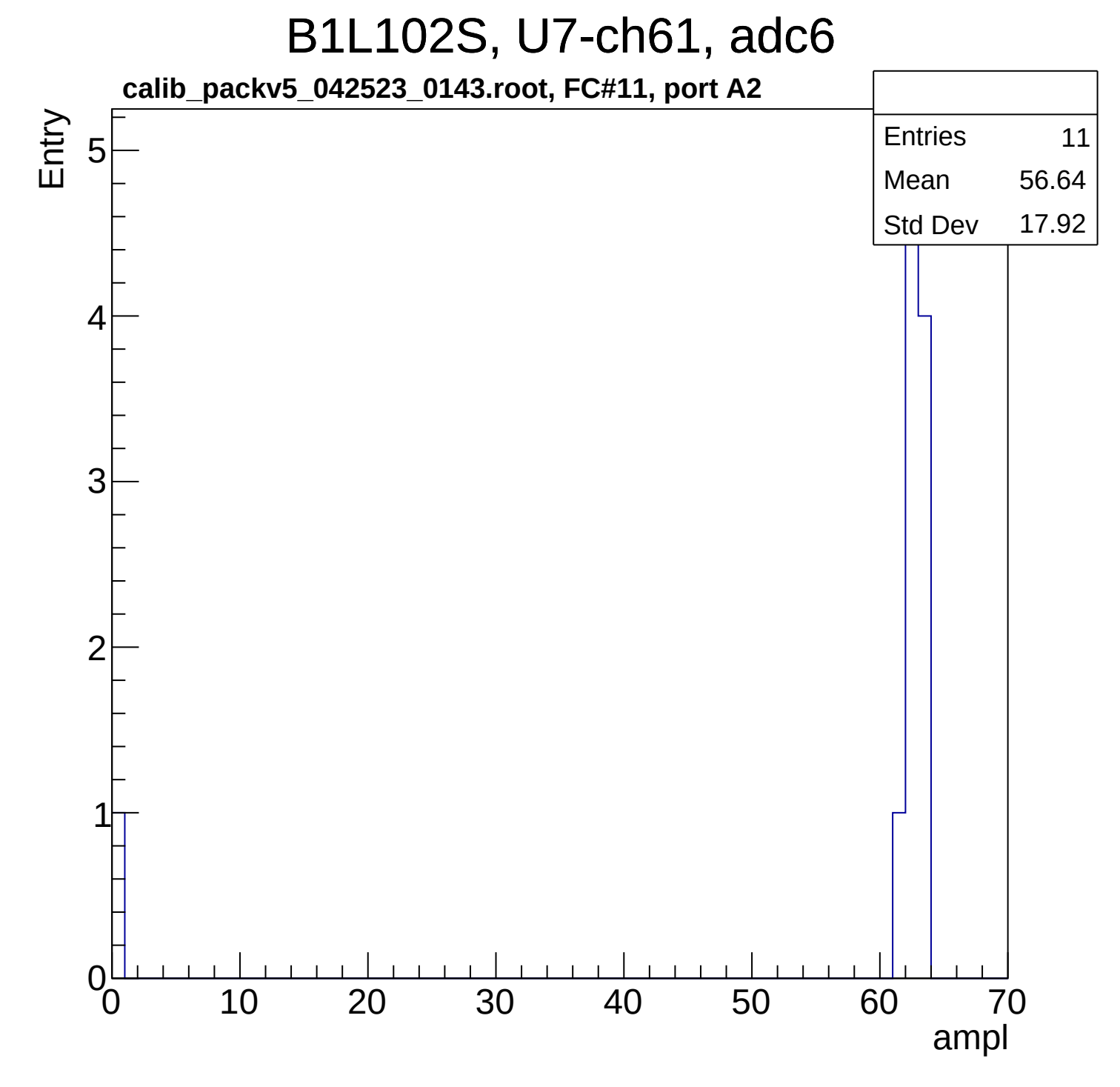
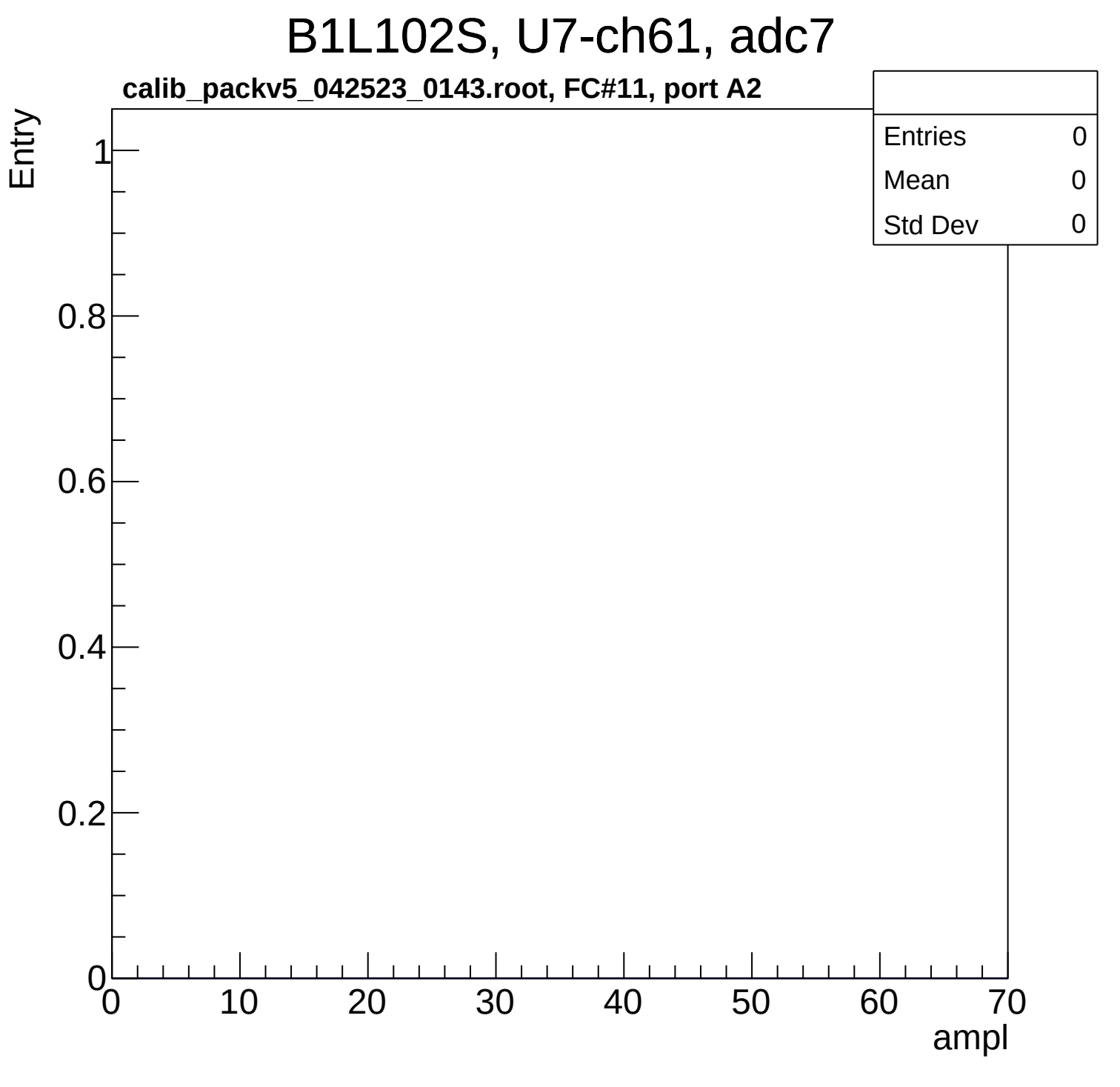
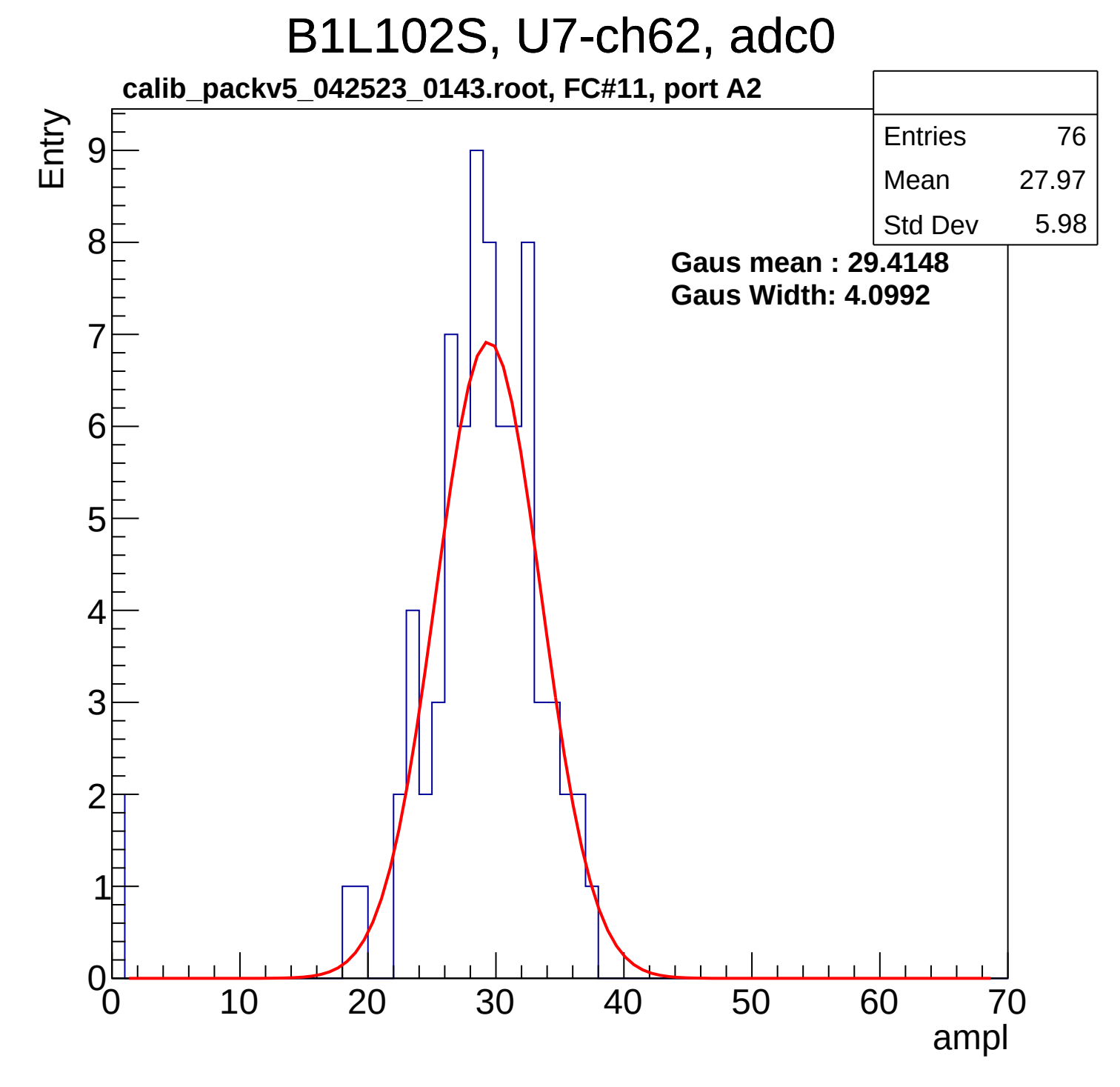
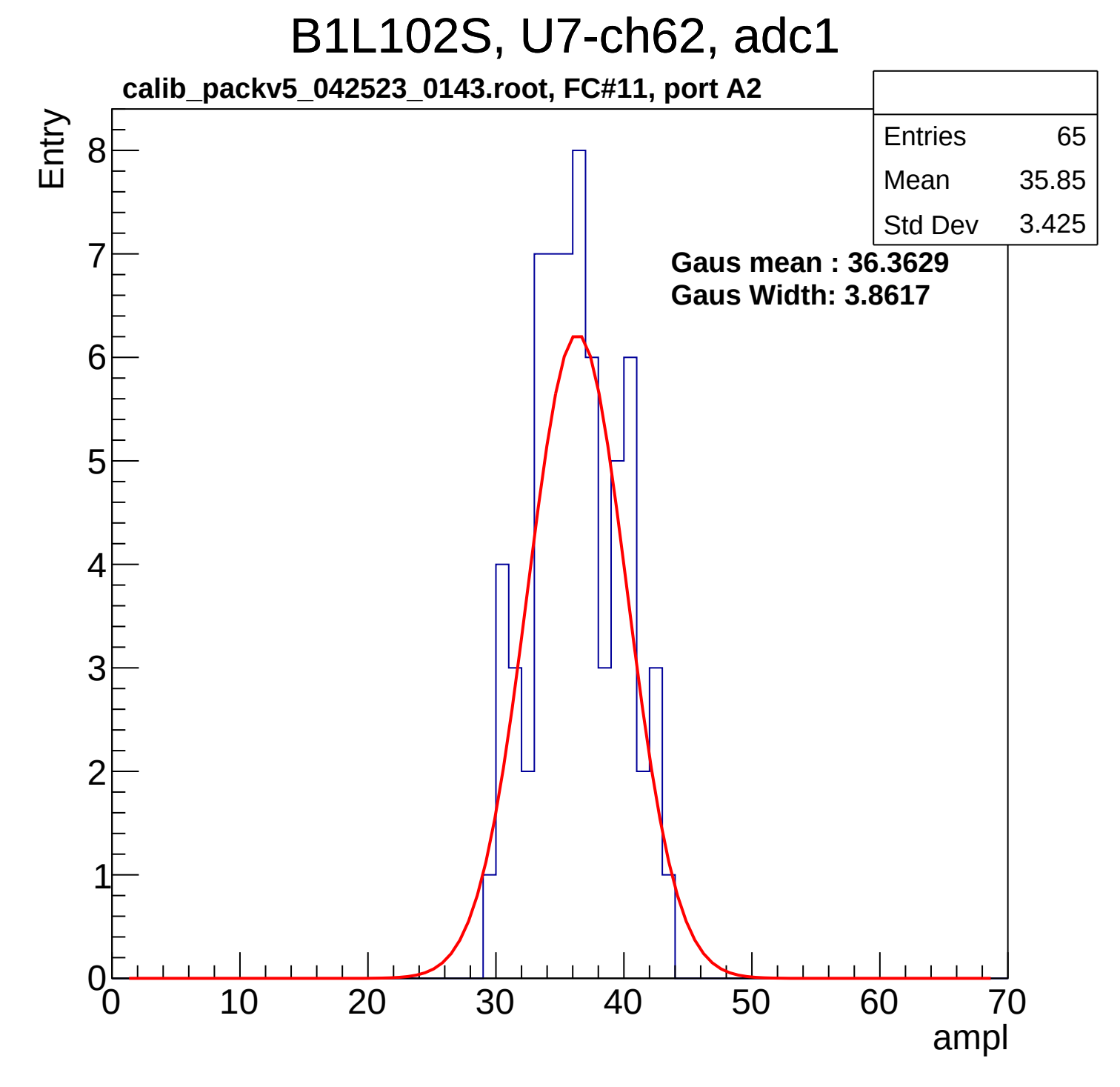
20
30
40
50
60
70


B1L102S, U7-ch61, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 11
Mean 56.64
Std Dev 17.92
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L102S, U7-ch61, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U7-ch62, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 76
Mean 27.97
Std Dev 5.98
Gaus mean : 29.4148
Gaus Width: 4.0992
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L102S, U7-ch62, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 65
Mean 35.85
Std Dev 3.425
Gaus mean : 36.3629
Gaus Width: 3.8617
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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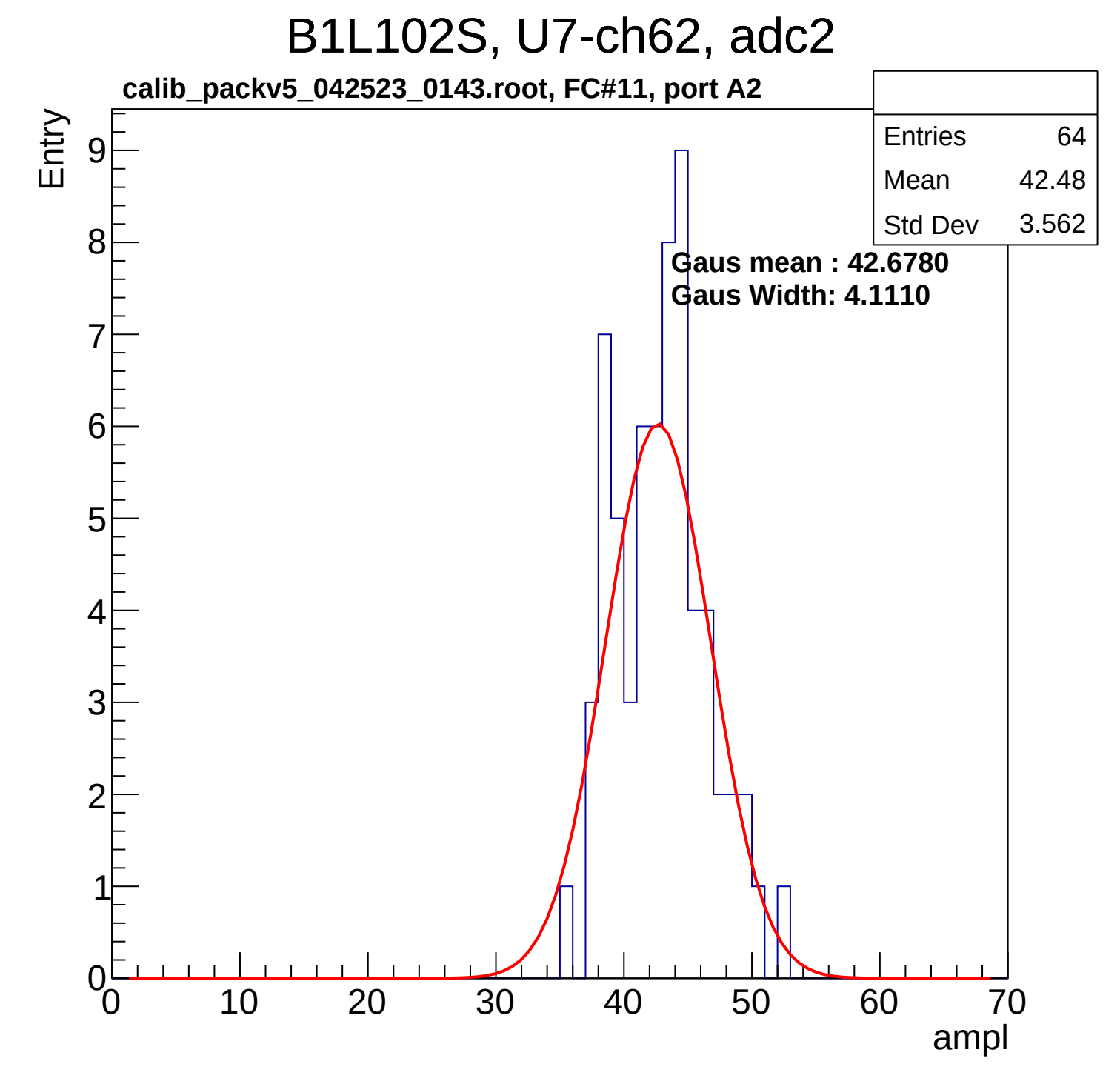
B1L102S, U7-ch62, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 64
Mean 42.48
Std Dev 3.562
Gaus mean : 42.6780
Gaus Width: 4.1110
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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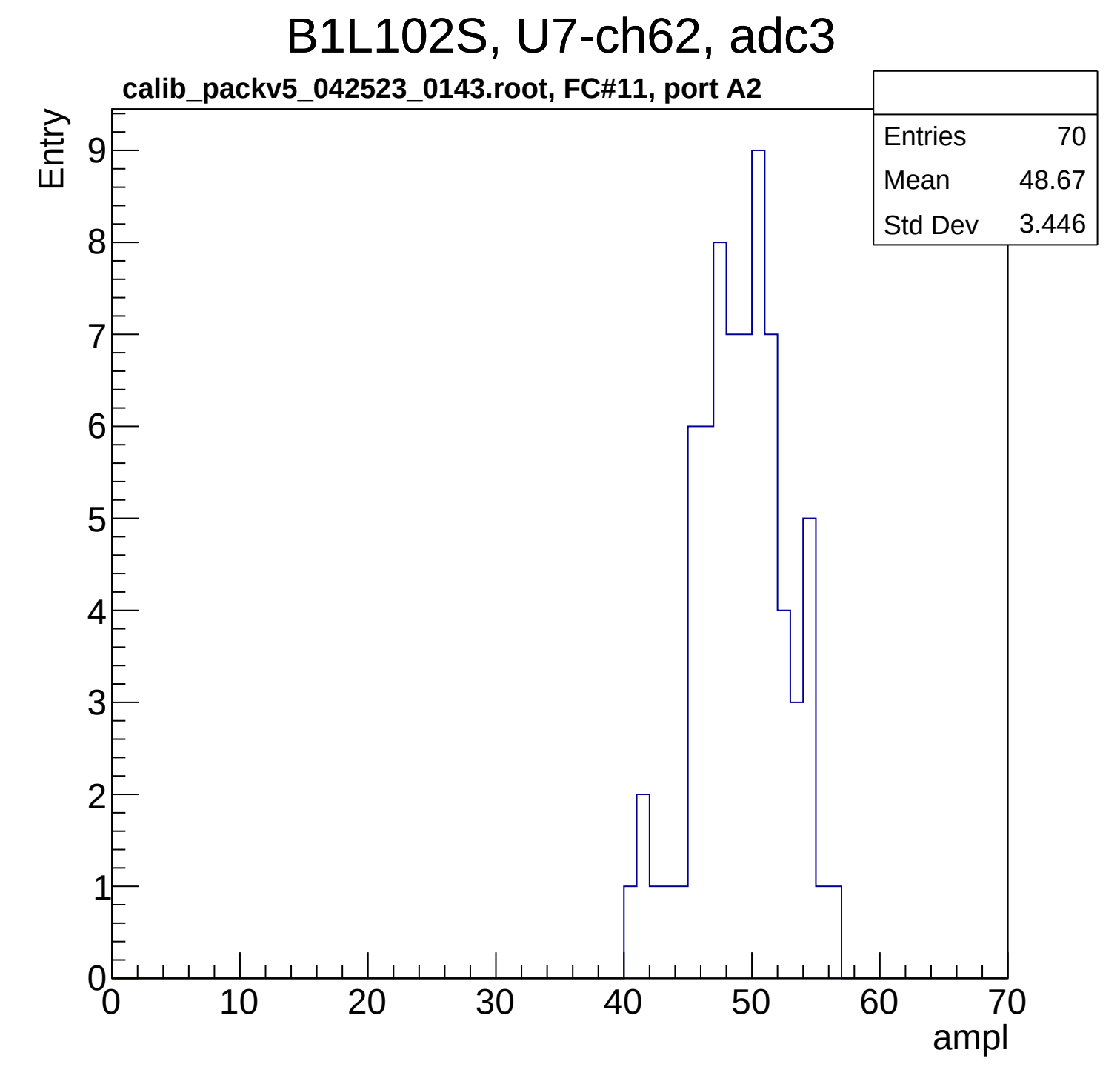
B1L102S, U7-ch62, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 70
Mean 48.67
Std Dev 3.446
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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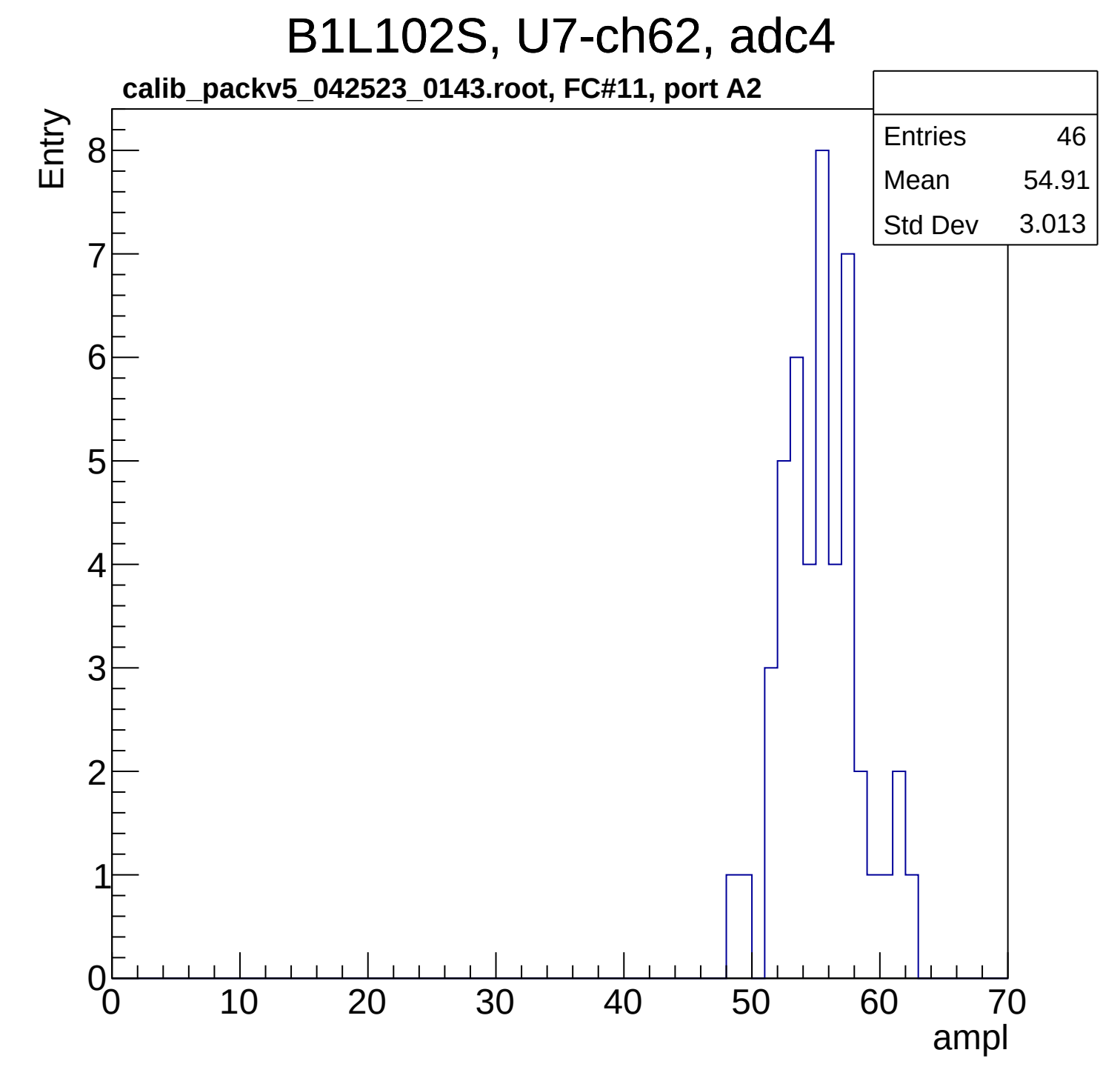
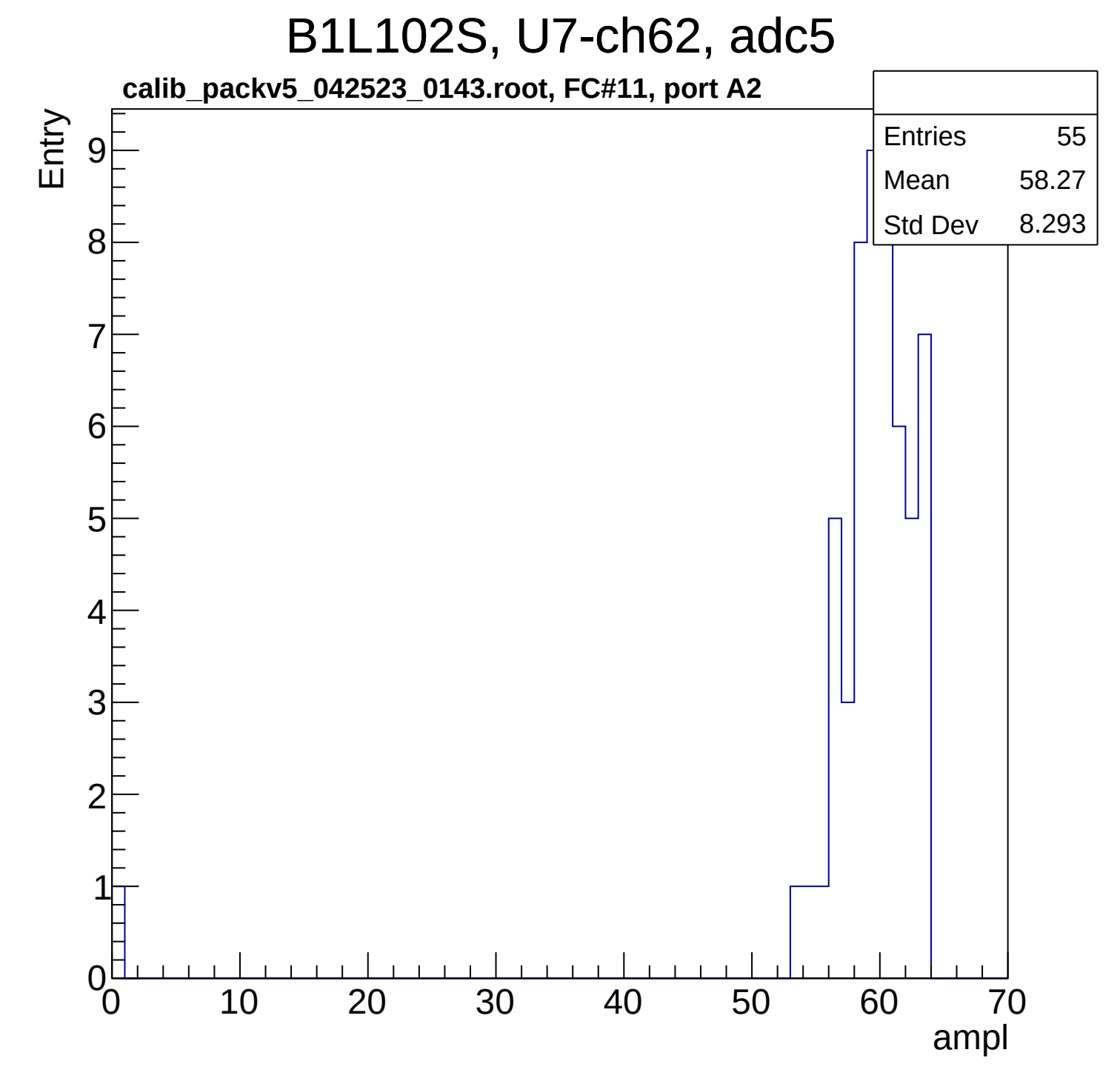
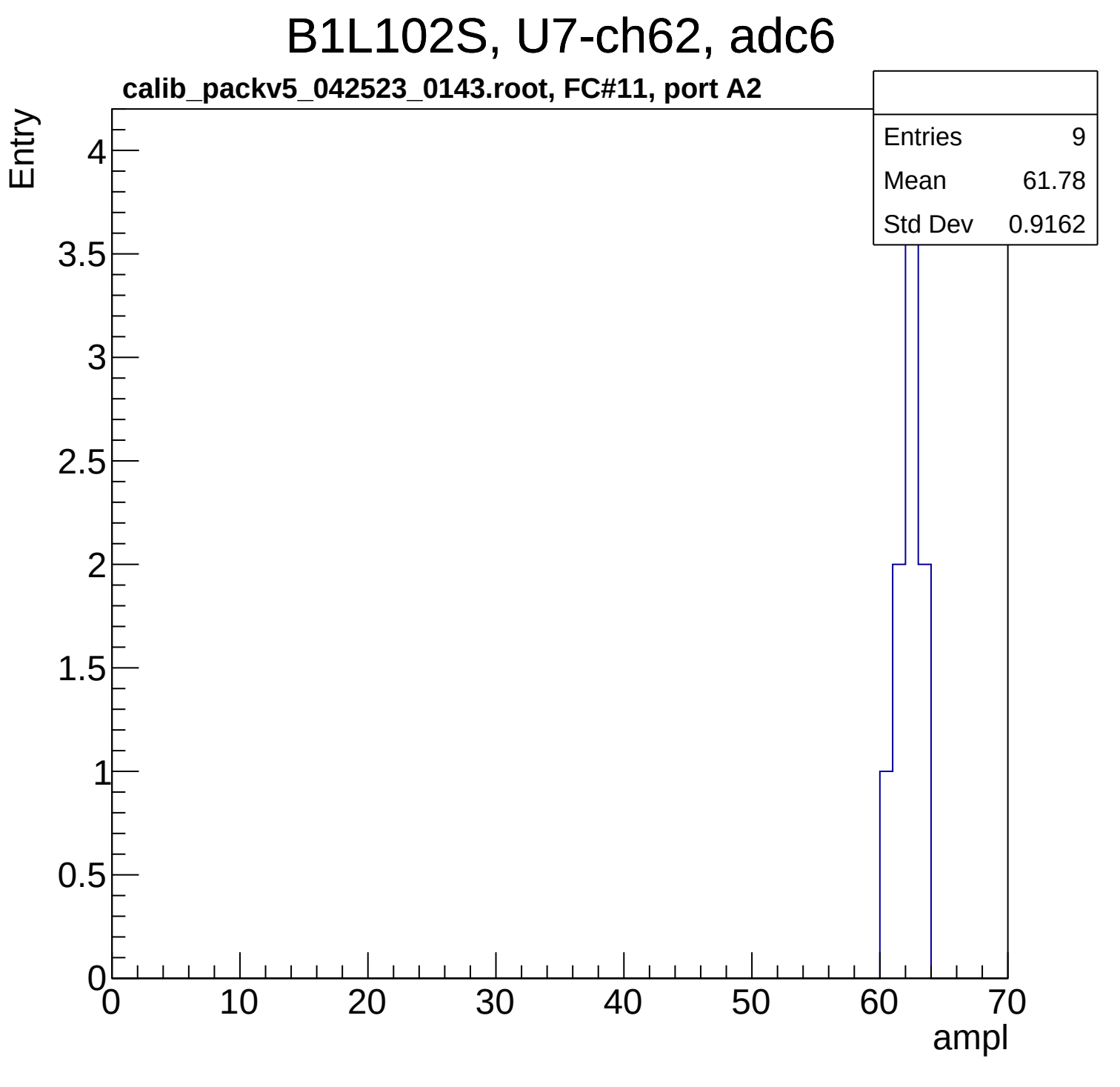
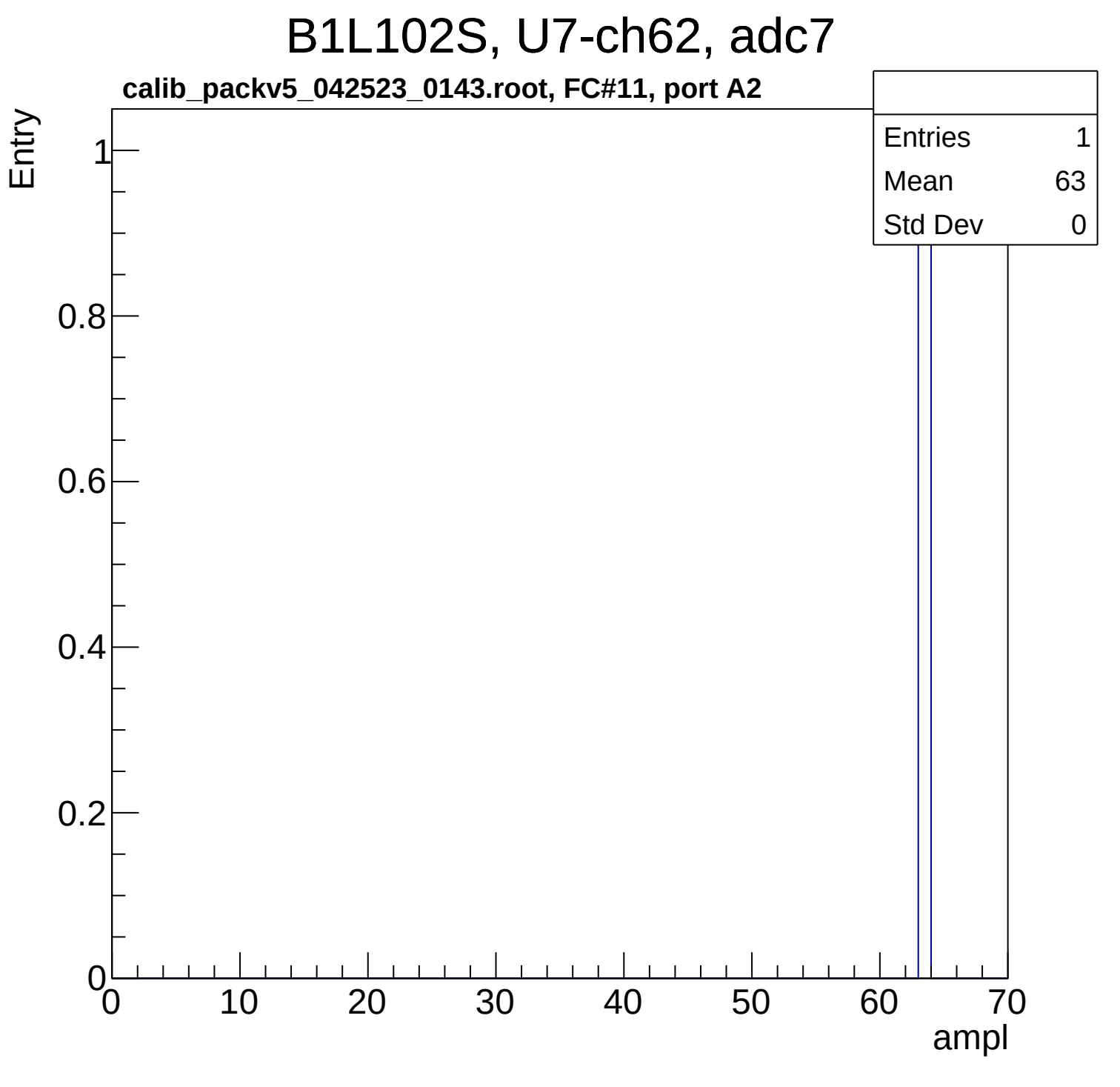

B1L102S, U7-ch62, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 46
Mean 54.91
Std Dev 3.013
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L102S, U7-ch62, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 55
Mean 58.27
Std Dev 8.293
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L102S, U7-ch62, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 9
Mean 61.78
Std Dev 0.9162
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L102S, U7-ch62, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 1
Mean 63
Std Dev 0
Entry
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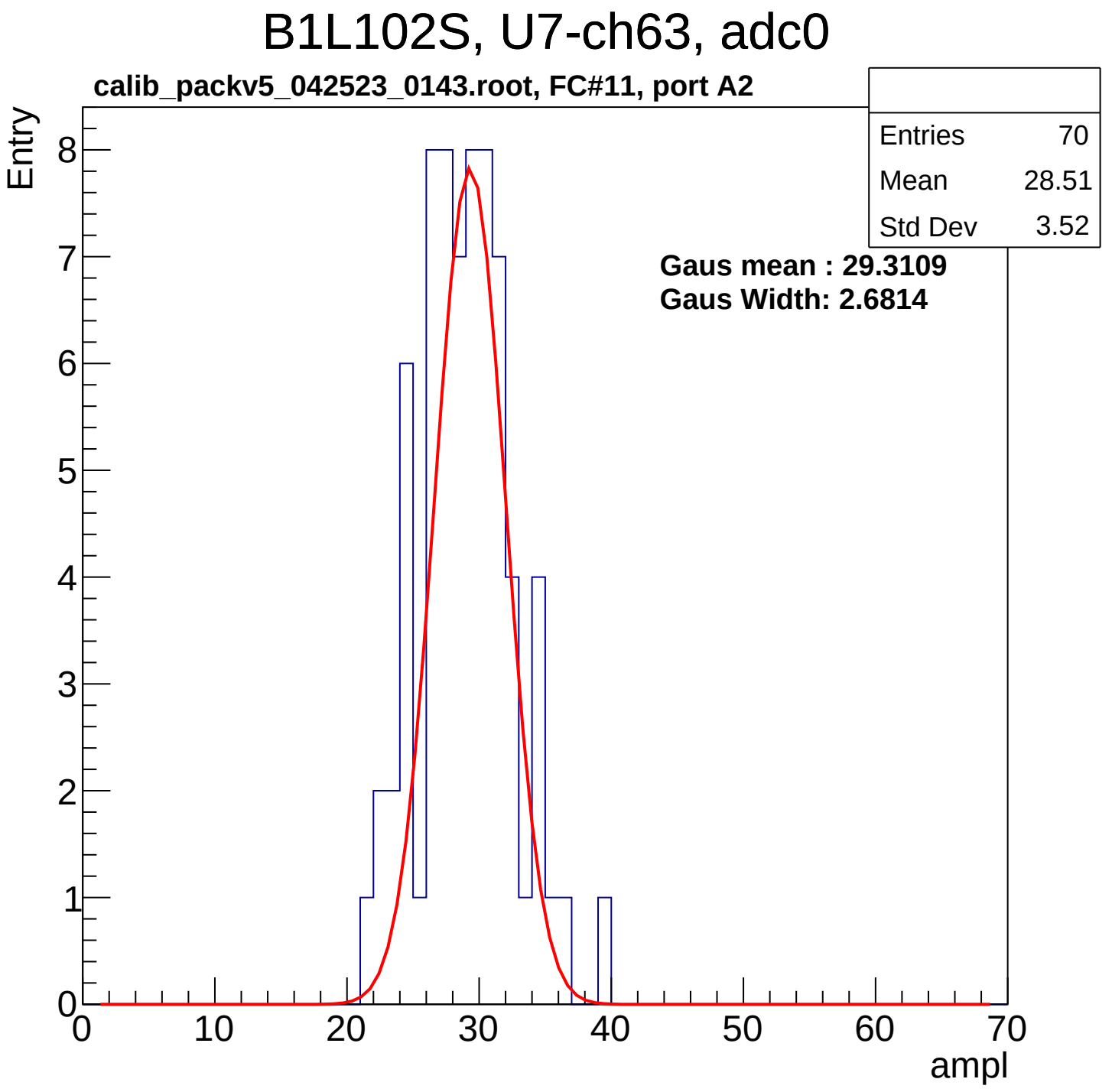
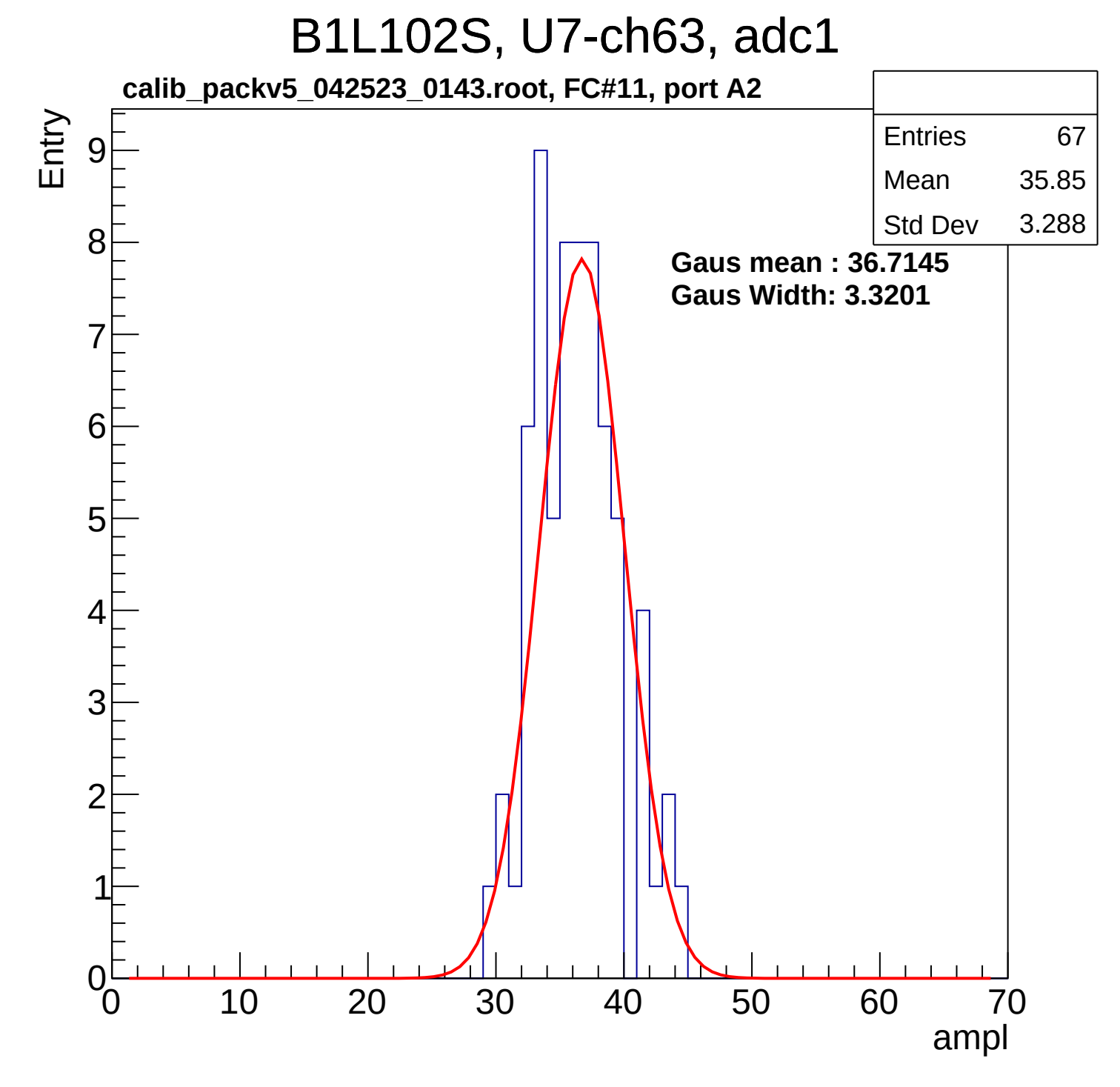
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U7-ch63, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 70
Mean 28.51
Std Dev 3.52
Gaus mean : 29.3109
Gaus Width: 2.6814
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L102S, U7-ch63, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 67
Mean 35.85
Std Dev 3.288
Gaus mean : 36.7145
Gaus Width: 3.3201
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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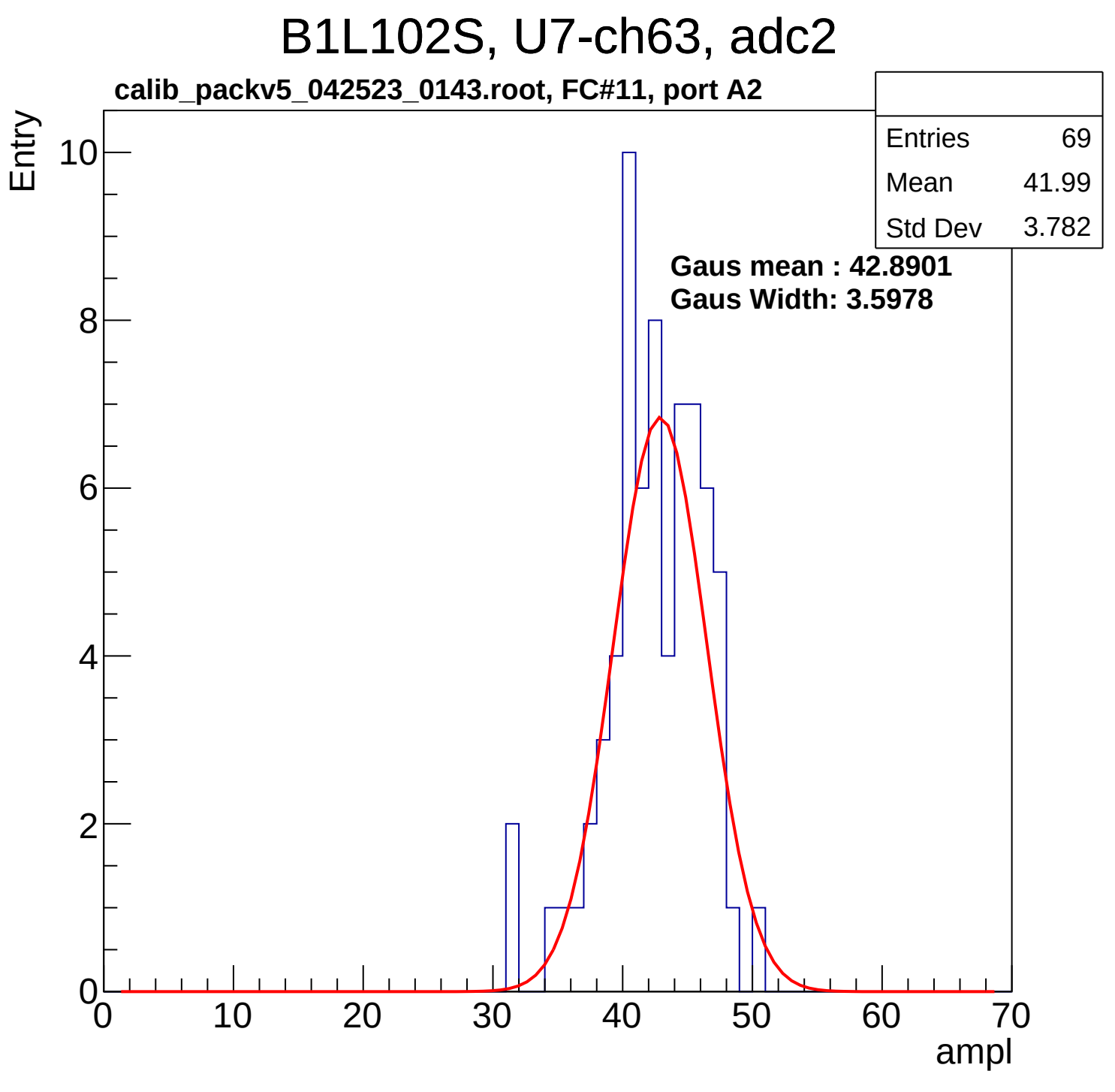
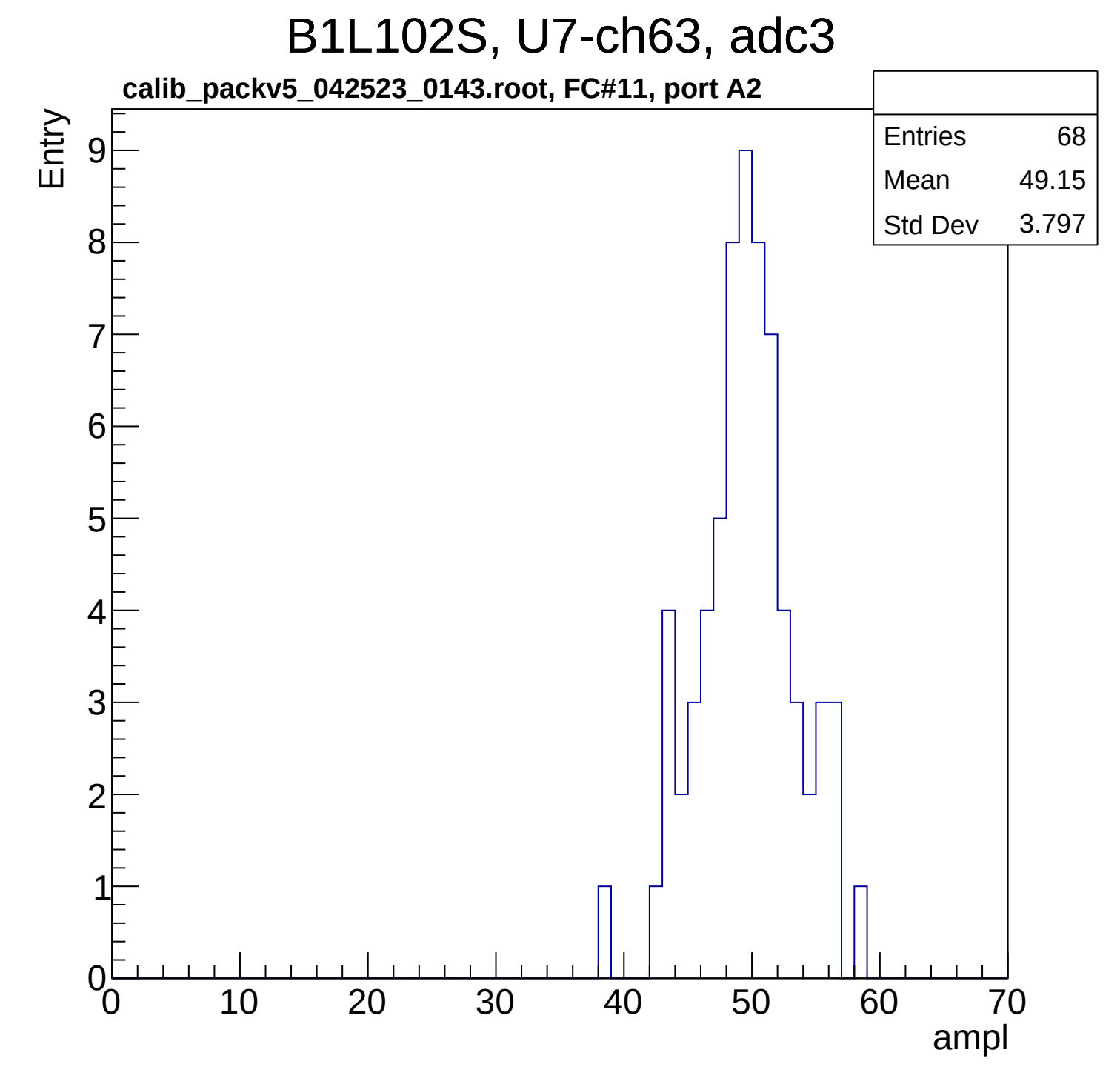
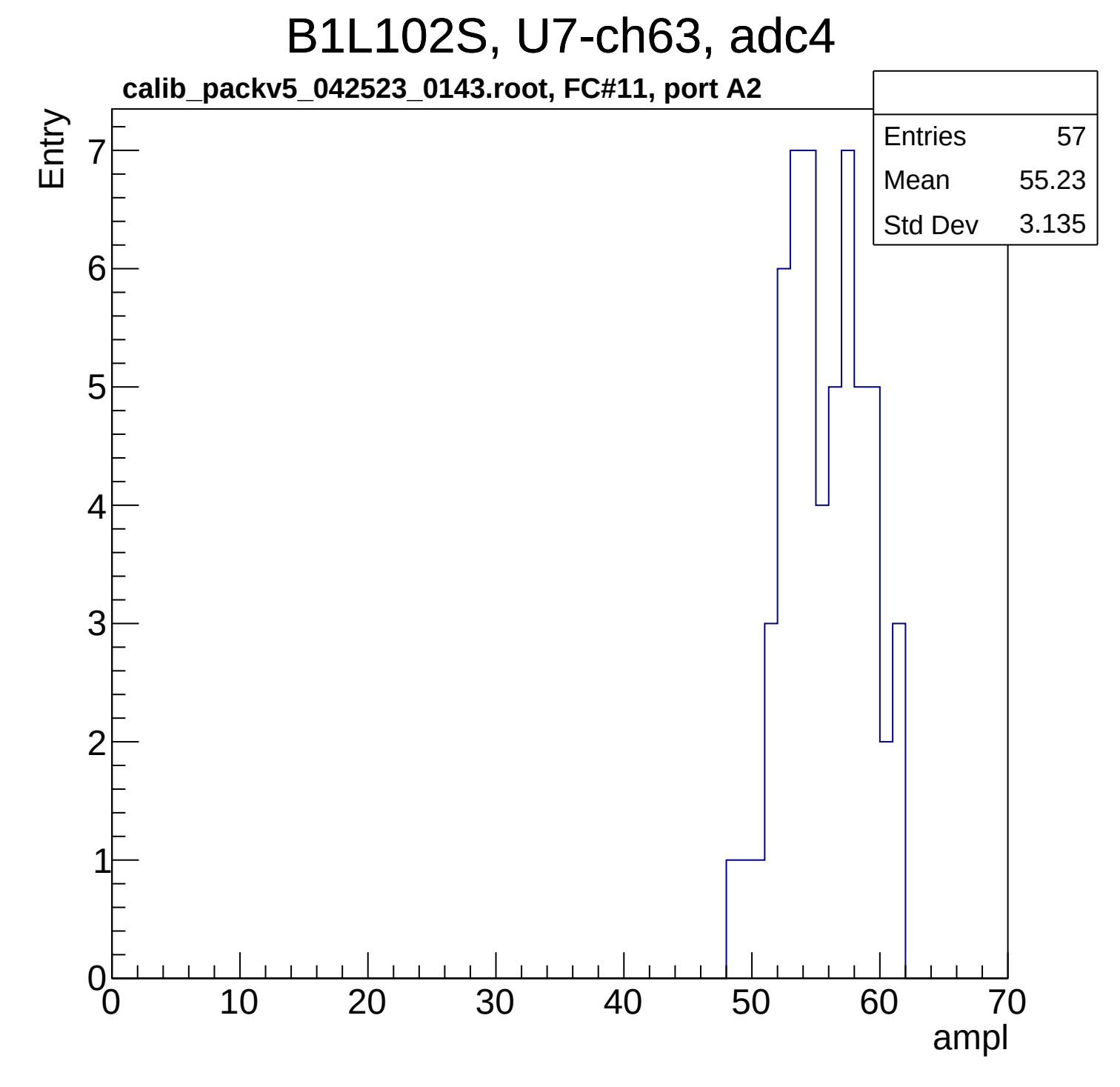
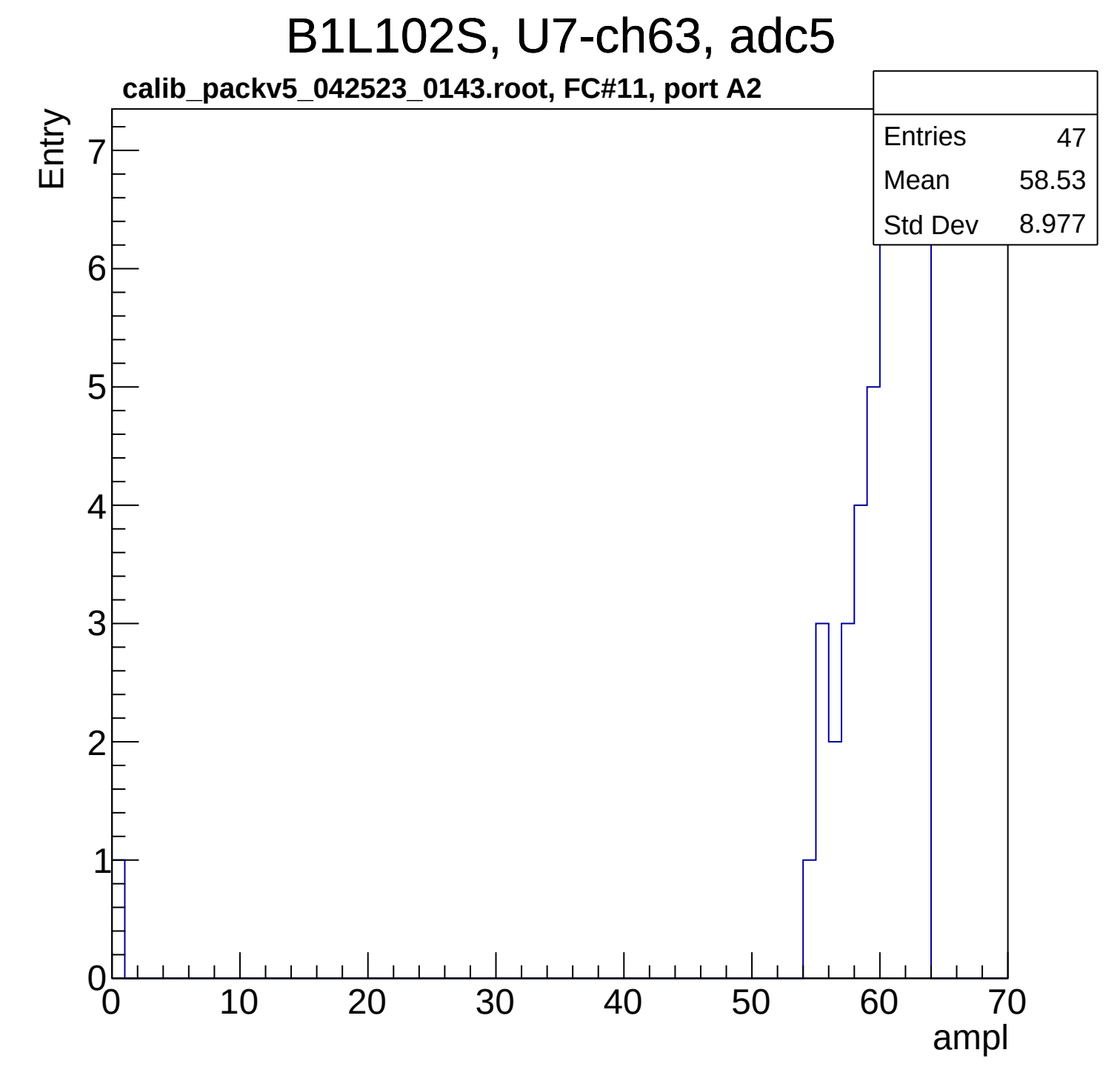
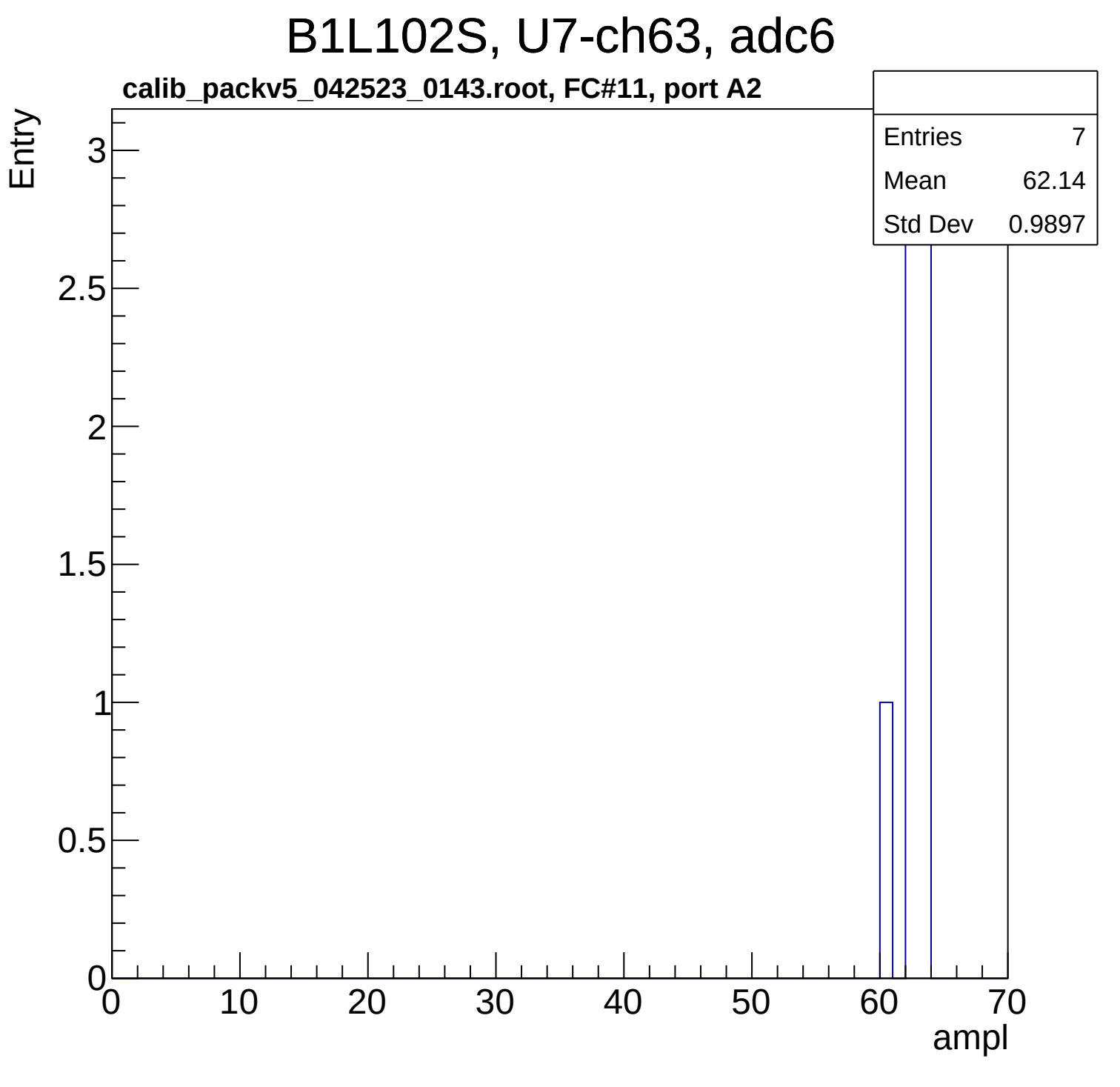

B1L102S, U7-ch63, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 69
Mean 41.99
Std Dev 3.782
Gaus mean : 42.8901
Gaus Width: 3.5978
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L102S, U7-ch63, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 68
Mean 49.15
Std Dev 3.797
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L102S, U7-ch63, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 57
Mean 55.23
Std Dev 3.135
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L102S, U7-ch63, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 47
Mean 58.53
Std Dev 8.977
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L102S, U7-ch63, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 7
Mean 62.14
Std Dev 0.9897
Entry
ampl
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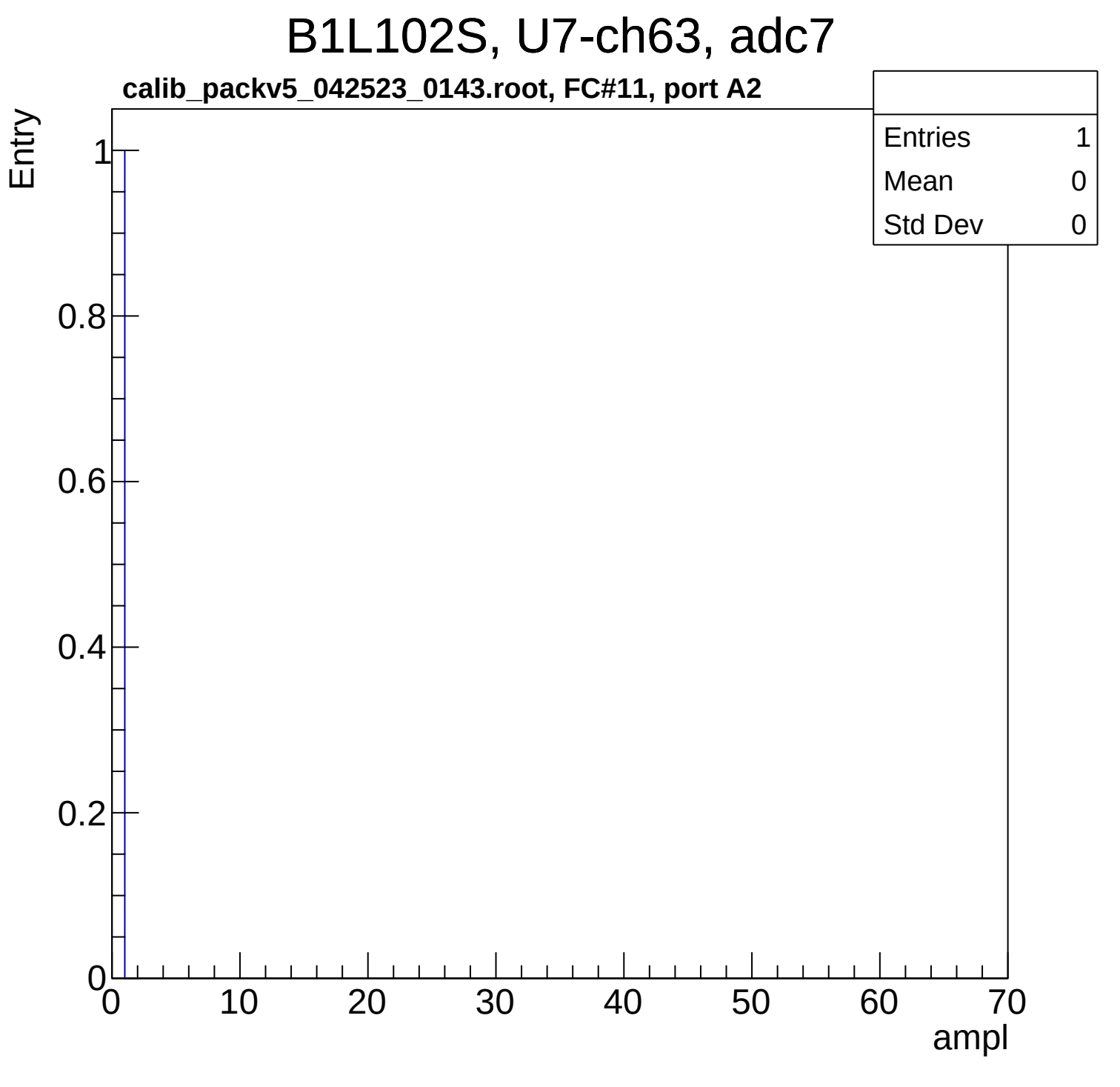
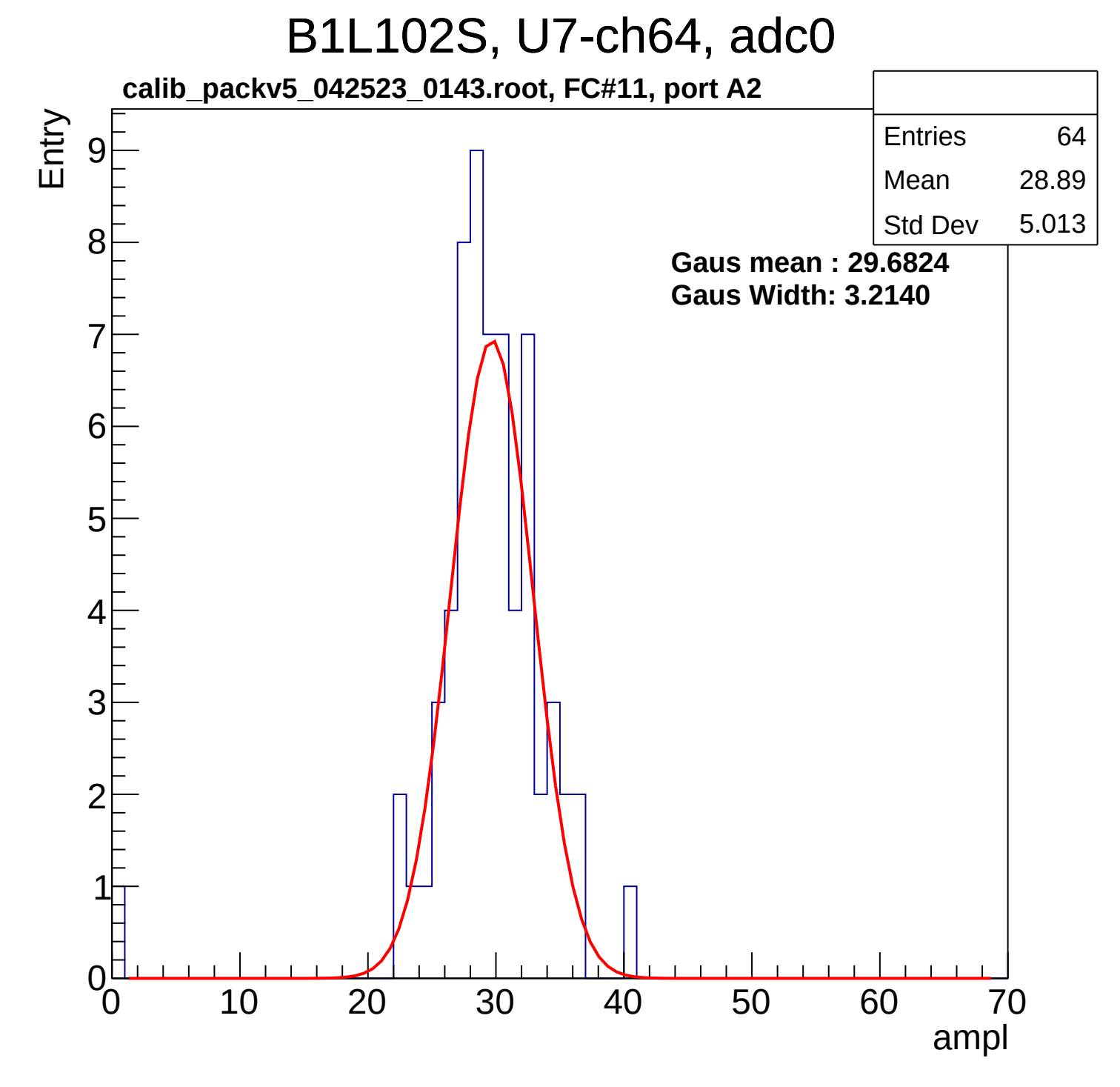
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L102S, U7-ch63, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U7-ch64, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 64
Mean 28.89
Std Dev 5.013
Gaus mean : 29.6824
Gaus Width: 3.2140
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
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20
30
40
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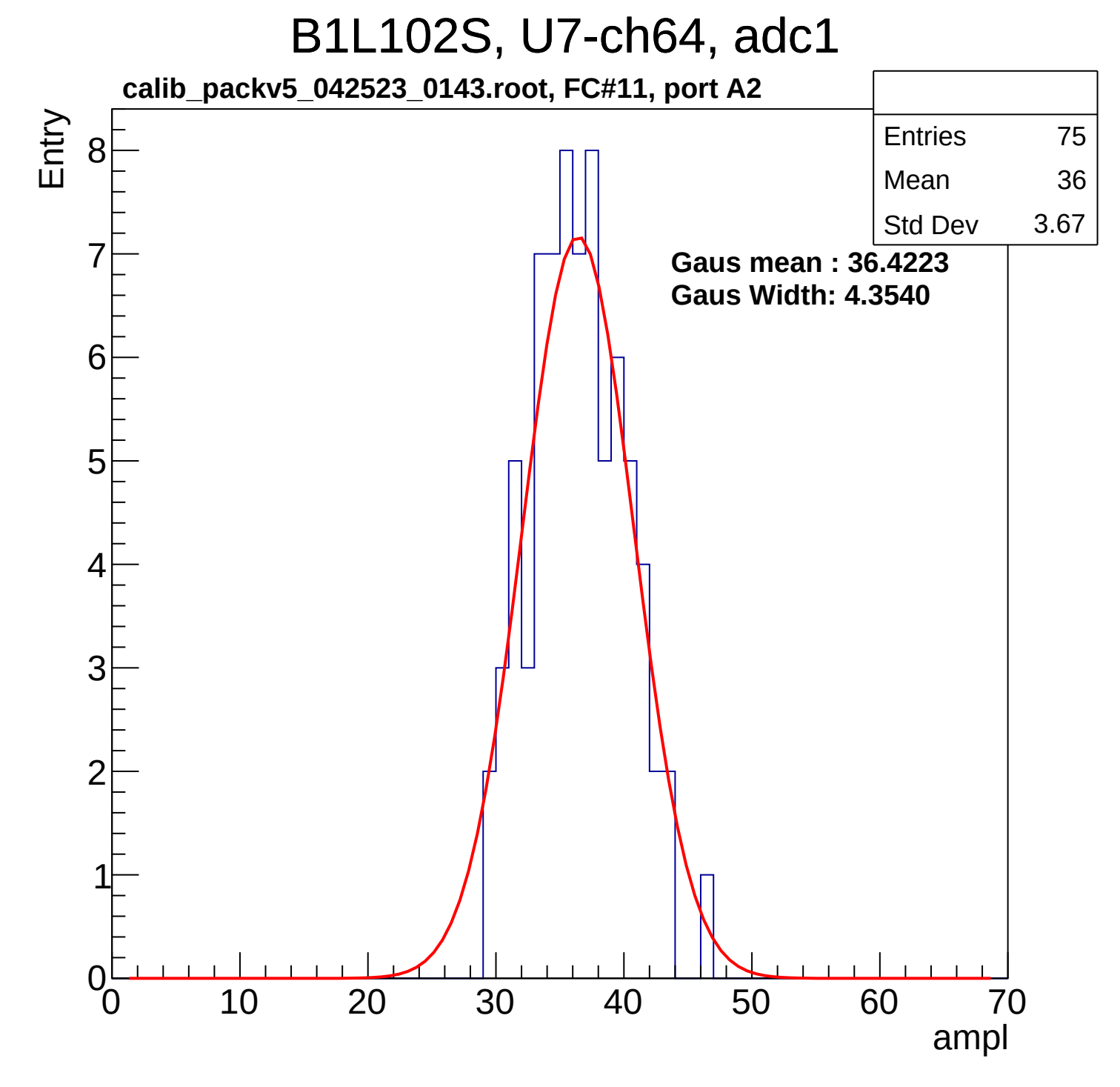
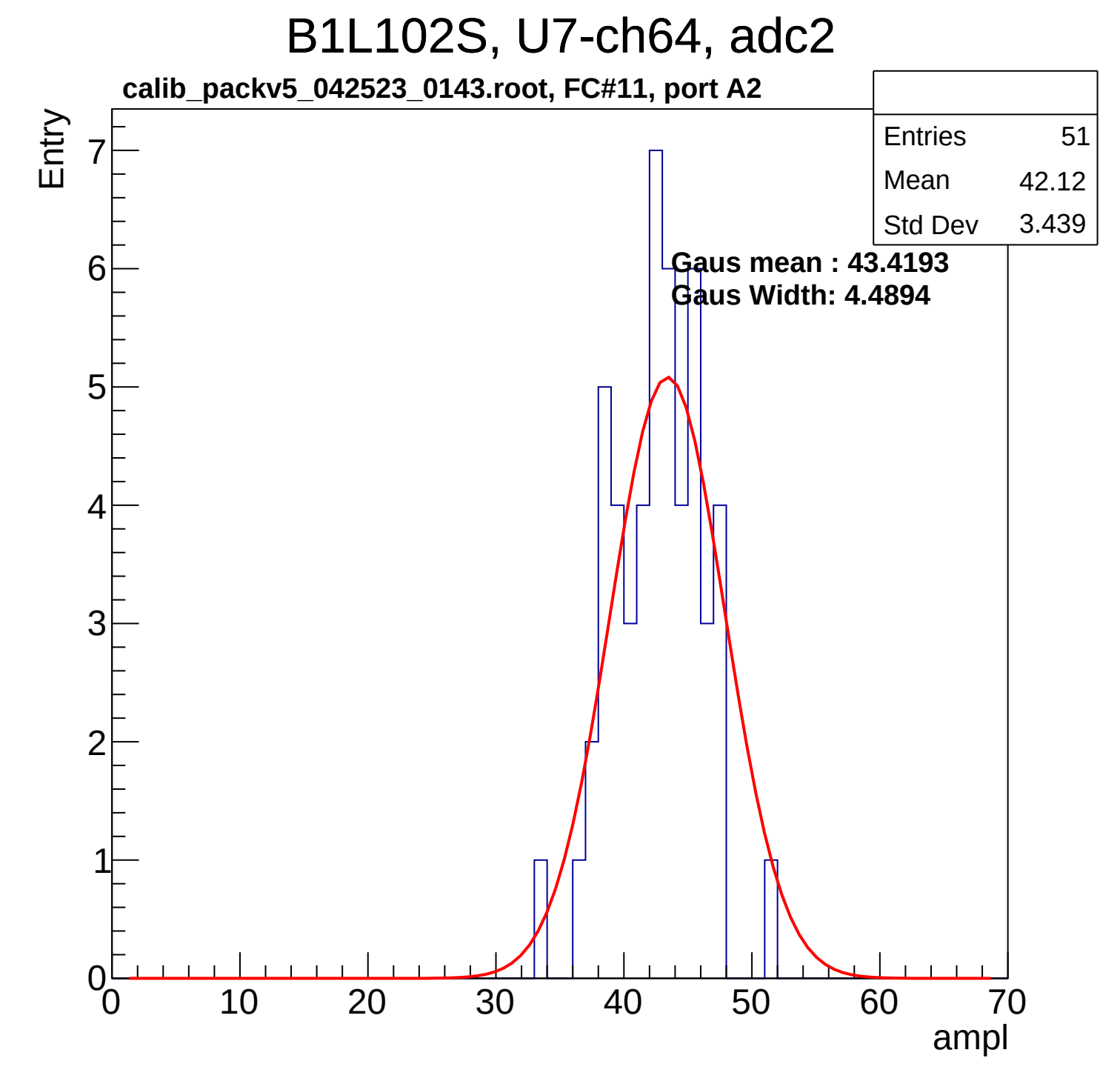
60
70


B1L102S, U7-ch64, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 75
Mean 36
Std Dev 3.67
Gaus mean : 36.4223
Gaus Width: 4.3540
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L102S, U7-ch64, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 51
Mean 42.12
Std Dev 3.439
Gaus mean : 43.4193
Gaus Width: 4.4894
Entry
ampl
0
1
2
3
4
5
6
7
0
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20
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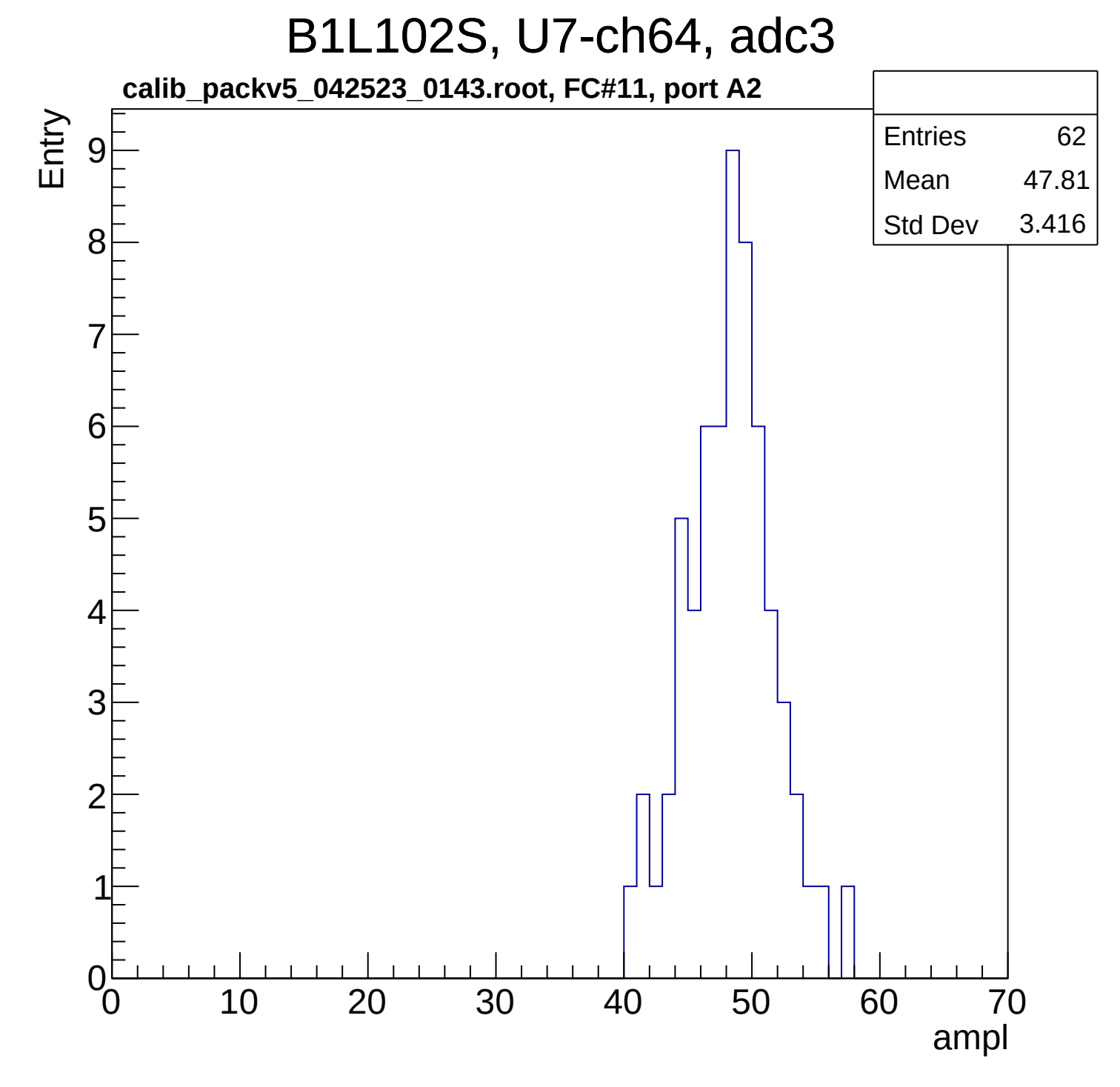
40
50
60
70


B1L102S, U7-ch64, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 62
Mean 47.81
Std Dev 3.416
Entry
ampl
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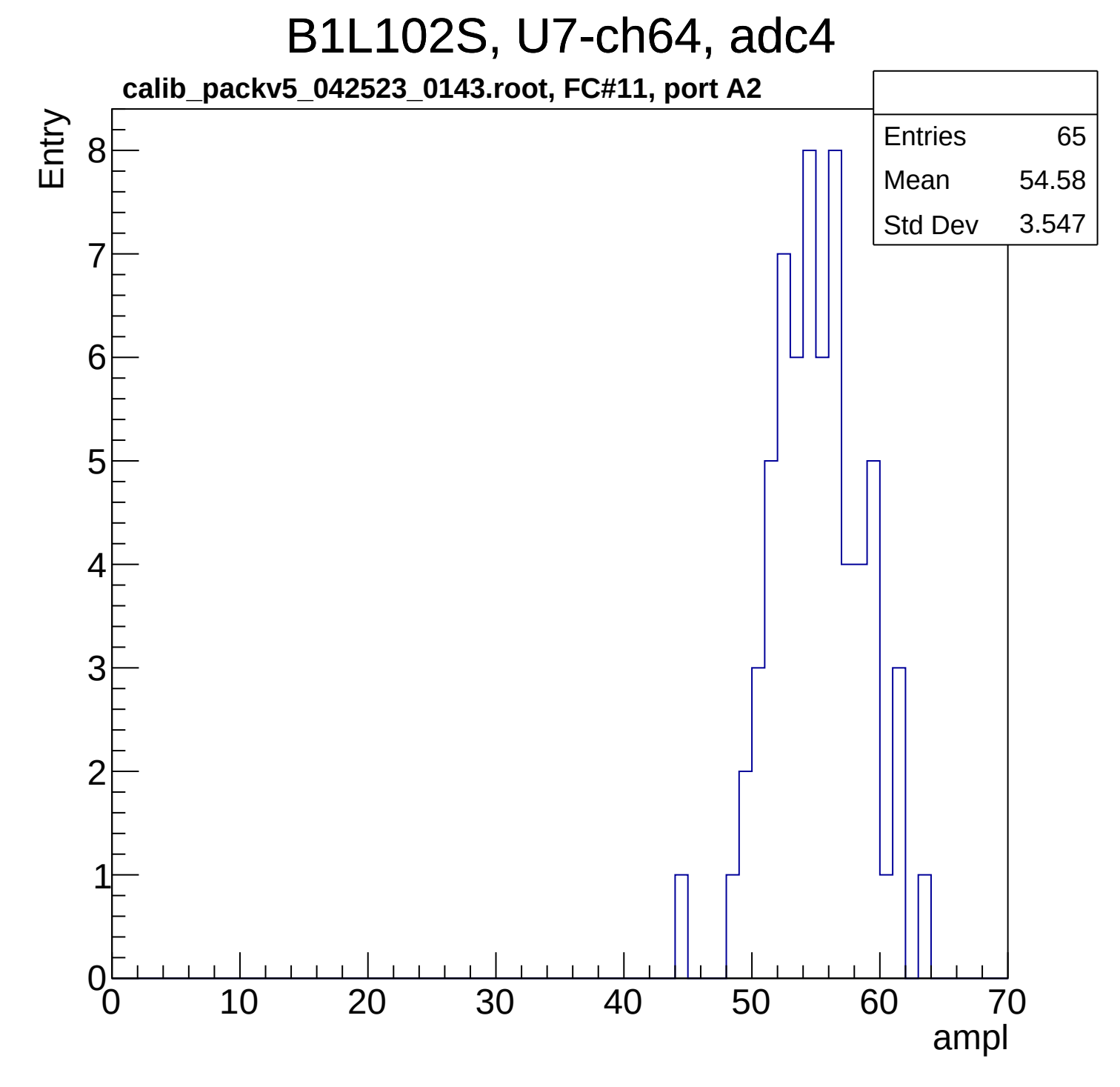
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L102S, U7-ch64, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 65
Mean 54.58
Std Dev 3.547
Entry
ampl
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2
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4
5
6
7
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0
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40
50
60
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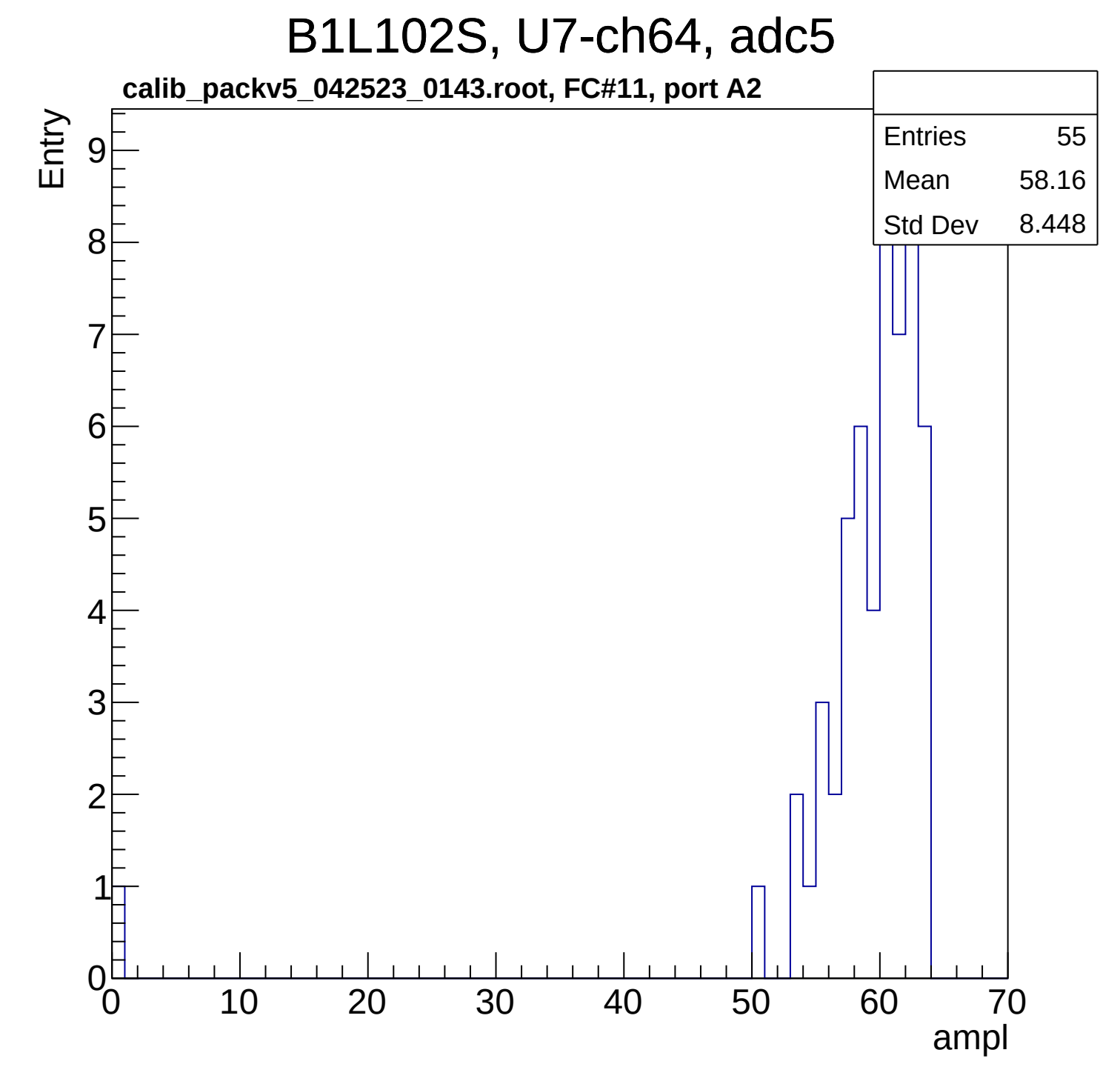
B1L102S, U7-ch64, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 55
Mean 58.16
Std Dev 8.448
Entry
ampl
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2
3
4
5
6
7
8
9
0
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40
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60
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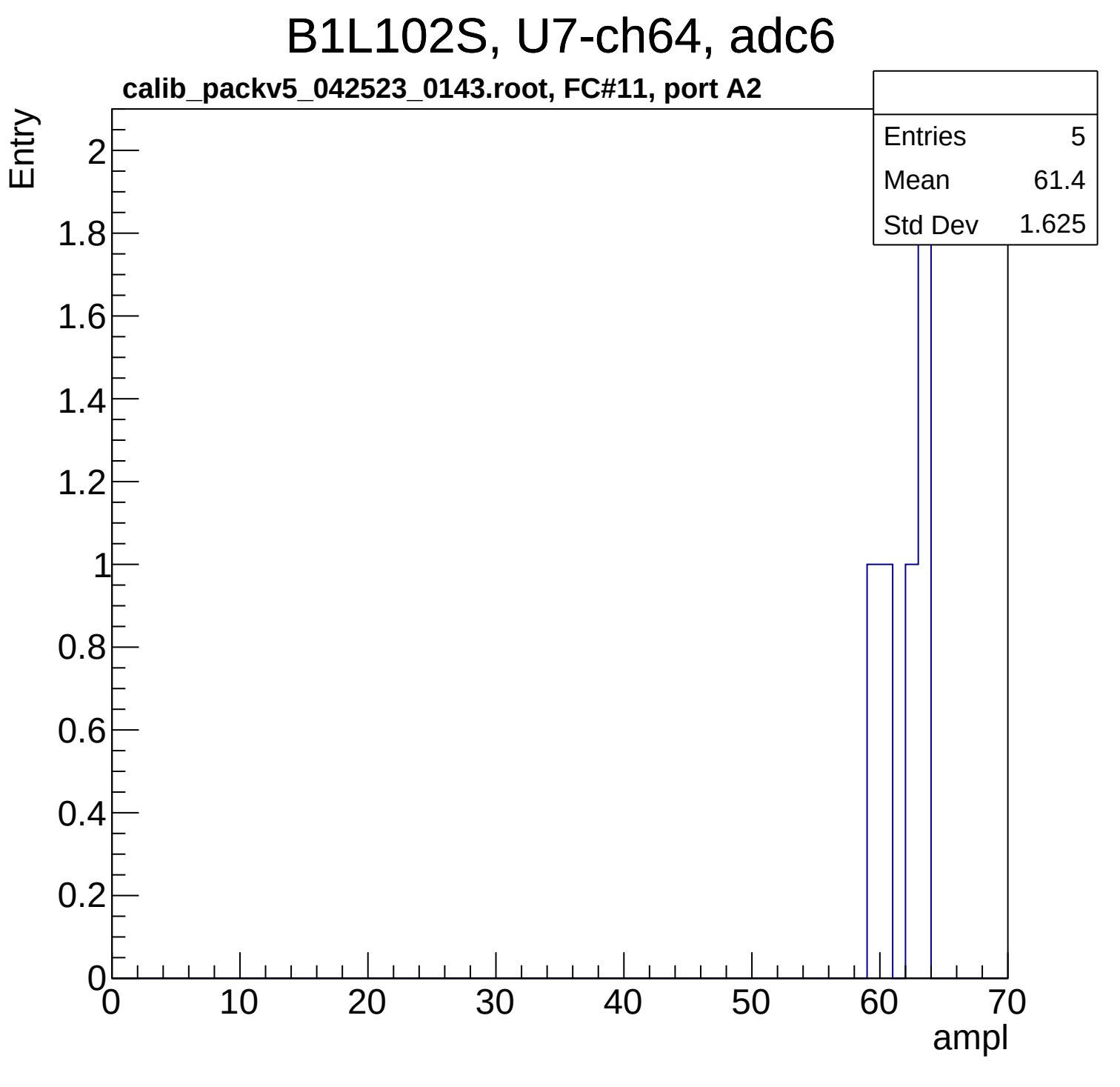
B1L102S, U7-ch64, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 5
Mean 61.4
Std Dev 1.625
Entry
ampl
0
0.2
0.4
0.6
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1
1.2
1.4
1.6
1.8
2
0
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20
30
40
50
60
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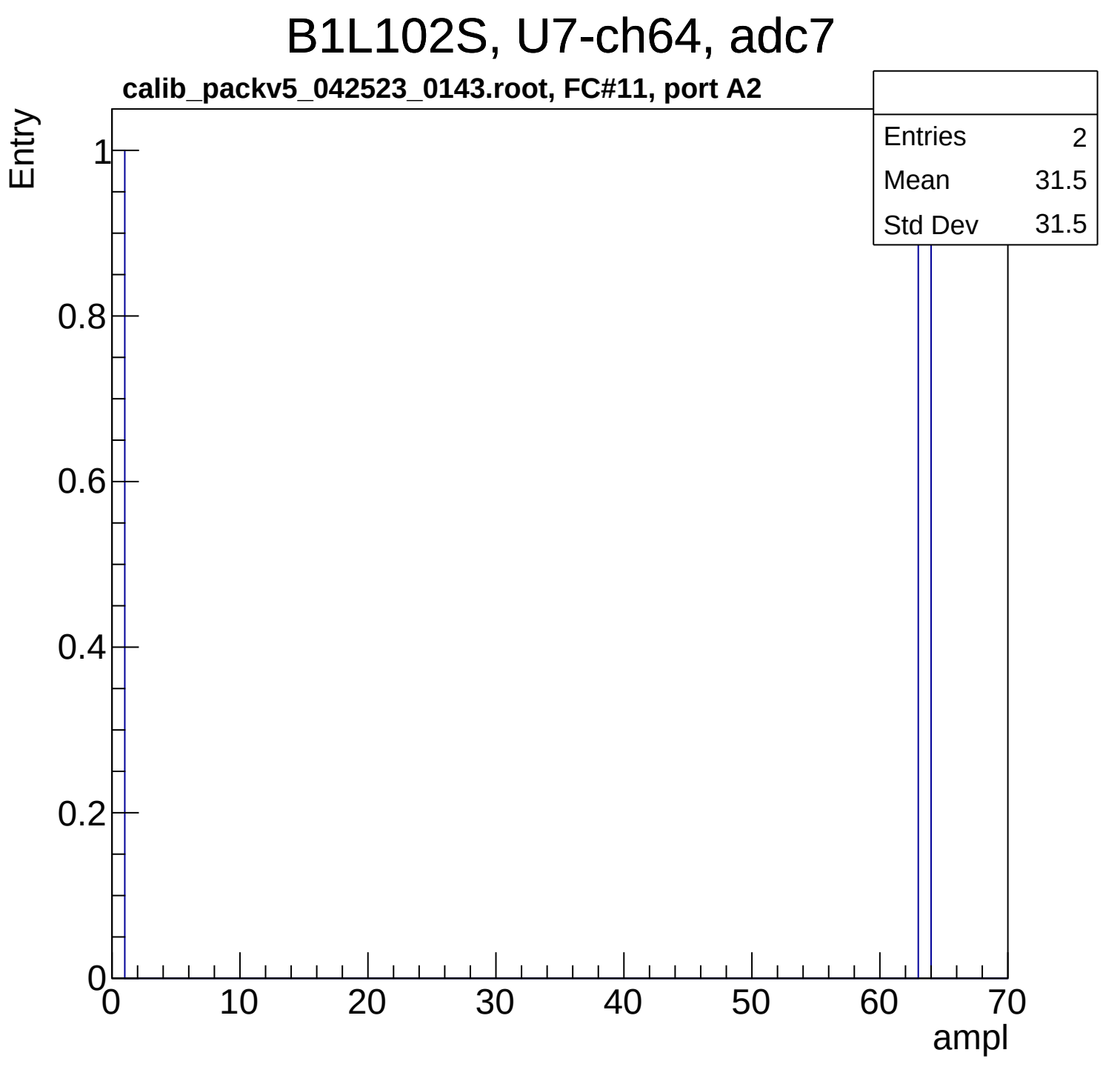
B1L102S, U7-ch64, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 2
Mean 31.5
Std Dev 31.5
Entry
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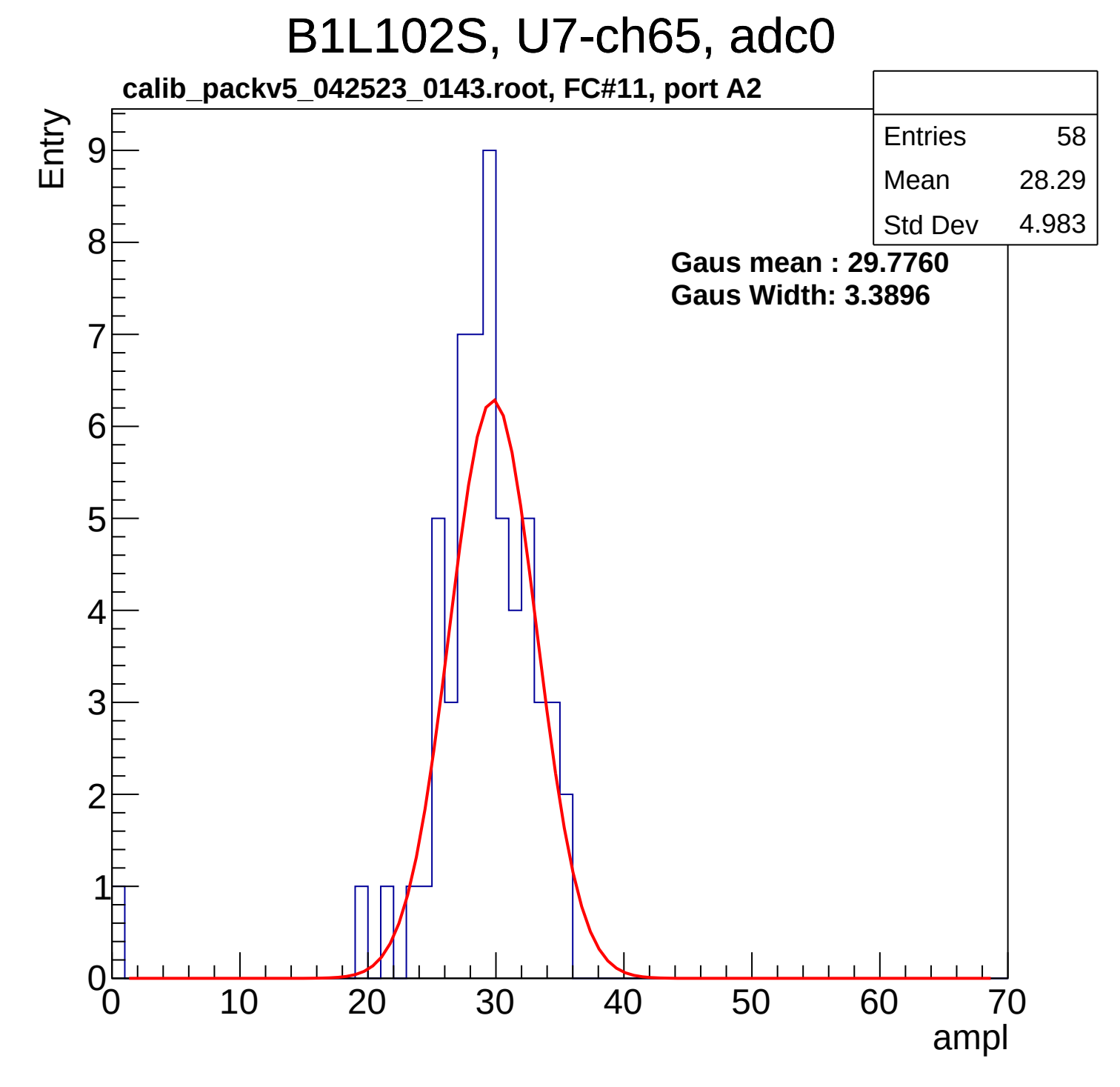
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U7-ch65, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 58
Mean 28.29
Std Dev 4.983
Gaus mean : 29.7760
Gaus Width: 3.3896
Entry
ampl
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2
3
4
5
6
7
8
9
0
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40
50
60
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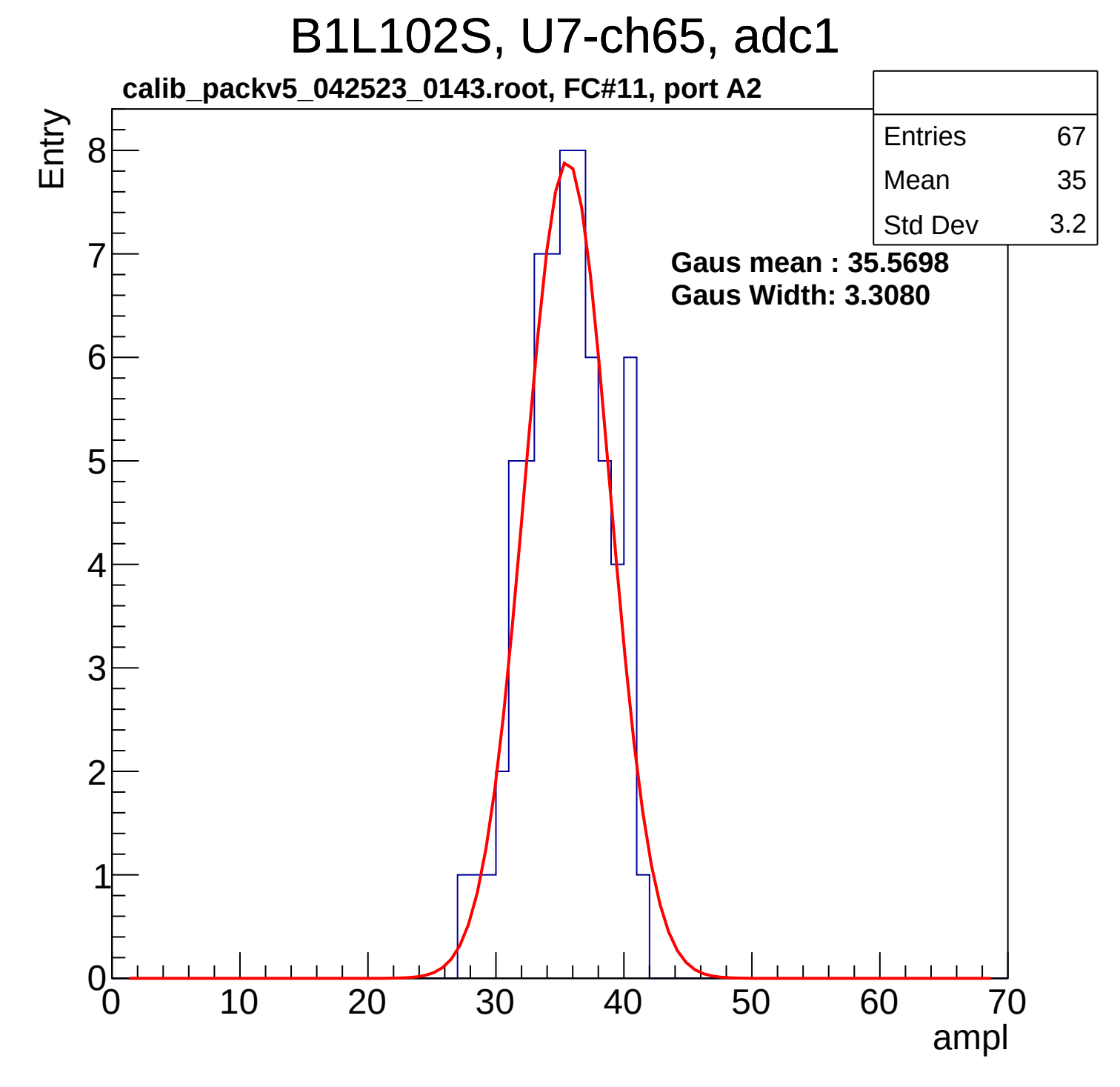
B1L102S, U7-ch65, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 67
Mean 35
Std Dev 3.2
Gaus mean : 35.5698
Gaus Width: 3.3080
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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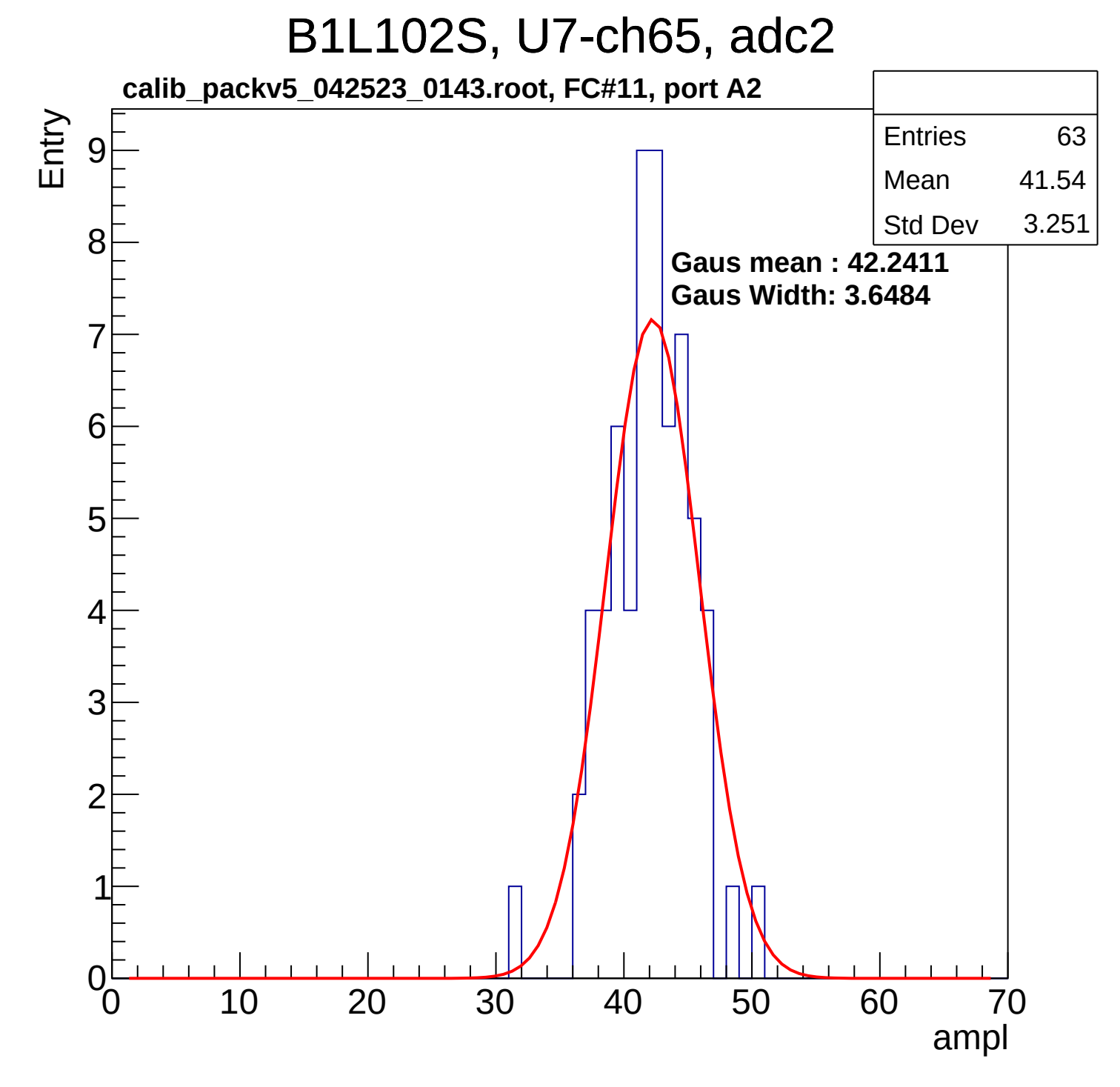
B1L102S, U7-ch65, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 63
Mean 41.54
Std Dev 3.251
Gaus mean : 42.2411
Gaus Width: 3.6484
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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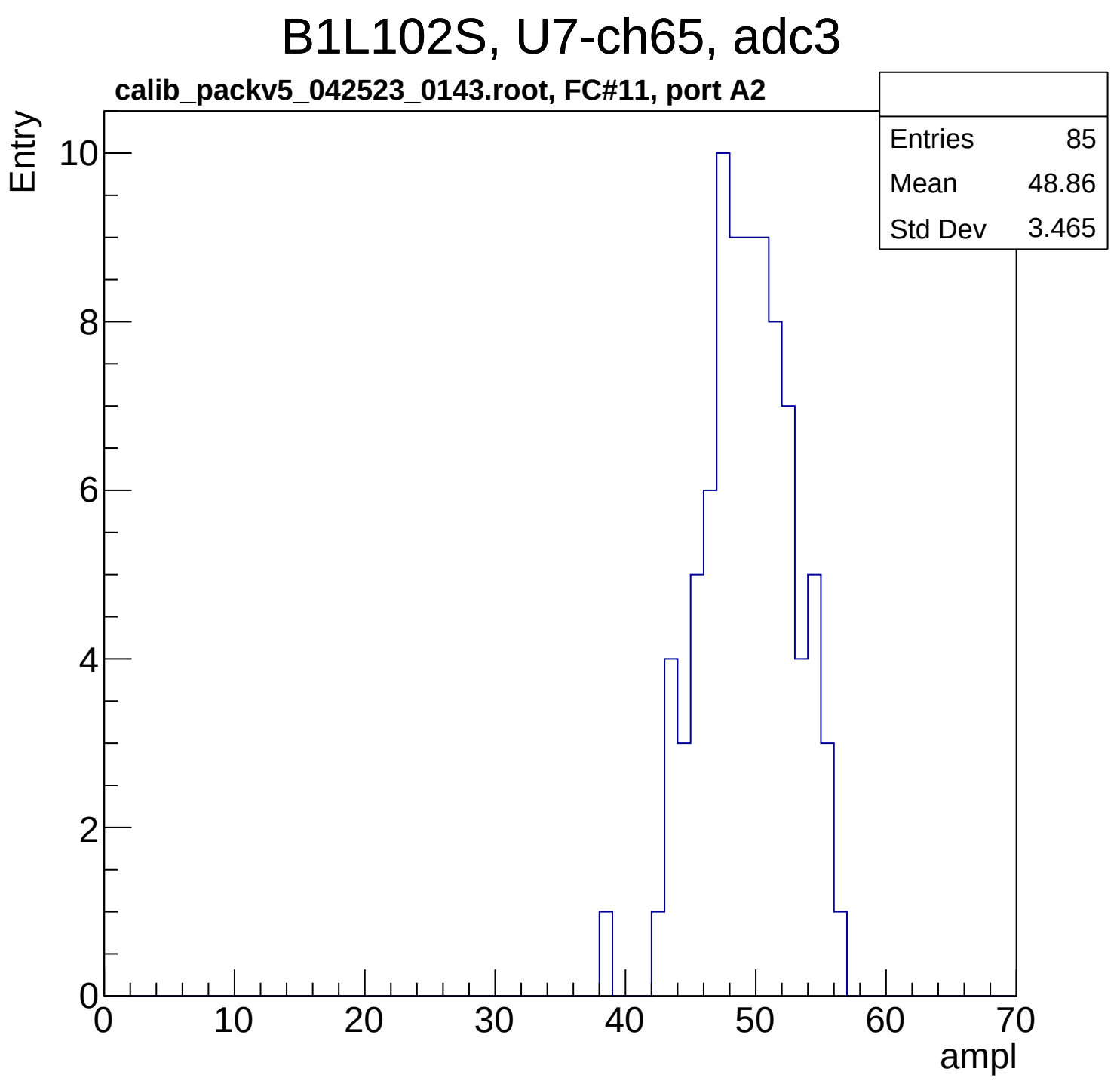
B1L102S, U7-ch65, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 85
Mean 48.86
Std Dev 3.465
Entry
ampl
0
2
4
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8
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0
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60
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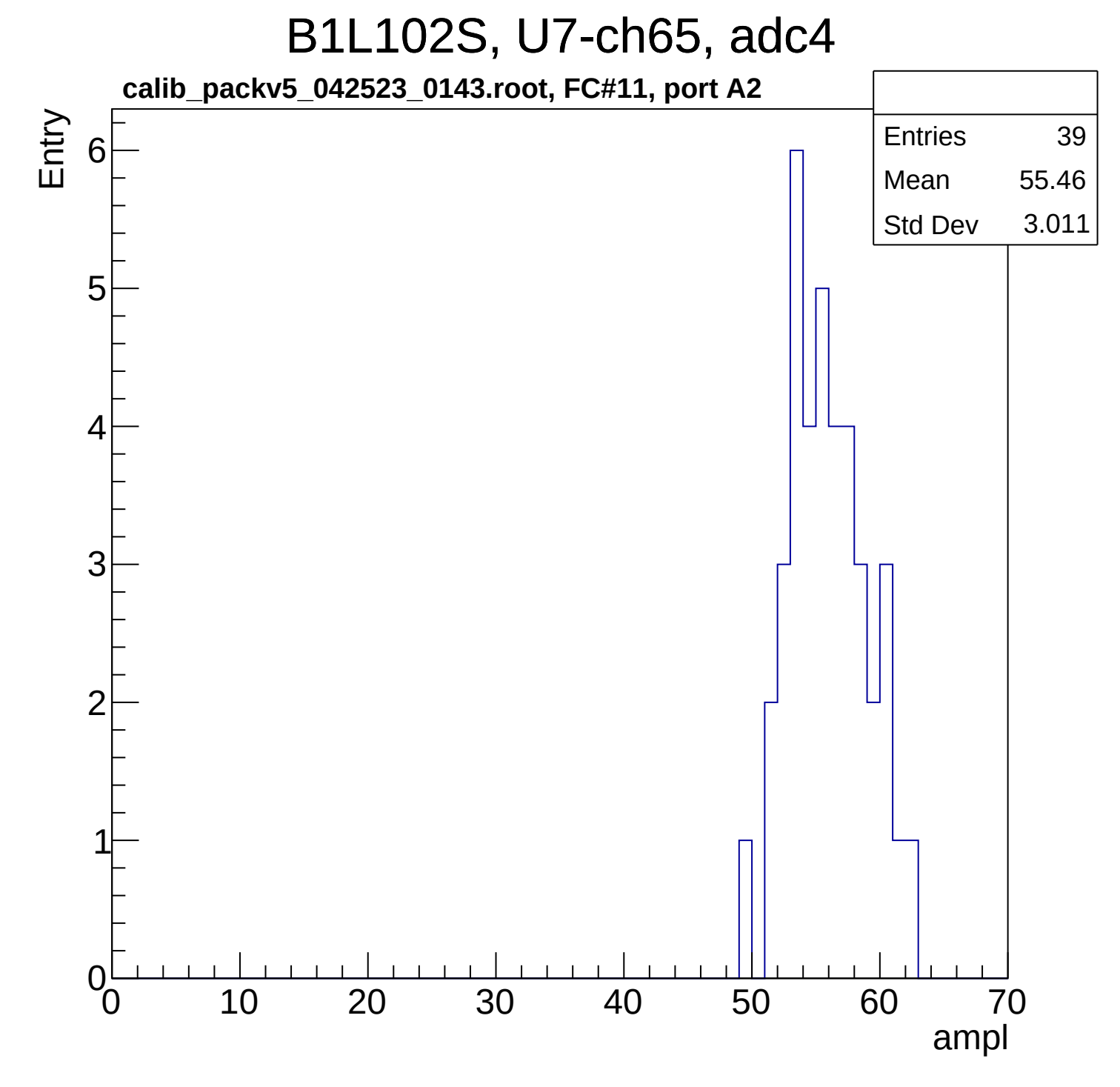
B1L102S, U7-ch65, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 39
Mean 55.46
Std Dev 3.011
Entry
ampl
0
1
2
3
4
5
6
0
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20
30
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60
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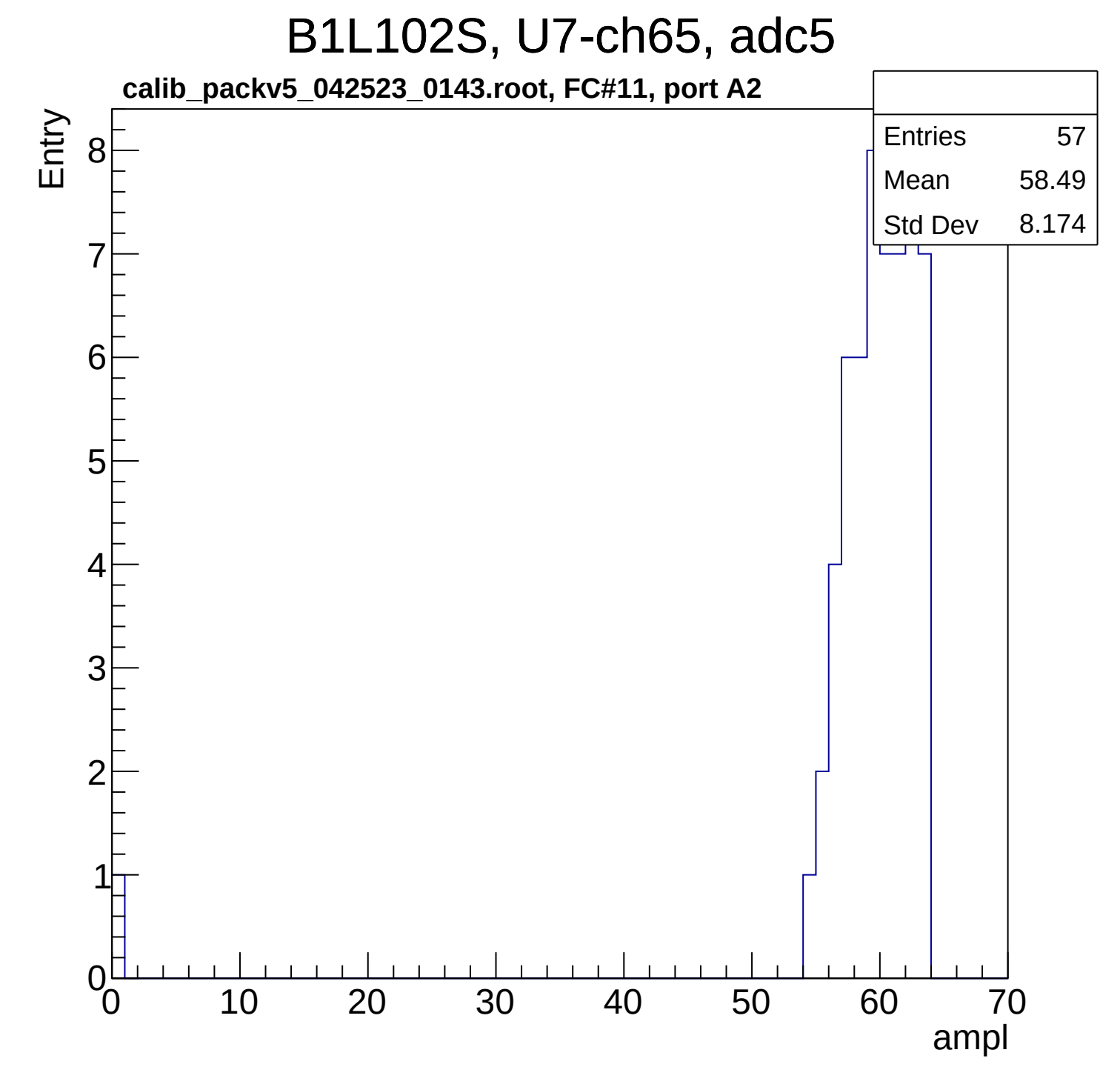
B1L102S, U7-ch65, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 57
Mean 58.49
Std Dev 8.174
Entry
ampl
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1
2
3
4
5
6
7
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0
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60
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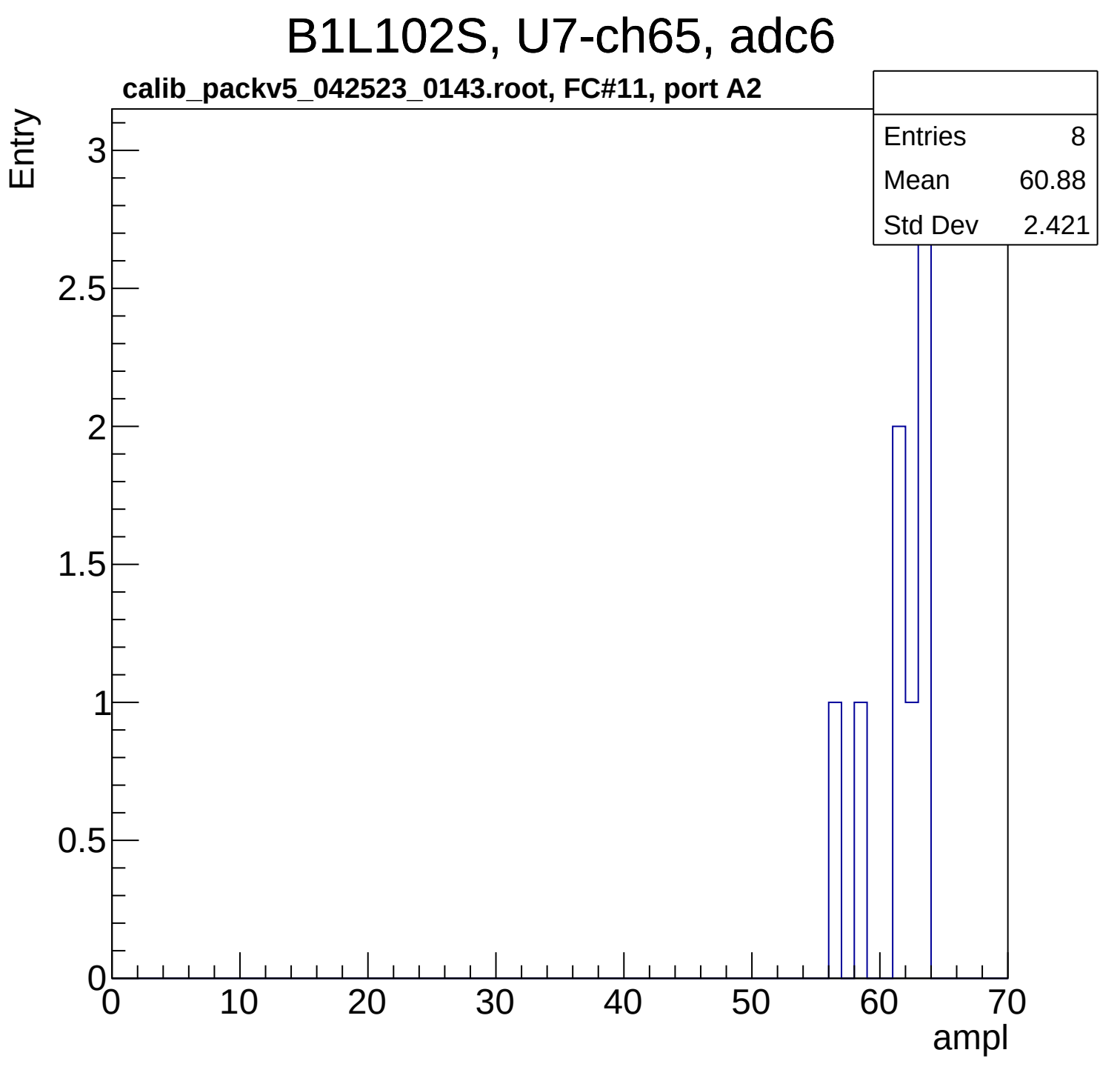
B1L102S, U7-ch65, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 8
Mean 60.88
Std Dev 2.421
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
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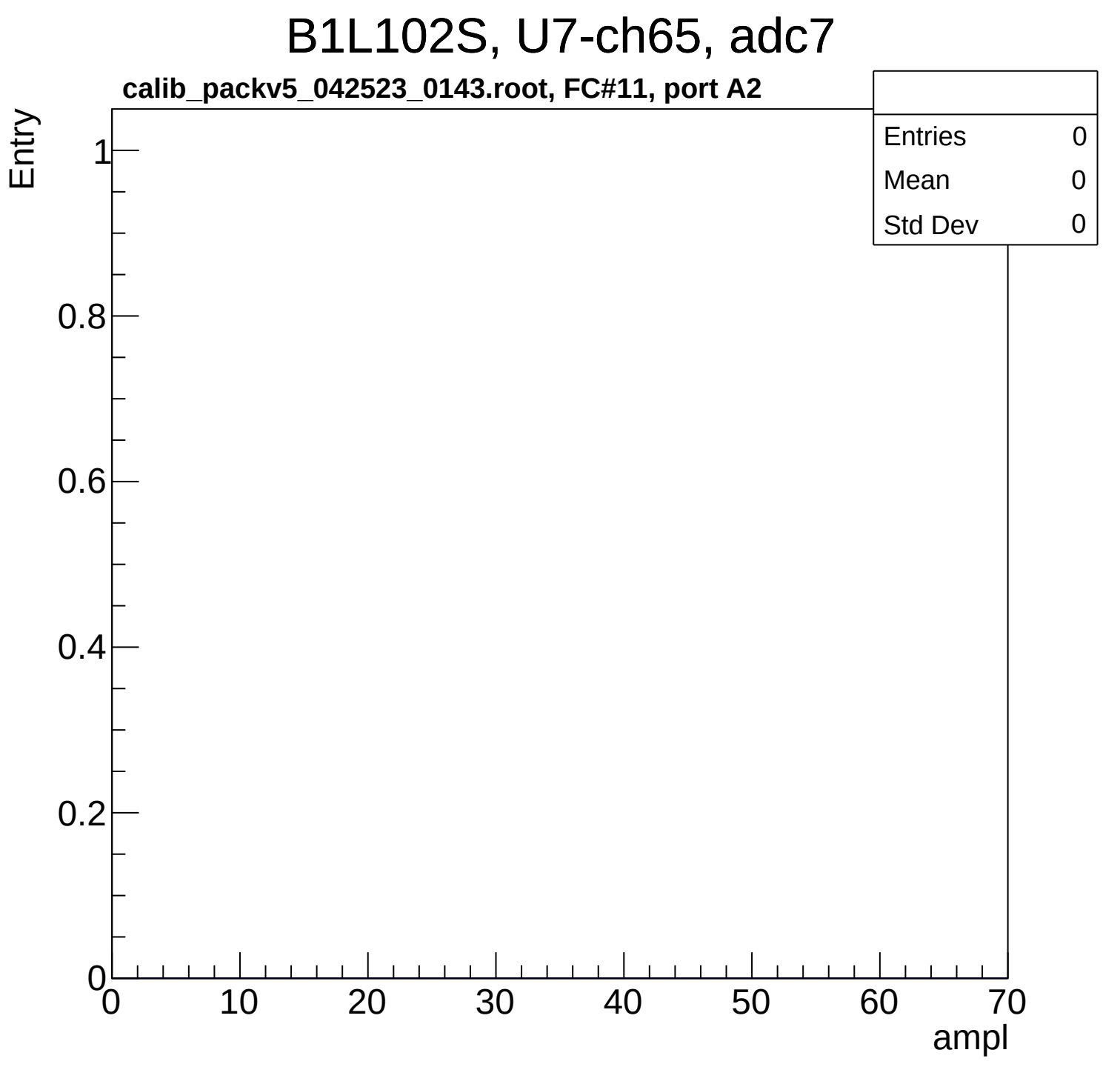
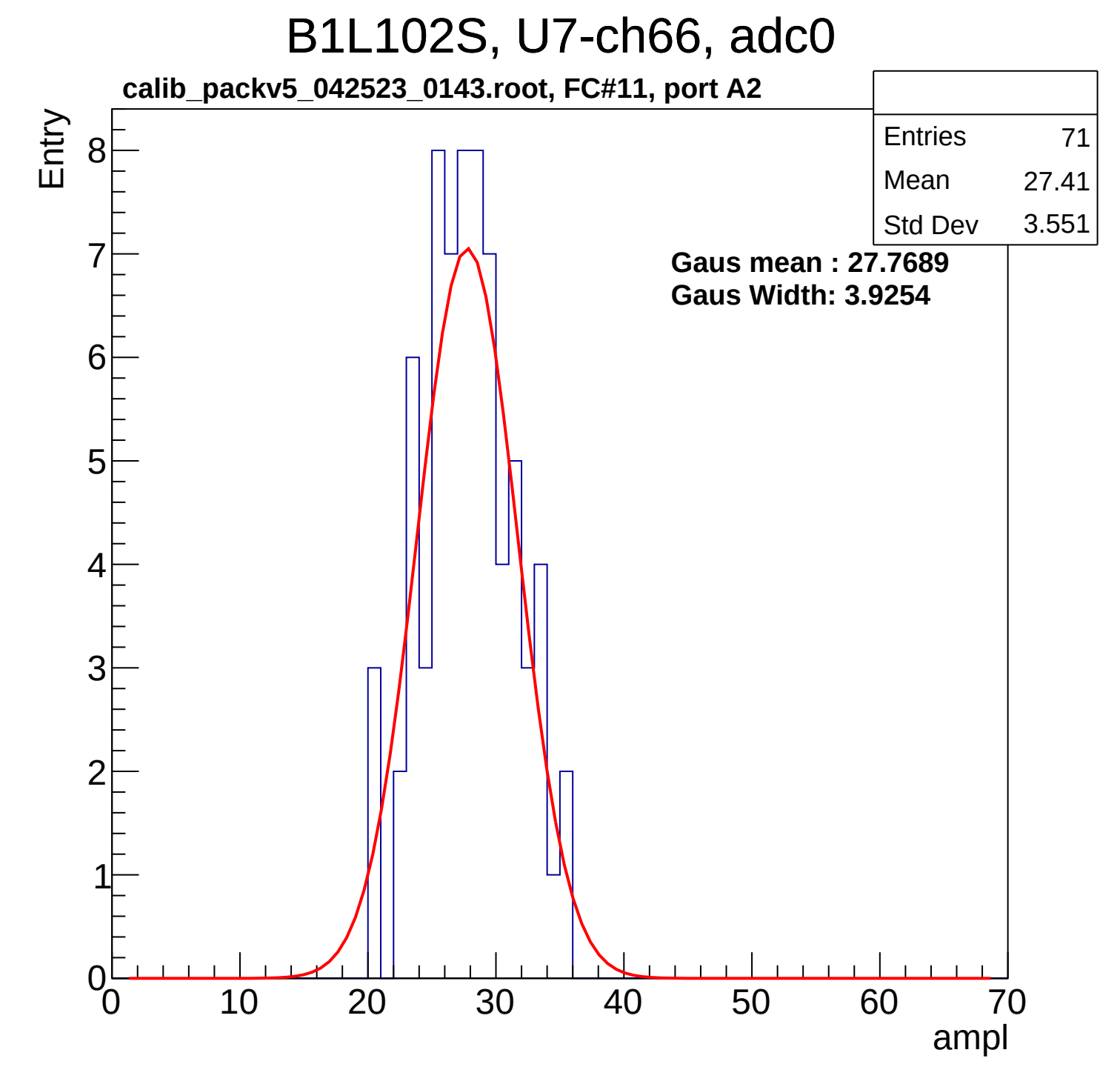

B1L102S, U7-ch65, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U7-ch66, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 71
Mean 27.41
Std Dev 3.551
Gaus mean : 27.7689
Gaus Width: 3.9254
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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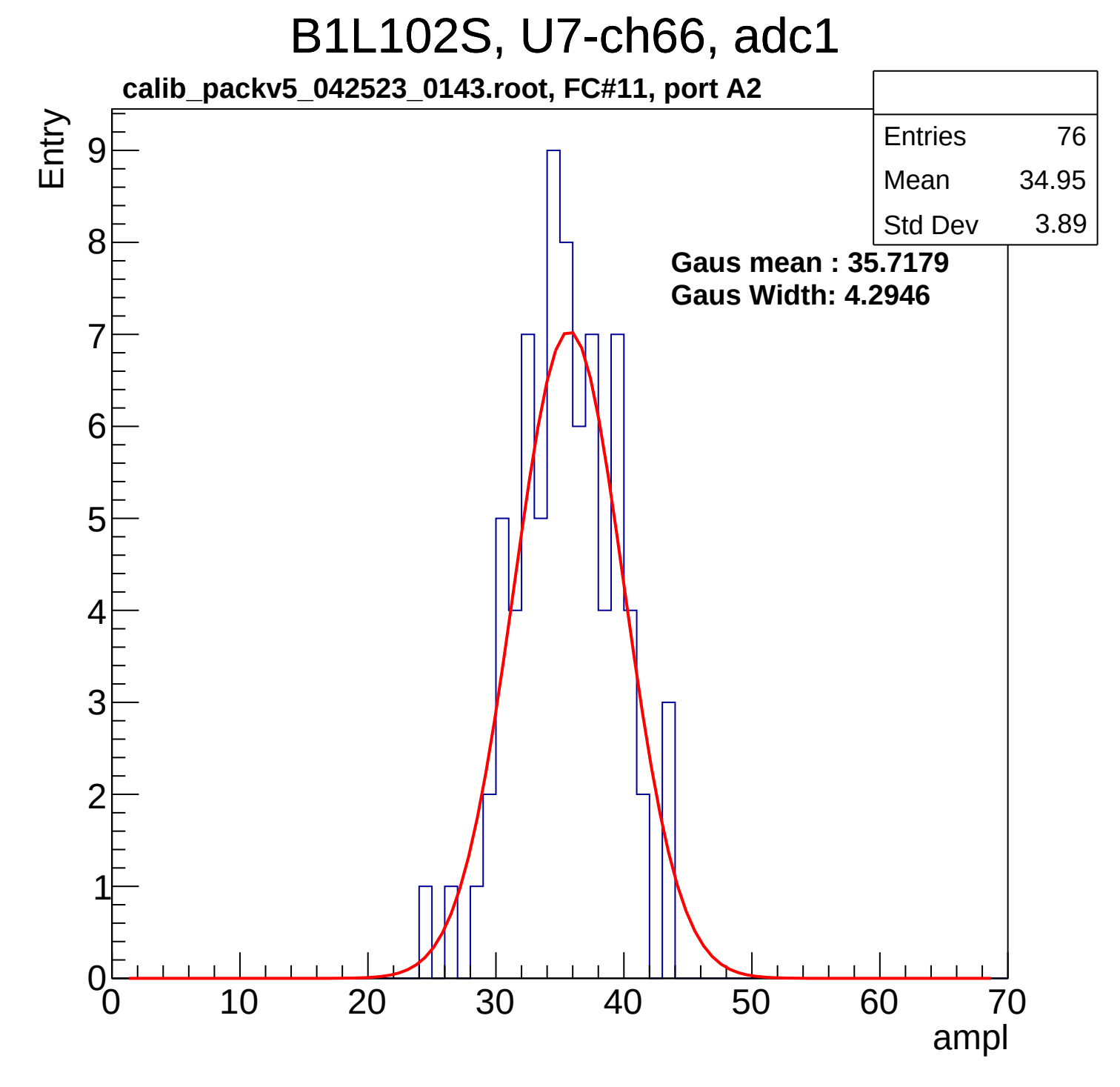
B1L102S, U7-ch66, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 76
Mean 34.95
Std Dev 3.89
Gaus mean : 35.7179
Gaus Width: 4.2946
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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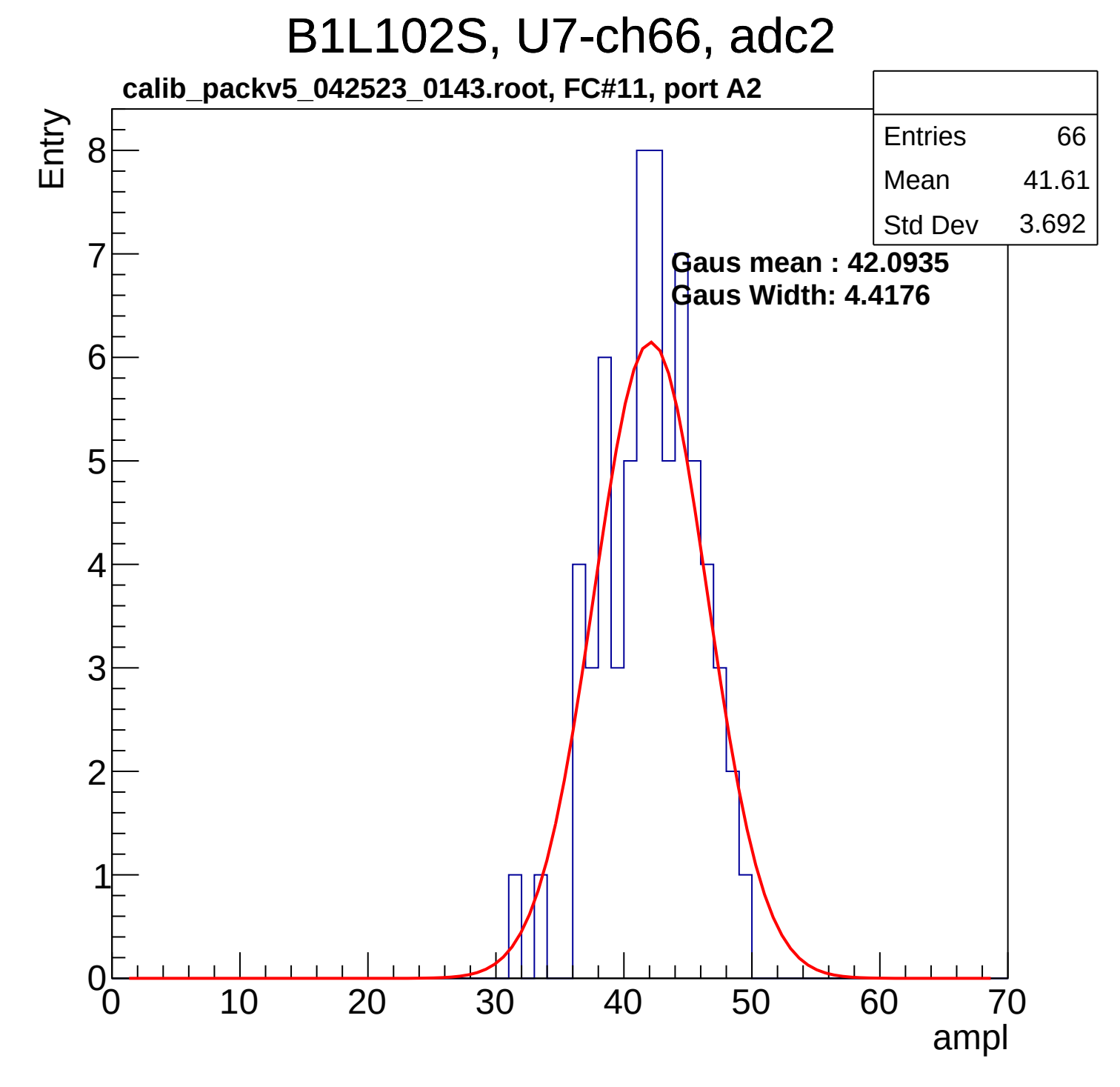
B1L102S, U7-ch66, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 66
Mean 41.61
Std Dev 3.692
Gaus mean : 42.0935
Gaus Width: 4.4176
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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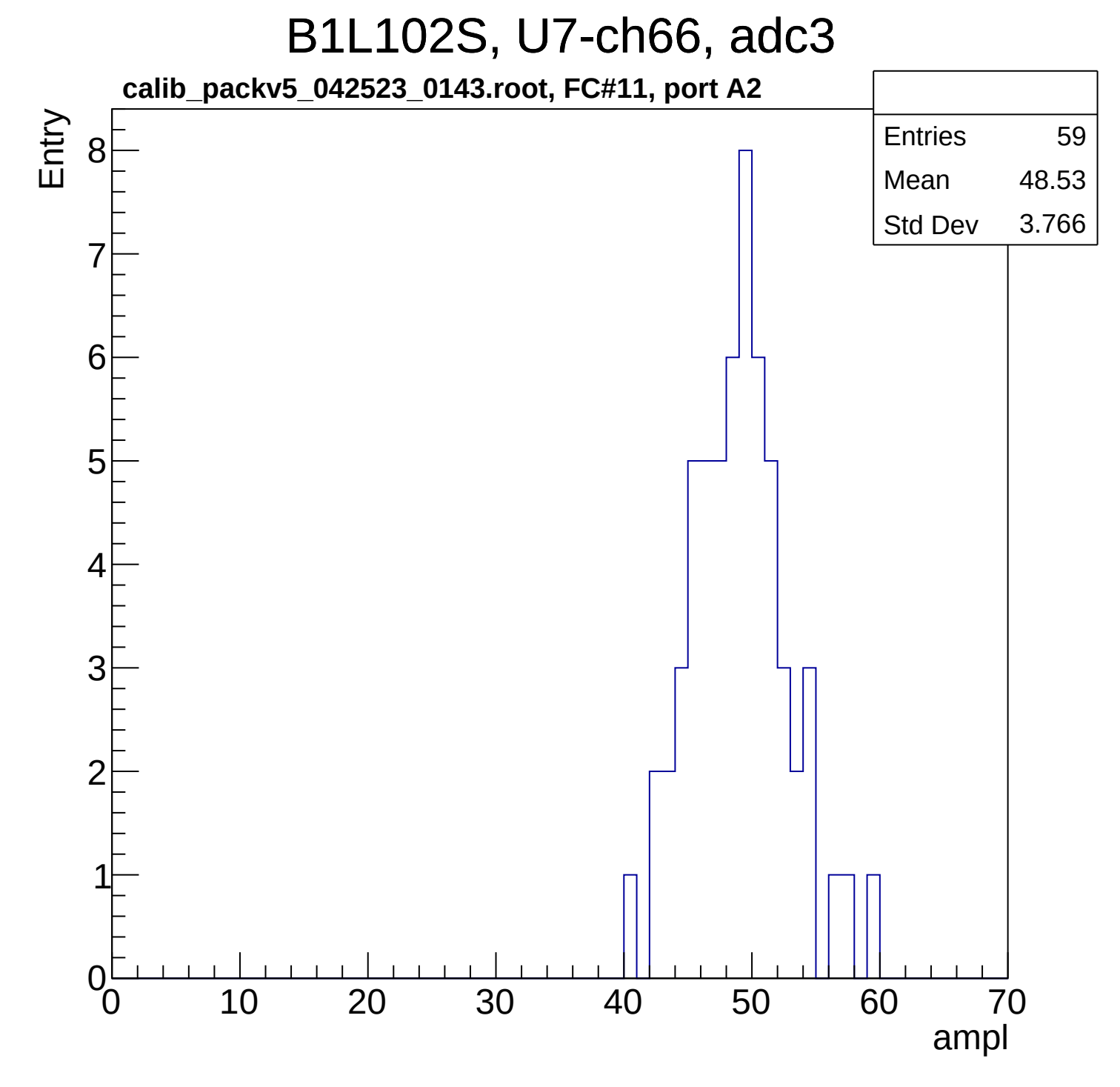
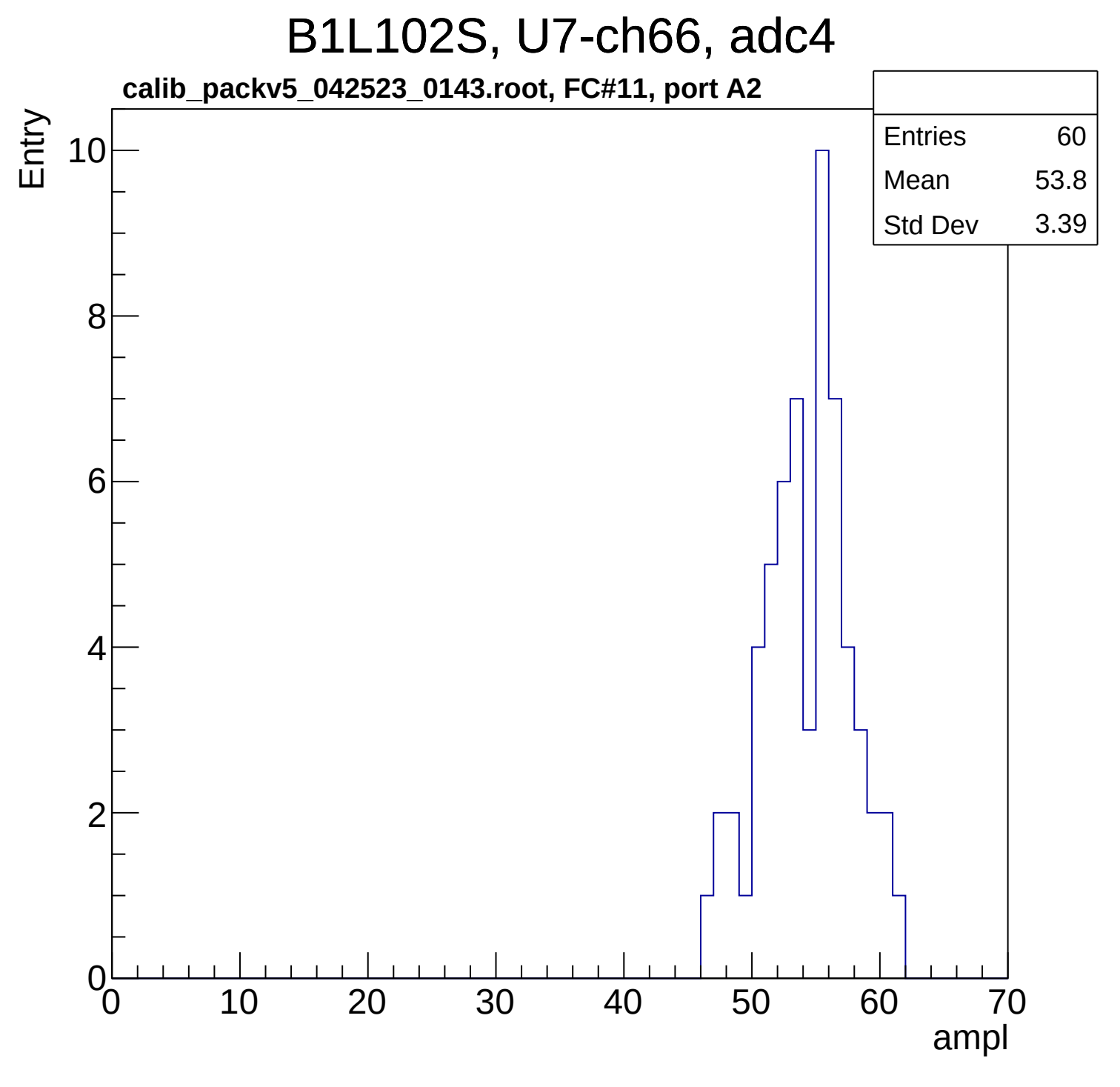
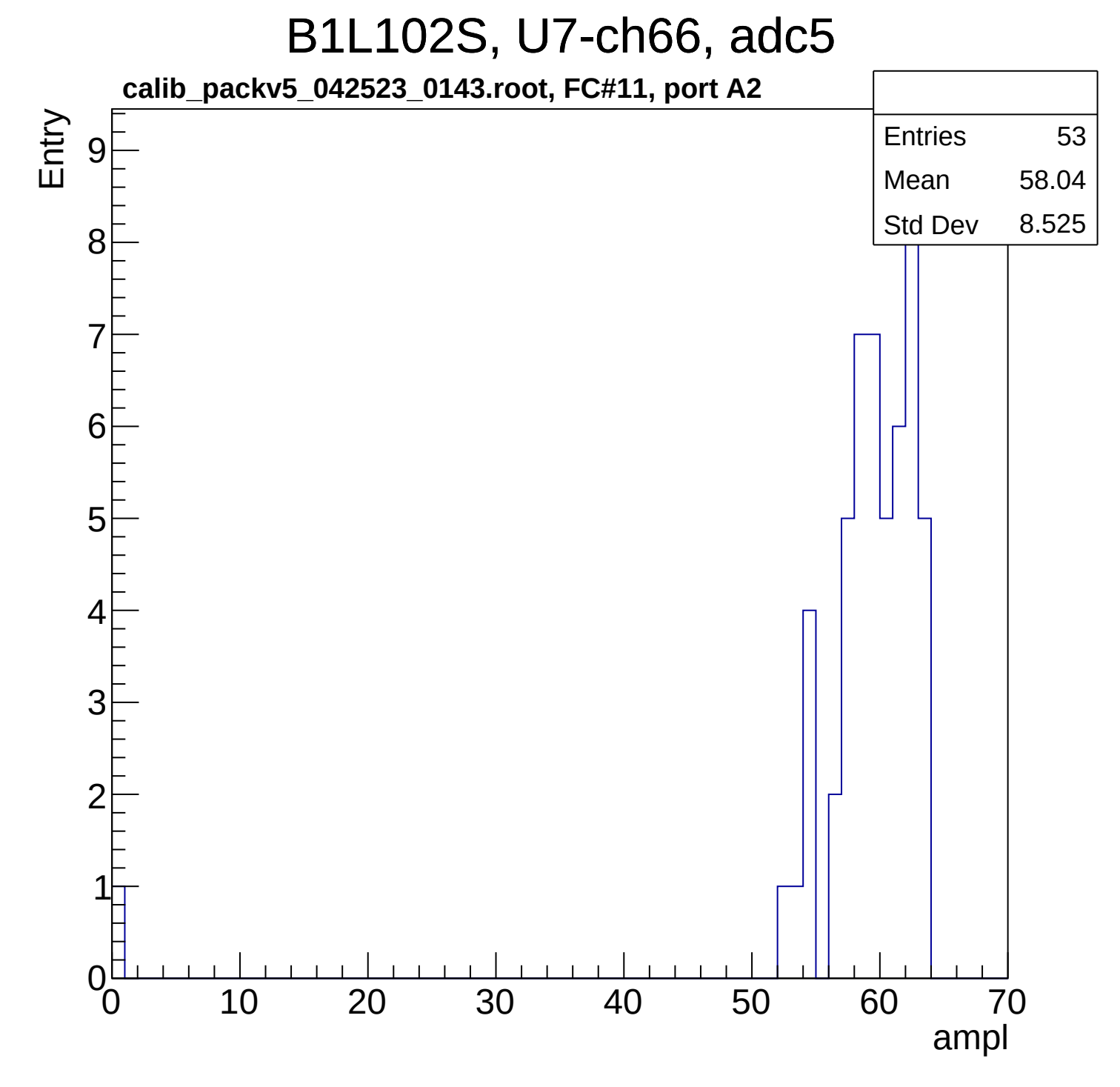

B1L102S, U7-ch66, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 59
Mean 48.53
Std Dev 3.766
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L102S, U7-ch66, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 60
Mean 53.8
Std Dev 3.39
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L102S, U7-ch66, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 53
Mean 58.04
Std Dev 8.525
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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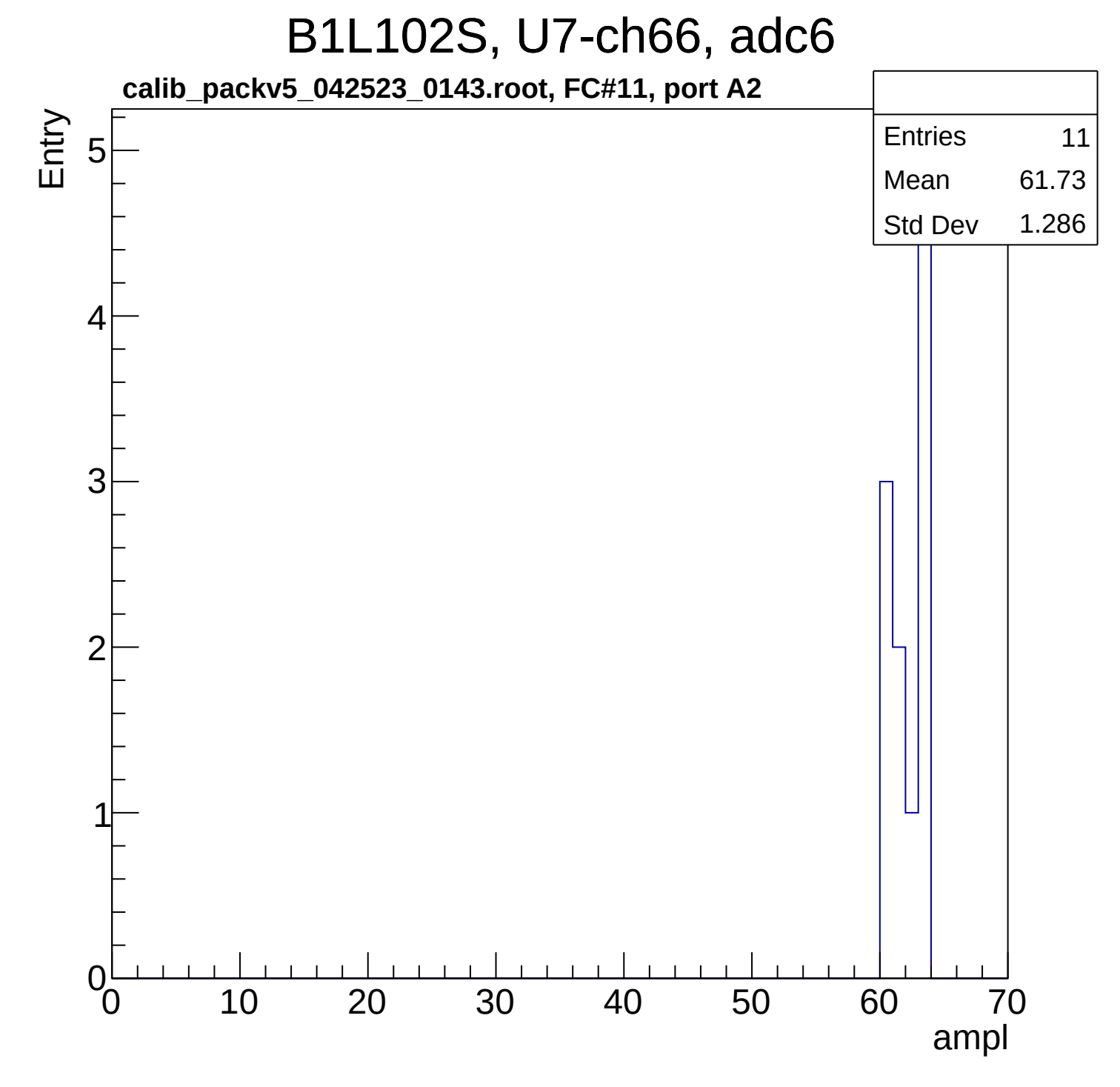
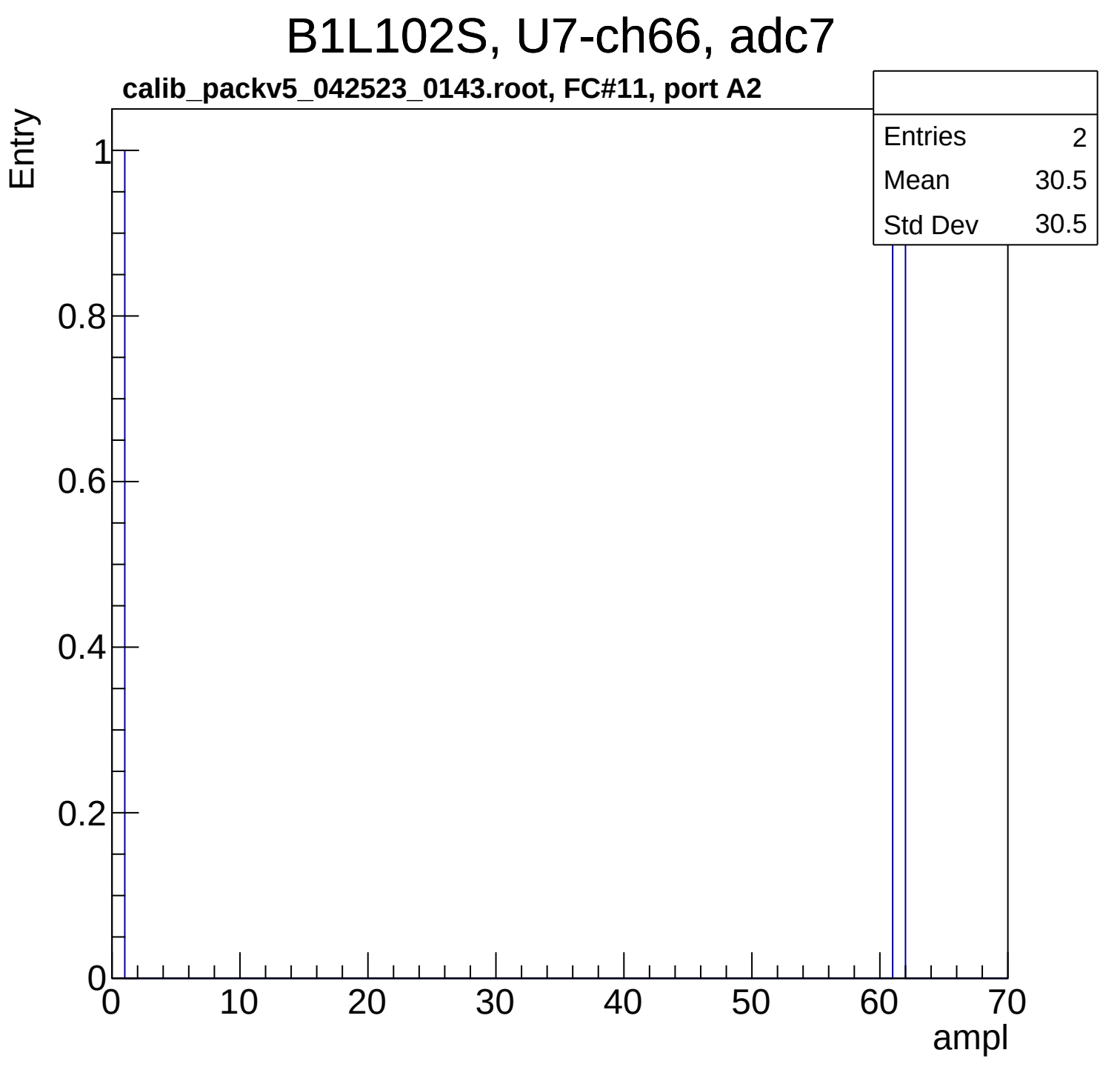
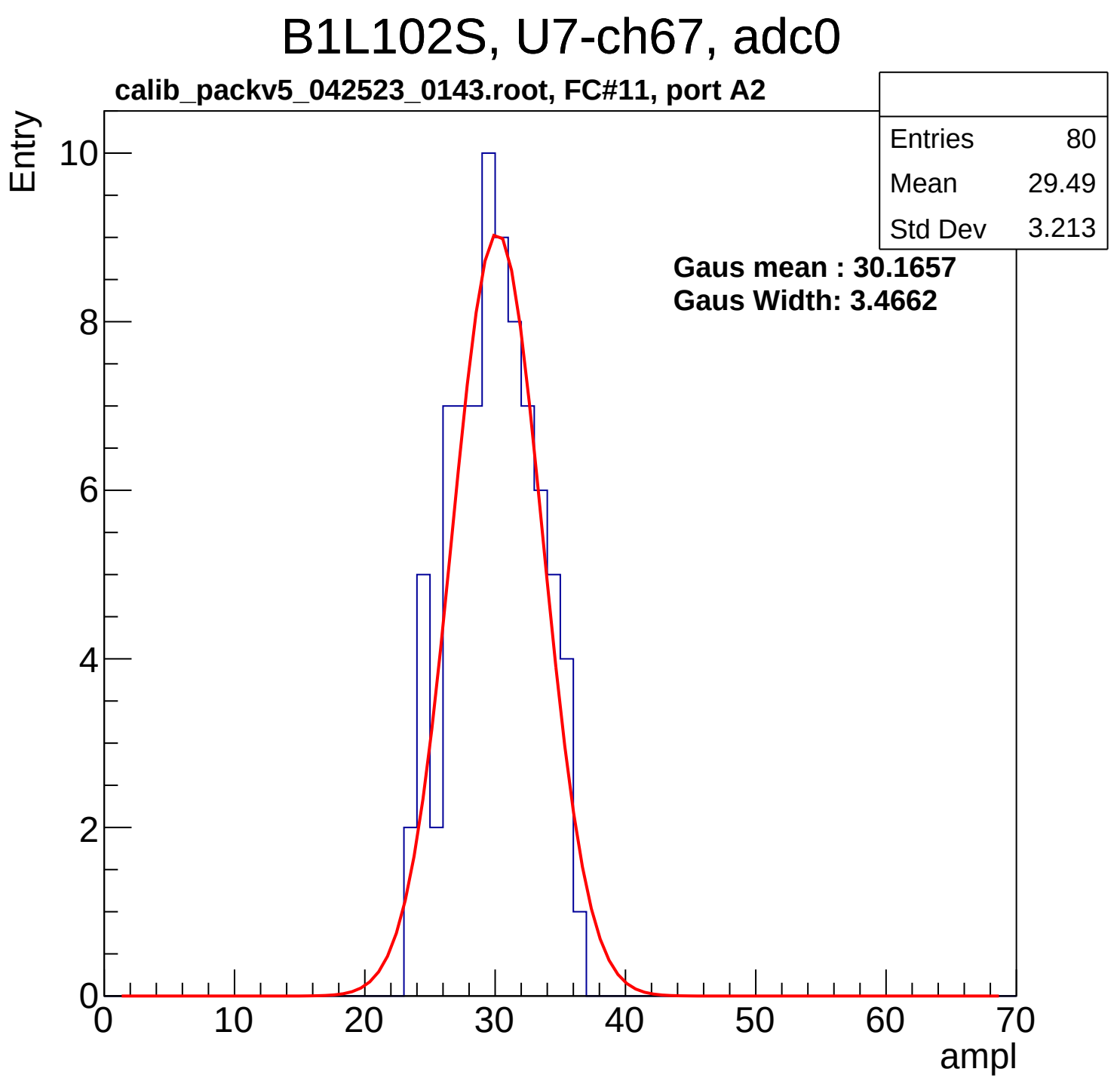
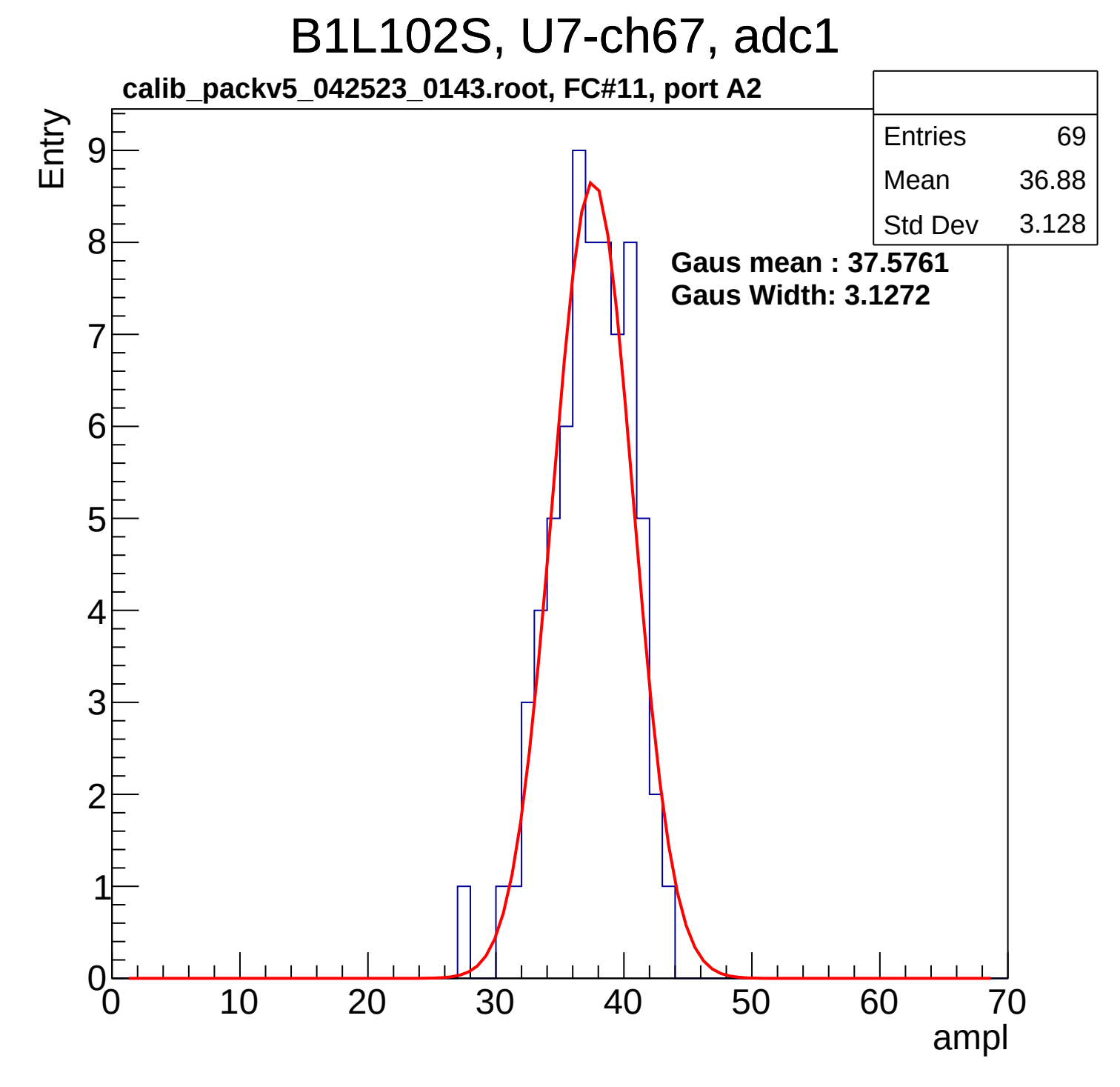
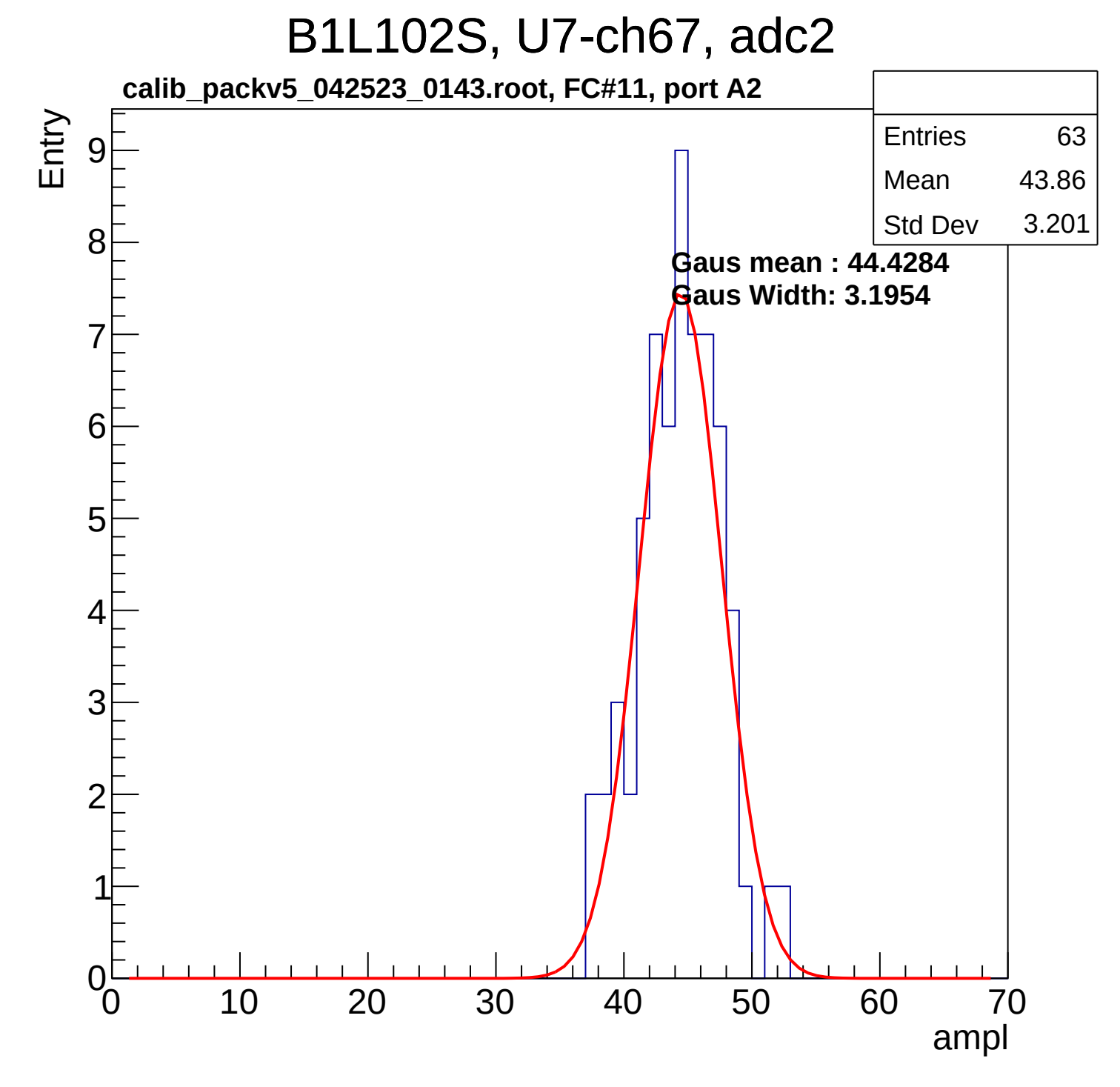

B1L102S, U7-ch66, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 11
Mean 61.73
Std Dev 1.286
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L102S, U7-ch66, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 2
Mean 30.5
Std Dev 30.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U7-ch67, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 80
Mean 29.49
Std Dev 3.213
Gaus mean : 30.1657
Gaus Width: 3.4662
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L102S, U7-ch67, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 69
Mean 36.88
Std Dev 3.128
Gaus mean : 37.5761
Gaus Width: 3.1272
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L102S, U7-ch67, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 63
Mean 43.86
Std Dev 3.201
Gaus mean : 44.4284
Gaus Width: 3.1954
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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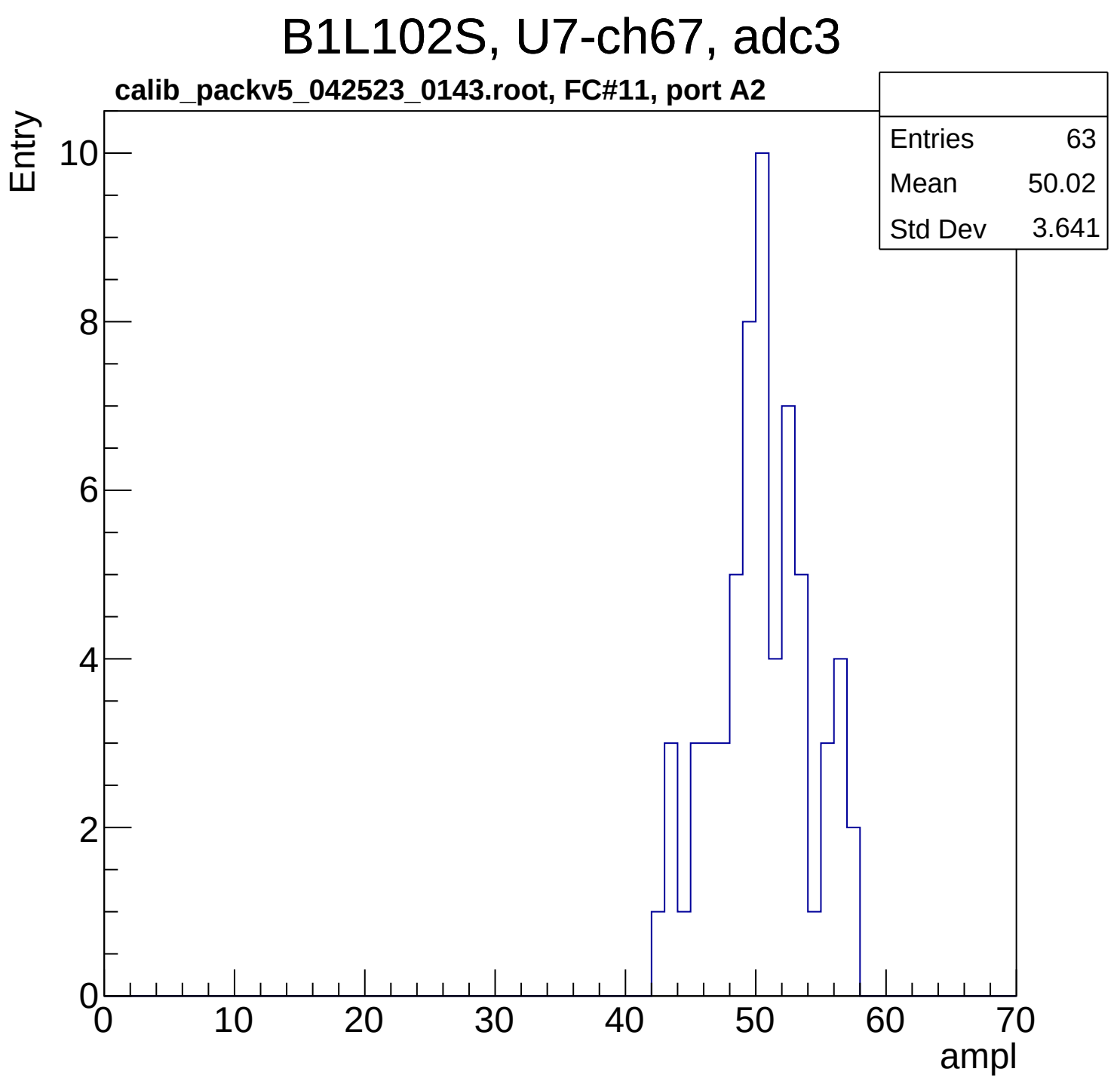
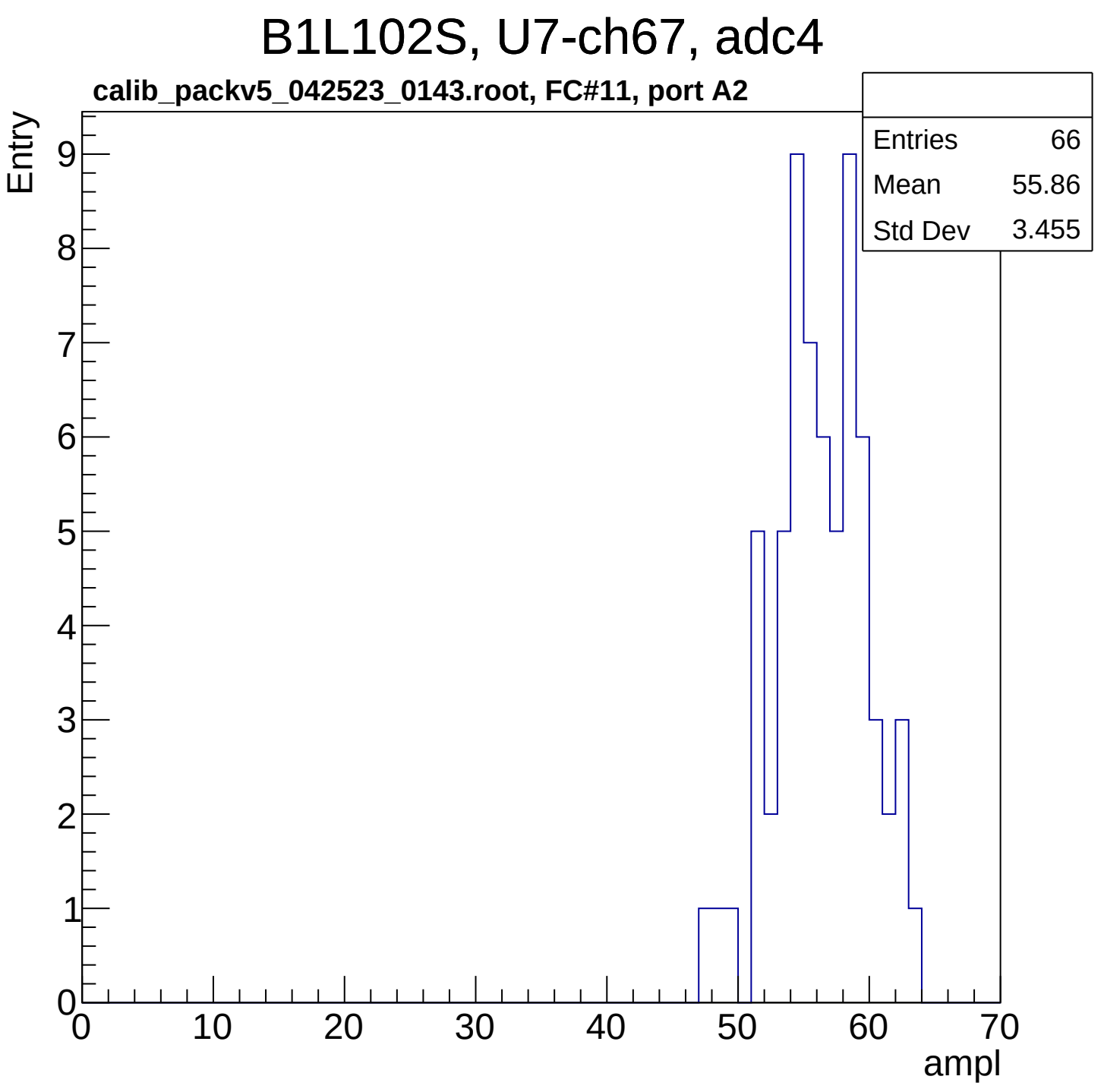
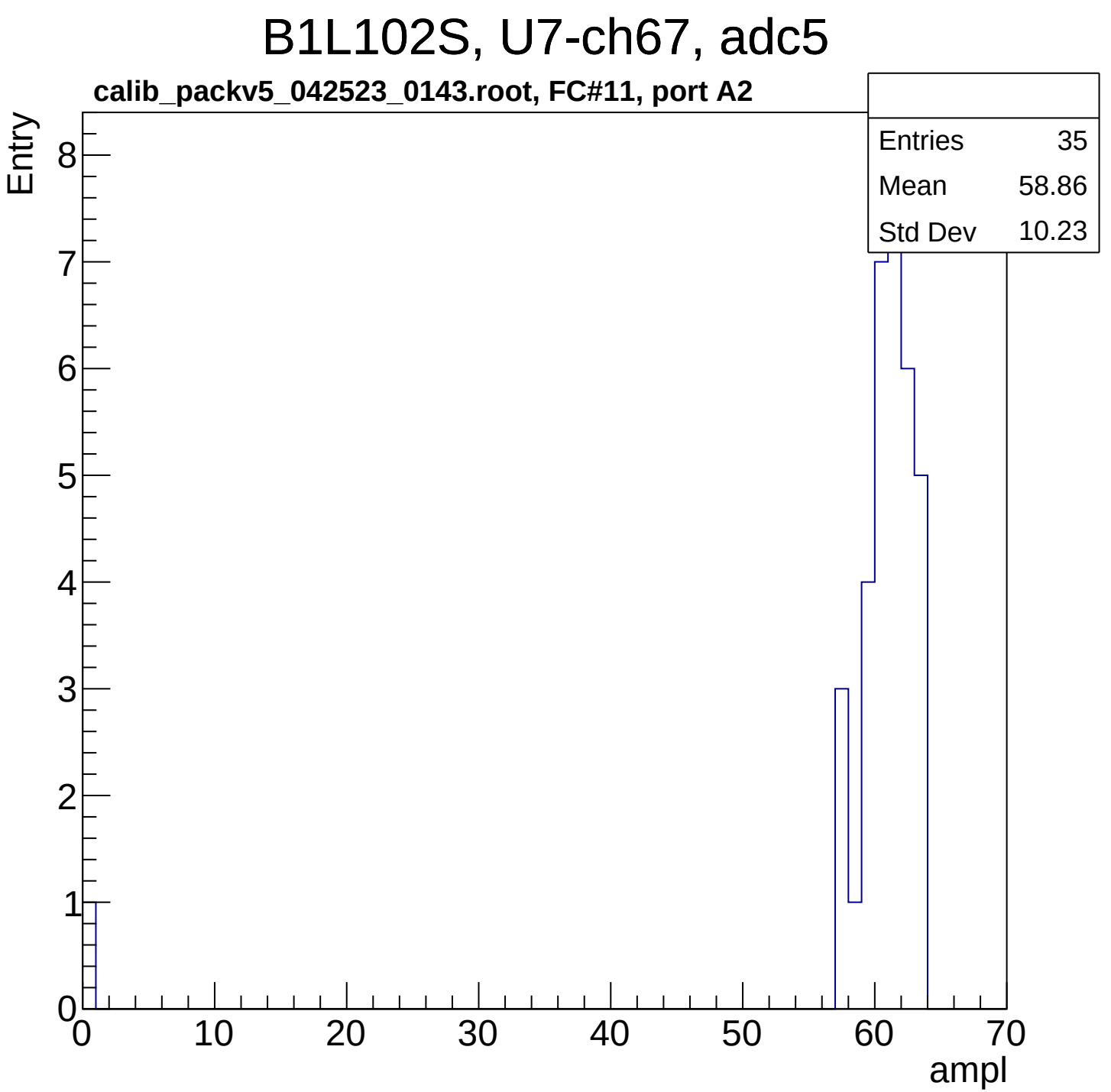

B1L102S, U7-ch67, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 63
Mean 50.02
Std Dev 3.641
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L102S, U7-ch67, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 66
Mean 55.86
Std Dev 3.455
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L102S, U7-ch67, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 35
Mean 58.86
Std Dev 10.23
Entry
ampl
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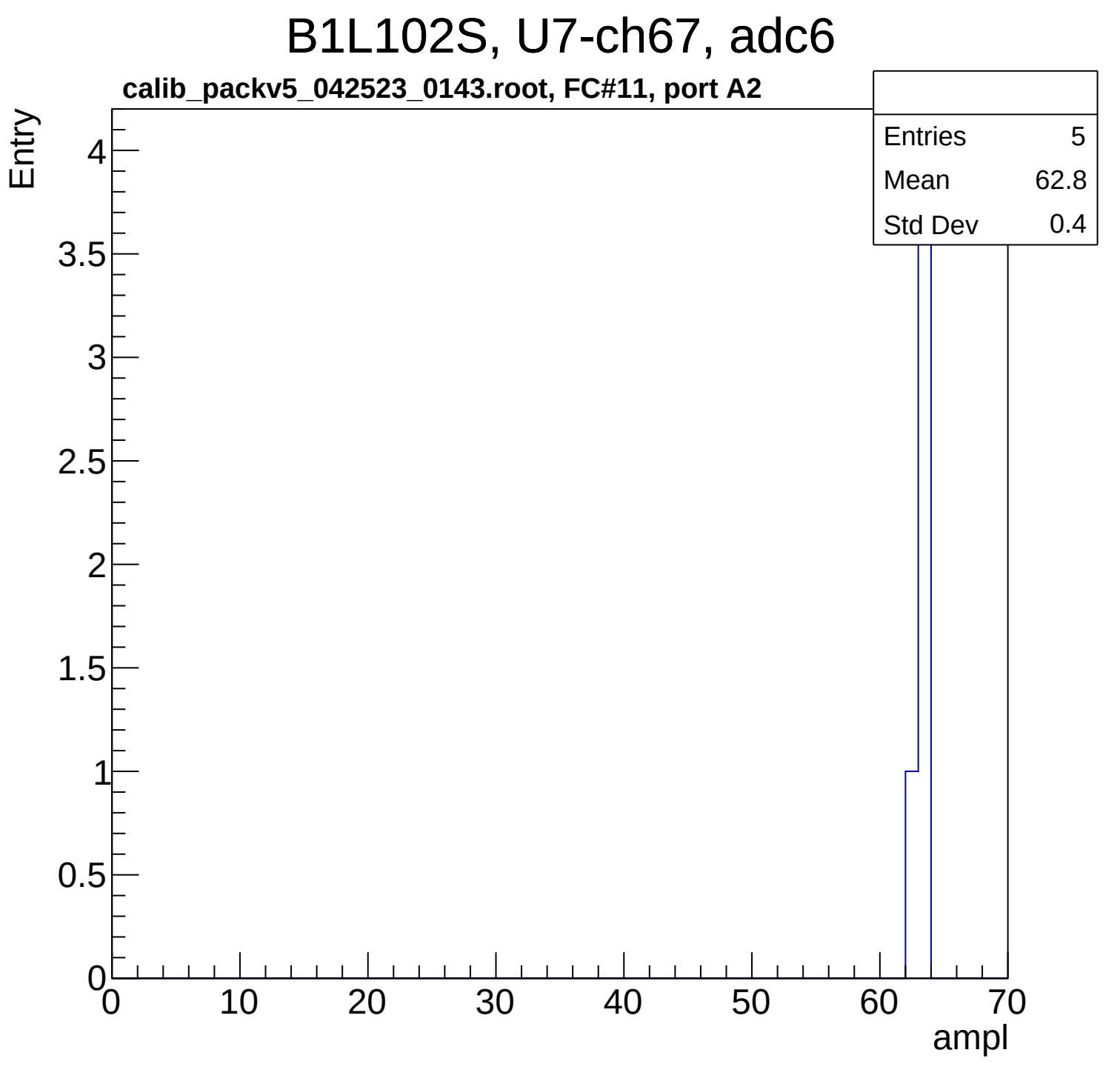
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L102S, U7-ch67, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 5
Mean 62.8
Std Dev 0.4
Entry
ampl
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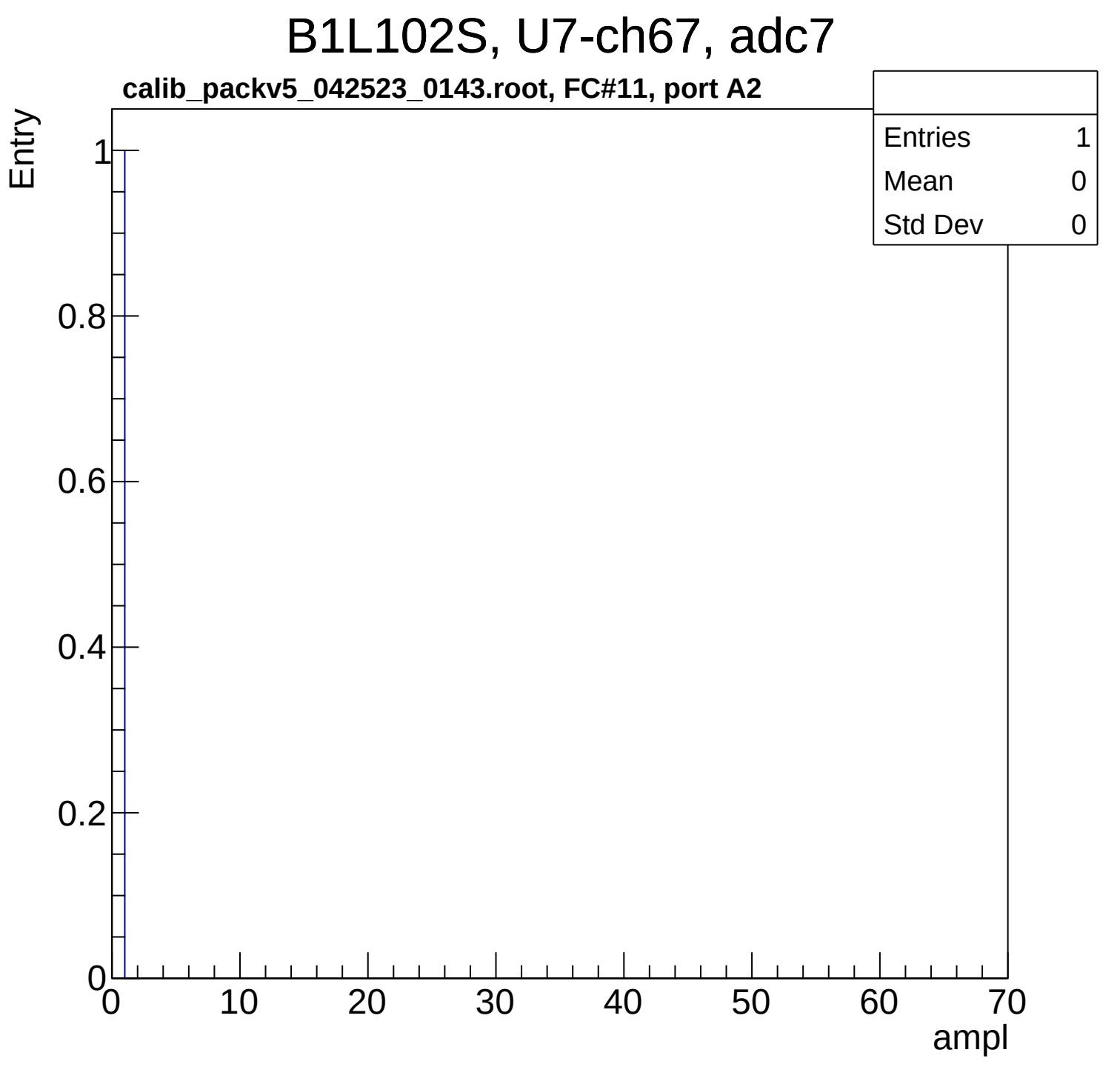
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L102S, U7-ch67, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
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10
20
30
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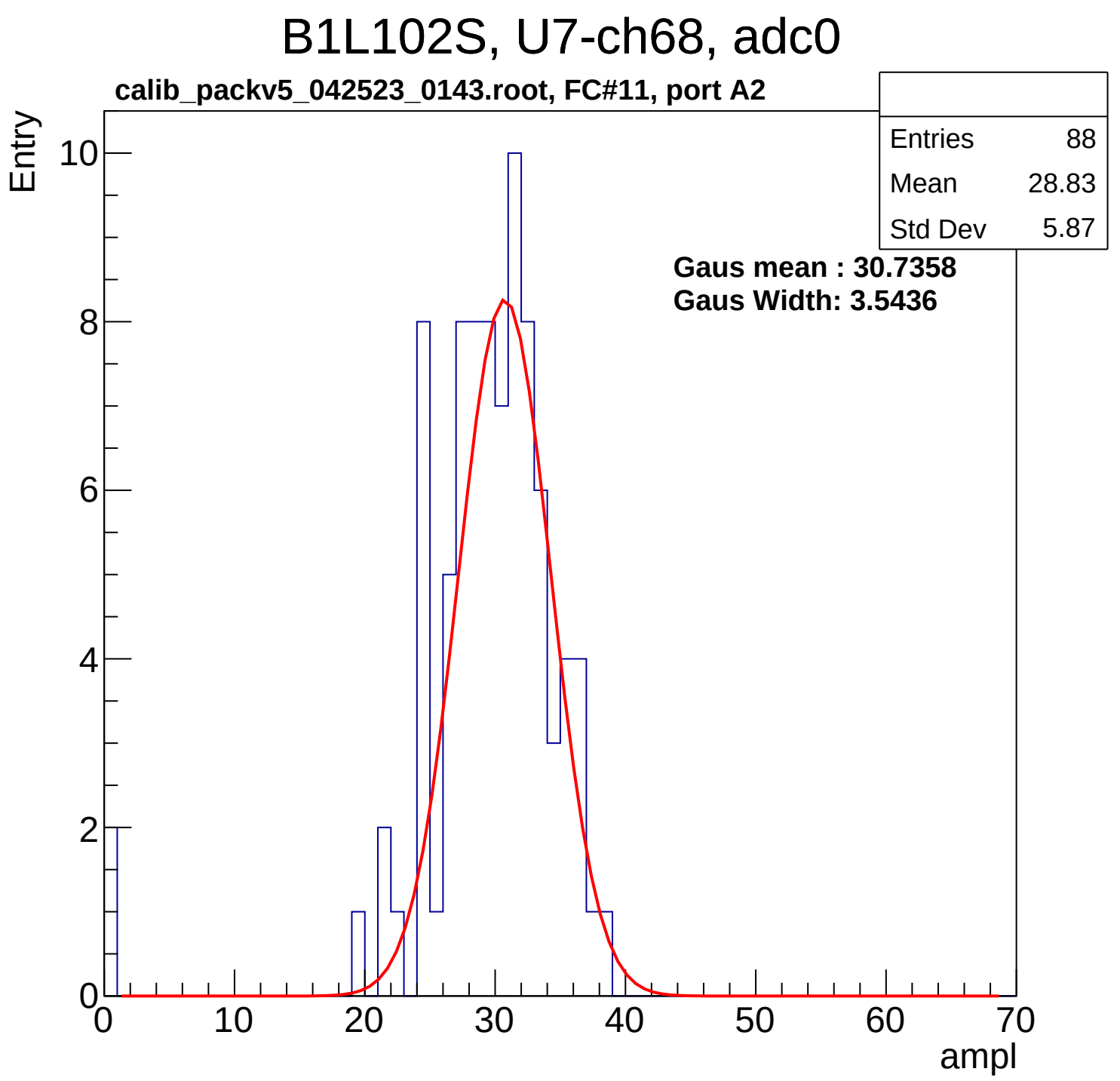
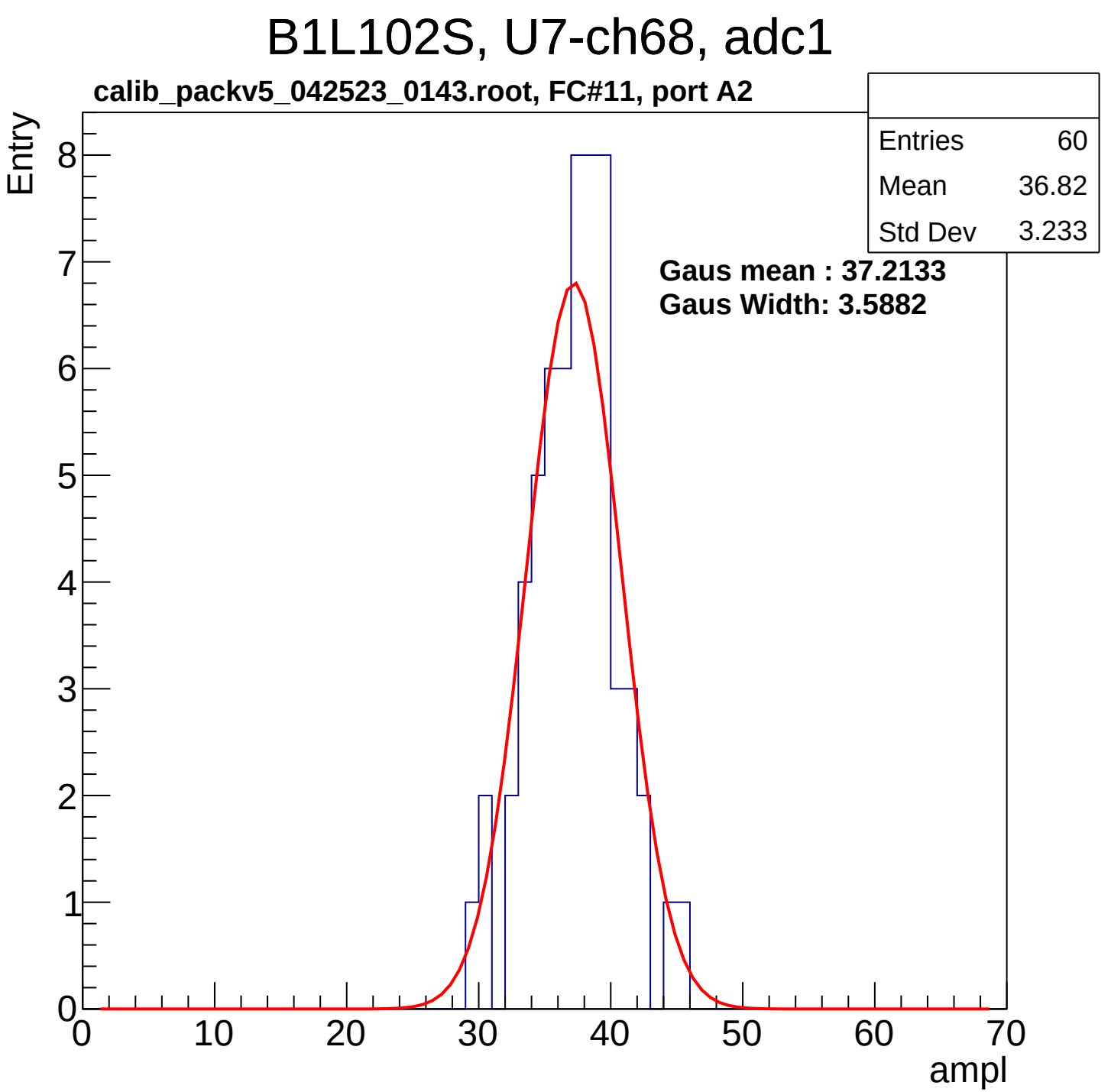
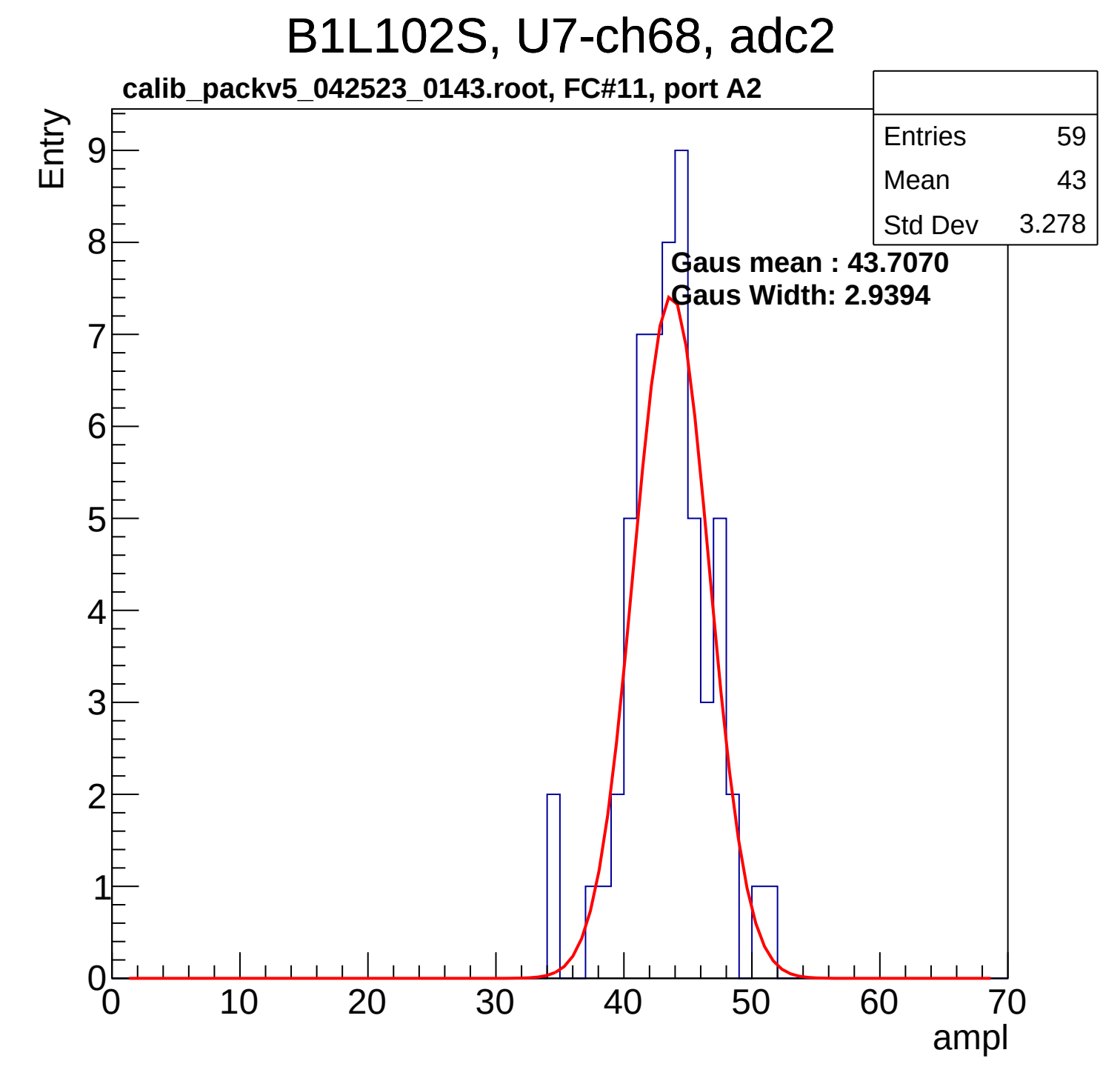
50
60
70
ampl


B1L102S, U7-ch68, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 88
Mean 28.83
Std Dev 5.87
Gaus mean : 30.7358
Gaus Width: 3.5436
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L102S, U7-ch68, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 60
Mean 36.82
Std Dev 3.233
Gaus mean : 37.2133
Gaus Width: 3.5882
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L102S, U7-ch68, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 59
Mean 43
Std Dev 3.278
Gaus mean : 43.7070
Gaus Width: 2.9394
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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40
50
60
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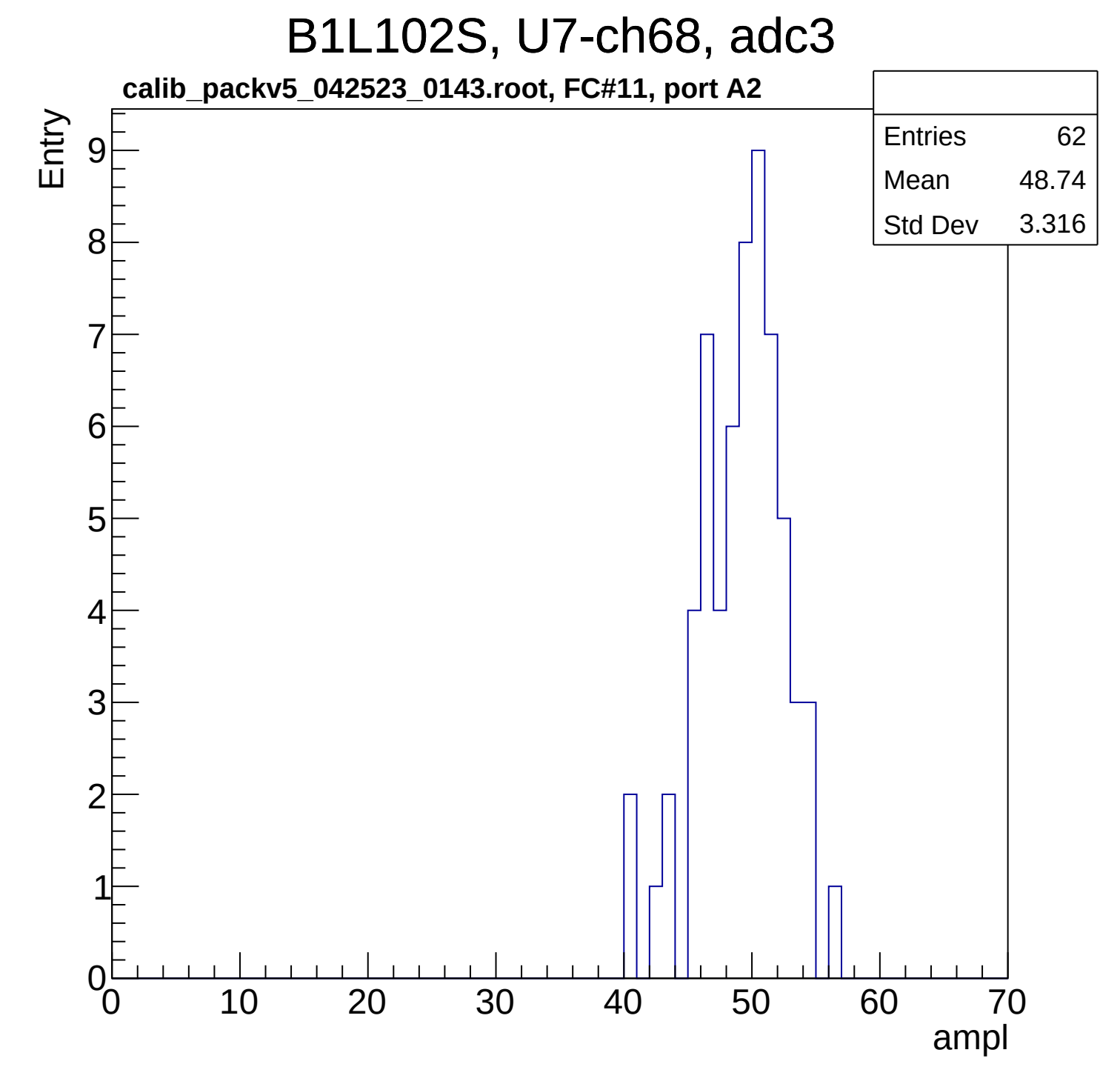
B1L102S, U7-ch68, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 62
Mean 48.74
Std Dev 3.316
Entry
ampl
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5
6
7
8
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0
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60
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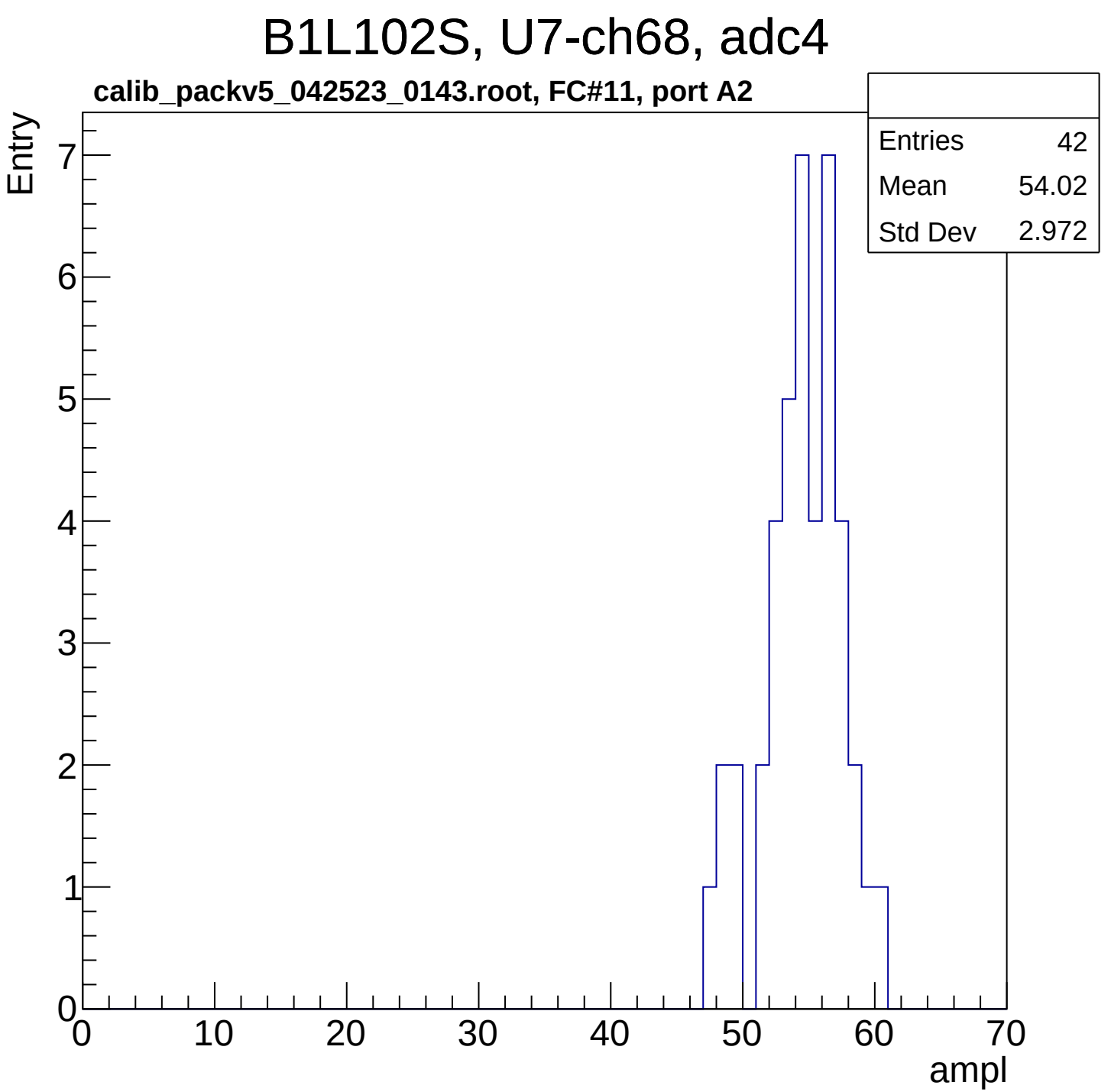
B1L102S, U7-ch68, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 42
Mean 54.02
Std Dev 2.972
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
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40
50
60
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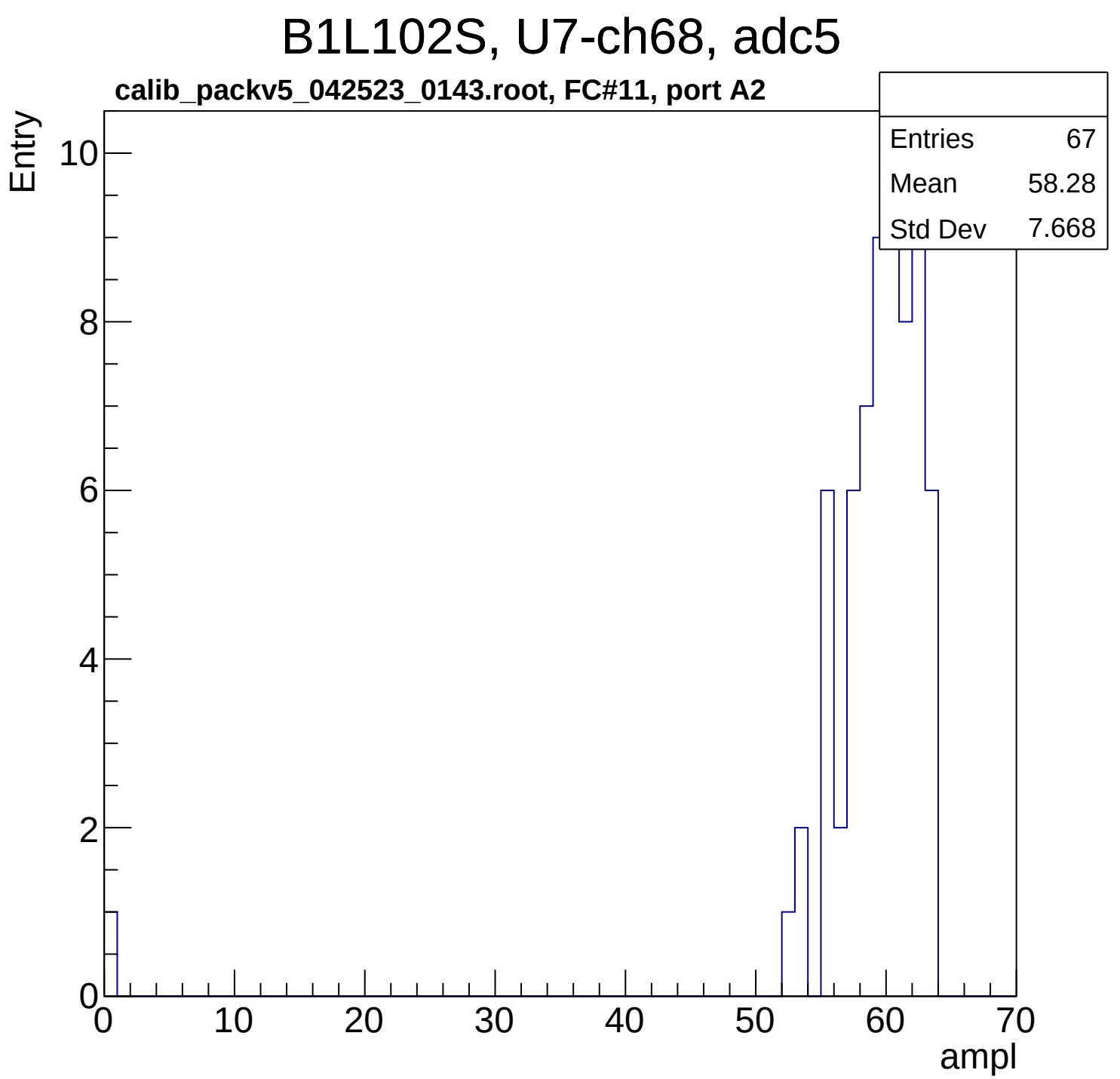
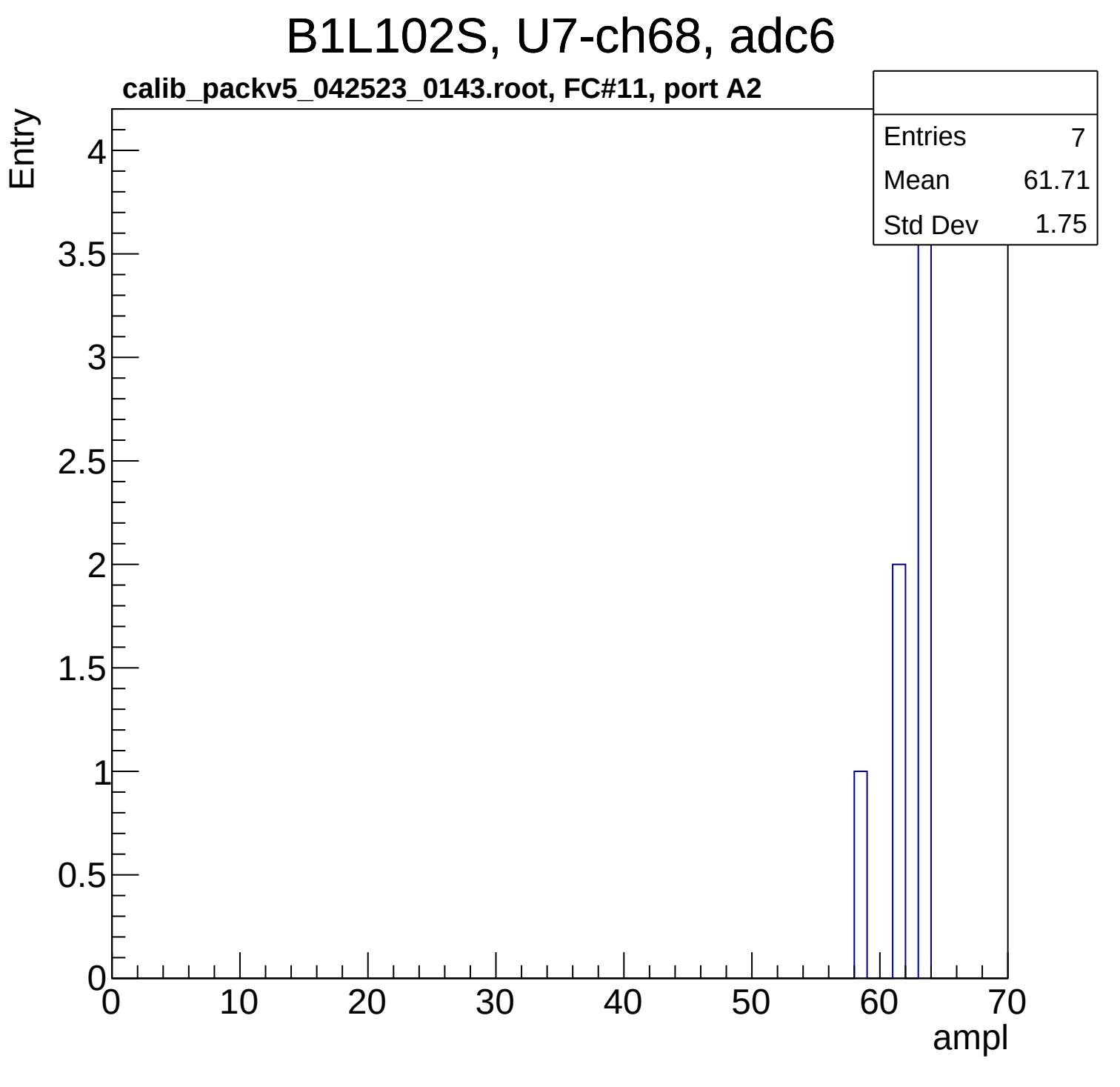

B1L102S, U7-ch68, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 67
Mean 58.28
Std Dev 7.668
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L102S, U7-ch68, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 7
Mean 61.71
Std Dev 1.75
Entry
ampl
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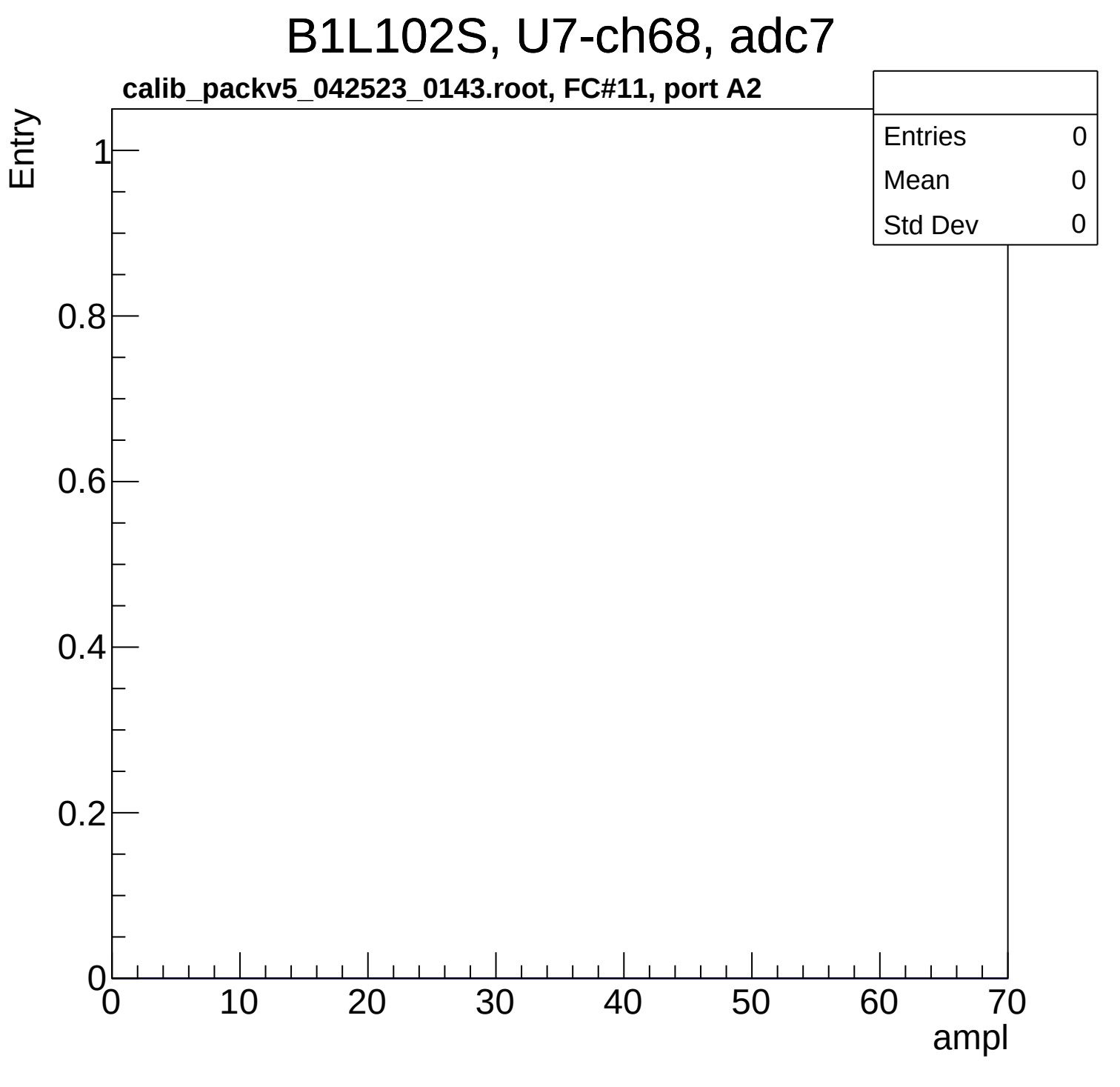
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L102S, U7-ch68, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 0
Mean 0
Std Dev 0
Entry
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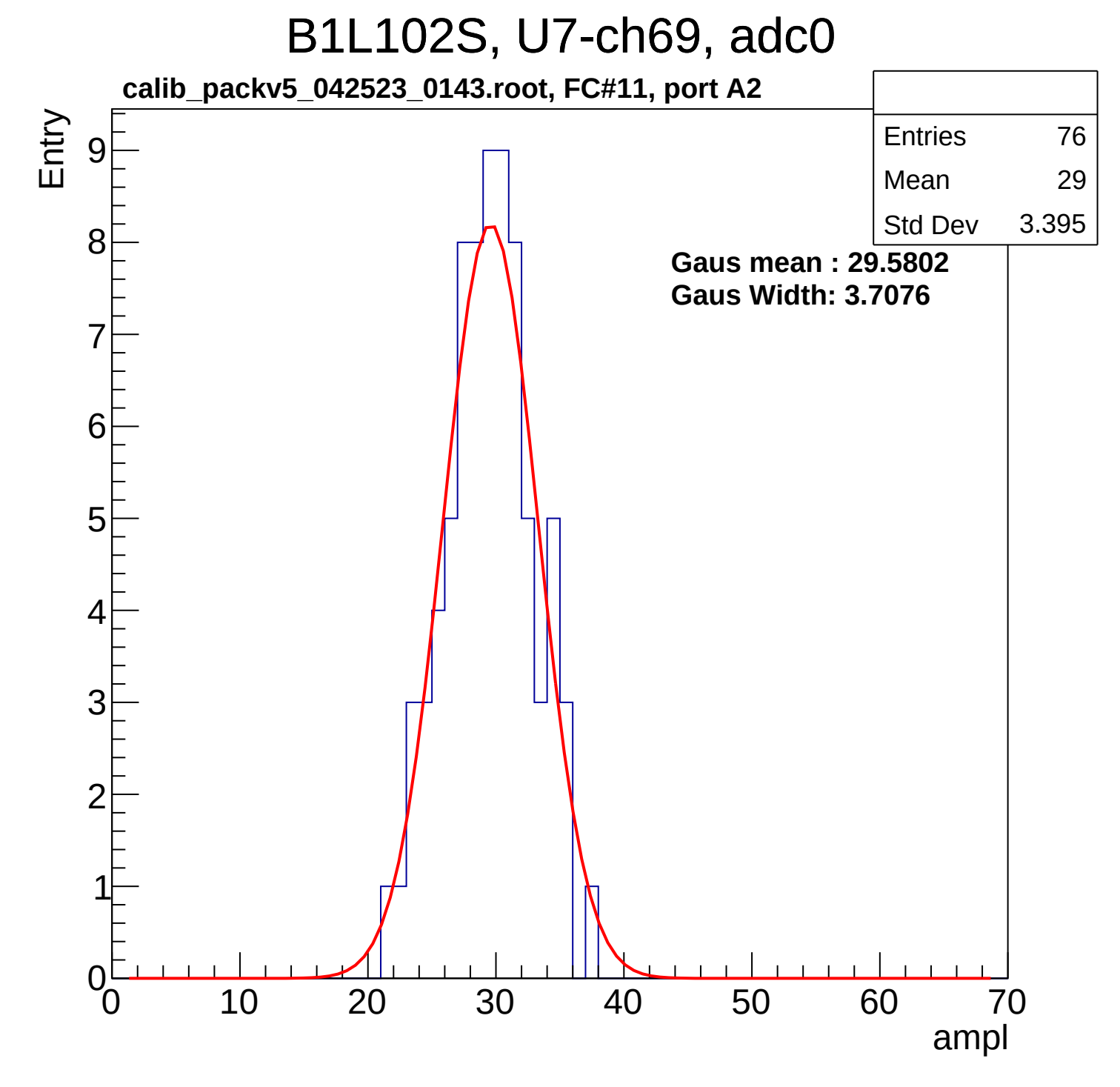
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U7-ch69, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 76
Mean 29
Std Dev 3.395
Gaus mean : 29.5802
Gaus Width: 3.7076
Entry
ampl
0
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2
3
4
5
6
7
8
9
0
10
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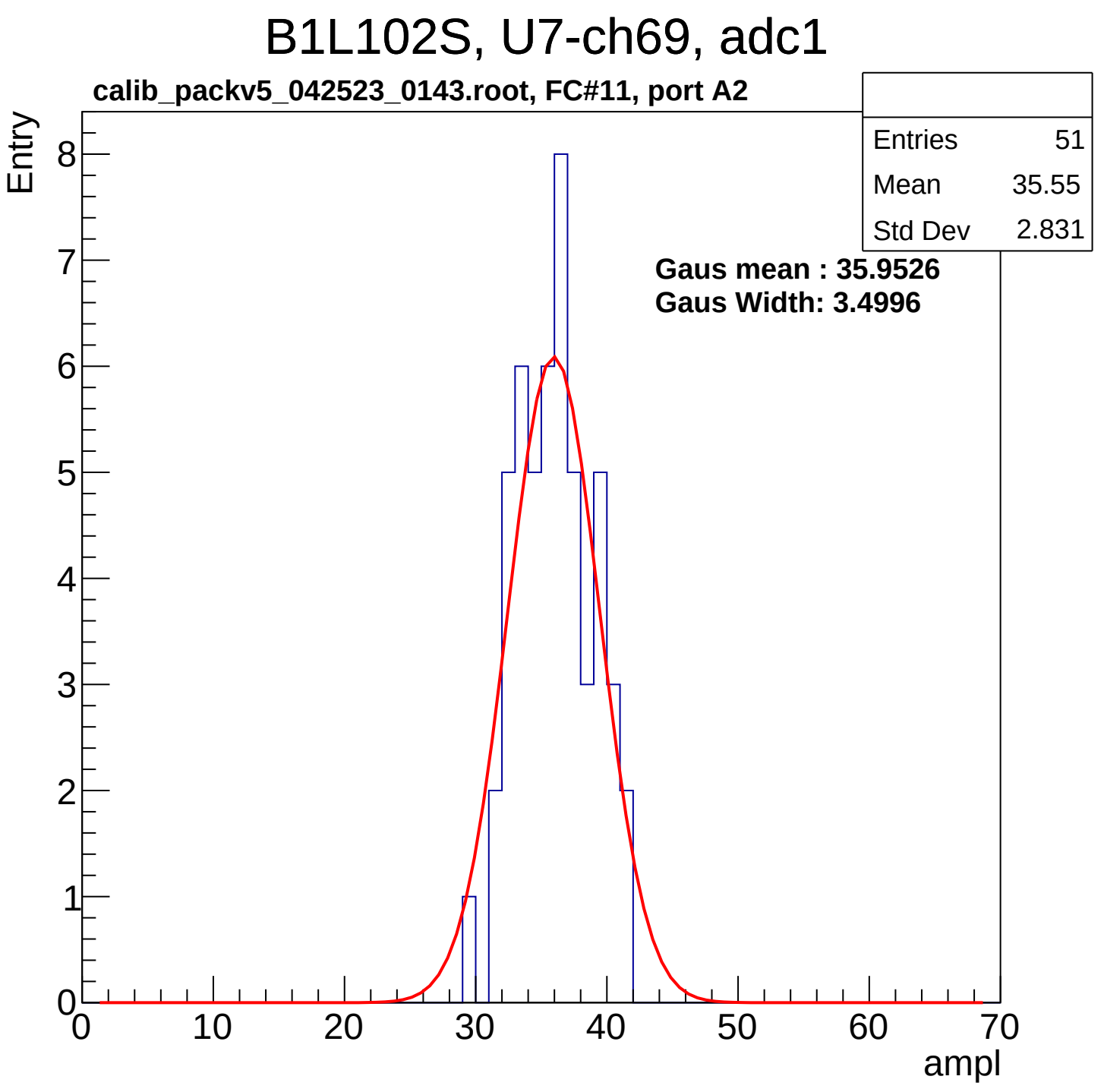
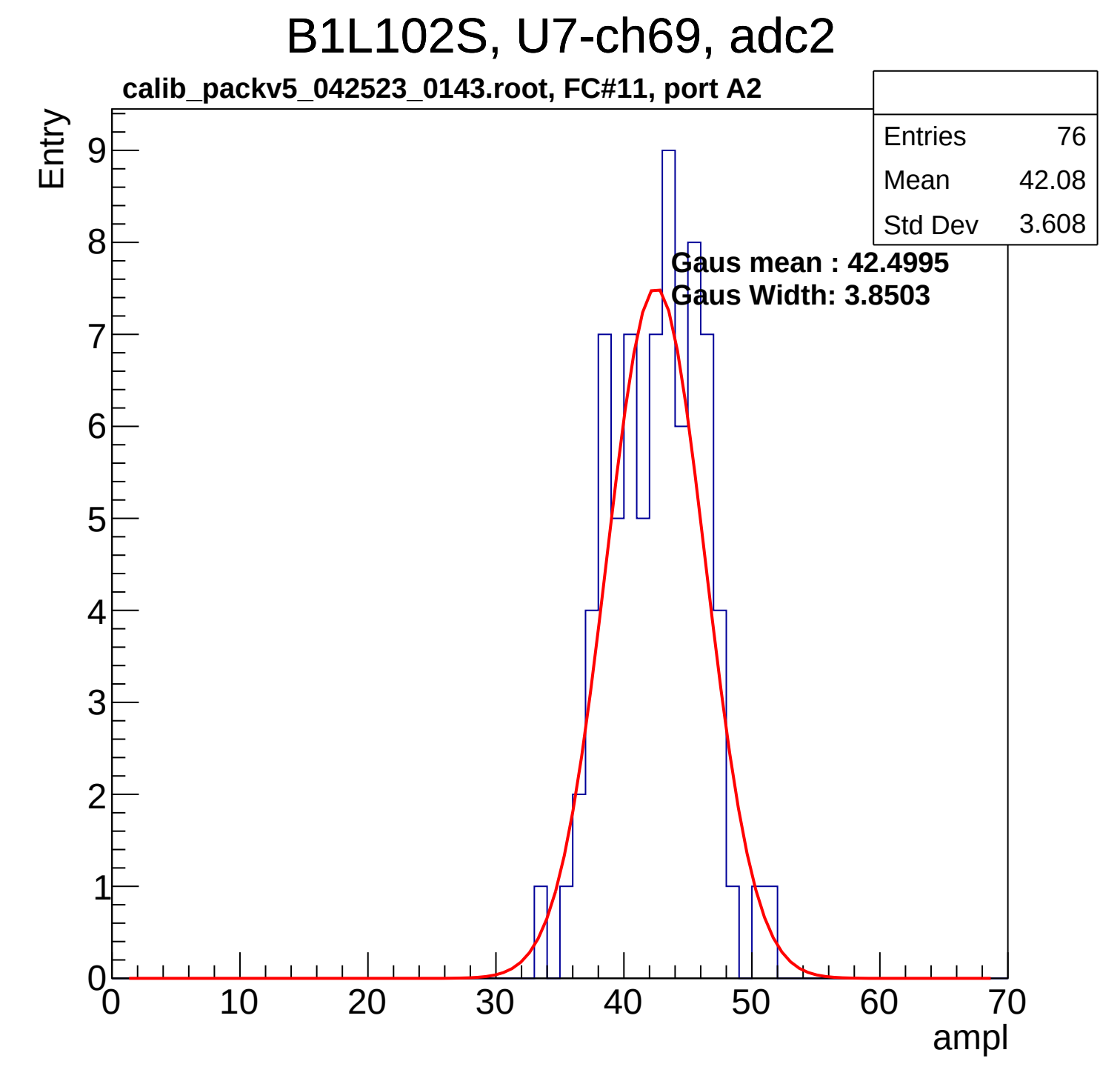

B1L102S, U7-ch69, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 51
Mean 35.55
Std Dev 2.831
Gaus mean : 35.9526
Gaus Width: 3.4996
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L102S, U7-ch69, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 76
Mean 42.08
Std Dev 3.608
Gaus mean : 42.4995
Gaus Width: 3.8503
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
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60
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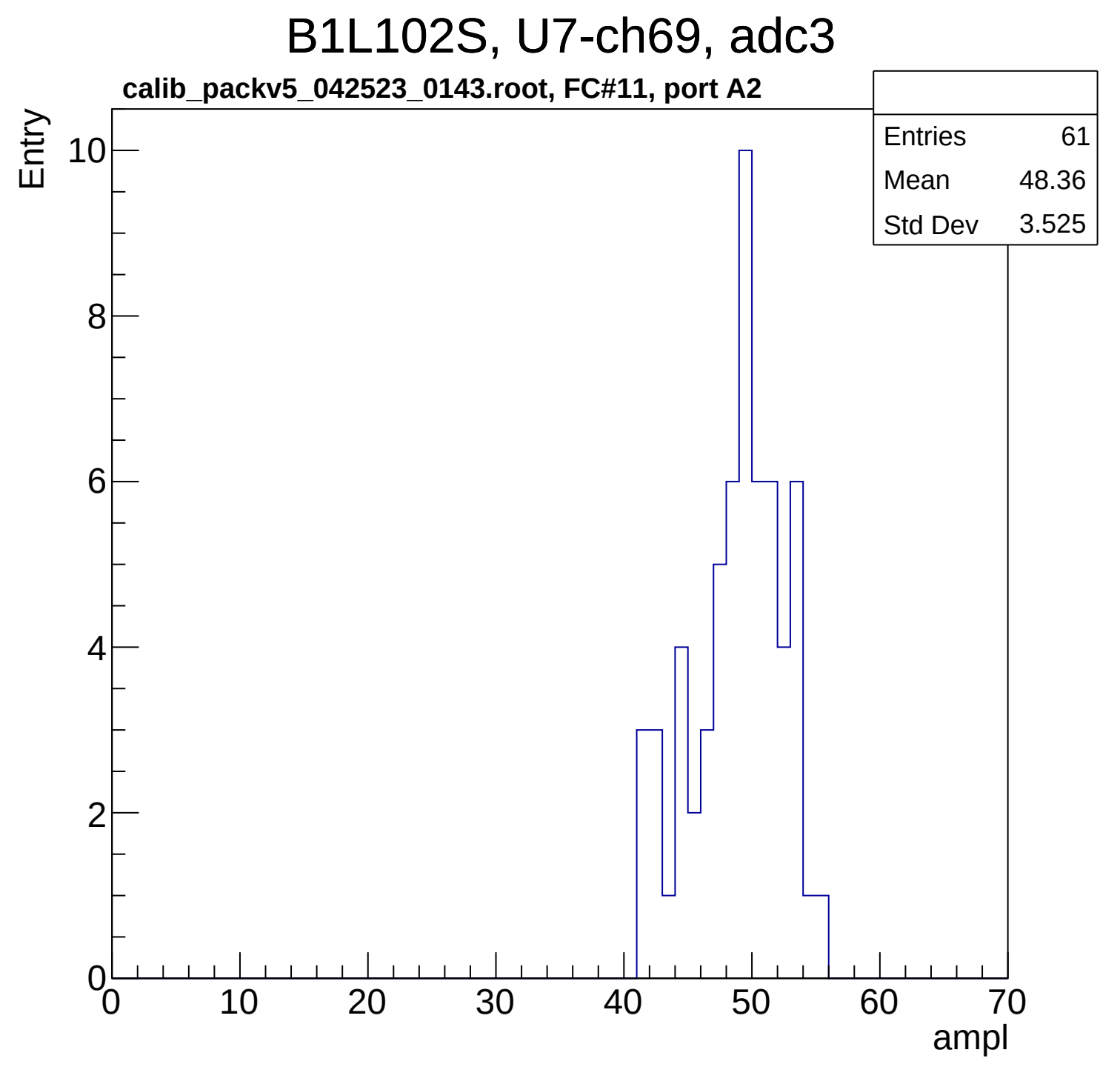
B1L102S, U7-ch69, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 61
Mean 48.36
Std Dev 3.525
Entry
ampl
0
2
4
6
8
10
0
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20
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40
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60
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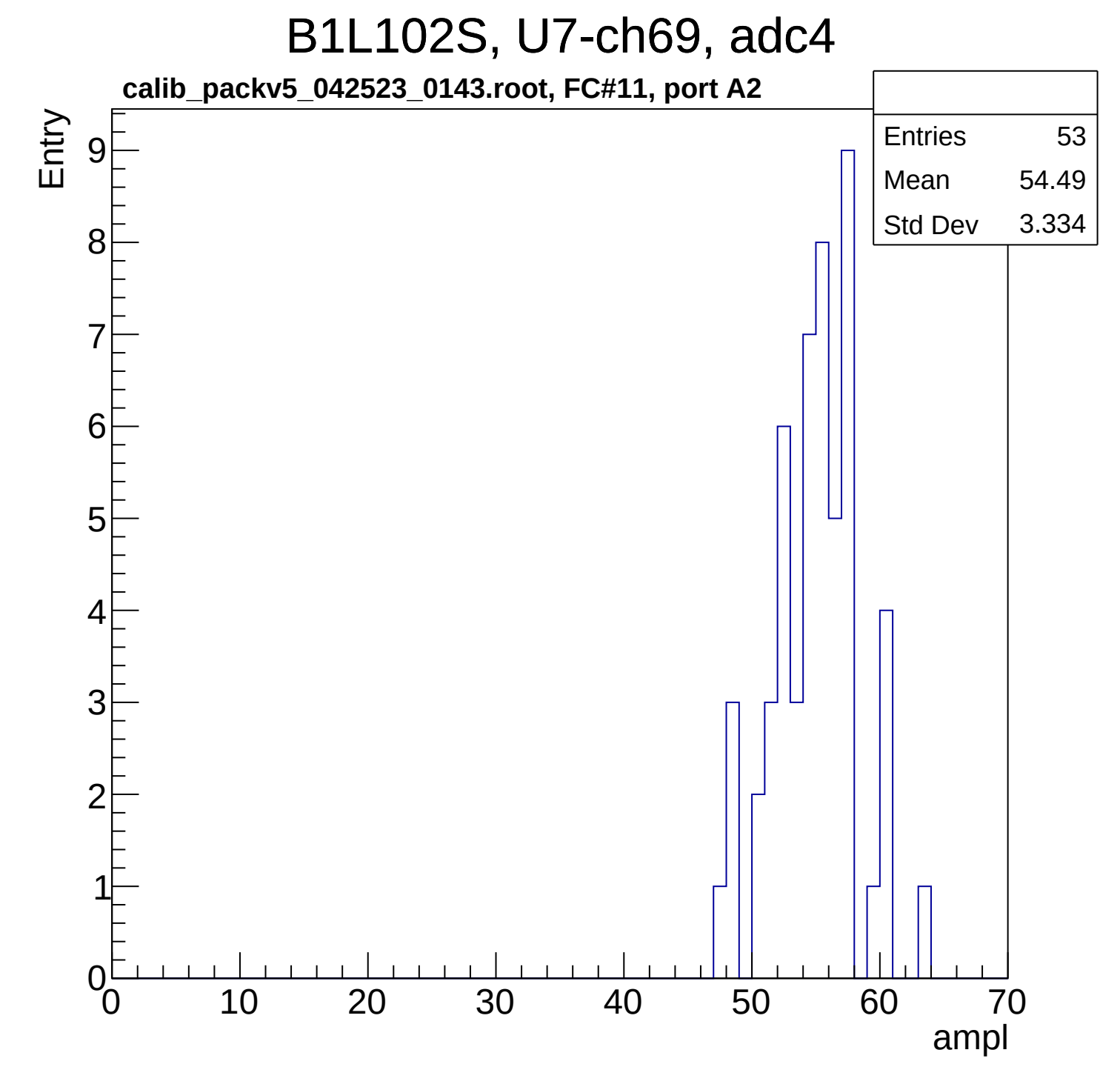
B1L102S, U7-ch69, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 53
Mean 54.49
Std Dev 3.334
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
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40
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60
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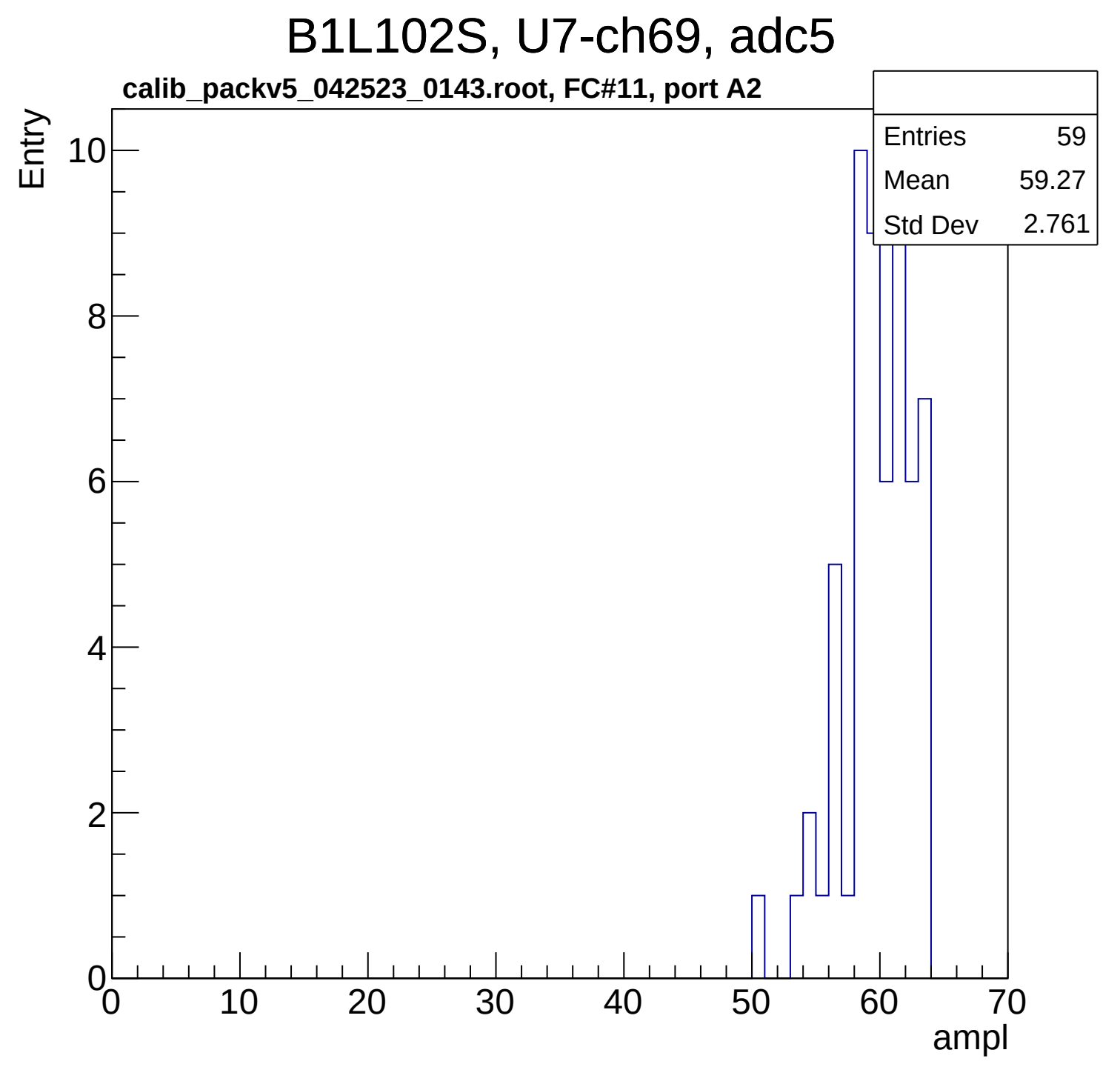
B1L102S, U7-ch69, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 59
Mean 59.27
Std Dev 2.761
Entry
ampl
0
2
4
6
8
10
0
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20
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40
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60
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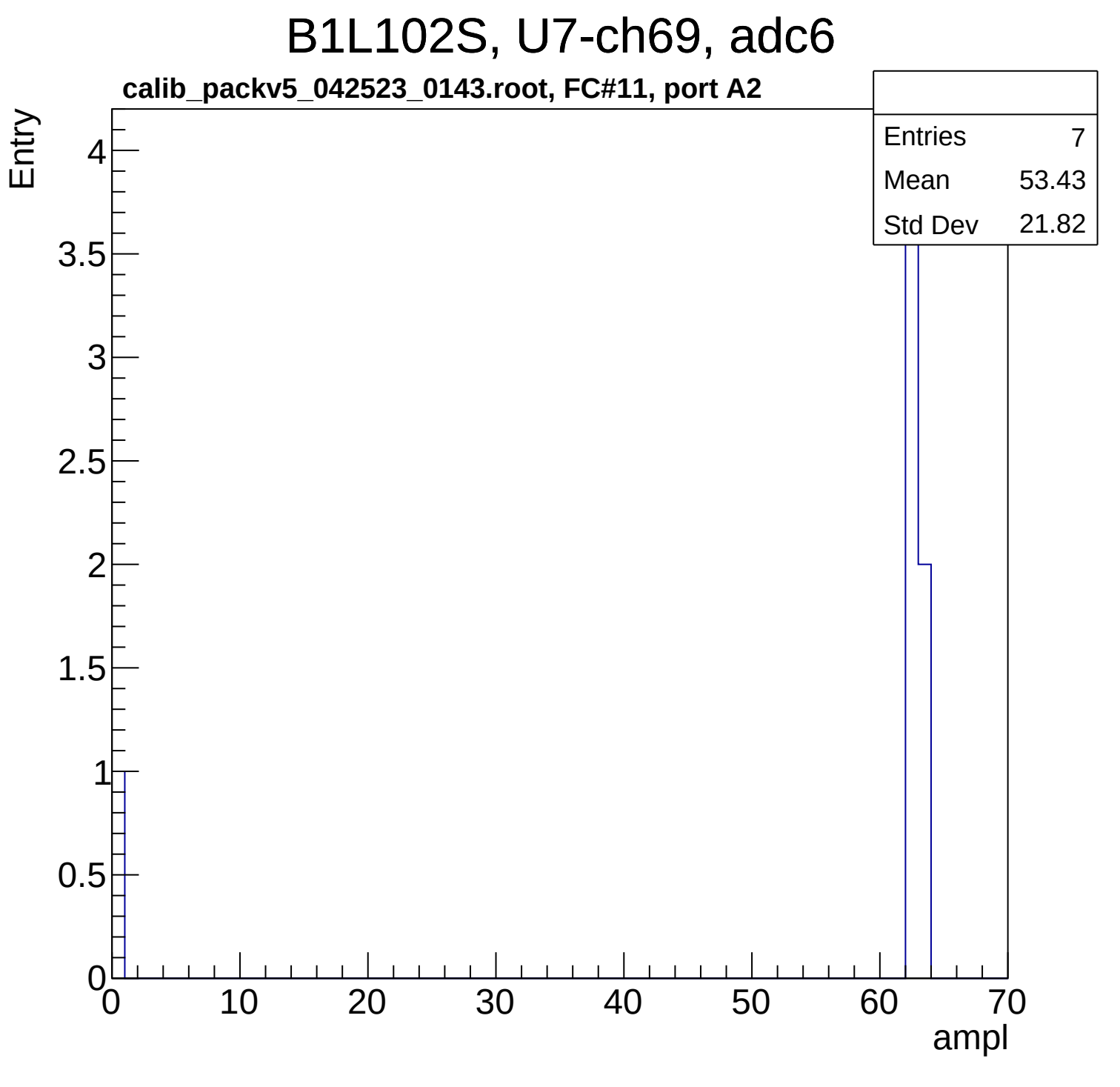
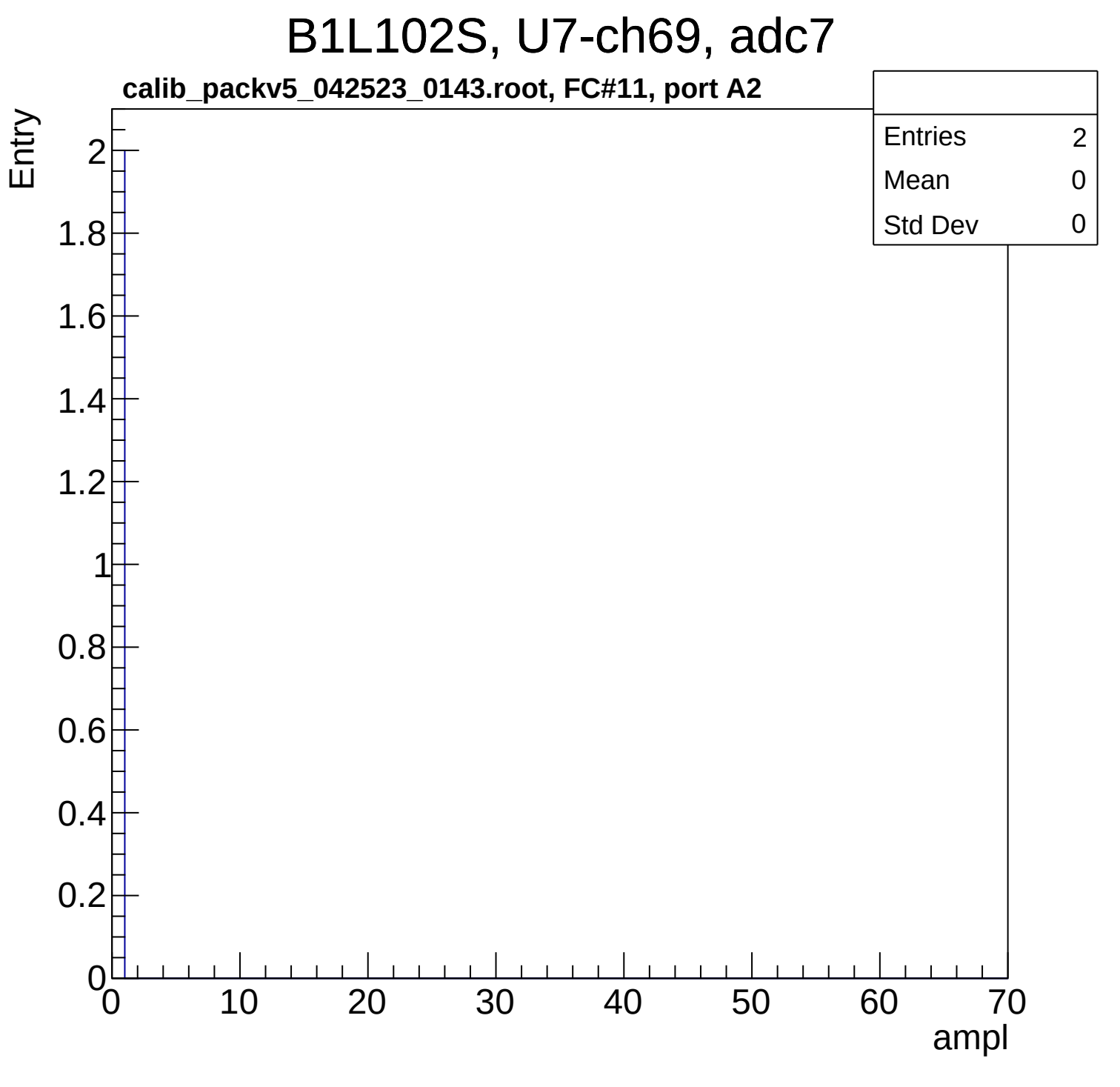

B1L102S, U7-ch69, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 7
Mean 53.43
Std Dev 21.82
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L102S, U7-ch69, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 2
Mean 0
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
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40
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60
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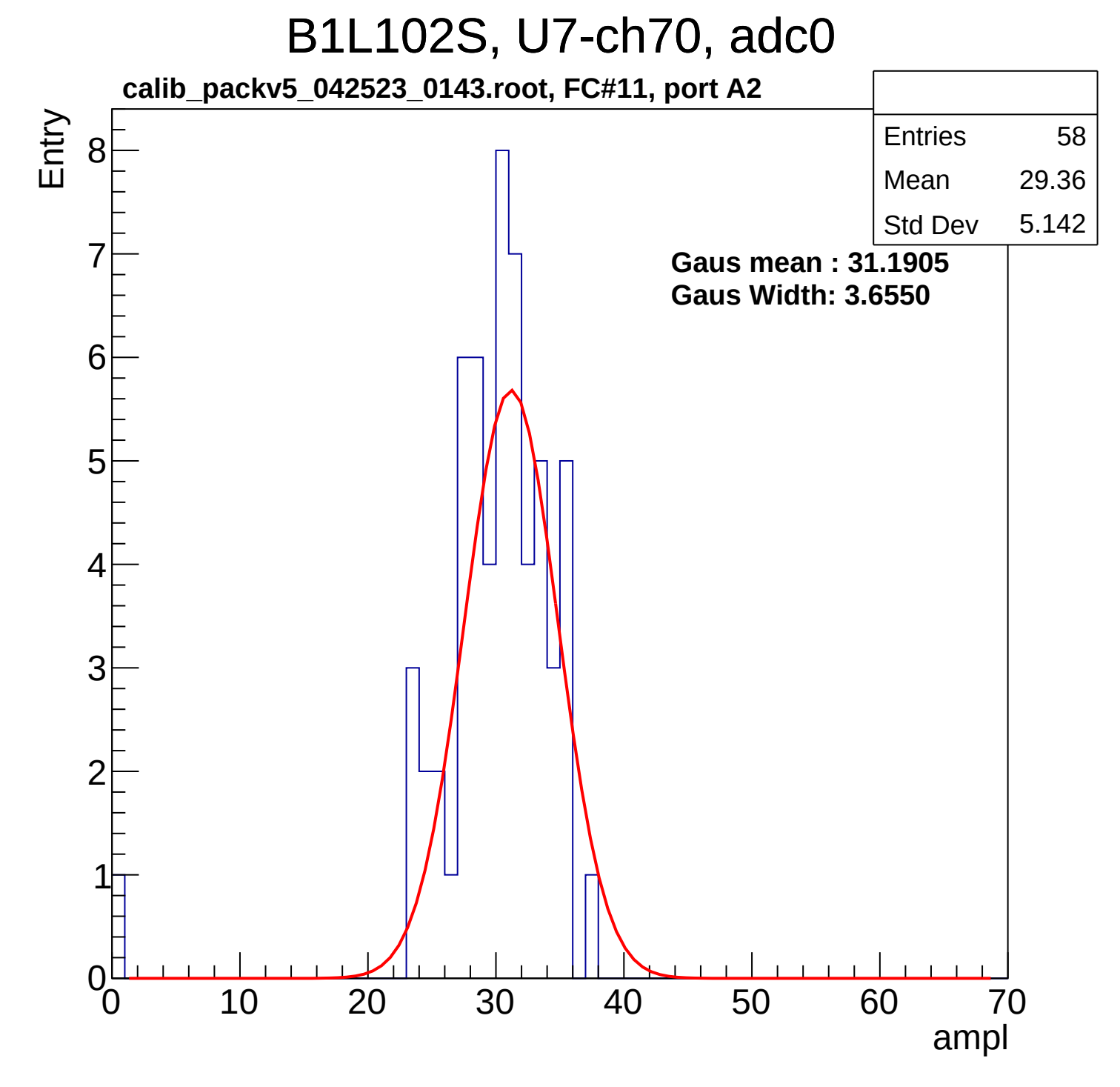
B1L102S, U7-ch70, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 58
Mean 29.36
Std Dev 5.142
Gaus mean : 31.1905
Gaus Width: 3.6550
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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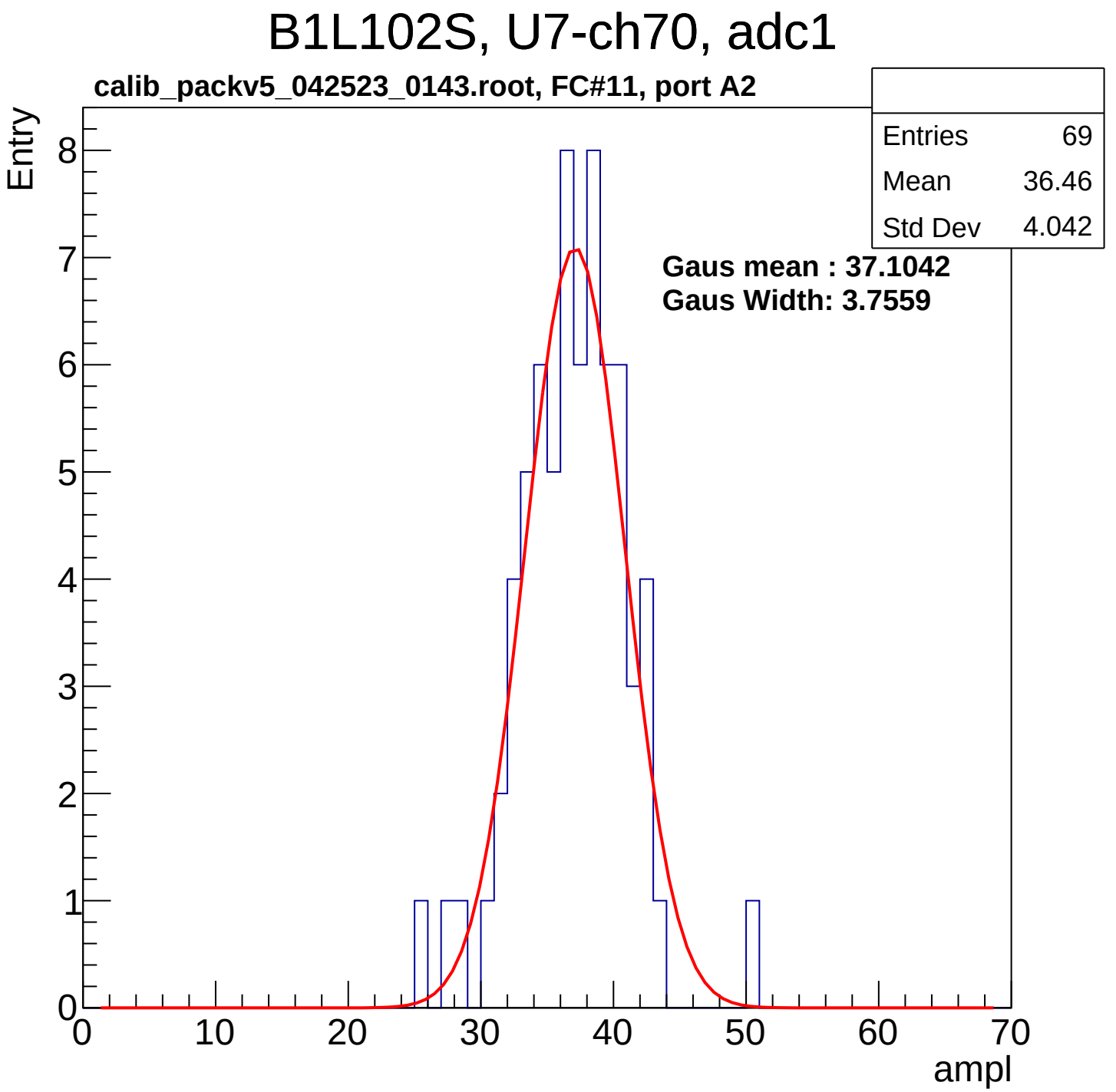
B1L102S, U7-ch70, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 69
Mean 36.46
Std Dev 4.042
Gaus mean : 37.1042
Gaus Width: 3.7559
Entry
ampl
0
1
2
3
4
5
6
7
8
0
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20
30
40
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60
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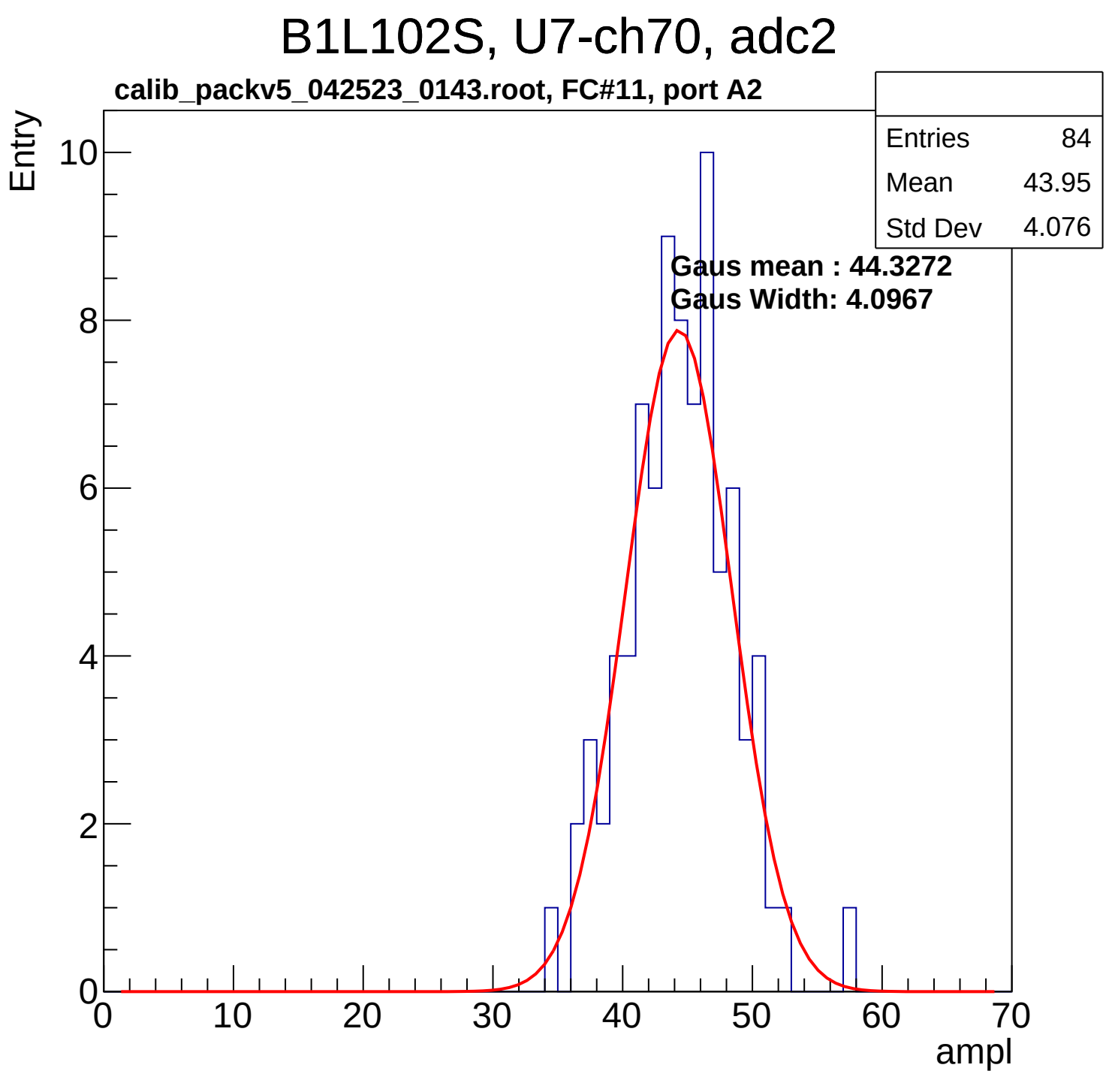
B1L102S, U7-ch70, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 84
Mean 43.95
Std Dev 4.076
Gaus mean : 44.3272
Gaus Width: 4.0967
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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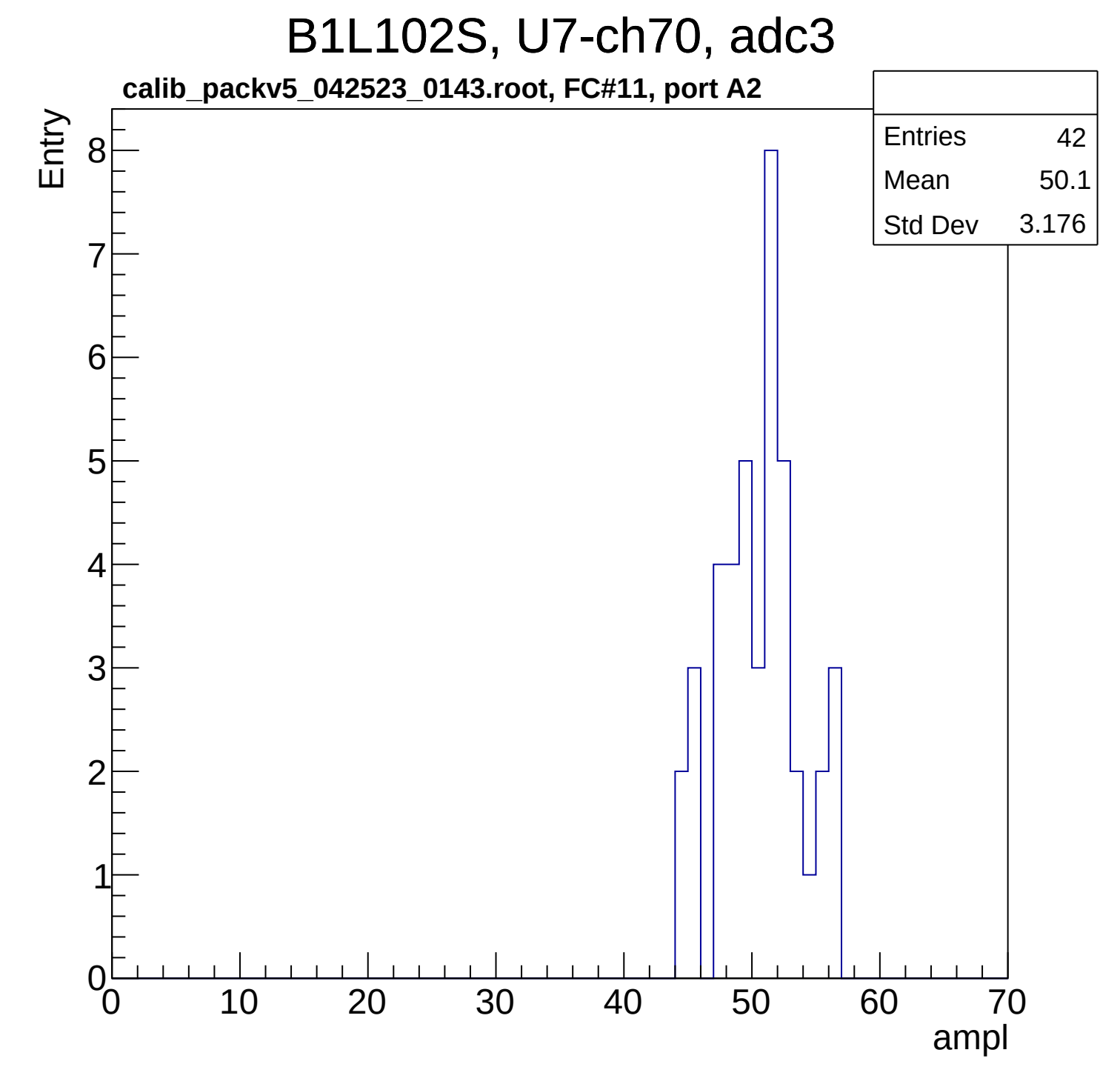
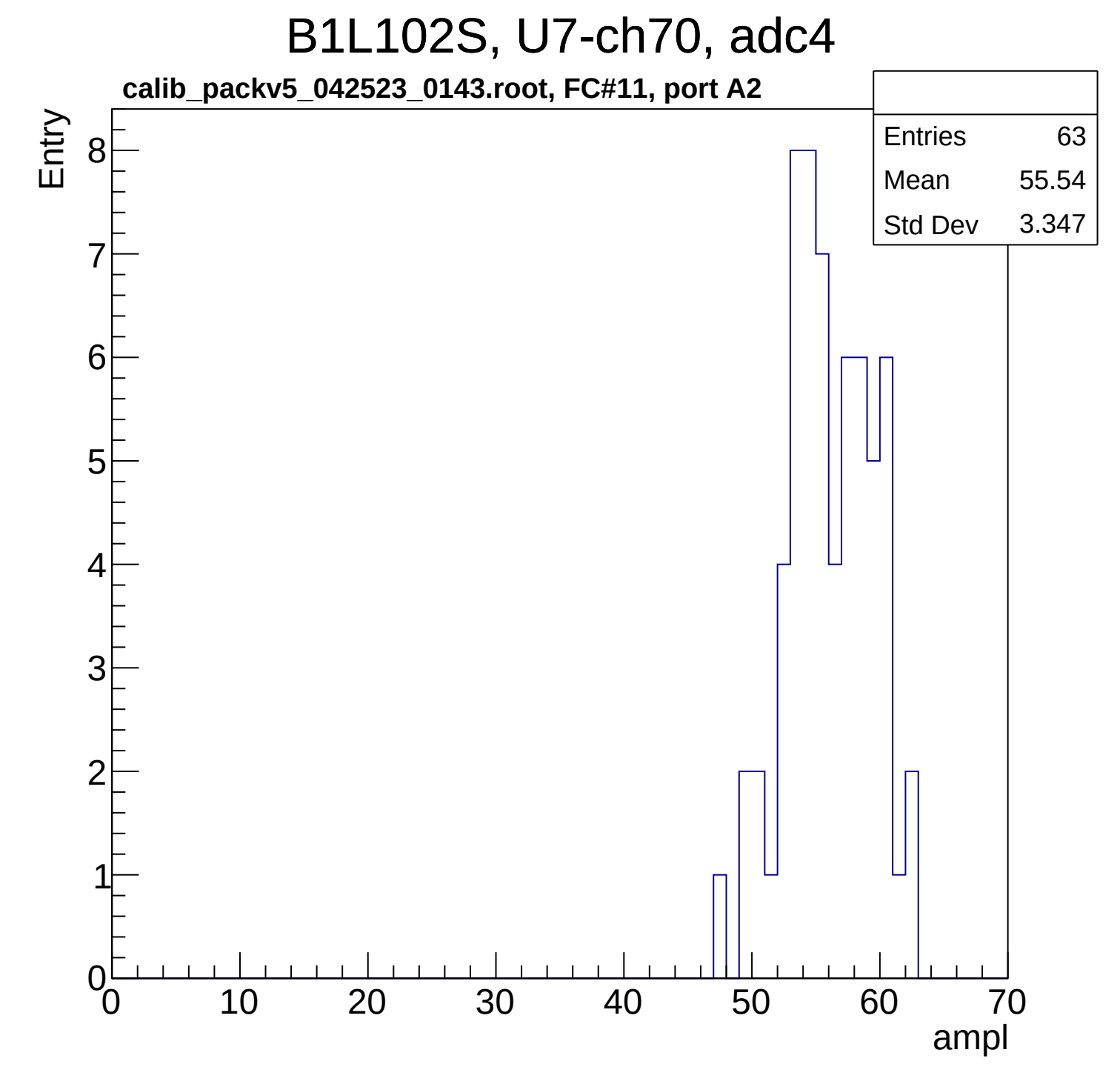

B1L102S, U7-ch70, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 42
Mean 50.1
Std Dev 3.176
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L102S, U7-ch70, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 63
Mean 55.54
Std Dev 3.347
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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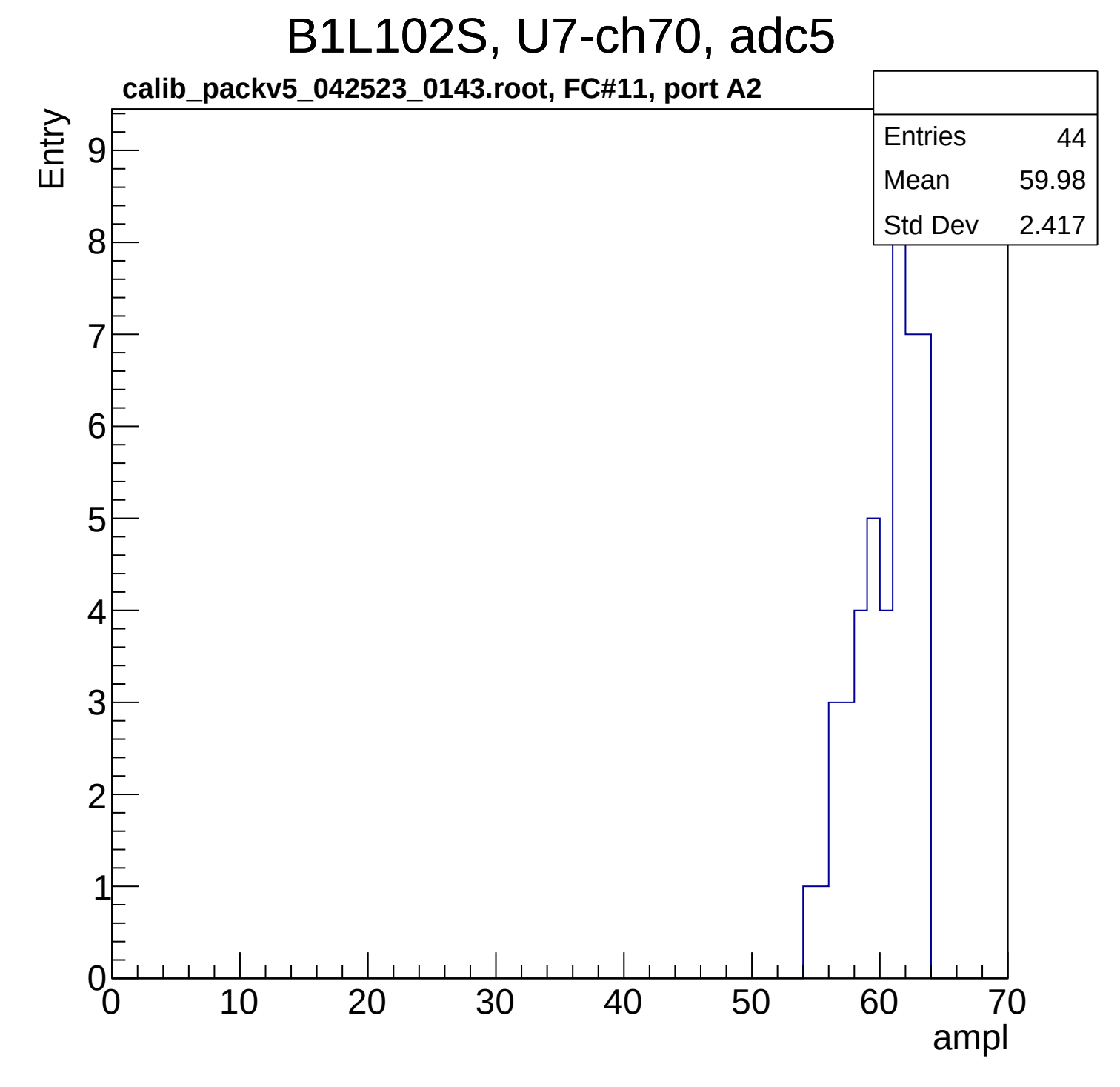
B1L102S, U7-ch70, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 44
Mean 59.98
Std Dev 2.417
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
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20
30
40
50
60
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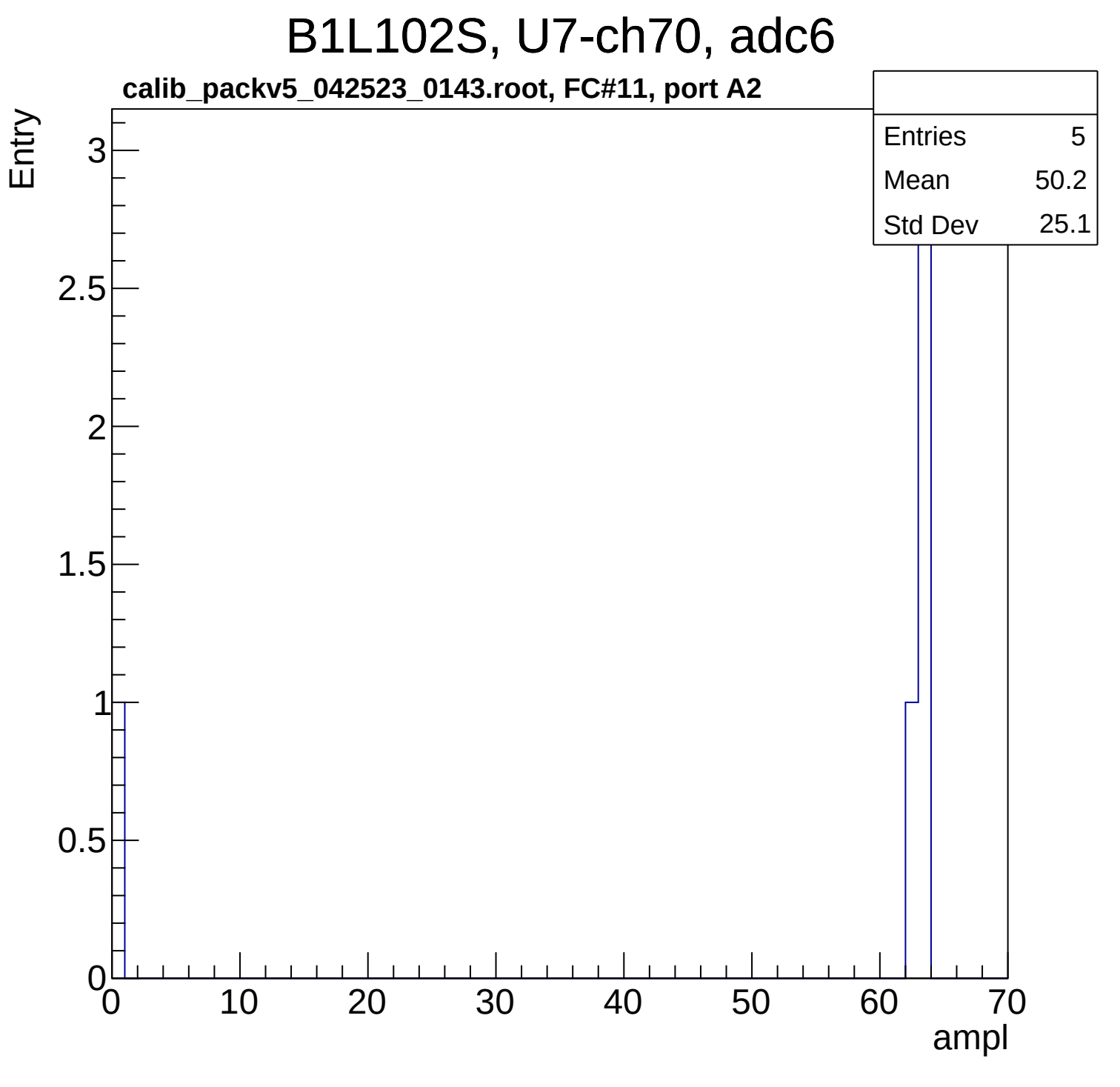
B1L102S, U7-ch70, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 5
Mean 50.2
Std Dev 25.1
Entry
ampl
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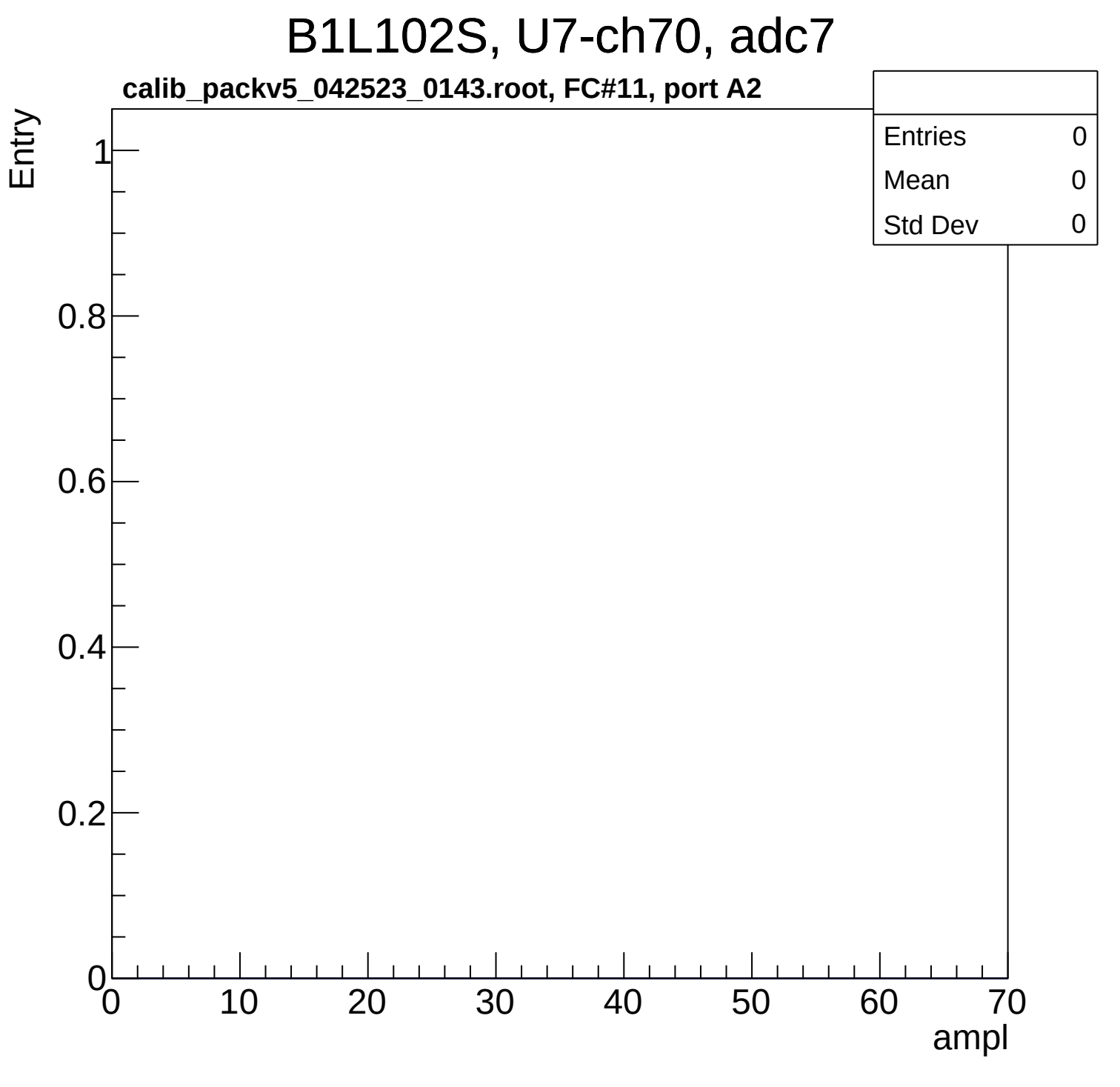
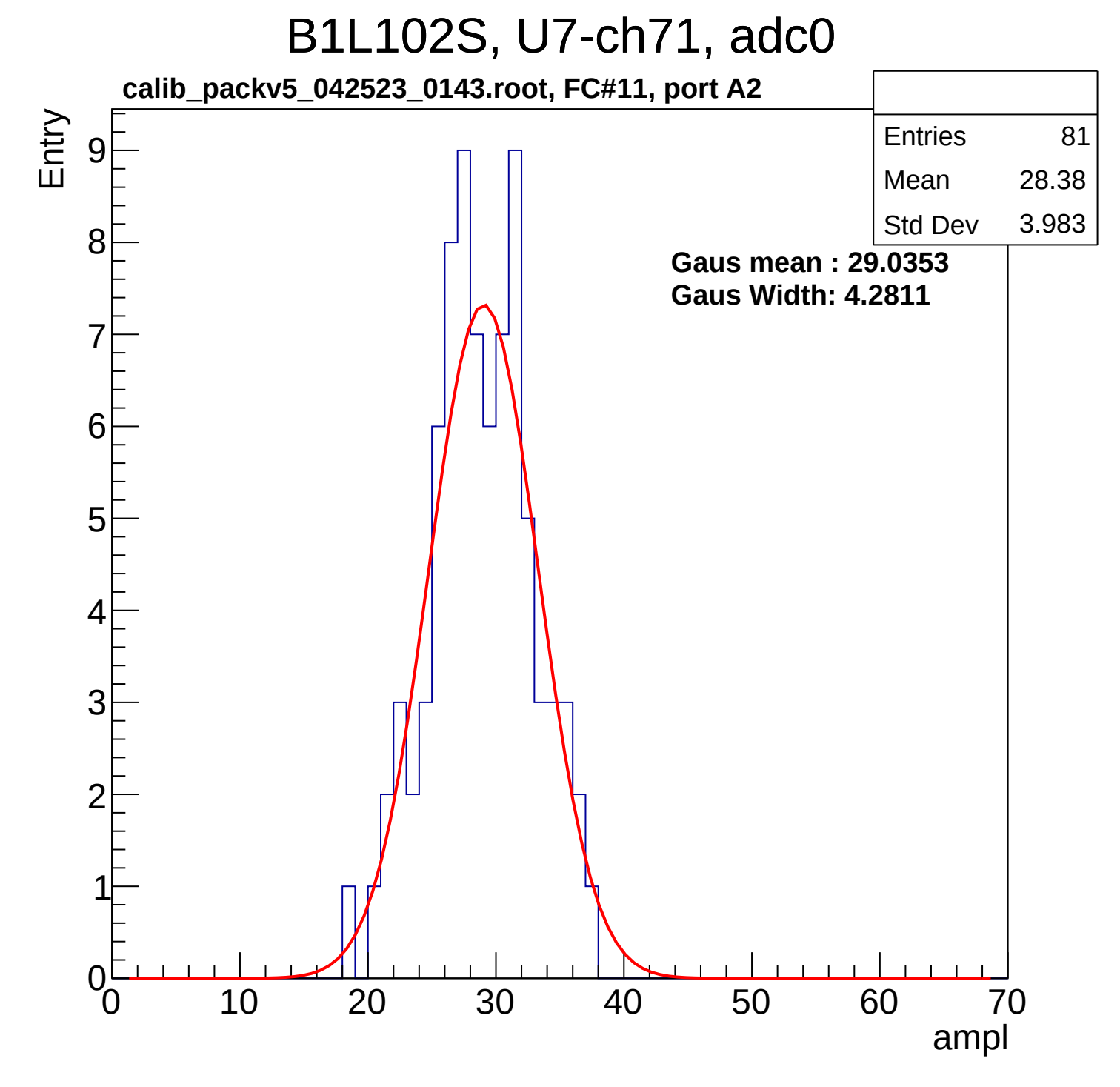
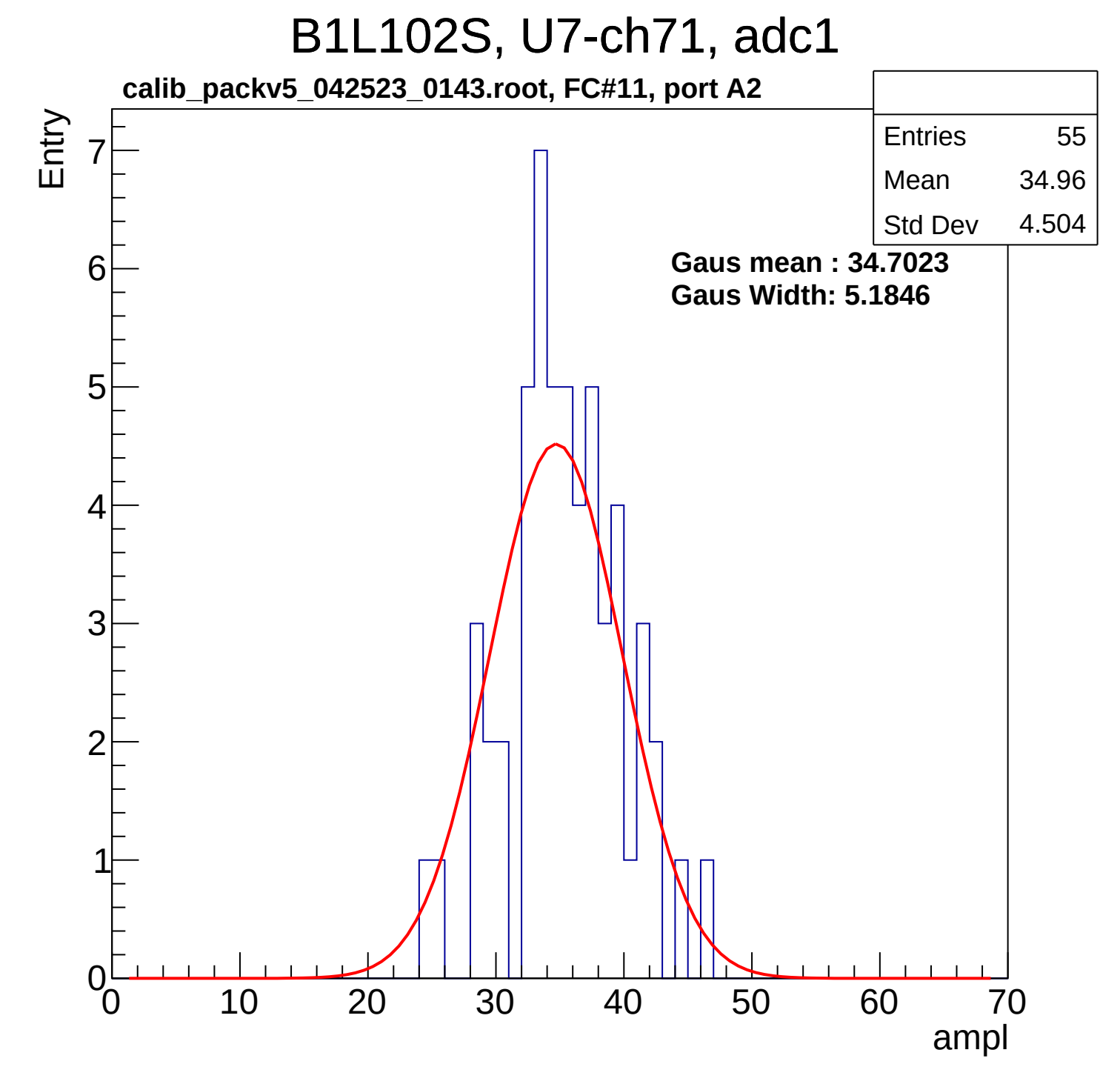
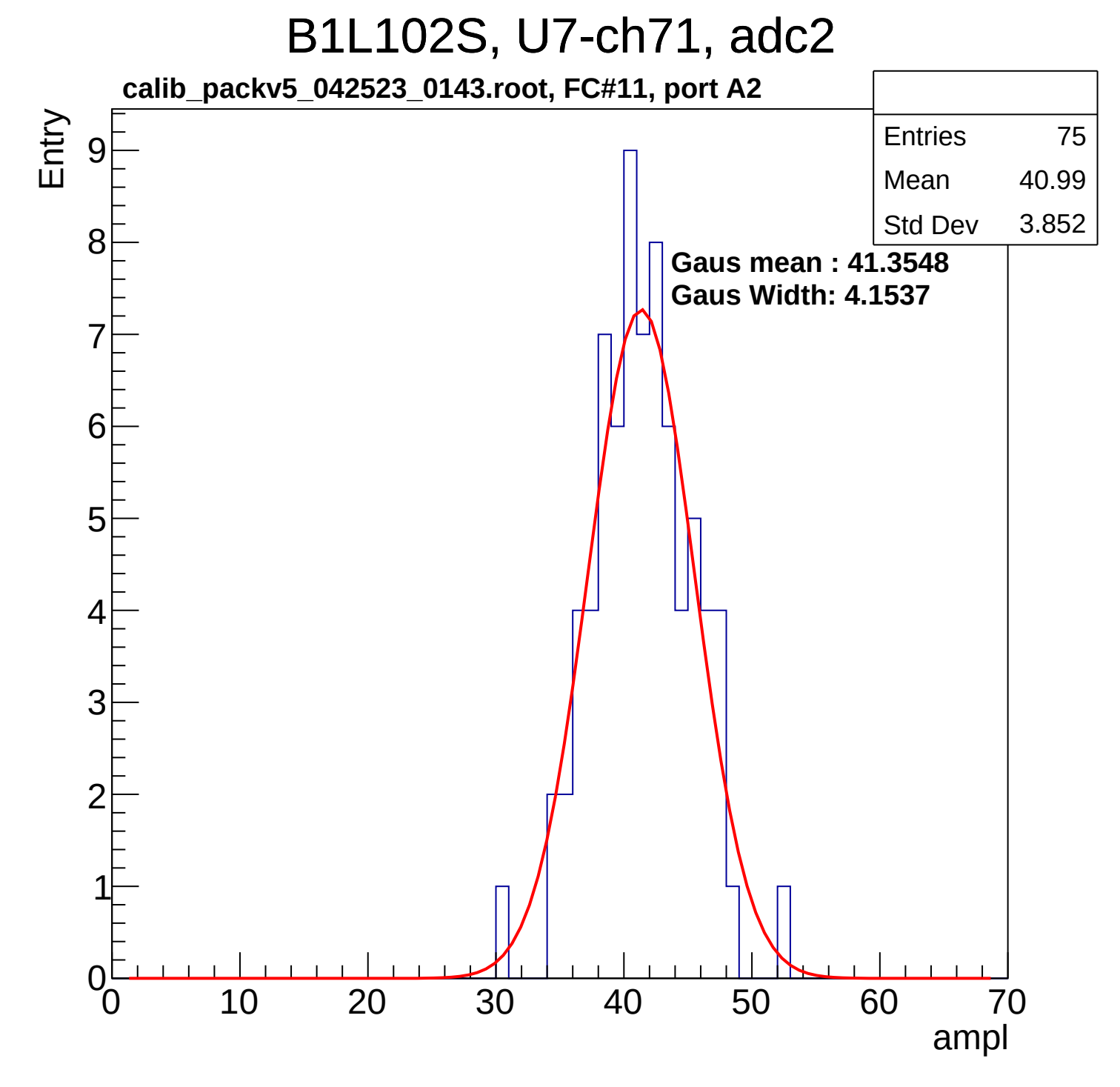
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L102S, U7-ch70, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U7-ch71, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 81
Mean 28.38
Std Dev 3.983
Gaus mean : 29.0353
Gaus Width: 4.2811
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L102S, U7-ch71, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 55
Mean 34.96
Std Dev 4.504
Gaus mean : 34.7023
Gaus Width: 5.1846
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L102S, U7-ch71, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 75
Mean 40.99
Std Dev 3.852
Gaus mean : 41.3548
Gaus Width: 4.1537
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
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40
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60
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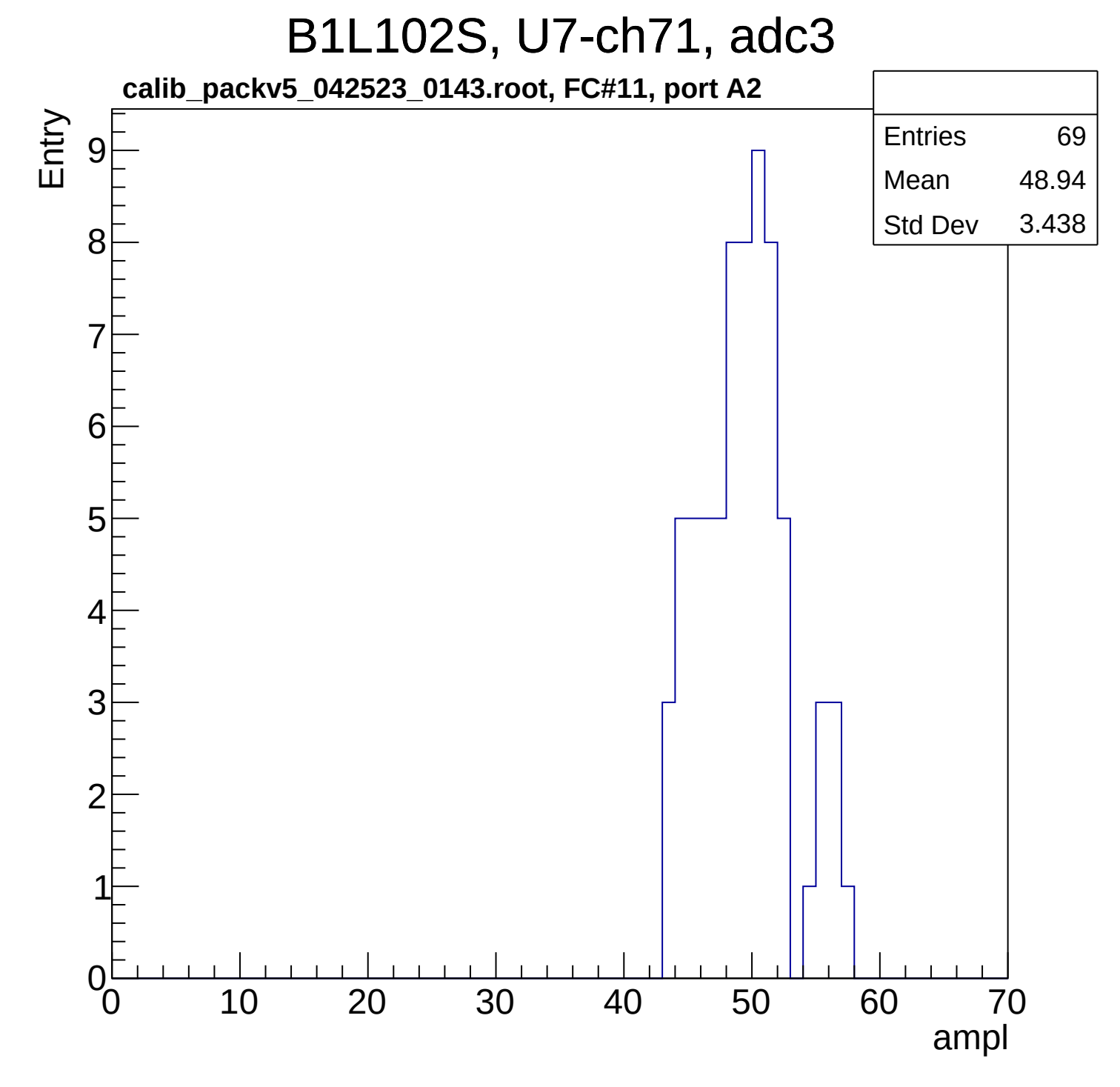
B1L102S, U7-ch71, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 69
Mean 48.94
Std Dev 3.438
Entry
ampl
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1
2
3
4
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6
7
8
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0
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60
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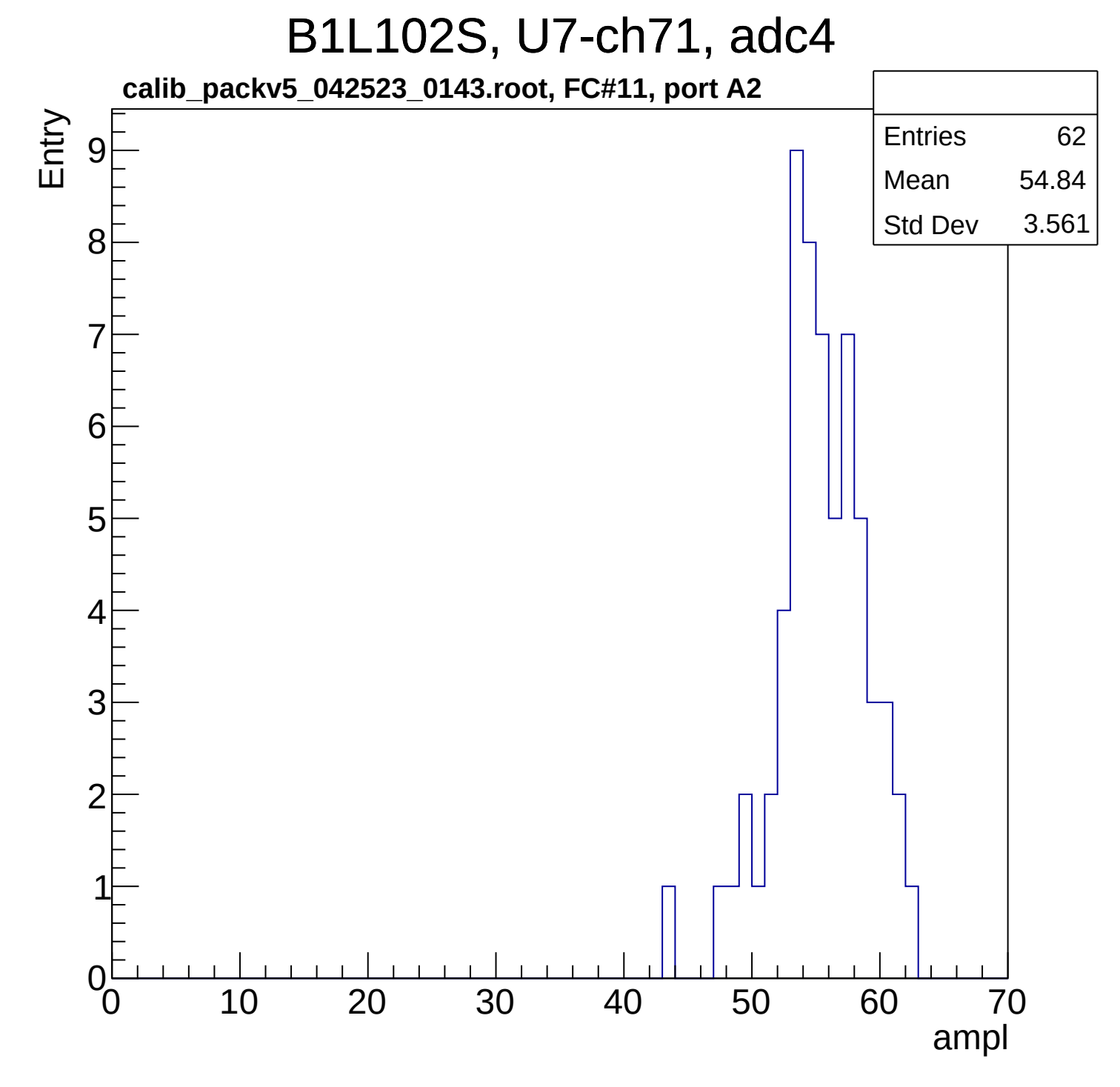
B1L102S, U7-ch71, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 62
Mean 54.84
Std Dev 3.561
Entry
ampl
0
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2
3
4
5
6
7
8
9
0
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20
30
40
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60
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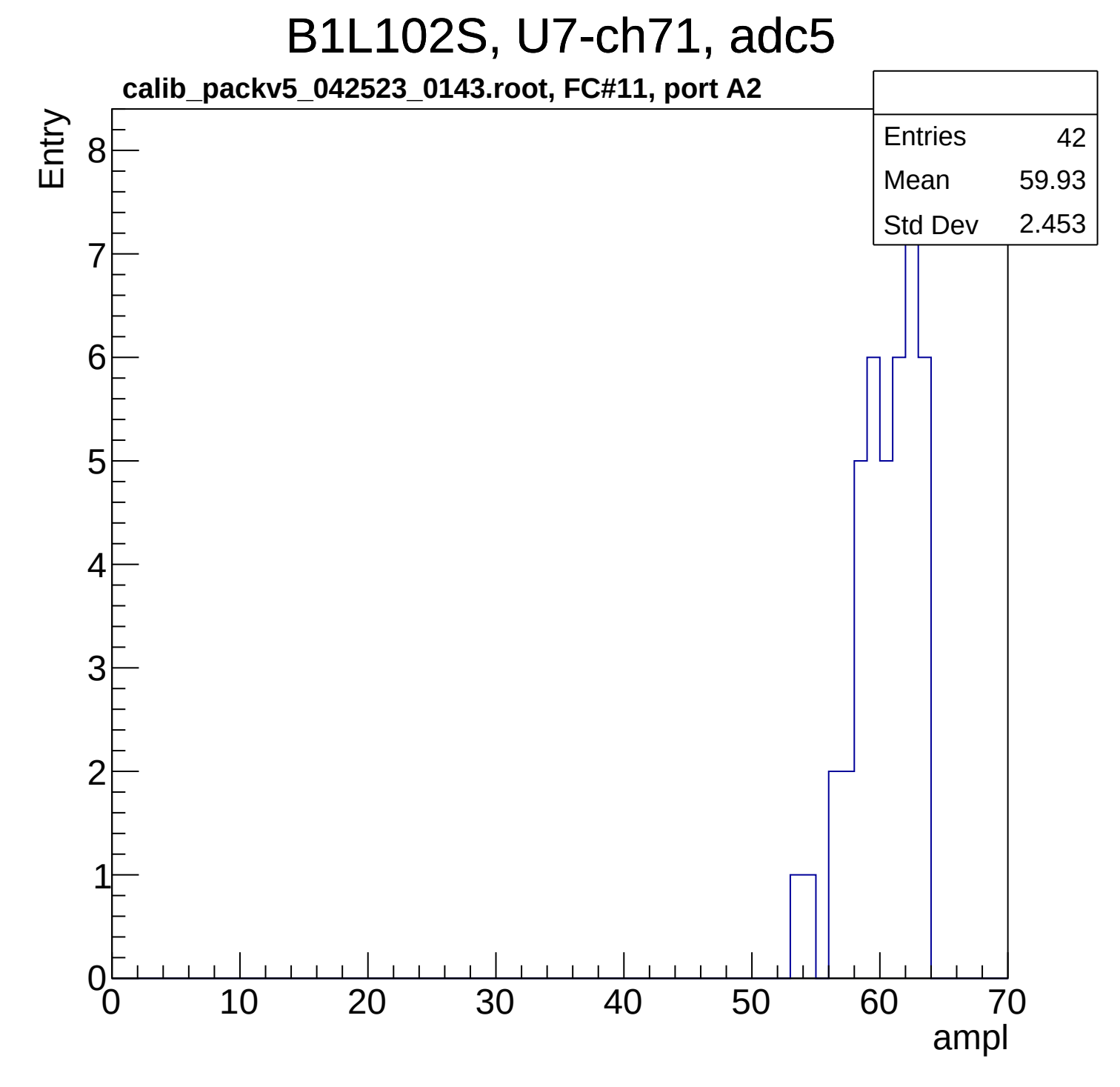
B1L102S, U7-ch71, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 42
Mean 59.93
Std Dev 2.453
Entry
ampl
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1
2
3
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5
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0
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60
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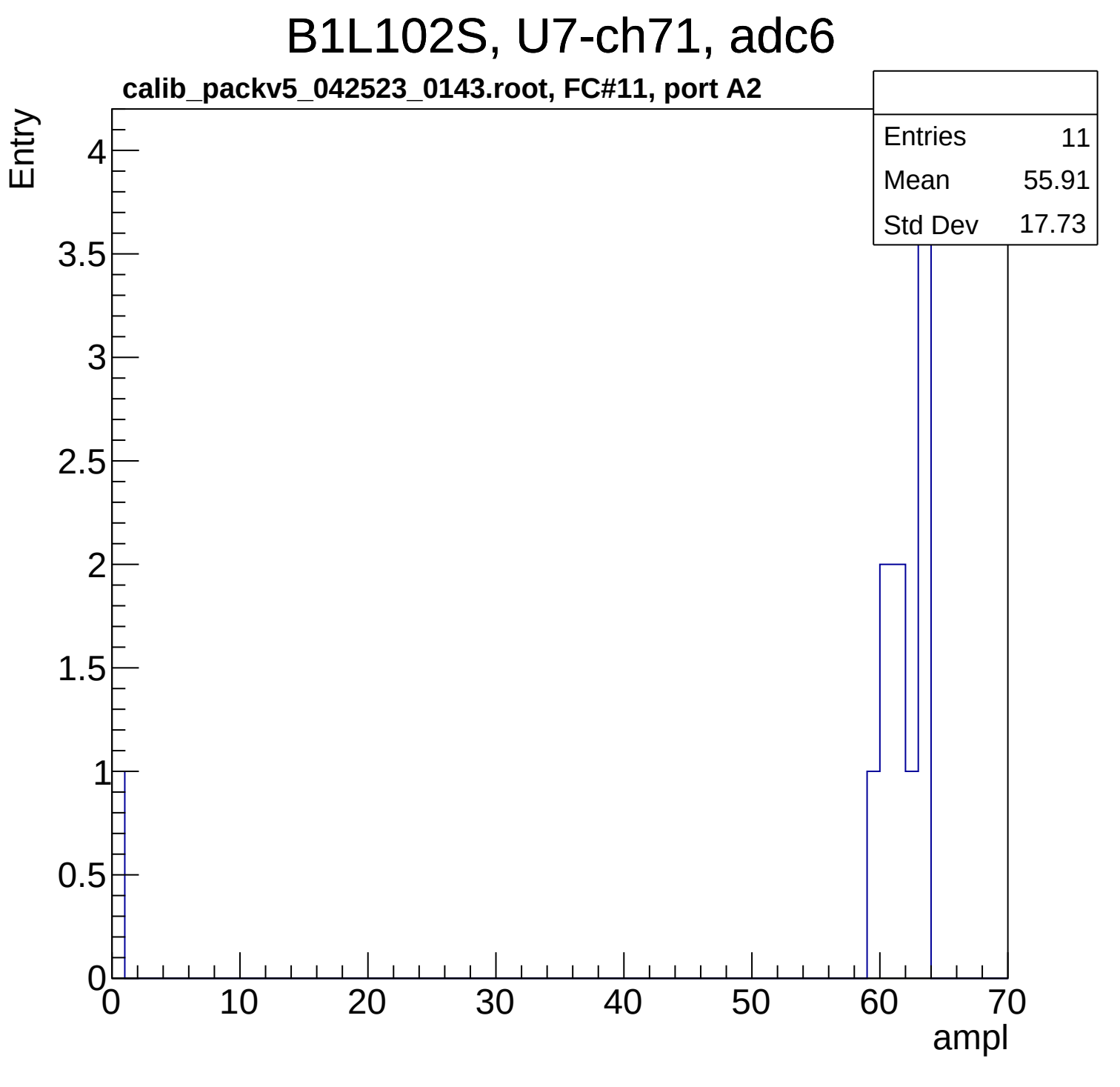
B1L102S, U7-ch71, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 11
Mean 55.91
Std Dev 17.73
Entry
ampl
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0.5
1
1.5
2
2.5
3
3.5
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0
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60
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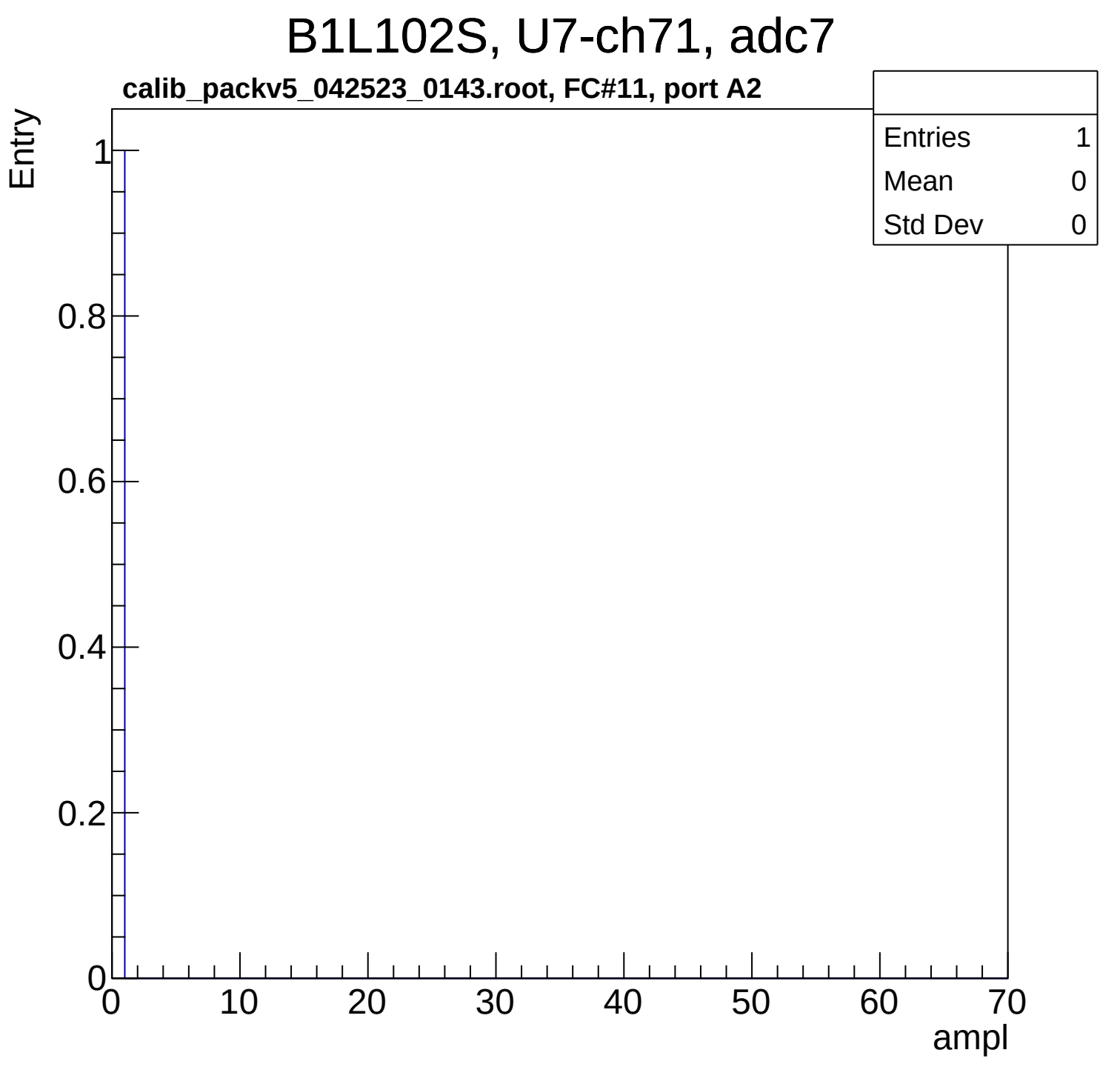
B1L102S, U7-ch71, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
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30
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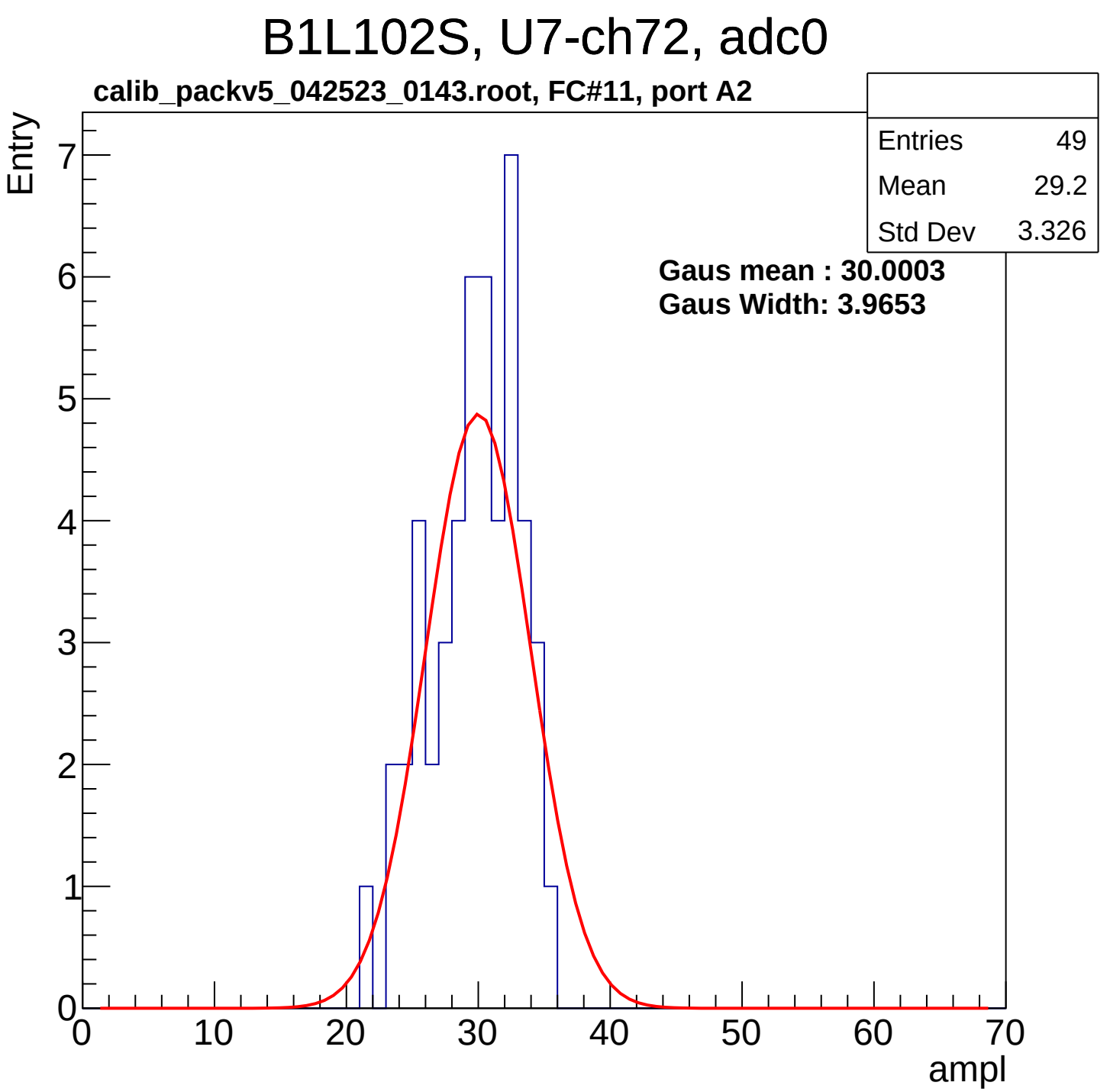
50
60
70
ampl


B1L102S, U7-ch72, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 49
Mean 29.2
Std Dev 3.326
Gaus mean : 30.0003
Gaus Width: 3.9653
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
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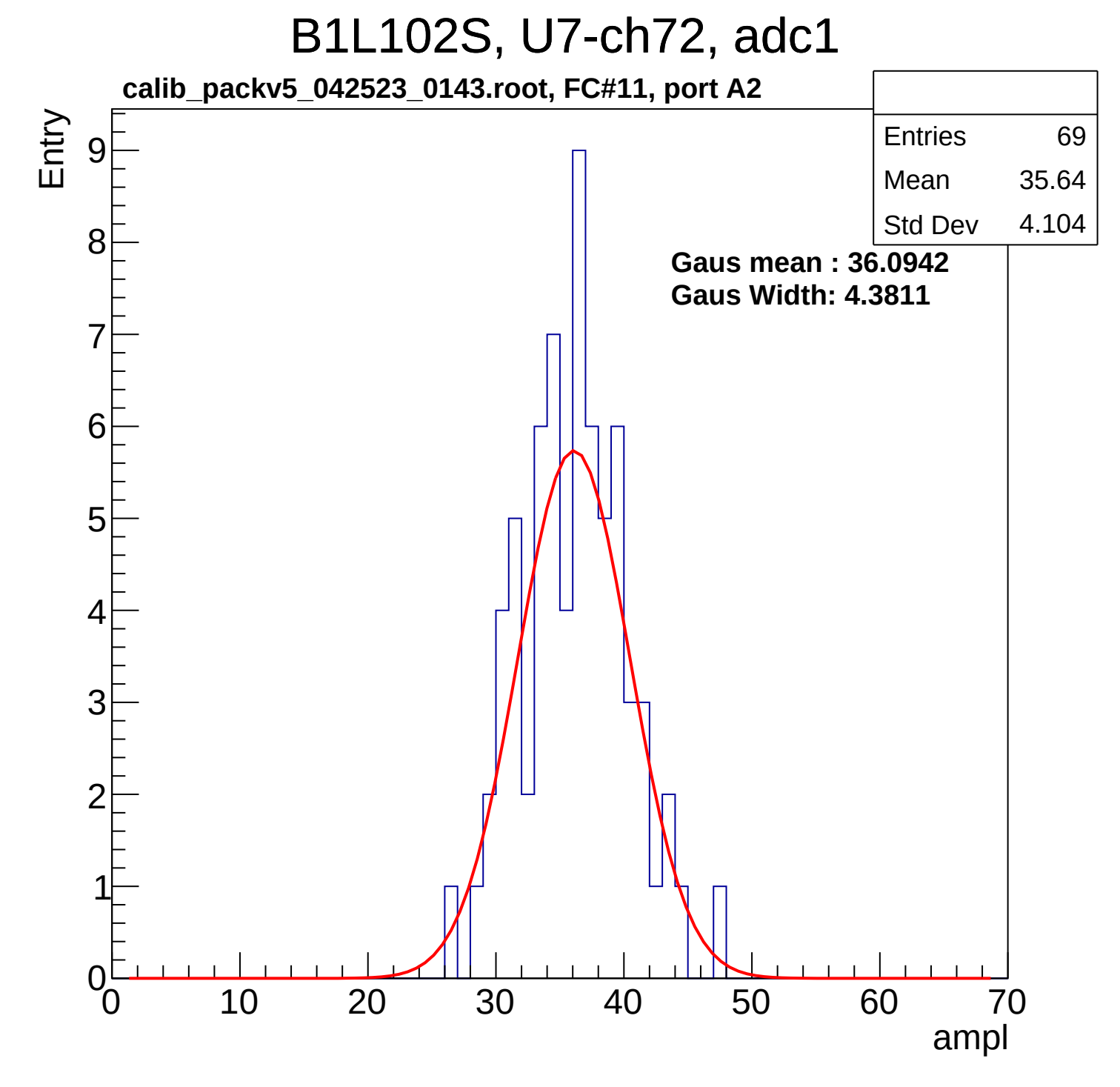
40
50
60
70


B1L102S, U7-ch72, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 69
Mean 35.64
Std Dev 4.104
Gaus mean : 36.0942
Gaus Width: 4.3811
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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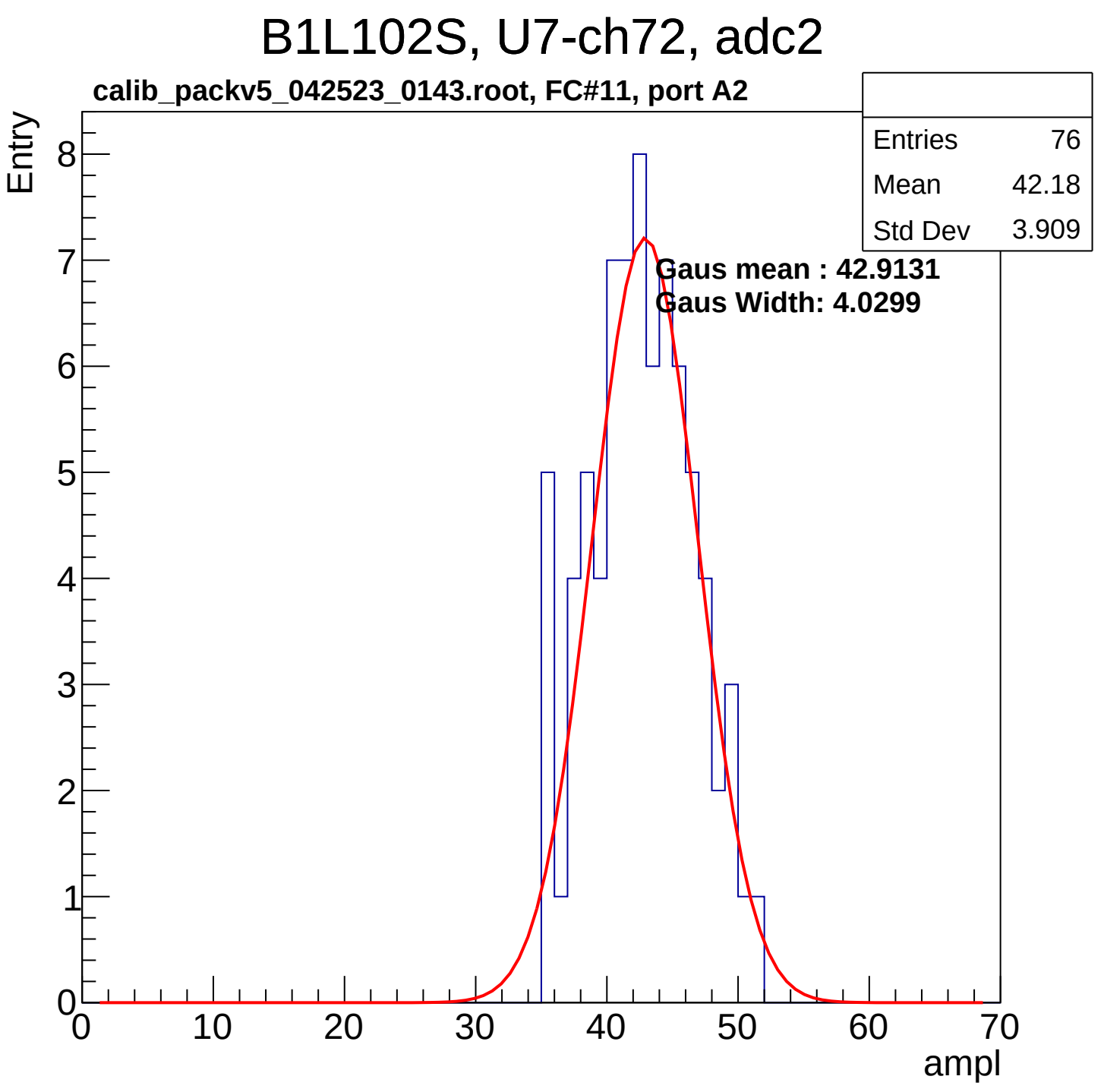
B1L102S, U7-ch72, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 76
Mean 42.18
Std Dev 3.909
Gaus mean : 42.9131
Gaus Width: 4.0299
Entry
ampl
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1
2
3
4
5
6
7
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0
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20
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60
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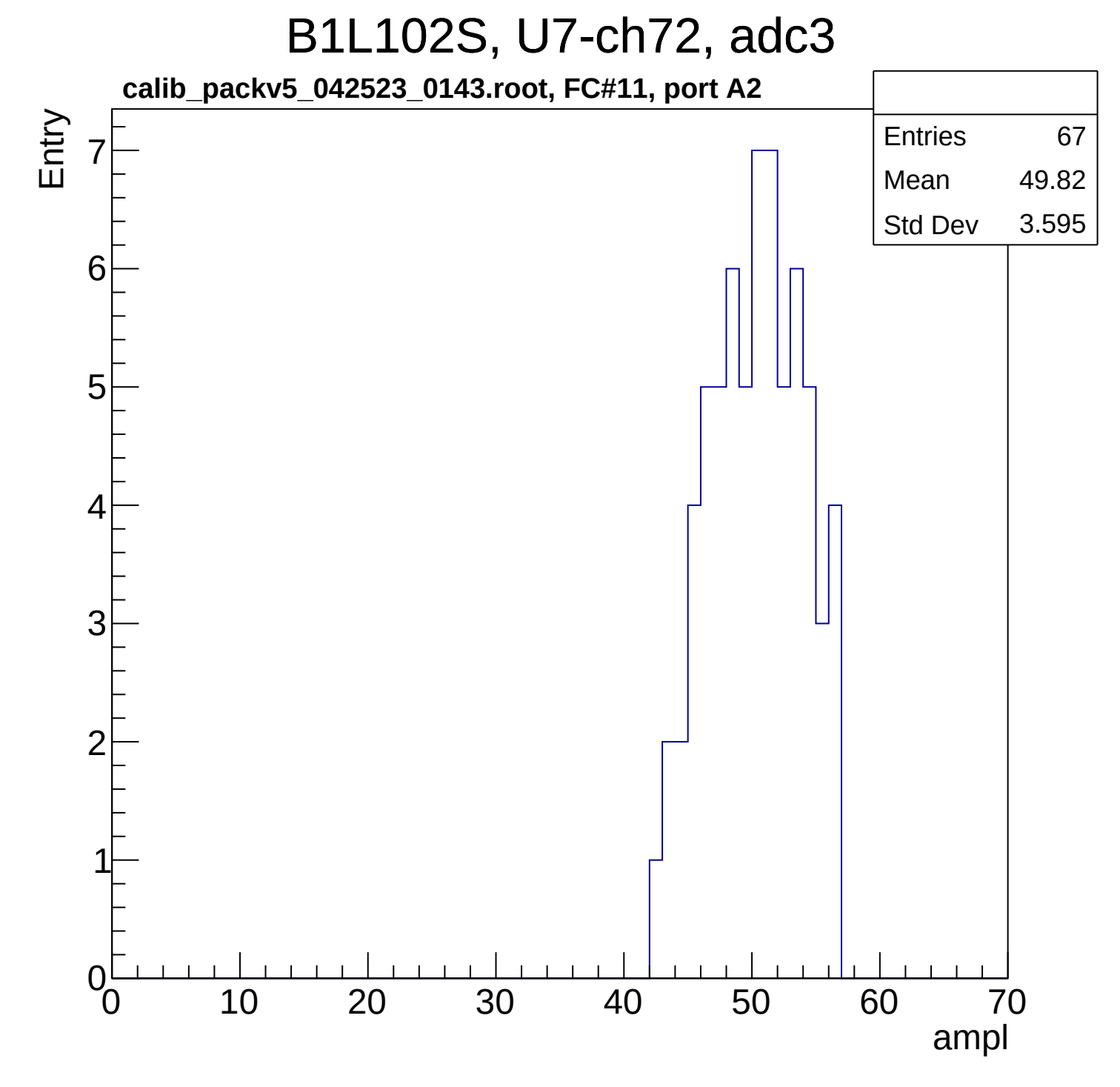
B1L102S, U7-ch72, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 67
Mean 49.82
Std Dev 3.595
Entry
ampl
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3
4
5
6
7
0
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20
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40
50
60
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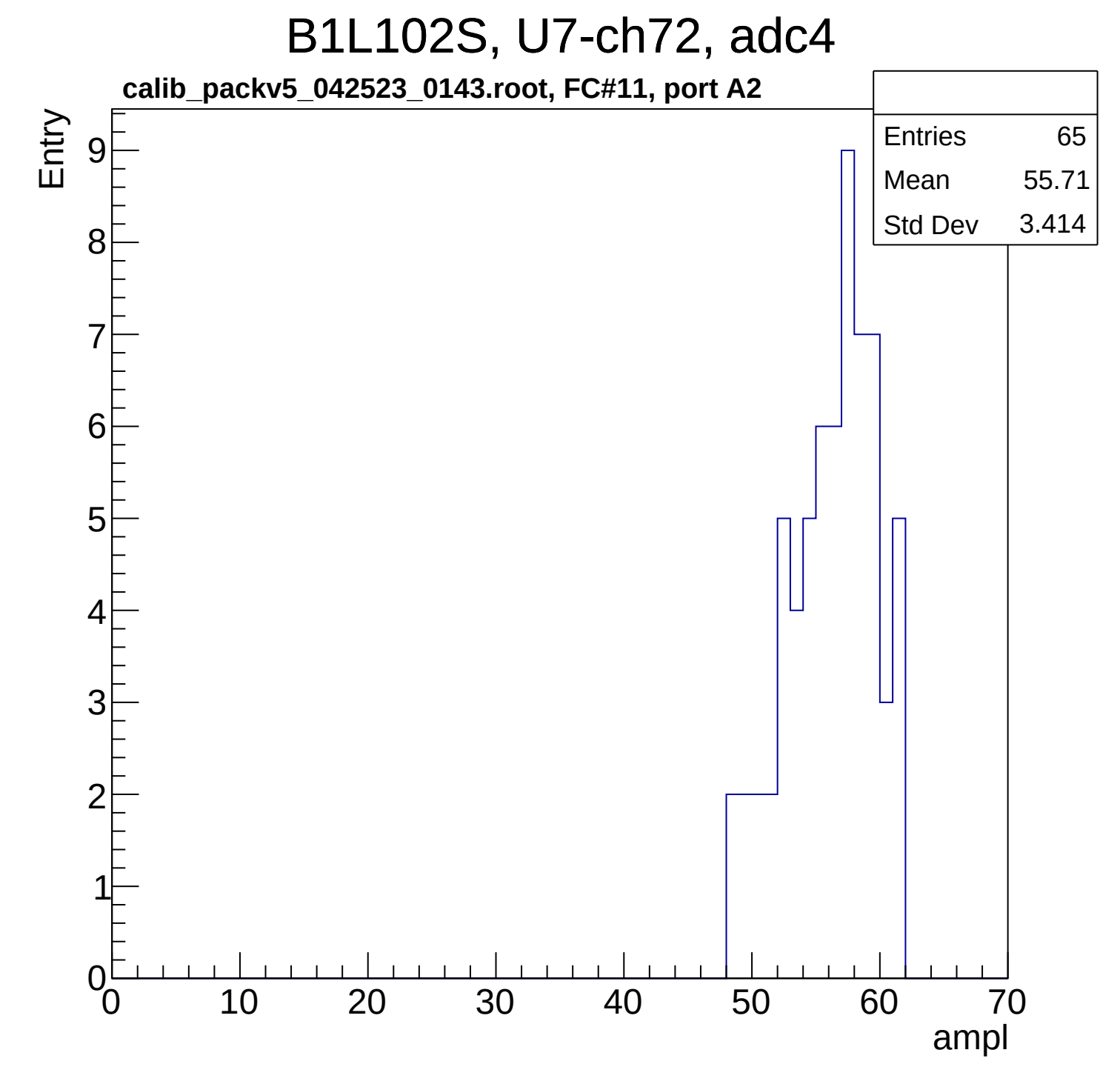
B1L102S, U7-ch72, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 65
Mean 55.71
Std Dev 3.414
Entry
ampl
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2
3
4
5
6
7
8
9
0
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40
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60
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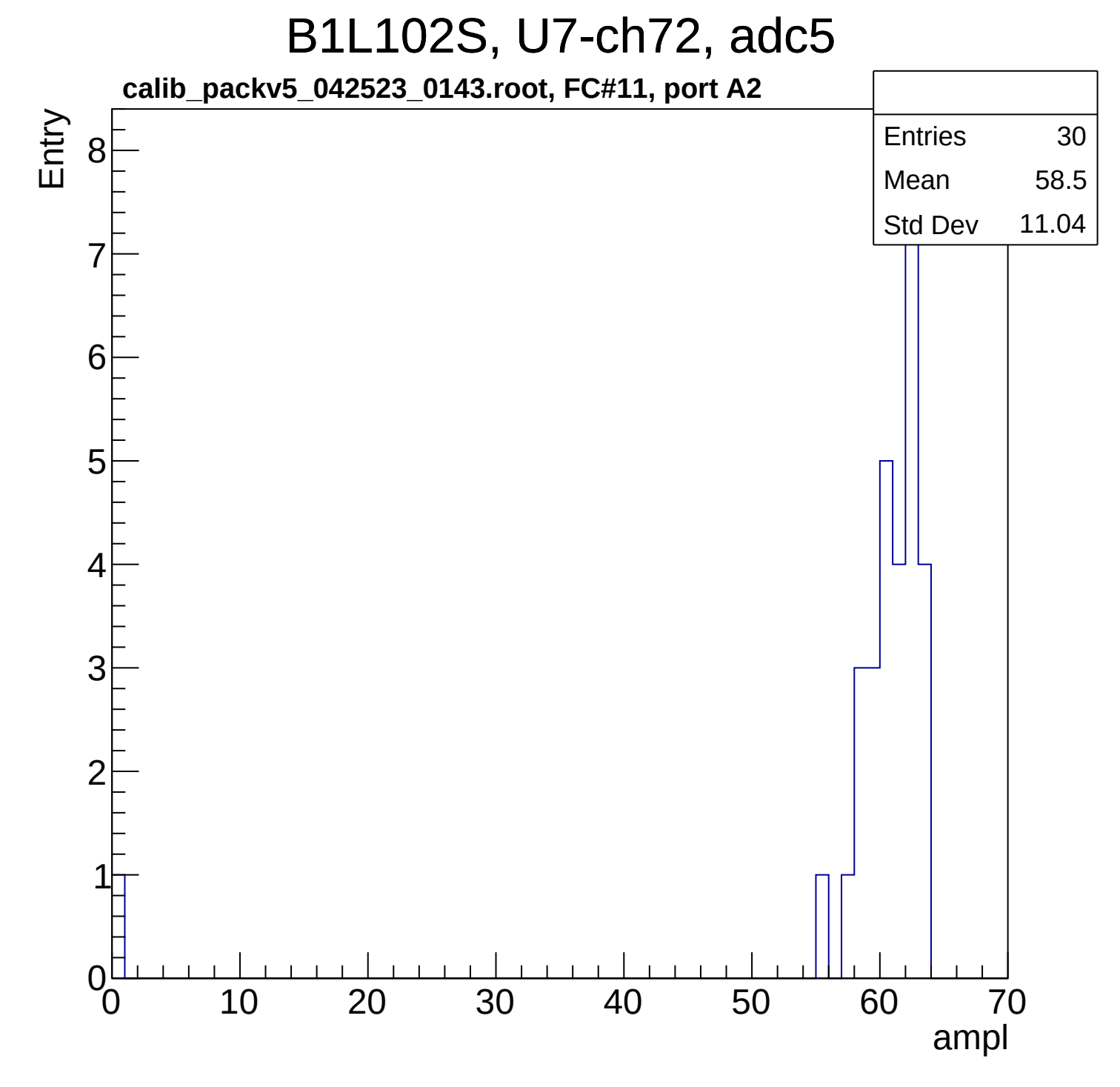
B1L102S, U7-ch72, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 30
Mean 58.5
Std Dev 11.04
Entry
ampl
0
1
2
3
4
5
6
7
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0
10
20
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60
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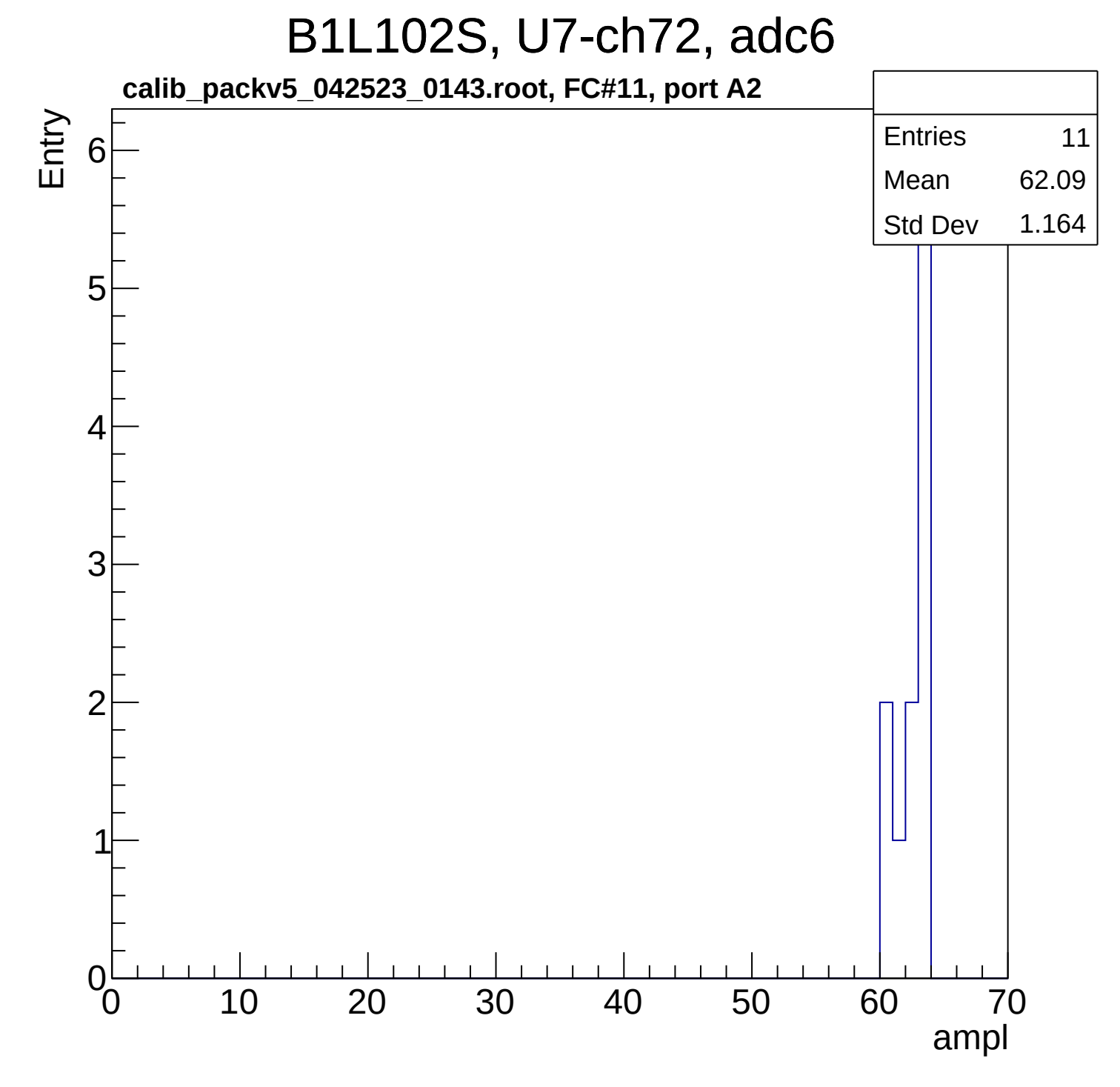
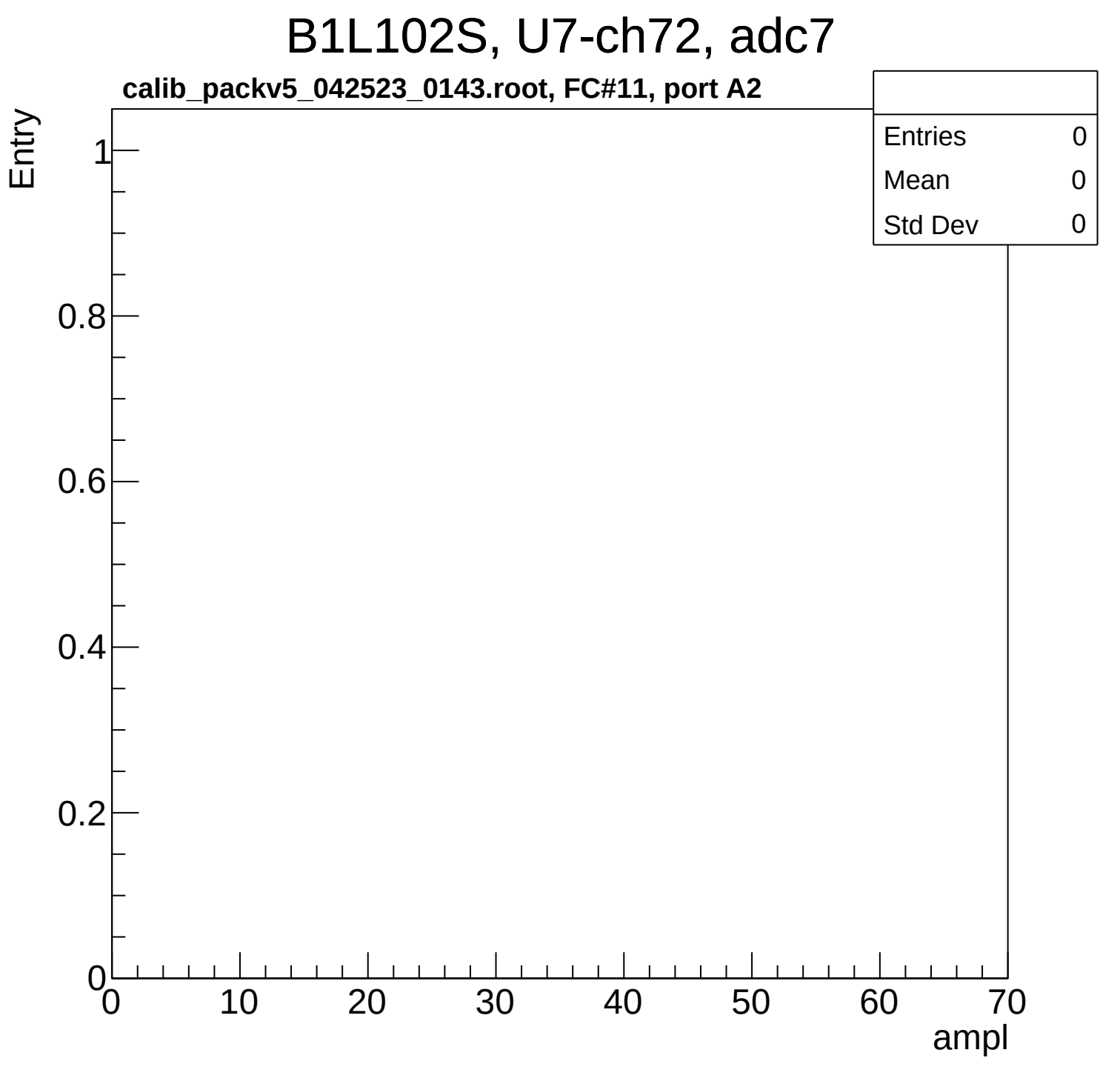

B1L102S, U7-ch72, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 11
Mean 62.09
Std Dev 1.164
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L102S, U7-ch72, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 0
Mean 0
Std Dev 0
Entry
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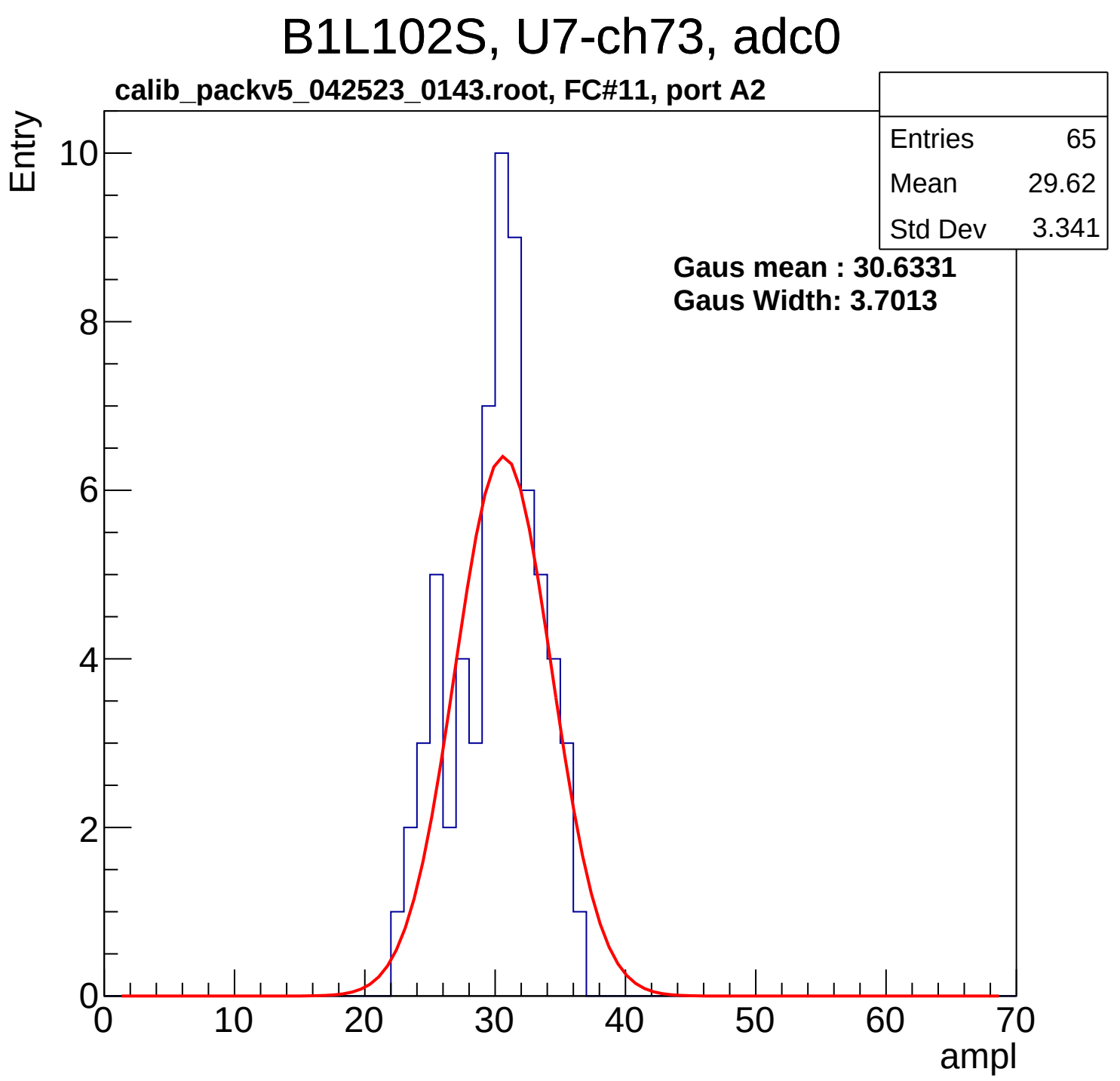
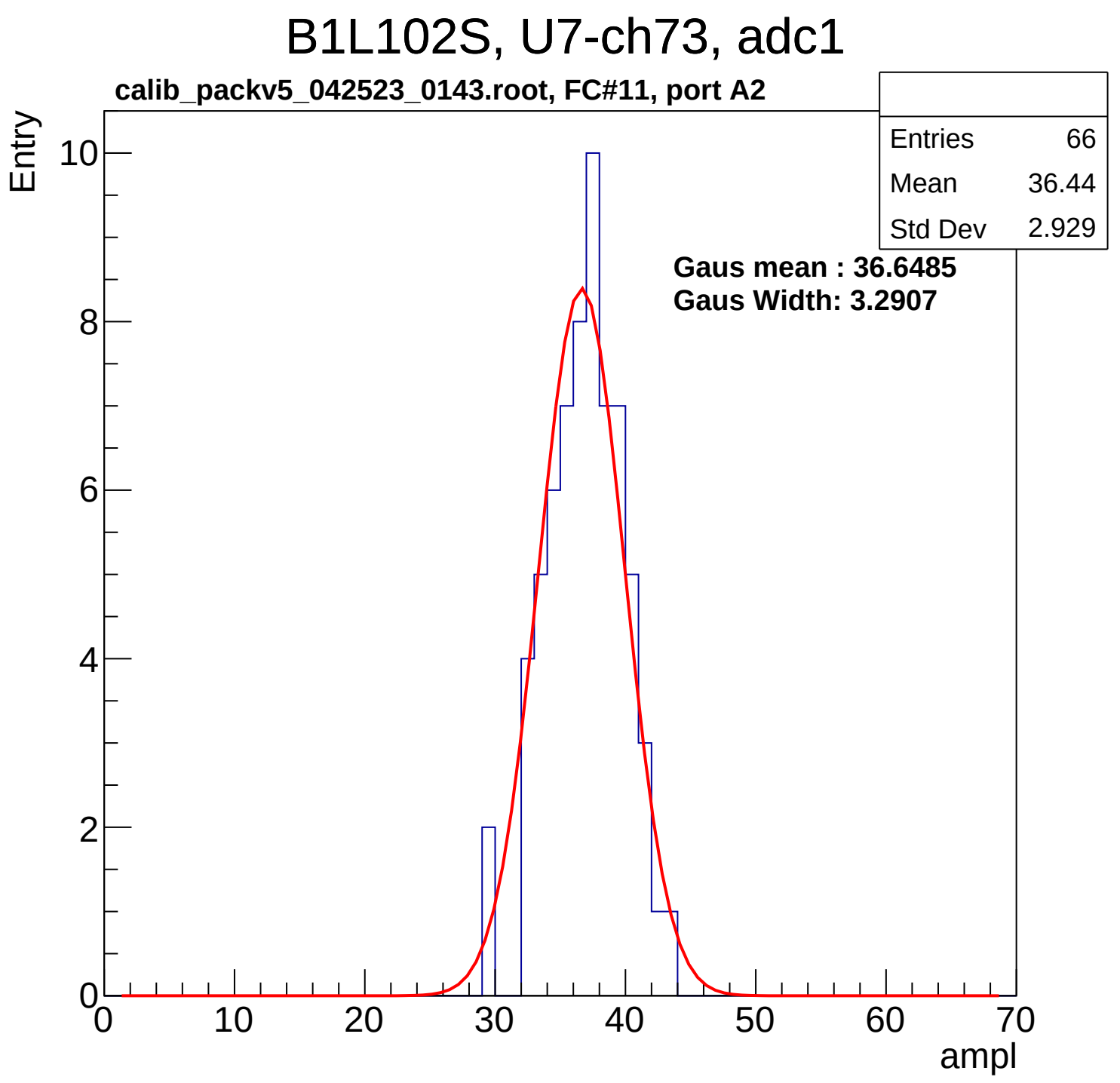
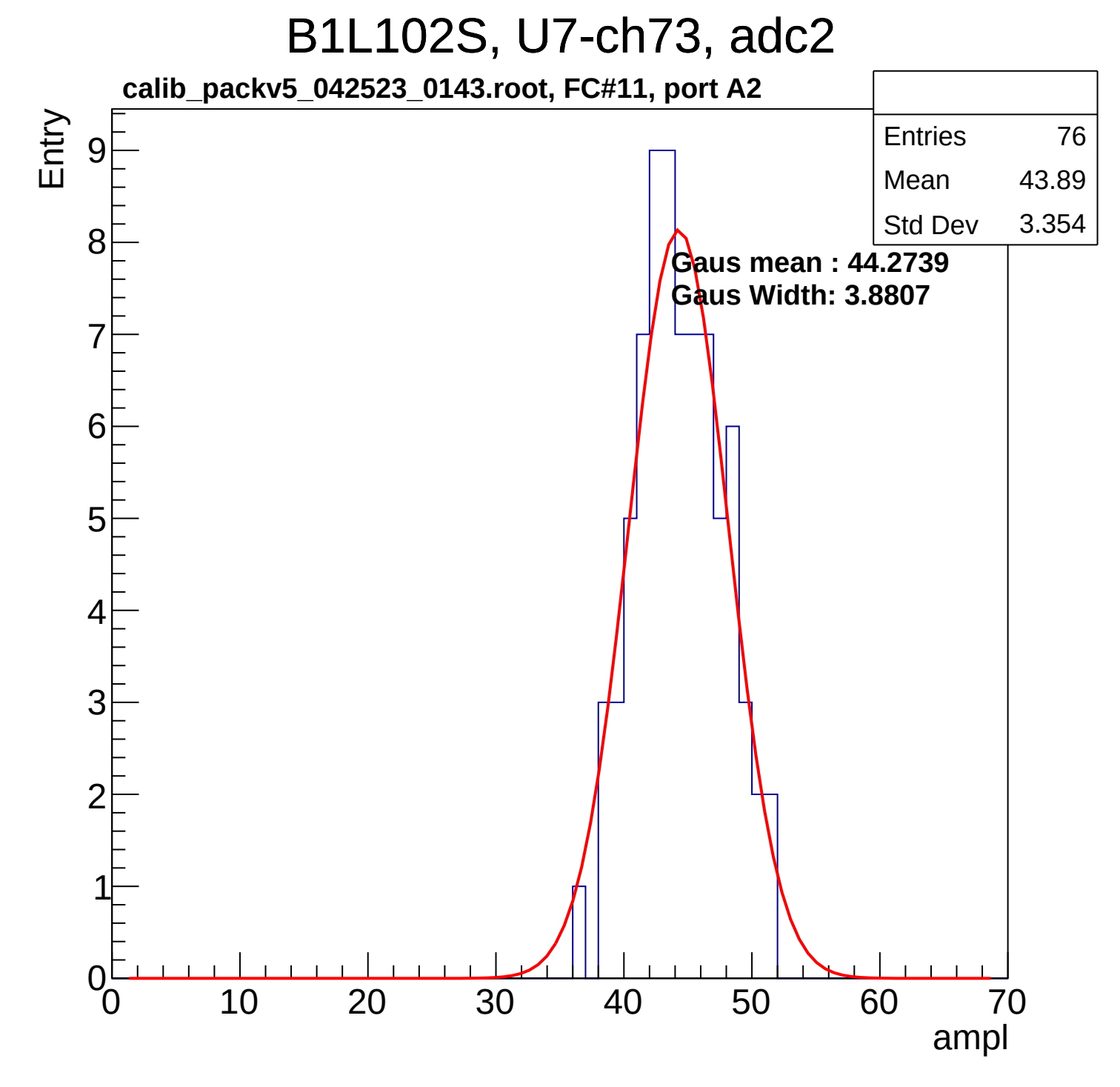
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U7-ch73, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 65
Mean 29.62
Std Dev 3.341
Gaus mean : 30.6331
Gaus Width: 3.7013
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L102S, U7-ch73, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 66
Mean 36.44
Std Dev 2.929
Gaus mean : 36.6485
Gaus Width: 3.2907
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L102S, U7-ch73, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 76
Mean 43.89
Std Dev 3.354
Gaus mean : 44.2739
Gaus Width: 3.8807
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
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40
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60
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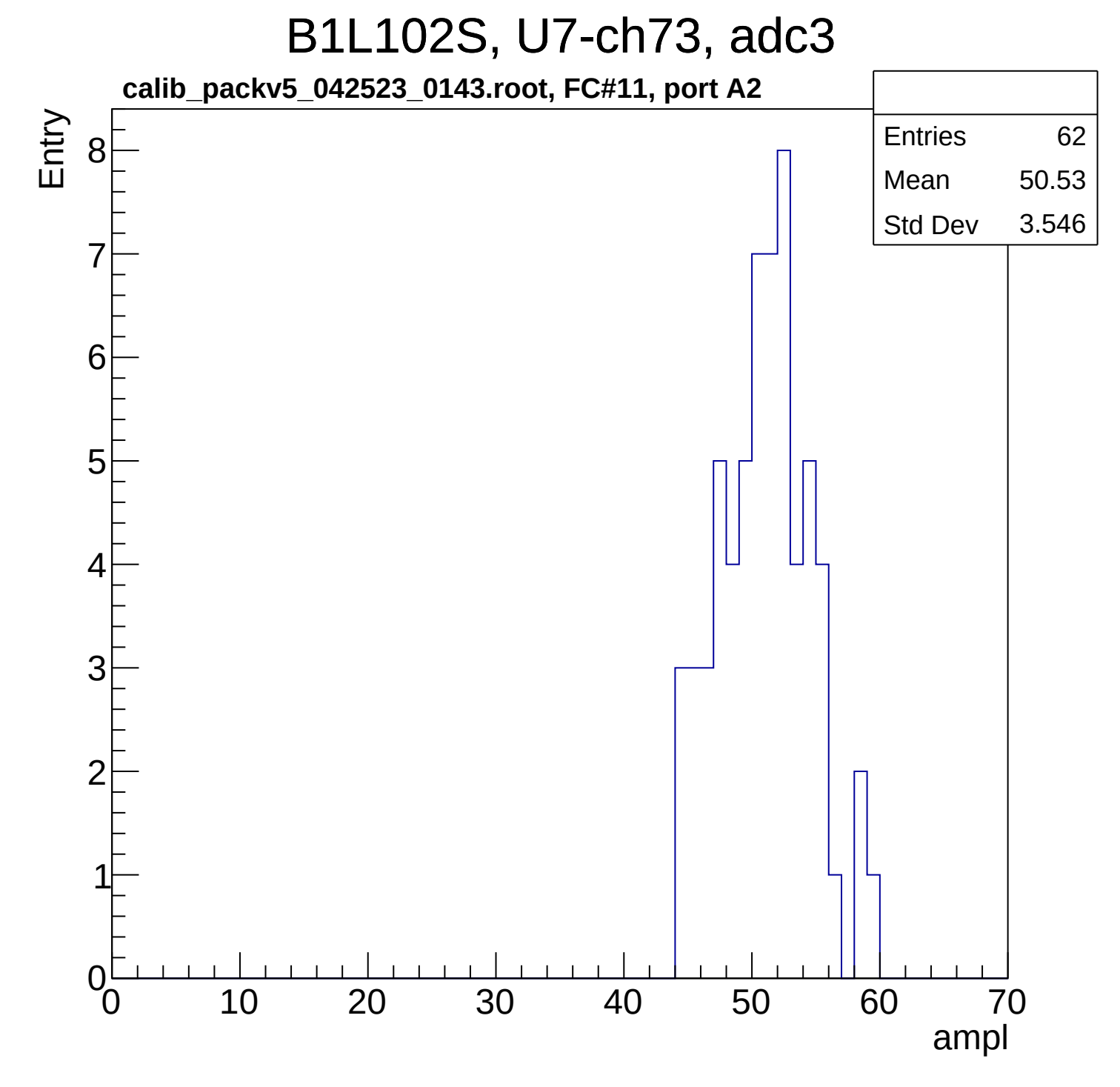
B1L102S, U7-ch73, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 62
Mean 50.53
Std Dev 3.546
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
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40
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60
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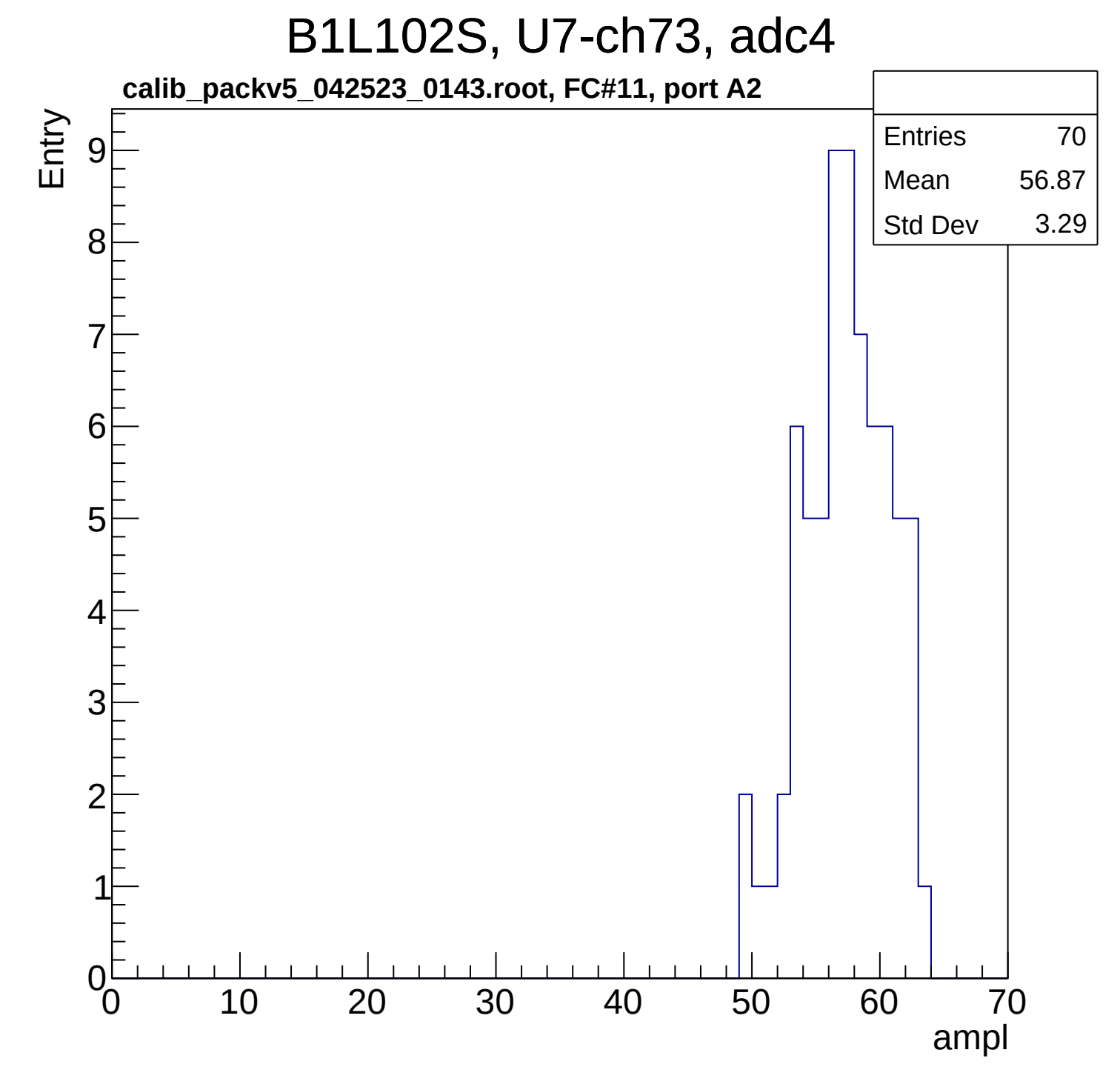
B1L102S, U7-ch73, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 70
Mean 56.87
Std Dev 3.29
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
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30
40
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60
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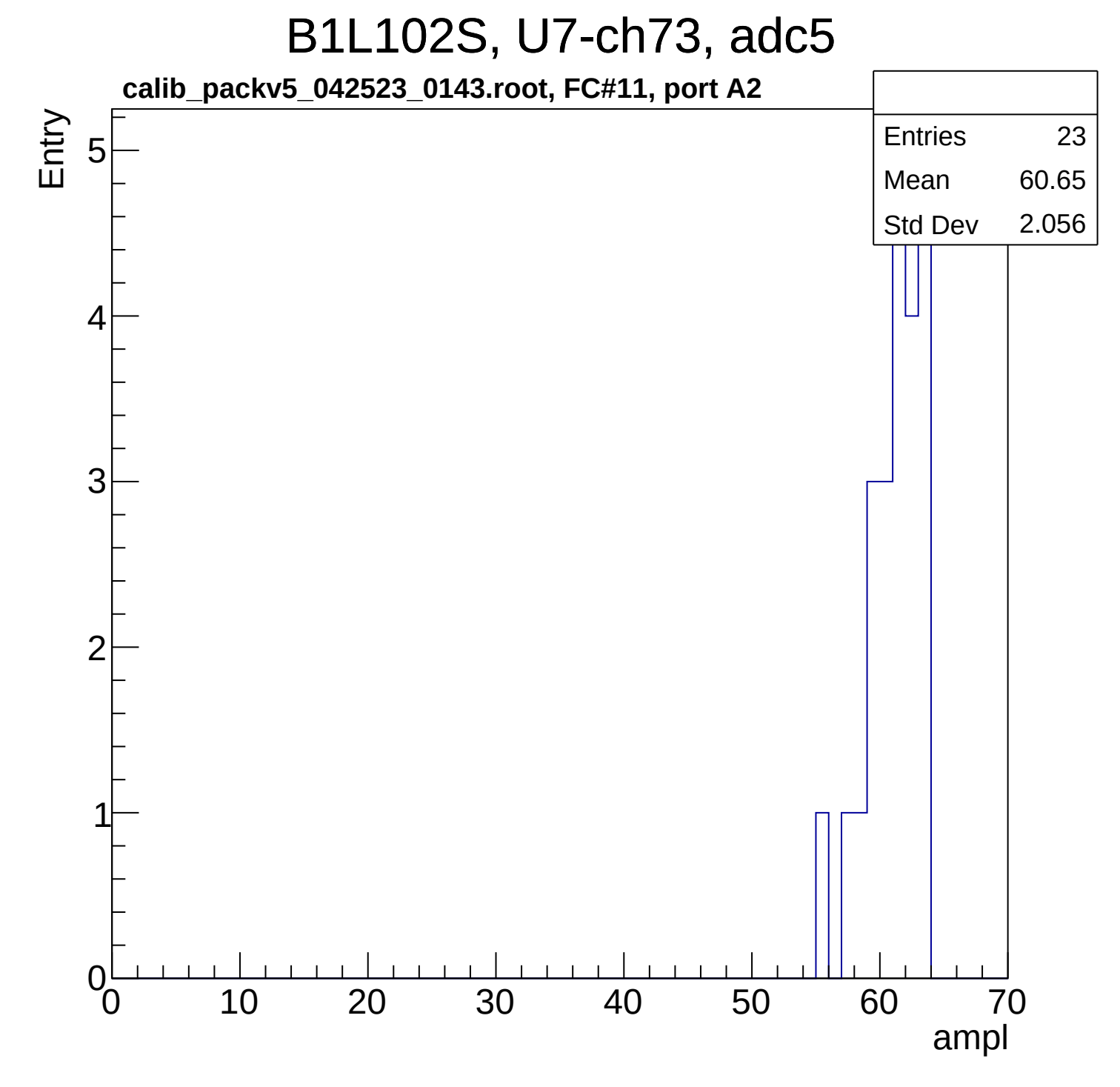
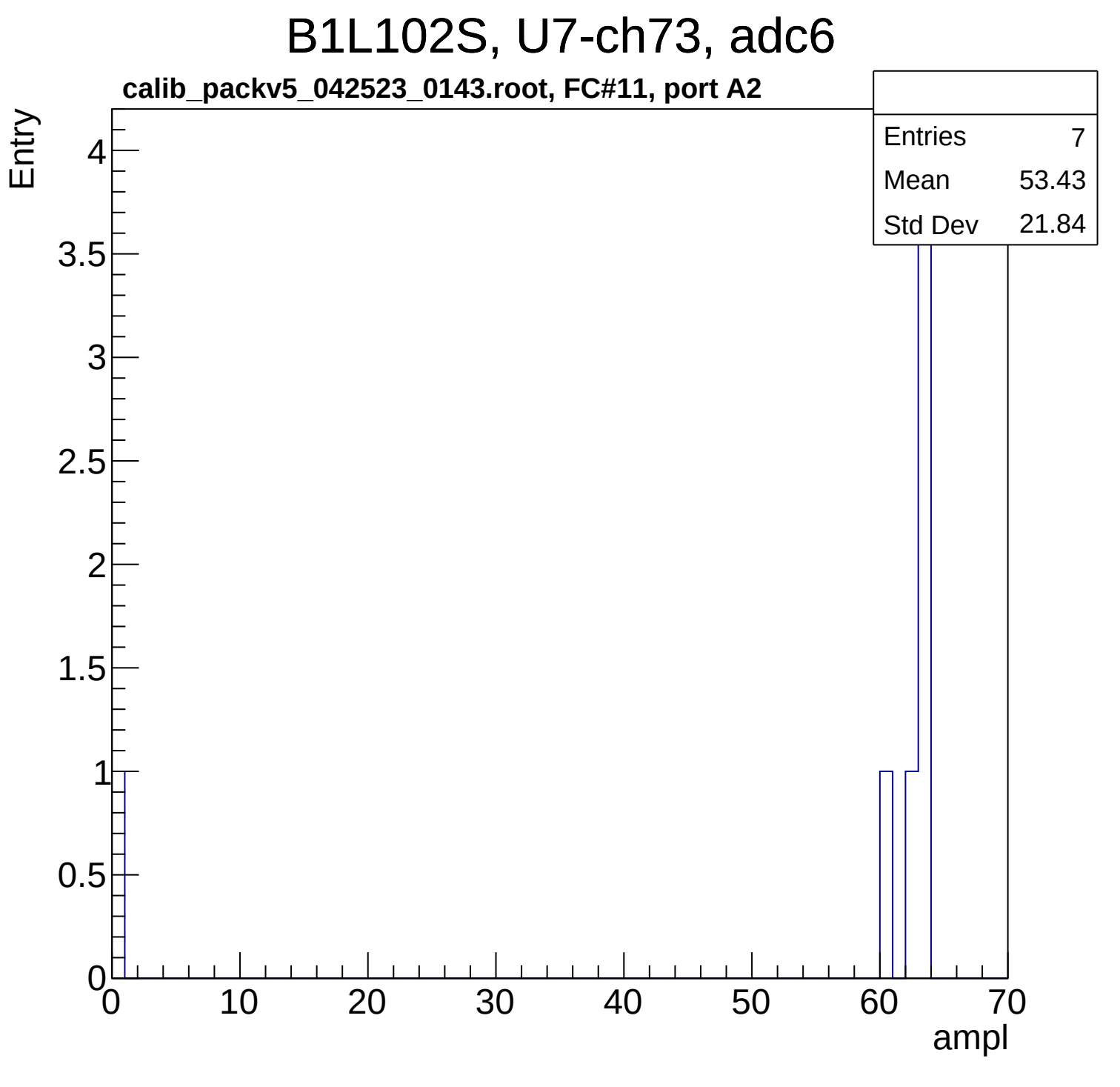

B1L102S, U7-ch73, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 23
Mean 60.65
Std Dev 2.056
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L102S, U7-ch73, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 7
Mean 53.43
Std Dev 21.84
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
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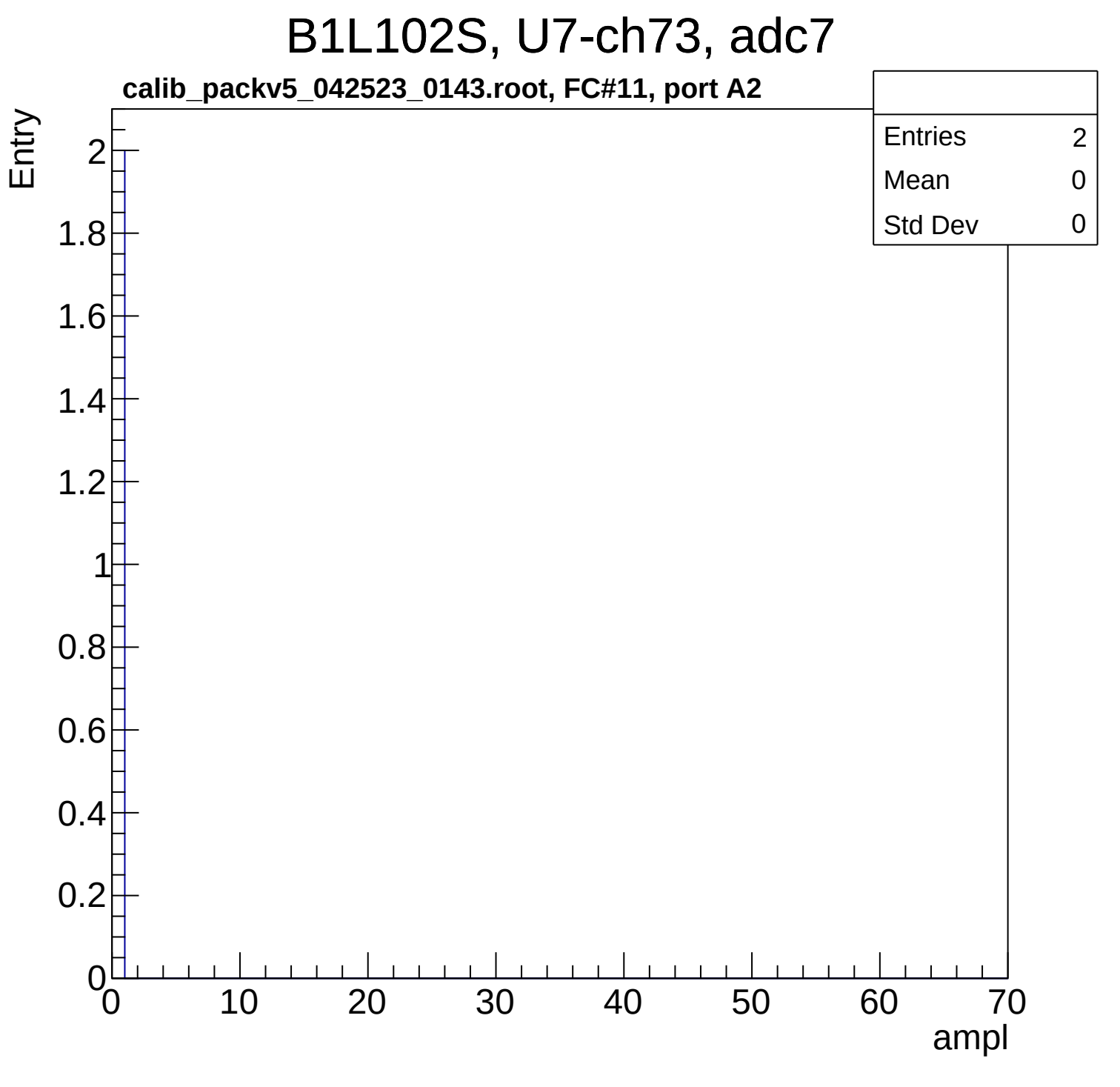
B1L102S, U7-ch73, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 2
Mean 0
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
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60
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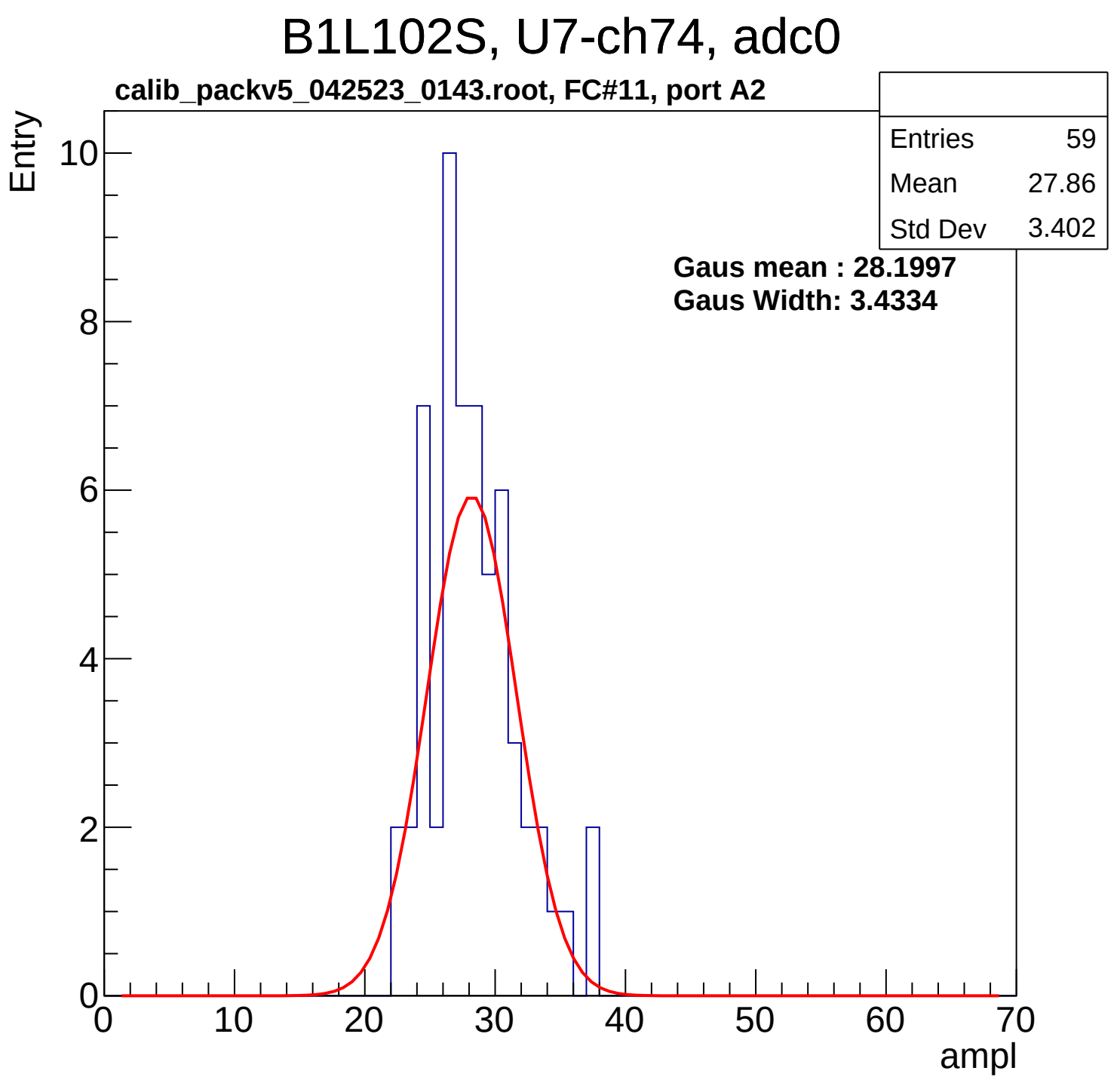
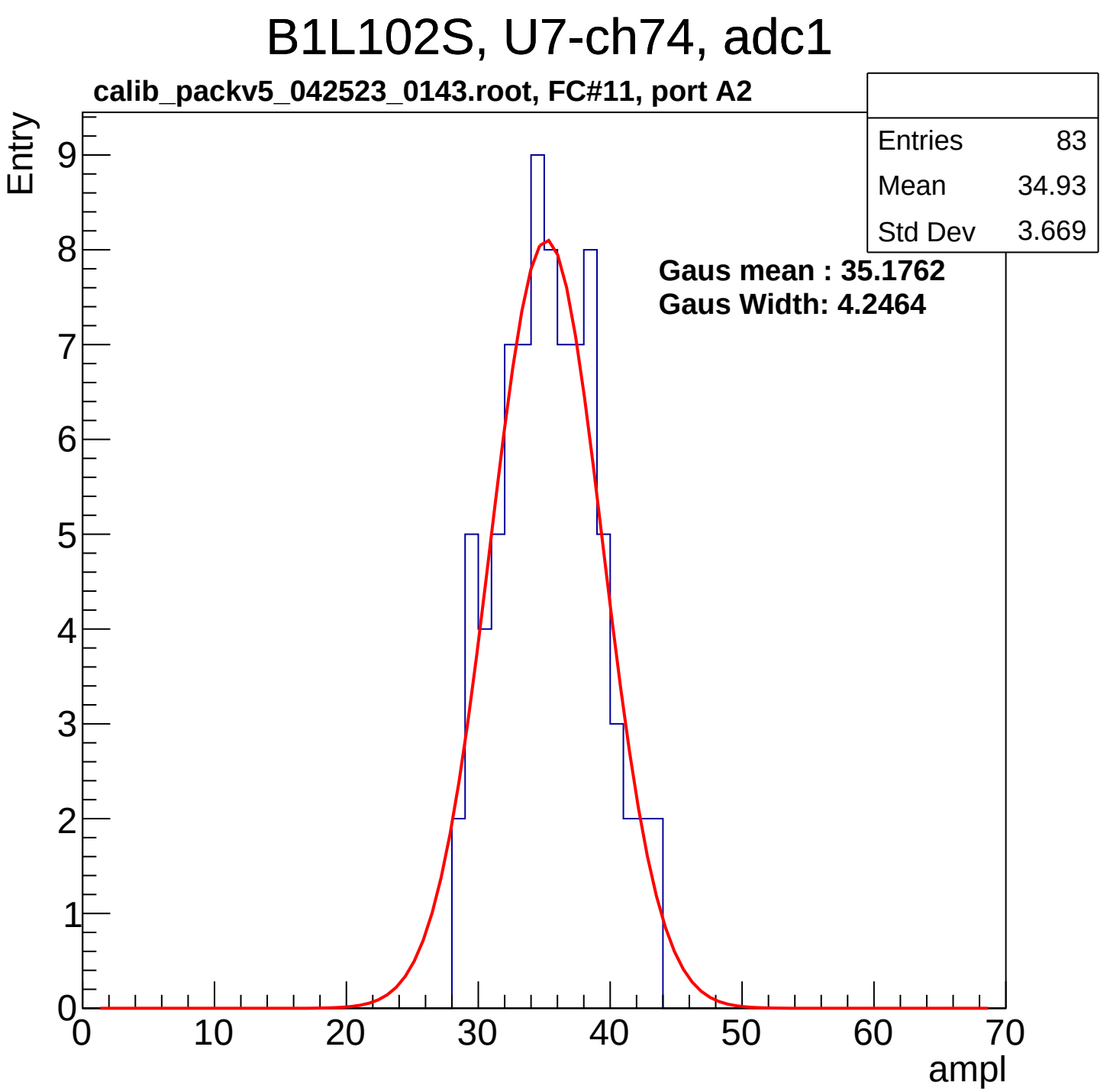

B1L102S, U7-ch74, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 59
Mean 27.86
Std Dev 3.402
Gaus mean : 28.1997
Gaus Width: 3.4334
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L102S, U7-ch74, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 83
Mean 34.93
Std Dev 3.669
Gaus mean : 35.1762
Gaus Width: 4.2464
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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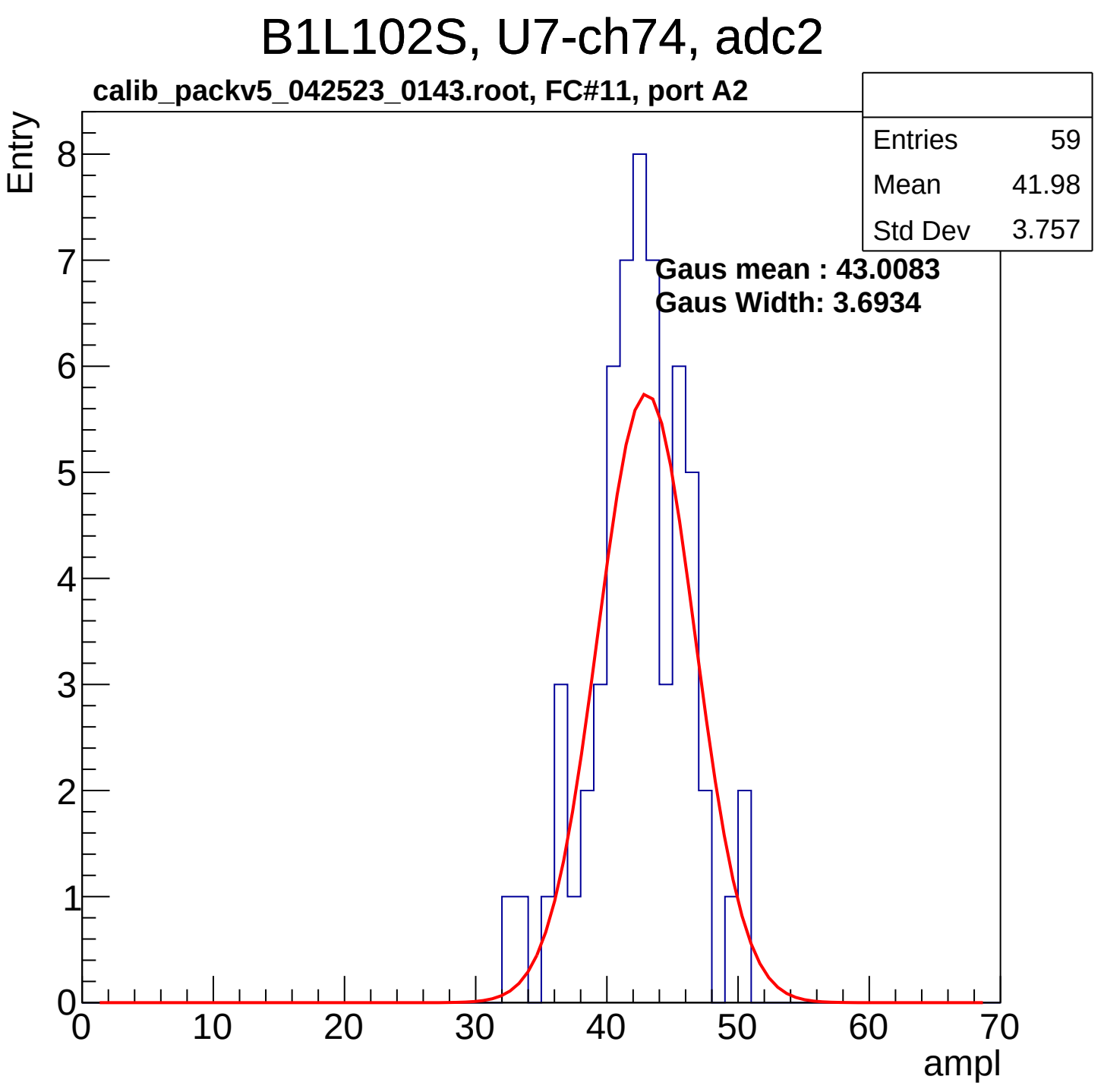
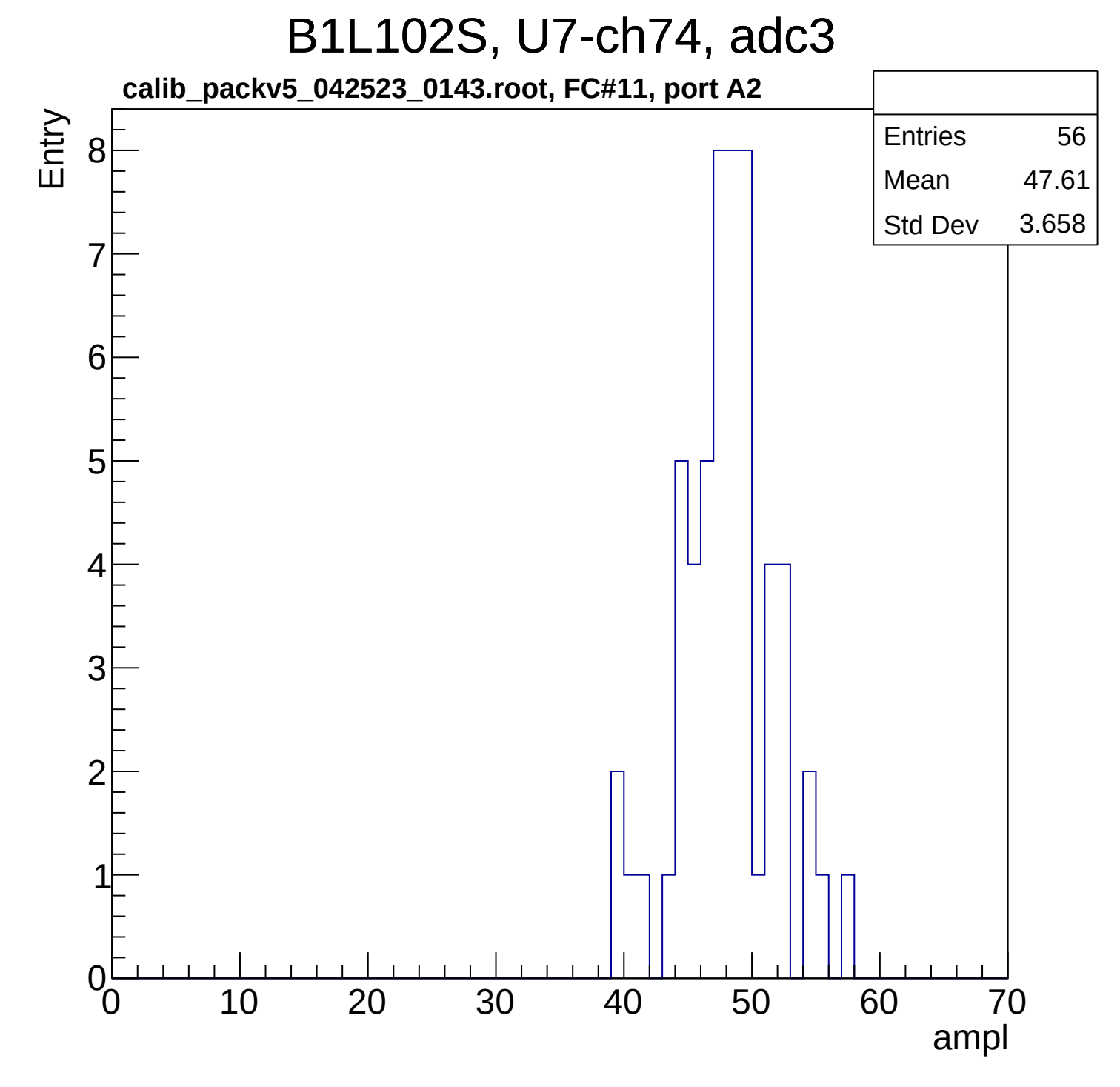
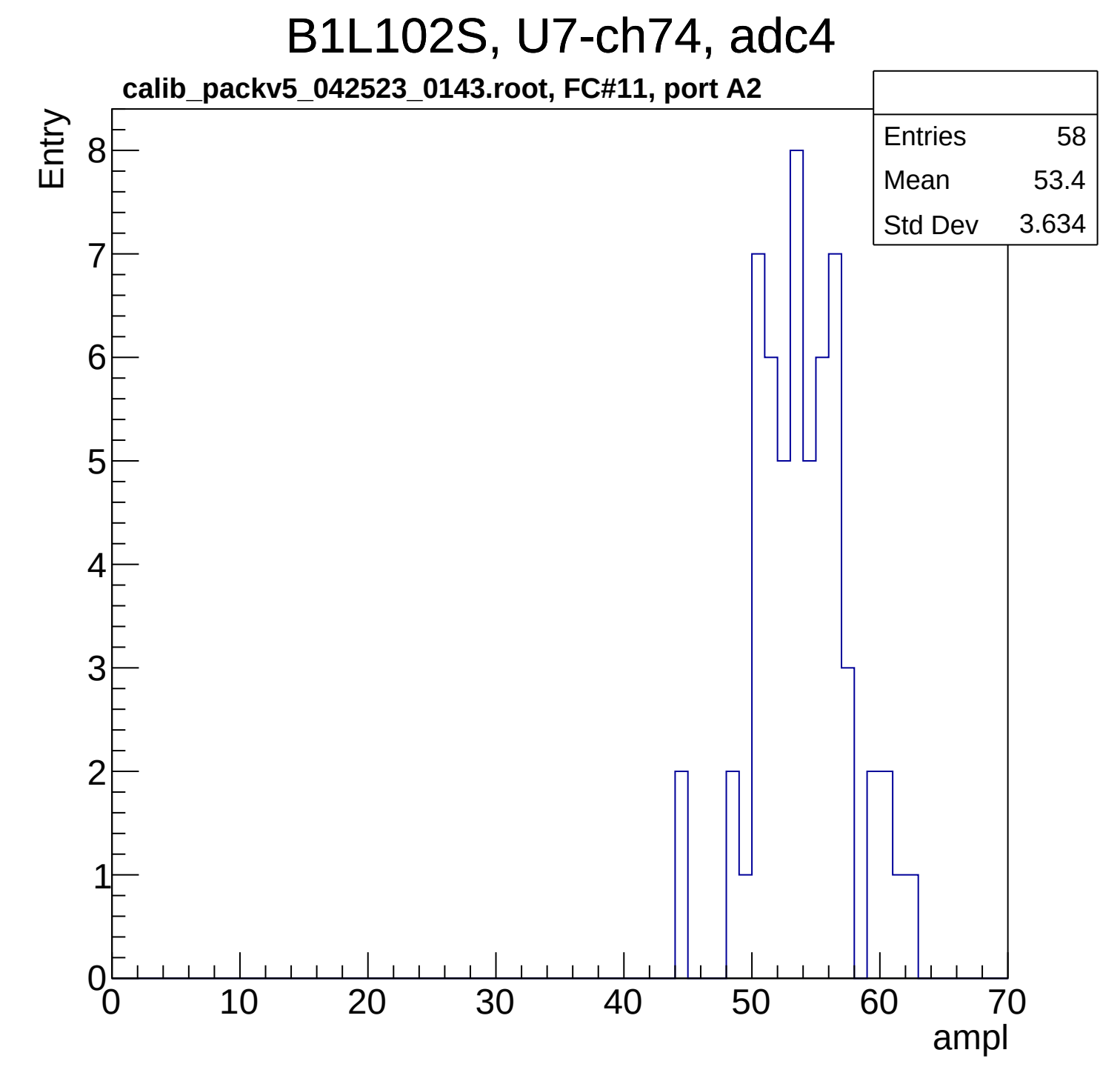
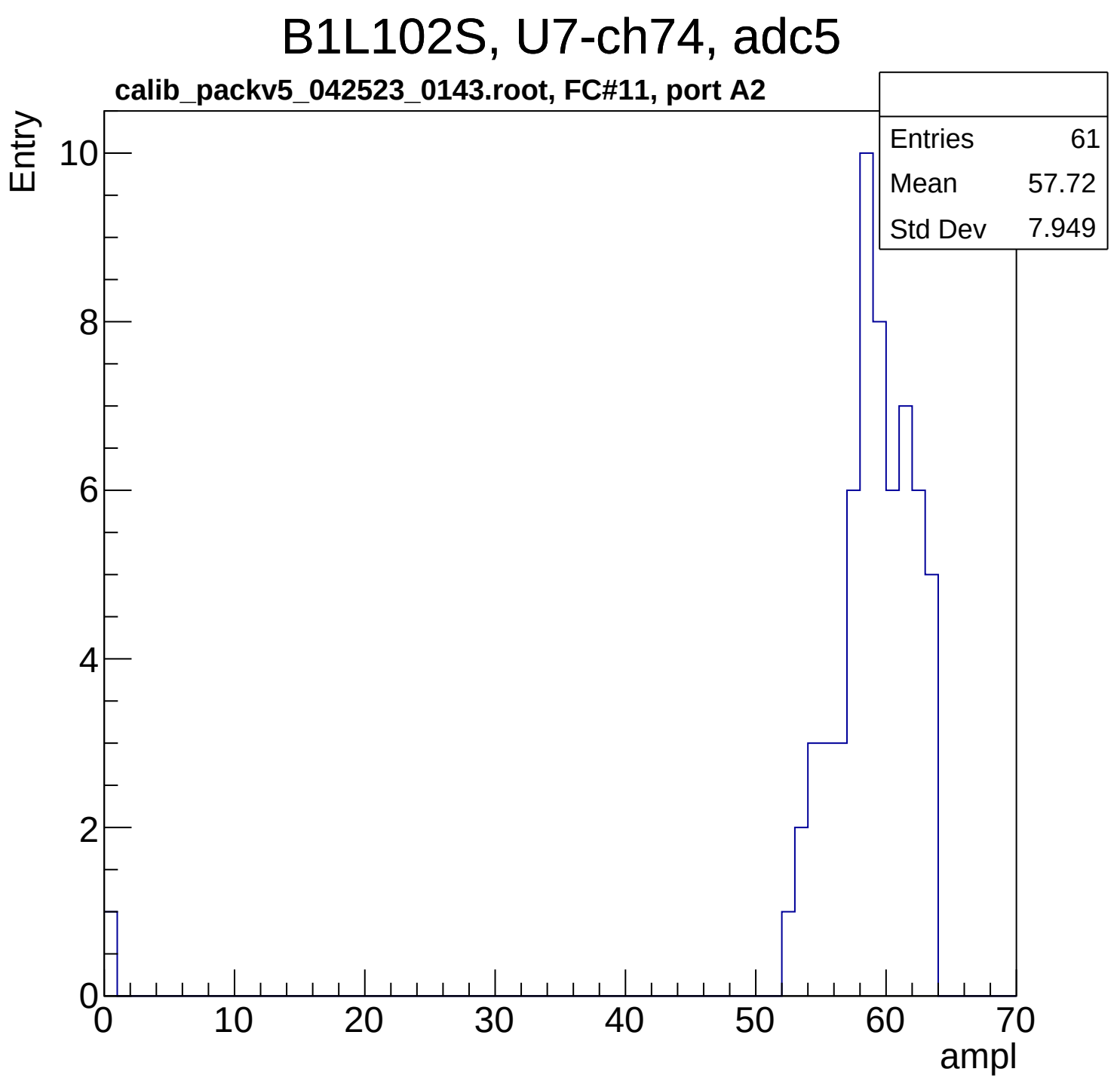
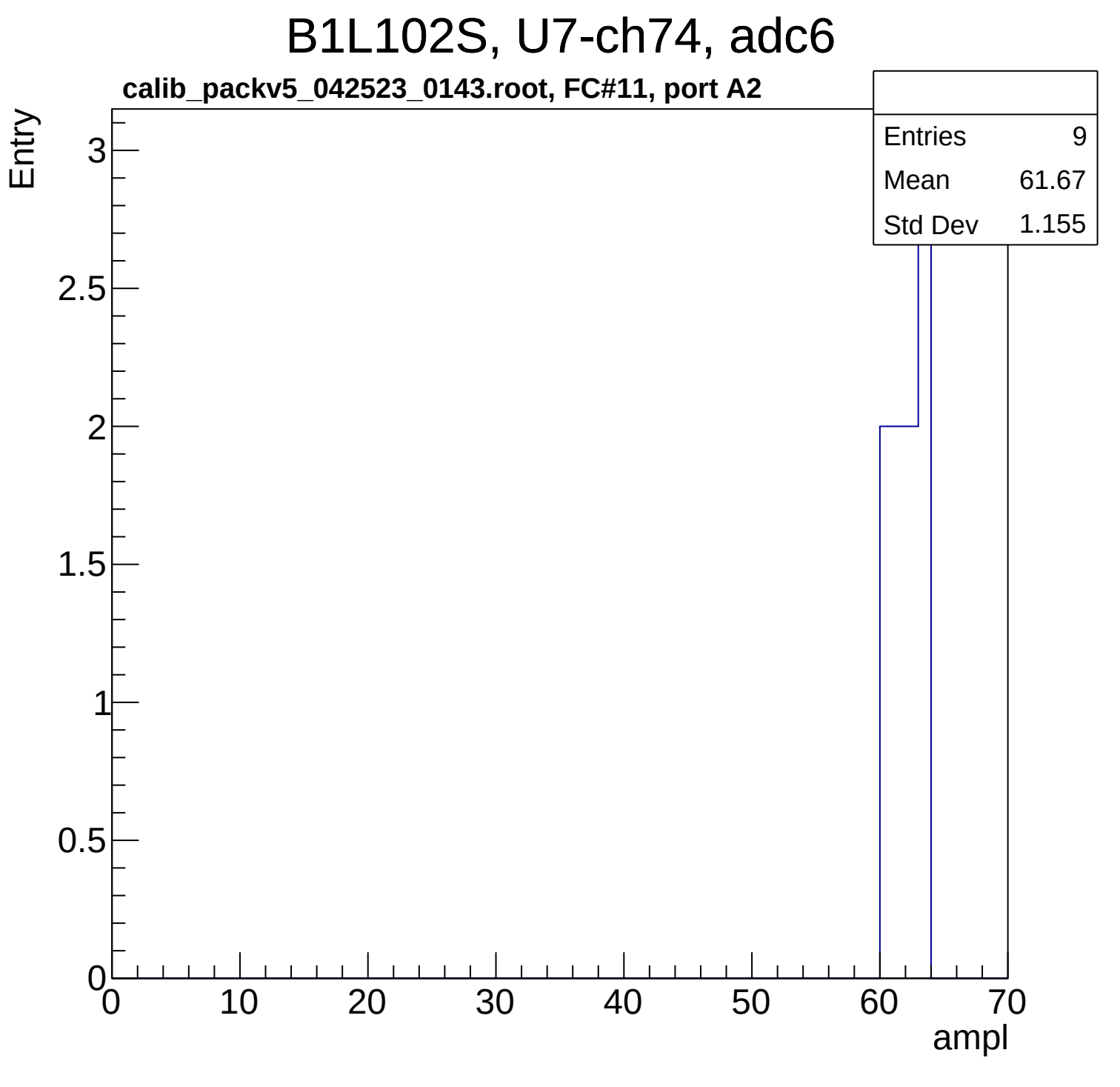
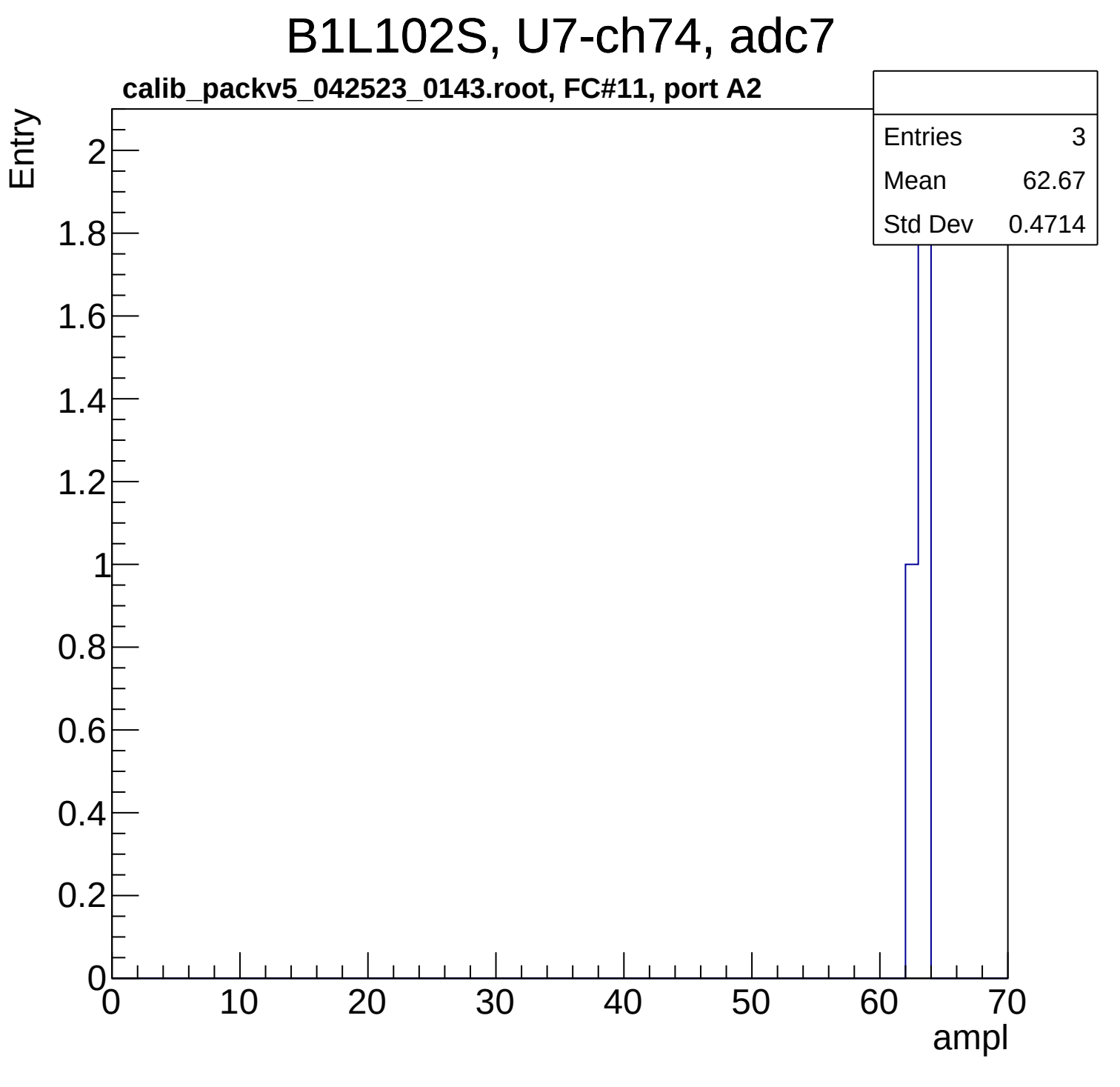

B1L102S, U7-ch74, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 59
Mean 41.98
Std Dev 3.757
Gaus mean : 43.0083
Gaus Width: 3.6934
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

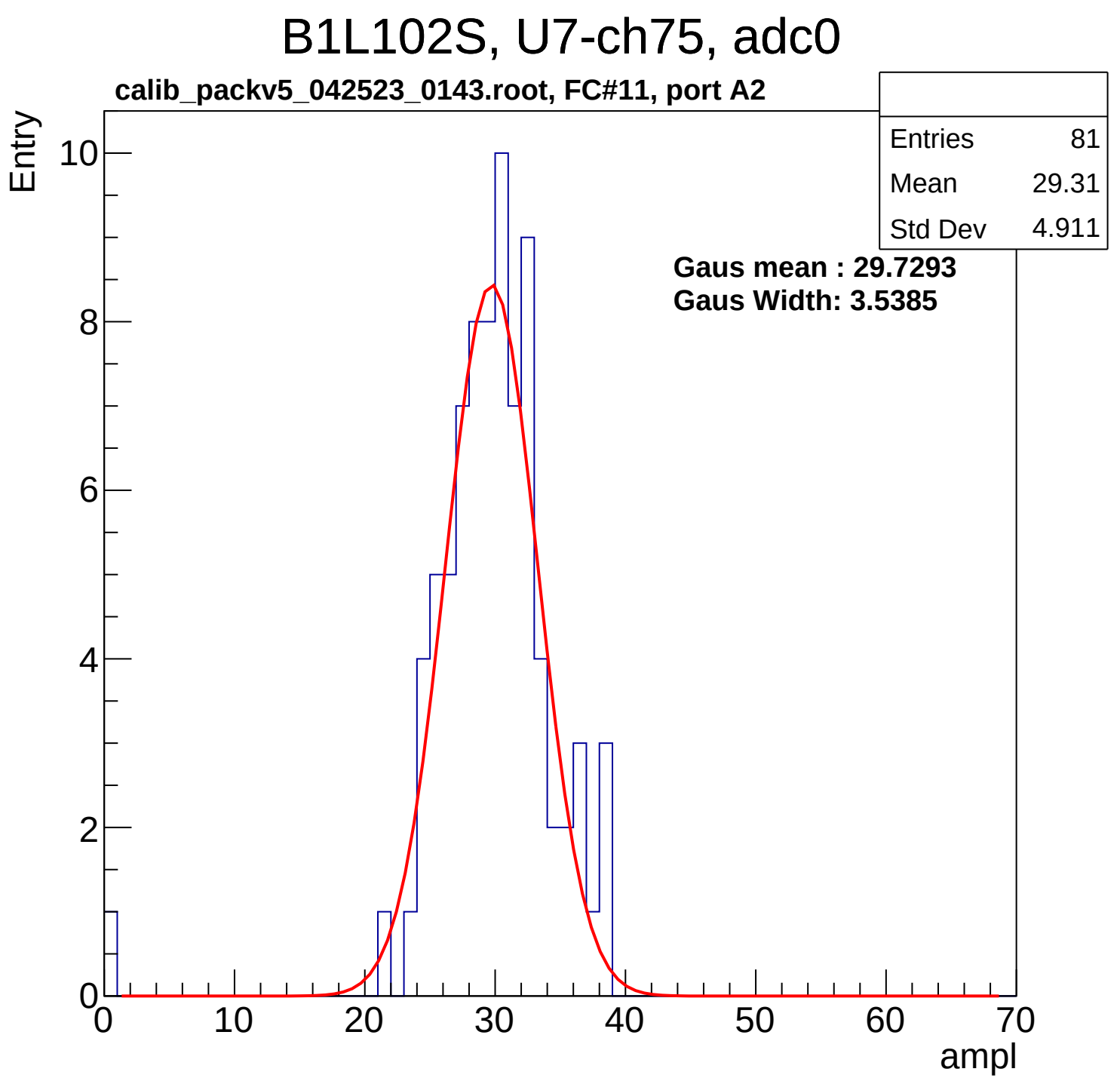

B1L102S, U7-ch74, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 56
Mean 47.61
Std Dev 3.658
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

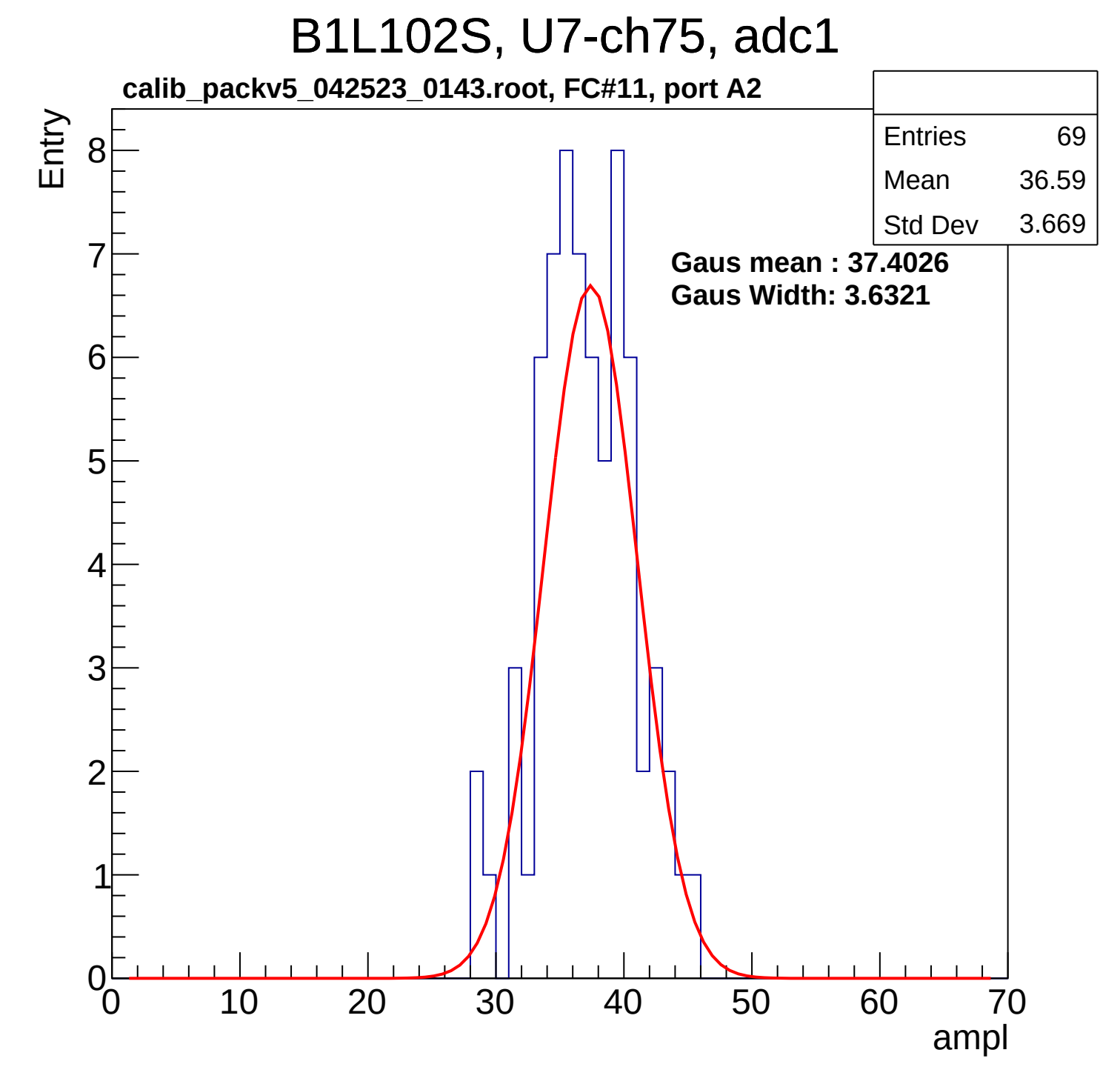

B1L102S, U7-ch74, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 58
Mean 53.4
Std Dev 3.634
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

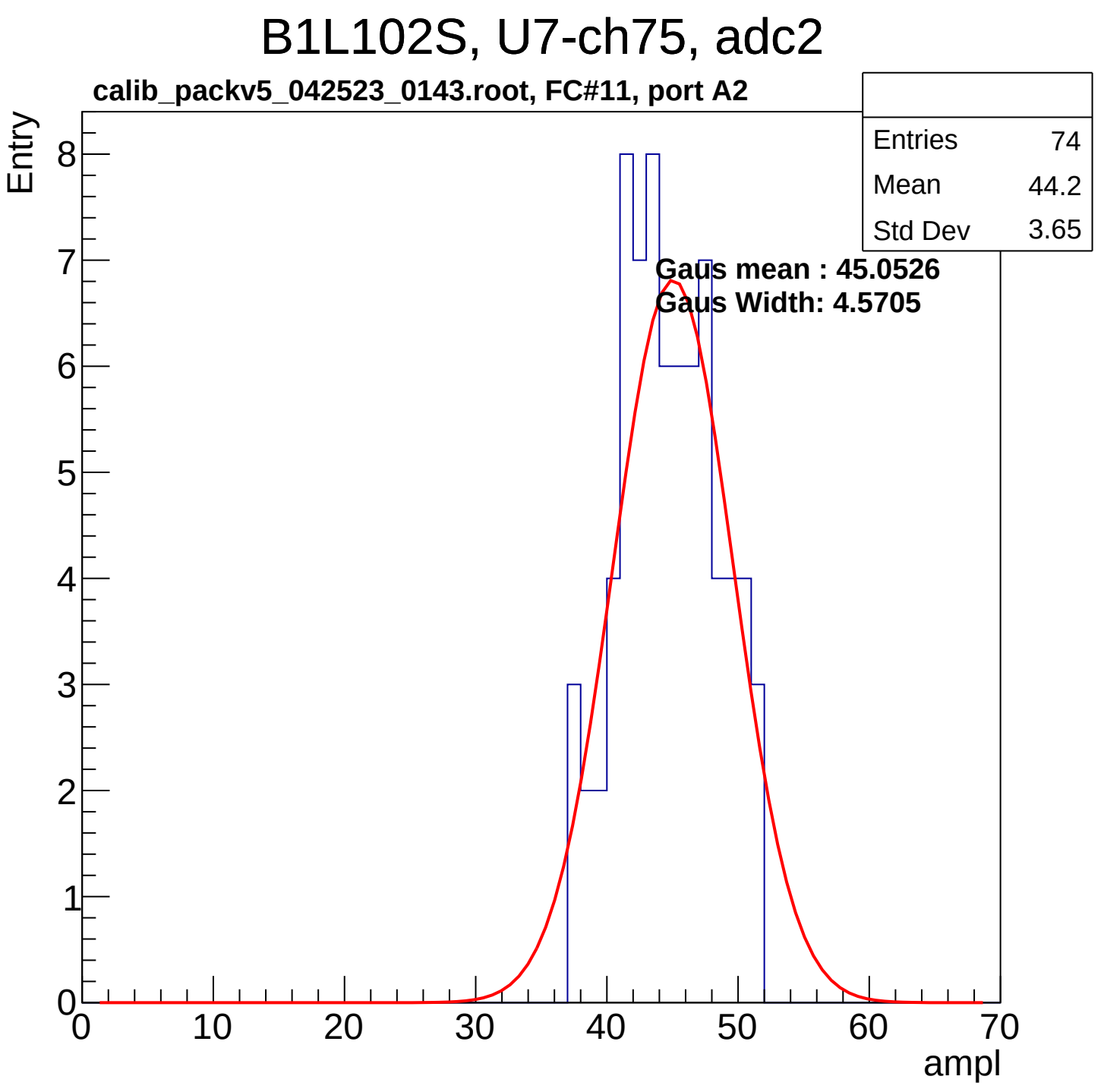

B1L102S, U7-ch74, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 61
Mean 57.72
Std Dev 7.949
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

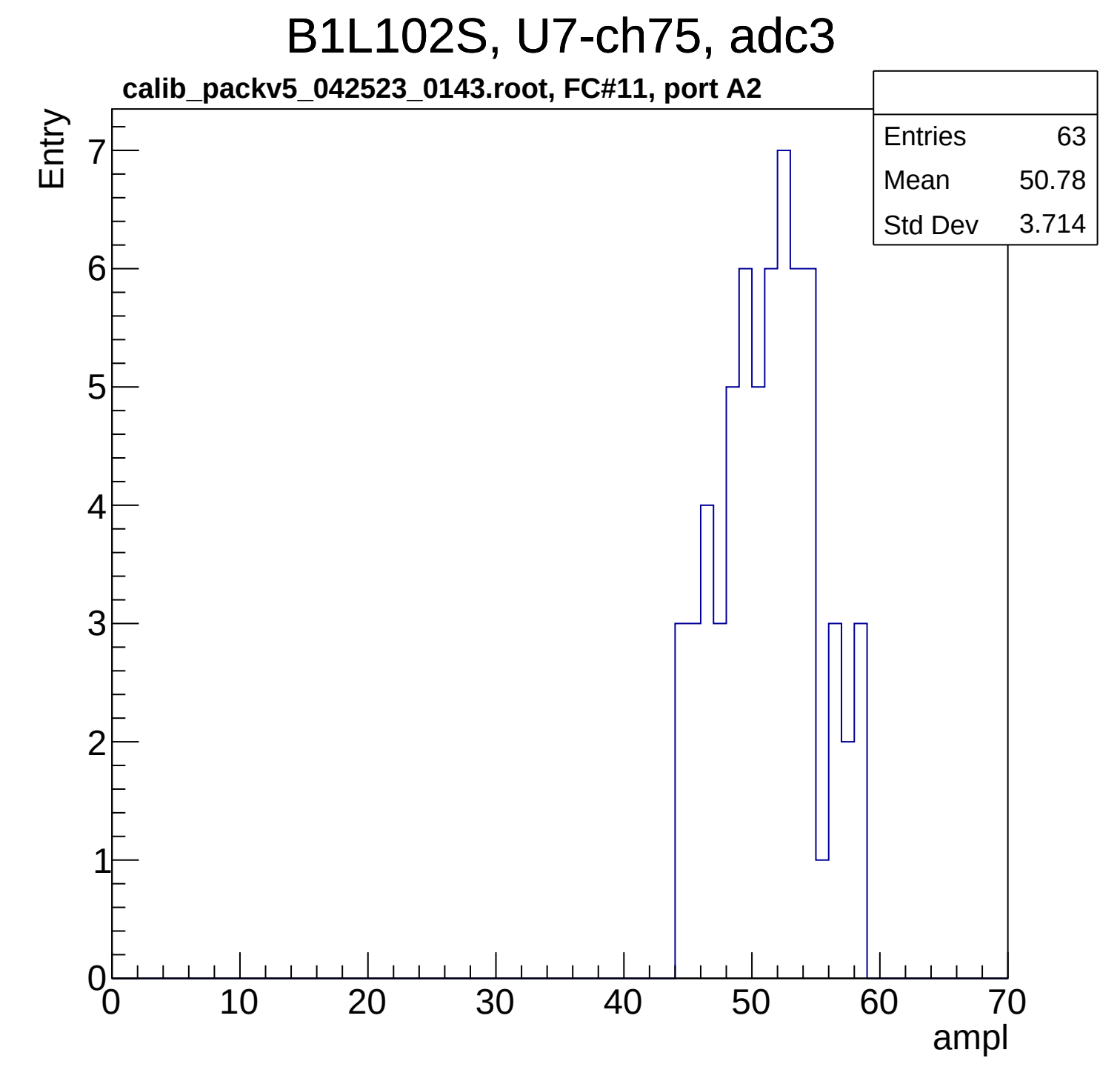

B1L102S, U7-ch74, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 9
Mean 61.67
Std Dev 1.155
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L102S, U7-ch74, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 3
Mean 62.67
Std Dev 0.4714
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L102S, U7-ch75, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 81
Mean 29.31
Std Dev 4.911
Gaus mean : 29.7293
Gaus Width: 3.5385
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L102S, U7-ch75, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 69
Mean 36.59
Std Dev 3.669
Gaus mean : 37.4026
Gaus Width: 3.6321
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L102S, U7-ch75, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 74
Mean 44.2
Std Dev 3.65
Gaus mean : 45.0526
Gaus Width: 4.5705
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L102S, U7-ch75, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 63
Mean 50.78
Std Dev 3.714
Entry
ampl
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1
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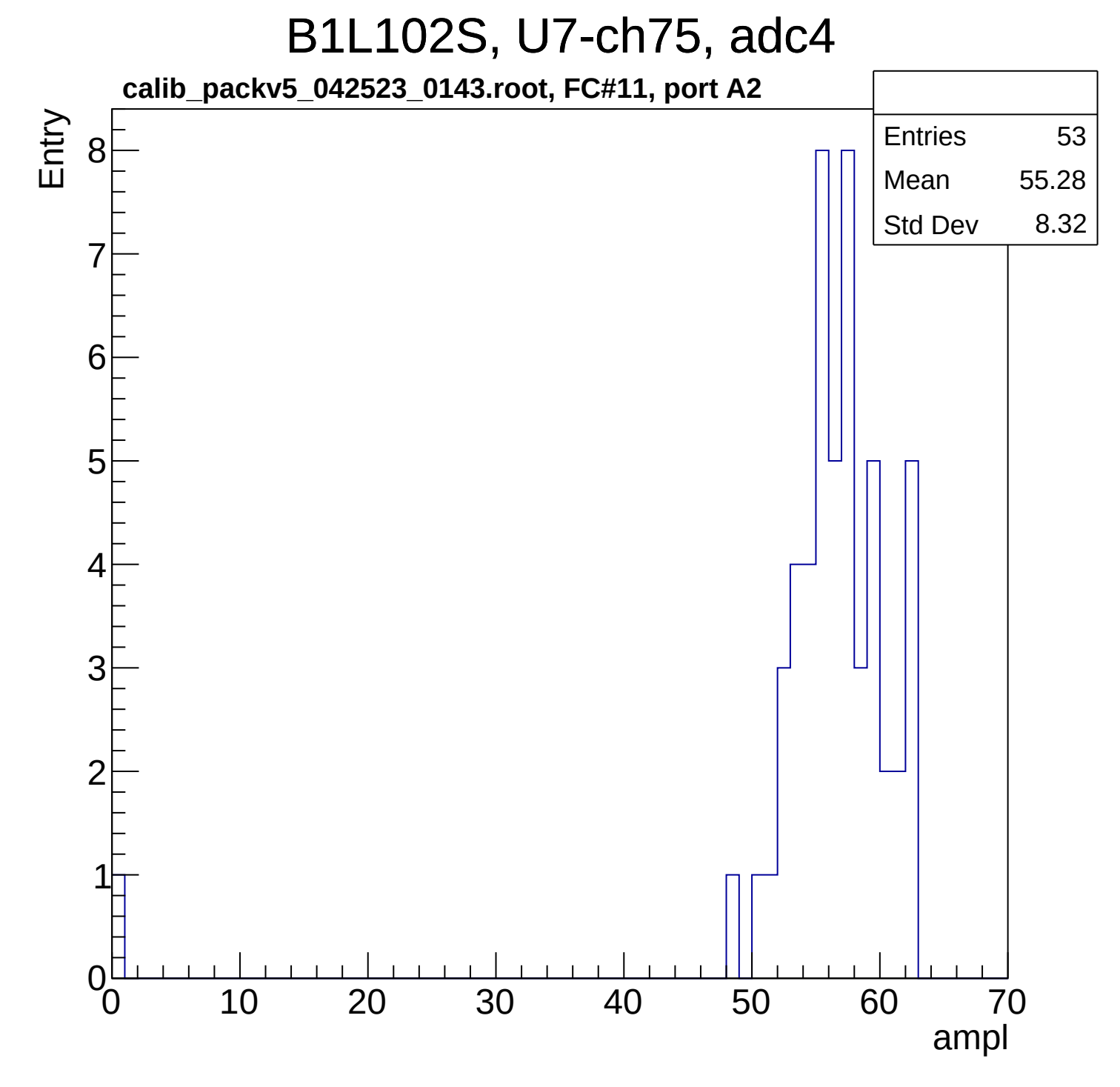
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L102S, U7-ch75, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 53
Mean 55.28
Std Dev 8.32
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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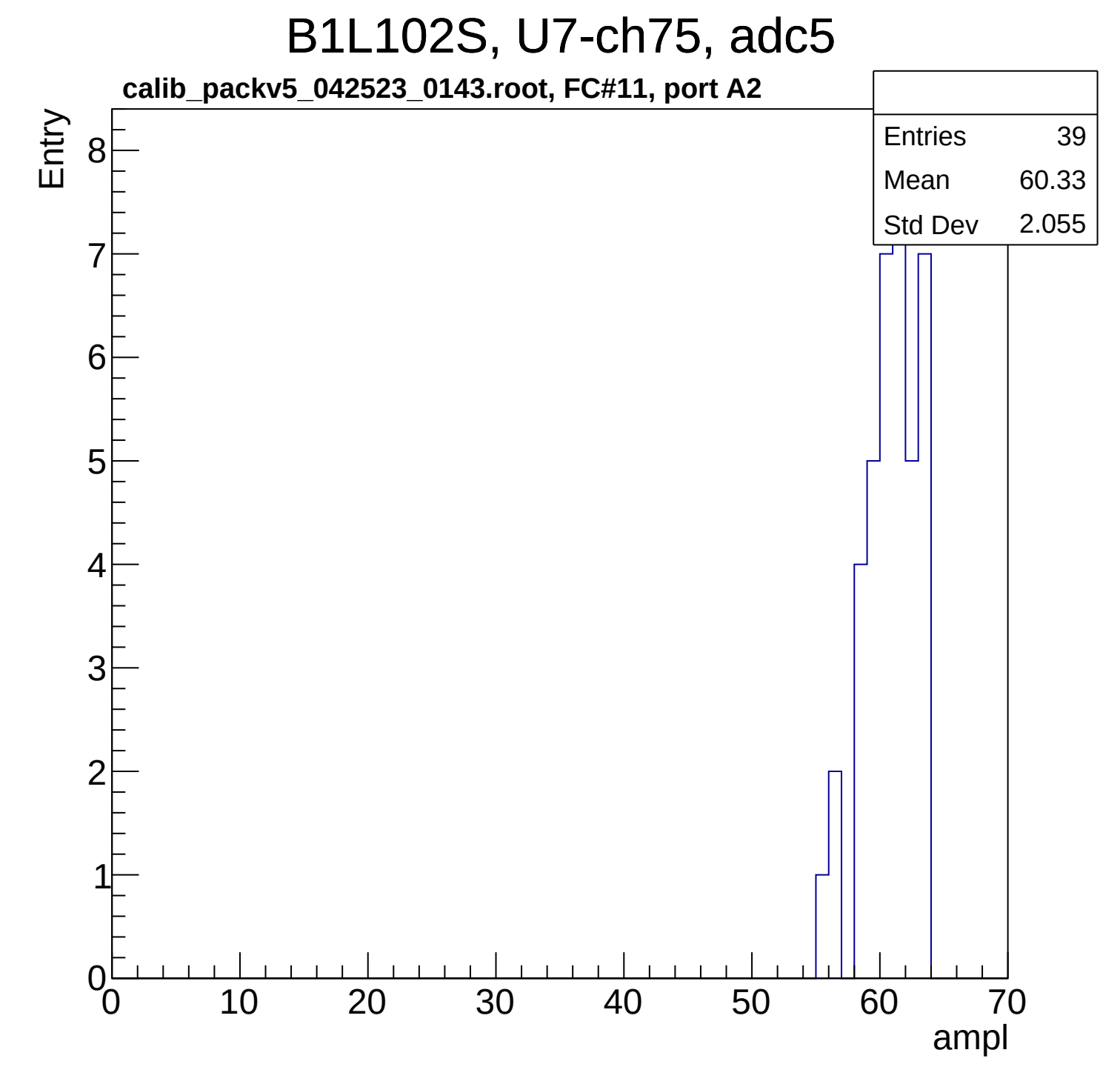
B1L102S, U7-ch75, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 39
Mean 60.33
Std Dev 2.055
Entry
ampl
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1
2
3
4
5
6
7
8
0
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60
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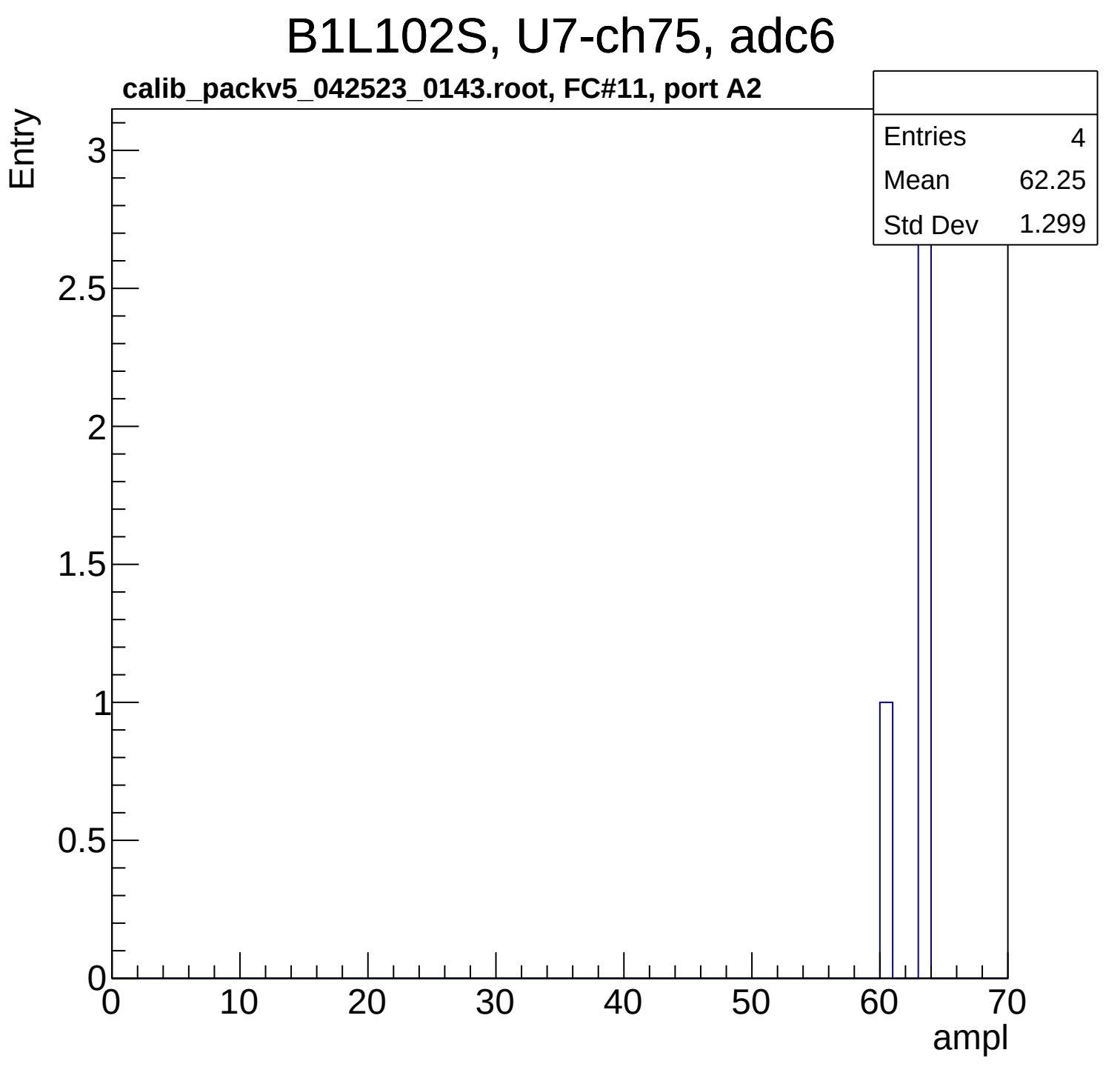
B1L102S, U7-ch75, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 4
Mean 62.25
Std Dev 1.299
Entry
ampl
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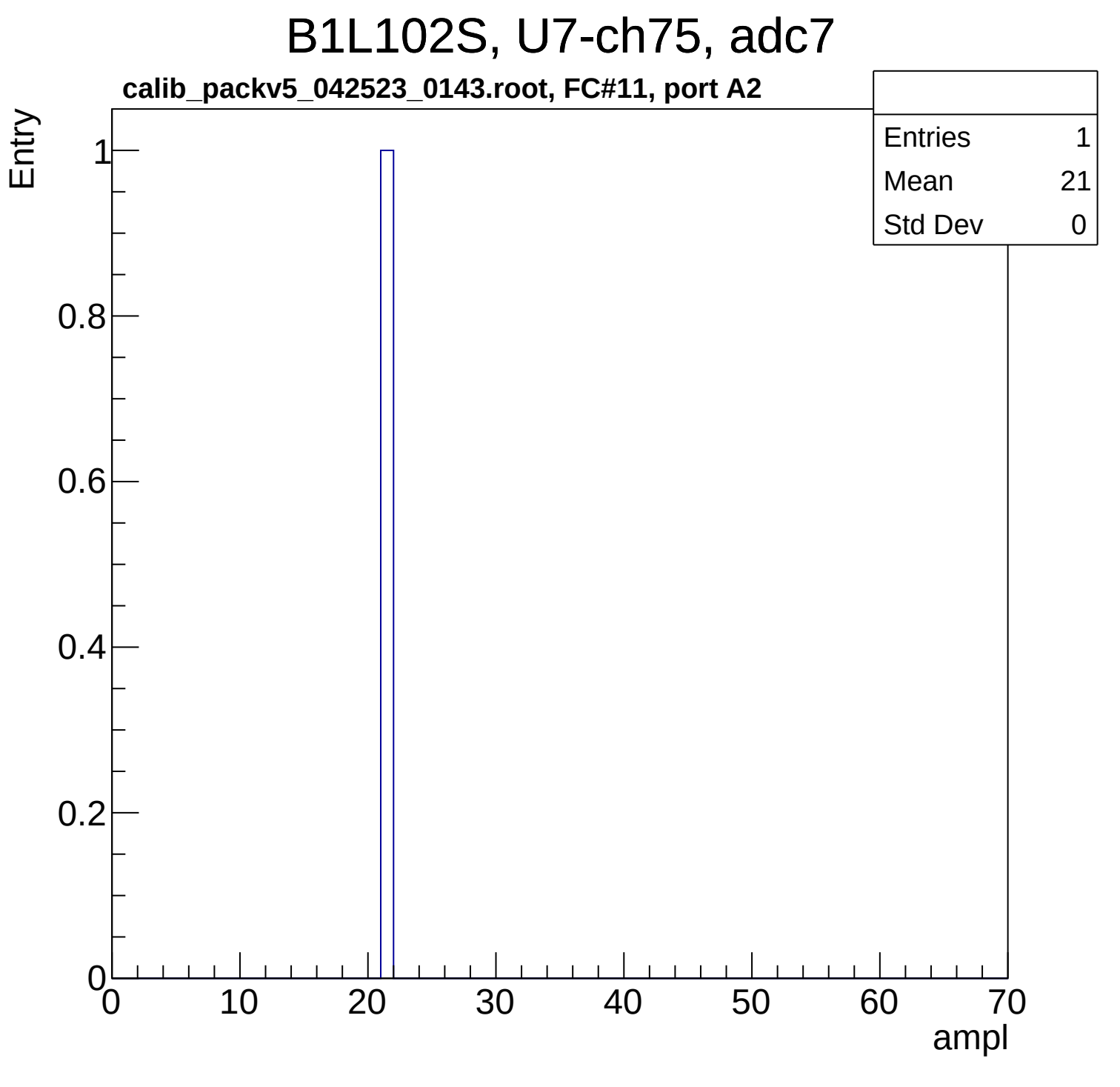
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L102S, U7-ch75, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 1
Mean 21
Std Dev 0
Entry
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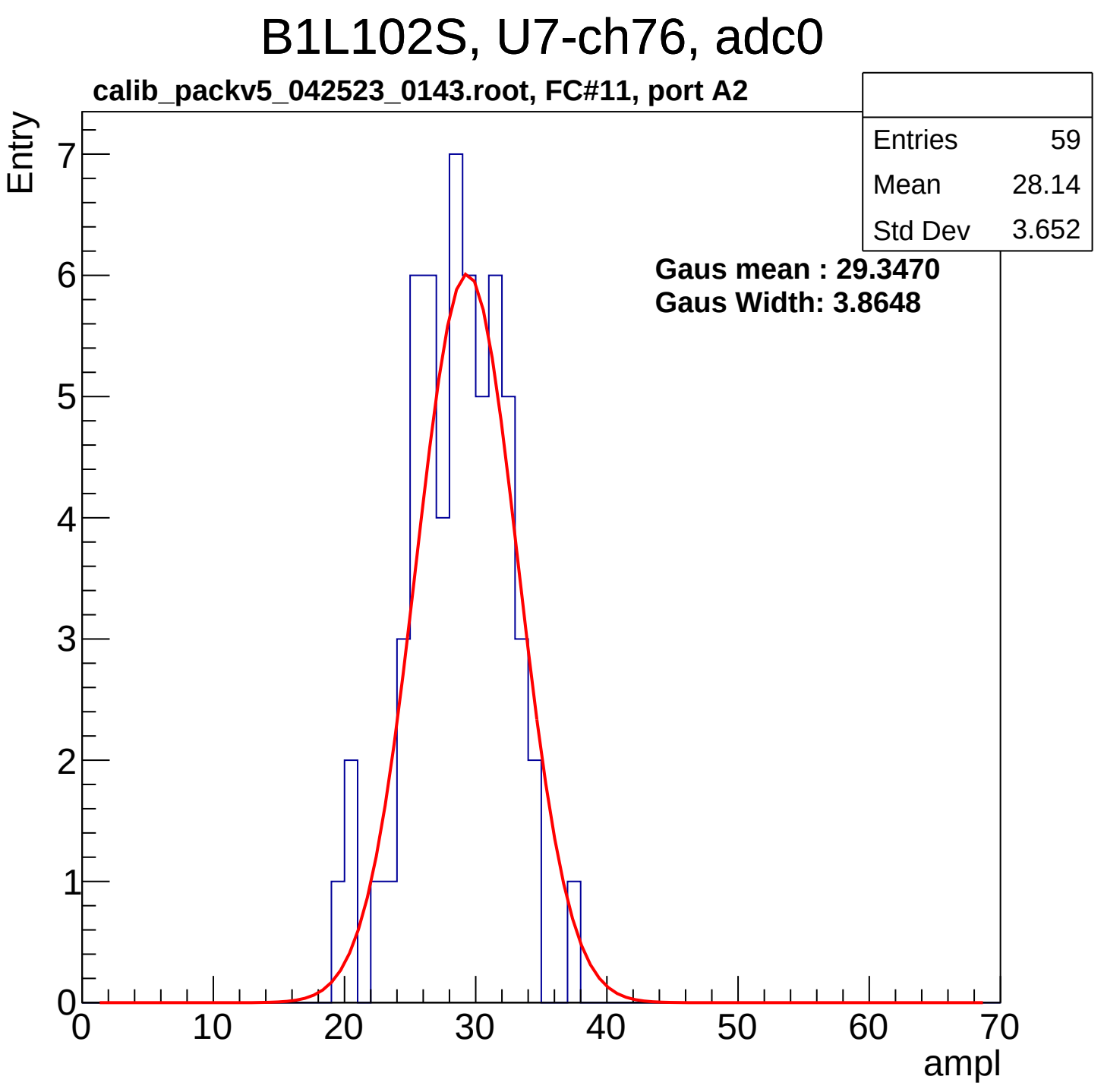
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U7-ch76, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 59
Mean 28.14
Std Dev 3.652
Gaus mean : 29.3470
Gaus Width: 3.8648
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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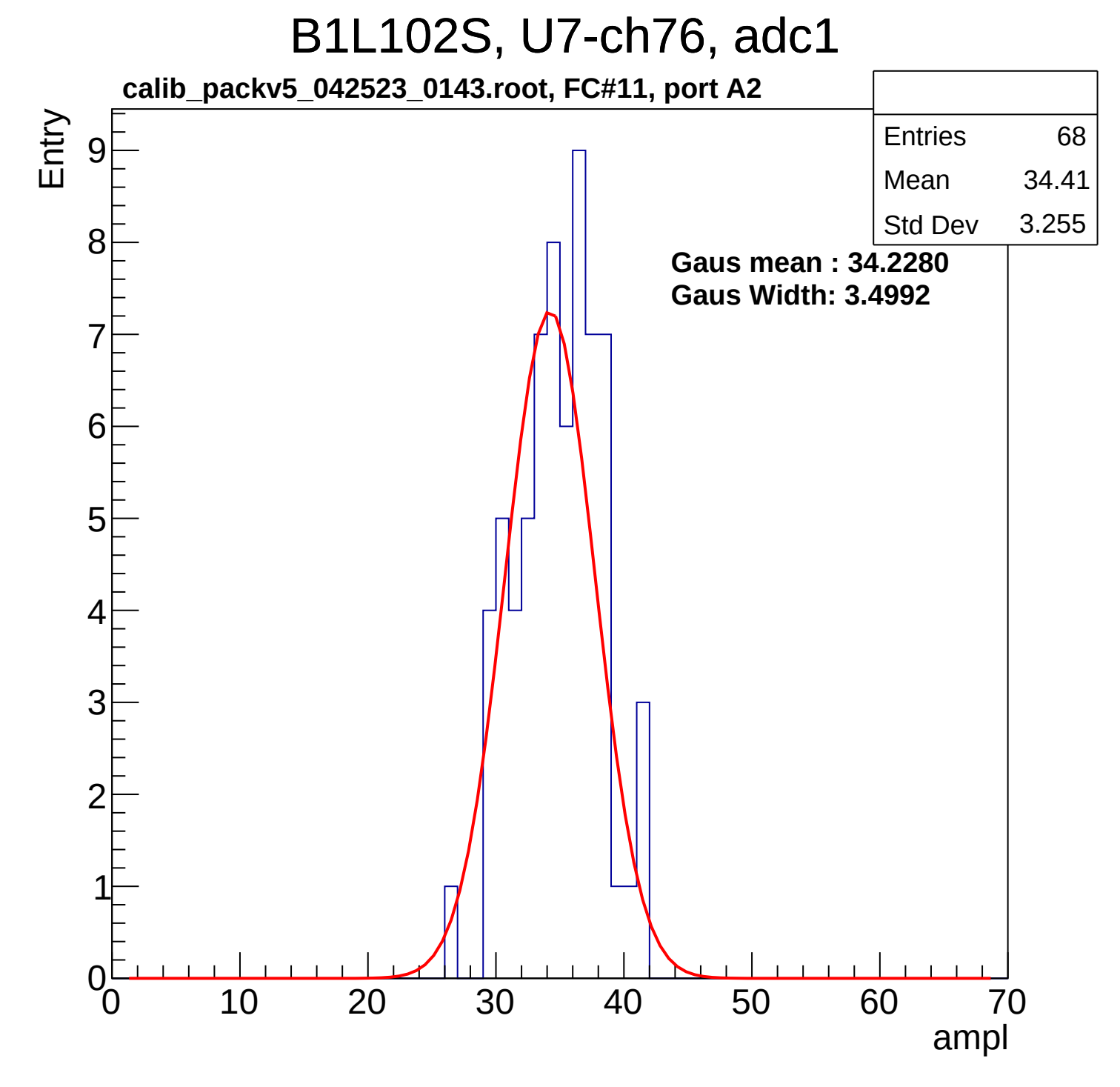
B1L102S, U7-ch76, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 68
Mean 34.41
Std Dev 3.255
Gaus mean : 34.2280
Gaus Width: 3.4992
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
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20
30
40
50
60
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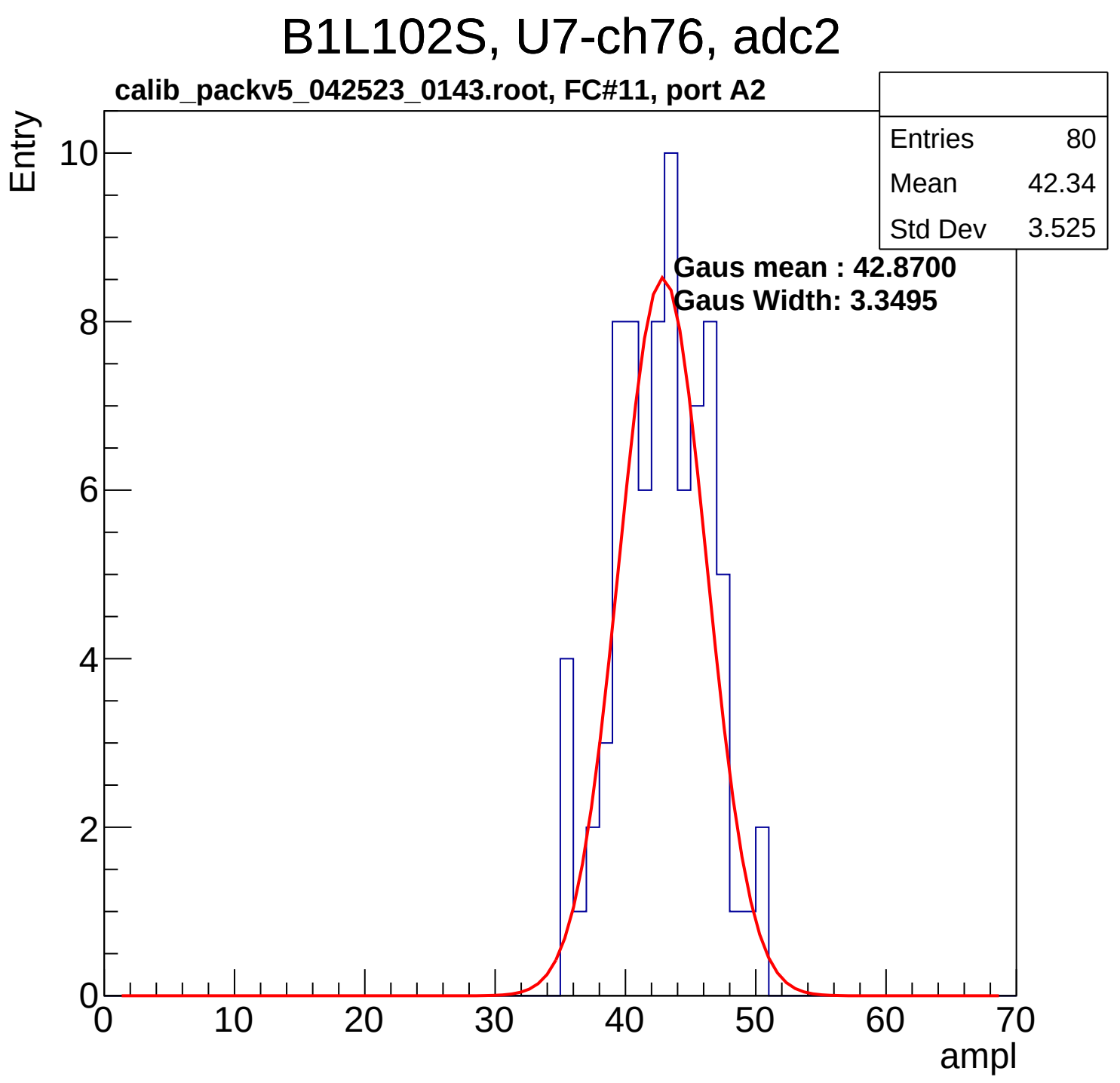
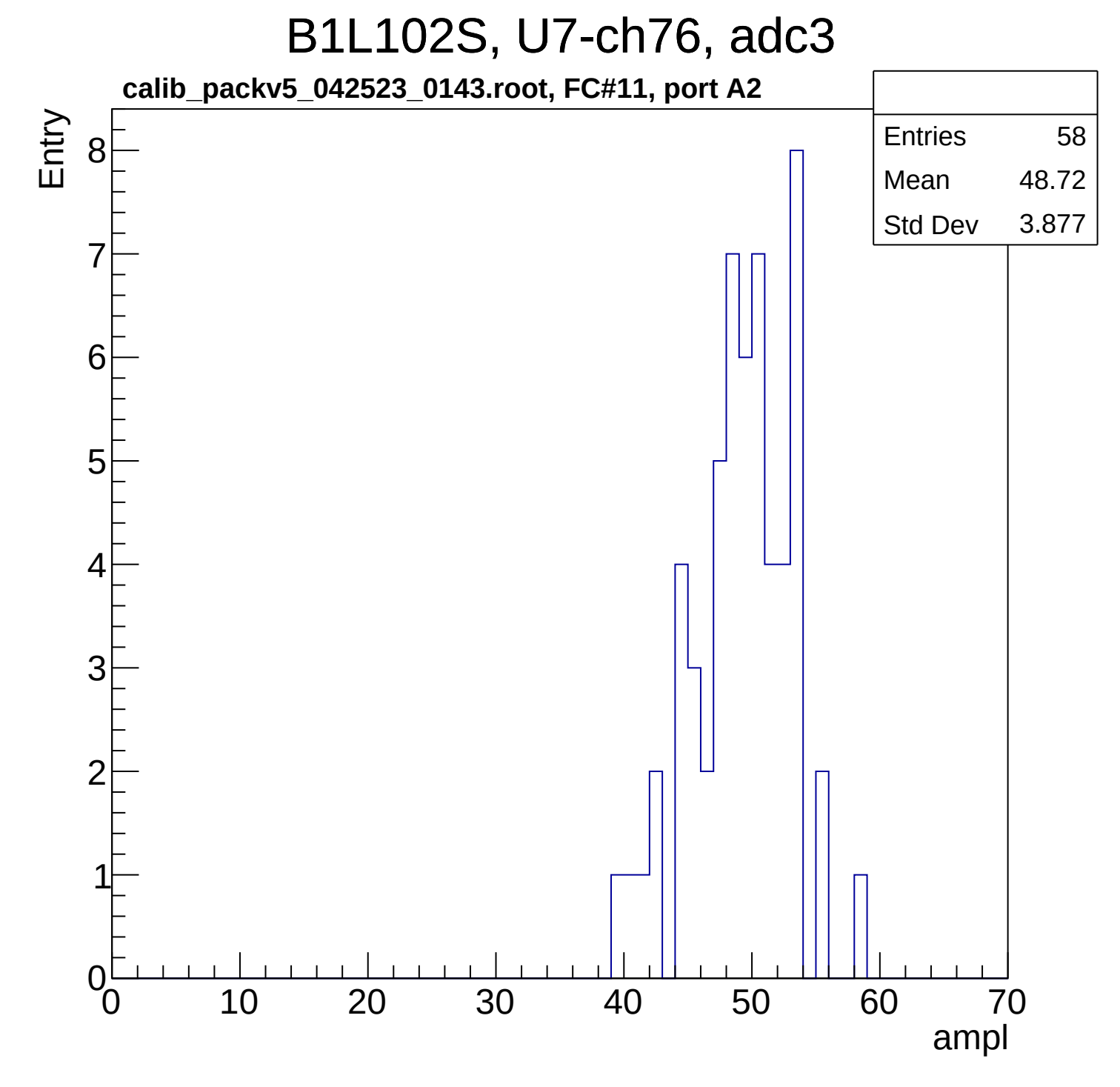

B1L102S, U7-ch76, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 80
Mean 42.34
Std Dev 3.525
Gaus mean : 42.8700
Gaus Width: 3.3495
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L102S, U7-ch76, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 58
Mean 48.72
Std Dev 3.877
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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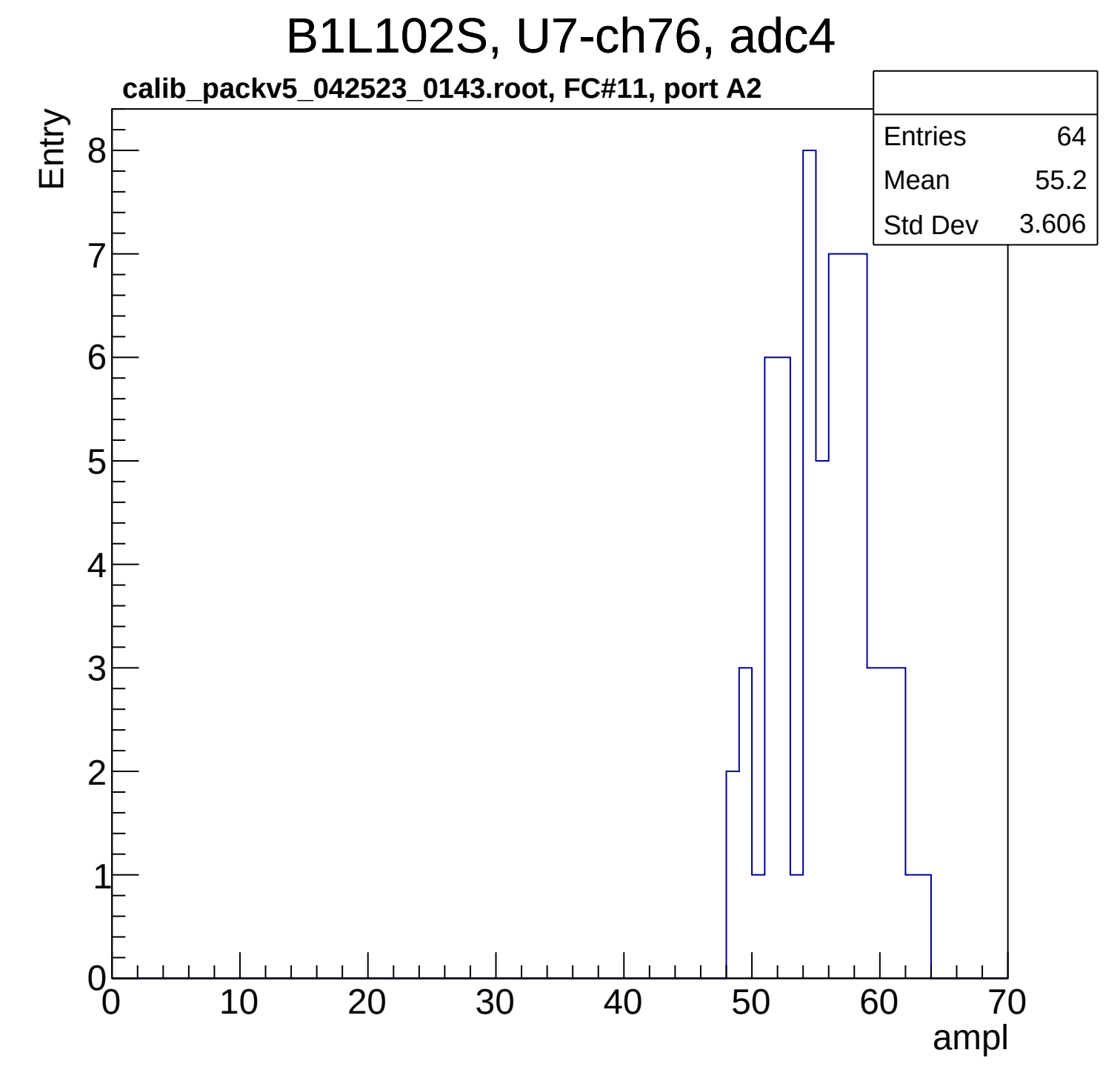
B1L102S, U7-ch76, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 64
Mean 55.2
Std Dev 3.606
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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40
50
60
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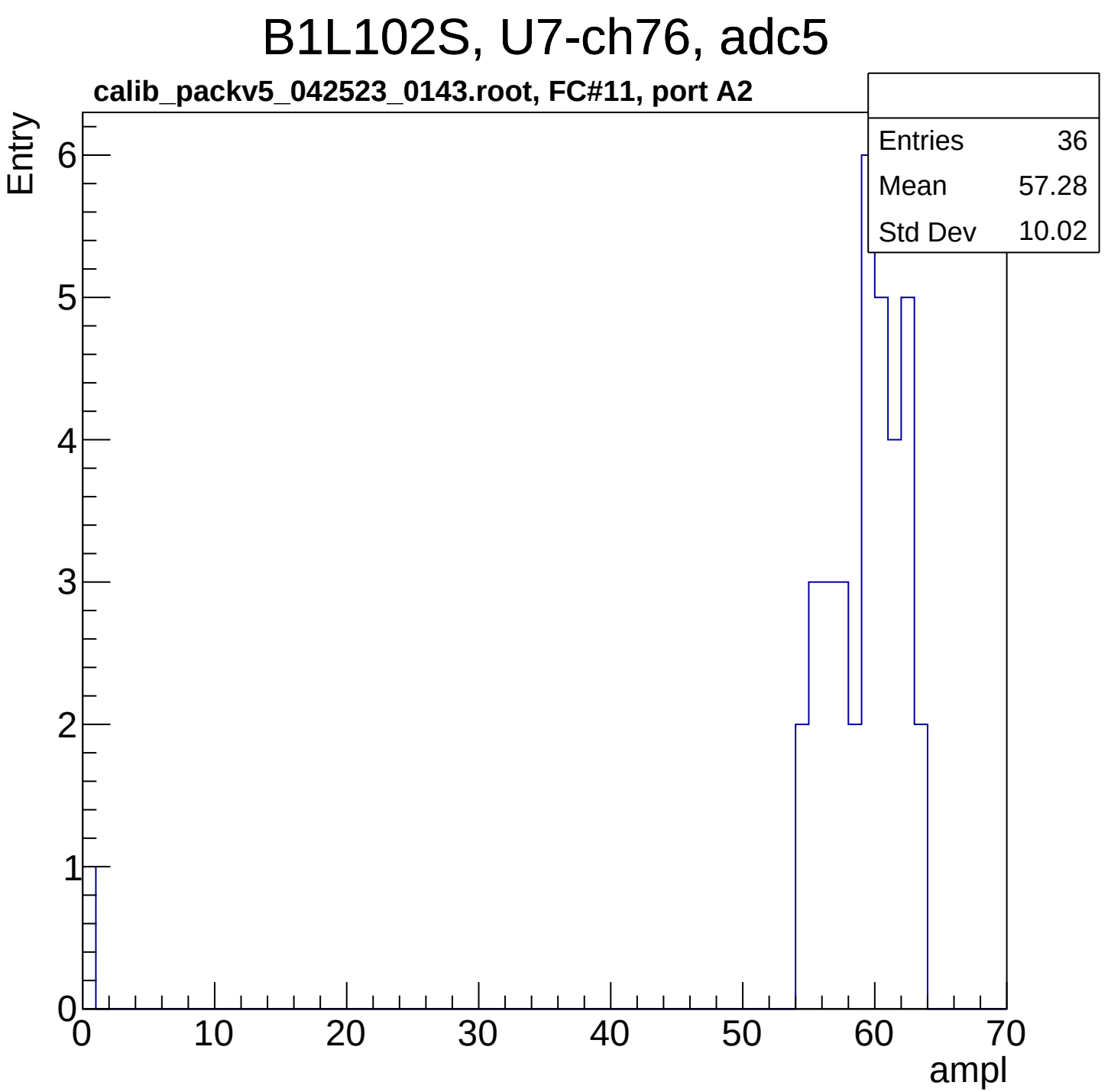
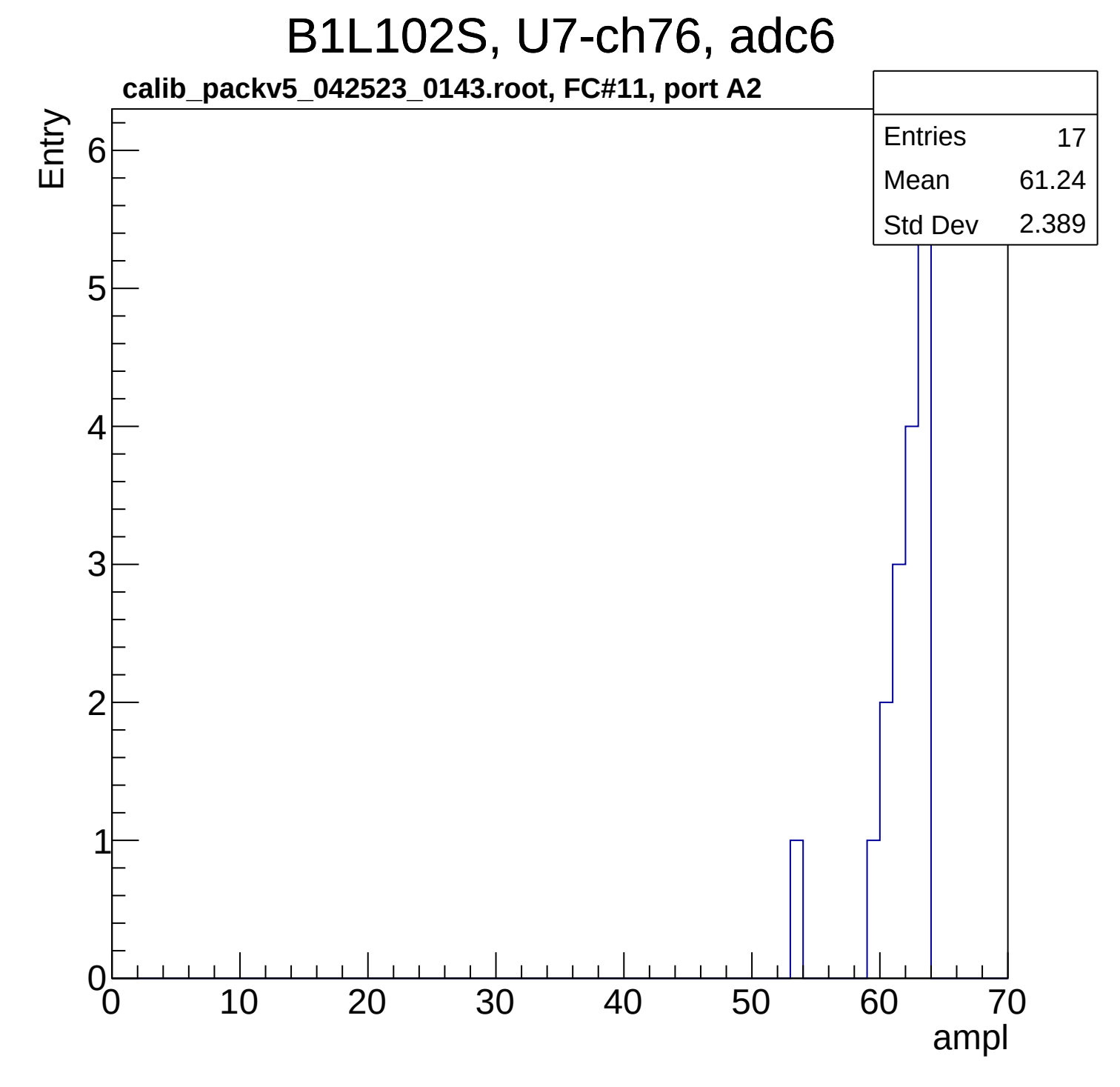
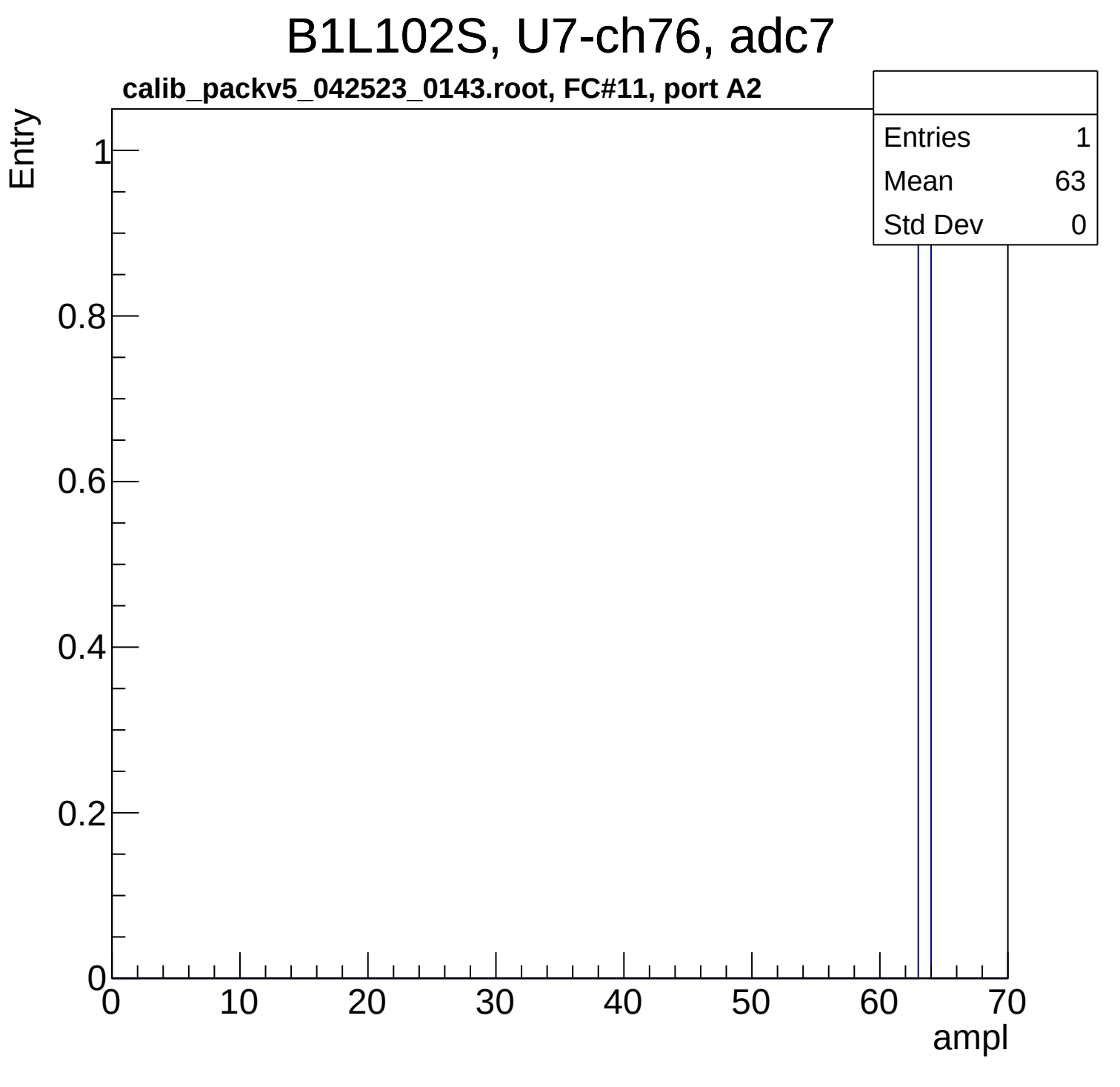

B1L102S, U7-ch76, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 36
Mean 57.28
Std Dev 10.02
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L102S, U7-ch76, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 17
Mean 61.24
Std Dev 2.389
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L102S, U7-ch76, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 1
Mean 63
Std Dev 0
Entry
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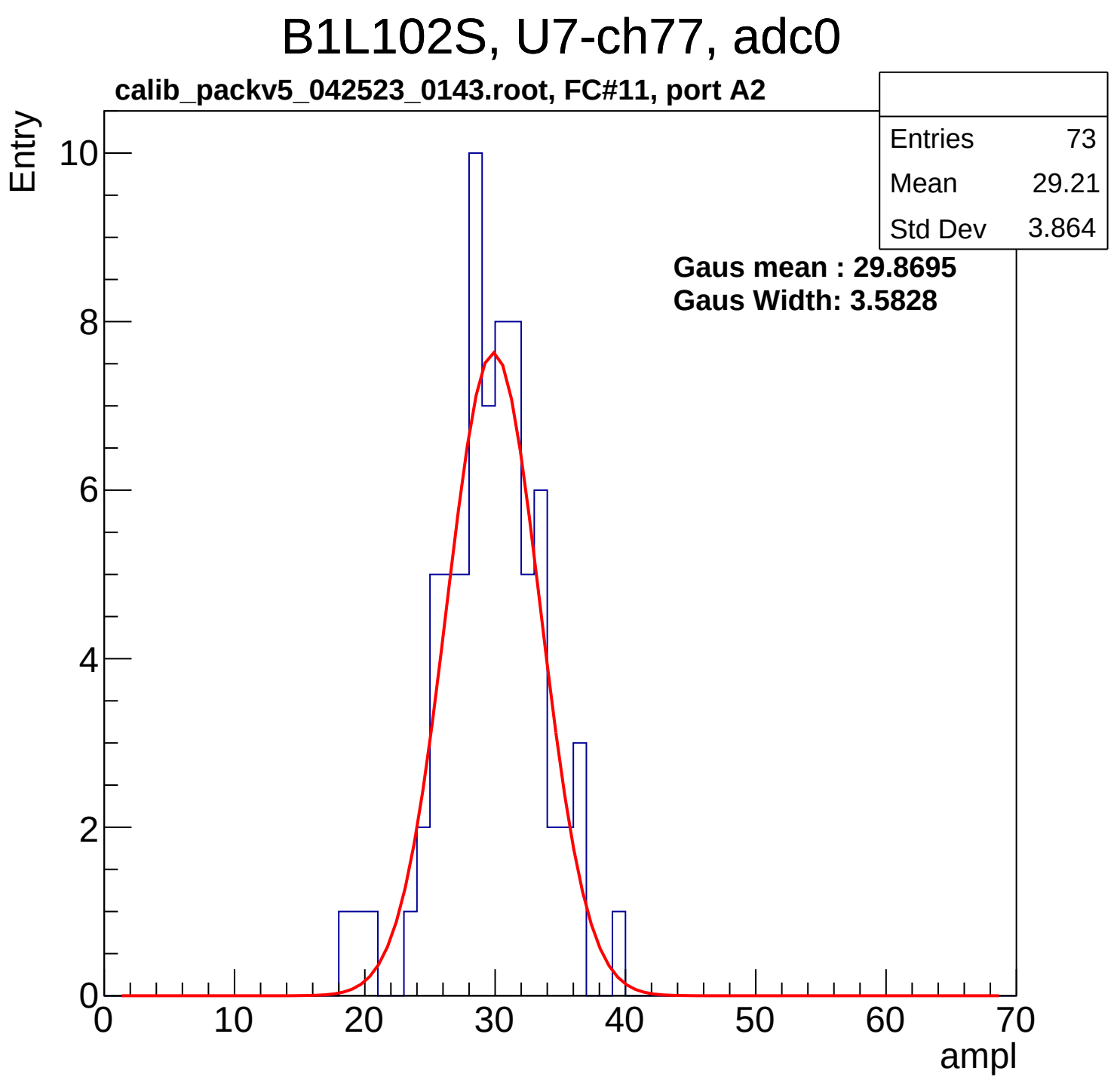
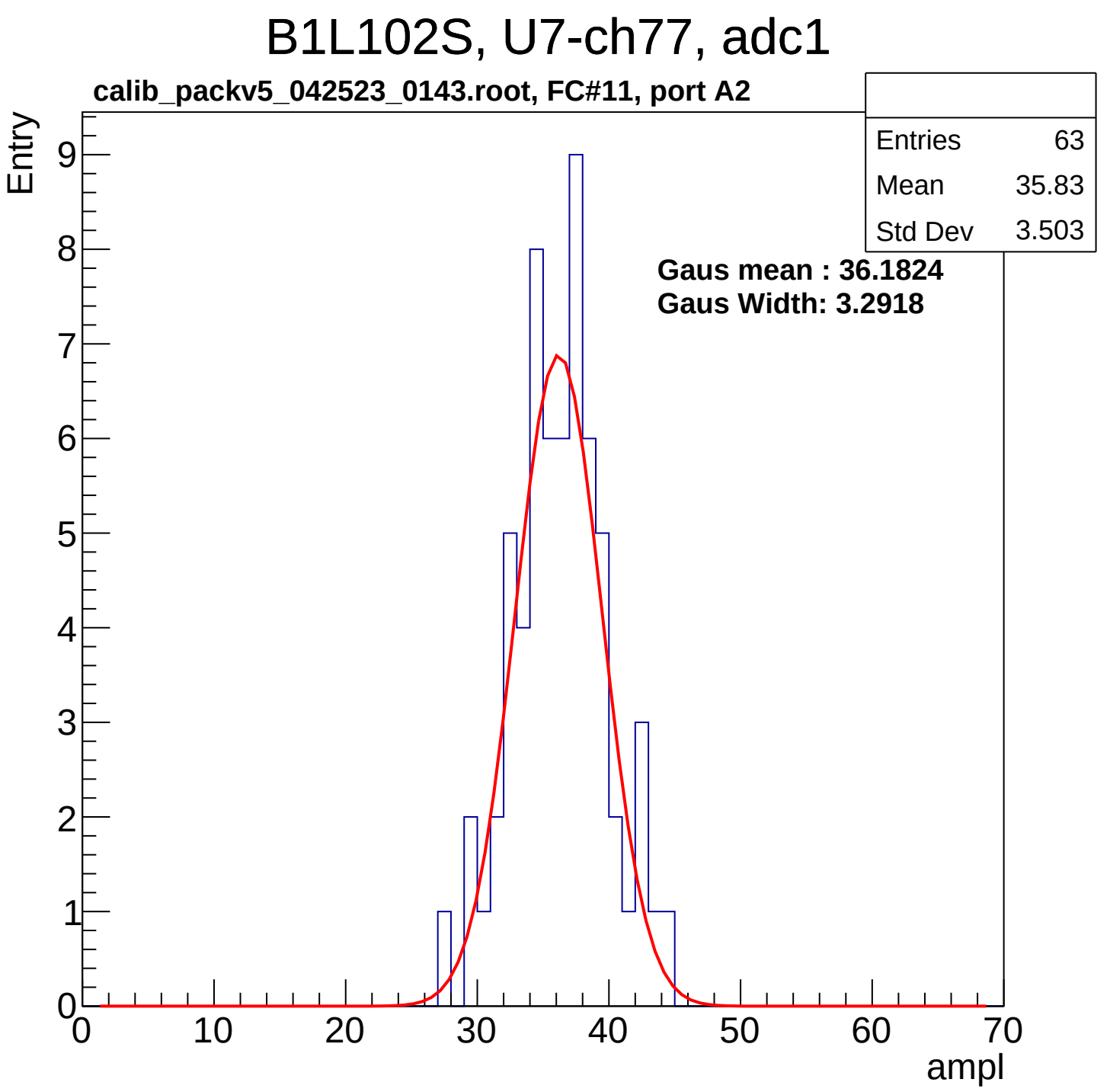
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U7-ch77, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 73
Mean 29.21
Std Dev 3.864
Gaus mean : 29.8695
Gaus Width: 3.5828
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L102S, U7-ch77, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 63
Mean 35.83
Std Dev 3.503
Gaus mean : 36.1824
Gaus Width: 3.2918
Entry
ampl
0
1
2
3
4
5
6
7
8
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0
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20
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40
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60
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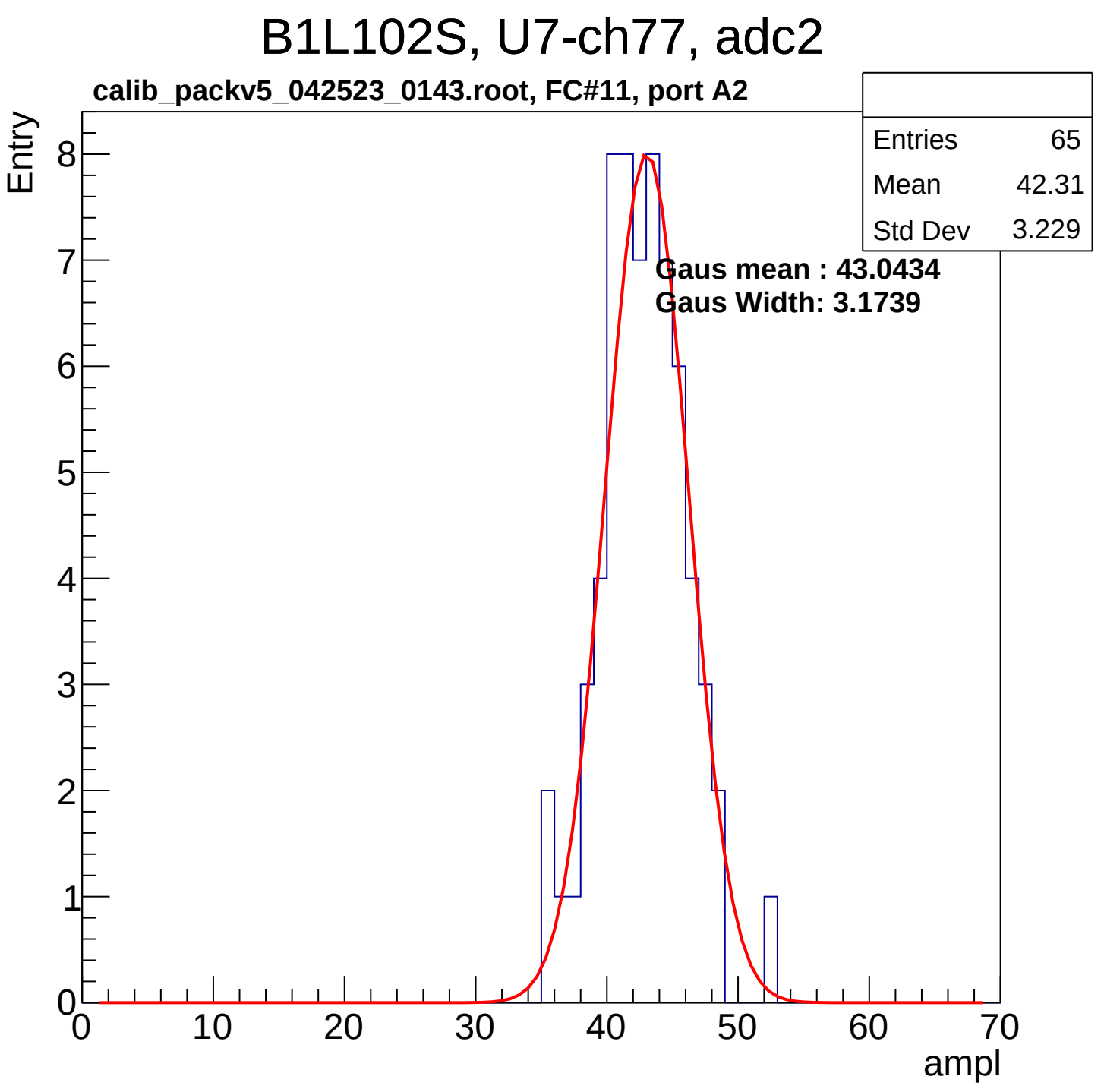
B1L102S, U7-ch77, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 65
Mean 42.31
Std Dev 3.229
Gaus mean : 43.0434
Gaus Width: 3.1739
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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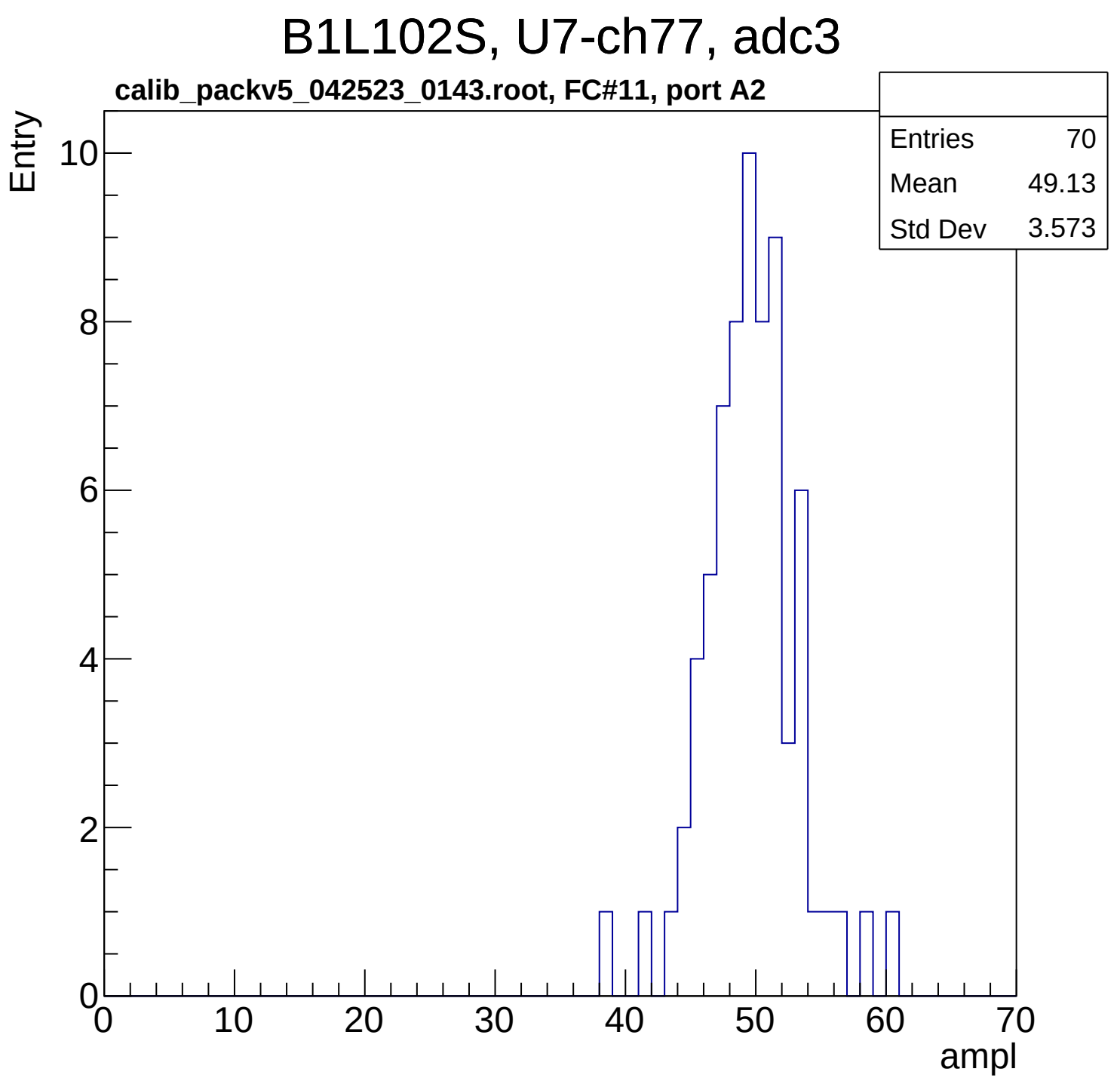
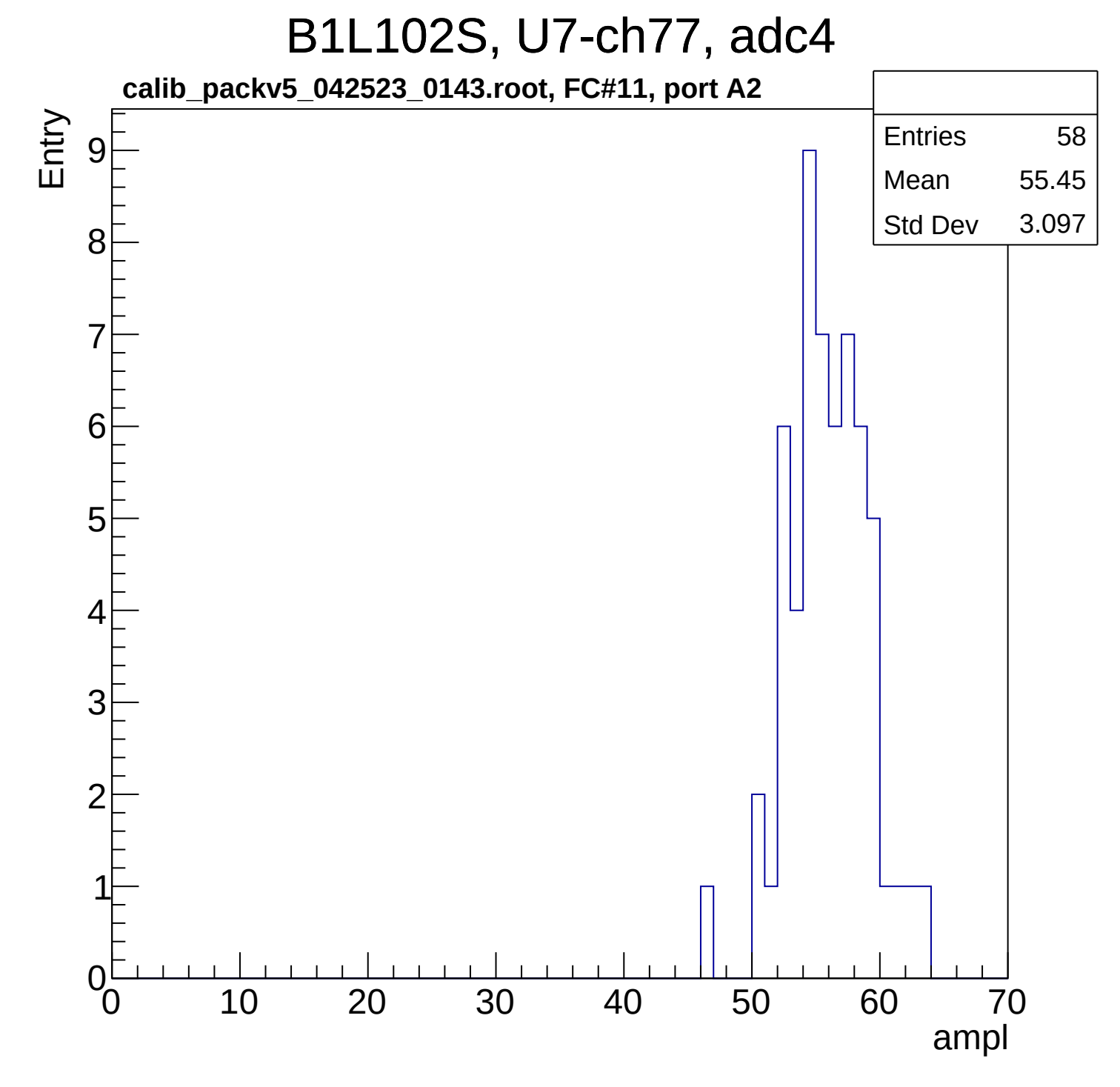
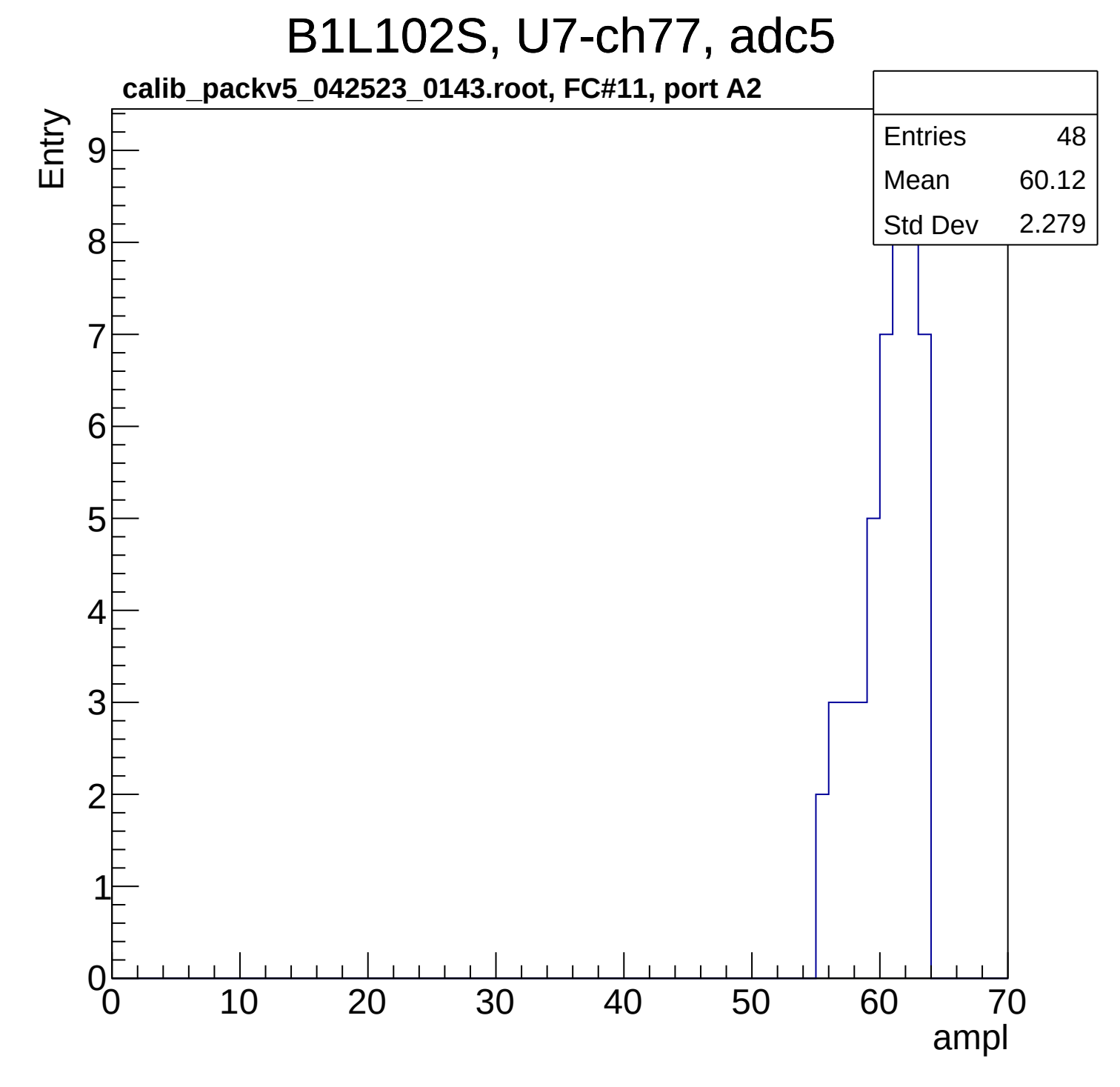

B1L102S, U7-ch77, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 70
Mean 49.13
Std Dev 3.573
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L102S, U7-ch77, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 58
Mean 55.45
Std Dev 3.097
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L102S, U7-ch77, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 48
Mean 60.12
Std Dev 2.279
Entry
ampl
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2
3
4
5
6
7
8
9
0
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60
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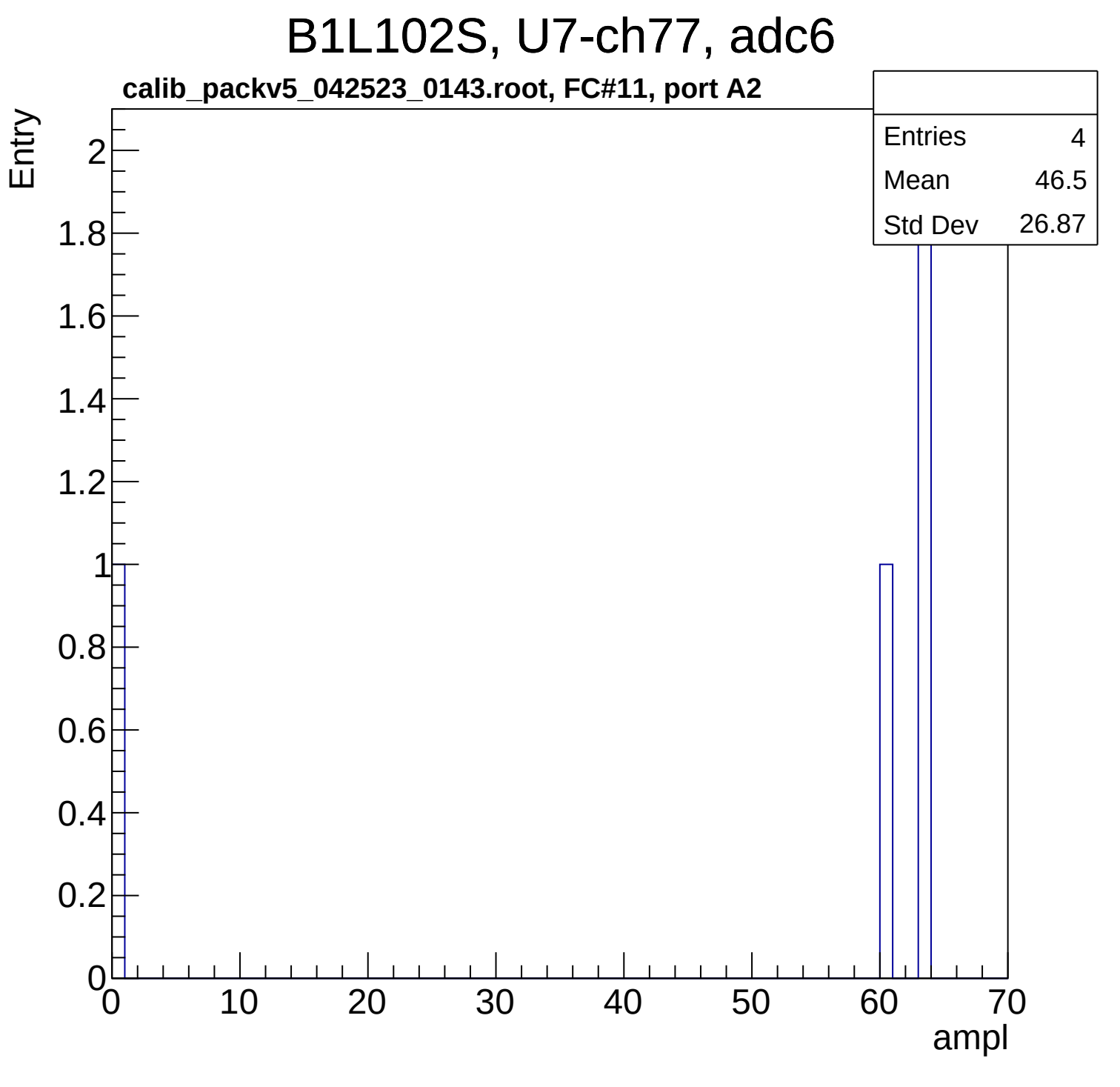
B1L102S, U7-ch77, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 4
Mean 46.5
Std Dev 26.87
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
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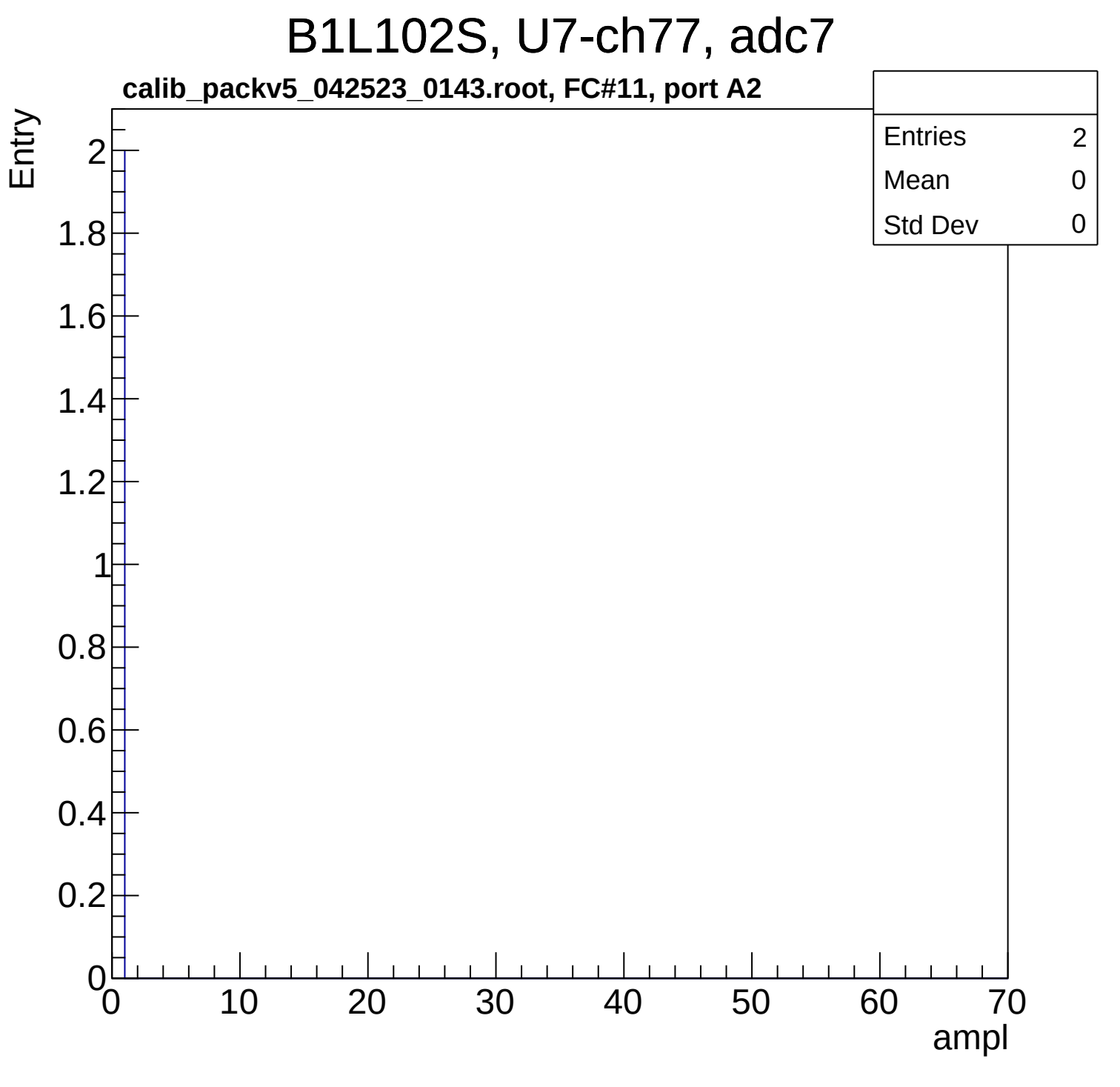
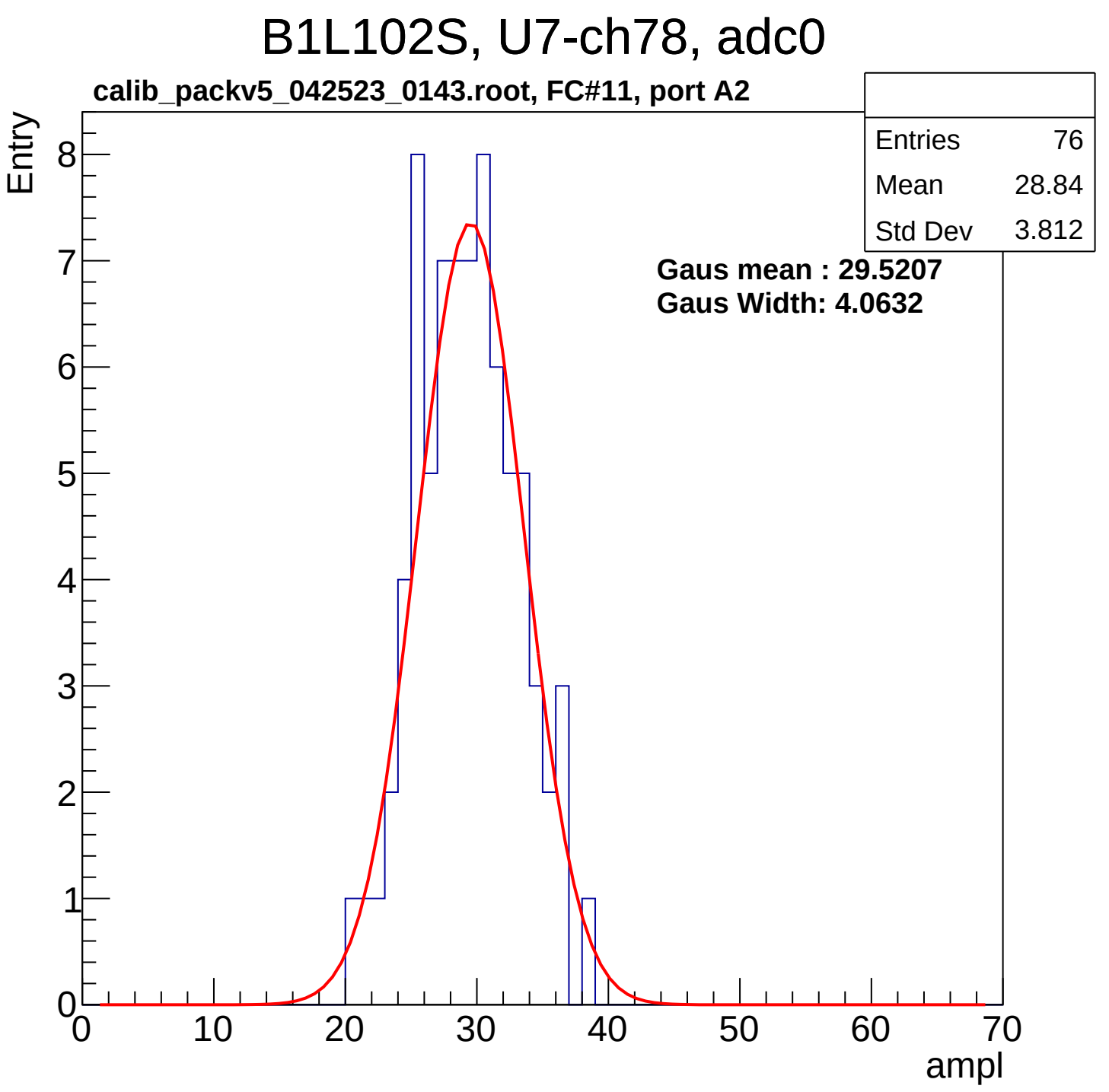
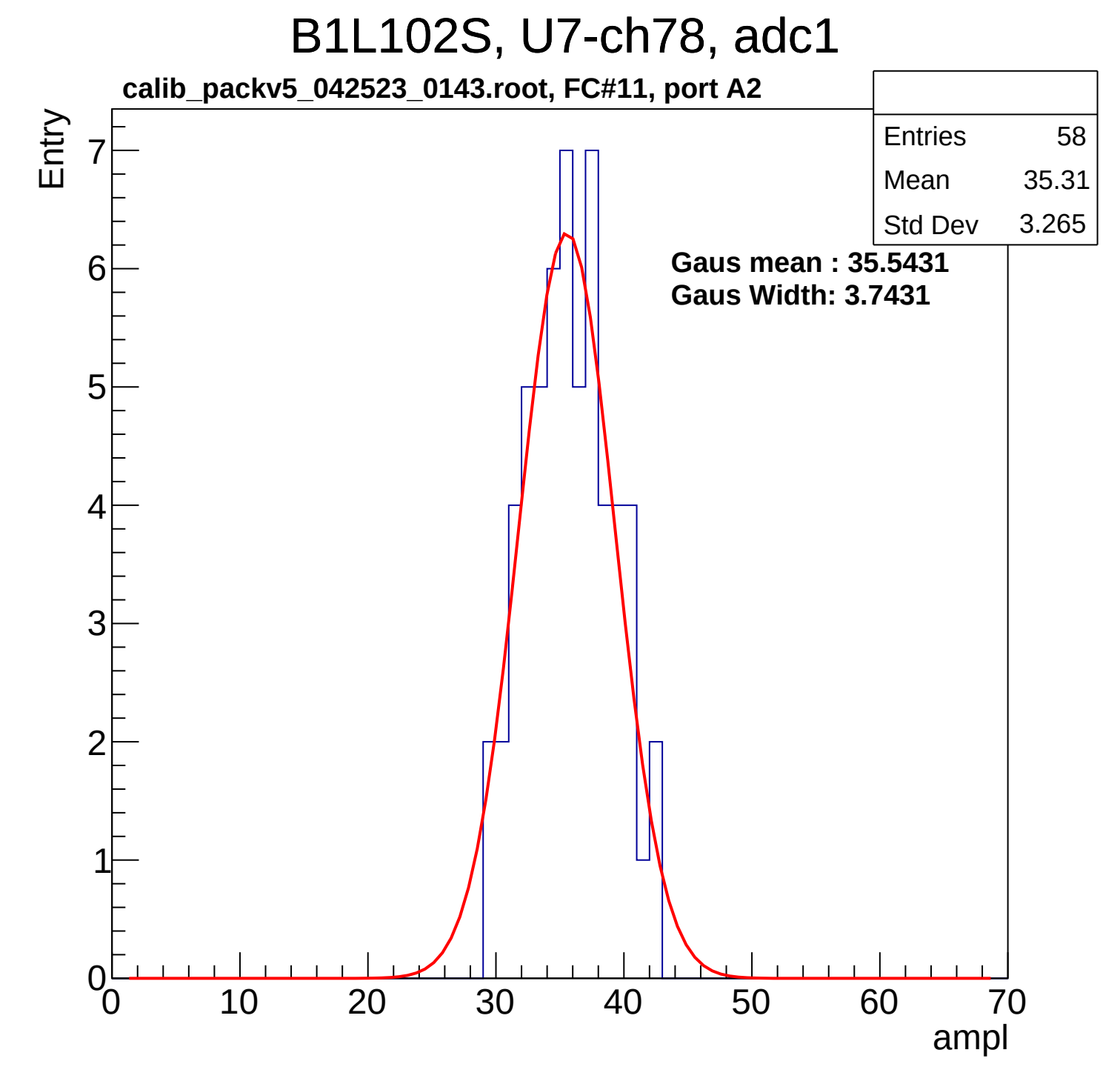
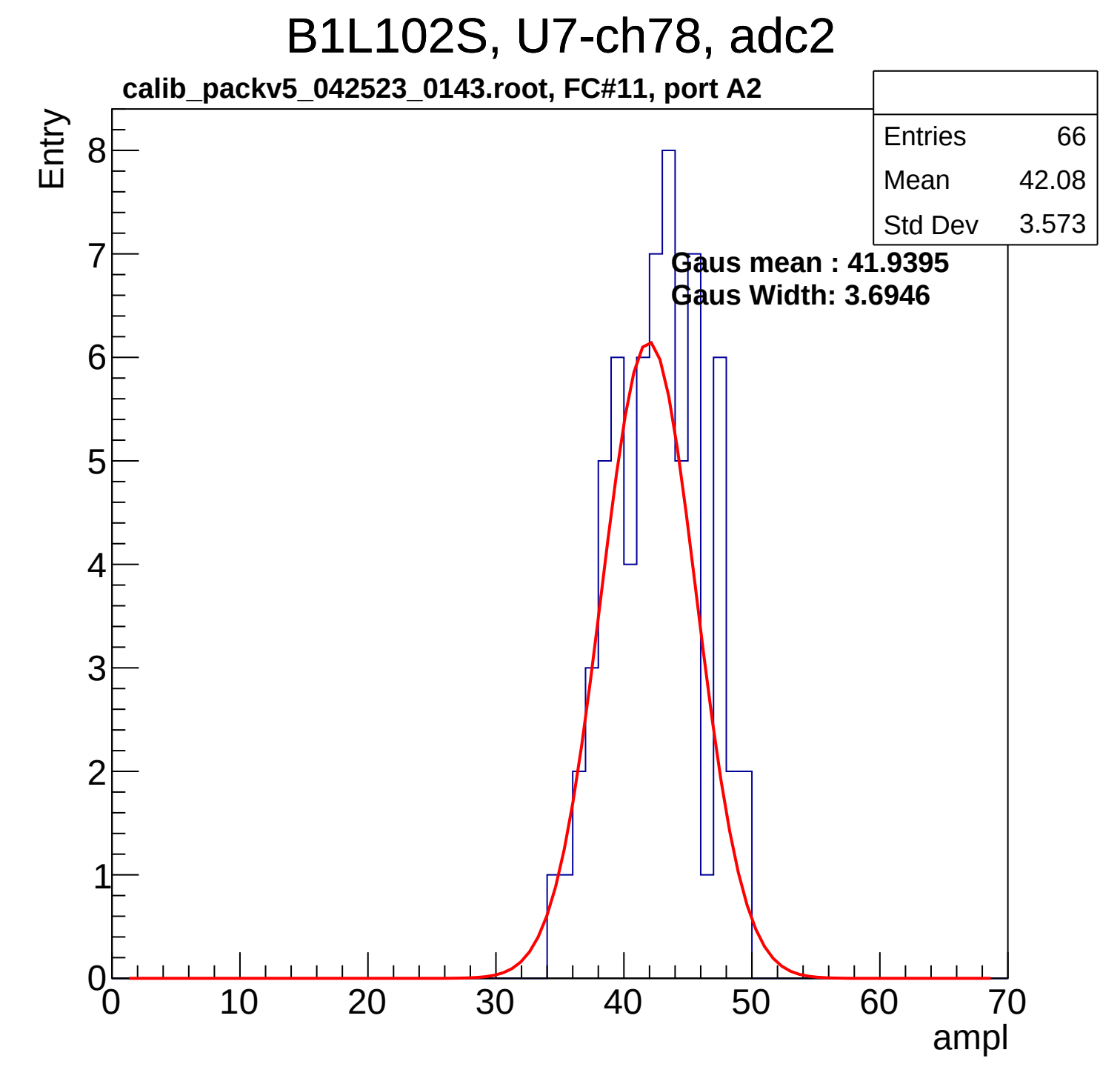

B1L102S, U7-ch77, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 2
Mean 0
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L102S, U7-ch78, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 76
Mean 28.84
Std Dev 3.812
Gaus mean : 29.5207
Gaus Width: 4.0632
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L102S, U7-ch78, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 58
Mean 35.31
Std Dev 3.265
Gaus mean : 35.5431
Gaus Width: 3.7431
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L102S, U7-ch78, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 66
Mean 42.08
Std Dev 3.573
Gaus mean : 41.9395
Gaus Width: 3.6946
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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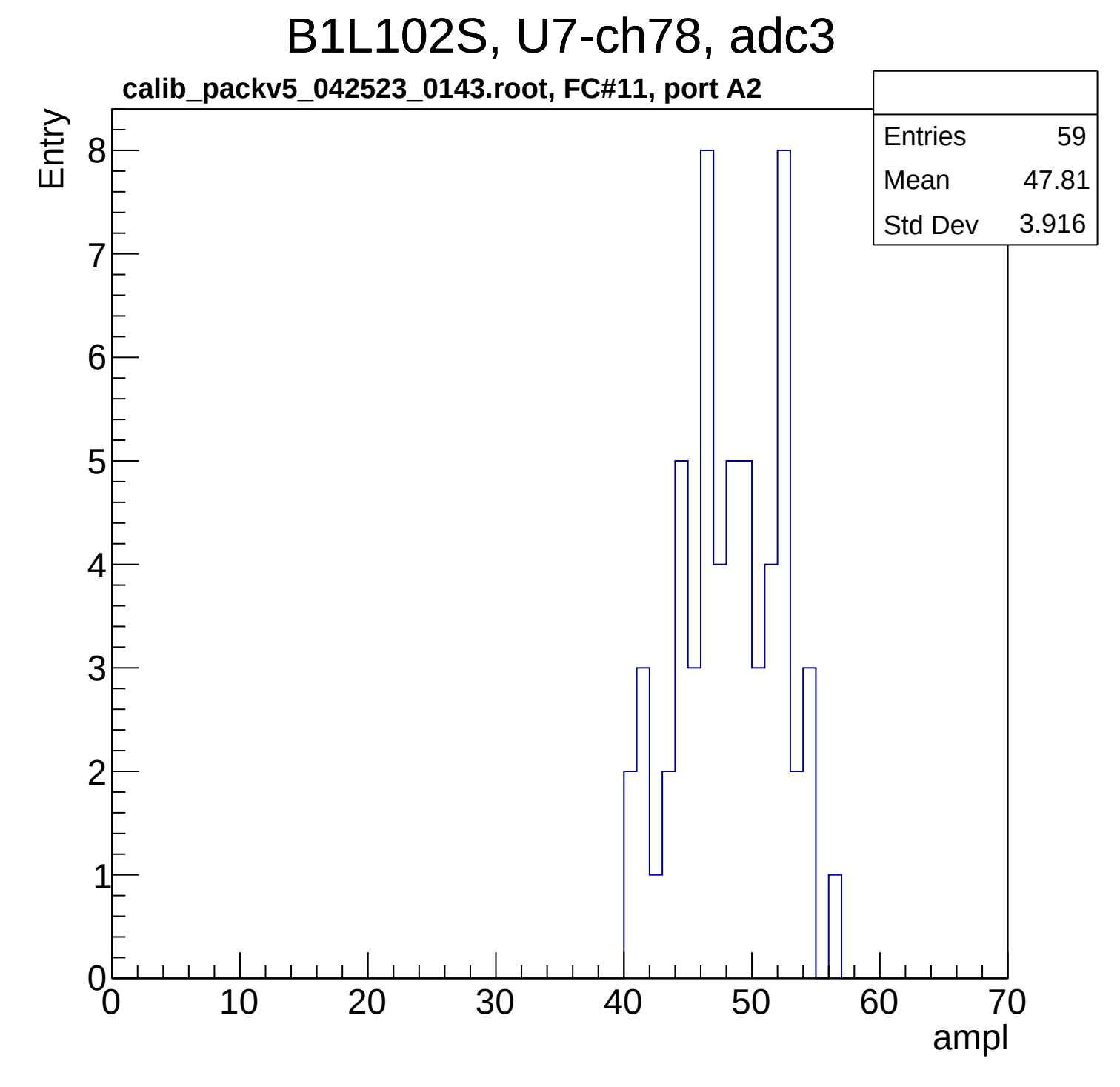
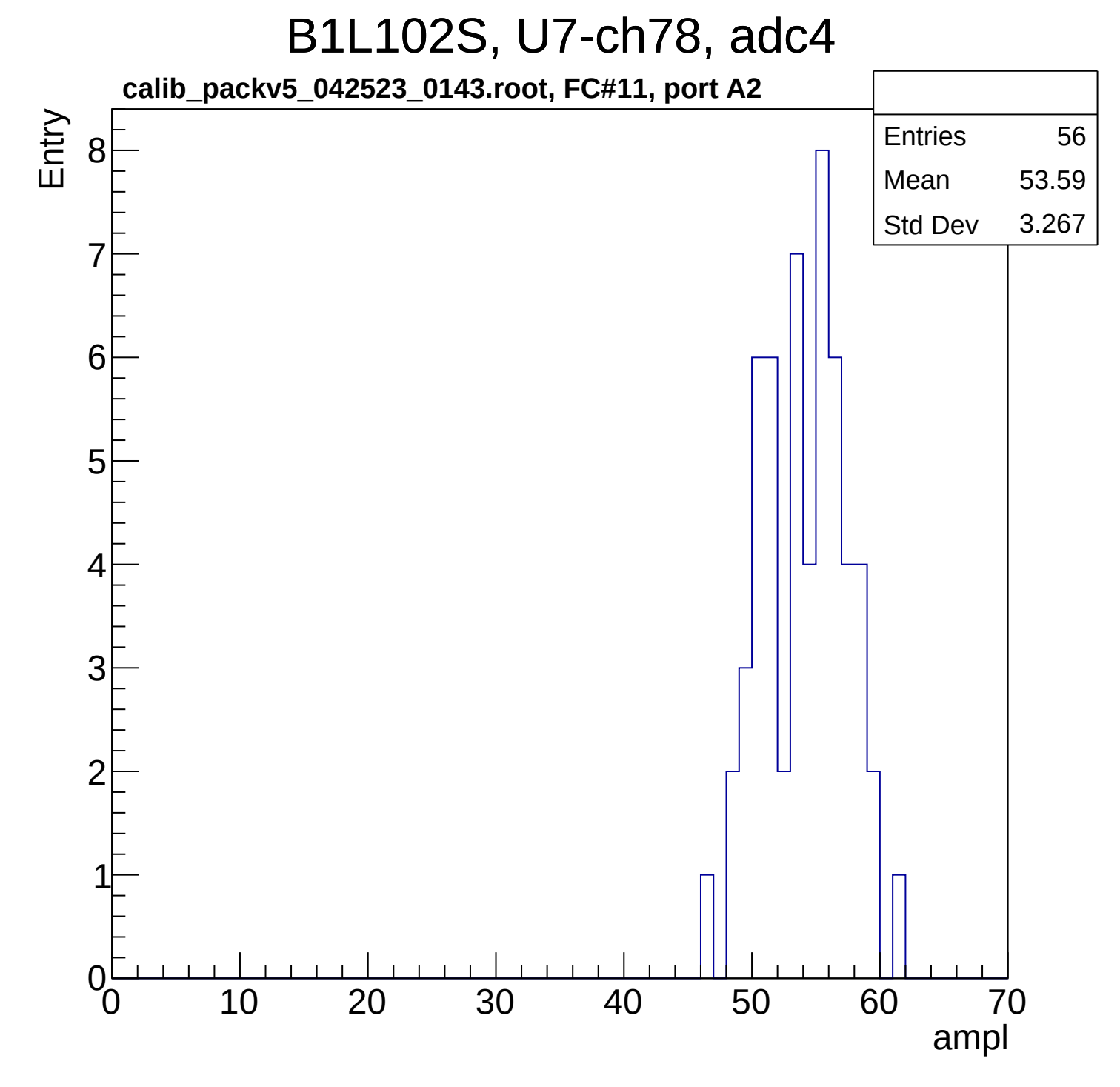

B1L102S, U7-ch78, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 59
Mean 47.81
Std Dev 3.916
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L102S, U7-ch78, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 56
Mean 53.59
Std Dev 3.267
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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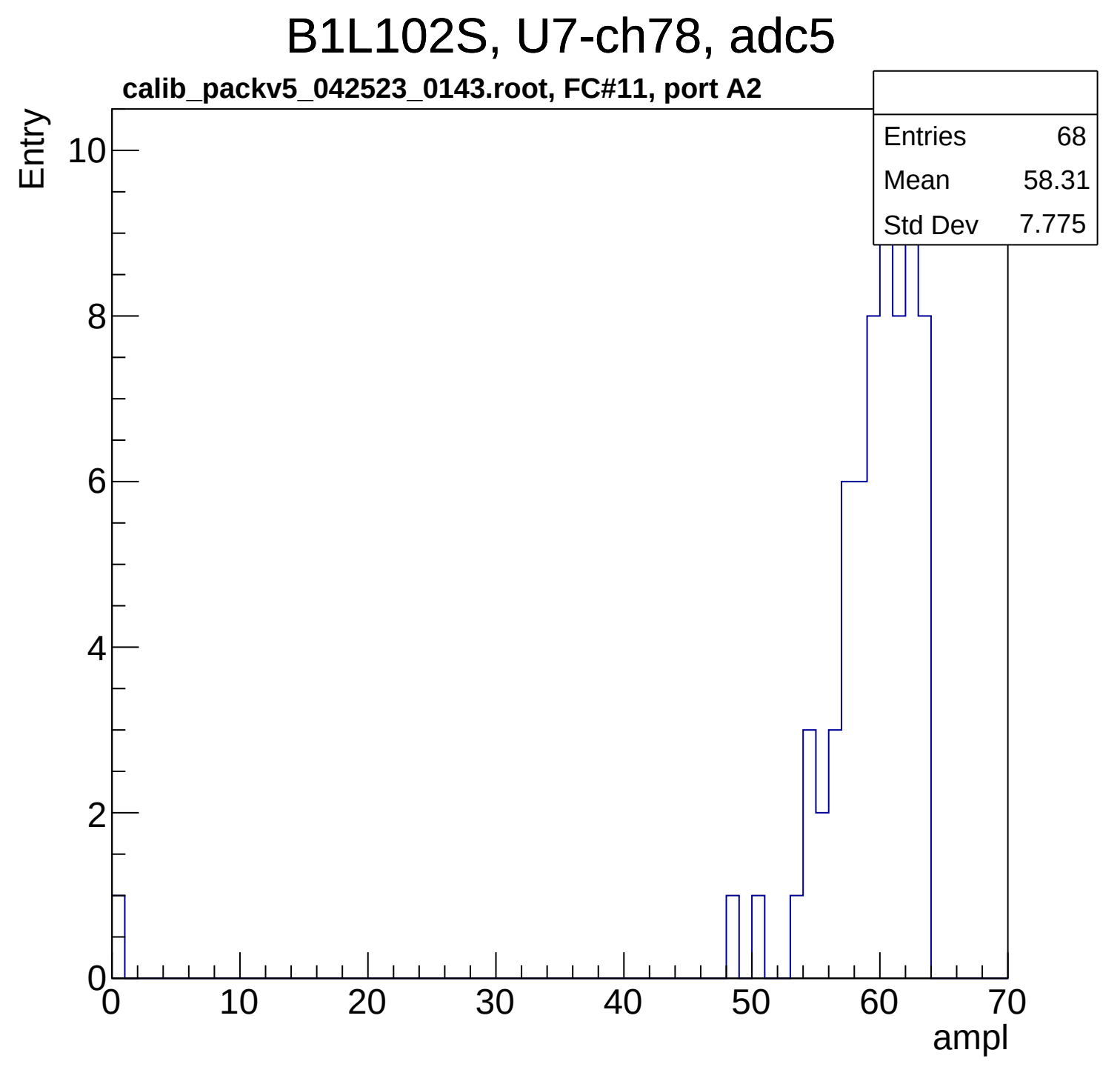
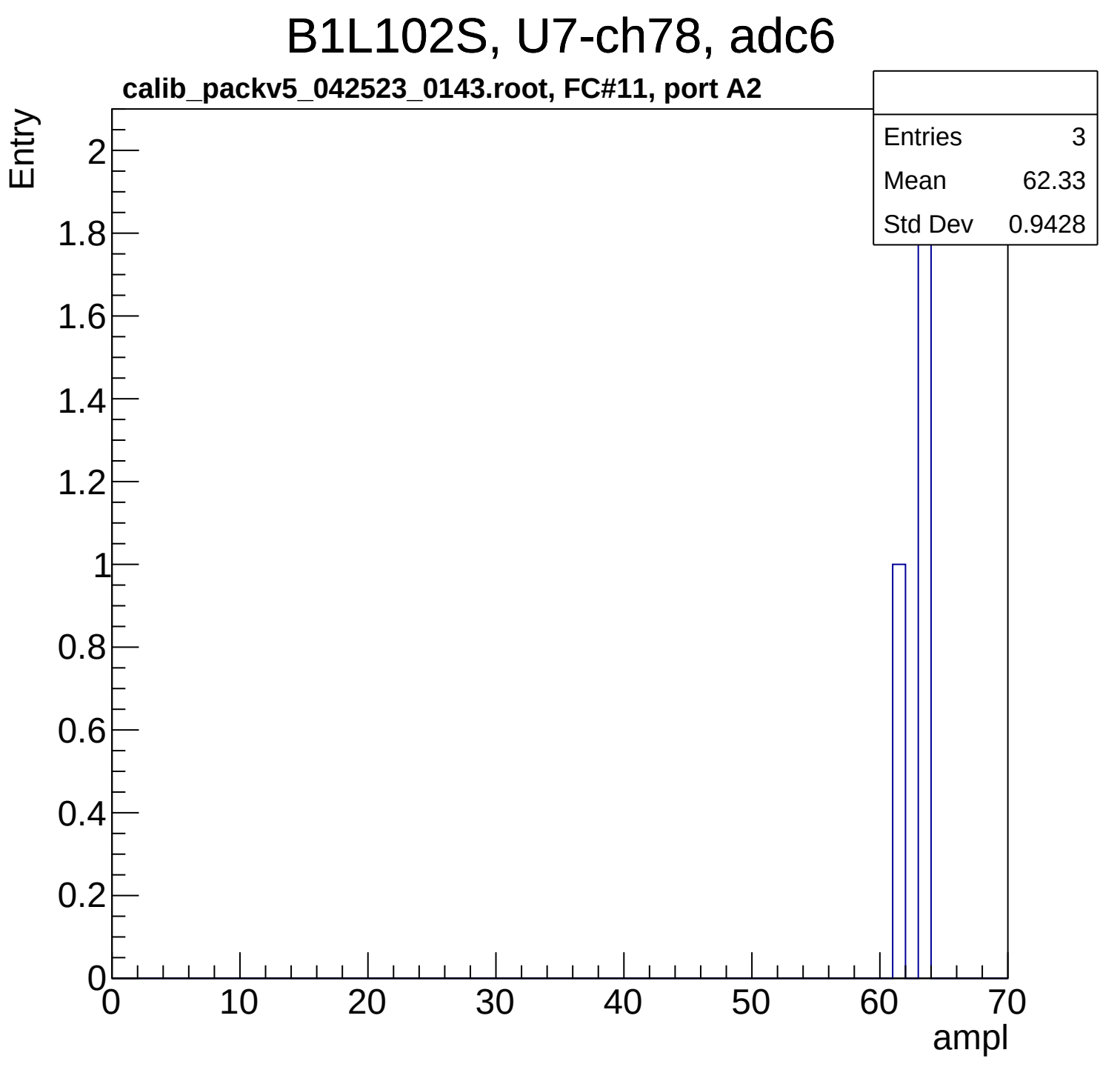
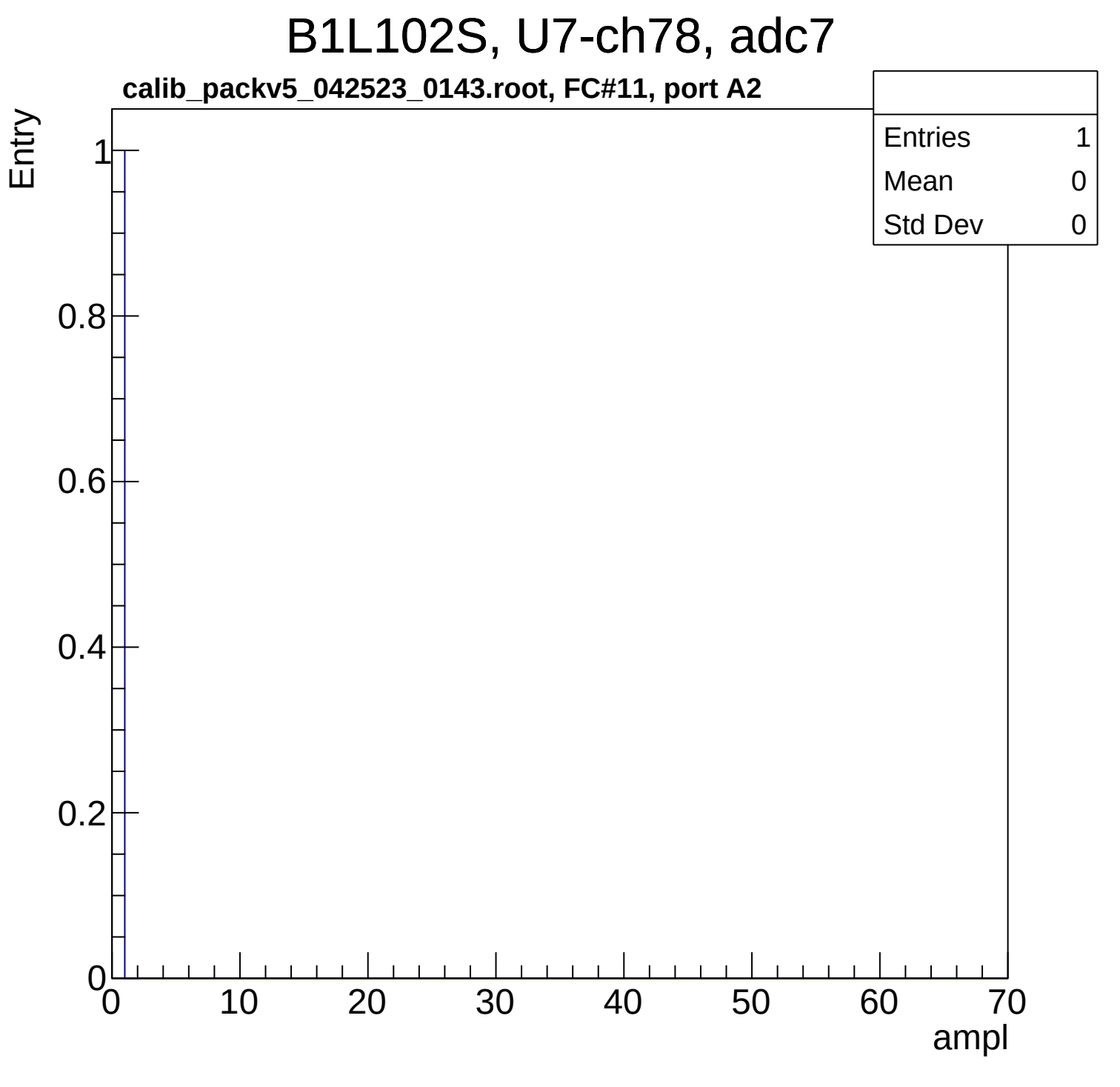
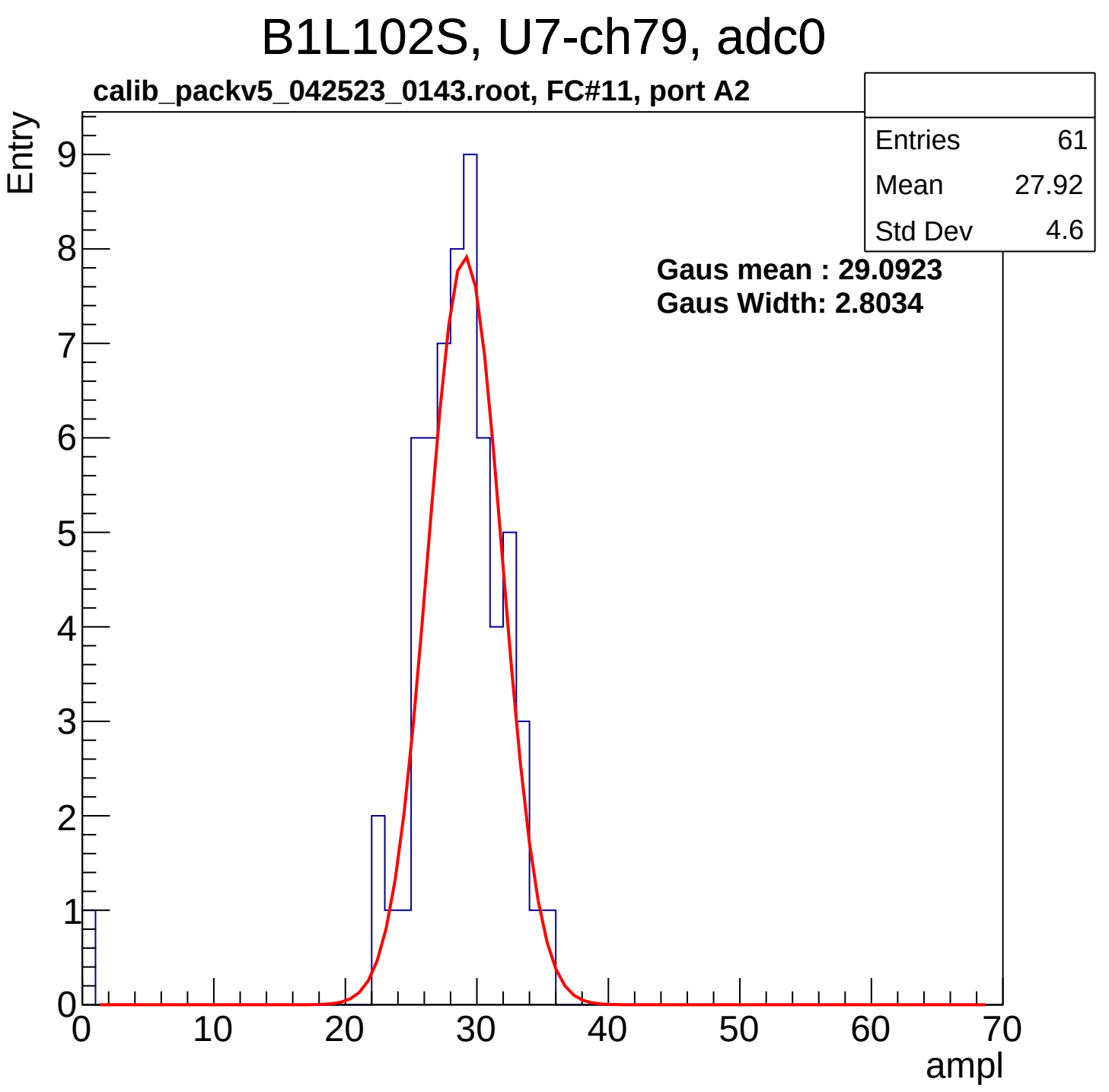
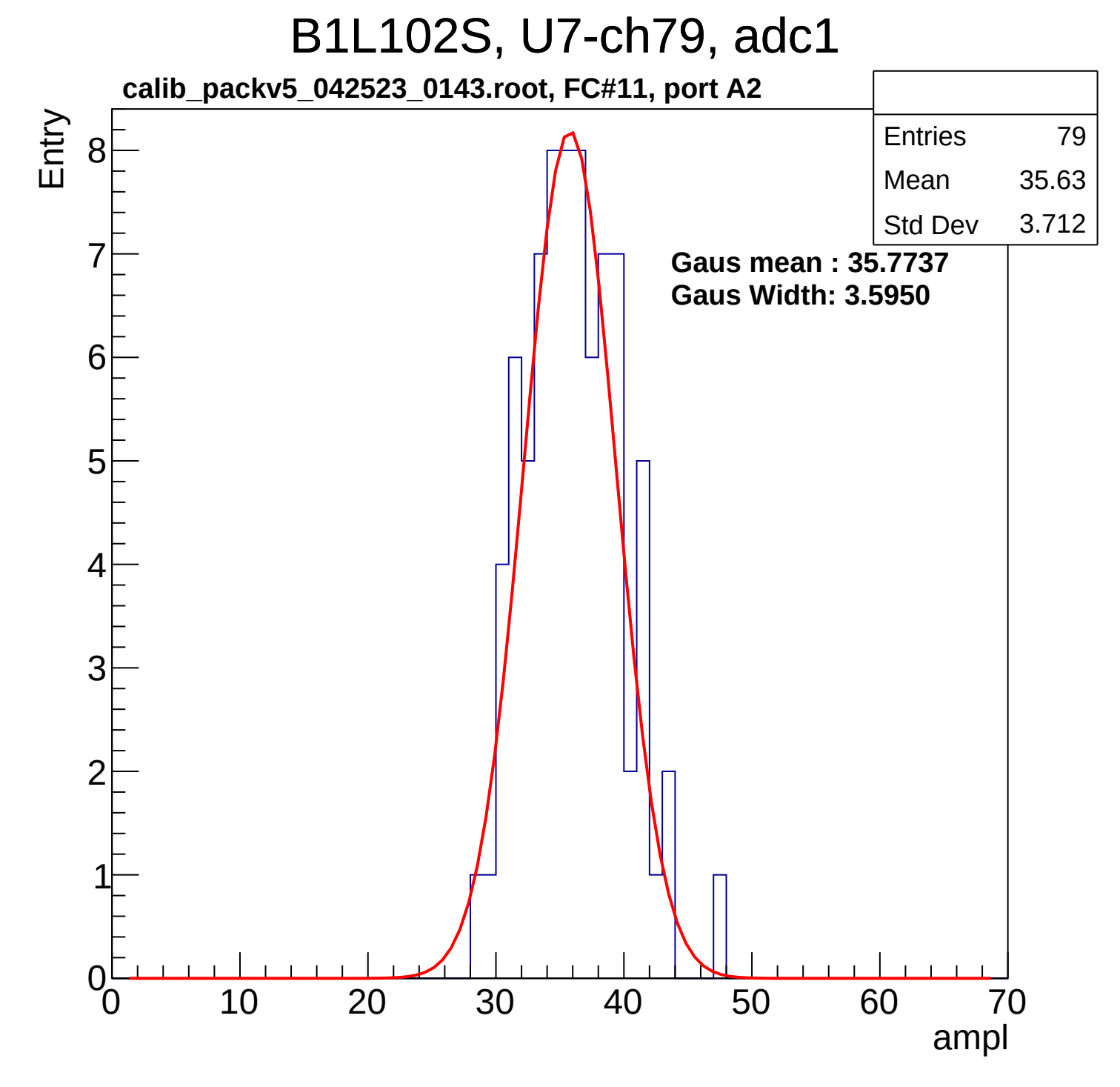
40
50
60
70

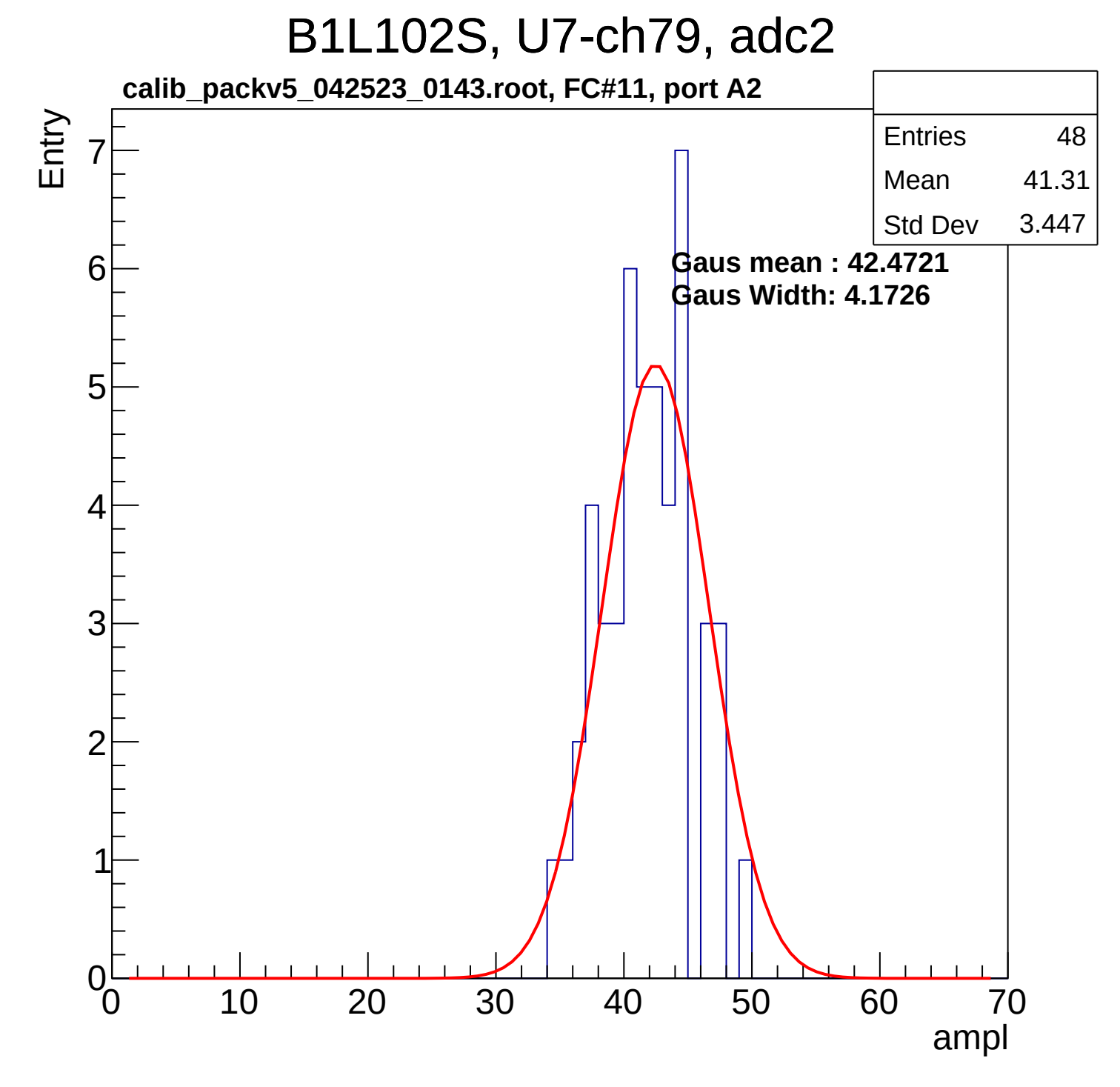

B1L102S, U7-ch78, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 68
Mean 58.31
Std Dev 7.775
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L102S, U7-ch78, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 3
Mean 62.33
Std Dev 0.9428
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L102S, U7-ch78, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U7-ch79, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 61
Mean 27.92
Std Dev 4.6
Gaus mean : 29.0923
Gaus Width: 2.8034
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L102S, U7-ch79, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 79
Mean 35.63
Std Dev 3.712
Gaus mean : 35.7737
Gaus Width: 3.5950
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L102S, U7-ch79, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 48
Mean 41.31
Std Dev 3.447
Gaus mean : 42.4721
Gaus Width: 4.1726
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
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40
50
60
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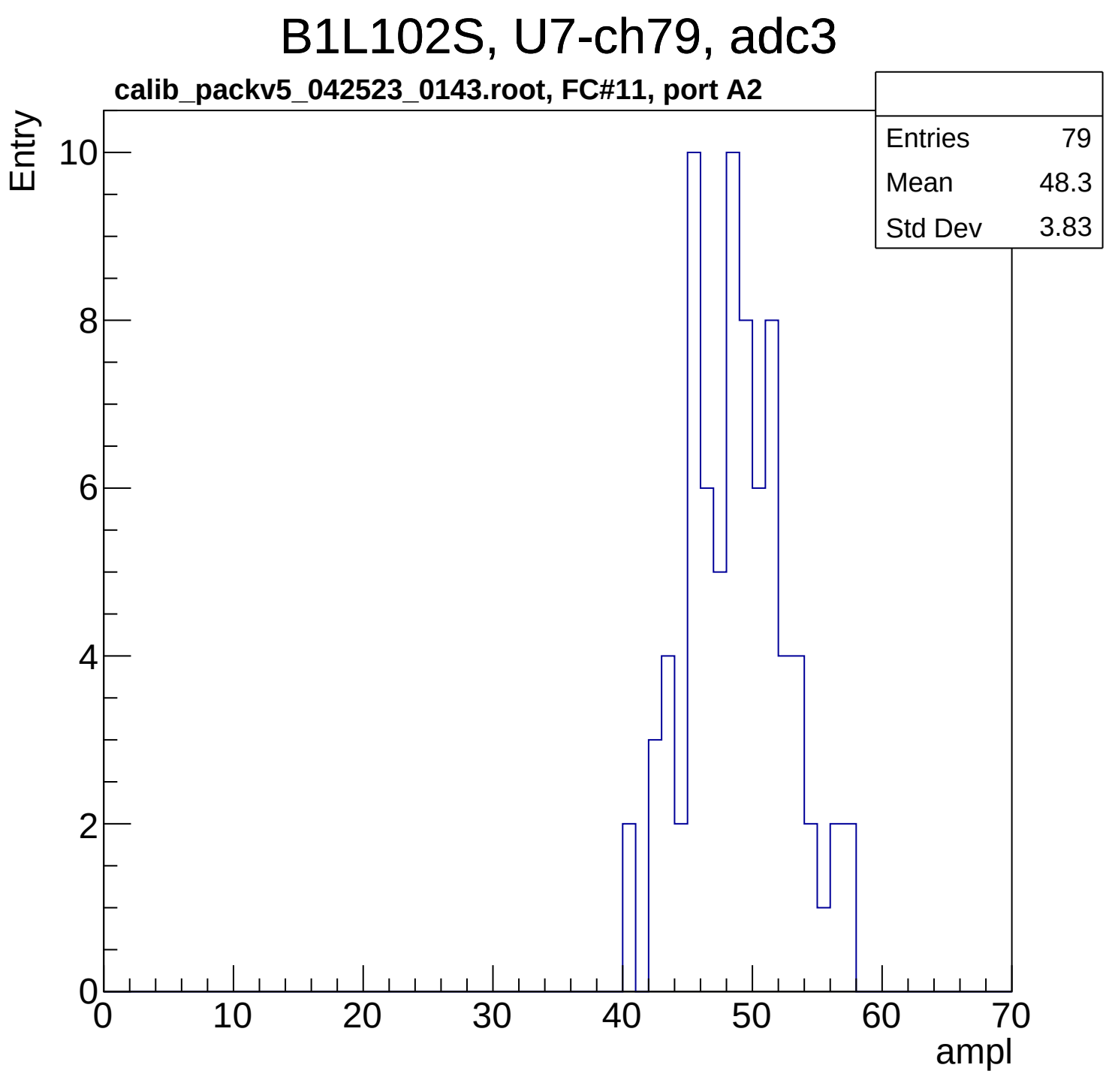
B1L102S, U7-ch79, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 79
Mean 48.3
Std Dev 3.83
Entry
ampl
0
2
4
6
8
10
0
10
20
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40
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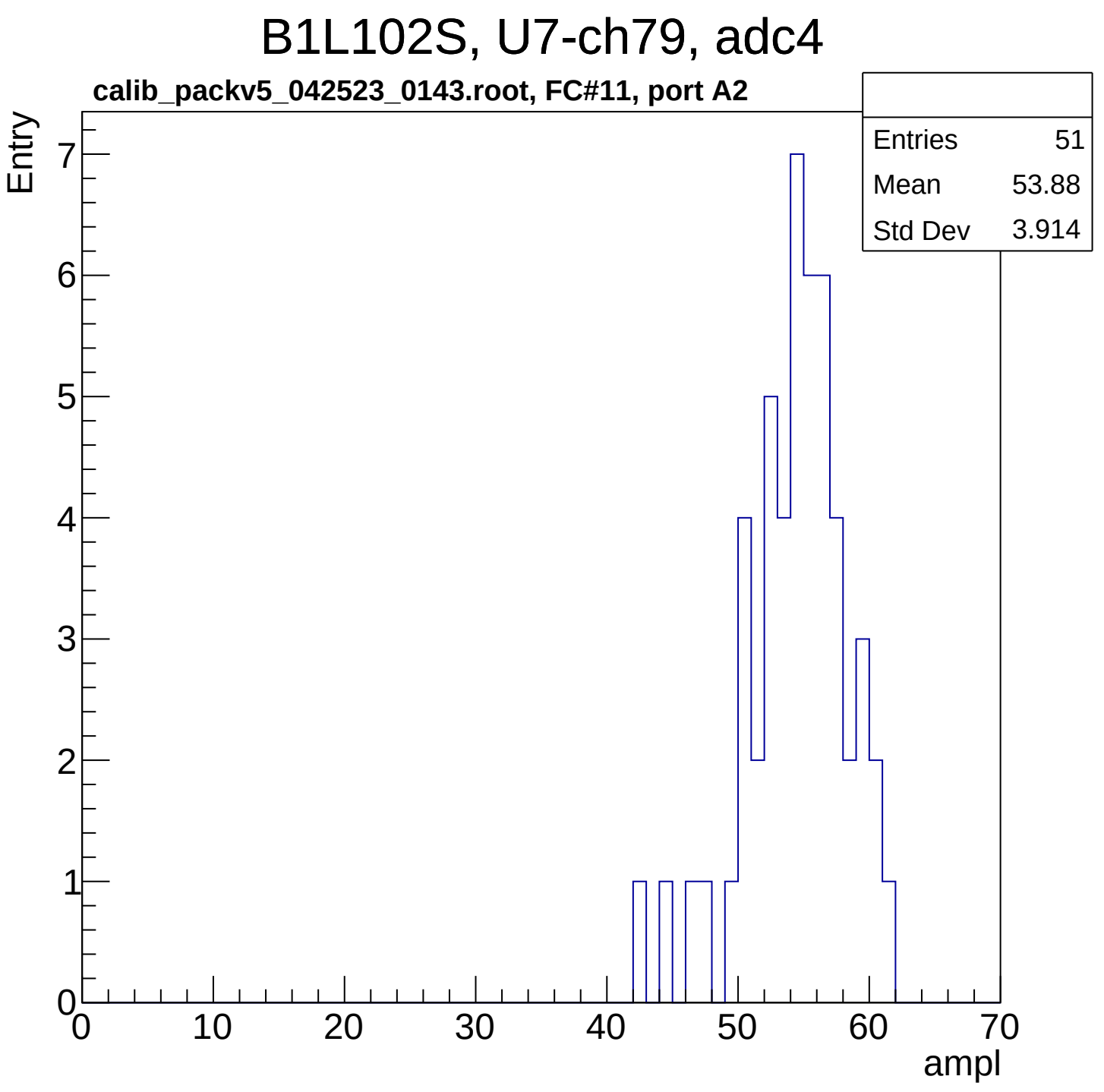
60
70


B1L102S, U7-ch79, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 51
Mean 53.88
Std Dev 3.914
Entry
ampl
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1
2
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4
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6
7
0
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20
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40
50
60
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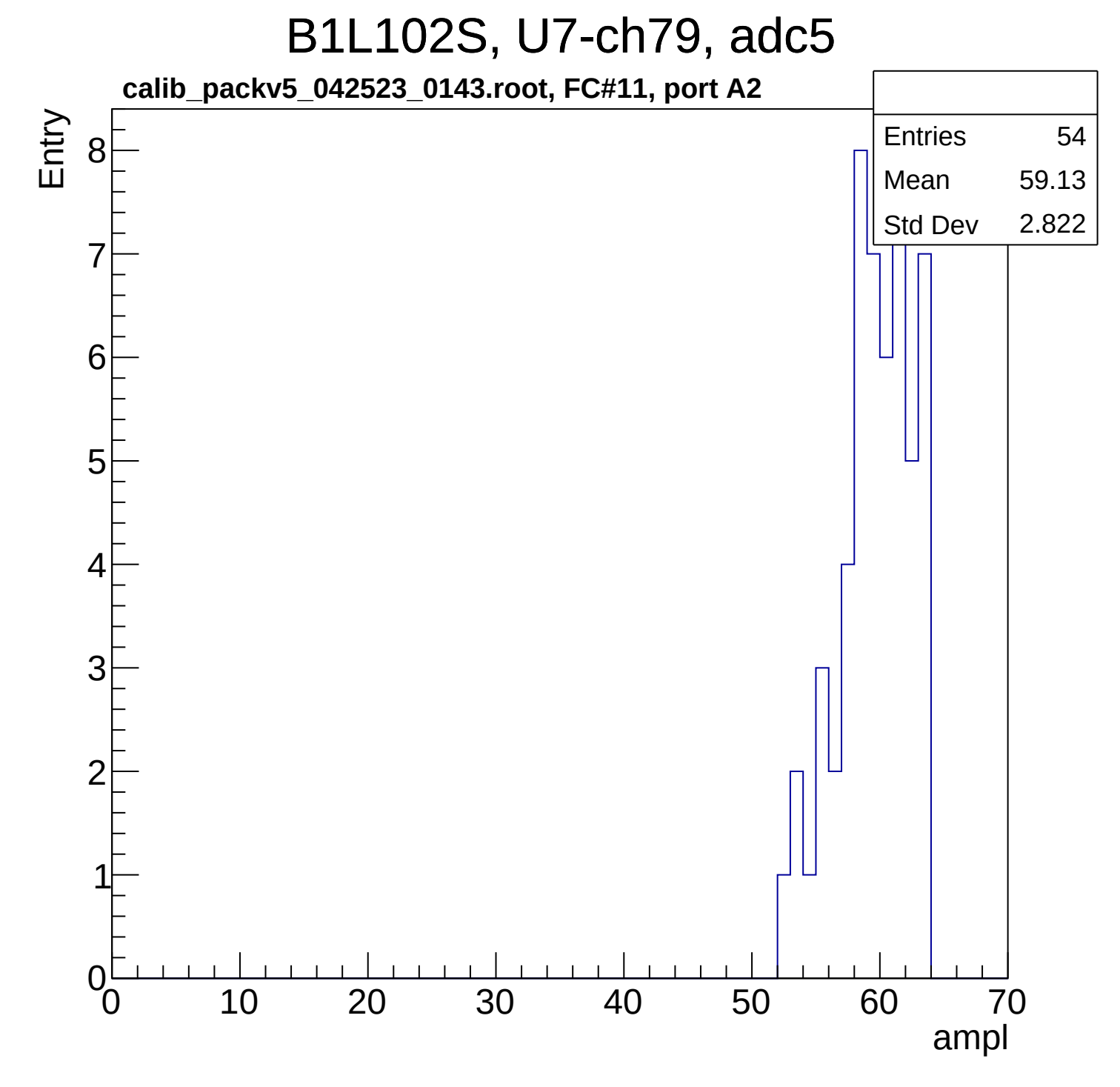
B1L102S, U7-ch79, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 54
Mean 59.13
Std Dev 2.822
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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40
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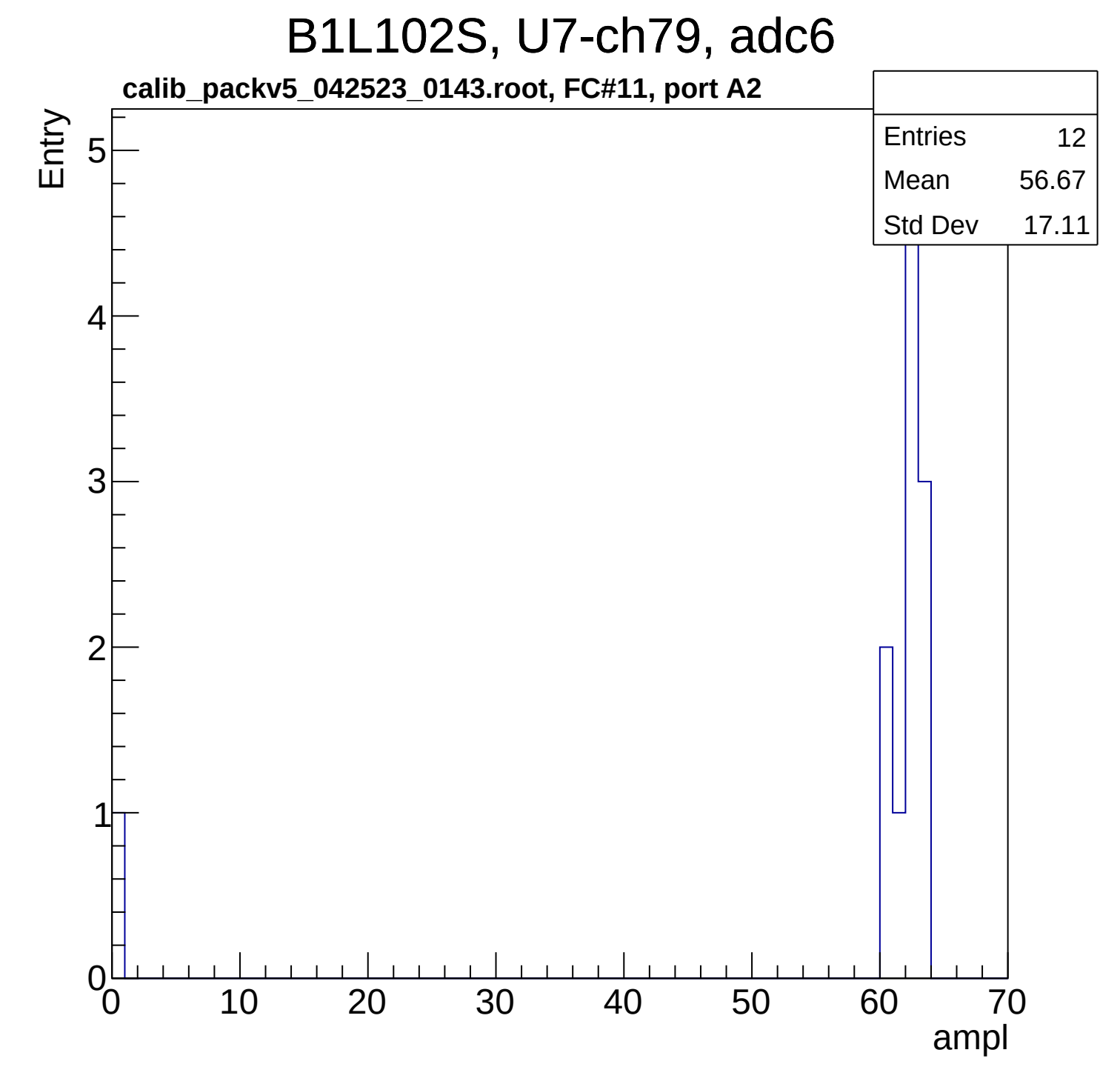
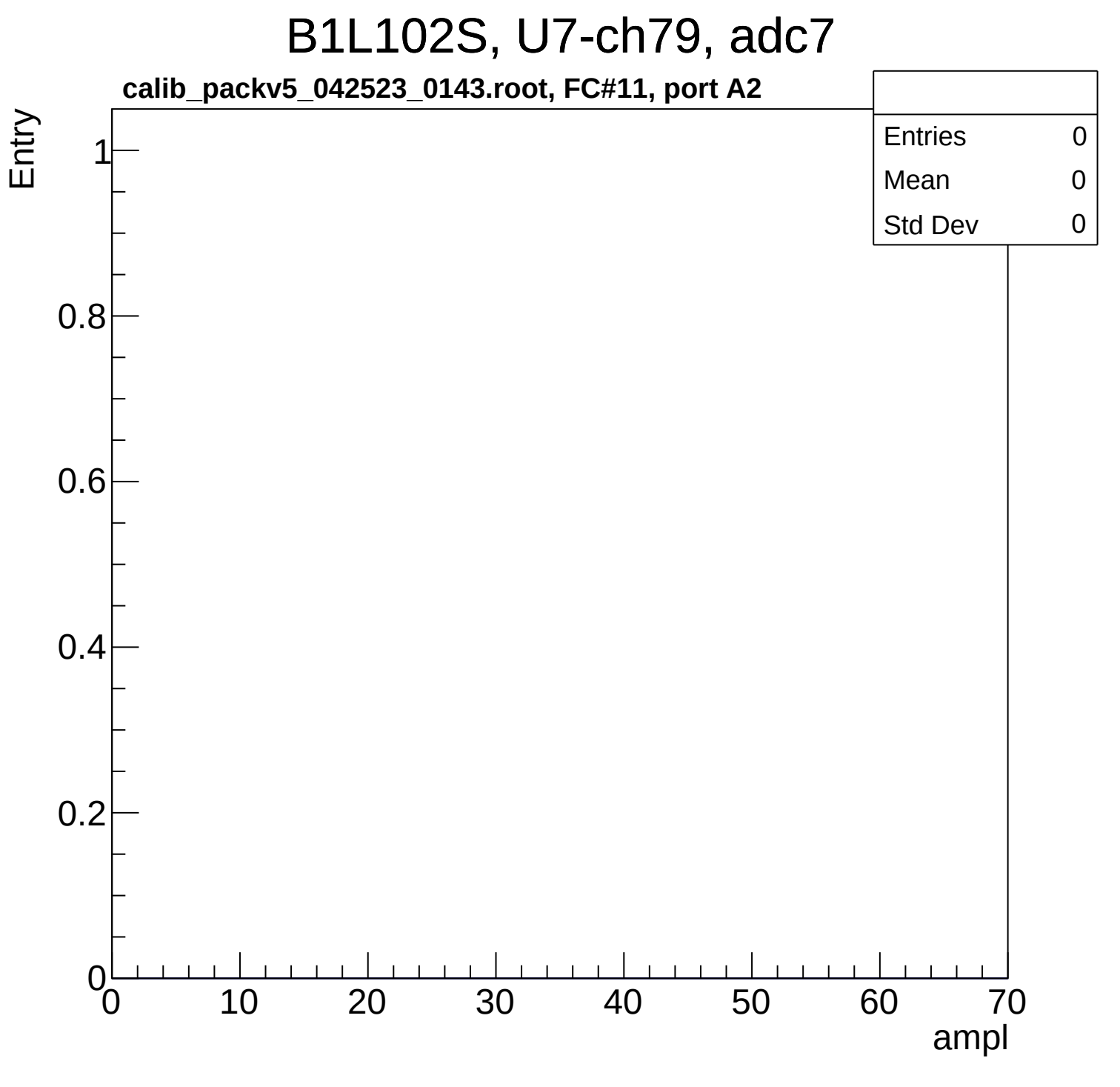
60
70


B1L102S, U7-ch79, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 12
Mean 56.67
Std Dev 17.11
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L102S, U7-ch79, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 0
Mean 0
Std Dev 0
Entry
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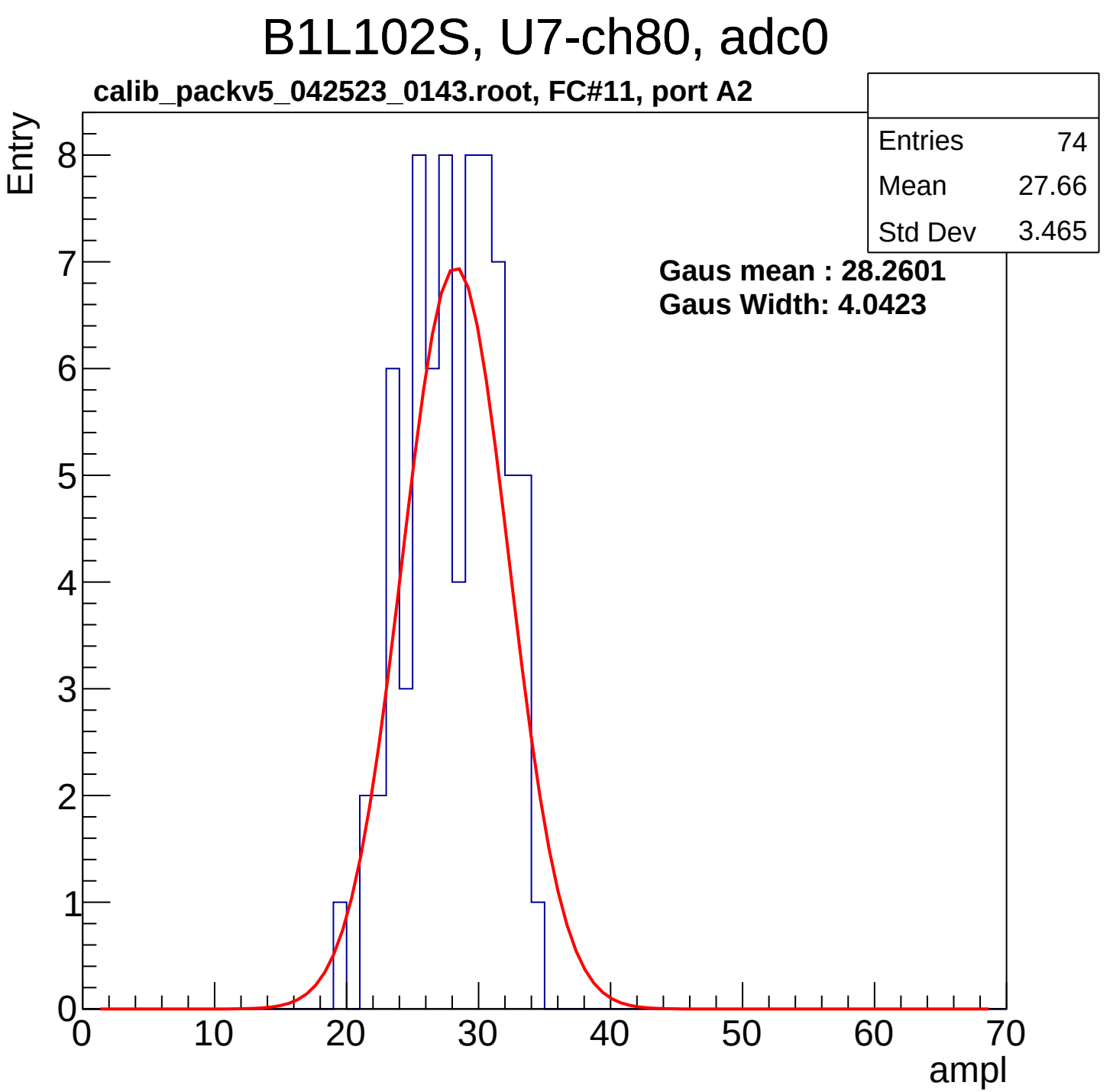
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U7-ch80, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 74
Mean 27.66
Std Dev 3.465
Gaus mean : 28.2601
Gaus Width: 4.0423
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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40
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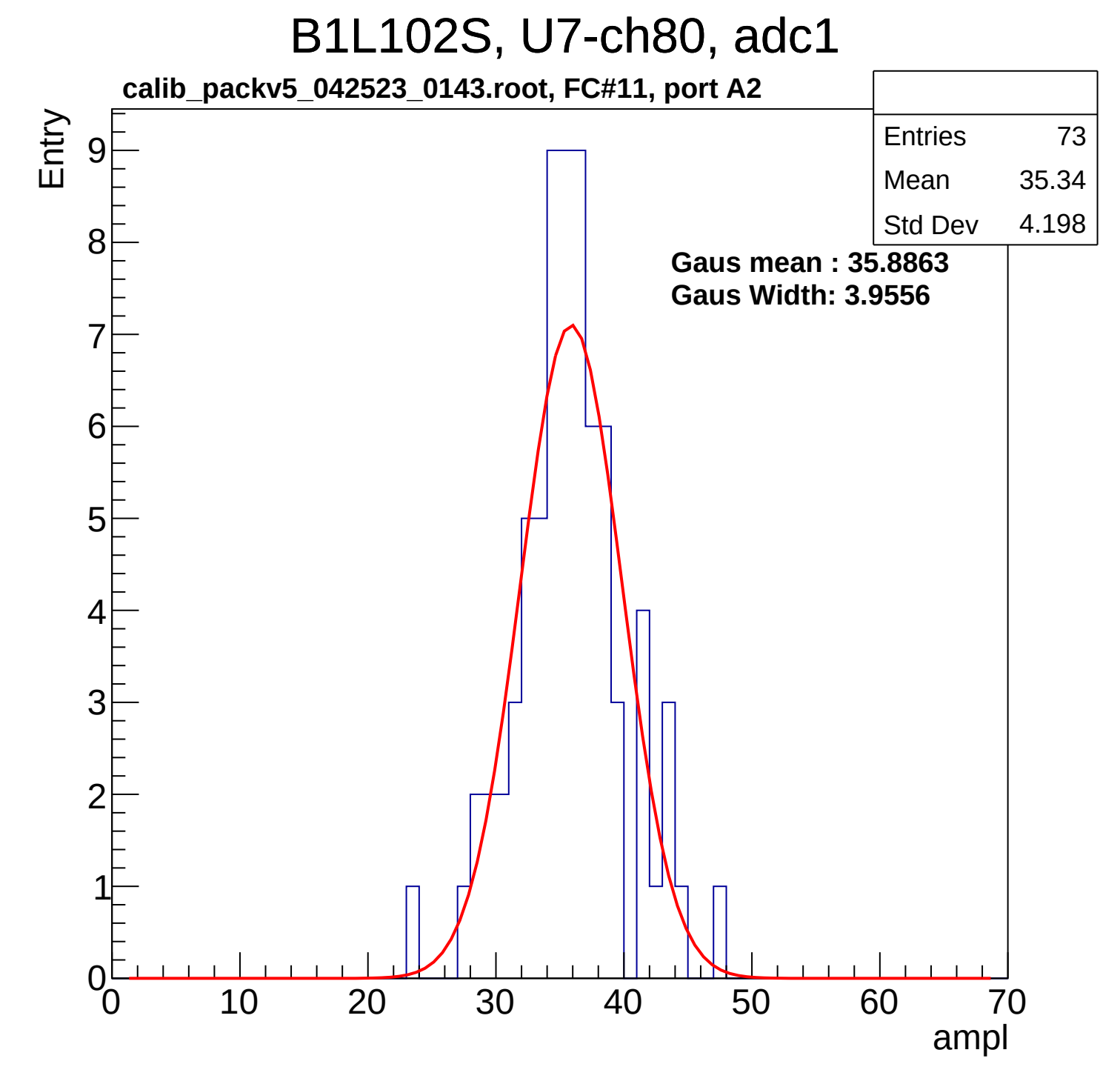
60
70


B1L102S, U7-ch80, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 73
Mean 35.34
Std Dev 4.198
Gaus mean : 35.8863
Gaus Width: 3.9556
Entry
ampl
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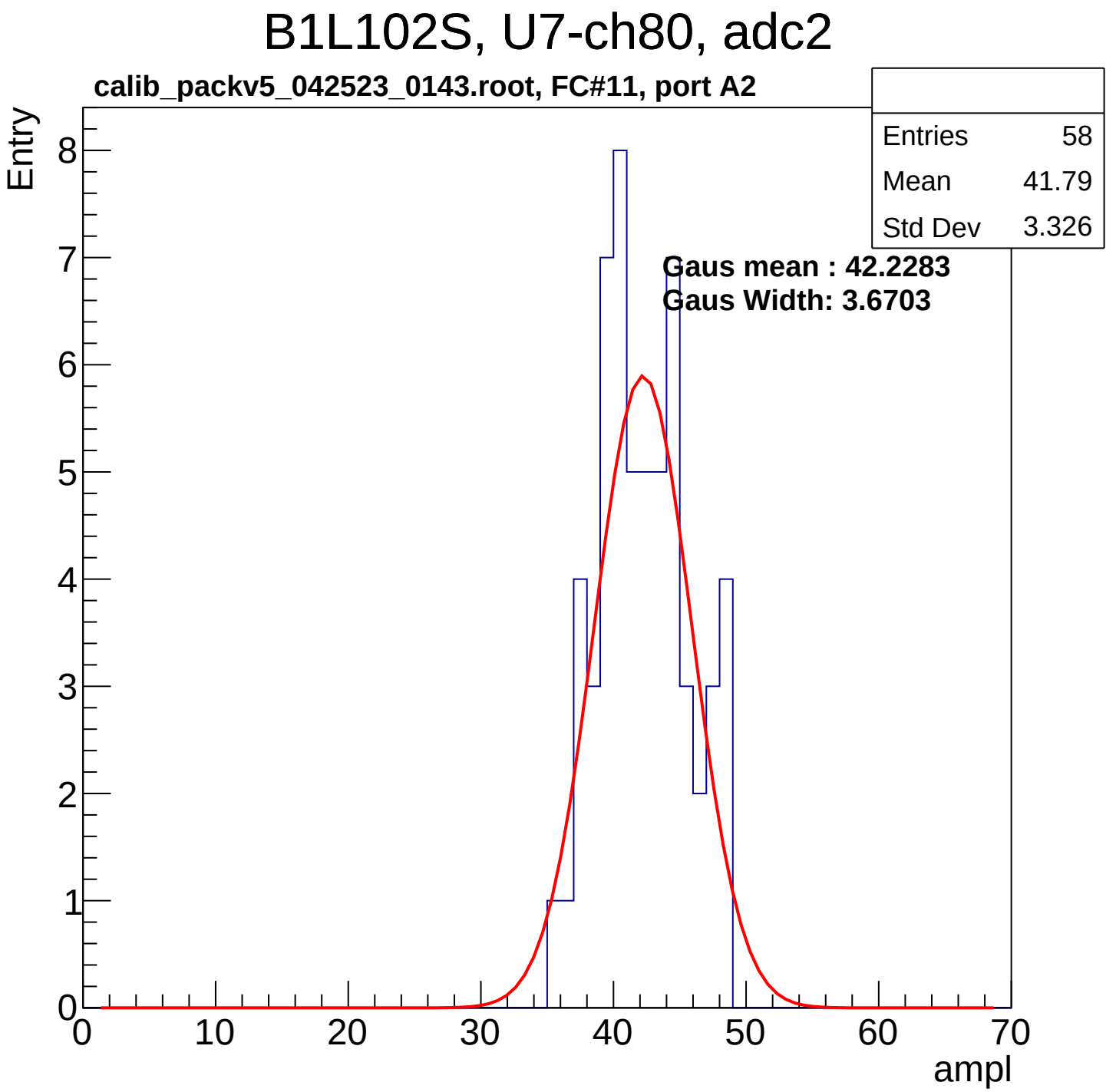
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9


B1L102S, U7-ch80, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 58
Mean 41.79
Std Dev 3.326
Gaus mean : 42.2283
Gaus Width: 3.6703
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
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40
50
60
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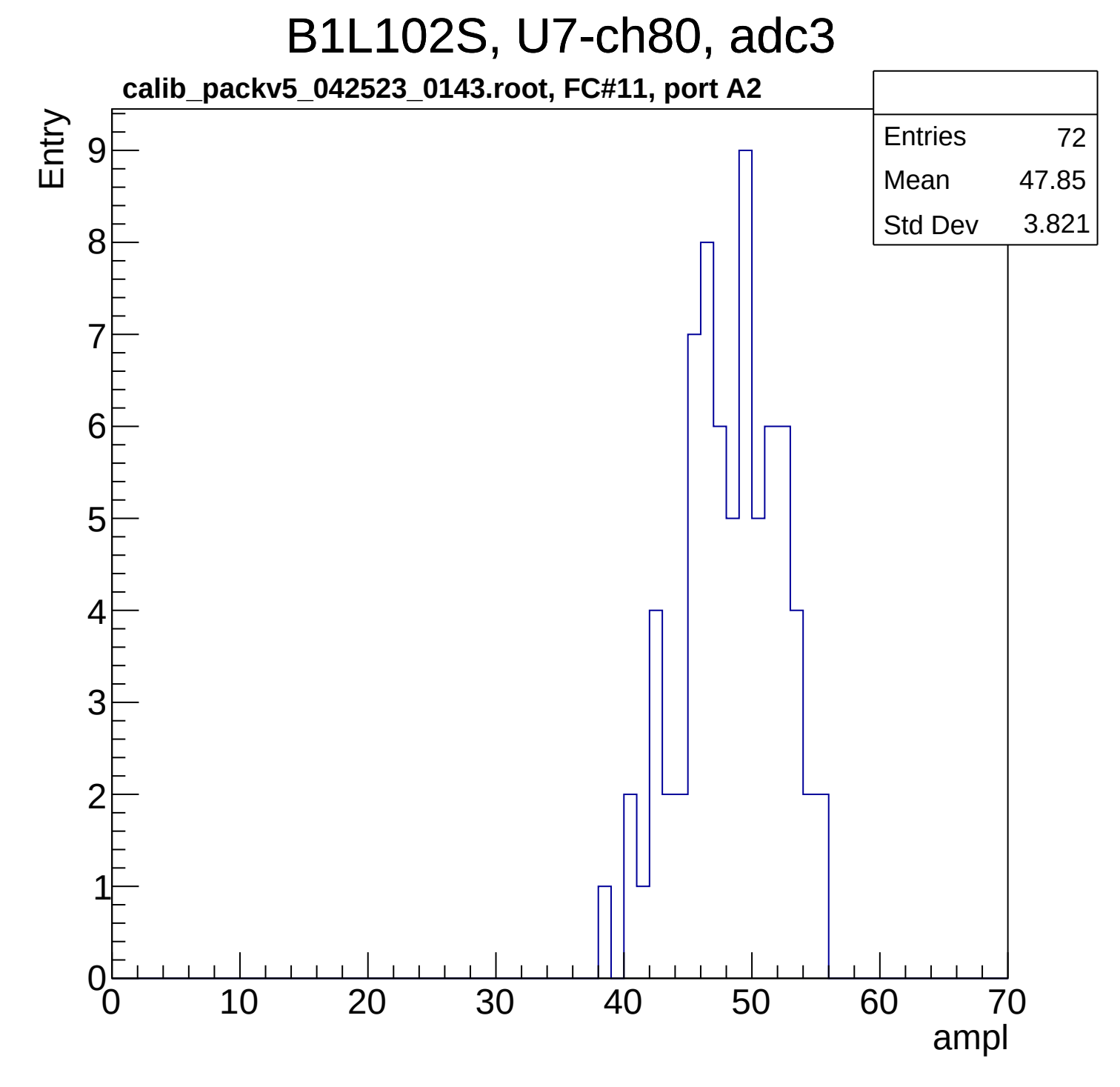
B1L102S, U7-ch80, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 72
Mean 47.85
Std Dev 3.821
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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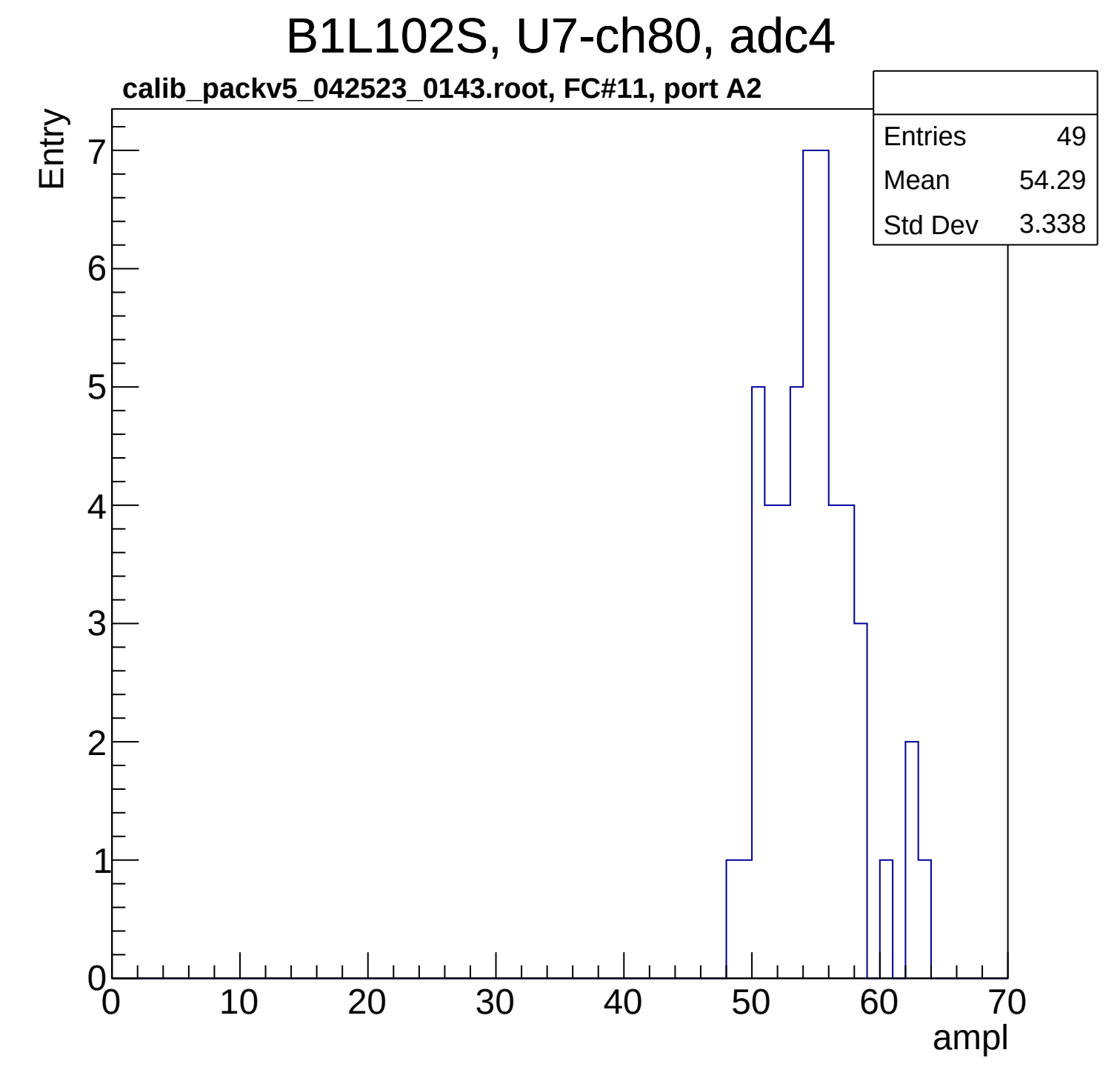
B1L102S, U7-ch80, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 49
Mean 54.29
Std Dev 3.338
Entry
ampl
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2
3
4
5
6
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0
10
20
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40
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60
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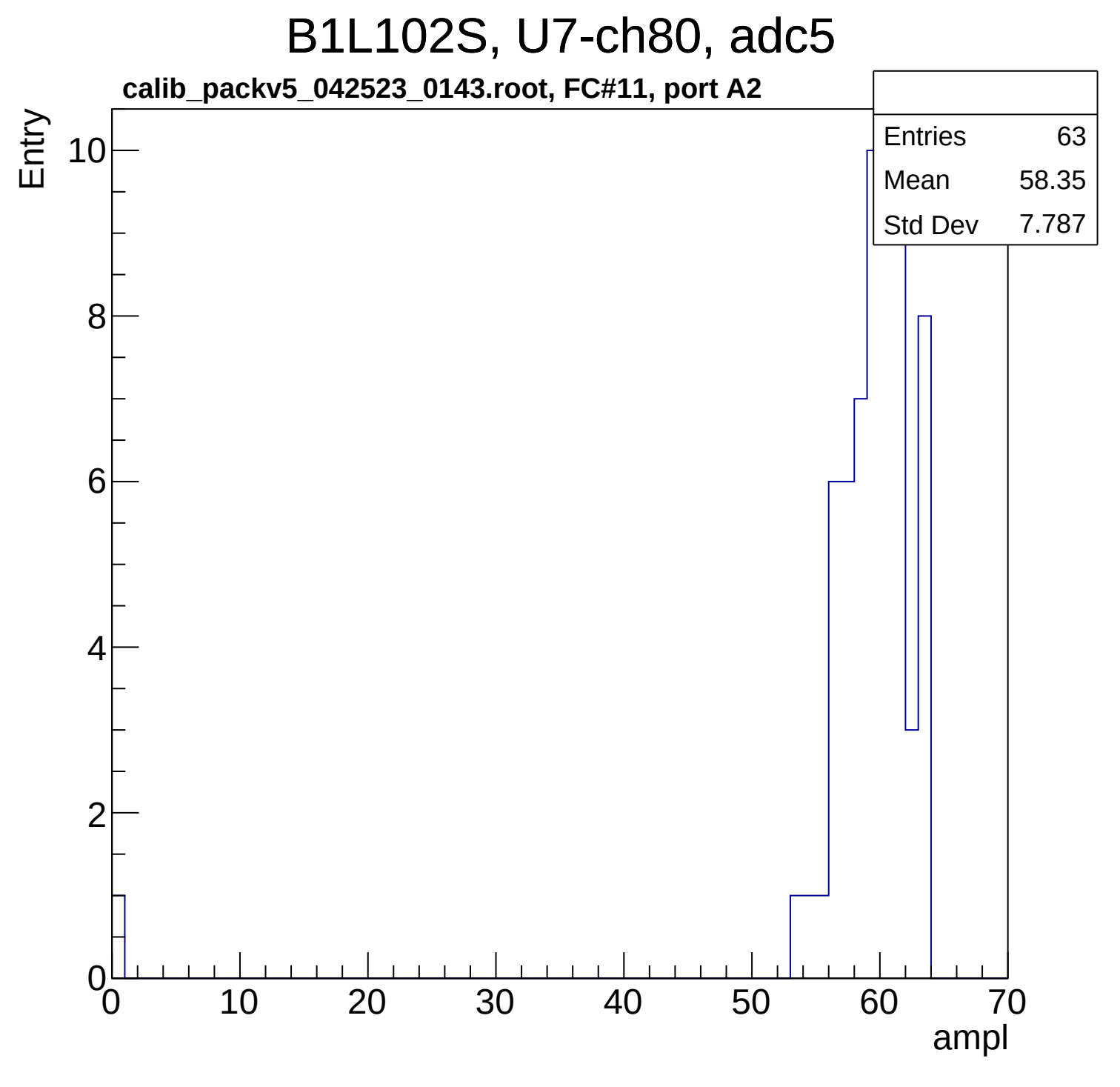
B1L102S, U7-ch80, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 63
Mean 58.35
Std Dev 7.787
Entry
ampl
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2
4
6
8
10
0
10
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40
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60
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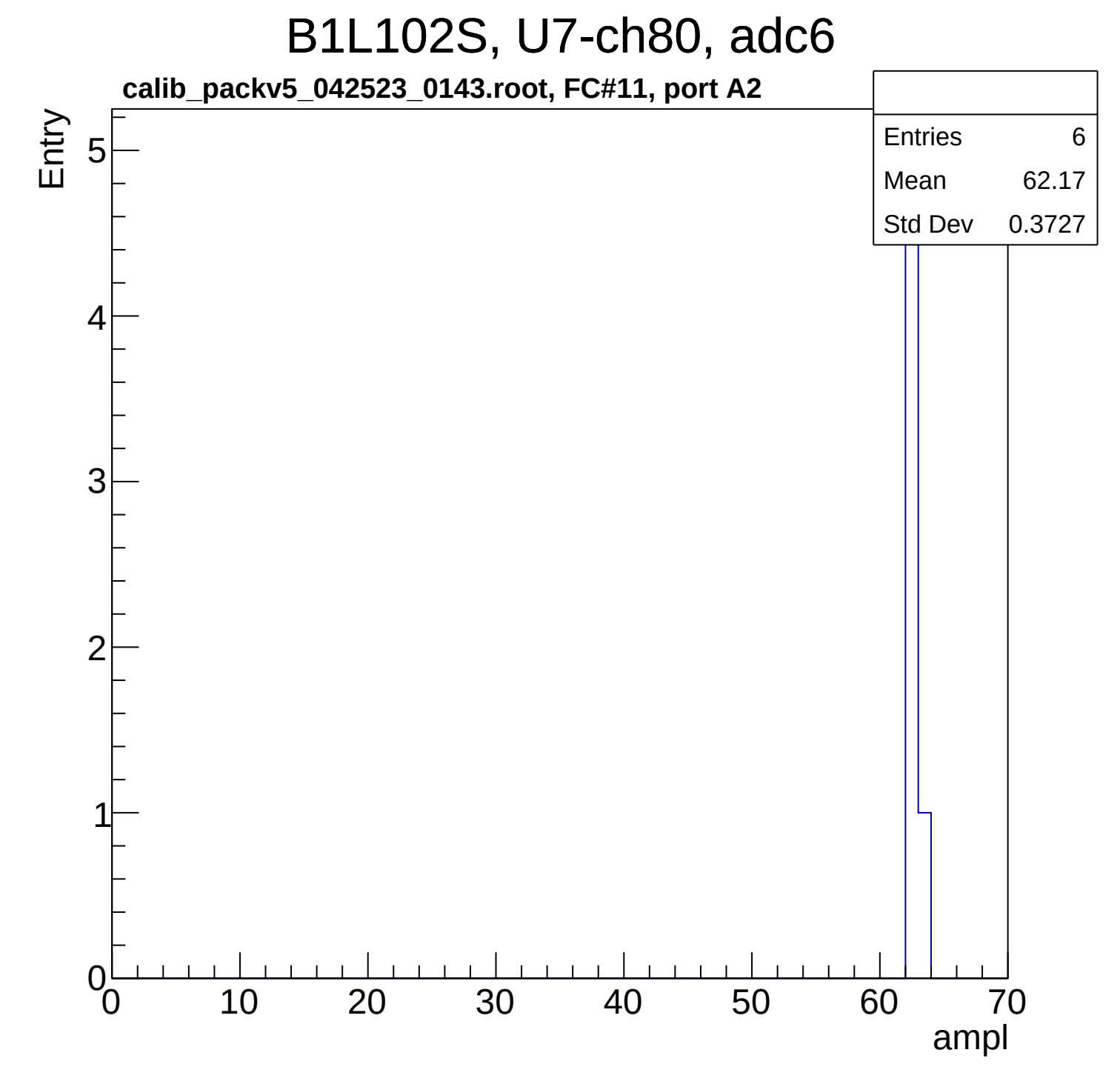
B1L102S, U7-ch80, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 6
Mean 62.17
Std Dev 0.3727
Entry
ampl
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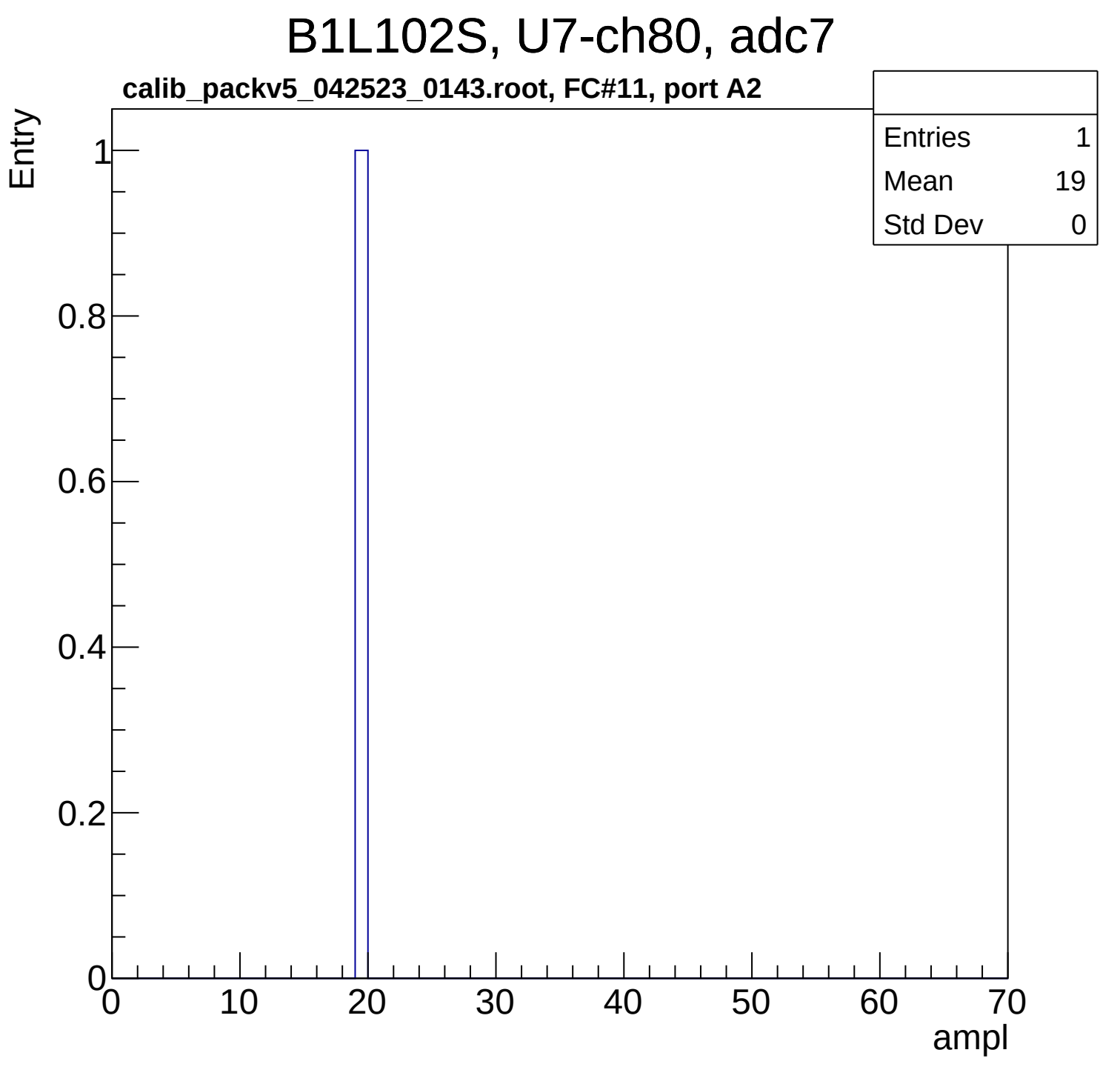
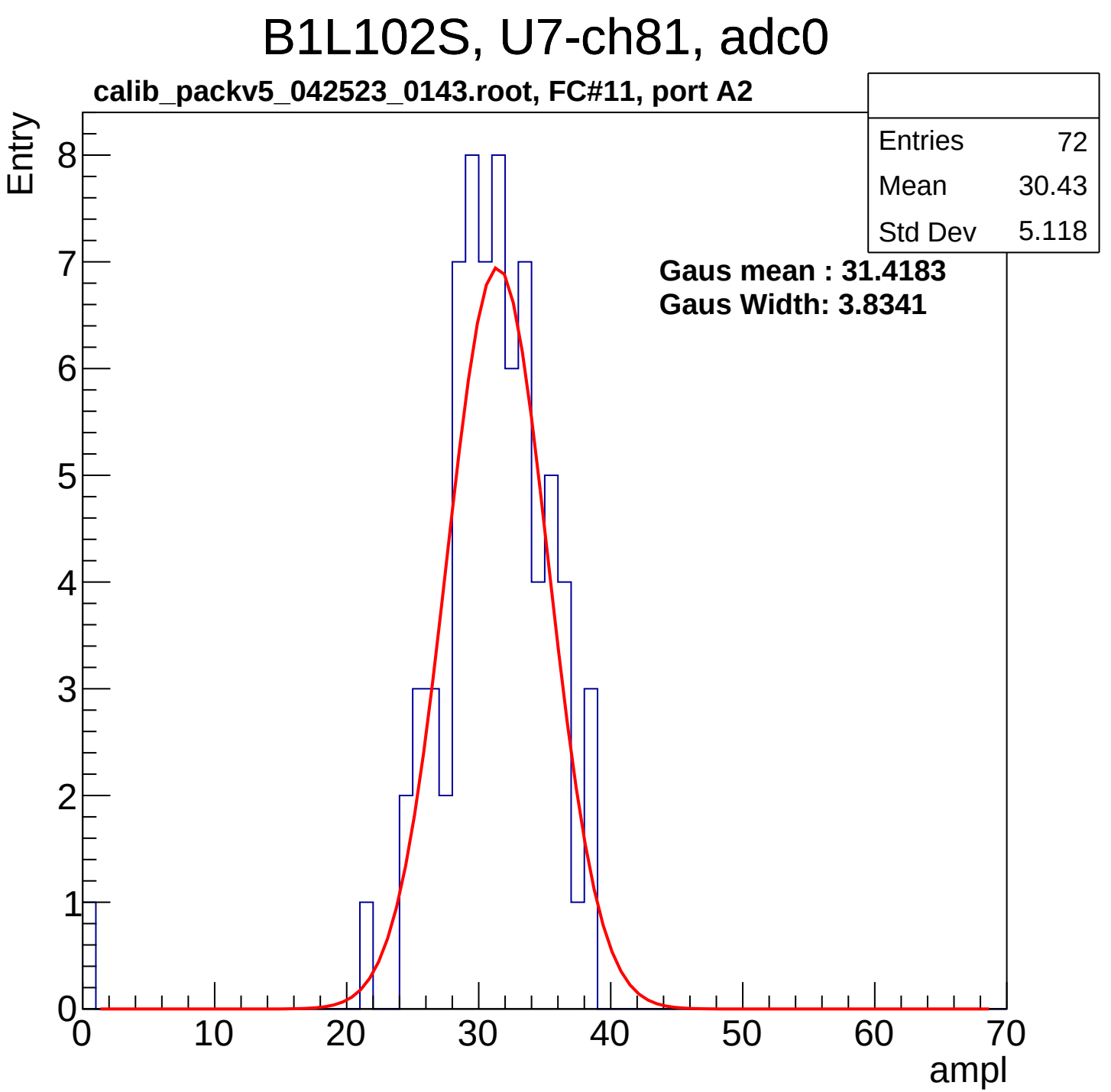
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L102S, U7-ch80, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 1
Mean 19
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U7-ch81, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 72
Mean 30.43
Std Dev 5.118
Gaus mean : 31.4183
Gaus Width: 3.8341
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
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40
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60
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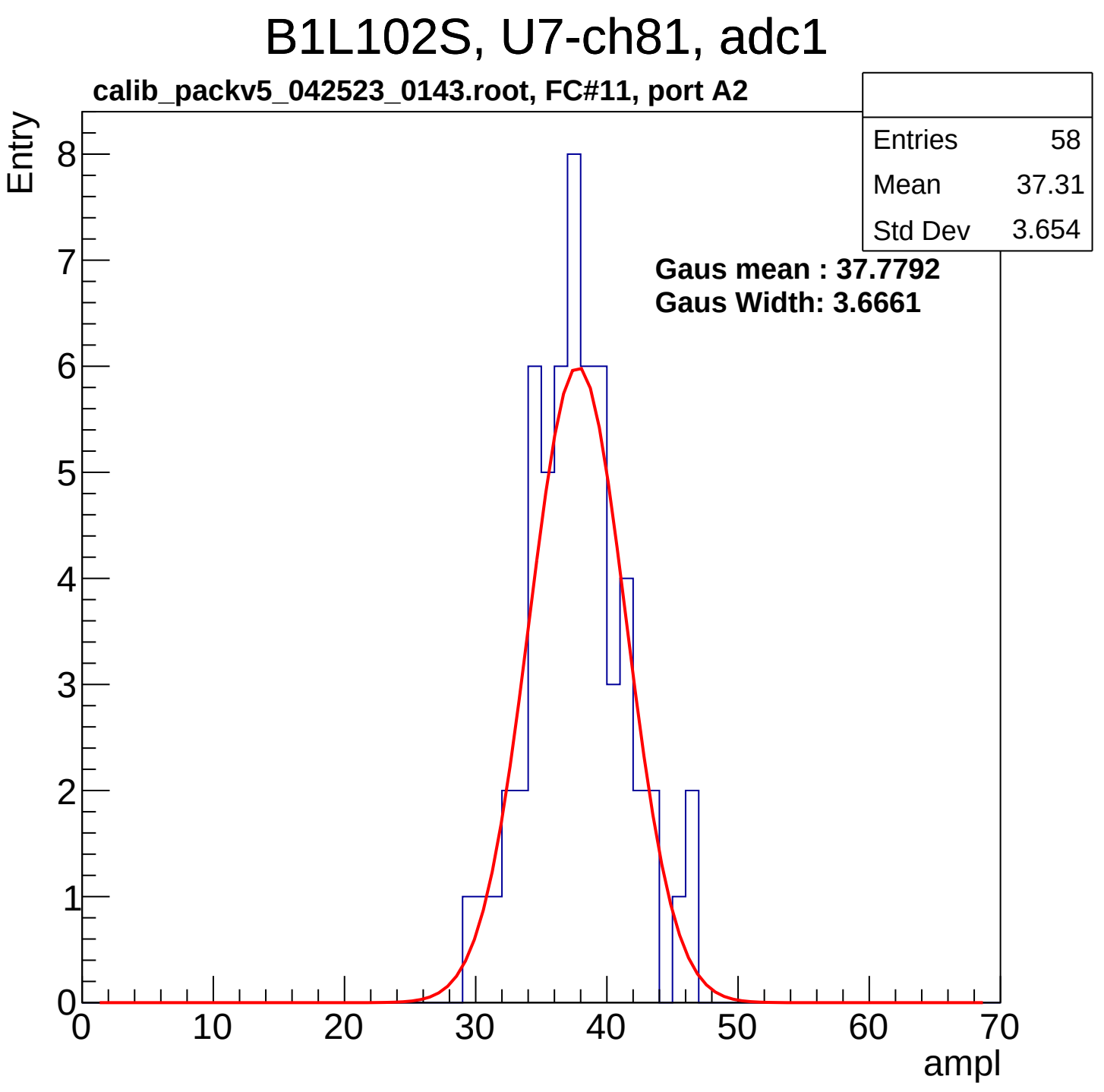
B1L102S, U7-ch81, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 58
Mean 37.31
Std Dev 3.654
Gaus mean : 37.7792
Gaus Width: 3.6661
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
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40
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60
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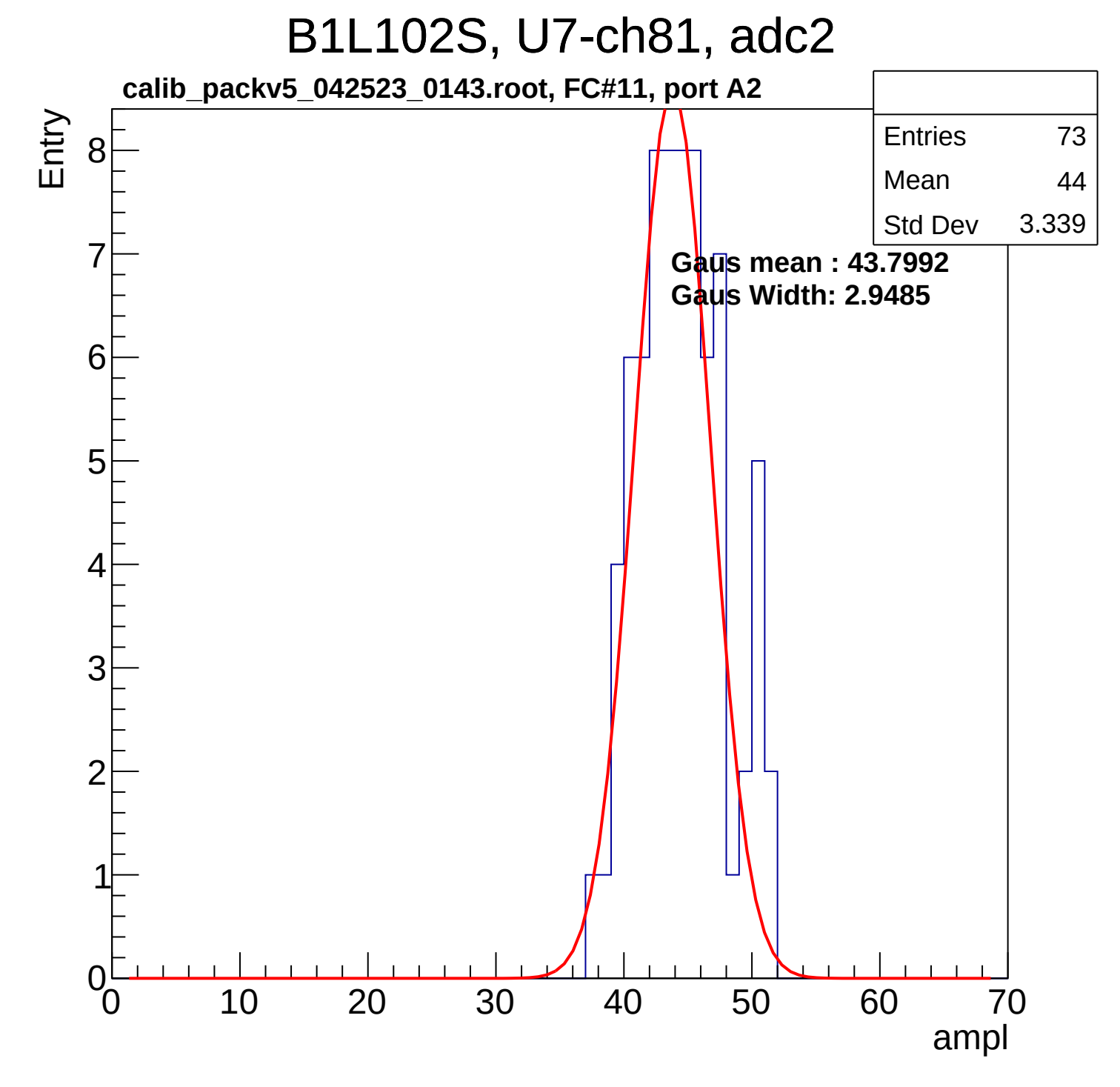
B1L102S, U7-ch81, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 73
Mean 44
Std Dev 3.339
Gaus mean : 43.7992
Gaus Width: 2.9485
Entry
ampl
0
1
2
3
4
5
6
7
8
0
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40
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60
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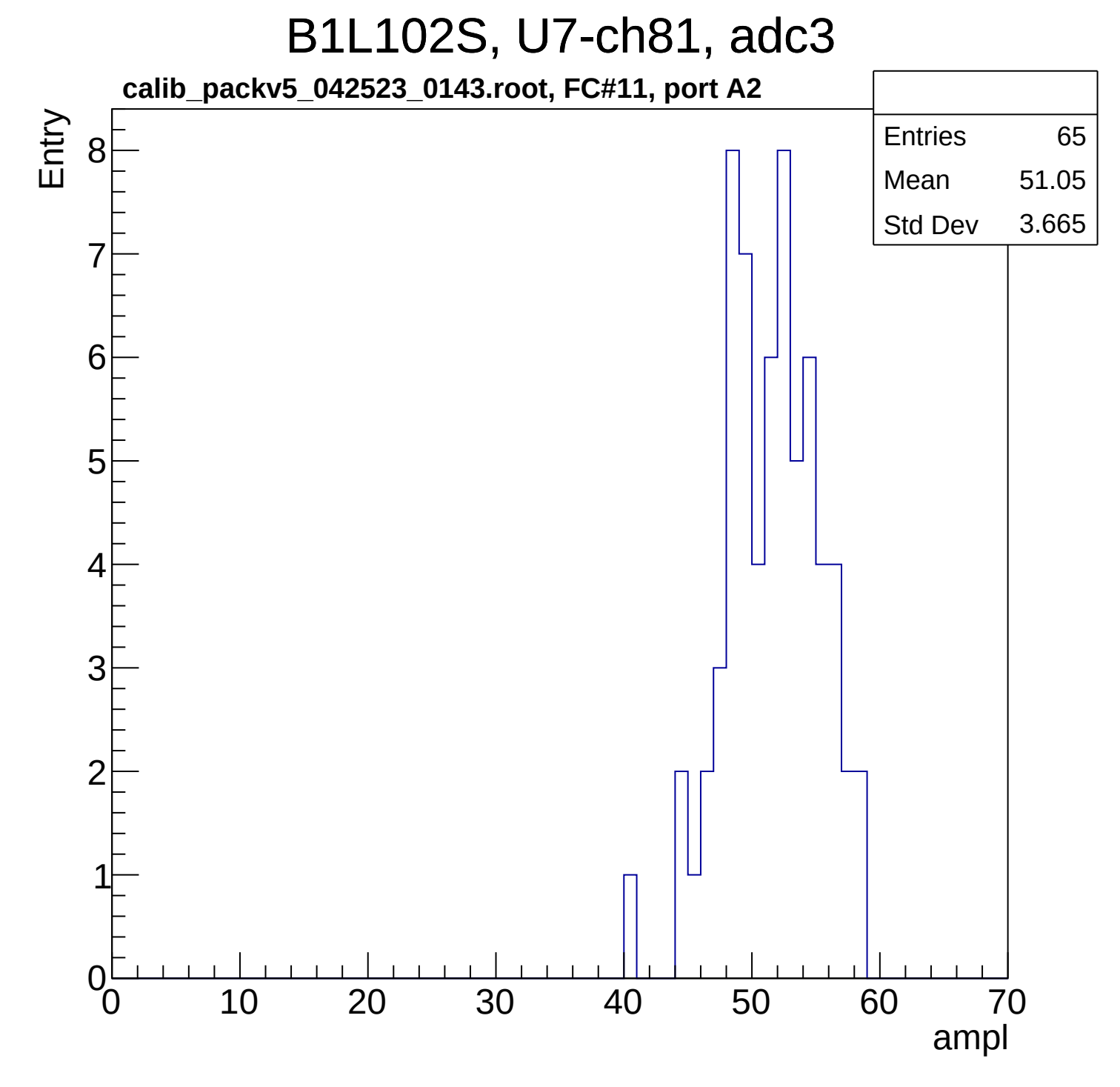
B1L102S, U7-ch81, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 65
Mean 51.05
Std Dev 3.665
Entry
ampl
0
1
2
3
4
5
6
7
8
0
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20
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60
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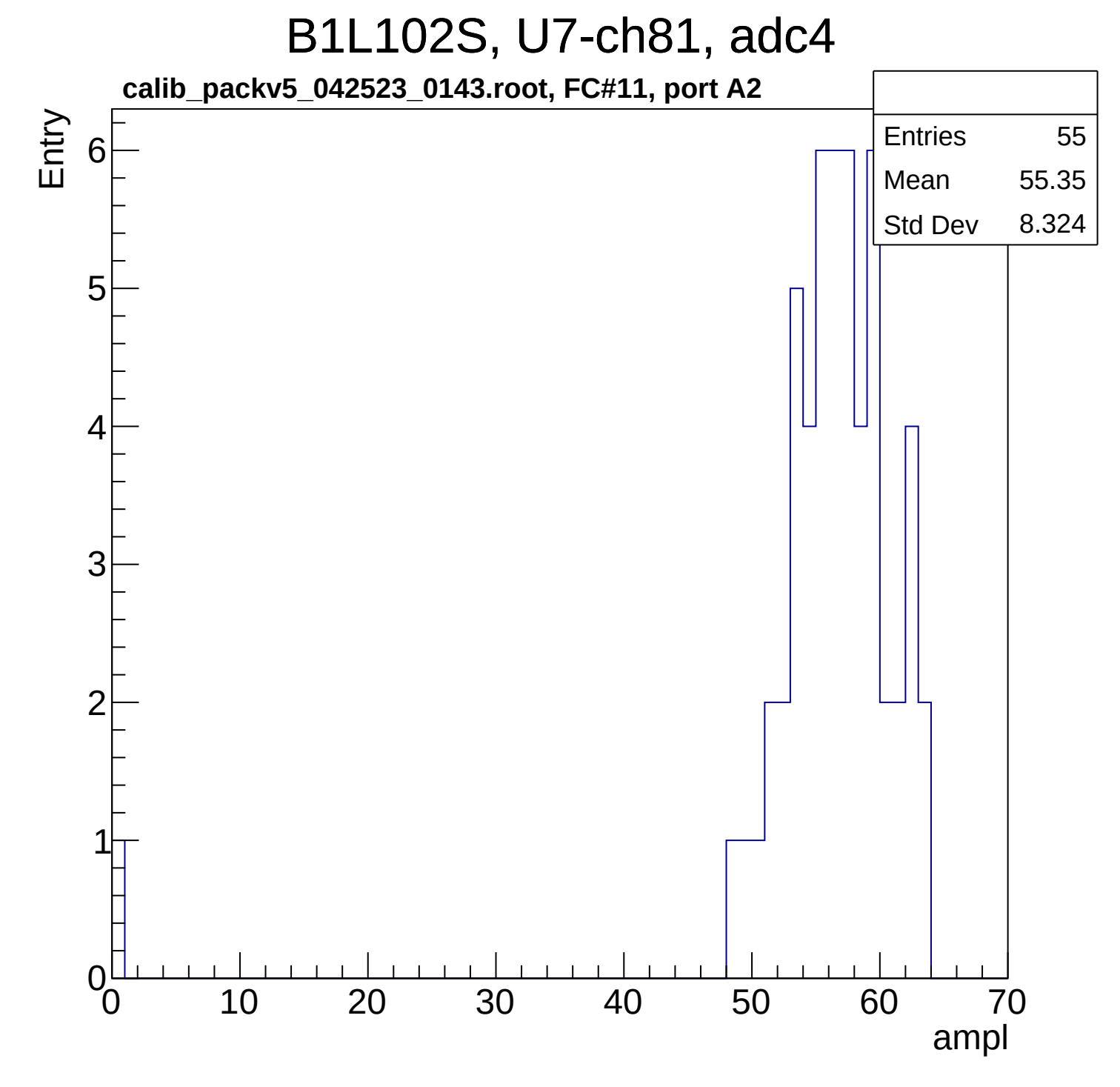
B1L102S, U7-ch81, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 55
Mean 55.35
Std Dev 8.324
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
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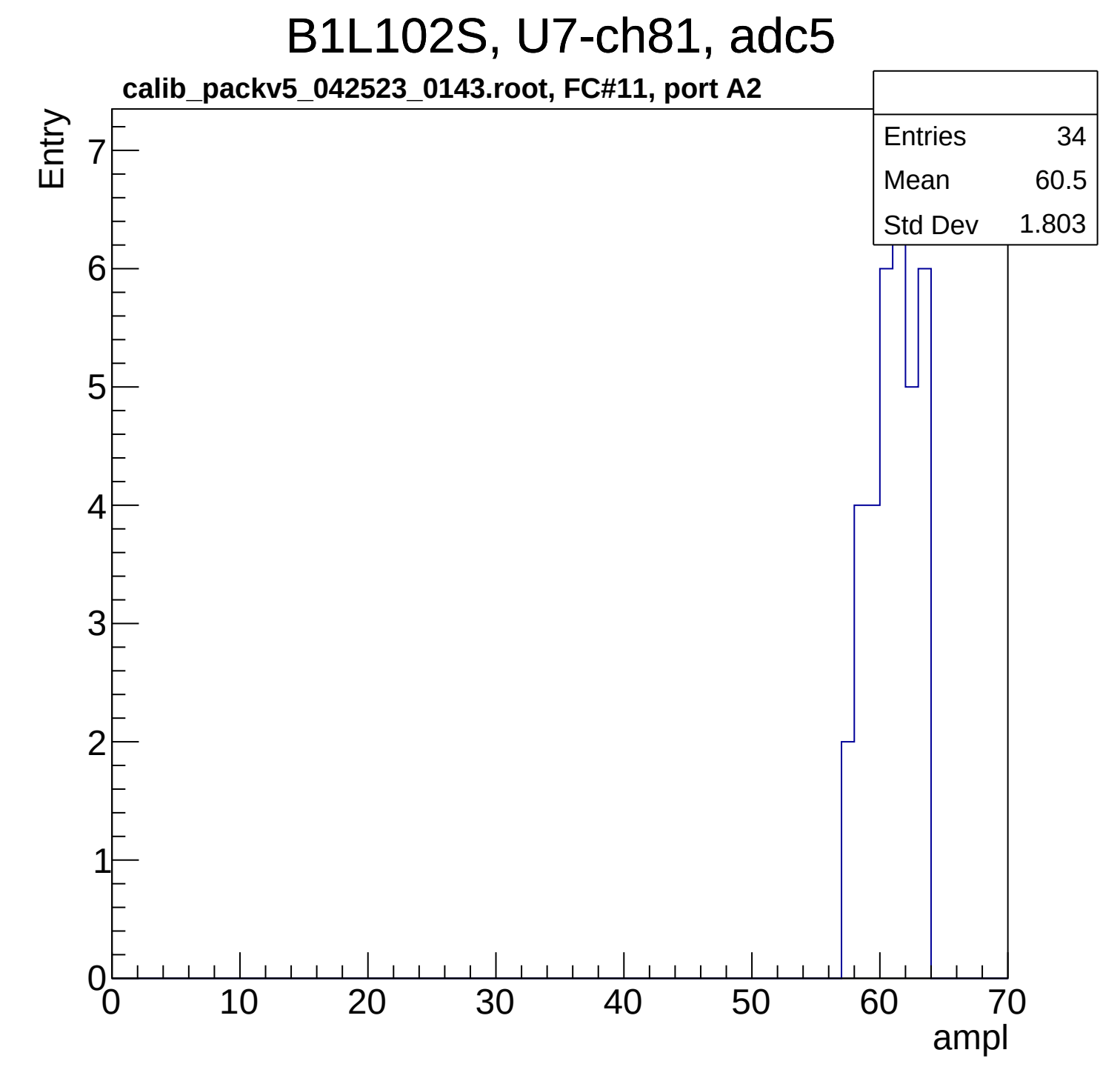
B1L102S, U7-ch81, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 34
Mean 60.5
Std Dev 1.803
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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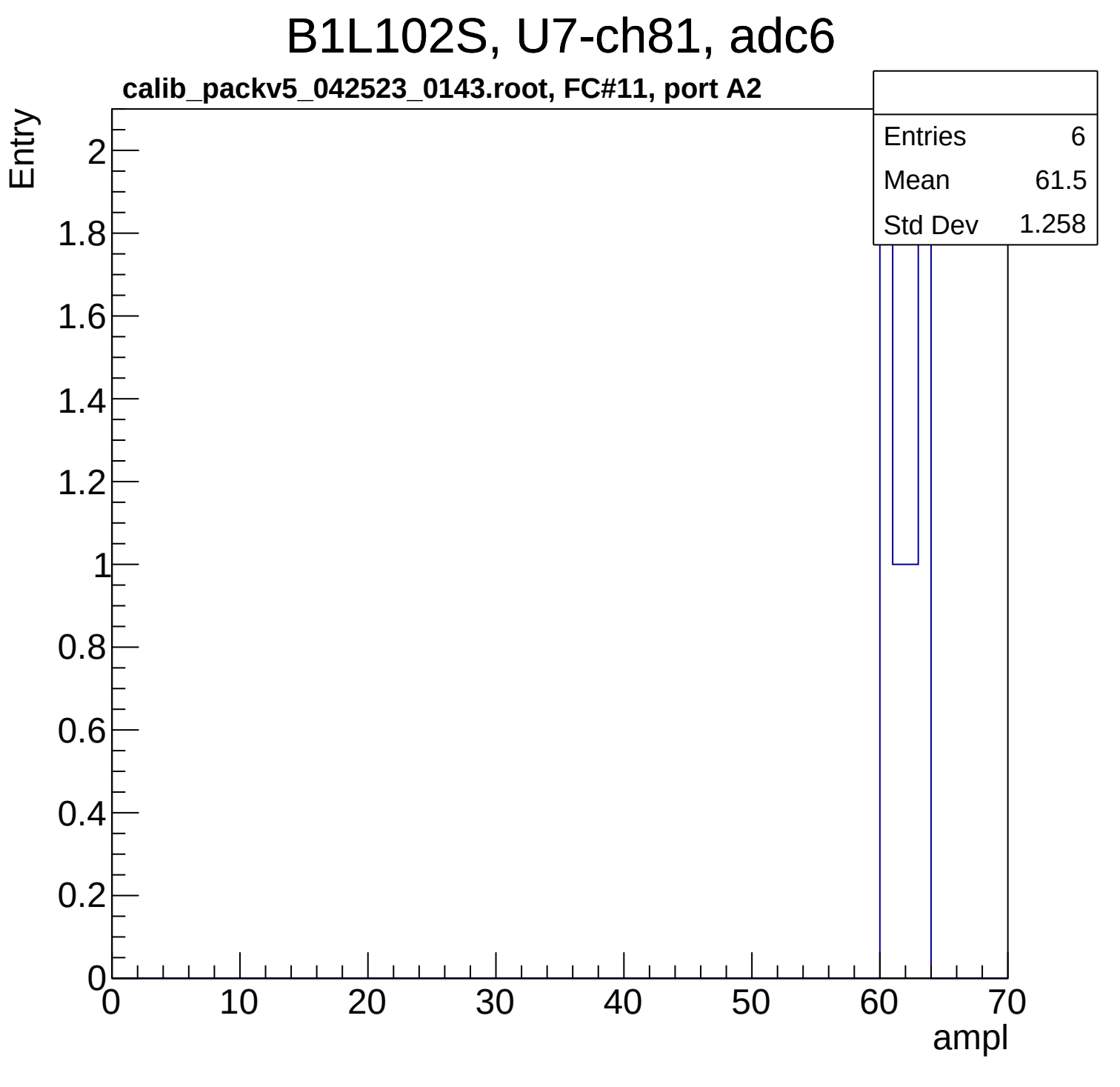
B1L102S, U7-ch81, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 6
Mean 61.5
Std Dev 1.258
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
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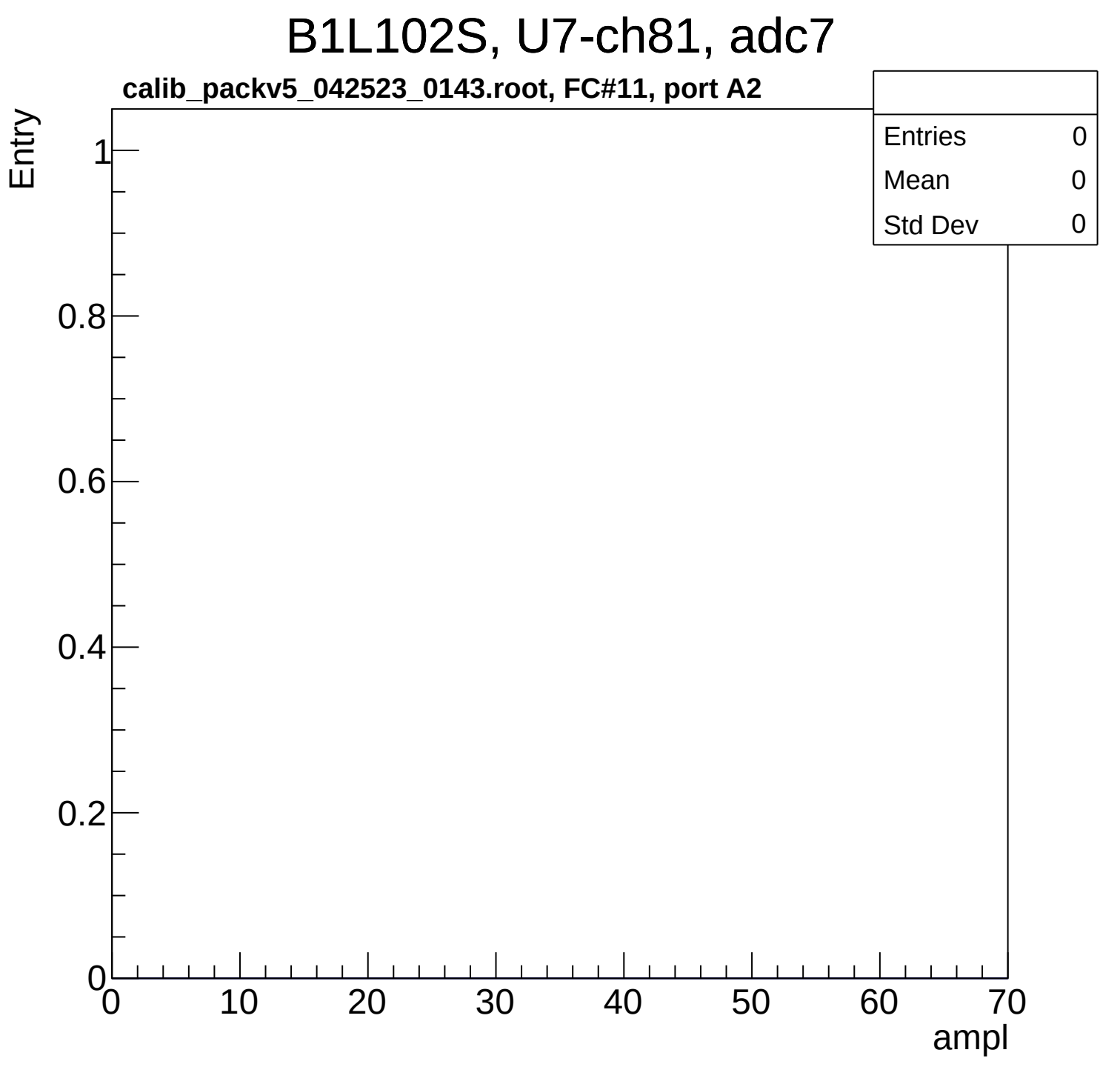
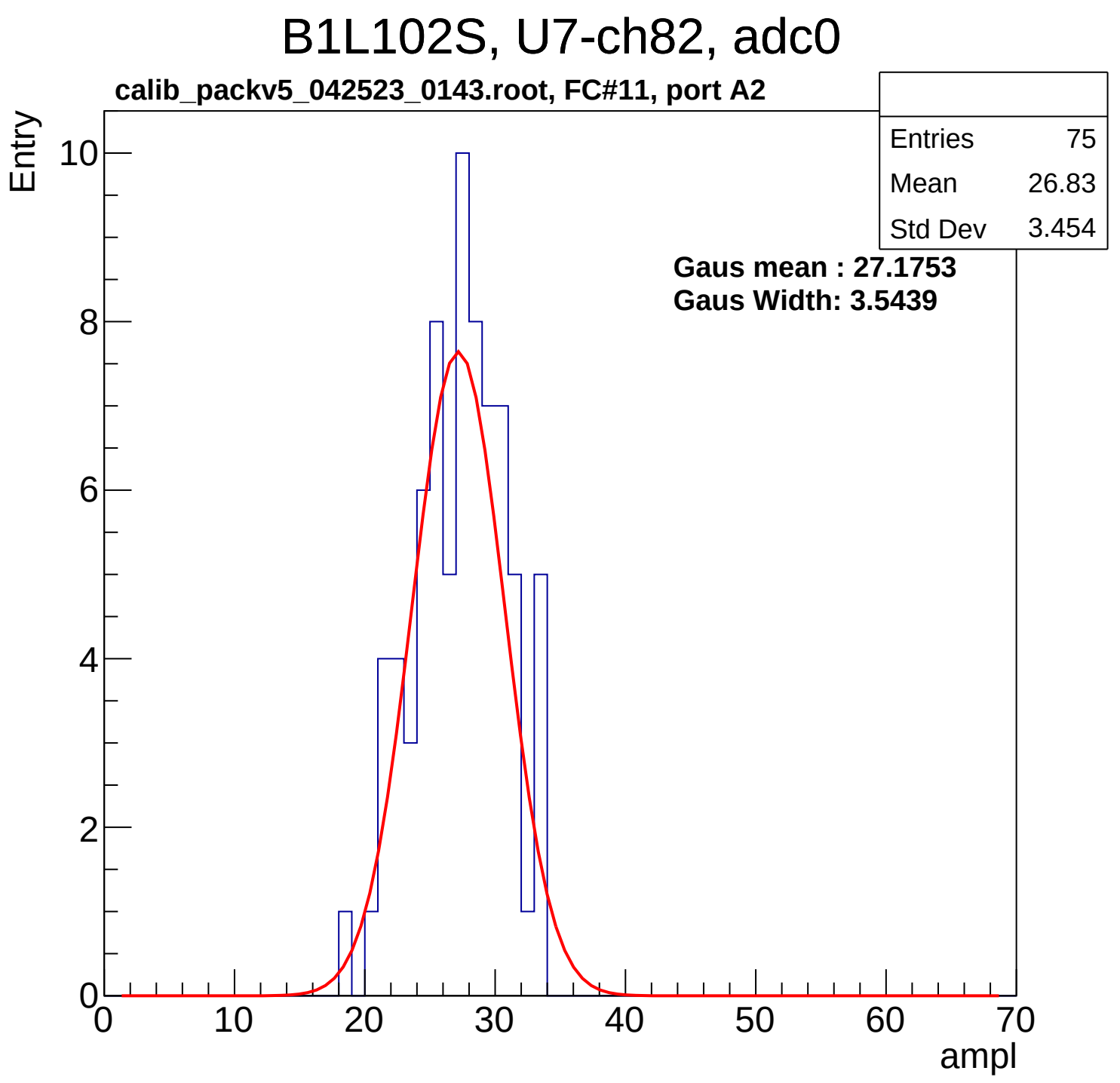
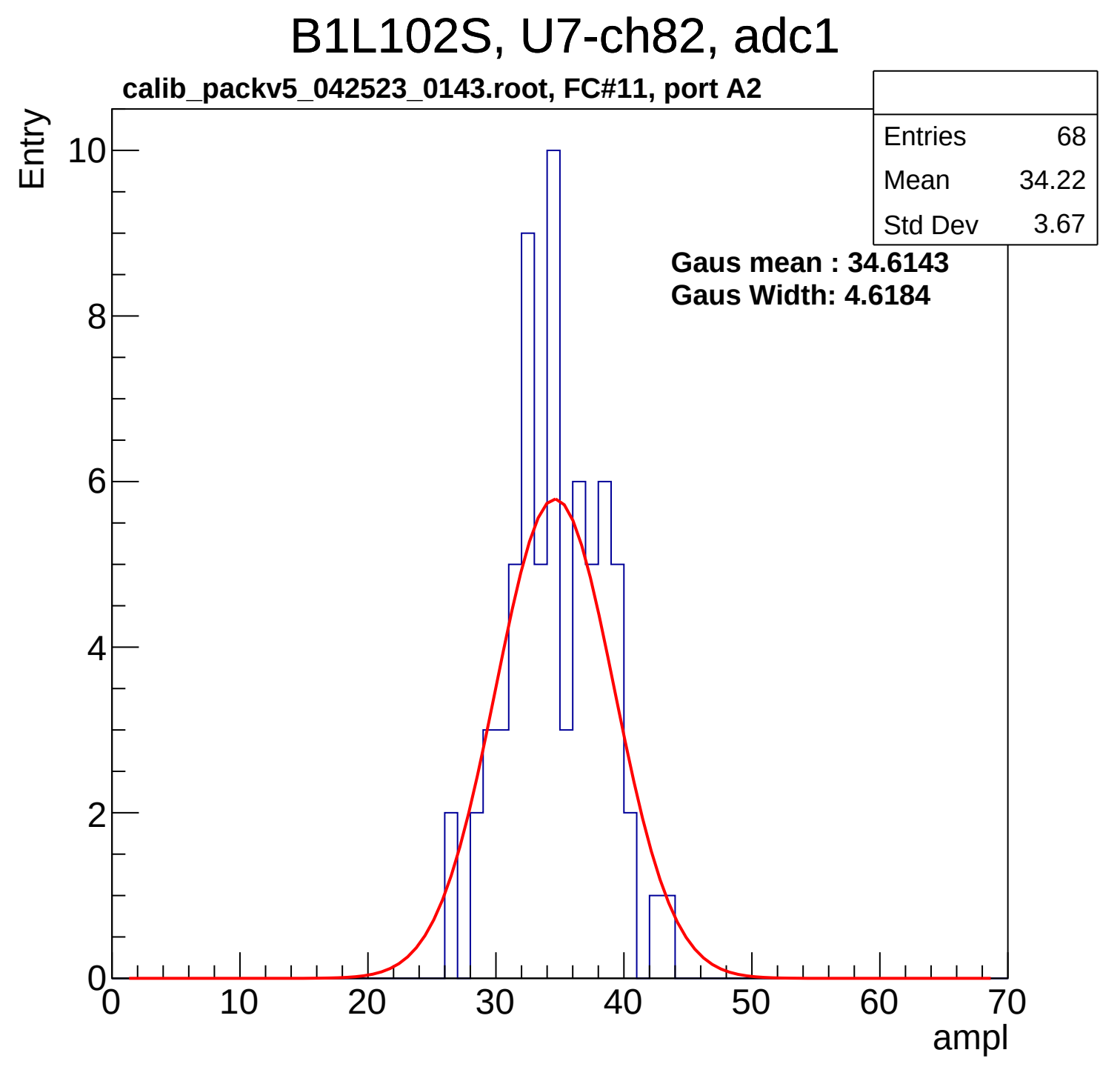
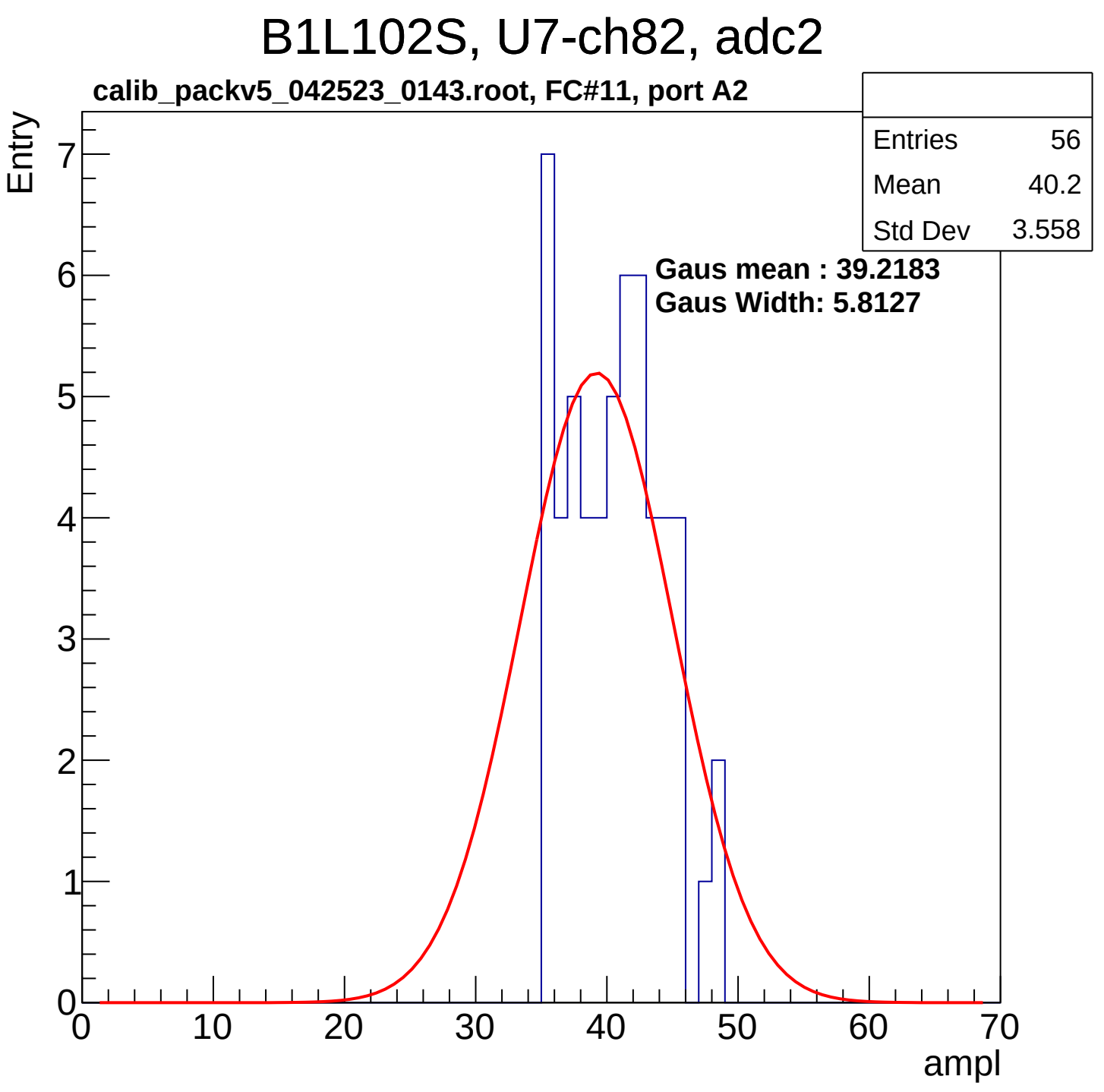
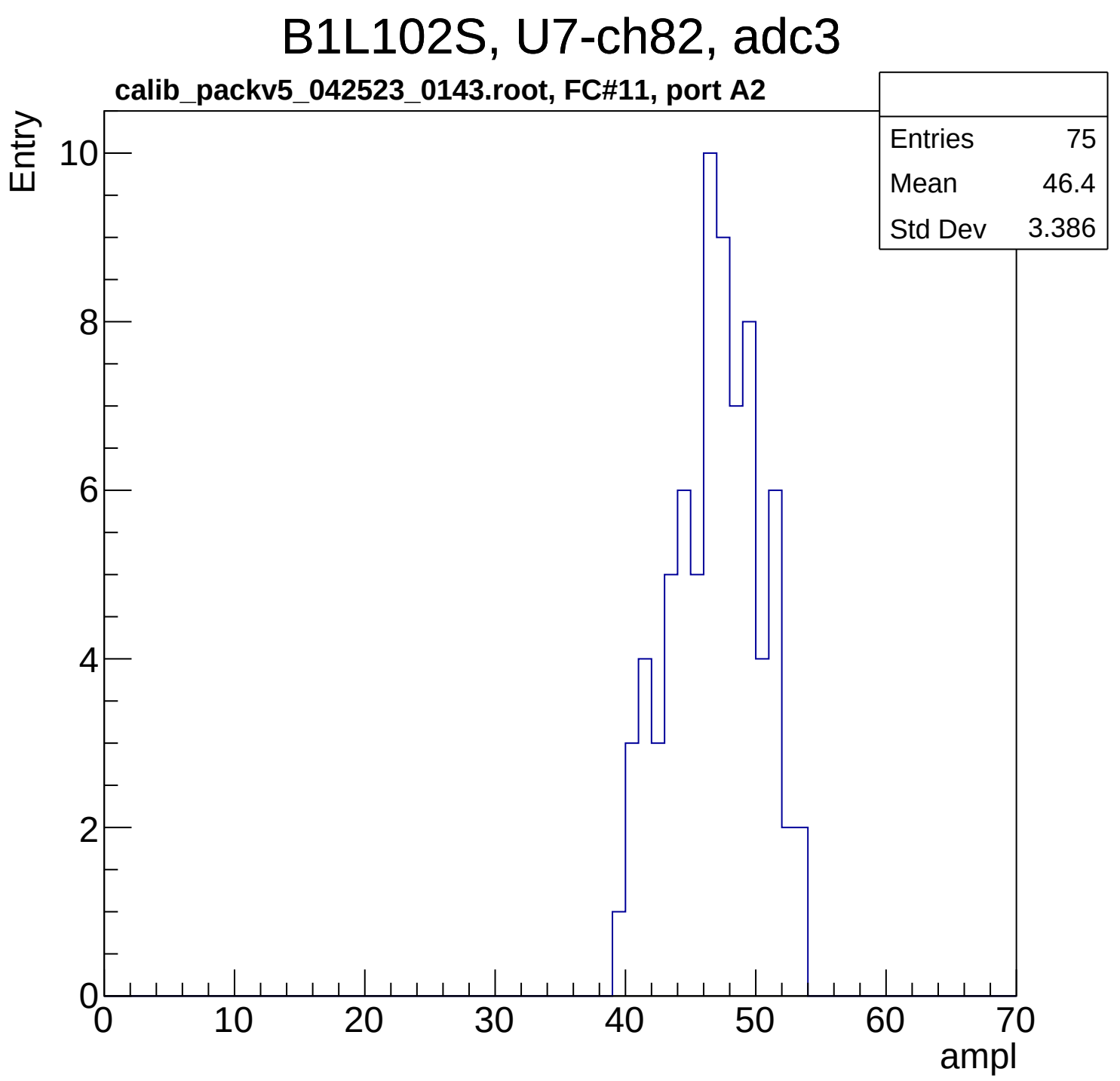
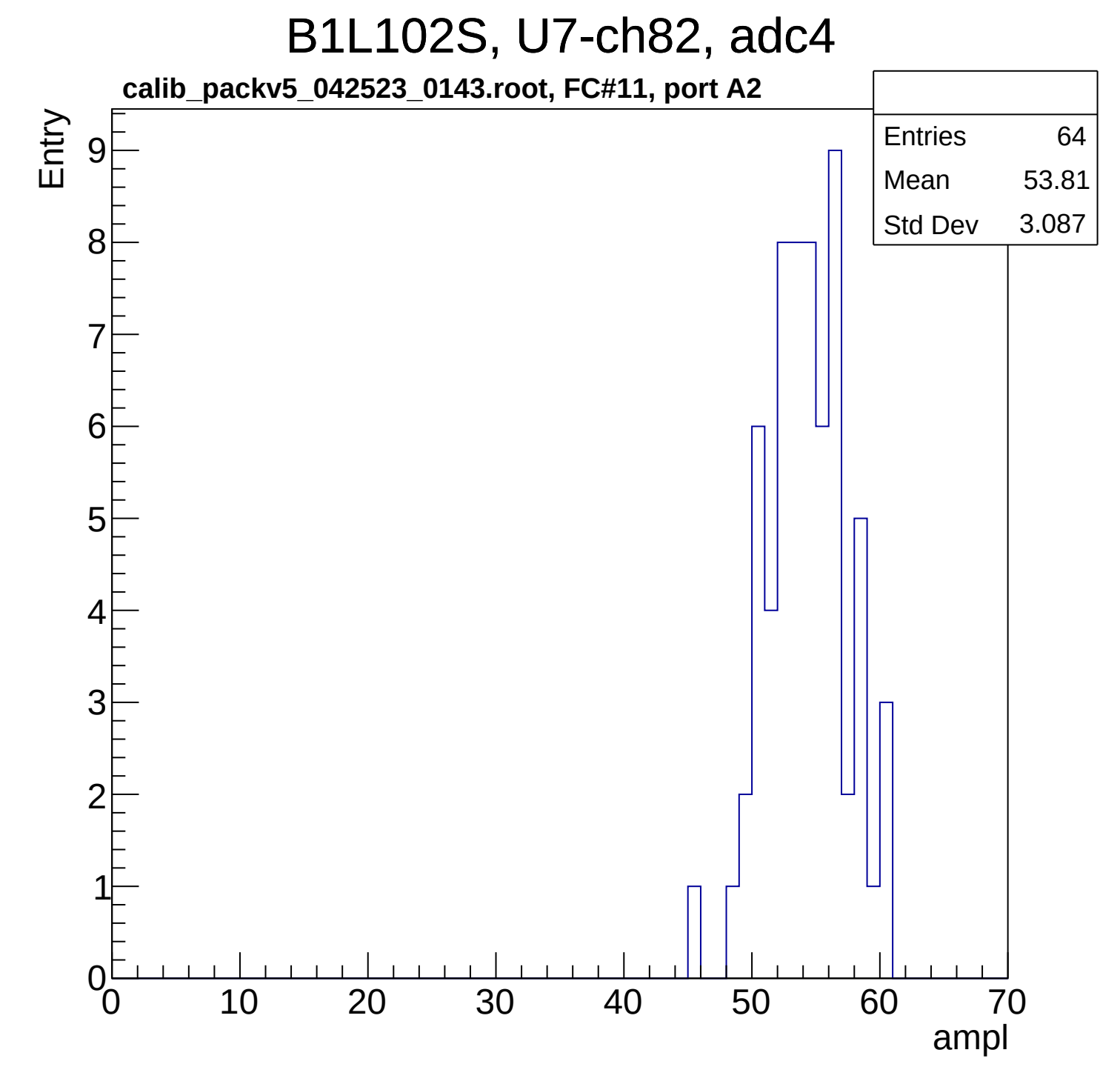

B1L102S, U7-ch81, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U7-ch82, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 75
Mean 26.83
Std Dev 3.454
Gaus mean : 27.1753
Gaus Width: 3.5439
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L102S, U7-ch82, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 68
Mean 34.22
Std Dev 3.67
Gaus mean : 34.6143
Gaus Width: 4.6184
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L102S, U7-ch82, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 56
Mean 40.2
Std Dev 3.558
Gaus mean : 39.2183
Gaus Width: 5.8127
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L102S, U7-ch82, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 75
Mean 46.4
Std Dev 3.386
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L102S, U7-ch82, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 64
Mean 53.81
Std Dev 3.087
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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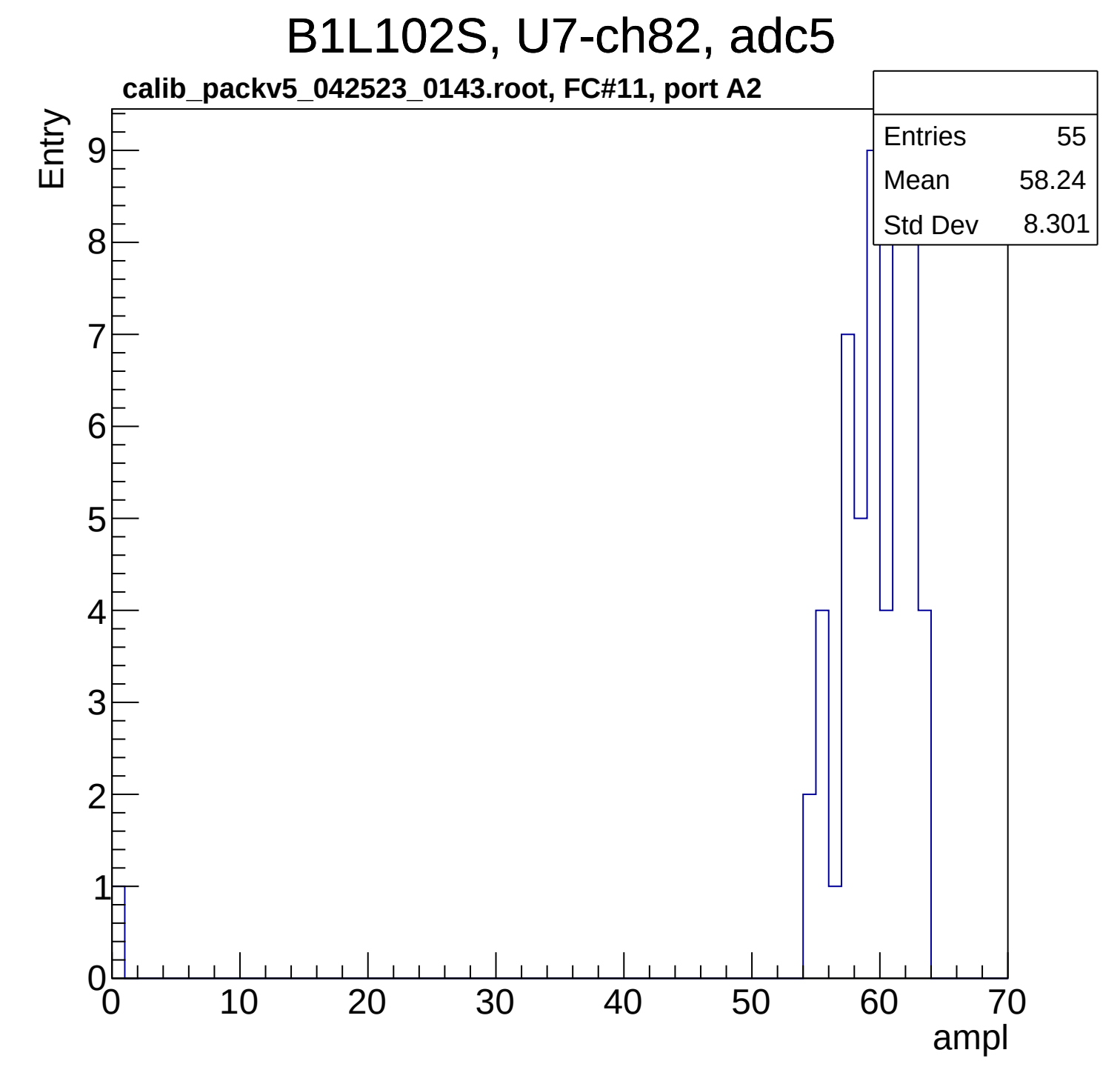
B1L102S, U7-ch82, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 55
Mean 58.24
Std Dev 8.301
Entry
ampl
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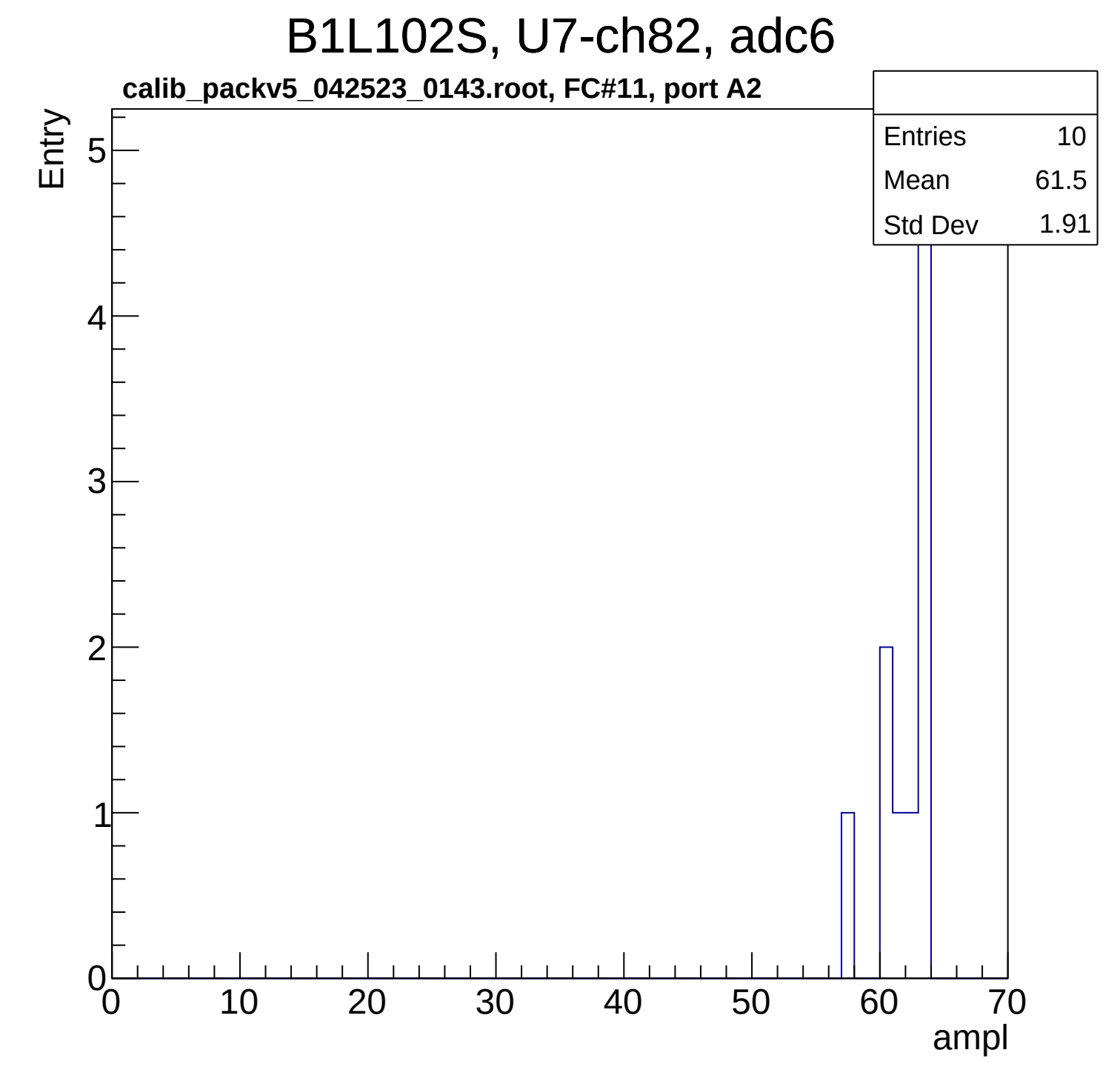
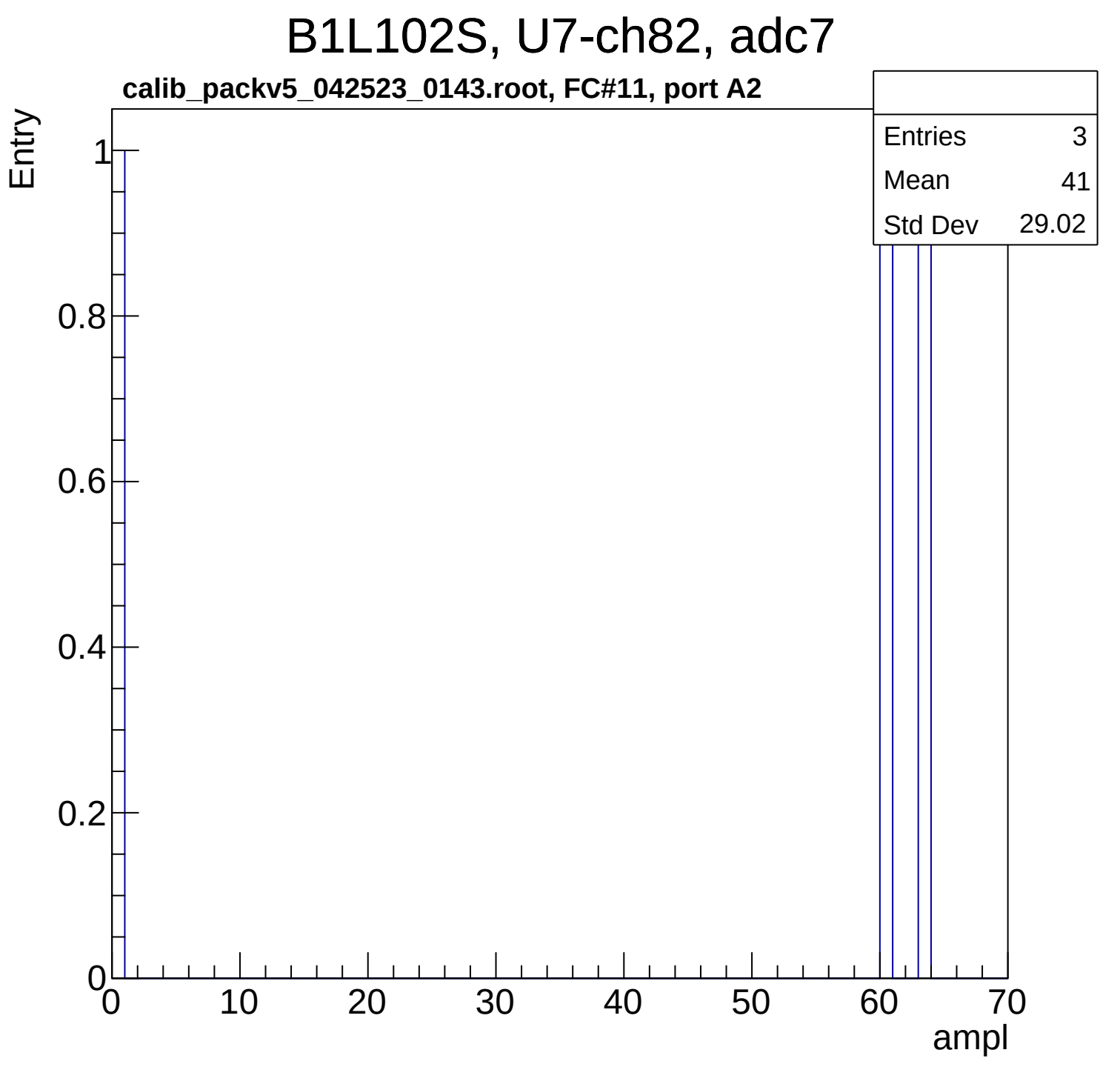
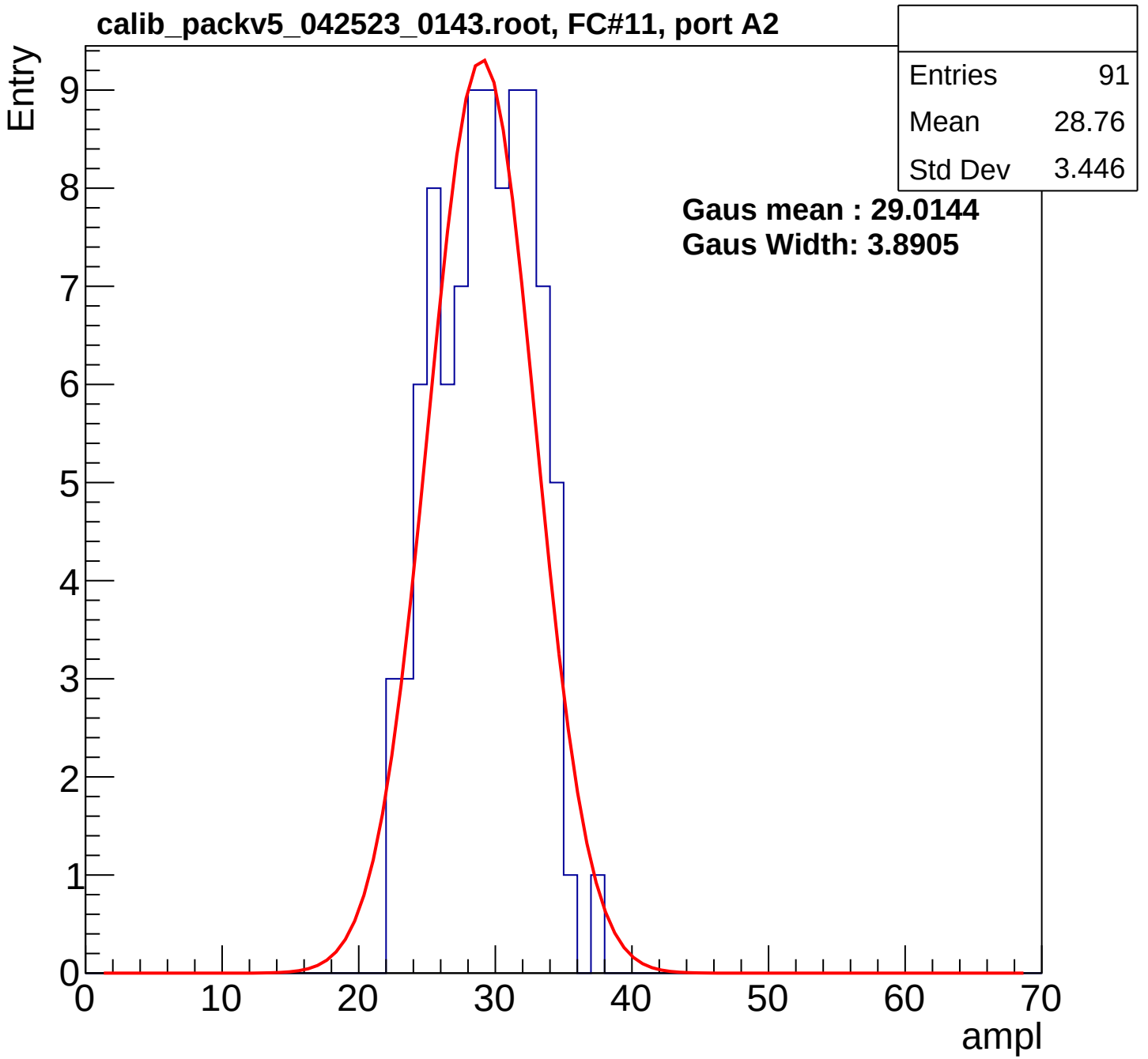
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9


B1L102S, U7-ch82, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 10
Mean 61.5
Std Dev 1.91
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L102S, U7-ch82, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 3
Mean 41
Std Dev 29.02
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U7-ch83, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 91
Mean 28.76
Std Dev 3.446
Gaus mean : 29.0144
Gaus Width: 3.8905
Entry
ampl
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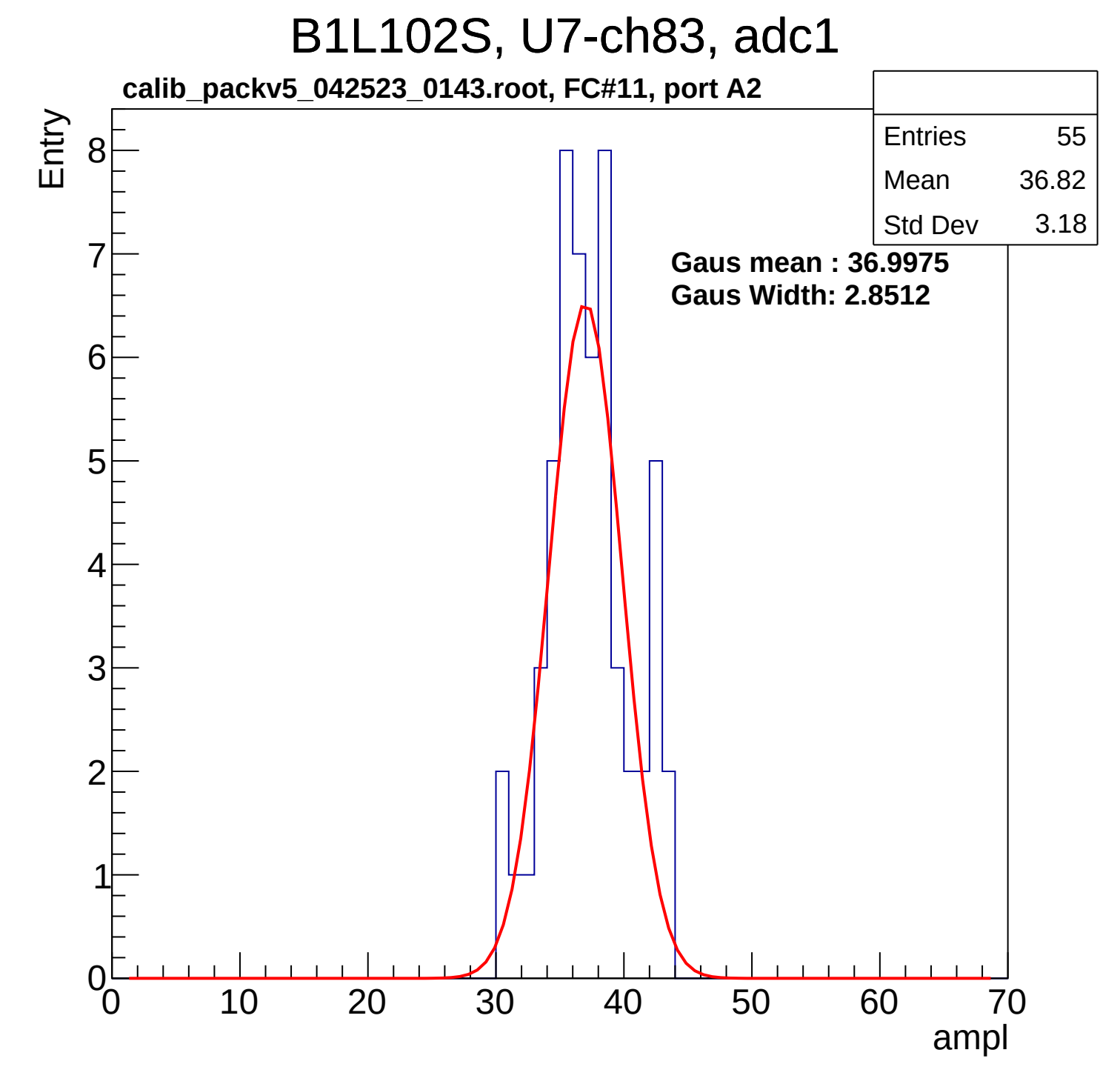
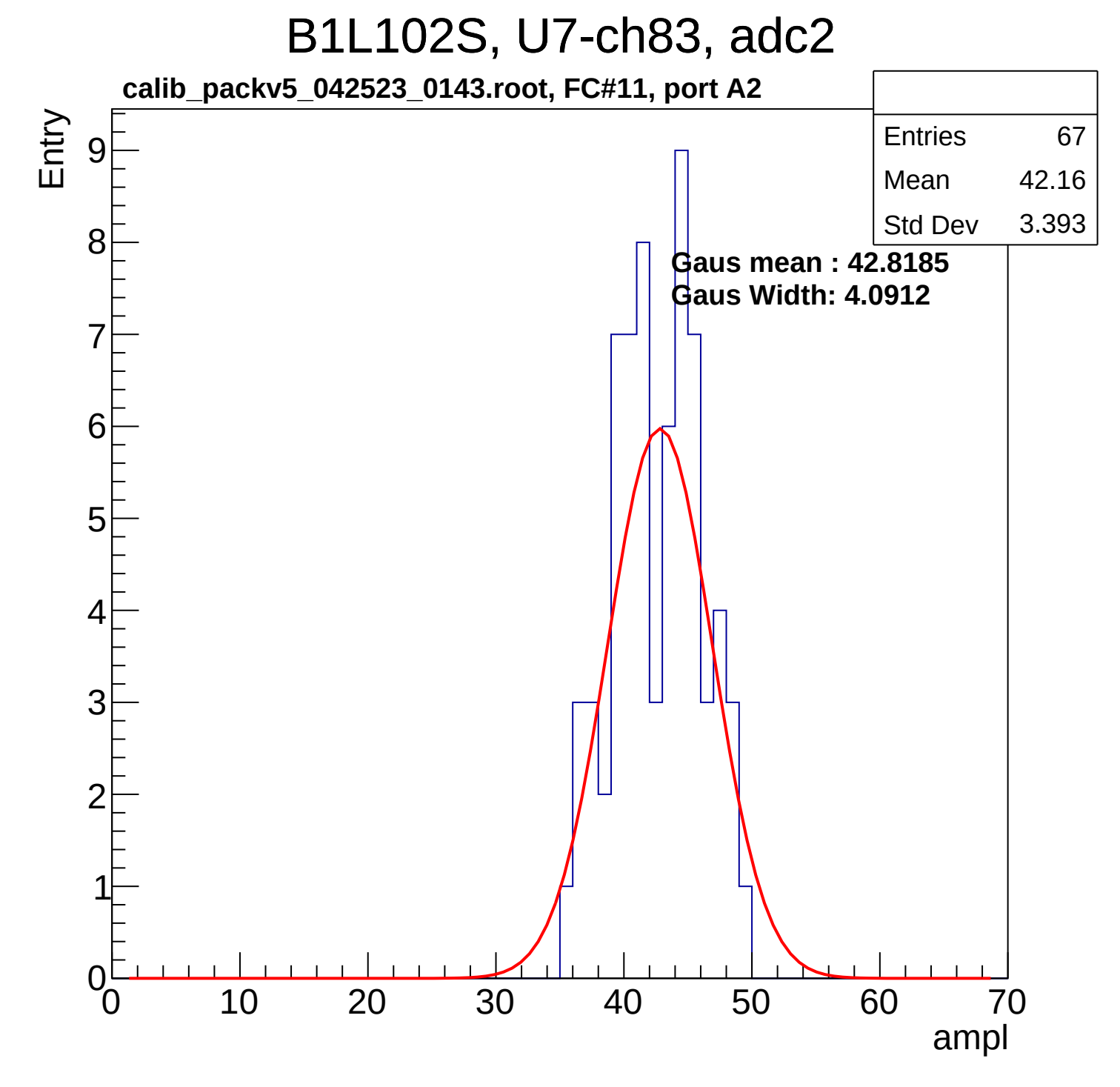
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L102S, U7-ch83, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 55
Mean 36.82
Std Dev 3.18
Gaus mean : 36.9975
Gaus Width: 2.8512
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L102S, U7-ch83, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 67
Mean 42.16
Std Dev 3.393
Gaus mean : 42.8185
Gaus Width: 4.0912
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
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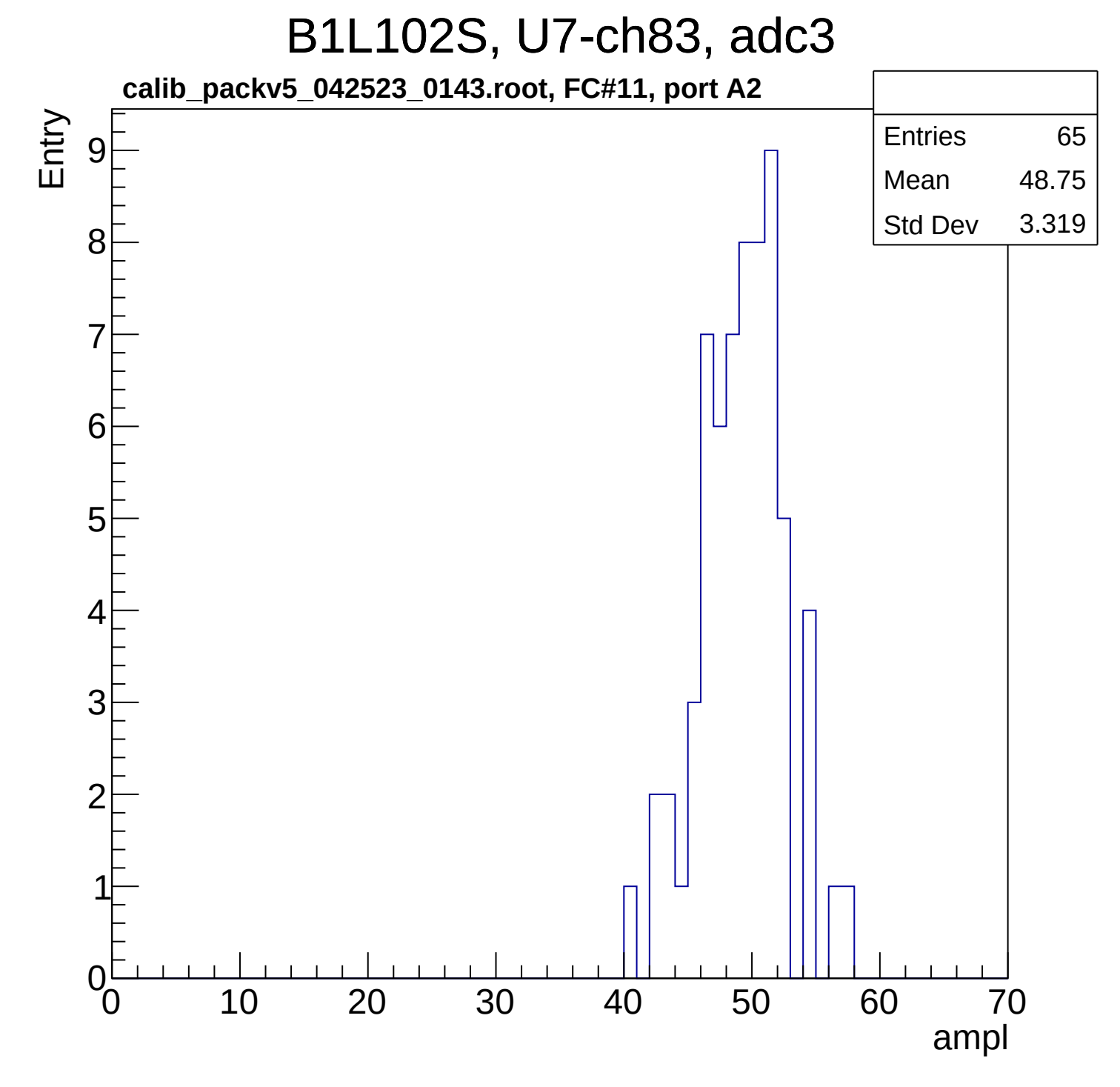
60
70


B1L102S, U7-ch83, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 65
Mean 48.75
Std Dev 3.319
Entry
ampl
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3
4
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6
7
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0
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60
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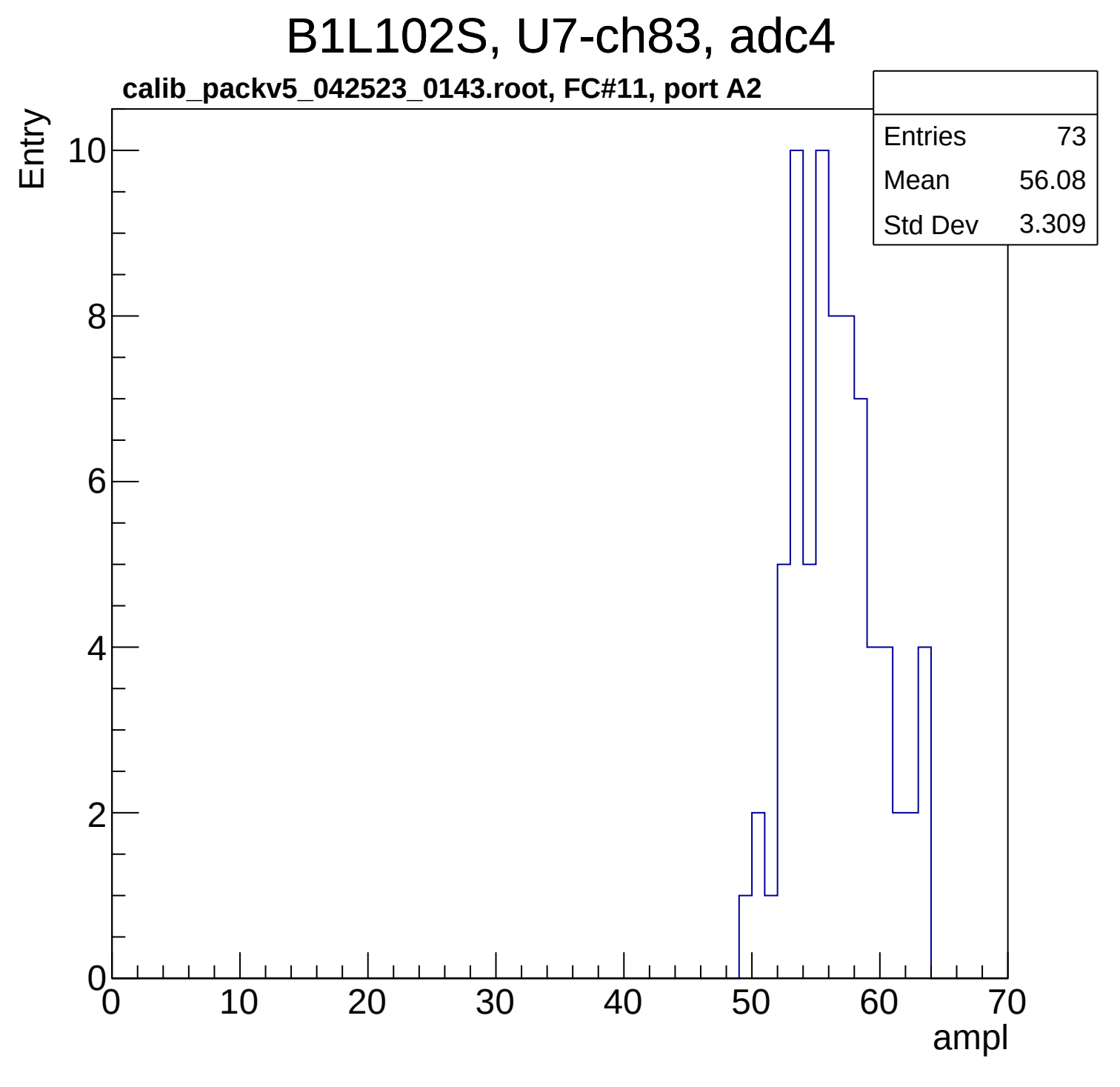
B1L102S, U7-ch83, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 73
Mean 56.08
Std Dev 3.309
Entry
ampl
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0
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20
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40
50
60
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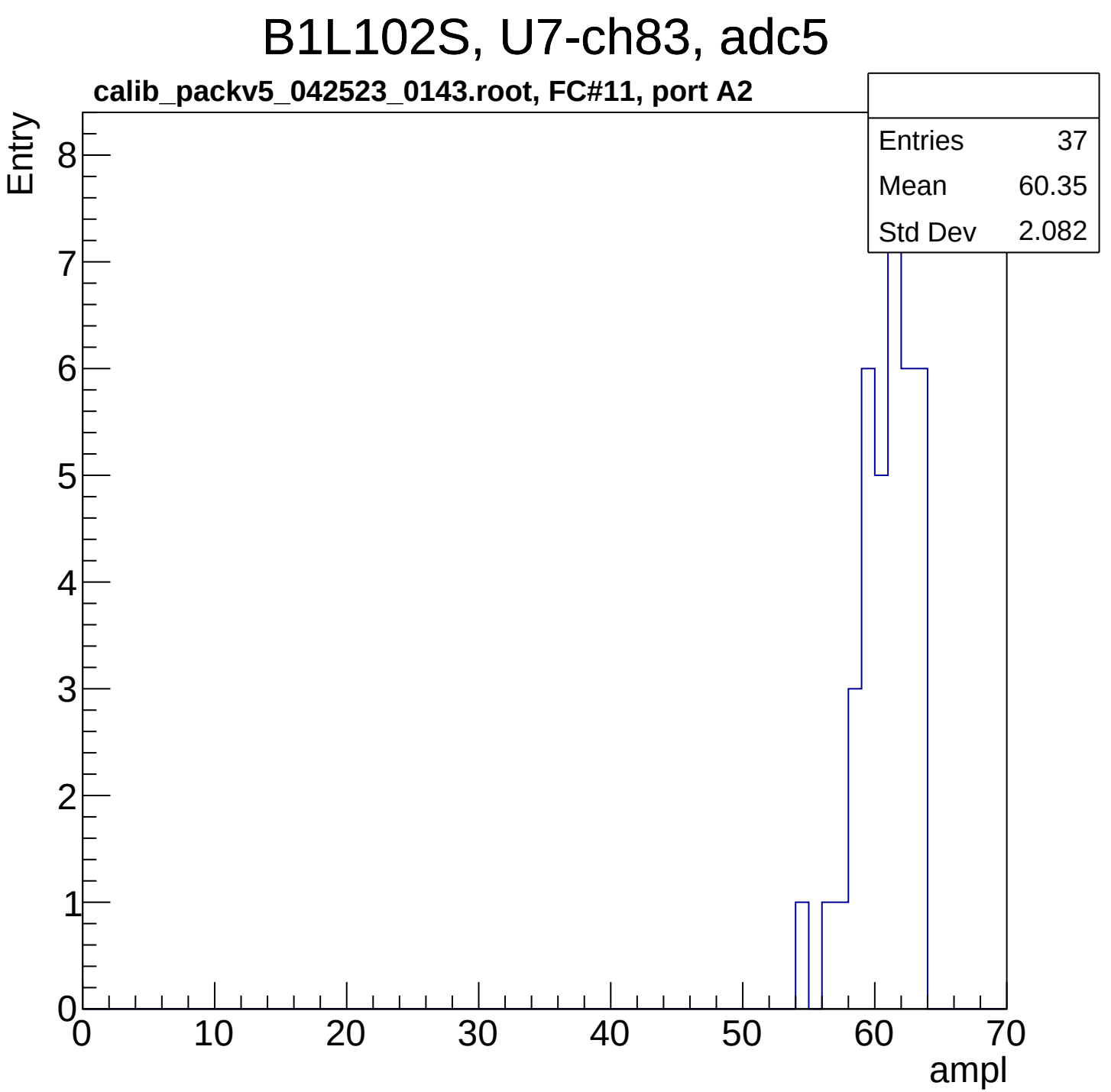
B1L102S, U7-ch83, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 37
Mean 60.35
Std Dev 2.082
Entry
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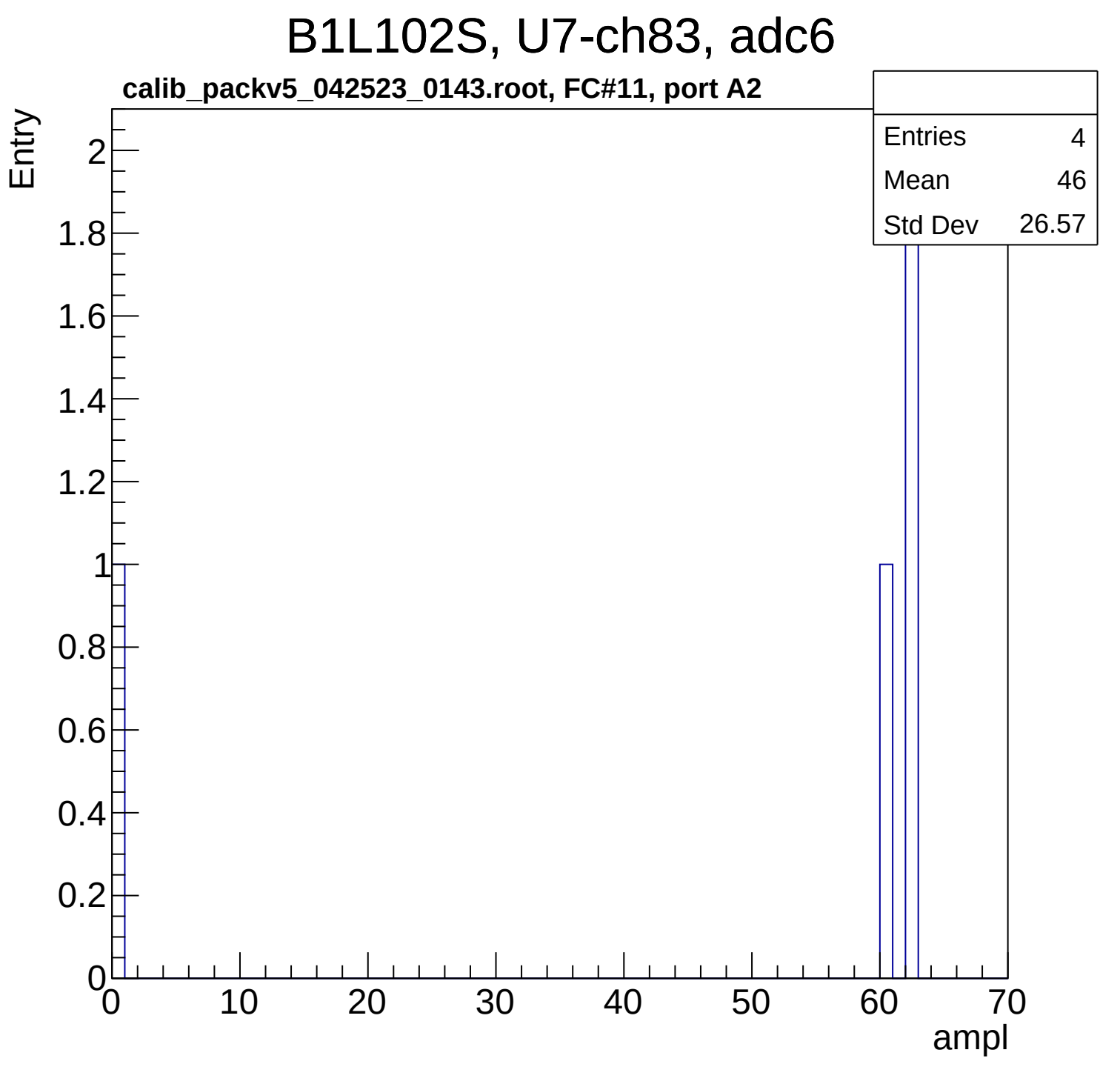
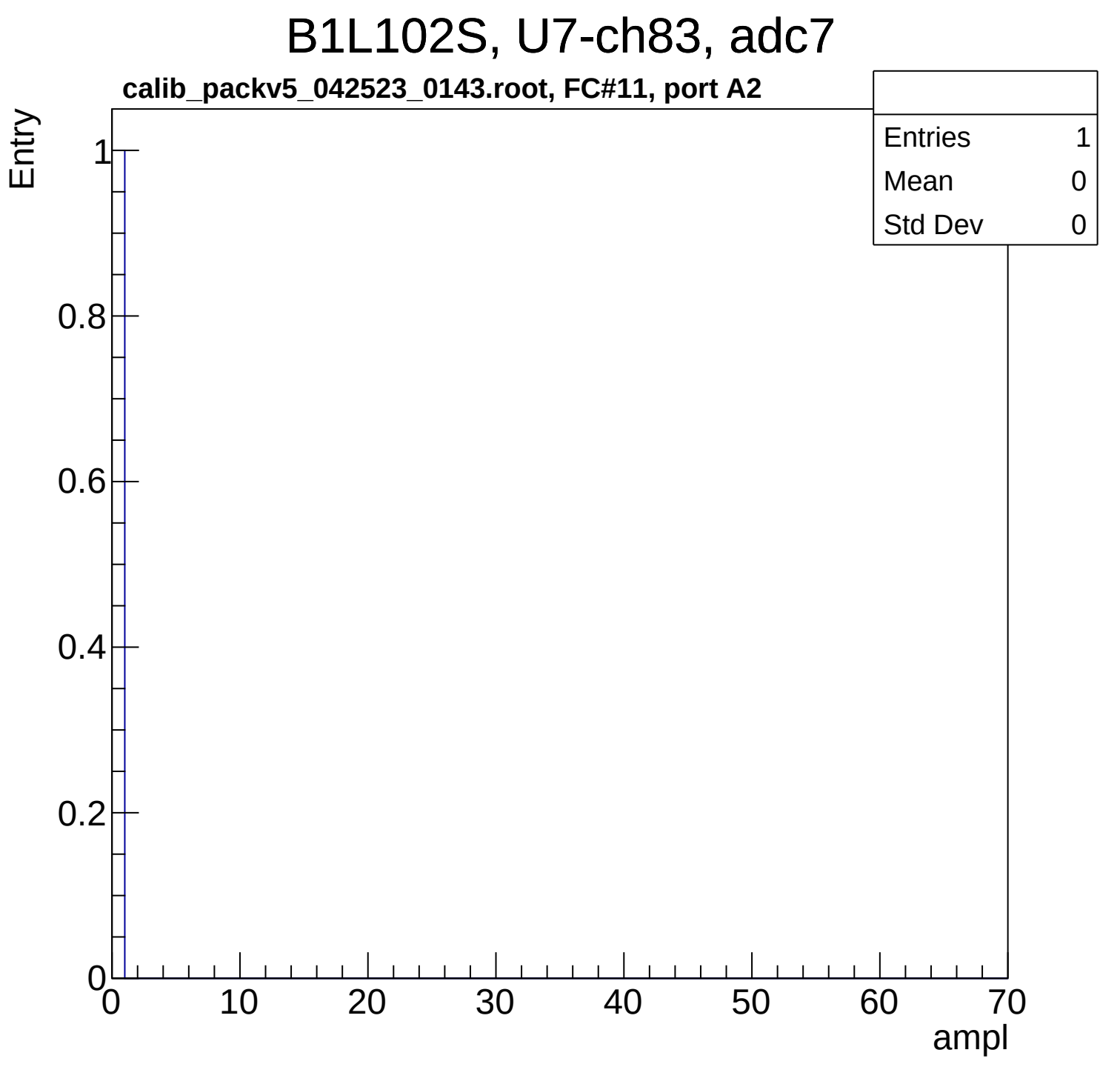
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L102S, U7-ch83, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 4
Mean 46
Std Dev 26.57
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L102S, U7-ch83, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 1
Mean 0
Std Dev 0
Entry
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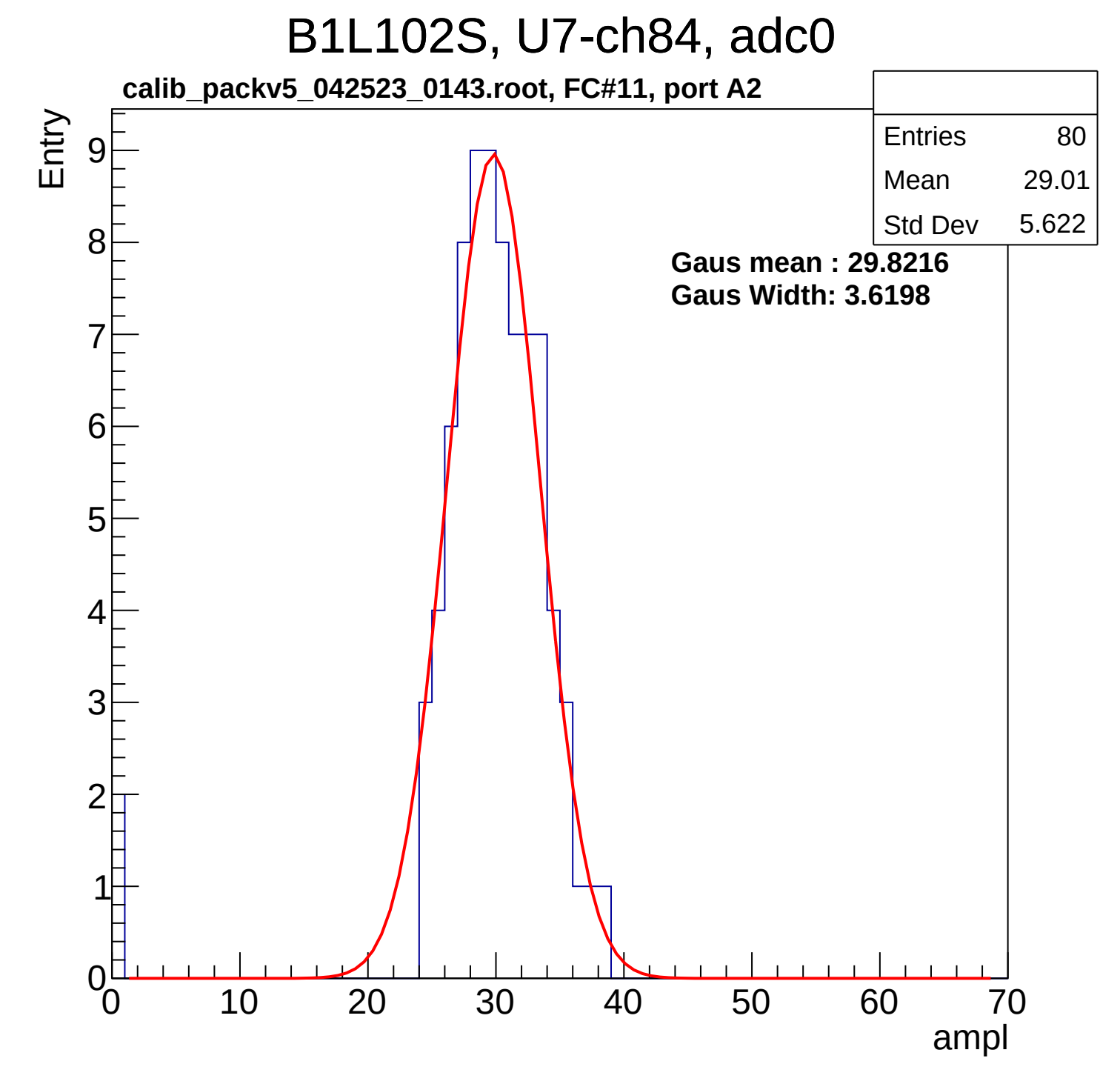
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U7-ch84, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 80
Mean 29.01
Std Dev 5.622
Gaus mean : 29.8216
Gaus Width: 3.6198
Entry
ampl
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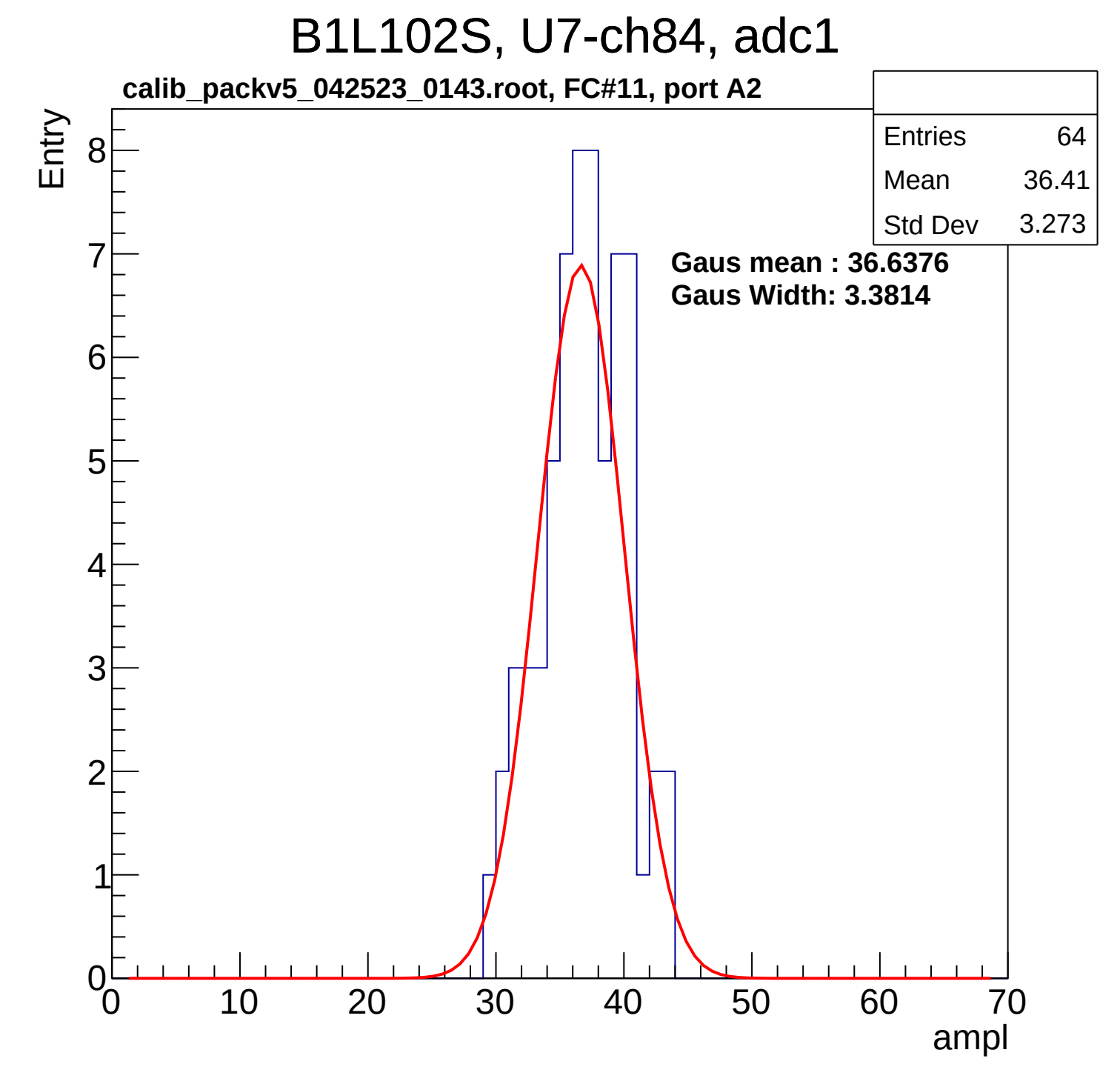
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L102S, U7-ch84, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 64
Mean 36.41
Std Dev 3.273
Gaus mean : 36.6376
Gaus Width: 3.3814
Entry
ampl
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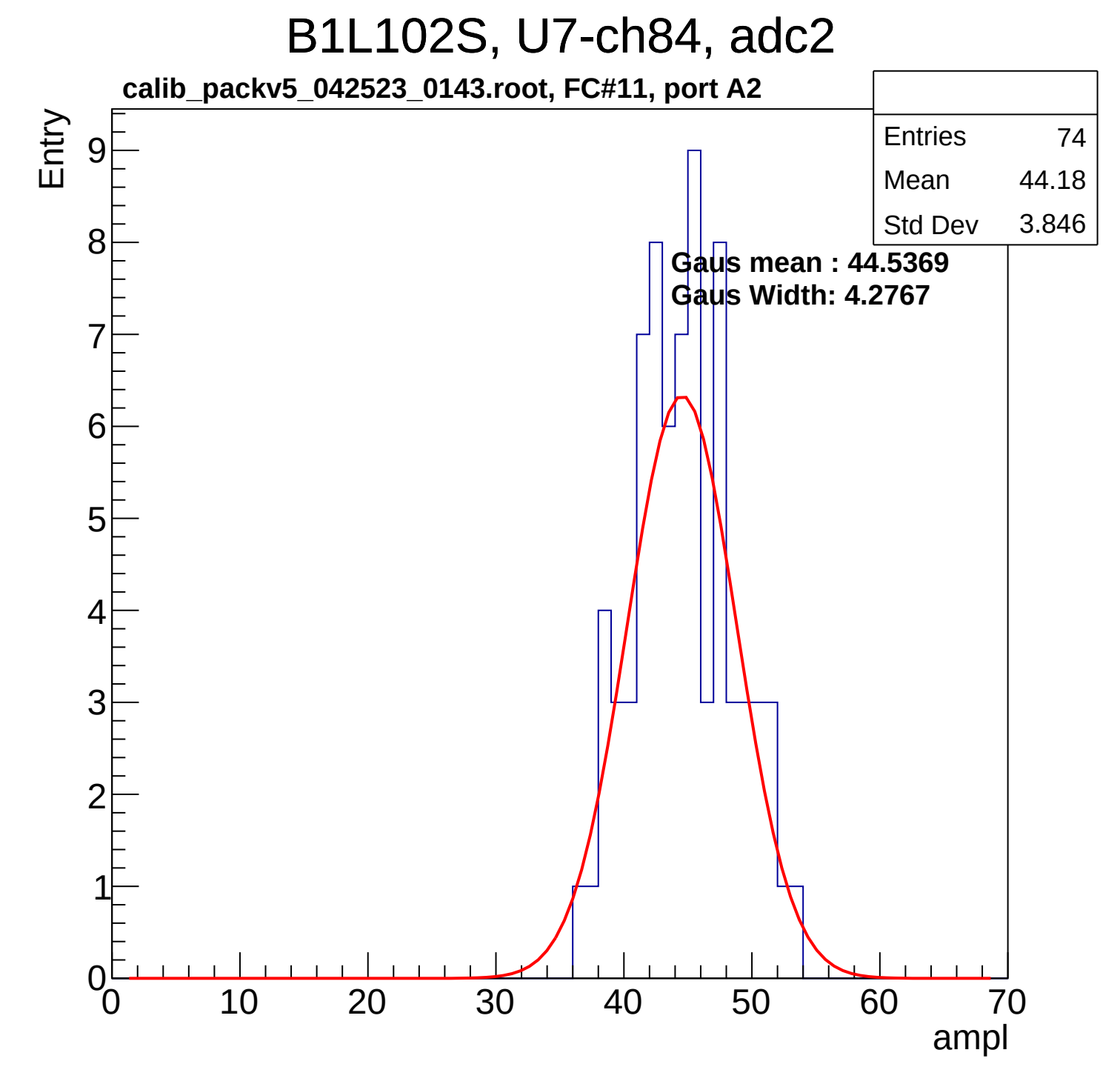
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L102S, U7-ch84, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 74
Mean 44.18
Std Dev 3.846
Gaus mean : 44.5369
Gaus Width: 4.2767
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
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40
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60
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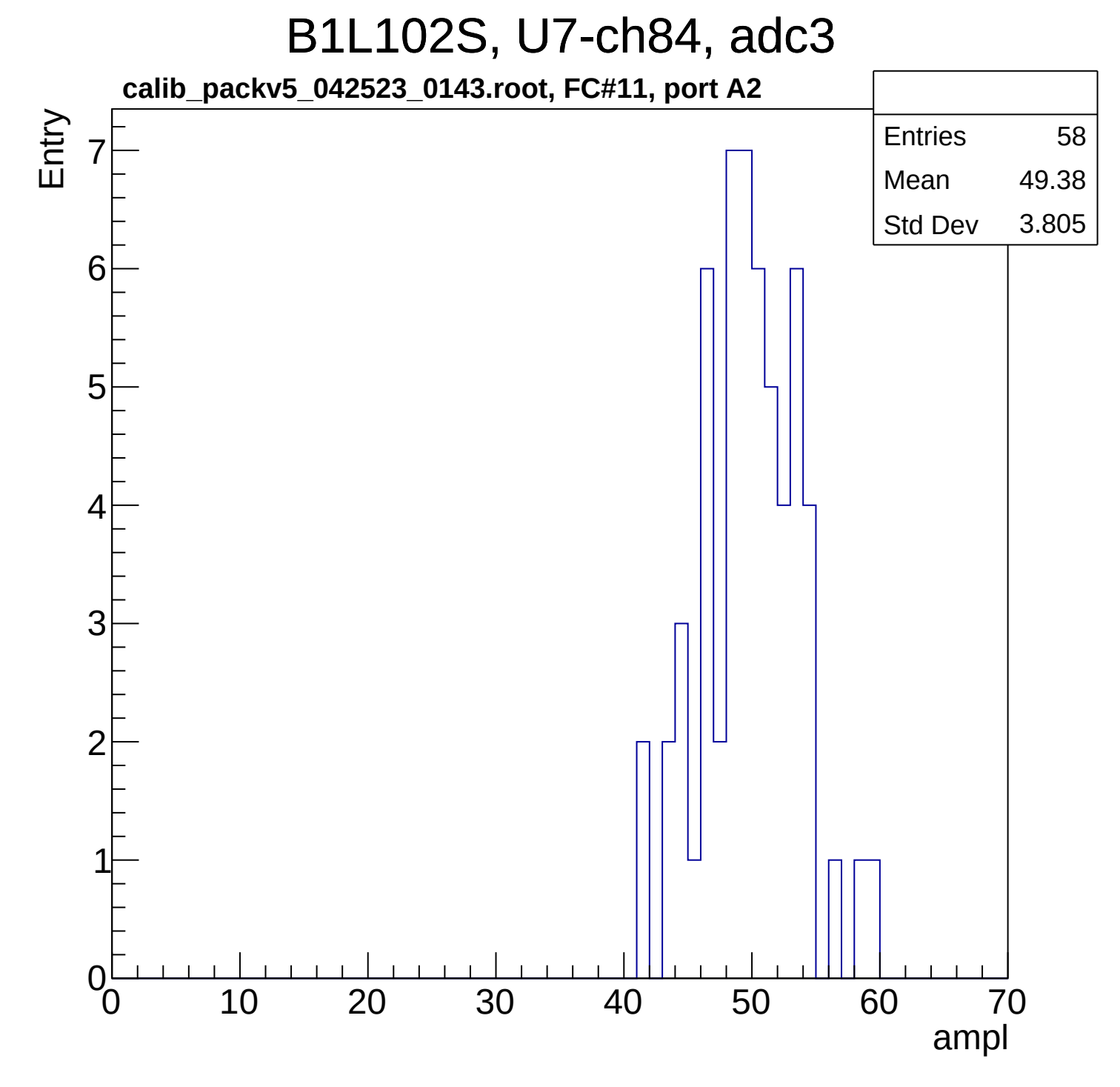
B1L102S, U7-ch84, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 58
Mean 49.38
Std Dev 3.805
Entry
ampl
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2
3
4
5
6
7
0
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20
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60
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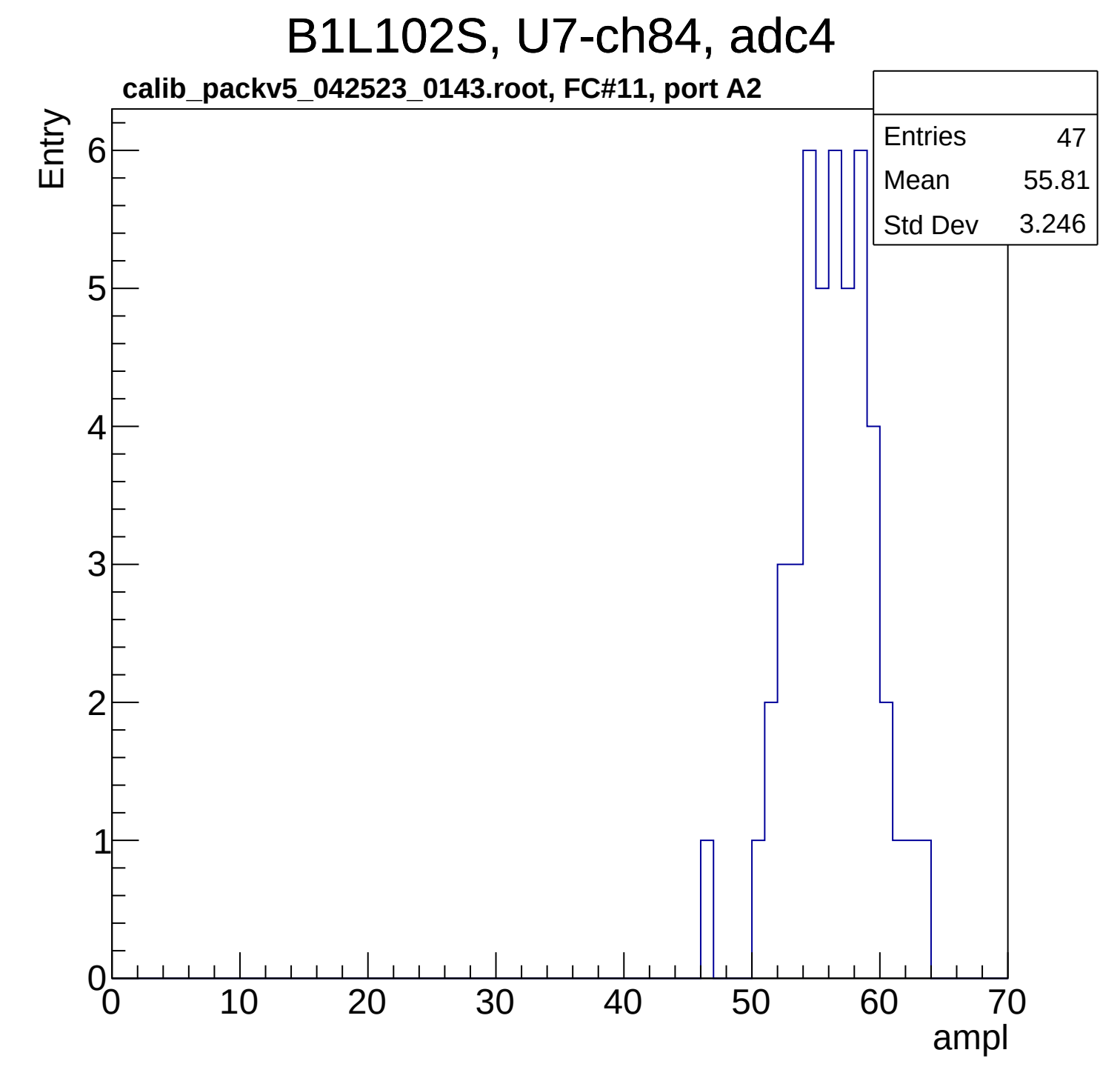
B1L102S, U7-ch84, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 47
Mean 55.81
Std Dev 3.246
Entry
ampl
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2
3
4
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6
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20
30
40
50
60
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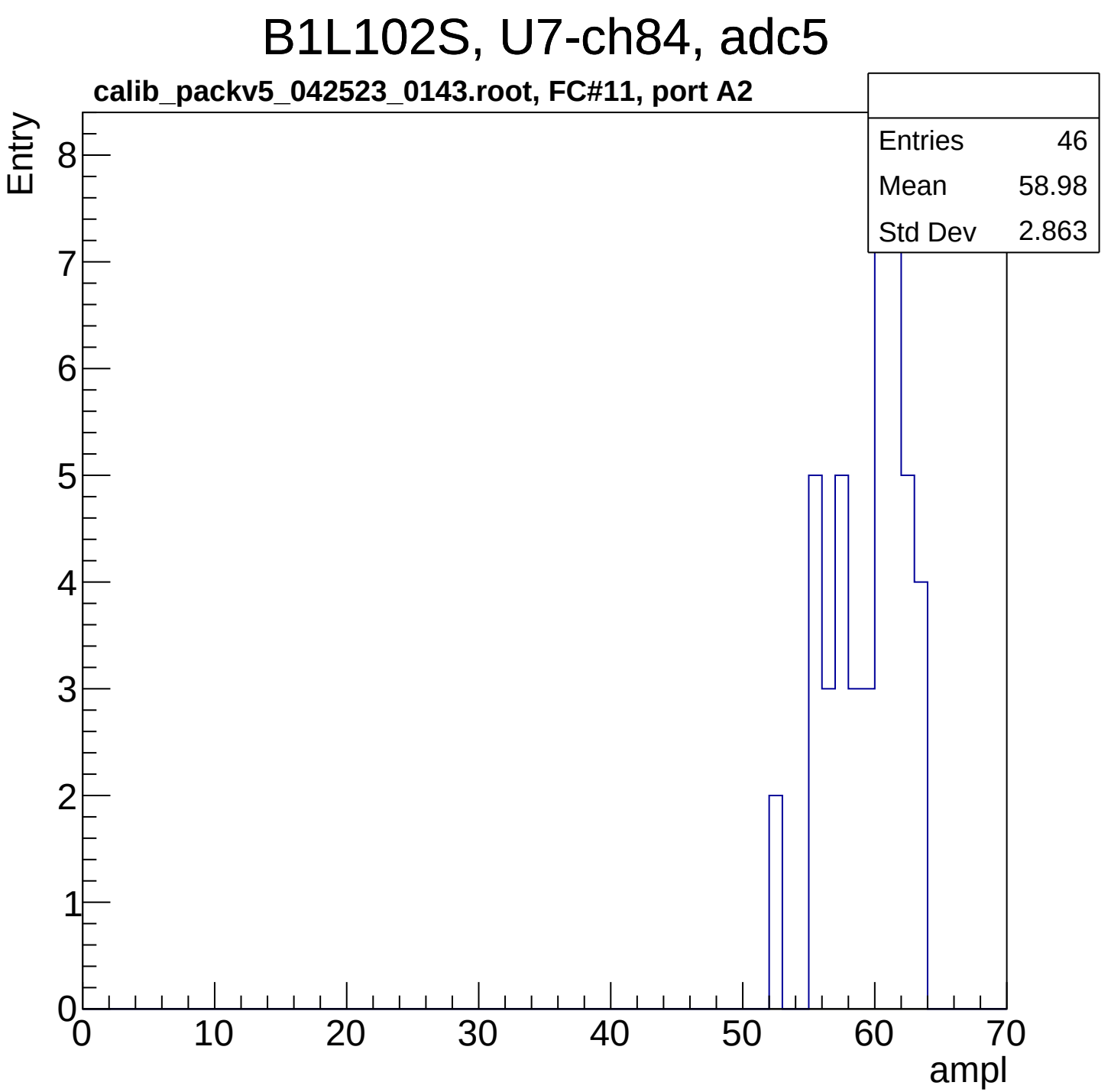
B1L102S, U7-ch84, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 46
Mean 58.98
Std Dev 2.863
Entry
ampl
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3
4
5
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7
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20
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40
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60
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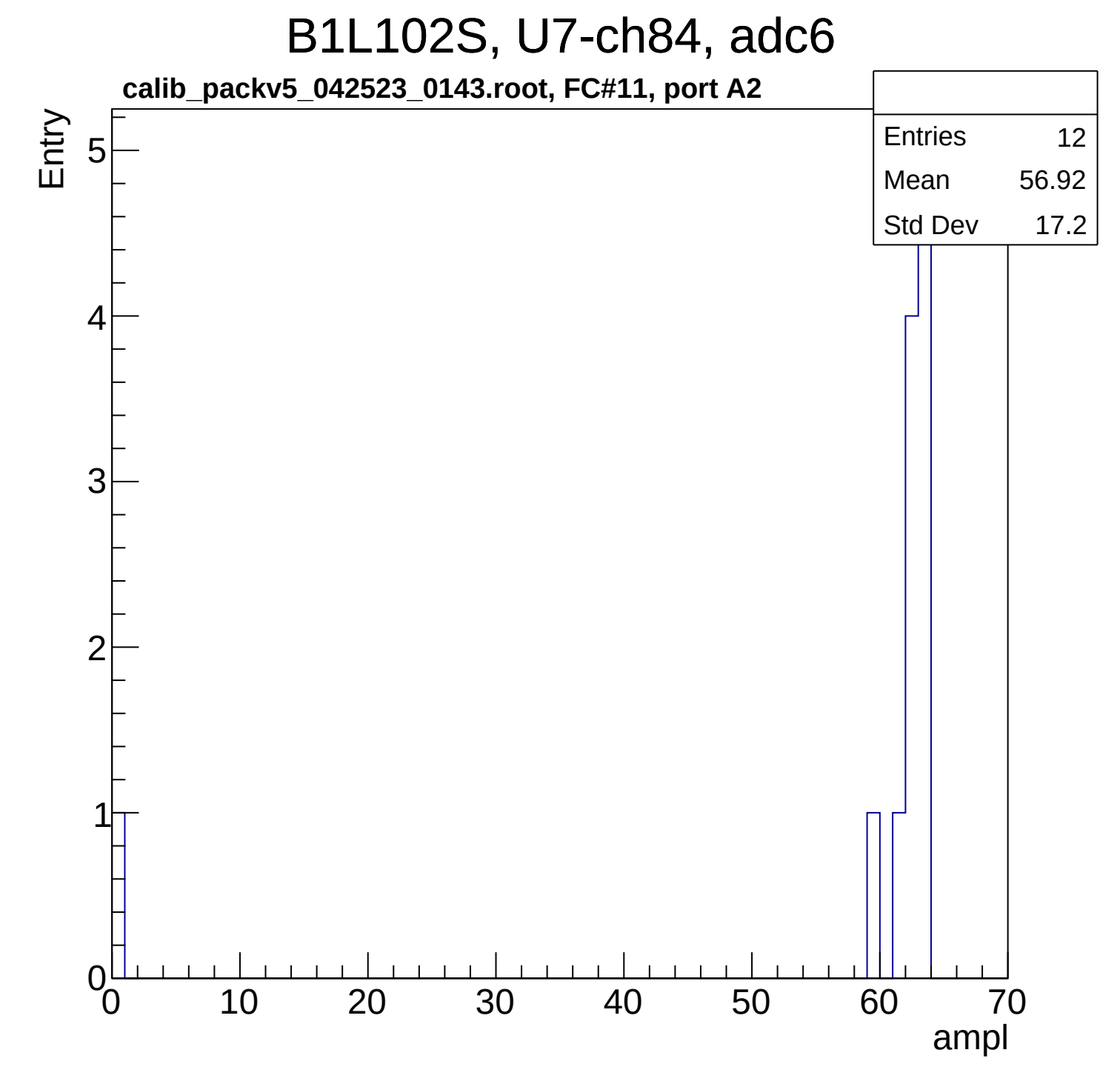
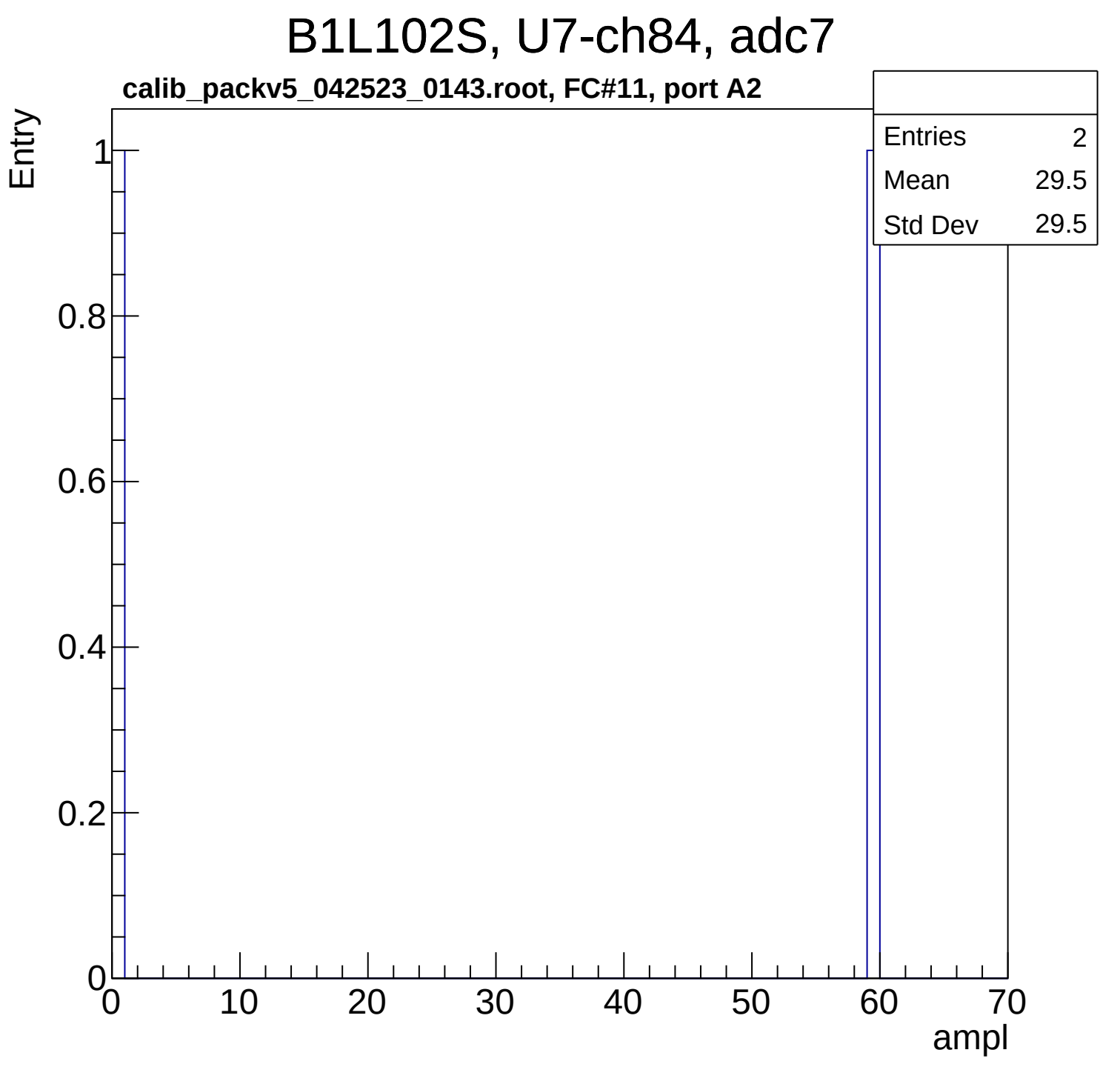
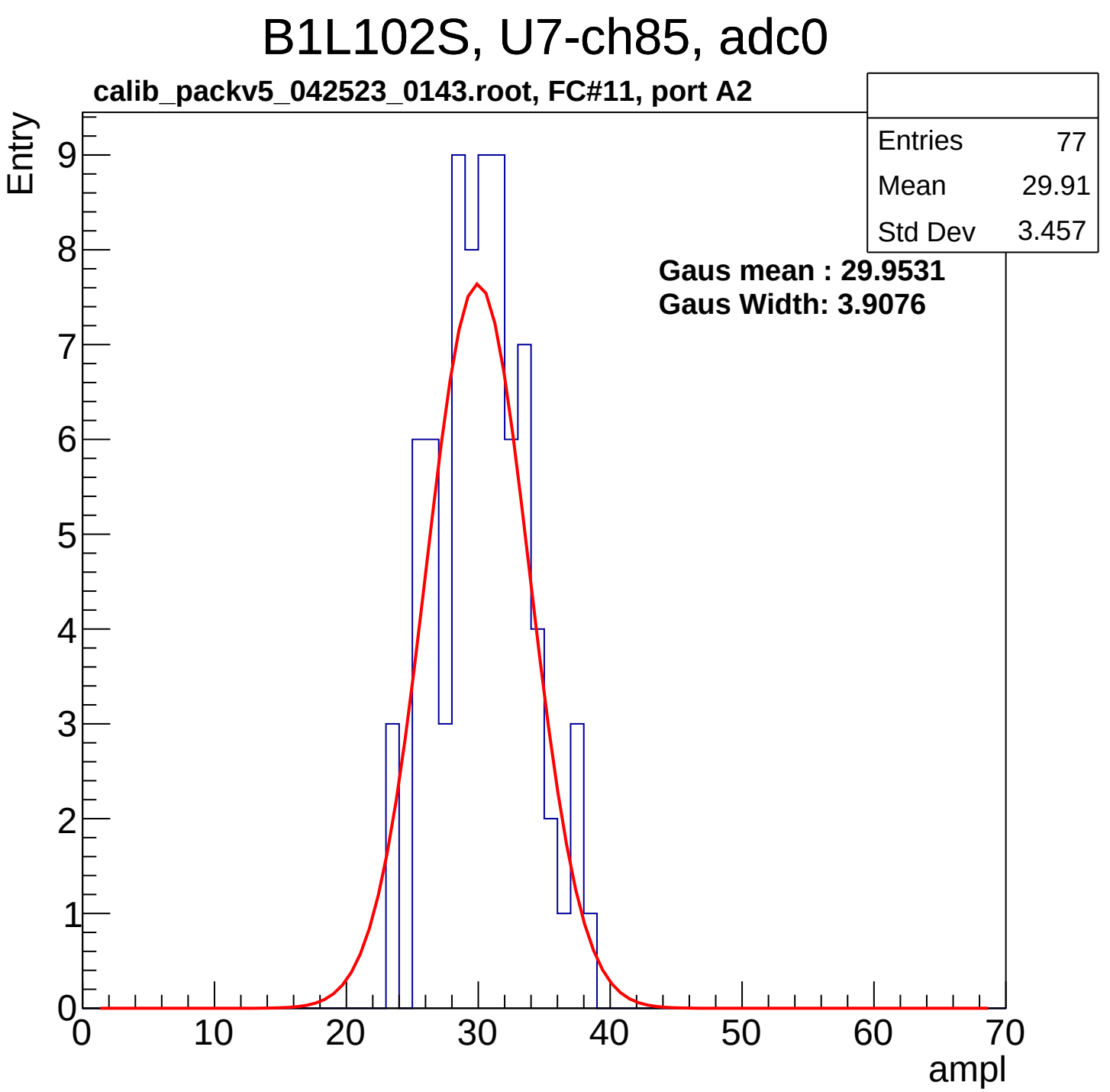

B1L102S, U7-ch84, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 12
Mean 56.92
Std Dev 17.2
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L102S, U7-ch84, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 2
Mean 29.5
Std Dev 29.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U7-ch85, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 77
Mean 29.91
Std Dev 3.457
Gaus mean : 29.9531
Gaus Width: 3.9076
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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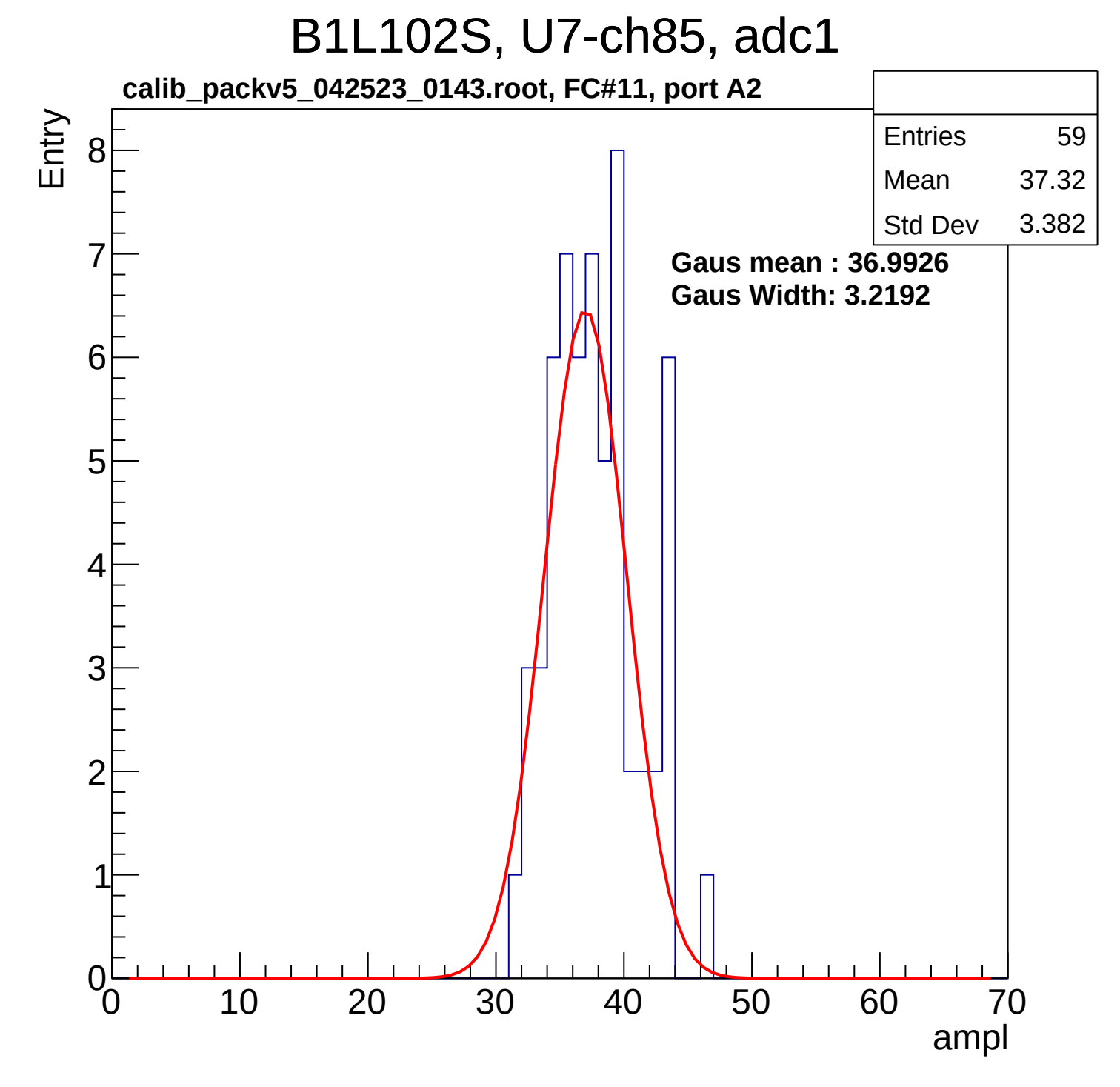
B1L102S, U7-ch85, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 59
Mean 37.32
Std Dev 3.382
Gaus mean : 36.9926
Gaus Width: 3.2192
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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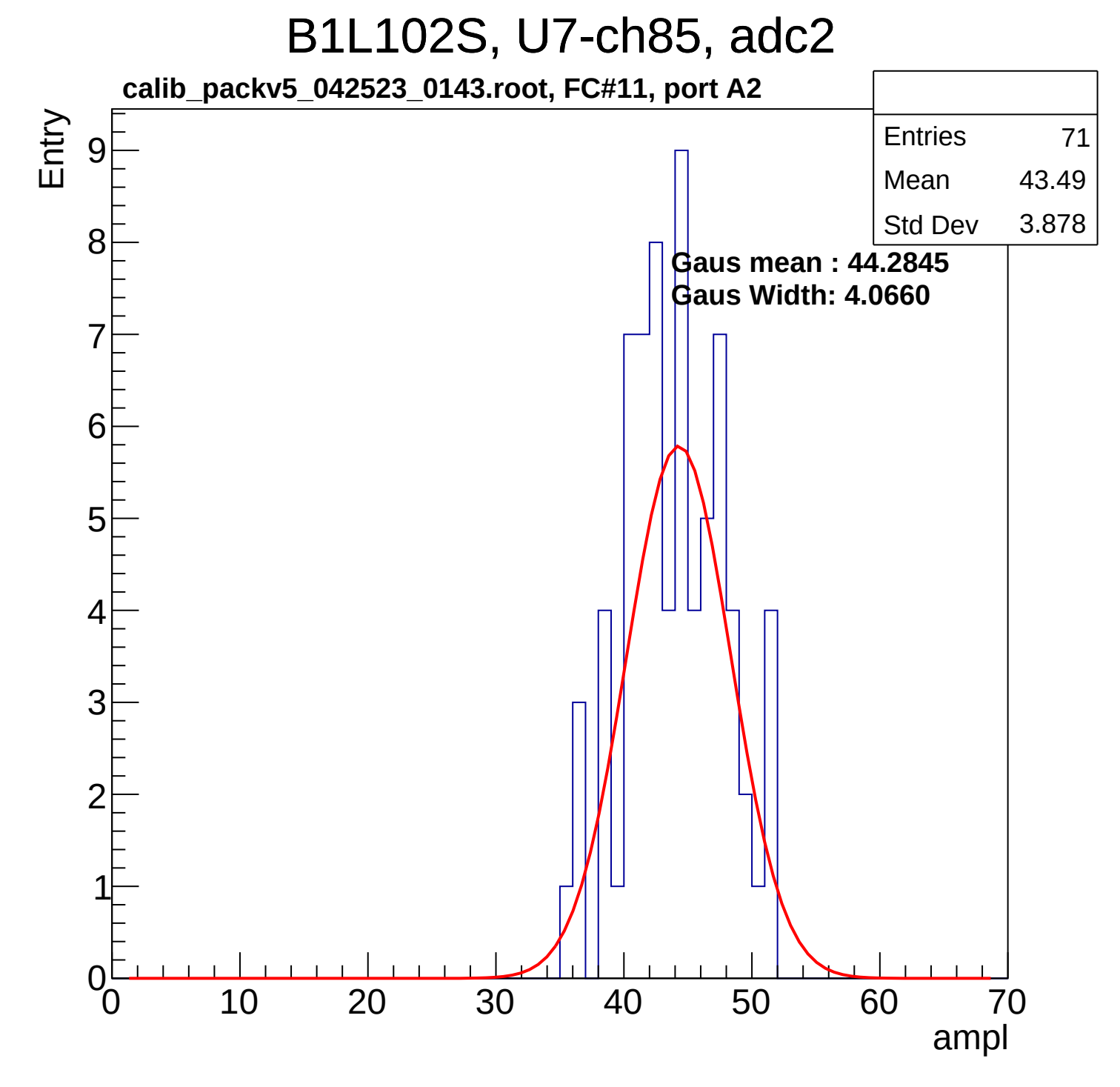
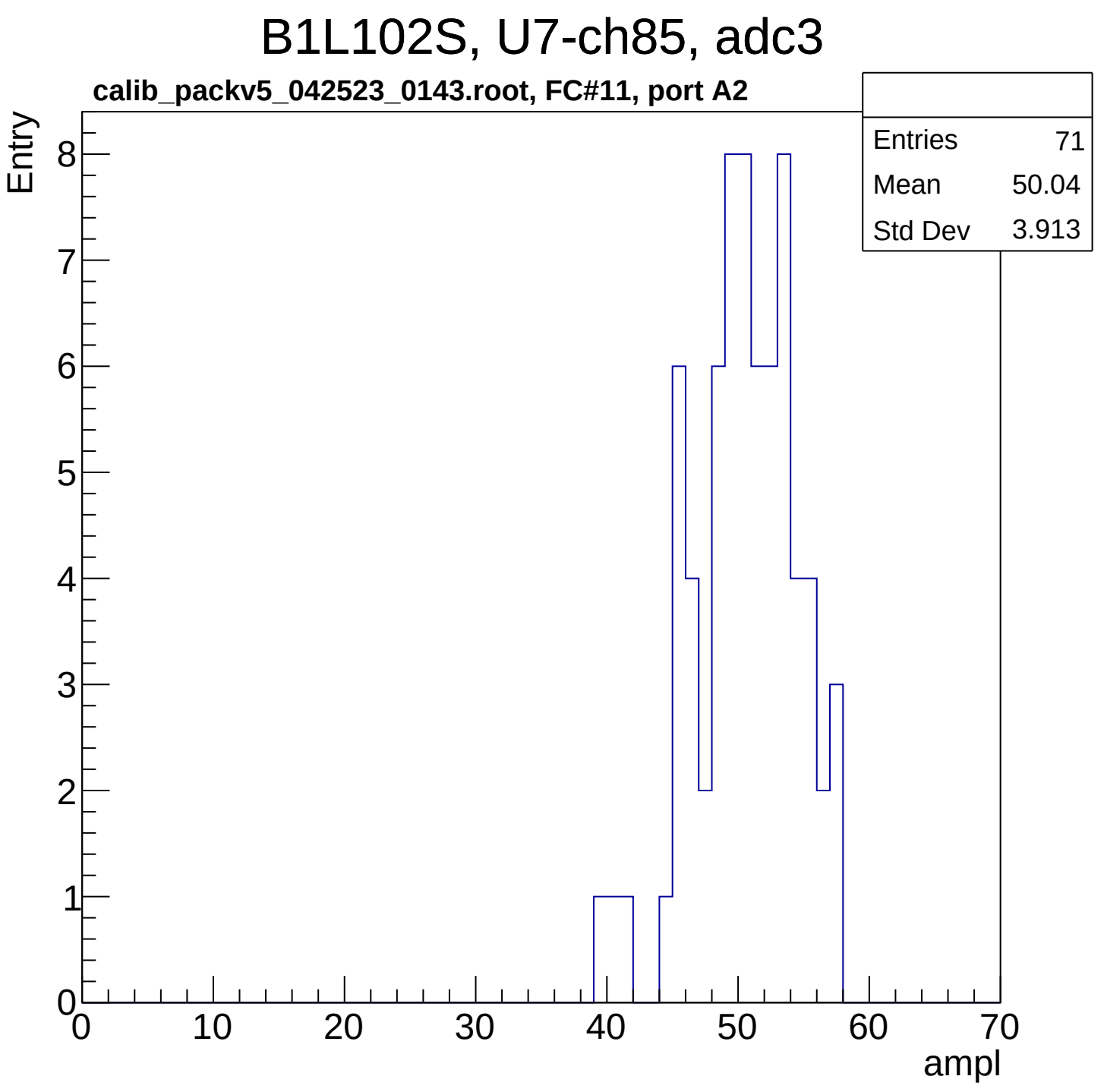

B1L102S, U7-ch85, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 71
Mean 43.49
Std Dev 3.878
Gaus mean : 44.2845
Gaus Width: 4.0660
Entry
ampl
0
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9


B1L102S, U7-ch85, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 71
Mean 50.04
Std Dev 3.913
Entry
0
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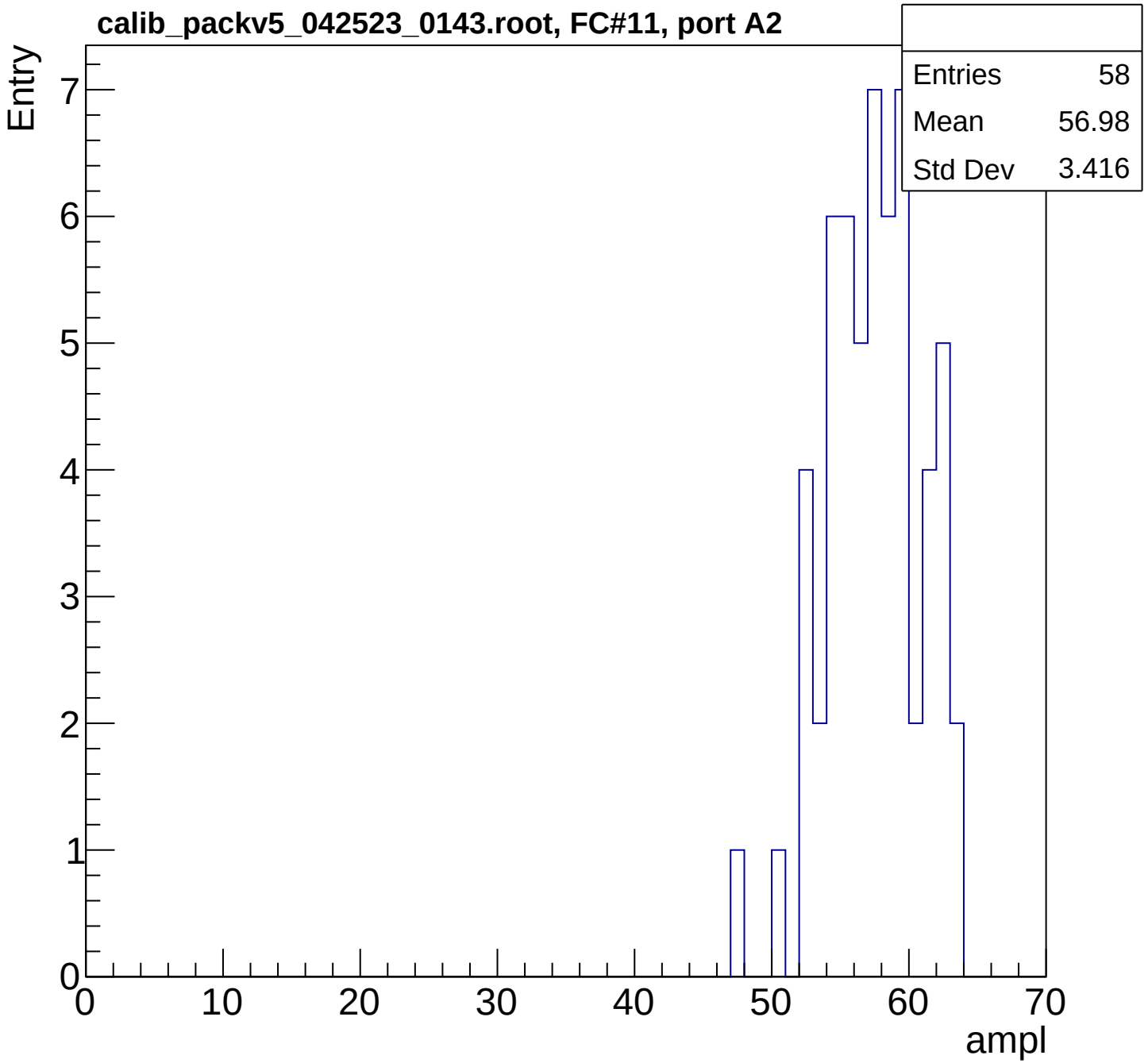
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L102S, U7-ch85, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 58
Mean 56.98
Std Dev 3.416
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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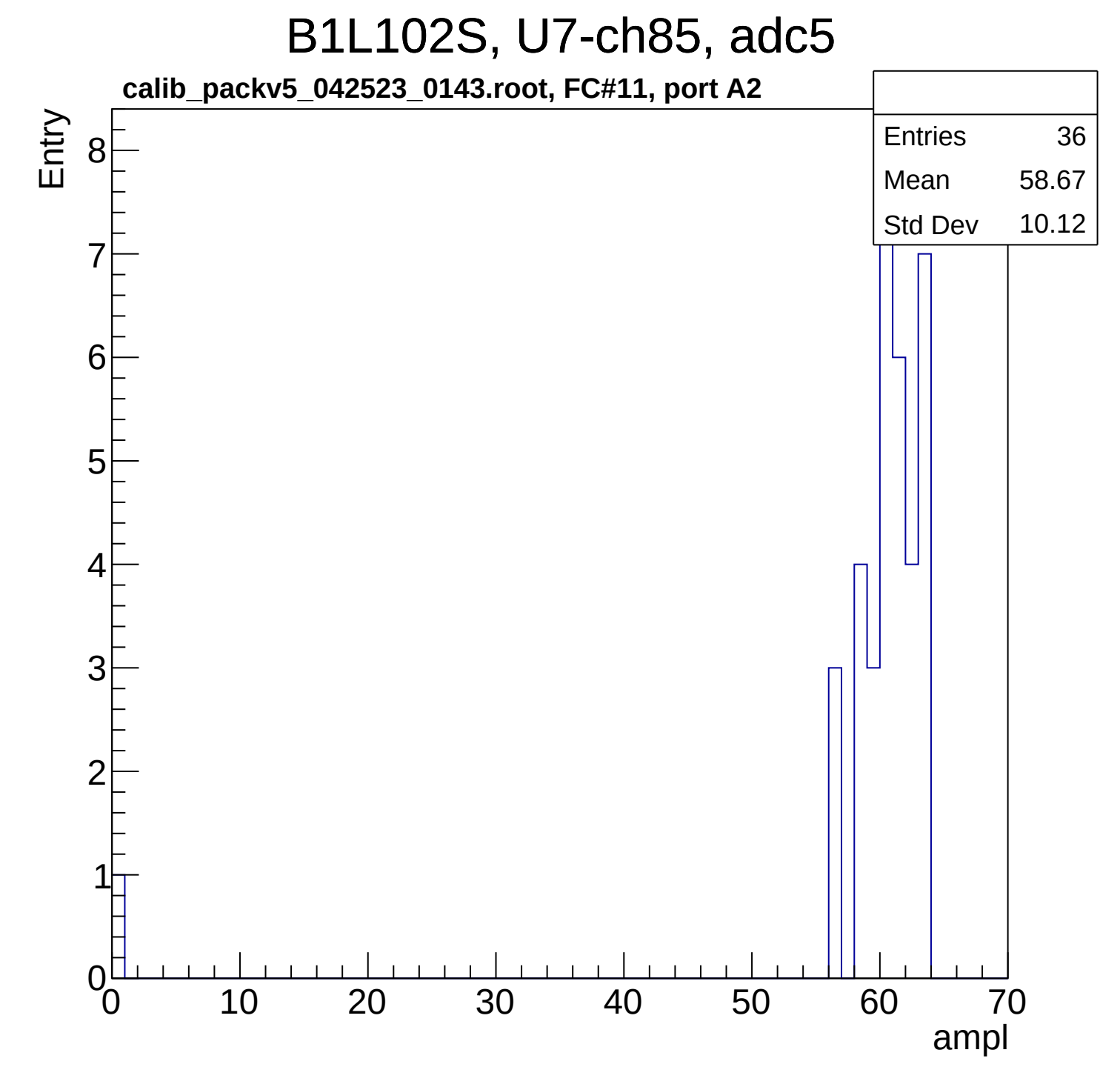
B1L102S, U7-ch85, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 36
Mean 58.67
Std Dev 10.12
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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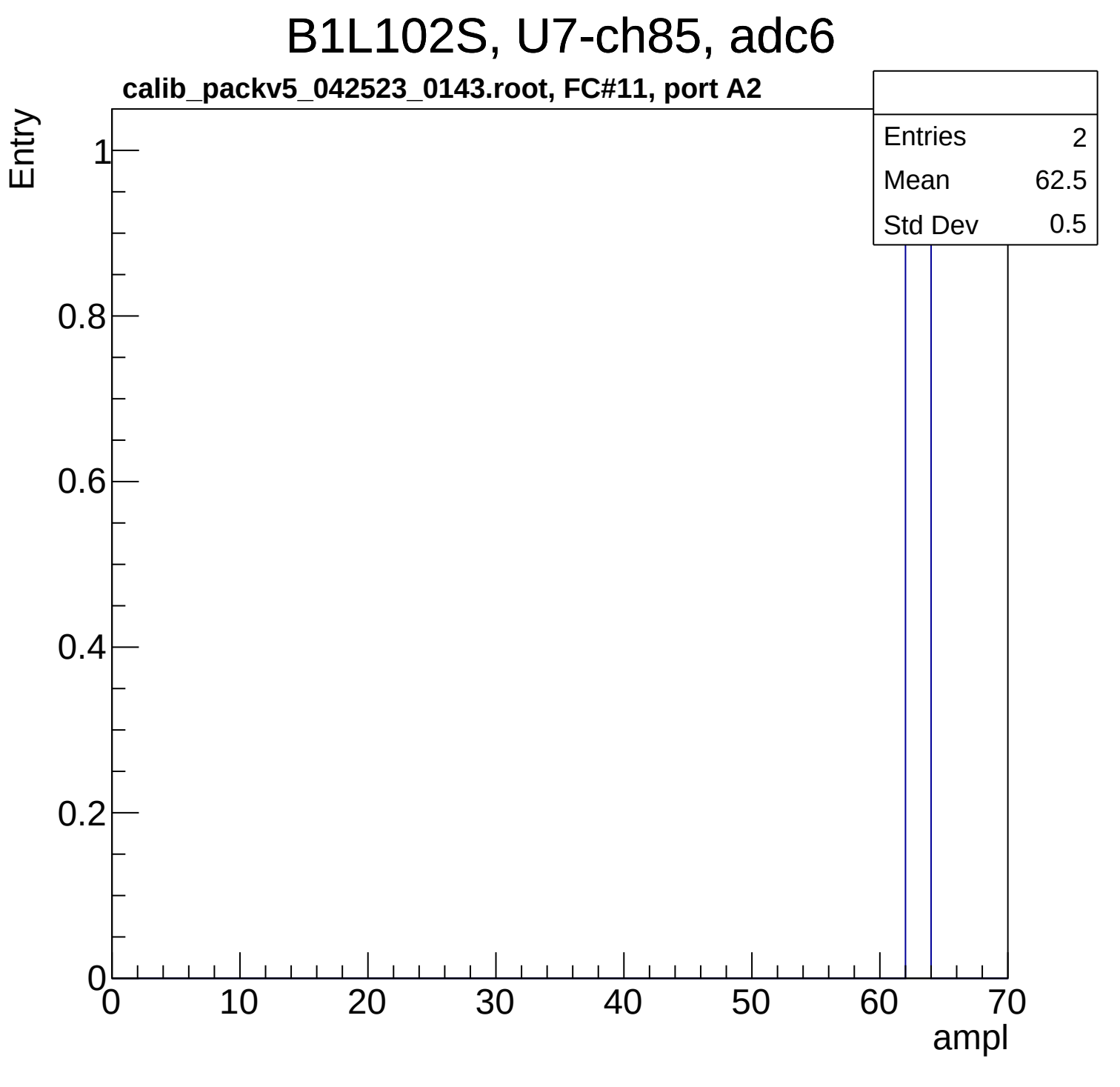
B1L102S, U7-ch85, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 2
Mean 62.5
Std Dev 0.5
Entry
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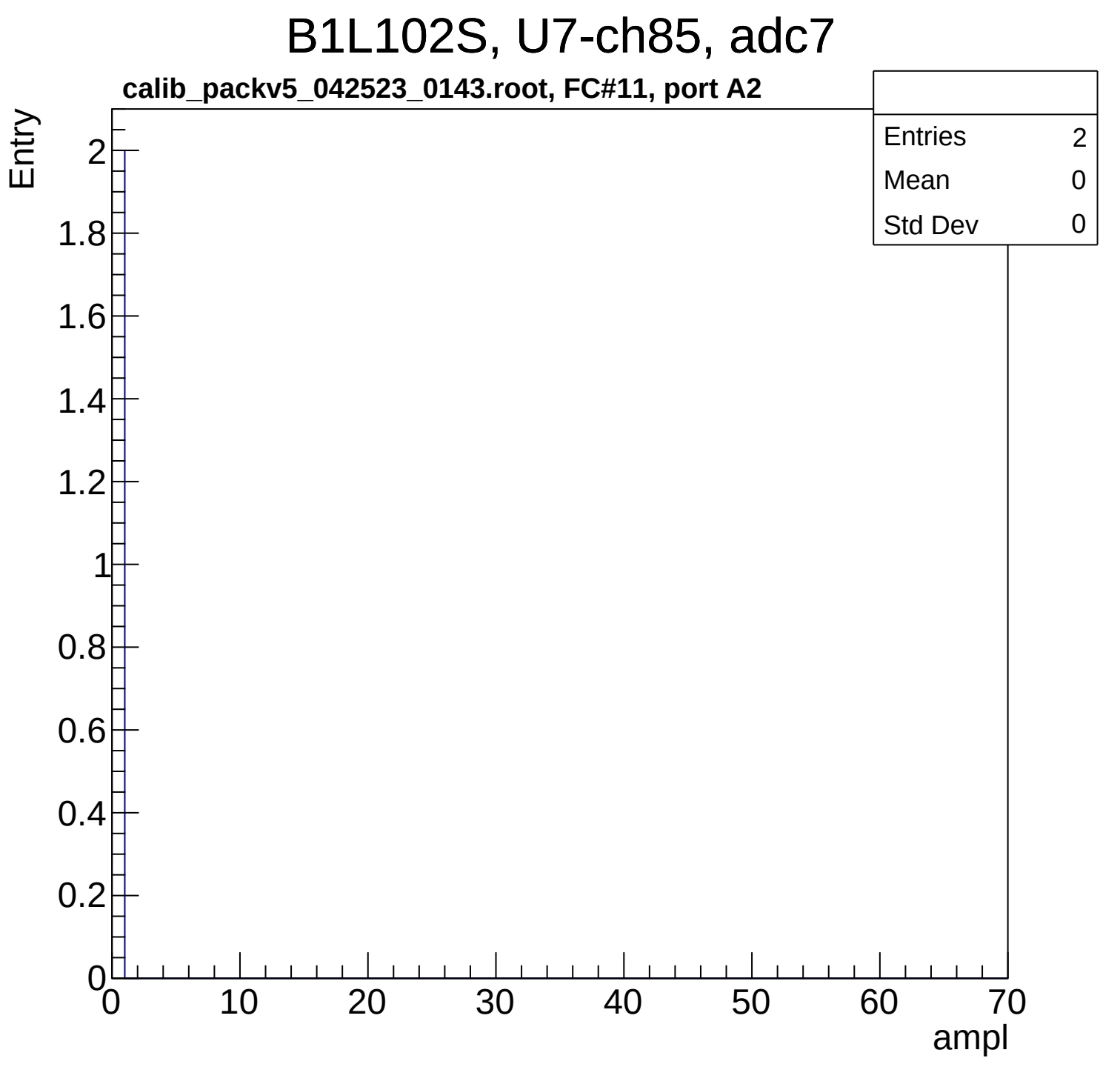
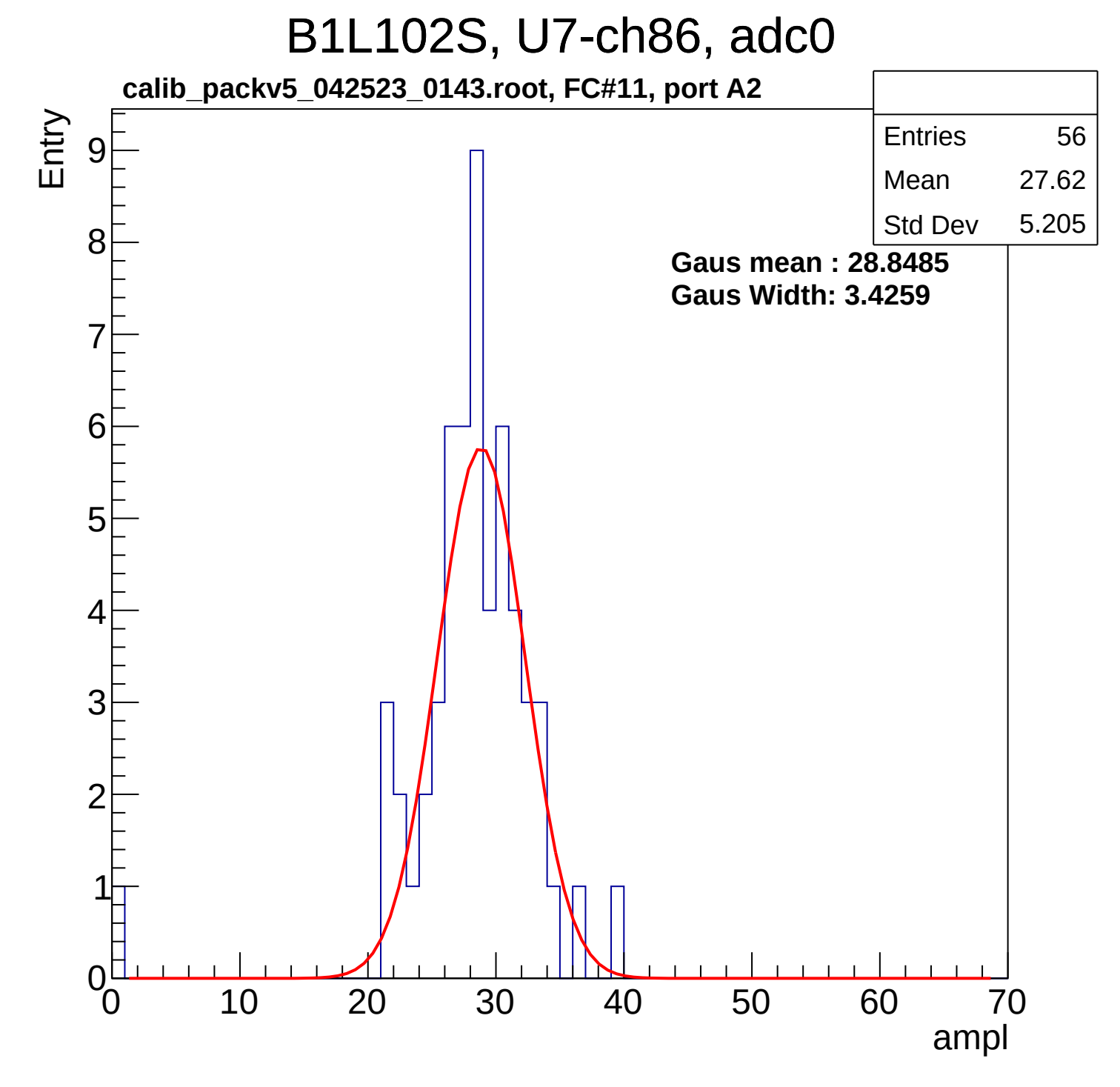
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U7-ch85, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 2
Mean 0
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L102S, U7-ch86, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 56
Mean 27.62
Std Dev 5.205
Gaus mean : 28.8485
Gaus Width: 3.4259
Entry
ampl
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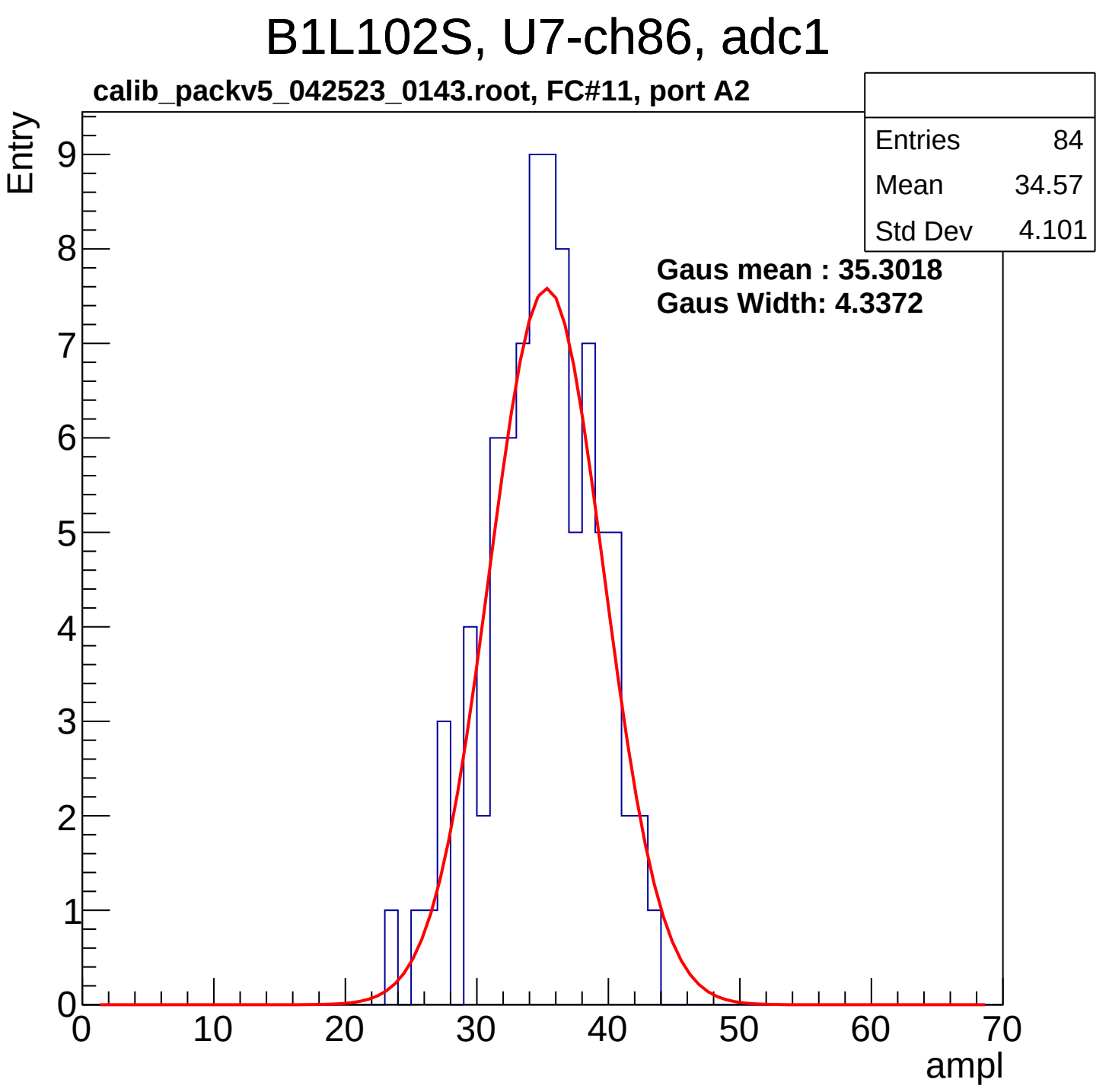
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L102S, U7-ch86, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 84
Mean 34.57
Std Dev 4.101
Gaus mean : 35.3018
Gaus Width: 4.3372
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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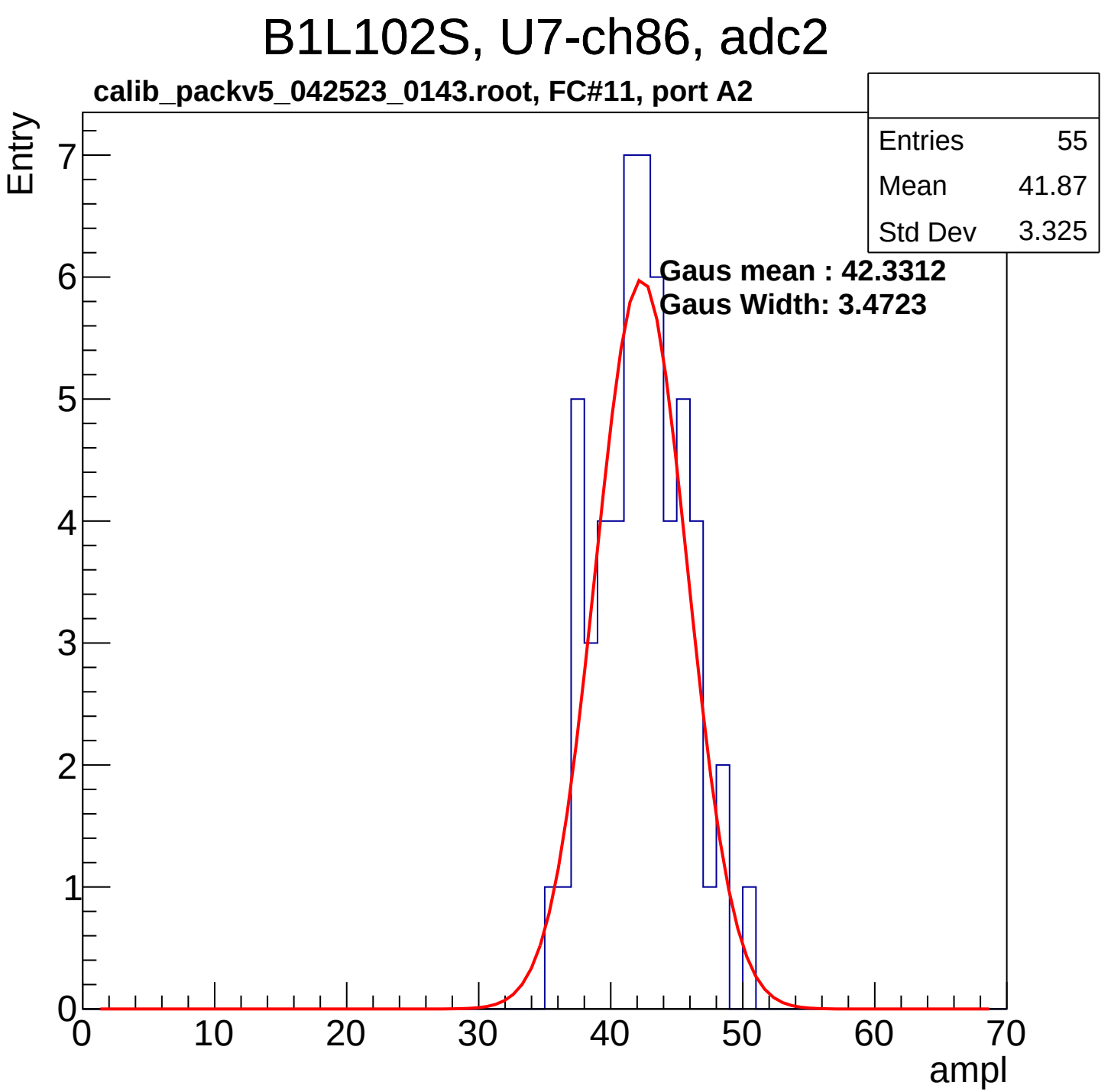
B1L102S, U7-ch86, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 55
Mean 41.87
Std Dev 3.325
Gaus mean : 42.3312
Gaus Width: 3.4723
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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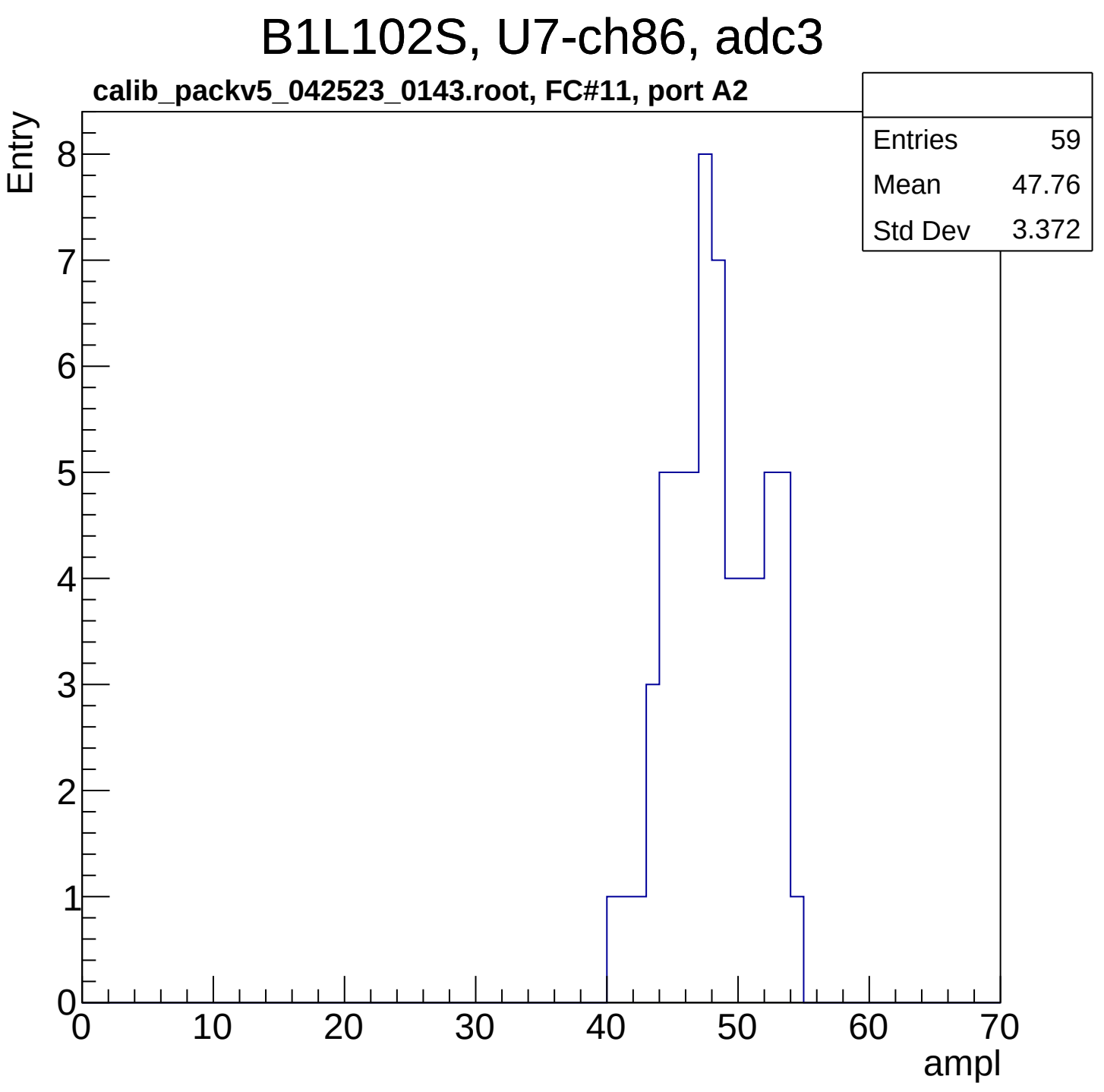
B1L102S, U7-ch86, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 59
Mean 47.76
Std Dev 3.372
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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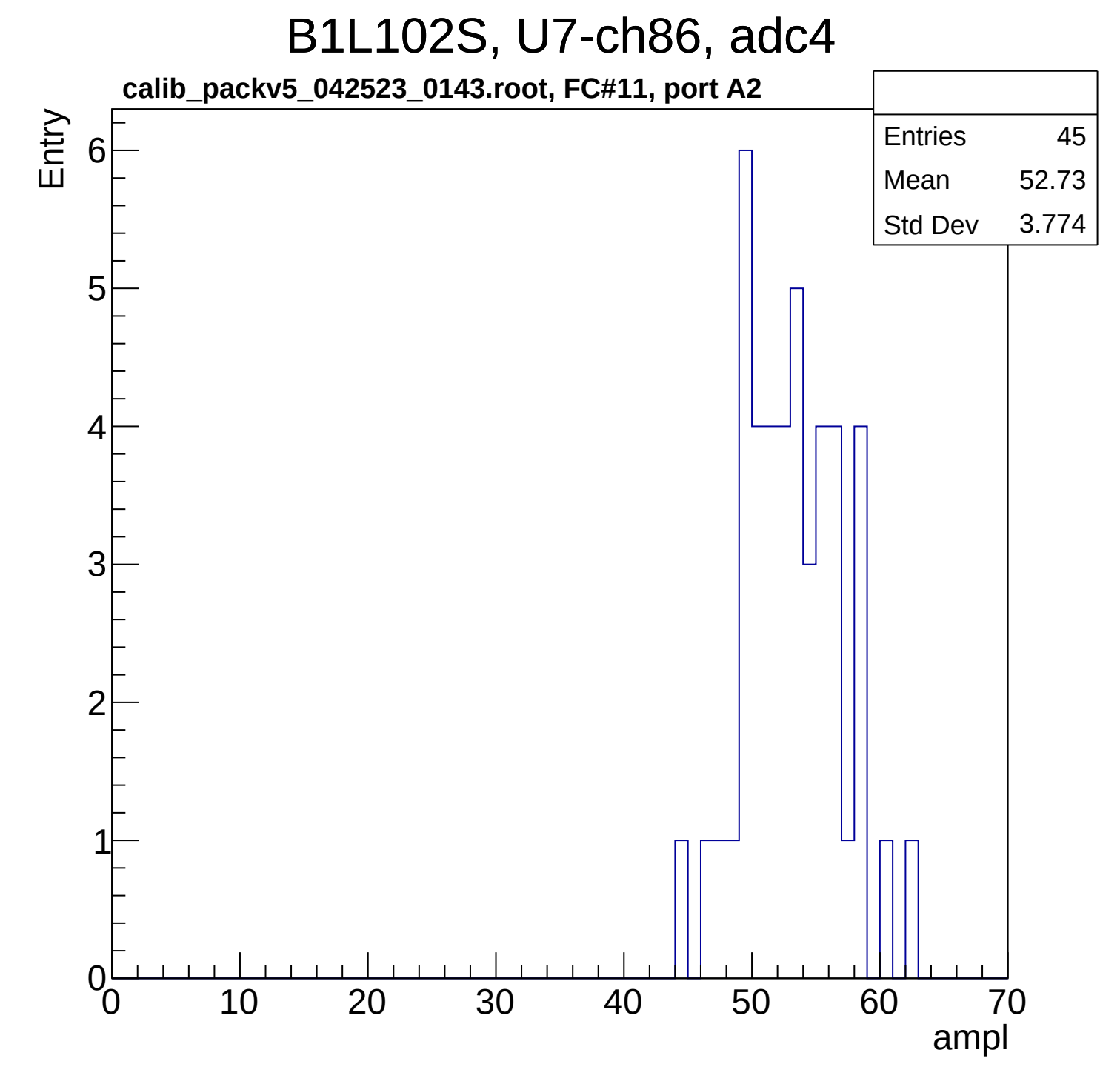
B1L102S, U7-ch86, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 45
Mean 52.73
Std Dev 3.774
Entry
ampl
0
1
2
3
4
5
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0
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20
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40
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60
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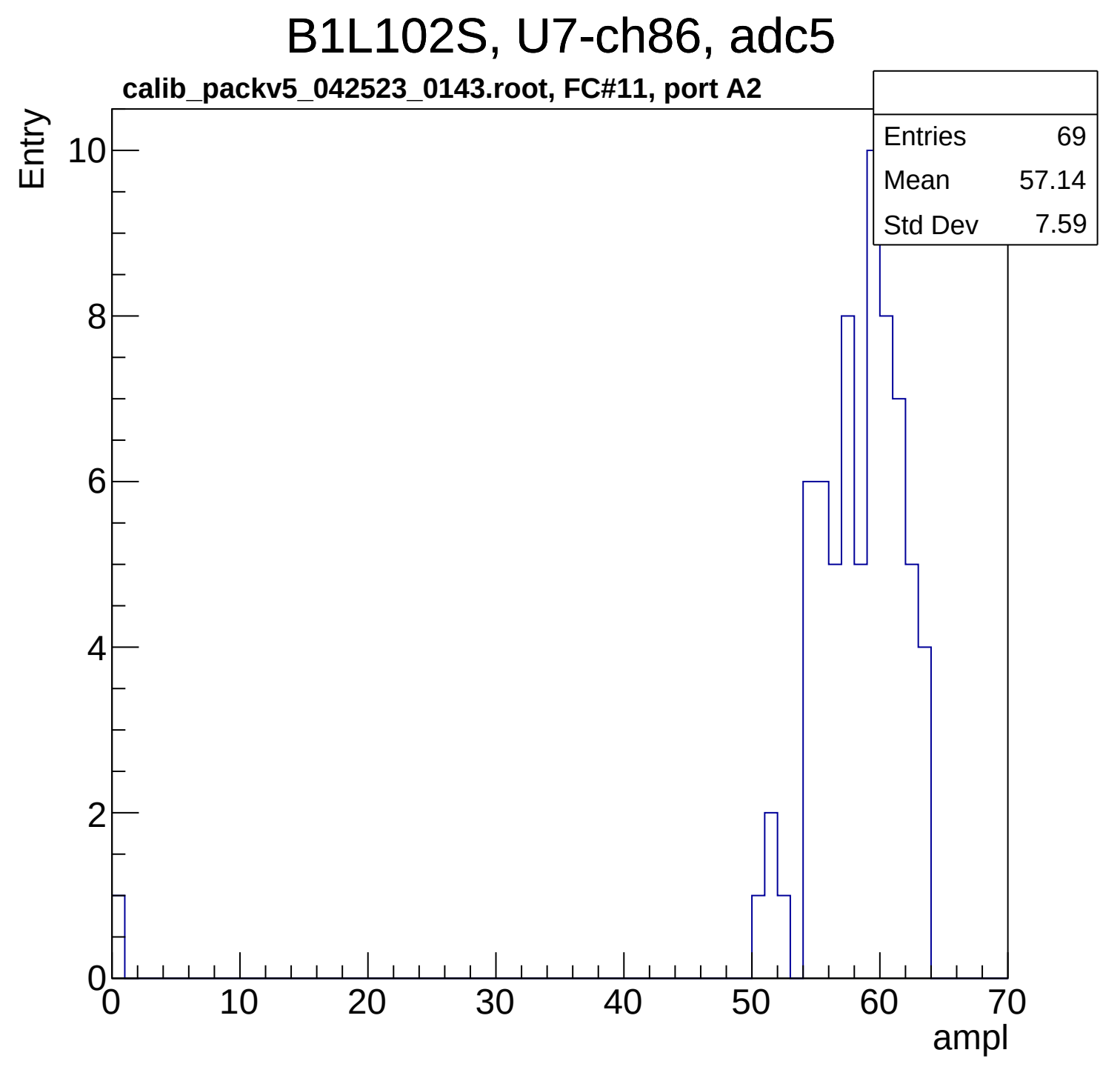
B1L102S, U7-ch86, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 69
Mean 57.14
Std Dev 7.59
Entry
ampl
0
2
4
6
8
10
0
10
20
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40
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60
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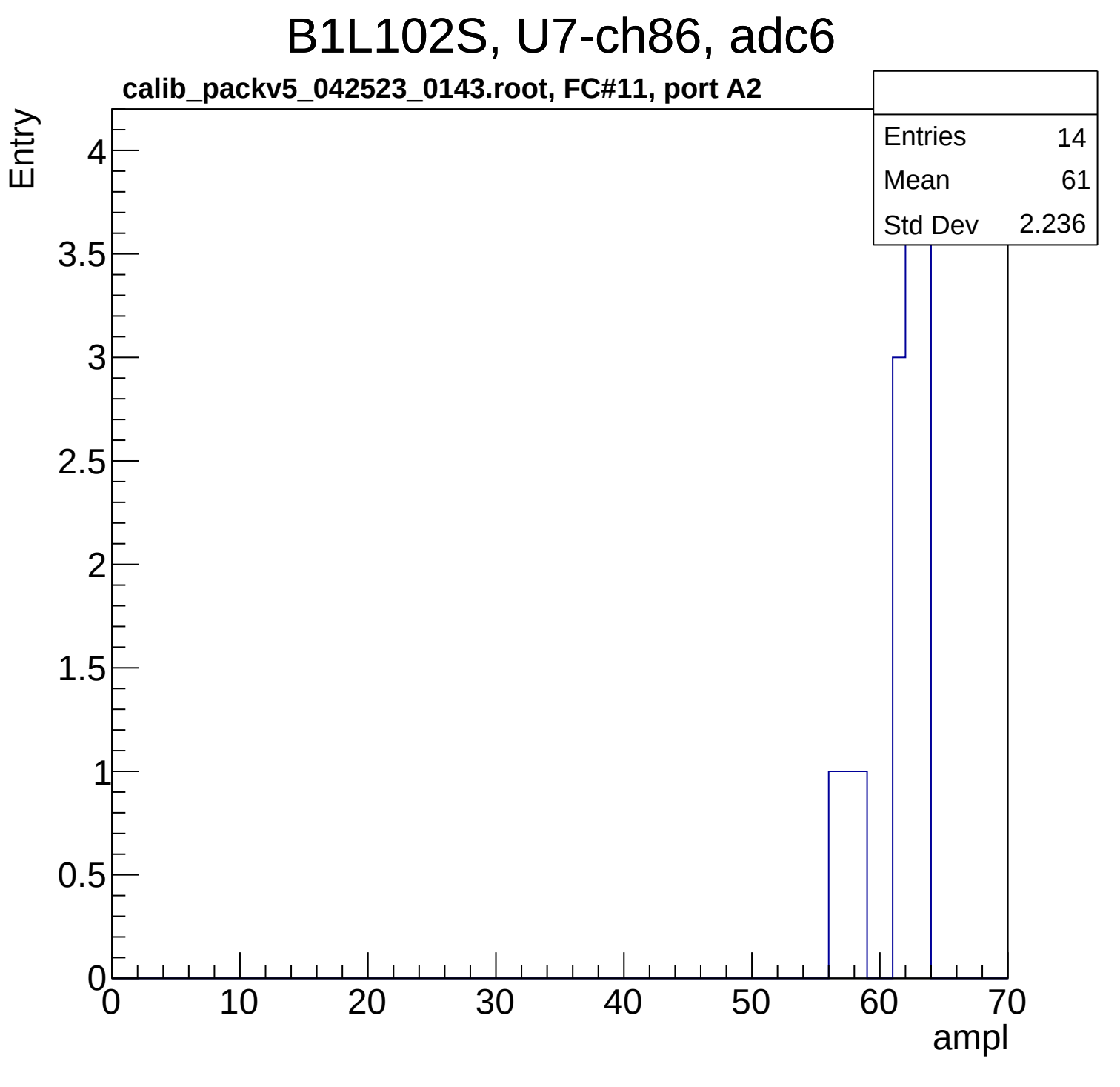
B1L102S, U7-ch86, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 14
Mean 61
Std Dev 2.236
Entry
ampl
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0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
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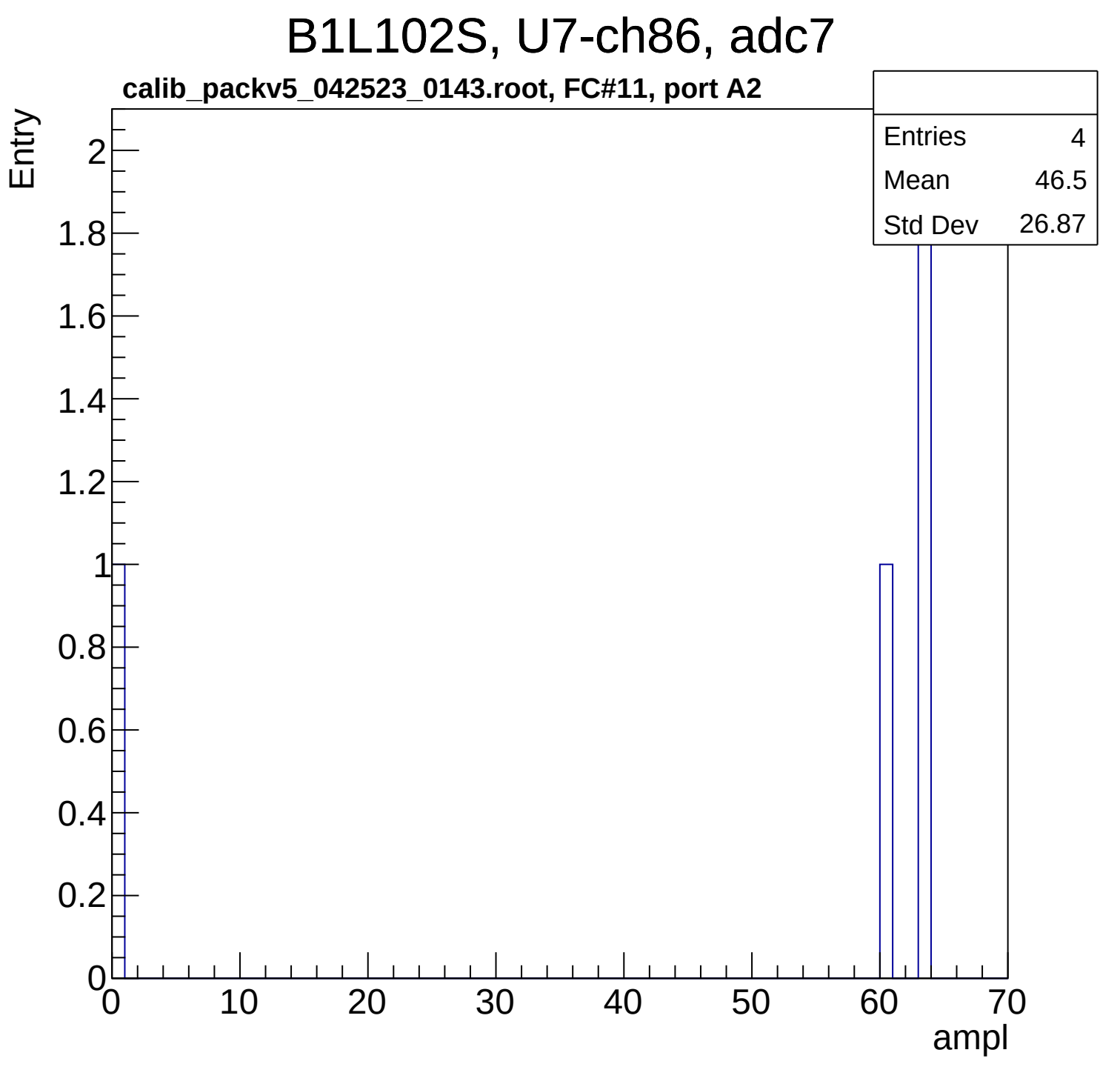
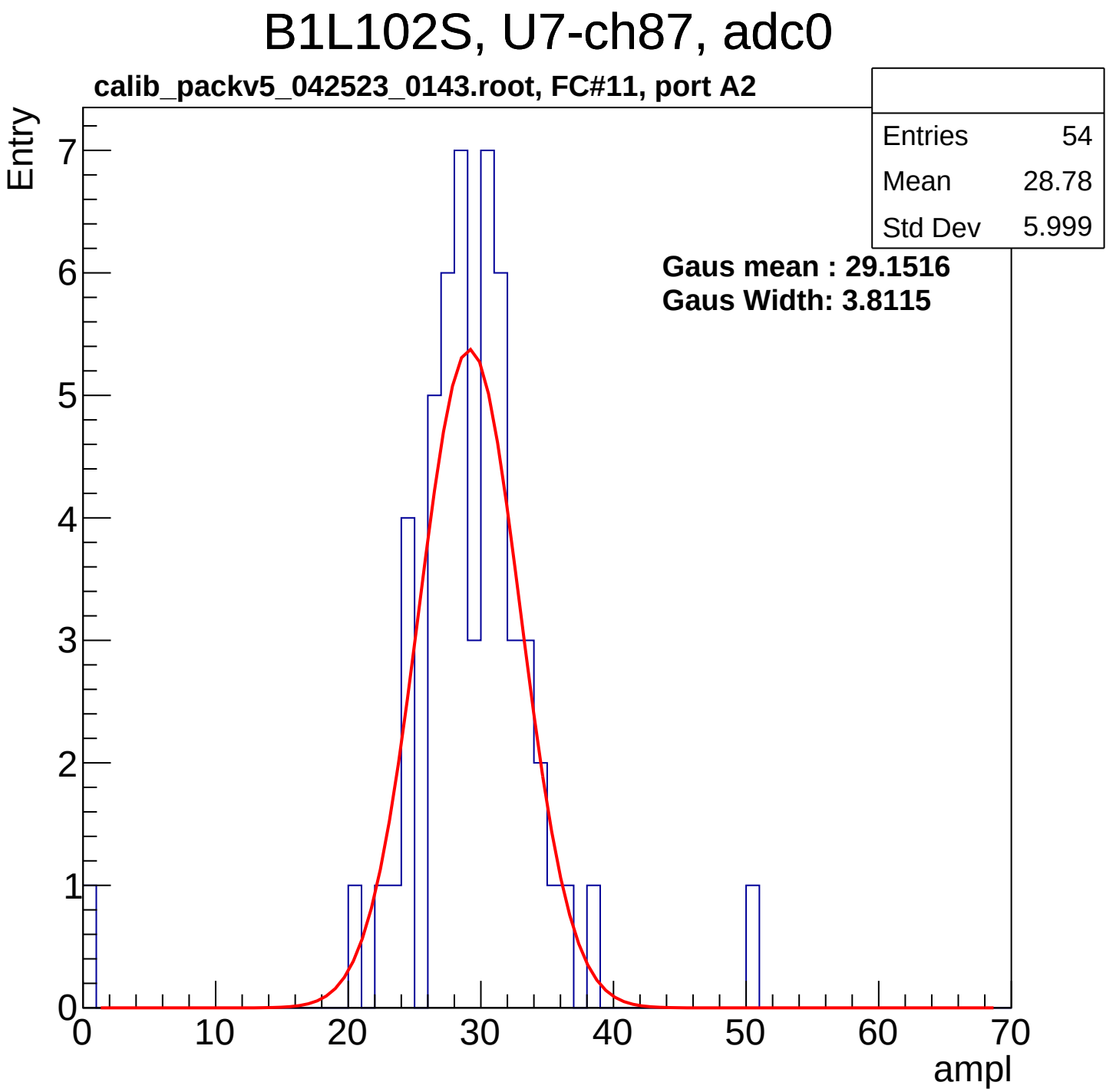
60
70


B1L102S, U7-ch86, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 4
Mean 46.5
Std Dev 26.87
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L102S, U7-ch87, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 54
Mean 28.78
Std Dev 5.999
Gaus mean : 29.1516
Gaus Width: 3.8115
Entry
ampl
0
1
2
3
4
5
6
7
0
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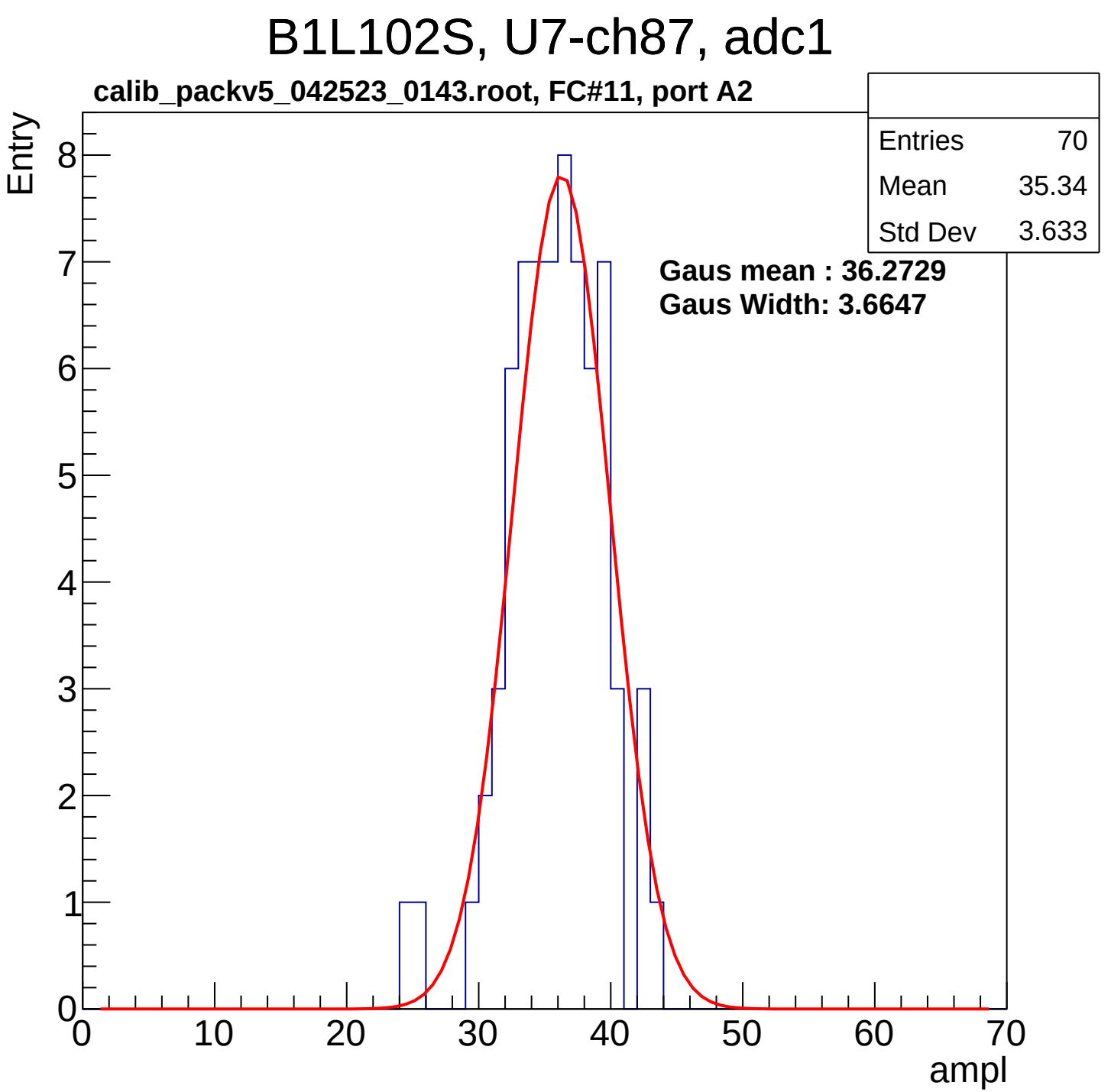
20
30
40
50
60
70


B1L102S, U7-ch87, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 70
Mean 35.34
Std Dev 3.633
Gaus mean : 36.2729
Gaus Width: 3.6647
Entry
ampl
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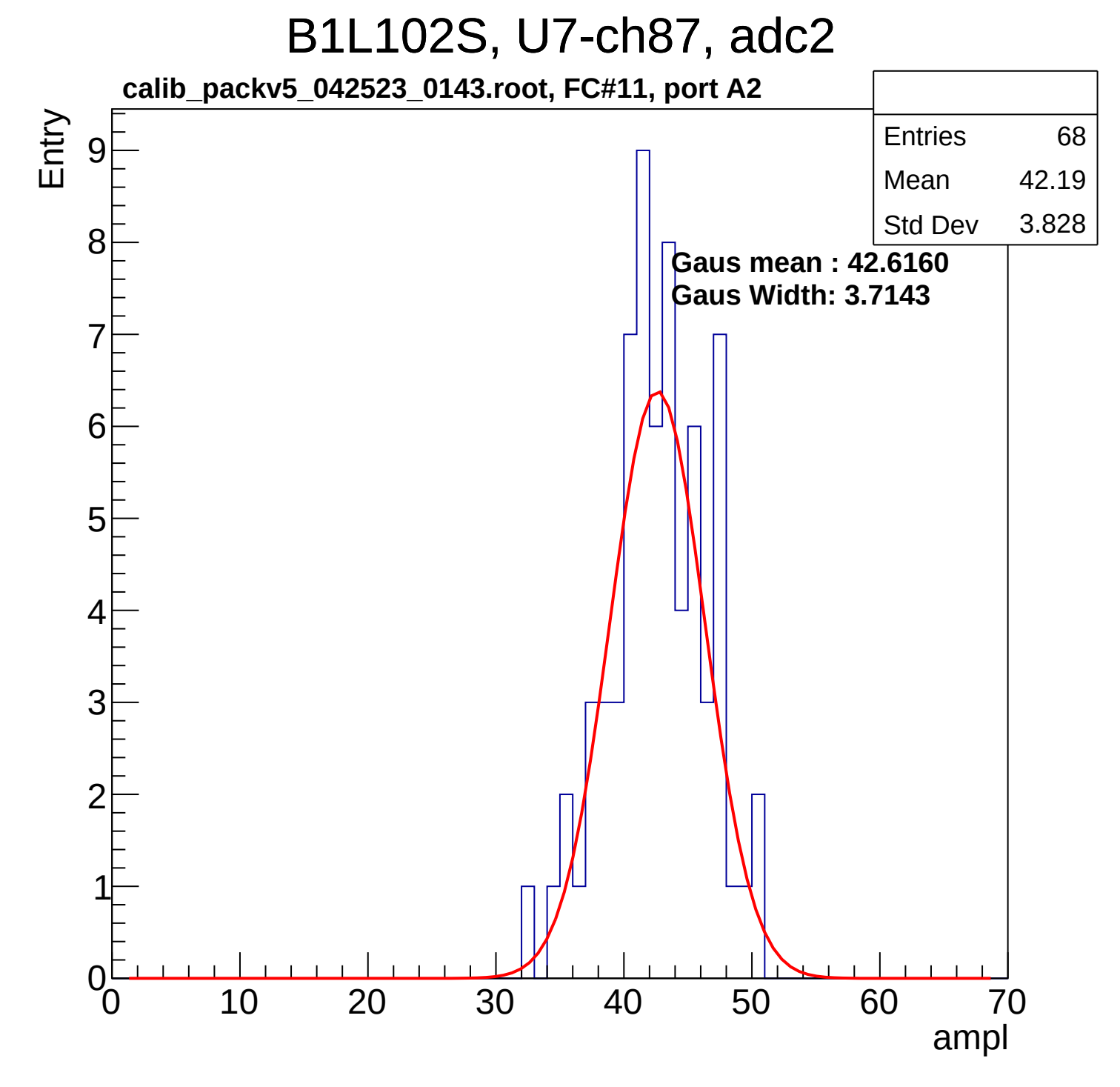
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L102S, U7-ch87, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 68
Mean 42.19
Std Dev 3.828
Gaus mean : 42.6160
Gaus Width: 3.7143
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
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40
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60
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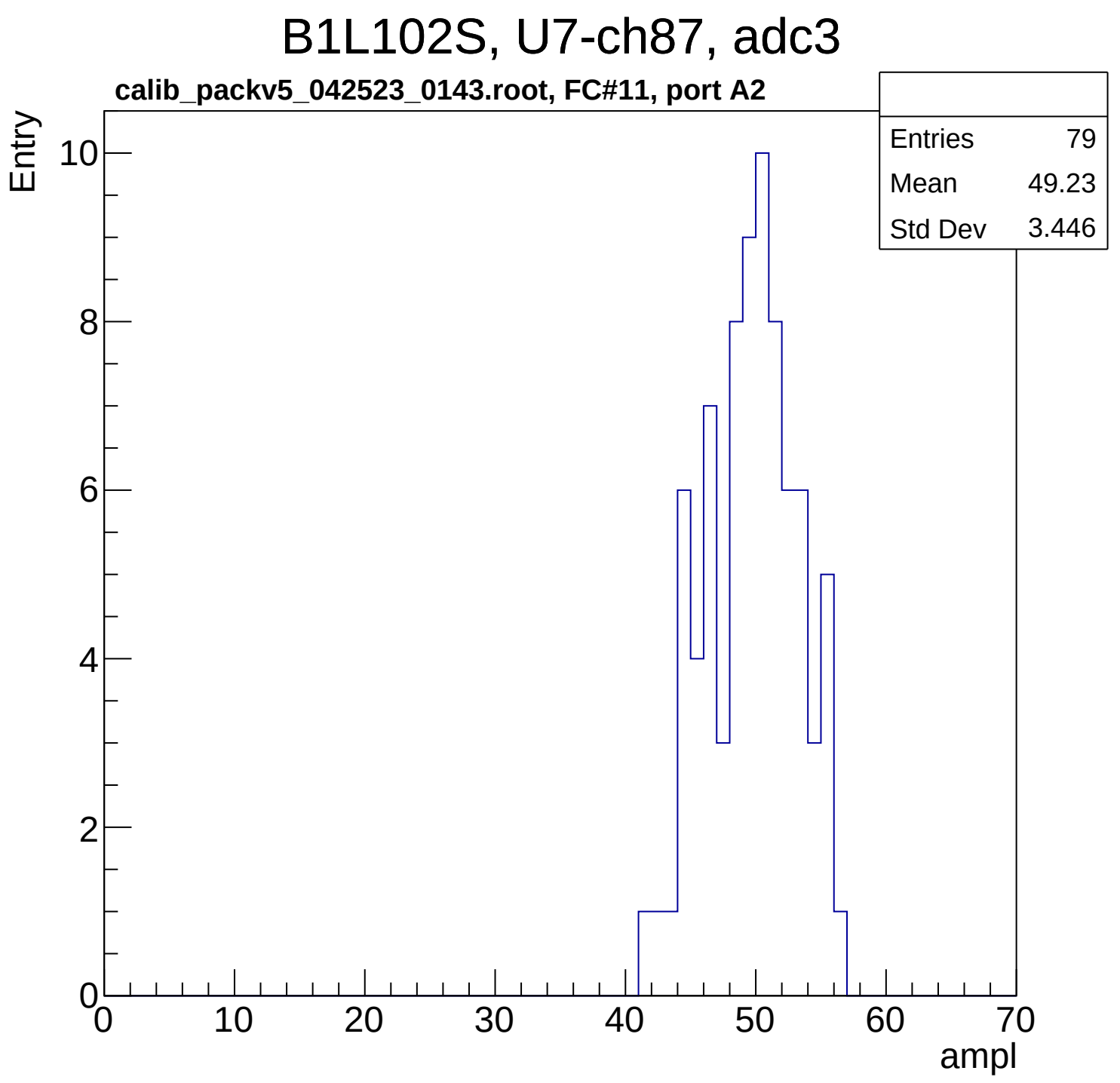
B1L102S, U7-ch87, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 79
Mean 49.23
Std Dev 3.446
Entry
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2
4
6
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10
0
10
20
30
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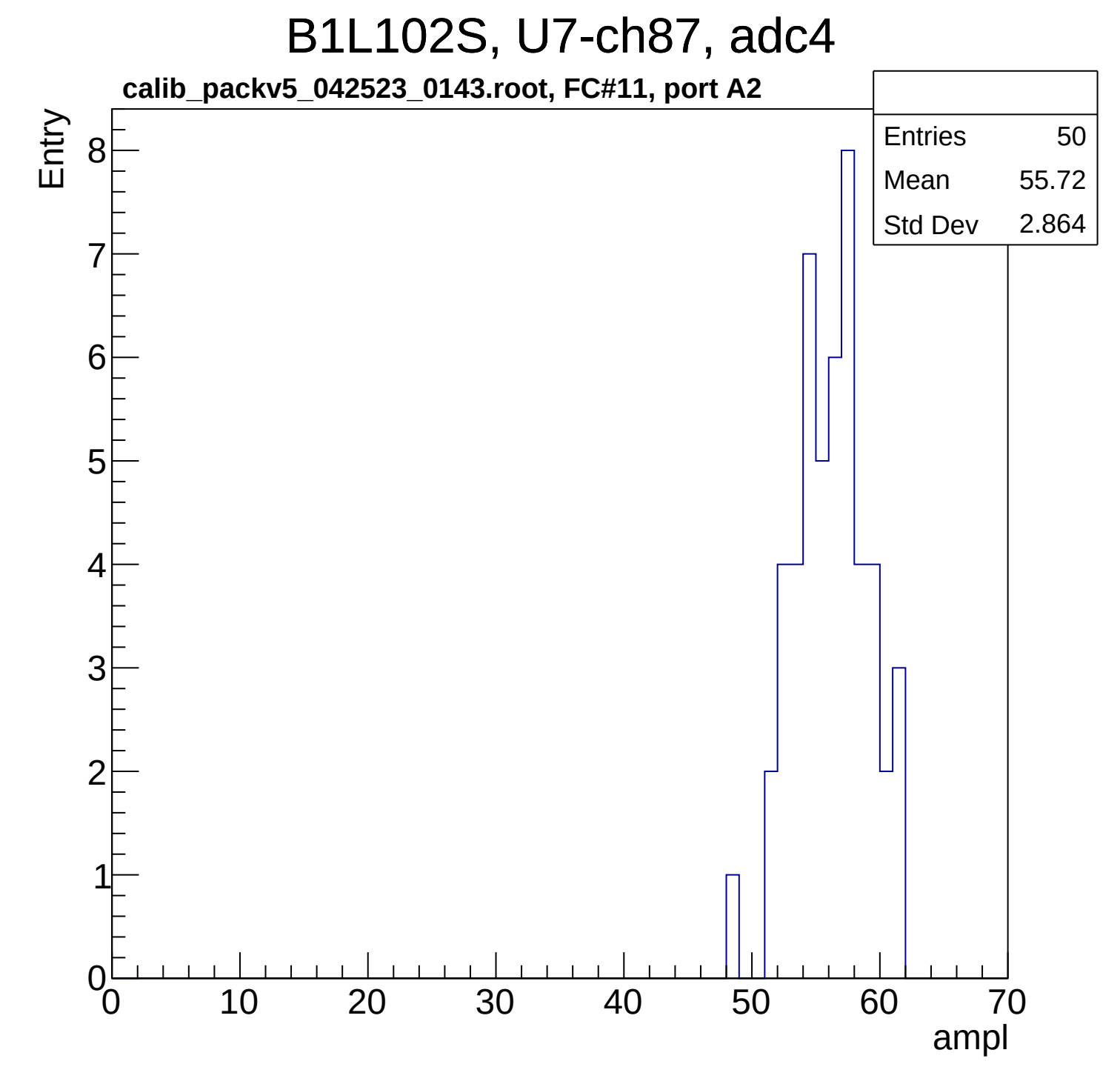
50
60
70
ampl


B1L102S, U7-ch87, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 50
Mean 55.72
Std Dev 2.864
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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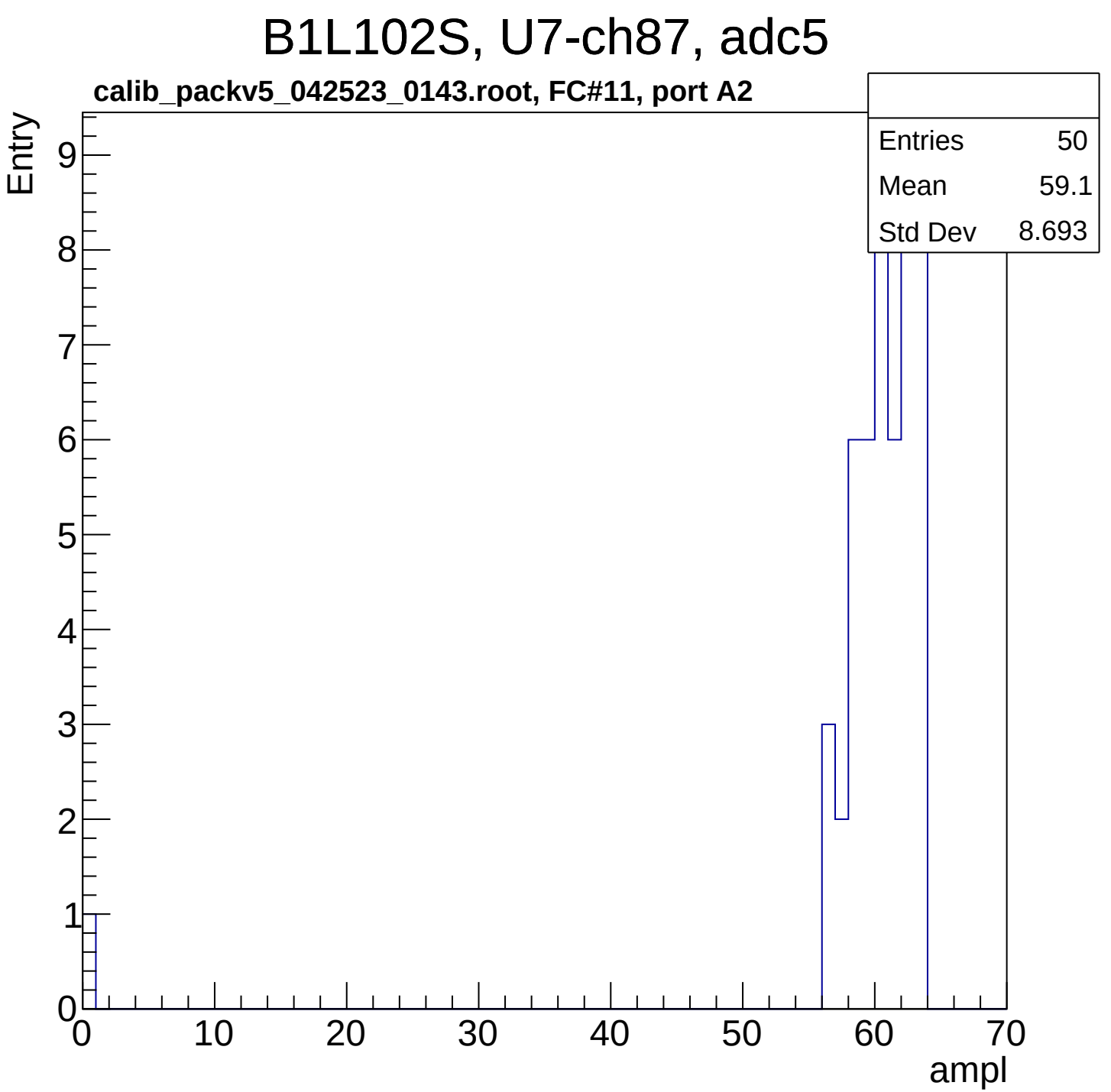
40
50
60
70


B1L102S, U7-ch87, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 50
Mean 59.1
Std Dev 8.693
Entry
ampl
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7
8
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0
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60
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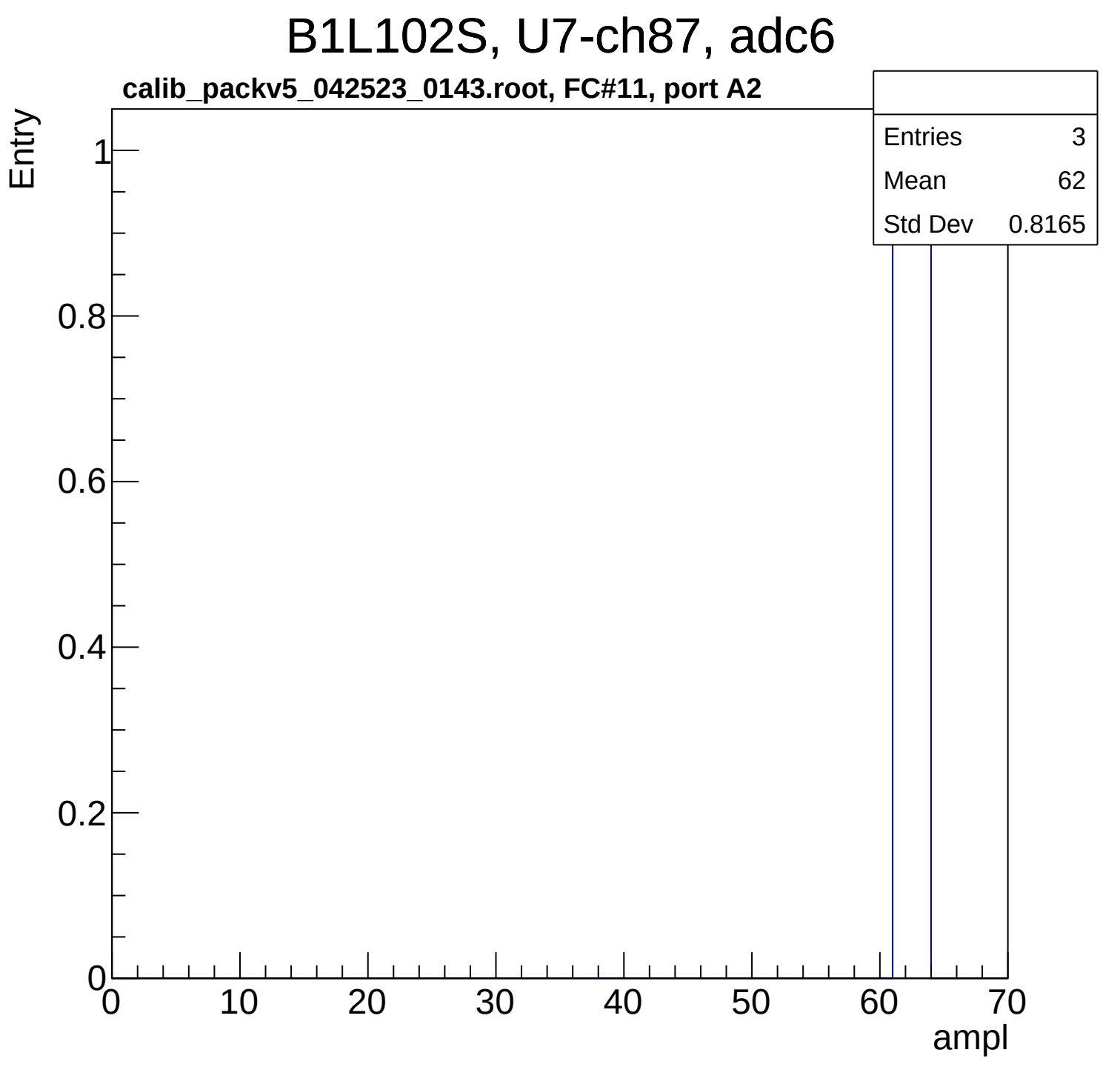
B1L102S, U7-ch87, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 3
Mean 62
Std Dev 0.8165
Entry
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0.6
0.4
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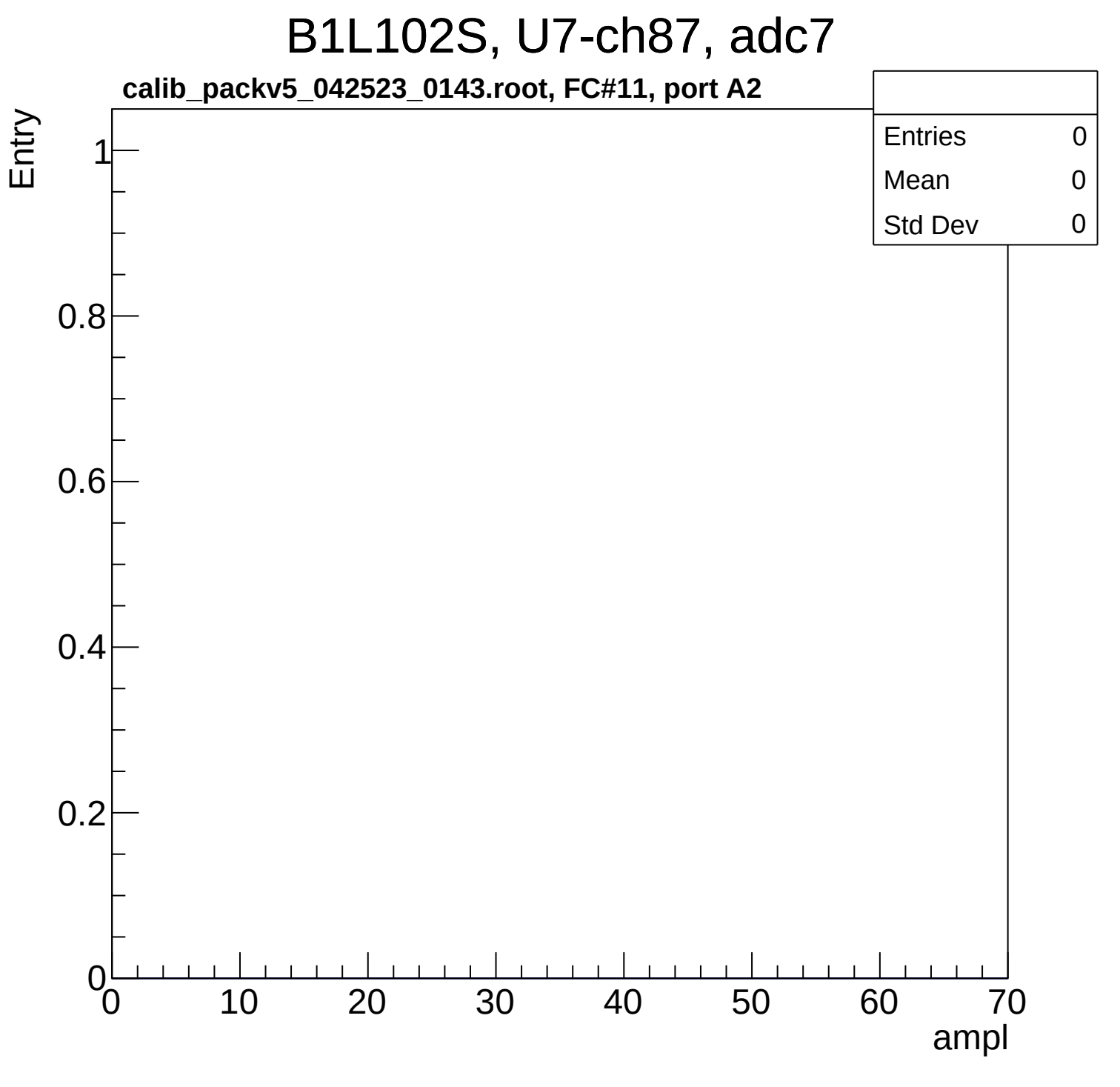
10
20
30
40
50
60
70
ampl


B1L102S, U7-ch87, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 0
Mean 0
Std Dev 0
Entry
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0.6
0.4
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10
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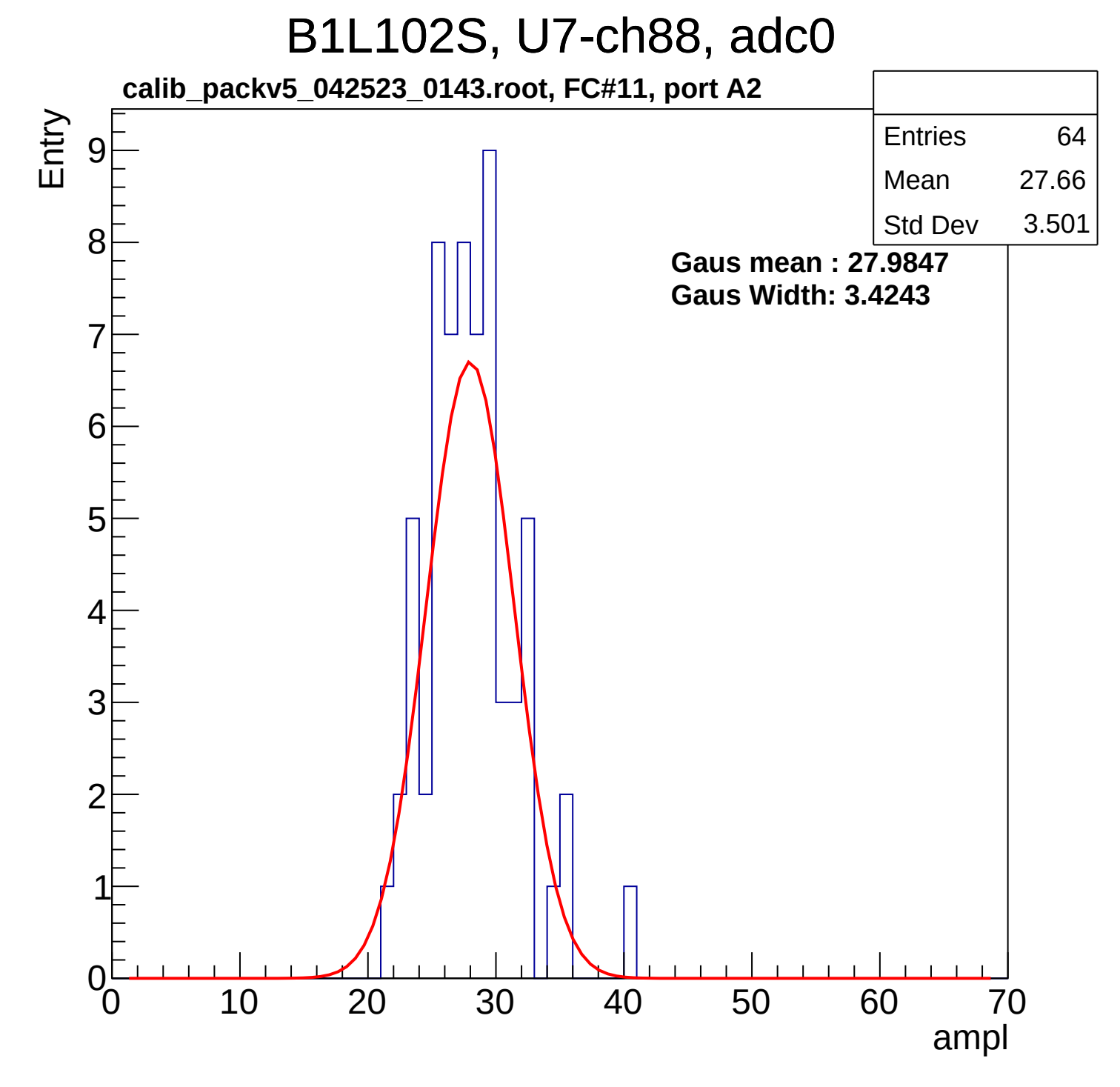
40
50
60
70
ampl


B1L102S, U7-ch88, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 64
Mean 27.66
Std Dev 3.501
Gaus mean : 27.9847
Gaus Width: 3.4243
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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40
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60
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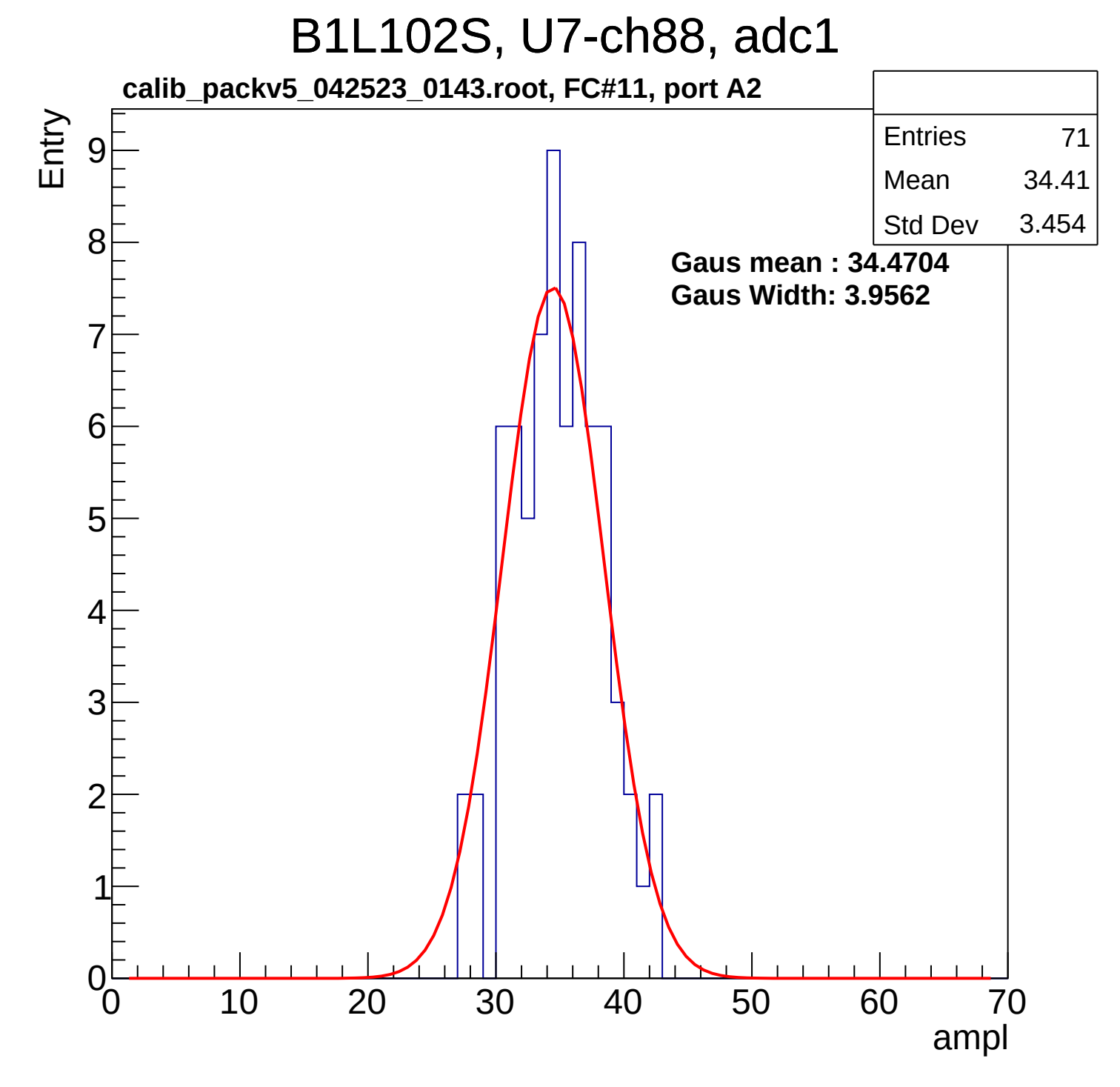
B1L102S, U7-ch88, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 71
Mean 34.41
Std Dev 3.454
Gaus mean : 34.4704
Gaus Width: 3.9562
Entry
ampl
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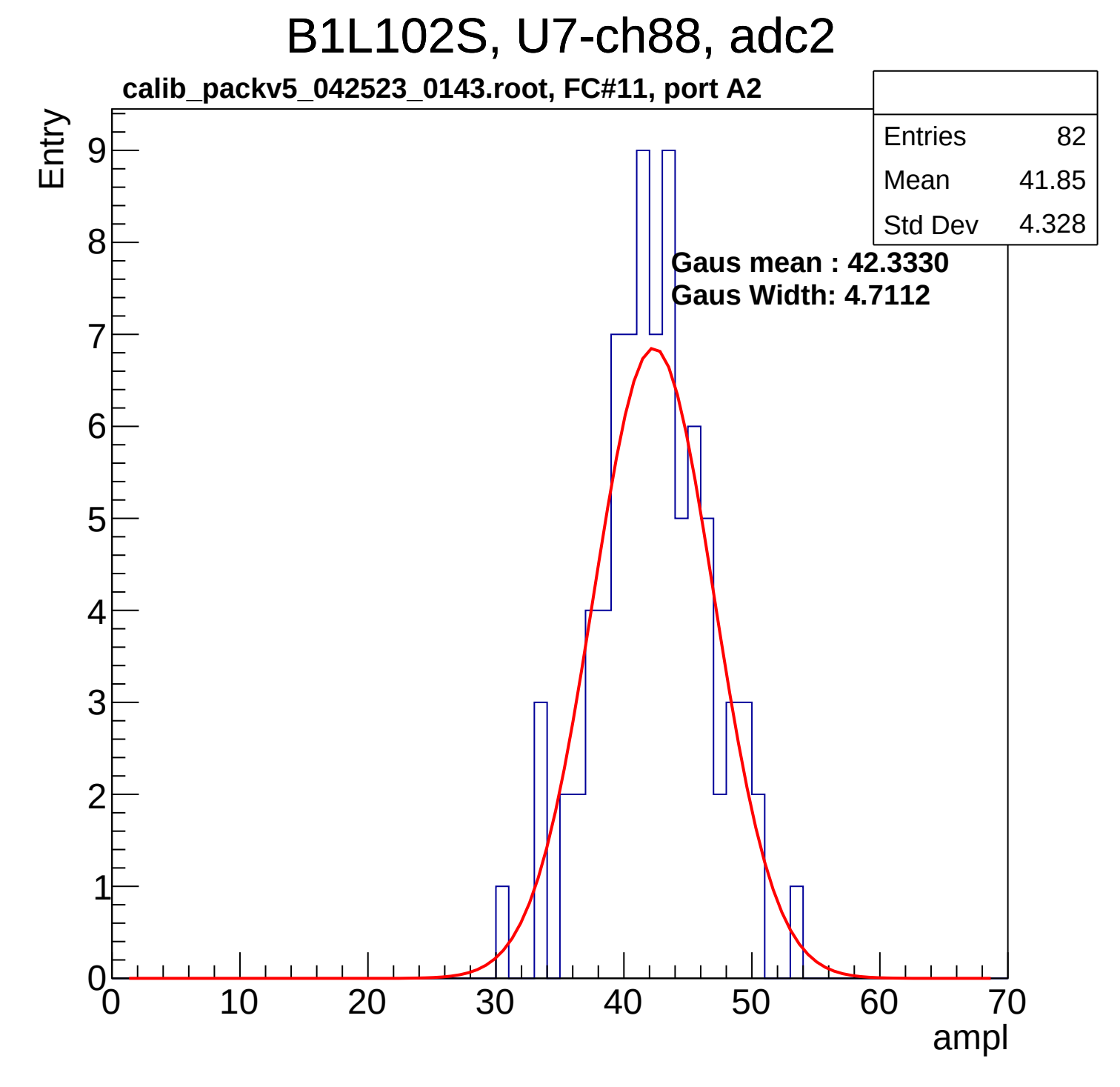
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9


B1L102S, U7-ch88, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 82
Mean 41.85
Std Dev 4.328
Gaus mean : 42.3330
Gaus Width: 4.7112
Entry
ampl
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2
3
4
5
6
7
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9
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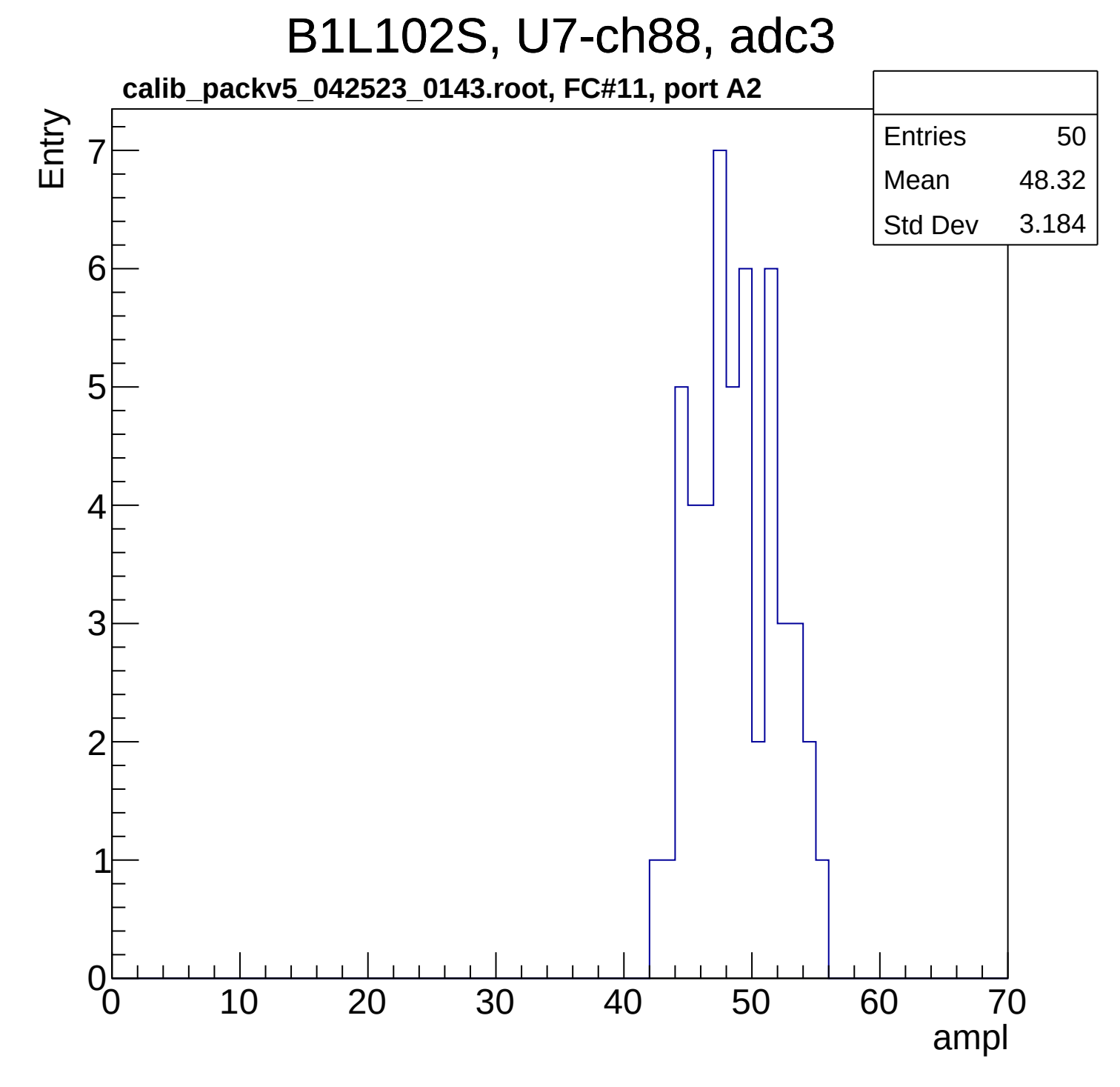
B1L102S, U7-ch88, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 50
Mean 48.32
Std Dev 3.184
Entry
ampl
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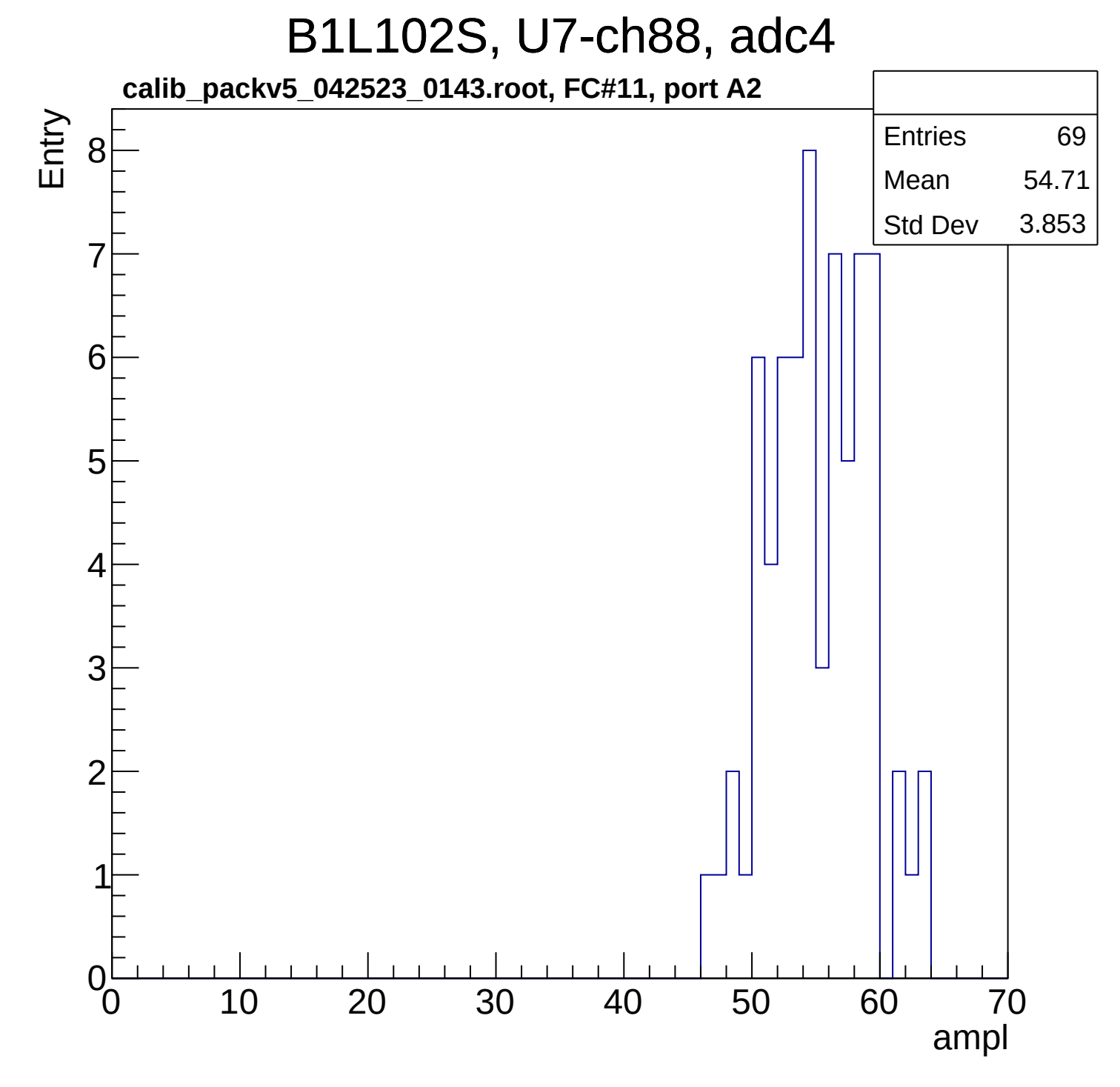
B1L102S, U7-ch88, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 69
Mean 54.71
Std Dev 3.853
Entry
ampl
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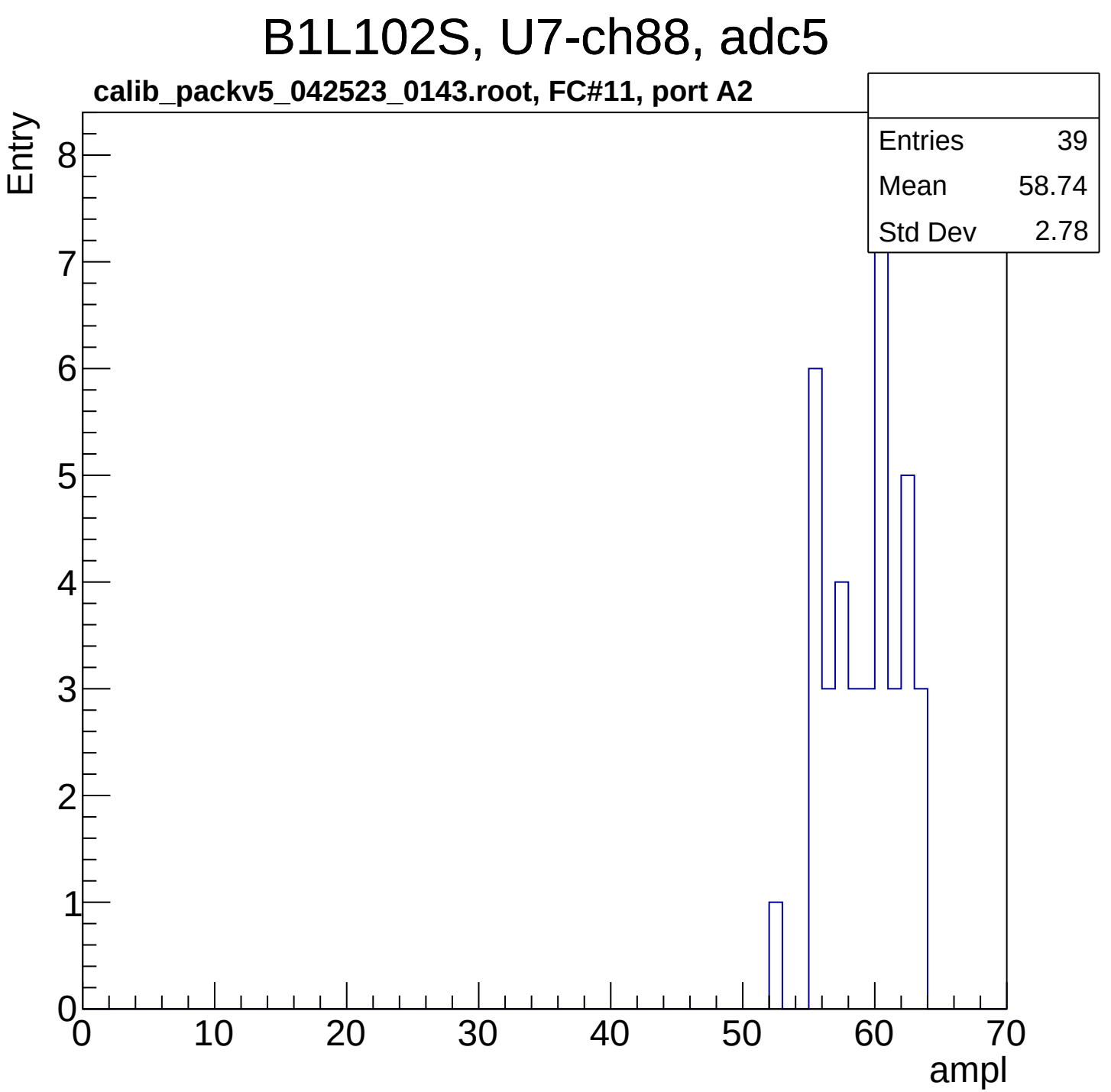
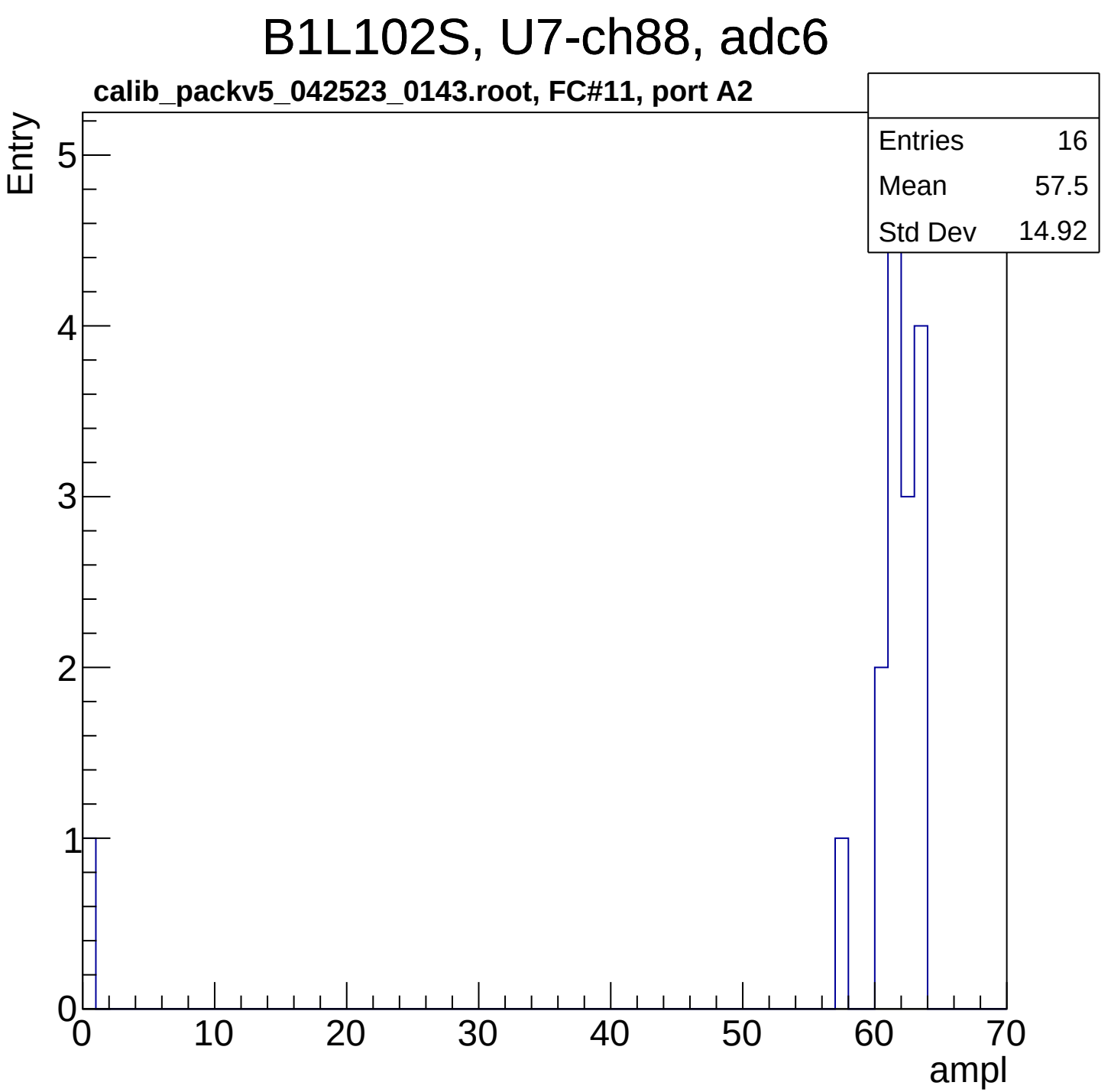

B1L102S, U7-ch88, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 39
Mean 58.74
Std Dev 2.78
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L102S, U7-ch88, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 16
Mean 57.5
Std Dev 14.92
Entry
0
1
2
3
4
5
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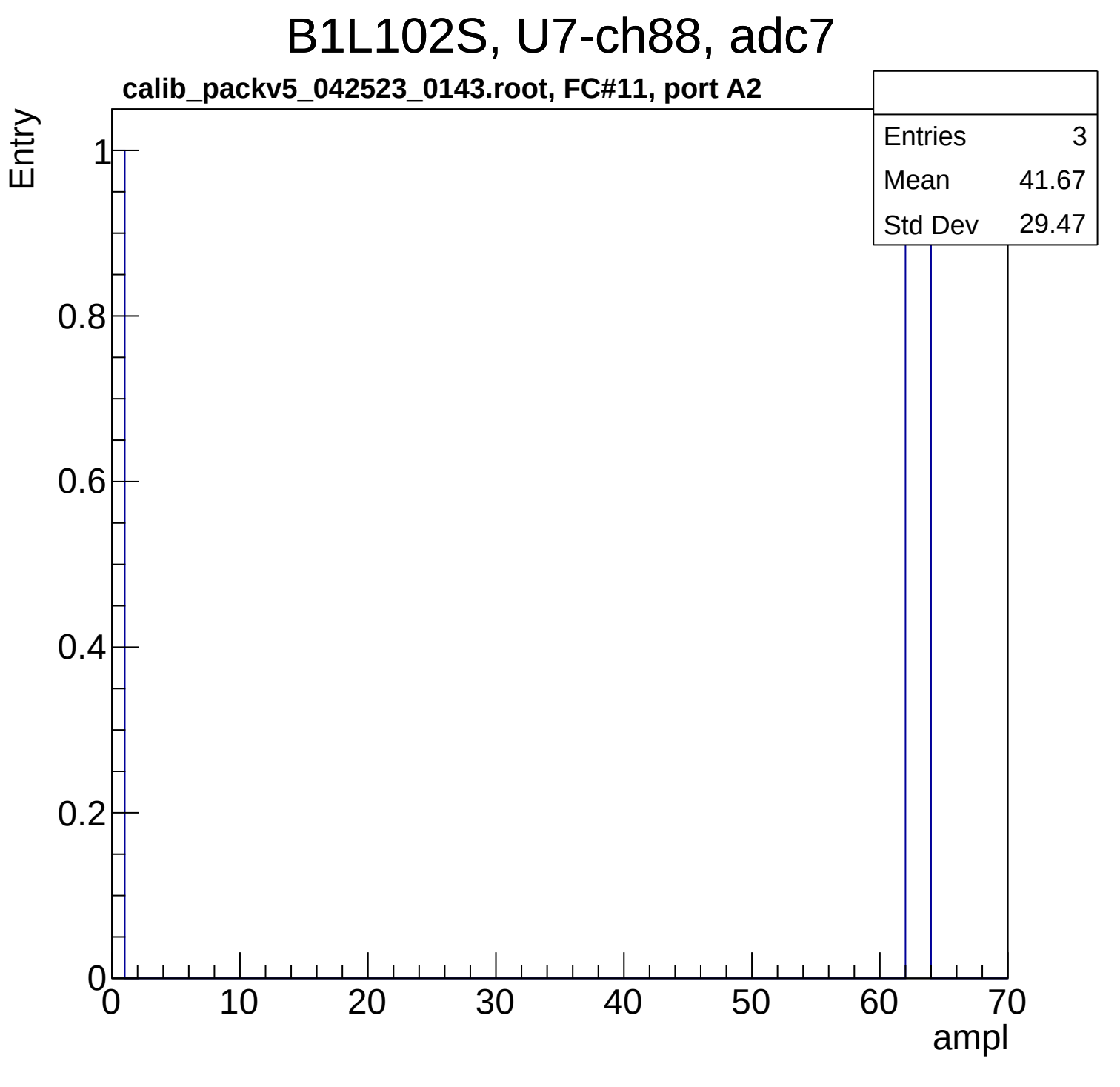
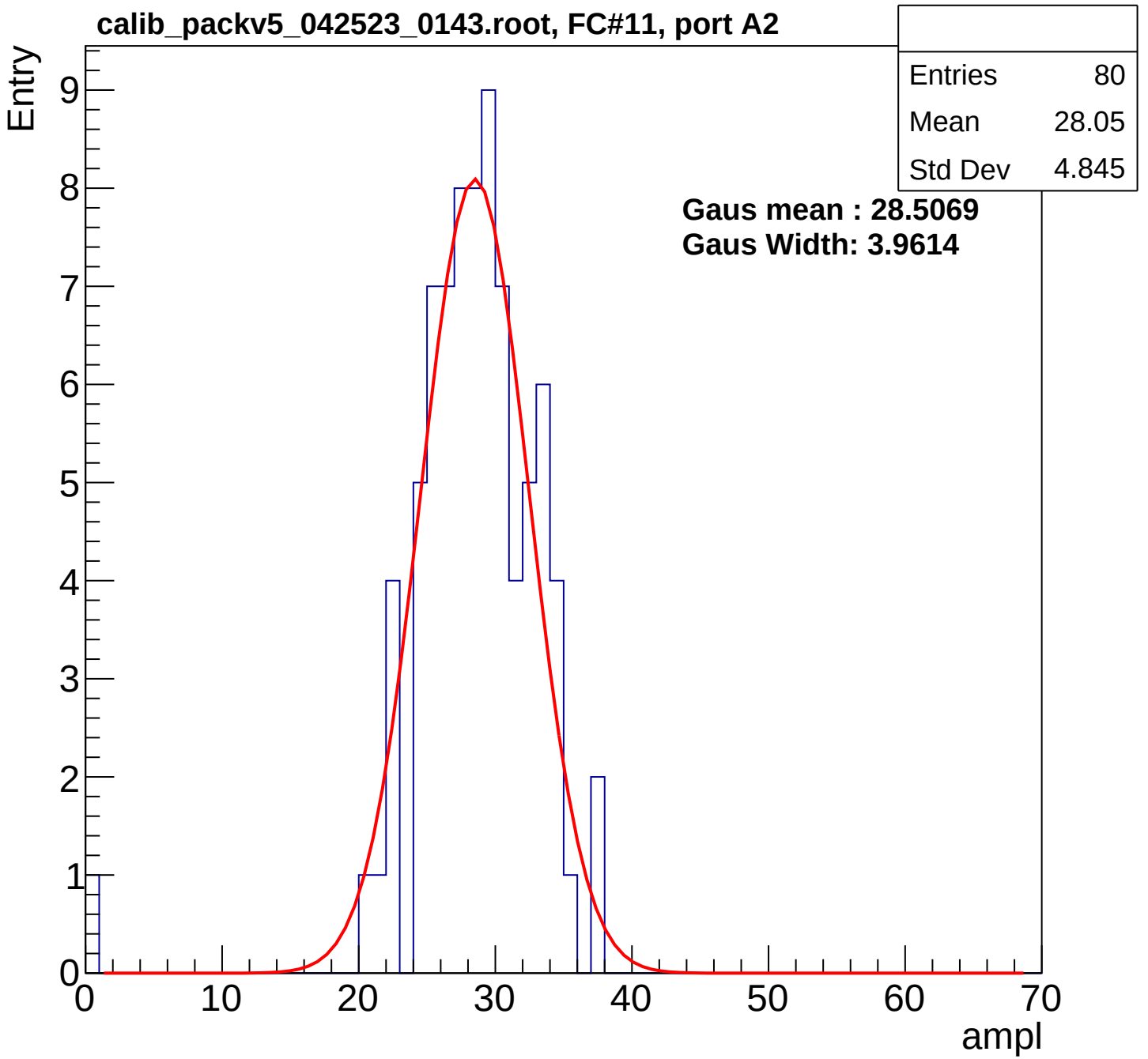
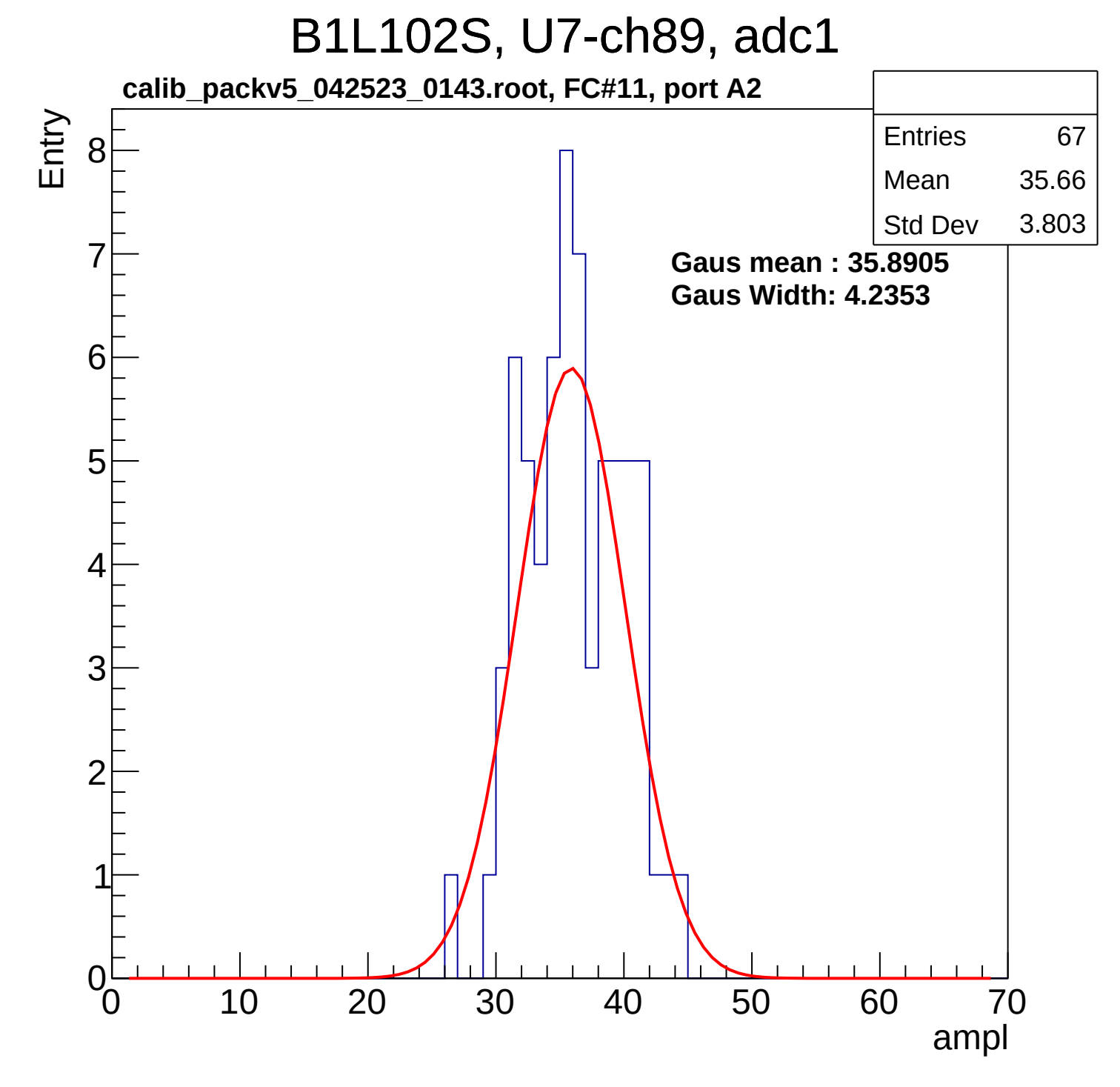
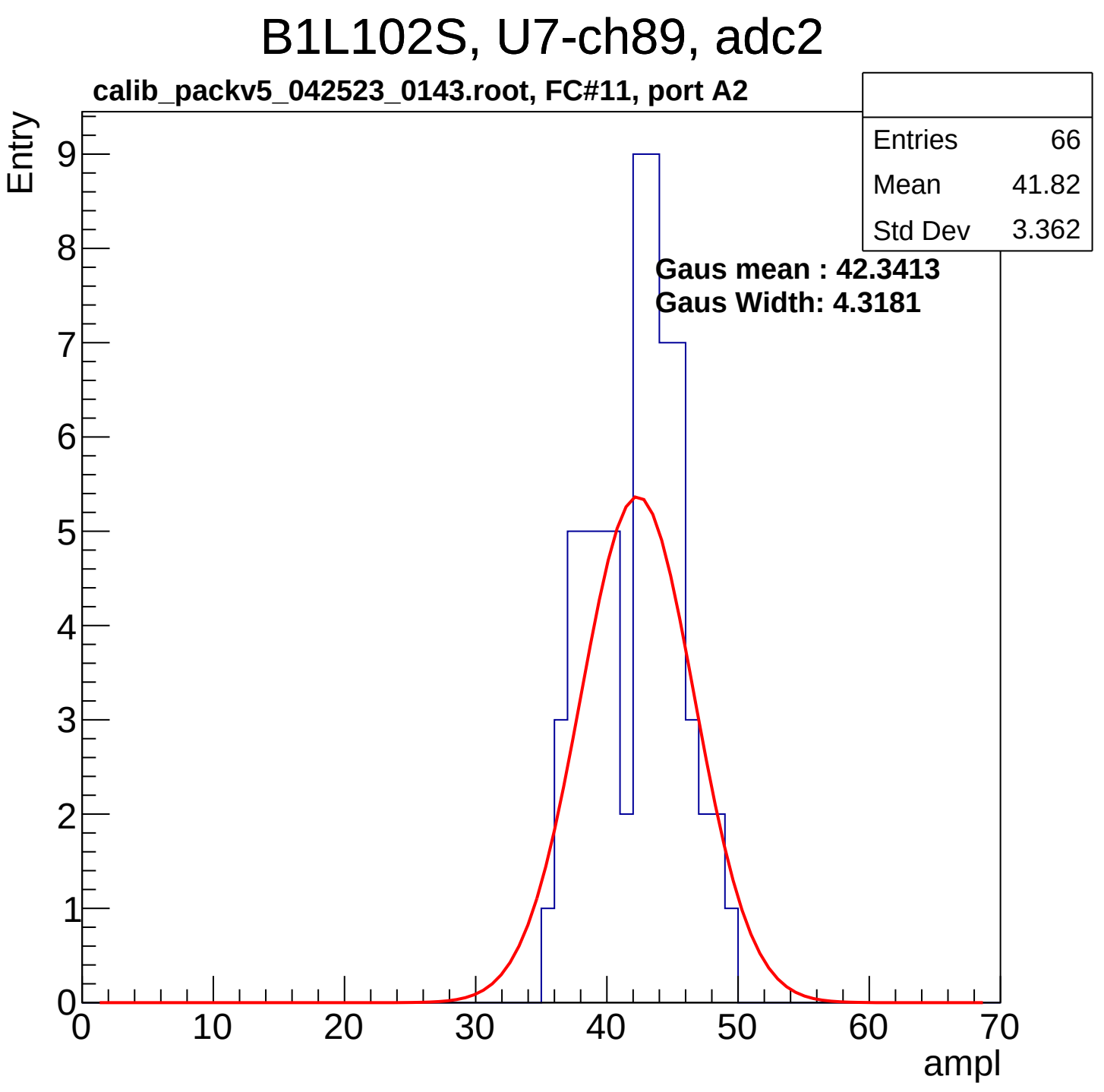
70
ampl


B1L102S, U7-ch88, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 3
Mean 41.67
Std Dev 29.47
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U7-ch89, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 80
Mean 28.05
Std Dev 4.845
Gaus mean : 28.5069
Gaus Width: 3.9614
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L102S, U7-ch89, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 67
Mean 35.66
Std Dev 3.803
Gaus mean : 35.8905
Gaus Width: 4.2353
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L102S, U7-ch89, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 66
Mean 41.82
Std Dev 3.362
Gaus mean : 42.3413
Gaus Width: 4.3181
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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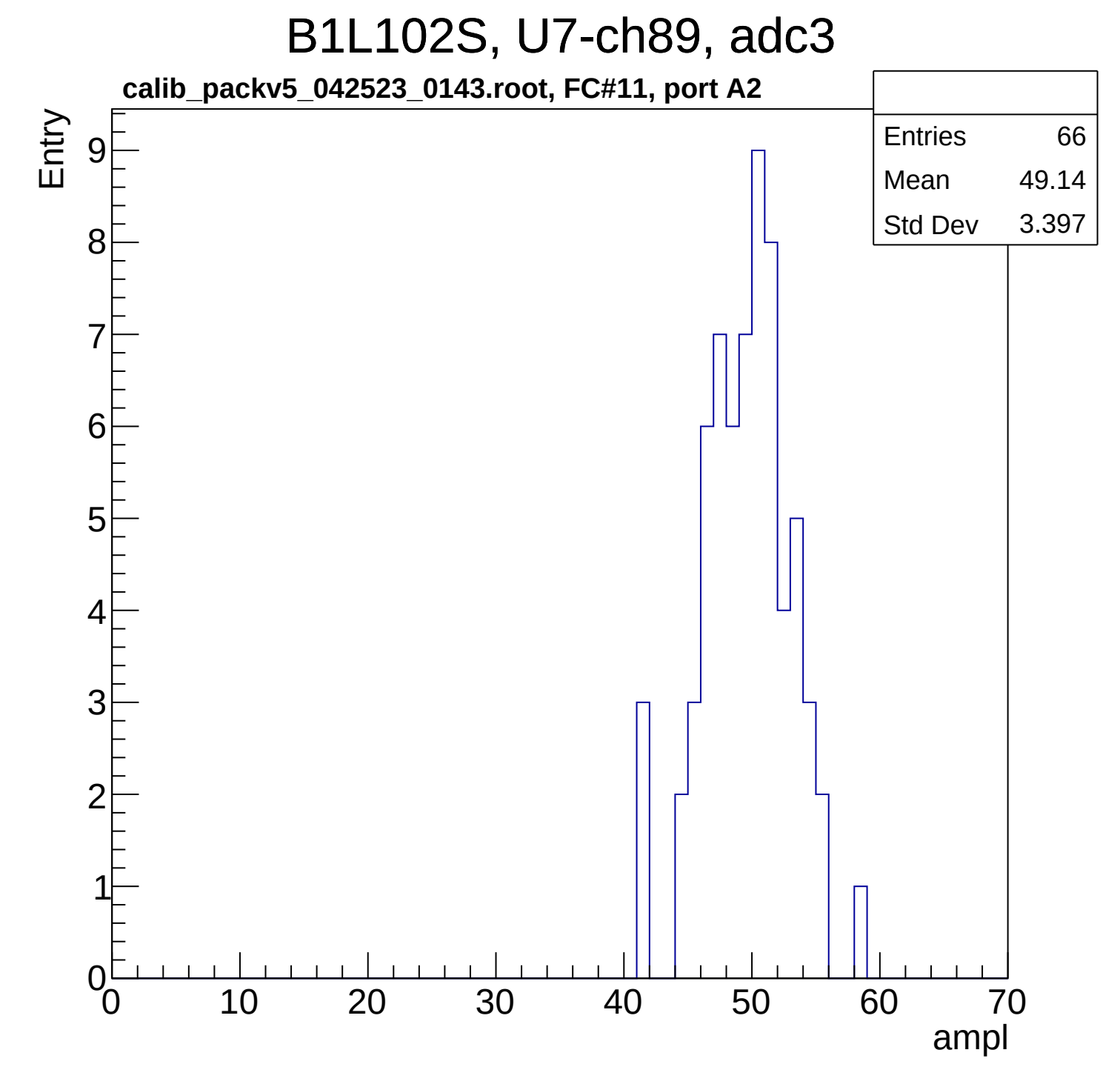
B1L102S, U7-ch89, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 66
Mean 49.14
Std Dev 3.397
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
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40
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60
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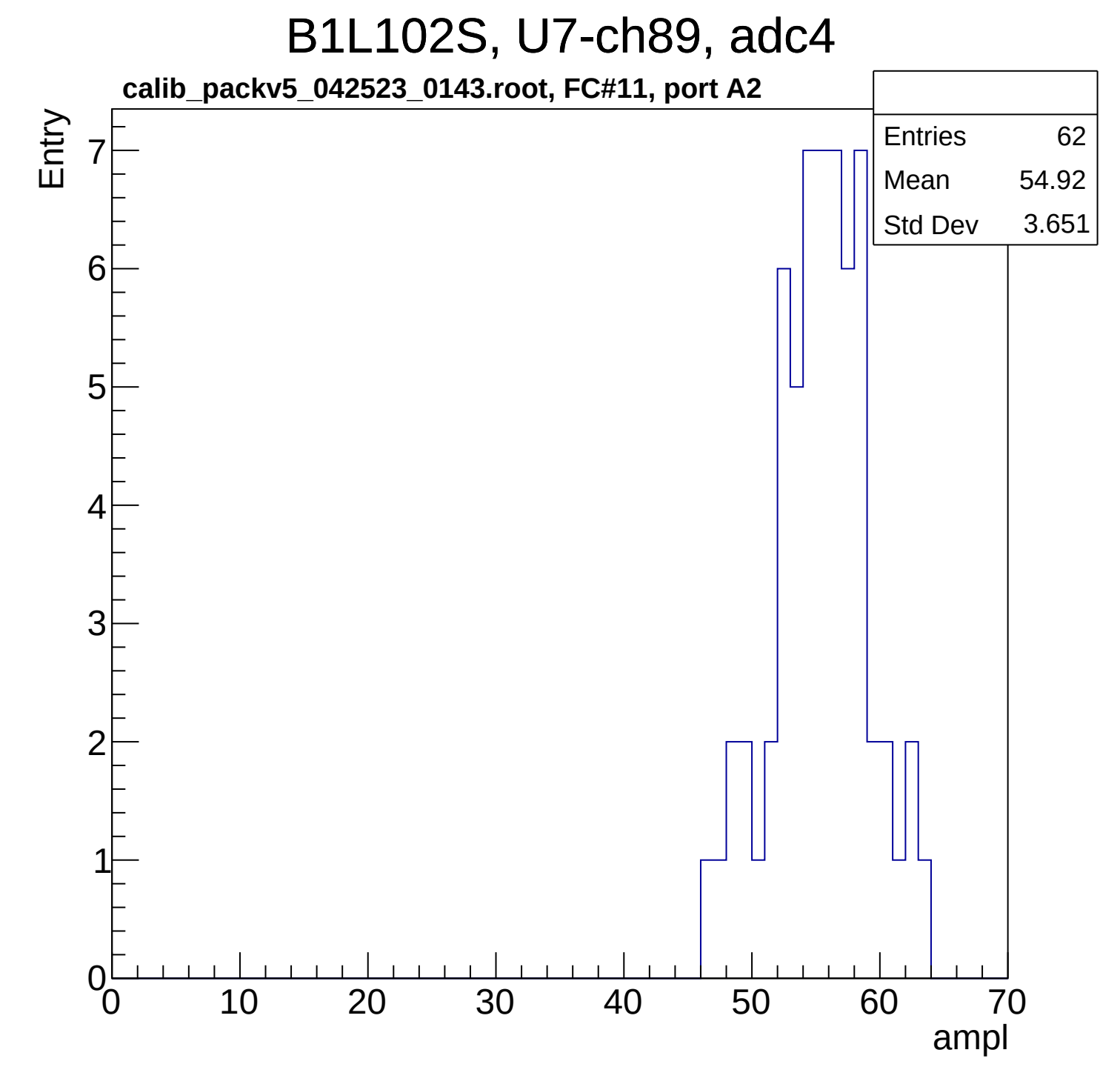
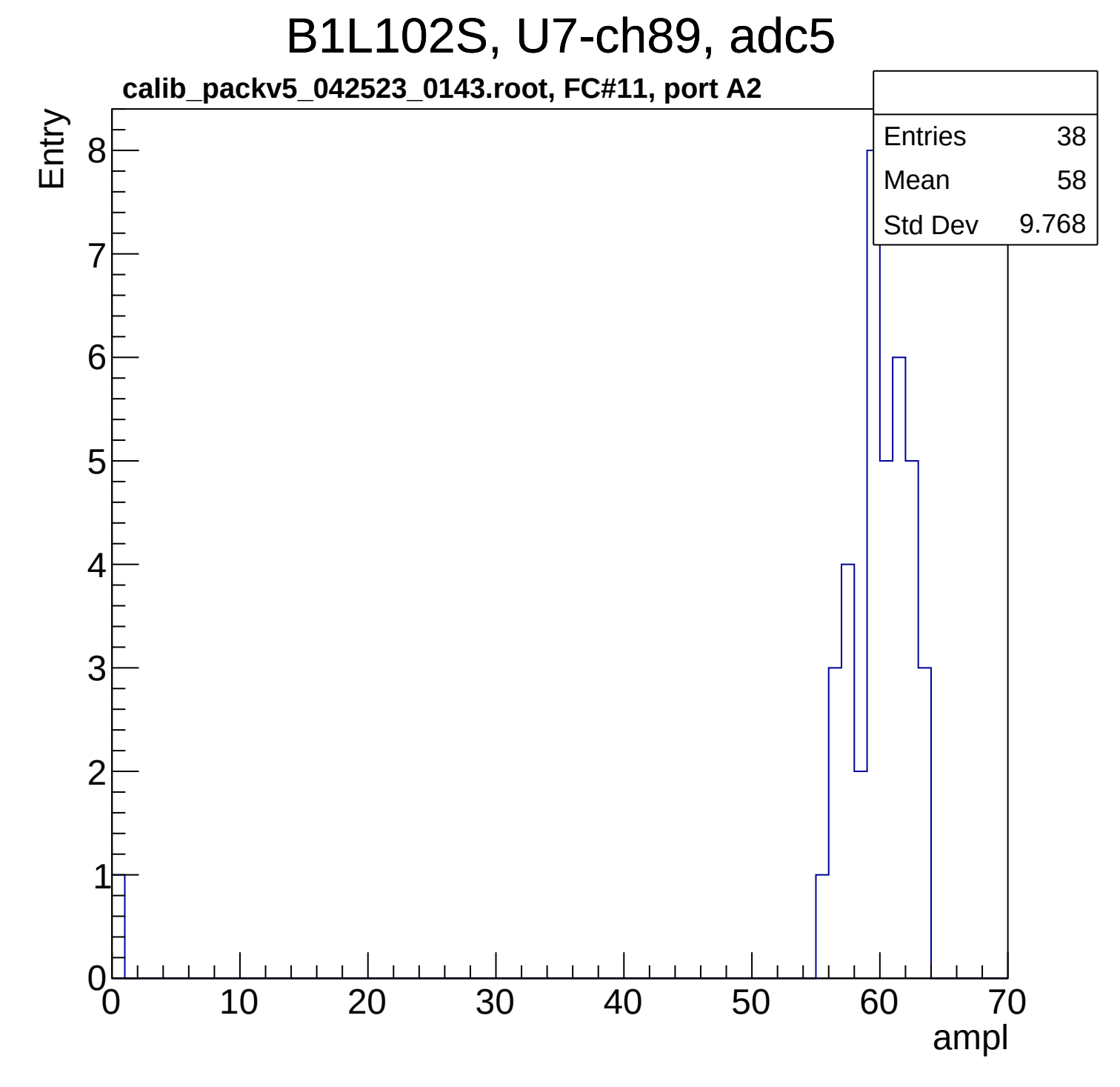

B1L102S, U7-ch89, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 62
Mean 54.92
Std Dev 3.651
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L102S, U7-ch89, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 38
Mean 58
Std Dev 9.768
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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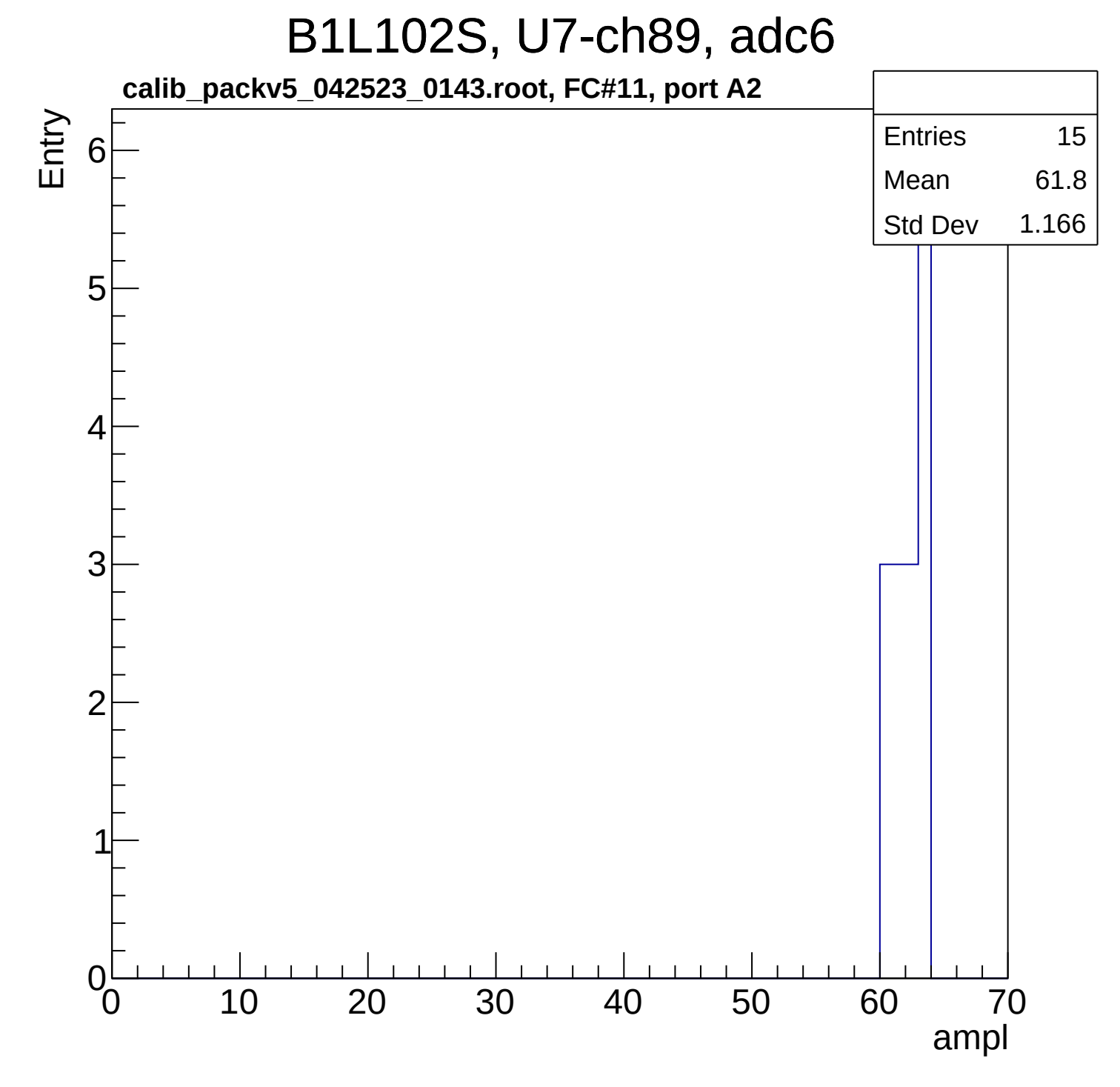
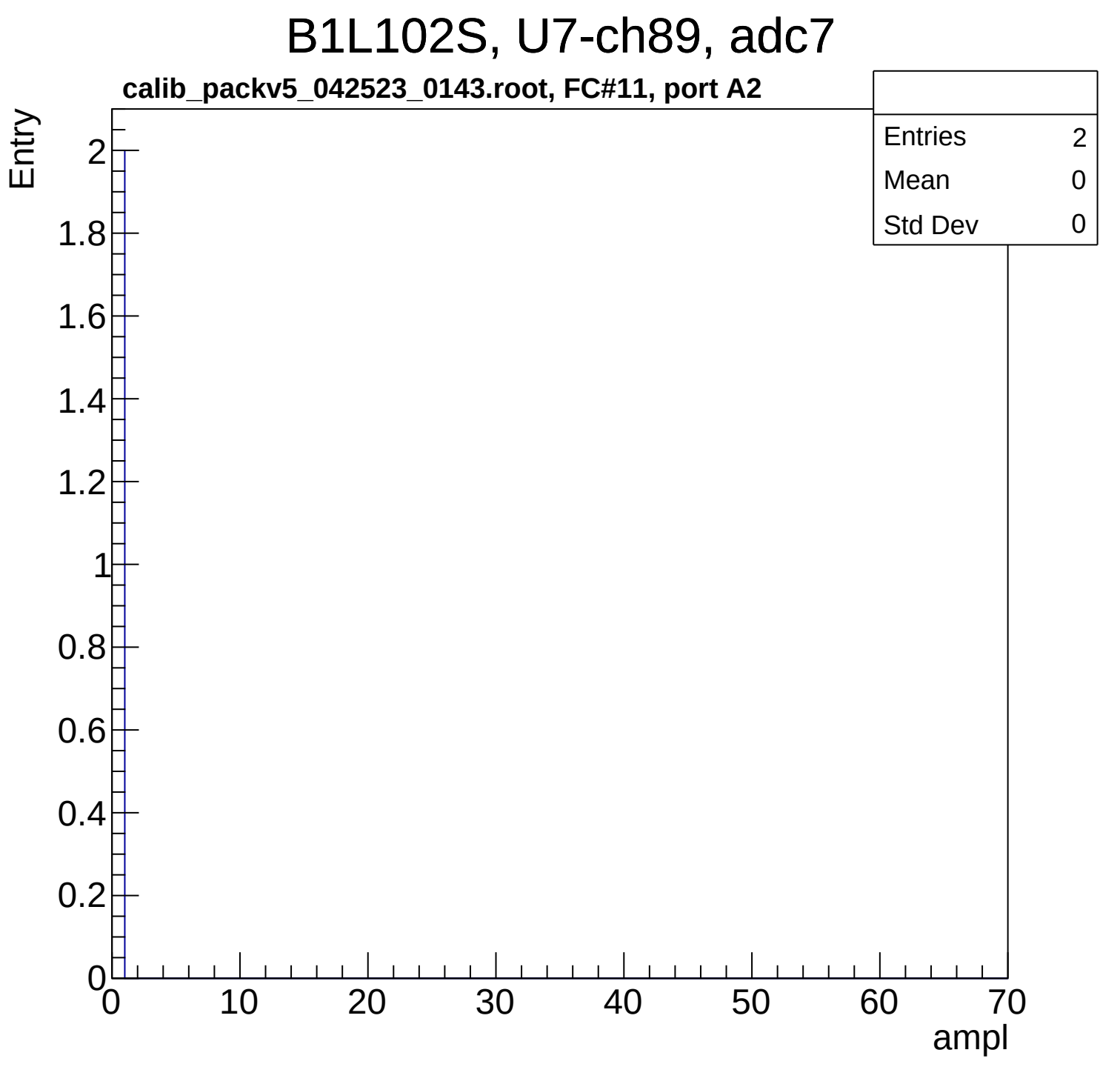
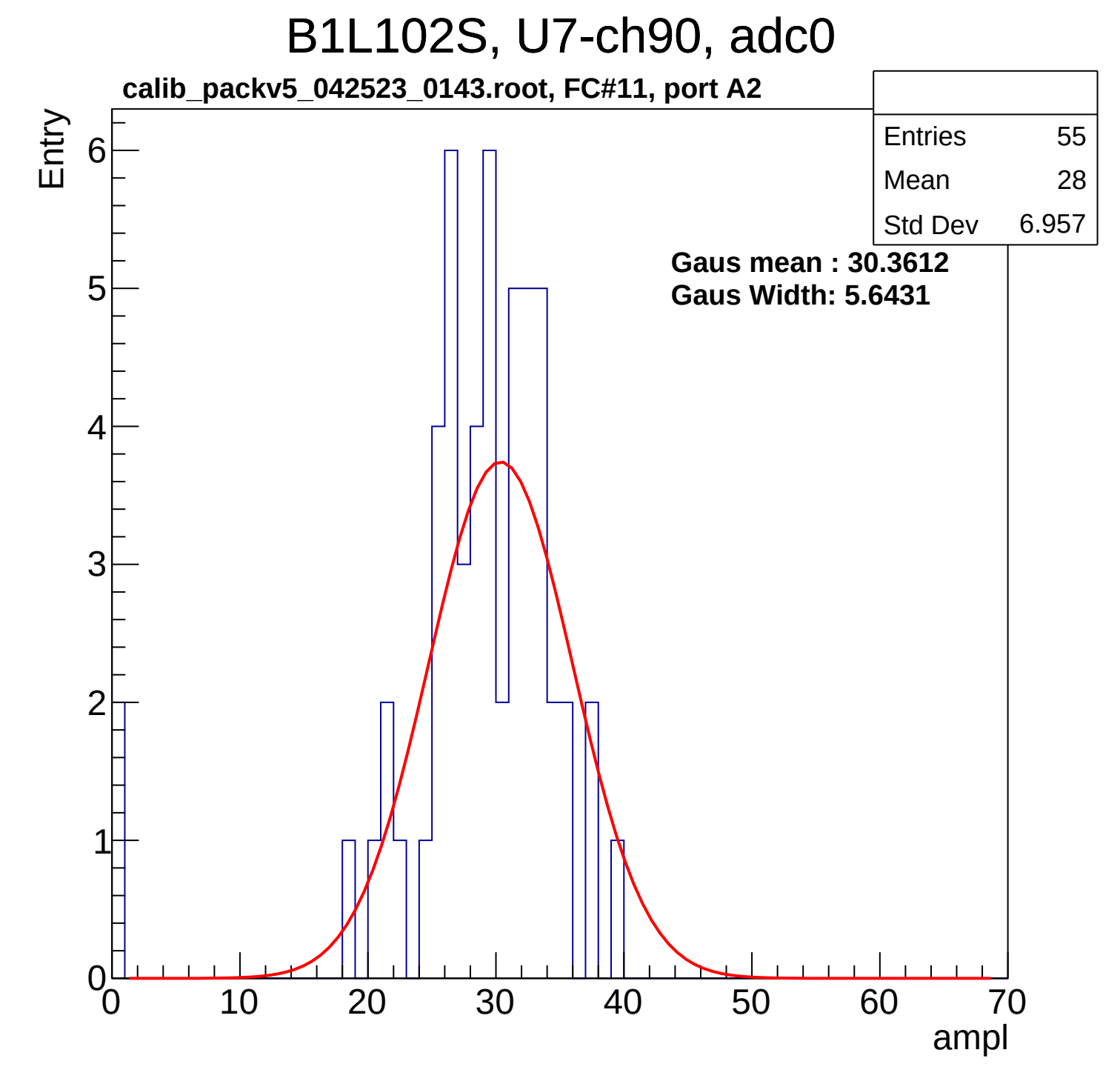
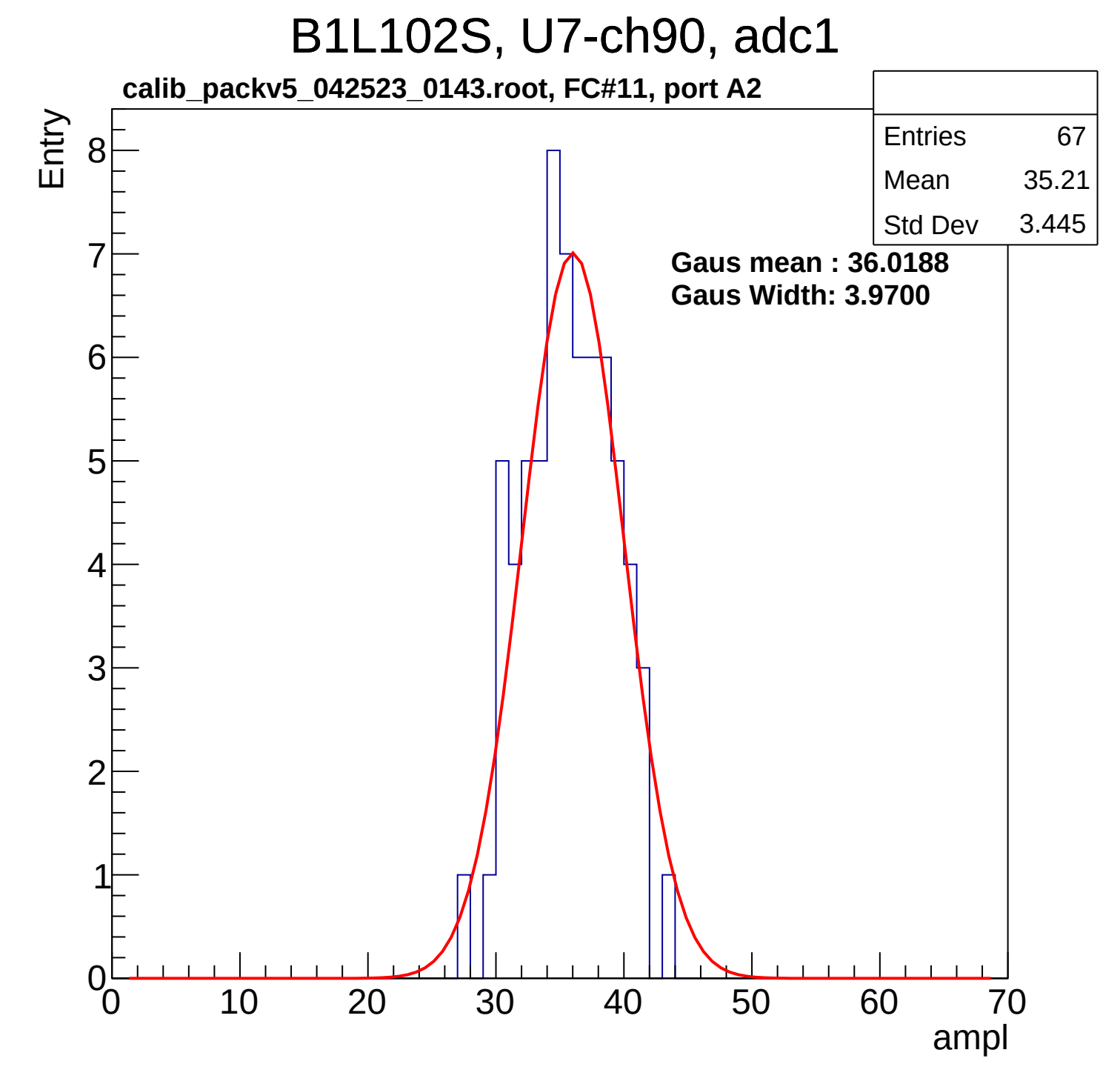

B1L102S, U7-ch89, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 15
Mean 61.8
Std Dev 1.166
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L102S, U7-ch89, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 2
Mean 0
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L102S, U7-ch90, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 55
Mean 28
Std Dev 6.957
Gaus mean : 30.3612
Gaus Width: 5.6431
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L102S, U7-ch90, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 67
Mean 35.21
Std Dev 3.445
Gaus mean : 36.0188
Gaus Width: 3.9700
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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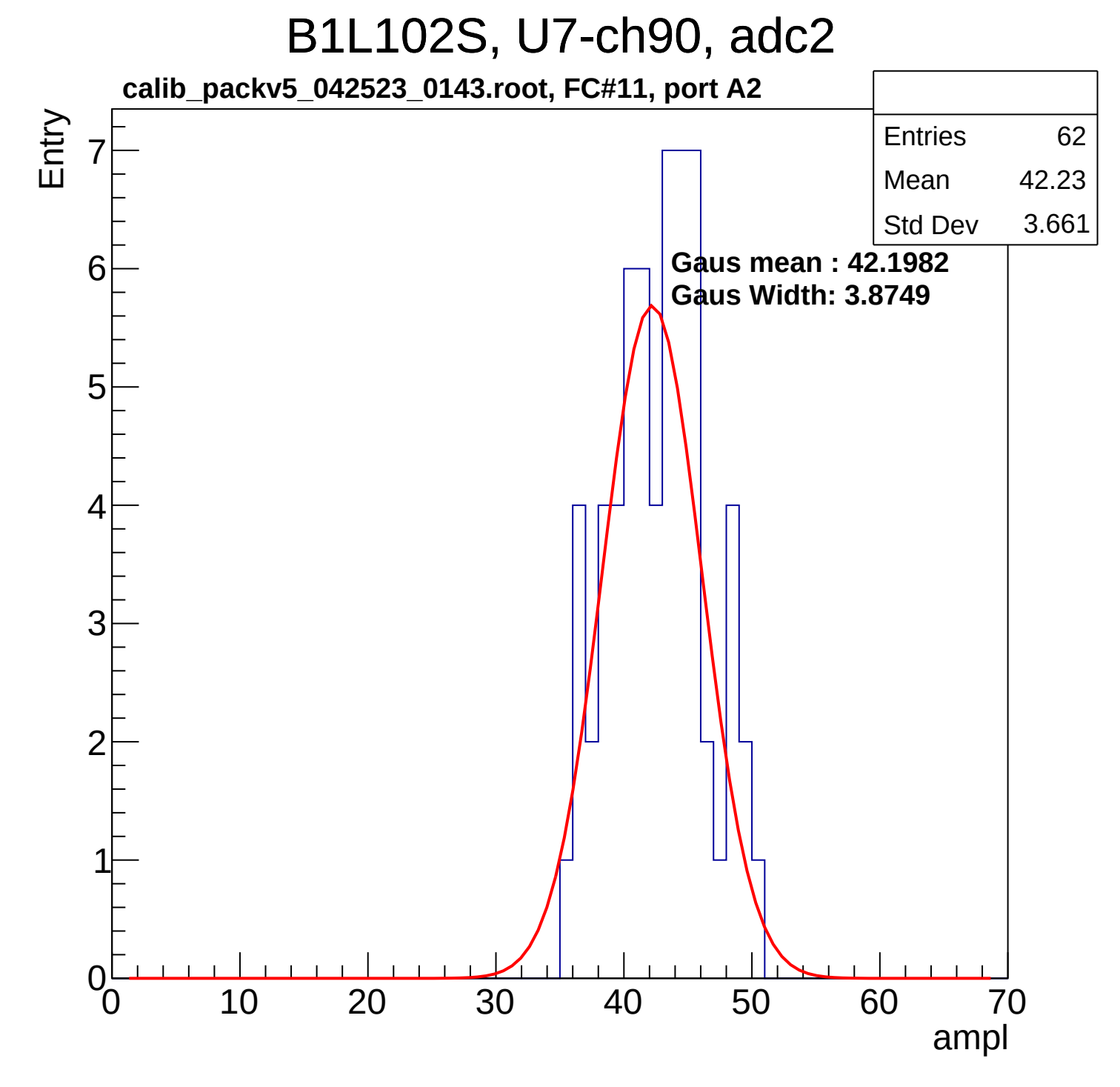
B1L102S, U7-ch90, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 62
Mean 42.23
Std Dev 3.661
Gaus mean : 42.1982
Gaus Width: 3.8749
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
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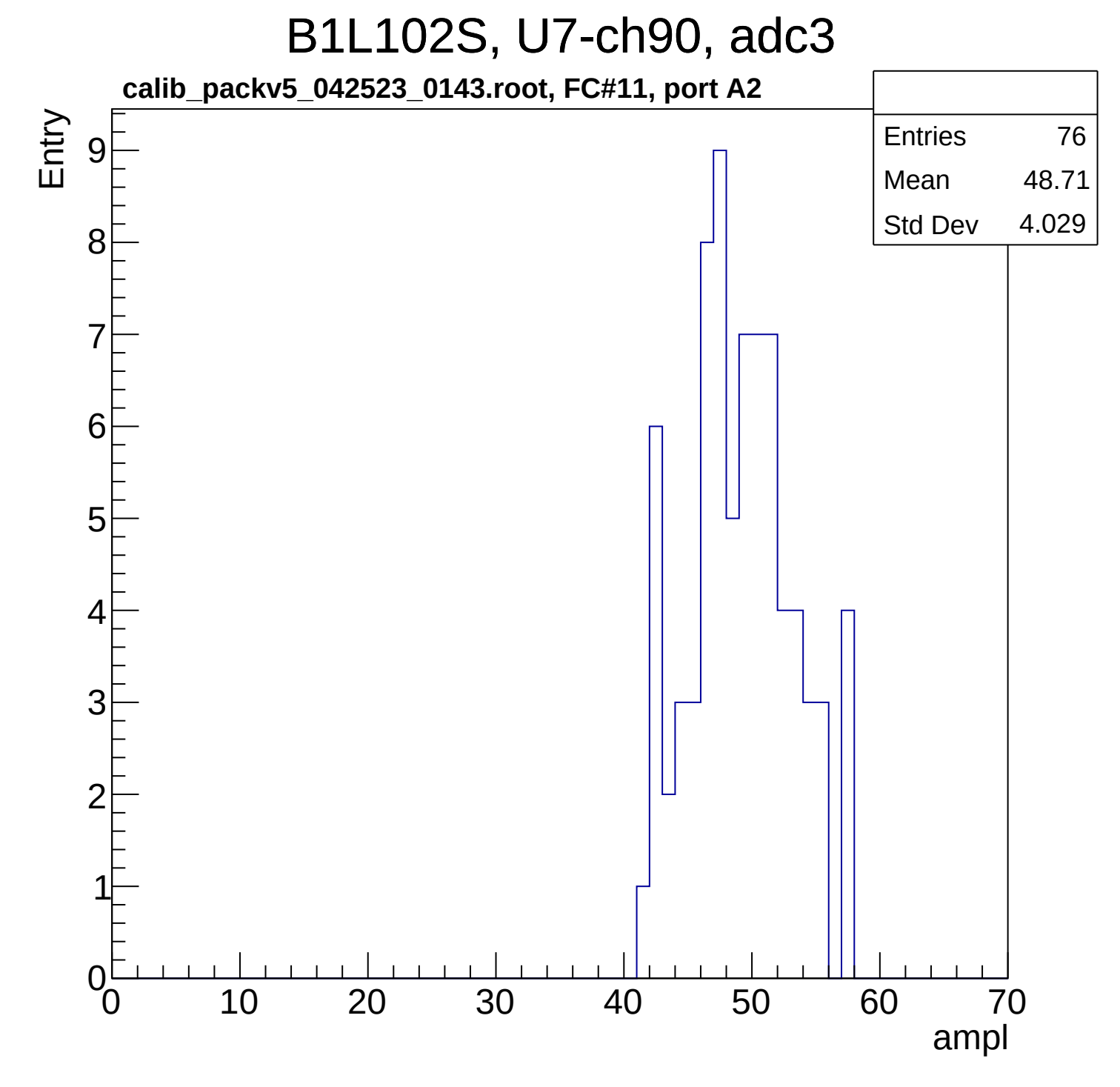
40
50
60
70


B1L102S, U7-ch90, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 76
Mean 48.71
Std Dev 4.029
Entry
ampl
0
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2
3
4
5
6
7
8
9
0
10
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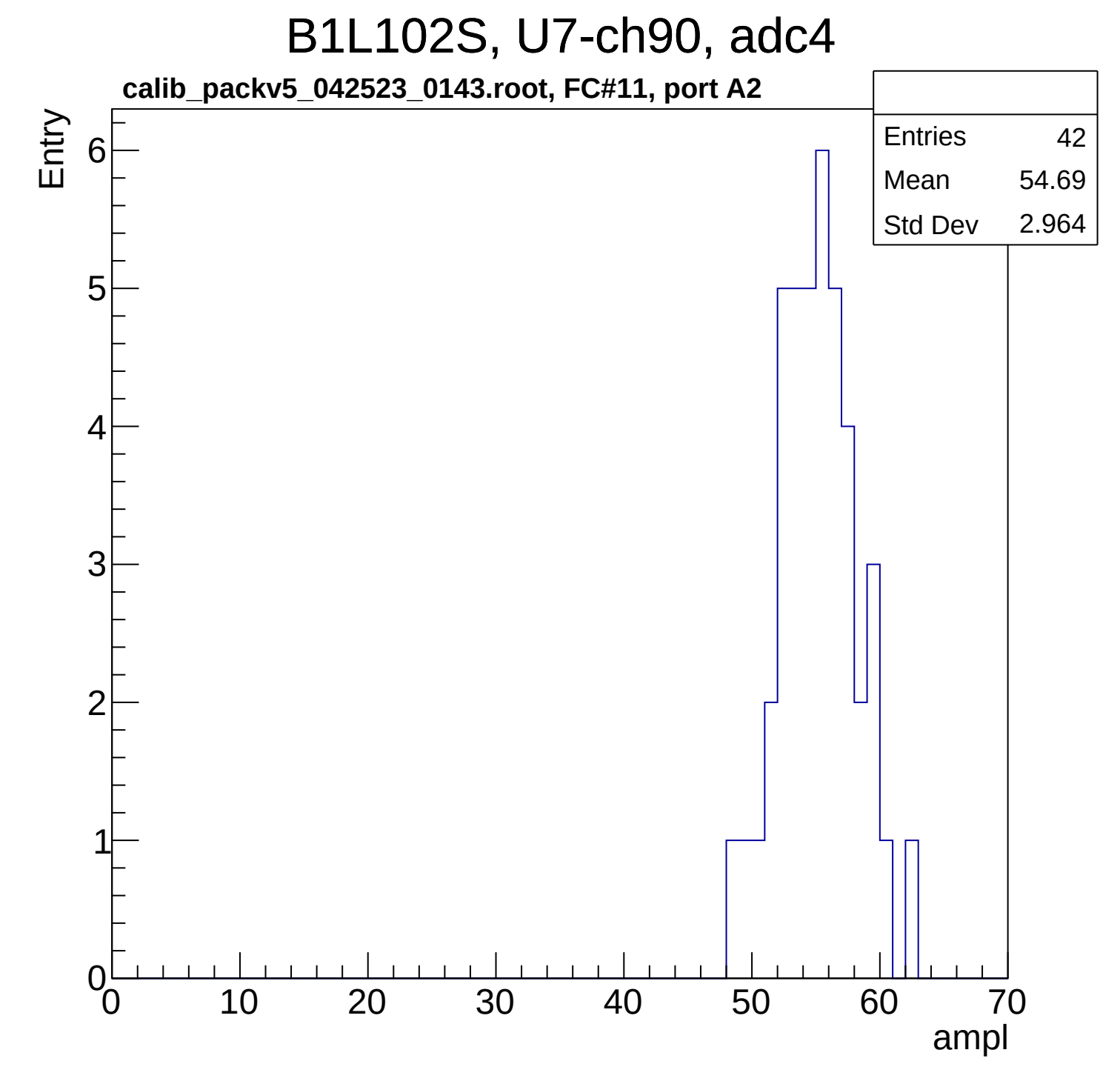
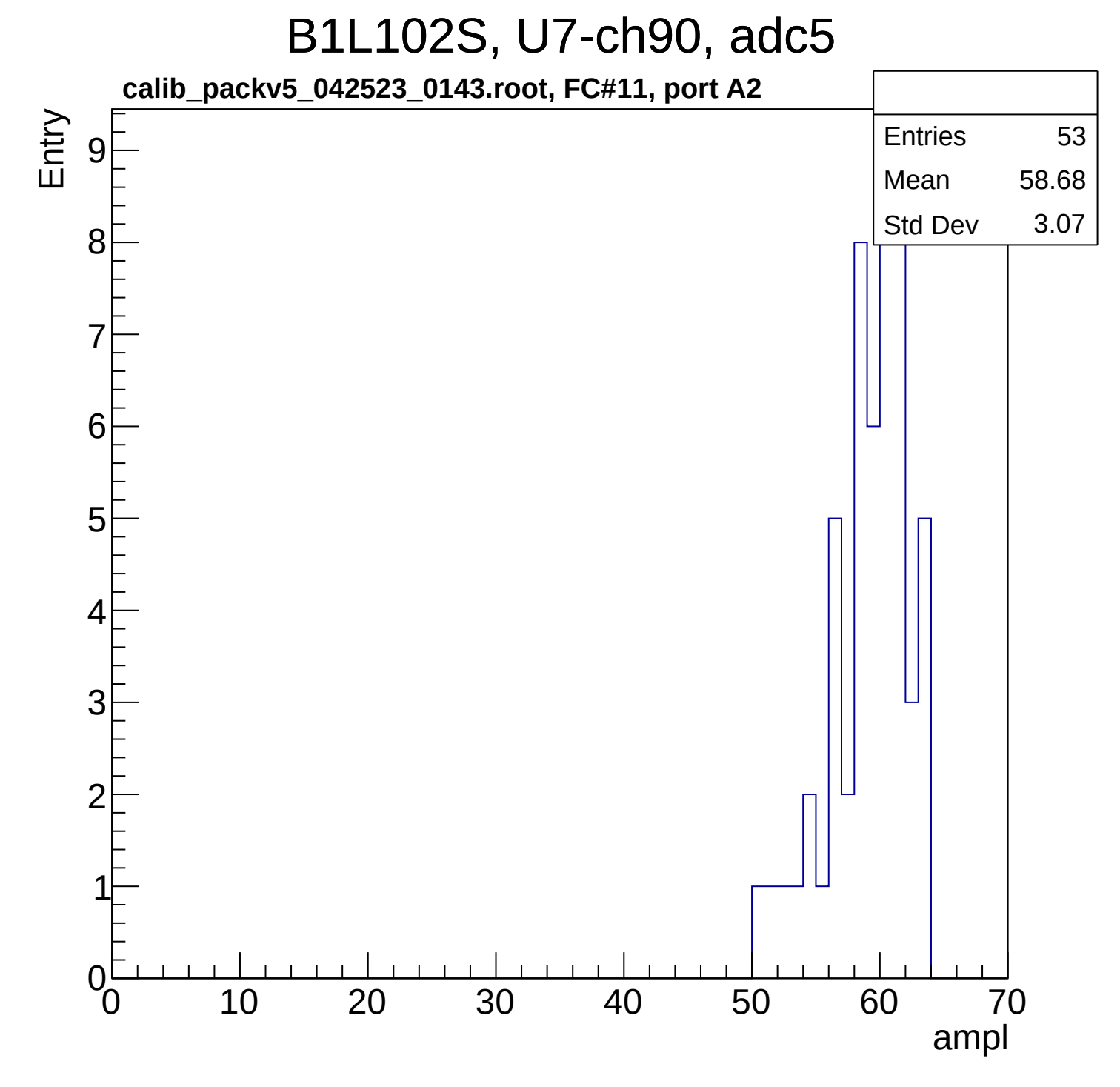
40
50
60
70


B1L102S, U7-ch90, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 42
Mean 54.69
Std Dev 2.964
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L102S, U7-ch90, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 53
Mean 58.68
Std Dev 3.07
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
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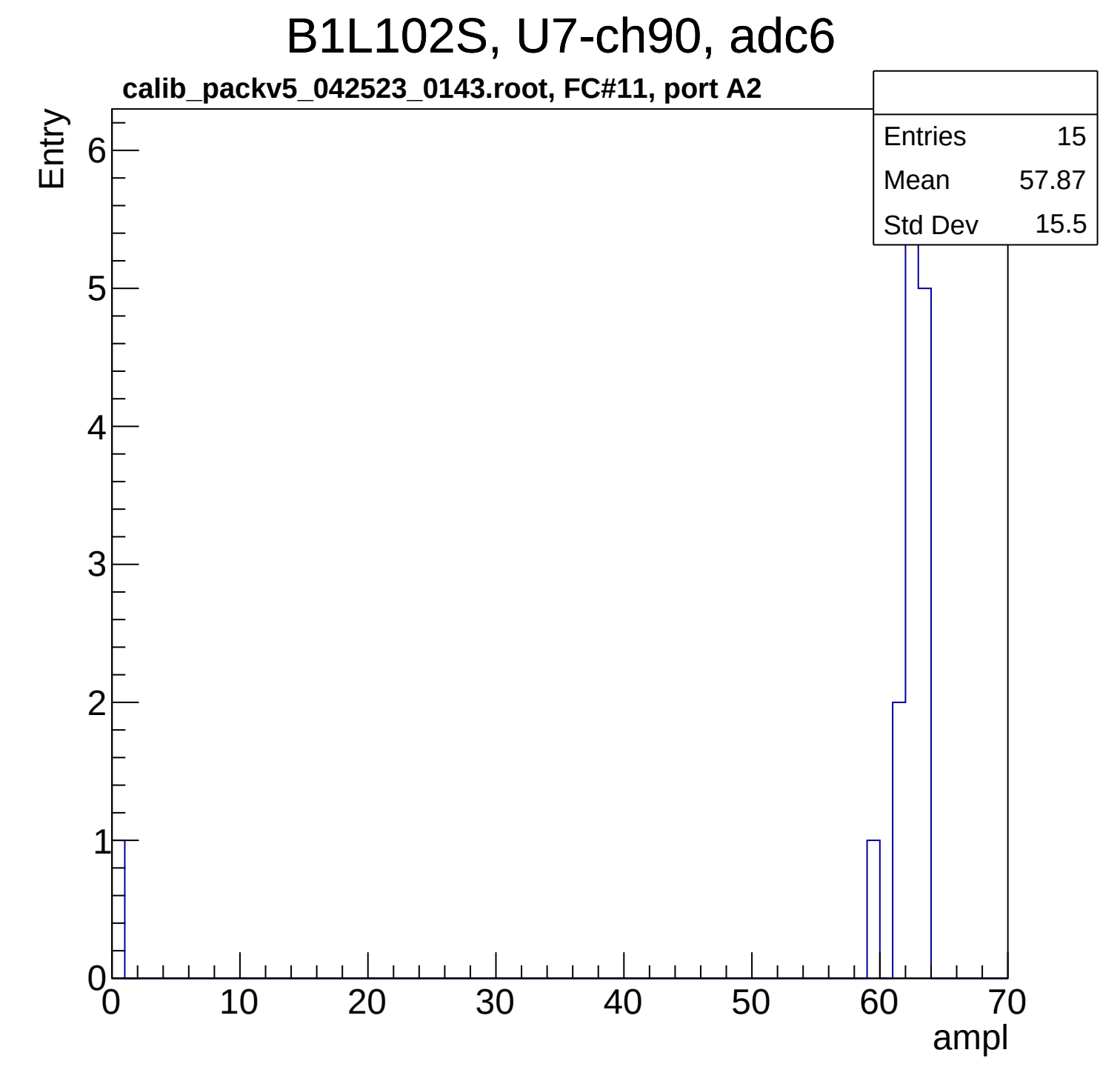
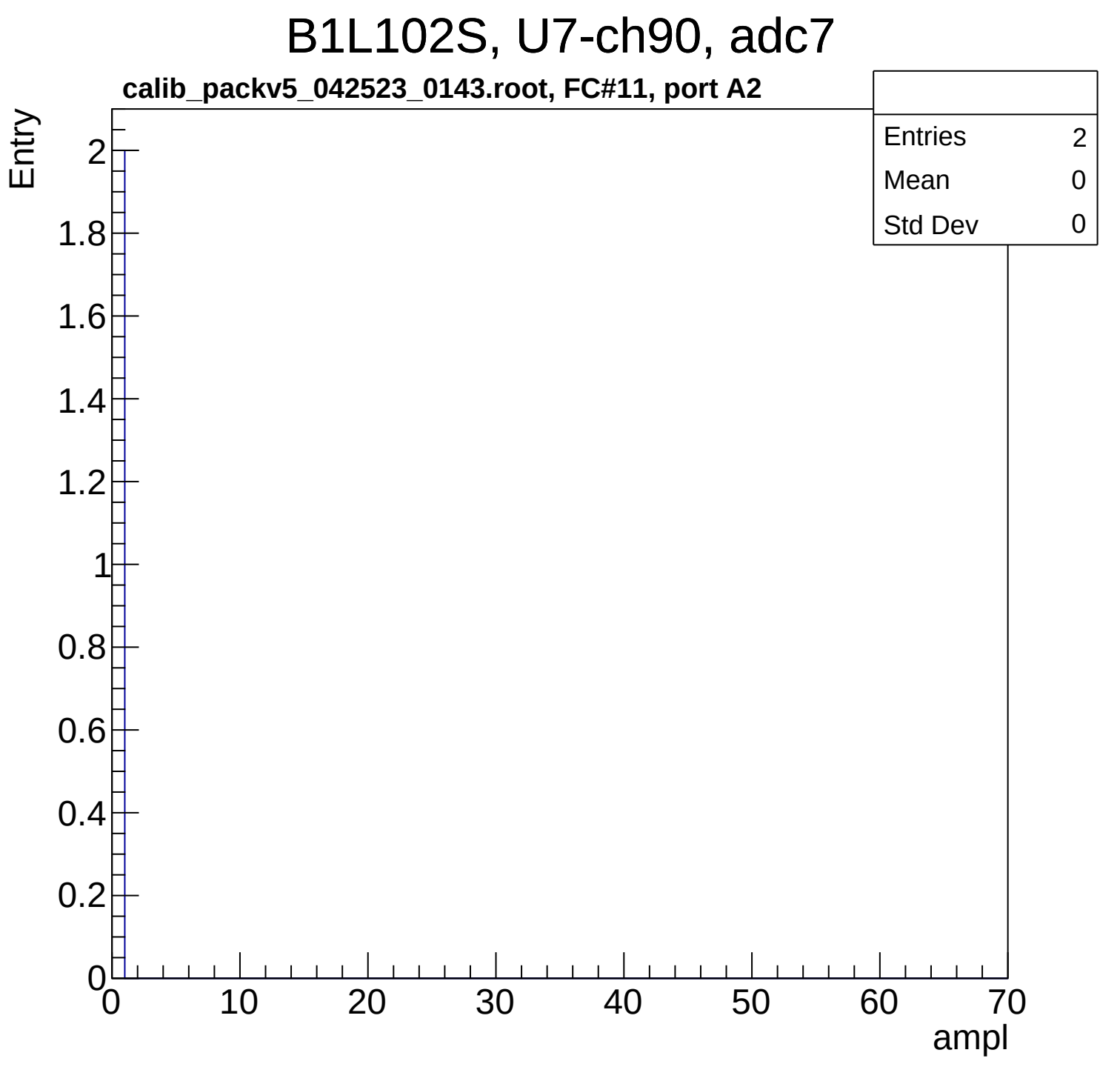
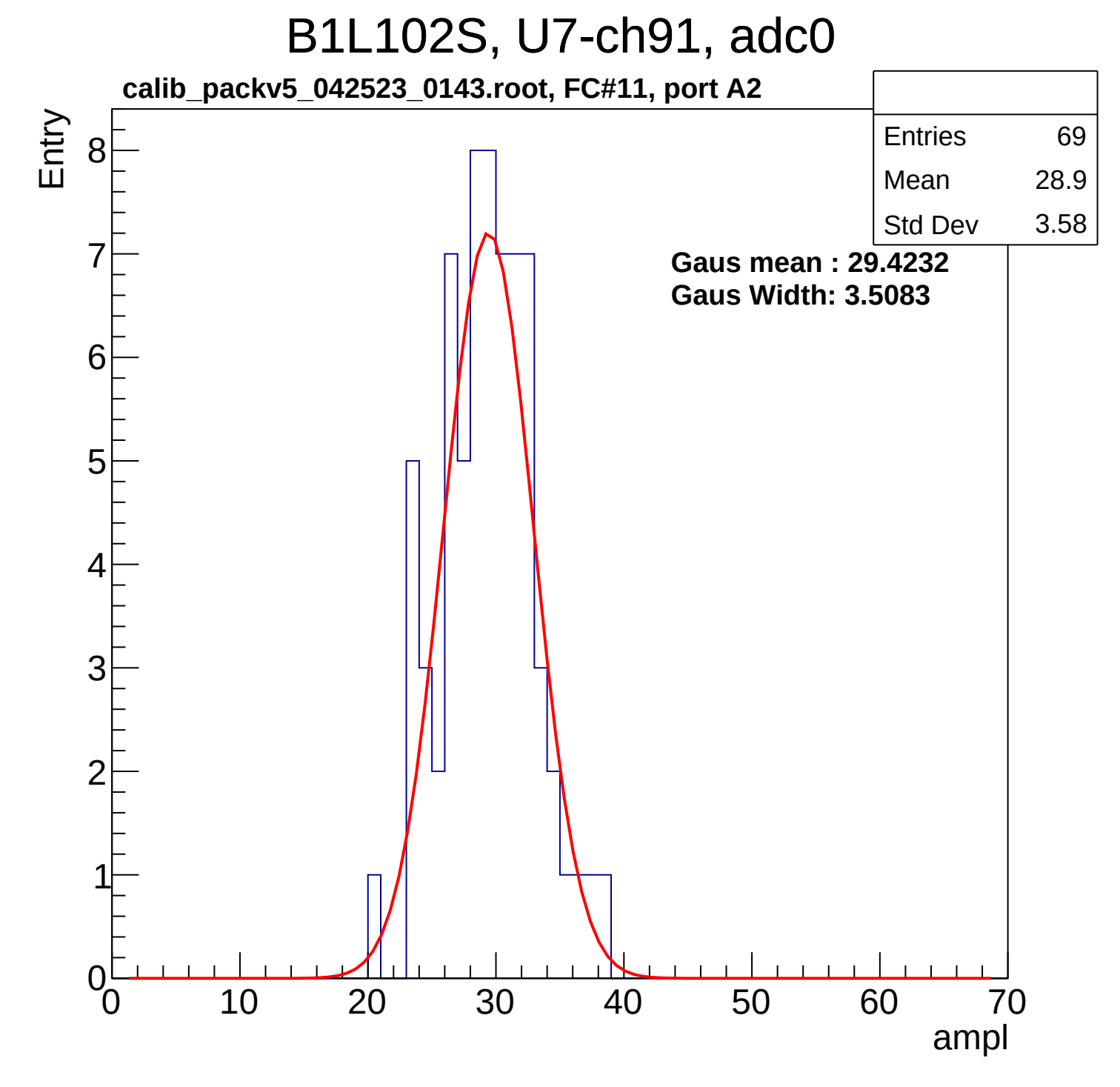
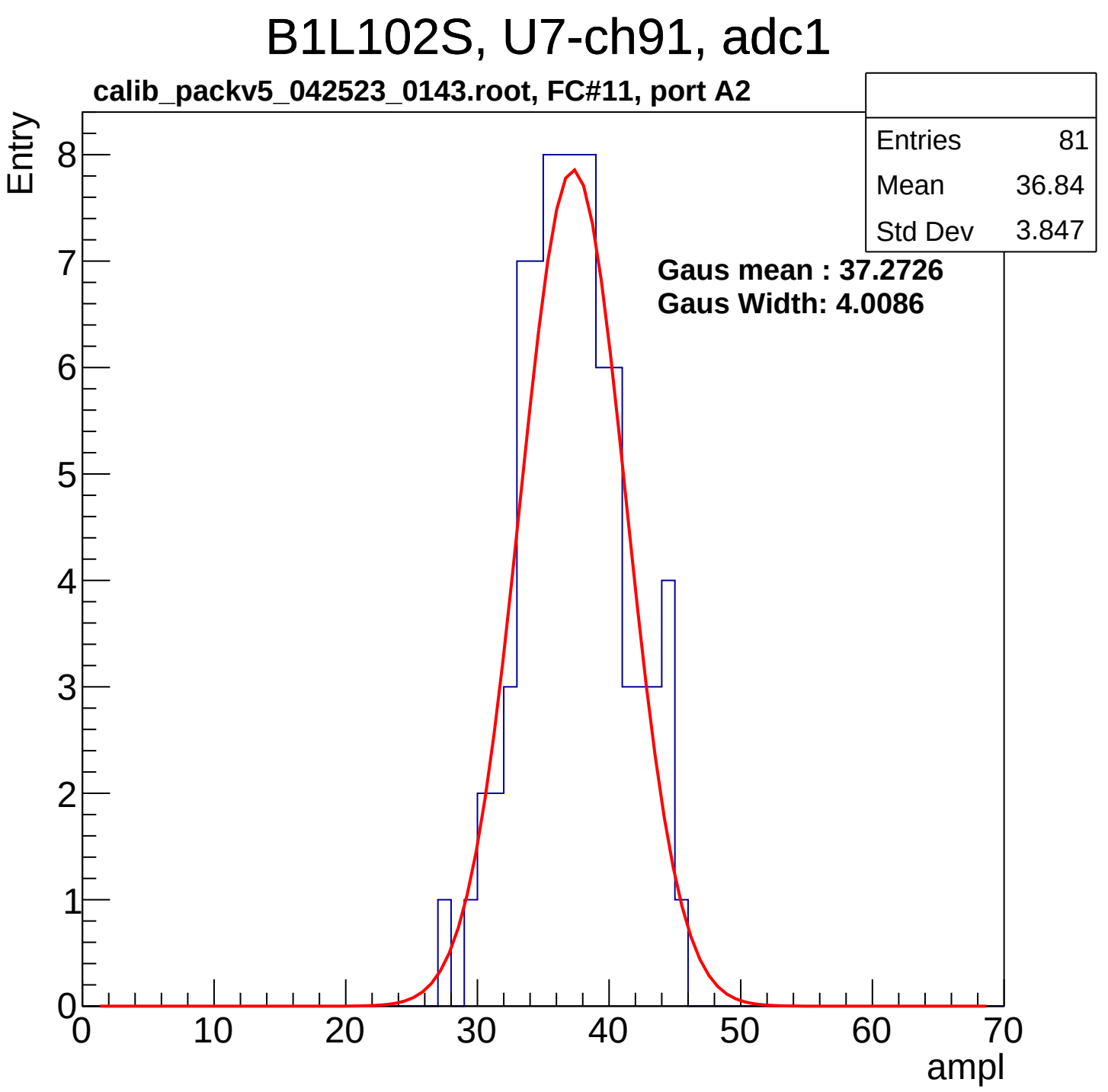
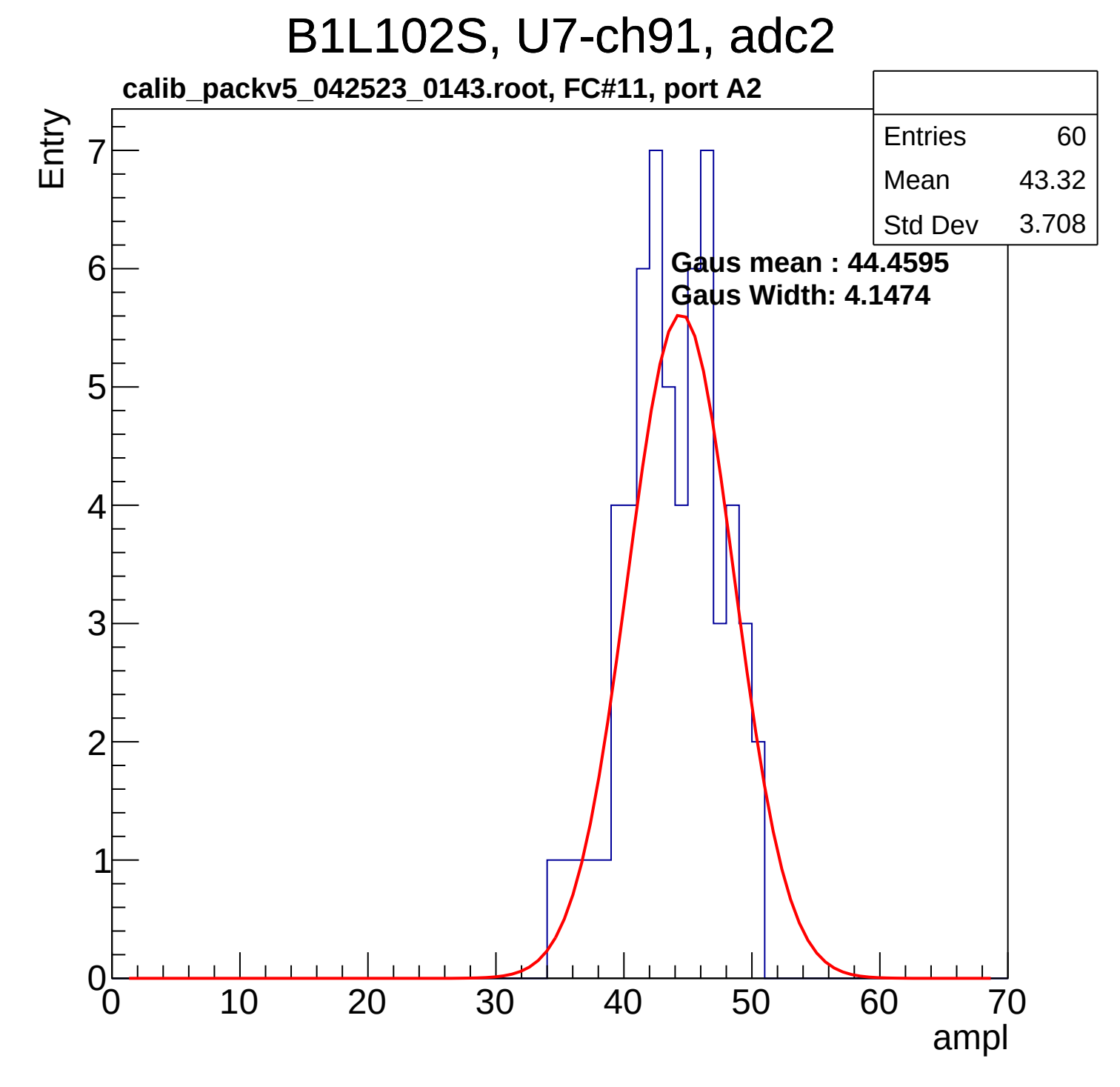
40
50
60
70

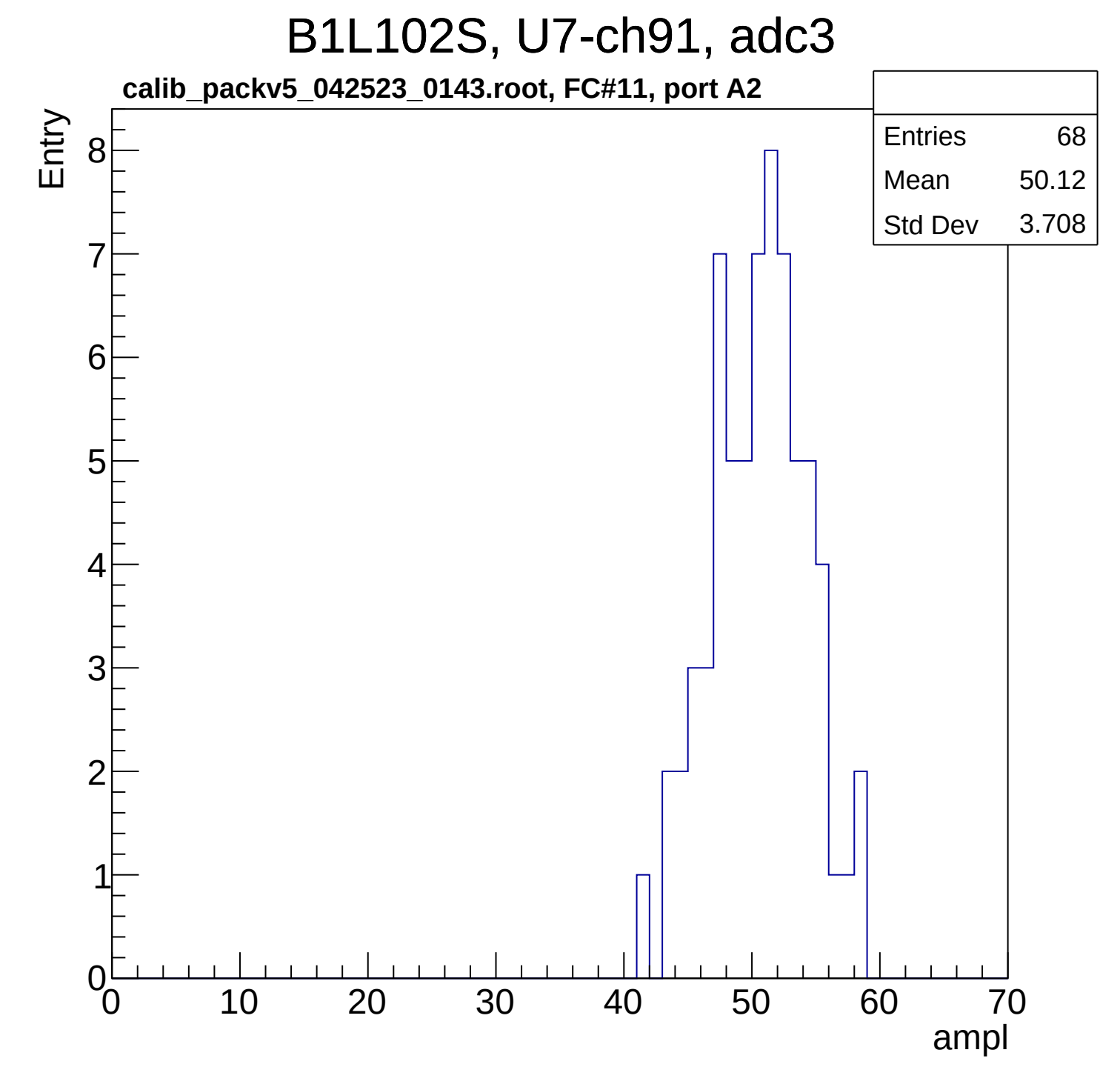

B1L102S, U7-ch90, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 15
Mean 57.87
Std Dev 15.5
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L102S, U7-ch90, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 2
Mean 0
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L102S, U7-ch91, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 69
Mean 28.9
Std Dev 3.58
Gaus mean : 29.4232
Gaus Width: 3.5083
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L102S, U7-ch91, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 81
Mean 36.84
Std Dev 3.847
Gaus mean : 37.2726
Gaus Width: 4.0086
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L102S, U7-ch91, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 60
Mean 43.32
Std Dev 3.708
Gaus mean : 44.4595
Gaus Width: 4.1474
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L102S, U7-ch91, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 68
Mean 50.12
Std Dev 3.708
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
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40
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60
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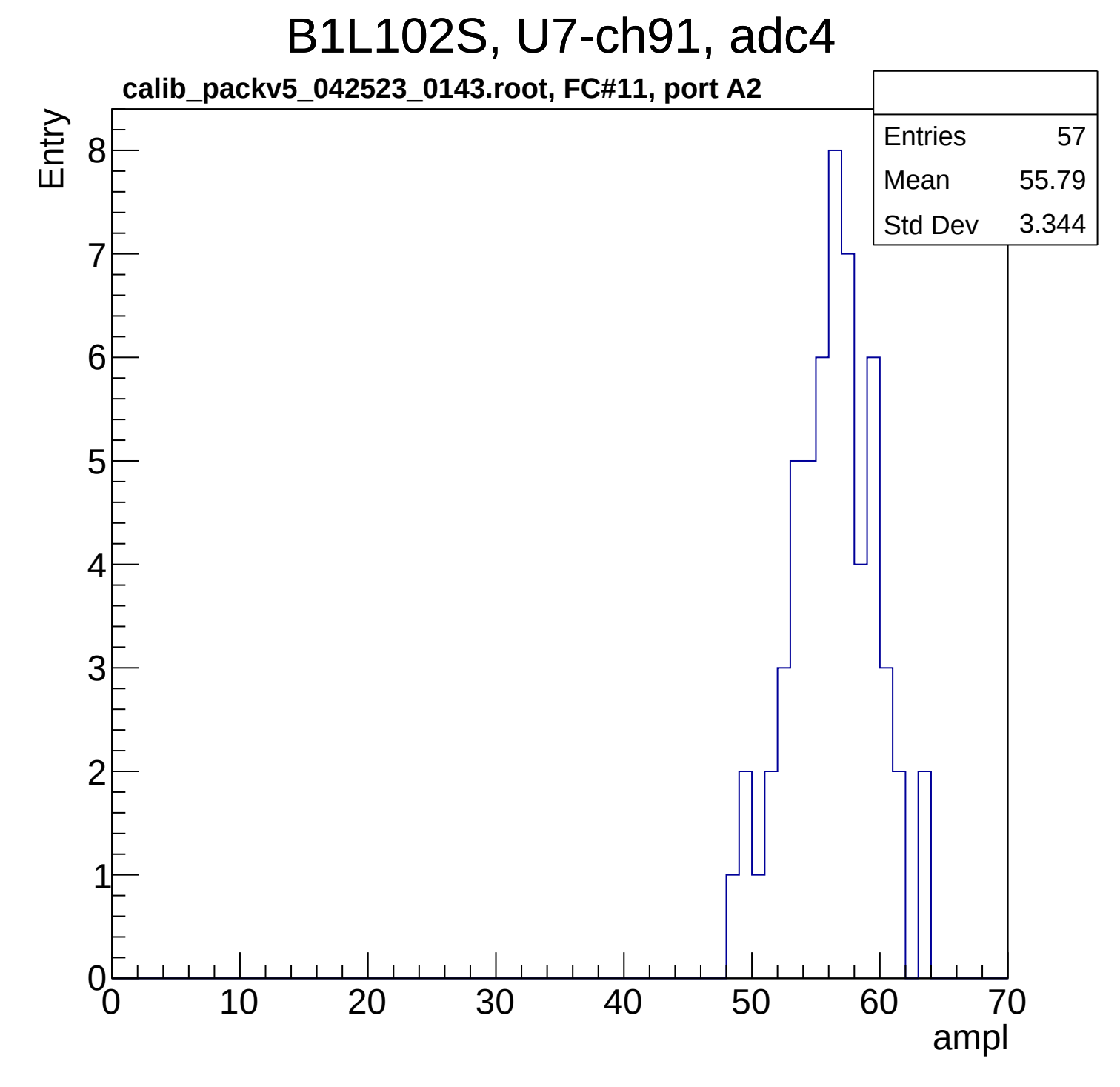
B1L102S, U7-ch91, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 57
Mean 55.79
Std Dev 3.344
Entry
ampl
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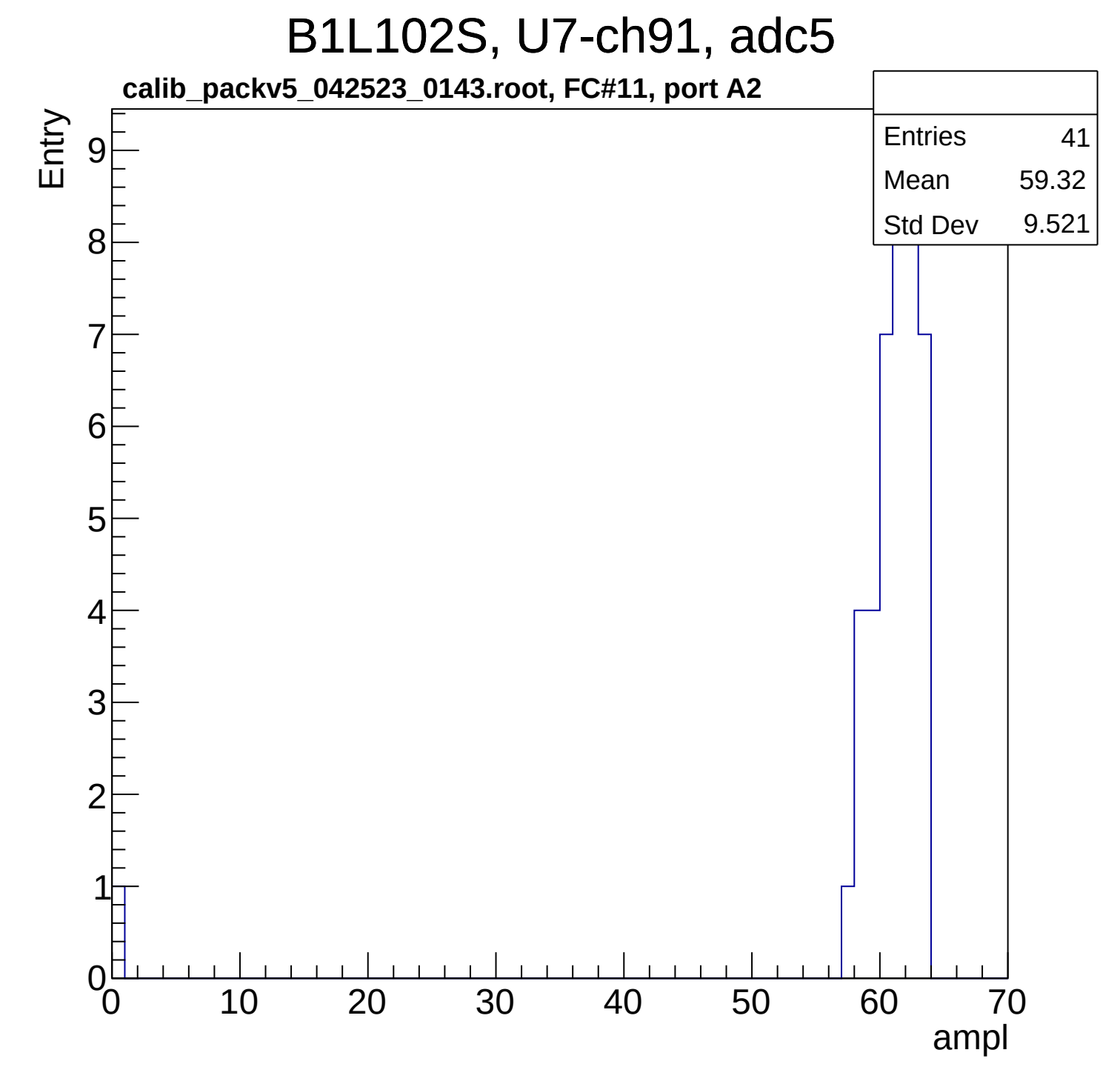
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L102S, U7-ch91, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 41
Mean 59.32
Std Dev 9.521
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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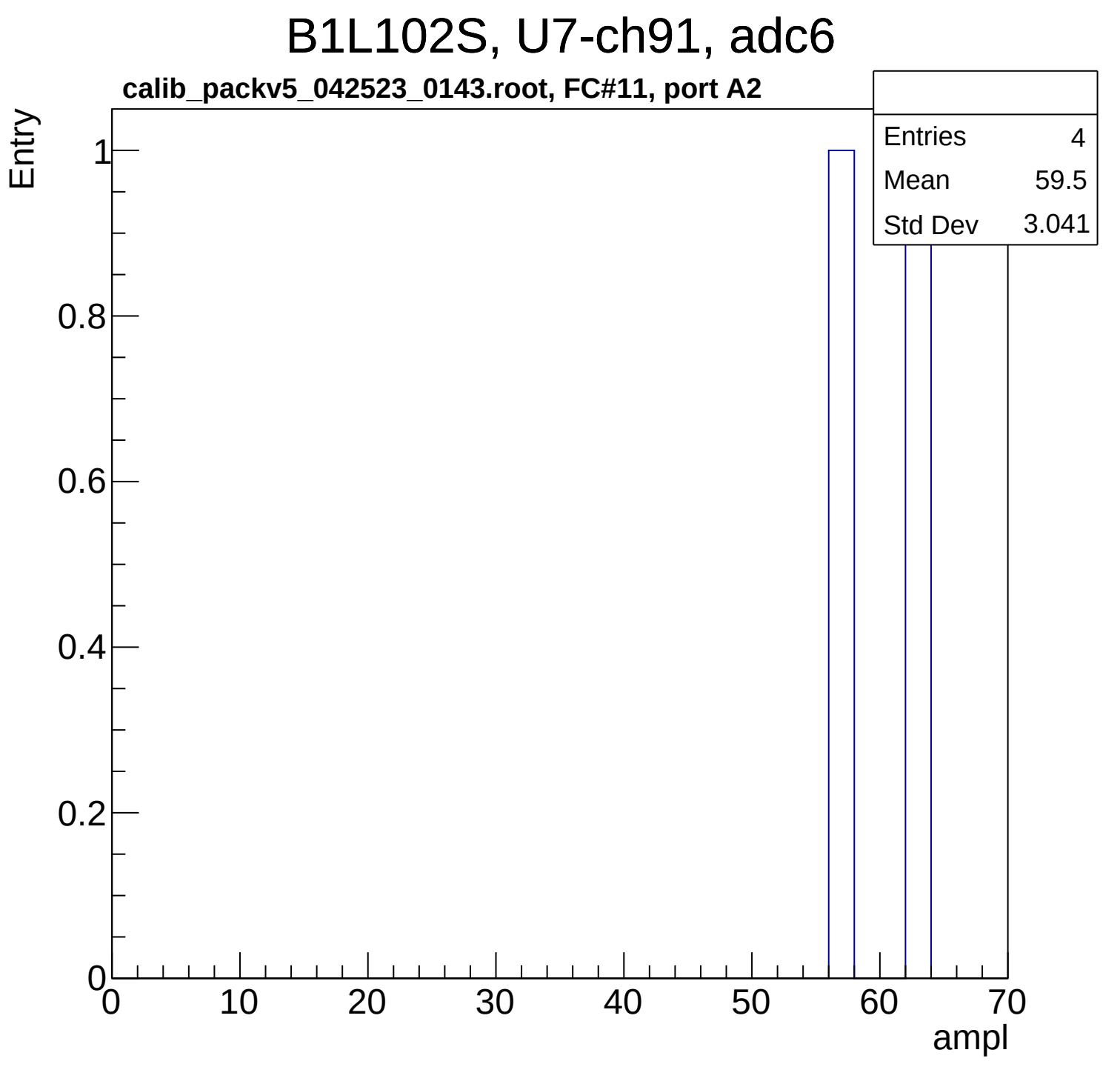
40
50
60
70


B1L102S, U7-ch91, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 4
Mean 59.5
Std Dev 3.041
Entry
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0.6
0.4
0.2
0
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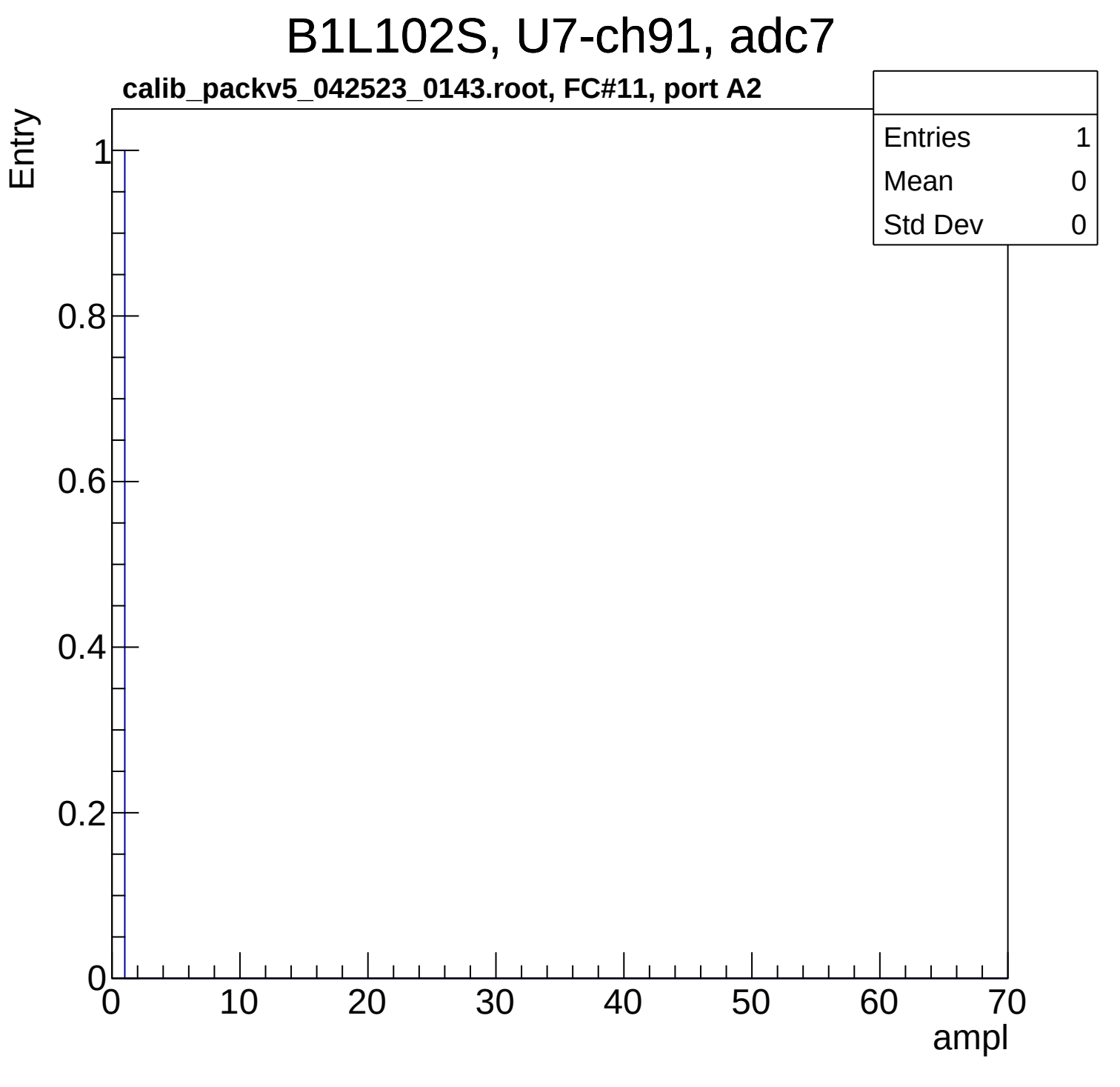
10
20
30
40
50
60
70
ampl


B1L102S, U7-ch91, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 1
Mean 0
Std Dev 0
Entry
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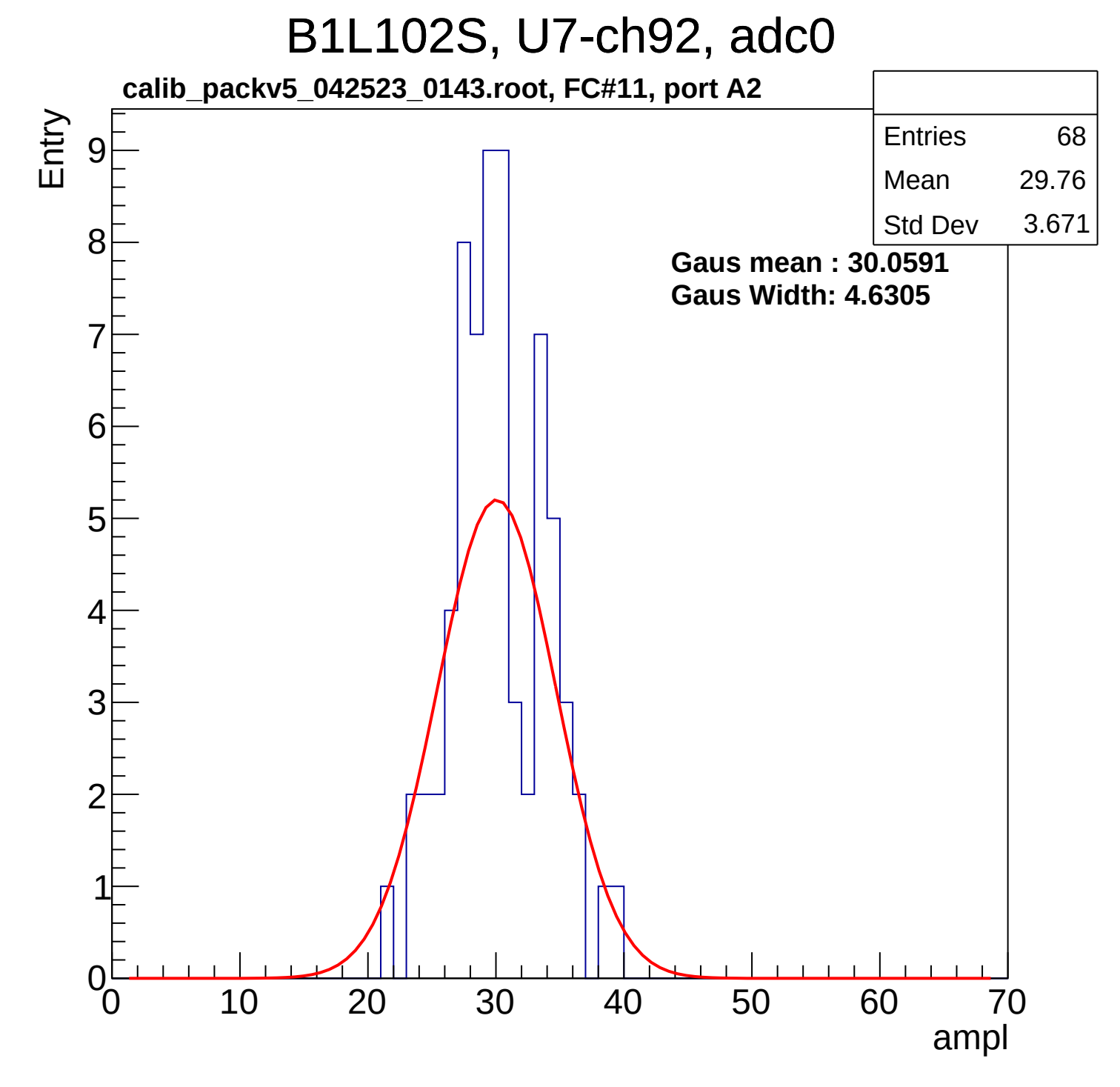
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U7-ch92, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 68
Mean 29.76
Std Dev 3.671
Gaus mean : 30.0591
Gaus Width: 4.6305
Entry
ampl
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2
3
4
5
6
7
8
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0
10
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30
40
50
60
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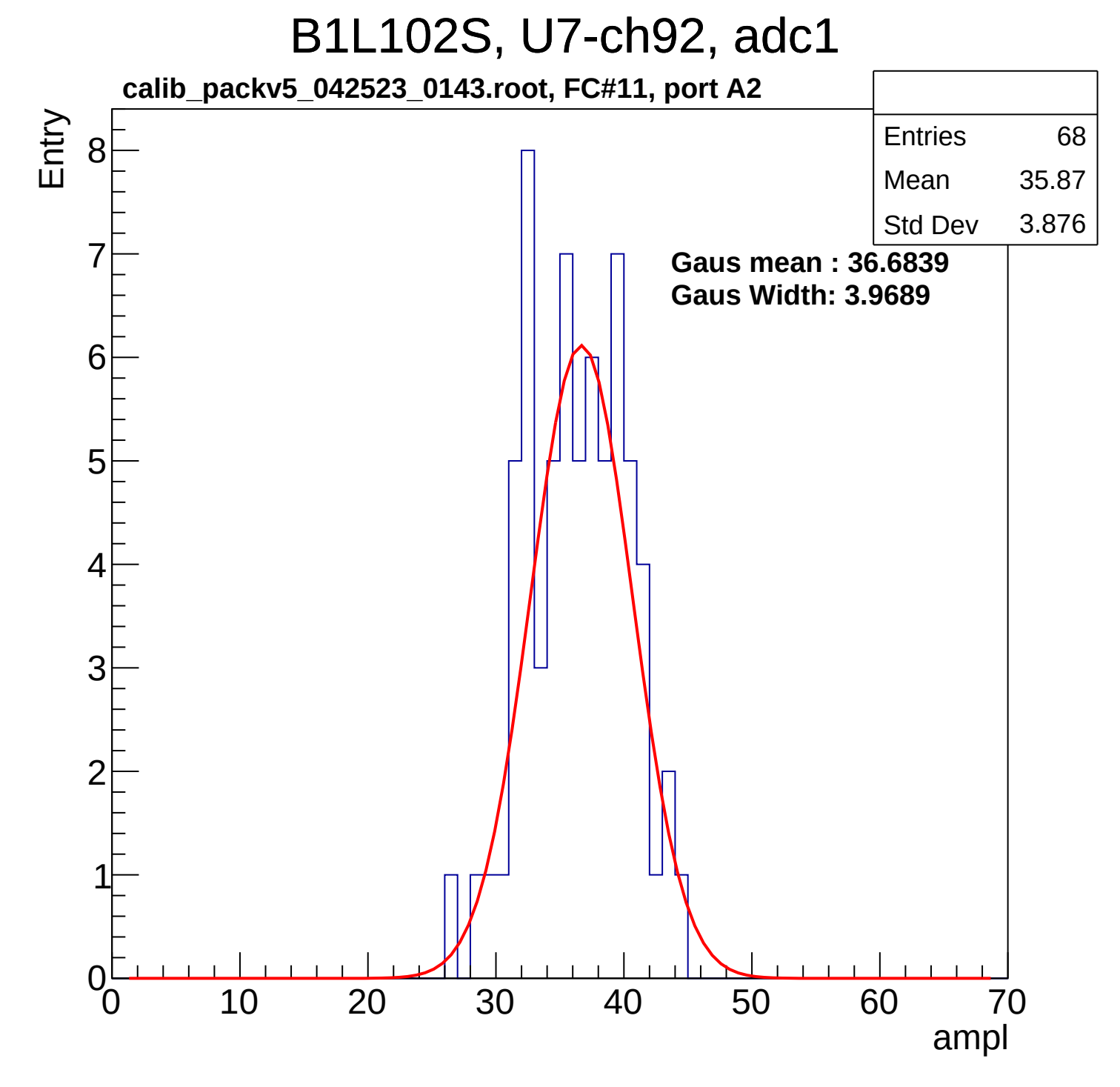
B1L102S, U7-ch92, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 68
Mean 35.87
Std Dev 3.876
Gaus mean : 36.6839
Gaus Width: 3.9689
Entry
ampl
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1
2
3
4
5
6
7
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0
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60
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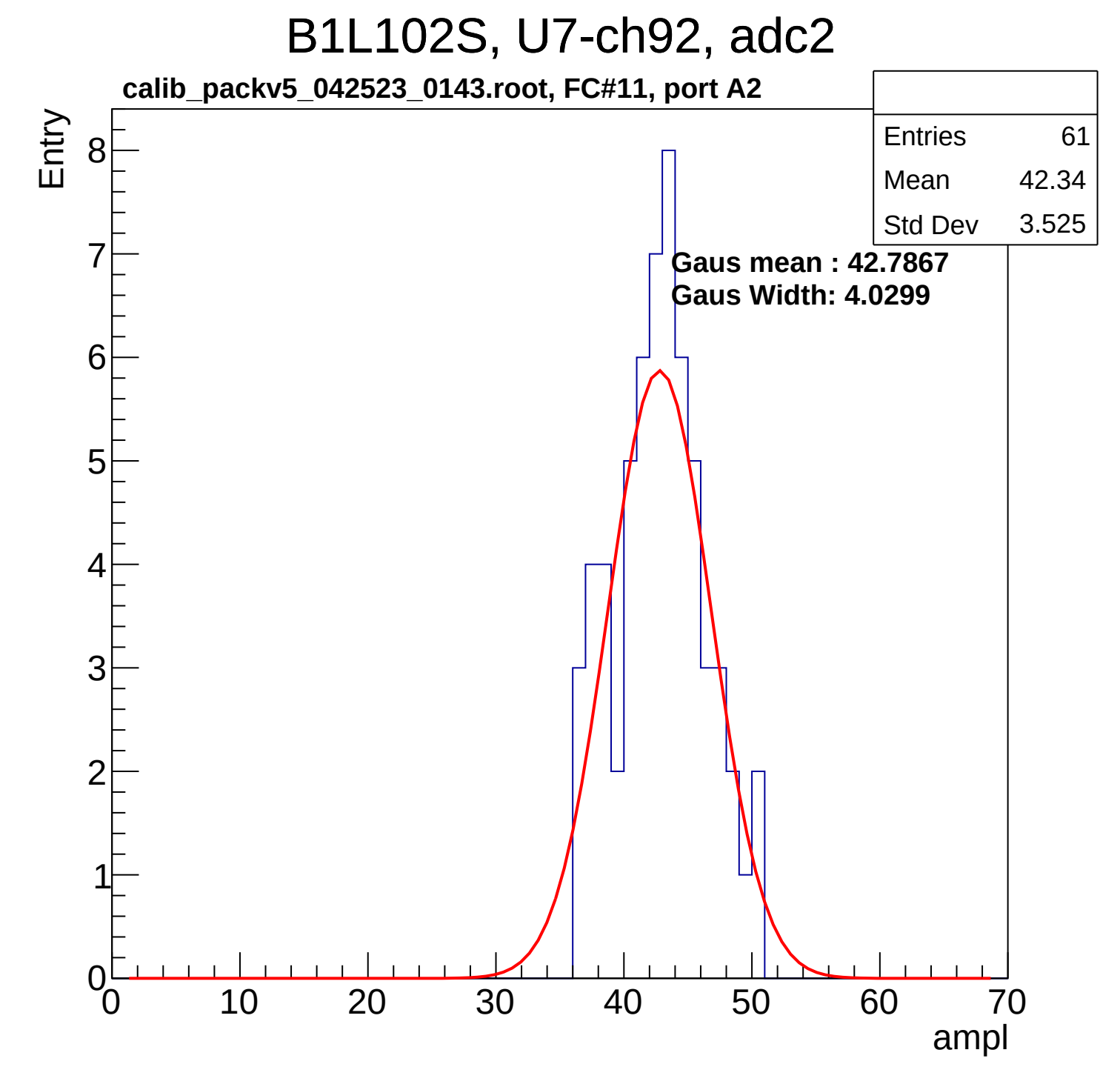
B1L102S, U7-ch92, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 61
Mean 42.34
Std Dev 3.525
Gaus mean : 42.7867
Gaus Width: 4.0299
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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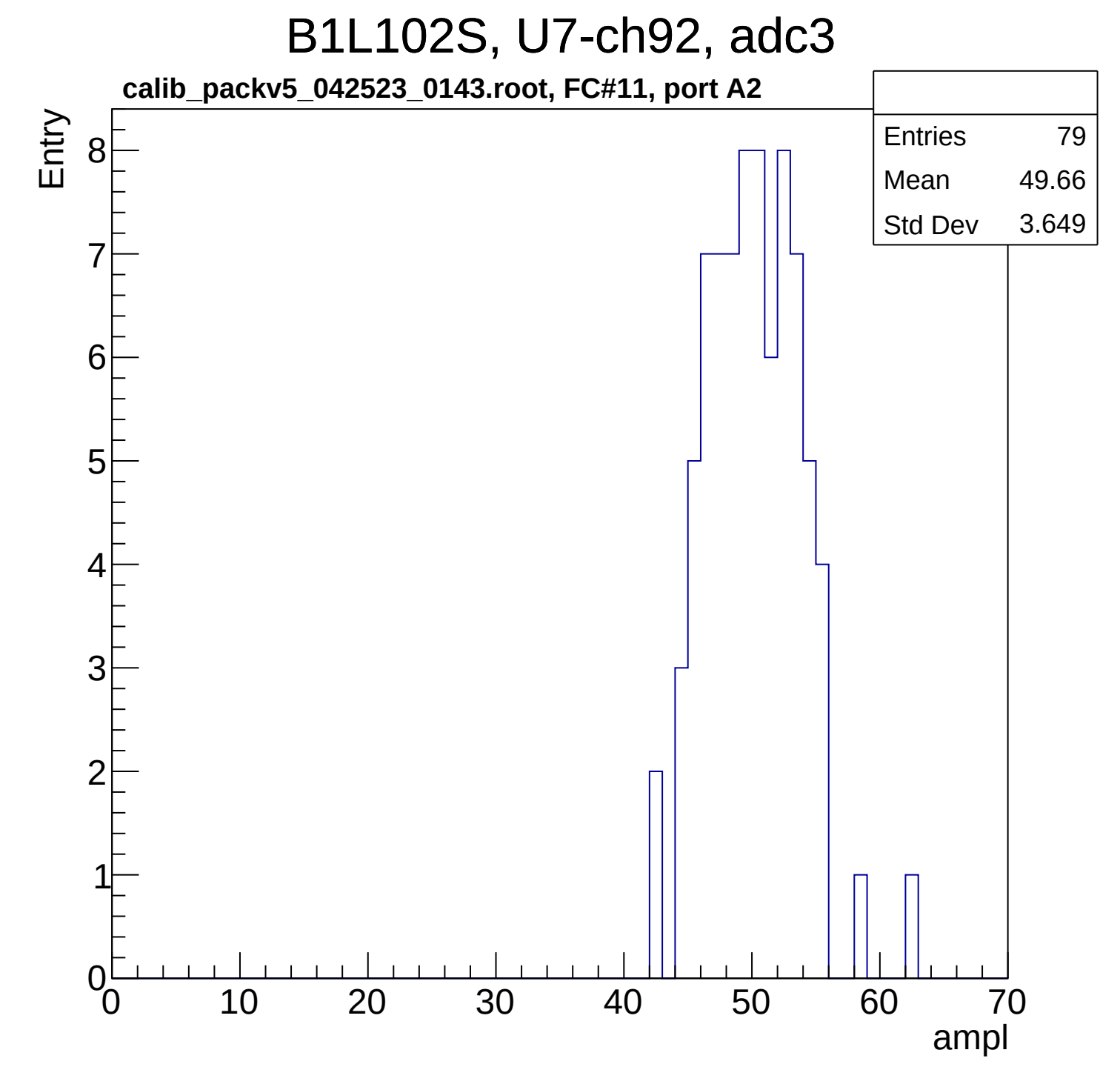
B1L102S, U7-ch92, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 79
Mean 49.66
Std Dev 3.649
Entry
ampl
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2
3
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5
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0
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60
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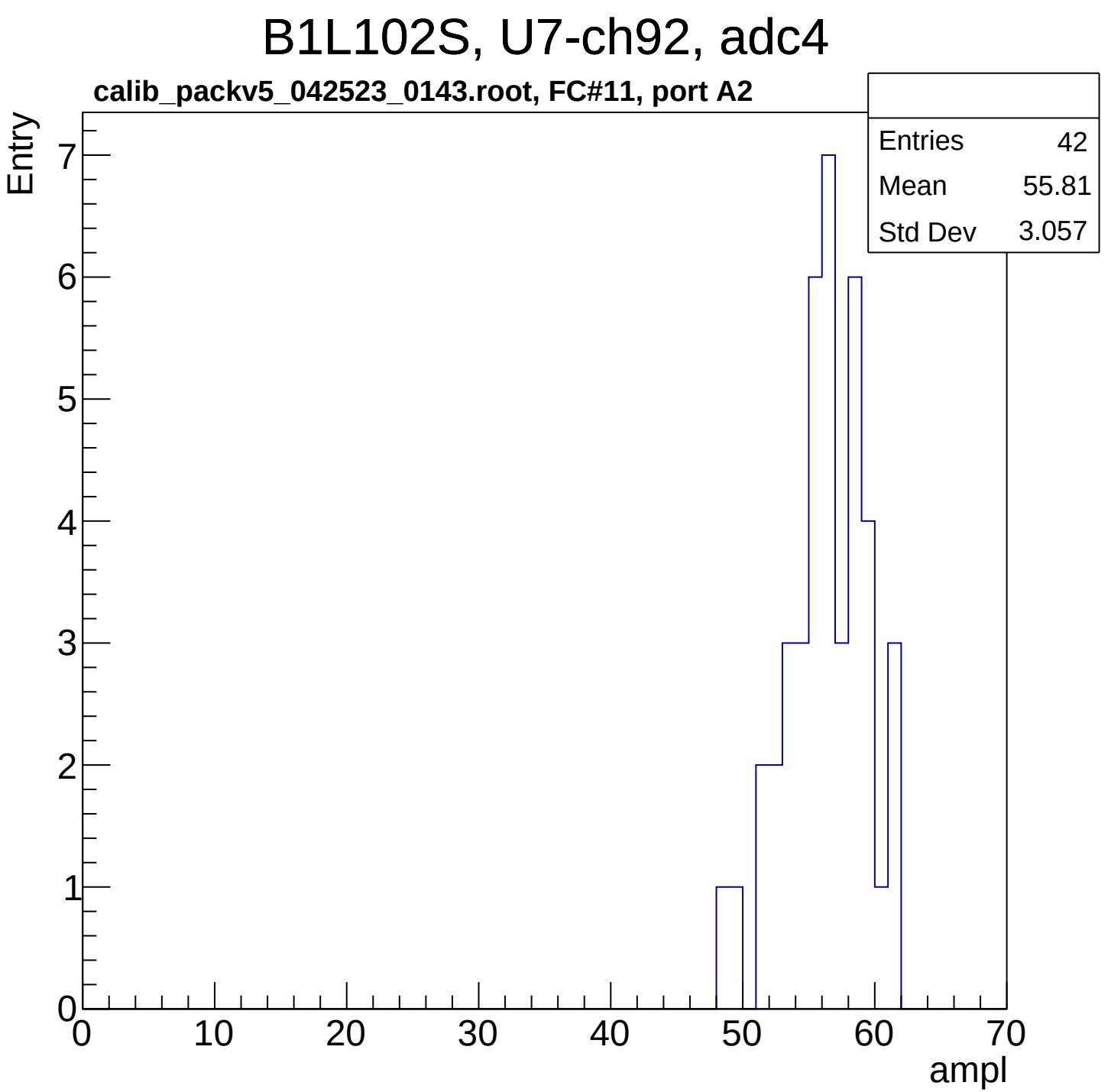
B1L102S, U7-ch92, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 42
Mean 55.81
Std Dev 3.057
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
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40
50
60
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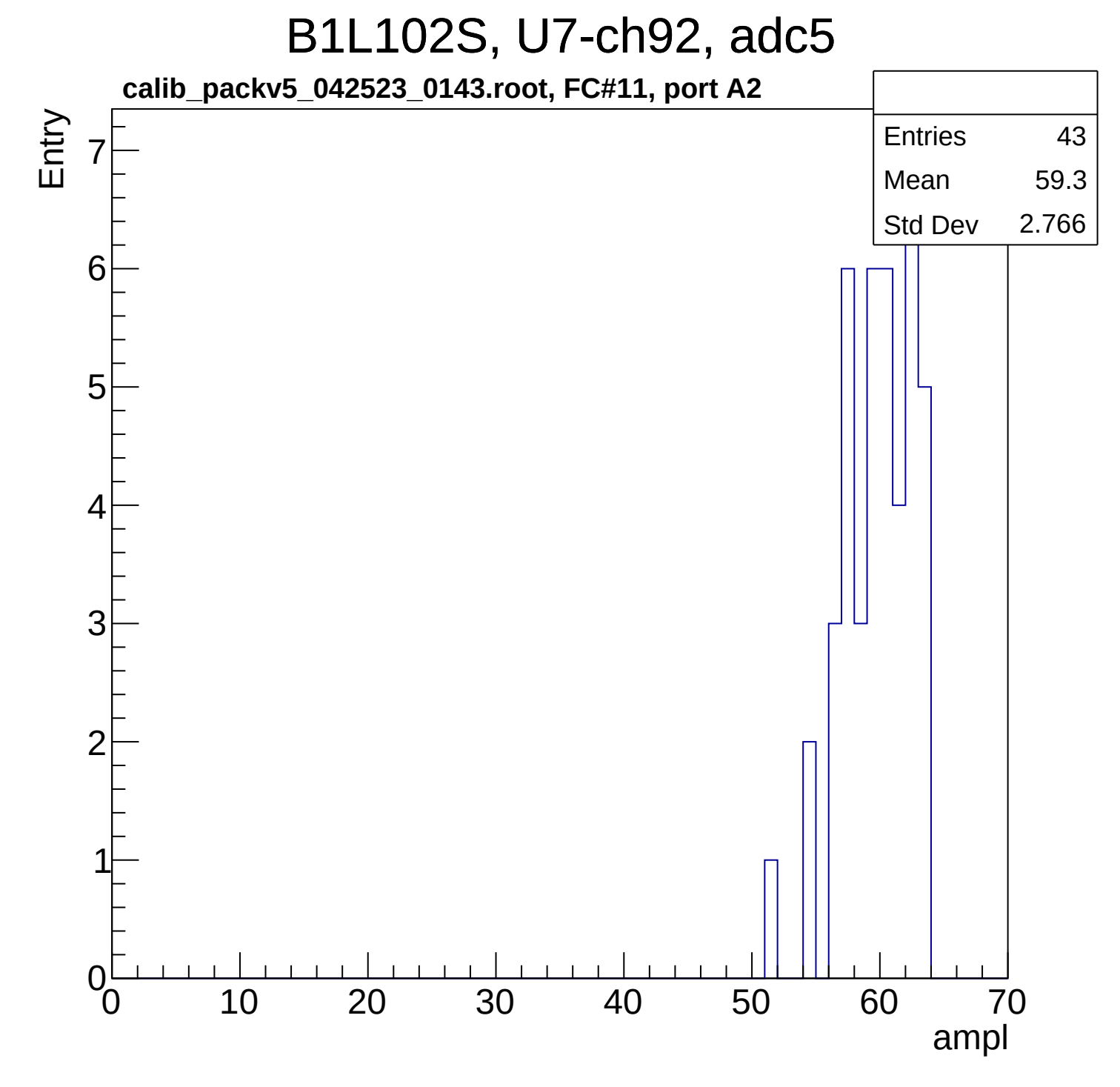
B1L102S, U7-ch92, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 43
Mean 59.3
Std Dev 2.766
Entry
ampl
0
1
2
3
4
5
6
7
0
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20
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40
50
60
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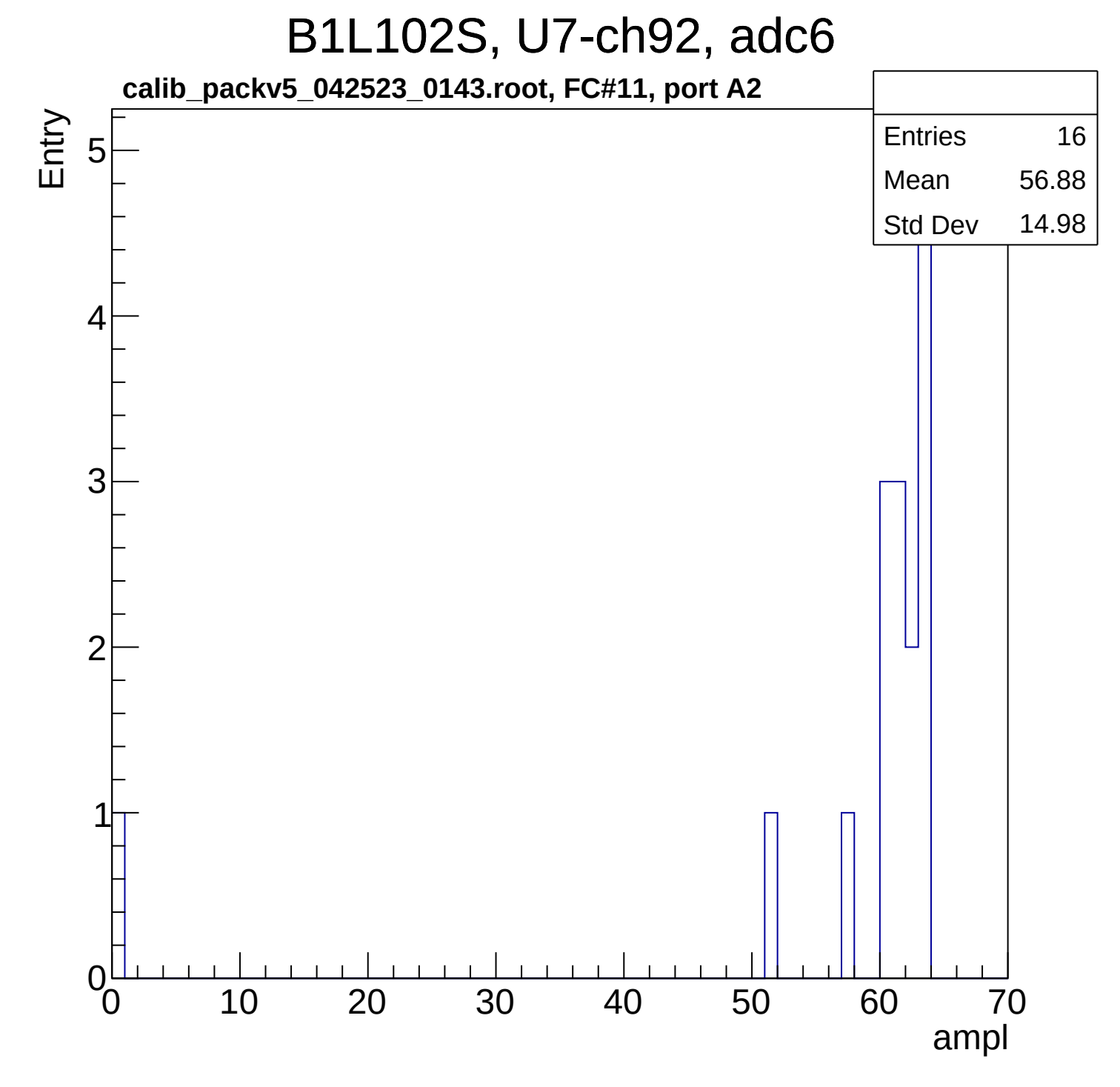
B1L102S, U7-ch92, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 16
Mean 56.88
Std Dev 14.98
Entry
ampl
0
1
2
3
4
5
0
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20
30
40
50
60
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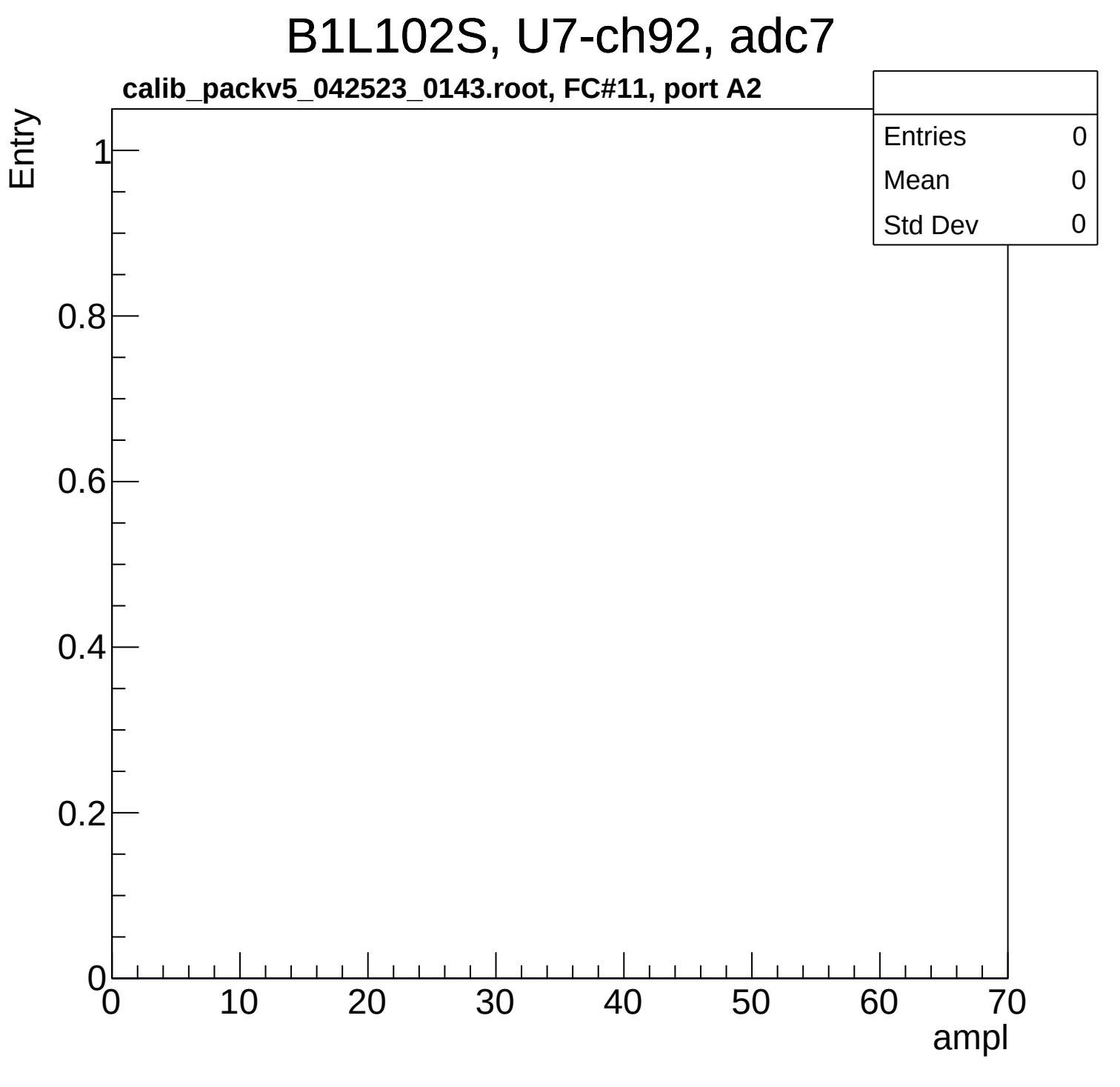
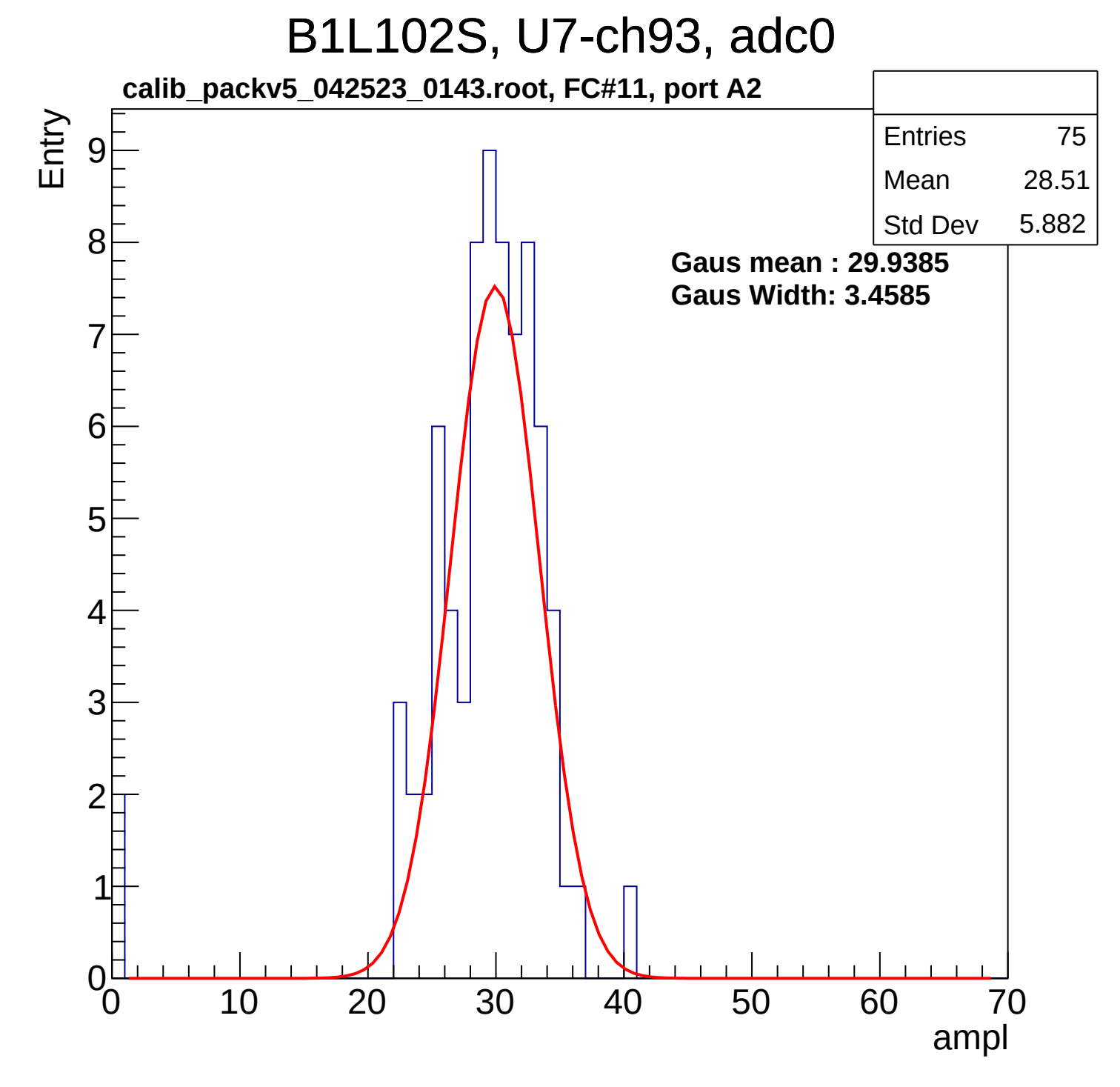

B1L102S, U7-ch92, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U7-ch93, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 75
Mean 28.51
Std Dev 5.882
Gaus mean : 29.9385
Gaus Width: 3.4585
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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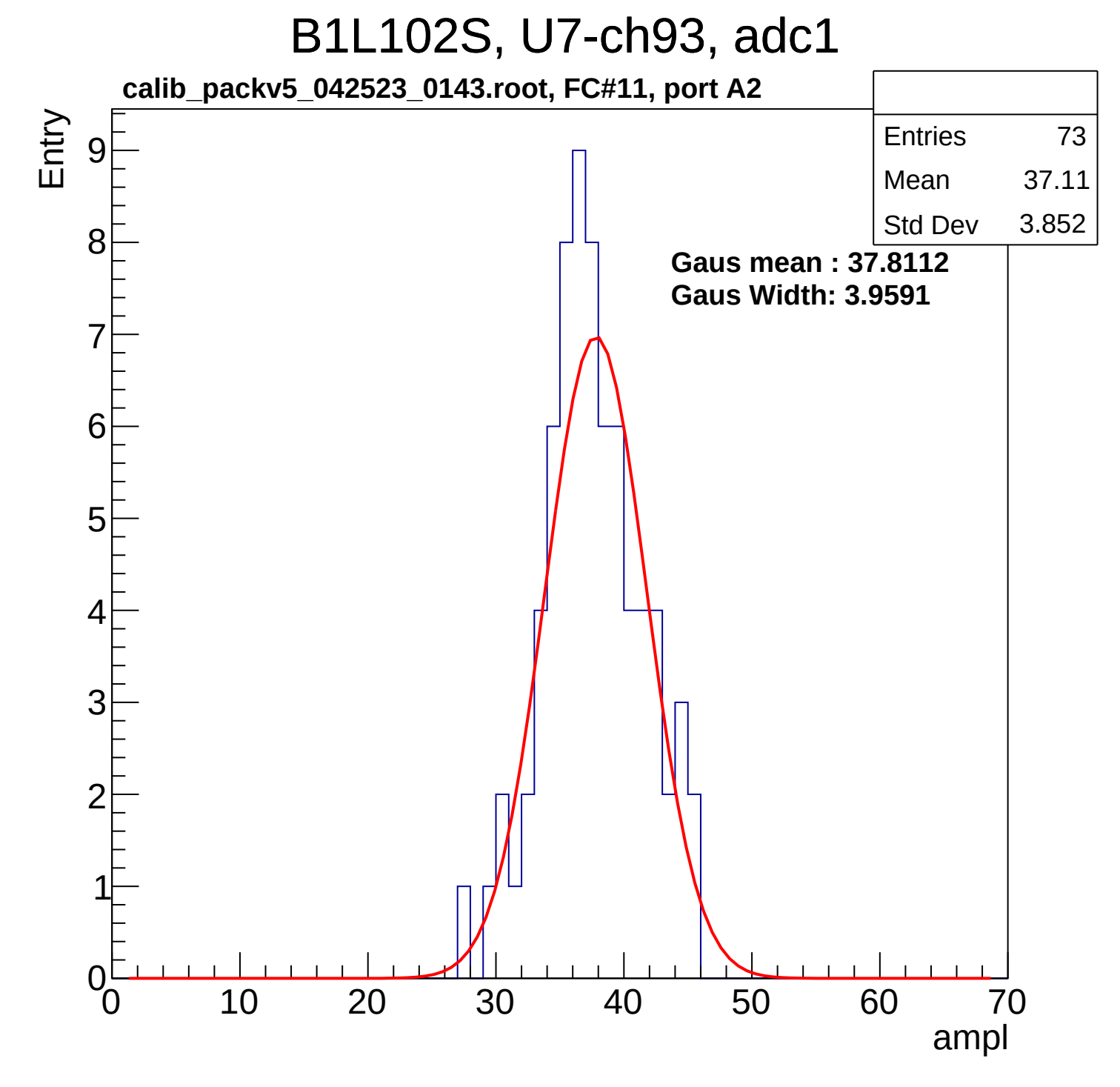
B1L102S, U7-ch93, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 73
Mean 37.11
Std Dev 3.852
Gaus mean : 37.8112
Gaus Width: 3.9591
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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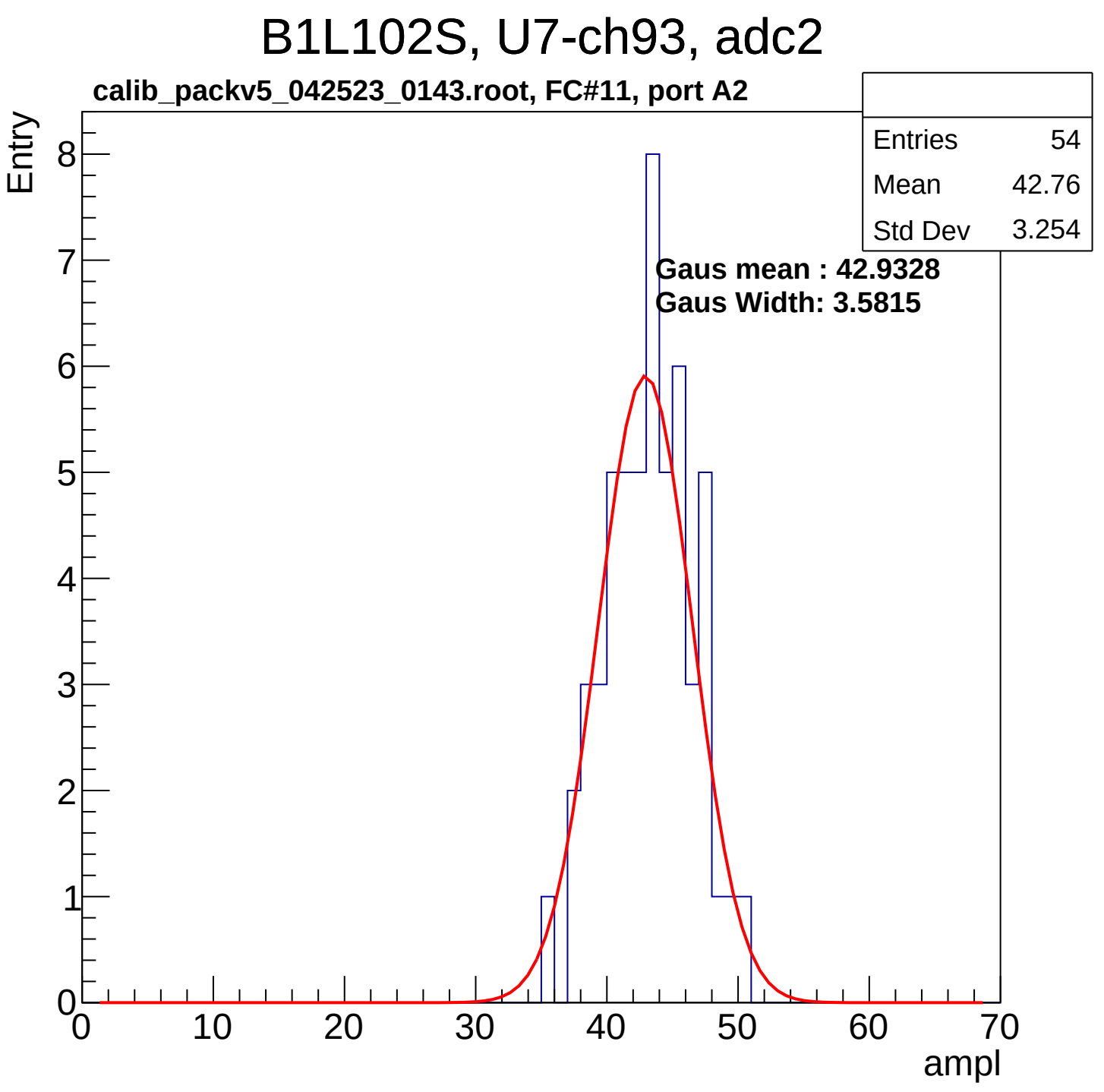
B1L102S, U7-ch93, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 54
Mean 42.76
Std Dev 3.254
Gaus mean : 42.9328
Gaus Width: 3.5815
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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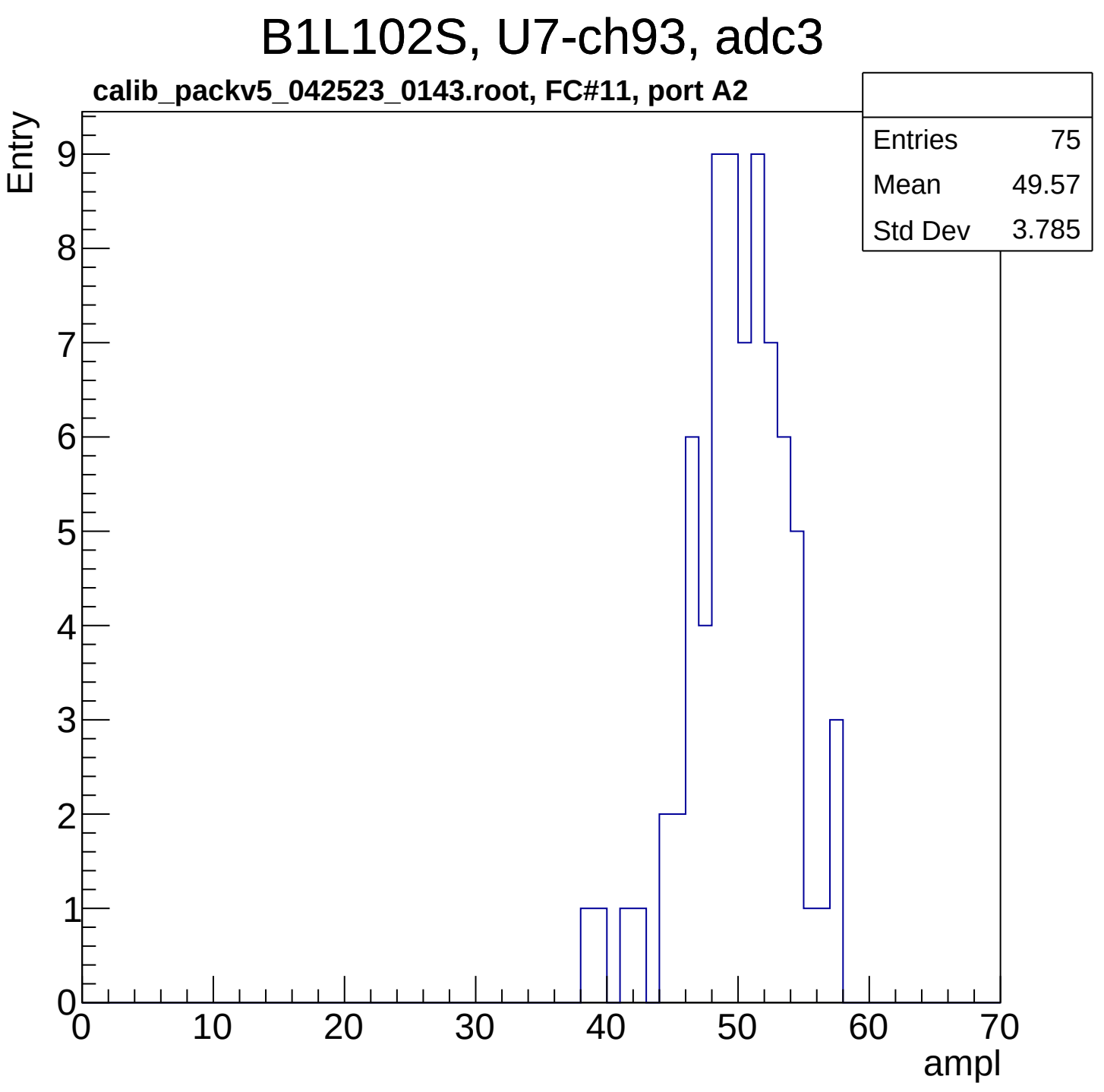
B1L102S, U7-ch93, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 75
Mean 49.57
Std Dev 3.785
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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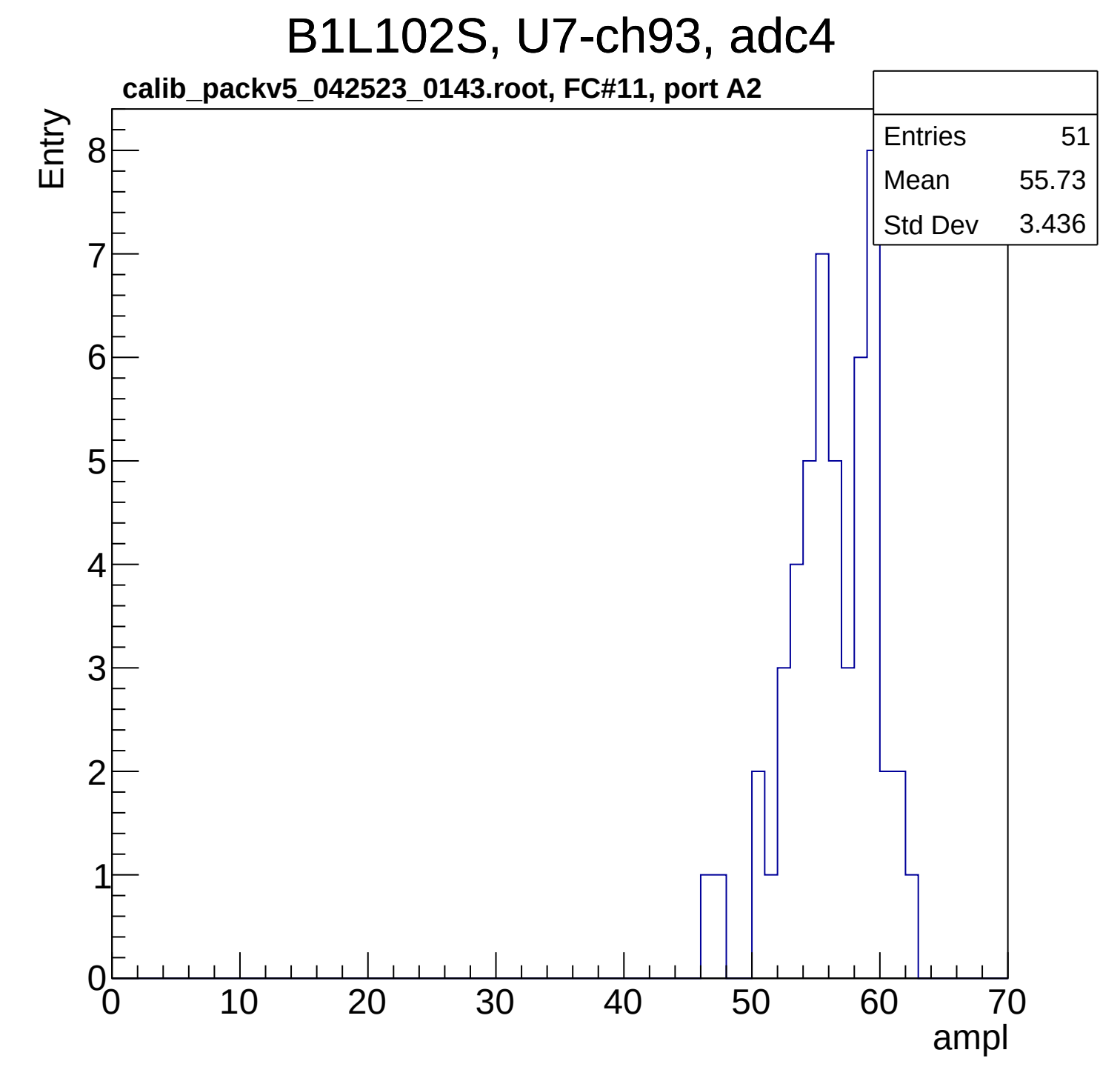
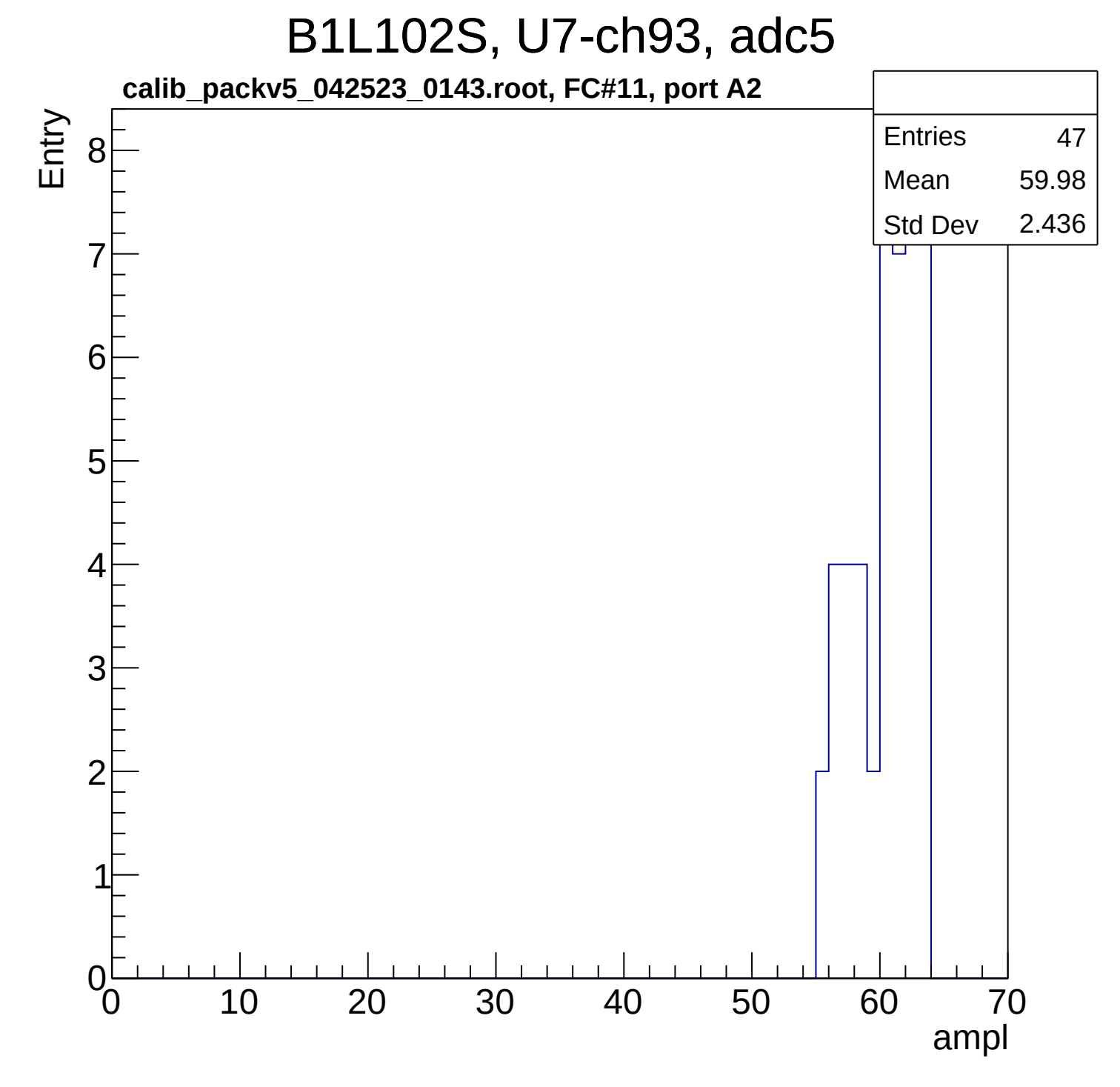

B1L102S, U7-ch93, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 51
Mean 55.73
Std Dev 3.436
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L102S, U7-ch93, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 47
Mean 59.98
Std Dev 2.436
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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40
50
60
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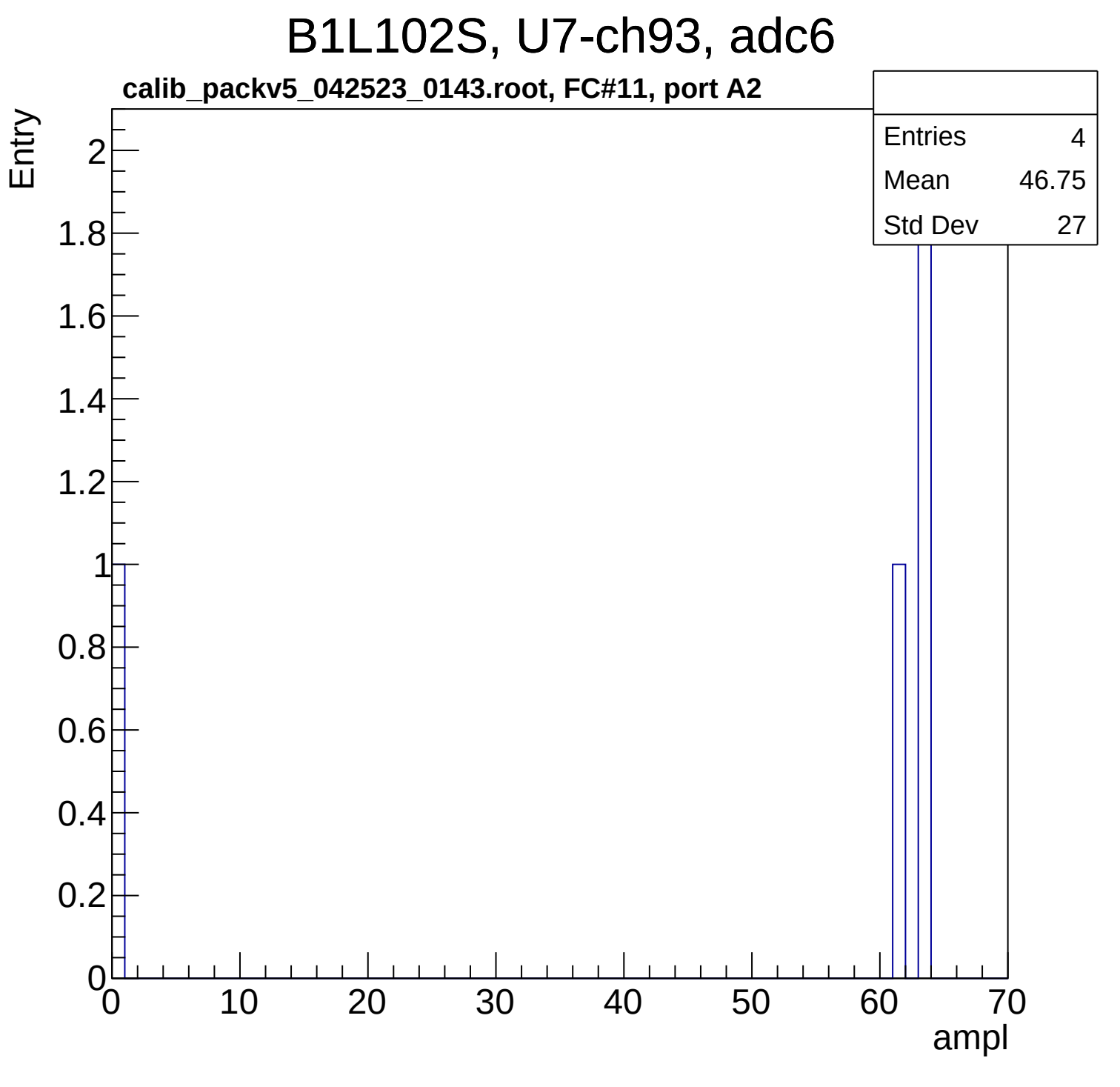
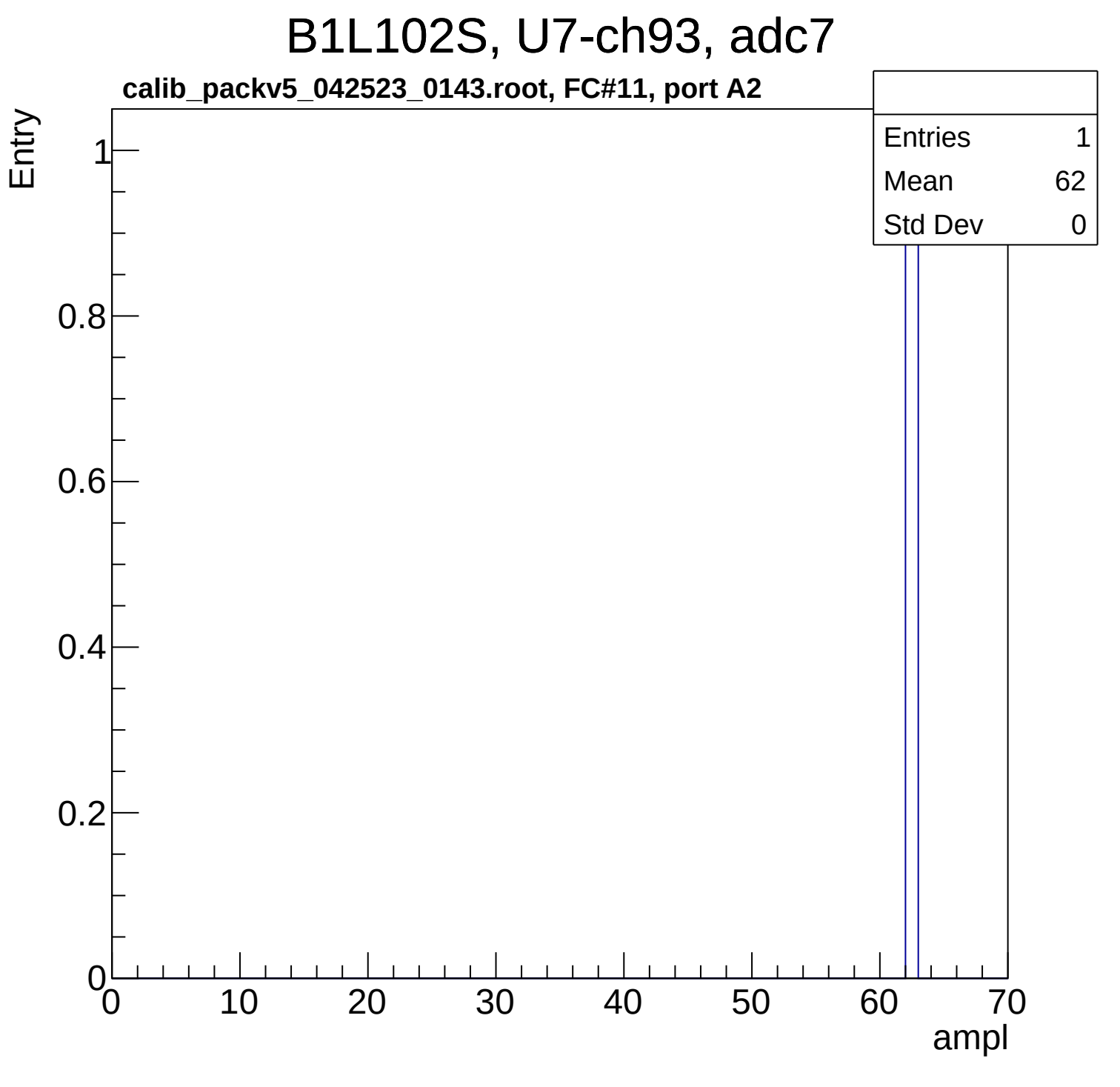
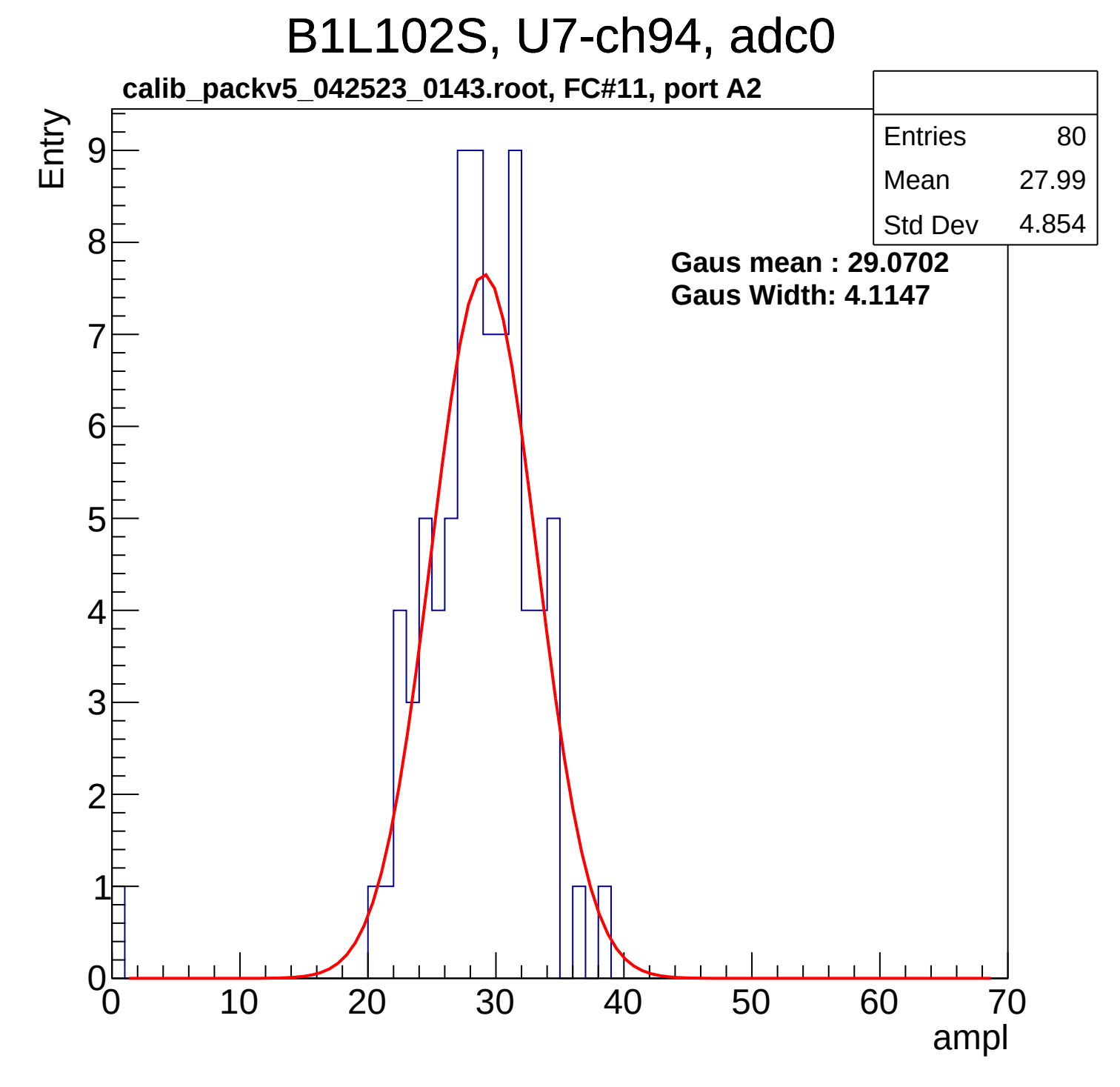
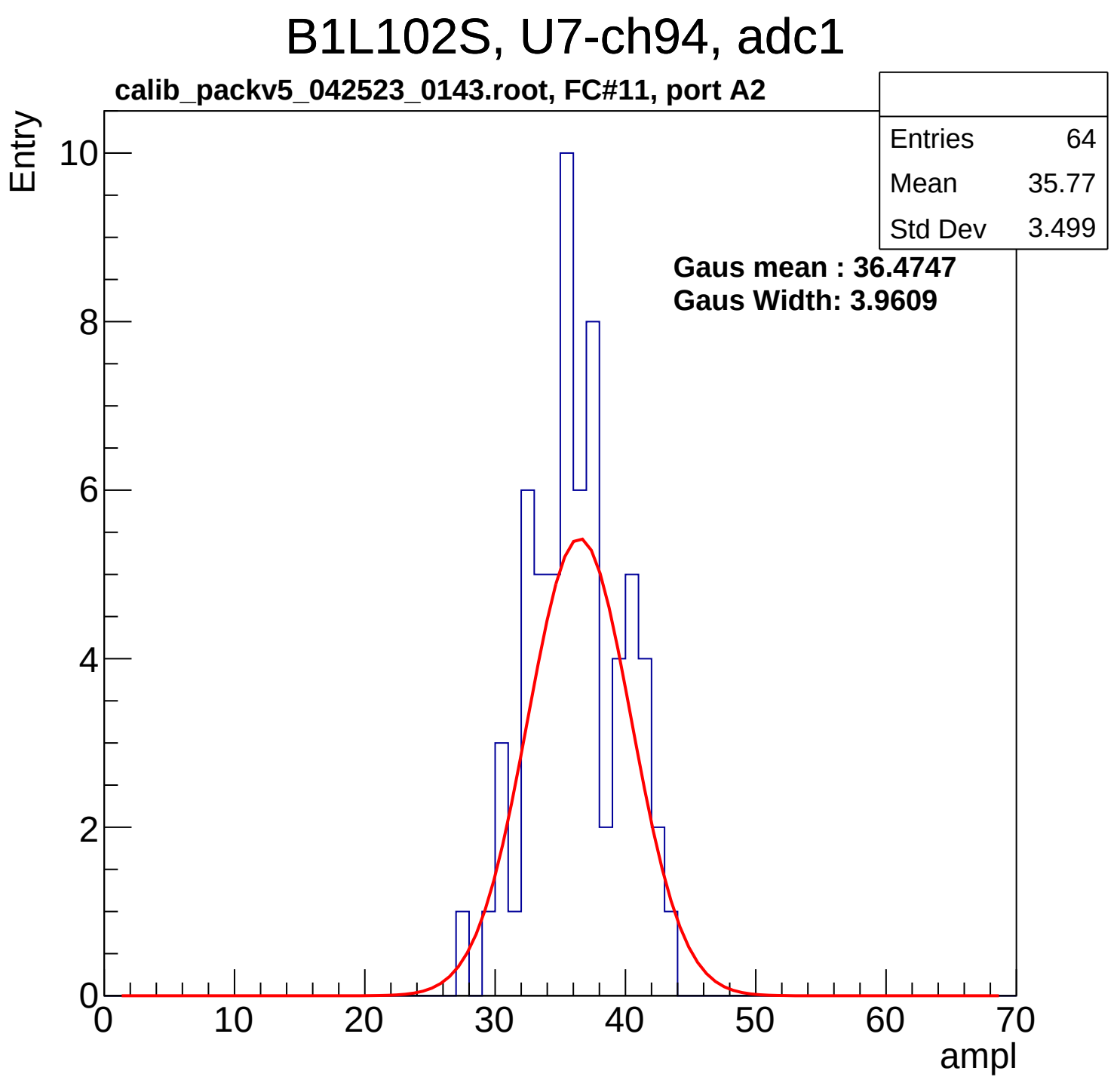
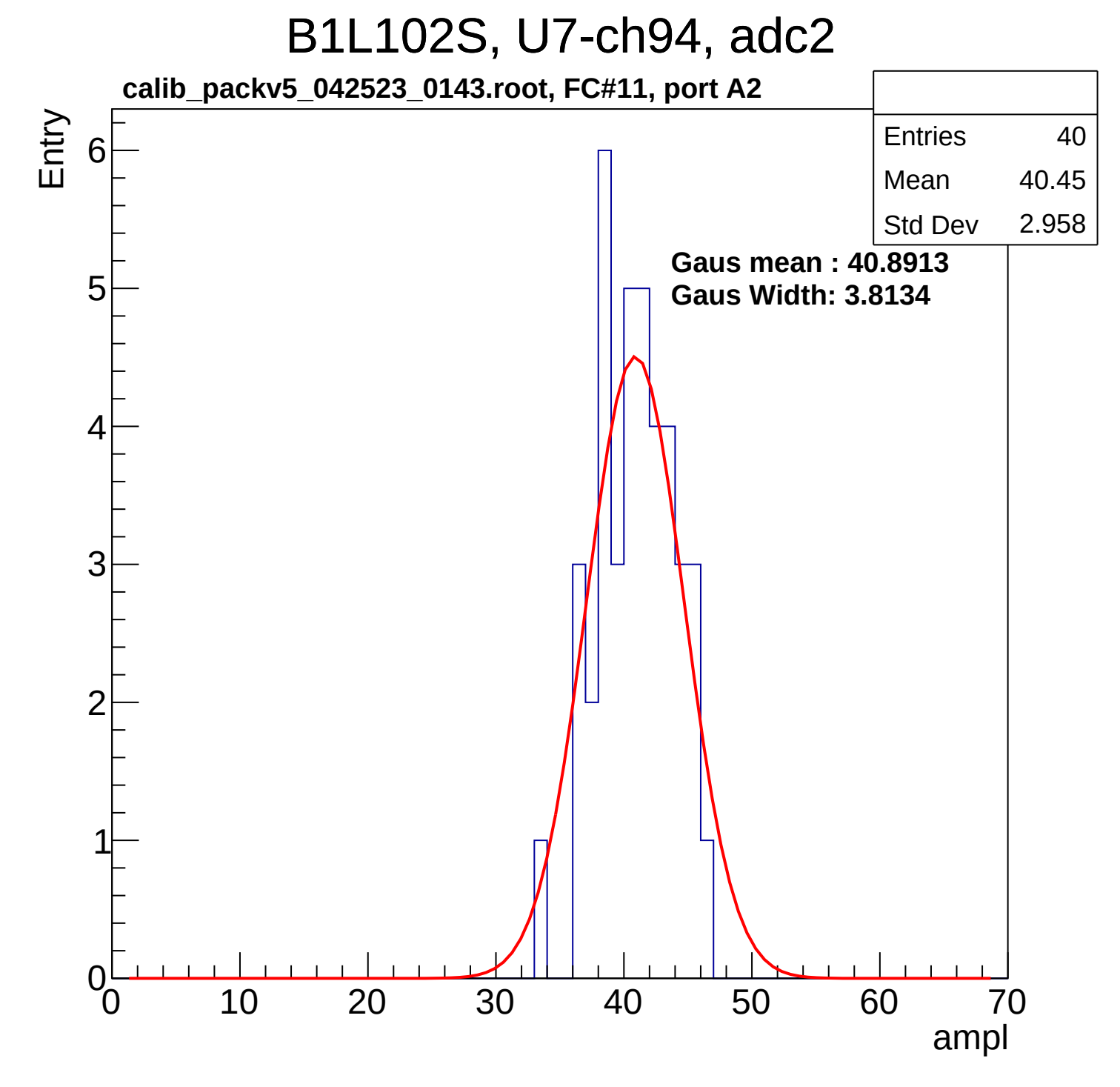
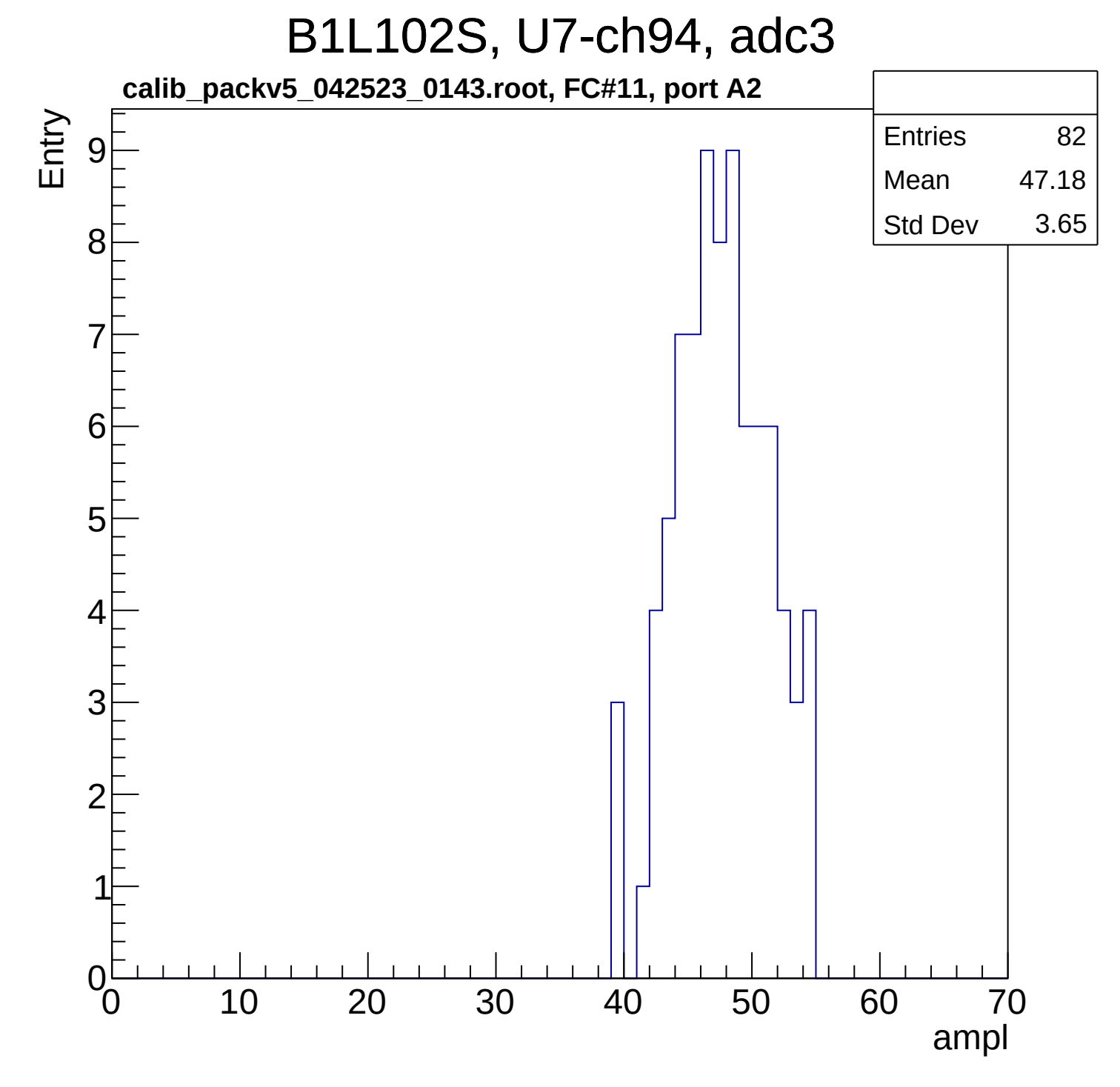

B1L102S, U7-ch93, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 4
Mean 46.75
Std Dev 27
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L102S, U7-ch93, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 1
Mean 62
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U7-ch94, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 80
Mean 27.99
Std Dev 4.854
Gaus mean : 29.0702
Gaus Width: 4.1147
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L102S, U7-ch94, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 64
Mean 35.77
Std Dev 3.499
Gaus mean : 36.4747
Gaus Width: 3.9609
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L102S, U7-ch94, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 40
Mean 40.45
Std Dev 2.958
Gaus mean : 40.8913
Gaus Width: 3.8134
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L102S, U7-ch94, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 82
Mean 47.18
Std Dev 3.65
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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40
50
60
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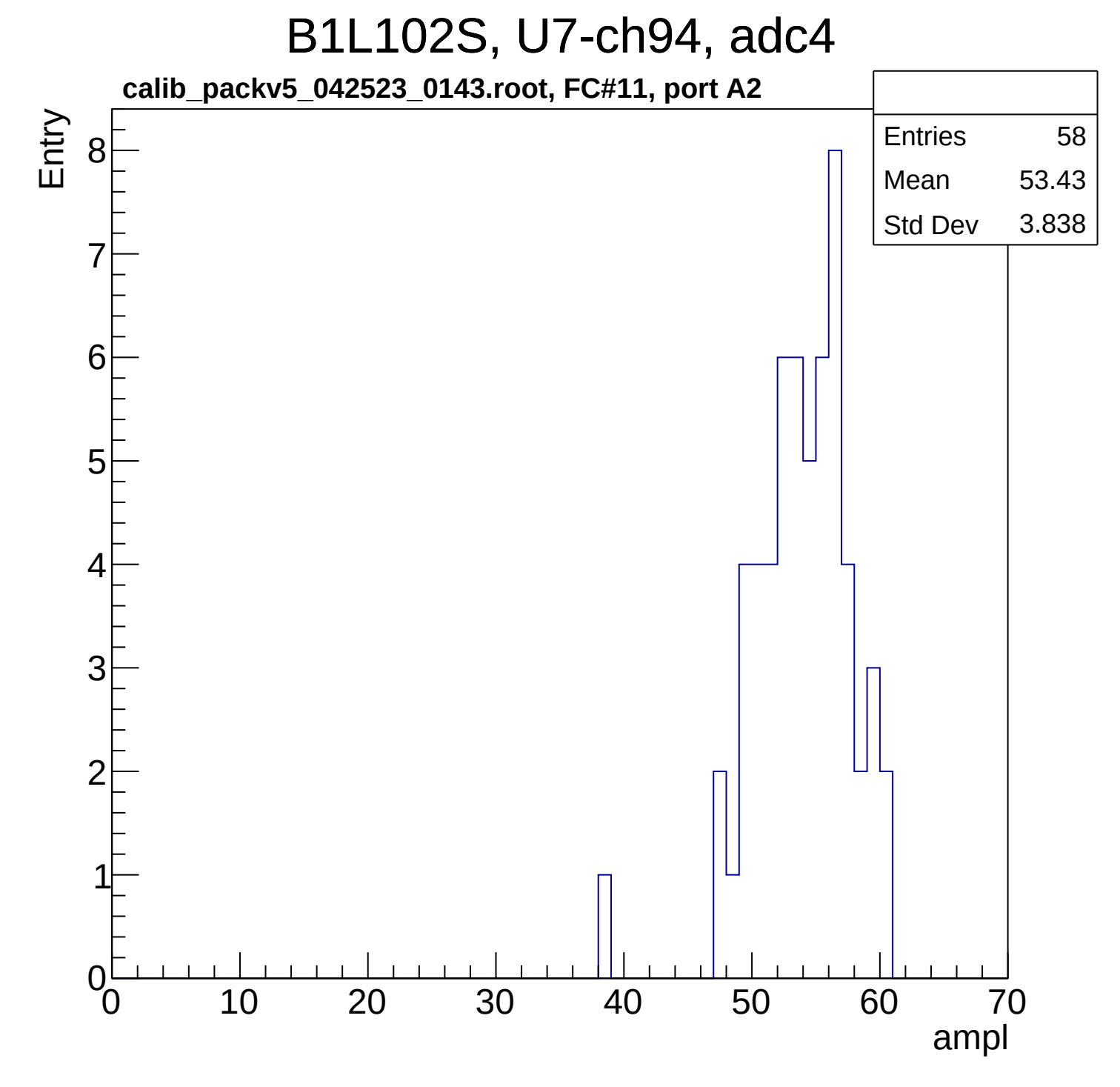
B1L102S, U7-ch94, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 58
Mean 53.43
Std Dev 3.838
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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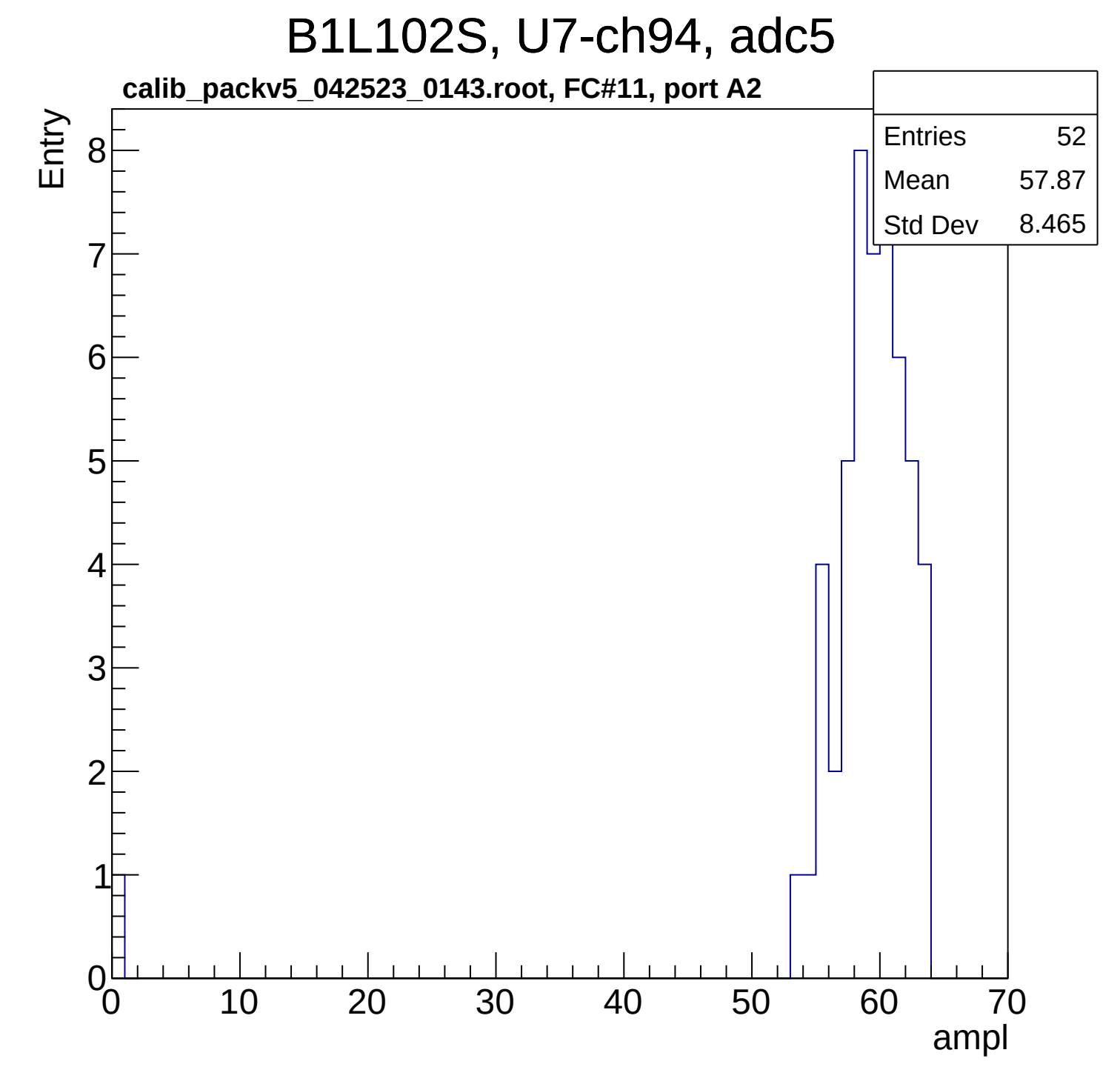
40
50
60
70


B1L102S, U7-ch94, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 52
Mean 57.87
Std Dev 8.465
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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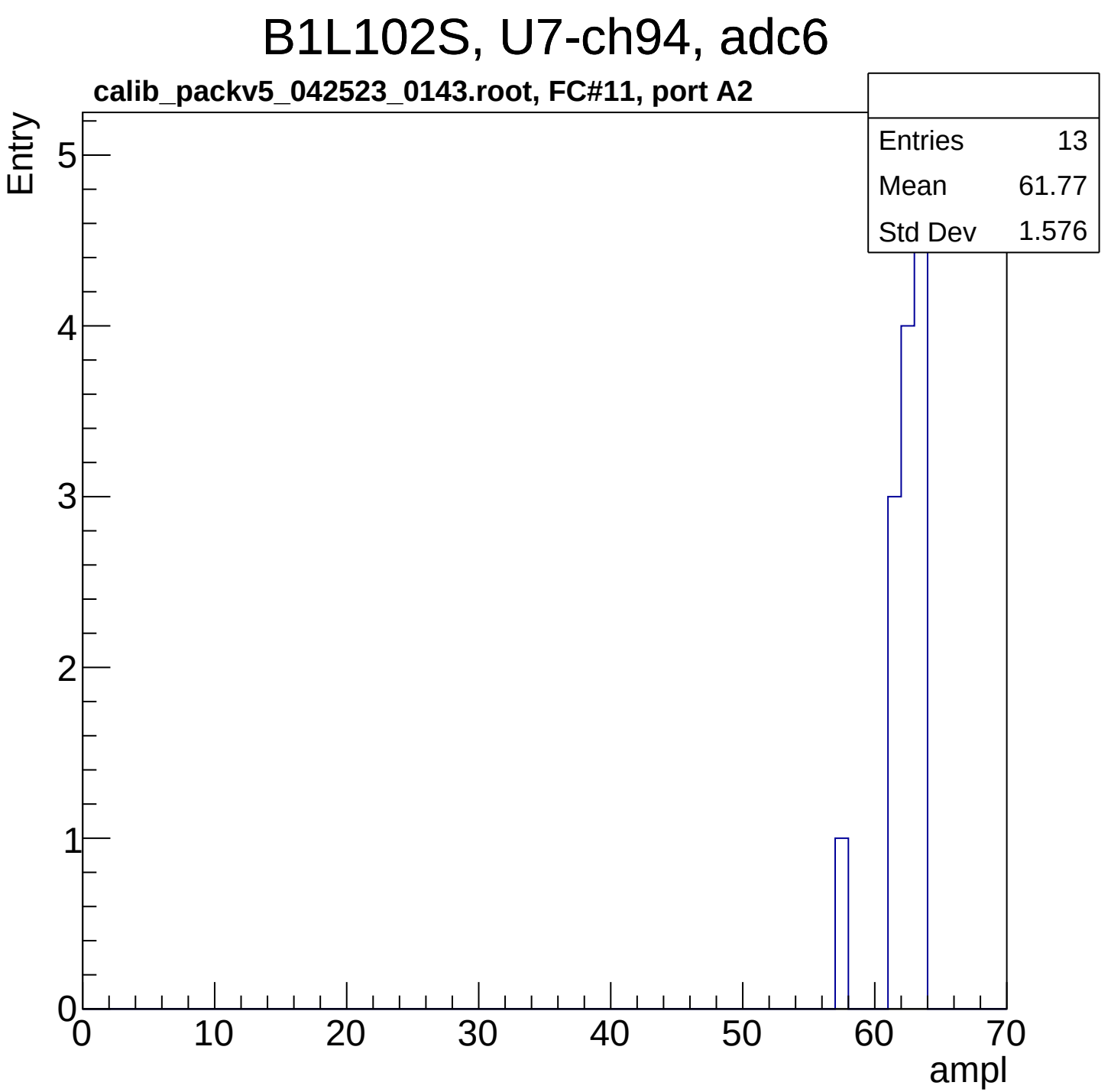
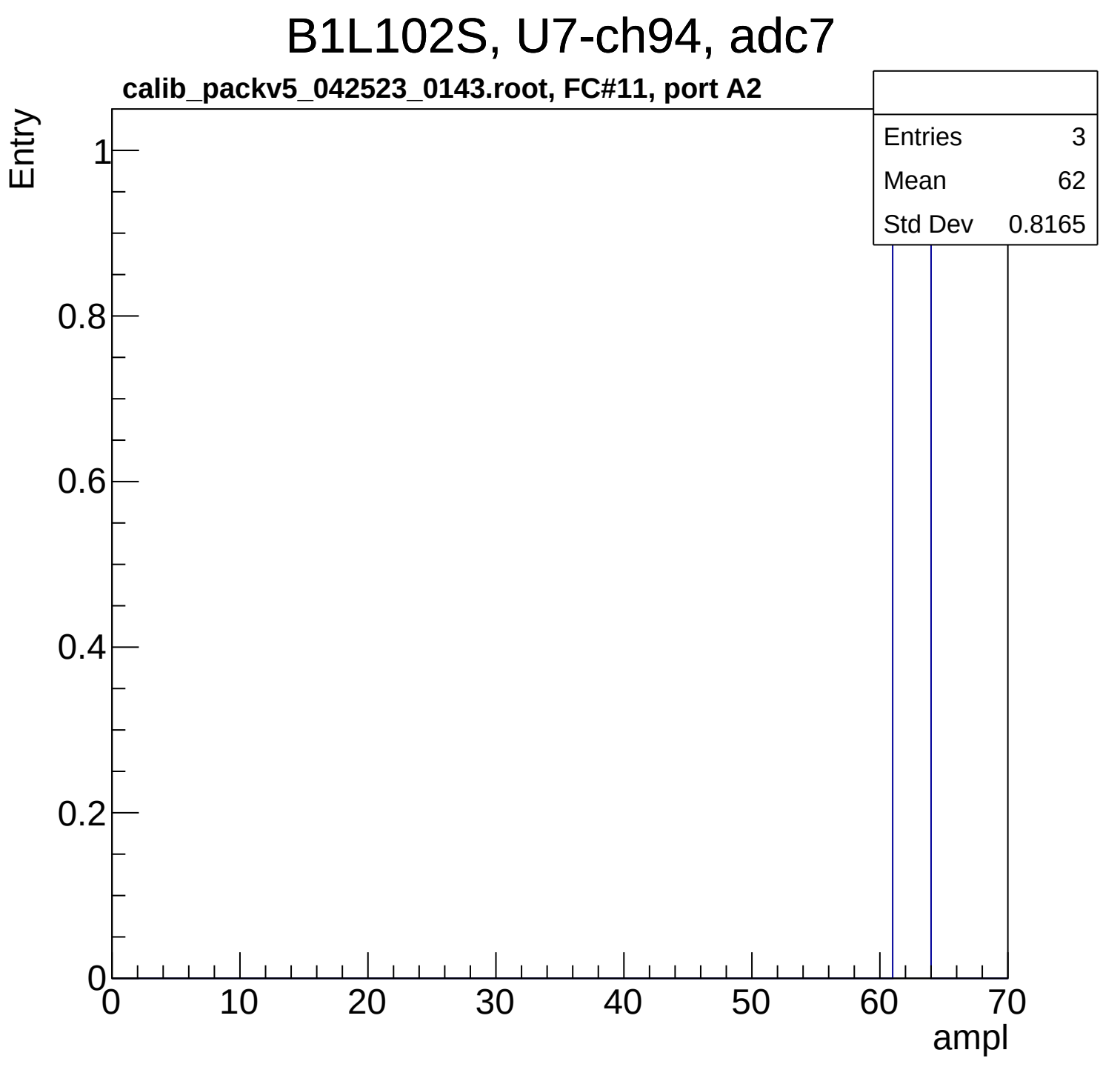
40
50
60
70


B1L102S, U7-ch94, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 13
Mean 61.77
Std Dev 1.576
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L102S, U7-ch94, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 3
Mean 62
Std Dev 0.8165
Entry
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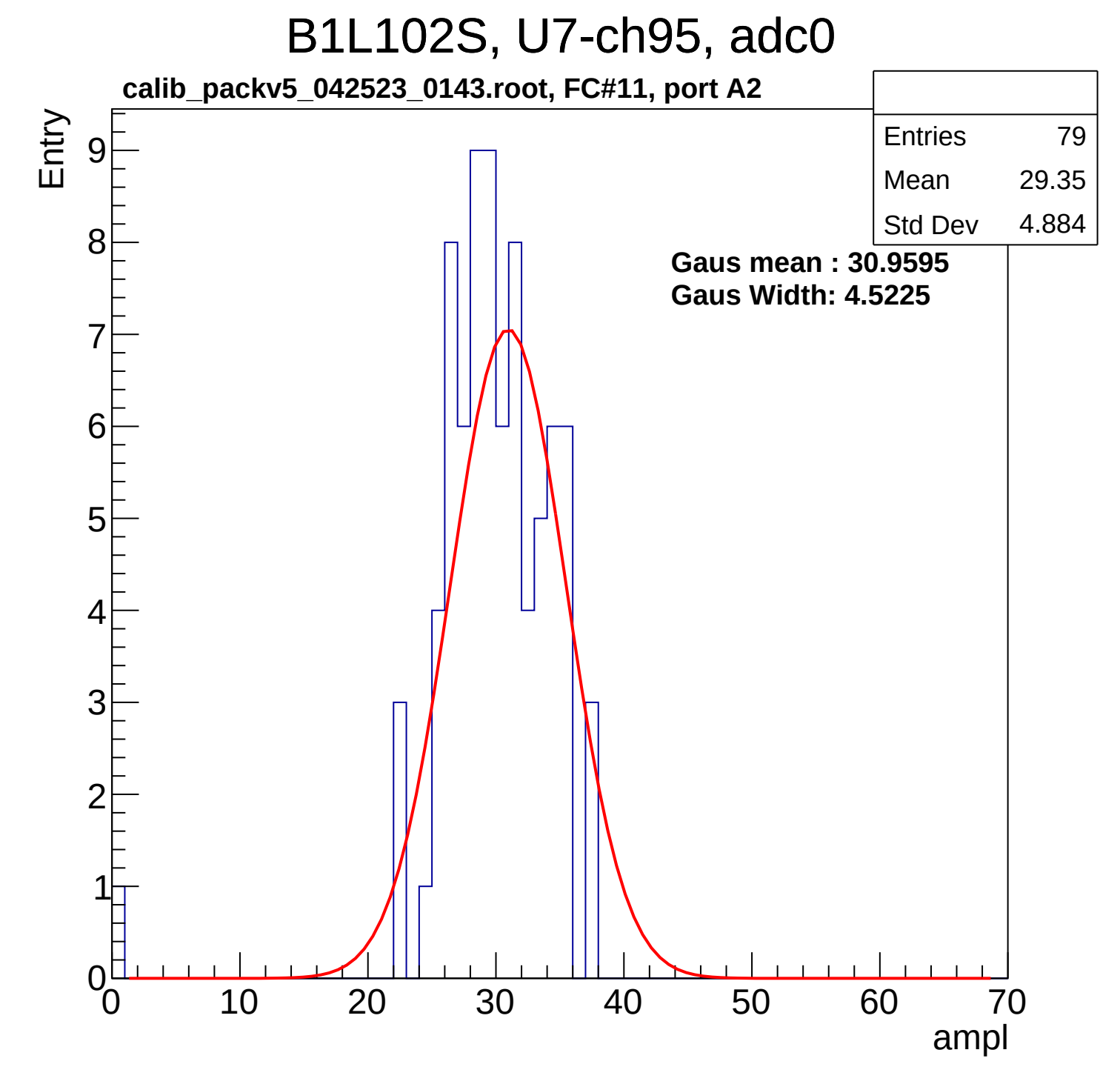
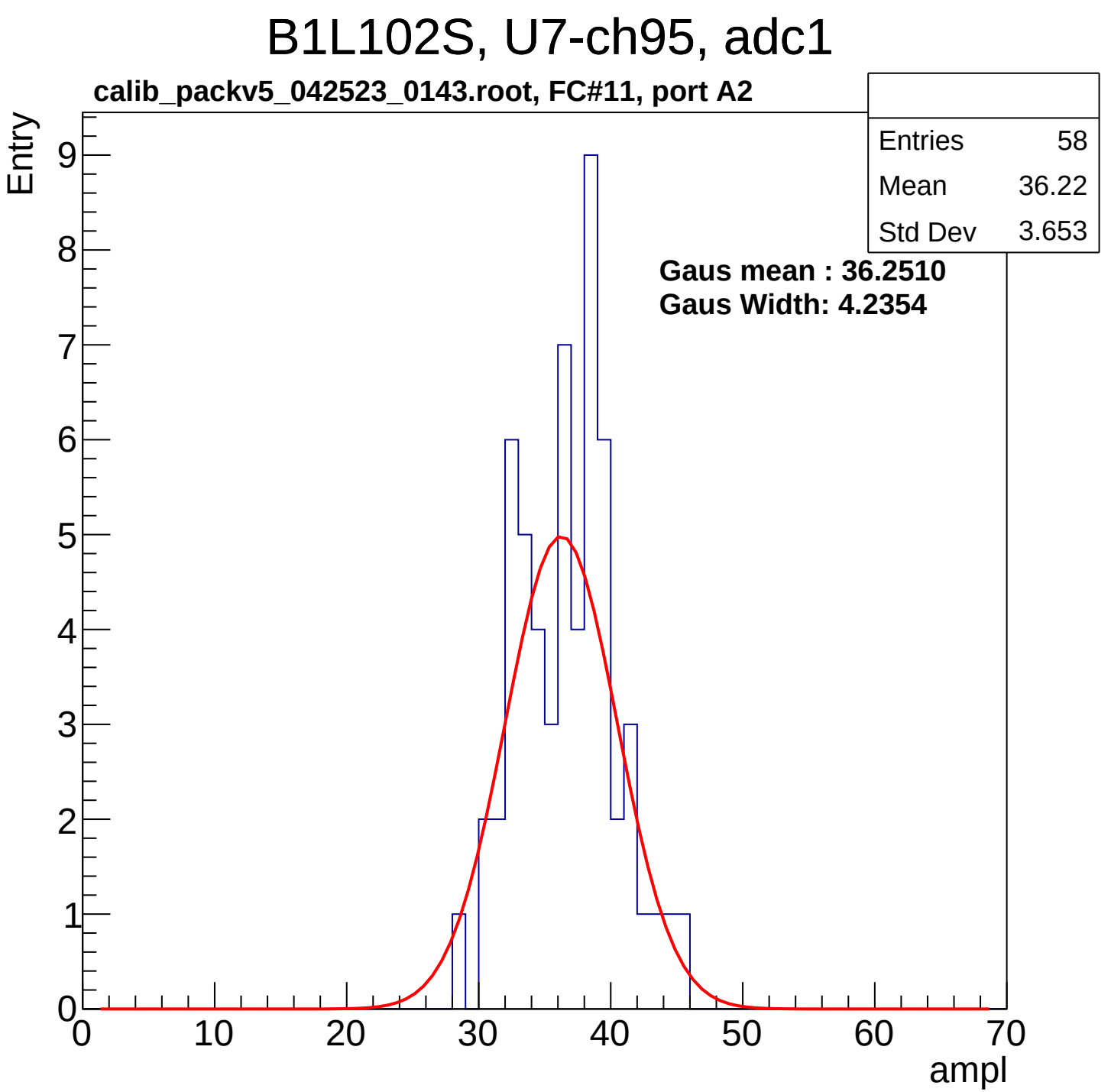
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U7-ch95, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 79
Mean 29.35
Std Dev 4.884
Gaus mean : 30.9595
Gaus Width: 4.5225
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L102S, U7-ch95, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 58
Mean 36.22
Std Dev 3.653
Gaus mean : 36.2510
Gaus Width: 4.2354
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
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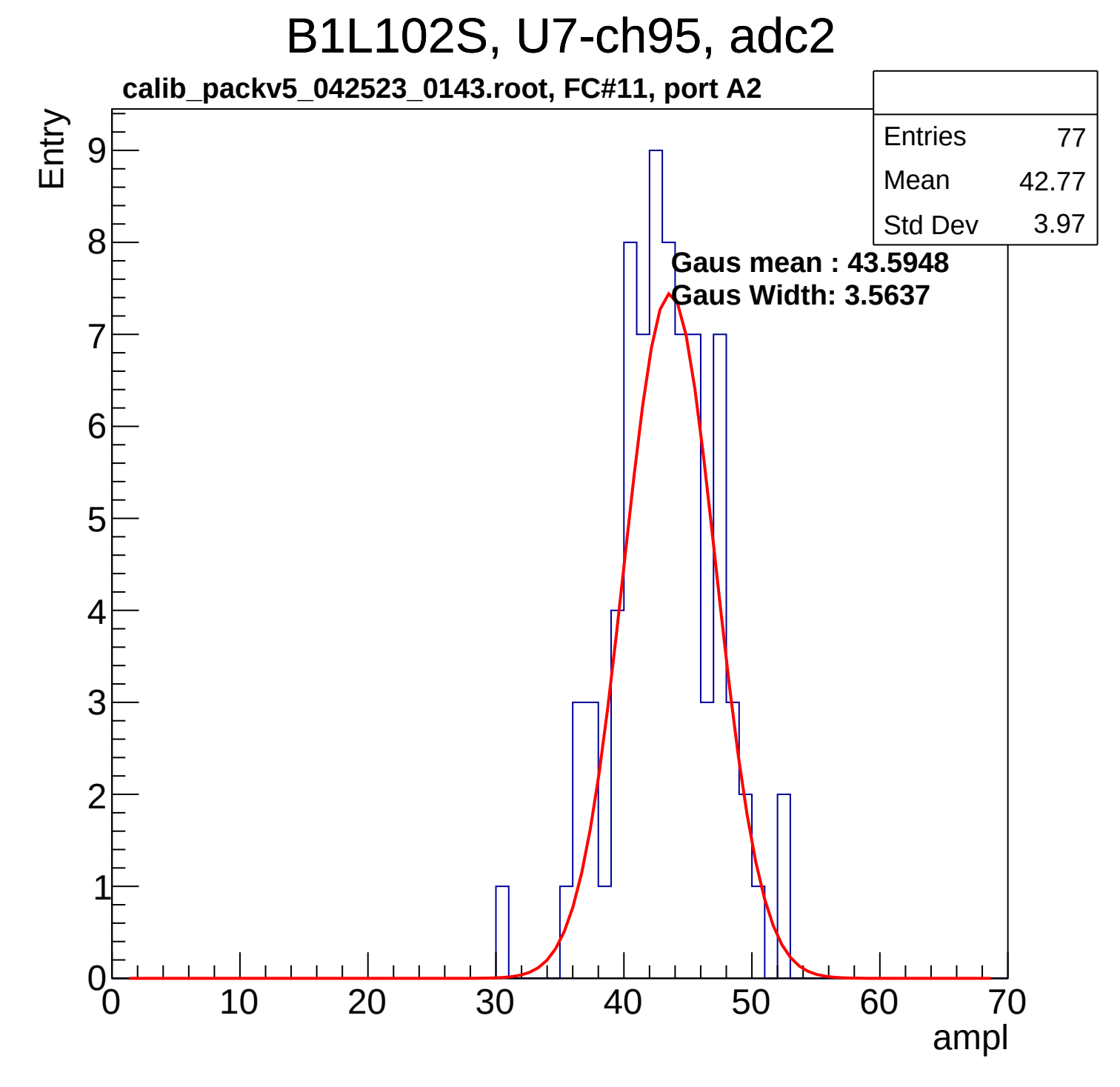
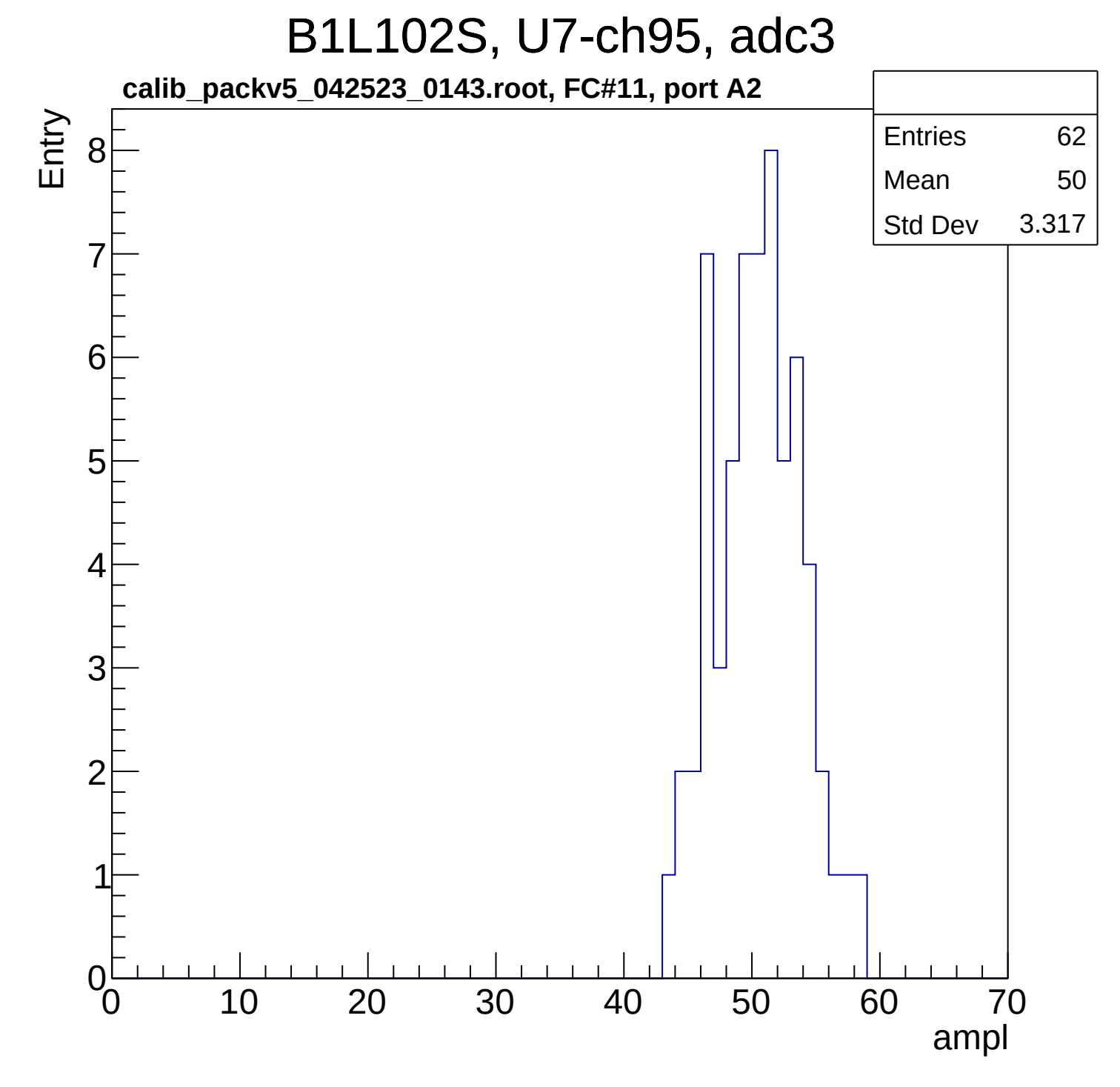
20
30
40
50
60
70


B1L102S, U7-ch95, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 77
Mean 42.77
Std Dev 3.97
Gaus mean : 43.5948
Gaus Width: 3.5637
Entry
ampl
0
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9


B1L102S, U7-ch95, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 62
Mean 50
Std Dev 3.317
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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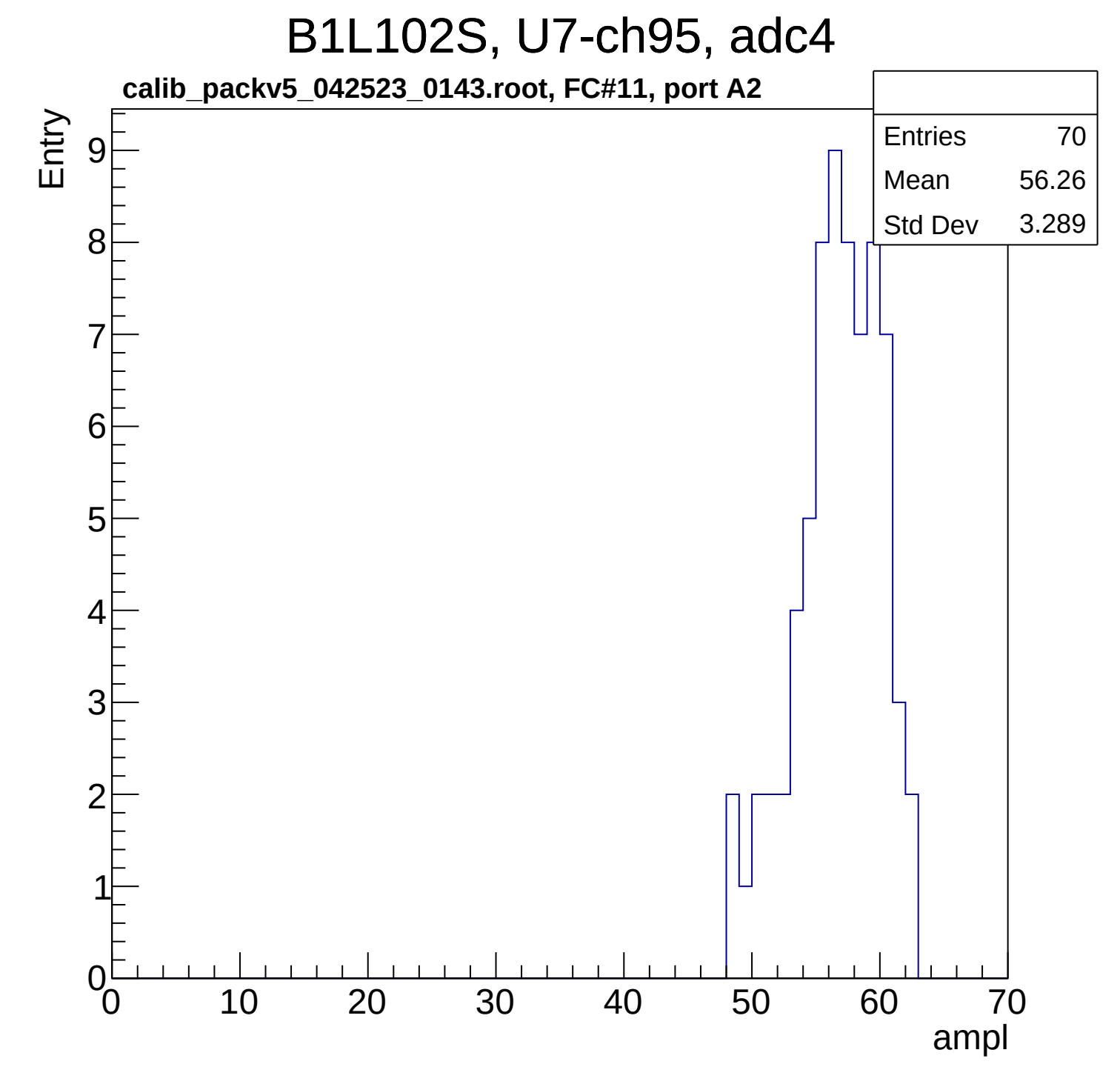
40
50
60
70


B1L102S, U7-ch95, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 70
Mean 56.26
Std Dev 3.289
Entry
ampl
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3
4
5
6
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0
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40
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60
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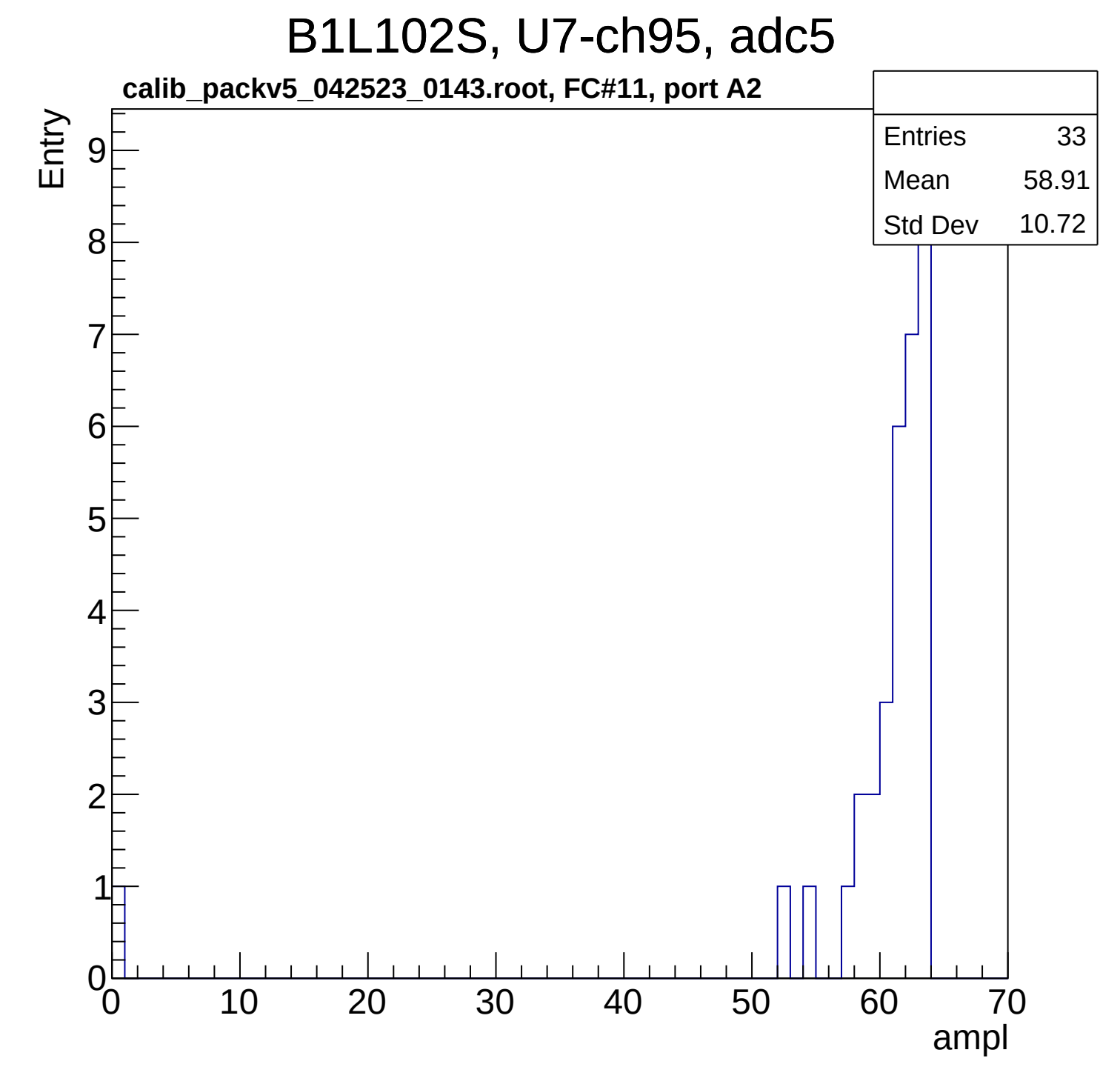
B1L102S, U7-ch95, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 33
Mean 58.91
Std Dev 10.72
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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60
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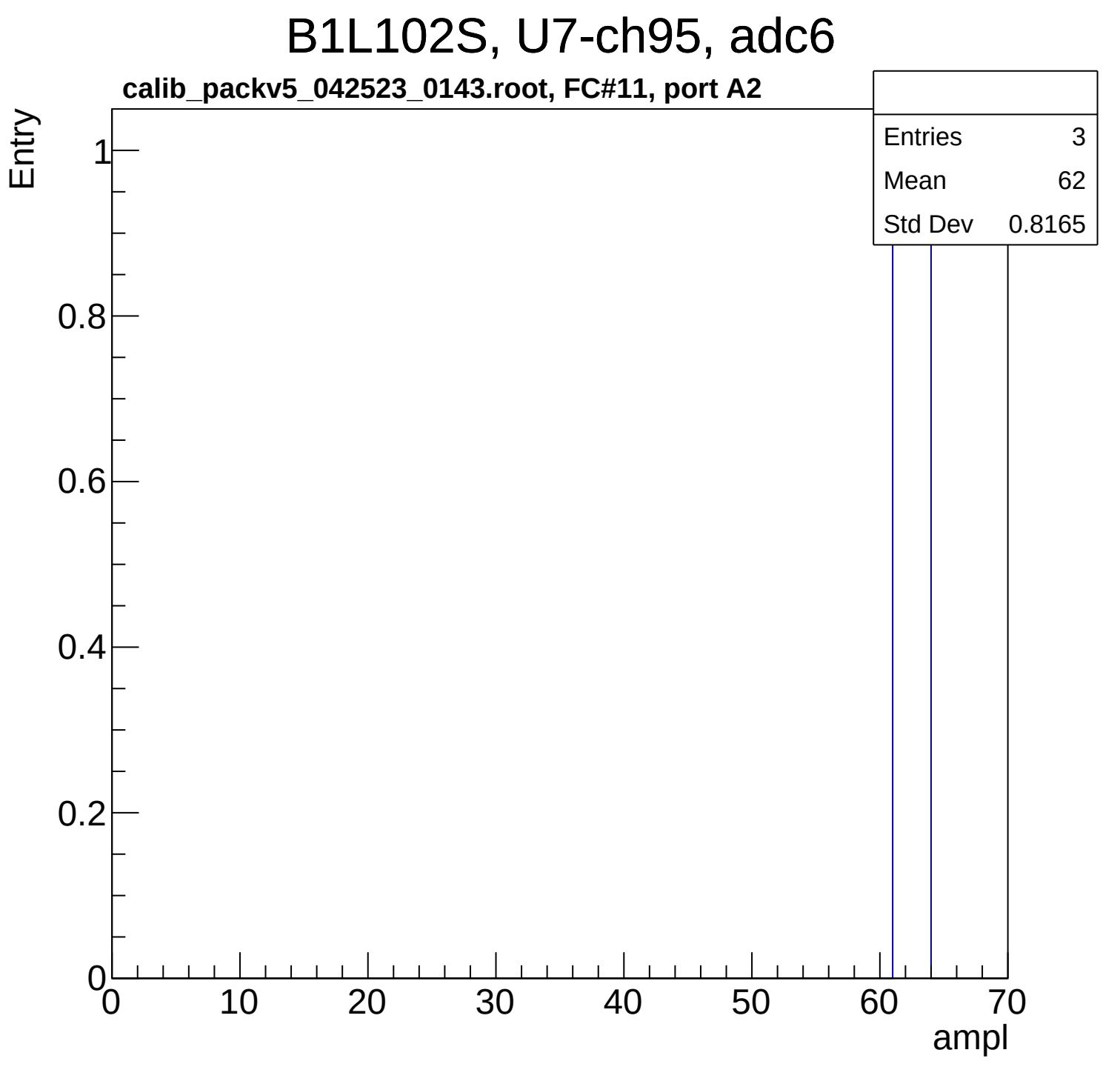
B1L102S, U7-ch95, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 3
Mean 62
Std Dev 0.8165
Entry
1
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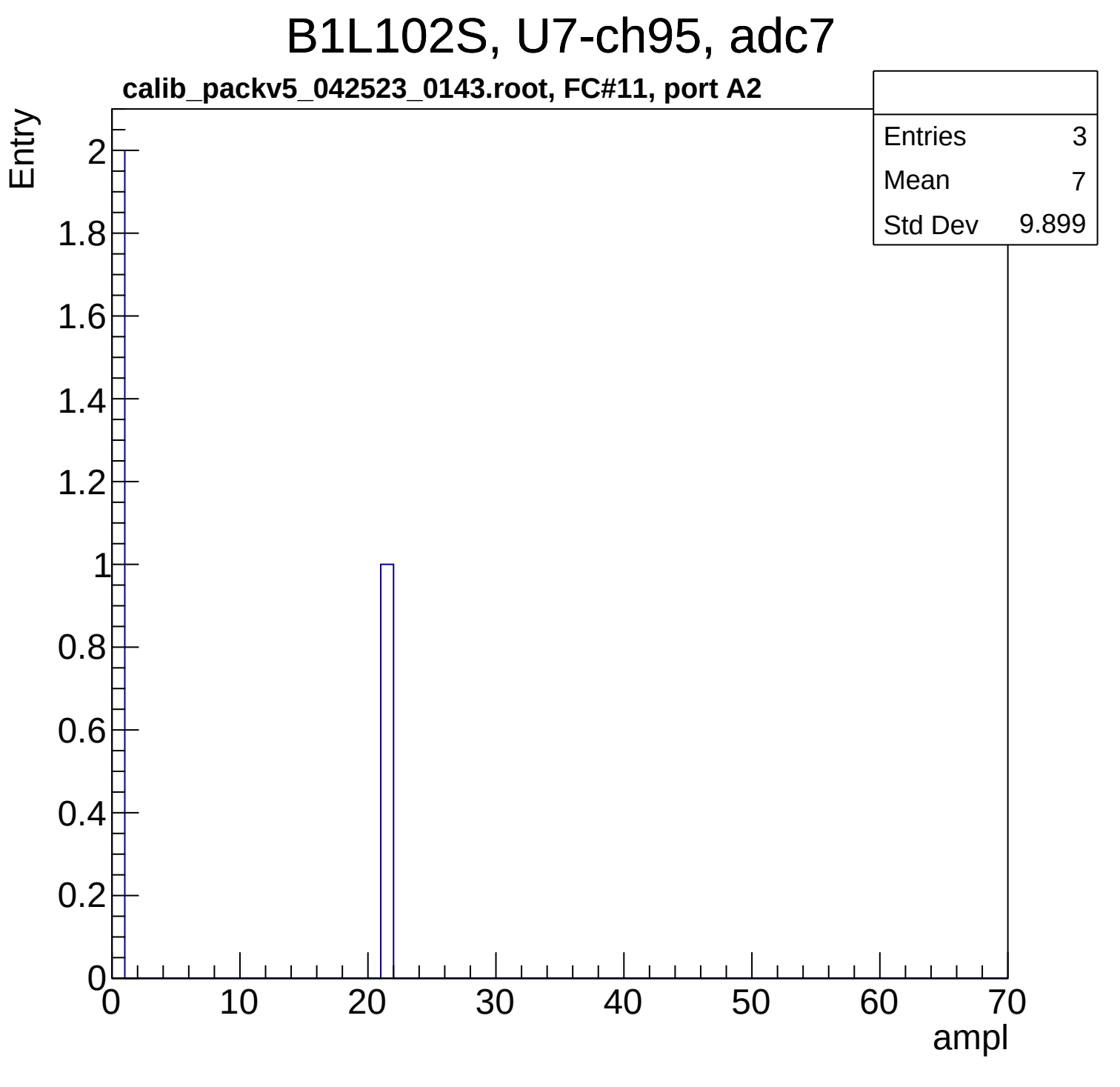
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U7-ch95, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 3
Mean 7
Std Dev 9.899
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
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40
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60
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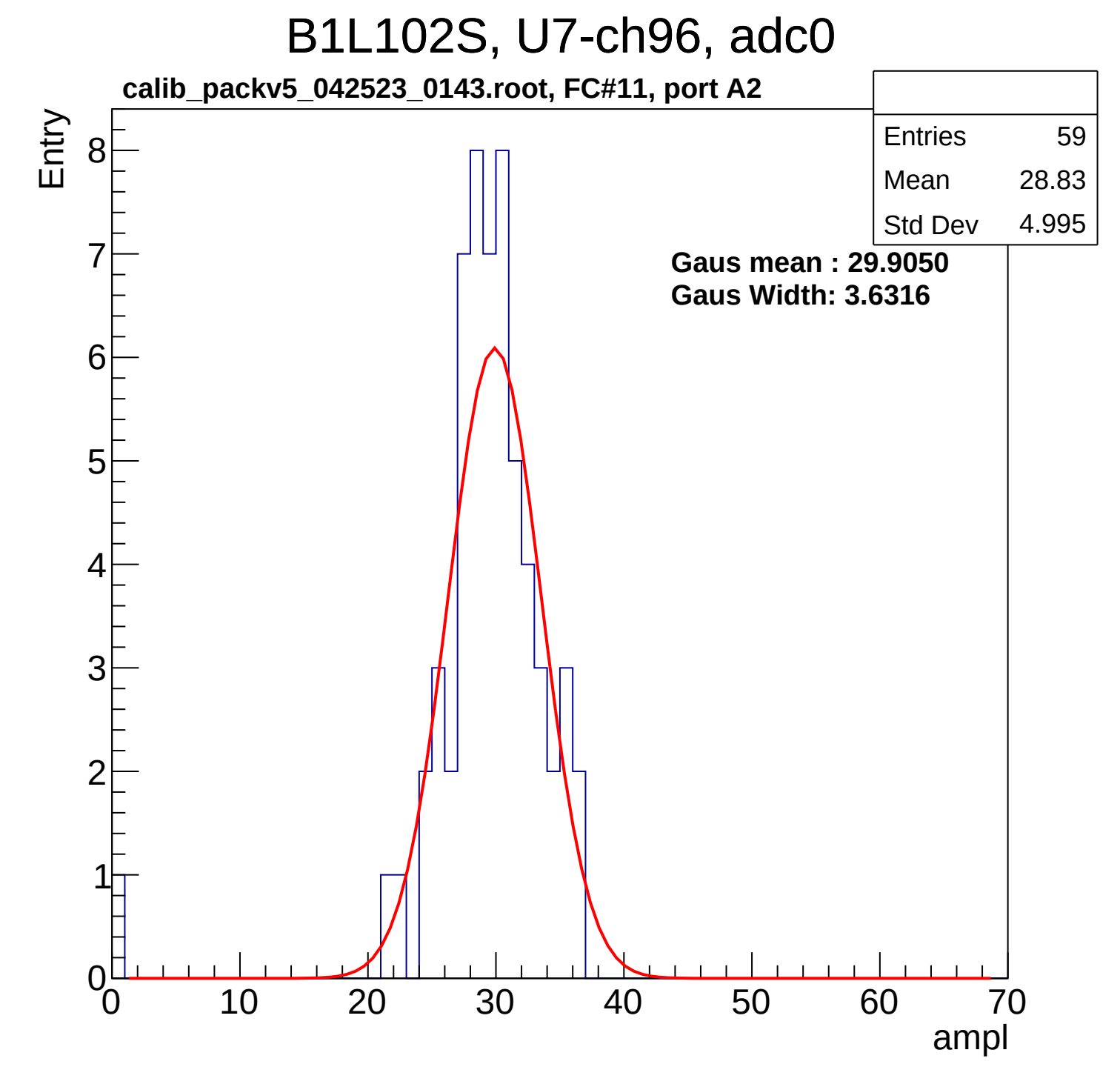
B1L102S, U7-ch96, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 59
Mean 28.83
Std Dev 4.995
Gaus mean : 29.9050
Gaus Width: 3.6316
Entry
ampl
0
1
2
3
4
5
6
7
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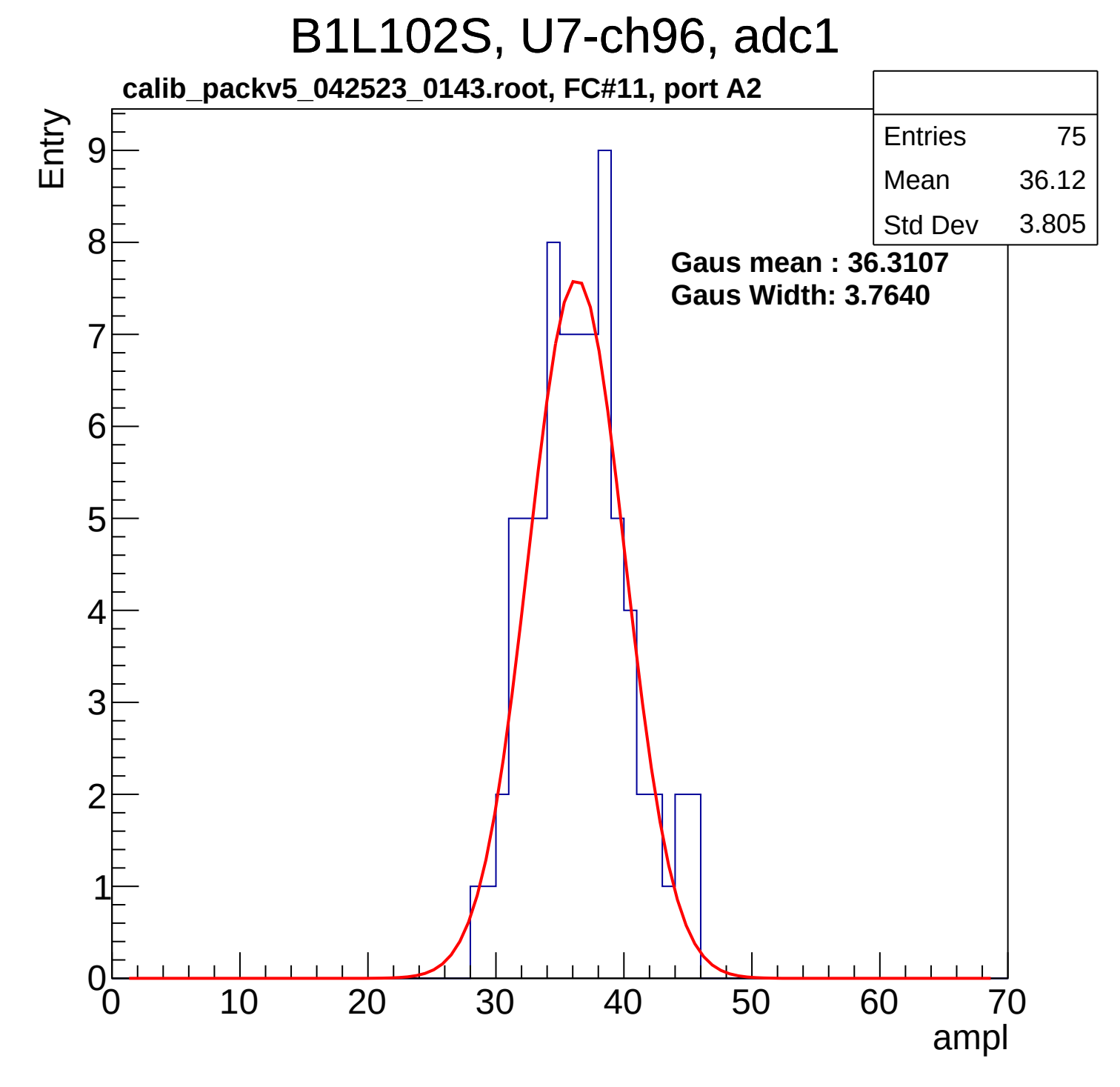
B1L102S, U7-ch96, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 75
Mean 36.12
Std Dev 3.805
Gaus mean : 36.3107
Gaus Width: 3.7640
Entry
ampl
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2
3
4
5
6
7
8
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0
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40
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60
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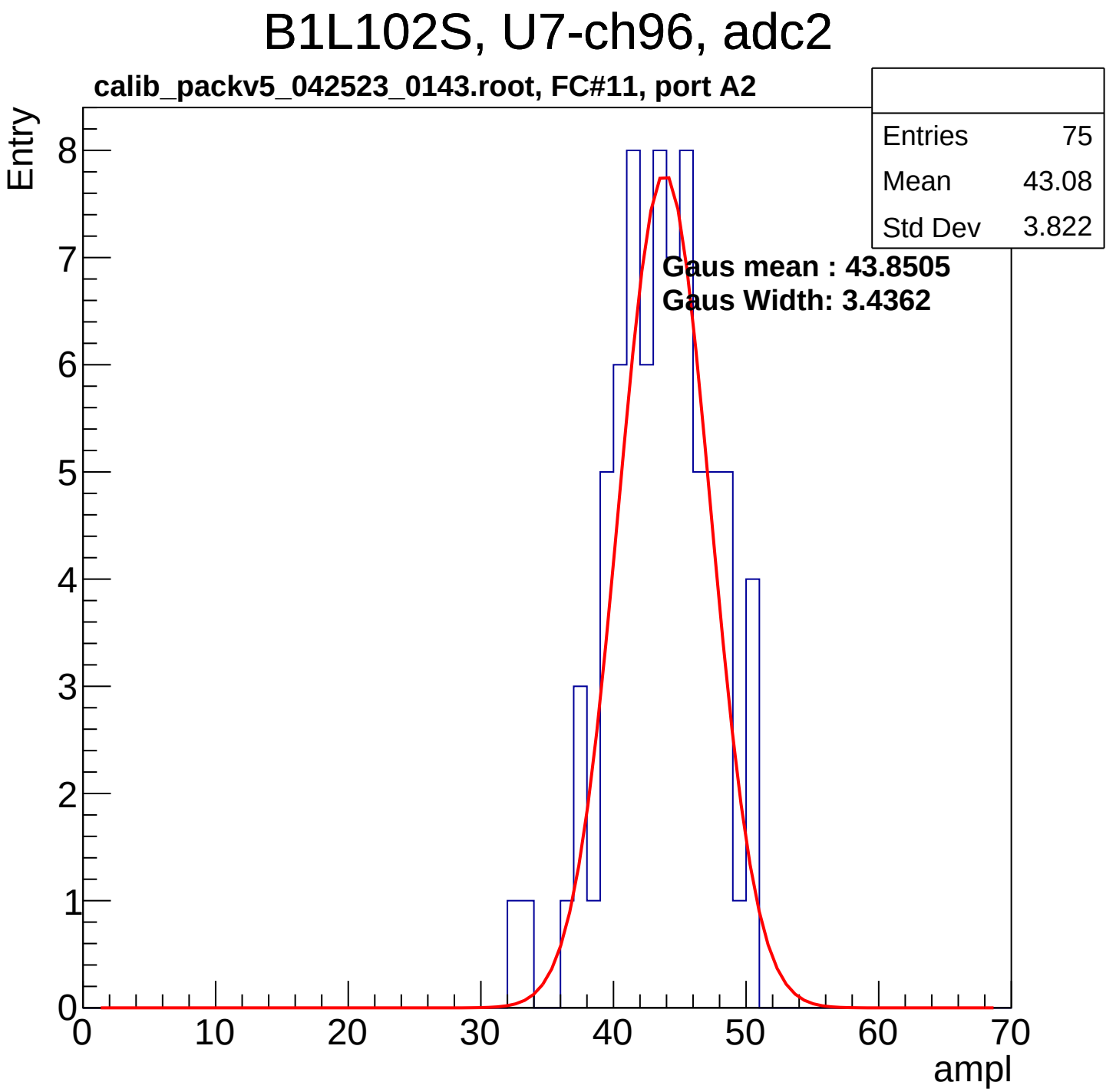
B1L102S, U7-ch96, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 75
Mean 43.08
Std Dev 3.822
Gaus mean : 43.8505
Gaus Width: 3.4362
Entry
ampl
0
1
2
3
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5
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0
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60
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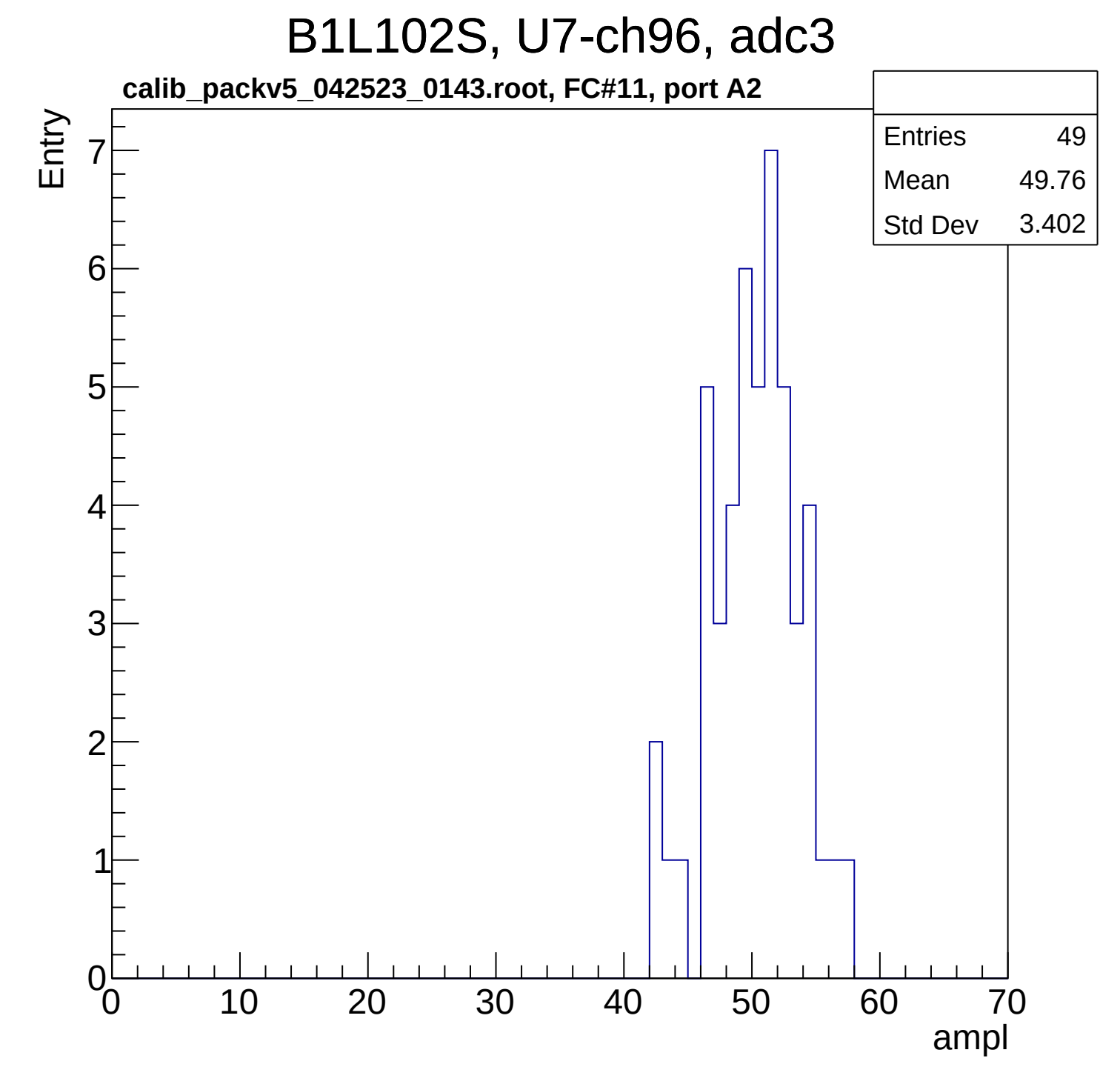
B1L102S, U7-ch96, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 49
Mean 49.76
Std Dev 3.402
Entry
ampl
0
1
2
3
4
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6
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0
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40
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60
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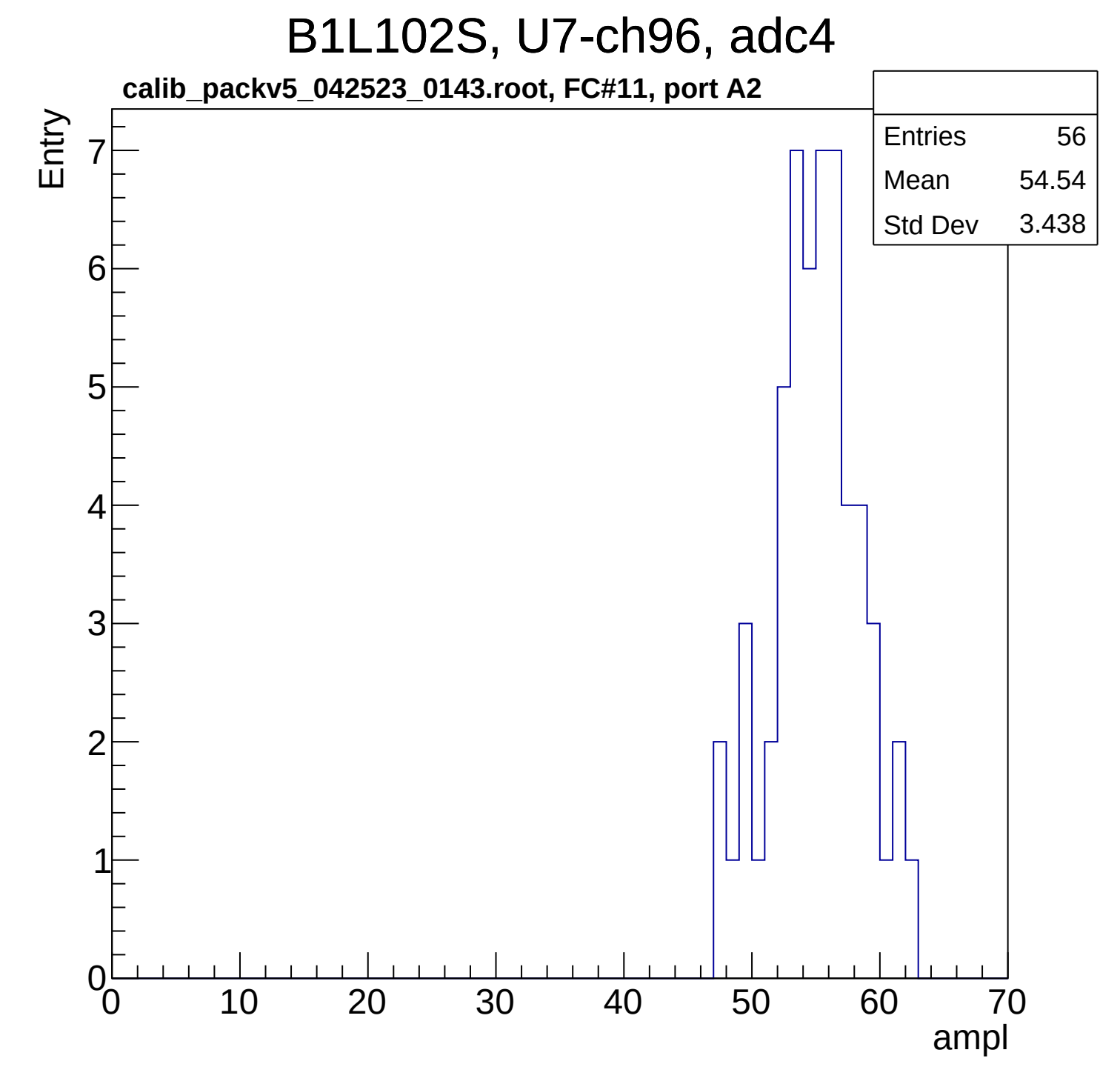
B1L102S, U7-ch96, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 56
Mean 54.54
Std Dev 3.438
Entry
ampl
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1
2
3
4
5
6
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0
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60
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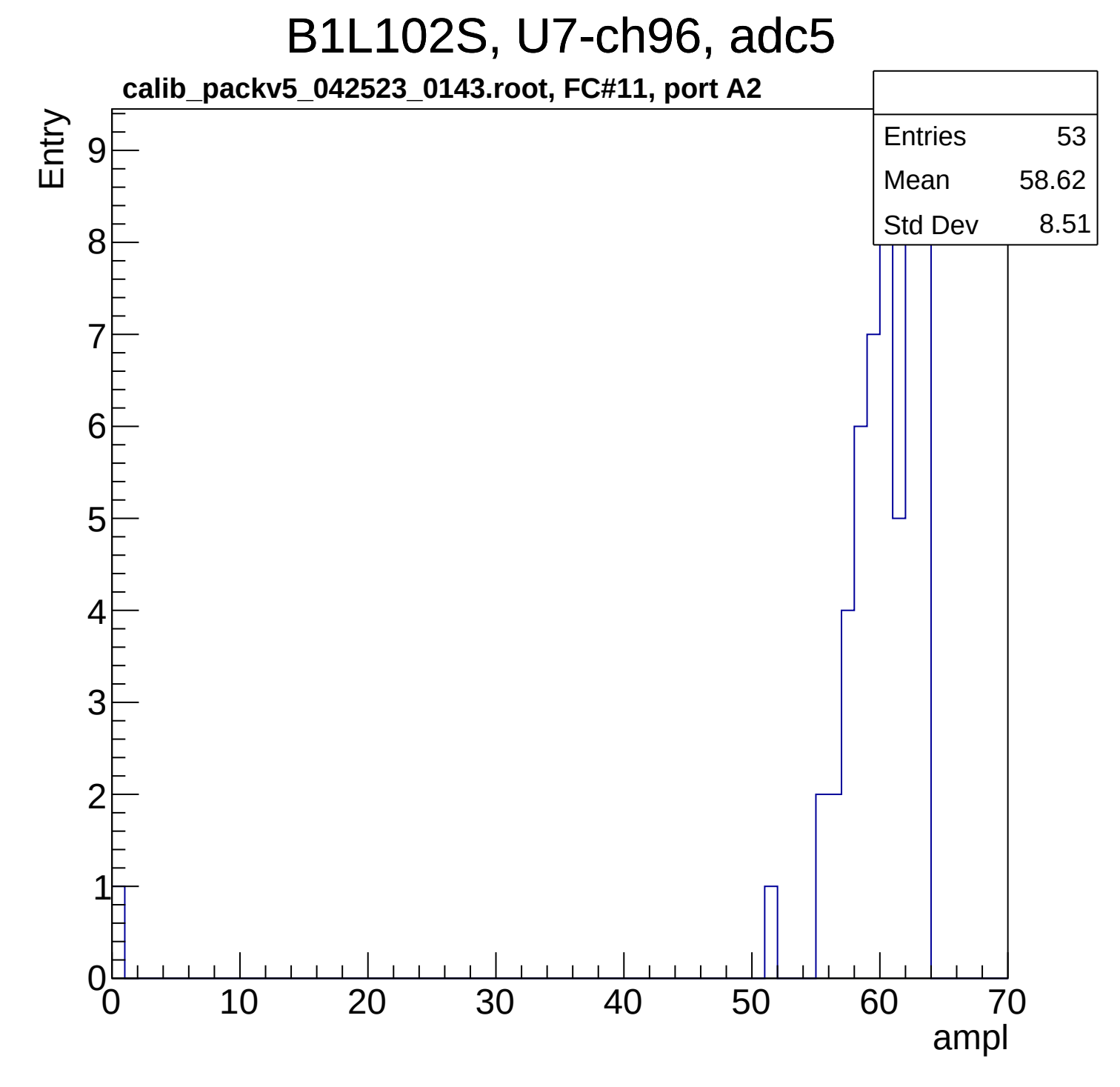
B1L102S, U7-ch96, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 53
Mean 58.62
Std Dev 8.51
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
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60
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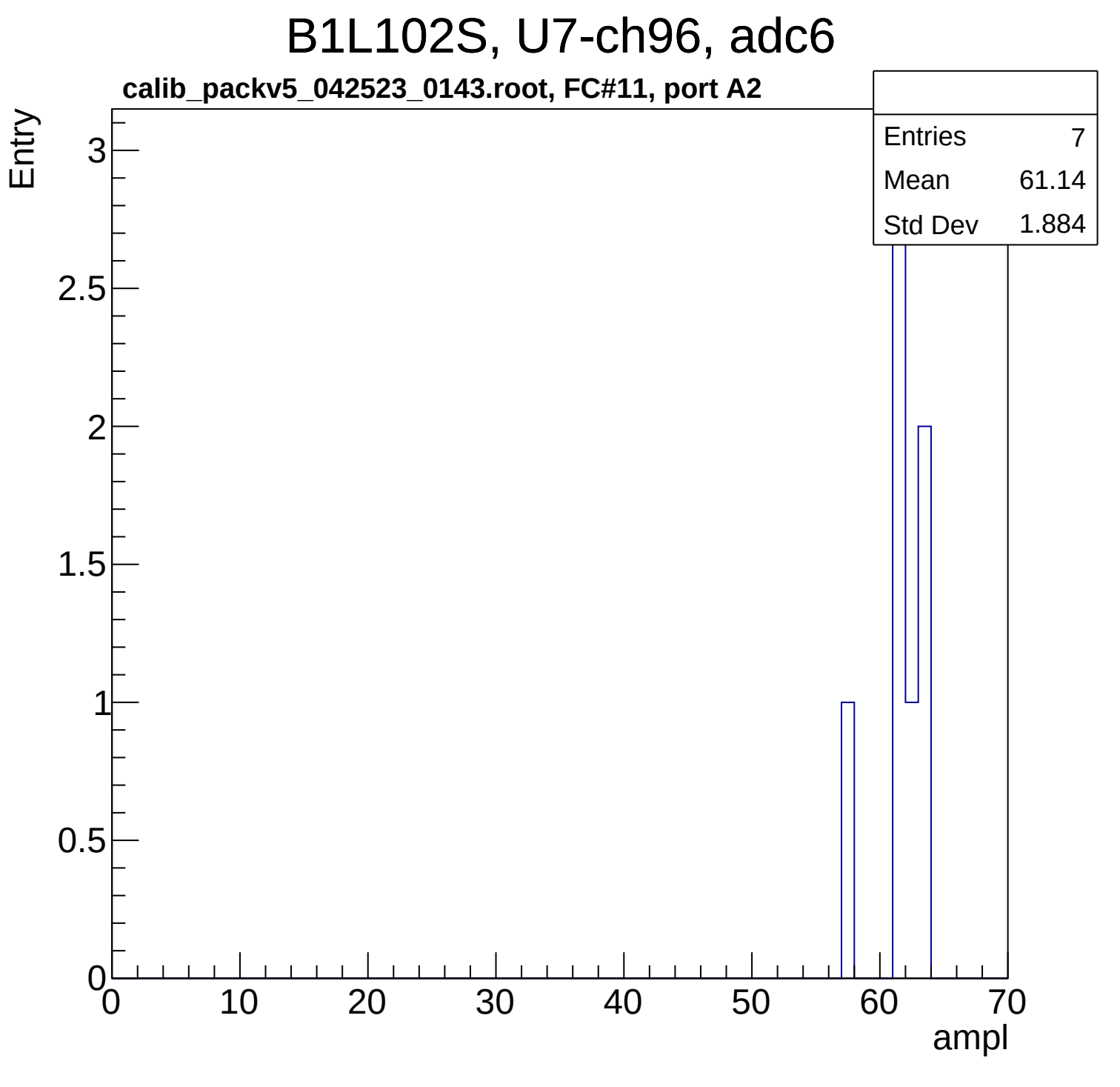
B1L102S, U7-ch96, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 7
Mean 61.14
Std Dev 1.884
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
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20
30
40
50
60
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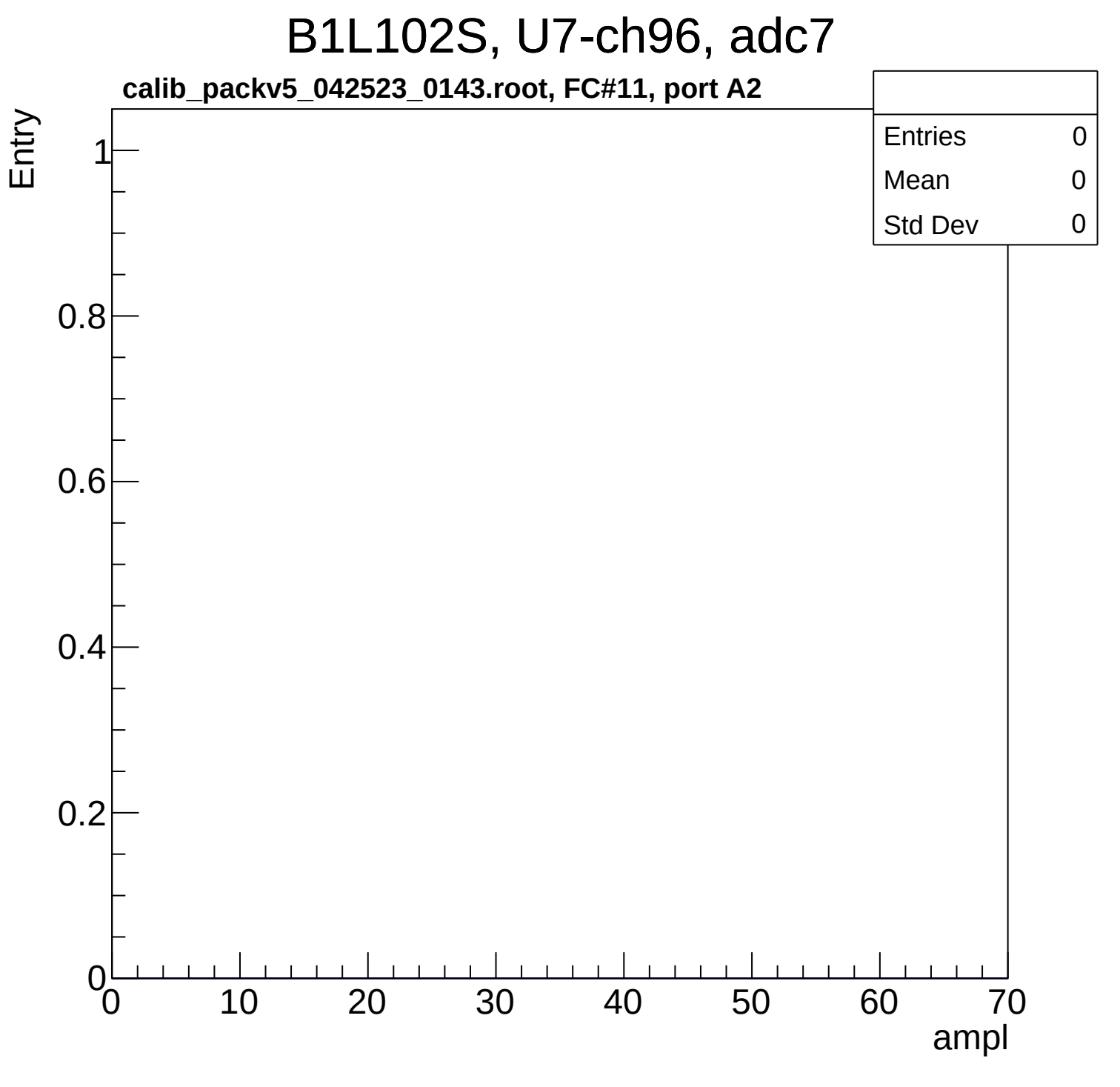
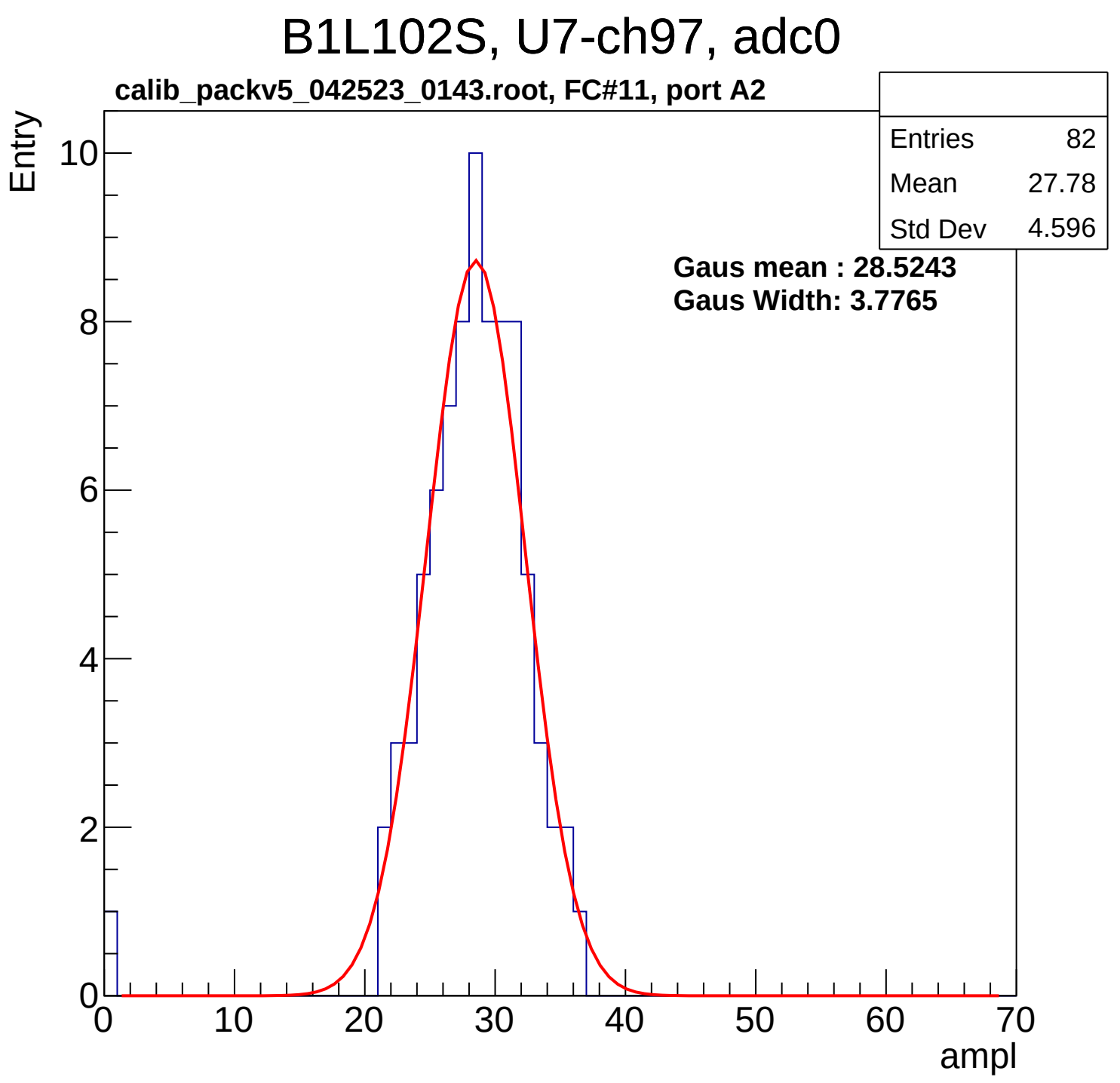

B1L102S, U7-ch96, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U7-ch97, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 82
Mean 27.78
Std Dev 4.596
Gaus mean : 28.5243
Gaus Width: 3.7765
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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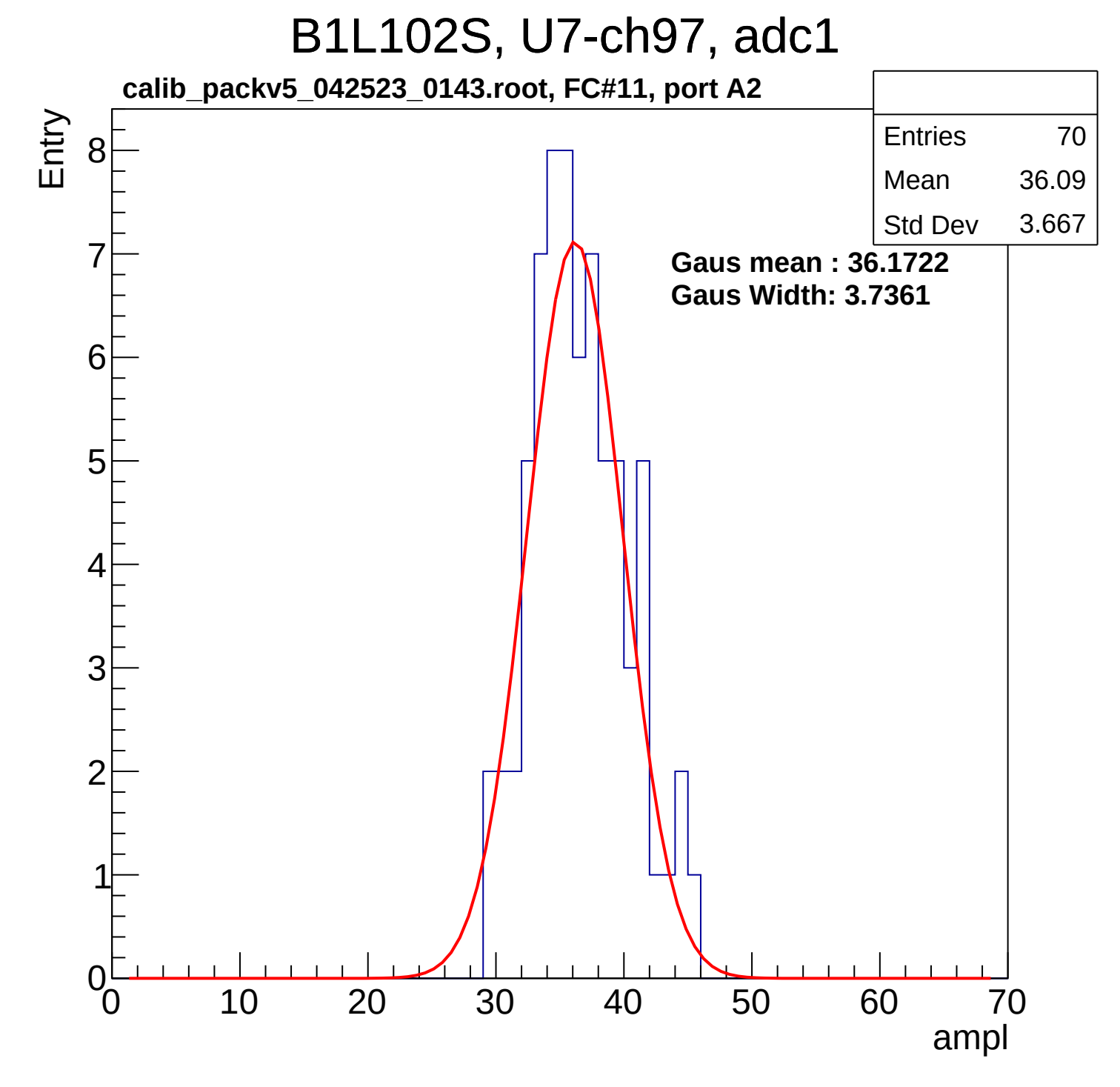
B1L102S, U7-ch97, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 70
Mean 36.09
Std Dev 3.667
Gaus mean : 36.1722
Gaus Width: 3.7361
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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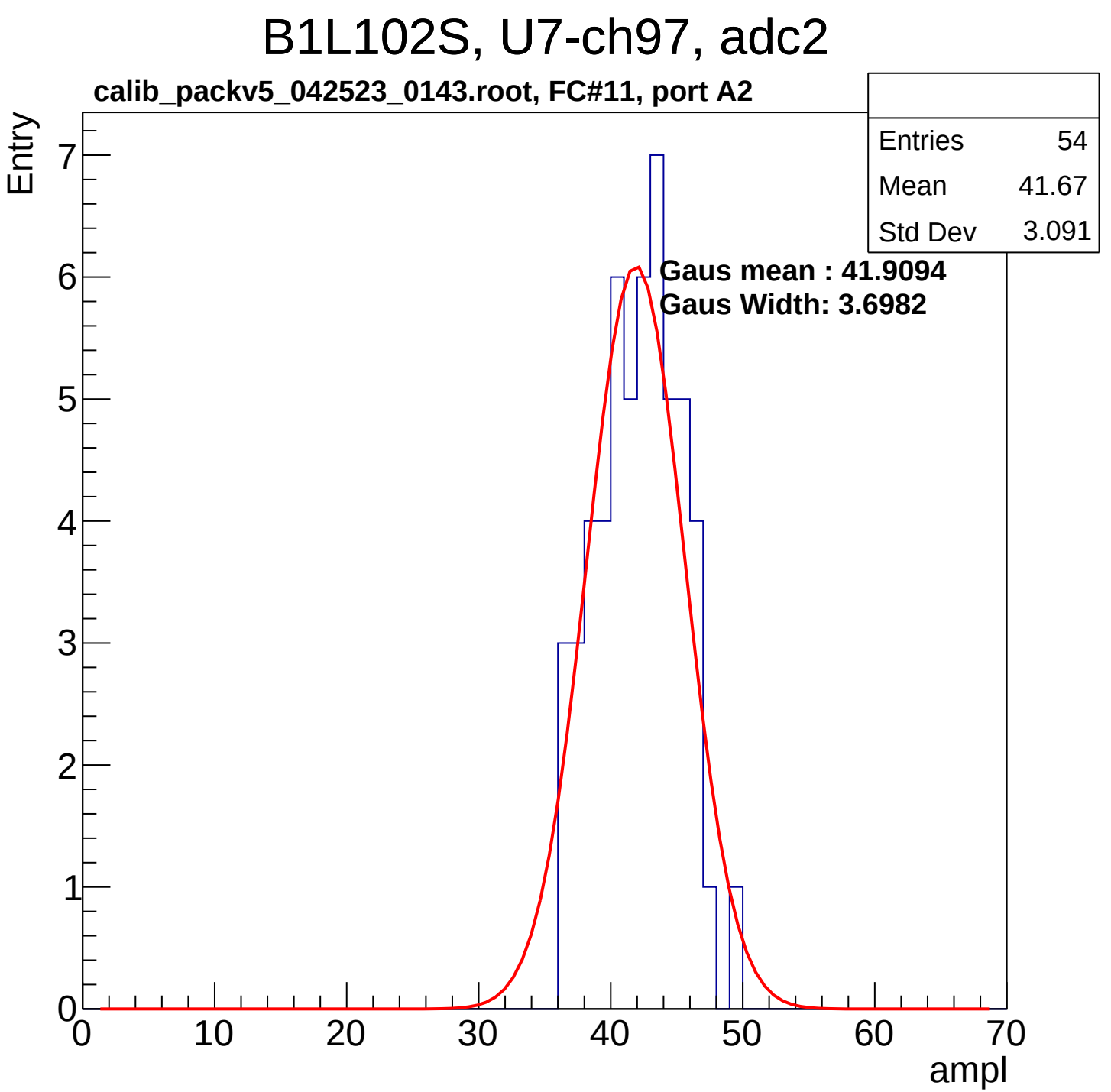
B1L102S, U7-ch97, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 54
Mean 41.67
Std Dev 3.091
Gaus mean : 41.9094
Gaus Width: 3.6982
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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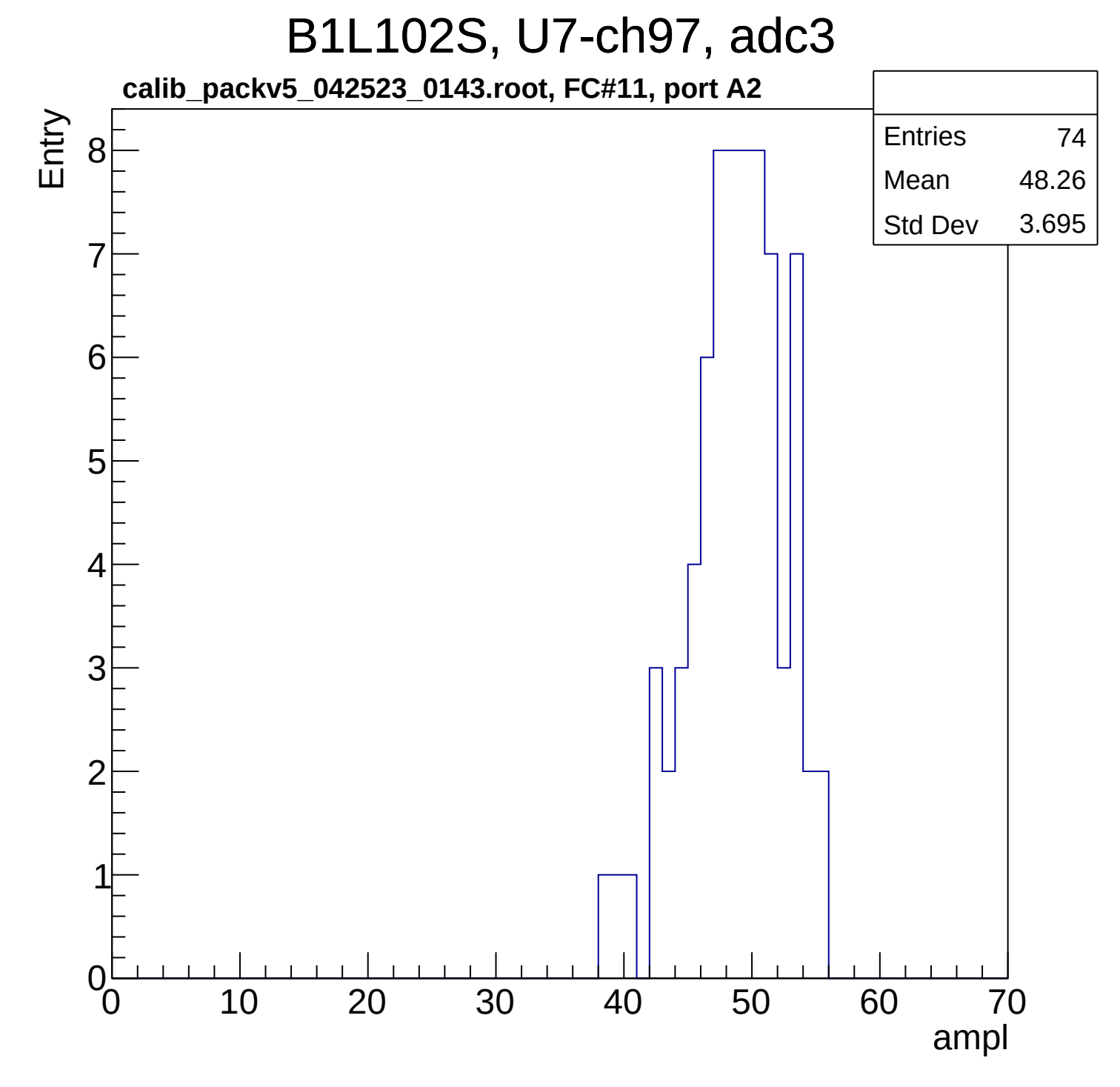
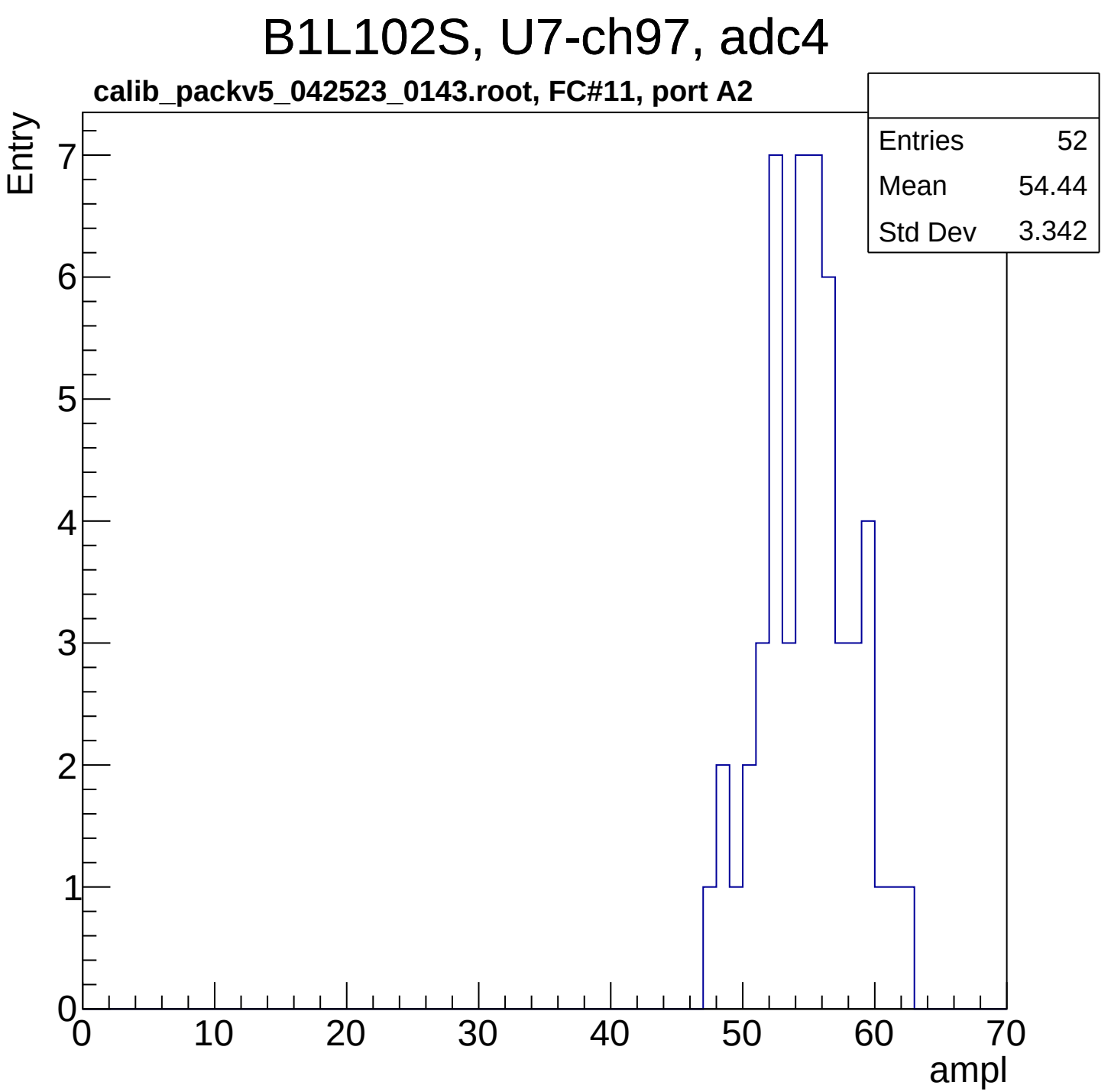
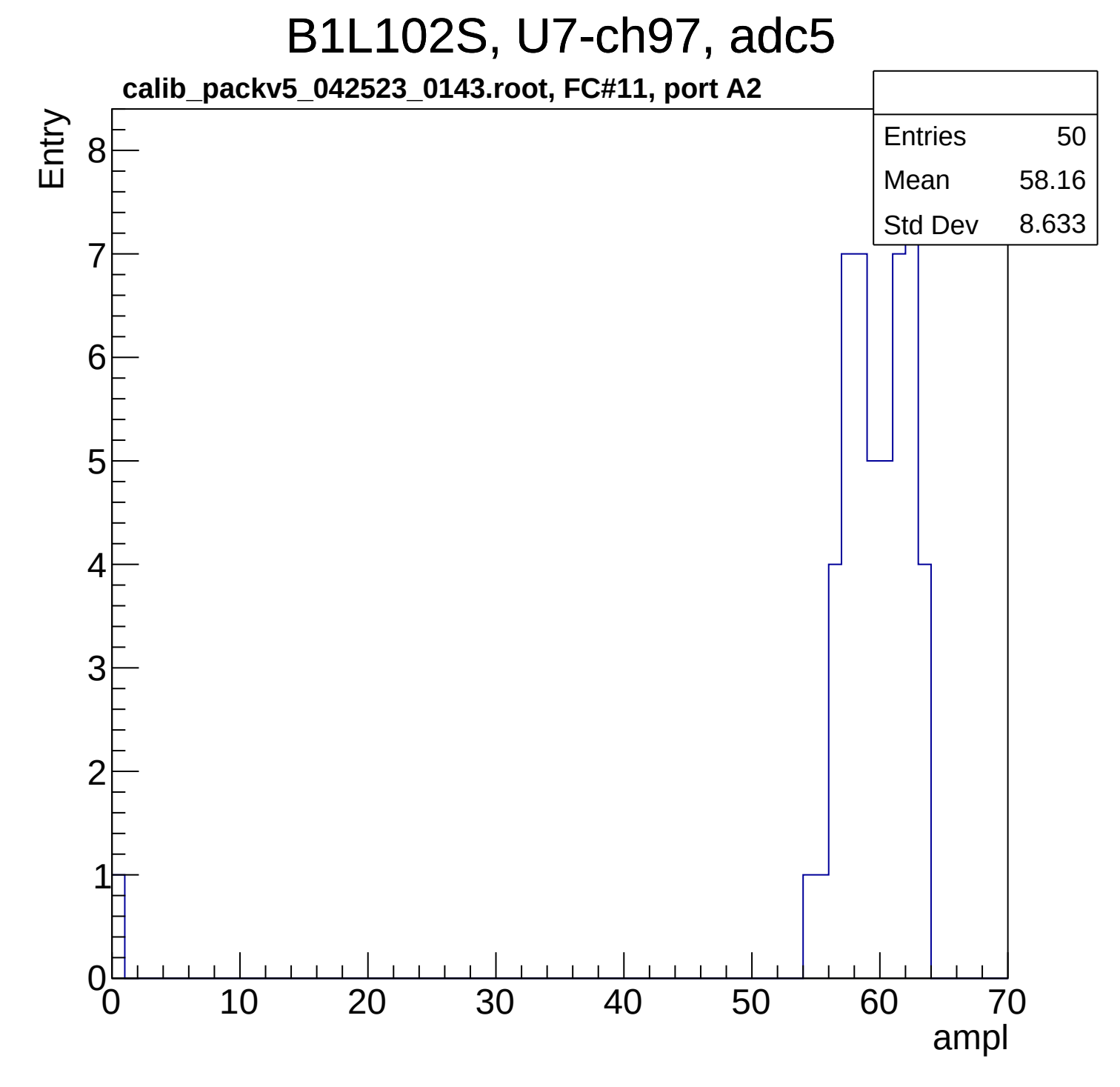

B1L102S, U7-ch97, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 74
Mean 48.26
Std Dev 3.695
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L102S, U7-ch97, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 52
Mean 54.44
Std Dev 3.342
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L102S, U7-ch97, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 50
Mean 58.16
Std Dev 8.633
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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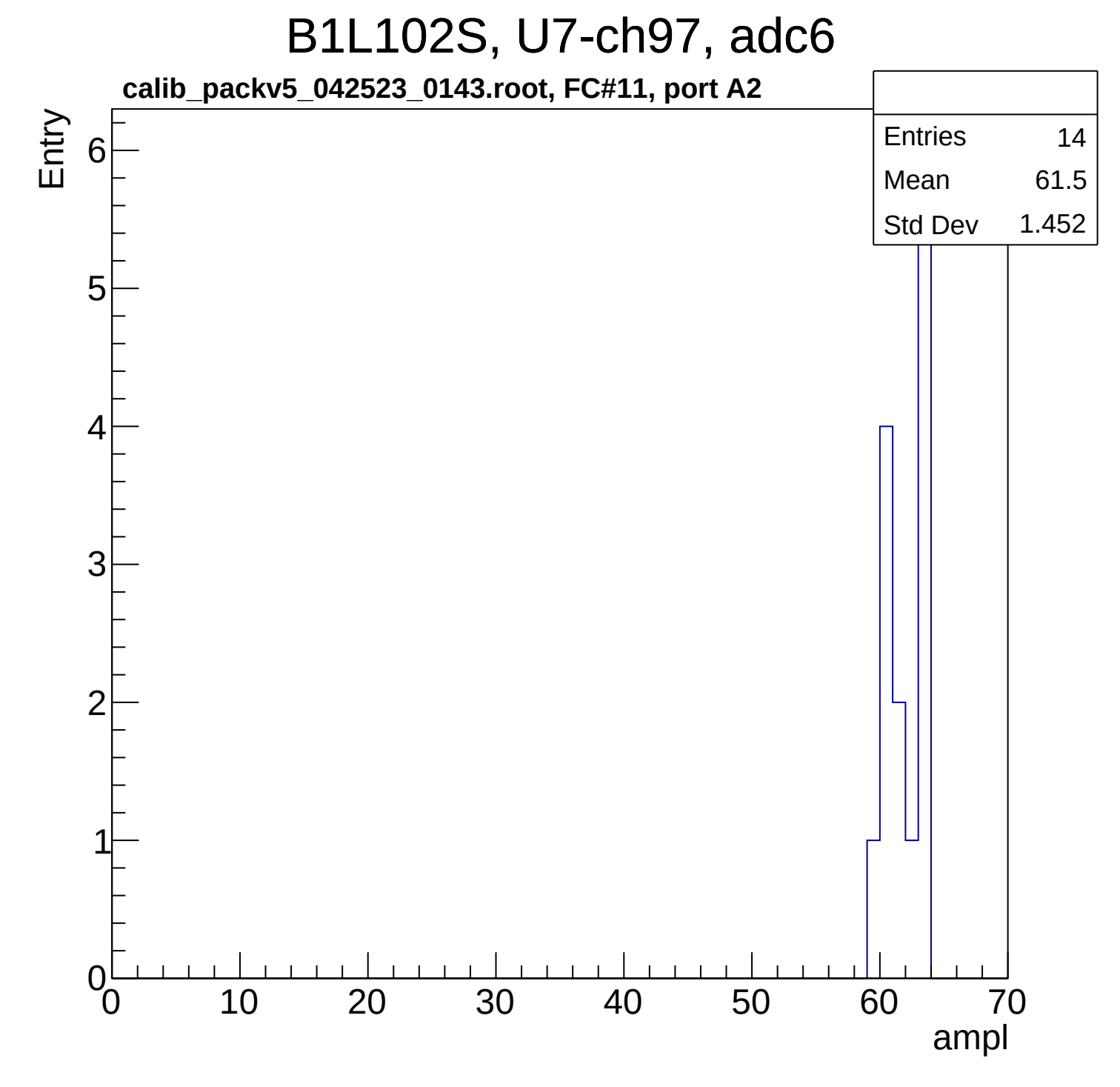
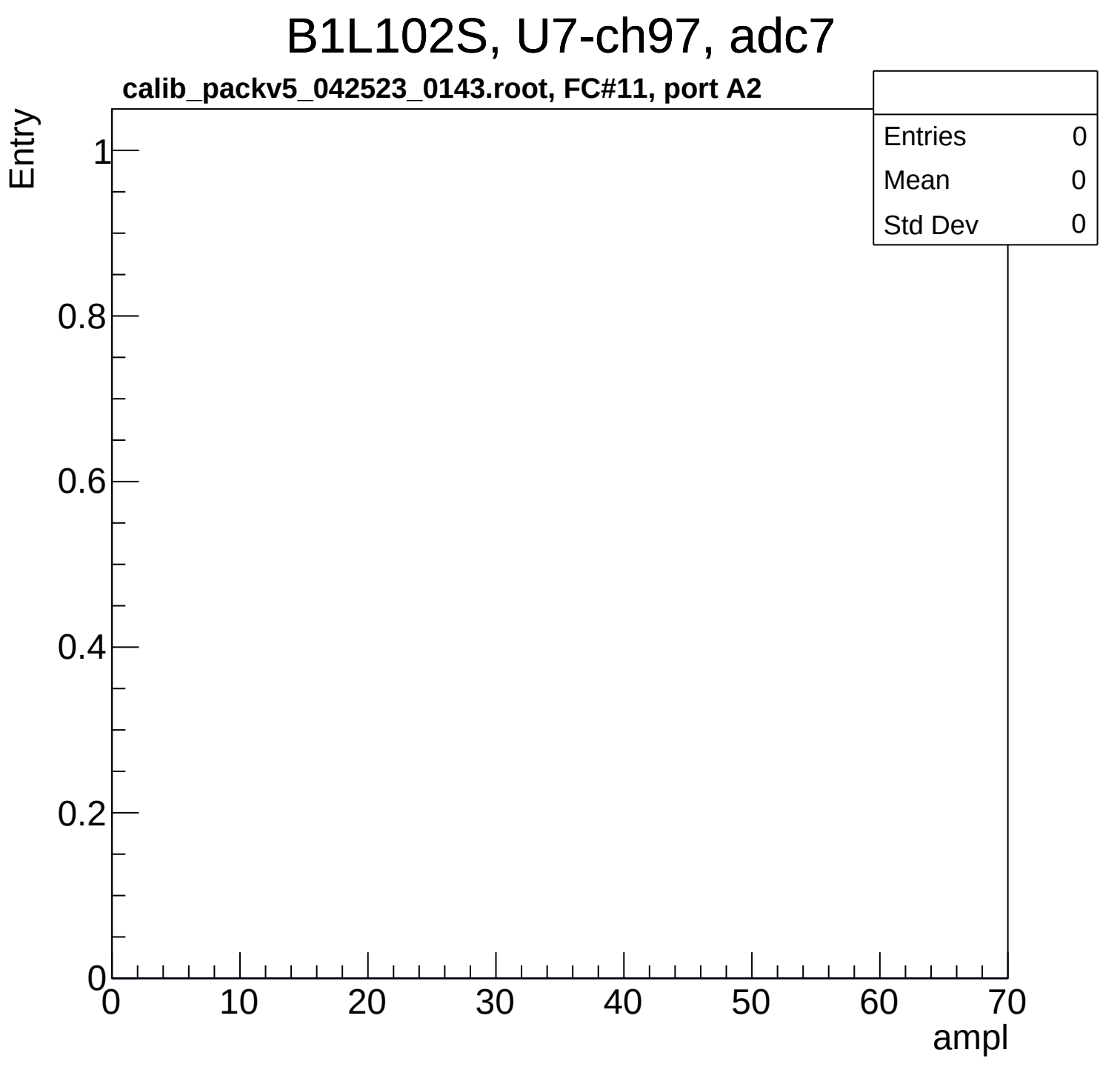
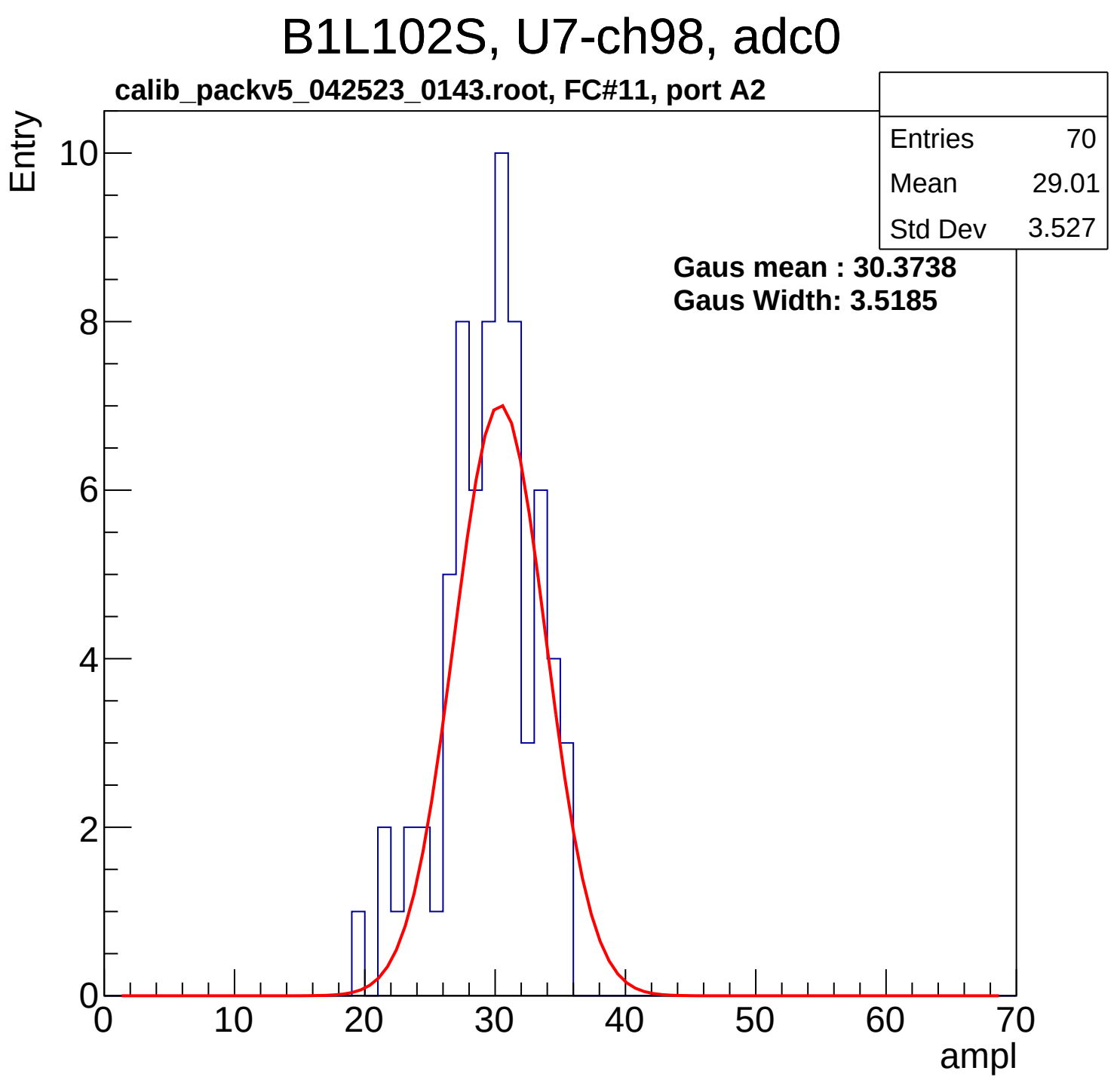
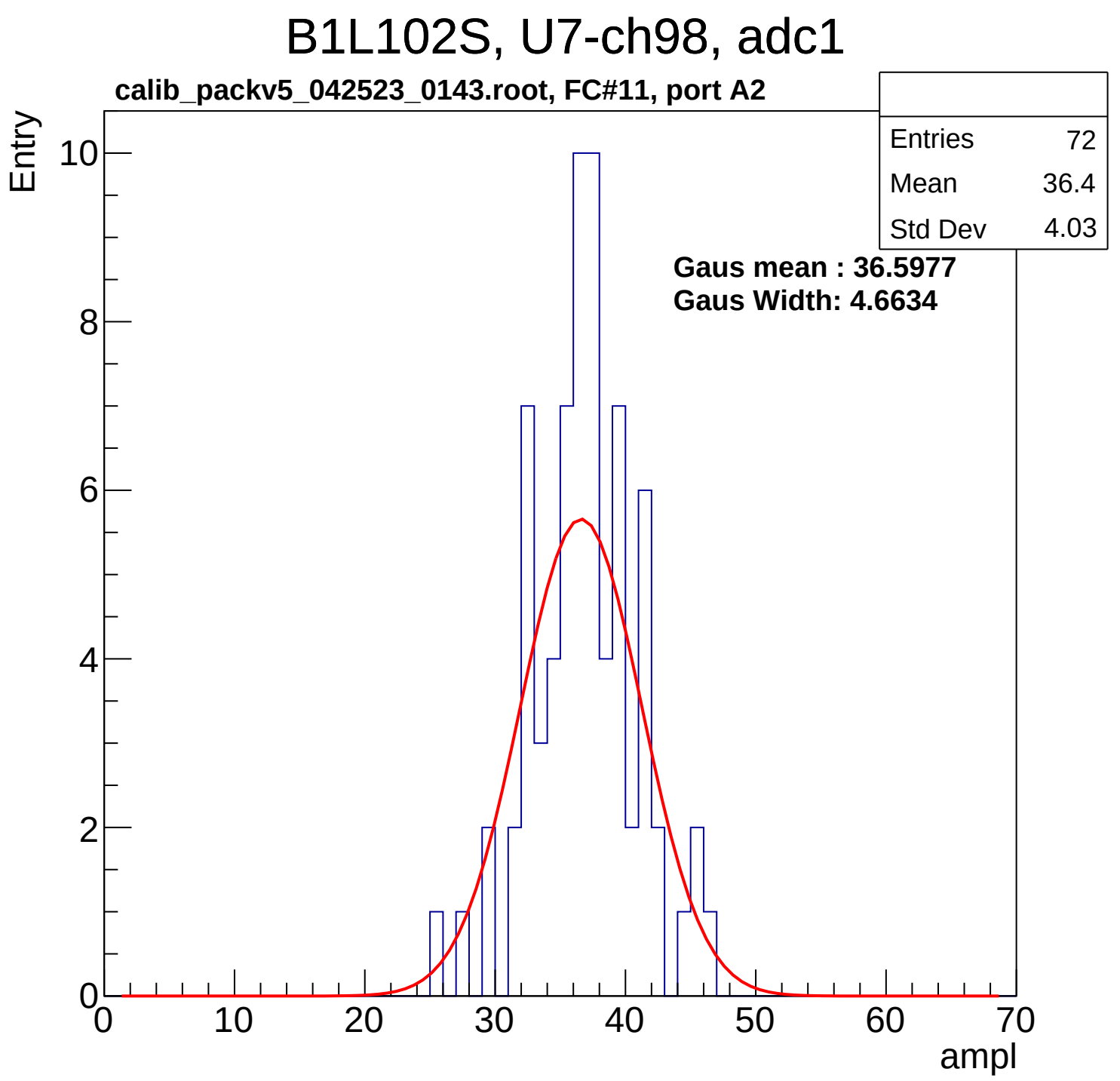
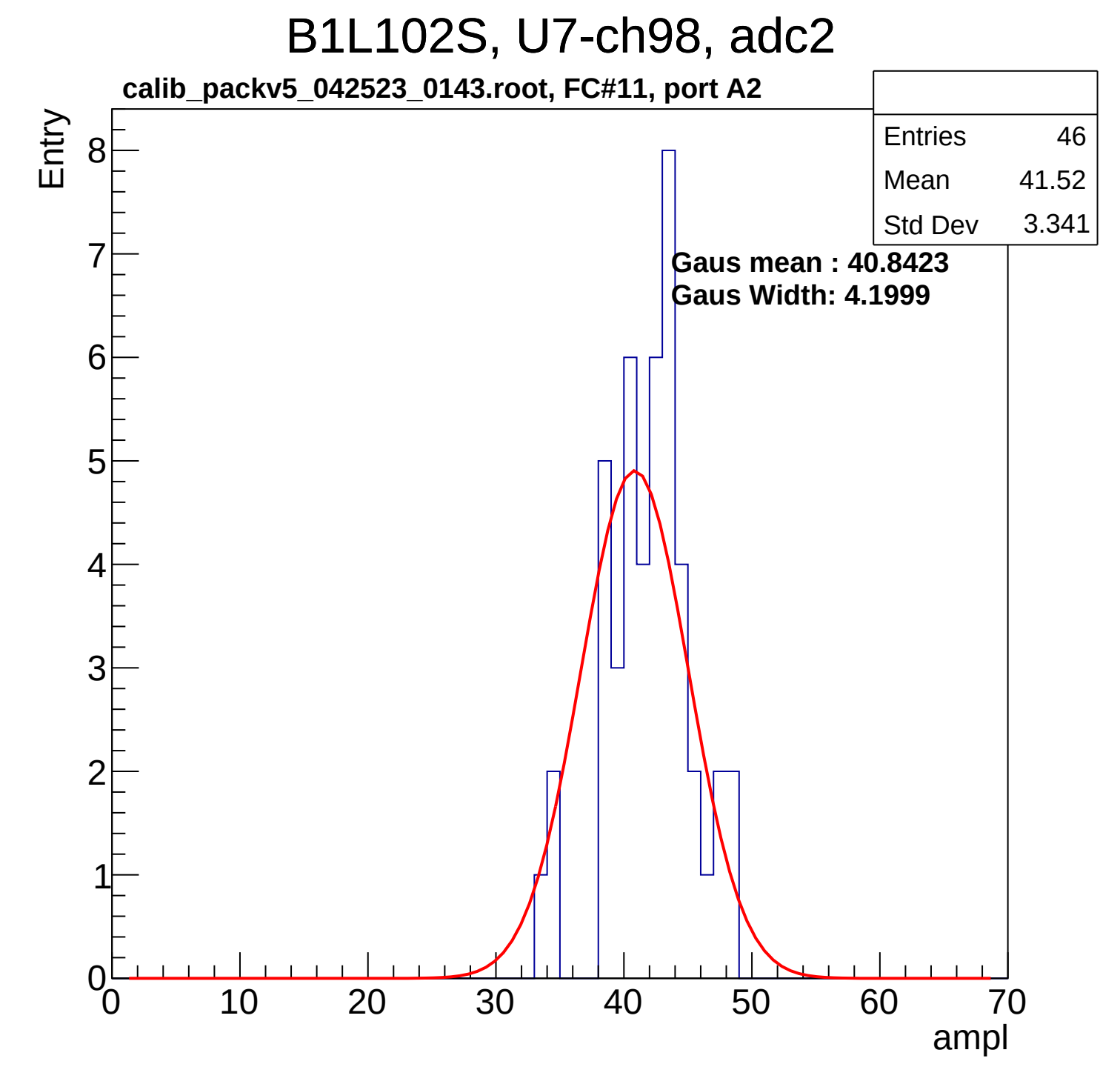

B1L102S, U7-ch97, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 14
Mean 61.5
Std Dev 1.452
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L102S, U7-ch97, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U7-ch98, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 70
Mean 29.01
Std Dev 3.527
Gaus mean : 30.3738
Gaus Width: 3.5185
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L102S, U7-ch98, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 72
Mean 36.4
Std Dev 4.03
Gaus mean : 36.5977
Gaus Width: 4.6634
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L102S, U7-ch98, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 46
Mean 41.52
Std Dev 3.341
Gaus mean : 40.8423
Gaus Width: 4.1999
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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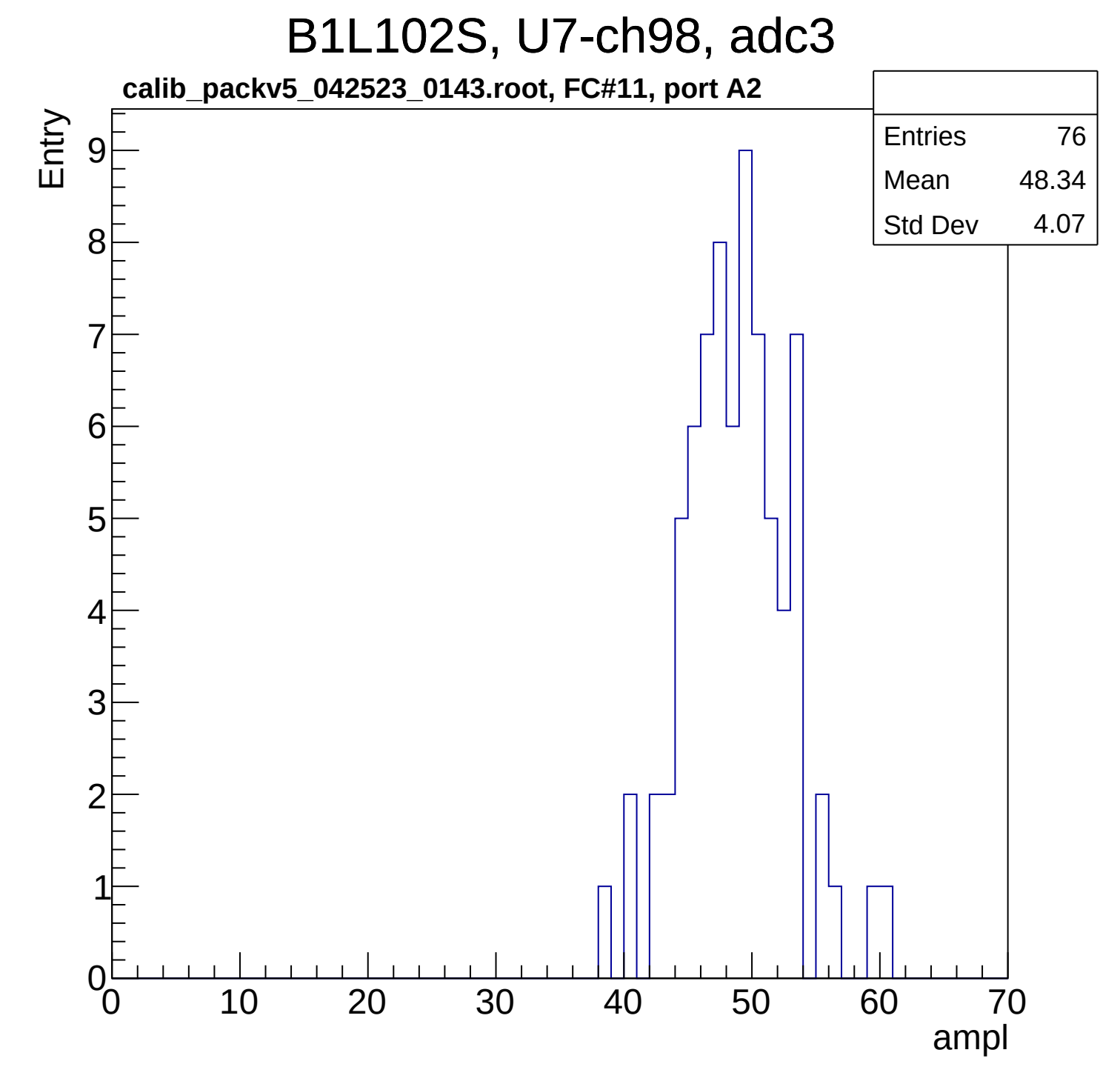
B1L102S, U7-ch98, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 76
Mean 48.34
Std Dev 4.07
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
30
40
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60
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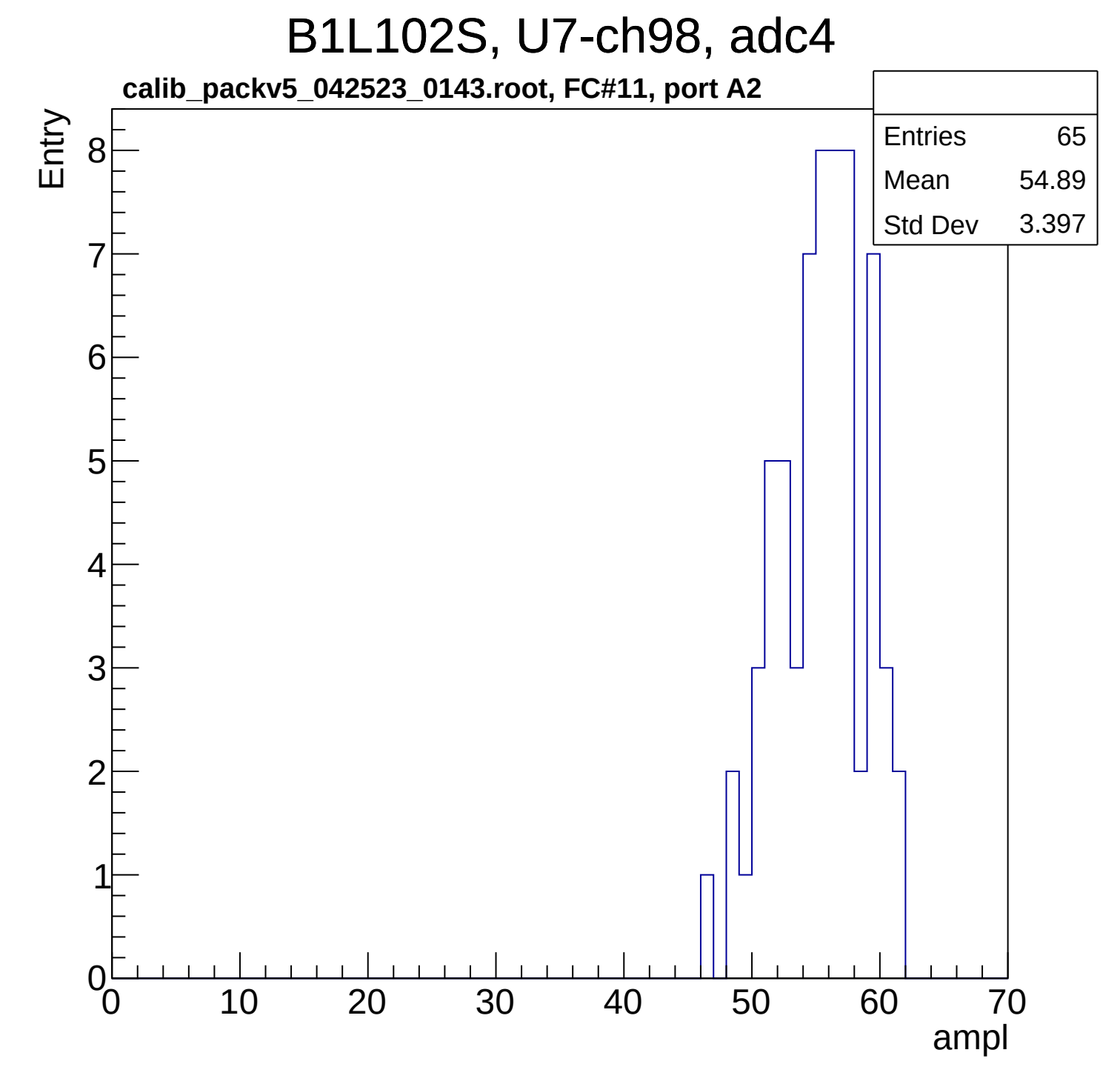
B1L102S, U7-ch98, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 65
Mean 54.89
Std Dev 3.397
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
30
40
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60
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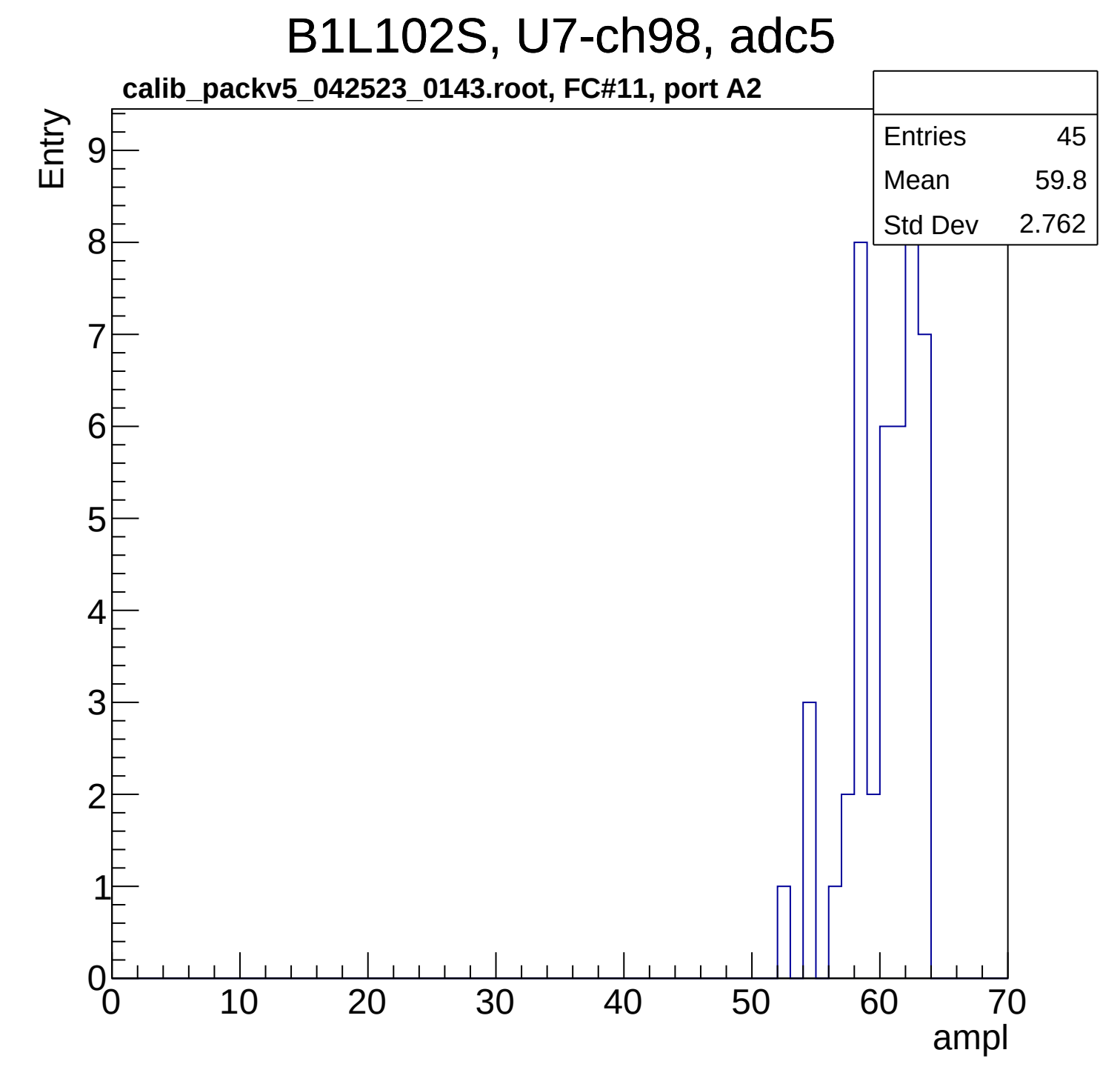
B1L102S, U7-ch98, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 45
Mean 59.8
Std Dev 2.762
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
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20
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40
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60
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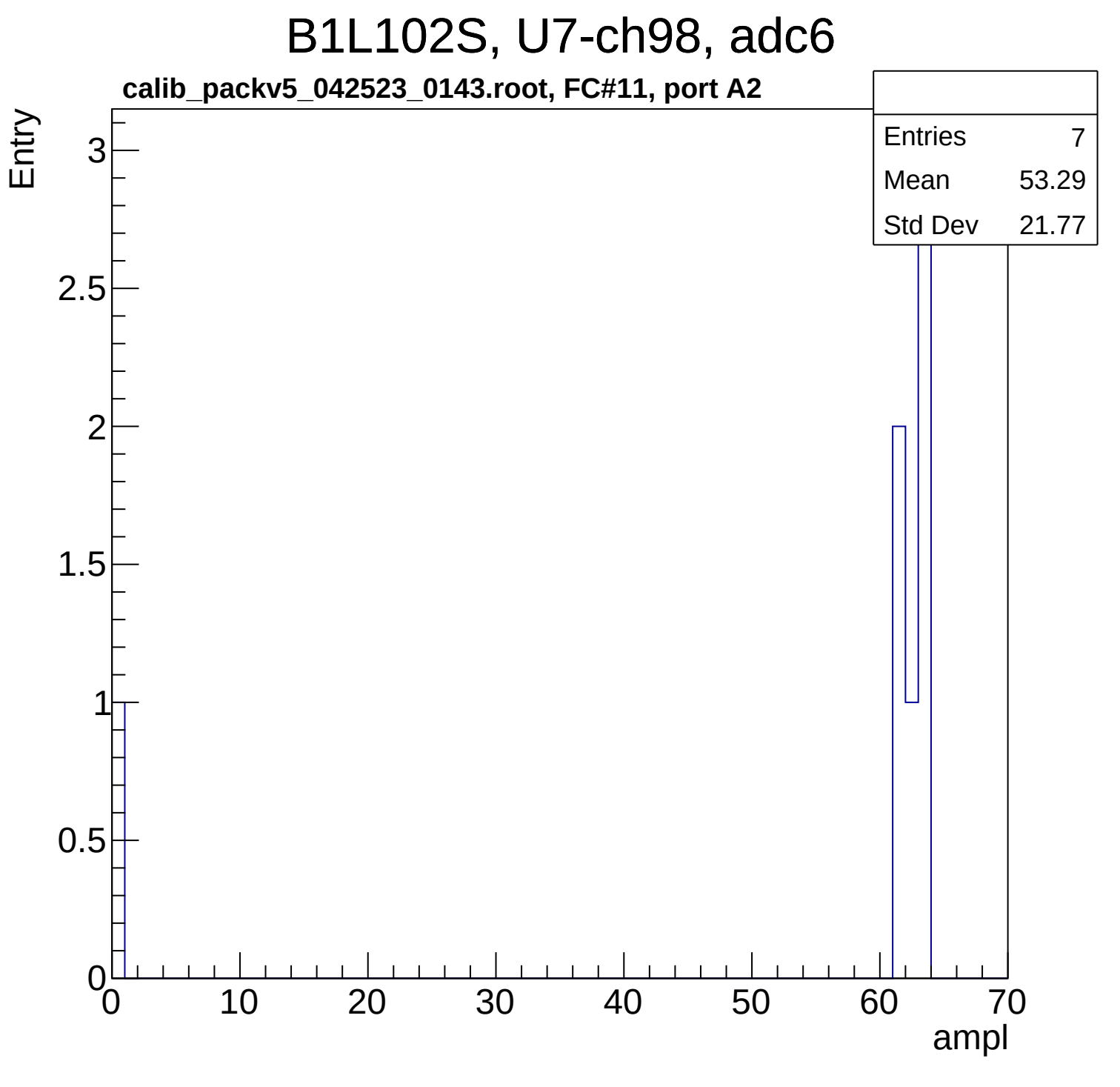
B1L102S, U7-ch98, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 7
Mean 53.29
Std Dev 21.77
Entry
ampl
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1
1.5
2
2.5
3
0
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60
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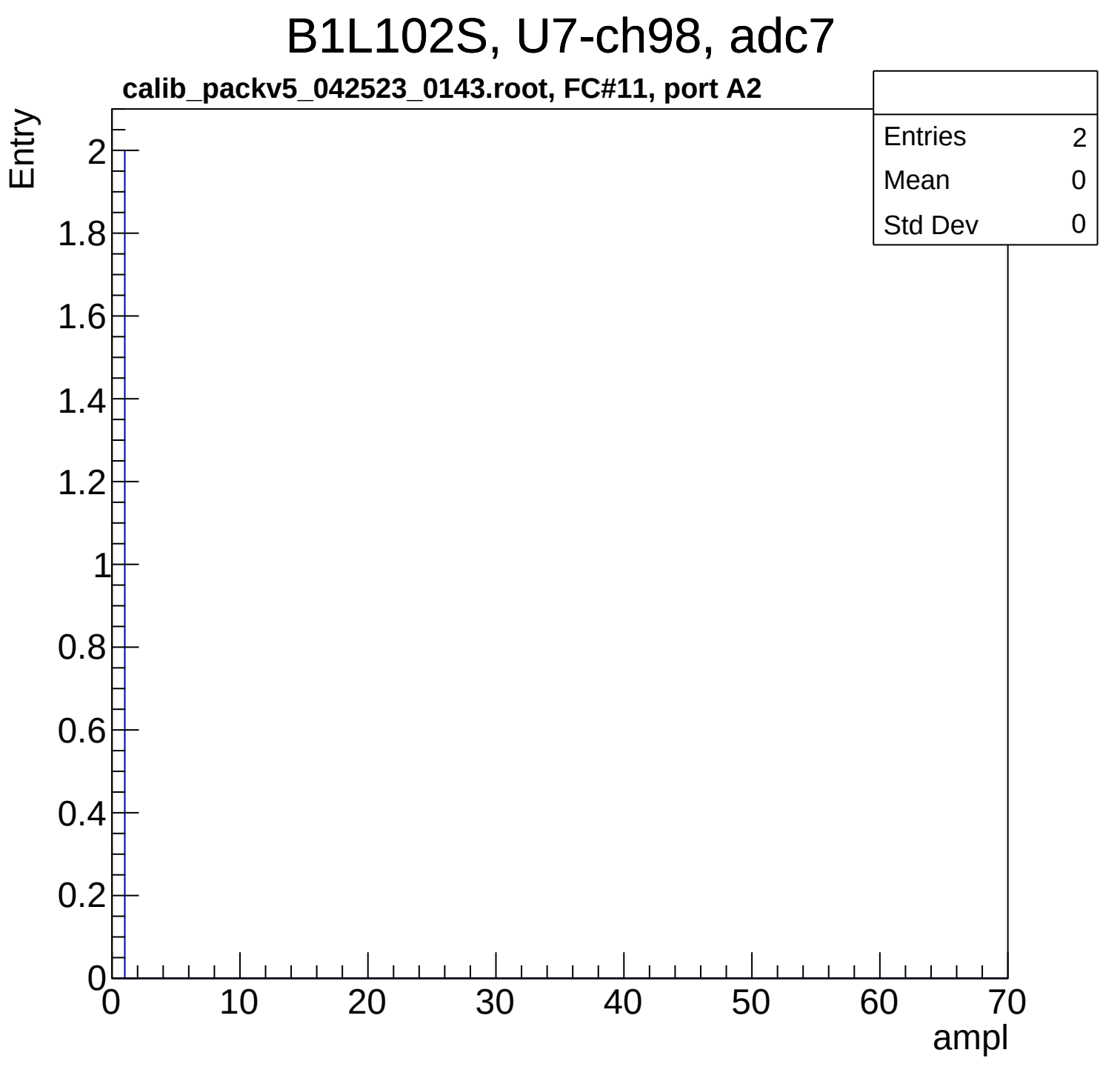
B1L102S, U7-ch98, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 2
Mean 0
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
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1
1.2
1.4
1.6
1.8
2
0
10
20
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40
50
60
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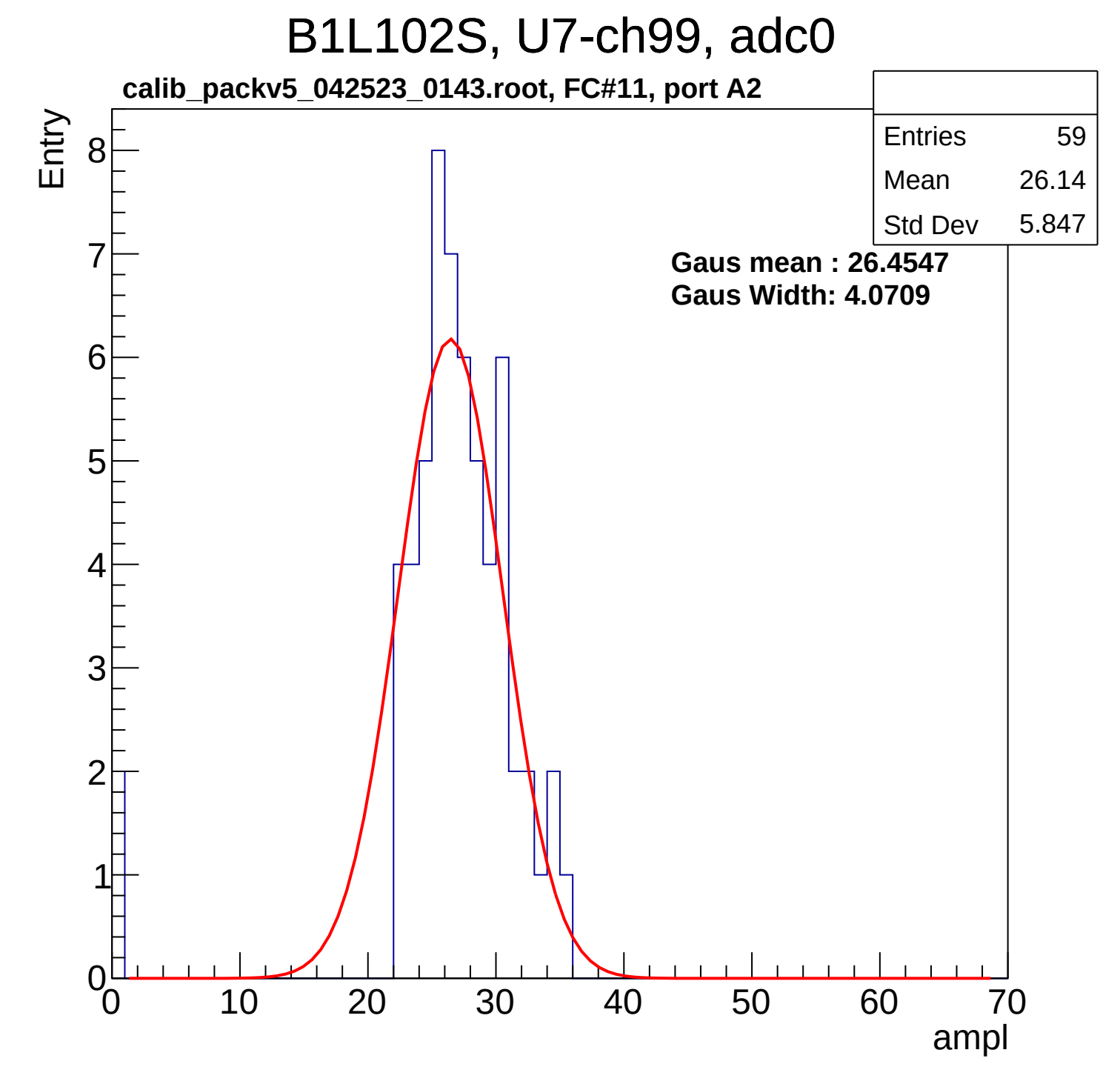
B1L102S, U7-ch99, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 59
Mean 26.14
Std Dev 5.847
Gaus mean : 26.4547
Gaus Width: 4.0709
Entry
ampl
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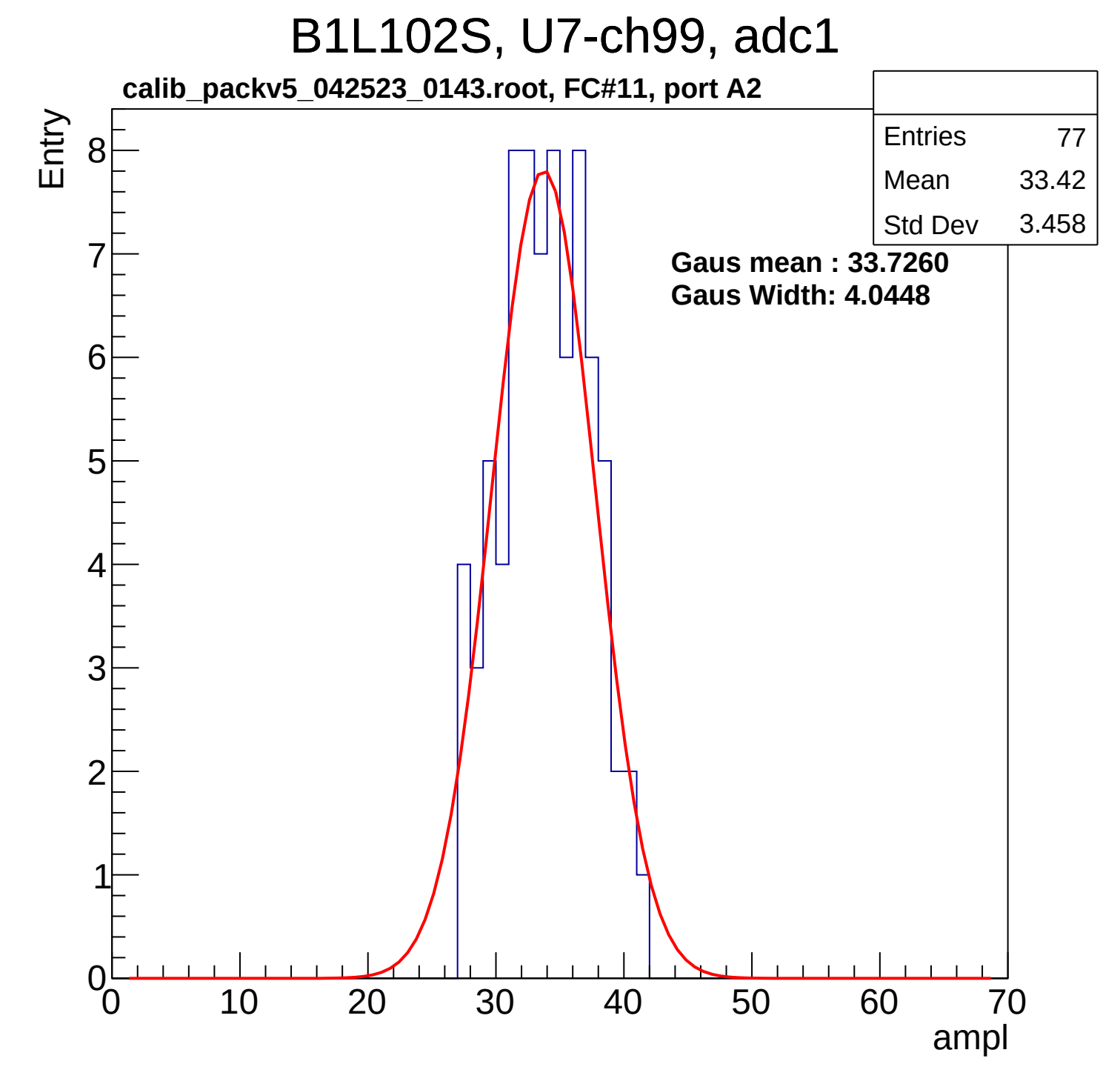
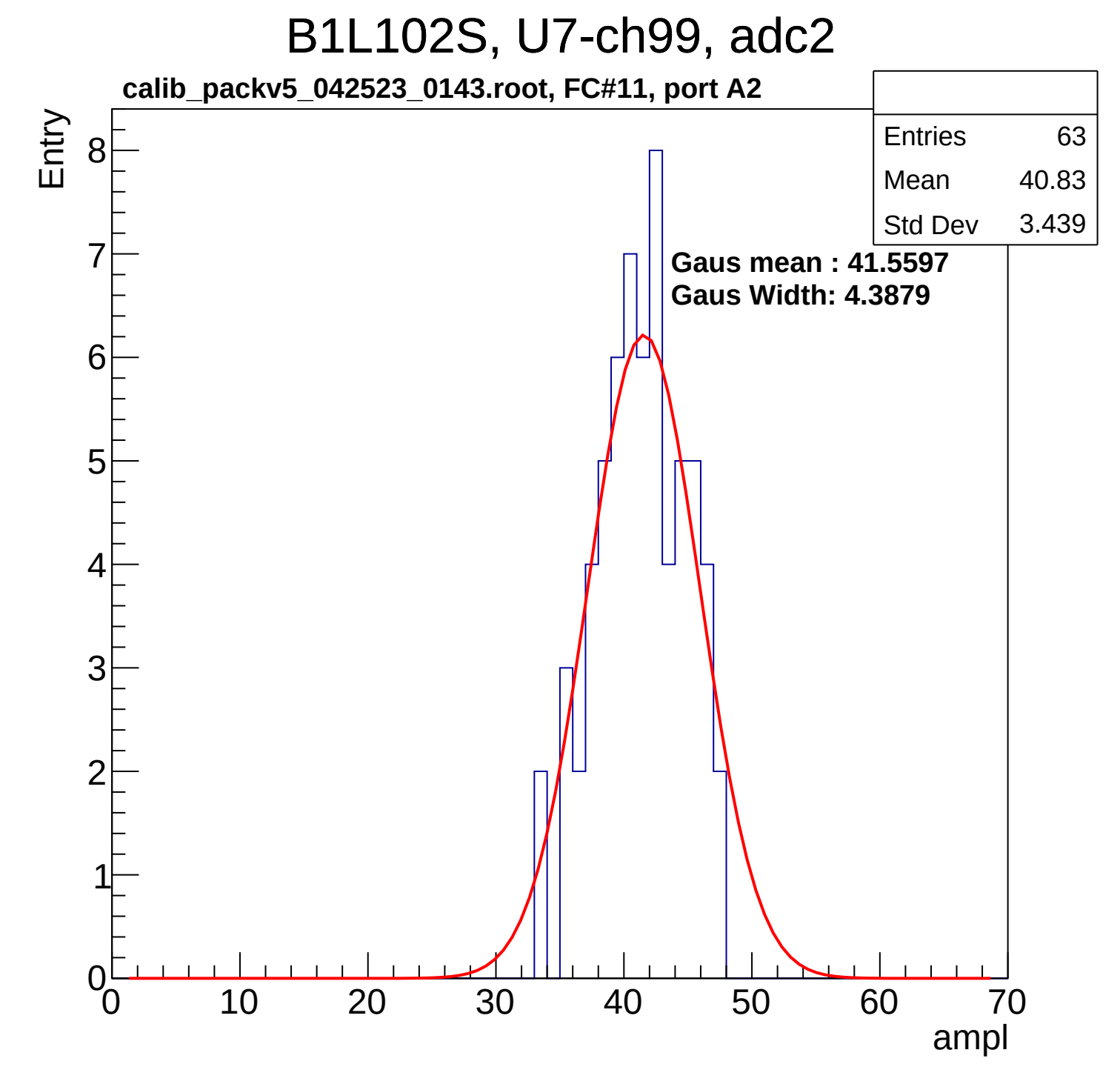
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L102S, U7-ch99, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 77
Mean 33.42
Std Dev 3.458
Gaus mean : 33.7260
Gaus Width: 4.0448
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L102S, U7-ch99, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 63
Mean 40.83
Std Dev 3.439
Gaus mean : 41.5597
Gaus Width: 4.3879
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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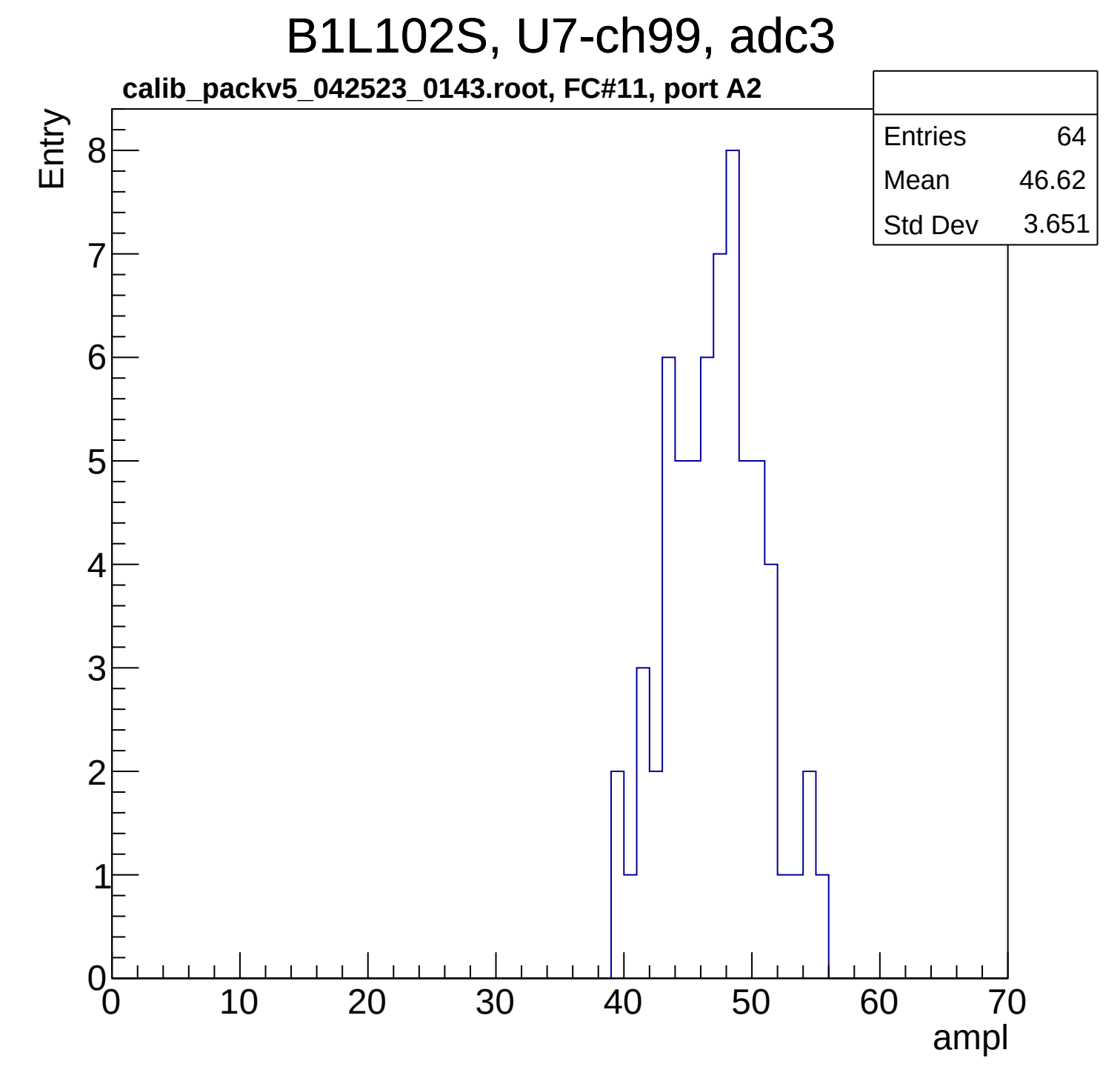
B1L102S, U7-ch99, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 64
Mean 46.62
Std Dev 3.651
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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40
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60
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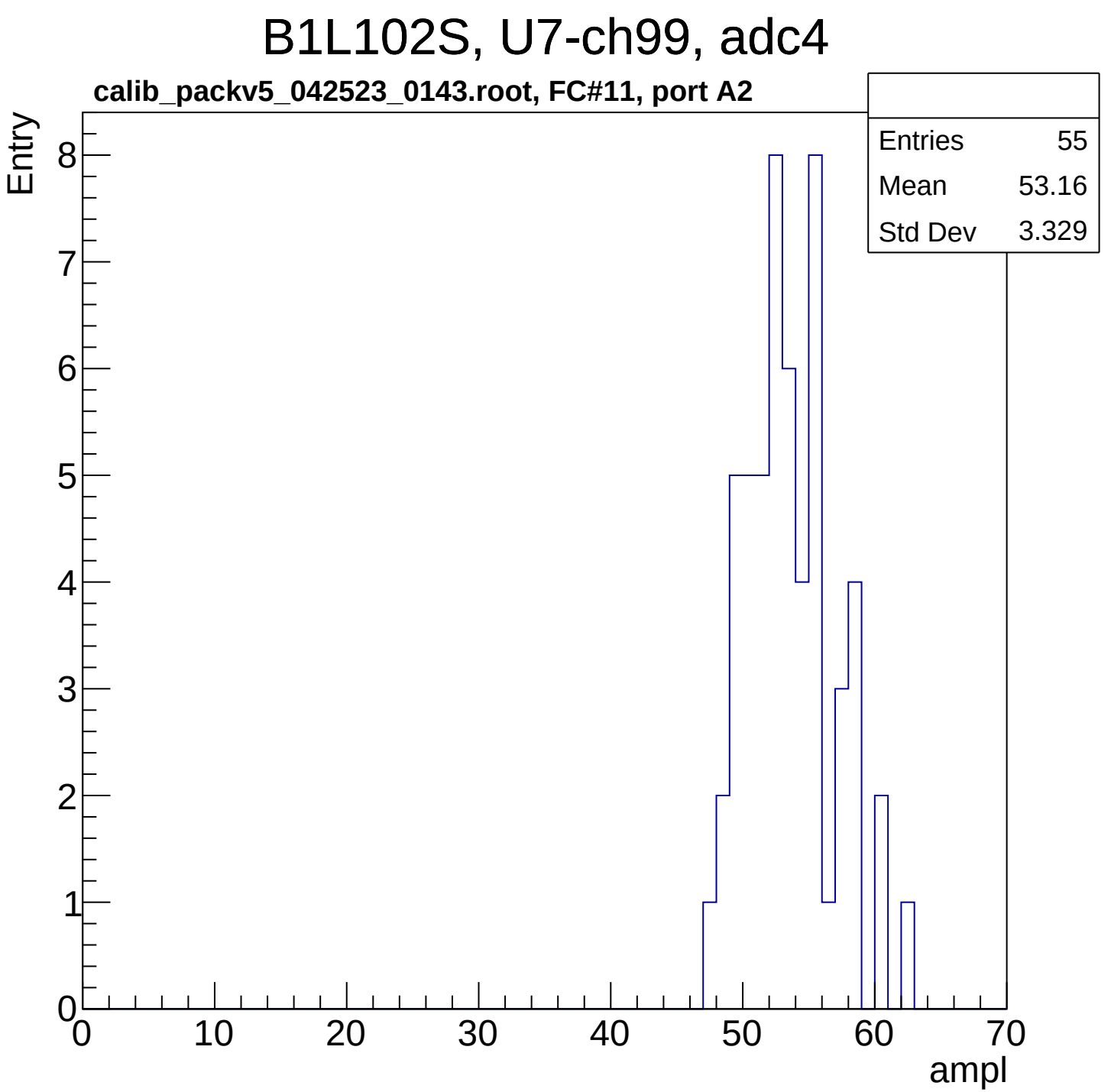
B1L102S, U7-ch99, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 55
Mean 53.16
Std Dev 3.329
Entry
ampl
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1
2
3
4
5
6
7
8
0
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40
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60
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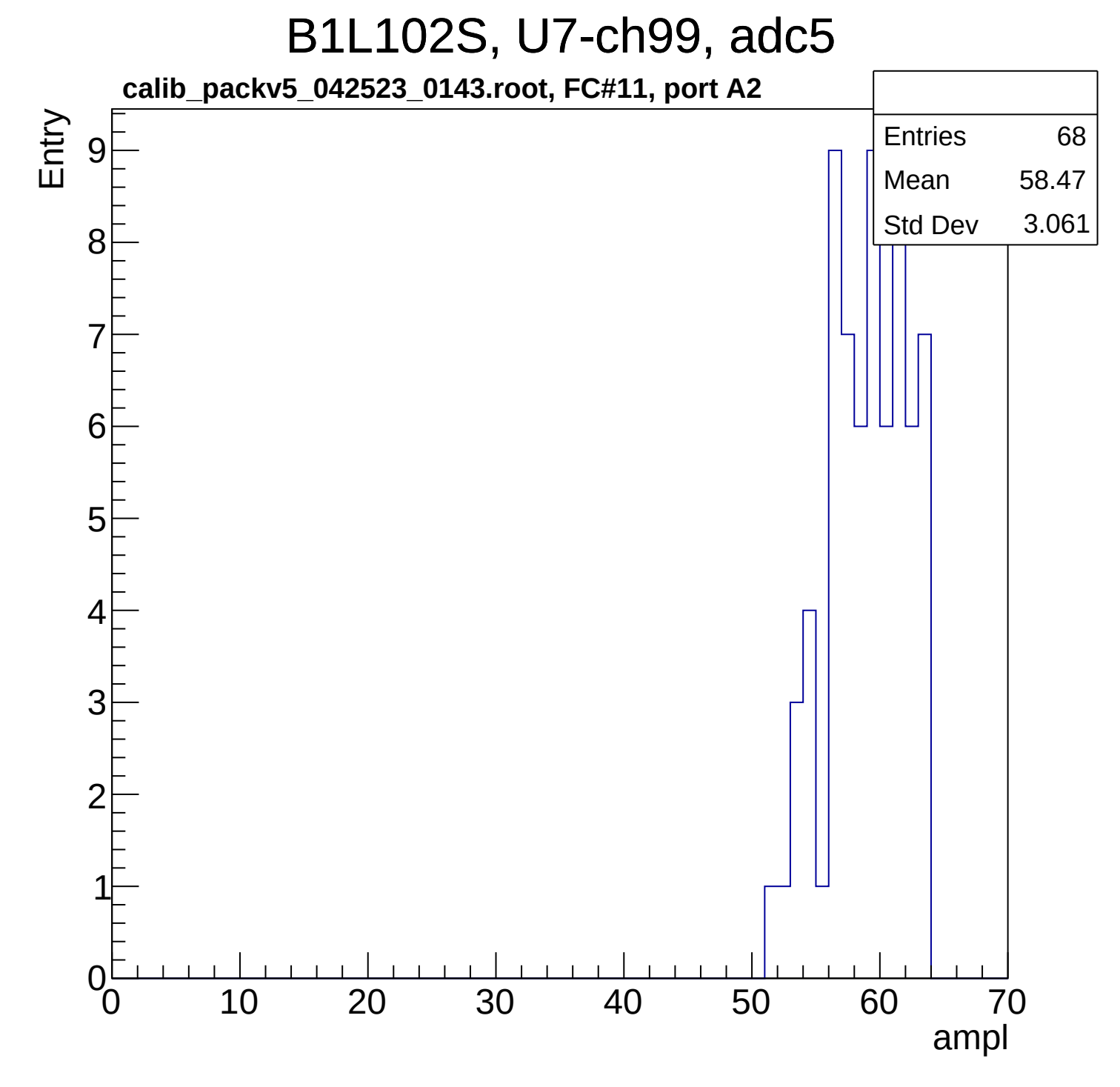
B1L102S, U7-ch99, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 68
Mean 58.47
Std Dev 3.061
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
50
60
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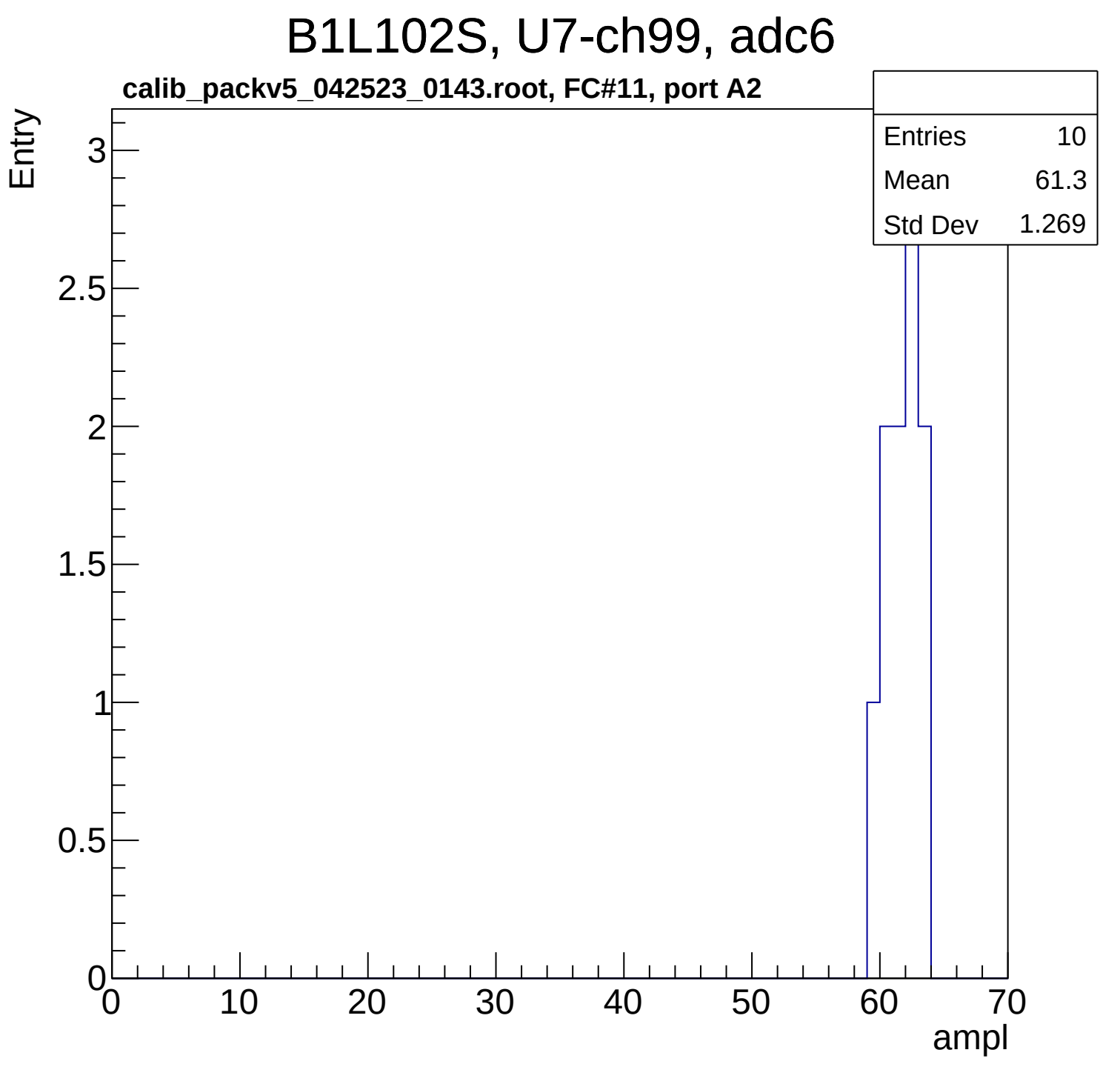
B1L102S, U7-ch99, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 10
Mean 61.3
Std Dev 1.269
Entry
ampl
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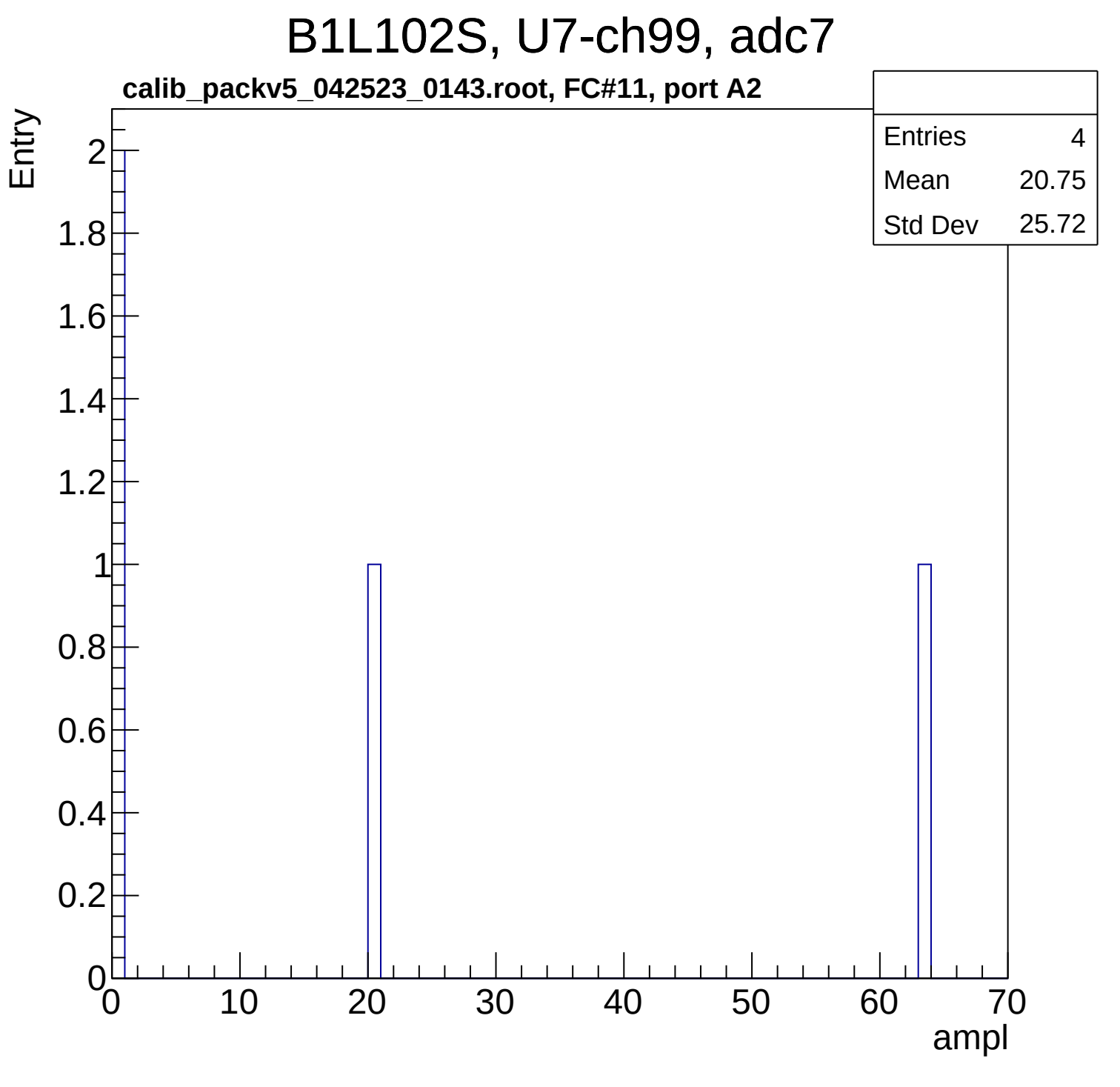
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L102S, U7-ch99, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 4
Mean 20.75
Std Dev 25.72
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
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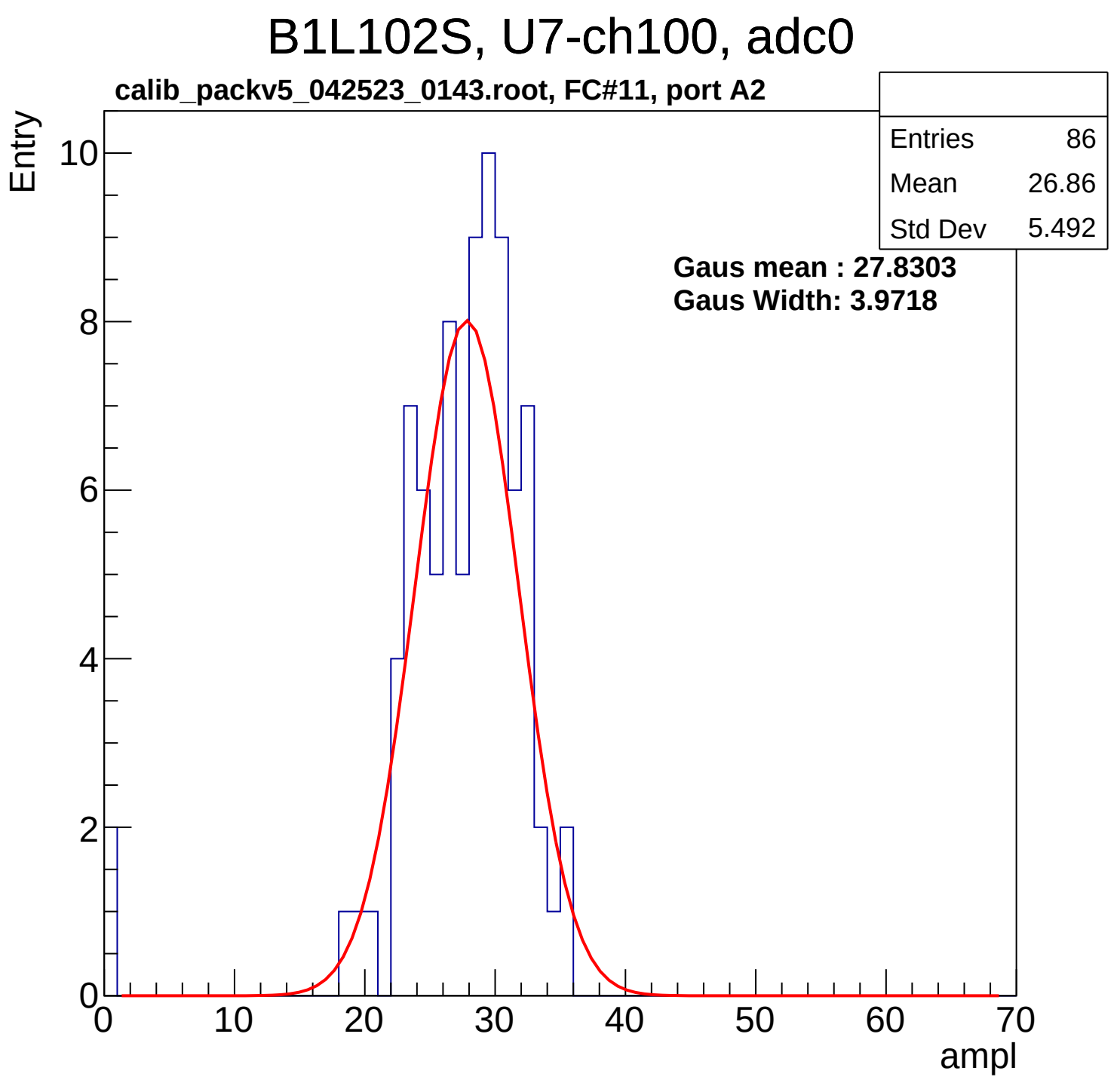
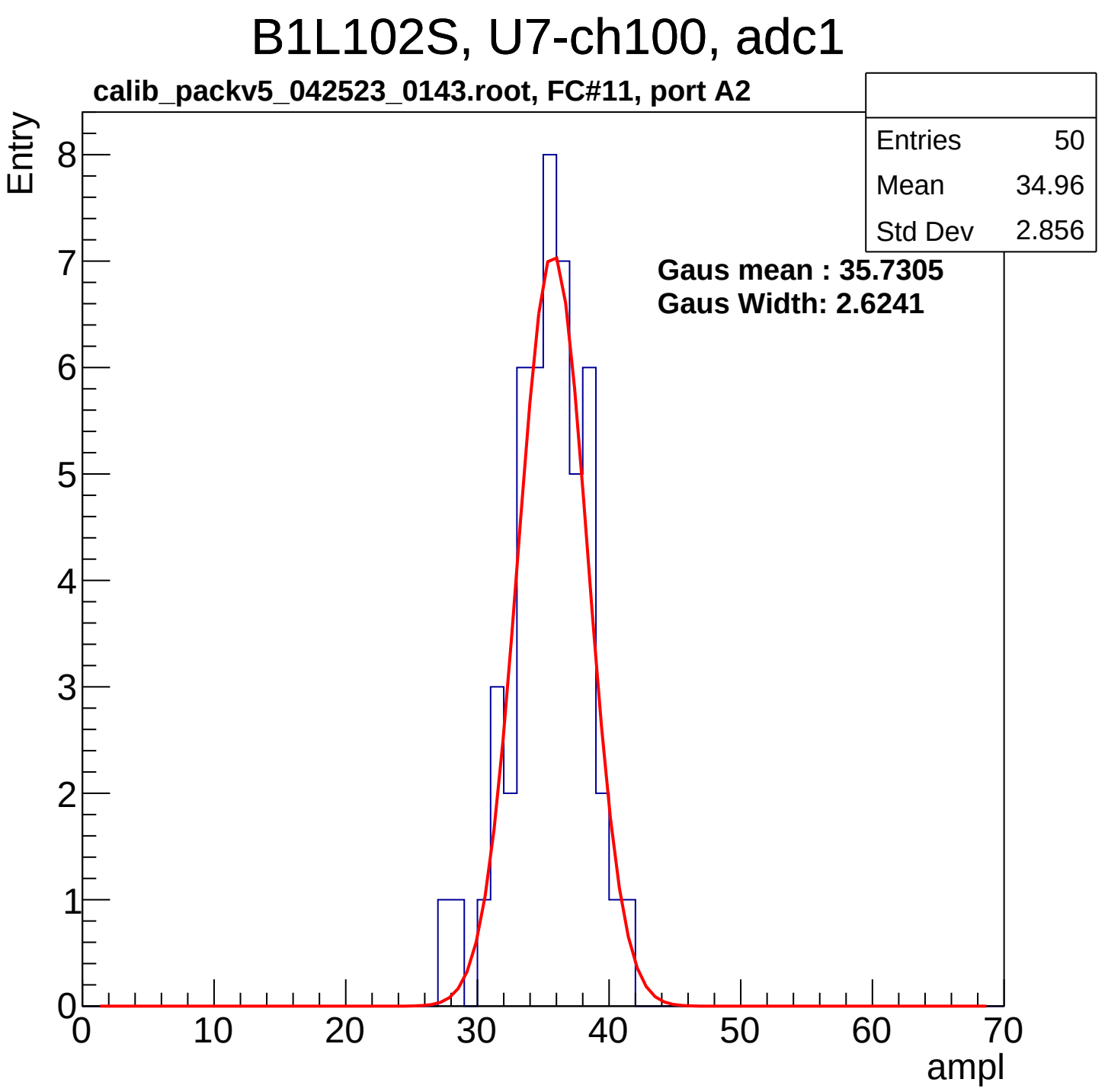

B1L102S, U7-ch100, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 86
Mean 26.86
Std Dev 5.492
Gaus mean : 27.8303
Gaus Width: 3.9718
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L102S, U7-ch100, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 50
Mean 34.96
Std Dev 2.856
Gaus mean : 35.7305
Gaus Width: 2.6241
Entry
ampl
0
1
2
3
4
5
6
7
8
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20
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60
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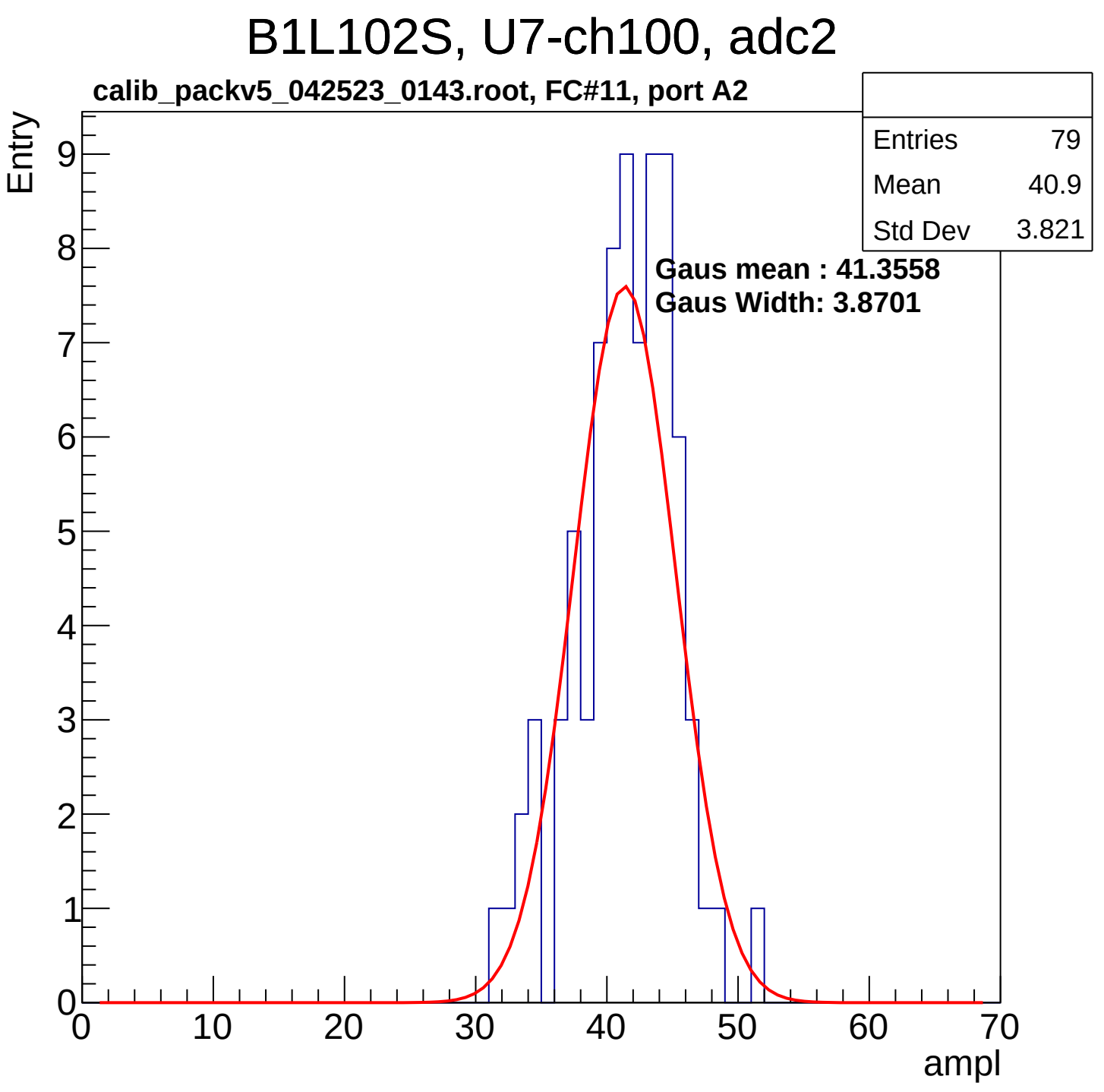
B1L102S, U7-ch100, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 79
Mean 40.9
Std Dev 3.821
Gaus mean : 41.3558
Gaus Width: 3.8701
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
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60
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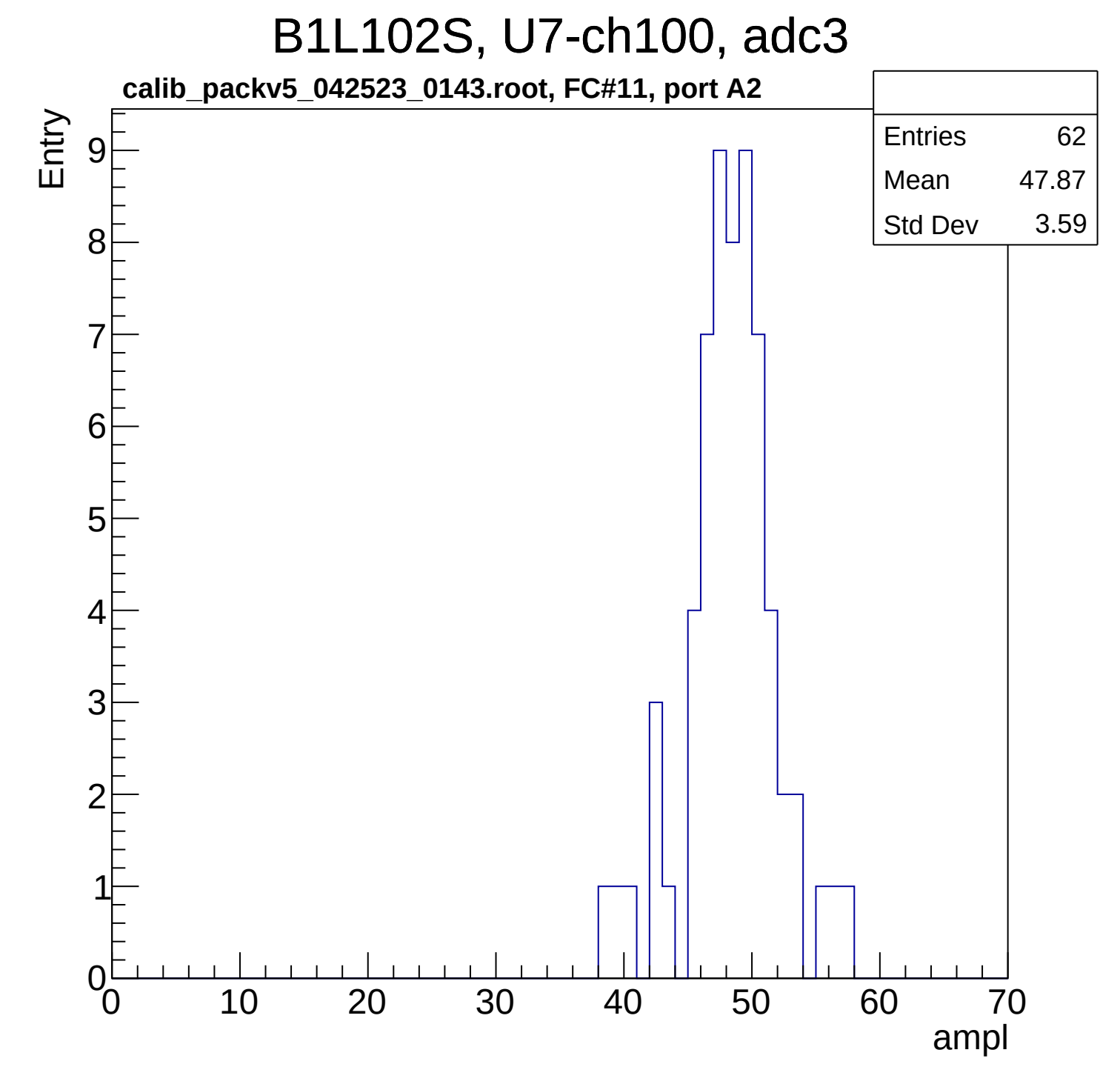
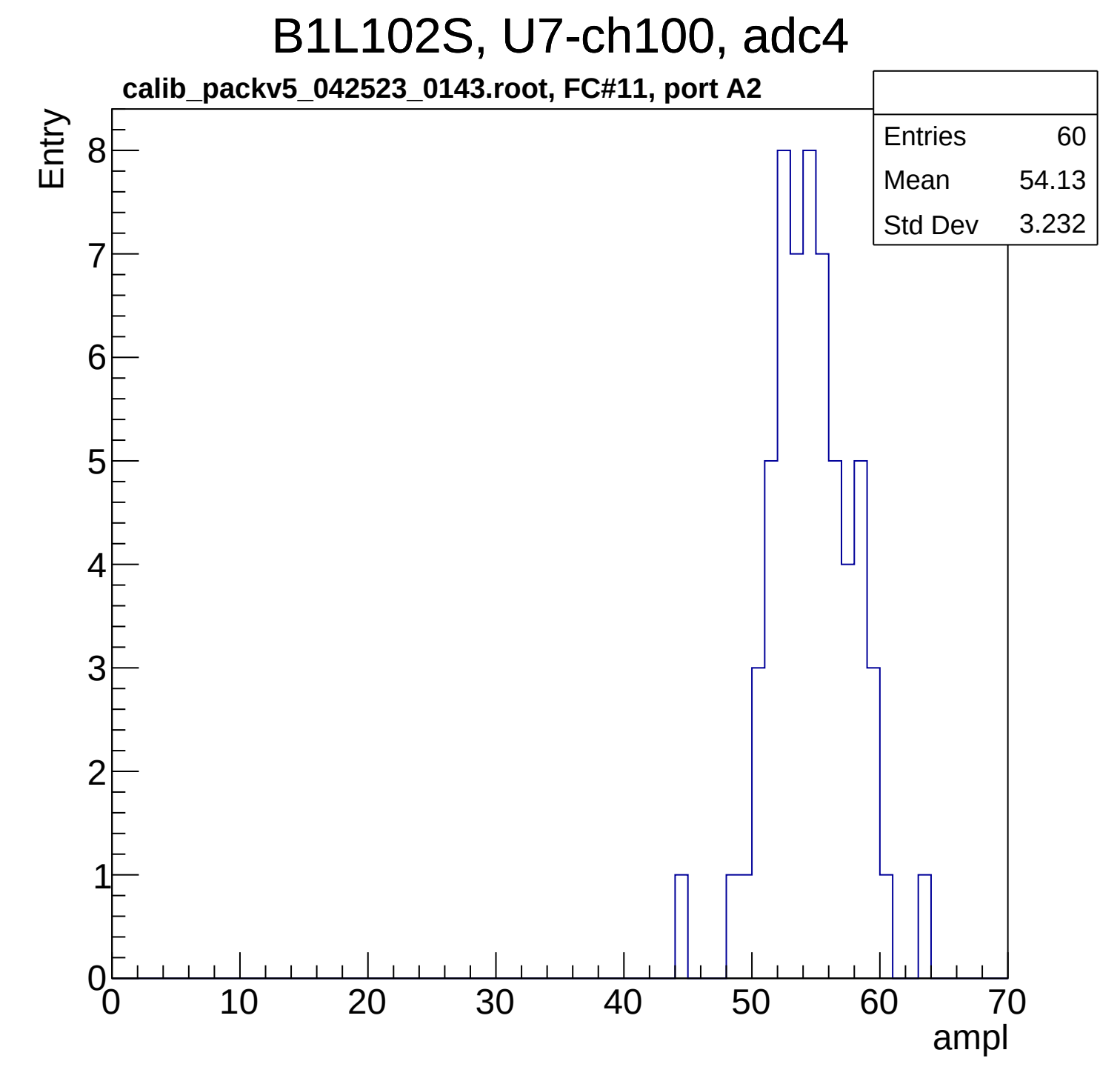
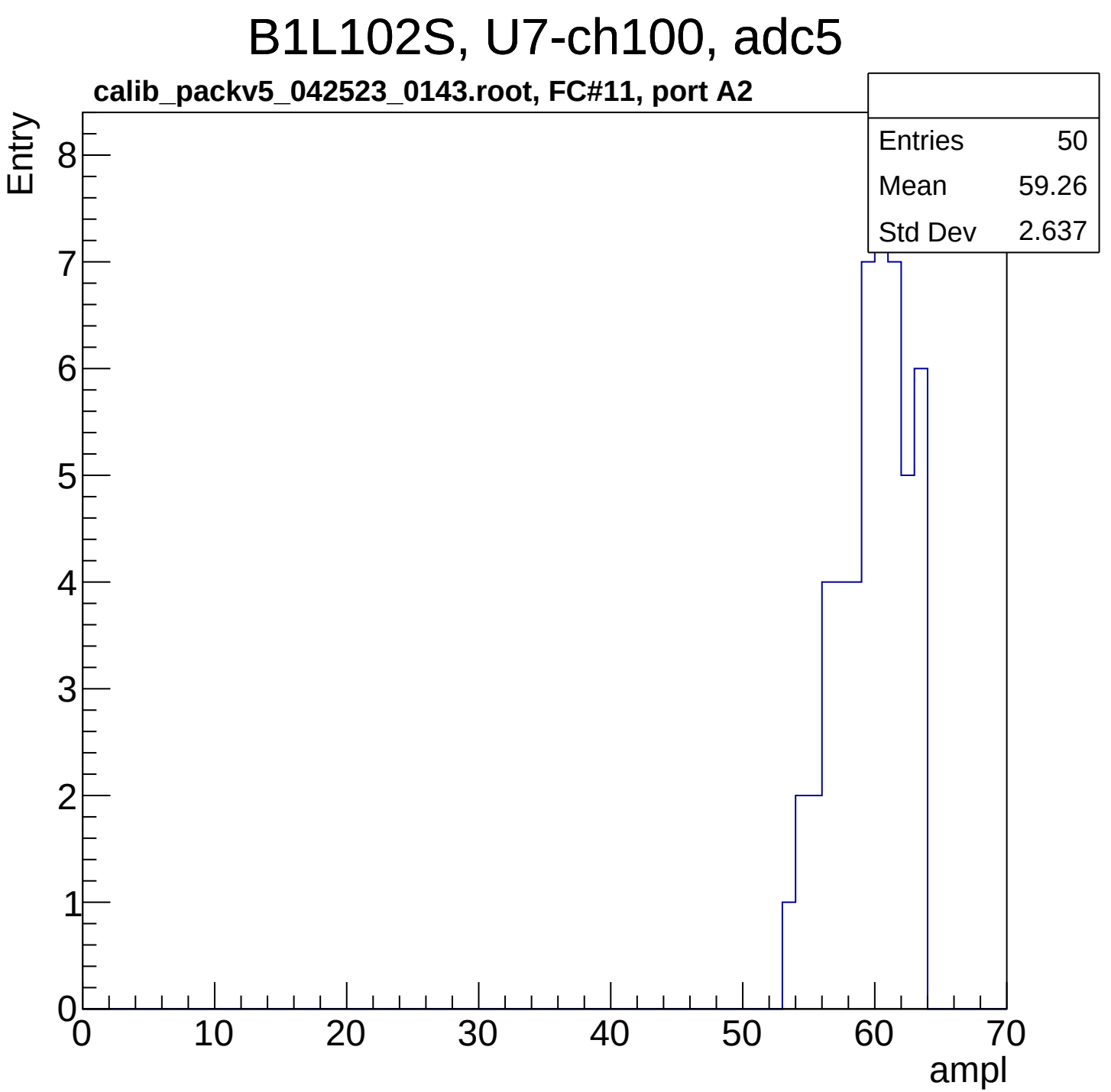

B1L102S, U7-ch100, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 62
Mean 47.87
Std Dev 3.59
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L102S, U7-ch100, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 60
Mean 54.13
Std Dev 3.232
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L102S, U7-ch100, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 50
Mean 59.26
Std Dev 2.637
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
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60
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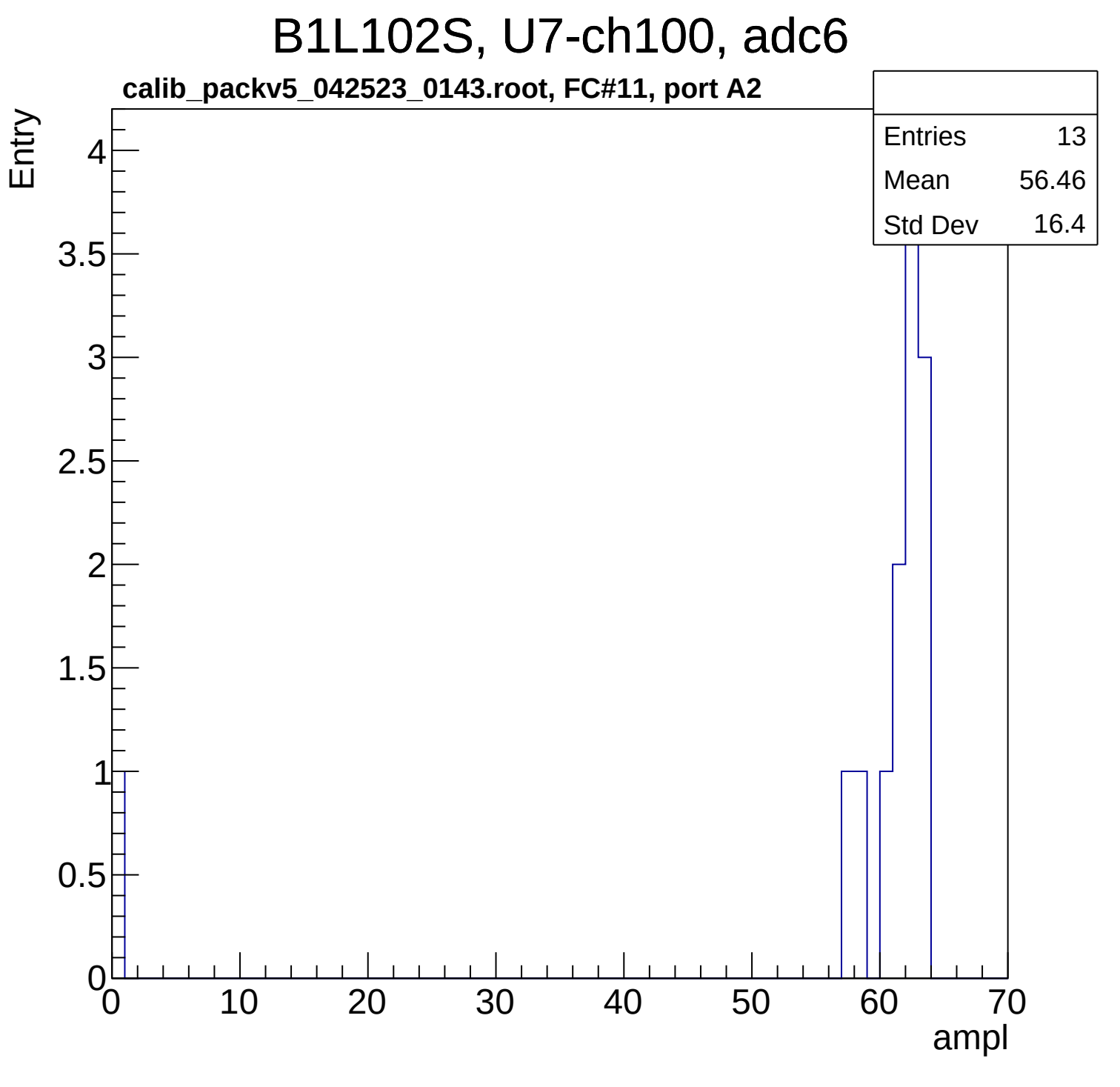
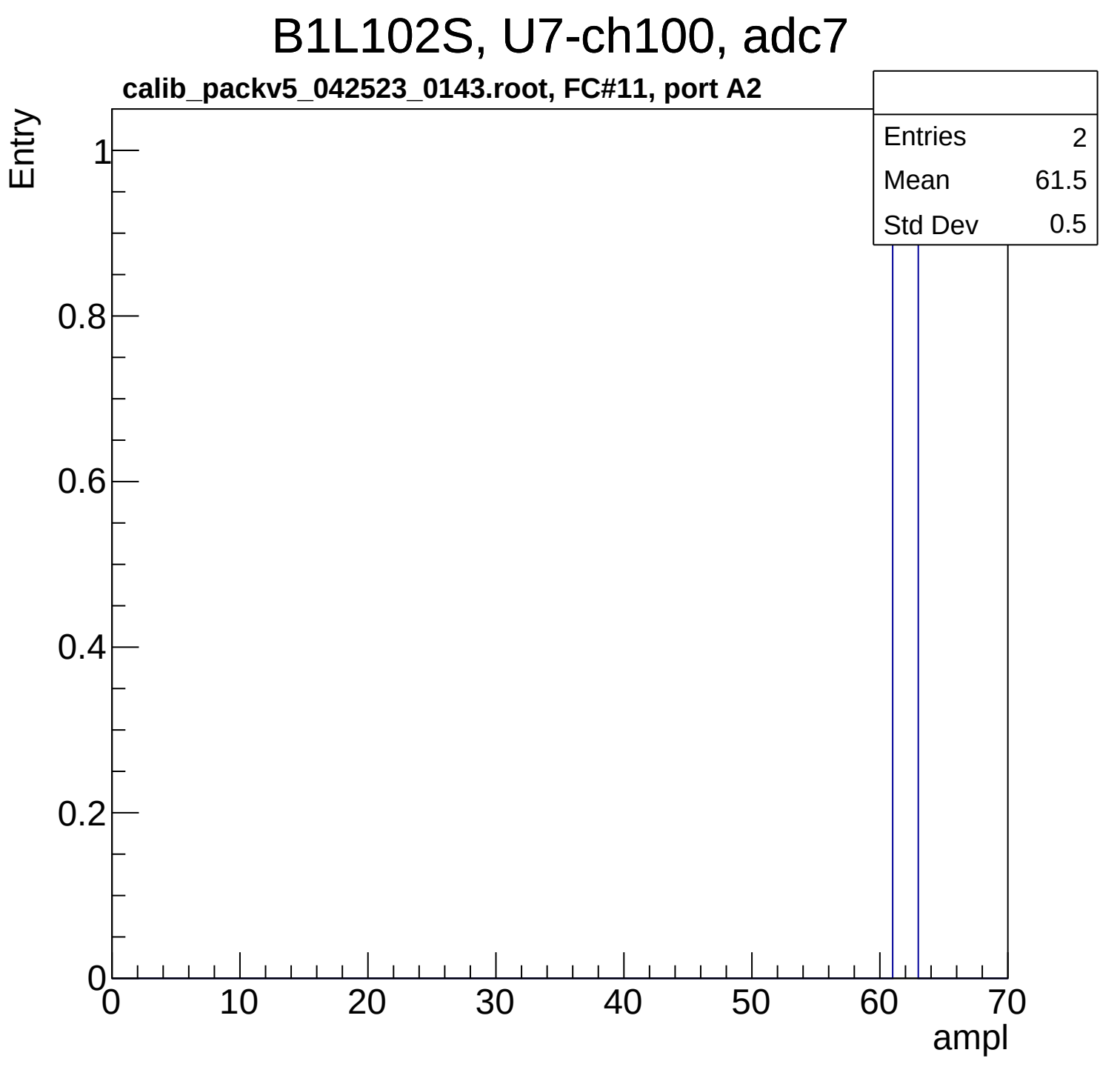
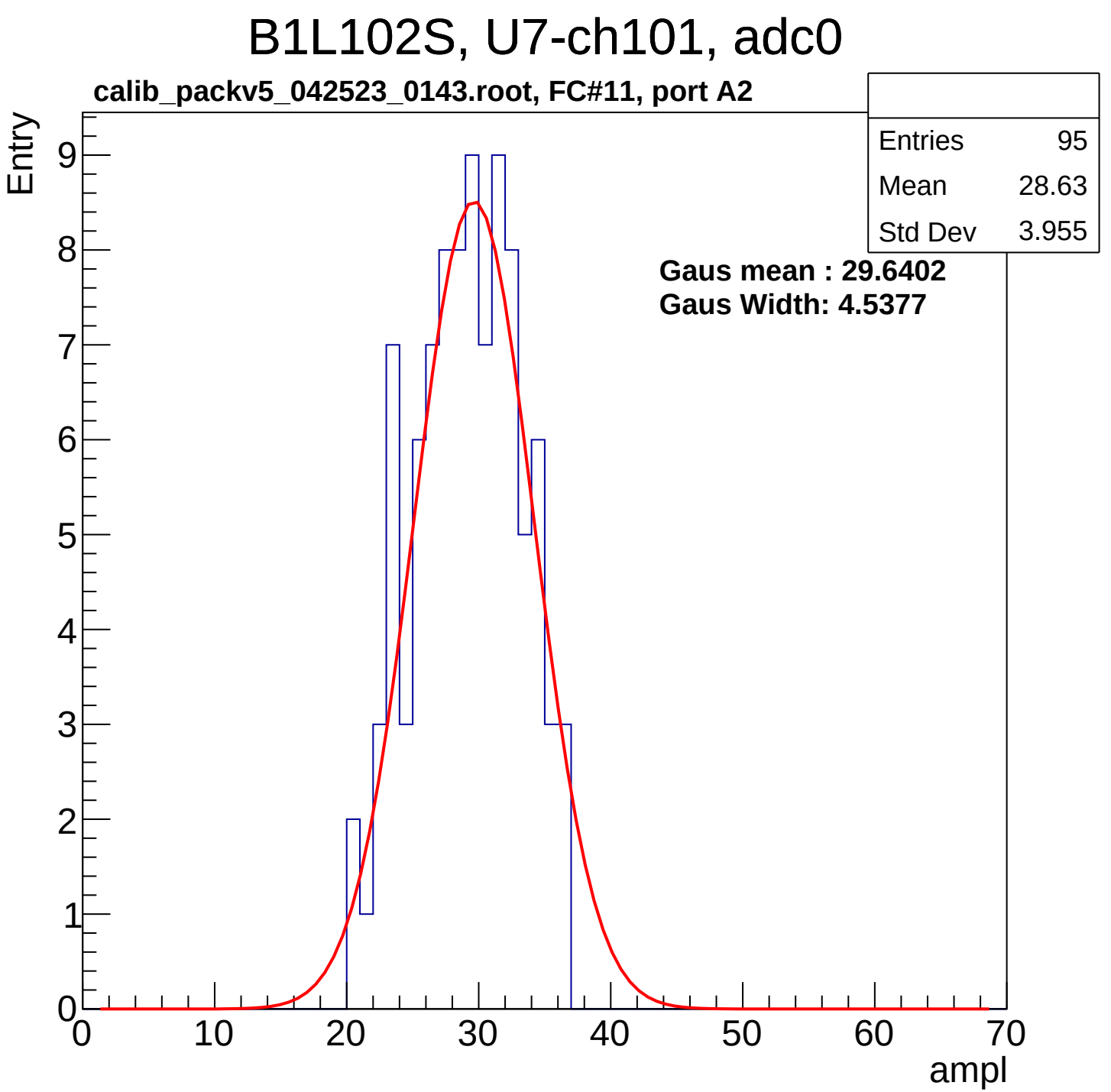
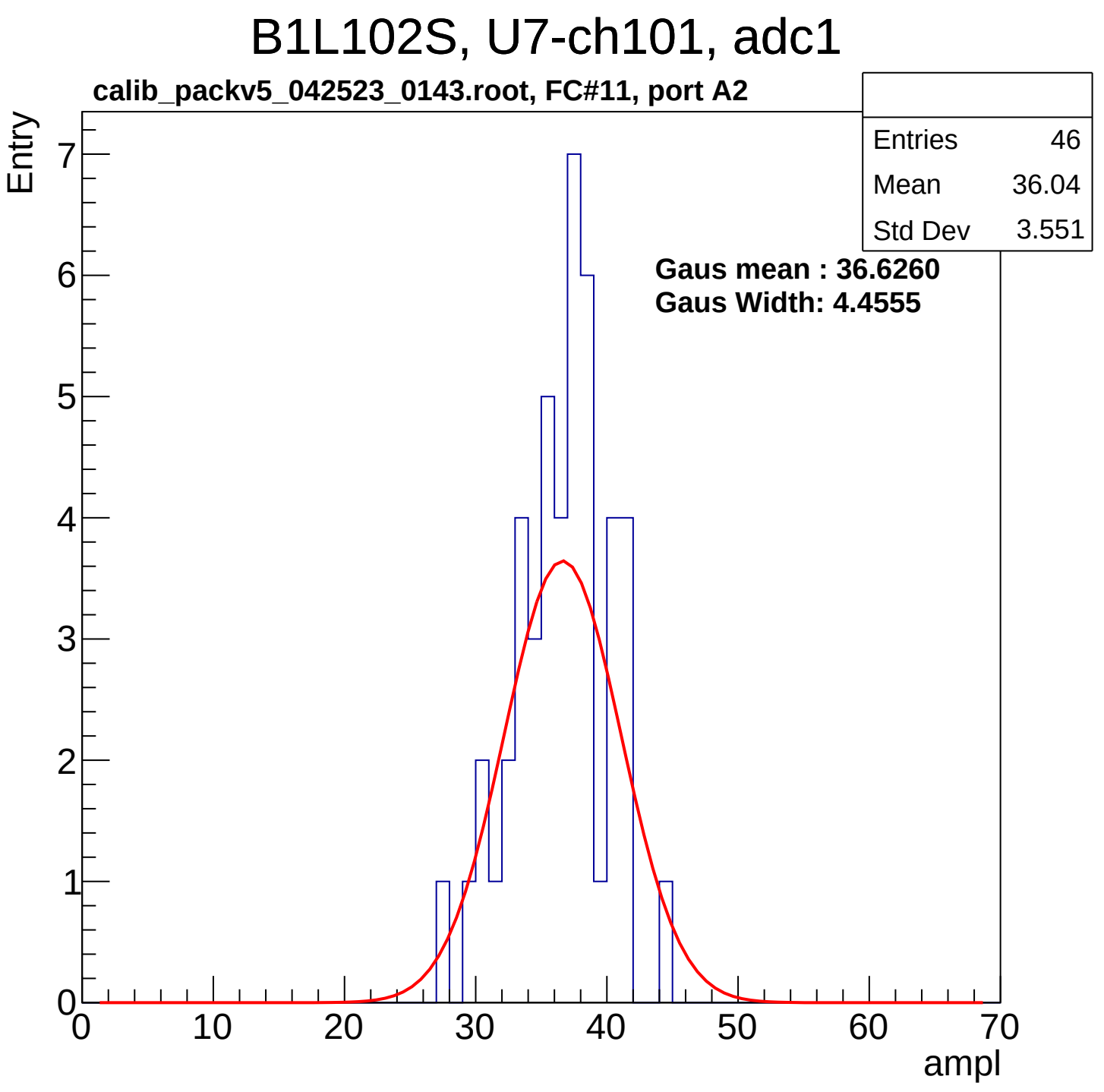
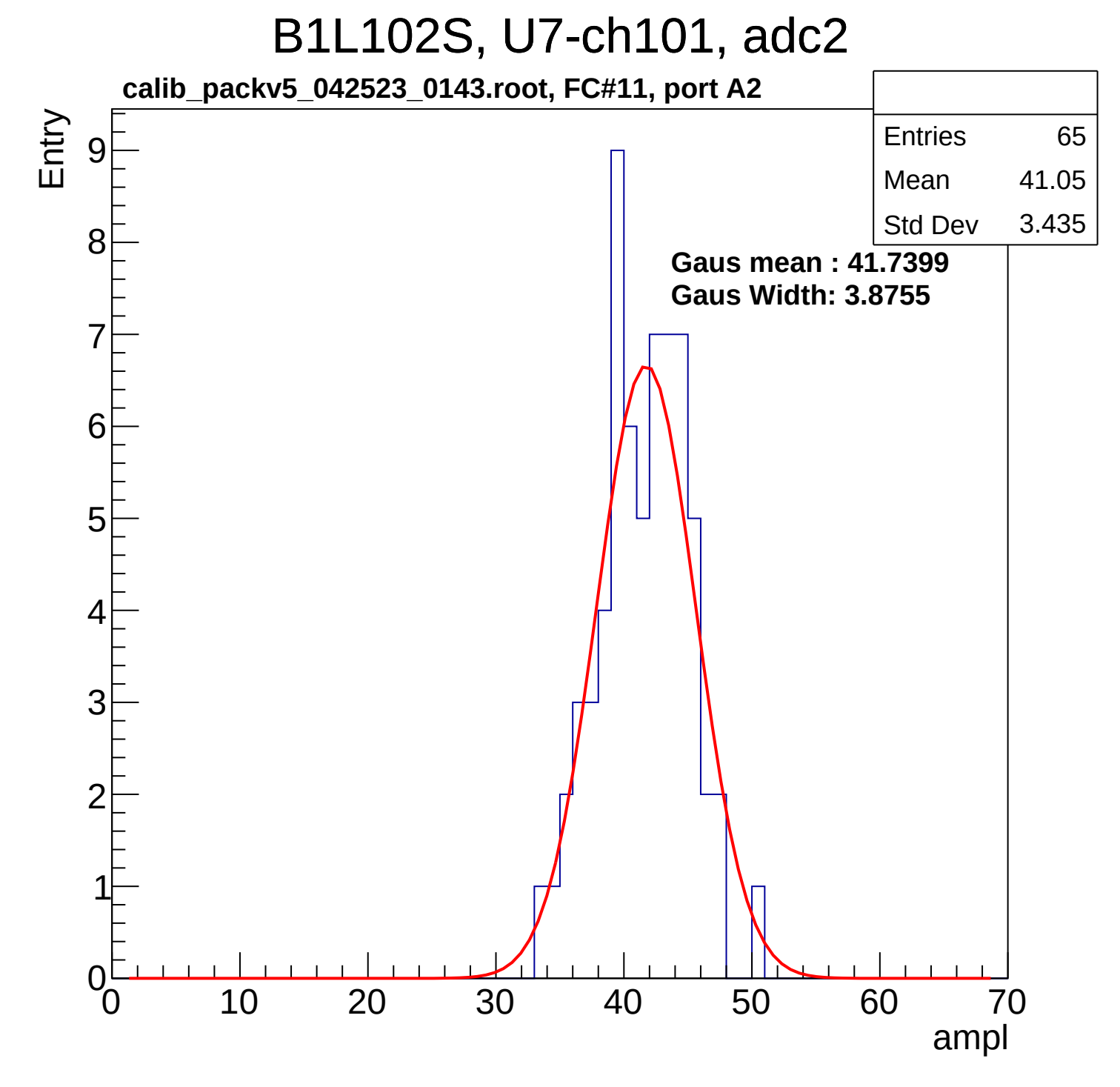
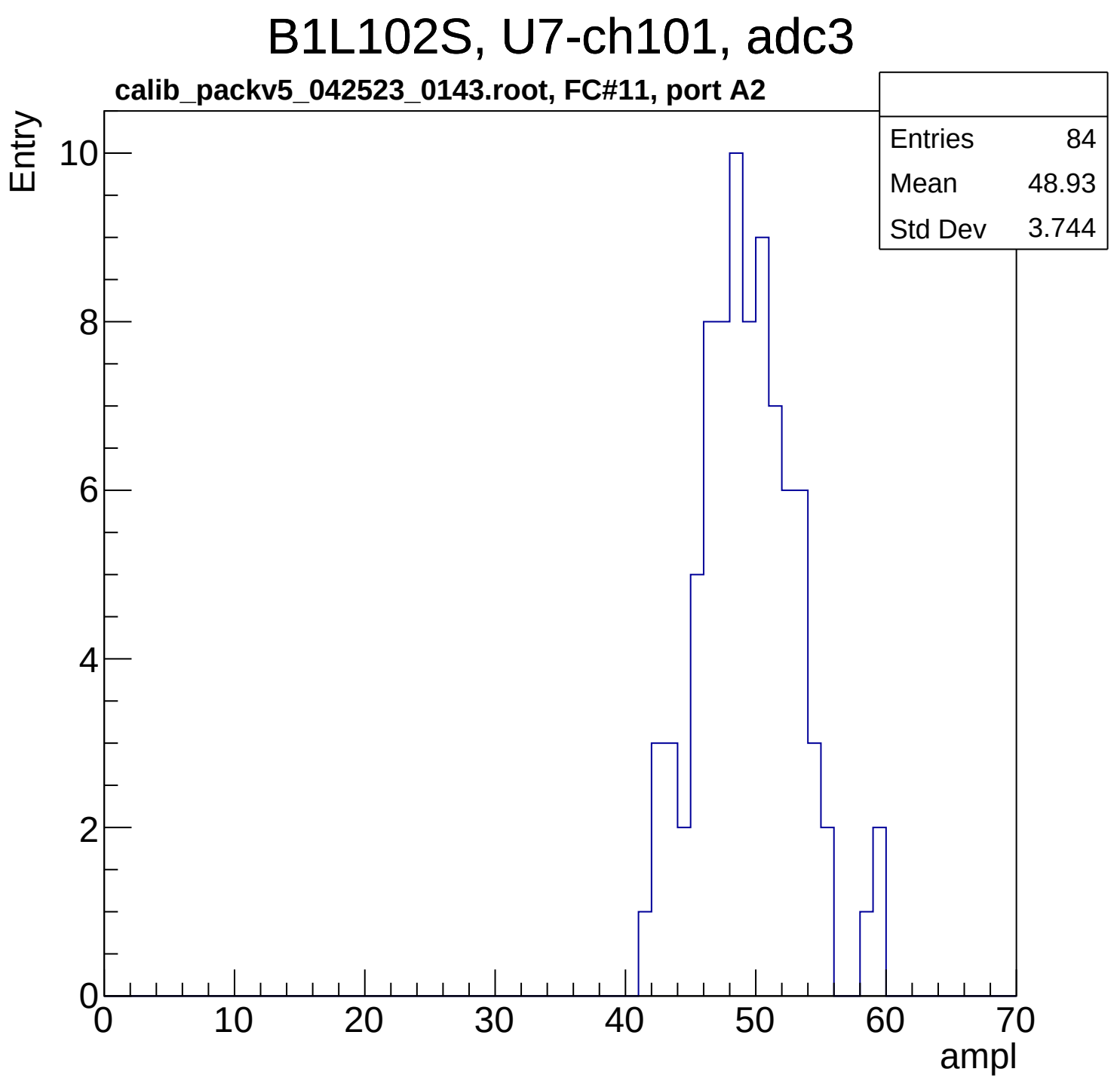

B1L102S, U7-ch100, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 13
Mean 56.46
Std Dev 16.4
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

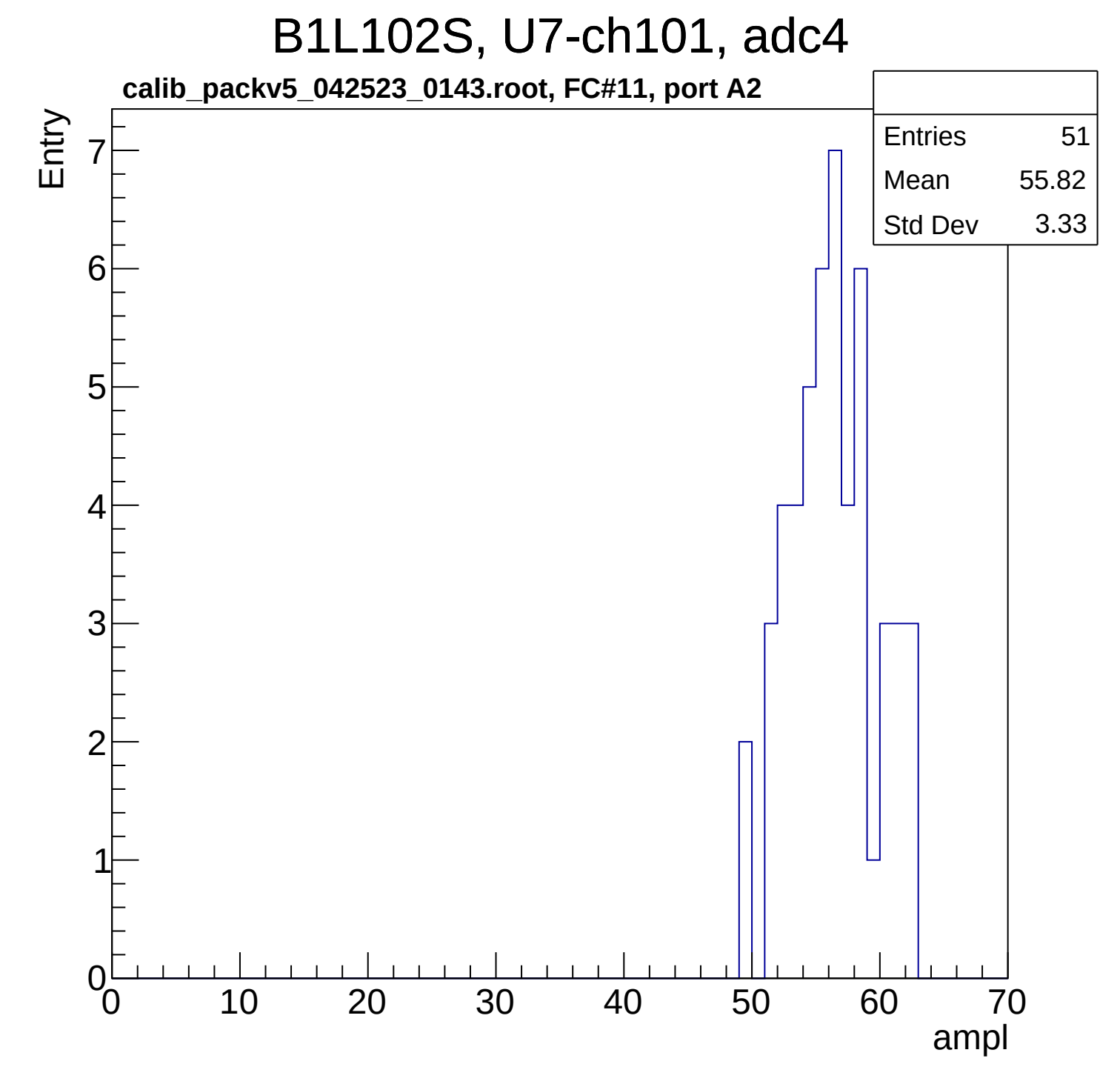

B1L102S, U7-ch100, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 2
Mean 61.5
Std Dev 0.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

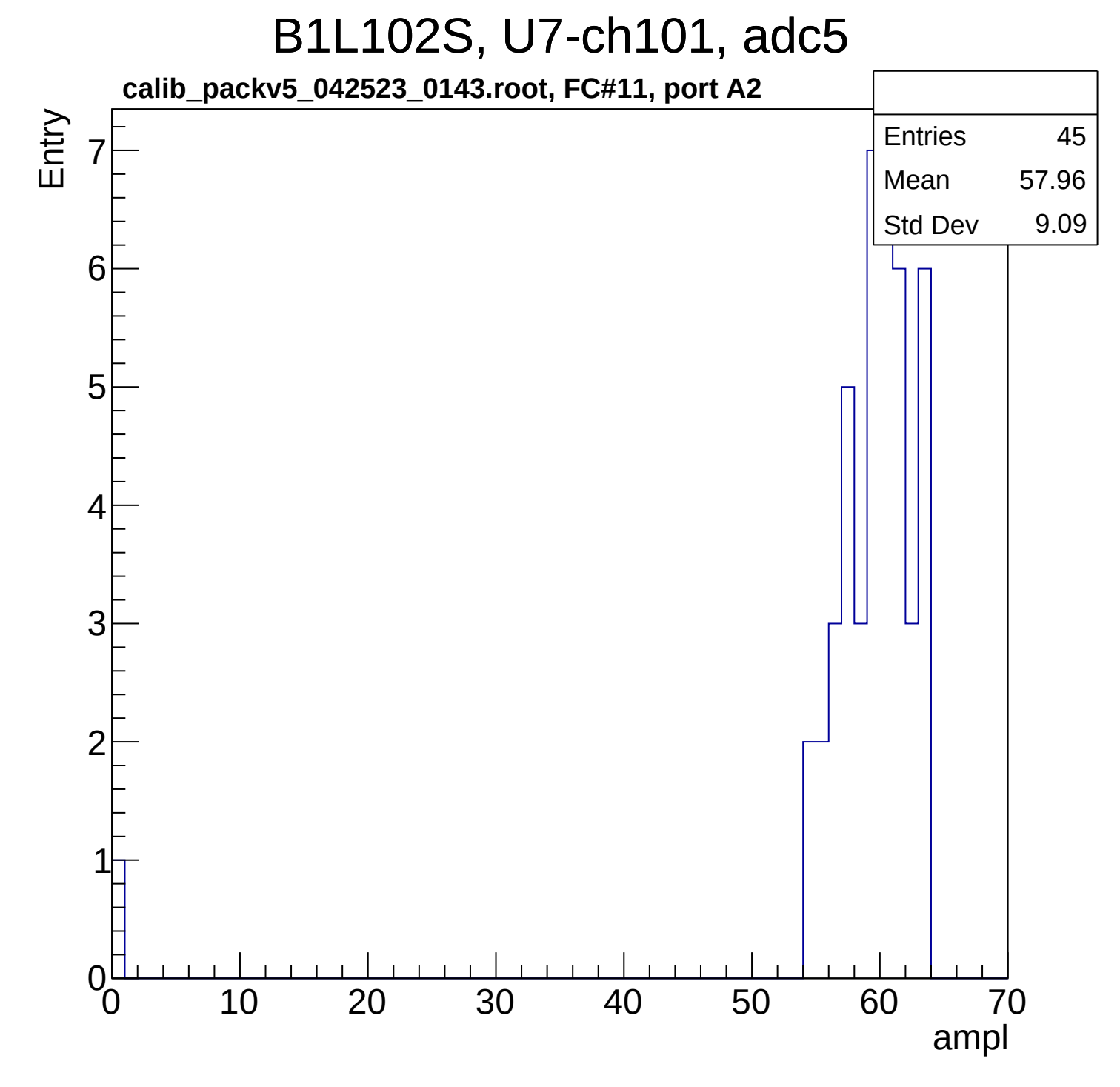

B1L102S, U7-ch101, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 95
Mean 28.63
Std Dev 3.955
Gaus mean : 29.6402
Gaus Width: 4.5377
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L102S, U7-ch101, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 46
Mean 36.04
Std Dev 3.551
Gaus mean : 36.6260
Gaus Width: 4.4555
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L102S, U7-ch101, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 65
Mean 41.05
Std Dev 3.435
Gaus mean : 41.7399
Gaus Width: 3.8755
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L102S, U7-ch101, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 84
Mean 48.93
Std Dev 3.744
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L102S, U7-ch101, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 51
Mean 55.82
Std Dev 3.33
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L102S, U7-ch101, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 45
Mean 57.96
Std Dev 9.09
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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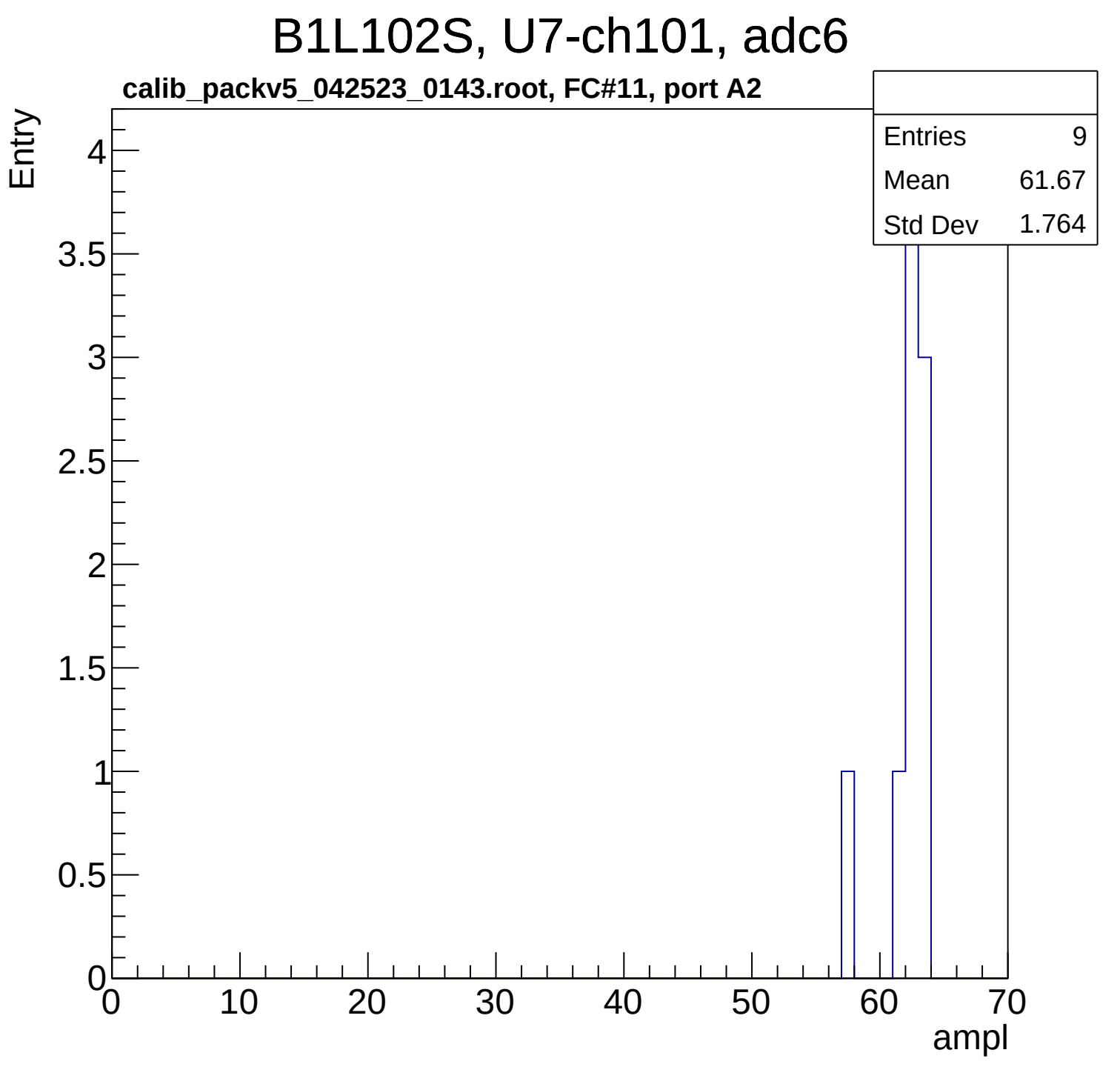
B1L102S, U7-ch101, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 9
Mean 61.67
Std Dev 1.764
Entry
ampl
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0.5
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1.5
2
2.5
3
3.5
4
0
10
20
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40
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60
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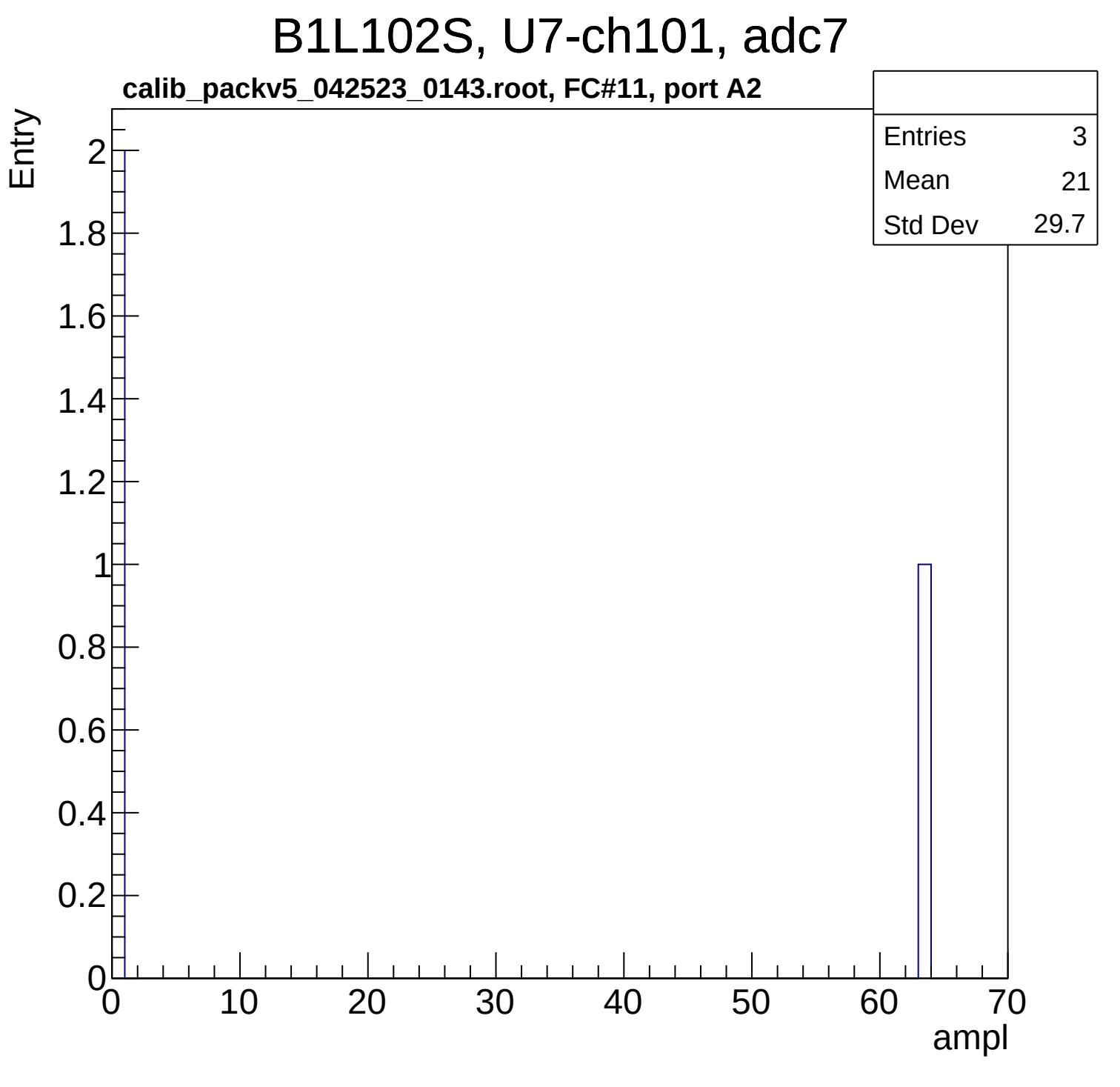
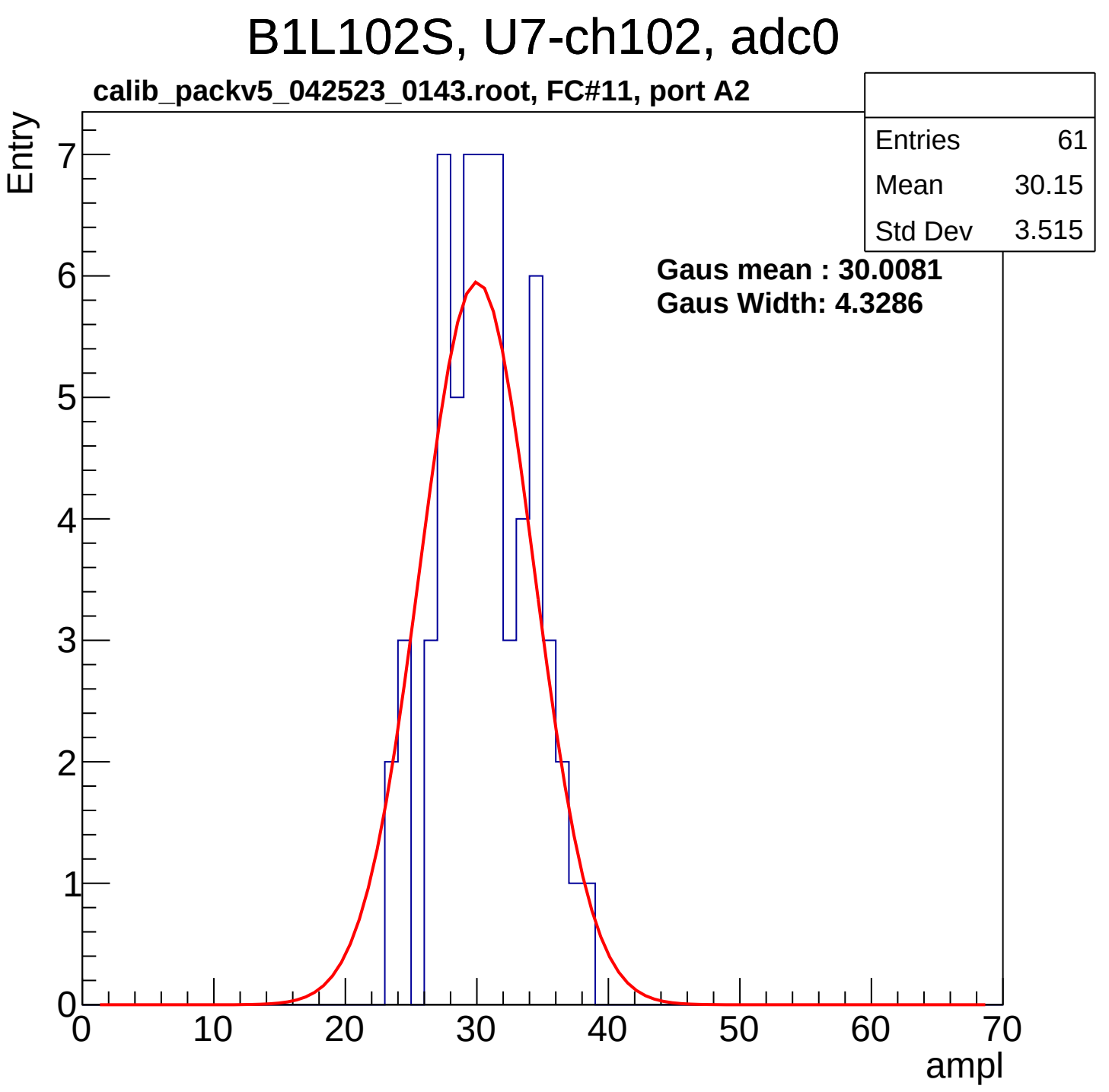
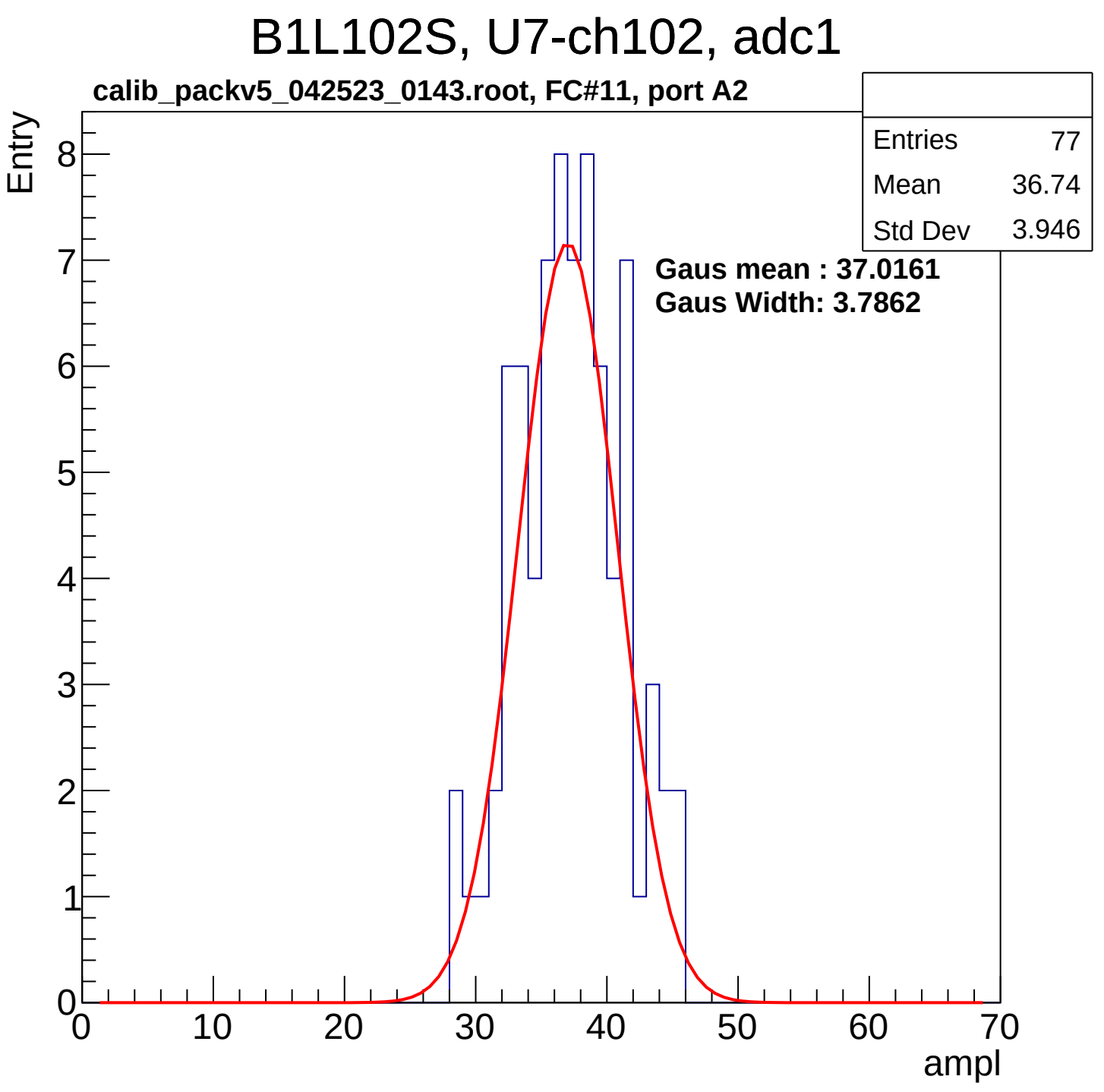
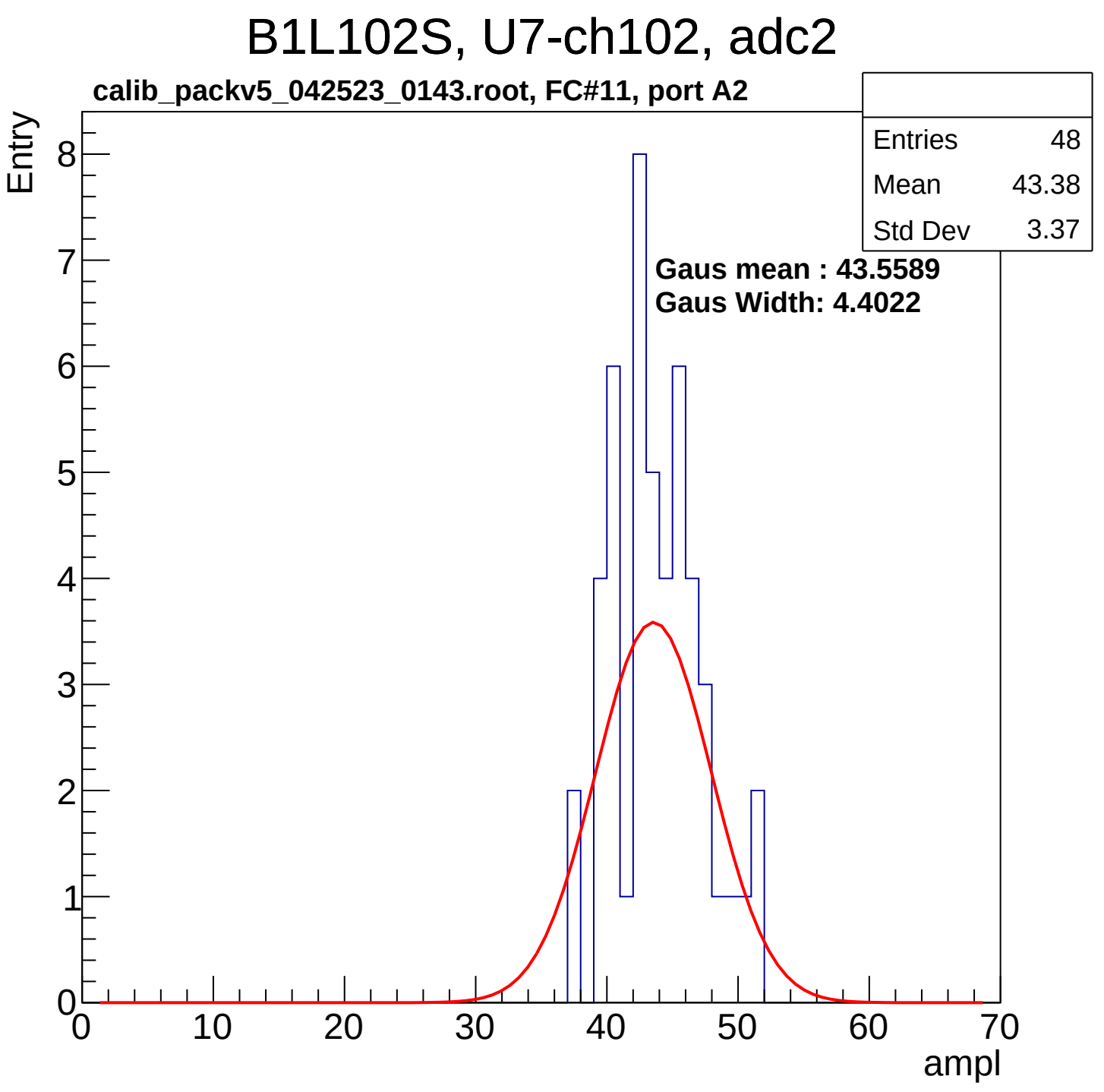
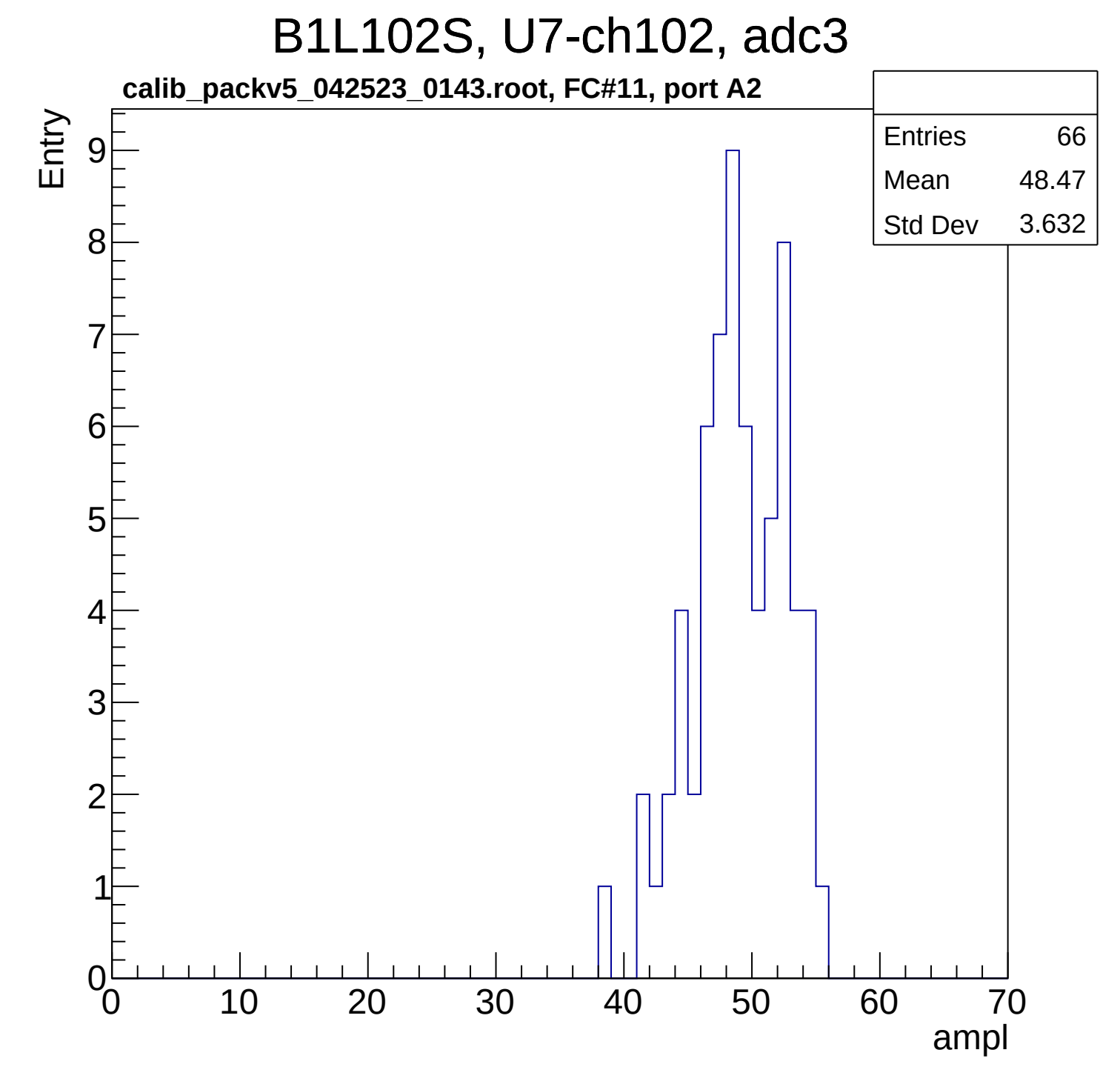

B1L102S, U7-ch101, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 3
Mean 21
Std Dev 29.7
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L102S, U7-ch102, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 61
Mean 30.15
Std Dev 3.515
Gaus mean : 30.0081
Gaus Width: 4.3286
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L102S, U7-ch102, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 77
Mean 36.74
Std Dev 3.946
Gaus mean : 37.0161
Gaus Width: 3.7862
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L102S, U7-ch102, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 48
Mean 43.38
Std Dev 3.37
Gaus mean : 43.5589
Gaus Width: 4.4022
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L102S, U7-ch102, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 66
Mean 48.47
Std Dev 3.632
Entry
ampl
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2
3
4
5
6
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9
0
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60
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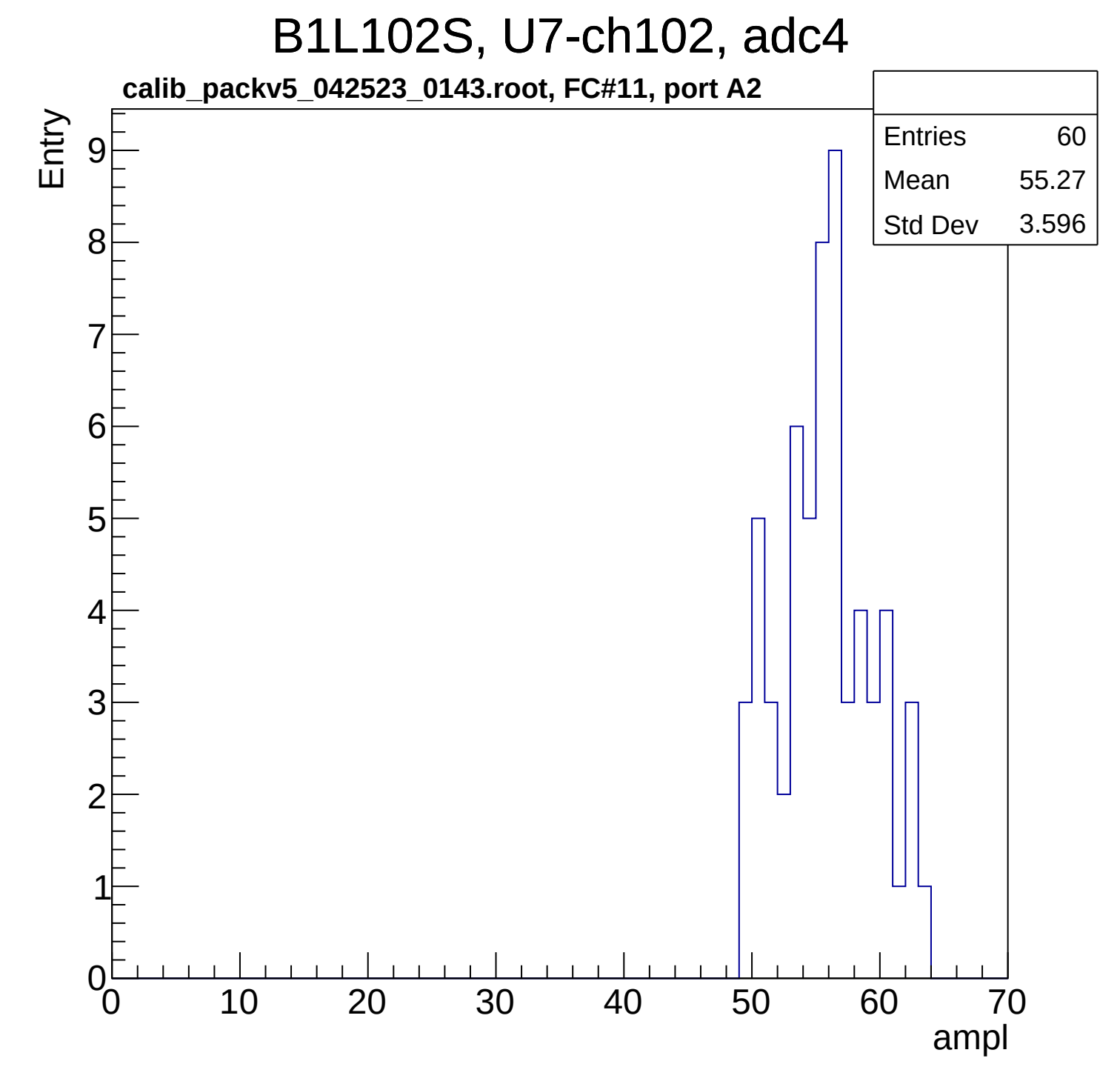
B1L102S, U7-ch102, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 60
Mean 55.27
Std Dev 3.596
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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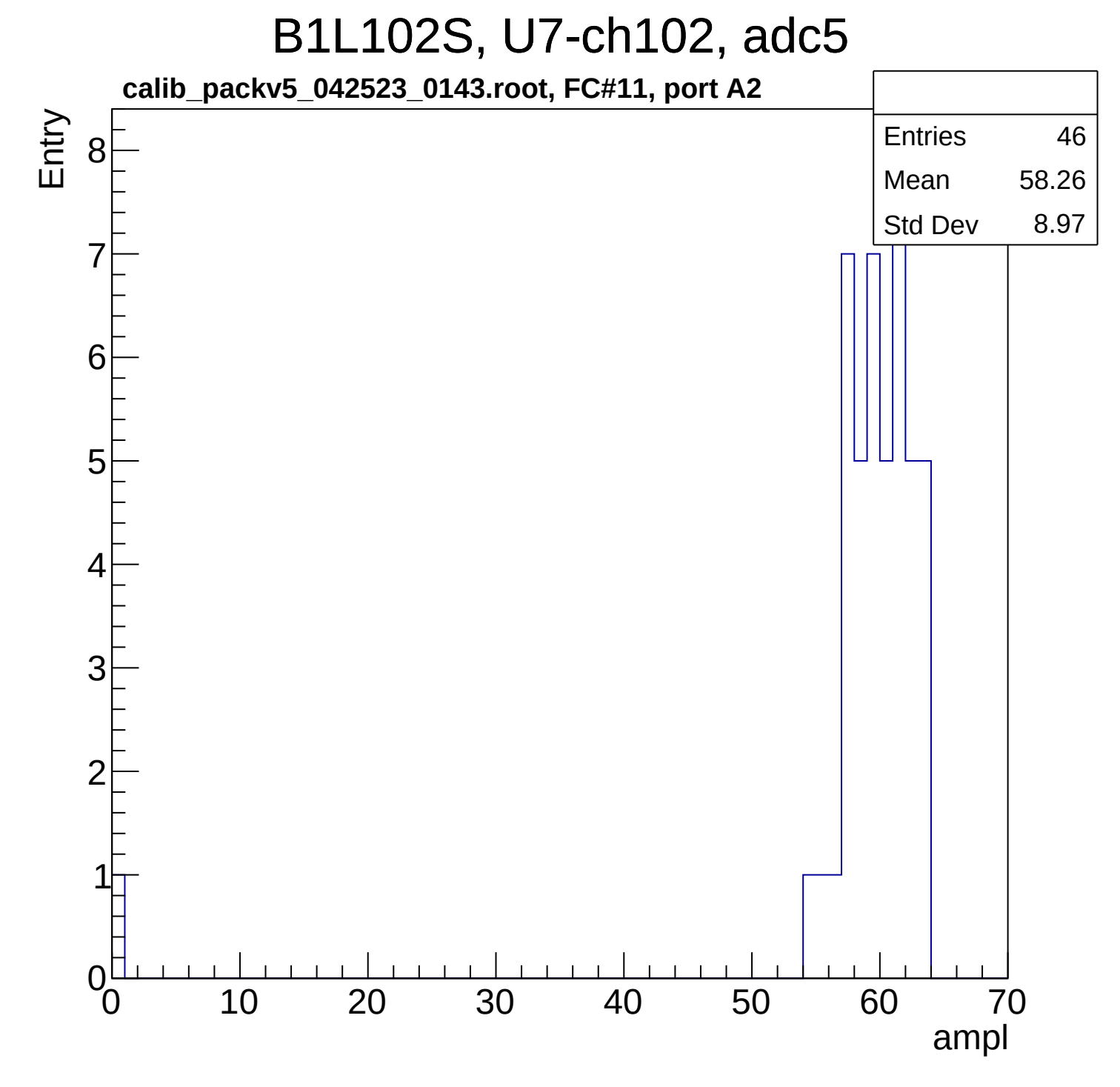
B1L102S, U7-ch102, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 46
Mean 58.26
Std Dev 8.97
Entry
ampl
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1
2
3
4
5
6
7
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0
10
20
30
40
50
60
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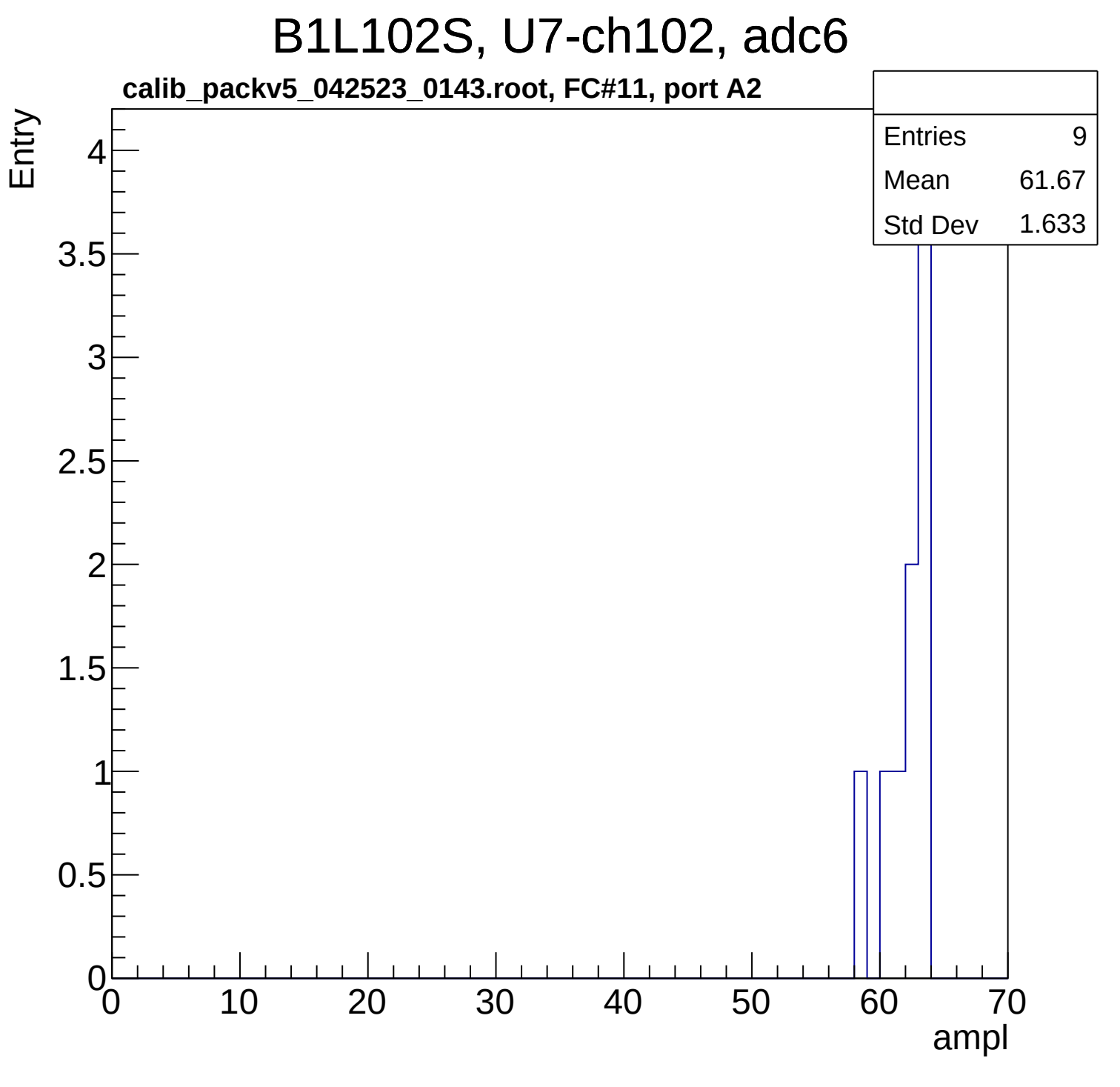
B1L102S, U7-ch102, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 9
Mean 61.67
Std Dev 1.633
Entry
ampl
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0.5
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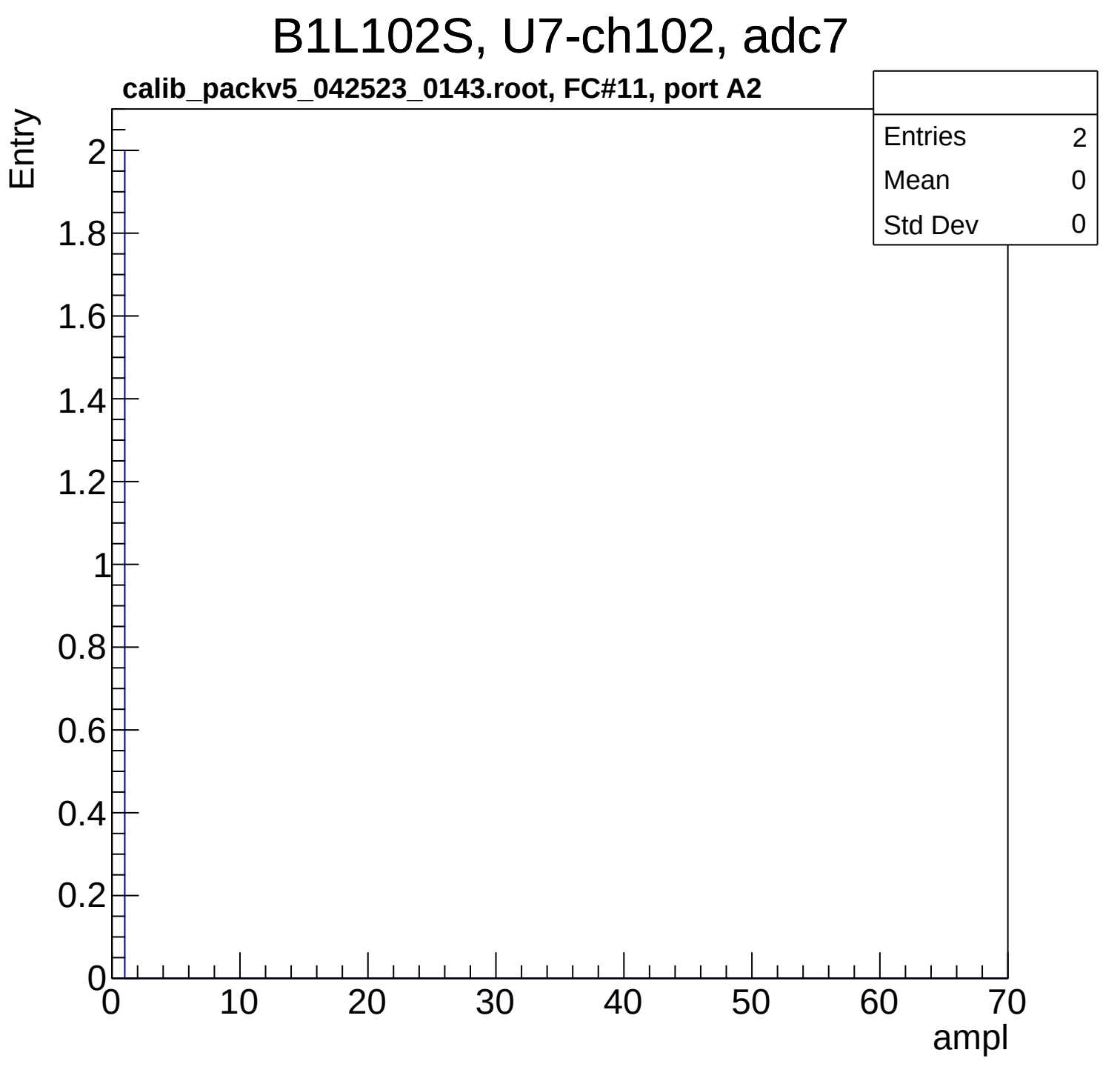
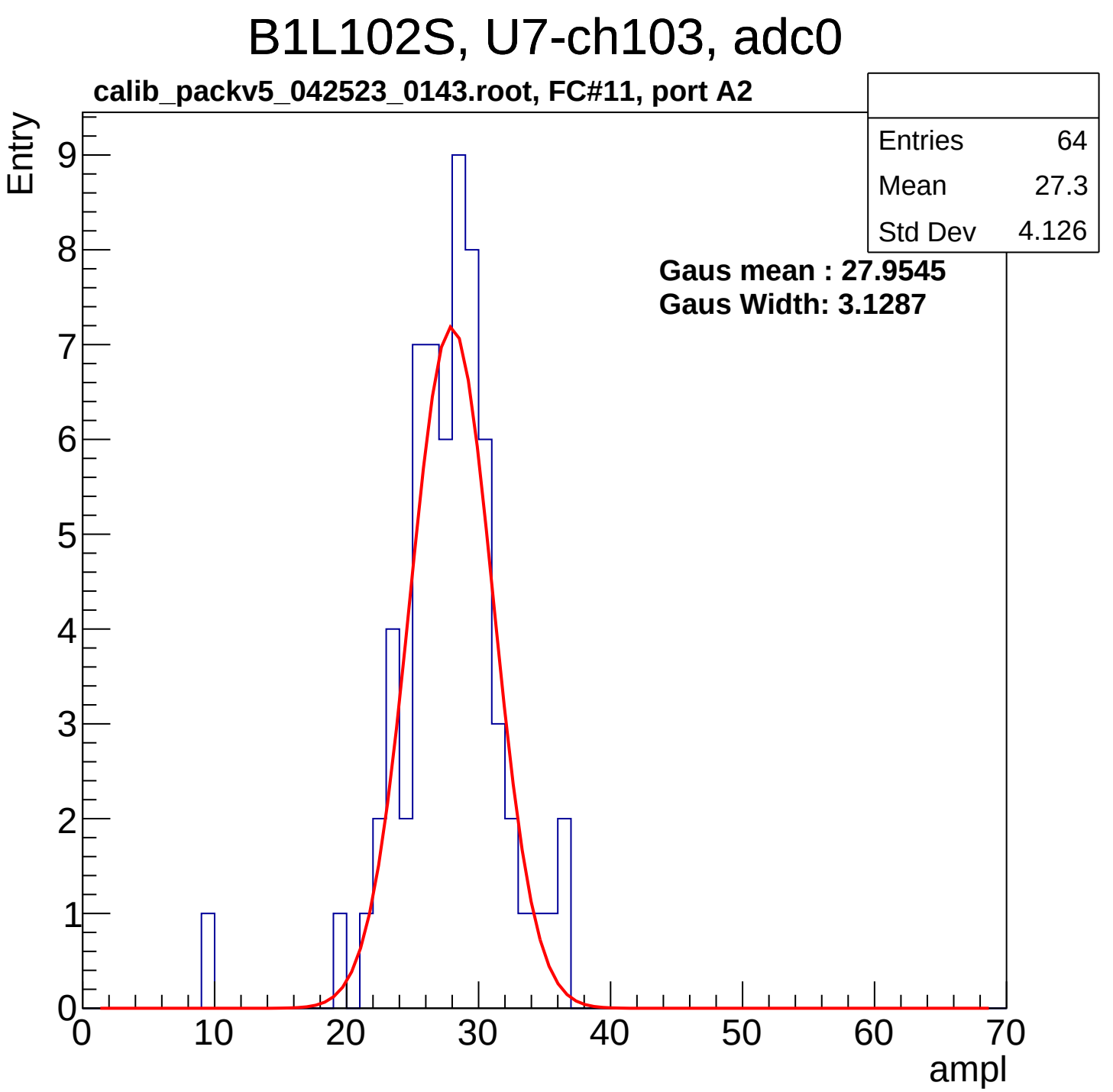
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L102S, U7-ch102, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 2
Mean 0
Std Dev 0
Entry
2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U7-ch103, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 64
Mean 27.3
Std Dev 4.126
Gaus mean : 27.9545
Gaus Width: 3.1287
Entry
ampl
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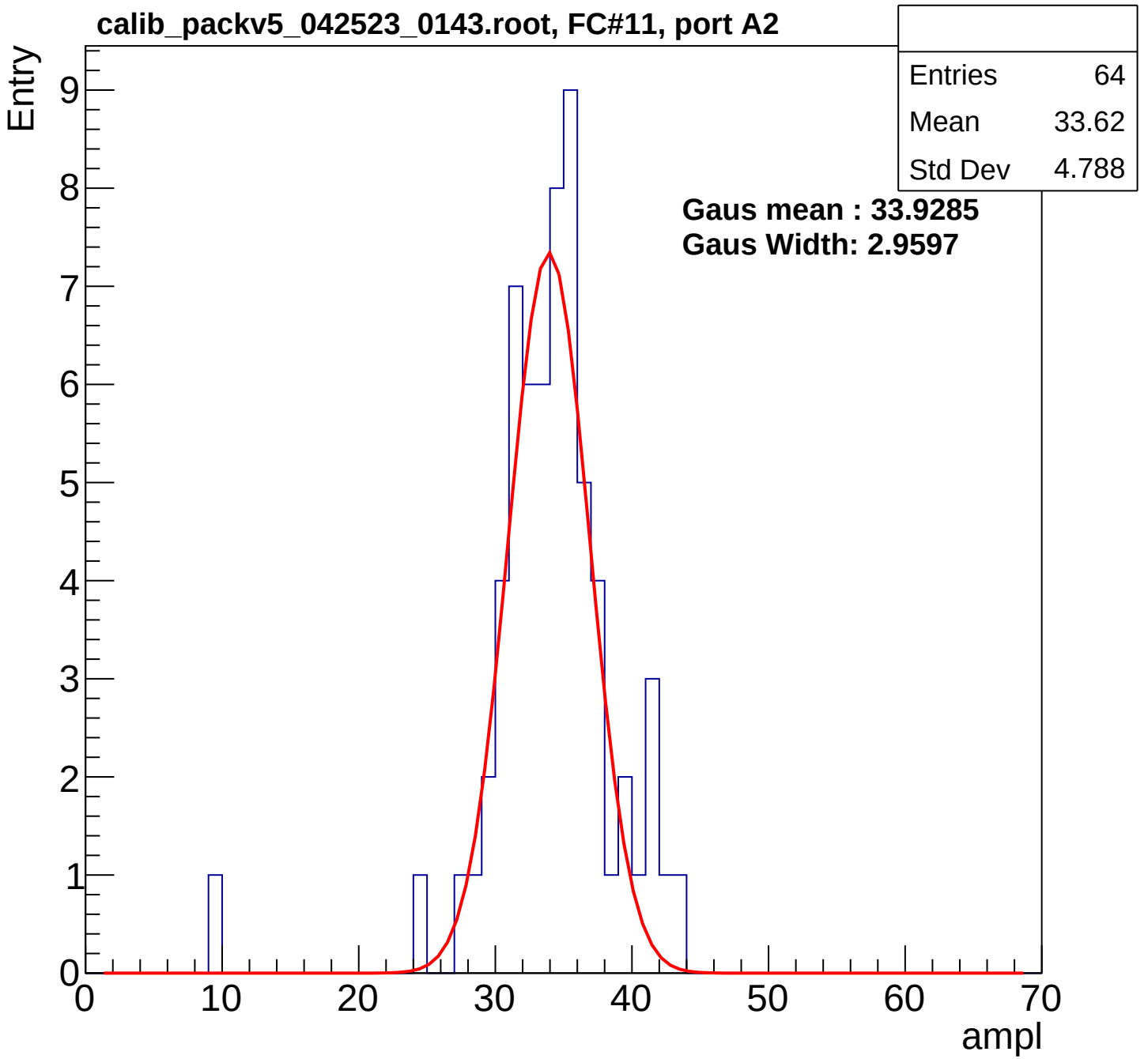
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L102S, U7-ch103, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 64
Mean 33.62
Std Dev 4.788
Gaus mean : 33.9285
Gaus Width: 2.9597
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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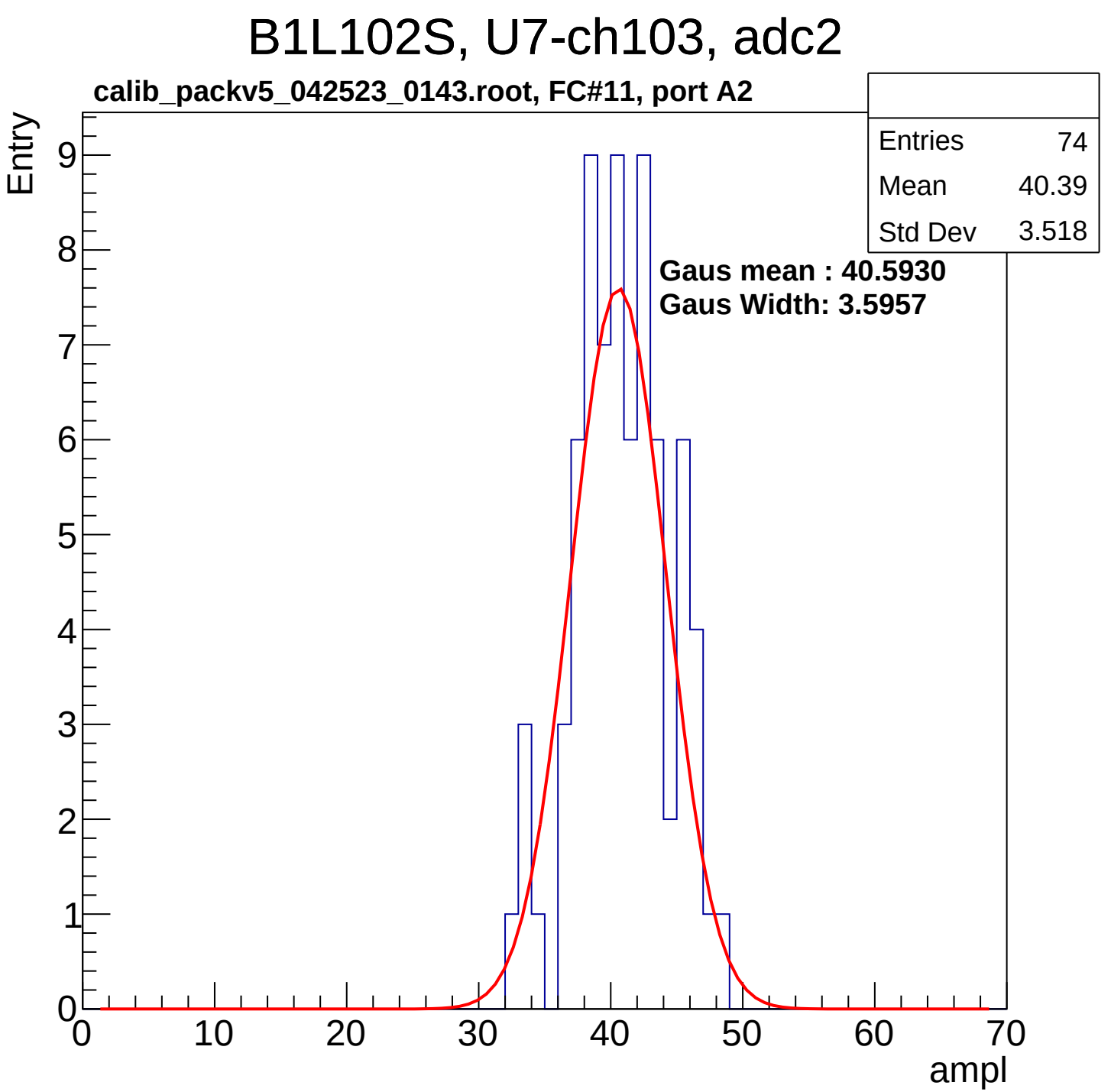
B1L102S, U7-ch103, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 74
Mean 40.39
Std Dev 3.518
Gaus mean : 40.5930
Gaus Width: 3.5957
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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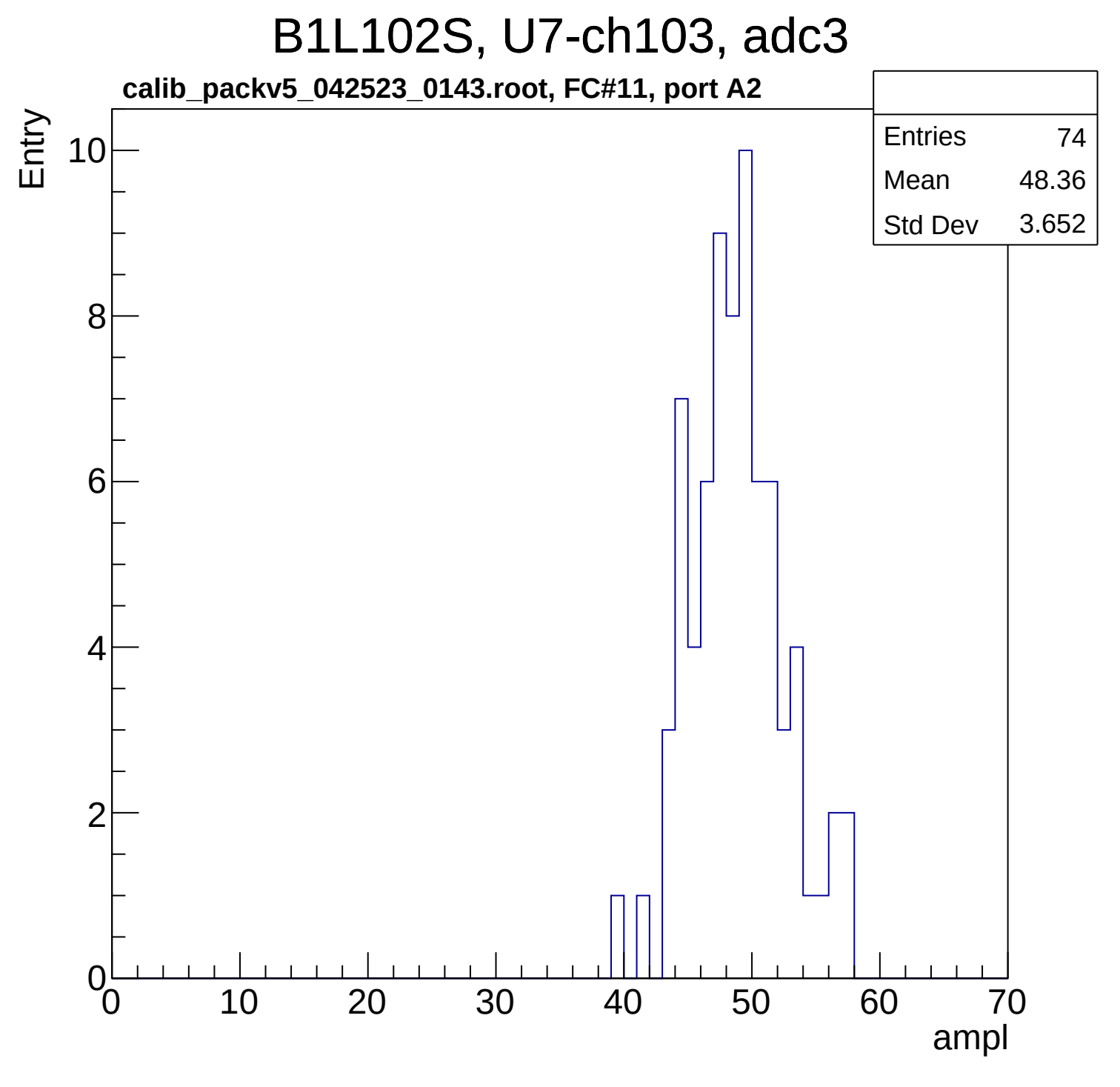
B1L102S, U7-ch103, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 74
Mean 48.36
Std Dev 3.652
Entry
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2
4
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10
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10
20
30
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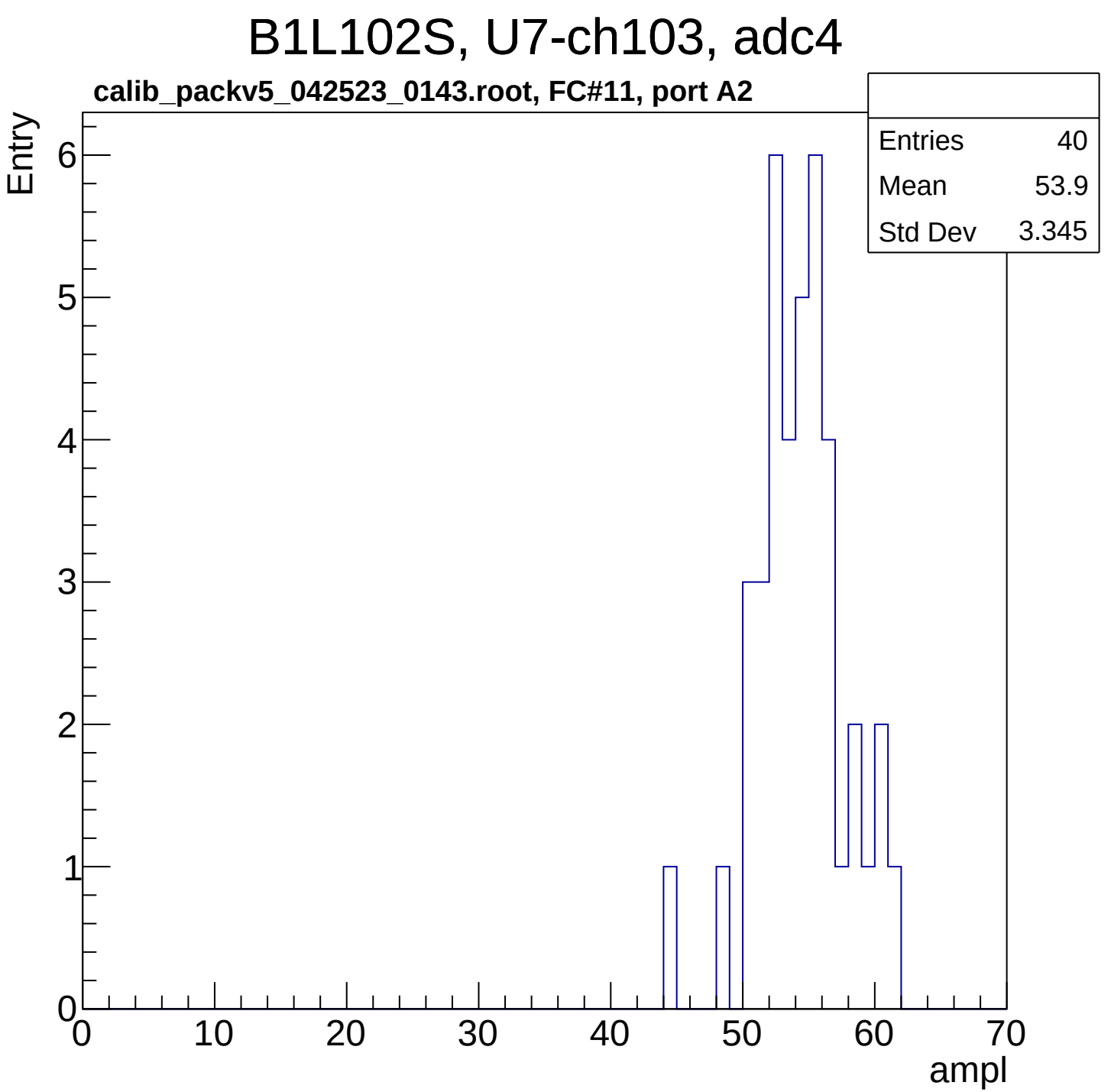
50
60
70
ampl


B1L102S, U7-ch103, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 40
Mean 53.9
Std Dev 3.345
Entry
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1
2
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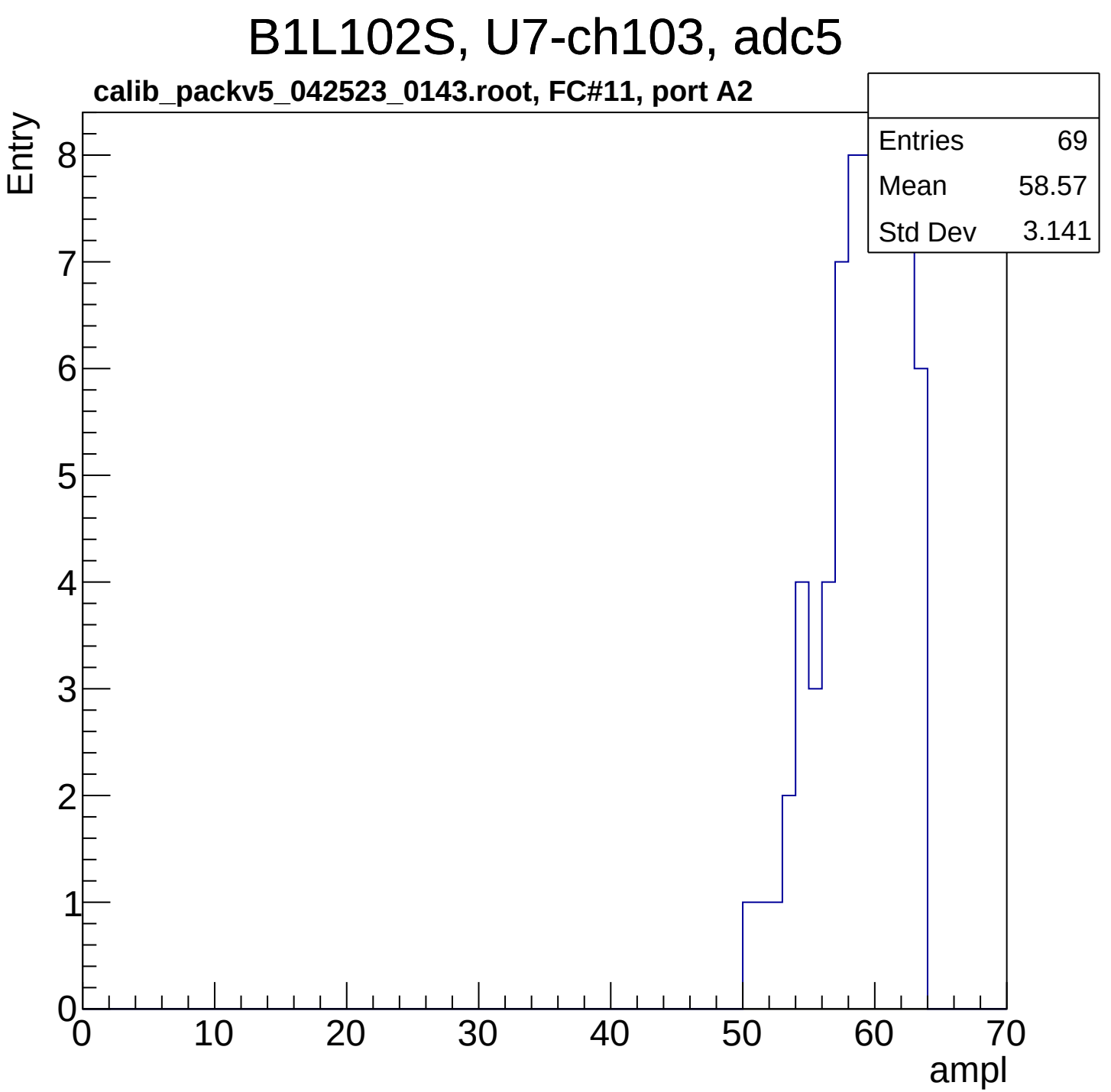
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L102S, U7-ch103, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 69
Mean 58.57
Std Dev 3.141
Entry
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2
3
4
5
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7
8
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10
20
30
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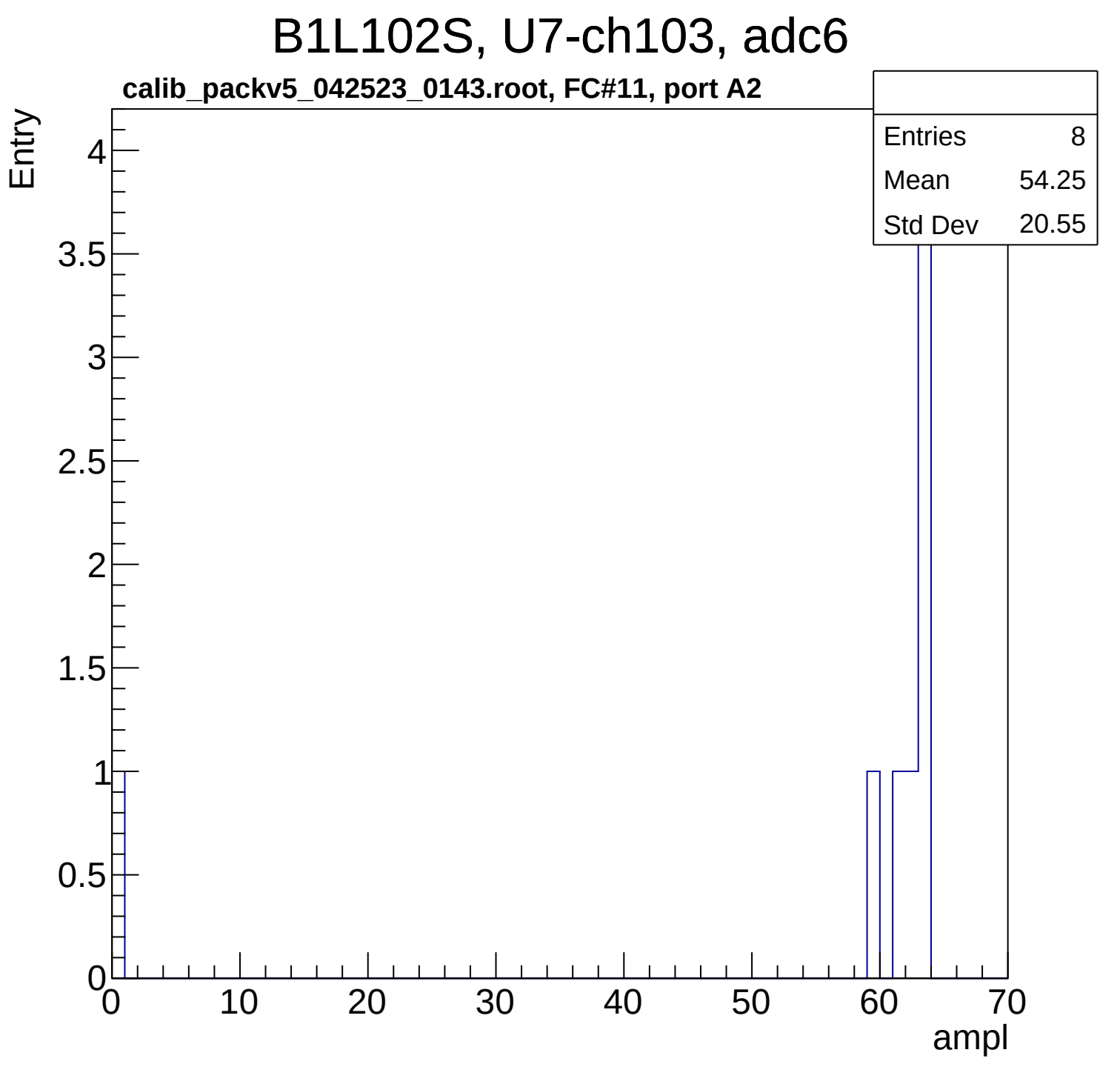
50
60
70
ampl


B1L102S, U7-ch103, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 8
Mean 54.25
Std Dev 20.55
Entry
ampl
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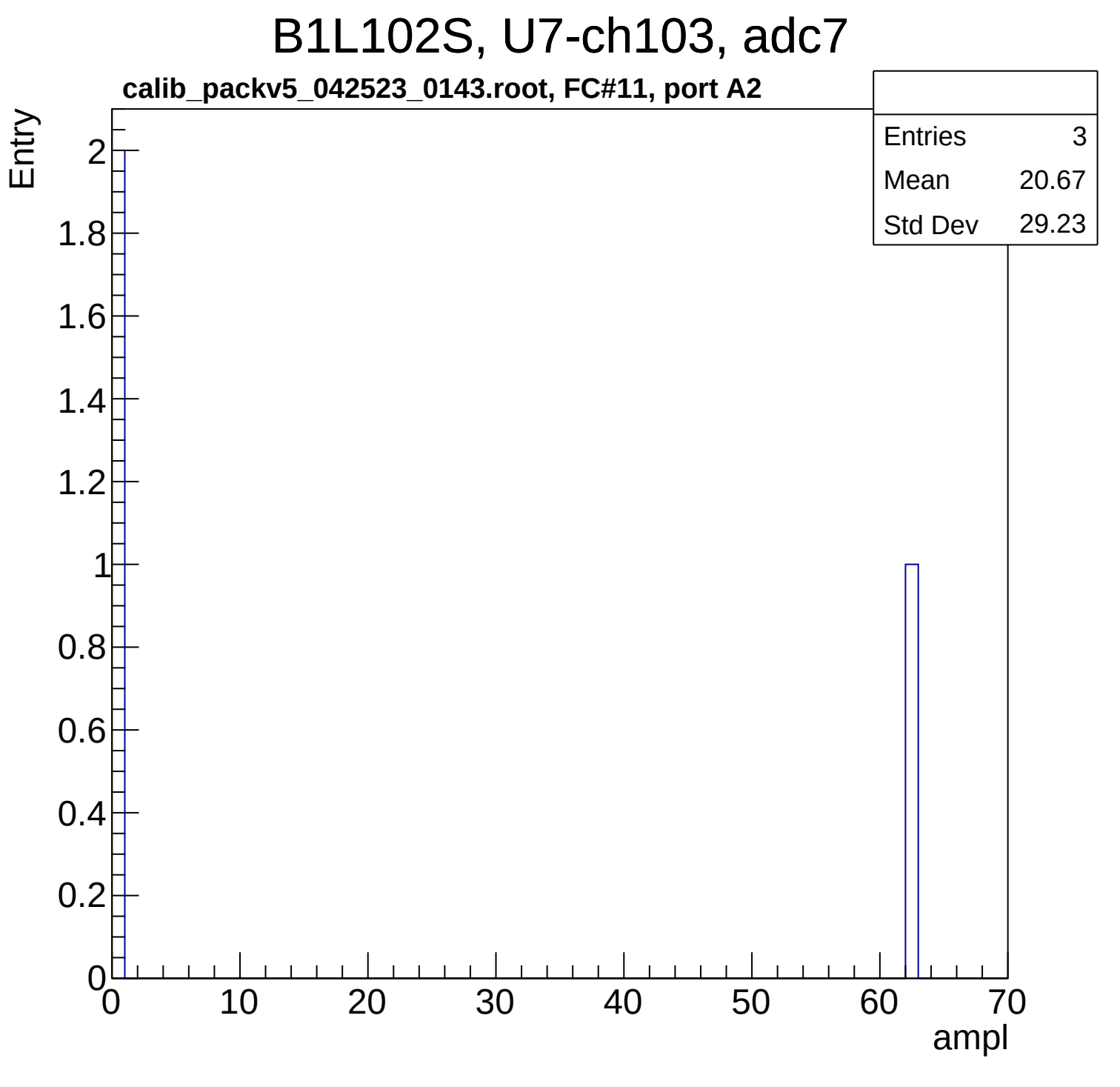
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L102S, U7-ch103, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 3
Mean 20.67
Std Dev 29.23
Entry
ampl
0
0.2
0.4
0.6
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1
1.2
1.4
1.6
1.8
2
0
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40
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60
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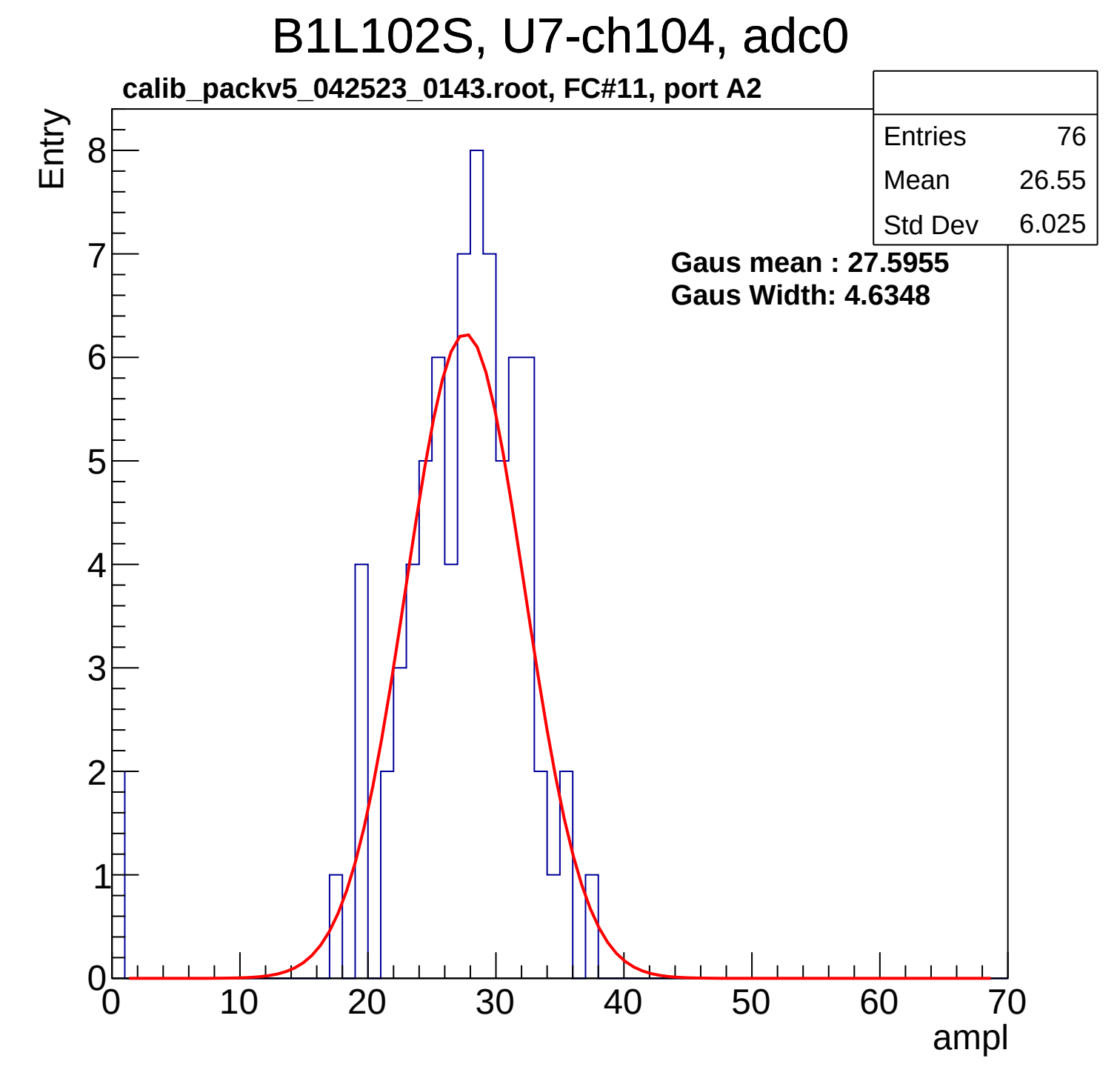
B1L102S, U7-ch104, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 76
Mean 26.55
Std Dev 6.025
Gaus mean : 27.5955
Gaus Width: 4.6348
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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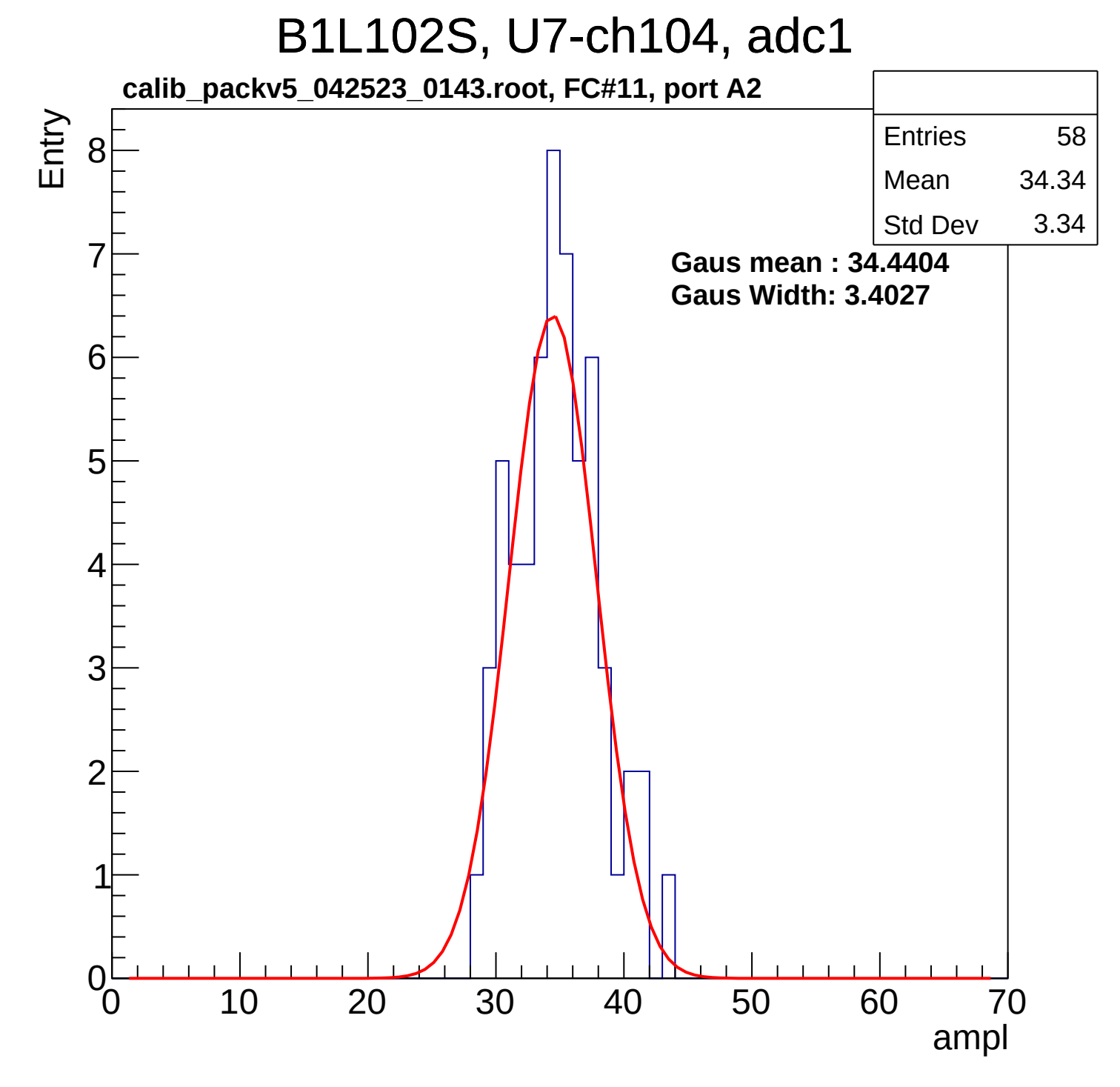
B1L102S, U7-ch104, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 58
Mean 34.34
Std Dev 3.34
Gaus mean : 34.4404
Gaus Width: 3.4027
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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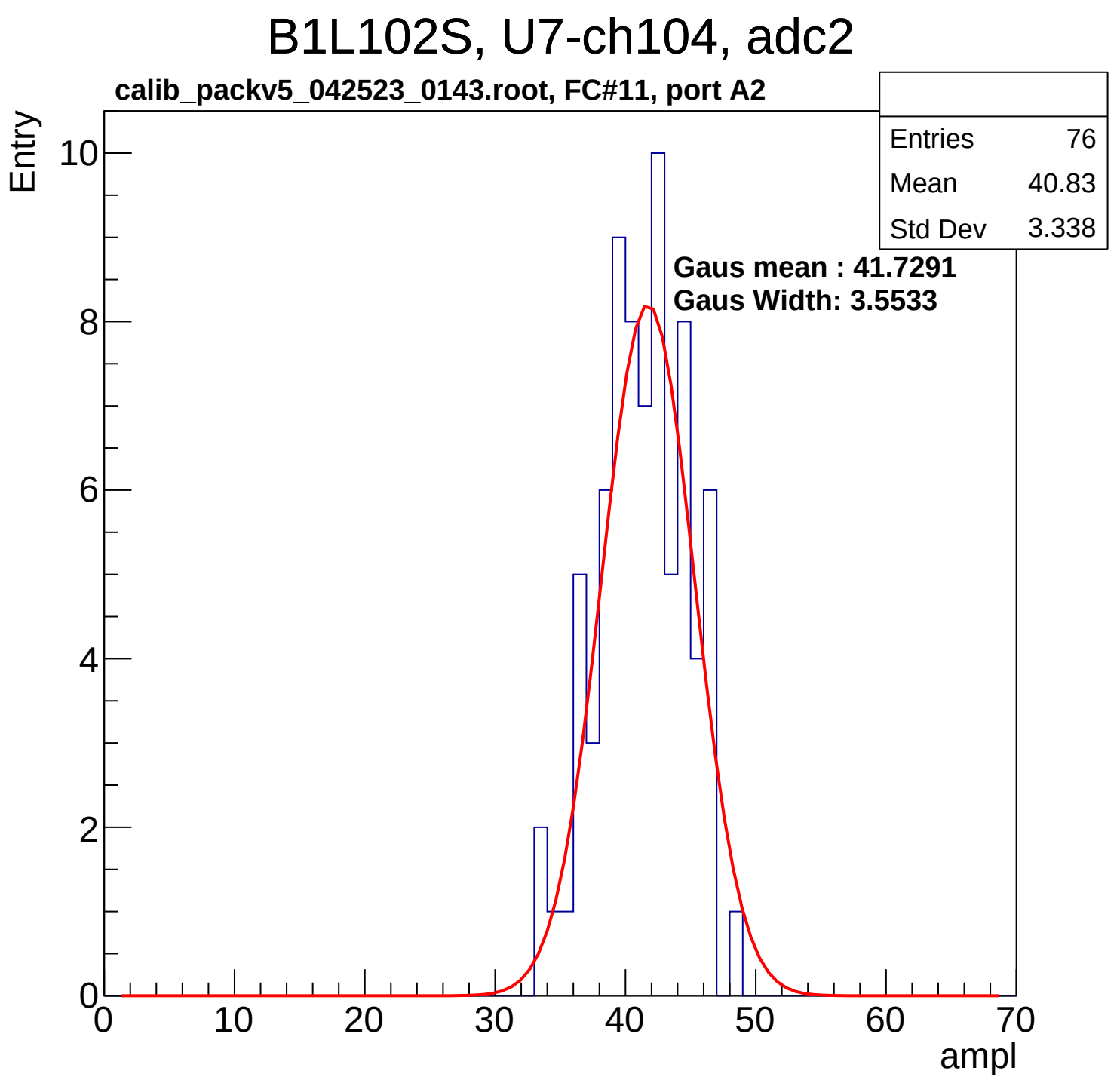
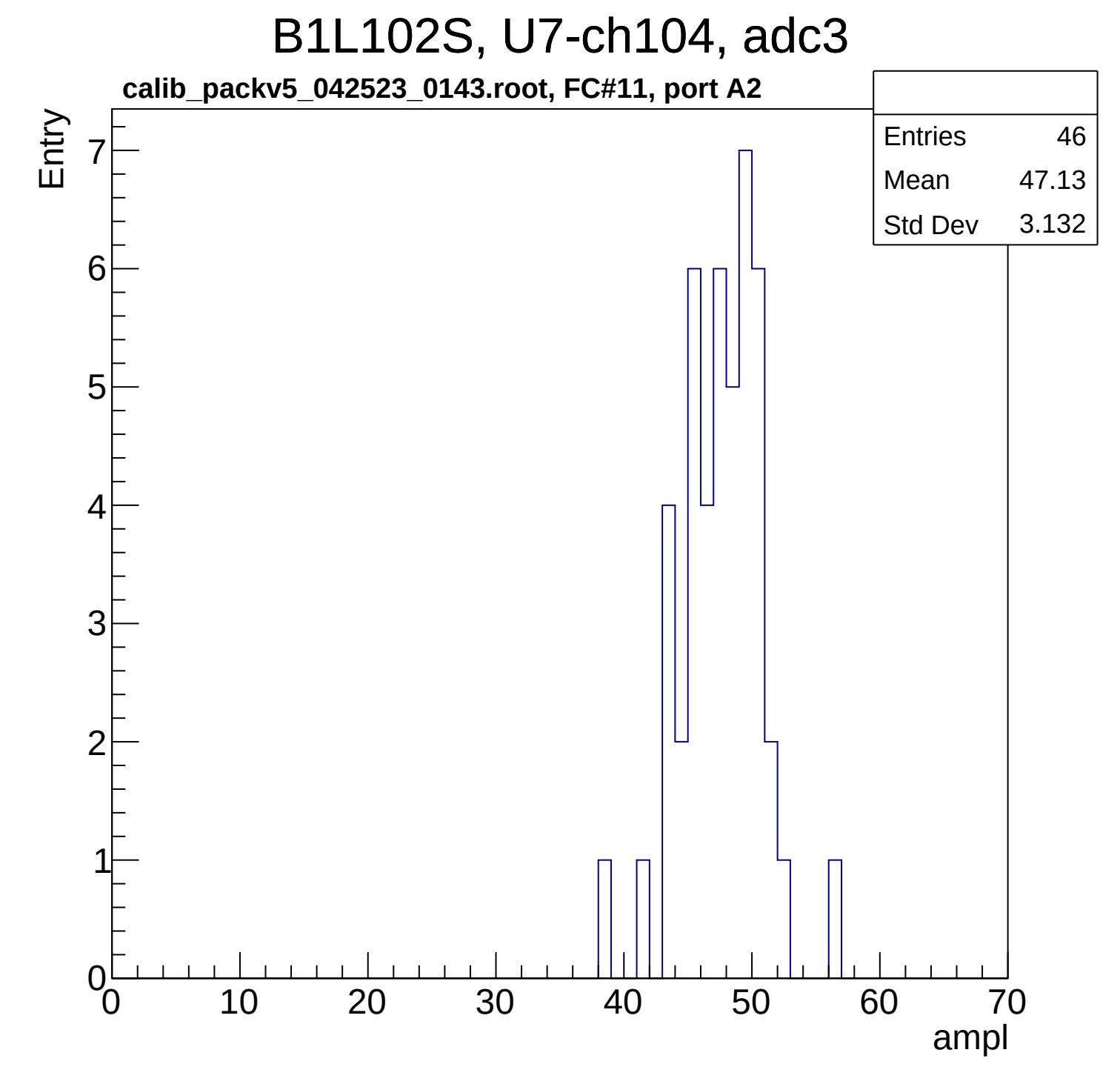

B1L102S, U7-ch104, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 76
Mean 40.83
Std Dev 3.338
Gaus mean : 41.7291
Gaus Width: 3.5533
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L102S, U7-ch104, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 46
Mean 47.13
Std Dev 3.132
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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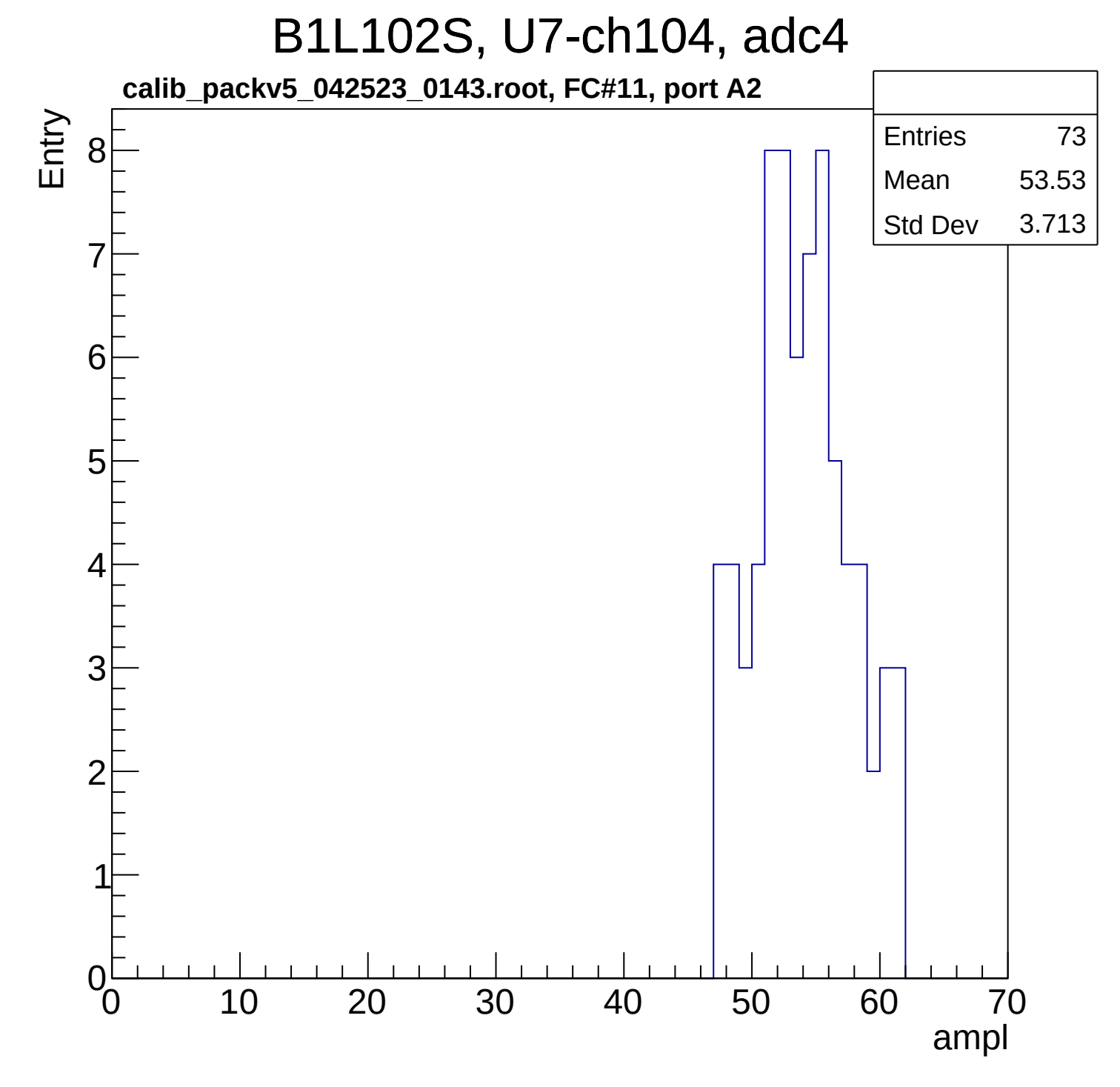
B1L102S, U7-ch104, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 73
Mean 53.53
Std Dev 3.713
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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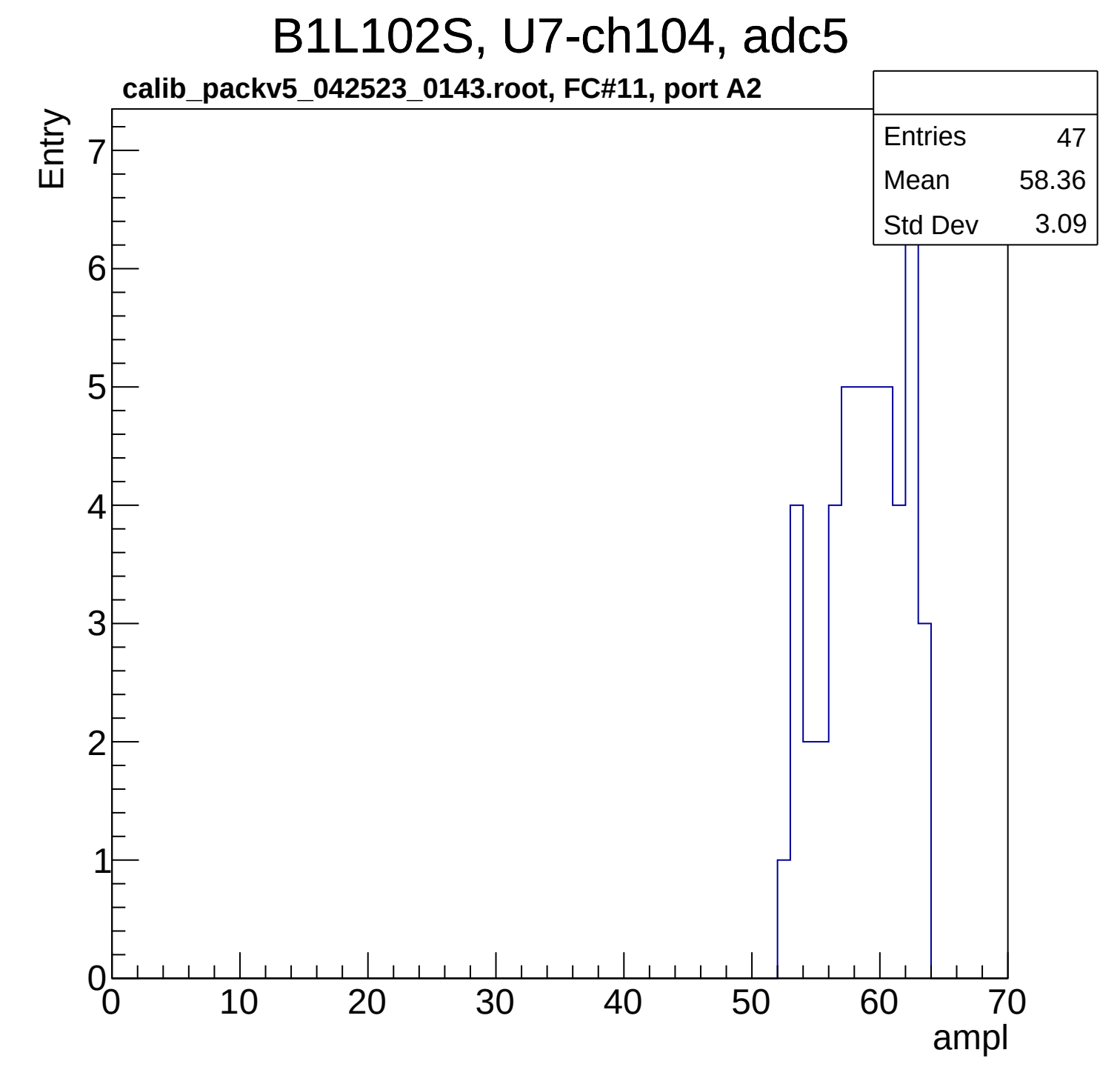
B1L102S, U7-ch104, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 47
Mean 58.36
Std Dev 3.09
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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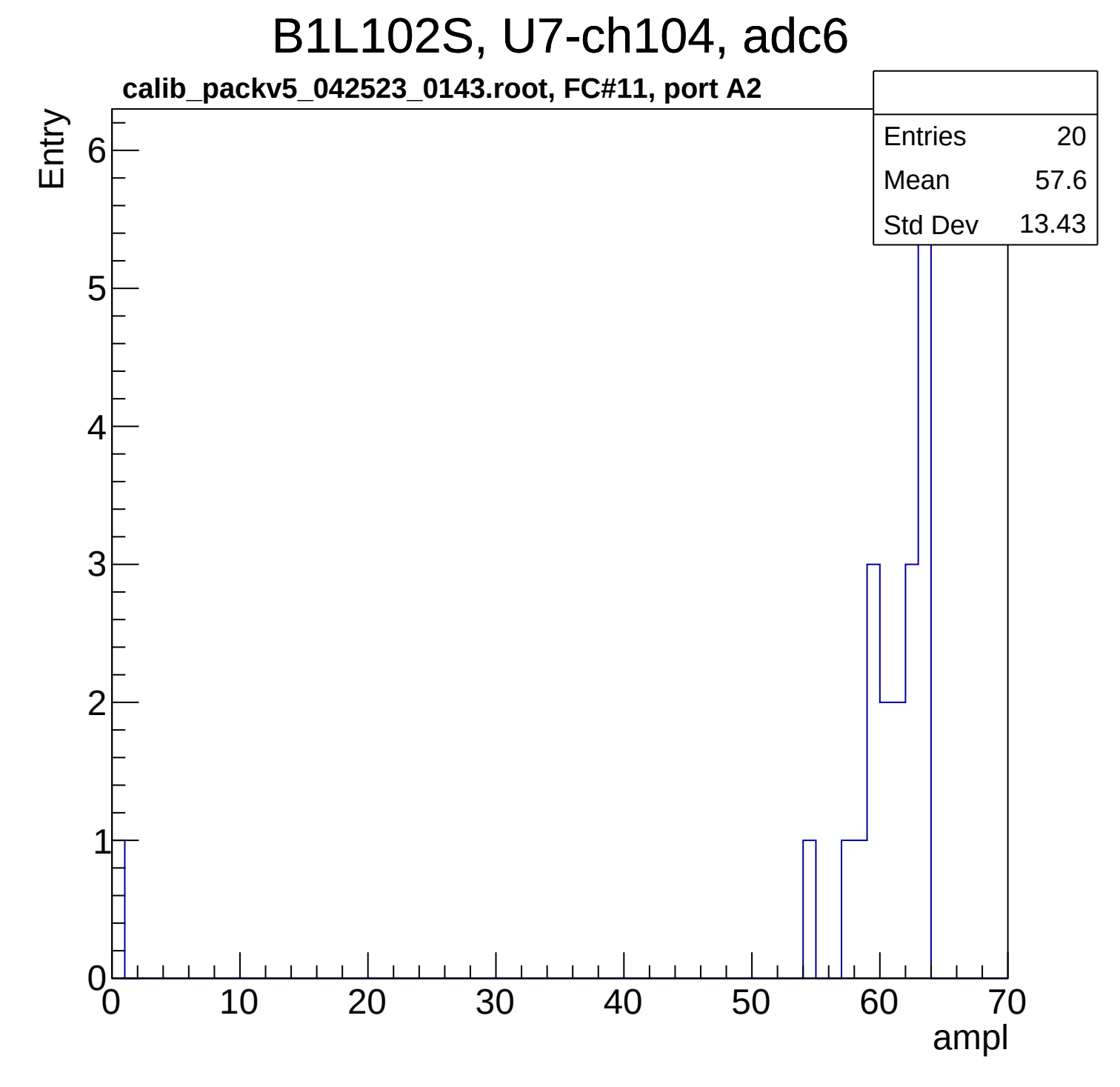
B1L102S, U7-ch104, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 20
Mean 57.6
Std Dev 13.43
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
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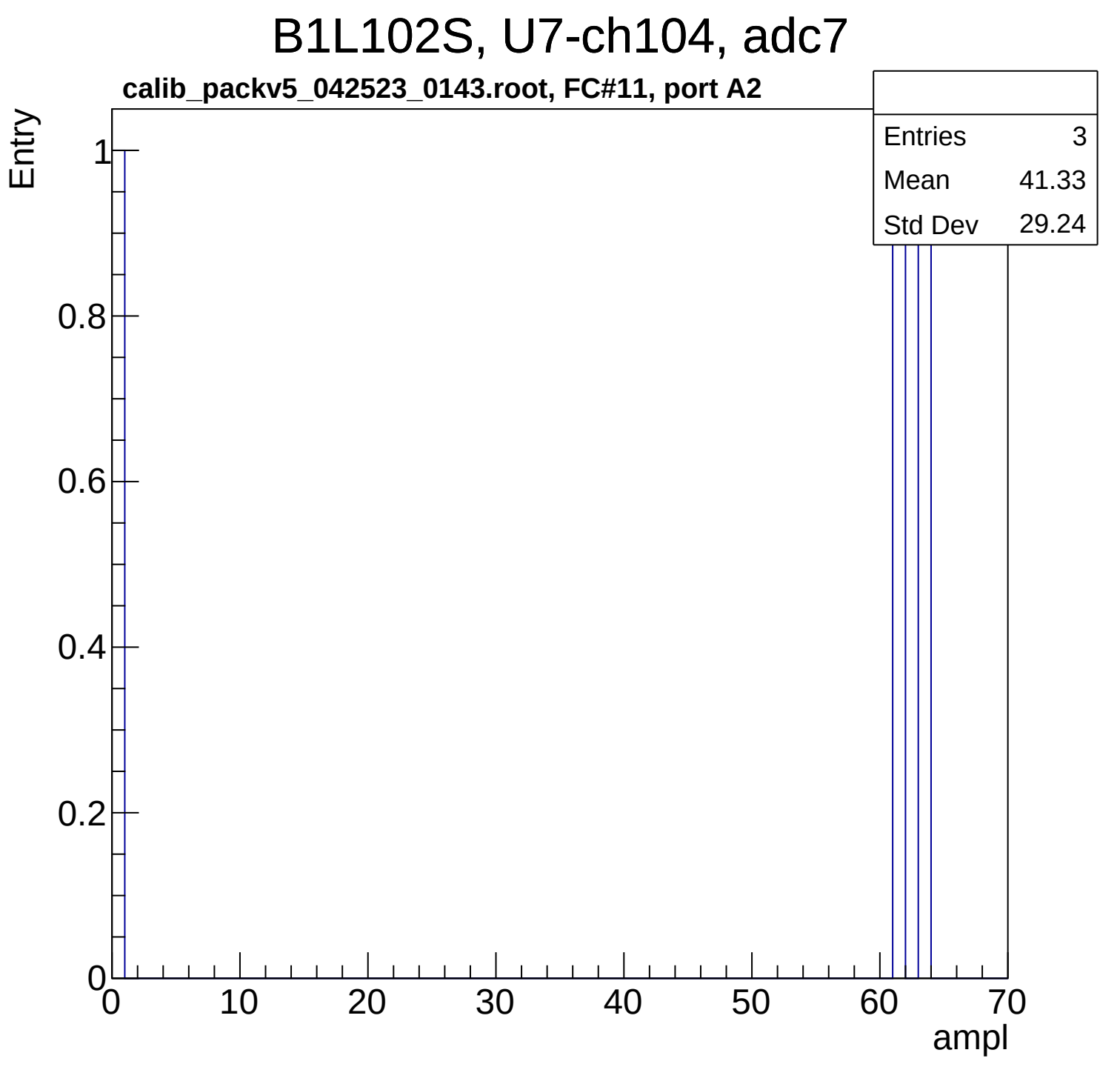
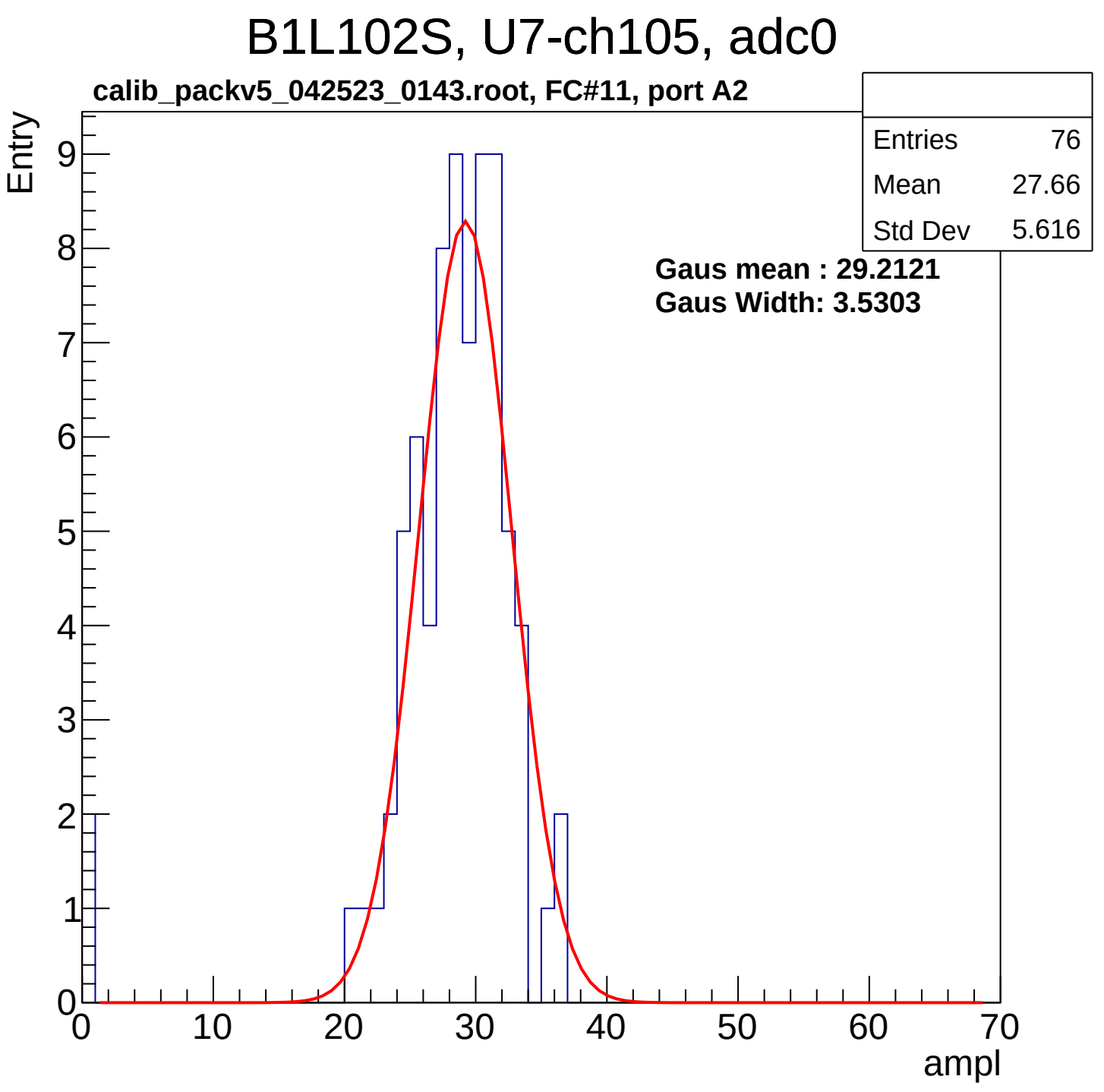
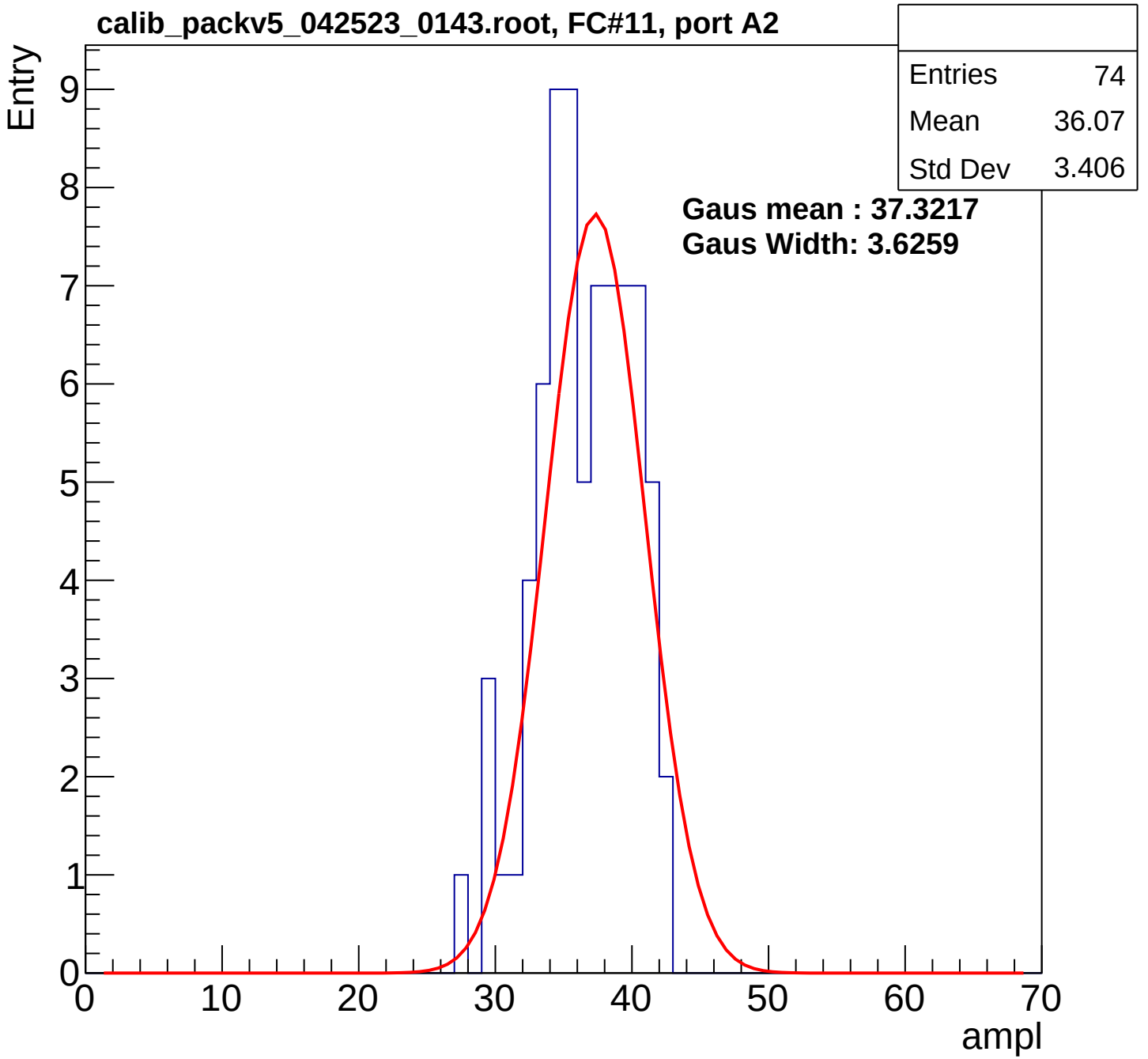
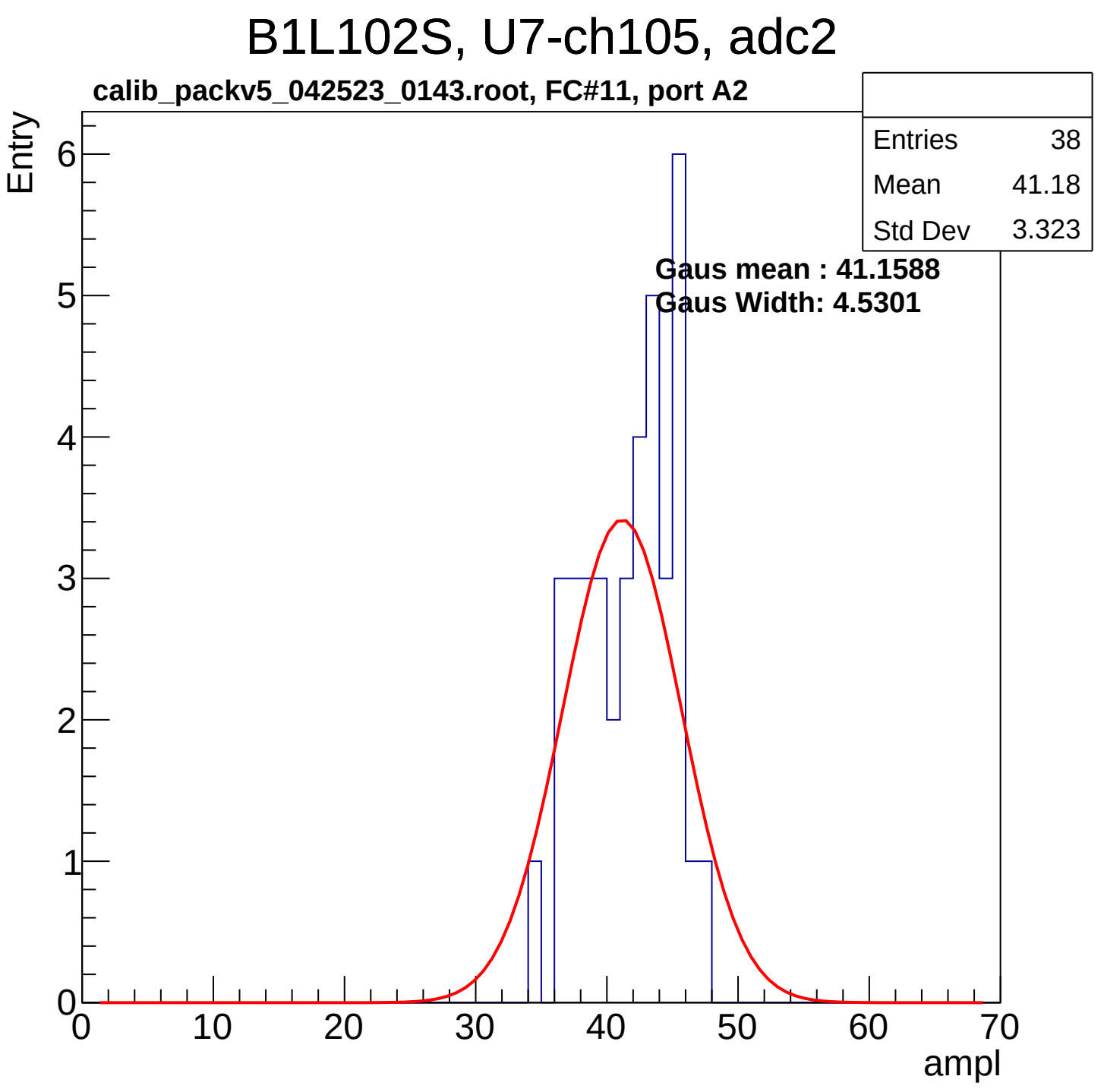
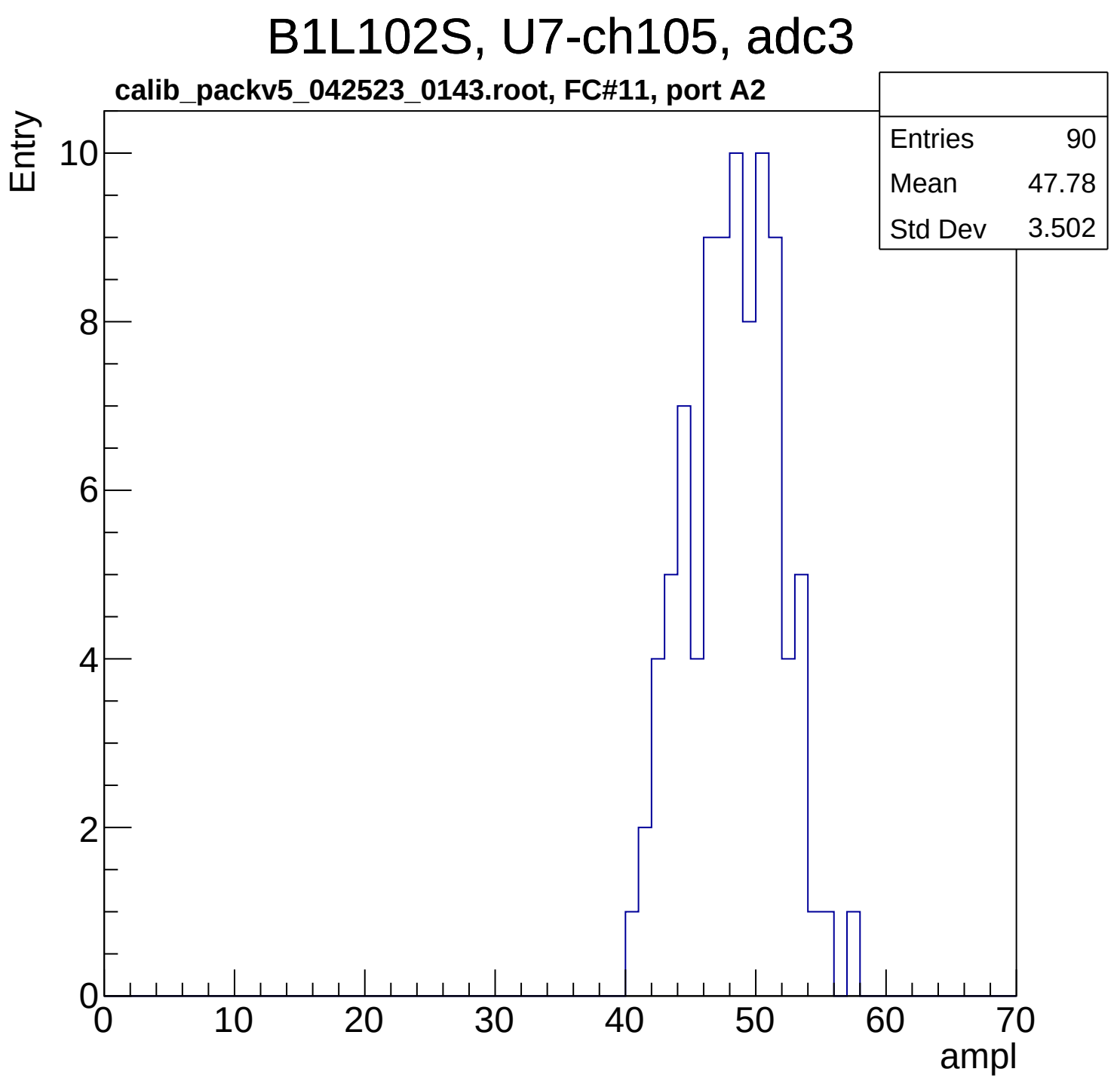
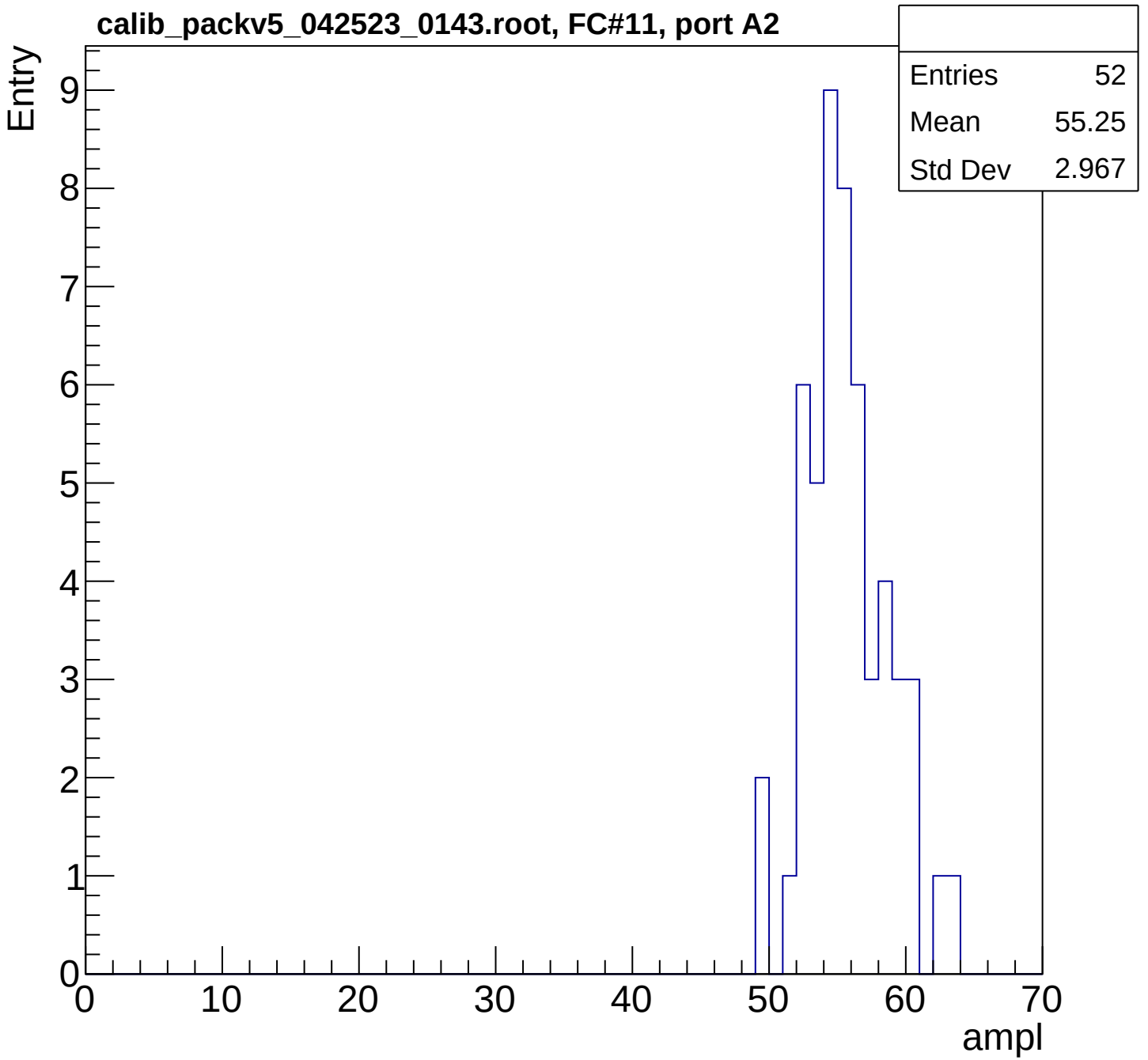

B1L102S, U7-ch104, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 3
Mean 41.33
Std Dev 29.24
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

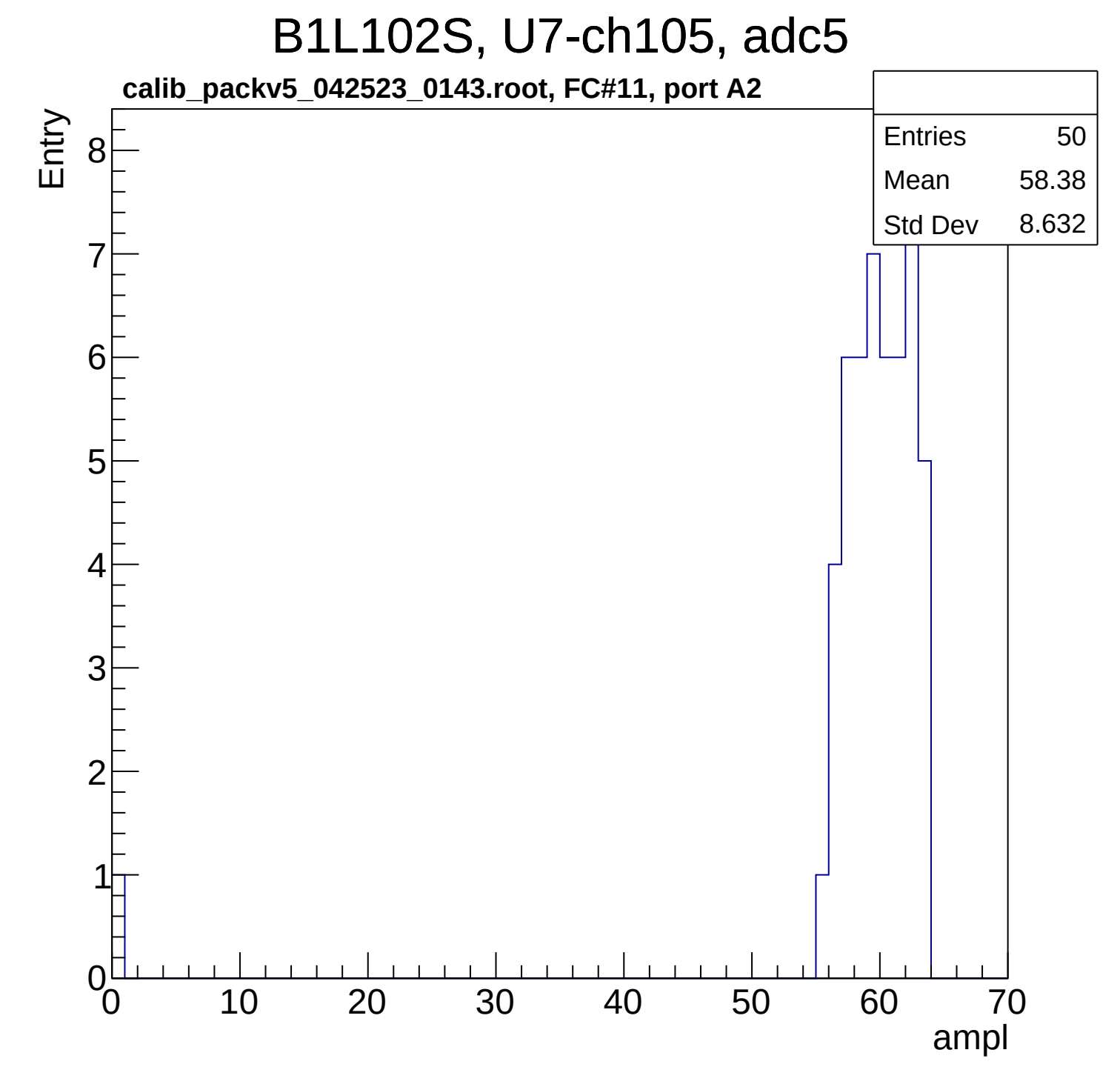

B1L102S, U7-ch105, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 76
Mean 27.66
Std Dev 5.616
Gaus mean : 29.2121
Gaus Width: 3.5303
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L102S, U7-ch105, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 74
Mean 36.07
Std Dev 3.406
Gaus mean : 37.3217
Gaus Width: 3.6259
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L102S, U7-ch105, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 38
Mean 41.18
Std Dev 3.323
Gaus mean : 41.1588
Gaus Width: 4.5301
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L102S, U7-ch105, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 90
Mean 47.78
Std Dev 3.502
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L102S, U7-ch105, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 52
Mean 55.25
Std Dev 2.967
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L102S, U7-ch105, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 50
Mean 58.38
Std Dev 8.632
Entry
ampl
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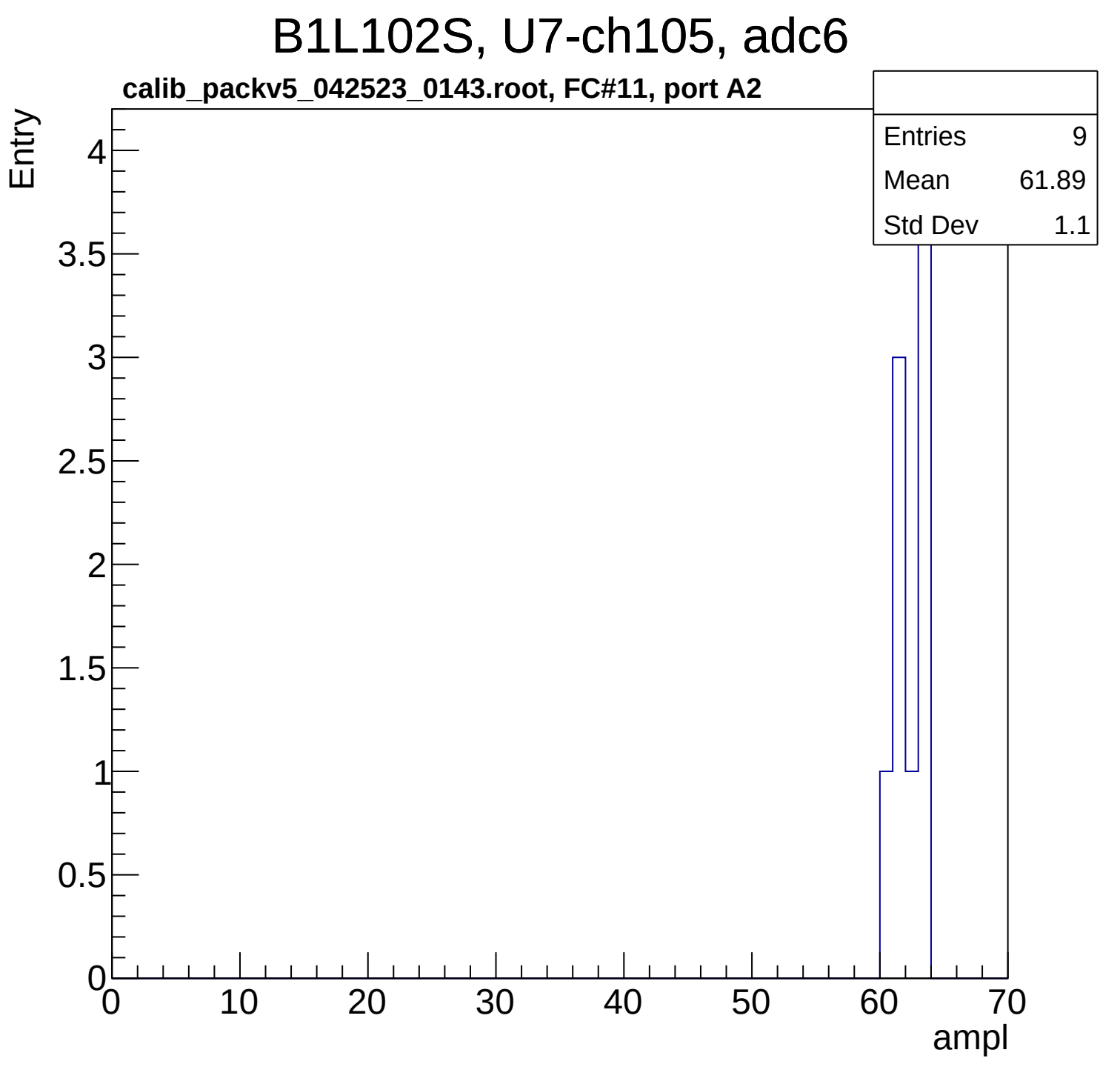
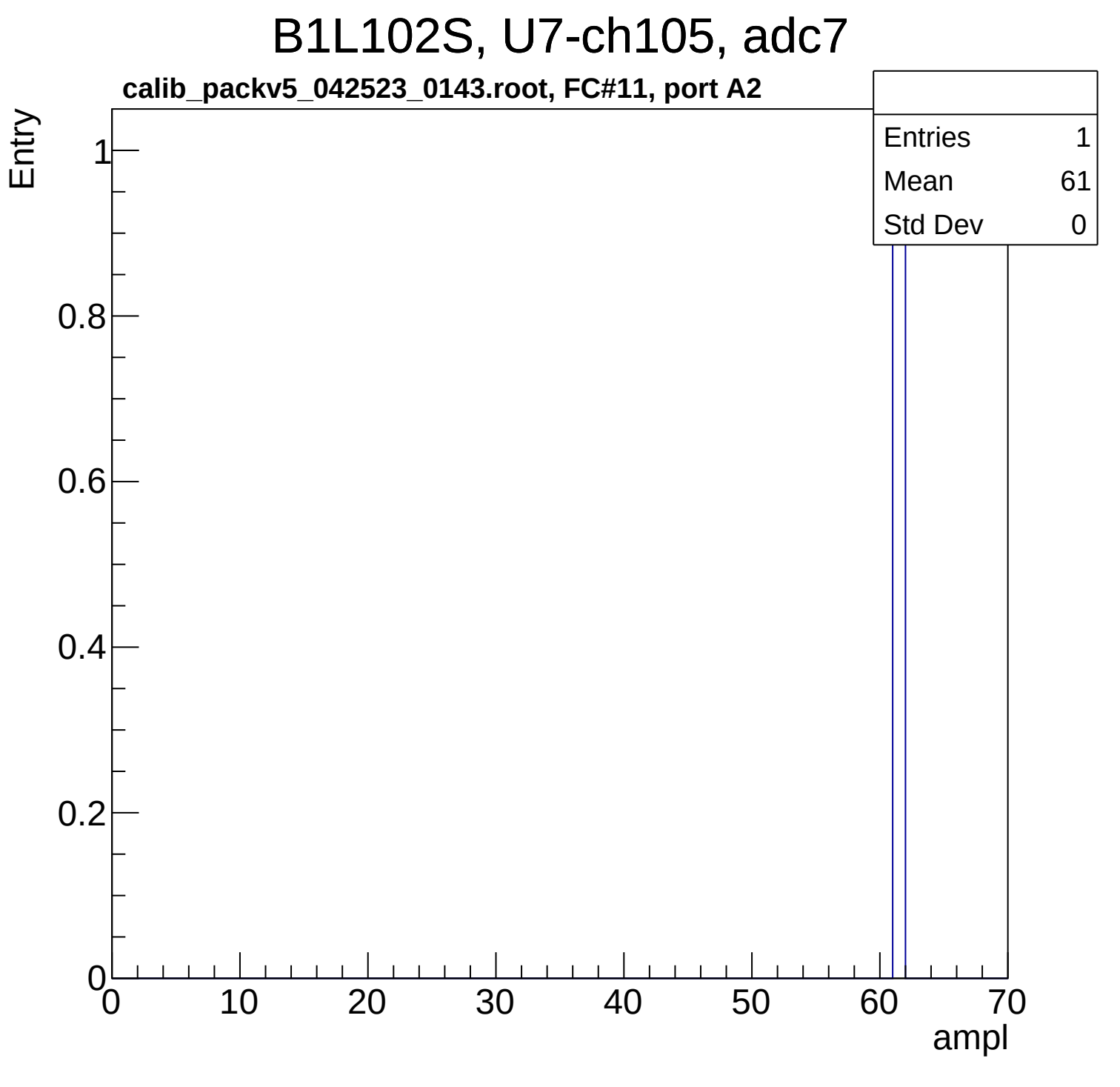
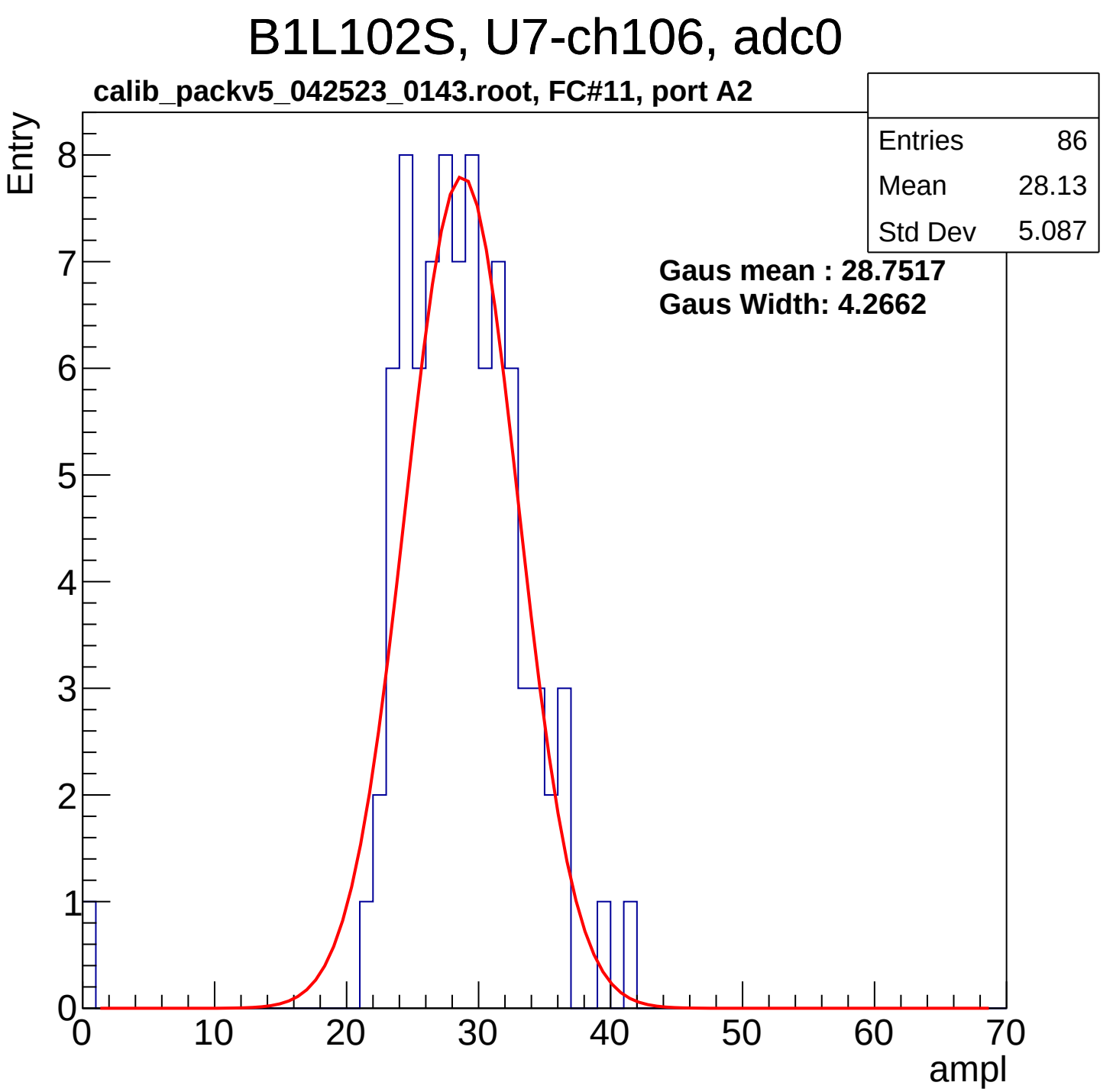
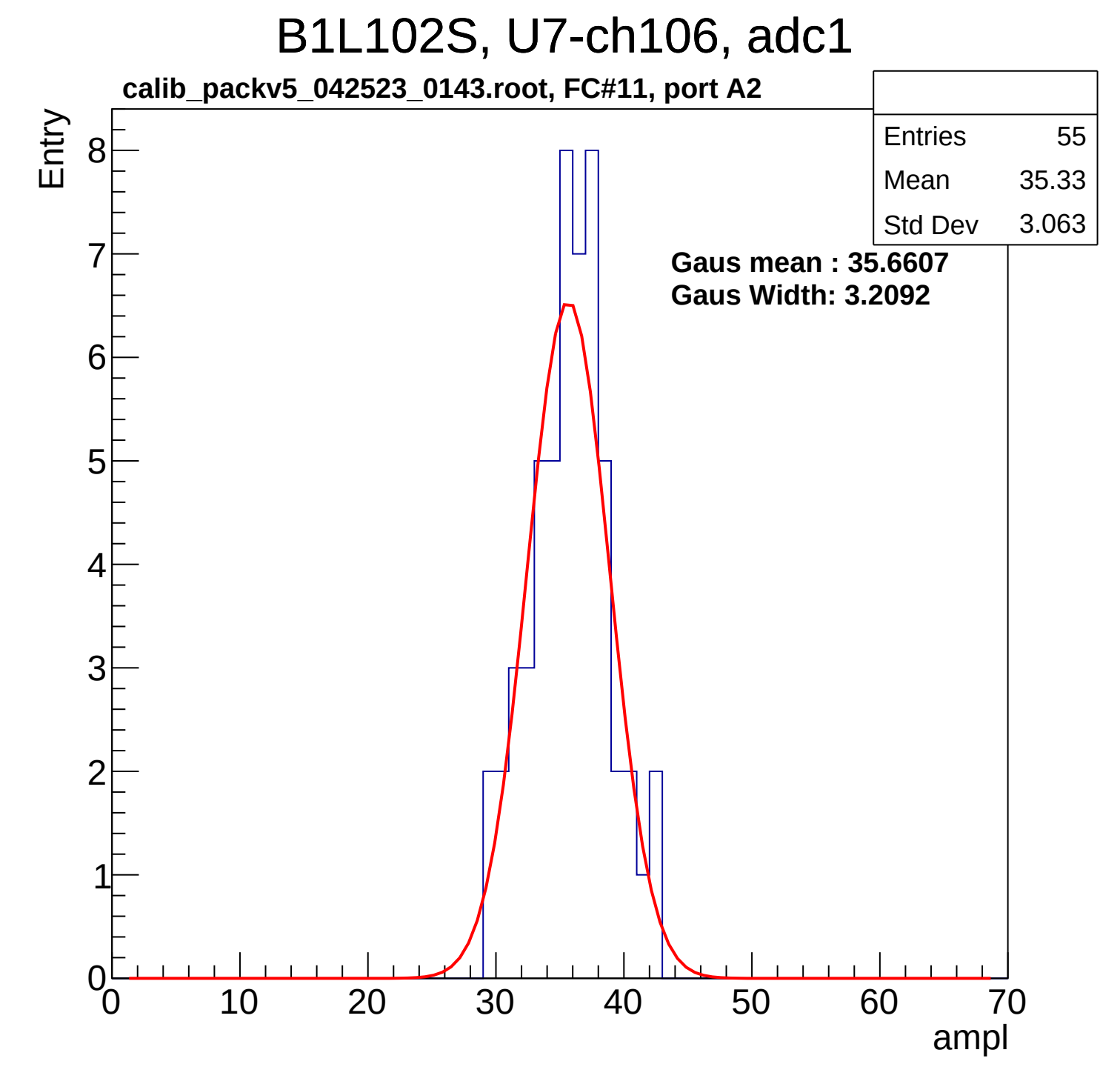
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L102S, U7-ch105, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 9
Mean 61.89
Std Dev 1.1
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L102S, U7-ch105, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 1
Mean 61
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U7-ch106, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 86
Mean 28.13
Std Dev 5.087
Gaus mean : 28.7517
Gaus Width: 4.2662
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L102S, U7-ch106, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 55
Mean 35.33
Std Dev 3.063
Gaus mean : 35.6607
Gaus Width: 3.2092
Entry
ampl
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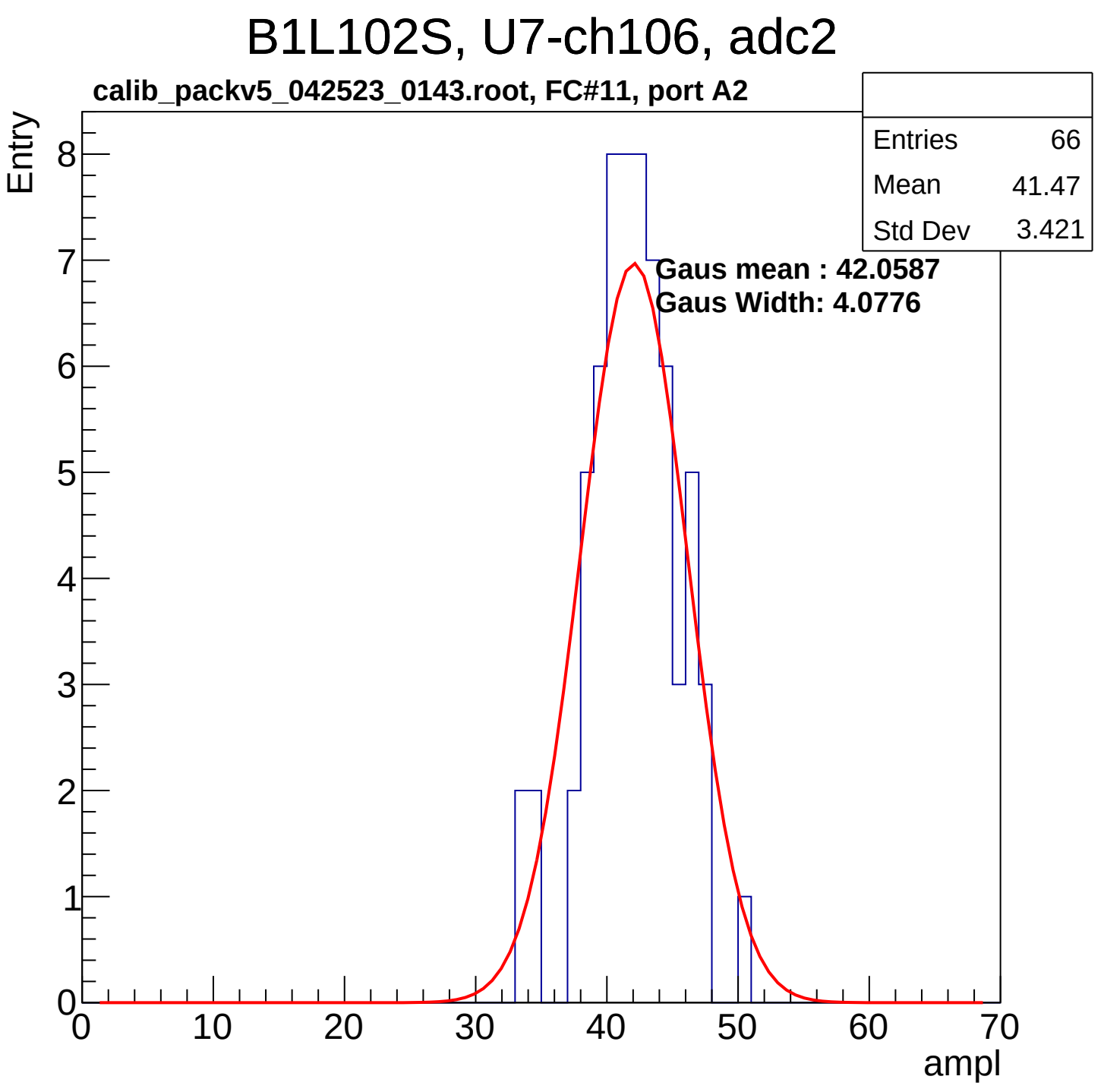
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L102S, U7-ch106, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 66
Mean 41.47
Std Dev 3.421
Gaus mean : 42.0587
Gaus Width: 4.0776
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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40
50
60
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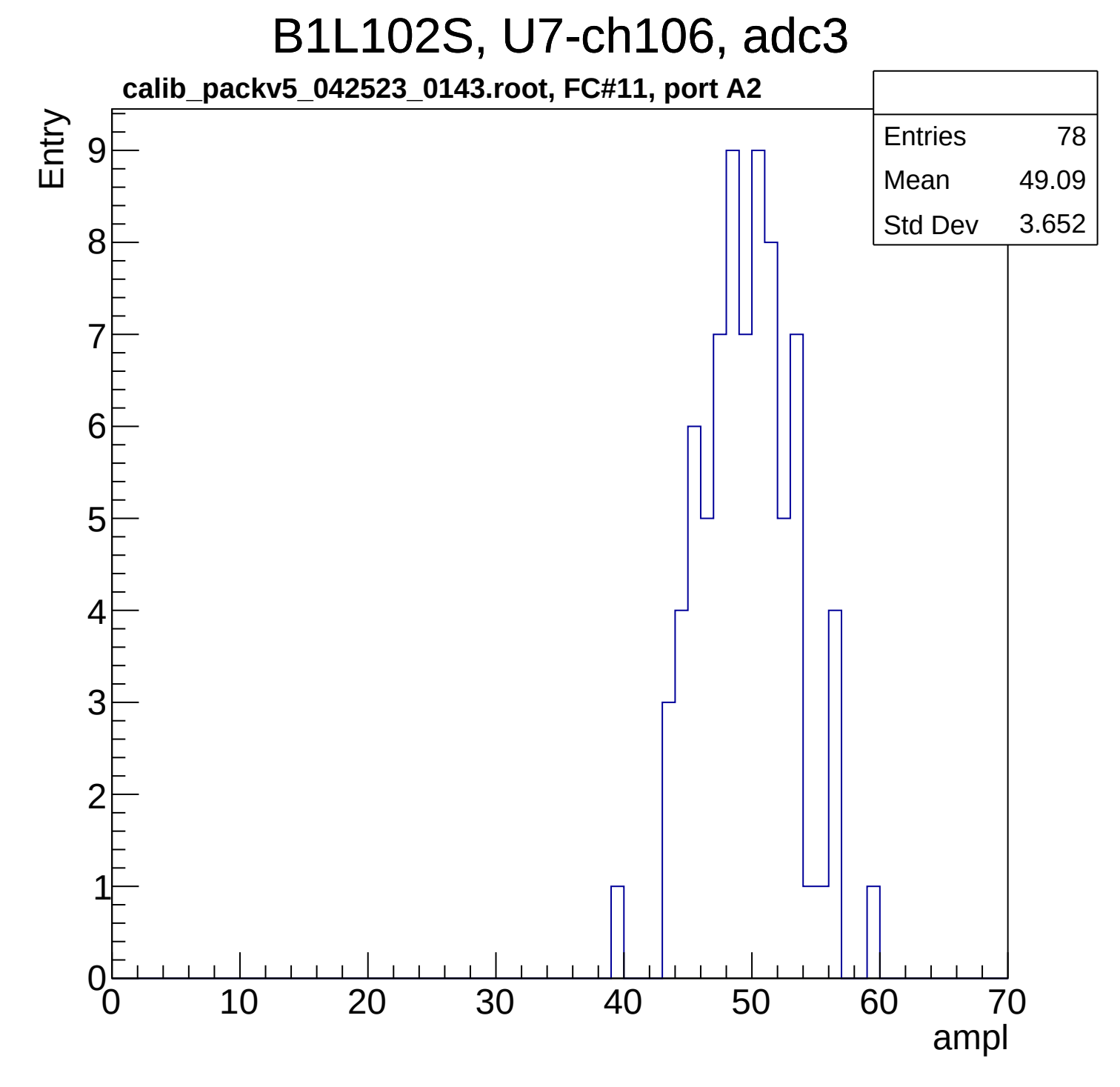
B1L102S, U7-ch106, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 78
Mean 49.09
Std Dev 3.652
Entry
ampl
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3
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6
7
8
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0
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20
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60
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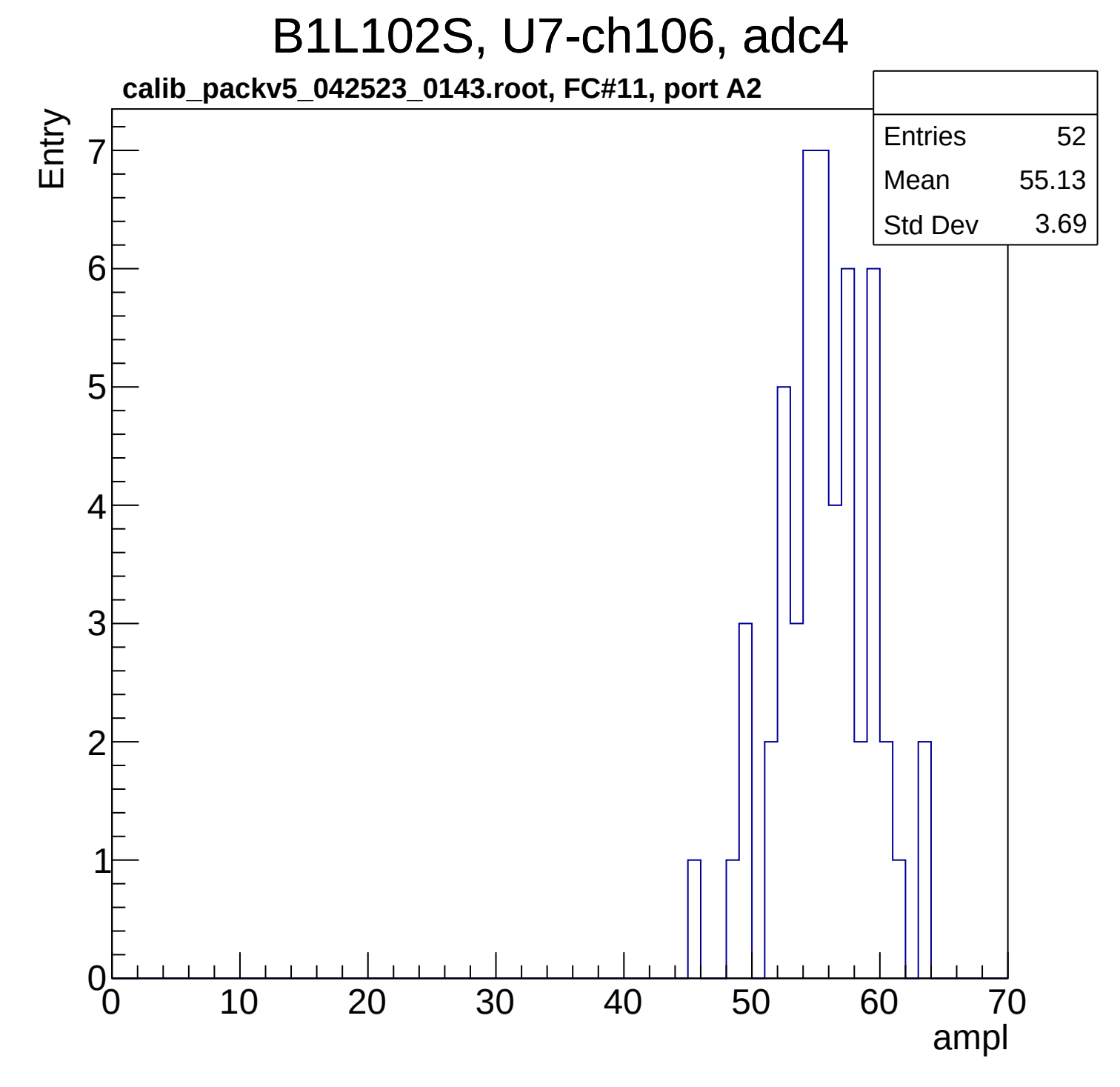
B1L102S, U7-ch106, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 52
Mean 55.13
Std Dev 3.69
Entry
ampl
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1
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3
4
5
6
7
0
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20
30
40
50
60
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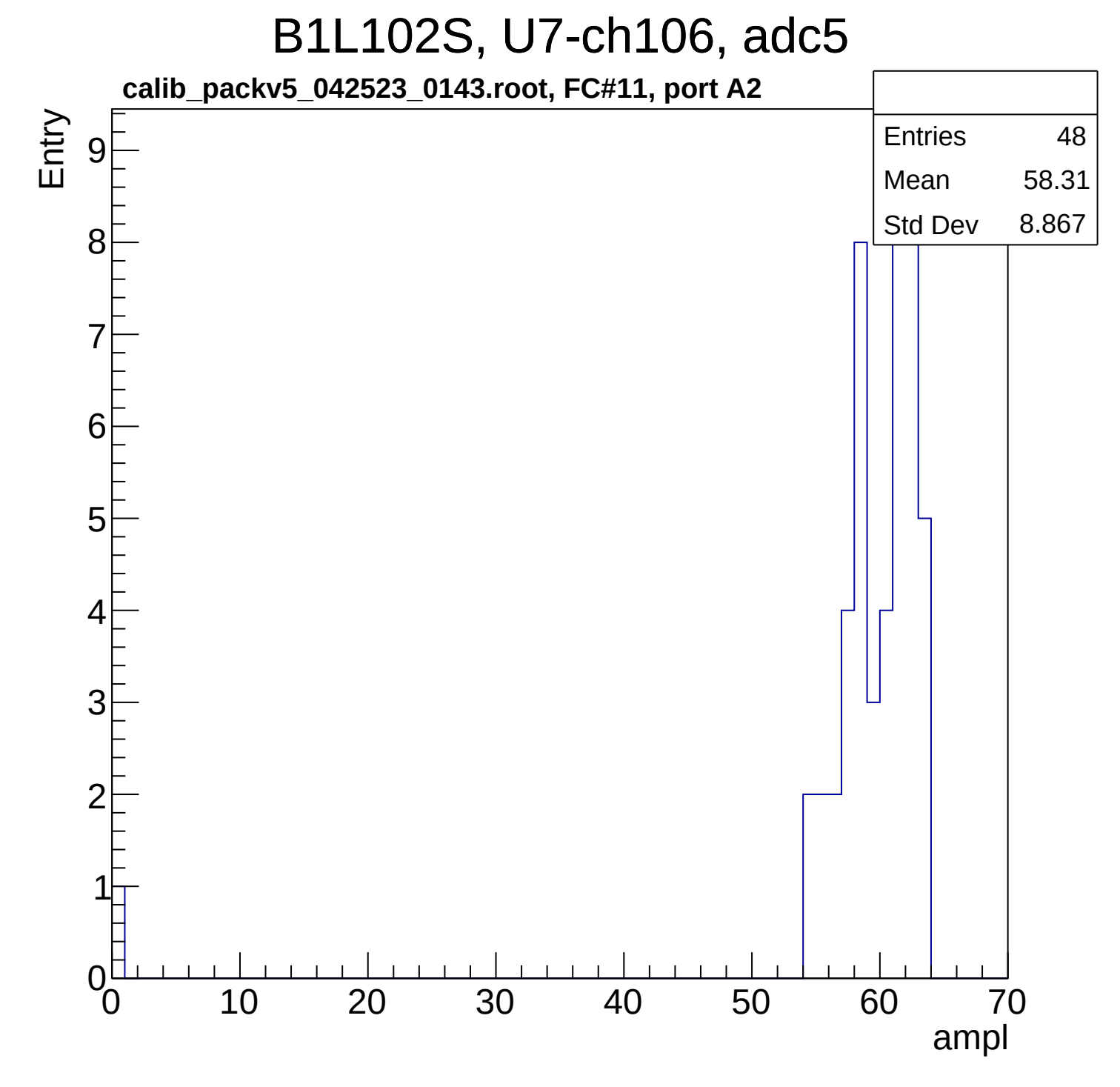
B1L102S, U7-ch106, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 48
Mean 58.31
Std Dev 8.867
Entry
ampl
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3
4
5
6
7
8
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0
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40
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60
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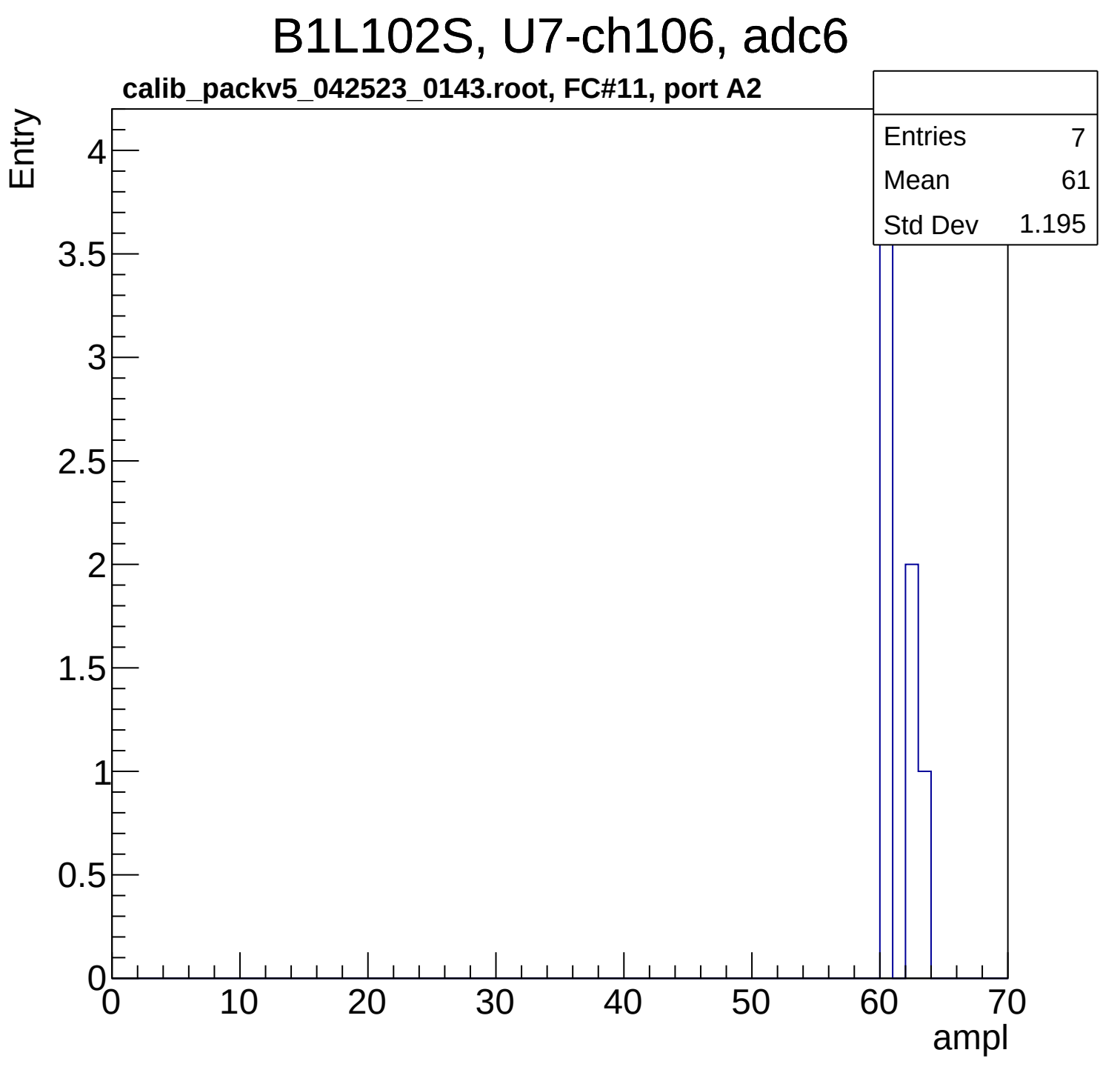
B1L102S, U7-ch106, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 7
Mean 61
Std Dev 1.195
Entry
ampl
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1.5
2
2.5
3
3.5
4
0
10
20
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40
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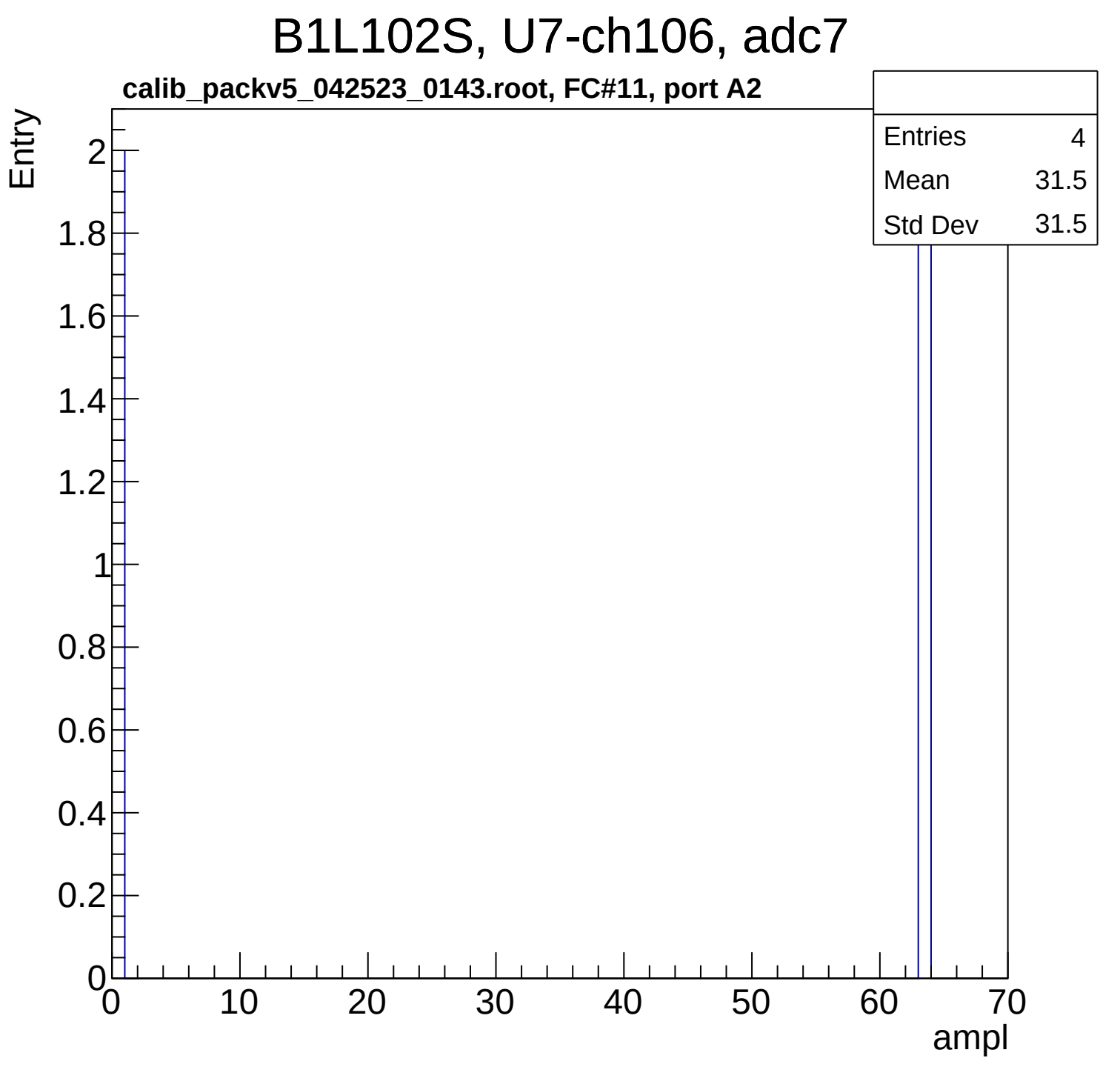
60
70


B1L102S, U7-ch106, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 4
Mean 31.5
Std Dev 31.5
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
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40
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60
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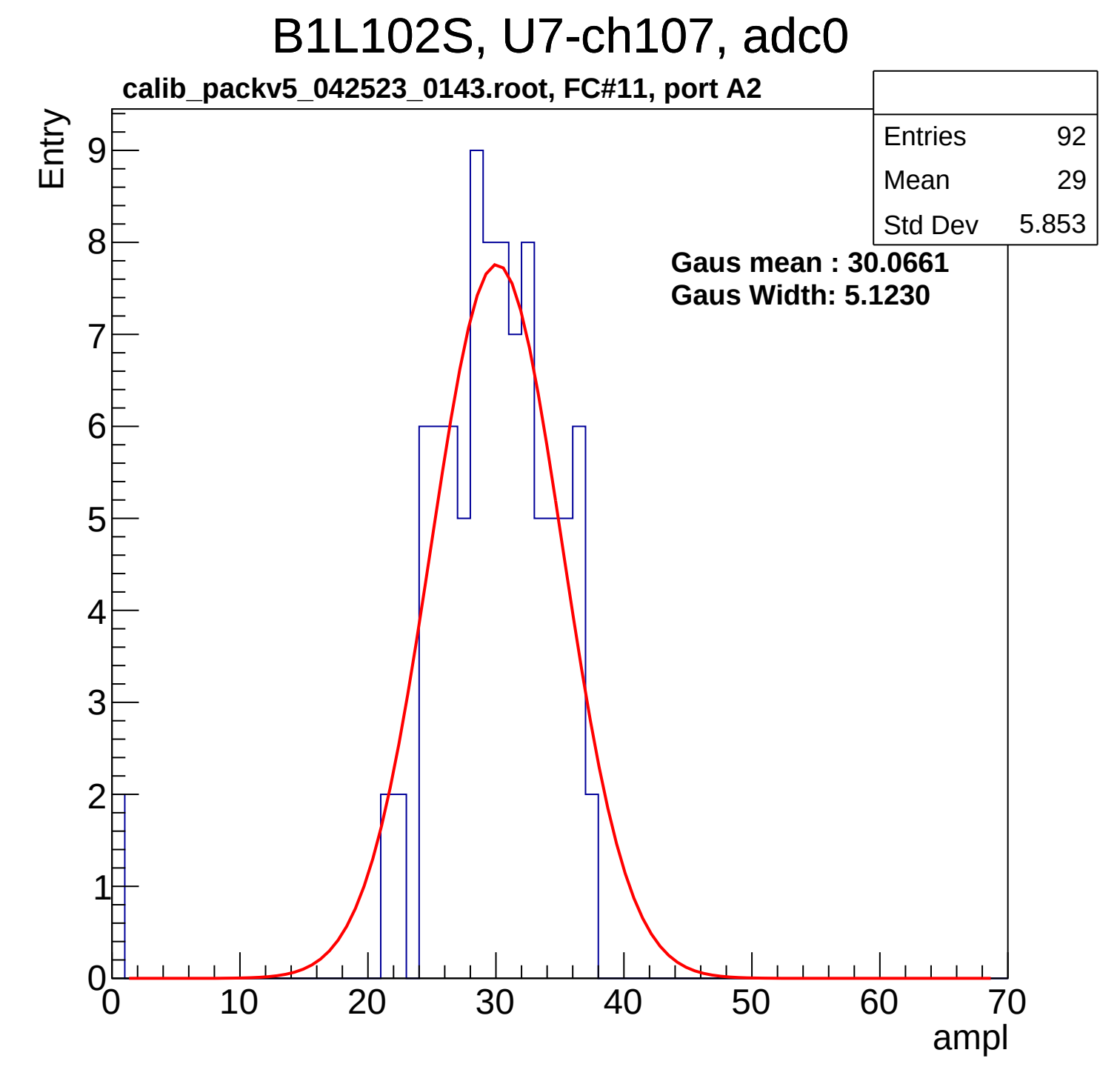
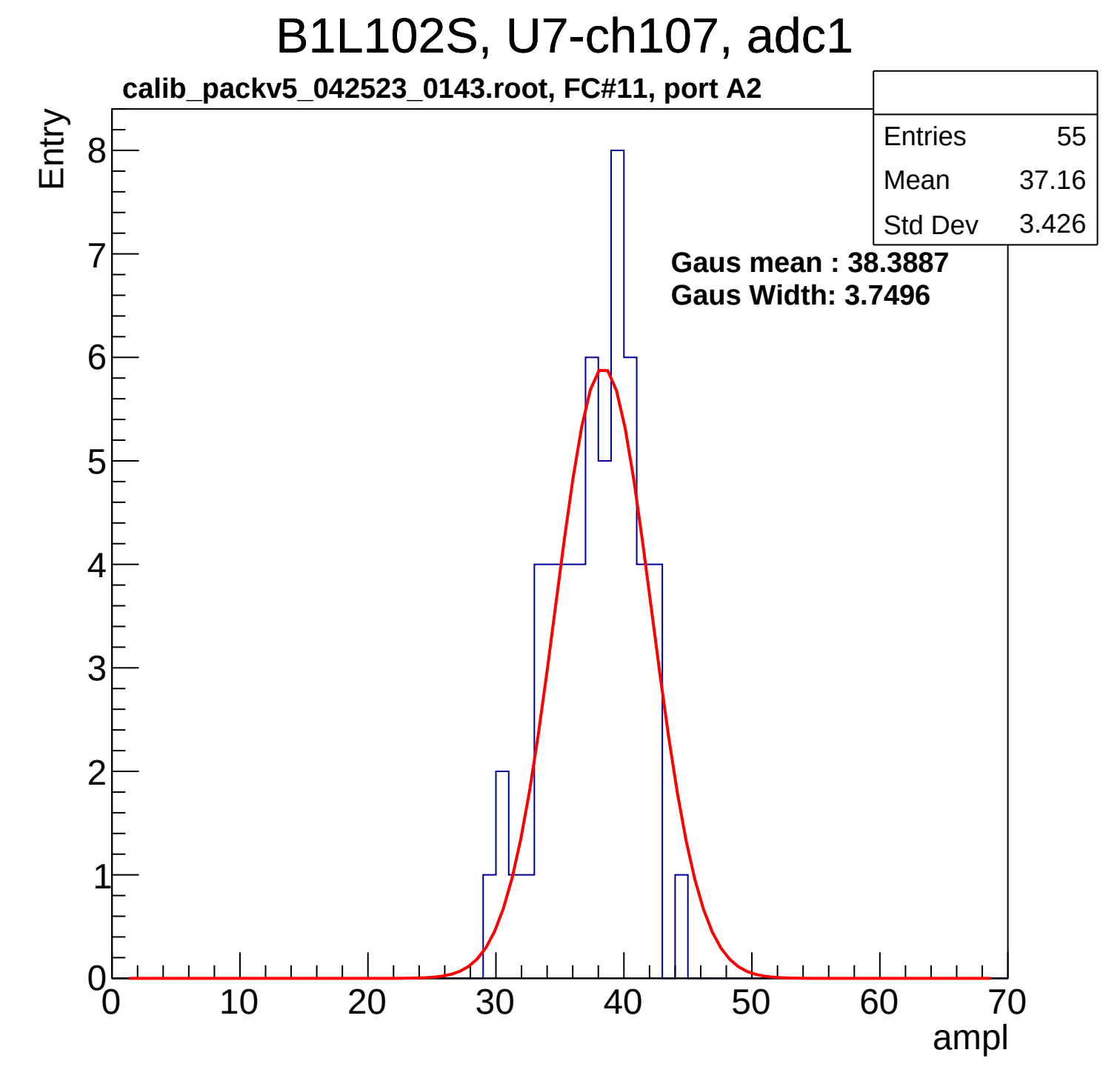

B1L102S, U7-ch107, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 92
Mean 29
Std Dev 5.853
Gaus mean : 30.0661
Gaus Width: 5.1230
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L102S, U7-ch107, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 55
Mean 37.16
Std Dev 3.426
Gaus mean : 38.3887
Gaus Width: 3.7496
Entry
ampl
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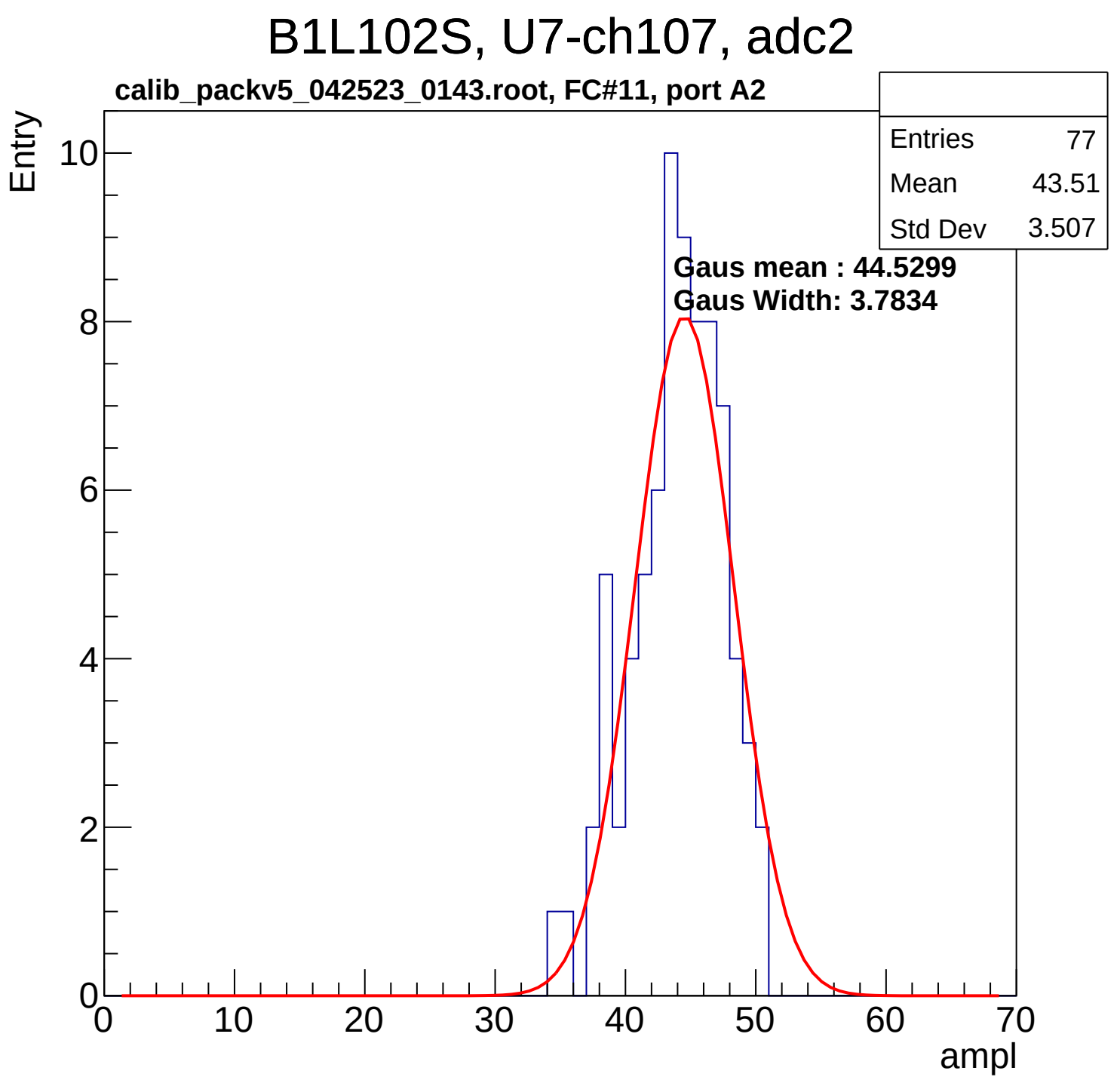
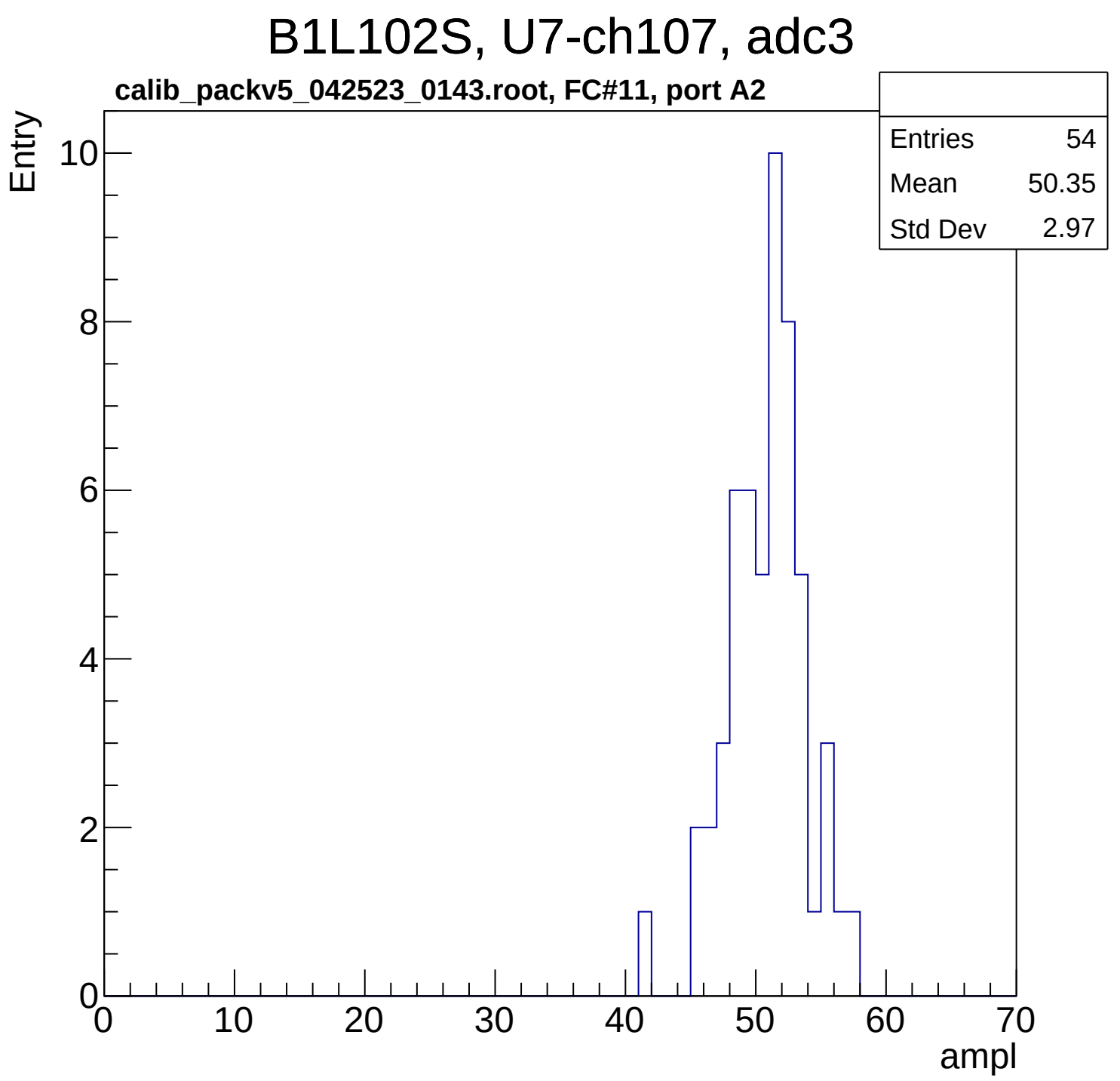
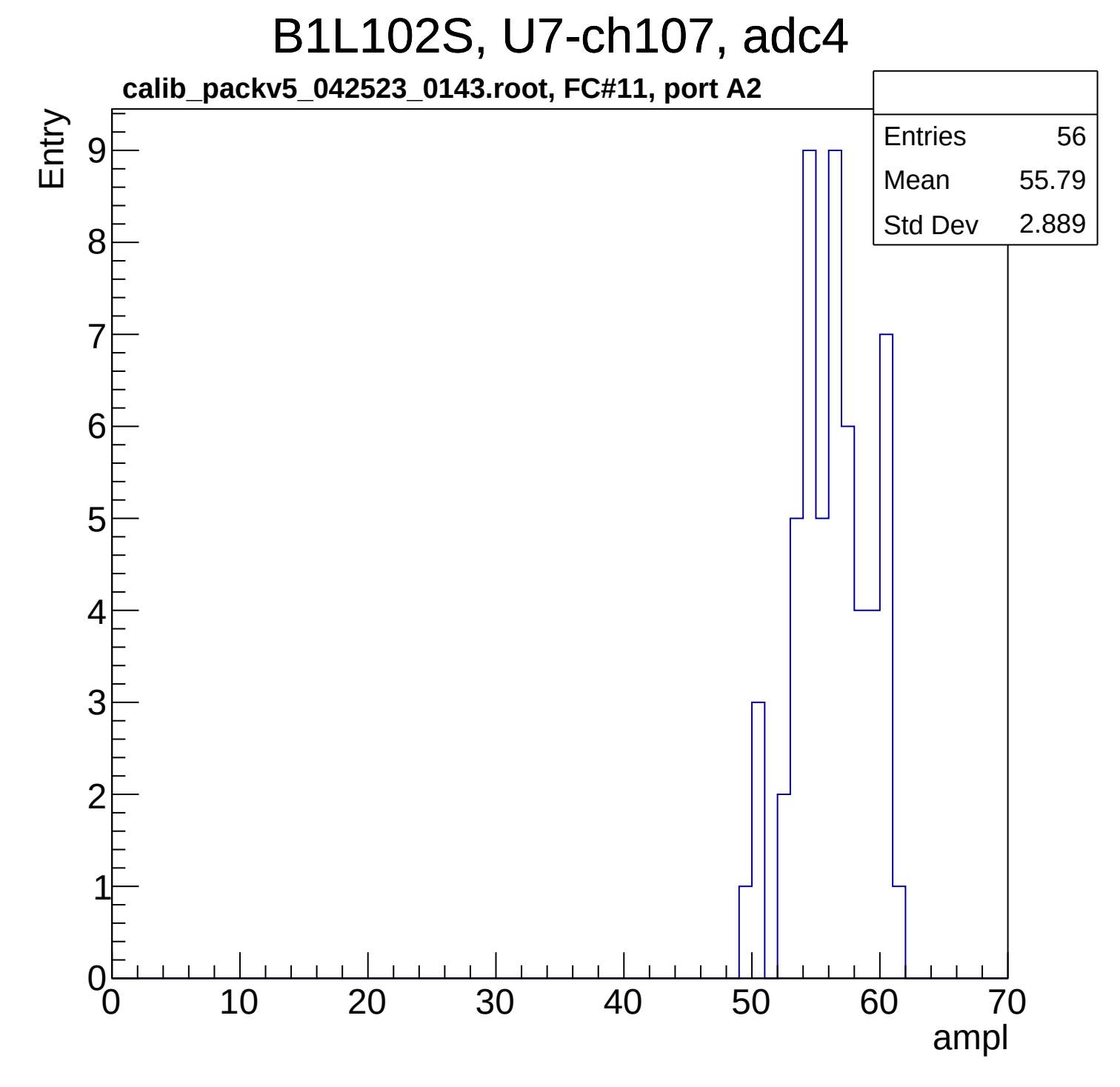
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L102S, U7-ch107, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 77
Mean 43.51
Std Dev 3.507
Gaus mean : 44.5299
Gaus Width: 3.7834
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L102S, U7-ch107, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 54
Mean 50.35
Std Dev 2.97
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L102S, U7-ch107, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 56
Mean 55.79
Std Dev 2.889
Entry
ampl
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3
4
5
6
7
8
9
0
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20
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40
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60
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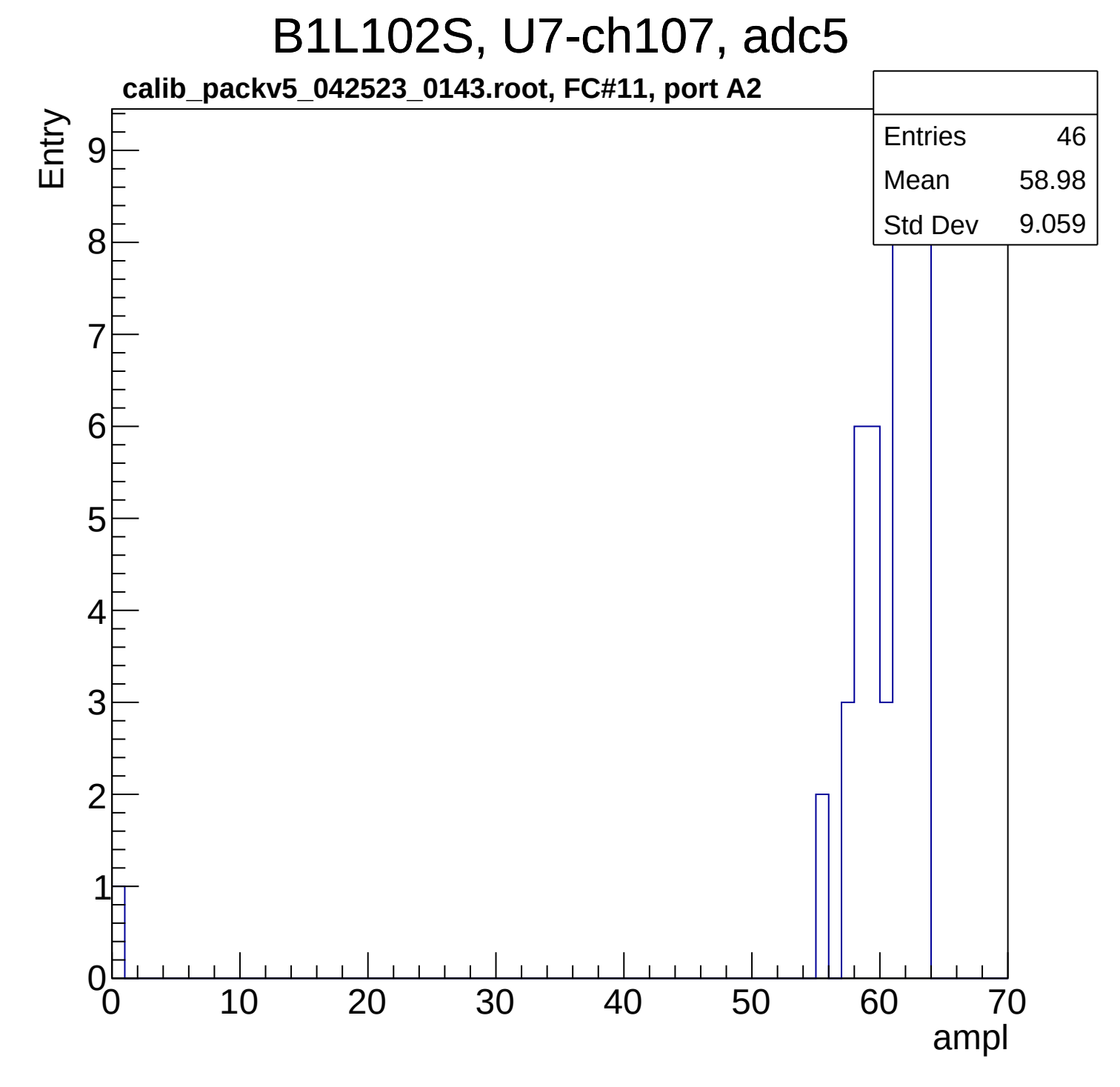
B1L102S, U7-ch107, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 46
Mean 58.98
Std Dev 9.059
Entry
ampl
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2
3
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5
6
7
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0
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40
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60
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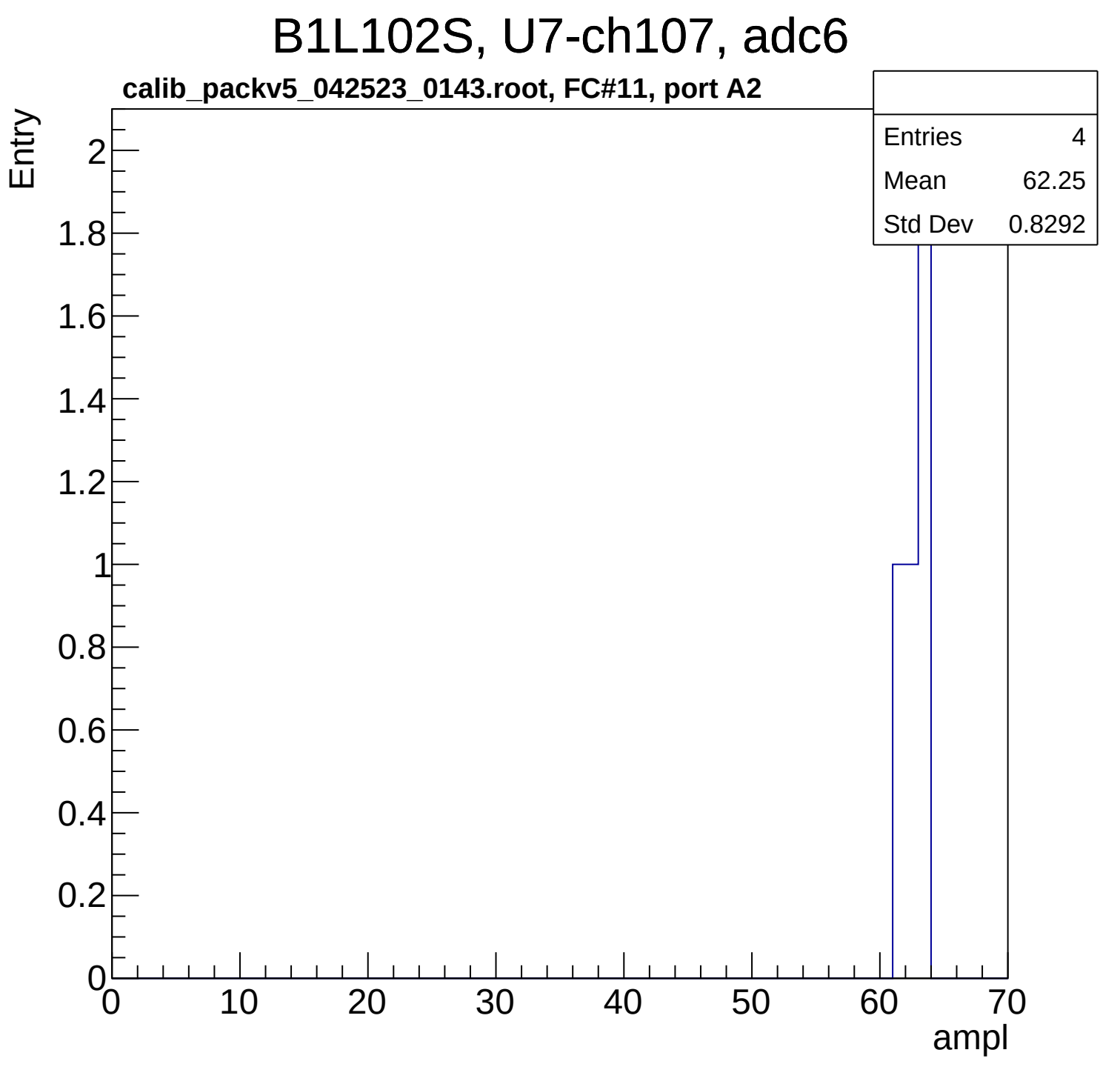
B1L102S, U7-ch107, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 4
Mean 62.25
Std Dev 0.8292
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
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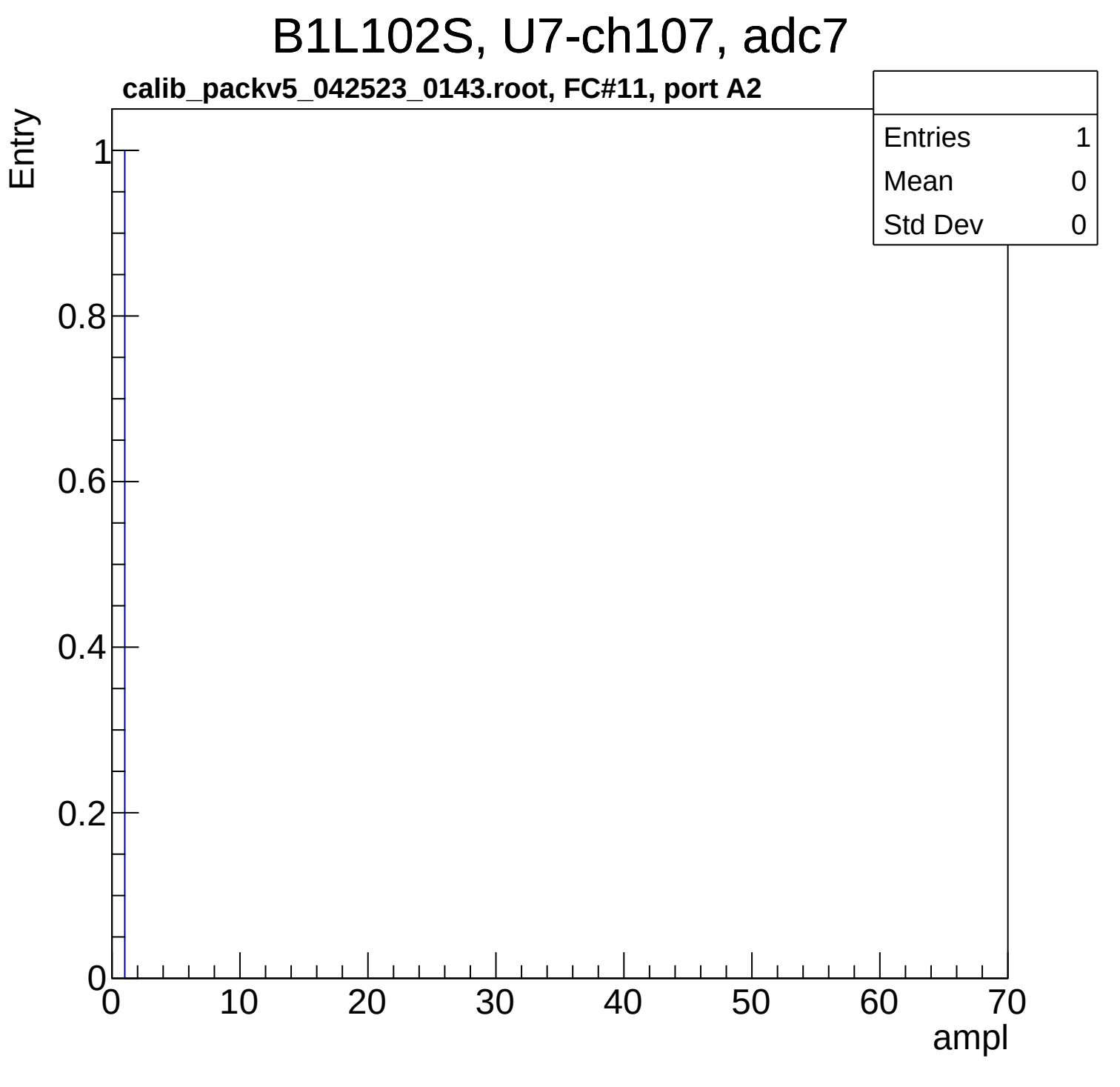
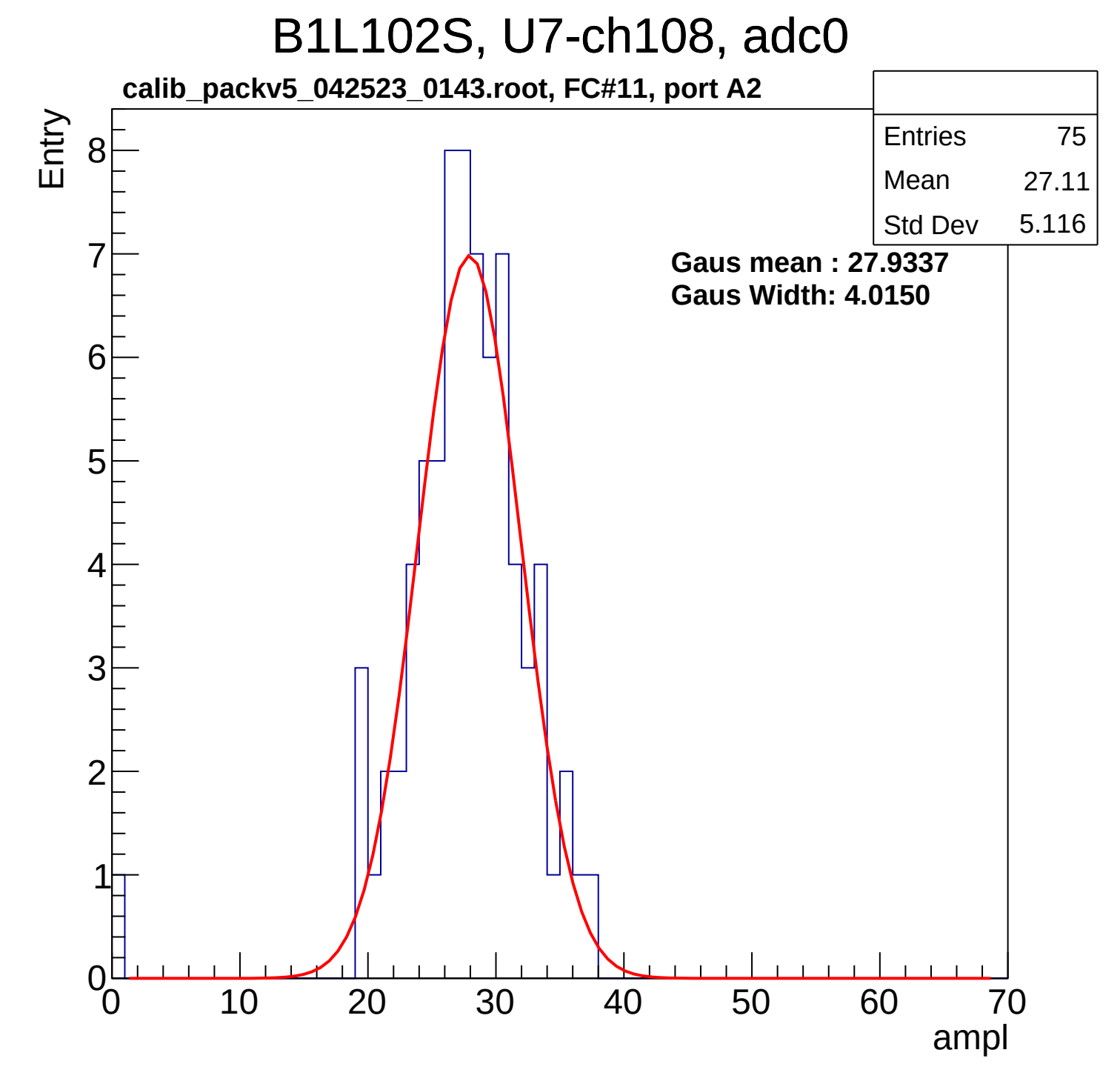
40
50
60
70


B1L102S, U7-ch107, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U7-ch108, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 75
Mean 27.11
Std Dev 5.116
Gaus mean : 27.9337
Gaus Width: 4.0150
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
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40
50
60
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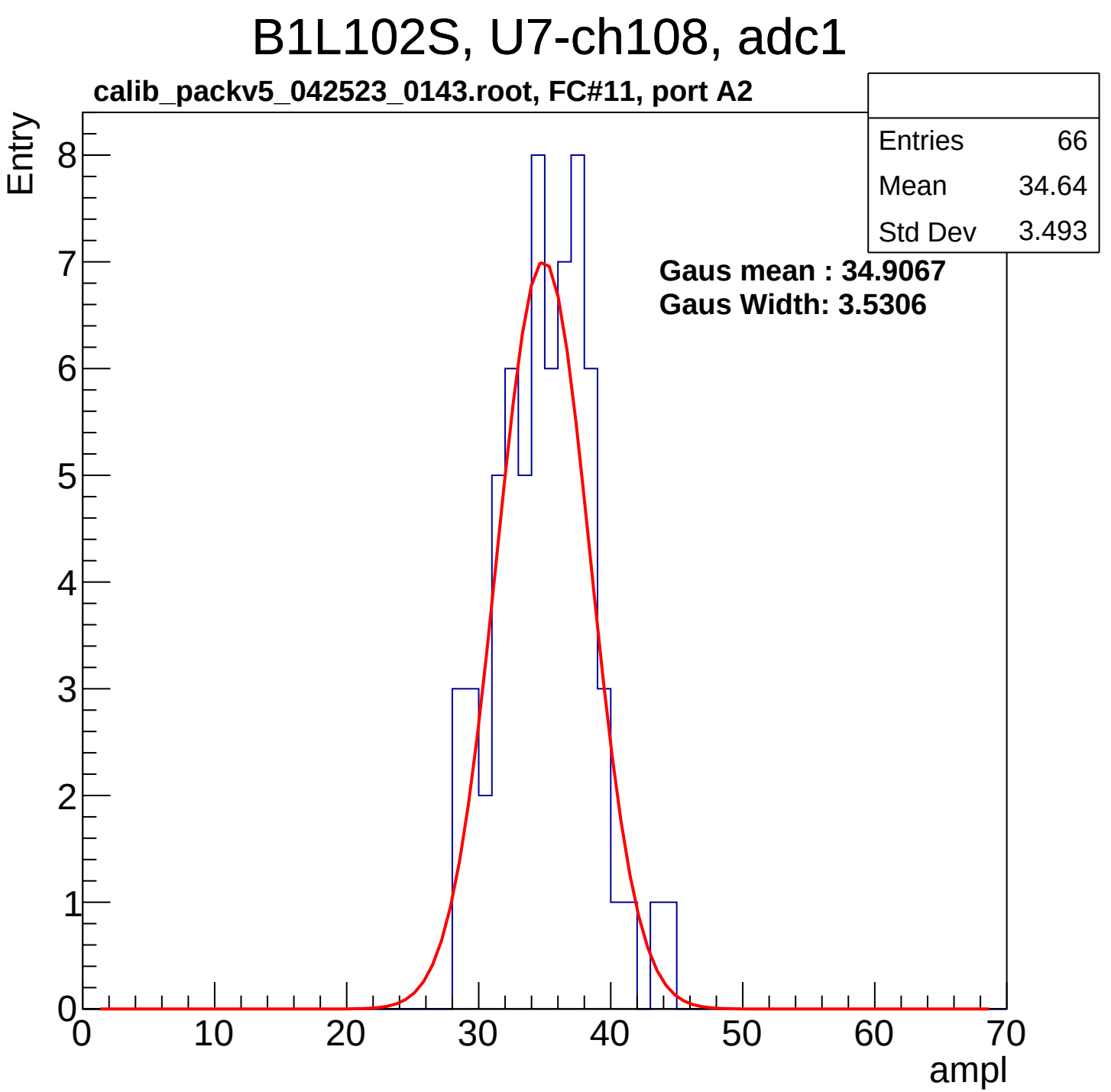
B1L102S, U7-ch108, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 66
Mean 34.64
Std Dev 3.493
Gaus mean : 34.9067
Gaus Width: 3.5306
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
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40
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60
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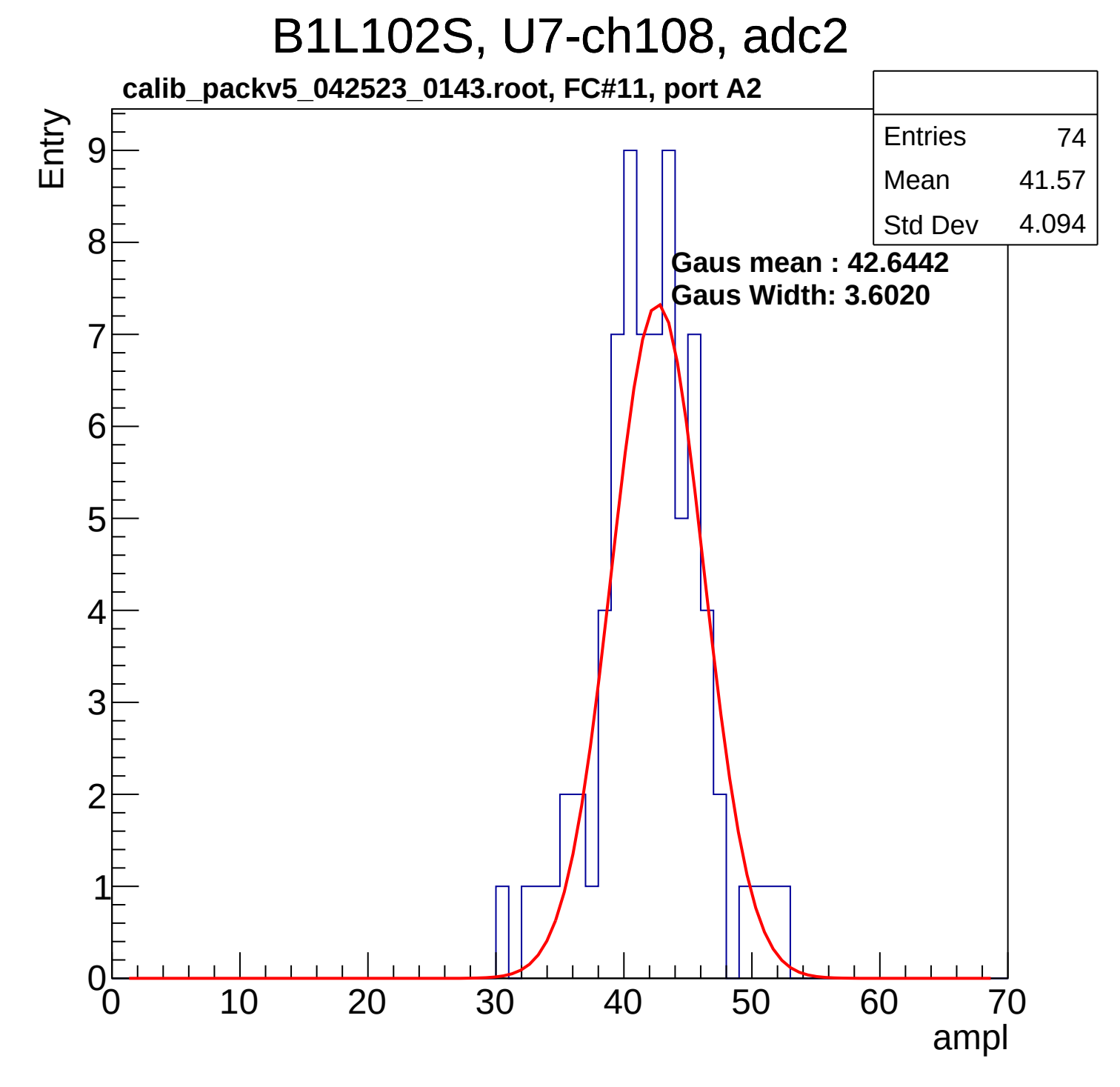
B1L102S, U7-ch108, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 74
Mean 41.57
Std Dev 4.094
Gaus mean : 42.6442
Gaus Width: 3.6020
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
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20
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40
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60
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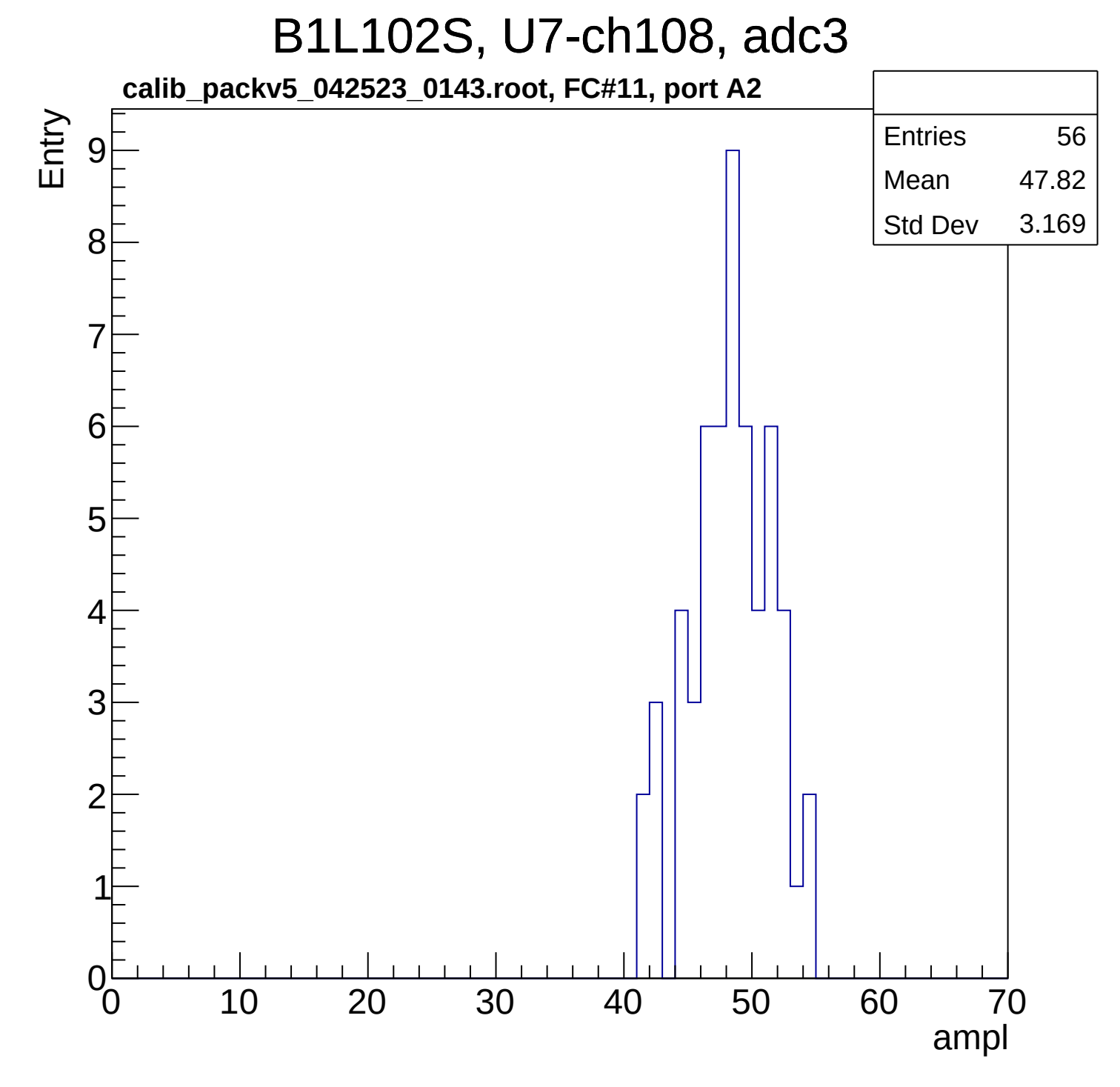
B1L102S, U7-ch108, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 56
Mean 47.82
Std Dev 3.169
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
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60
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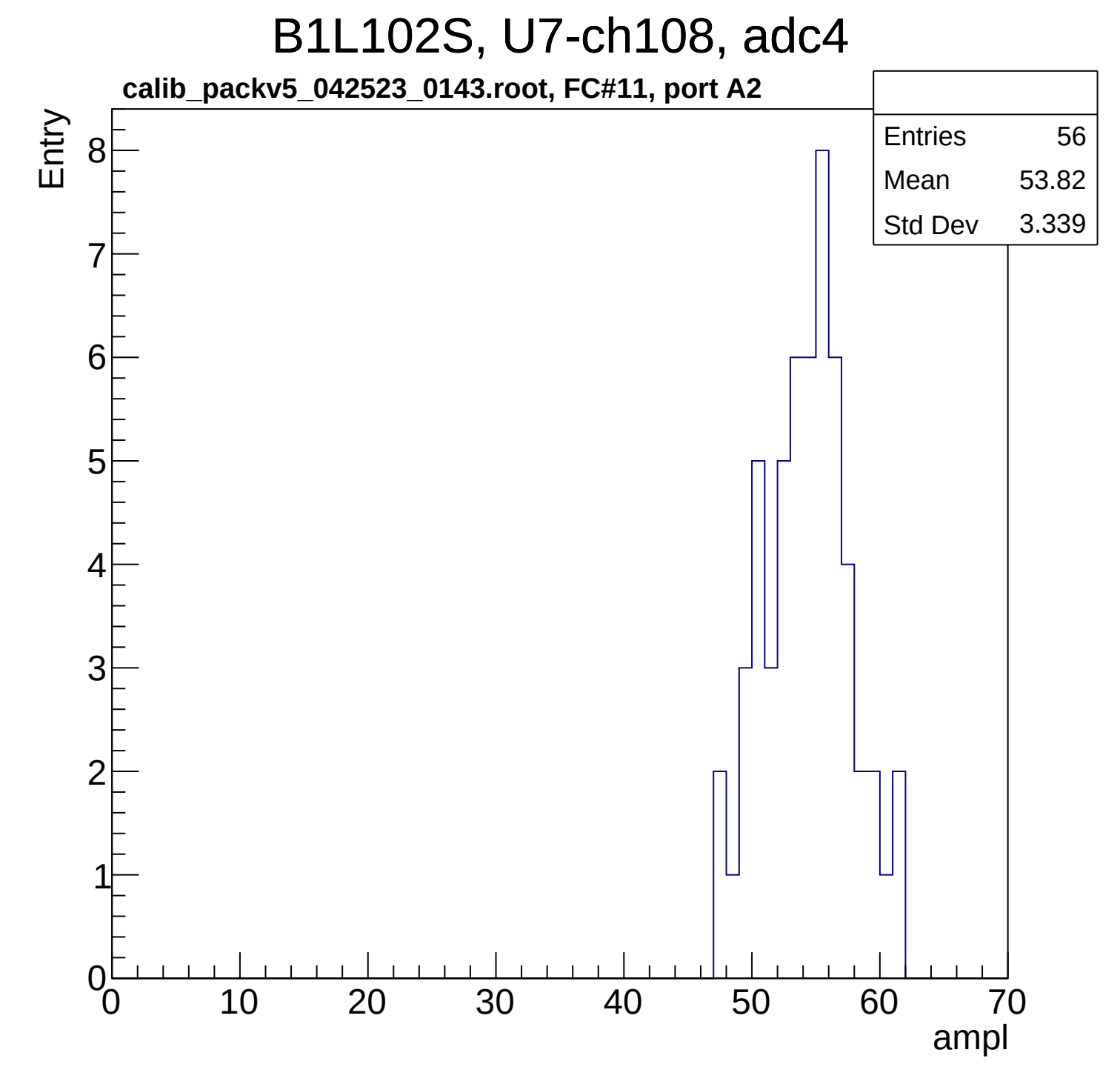
B1L102S, U7-ch108, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 56
Mean 53.82
Std Dev 3.339
Entry
ampl
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1
2
3
4
5
6
7
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0
10
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40
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60
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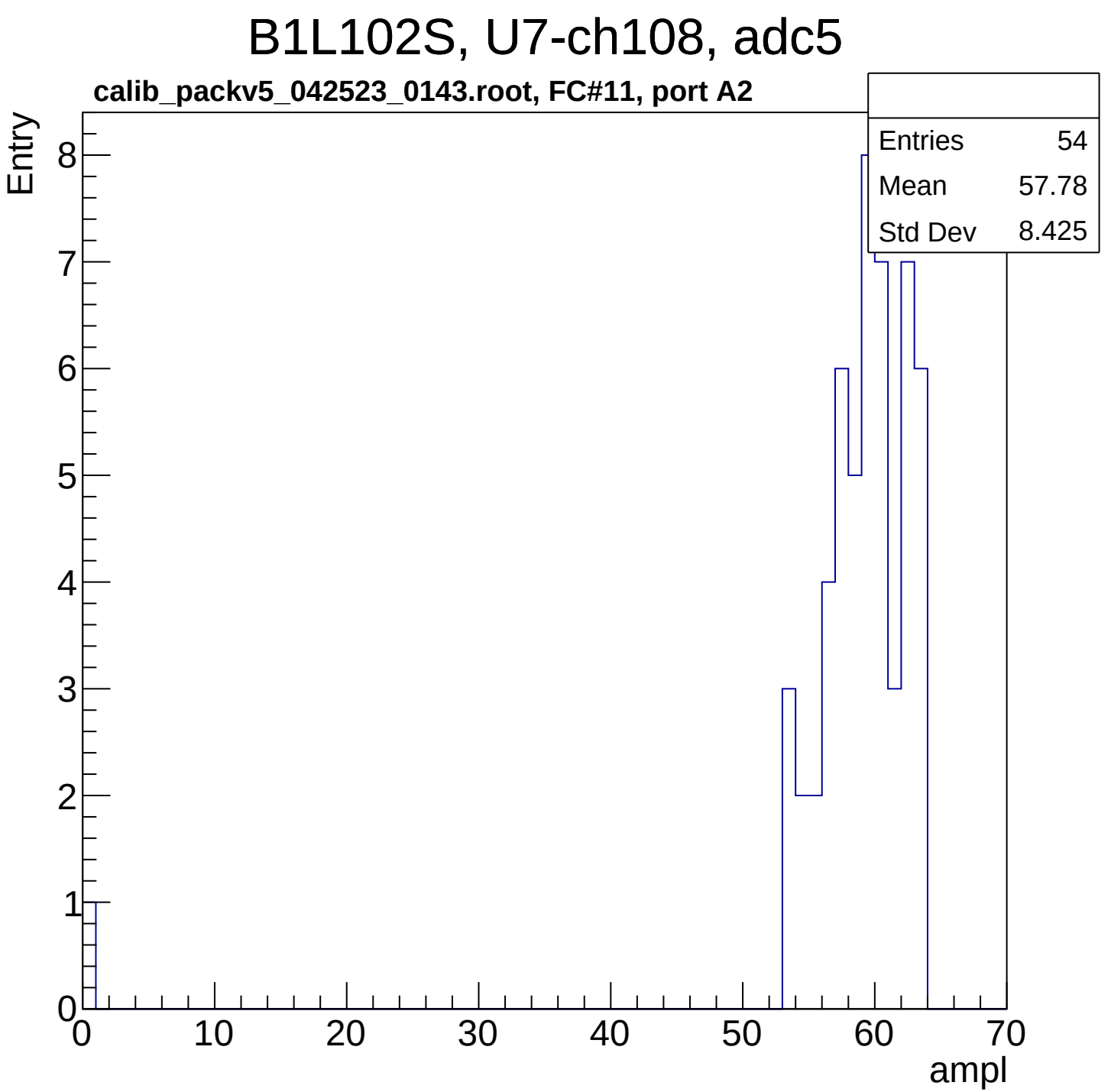
B1L102S, U7-ch108, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 54
Mean 57.78
Std Dev 8.425
Entry
ampl
0
1
2
3
4
5
6
7
8
0
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40
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60
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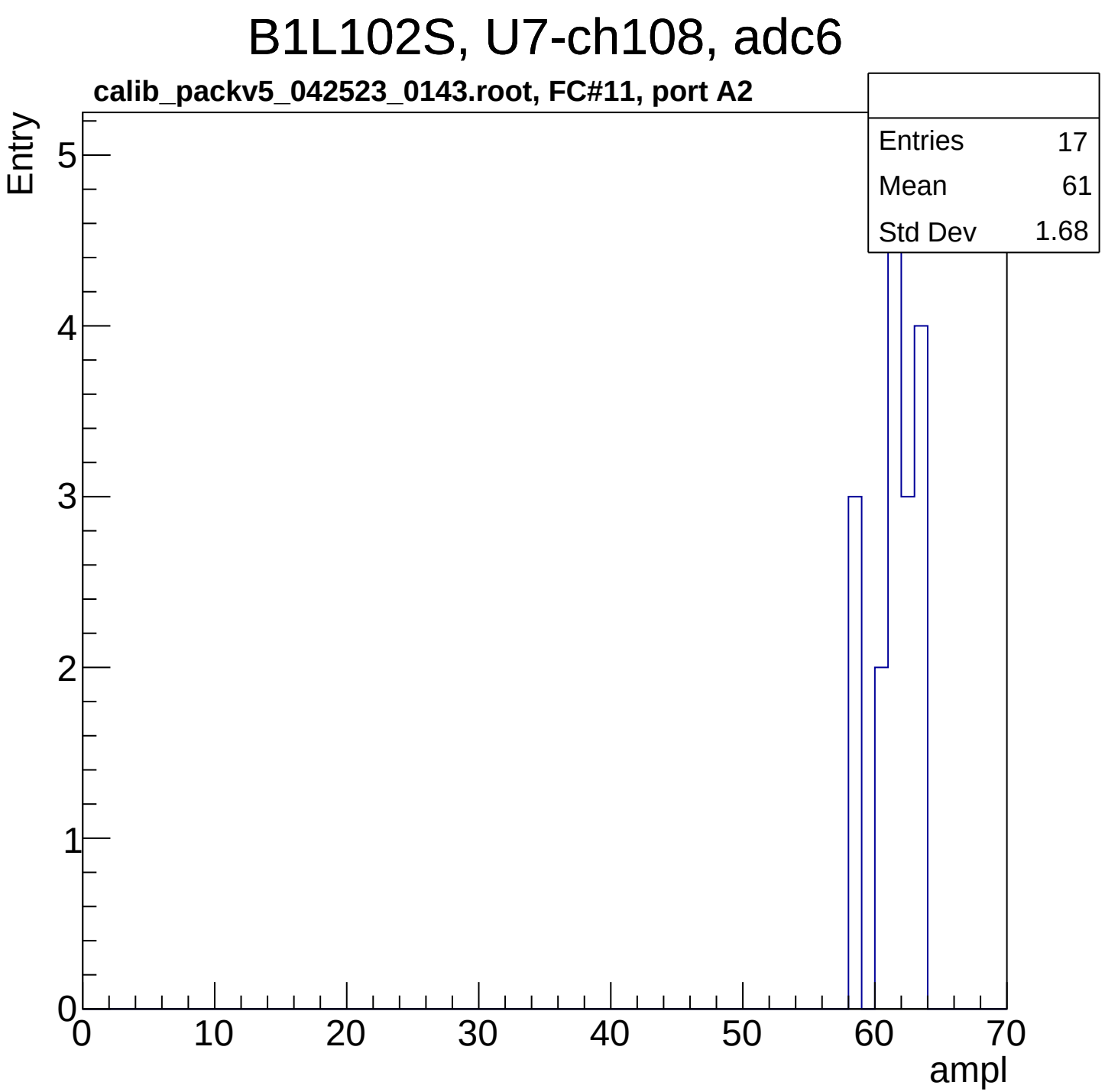
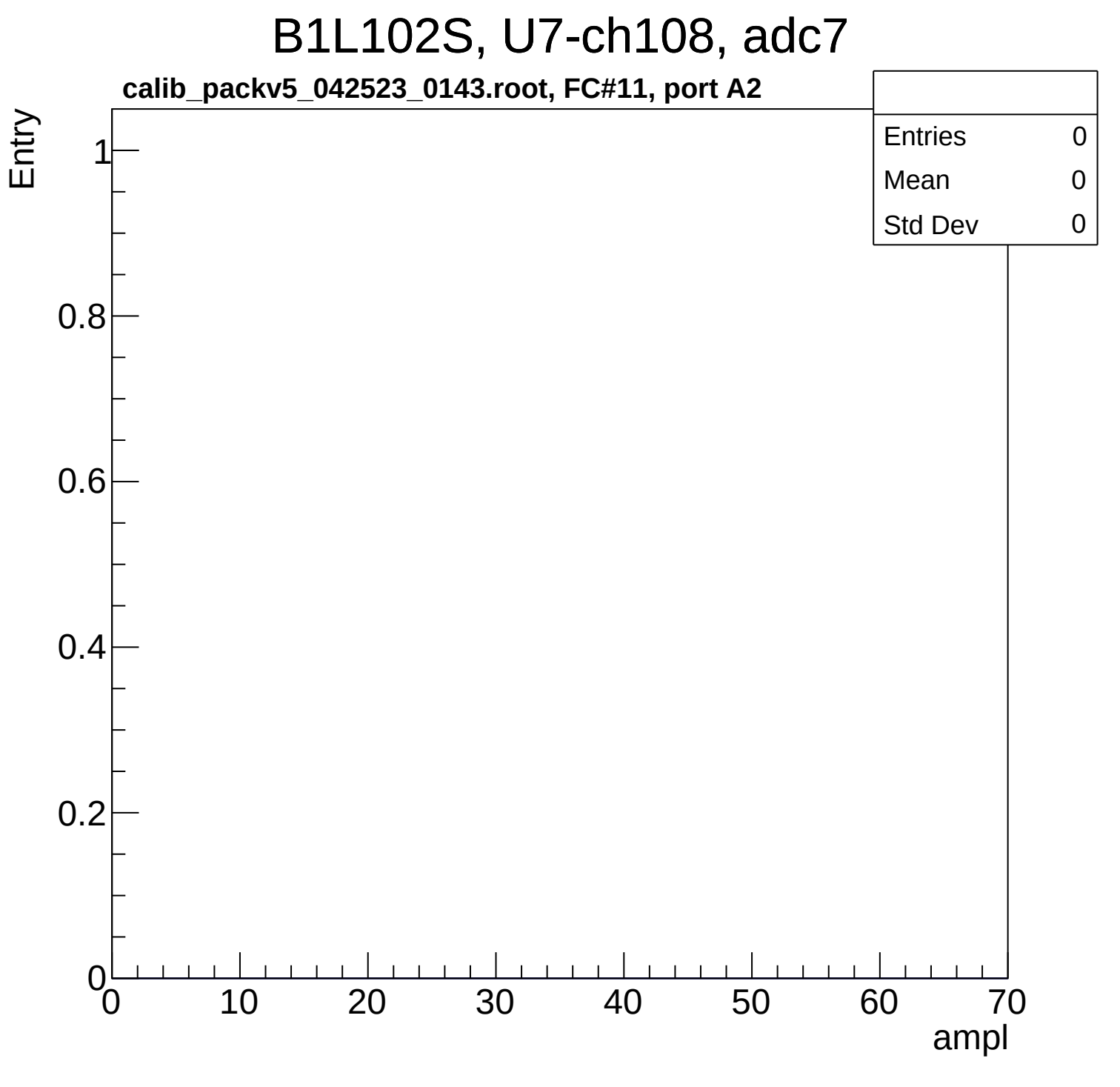
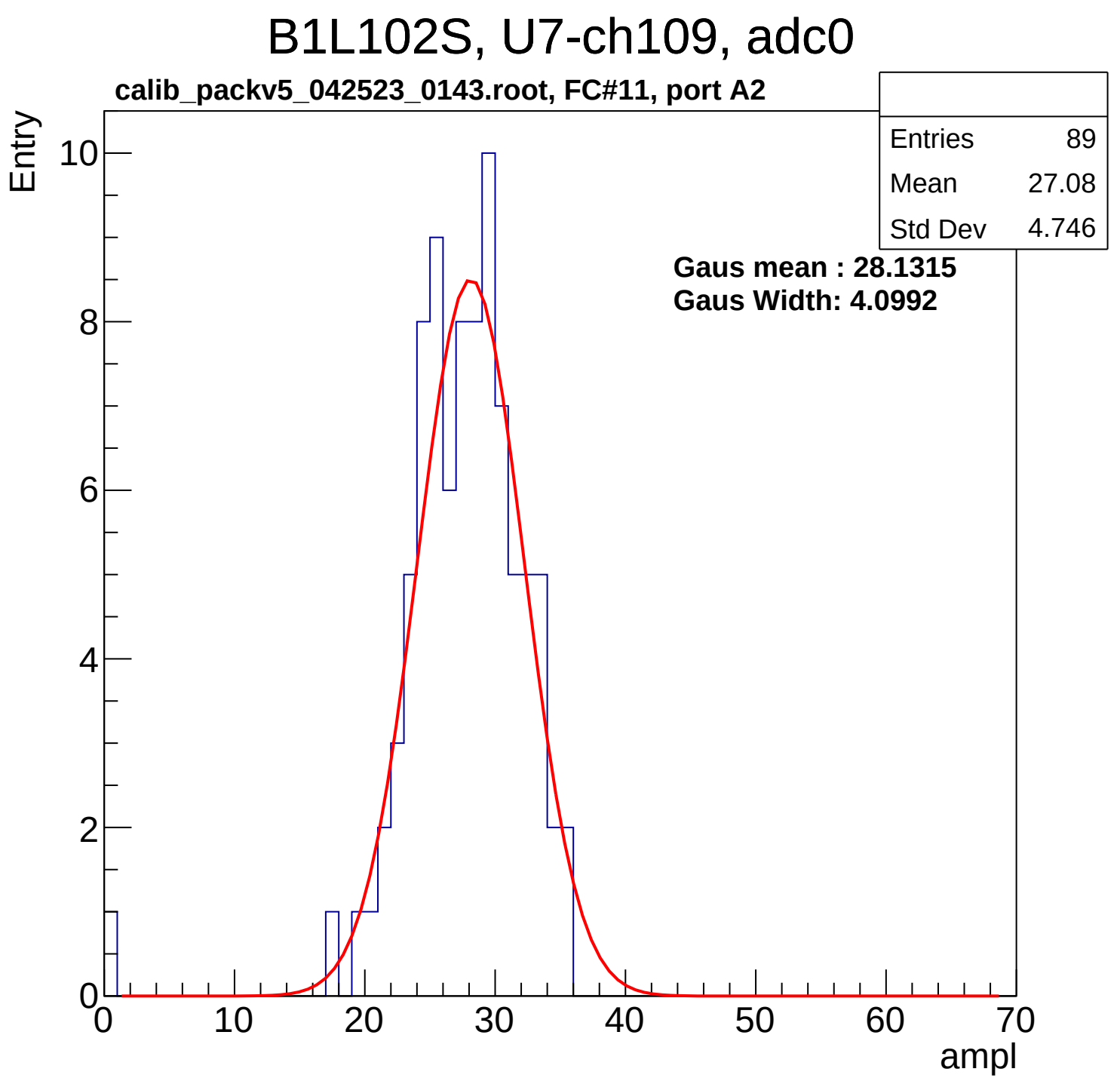
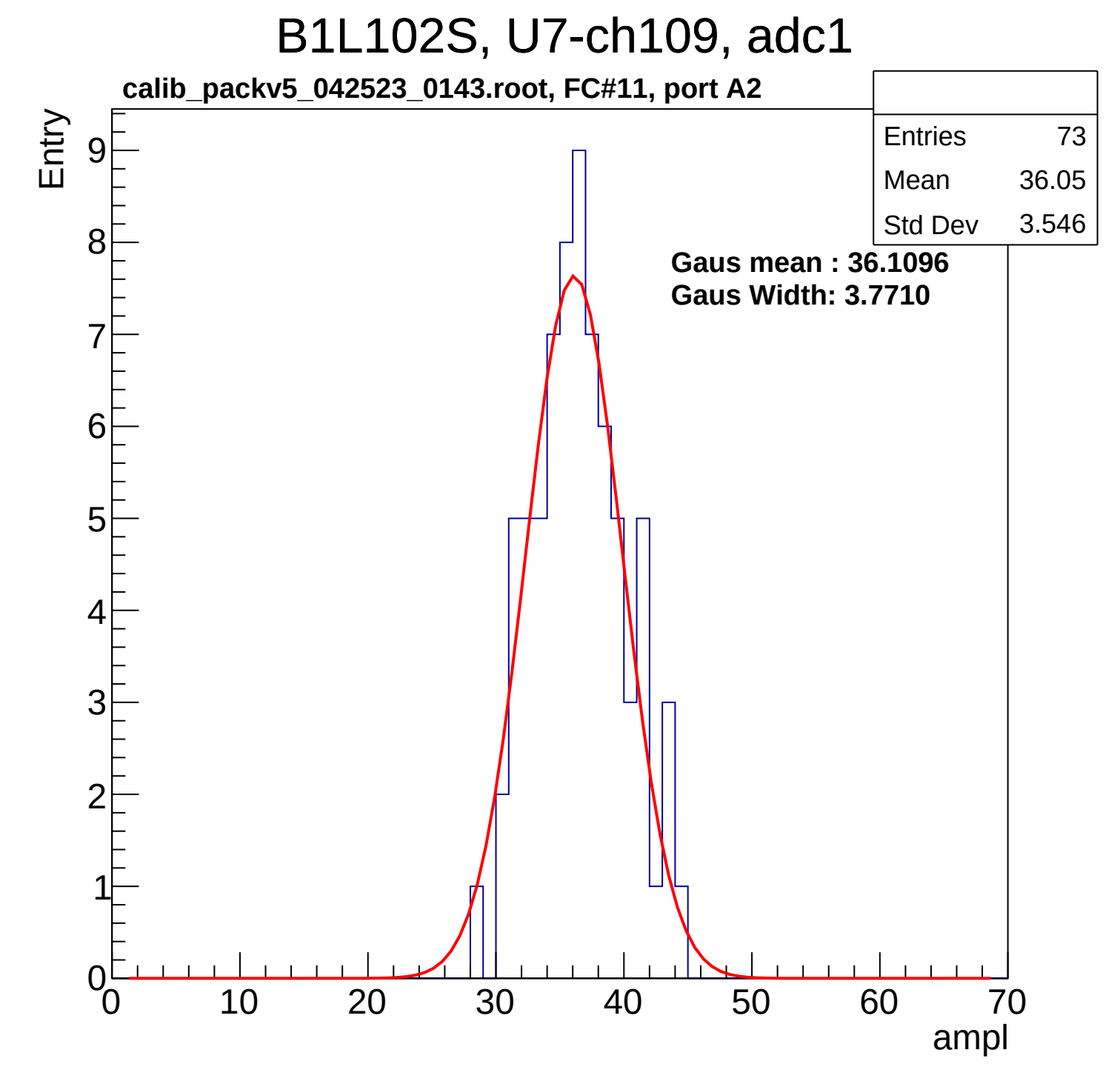

B1L102S, U7-ch108, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 17
Mean 61
Std Dev 1.68
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L102S, U7-ch108, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U7-ch109, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 89
Mean 27.08
Std Dev 4.746
Gaus mean : 28.1315
Gaus Width: 4.0992
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L102S, U7-ch109, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 73
Mean 36.05
Std Dev 3.546
Gaus mean : 36.1096
Gaus Width: 3.7710
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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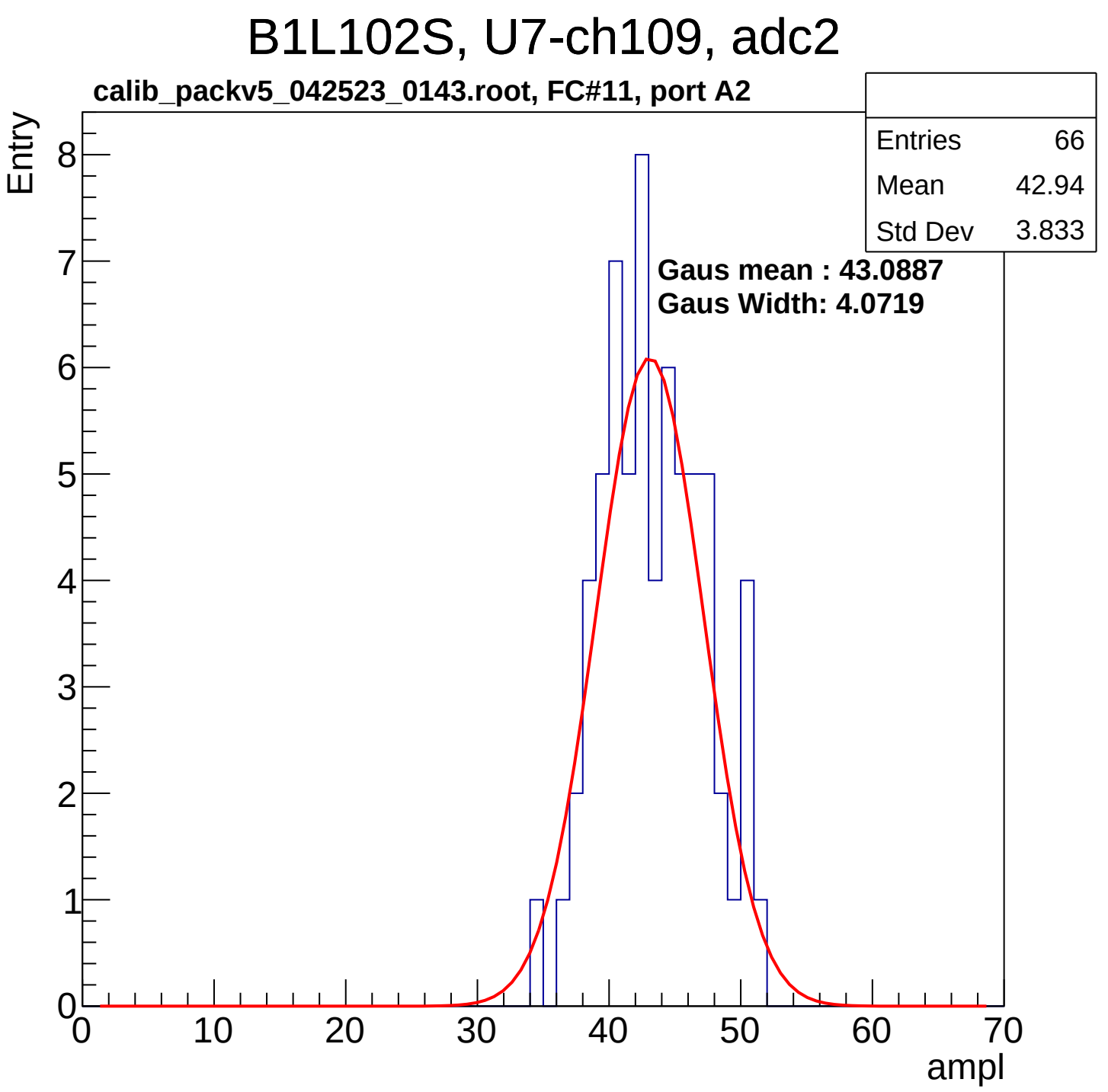
B1L102S, U7-ch109, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 66
Mean 42.94
Std Dev 3.833
Gaus mean : 43.0887
Gaus Width: 4.0719
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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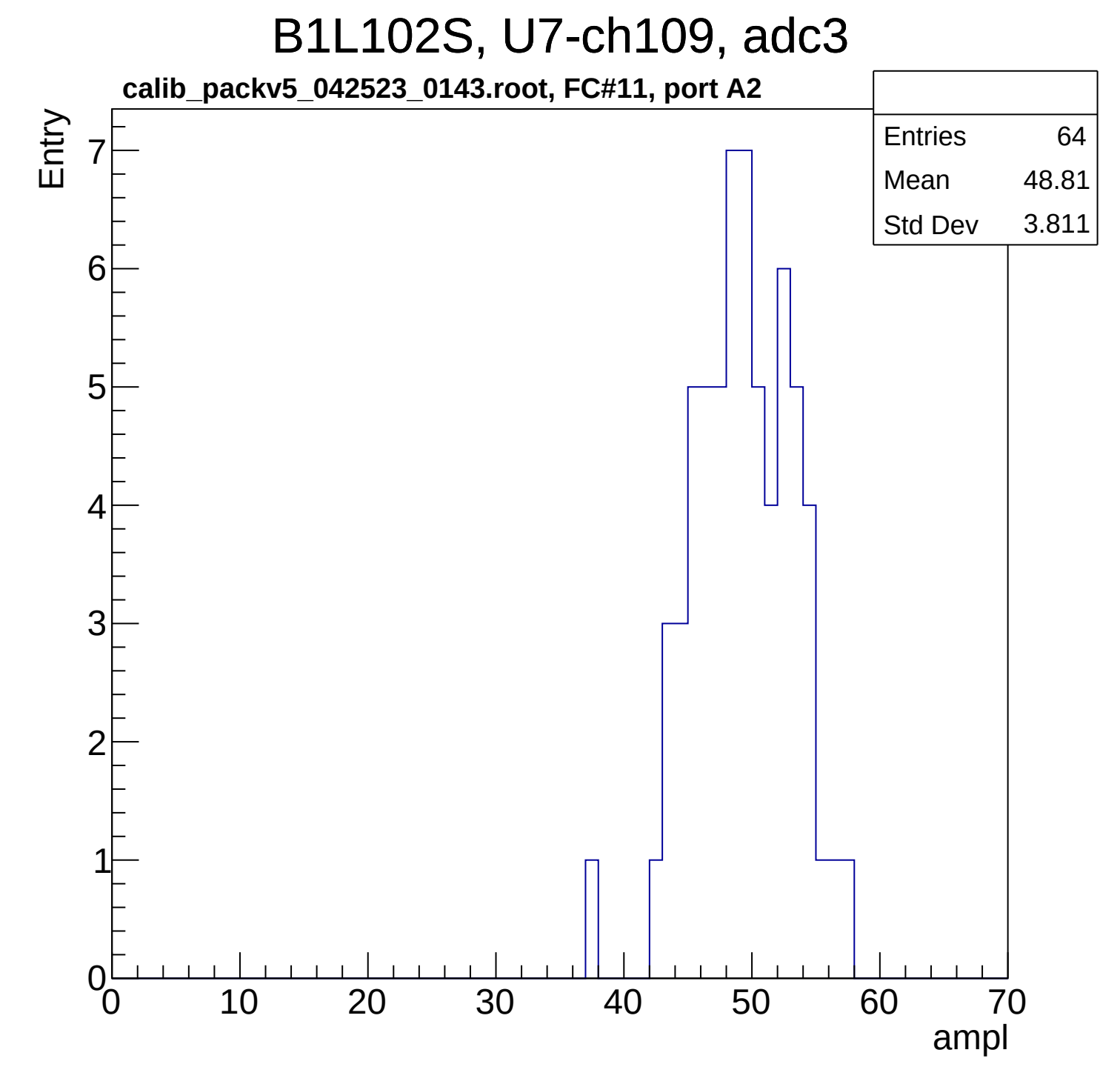
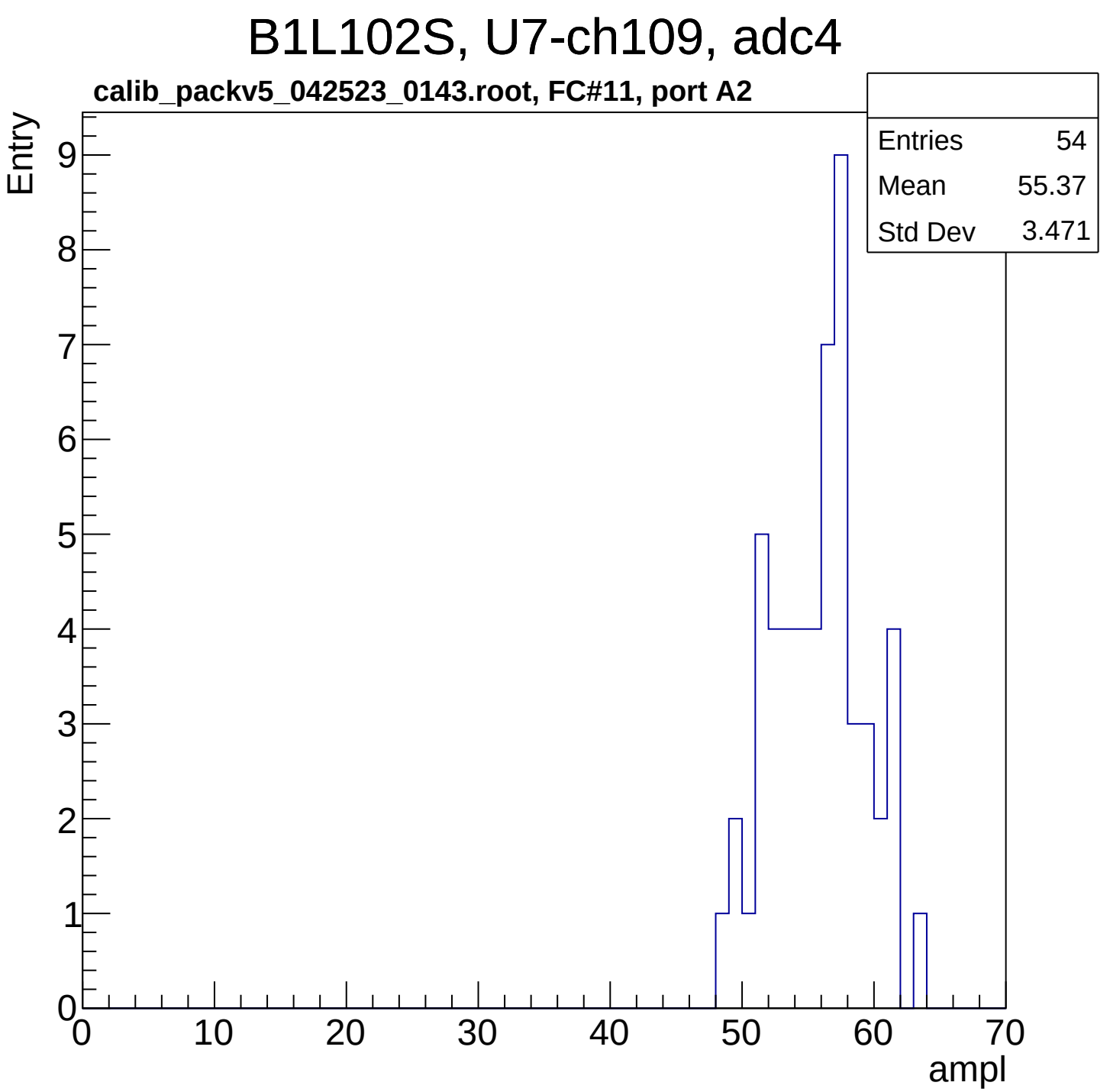

B1L102S, U7-ch109, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 64
Mean 48.81
Std Dev 3.811
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L102S, U7-ch109, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 54
Mean 55.37
Std Dev 3.471
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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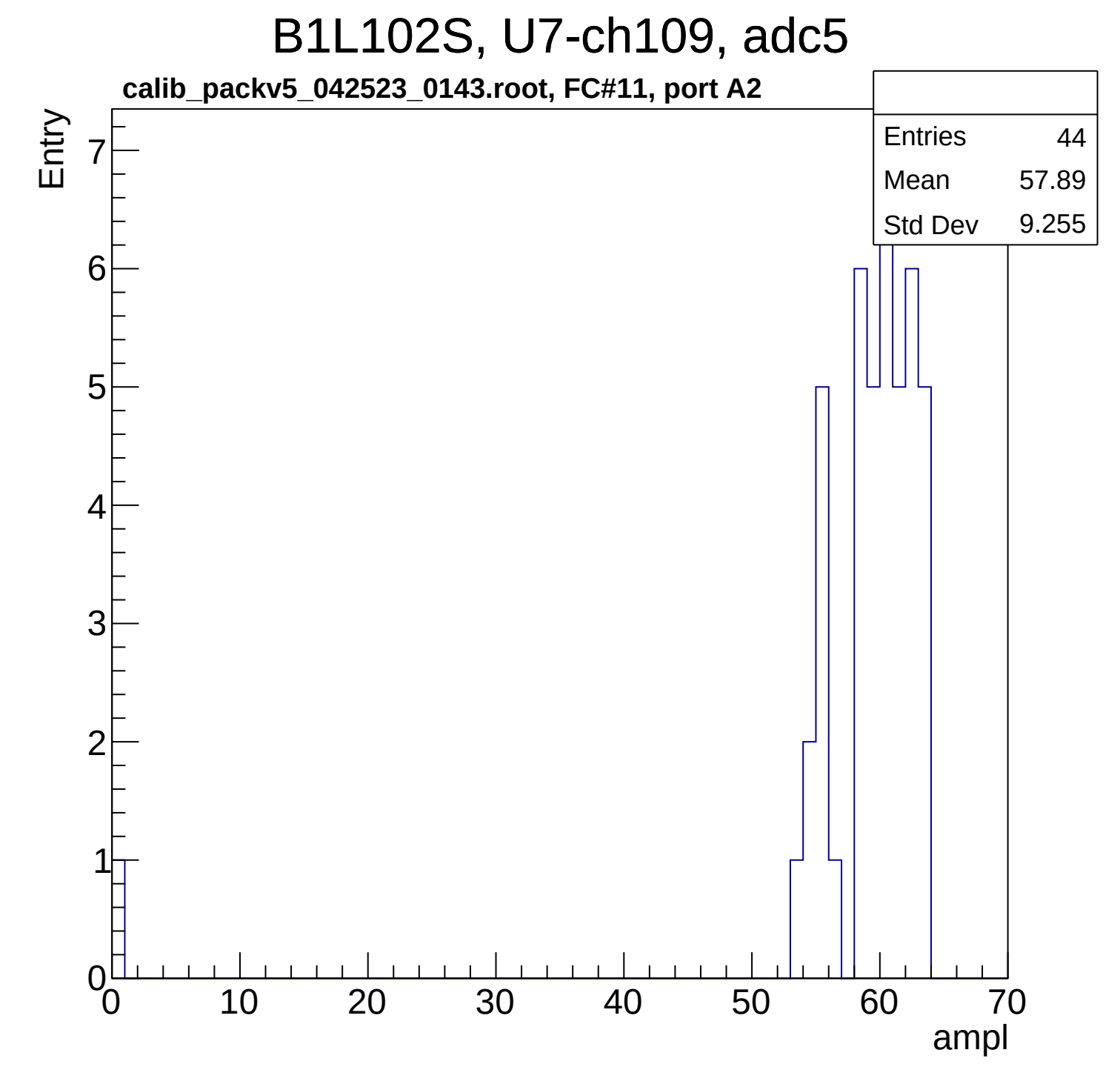
B1L102S, U7-ch109, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 44
Mean 57.89
Std Dev 9.255
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
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40
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60
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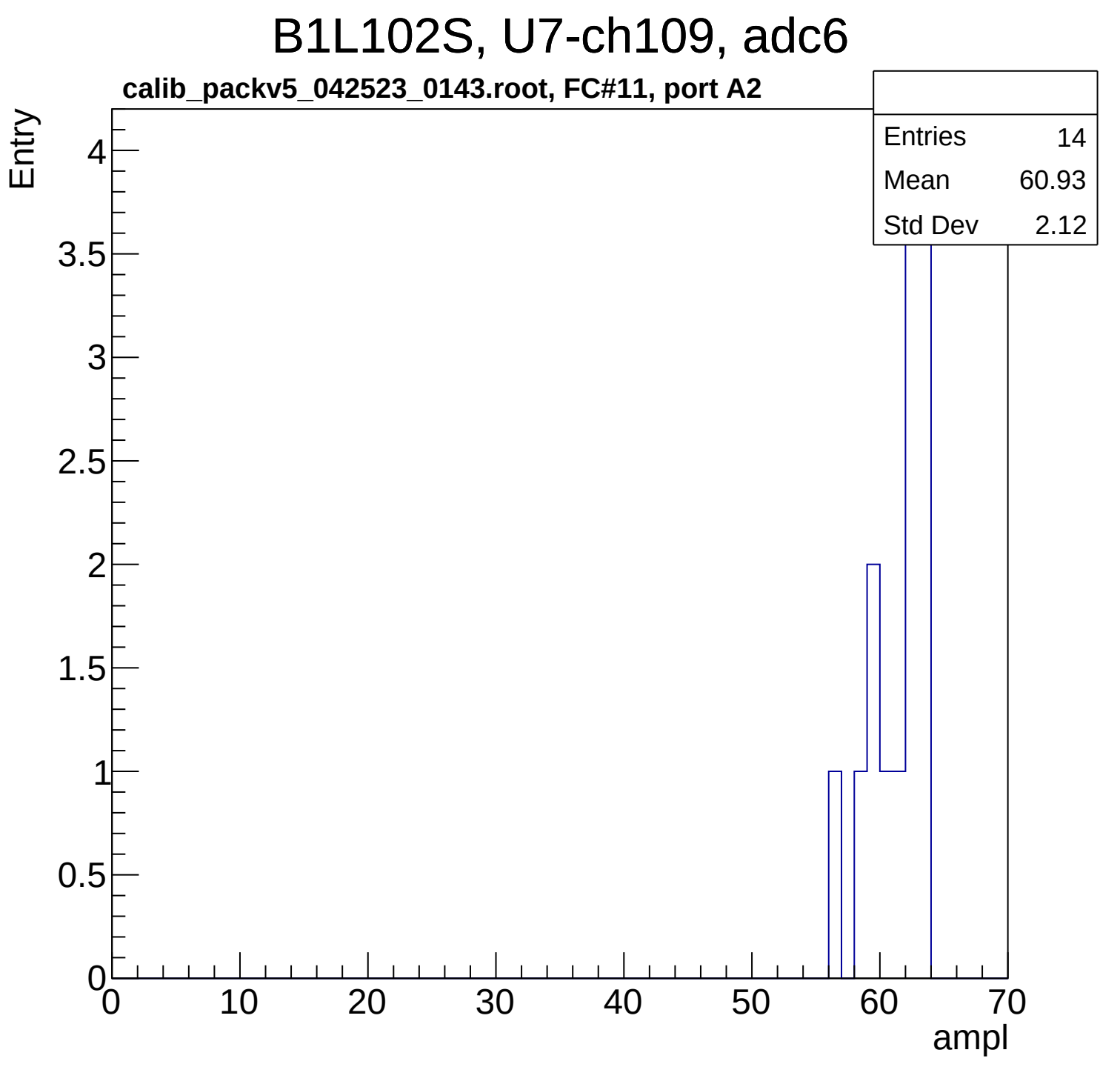
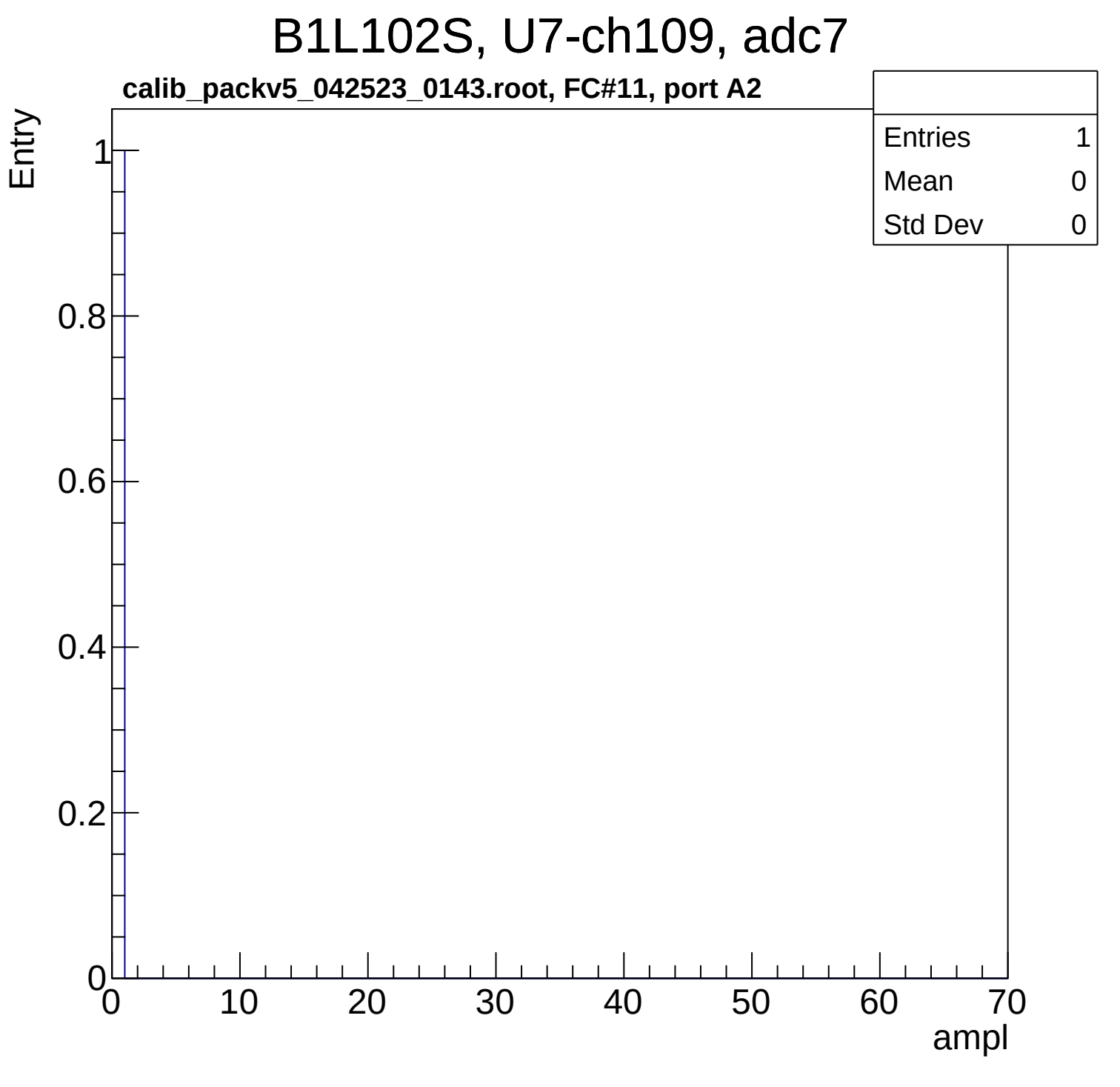
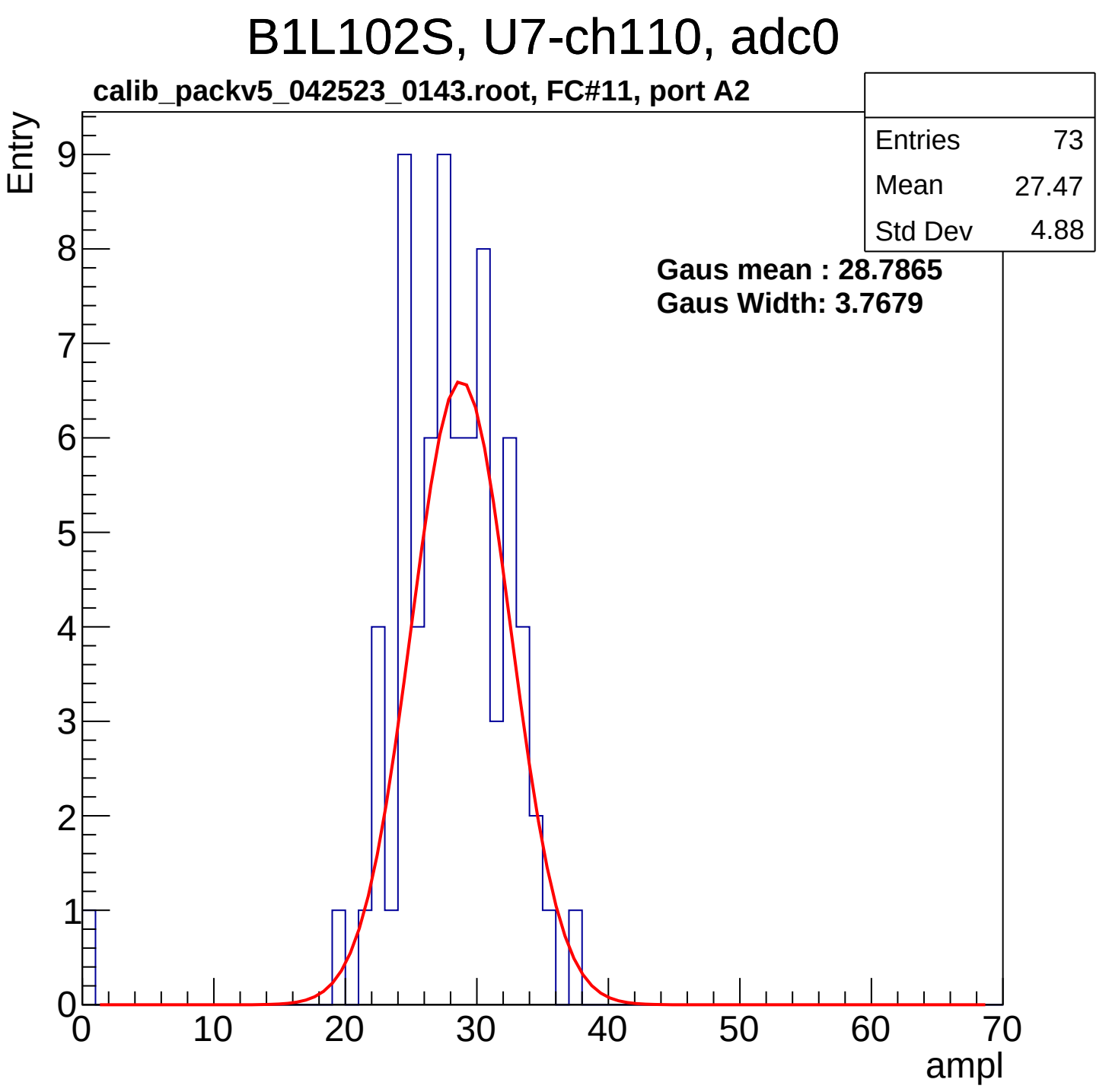
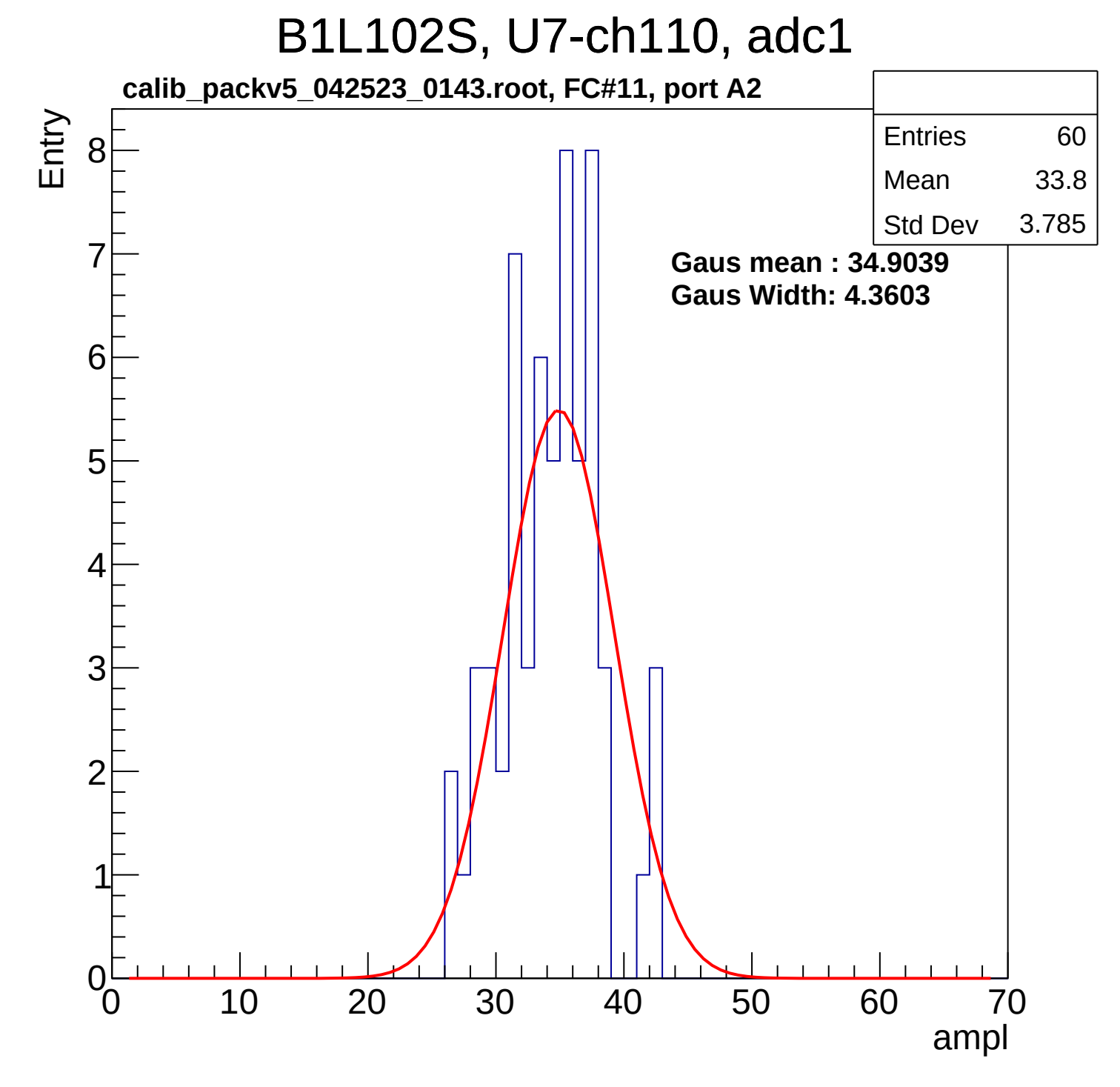

B1L102S, U7-ch109, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 14
Mean 60.93
Std Dev 2.12
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L102S, U7-ch109, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U7-ch110, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 73
Mean 27.47
Std Dev 4.88
Gaus mean : 28.7865
Gaus Width: 3.7679
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L102S, U7-ch110, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 60
Mean 33.8
Std Dev 3.785
Gaus mean : 34.9039
Gaus Width: 4.3603
Entry
ampl
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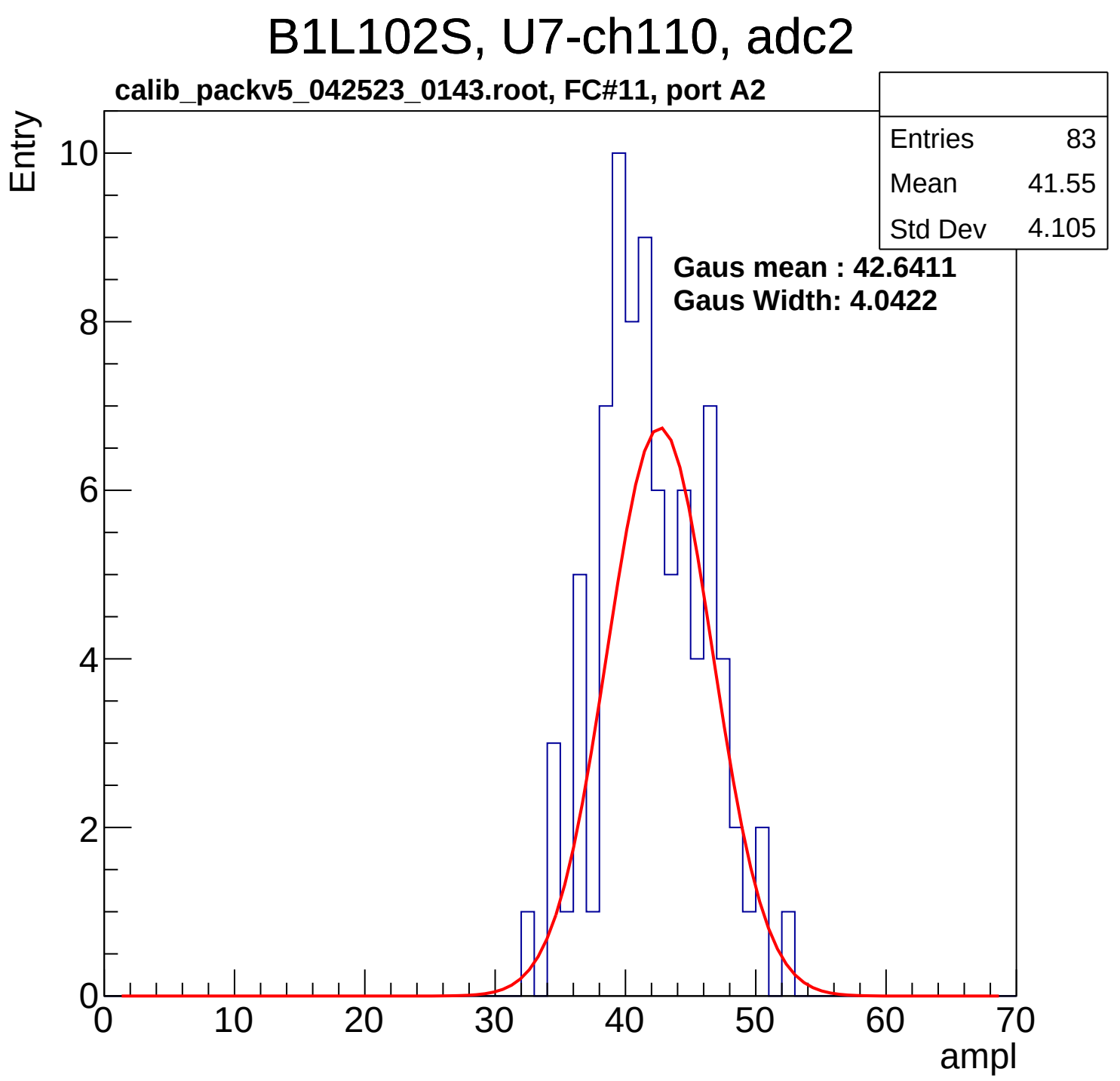
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L102S, U7-ch110, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 83
Mean 41.55
Std Dev 4.105
Gaus mean : 42.6411
Gaus Width: 4.0422
Entry
ampl
0
2
4
6
8
10
0
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20
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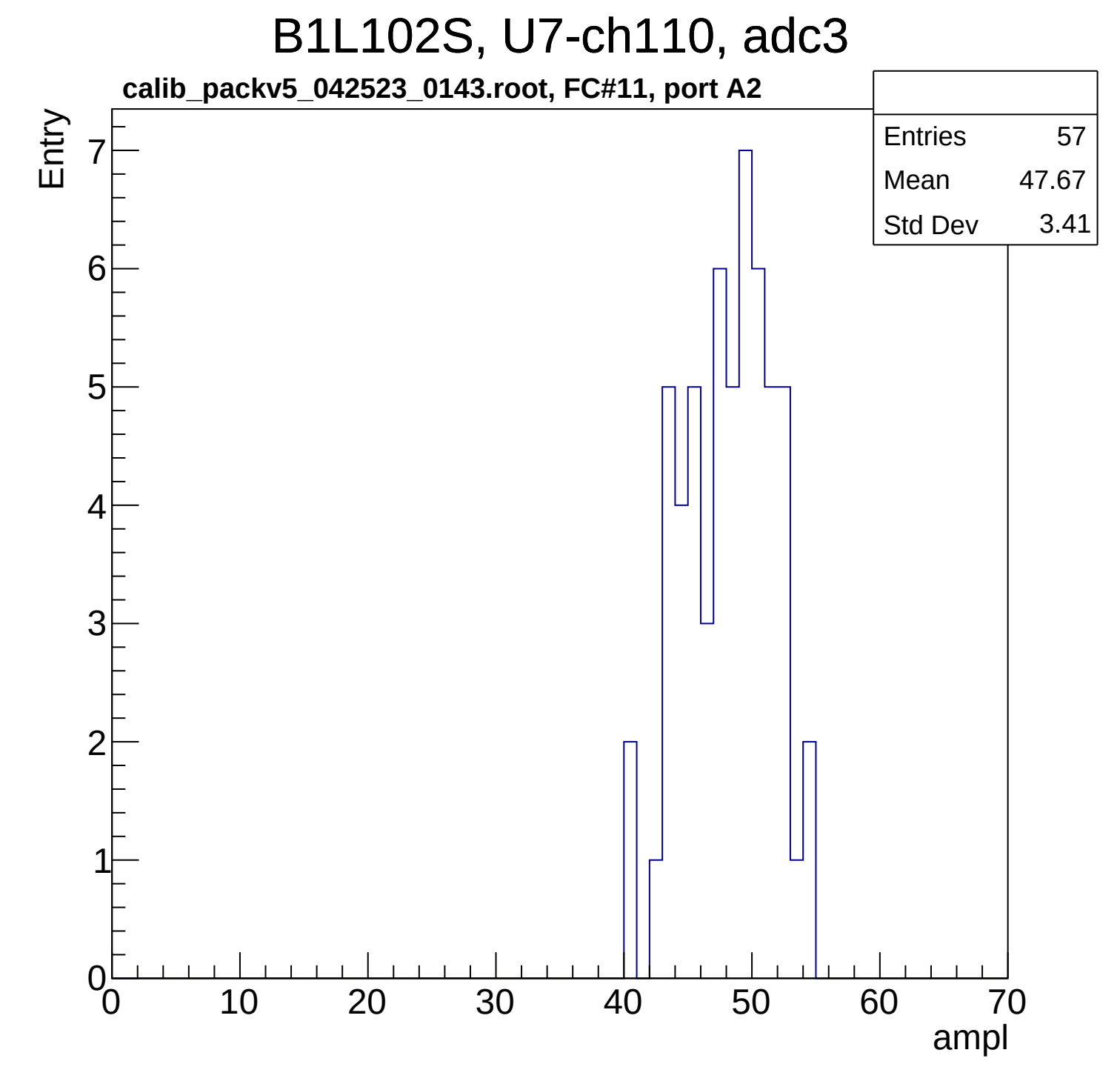
40
50
60
70


B1L102S, U7-ch110, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 57
Mean 47.67
Std Dev 3.41
Entry
ampl
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1
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3
4
5
6
7
0
10
20
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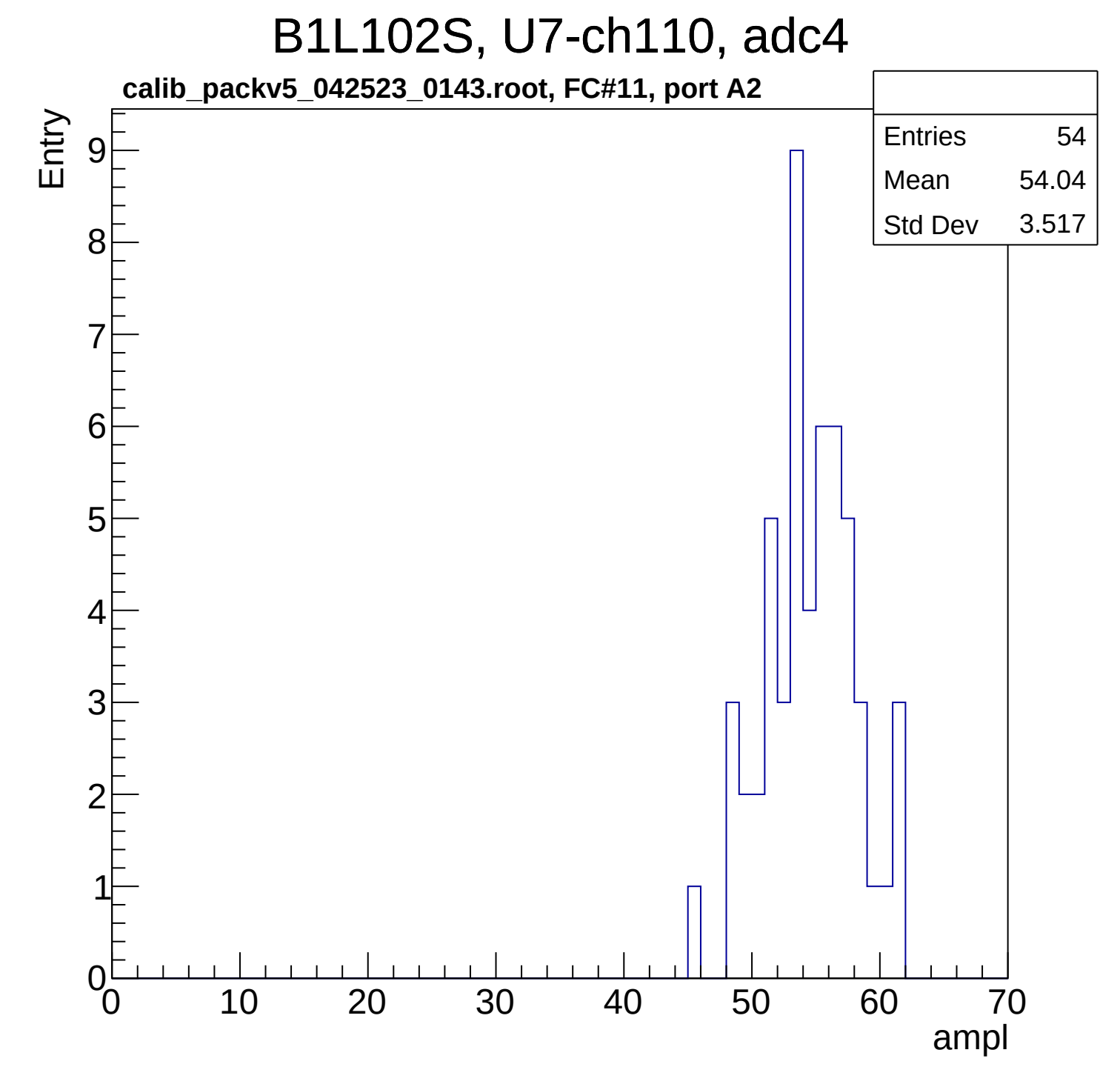
40
50
60
70


B1L102S, U7-ch110, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 54
Mean 54.04
Std Dev 3.517
Entry
ampl
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2
3
4
5
6
7
8
9
0
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60
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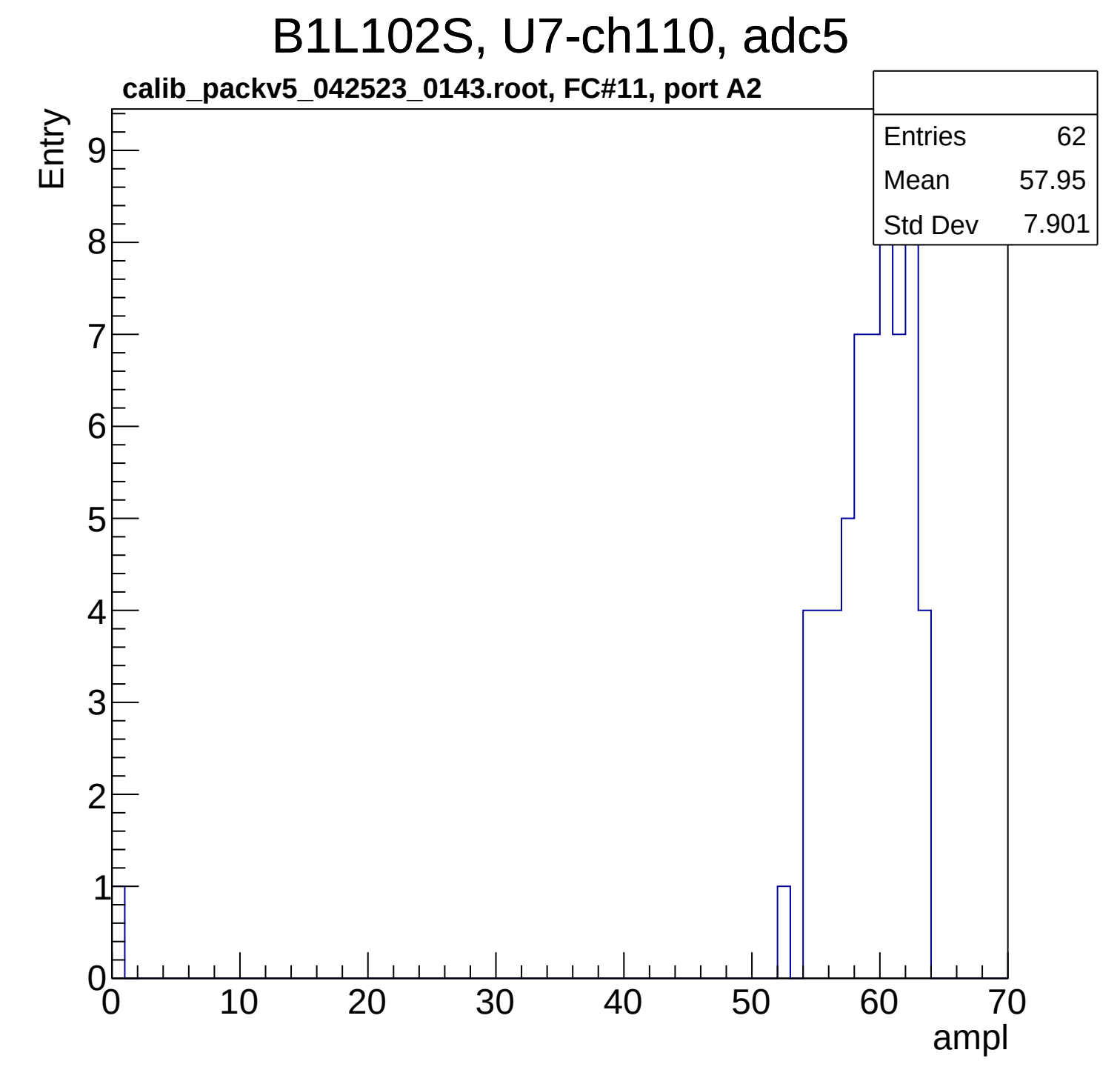
B1L102S, U7-ch110, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 62
Mean 57.95
Std Dev 7.901
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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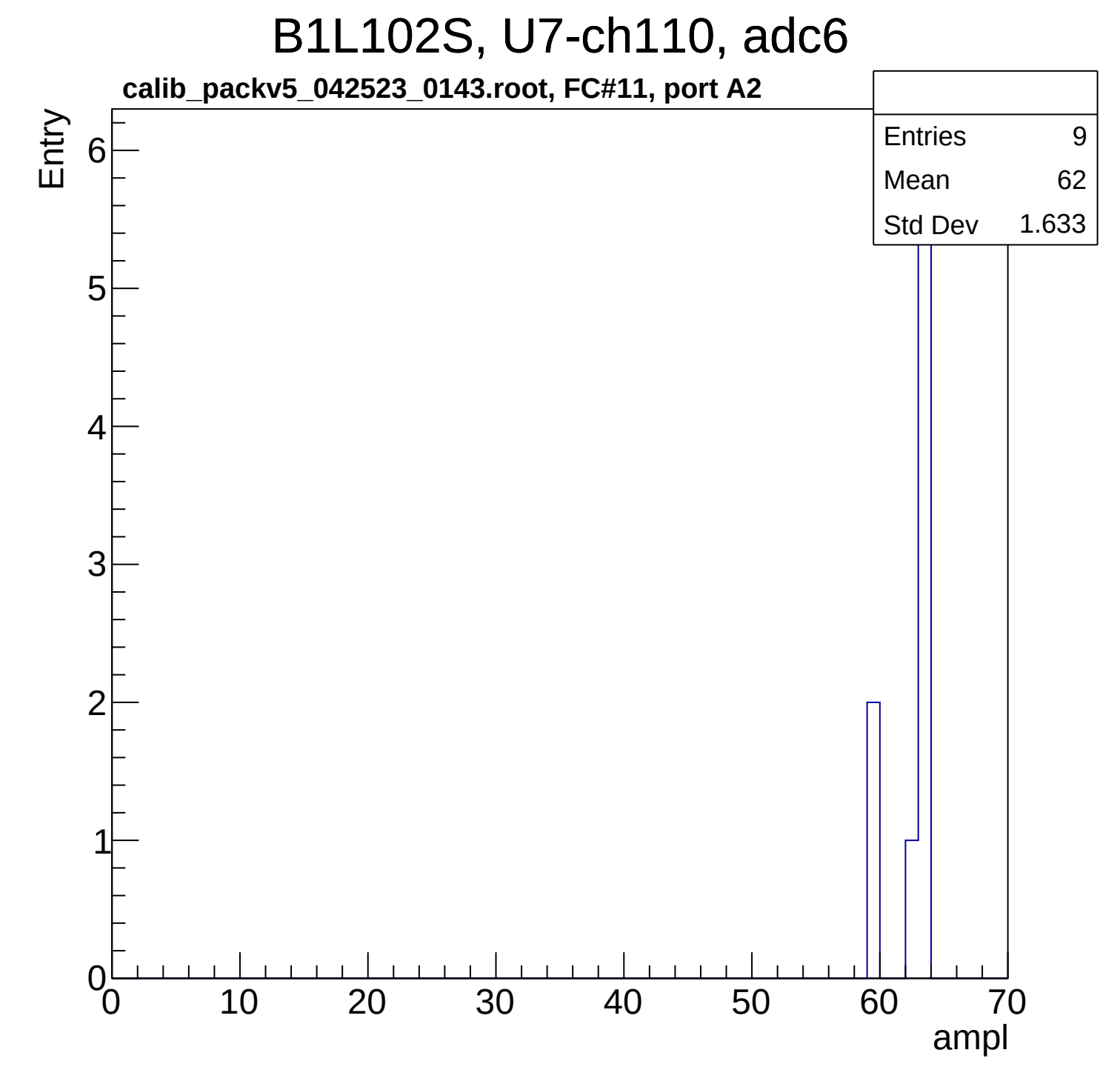
40
50
60
70


B1L102S, U7-ch110, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 9
Mean 62
Std Dev 1.633
Entry
0
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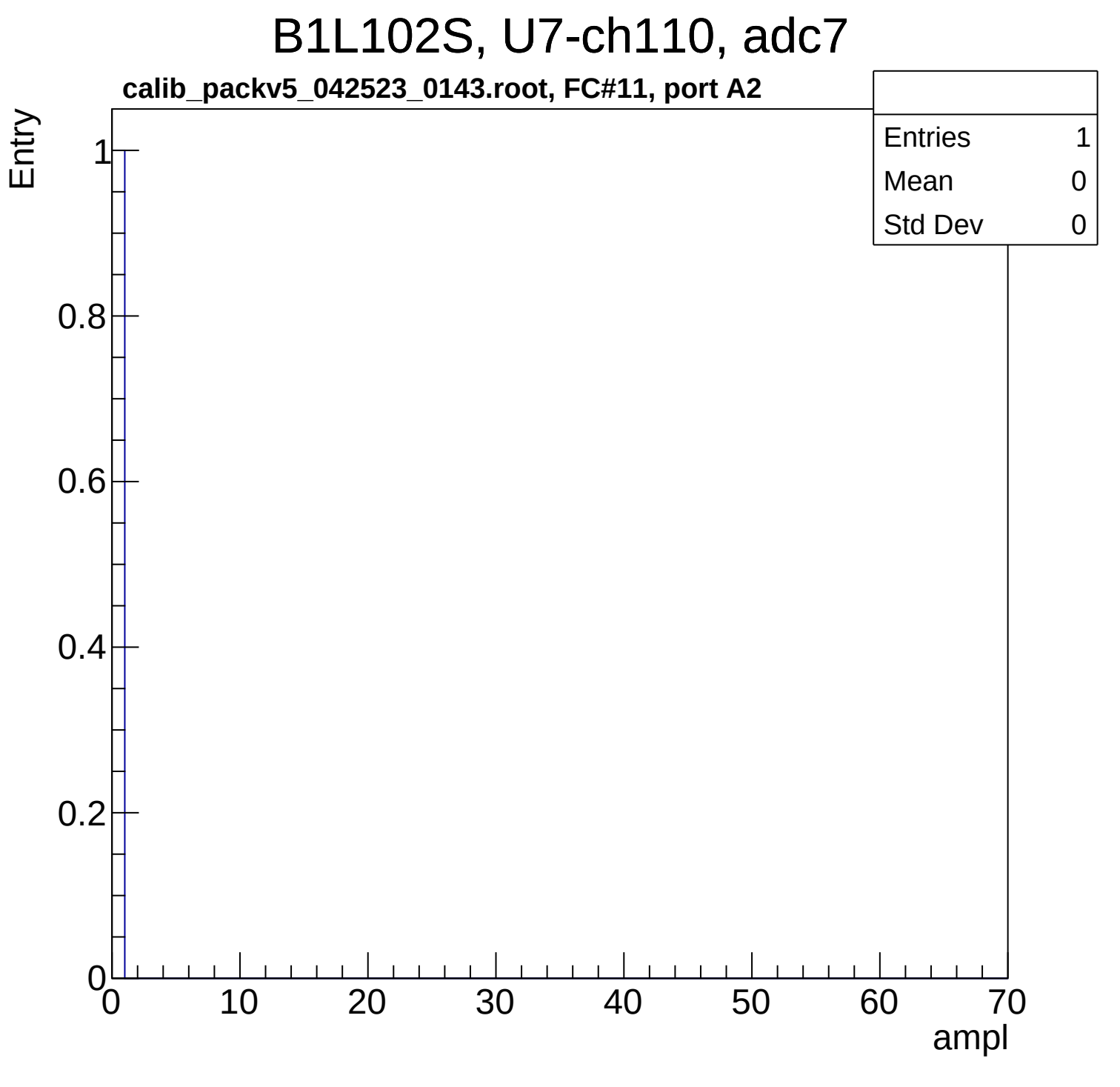
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L102S, U7-ch110, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 1
Mean 0
Std Dev 0
Entry
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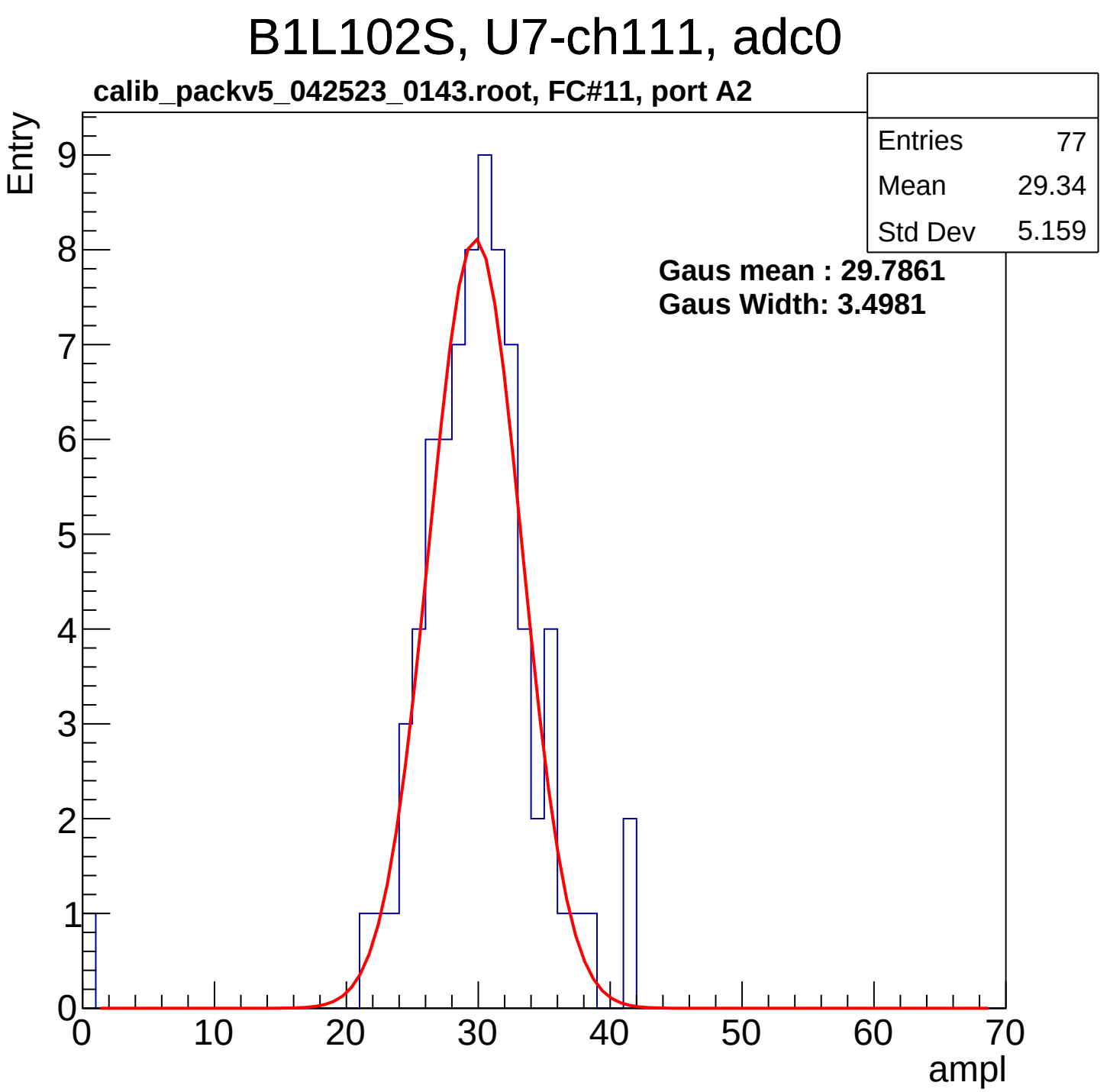
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U7-ch111, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 77
Mean 29.34
Std Dev 5.159
Gaus mean : 29.7861
Gaus Width: 3.4981
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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40
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60
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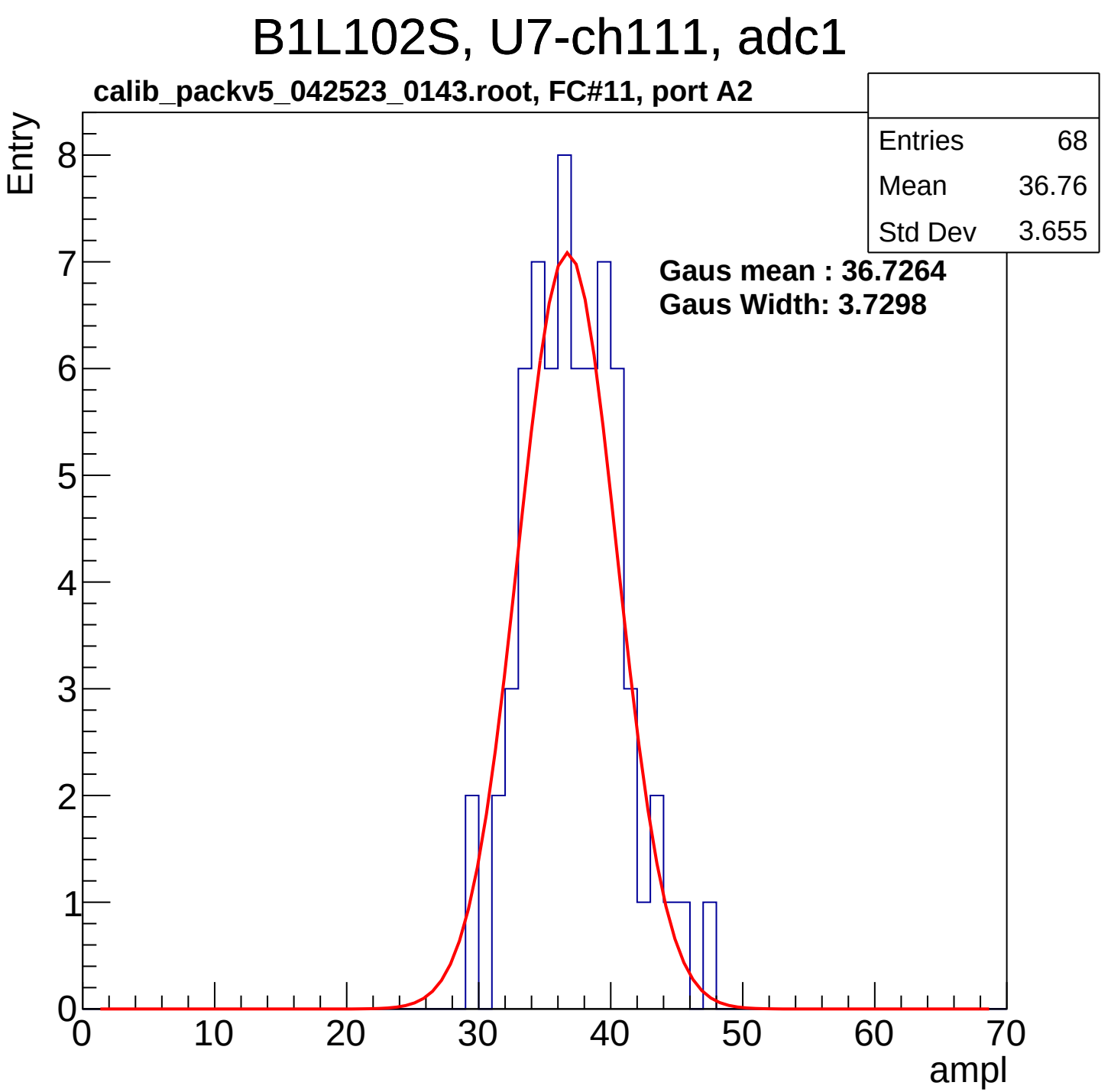
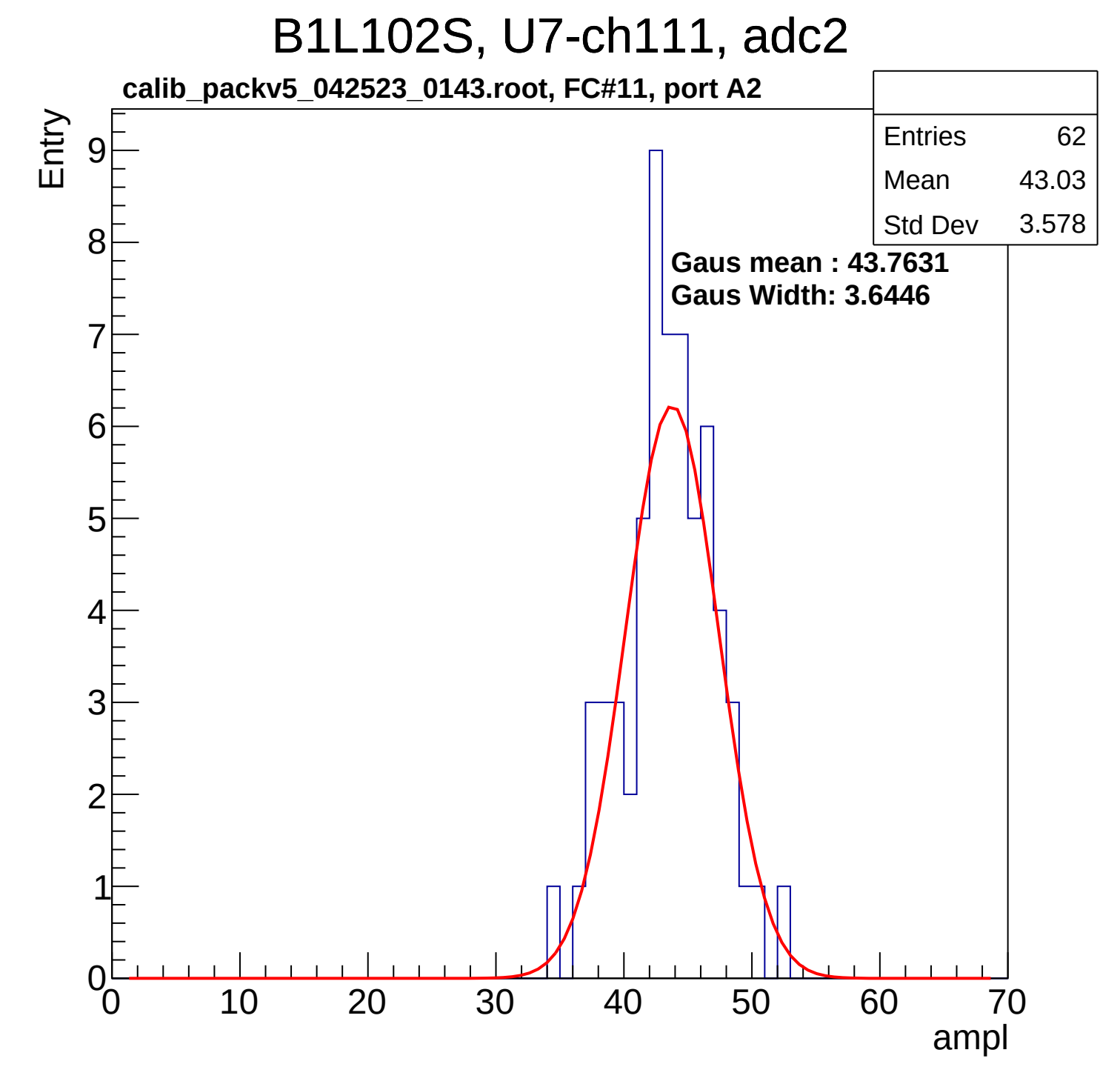

B1L102S, U7-ch111, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 68
Mean 36.76
Std Dev 3.655
Gaus mean : 36.7264
Gaus Width: 3.7298
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L102S, U7-ch111, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 62
Mean 43.03
Std Dev 3.578
Gaus mean : 43.7631
Gaus Width: 3.6446
Entry
ampl
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10
20
30
40
50
60
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1
2
3
4
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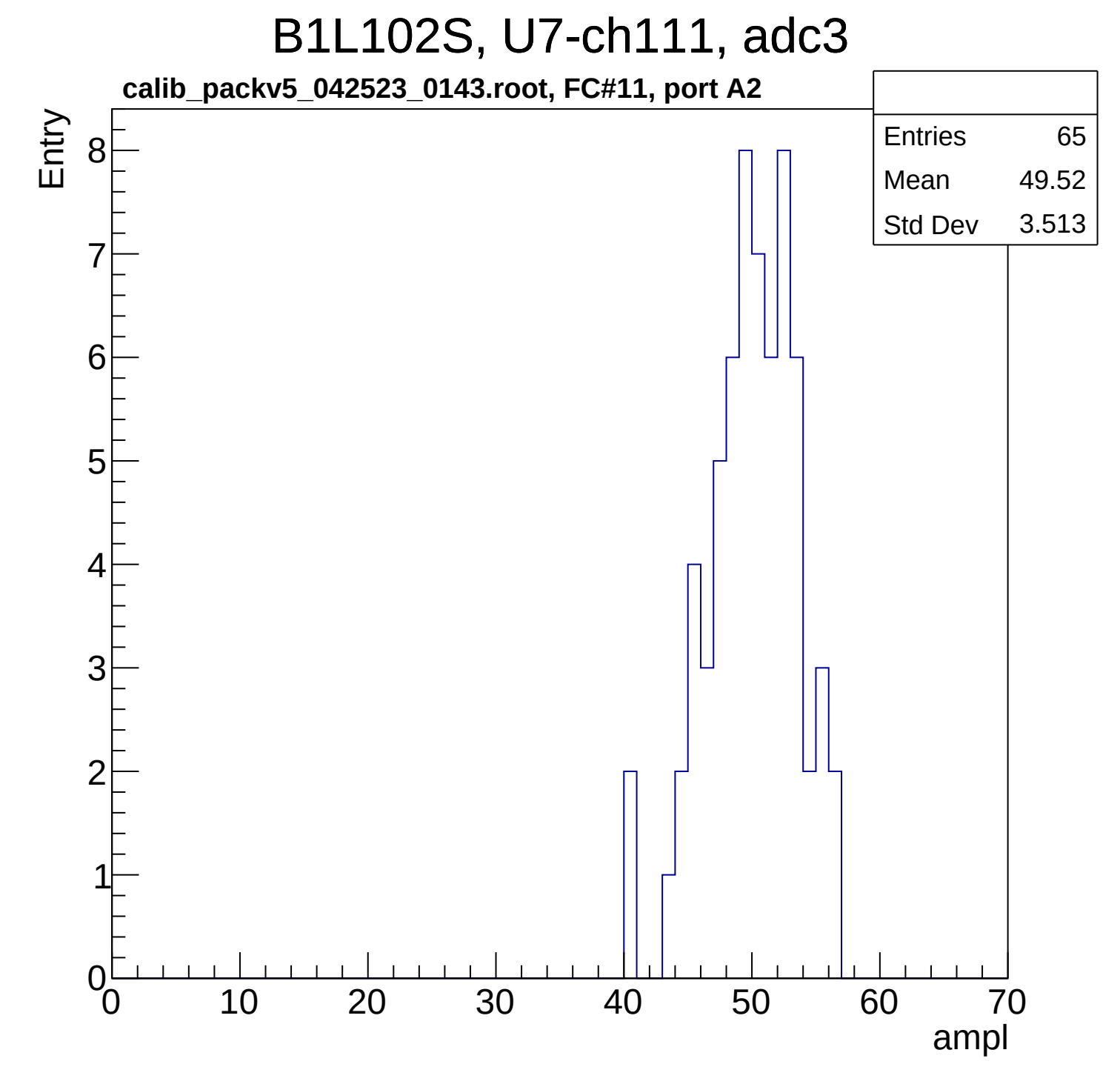
6
7
8
9


B1L102S, U7-ch111, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 65
Mean 49.52
Std Dev 3.513
Entry
ampl
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3
4
5
6
7
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0
10
20
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40
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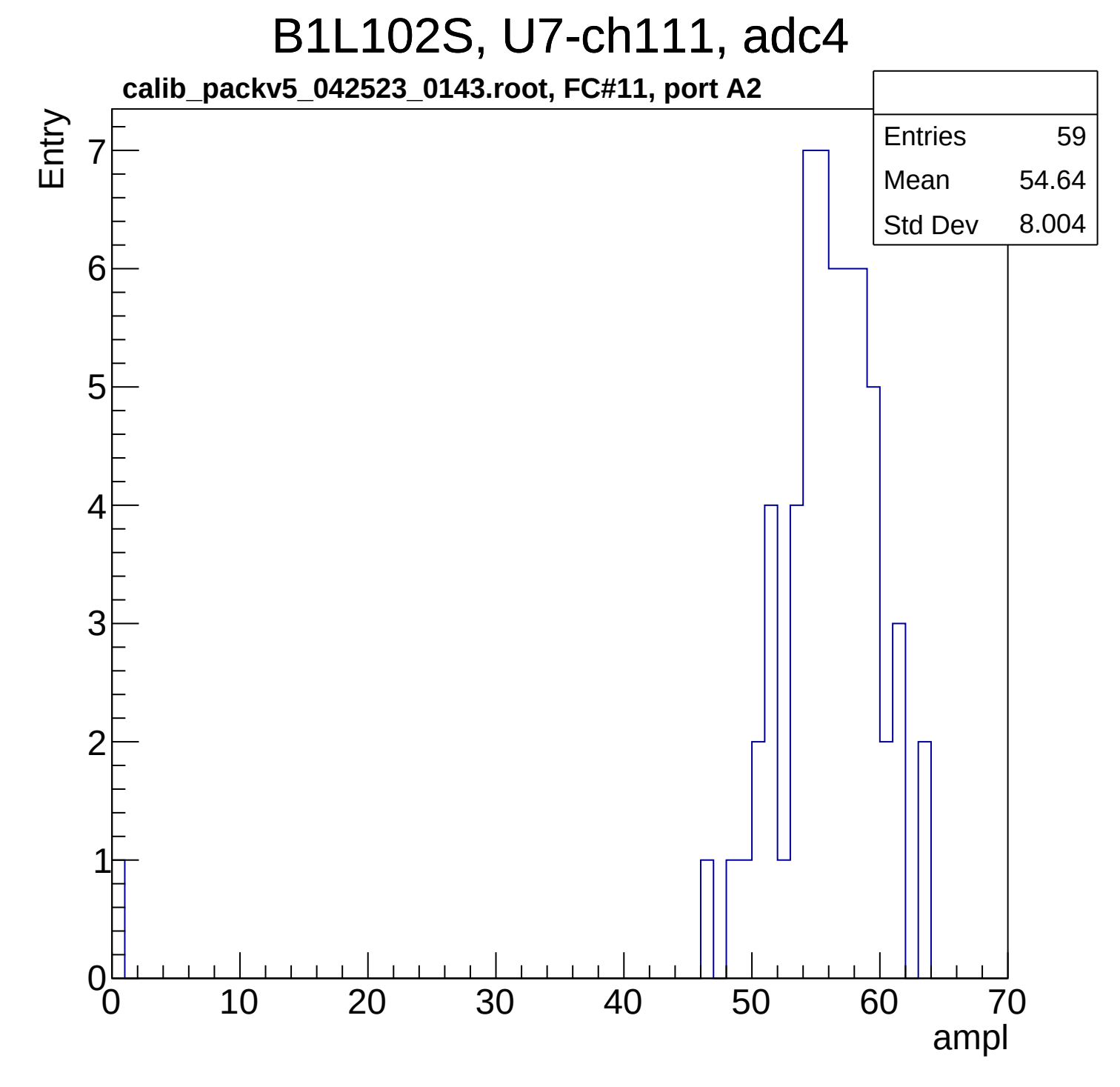
B1L102S, U7-ch111, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 59
Mean 54.64
Std Dev 8.004
Entry
ampl
0
1
2
3
4
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6
7
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40
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60
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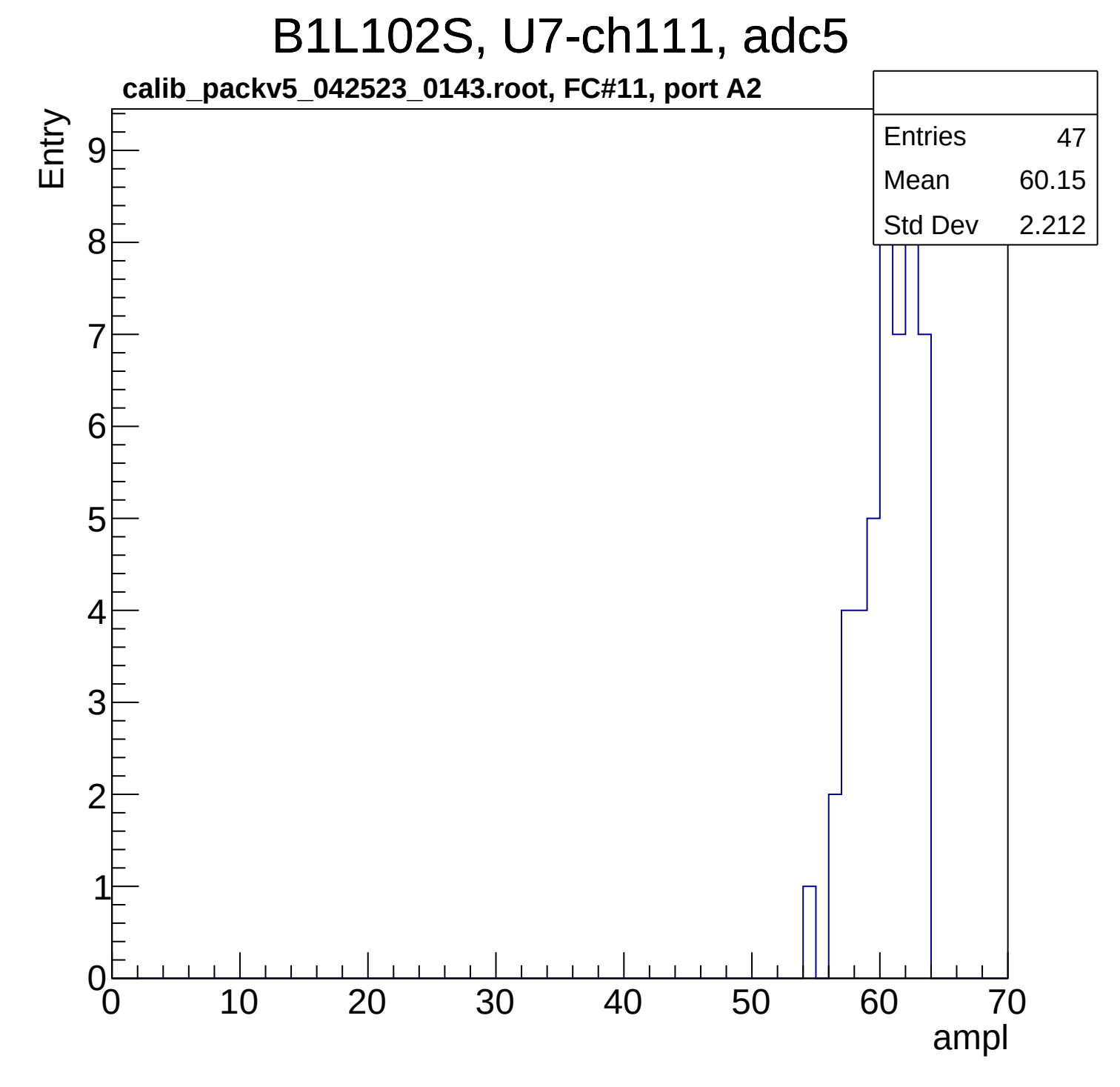
B1L102S, U7-ch111, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 47
Mean 60.15
Std Dev 2.212
Entry
ampl
0
1
2
3
4
5
6
7
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0
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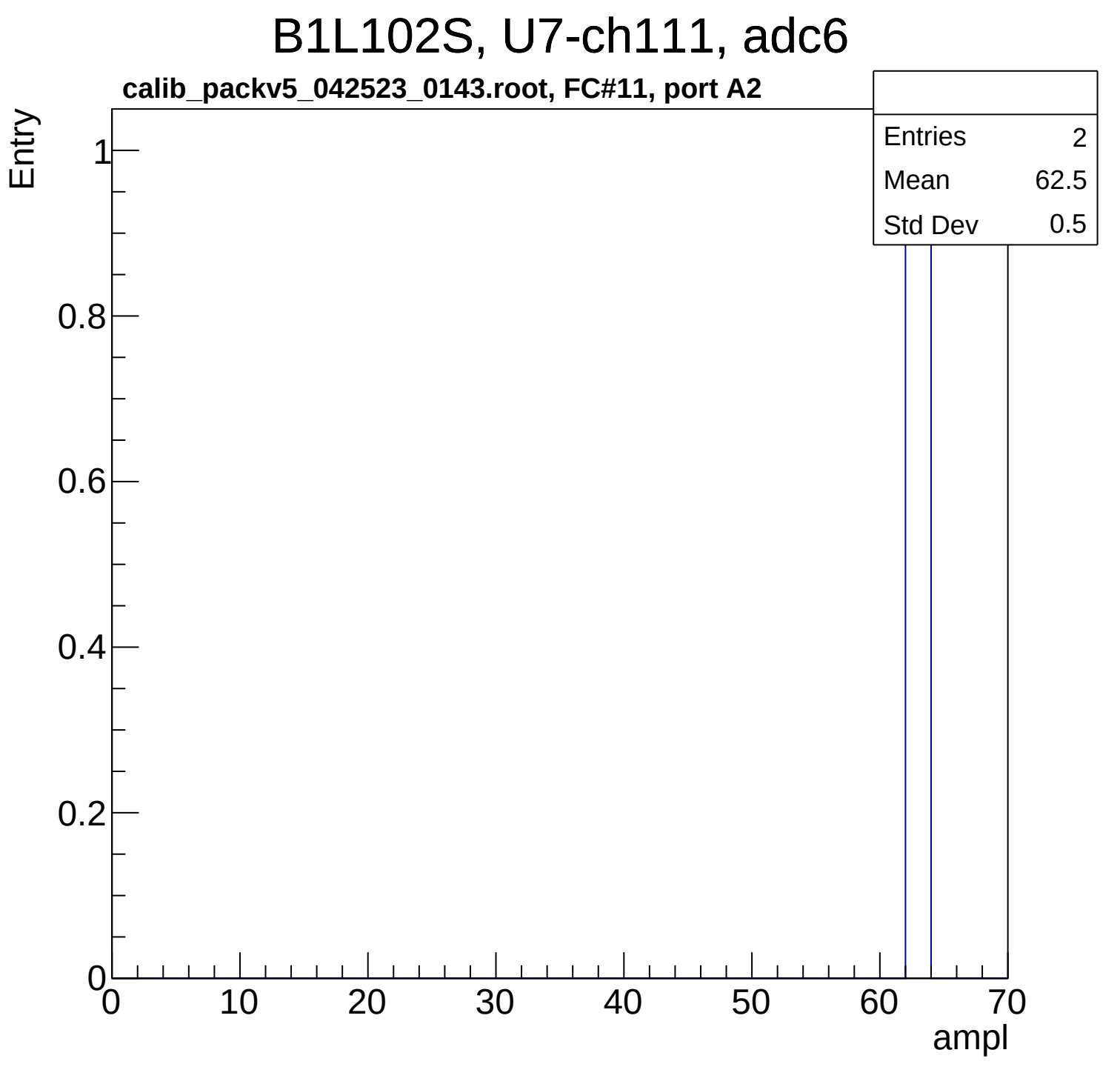
B1L102S, U7-ch111, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 2
Mean 62.5
Std Dev 0.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
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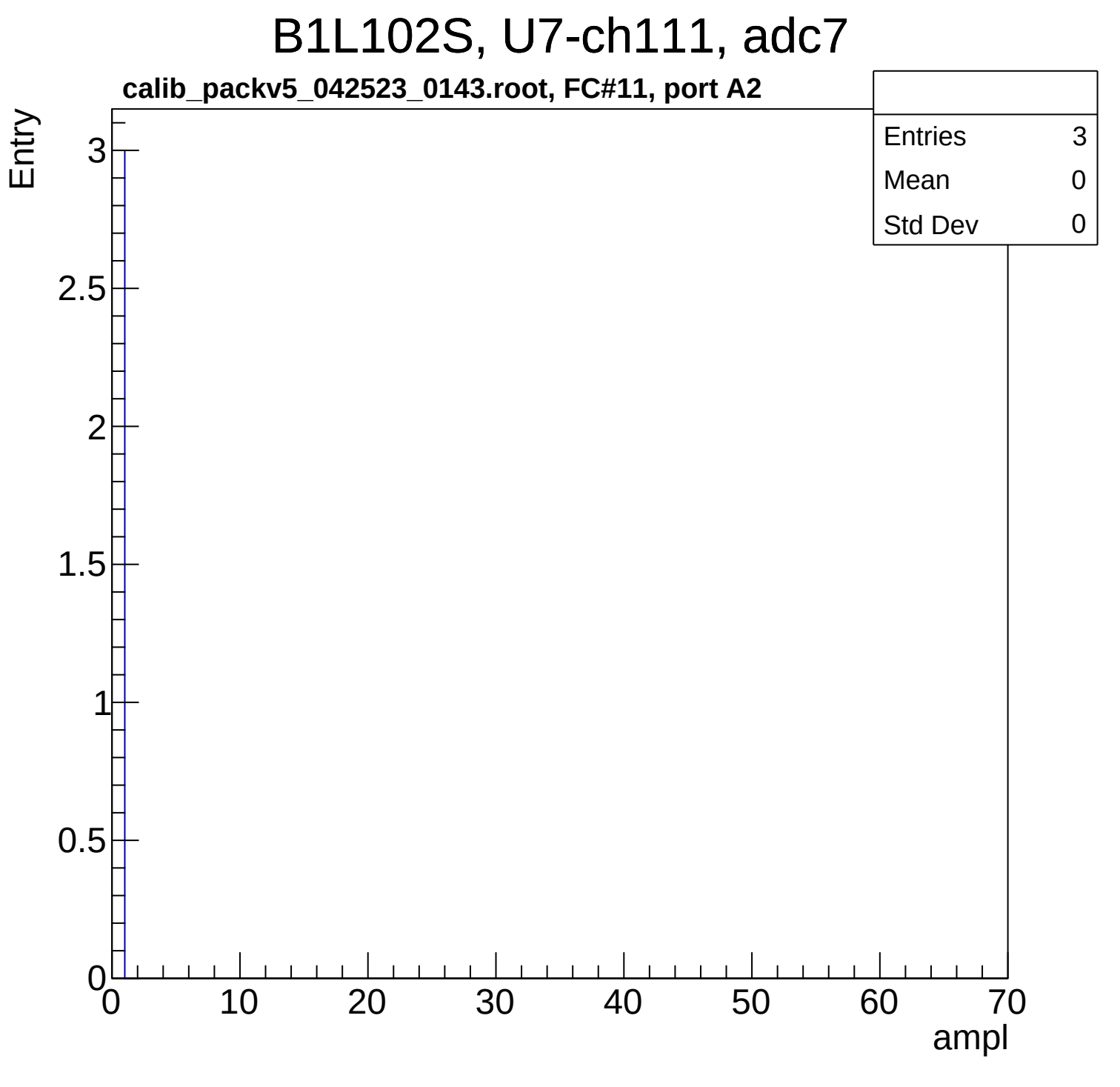
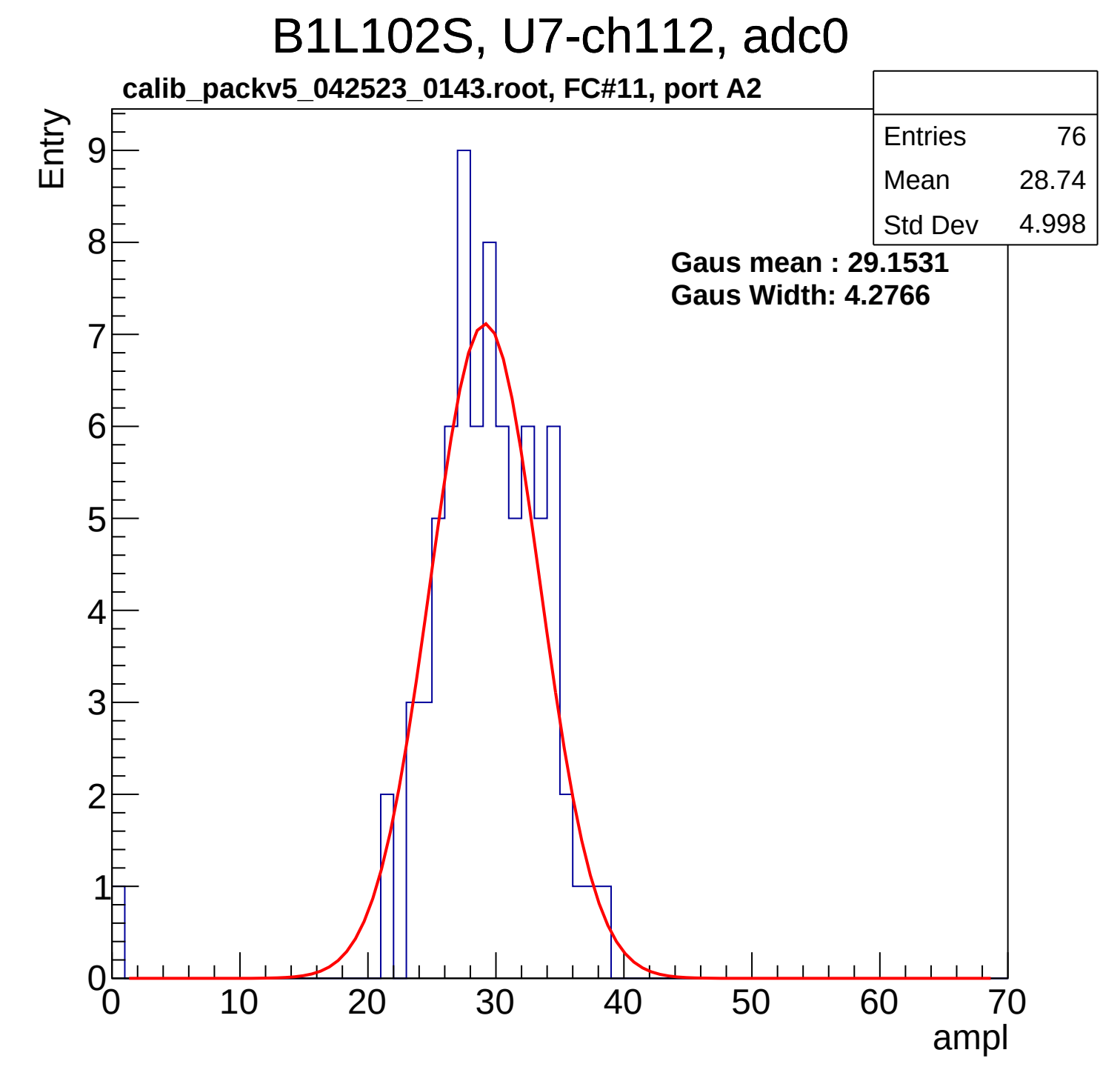
70
ampl


B1L102S, U7-ch111, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 3
Mean 0
Std Dev 0
Entry
3
2.5
2
1.5
1
0.5
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U7-ch112, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 76
Mean 28.74
Std Dev 4.998
Gaus mean : 29.1531
Gaus Width: 4.2766
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
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40
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60
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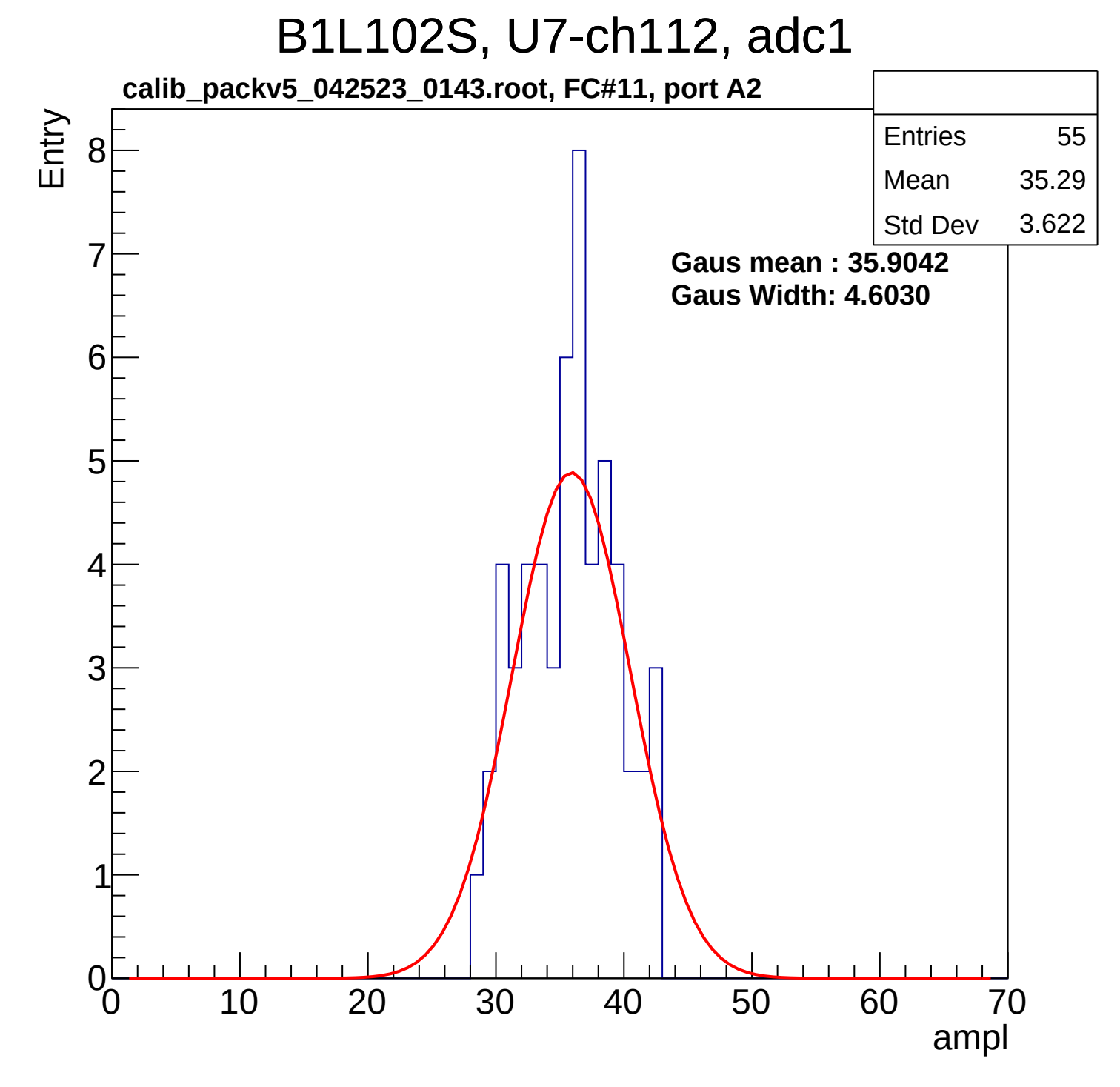
B1L102S, U7-ch112, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 55
Mean 35.29
Std Dev 3.622
Gaus mean : 35.9042
Gaus Width: 4.6030
Entry
ampl
0
1
2
3
4
5
6
7
8
0
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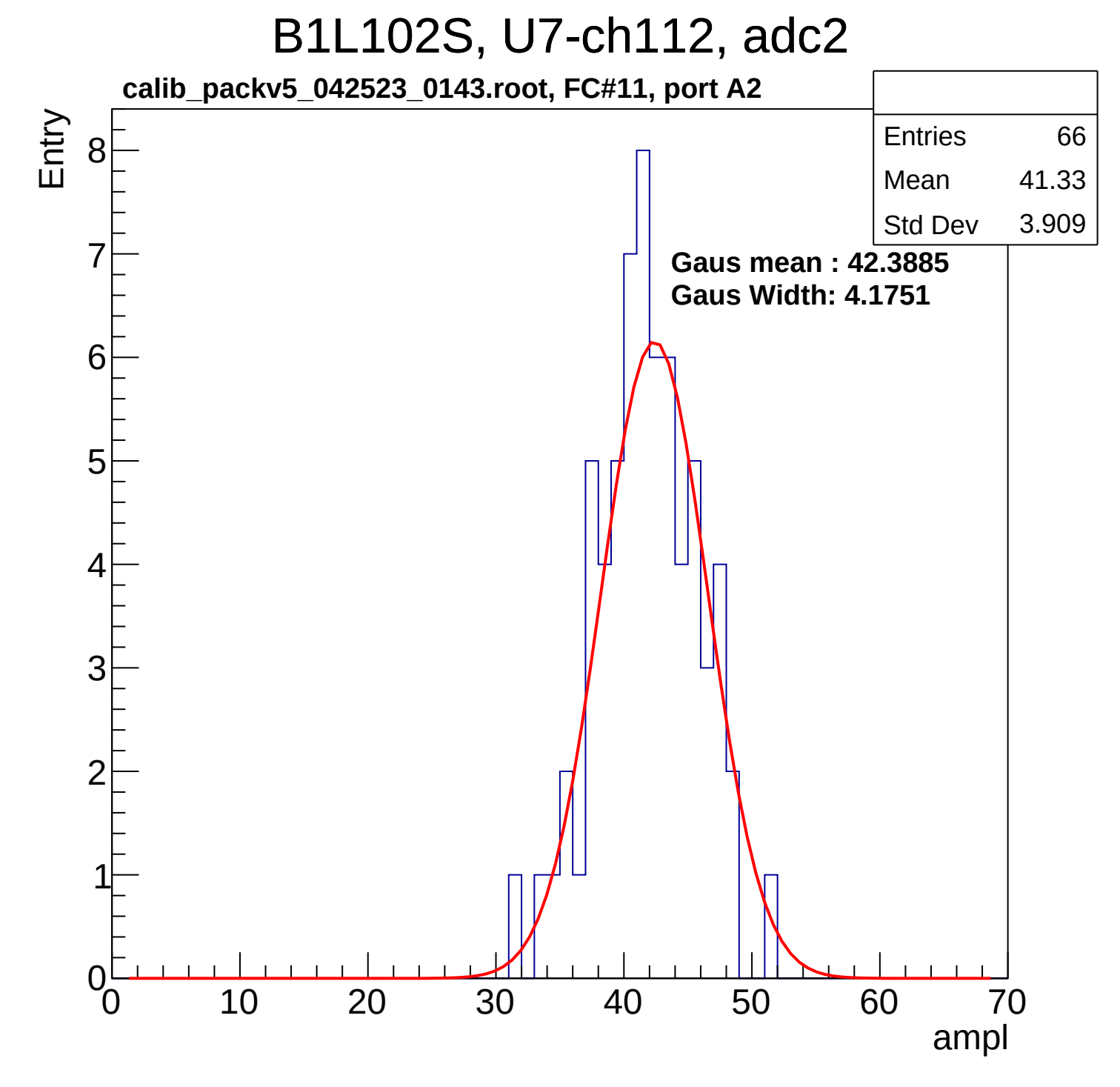
B1L102S, U7-ch112, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 66
Mean 41.33
Std Dev 3.909
Gaus mean : 42.3885
Gaus Width: 4.1751
Entry
ampl
0
1
2
3
4
5
6
7
8
0
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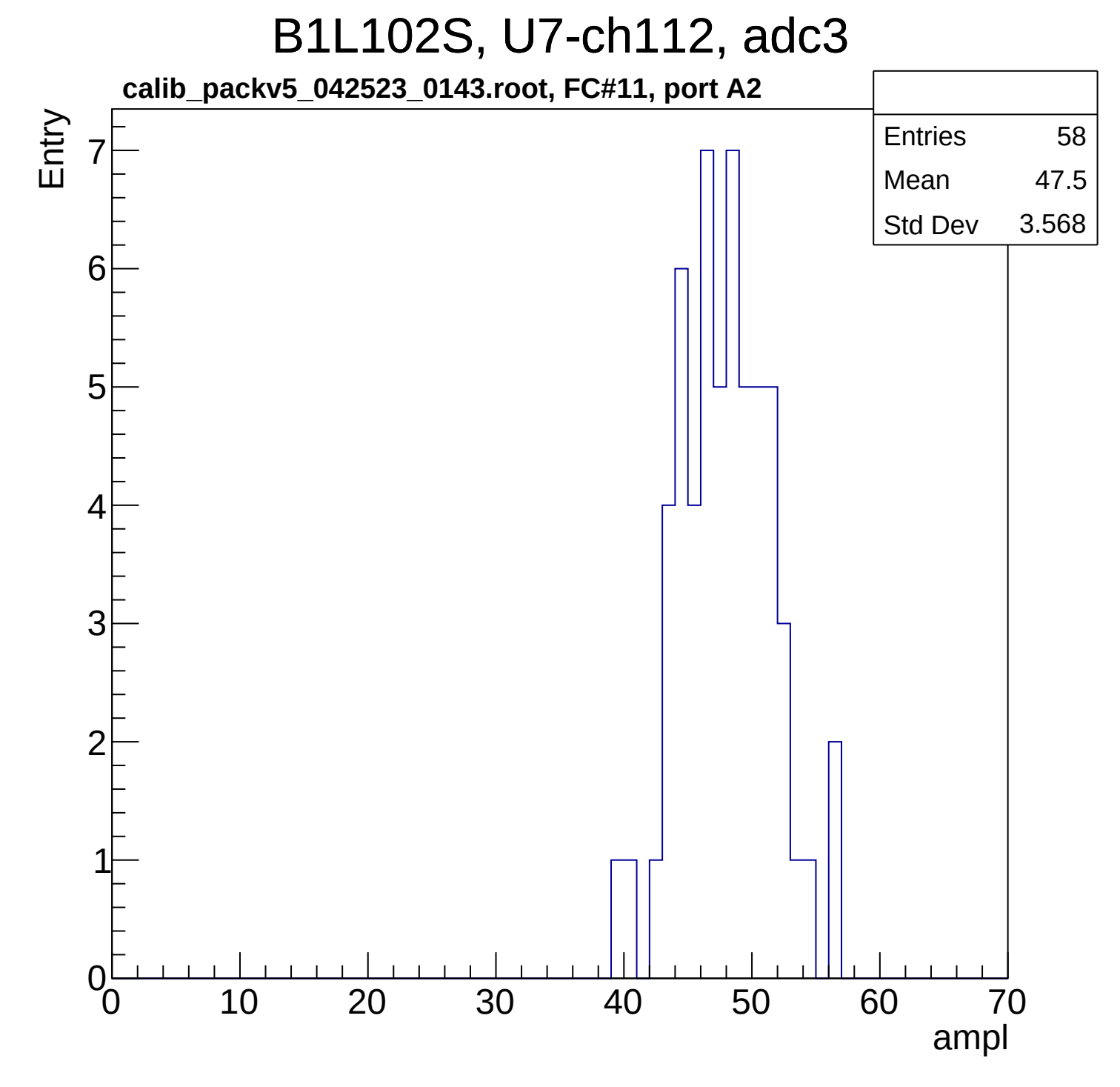
B1L102S, U7-ch112, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 58
Mean 47.5
Std Dev 3.568
Entry
ampl
0
1
2
3
4
5
6
7
0
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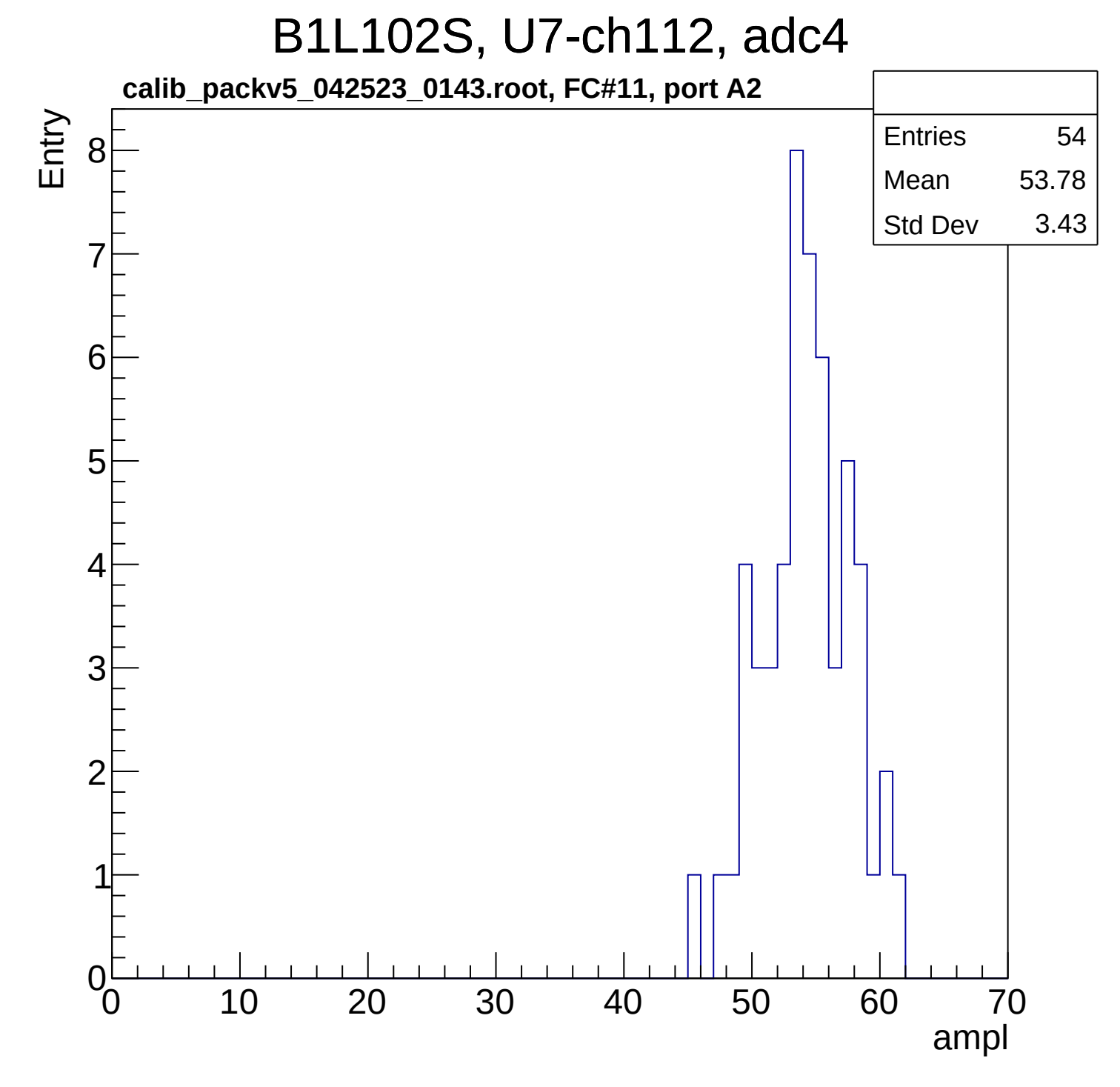
B1L102S, U7-ch112, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 54
Mean 53.78
Std Dev 3.43
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
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40
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60
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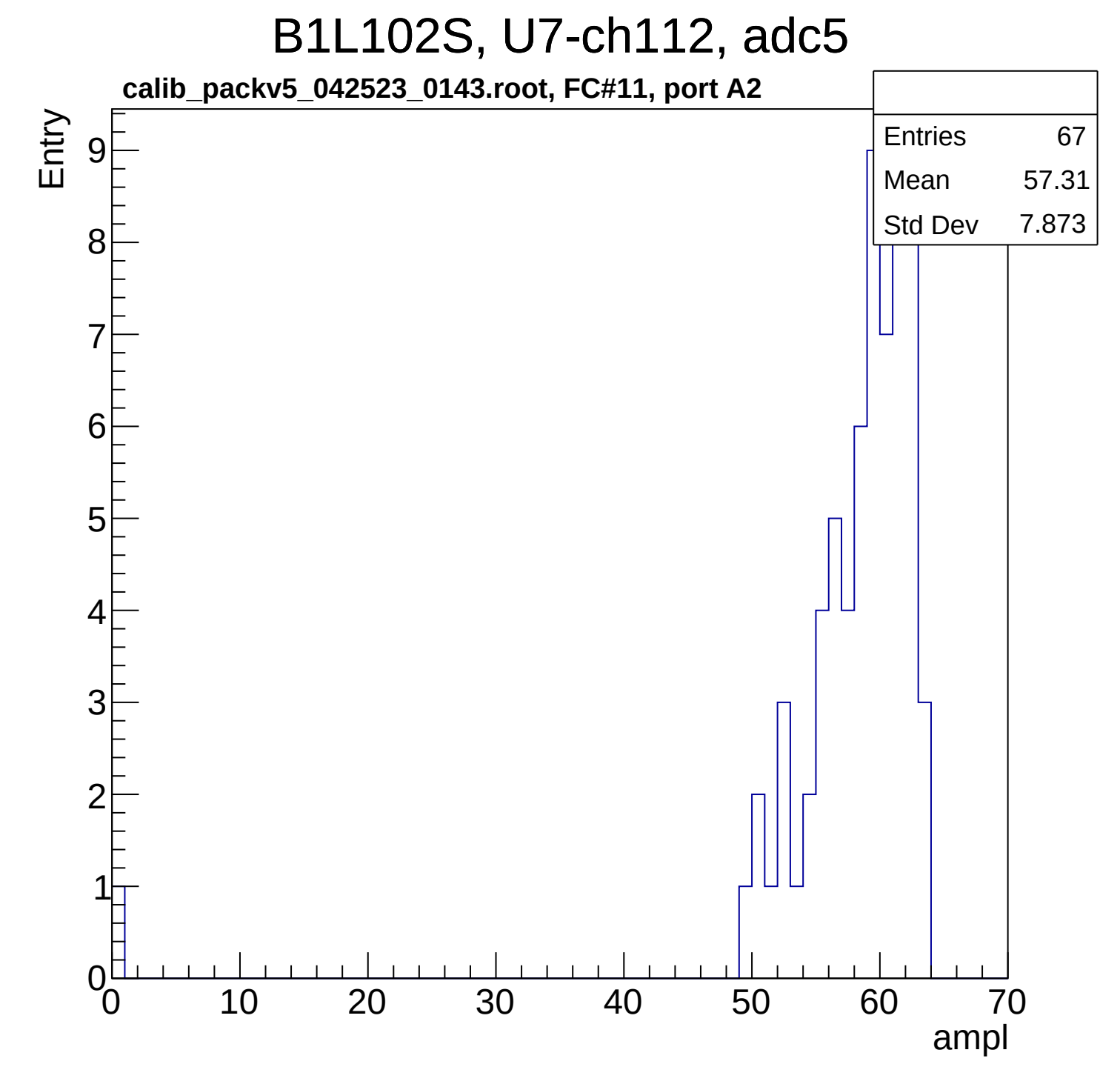
B1L102S, U7-ch112, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 67
Mean 57.31
Std Dev 7.873
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
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60
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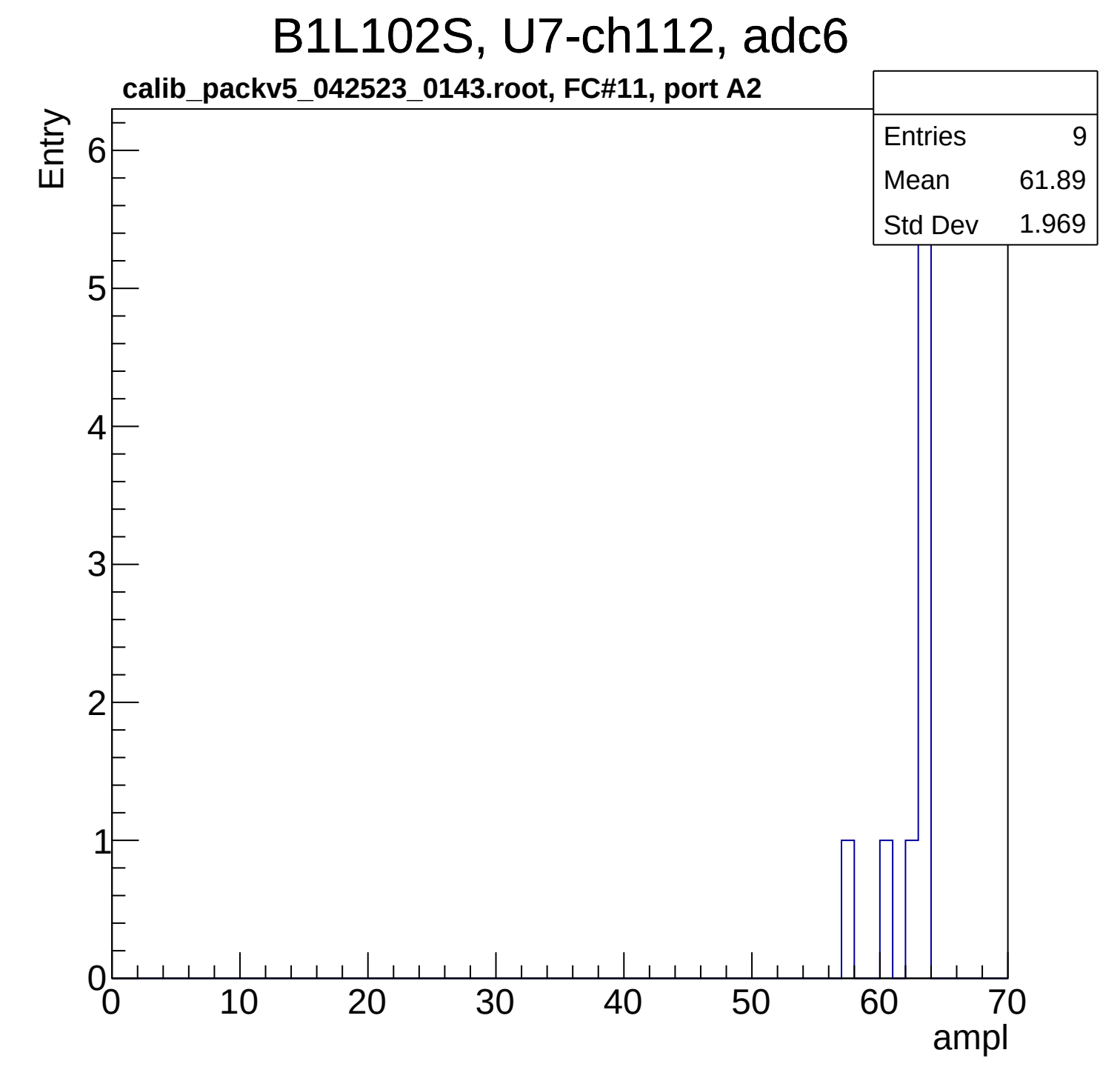
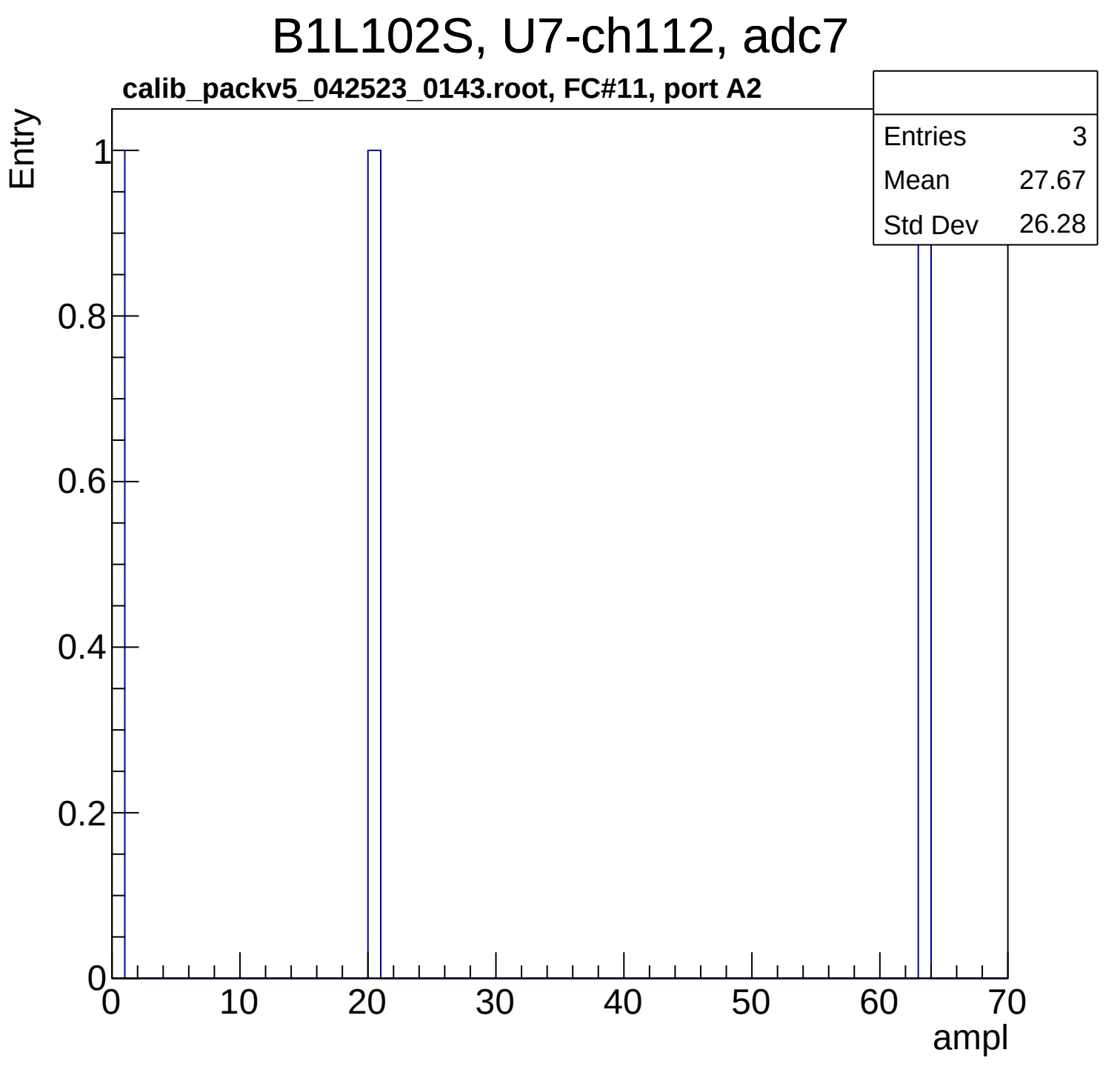
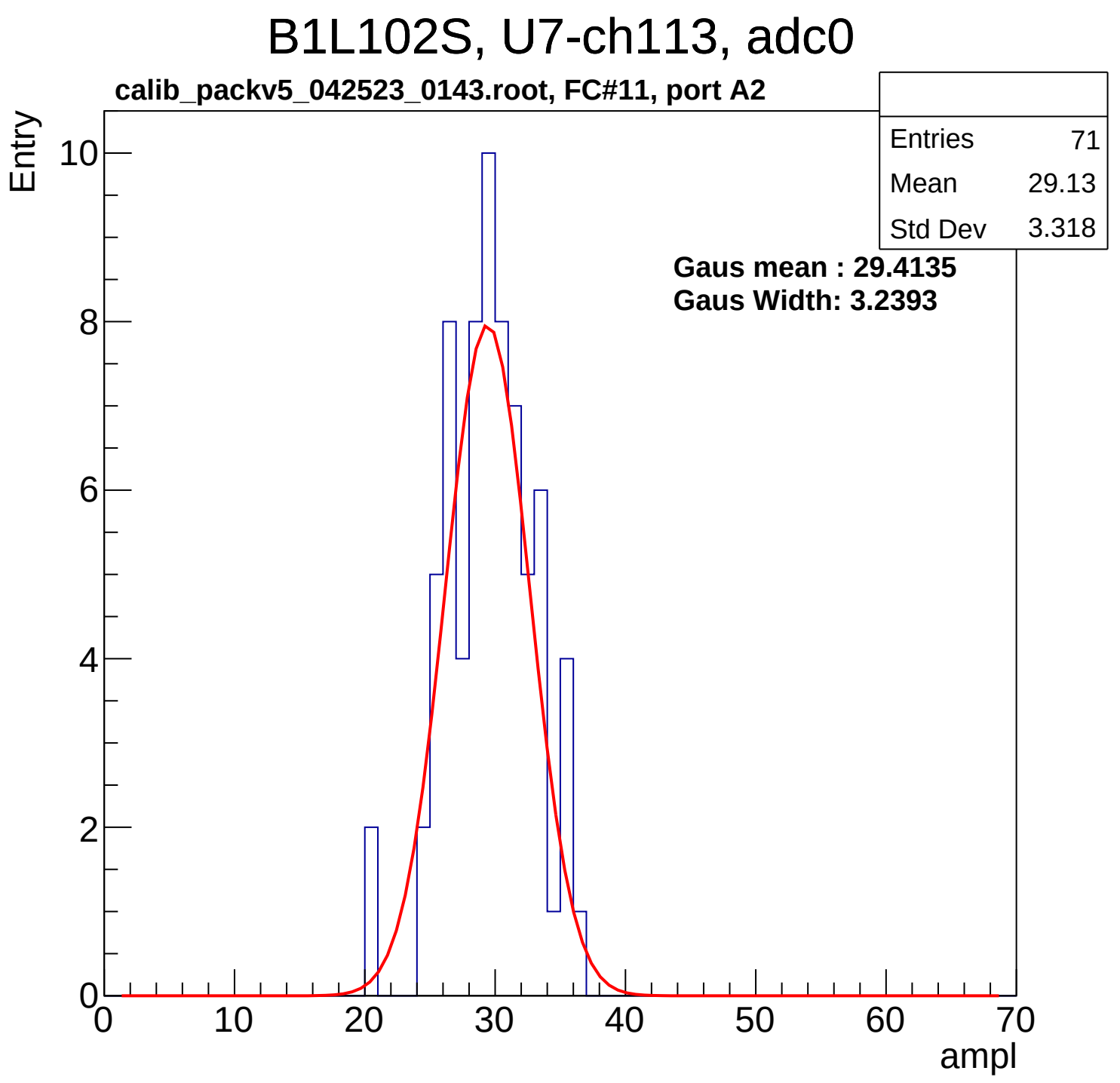
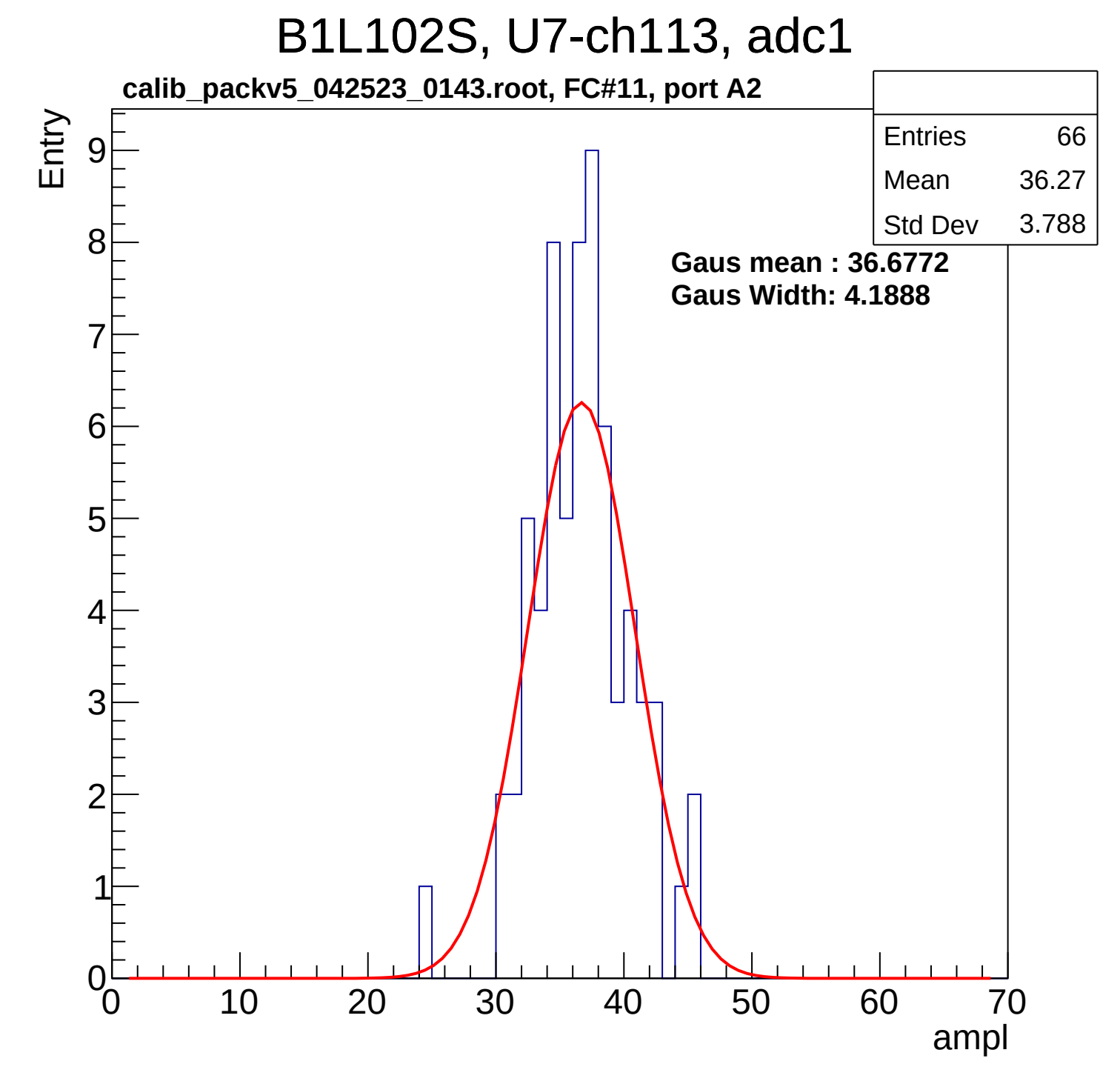

B1L102S, U7-ch112, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 9
Mean 61.89
Std Dev 1.969
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L102S, U7-ch112, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 3
Mean 27.67
Std Dev 26.28
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70


B1L102S, U7-ch113, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 71
Mean 29.13
Std Dev 3.318
Gaus mean : 29.4135
Gaus Width: 3.2393
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L102S, U7-ch113, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 66
Mean 36.27
Std Dev 3.788
Gaus mean : 36.6772
Gaus Width: 4.1888
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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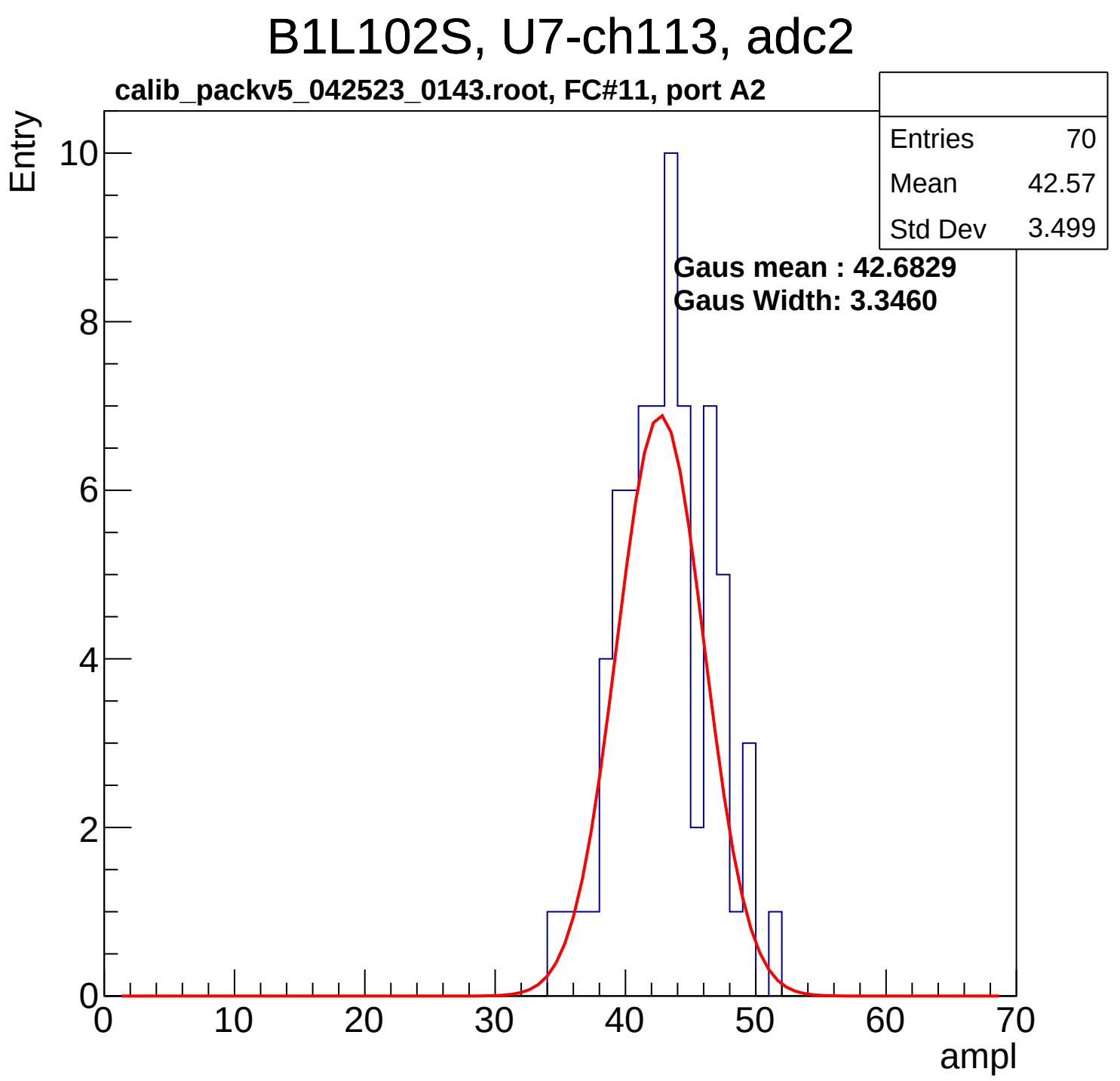
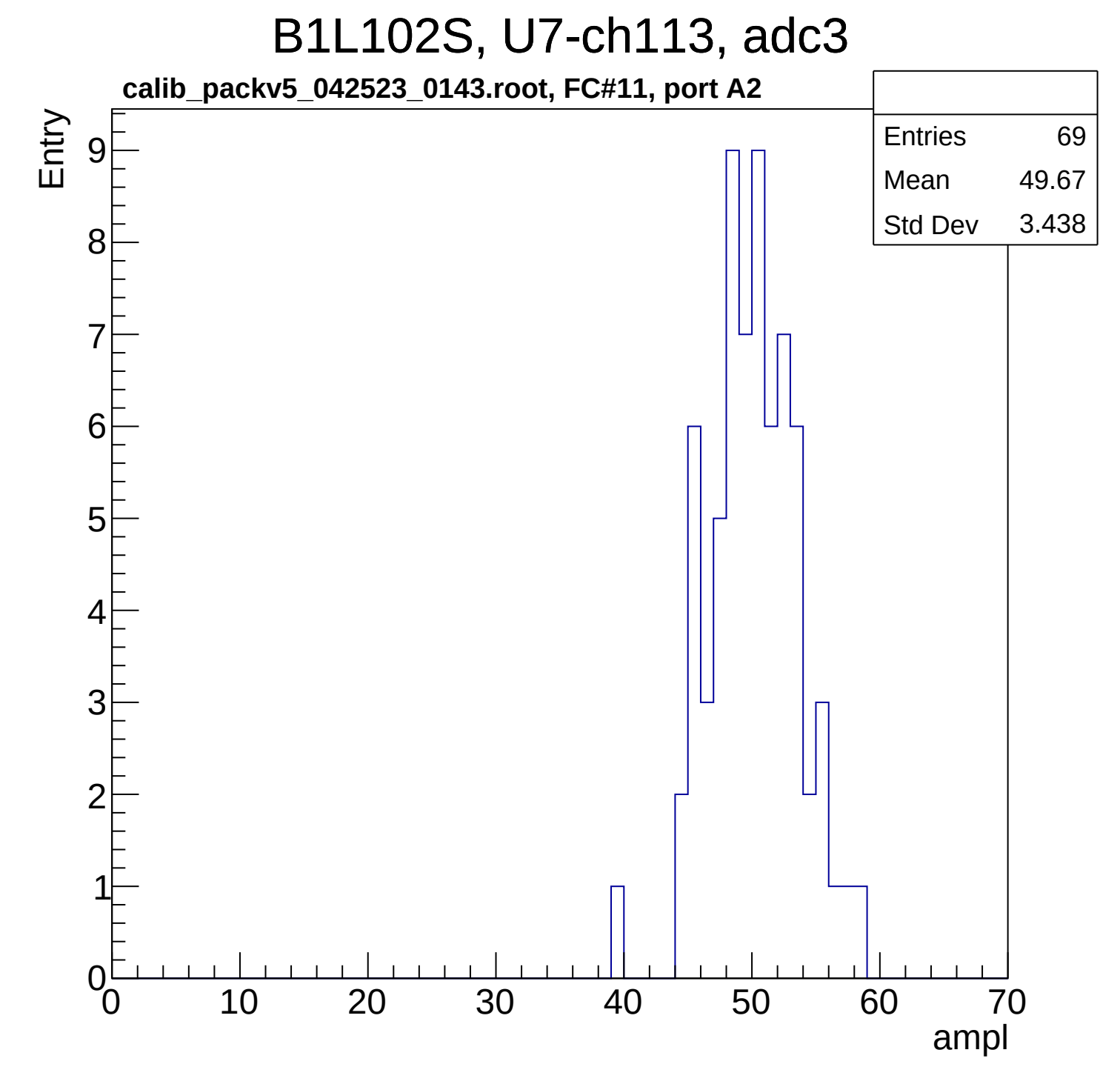

B1L102S, U7-ch113, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 70
Mean 42.57
Std Dev 3.499
Gaus mean : 42.6829
Gaus Width: 3.3460
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L102S, U7-ch113, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 69
Mean 49.67
Std Dev 3.438
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
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40
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60
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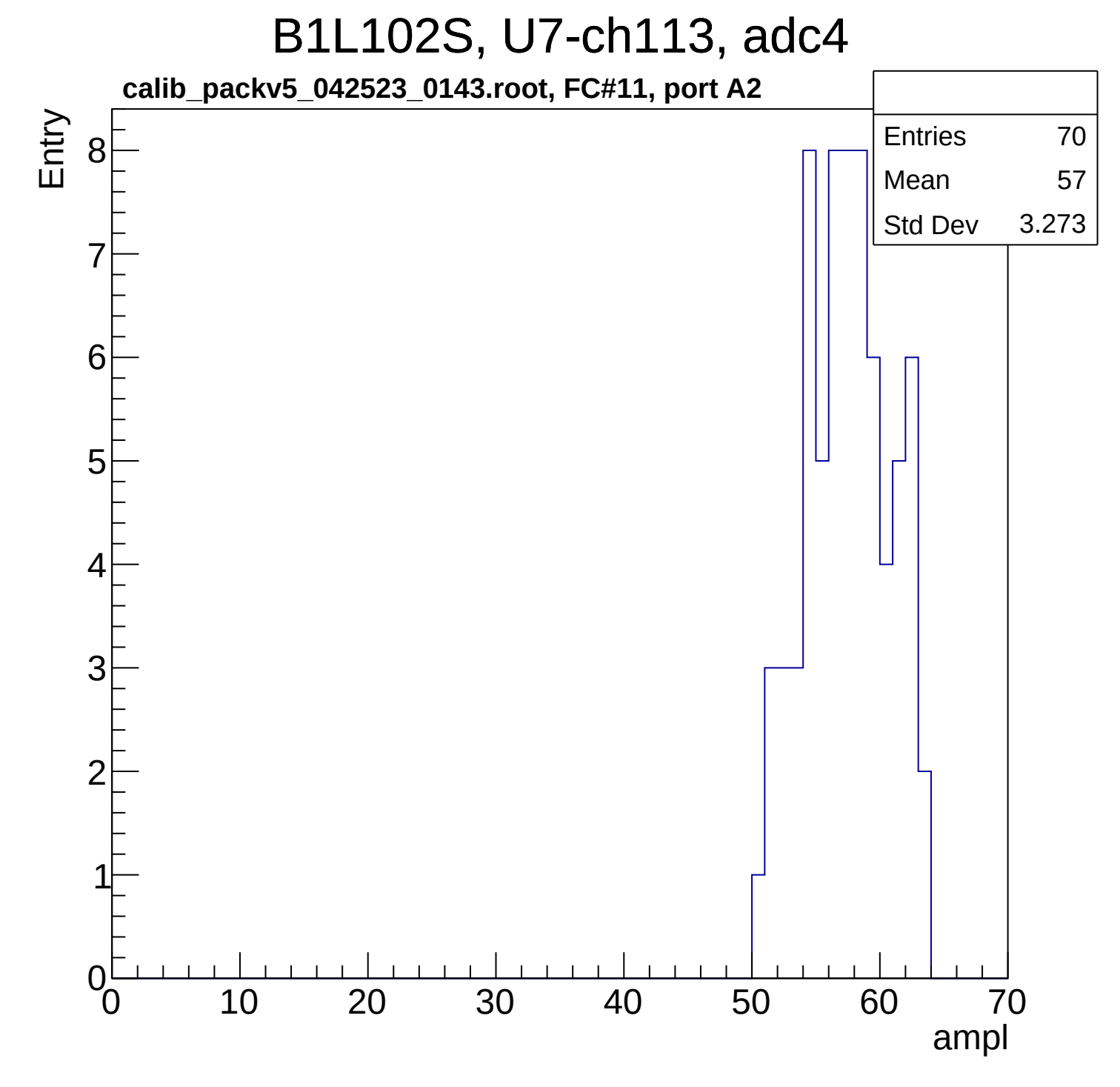
B1L102S, U7-ch113, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 70
Mean 57
Std Dev 3.273
Entry
ampl
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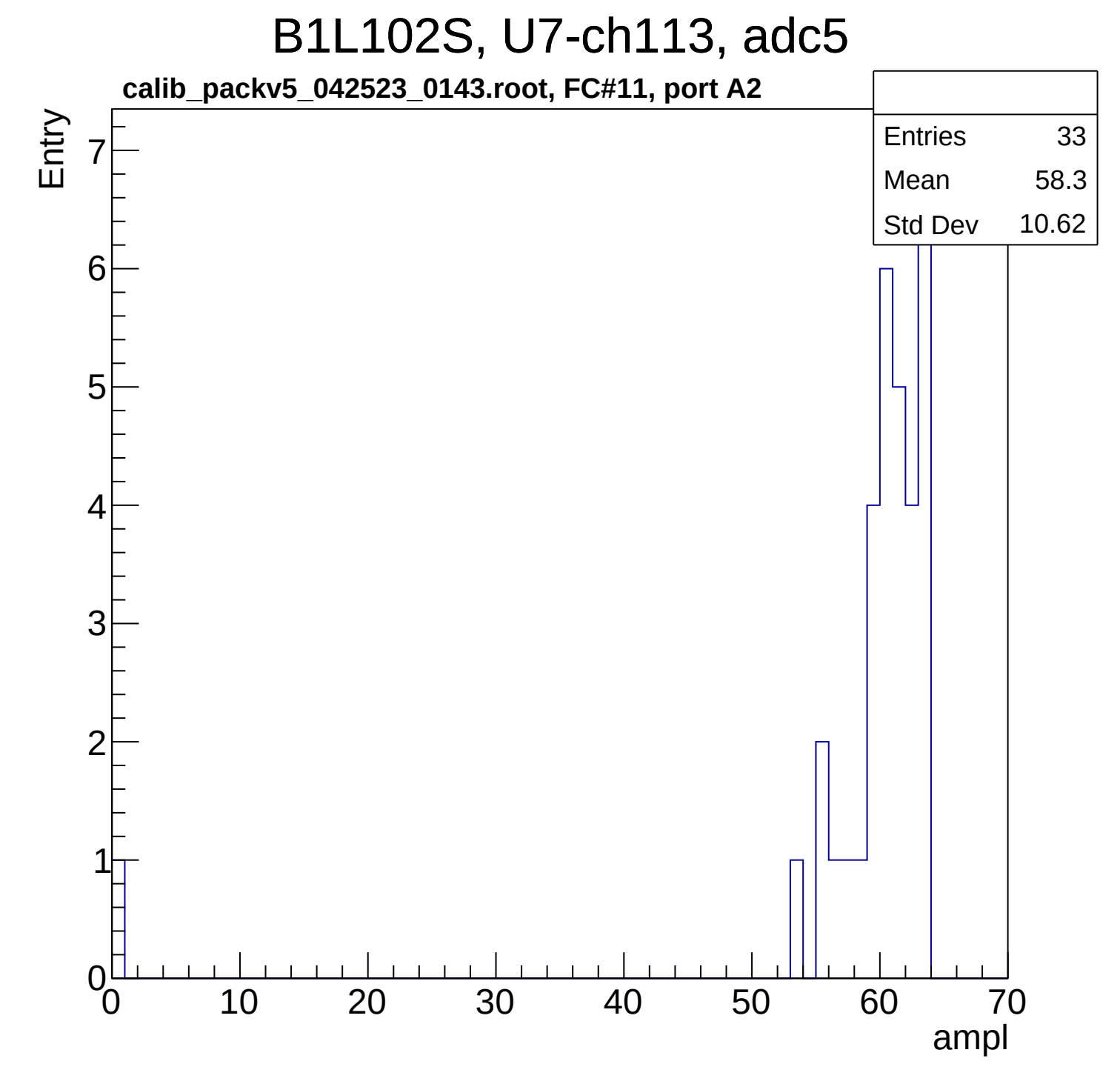
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L102S, U7-ch113, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 33
Mean 58.3
Std Dev 10.62
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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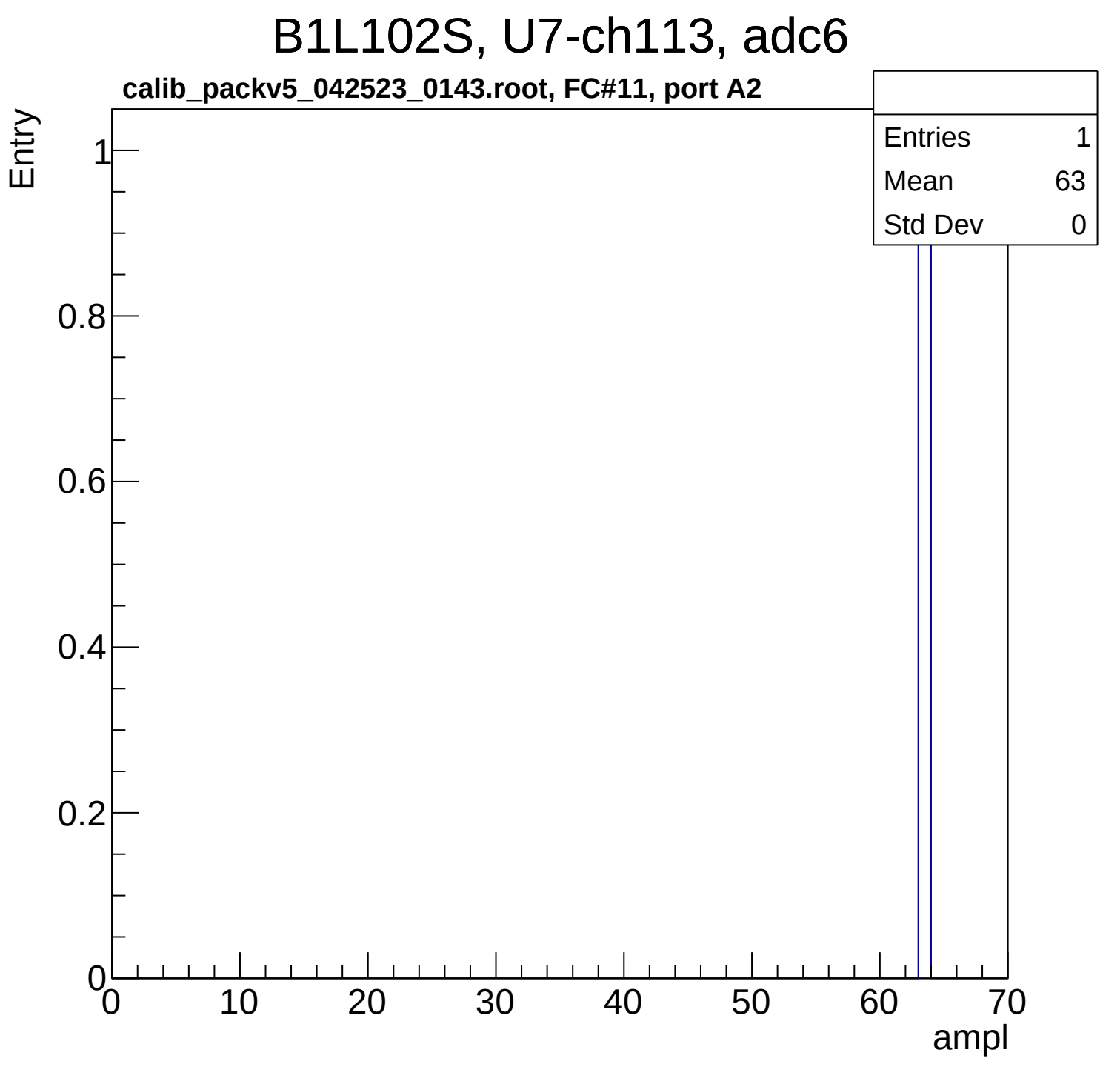
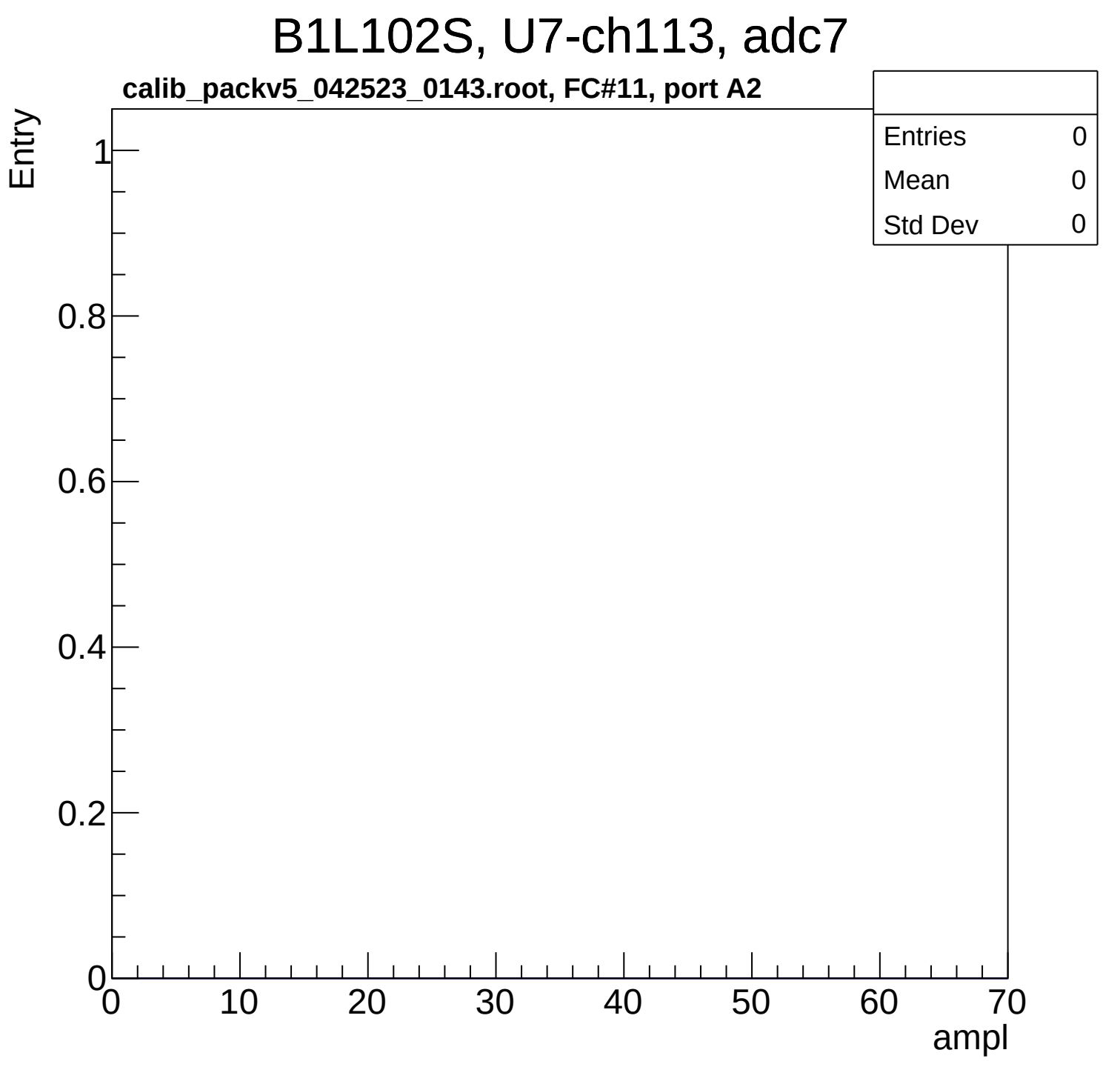
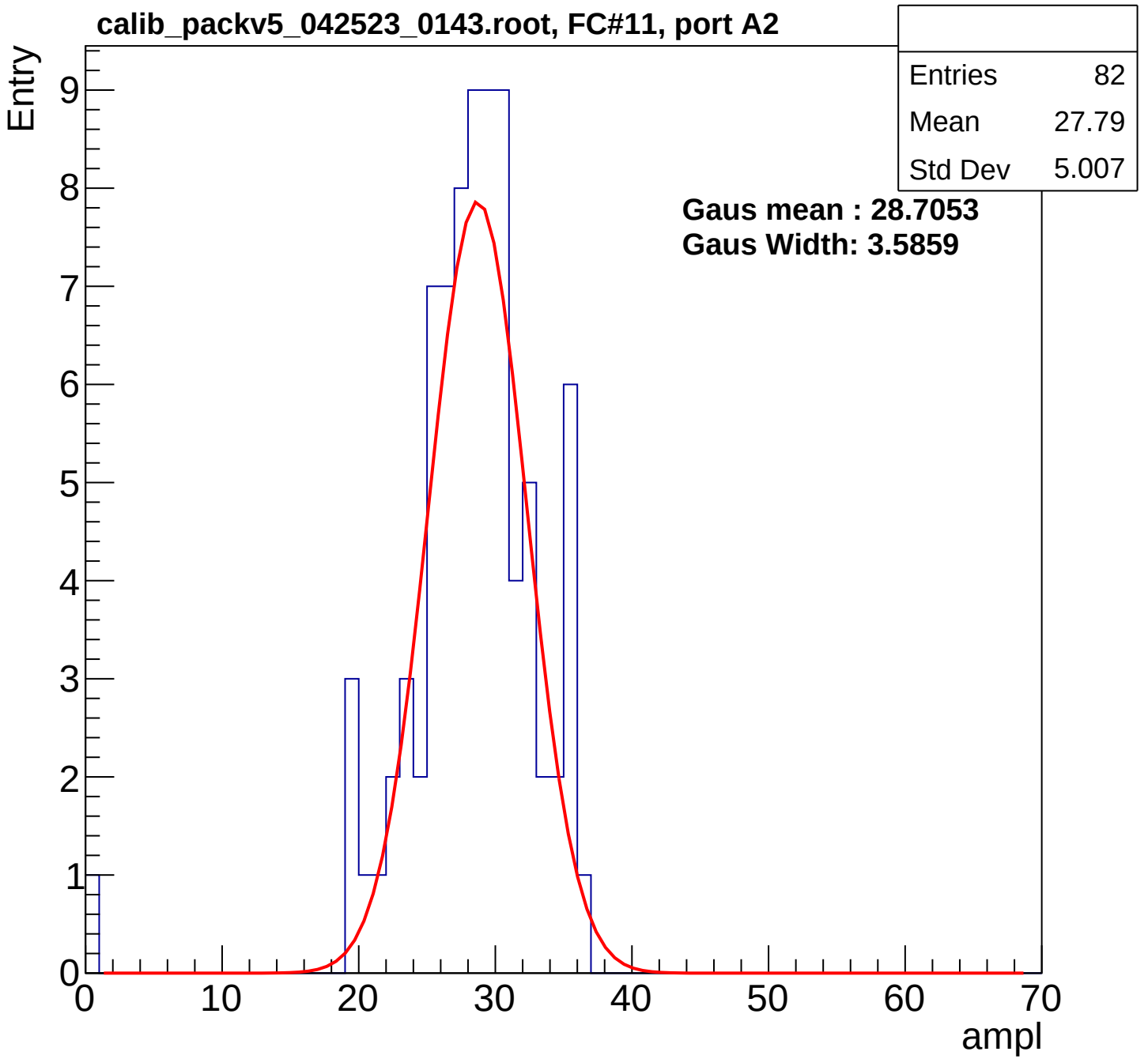

B1L102S, U7-ch113, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 1
Mean 63
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U7-ch113, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U7-ch114, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 82
Mean 27.79
Std Dev 5.007
Gaus mean : 28.7053
Gaus Width: 3.5859
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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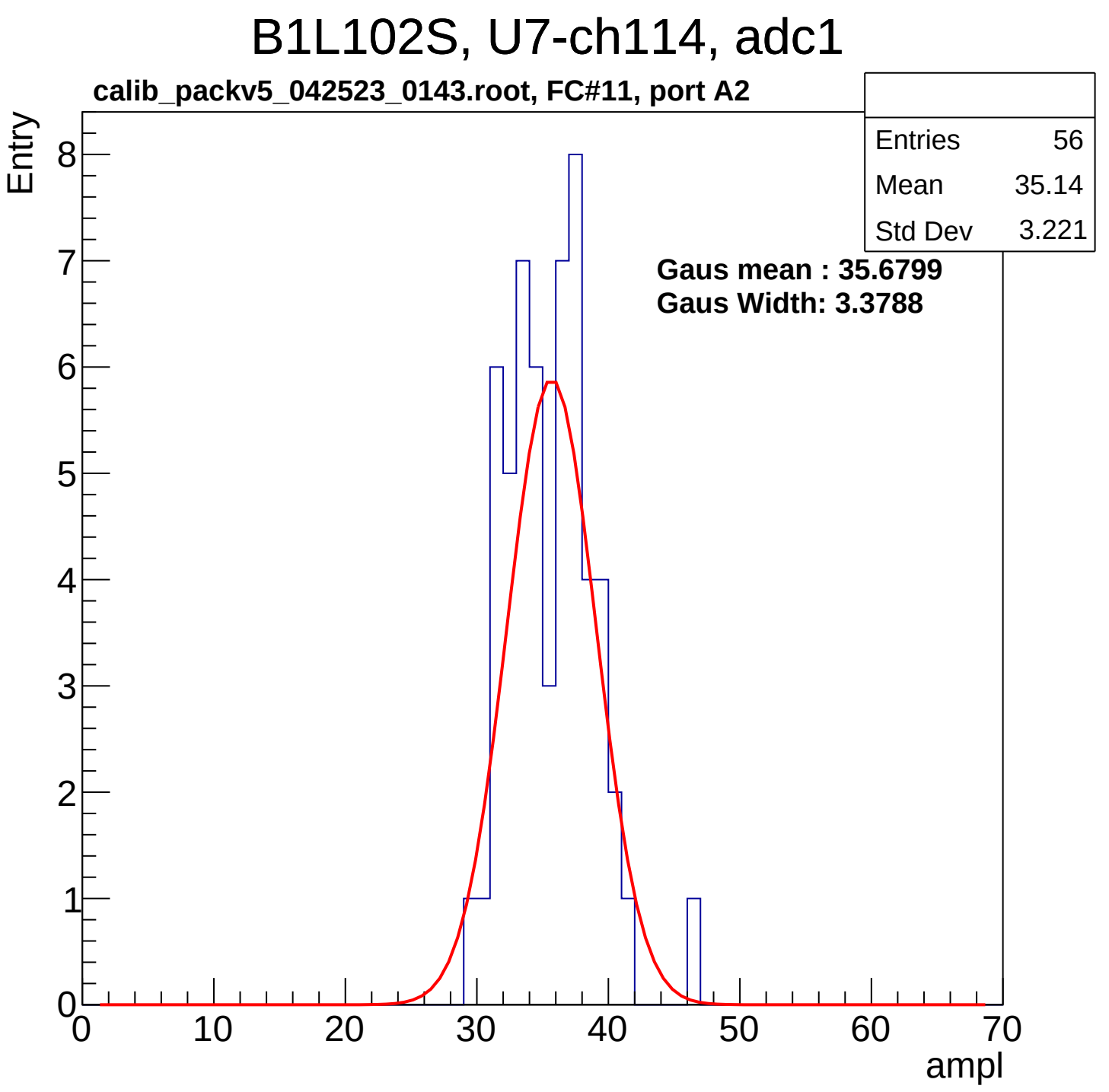
60
70


B1L102S, U7-ch114, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 56
Mean 35.14
Std Dev 3.221
Gaus mean : 35.6799
Gaus Width: 3.3788
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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40
50
60
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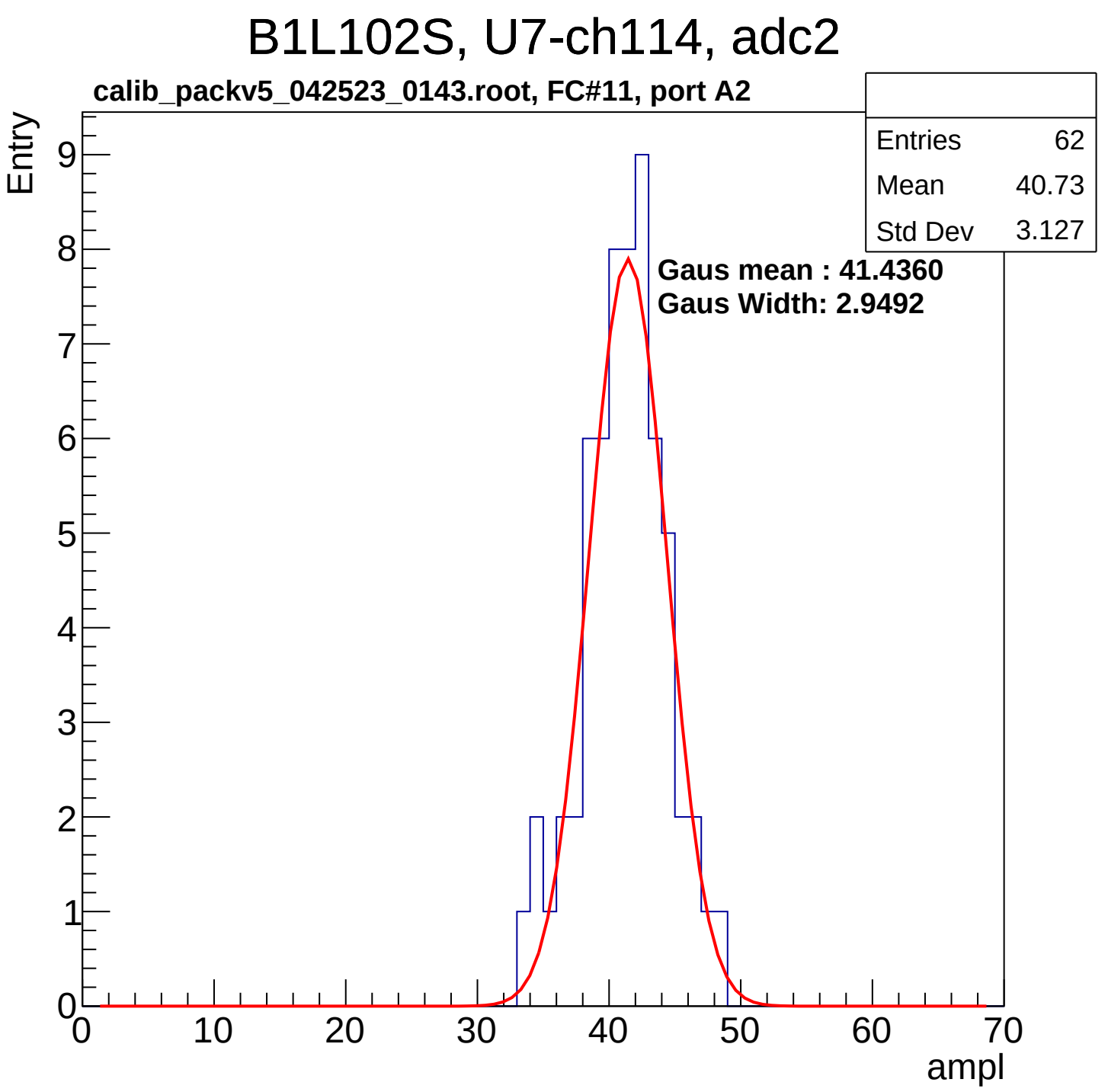
B1L102S, U7-ch114, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 62
Mean 40.73
Std Dev 3.127
Gaus mean : 41.4360
Gaus Width: 2.9492
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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40
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60
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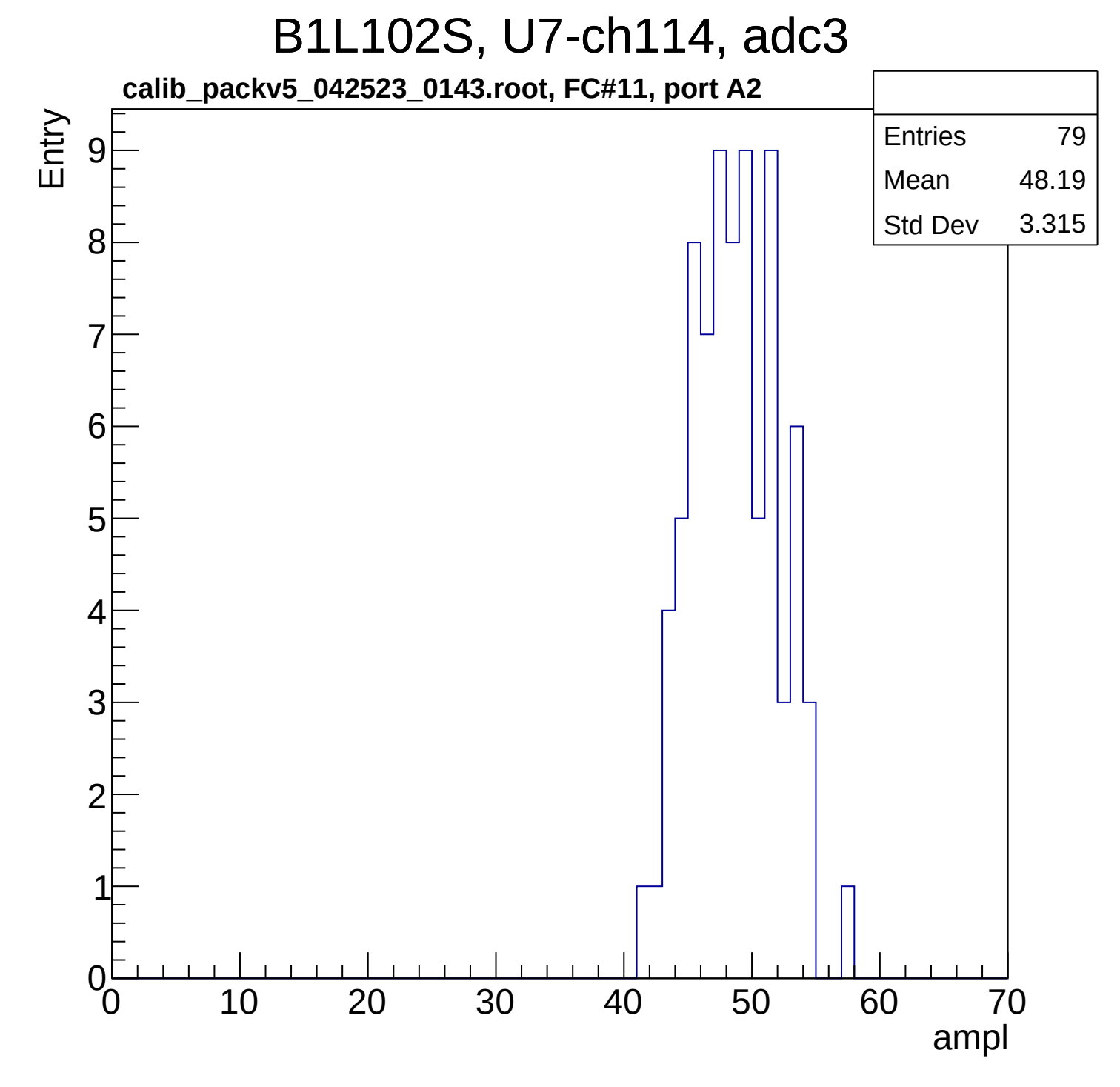
B1L102S, U7-ch114, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 79
Mean 48.19
Std Dev 3.315
Entry
ampl
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2
3
4
5
6
7
8
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0
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20
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60
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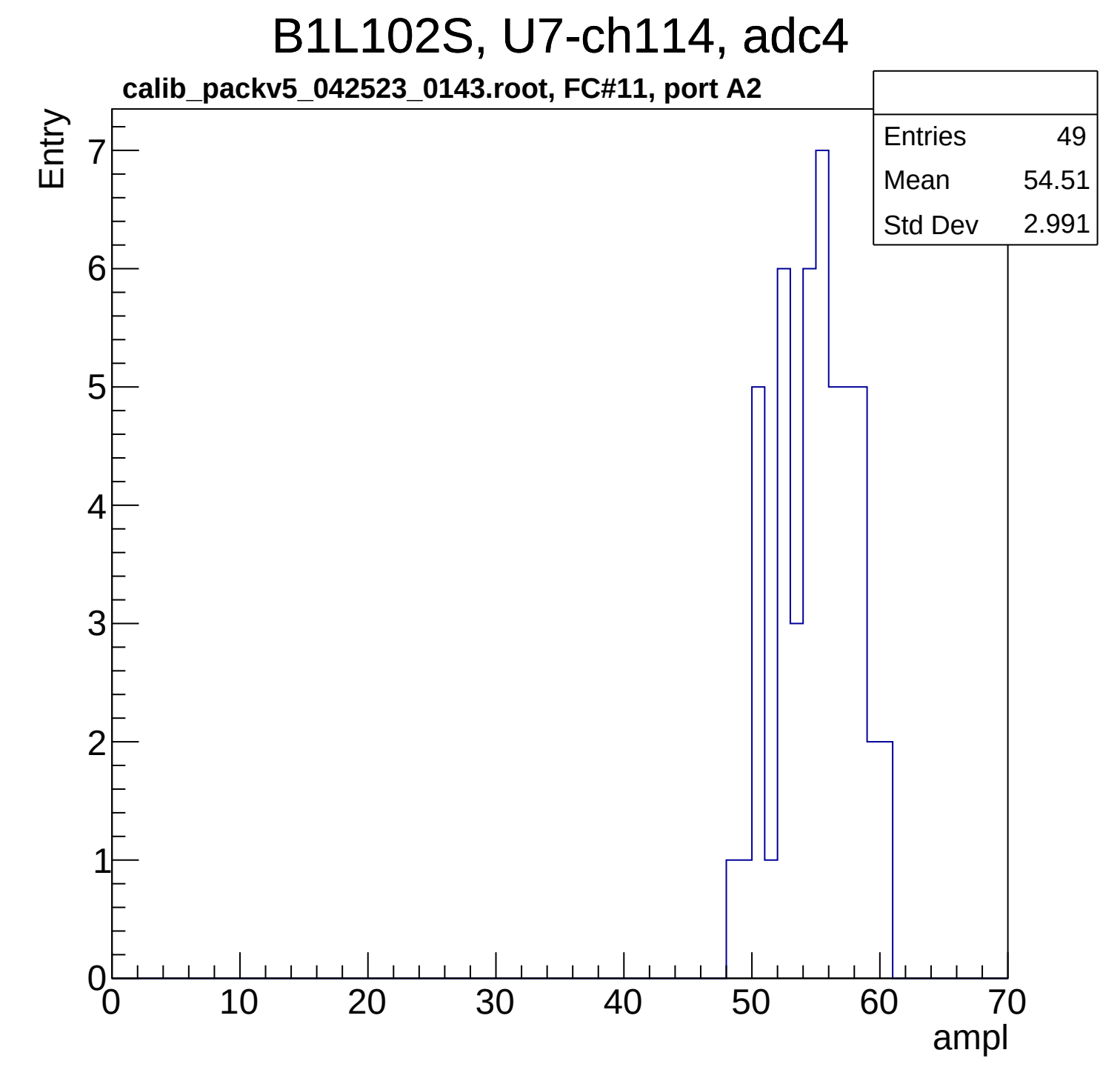
B1L102S, U7-ch114, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 49
Mean 54.51
Std Dev 2.991
Entry
ampl
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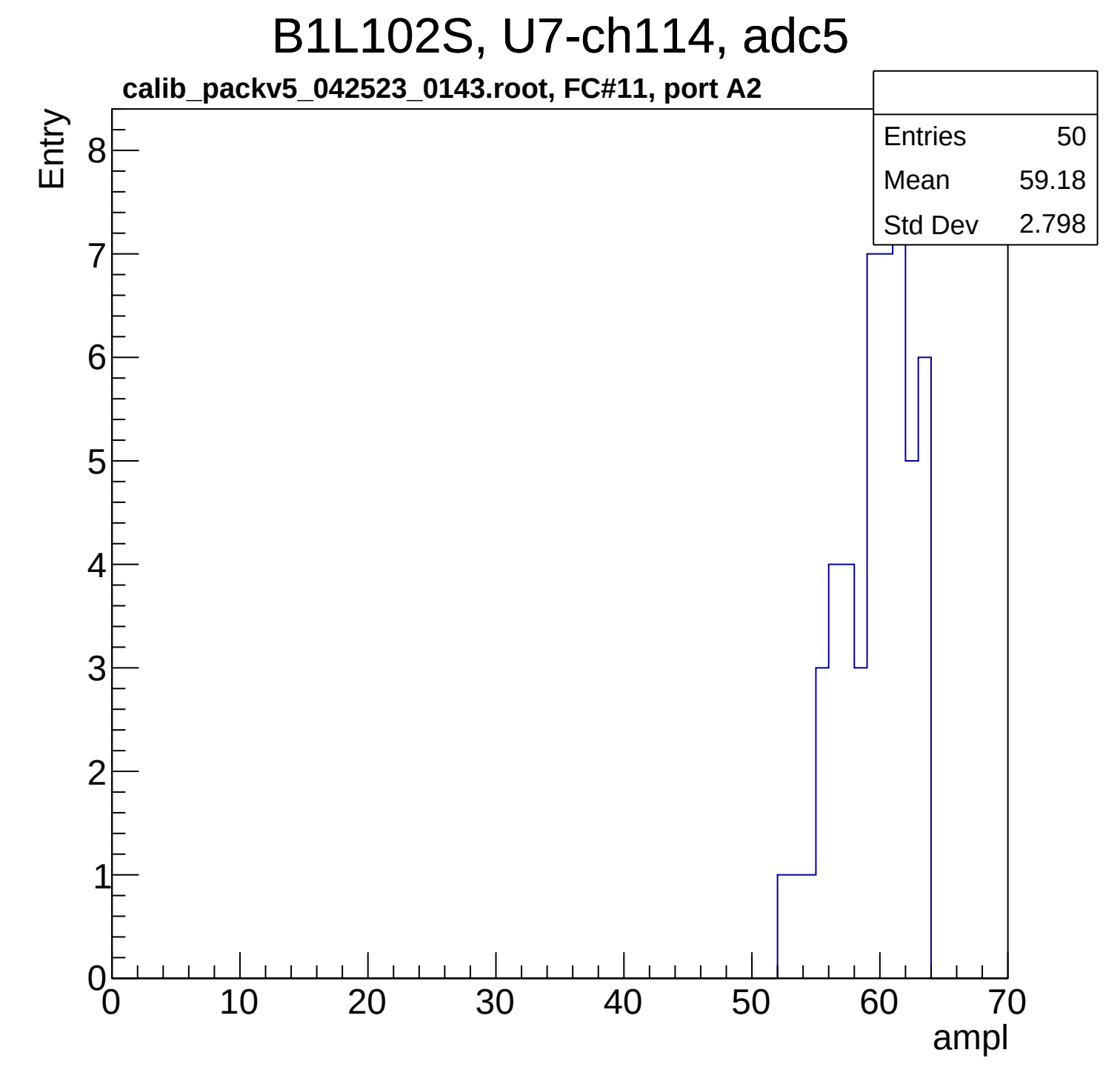
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L102S, U7-ch114, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 50
Mean 59.18
Std Dev 2.798
Entry
ampl
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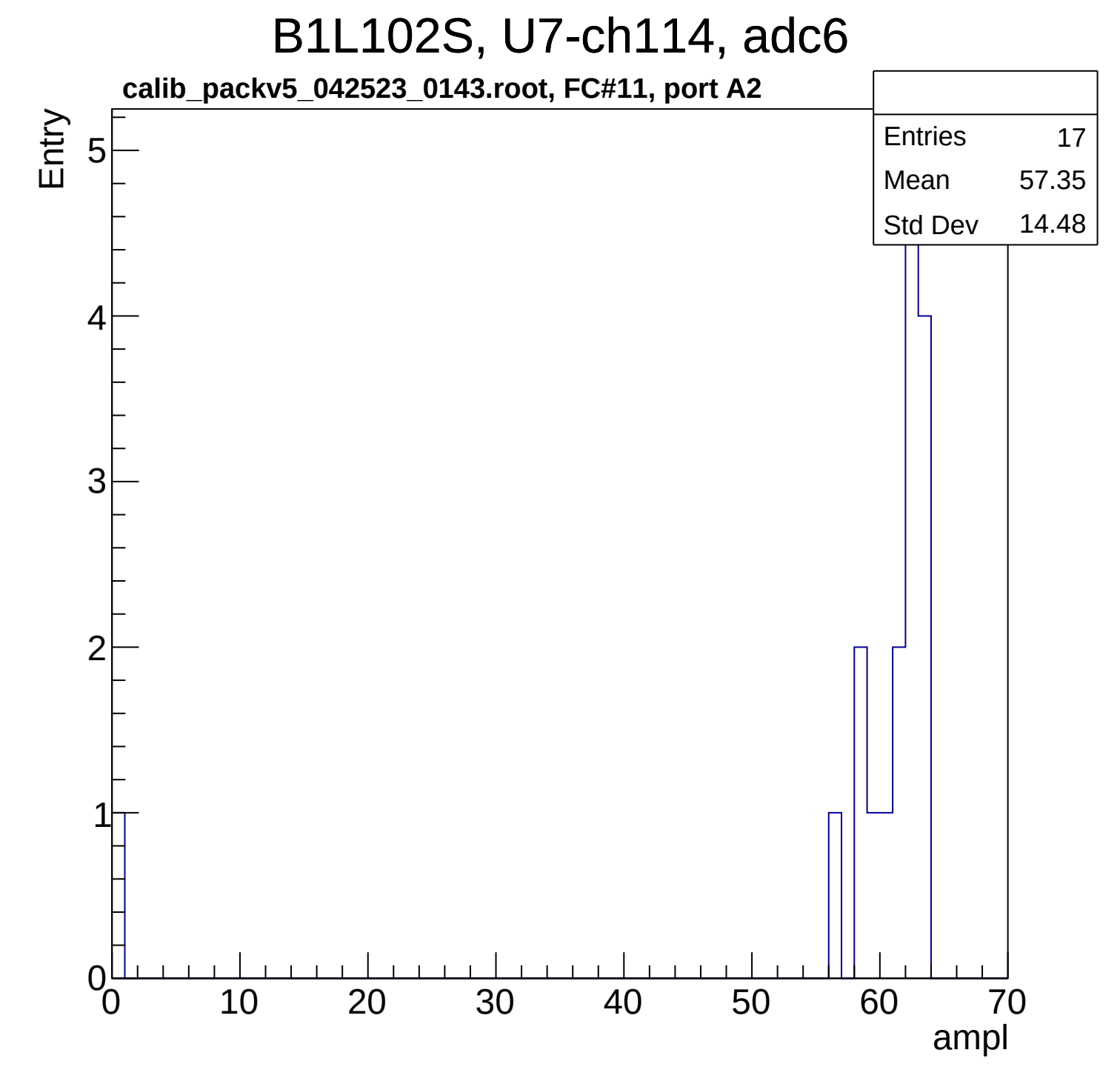
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L102S, U7-ch114, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 17
Mean 57.35
Std Dev 14.48
Entry
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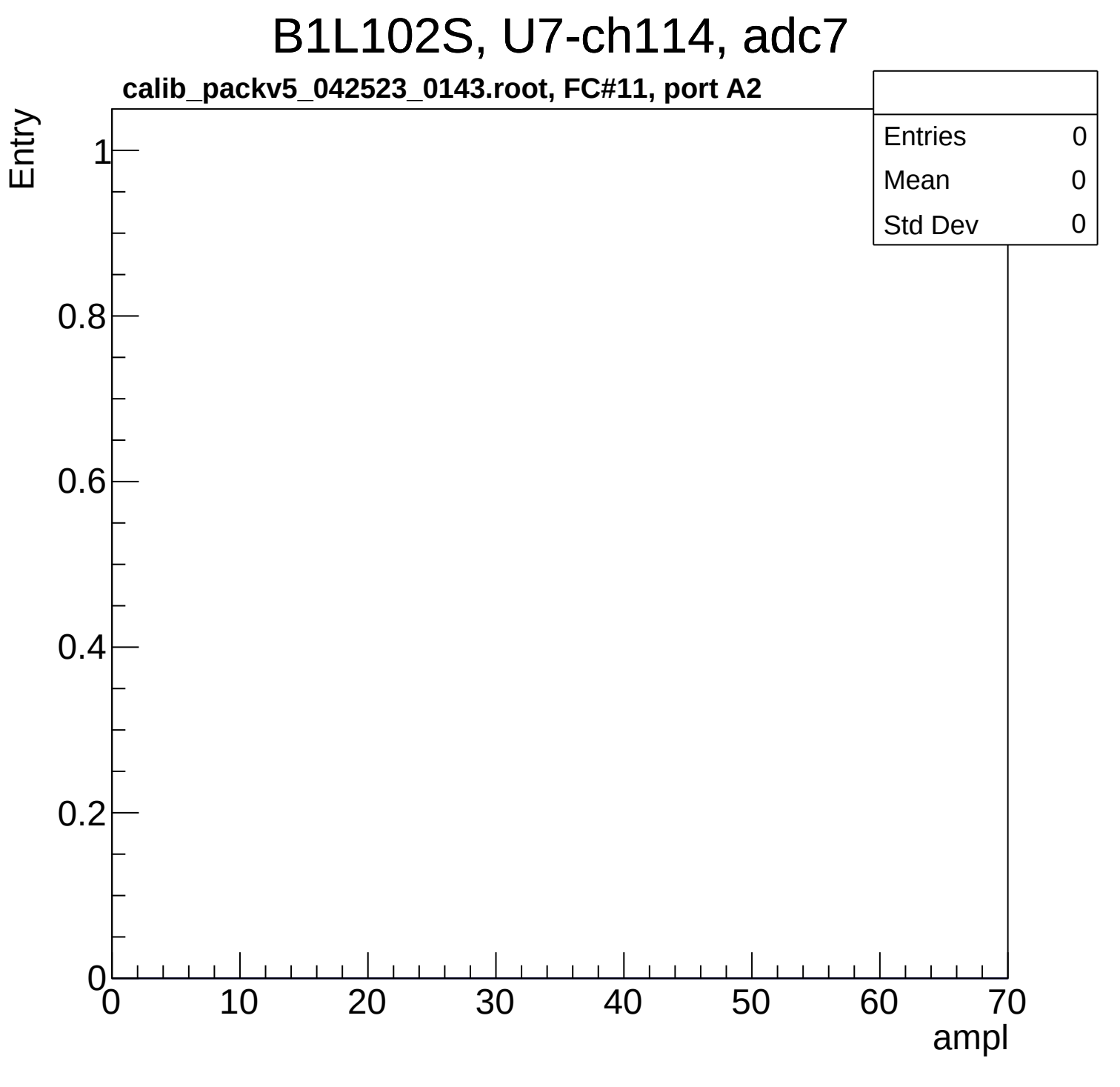
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L102S, U7-ch114, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 0
Mean 0
Std Dev 0
Entry
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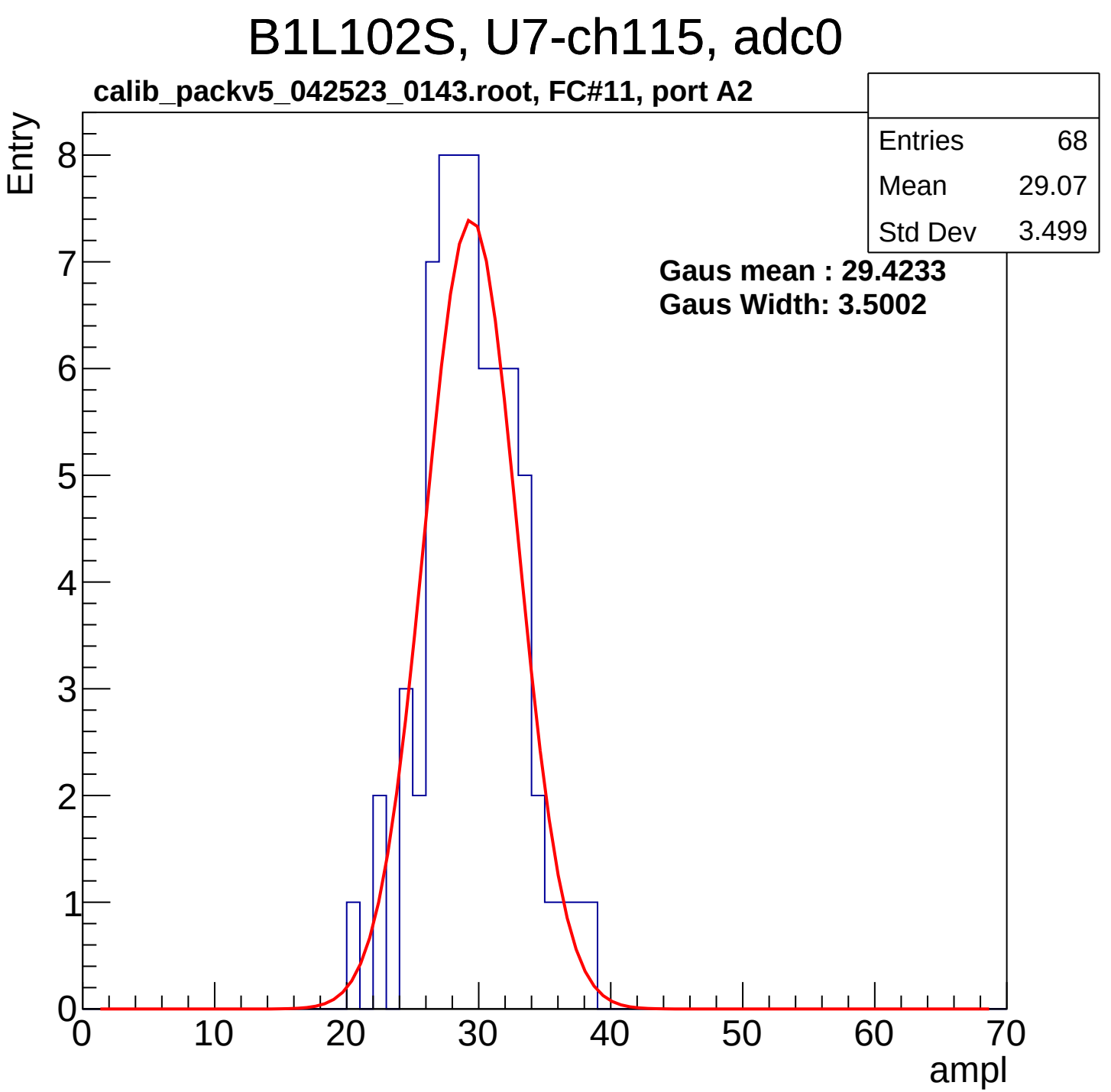
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U7-ch115, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 68
Mean 29.07
Std Dev 3.499
Gaus mean : 29.4233
Gaus Width: 3.5002
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
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60
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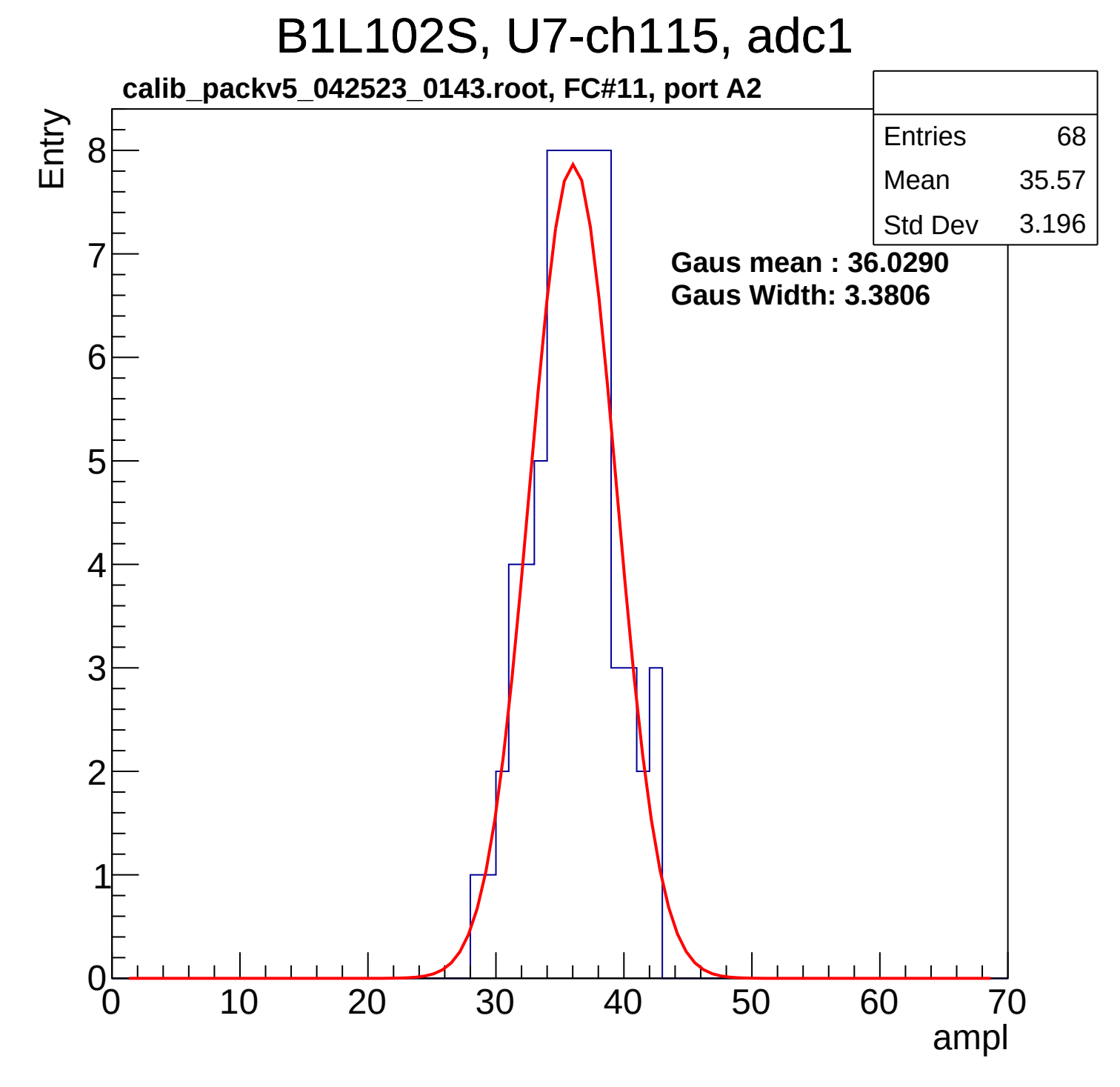
B1L102S, U7-ch115, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 68
Mean 35.57
Std Dev 3.196
Gaus mean : 36.0290
Gaus Width: 3.3806
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
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40
50
60
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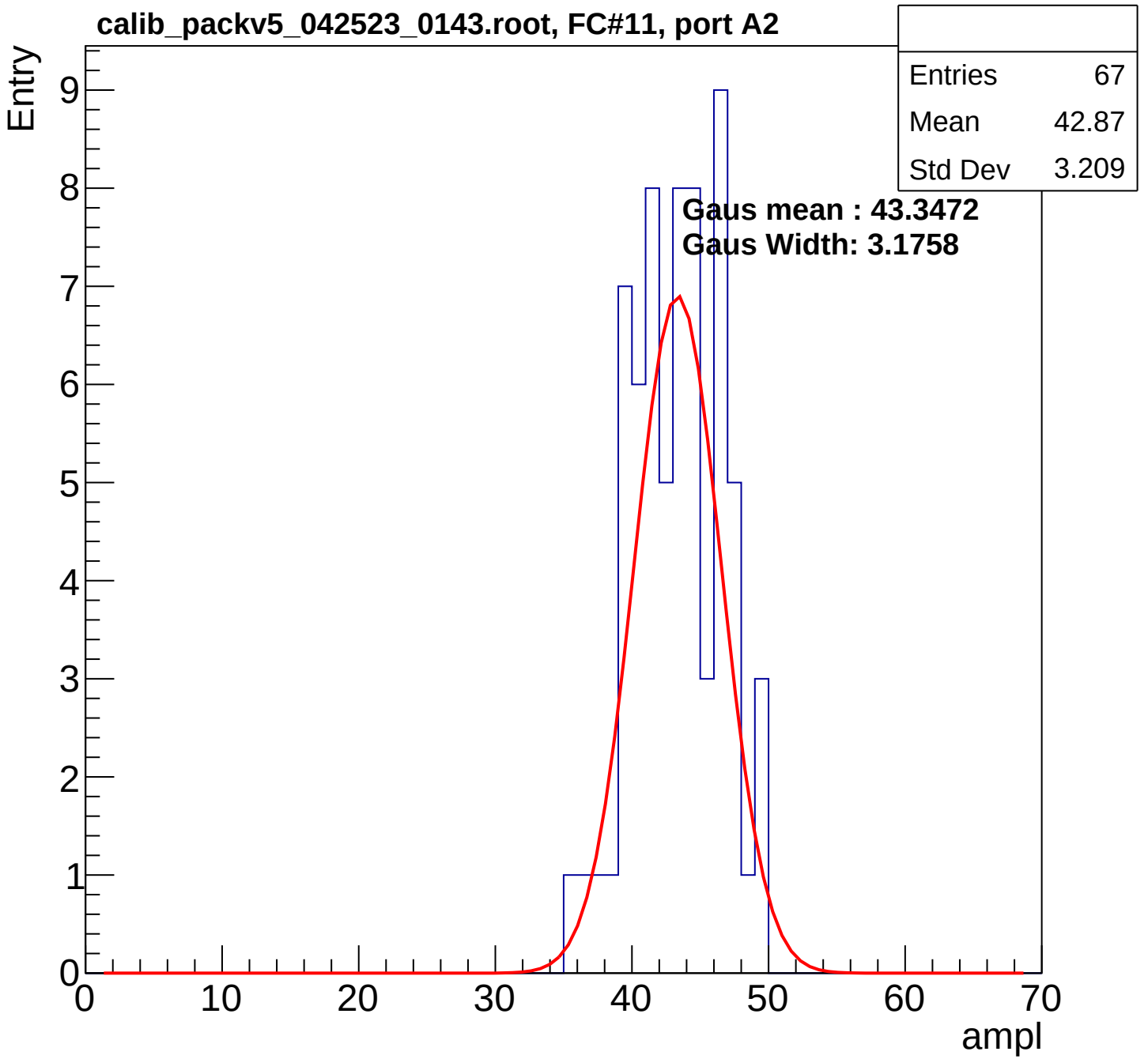
B1L102S, U7-ch115, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 67
Mean 42.87
Std Dev 3.209
Gaus mean : 43.3472
Gaus Width: 3.1758
Entry
ampl
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2
3
4
5
6
7
8
9
0
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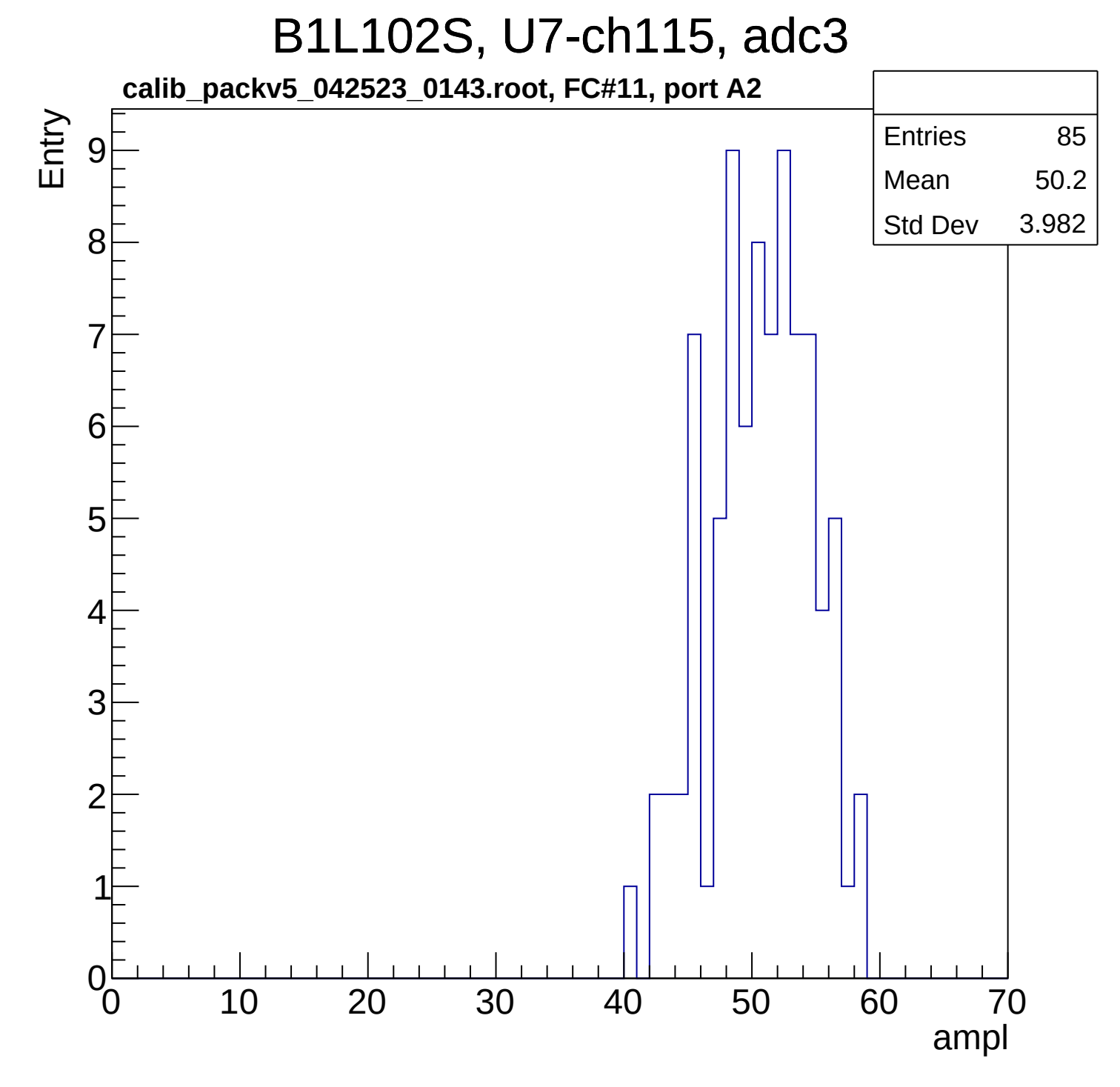
B1L102S, U7-ch115, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 85
Mean 50.2
Std Dev 3.982
Entry
ampl
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3
4
5
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7
8
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0
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20
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60
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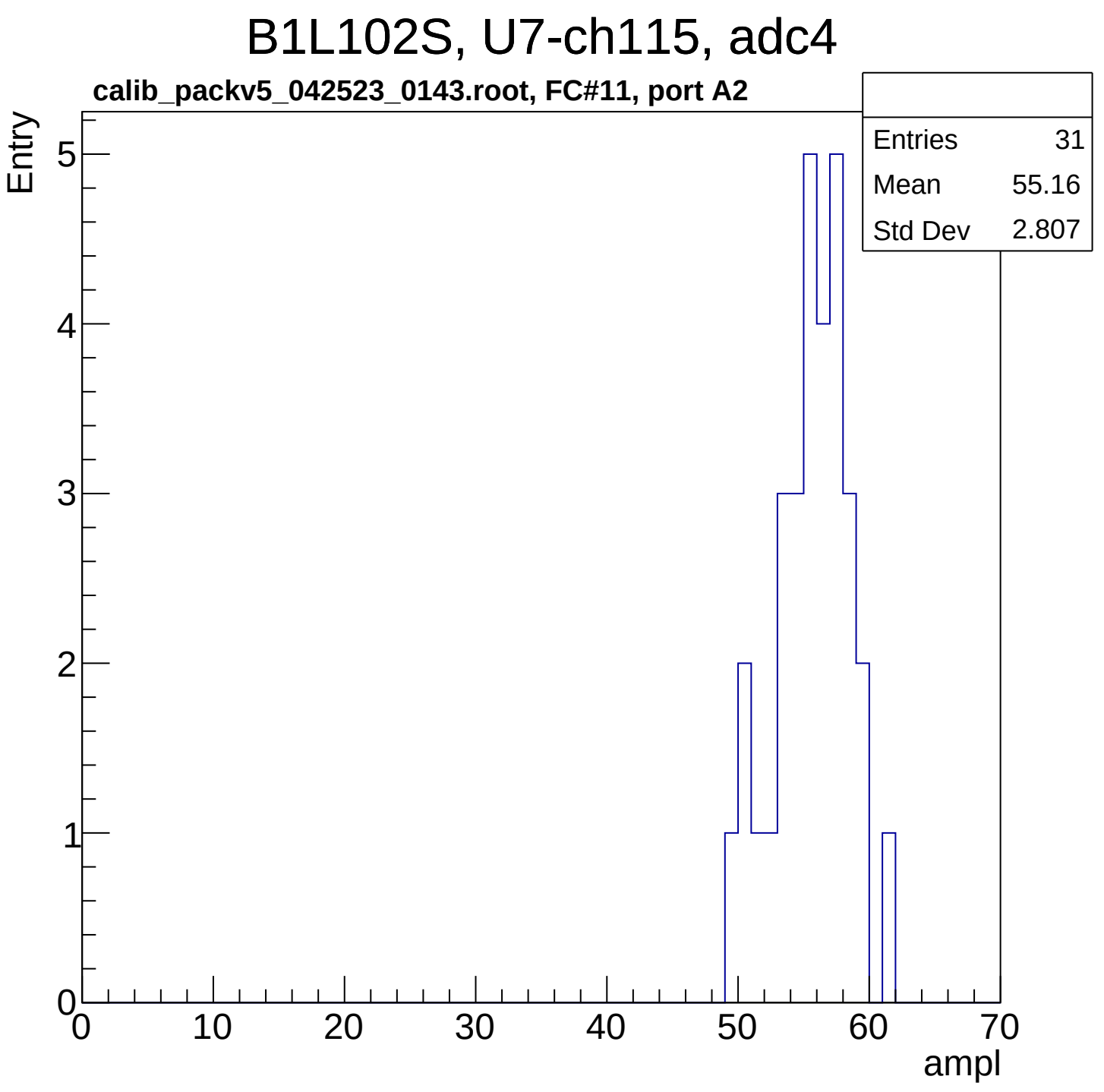
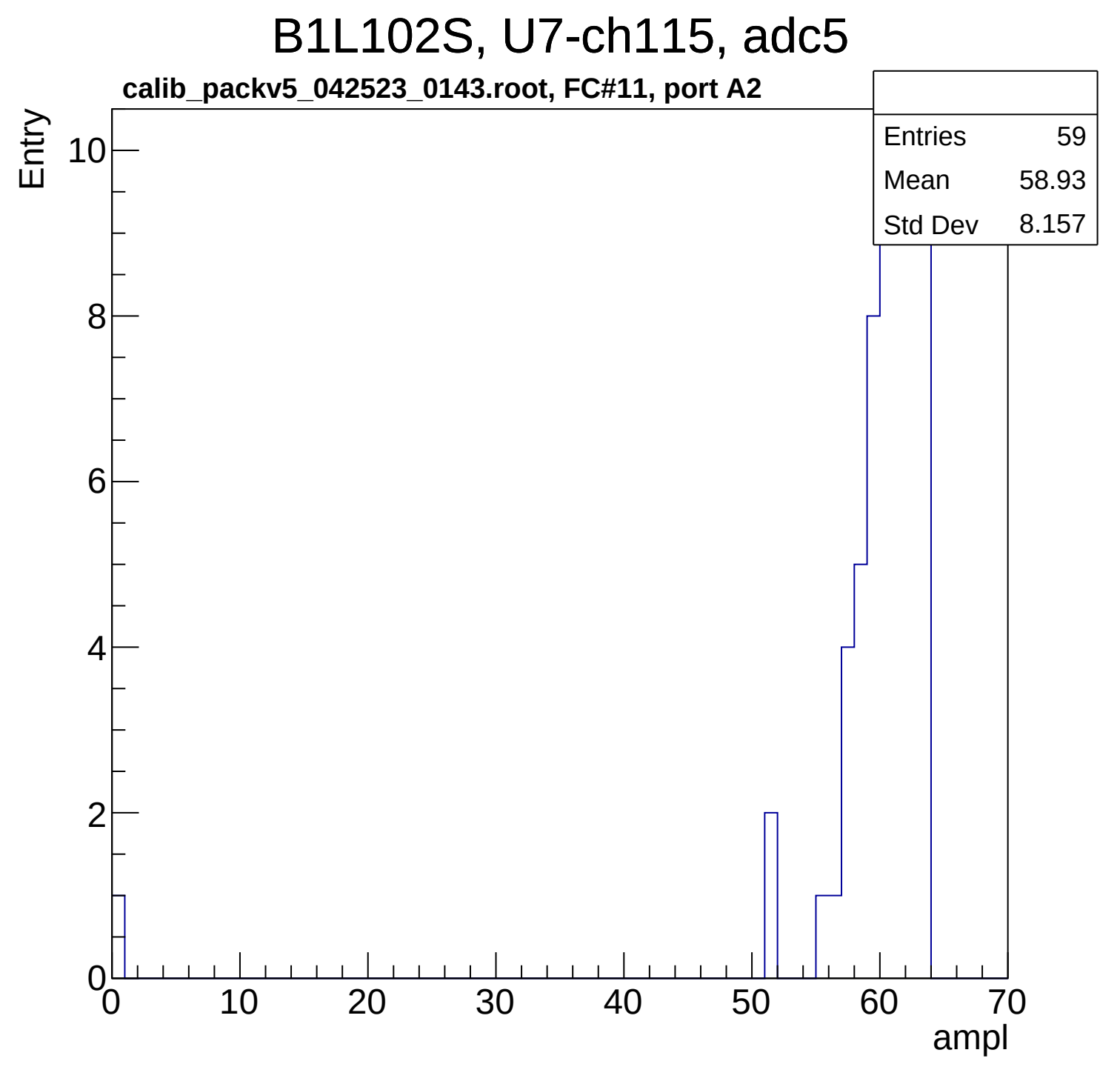

B1L102S, U7-ch115, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 31
Mean 55.16
Std Dev 2.807
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L102S, U7-ch115, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 59
Mean 58.93
Std Dev 8.157
Entry
ampl
0
2
4
6
8
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0
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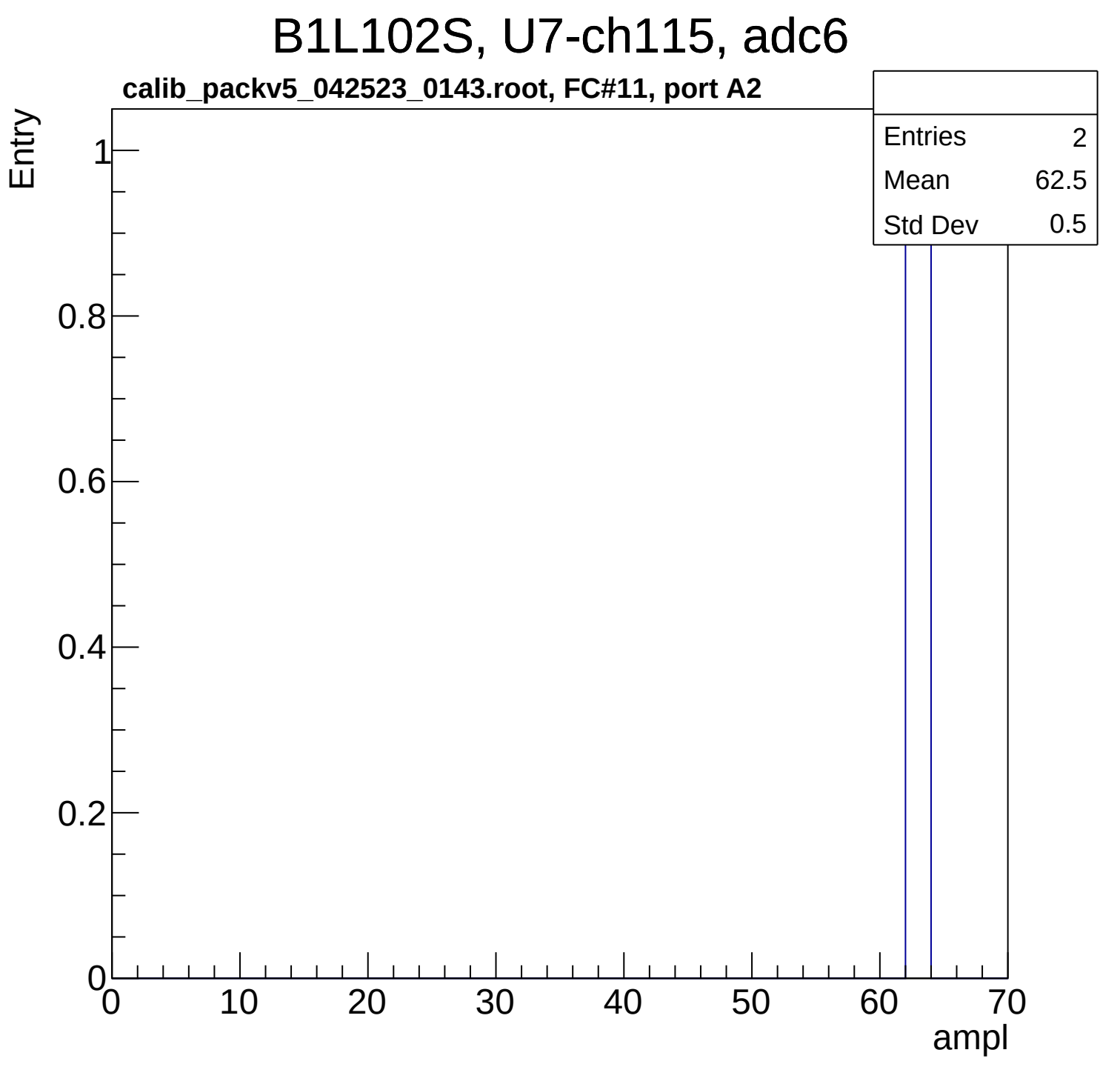
60
70


B1L102S, U7-ch115, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 2
Mean 62.5
Std Dev 0.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
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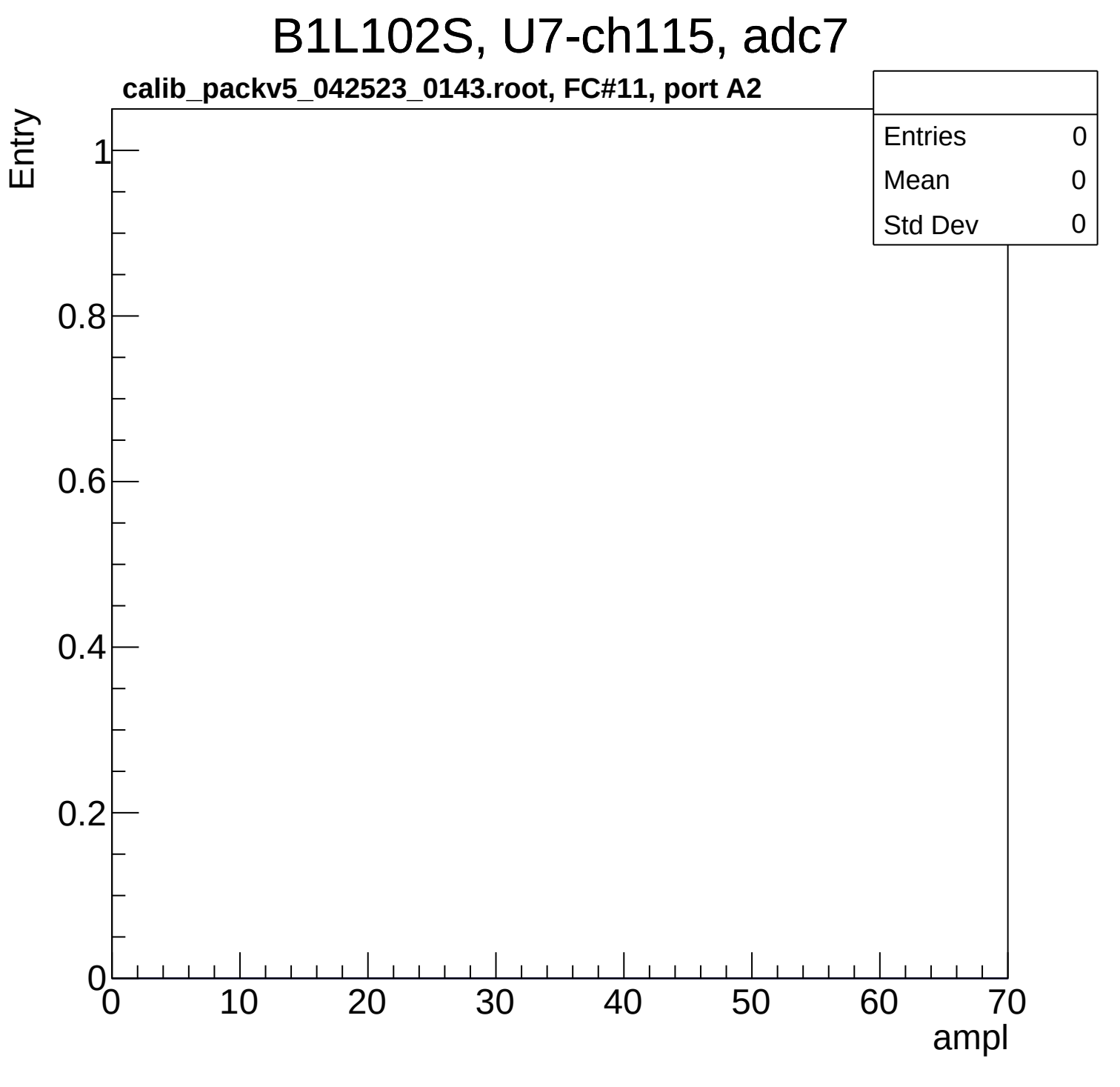
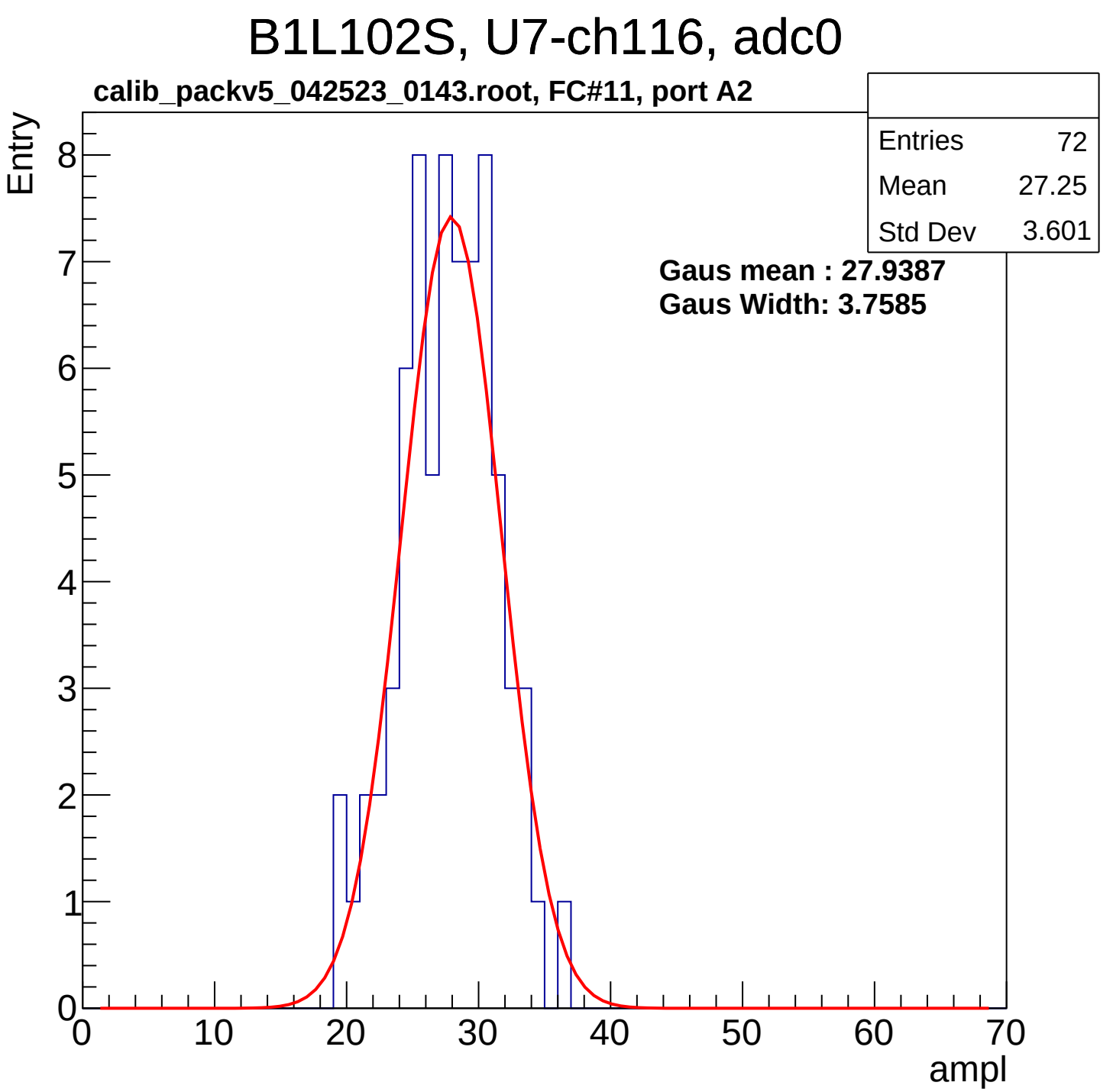
40
50
60
70
ampl


B1L102S, U7-ch115, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U7-ch116, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 72
Mean 27.25
Std Dev 3.601
Gaus mean : 27.9387
Gaus Width: 3.7585
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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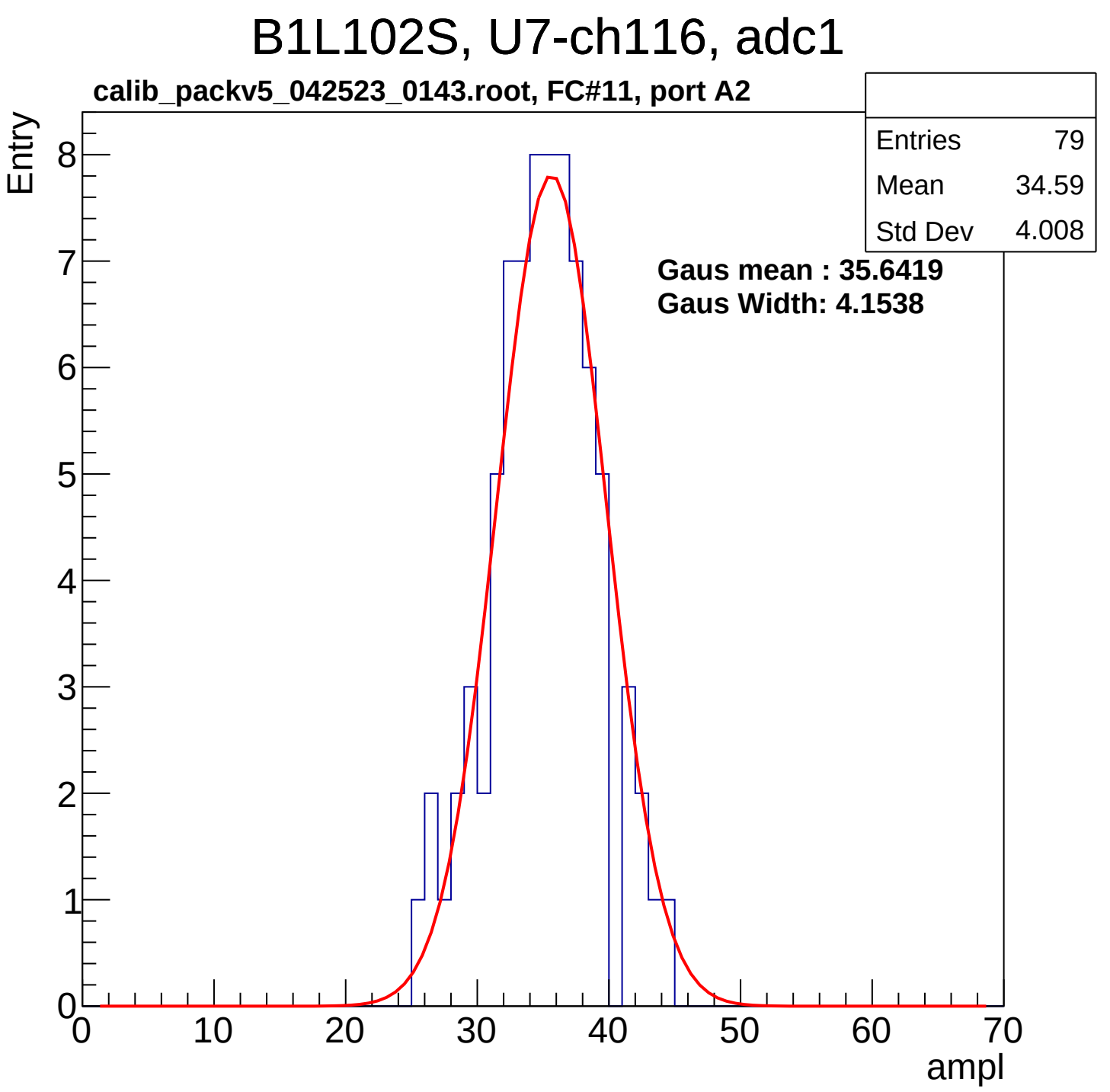
B1L102S, U7-ch116, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 79
Mean 34.59
Std Dev 4.008
Gaus mean : 35.6419
Gaus Width: 4.1538
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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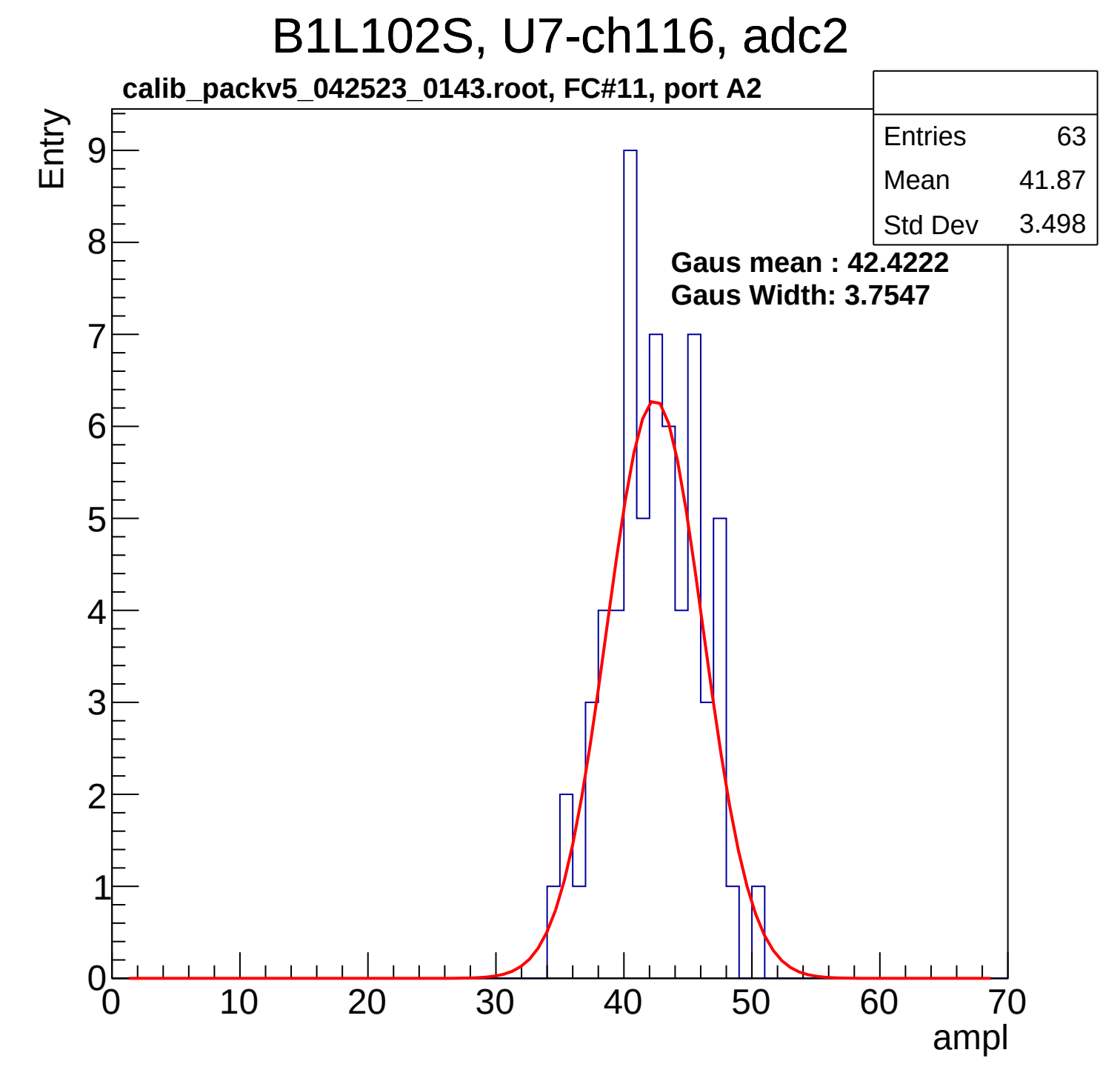
B1L102S, U7-ch116, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 63
Mean 41.87
Std Dev 3.498
Gaus mean : 42.4222
Gaus Width: 3.7547
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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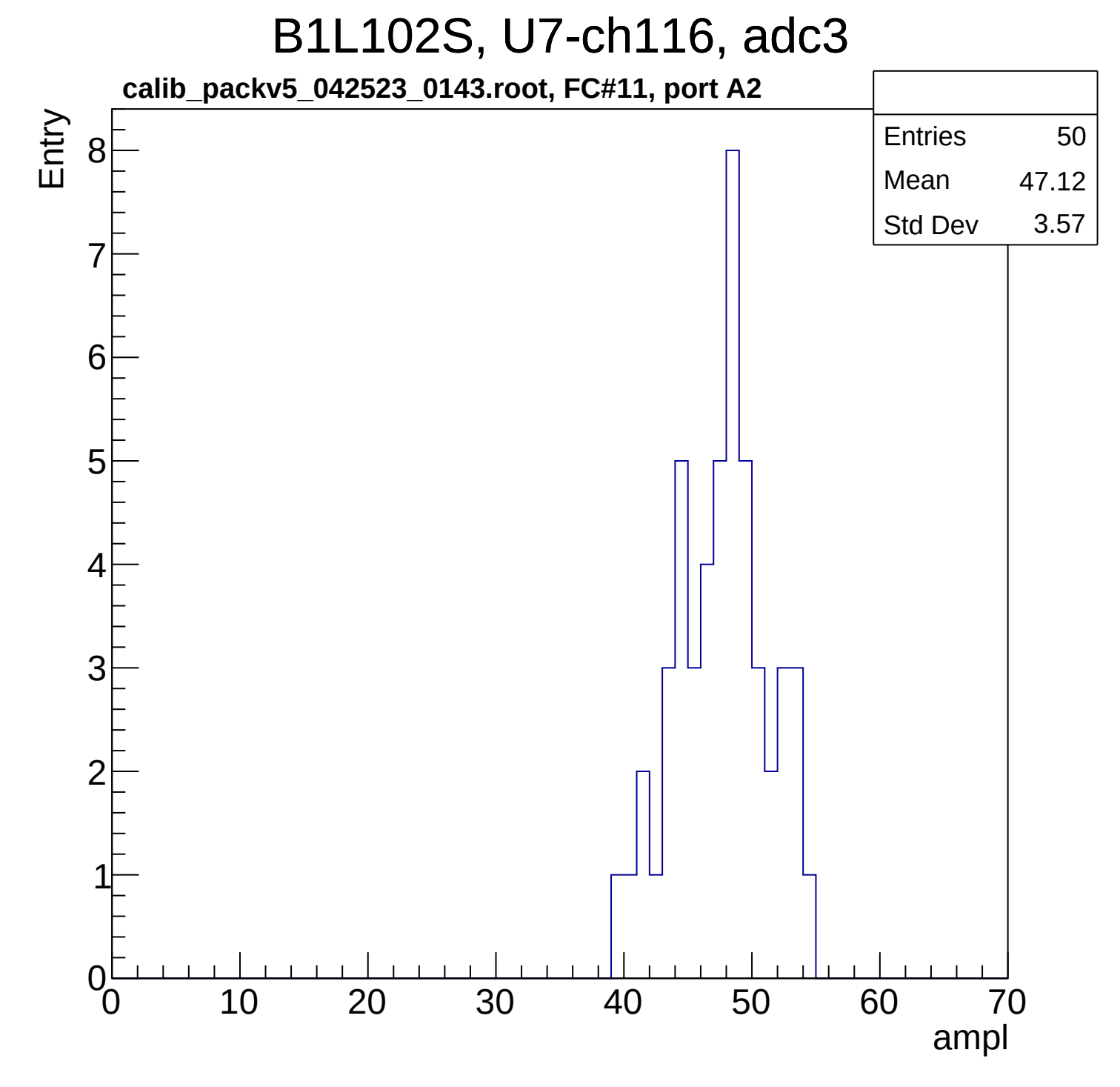
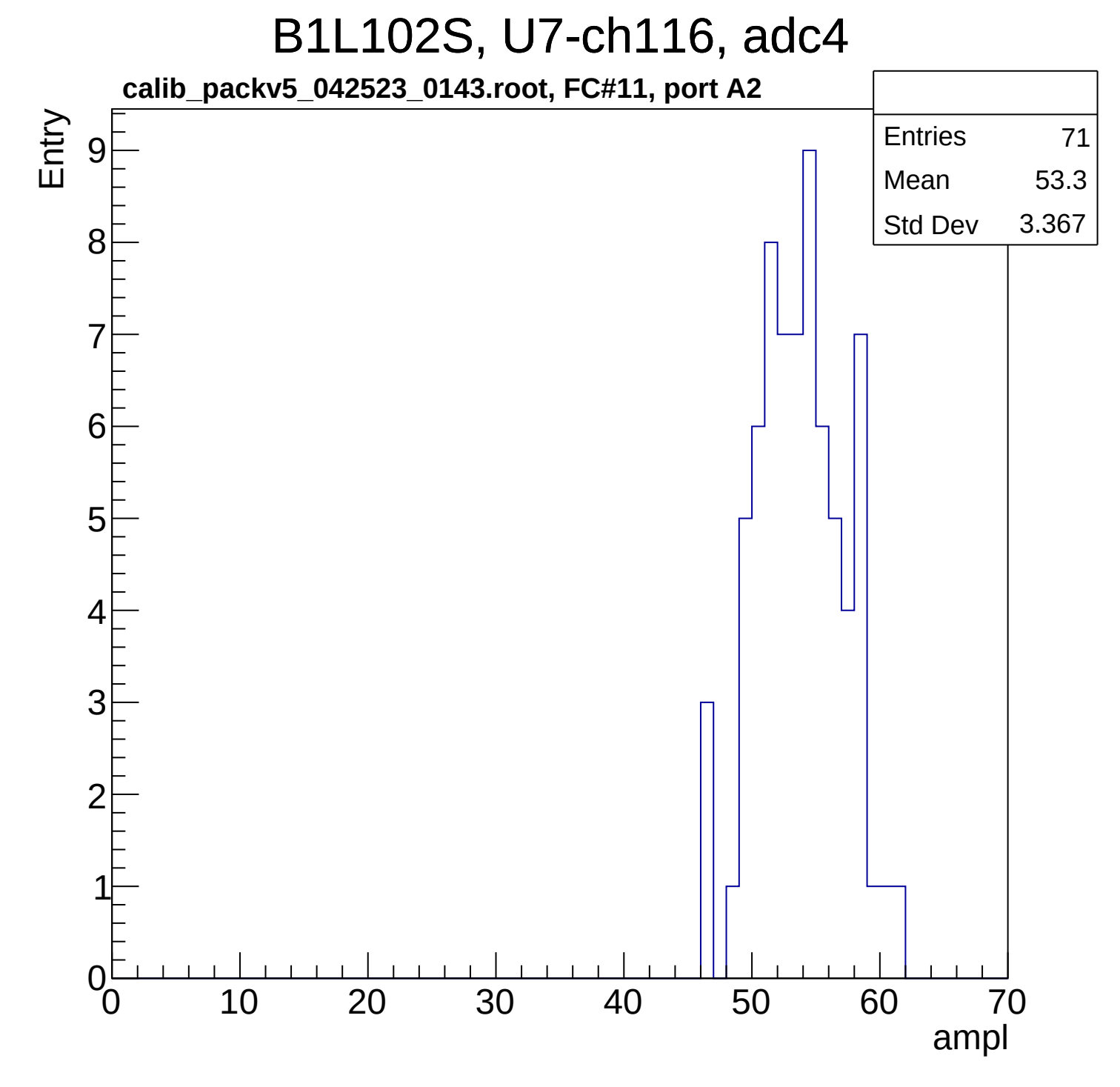
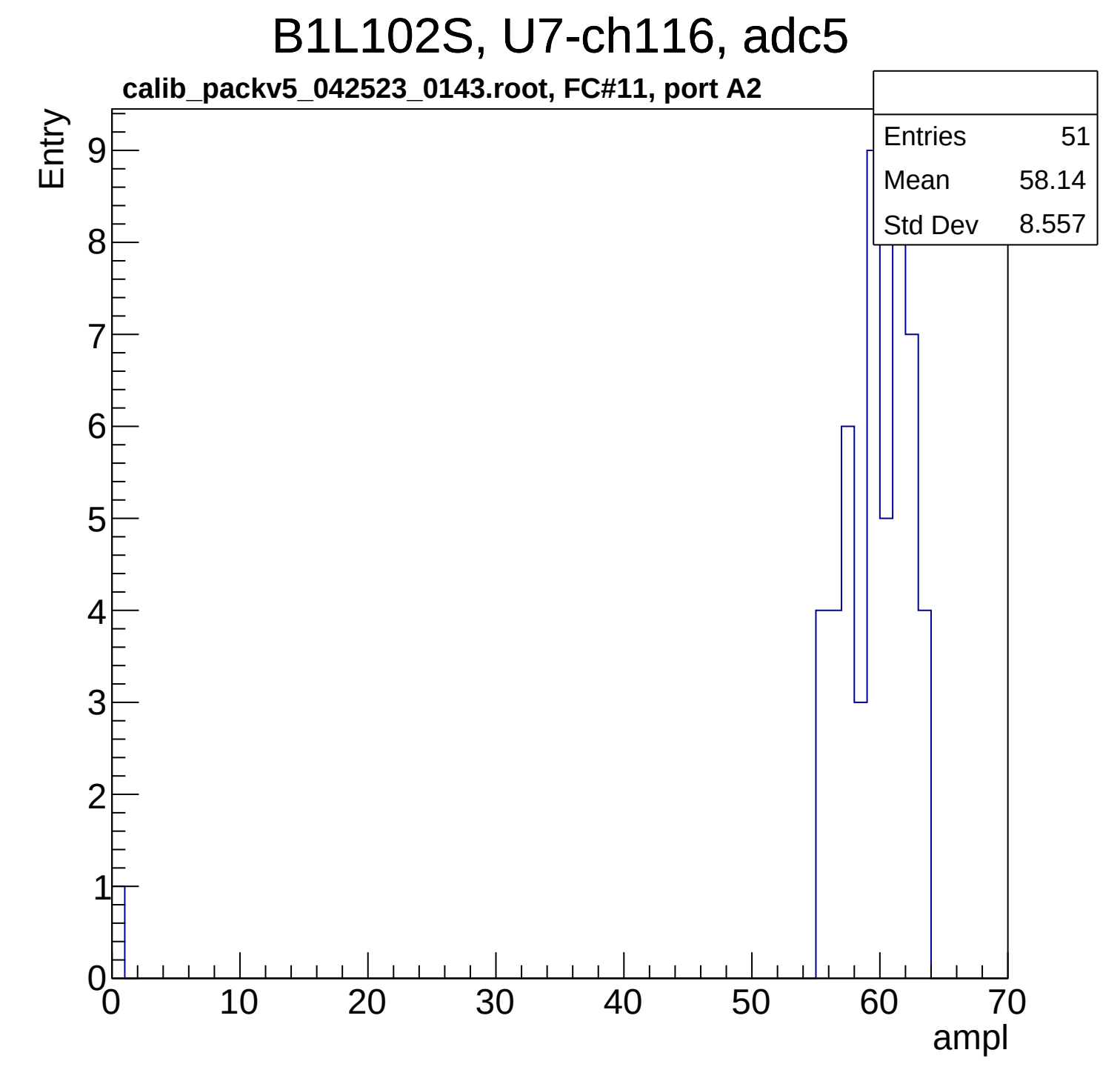
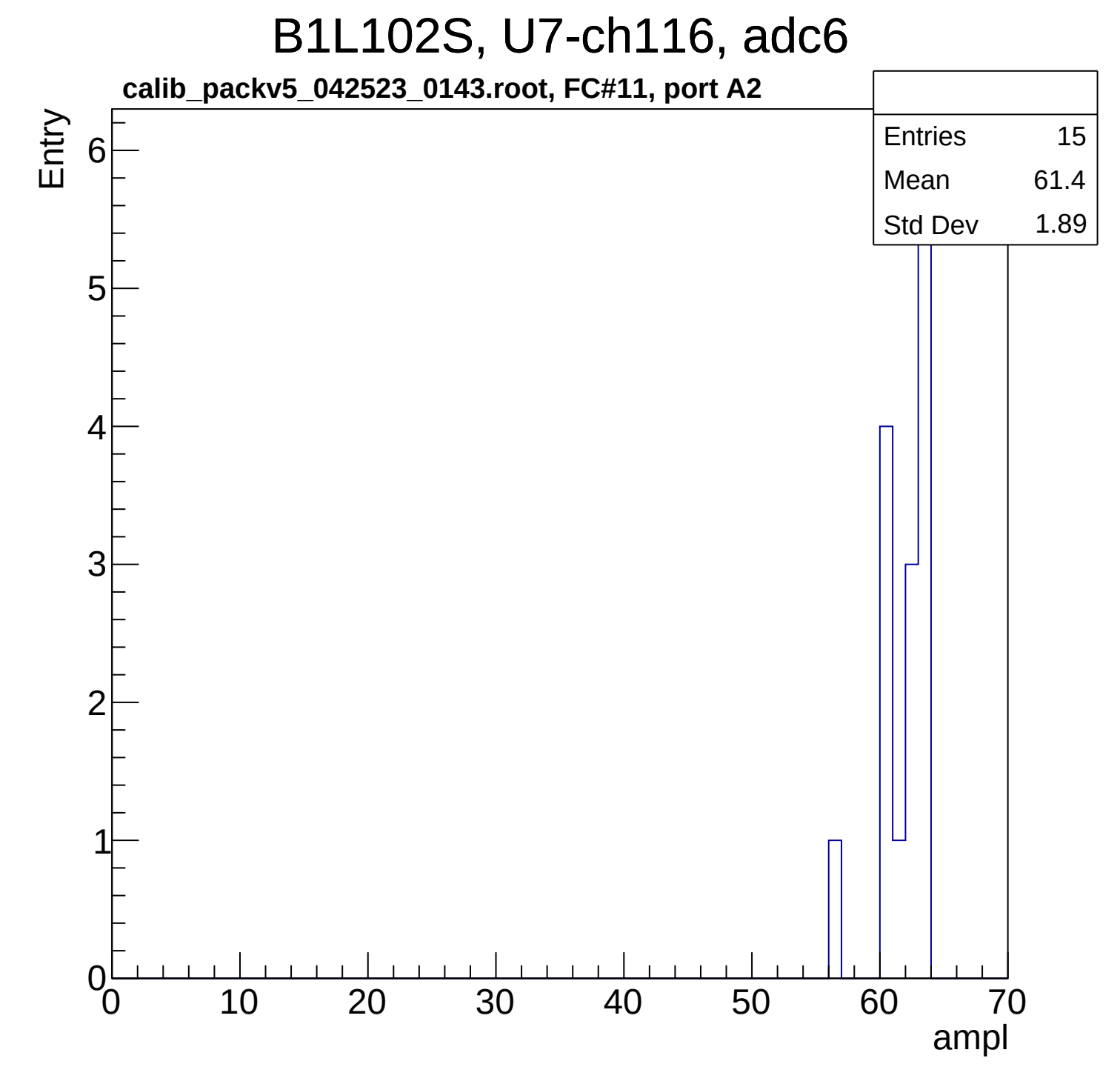
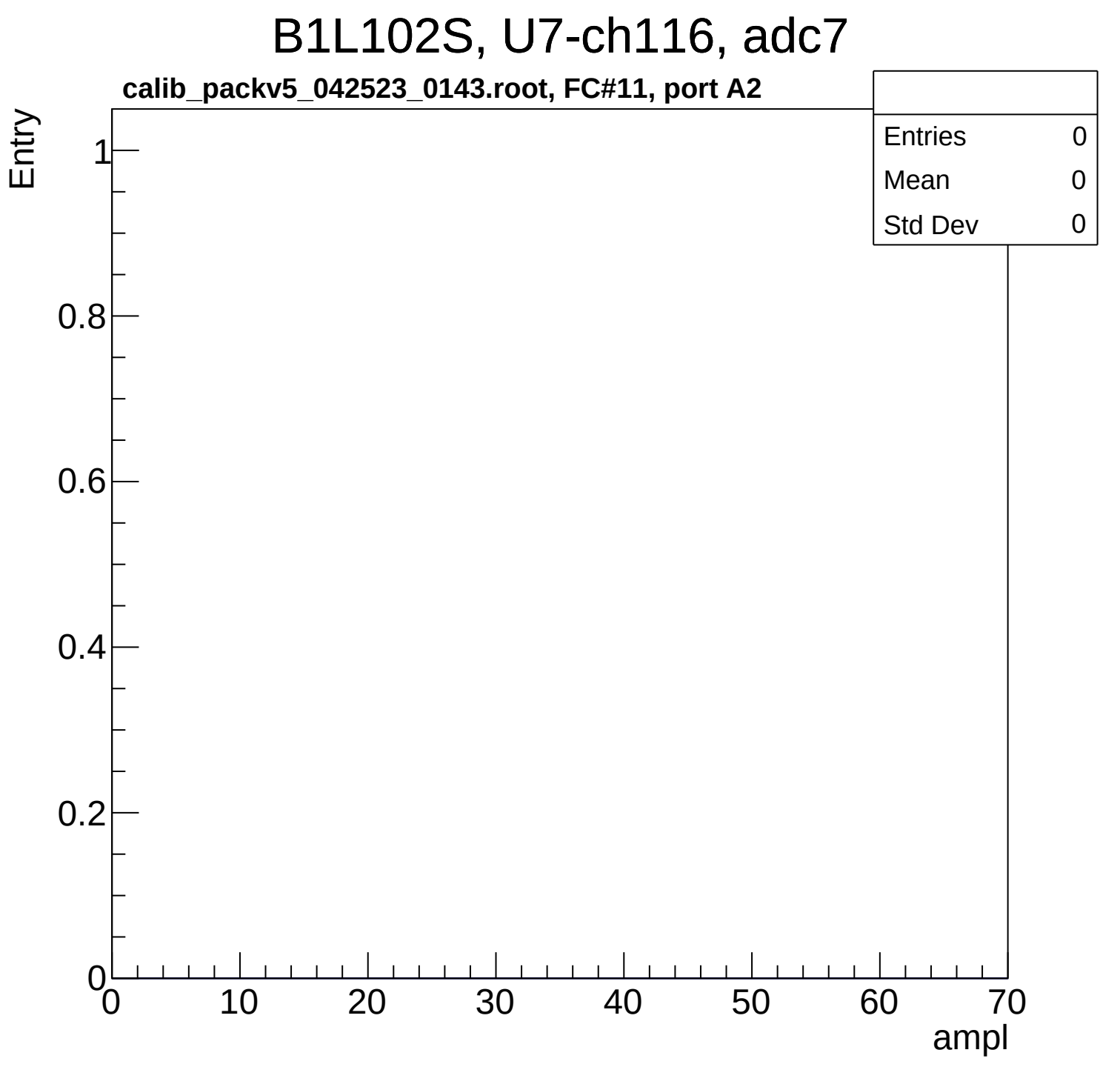
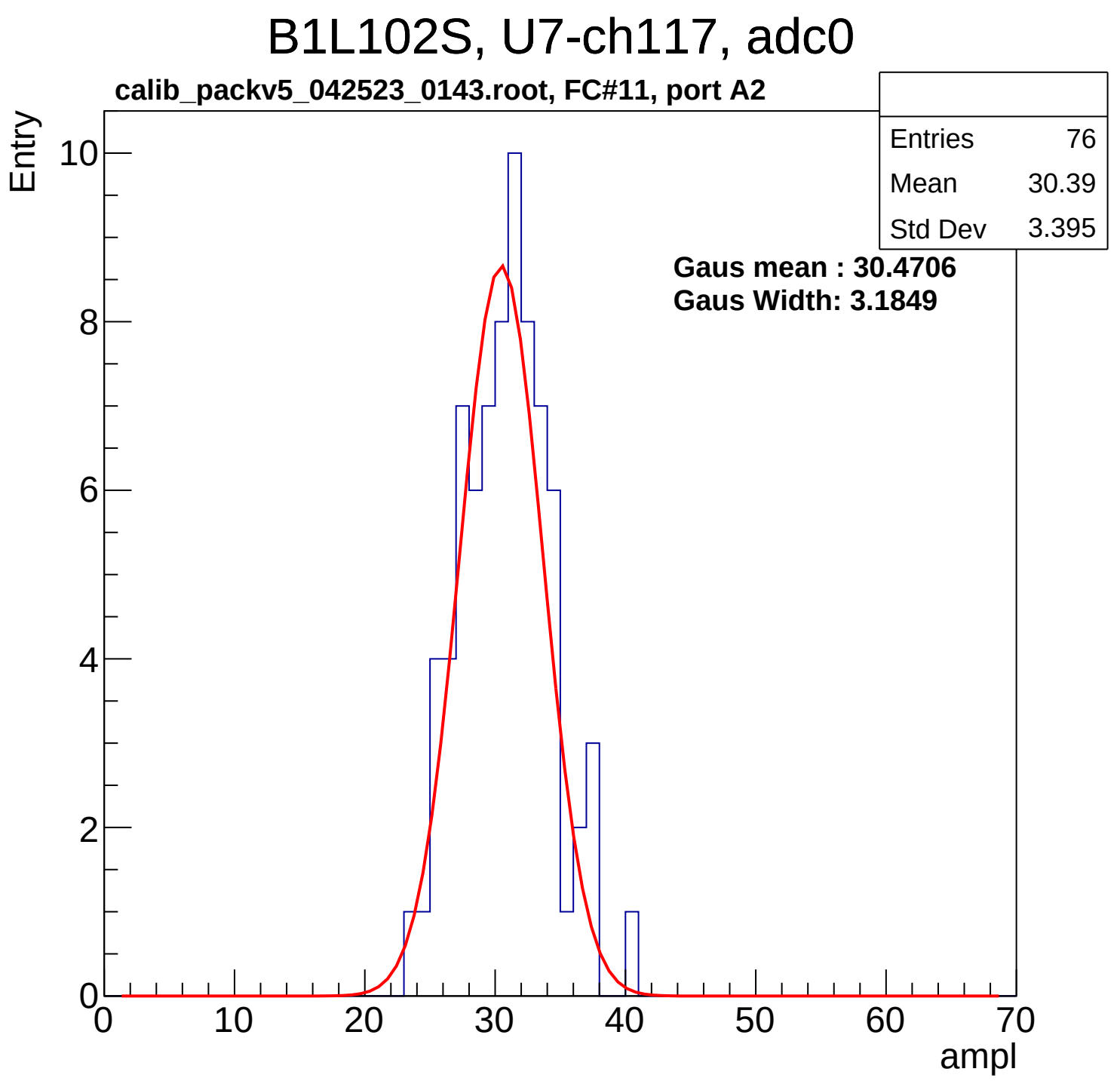

B1L102S, U7-ch116, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 50
Mean 47.12
Std Dev 3.57
Entry
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl

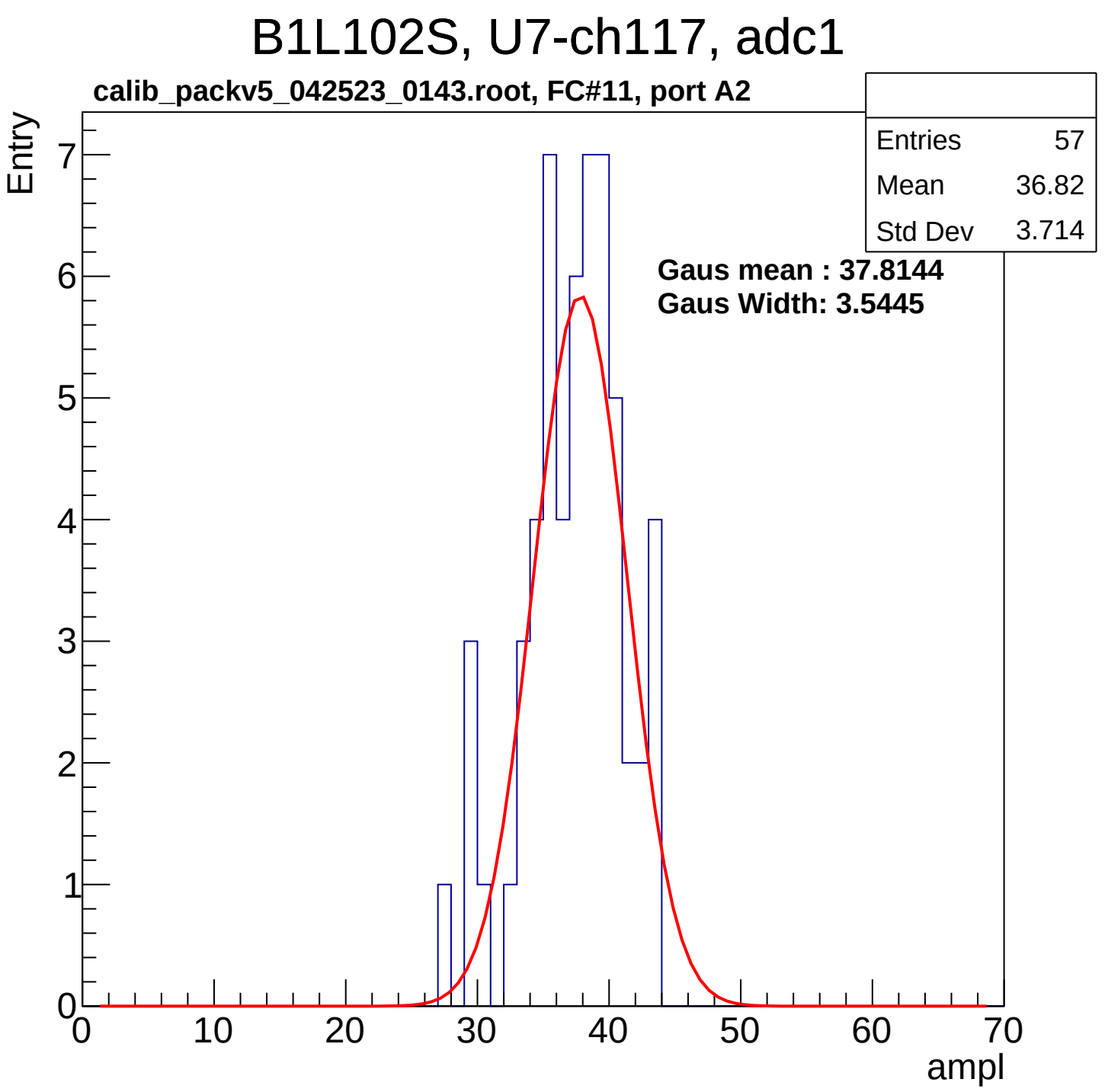

B1L102S, U7-ch116, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 71
Mean 53.3
Std Dev 3.367
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

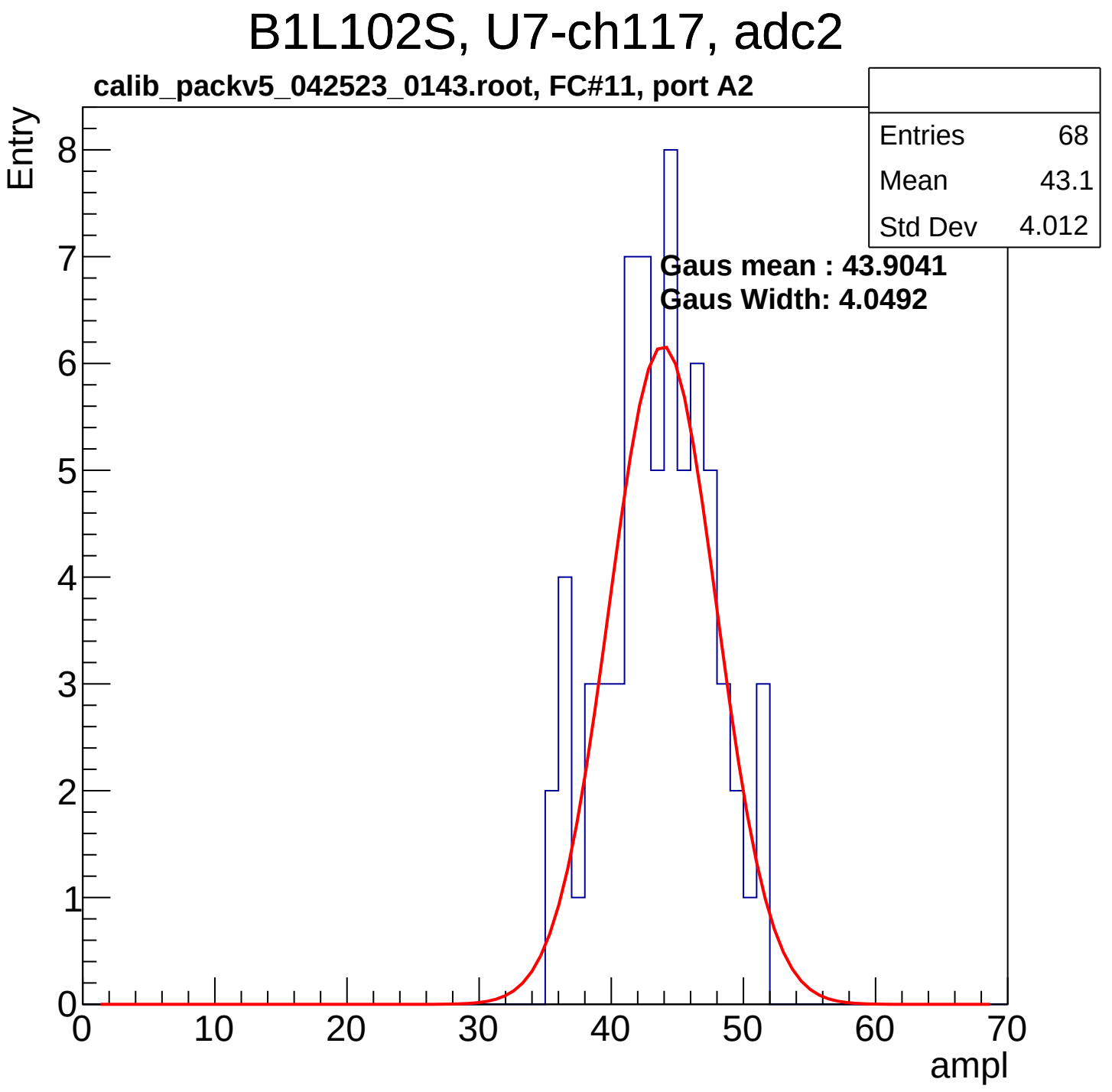

B1L102S, U7-ch116, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 51
Mean 58.14
Std Dev 8.557
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

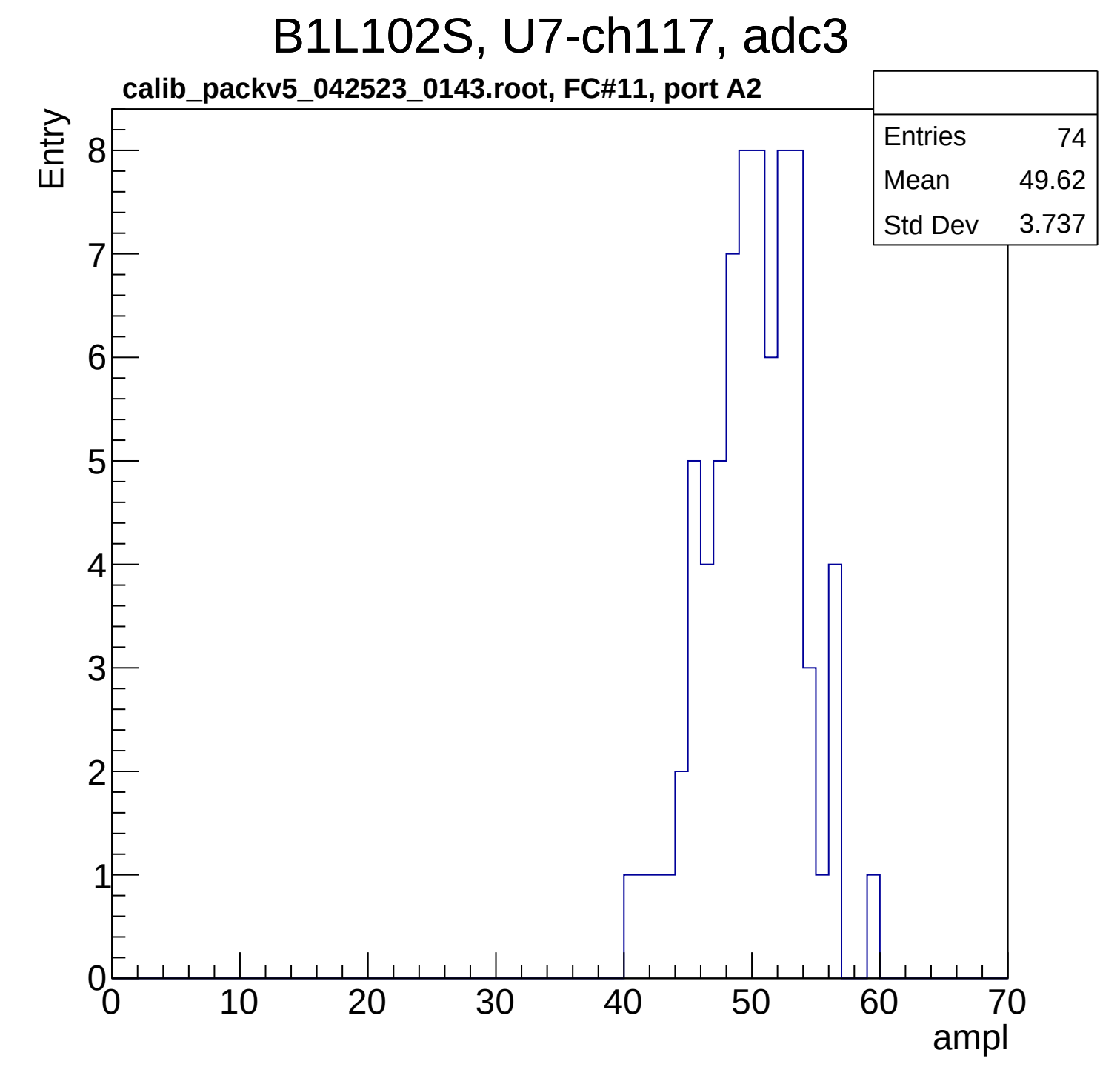

B1L102S, U7-ch116, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 15
Mean 61.4
Std Dev 1.89
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

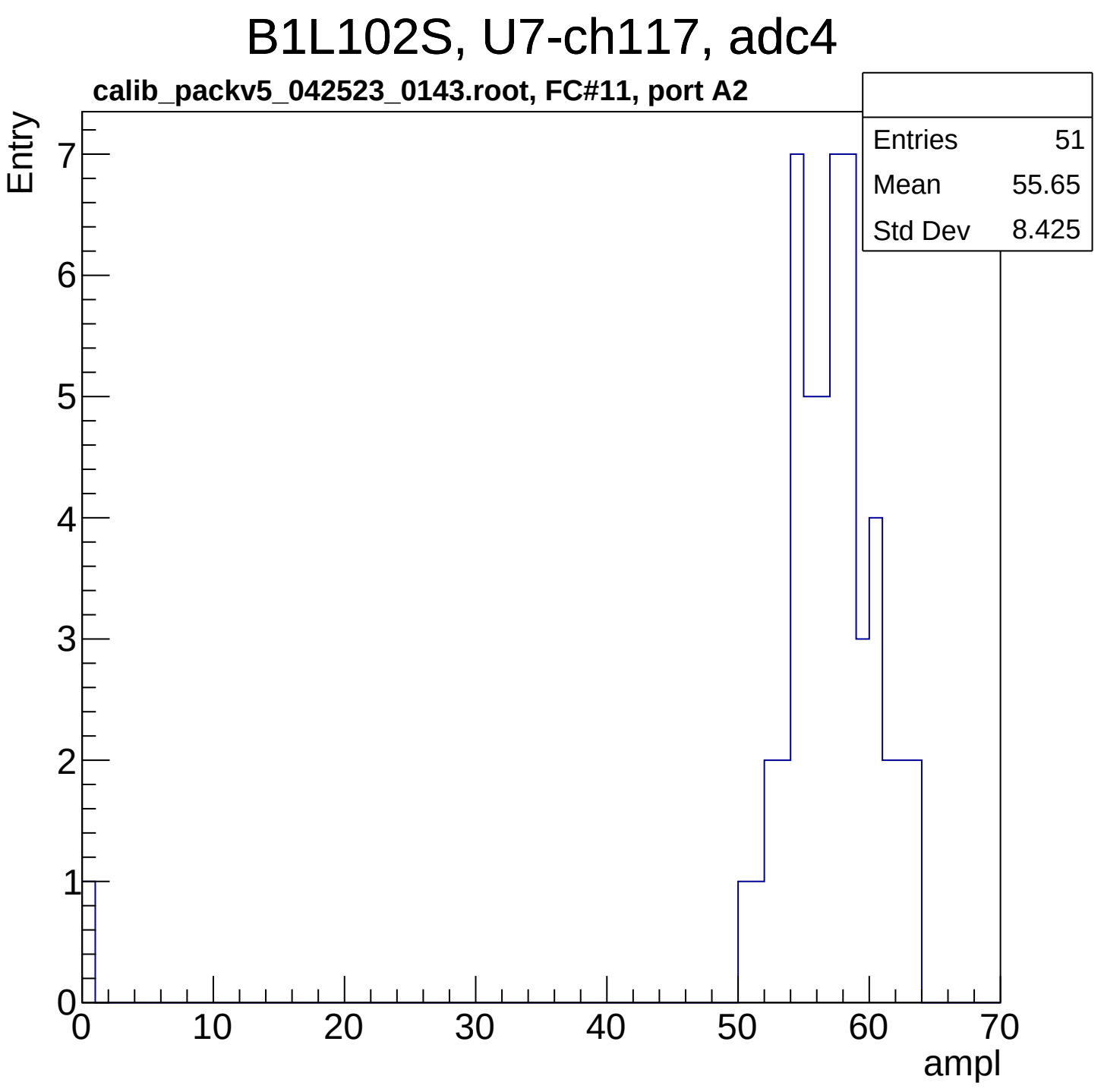

B1L102S, U7-ch116, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

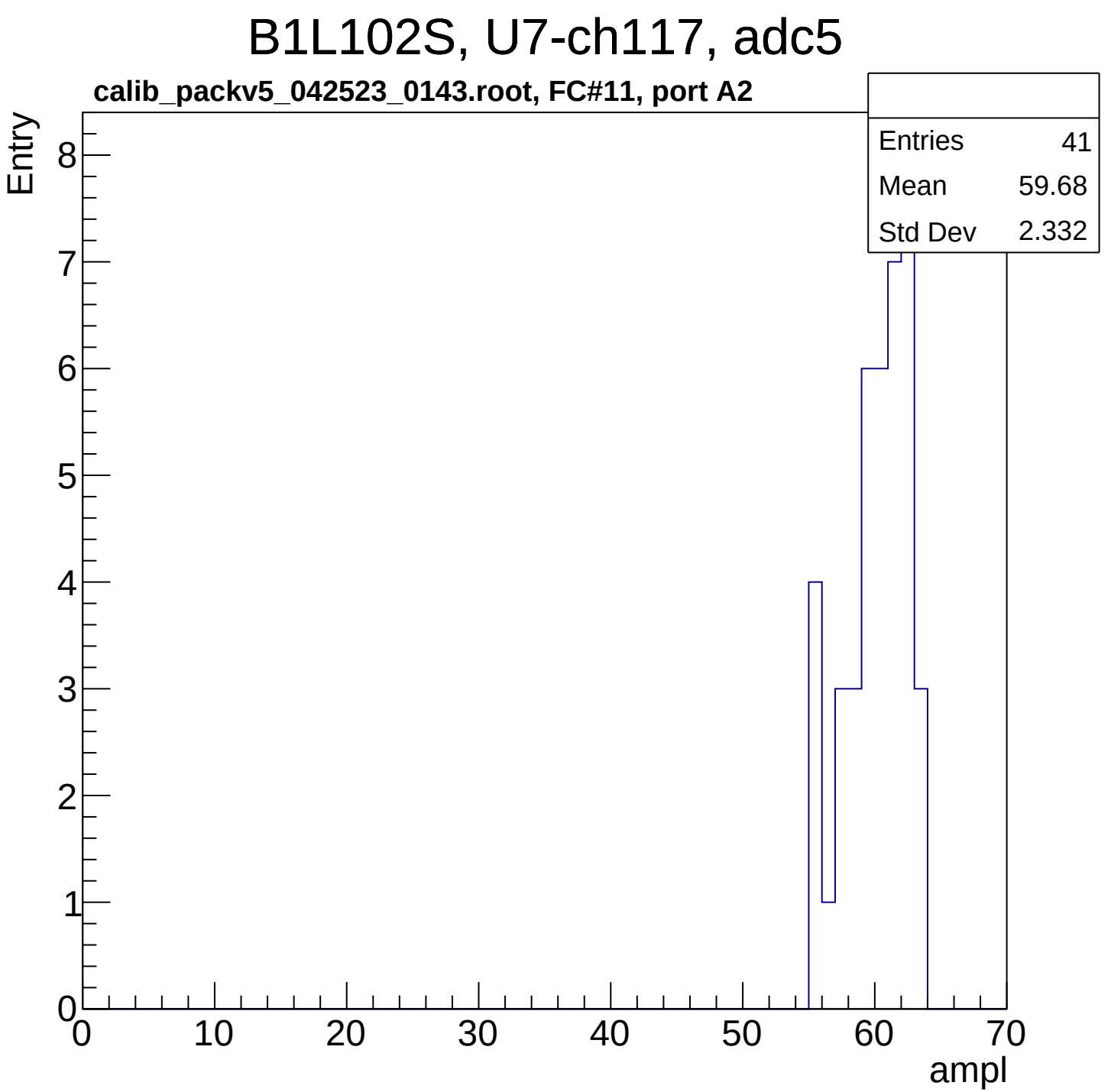

B1L102S, U7-ch117, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 76
Mean 30.39
Std Dev 3.395
Gaus mean : 30.4706
Gaus Width: 3.1849
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

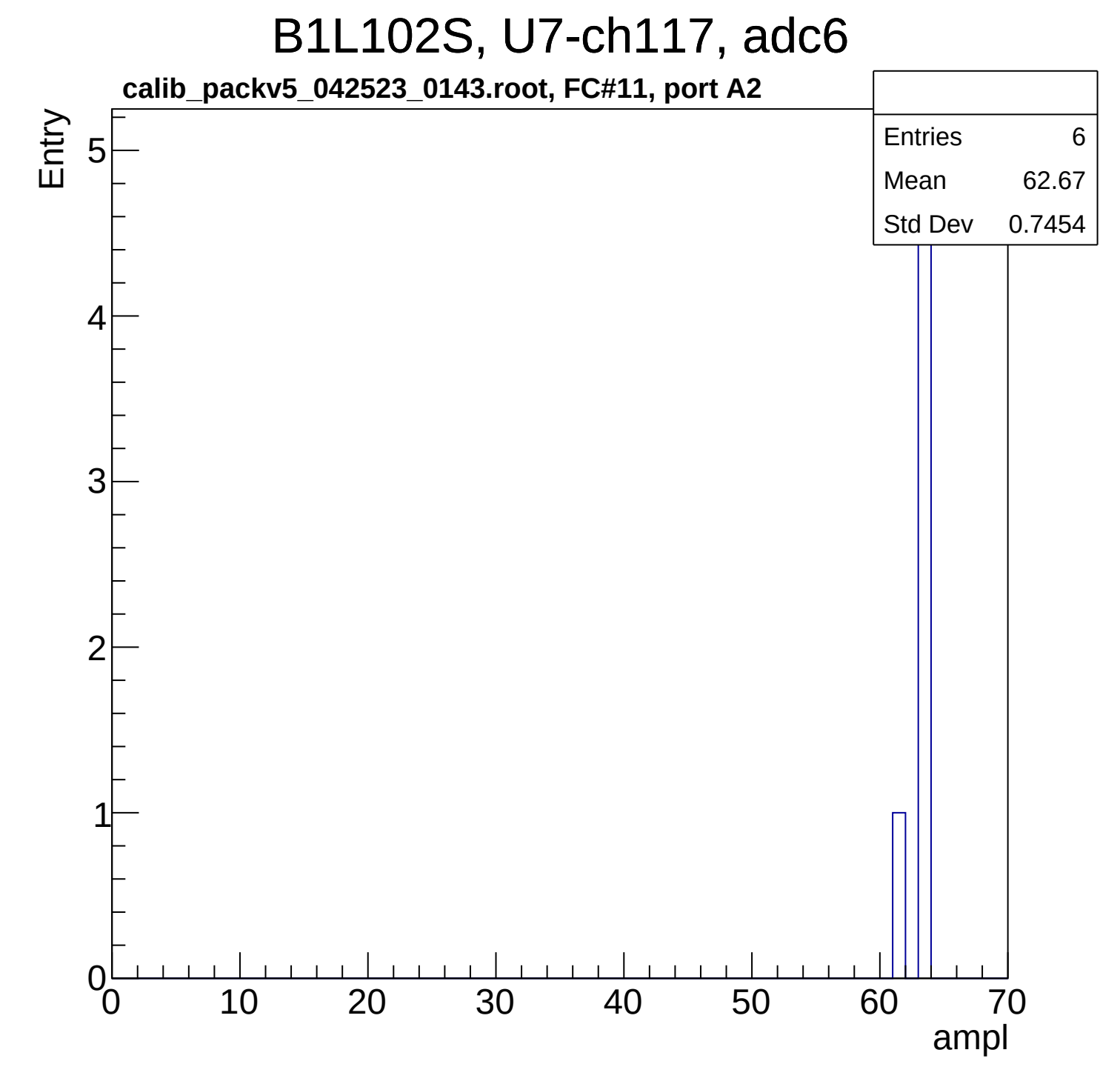

B1L102S, U7-ch117, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 57
Mean 36.82
Std Dev 3.714
Gaus mean : 37.8144
Gaus Width: 3.5445
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

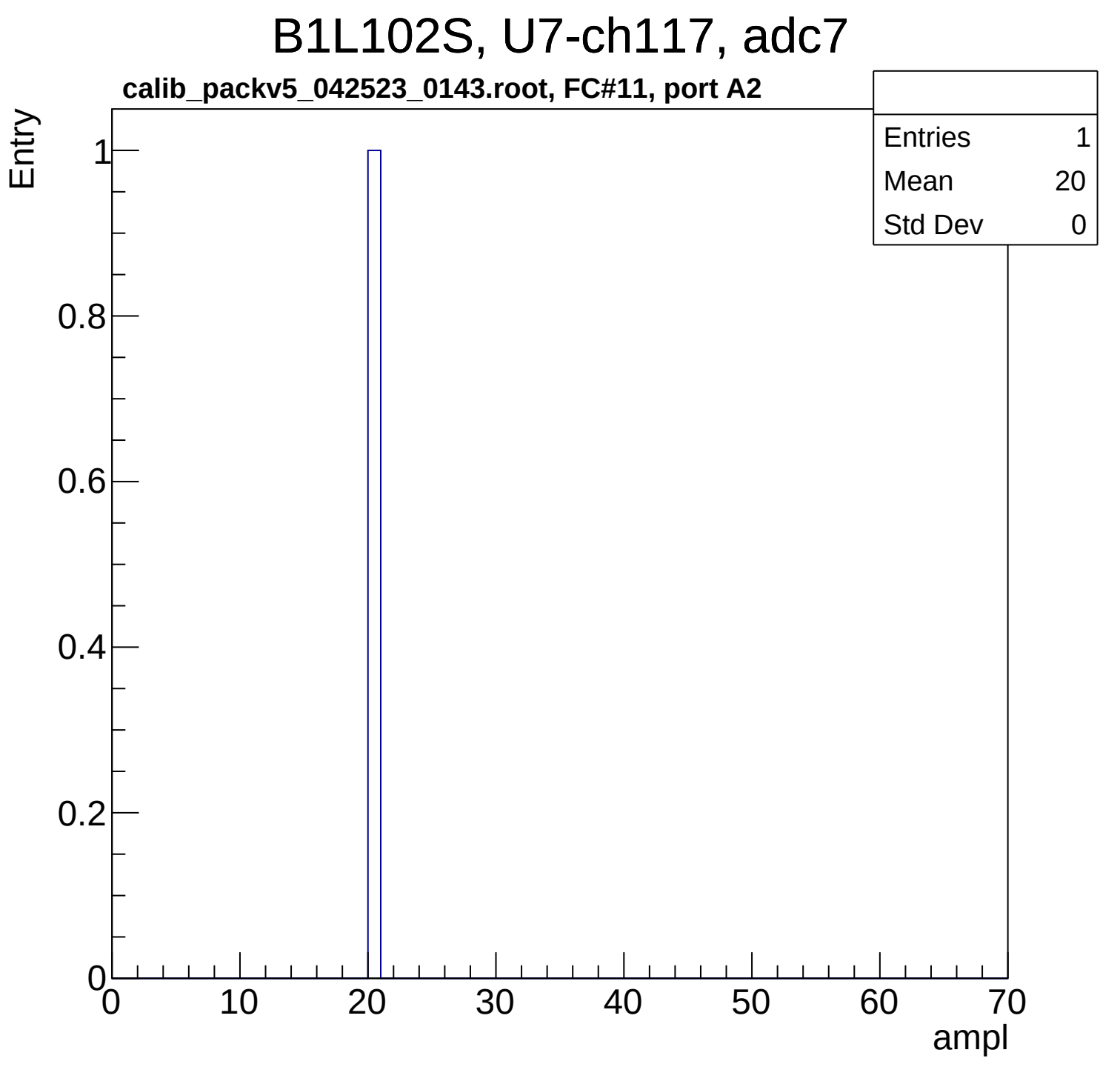

B1L102S, U7-ch117, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 68
Mean 43.1
Std Dev 4.012
Gaus mean : 43.9041
Gaus Width: 4.0492
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

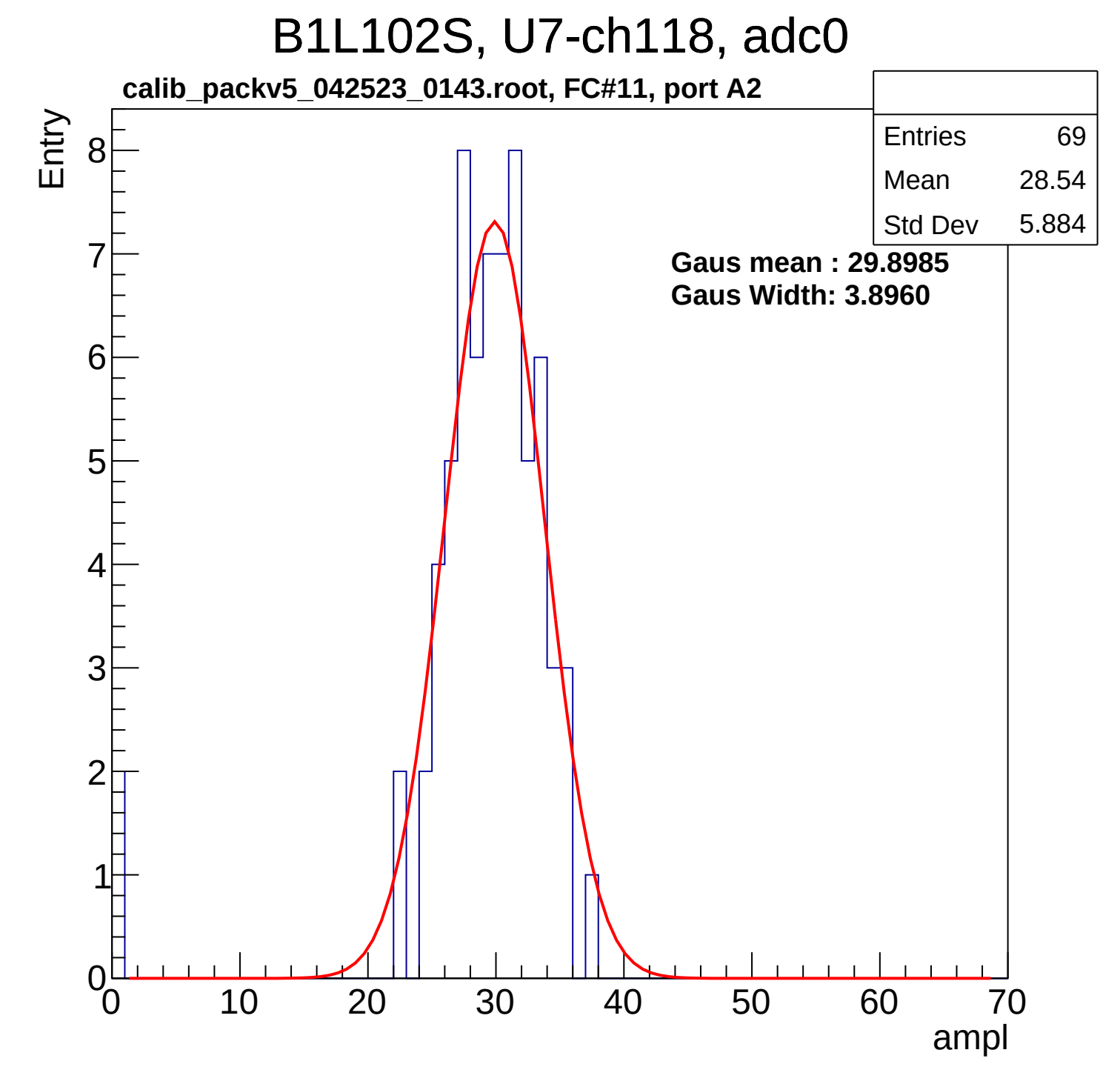

B1L102S, U7-ch117, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 74
Mean 49.62
Std Dev 3.737
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L102S, U7-ch117, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 51
Mean 55.65
Std Dev 8.425
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L102S, U7-ch117, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 41
Mean 59.68
Std Dev 2.332
Entry
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L102S, U7-ch117, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 6
Mean 62.67
Std Dev 0.7454
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L102S, U7-ch117, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 1
Mean 20
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U7-ch118, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 69
Mean 28.54
Std Dev 5.884
Gaus mean : 29.8985
Gaus Width: 3.8960
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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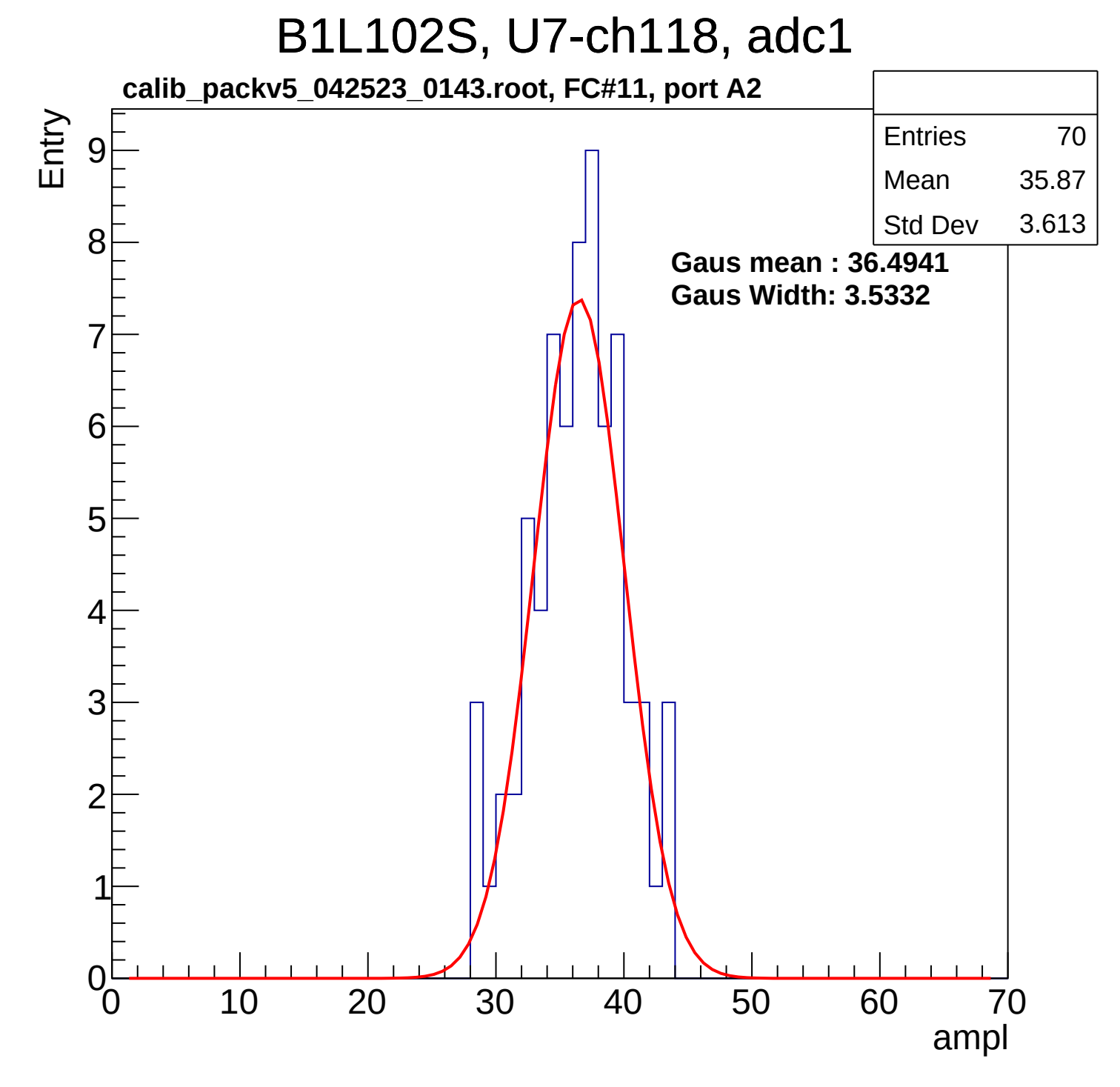
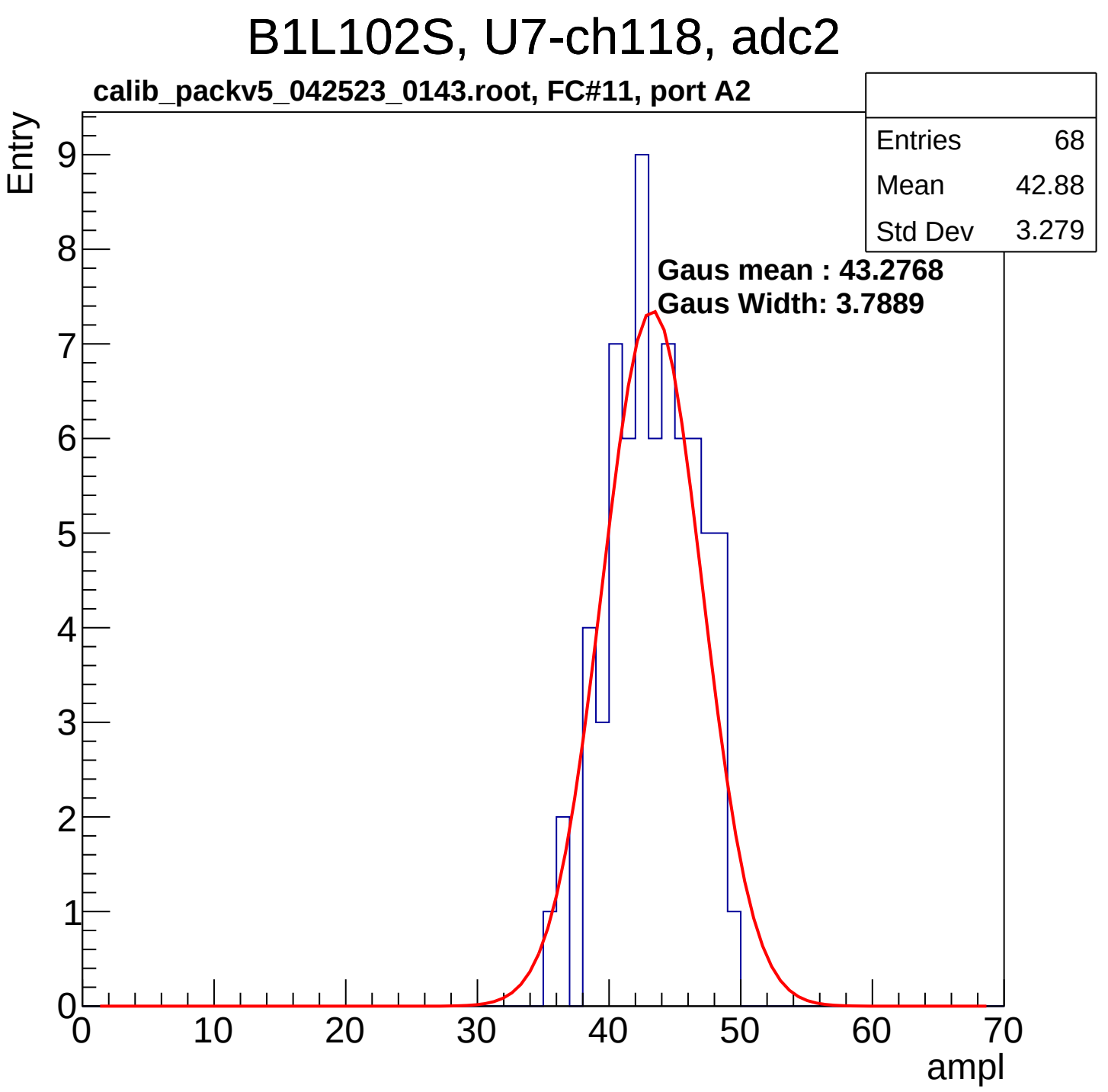
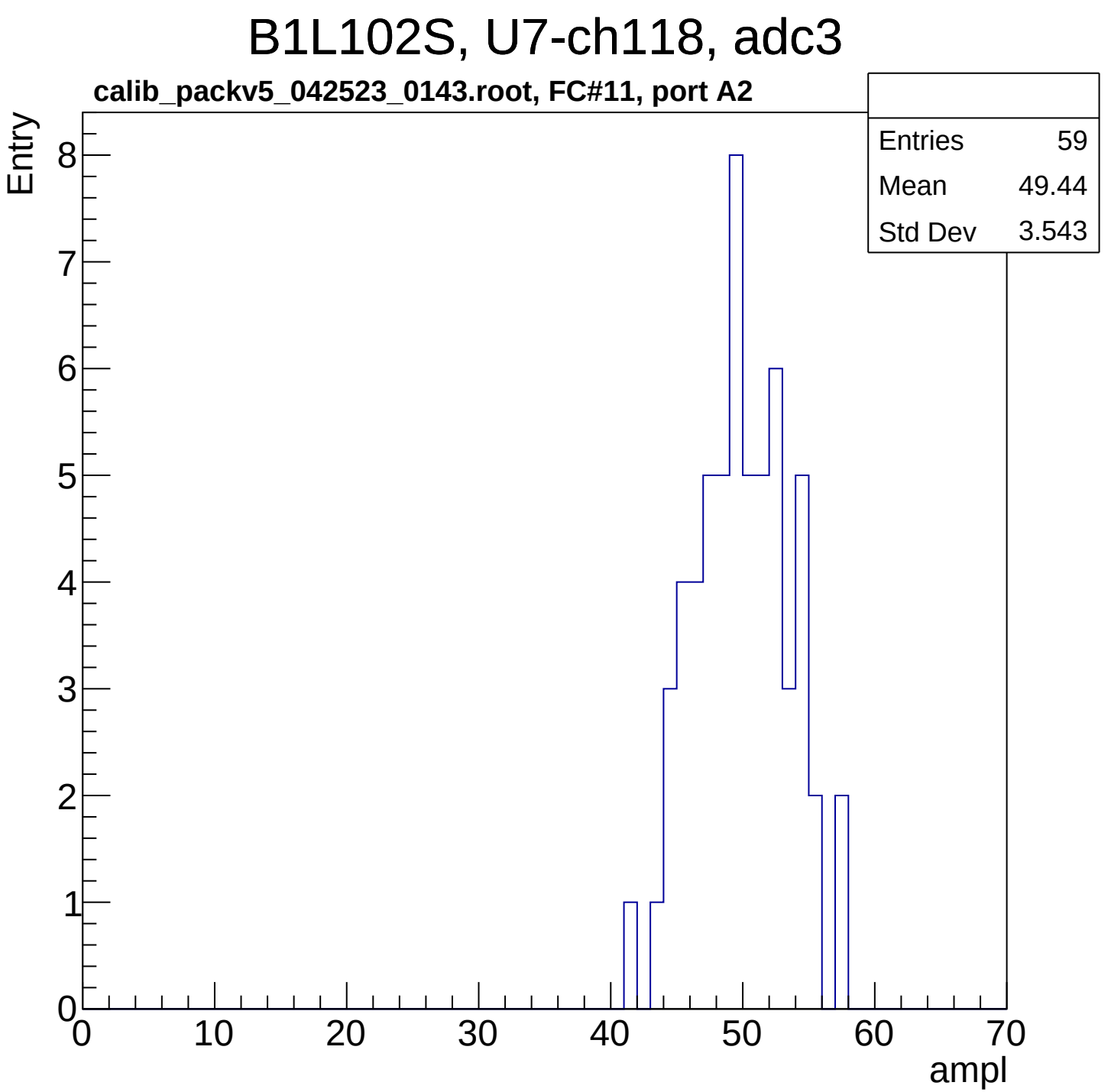

B1L102S, U7-ch118, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 70
Mean 35.87
Std Dev 3.613
Gaus mean : 36.4941
Gaus Width: 3.5332
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L102S, U7-ch118, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 68
Mean 42.88
Std Dev 3.279
Gaus mean : 43.2768
Gaus Width: 3.7889
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L102S, U7-ch118, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 59
Mean 49.44
Std Dev 3.543
Entry
ampl
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1
2
3
4
5
6
7
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0
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40
50
60
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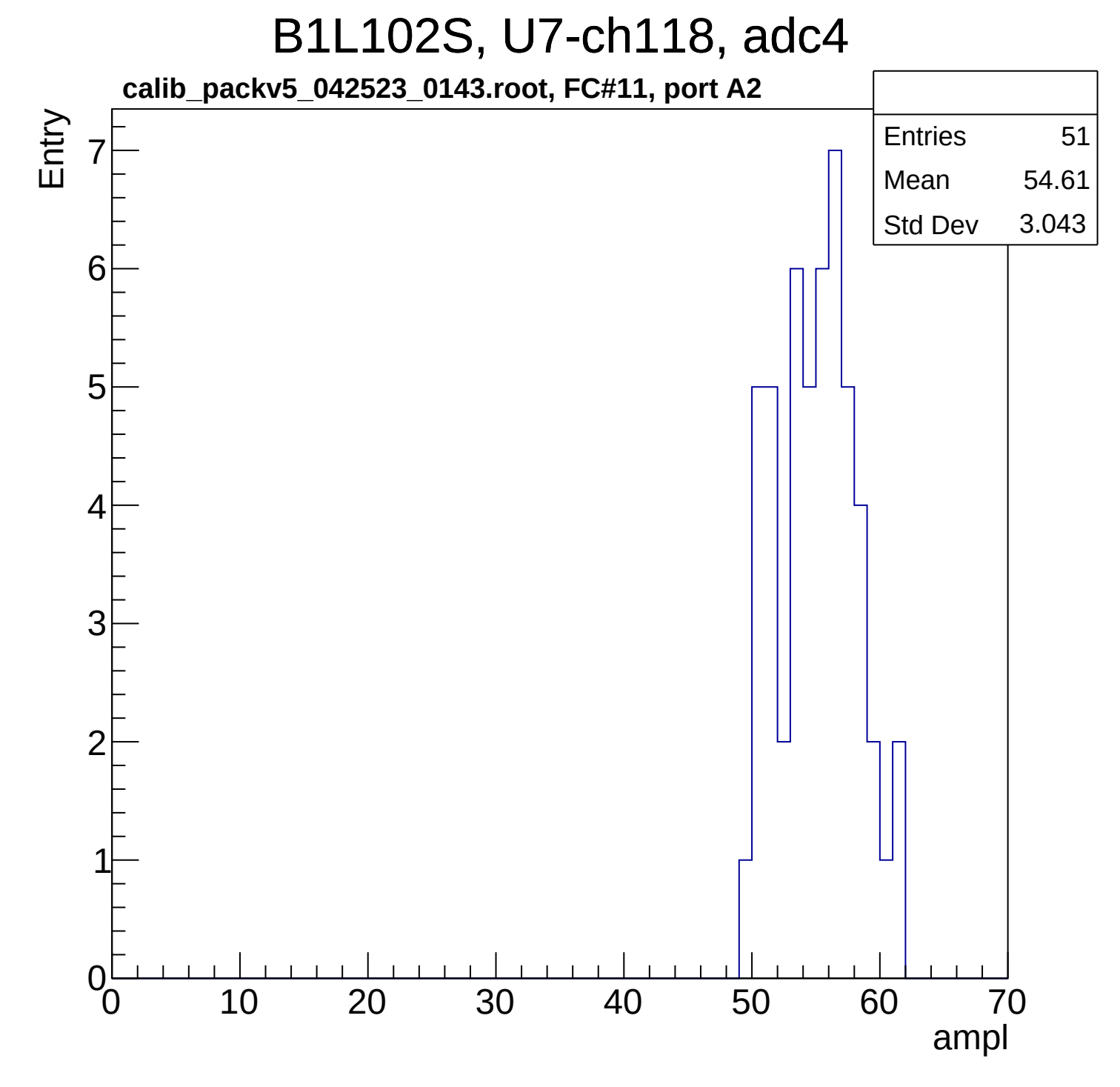
B1L102S, U7-ch118, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 51
Mean 54.61
Std Dev 3.043
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
30
40
50
60
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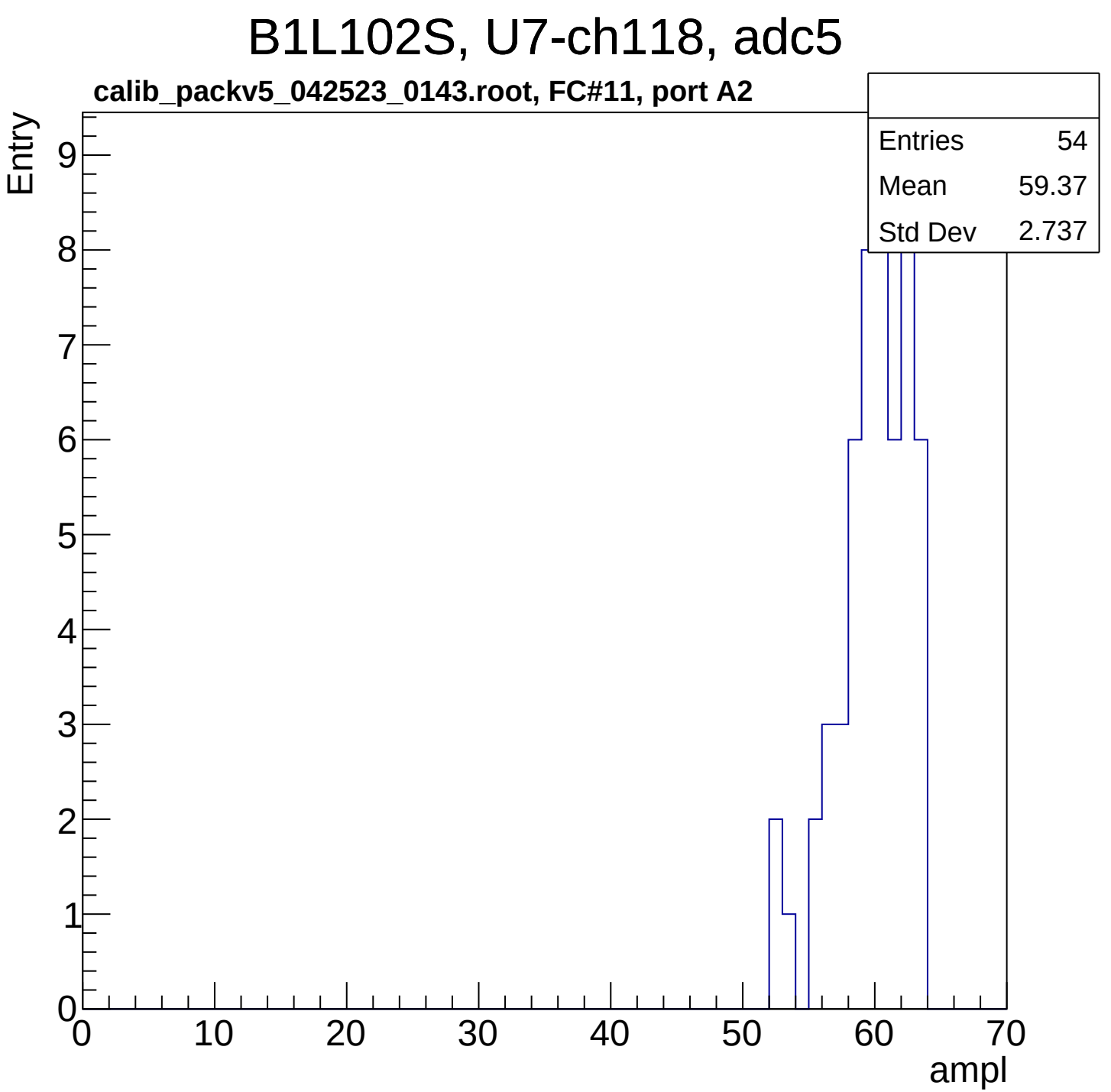
B1L102S, U7-ch118, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 54
Mean 59.37
Std Dev 2.737
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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40
50
60
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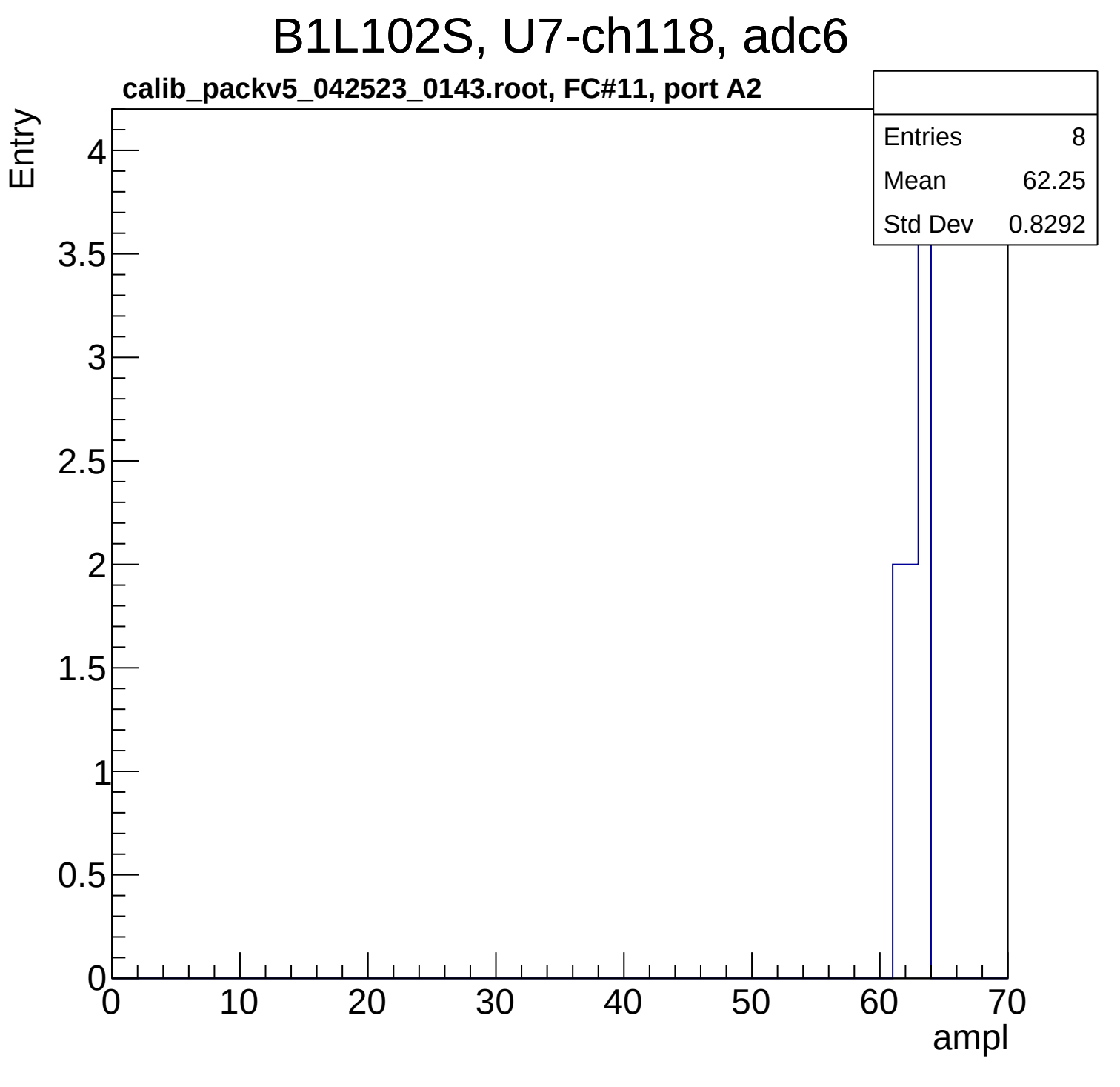
B1L102S, U7-ch118, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 8
Mean 62.25
Std Dev 0.8292
Entry
ampl
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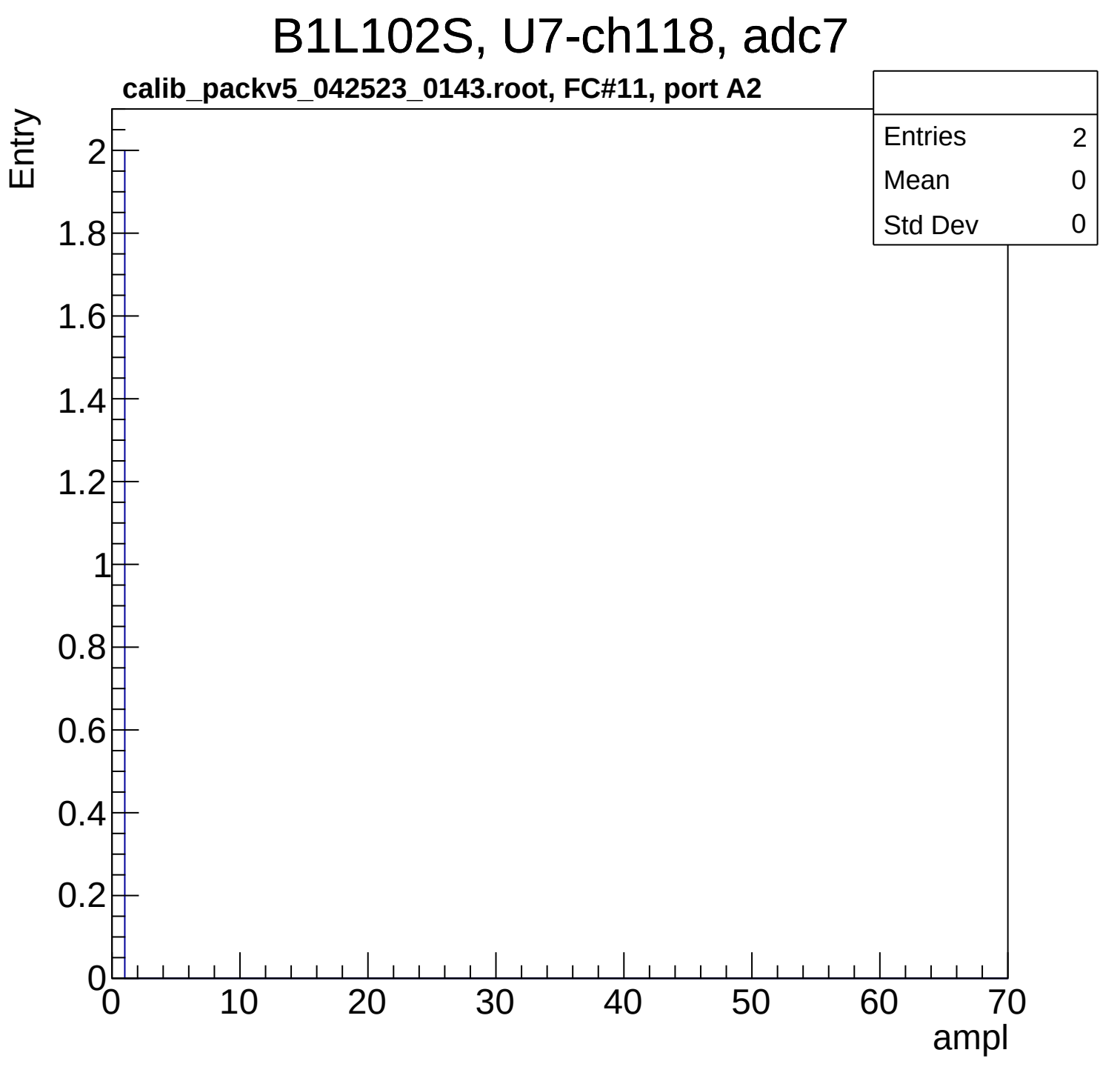
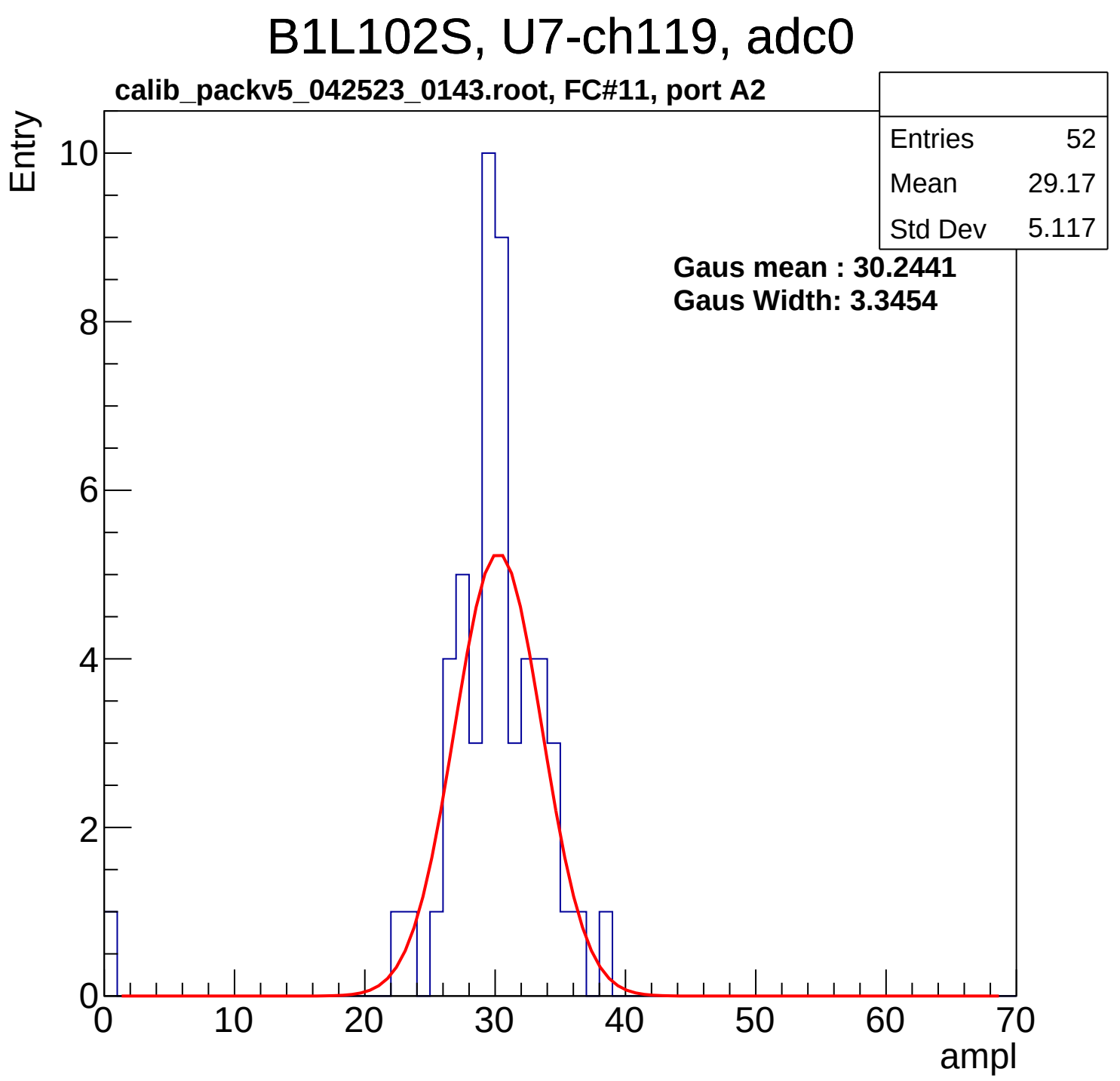
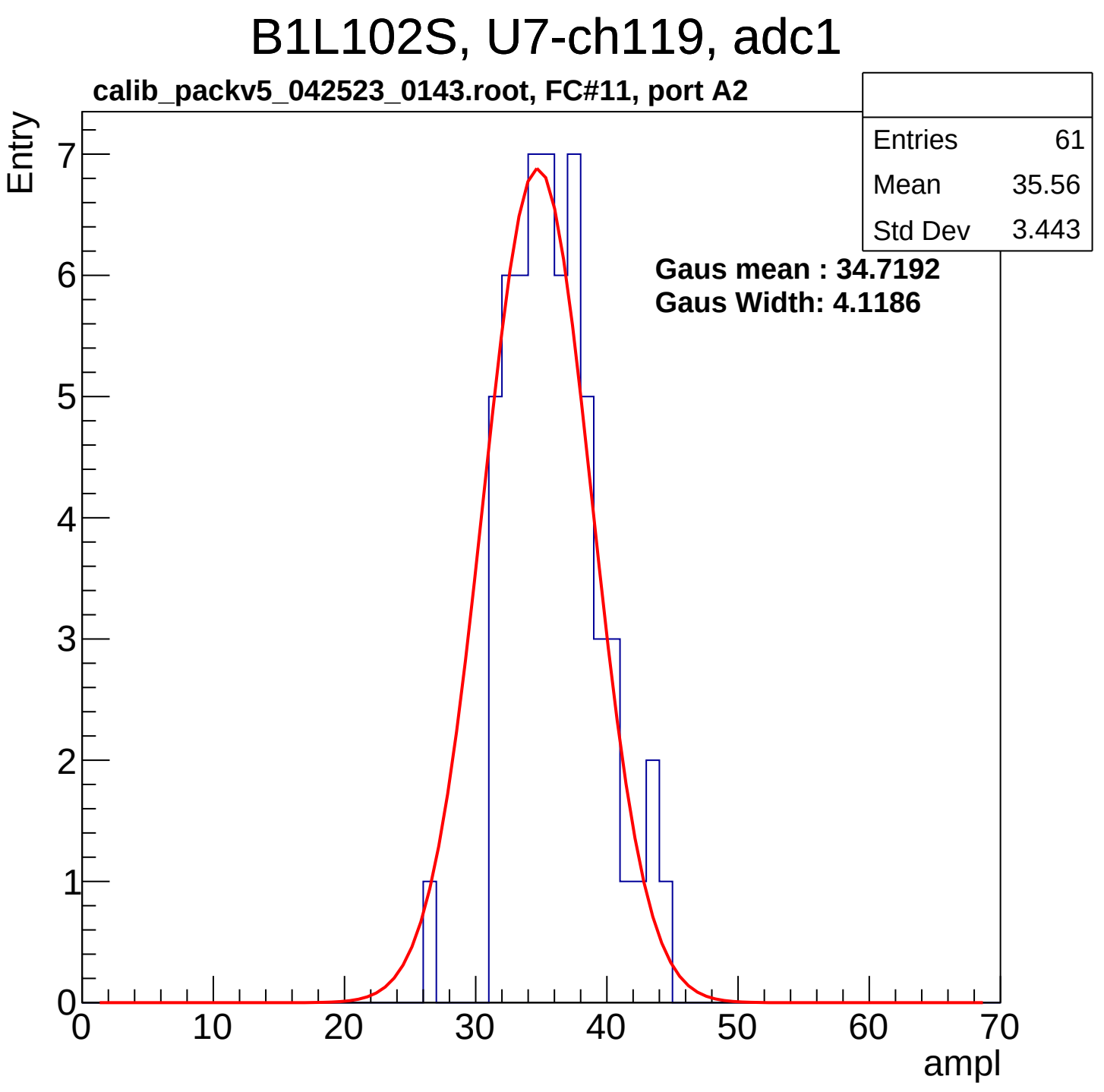
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L102S, U7-ch118, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 2
Mean 0
Std Dev 0
Entry
2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U7-ch119, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 52
Mean 29.17
Std Dev 5.117
Gaus mean : 30.2441
Gaus Width: 3.3454
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L102S, U7-ch119, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 61
Mean 35.56
Std Dev 3.443
Gaus mean : 34.7192
Gaus Width: 4.1186
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
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40
50
60
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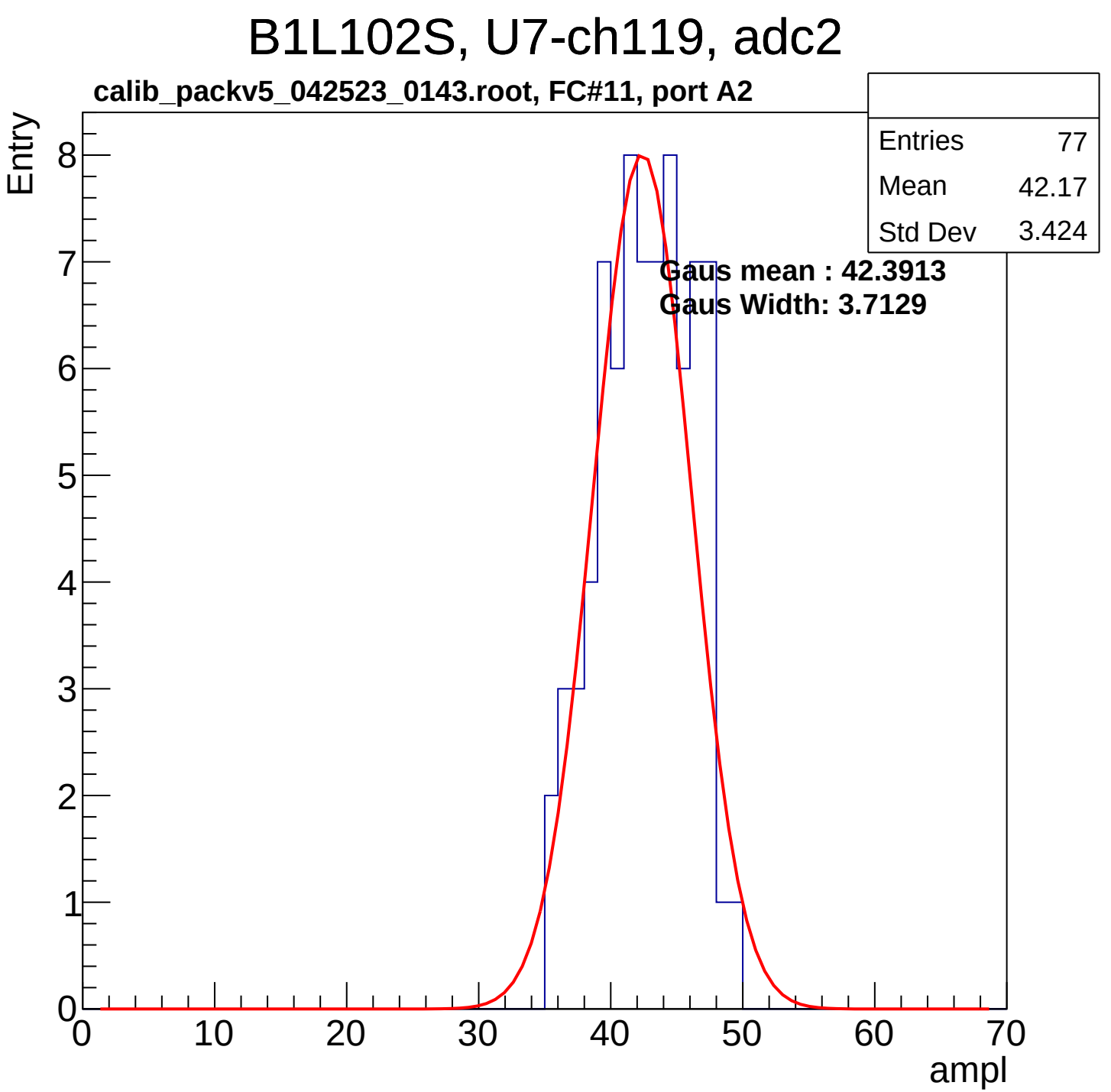
B1L102S, U7-ch119, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 77
Mean 42.17
Std Dev 3.424
Gaus mean : 42.3913
Gaus Width: 3.7129
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
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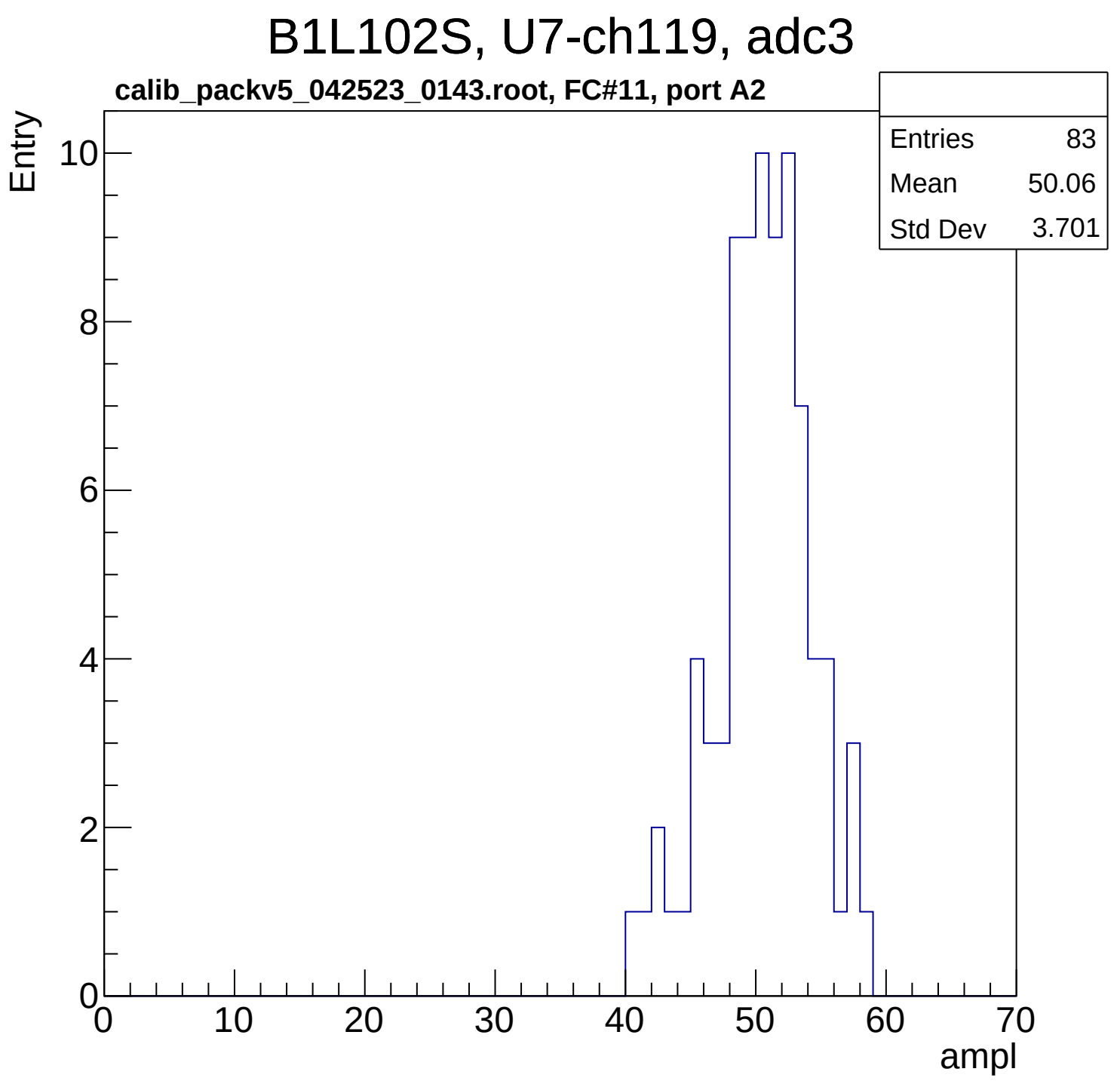
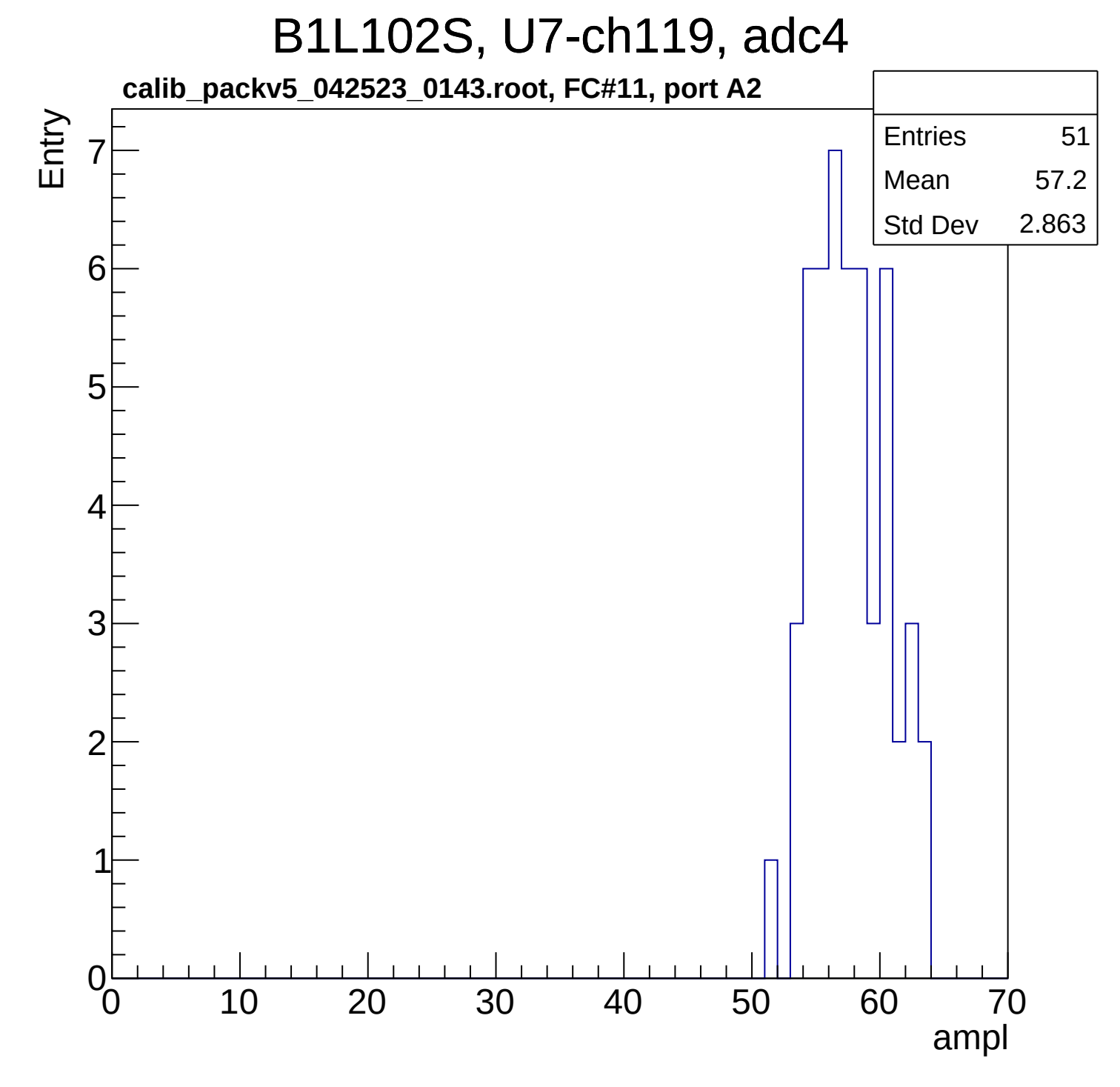
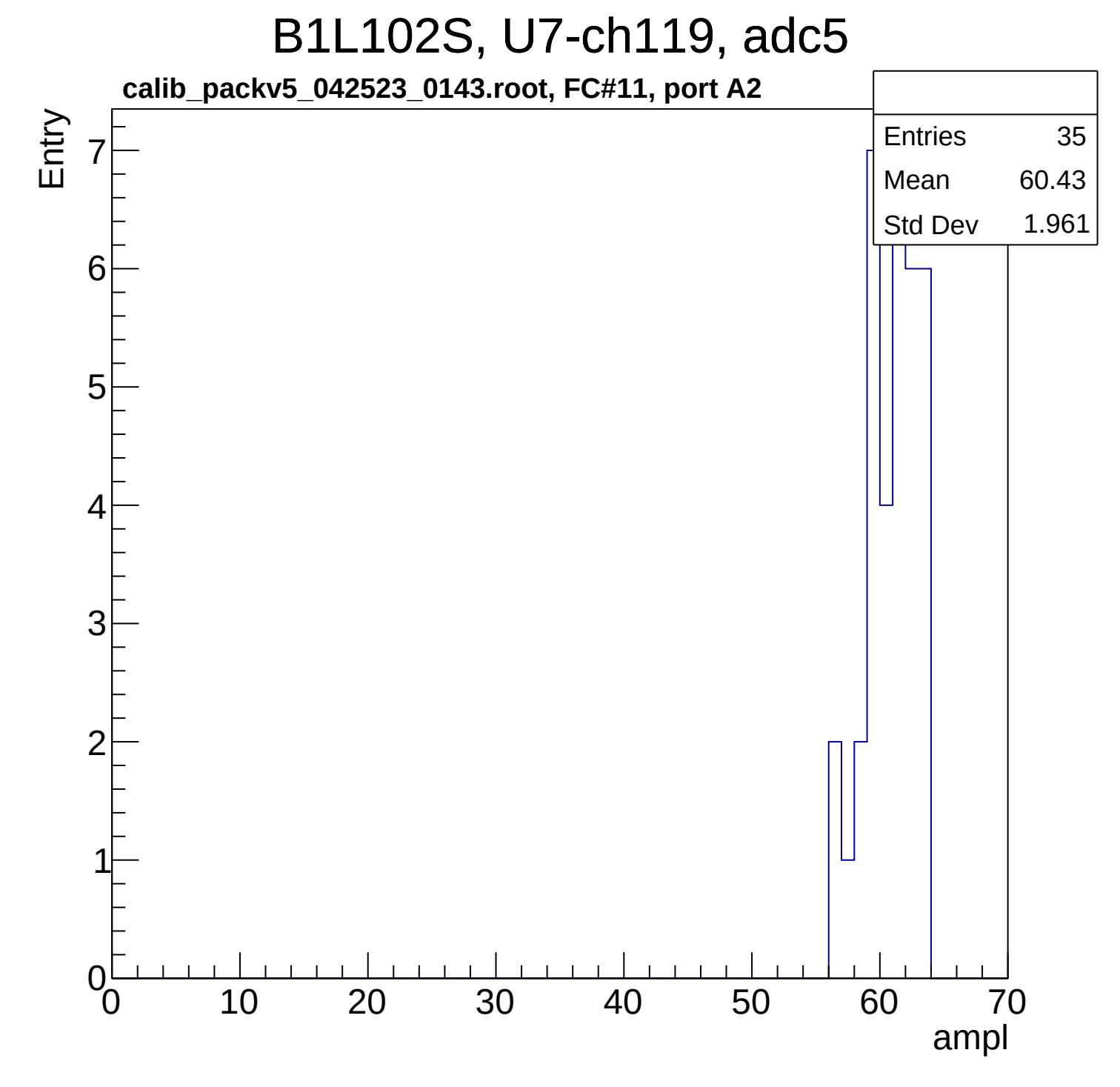
40
50
60
70


B1L102S, U7-ch119, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 83
Mean 50.06
Std Dev 3.701
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L102S, U7-ch119, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 51
Mean 57.2
Std Dev 2.863
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L102S, U7-ch119, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 35
Mean 60.43
Std Dev 1.961
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
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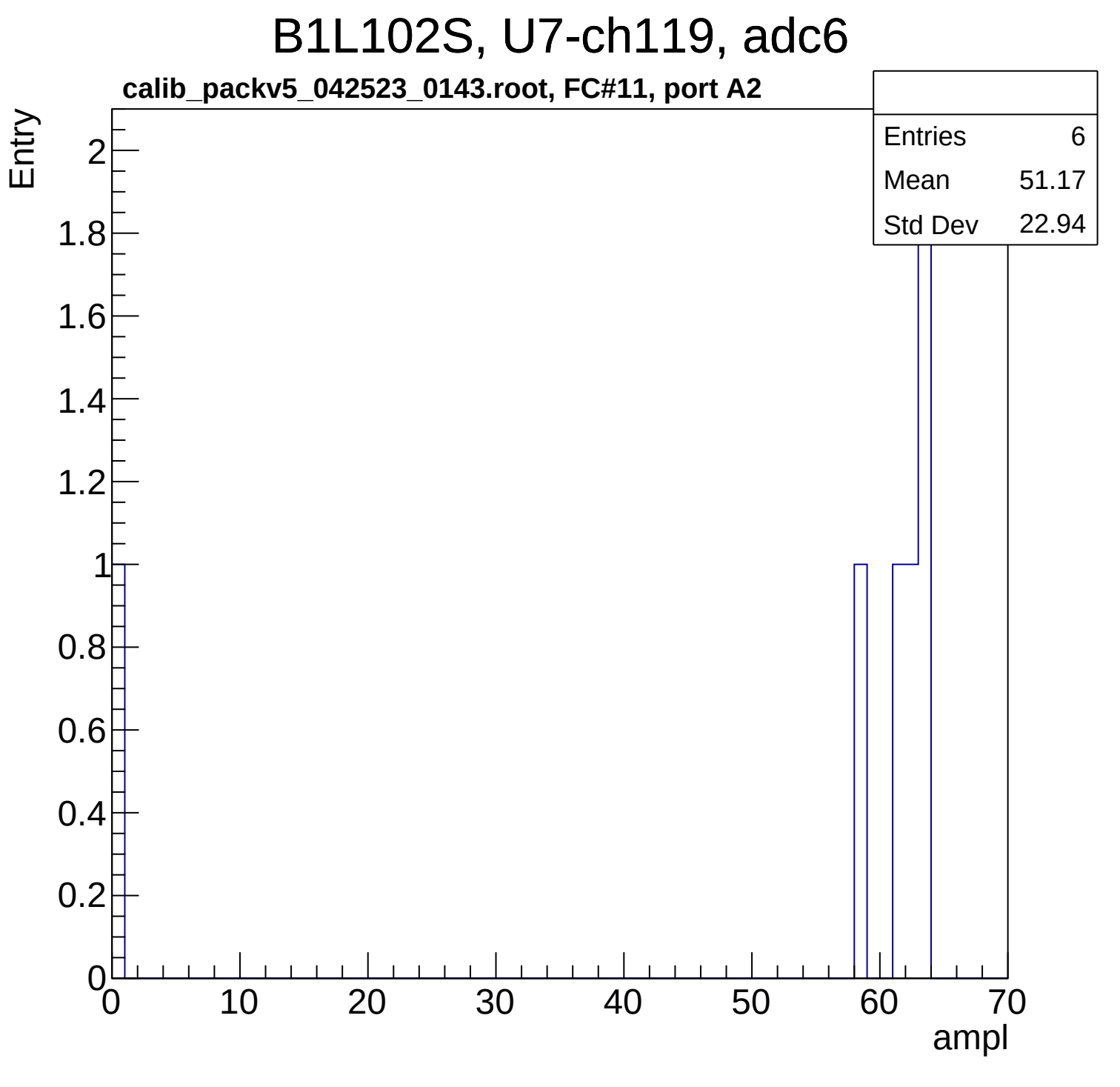
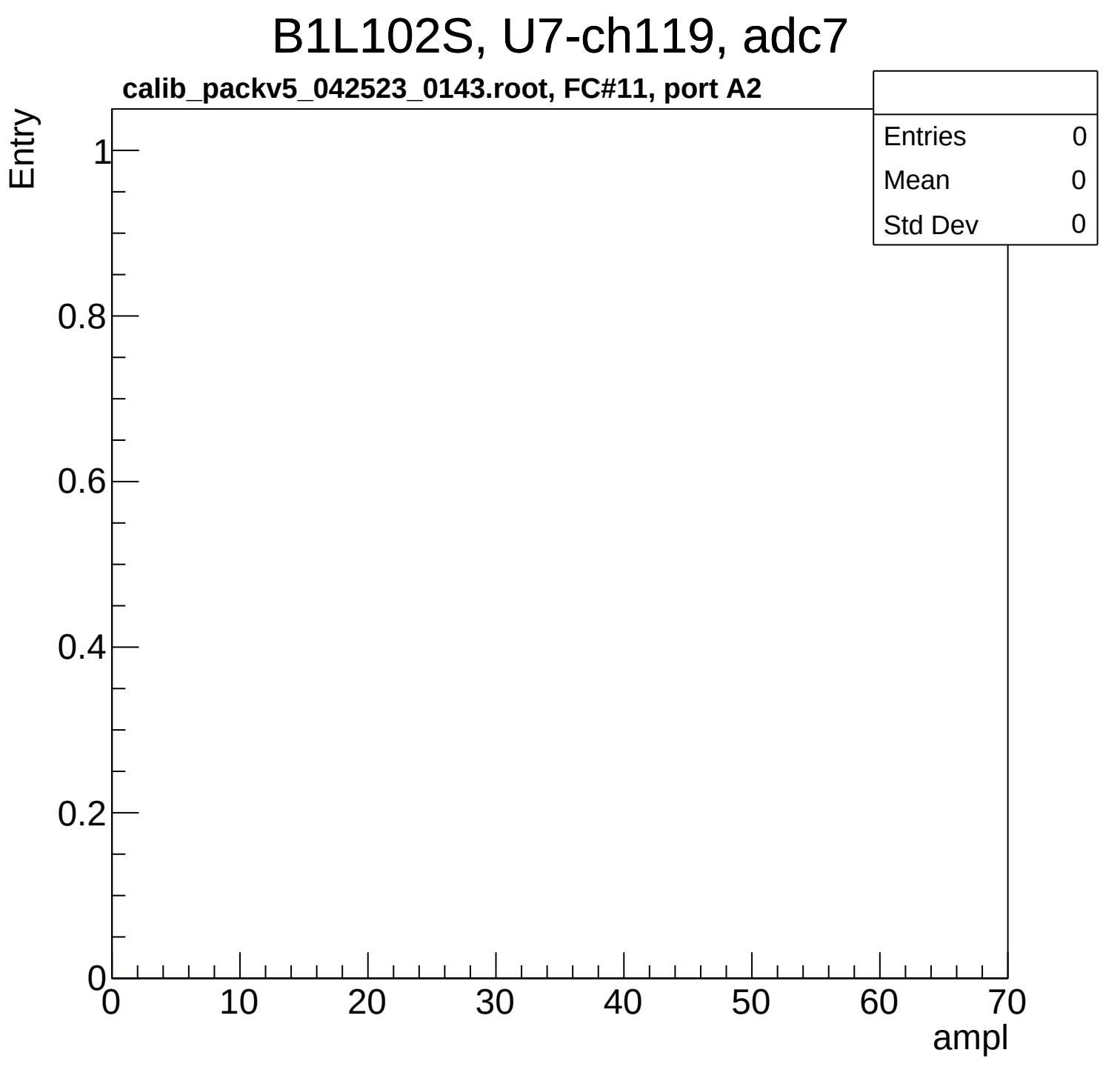
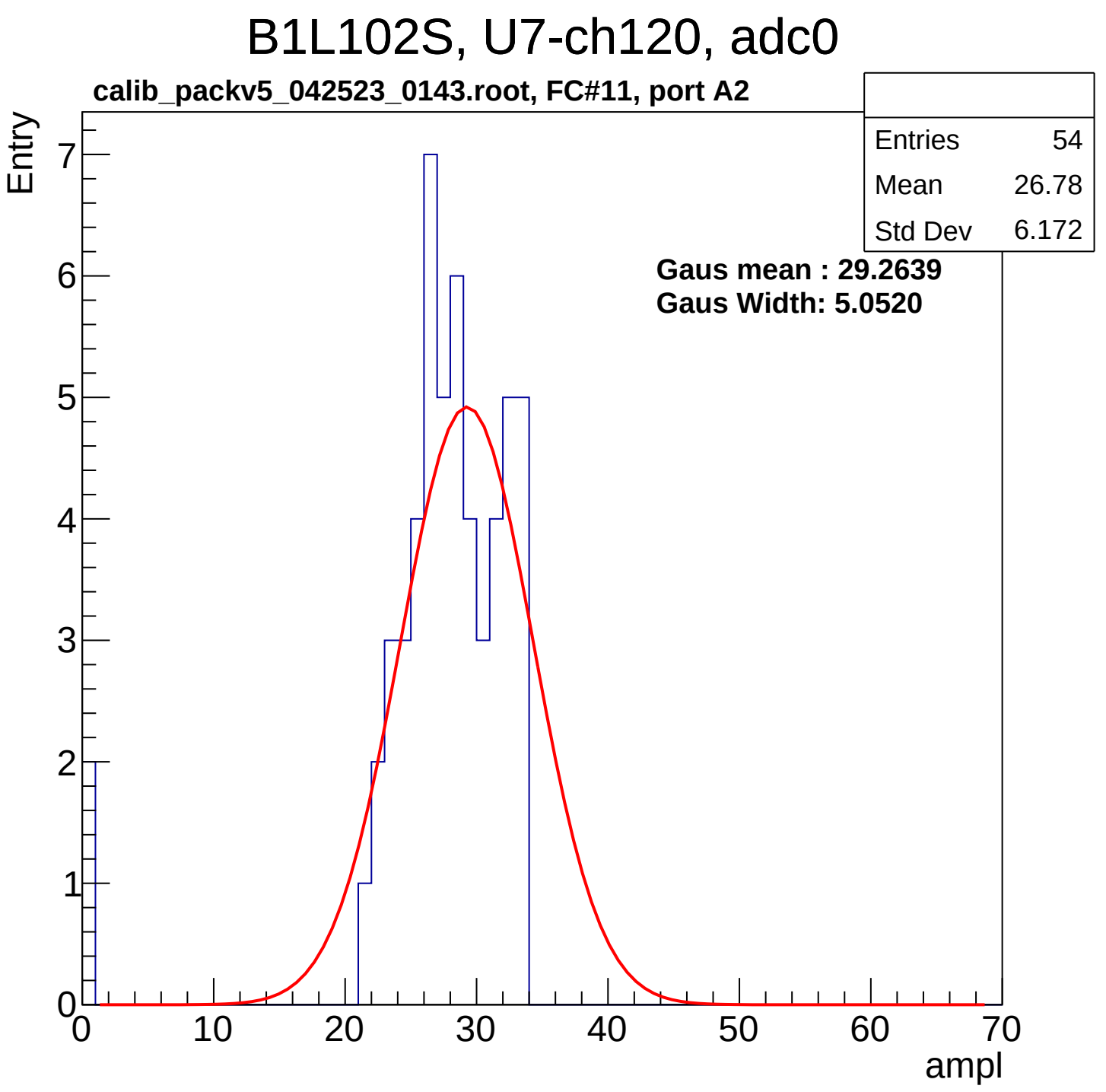
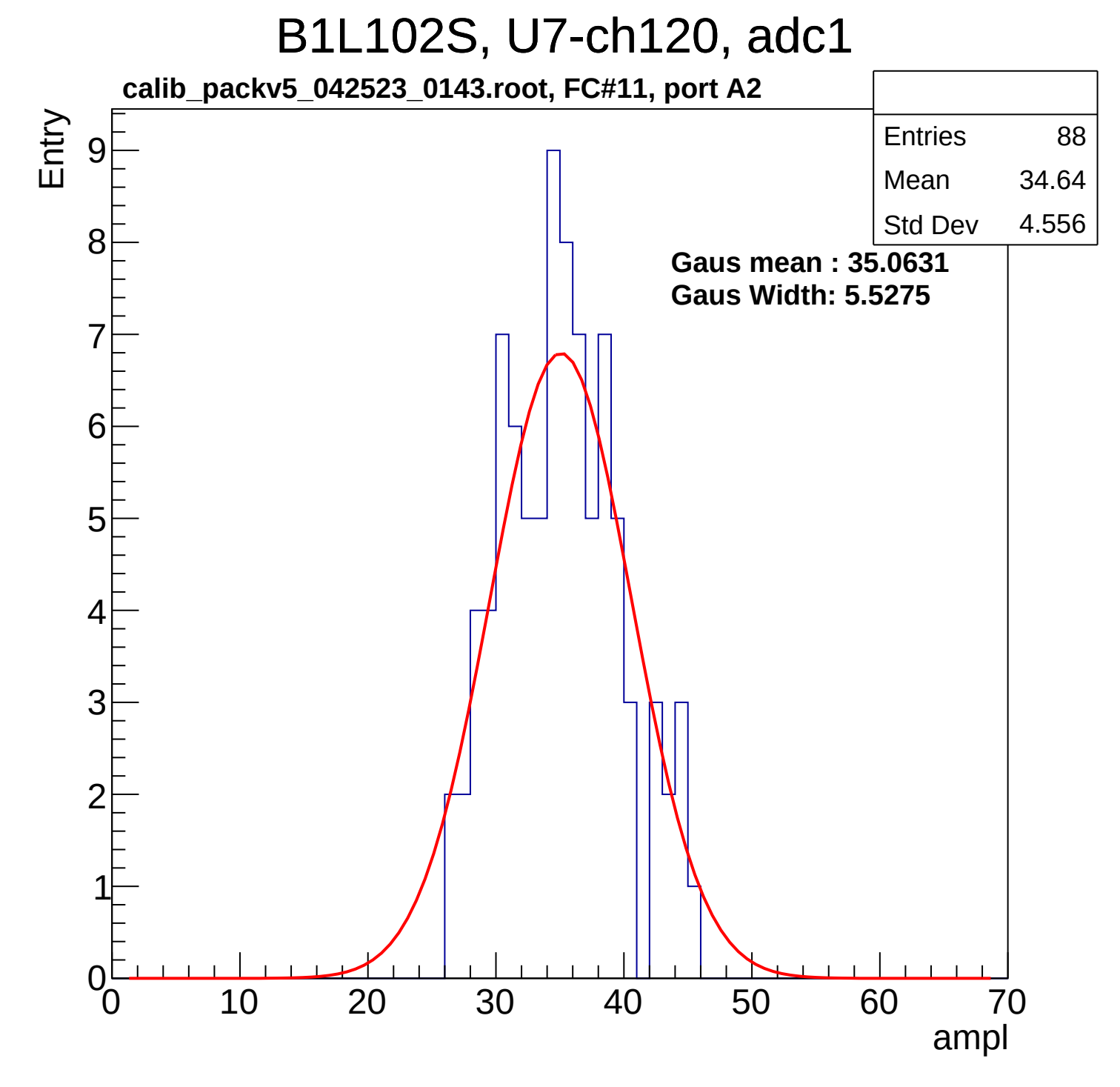
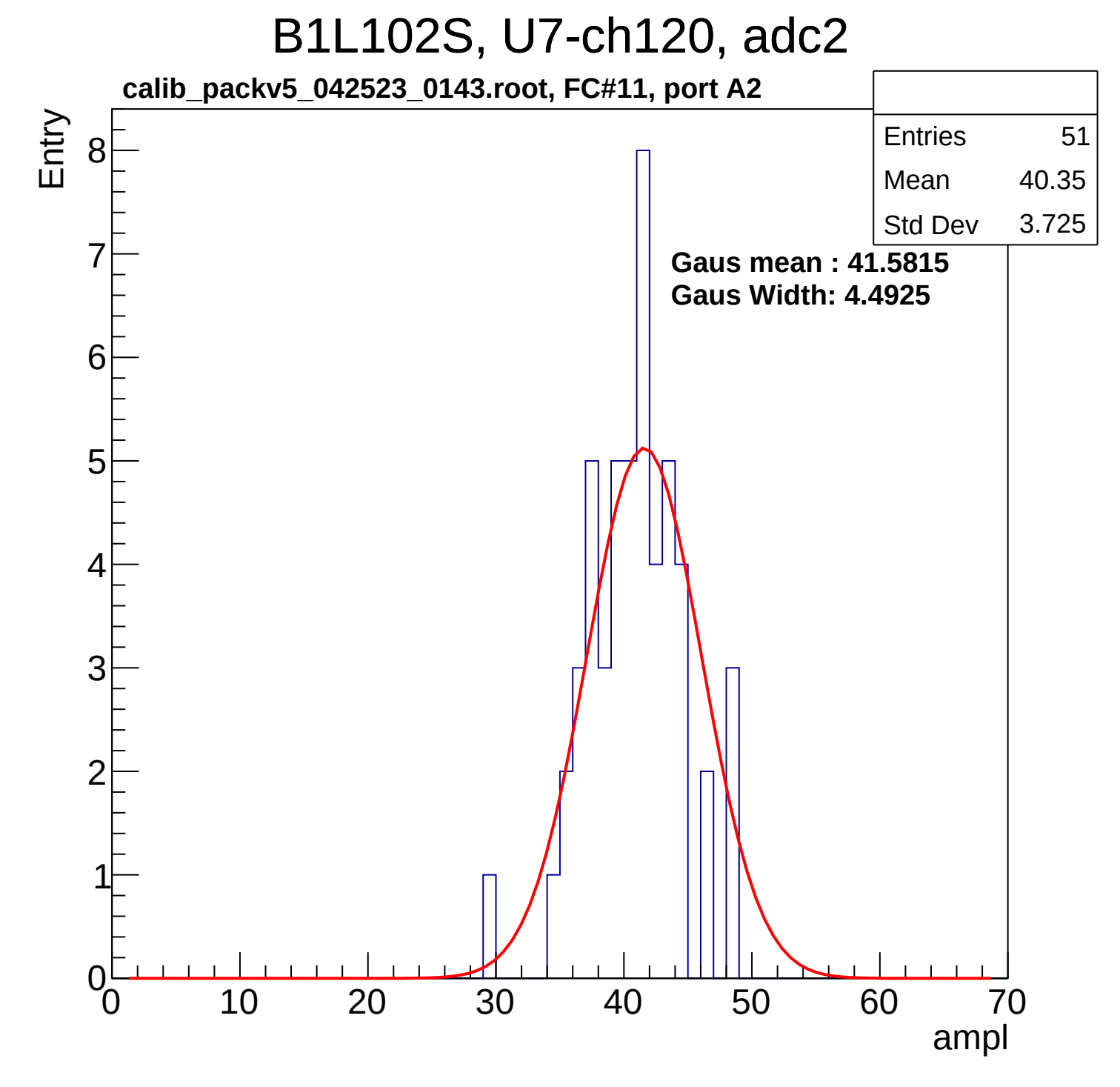
40
50
60
70

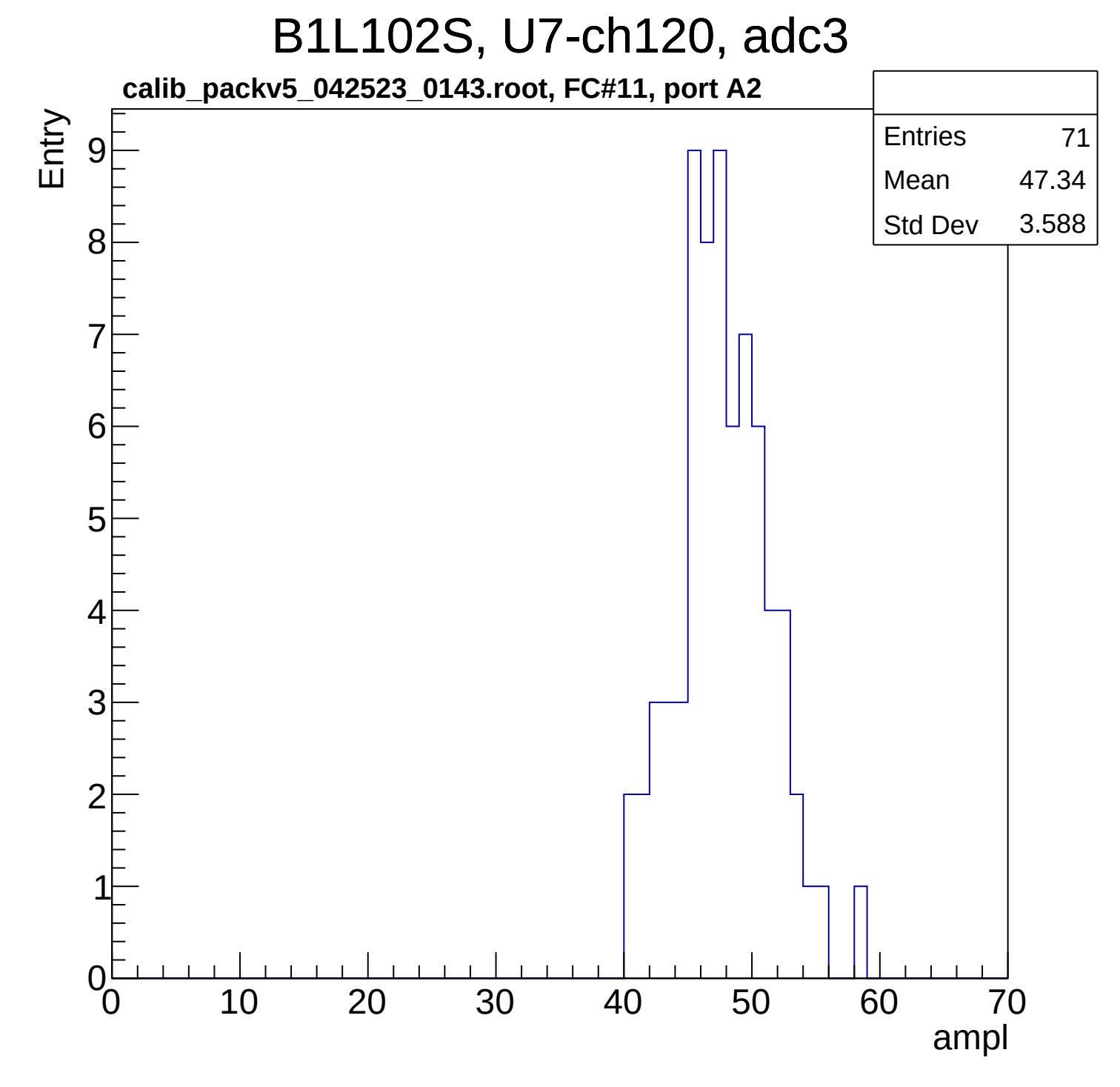

B1L102S, U7-ch119, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 6
Mean 51.17
Std Dev 22.94
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L102S, U7-ch119, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U7-ch120, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 54
Mean 26.78
Std Dev 6.172
Gaus mean : 29.2639
Gaus Width: 5.0520
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L102S, U7-ch120, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 88
Mean 34.64
Std Dev 4.556
Gaus mean : 35.0631
Gaus Width: 5.5275
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L102S, U7-ch120, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 51
Mean 40.35
Std Dev 3.725
Gaus mean : 41.5815
Gaus Width: 4.4925
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L102S, U7-ch120, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 71
Mean 47.34
Std Dev 3.588
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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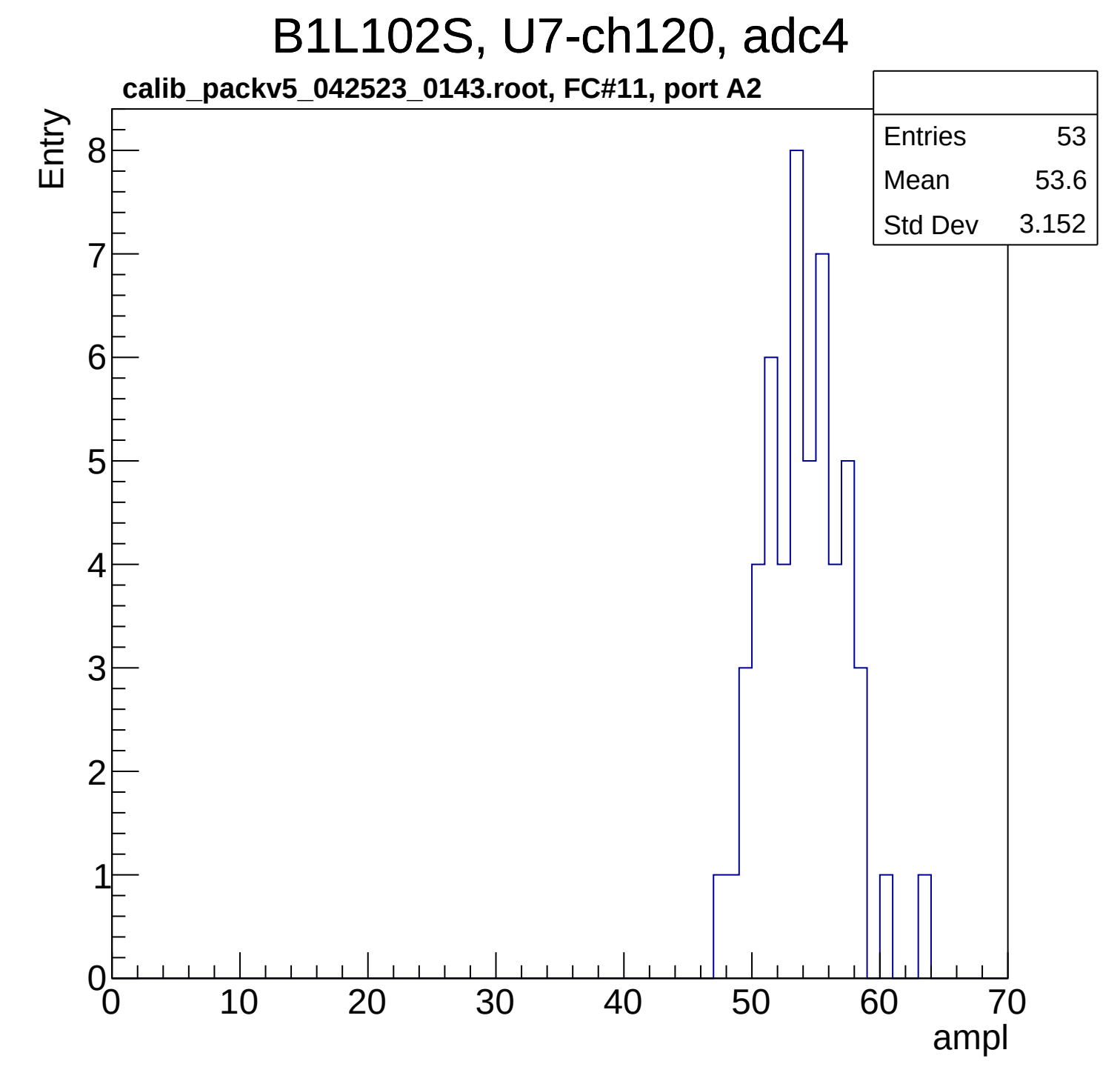
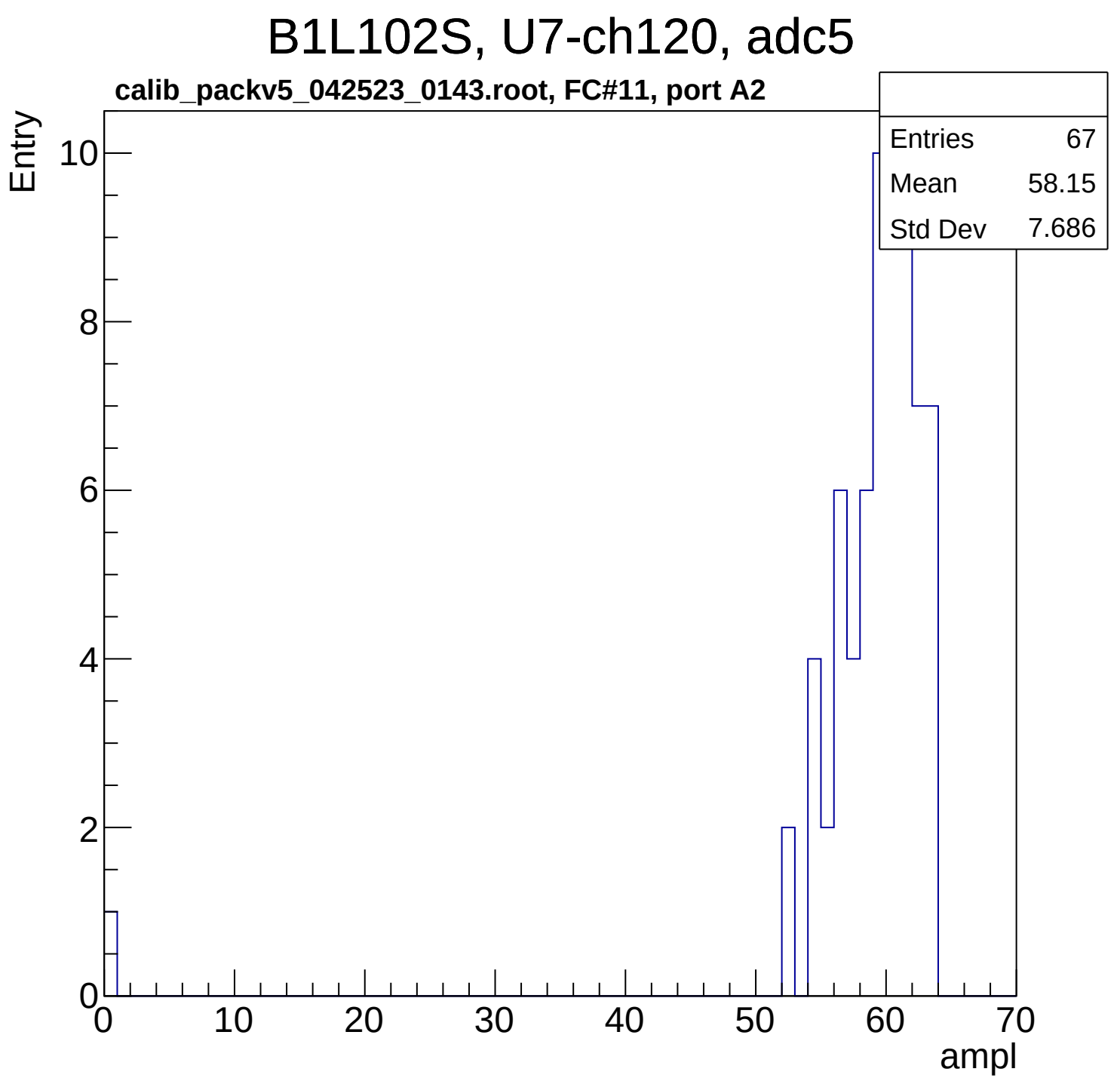
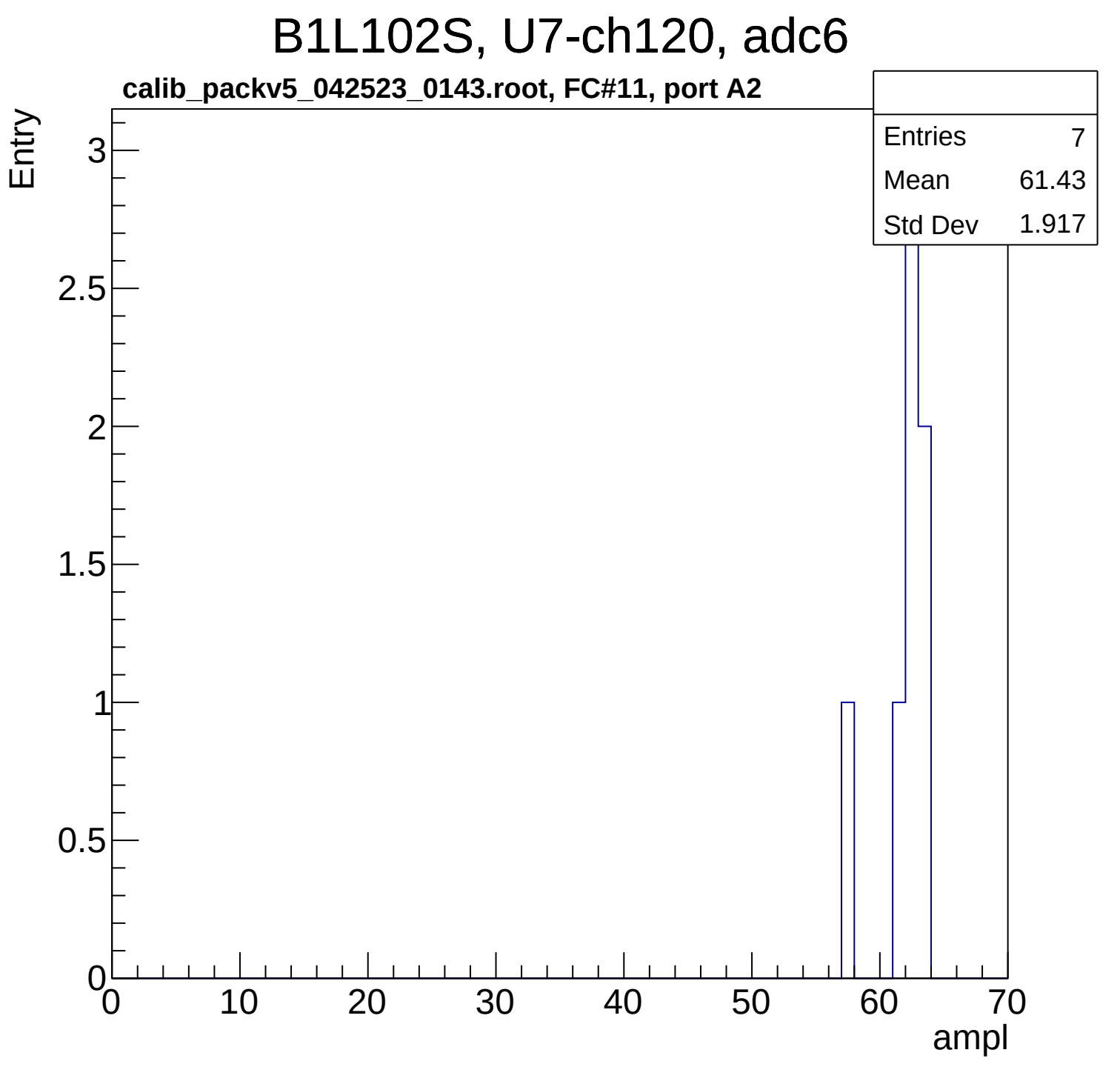
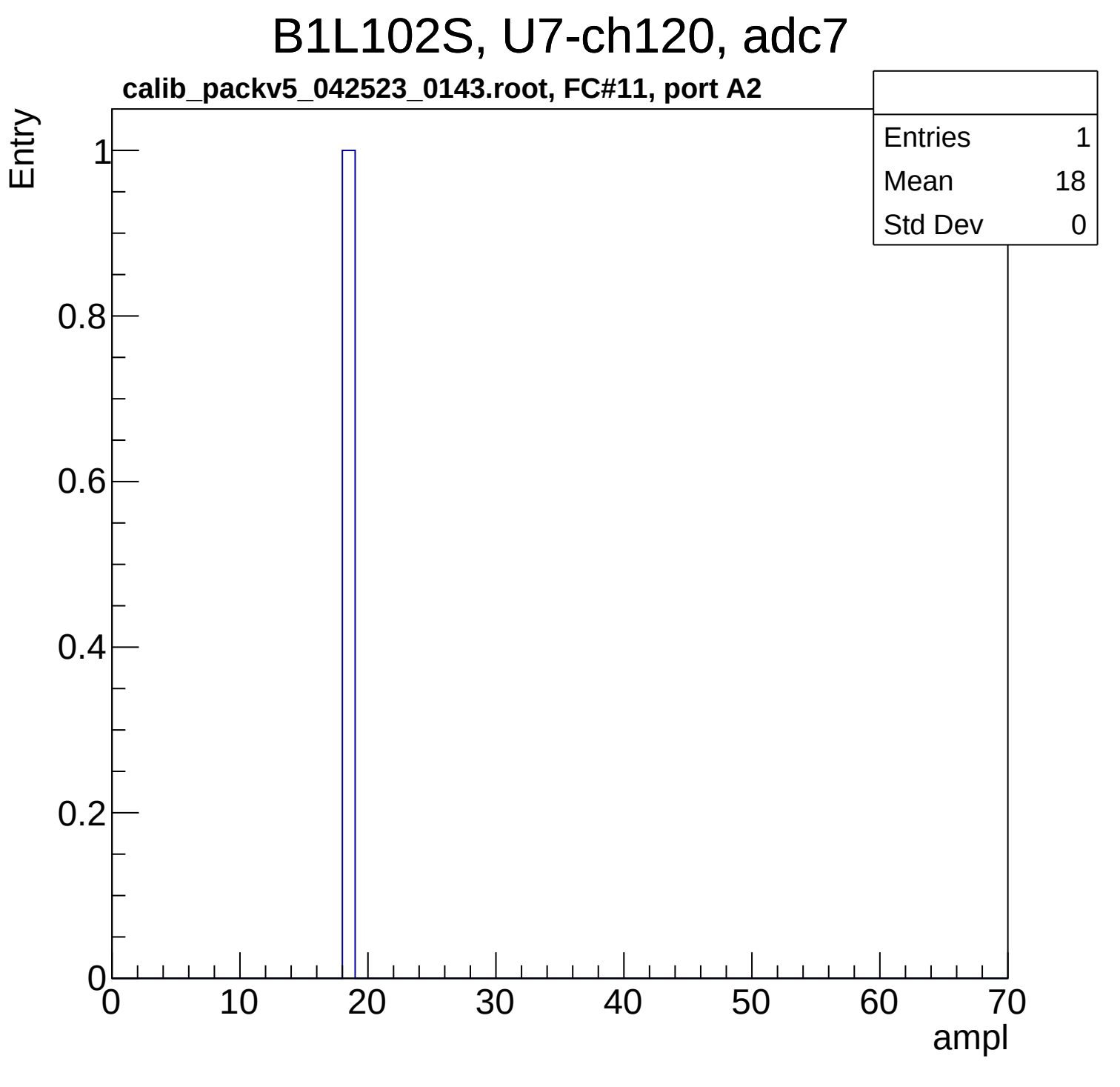
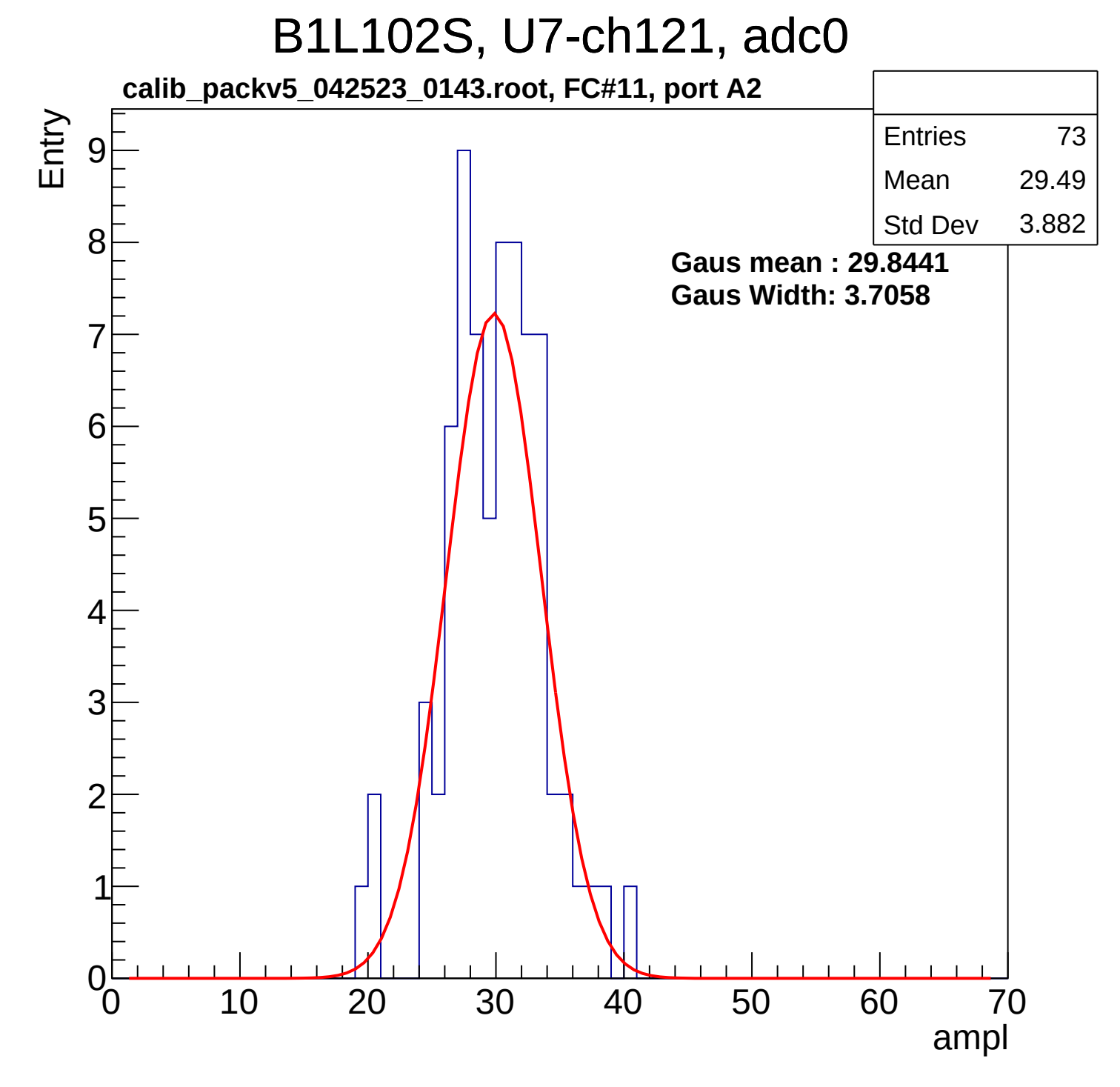
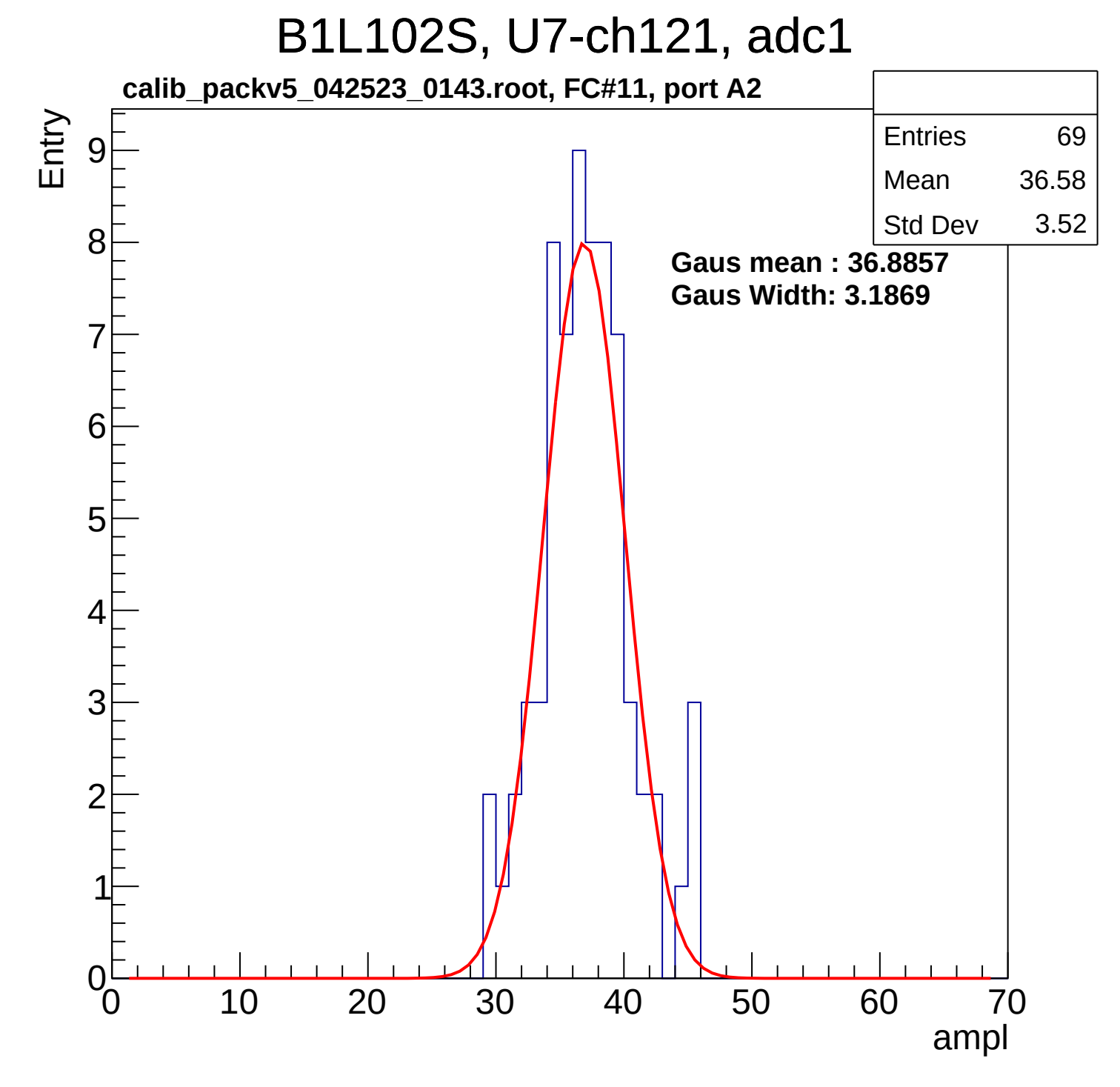

B1L102S, U7-ch120, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 53
Mean 53.6
Std Dev 3.152
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

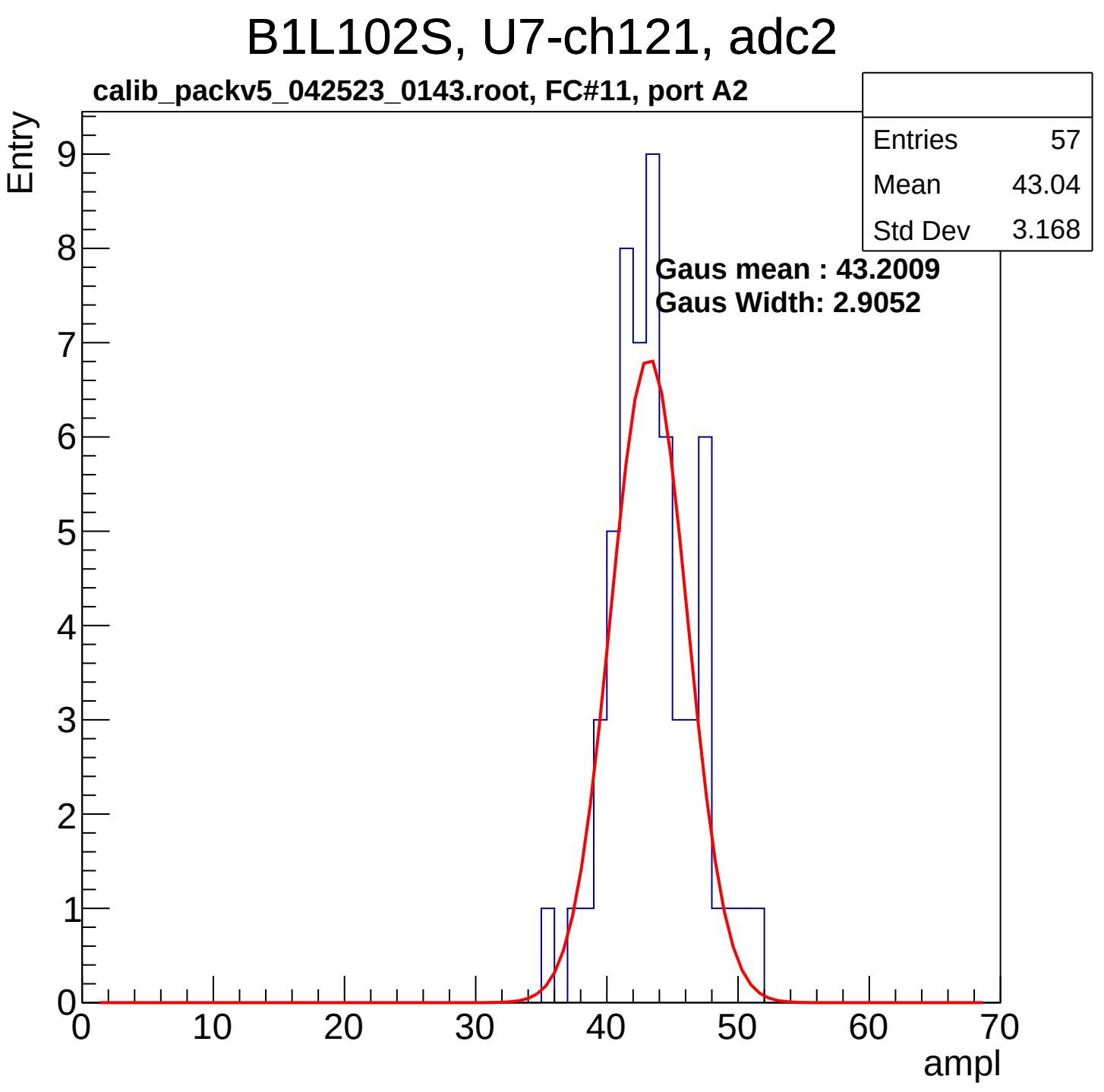

B1L102S, U7-ch120, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 67
Mean 58.15
Std Dev 7.686
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

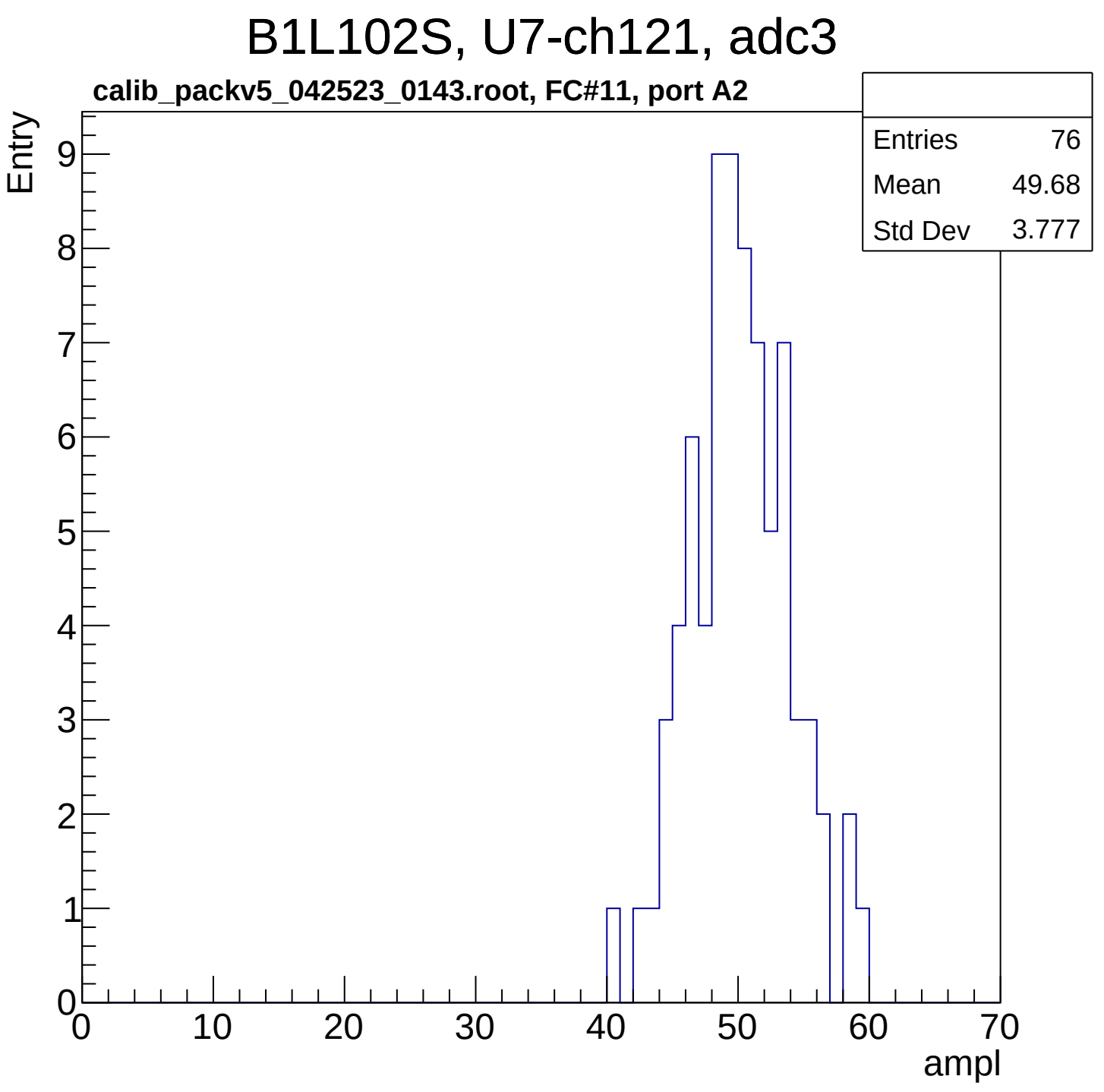

B1L102S, U7-ch120, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 7
Mean 61.43
Std Dev 1.917
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L102S, U7-ch120, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 1
Mean 18
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U7-ch121, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 73
Mean 29.49
Std Dev 3.882
Gaus mean : 29.8441
Gaus Width: 3.7058
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L102S, U7-ch121, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 69
Mean 36.58
Std Dev 3.52
Gaus mean : 36.8857
Gaus Width: 3.1869
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L102S, U7-ch121, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 57
Mean 43.04
Std Dev 3.168
Gaus mean : 43.2009
Gaus Width: 2.9052
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L102S, U7-ch121, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 76
Mean 49.68
Std Dev 3.777
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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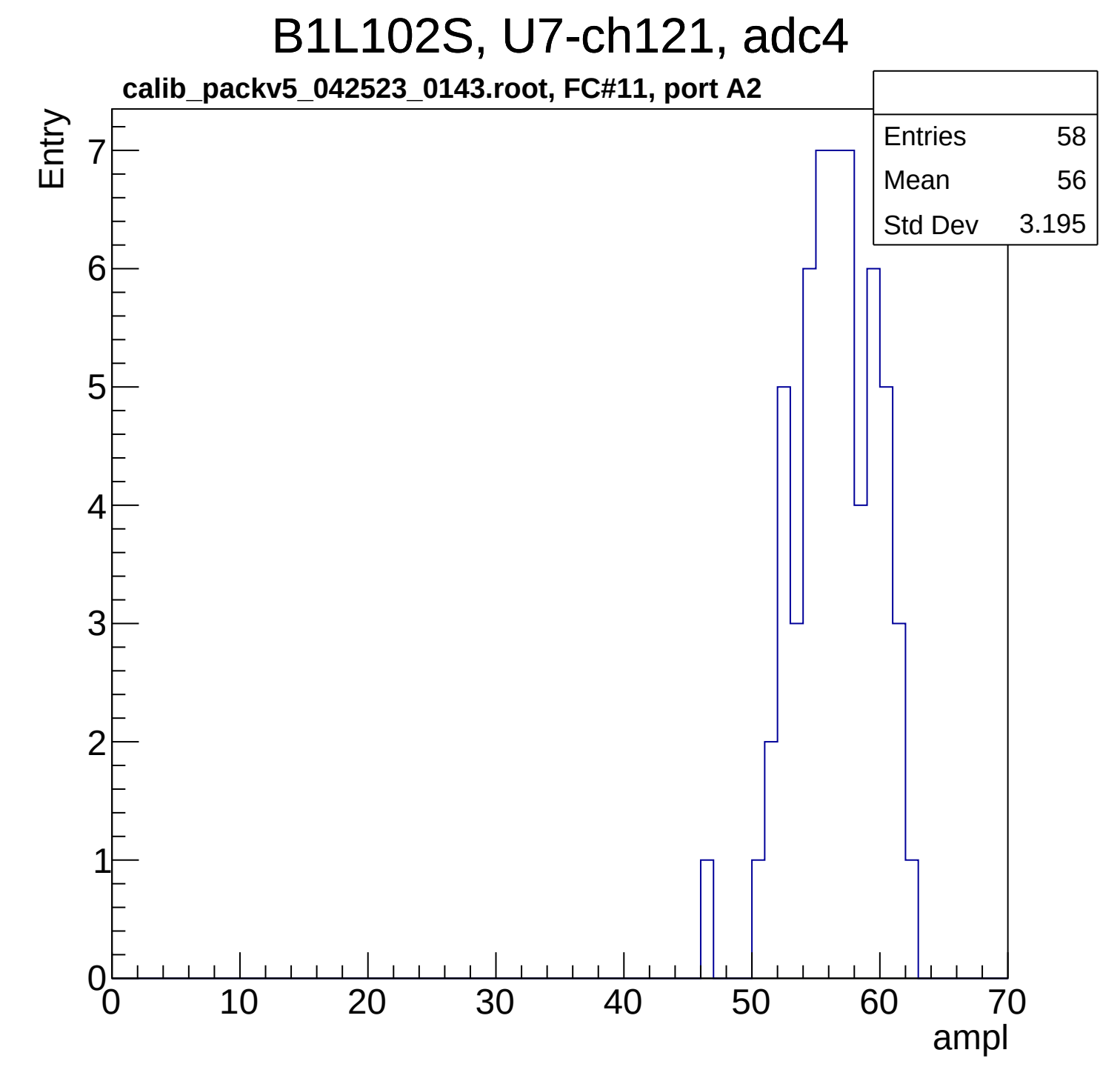
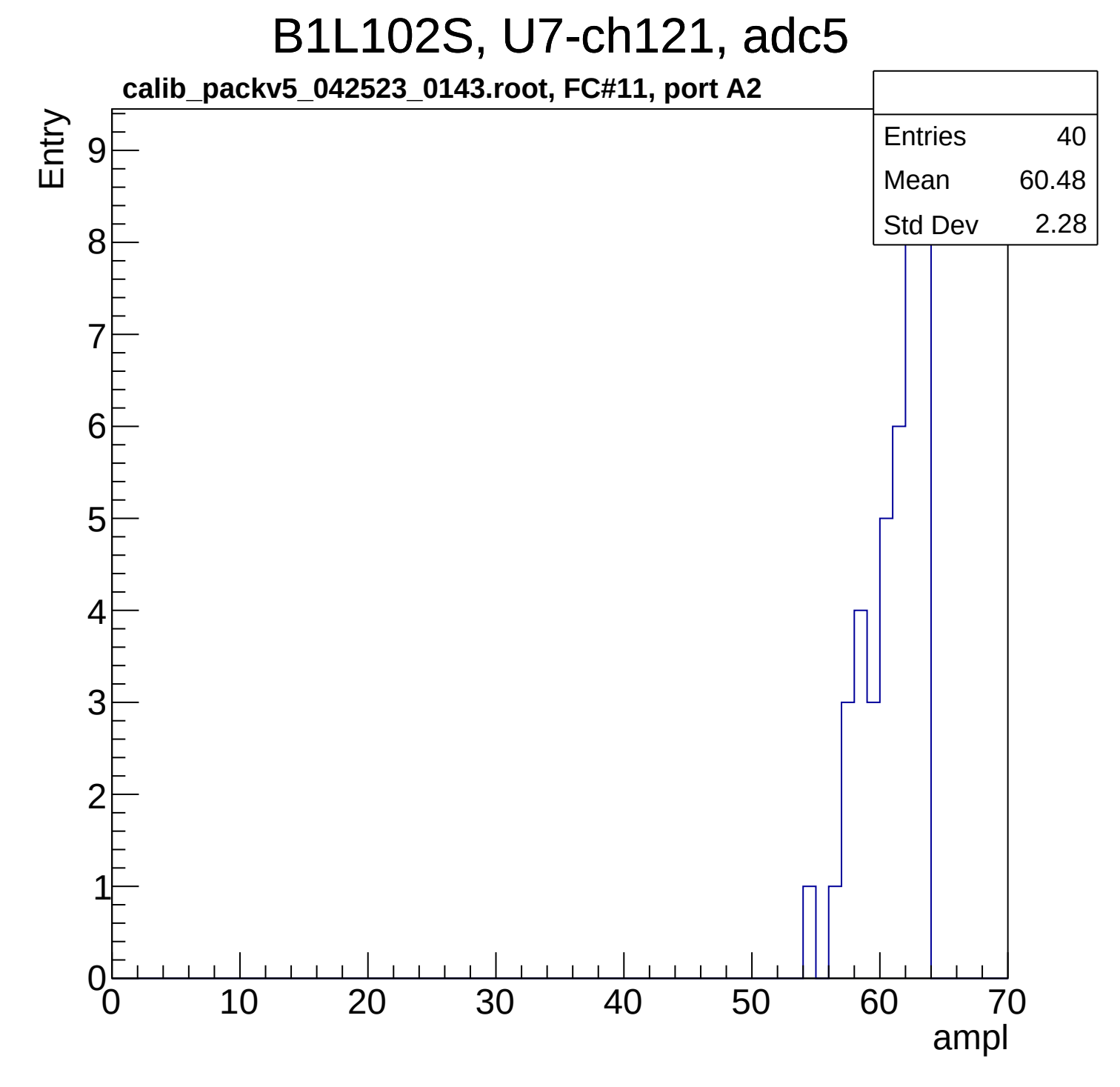
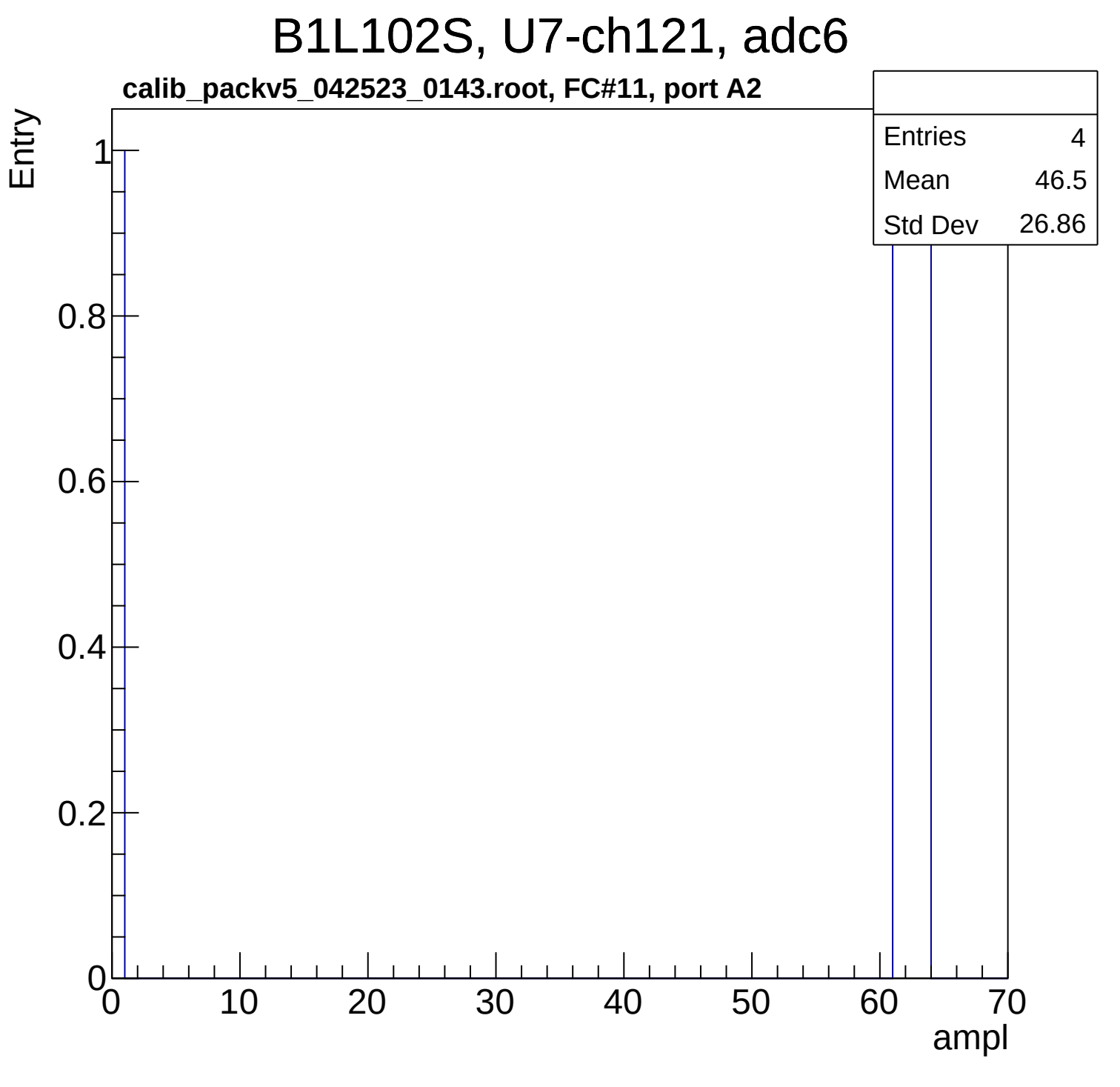
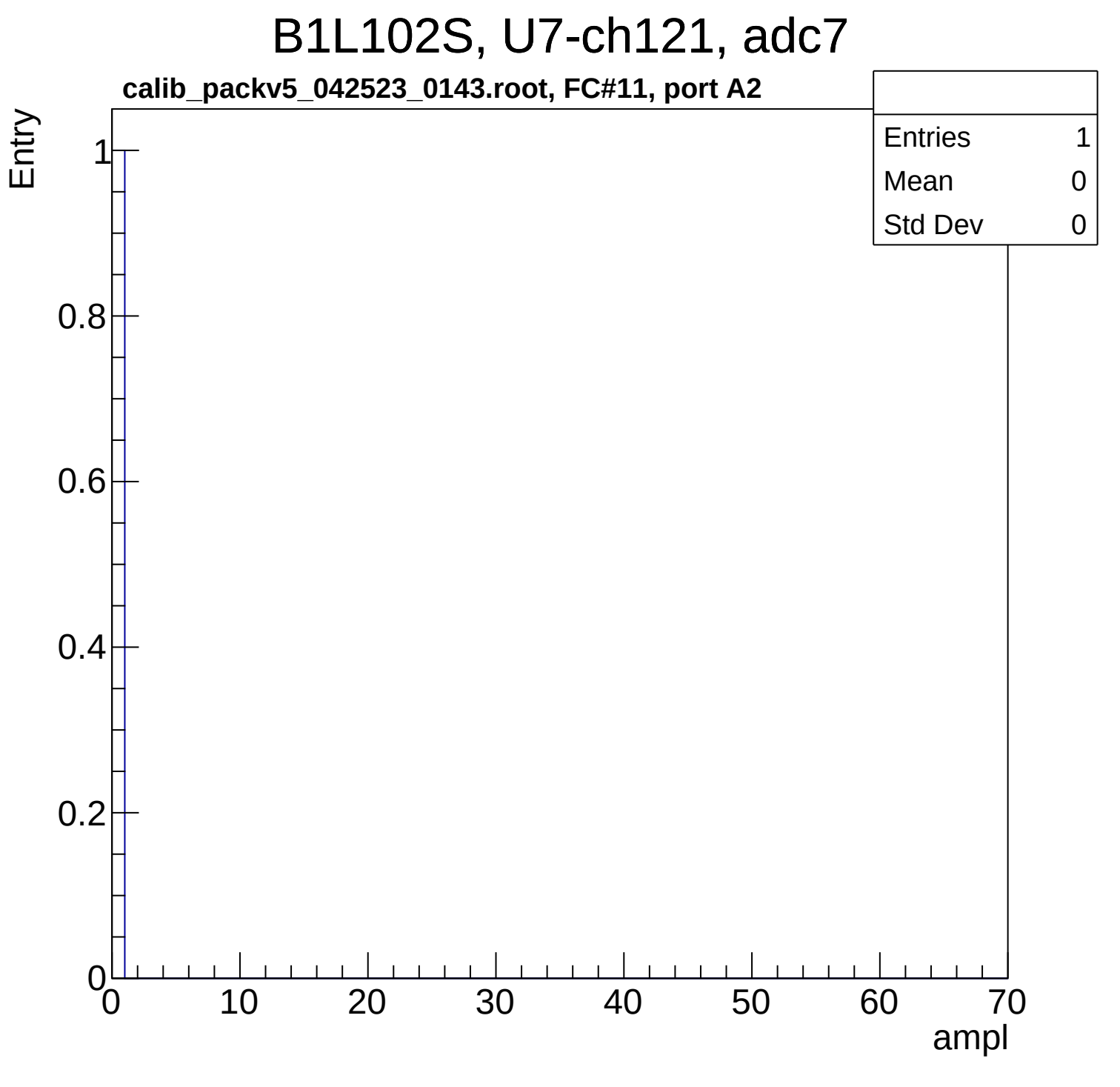
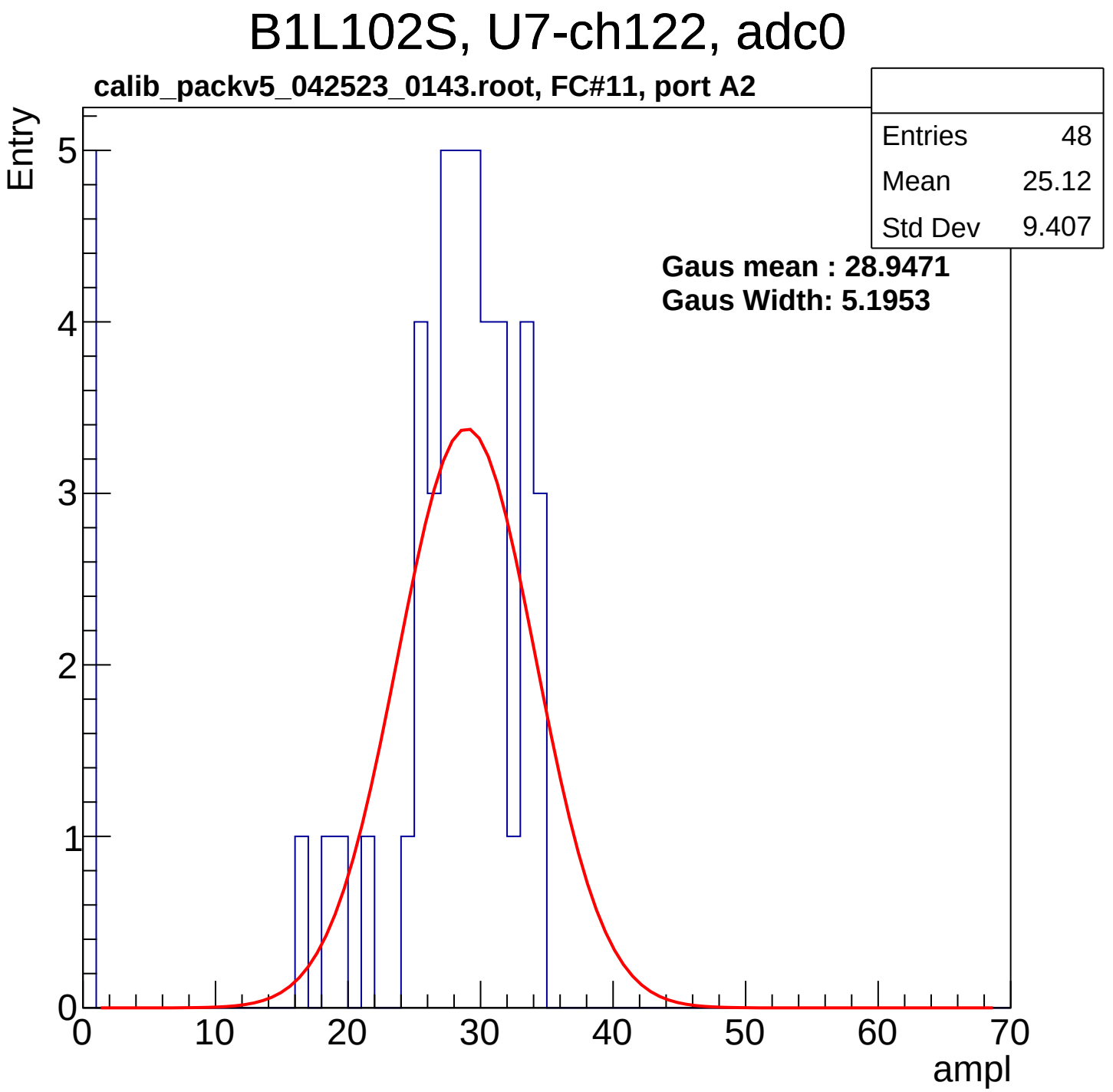
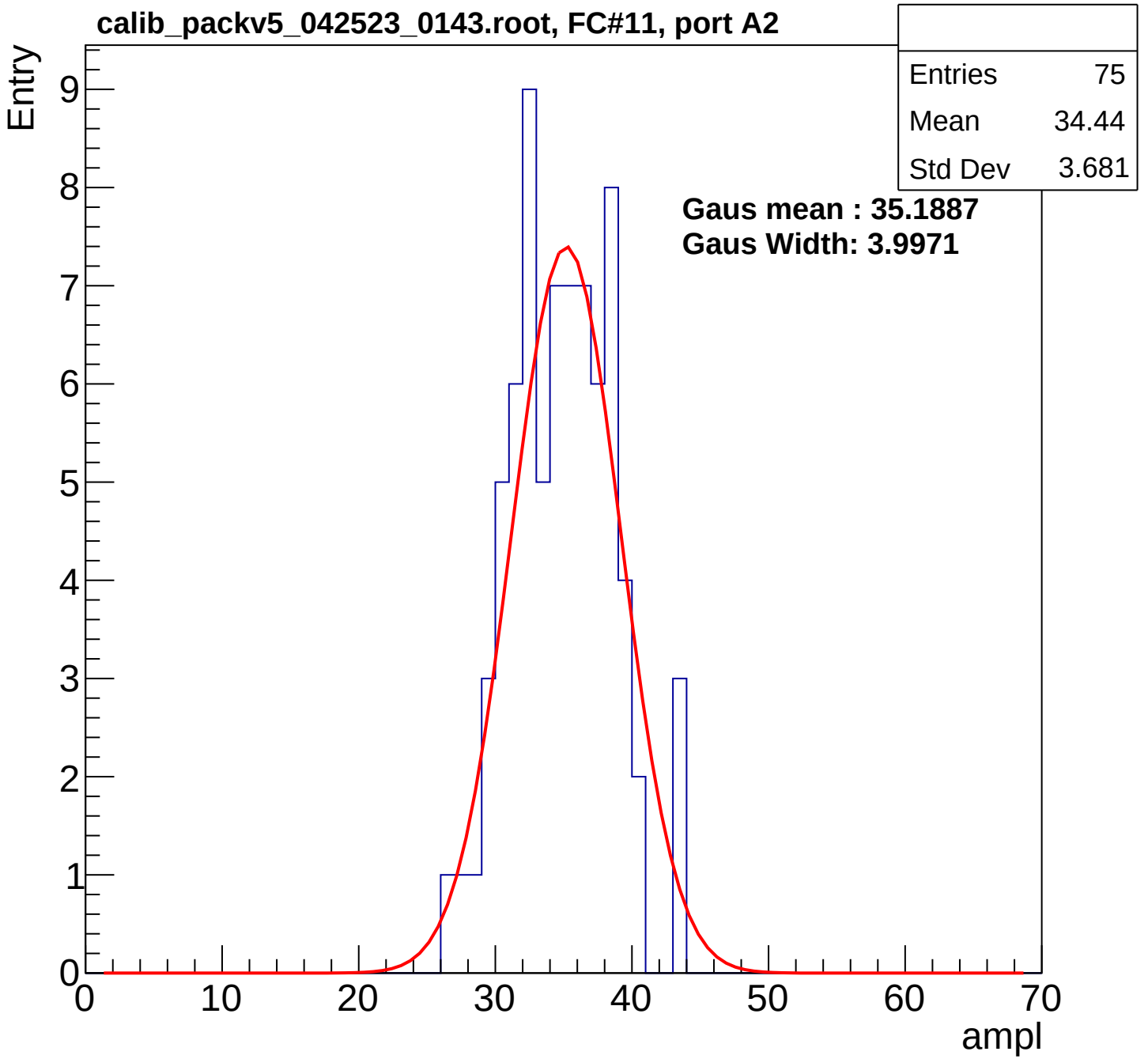

B1L102S, U7-ch121, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 58
Mean 56
Std Dev 3.195
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

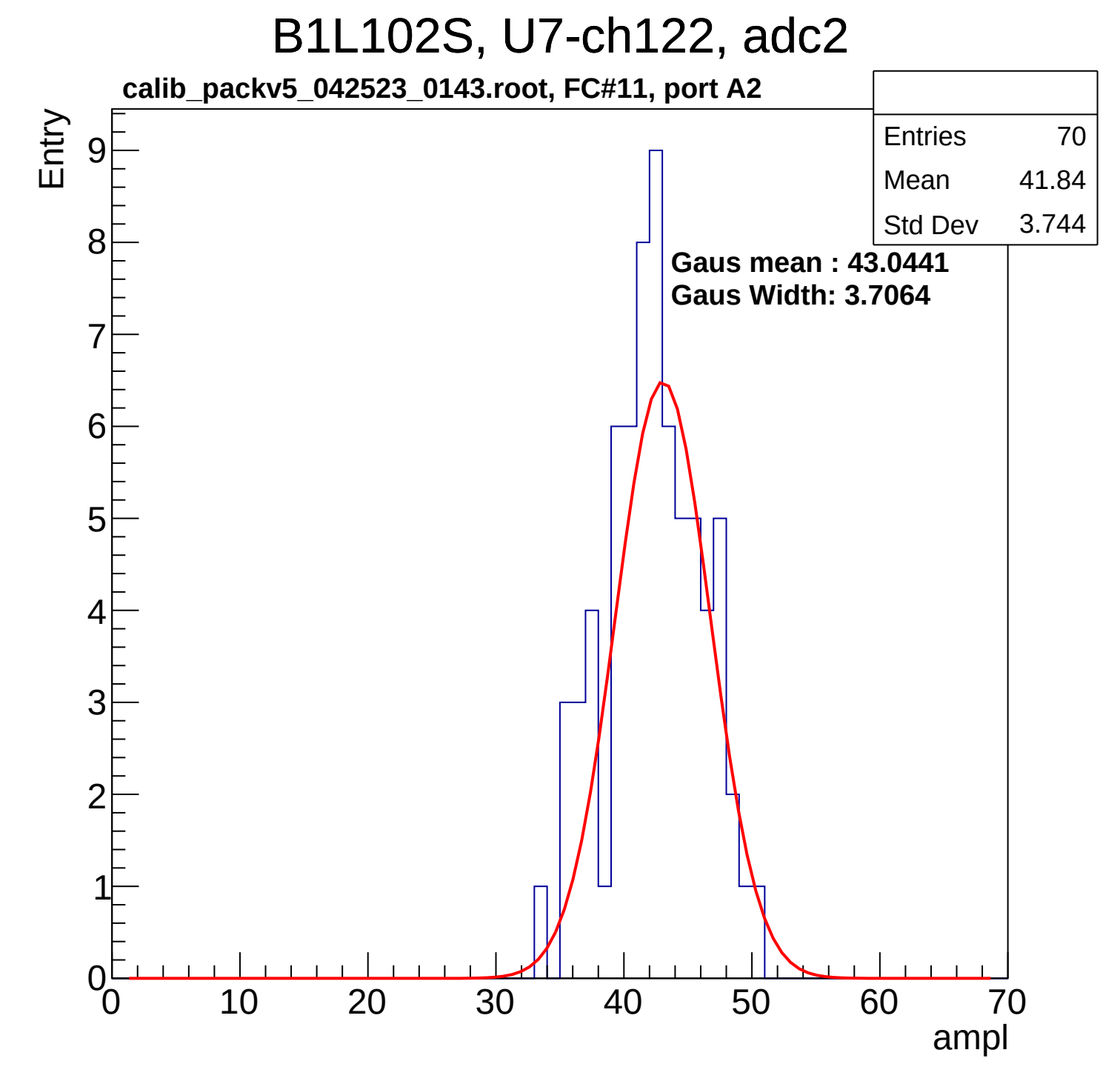

B1L102S, U7-ch121, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 40
Mean 60.48
Std Dev 2.28
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L102S, U7-ch121, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 4
Mean 46.5
Std Dev 26.86
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U7-ch121, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U7-ch122, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 48
Mean 25.12
Std Dev 9.407
Gaus mean : 28.9471
Gaus Width: 5.1953
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L102S, U7-ch122, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 75
Mean 34.44
Std Dev 3.681
Gaus mean : 35.1887
Gaus Width: 3.9971
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L102S, U7-ch122, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 70
Mean 41.84
Std Dev 3.744
Gaus mean : 43.0441
Gaus Width: 3.7064
Entry
ampl
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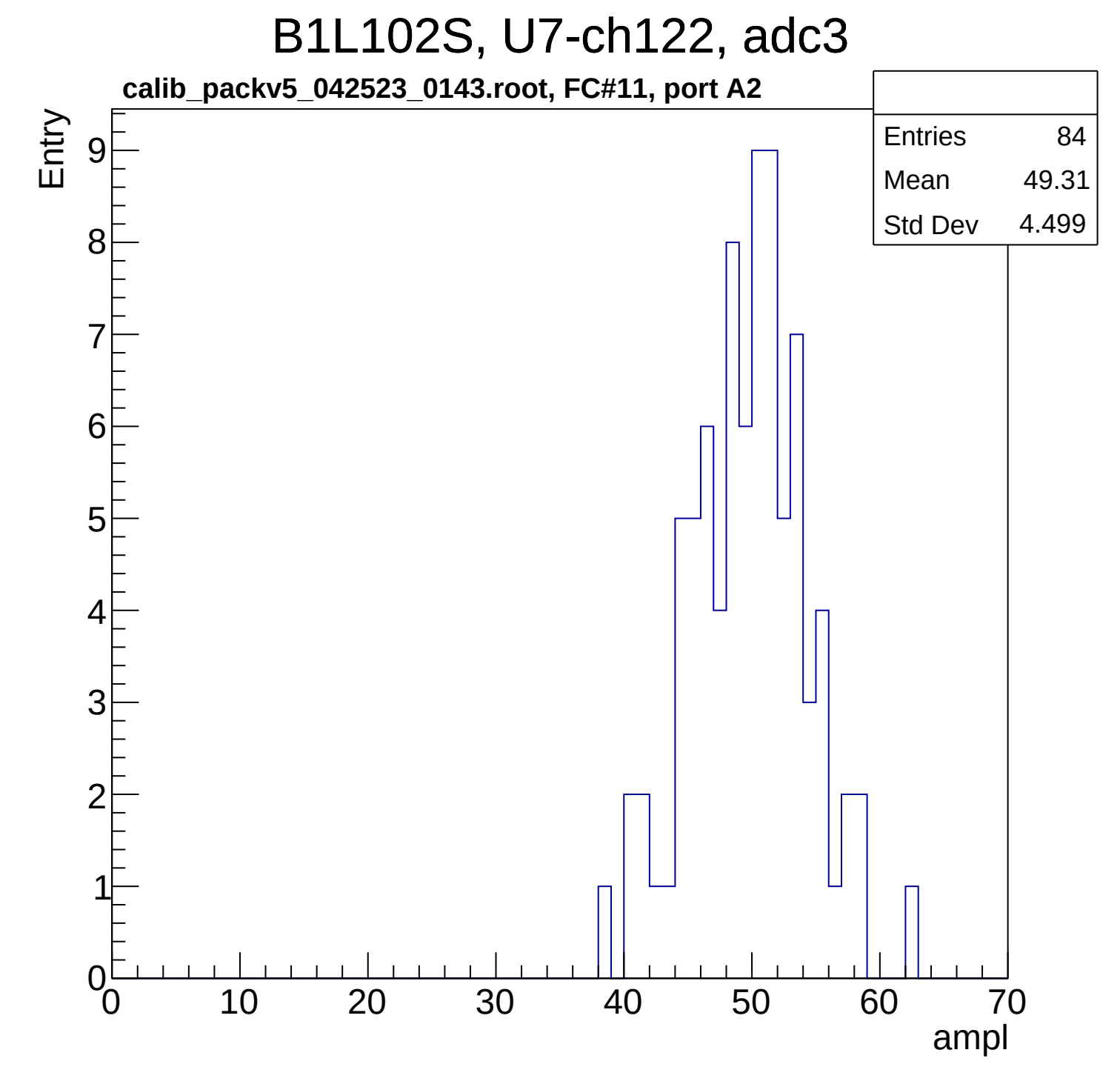
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L102S, U7-ch122, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 84
Mean 49.31
Std Dev 4.499
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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40
50
60
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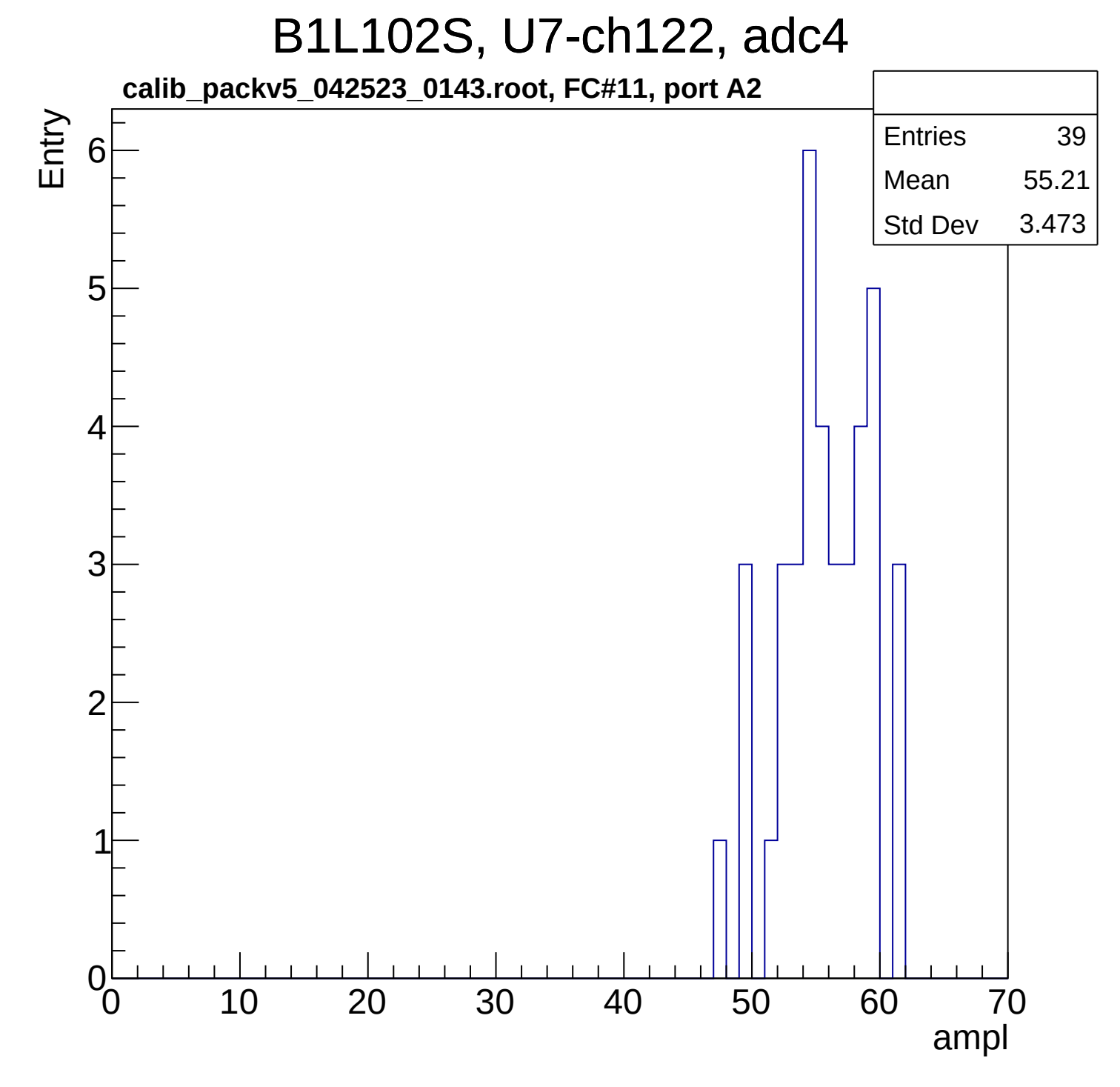
B1L102S, U7-ch122, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 39
Mean 55.21
Std Dev 3.473
Entry
ampl
0
1
2
3
4
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0
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60
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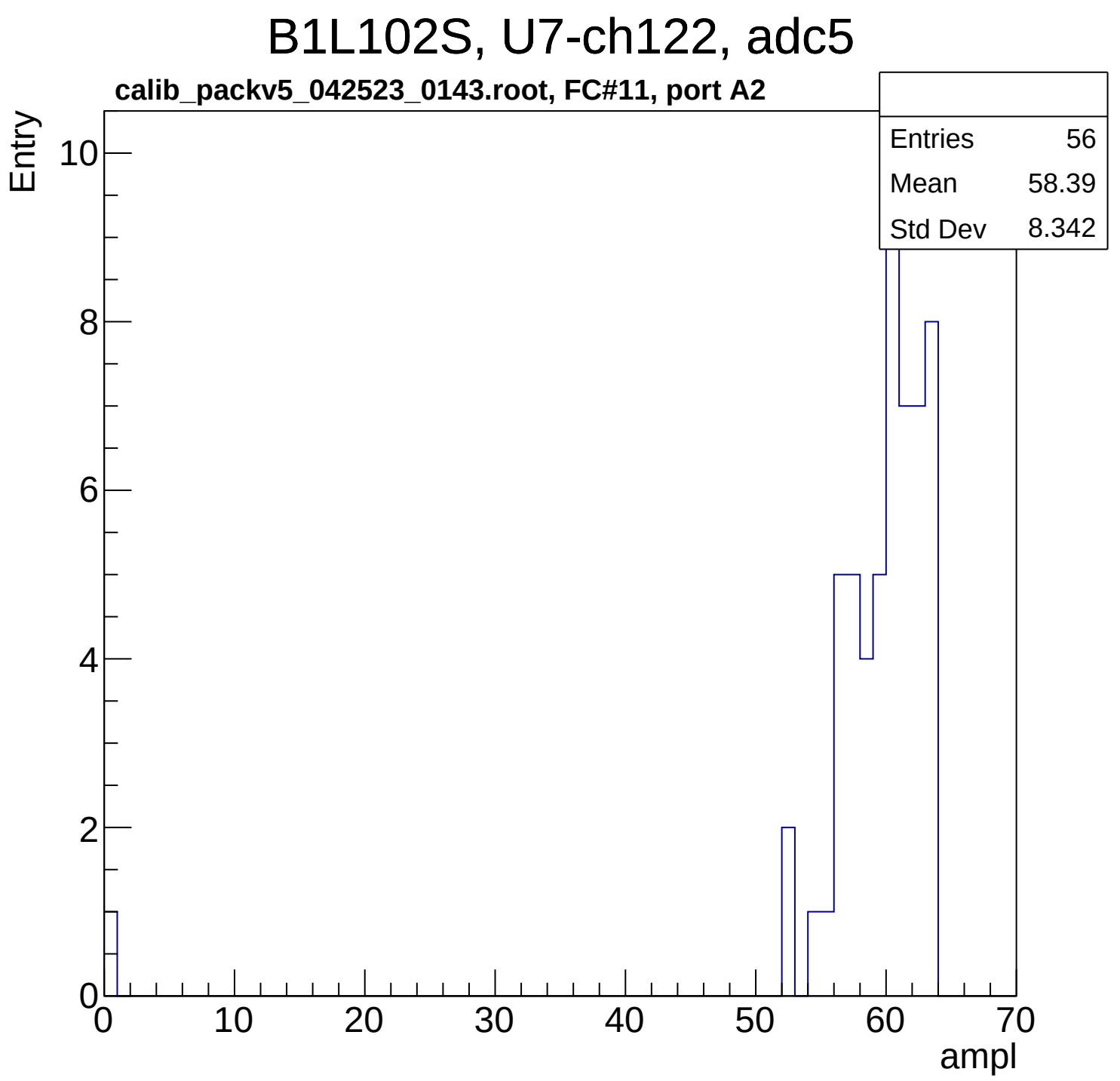
B1L102S, U7-ch122, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 56
Mean 58.39
Std Dev 8.342
Entry
ampl
0
2
4
6
8
10
0
10
20
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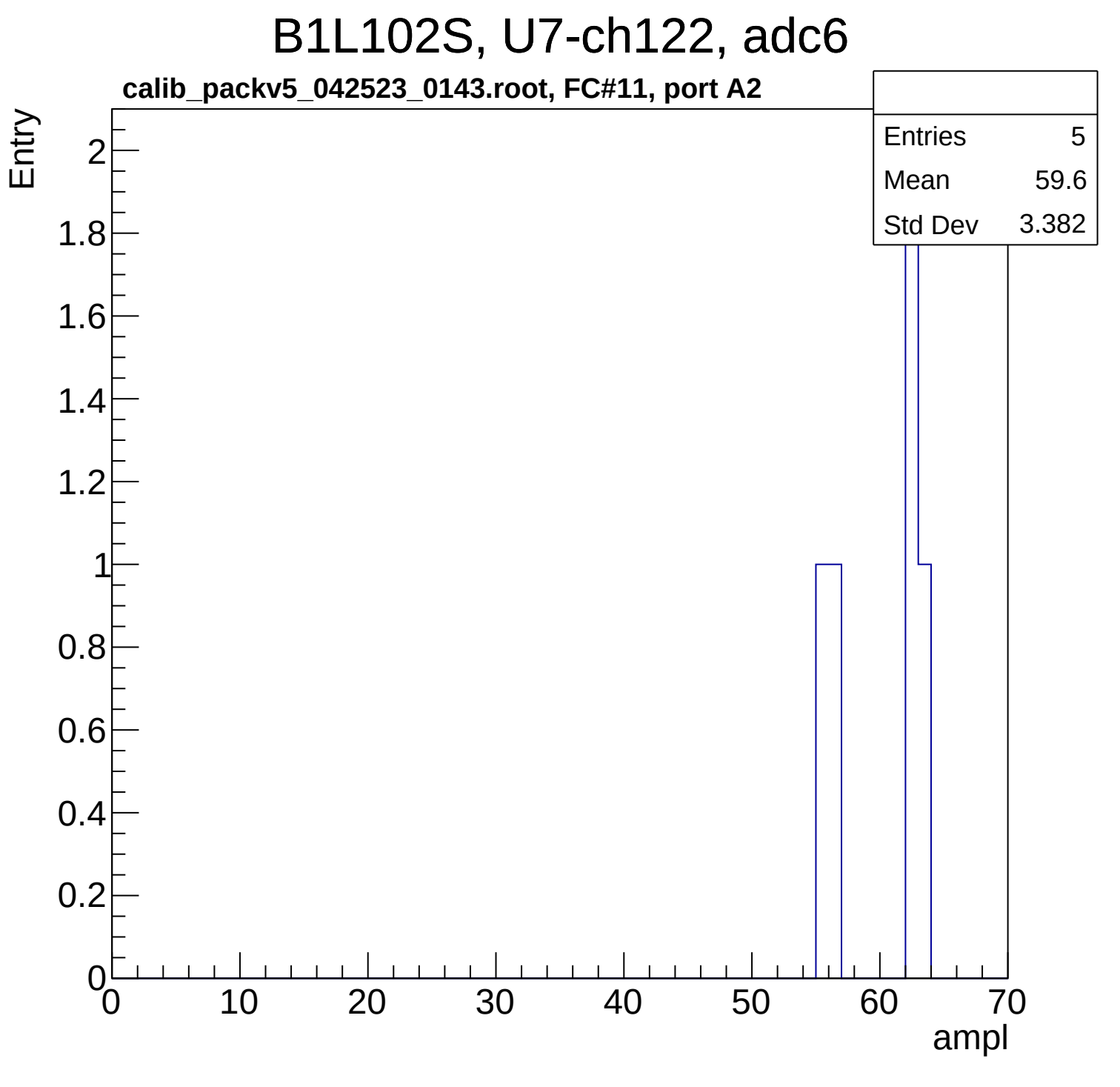
40
50
60
70


B1L102S, U7-ch122, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 5
Mean 59.6
Std Dev 3.382
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
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30
40
50
60
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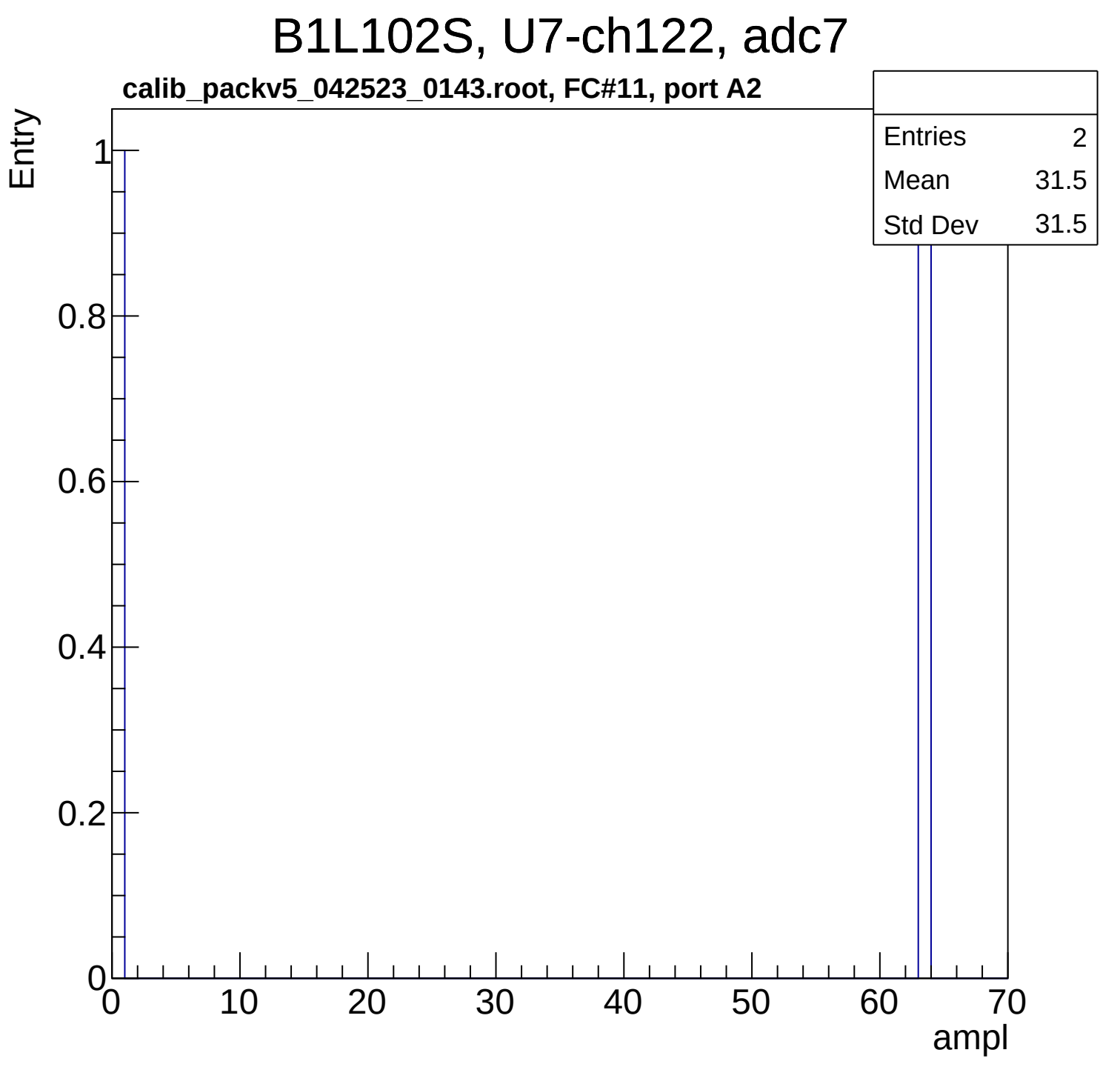
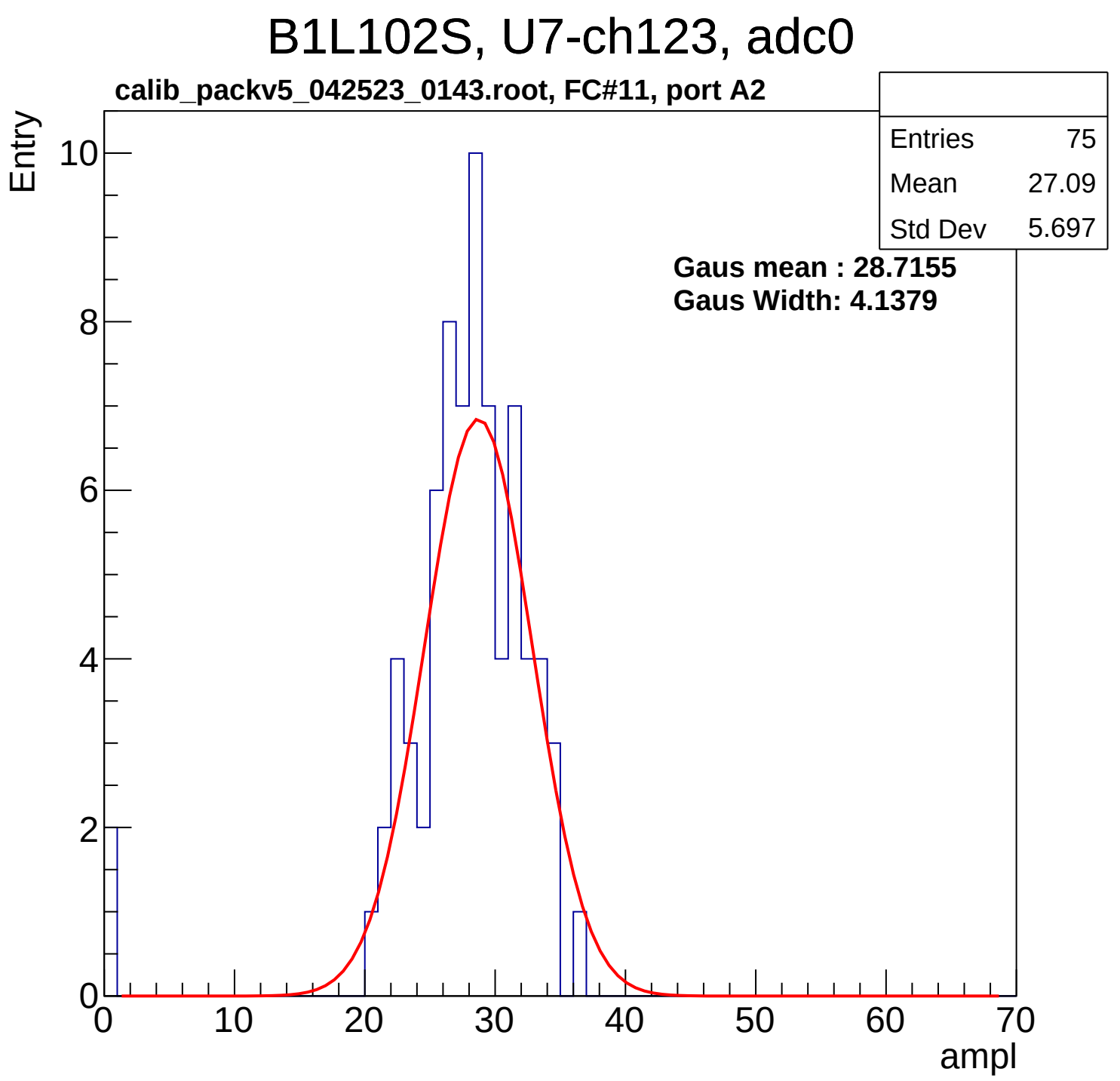

B1L102S, U7-ch122, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 2
Mean 31.5
Std Dev 31.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U7-ch123, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 75
Mean 27.09
Std Dev 5.697
Gaus mean : 28.7155
Gaus Width: 4.1379
Entry
ampl
0
2
4
6
8
10
0
10
20
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40
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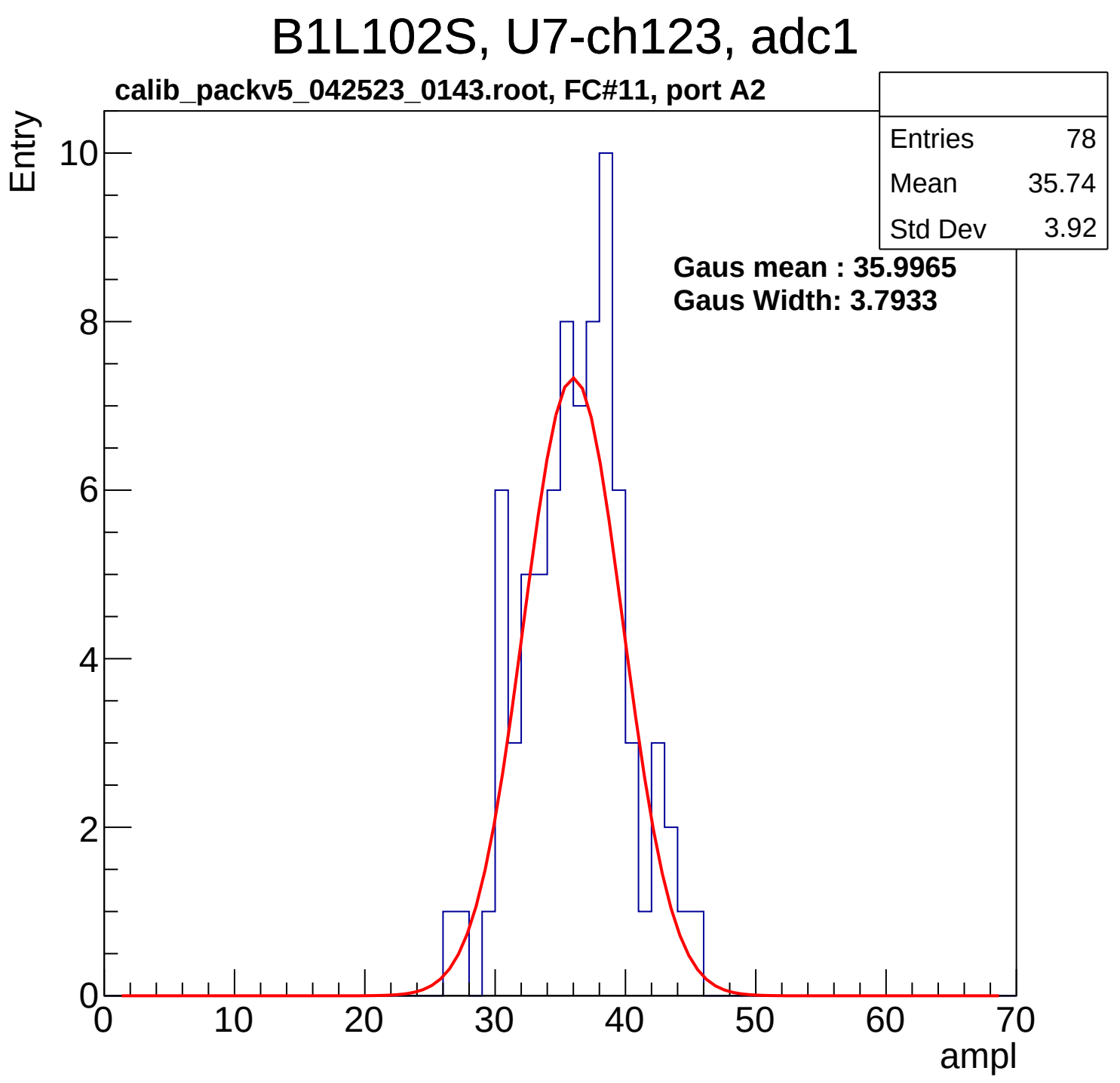
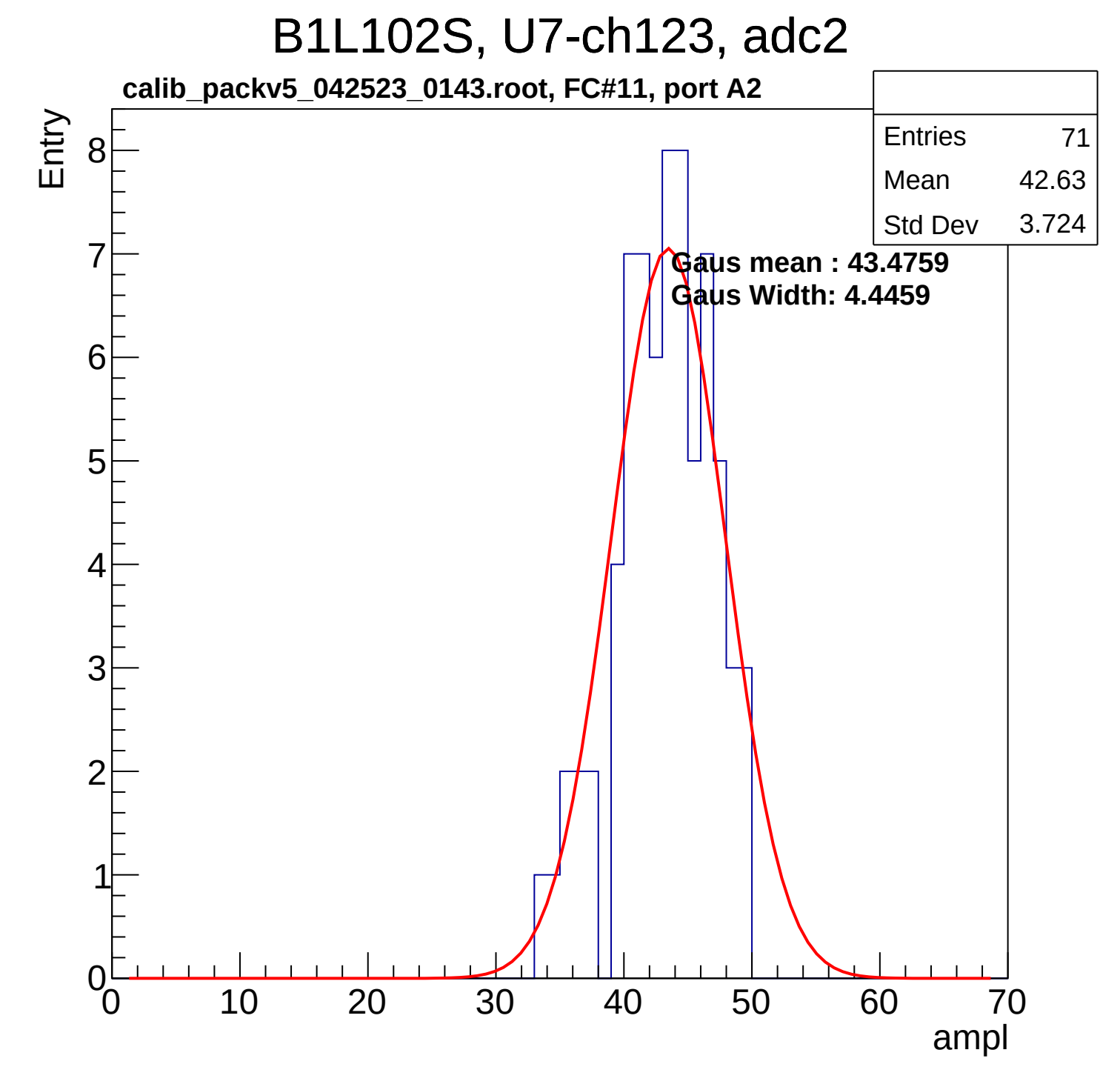
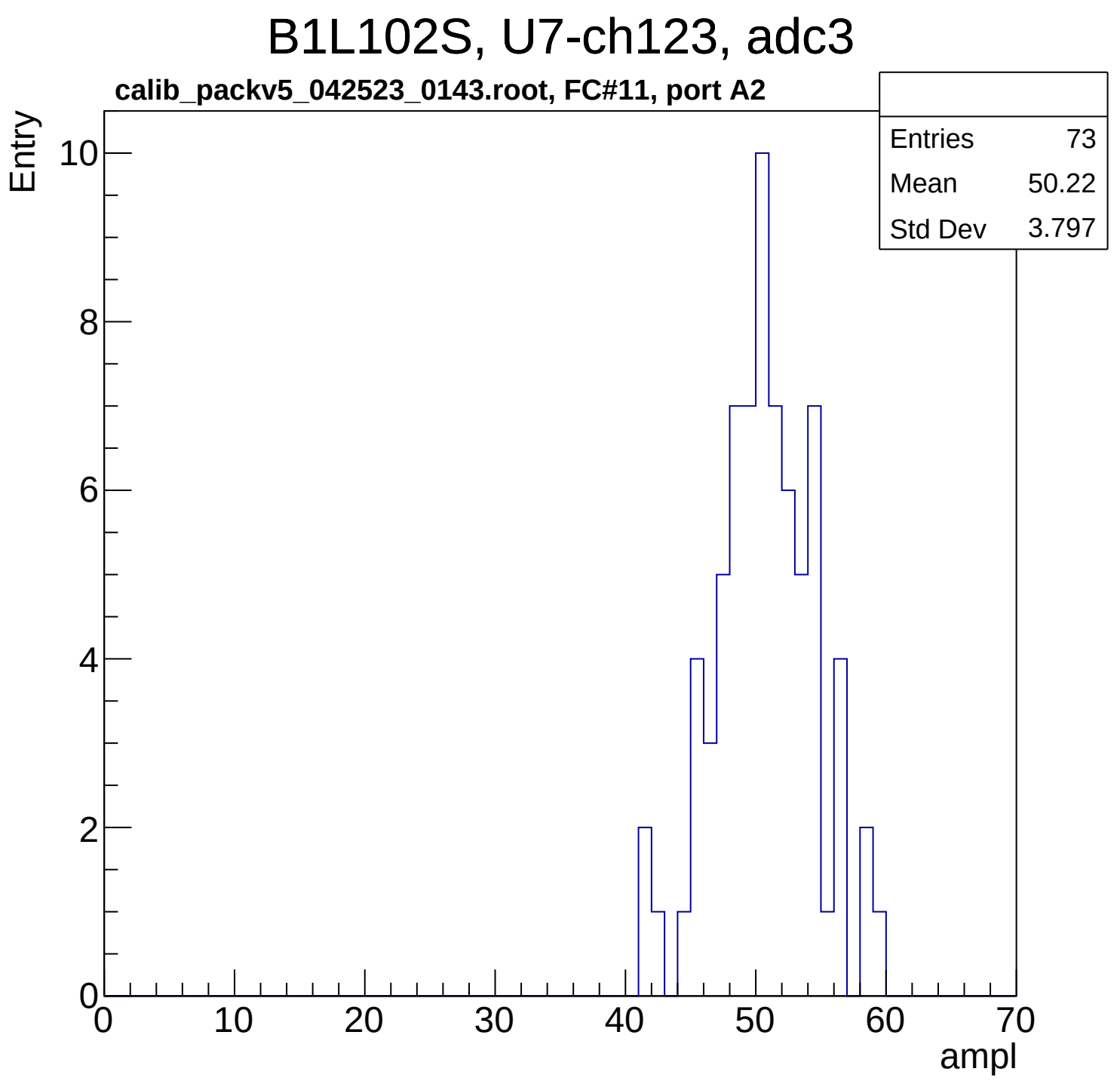
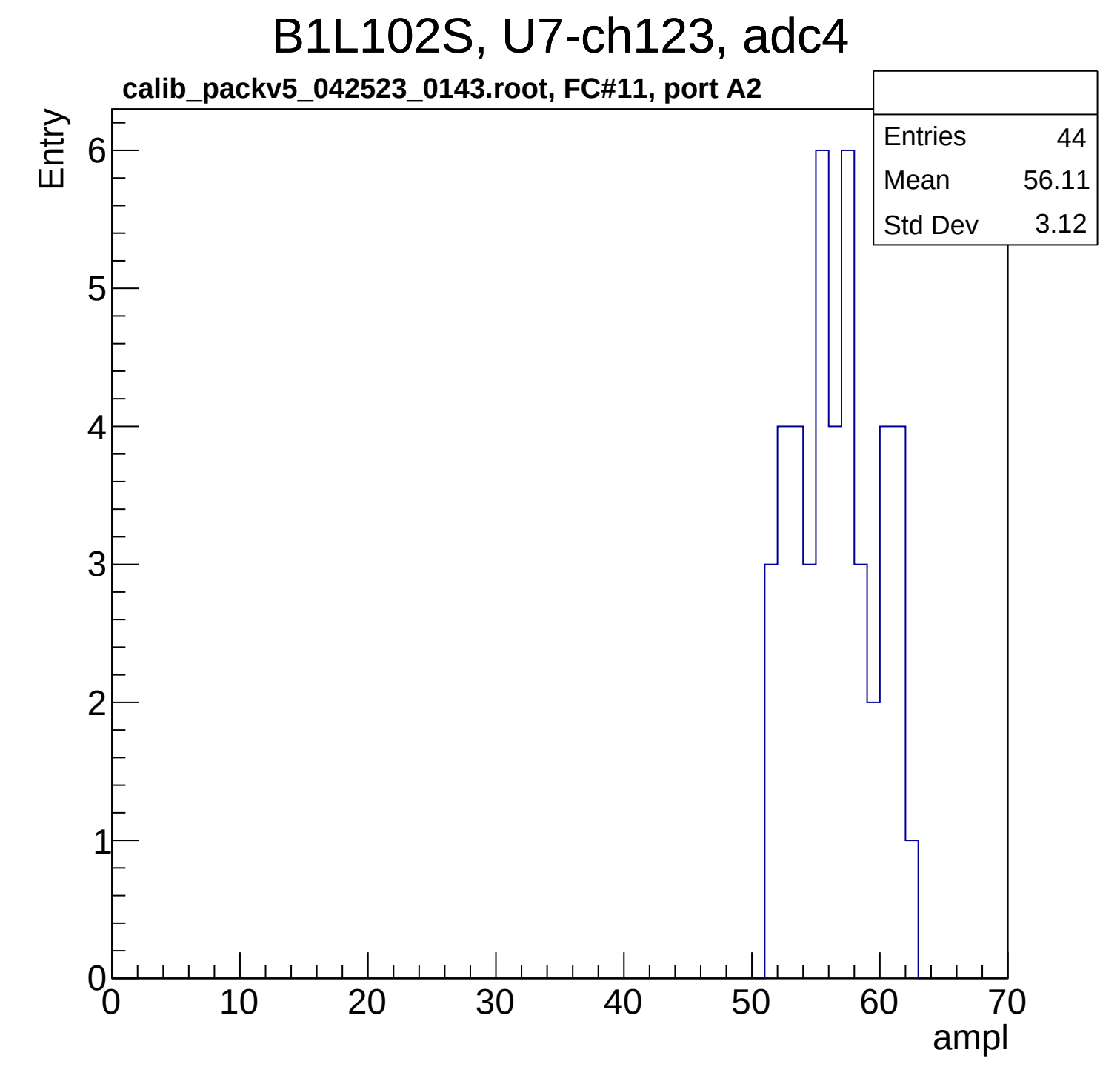
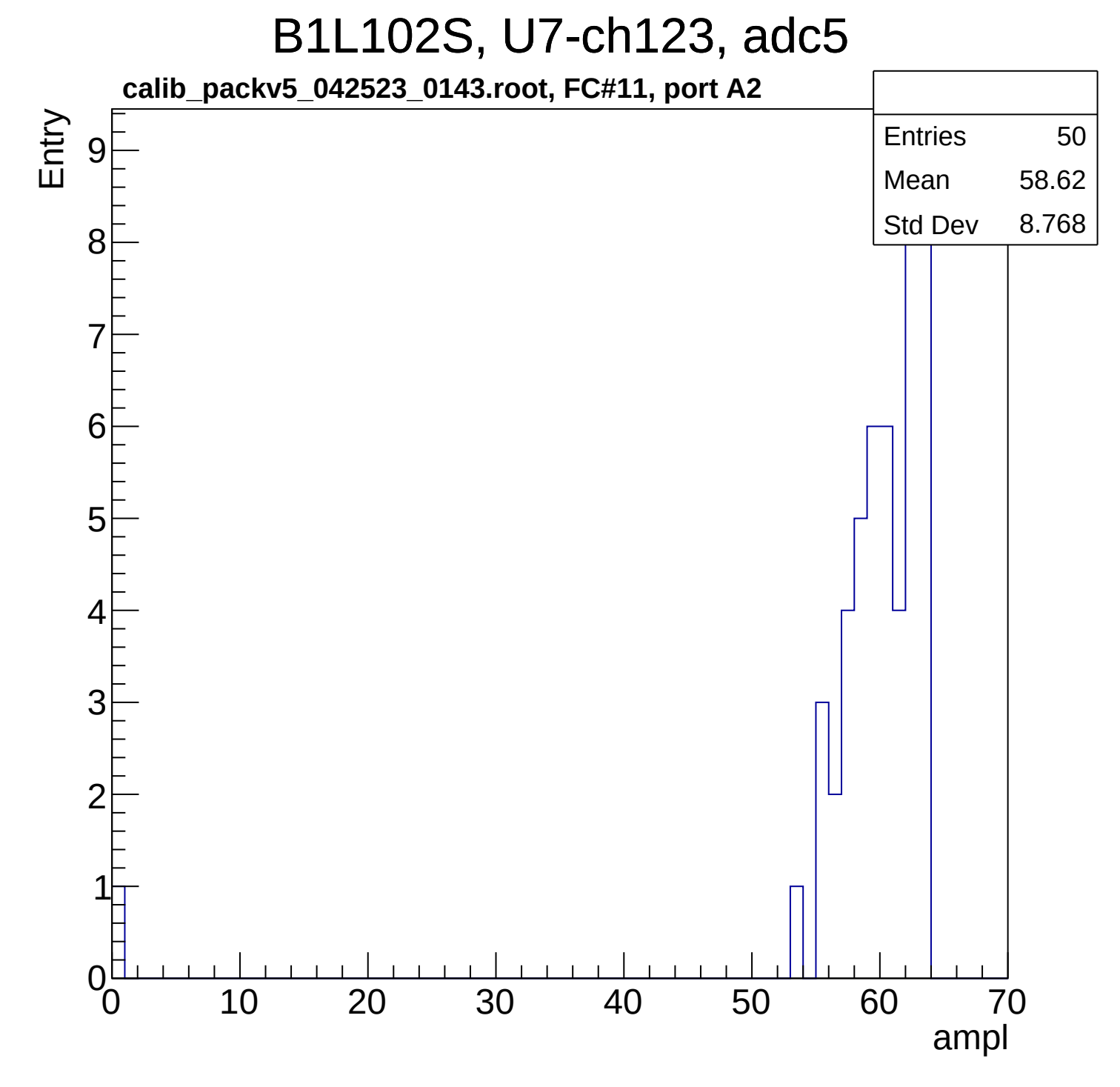

B1L102S, U7-ch123, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 78
Mean 35.74
Std Dev 3.92
Gaus mean : 35.9965
Gaus Width: 3.7933
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L102S, U7-ch123, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 71
Mean 42.63
Std Dev 3.724
Gaus mean : 43.4759
Gaus Width: 4.4459
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L102S, U7-ch123, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 73
Mean 50.22
Std Dev 3.797
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L102S, U7-ch123, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 44
Mean 56.11
Std Dev 3.12
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L102S, U7-ch123, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 50
Mean 58.62
Std Dev 8.768
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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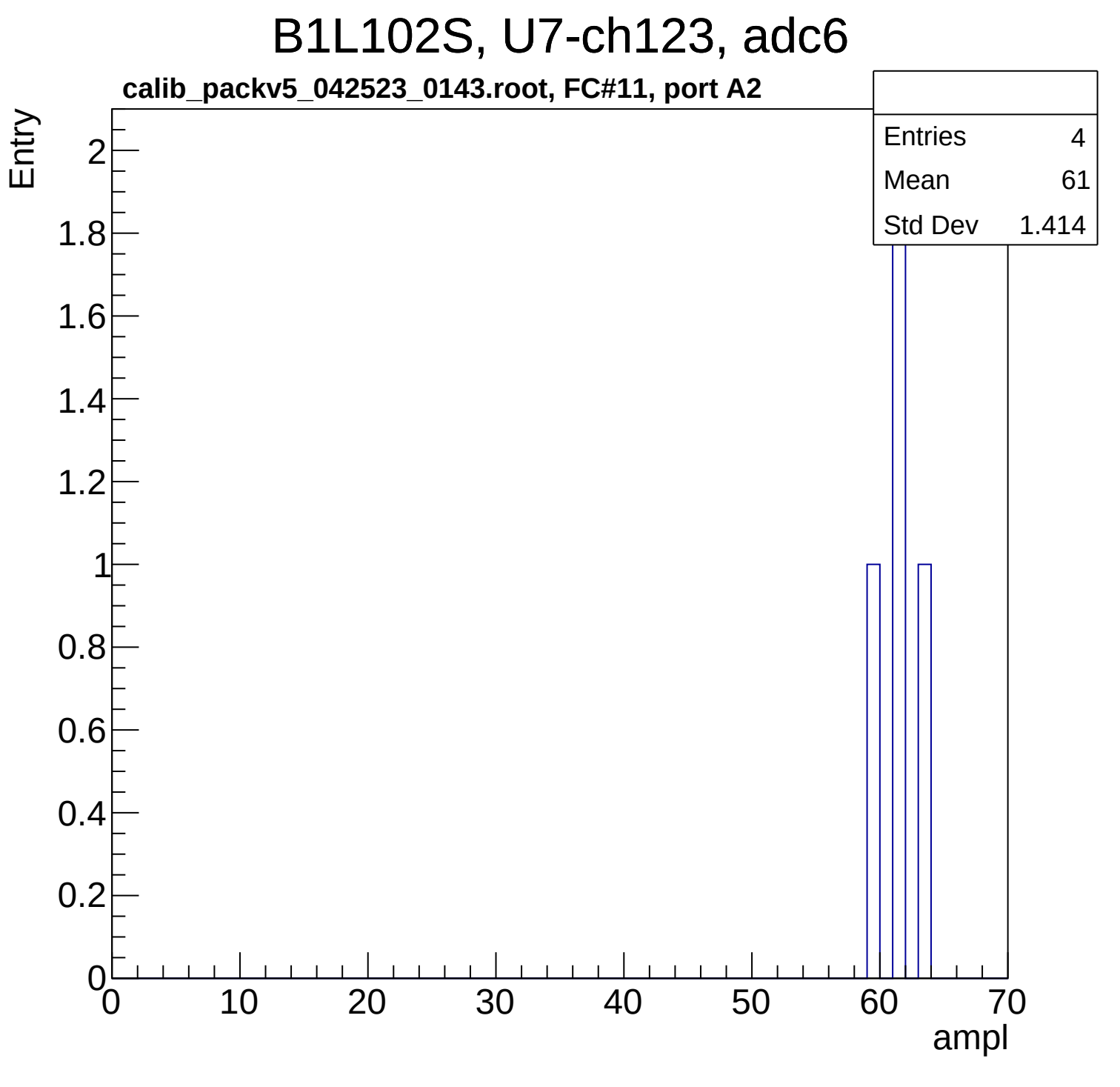
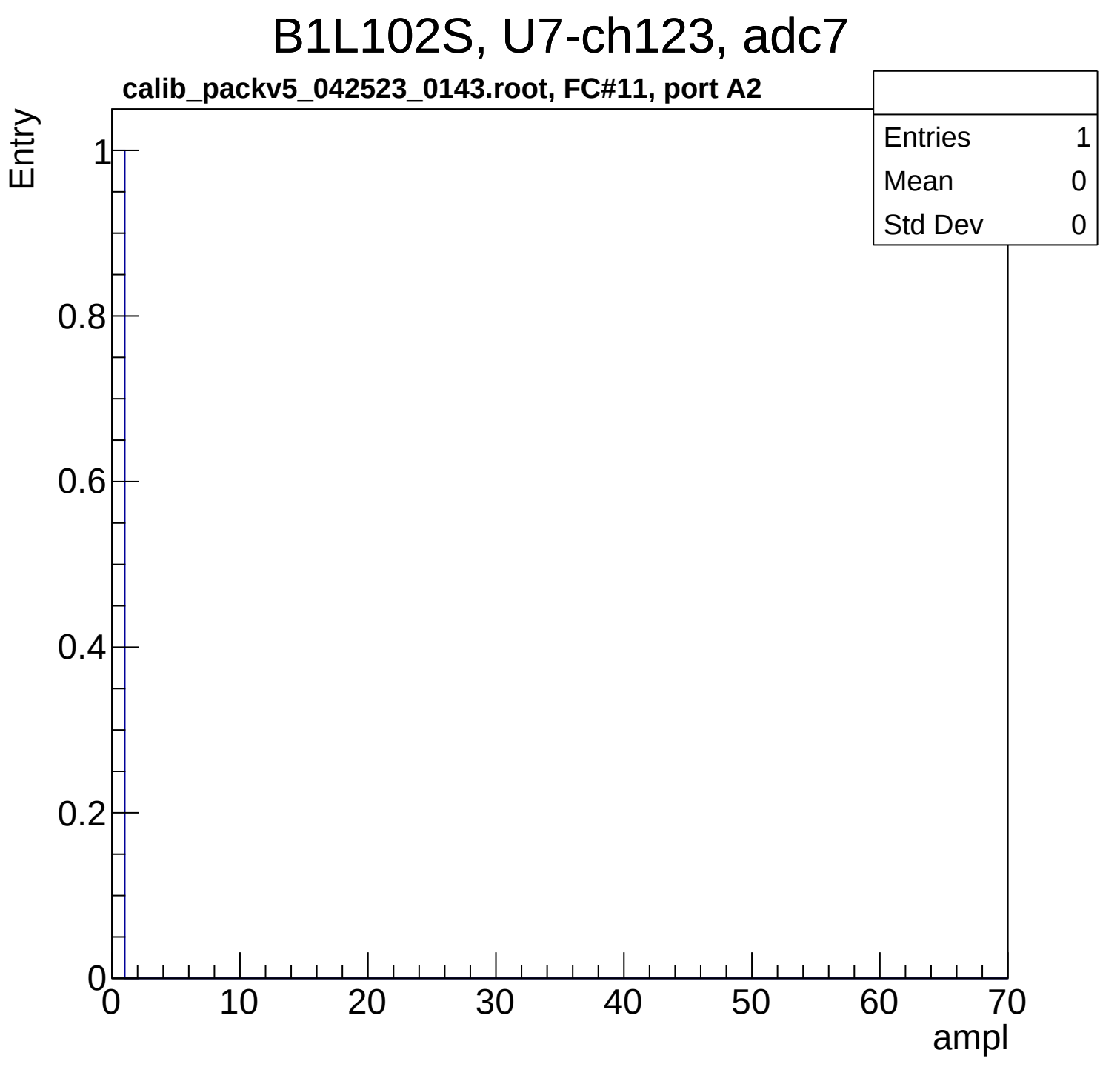
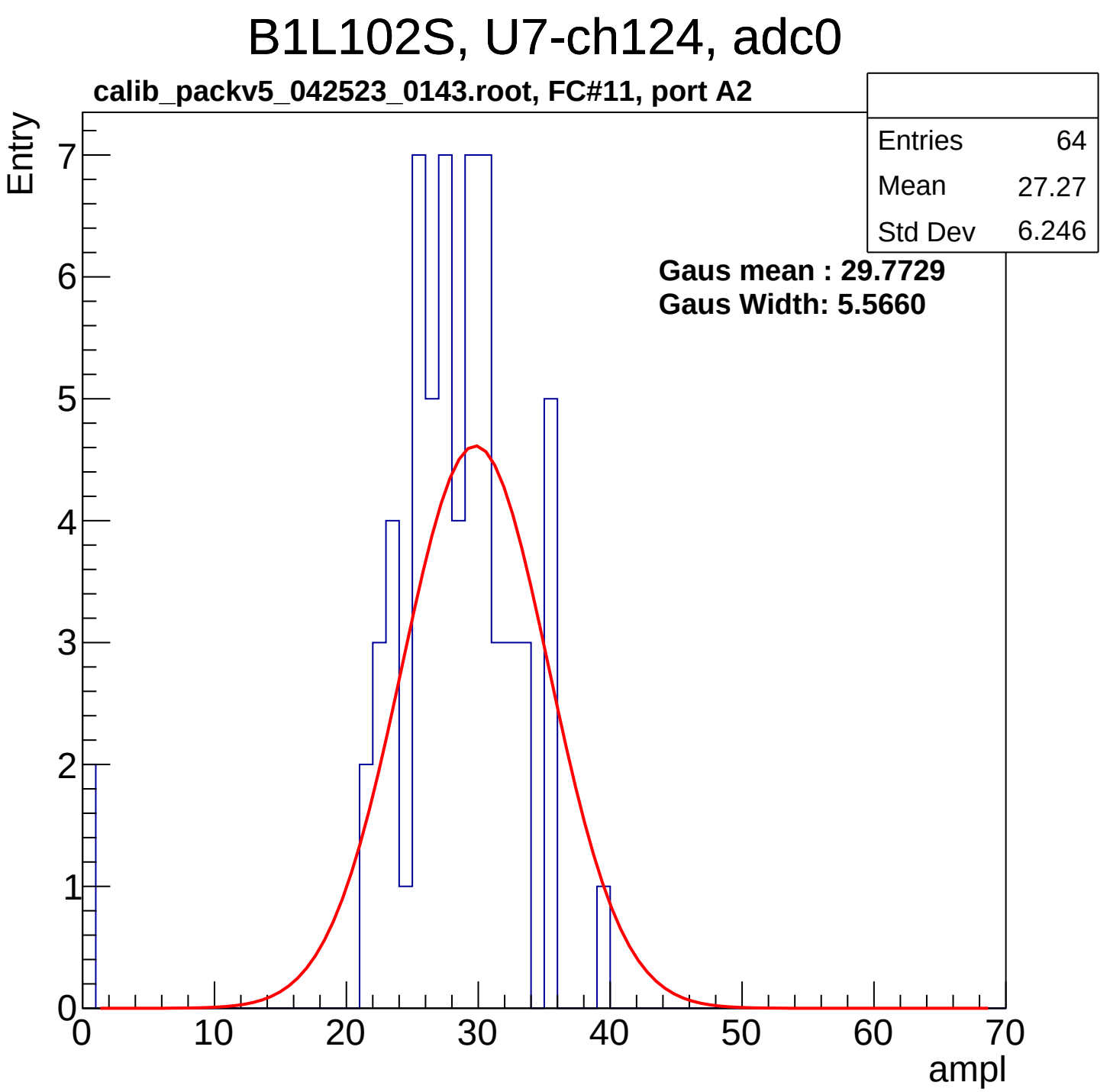
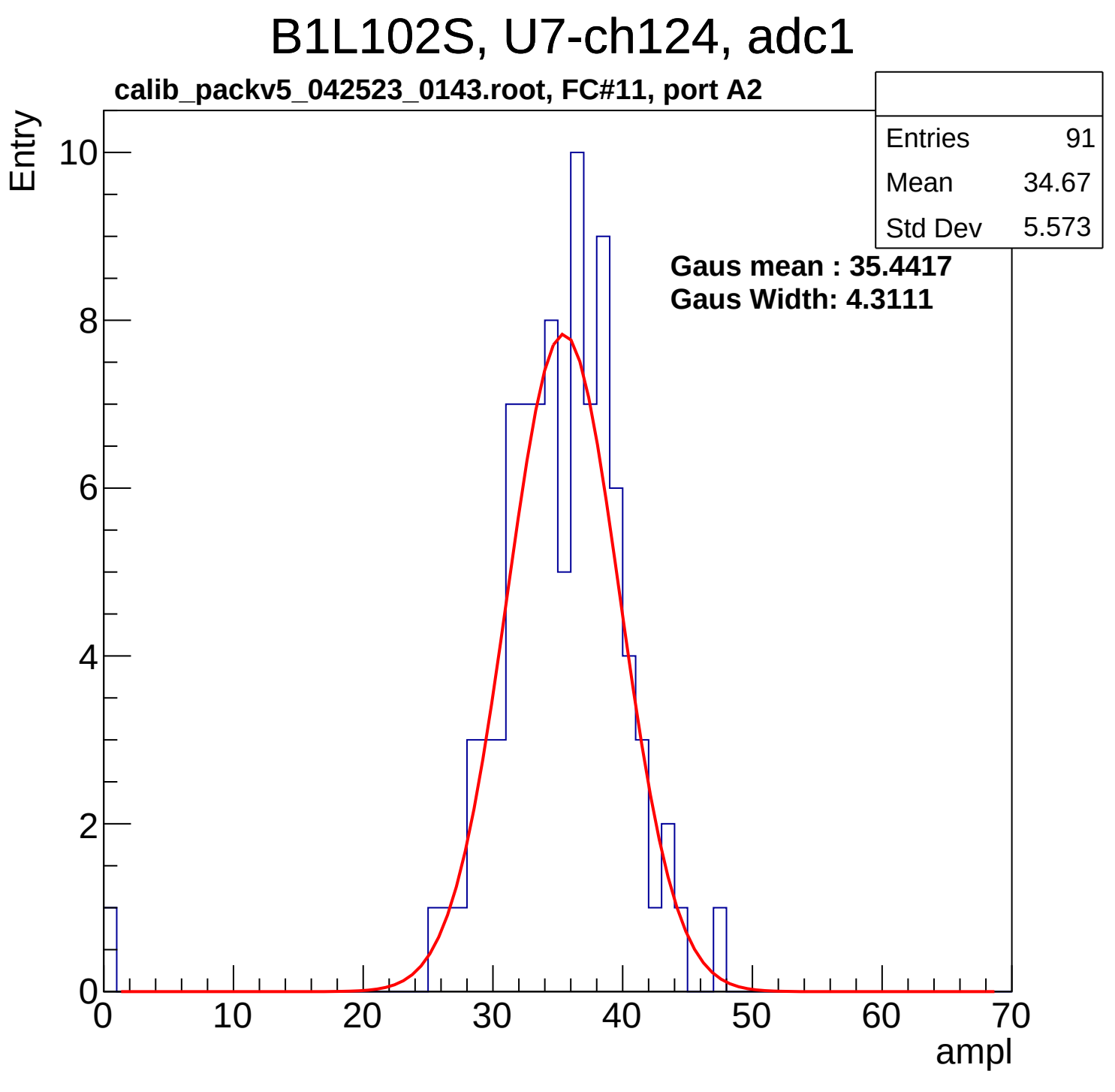
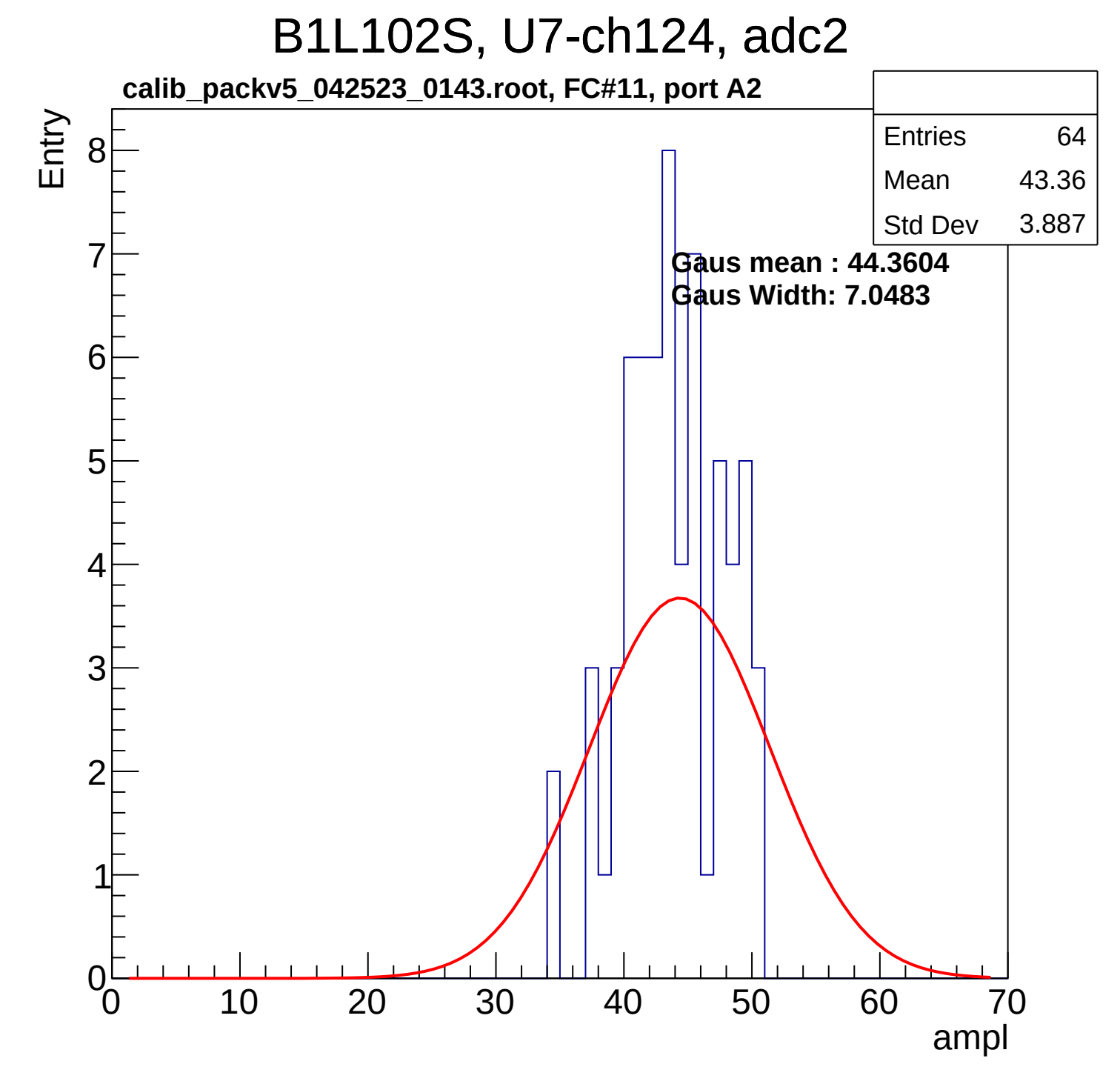
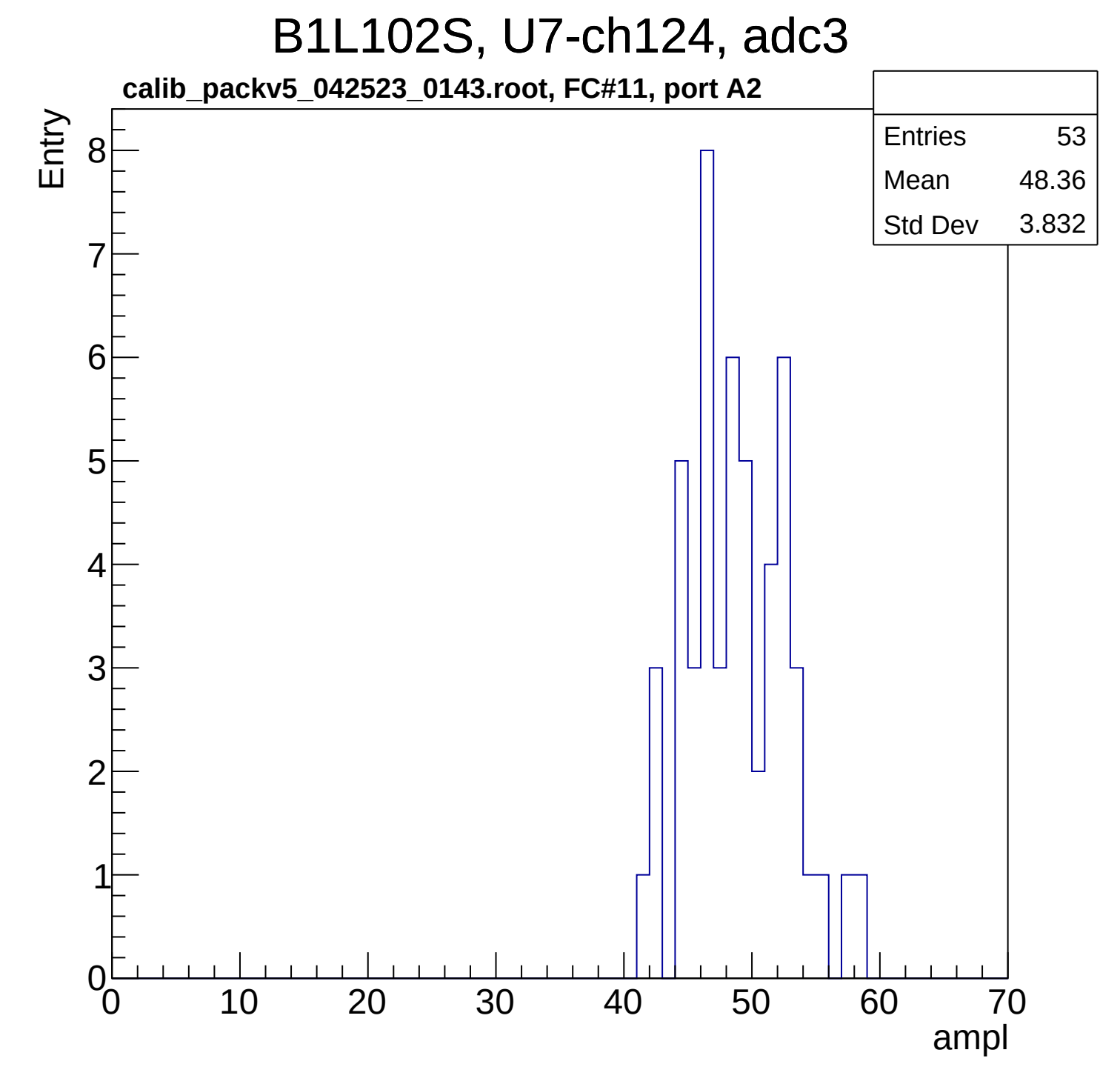

B1L102S, U7-ch123, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 4
Mean 61
Std Dev 1.414
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

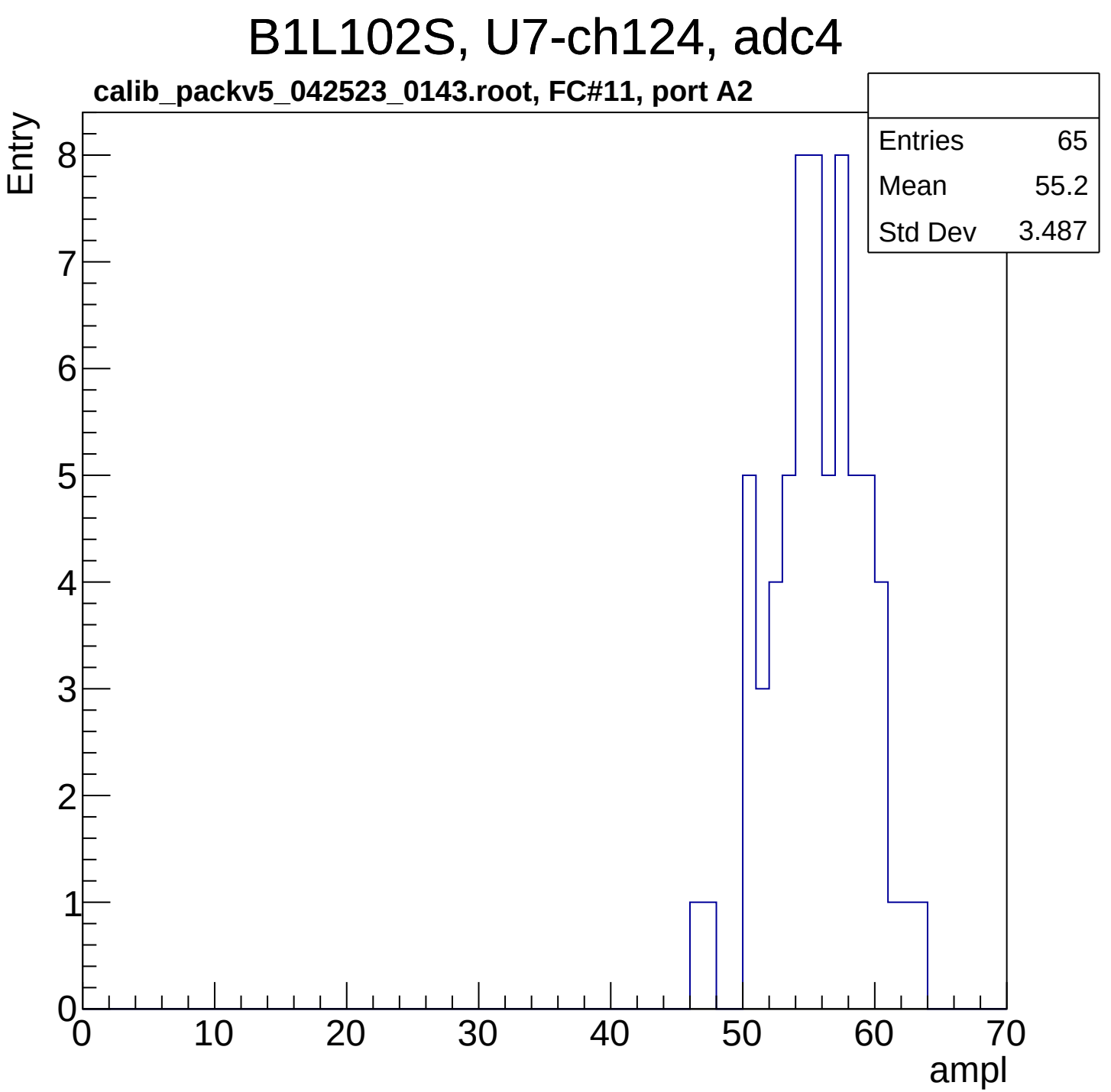

B1L102S, U7-ch123, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

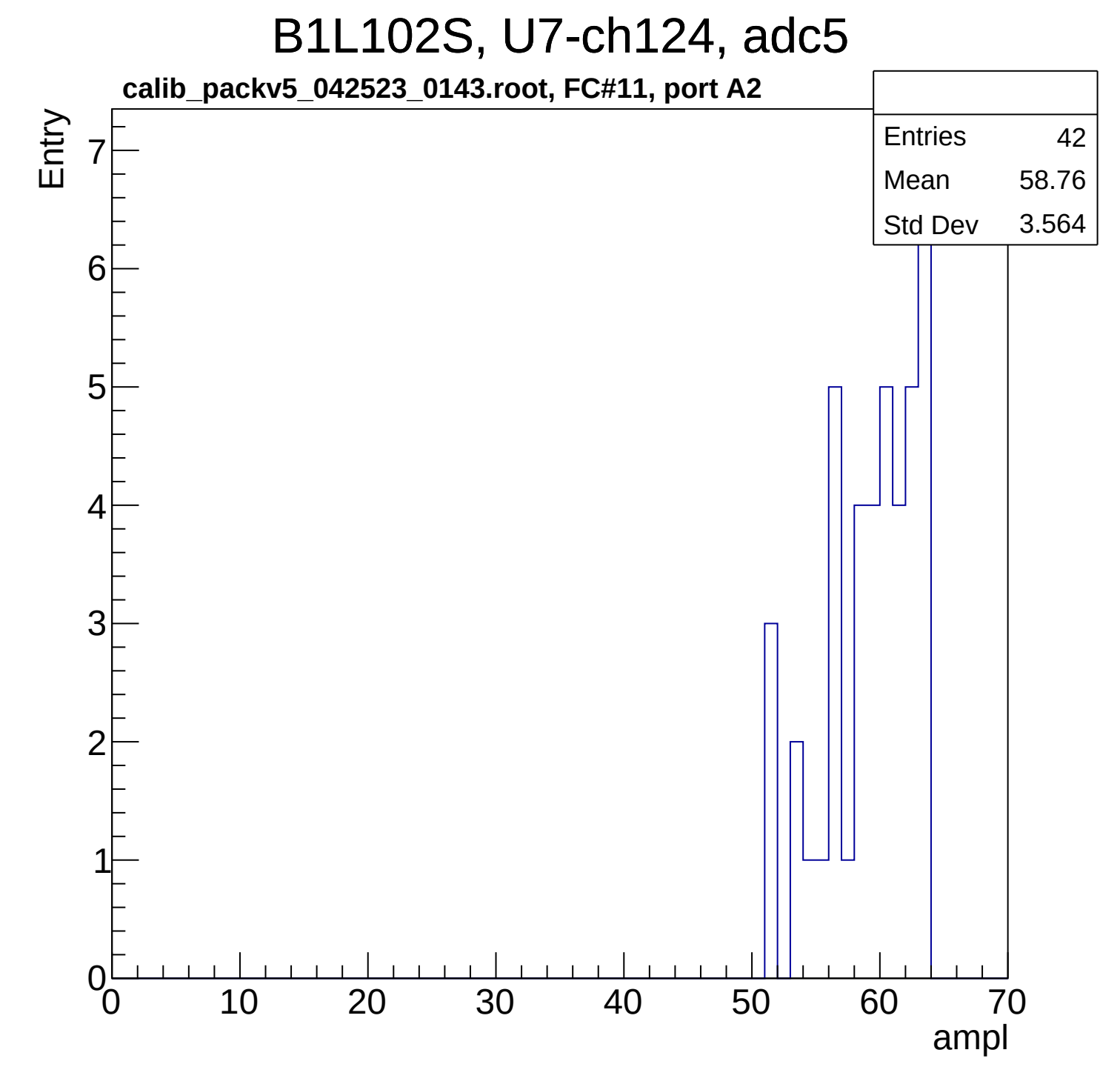

B1L102S, U7-ch124, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 64
Mean 27.27
Std Dev 6.246
Gaus mean : 29.7729
Gaus Width: 5.5660
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

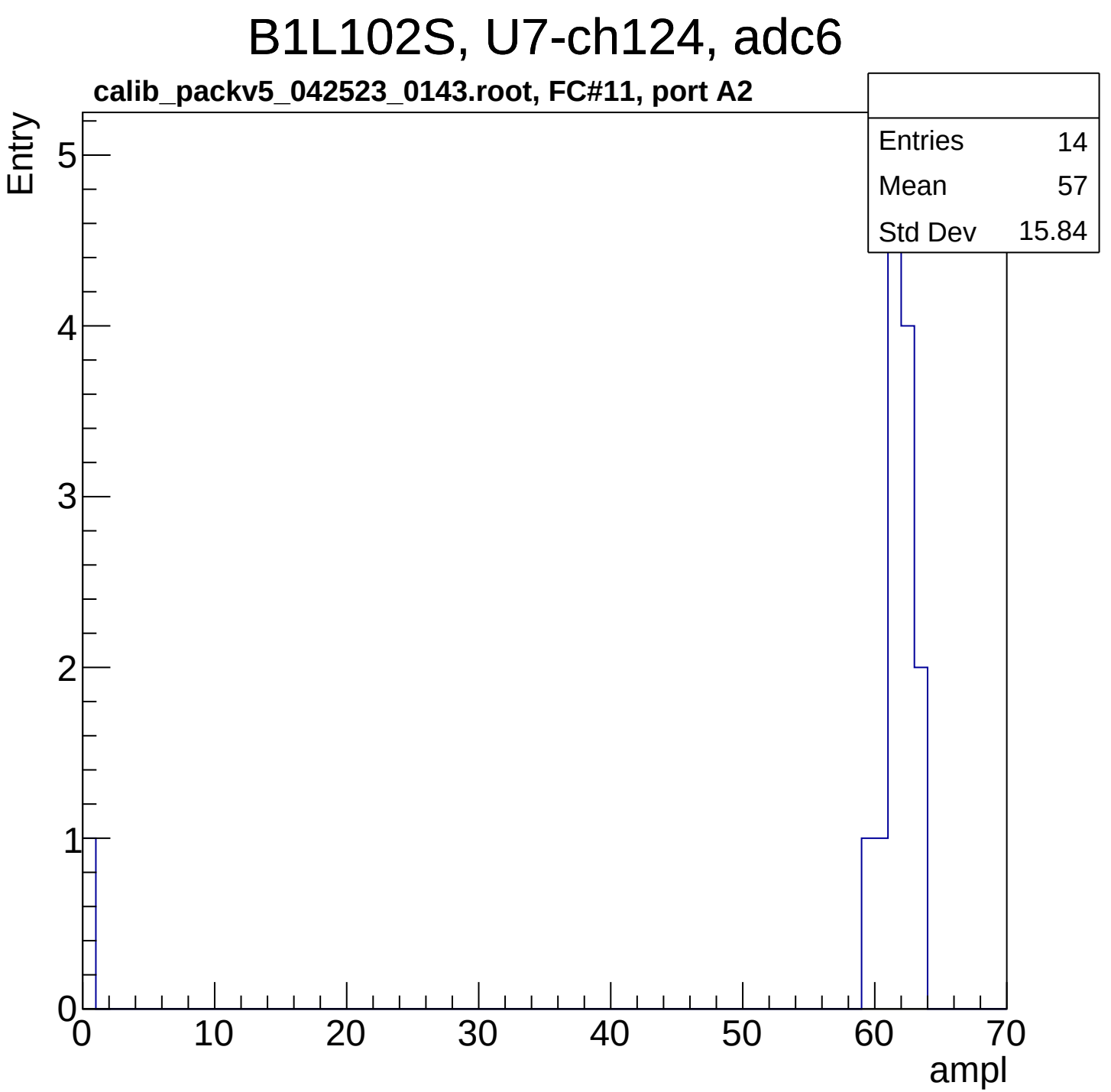

B1L102S, U7-ch124, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 91
Mean 34.67
Std Dev 5.573
Gaus mean : 35.4417
Gaus Width: 4.3111
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

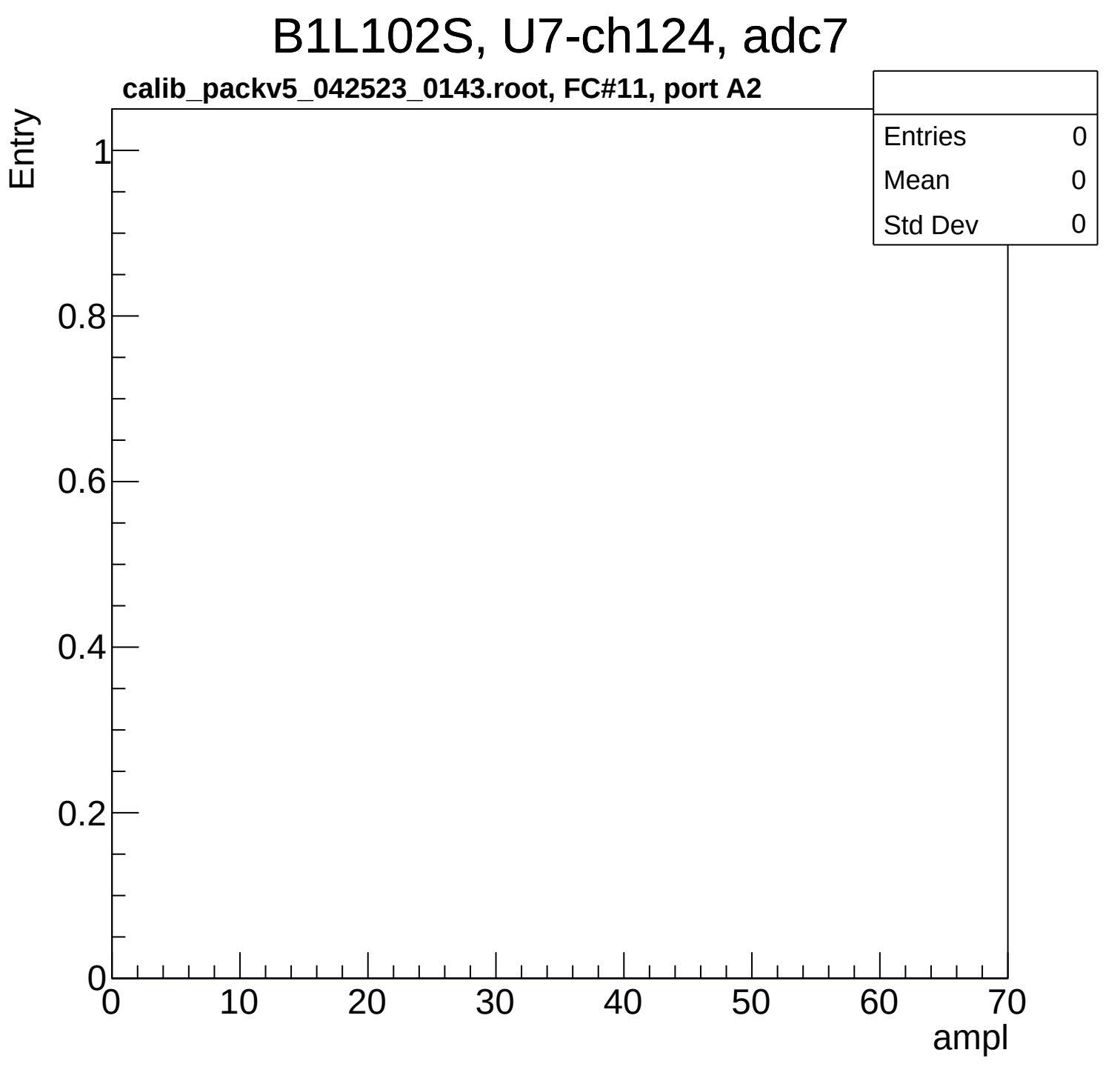

B1L102S, U7-ch124, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 64
Mean 43.36
Std Dev 3.887
Gaus mean : 44.3604
Gaus Width: 7.0483
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

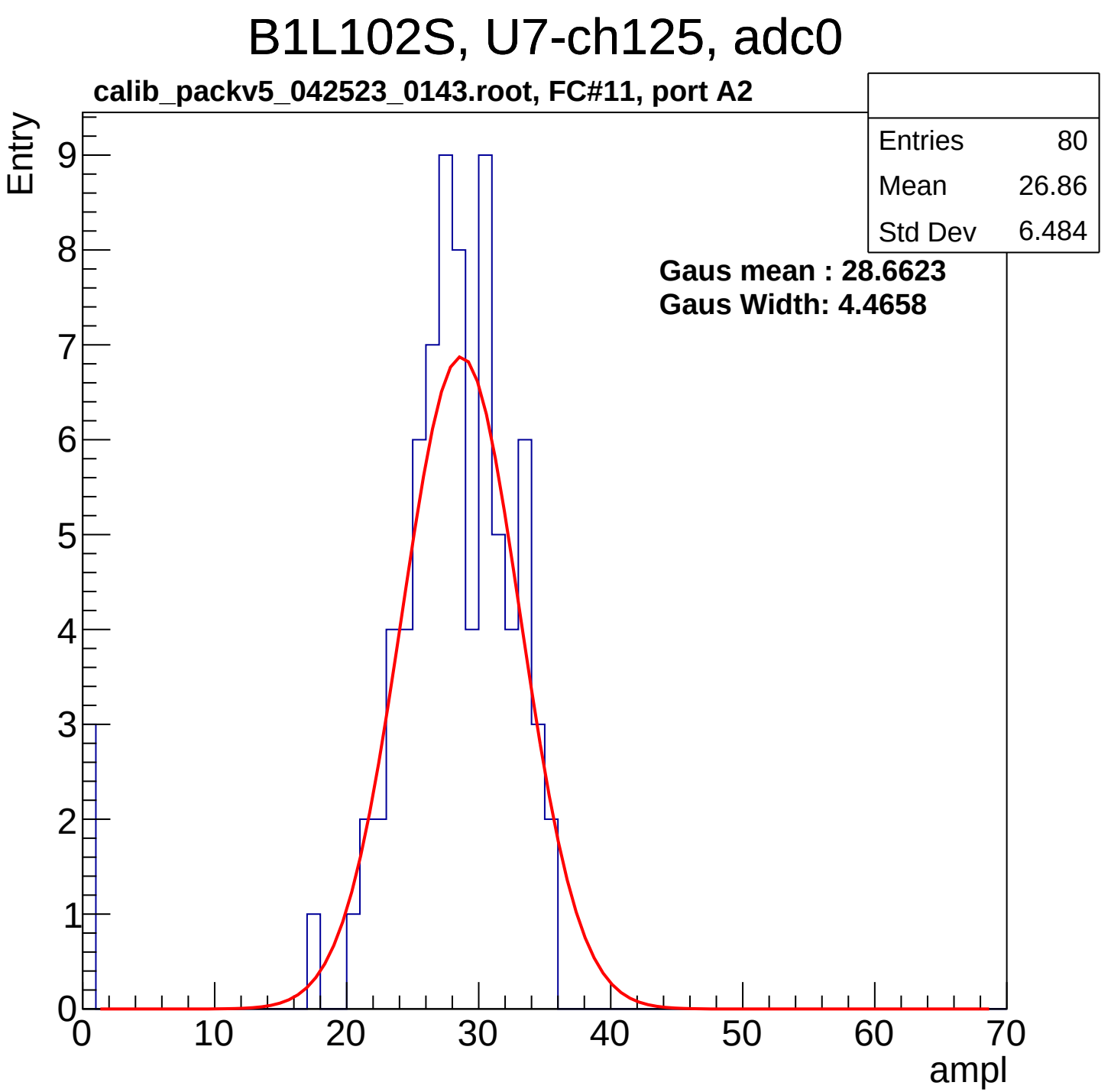

B1L102S, U7-ch124, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 53
Mean 48.36
Std Dev 3.832
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

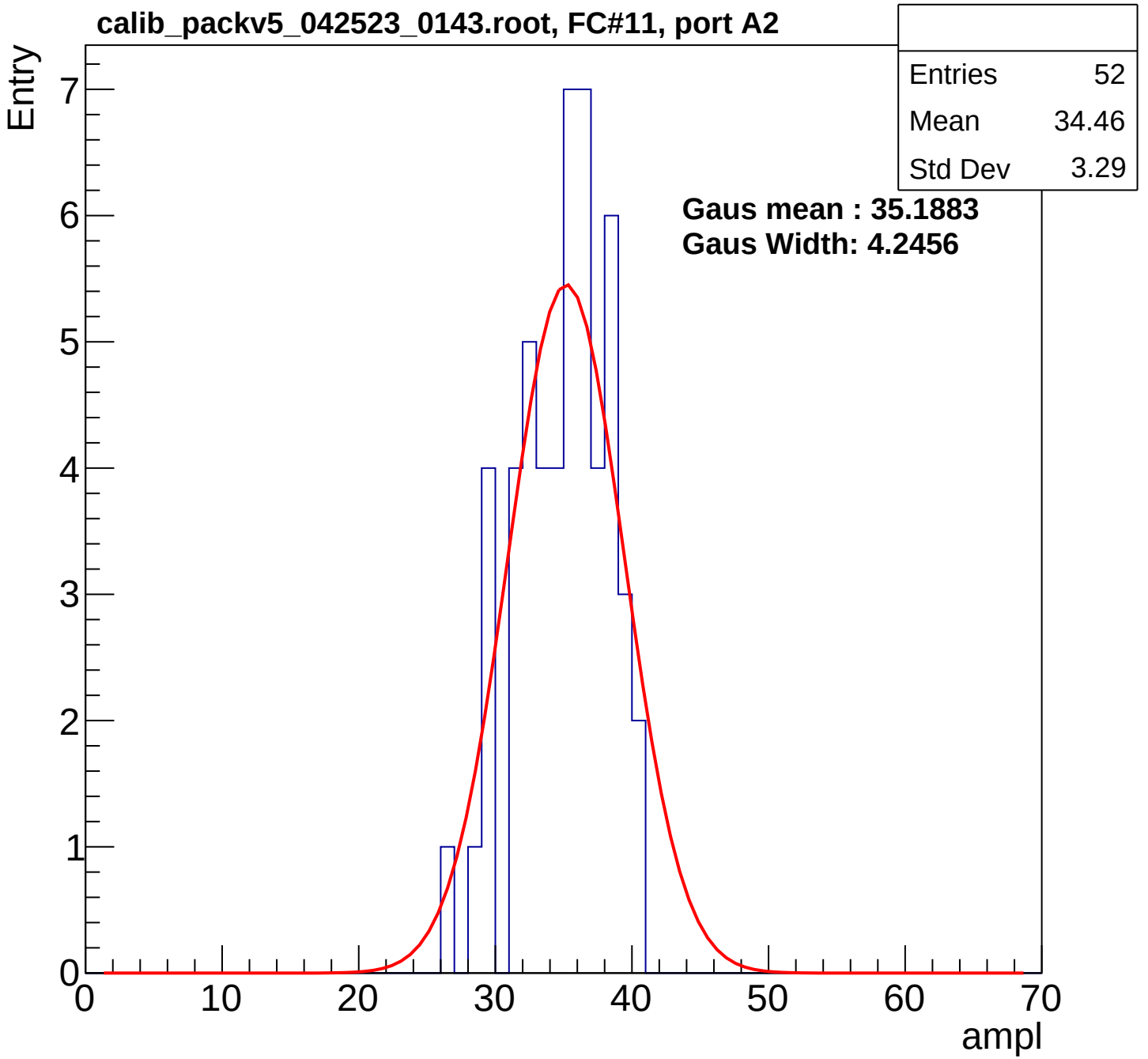

B1L102S, U7-ch124, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 65
Mean 55.2
Std Dev 3.487
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

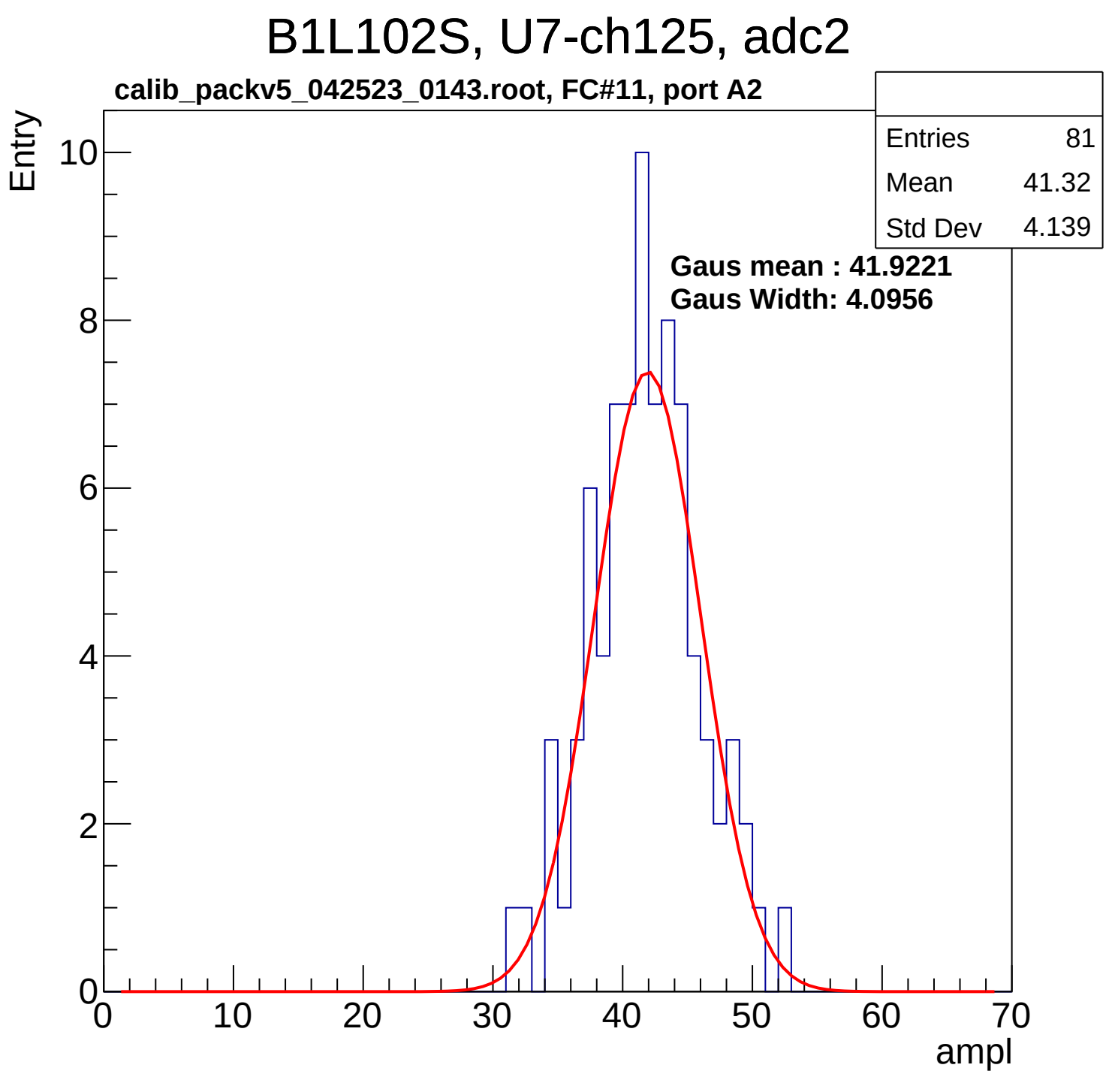

B1L102S, U7-ch124, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 42
Mean 58.76
Std Dev 3.564
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

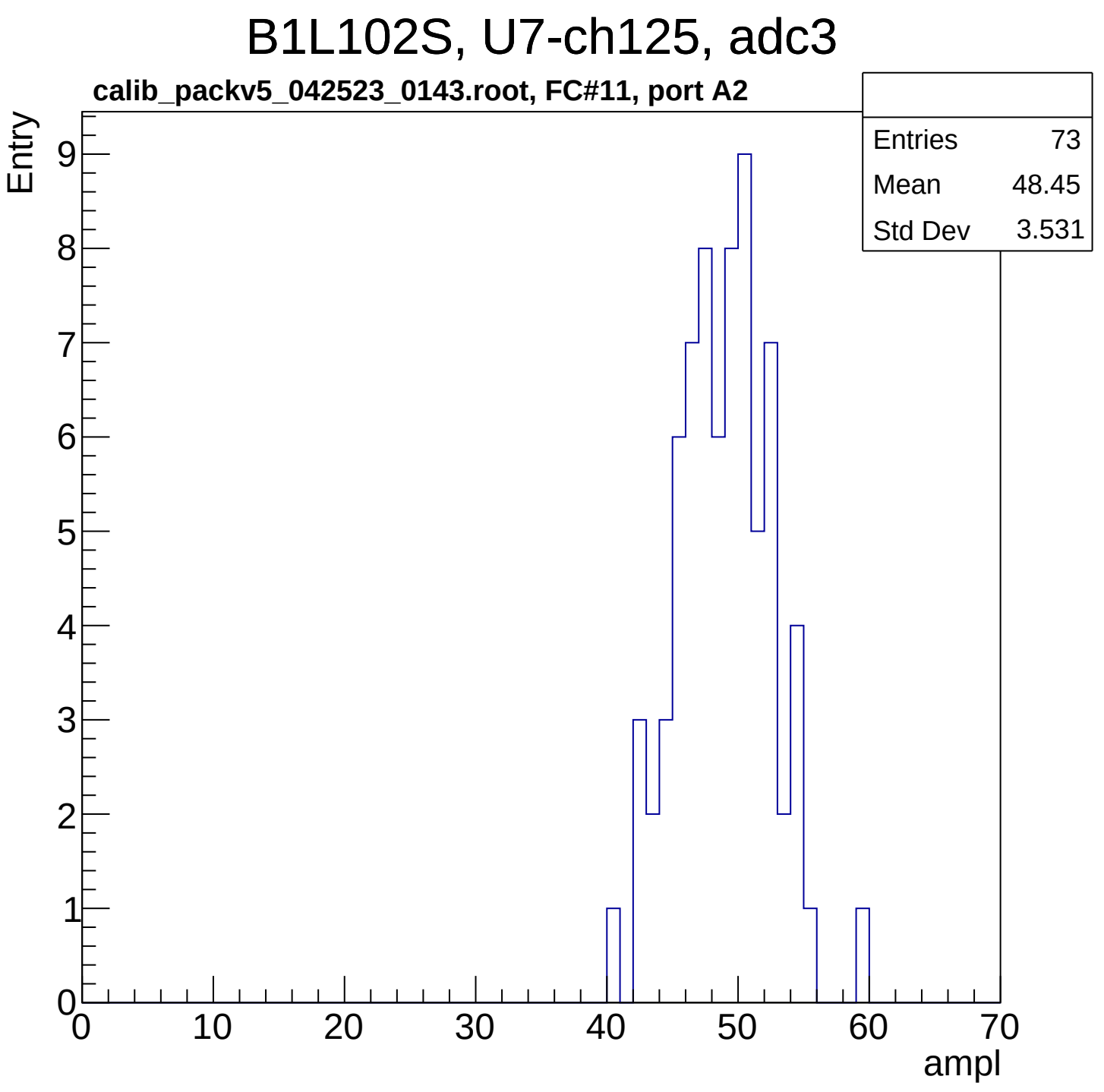

B1L102S, U7-ch124, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 14
Mean 57
Std Dev 15.84
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

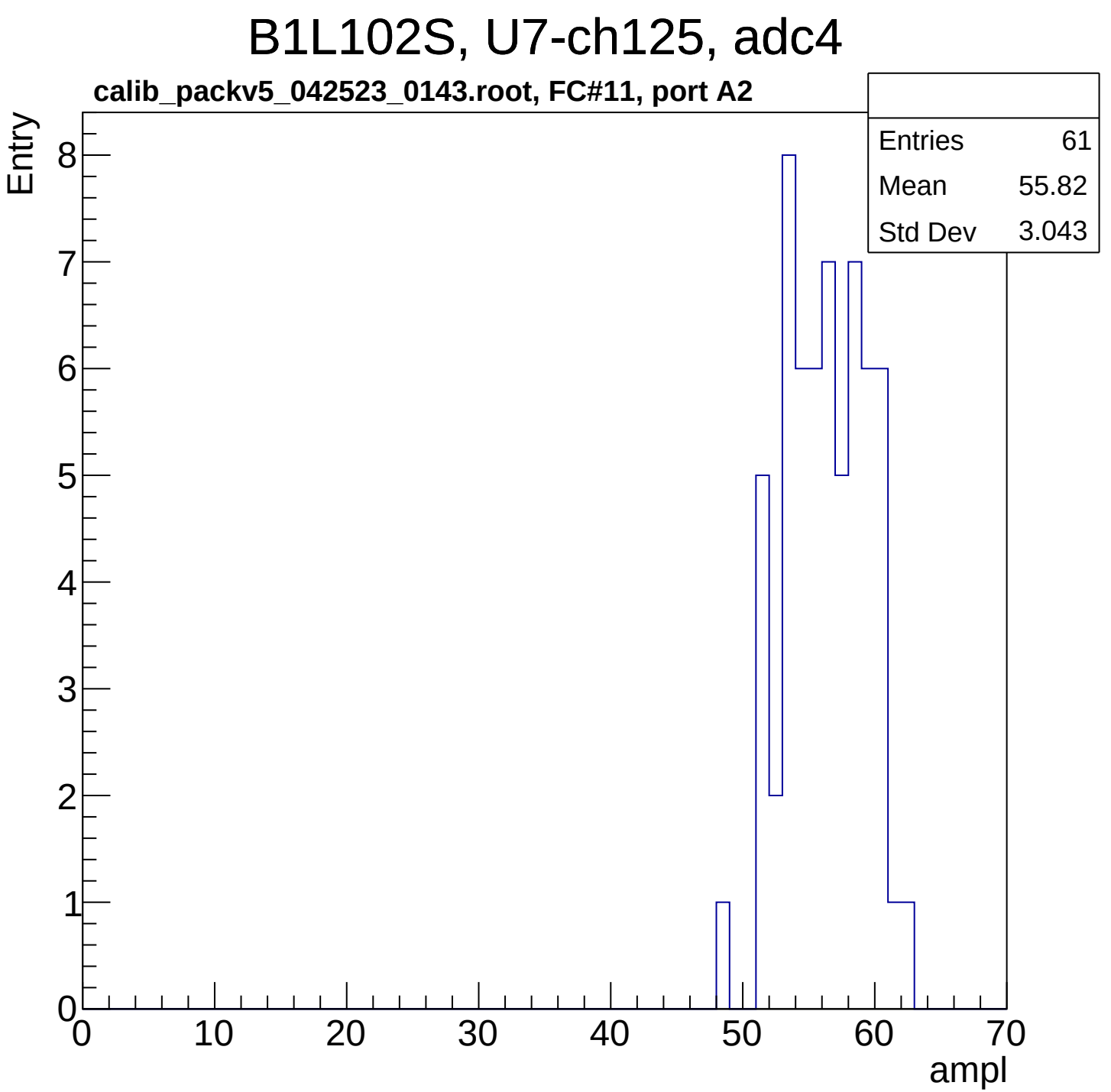

B1L102S, U7-ch124, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

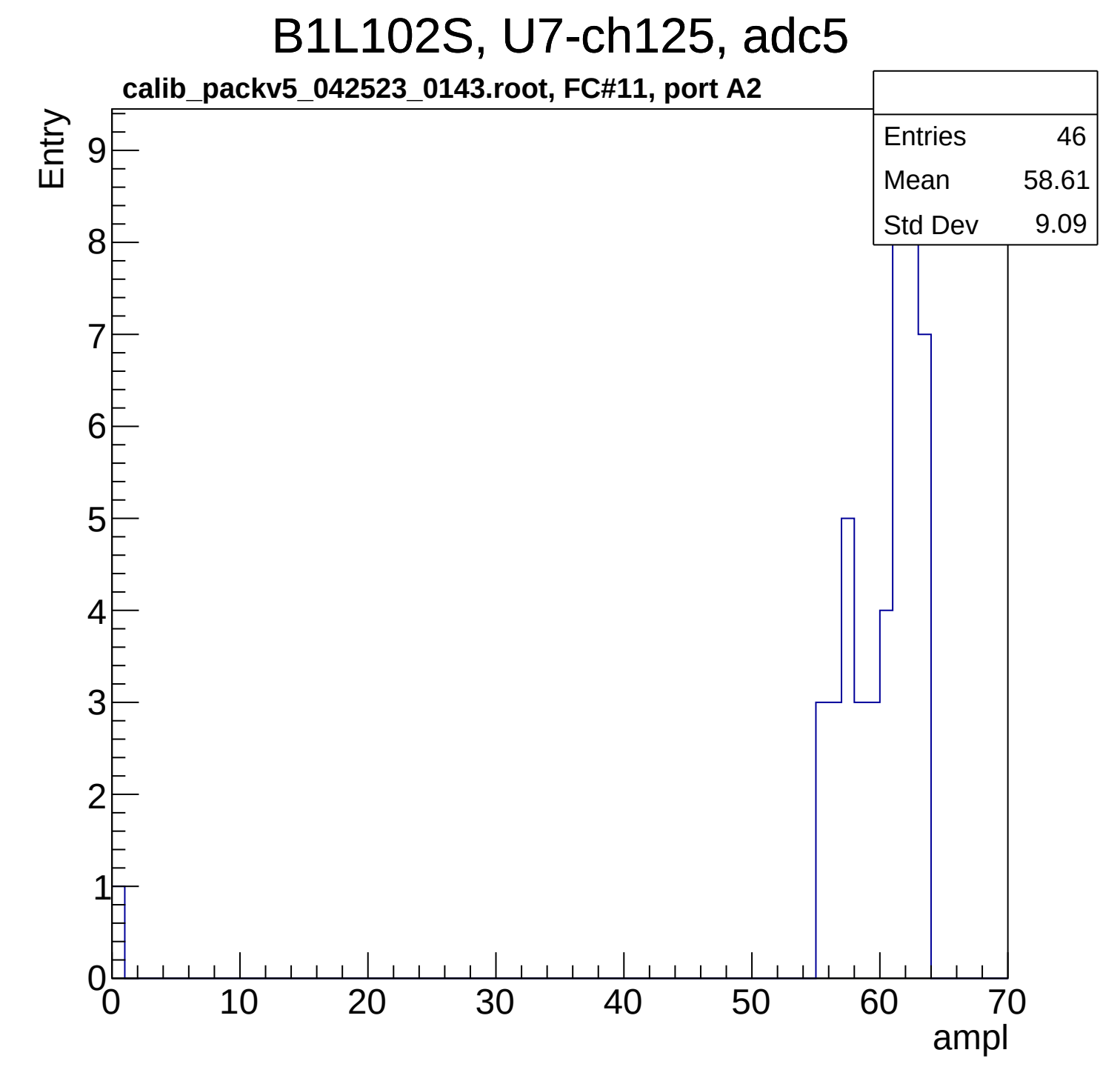

B1L102S, U7-ch125, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 80
Mean 26.86
Std Dev 6.484
Gaus mean : 28.6623
Gaus Width: 4.4658
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

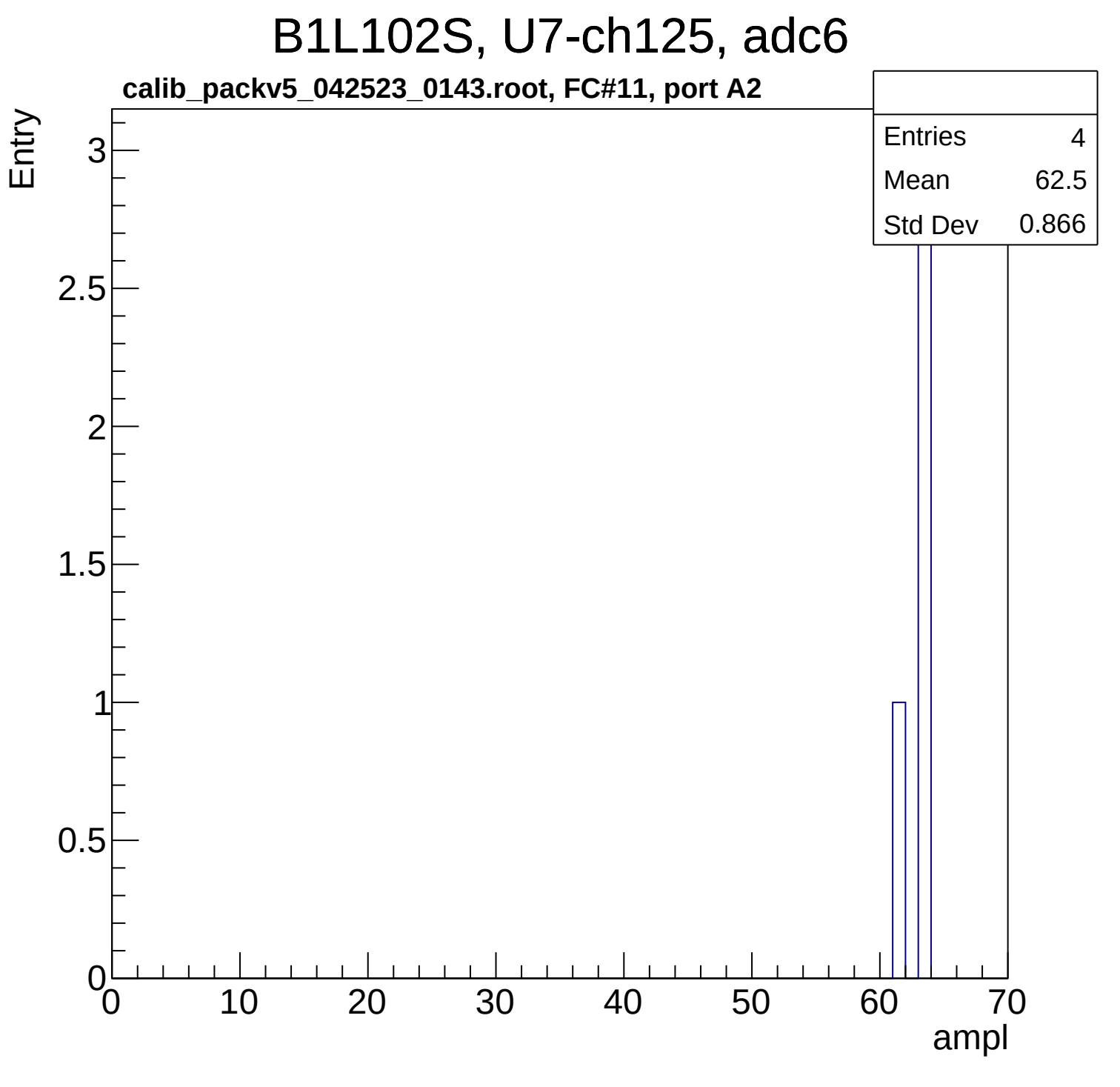

B1L102S, U7-ch125, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 52
Mean 34.46
Std Dev 3.29
Gaus mean : 35.1883
Gaus Width: 4.2456
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

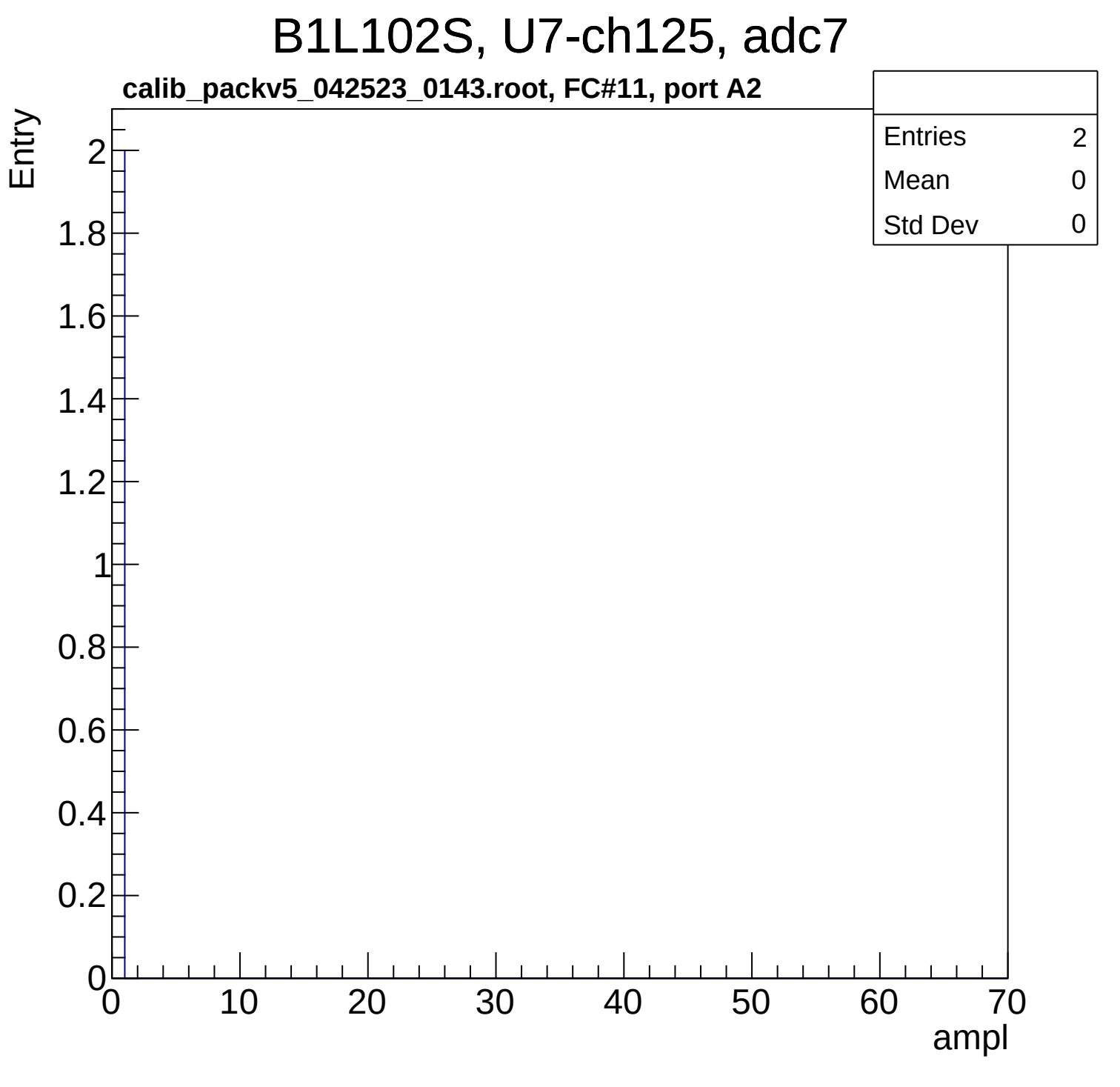

B1L102S, U7-ch125, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 81
Mean 41.32
Std Dev 4.139
Gaus mean : 41.9221
Gaus Width: 4.0956
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

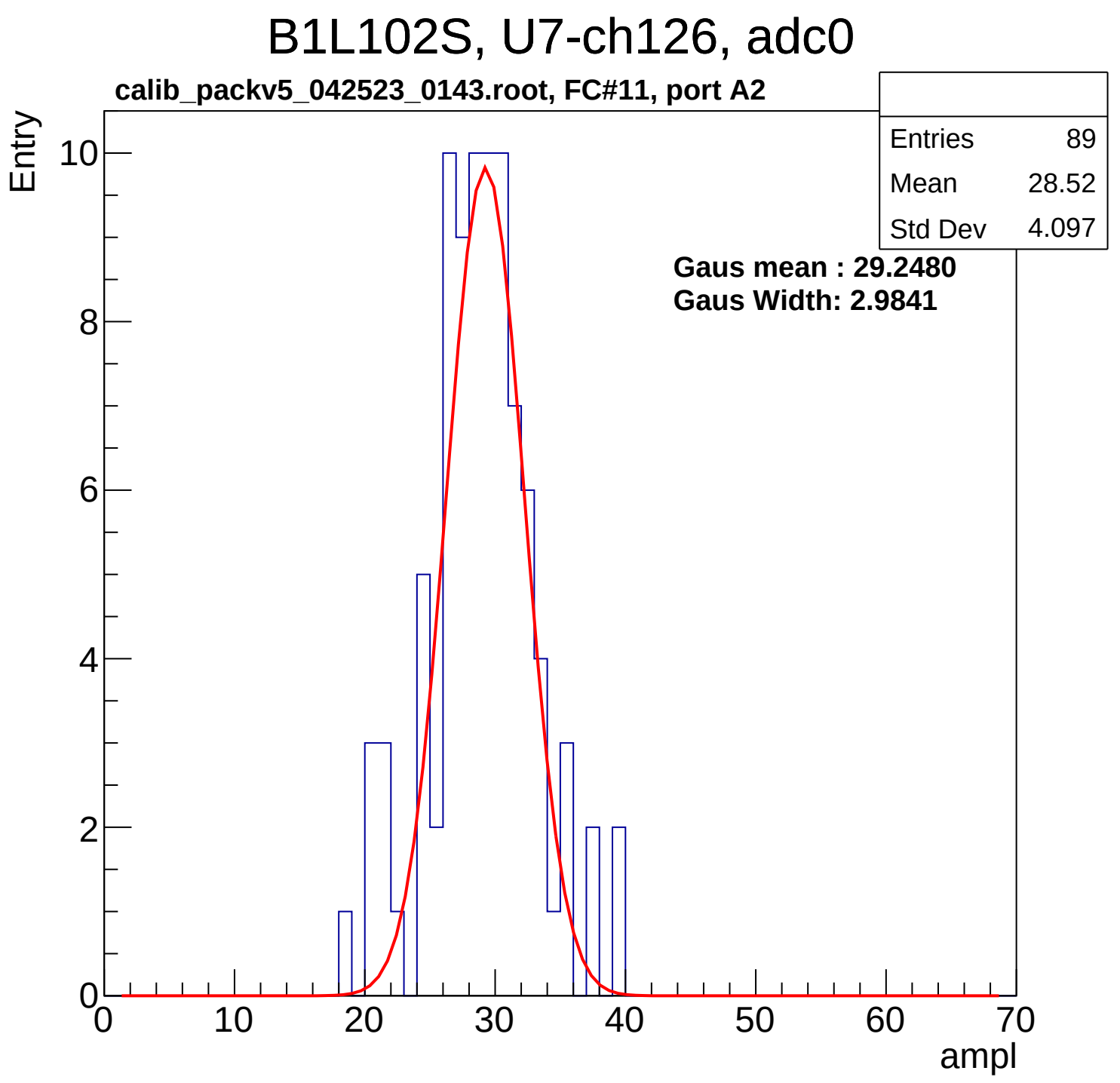

B1L102S, U7-ch125, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 73
Mean 48.45
Std Dev 3.531
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

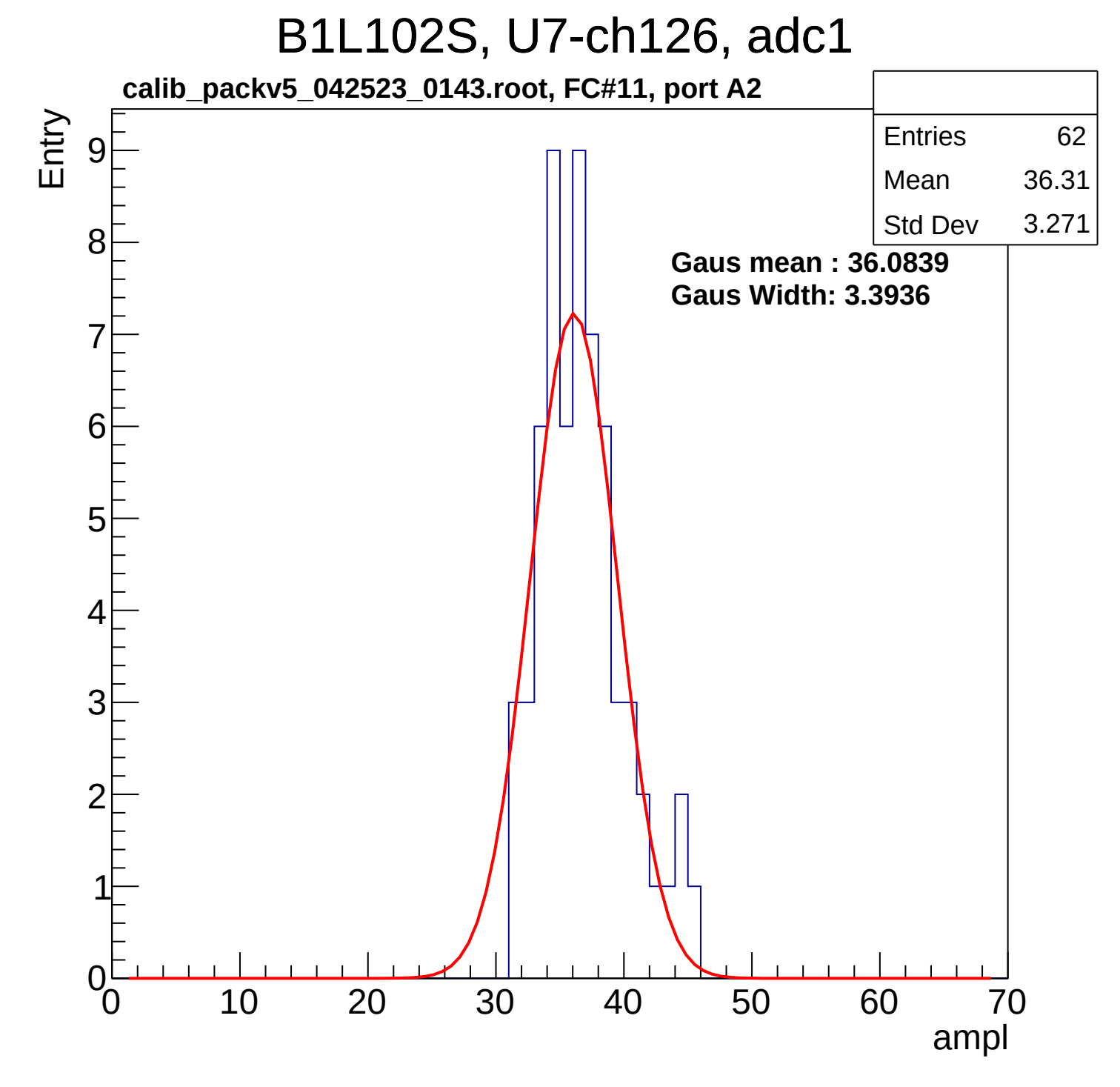

B1L102S, U7-ch125, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 61
Mean 55.82
Std Dev 3.043
Entry
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl

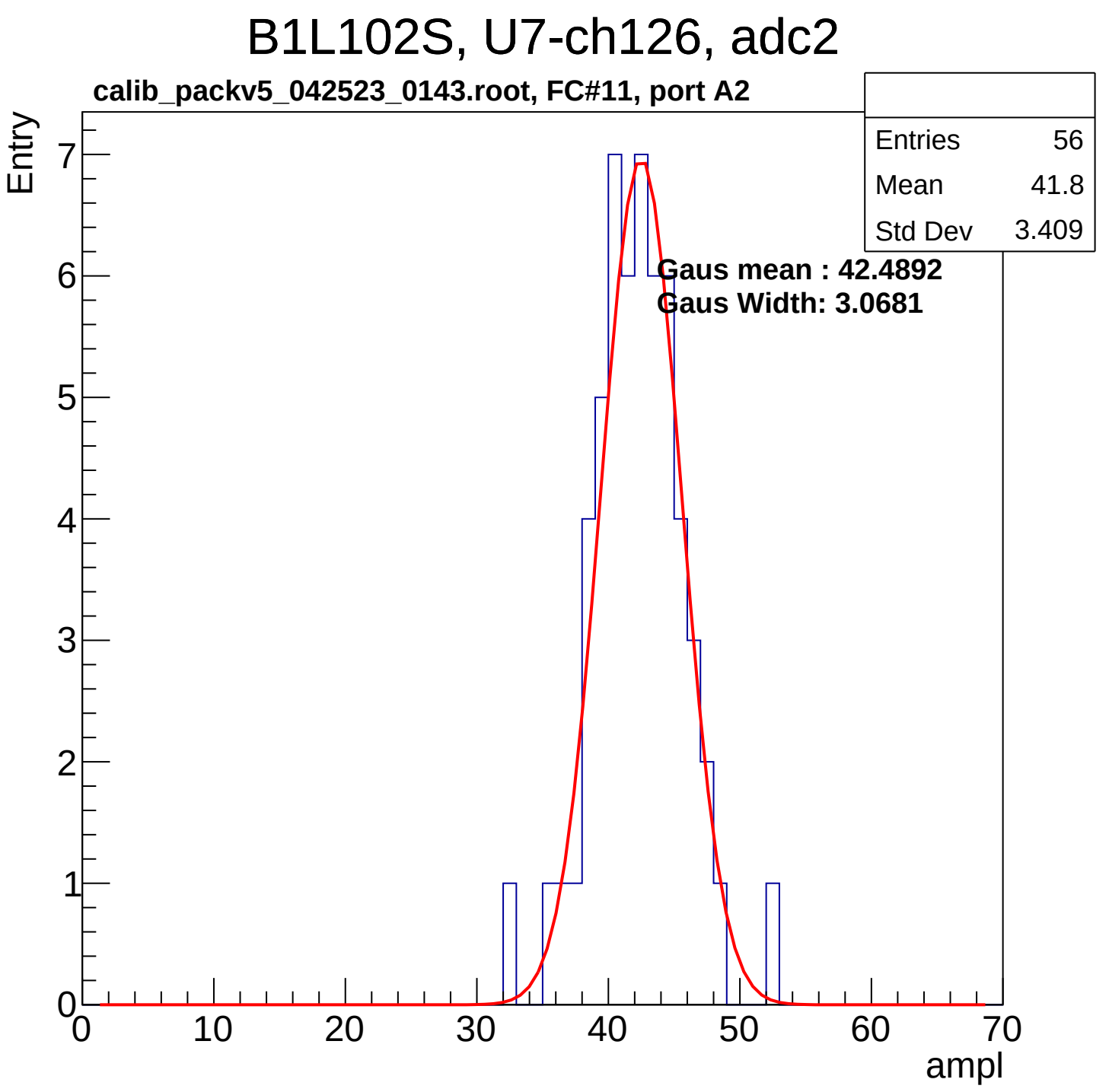

B1L102S, U7-ch125, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 46
Mean 58.61
Std Dev 9.09
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

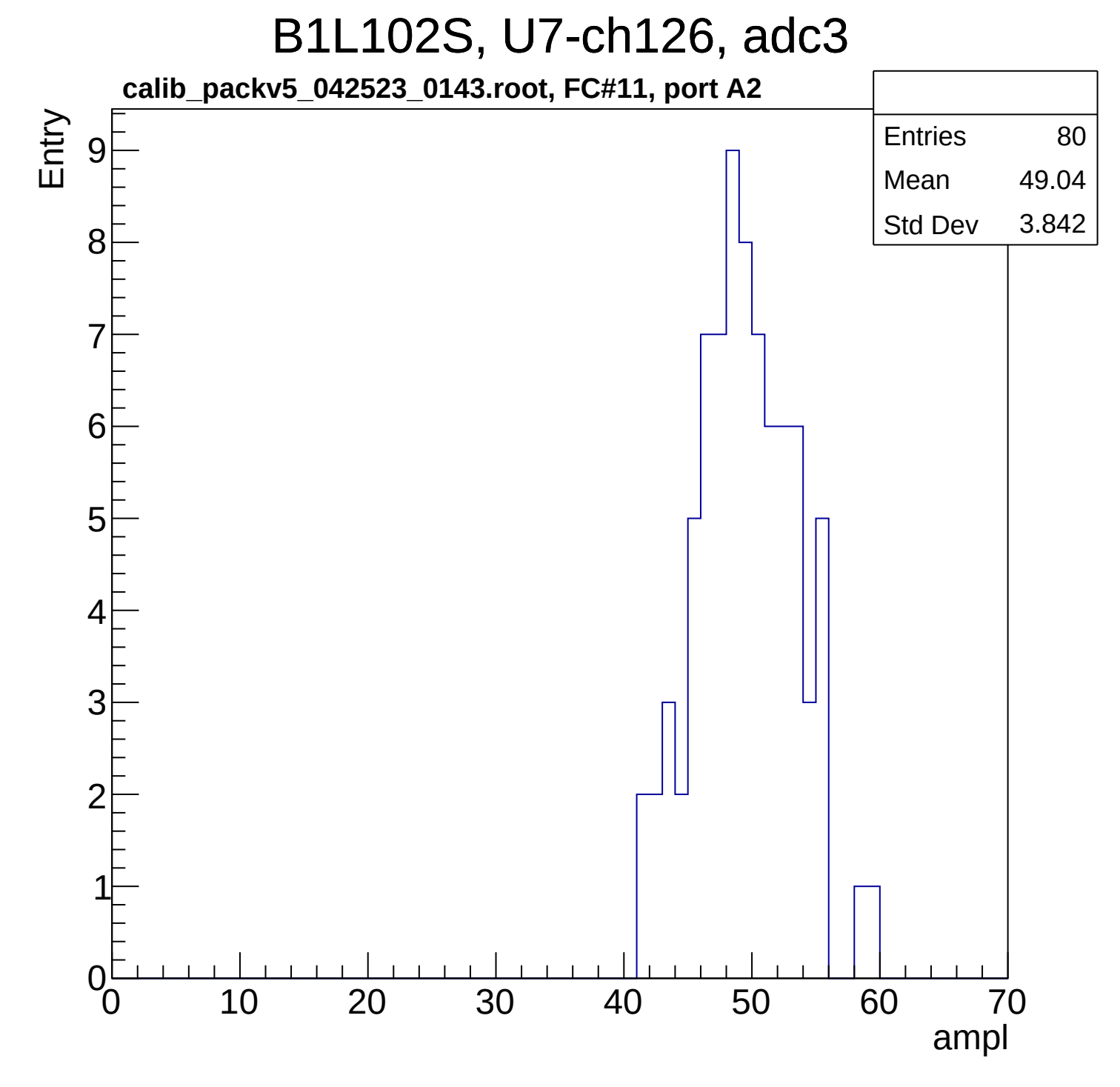

B1L102S, U7-ch125, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 4
Mean 62.5
Std Dev 0.866
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L102S, U7-ch125, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 2
Mean 0
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L102S, U7-ch126, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 89
Mean 28.52
Std Dev 4.097
Gaus mean : 29.2480
Gaus Width: 2.9841
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L102S, U7-ch126, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 62
Mean 36.31
Std Dev 3.271
Gaus mean : 36.0839
Gaus Width: 3.3936
Entry
ampl
0
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9


B1L102S, U7-ch126, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 56
Mean 41.8
Std Dev 3.409
Gaus mean : 42.4892
Gaus Width: 3.0681
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L102S, U7-ch126, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 80
Mean 49.04
Std Dev 3.842
Entry
ampl
0
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2
3
4
5
6
7
8
9
0
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30
40
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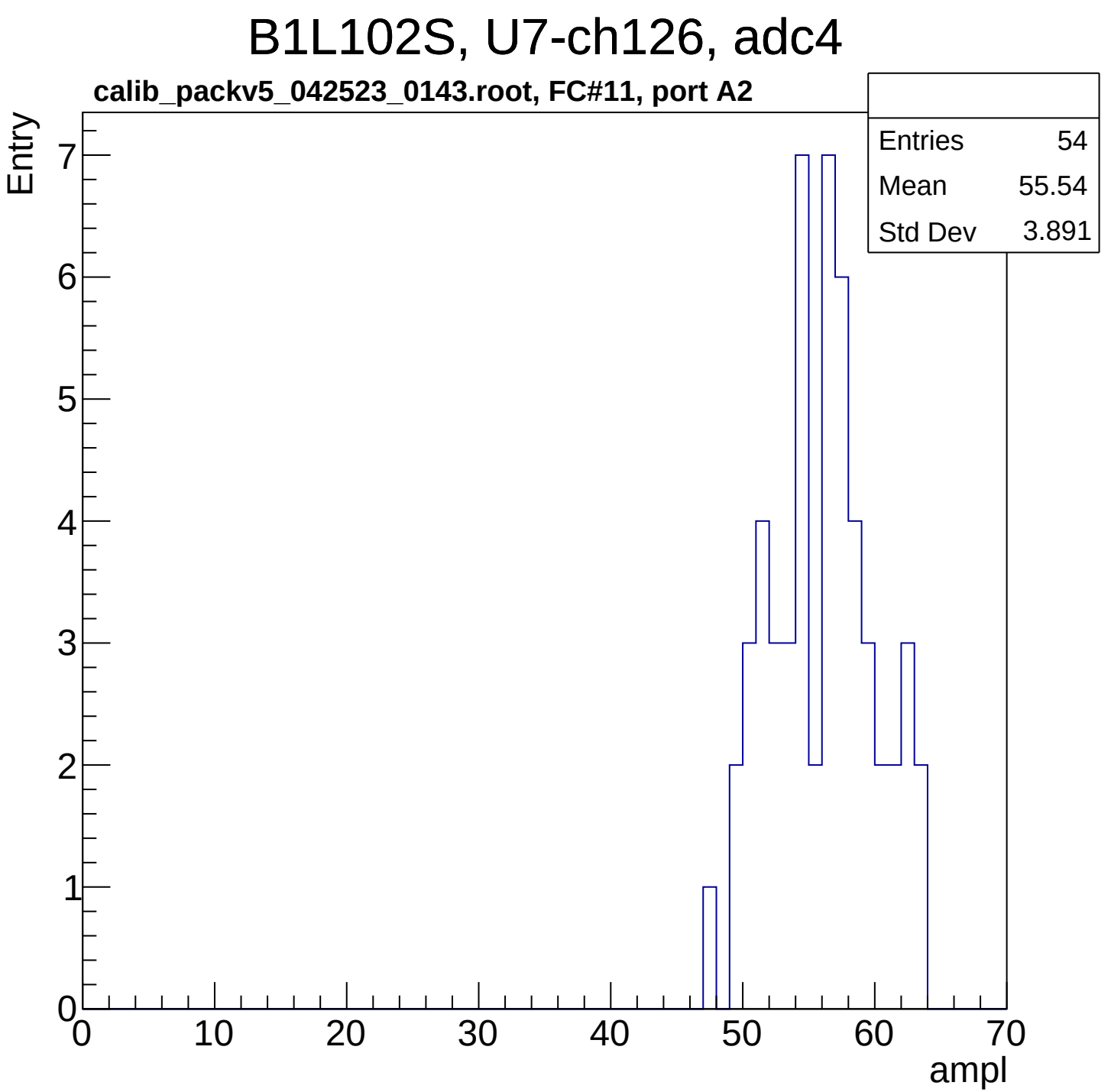
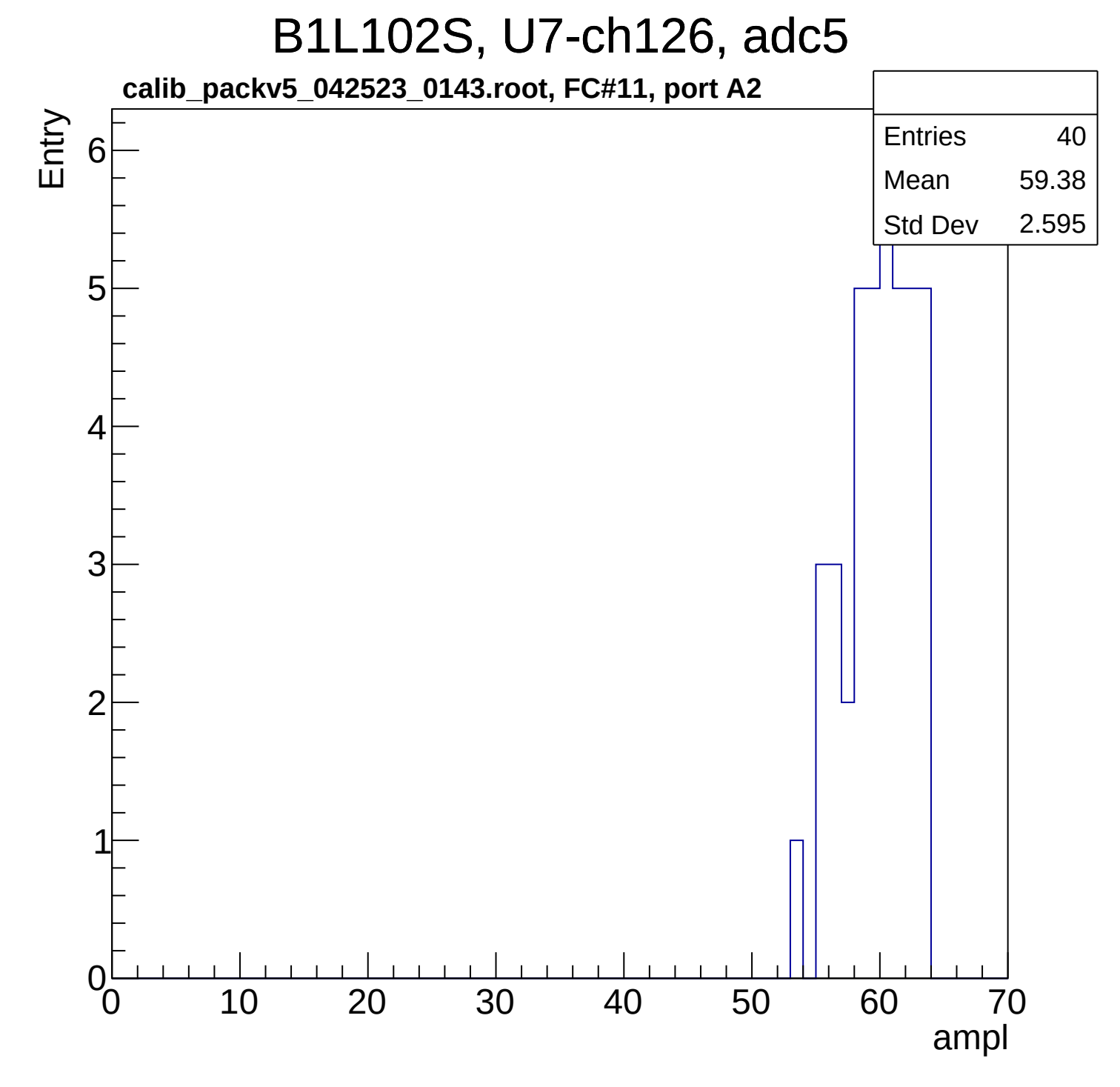
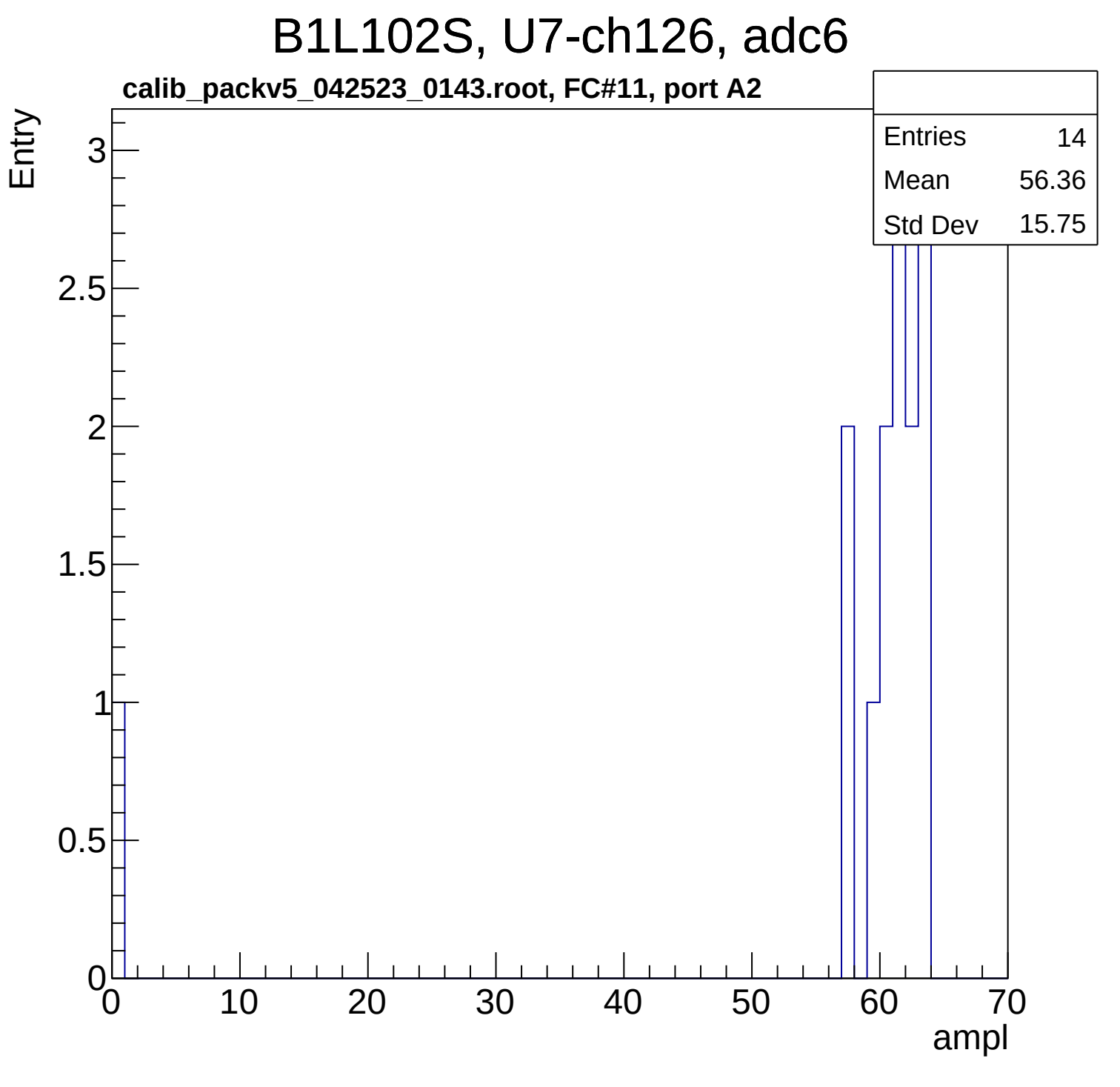
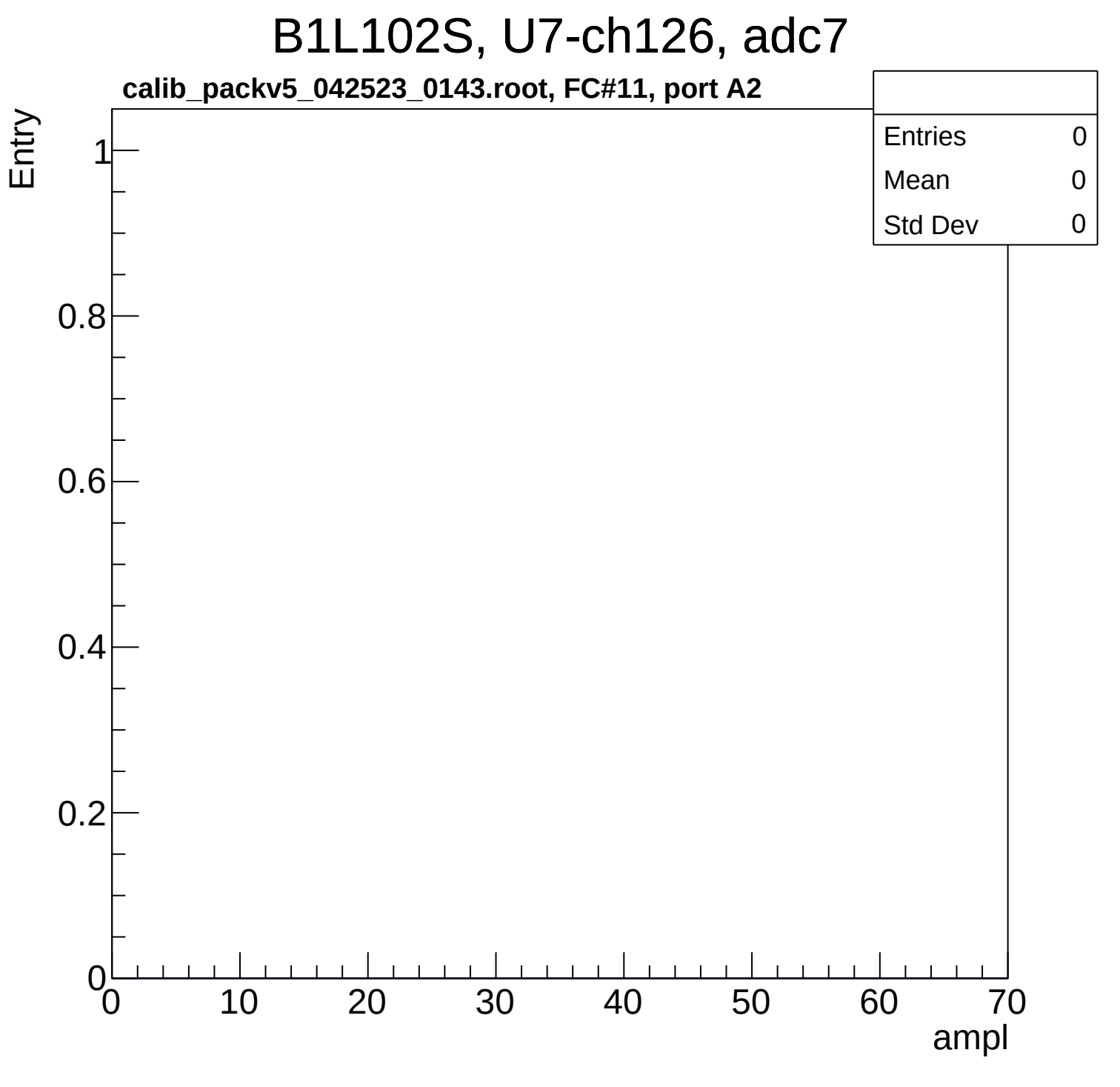
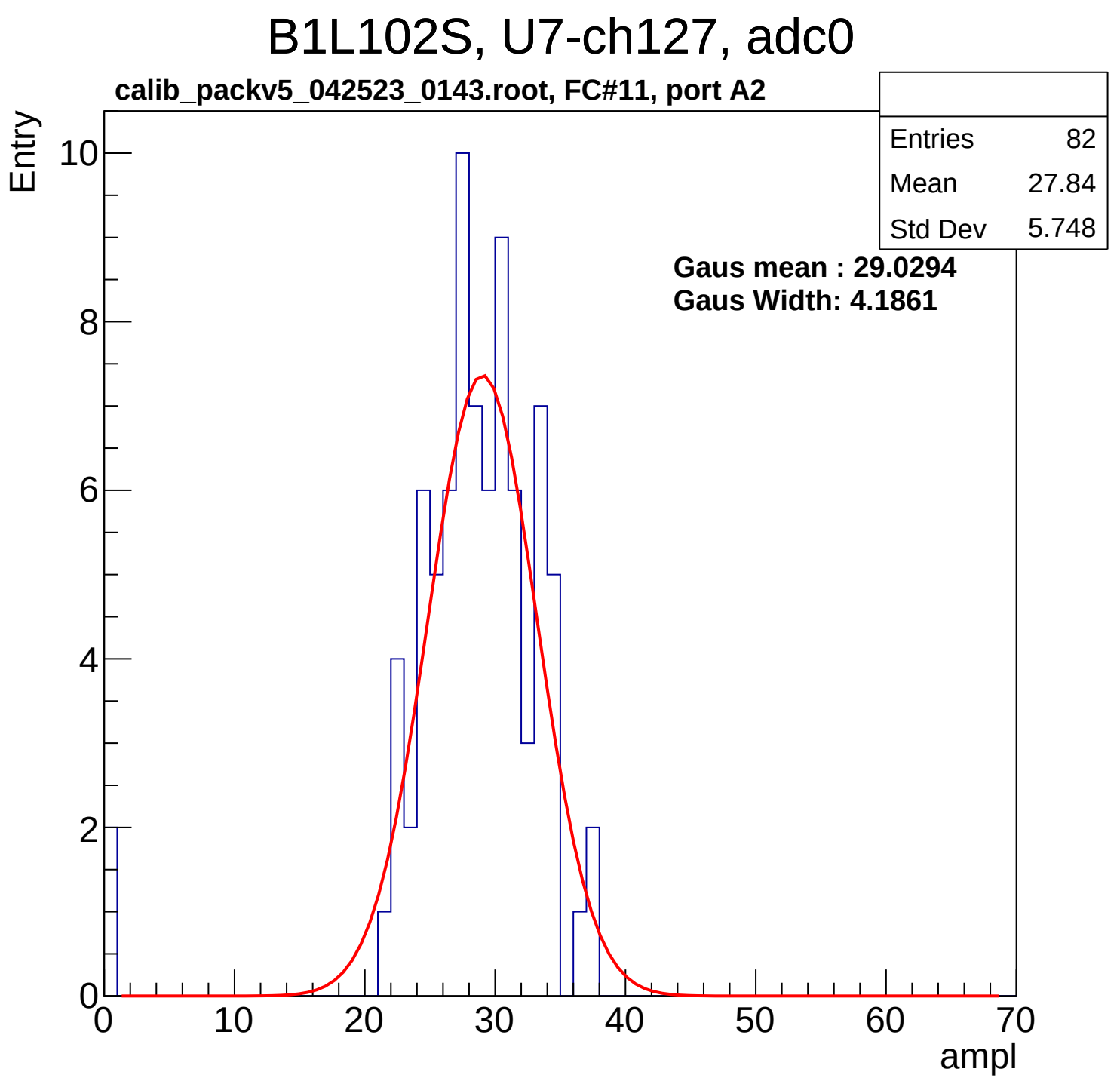
60
70

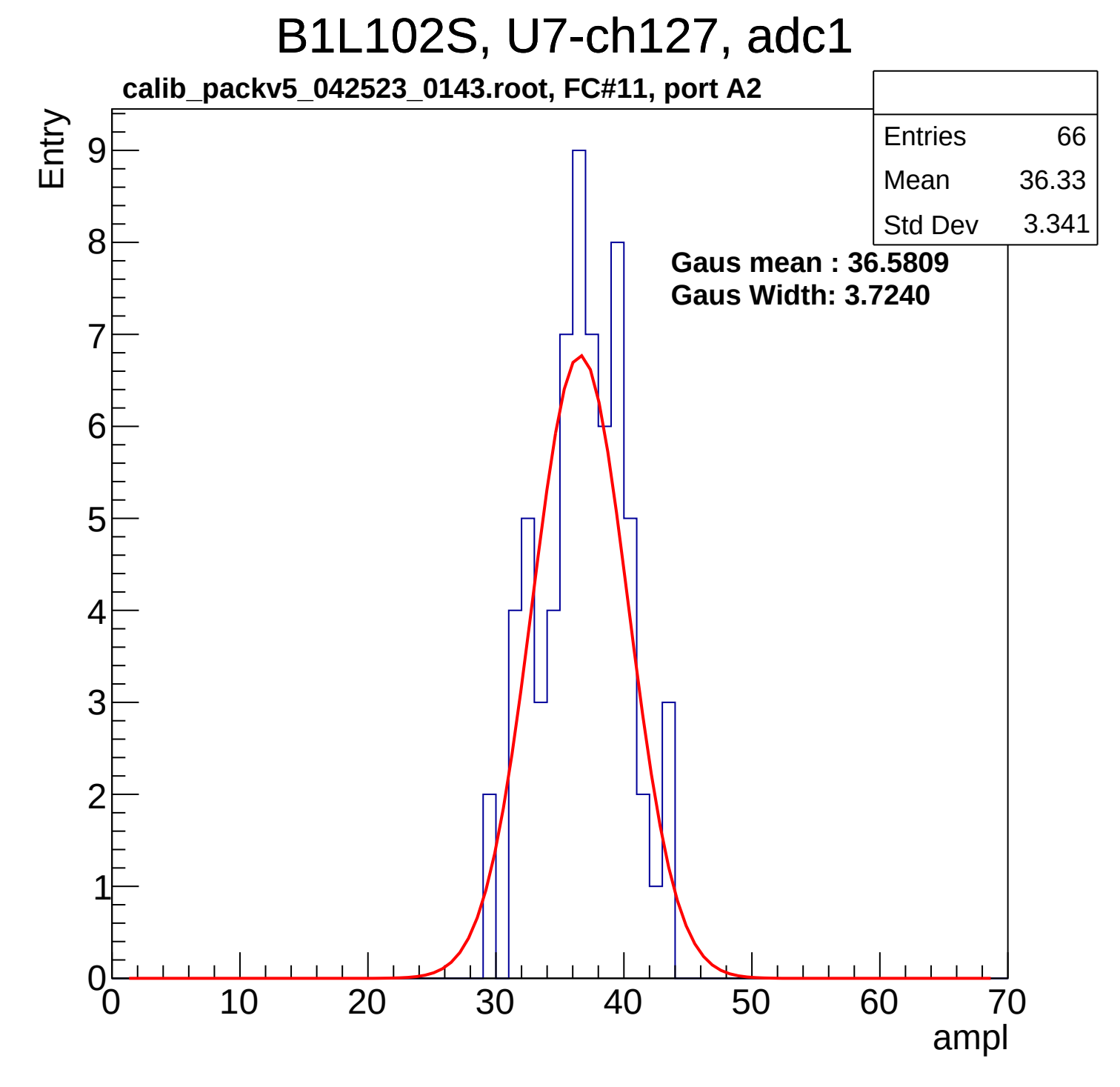

B1L102S, U7-ch126, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 54
Mean 55.54
Std Dev 3.891
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

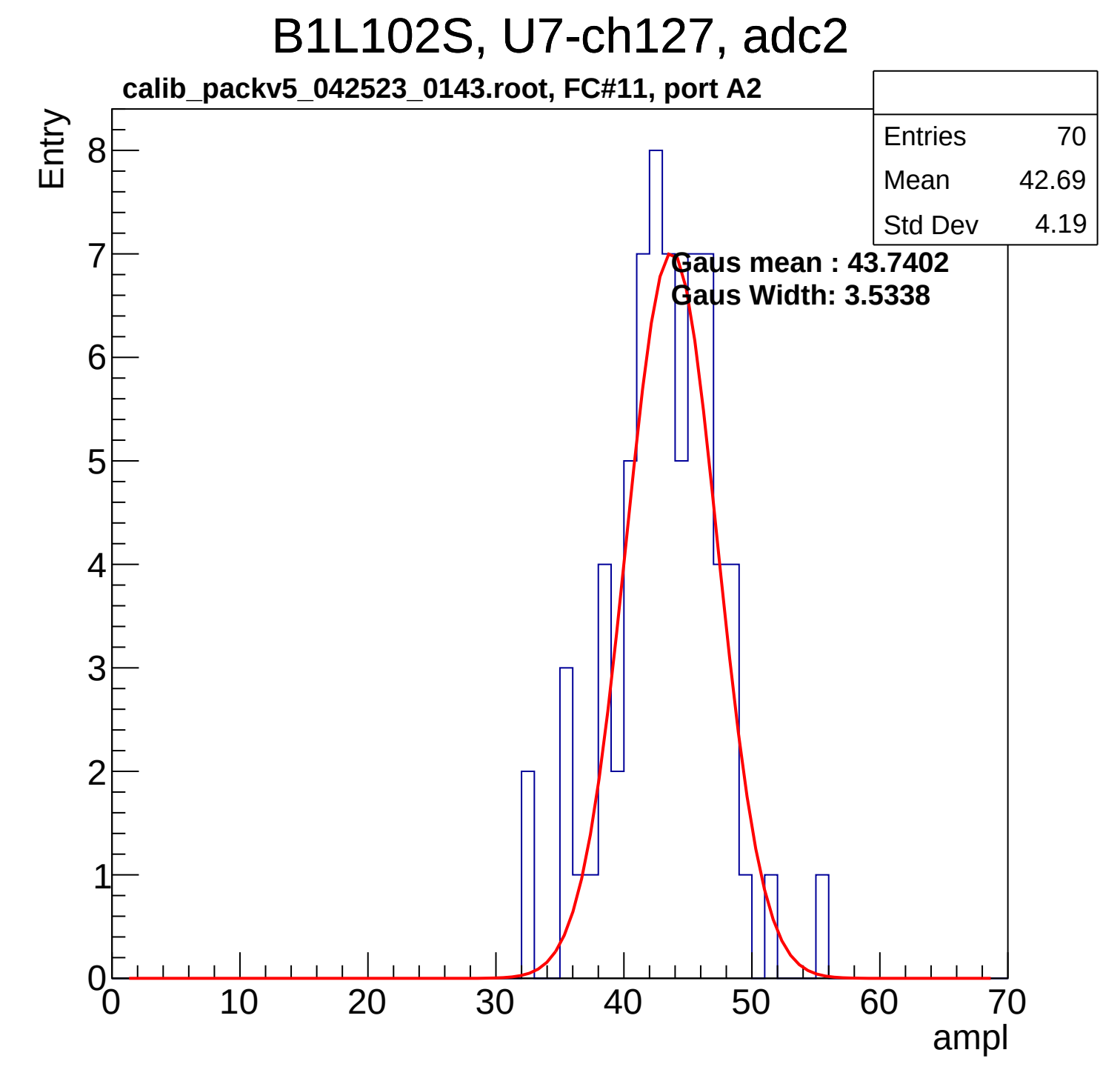

B1L102S, U7-ch126, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 40
Mean 59.38
Std Dev 2.595
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

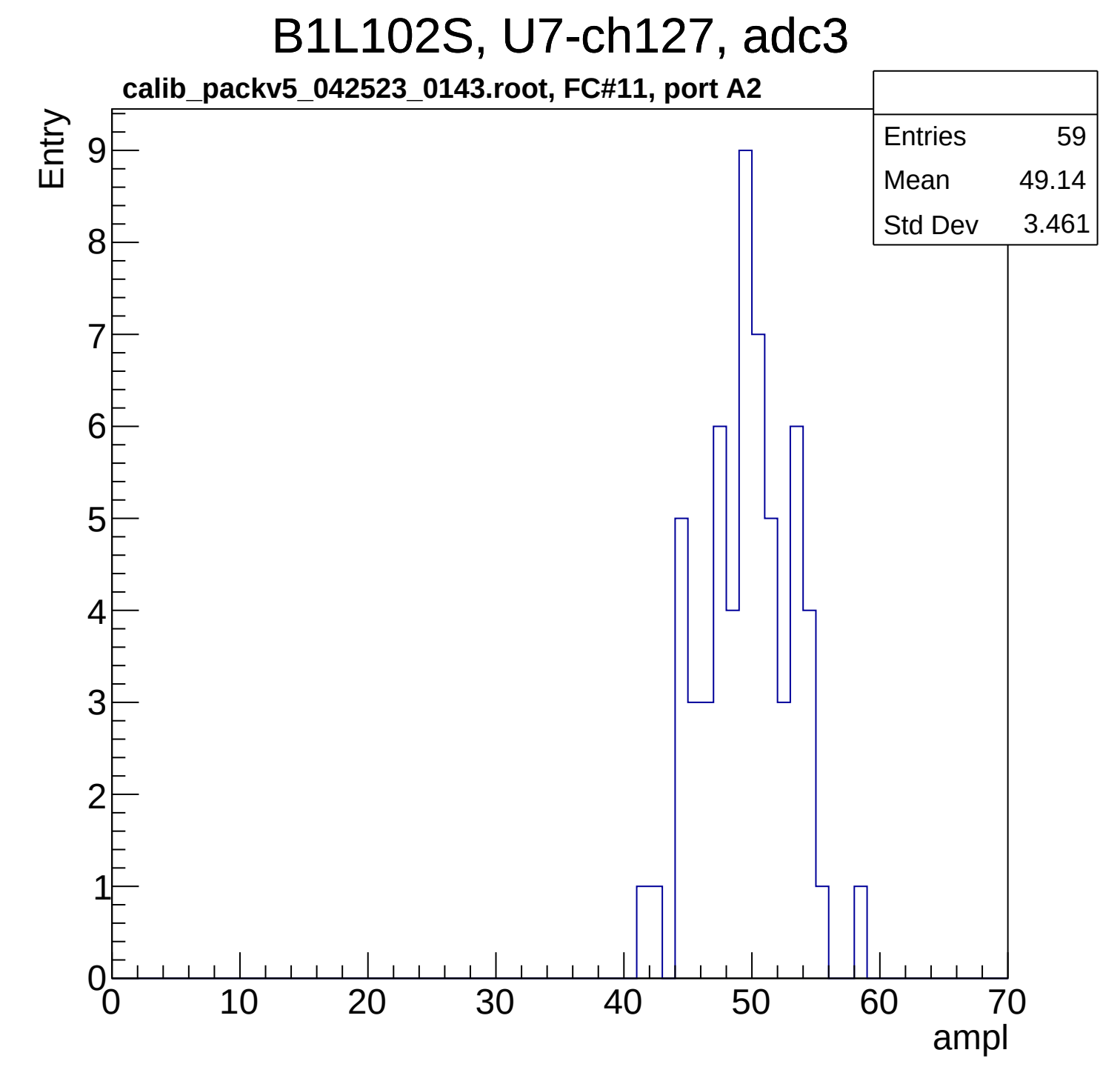

B1L102S, U7-ch126, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 14
Mean 56.36
Std Dev 15.75
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

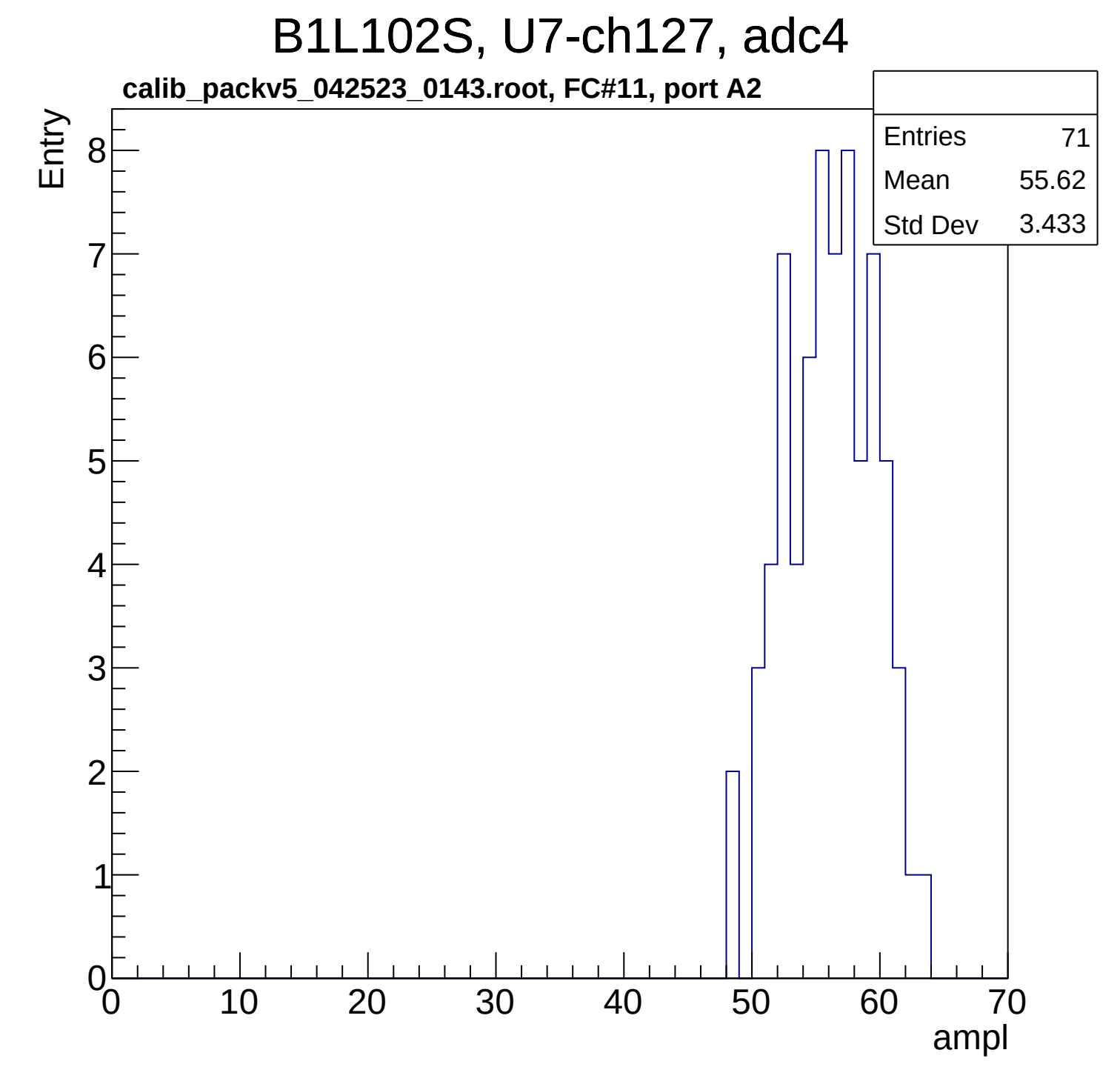

B1L102S, U7-ch126, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

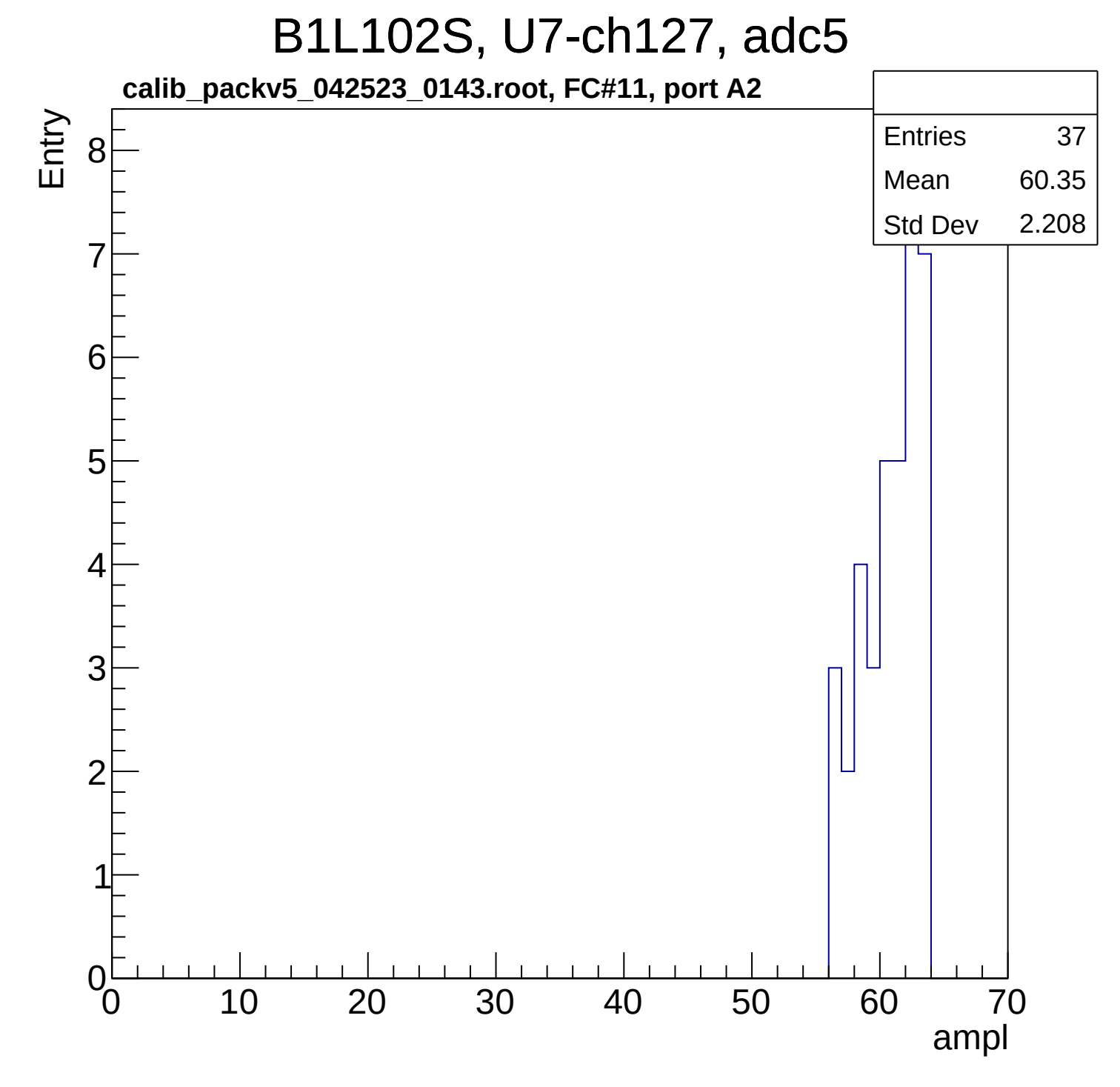

B1L102S, U7-ch127, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 82
Mean 27.84
Std Dev 5.748
Gaus mean : 29.0294
Gaus Width: 4.1861
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

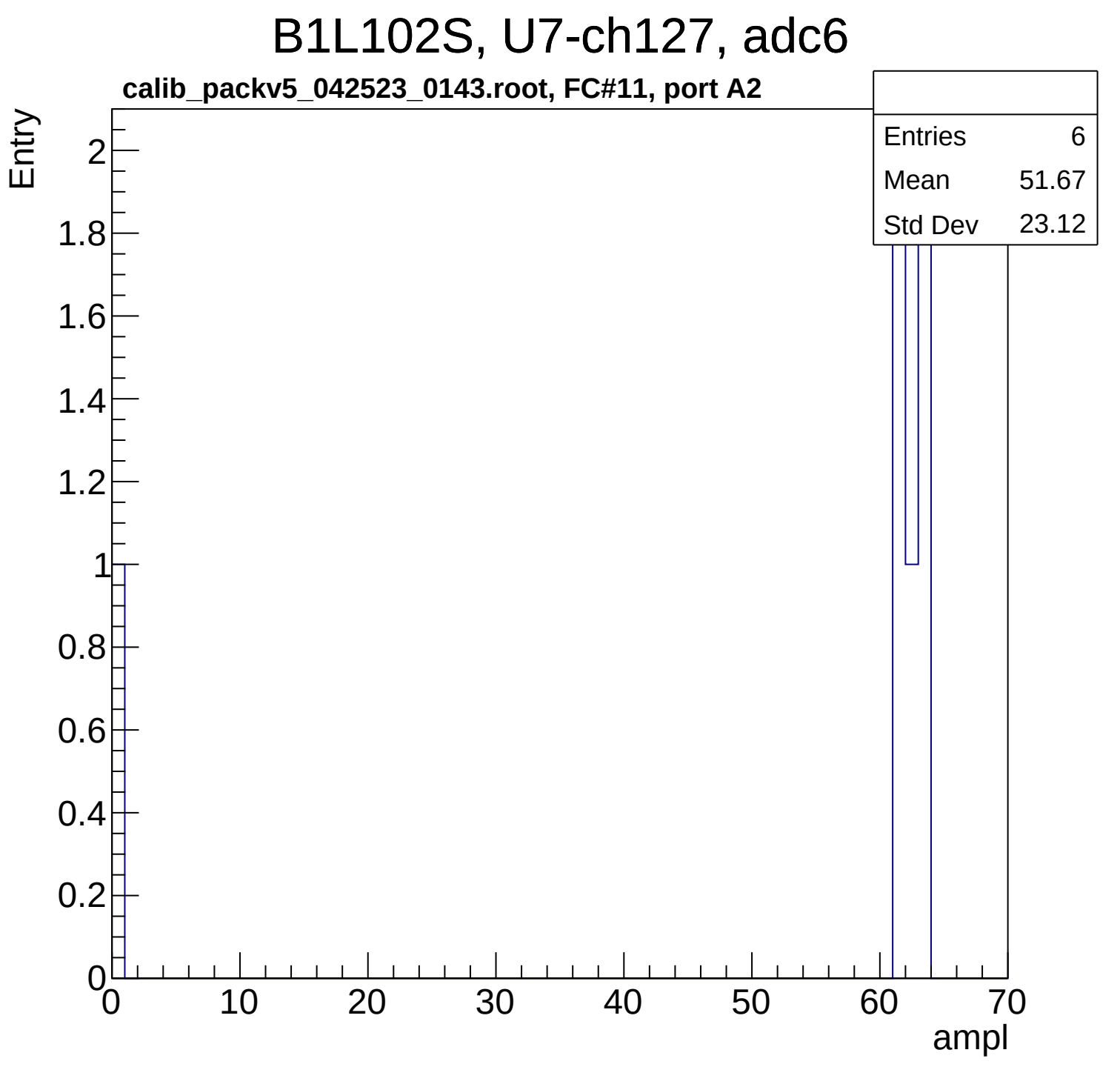

B1L102S, U7-ch127, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 66
Mean 36.33
Std Dev 3.341
Gaus mean : 36.5809
Gaus Width: 3.7240
Entry
ampl
0
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9

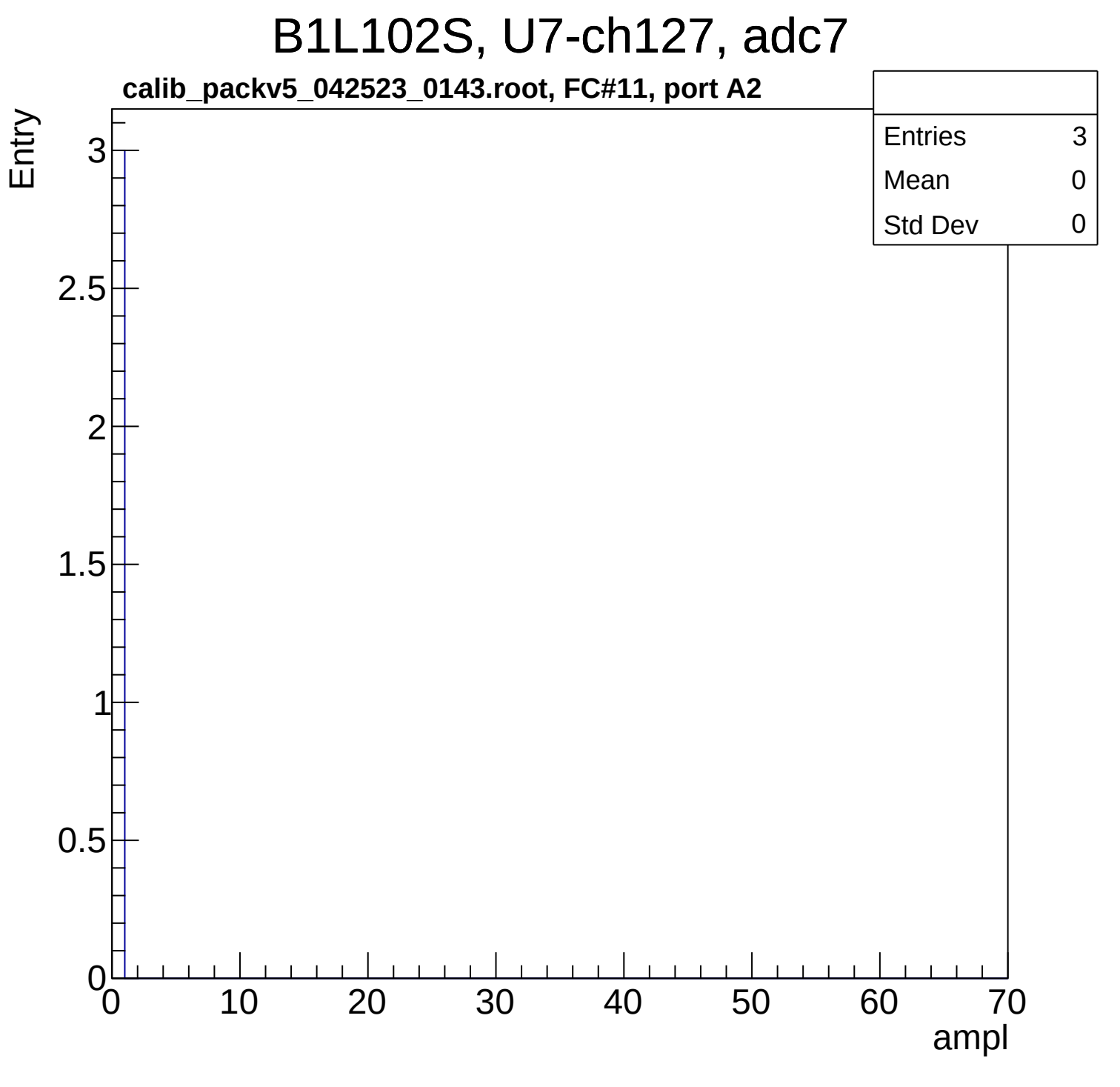

B1L102S, U7-ch127, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 70
Mean 42.69
Std Dev 4.19
Gaus mean : 43.7402
Gaus Width: 3.5338
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

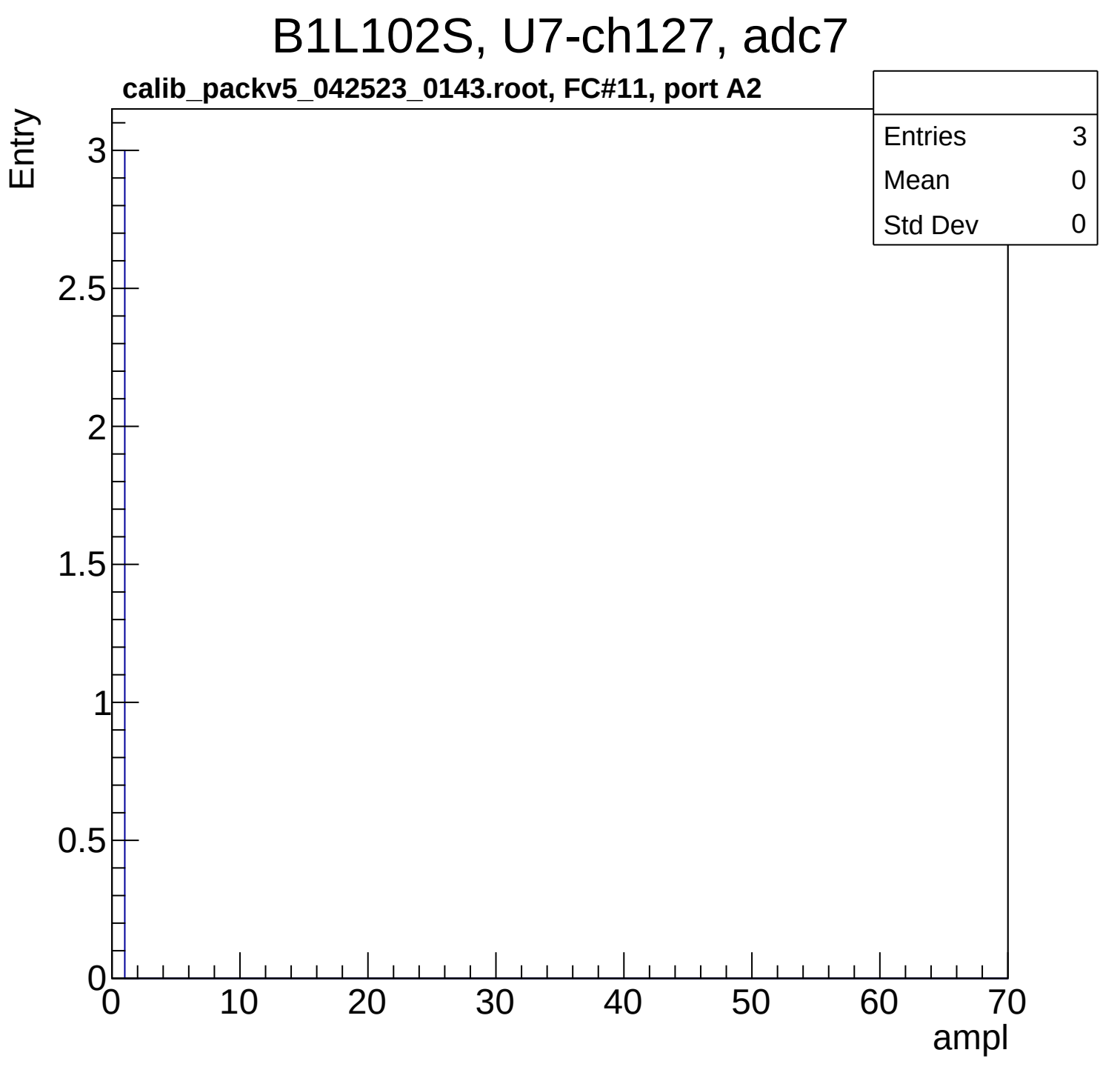

B1L102S, U7-ch127, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 59
Mean 49.14
Std Dev 3.461
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L102S, U7-ch127, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 71
Mean 55.62
Std Dev 3.433
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L102S, U7-ch127, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 37
Mean 60.35
Std Dev 2.208
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L102S, U7-ch127, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 6
Mean 51.67
Std Dev 23.12
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L102S, U7-ch127, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 3
Mean 0
Std Dev 0
Entry
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70
ampl


B1L102S, U7-ch127, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 3
Mean 0
Std Dev 0
Entry
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70
ampl