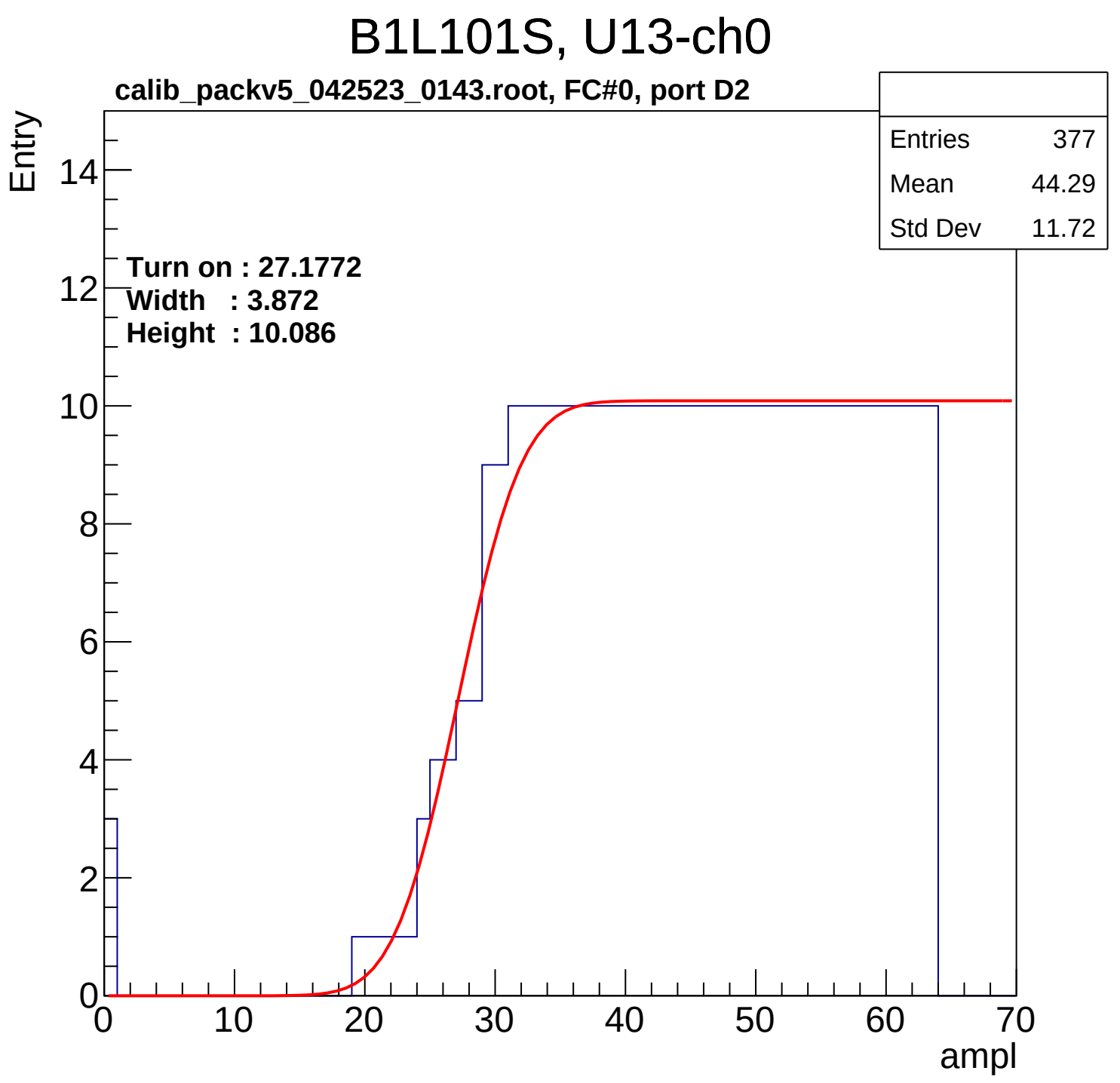
B1L101S, U13-ch0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 377
Mean 44.29
Std Dev 11.72
Turn on : 27.1772
Width : 3.872
Height : 10.086
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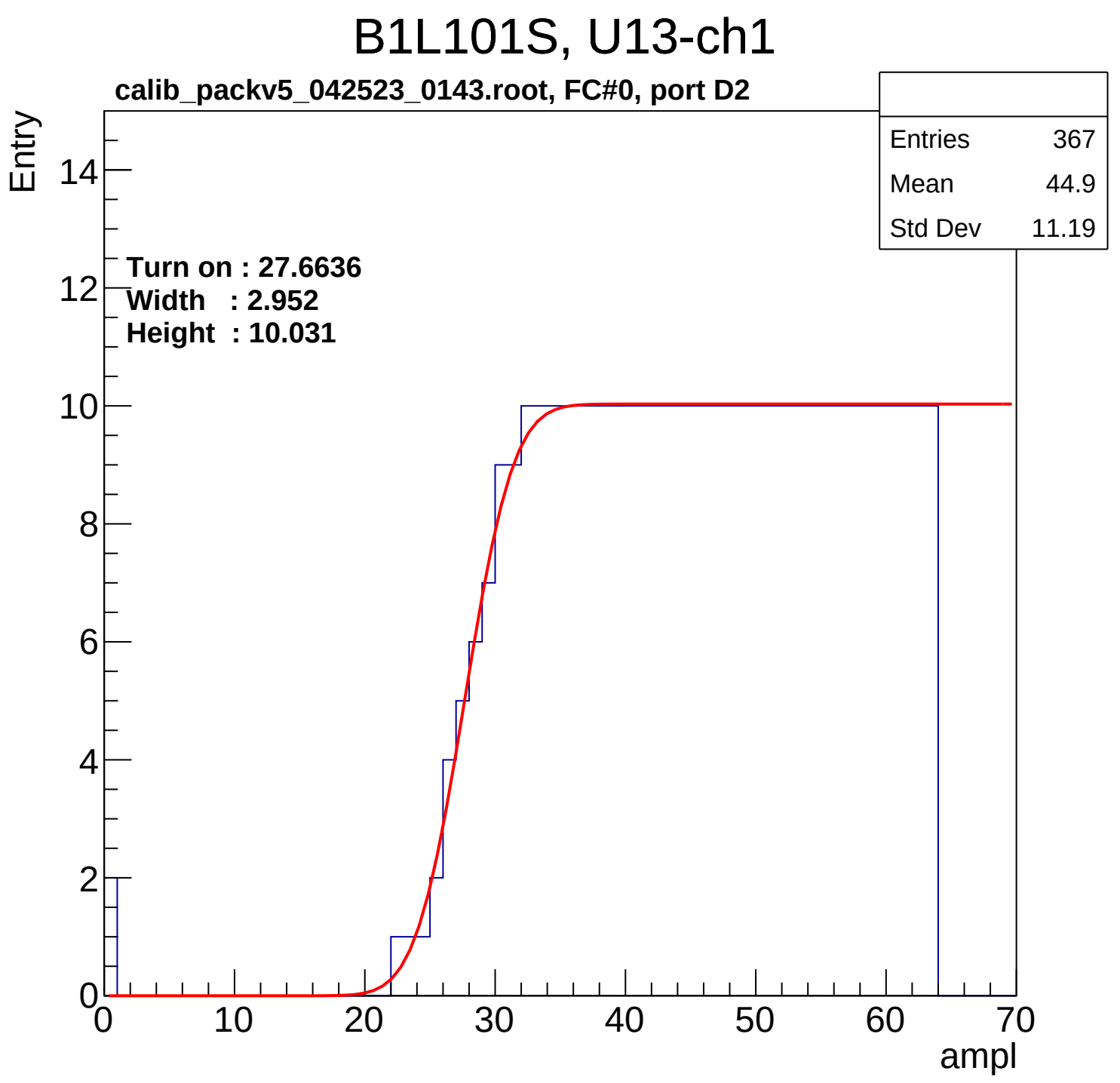
B1L101S, U13-ch1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 367
Mean 44.9
Std Dev 11.19
Turn on : 27.6636
Width : 2.952
Height : 10.031
Entry
ampl
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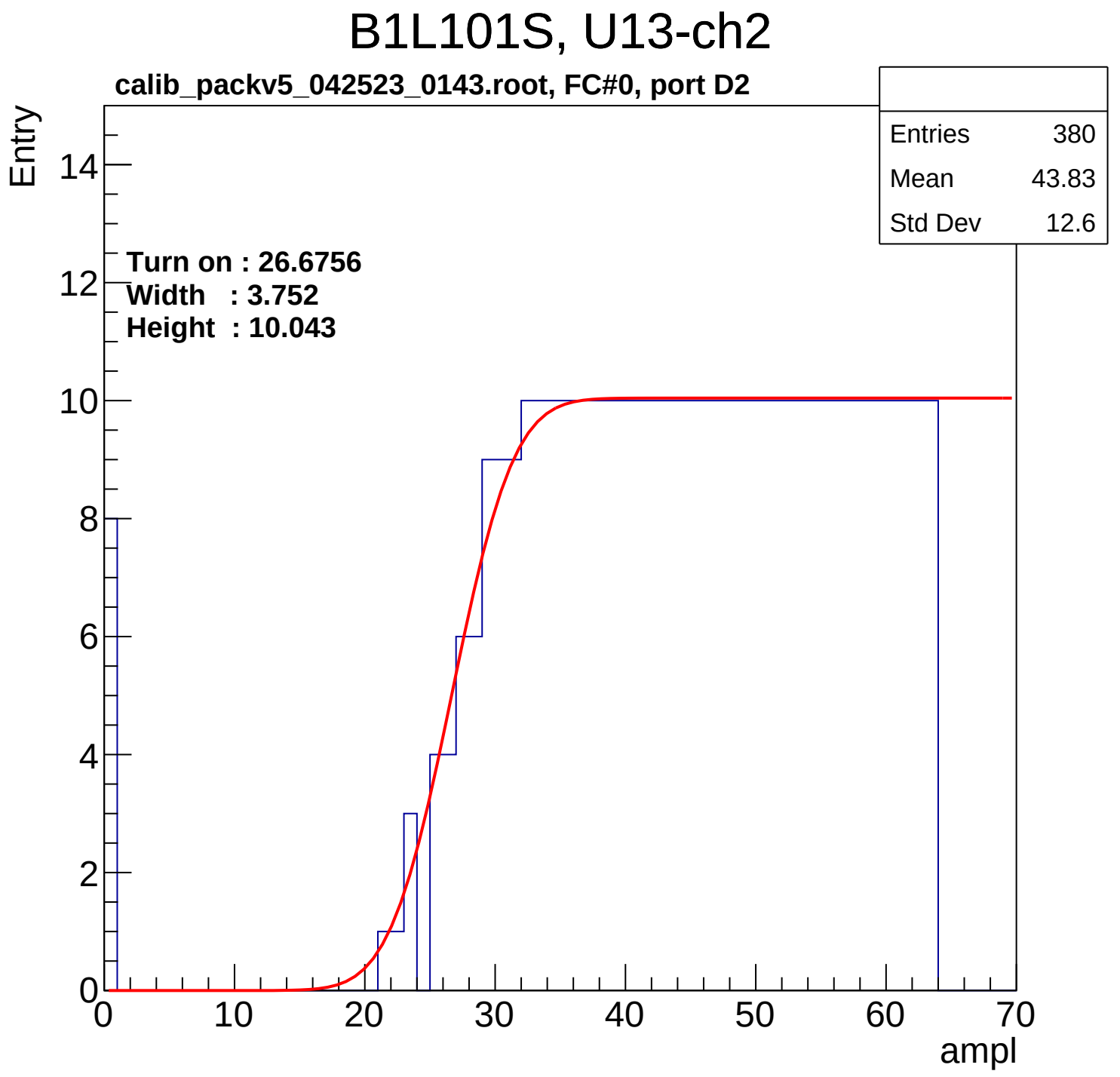
B1L101S, U13-ch2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 380
Mean 43.83
Std Dev 12.6
Turn on : 26.6756
Width : 3.752
Height : 10.043
Entry
ampl
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6
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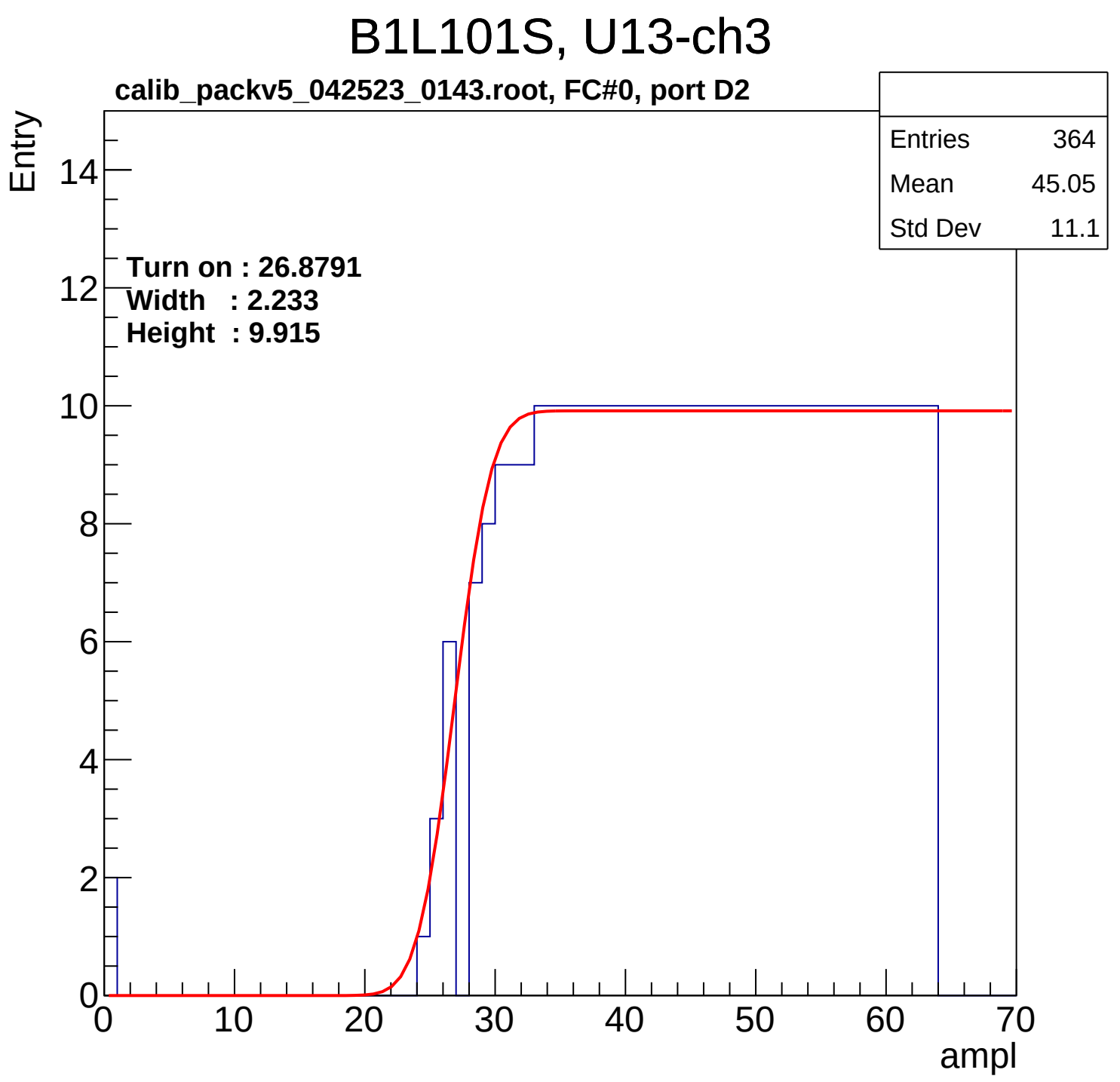
B1L101S, U13-ch3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 364
Mean 45.05
Std Dev 11.1
Turn on : 26.8791
Width : 2.233
Height : 9.915
Entry
ampl
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2
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6
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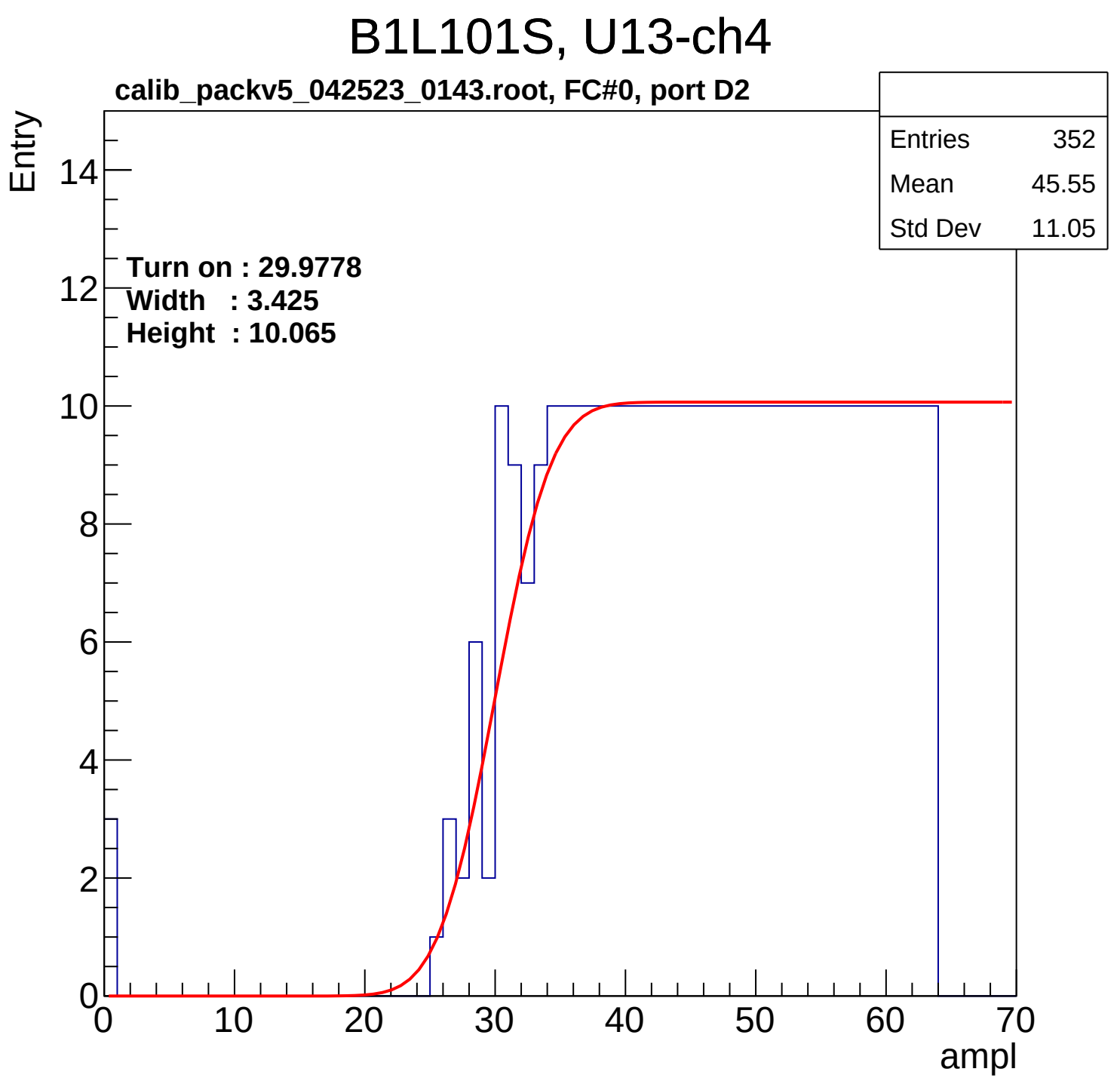
B1L101S, U13-ch4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 352
Mean 45.55
Std Dev 11.05
Turn on : 29.9778
Width : 3.425
Height : 10.065
Entry
ampl
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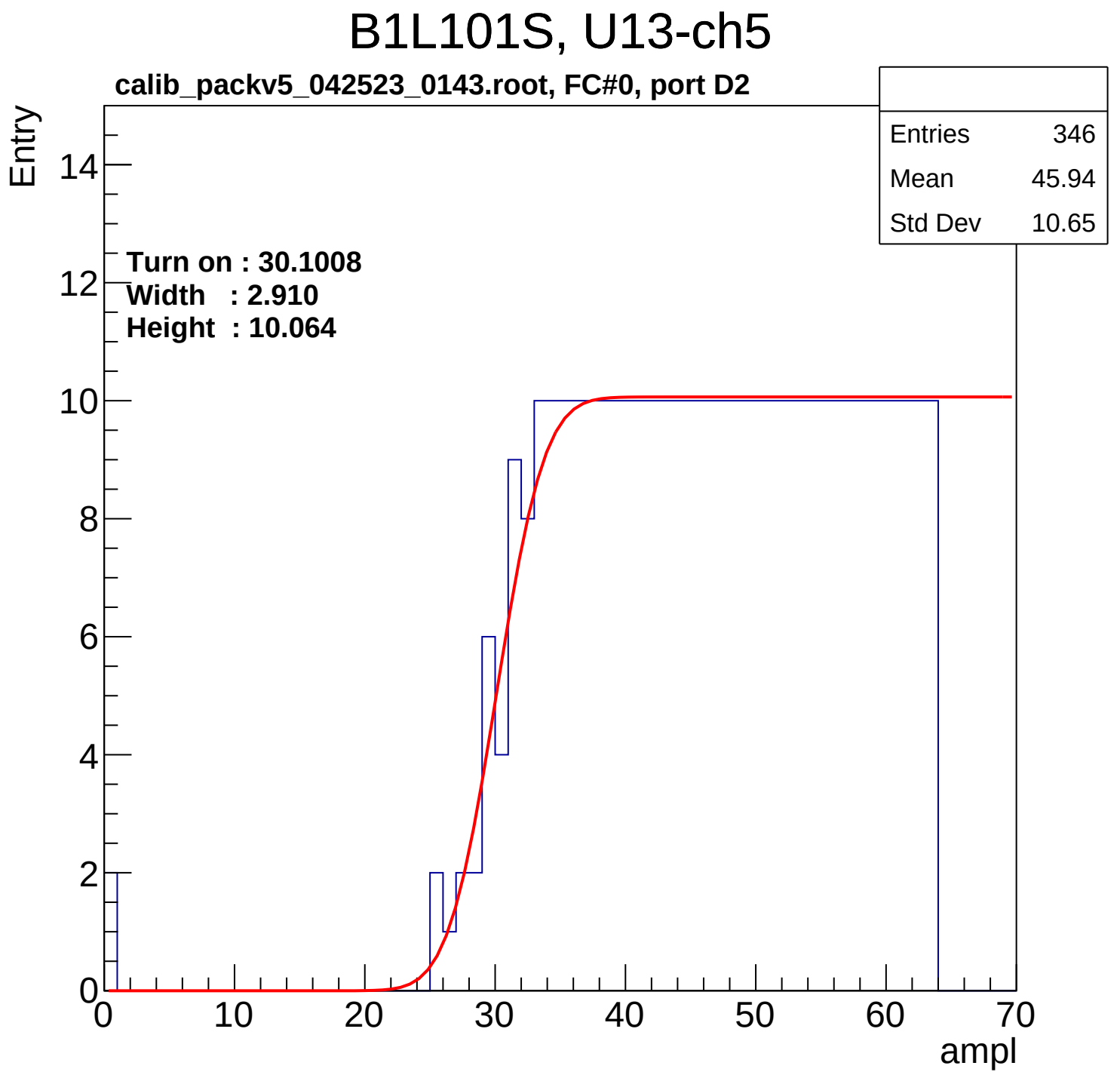
B1L101S, U13-ch5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 346
Mean 45.94
Std Dev 10.65
Turn on : 30.1008
Width : 2.910
Height : 10.064
Entry
ampl
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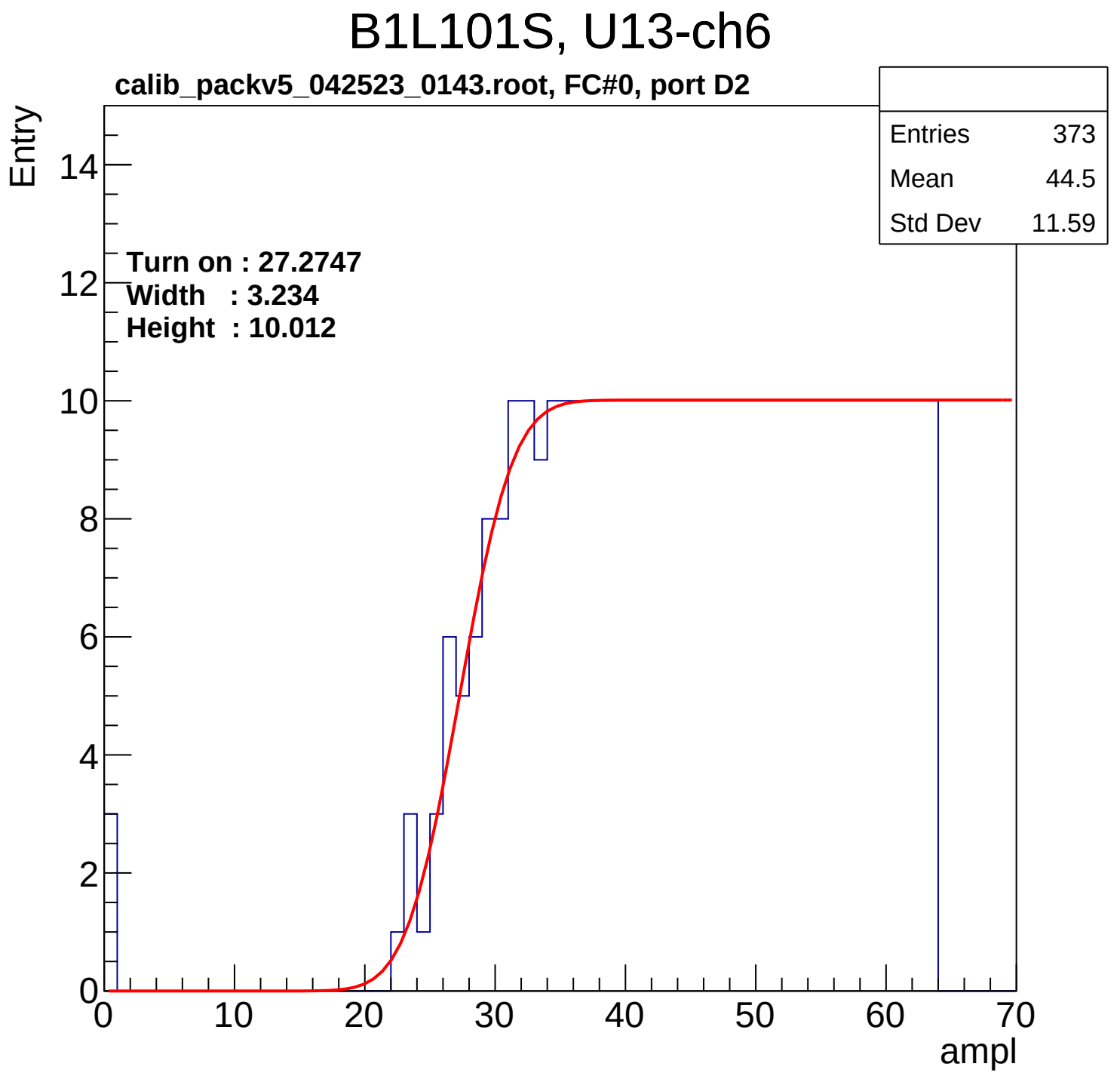
B1L101S, U13-ch6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 373
Mean 44.5
Std Dev 11.59
Turn on : 27.2747
Width : 3.234
Height : 10.012
Entry
ampl
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4
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8
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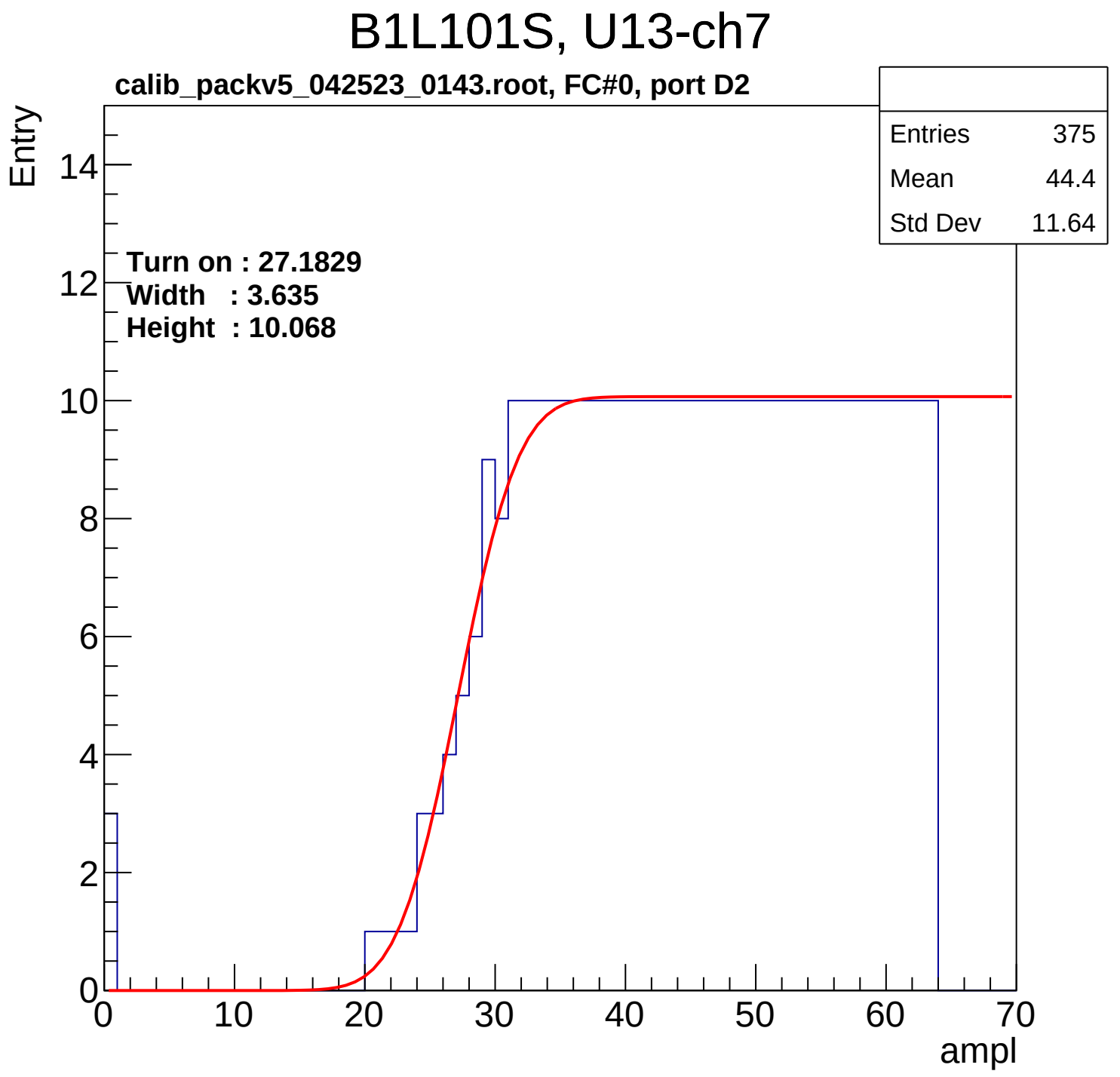
B1L101S, U13-ch7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 375
Mean 44.4
Std Dev 11.64
Turn on : 27.1829
Width : 3.635
Height : 10.068
Entry
ampl
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6
8
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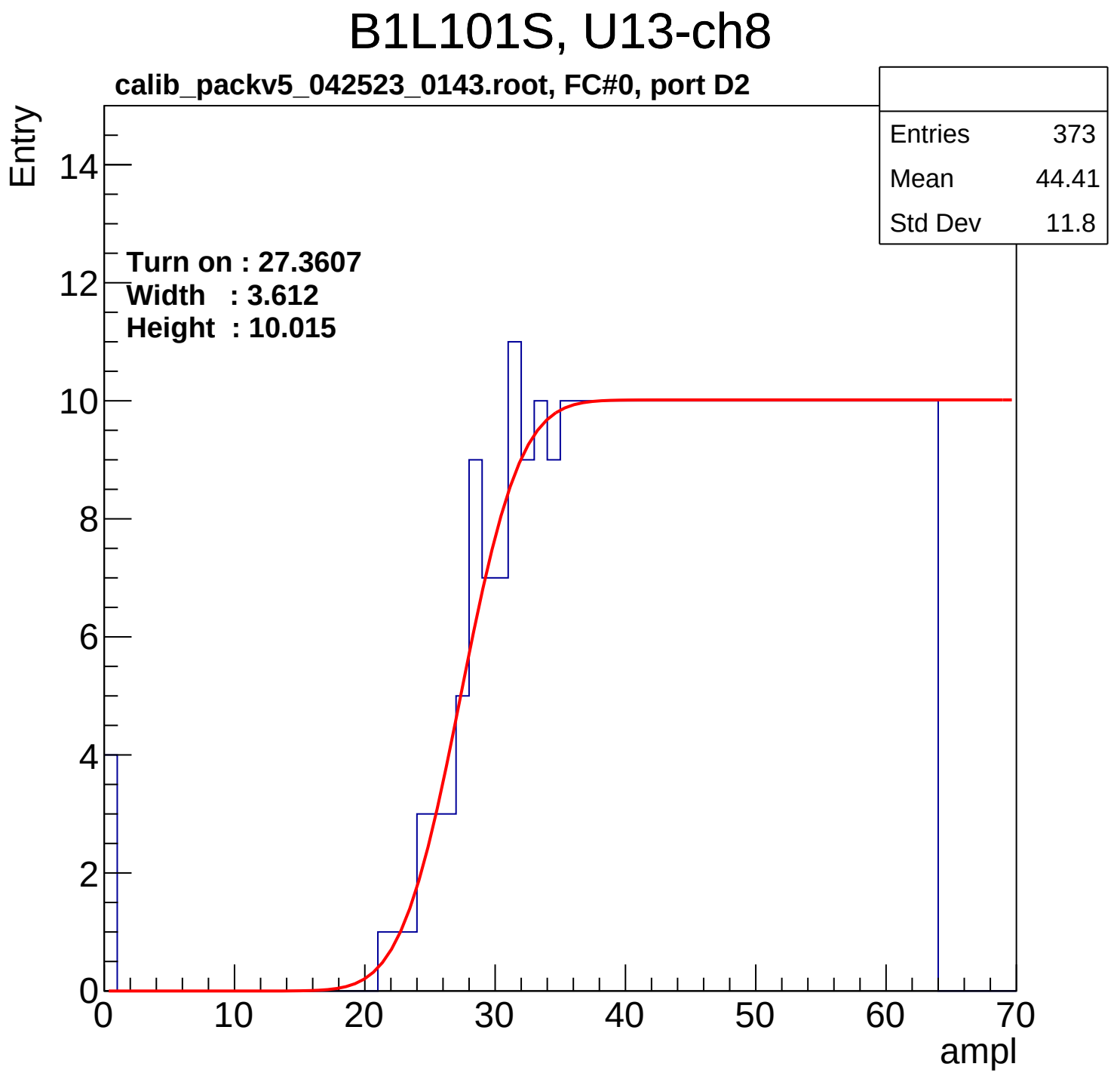
B1L101S, U13-ch8
calib_packv5_042523_0143.root, FC#0, port D2
Entries 373
Mean 44.41
Std Dev 11.8
Turn on : 27.3607
Width : 3.612
Height : 10.015
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ampl
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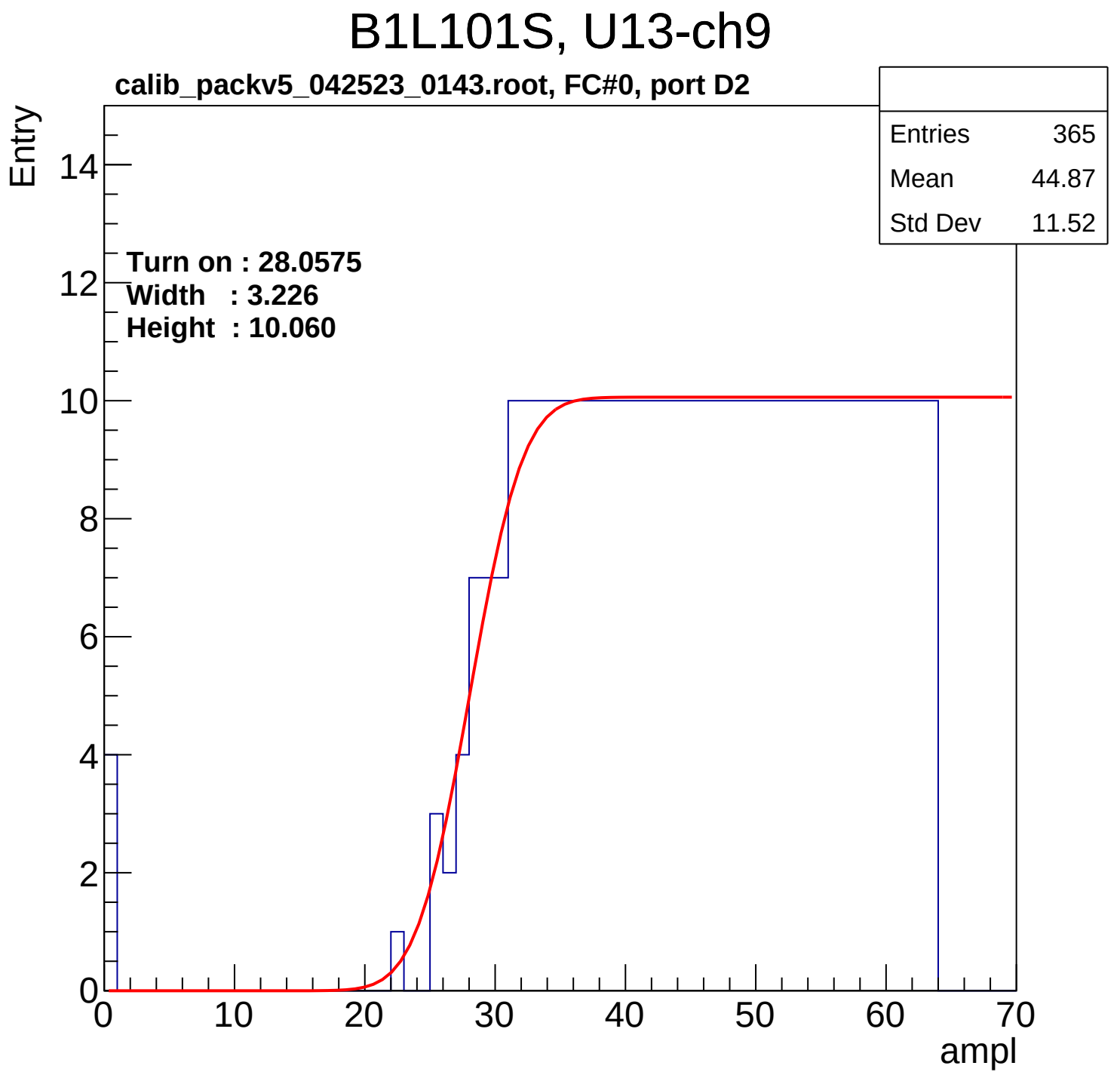
B1L101S, U13-ch9
calib_packv5_042523_0143.root, FC#0, port D2
Entries 365
Mean 44.87
Std Dev 11.52
Turn on : 28.0575
Width : 3.226
Height : 10.060
Entry
ampl
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6
8
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12
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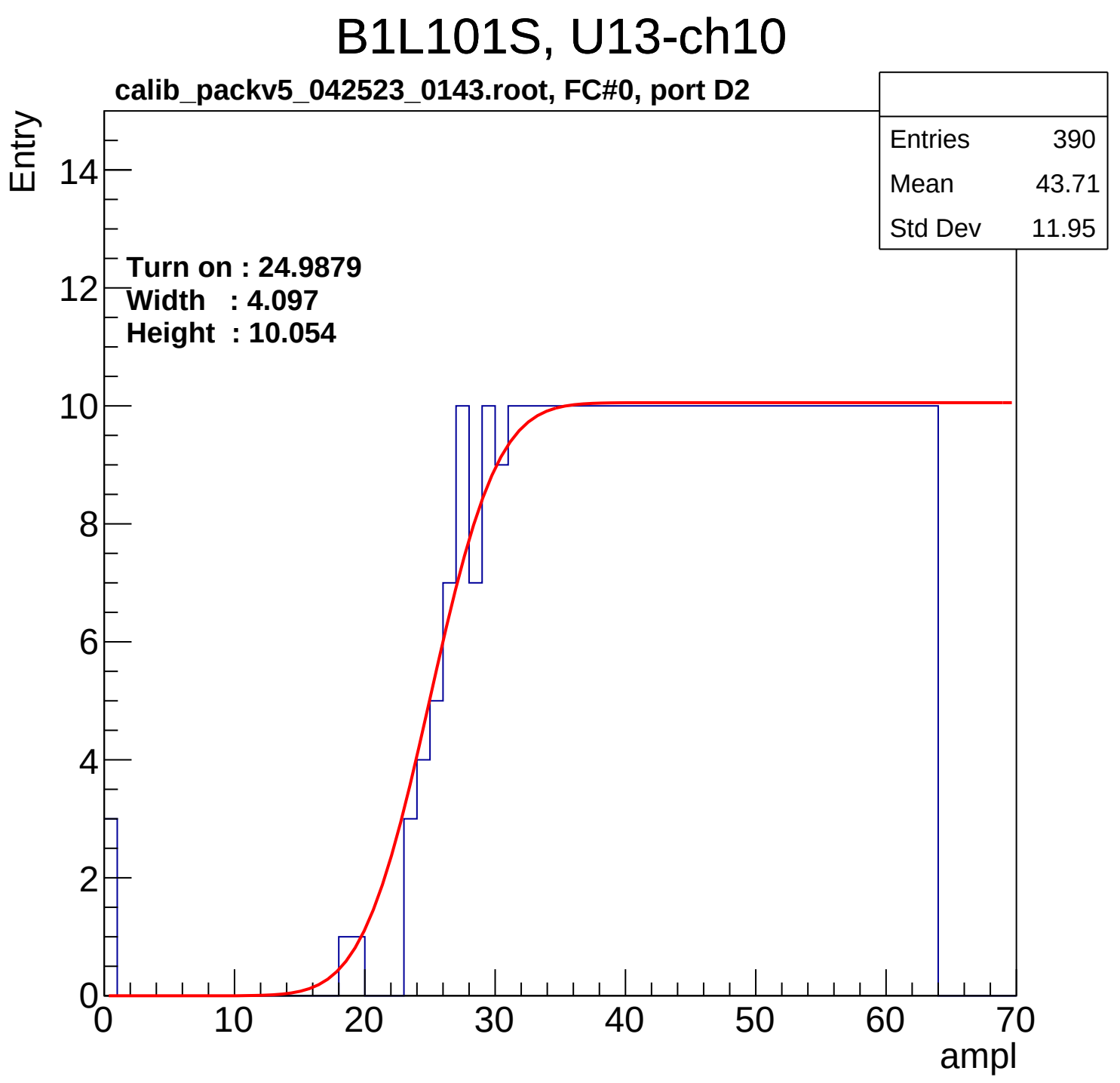
B1L101S, U13-ch10
calib_packv5_042523_0143.root, FC#0, port D2
Entries 390
Mean 43.71
Std Dev 11.95
Turn on : 24.9879
Width : 4.097
Height : 10.054
Entry
ampl
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4
6
8
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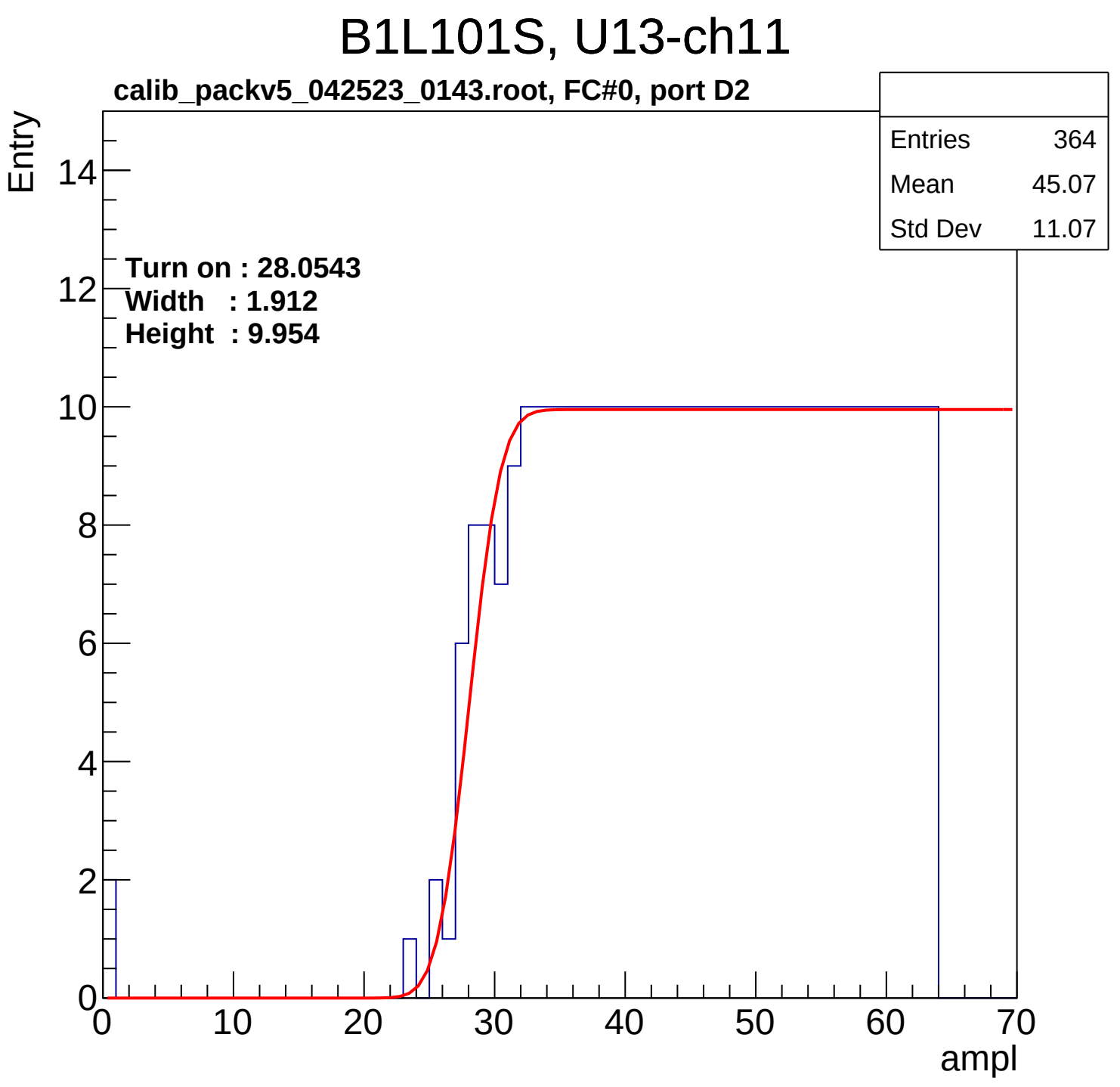
B1L101S, U13-ch11
calib_packv5_042523_0143.root, FC#0, port D2
Entries 364
Mean 45.07
Std Dev 11.07
Turn on : 28.0543
Width : 1.912
Height : 9.954
Entry
ampl
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6
8
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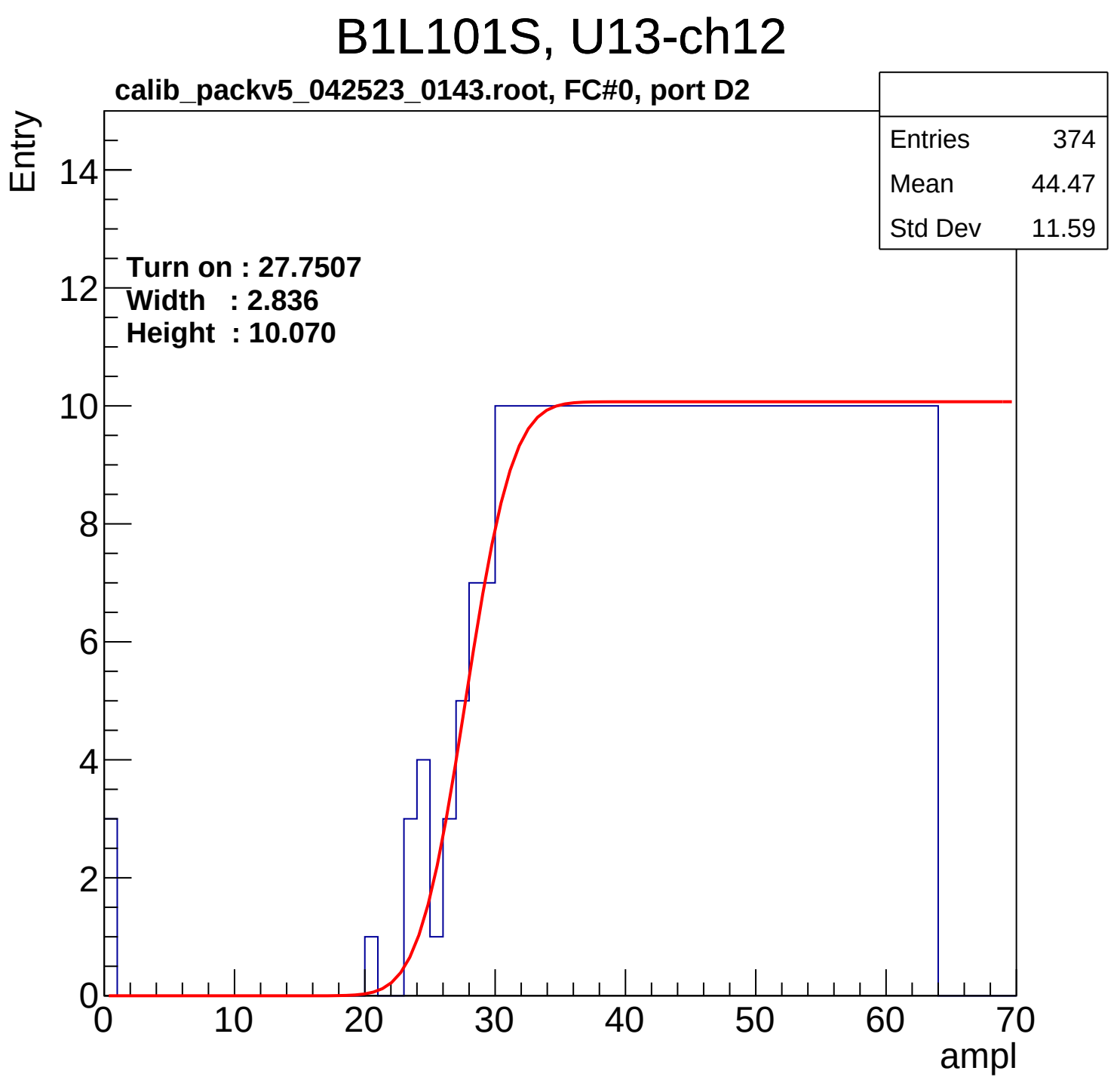
B1L101S, U13-ch12
calib_packv5_042523_0143.root, FC#0, port D2
Entries 374
Mean 44.47
Std Dev 11.59
Turn on : 27.7507
Width : 2.836
Height : 10.070
Entry
ampl
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6
8
10
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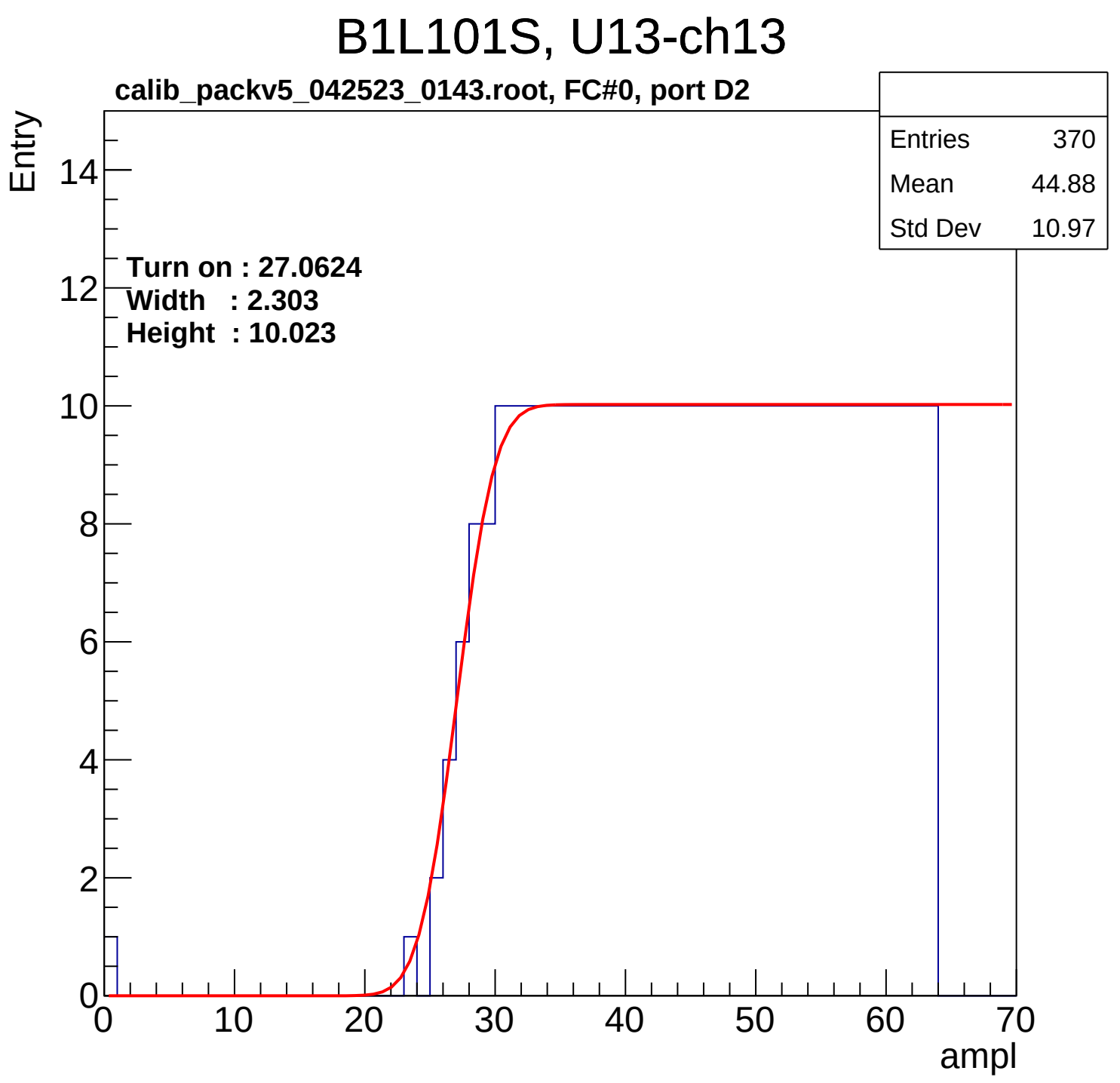
B1L101S, U13-ch13
calib_packv5_042523_0143.root, FC#0, port D2
Entries 370
Mean 44.88
Std Dev 10.97
Turn on : 27.0624
Width : 2.303
Height : 10.023
Entry
ampl
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6
8
10
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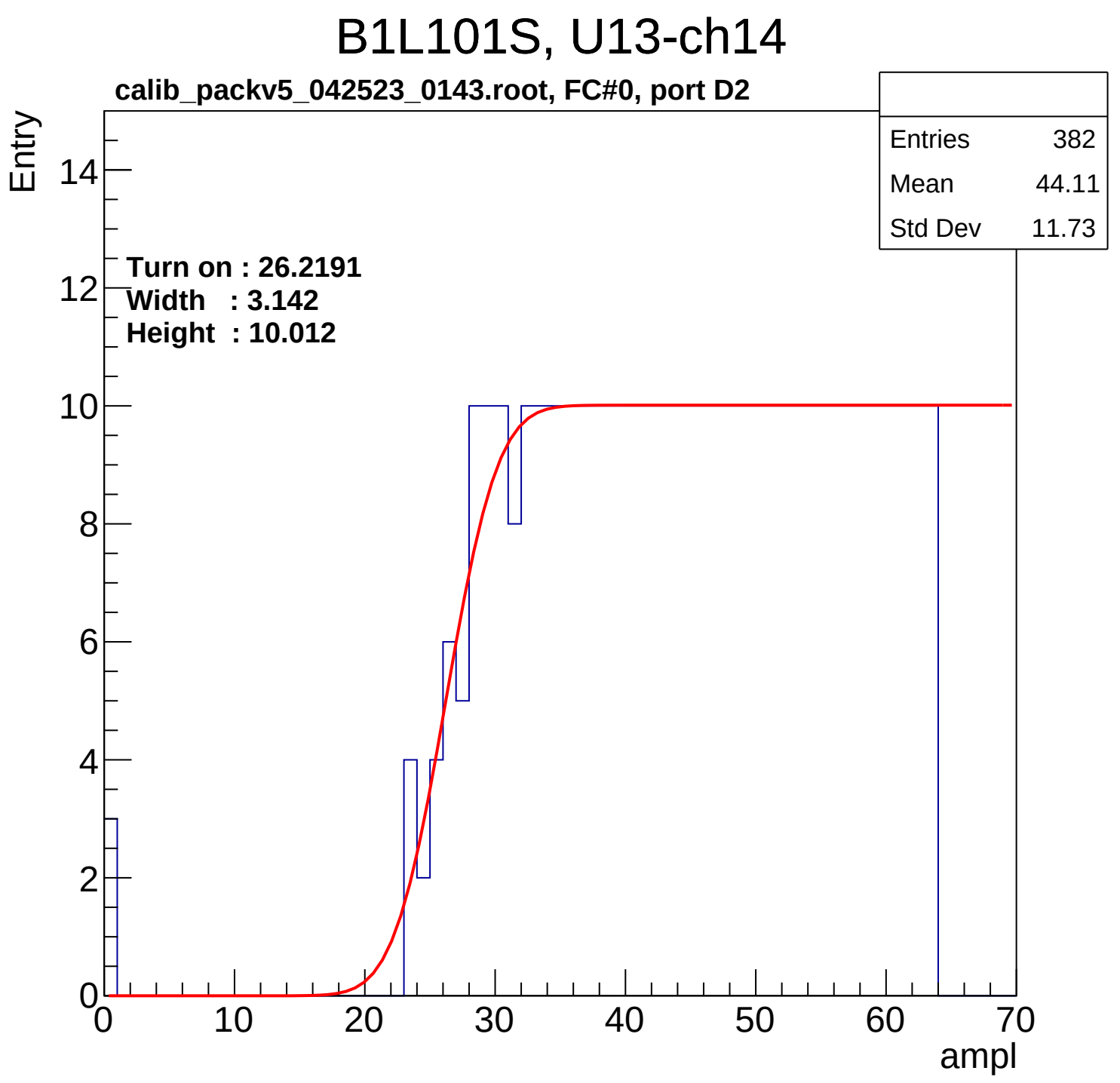
B1L101S, U13-ch14
calib_packv5_042523_0143.root, FC#0, port D2
Entries 382
Mean 44.11
Std Dev 11.73
Turn on : 26.2191
Width : 3.142
Height : 10.012
Entry
ampl
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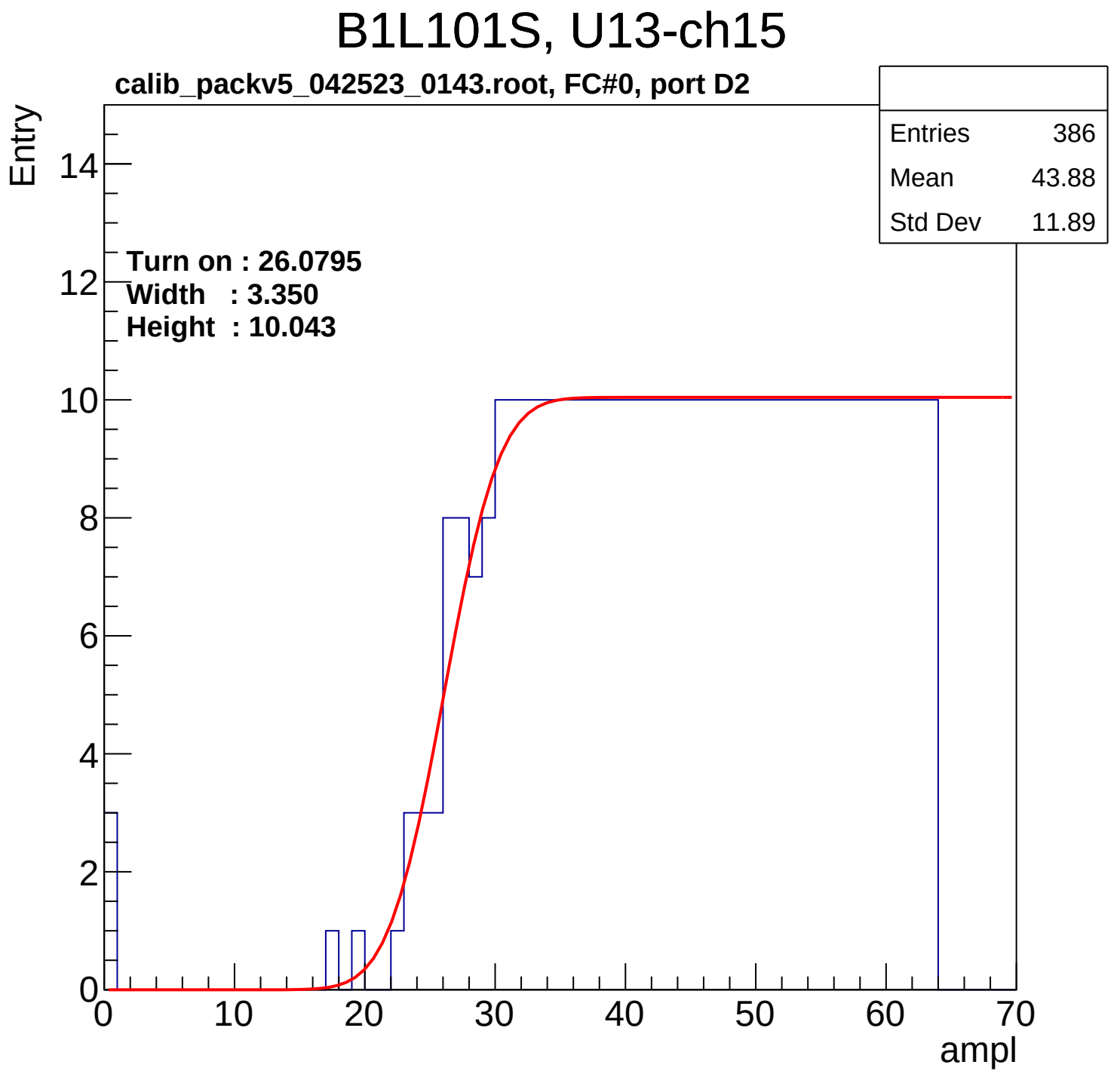
B1L101S, U13-ch15
calib_packv5_042523_0143.root, FC#0, port D2
Entries 386
Mean 43.88
Std Dev 11.89
Turn on : 26.0795
Width : 3.350
Height : 10.043
Entry
ampl
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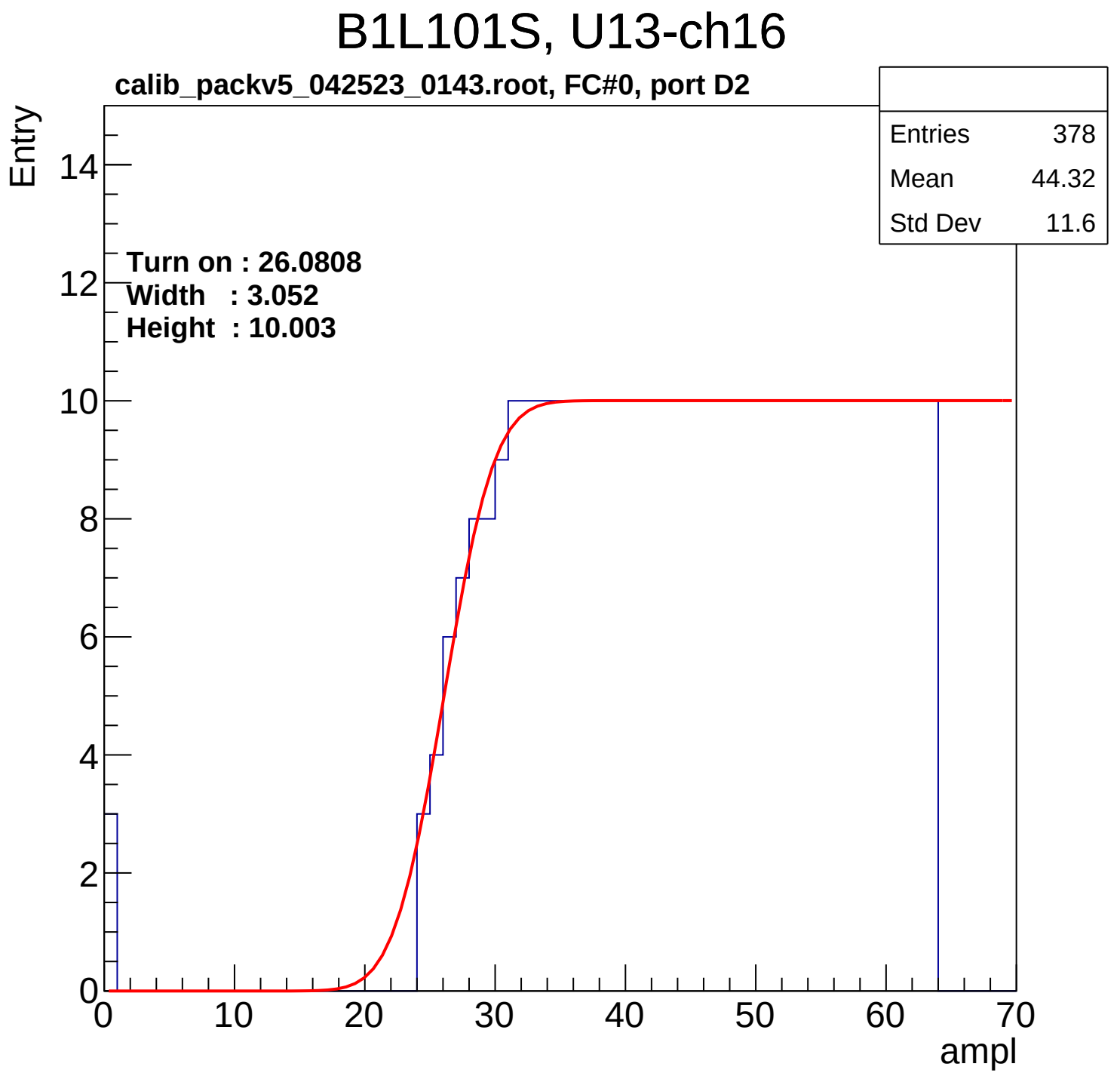
B1L101S, U13-ch16
calib_packv5_042523_0143.root, FC#0, port D2
Entries 378
Mean 44.32
Std Dev 11.6
Turn on : 26.0808
Width : 3.052
Height : 10.003
Entry
ampl
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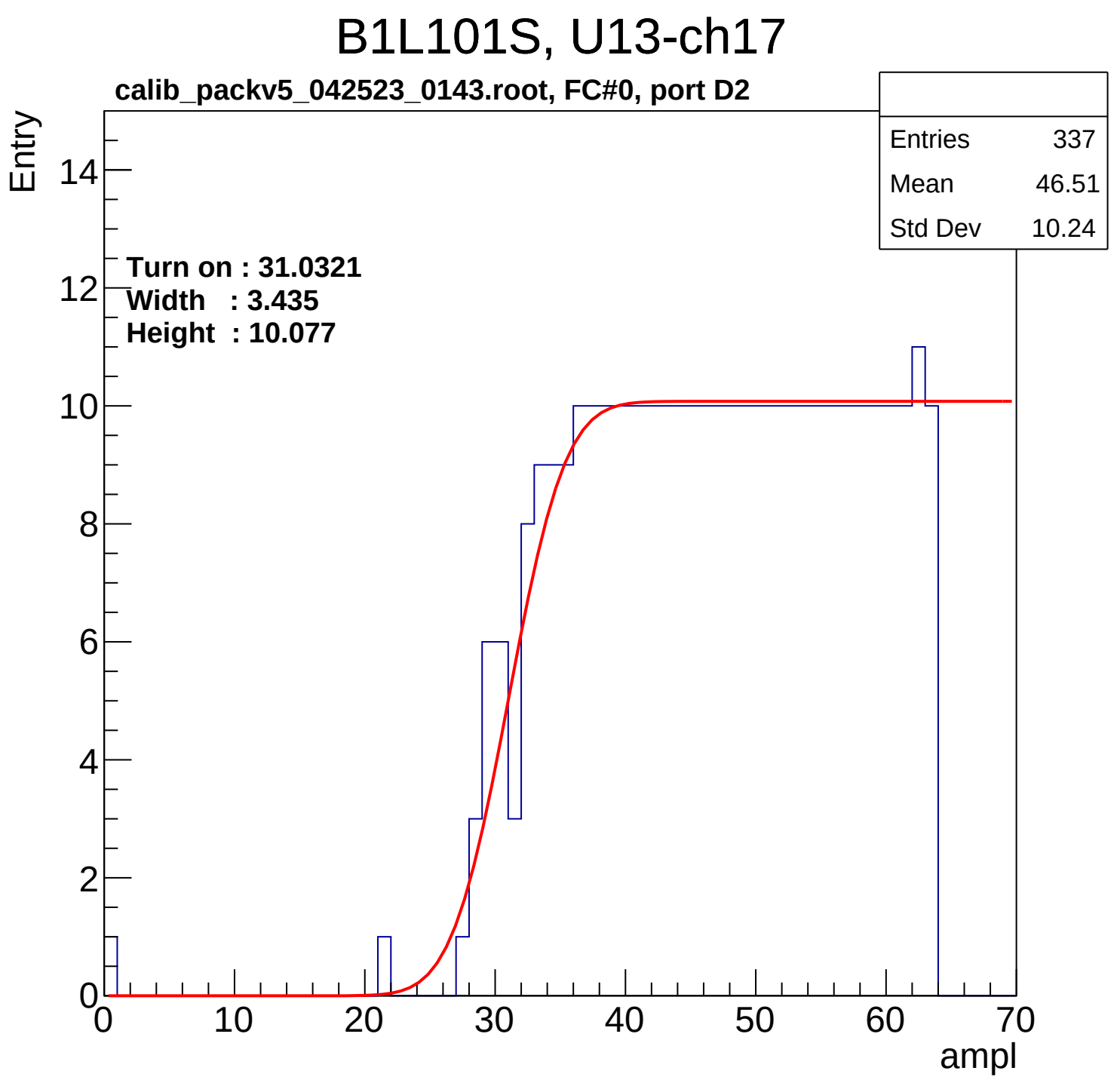
B1L101S, U13-ch17
calib_packv5_042523_0143.root, FC#0, port D2
Entries 337
Mean 46.51
Std Dev 10.24
Turn on : 31.0321
Width : 3.435
Height : 10.077
Entry
ampl
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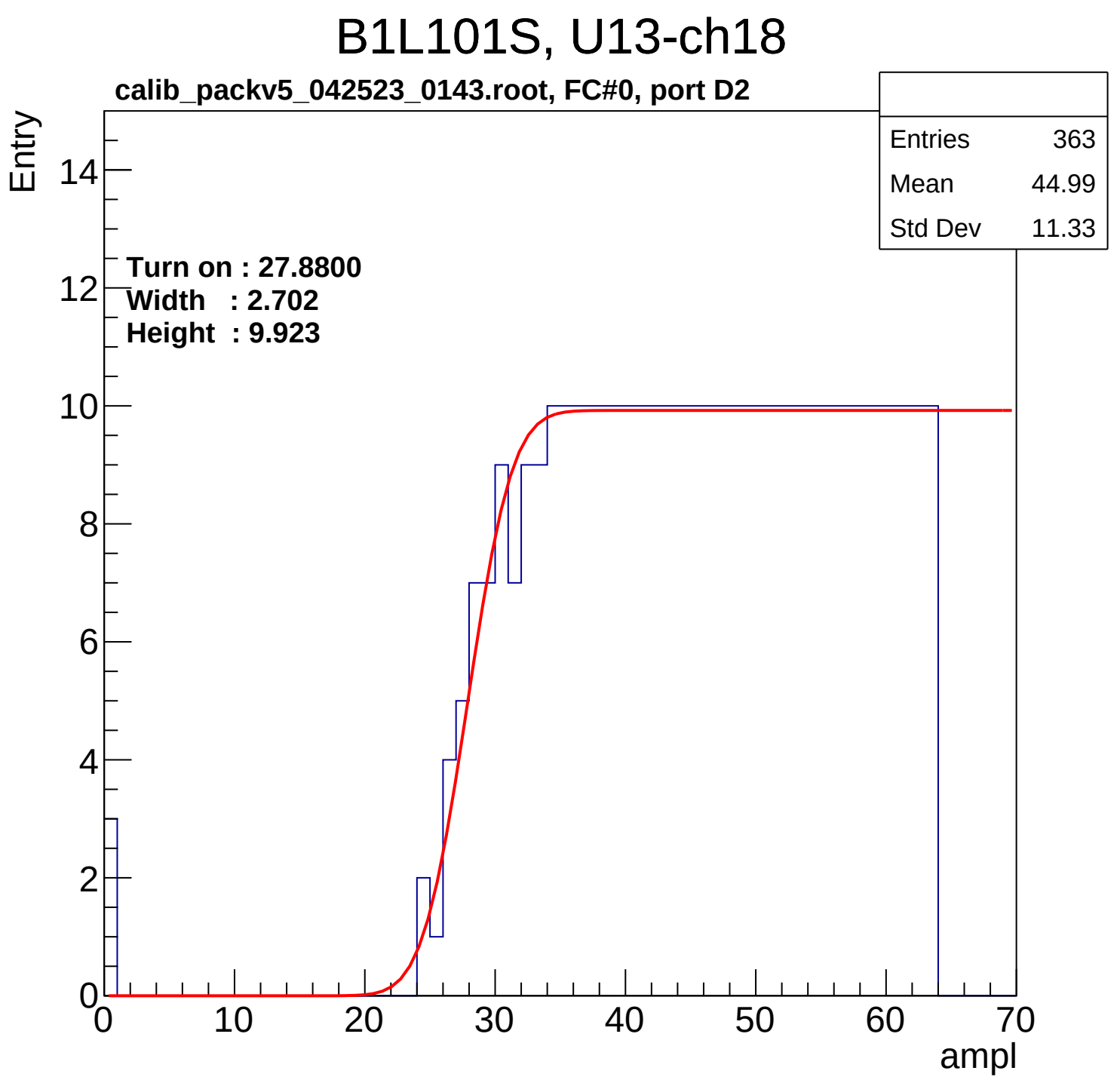
B1L101S, U13-ch18
calib_packv5_042523_0143.root, FC#0, port D2
Entries 363
Mean 44.99
Std Dev 11.33
Turn on : 27.8800
Width : 2.702
Height : 9.923
Entry
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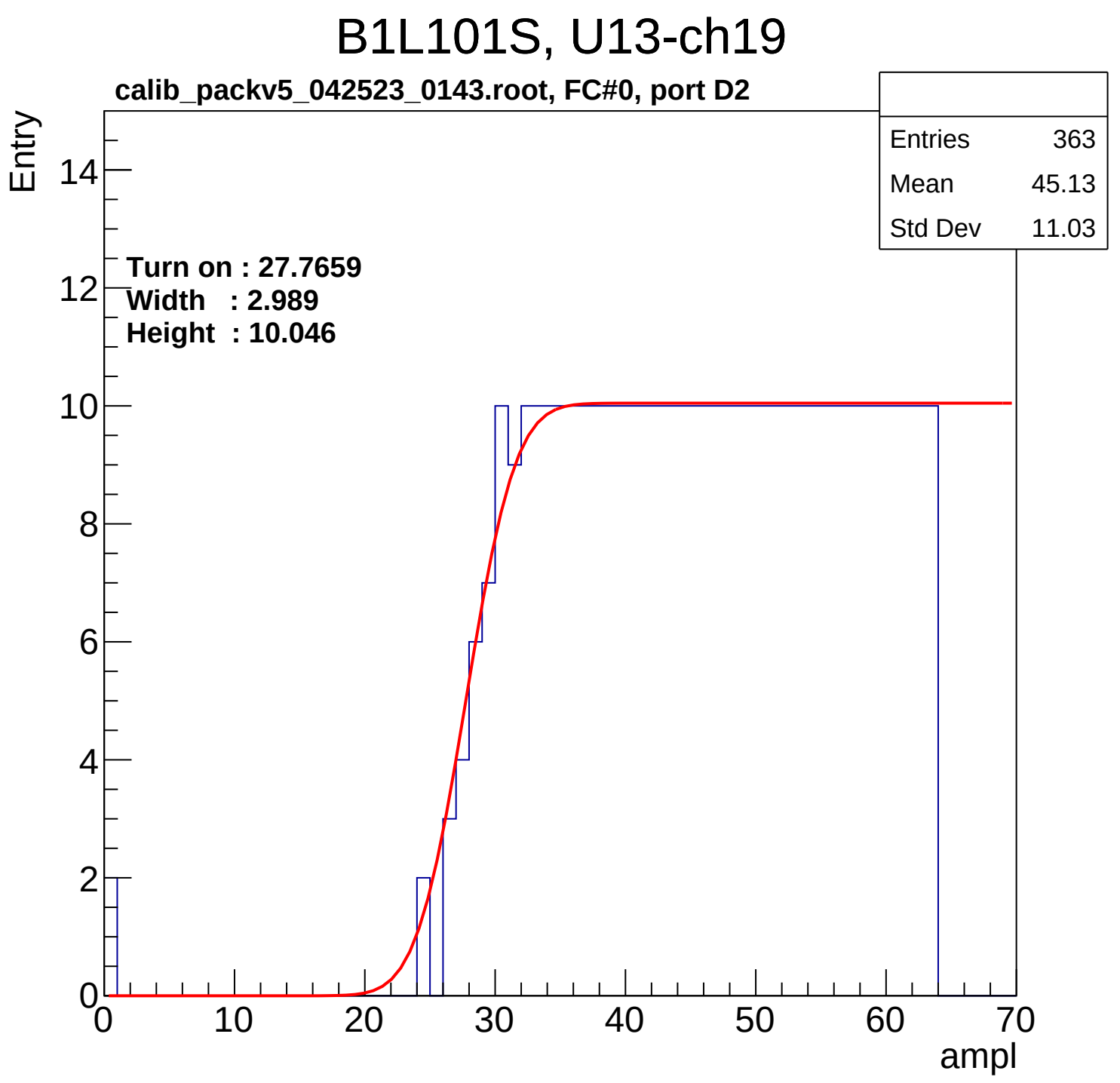
B1L101S, U13-ch19
calib_packv5_042523_0143.root, FC#0, port D2
Entries 363
Mean 45.13
Std Dev 11.03
Turn on : 27.7659
Width : 2.989
Height : 10.046
Entry
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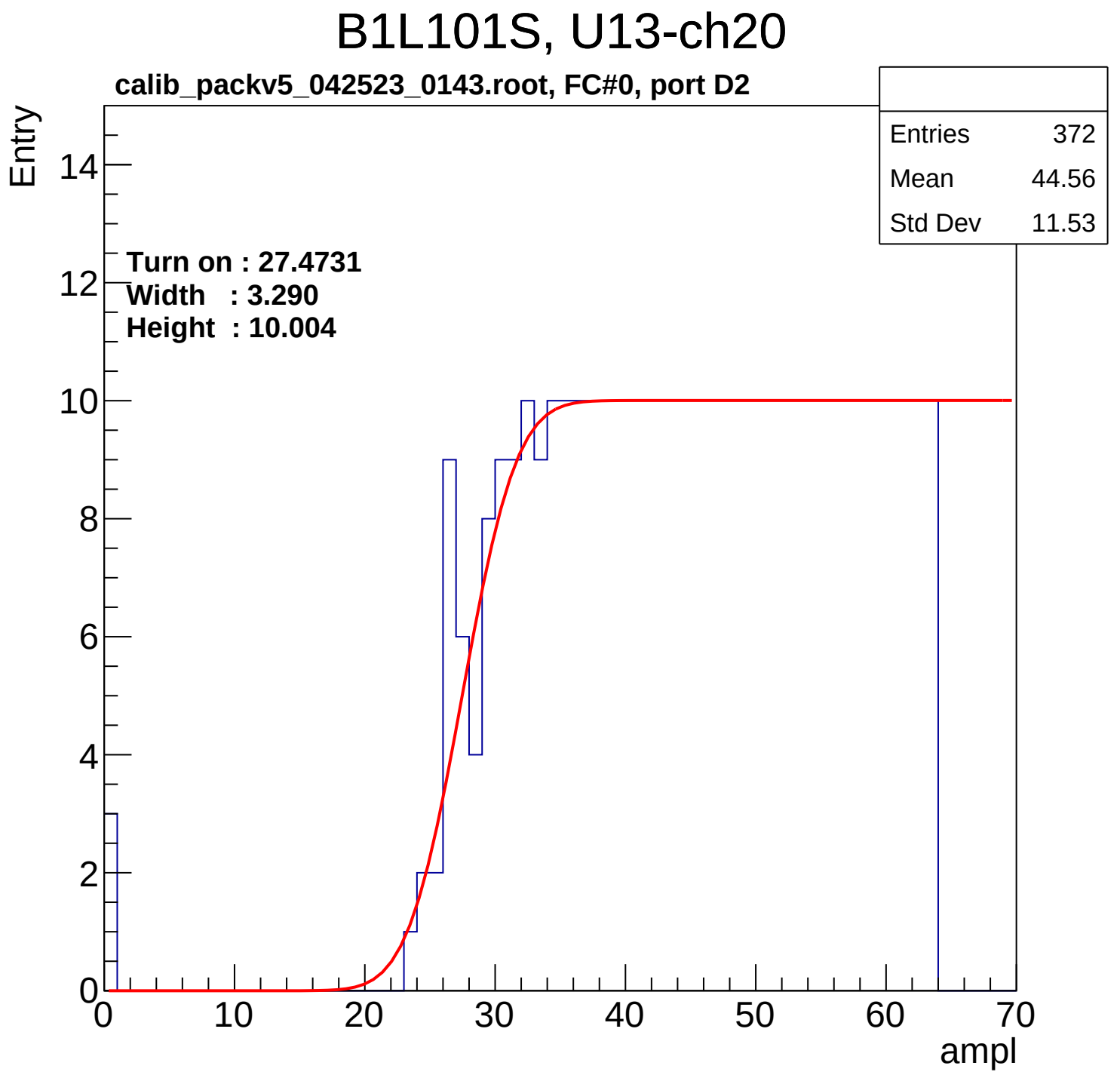
B1L101S, U13-ch20
calib_packv5_042523_0143.root, FC#0, port D2
Entries 372
Mean 44.56
Std Dev 11.53
Turn on : 27.4731
Width : 3.290
Height : 10.004
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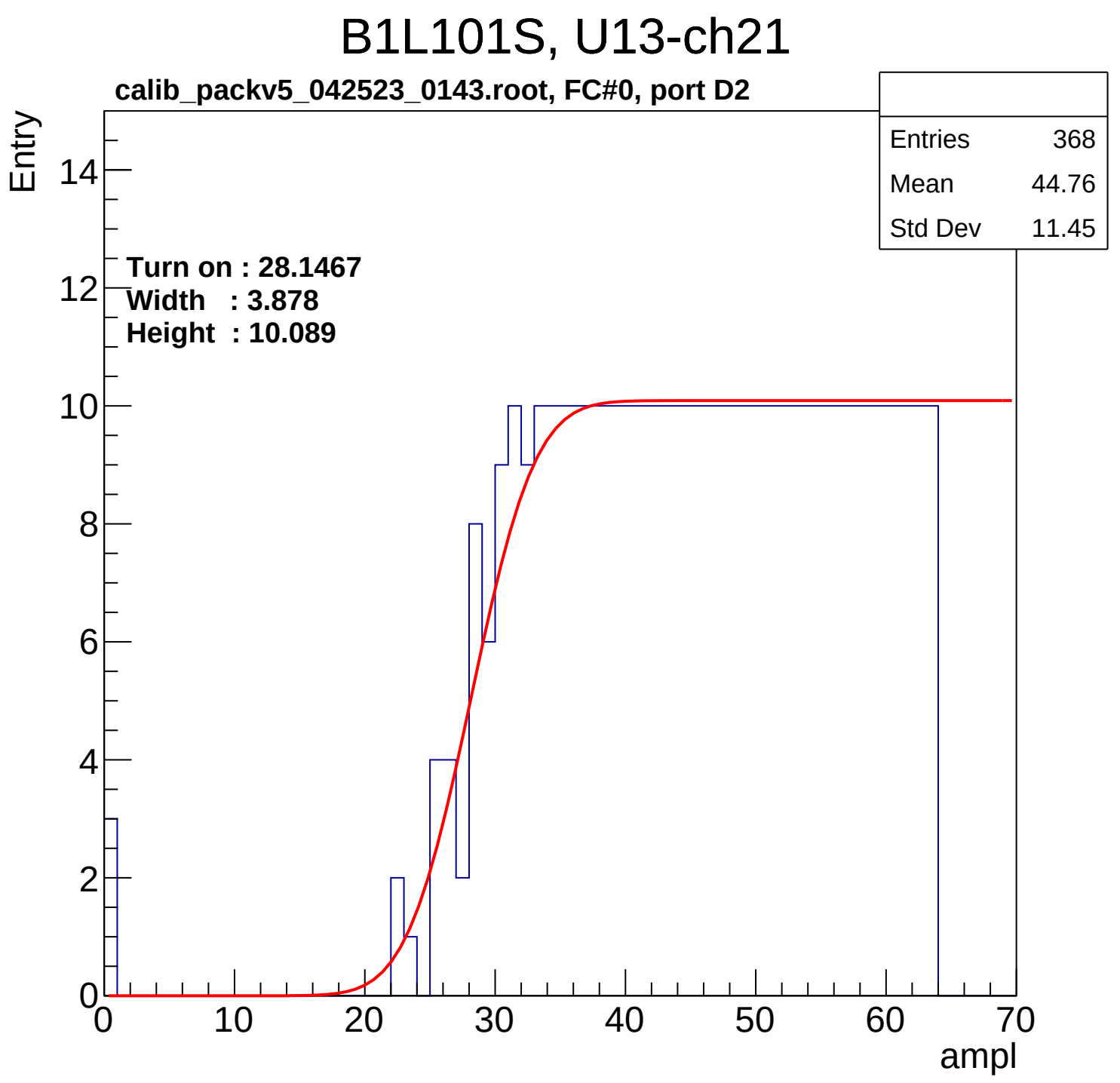
B1L101S, U13-ch21
calib_packv5_042523_0143.root, FC#0, port D2
Entries 368
Mean 44.76
Std Dev 11.45
Turn on : 28.1467
Width : 3.878
Height : 10.089
Entry
ampl
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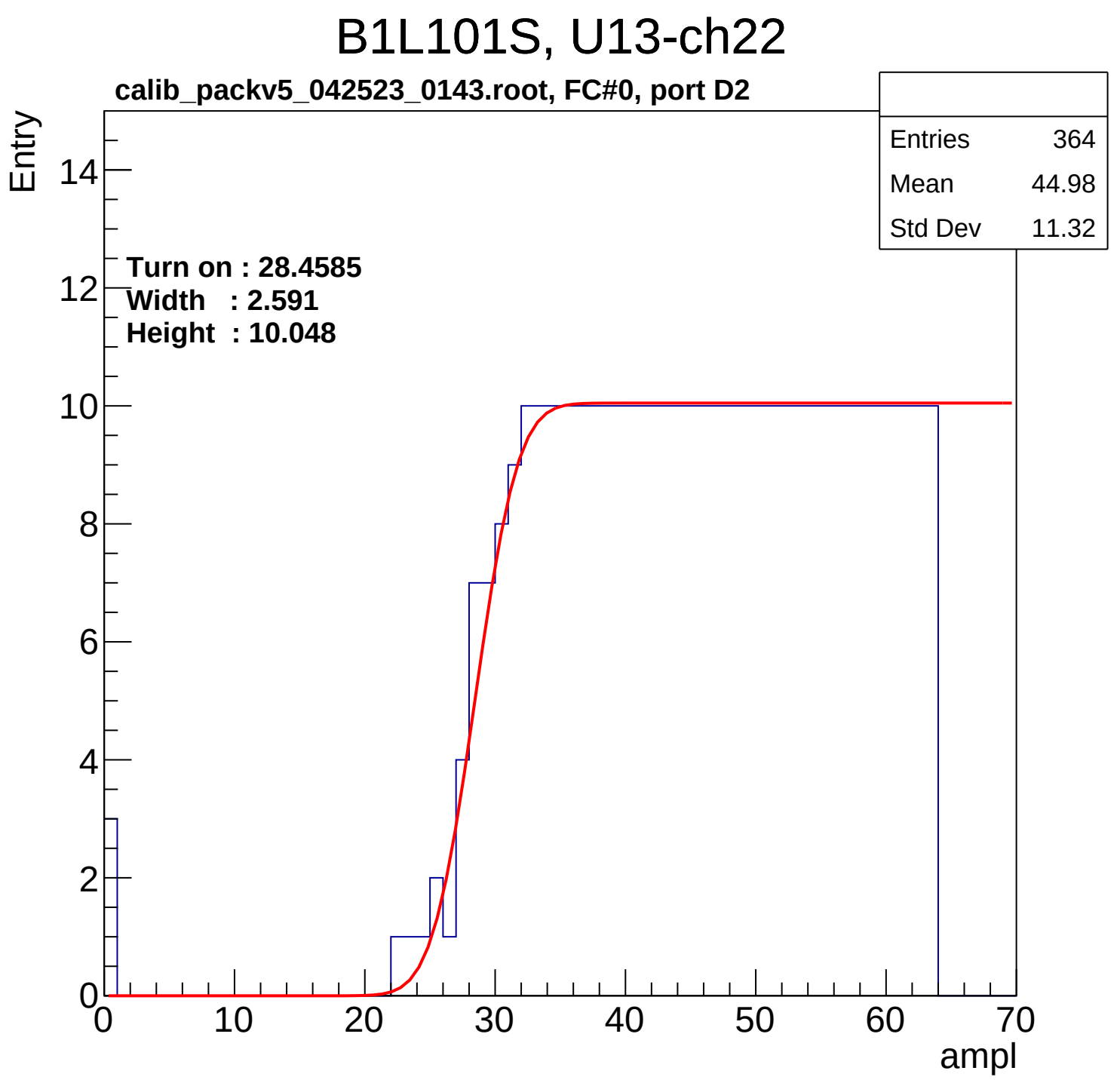
B1L101S, U13-ch22
calib_packv5_042523_0143.root, FC#0, port D2
Entries 364
Mean 44.98
Std Dev 11.32
Turn on : 28.4585
Width : 2.591
Height : 10.048
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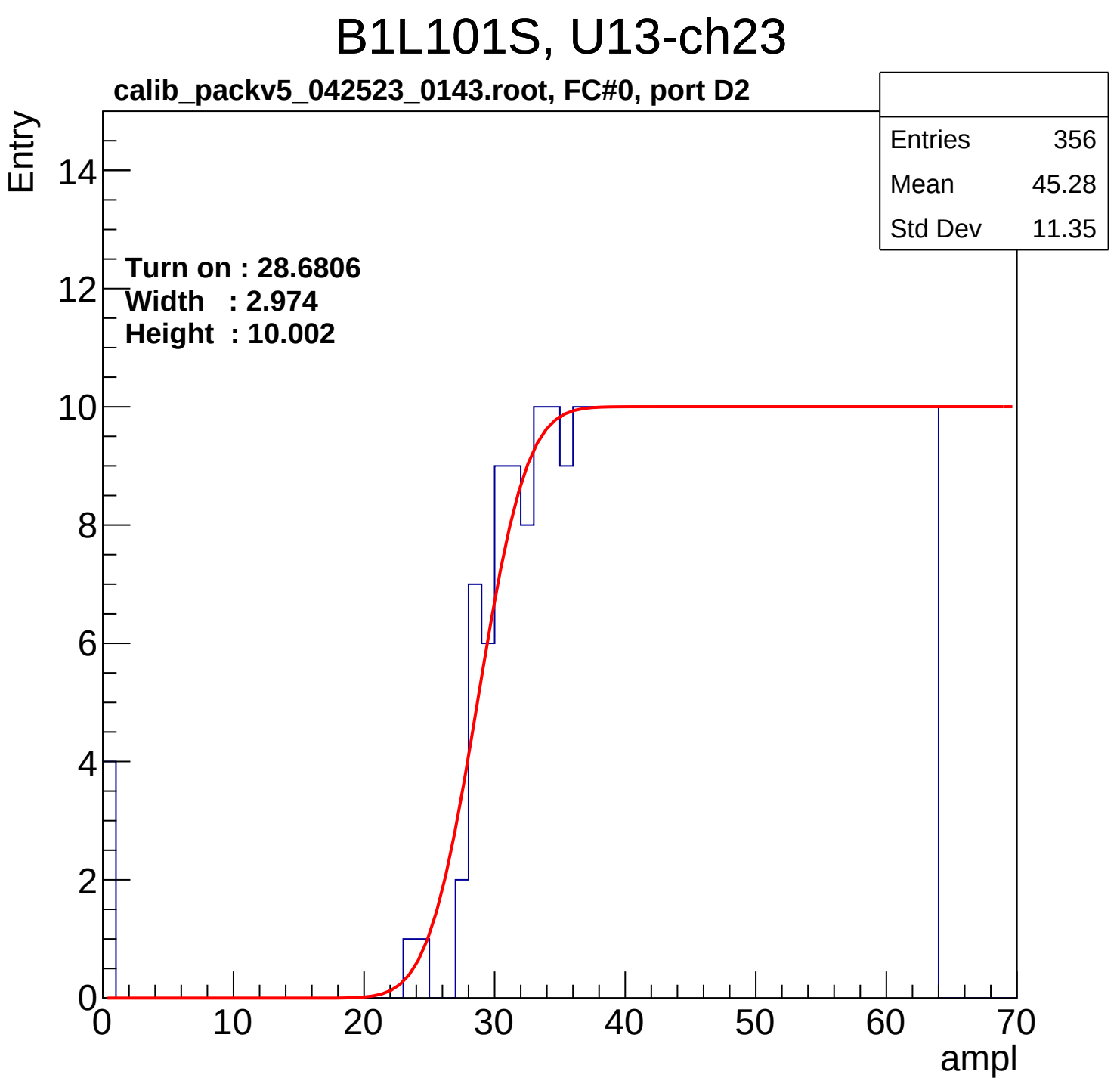
B1L101S, U13-ch23
calib_packv5_042523_0143.root, FC#0, port D2
Entries 356
Mean 45.28
Std Dev 11.35
Turn on : 28.6806
Width : 2.974
Height : 10.002
Entry
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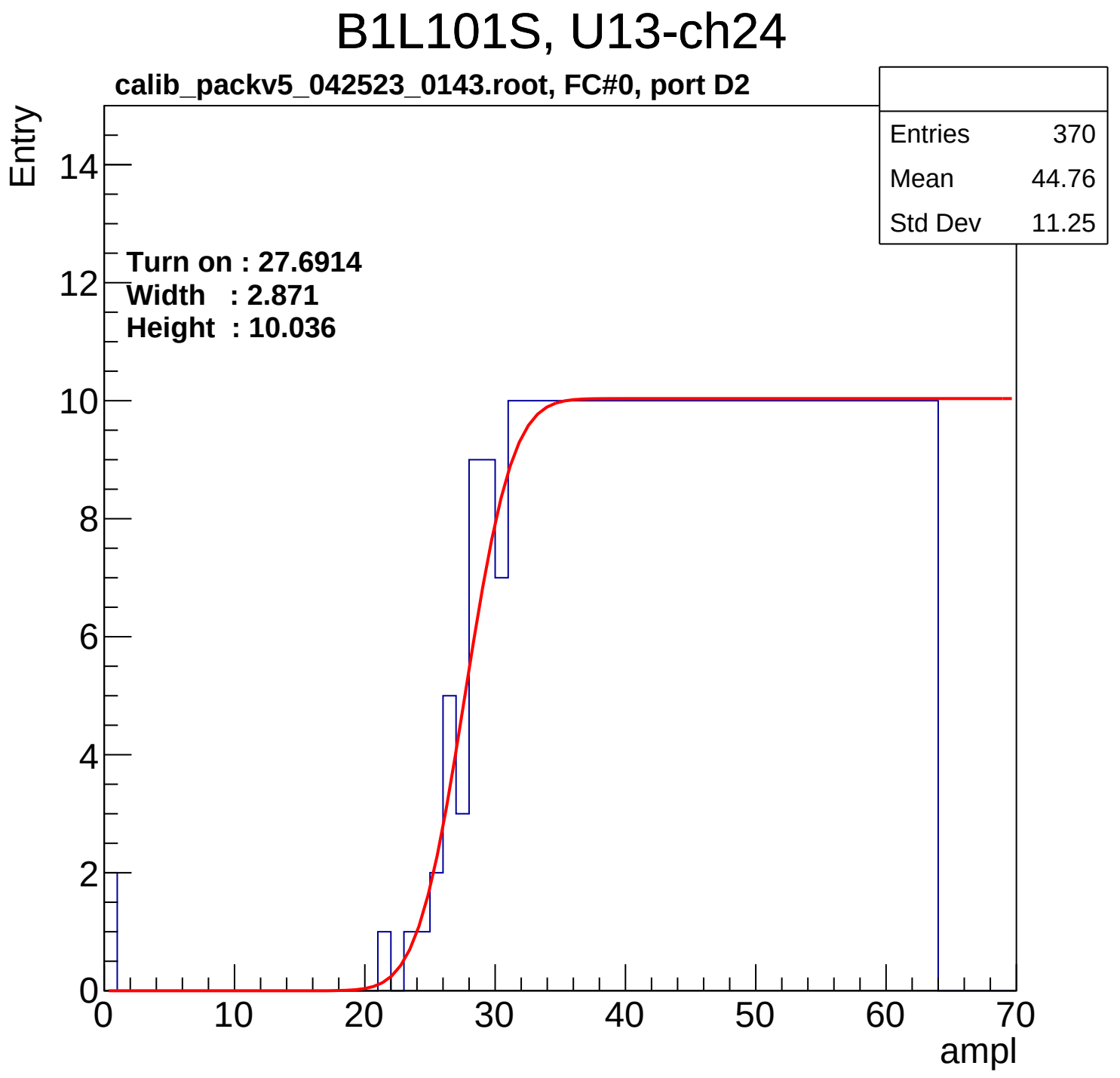
B1L101S, U13-ch24
calib_packv5_042523_0143.root, FC#0, port D2
Entries 370
Mean 44.76
Std Dev 11.25
Turn on : 27.6914
Width : 2.871
Height : 10.036
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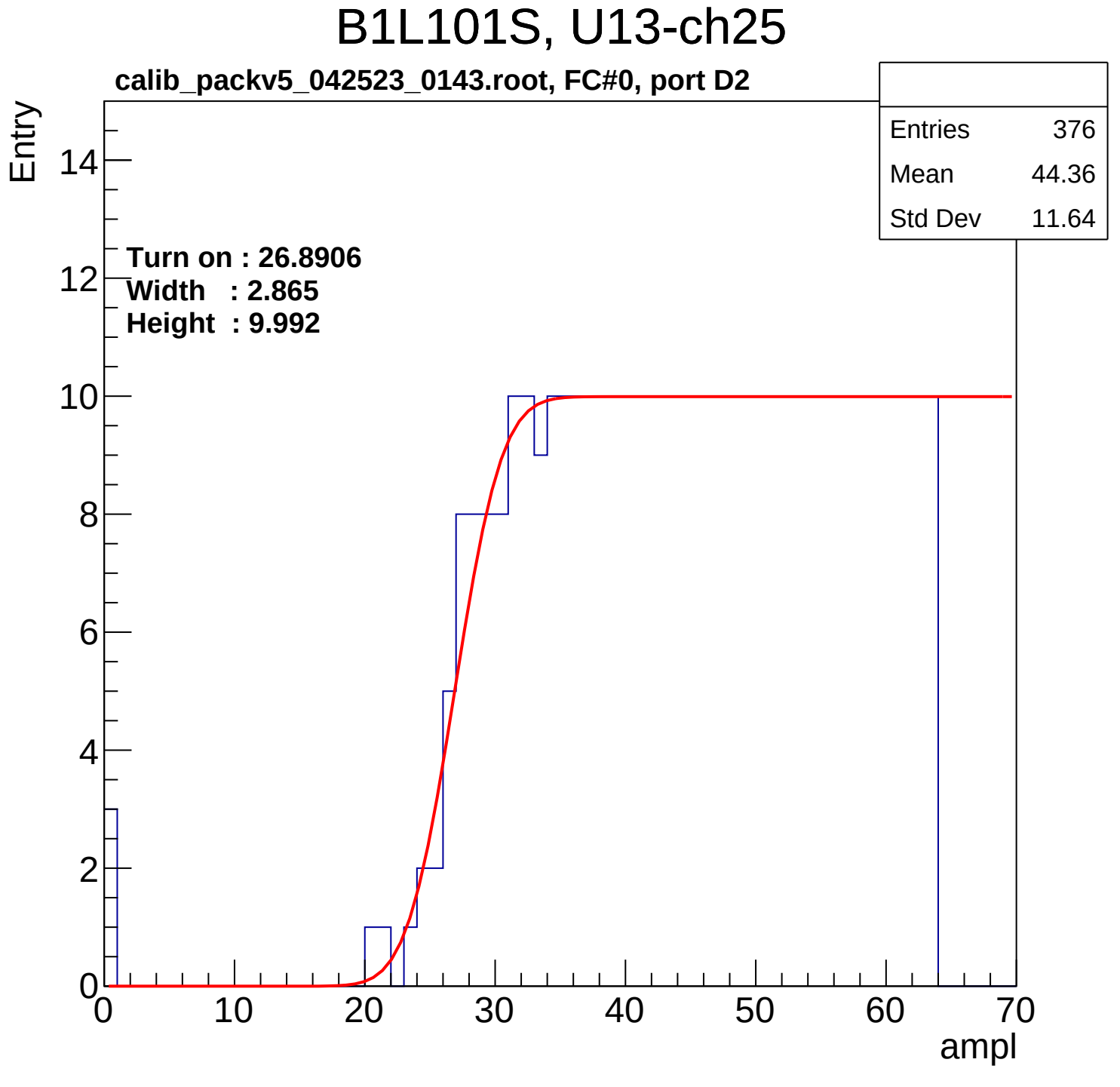
B1L101S, U13-ch25
calib_packv5_042523_0143.root, FC#0, port D2
Entries 376
Mean 44.36
Std Dev 11.64
Turn on : 26.8906
Width : 2.865
Height : 9.992
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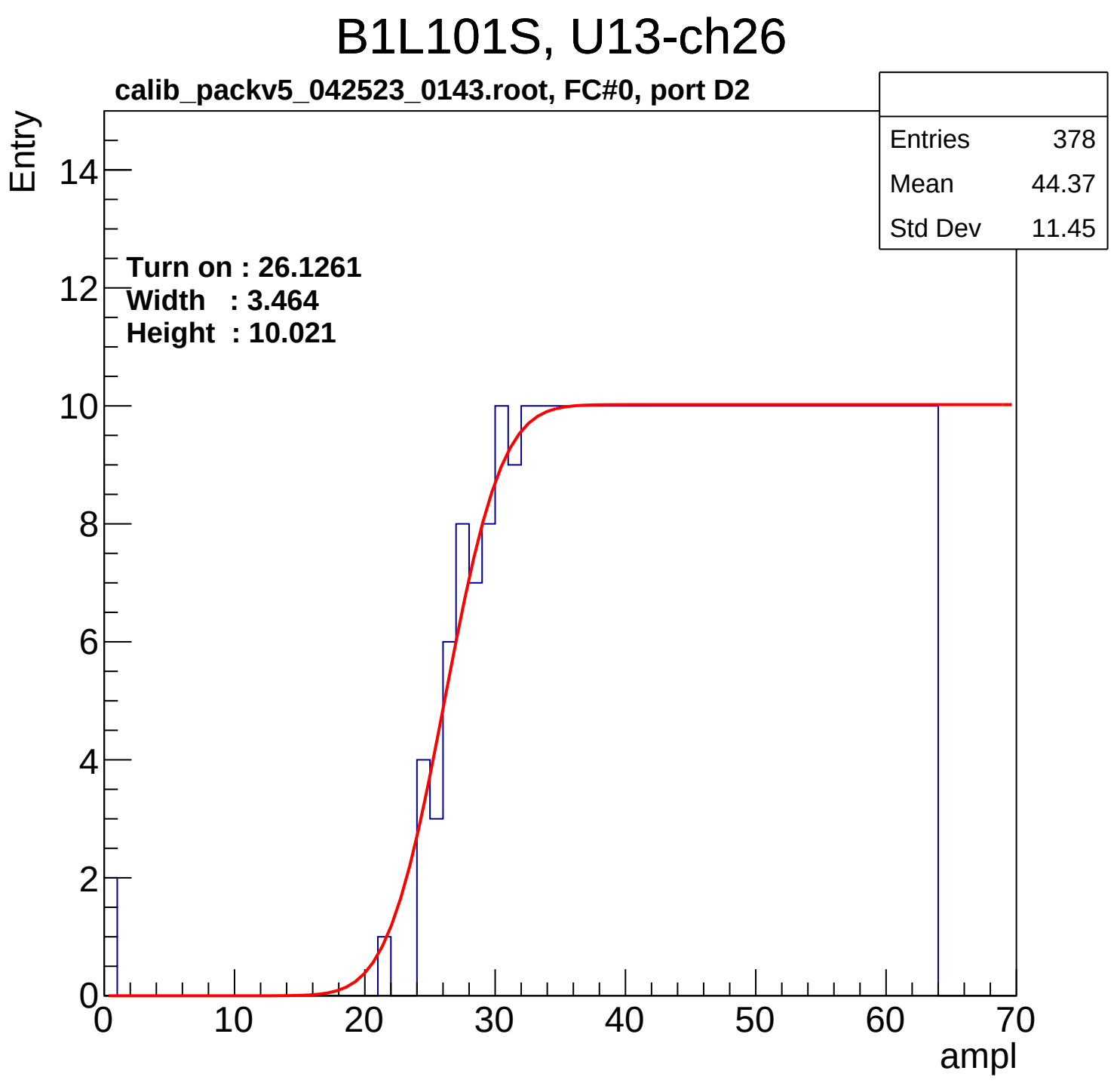
B1L101S, U13-ch26
calib_packv5_042523_0143.root, FC#0, port D2
Entries 378
Mean 44.37
Std Dev 11.45
Turn on : 26.1261
Width : 3.464
Height : 10.021
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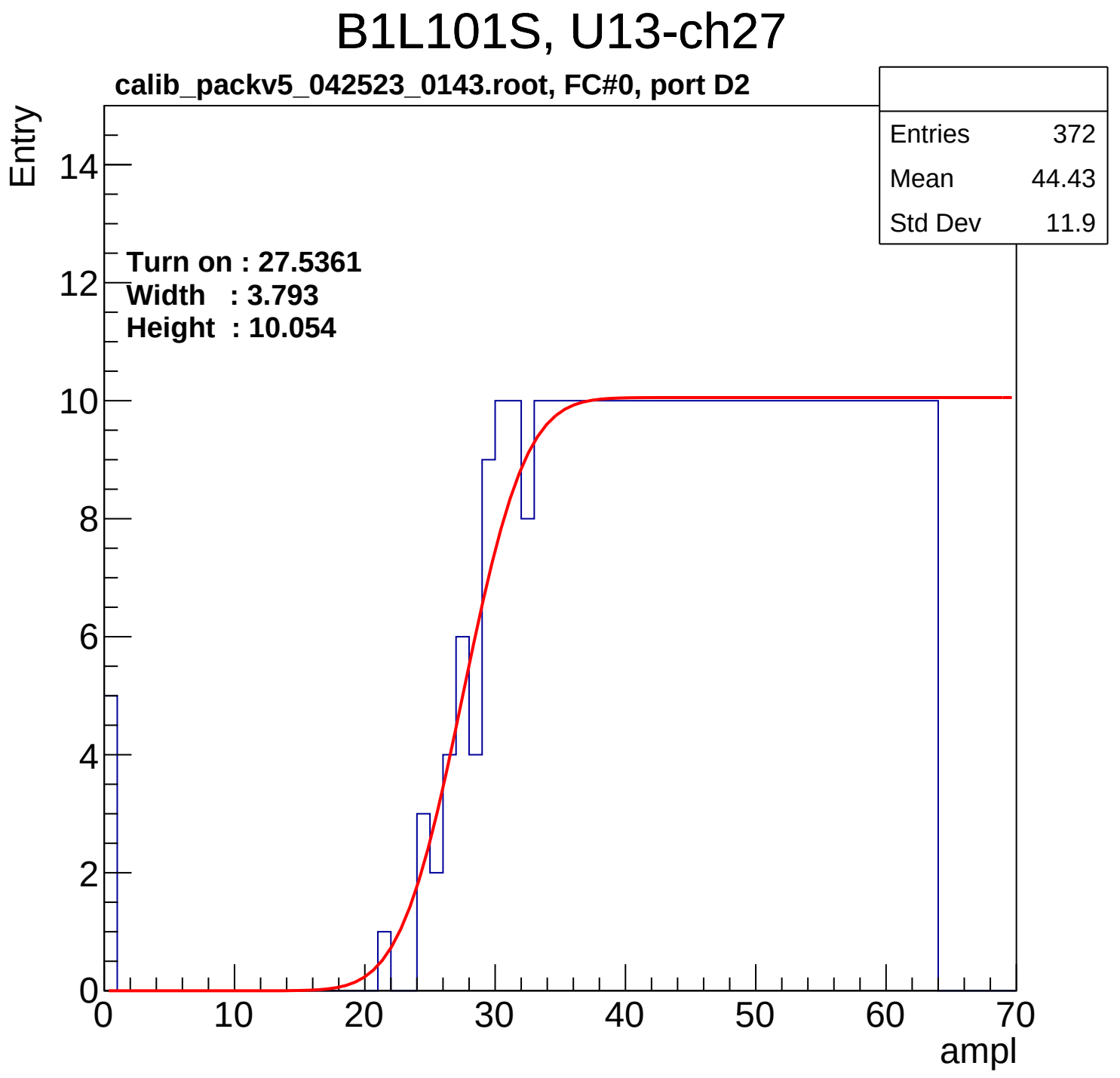
B1L101S, U13-ch27
calib_packv5_042523_0143.root, FC#0, port D2
Entries 372
Mean 44.43
Std Dev 11.9
Turn on : 27.5361
Width : 3.793
Height : 10.054
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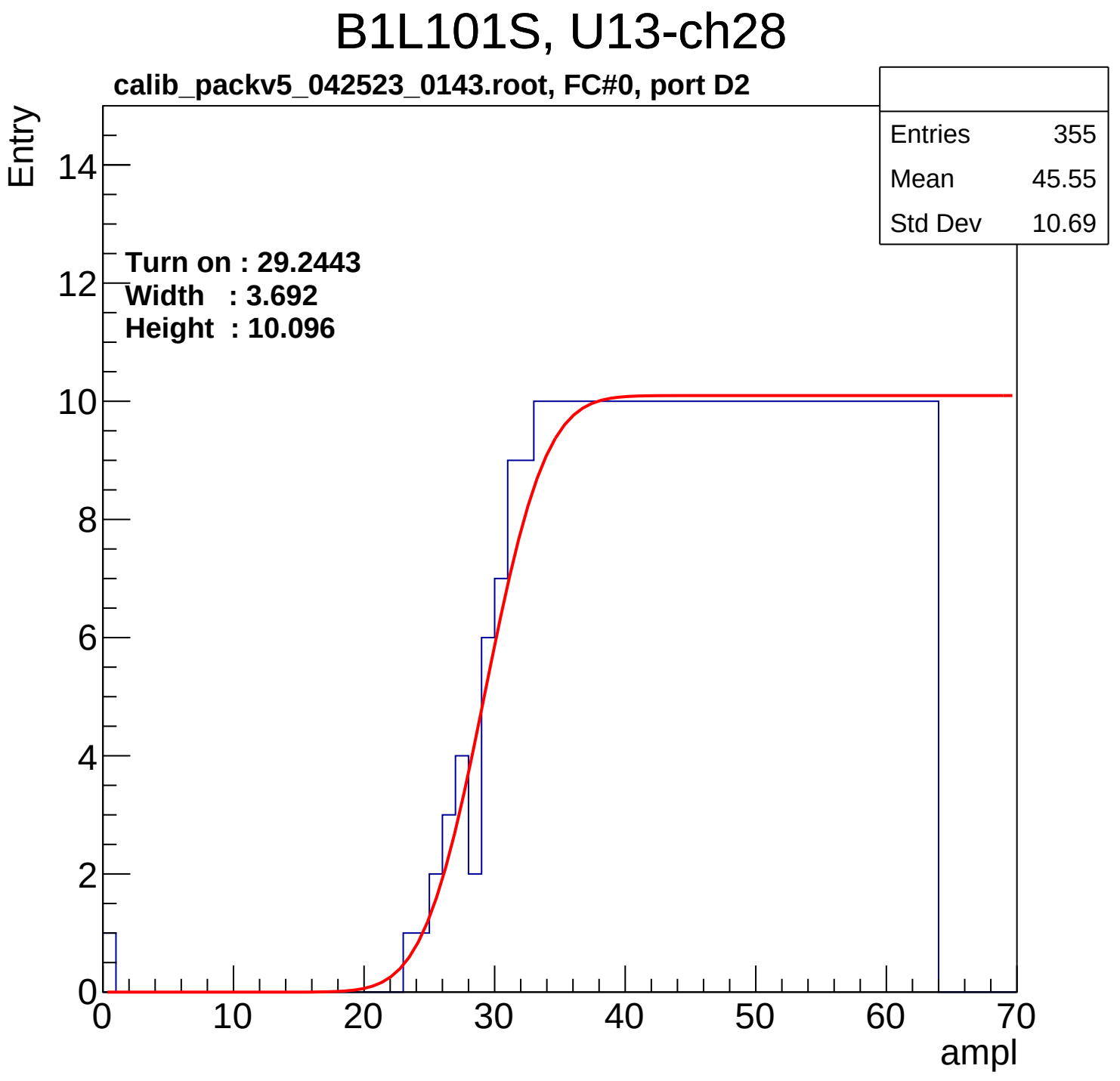
B1L101S, U13-ch28
calib_packv5_042523_0143.root, FC#0, port D2
Entries 355
Mean 45.55
Std Dev 10.69
Turn on : 29.2443
Width : 3.692
Height : 10.096
Entry
ampl
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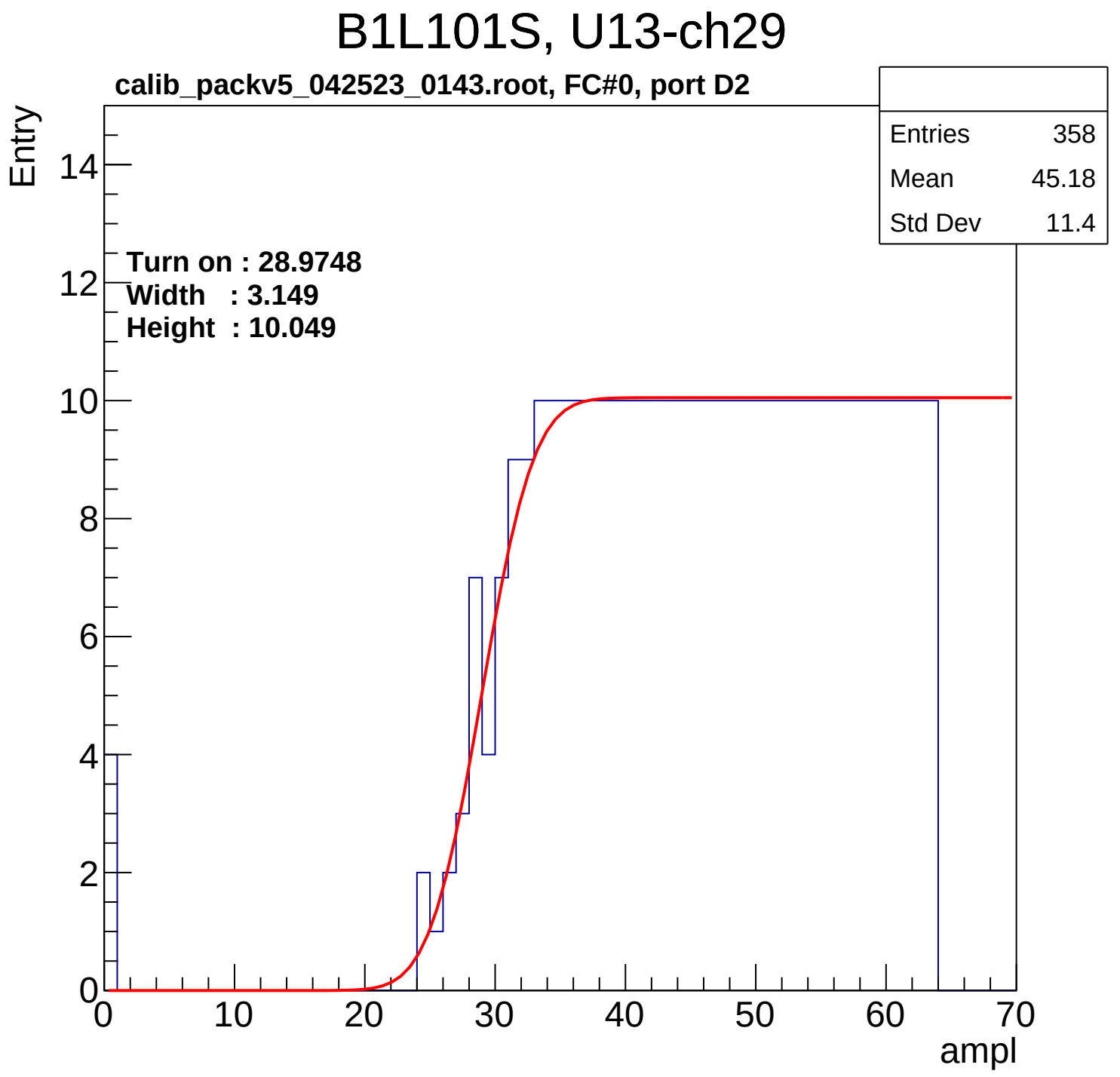
B1L101S, U13-ch29
calib_packv5_042523_0143.root, FC#0, port D2
Entries 358
Mean 45.18
Std Dev 11.4
Turn on : 28.9748
Width : 3.149
Height : 10.049
Entry
ampl
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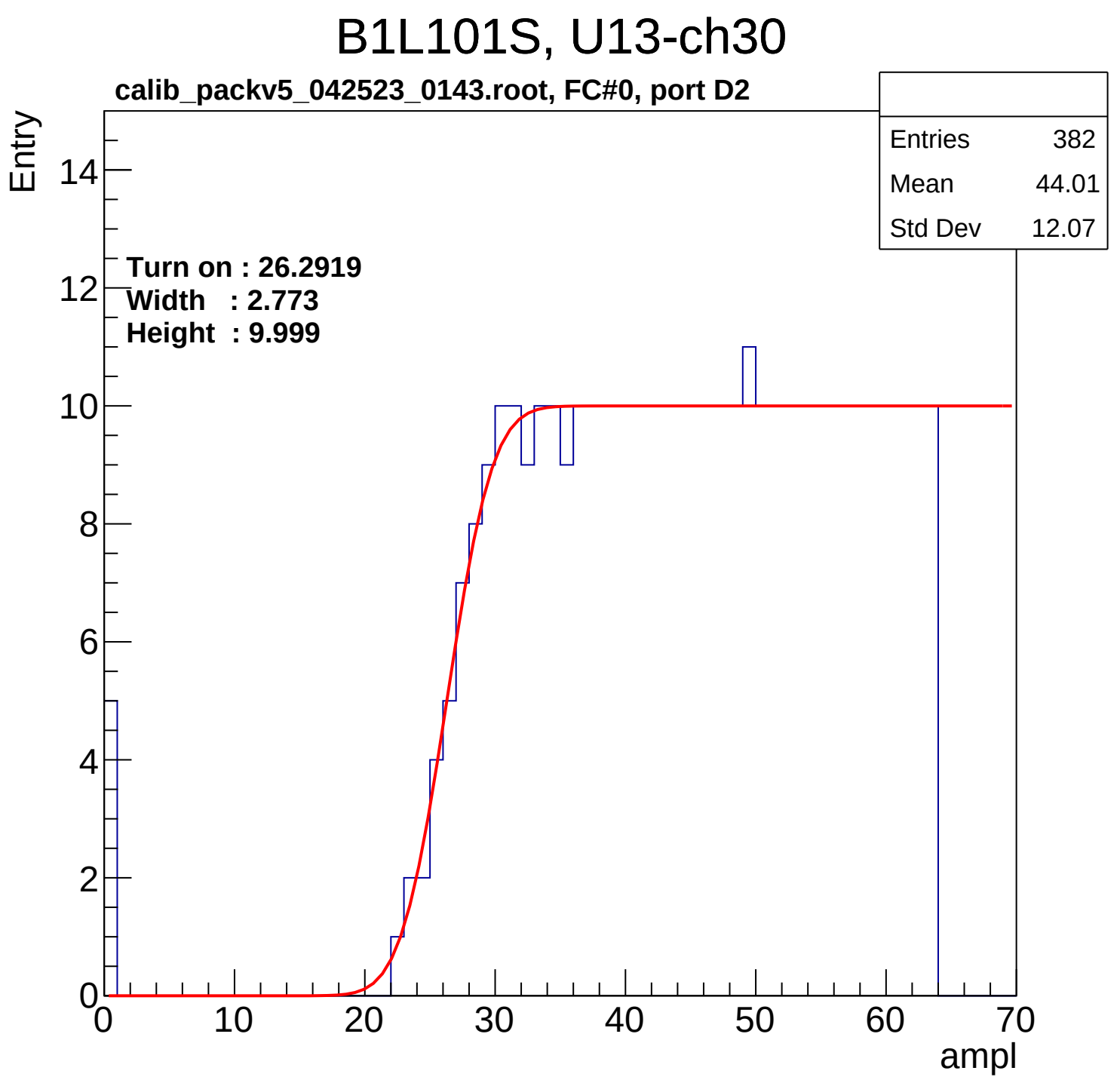
B1L101S, U13-ch30
calib_packv5_042523_0143.root, FC#0, port D2
Entries 382
Mean 44.01
Std Dev 12.07
Turn on : 26.2919
Width : 2.773
Height : 9.999
Entry
ampl
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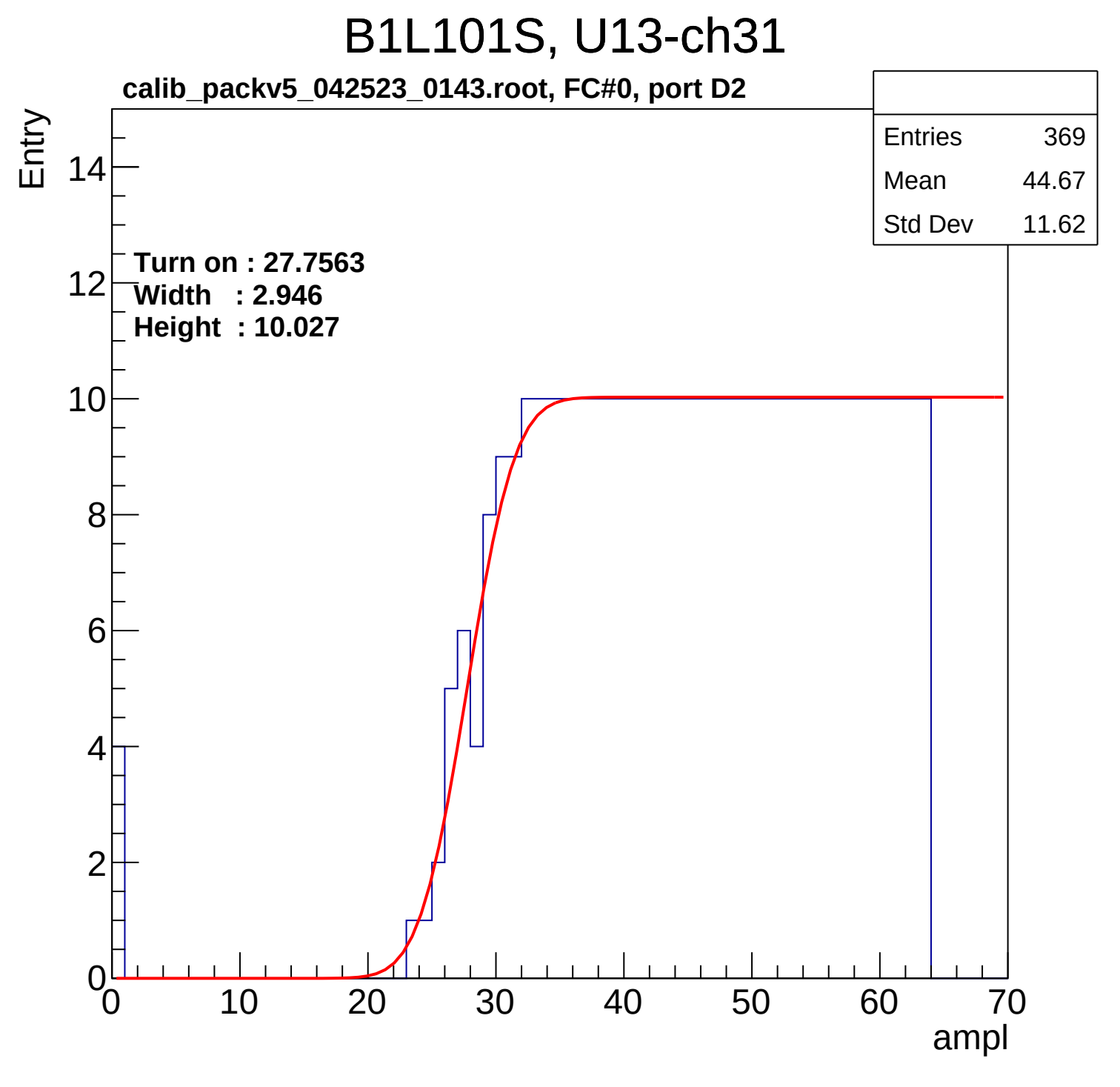
B1L101S, U13-ch31
calib_packv5_042523_0143.root, FC#0, port D2
Entries 369
Mean 44.67
Std Dev 11.62
Turn on : 27.7563
Width : 2.946
Height : 10.027
Entry
ampl
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2
4
6
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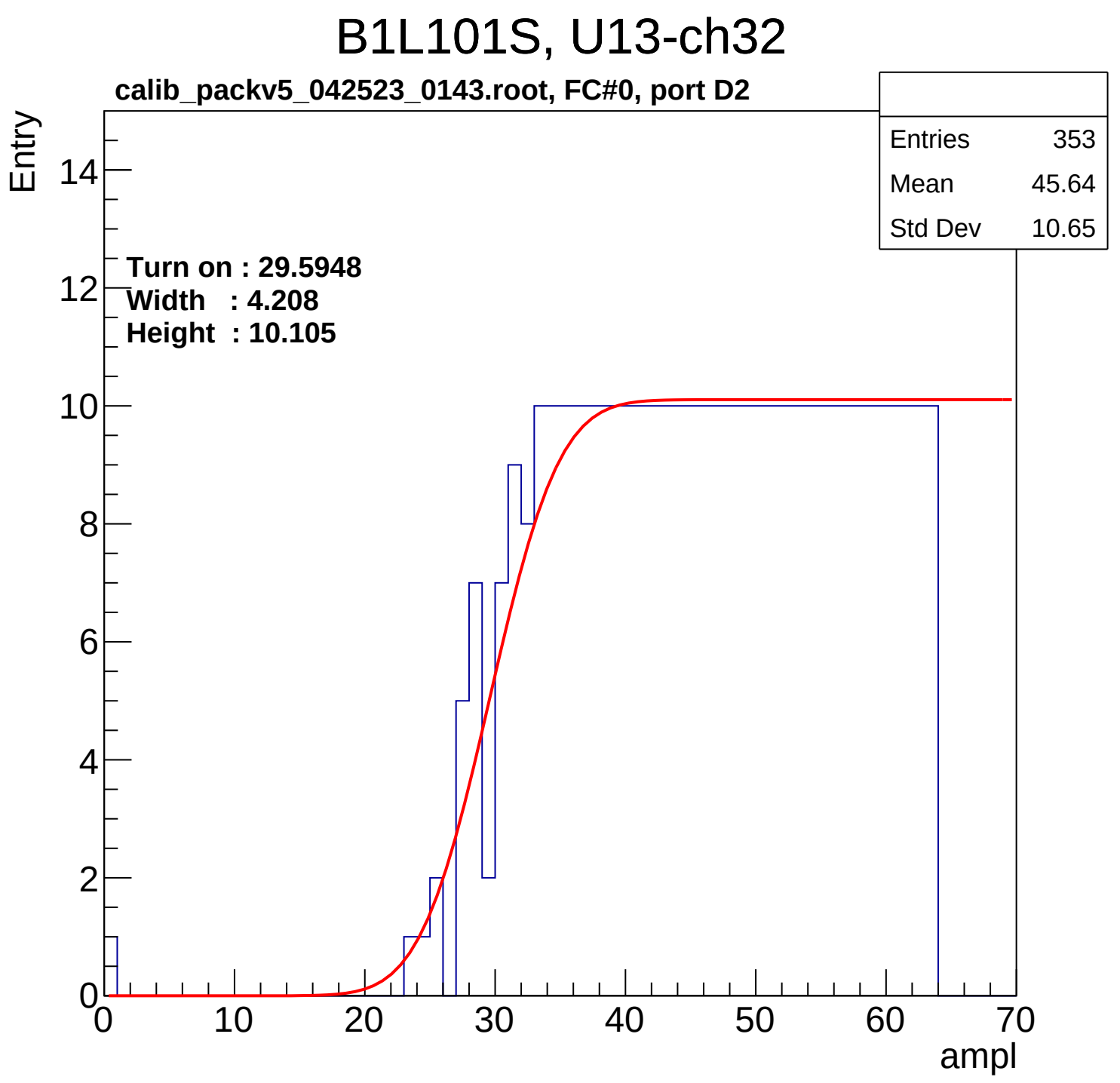
B1L101S, U13-ch32
calib_packv5_042523_0143.root, FC#0, port D2
Entries 353
Mean 45.64
Std Dev 10.65
Turn on : 29.5948
Width : 4.208
Height : 10.105
Entry
ampl
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2
4
6
8
10
12
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0
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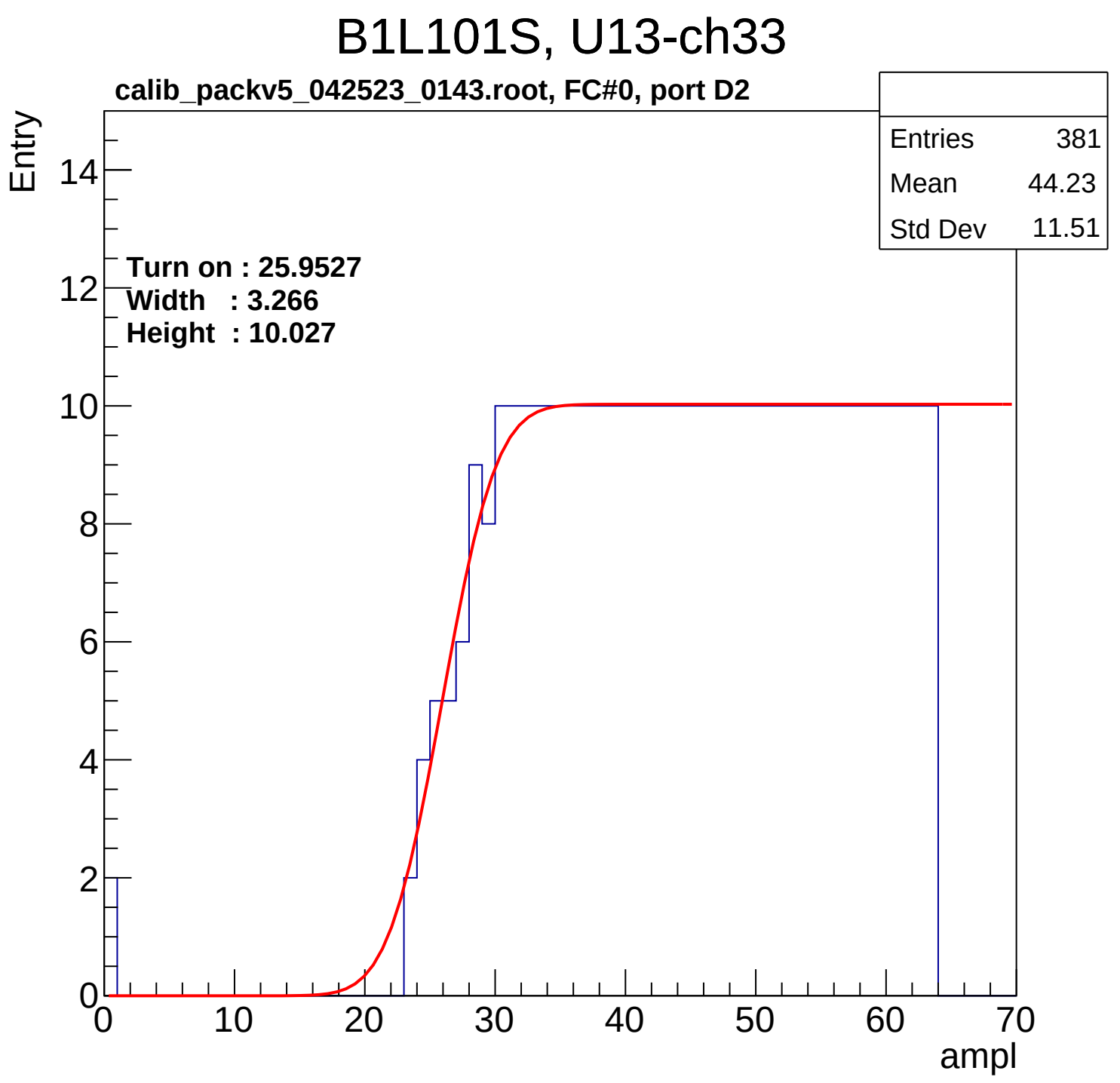
B1L101S, U13-ch33
calib_packv5_042523_0143.root, FC#0, port D2
Entries 381
Mean 44.23
Std Dev 11.51
Turn on : 25.9527
Width : 3.266
Height : 10.027
Entry
ampl
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2
4
6
8
10
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0
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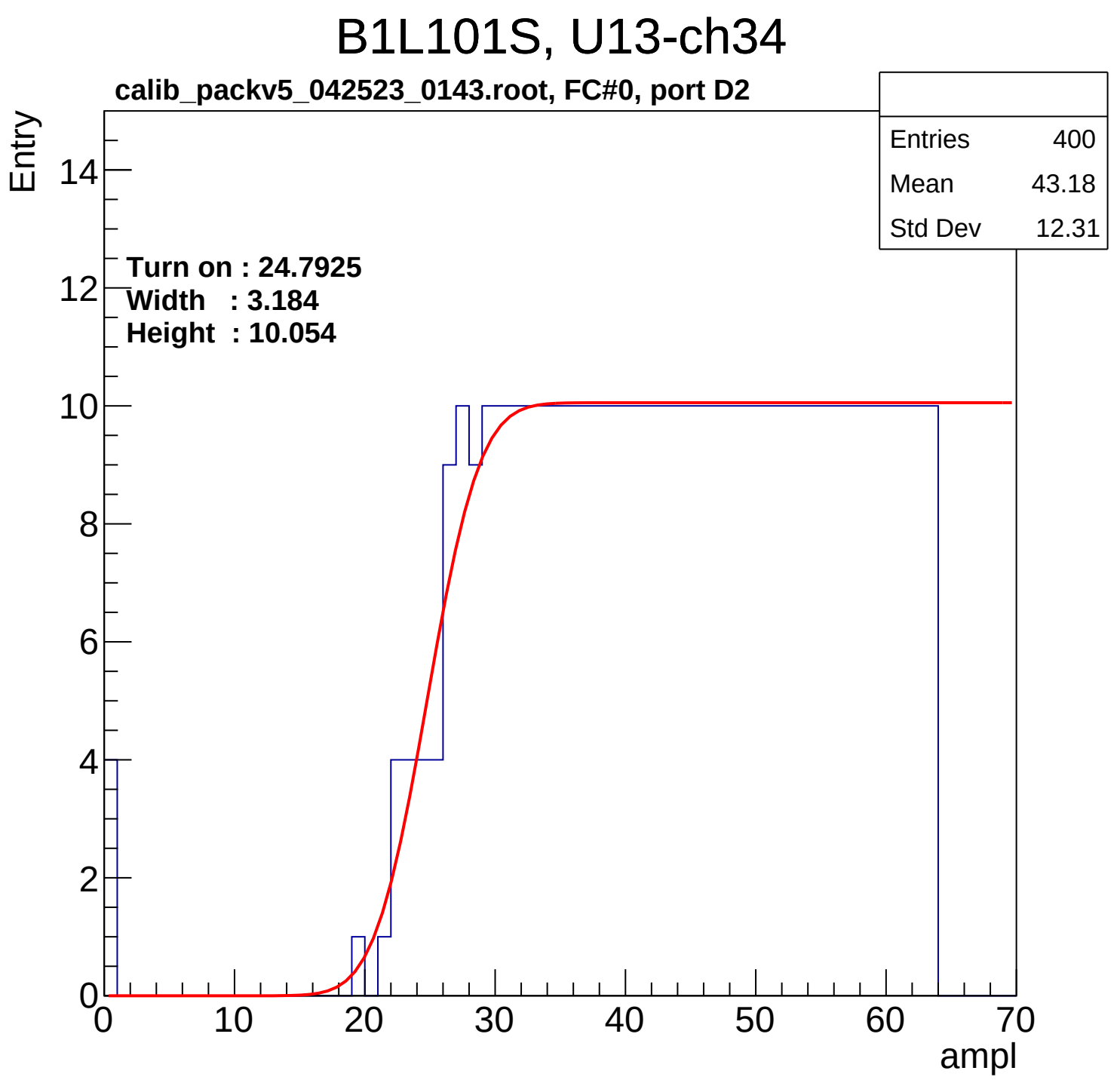
B1L101S, U13-ch34
calib_packv5_042523_0143.root, FC#0, port D2
Entries 400
Mean 43.18
Std Dev 12.31
Turn on : 24.7925
Width : 3.184
Height : 10.054
Entry
ampl
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2
4
6
8
10
12
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0
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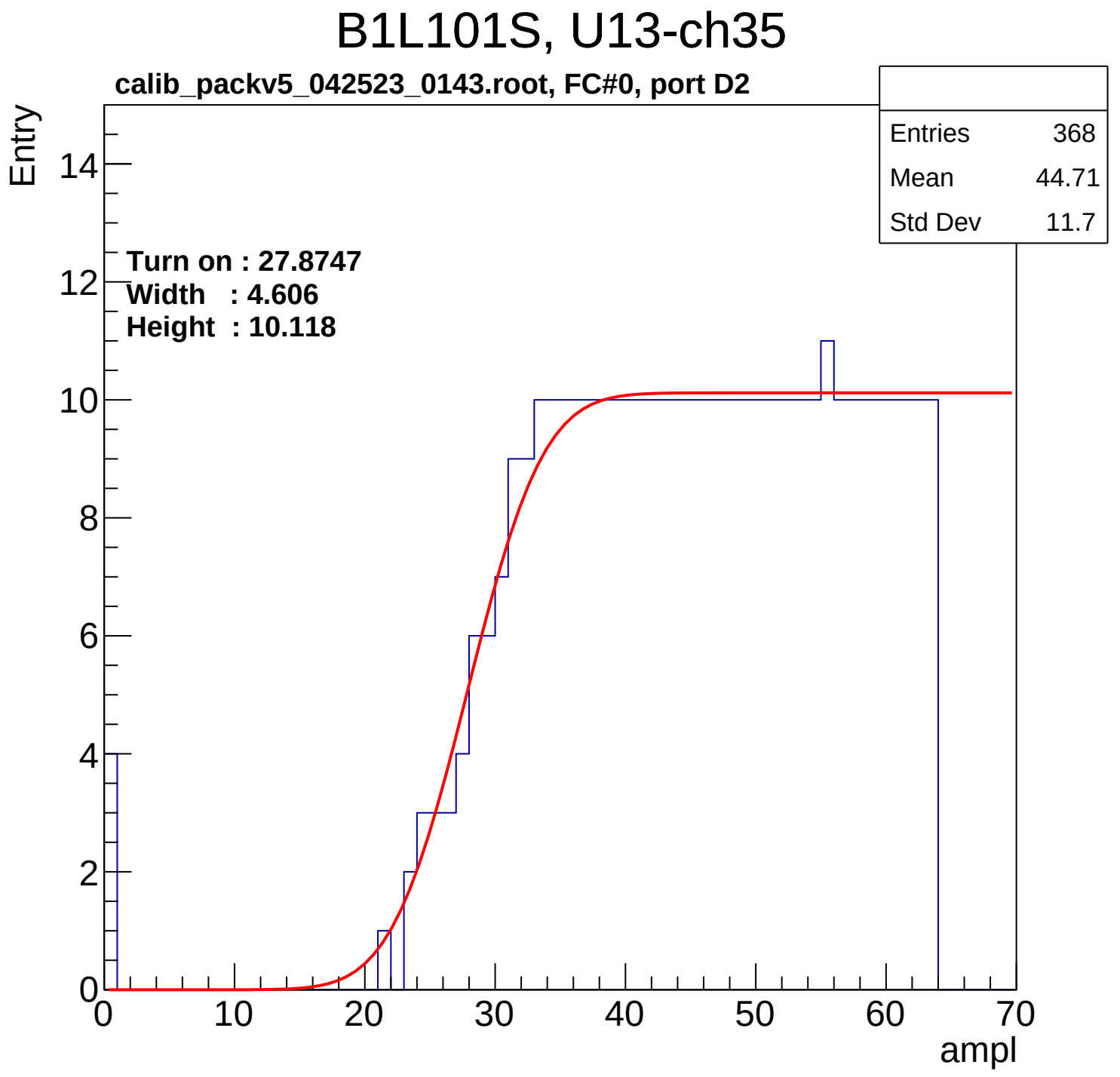
B1L101S, U13-ch35
calib_packv5_042523_0143.root, FC#0, port D2
Entries 368
Mean 44.71
Std Dev 11.7
Turn on : 27.8747
Width : 4.606
Height : 10.118
Entry
ampl
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2
4
6
8
10
12
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0
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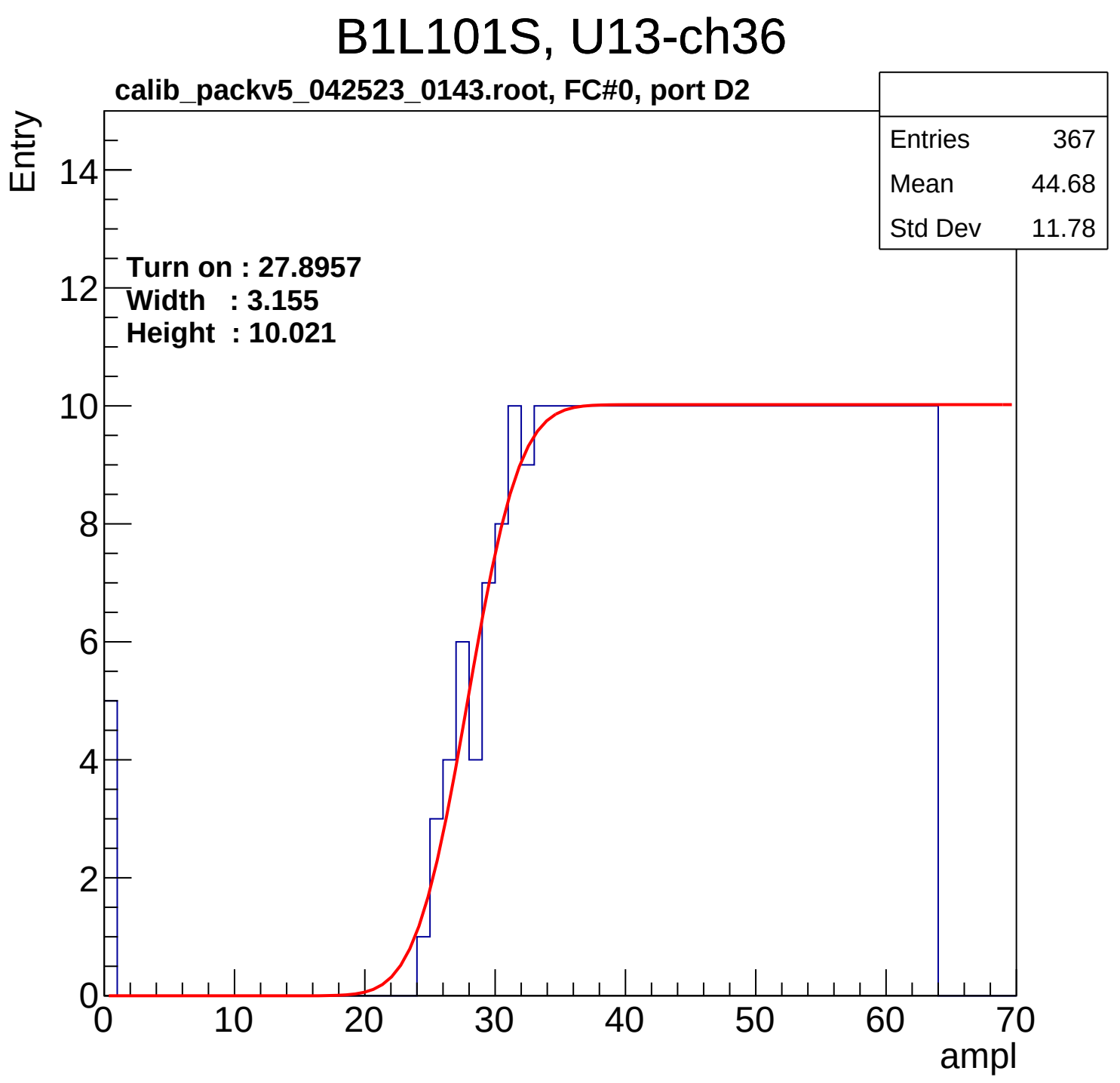
B1L101S, U13-ch36
calib_packv5_042523_0143.root, FC#0, port D2
Entries 367
Mean 44.68
Std Dev 11.78
Turn on : 27.8957
Width : 3.155
Height : 10.021
Entry
ampl
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2
4
6
8
10
12
14
0
10
20
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40
50
60
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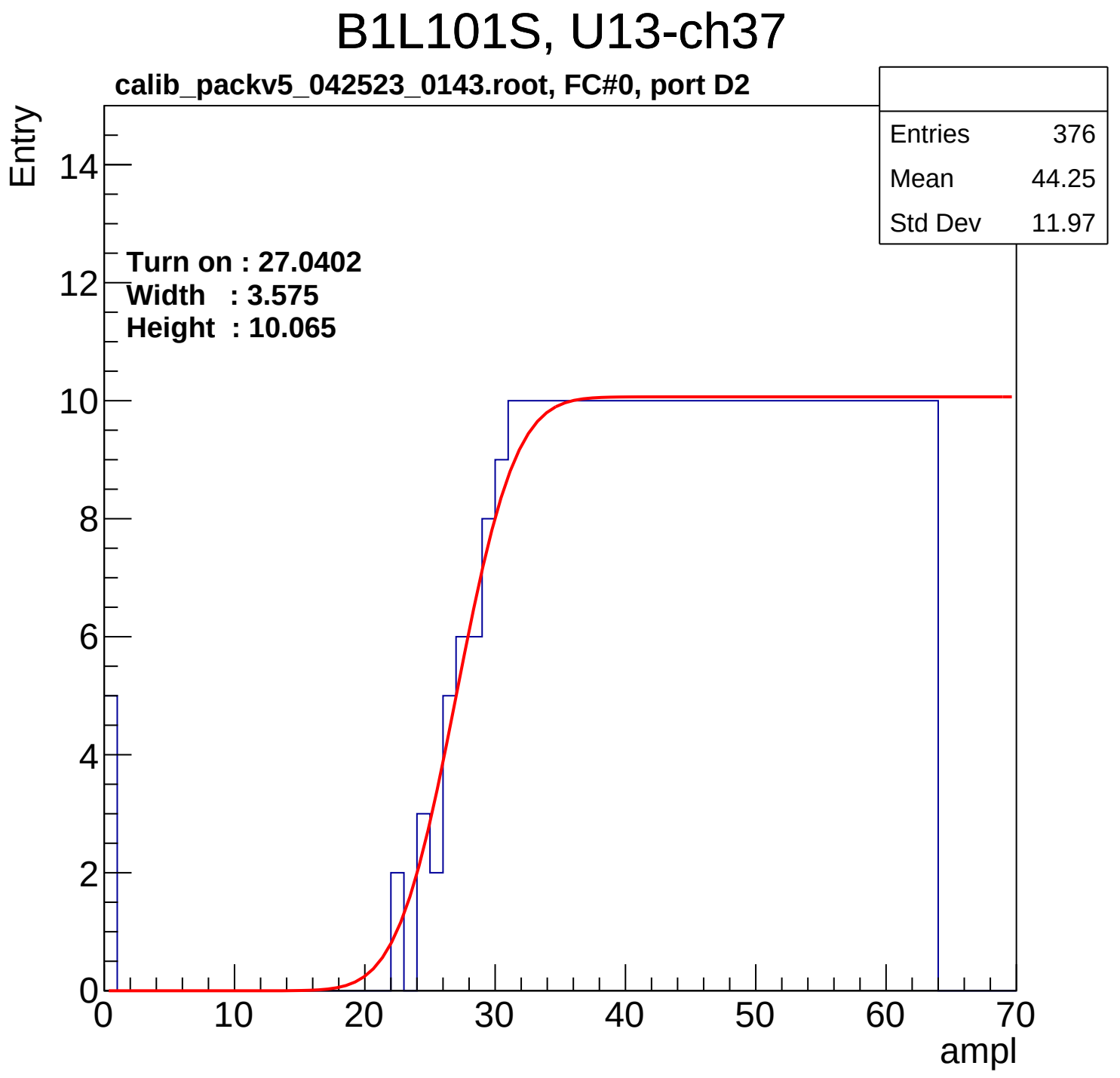
B1L101S, U13-ch37
calib_packv5_042523_0143.root, FC#0, port D2
Entries 376
Mean 44.25
Std Dev 11.97
Turn on : 27.0402
Width : 3.575
Height : 10.065
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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40
50
60
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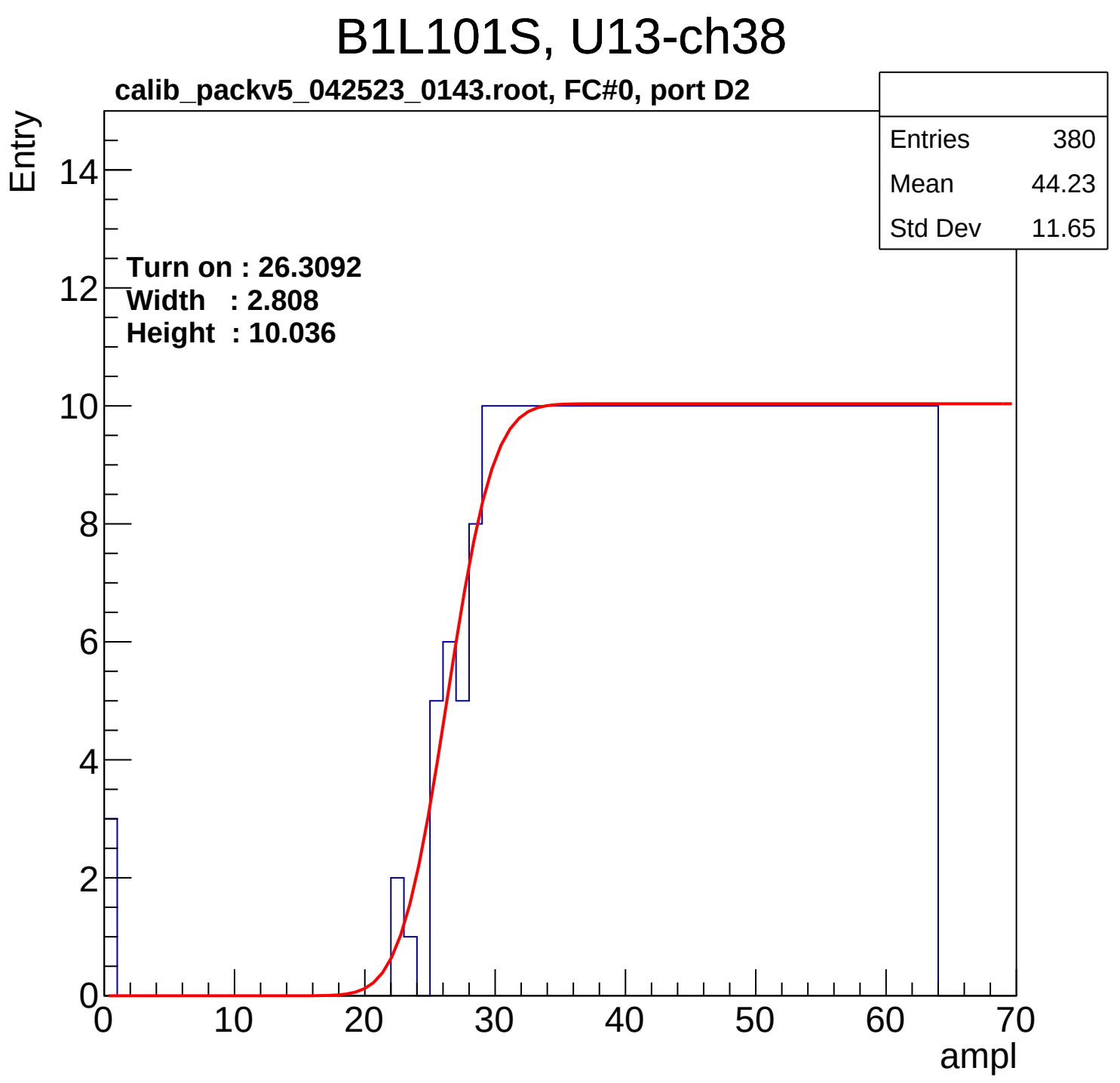
B1L101S, U13-ch38
calib_packv5_042523_0143.root, FC#0, port D2
Entries 380
Mean 44.23
Std Dev 11.65
Turn on : 26.3092
Width : 2.808
Height : 10.036
Entry
ampl
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2
4
6
8
10
12
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0
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20
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40
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60
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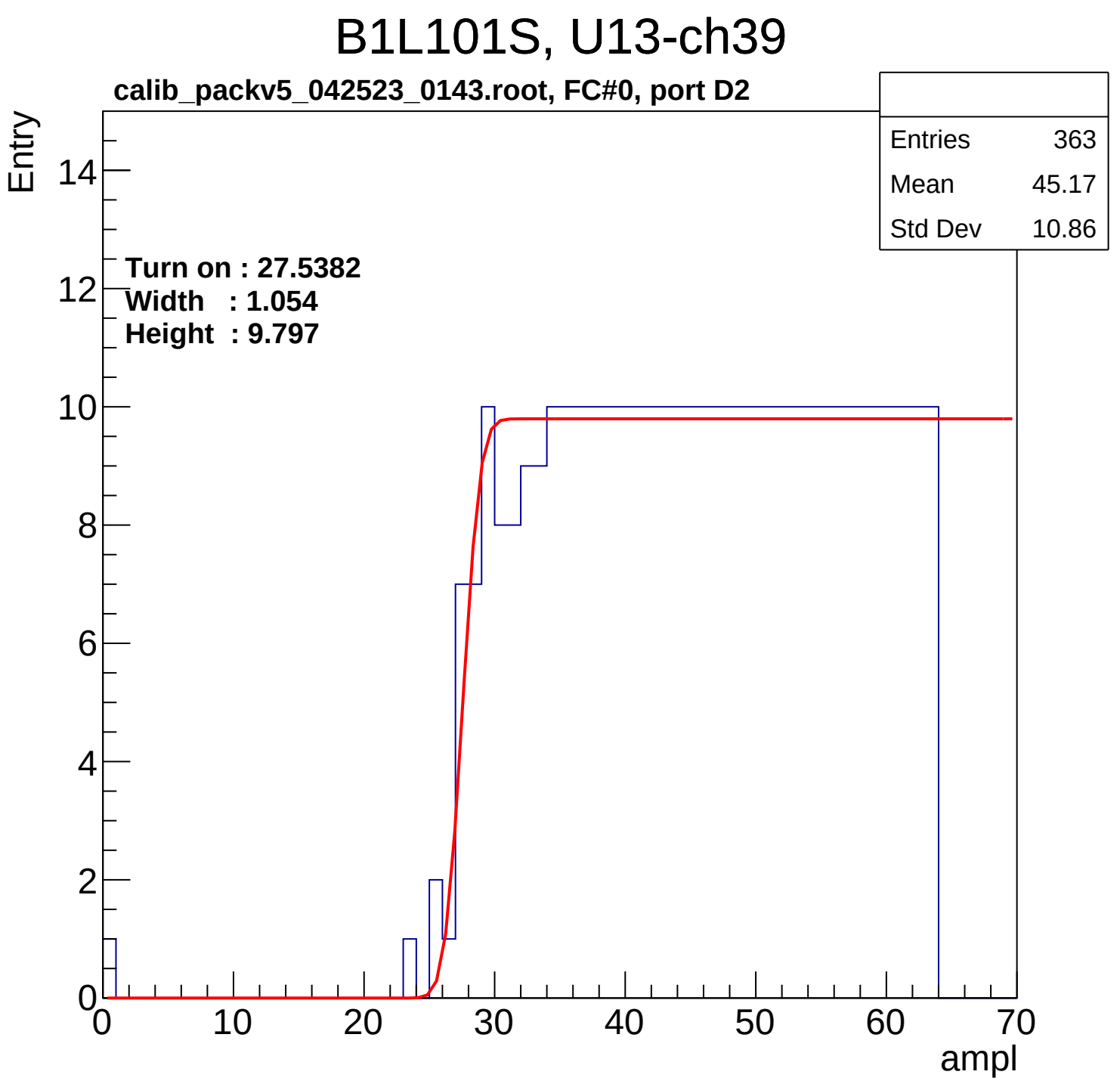
B1L101S, U13-ch39
calib_packv5_042523_0143.root, FC#0, port D2
Entries 363
Mean 45.17
Std Dev 10.86
Turn on : 27.5382
Width : 1.054
Height : 9.797
Entry
ampl
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2
4
6
8
10
12
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0
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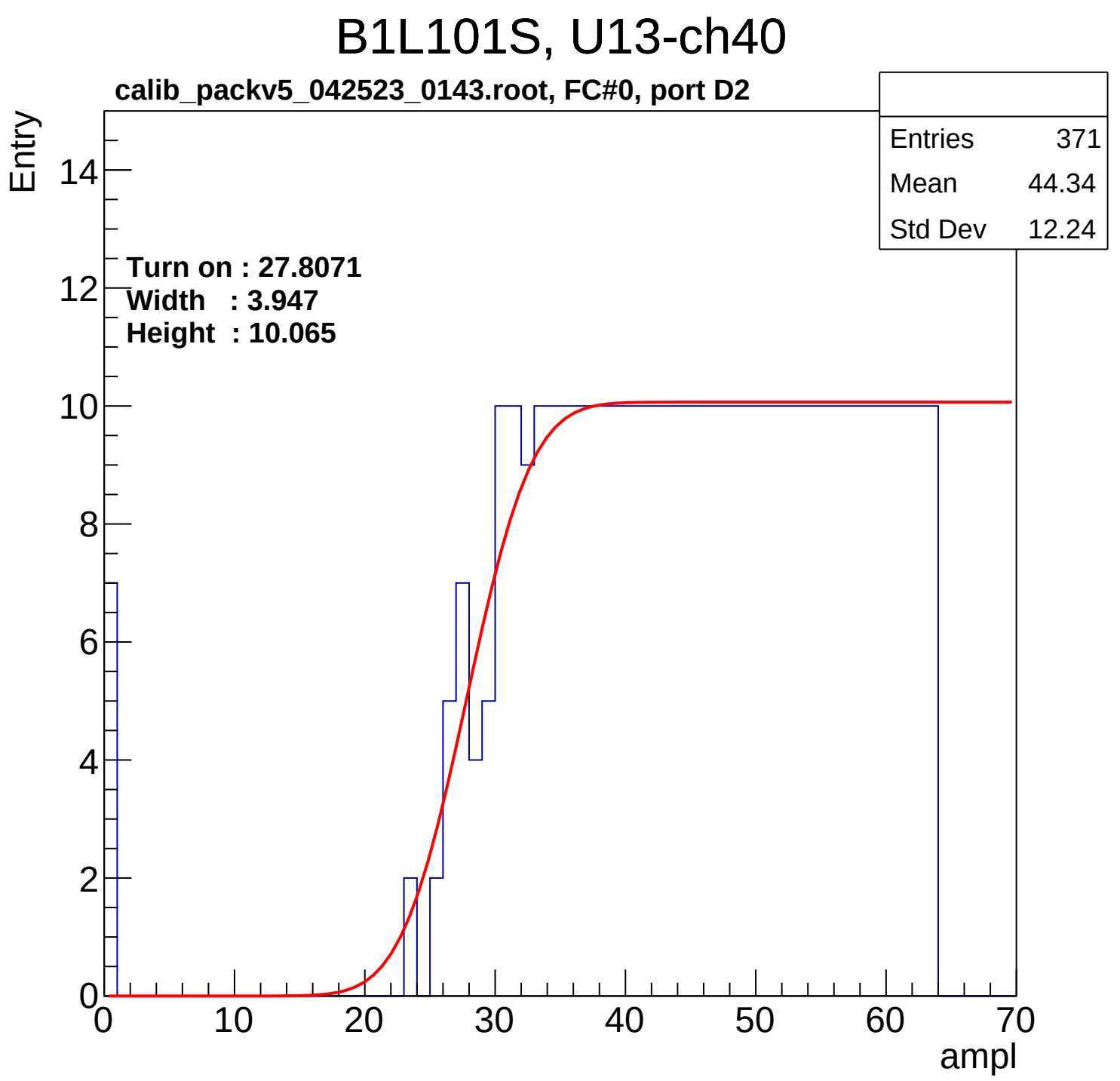
B1L101S, U13-ch40
calib_packv5_042523_0143.root, FC#0, port D2
Entries 371
Mean 44.34
Std Dev 12.24
Turn on : 27.8071
Width : 3.947
Height : 10.065
Entry
ampl
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4
6
8
10
12
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0
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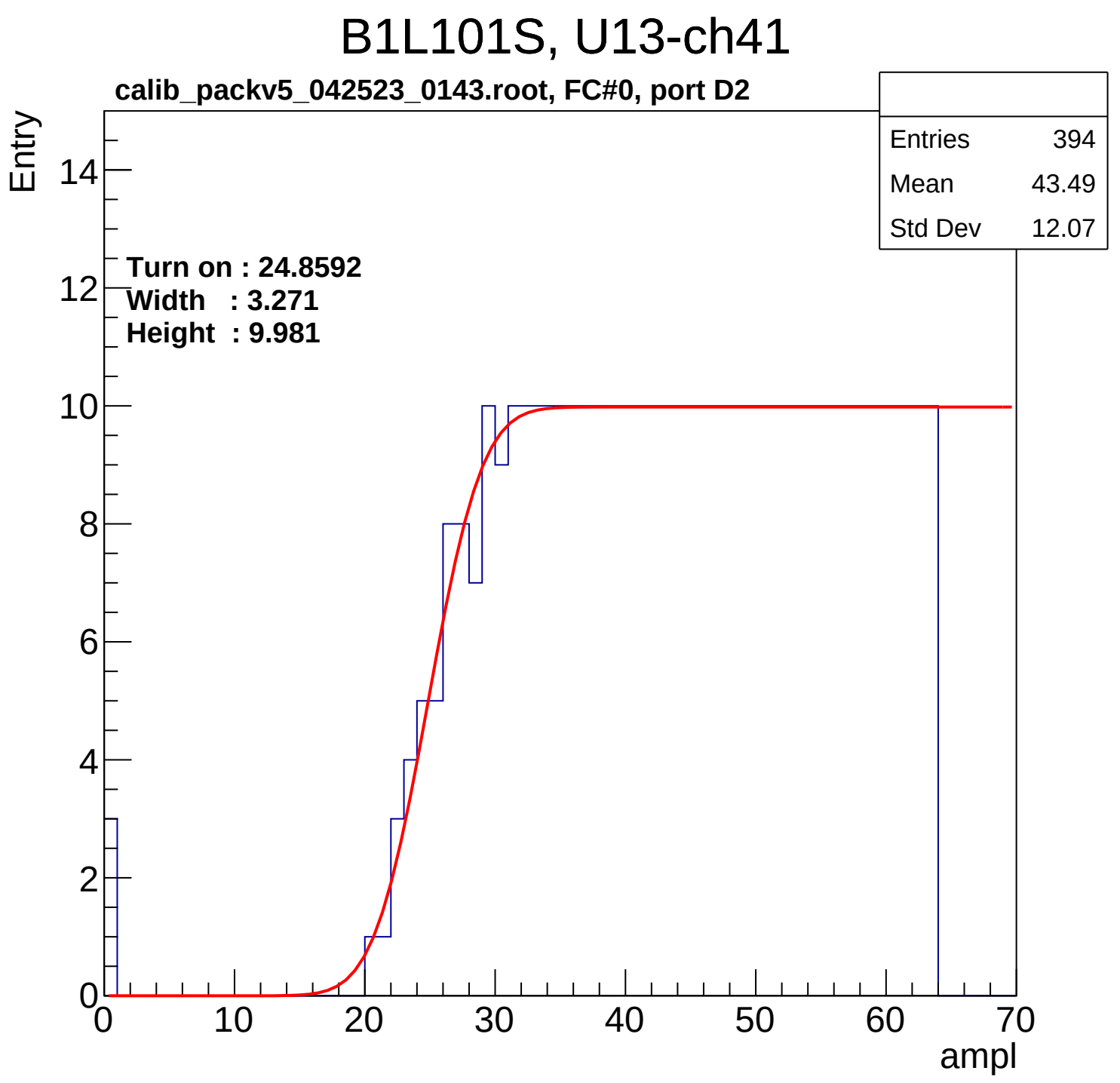
B1L101S, U13-ch41
calib_packv5_042523_0143.root, FC#0, port D2
Entries 394
Mean 43.49
Std Dev 12.07
Turn on : 24.8592
Width : 3.271
Height : 9.981
Entry
ampl
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8
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0
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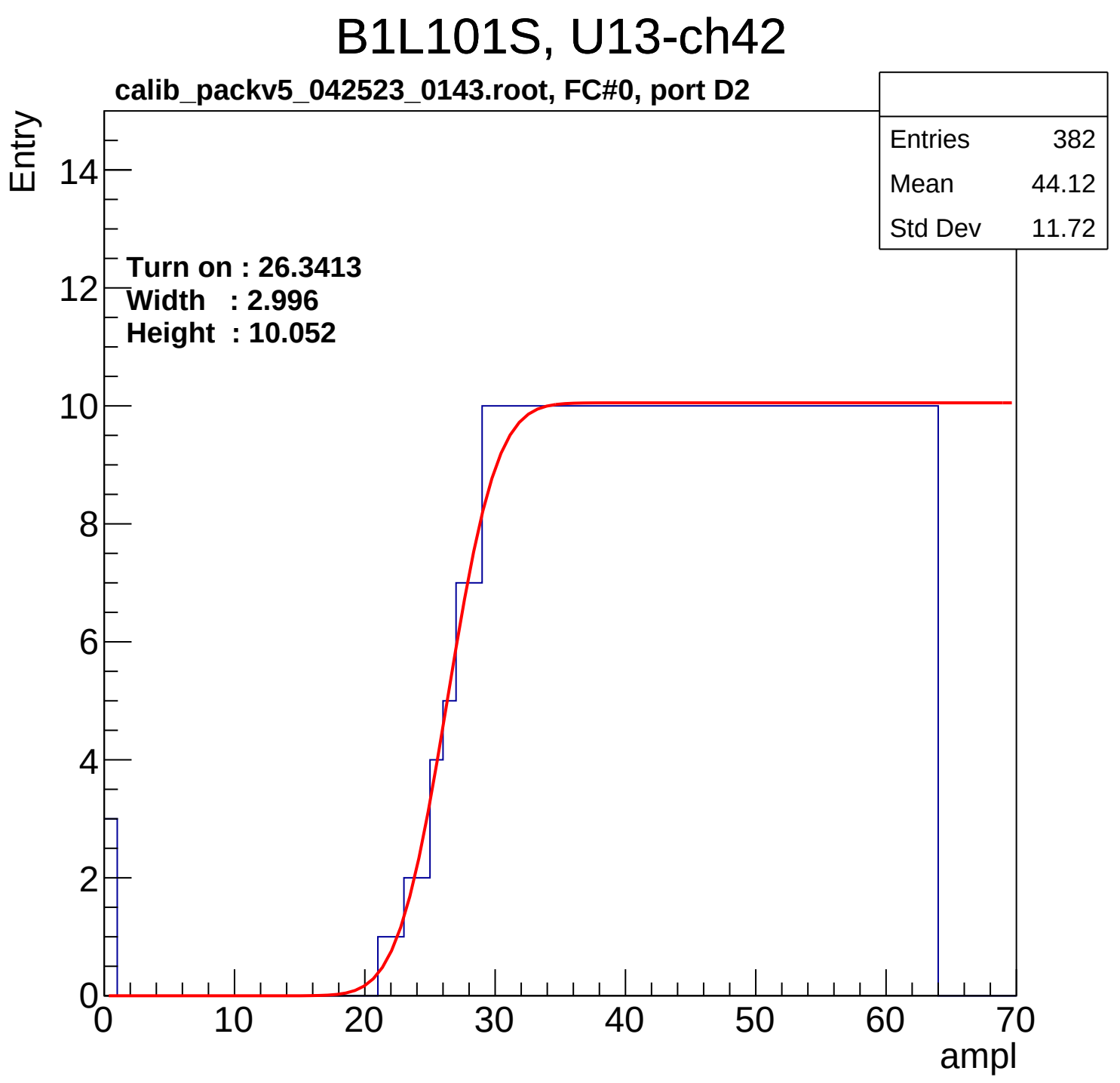
B1L101S, U13-ch42
calib_packv5_042523_0143.root, FC#0, port D2
Entries 382
Mean 44.12
Std Dev 11.72
Turn on : 26.3413
Width : 2.996
Height : 10.052
Entry
ampl
0
2
4
6
8
10
12
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0
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20
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40
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60
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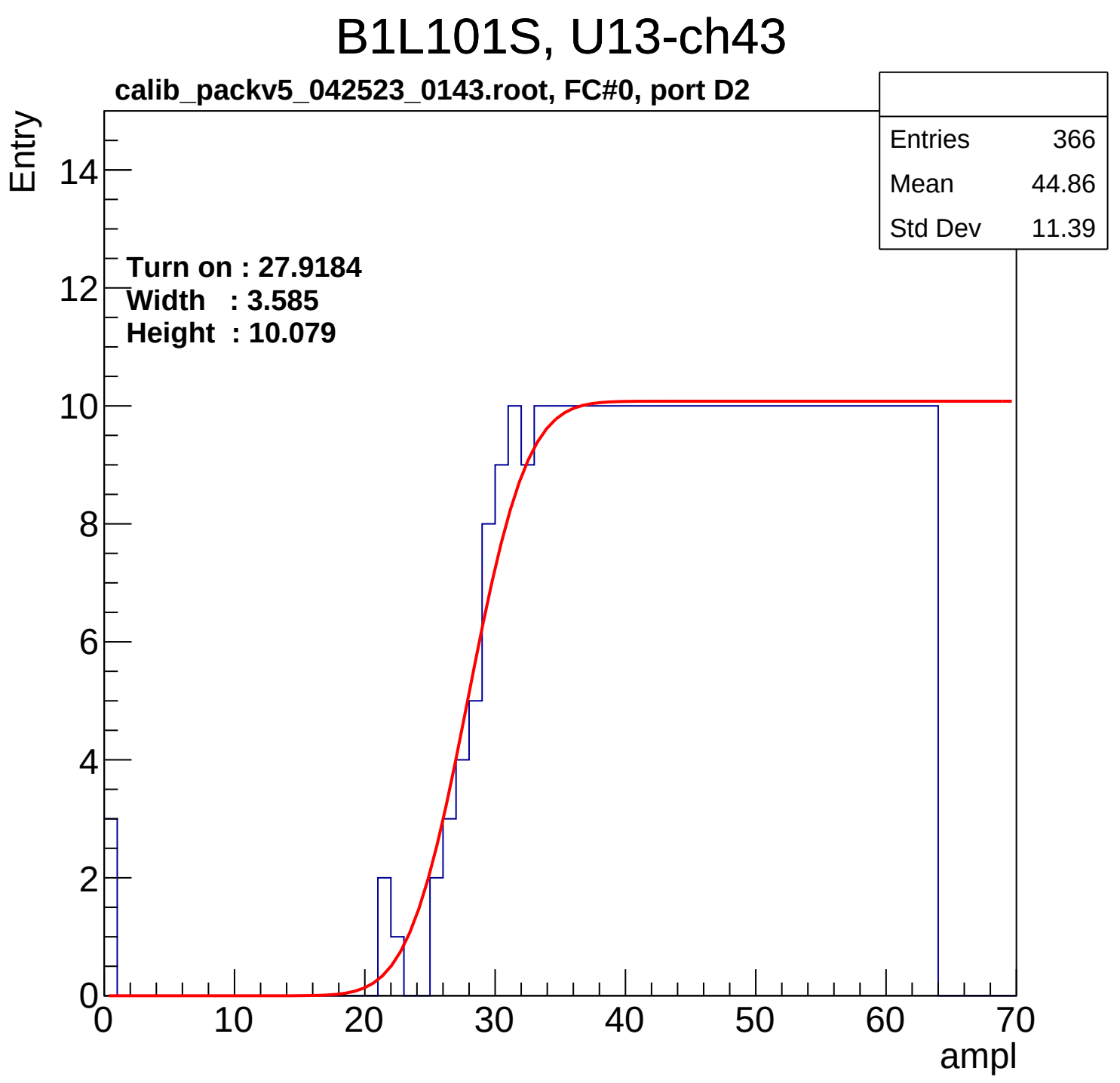
B1L101S, U13-ch43
calib_packv5_042523_0143.root, FC#0, port D2
Entries 366
Mean 44.86
Std Dev 11.39
Turn on : 27.9184
Width : 3.585
Height : 10.079
Entry
ampl
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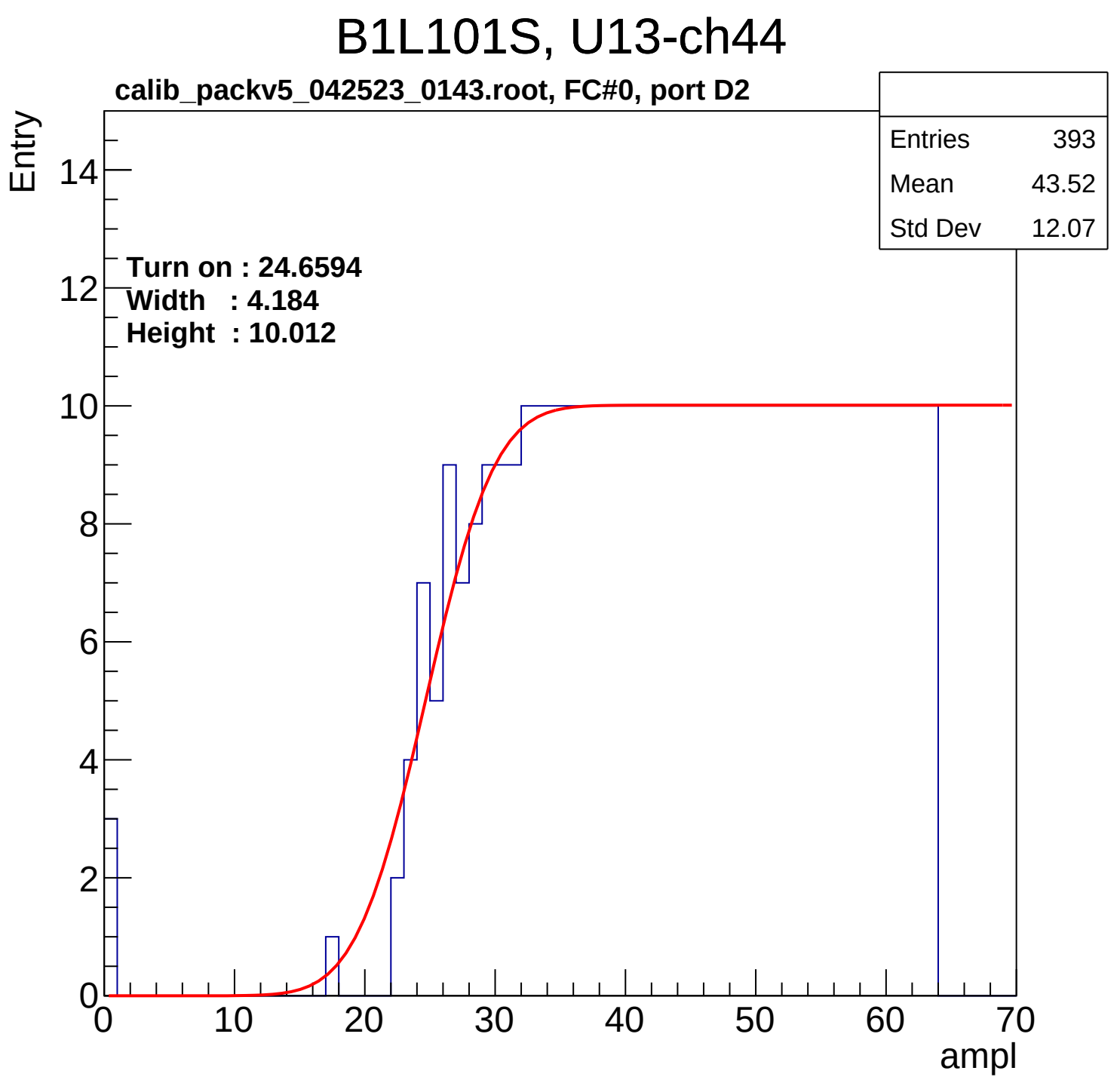
B1L101S, U13-ch44
calib_packv5_042523_0143.root, FC#0, port D2
Entries 393
Mean 43.52
Std Dev 12.07
Turn on : 24.6594
Width : 4.184
Height : 10.012
Entry
ampl
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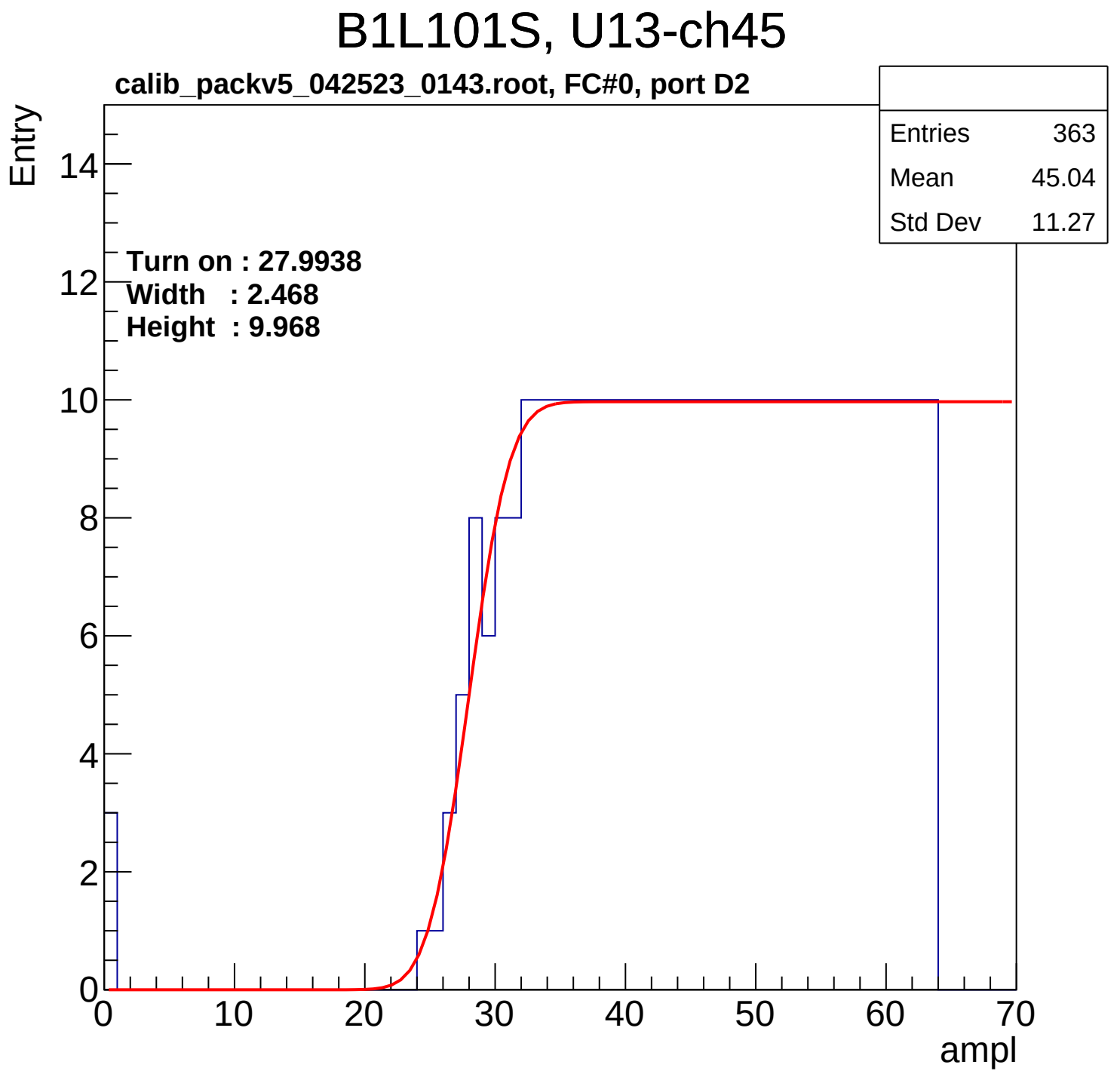
B1L101S, U13-ch45
calib_packv5_042523_0143.root, FC#0, port D2
Entries 363
Mean 45.04
Std Dev 11.27
Turn on : 27.9938
Width : 2.468
Height : 9.968
Entry
ampl
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8
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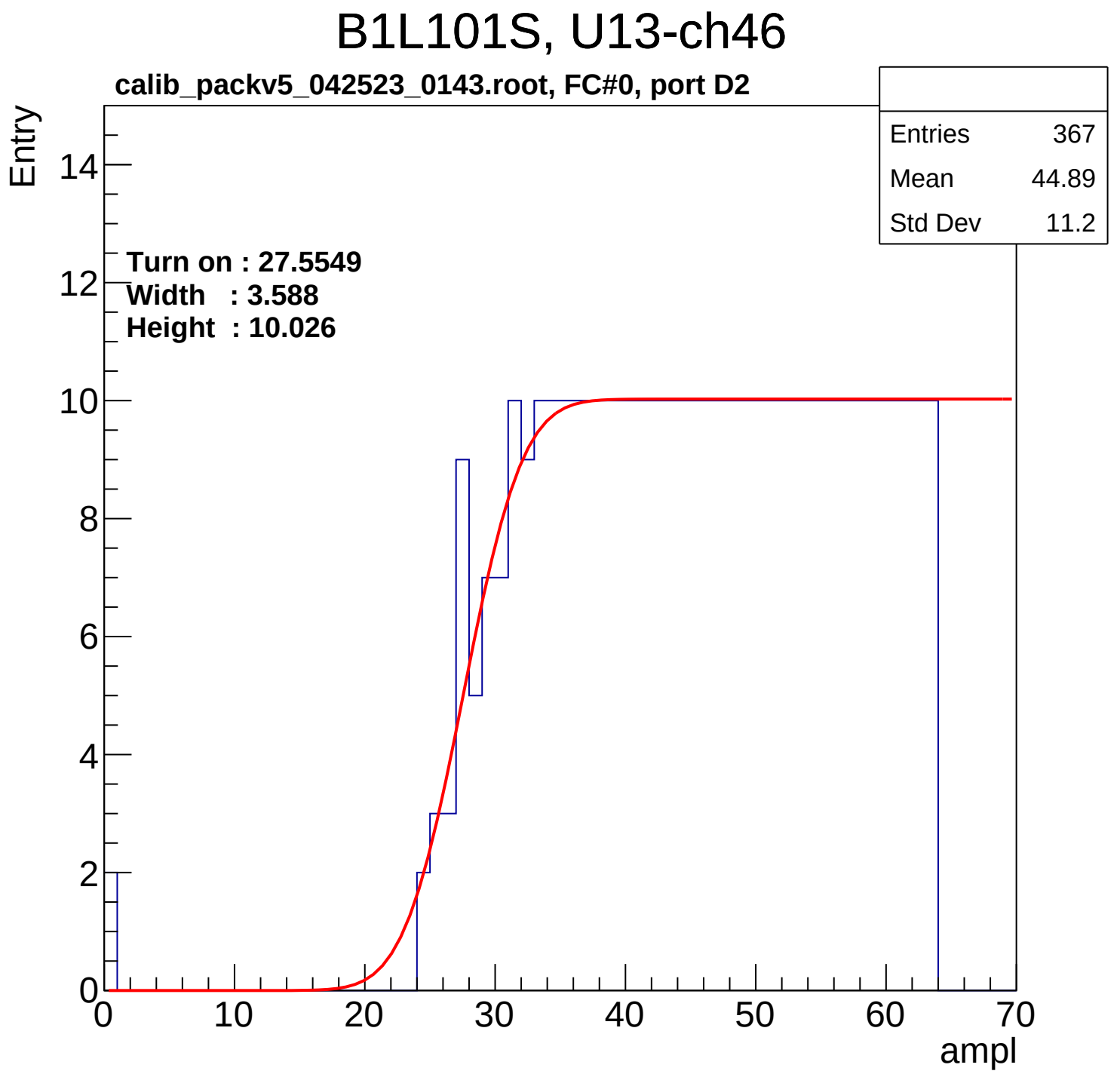
B1L101S, U13-ch46
calib_packv5_042523_0143.root, FC#0, port D2
Entries 367
Mean 44.89
Std Dev 11.2
Turn on : 27.5549
Width : 3.588
Height : 10.026
Entry
ampl
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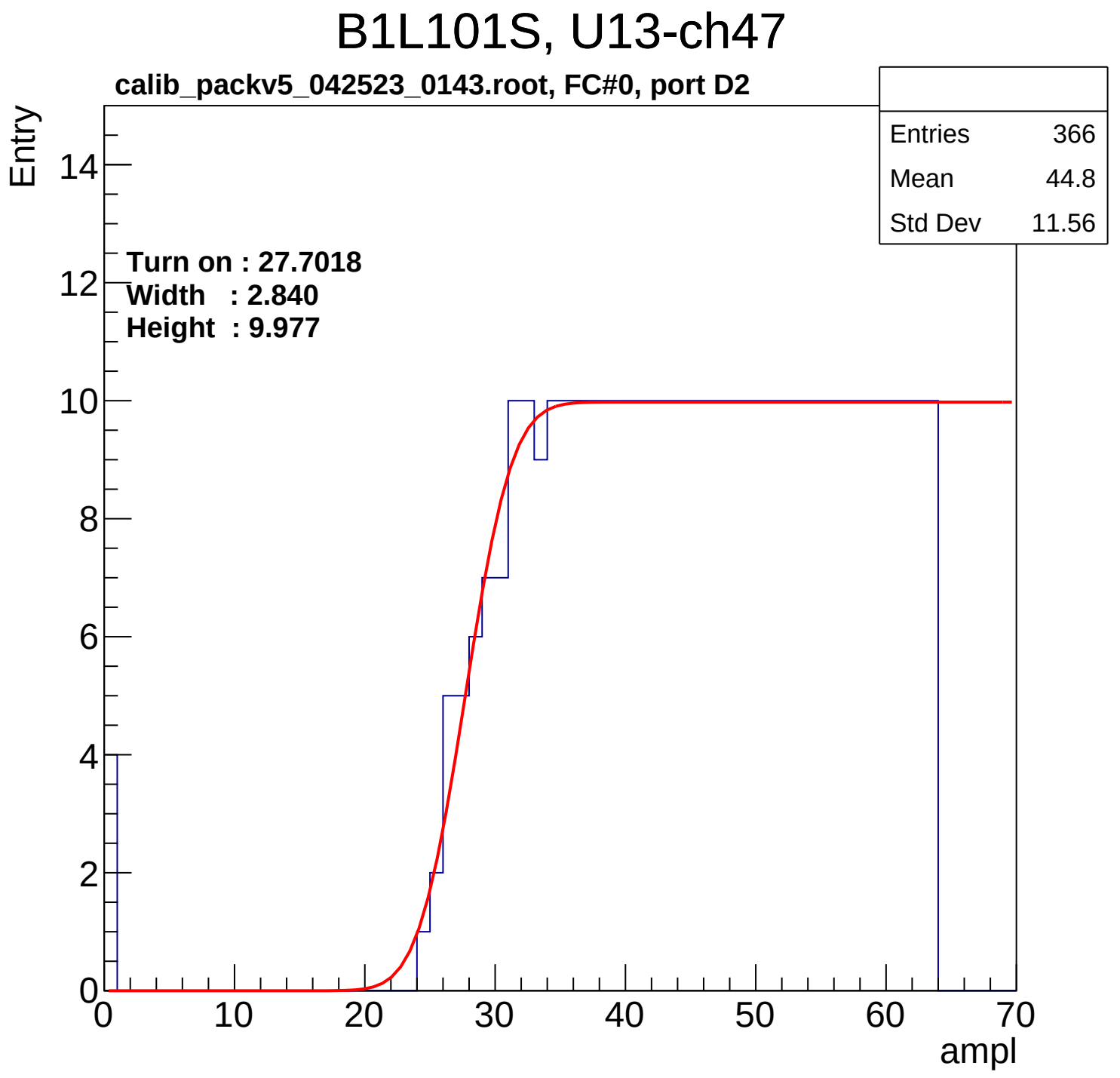
B1L101S, U13-ch47
calib_packv5_042523_0143.root, FC#0, port D2
Entries 366
Mean 44.8
Std Dev 11.56
Turn on : 27.7018
Width : 2.840
Height : 9.977
Entry
ampl
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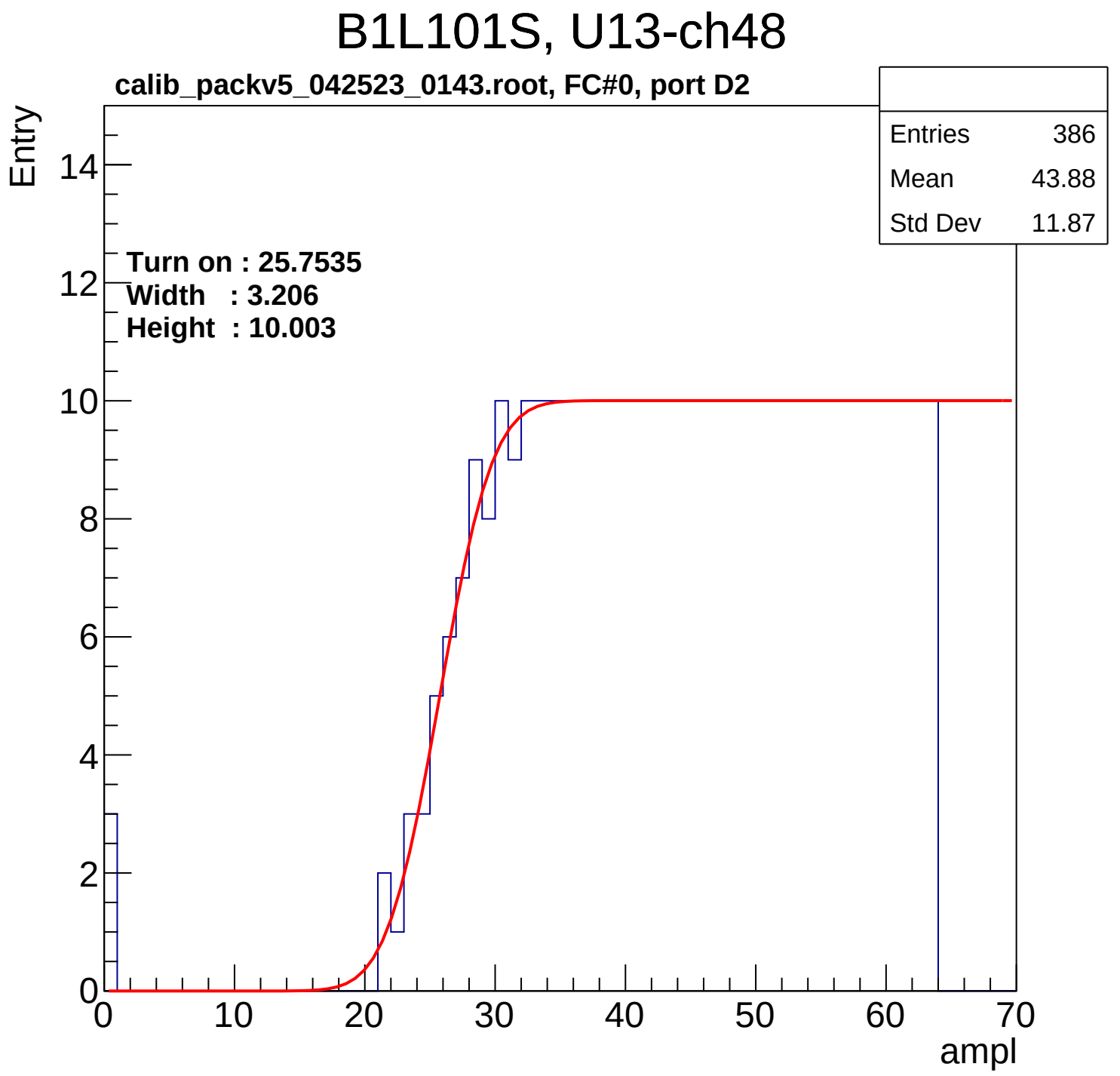
B1L101S, U13-ch48
calib_packv5_042523_0143.root, FC#0, port D2
Entries 386
Mean 43.88
Std Dev 11.87
Turn on : 25.7535
Width : 3.206
Height : 10.003
Entry
ampl
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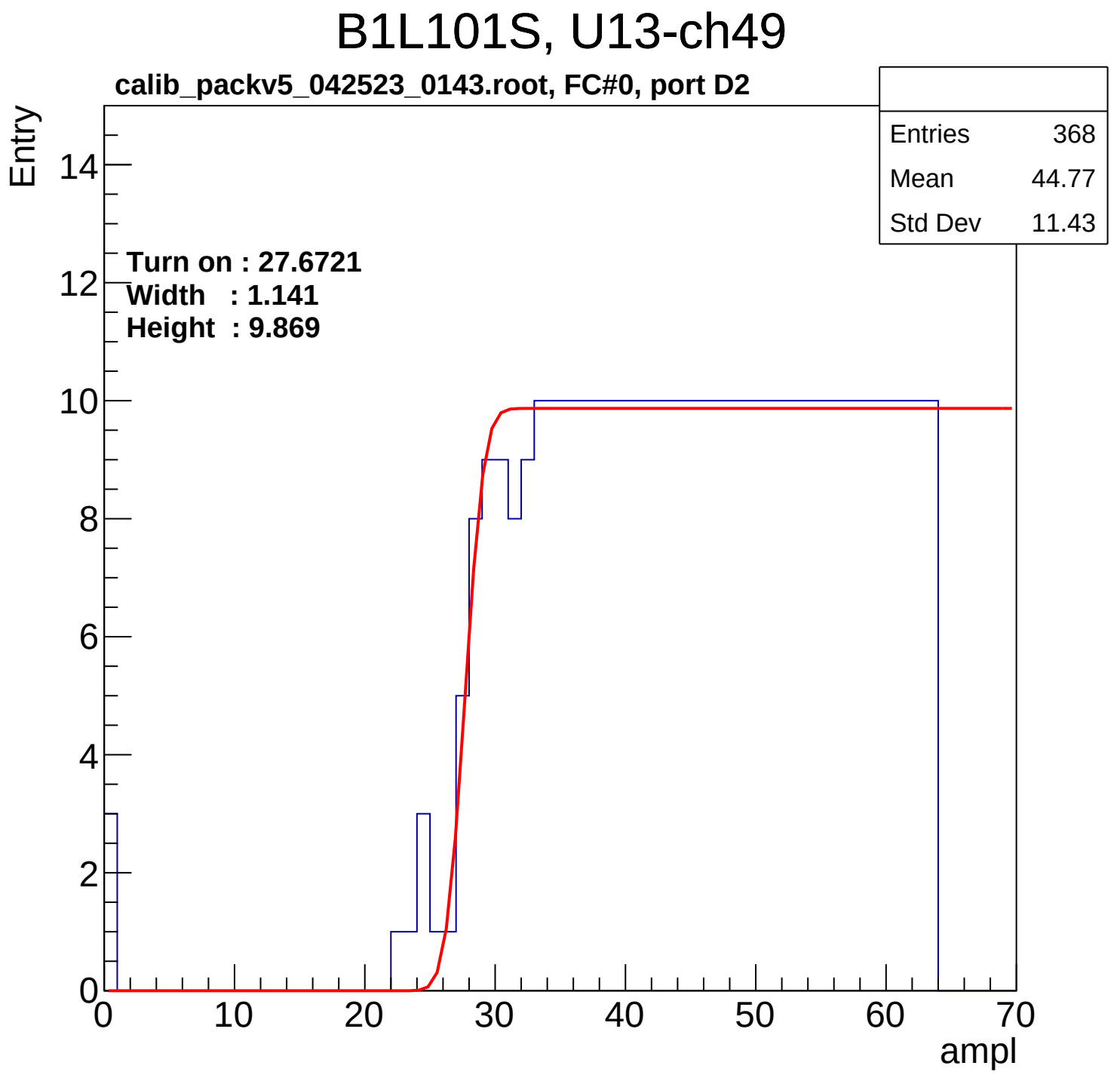
B1L101S, U13-ch49
calib_packv5_042523_0143.root, FC#0, port D2
Entries 368
Mean 44.77
Std Dev 11.43
Turn on : 27.6721
Width : 1.141
Height : 9.869
Entry
ampl
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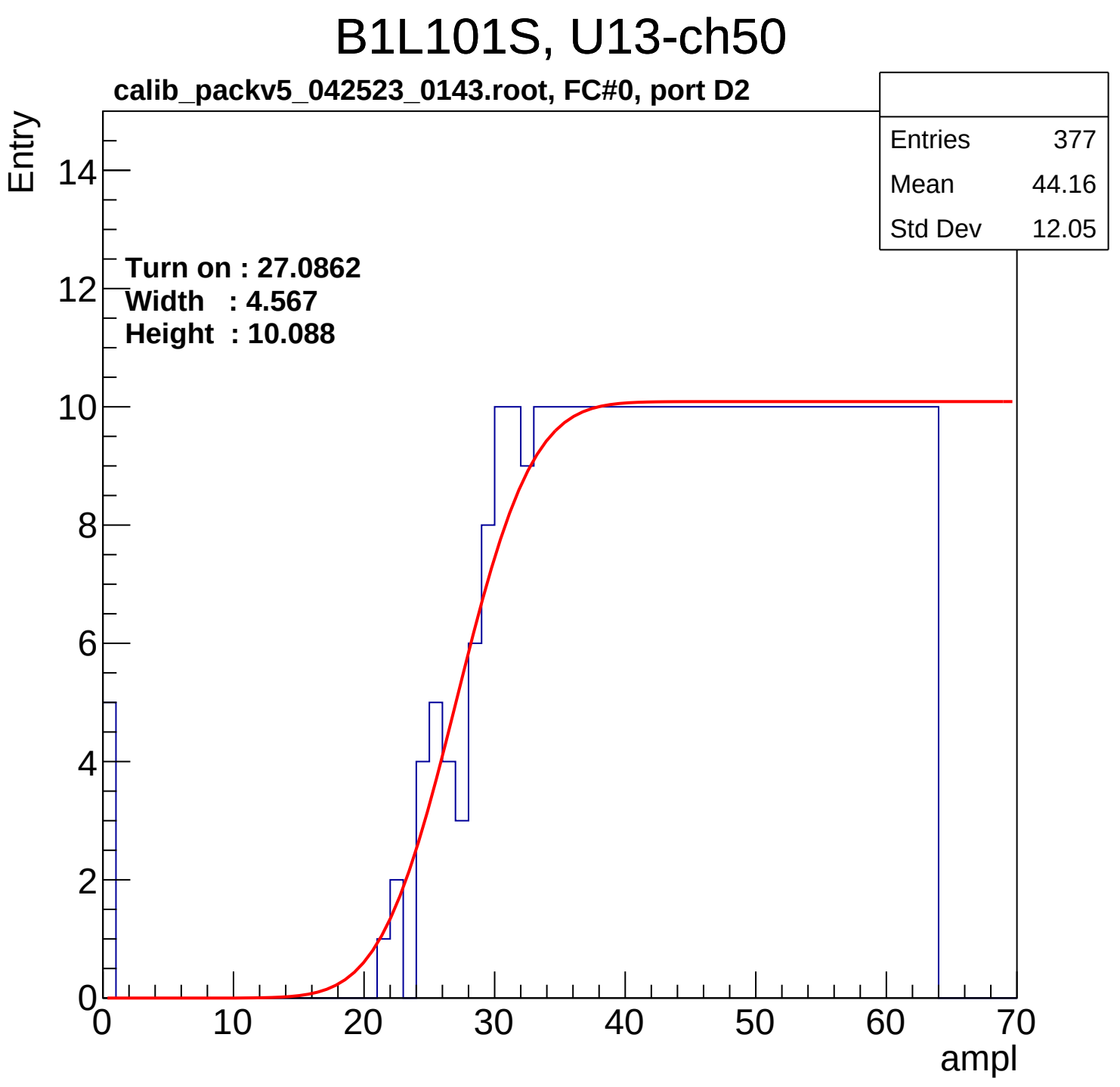
B1L101S, U13-ch50
calib_packv5_042523_0143.root, FC#0, port D2
Entries 377
Mean 44.16
Std Dev 12.05
Turn on : 27.0862
Width : 4.567
Height : 10.088
Entry
ampl
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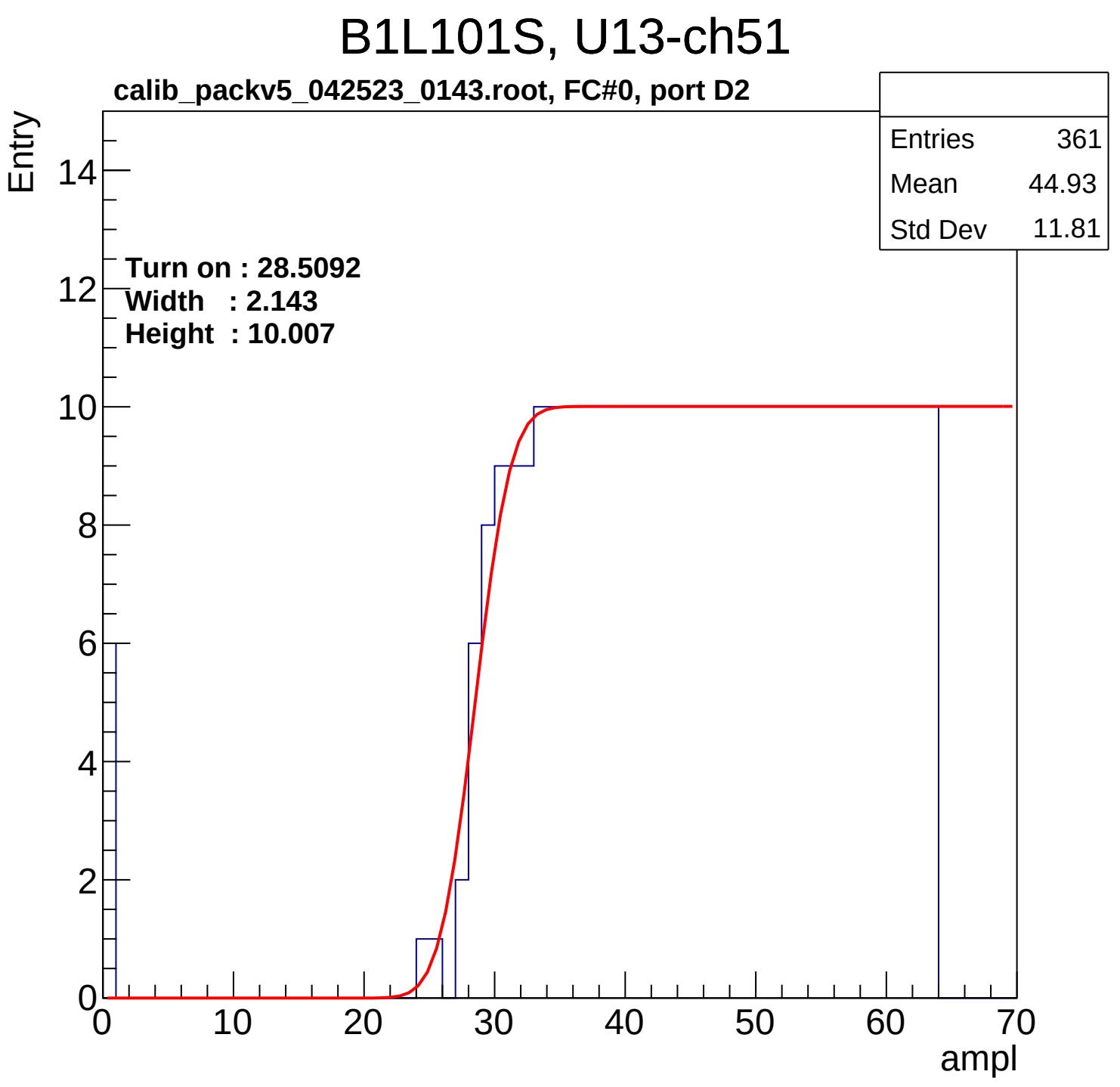
B1L101S, U13-ch51
calib_packv5_042523_0143.root, FC#0, port D2
Entries 361
Mean 44.93
Std Dev 11.81
Turn on : 28.5092
Width : 2.143
Height : 10.007
Entry
ampl
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2
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6
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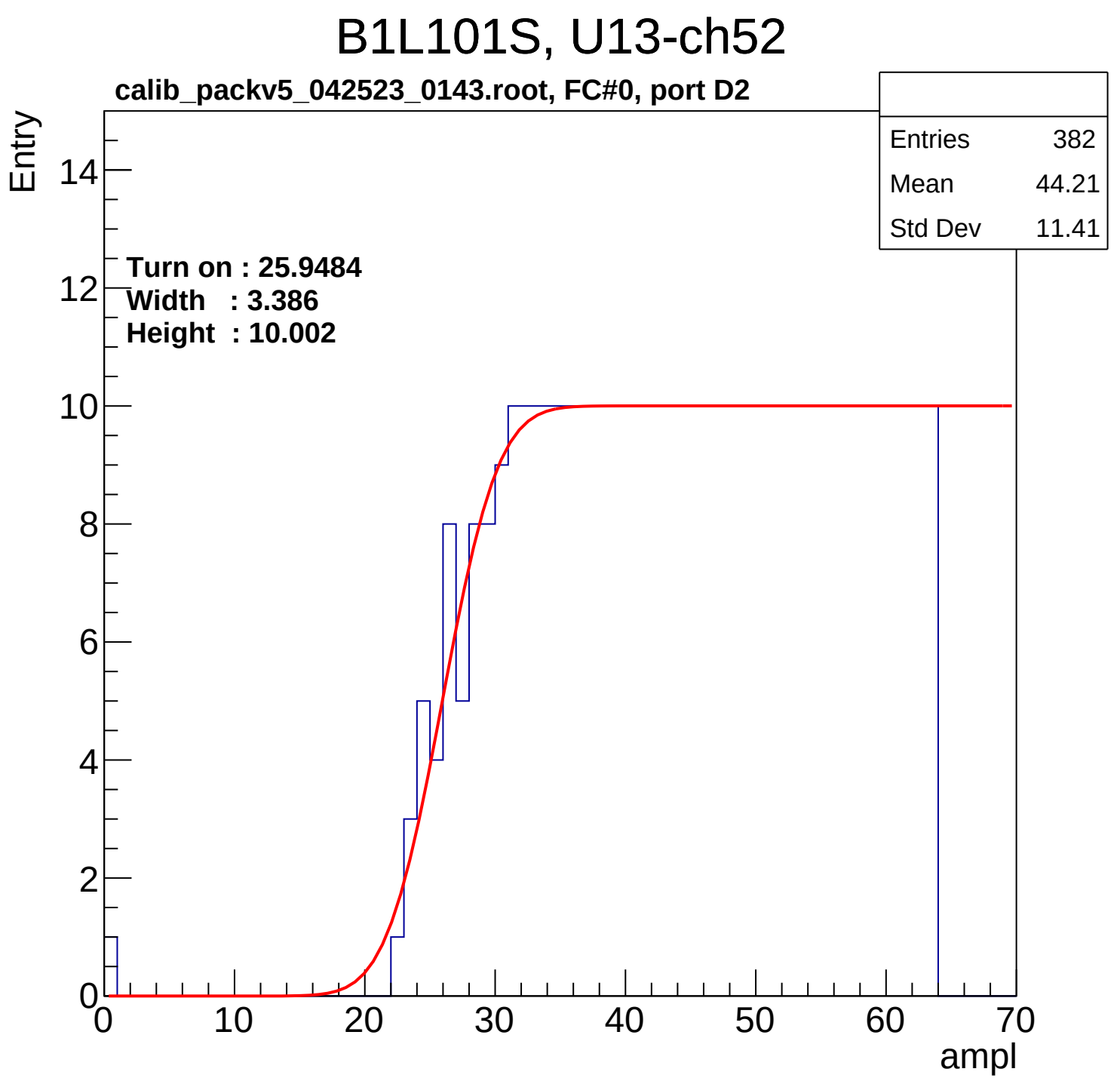
B1L101S, U13-ch52
calib_packv5_042523_0143.root, FC#0, port D2
Entries 382
Mean 44.21
Std Dev 11.41
Turn on : 25.9484
Width : 3.386
Height : 10.002
Entry
ampl
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8
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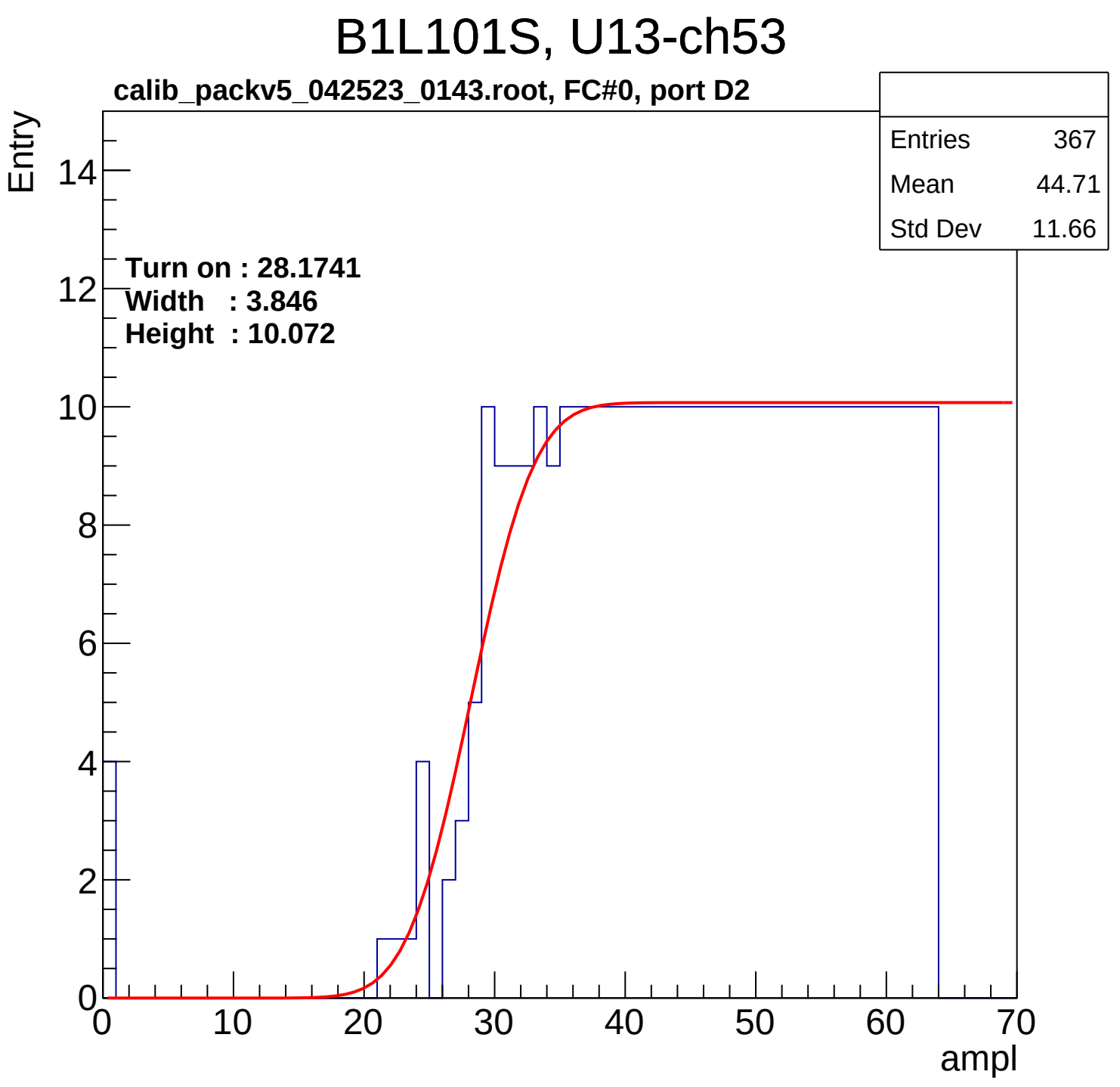
B1L101S, U13-ch53
calib_packv5_042523_0143.root, FC#0, port D2
Entries 367
Mean 44.71
Std Dev 11.66
Turn on : 28.1741
Width : 3.846
Height : 10.072
Entry
ampl
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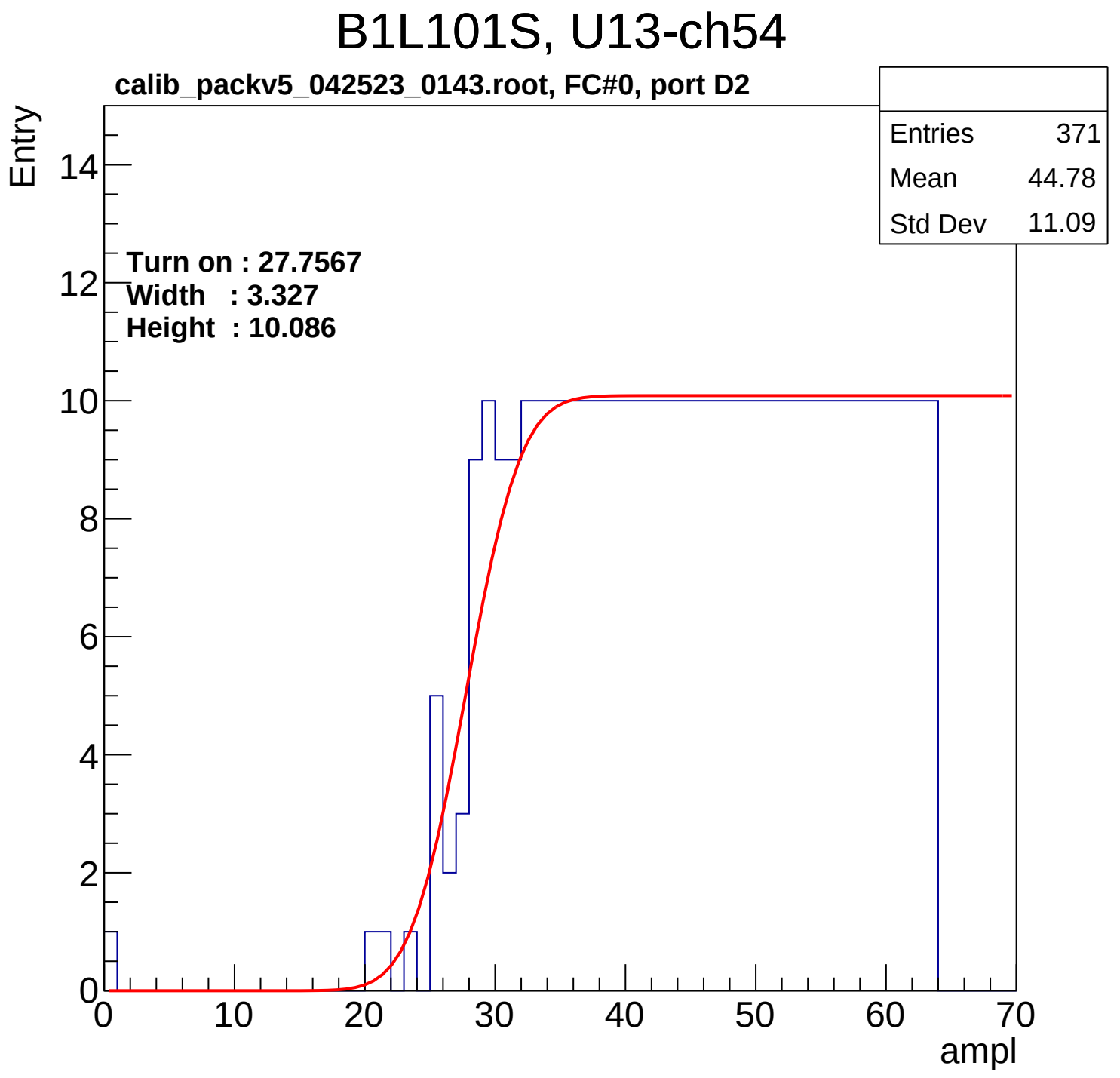
B1L101S, U13-ch54
calib_packv5_042523_0143.root, FC#0, port D2
Entries 371
Mean 44.78
Std Dev 11.09
Turn on : 27.7567
Width : 3.327
Height : 10.086
Entry
ampl
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2
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6
8
10
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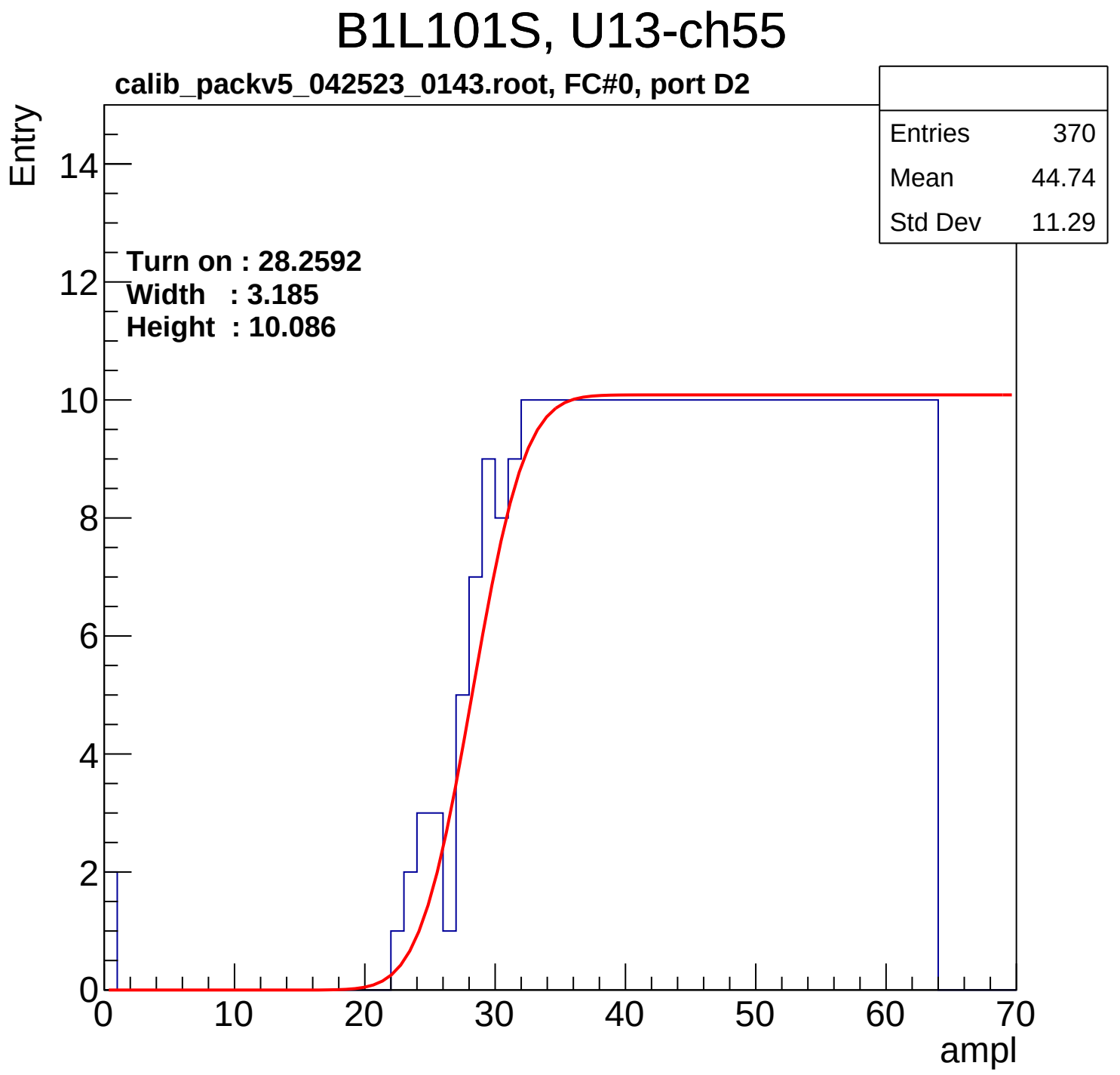
B1L101S, U13-ch55
calib_packv5_042523_0143.root, FC#0, port D2
Entries 370
Mean 44.74
Std Dev 11.29
Turn on : 28.2592
Width : 3.185
Height : 10.086
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ampl
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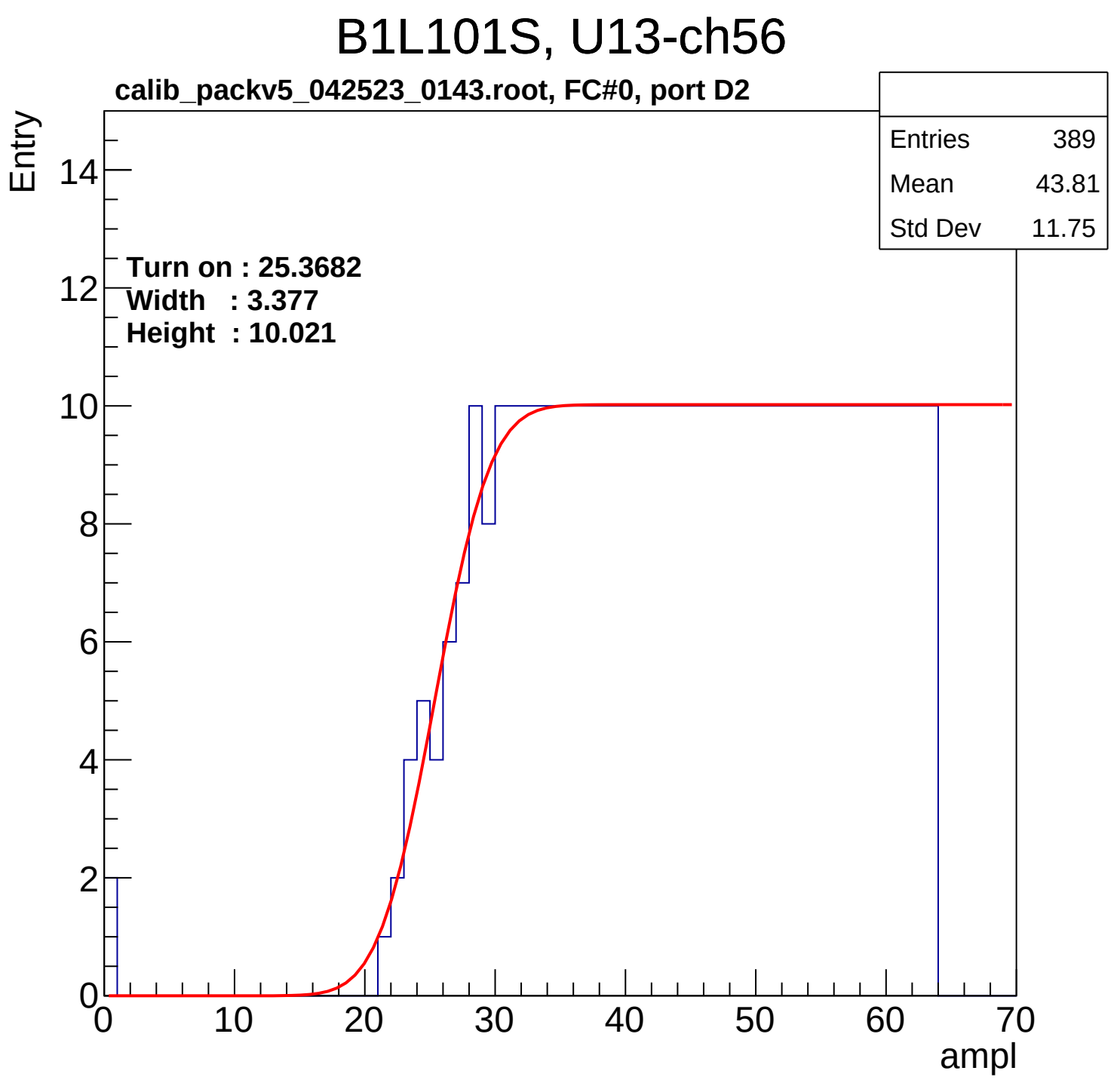
B1L101S, U13-ch56
calib_packv5_042523_0143.root, FC#0, port D2
Entries 389
Mean 43.81
Std Dev 11.75
Turn on : 25.3682
Width : 3.377
Height : 10.021
Entry
ampl
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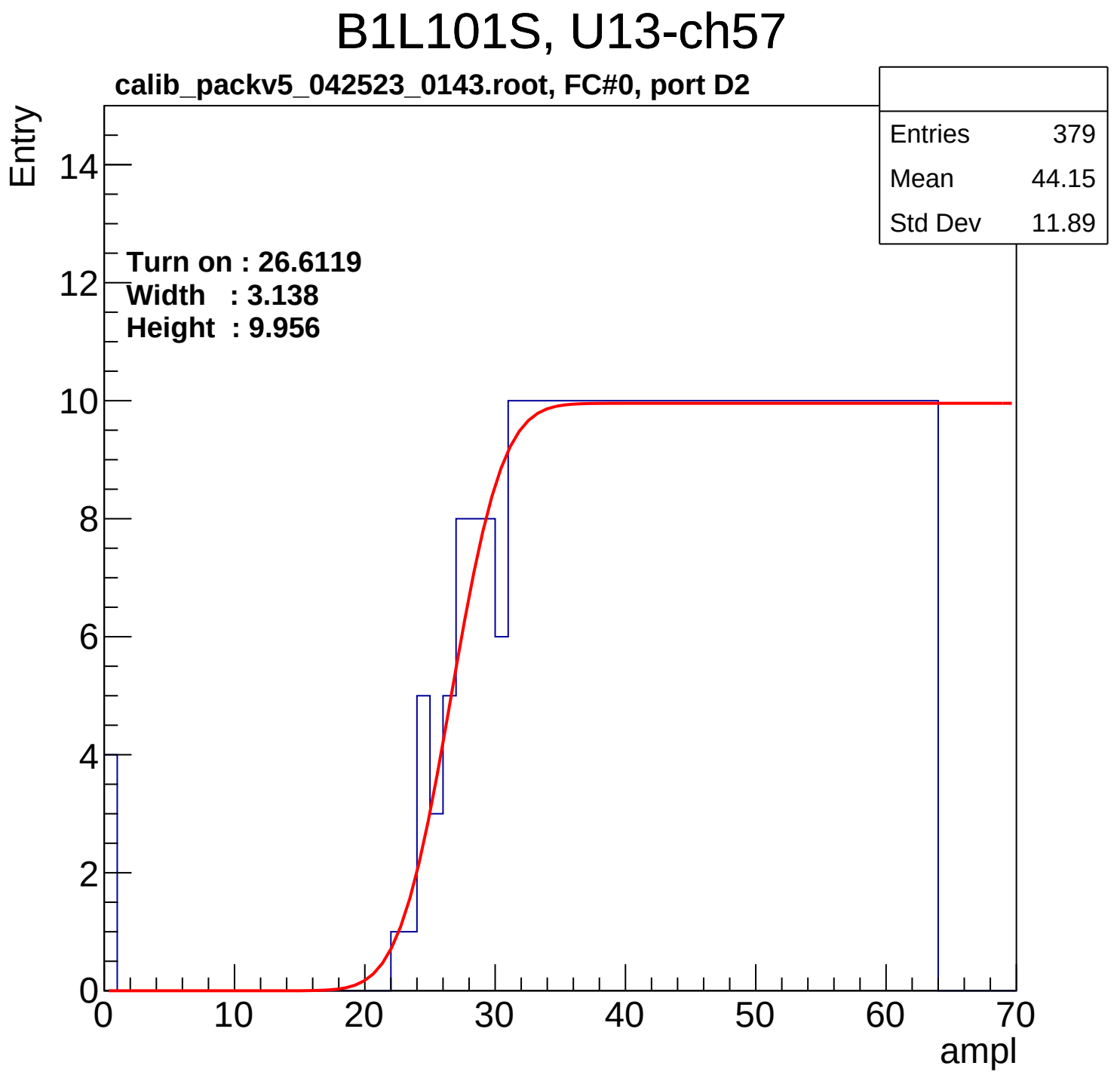
B1L101S, U13-ch57
calib_packv5_042523_0143.root, FC#0, port D2
Entries 379
Mean 44.15
Std Dev 11.89
Turn on : 26.6119
Width : 3.138
Height : 9.956
Entry
ampl
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4
6
8
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10
20
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50
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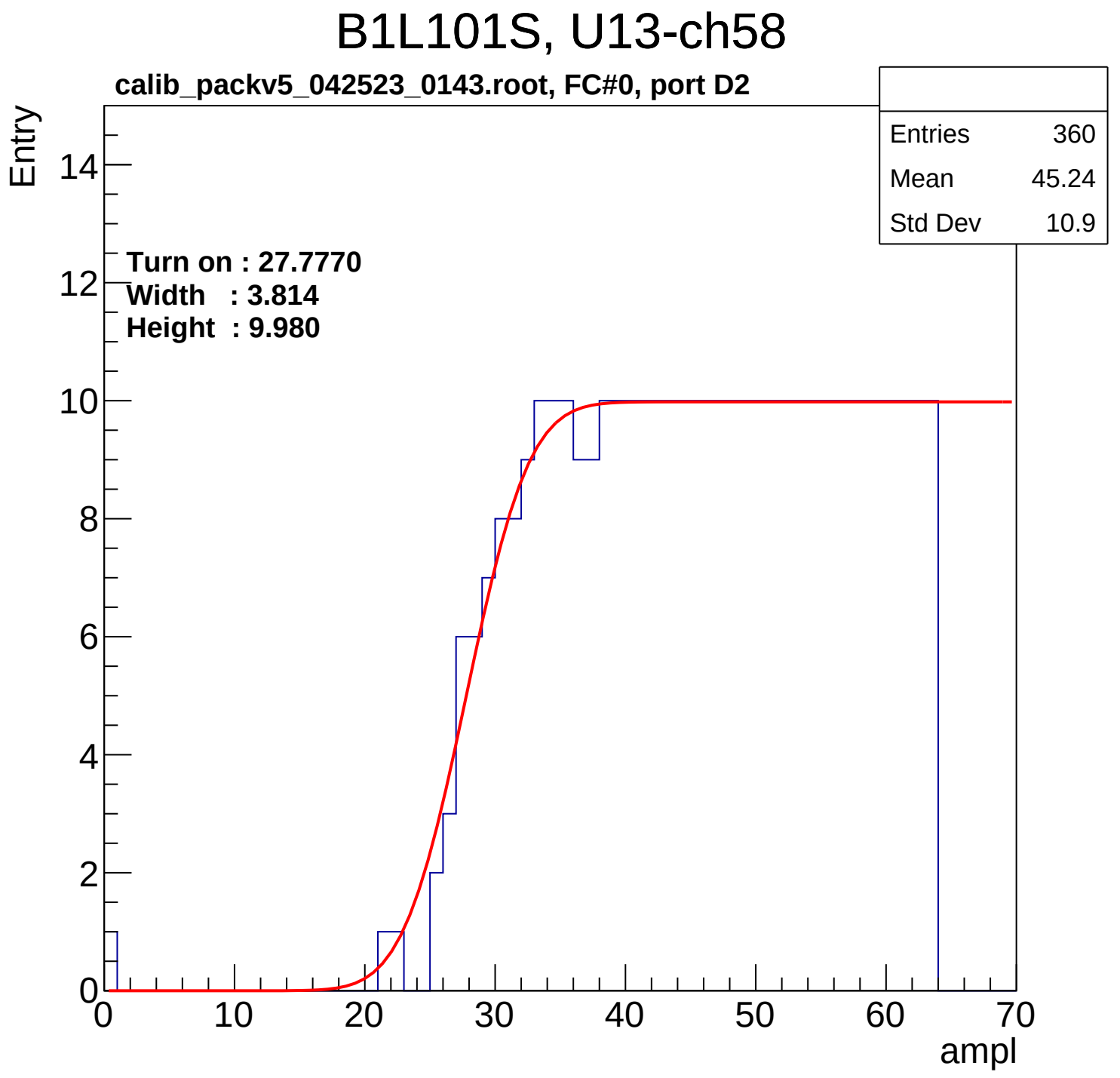
B1L101S, U13-ch58
calib_packv5_042523_0143.root, FC#0, port D2
Entries 360
Mean 45.24
Std Dev 10.9
Turn on : 27.7770
Width : 3.814
Height : 9.980
Entry
ampl
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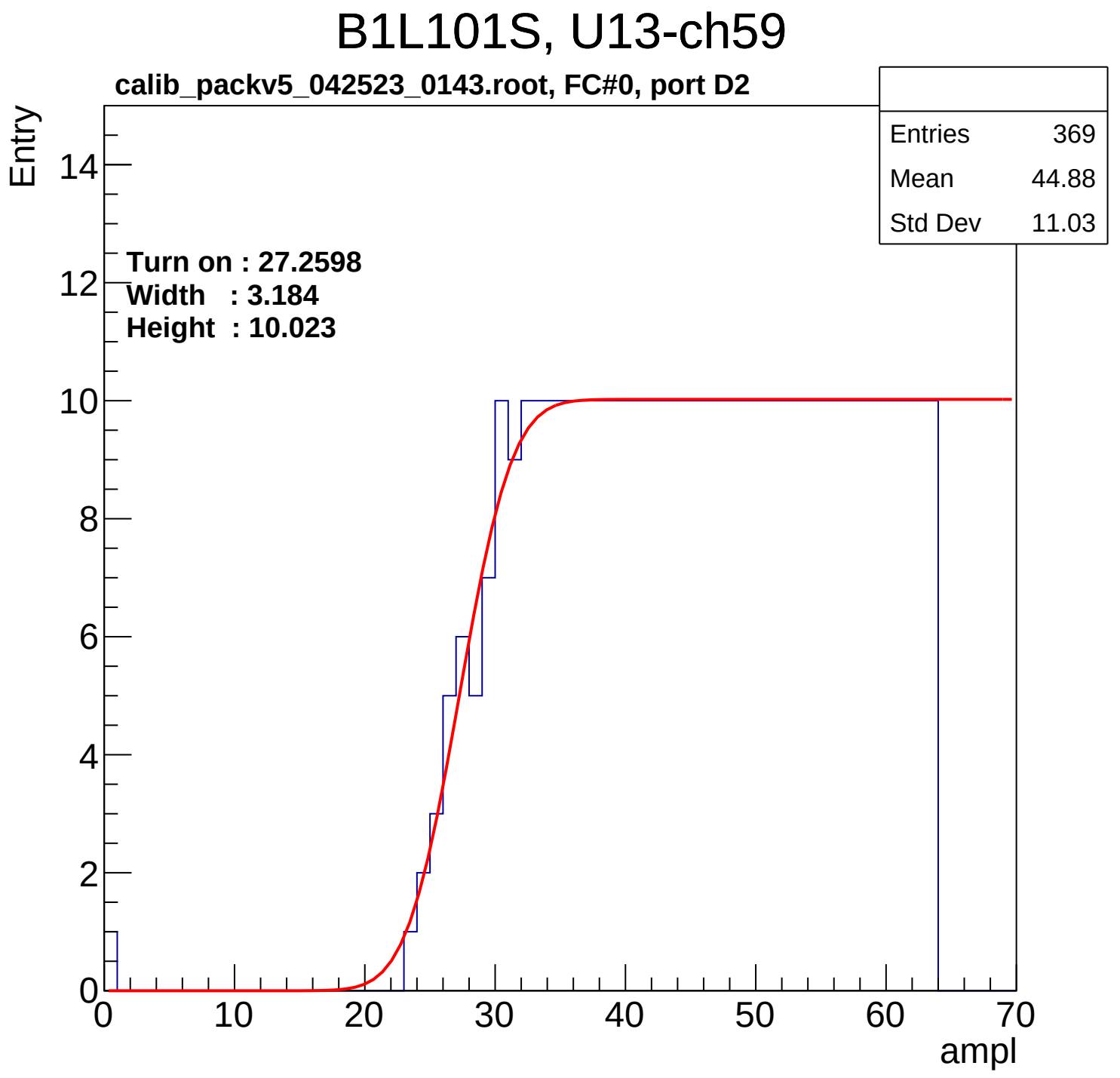
B1L101S, U13-ch59
calib_packv5_042523_0143.root, FC#0, port D2
Entries 369
Mean 44.88
Std Dev 11.03
Turn on : 27.2598
Width : 3.184
Height : 10.023
Entry
ampl
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2
4
6
8
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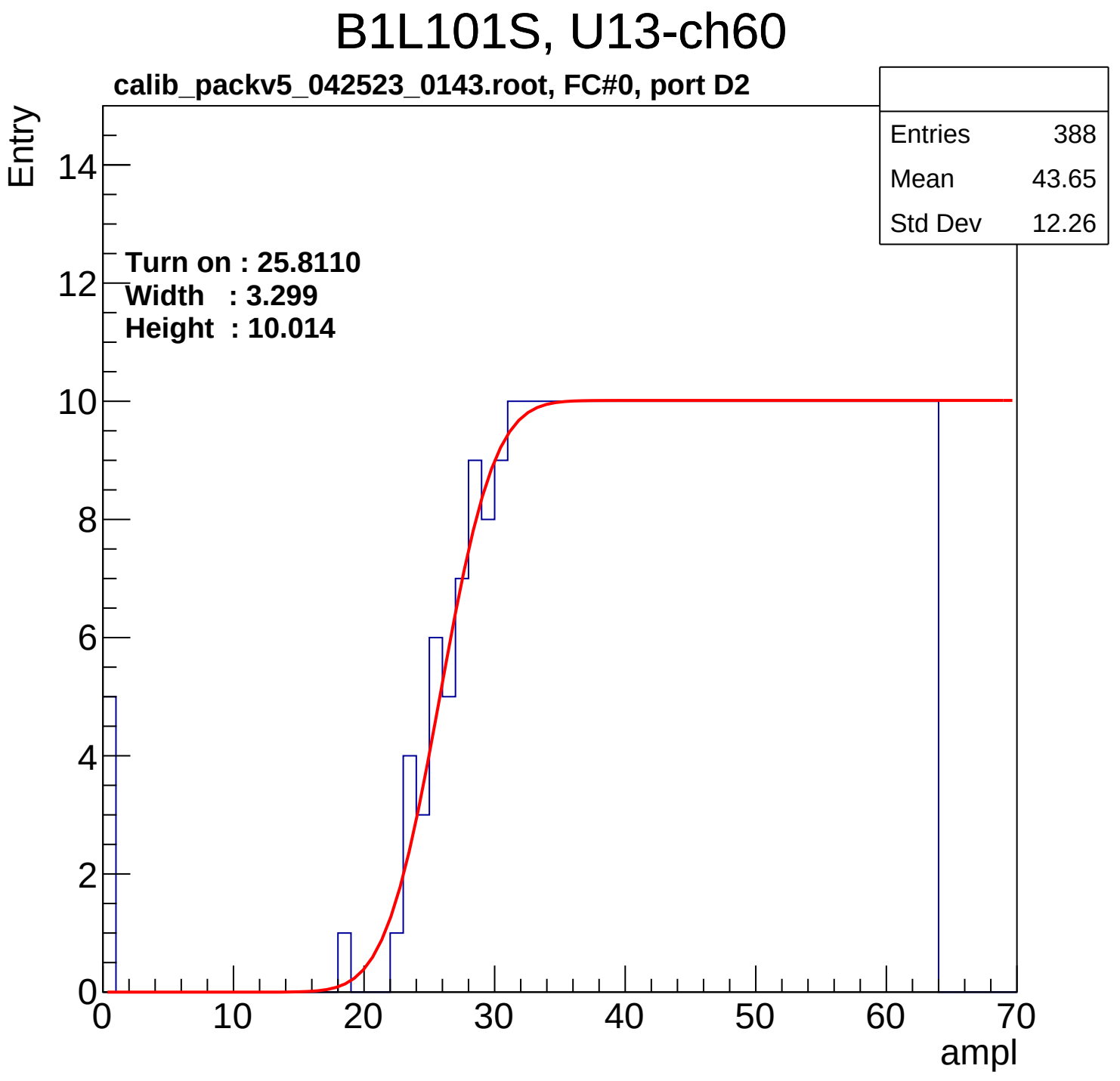
B1L101S, U13-ch60
calib_packv5_042523_0143.root, FC#0, port D2
Entries 388
Mean 43.65
Std Dev 12.26
Turn on : 25.8110
Width : 3.299
Height : 10.014
Entry
ampl
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2
4
6
8
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0
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60
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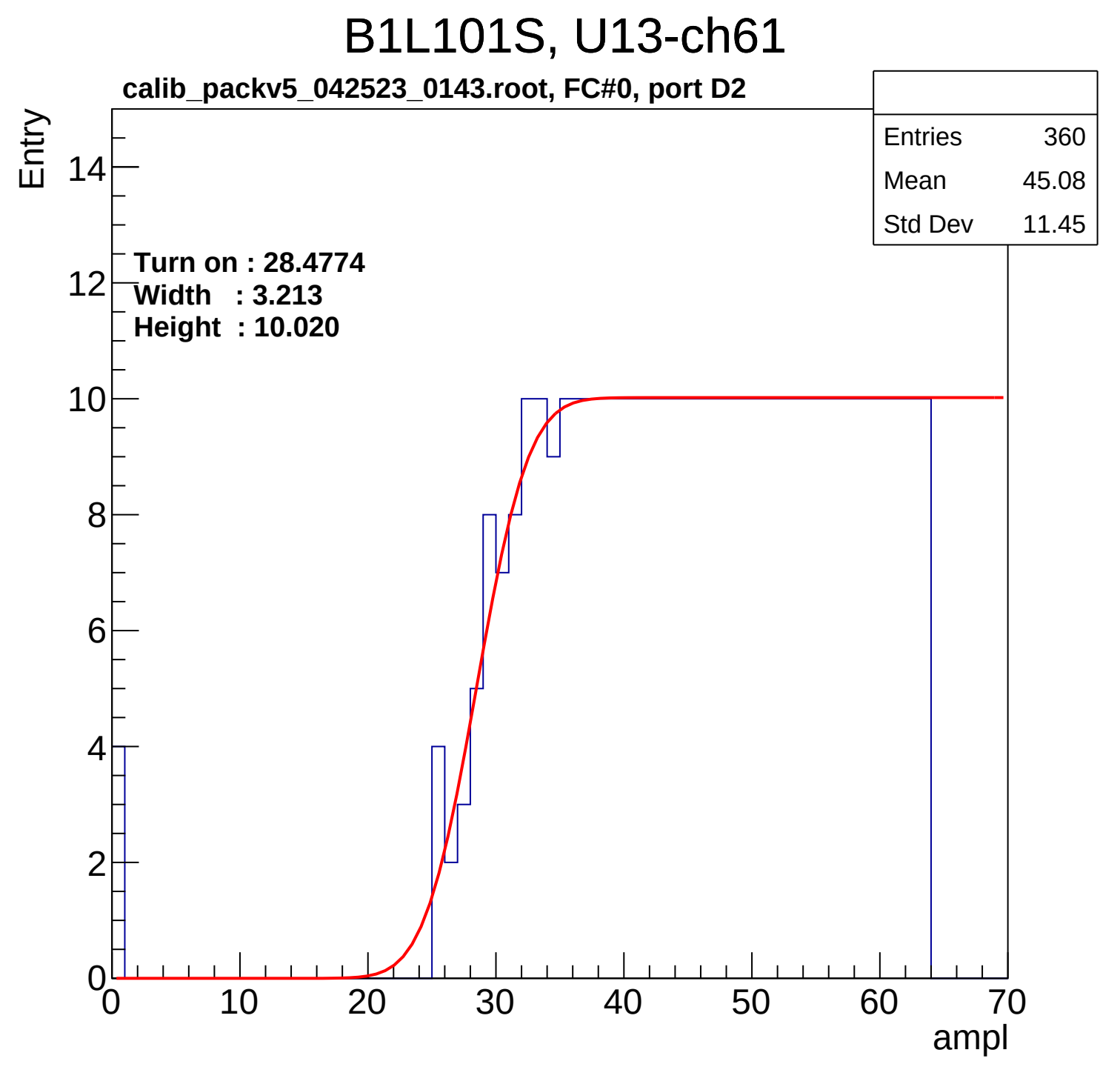
B1L101S, U13-ch61
calib_packv5_042523_0143.root, FC#0, port D2
Entries 360
Mean 45.08
Std Dev 11.45
Turn on : 28.4774
Width : 3.213
Height : 10.020
Entry
ampl
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4
6
8
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0
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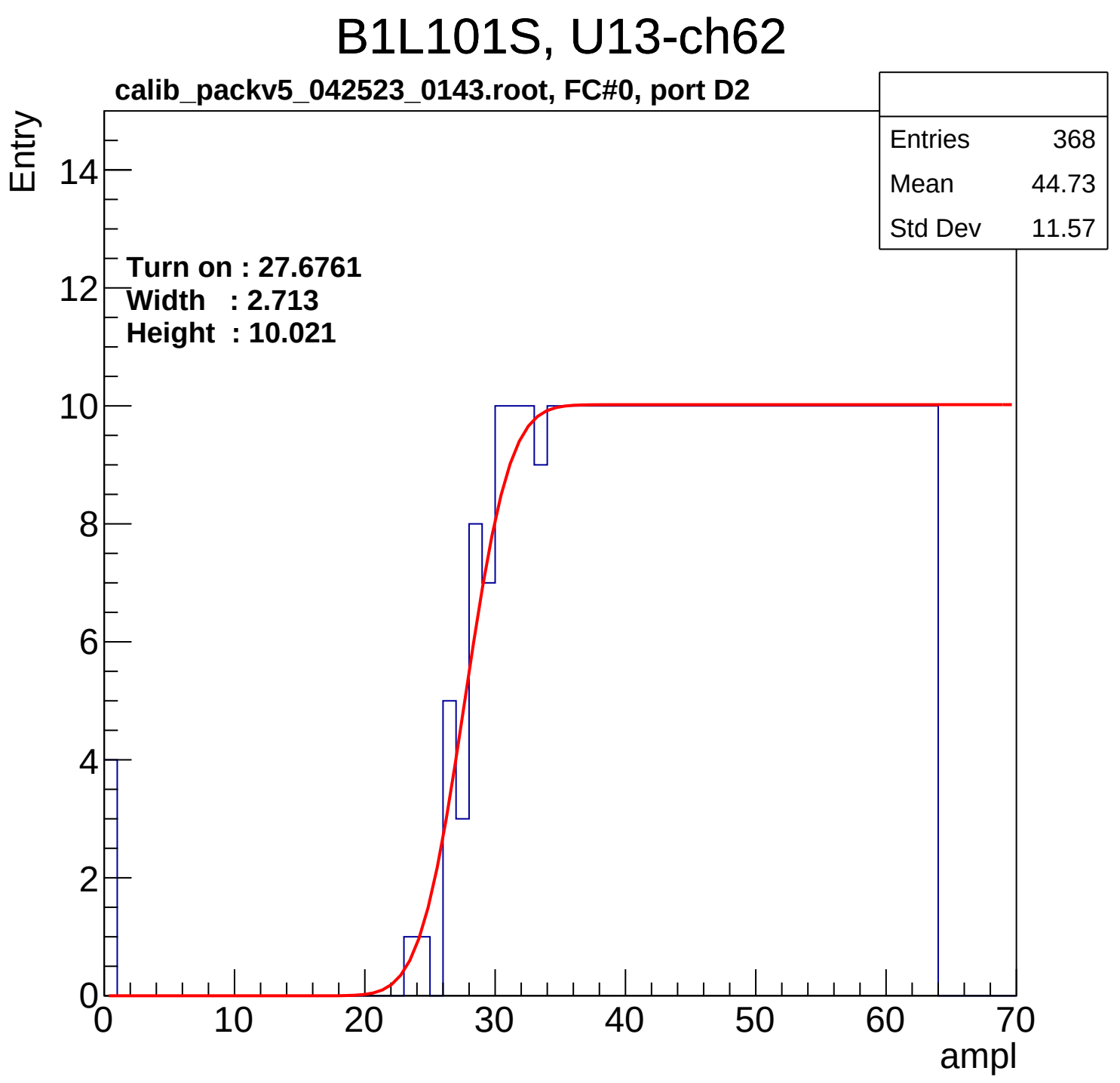
B1L101S, U13-ch62
calib_packv5_042523_0143.root, FC#0, port D2
Entries 368
Mean 44.73
Std Dev 11.57
Turn on : 27.6761
Width : 2.713
Height : 10.021
Entry
ampl
0
2
4
6
8
10
12
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0
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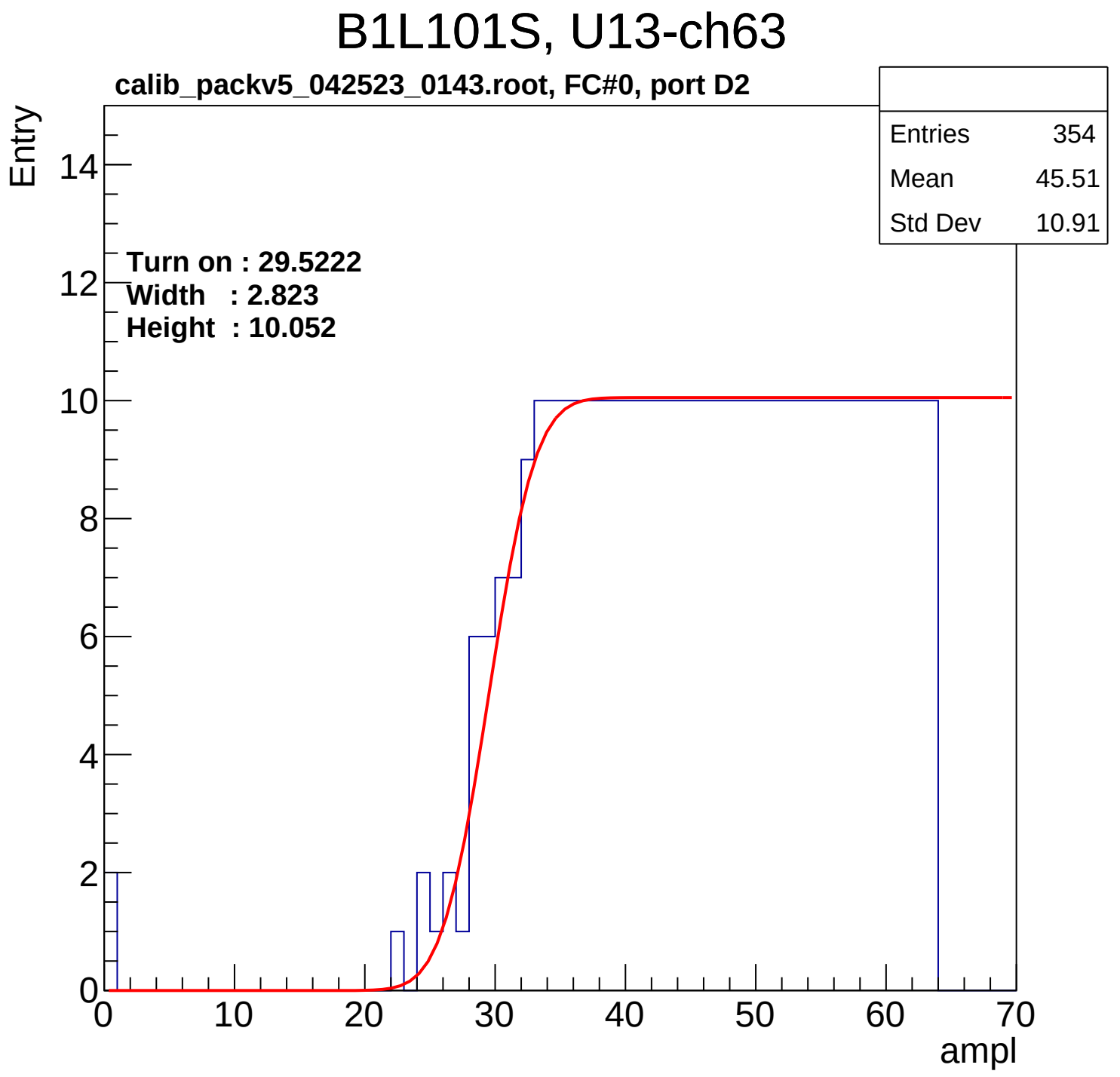
B1L101S, U13-ch63
calib_packv5_042523_0143.root, FC#0, port D2
Entries 354
Mean 45.51
Std Dev 10.91
Turn on : 29.5222
Width : 2.823
Height : 10.052
Entry
ampl
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2
4
6
8
10
12
14
0
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20
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60
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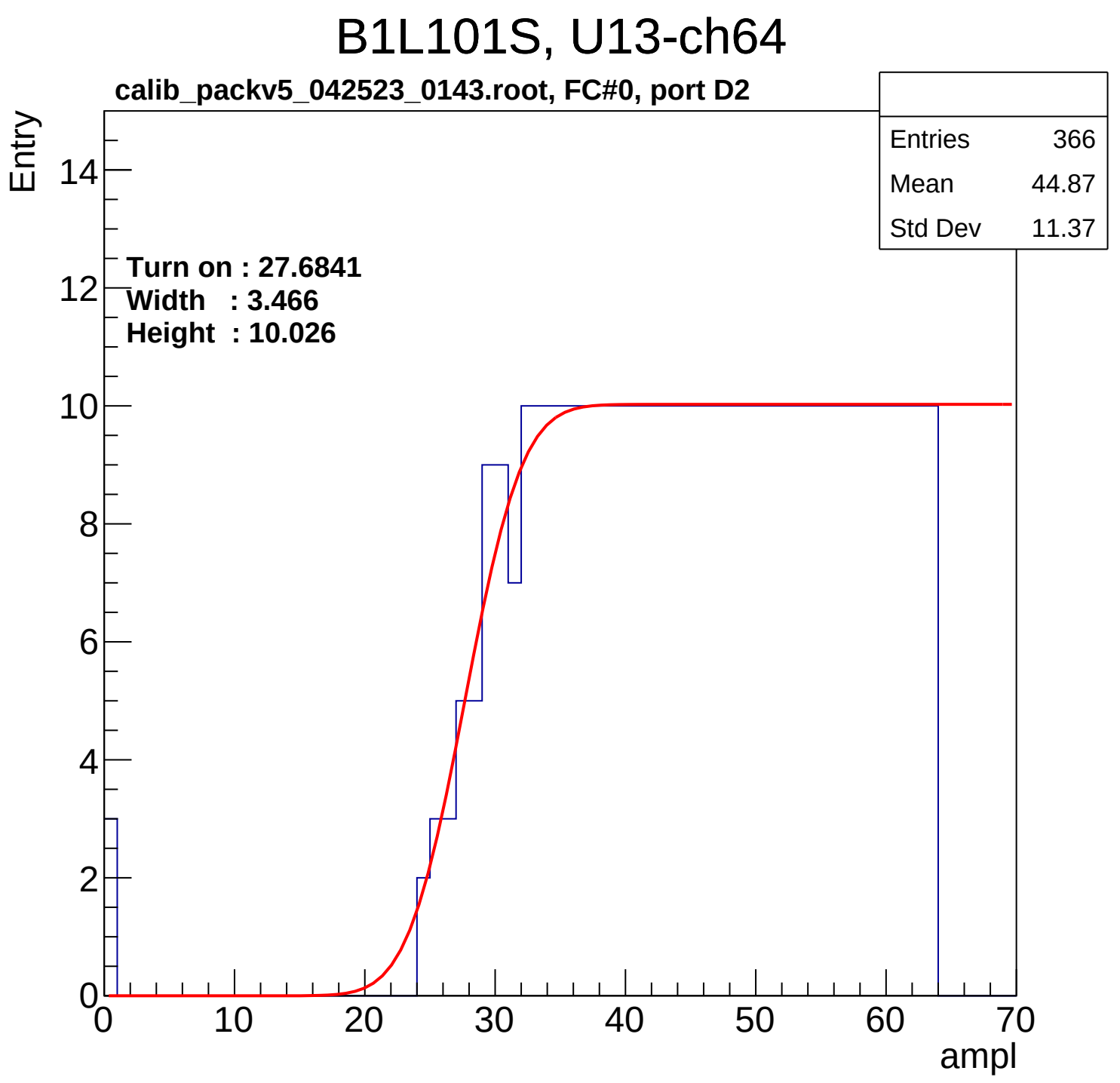
B1L101S, U13-ch64
calib_packv5_042523_0143.root, FC#0, port D2
Entries 366
Mean 44.87
Std Dev 11.37
Turn on : 27.6841
Width : 3.466
Height : 10.026
Entry
ampl
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2
4
6
8
10
12
14
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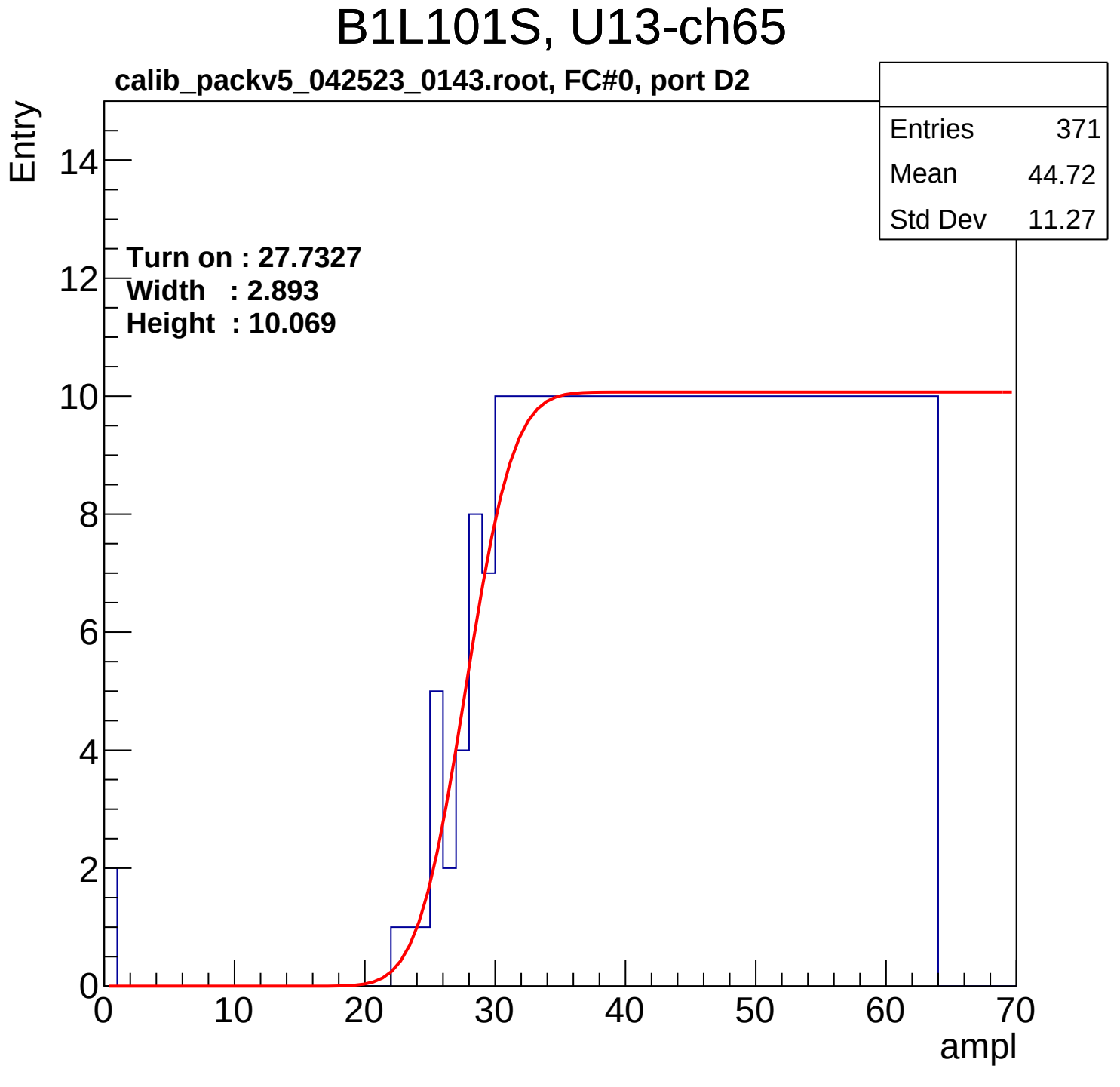
B1L101S, U13-ch65
calib_packv5_042523_0143.root, FC#0, port D2
Entries 371
Mean 44.72
Std Dev 11.27
Turn on : 27.7327
Width : 2.893
Height : 10.069
Entry
ampl
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2
4
6
8
10
12
14
0
10
20
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40
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60
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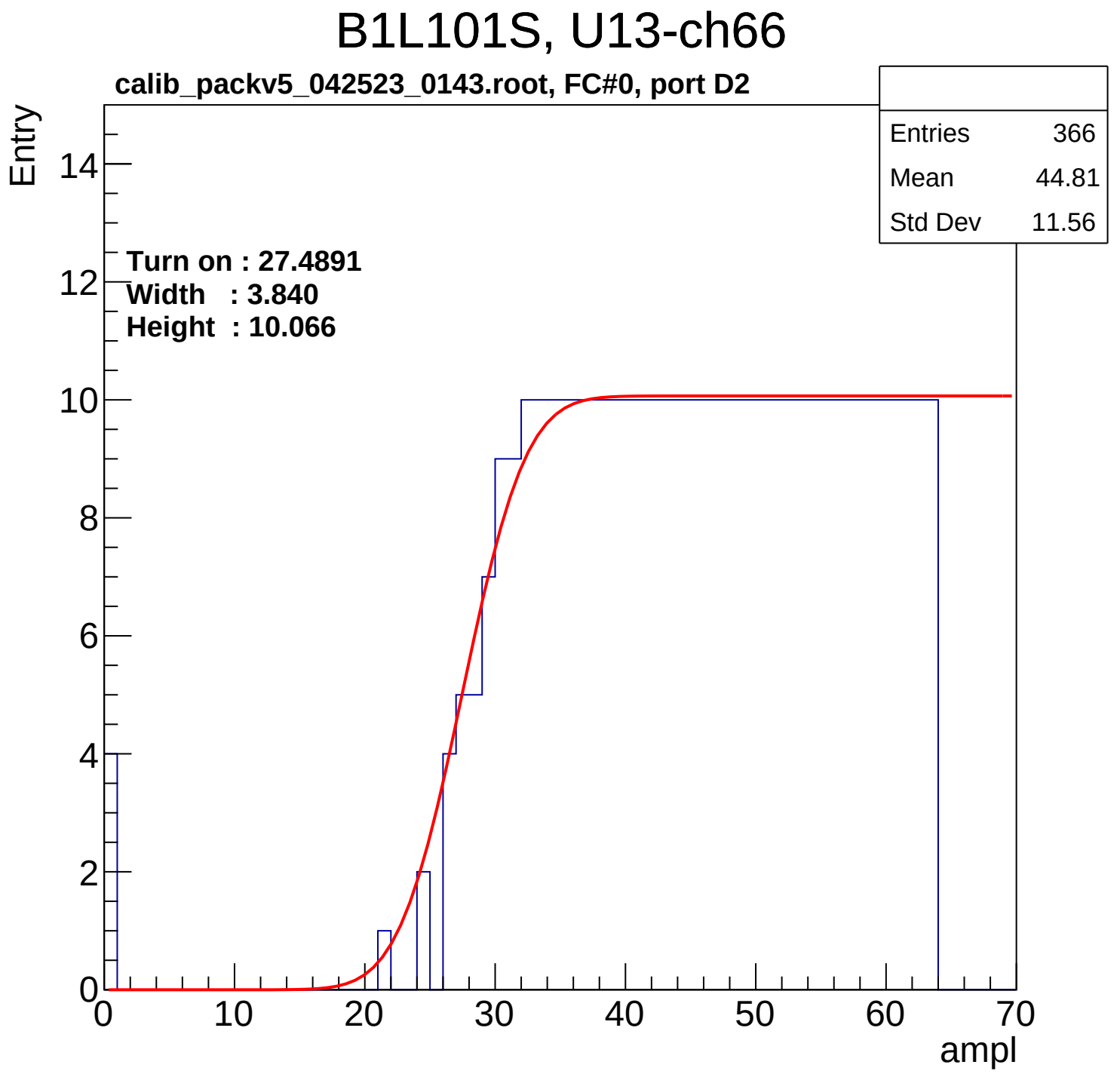
B1L101S, U13-ch66
calib_packv5_042523_0143.root, FC#0, port D2
Entries 366
Mean 44.81
Std Dev 11.56
Turn on : 27.4891
Width : 3.840
Height : 10.066
Entry
ampl
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4
6
8
10
12
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0
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60
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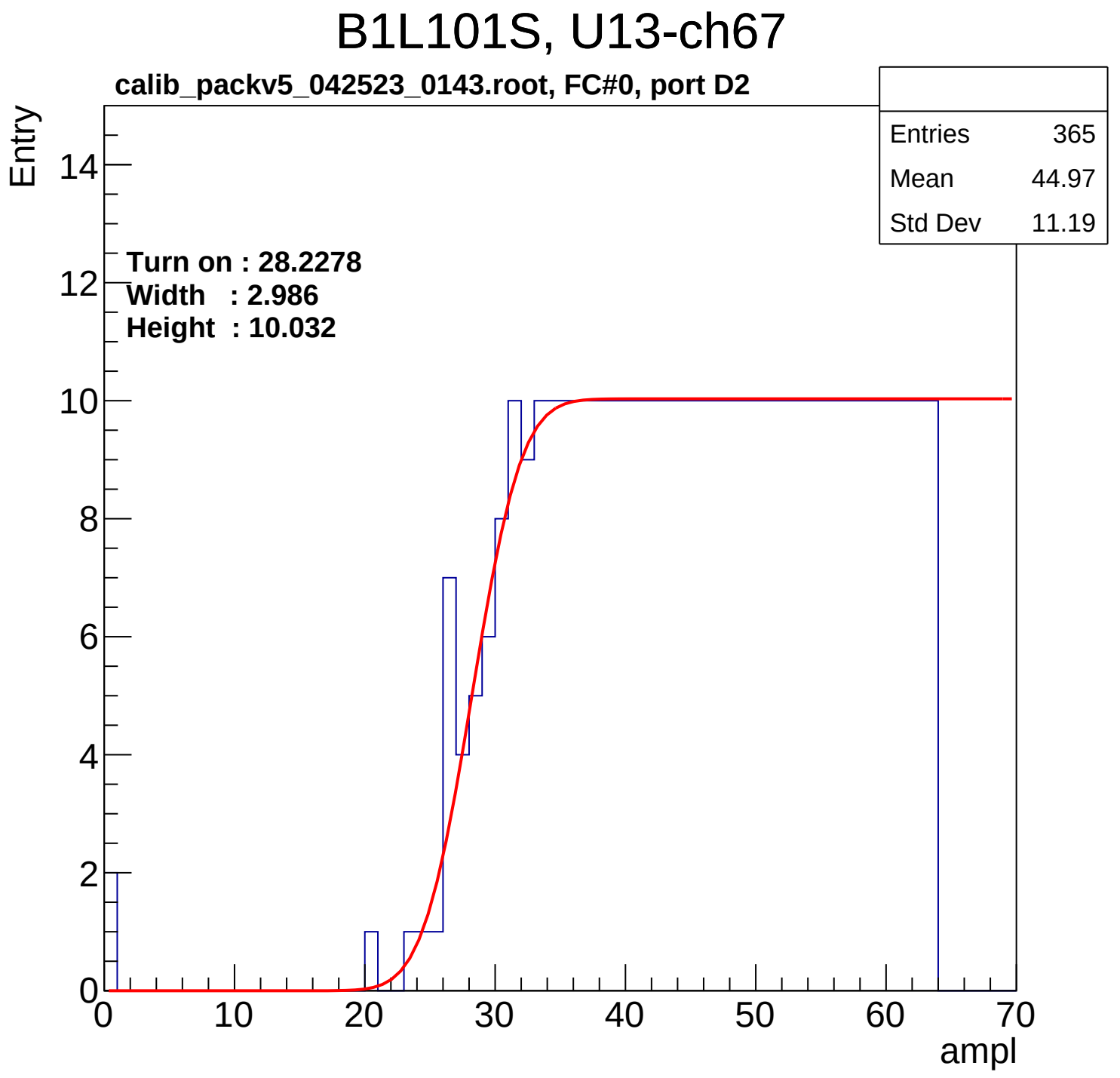
B1L101S, U13-ch67
calib_packv5_042523_0143.root, FC#0, port D2
Entries 365
Mean 44.97
Std Dev 11.19
Turn on : 28.2278
Width : 2.986
Height : 10.032
Entry
ampl
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2
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6
8
10
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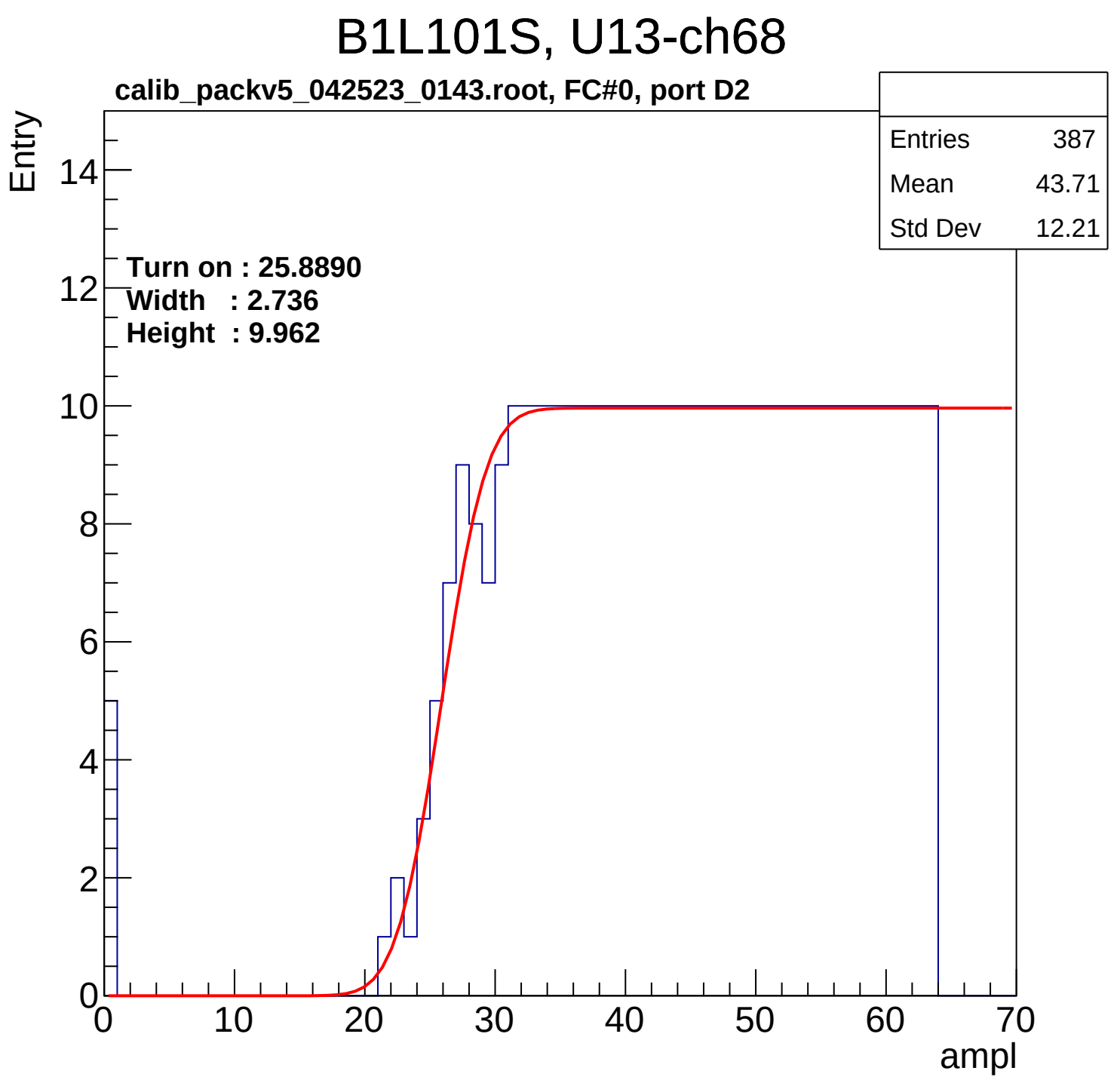
B1L101S, U13-ch68
calib_packv5_042523_0143.root, FC#0, port D2
Entries 387
Mean 43.71
Std Dev 12.21
Turn on : 25.8890
Width : 2.736
Height : 9.962
Entry
ampl
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2
4
6
8
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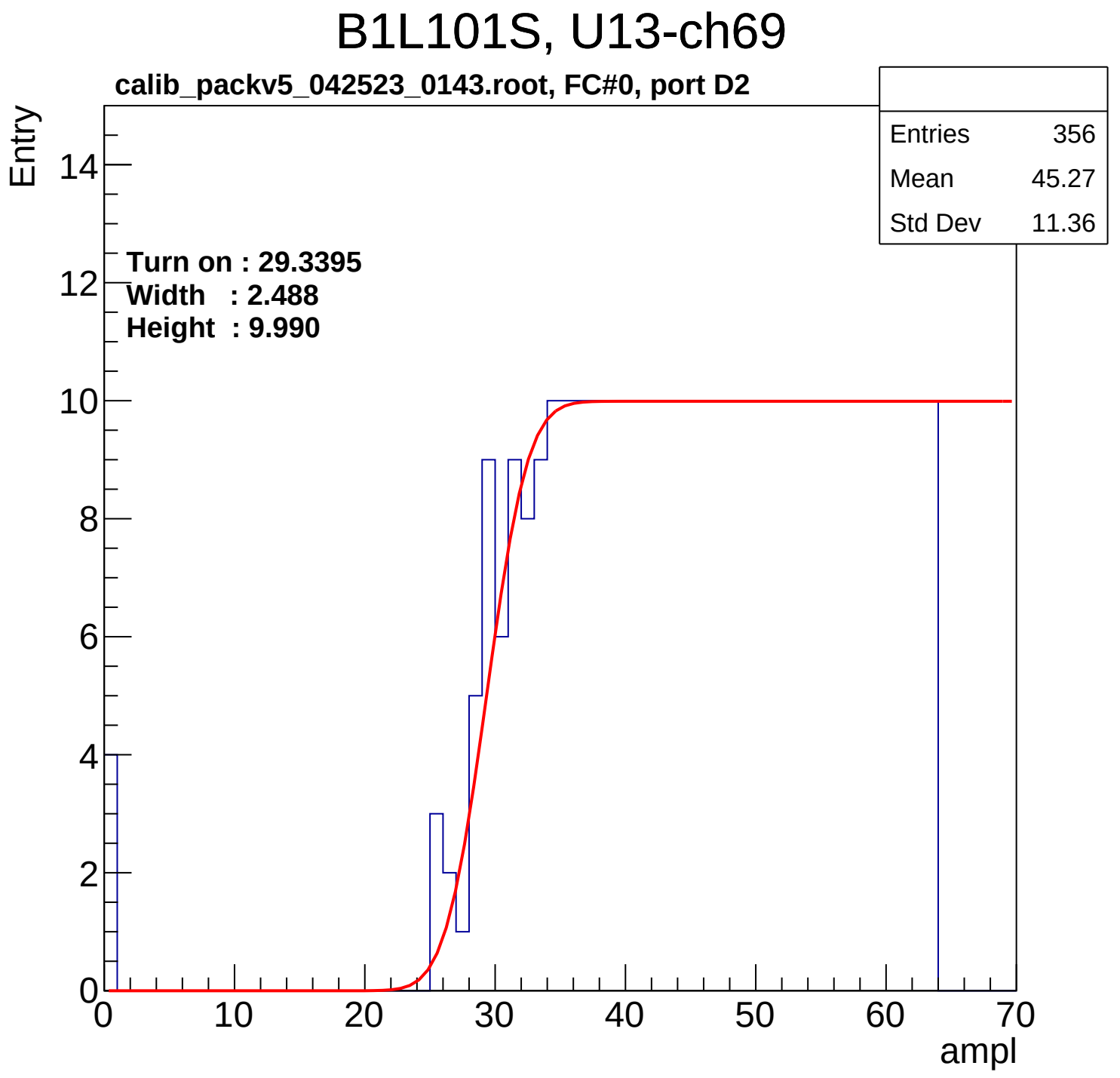
B1L101S, U13-ch69
calib_packv5_042523_0143.root, FC#0, port D2
Entries 356
Mean 45.27
Std Dev 11.36
Turn on : 29.3395
Width : 2.488
Height : 9.990
Entry
ampl
0
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4
6
8
10
12
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60
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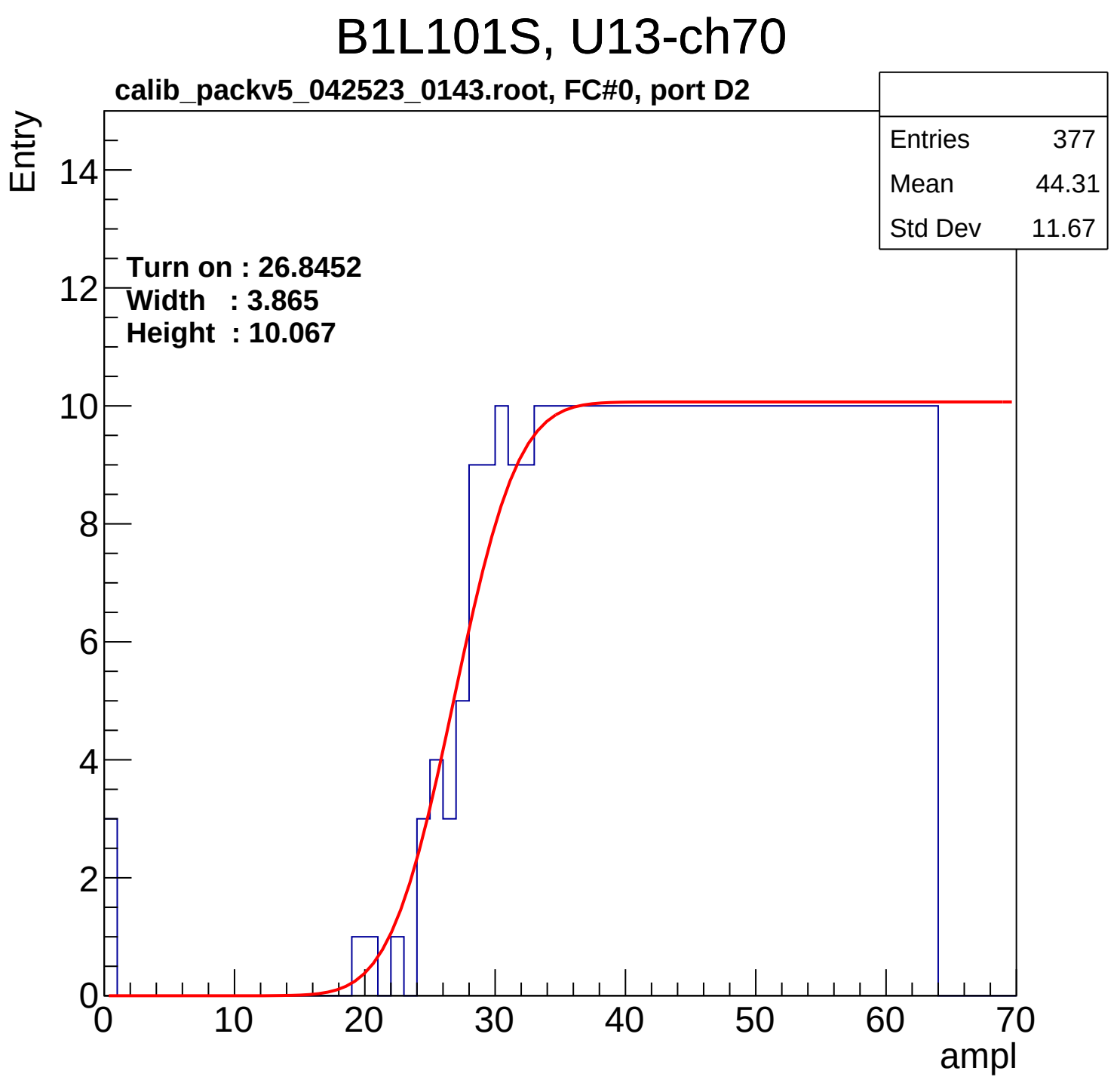
B1L101S, U13-ch70
calib_packv5_042523_0143.root, FC#0, port D2
Entries 377
Mean 44.31
Std Dev 11.67
Turn on : 26.8452
Width : 3.865
Height : 10.067
Entry
ampl
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4
6
8
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12
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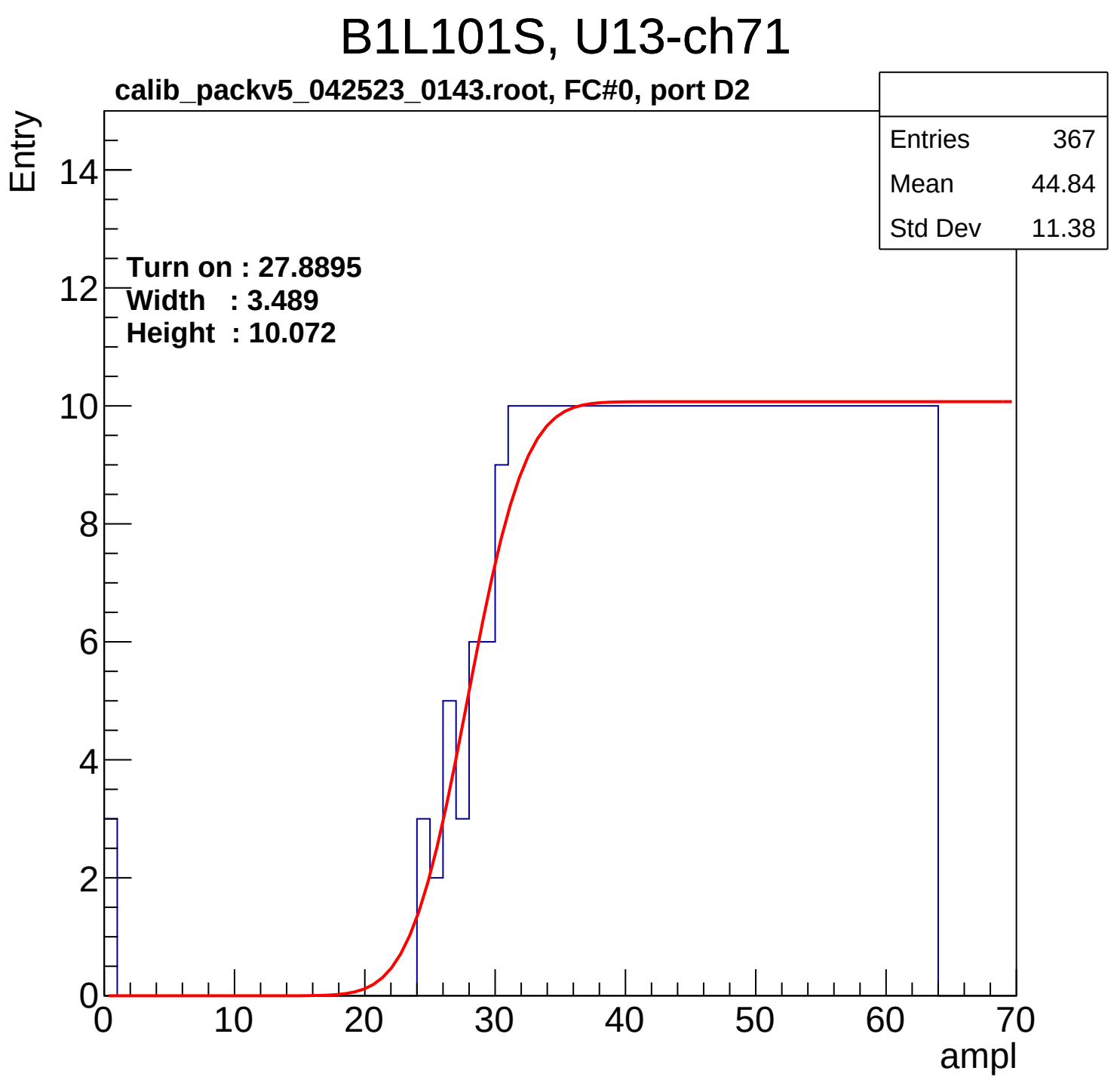
B1L101S, U13-ch71
calib_packv5_042523_0143.root, FC#0, port D2
Entries 367
Mean 44.84
Std Dev 11.38
Turn on : 27.8895
Width : 3.489
Height : 10.072
Entry
ampl
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6
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10
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0
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60
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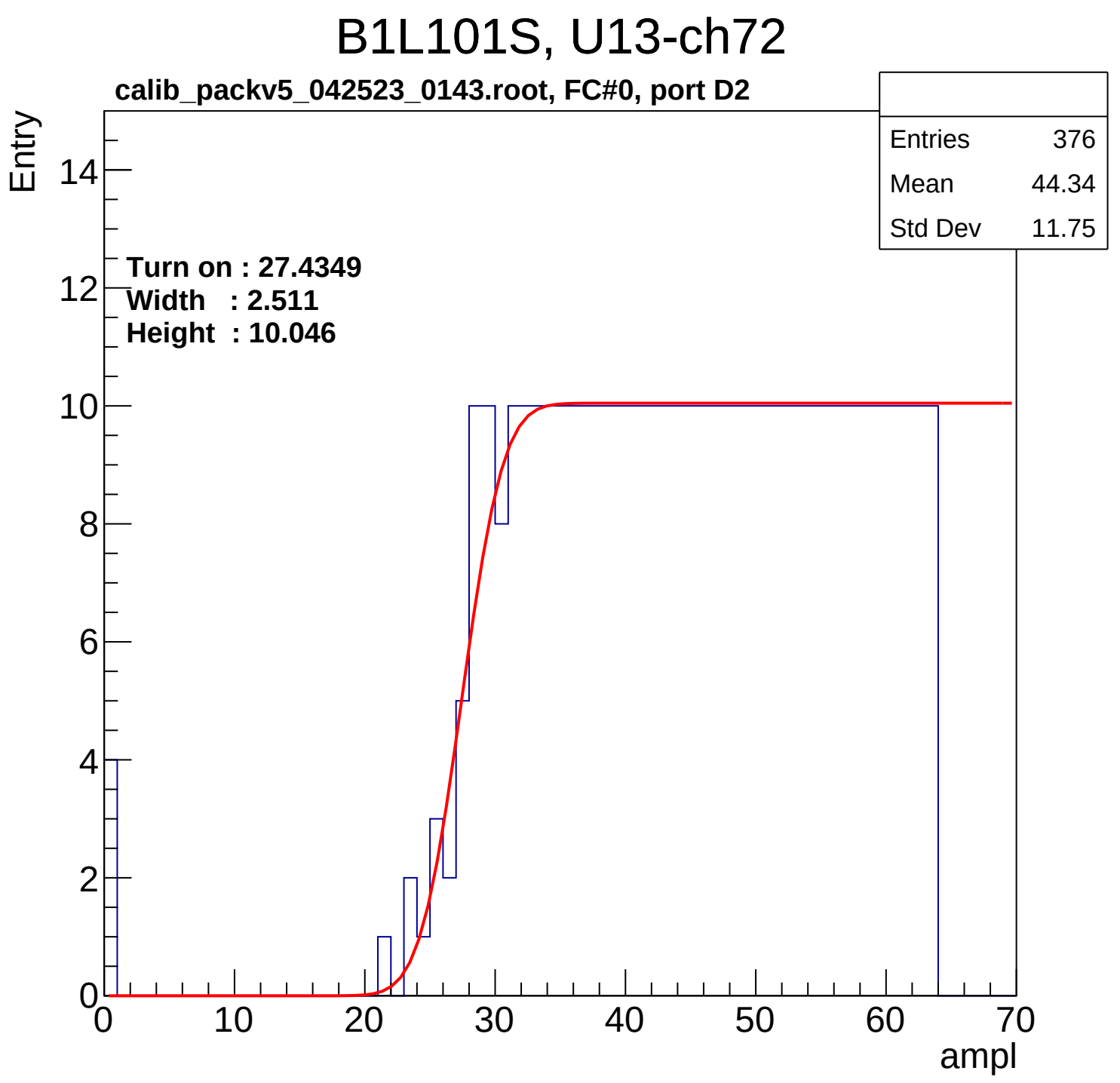
B1L101S, U13-ch72
calib_packv5_042523_0143.root, FC#0, port D2
Entries 376
Mean 44.34
Std Dev 11.75
Turn on : 27.4349
Width : 2.511
Height : 10.046
Entry
ampl
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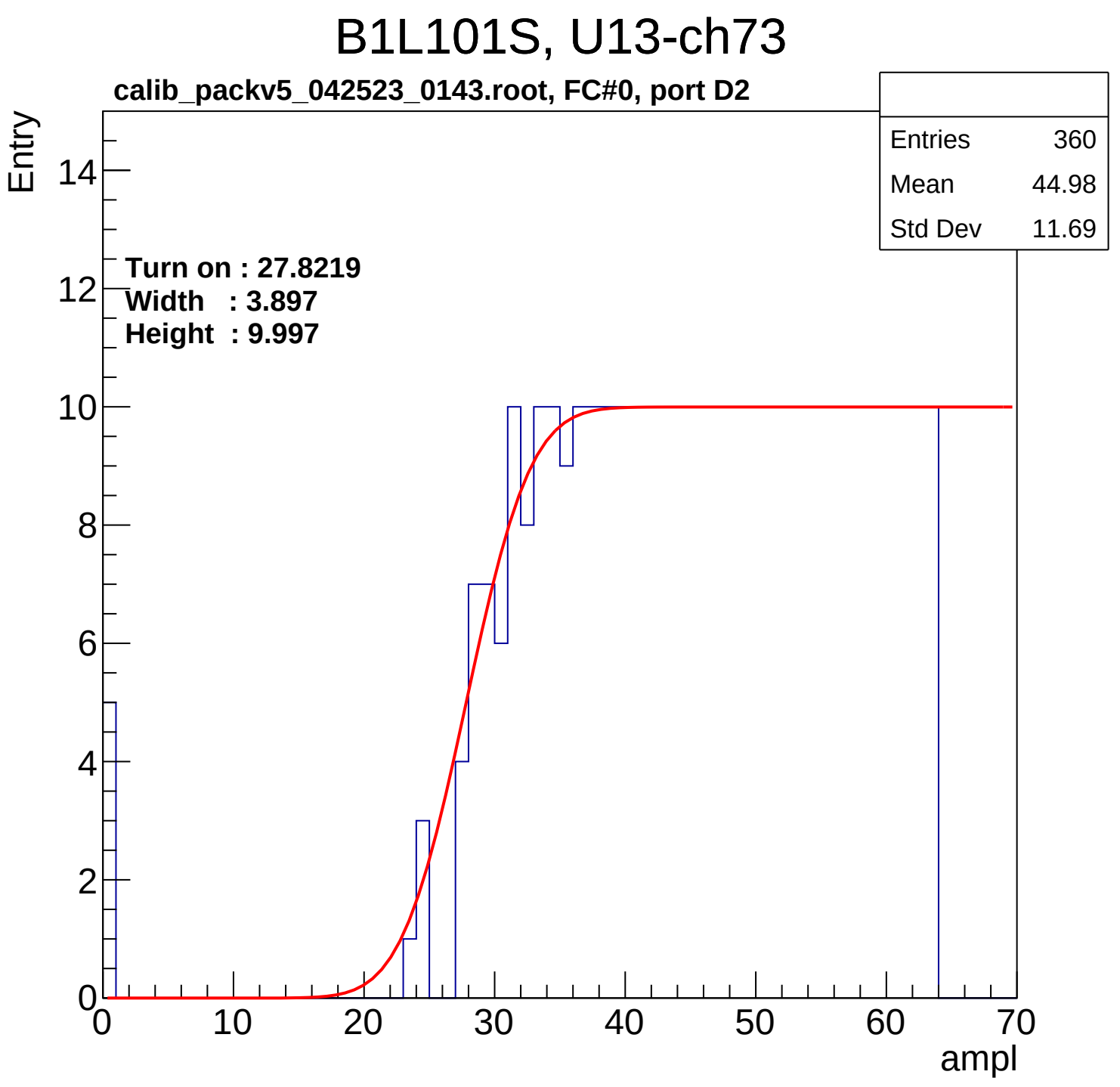
B1L101S, U13-ch73
calib_packv5_042523_0143.root, FC#0, port D2
Entries 360
Mean 44.98
Std Dev 11.69
Turn on : 27.8219
Width : 3.897
Height : 9.997
Entry
ampl
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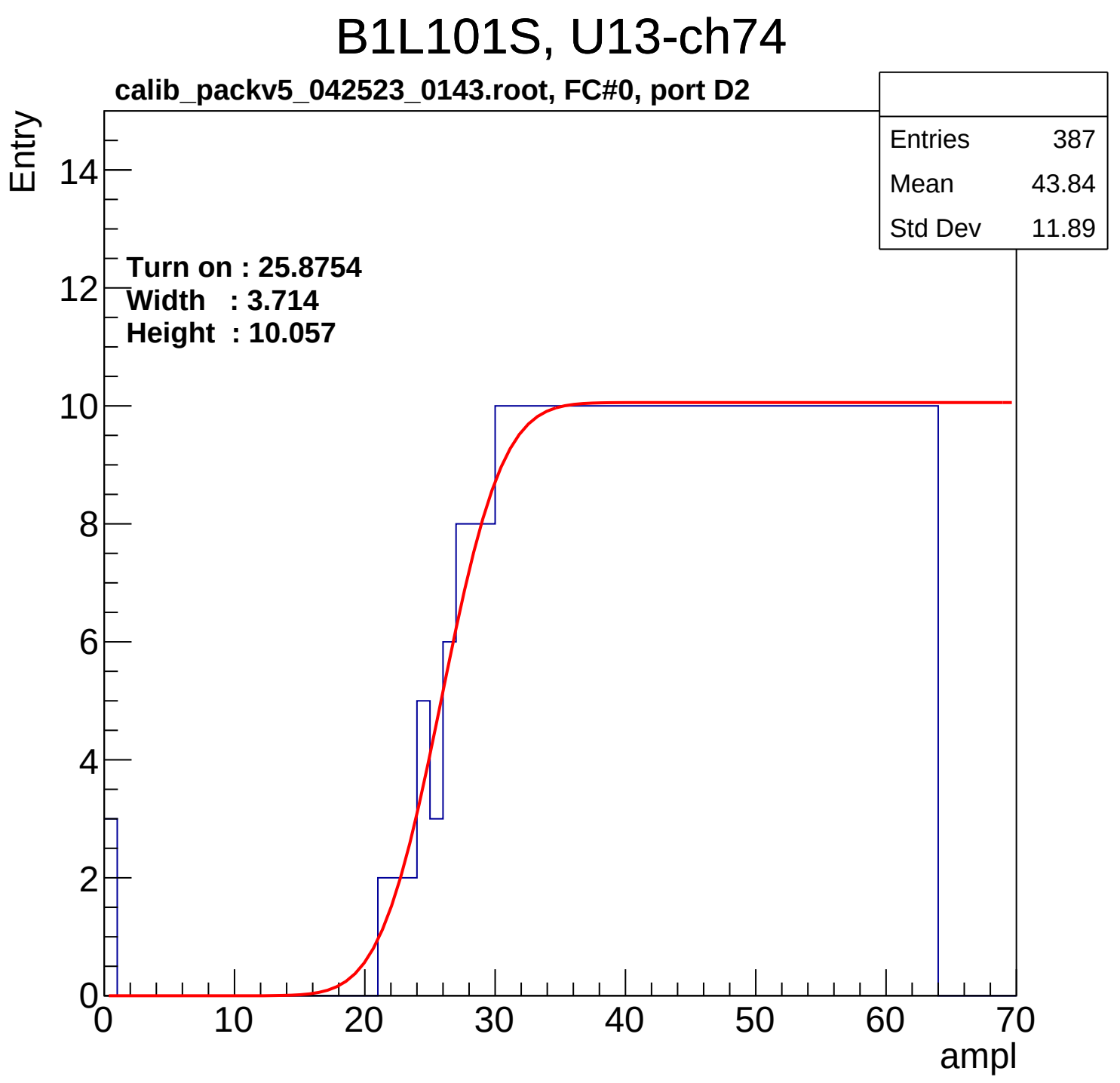
B1L101S, U13-ch74
calib_packv5_042523_0143.root, FC#0, port D2
Entries 387
Mean 43.84
Std Dev 11.89
Turn on : 25.8754
Width : 3.714
Height : 10.057
Entry
ampl
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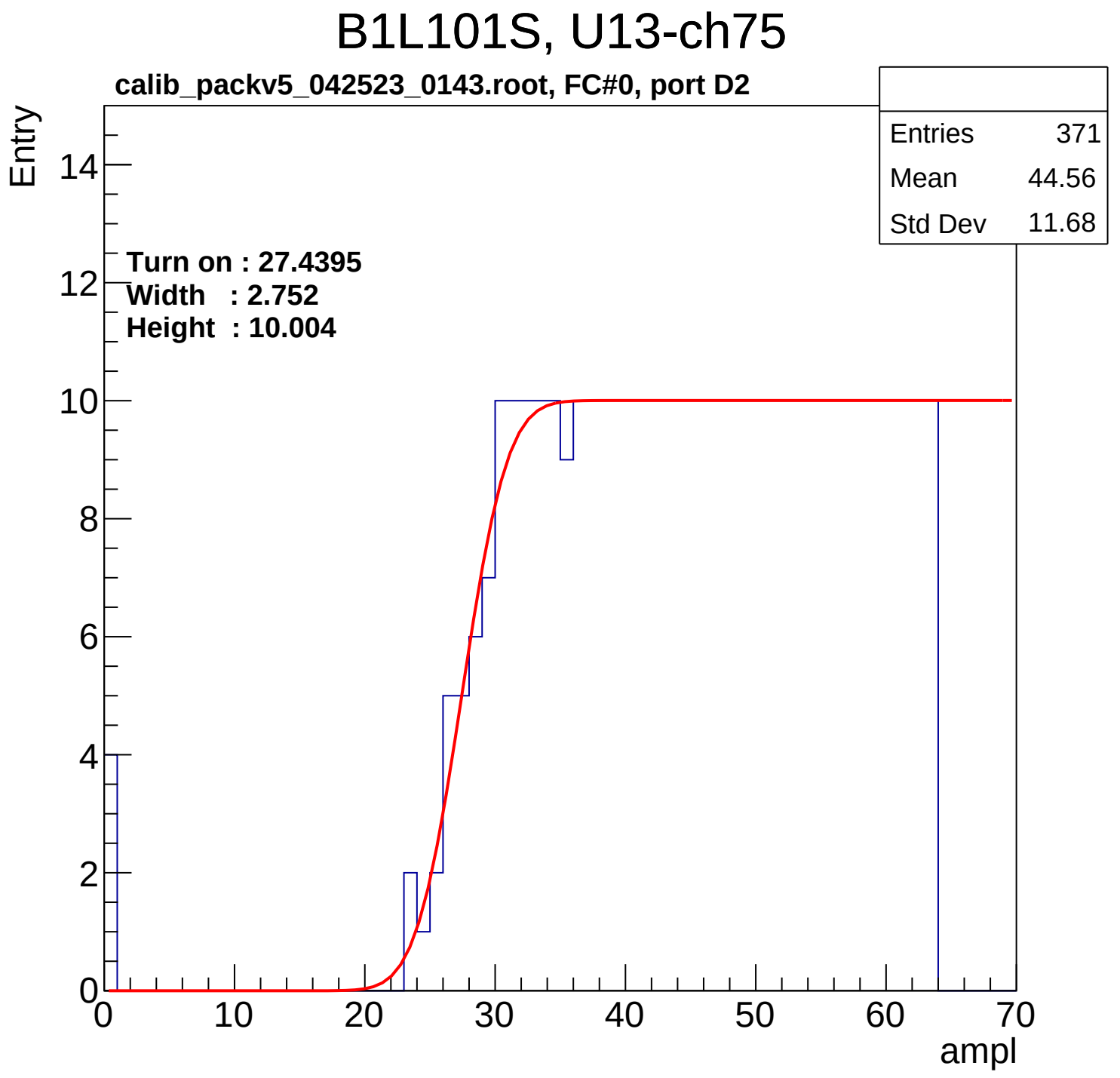
B1L101S, U13-ch75
calib_packv5_042523_0143.root, FC#0, port D2
Entries 371
Mean 44.56
Std Dev 11.68
Turn on : 27.4395
Width : 2.752
Height : 10.004
Entry
ampl
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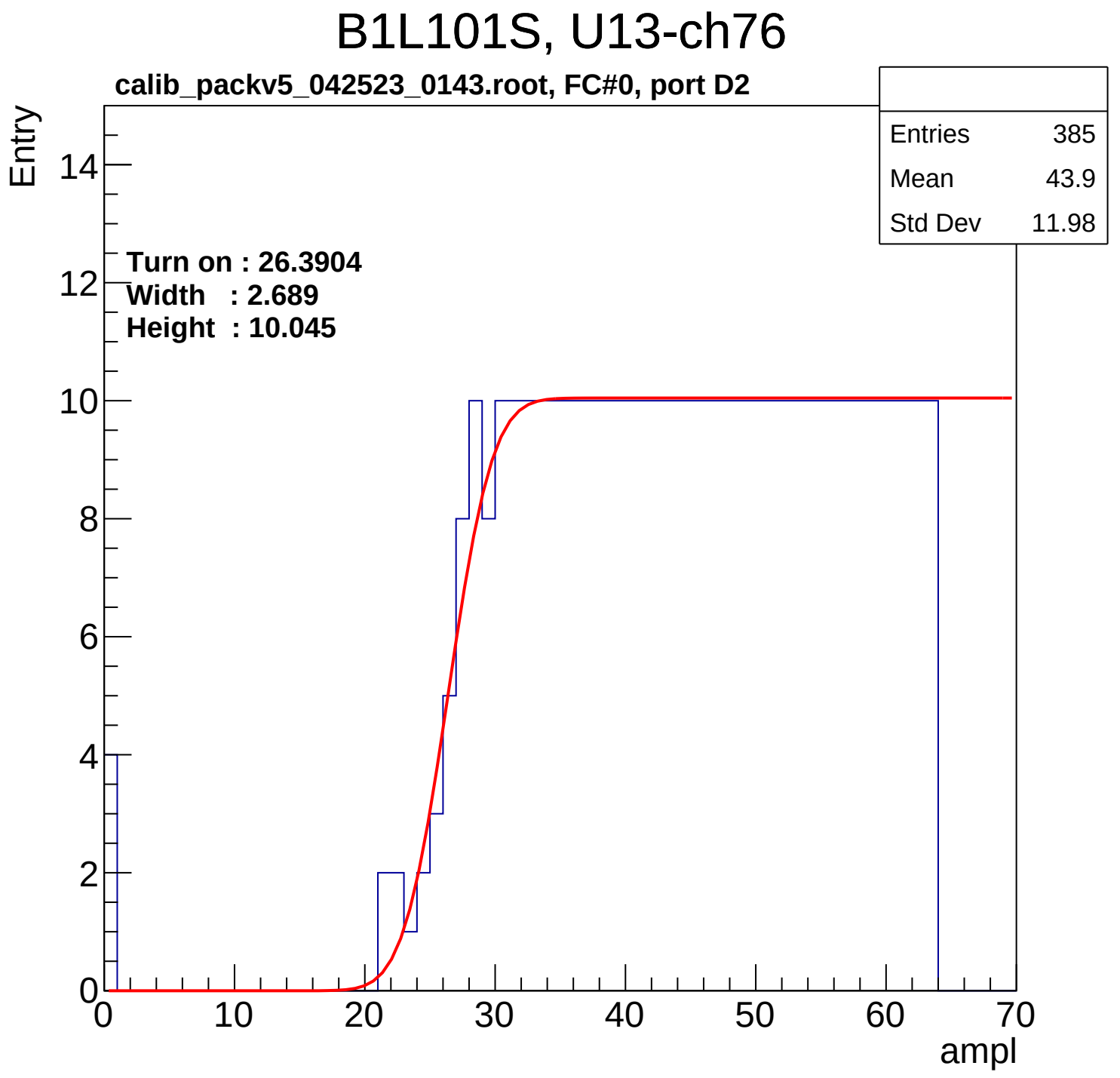
B1L101S, U13-ch76
calib_packv5_042523_0143.root, FC#0, port D2
Entries 385
Mean 43.9
Std Dev 11.98
Turn on : 26.3904
Width : 2.689
Height : 10.045
Entry
ampl
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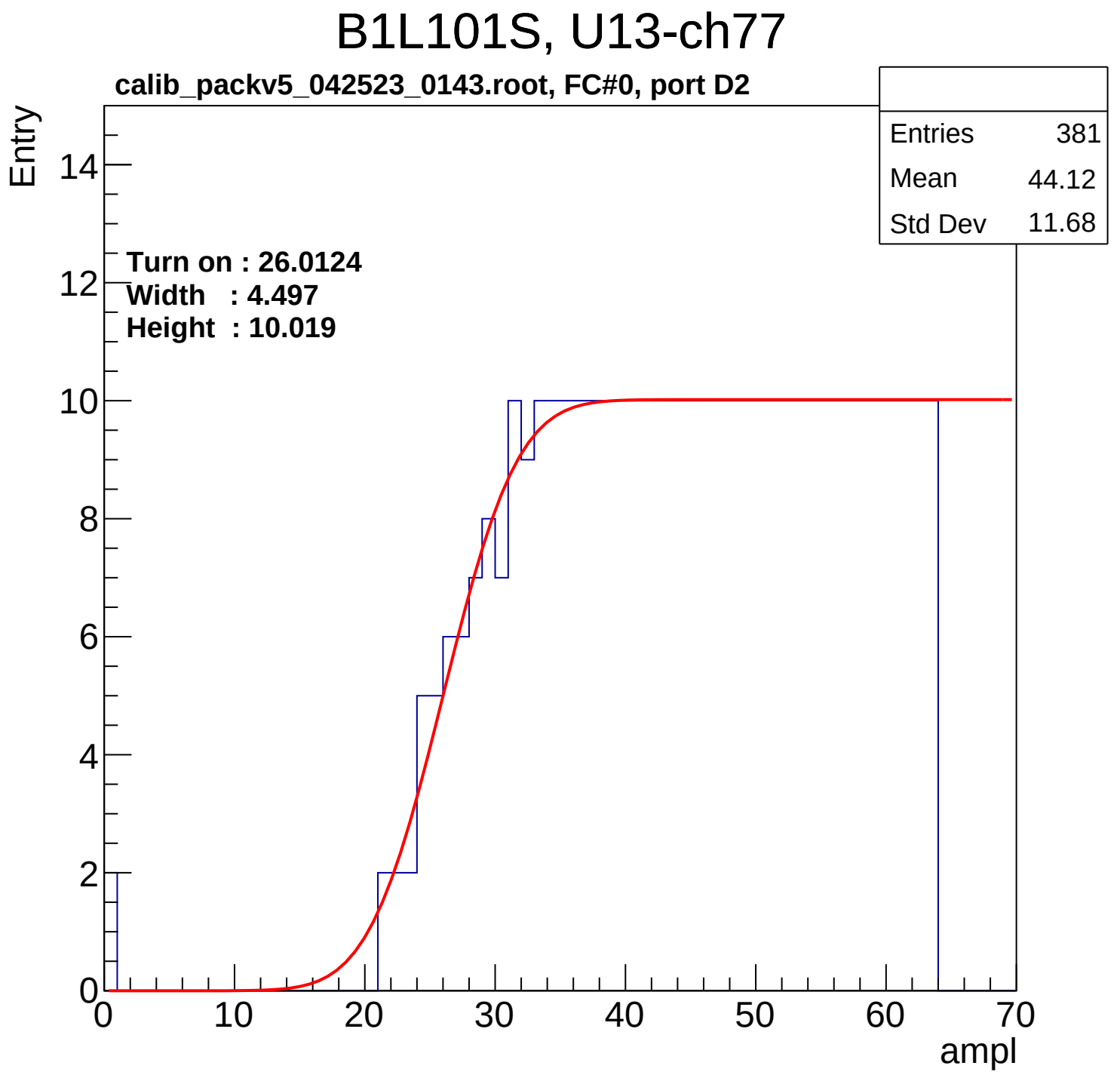
B1L101S, U13-ch77
calib_packv5_042523_0143.root, FC#0, port D2
Entries 381
Mean 44.12
Std Dev 11.68
Turn on : 26.0124
Width : 4.497
Height : 10.019
Entry
ampl
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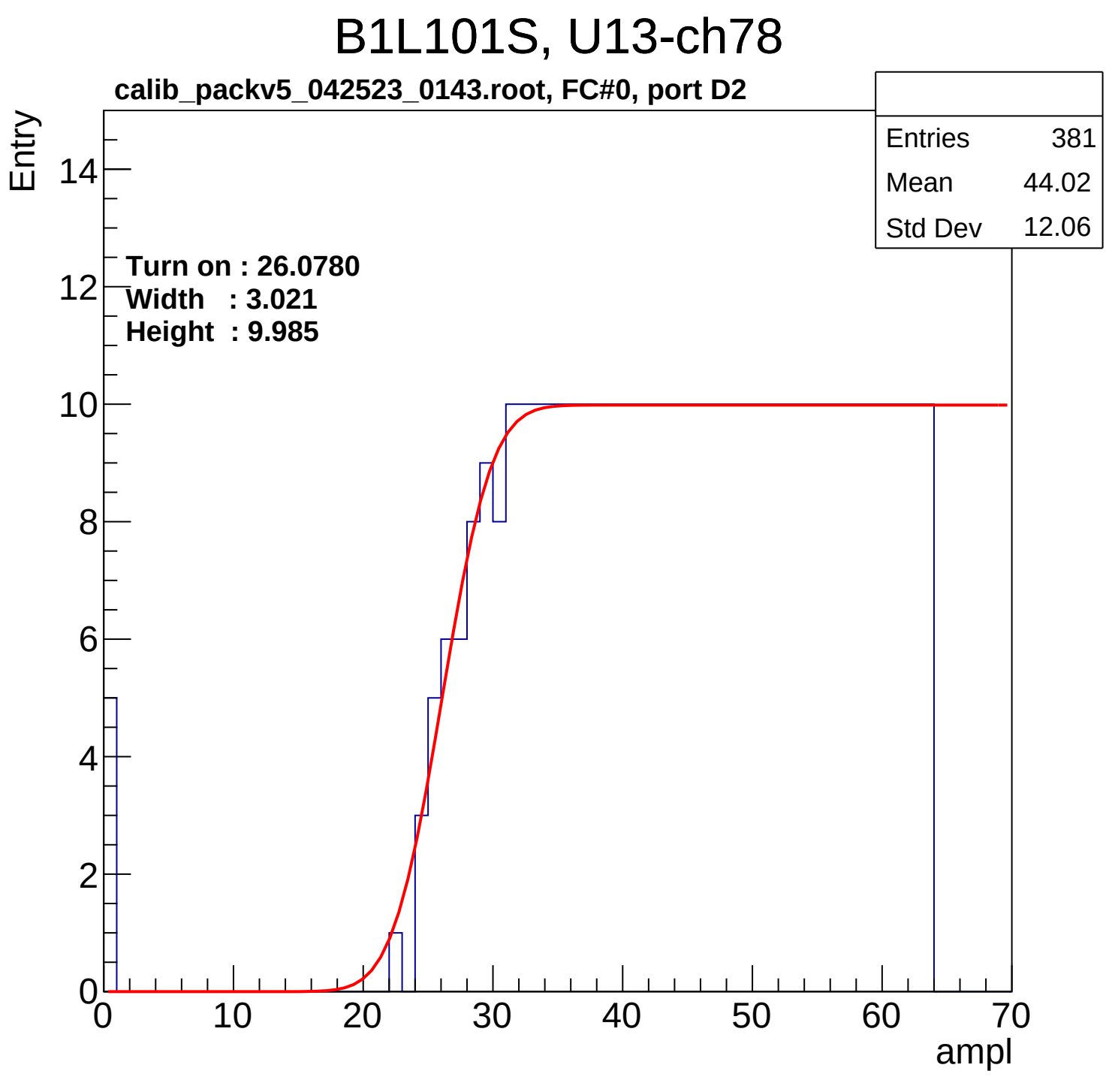
B1L101S, U13-ch78
calib_packv5_042523_0143.root, FC#0, port D2
Entries 381
Mean 44.02
Std Dev 12.06
Turn on : 26.0780
Width : 3.021
Height : 9.985
Entry
ampl
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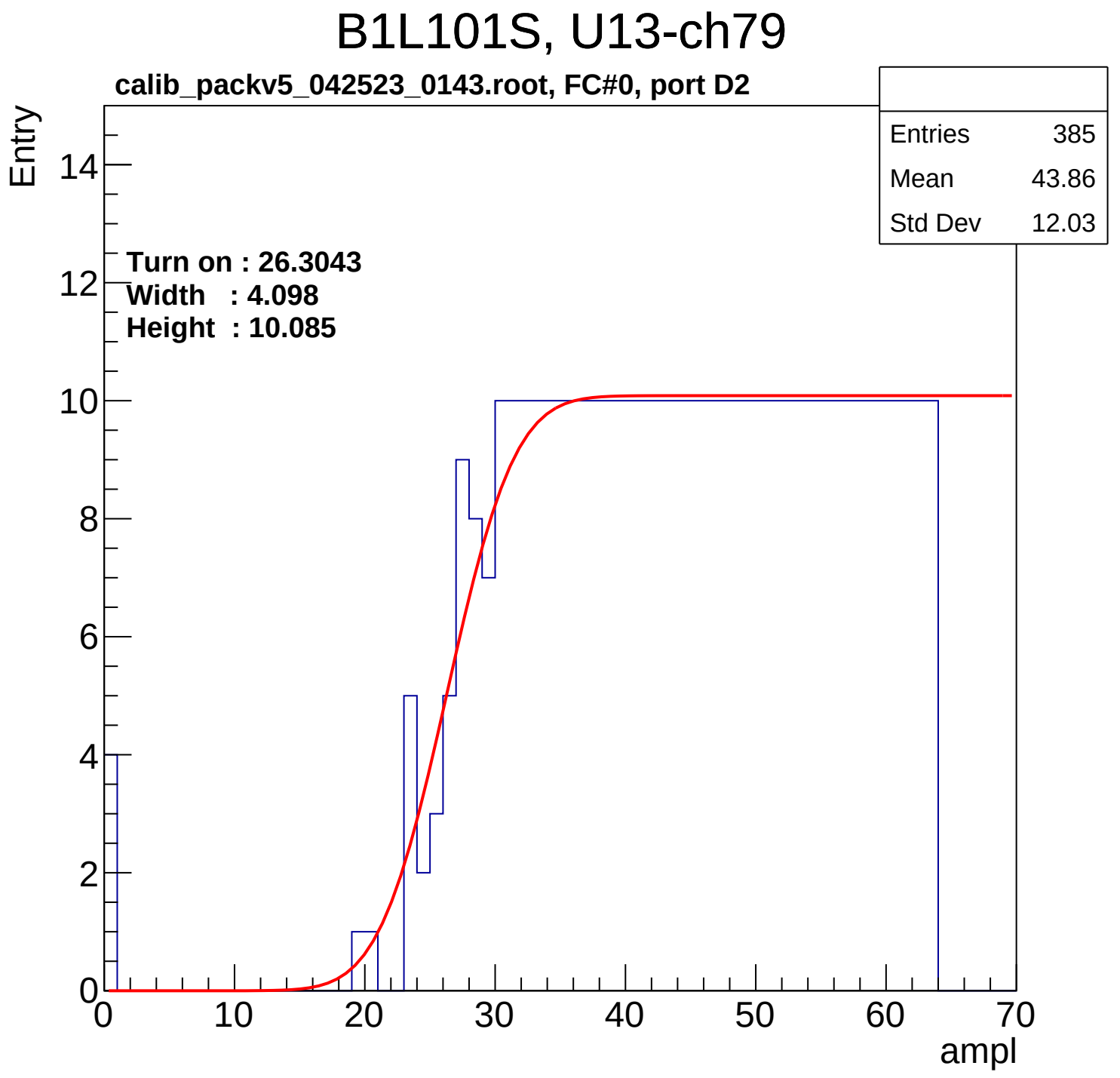
B1L101S, U13-ch79
calib_packv5_042523_0143.root, FC#0, port D2
Entries 385
Mean 43.86
Std Dev 12.03
Turn on : 26.3043
Width : 4.098
Height : 10.085
Entry
ampl
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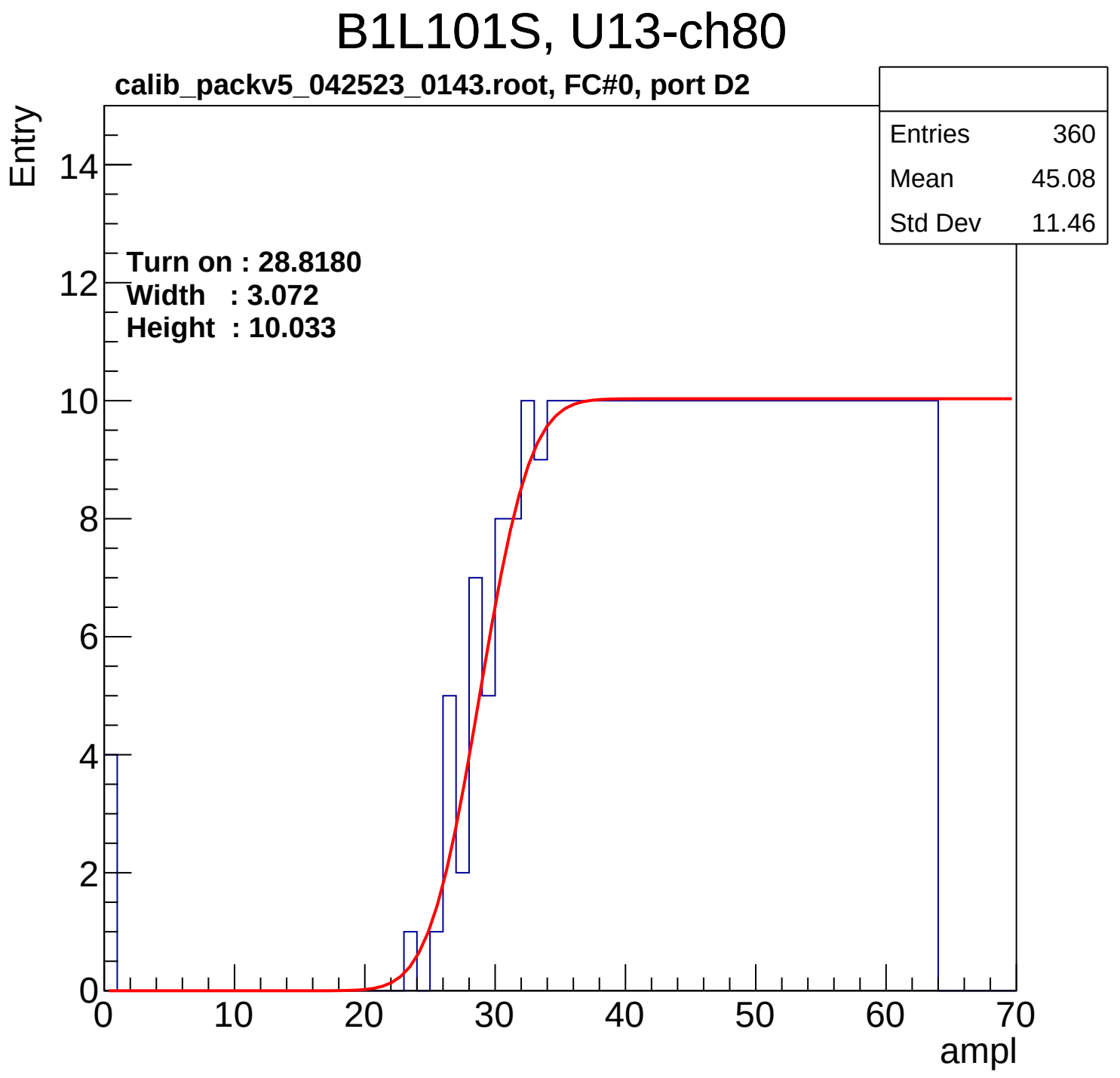
B1L101S, U13-ch80
calib_packv5_042523_0143.root, FC#0, port D2
Entries 360
Mean 45.08
Std Dev 11.46
Turn on : 28.8180
Width : 3.072
Height : 10.033
Entry
ampl
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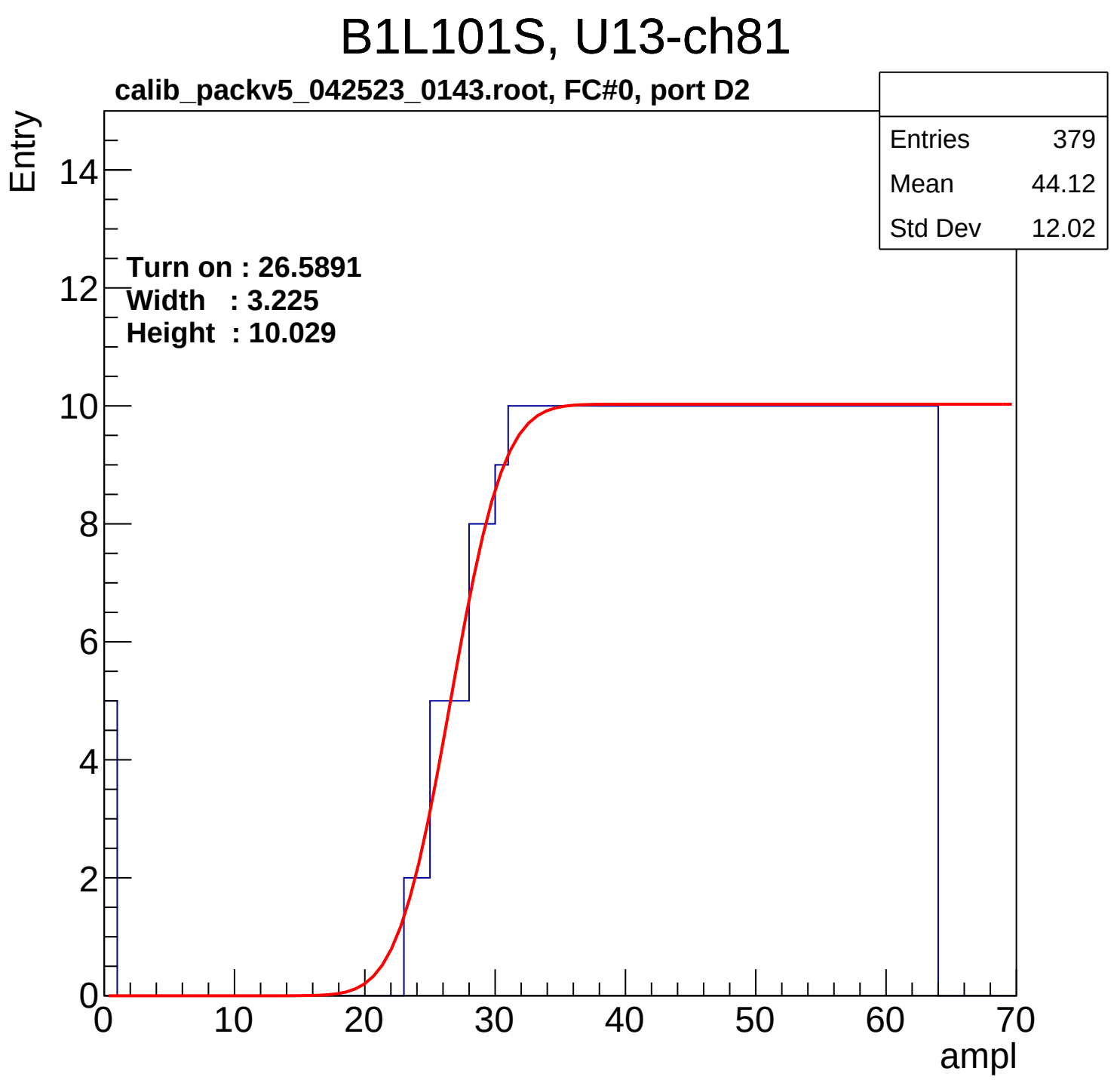
B1L101S, U13-ch81
calib_packv5_042523_0143.root, FC#0, port D2
Entries 379
Mean 44.12
Std Dev 12.02
Turn on : 26.5891
Width : 3.225
Height : 10.029
Entry
ampl
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2
4
6
8
10
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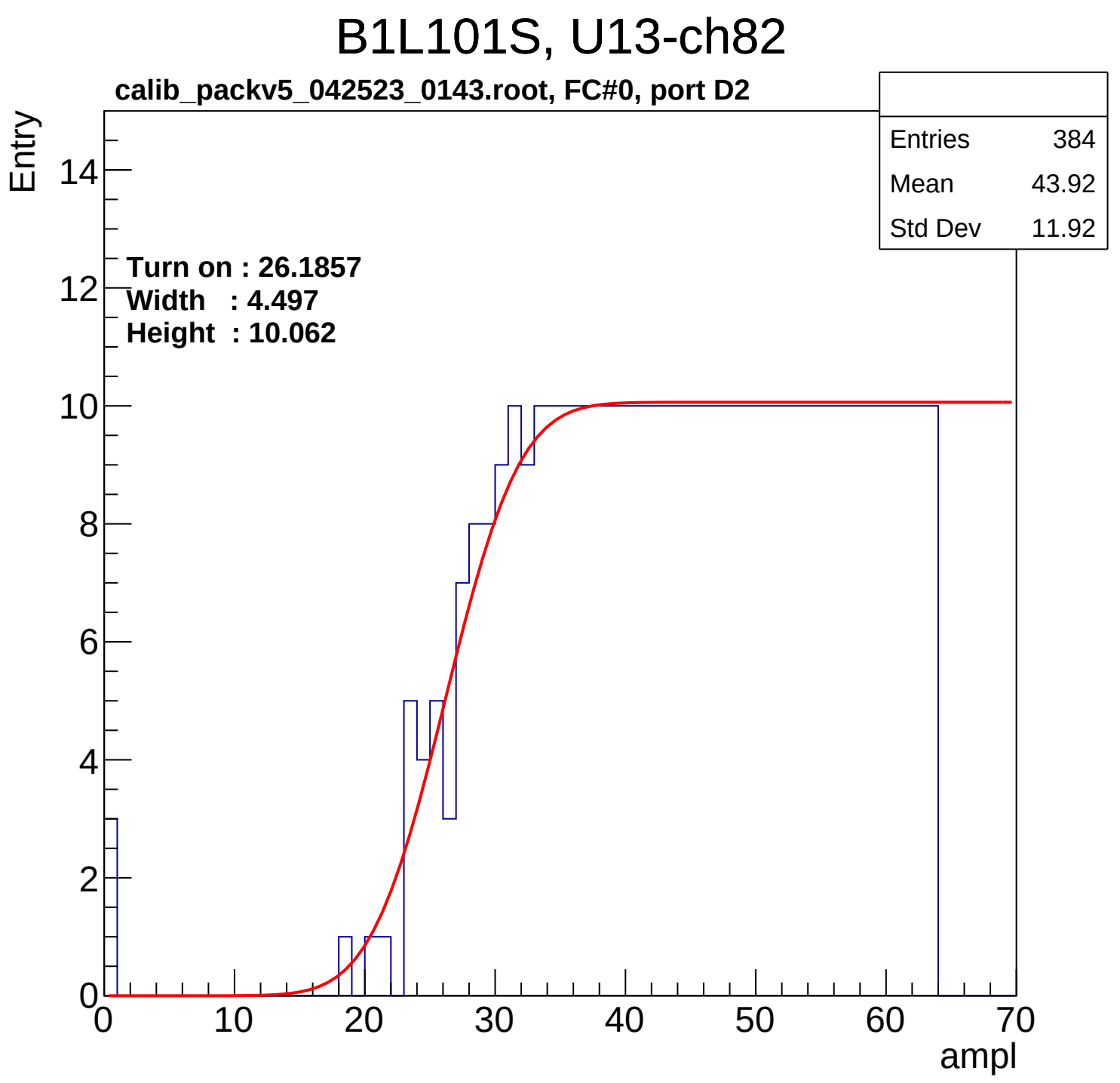
B1L101S, U13-ch82
calib_packv5_042523_0143.root, FC#0, port D2
Entries 384
Mean 43.92
Std Dev 11.92
Turn on : 26.1857
Width : 4.497
Height : 10.062
Entry
ampl
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6
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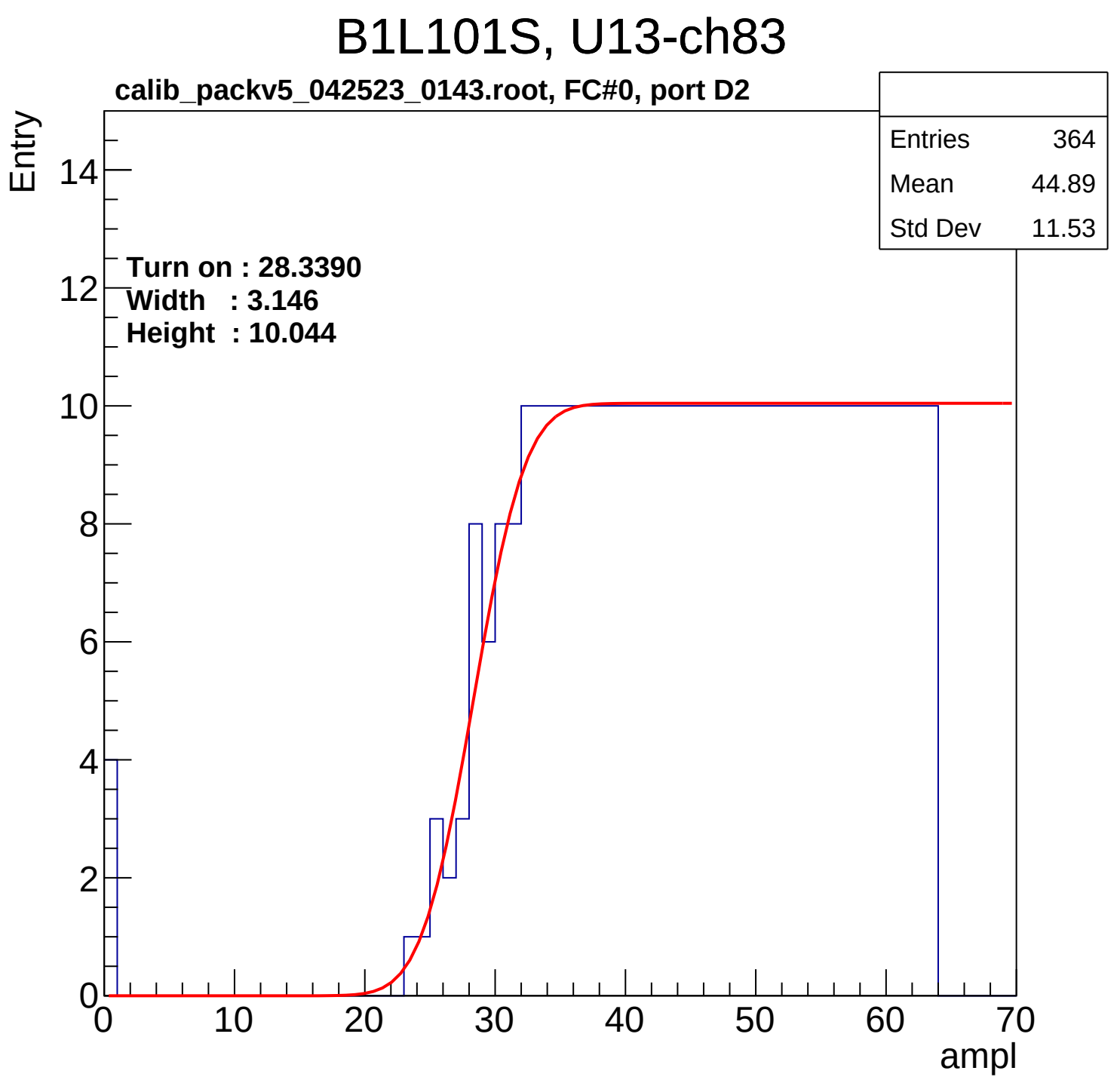
B1L101S, U13-ch83
calib_packv5_042523_0143.root, FC#0, port D2
Entries 364
Mean 44.89
Std Dev 11.53
Turn on : 28.3390
Width : 3.146
Height : 10.044
Entry
ampl
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6
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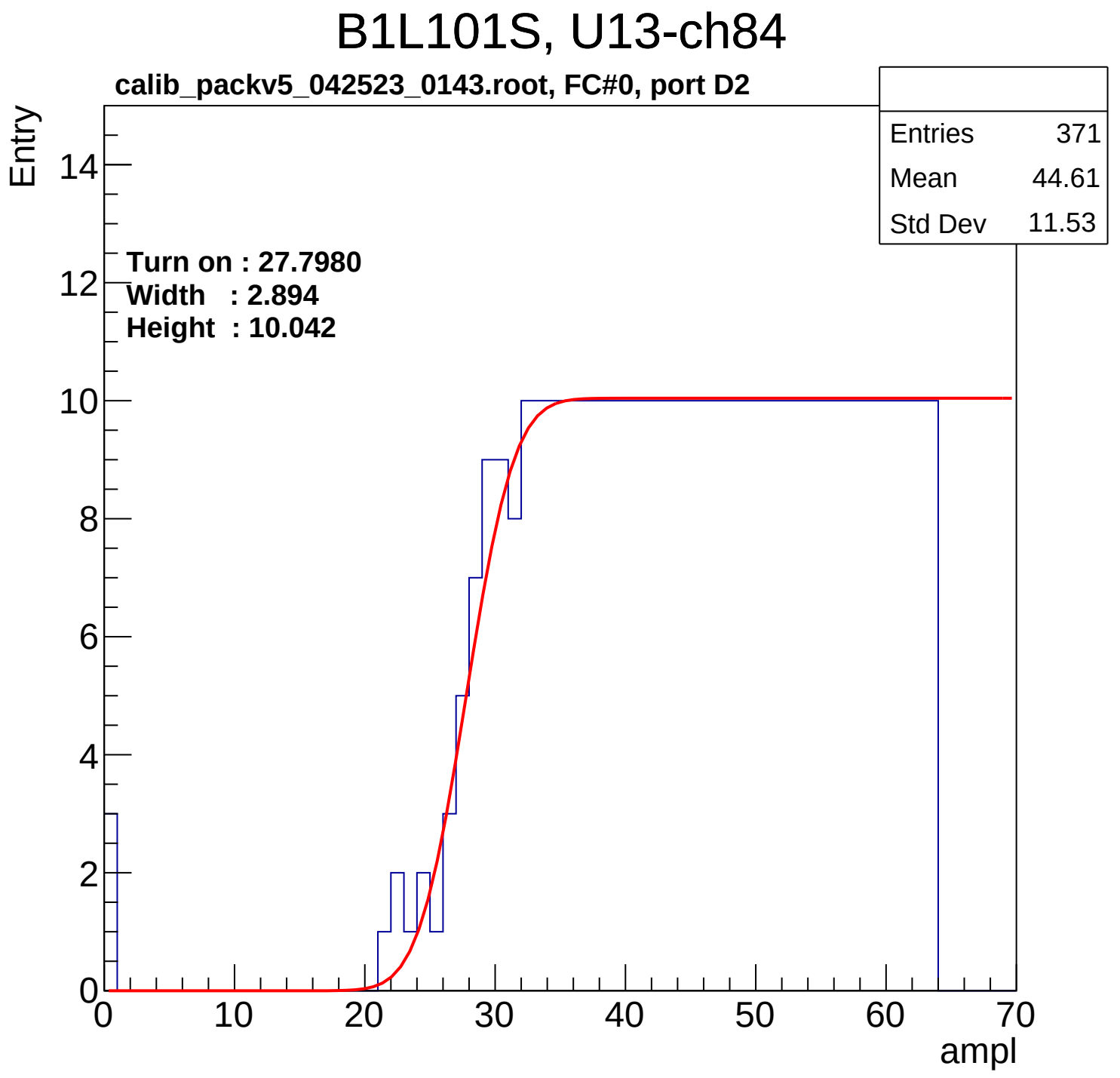
B1L101S, U13-ch84
calib_packv5_042523_0143.root, FC#0, port D2
Entries 371
Mean 44.61
Std Dev 11.53
Turn on : 27.7980
Width : 2.894
Height : 10.042
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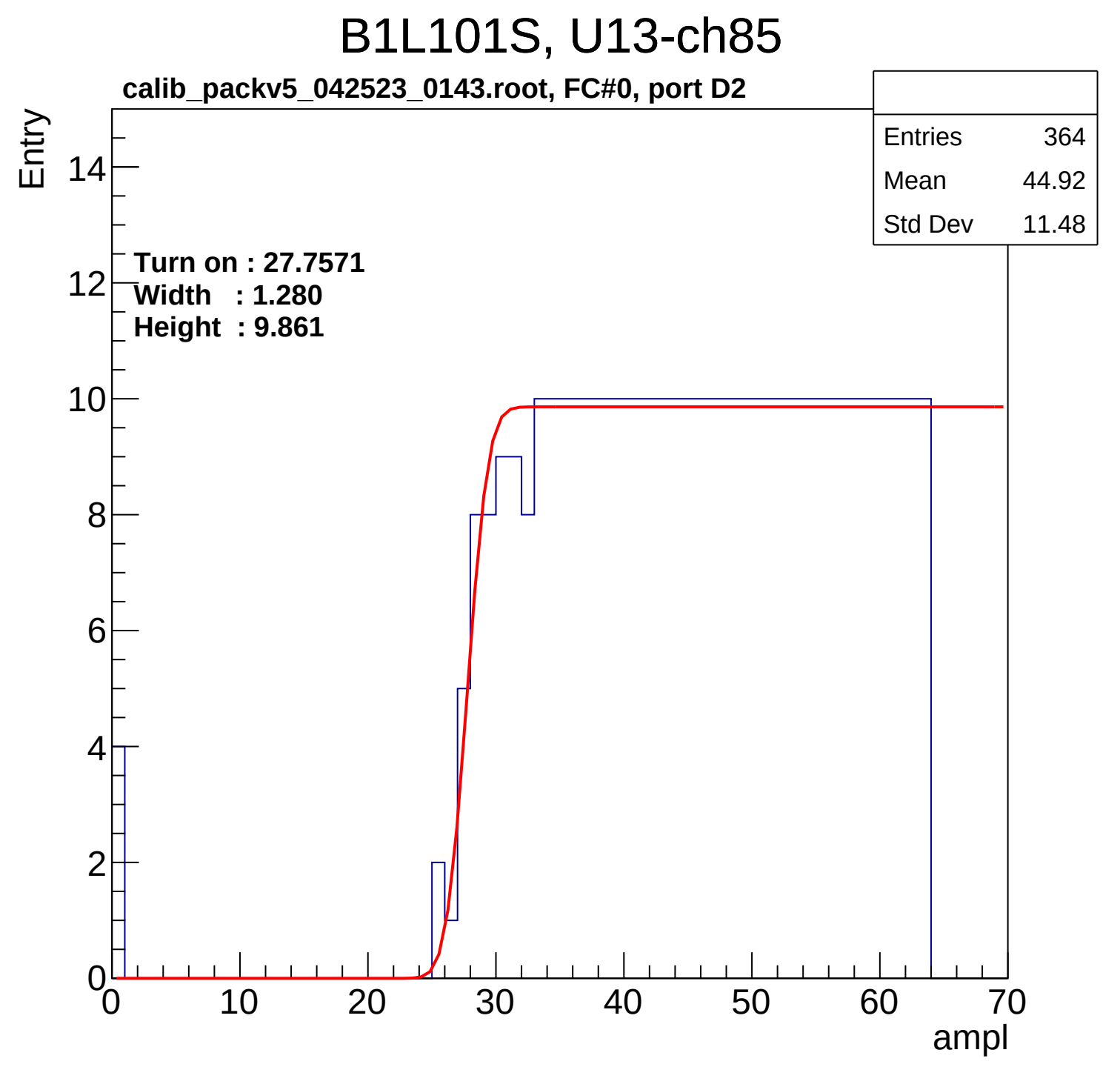
B1L101S, U13-ch85
calib_packv5_042523_0143.root, FC#0, port D2
Entries 364
Mean 44.92
Std Dev 11.48
Turn on : 27.7571
Width : 1.280
Height : 9.861
Entry
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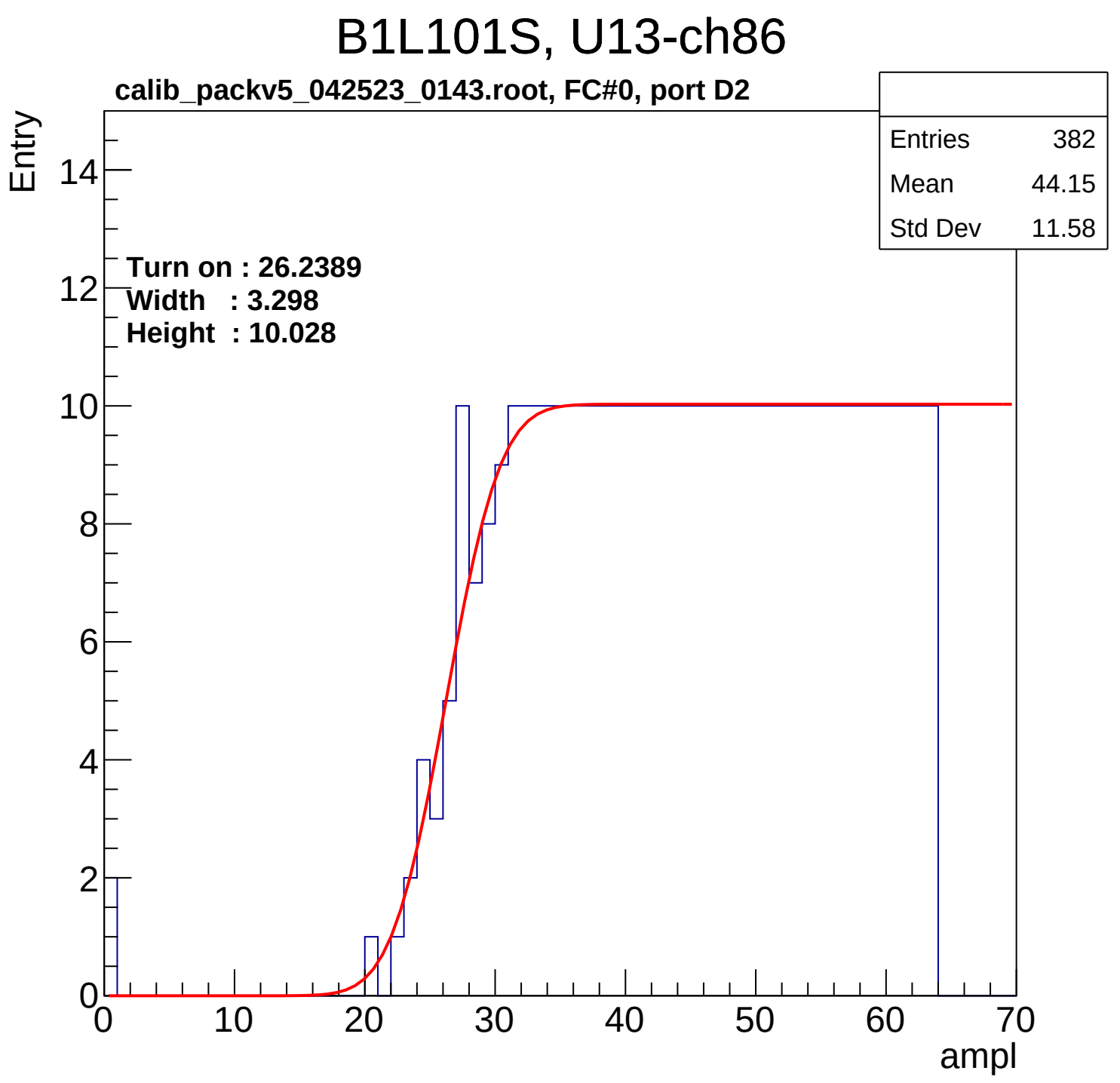
B1L101S, U13-ch86
calib_packv5_042523_0143.root, FC#0, port D2
Entries 382
Mean 44.15
Std Dev 11.58
Turn on : 26.2389
Width : 3.298
Height : 10.028
Entry
ampl
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6
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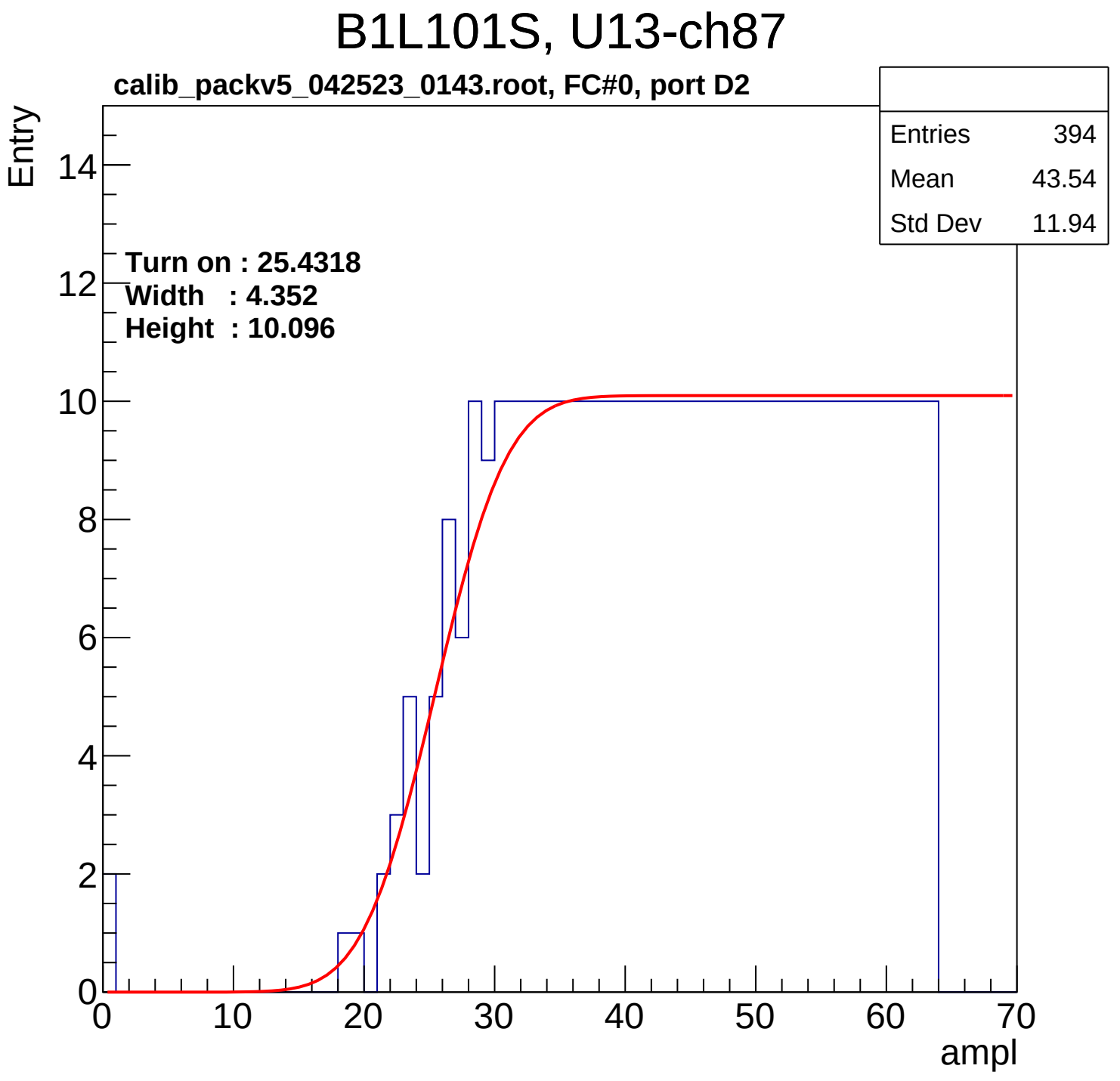
B1L101S, U13-ch87
calib_packv5_042523_0143.root, FC#0, port D2
Entries 394
Mean 43.54
Std Dev 11.94
Turn on : 25.4318
Width : 4.352
Height : 10.096
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ampl
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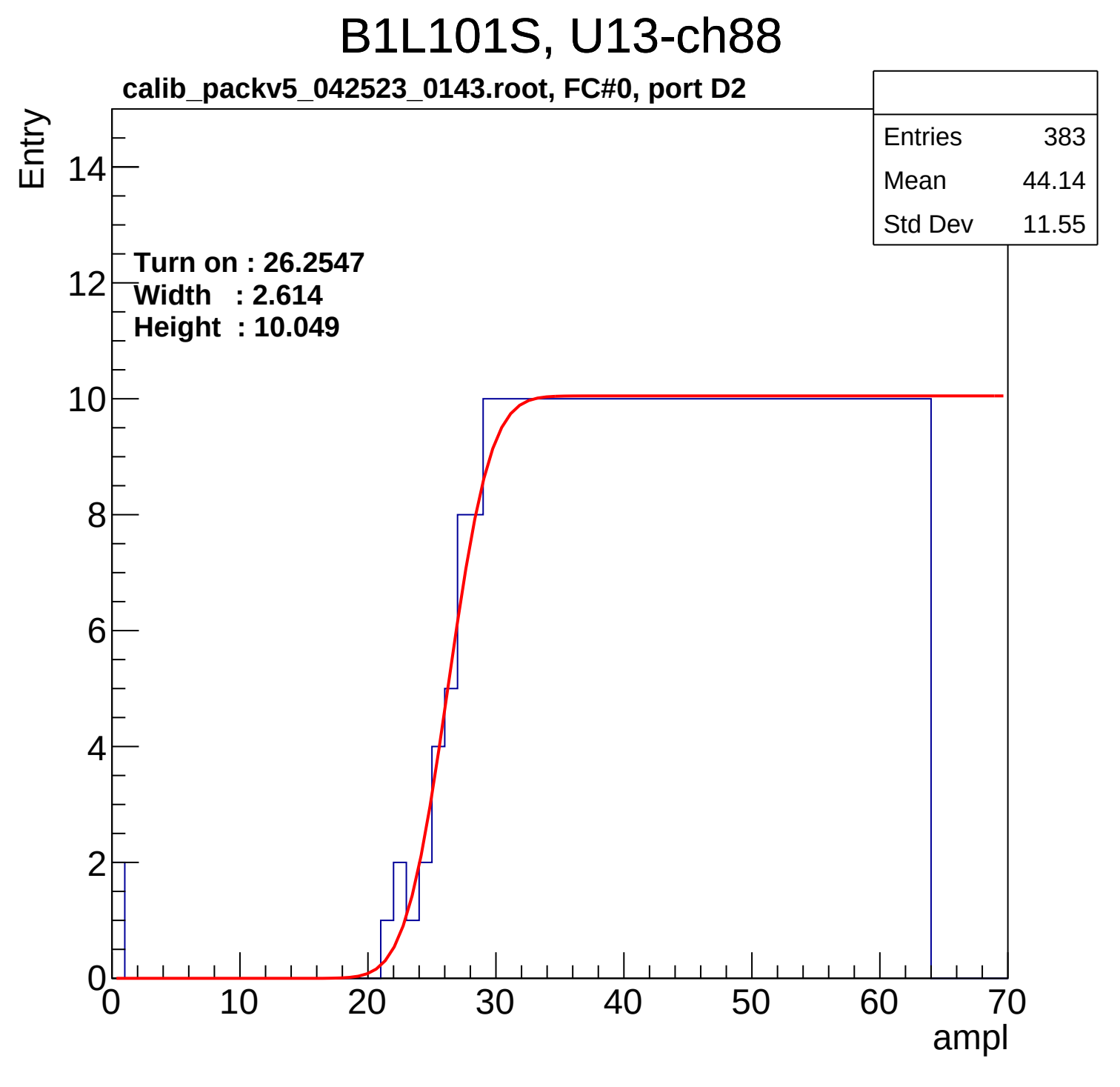
B1L101S, U13-ch88
calib_packv5_042523_0143.root, FC#0, port D2
Entries 383
Mean 44.14
Std Dev 11.55
Turn on : 26.2547
Width : 2.614
Height : 10.049
Entry
ampl
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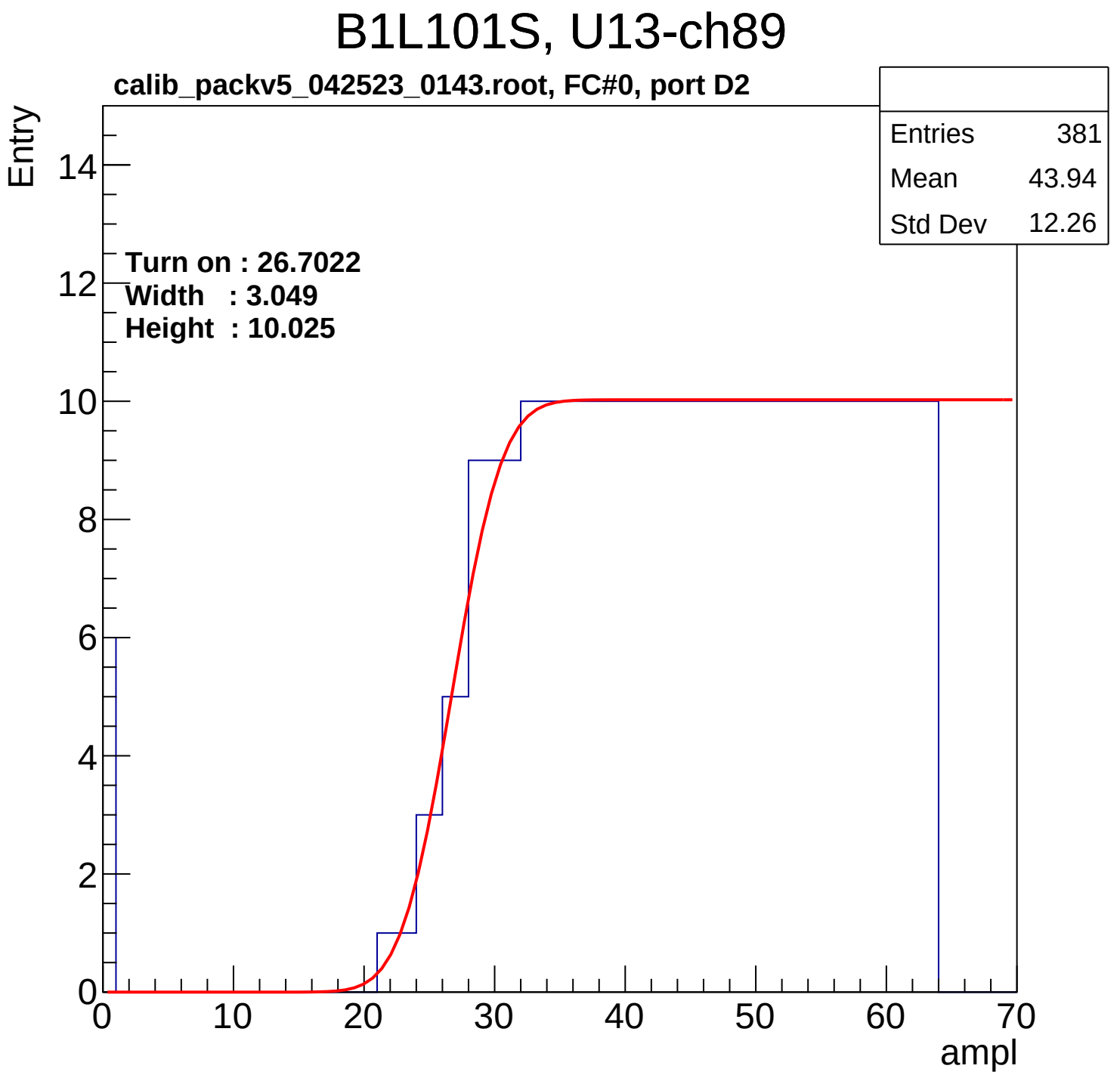
B1L101S, U13-ch89
calib_packv5_042523_0143.root, FC#0, port D2
Entries 381
Mean 43.94
Std Dev 12.26
Turn on : 26.7022
Width : 3.049
Height : 10.025
Entry
ampl
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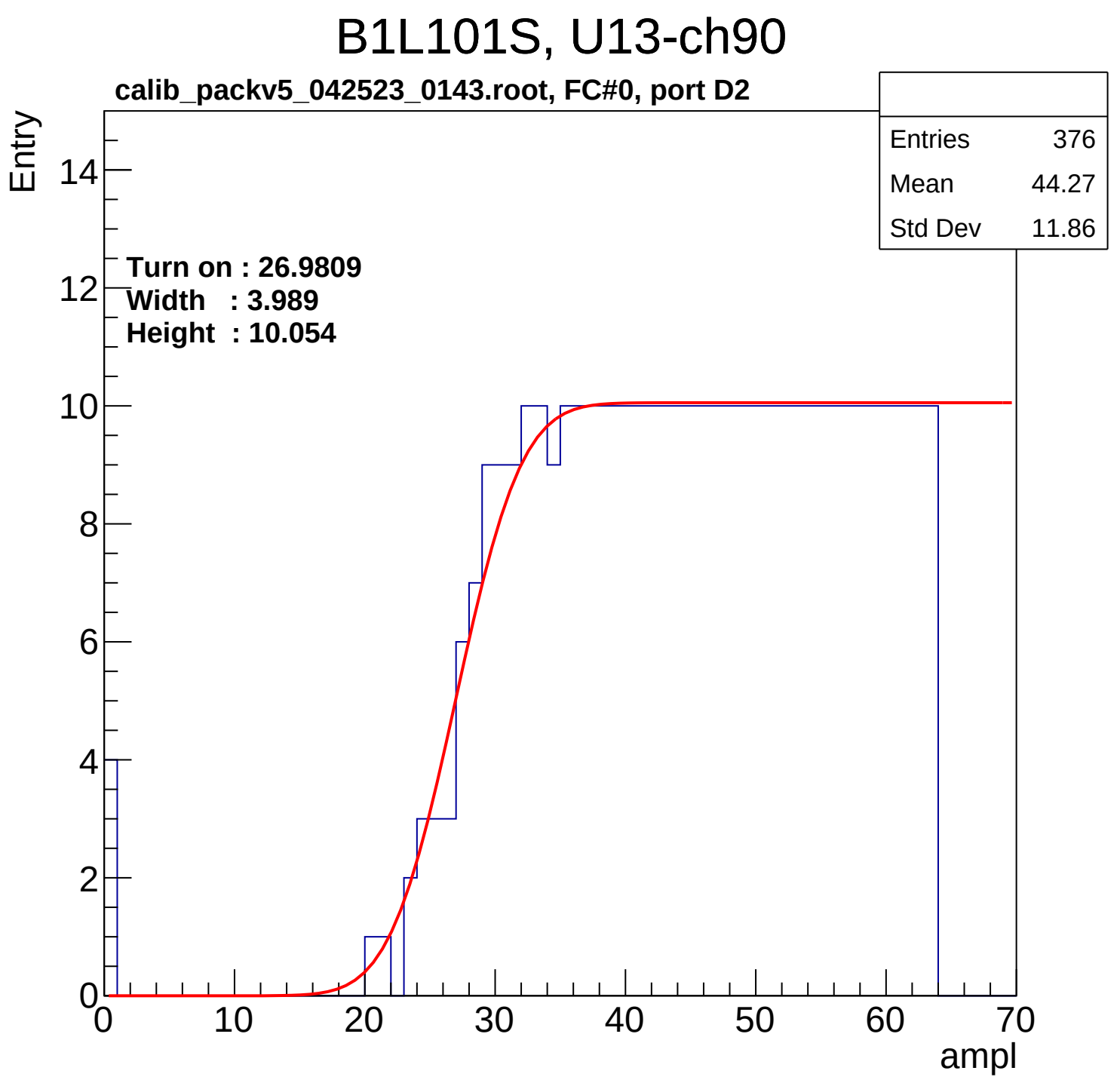
B1L101S, U13-ch90
calib_packv5_042523_0143.root, FC#0, port D2
Entries 376
Mean 44.27
Std Dev 11.86
Turn on : 26.9809
Width : 3.989
Height : 10.054
Entry
ampl
0
2
4
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8
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12
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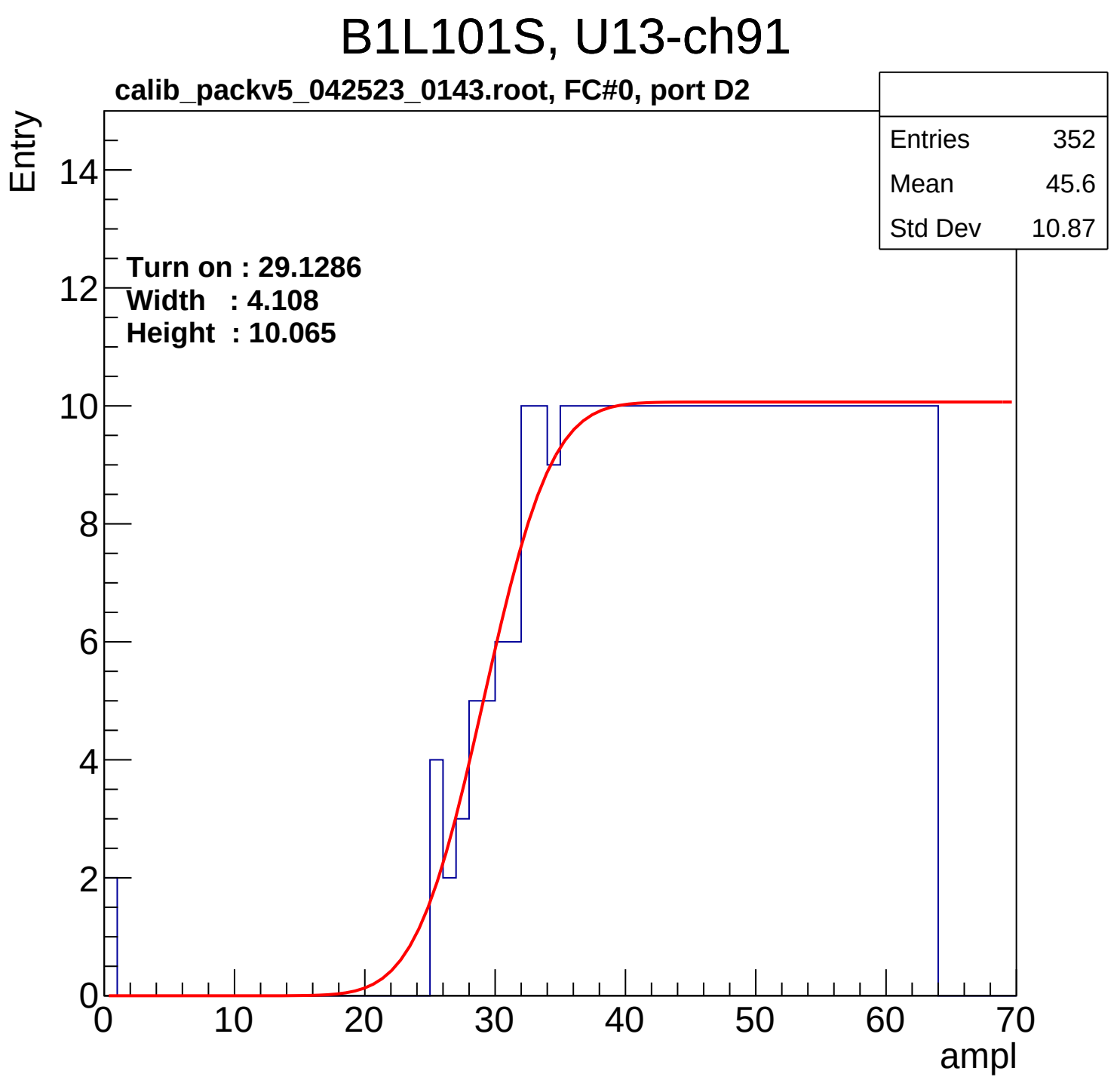
B1L101S, U13-ch91
calib_packv5_042523_0143.root, FC#0, port D2
Entries 352
Mean 45.6
Std Dev 10.87
Turn on : 29.1286
Width : 4.108
Height : 10.065
Entry
ampl
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2
4
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8
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12
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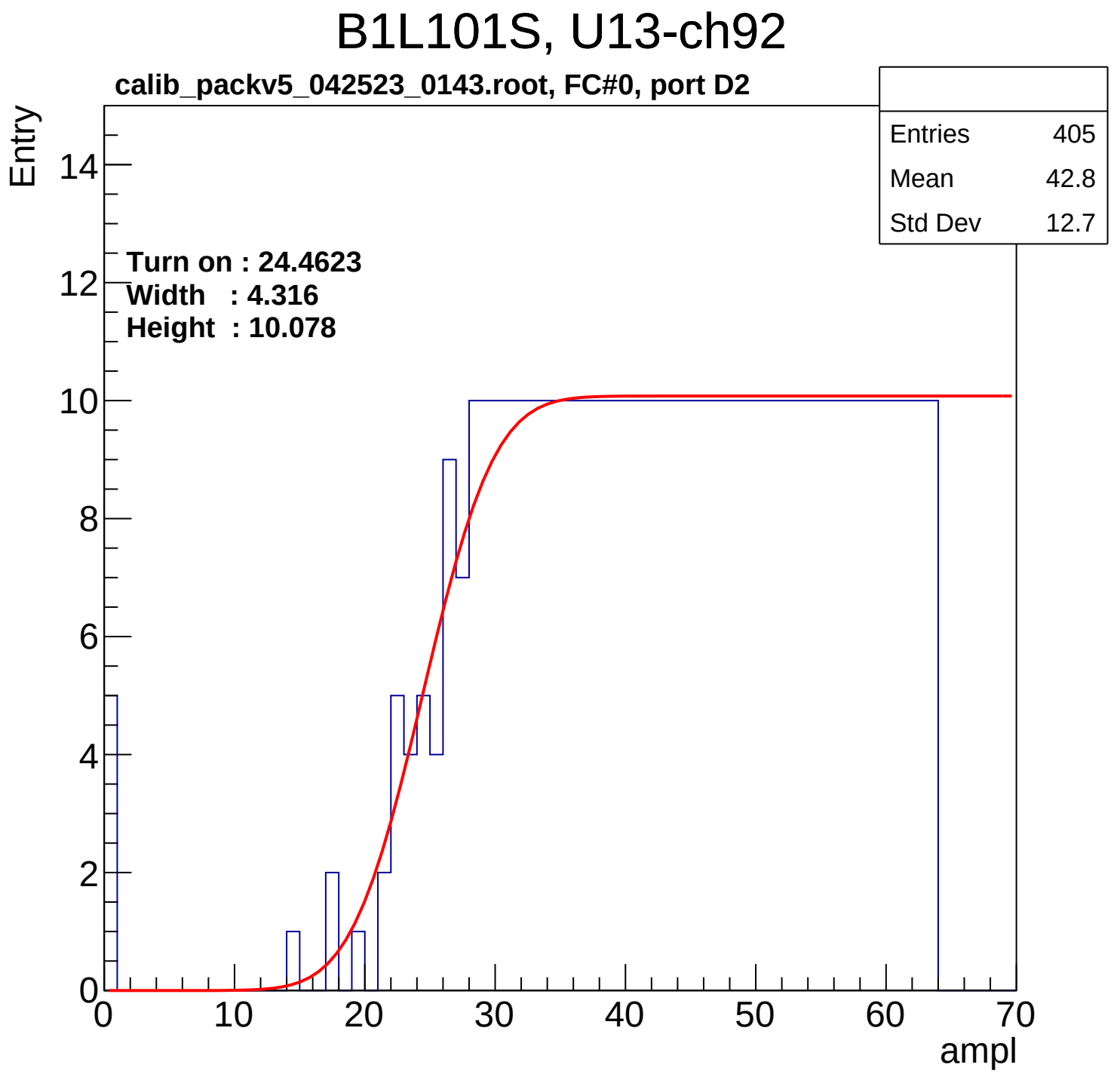
B1L101S, U13-ch92
calib_packv5_042523_0143.root, FC#0, port D2
Entries 405
Mean 42.8
Std Dev 12.7
Turn on : 24.4623
Width : 4.316
Height : 10.078
Entry
ampl
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2
4
6
8
10
12
14
0
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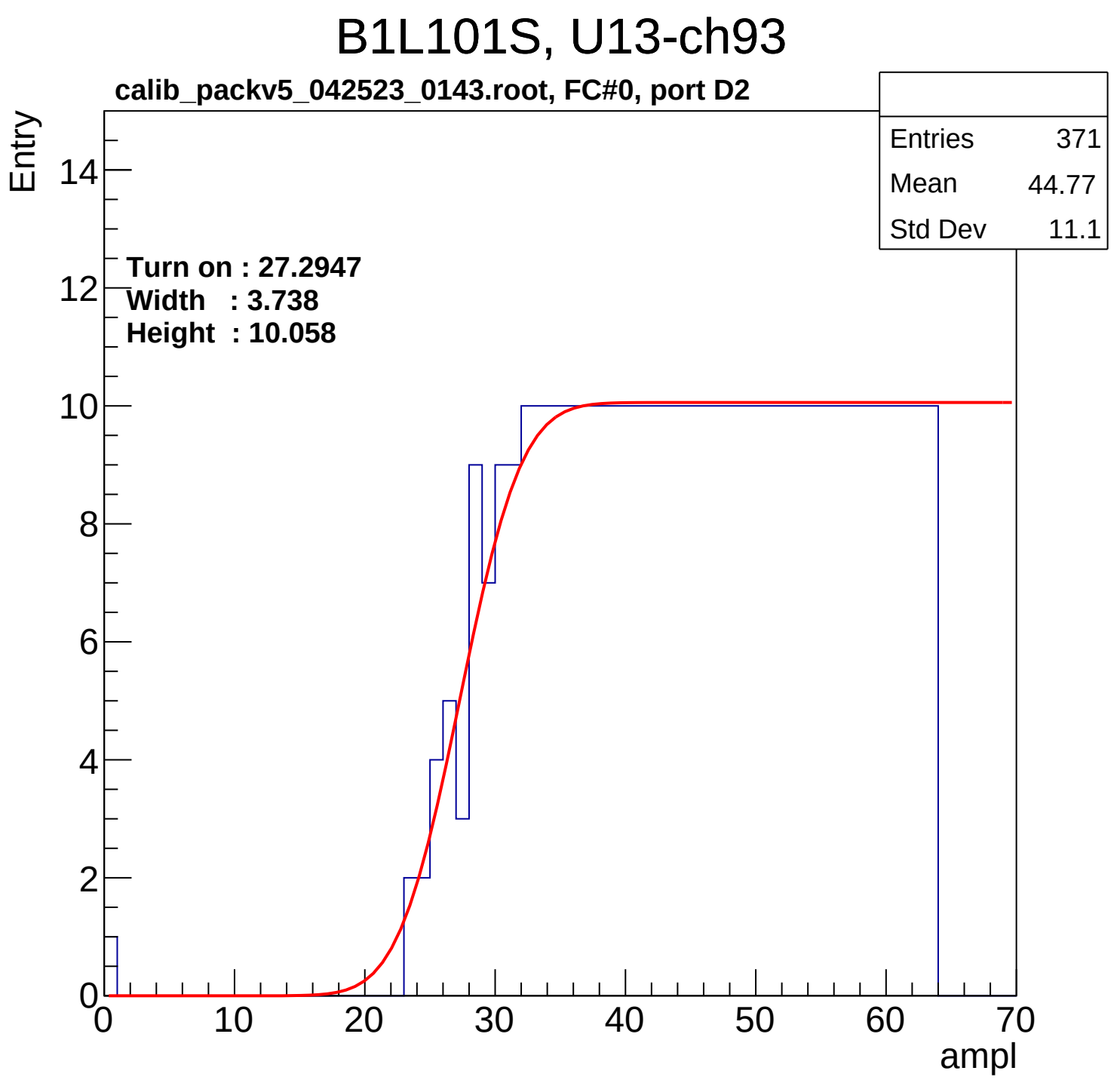
B1L101S, U13-ch93
calib_packv5_042523_0143.root, FC#0, port D2
Entries 371
Mean 44.77
Std Dev 11.1
Turn on : 27.2947
Width : 3.738
Height : 10.058
Entry
ampl
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2
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6
8
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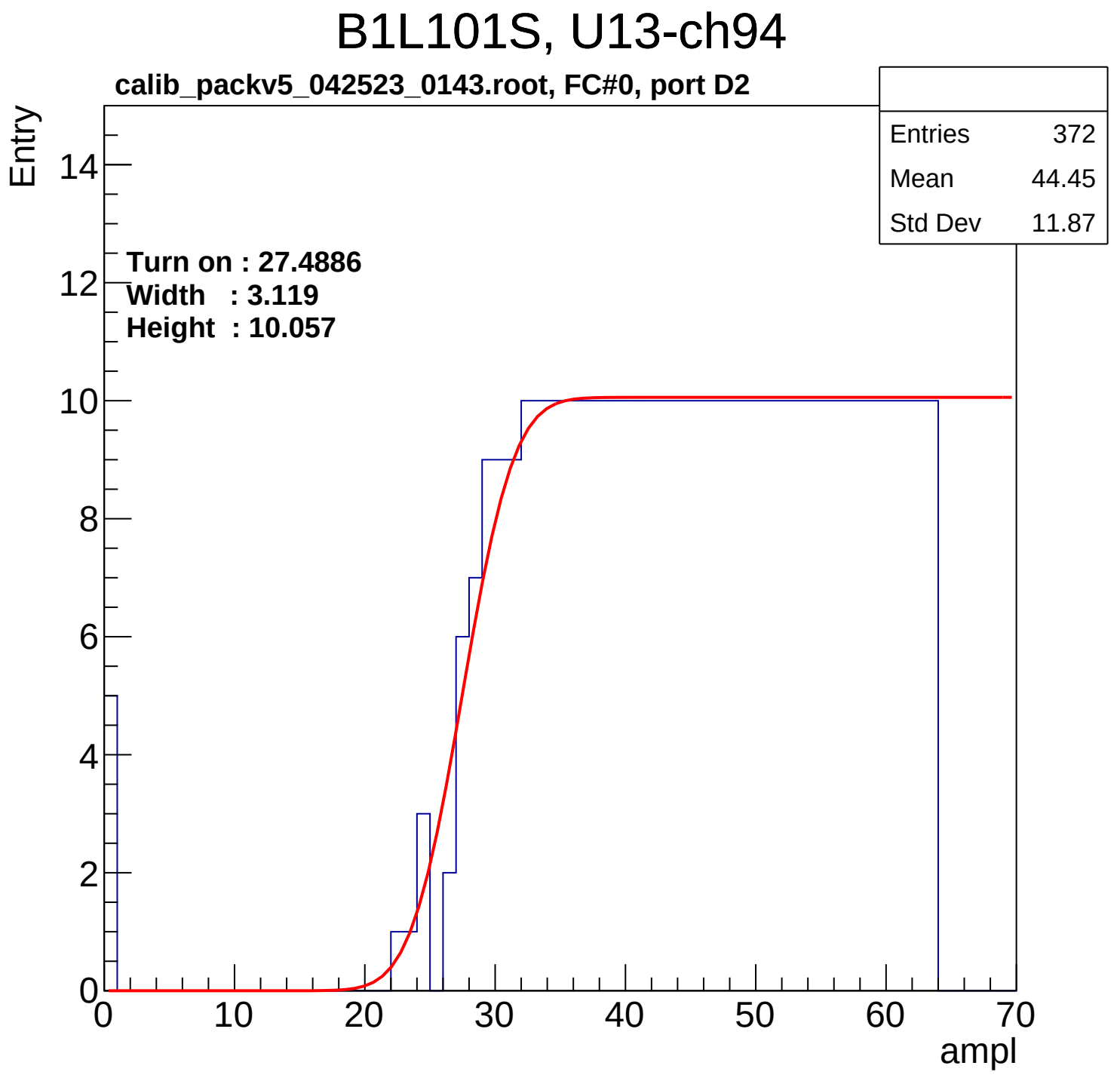
B1L101S, U13-ch94
calib_packv5_042523_0143.root, FC#0, port D2
Entries 372
Mean 44.45
Std Dev 11.87
Turn on : 27.4886
Width : 3.119
Height : 10.057
Entry
ampl
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2
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6
8
10
12
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0
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60
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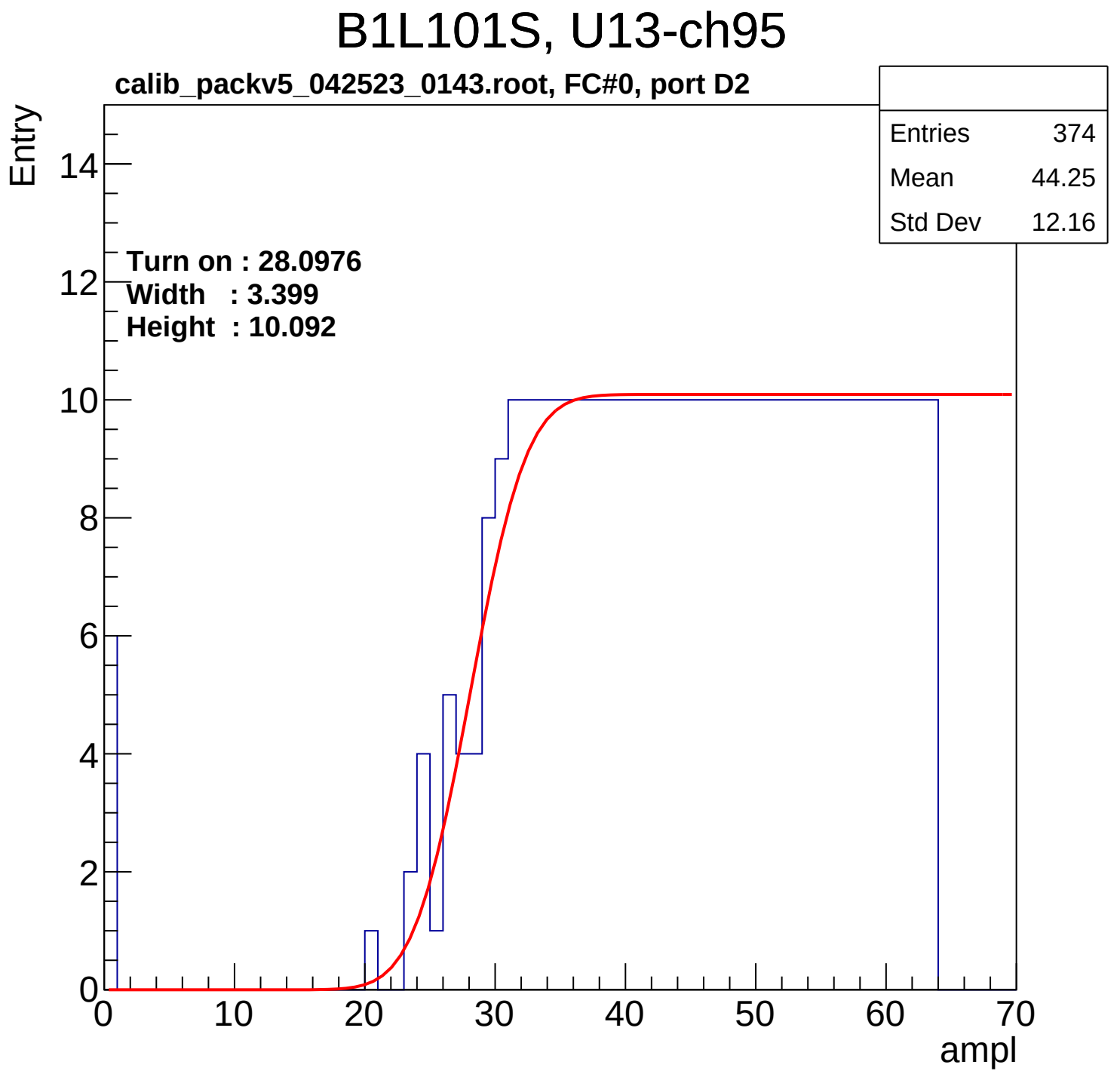
B1L101S, U13-ch95
calib_packv5_042523_0143.root, FC#0, port D2
Entries 374
Mean 44.25
Std Dev 12.16
Turn on : 28.0976
Width : 3.399
Height : 10.092
Entry
ampl
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2
4
6
8
10
12
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0
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60
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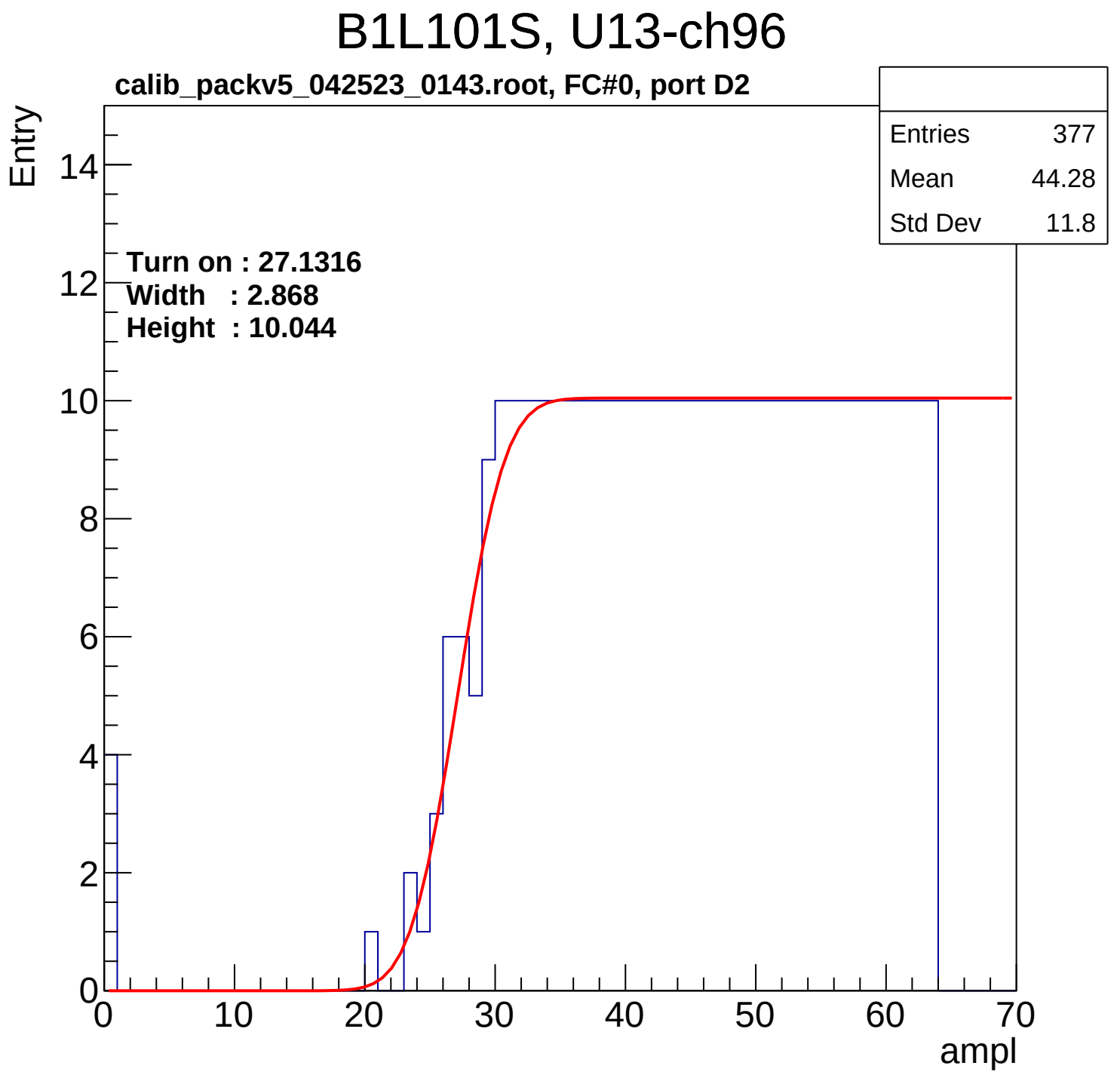
B1L101S, U13-ch96
calib_packv5_042523_0143.root, FC#0, port D2
Entries 377
Mean 44.28
Std Dev 11.8
Turn on : 27.1316
Width : 2.868
Height : 10.044
Entry
ampl
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2
4
6
8
10
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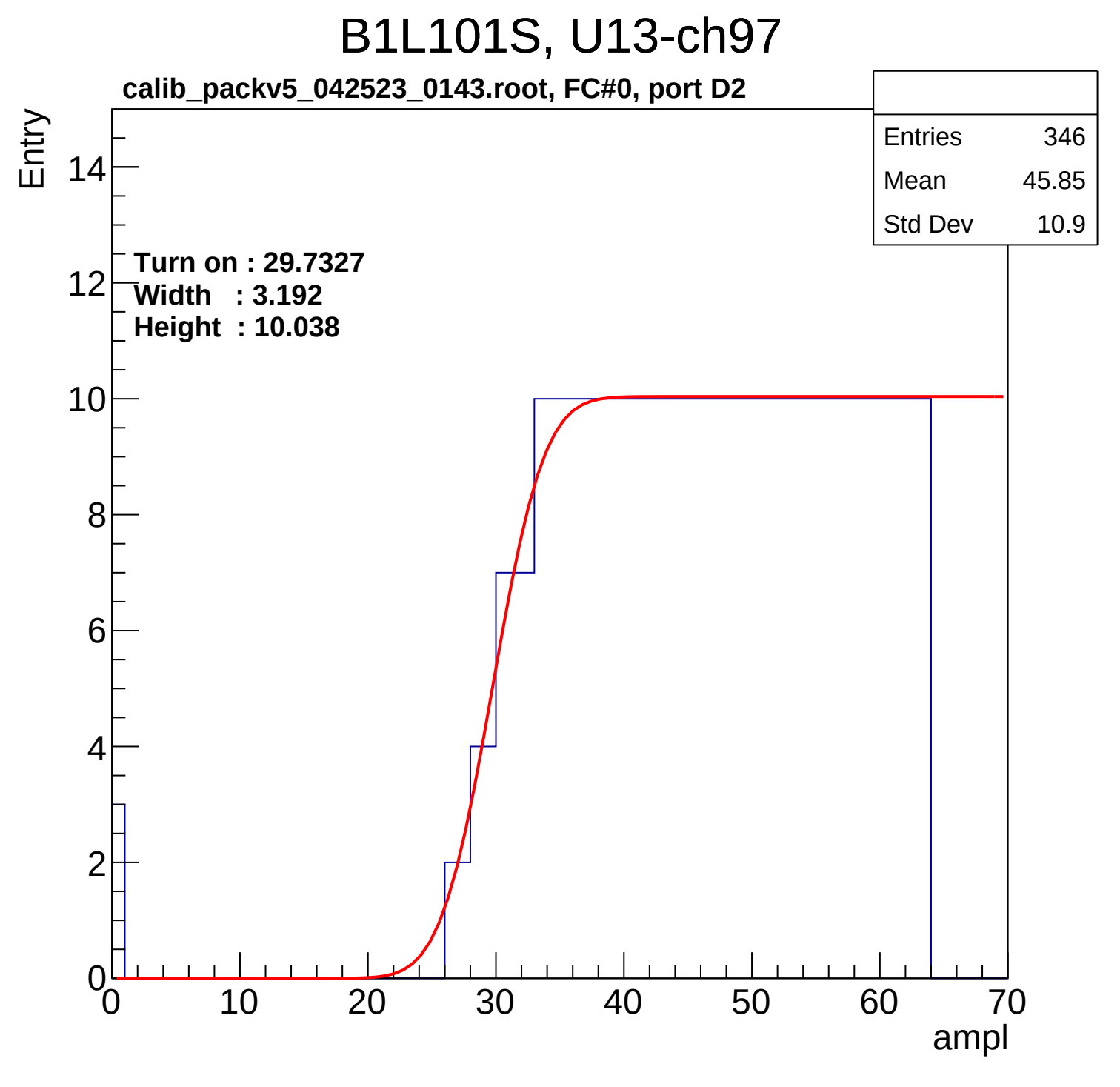
B1L101S, U13-ch97
calib_packv5_042523_0143.root, FC#0, port D2
Entries 346
Mean 45.85
Std Dev 10.9
Turn on : 29.7327
Width : 3.192
Height : 10.038
Entry
ampl
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6
8
10
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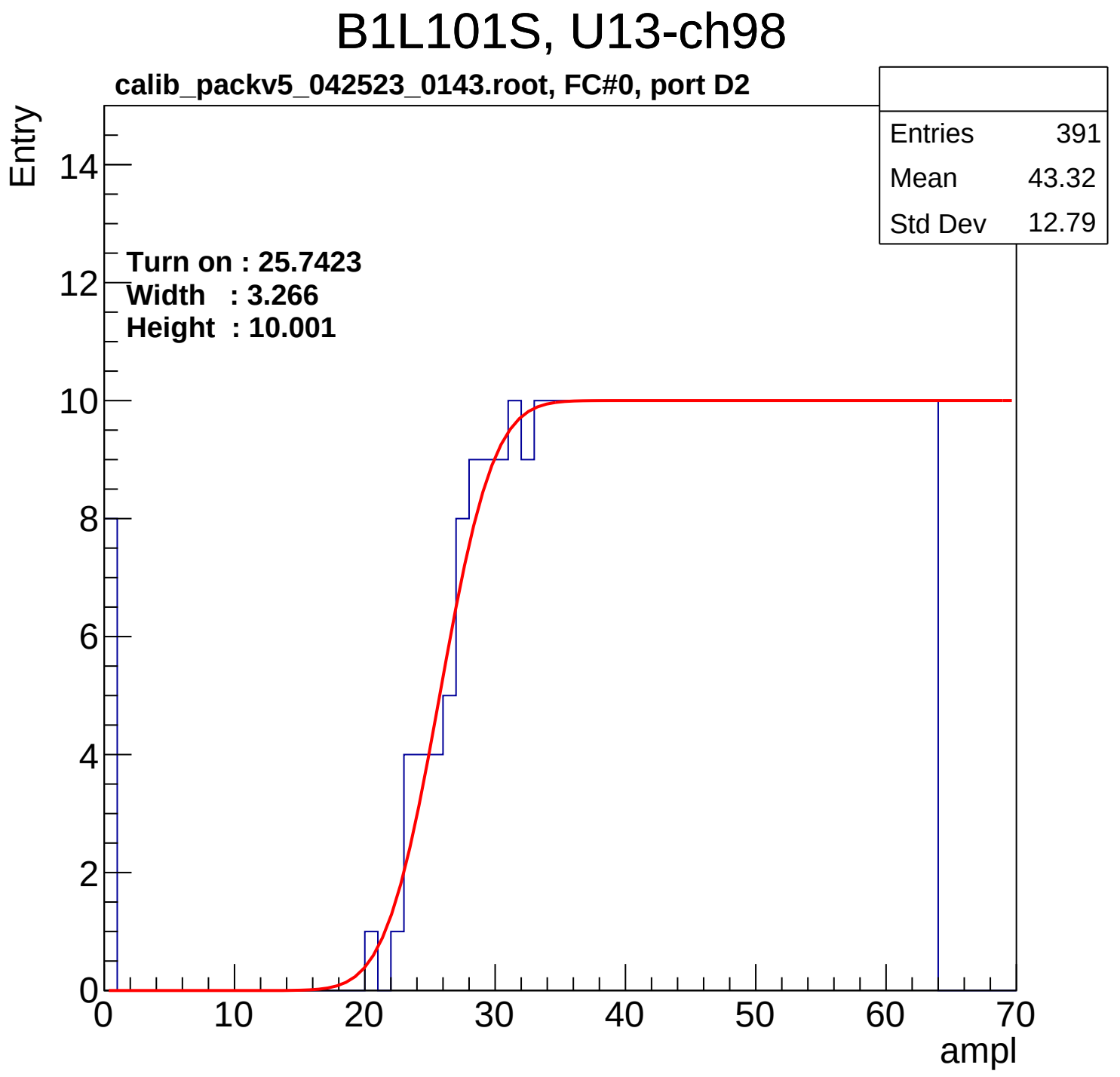
B1L101S, U13-ch98
calib_packv5_042523_0143.root, FC#0, port D2
Entries 391
Mean 43.32
Std Dev 12.79
Turn on : 25.7423
Width : 3.266
Height : 10.001
Entry
ampl
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4
6
8
10
12
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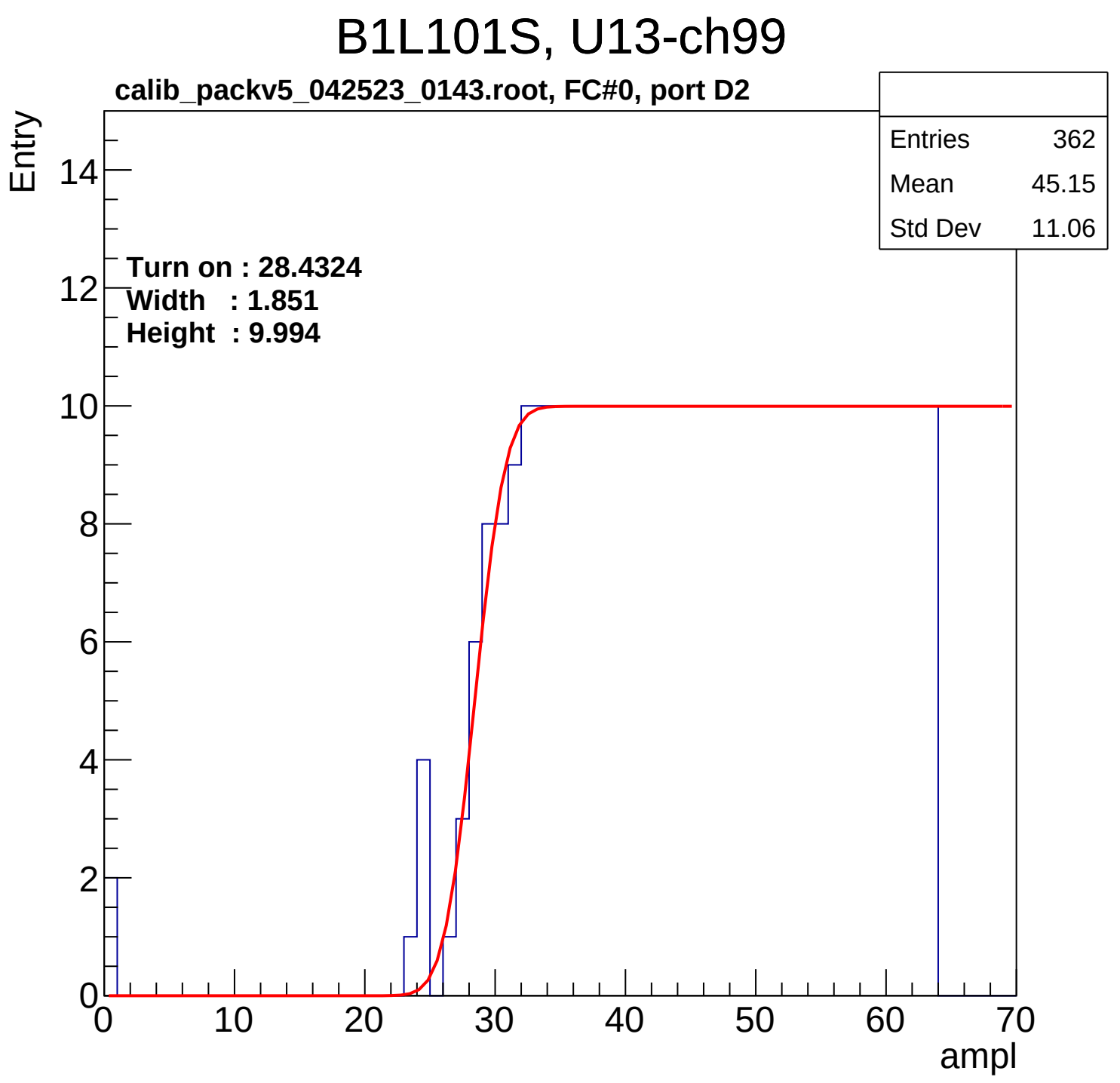
B1L101S, U13-ch99
calib_packv5_042523_0143.root, FC#0, port D2
Entries 362
Mean 45.15
Std Dev 11.06
Turn on : 28.4324
Width : 1.851
Height : 9.994
Entry
ampl
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6
8
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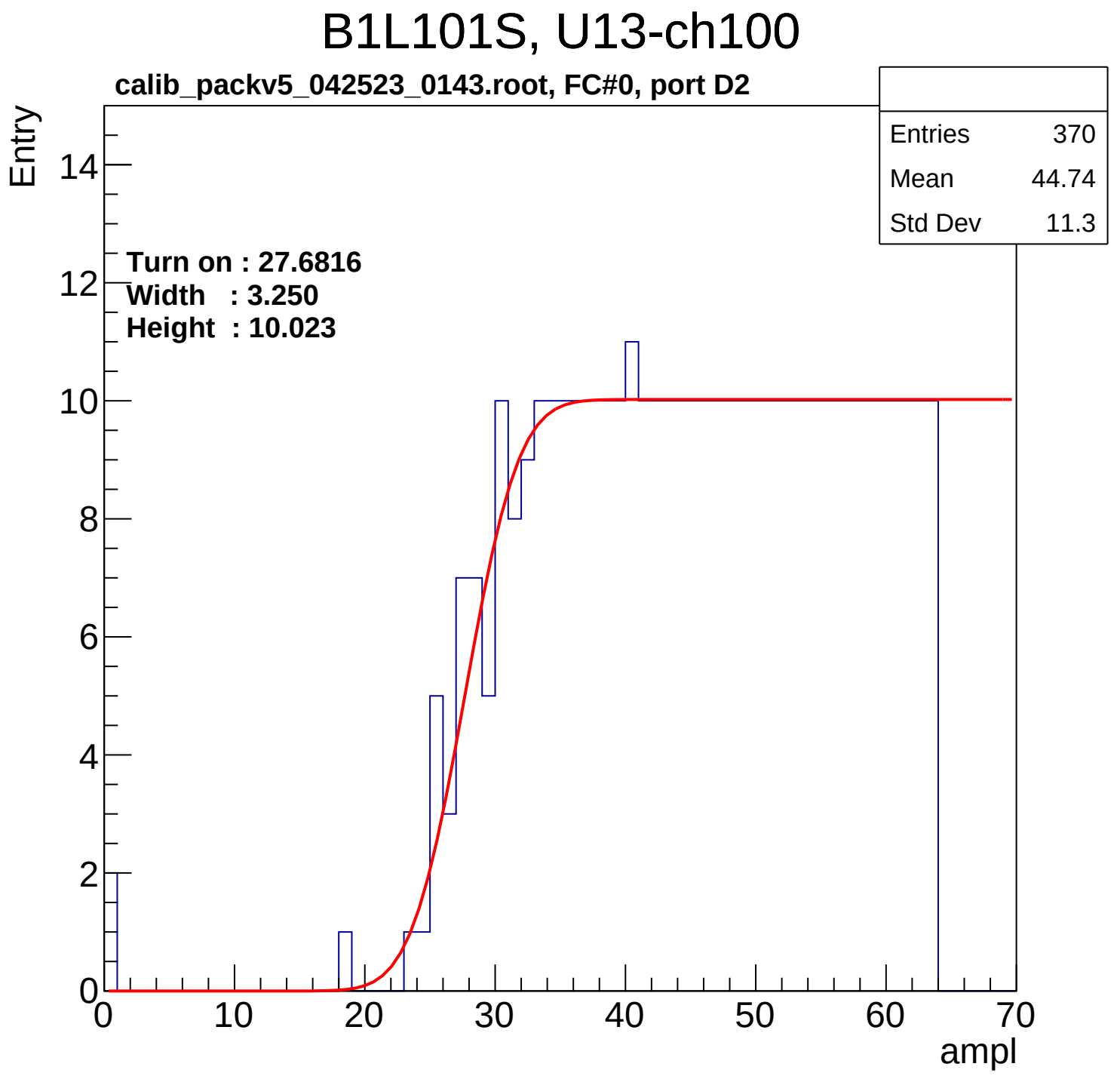
B1L101S, U13-ch100
calib_packv5_042523_0143.root, FC#0, port D2
Entries 370
Mean 44.74
Std Dev 11.3
Turn on : 27.6816
Width : 3.250
Height : 10.023
Entry
ampl
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6
8
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0
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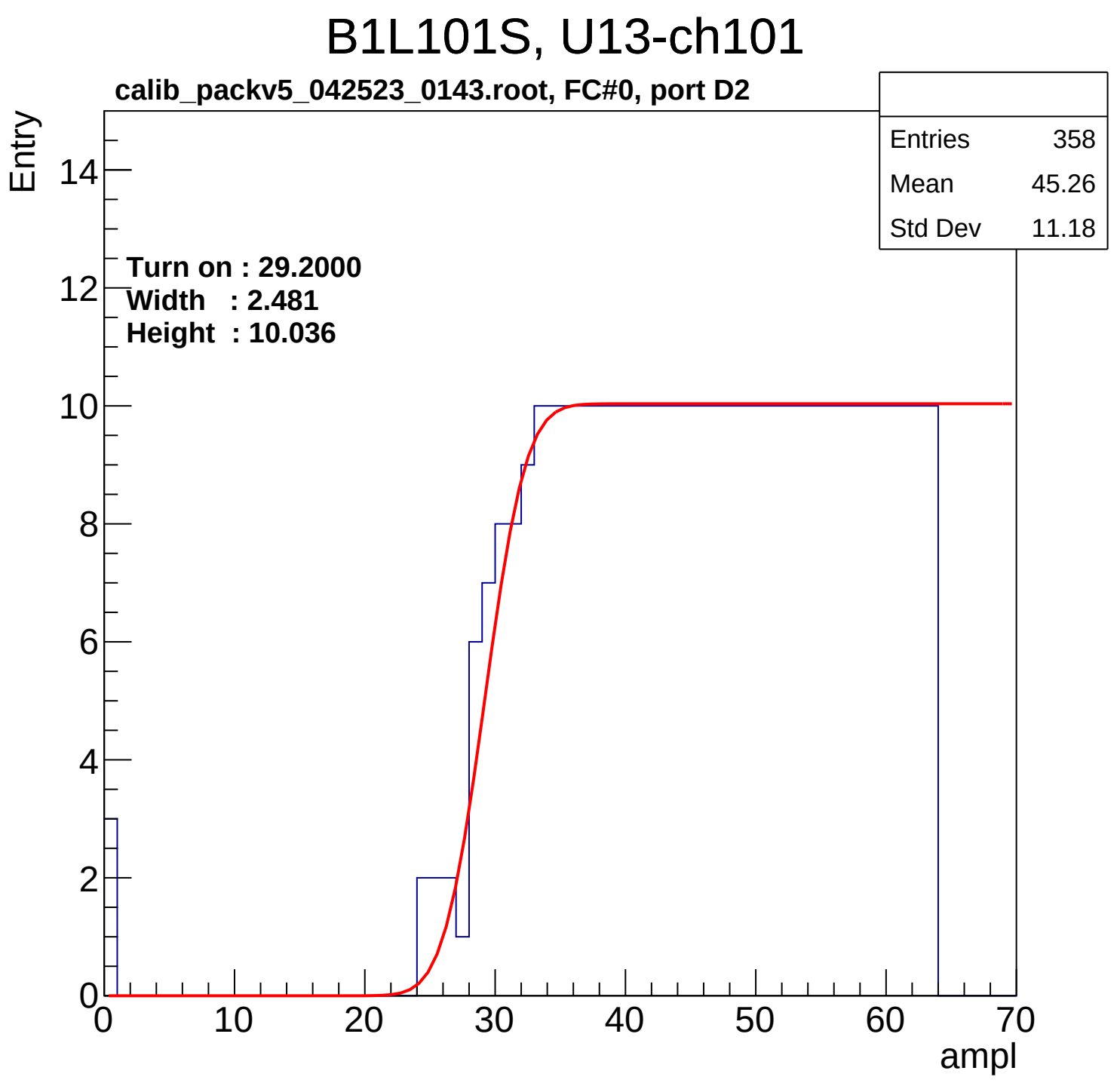
B1L101S, U13-ch101
calib_packv5_042523_0143.root, FC#0, port D2
Entries 358
Mean 45.26
Std Dev 11.18
Turn on : 29.2000
Width : 2.481
Height : 10.036
Entry
ampl
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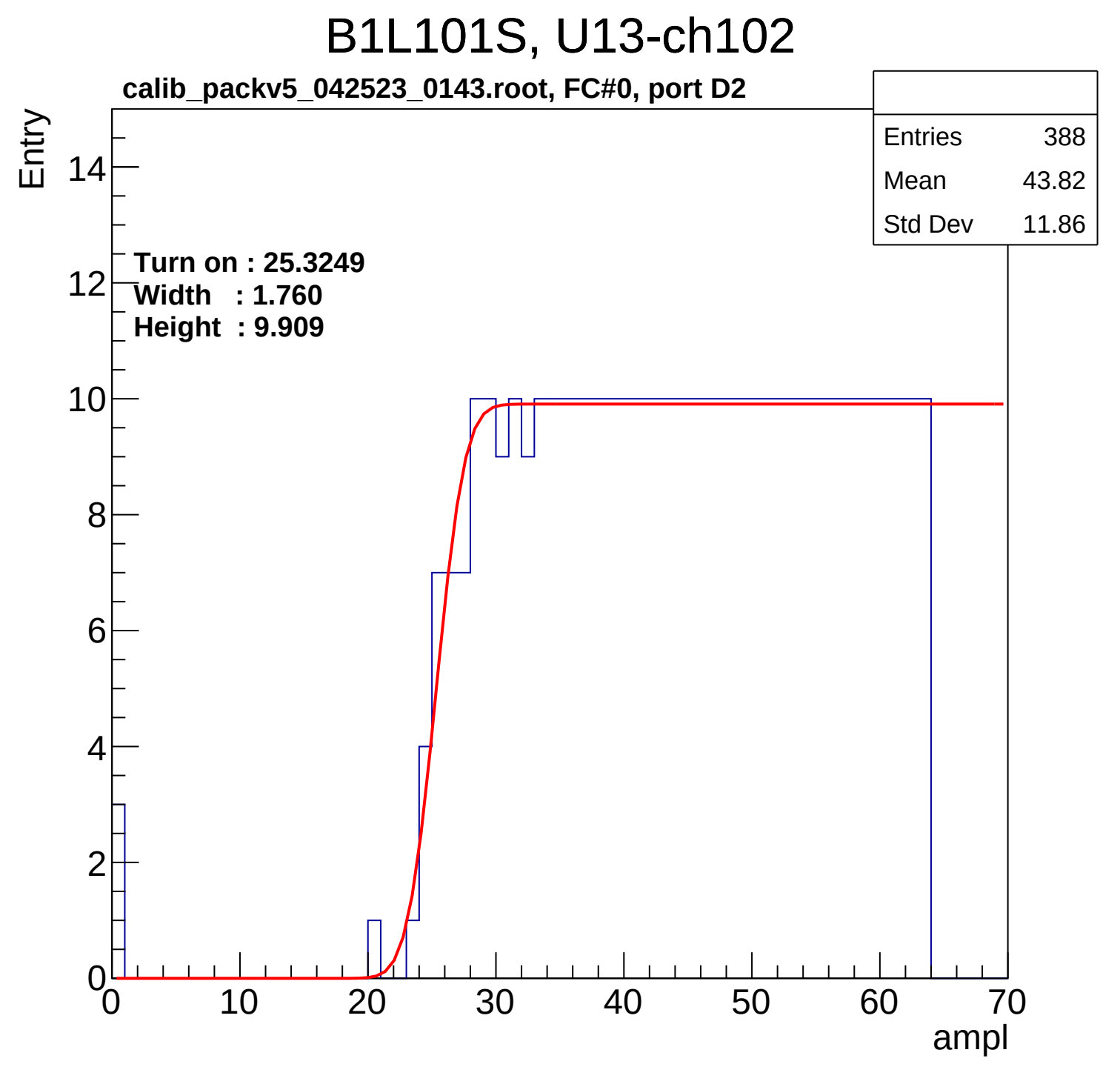
B1L101S, U13-ch102
calib_packv5_042523_0143.root, FC#0, port D2
Entries 388
Mean 43.82
Std Dev 11.86
Turn on : 25.3249
Width : 1.760
Height : 9.909
Entry
ampl
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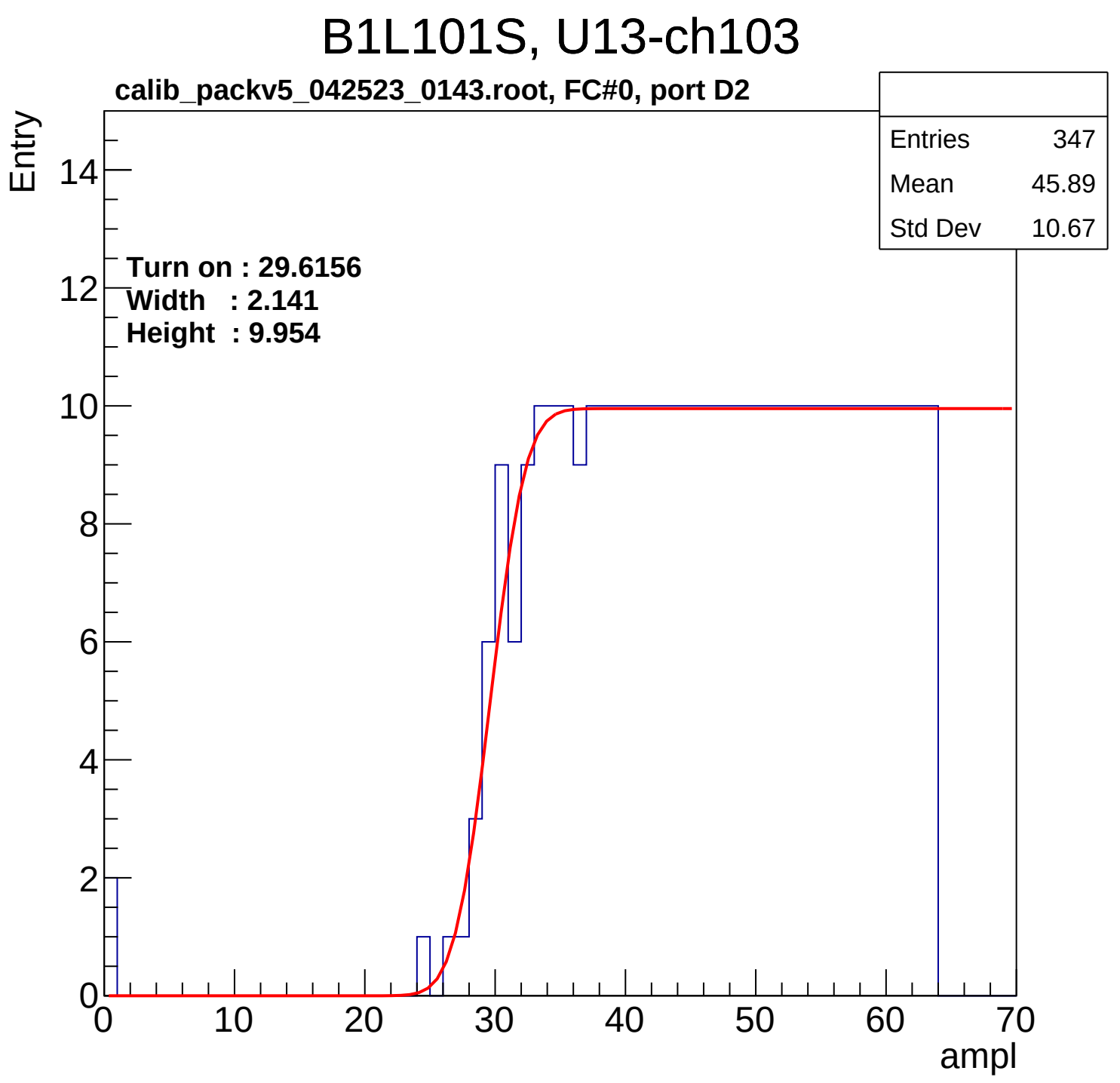
B1L101S, U13-ch103
calib_packv5_042523_0143.root, FC#0, port D2
Entries 347
Mean 45.89
Std Dev 10.67
Turn on : 29.6156
Width : 2.141
Height : 9.954
Entry
ampl
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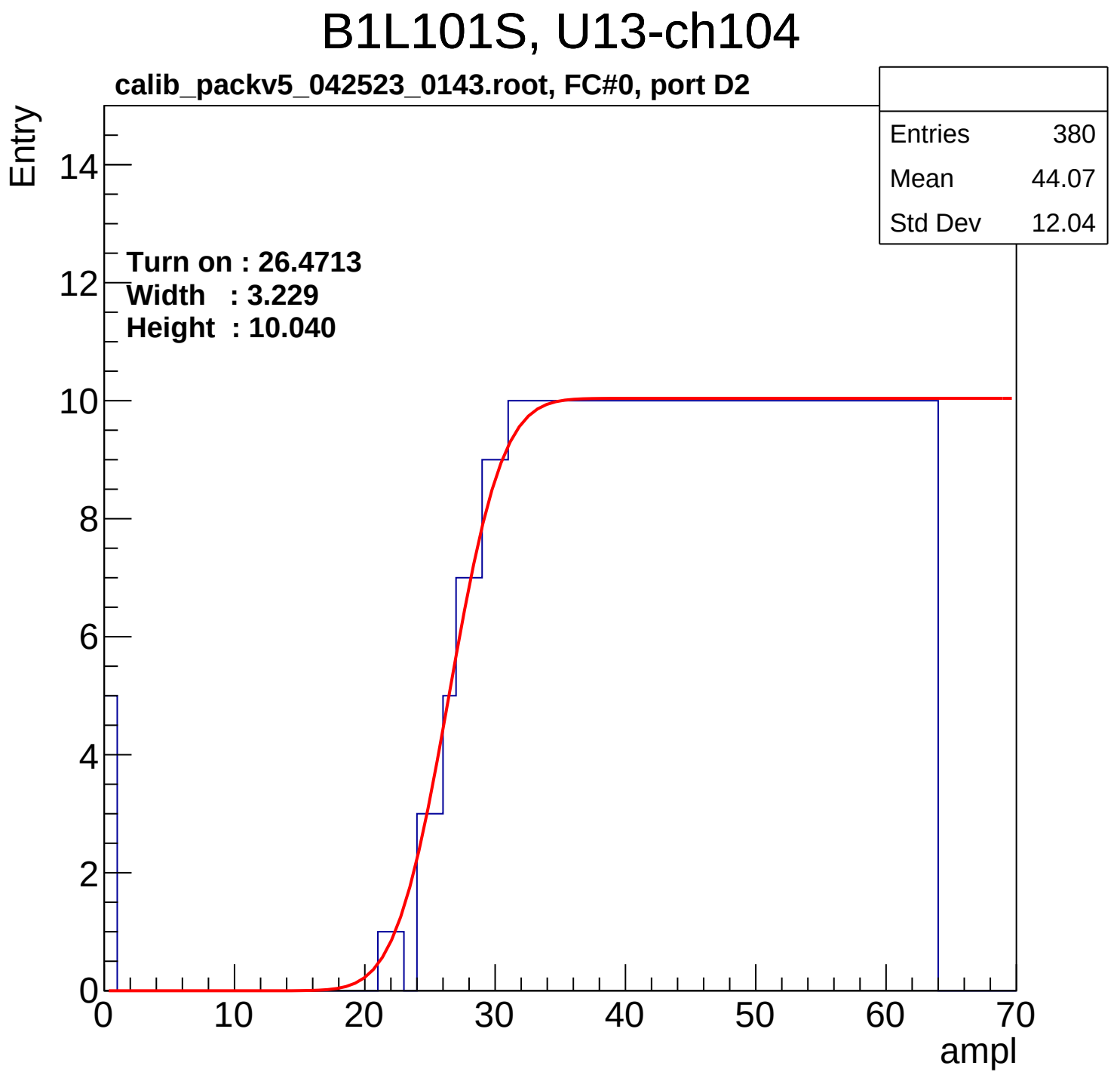
B1L101S, U13-ch104
calib_packv5_042523_0143.root, FC#0, port D2
Entries 380
Mean 44.07
Std Dev 12.04
Turn on : 26.4713
Width : 3.229
Height : 10.040
Entry
ampl
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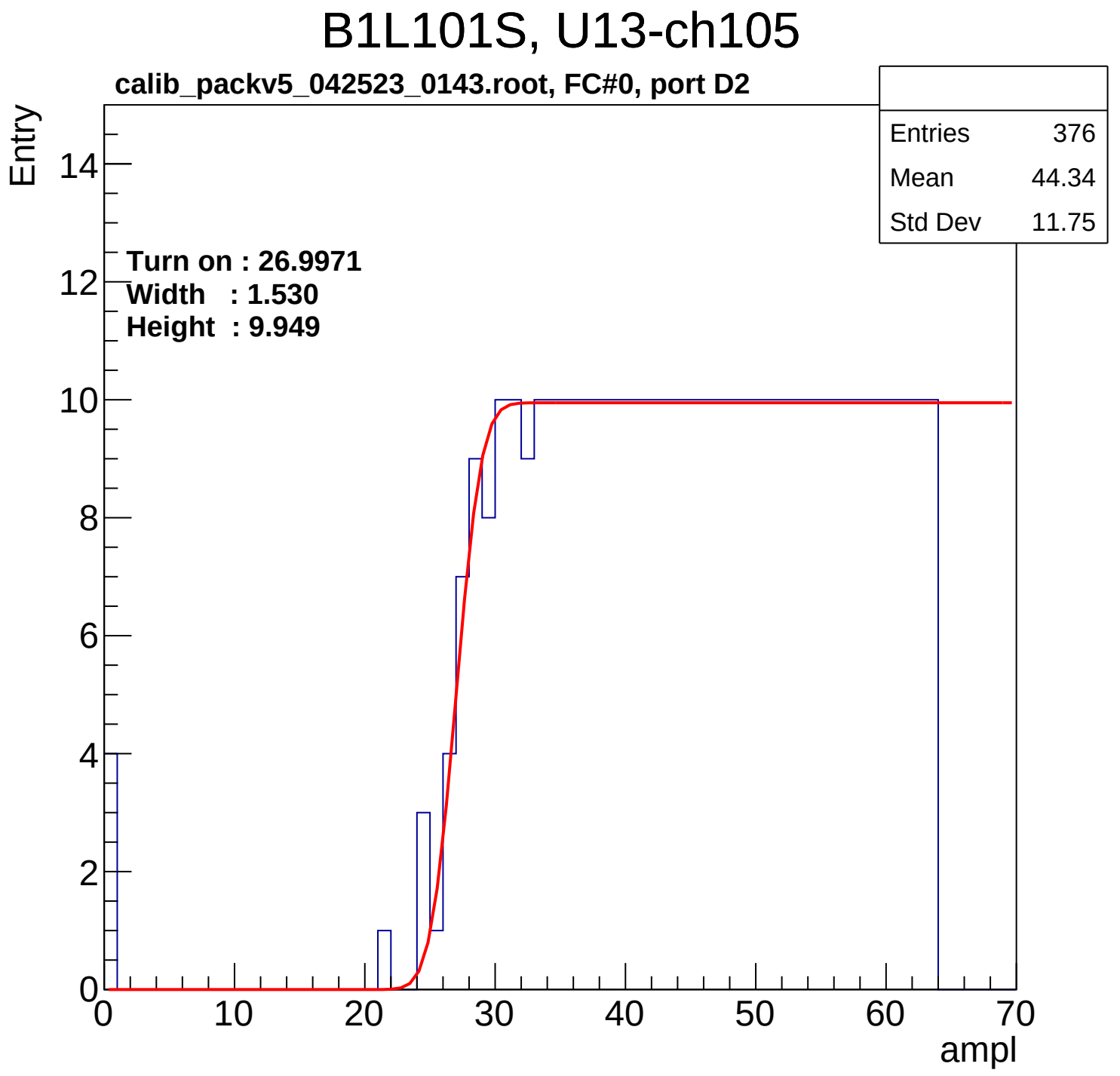
B1L101S, U13-ch105
calib_packv5_042523_0143.root, FC#0, port D2
Entries 376
Mean 44.34
Std Dev 11.75
Turn on : 26.9971
Width : 1.530
Height : 9.949
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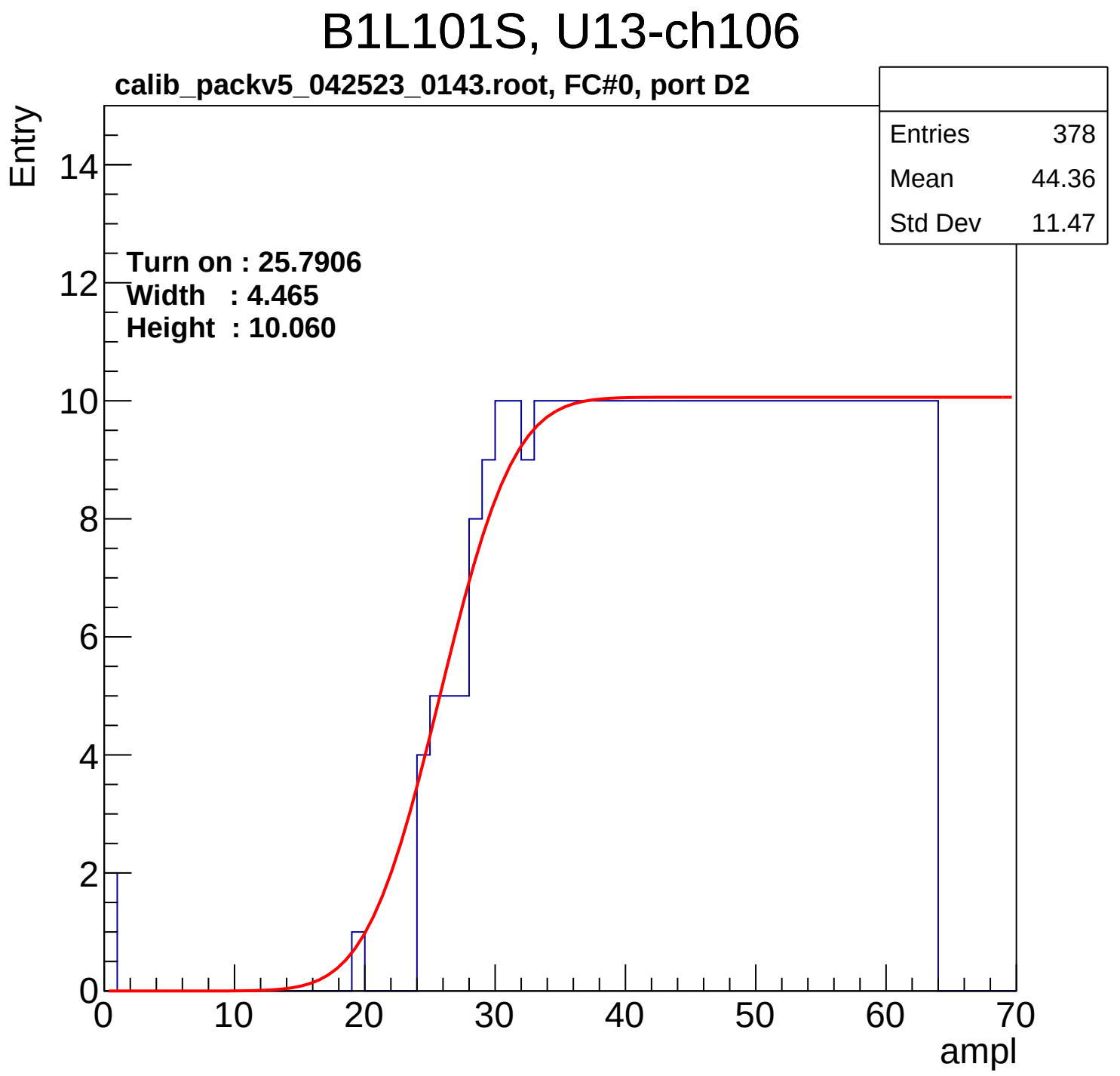
B1L101S, U13-ch106
calib_packv5_042523_0143.root, FC#0, port D2
Entries 378
Mean 44.36
Std Dev 11.47
Turn on : 25.7906
Width : 4.465
Height : 10.060
Entry
ampl
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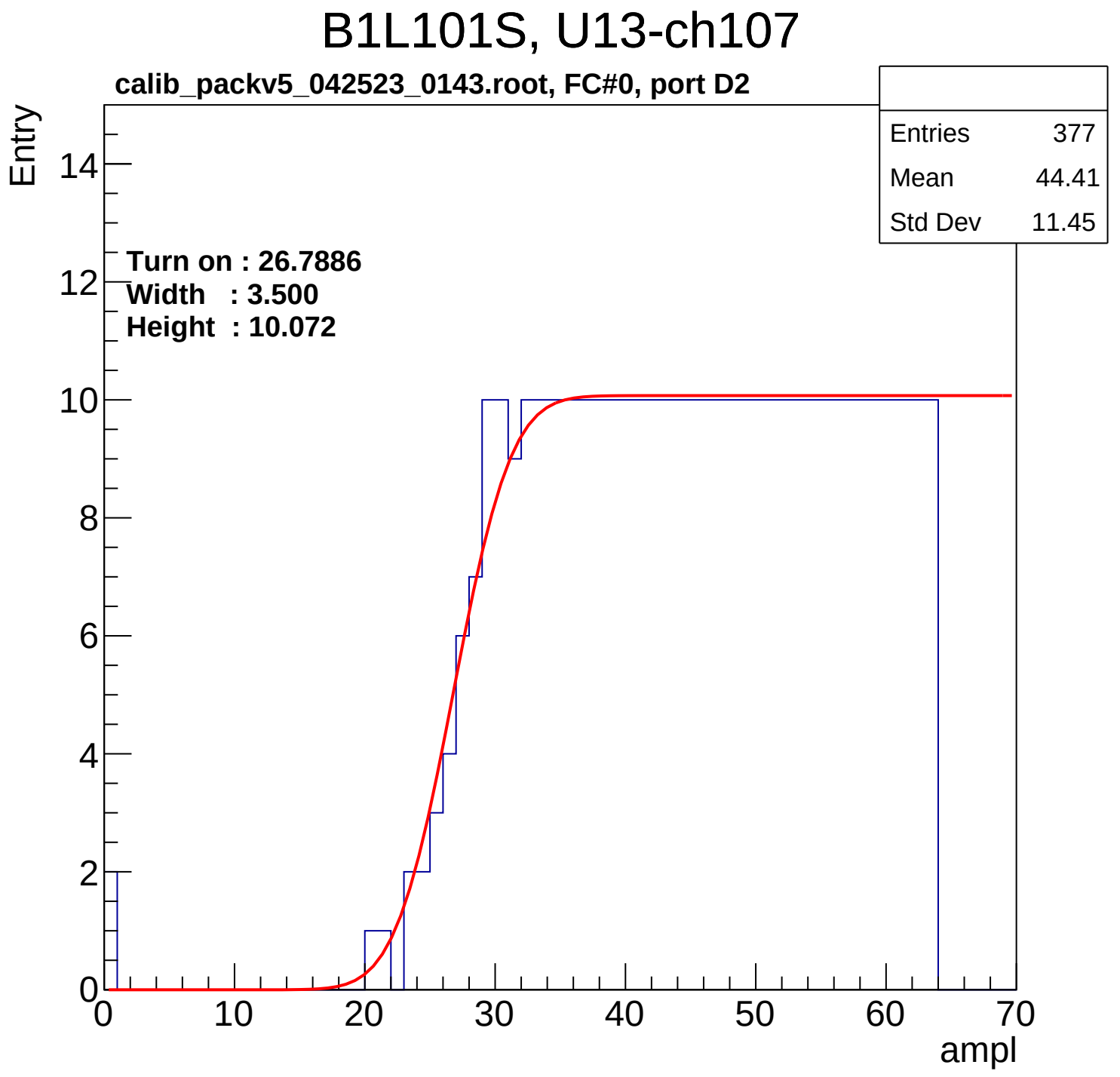
B1L101S, U13-ch107
calib_packv5_042523_0143.root, FC#0, port D2
Entries 377
Mean 44.41
Std Dev 11.45
Turn on : 26.7886
Width : 3.500
Height : 10.072
Entry
ampl
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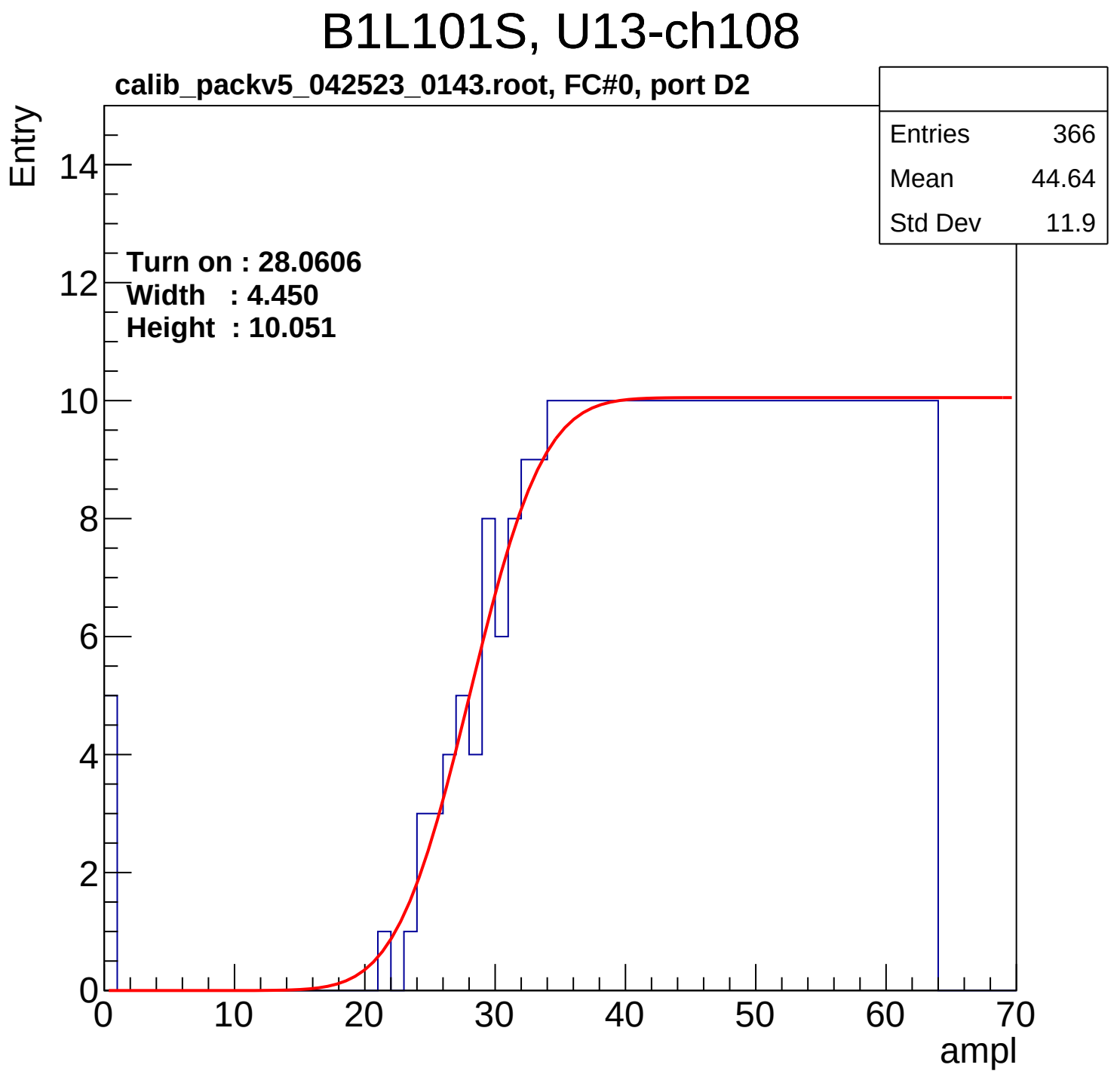
B1L101S, U13-ch108
calib_packv5_042523_0143.root, FC#0, port D2
Entries 366
Mean 44.64
Std Dev 11.9
Turn on : 28.0606
Width : 4.450
Height : 10.051
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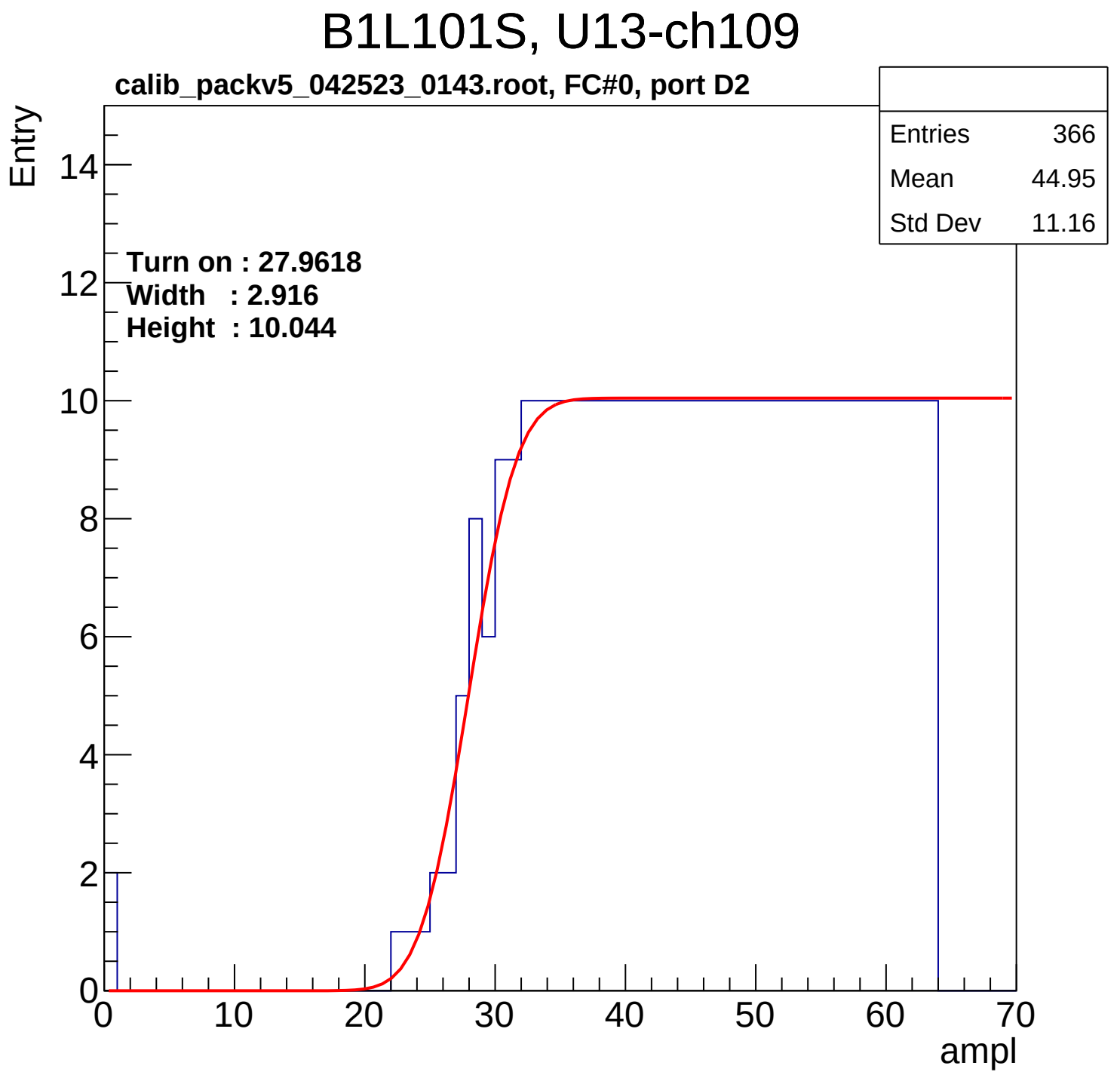
B1L101S, U13-ch109
calib_packv5_042523_0143.root, FC#0, port D2
Entries 366
Mean 44.95
Std Dev 11.16
Turn on : 27.9618
Width : 2.916
Height : 10.044
Entry
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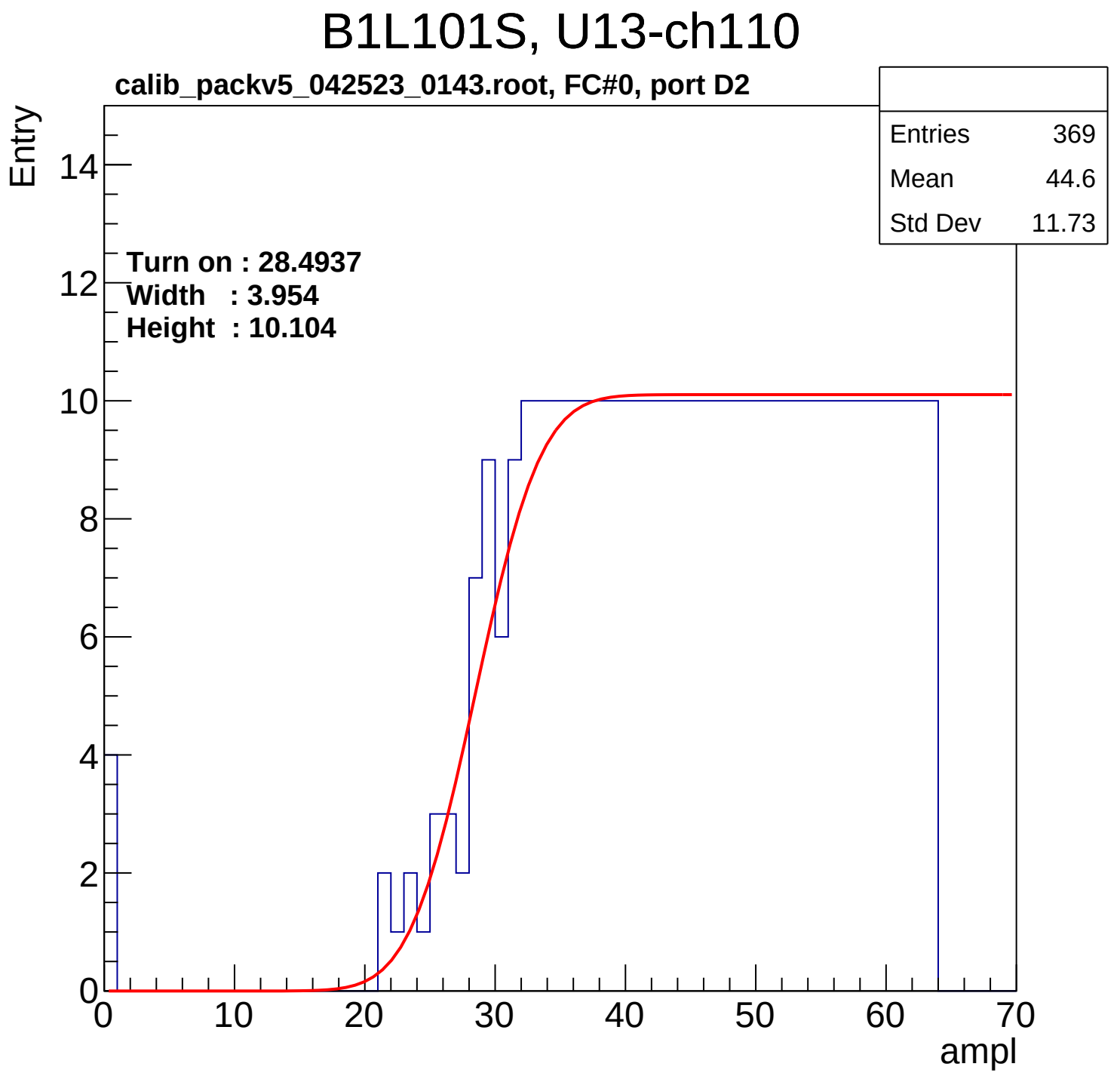
B1L101S, U13-ch110
calib_packv5_042523_0143.root, FC#0, port D2
Entries 369
Mean 44.6
Std Dev 11.73
Turn on : 28.4937
Width : 3.954
Height : 10.104
Entry
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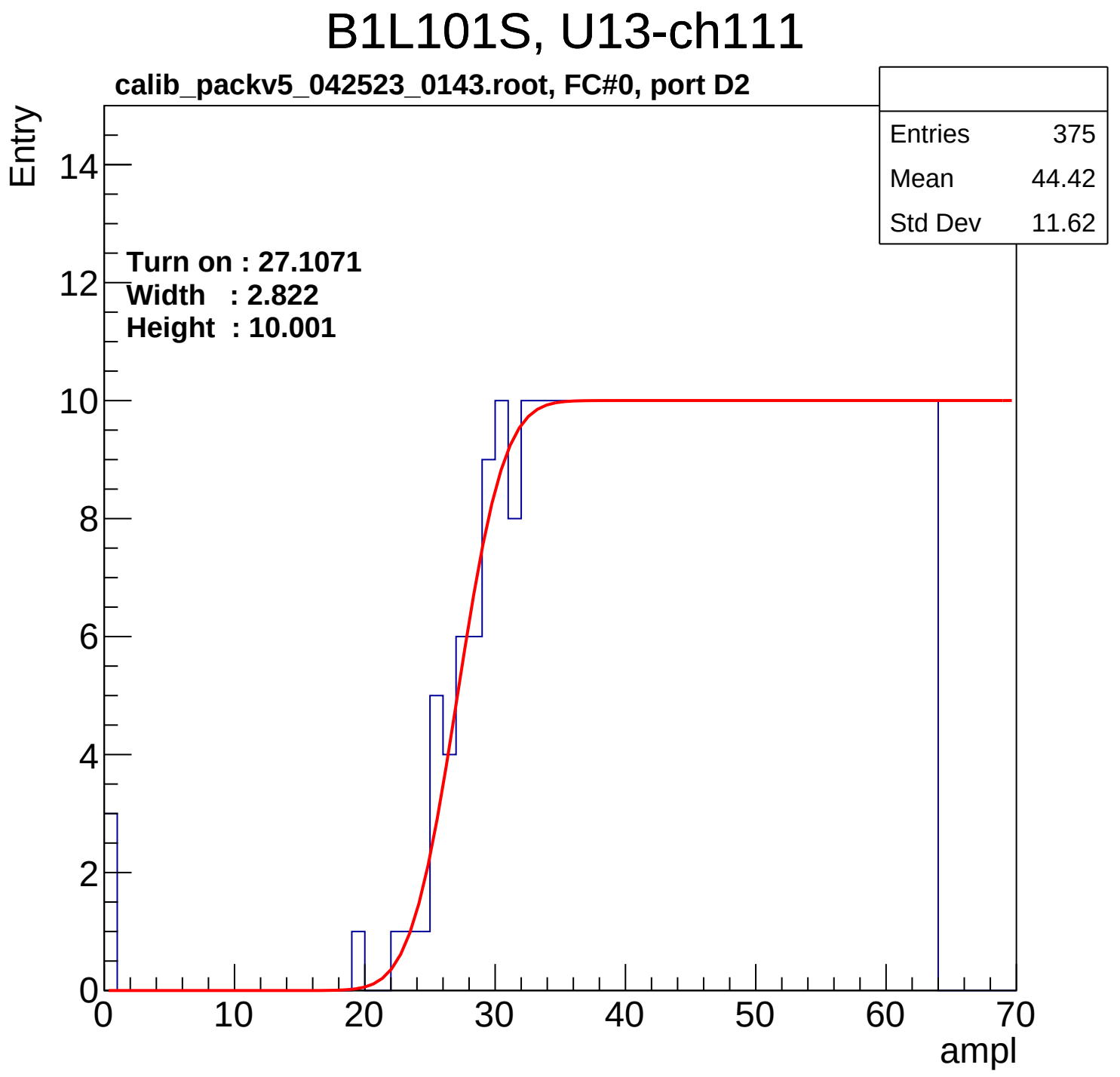
B1L101S, U13-ch111
calib_packv5_042523_0143.root, FC#0, port D2
Entries 375
Mean 44.42
Std Dev 11.62
Turn on : 27.1071
Width : 2.822
Height : 10.001
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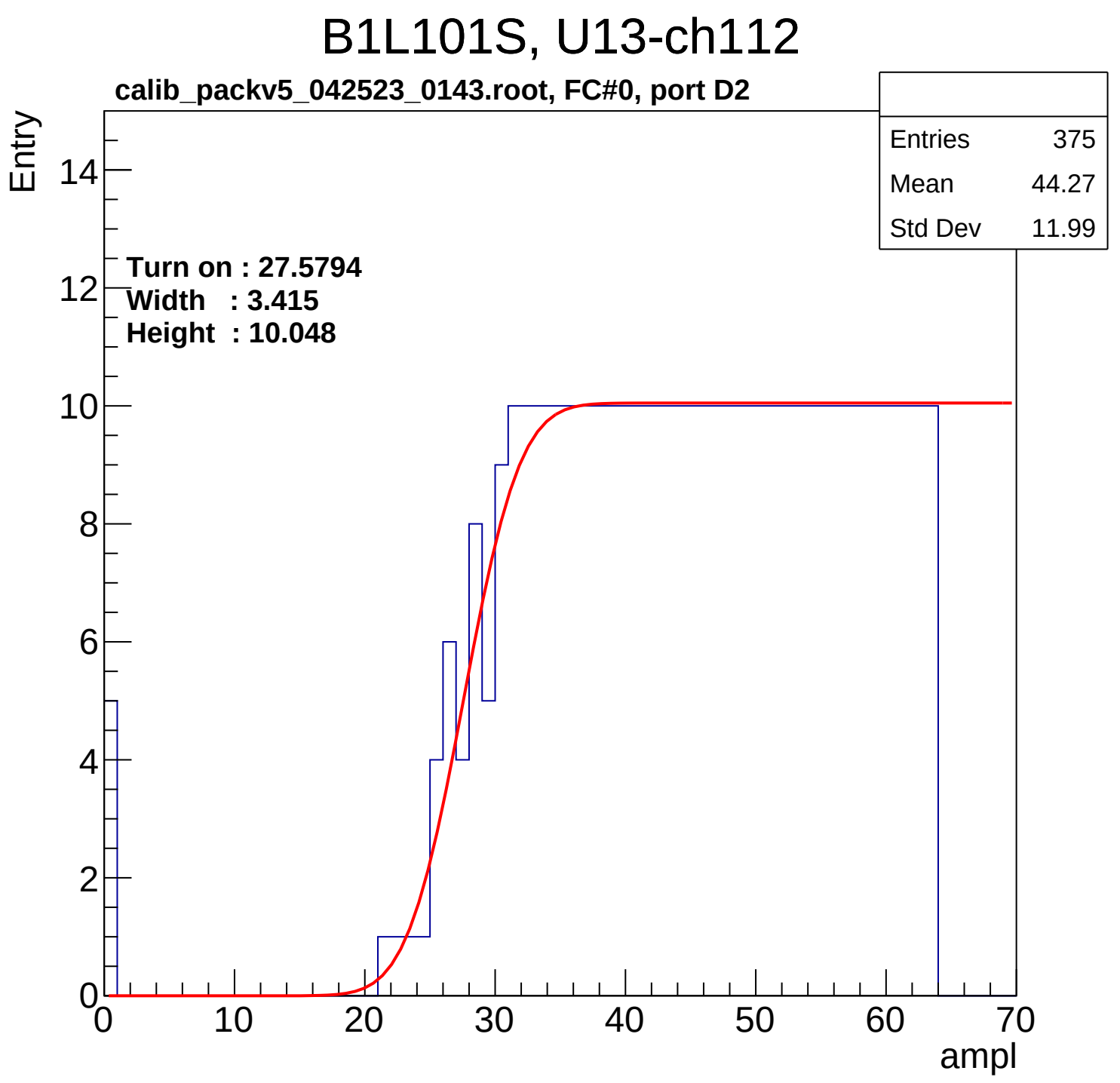
B1L101S, U13-ch112
calib_packv5_042523_0143.root, FC#0, port D2
Entries 375
Mean 44.27
Std Dev 11.99
Turn on : 27.5794
Width : 3.415
Height : 10.048
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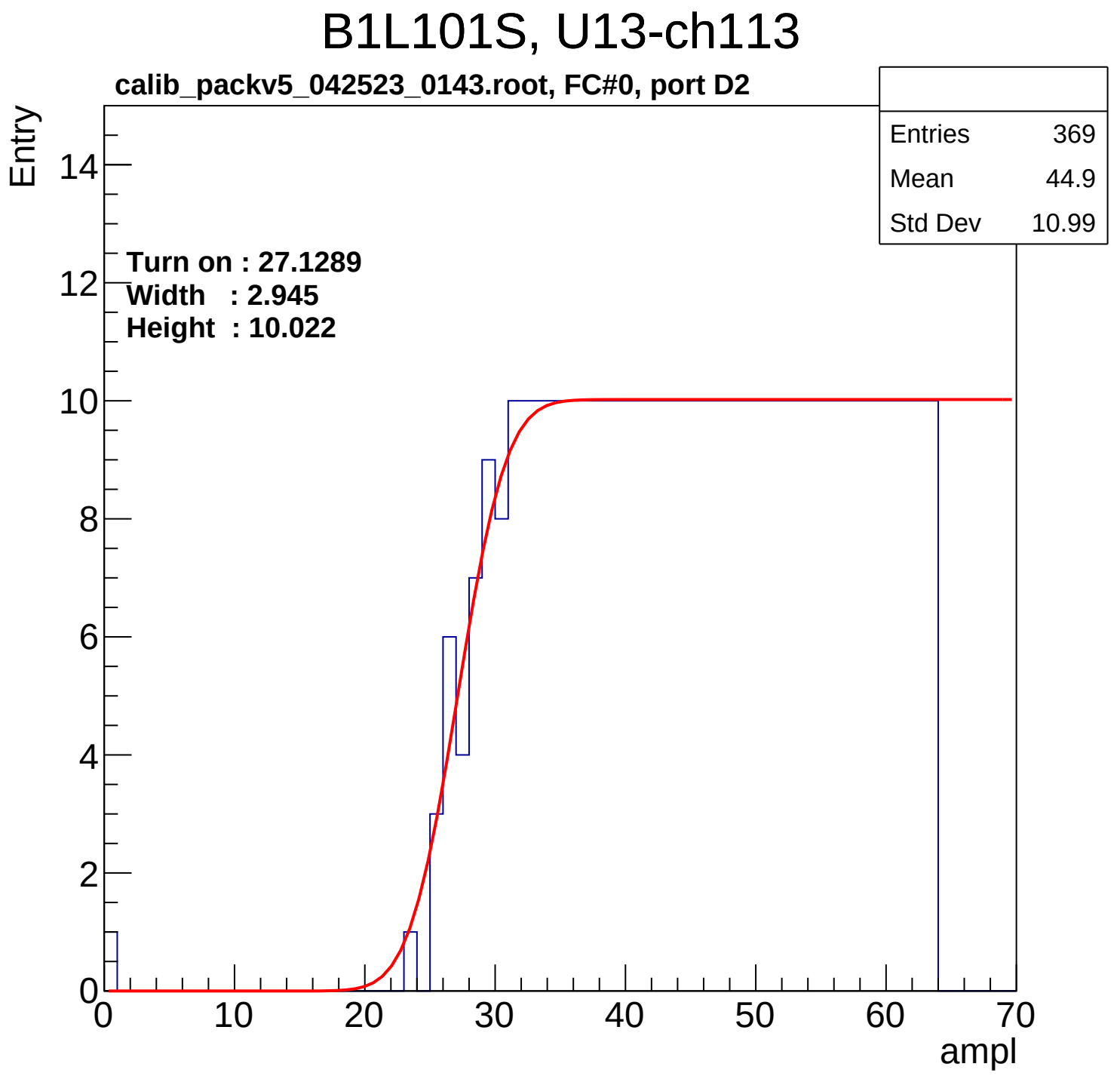
B1L101S, U13-ch113
calib_packv5_042523_0143.root, FC#0, port D2
Entries 369
Mean 44.9
Std Dev 10.99
Turn on : 27.1289
Width : 2.945
Height : 10.022
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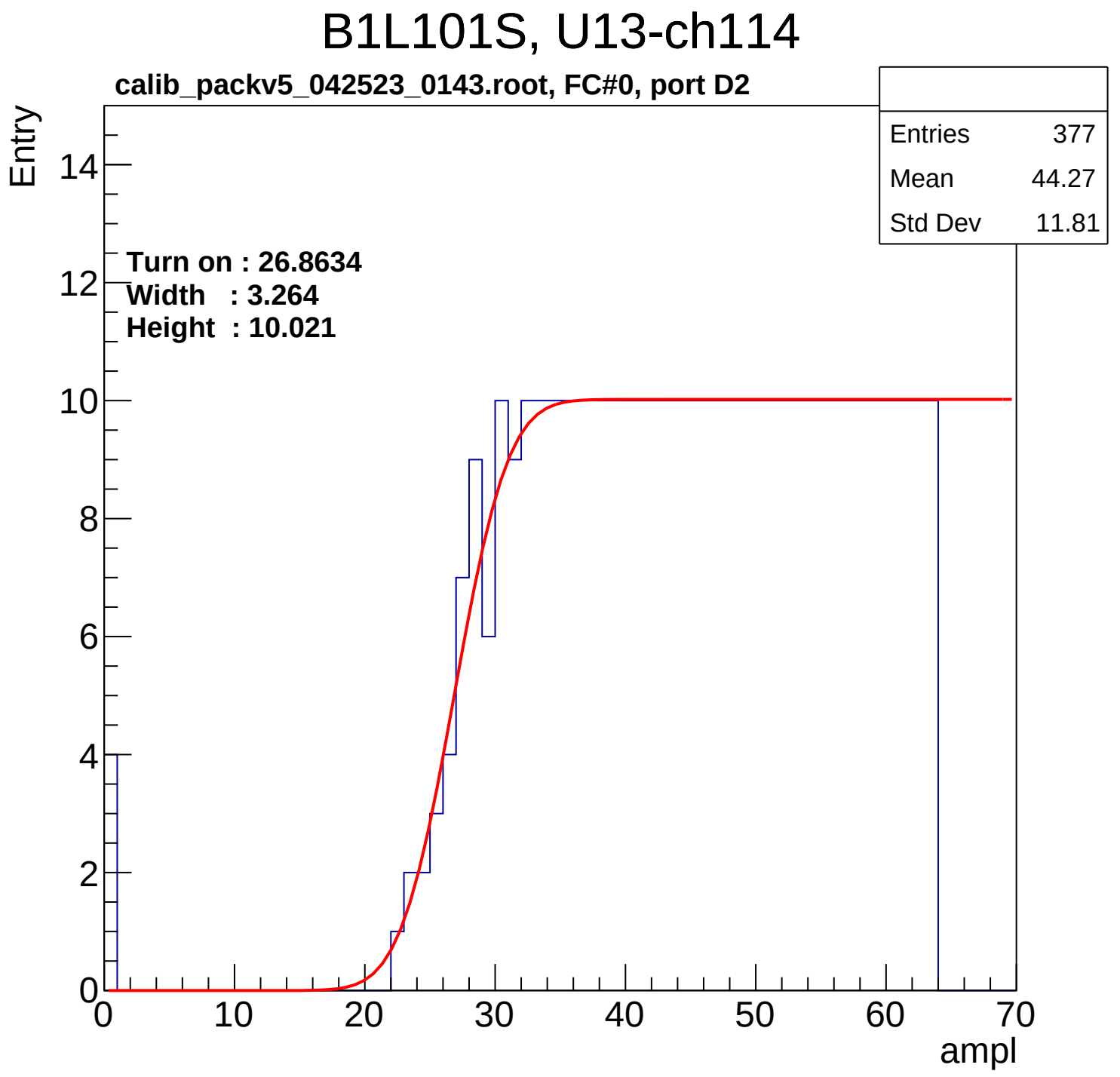
B1L101S, U13-ch114
calib_packv5_042523_0143.root, FC#0, port D2
Entries 377
Mean 44.27
Std Dev 11.81
Turn on : 26.8634
Width : 3.264
Height : 10.021
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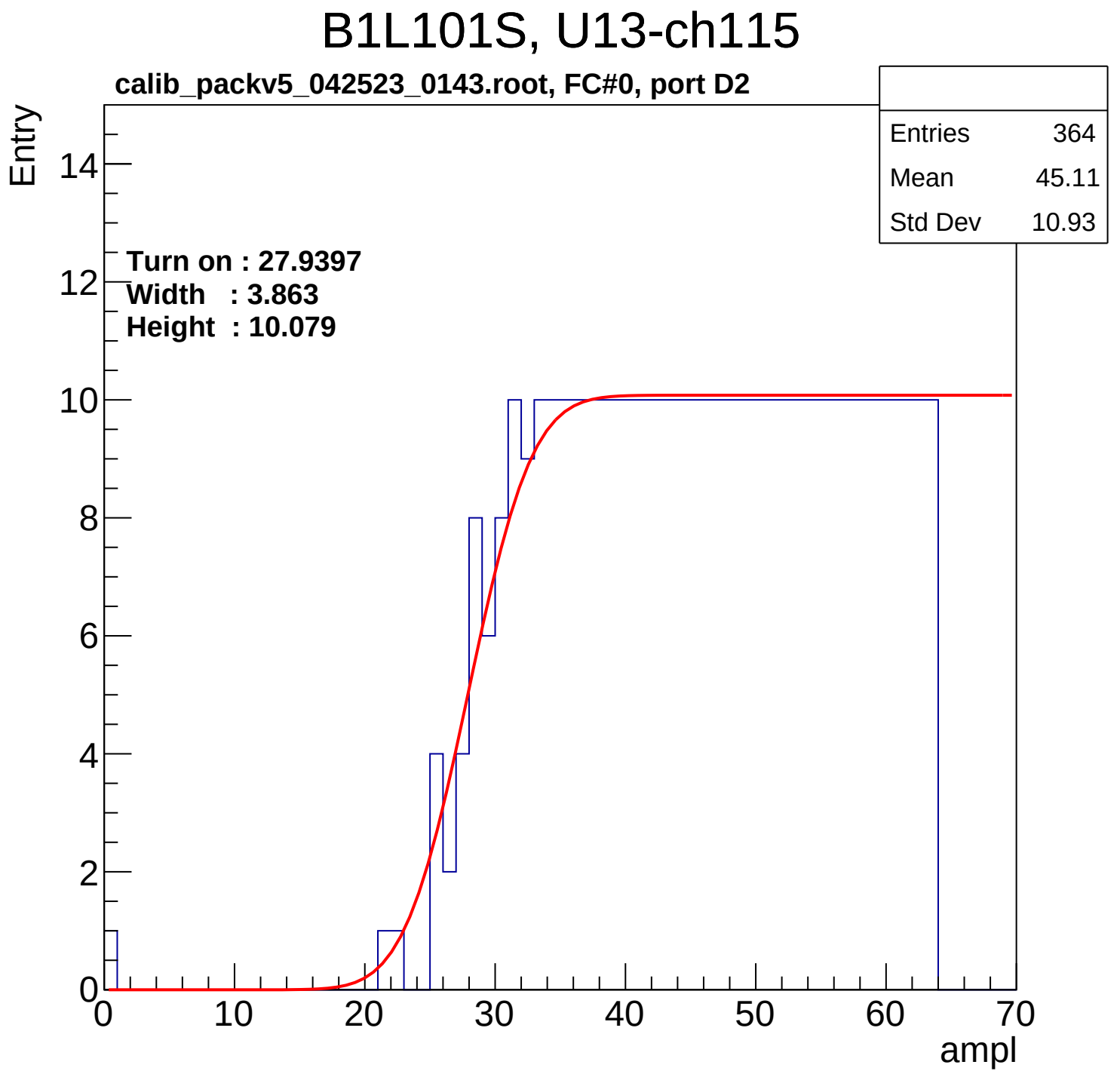
B1L101S, U13-ch115
calib_packv5_042523_0143.root, FC#0, port D2
Entries 364
Mean 45.11
Std Dev 10.93
Turn on : 27.9397
Width : 3.863
Height : 10.079
Entry
ampl
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4
6
8
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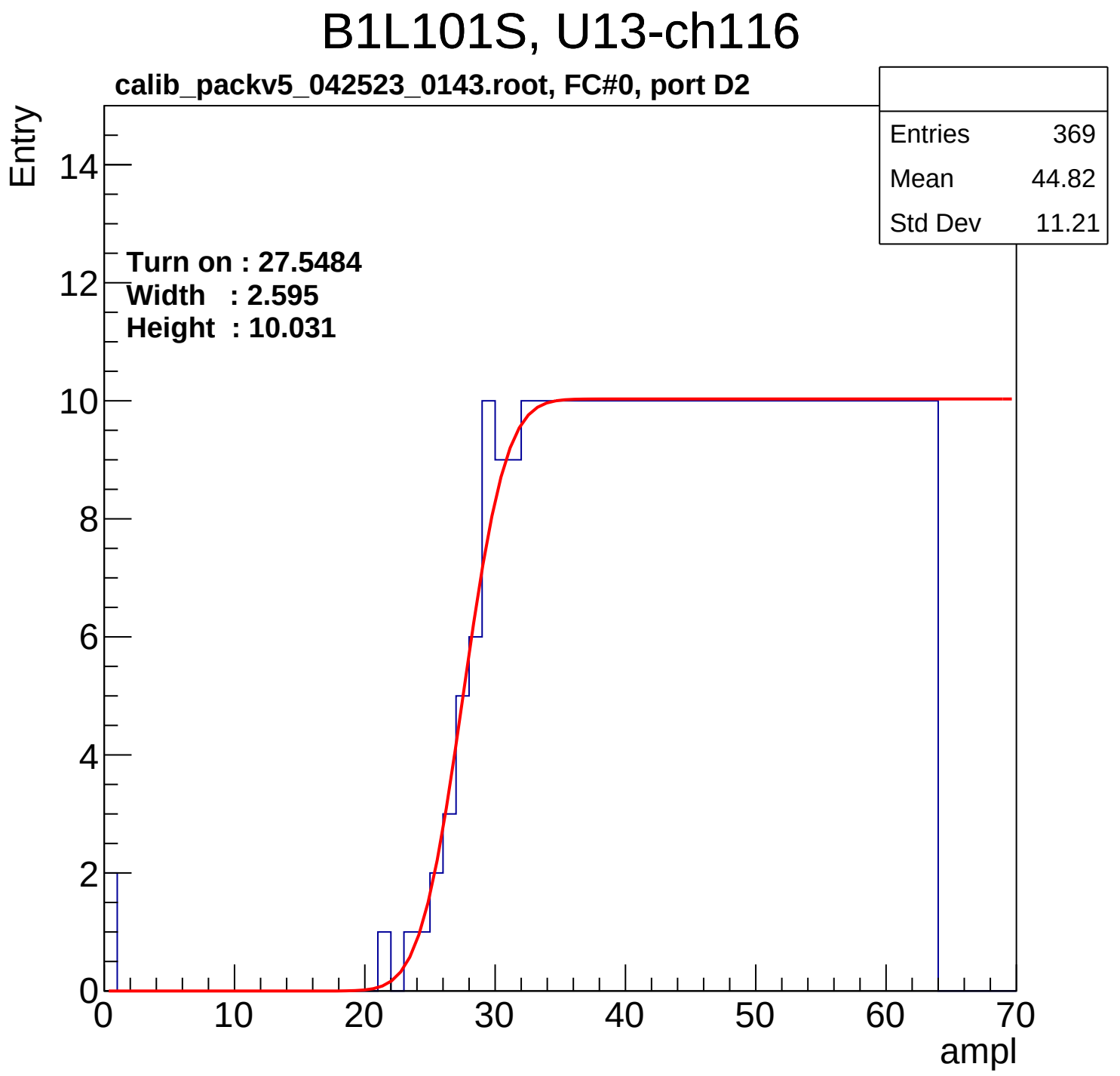
B1L101S, U13-ch116
calib_packv5_042523_0143.root, FC#0, port D2
Entries 369
Mean 44.82
Std Dev 11.21
Turn on : 27.5484
Width : 2.595
Height : 10.031
Entry
ampl
0
2
4
6
8
10
12
14
0
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20
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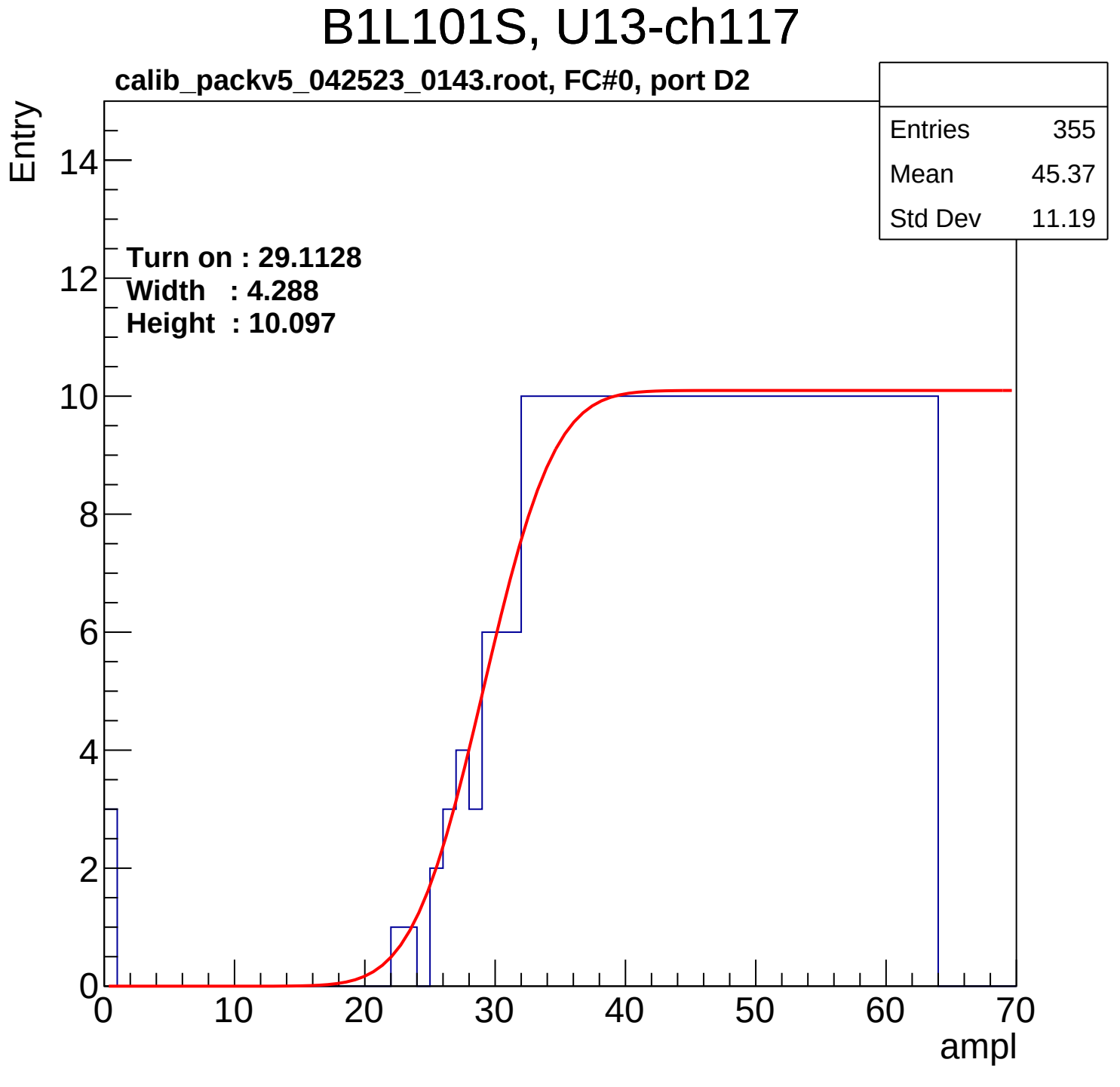
B1L101S, U13-ch117
calib_packv5_042523_0143.root, FC#0, port D2
Entries 355
Mean 45.37
Std Dev 11.19
Turn on : 29.1128
Width : 4.288
Height : 10.097
Entry
ampl
0
2
4
6
8
10
12
14
0
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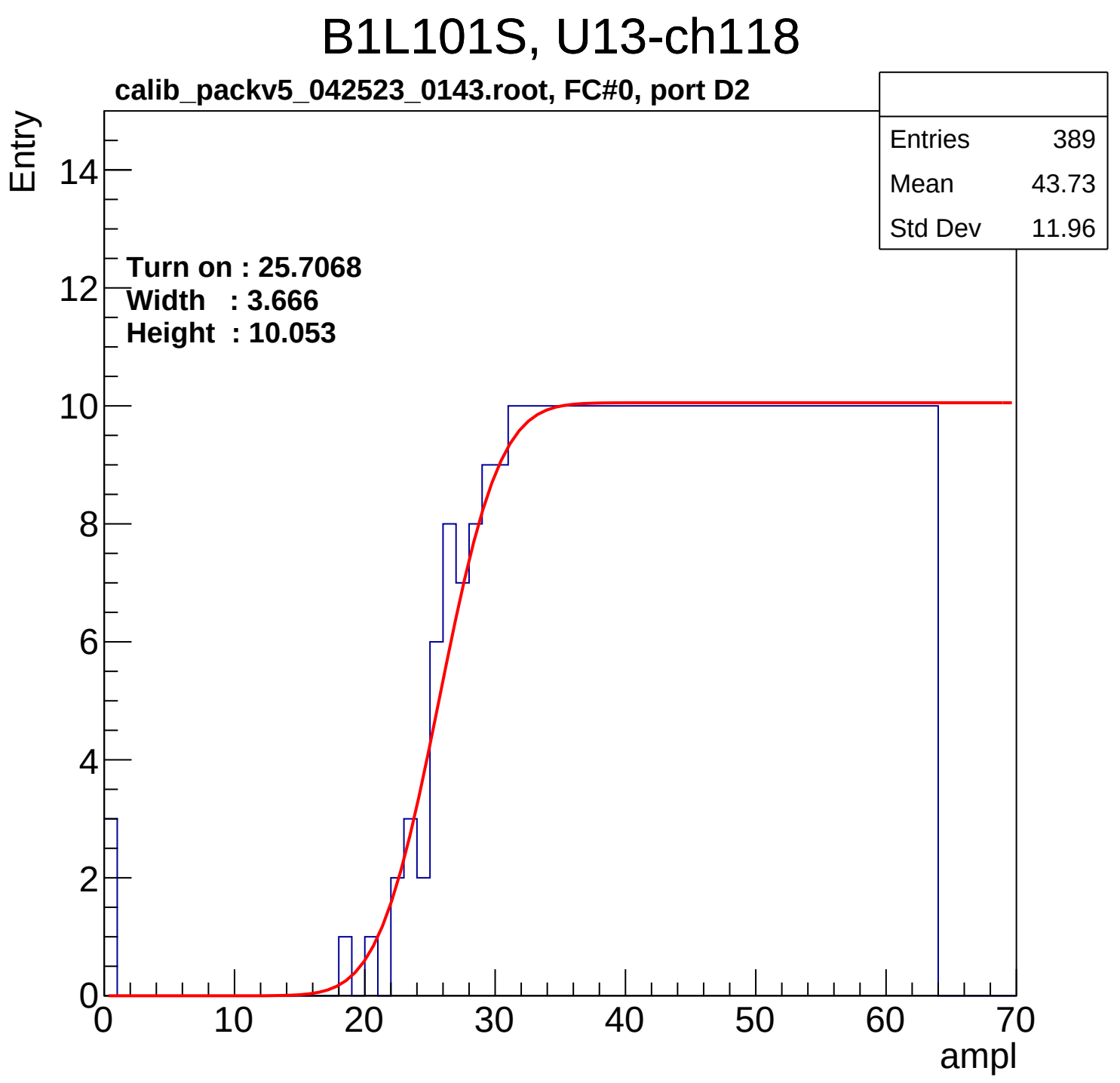
B1L101S, U13-ch118
calib_packv5_042523_0143.root, FC#0, port D2
Entries 389
Mean 43.73
Std Dev 11.96
Turn on : 25.7068
Width : 3.666
Height : 10.053
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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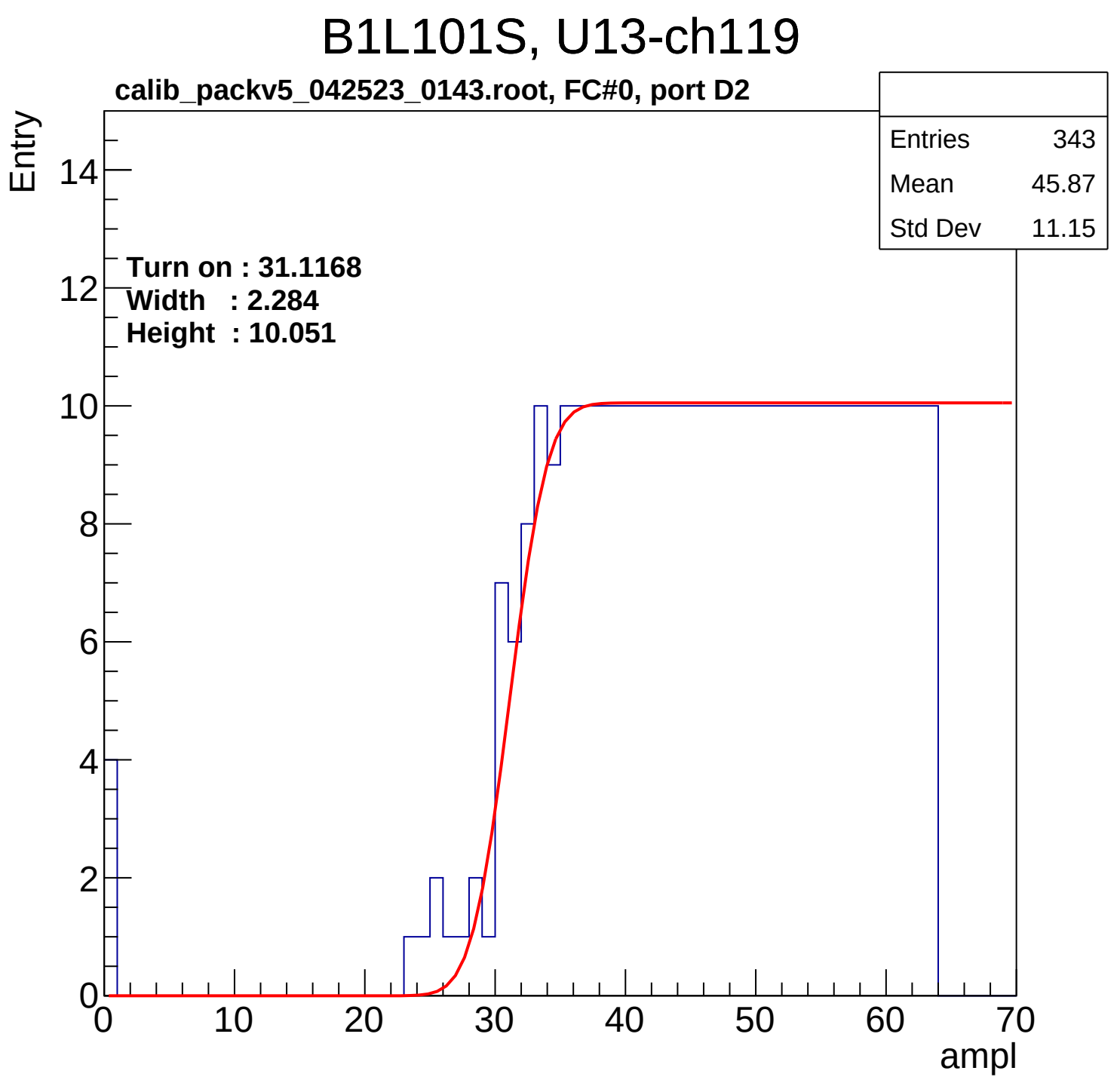
B1L101S, U13-ch119
calib_packv5_042523_0143.root, FC#0, port D2
Entries 343
Mean 45.87
Std Dev 11.15
Turn on : 31.1168
Width : 2.284
Height : 10.051
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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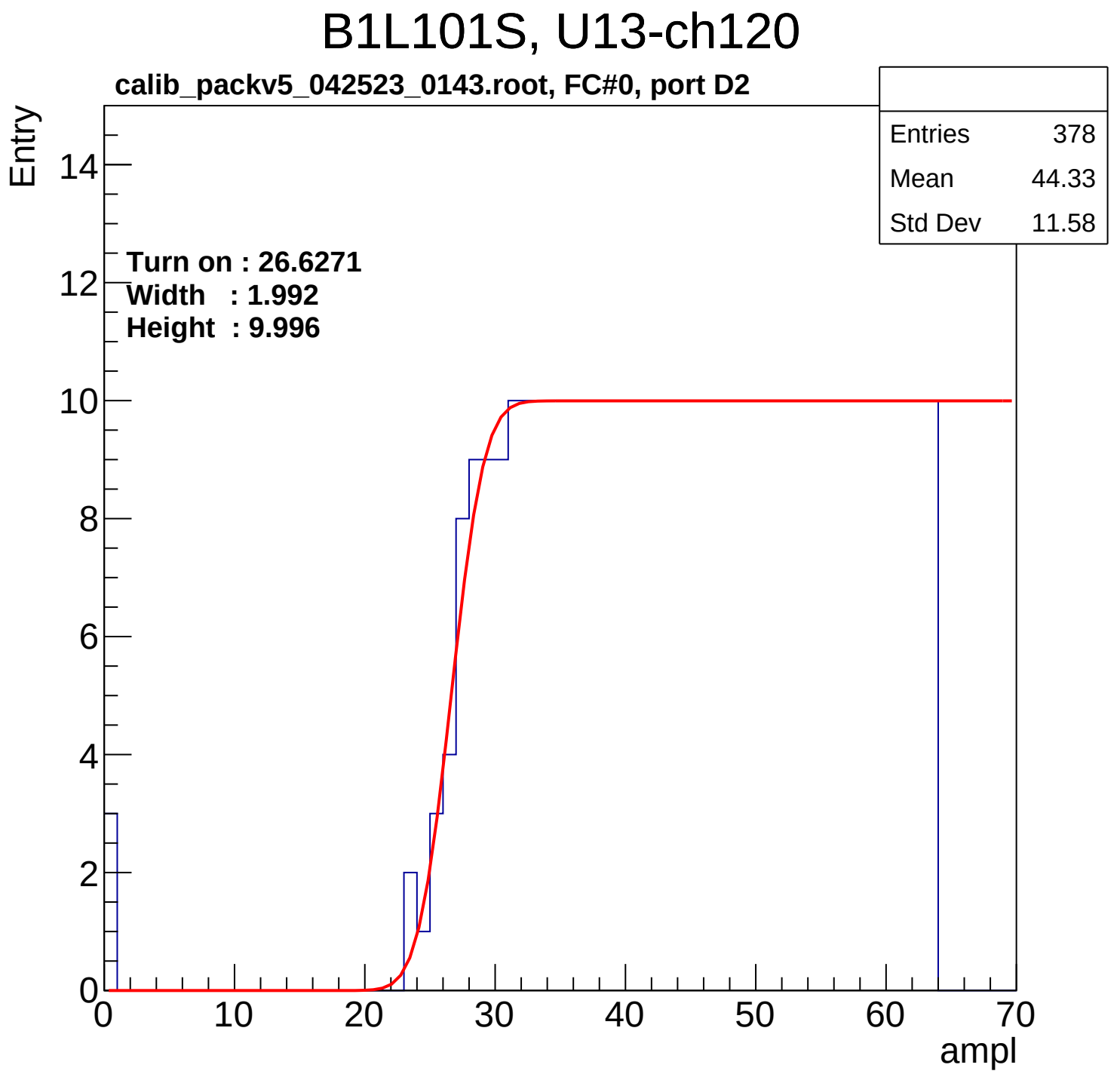
B1L101S, U13-ch120
calib_packv5_042523_0143.root, FC#0, port D2
Entries 378
Mean 44.33
Std Dev 11.58
Turn on : 26.6271
Width : 1.992
Height : 9.996
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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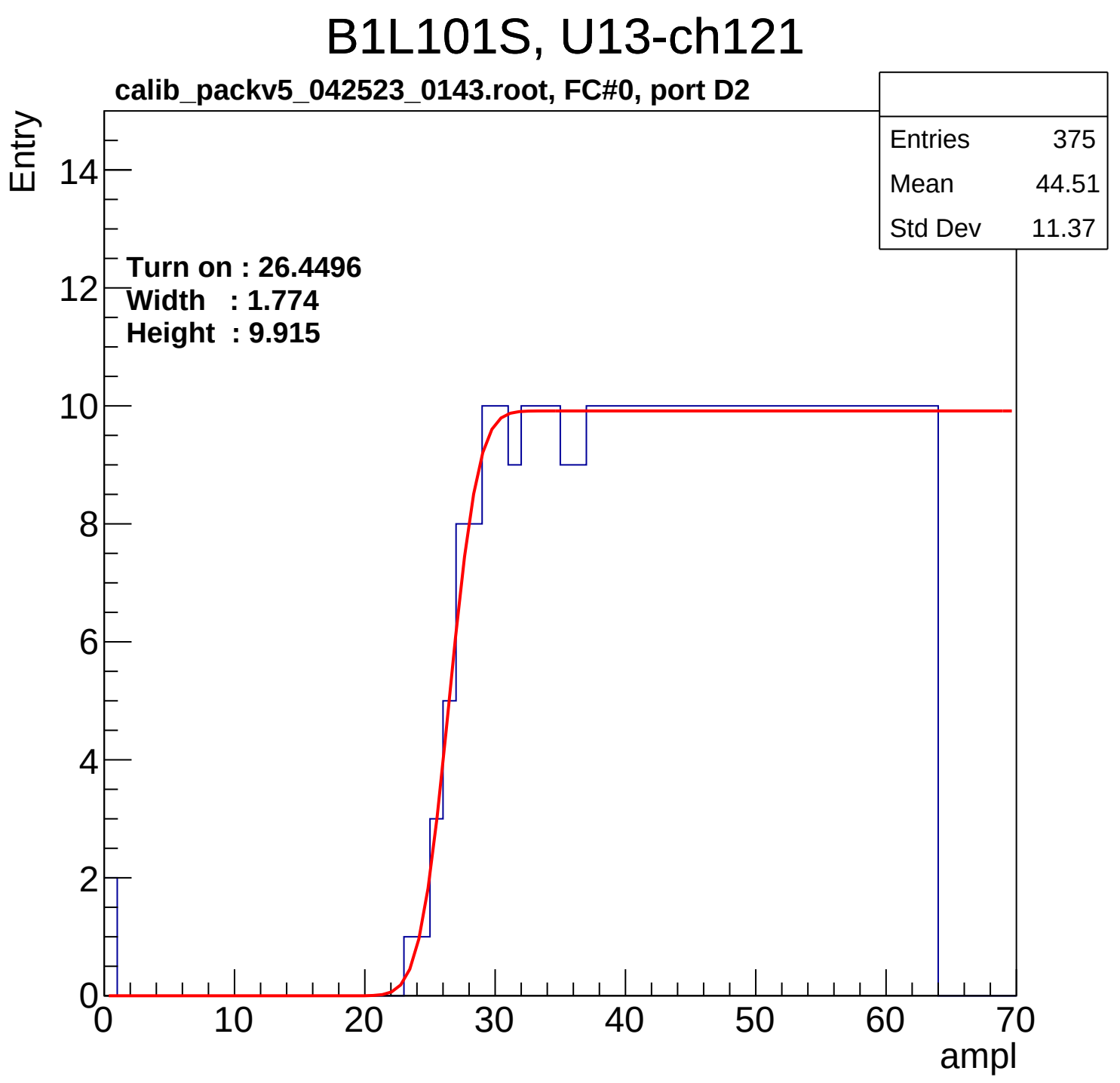
B1L101S, U13-ch121
calib_packv5_042523_0143.root, FC#0, port D2
Entries 375
Mean 44.51
Std Dev 11.37
Turn on : 26.4496
Width : 1.774
Height : 9.915
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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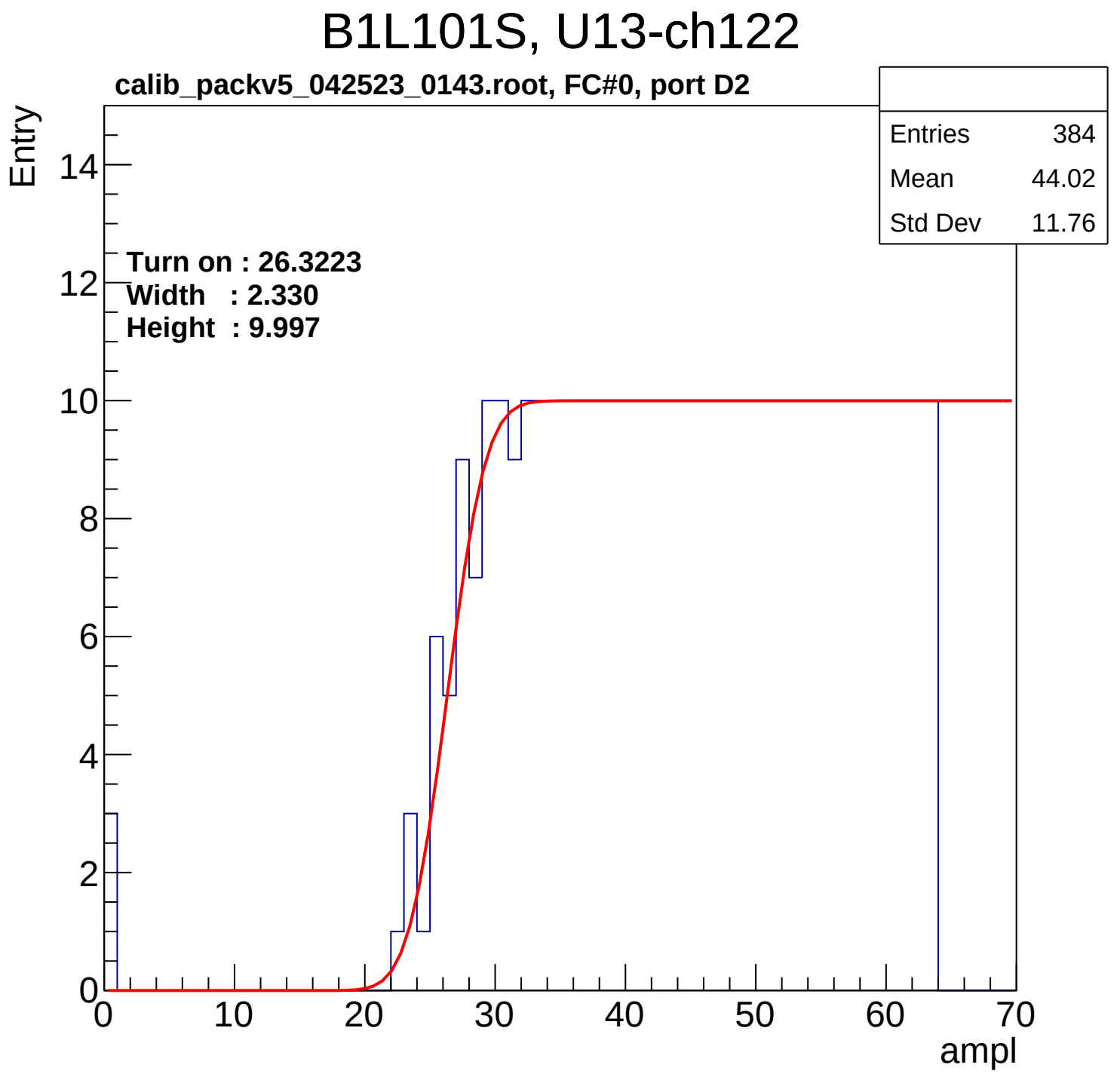
B1L101S, U13-ch122
calib_packv5_042523_0143.root, FC#0, port D2
Entries 384
Mean 44.02
Std Dev 11.76
Turn on : 26.3223
Width : 2.330
Height : 9.997
Entry
ampl
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2
4
6
8
10
12
14
0
10
20
30
40
50
60
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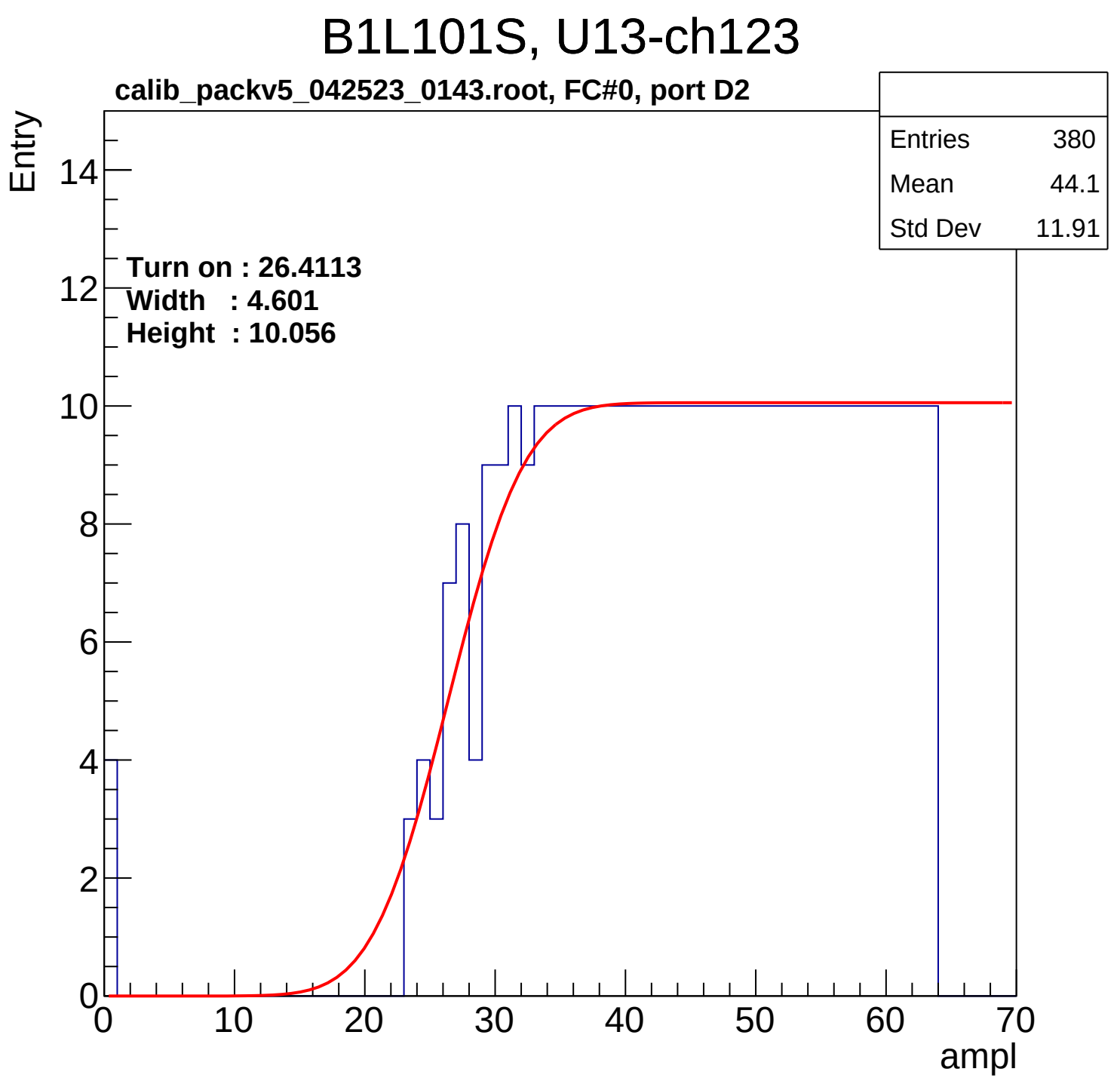
B1L101S, U13-ch123
calib_packv5_042523_0143.root, FC#0, port D2
Entries 380
Mean 44.1
Std Dev 11.91
Turn on : 26.4113
Width : 4.601
Height : 10.056
Entry
ampl
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2
4
6
8
10
12
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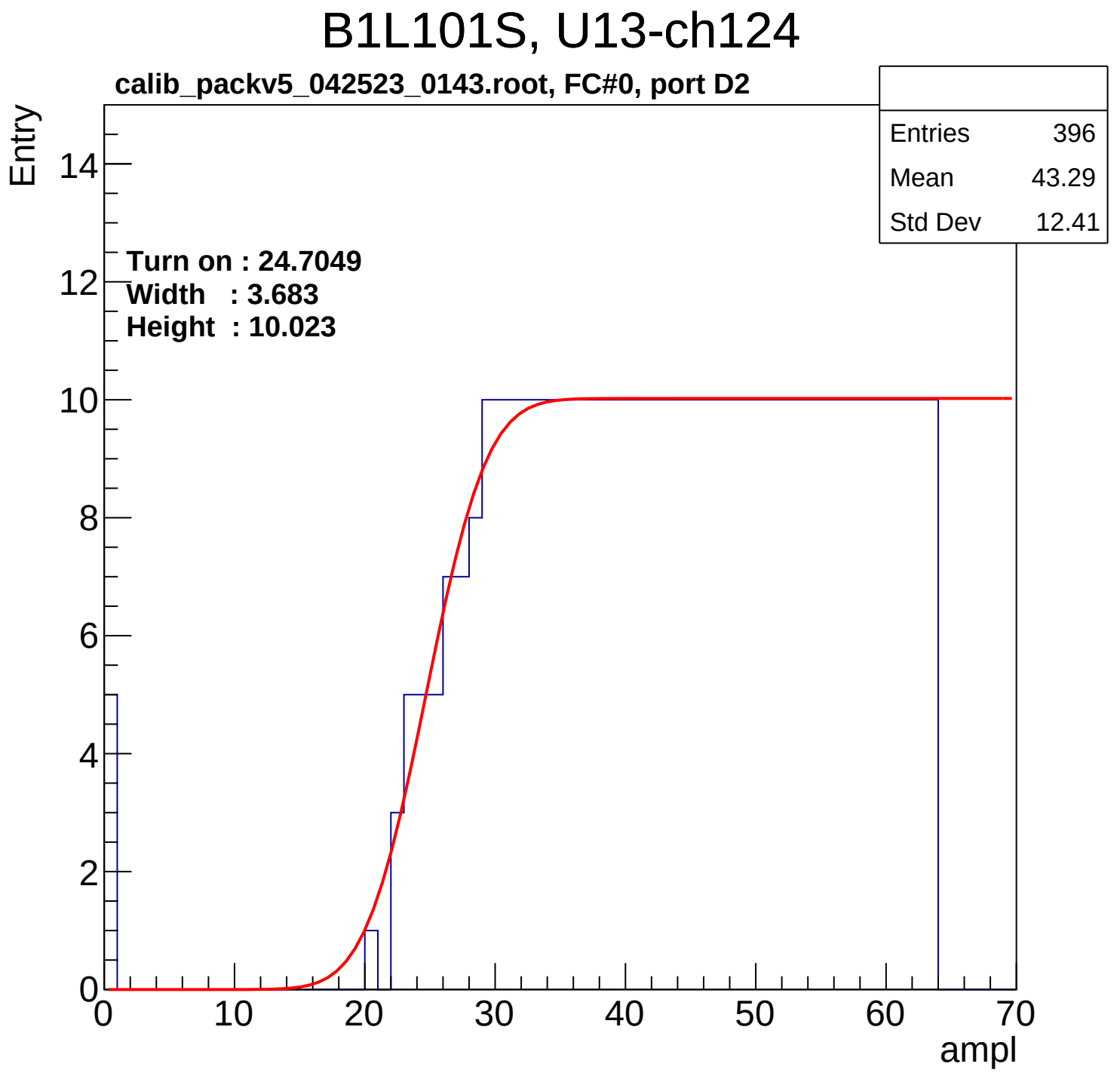
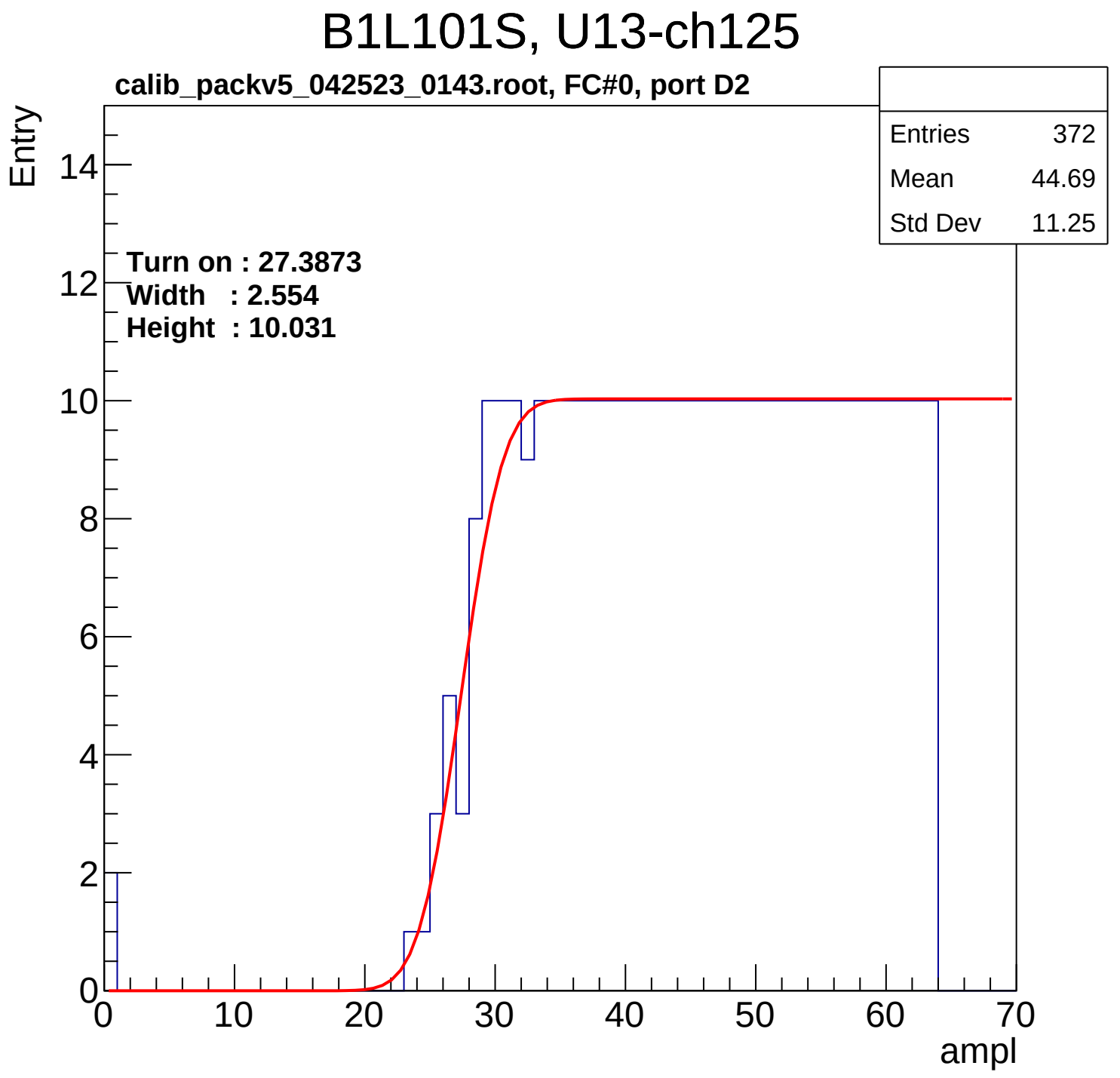
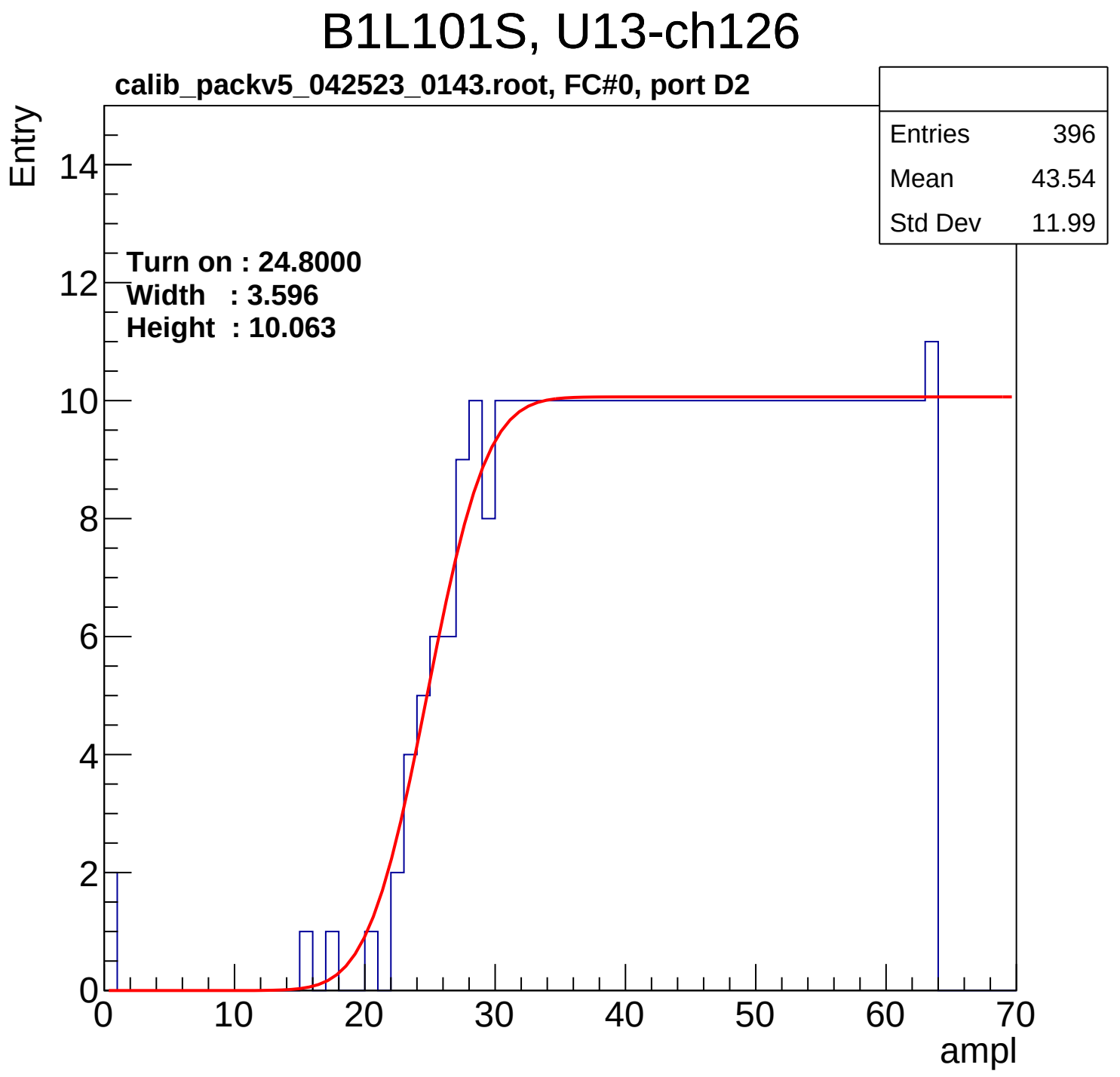
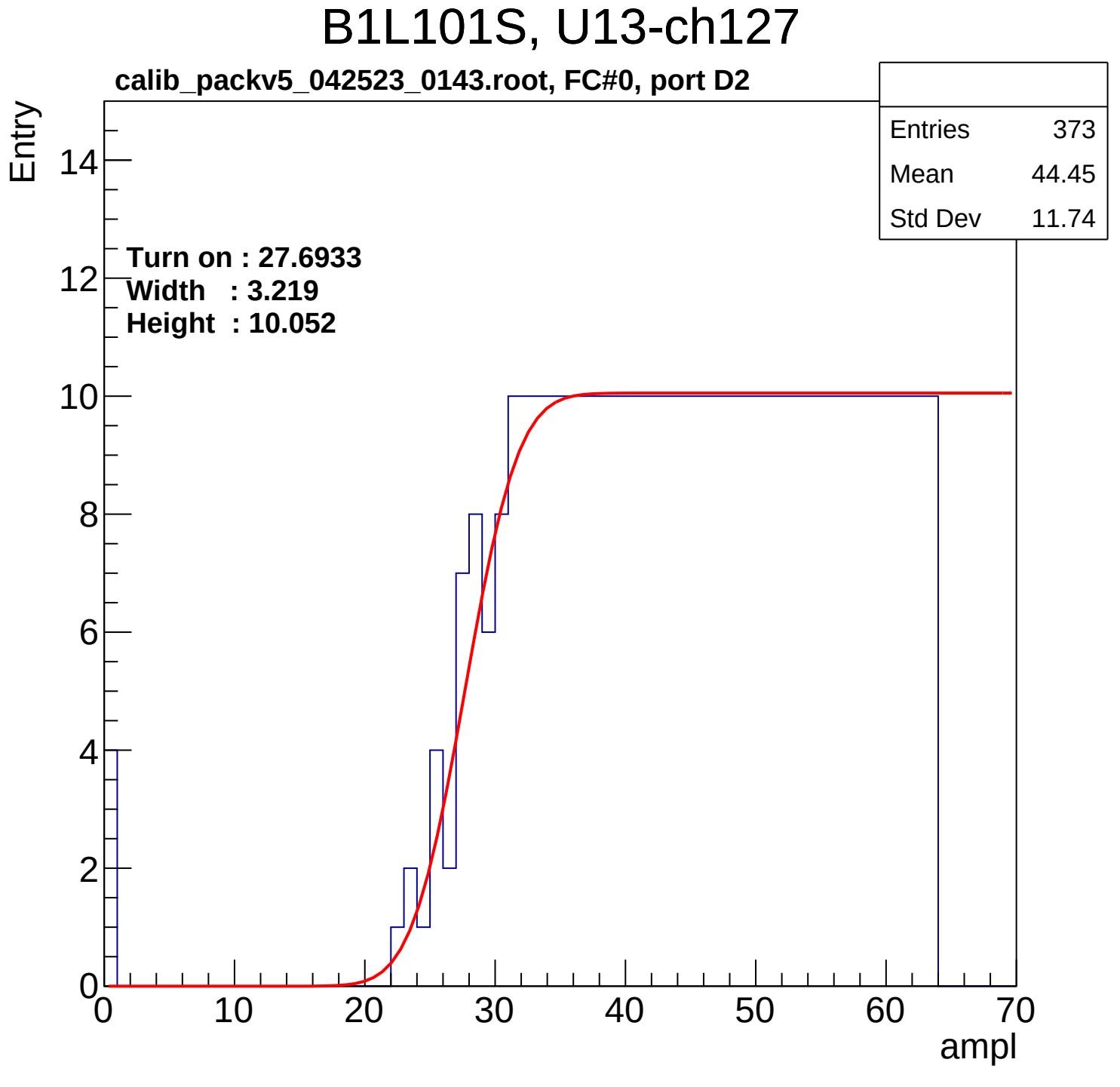
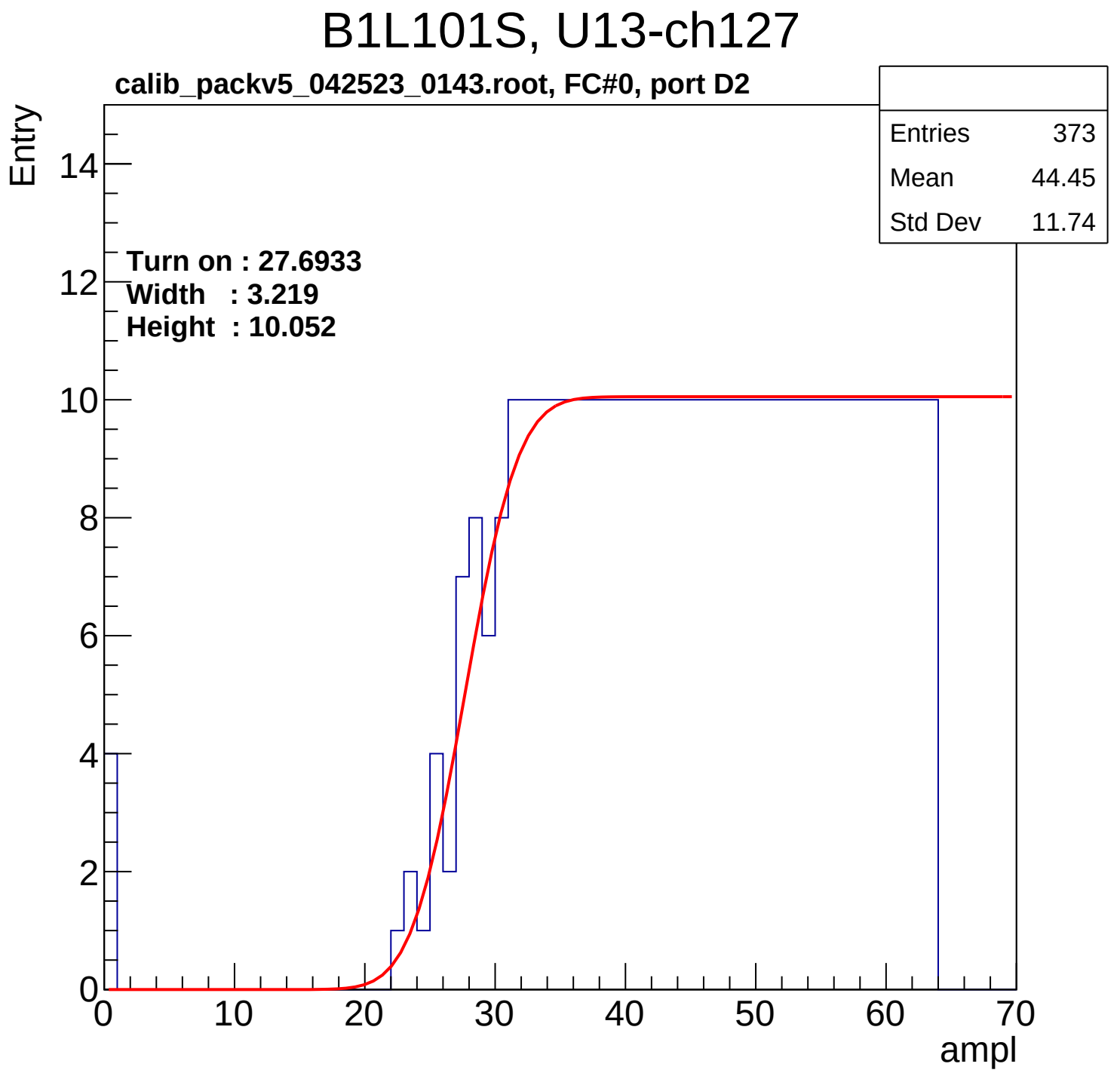
0
10
20
30
40
50
60
70


B1L101S, U13-ch124
calib_packv5_042523_0143.root, FC#0, port D2
Entries 396
Mean 43.29
Std Dev 12.41
Turn on : 24.7049
Width : 3.683
Height : 10.023
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L101S, U13-ch125
calib_packv5_042523_0143.root, FC#0, port D2
Entries 372
Mean 44.69
Std Dev 11.25
Turn on : 27.3873
Width : 2.554
Height : 10.031
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L101S, U13-ch126
calib_packv5_042523_0143.root, FC#0, port D2
Entries 396
Mean 43.54
Std Dev 11.99
Turn on : 24.8000
Width : 3.596
Height : 10.063
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L101S, U13-ch127
calib_packv5_042523_0143.root, FC#0, port D2
Entries 373
Mean 44.45
Std Dev 11.74
Turn on : 27.6933
Width : 3.219
Height : 10.052
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L101S, U13-ch127
calib_packv5_042523_0143.root, FC#0, port D2
Entries 373
Mean 44.45
Std Dev 11.74
Turn on : 27.6933
Width : 3.219
Height : 10.052
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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60
70