

B1L103S, U2-ch0

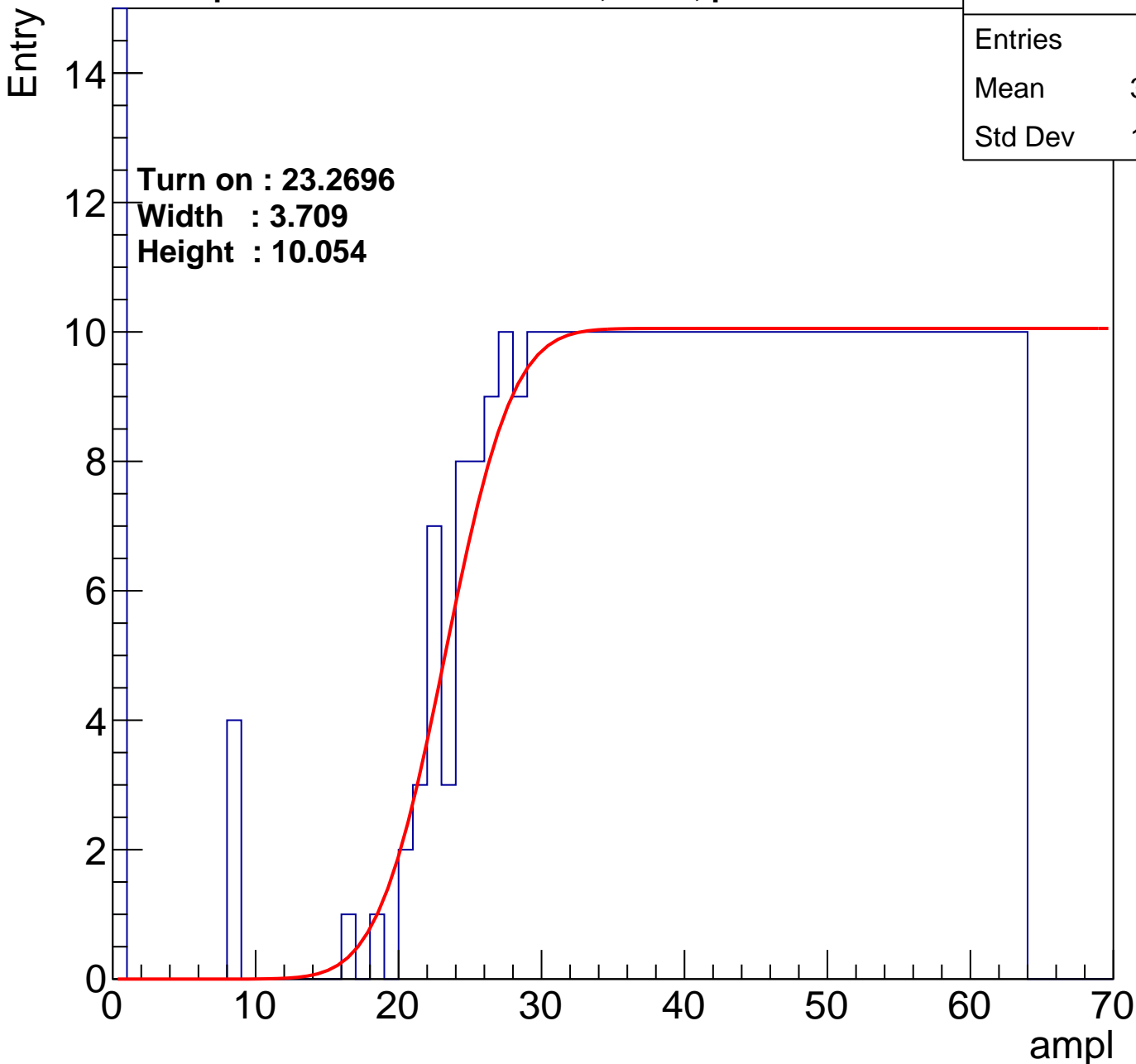
calib_packv5_041523_1651.root, FC#0, port C2

Entries	489
Mean	36.07
Std Dev	19.08

Turn on : 23.2696

Width : 3.709

Height : 10.054



B1L103S, U2-ch1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	416
Mean	40.07
Std Dev	17.21

Turn on : 27.6509

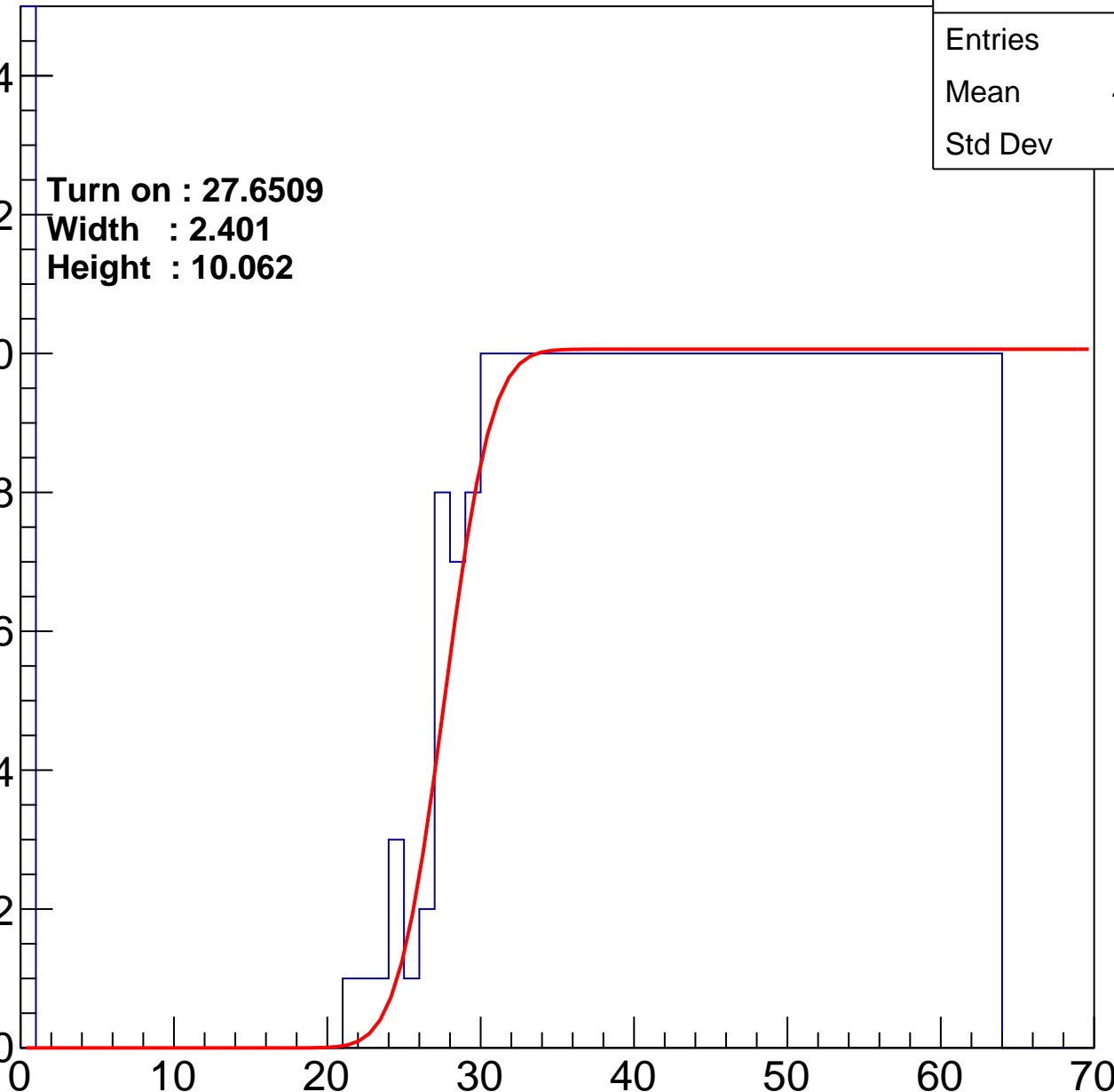
Width : 2.401

Height : 10.062

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch2

calib_packv5_041523_1651.root, FC#0, port C2

Entries	440
Mean	38.54
Std Dev	18.16

Turn on : 25.7600

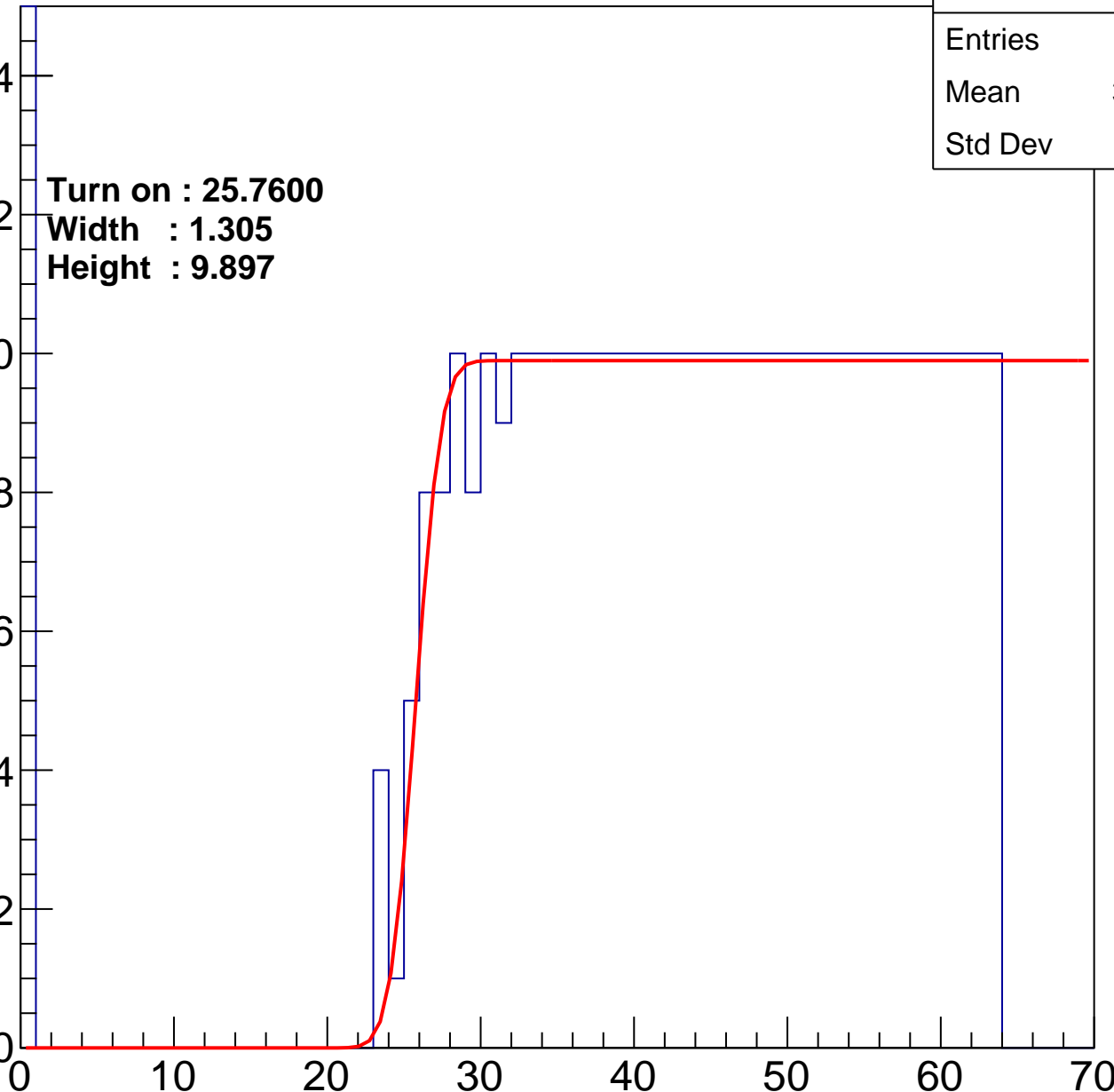
Width : 1.305

Height : 9.897

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch3

calib_packv5_041523_1651.root, FC#0, port C2

Entries	448
Mean	38.29
Std Dev	18.06

Turn on : 25.5872

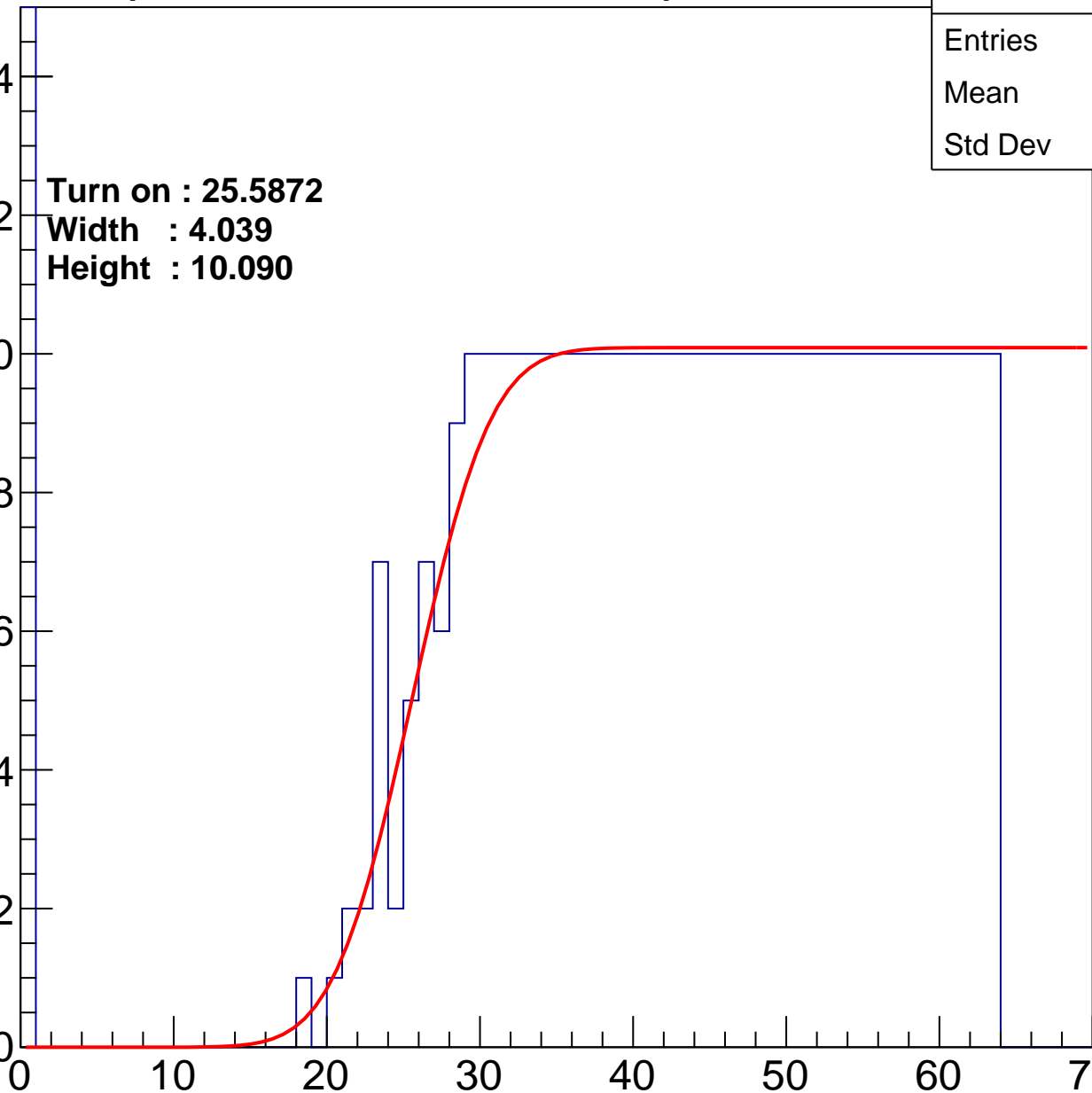
Width : 4.039

Height : 10.090

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch4

calib_packv5_041523_1651.root, FC#0, port C2

Entries	428
Mean	39.06
Std Dev	18.04

Turn on : 26.7531

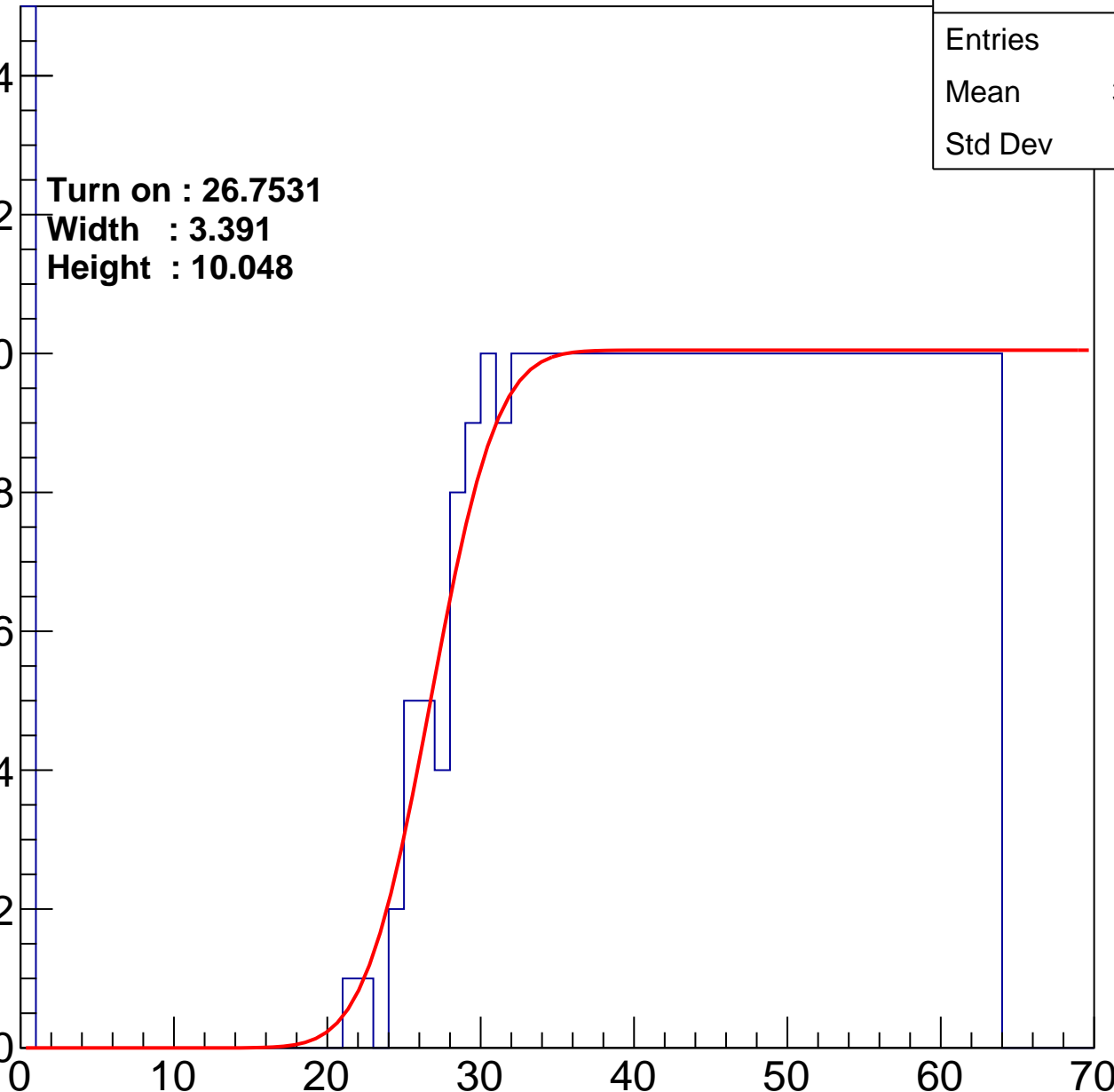
Width : 3.391

Height : 10.048

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch5

calib_packv5_041523_1651.root, FC#0, port C2

Entries	443
Mean	38.18
Std Dev	18.48

Turn on : 25.7936

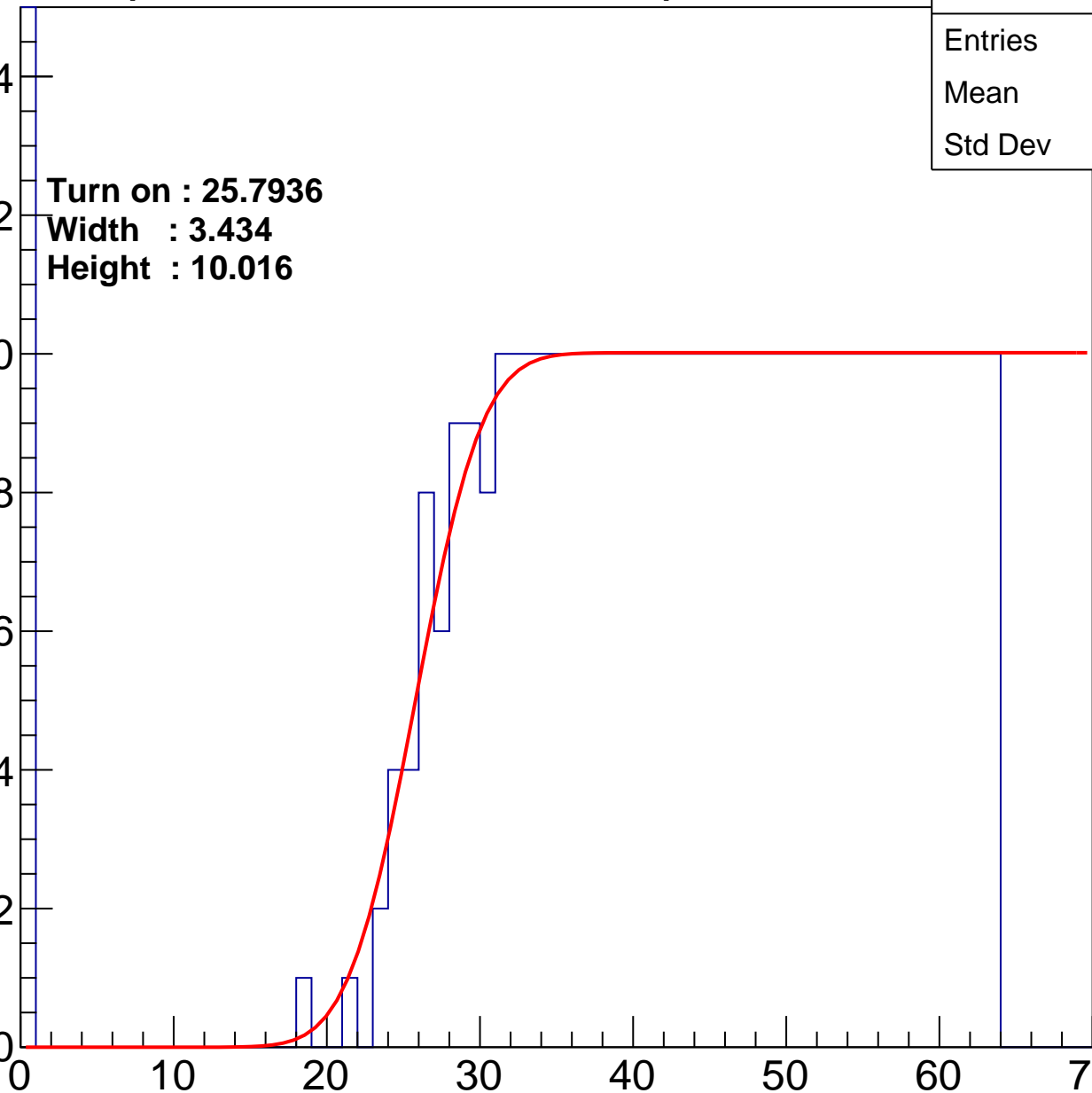
Width : 3.434

Height : 10.016

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch6

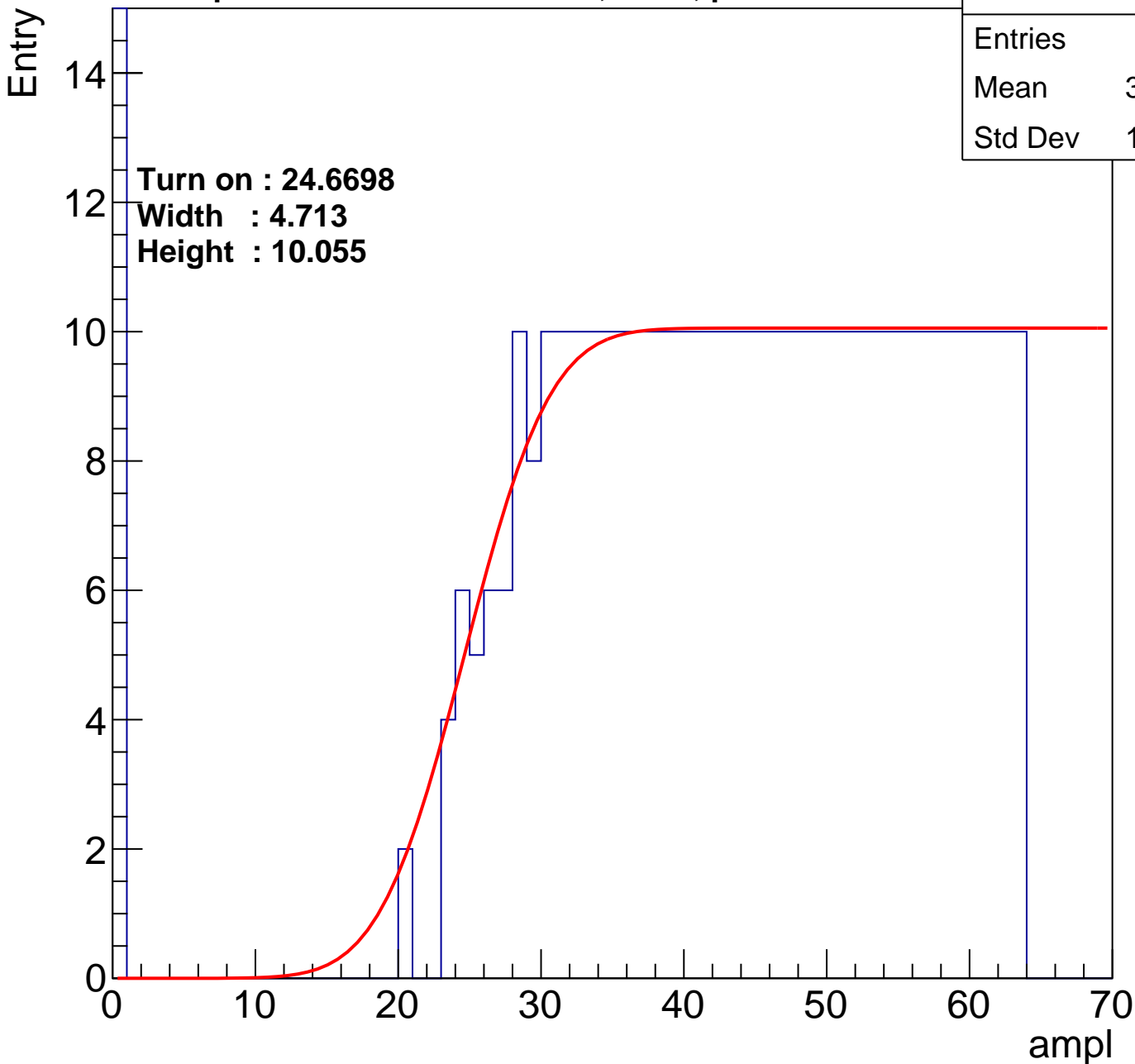
calib_packv5_041523_1651.root, FC#0, port C2

Entries	431
Mean	39.54
Std Dev	17.14

Turn on : 24.6698

Width : 4.713

Height : 10.055



B1L103S, U2-ch7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	421
Mean	38.95
Std Dev	18.56

Turn on : 27.8692

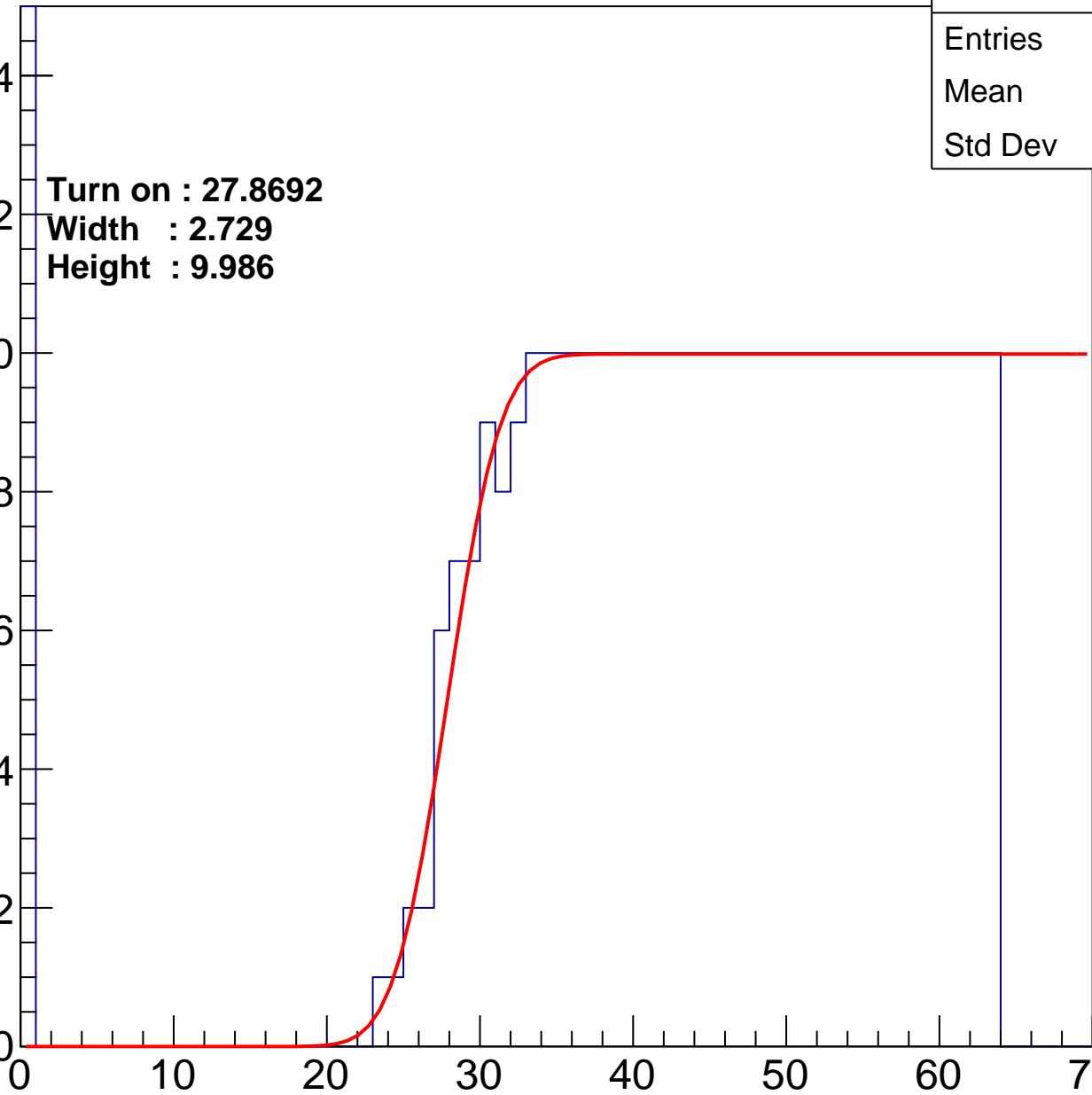
Width : 2.729

Height : 9.986

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch8

calib_packv5_041523_1651.root, FC#0, port C2

Entries	438
Mean	38.98
Std Dev	17.61

Turn on : 25.0507

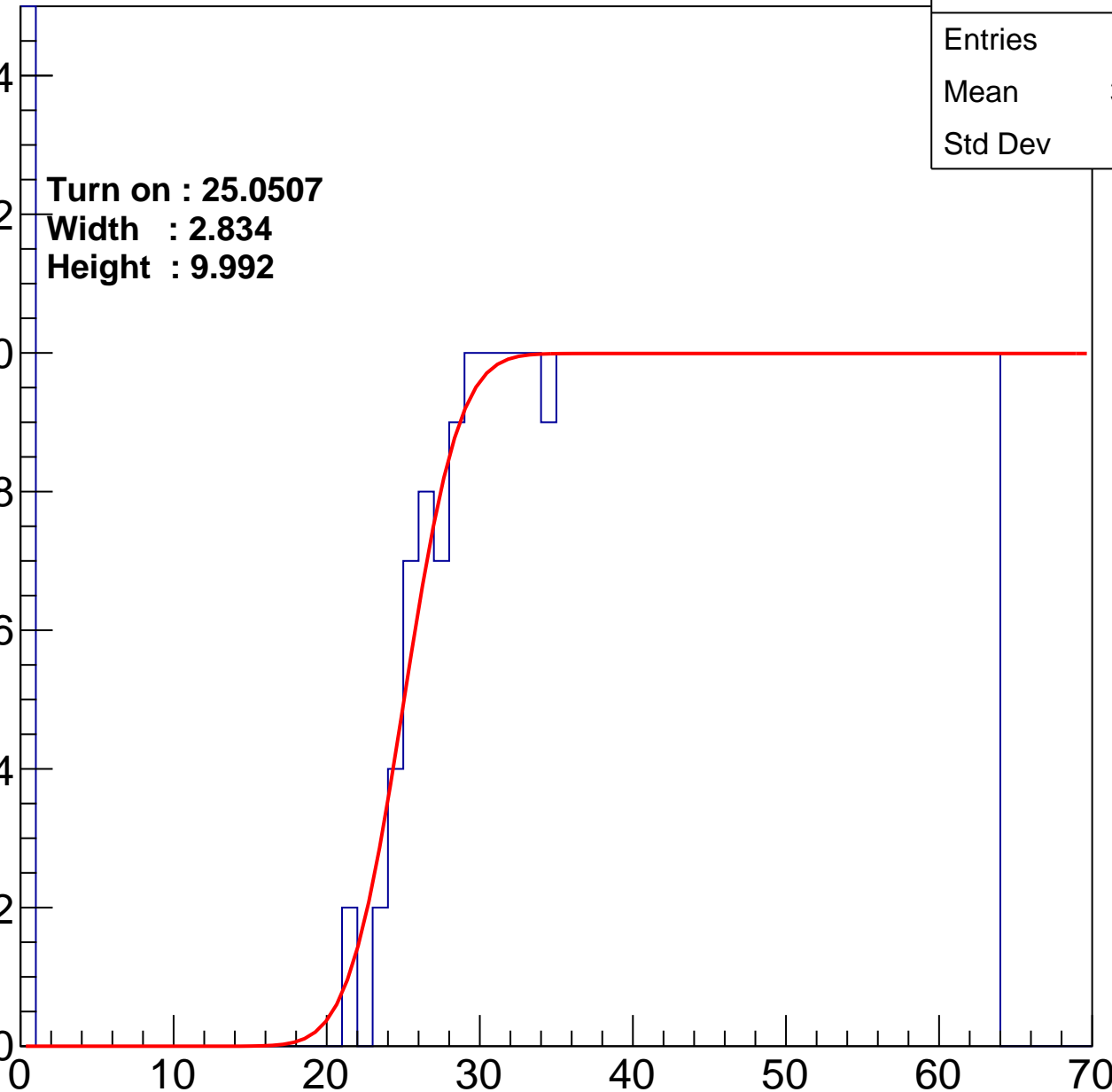
Width : 2.834

Height : 9.992

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch9

calib_packv5_041523_1651.root, FC#0, port C2

Entries	422
Mean	39.19
Std Dev	18.18

Turn on : 27.5945

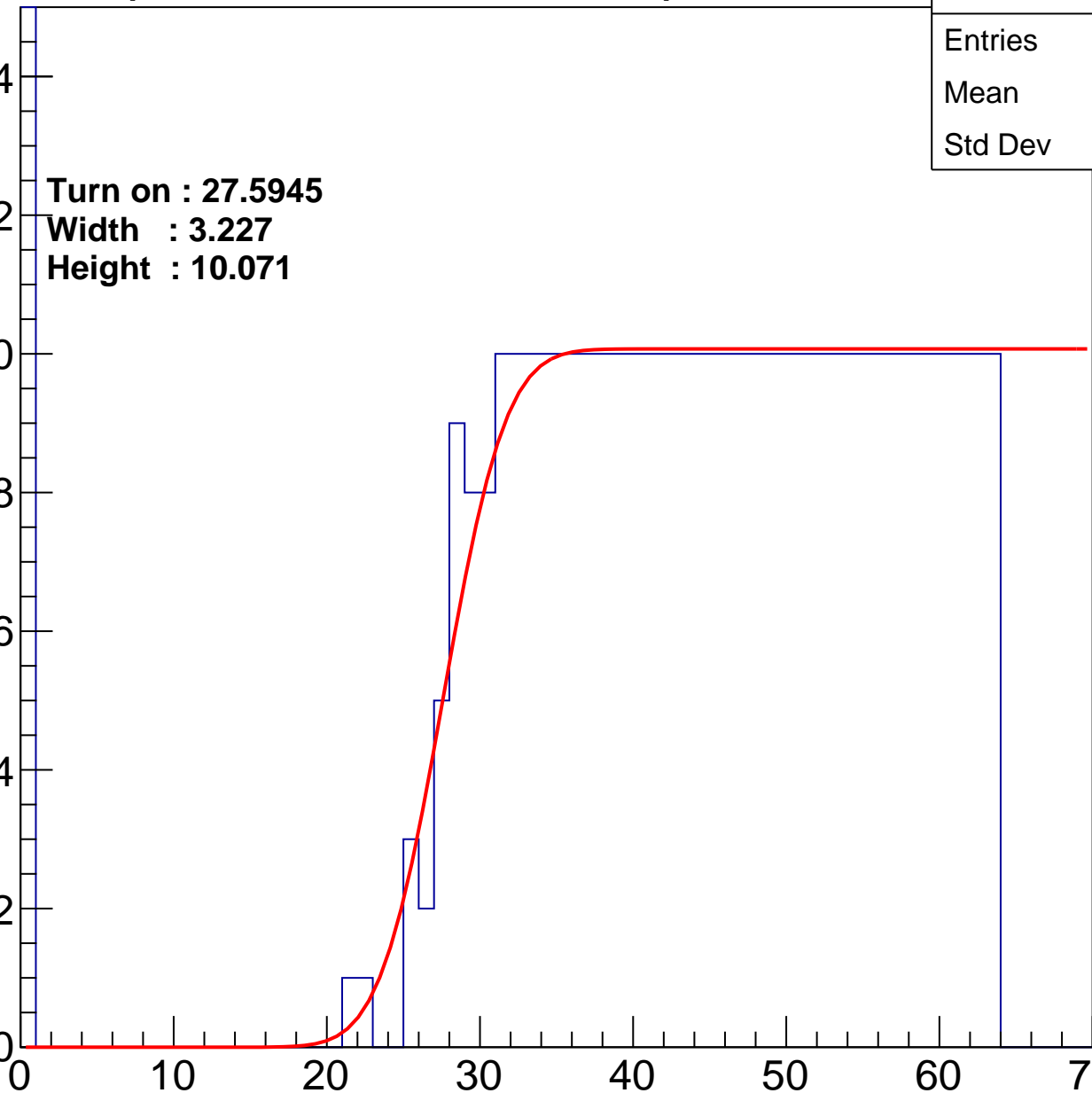
Width : 3.227

Height : 10.071

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch10

calib_packv5_041523_1651.root, FC#0, port C2

Entries	432
Mean	39.06
Std Dev	17.78

Turn on : 25.5290

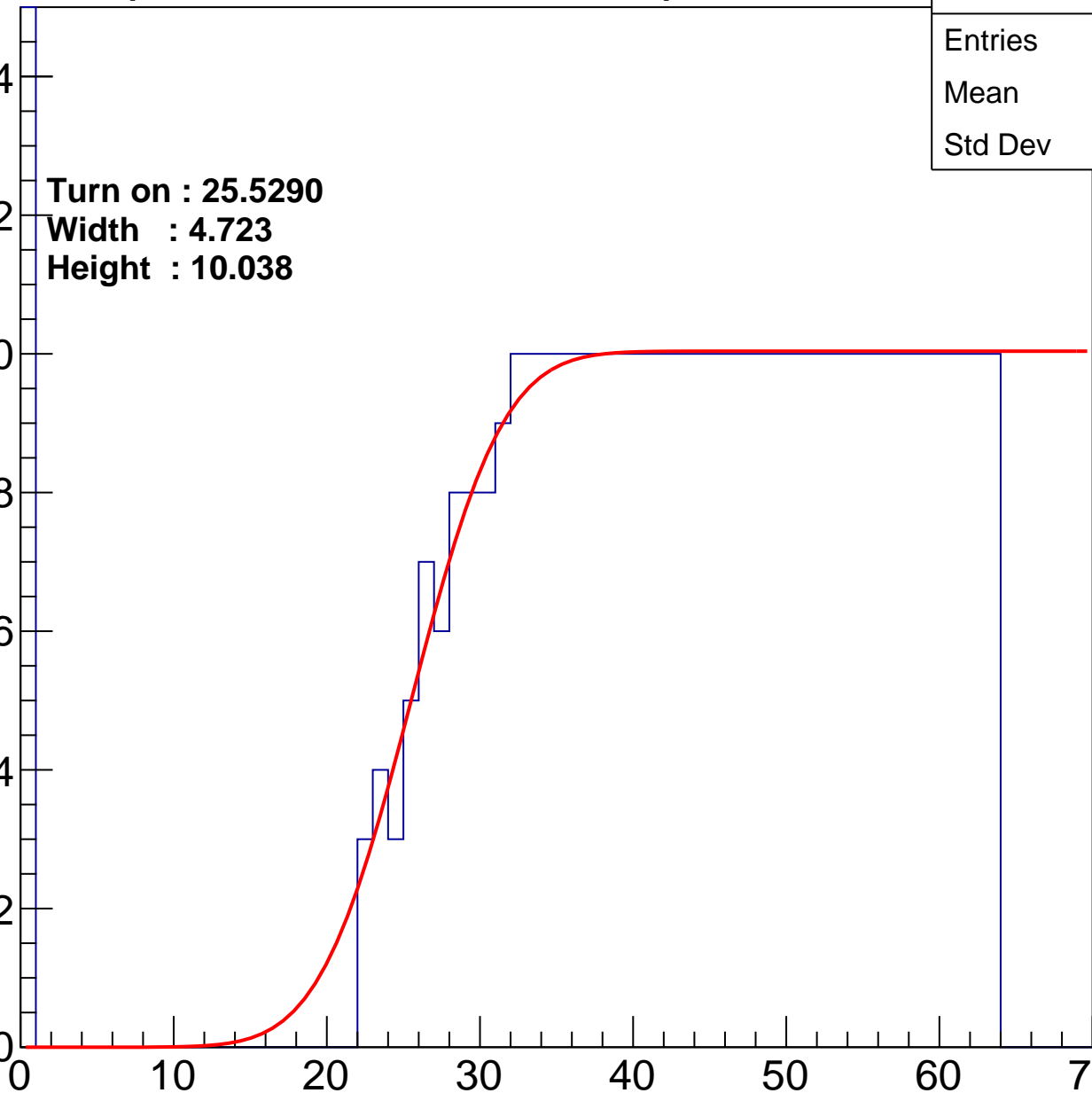
Width : 4.723

Height : 10.038

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch11

calib_packv5_041523_1651.root, FC#0, port C2

Entries	437
Mean	39.15
Std Dev	17.43

Turn on : 25.5676

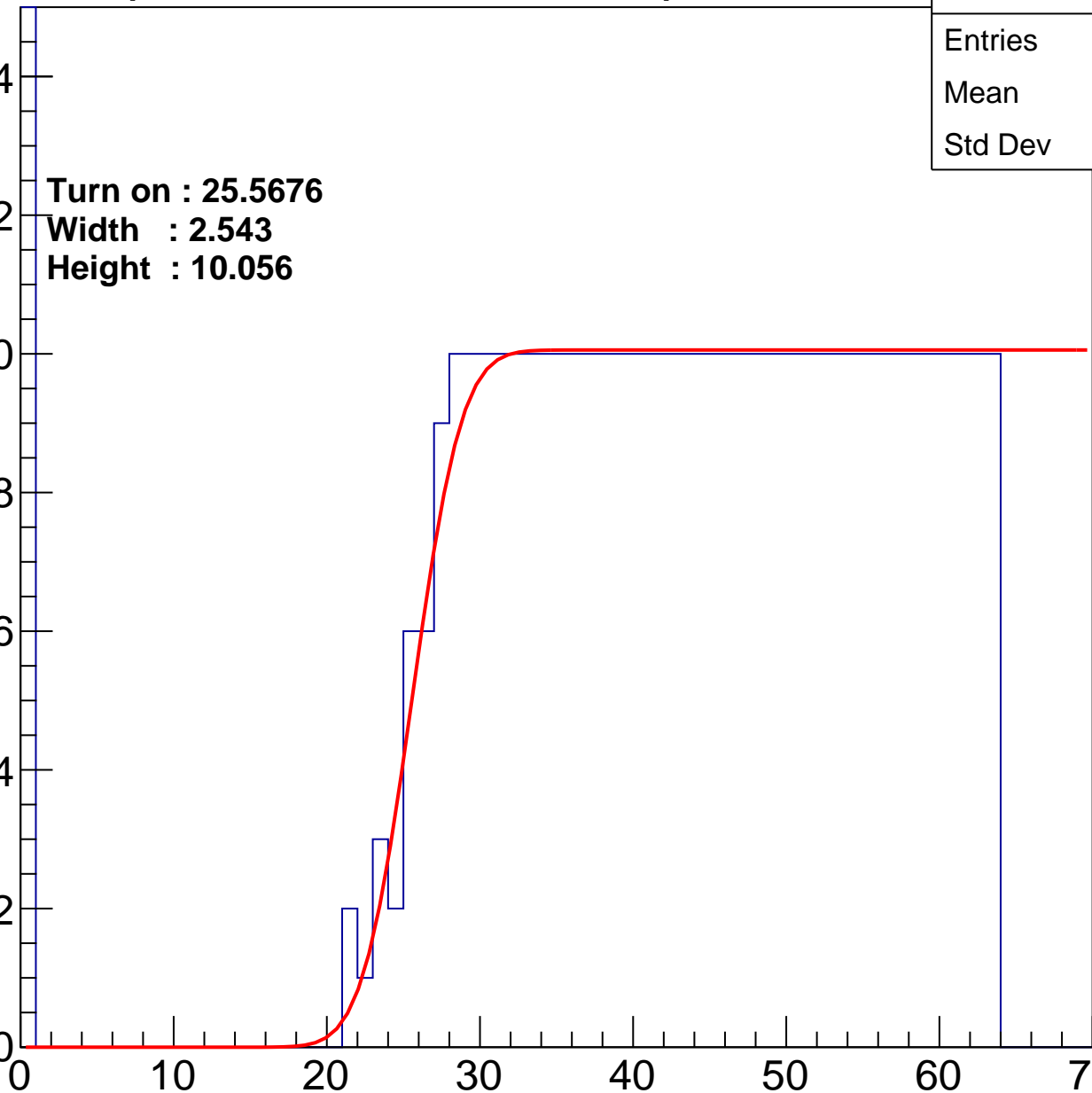
Width : 2.543

Height : 10.056

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch12

calib_packv5_041523_1651.root, FC#0, port C2

Entries	429
Mean	39.83
Std Dev	16.79

Turn on : 25.4515

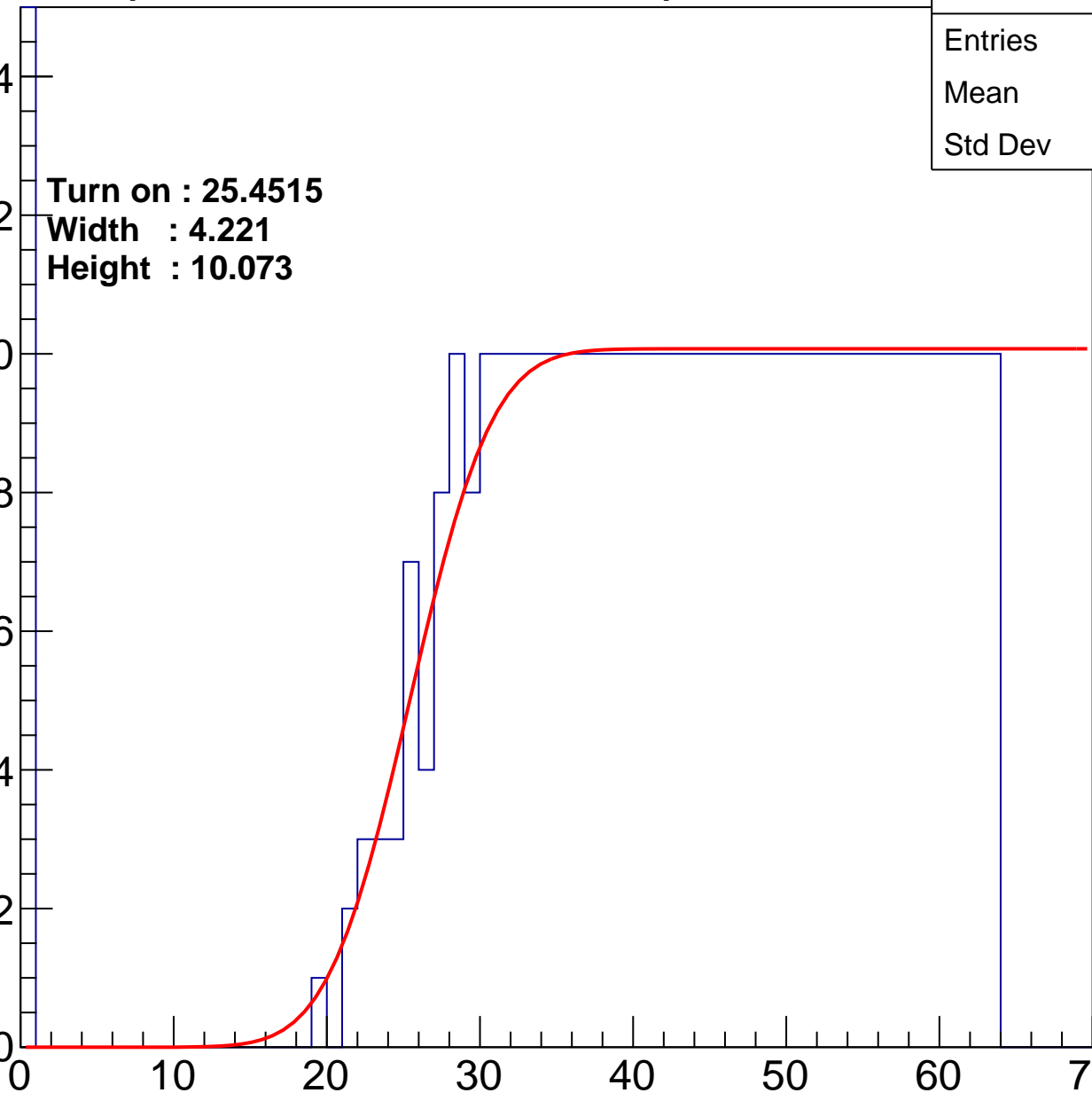
Width : 4.221

Height : 10.073

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch13

calib_packv5_041523_1651.root, FC#0, port C2

Entries	439
Mean	38.55
Std Dev	18.19

Turn on : 26.1566

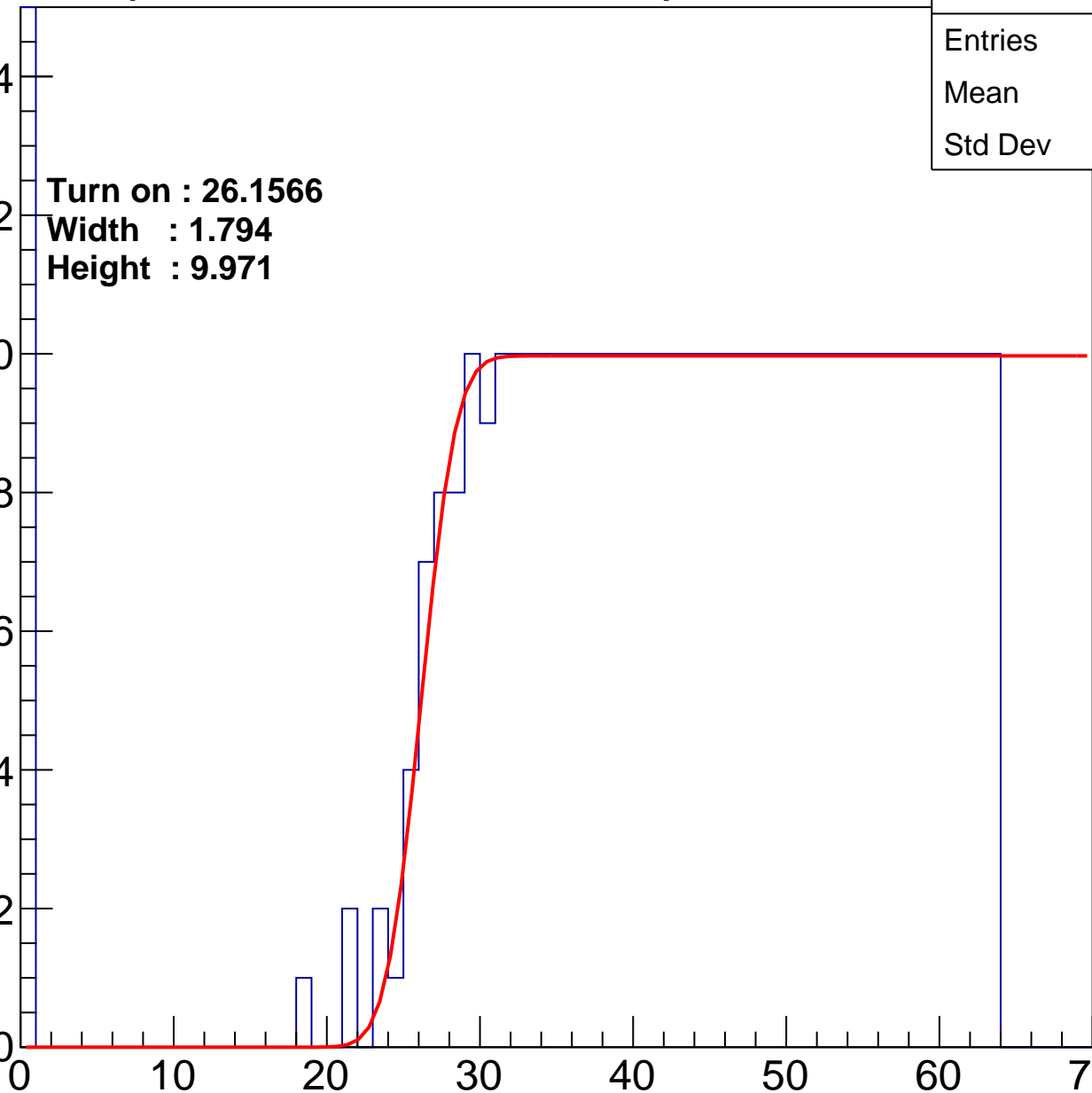
Width : 1.794

Height : 9.971

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch14

calib_packv5_041523_1651.root, FC#0, port C2

Entries	424
Mean	39.18
Std Dev	18.08

Turn on : 27.0464

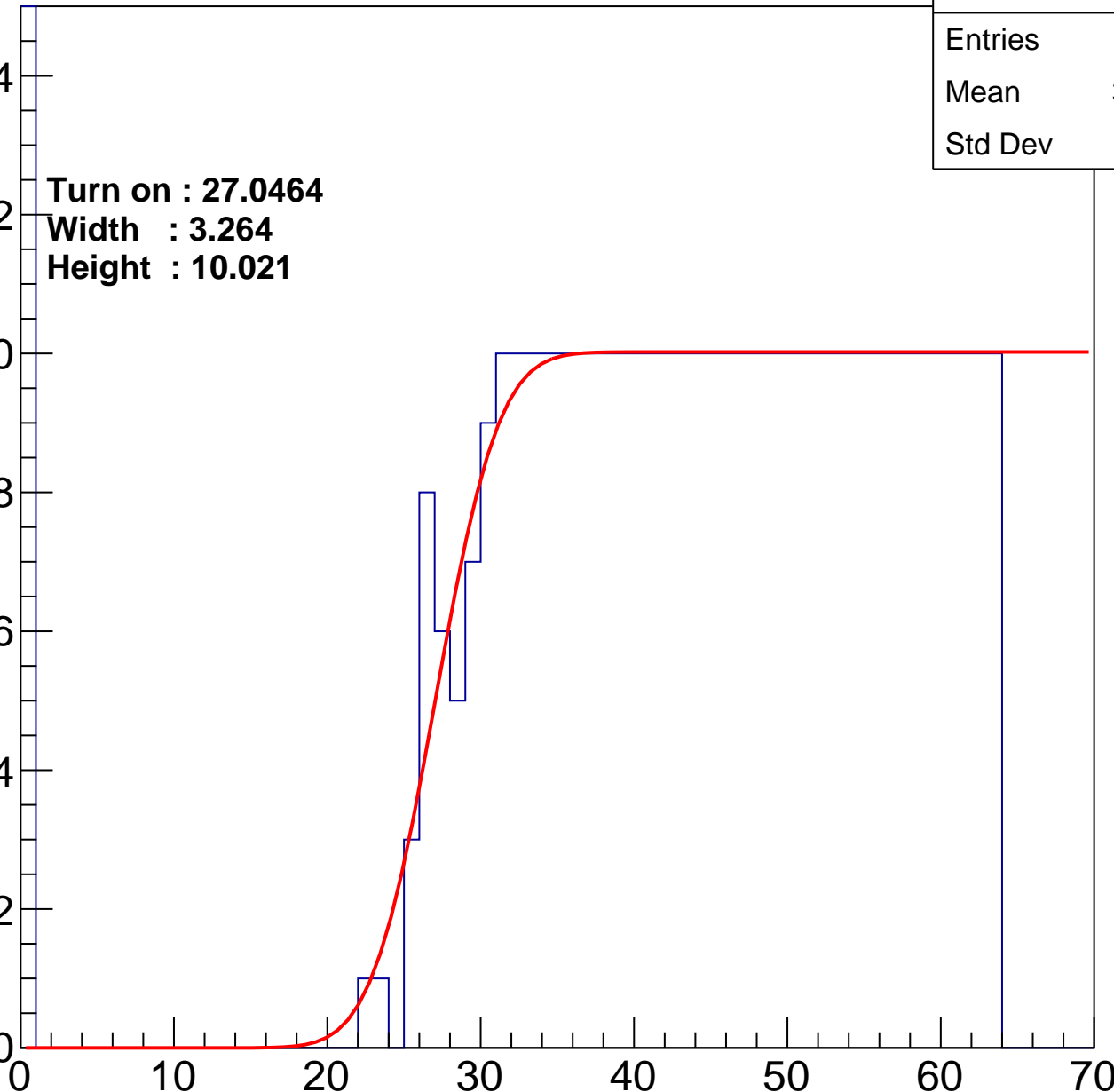
Width : 3.264

Height : 10.021

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch15

calib_packv5_041523_1651.root, FC#0, port C2

Entries	423
Mean	39.83
Std Dev	17.16

Turn on : 26.2267

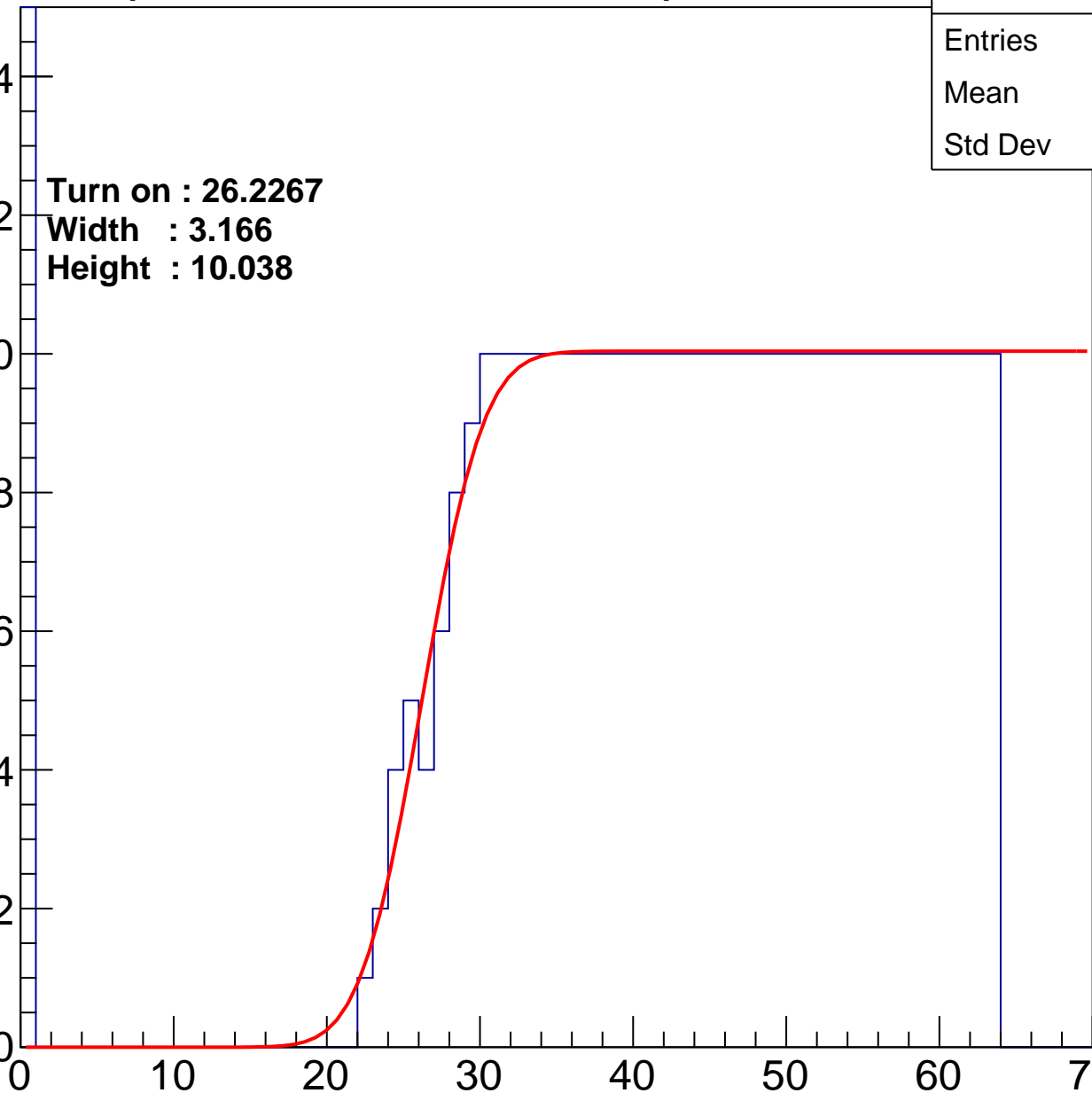
Width : 3.166

Height : 10.038

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch16

calib_packv5_041523_1651.root, FC#0, port C2

Entries	454
Mean	38.08
Std Dev	18.12

Turn on : 25.3638

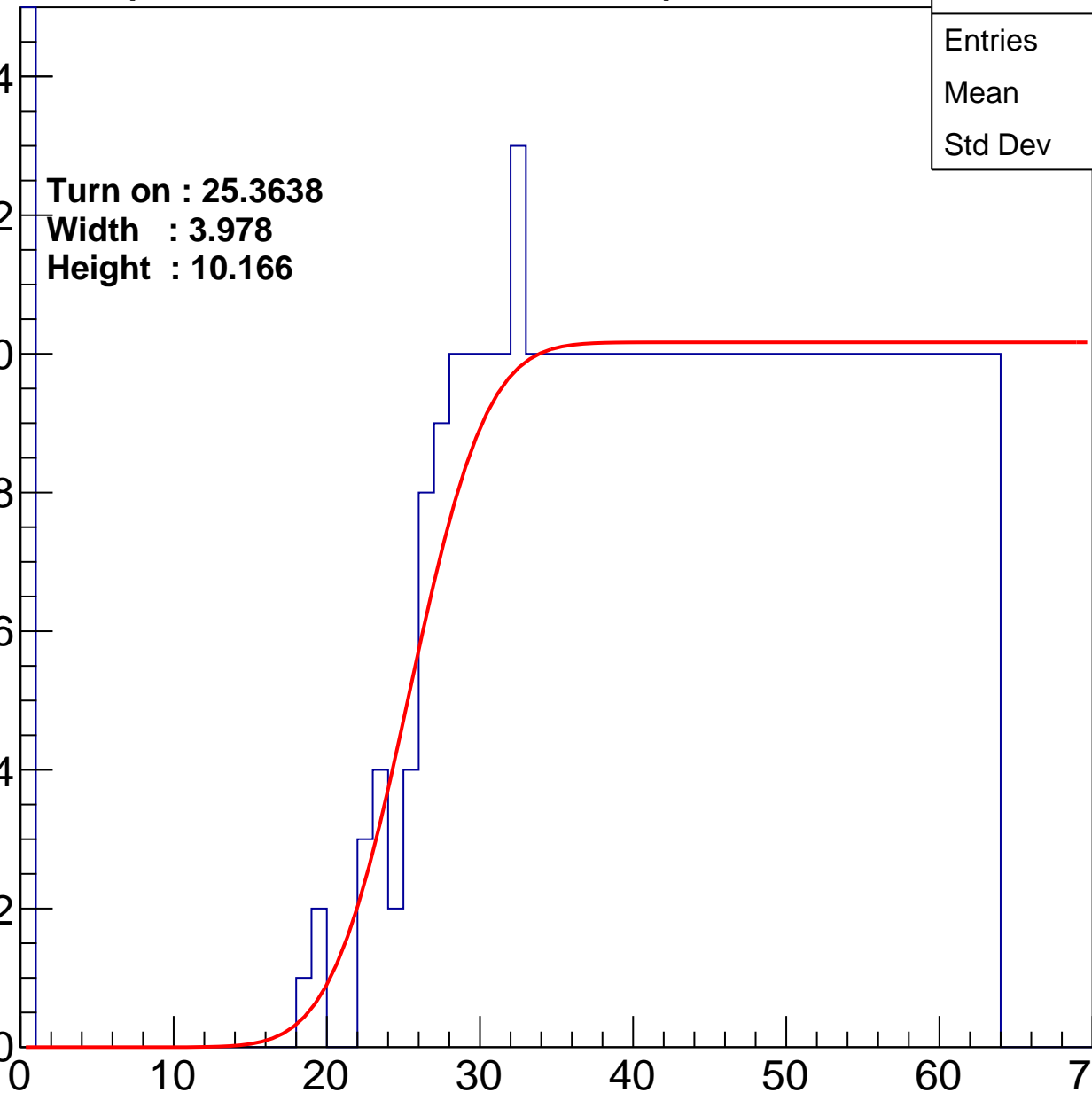
Width : 3.978

Height : 10.166

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch17

calib_packv5_041523_1651.root, FC#0, port C2

Entries	438
Mean	38.71
Std Dev	18.02

Turn on : 25.4558

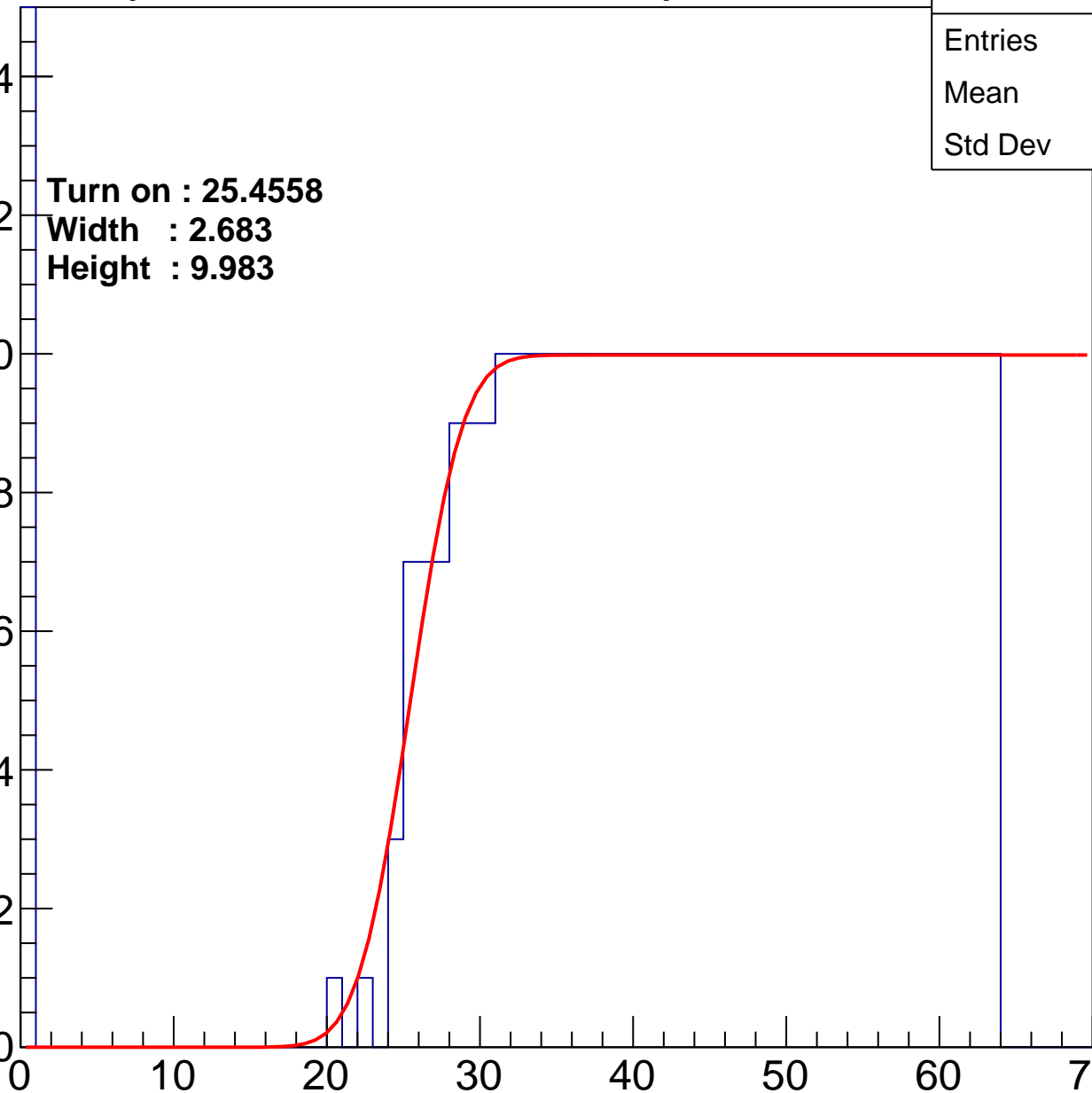
Width : 2.683

Height : 9.983

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch18

calib_packv5_041523_1651.root, FC#0, port C2

Entries	428
Mean	39.59
Std Dev	17.24

Turn on : 26.0783

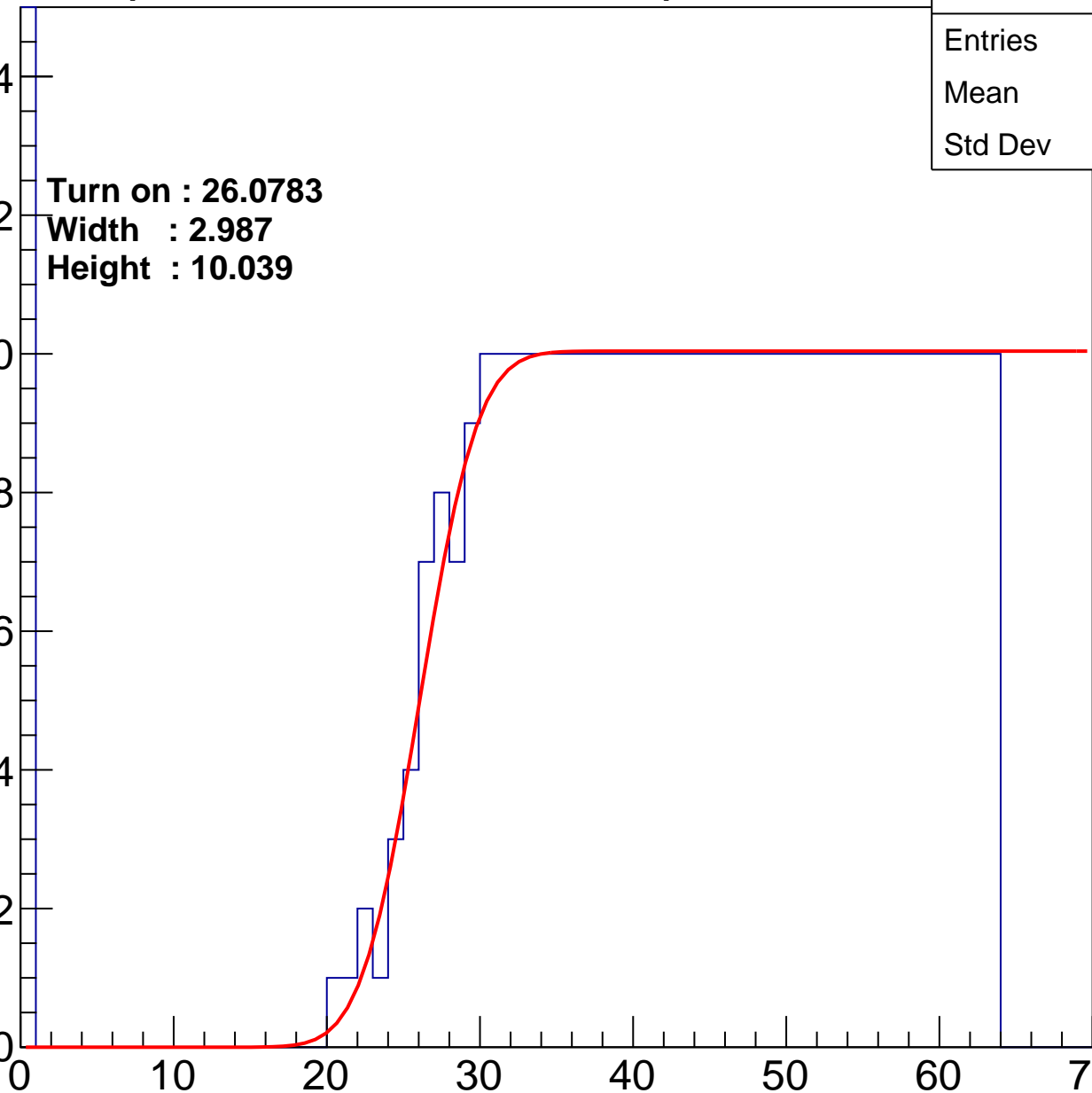
Width : 2.987

Height : 10.039

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch19

calib_packv5_041523_1651.root, FC#0, port C2

Entries	440
Mean	38.24
Std Dev	18.57

Turn on : 26.7100

Width : 2.804

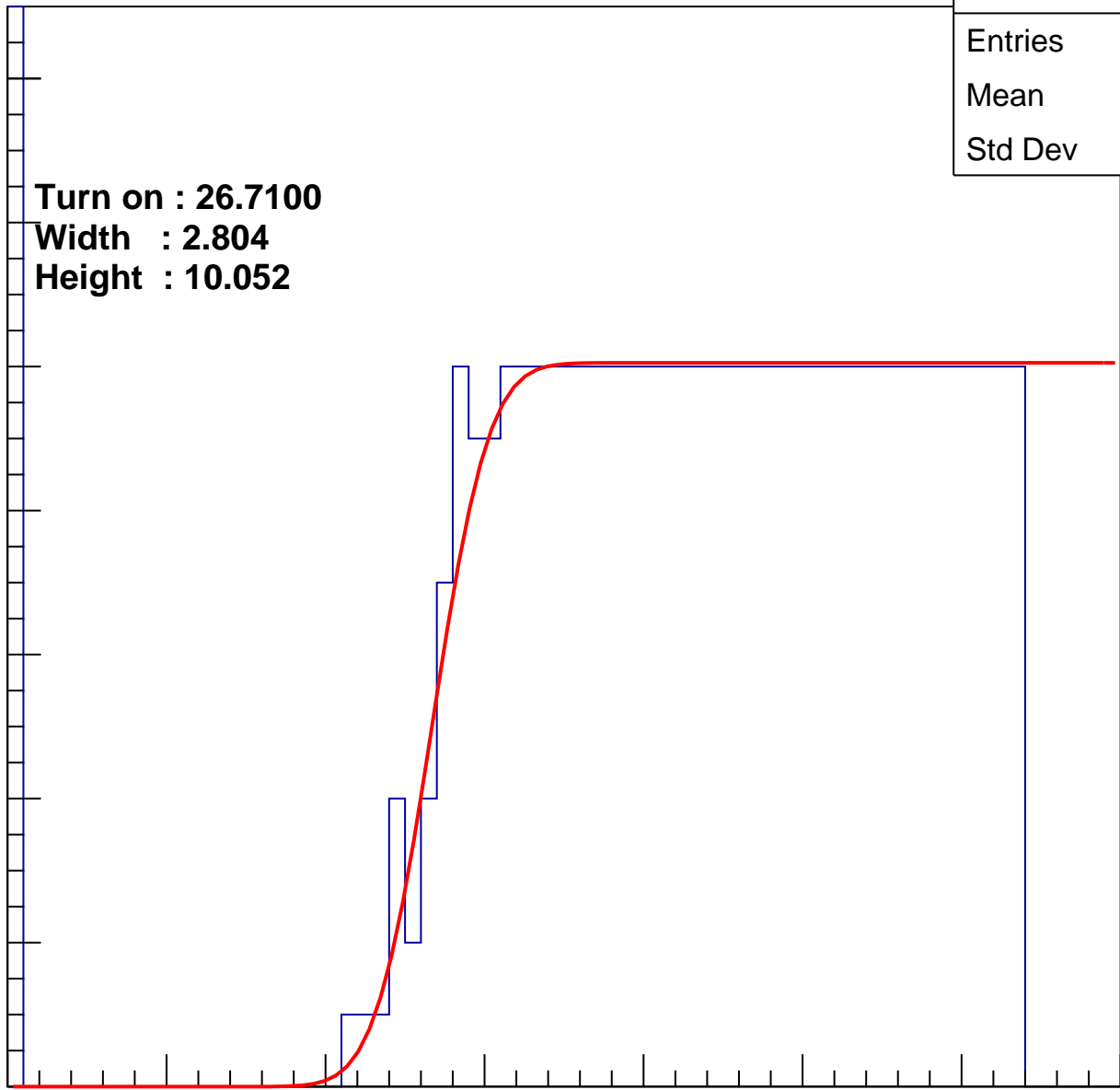
Height : 10.052

Entry

14
12
10
8
6
4
2
0

ampl

0 10 20 30 40 50 60 70



B1L103S, U2-ch20

calib_packv5_041523_1651.root, FC#0, port C2

Entries	438
Mean	39.12
Std Dev	17.38

Turn on : 25.6283

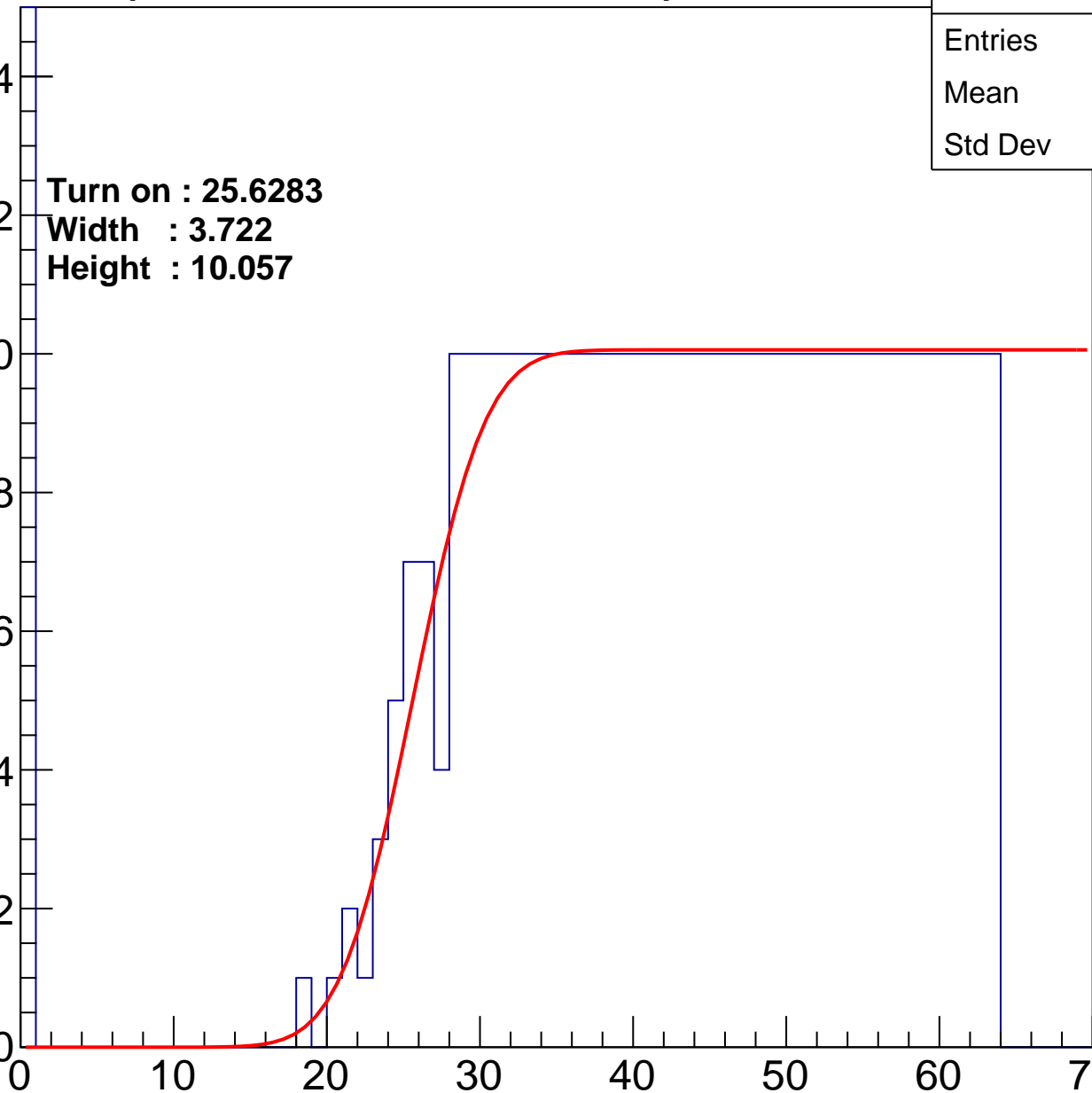
Width : 3.722

Height : 10.057

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch21

calib_packv5_041523_1651.root, FC#0, port C2

Entries	425
Mean	39.52
Std Dev	17.53

Turn on : 26.5439

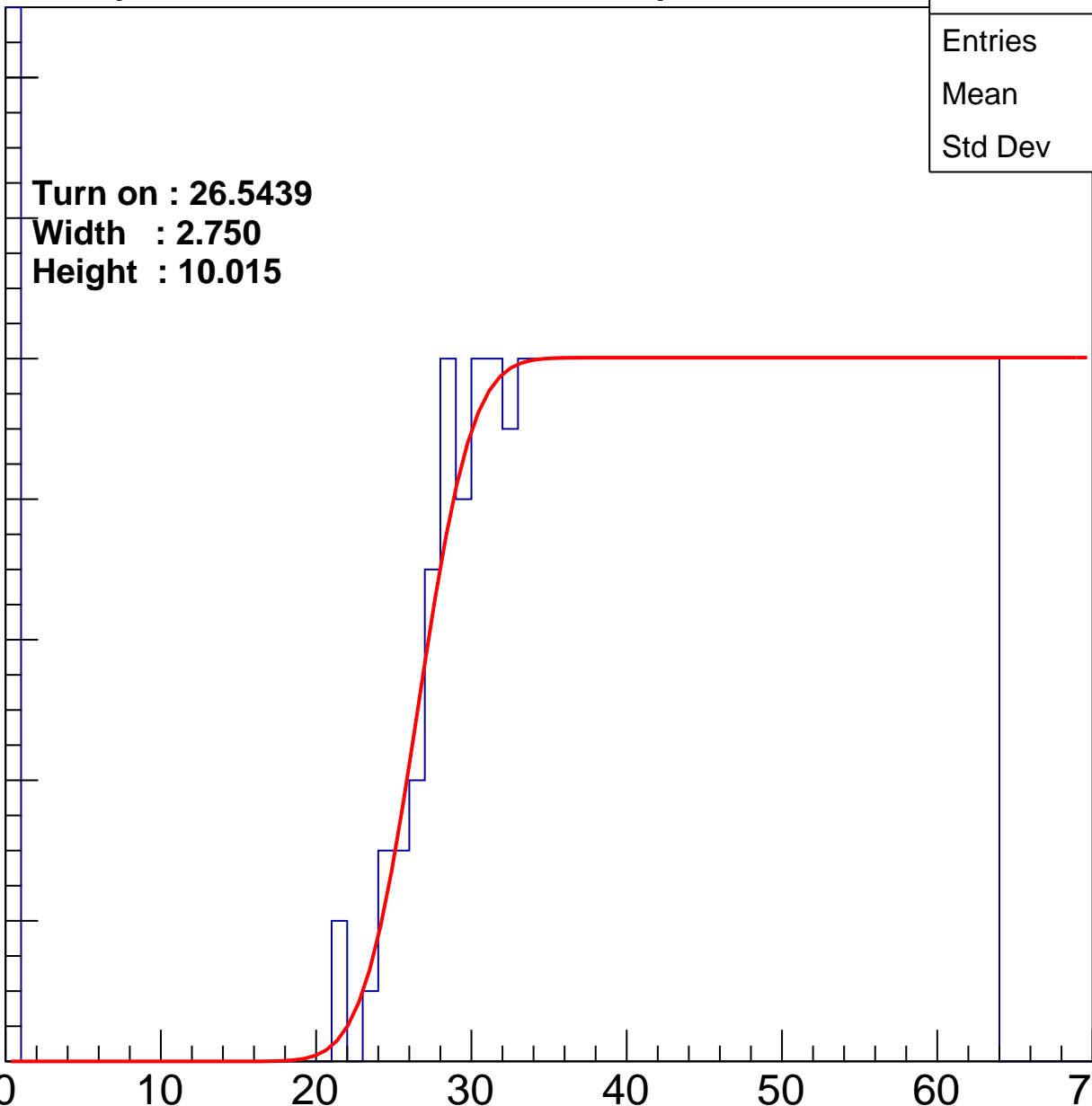
Width : 2.750

Height : 10.015

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch22

calib_packv5_041523_1651.root, FC#0, port C2

Entries	457
Mean	38.58
Std Dev	17.14

Turn on : 23.4093

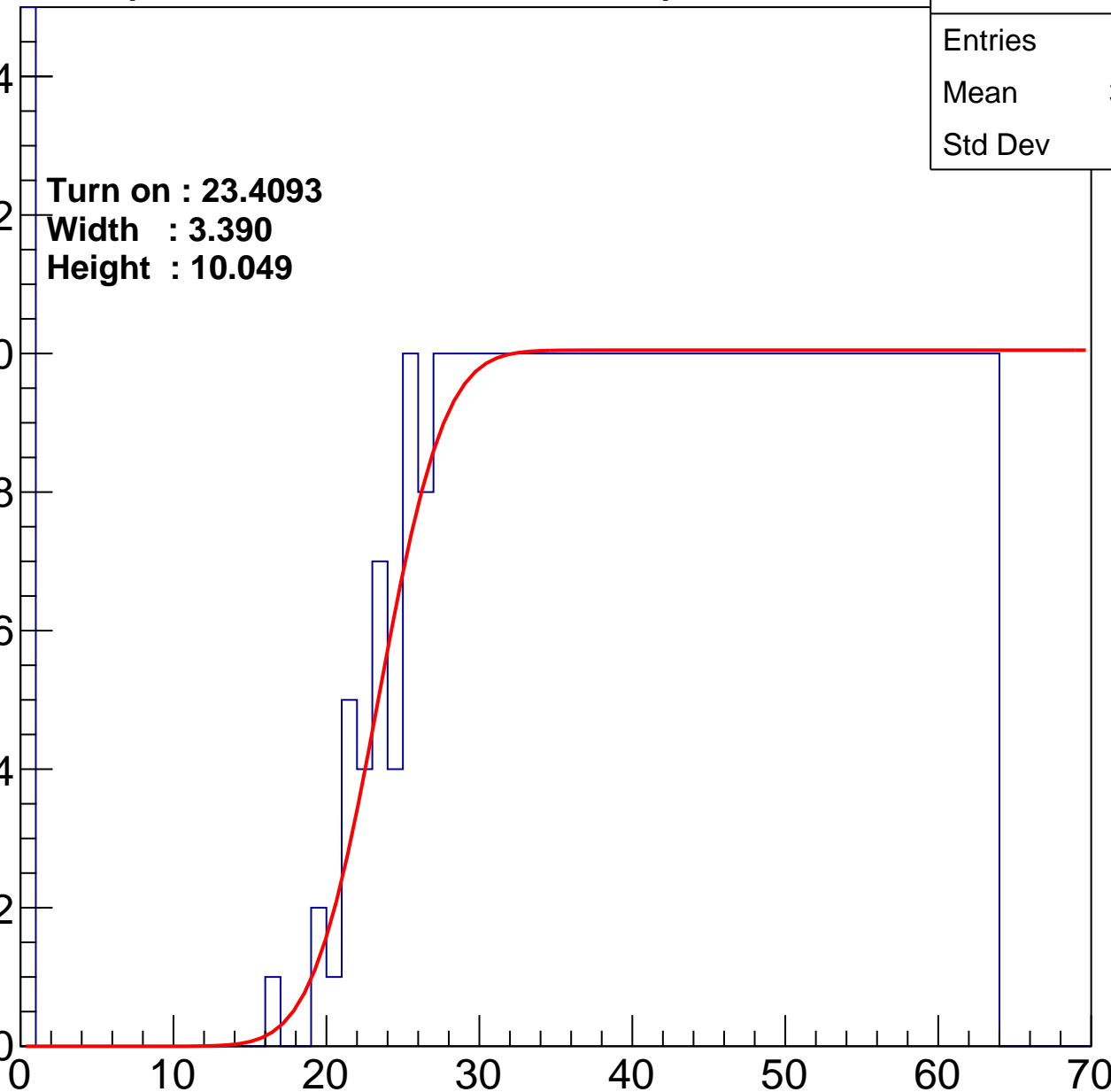
Width : 3.390

Height : 10.049

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch23

calib_packv5_041523_1651.root, FC#0, port C2

Entries	436
Mean	39.05
Std Dev	17.62

Turn on : 26.2168

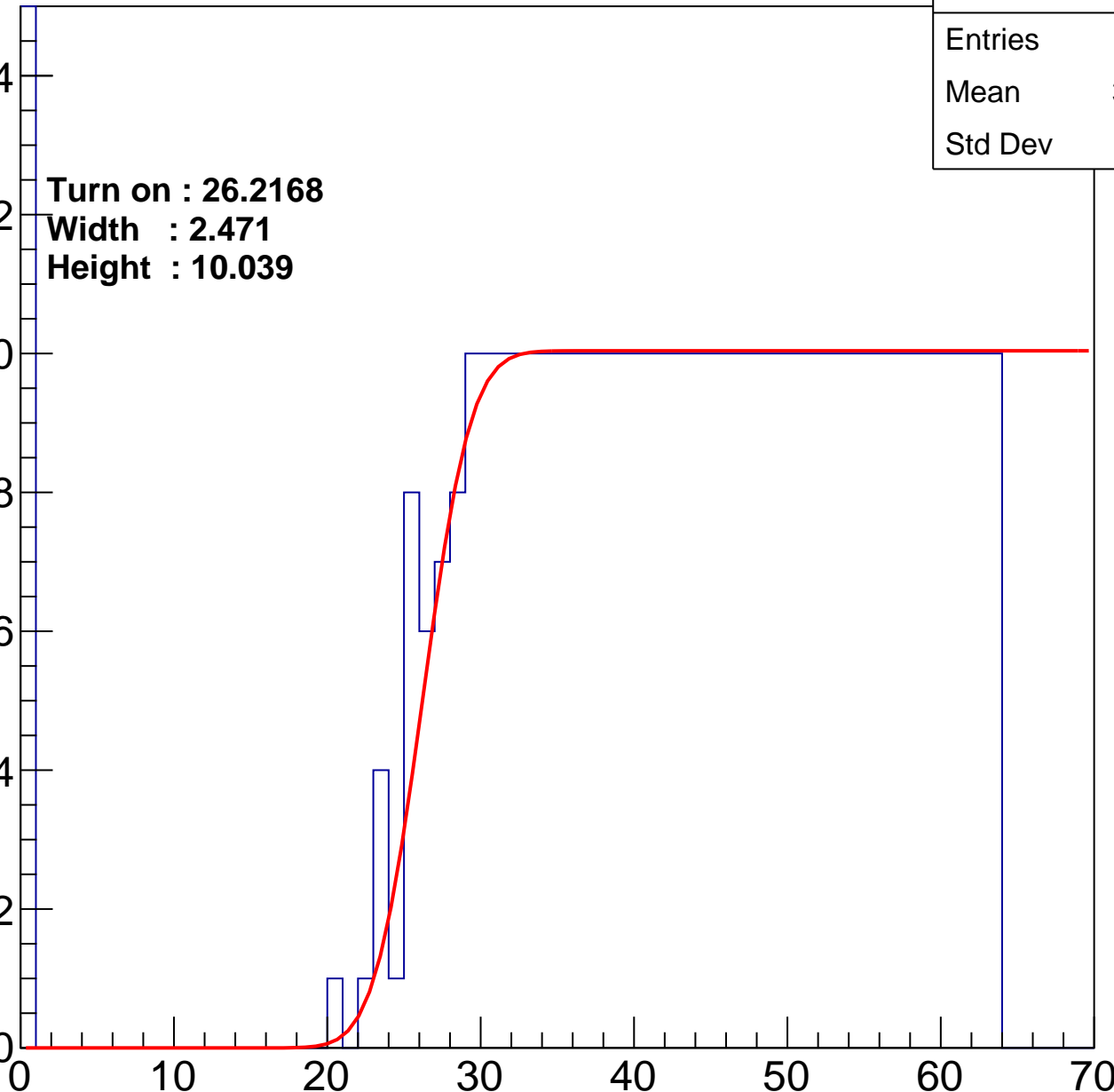
Width : 2.471

Height : 10.039

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch24

calib_packv5_041523_1651.root, FC#0, port C2

Entries	439
Mean	39
Std Dev	17.53

Turn on : 25.4694

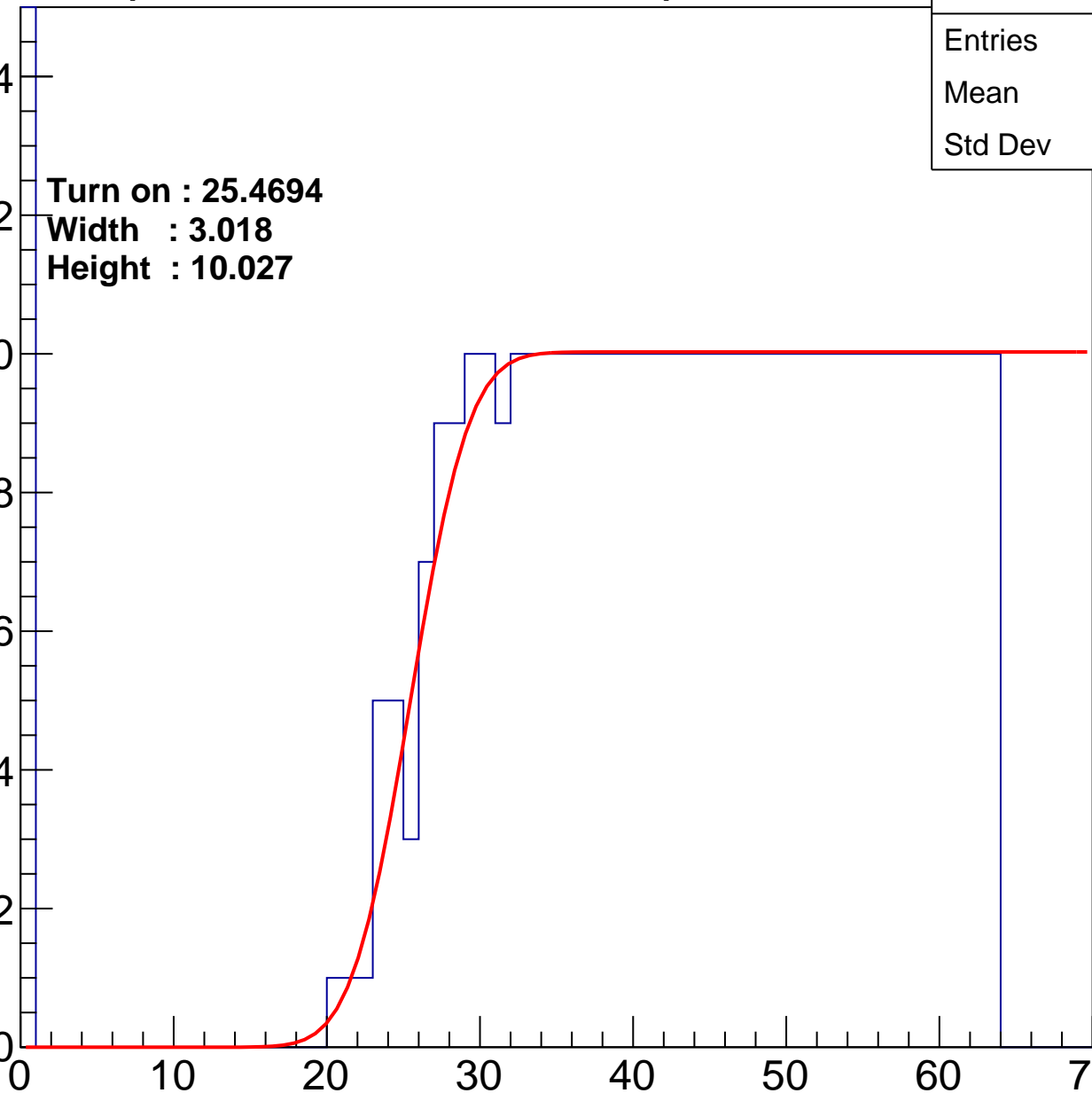
Width : 3.018

Height : 10.027

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch25

calib_packv5_041523_1651.root, FC#0, port C2

Entries	452
Mean	38.23
Std Dev	17.95

Turn on : 24.2413

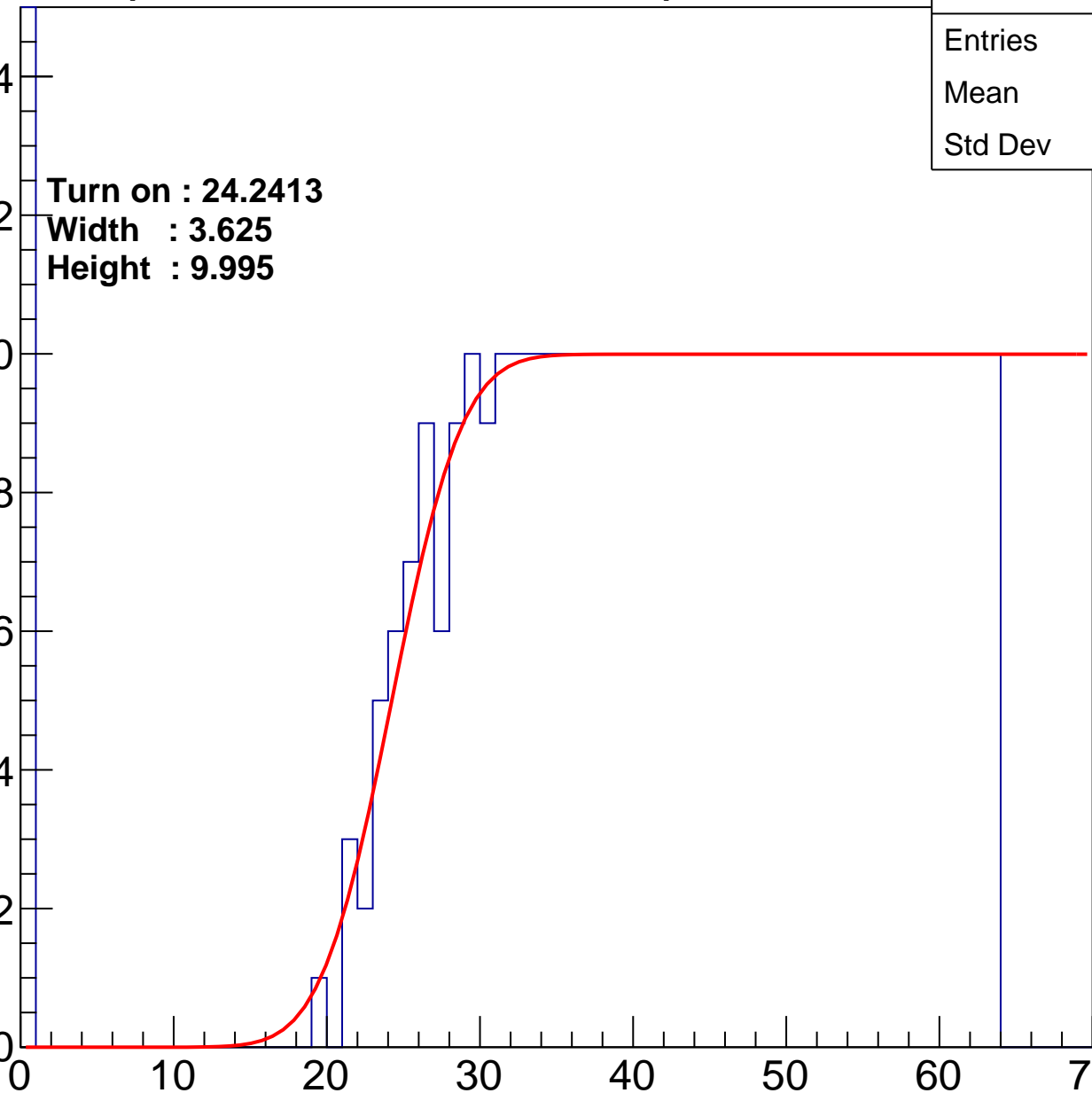
Width : 3.625

Height : 9.995

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch26

calib_packv5_041523_1651.root, FC#0, port C2

Entries	435
Mean	38.97
Std Dev	17.8

Turn on : 25.7971

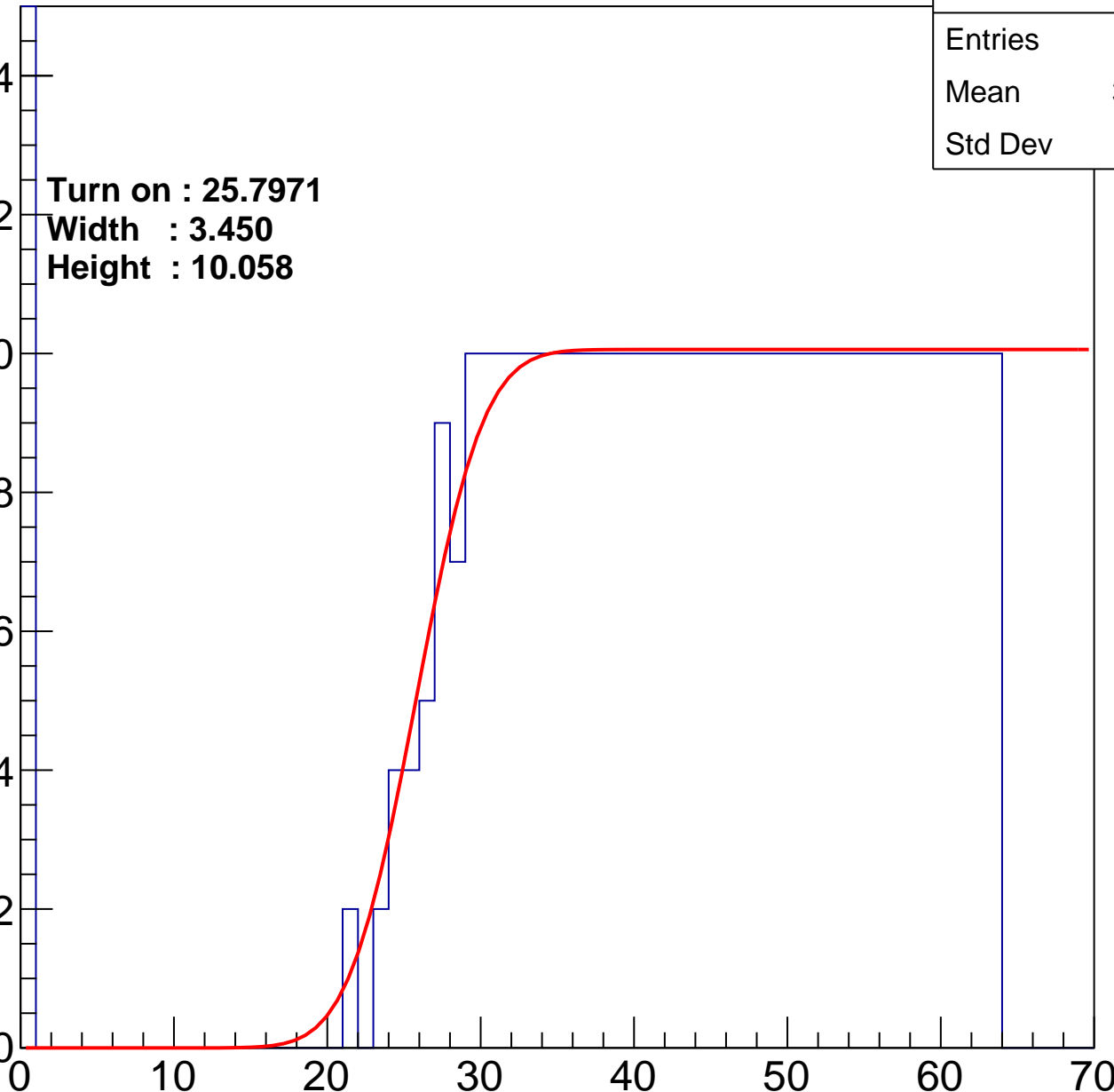
Width : 3.450

Height : 10.058

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch27

calib_packv5_041523_1651.root, FC#0, port C2

Entries	424
Mean	39.67
Std Dev	17.35

Turn on : 26.3817

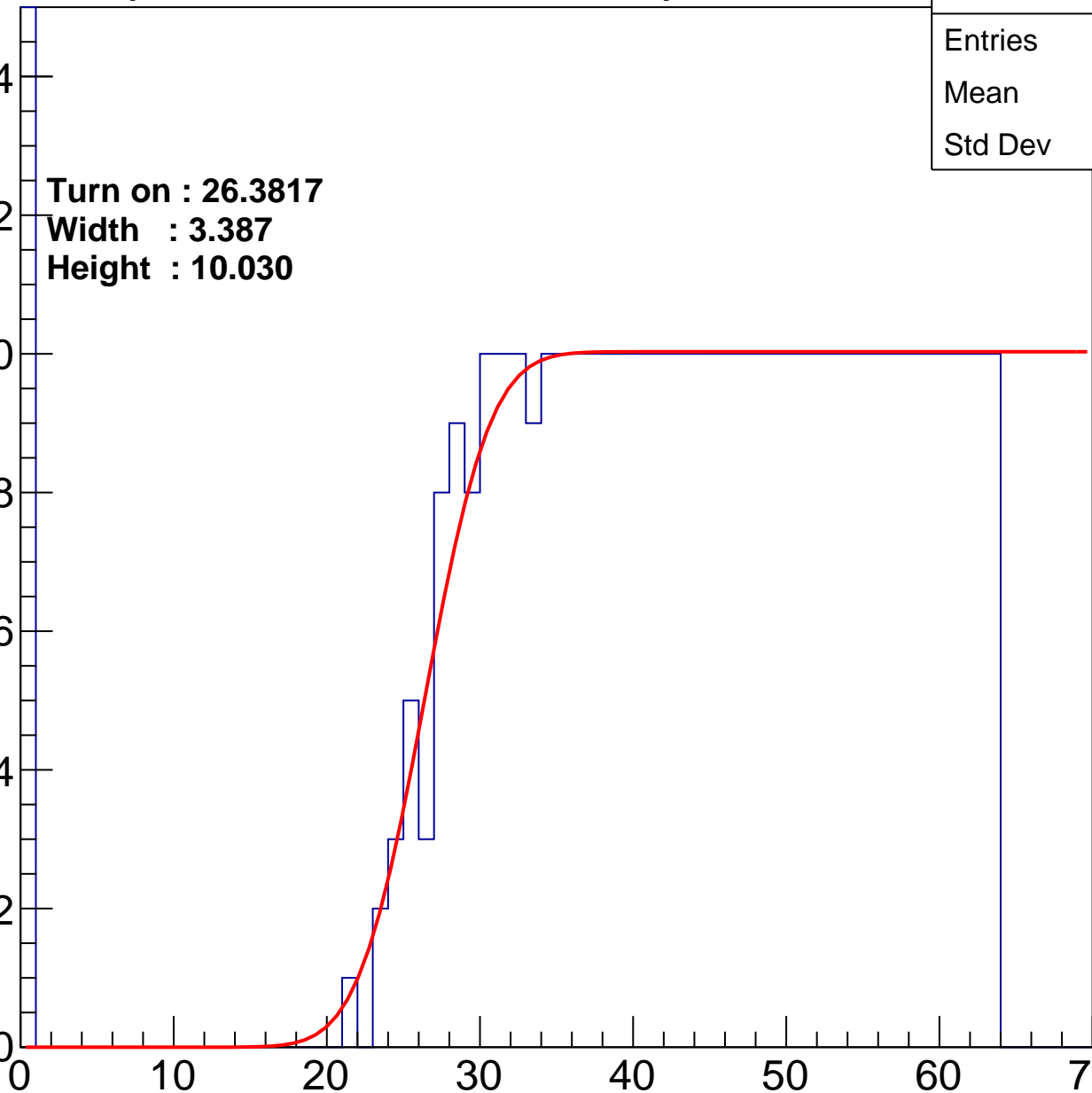
Width : 3.387

Height : 10.030

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch28

calib_packv5_041523_1651.root, FC#0, port C2

Entries	454
Mean	37.76
Std Dev	18.52

Turn on : 24.7893

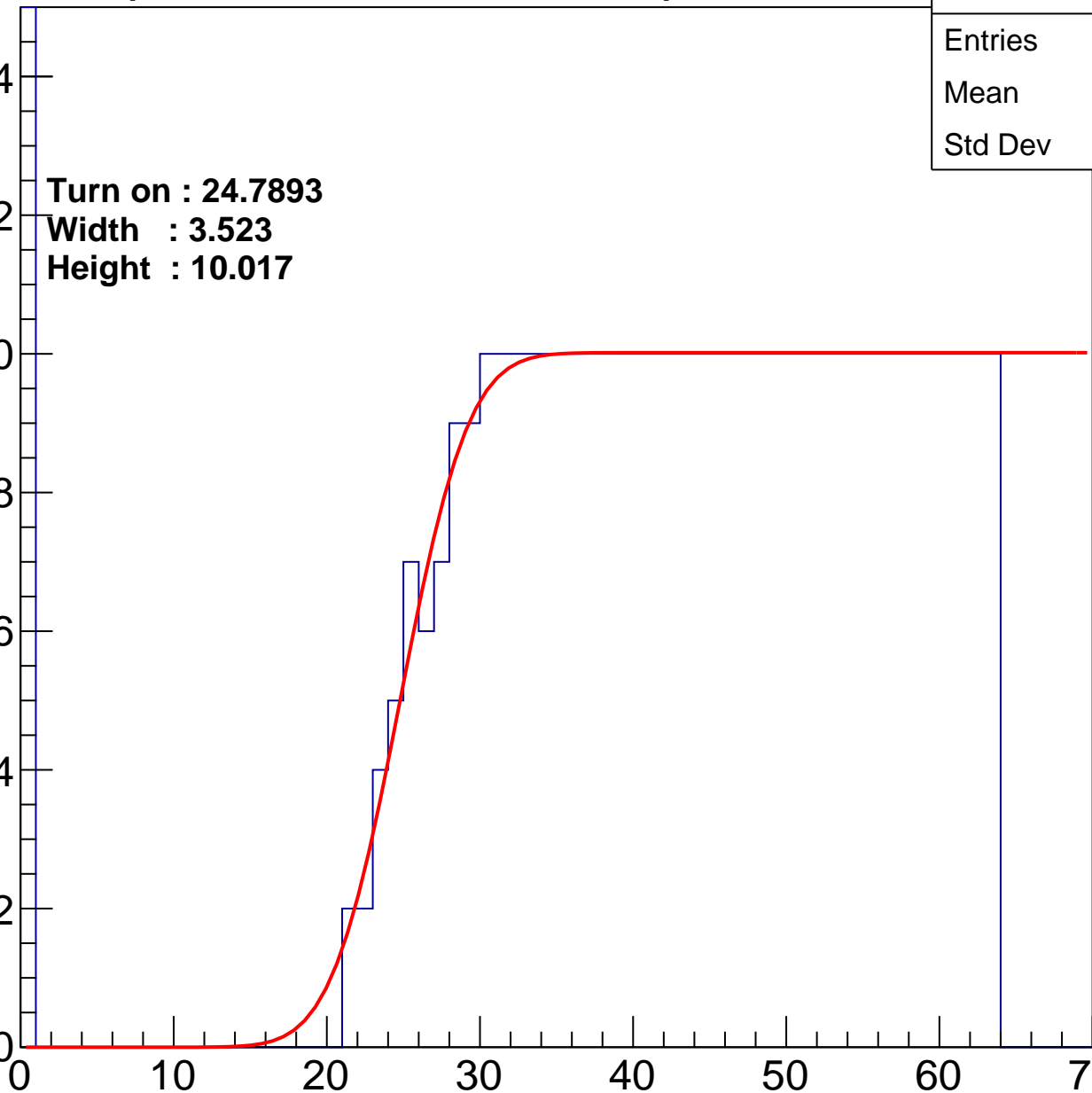
Width : 3.523

Height : 10.017

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch29

calib_packv5_041523_1651.root, FC#0, port C2

Entries	429
Mean	39.55
Std Dev	17.24

Turn on : 25.7326

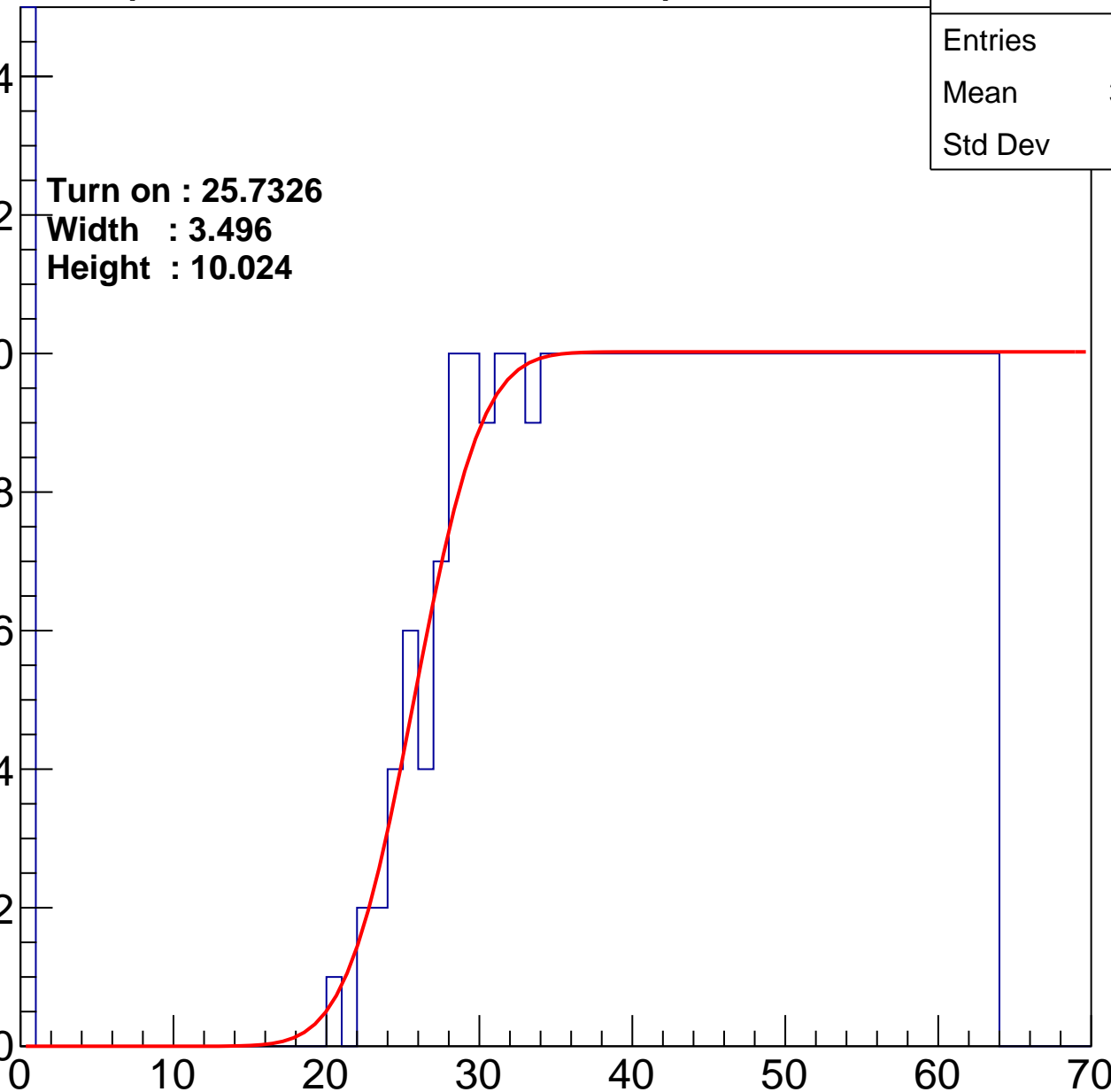
Width : 3.496

Height : 10.024

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch30

calib_packv5_041523_1651.root, FC#0, port C2

Entries	446
Mean	38.85
Std Dev	17.35

Turn on : 24.2574

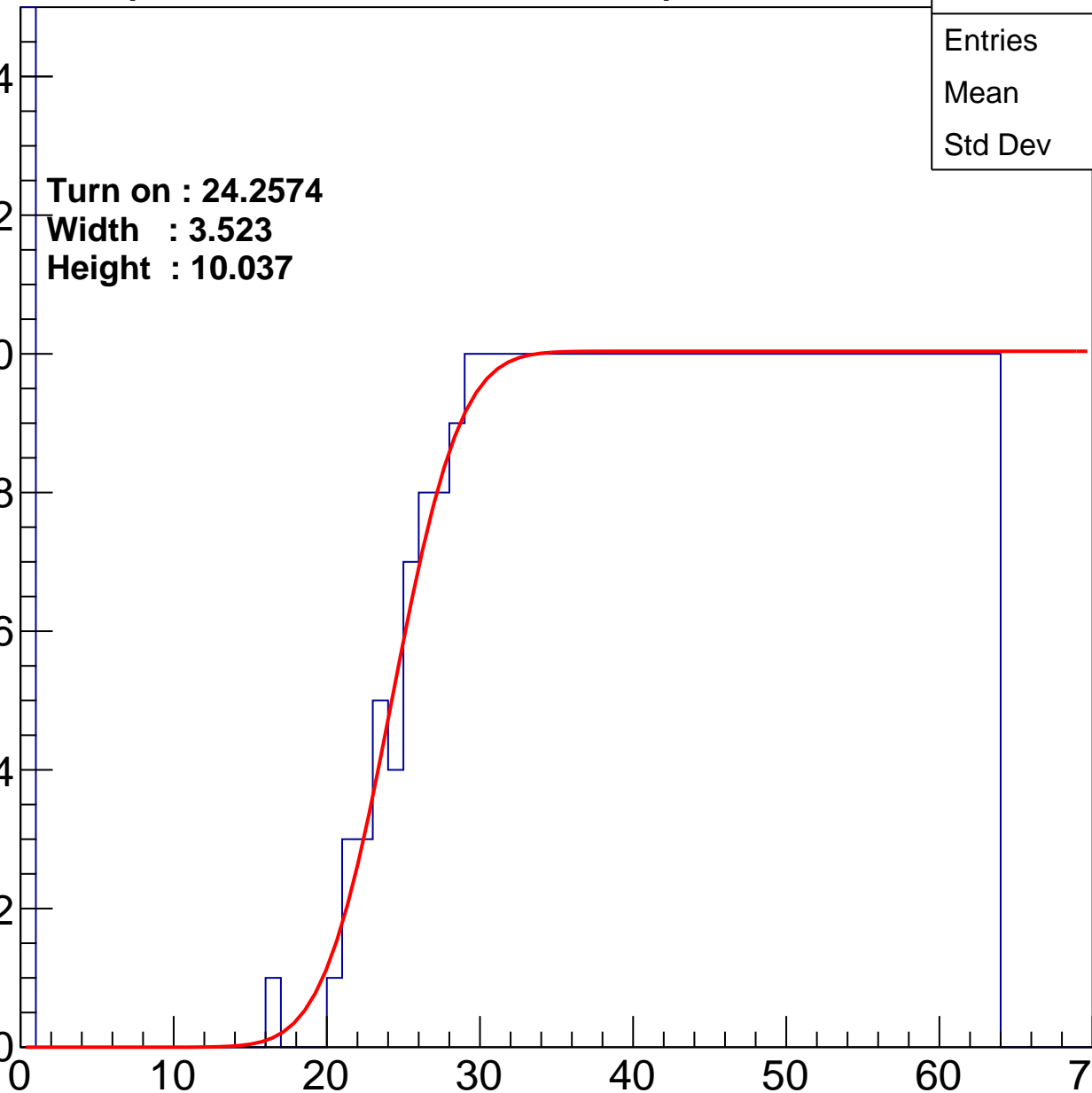
Width : 3.523

Height : 10.037

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch31

calib_packv5_041523_1651.root, FC#0, port C2

Entries	428
Mean	39.78
Std Dev	16.94

Turn on : 25.0779

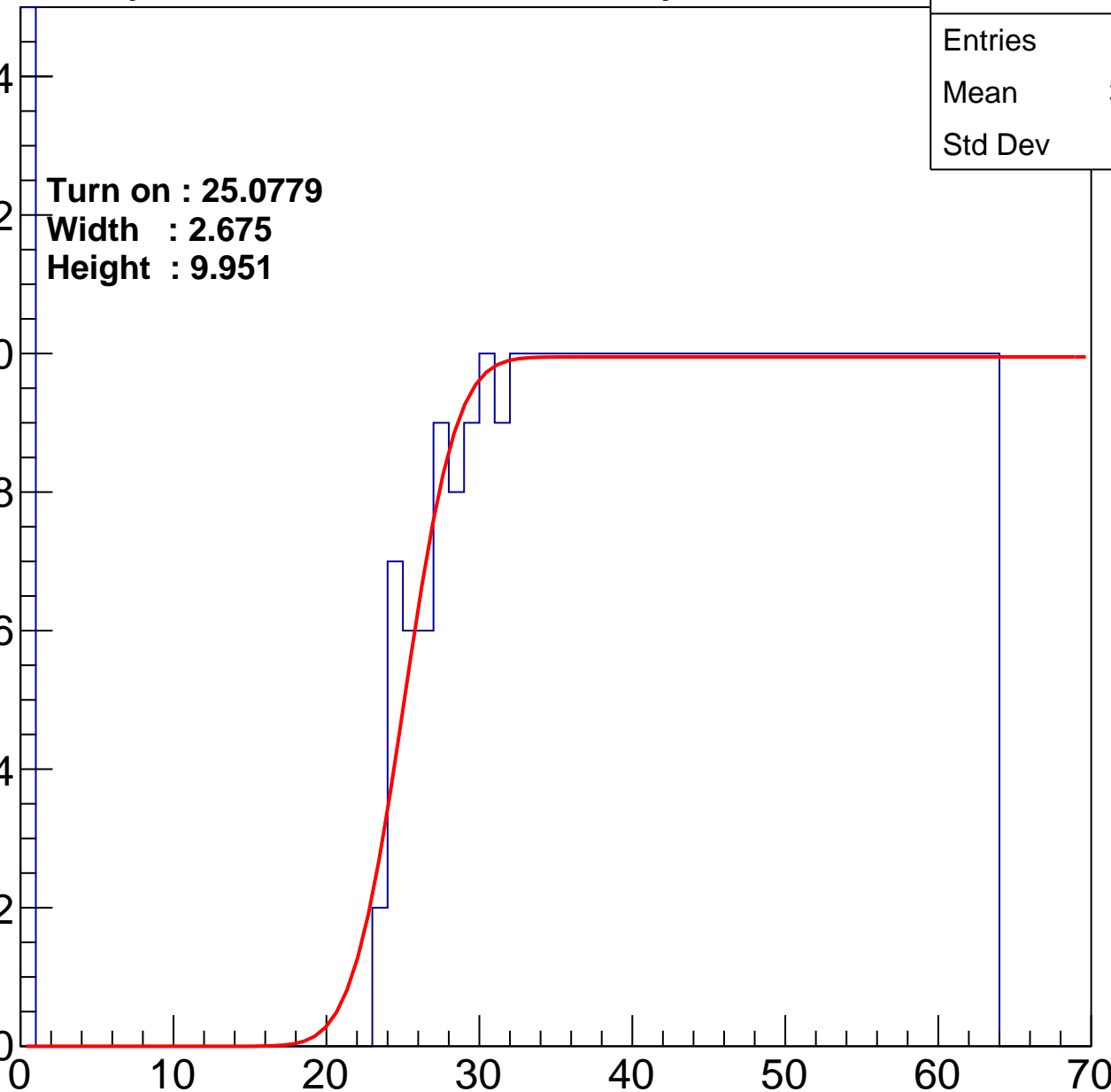
Width : 2.675

Height : 9.951

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch32

calib_packv5_041523_1651.root, FC#0, port C2

Entries	453
Mean	37.87
Std Dev	18.43

Turn on : 24.7325

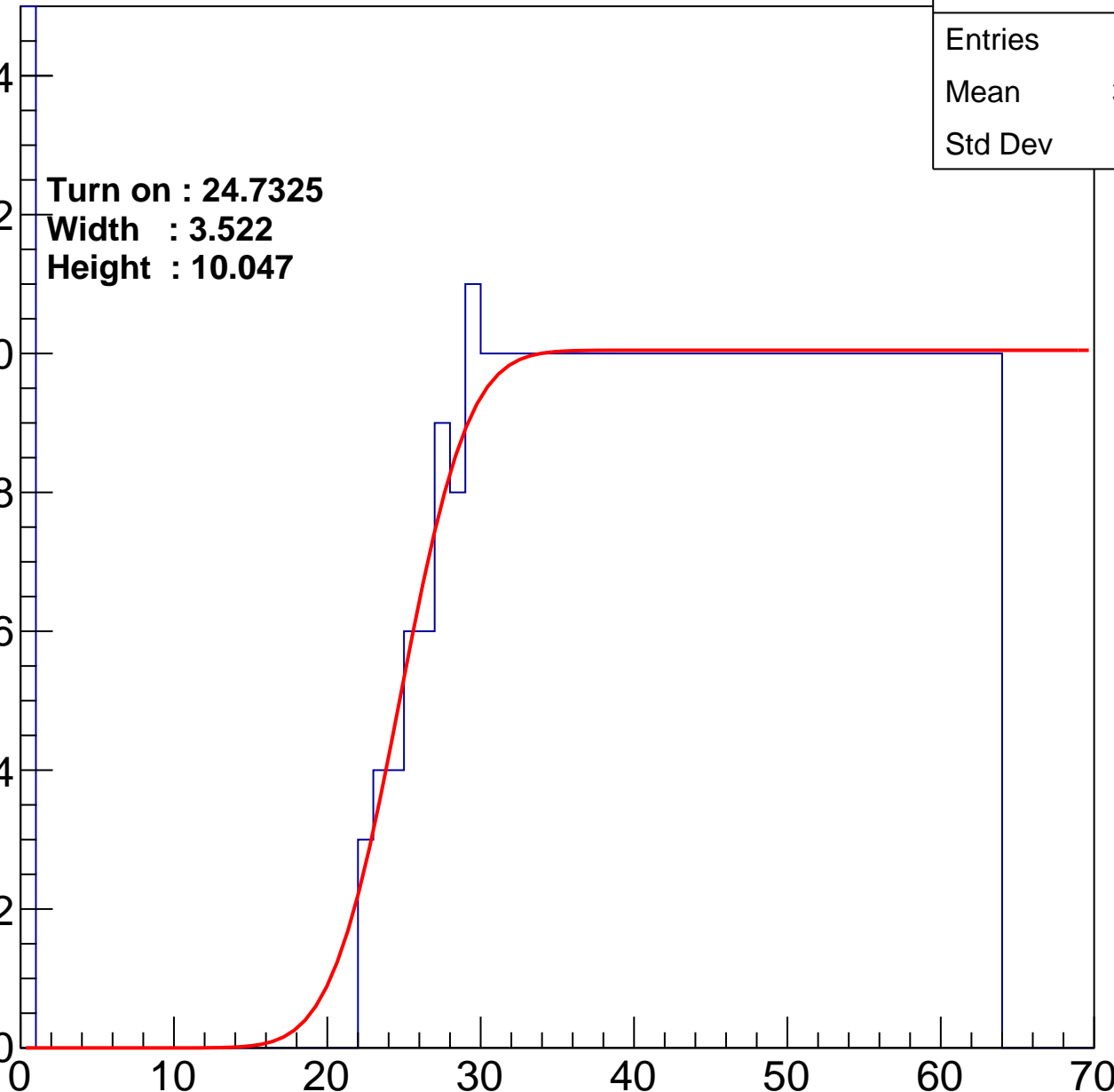
Width : 3.522

Height : 10.047

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch33

calib_packv5_041523_1651.root, FC#0, port C2

Entries	453
Mean	38.63
Std Dev	17.3

Turn on : 23.5128

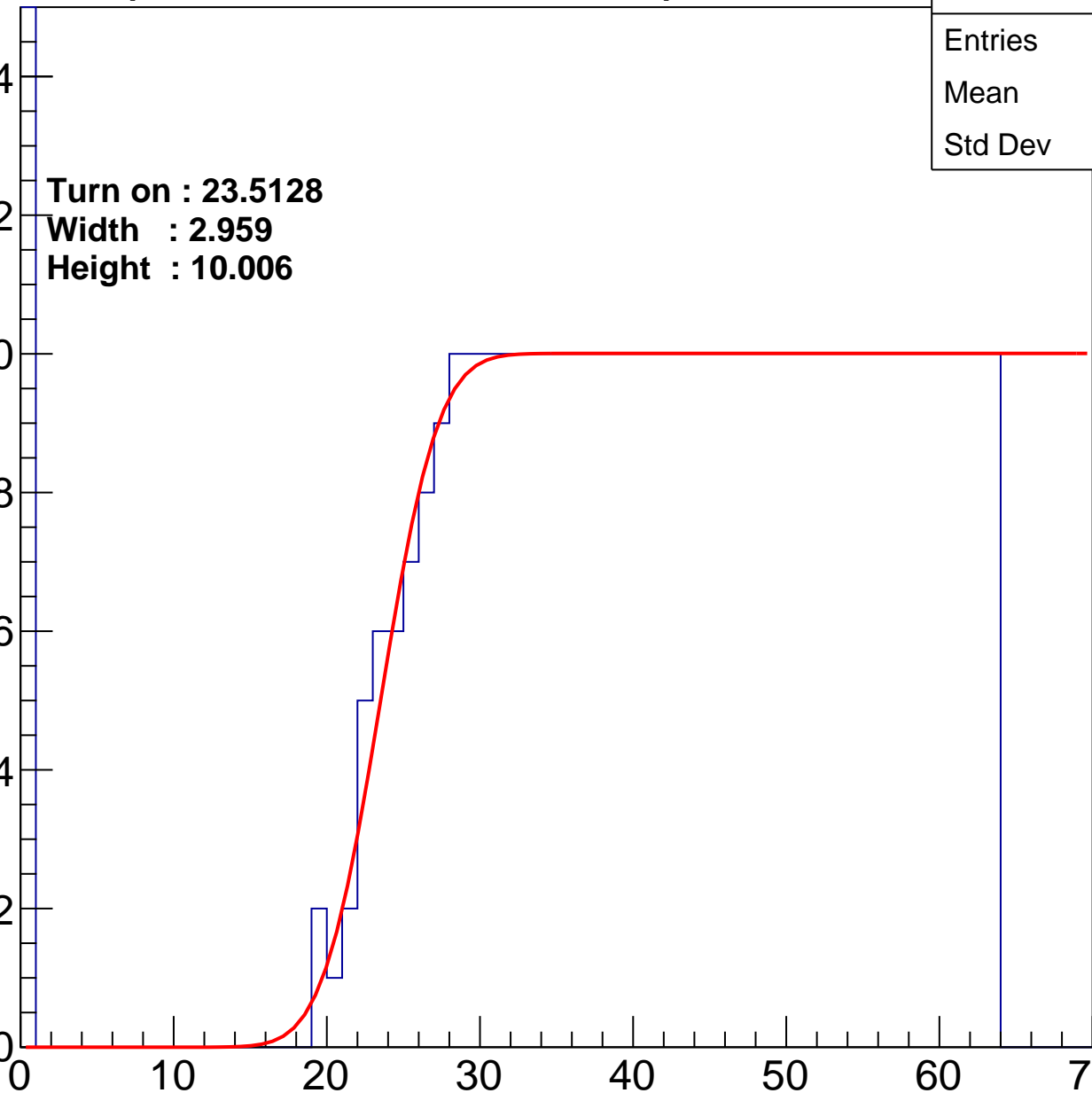
Width : 2.959

Height : 10.006

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch34

calib_packv5_041523_1651.root, FC#0, port C2

Entries	452
Mean	38.03
Std Dev	18.24

Turn on : 24.6307

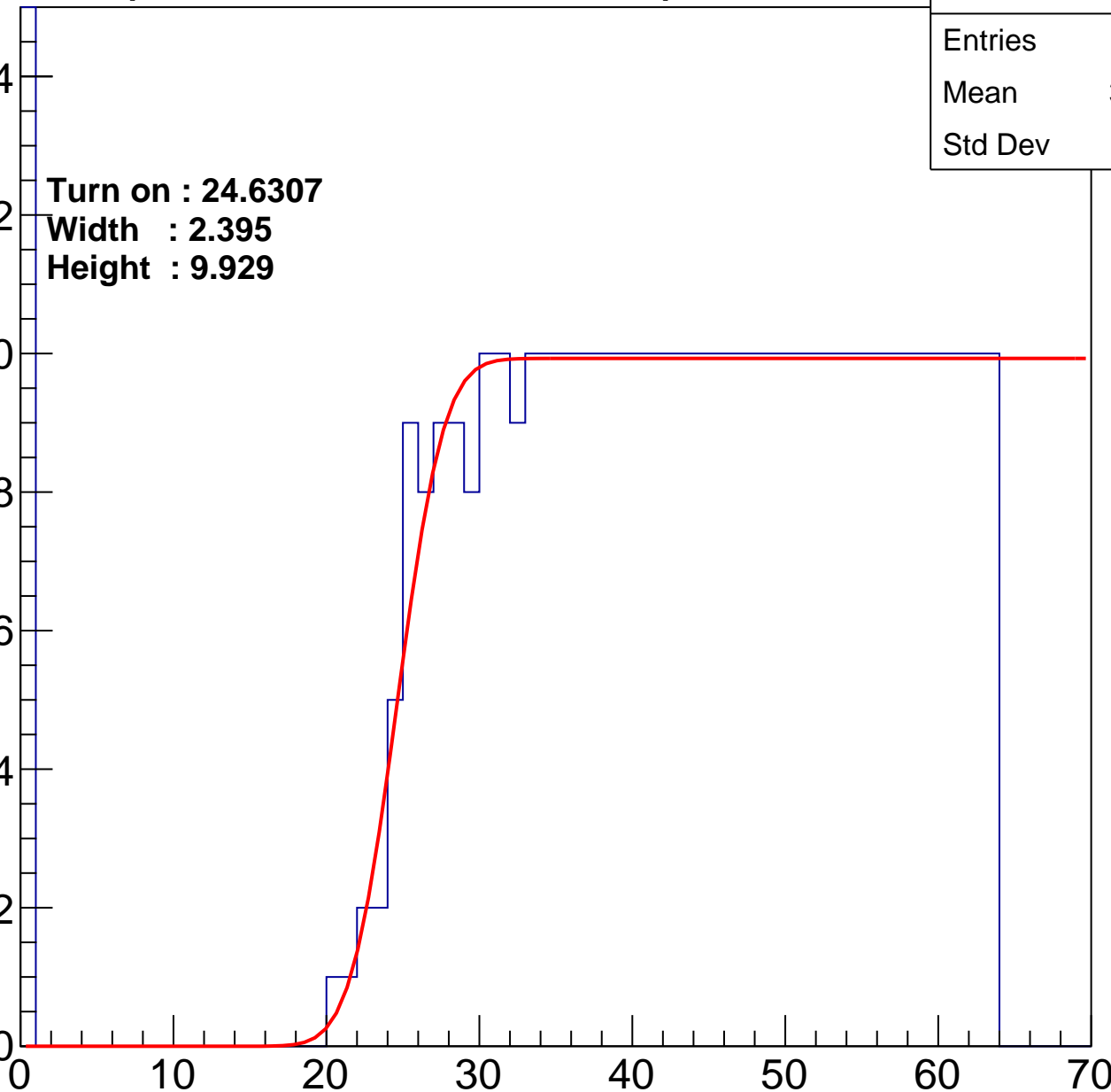
Width : 2.395

Height : 9.929

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch35

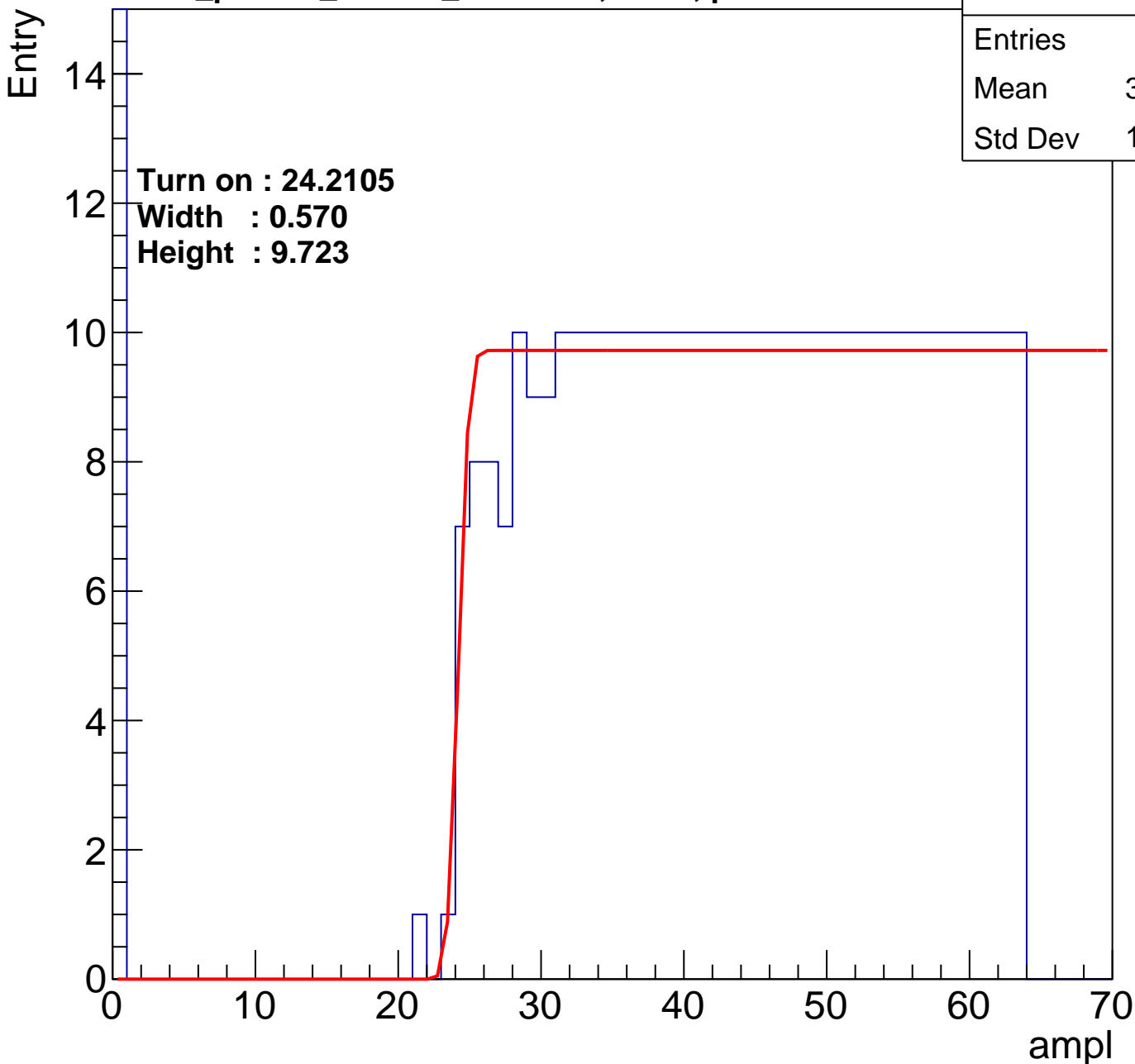
calib_packv5_041523_1651.root, FC#0, port C2

Entries	441
Mean	38.84
Std Dev	17.66

Turn on : 24.2105

Width : 0.570

Height : 9.723



B1L103S, U2-ch36

calib_packv5_041523_1651.root, FC#0, port C2

Entries	449
Mean	37.43
Std Dev	19.22

Turn on : 26.3639

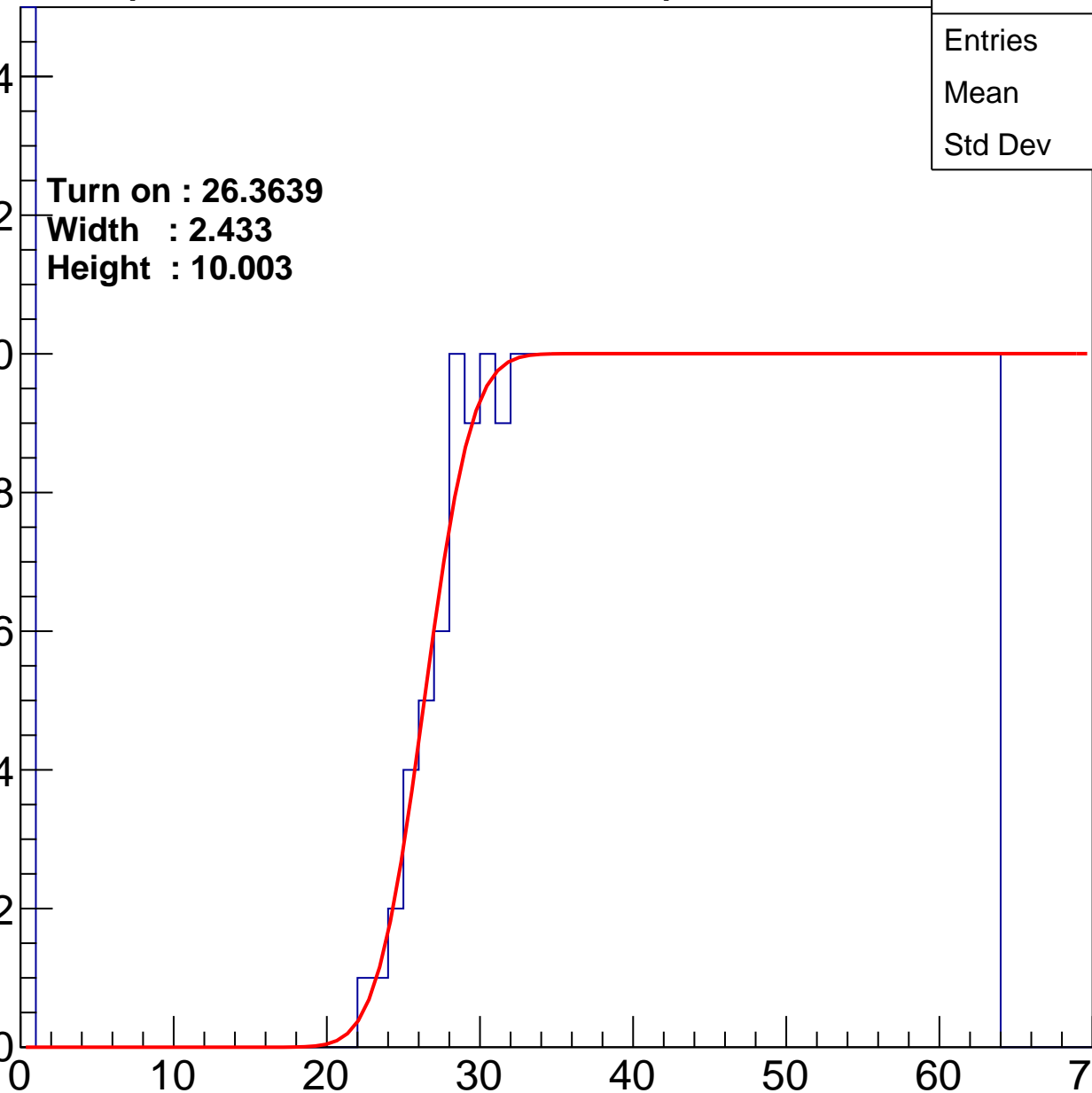
Width : 2.433

Height : 10.003

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch37

calib_packv5_041523_1651.root, FC#0, port C2

Entries	472
Mean	36.63
Std Dev	19.16

Turn on : 24.2879

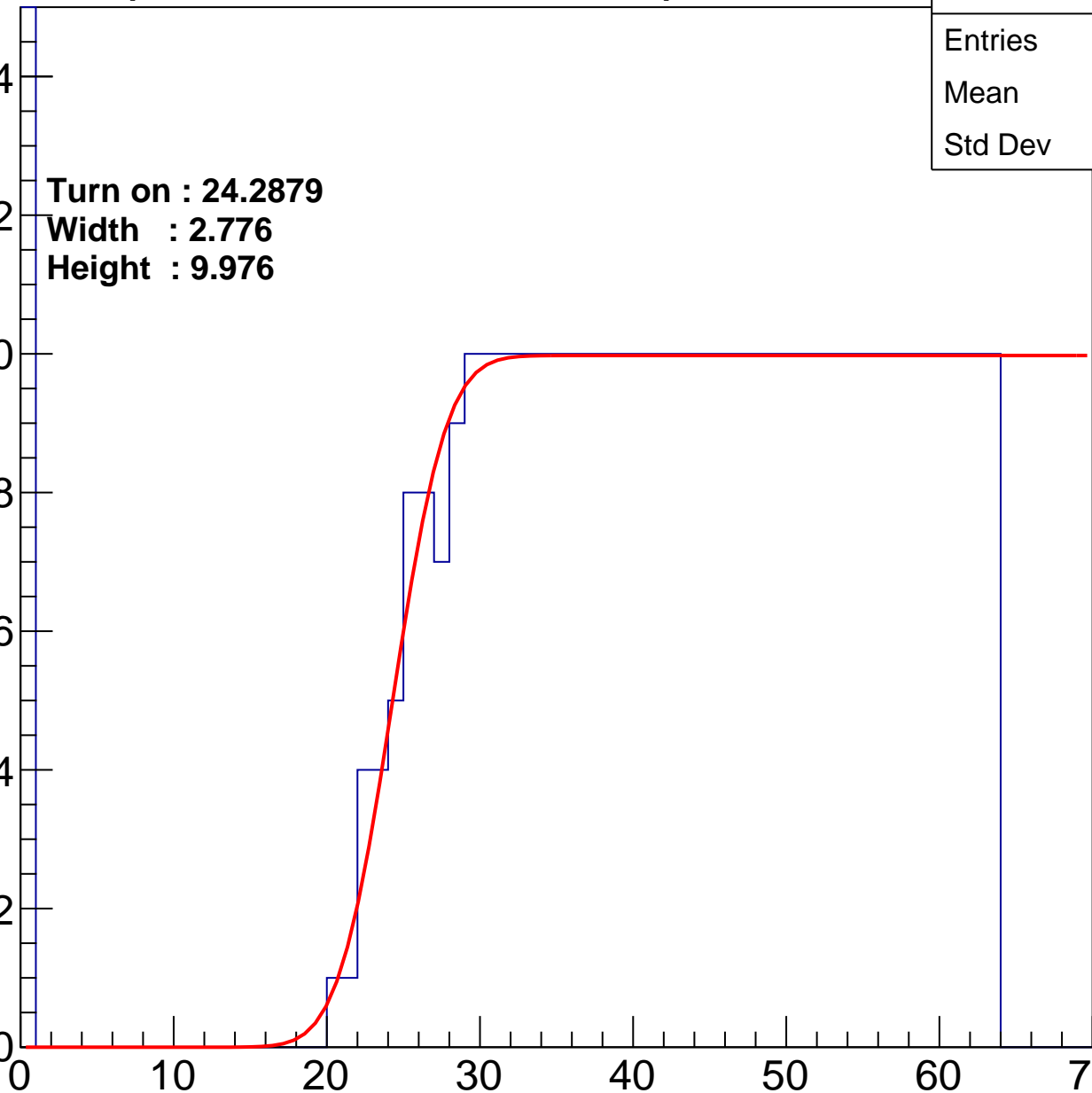
Width : 2.776

Height : 9.976

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch38

calib_packv5_041523_1651.root, FC#0, port C2

Entries	443
Mean	38.52
Std Dev	18.01

Turn on : 25.9609

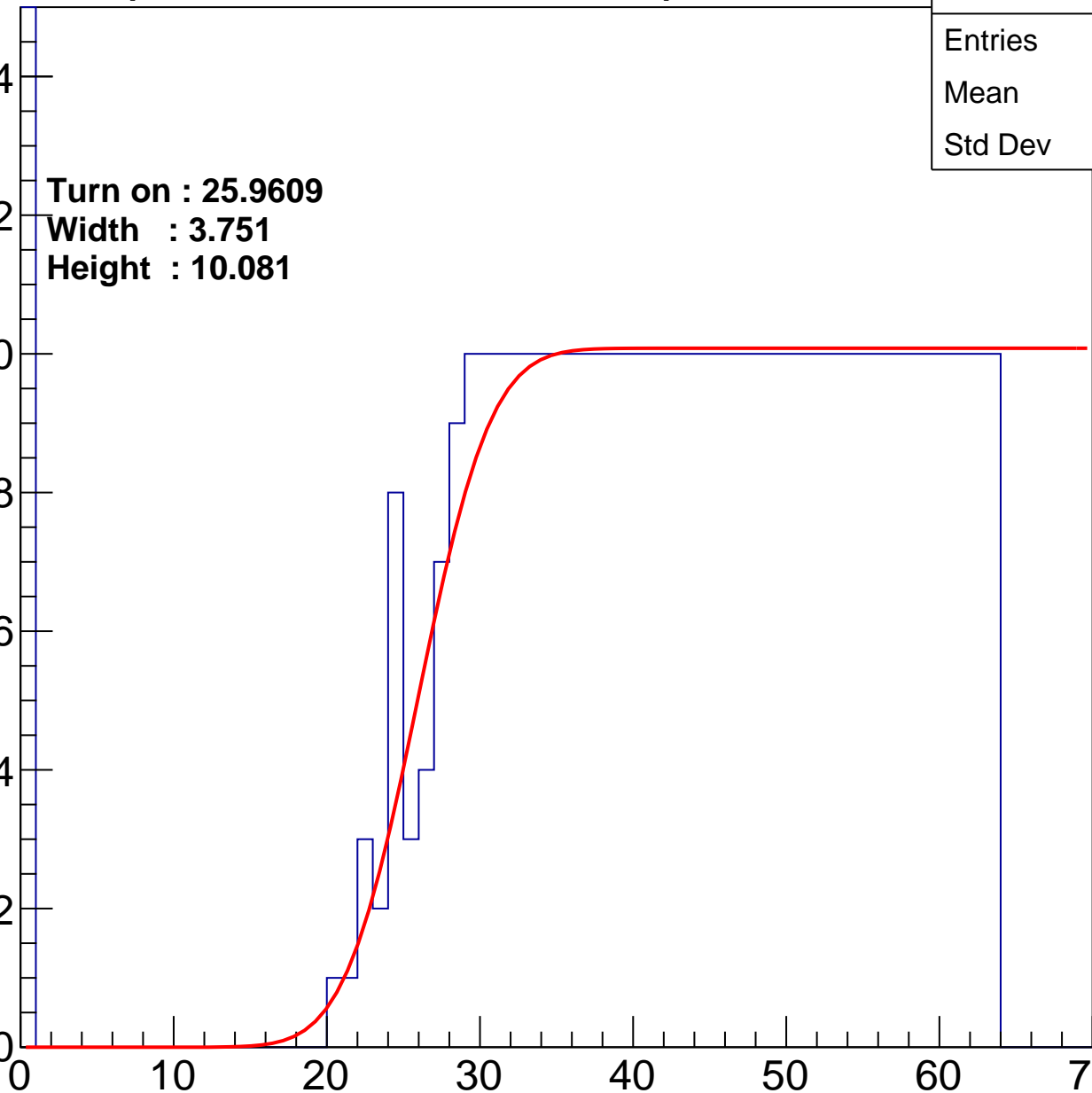
Width : 3.751

Height : 10.081

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch39

calib_packv5_041523_1651.root, FC#0, port C2

Entries	426
Mean	38.64
Std Dev	18.74

Turn on : 27.5601

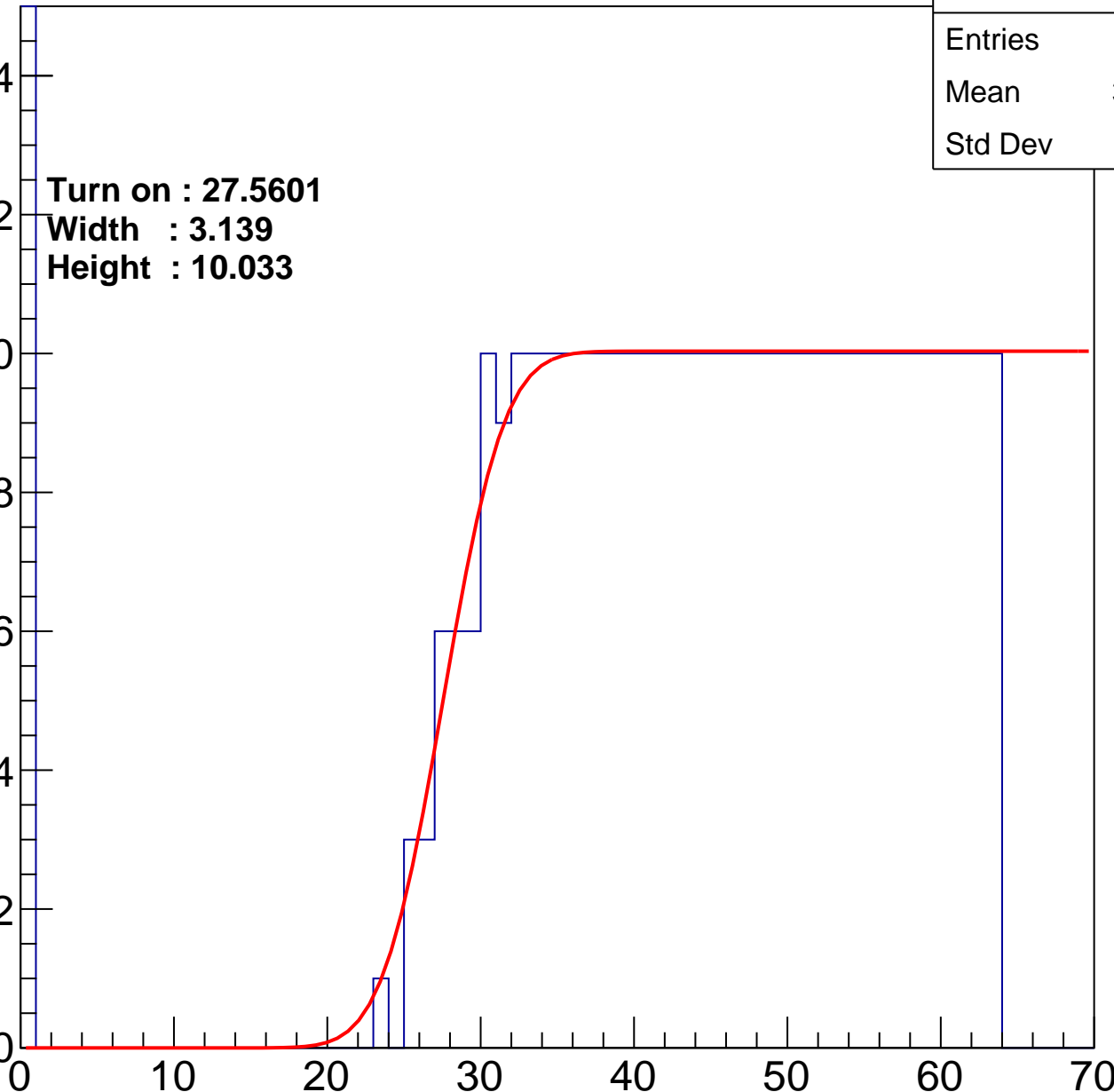
Width : 3.139

Height : 10.033

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch40

calib_packv5_041523_1651.root, FC#0, port C2

Entries	443
Mean	39.17
Std Dev	17.2

Turn on : 25.5391

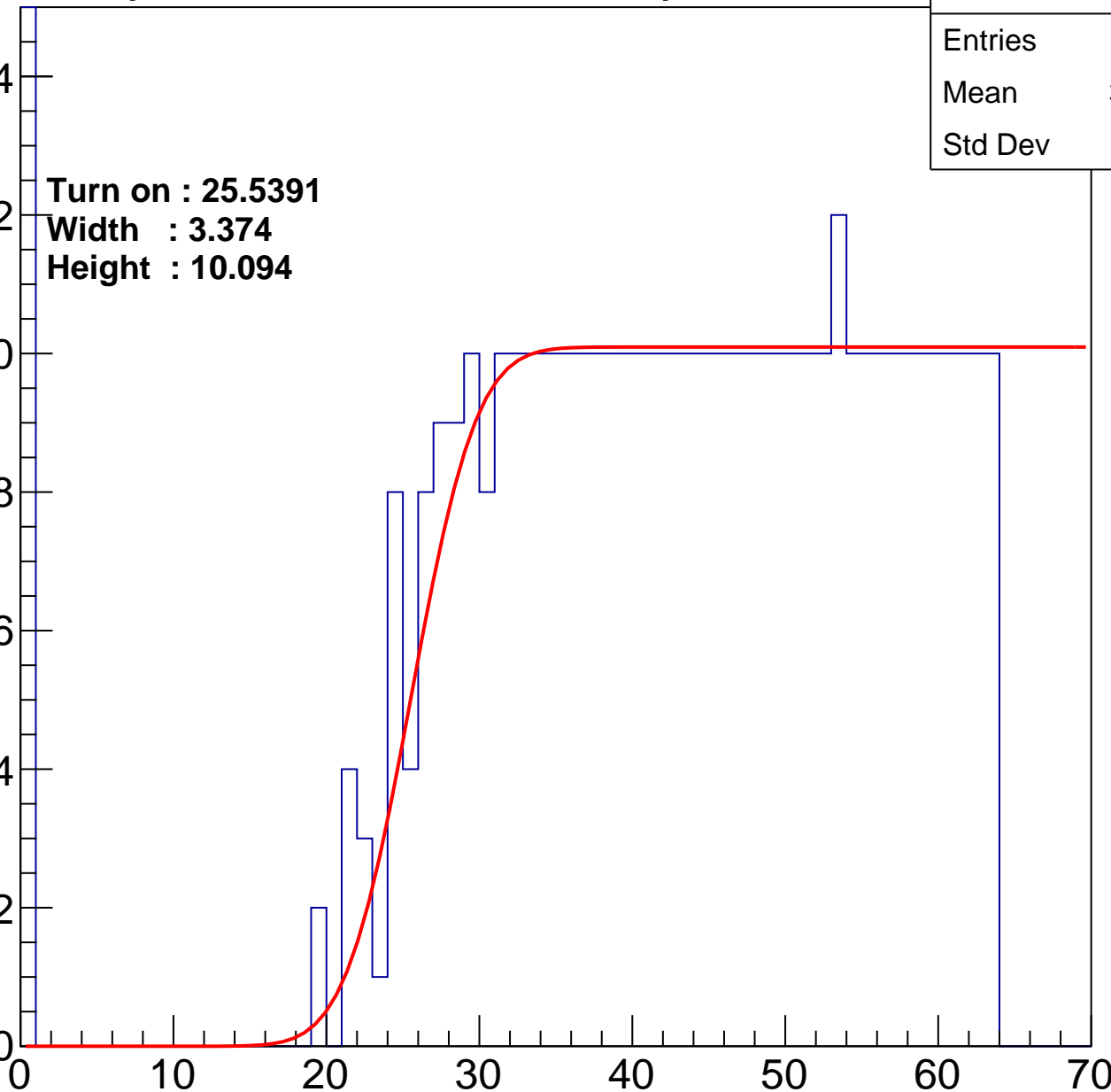
Width : 3.374

Height : 10.094

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch41

calib_packv5_041523_1651.root, FC#0, port C2

Entries	455
Mean	36.91
Std Dev	19.55

Turn on : 27.2058

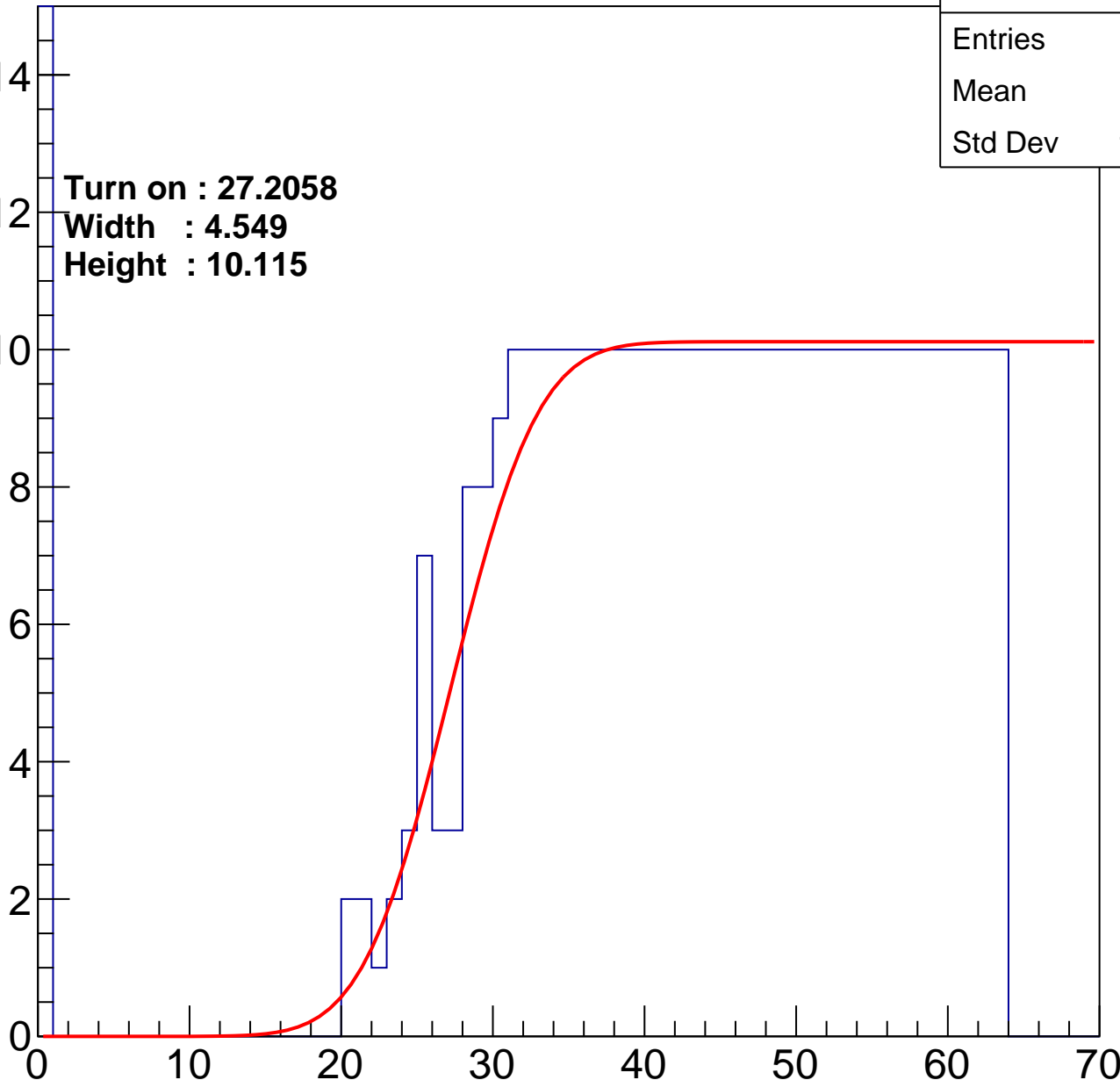
Width : 4.549

Height : 10.115

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch42

calib_packv5_041523_1651.root, FC#0, port C2

Entries	431
Mean	38.77
Std Dev	18.32

Turn on : 26.2514

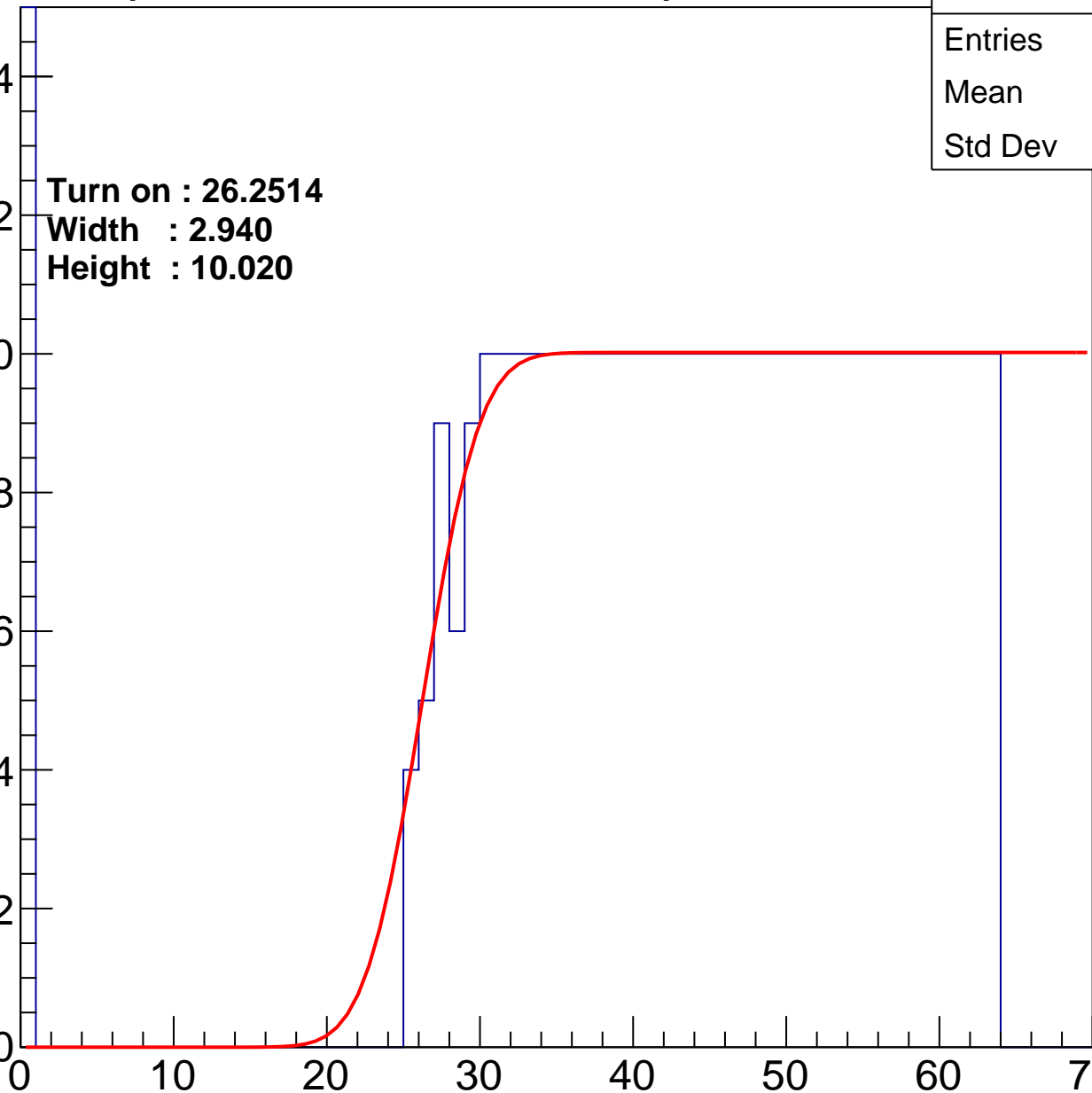
Width : 2.940

Height : 10.020

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch43

calib_packv5_041523_1651.root, FC#0, port C2

Entries	434
Mean	38.86
Std Dev	18

Turn on : 26.3259

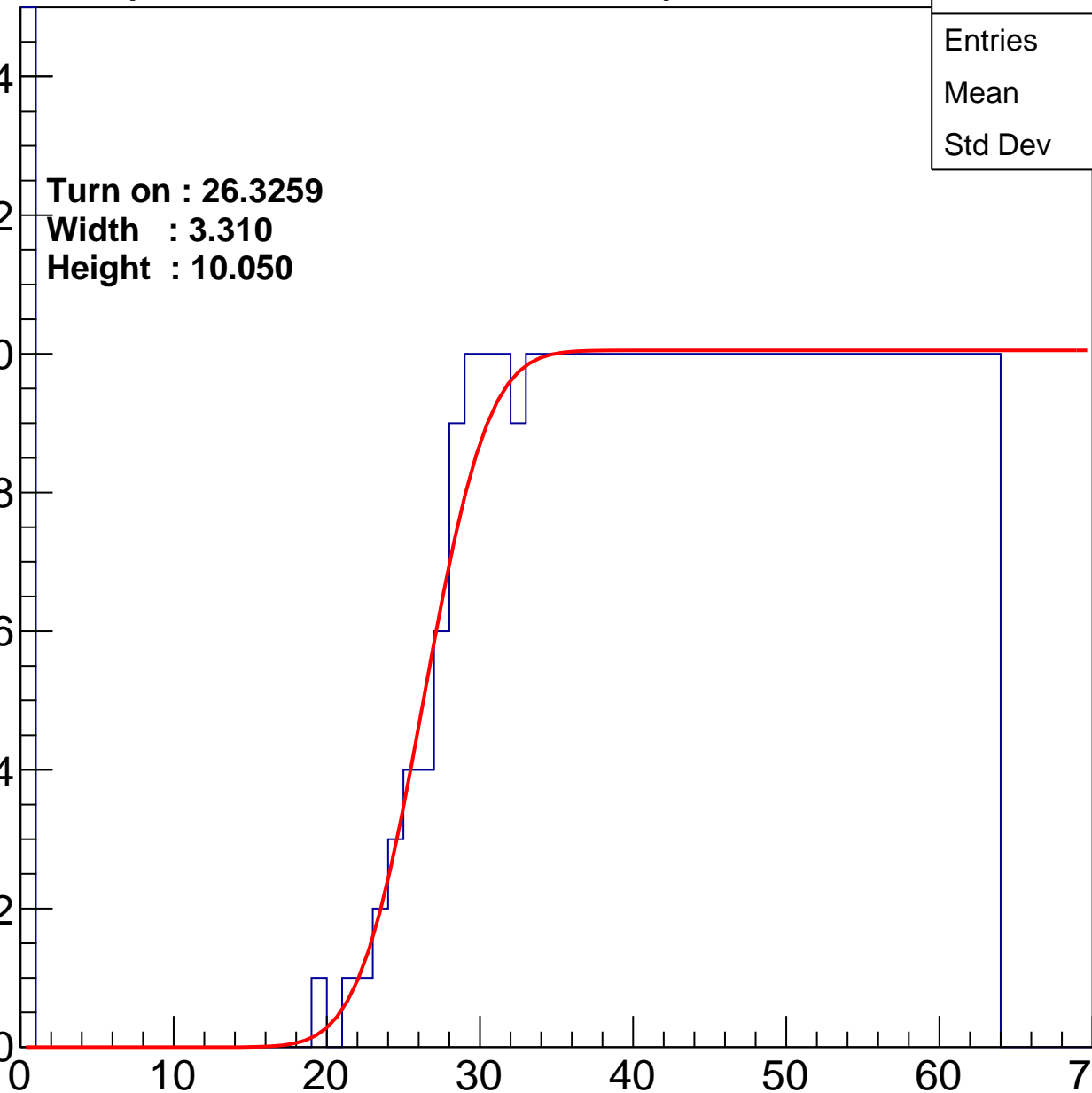
Width : 3.310

Height : 10.050

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch44

calib_packv5_041523_1651.root, FC#0, port C2

Entries	446
Mean	37.81
Std Dev	18.84

Turn on : 26.8545

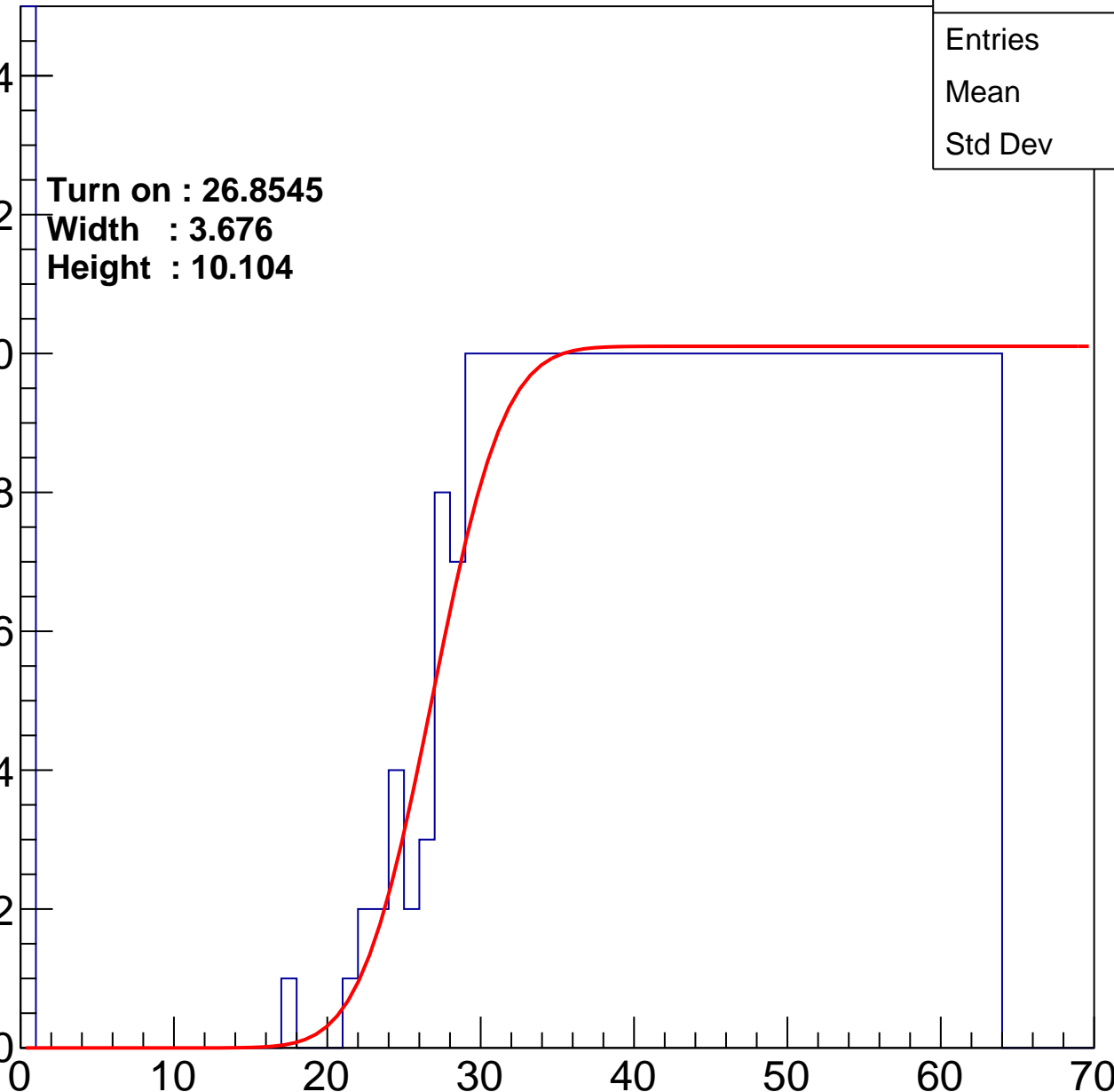
Width : 3.676

Height : 10.104

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch45

calib_packv5_041523_1651.root, FC#0, port C2

Entries	426
Mean	39.35
Std Dev	17.68

Turn on : 27.1958

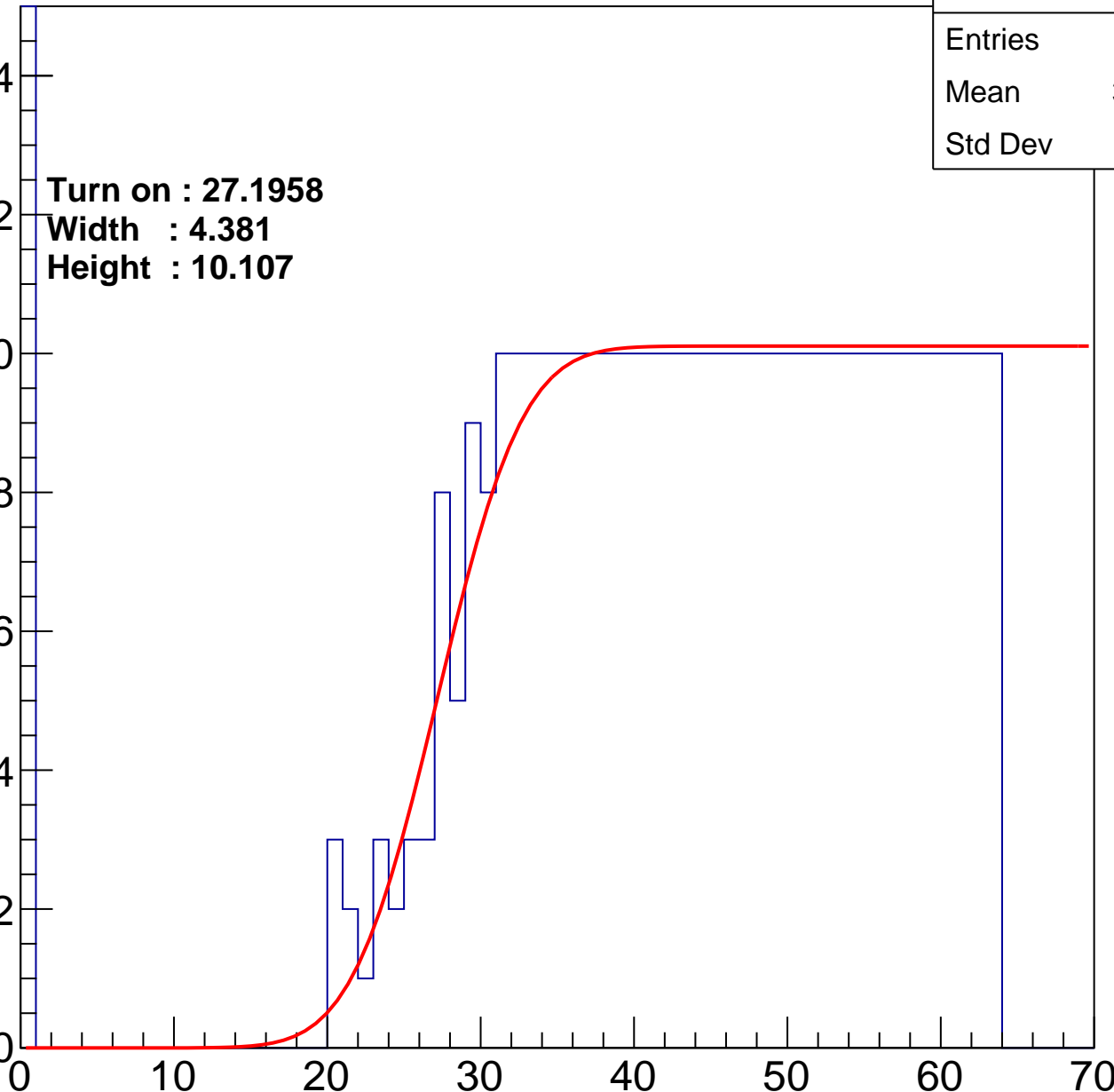
Width : 4.381

Height : 10.107

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch46

calib_packv5_041523_1651.root, FC#0, port C2

Entries	432
Mean	39.25
Std Dev	17.51

Turn on : 25.8537

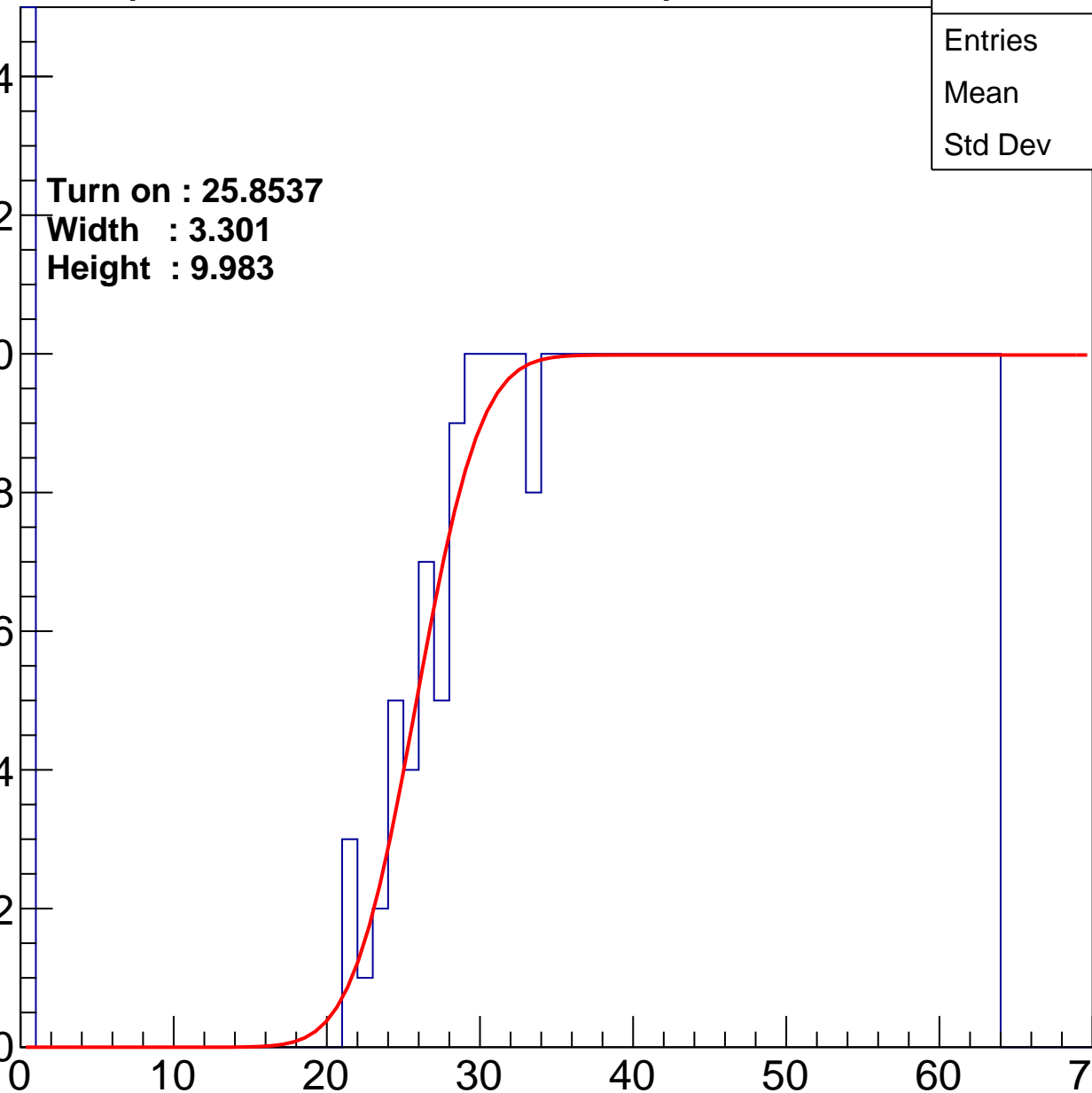
Width : 3.301

Height : 9.983

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch47

calib_packv5_041523_1651.root, FC#0, port C2

Entries	409
Mean	41.23
Std Dev	15.72

Turn on : 25.9720

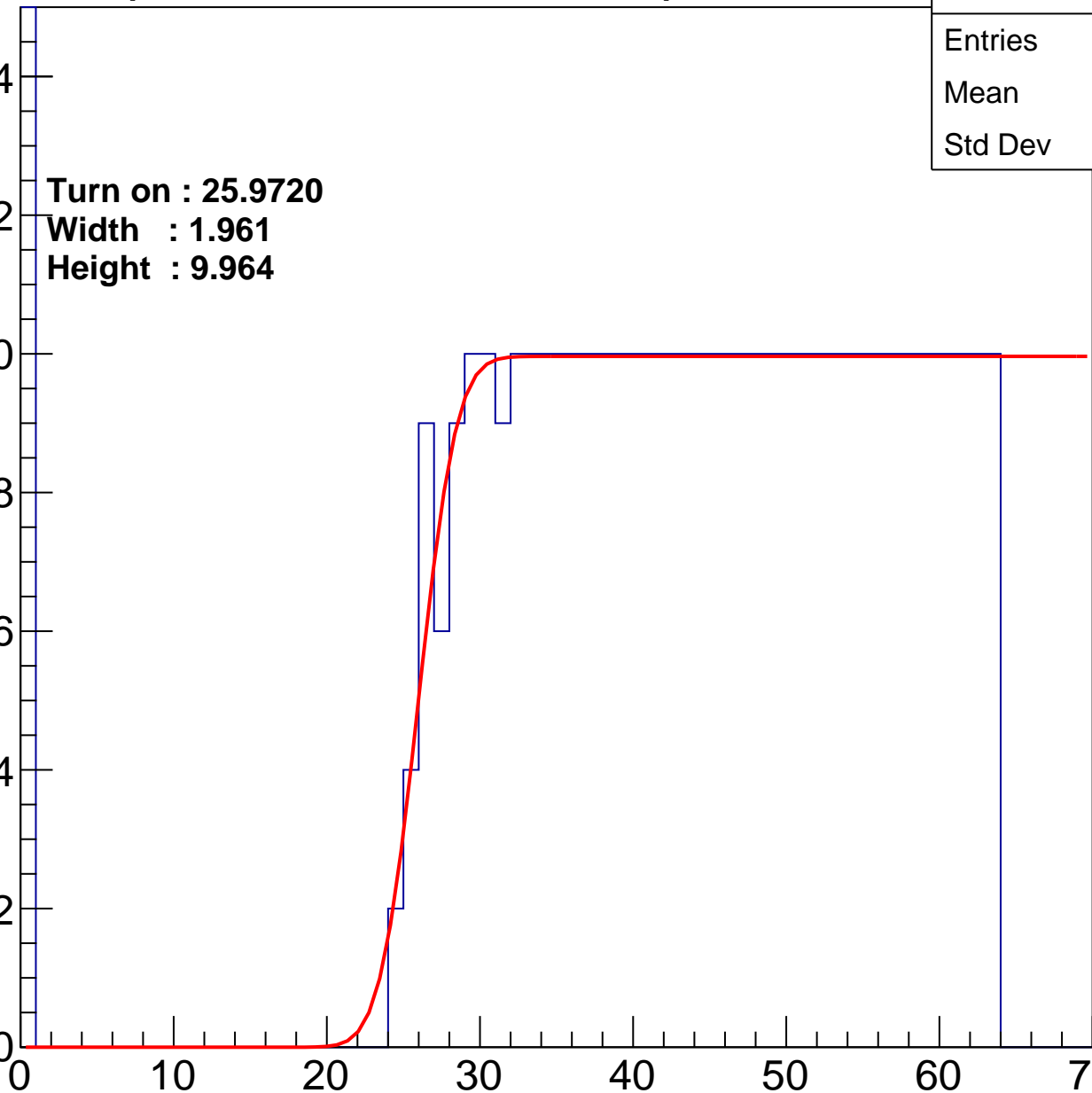
Width : 1.961

Height : 9.964

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch48

calib_packv5_041523_1651.root, FC#0, port C2

Entries	436
Mean	38.62
Std Dev	18.18

Turn on : 25.8285

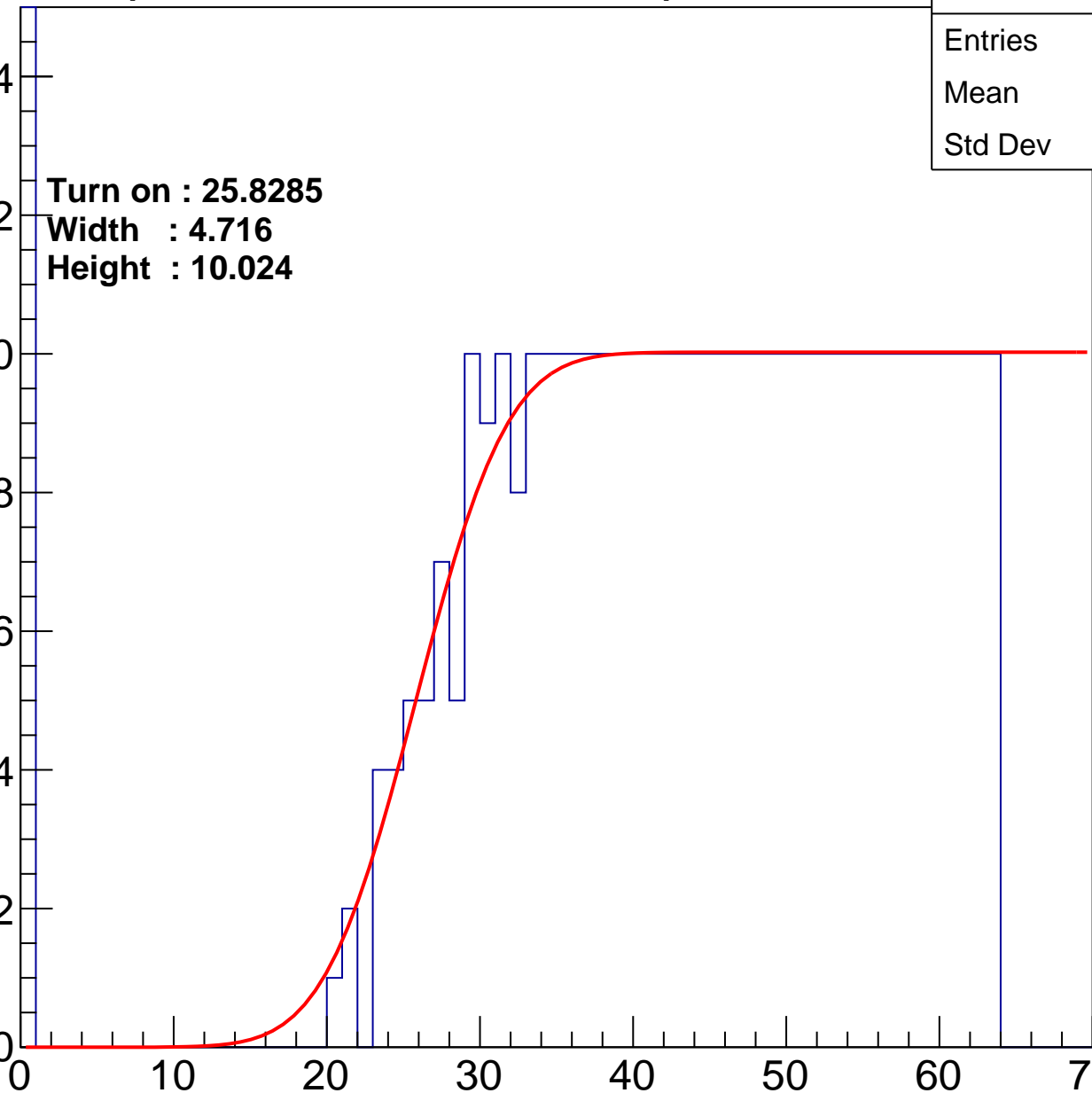
Width : 4.716

Height : 10.024

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch49

calib_packv5_041523_1651.root, FC#0, port C2

Entries	438
Mean	38.59
Std Dev	18.19

Turn on : 25.9864

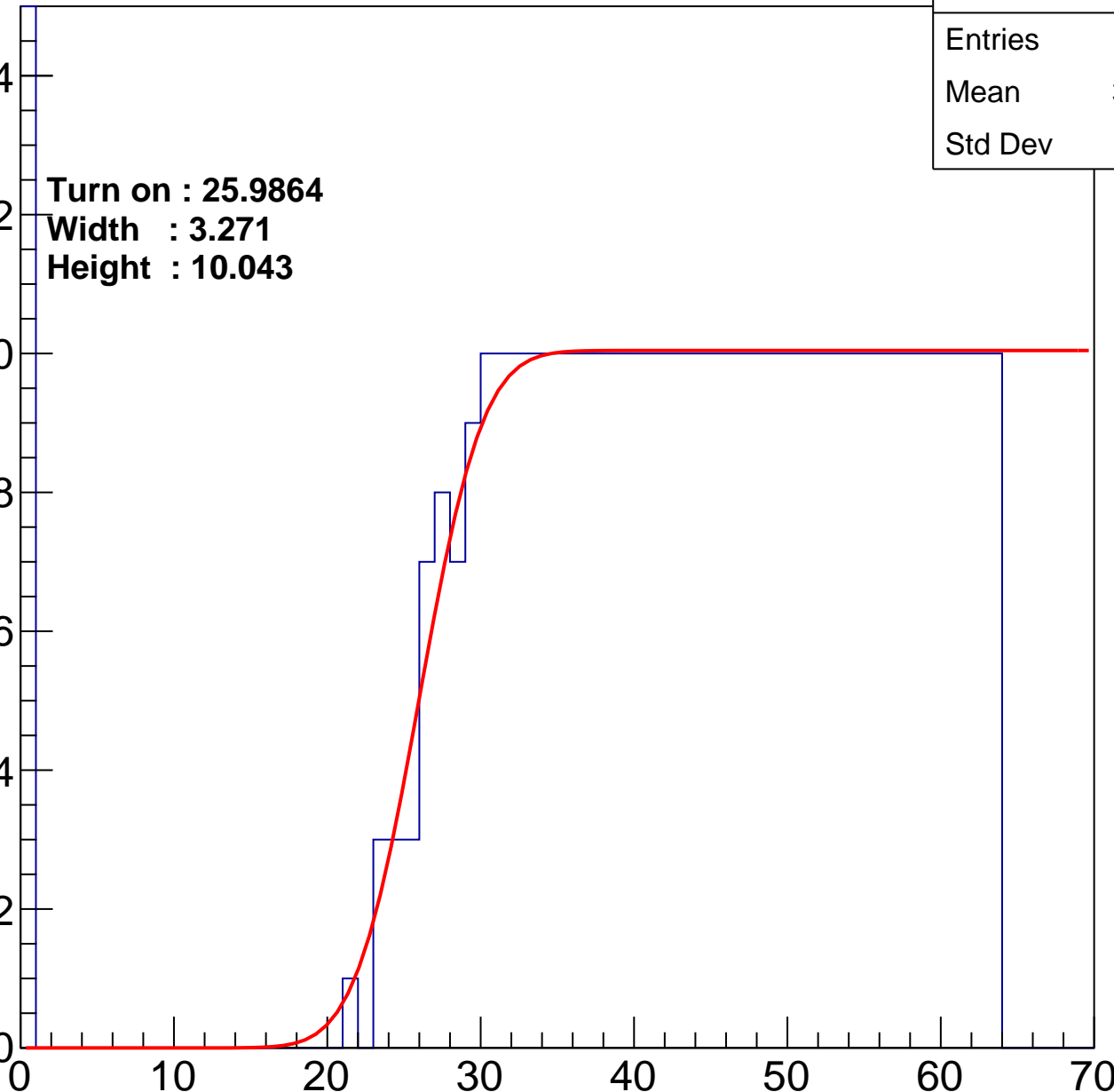
Width : 3.271

Height : 10.043

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch50

calib_packv5_041523_1651.root, FC#0, port C2

Entries	457
Mean	37.46
Std Dev	18.78

Turn on : 24.8690

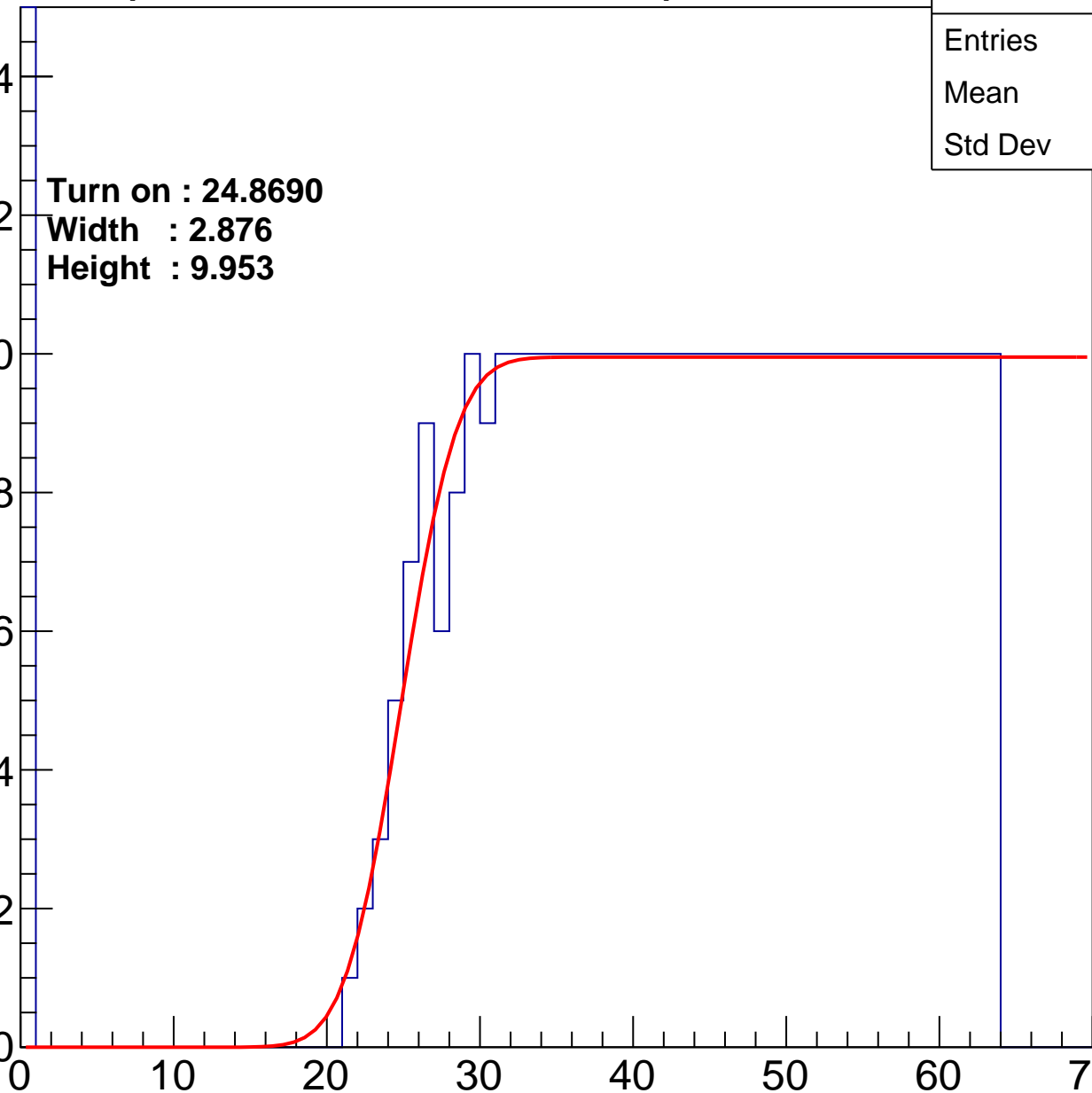
Width : 2.876

Height : 9.953

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch51

calib_packv5_041523_1651.root, FC#0, port C2

Entries	427
Mean	39.64
Std Dev	17.24

Turn on : 26.1757

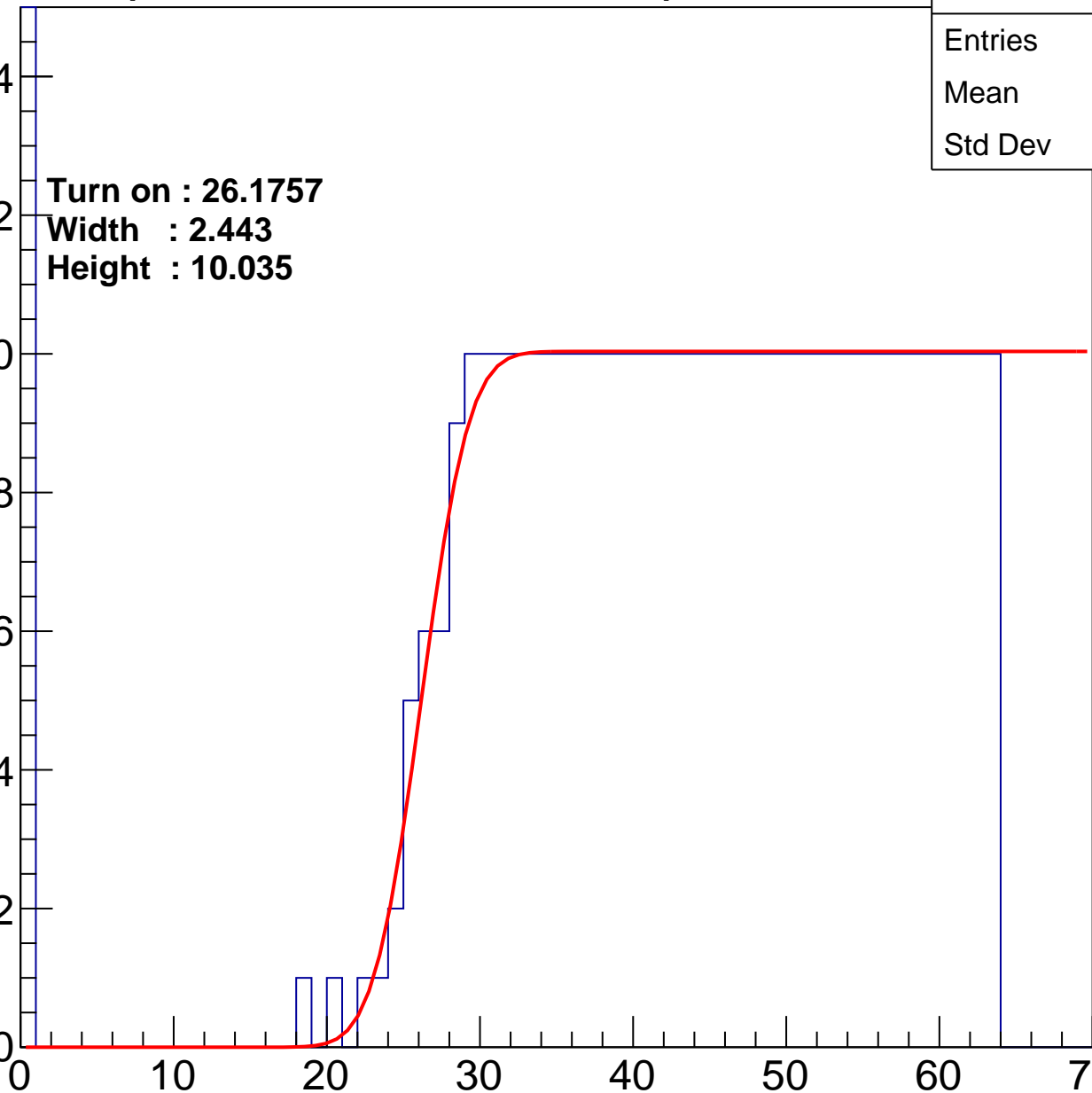
Width : 2.443

Height : 10.035

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch52

calib_packv5_041523_1651.root, FC#0, port C2

Entries	440
Mean	38.27
Std Dev	18.51

Turn on : 26.4700

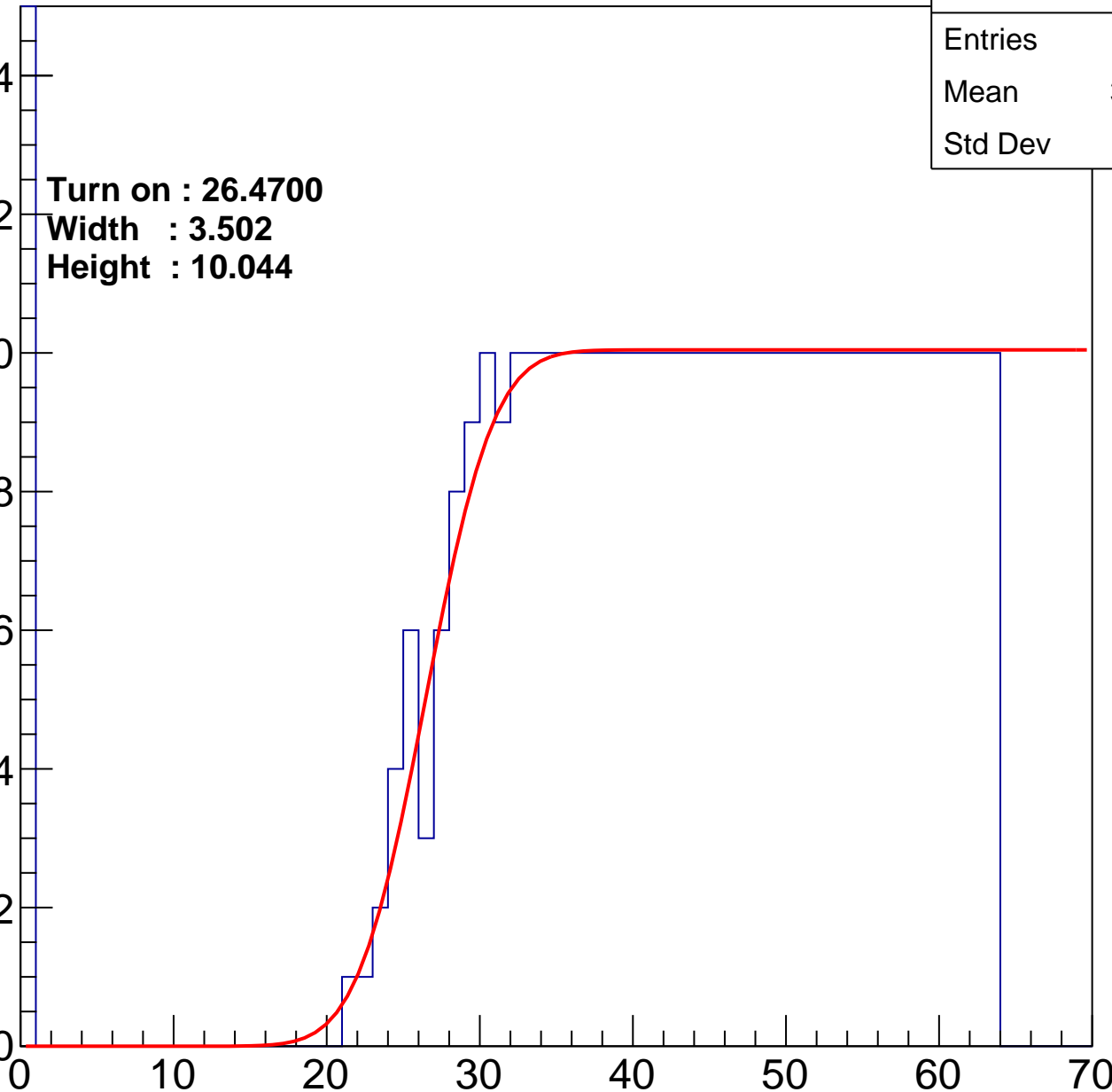
Width : 3.502

Height : 10.044

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch53

calib_packv5_041523_1651.root, FC#0, port C2

Entries	434
Mean	38.78
Std Dev	18.09

Turn on : 27.1104

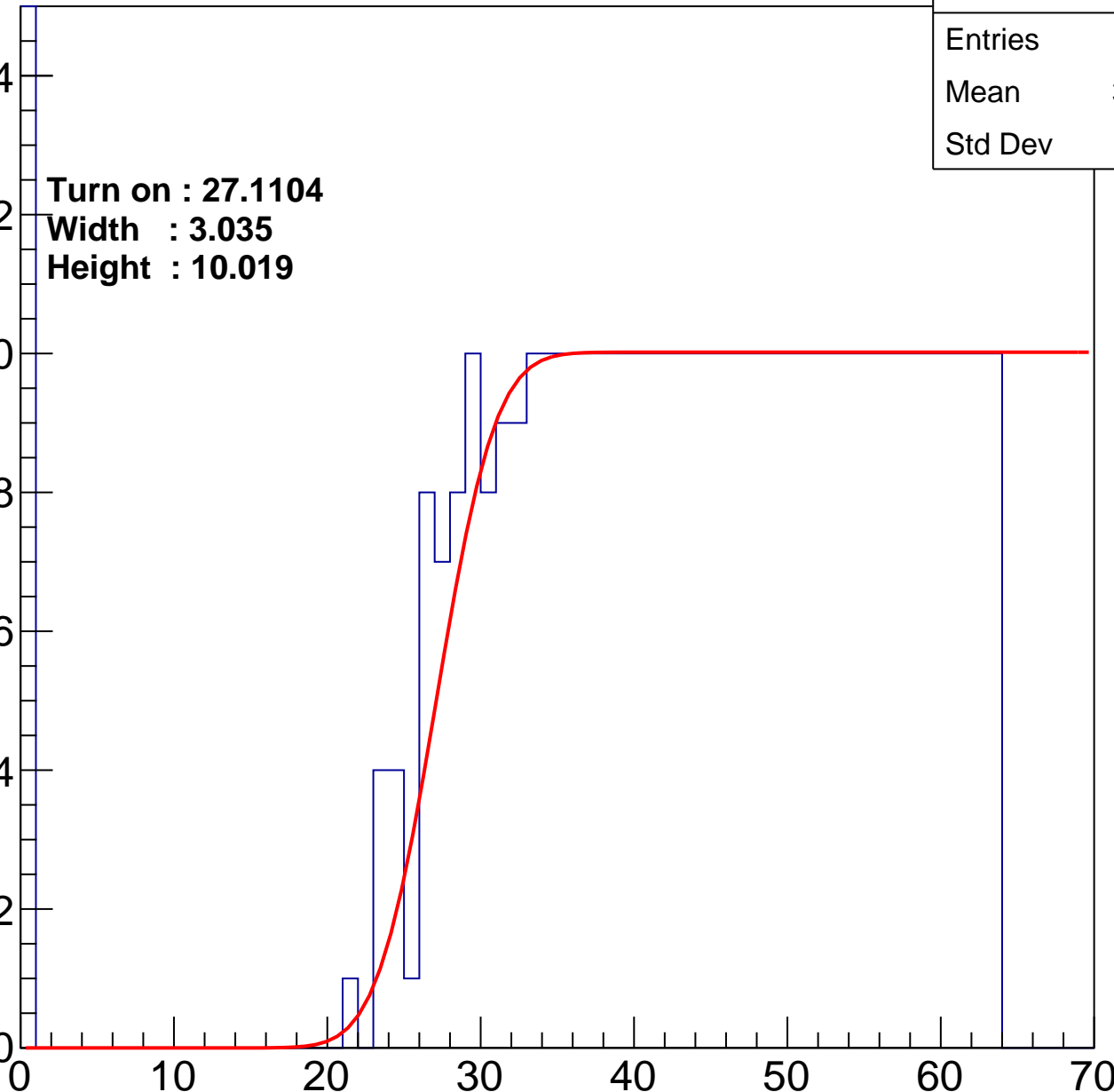
Width : 3.035

Height : 10.019

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch54

calib_packv5_041523_1651.root, FC#0, port C2

Entries	425
Mean	39.81
Std Dev	17.07

Turn on : 25.9873

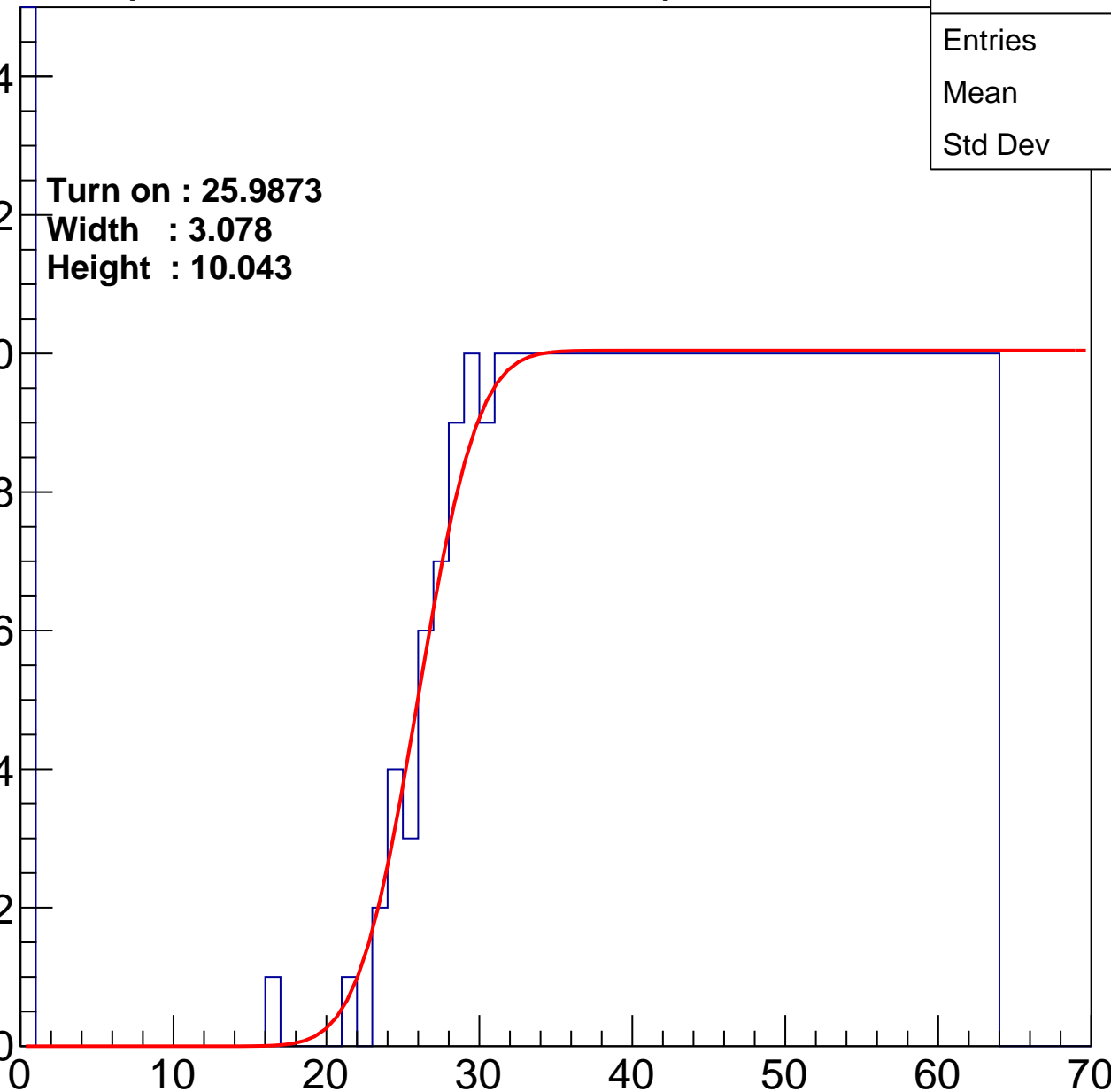
Width : 3.078

Height : 10.043

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch55

calib_packv5_041523_1651.root, FC#0, port C2

Entries	450
Mean	38.43
Std Dev	17.78

Turn on : 23.8463

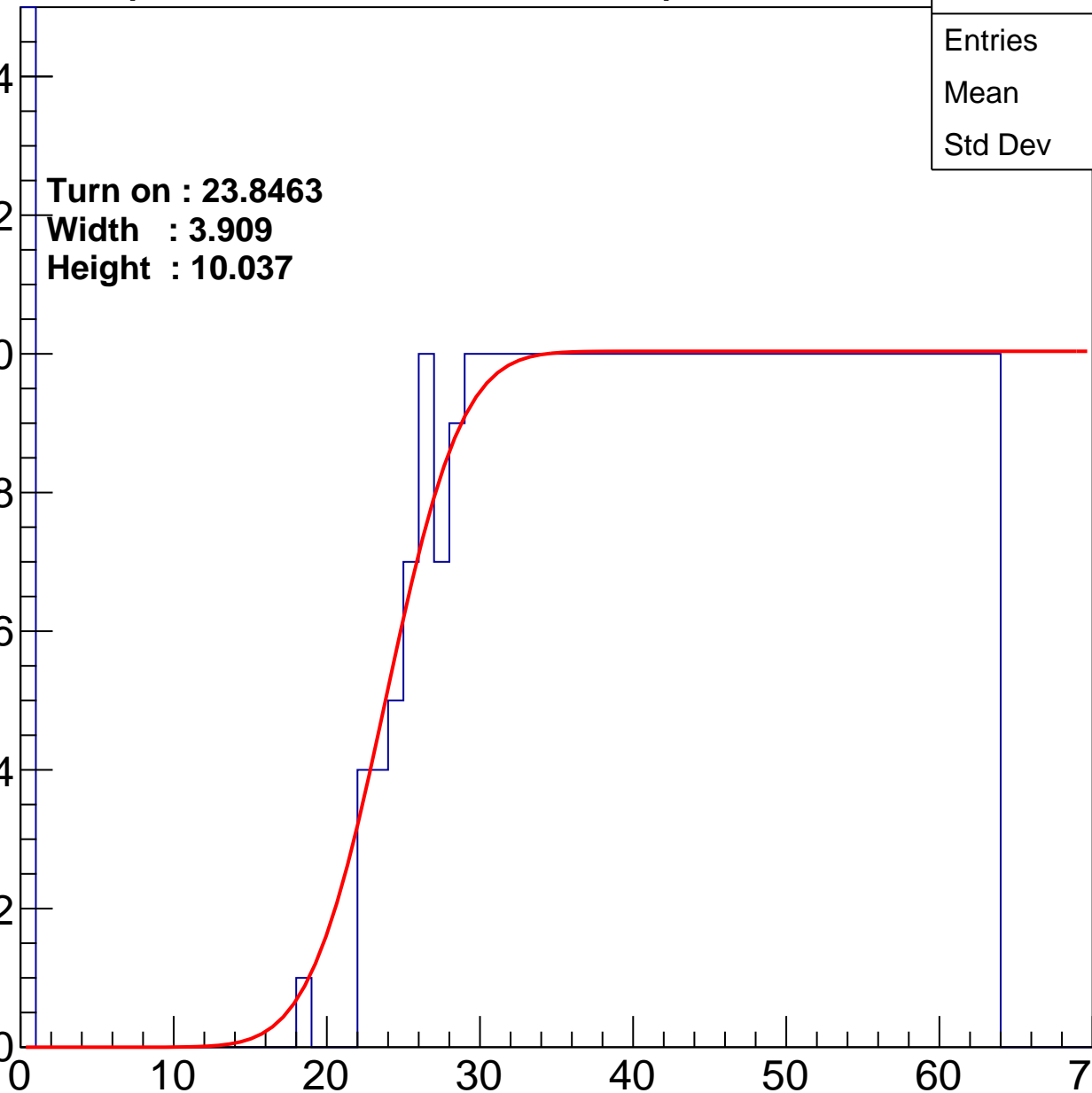
Width : 3.909

Height : 10.037

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch56

calib_packv5_041523_1651.root, FC#0, port C2

Entries	428
Mean	39.54
Std Dev	17.33

Turn on : 25.3101

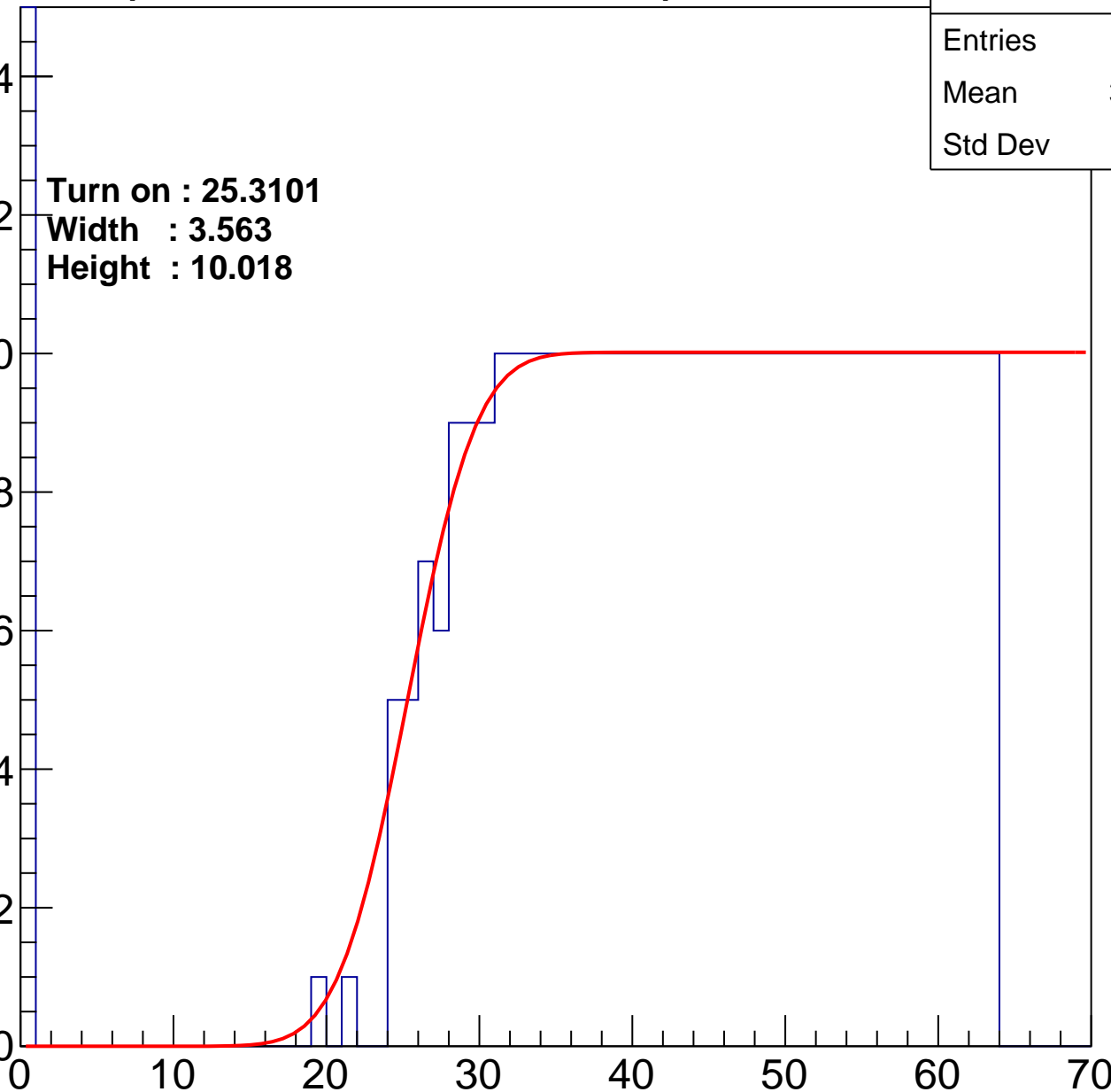
Width : 3.563

Height : 10.018

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch57

calib_packv5_041523_1651.root, FC#0, port C2

Entries	429
Mean	39.13
Std Dev	17.91

Turn on : 26.4230

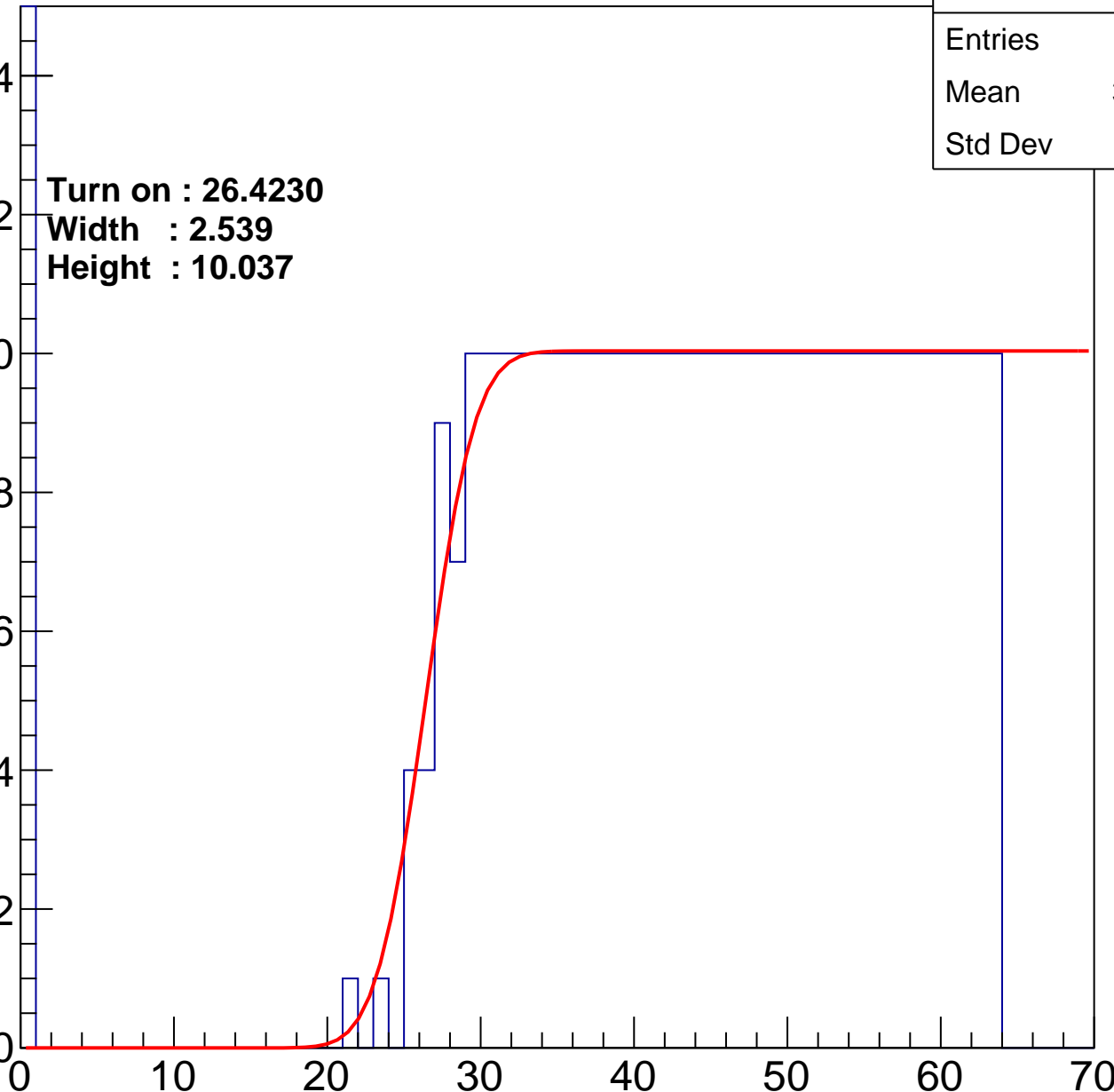
Width : 2.539

Height : 10.037

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch58

calib_packv5_041523_1651.root, FC#0, port C2

Entries	461
Mean	37.9
Std Dev	17.96

Turn on : 23.4091

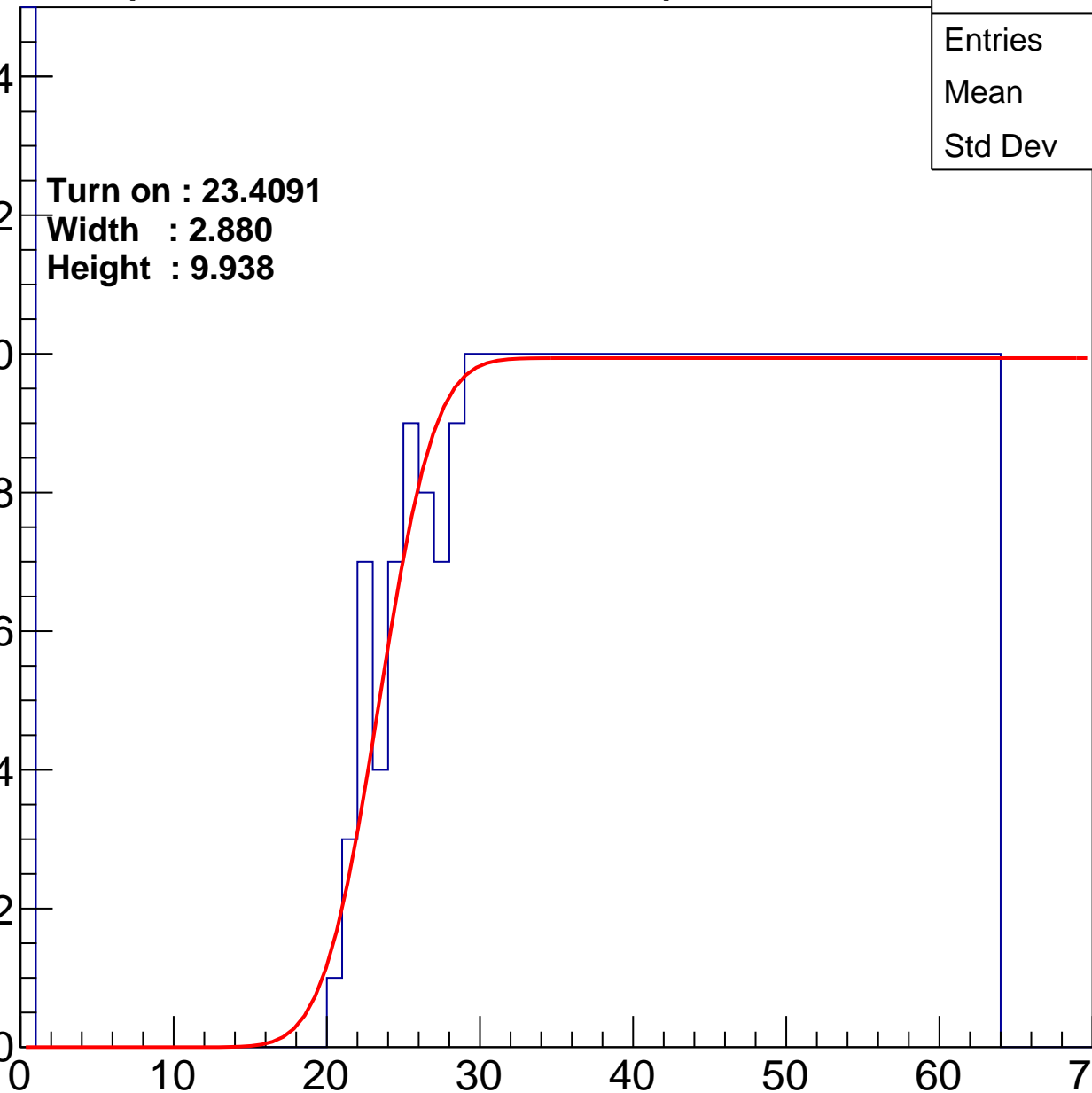
Width : 2.880

Height : 9.938

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch59

calib_packv5_041523_1651.root, FC#0, port C2

Entries	425
Mean	39.74
Std Dev	17.17

Turn on : 26.1986

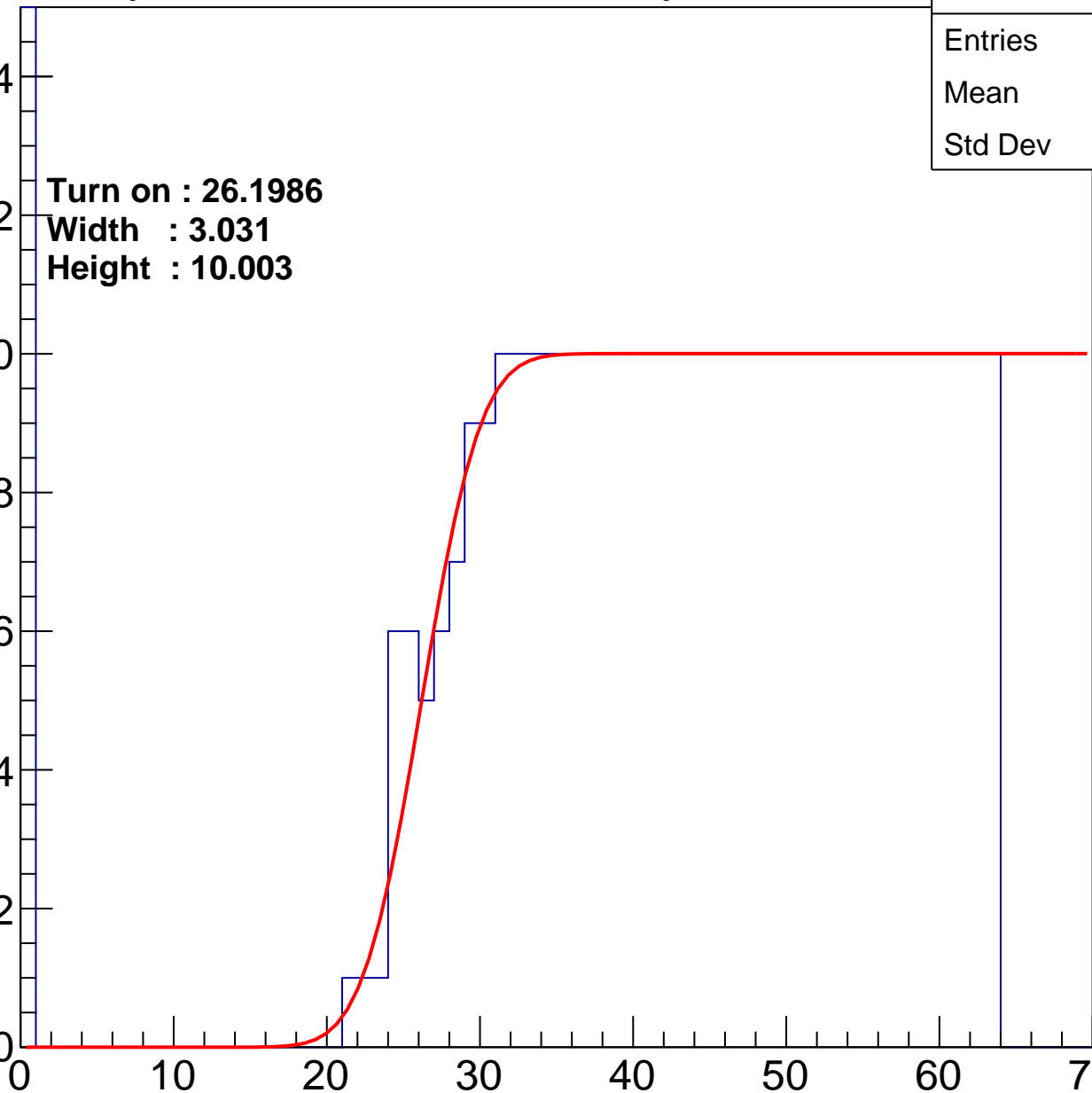
Width : 3.031

Height : 10.003

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch60

calib_packv5_041523_1651.root, FC#0, port C2

Entries	433
Mean	39.62
Std Dev	16.92

Turn on : 25.3412

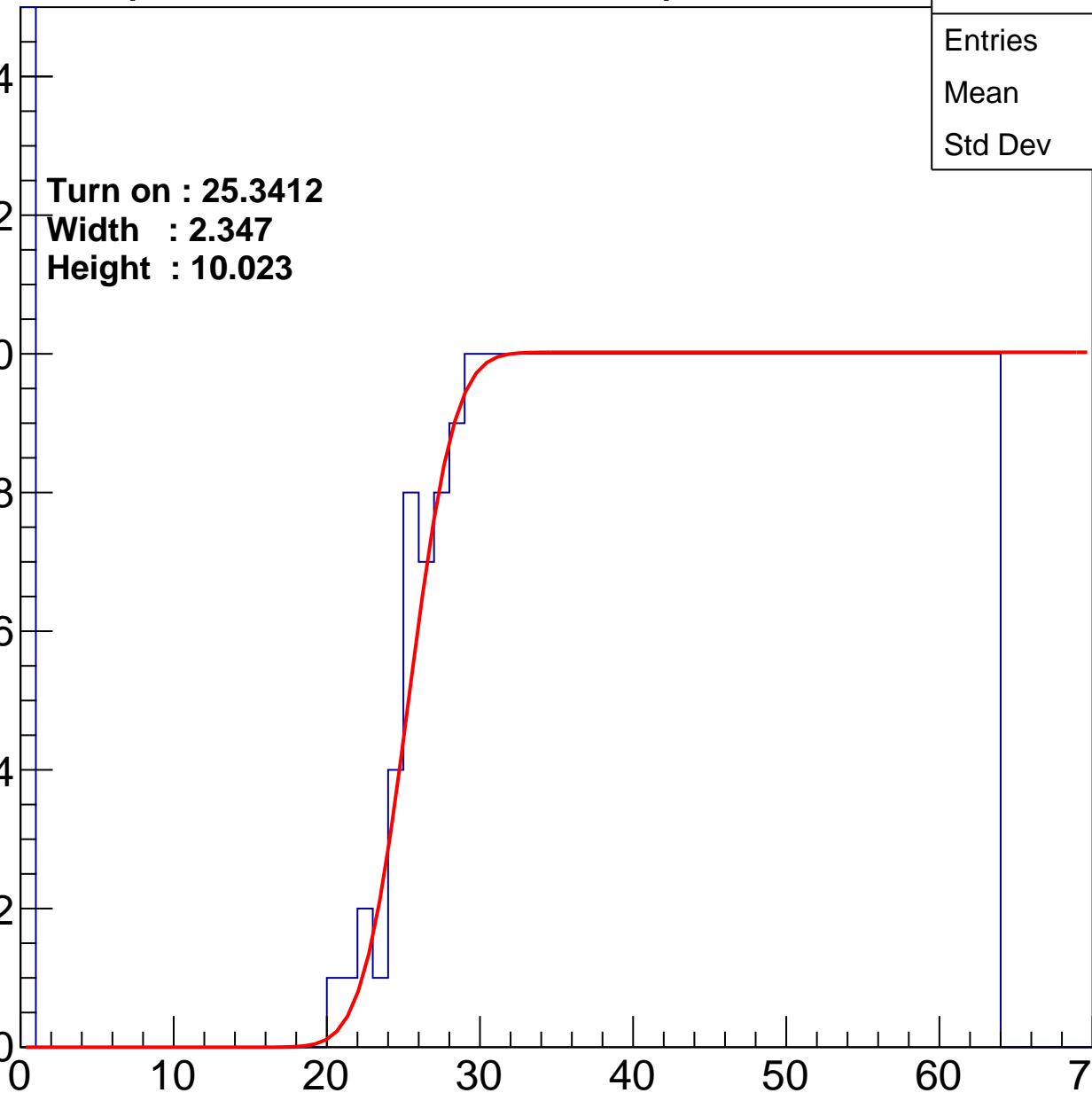
Width : 2.347

Height : 10.023

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch61

calib_packv5_041523_1651.root, FC#0, port C2

Entries	428
Mean	39.47
Std Dev	17.47

Turn on : 26.2195

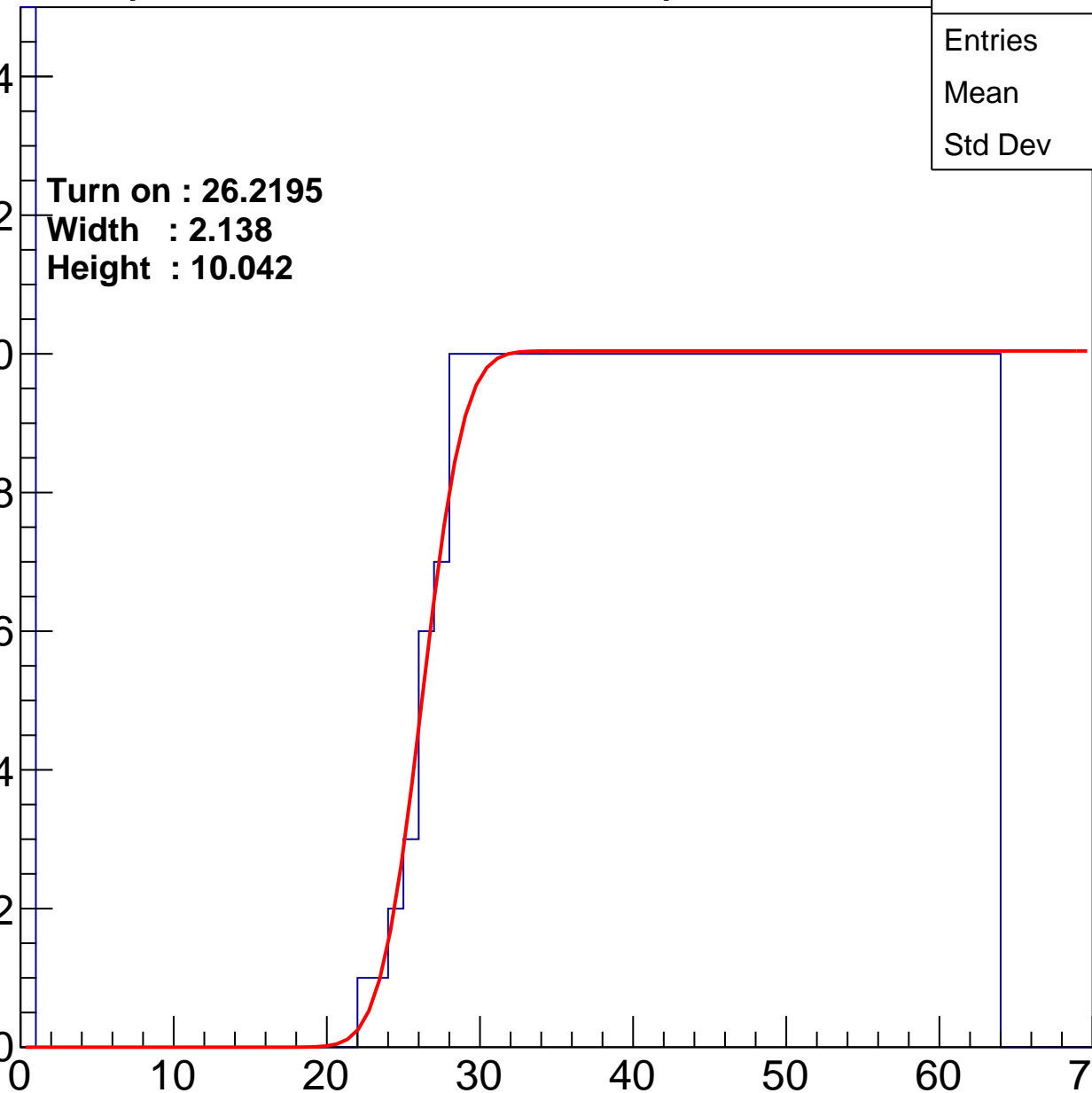
Width : 2.138

Height : 10.042

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch62

calib_packv5_041523_1651.root, FC#0, port C2

Entries	439
Mean	39.49
Std Dev	16.75

Turn on : 24.5298

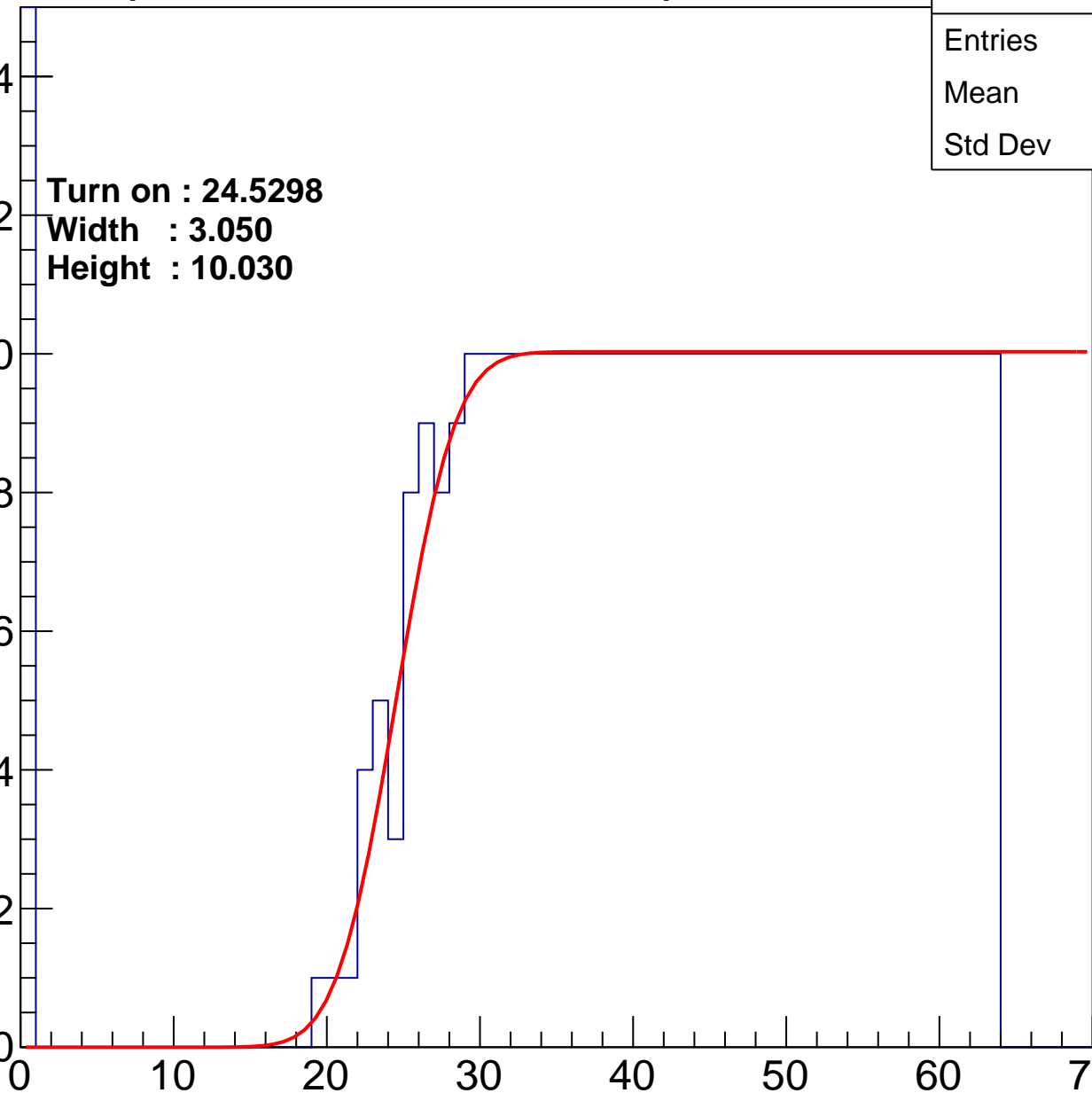
Width : 3.050

Height : 10.030

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch63

calib_packv5_041523_1651.root, FC#0, port C2

Entries	459
Mean	37.36
Std Dev	18.82

Turn on : 24.9921

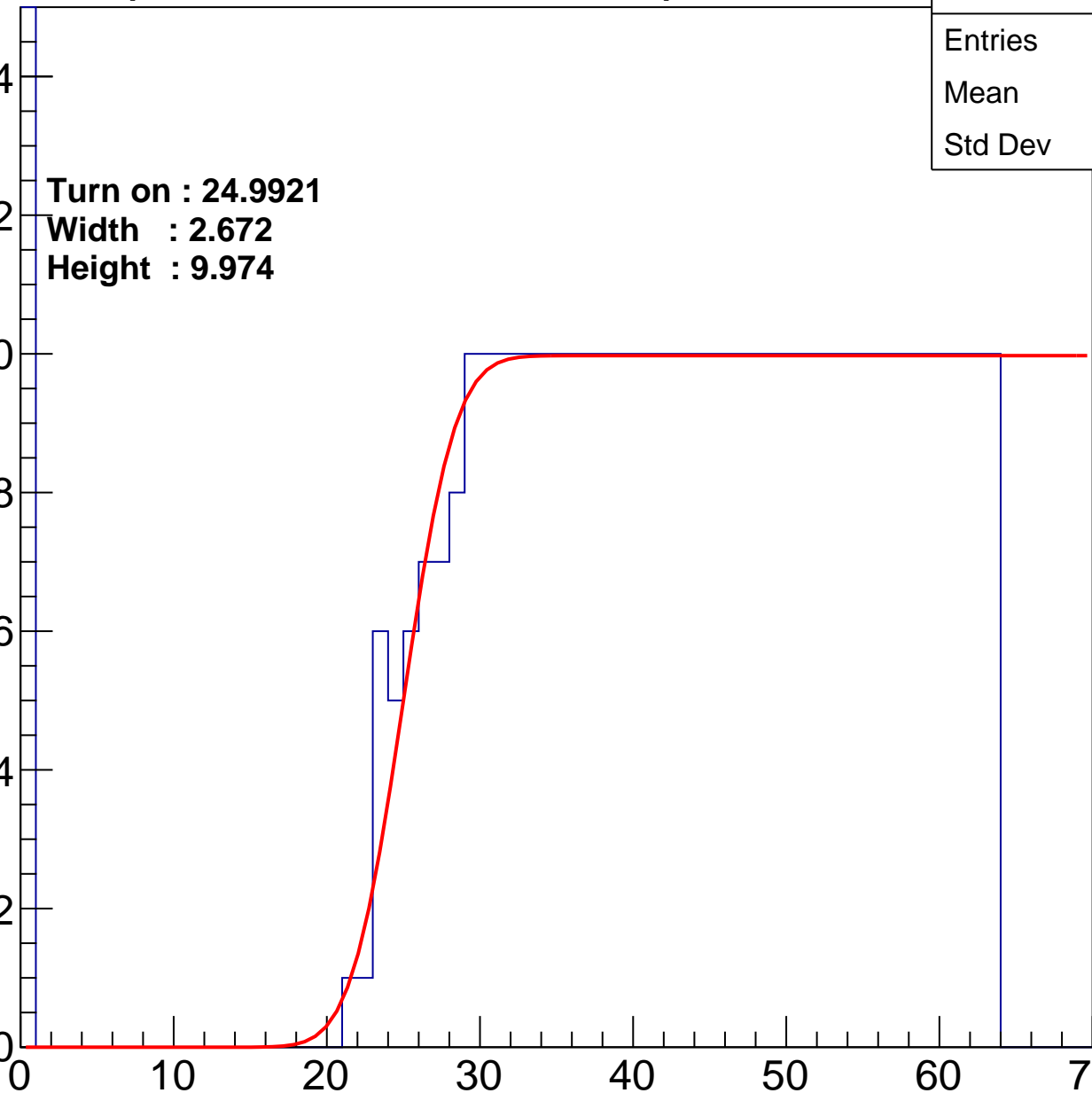
Width : 2.672

Height : 9.974

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch64

calib_packv5_041523_1651.root, FC#0, port C2

Entries	436
Mean	39.47
Std Dev	16.95

Turn on : 24.6486

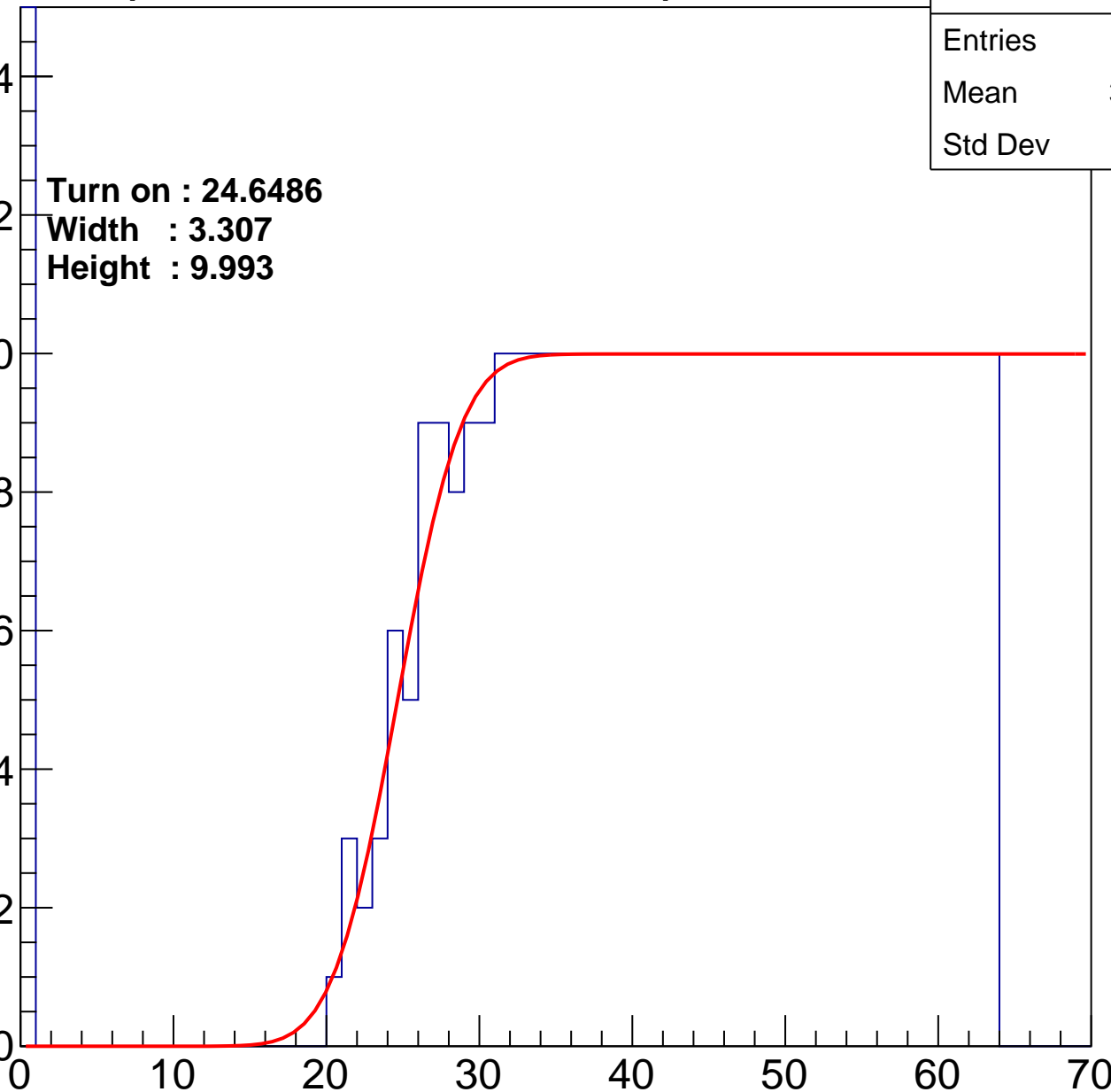
Width : 3.307

Height : 9.993

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch65

calib_packv5_041523_1651.root, FC#0, port C2

Entries	421
Mean	39.77
Std Dev	17.37

Turn on : 26.6000

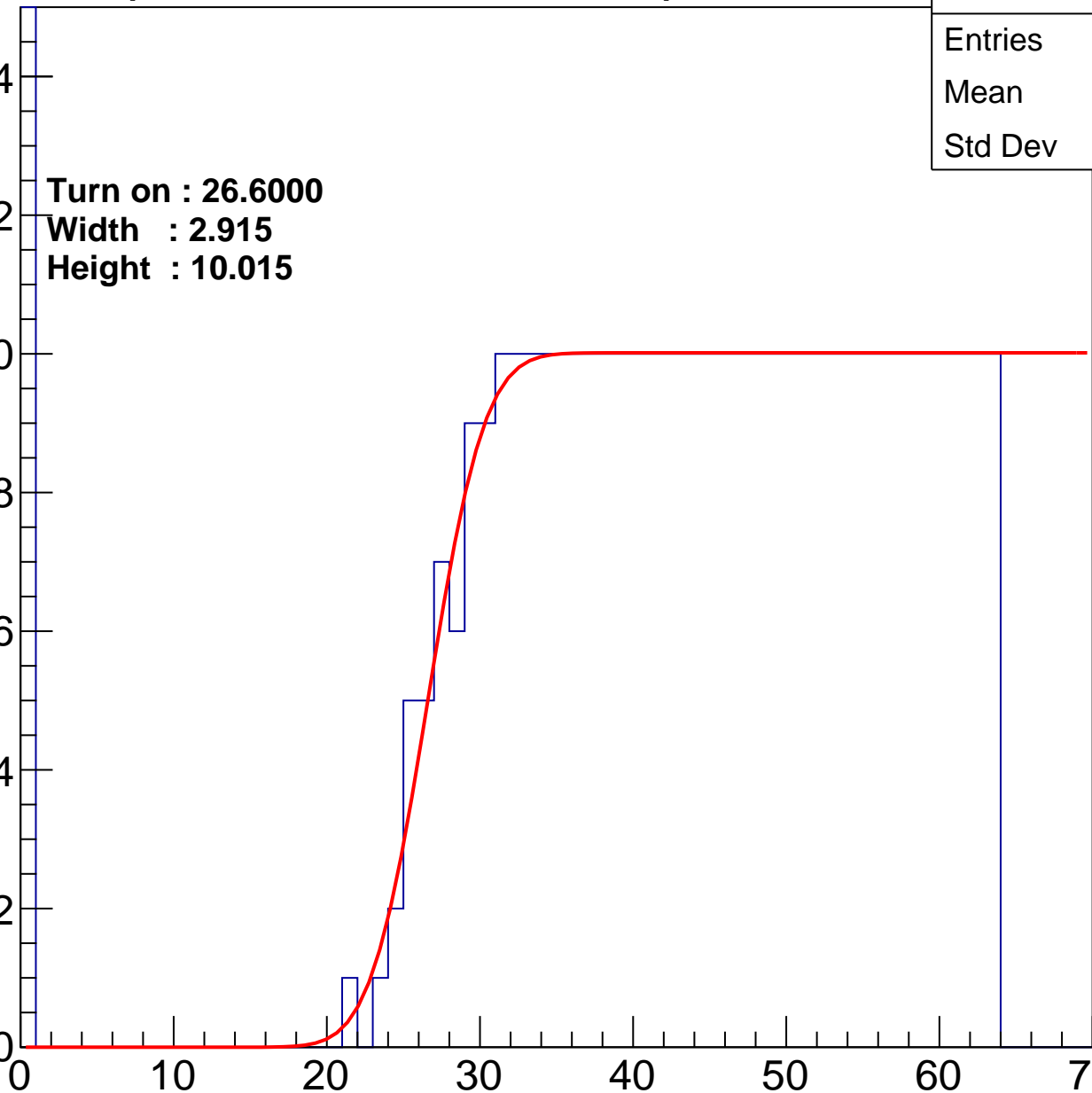
Width : 2.915

Height : 10.015

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch66

calib_packv5_041523_1651.root, FC#0, port C2

Entries	469
Mean	36.99
Std Dev	18.85

Turn on : 24.4853

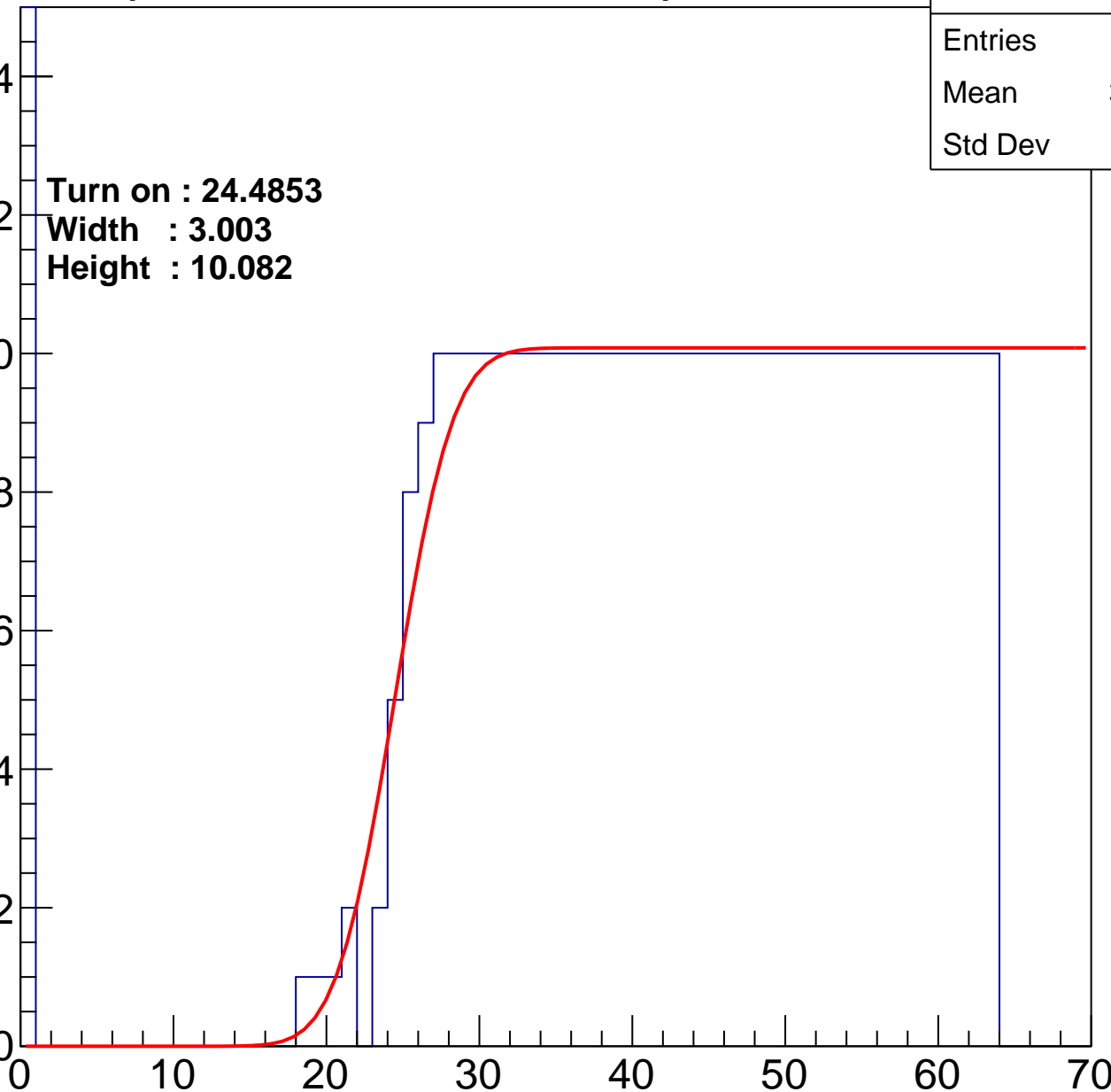
Width : 3.003

Height : 10.082

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch67

calib_packv5_041523_1651.root, FC#0, port C2

Entries	436
Mean	38.87
Std Dev	17.84

Turn on : 25.4322

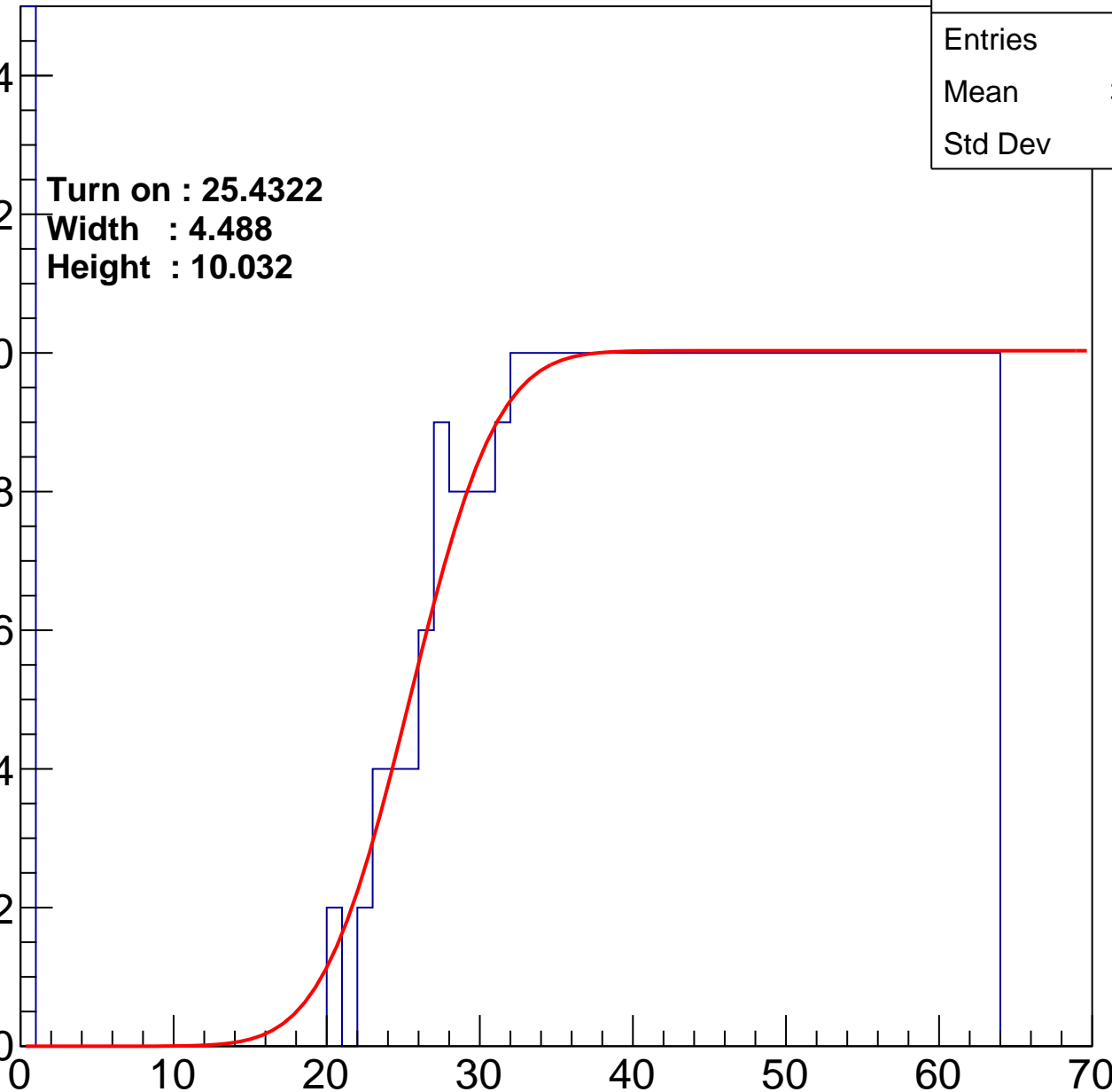
Width : 4.488

Height : 10.032

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch68

calib_packv5_041523_1651.root, FC#0, port C2

Entries	458
Mean	38.31
Std Dev	17.51

Turn on : 23.5826

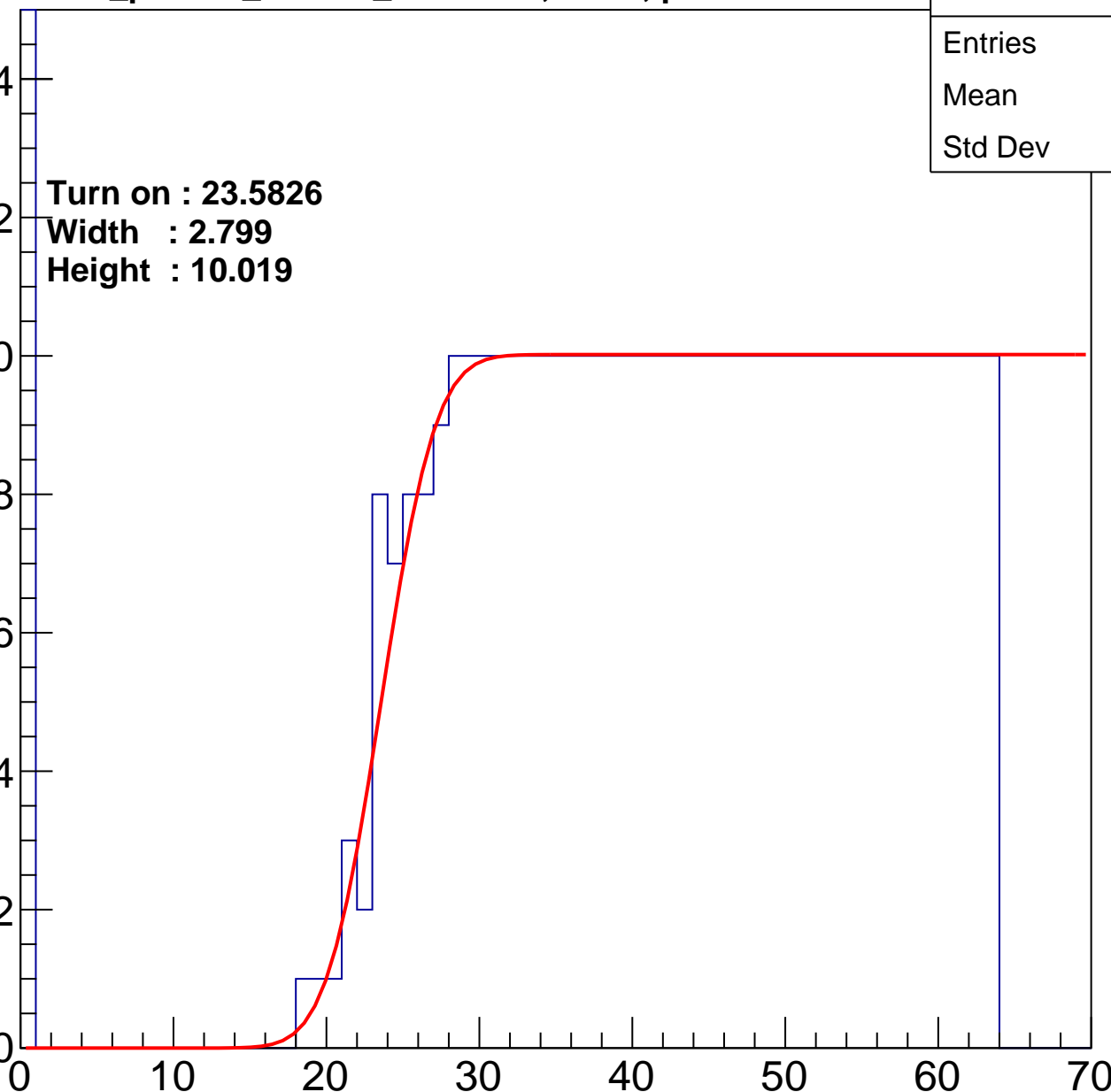
Width : 2.799

Height : 10.019

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch69

calib_packv5_041523_1651.root, FC#0, port C2

Entries	457
Mean	38.21
Std Dev	17.73

Turn on : 23.6873

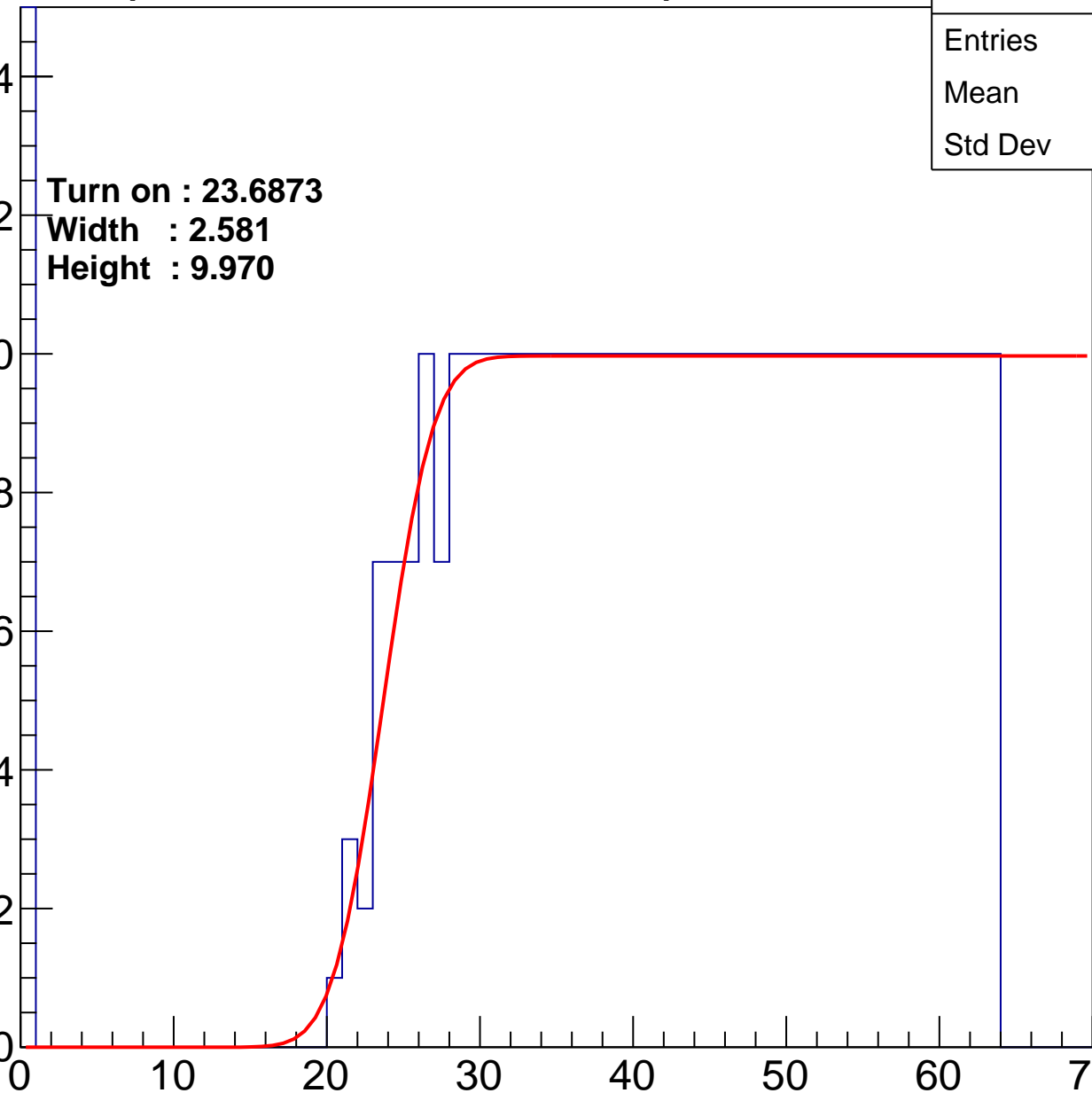
Width : 2.581

Height : 9.970

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch70

calib_packv5_041523_1651.root, FC#0, port C2

Entries	446
Mean	38.73
Std Dev	17.55

Turn on : 24.6756

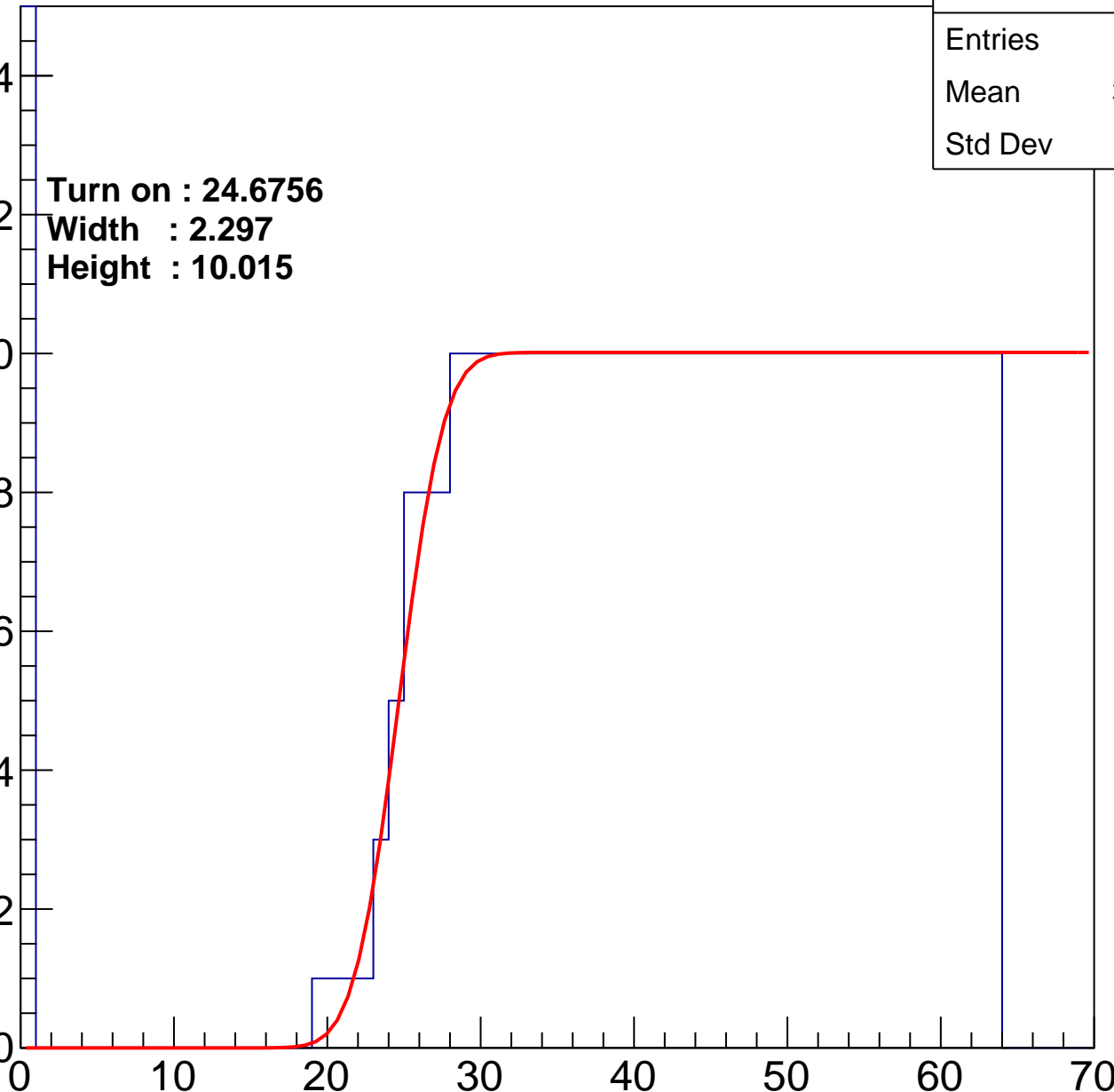
Width : 2.297

Height : 10.015

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch71

calib_packv5_041523_1651.root, FC#0, port C2

Entries	445
Mean	38.43
Std Dev	18.05

Turn on : 25.2409

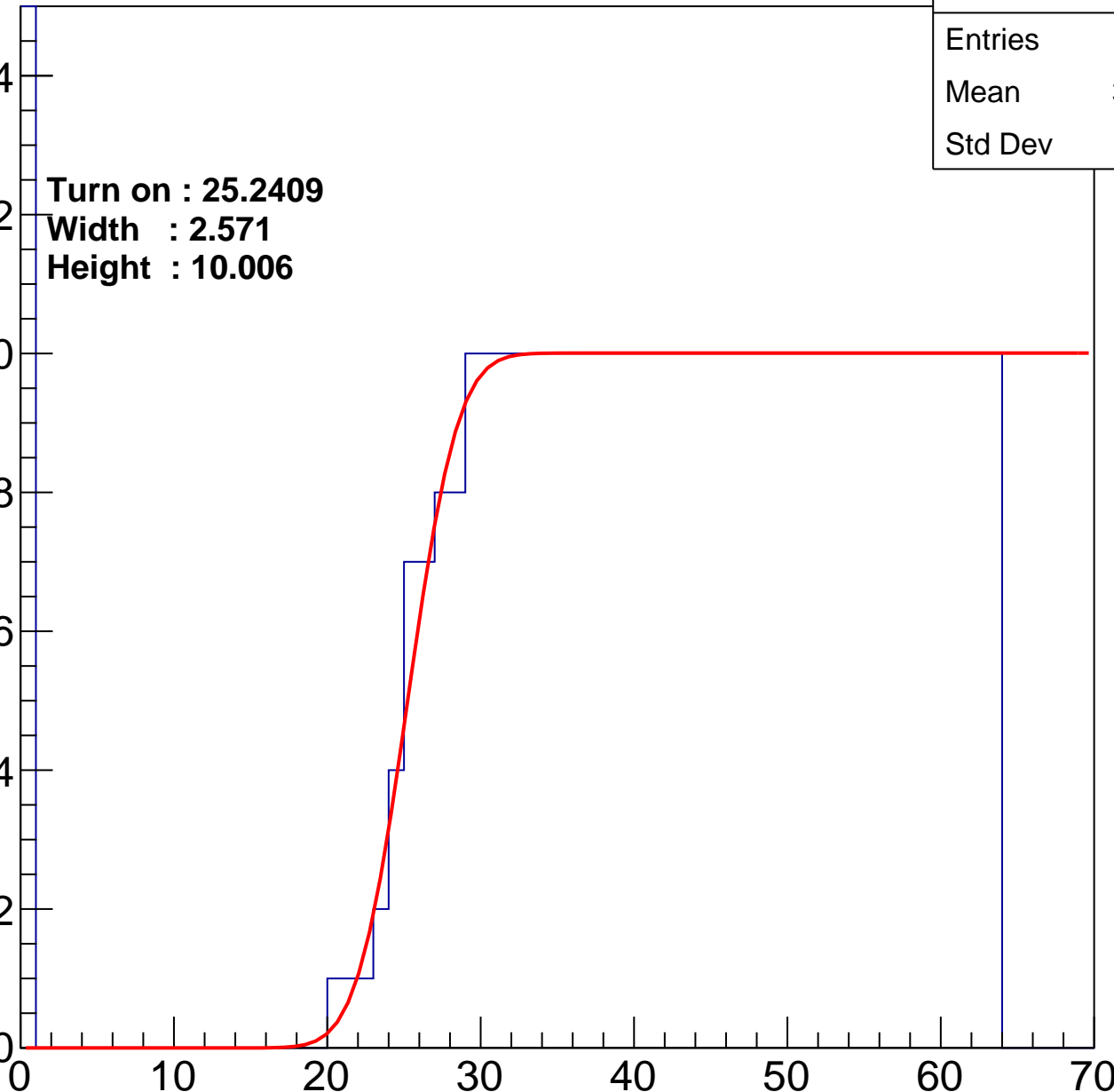
Width : 2.571

Height : 10.006

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch72

calib_packv5_041523_1651.root, FC#0, port C2

Entries	451
Mean	37.83
Std Dev	18.56

Turn on : 25.1485

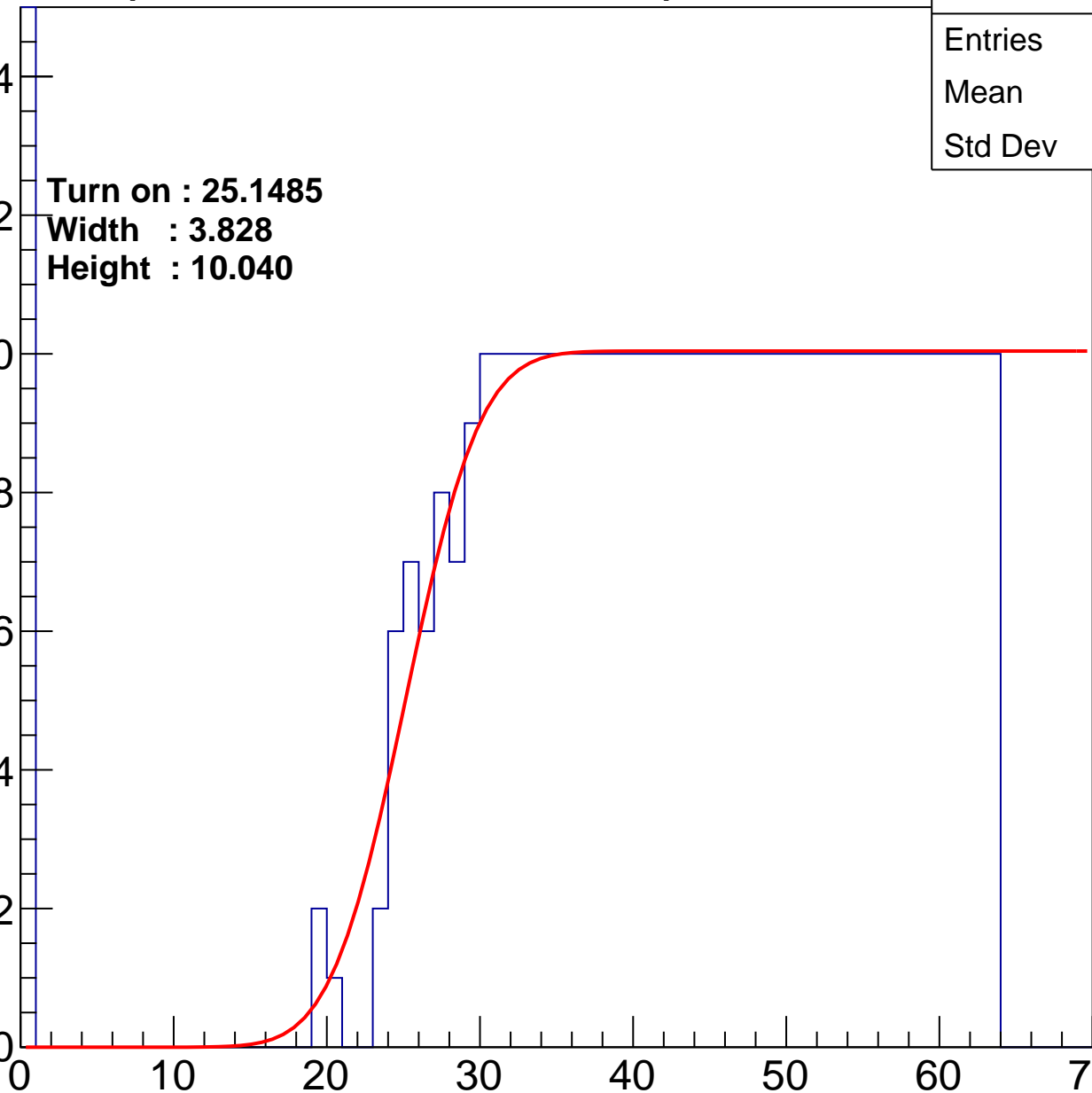
Width : 3.828

Height : 10.040

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch73

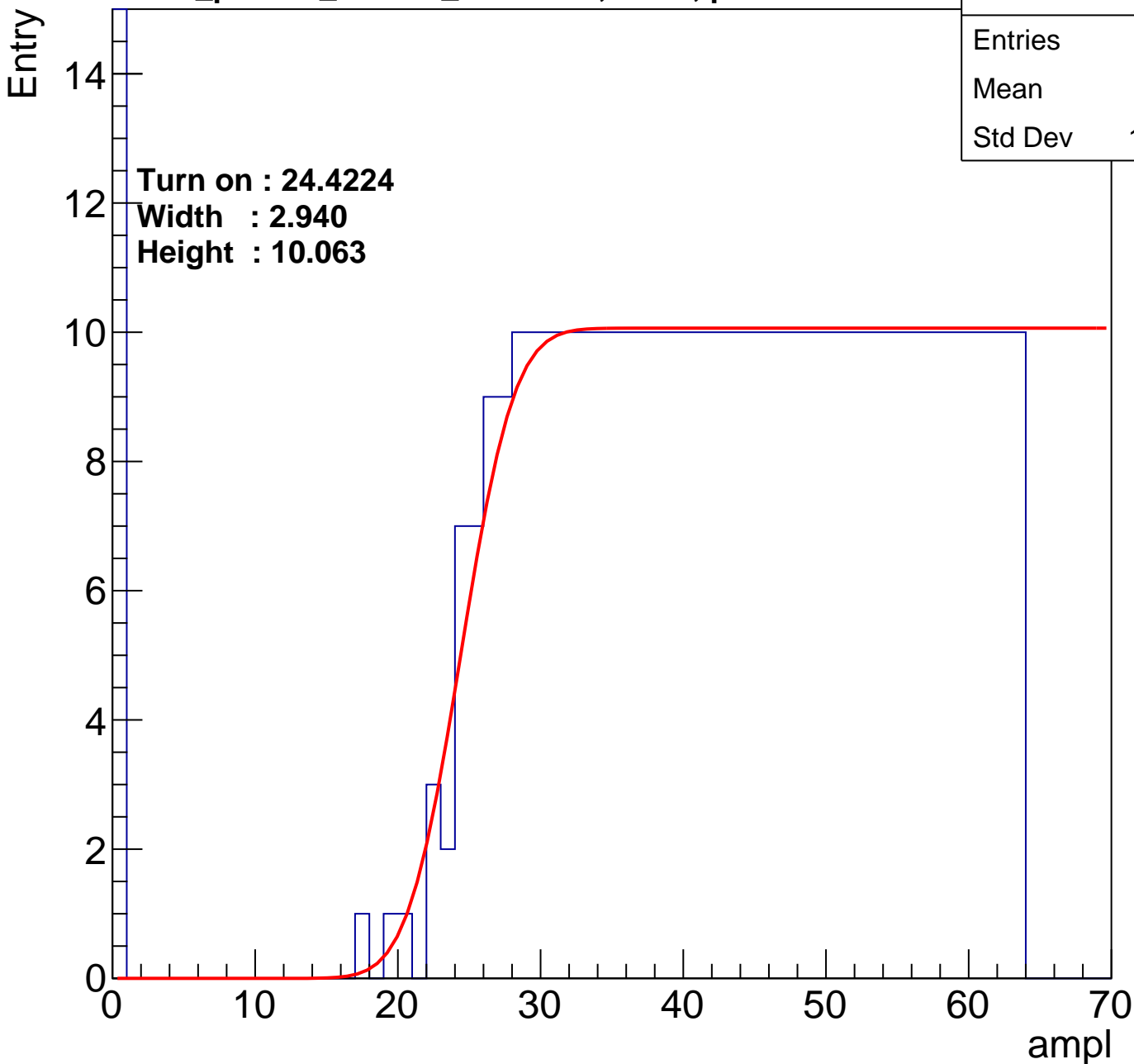
calib_packv5_041523_1651.root, FC#0, port C2

Entries	450
Mean	38.6
Std Dev	17.54

Turn on : 24.4224

Width : 2.940

Height : 10.063



B1L103S, U2-ch74

calib_packv5_041523_1651.root, FC#0, port C2

Entries	442
Mean	39.48
Std Dev	16.57

Turn on : 22.6905

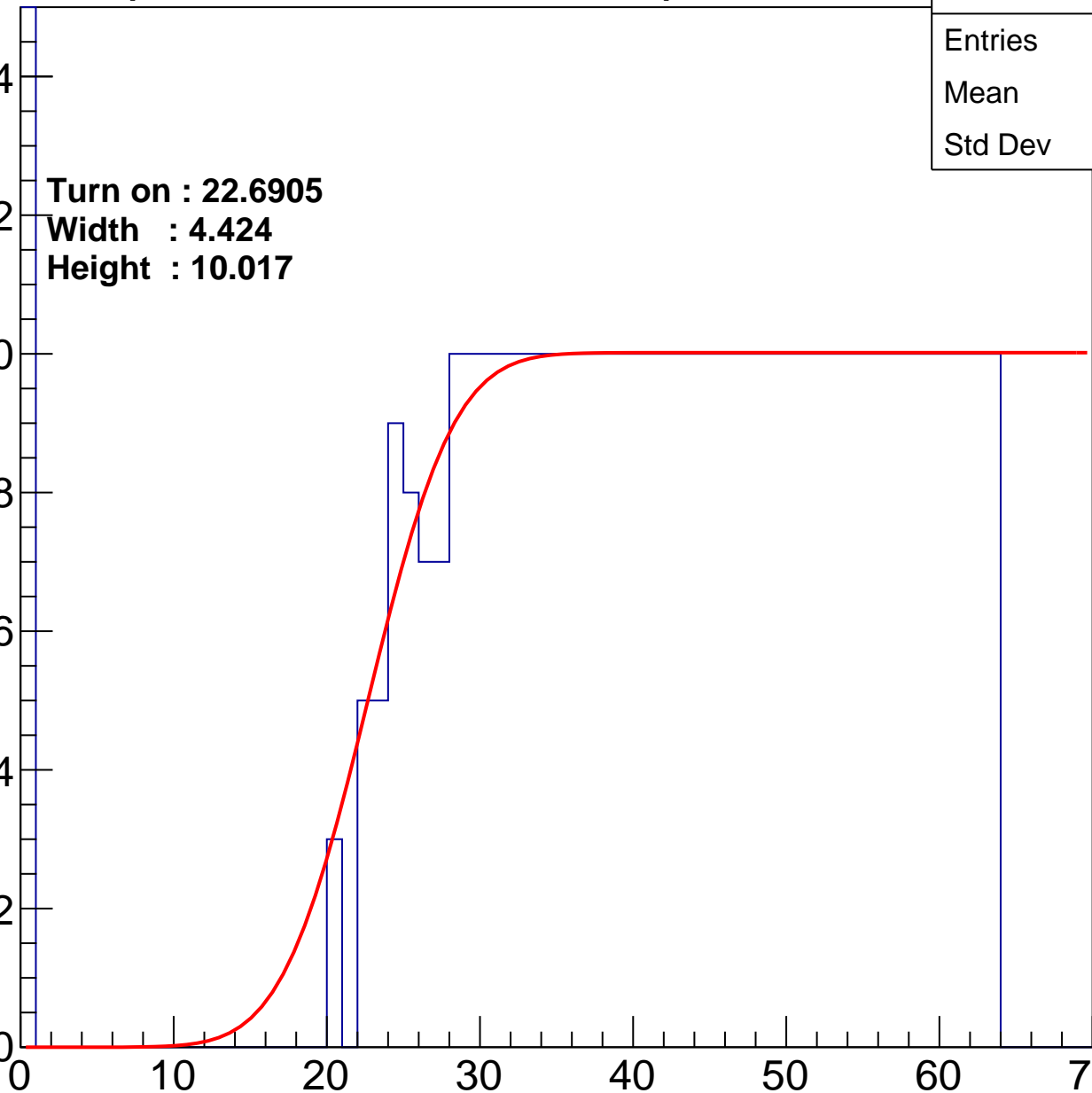
Width : 4.424

Height : 10.017

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch75

calib_packv5_041523_1651.root, FC#0, port C2

Entries	431
Mean	39.35
Std Dev	17.43

Turn on : 27.1555

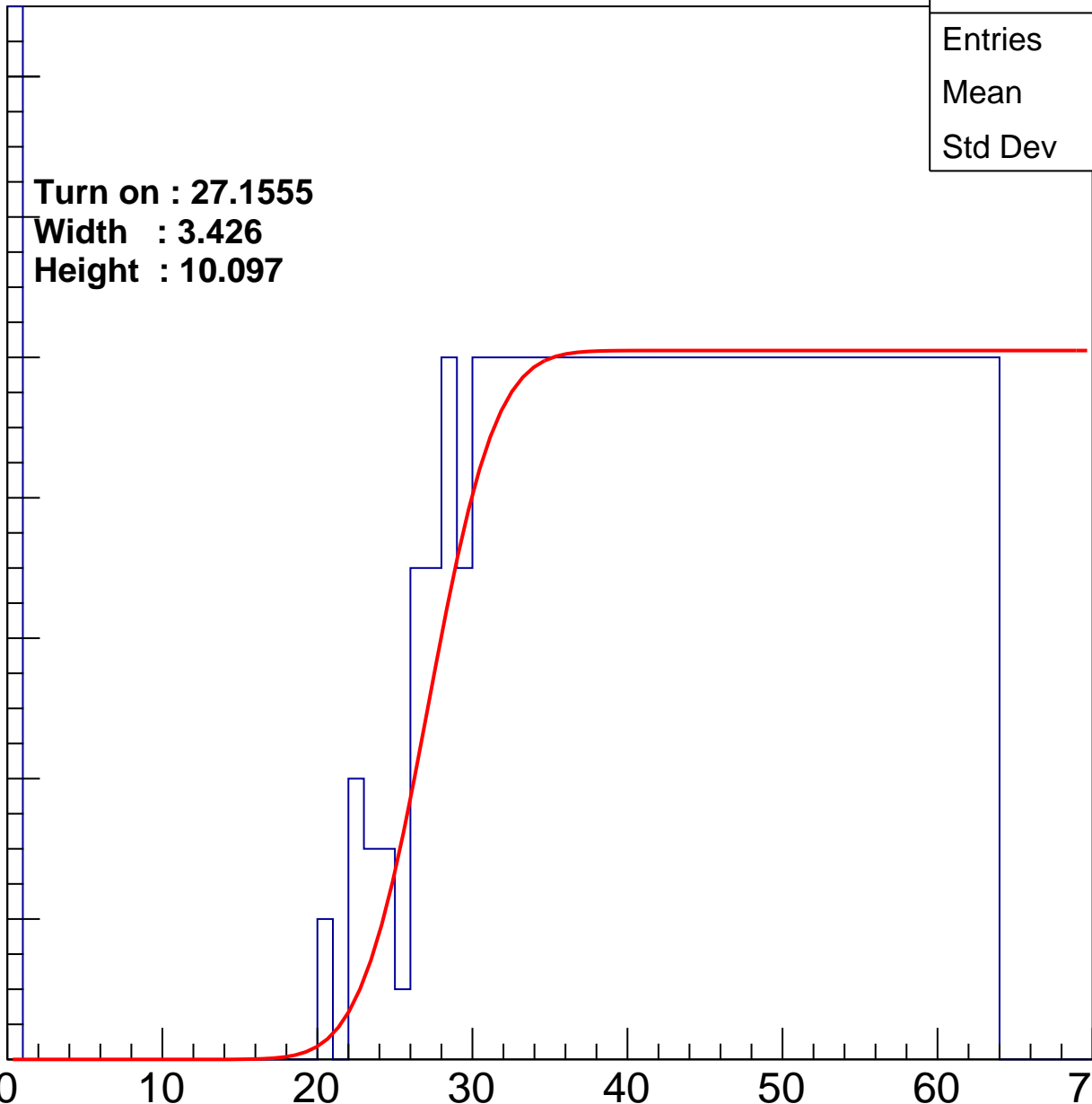
Width : 3.426

Height : 10.097

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch76

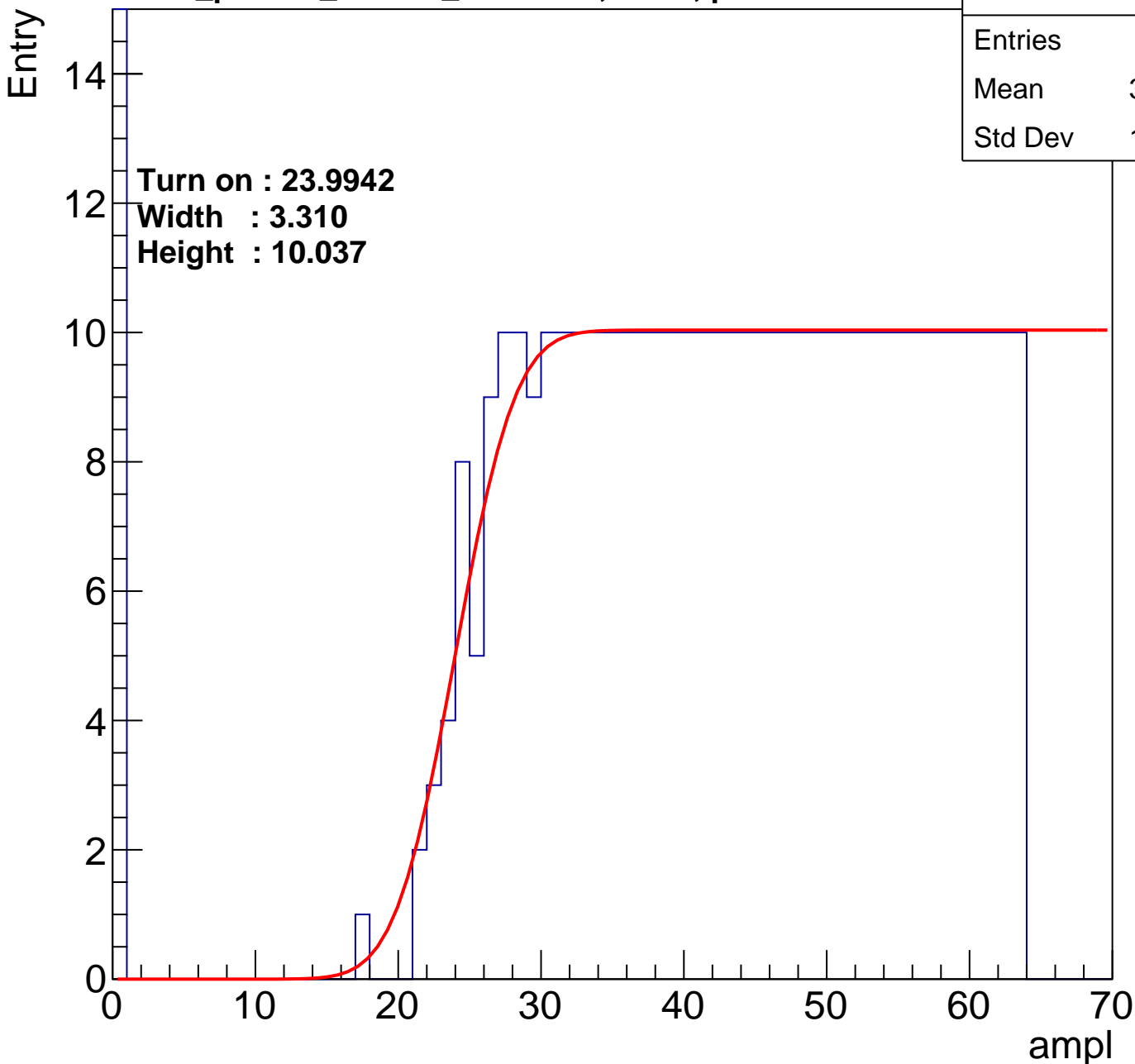
calib_packv5_041523_1651.root, FC#0, port C2

Entries	463
Mean	37.56
Std Dev	18.36

Turn on : 23.9942

Width : 3.310

Height : 10.037



B1L103S, U2-ch77

calib_packv5_041523_1651.root, FC#0, port C2

Entries	438
Mean	38.24
Std Dev	18.64

Turn on : 26.9770

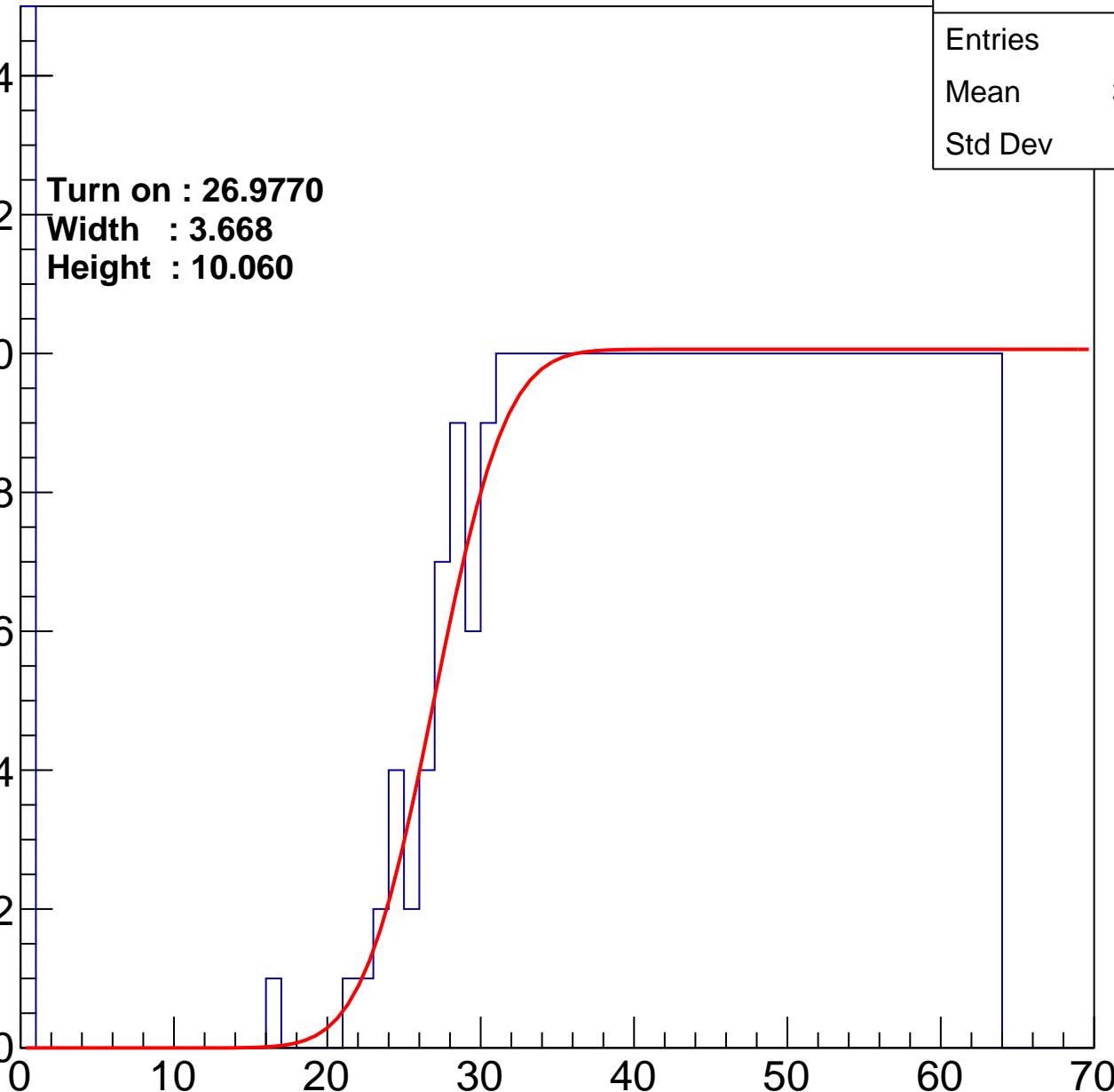
Width : 3.668

Height : 10.060

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch78

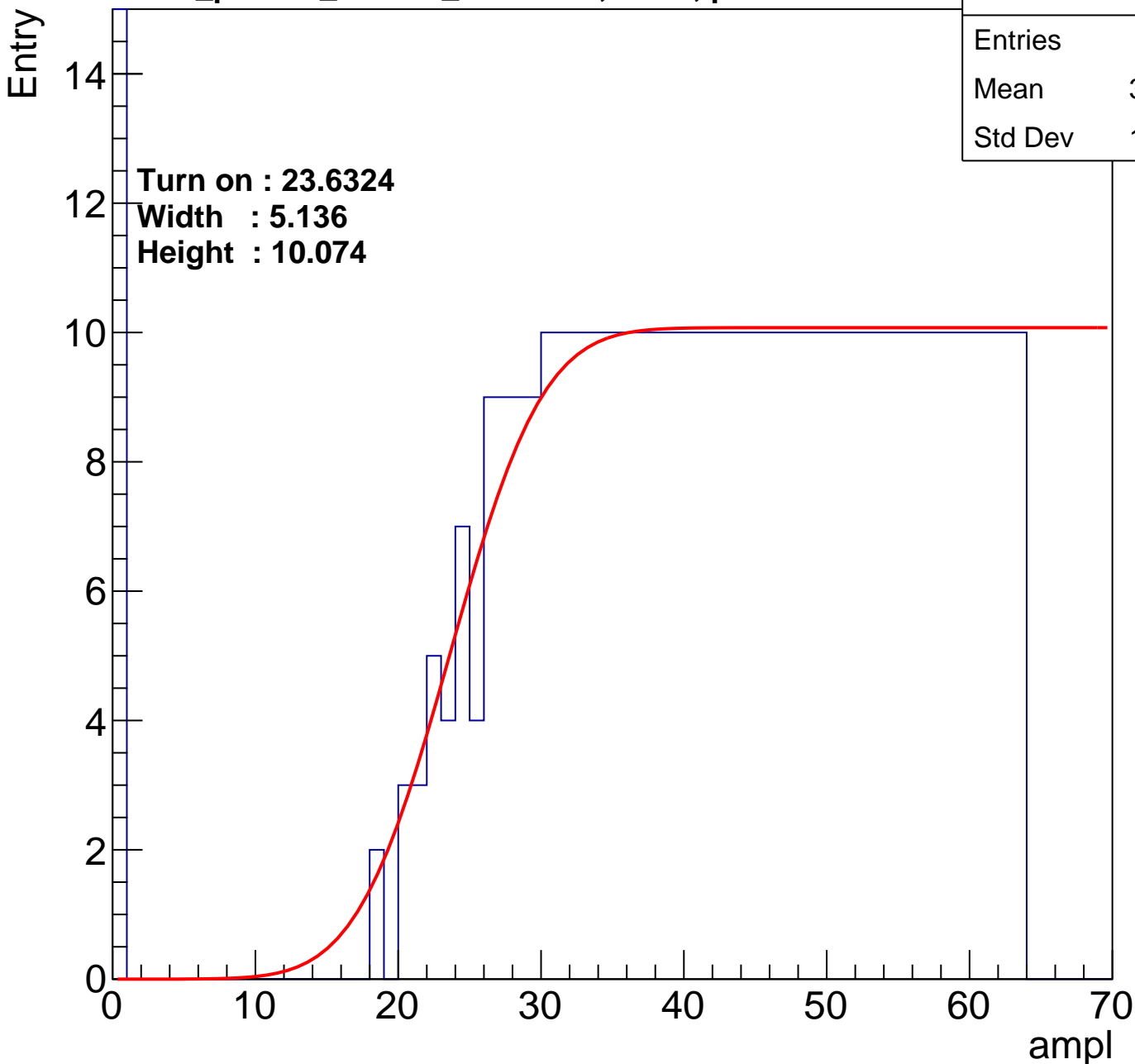
calib_packv5_041523_1651.root, FC#0, port C2

Entries	474
Mean	36.77
Std Dev	18.86

Turn on : 23.6324

Width : 5.136

Height : 10.074



B1L103S, U2-ch79

calib_packv5_041523_1651.root, FC#0, port C2

Entries	439
Mean	38.76
Std Dev	17.91

Turn on : 25.5122

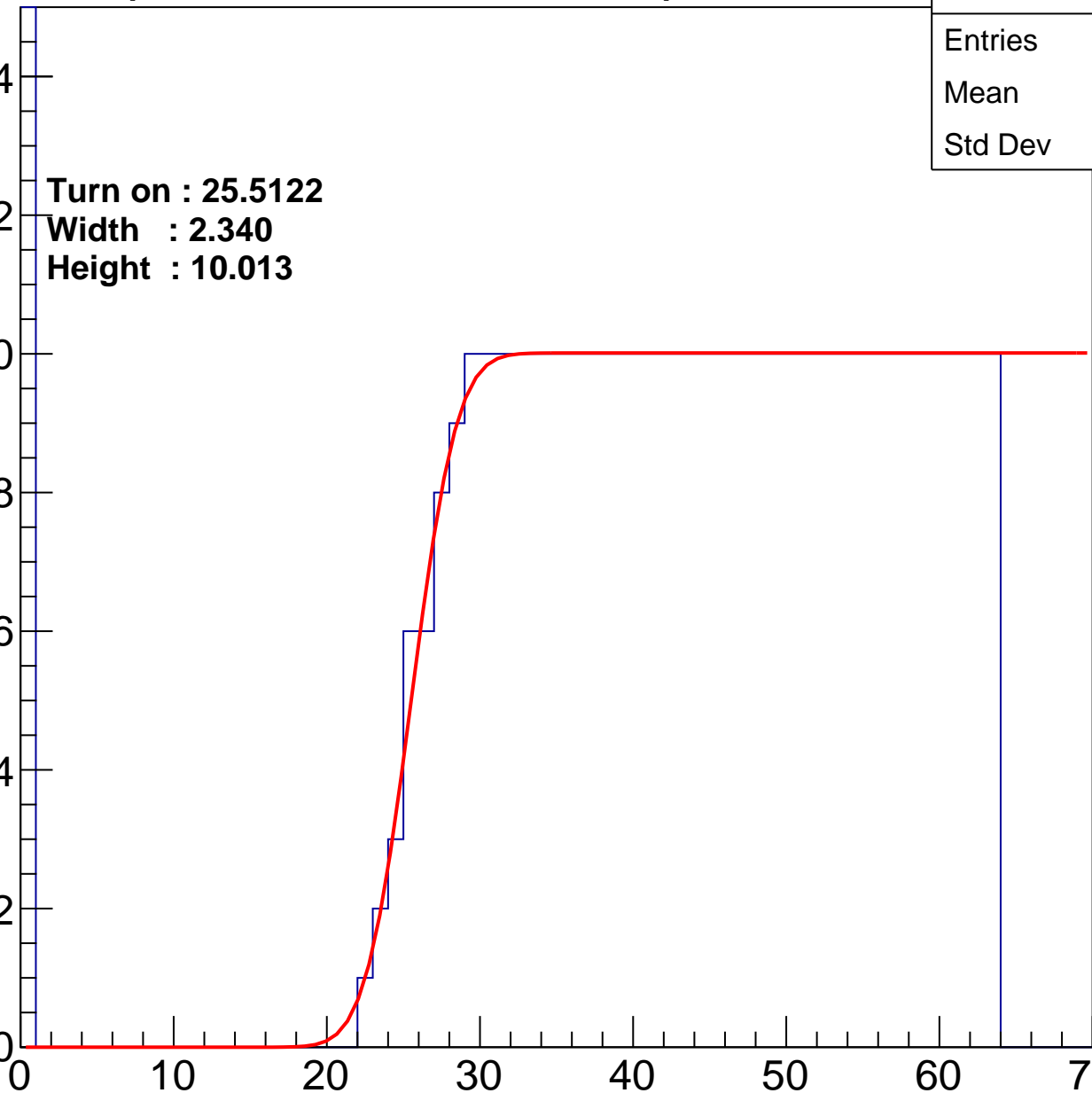
Width : 2.340

Height : 10.013

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch80

calib_packv5_041523_1651.root, FC#0, port C2

Entries	467
Mean	38.13
Std Dev	17.31

Turn on : 22.8898

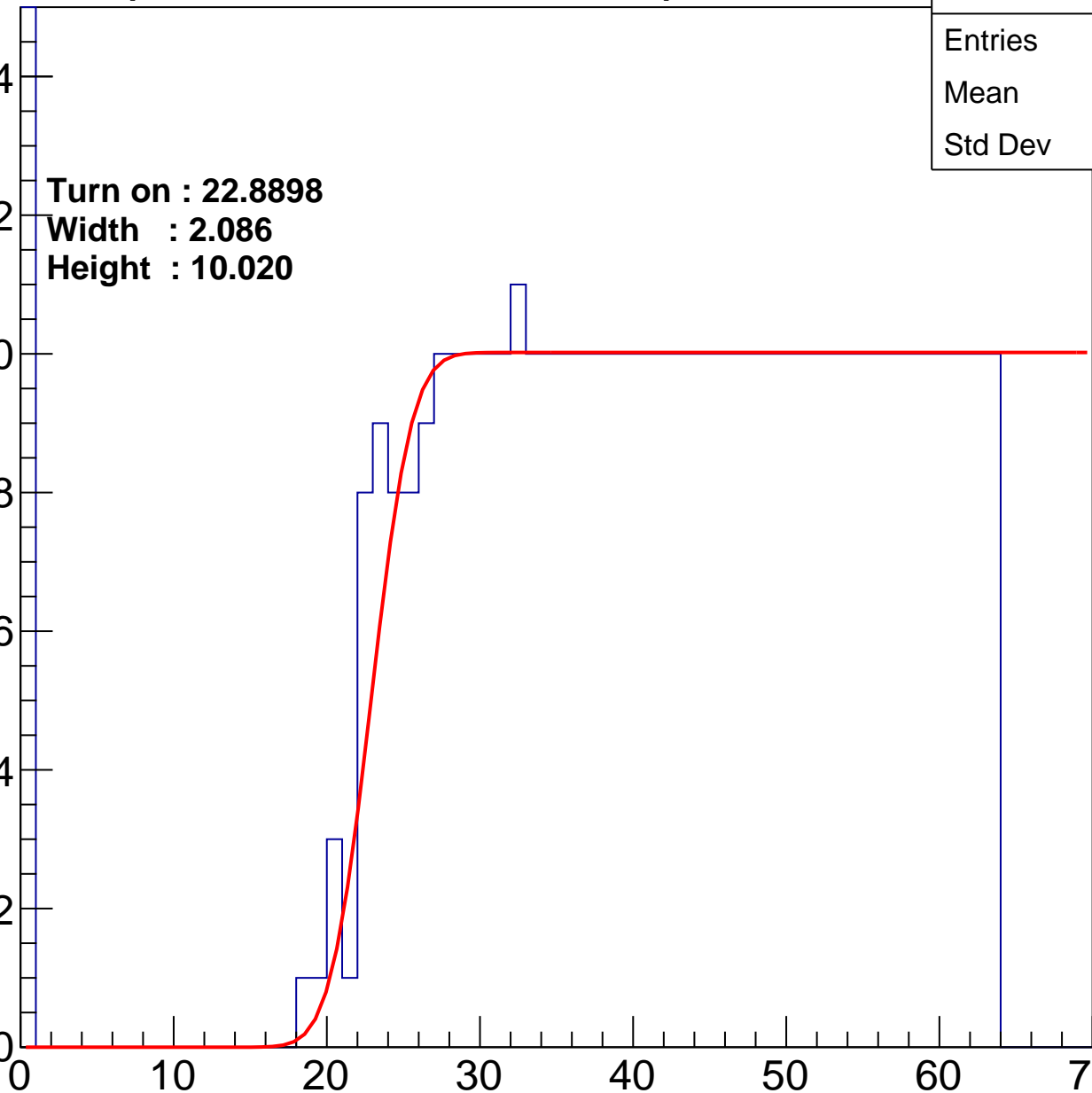
Width : 2.086

Height : 10.020

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch81

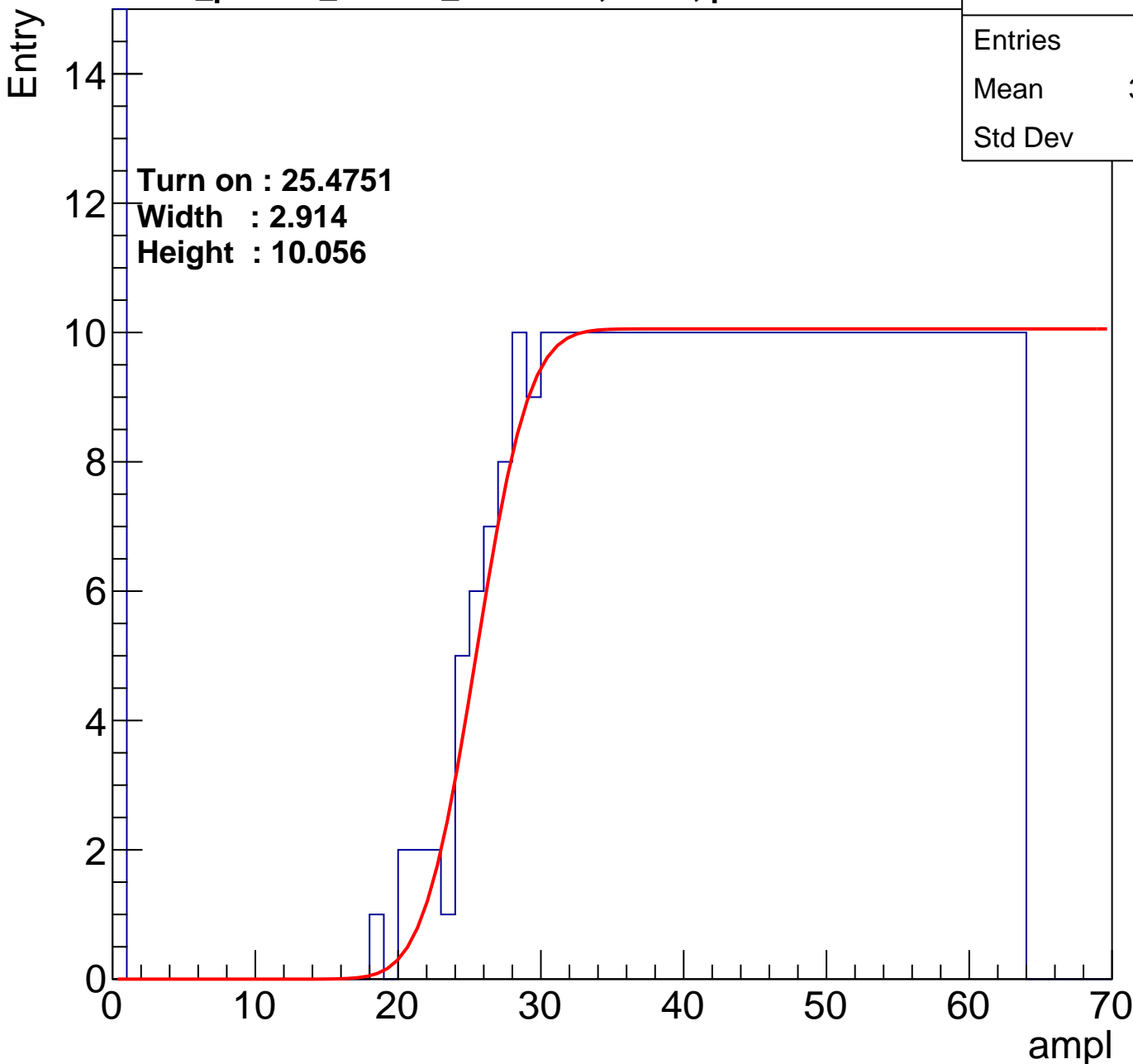
calib_packv5_041523_1651.root, FC#0, port C2

Entries	450
Mean	38.19
Std Dev	18.11

Turn on : 25.4751

Width : 2.914

Height : 10.056



B1L103S, U2-ch82

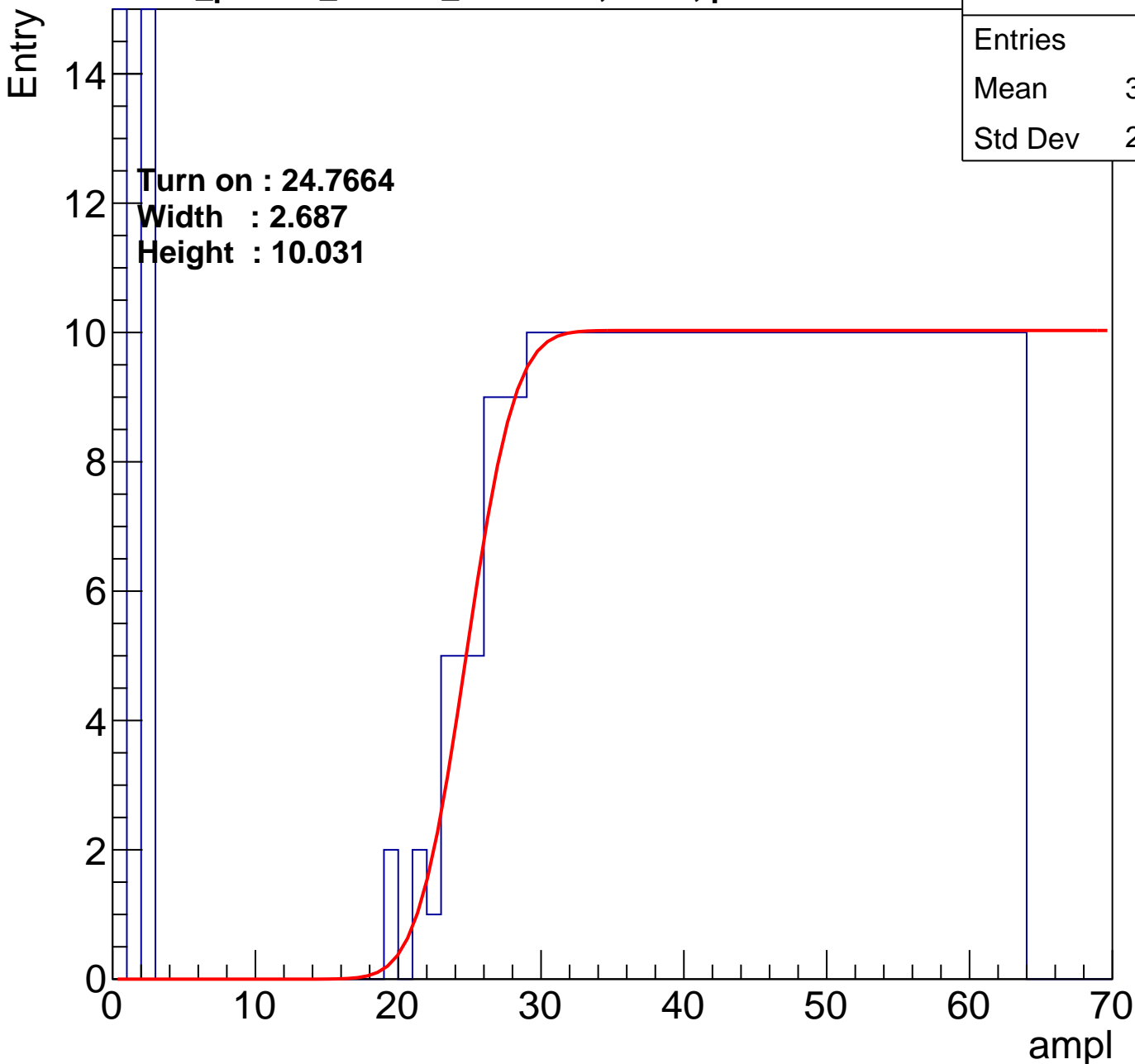
calib_packv5_041523_1651.root, FC#0, port C2

Entries	521
Mean	33.38
Std Dev	20.85

Turn on : 24.7664

Width : 2.687

Height : 10.031



B1L103S, U2-ch83

calib_packv5_041523_1651.root, FC#0, port C2

Entries	448
Mean	37.51
Std Dev	19.12

Turn on : 27.0681

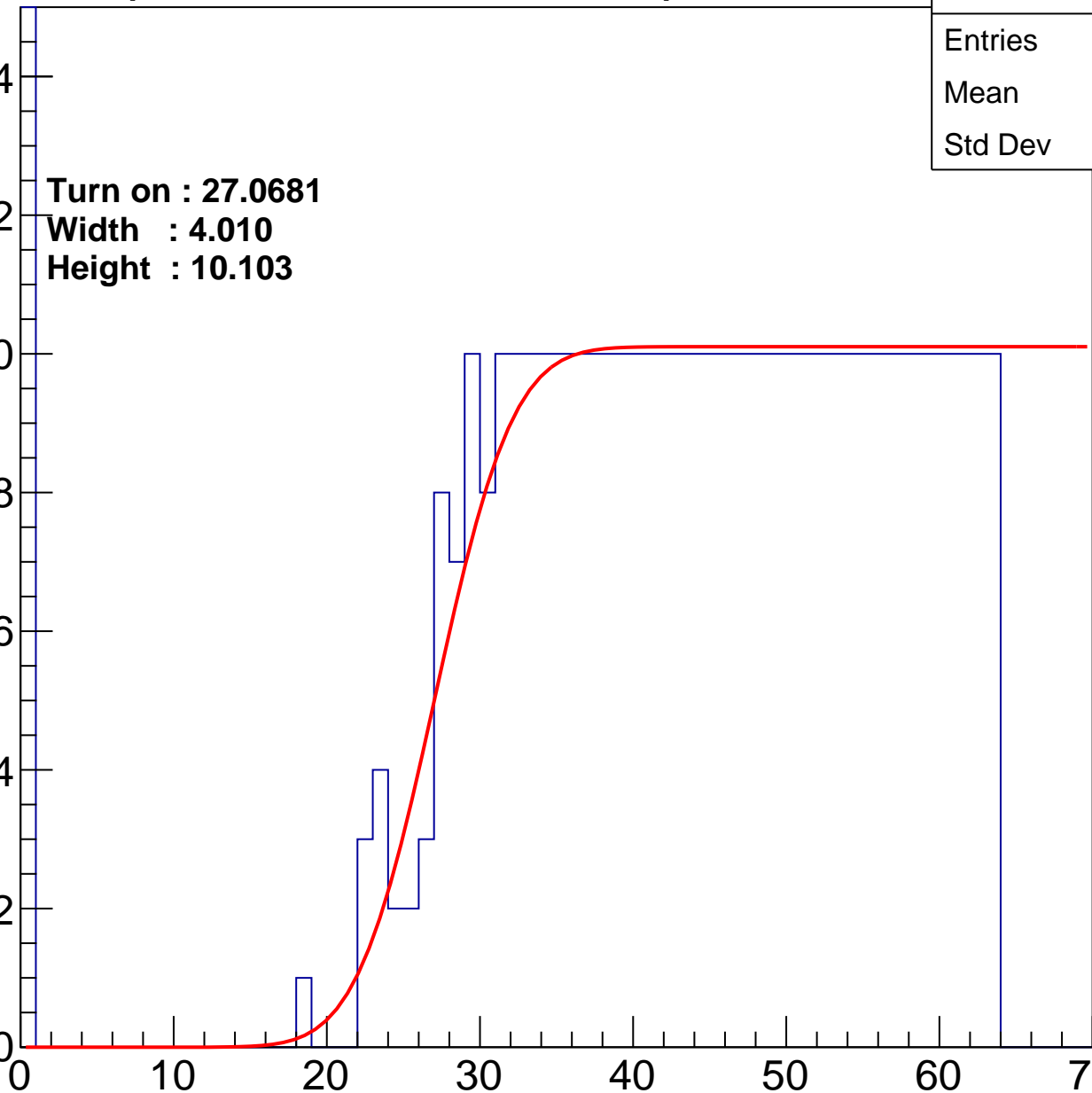
Width : 4.010

Height : 10.103

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch84

calib_packv5_041523_1651.root, FC#0, port C2

Entries	471
Mean	36.78
Std Dev	19

Turn on : 24.2852

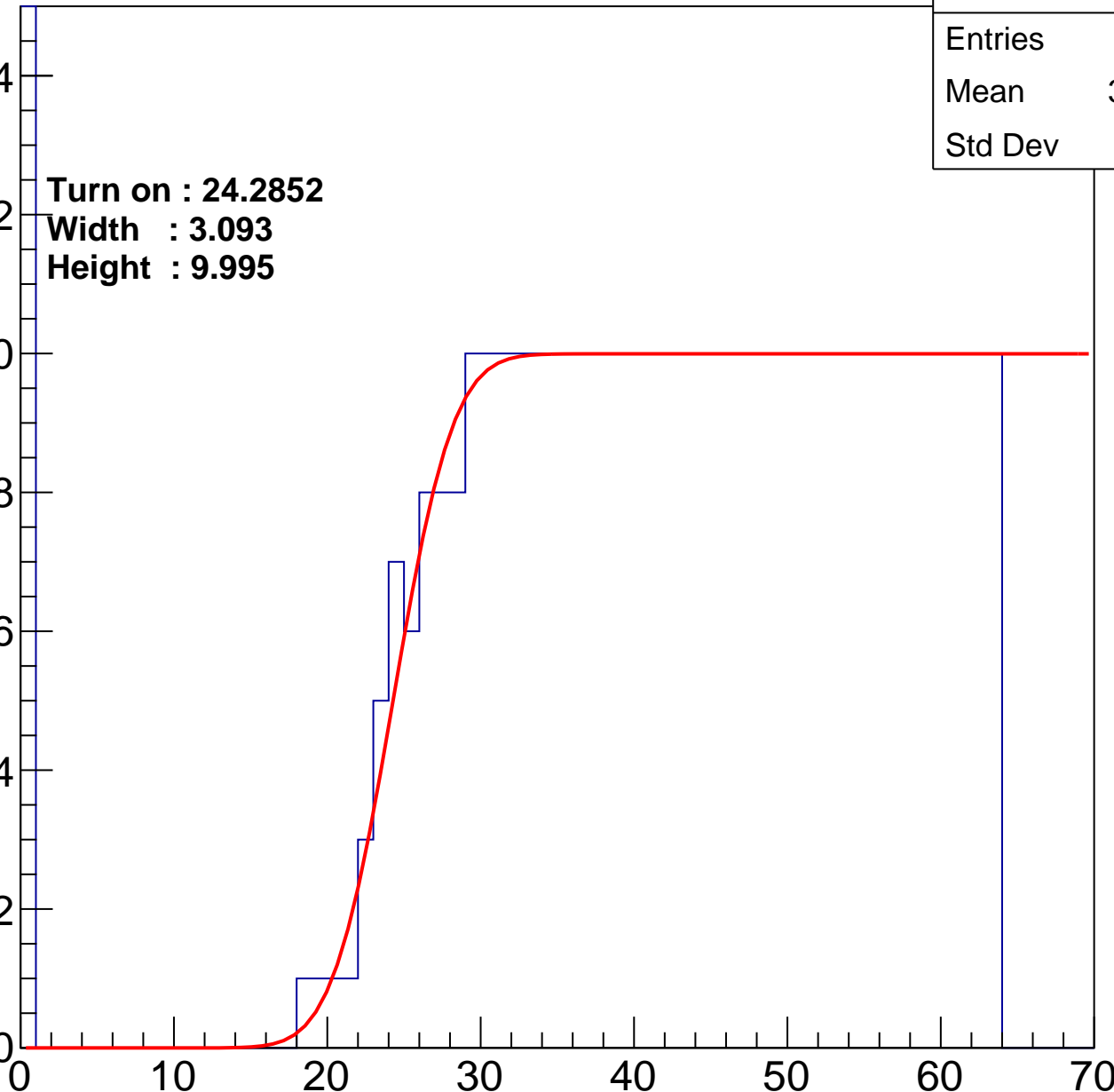
Width : 3.093

Height : 9.995

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch85

calib_packv5_041523_1651.root, FC#0, port C2

Entries	446
Mean	38.24
Std Dev	18.23

Turn on : 25.6777

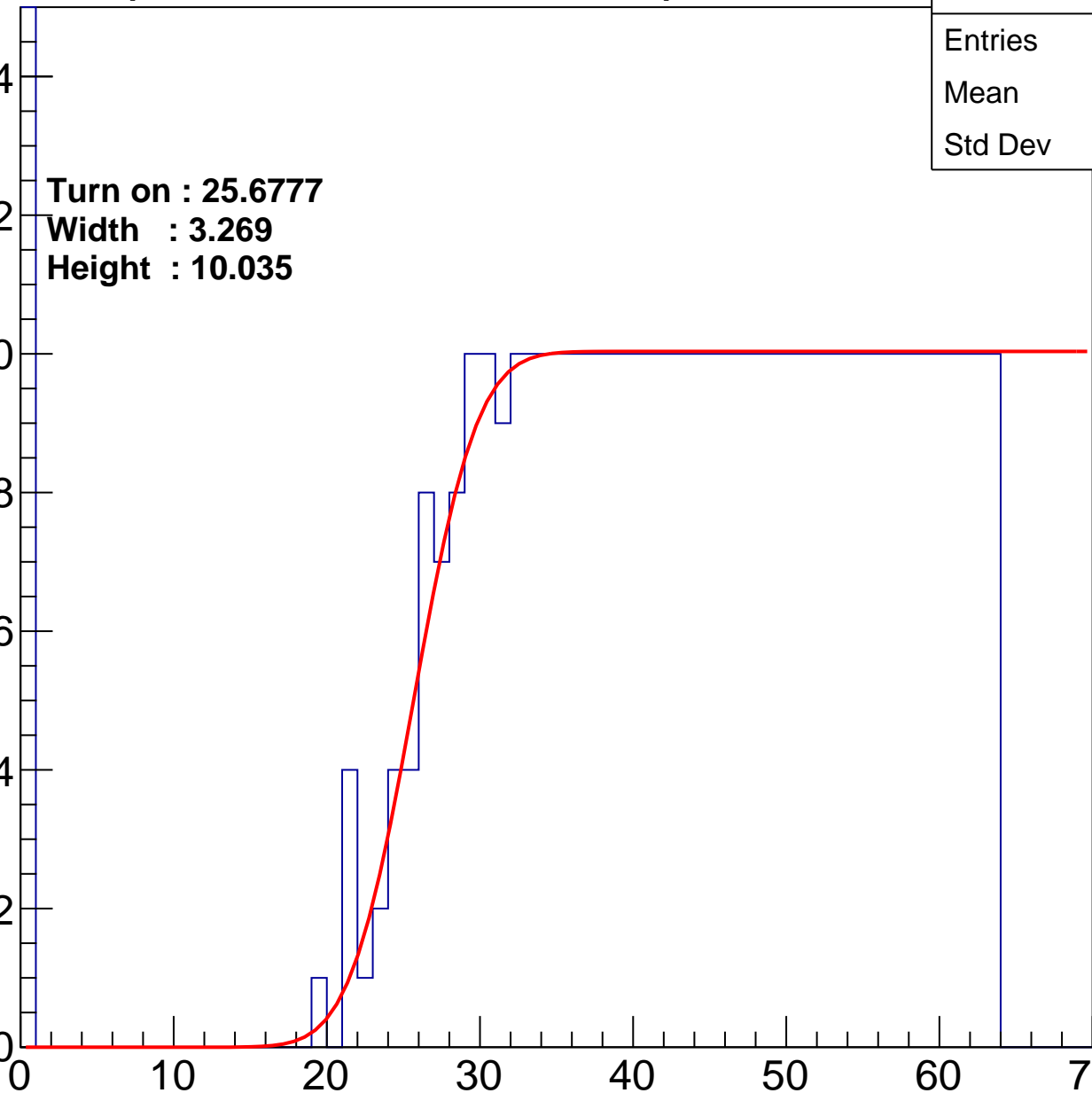
Width : 3.269

Height : 10.035

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch86

calib_packv5_041523_1651.root, FC#0, port C2

Entries	440
Mean	38.44
Std Dev	18.28

Turn on : 26.0471

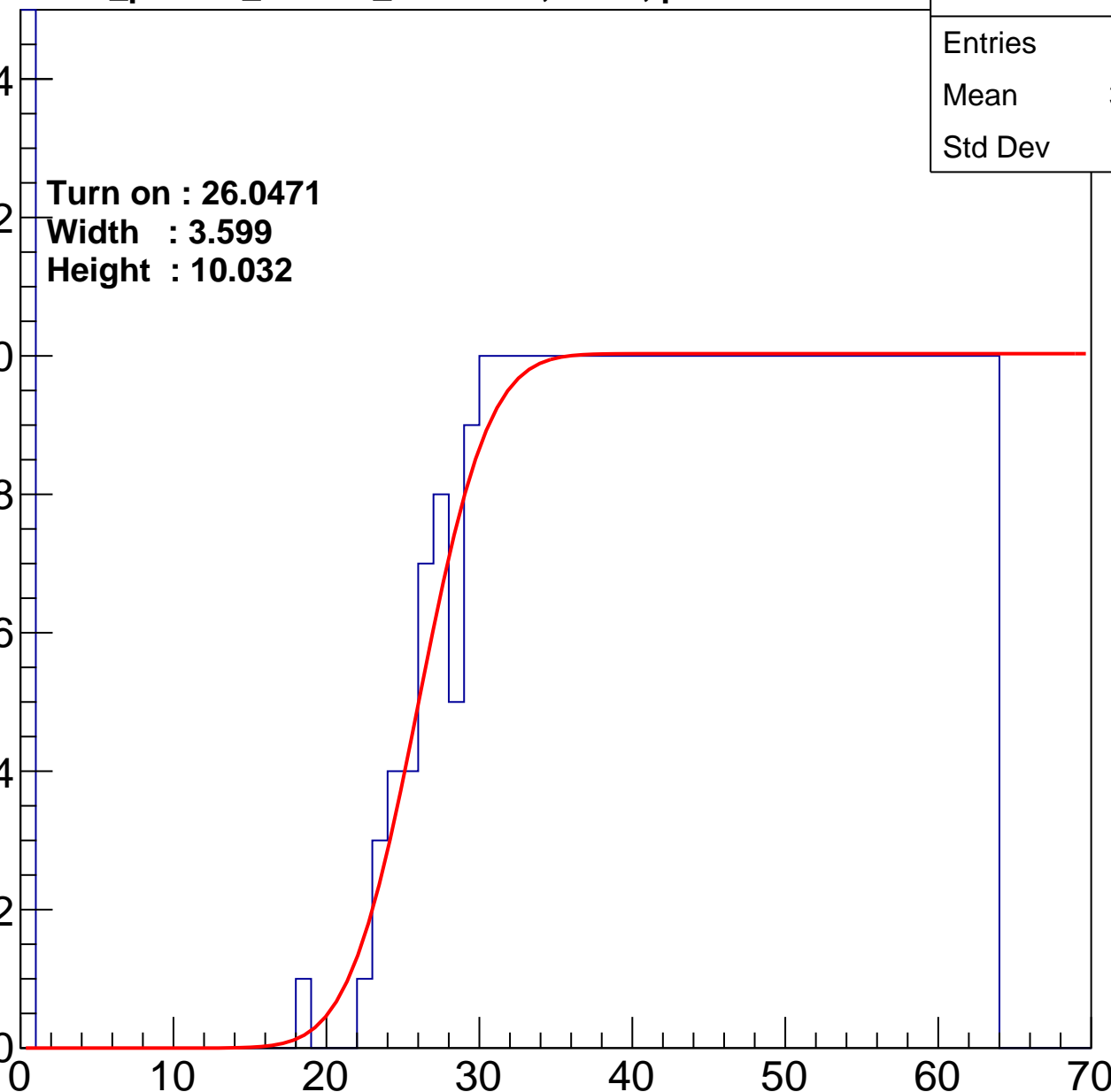
Width : 3.599

Height : 10.032

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch87

calib_packv5_041523_1651.root, FC#0, port C2

Entries	461
Mean	37.19
Std Dev	18.94

Turn on : 24.7975

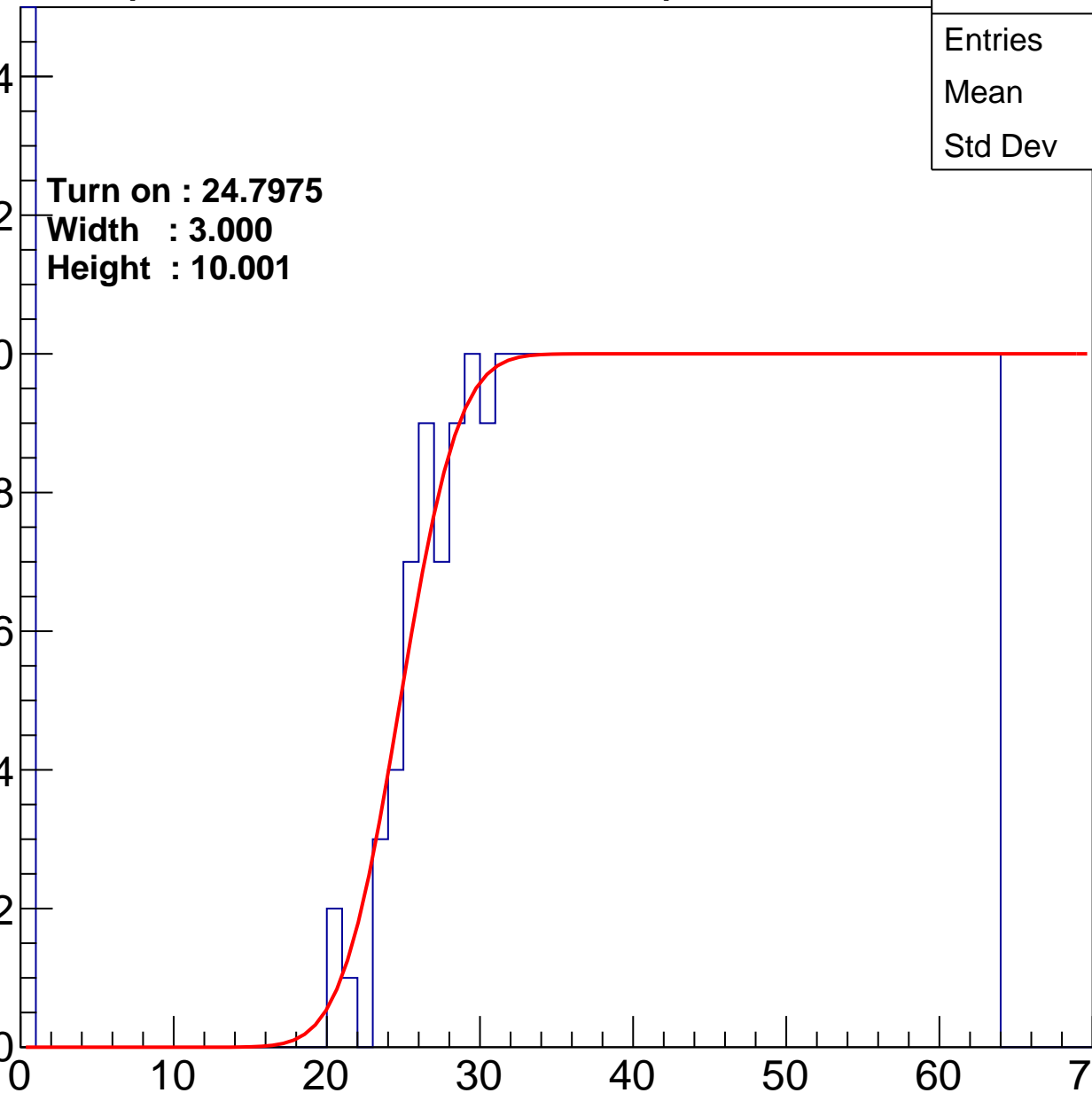
Width : 3.000

Height : 10.001

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch88

calib_packv5_041523_1651.root, FC#0, port C2

Entries	451
Mean	38.61
Std Dev	17.43

Turn on : 23.5372

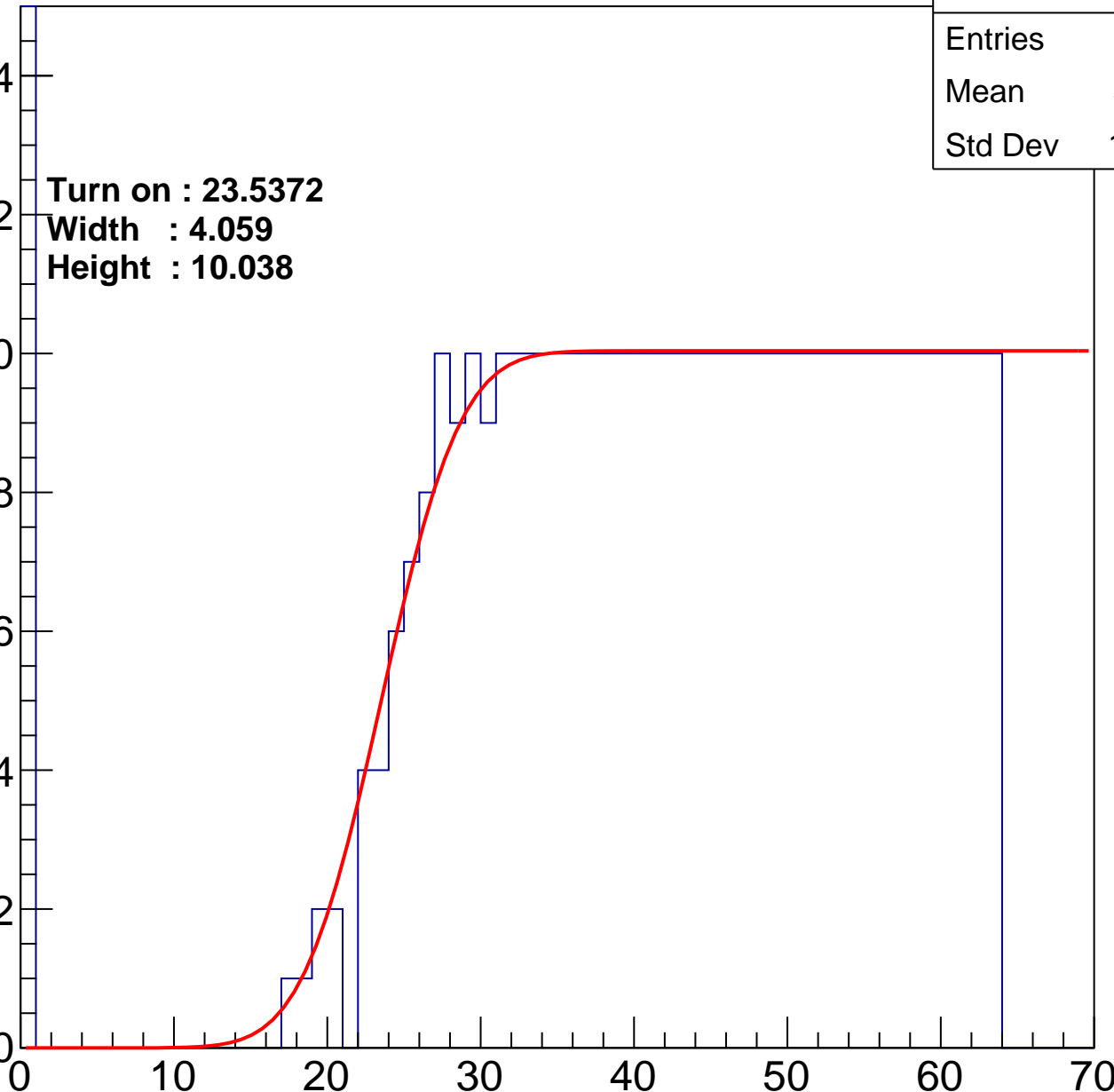
Width : 4.059

Height : 10.038

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch89

calib_packv5_041523_1651.root, FC#0, port C2

Entries	445
Mean	38.18
Std Dev	18.38

Turn on : 25.4375

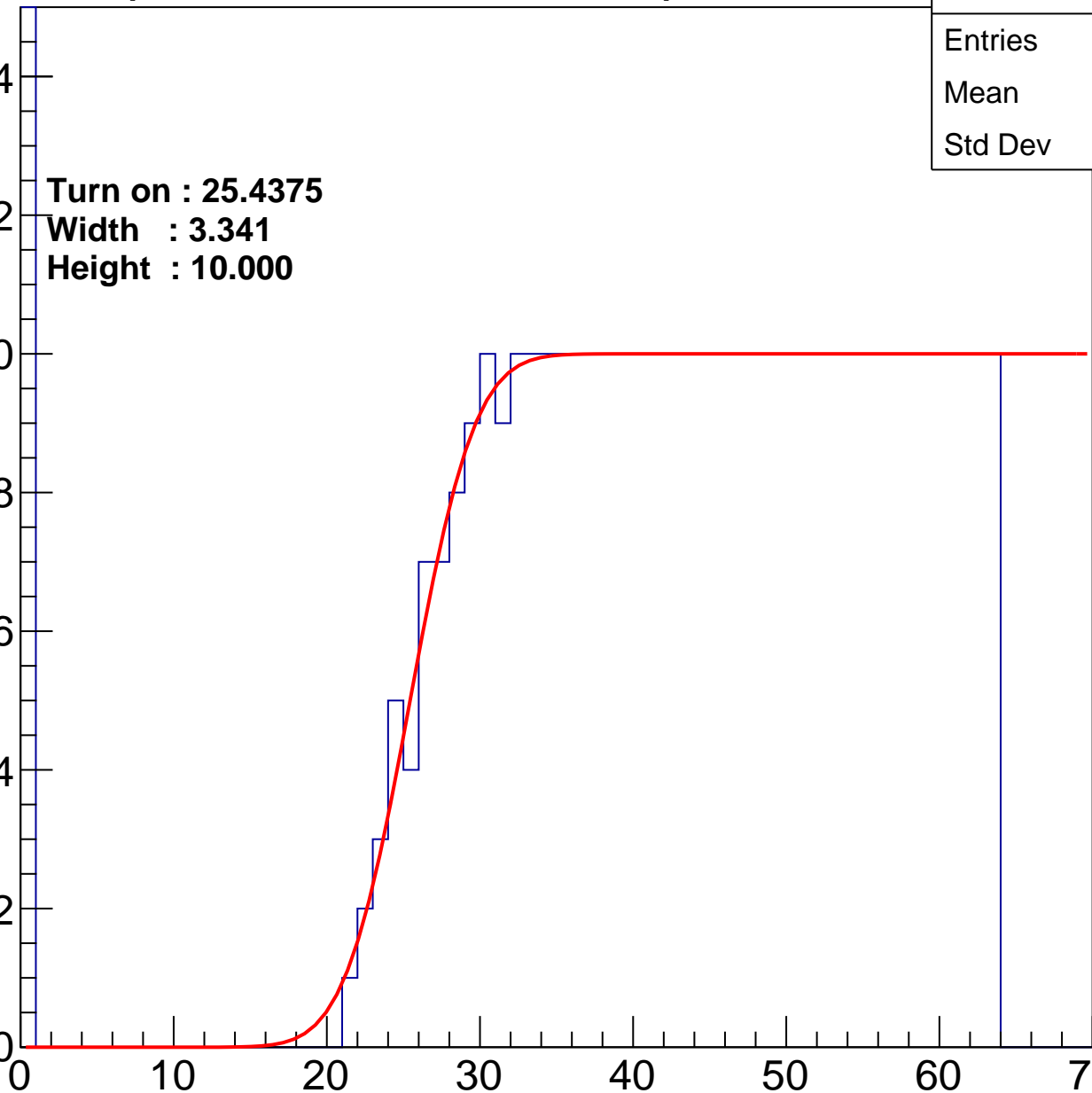
Width : 3.341

Height : 10.000

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch90

calib_packv5_041523_1651.root, FC#0, port C2

Entries	441
Mean	39.18
Std Dev	17.12

Turn on : 24.5586

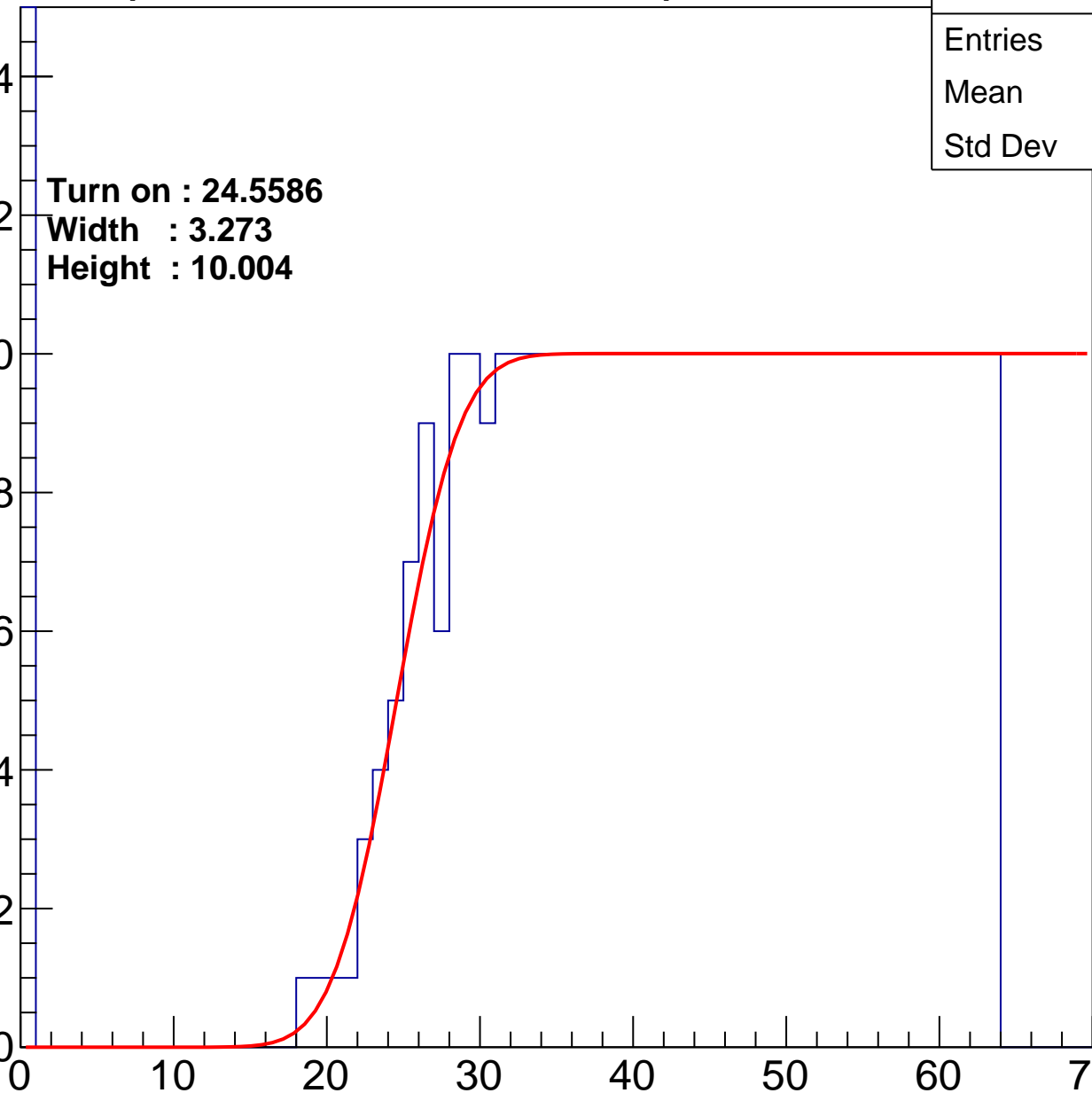
Width : 3.273

Height : 10.004

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch91

calib_packv5_041523_1651.root, FC#0, port C2

Entries	418
Mean	40.38
Std Dev	16.6

Turn on : 26.6022

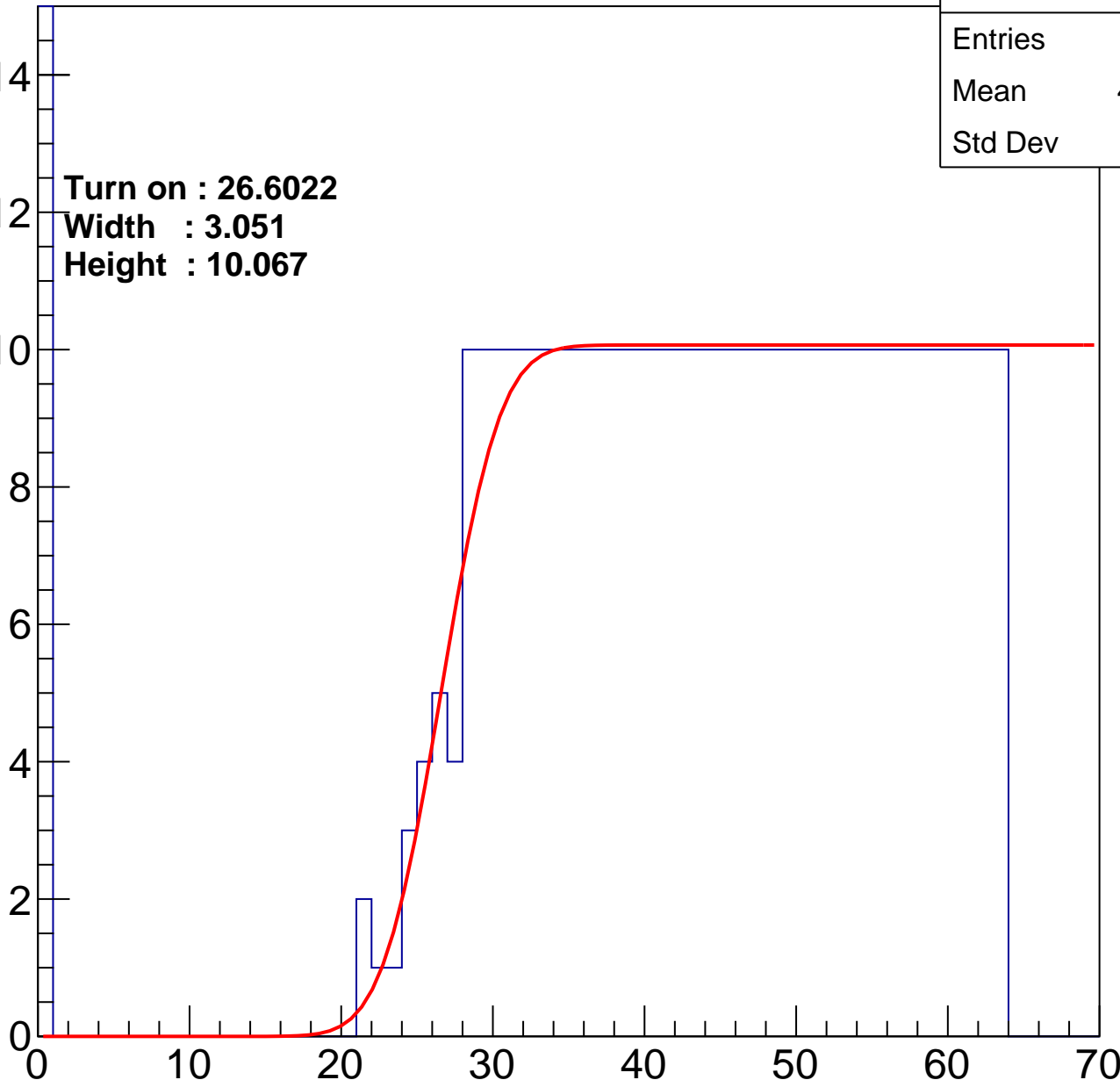
Width : 3.051

Height : 10.067

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch92

calib_packv5_041523_1651.root, FC#0, port C2

Entries	481
Mean	36.53
Std Dev	18.88

Turn on : 22.9621

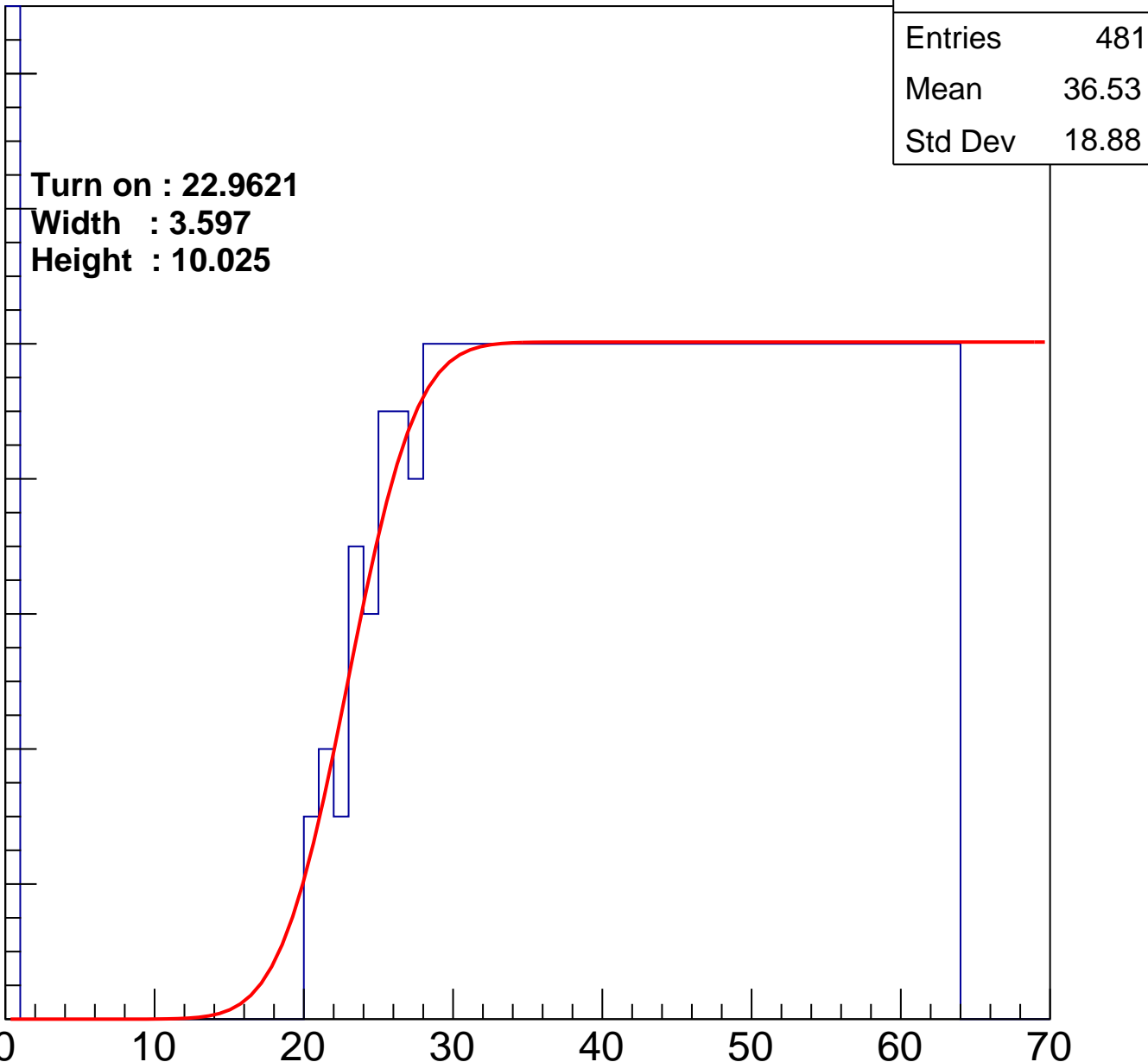
Width : 3.597

Height : 10.025

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch93

calib_packv5_041523_1651.root, FC#0, port C2

Entries	450
Mean	37.28
Std Dev	19.32

Turn on : 26.5864

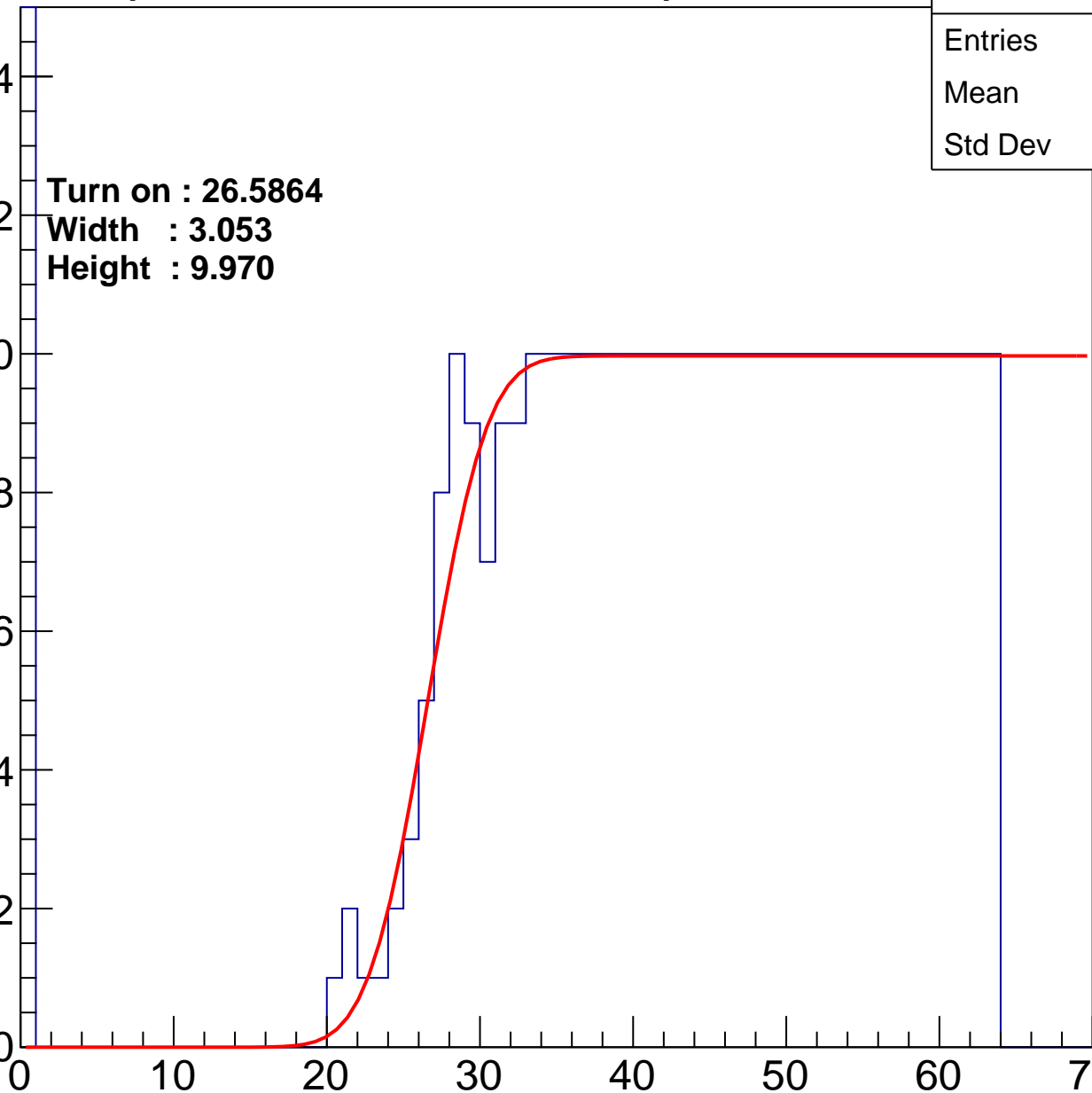
Width : 3.053

Height : 9.970

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch94

calib_packv5_041523_1651.root, FC#0, port C2

Entries	451
Mean	38.03
Std Dev	18.28

Turn on : 24.5817

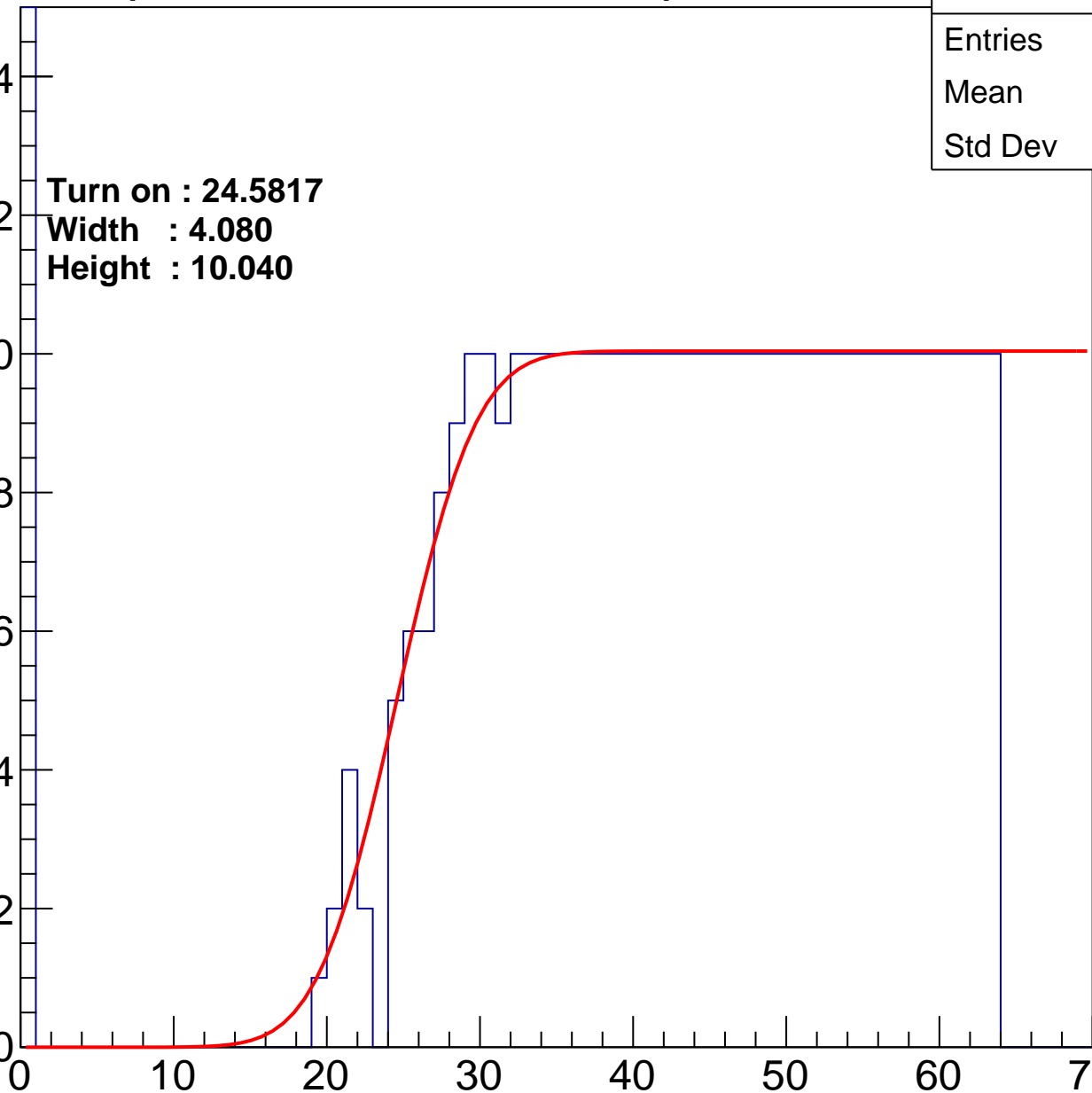
Width : 4.080

Height : 10.040

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch95

calib_packv5_041523_1651.root, FC#0, port C2

Entries	457
Mean	37.25
Std Dev	19.05

Turn on : 25.5929

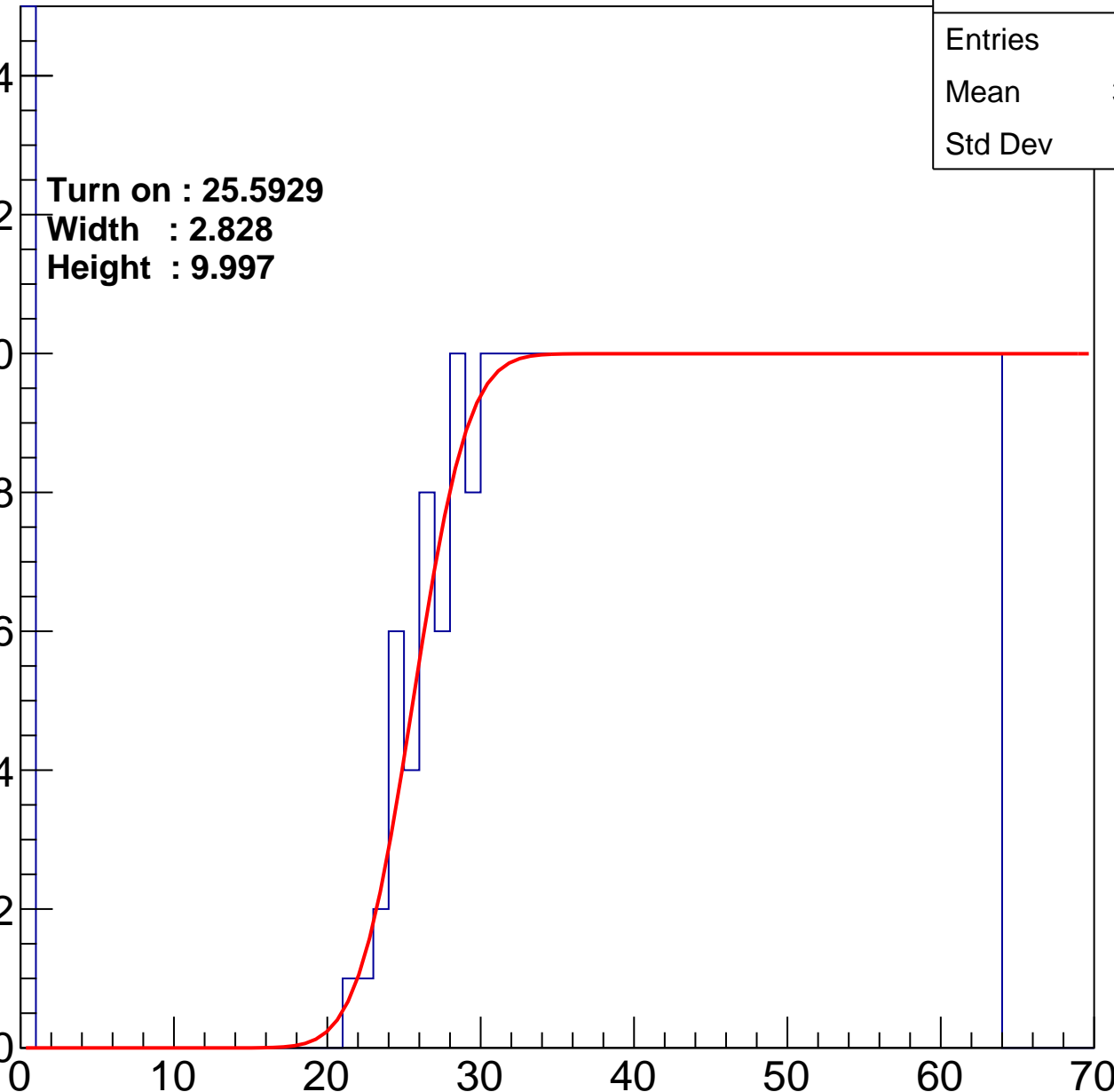
Width : 2.828

Height : 9.997

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch96

calib_packv5_041523_1651.root, FC#0, port C2

Entries	461
Mean	37.77
Std Dev	18.12

Turn on : 23.7358

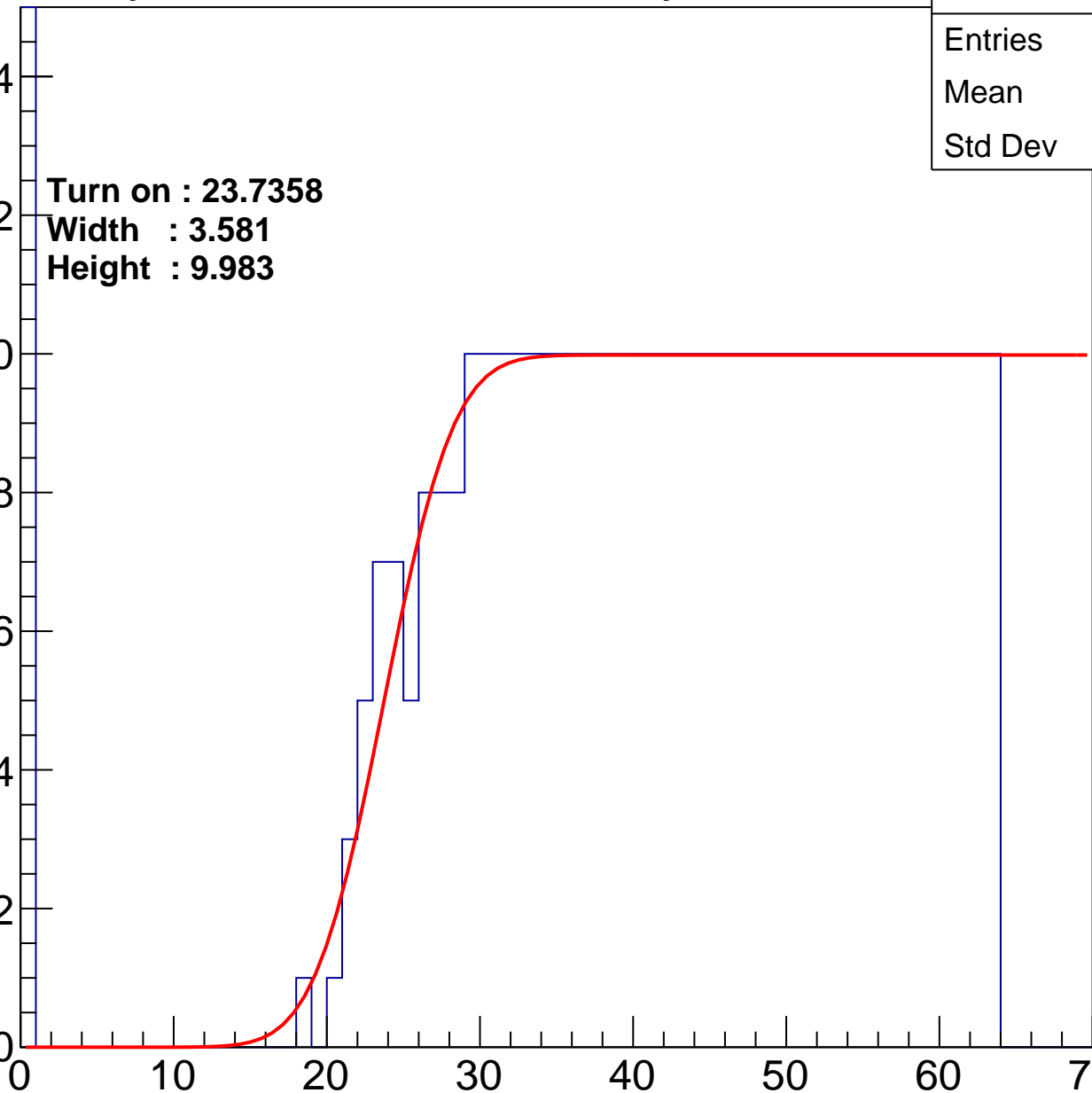
Width : 3.581

Height : 9.983

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch97

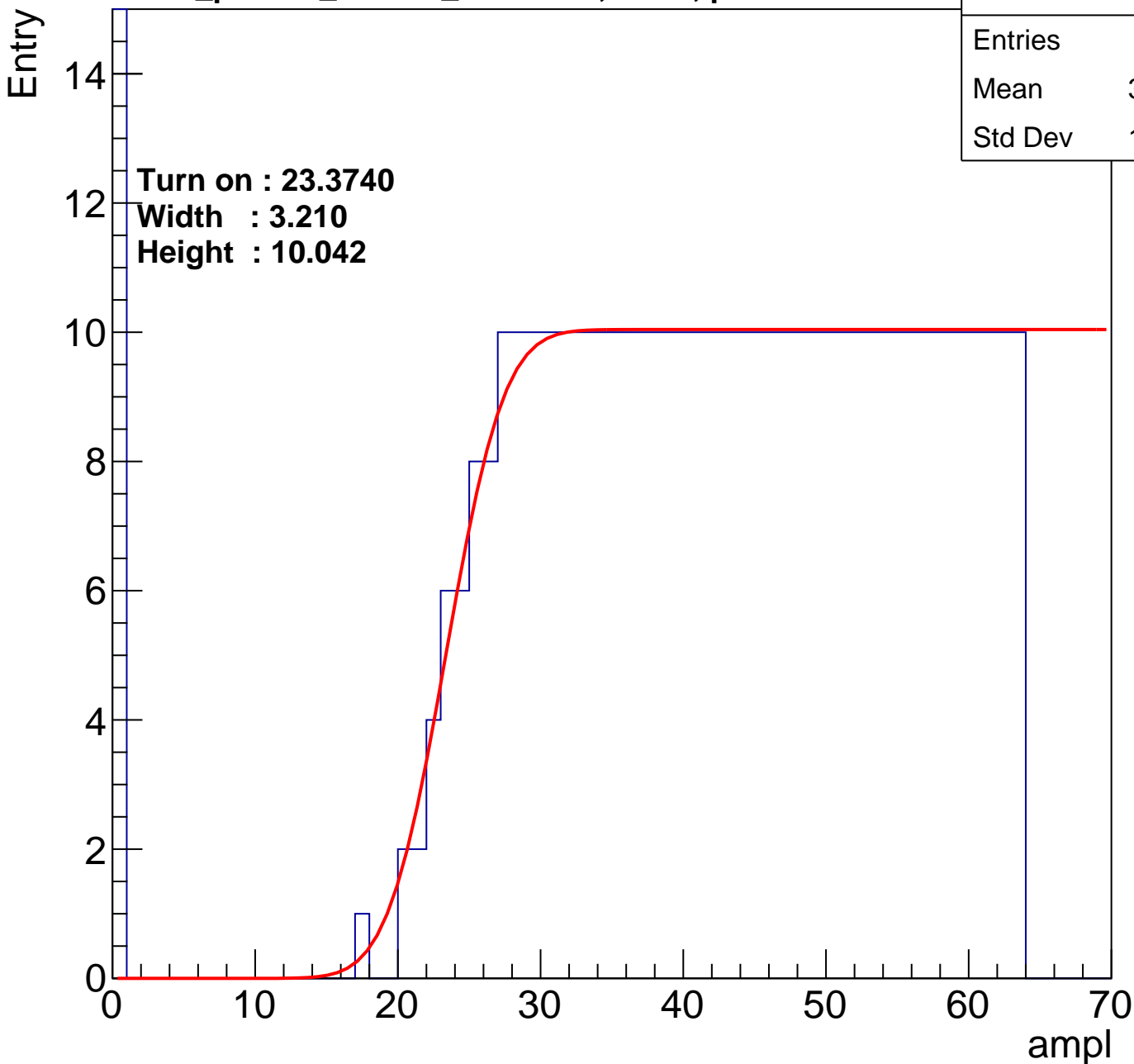
calib_packv5_041523_1651.root, FC#0, port C2

Entries	463
Mean	37.86
Std Dev	17.93

Turn on : 23.3740

Width : 3.210

Height : 10.042



B1L103S, U2-ch98

calib_packv5_041523_1651.root, FC#0, port C2

Entries	445
Mean	38.49
Std Dev	17.96

Turn on : 25.3859

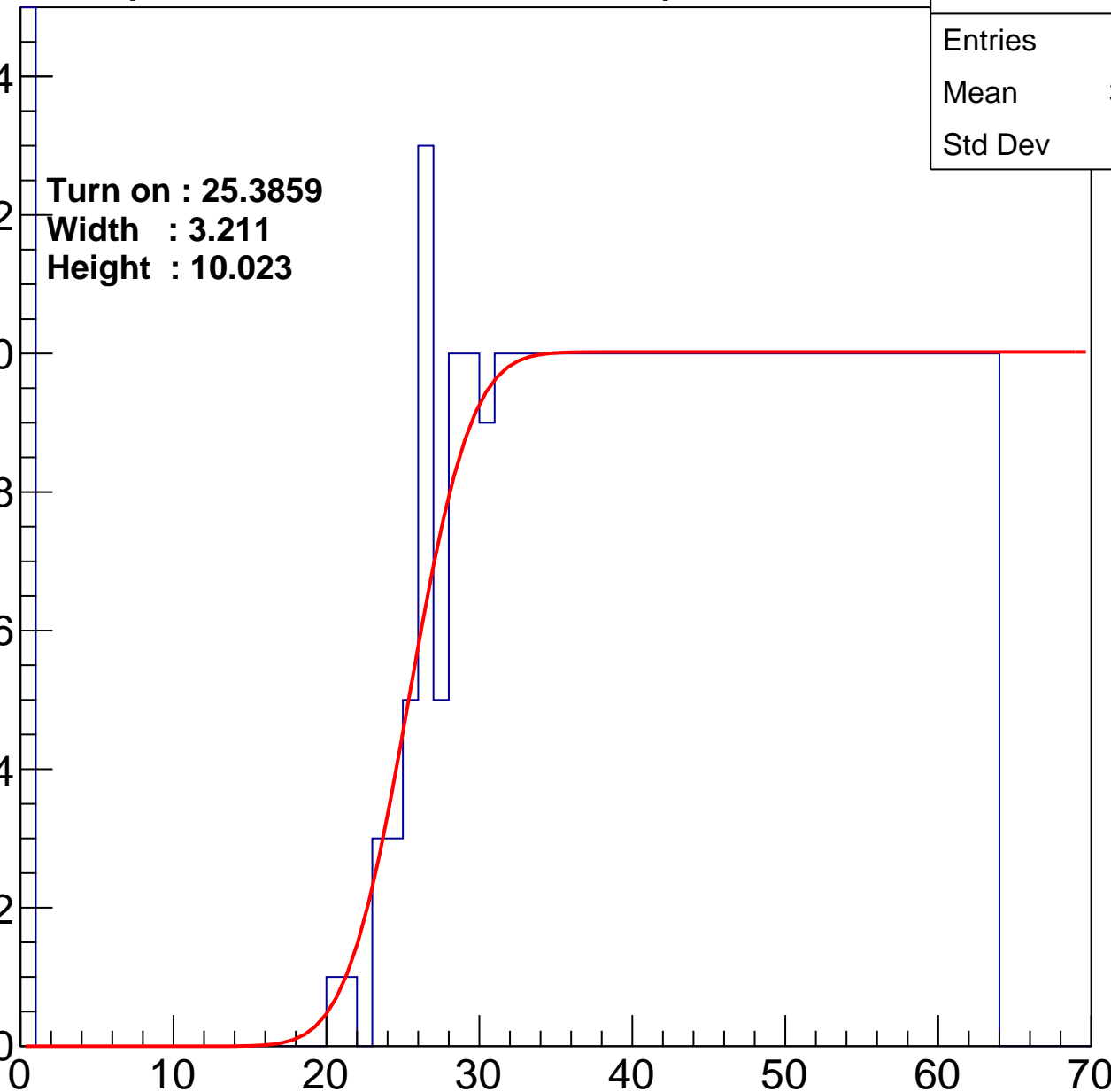
Width : 3.211

Height : 10.023

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch99

calib_packv5_041523_1651.root, FC#0, port C2

Entries	495
Mean	35.7
Std Dev	19.31

Turn on : 23.2772

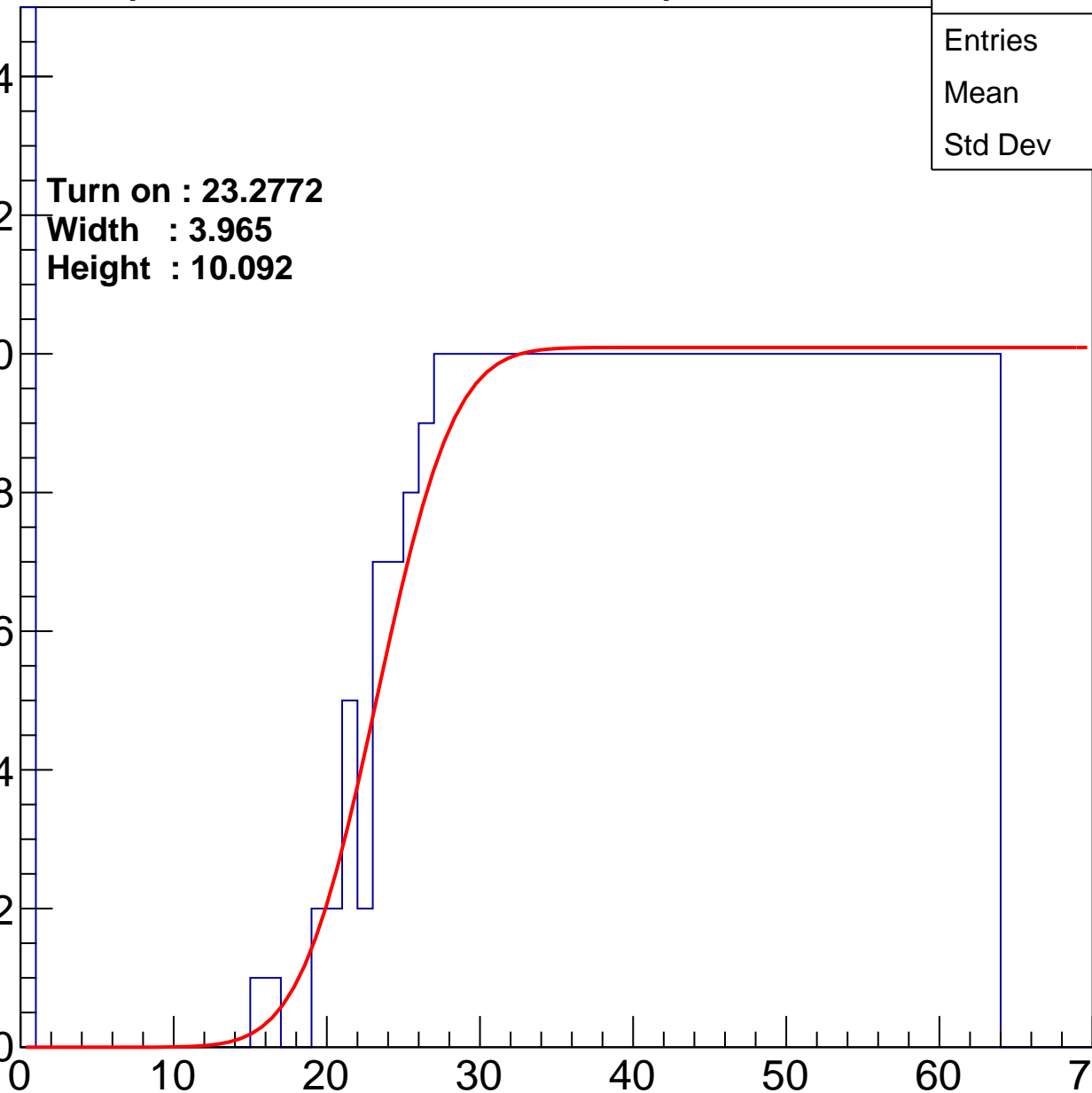
Width : 3.965

Height : 10.092

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch100

calib_packv5_041523_1651.root, FC#0, port C2

Entries	459
Mean	37.53
Std Dev	18.56

Turn on : 24.2326

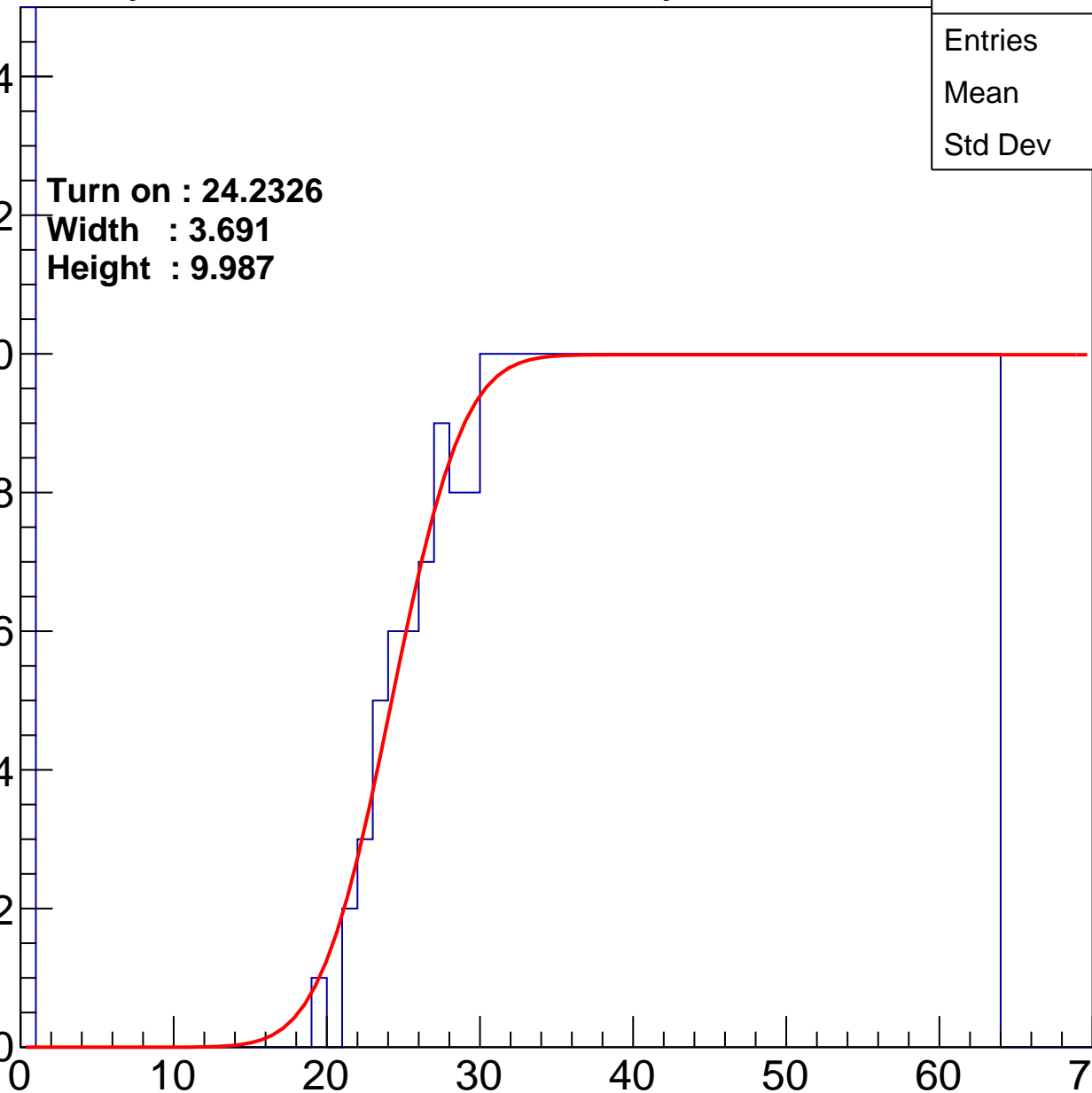
Width : 3.691

Height : 9.987

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch101

calib_packv5_041523_1651.root, FC#0, port C2

Entries	449
Mean	38.03
Std Dev	18.4

Turn on : 24.1612

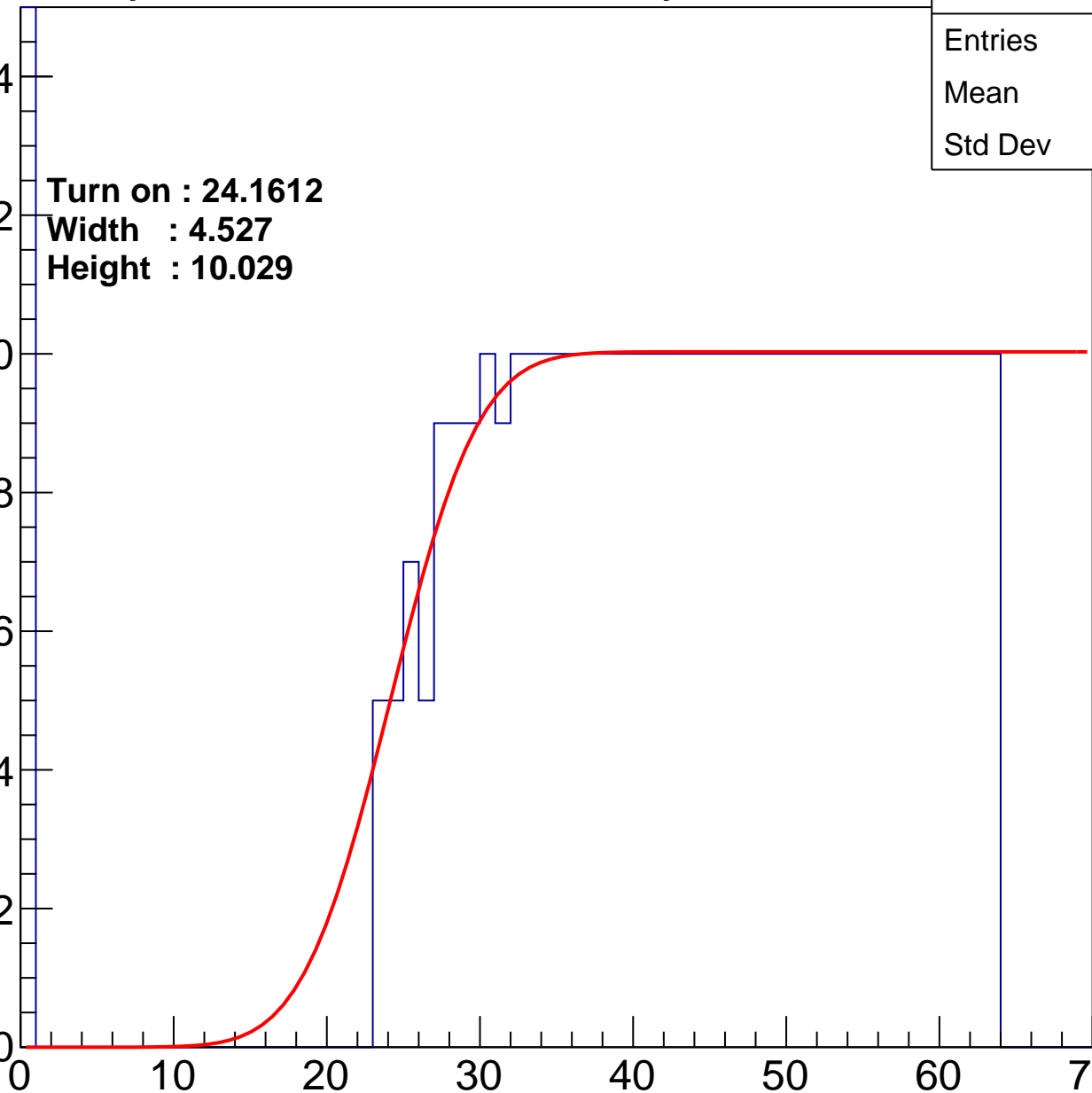
Width : 4.527

Height : 10.029

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch102

calib_packv5_041523_1651.root, FC#0, port C2

Entries	463
Mean	37.79
Std Dev	17.99

Turn on : 24.0375

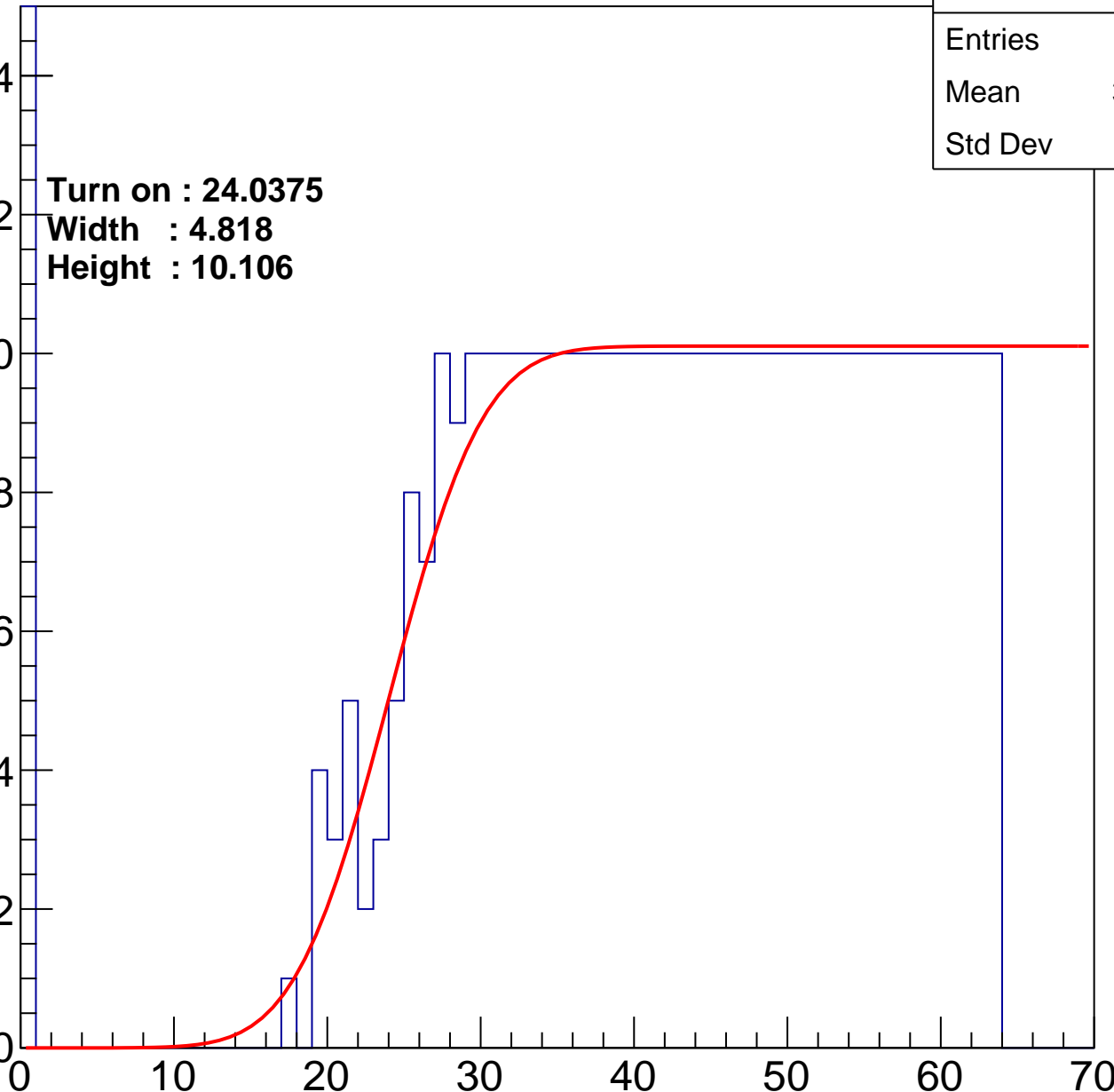
Width : 4.818

Height : 10.106

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch103

calib_packv5_041523_1651.root, FC#0, port C2

Entries	439
Mean	38.56
Std Dev	18.18

Turn on : 25.8735

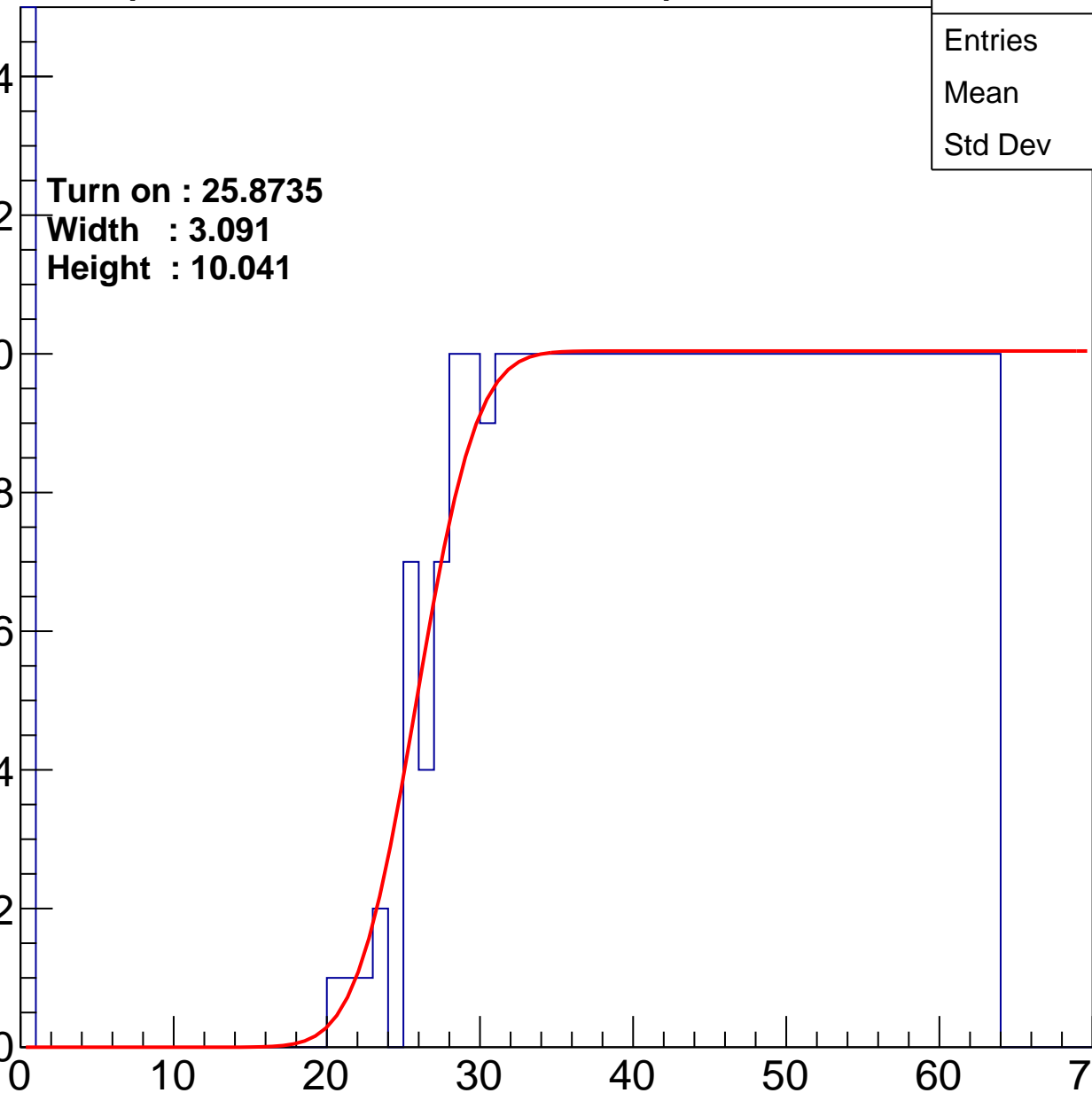
Width : 3.091

Height : 10.041

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch104

calib_packv5_041523_1651.root, FC#0, port C2

Entries	442
Mean	38.39
Std Dev	18.25

Turn on : 26.3042

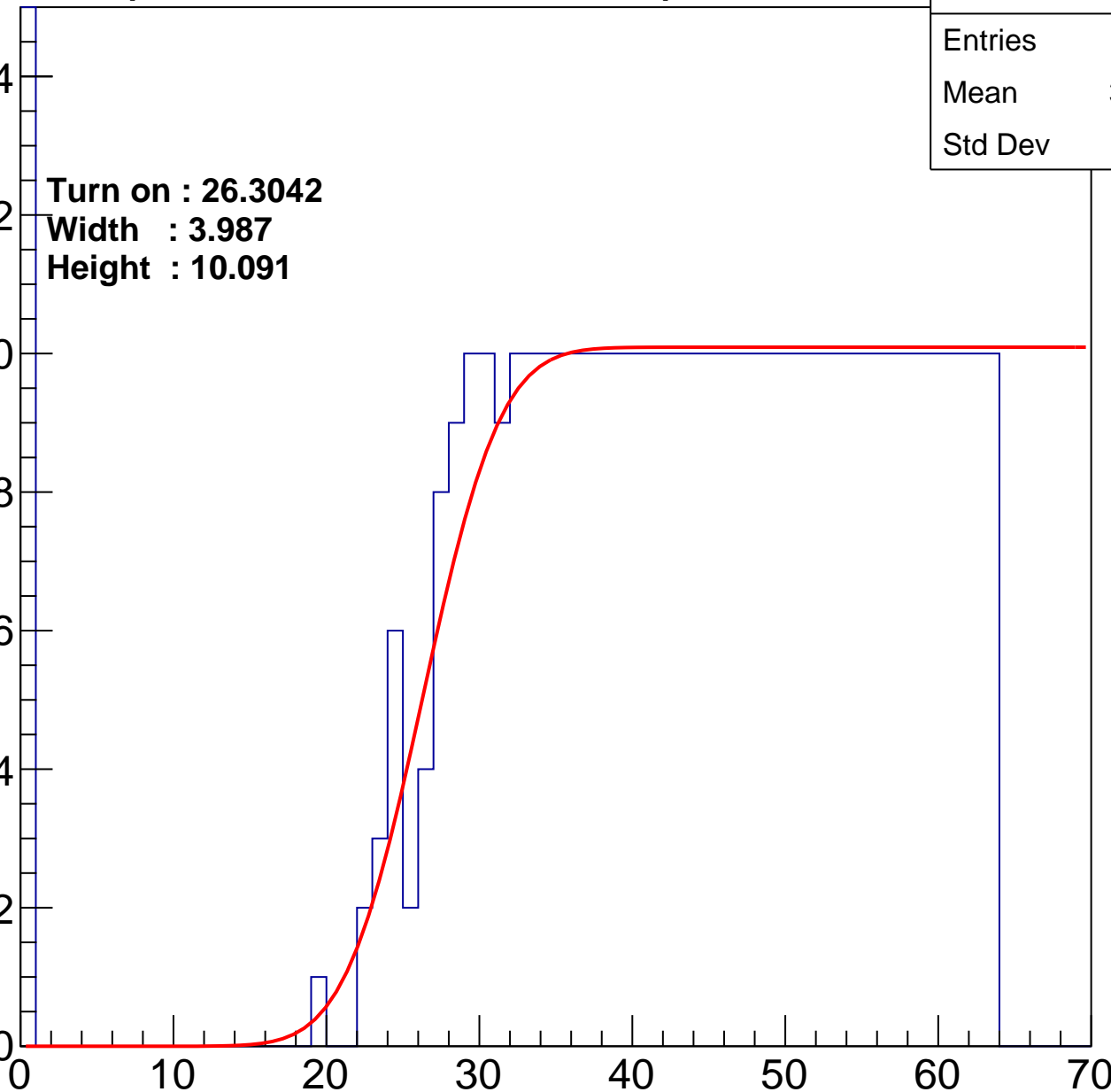
Width : 3.987

Height : 10.091

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch105

calib_packv5_041523_1651.root, FC#0, port C2

Entries	461
Mean	37.29
Std Dev	18.81

Turn on : 24.3533

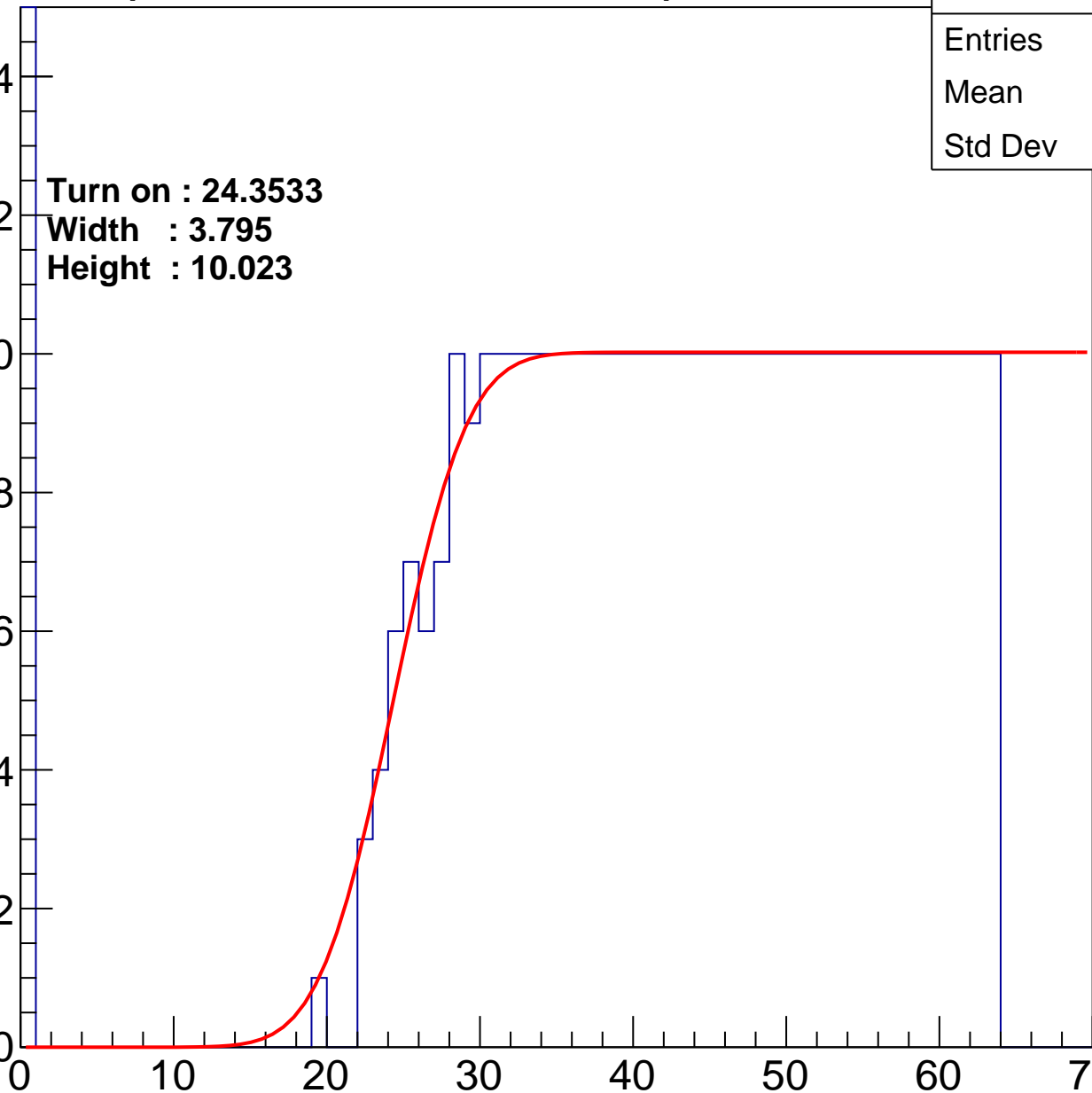
Width : 3.795

Height : 10.023

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch106

calib_packv5_041523_1651.root, FC#0, port C2

Entries	450
Mean	38.18
Std Dev	18.12

Turn on : 24.9650

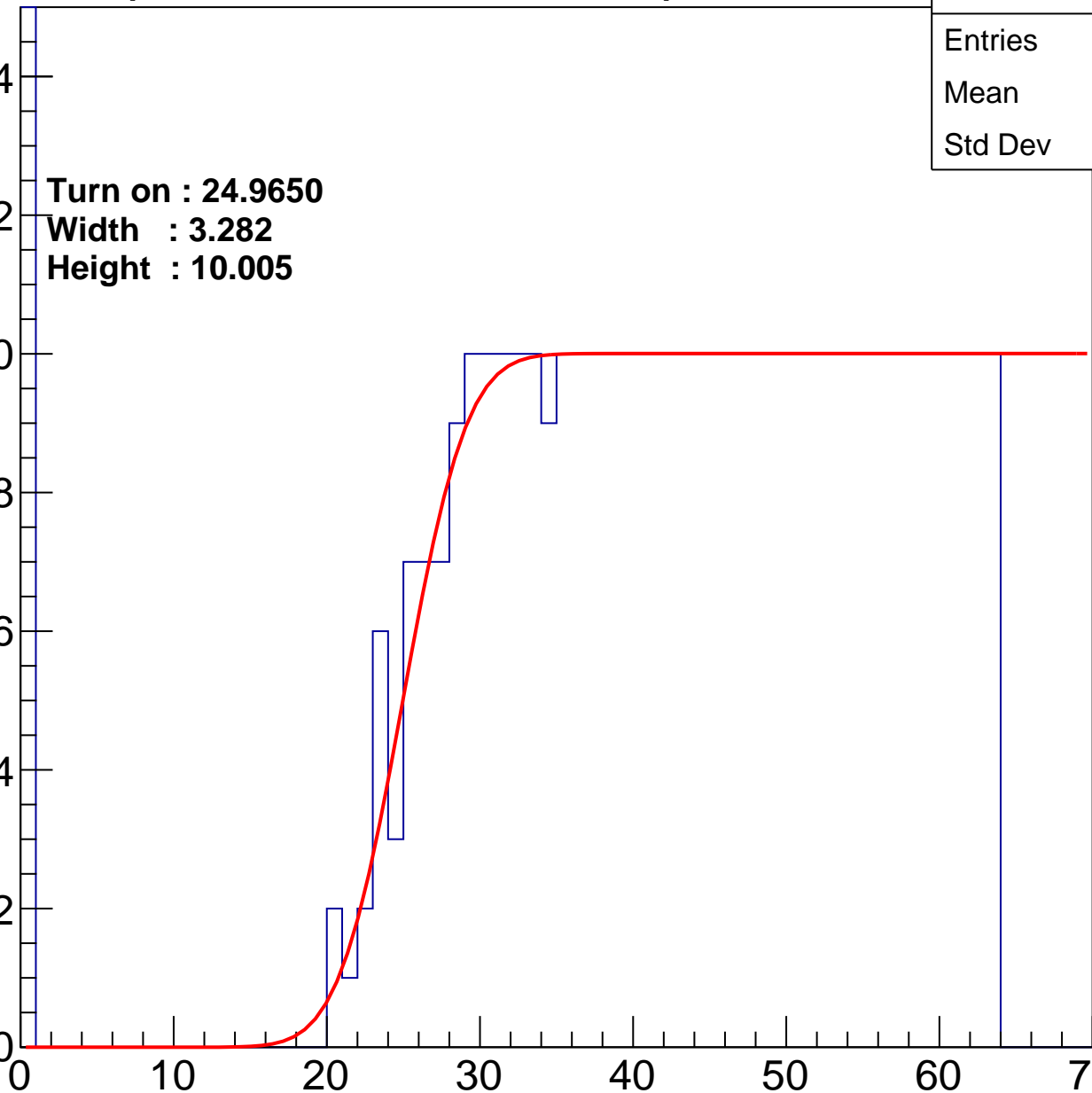
Width : 3.282

Height : 10.005

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch107

calib_packv5_041523_1651.root, FC#0, port C2

Entries	454
Mean	37.64
Std Dev	18.63

Turn on : 25.5576

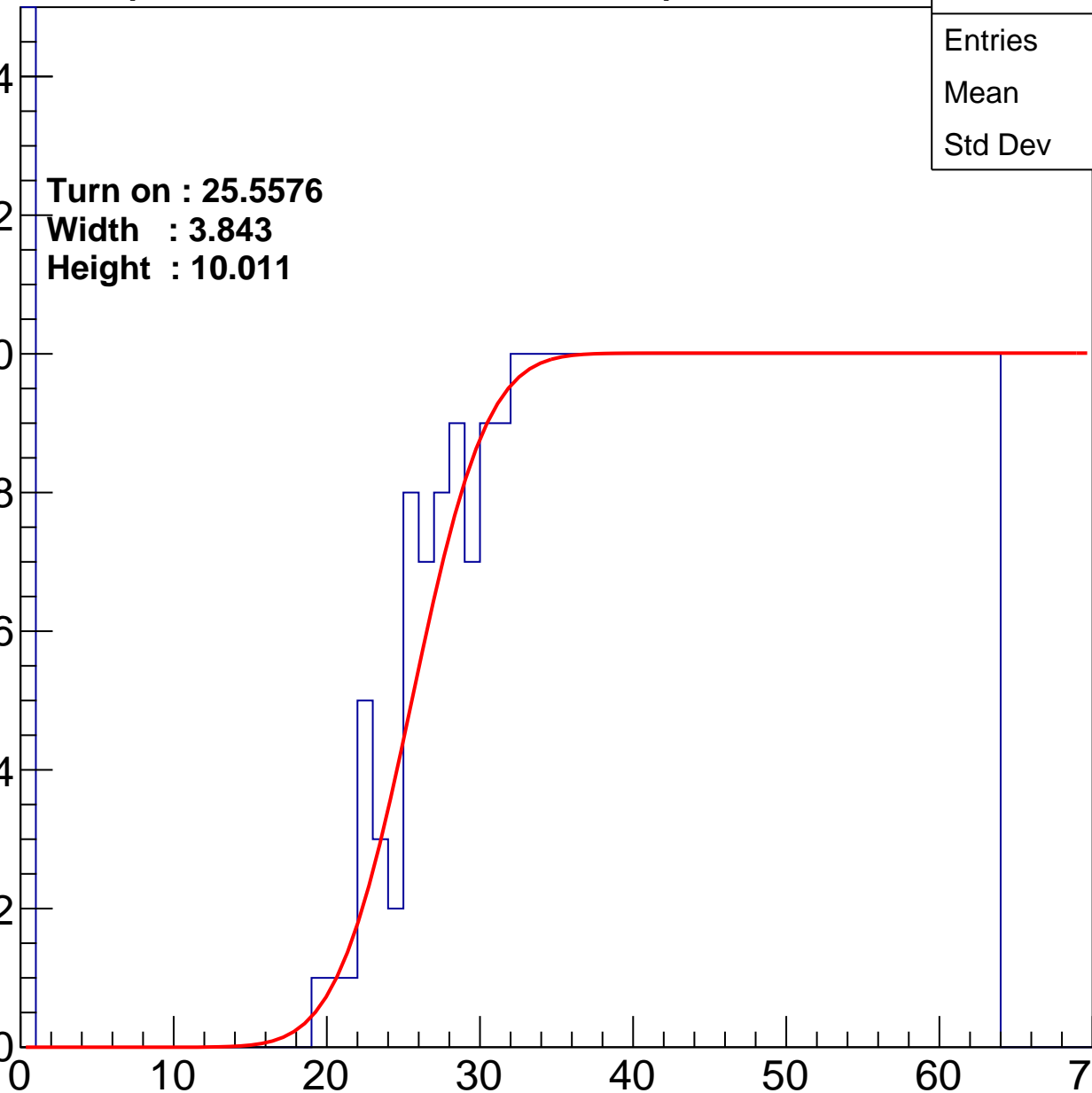
Width : 3.843

Height : 10.011

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch108

calib_packv5_041523_1651.root, FC#0, port C2

Entries	427
Mean	38.34
Std Dev	19.02

Turn on : 28.2996

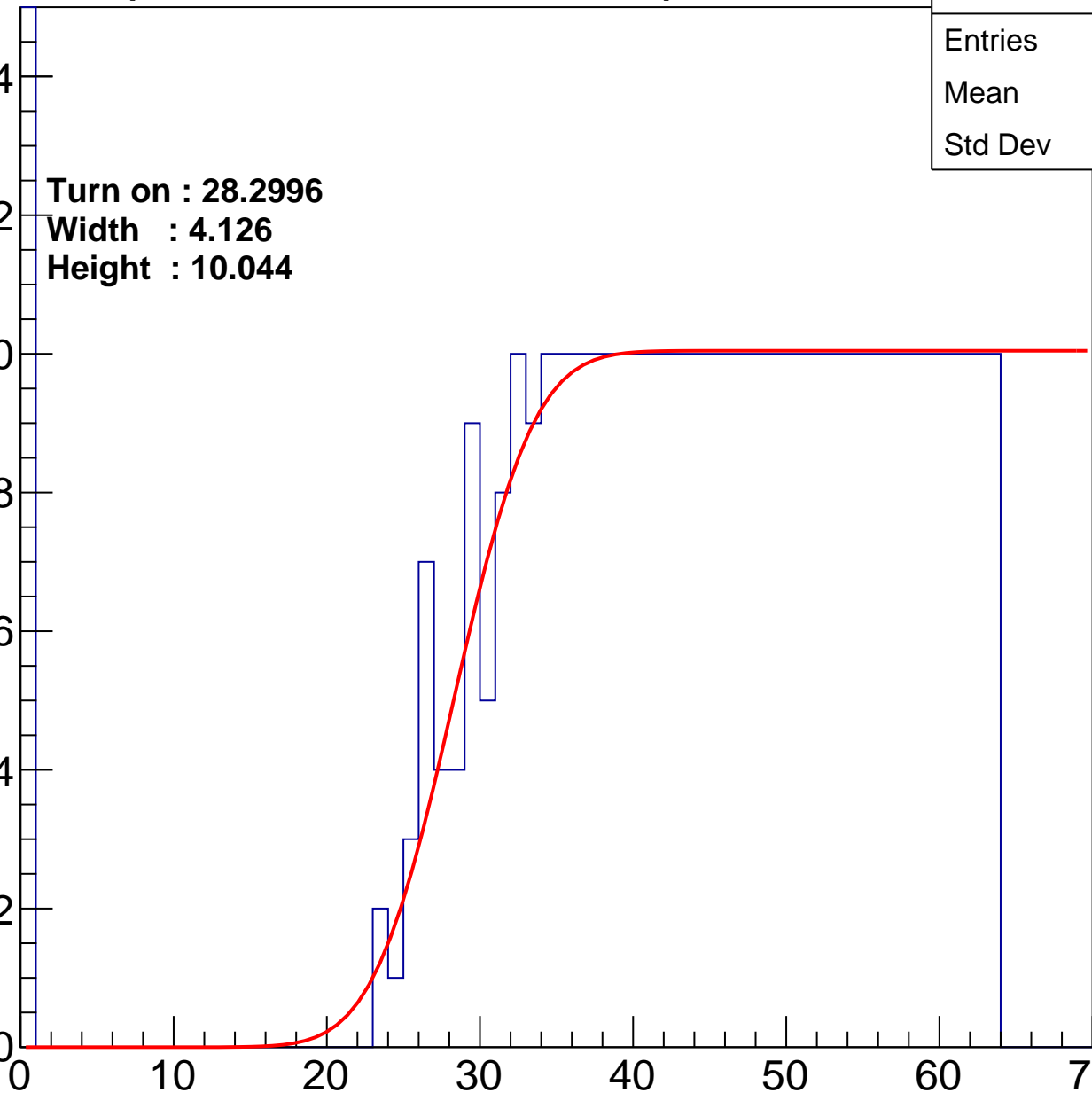
Width : 4.126

Height : 10.044

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch109

calib_packv5_041523_1651.root, FC#0, port C2

Entries	442
Mean	38.31
Std Dev	18.34

Turn on : 25.8655

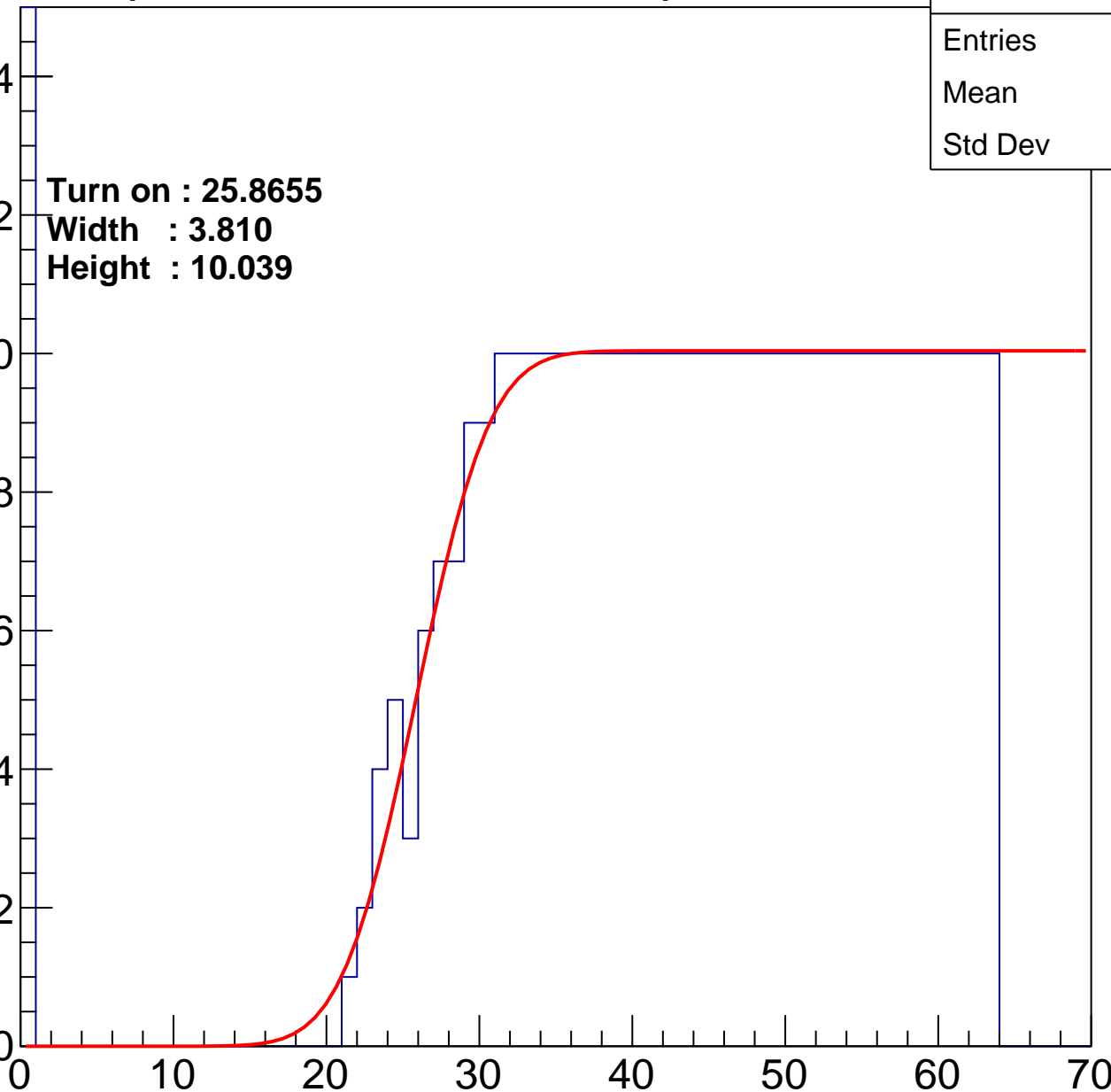
Width : 3.810

Height : 10.039

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch110

calib_packv5_041523_1651.root, FC#0, port C2

Entries	473
Mean	36.89
Std Dev	18.74

Turn on : 23.8878

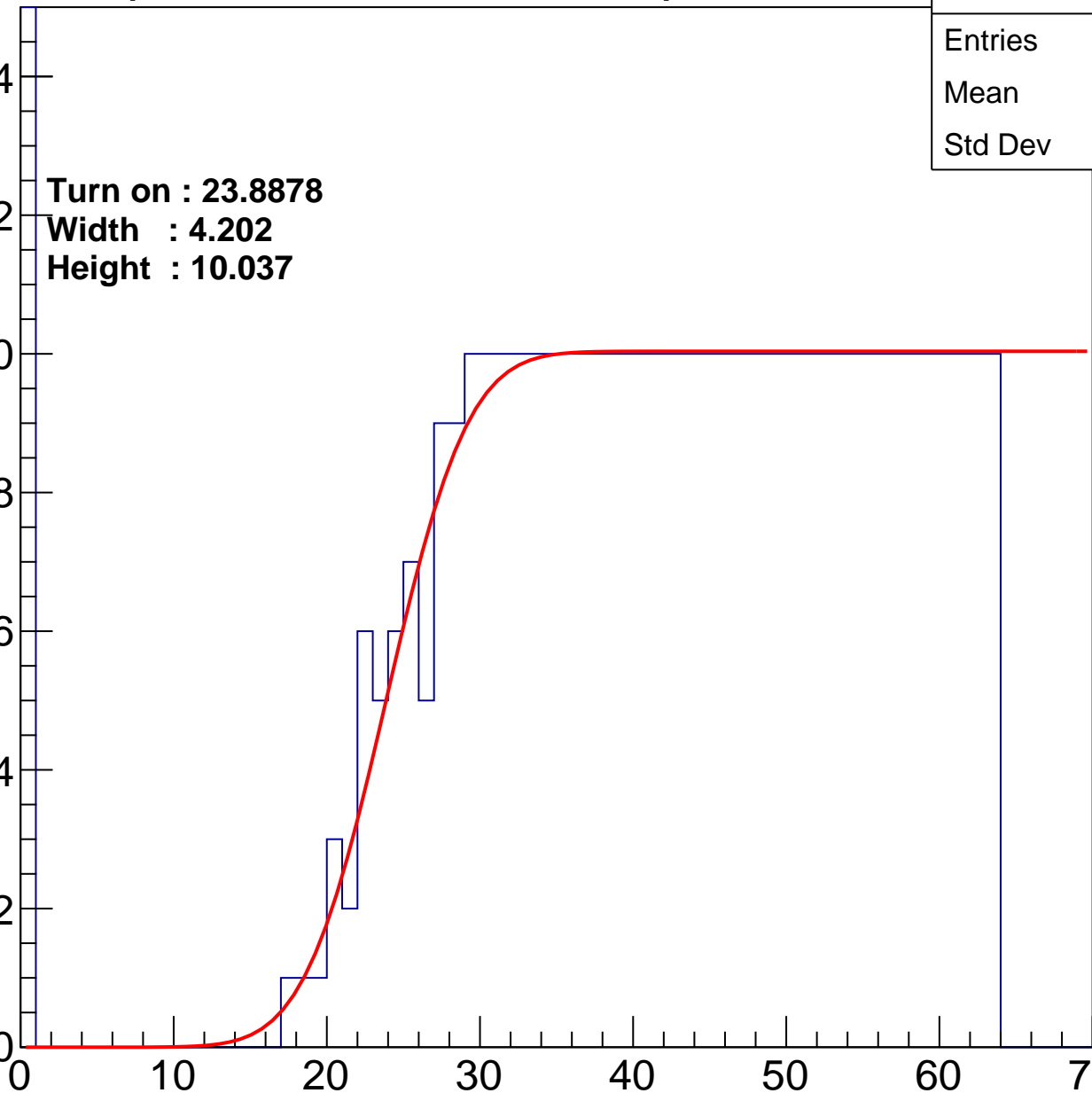
Width : 4.202

Height : 10.037

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch111

calib_packv5_041523_1651.root, FC#0, port C2

Entries	443
Mean	38.3
Std Dev	18.32

Turn on : 26.2324

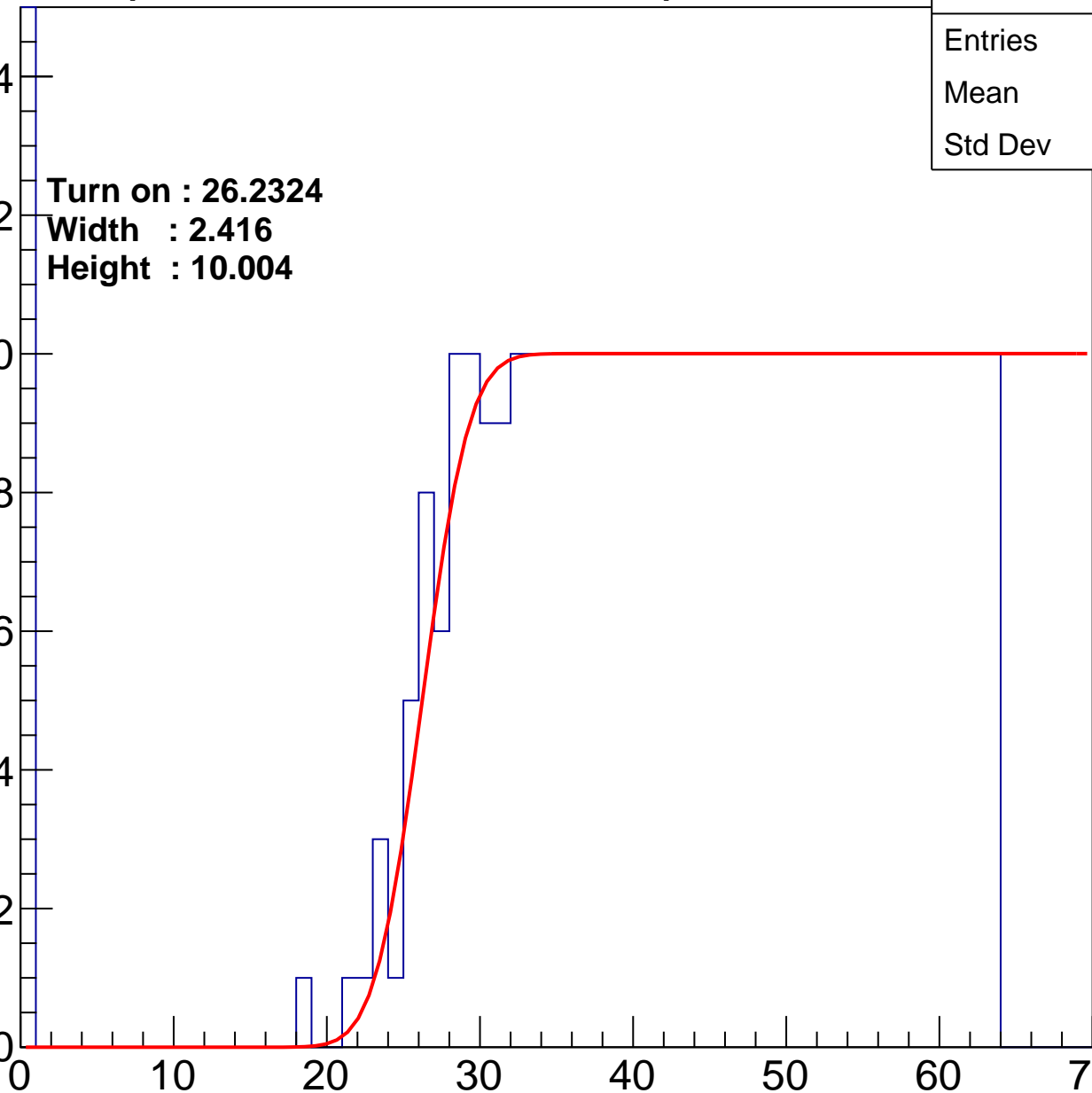
Width : 2.416

Height : 10.004

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch112

calib_packv5_041523_1651.root, FC#0, port C2

Entries	476
Mean	36.73
Std Dev	18.85

Turn on : 23.2559

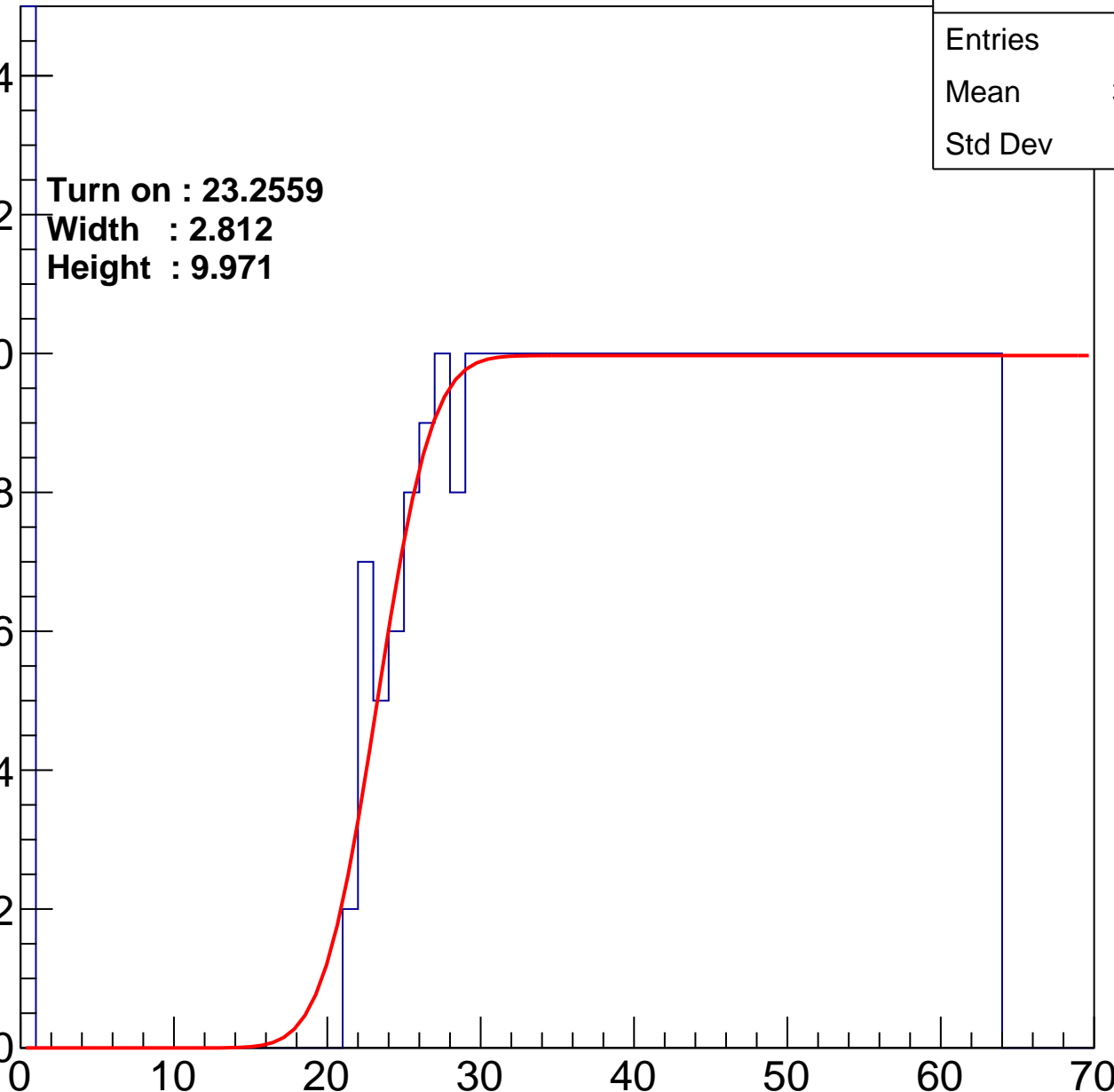
Width : 2.812

Height : 9.971

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch113

calib_packv5_041523_1651.root, FC#0, port C2

Entries	426
Mean	38.06
Std Dev	19.43

Turn on : 28.9180

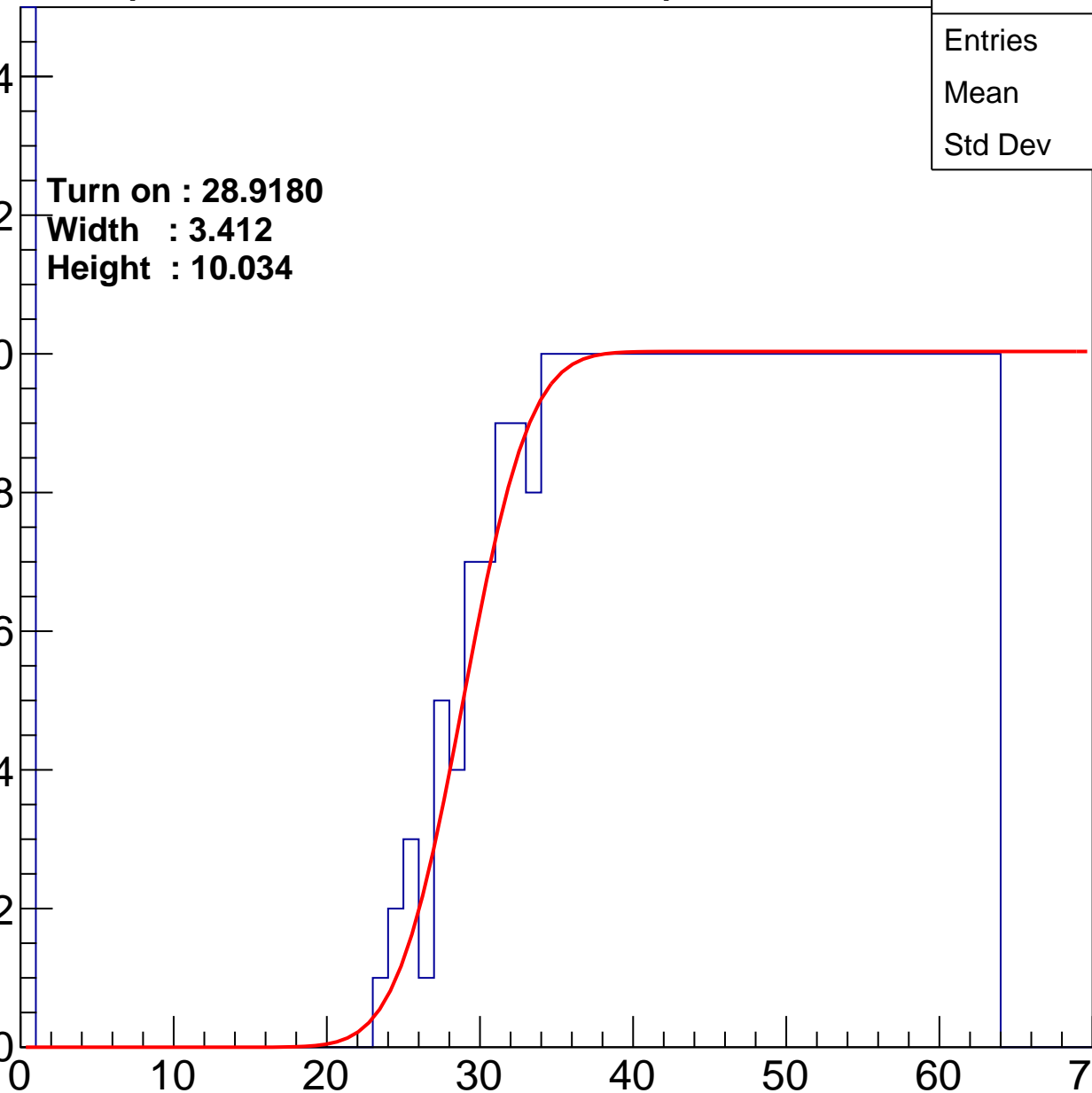
Width : 3.412

Height : 10.034

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch114

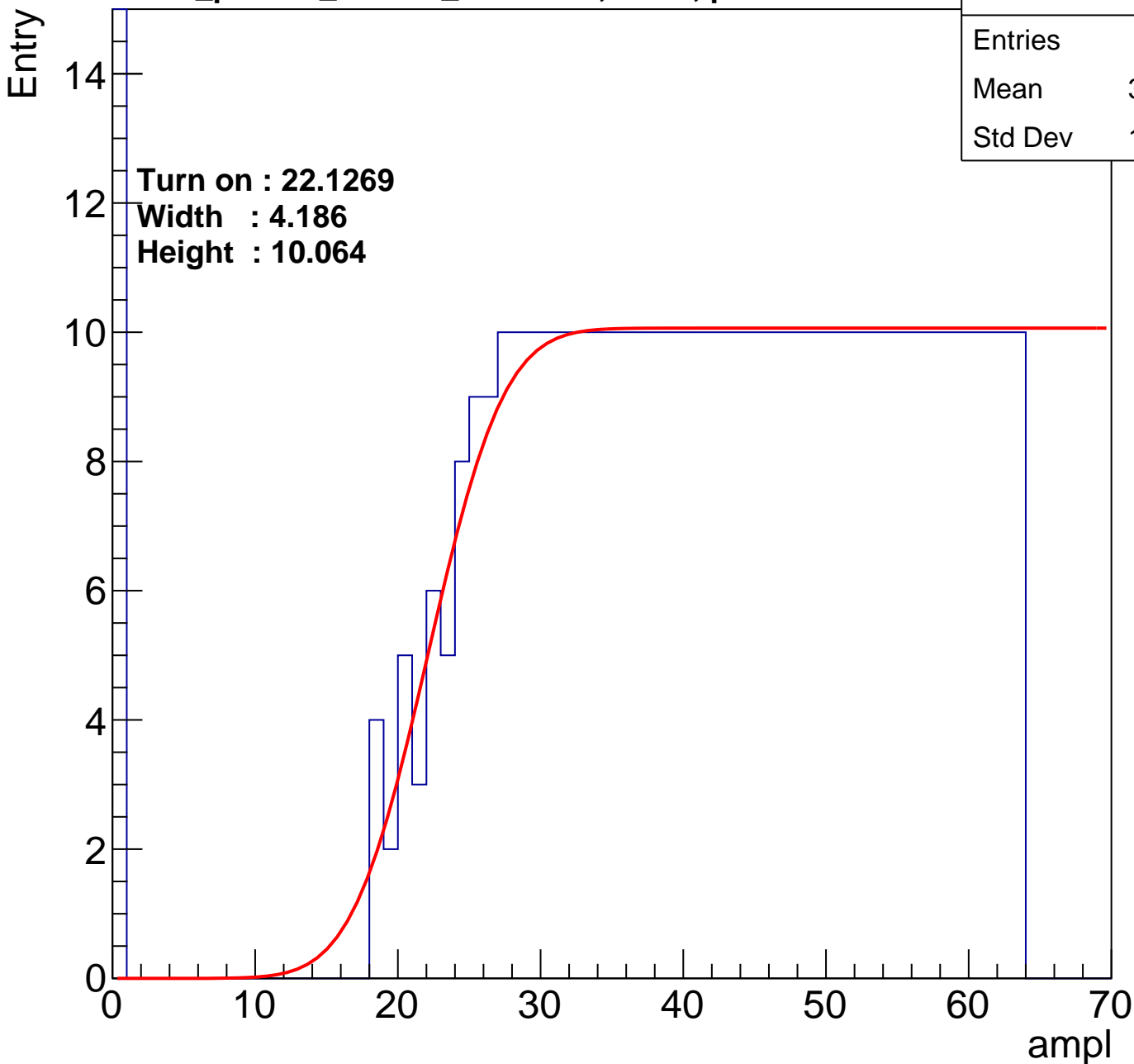
calib_packv5_041523_1651.root, FC#0, port C2

Entries	490
Mean	36.37
Std Dev	18.65

Turn on : 22.1269

Width : 4.186

Height : 10.064



B1L103S, U2-ch115

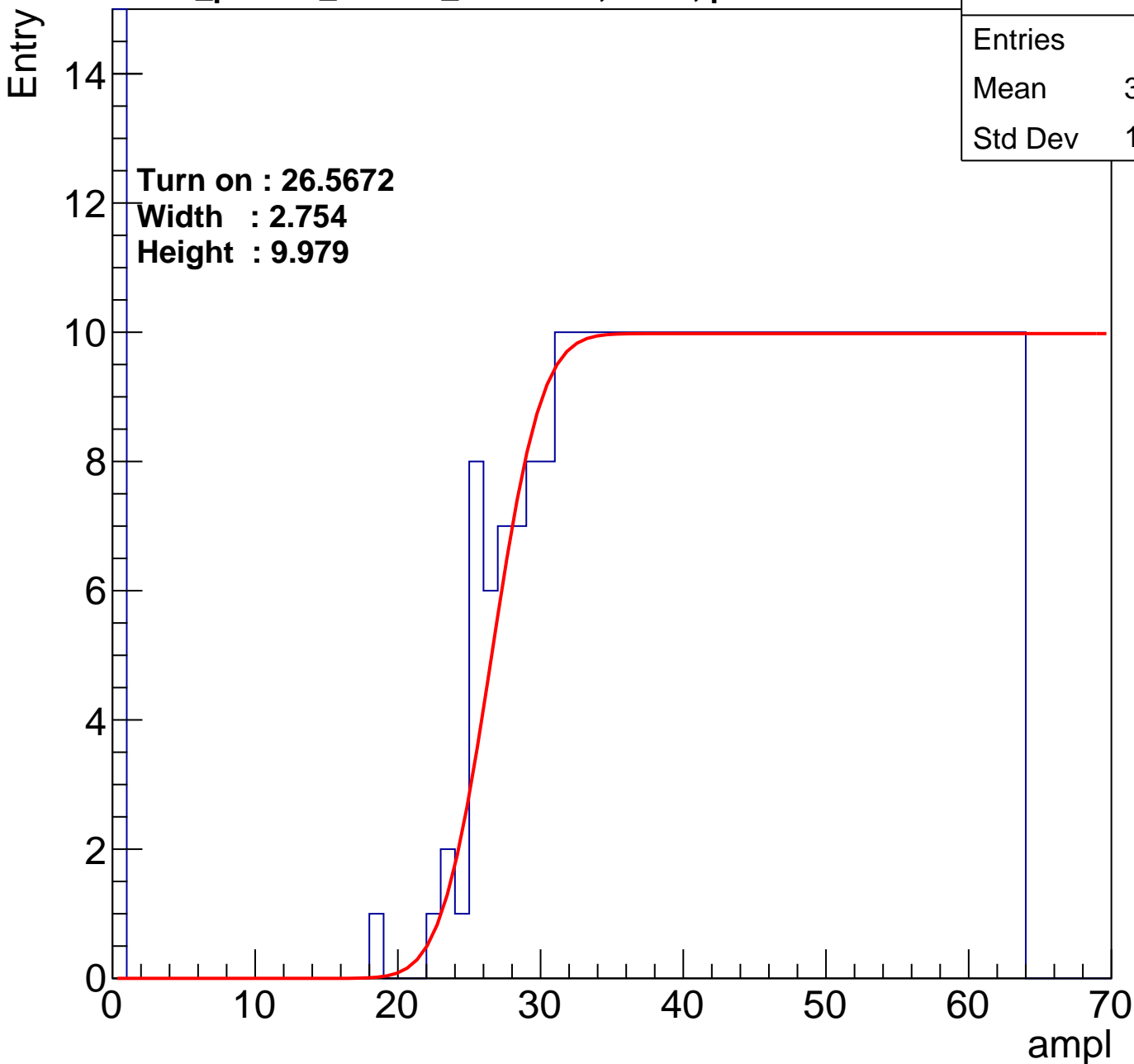
calib_packv5_041523_1651.root, FC#0, port C2

Entries	441
Mean	38.17
Std Dev	18.59

Turn on : 26.5672

Width : 2.754

Height : 9.979



B1L103S, U2-ch116

calib_packv5_041523_1651.root, FC#0, port C2

Entries	451
Mean	38.39
Std Dev	17.77

Turn on : 24.3093

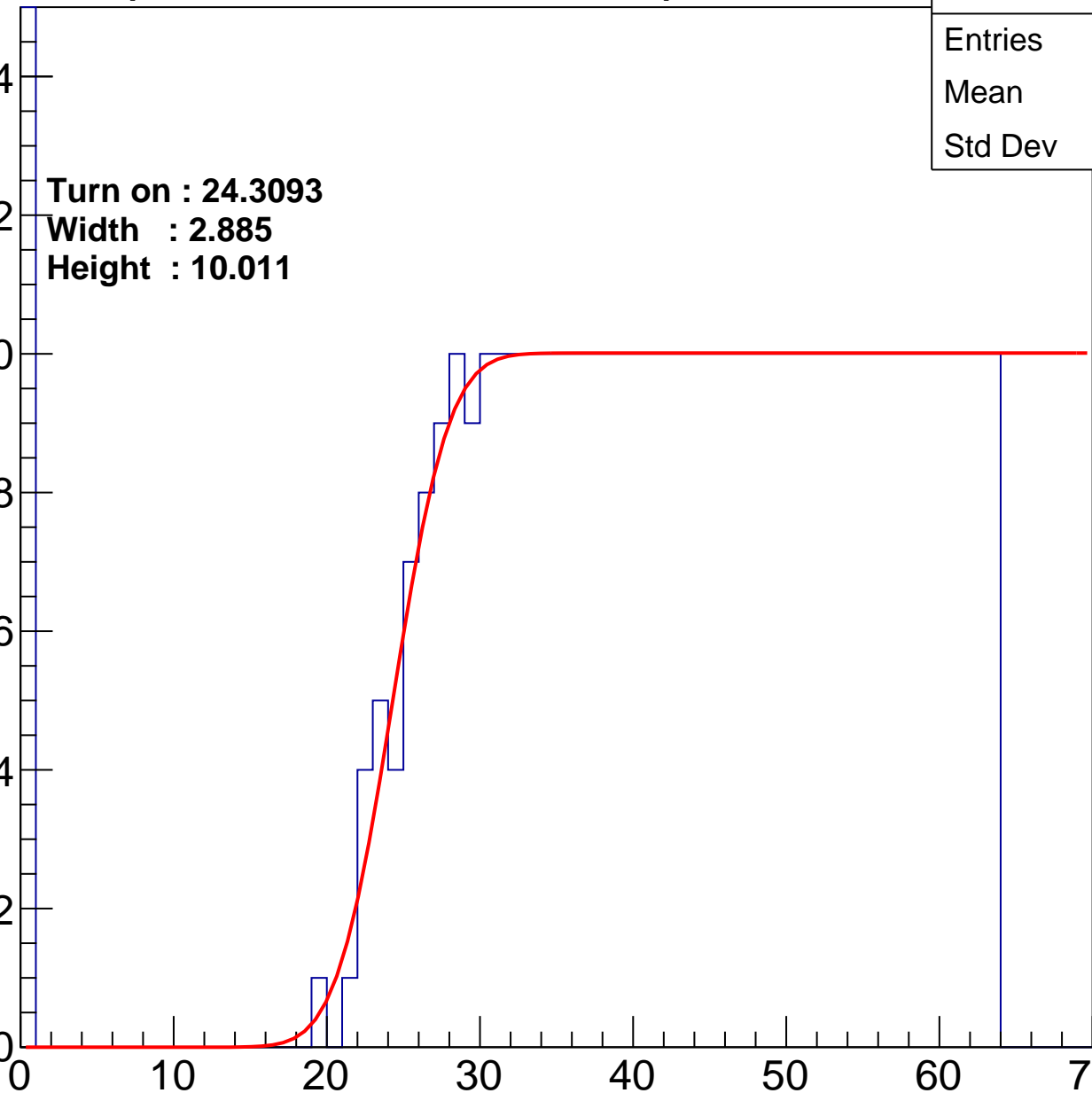
Width : 2.885

Height : 10.011

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch117

calib_packv5_041523_1651.root, FC#0, port C2

Entries	458
Mean	37.98
Std Dev	17.99

Turn on : 23.6028

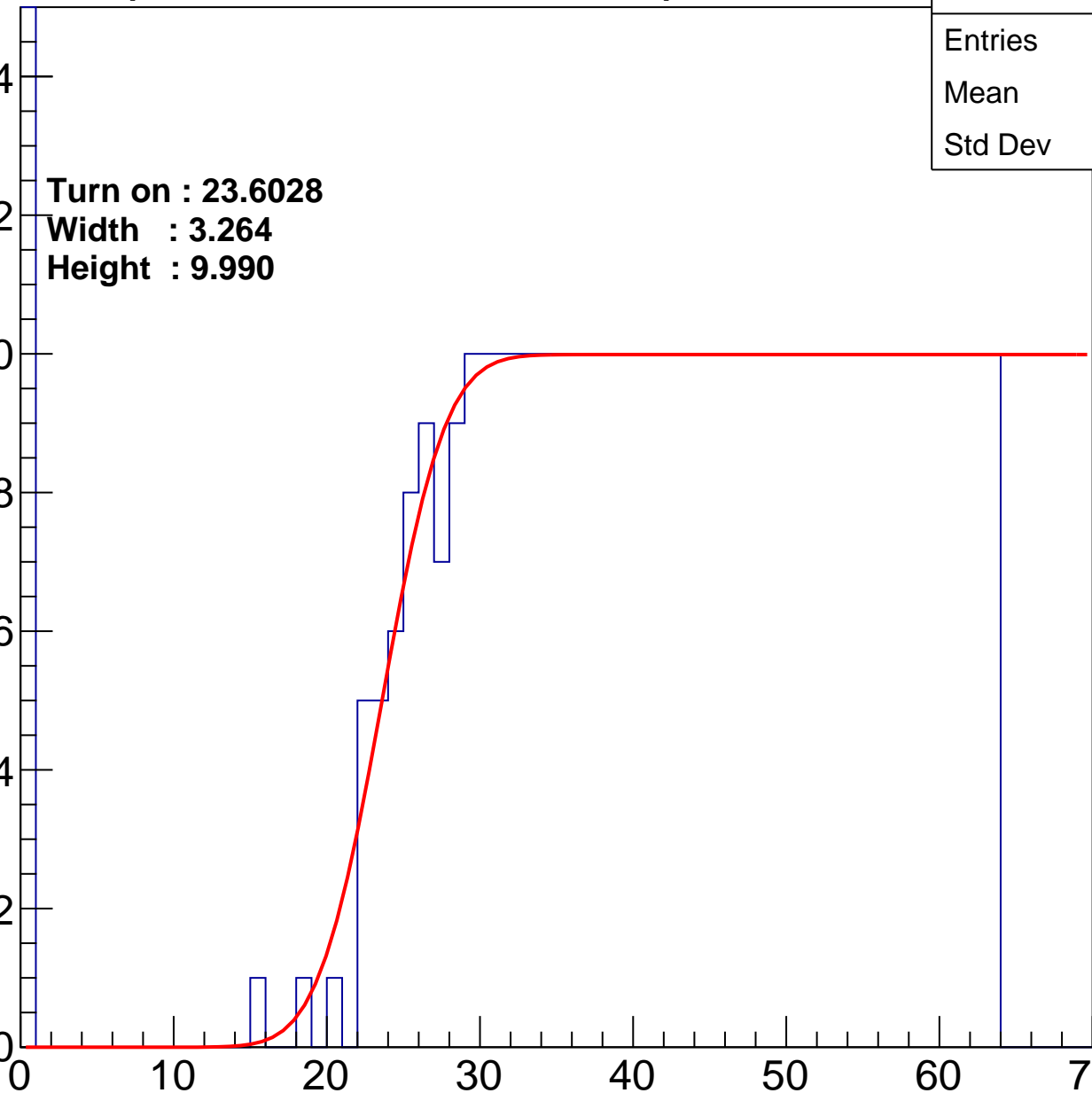
Width : 3.264

Height : 9.990

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch118

calib_packv5_041523_1651.root, FC#0, port C2

Entries	460
Mean	37.52
Std Dev	18.55

Turn on : 25.1725

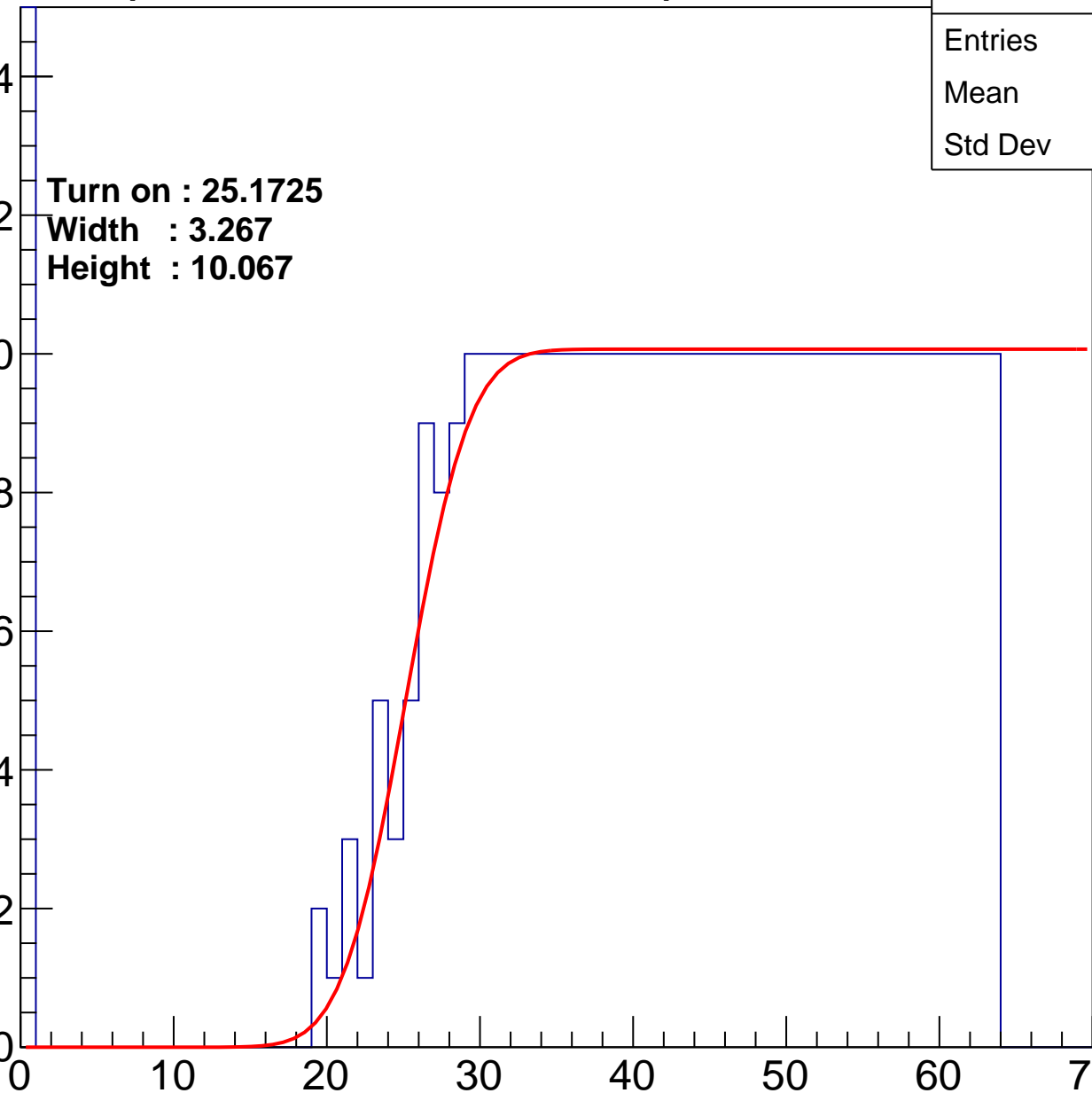
Width : 3.267

Height : 10.067

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch119

calib_packv5_041523_1651.root, FC#0, port C2

Entries	443
Mean	37.7
Std Dev	19.11

Turn on : 26.6926

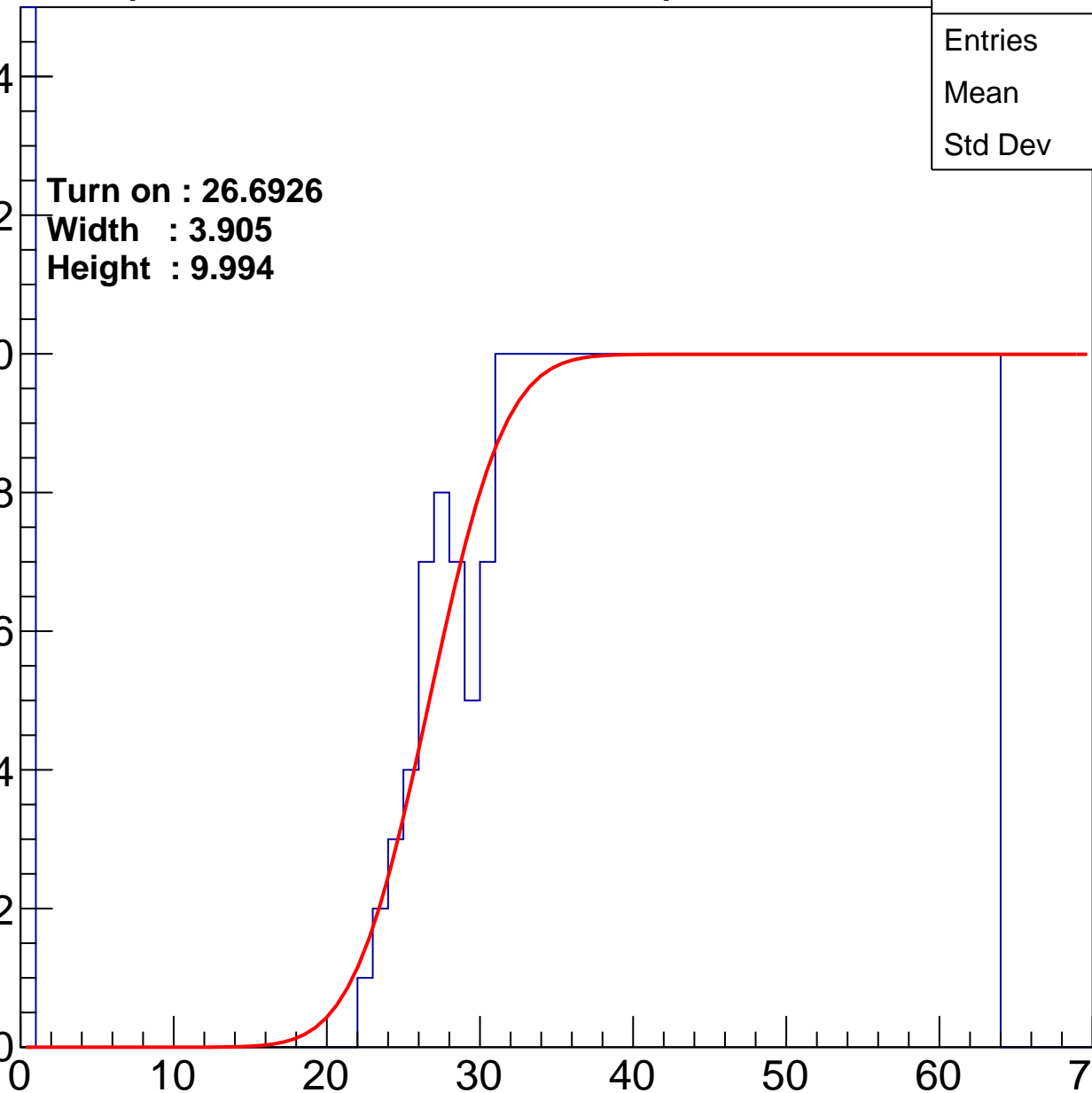
Width : 3.905

Height : 9.994

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch120

calib_packv5_041523_1651.root, FC#0, port C2

Entries	461
Mean	37.68
Std Dev	18.27

Turn on : 24.2472

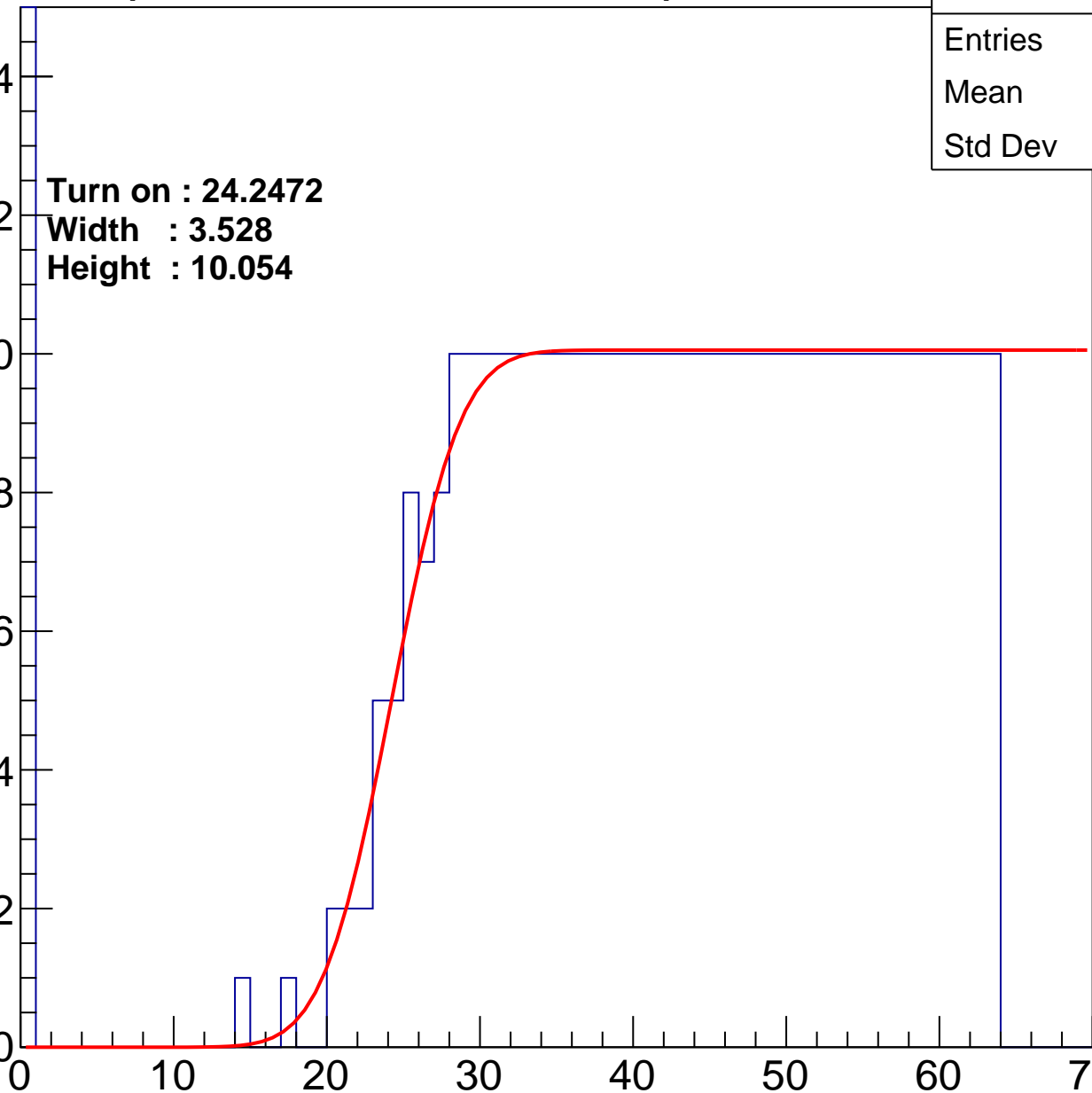
Width : 3.528

Height : 10.054

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch121

calib_packv5_041523_1651.root, FC#0, port C2

Entries	434
Mean	39.07
Std Dev	17.68

Turn on : 25.8059

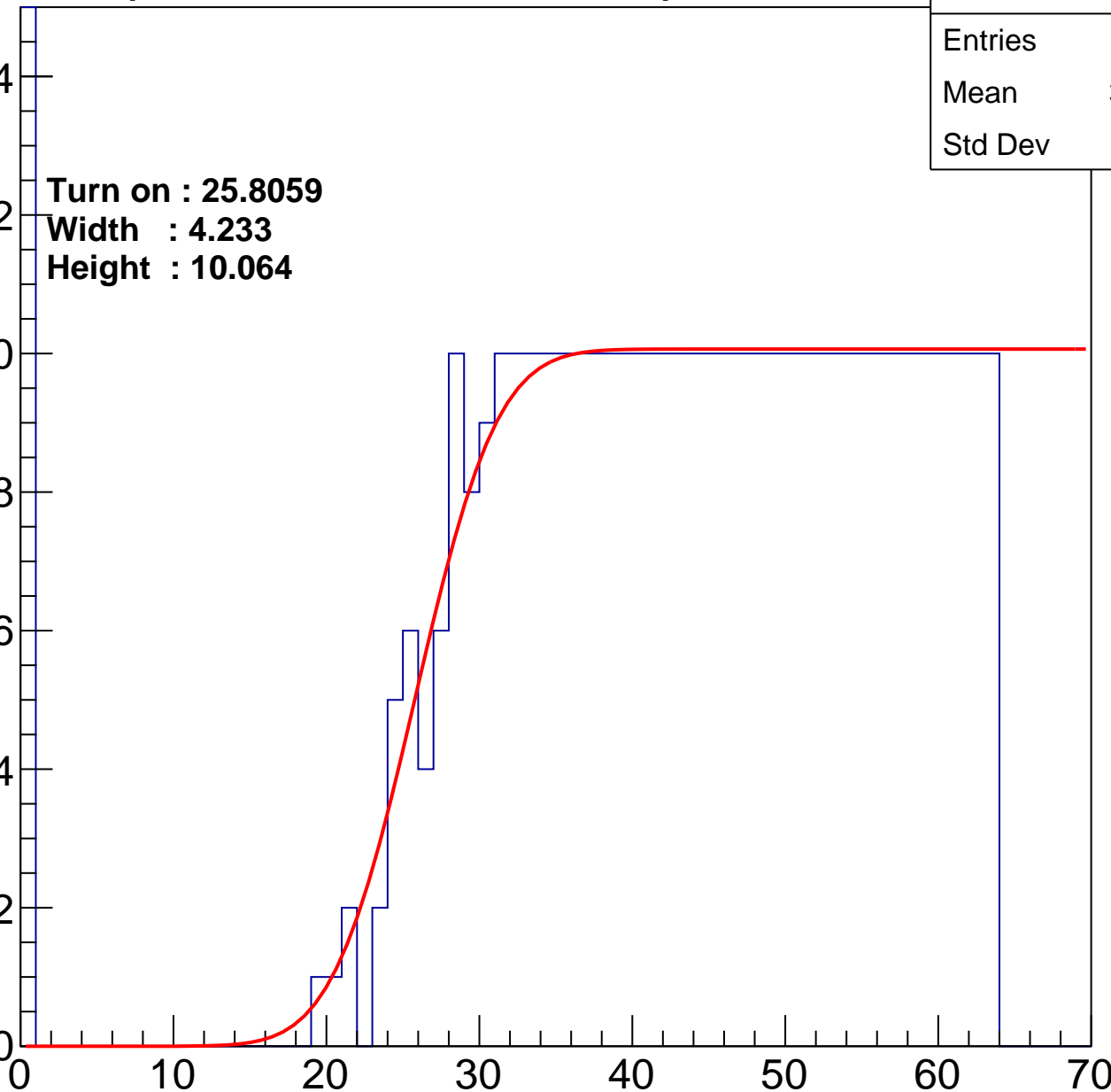
Width : 4.233

Height : 10.064

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch122

calib_packv5_041523_1651.root, FC#0, port C2

Entries	434
Mean	39.18
Std Dev	17.57

Turn on : 25.9220

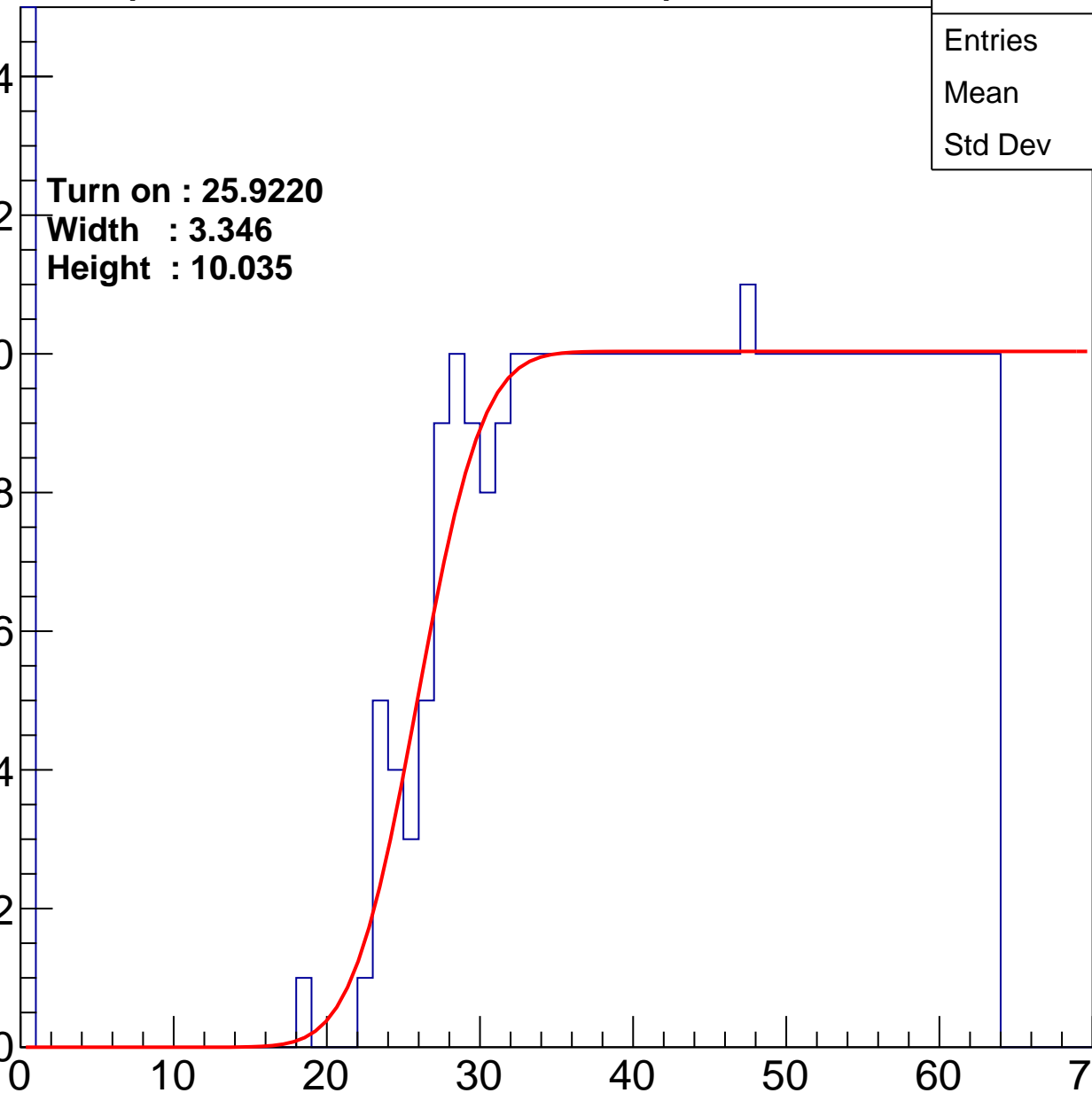
Width : 3.346

Height : 10.035

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch123

calib_packv5_041523_1651.root, FC#0, port C2

Entries	468
Mean	36.94
Std Dev	18.94

Turn on : 24.5592

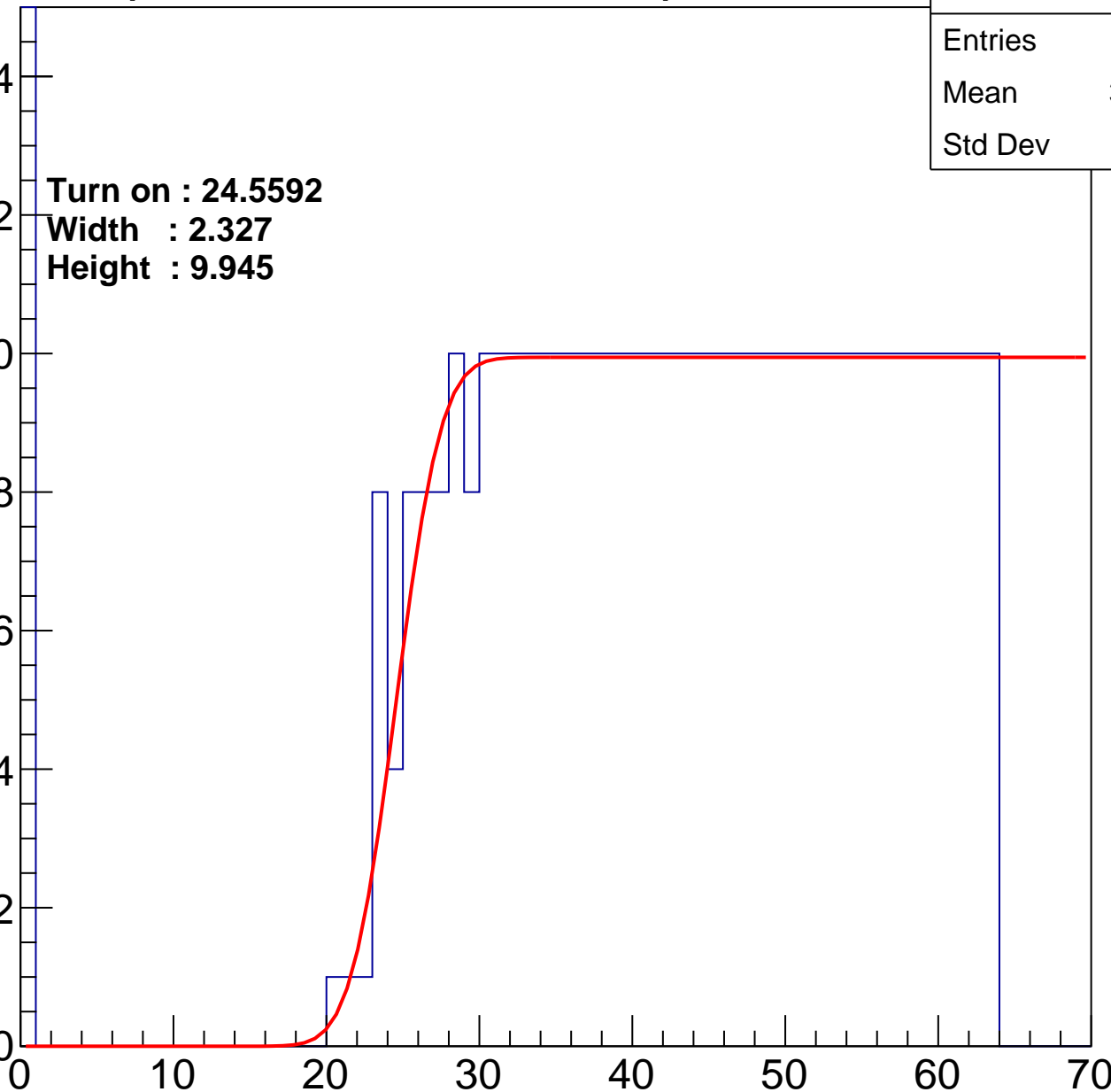
Width : 2.327

Height : 9.945

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch124

calib_packv5_041523_1651.root, FC#0, port C2

Entries	485
Mean	36.55
Std Dev	18.64

Turn on : 22.4794

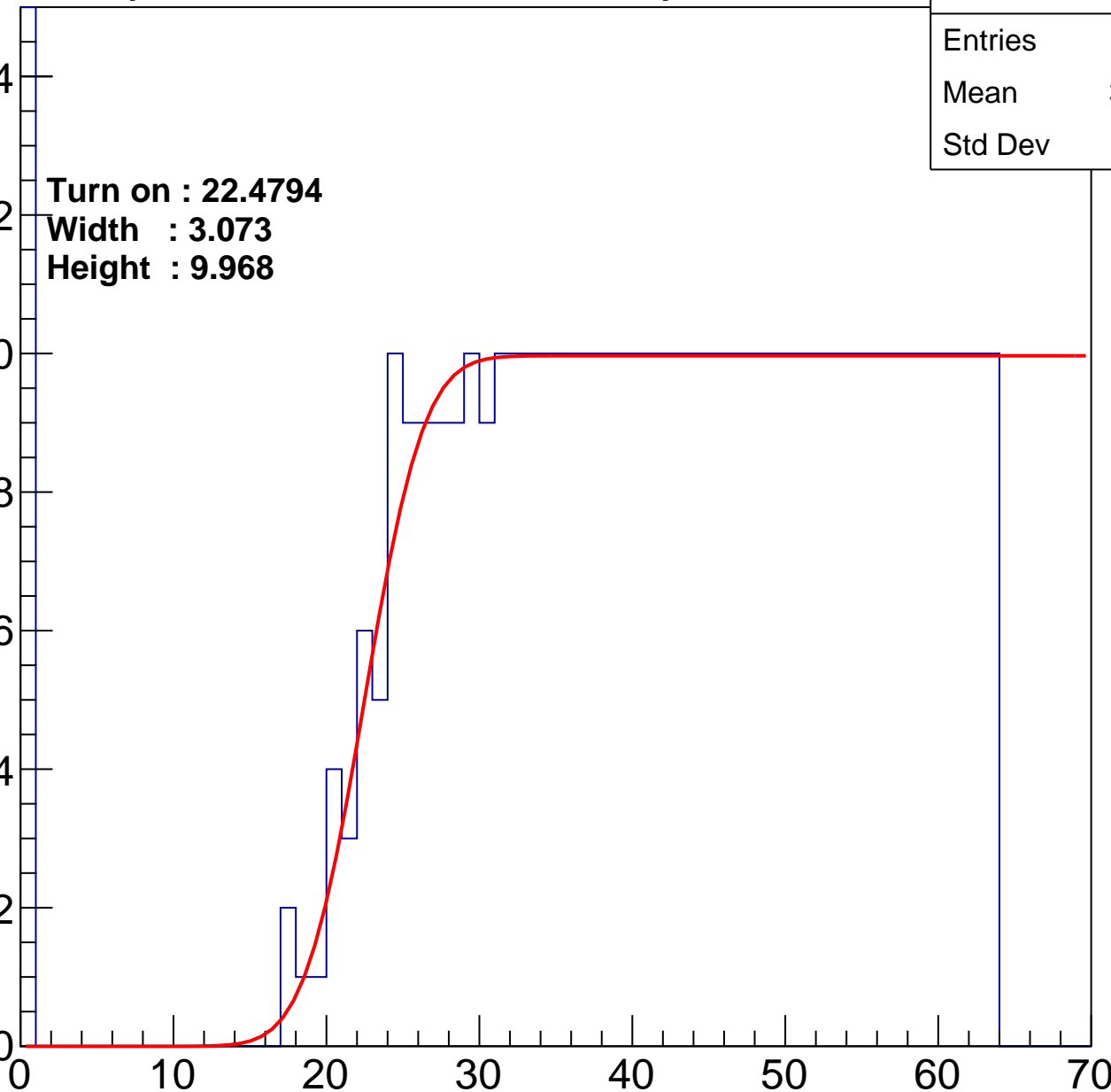
Width : 3.073

Height : 9.968

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch125

calib_packv5_041523_1651.root, FC#0, port C2

Entries	461
Mean	37.4
Std Dev	18.67

Turn on : 24.7888

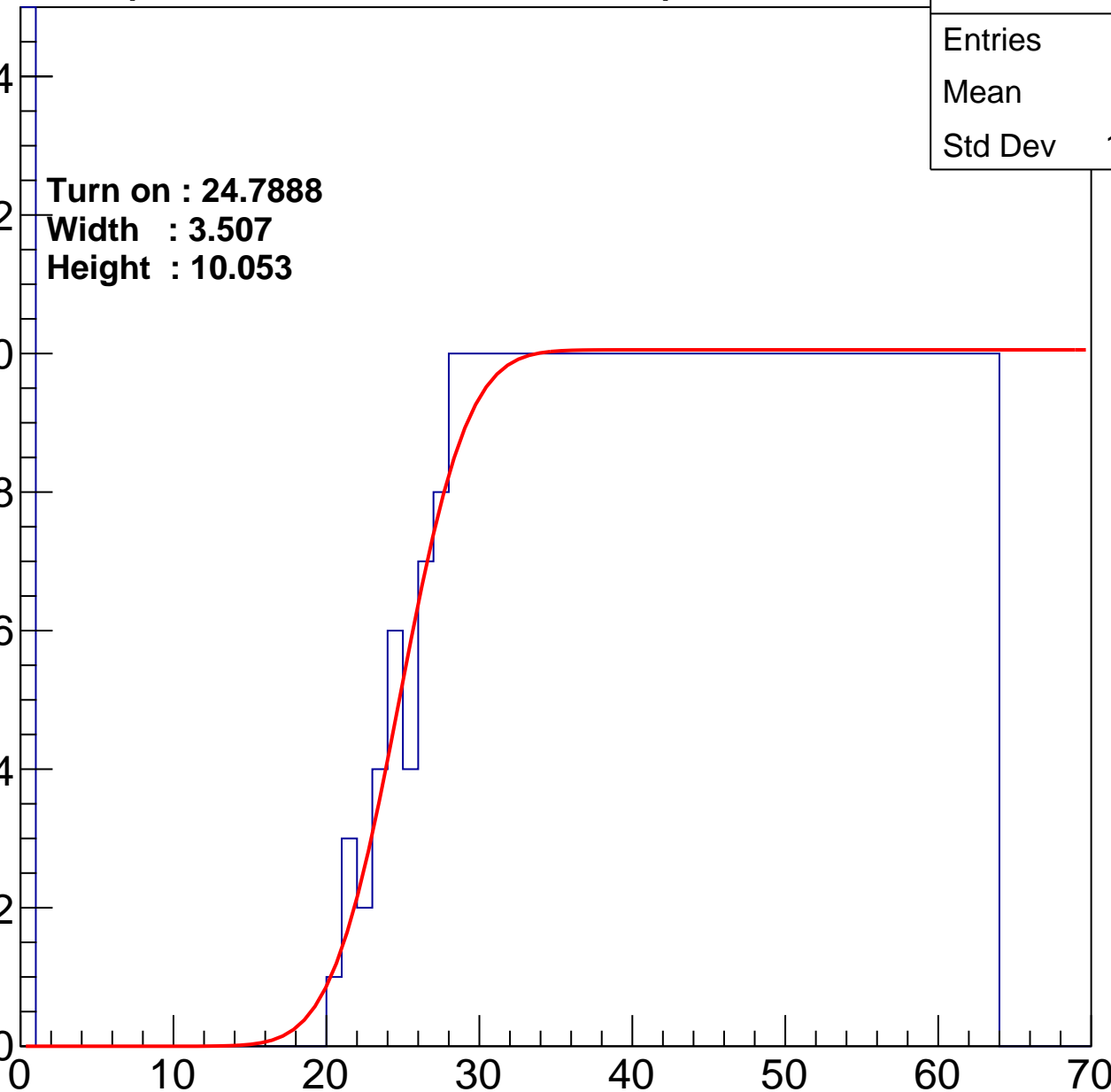
Width : 3.507

Height : 10.053

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch126

calib_packv5_041523_1651.root, FC#0, port C2

Entries	490
Mean	36.13
Std Dev	18.99

Turn on : 22.3776

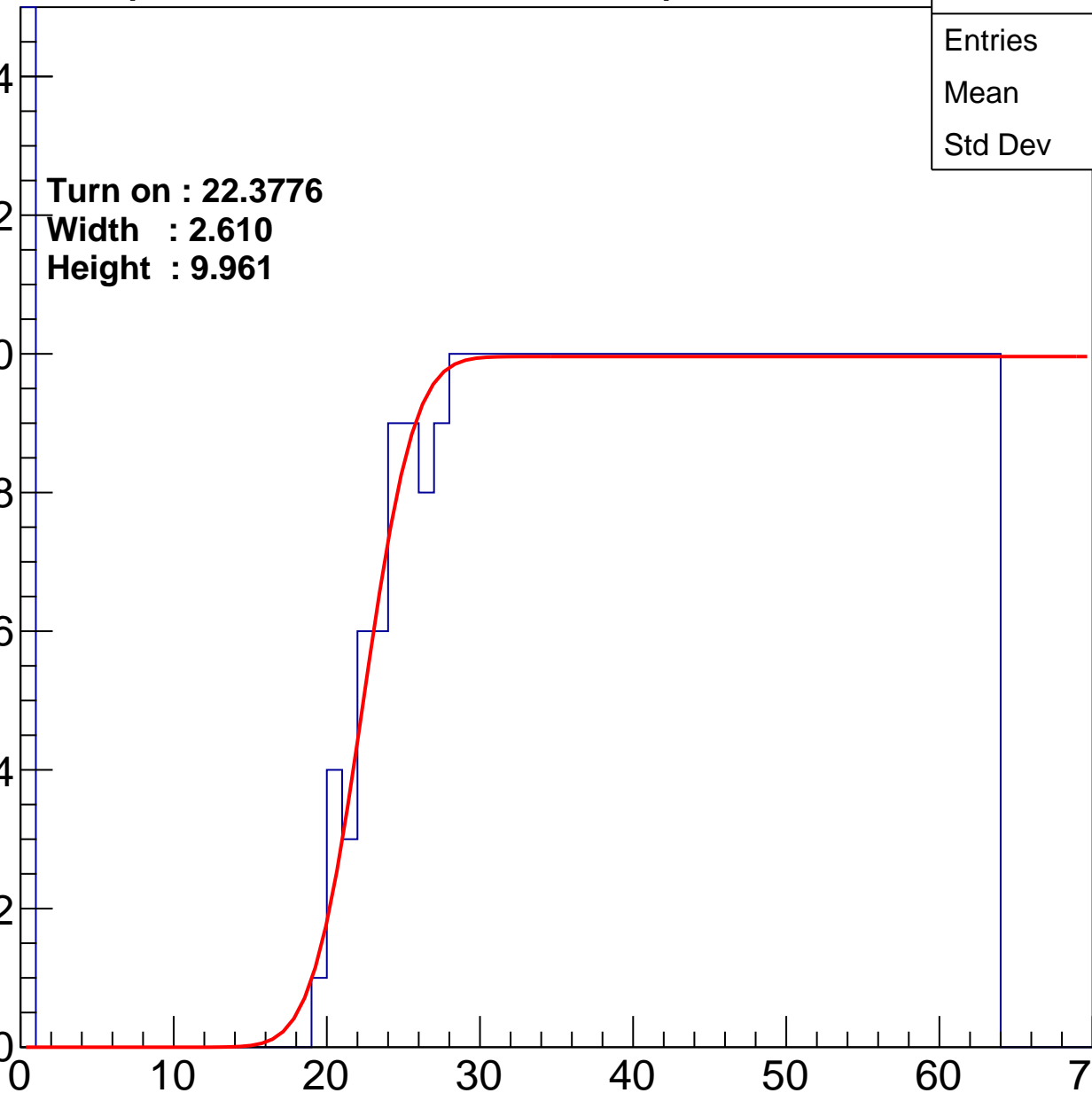
Width : 2.610

Height : 9.961

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch127

calib_packv5_041523_1651.root, FC#0, port C2

Entries	441
Mean	38.64
Std Dev	17.94

Turn on : 25.6158

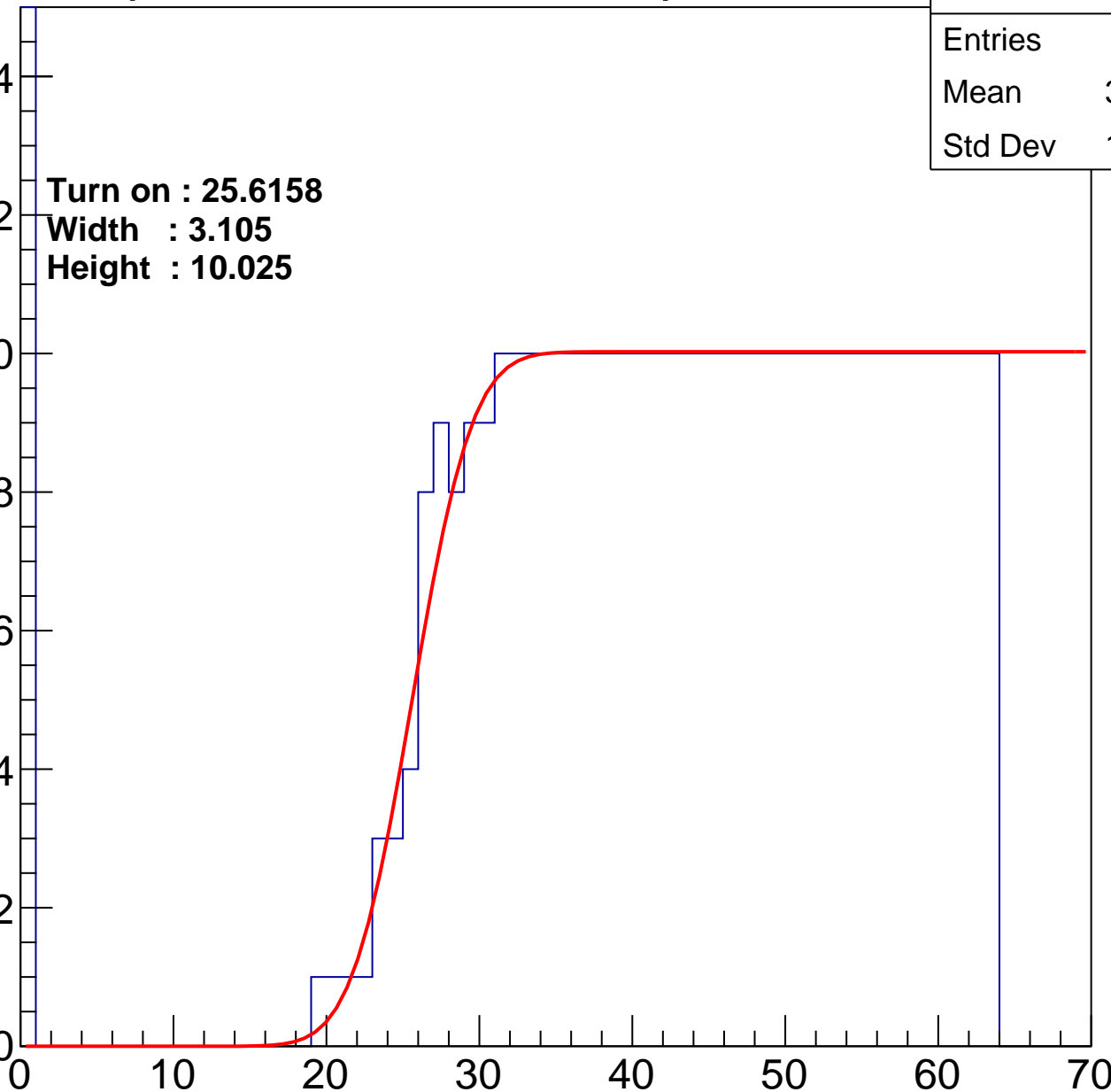
Width : 3.105

Height : 10.025

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch127

calib_packv5_041523_1651.root, FC#0, port C2

Entries	441
Mean	38.64
Std Dev	17.94

Turn on : 25.6158

Width : 3.105

Height : 10.025

Entry

14
12
10
8
6
4
2
0

ampl

