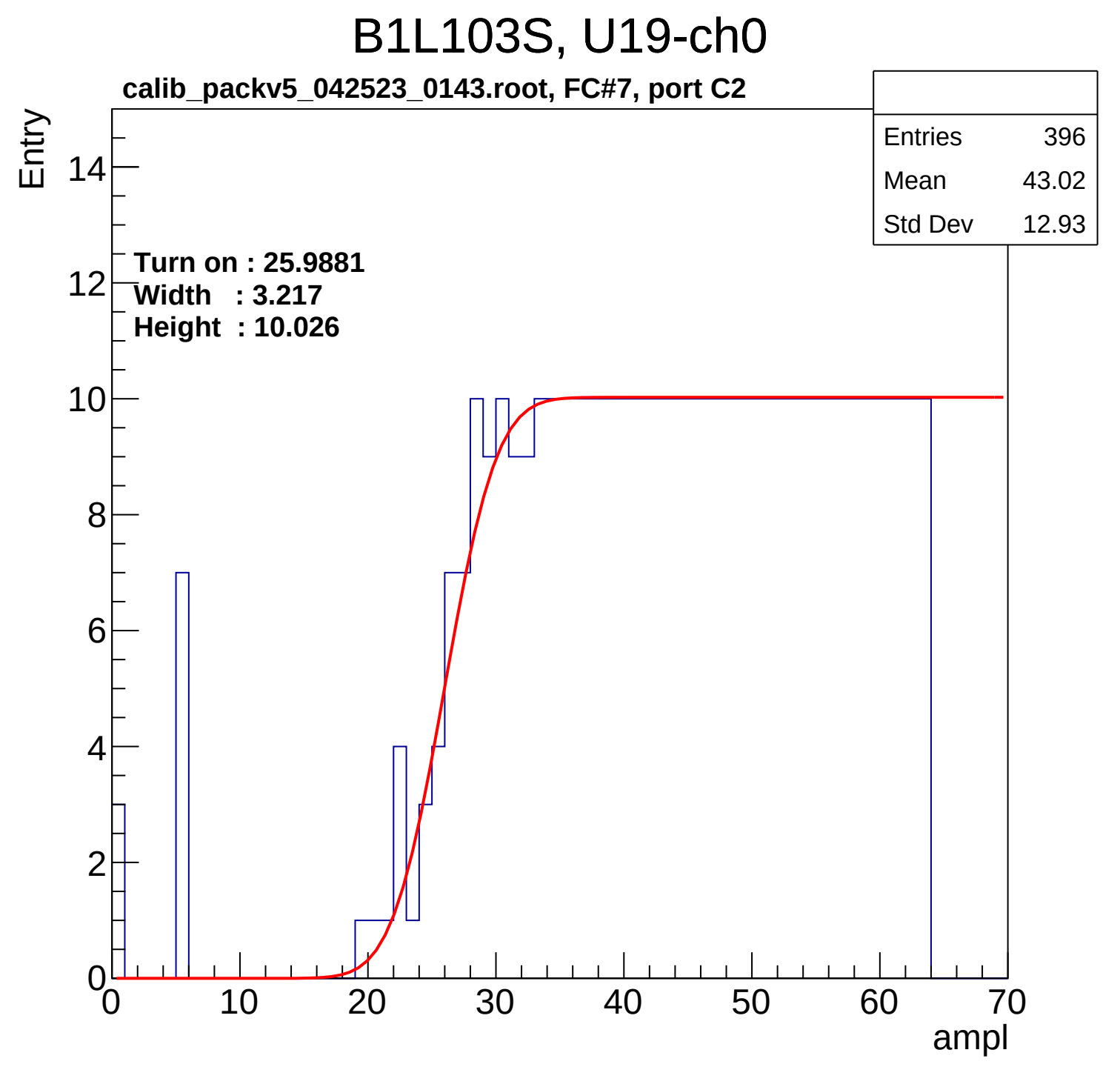
B1L103S, U19-ch0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 396
Mean 43.02
Std Dev 12.93
Turn on : 25.9881
Width : 3.217
Height : 10.026
Entry
ampl
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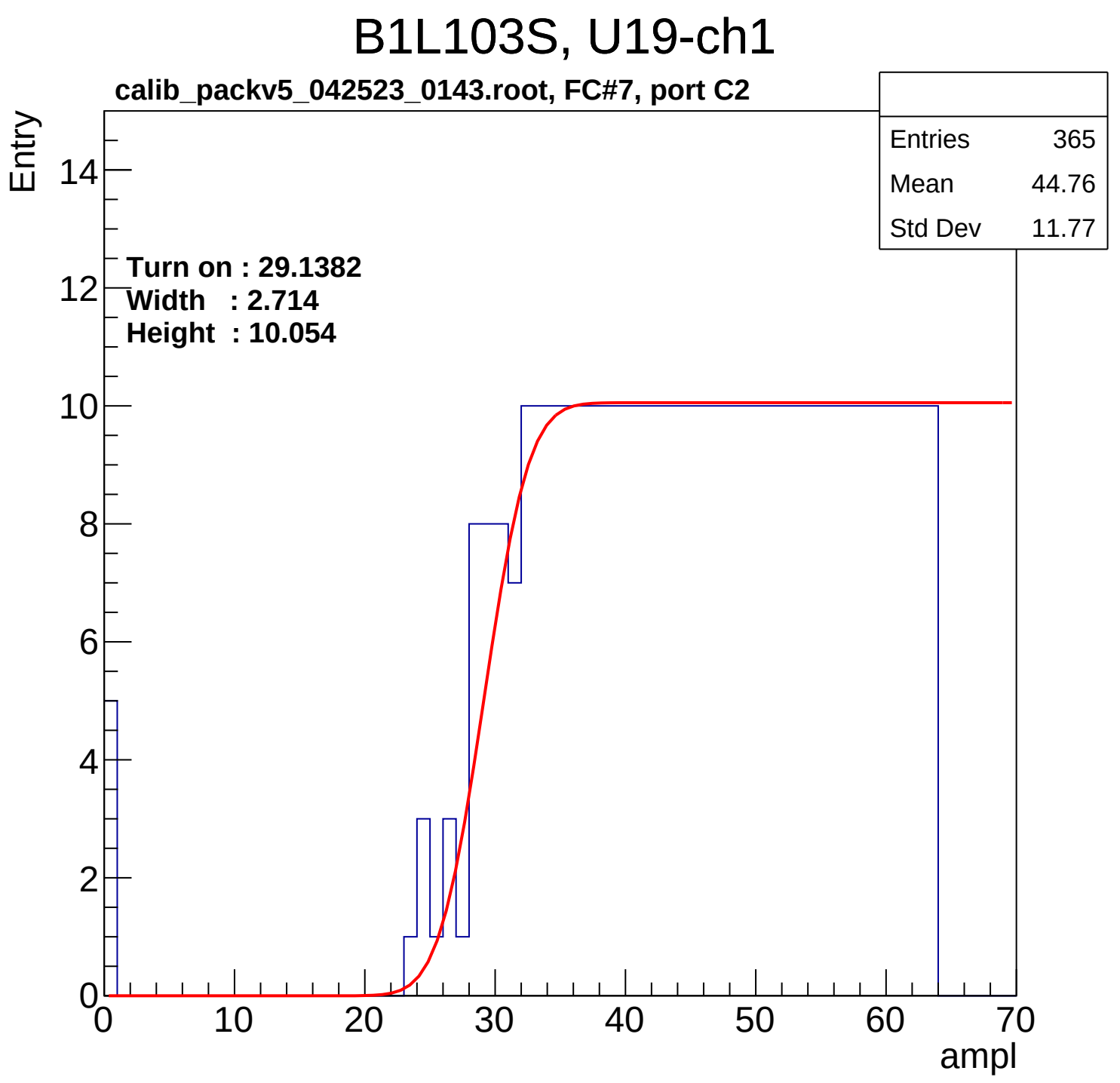
B1L103S, U19-ch1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 365
Mean 44.76
Std Dev 11.77
Turn on : 29.1382
Width : 2.714
Height : 10.054
Entry
ampl
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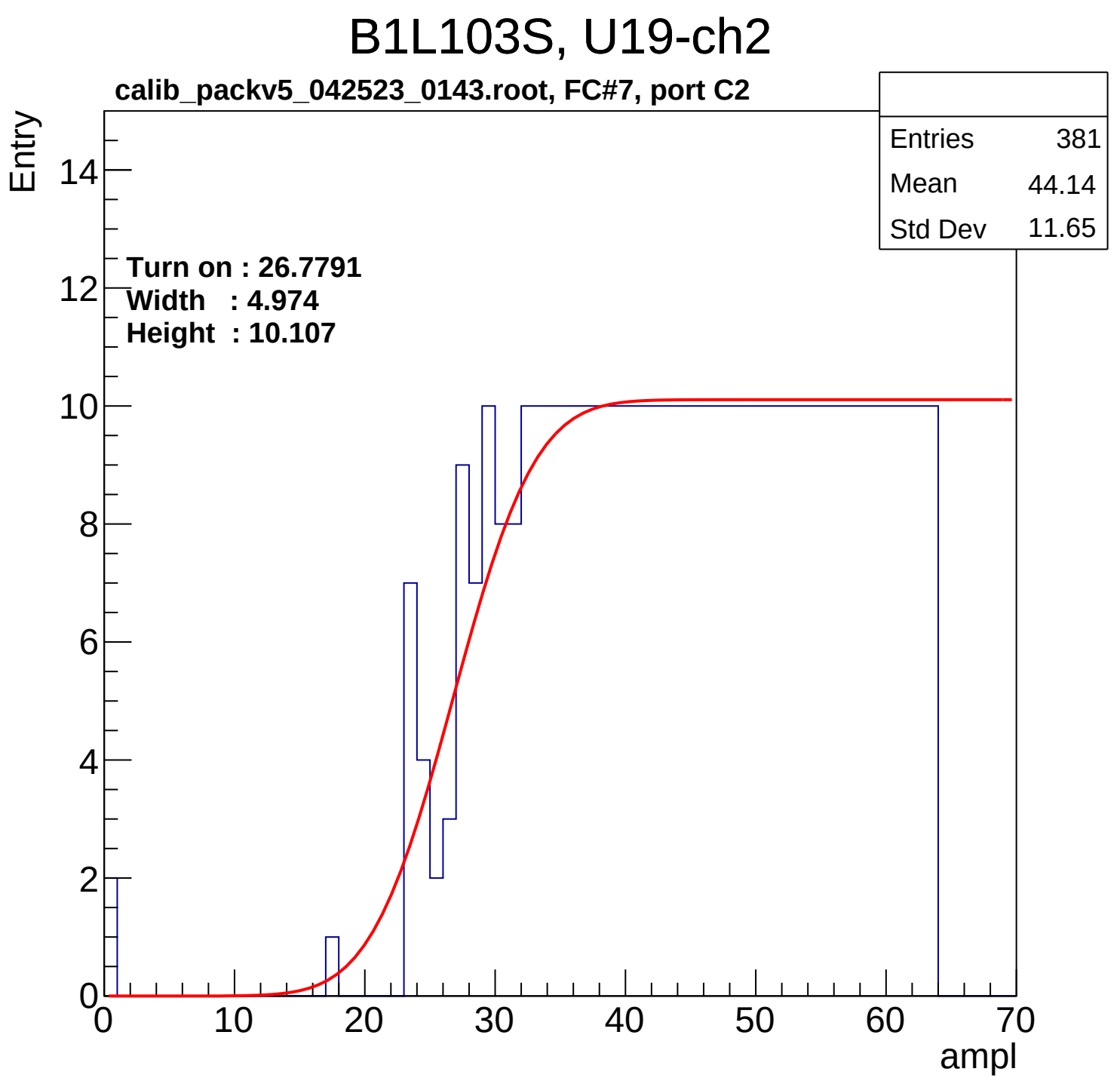
B1L103S, U19-ch2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 381
Mean 44.14
Std Dev 11.65
Turn on : 26.7791
Width : 4.974
Height : 10.107
Entry
ampl
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2
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6
8
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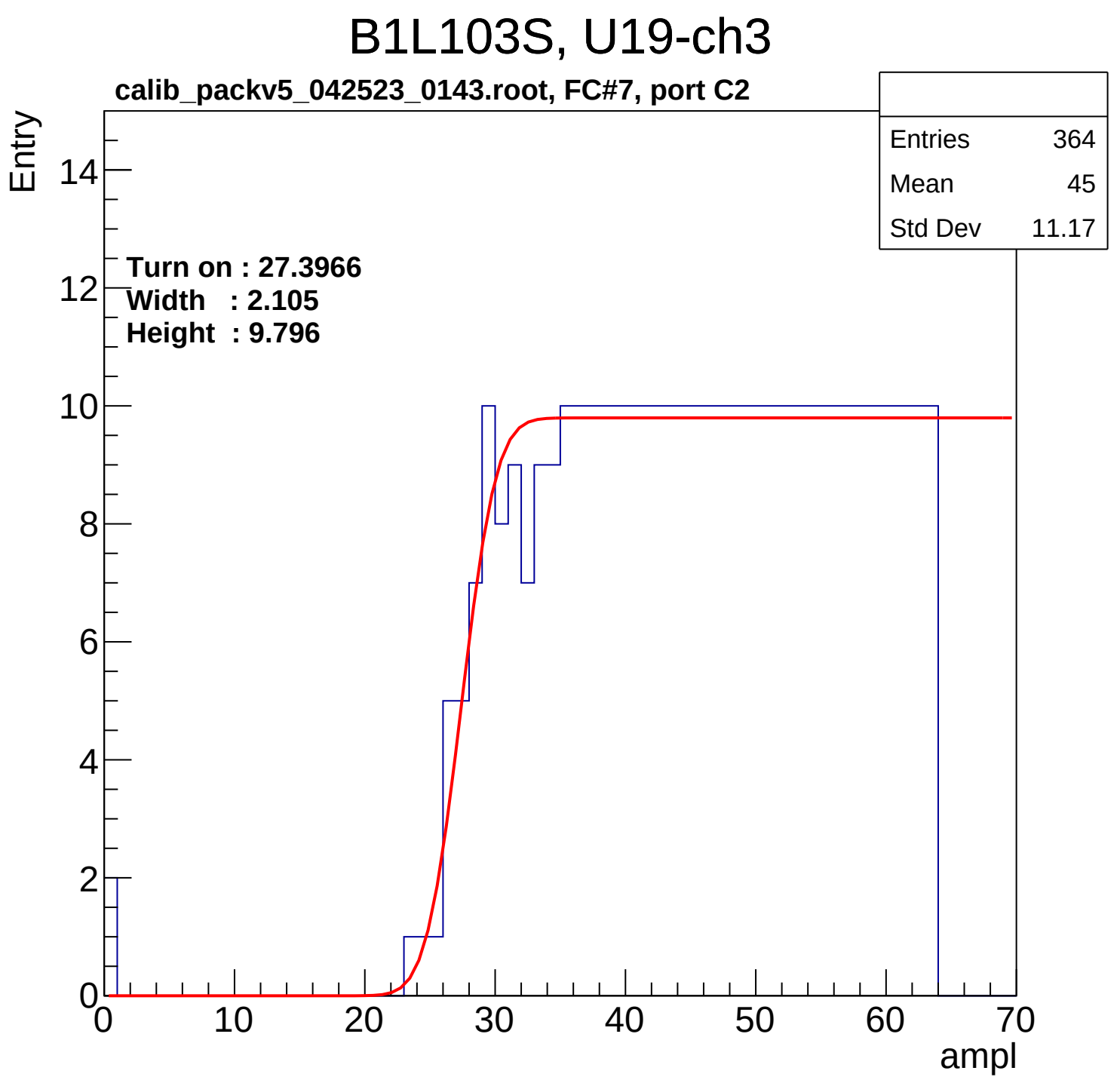
B1L103S, U19-ch3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 364
Mean 45
Std Dev 11.17
Turn on : 27.3966
Width : 2.105
Height : 9.796
Entry
ampl
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2
4
6
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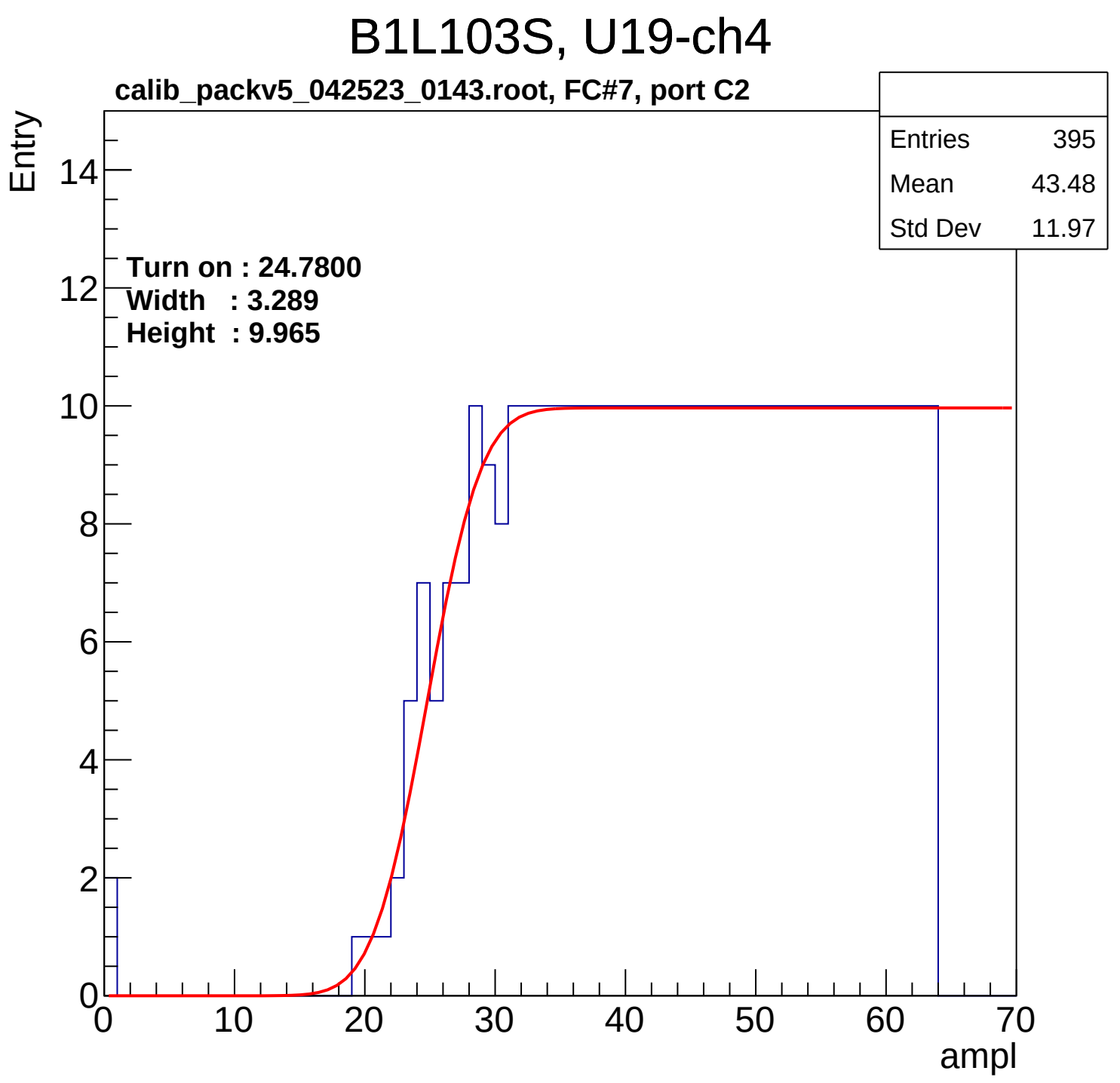
B1L103S, U19-ch4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 395
Mean 43.48
Std Dev 11.97
Turn on : 24.7800
Width : 3.289
Height : 9.965
Entry
ampl
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6
8
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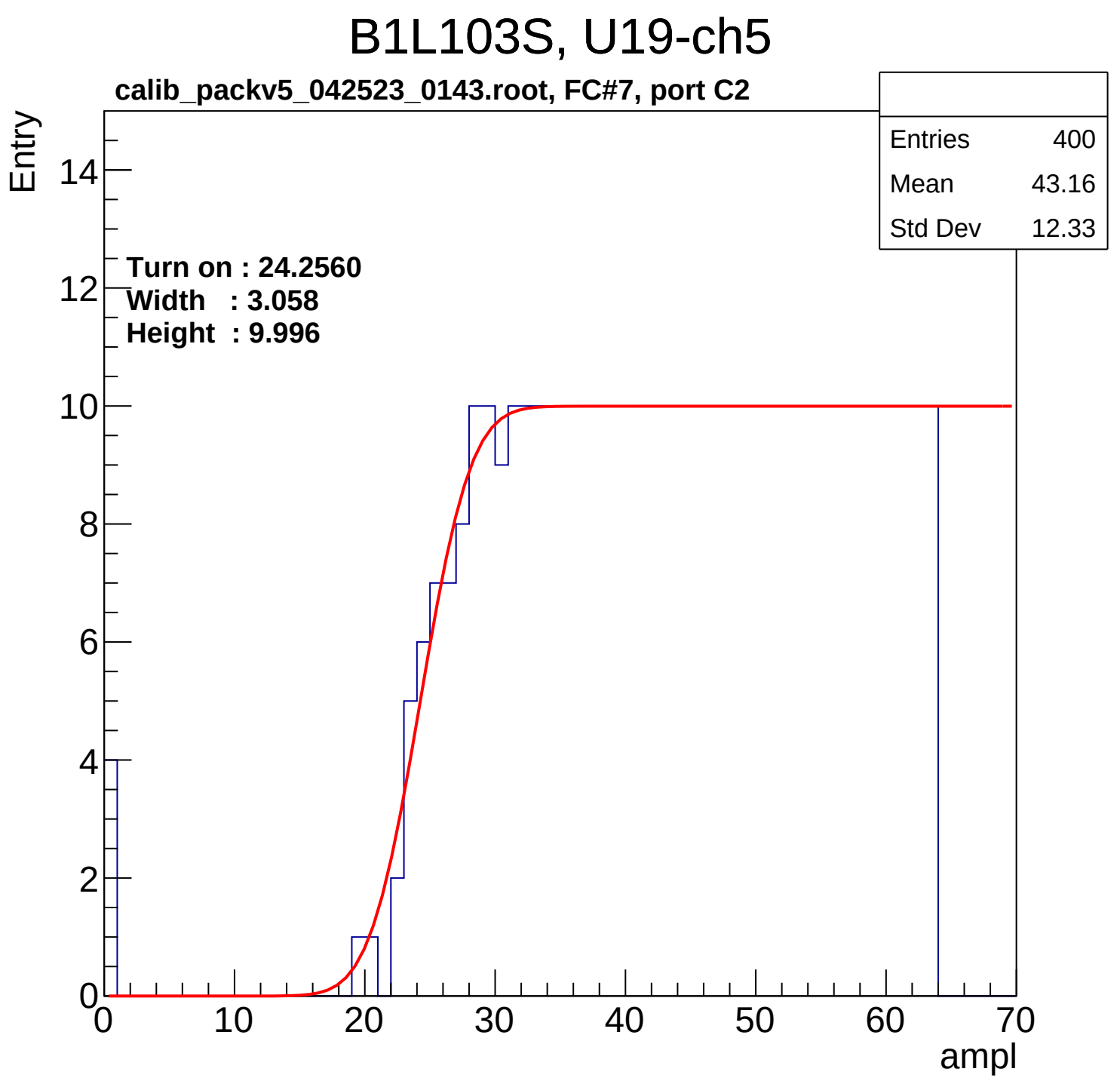
B1L103S, U19-ch5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 400
Mean 43.16
Std Dev 12.33
Turn on : 24.2560
Width : 3.058
Height : 9.996
Entry
ampl
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2
4
6
8
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0
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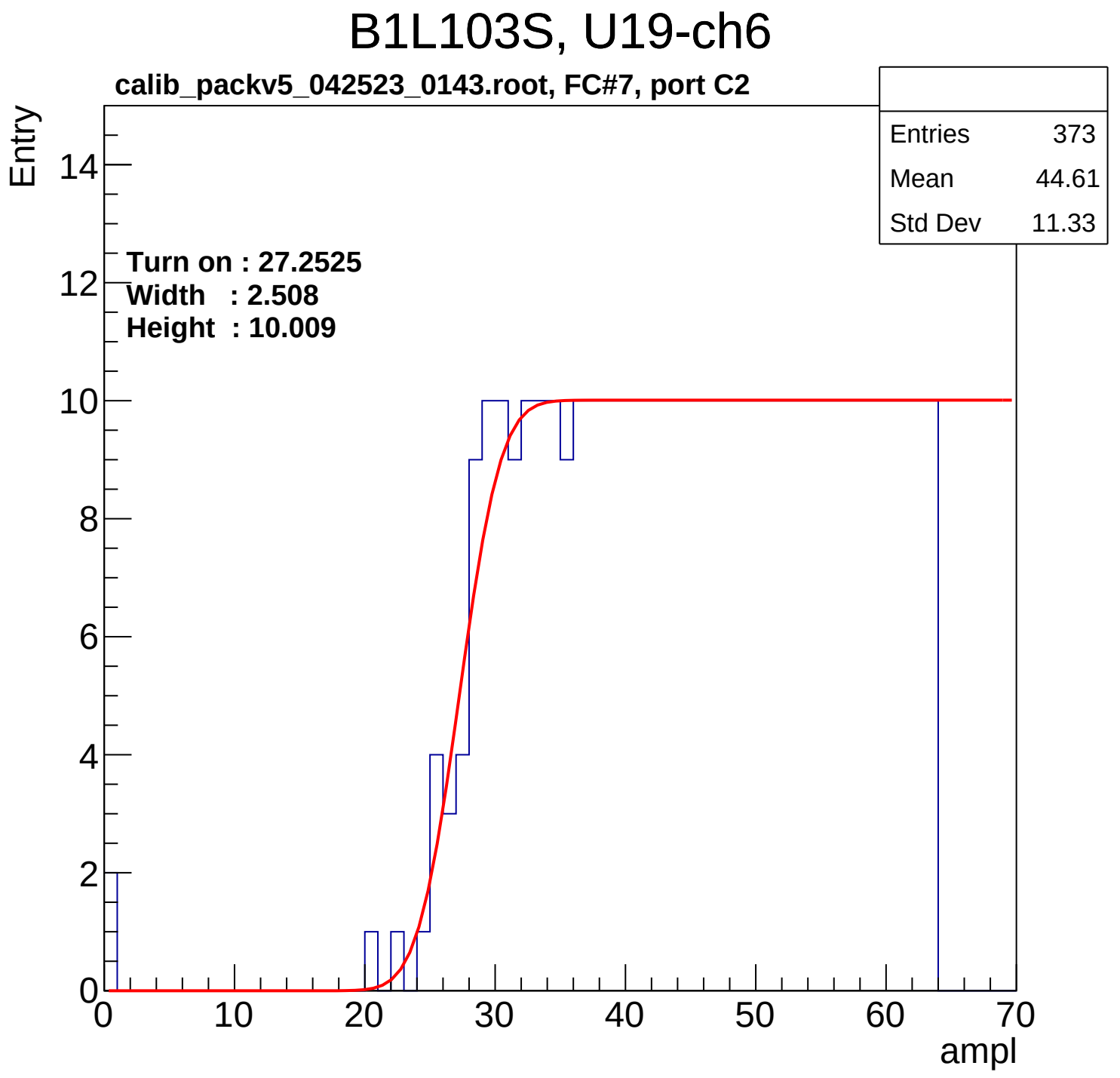
B1L103S, U19-ch6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 373
Mean 44.61
Std Dev 11.33
Turn on : 27.2525
Width : 2.508
Height : 10.009
Entry
ampl
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2
4
6
8
10
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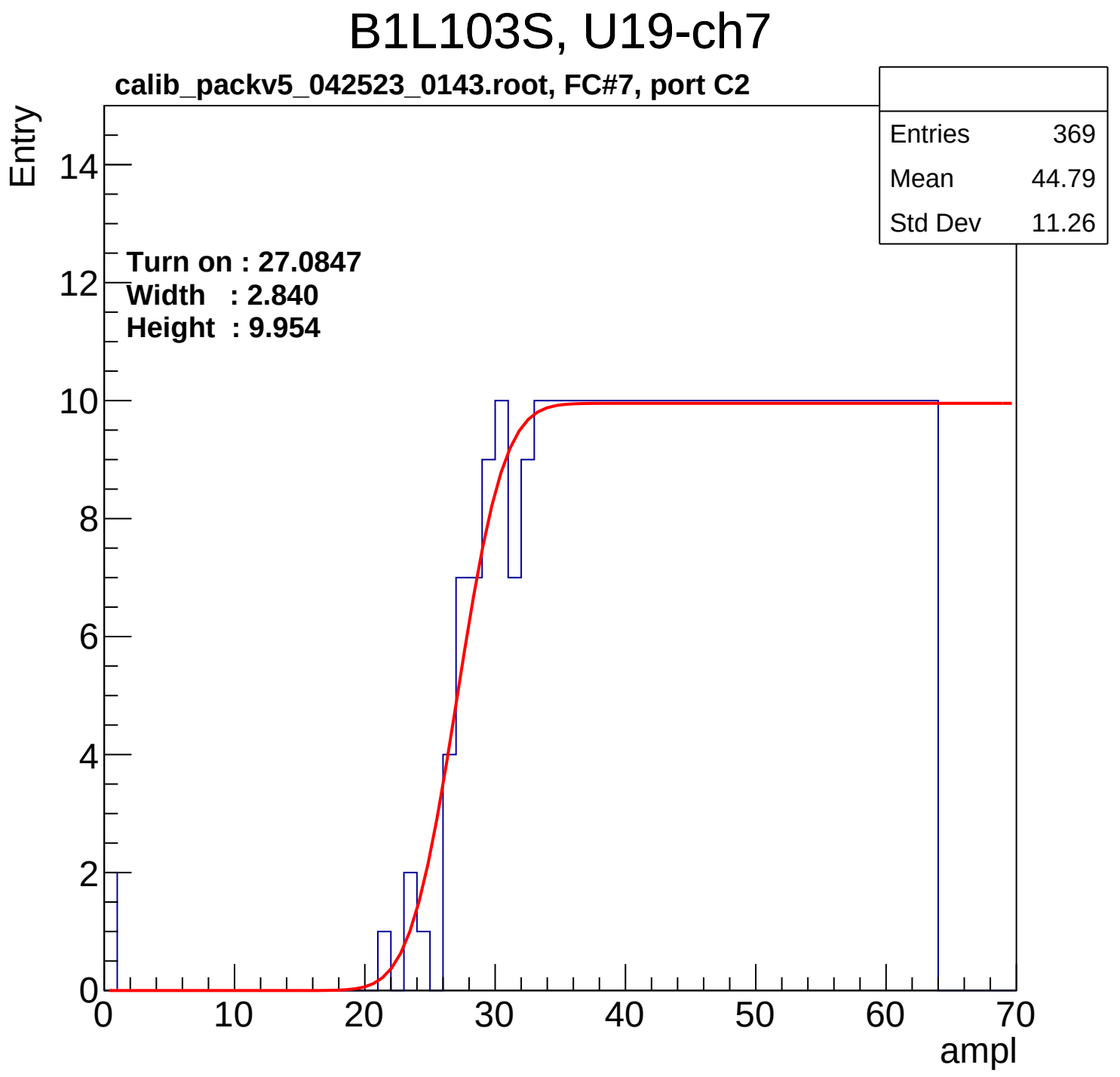
B1L103S, U19-ch7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 369
Mean 44.79
Std Dev 11.26
Turn on : 27.0847
Width : 2.840
Height : 9.954
Entry
ampl
0
2
4
6
8
10
12
14
0
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60
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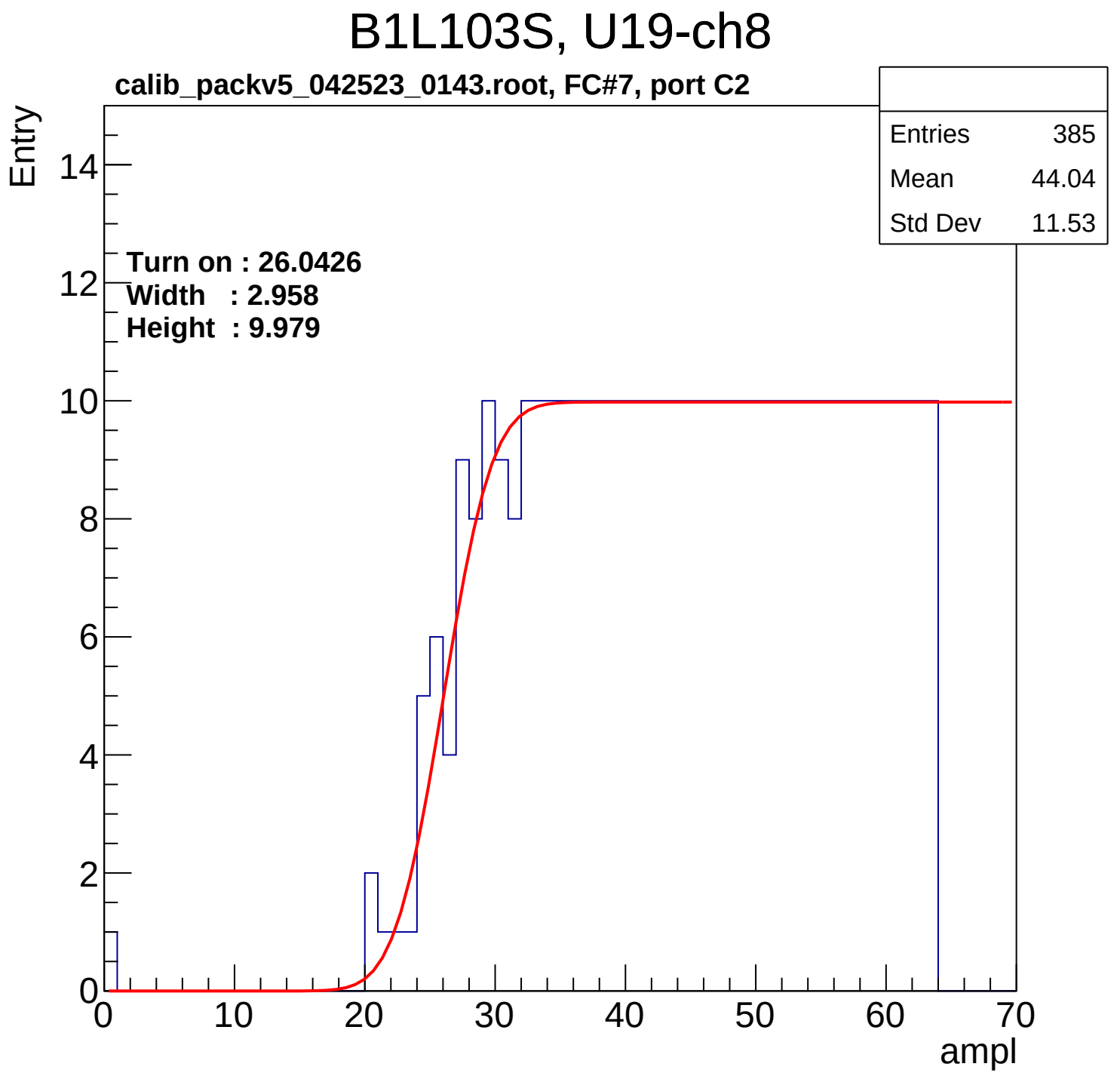
B1L103S, U19-ch8
calib_packv5_042523_0143.root, FC#7, port C2
Entries 385
Mean 44.04
Std Dev 11.53
Turn on : 26.0426
Width : 2.958
Height : 9.979
Entry
ampl
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2
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8
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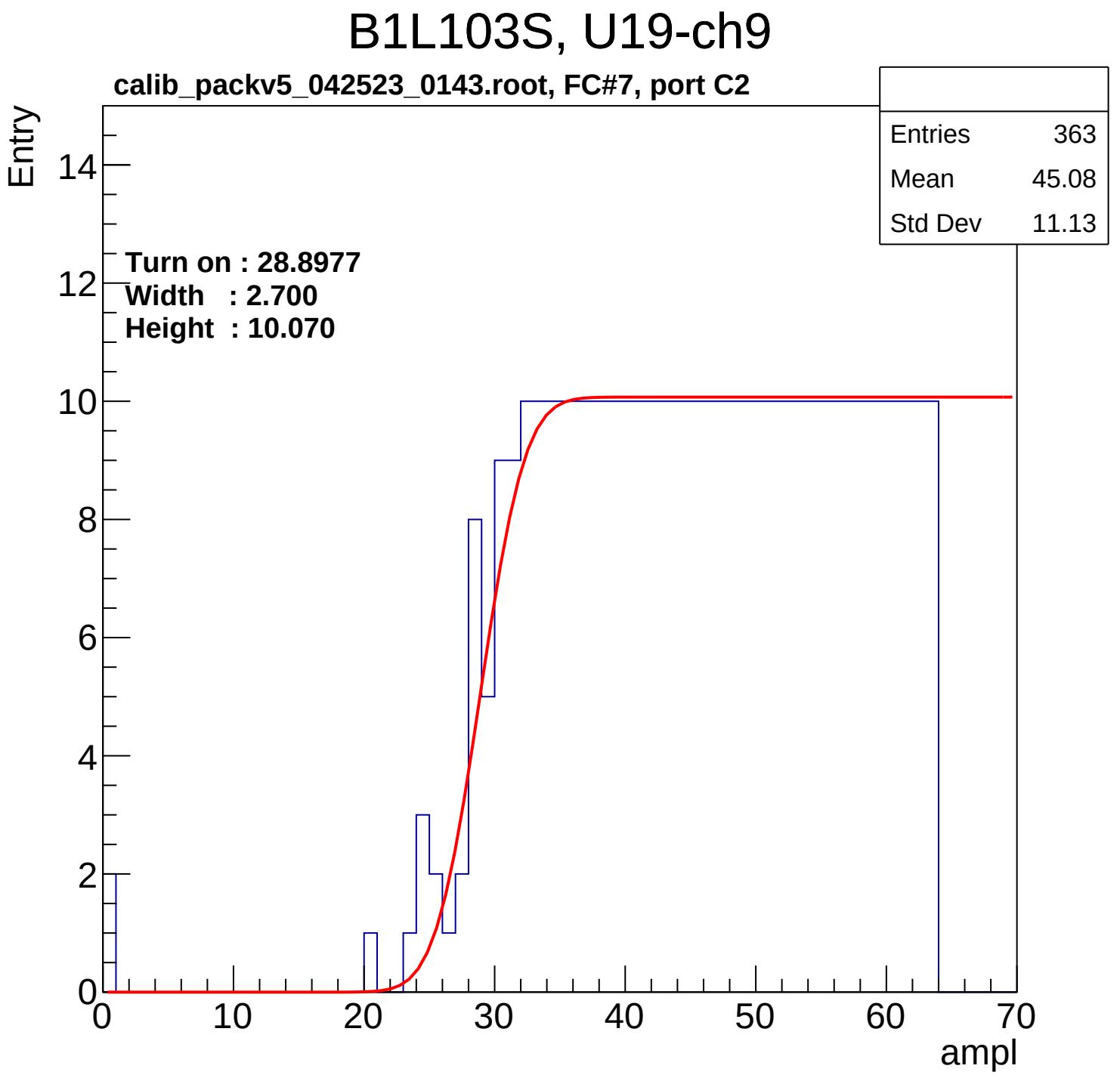
B1L103S, U19-ch9
calib_packv5_042523_0143.root, FC#7, port C2
Entries 363
Mean 45.08
Std Dev 11.13
Turn on : 28.8977
Width : 2.700
Height : 10.070
Entry
ampl
0
2
4
6
8
10
12
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0
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20
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60
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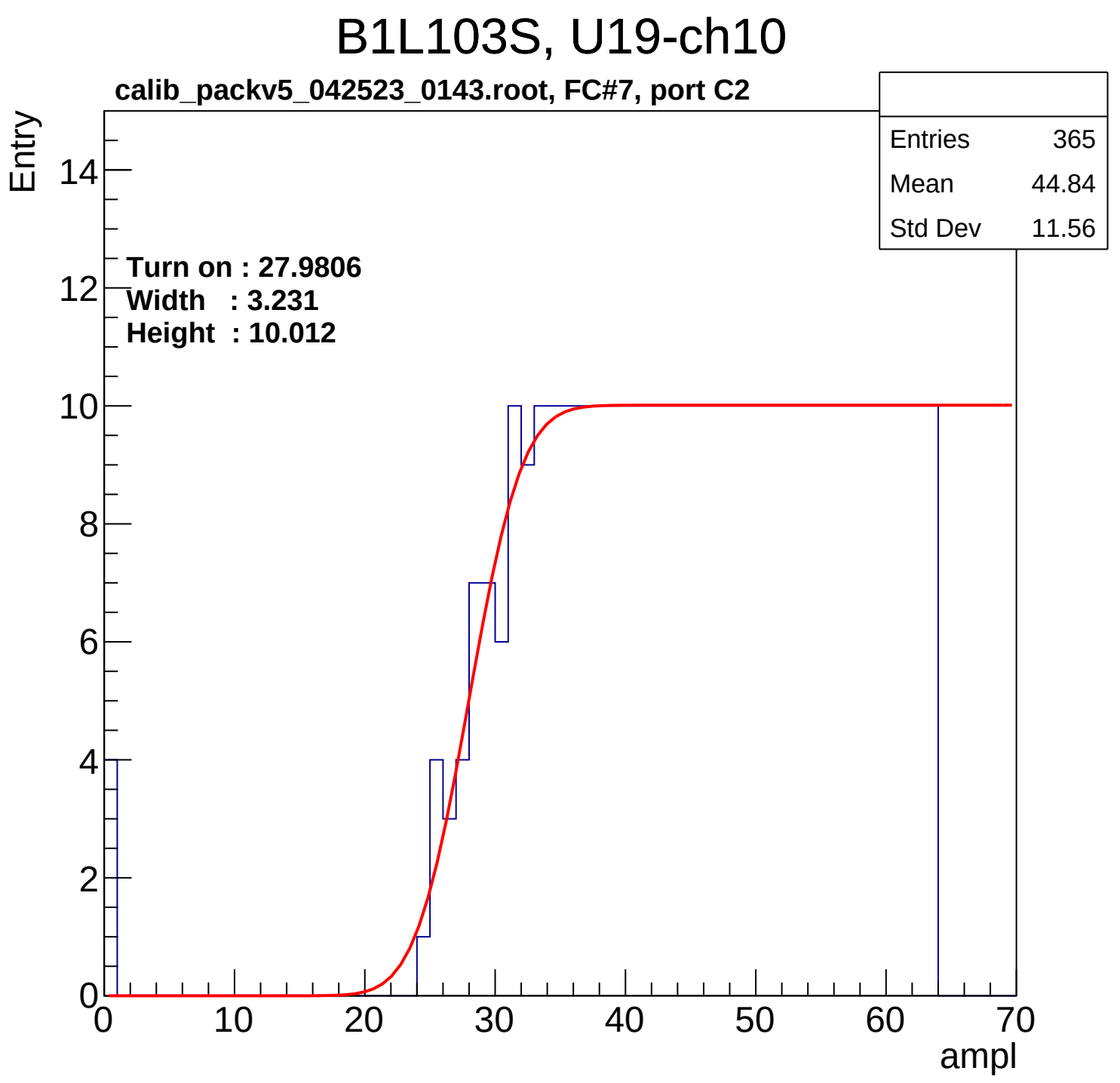
B1L103S, U19-ch10
calib_packv5_042523_0143.root, FC#7, port C2
Entries 365
Mean 44.84
Std Dev 11.56
Turn on : 27.9806
Width : 3.231
Height : 10.012
Entry
ampl
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6
8
10
12
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0
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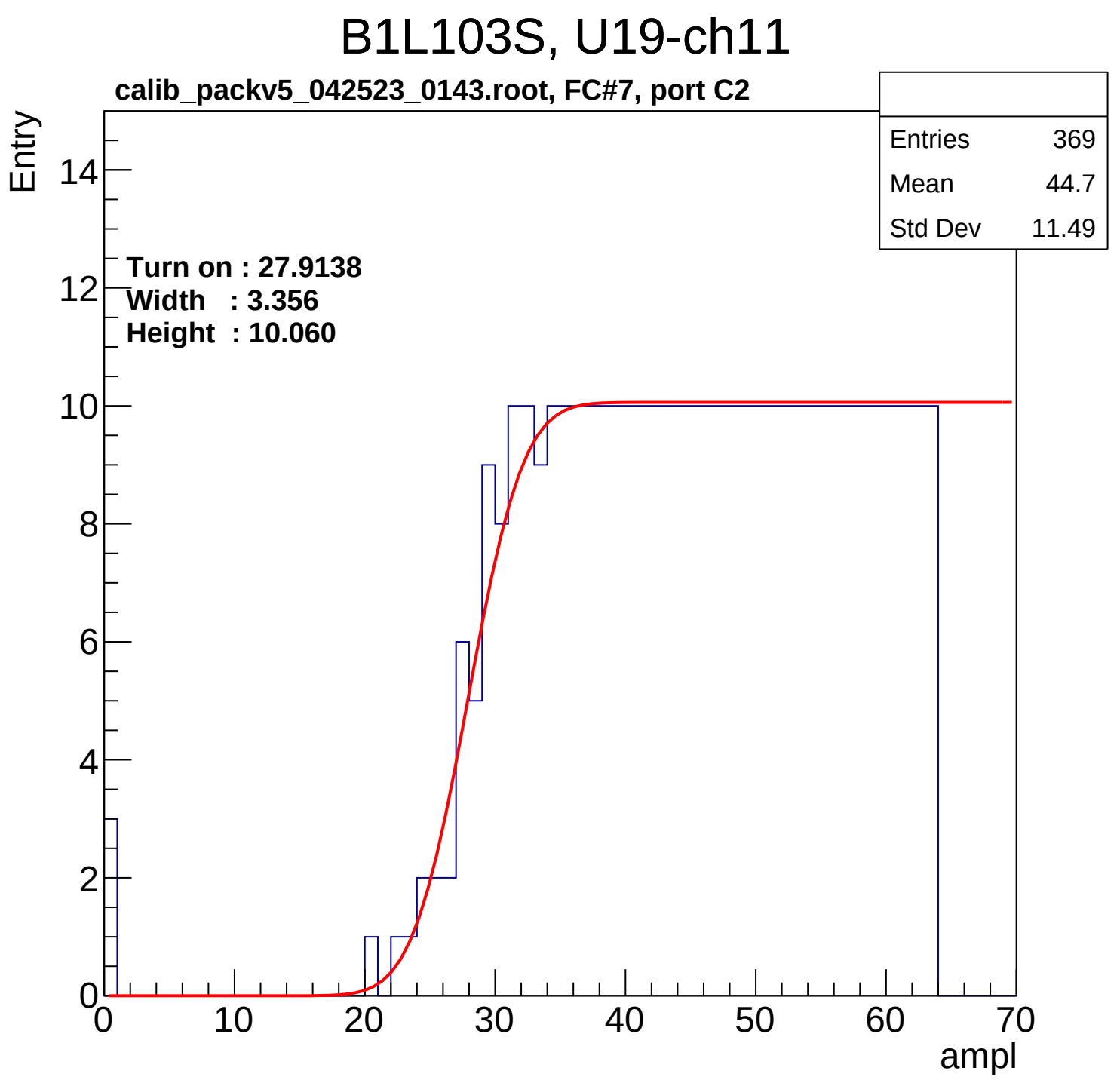
B1L103S, U19-ch11
calib_packv5_042523_0143.root, FC#7, port C2
Entries 369
Mean 44.7
Std Dev 11.49
Turn on : 27.9138
Width : 3.356
Height : 10.060
Entry
ampl
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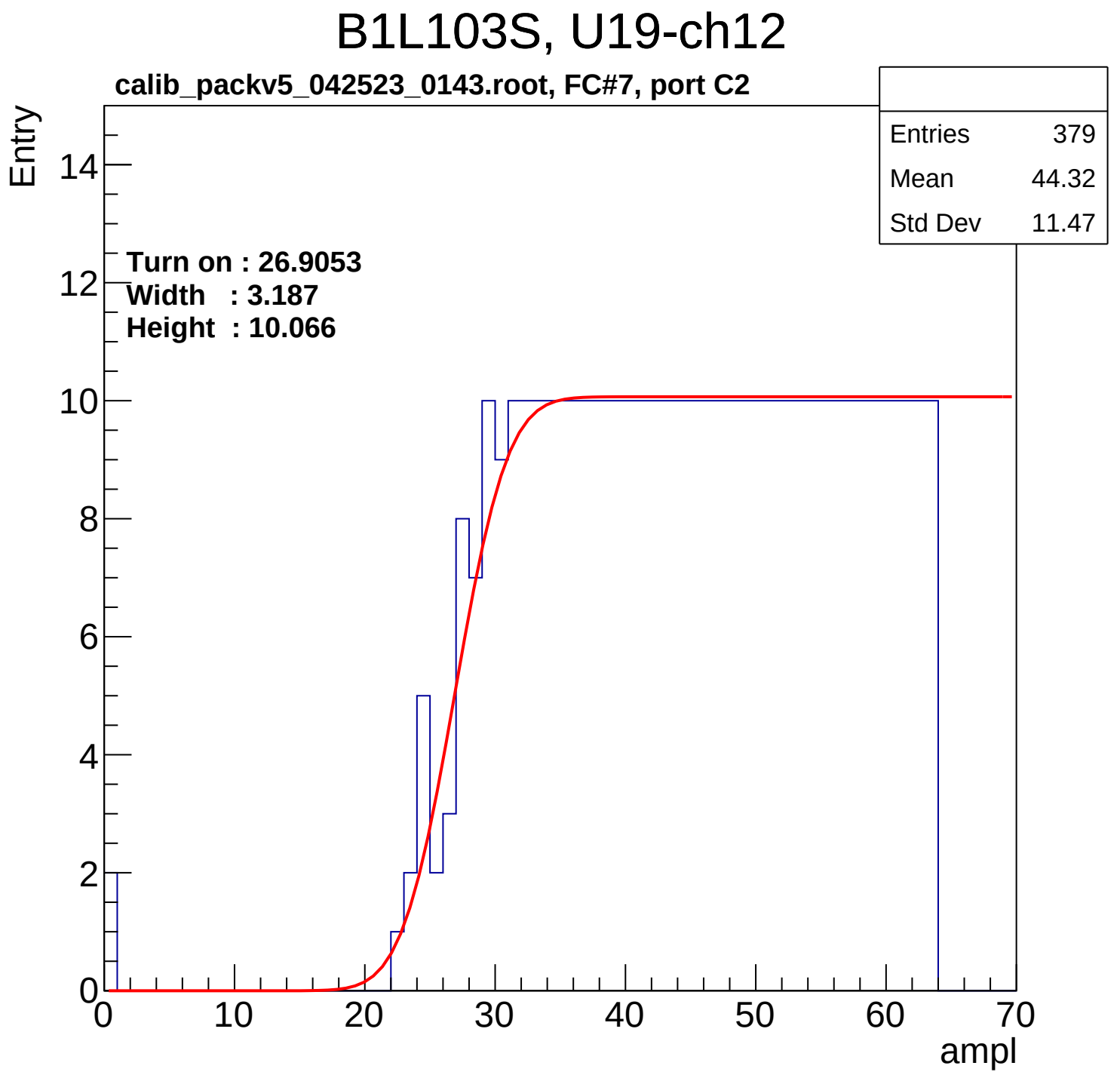
B1L103S, U19-ch12
calib_packv5_042523_0143.root, FC#7, port C2
Entries 379
Mean 44.32
Std Dev 11.47
Turn on : 26.9053
Width : 3.187
Height : 10.066
Entry
ampl
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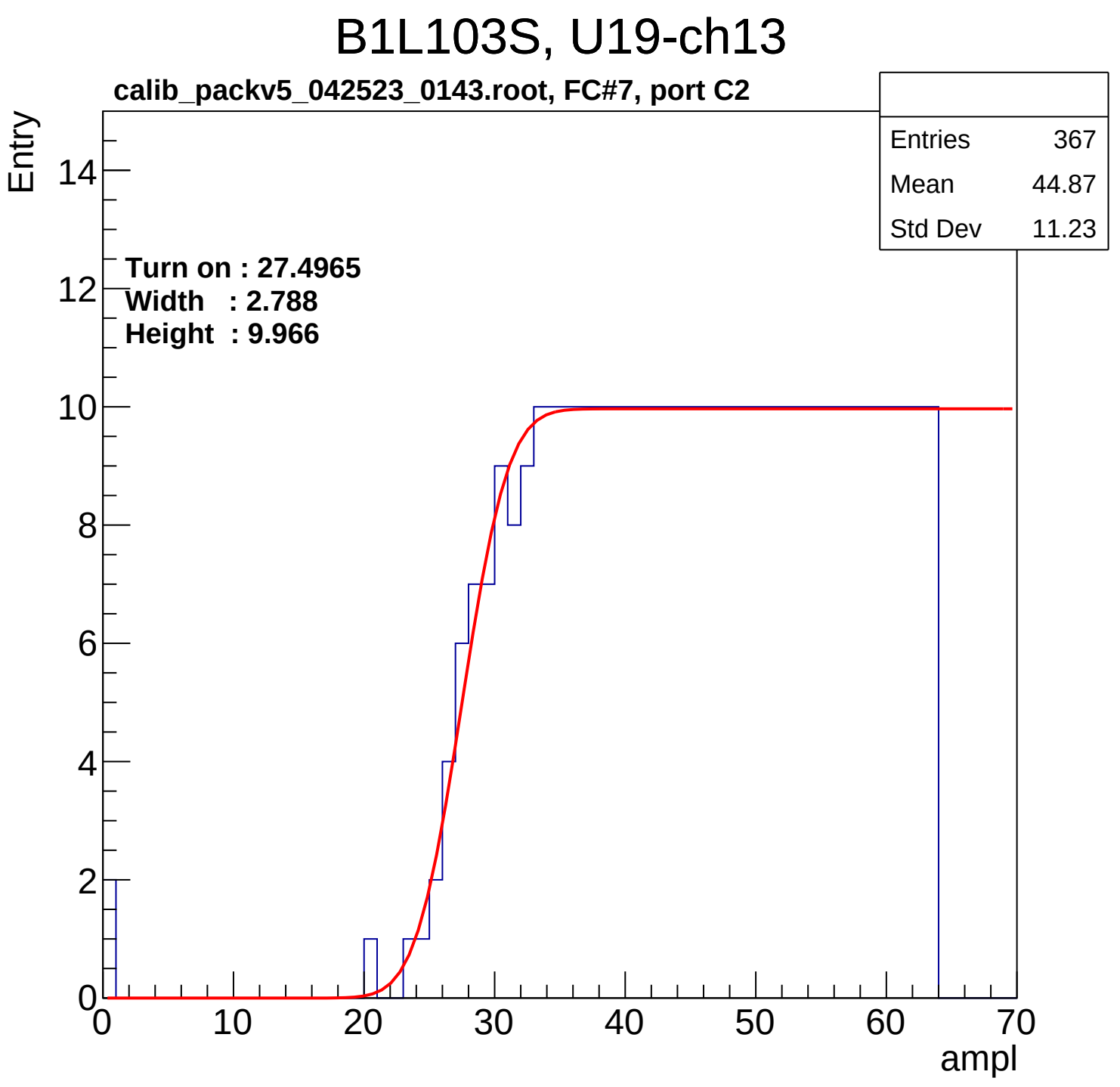
B1L103S, U19-ch13
calib_packv5_042523_0143.root, FC#7, port C2
Entries 367
Mean 44.87
Std Dev 11.23
Turn on : 27.4965
Width : 2.788
Height : 9.966
Entry
ampl
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2
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6
8
10
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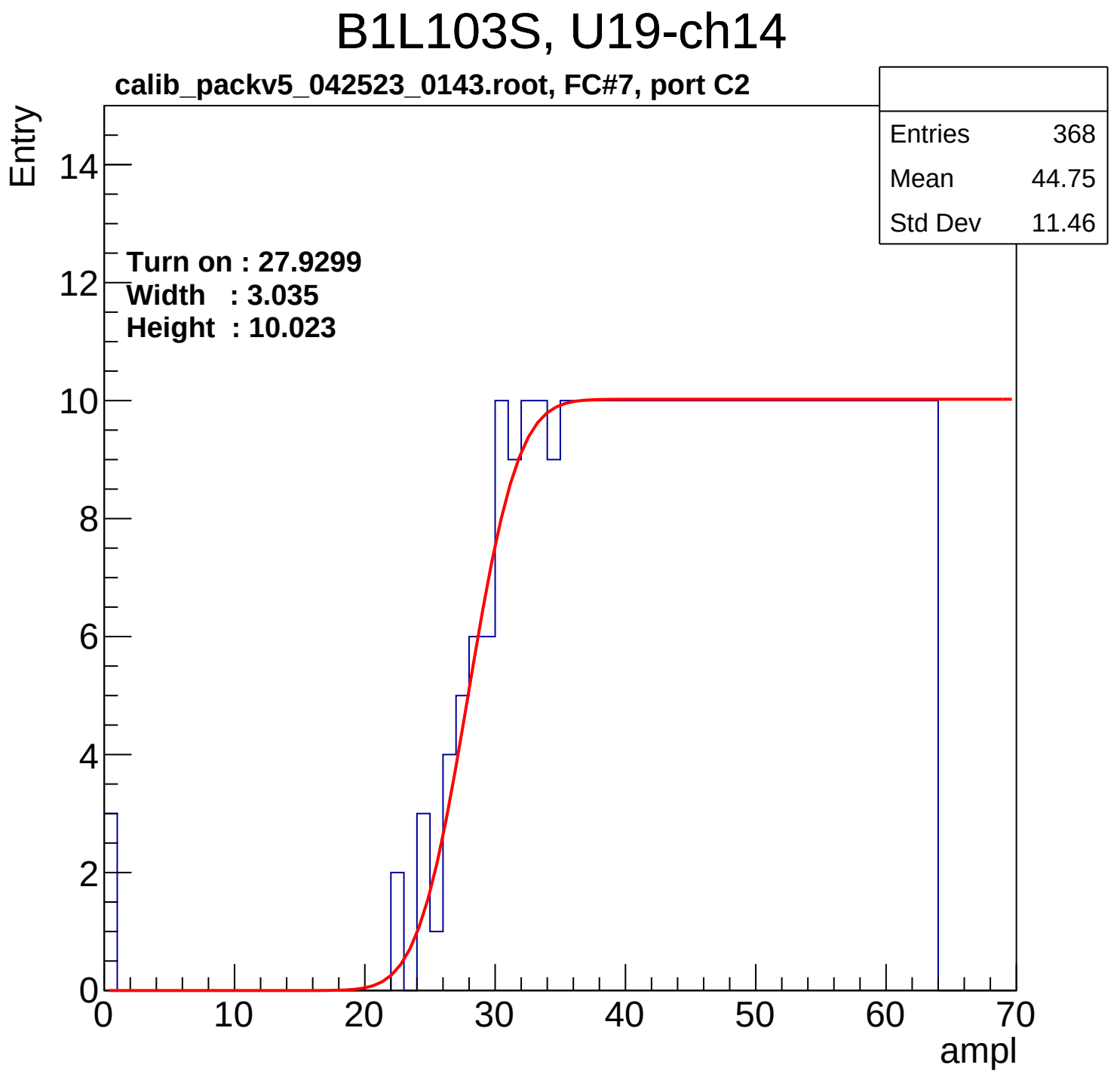
B1L103S, U19-ch14
calib_packv5_042523_0143.root, FC#7, port C2
Entries 368
Mean 44.75
Std Dev 11.46
Turn on : 27.9299
Width : 3.035
Height : 10.023
Entry
ampl
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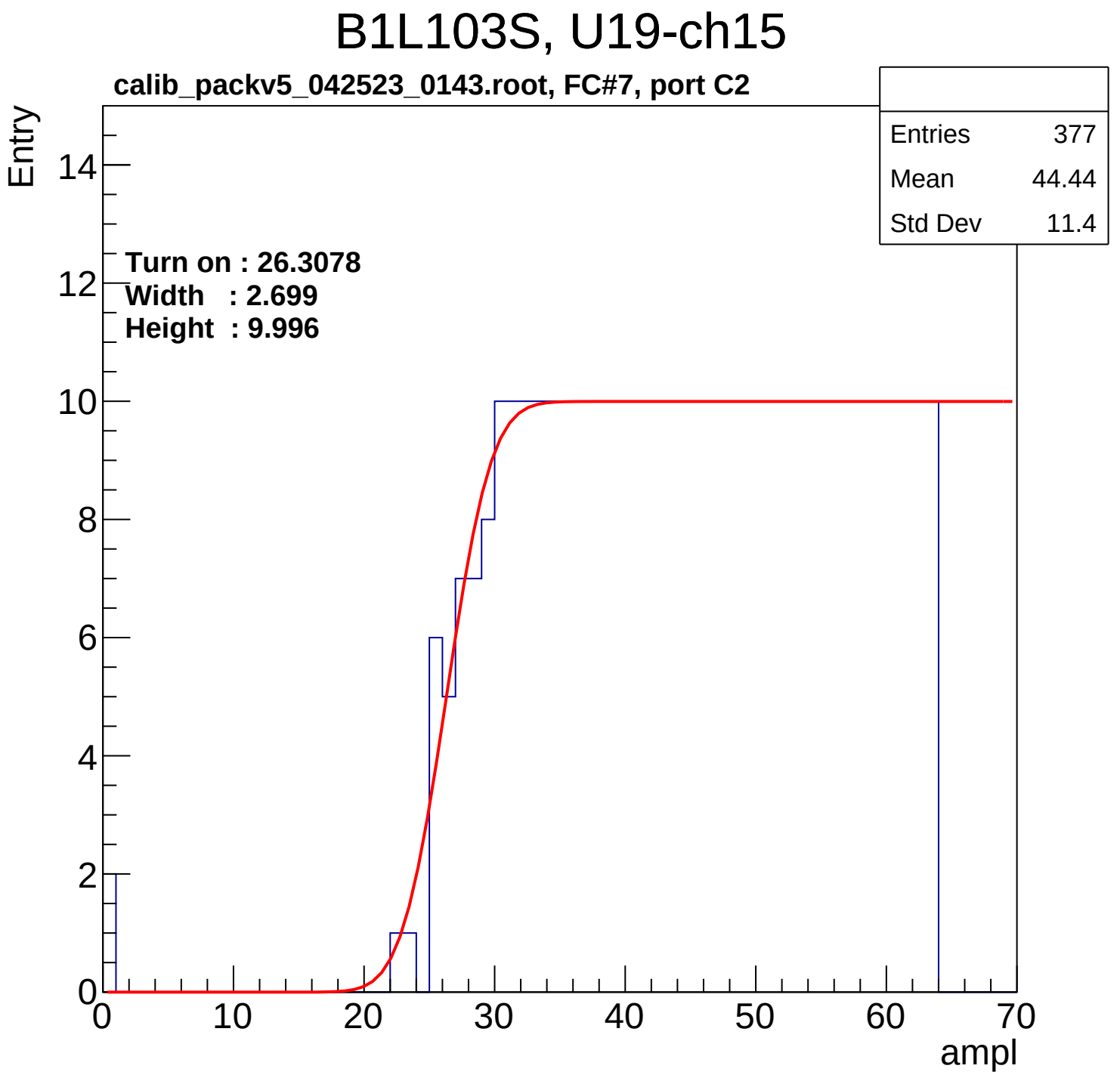
B1L103S, U19-ch15
calib_packv5_042523_0143.root, FC#7, port C2
Entries 377
Mean 44.44
Std Dev 11.4
Turn on : 26.3078
Width : 2.699
Height : 9.996
Entry
ampl
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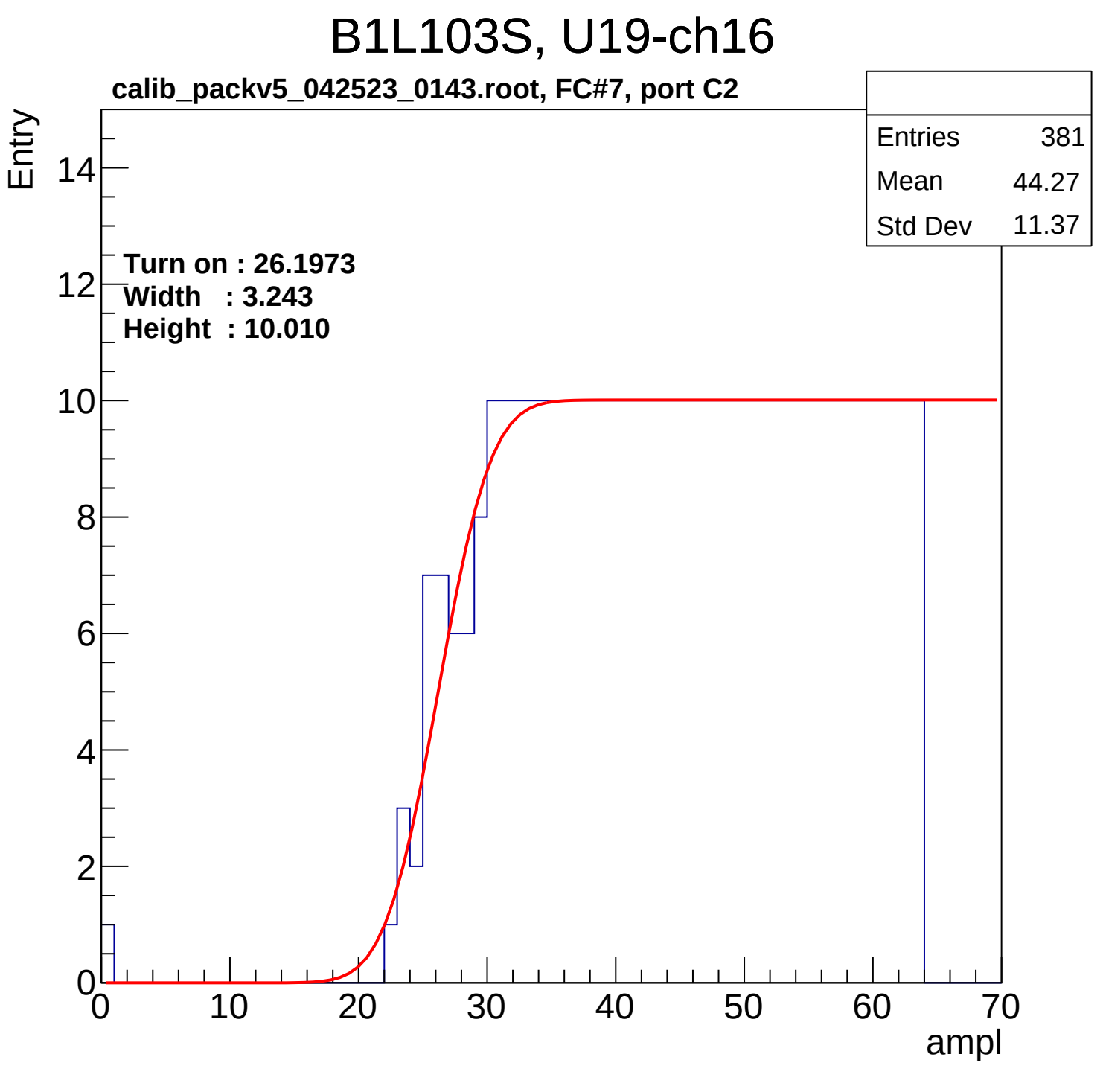
B1L103S, U19-ch16
calib_packv5_042523_0143.root, FC#7, port C2
Entries 381
Mean 44.27
Std Dev 11.37
Turn on : 26.1973
Width : 3.243
Height : 10.010
Entry
ampl
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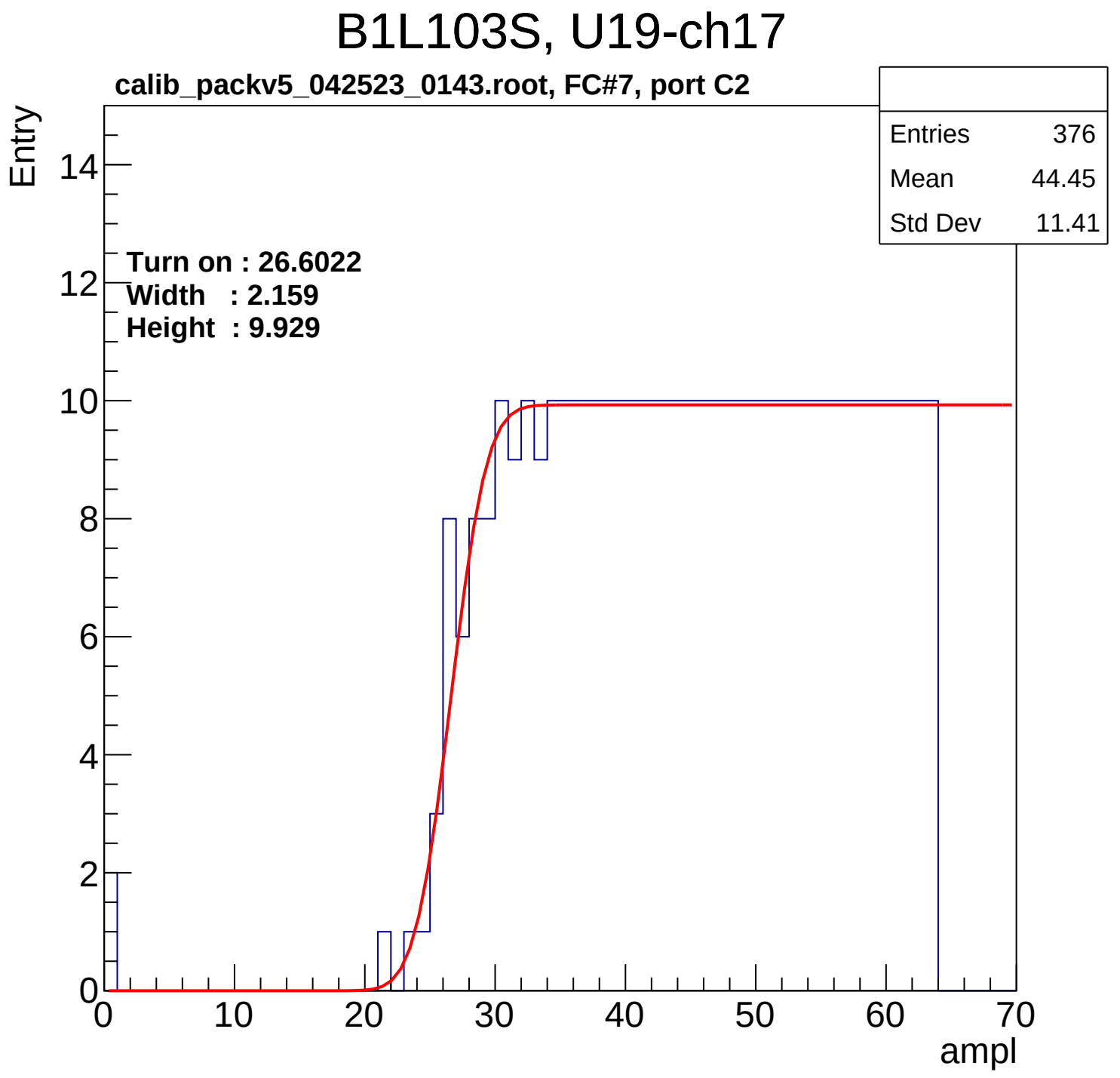
B1L103S, U19-ch17
calib_packv5_042523_0143.root, FC#7, port C2
Entries 376
Mean 44.45
Std Dev 11.41
Turn on : 26.6022
Width : 2.159
Height : 9.929
Entry
ampl
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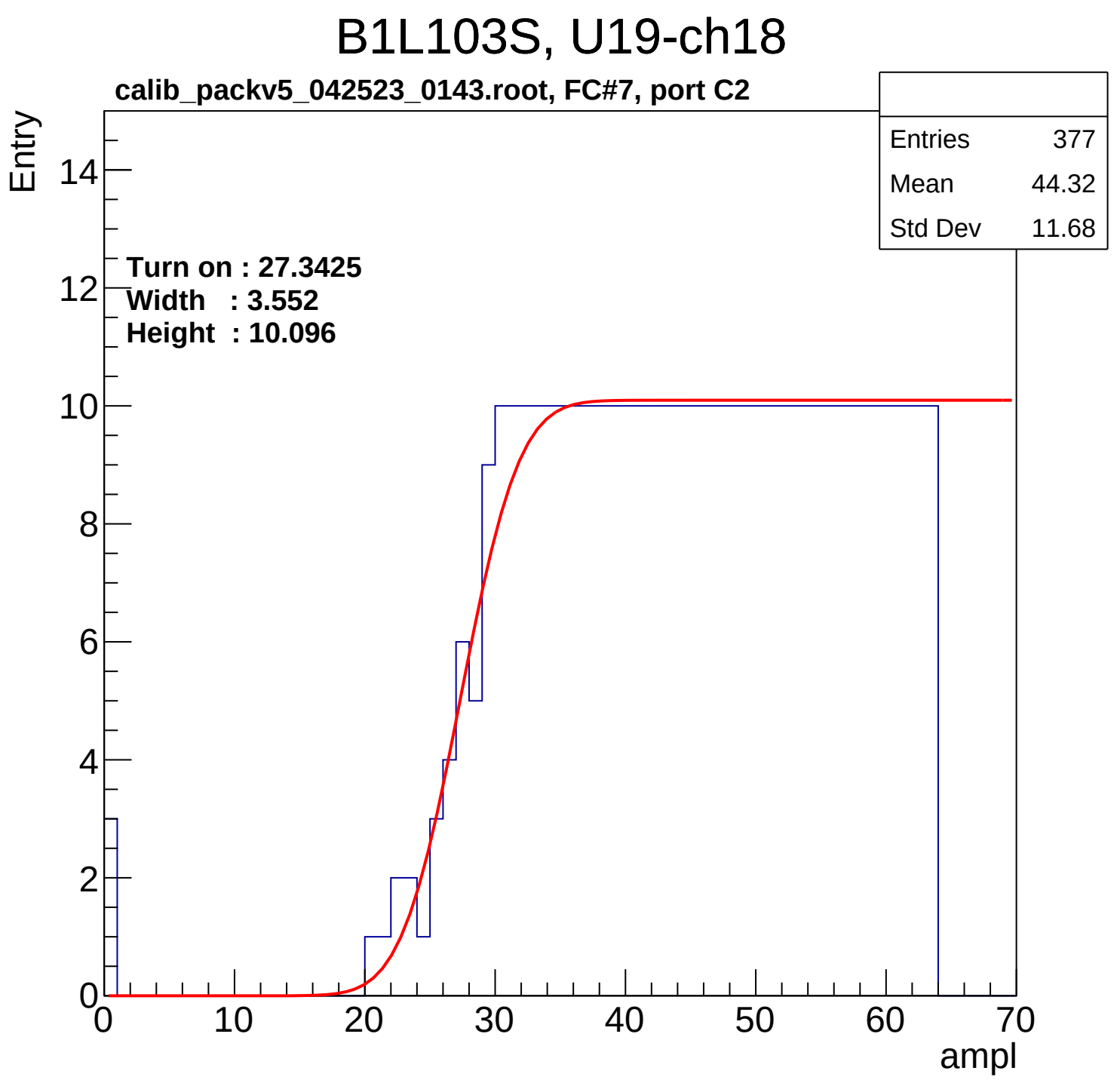
B1L103S, U19-ch18
calib_packv5_042523_0143.root, FC#7, port C2
Entries 377
Mean 44.32
Std Dev 11.68
Turn on : 27.3425
Width : 3.552
Height : 10.096
Entry
ampl
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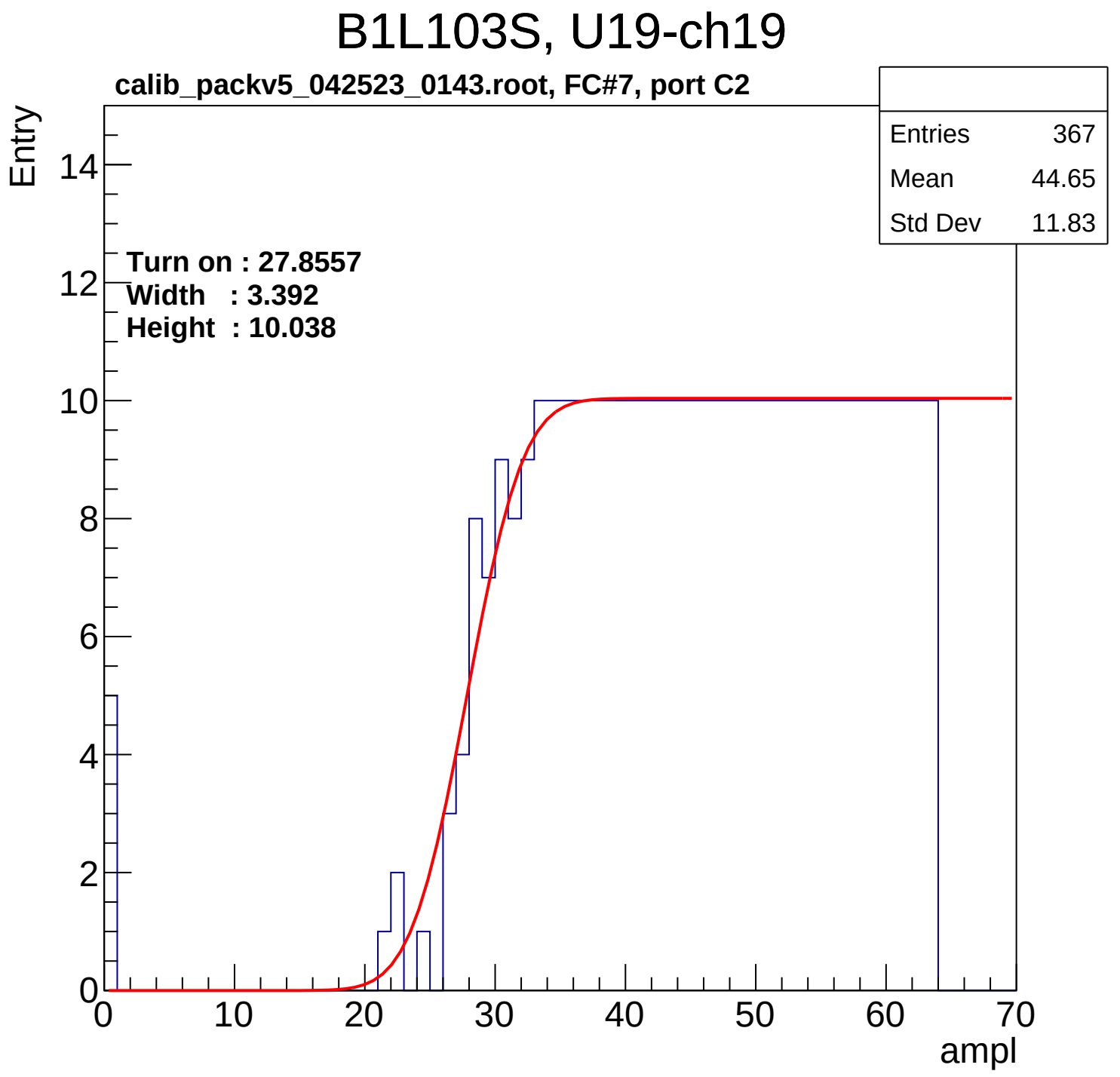
B1L103S, U19-ch19
calib_packv5_042523_0143.root, FC#7, port C2
Entries 367
Mean 44.65
Std Dev 11.83
Turn on : 27.8557
Width : 3.392
Height : 10.038
Entry
ampl
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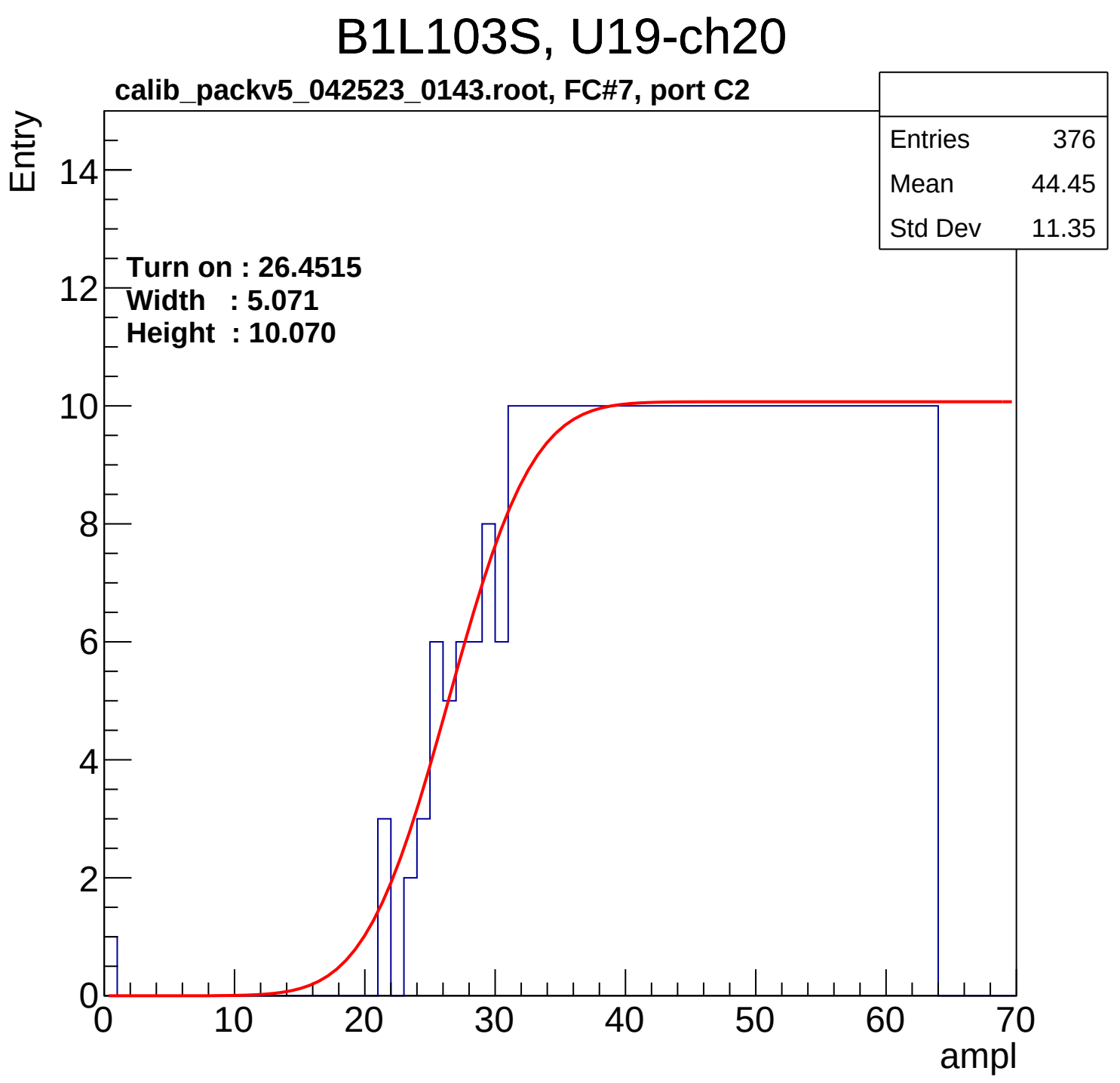
B1L103S, U19-ch20
calib_packv5_042523_0143.root, FC#7, port C2
Entries 376
Mean 44.45
Std Dev 11.35
Turn on : 26.4515
Width : 5.071
Height : 10.070
Entry
ampl
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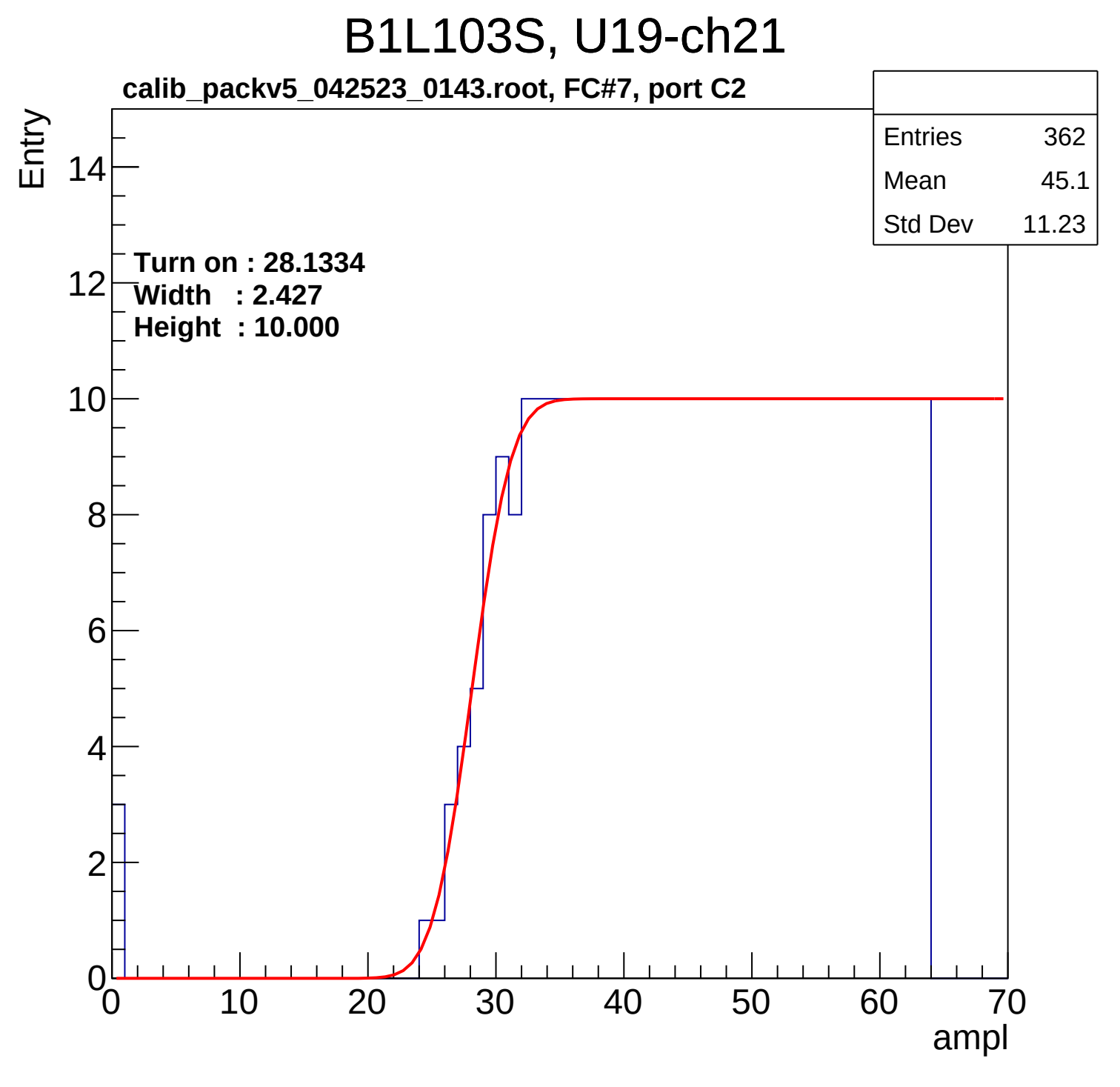
B1L103S, U19-ch21
calib_packv5_042523_0143.root, FC#7, port C2
Entries 362
Mean 45.1
Std Dev 11.23
Turn on : 28.1334
Width : 2.427
Height : 10.000
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ampl
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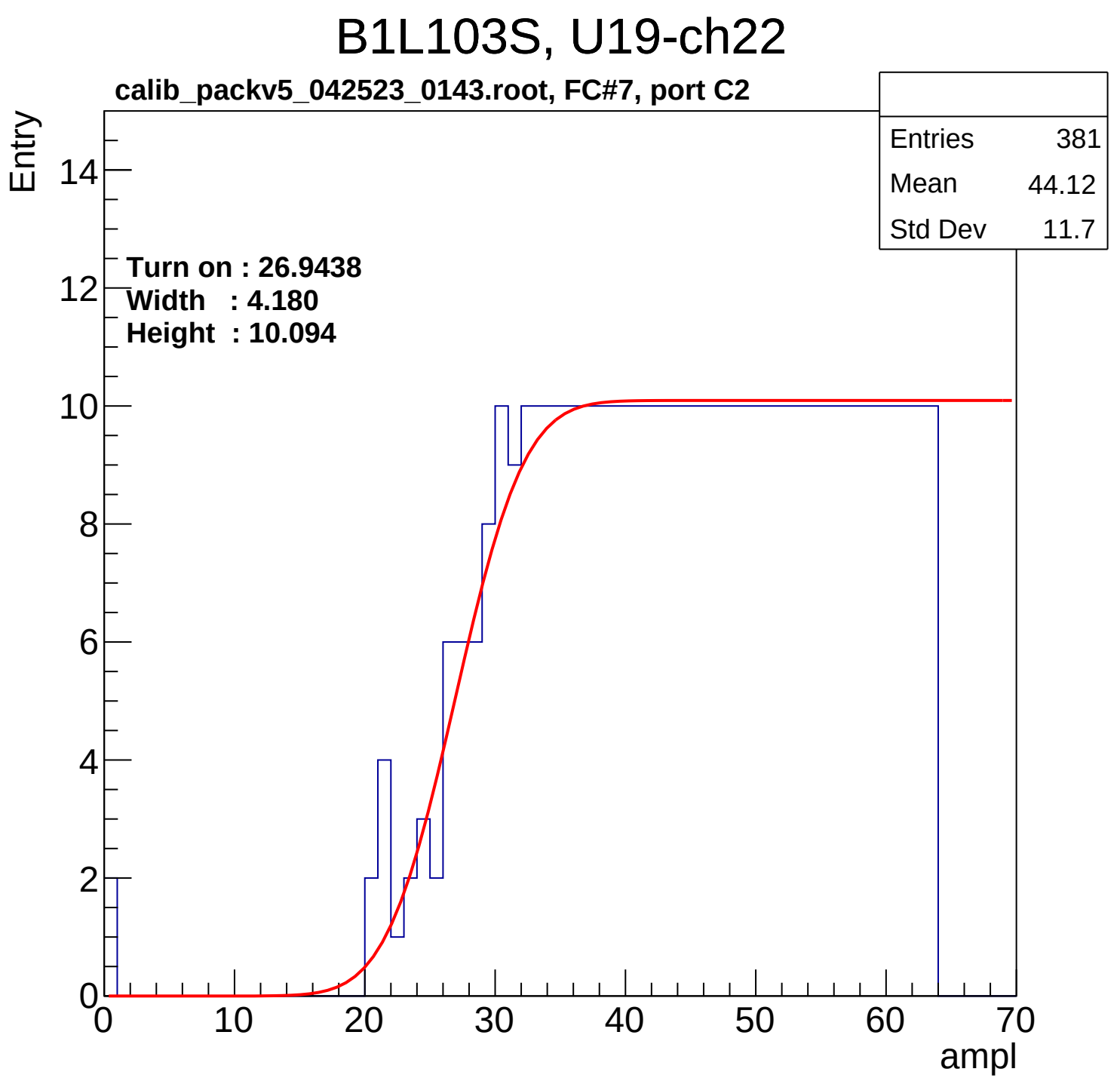
B1L103S, U19-ch22
calib_packv5_042523_0143.root, FC#7, port C2
Entries 381
Mean 44.12
Std Dev 11.7
Turn on : 26.9438
Width : 4.180
Height : 10.094
Entry
ampl
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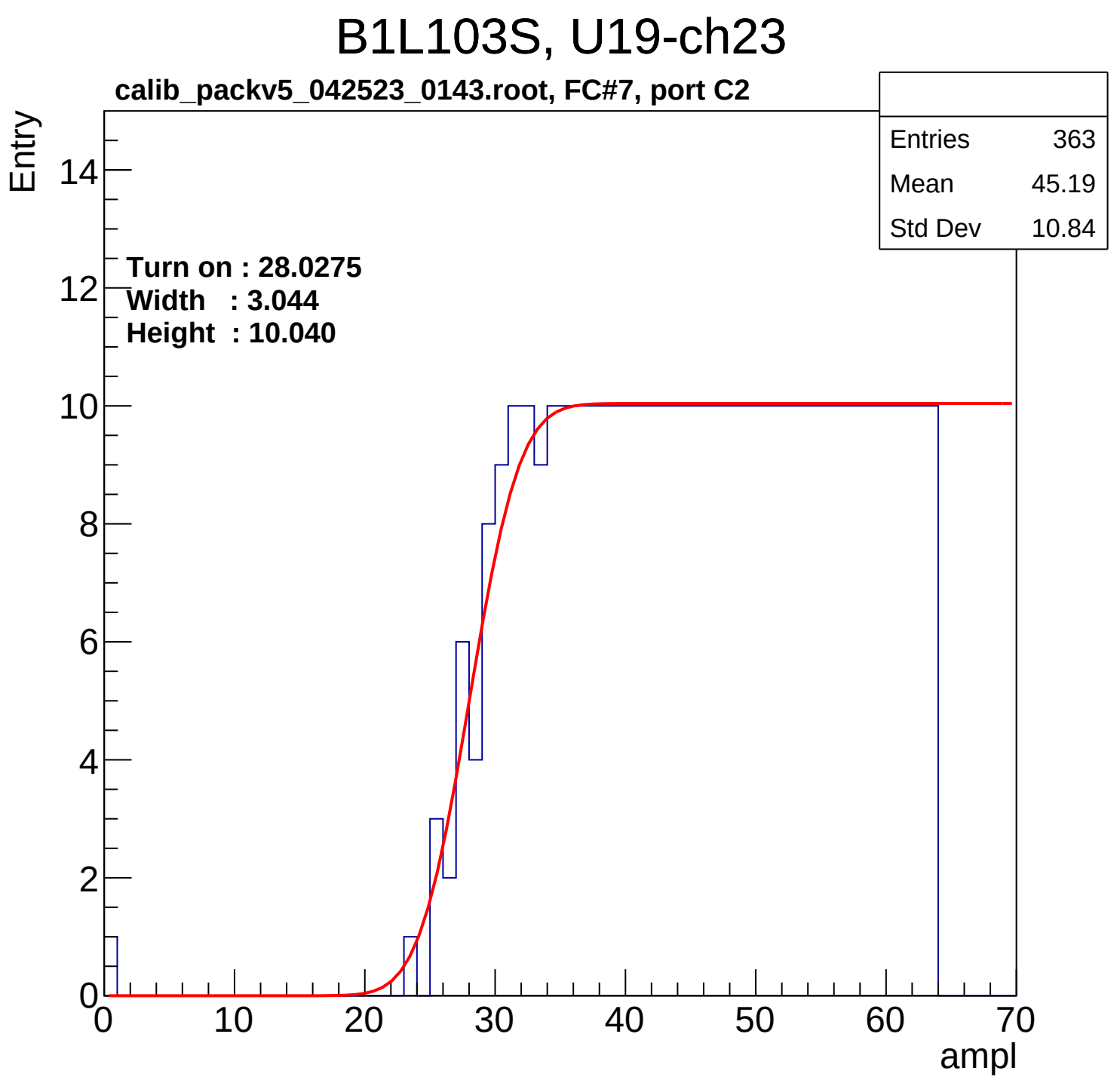
B1L103S, U19-ch23
calib_packv5_042523_0143.root, FC#7, port C2
Entries 363
Mean 45.19
Std Dev 10.84
Turn on : 28.0275
Width : 3.044
Height : 10.040
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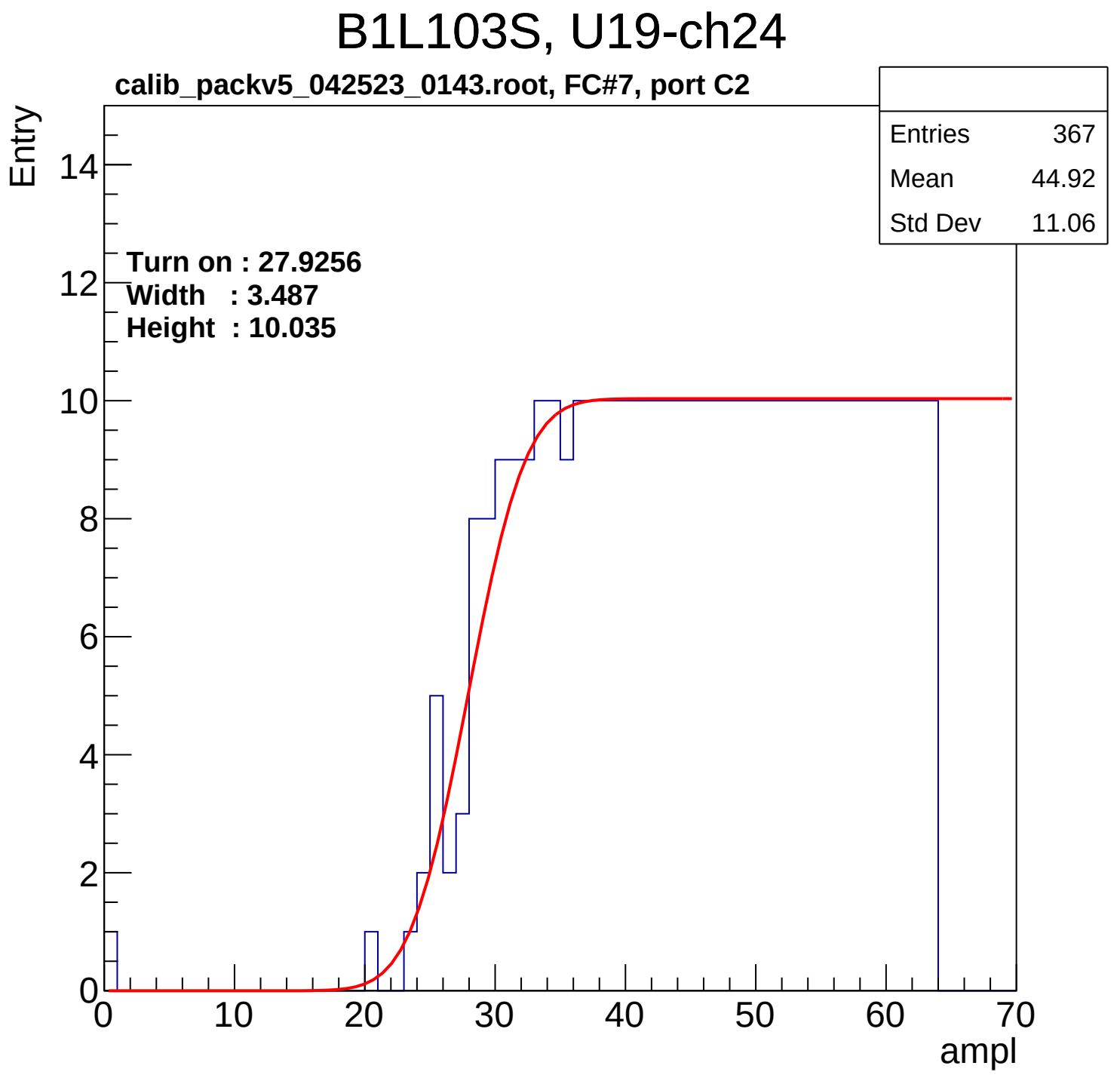
B1L103S, U19-ch24
calib_packv5_042523_0143.root, FC#7, port C2
Entries 367
Mean 44.92
Std Dev 11.06
Turn on : 27.9256
Width : 3.487
Height : 10.035
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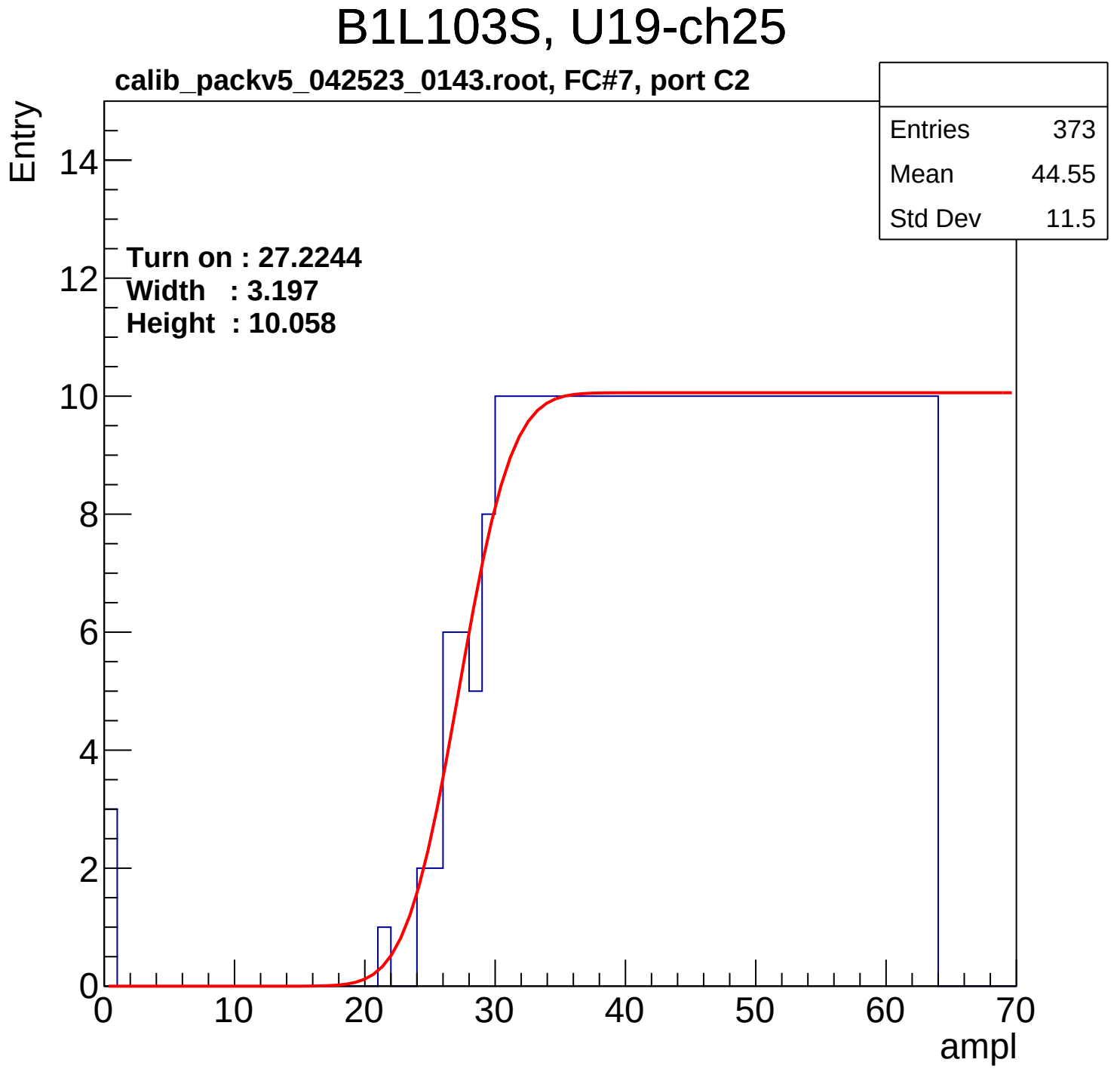
B1L103S, U19-ch25
calib_packv5_042523_0143.root, FC#7, port C2
Entries 373
Mean 44.55
Std Dev 11.5
Turn on : 27.2244
Width : 3.197
Height : 10.058
Entry
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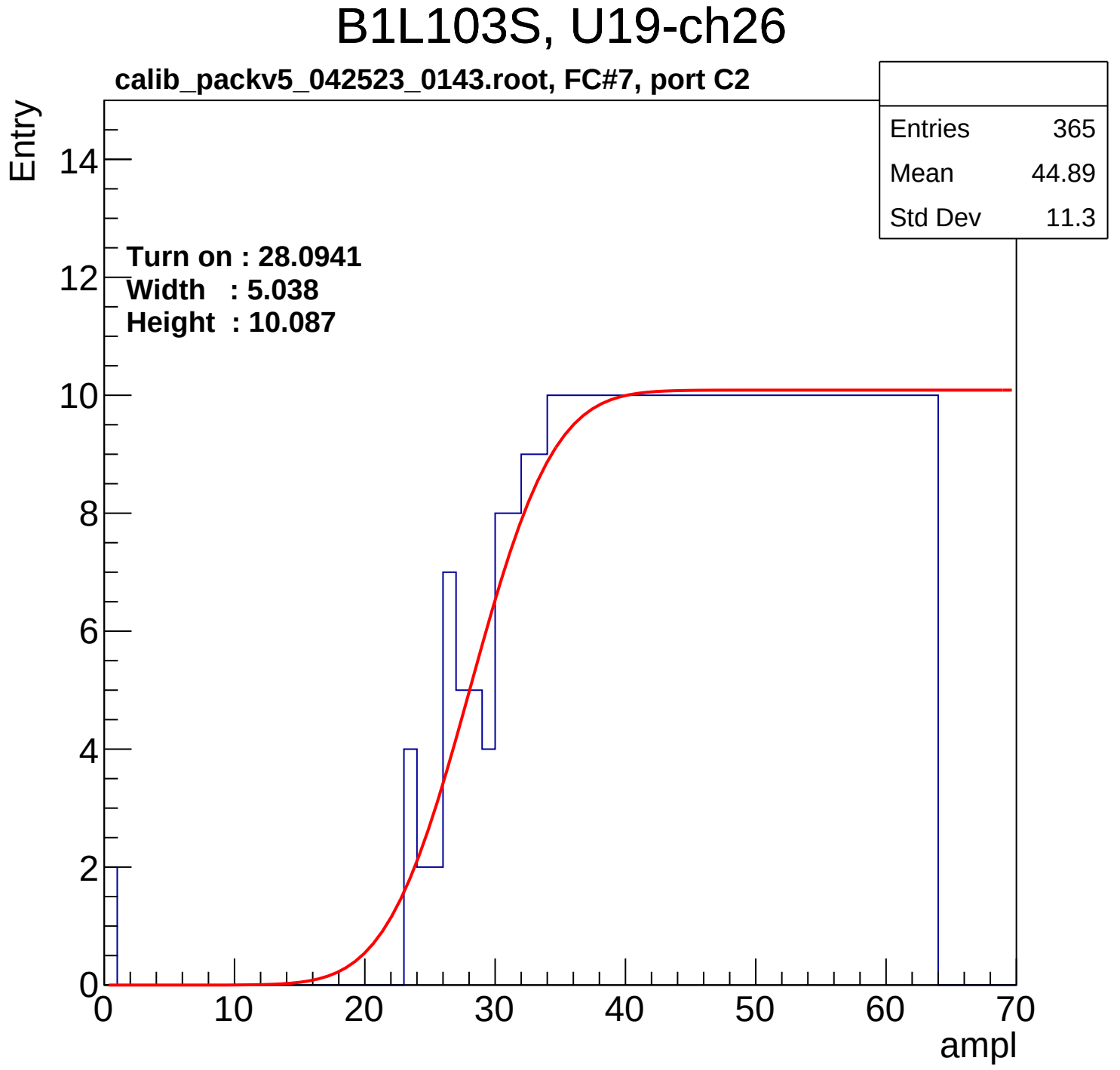
B1L103S, U19-ch26
calib_packv5_042523_0143.root, FC#7, port C2
Entries 365
Mean 44.89
Std Dev 11.3
Turn on : 28.0941
Width : 5.038
Height : 10.087
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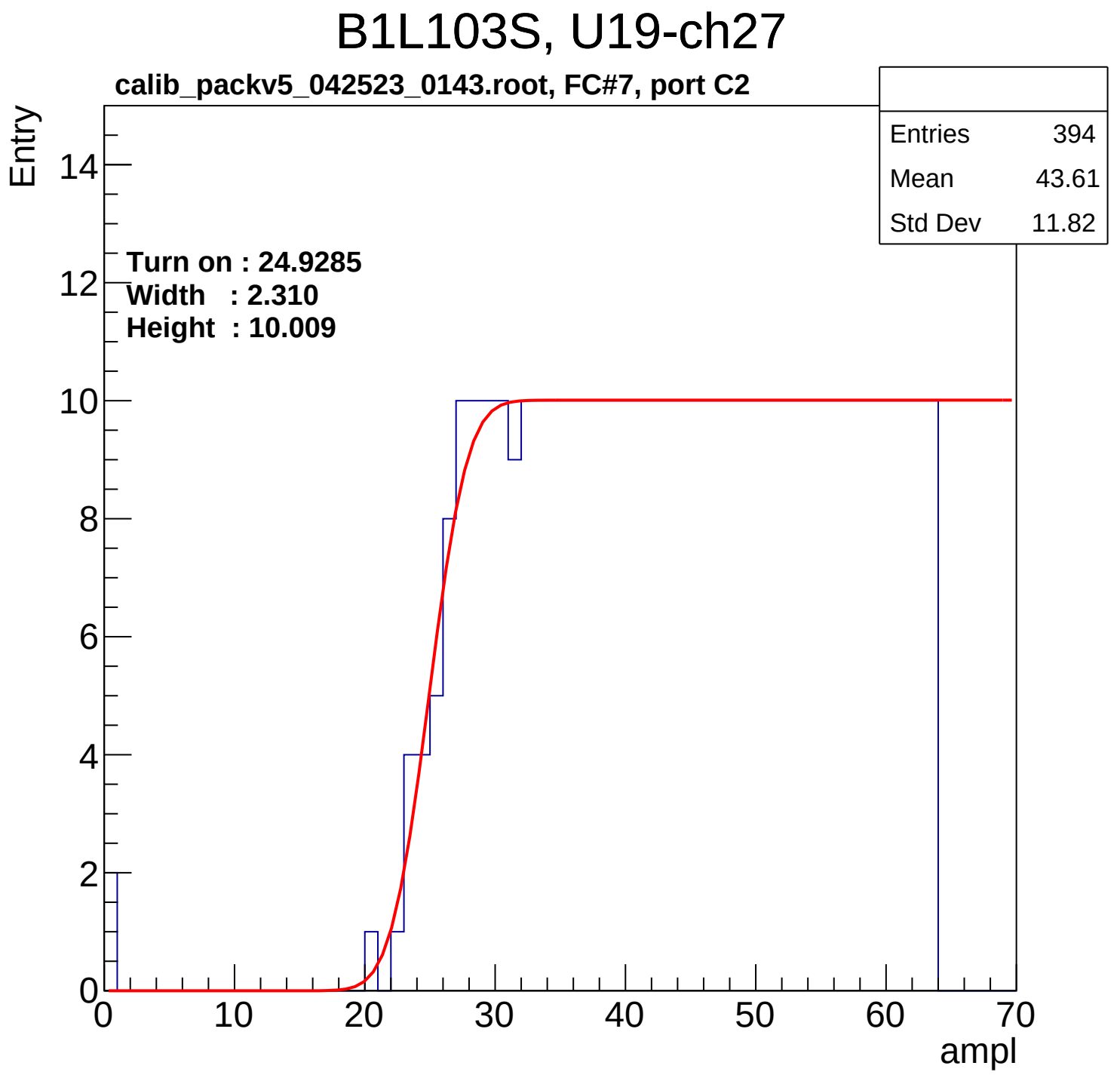
B1L103S, U19-ch27
calib_packv5_042523_0143.root, FC#7, port C2
Entries 394
Mean 43.61
Std Dev 11.82
Turn on : 24.9285
Width : 2.310
Height : 10.009
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ampl
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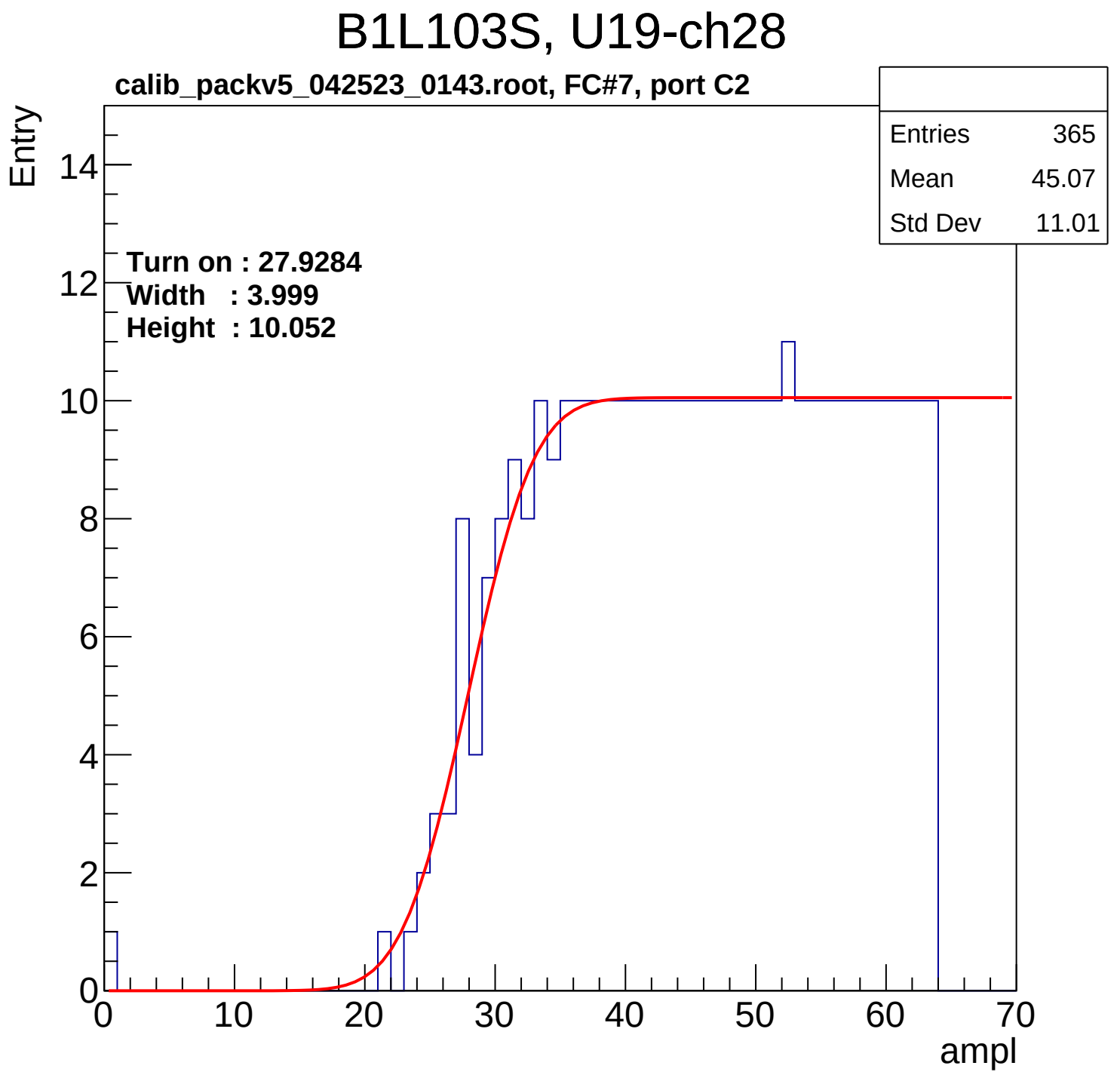
B1L103S, U19-ch28
calib_packv5_042523_0143.root, FC#7, port C2
Entries 365
Mean 45.07
Std Dev 11.01
Turn on : 27.9284
Width : 3.999
Height : 10.052
Entry
ampl
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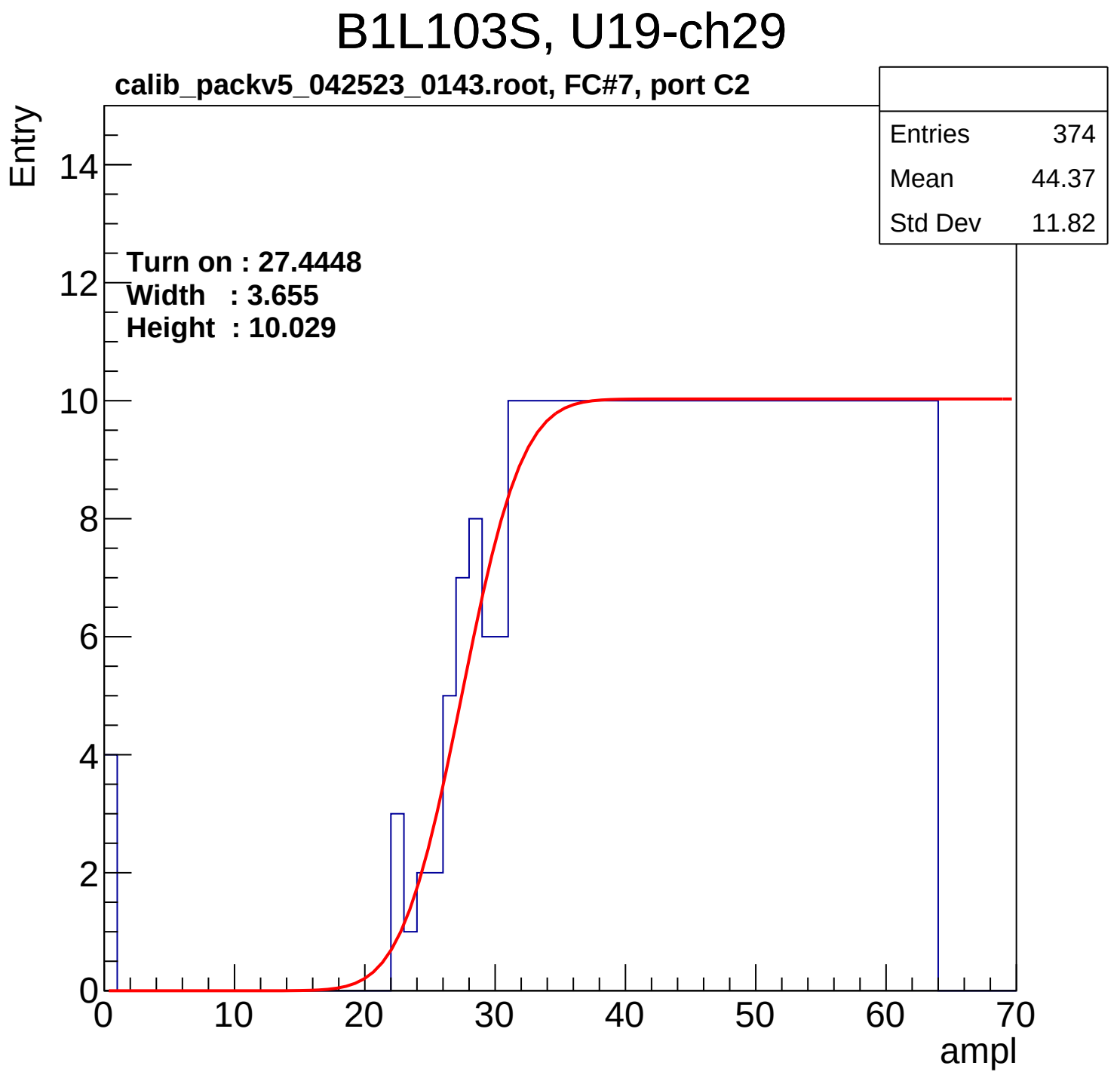
B1L103S, U19-ch29
calib_packv5_042523_0143.root, FC#7, port C2
Entries 374
Mean 44.37
Std Dev 11.82
Turn on : 27.4448
Width : 3.655
Height : 10.029
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ampl
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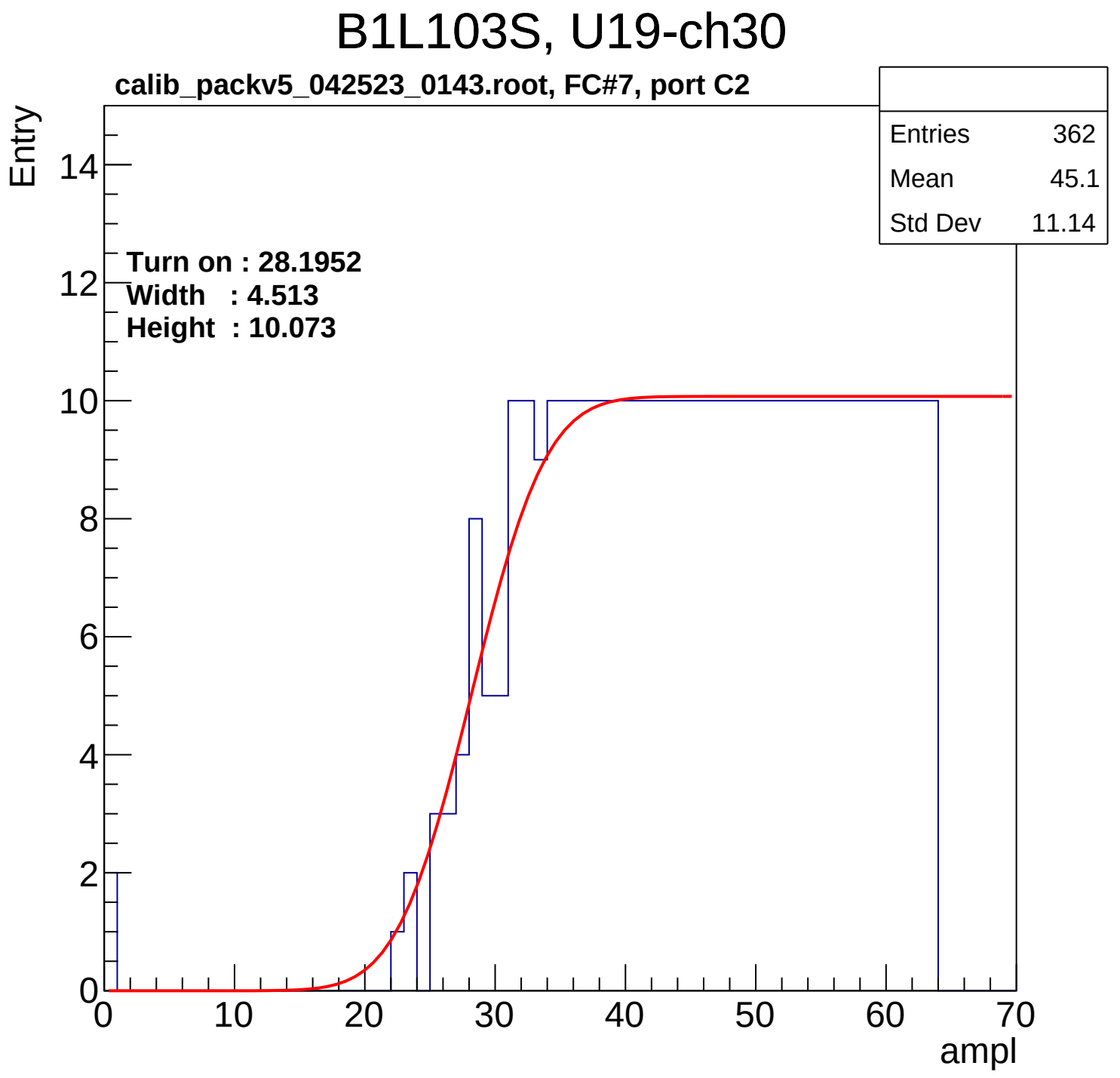
B1L103S, U19-ch30
calib_packv5_042523_0143.root, FC#7, port C2
Entries 362
Mean 45.1
Std Dev 11.14
Turn on : 28.1952
Width : 4.513
Height : 10.073
Entry
ampl
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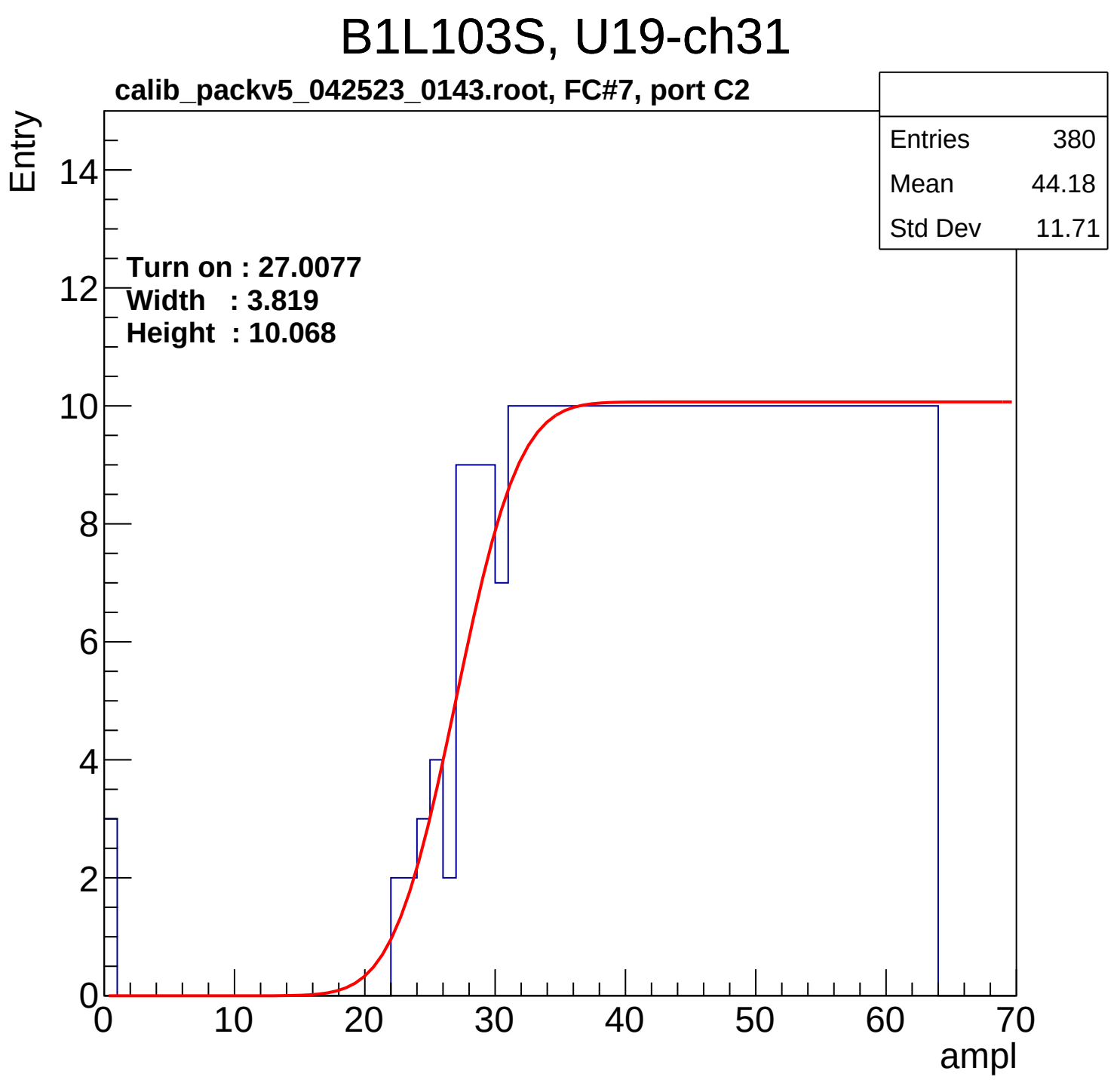
B1L103S, U19-ch31
calib_packv5_042523_0143.root, FC#7, port C2
Entries 380
Mean 44.18
Std Dev 11.71
Turn on : 27.0077
Width : 3.819
Height : 10.068
Entry
ampl
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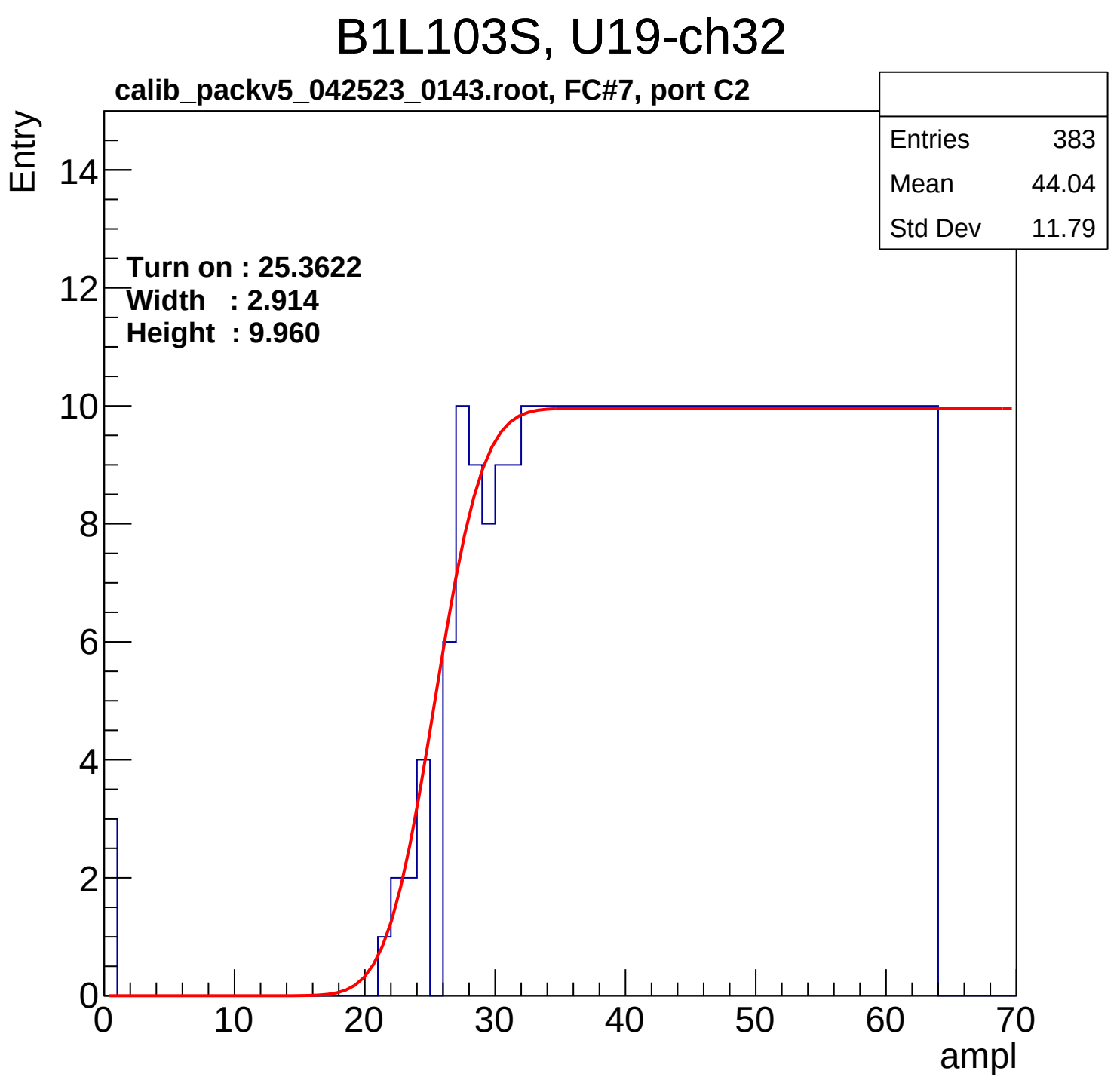
B1L103S, U19-ch32
calib_packv5_042523_0143.root, FC#7, port C2
Entries 383
Mean 44.04
Std Dev 11.79
Turn on : 25.3622
Width : 2.914
Height : 9.960
Entry
ampl
0
2
4
6
8
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0
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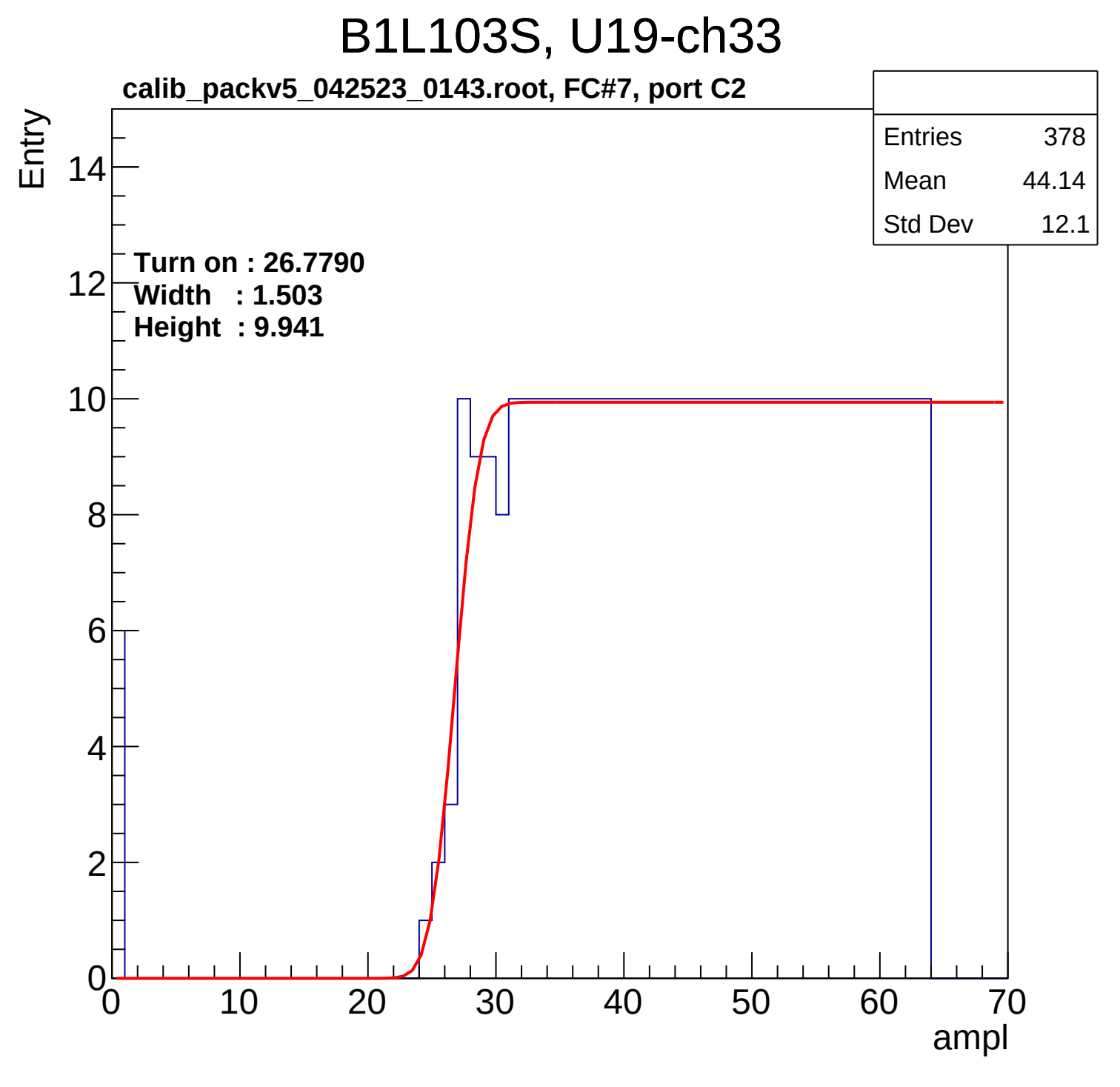
B1L103S, U19-ch33
calib_packv5_042523_0143.root, FC#7, port C2
Entries 378
Mean 44.14
Std Dev 12.1
Turn on : 26.7790
Width : 1.503
Height : 9.941
Entry
ampl
0
2
4
6
8
10
12
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0
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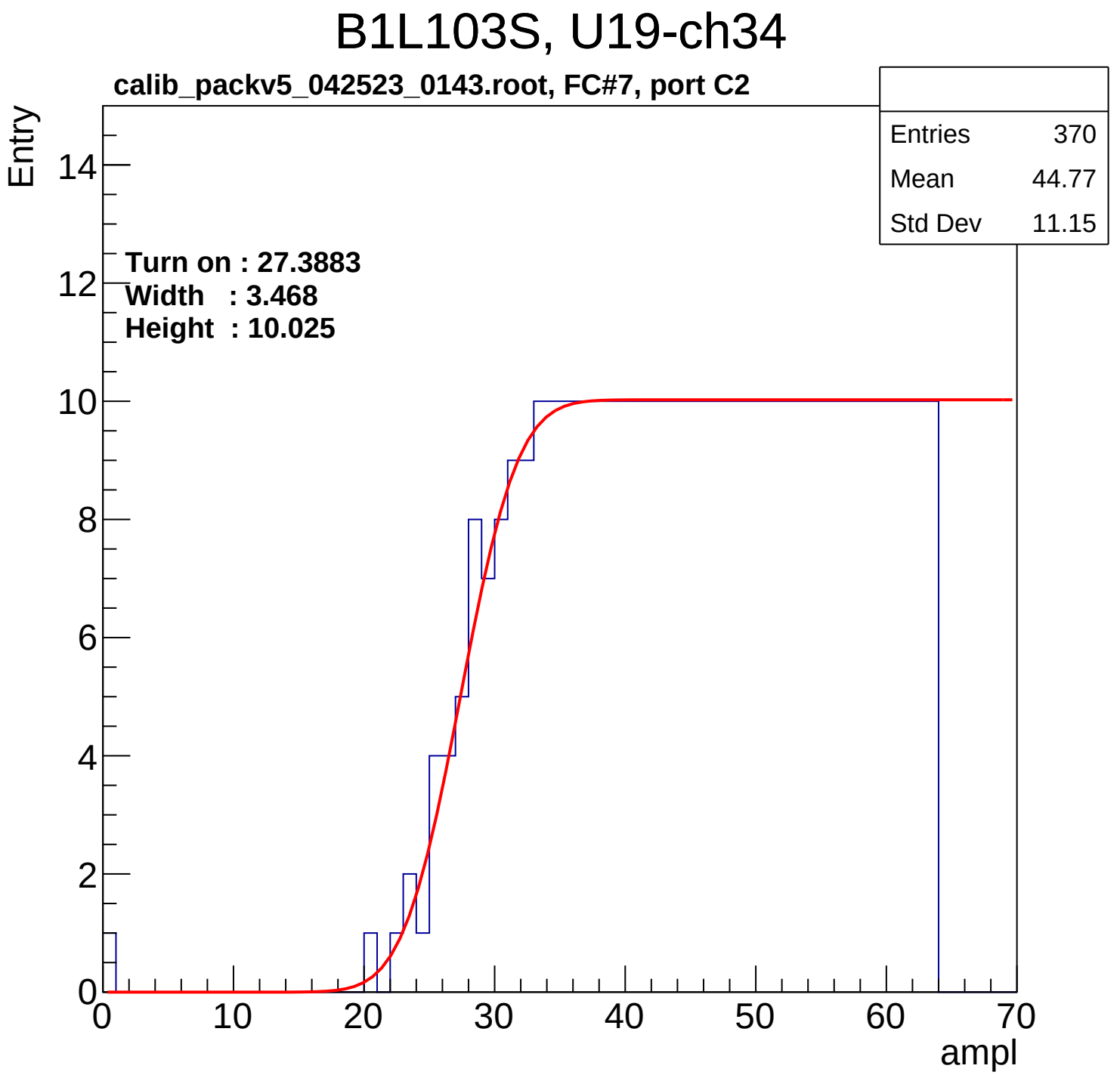
B1L103S, U19-ch34
calib_packv5_042523_0143.root, FC#7, port C2
Entries 370
Mean 44.77
Std Dev 11.15
Turn on : 27.3883
Width : 3.468
Height : 10.025
Entry
ampl
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4
6
8
10
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0
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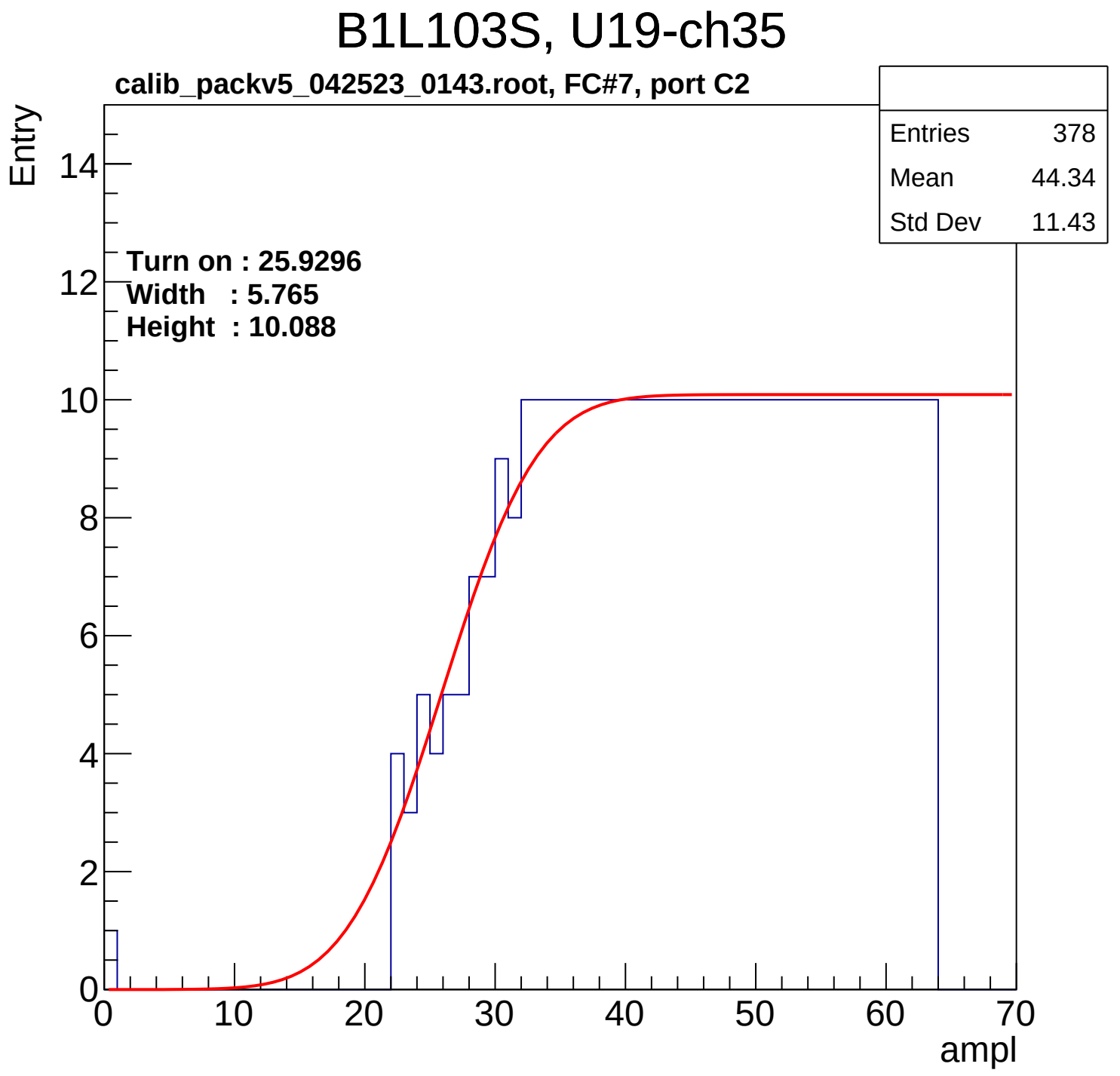
B1L103S, U19-ch35
calib_packv5_042523_0143.root, FC#7, port C2
Entries 378
Mean 44.34
Std Dev 11.43
Turn on : 25.9296
Width : 5.765
Height : 10.088
Entry
ampl
0
2
4
6
8
10
12
14
0
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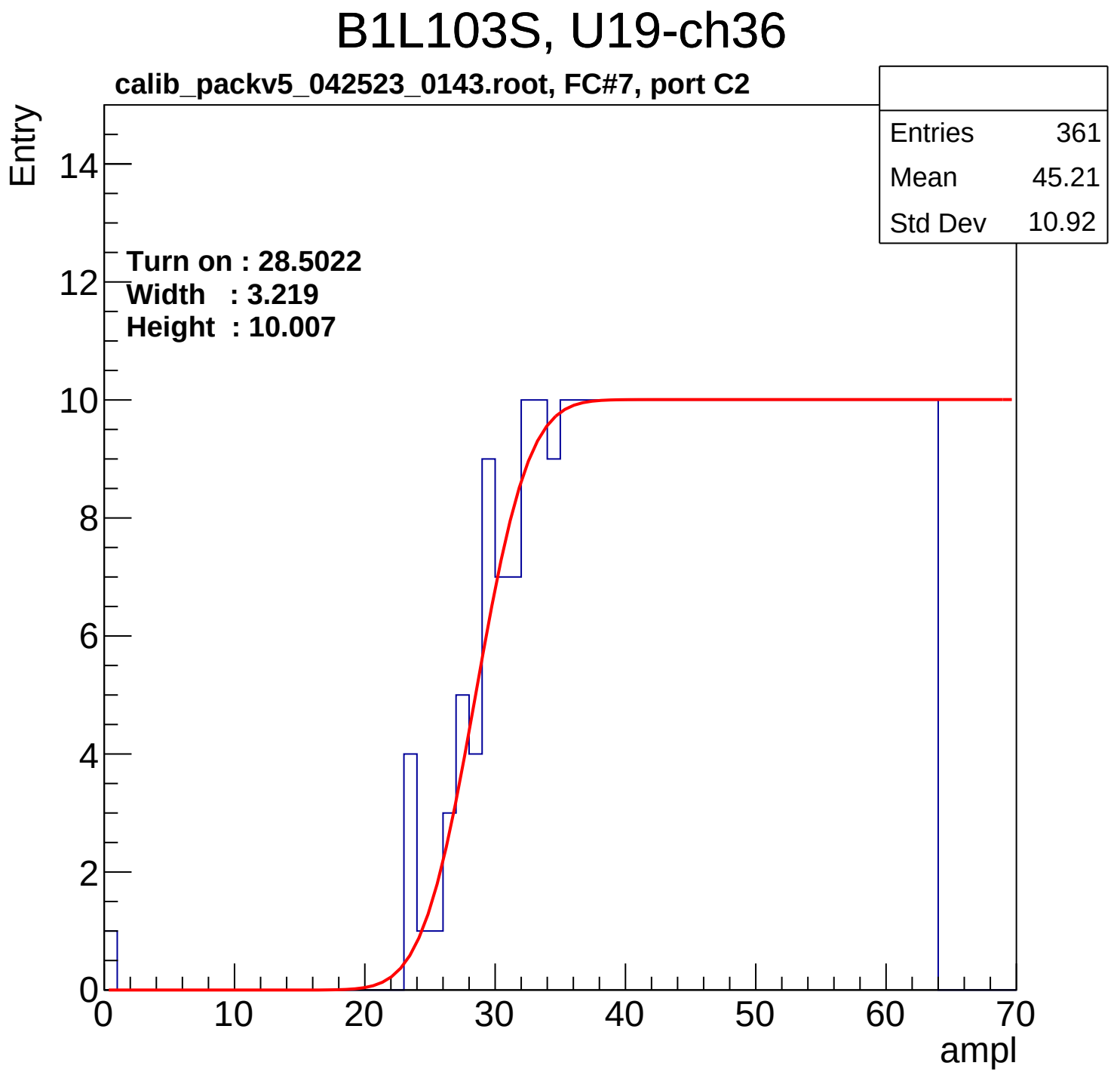
B1L103S, U19-ch36
calib_packv5_042523_0143.root, FC#7, port C2
Entries 361
Mean 45.21
Std Dev 10.92
Turn on : 28.5022
Width : 3.219
Height : 10.007
Entry
ampl
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2
4
6
8
10
12
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60
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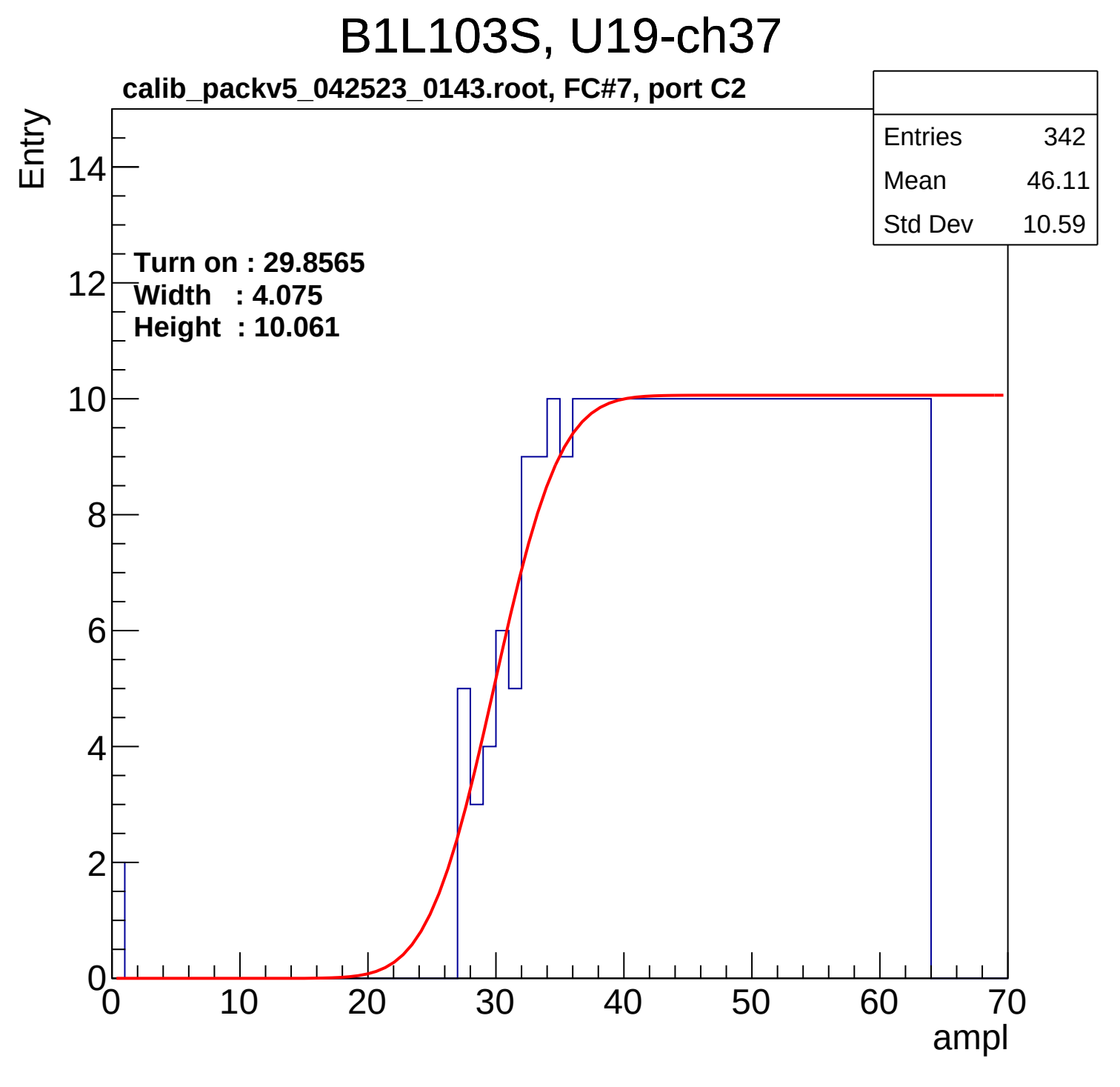
B1L103S, U19-ch37
calib_packv5_042523_0143.root, FC#7, port C2
Entries 342
Mean 46.11
Std Dev 10.59
Turn on : 29.8565
Width : 4.075
Height : 10.061
Entry
ampl
0
2
4
6
8
10
12
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0
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60
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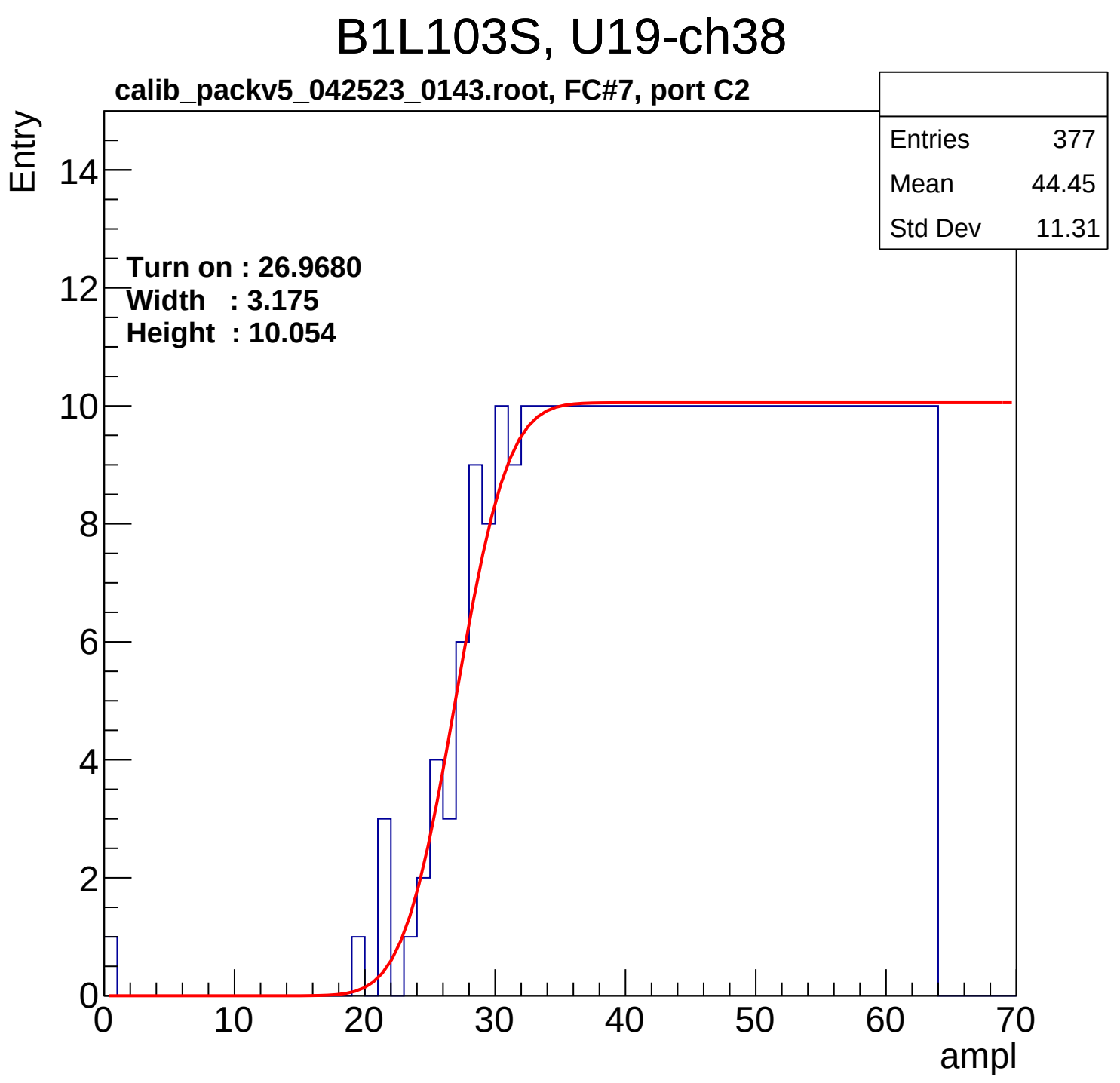
B1L103S, U19-ch38
calib_packv5_042523_0143.root, FC#7, port C2
Entries 377
Mean 44.45
Std Dev 11.31
Turn on : 26.9680
Width : 3.175
Height : 10.054
Entry
ampl
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2
4
6
8
10
12
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0
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20
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60
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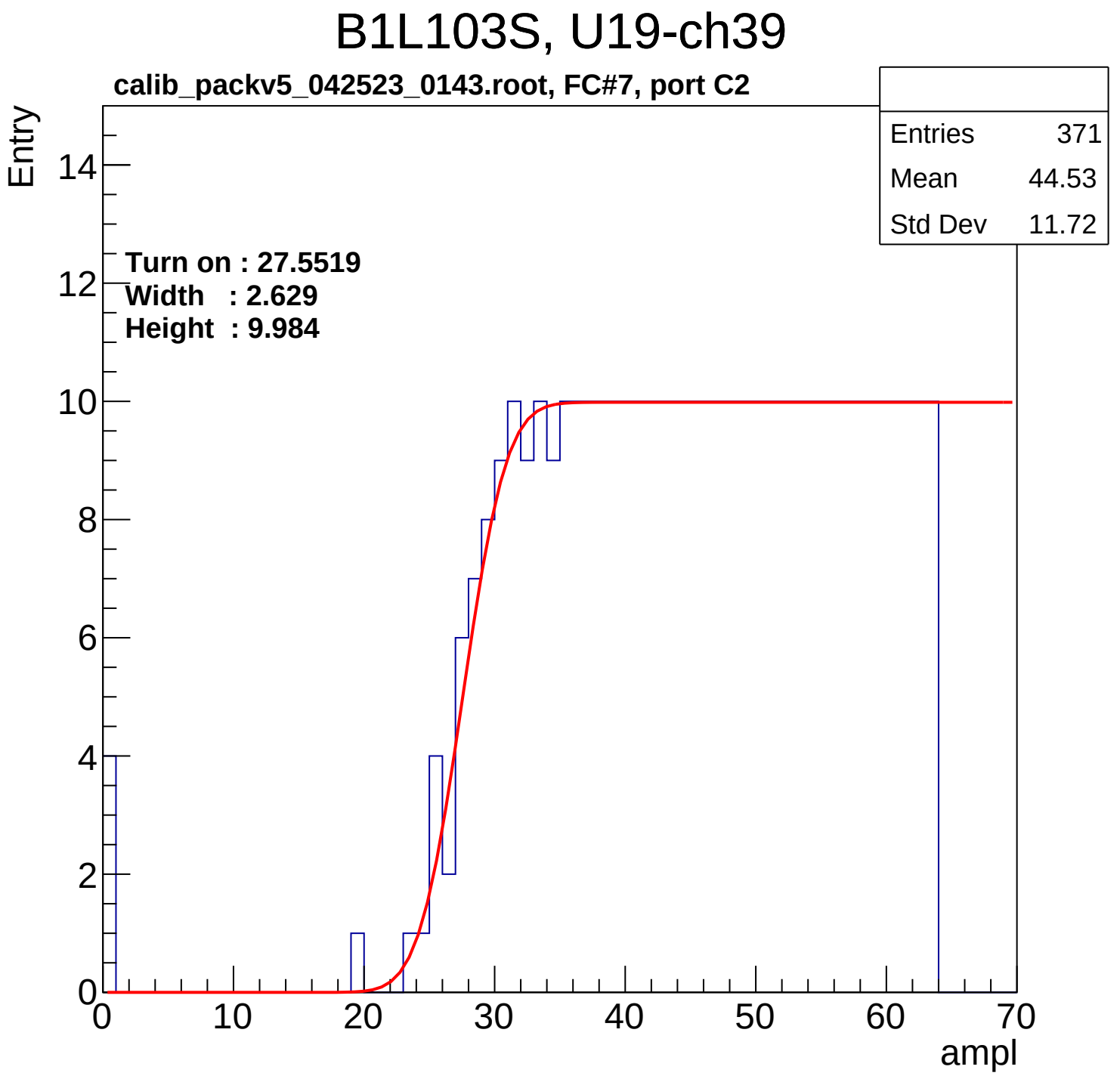
B1L103S, U19-ch39
calib_packv5_042523_0143.root, FC#7, port C2
Entries 371
Mean 44.53
Std Dev 11.72
Turn on : 27.5519
Width : 2.629
Height : 9.984
Entry
ampl
0
2
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6
8
10
12
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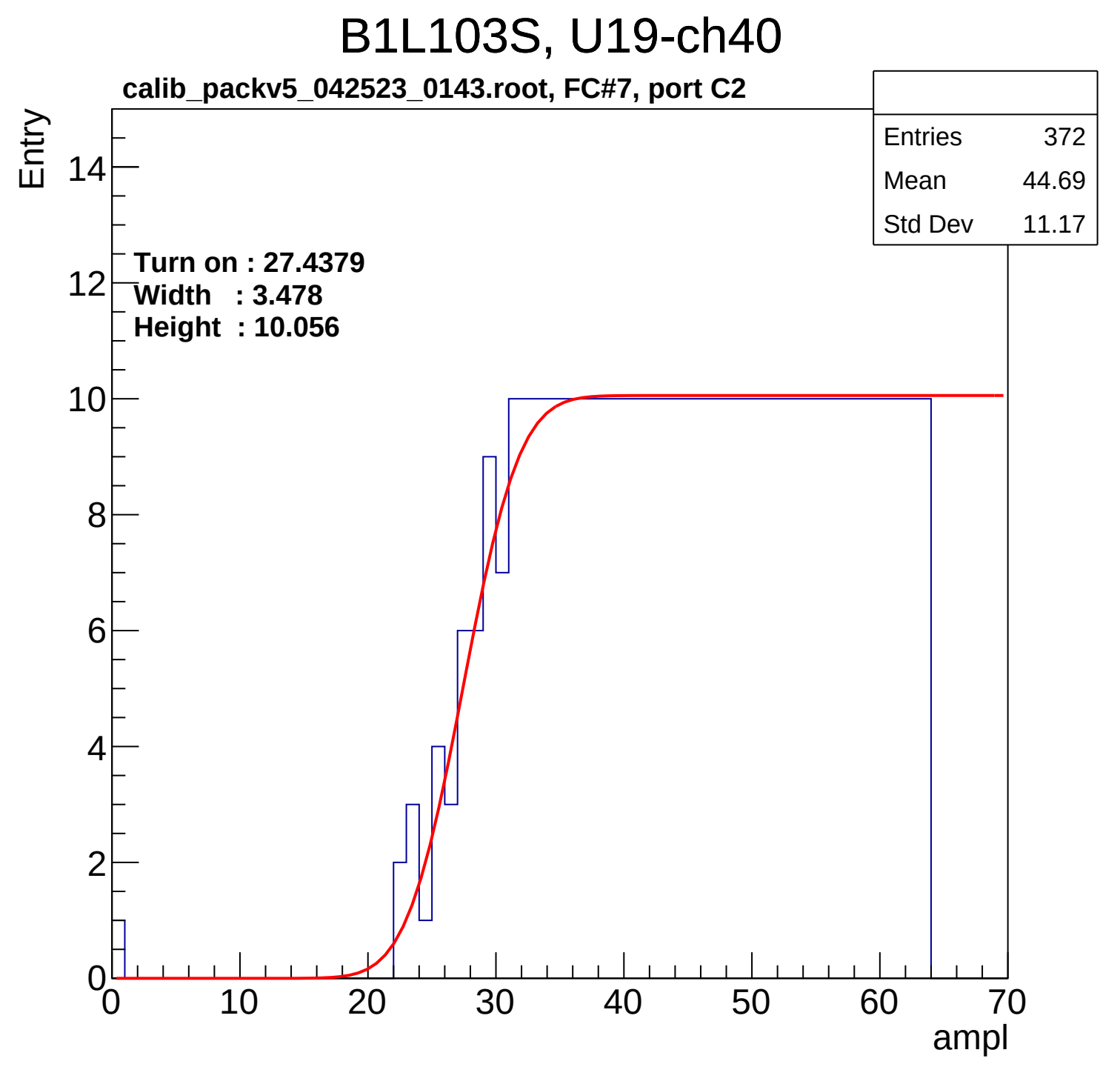
B1L103S, U19-ch40
calib_packv5_042523_0143.root, FC#7, port C2
Entries 372
Mean 44.69
Std Dev 11.17
Turn on : 27.4379
Width : 3.478
Height : 10.056
Entry
ampl
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8
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12
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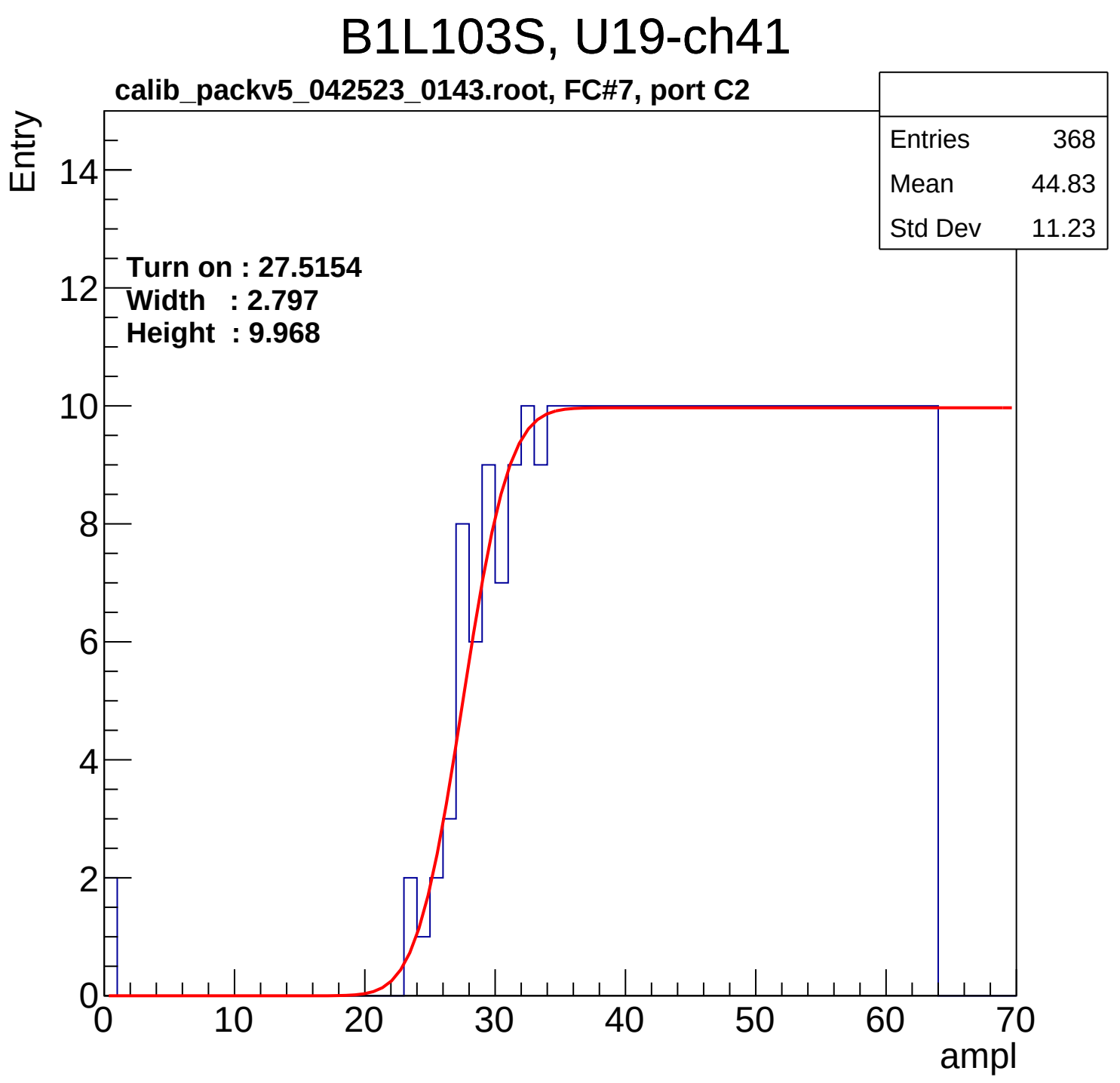
B1L103S, U19-ch41
calib_packv5_042523_0143.root, FC#7, port C2
Entries 368
Mean 44.83
Std Dev 11.23
Turn on : 27.5154
Width : 2.797
Height : 9.968
Entry
ampl
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6
8
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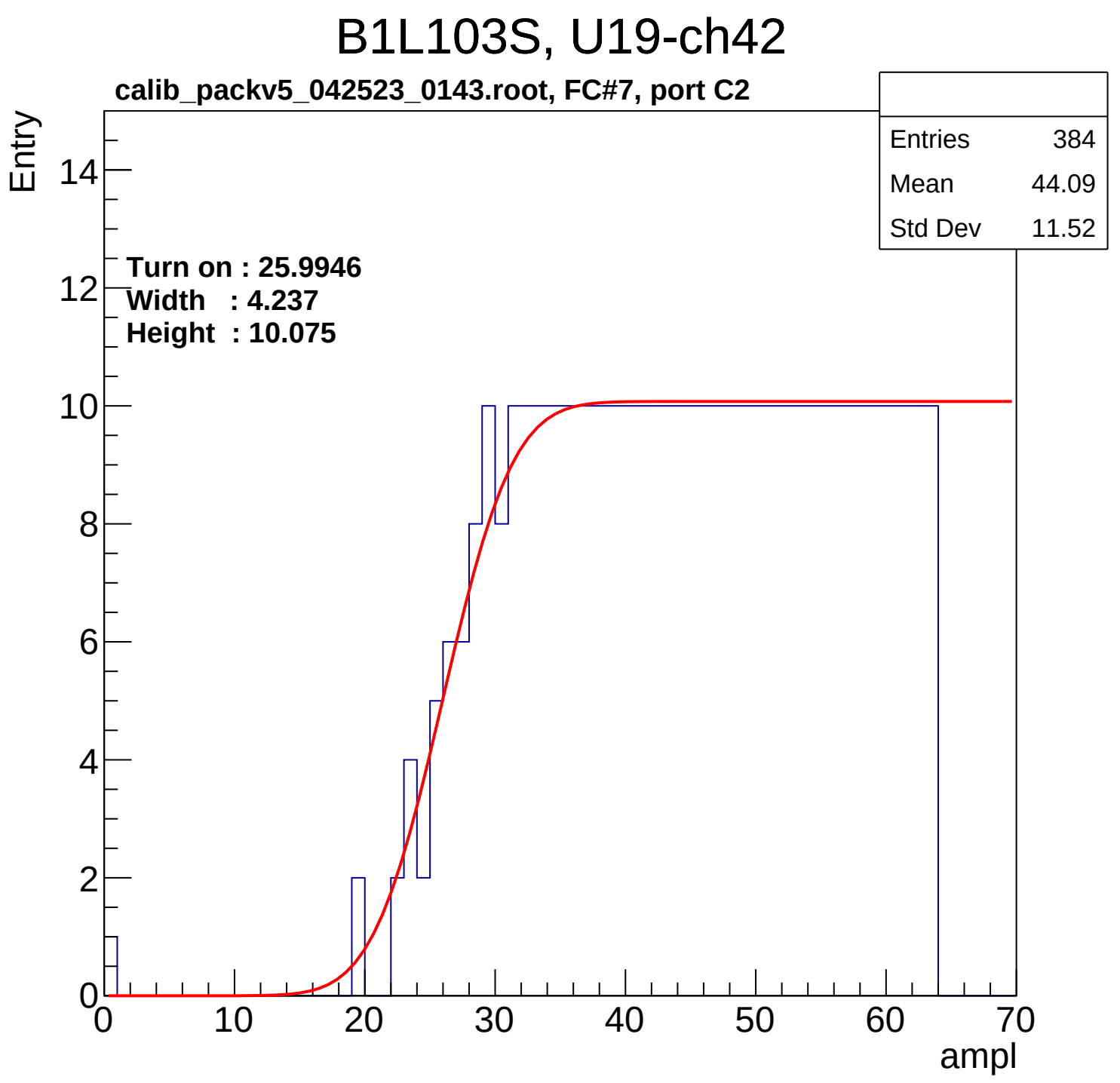
B1L103S, U19-ch42
calib_packv5_042523_0143.root, FC#7, port C2
Entries 384
Mean 44.09
Std Dev 11.52
Turn on : 25.9946
Width : 4.237
Height : 10.075
Entry
ampl
0
2
4
6
8
10
12
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0
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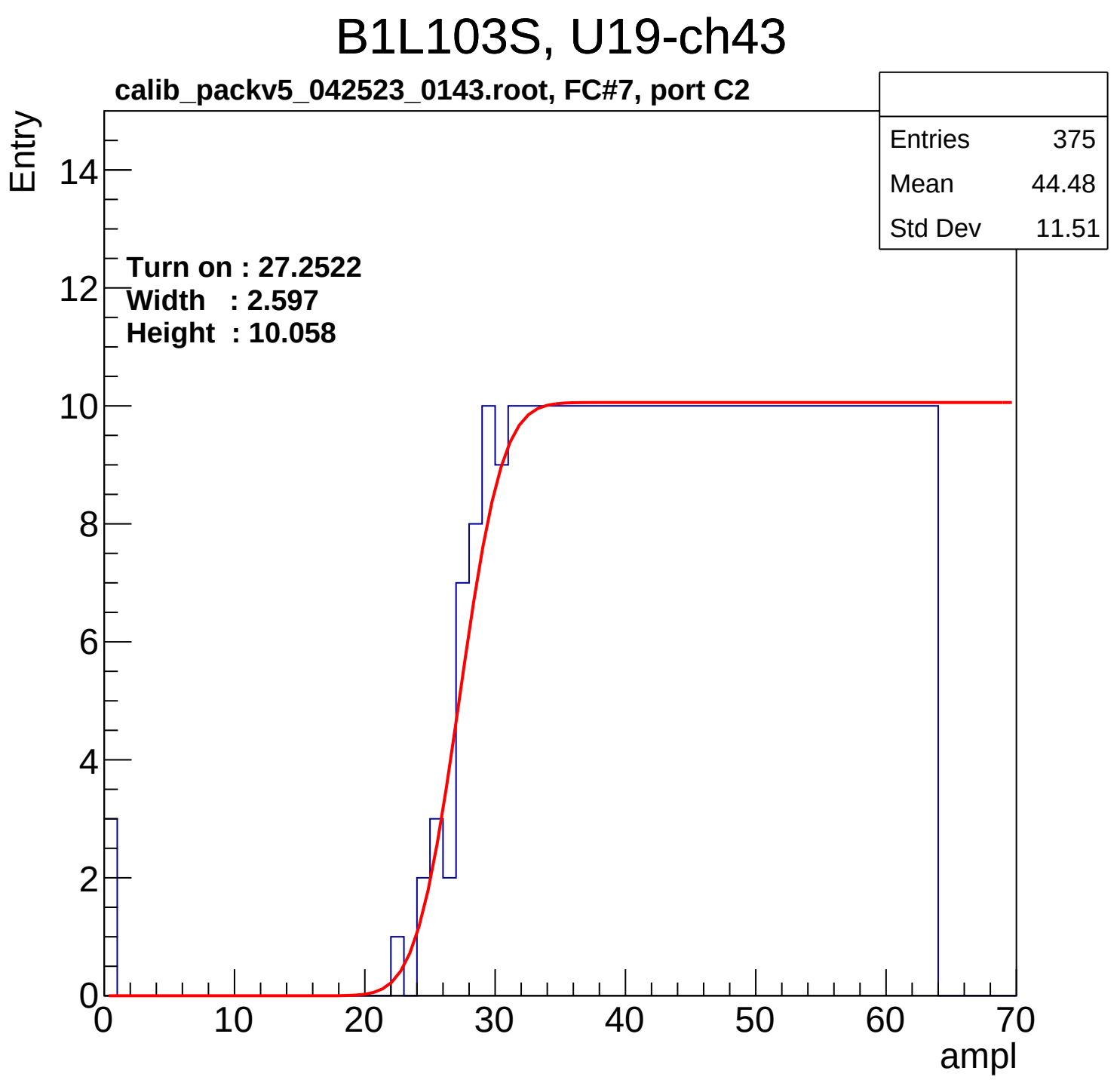
B1L103S, U19-ch43
calib_packv5_042523_0143.root, FC#7, port C2
Entries 375
Mean 44.48
Std Dev 11.51
Turn on : 27.2522
Width : 2.597
Height : 10.058
Entry
ampl
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6
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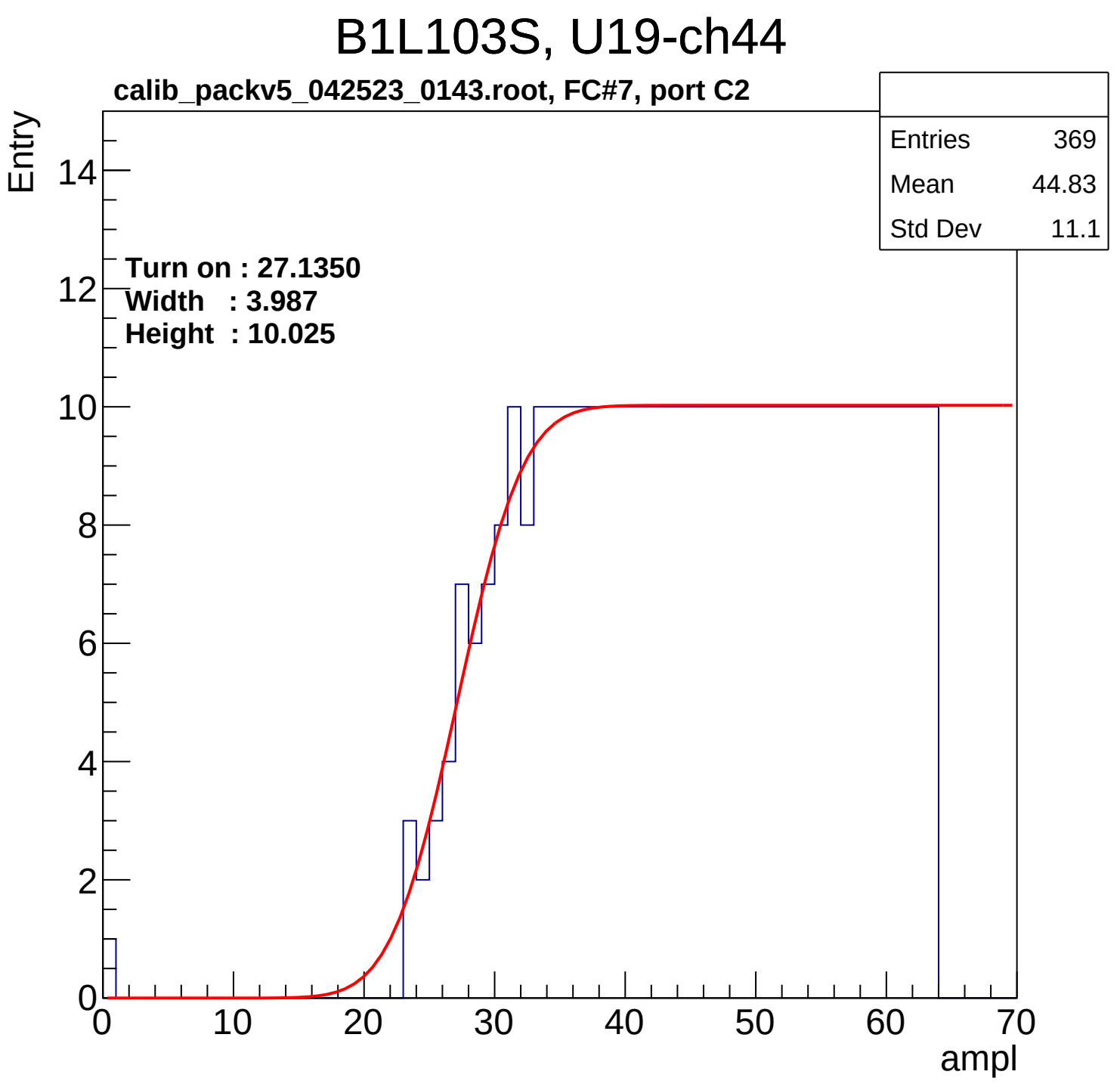
B1L103S, U19-ch44
calib_packv5_042523_0143.root, FC#7, port C2
Entries 369
Mean 44.83
Std Dev 11.1
Turn on : 27.1350
Width : 3.987
Height : 10.025
Entry
ampl
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6
8
10
12
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0
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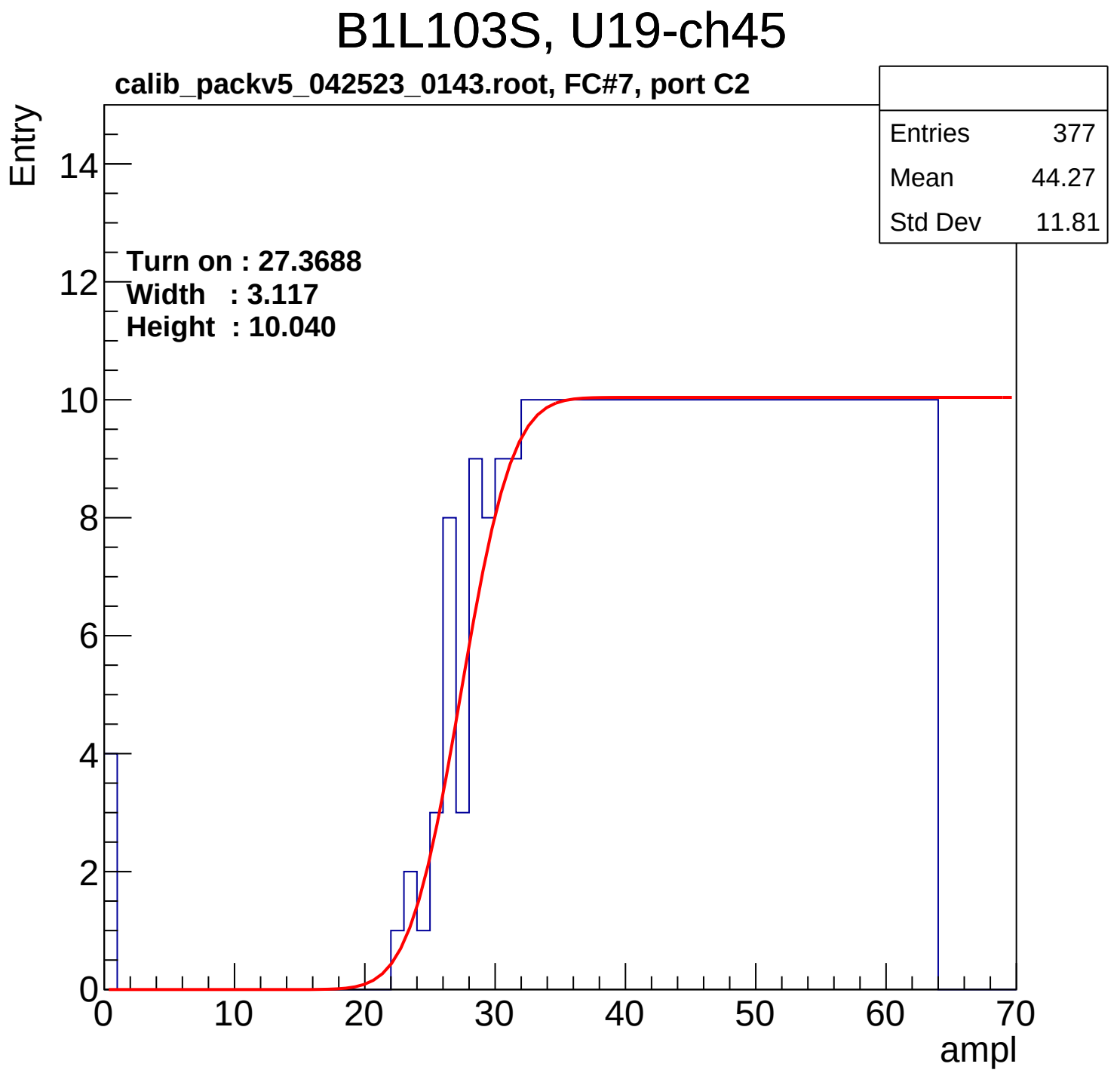
B1L103S, U19-ch45
calib_packv5_042523_0143.root, FC#7, port C2
Entries 377
Mean 44.27
Std Dev 11.81
Turn on : 27.3688
Width : 3.117
Height : 10.040
Entry
ampl
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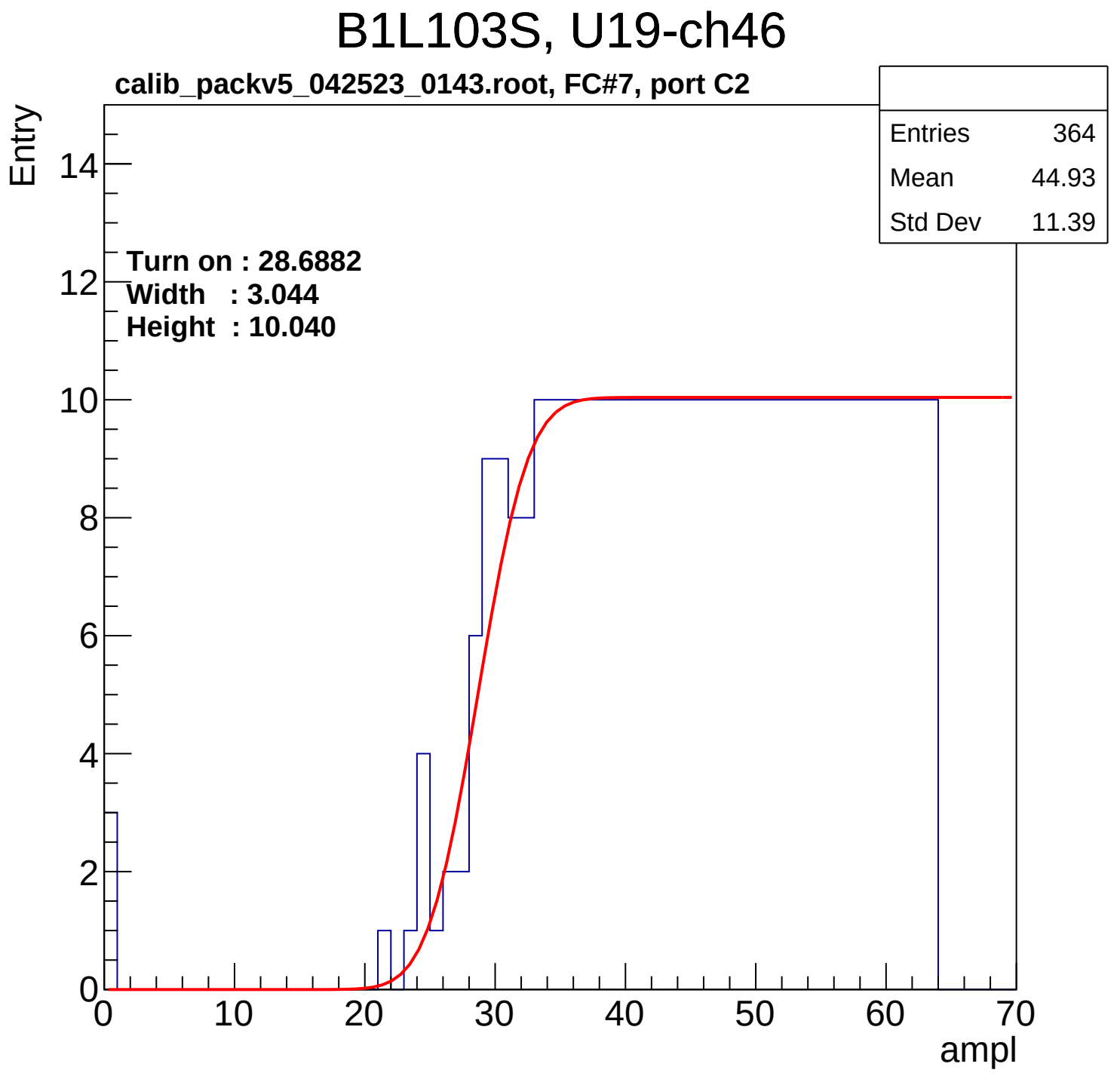
B1L103S, U19-ch46
calib_packv5_042523_0143.root, FC#7, port C2
Entries 364
Mean 44.93
Std Dev 11.39
Turn on : 28.6882
Width : 3.044
Height : 10.040
Entry
ampl
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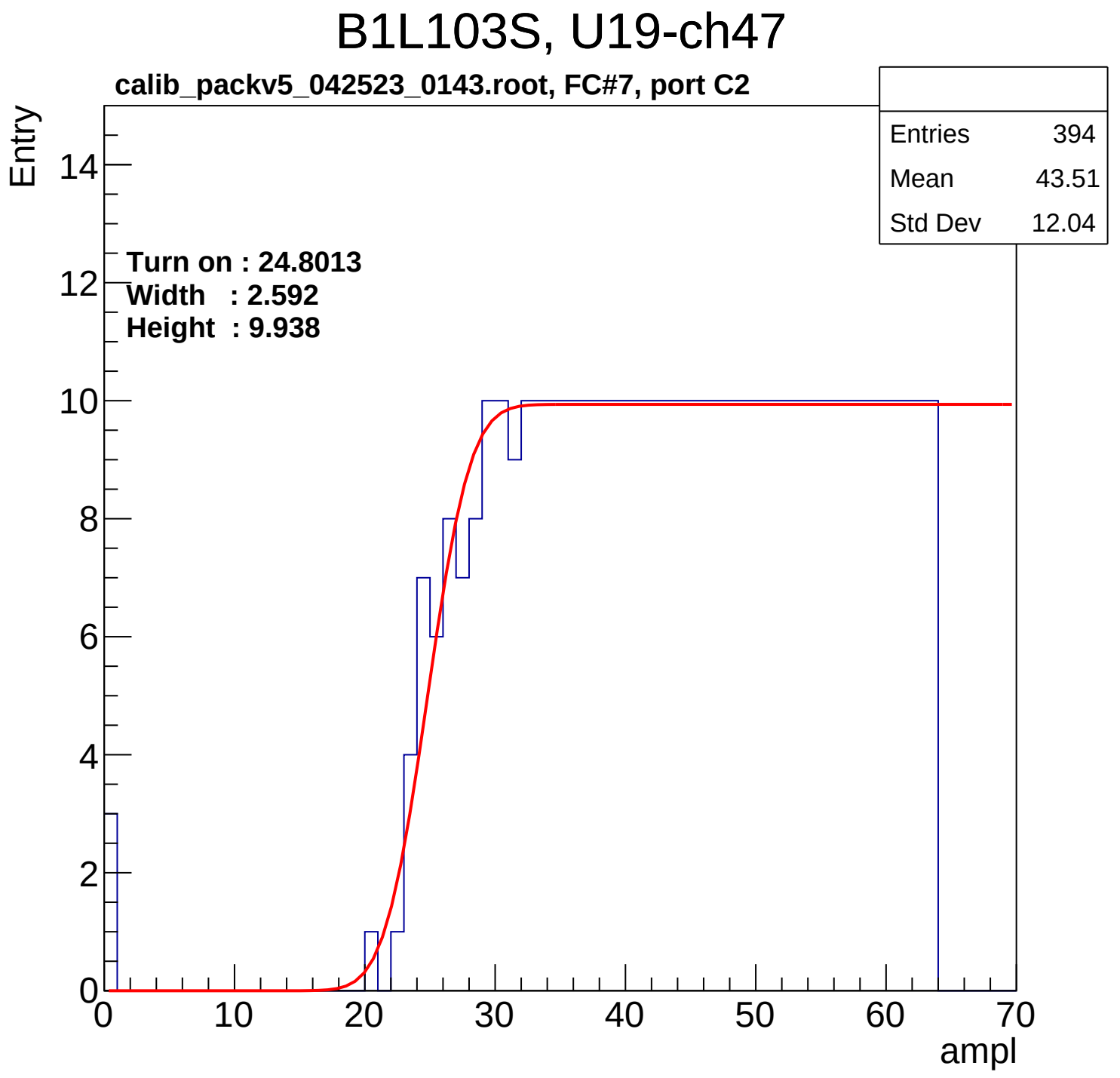
B1L103S, U19-ch47
calib_packv5_042523_0143.root, FC#7, port C2
Entries 394
Mean 43.51
Std Dev 12.04
Turn on : 24.8013
Width : 2.592
Height : 9.938
Entry
ampl
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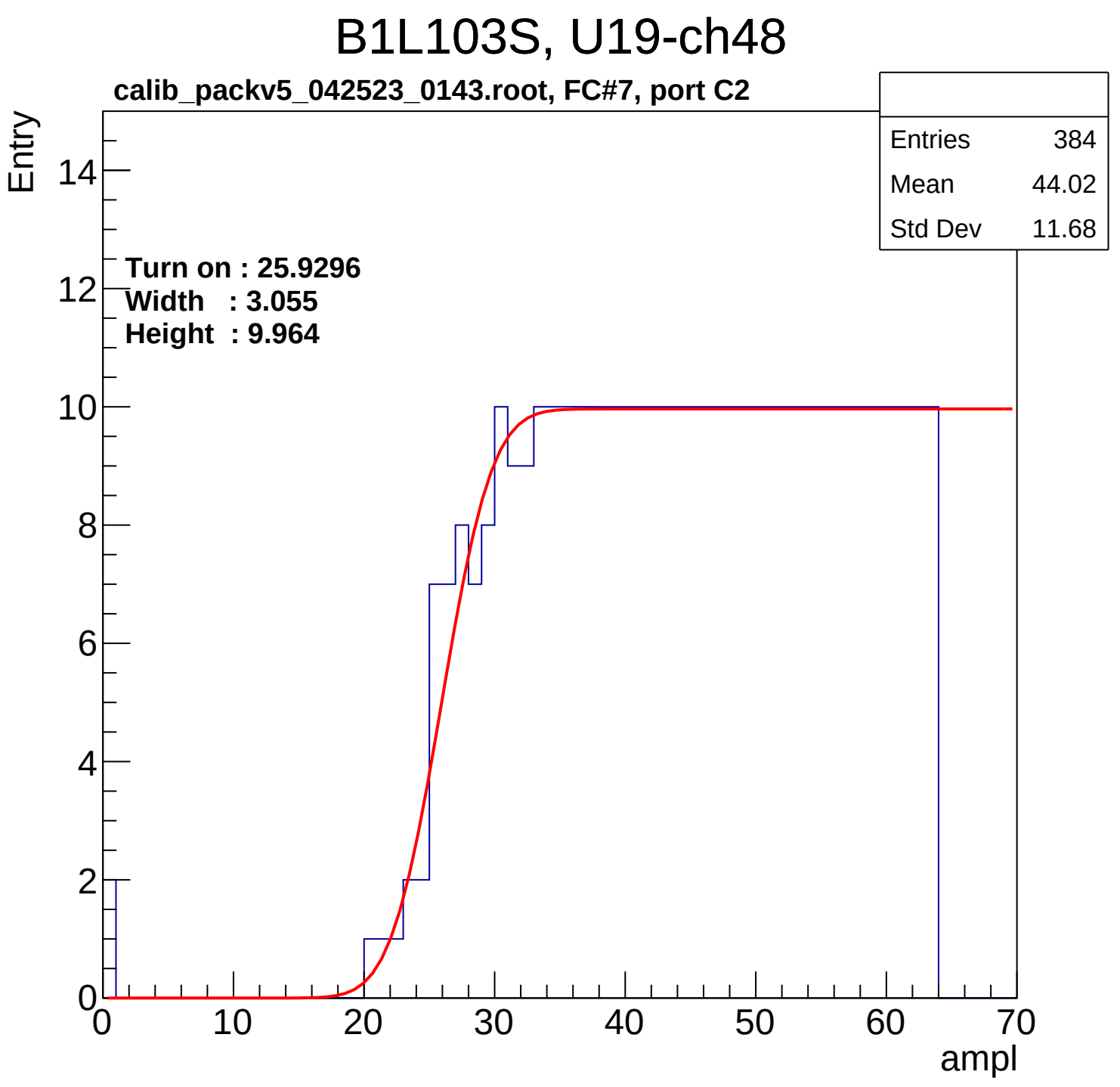
B1L103S, U19-ch48
calib_packv5_042523_0143.root, FC#7, port C2
Entries 384
Mean 44.02
Std Dev 11.68
Turn on : 25.9296
Width : 3.055
Height : 9.964
Entry
ampl
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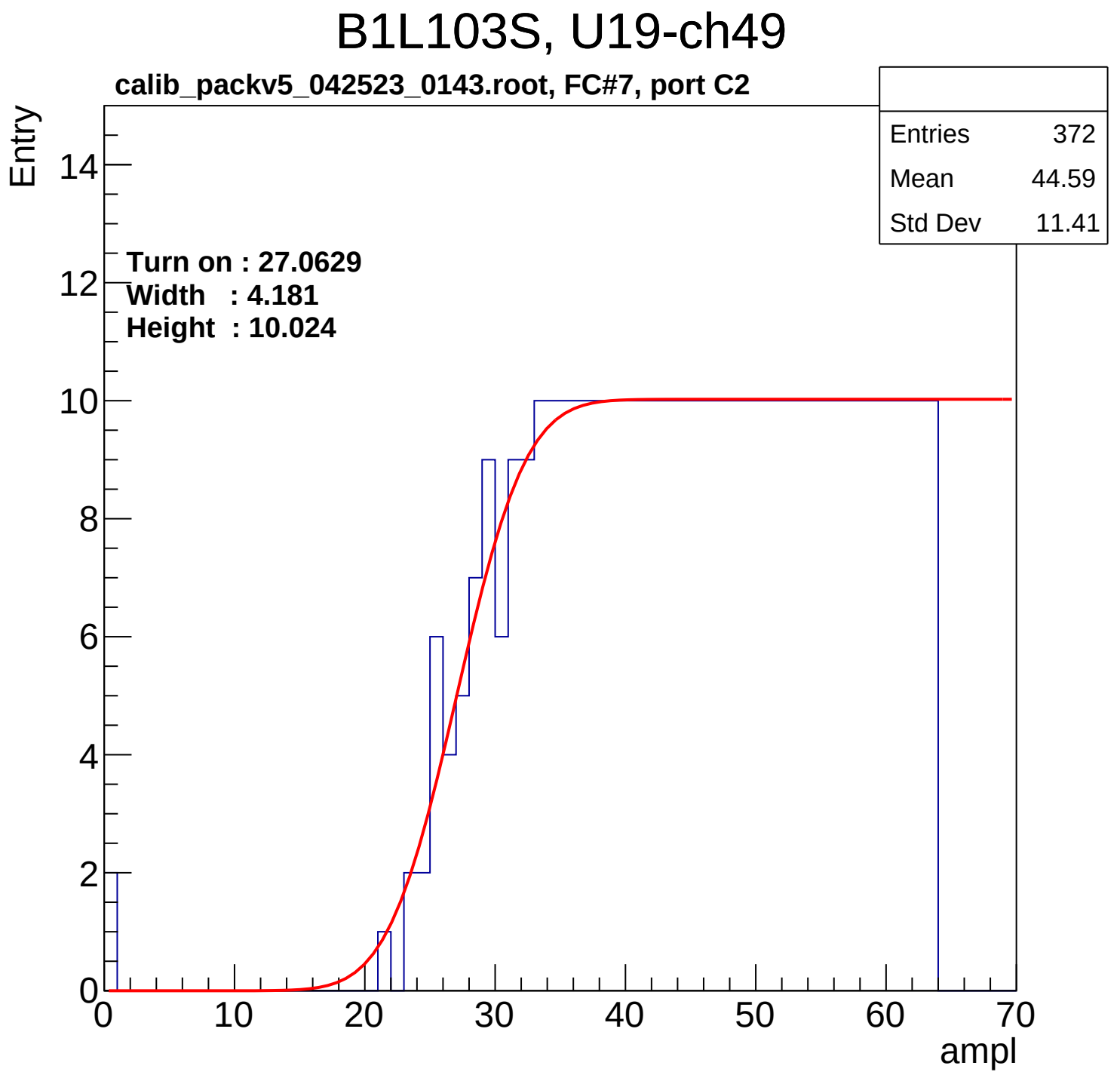
B1L103S, U19-ch49
calib_packv5_042523_0143.root, FC#7, port C2
Entries 372
Mean 44.59
Std Dev 11.41
Turn on : 27.0629
Width : 4.181
Height : 10.024
Entry
ampl
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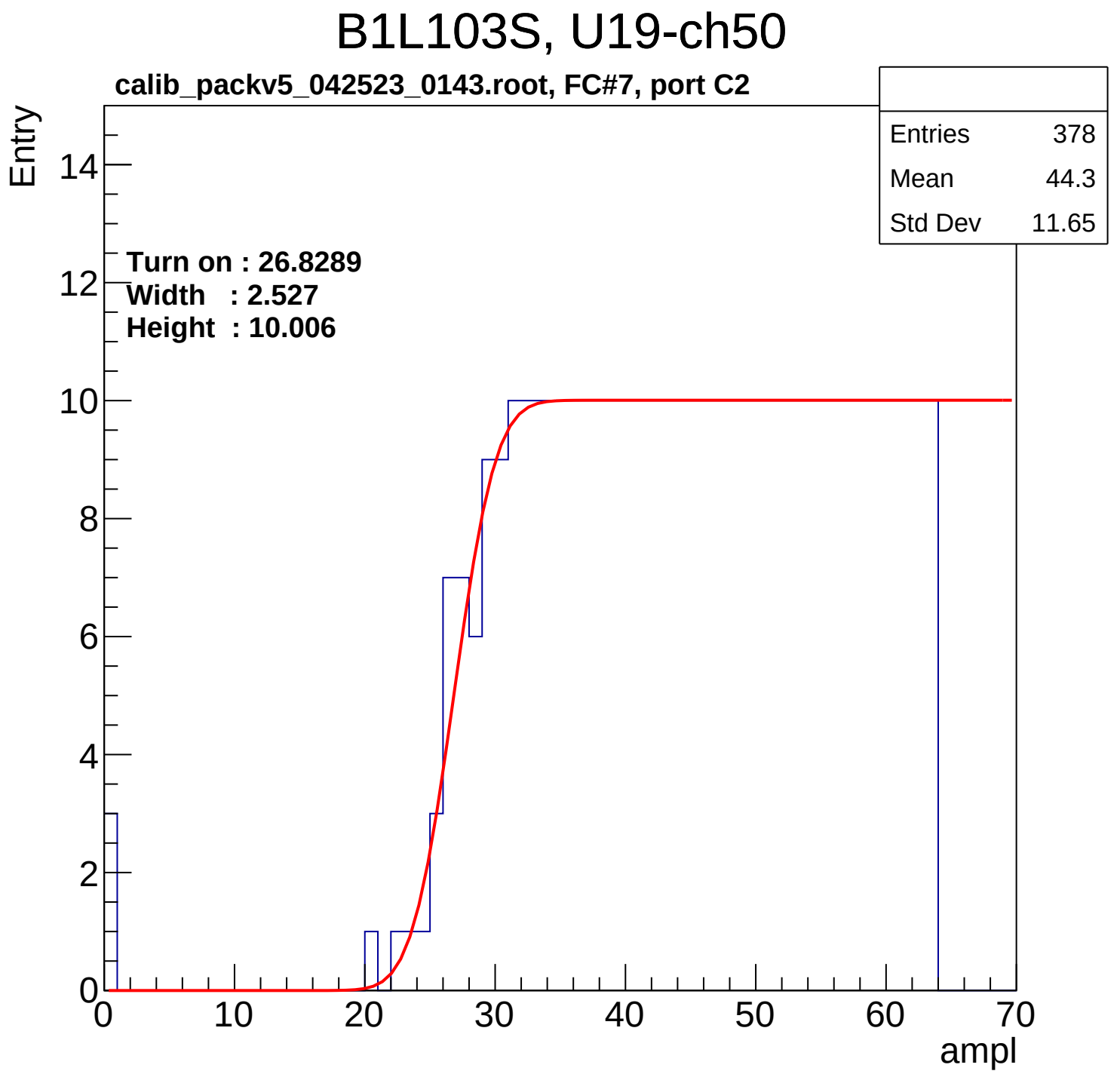
B1L103S, U19-ch50
calib_packv5_042523_0143.root, FC#7, port C2
Entries 378
Mean 44.3
Std Dev 11.65
Turn on : 26.8289
Width : 2.527
Height : 10.006
Entry
ampl
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8
10
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60
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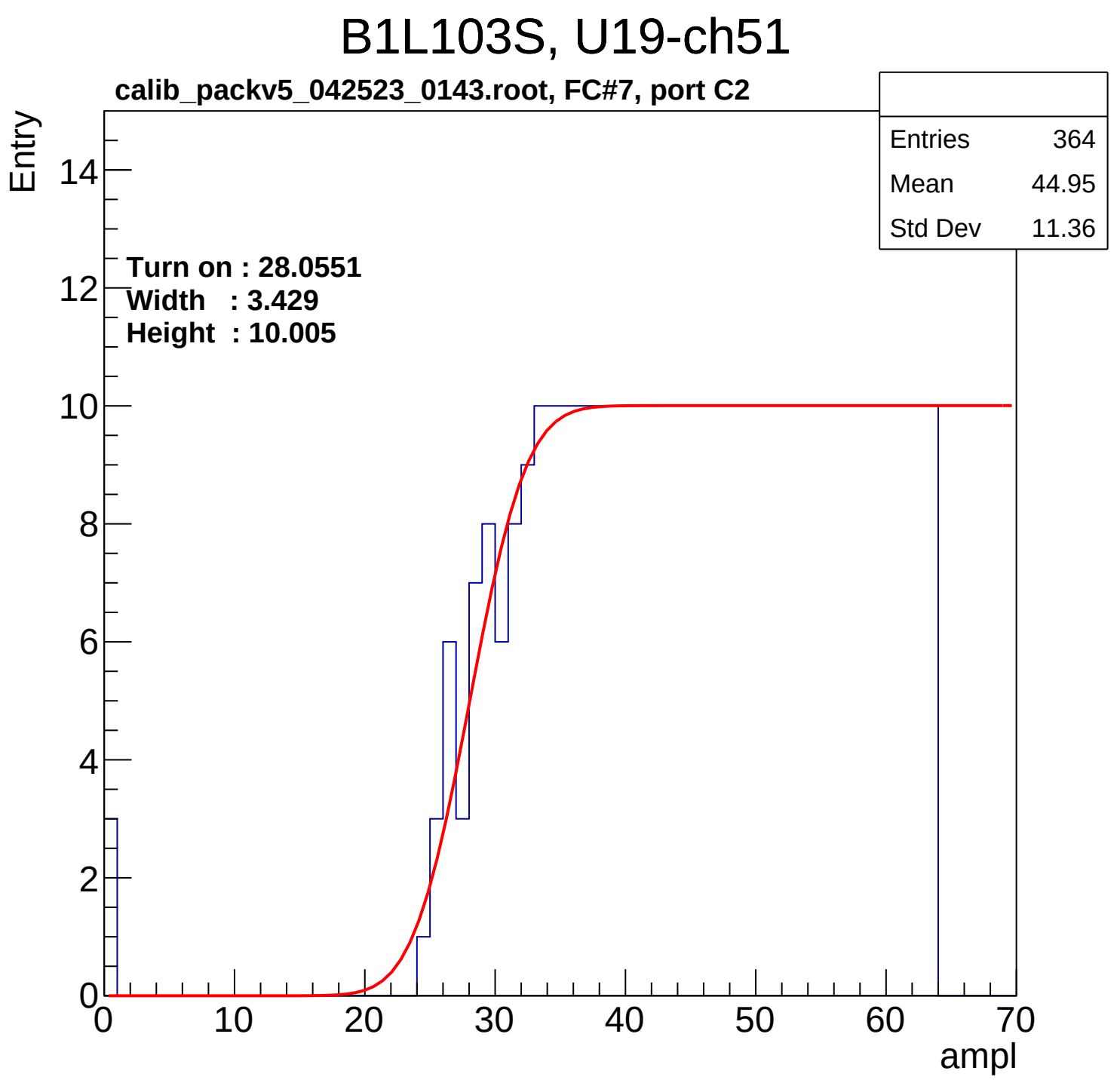
B1L103S, U19-ch51
calib_packv5_042523_0143.root, FC#7, port C2
Entries 364
Mean 44.95
Std Dev 11.36
Turn on : 28.0551
Width : 3.429
Height : 10.005
Entry
ampl
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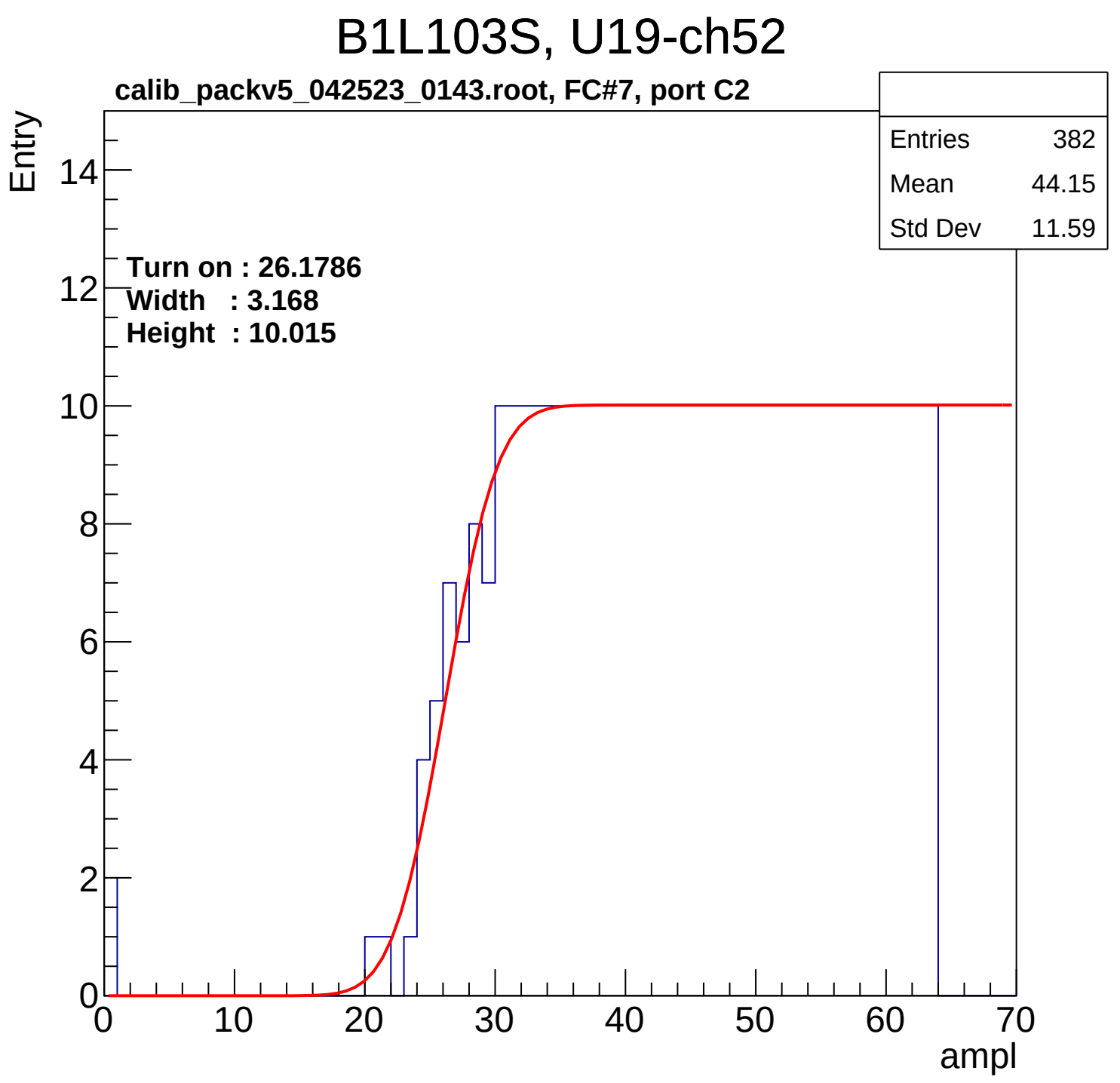
B1L103S, U19-ch52
calib_packv5_042523_0143.root, FC#7, port C2
Entries 382
Mean 44.15
Std Dev 11.59
Turn on : 26.1786
Width : 3.168
Height : 10.015
Entry
ampl
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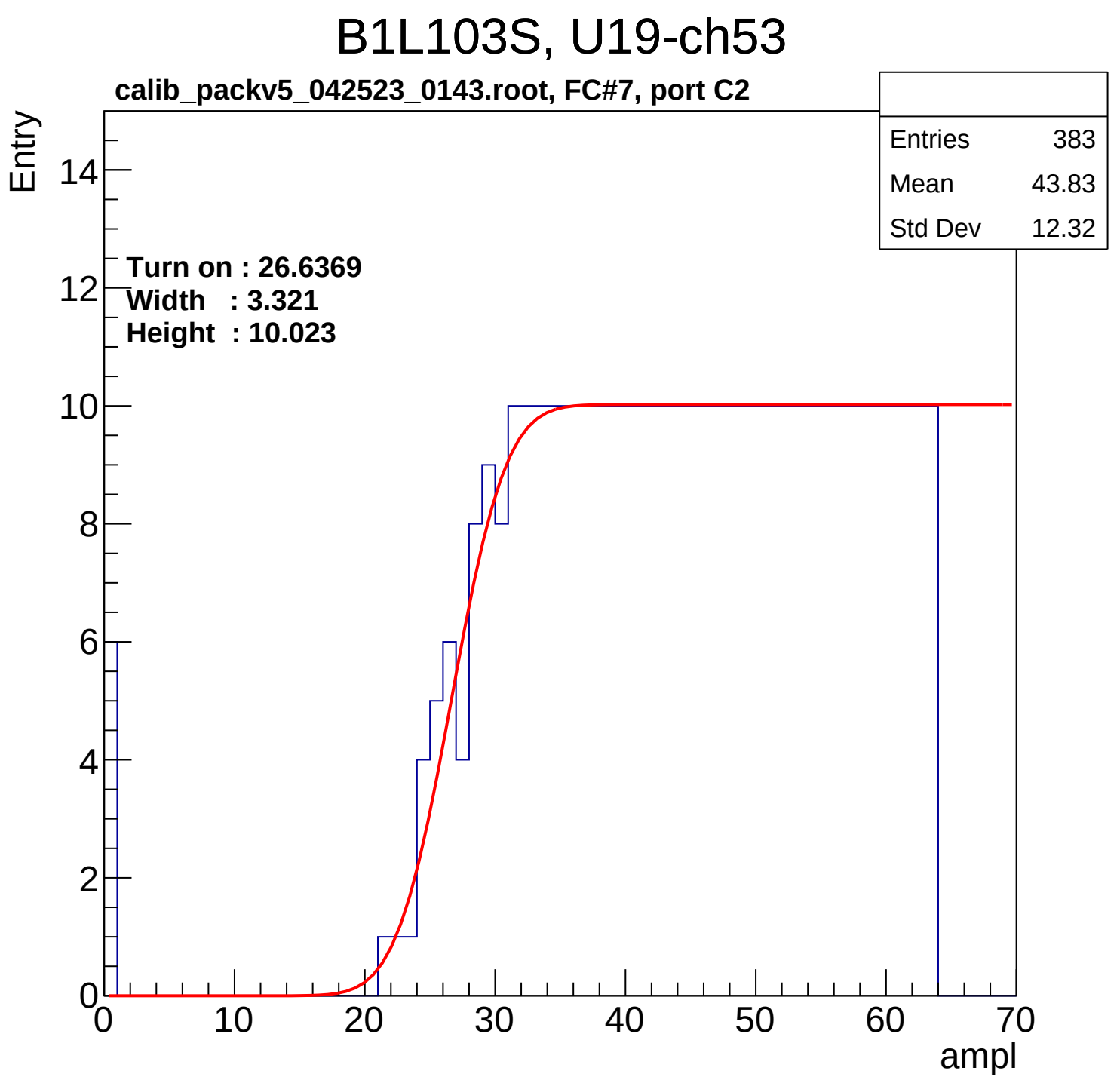
B1L103S, U19-ch53
calib_packv5_042523_0143.root, FC#7, port C2
Entries 383
Mean 43.83
Std Dev 12.32
Turn on : 26.6369
Width : 3.321
Height : 10.023
Entry
ampl
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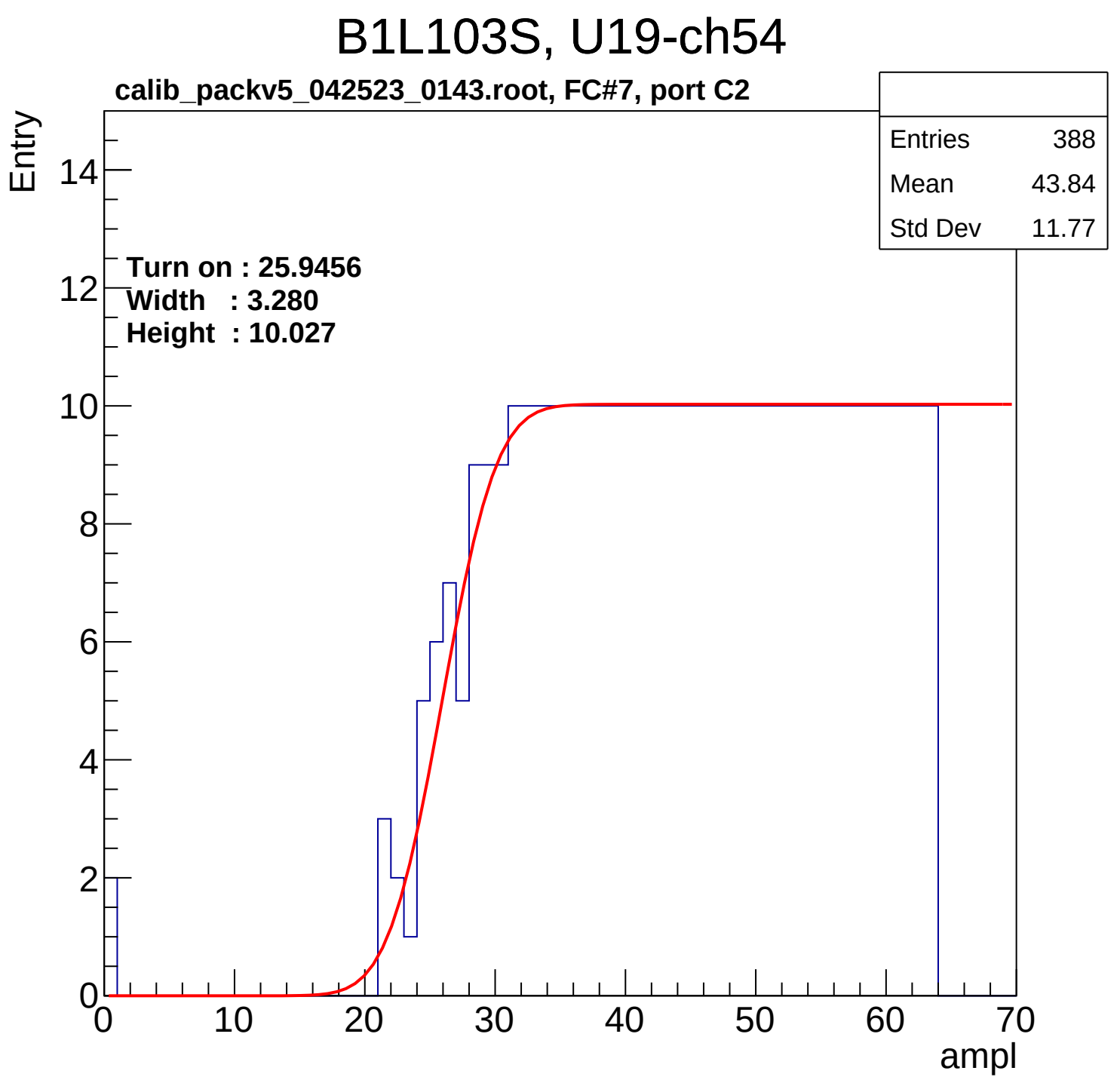
B1L103S, U19-ch54
calib_packv5_042523_0143.root, FC#7, port C2
Entries 388
Mean 43.84
Std Dev 11.77
Turn on : 25.9456
Width : 3.280
Height : 10.027
Entry
ampl
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4
6
8
10
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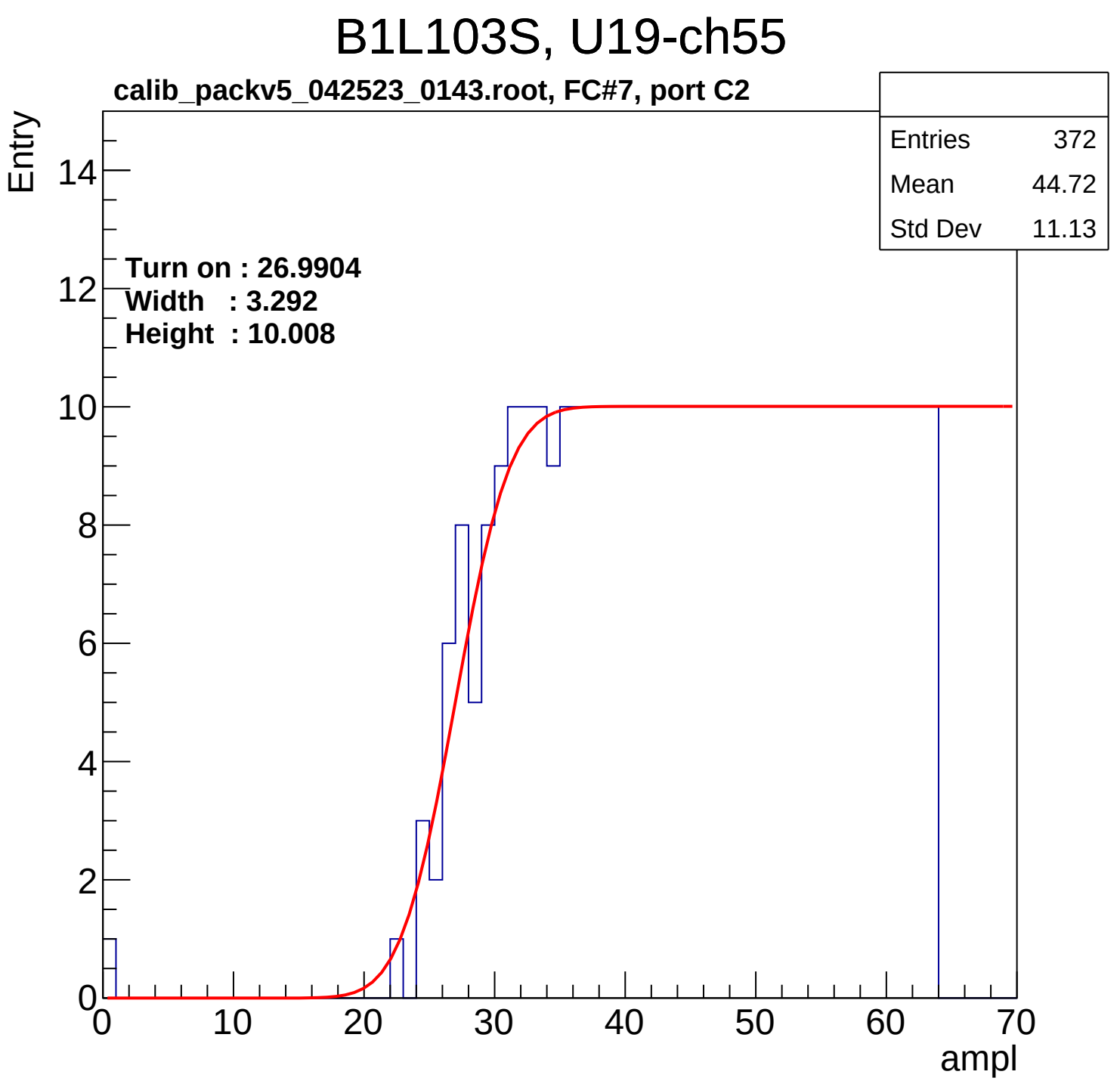
B1L103S, U19-ch55
calib_packv5_042523_0143.root, FC#7, port C2
Entries 372
Mean 44.72
Std Dev 11.13
Turn on : 26.9904
Width : 3.292
Height : 10.008
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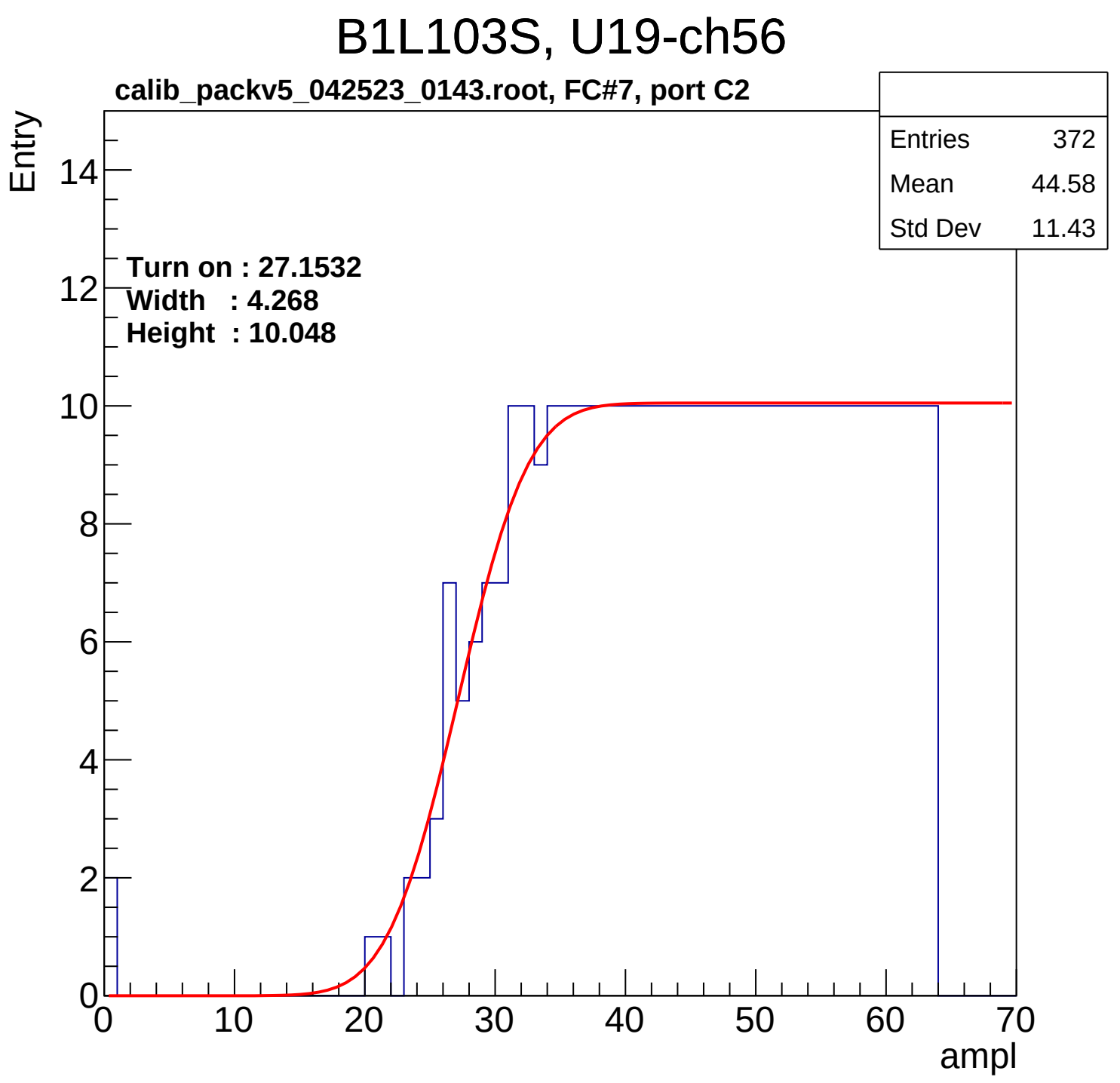
B1L103S, U19-ch56
calib_packv5_042523_0143.root, FC#7, port C2
Entries 372
Mean 44.58
Std Dev 11.43
Turn on : 27.1532
Width : 4.268
Height : 10.048
Entry
ampl
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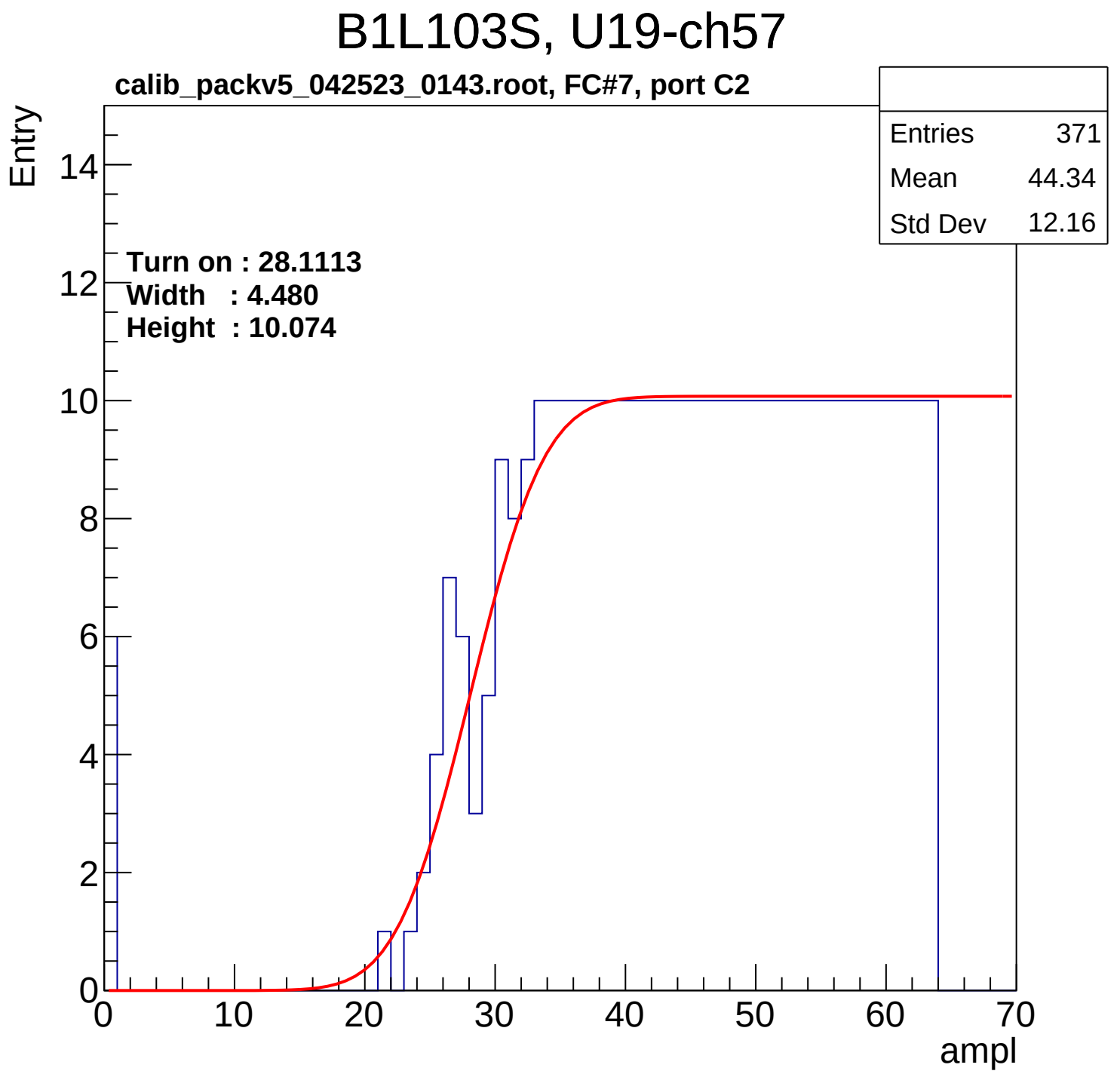
B1L103S, U19-ch57
calib_packv5_042523_0143.root, FC#7, port C2
Entries 371
Mean 44.34
Std Dev 12.16
Turn on : 28.1113
Width : 4.480
Height : 10.074
Entry
ampl
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20
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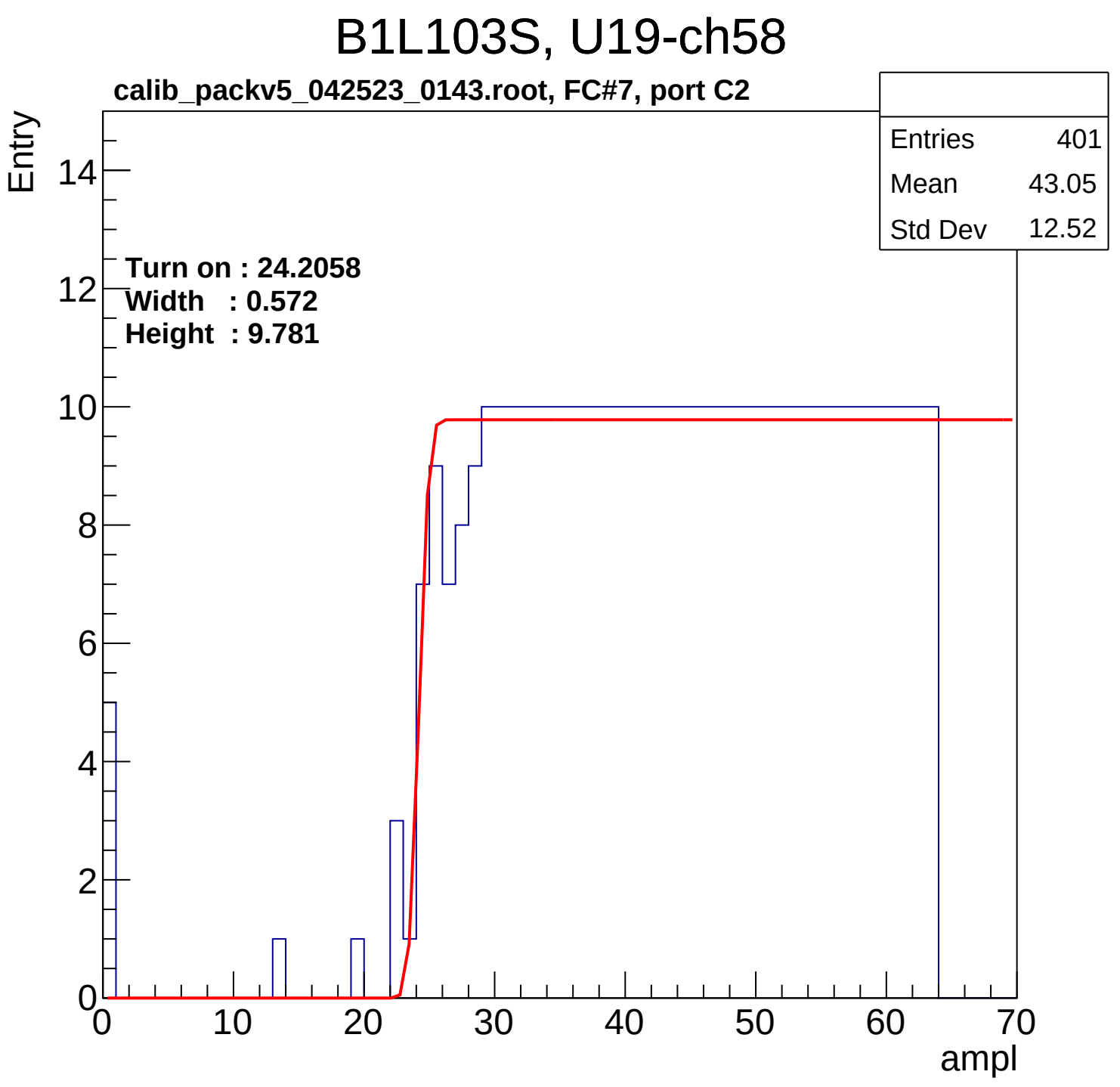
B1L103S, U19-ch58
calib_packv5_042523_0143.root, FC#7, port C2
Entries 401
Mean 43.05
Std Dev 12.52
Turn on : 24.2058
Width : 0.572
Height : 9.781
Entry
ampl
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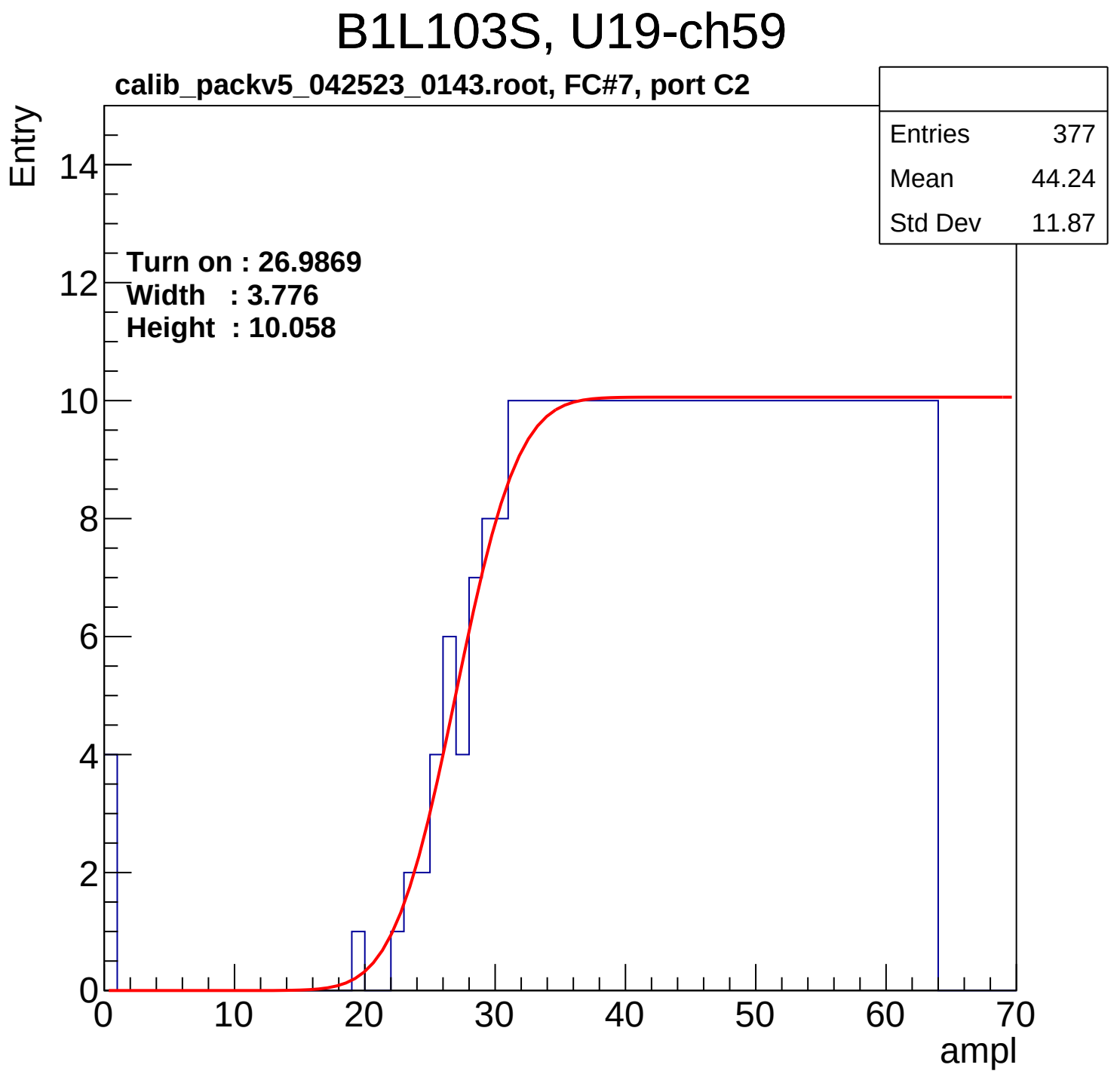
B1L103S, U19-ch59
calib_packv5_042523_0143.root, FC#7, port C2
Entries 377
Mean 44.24
Std Dev 11.87
Turn on : 26.9869
Width : 3.776
Height : 10.058
Entry
ampl
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2
4
6
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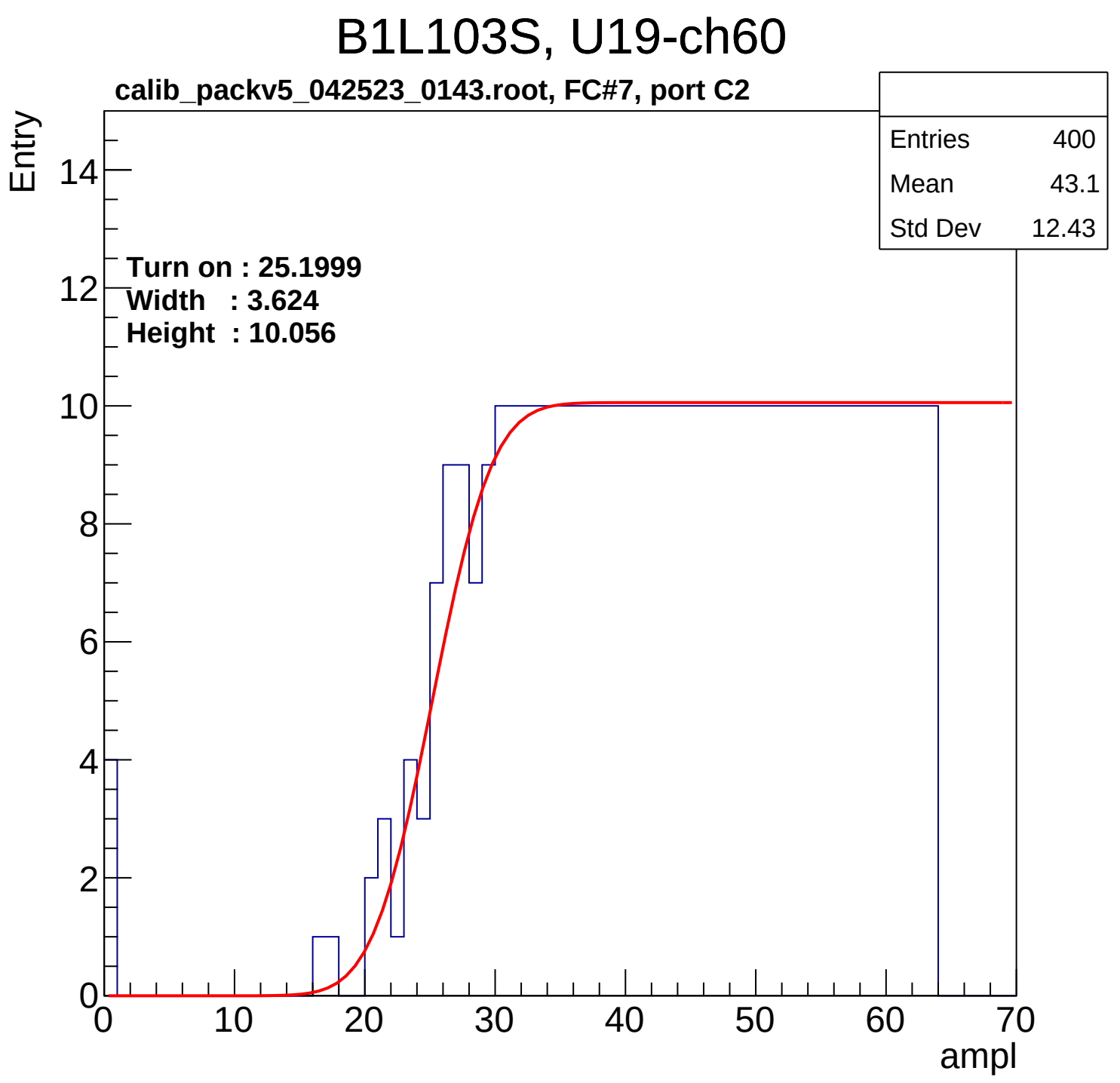
B1L103S, U19-ch60
calib_packv5_042523_0143.root, FC#7, port C2
Entries 400
Mean 43.1
Std Dev 12.43
Turn on : 25.1999
Width : 3.624
Height : 10.056
Entry
ampl
0
2
4
6
8
10
12
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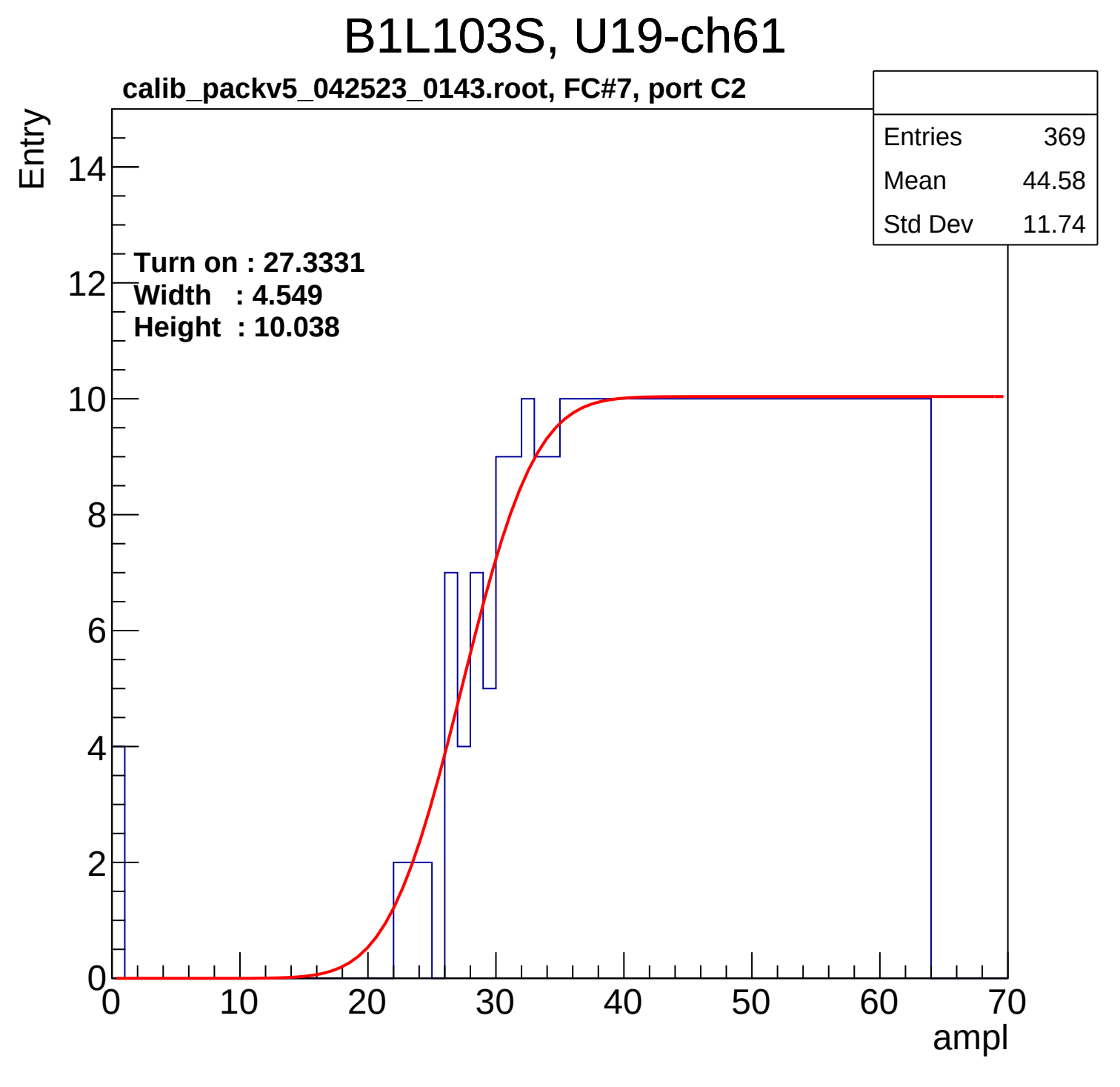
B1L103S, U19-ch61
calib_packv5_042523_0143.root, FC#7, port C2
Entries 369
Mean 44.58
Std Dev 11.74
Turn on : 27.3331
Width : 4.549
Height : 10.038
Entry
ampl
0
2
4
6
8
10
12
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0
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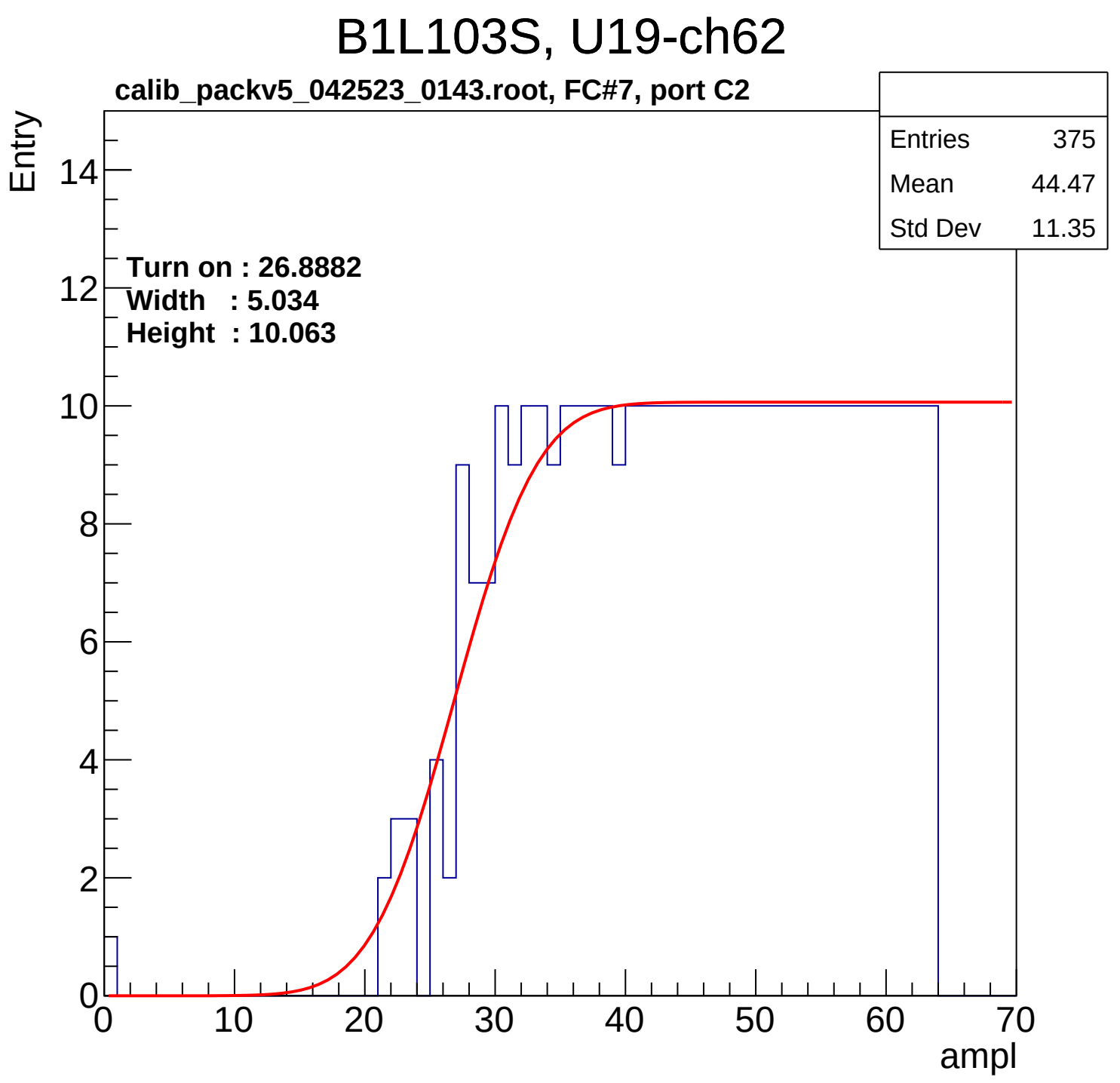
B1L103S, U19-ch62
calib_packv5_042523_0143.root, FC#7, port C2
Entries 375
Mean 44.47
Std Dev 11.35
Turn on : 26.8882
Width : 5.034
Height : 10.063
Entry
ampl
0
2
4
6
8
10
12
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0
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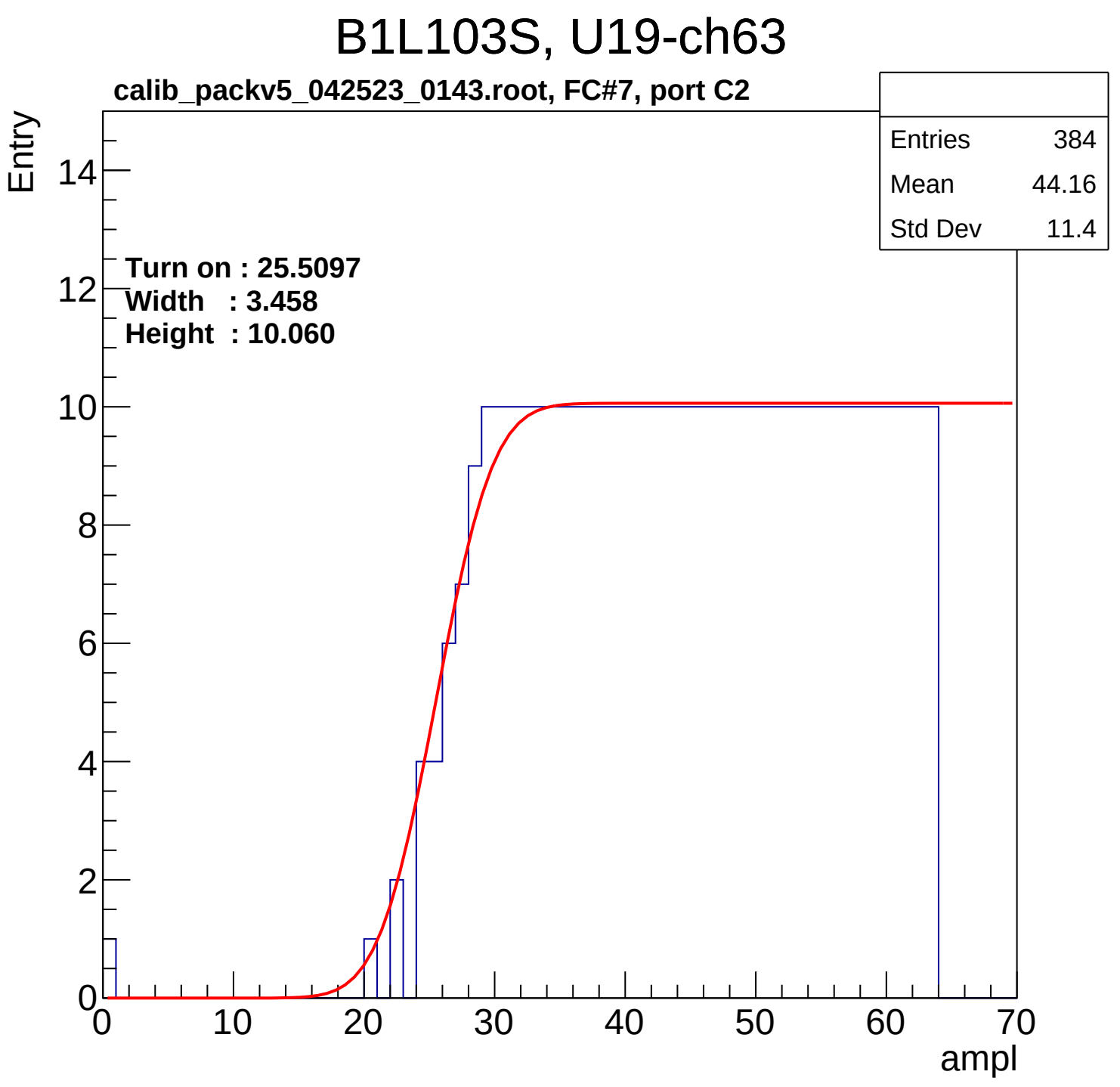
B1L103S, U19-ch63
calib_packv5_042523_0143.root, FC#7, port C2
Entries 384
Mean 44.16
Std Dev 11.4
Turn on : 25.5097
Width : 3.458
Height : 10.060
Entry
ampl
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4
6
8
10
12
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0
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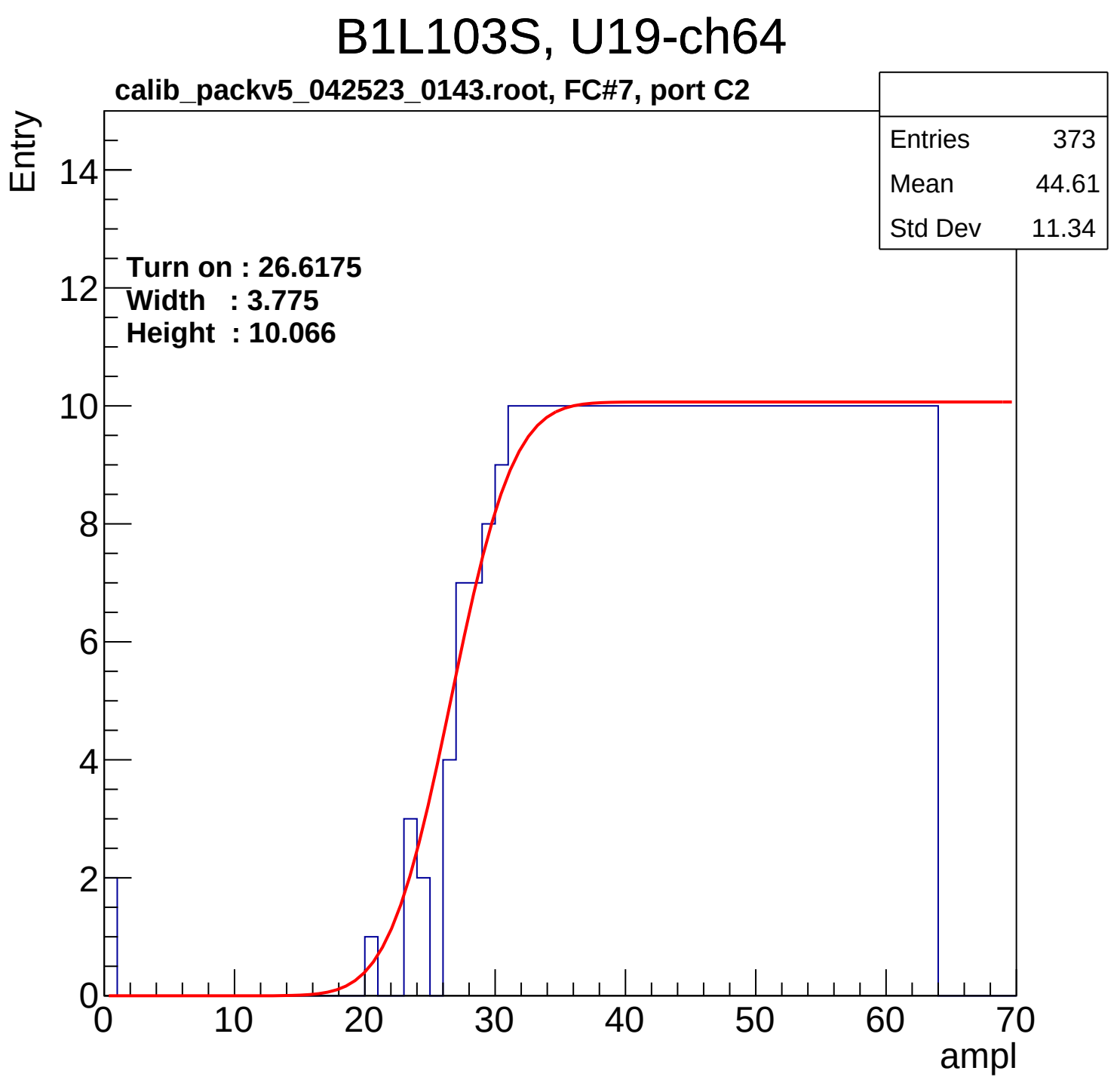
B1L103S, U19-ch64
calib_packv5_042523_0143.root, FC#7, port C2
Entries 373
Mean 44.61
Std Dev 11.34
Turn on : 26.6175
Width : 3.775
Height : 10.066
Entry
ampl
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4
6
8
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12
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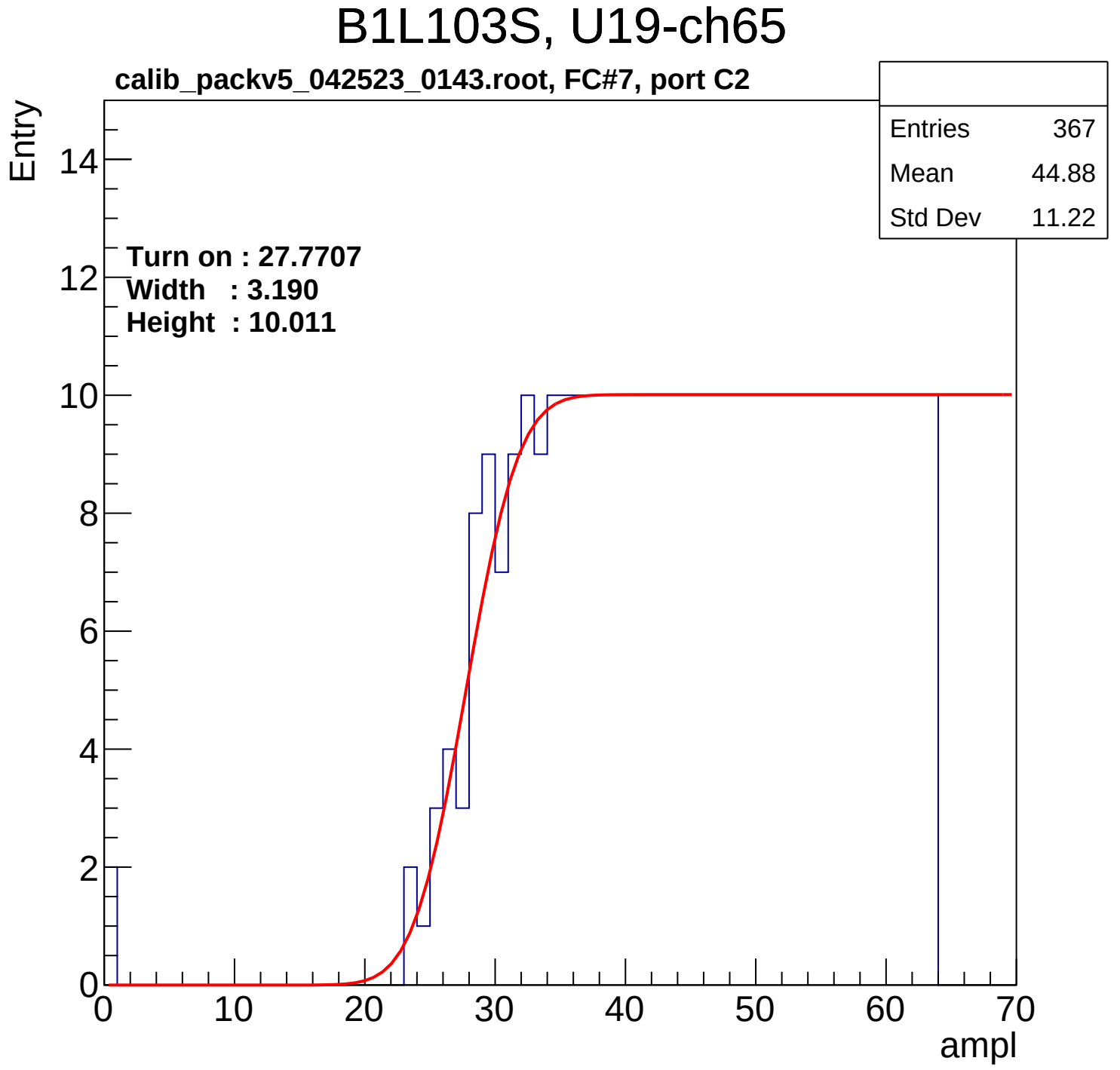
B1L103S, U19-ch65
calib_packv5_042523_0143.root, FC#7, port C2
Entries 367
Mean 44.88
Std Dev 11.22
Turn on : 27.7707
Width : 3.190
Height : 10.011
Entry
ampl
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4
6
8
10
12
14
0
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60
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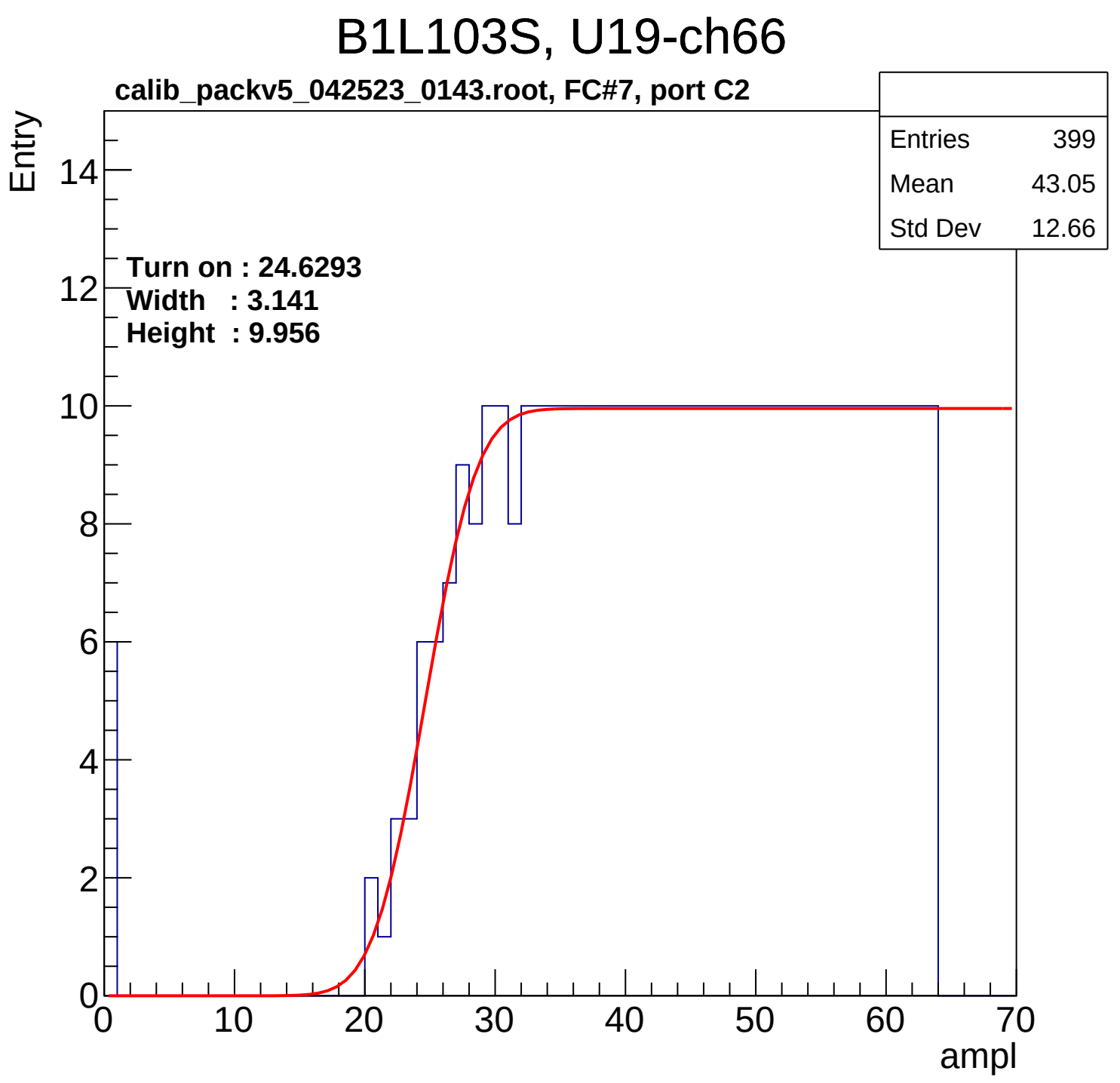
B1L103S, U19-ch66
calib_packv5_042523_0143.root, FC#7, port C2
Entries 399
Mean 43.05
Std Dev 12.66
Turn on : 24.6293
Width : 3.141
Height : 9.956
Entry
ampl
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6
8
10
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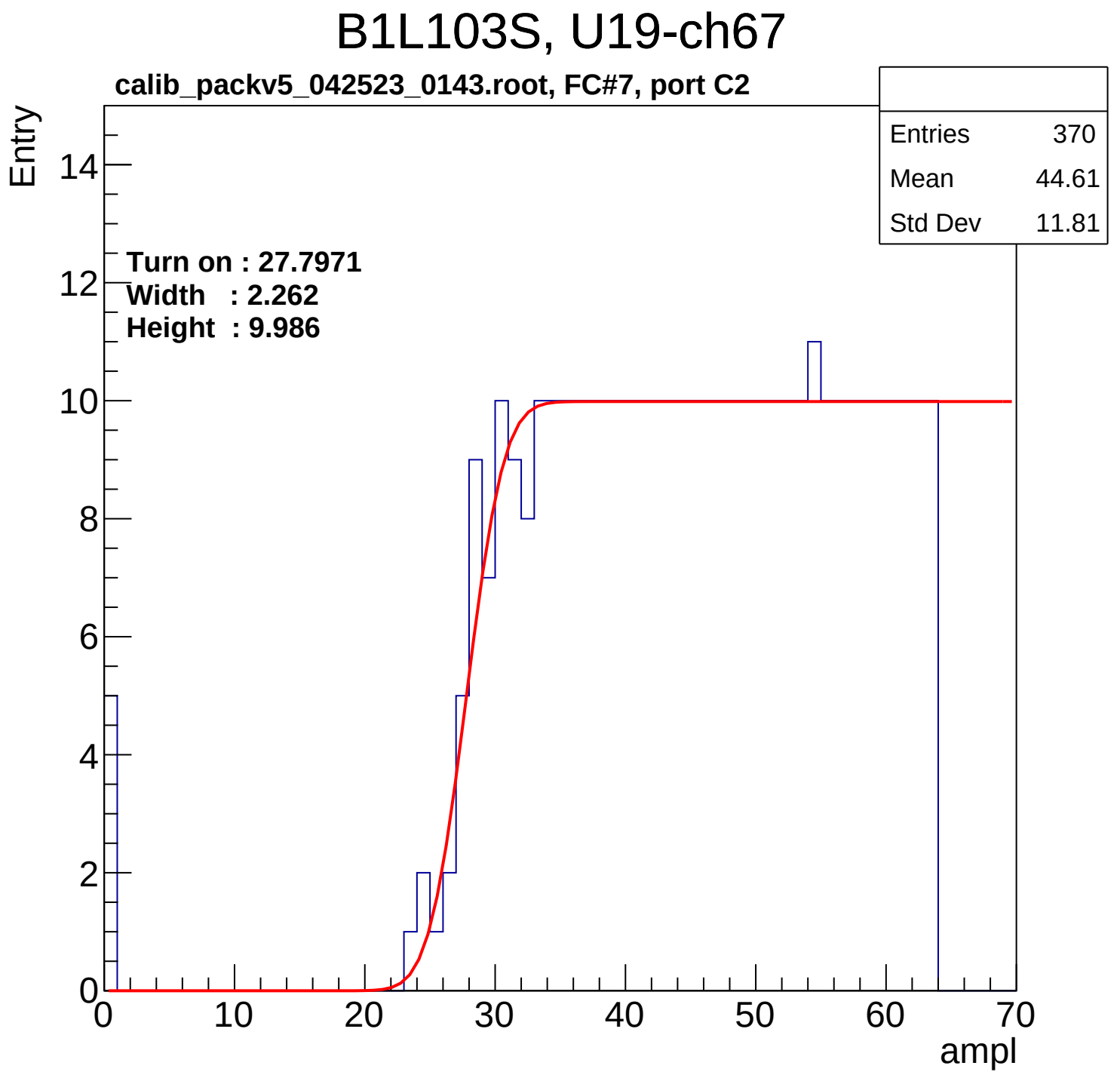
B1L103S, U19-ch67
calib_packv5_042523_0143.root, FC#7, port C2
Entries 370
Mean 44.61
Std Dev 11.81
Turn on : 27.7971
Width : 2.262
Height : 9.986
Entry
ampl
0
2
4
6
8
10
12
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0
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60
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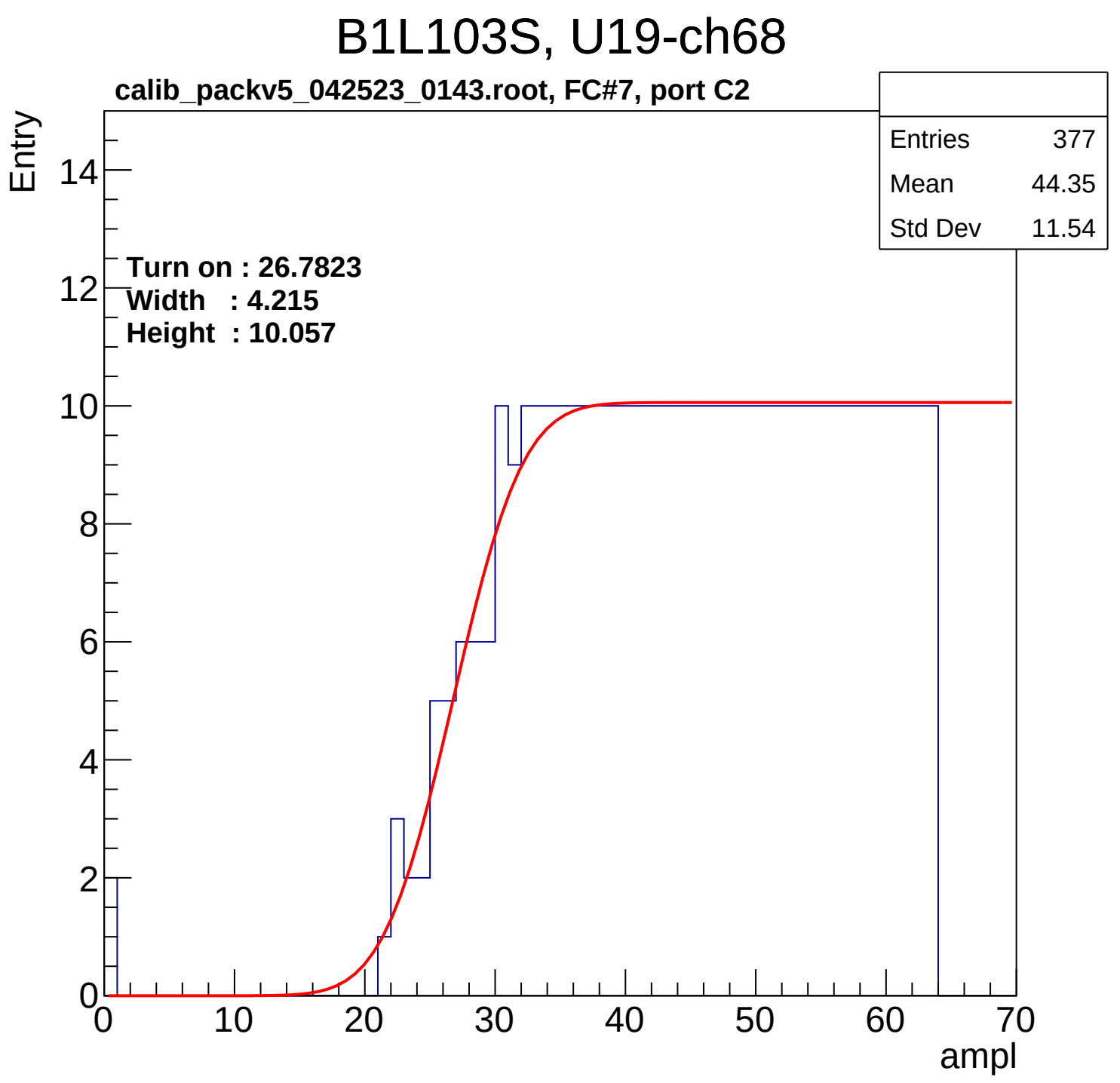
B1L103S, U19-ch68
calib_packv5_042523_0143.root, FC#7, port C2
Entries 377
Mean 44.35
Std Dev 11.54
Turn on : 26.7823
Width : 4.215
Height : 10.057
Entry
ampl
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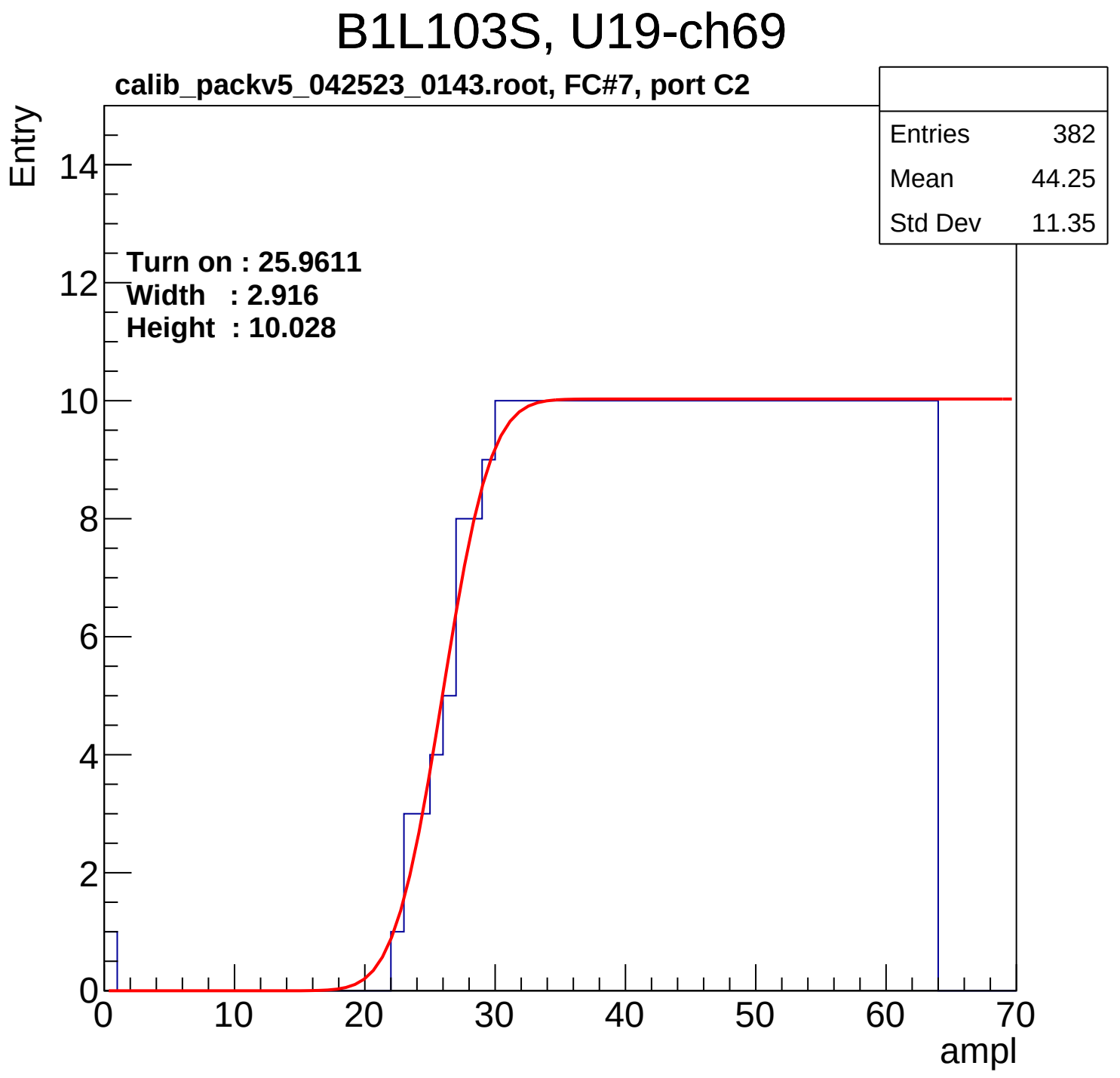
B1L103S, U19-ch69
calib_packv5_042523_0143.root, FC#7, port C2
Entries 382
Mean 44.25
Std Dev 11.35
Turn on : 25.9611
Width : 2.916
Height : 10.028
Entry
ampl
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2
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6
8
10
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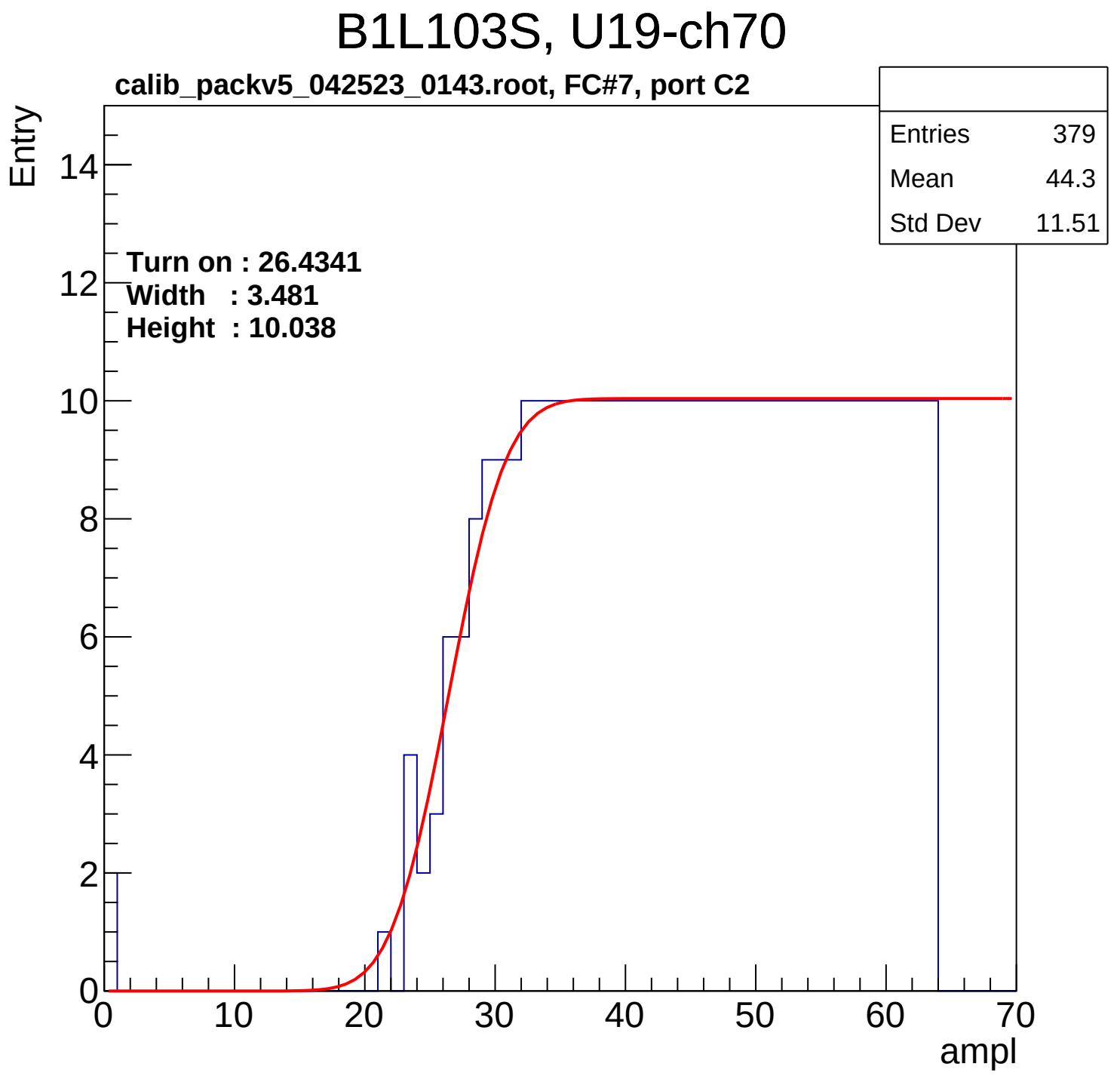
B1L103S, U19-ch70
calib_packv5_042523_0143.root, FC#7, port C2
Entries 379
Mean 44.3
Std Dev 11.51
Turn on : 26.4341
Width : 3.481
Height : 10.038
Entry
ampl
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6
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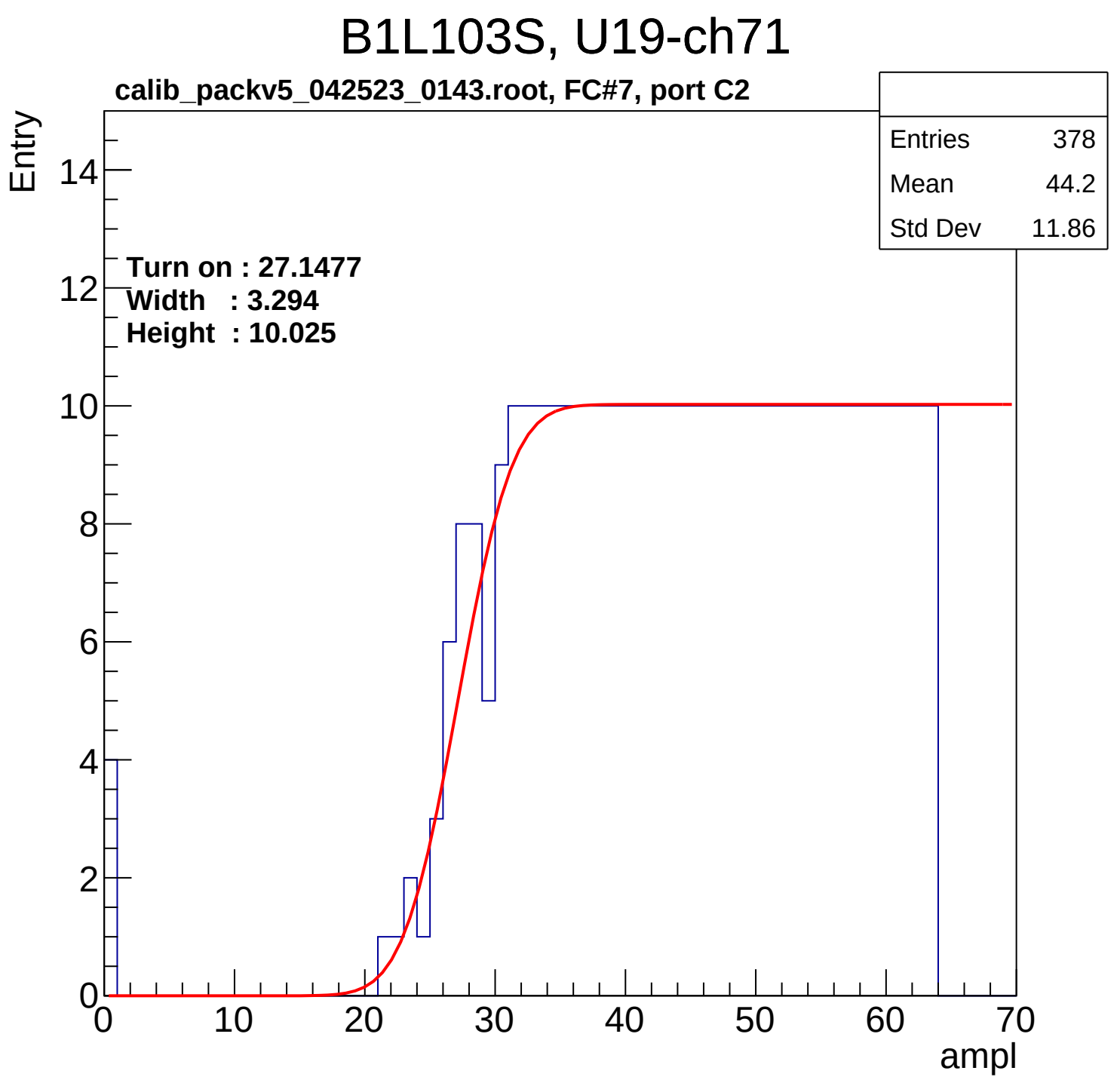
B1L103S, U19-ch71
calib_packv5_042523_0143.root, FC#7, port C2
Entries 378
Mean 44.2
Std Dev 11.86
Turn on : 27.1477
Width : 3.294
Height : 10.025
Entry
ampl
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6
8
10
12
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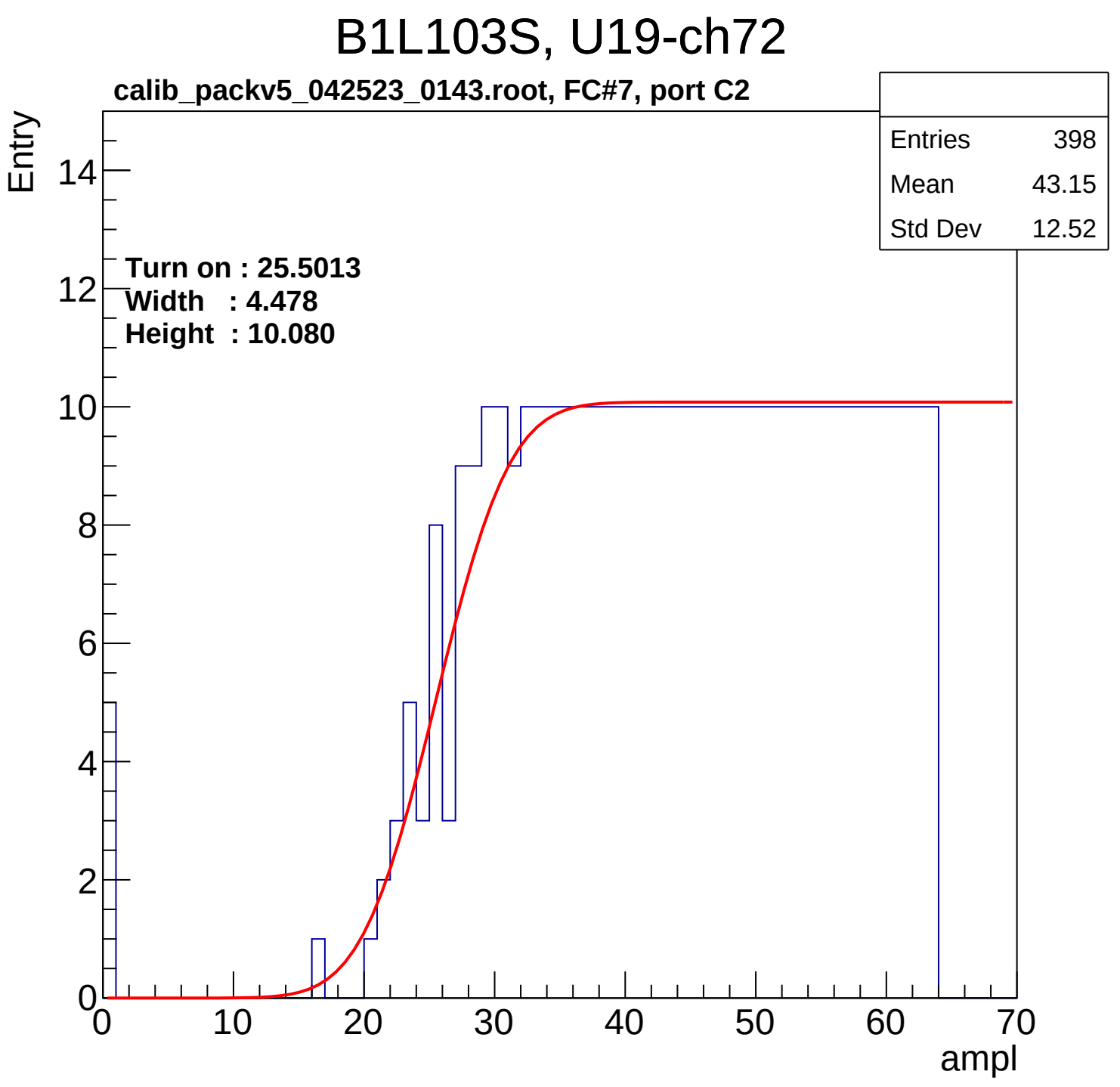
B1L103S, U19-ch72
calib_packv5_042523_0143.root, FC#7, port C2
Entries 398
Mean 43.15
Std Dev 12.52
Turn on : 25.5013
Width : 4.478
Height : 10.080
Entry
ampl
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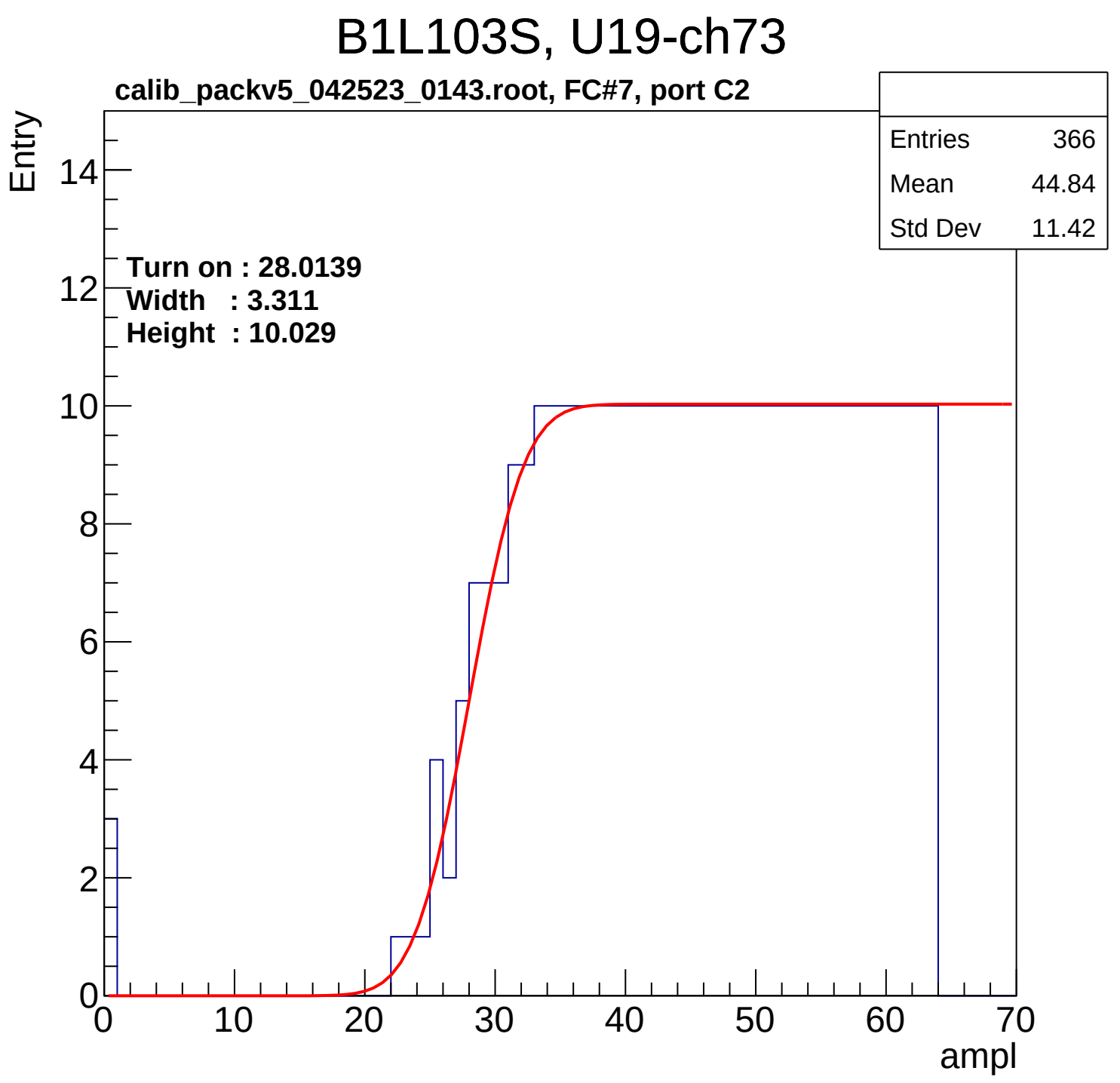
B1L103S, U19-ch73
calib_packv5_042523_0143.root, FC#7, port C2
Entries 366
Mean 44.84
Std Dev 11.42
Turn on : 28.0139
Width : 3.311
Height : 10.029
Entry
ampl
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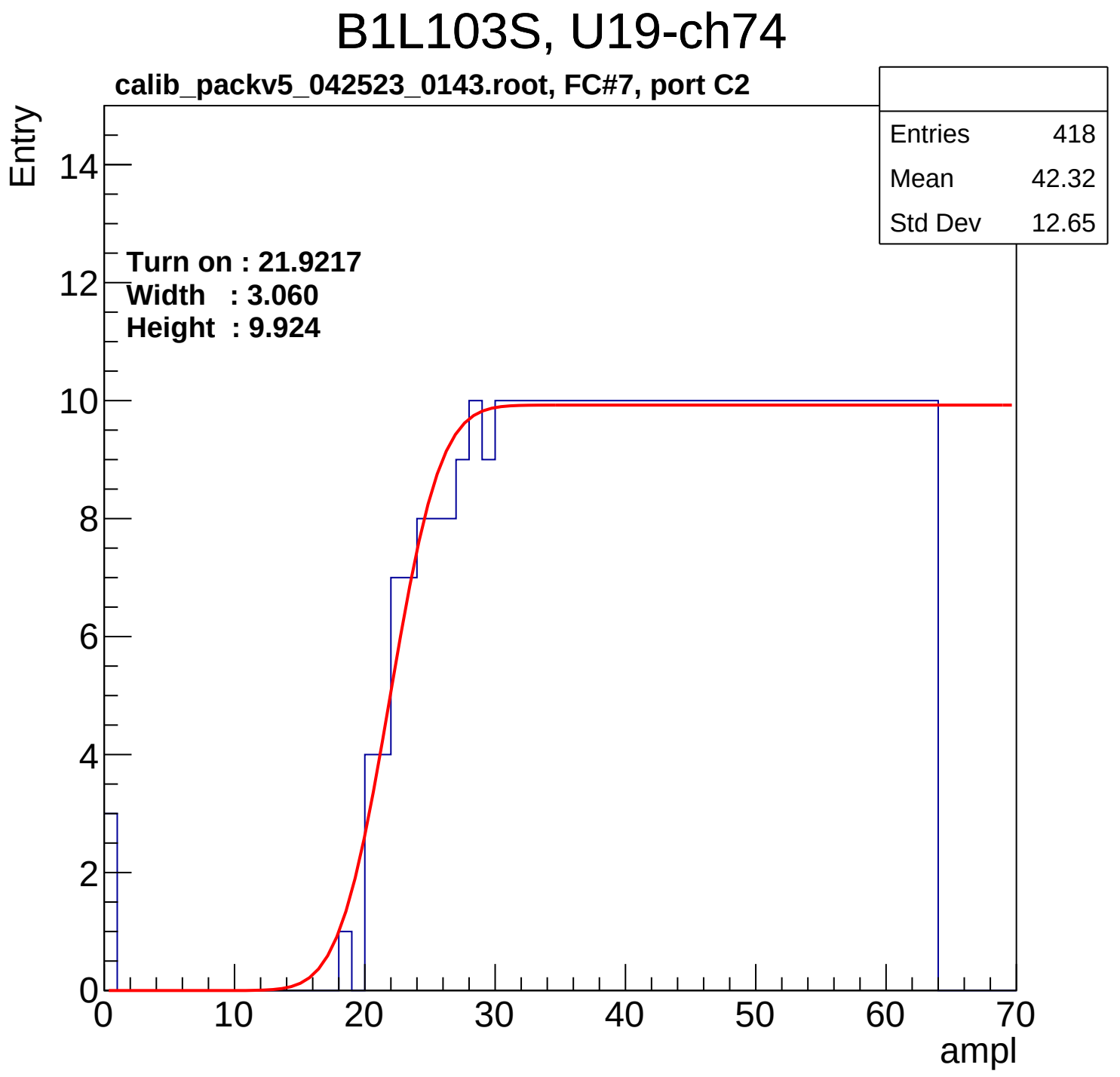
B1L103S, U19-ch74
calib_packv5_042523_0143.root, FC#7, port C2
Entries 418
Mean 42.32
Std Dev 12.65
Turn on : 21.9217
Width : 3.060
Height : 9.924
Entry
ampl
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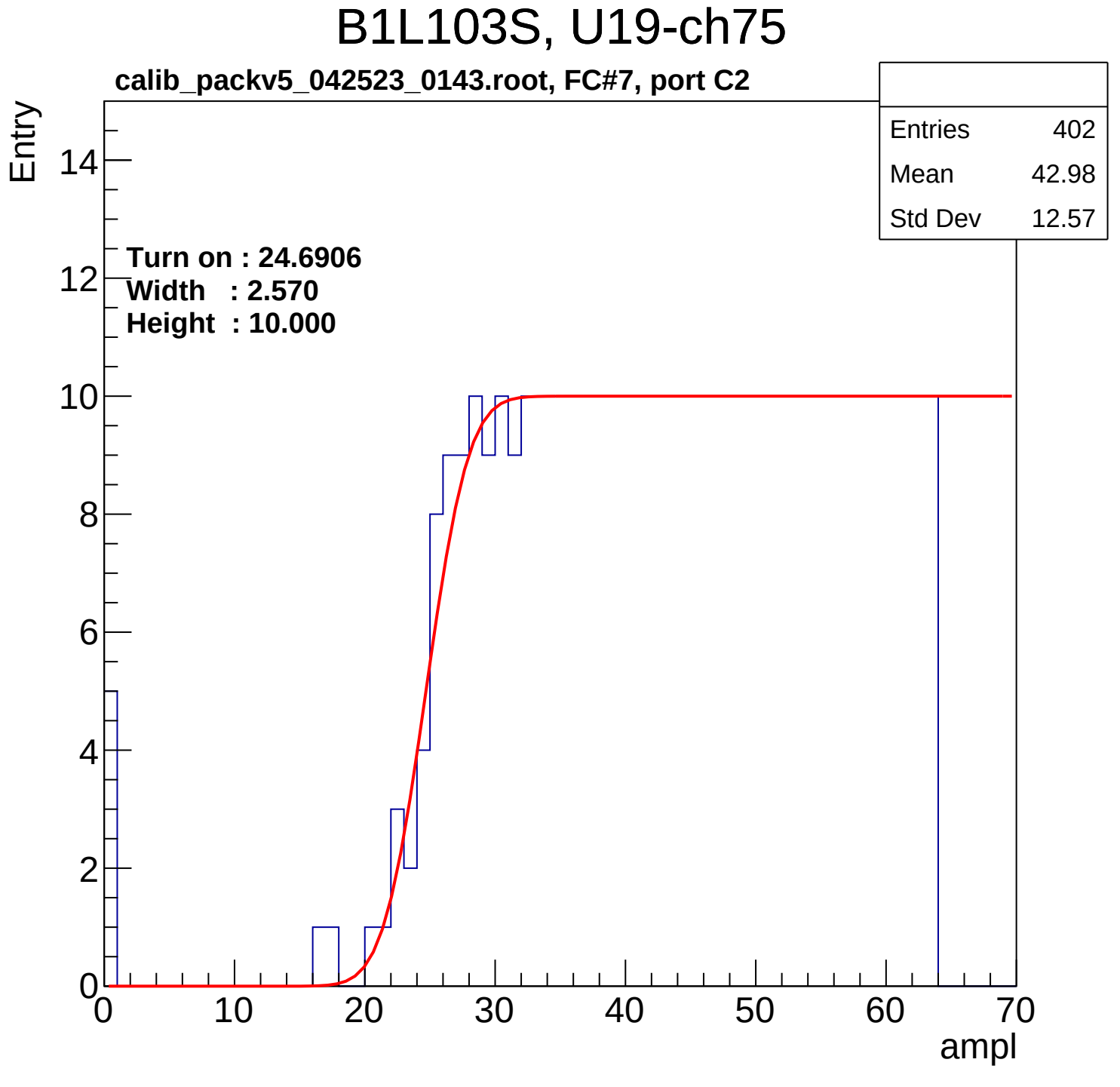
B1L103S, U19-ch75
calib_packv5_042523_0143.root, FC#7, port C2
Entries 402
Mean 42.98
Std Dev 12.57
Turn on : 24.6906
Width : 2.570
Height : 10.000
Entry
ampl
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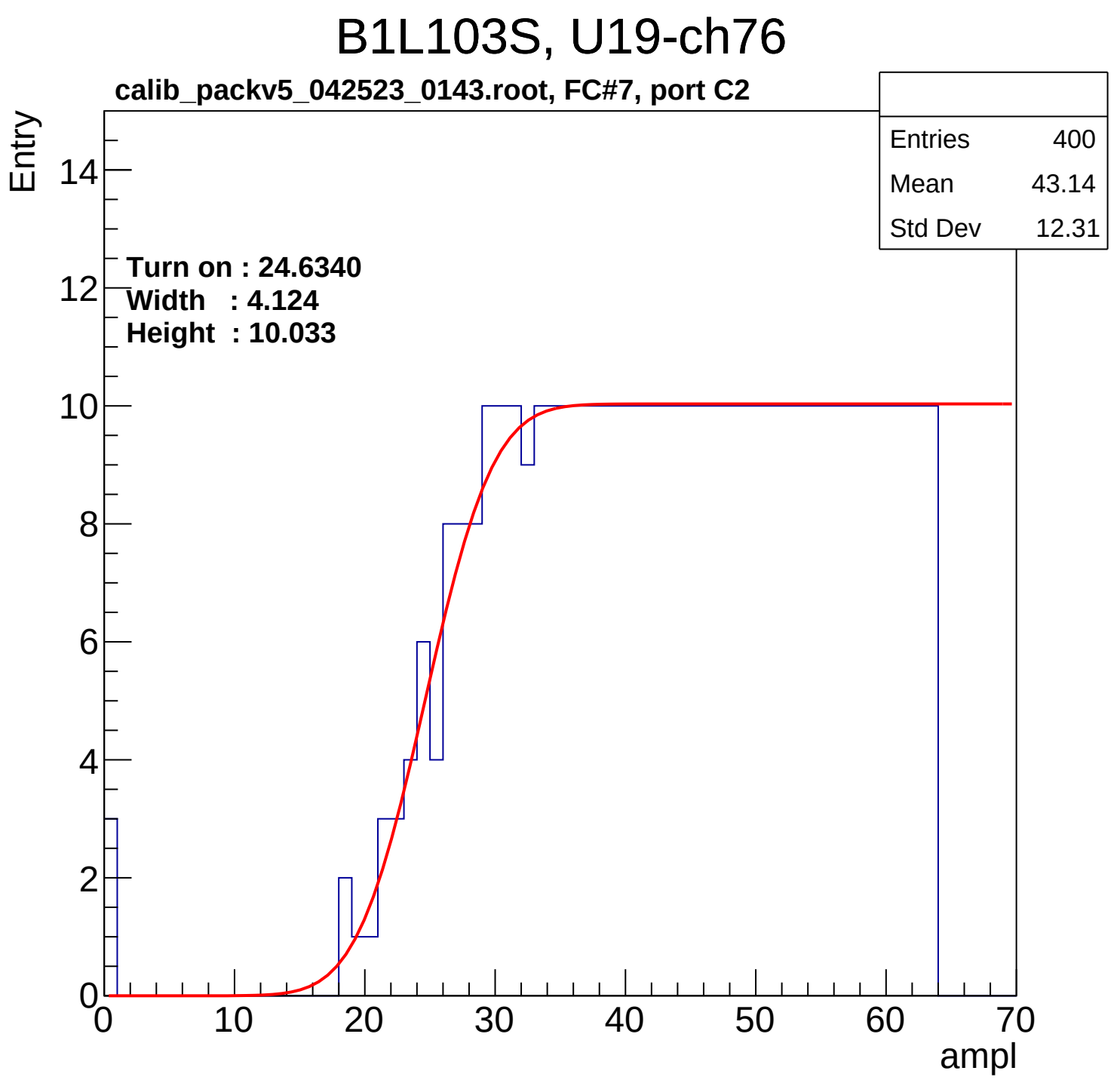
B1L103S, U19-ch76
calib_packv5_042523_0143.root, FC#7, port C2
Entries 400
Mean 43.14
Std Dev 12.31
Turn on : 24.6340
Width : 4.124
Height : 10.033
Entry
ampl
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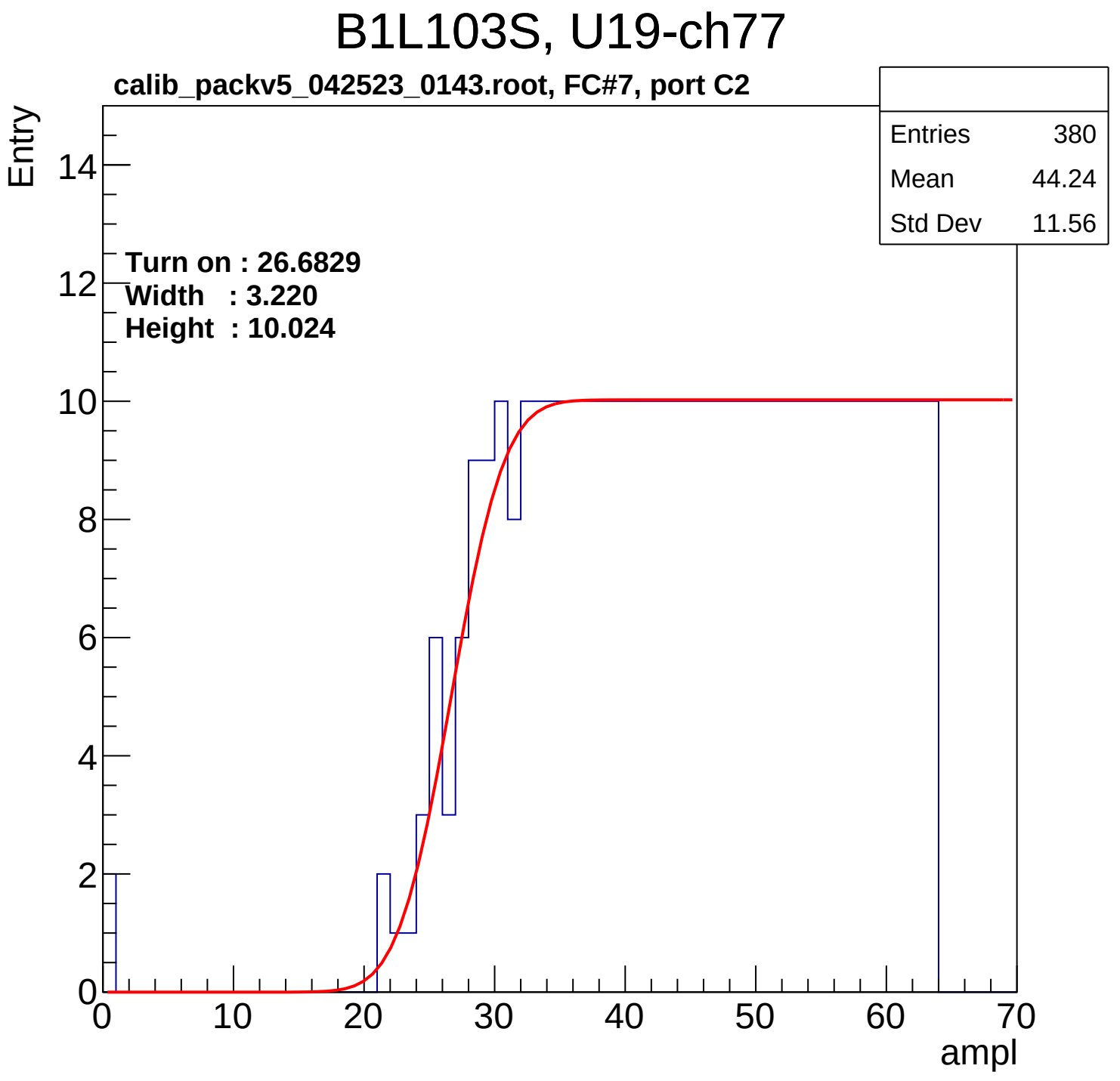
B1L103S, U19-ch77
calib_packv5_042523_0143.root, FC#7, port C2
Entries 380
Mean 44.24
Std Dev 11.56
Turn on : 26.6829
Width : 3.220
Height : 10.024
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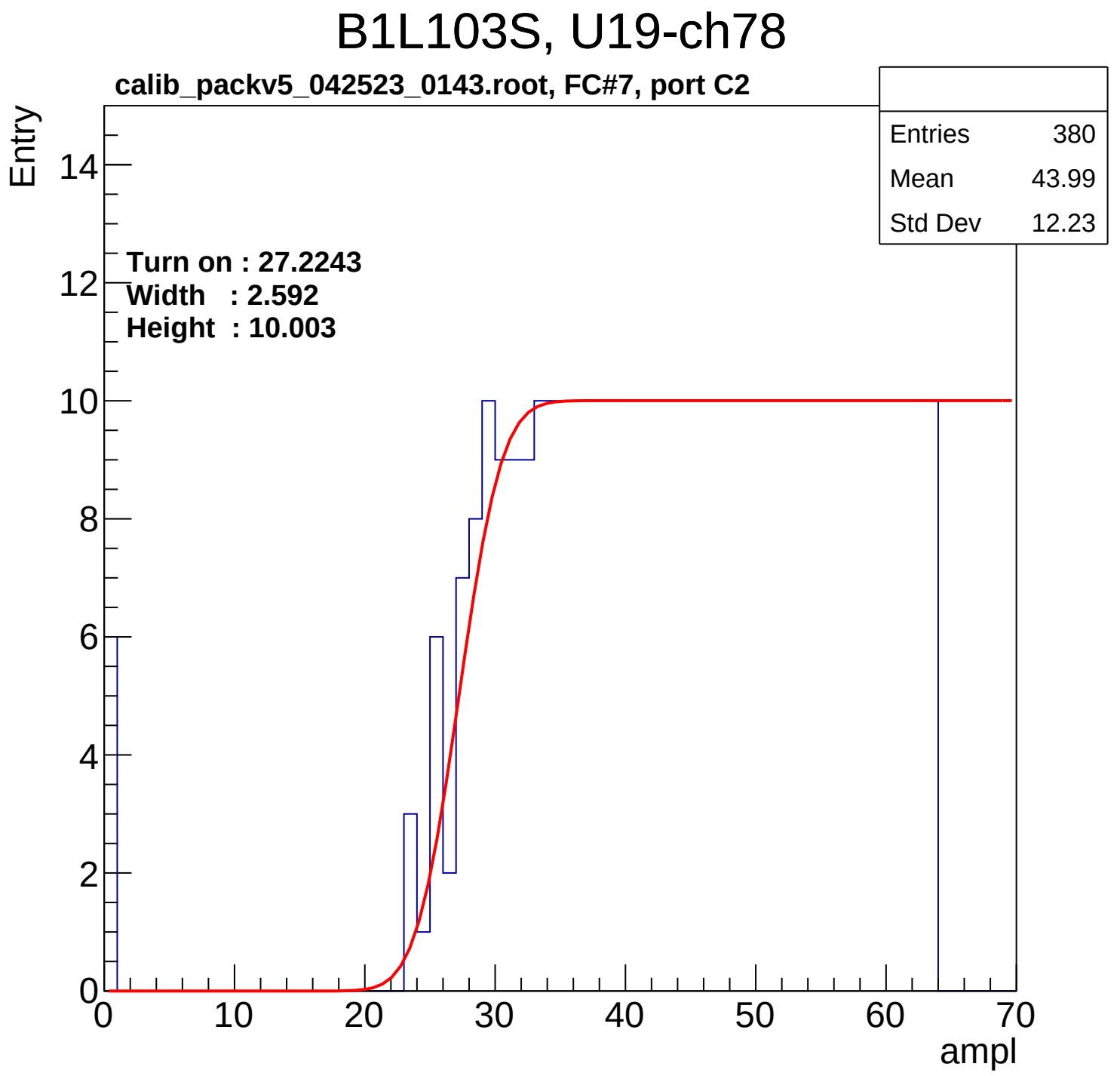
B1L103S, U19-ch78
calib_packv5_042523_0143.root, FC#7, port C2
Entries 380
Mean 43.99
Std Dev 12.23
Turn on : 27.2243
Width : 2.592
Height : 10.003
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ampl
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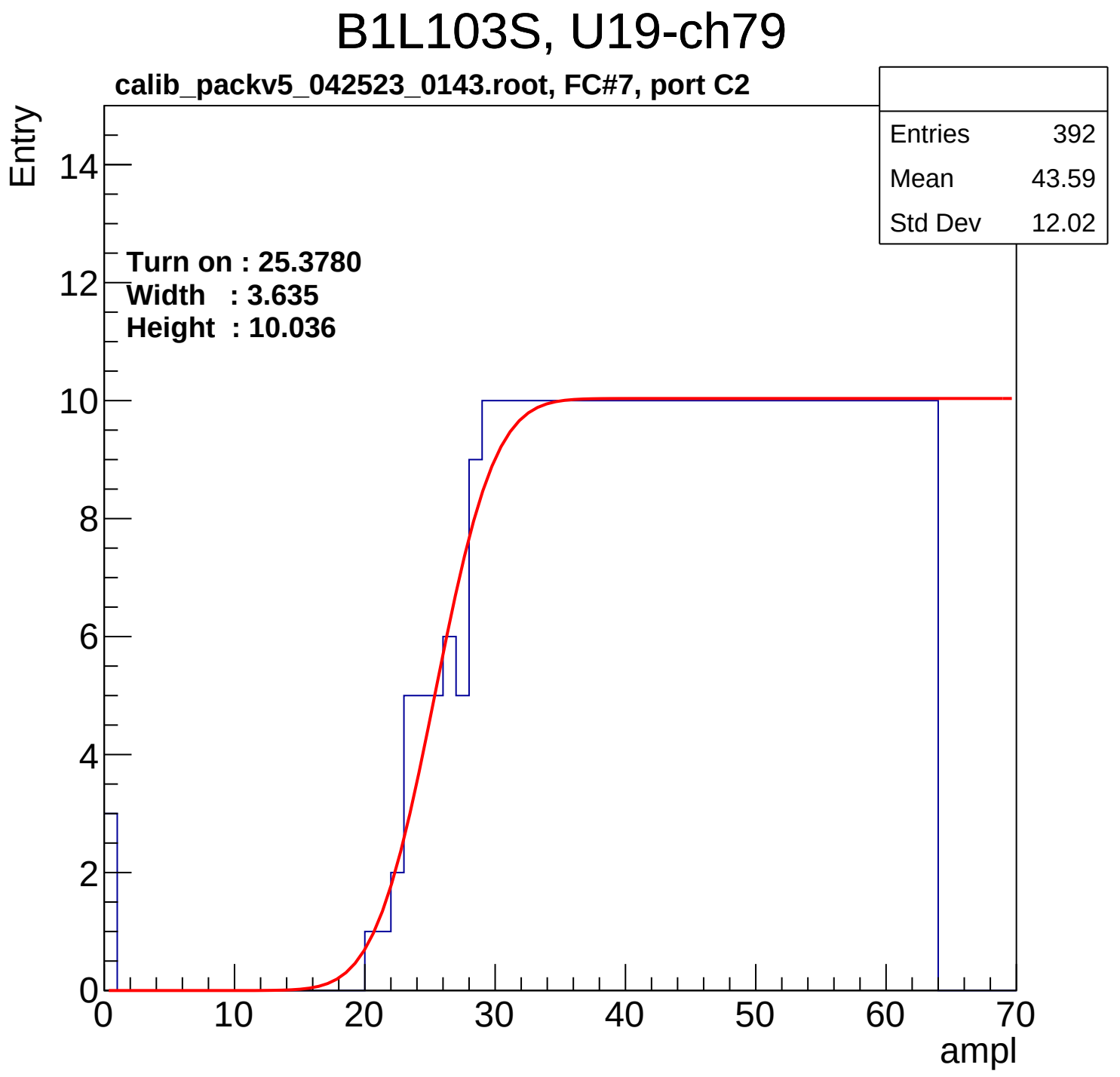
B1L103S, U19-ch79
calib_packv5_042523_0143.root, FC#7, port C2
Entries 392
Mean 43.59
Std Dev 12.02
Turn on : 25.3780
Width : 3.635
Height : 10.036
Entry
ampl
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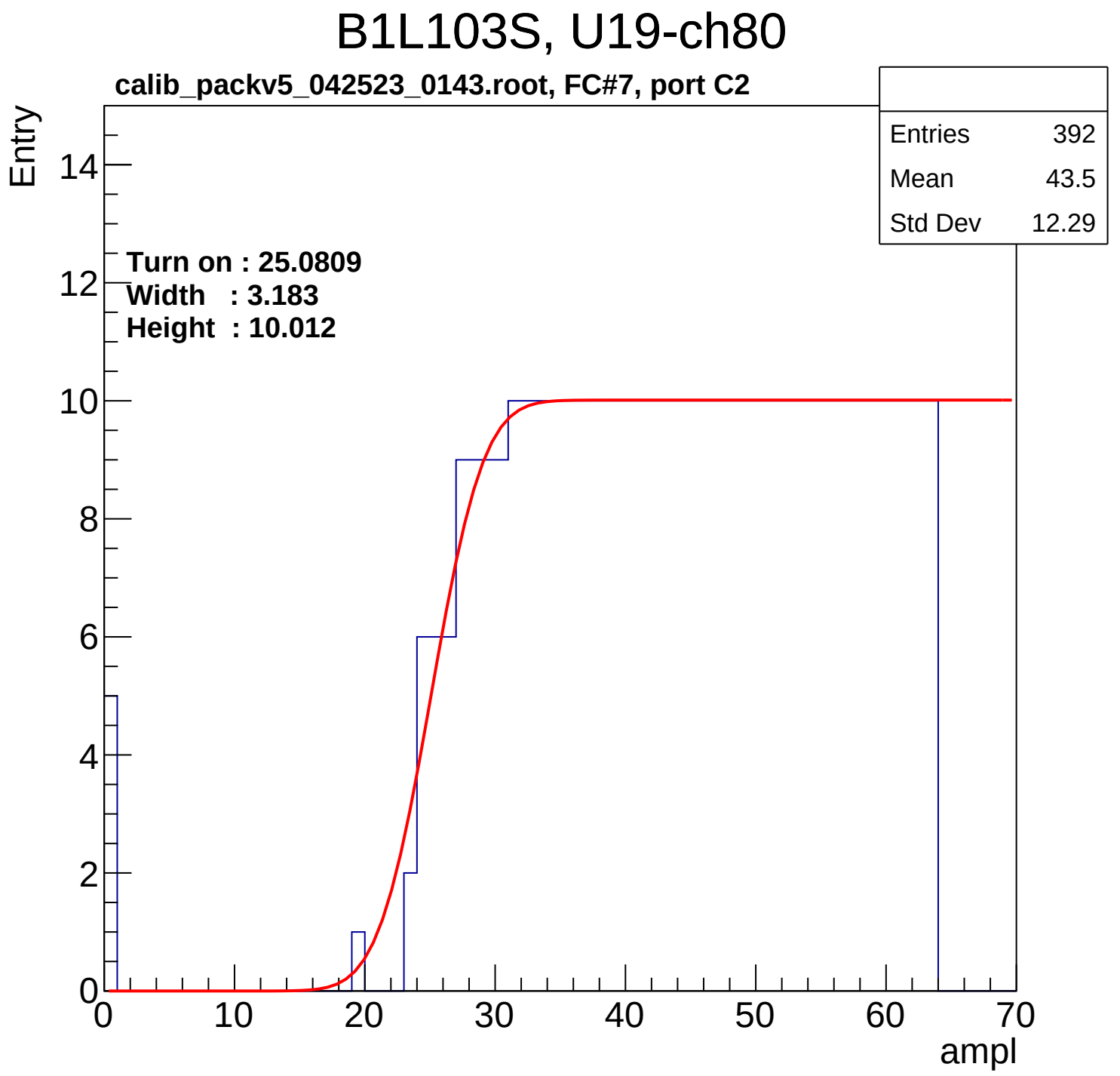
B1L103S, U19-ch80
calib_packv5_042523_0143.root, FC#7, port C2
Entries 392
Mean 43.5
Std Dev 12.29
Turn on : 25.0809
Width : 3.183
Height : 10.012
Entry
ampl
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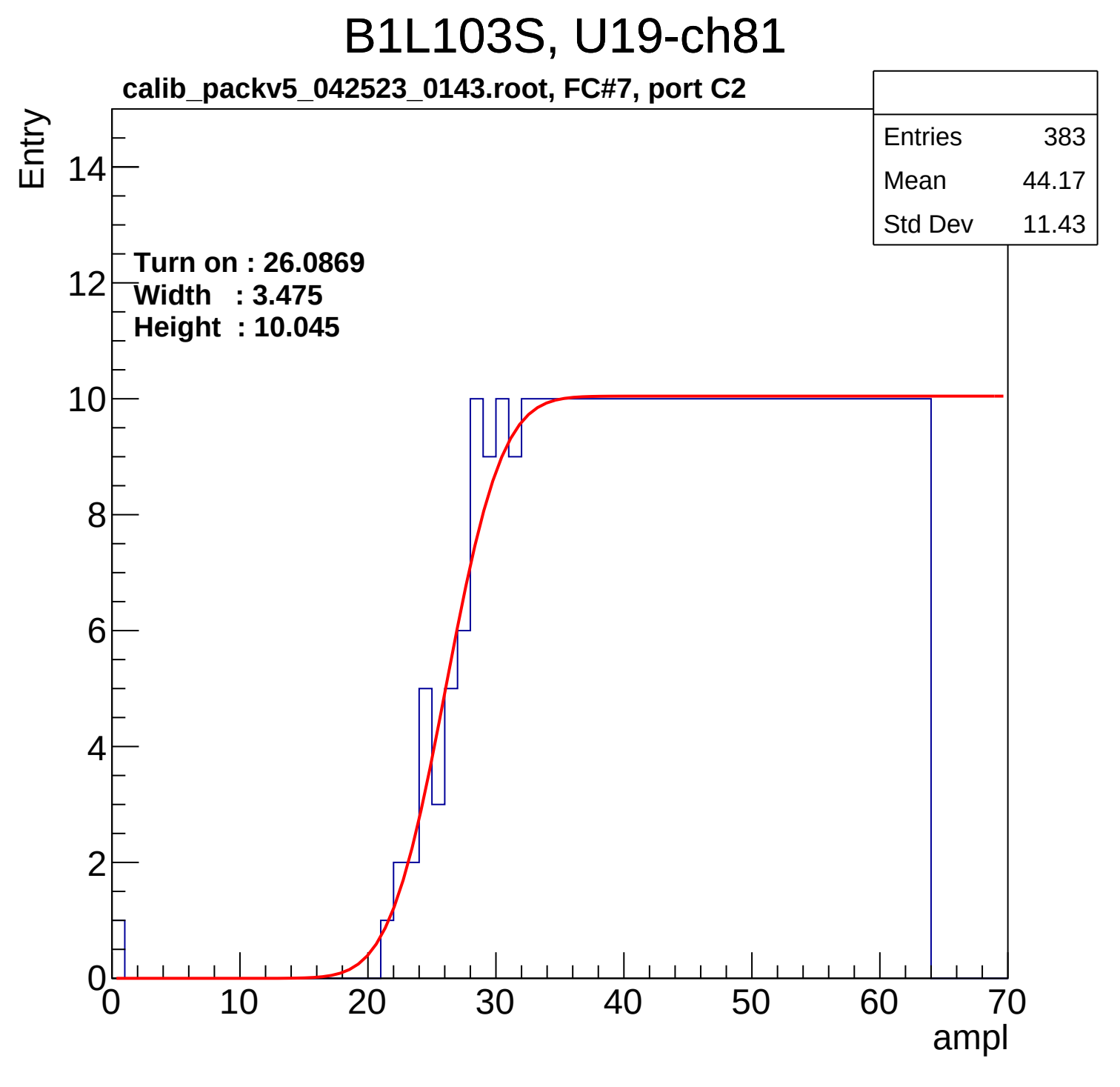
B1L103S, U19-ch81
calib_packv5_042523_0143.root, FC#7, port C2
Entries 383
Mean 44.17
Std Dev 11.43
Turn on : 26.0869
Width : 3.475
Height : 10.045
Entry
ampl
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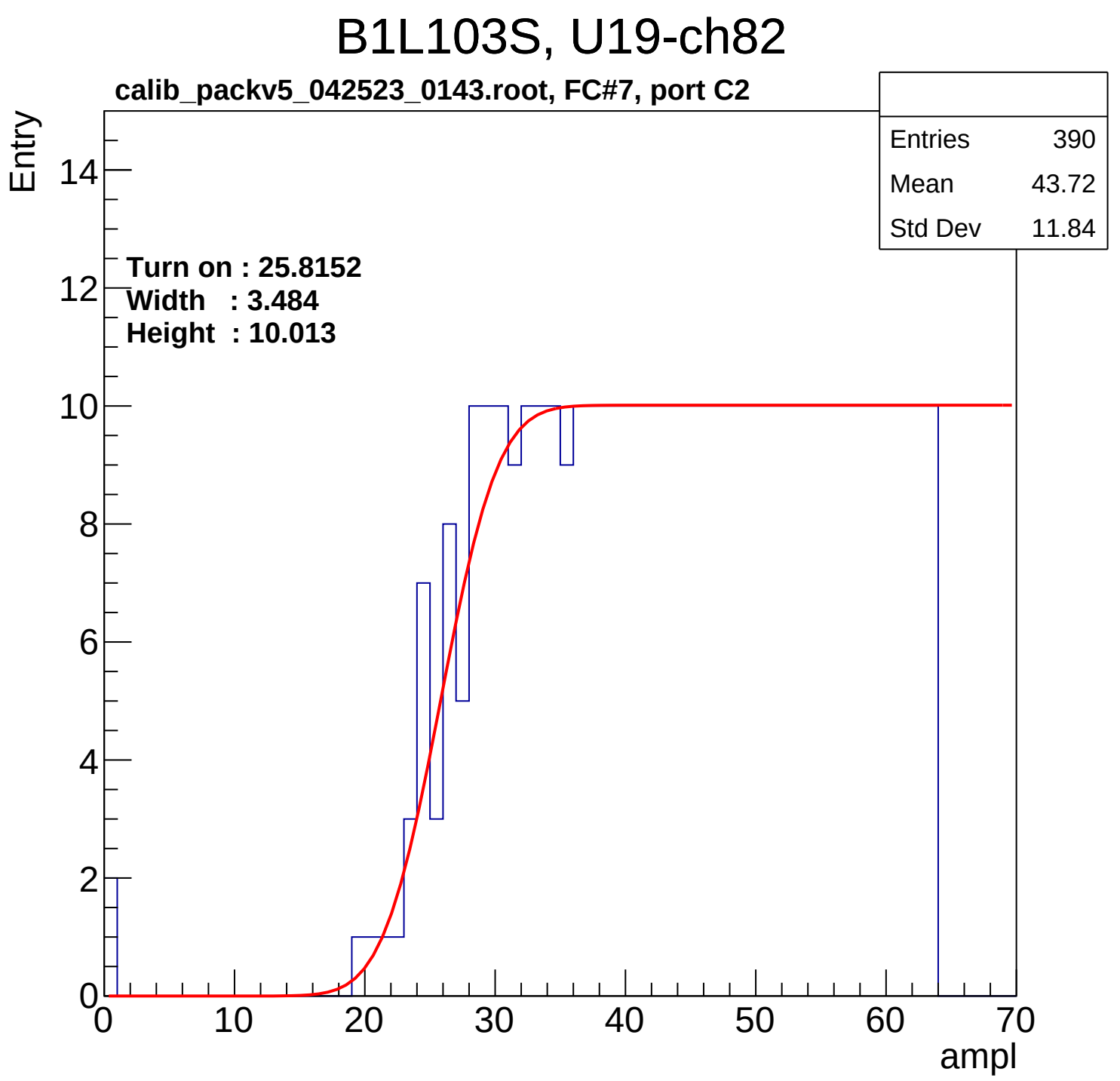
B1L103S, U19-ch82
calib_packv5_042523_0143.root, FC#7, port C2
Entries 390
Mean 43.72
Std Dev 11.84
Turn on : 25.8152
Width : 3.484
Height : 10.013
Entry
ampl
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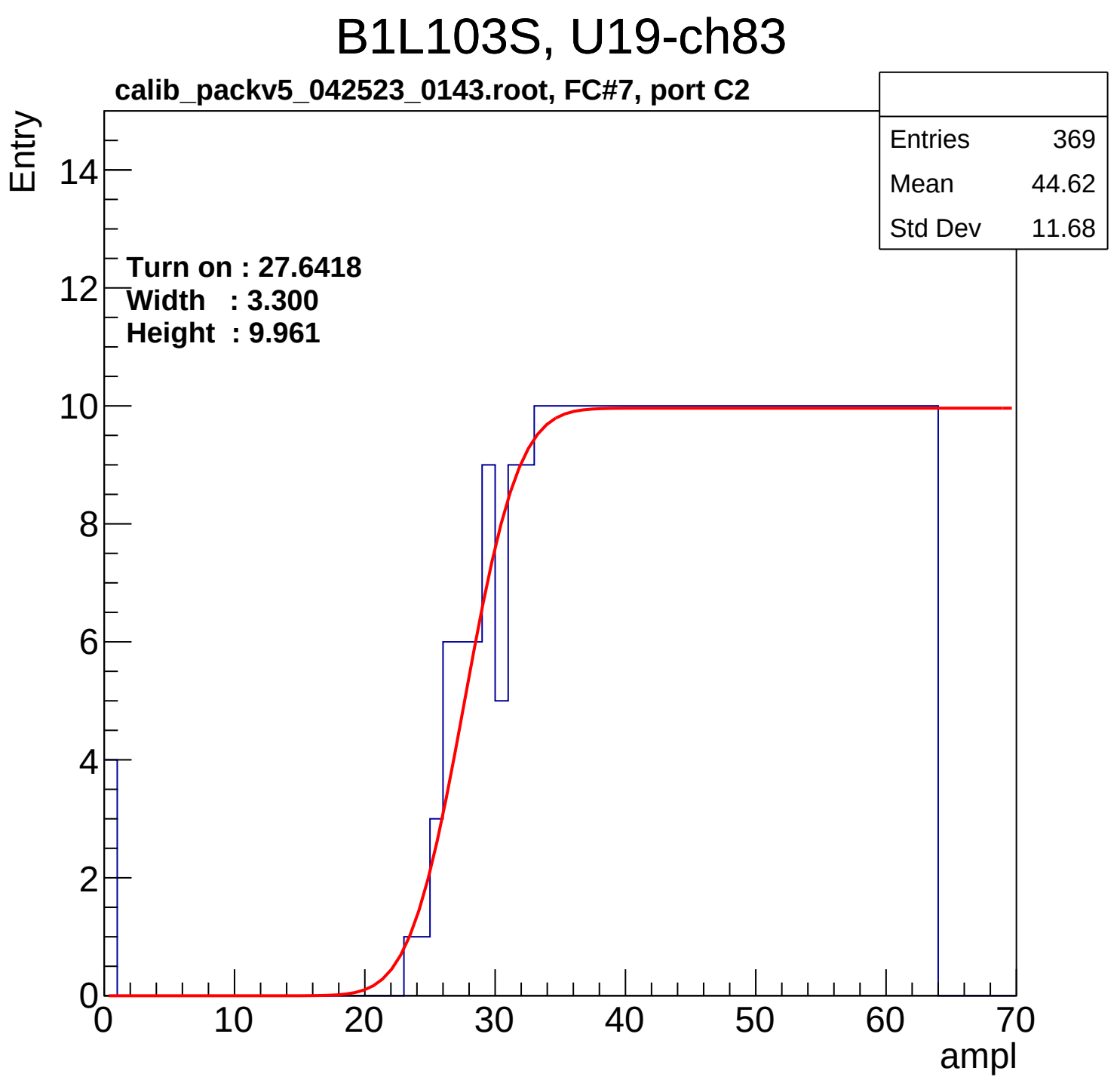
B1L103S, U19-ch83
calib_packv5_042523_0143.root, FC#7, port C2
Entries 369
Mean 44.62
Std Dev 11.68
Turn on : 27.6418
Width : 3.300
Height : 9.961
Entry
ampl
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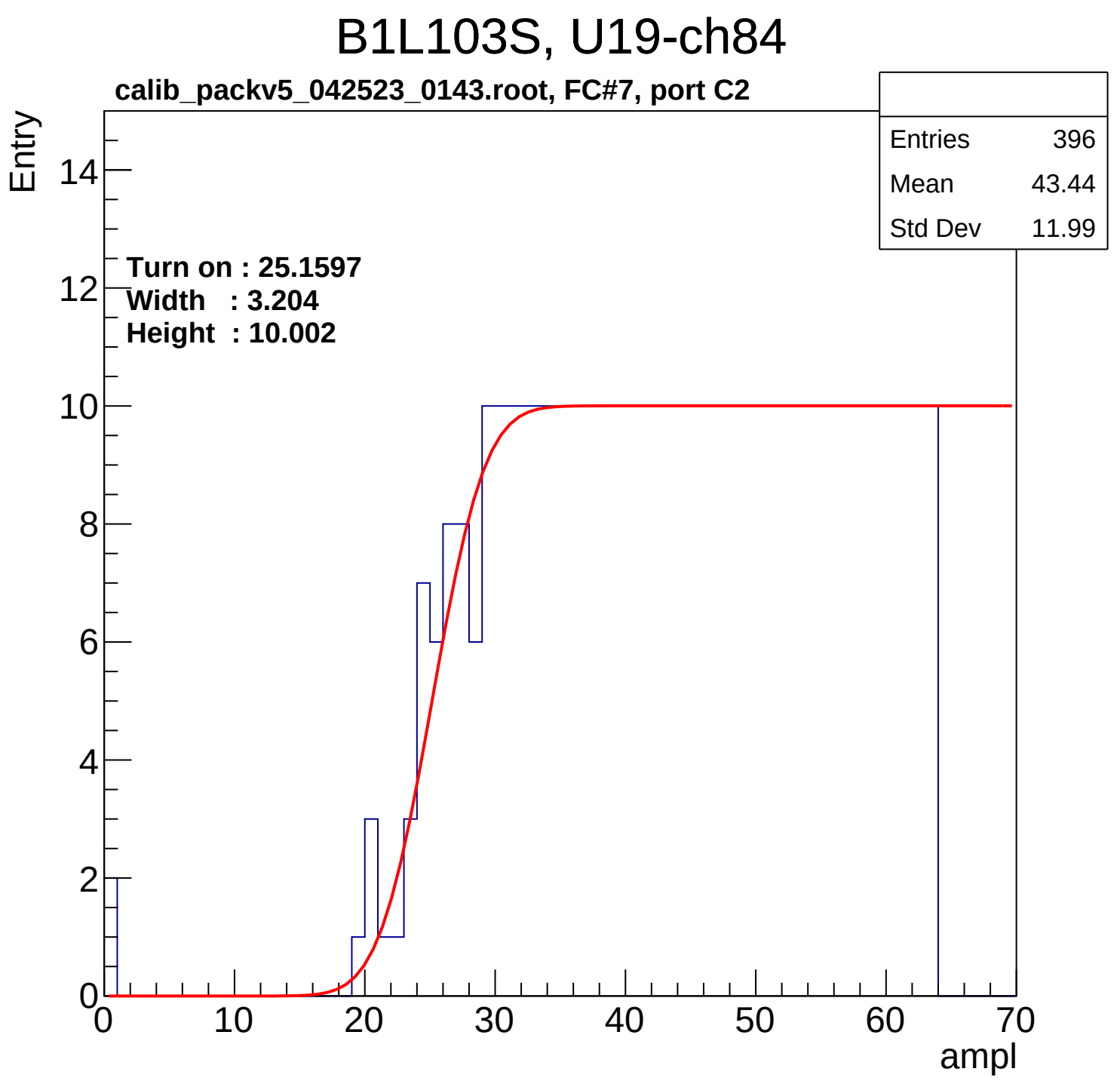
B1L103S, U19-ch84
calib_packv5_042523_0143.root, FC#7, port C2
Entries 396
Mean 43.44
Std Dev 11.99
Turn on : 25.1597
Width : 3.204
Height : 10.002
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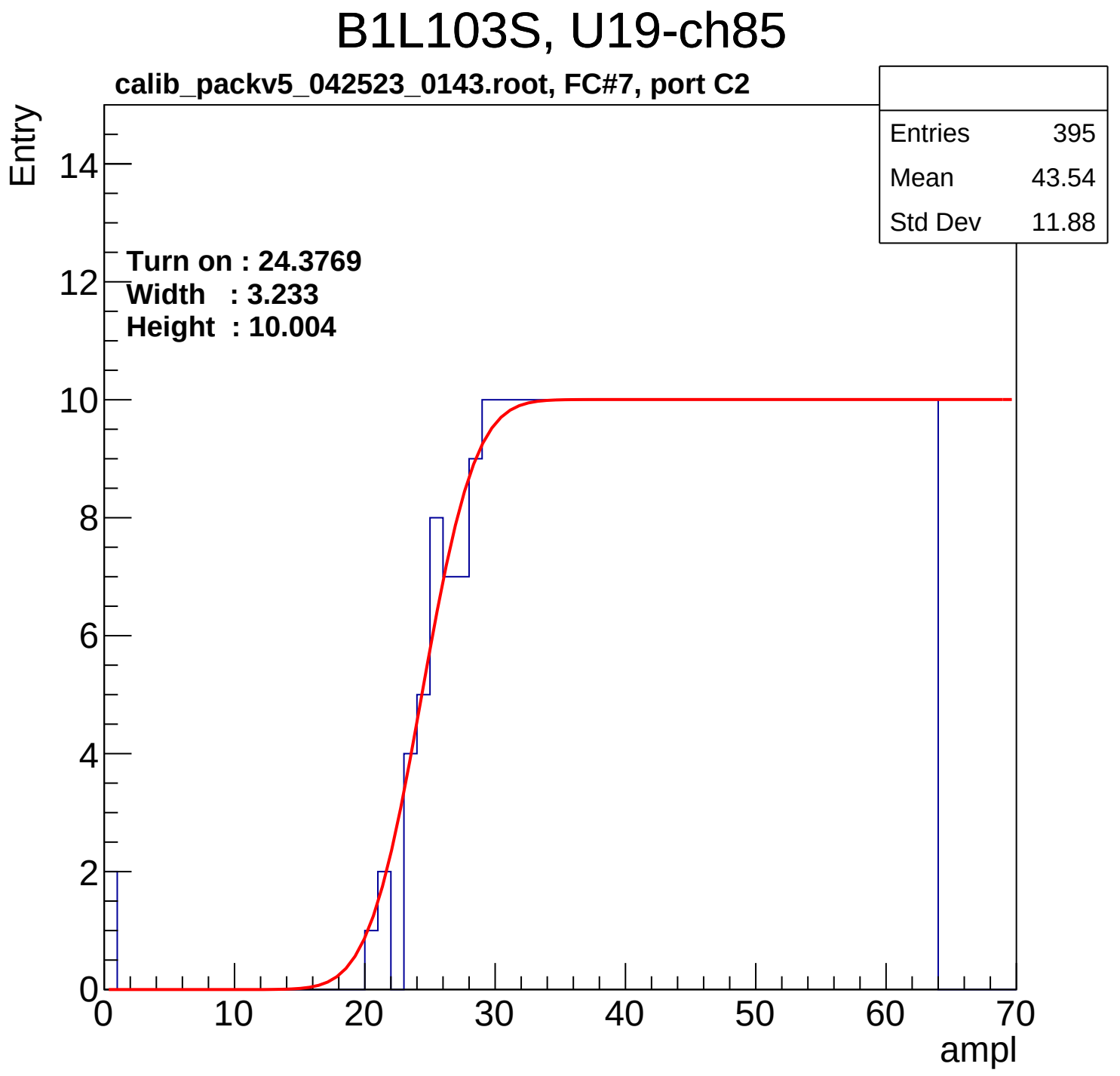
B1L103S, U19-ch85
calib_packv5_042523_0143.root, FC#7, port C2
Entries 395
Mean 43.54
Std Dev 11.88
Turn on : 24.3769
Width : 3.233
Height : 10.004
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ampl
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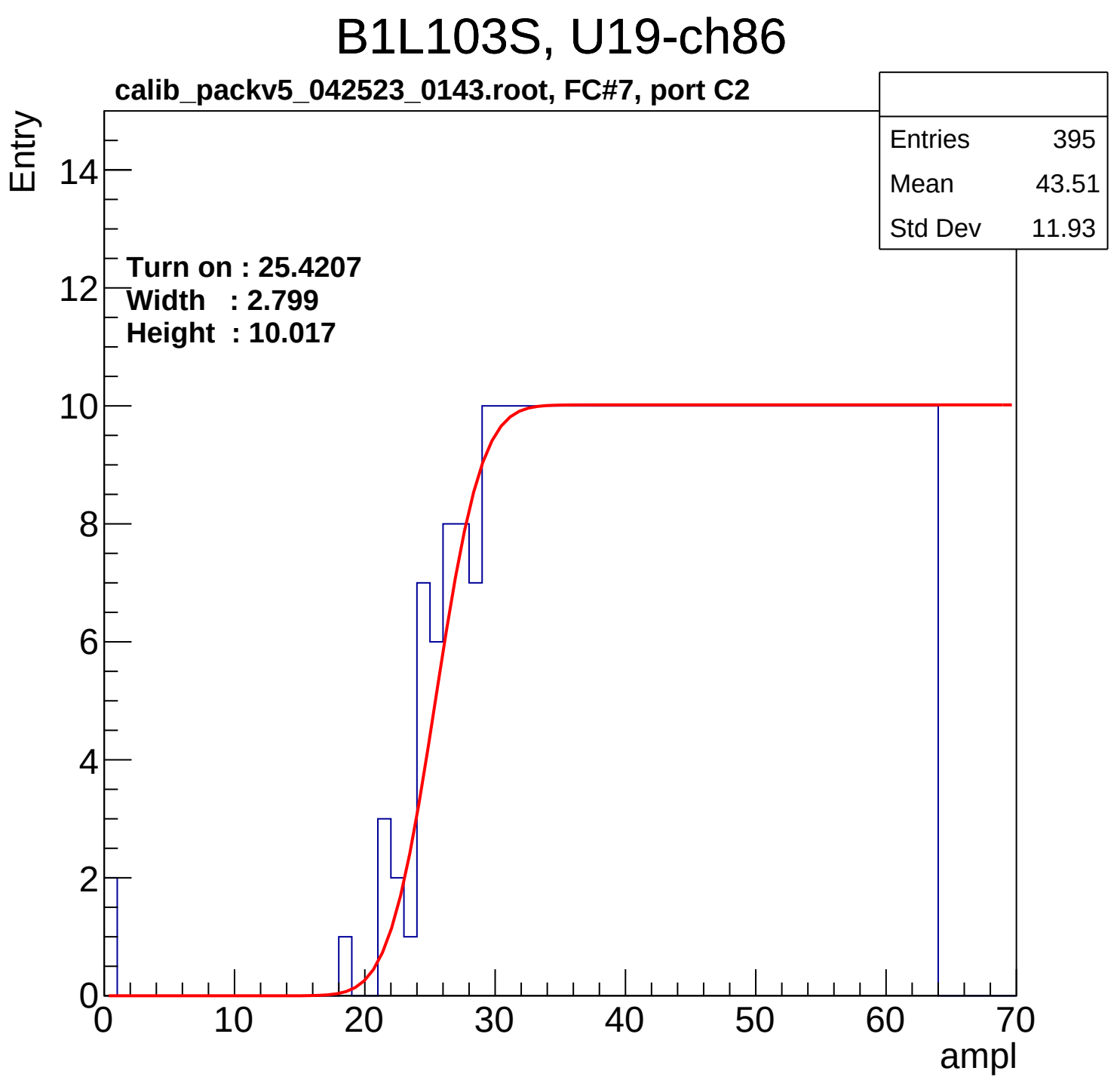
B1L103S, U19-ch86
calib_packv5_042523_0143.root, FC#7, port C2
Entries 395
Mean 43.51
Std Dev 11.93
Turn on : 25.4207
Width : 2.799
Height : 10.017
Entry
ampl
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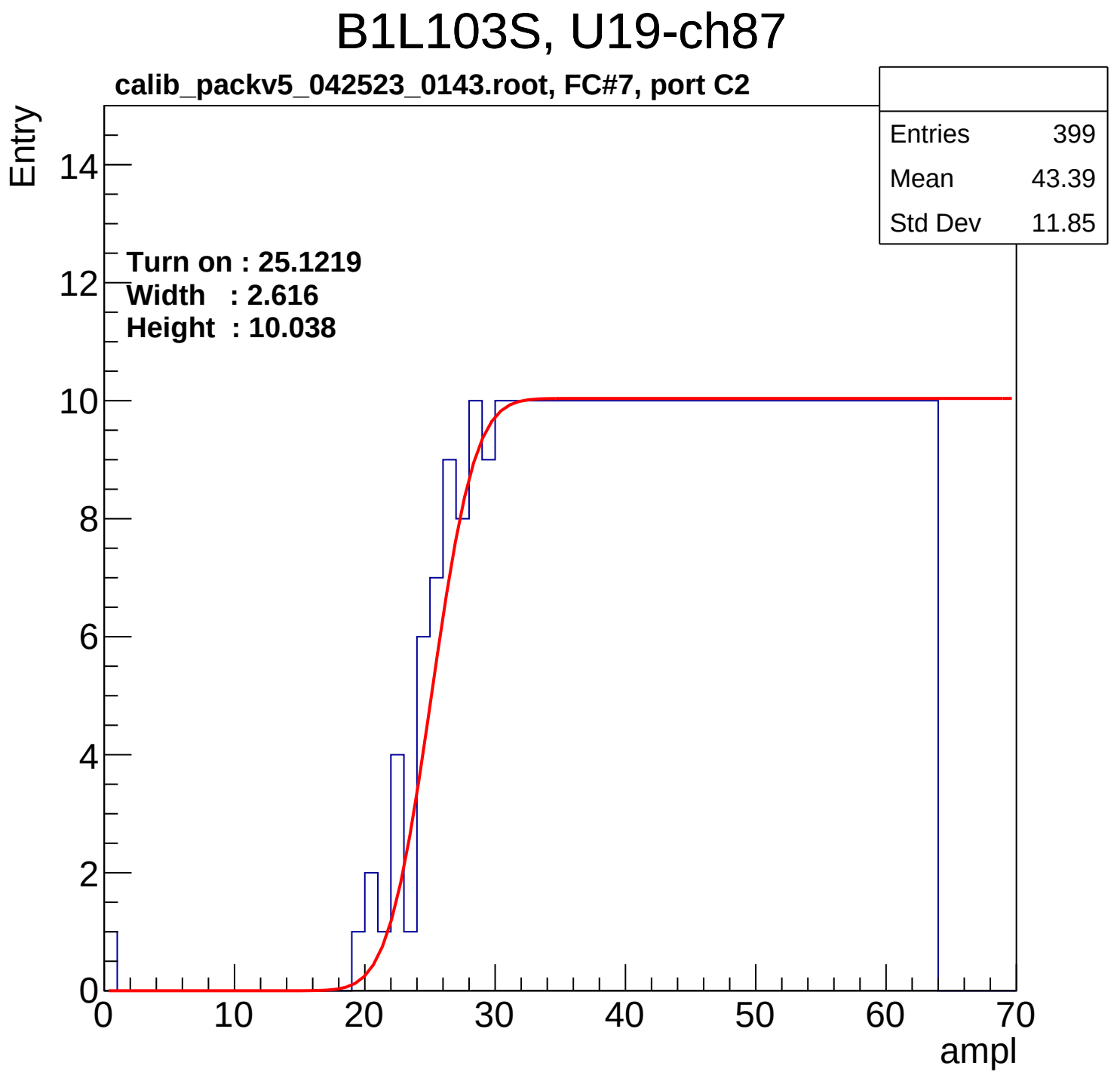
B1L103S, U19-ch87
calib_packv5_042523_0143.root, FC#7, port C2
Entries 399
Mean 43.39
Std Dev 11.85
Turn on : 25.1219
Width : 2.616
Height : 10.038
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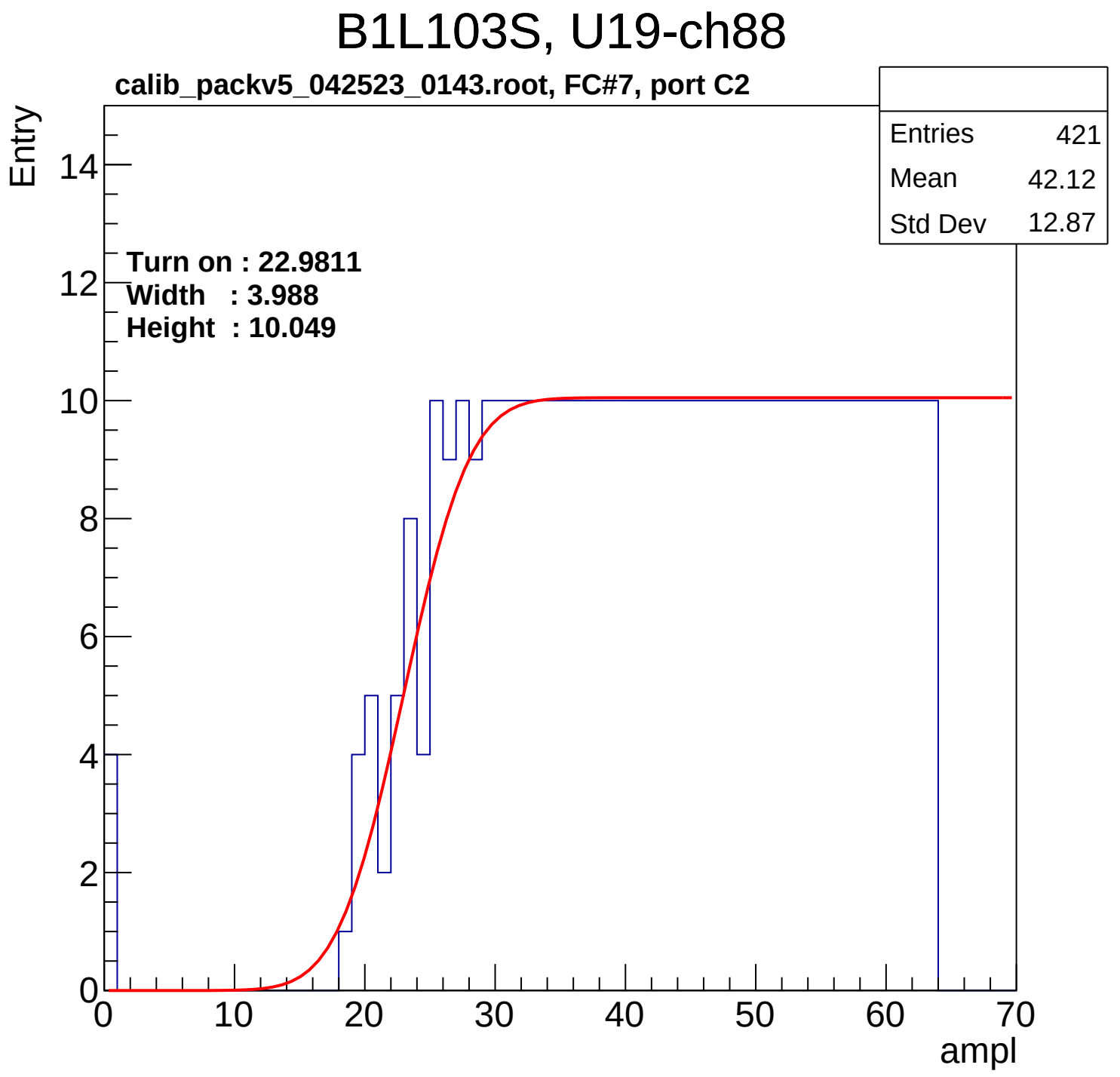
B1L103S, U19-ch88
calib_packv5_042523_0143.root, FC#7, port C2
Entries 421
Mean 42.12
Std Dev 12.87
Turn on : 22.9811
Width : 3.988
Height : 10.049
Entry
ampl
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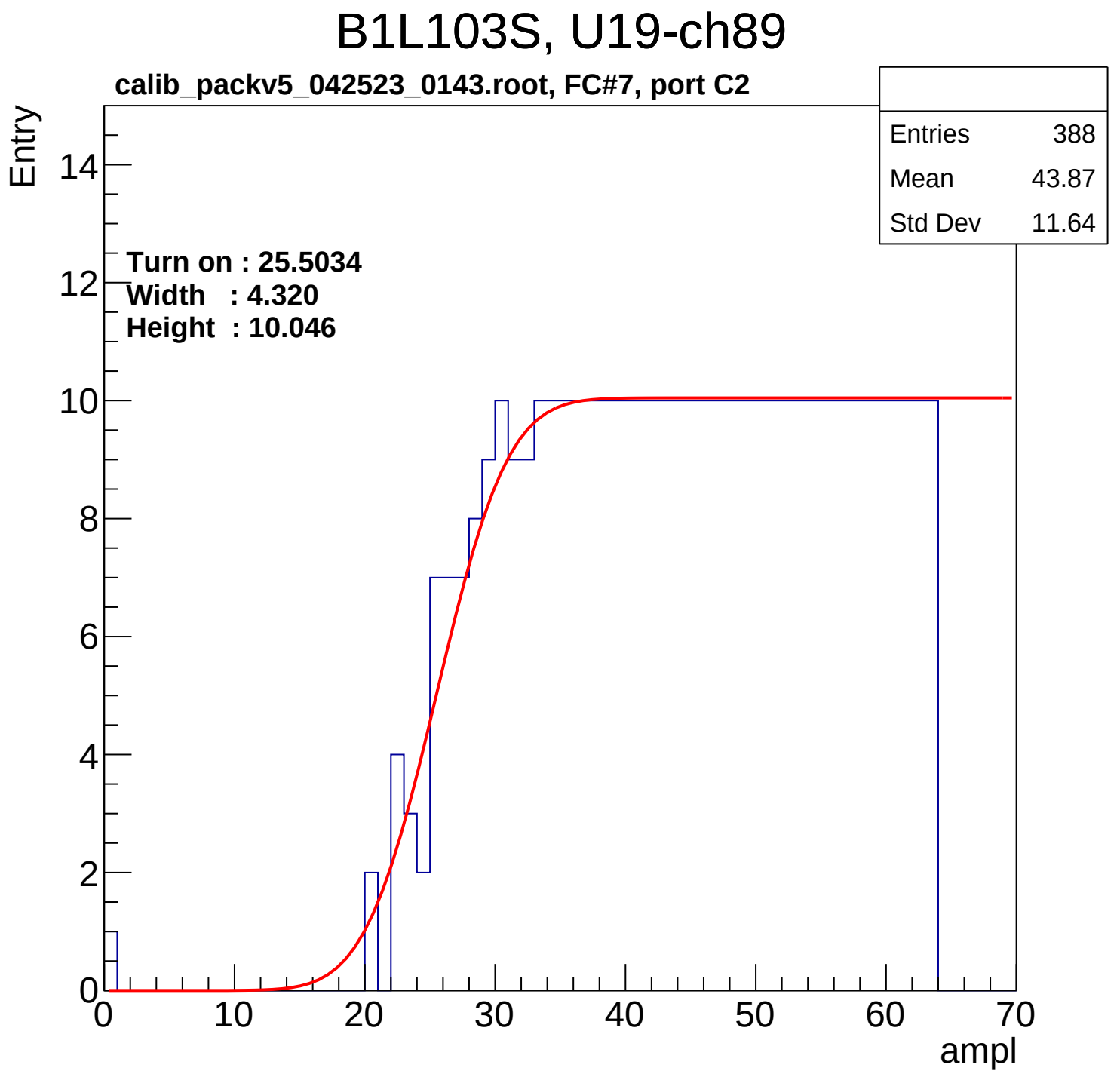
B1L103S, U19-ch89
calib_packv5_042523_0143.root, FC#7, port C2
Entries 388
Mean 43.87
Std Dev 11.64
Turn on : 25.5034
Width : 4.320
Height : 10.046
Entry
ampl
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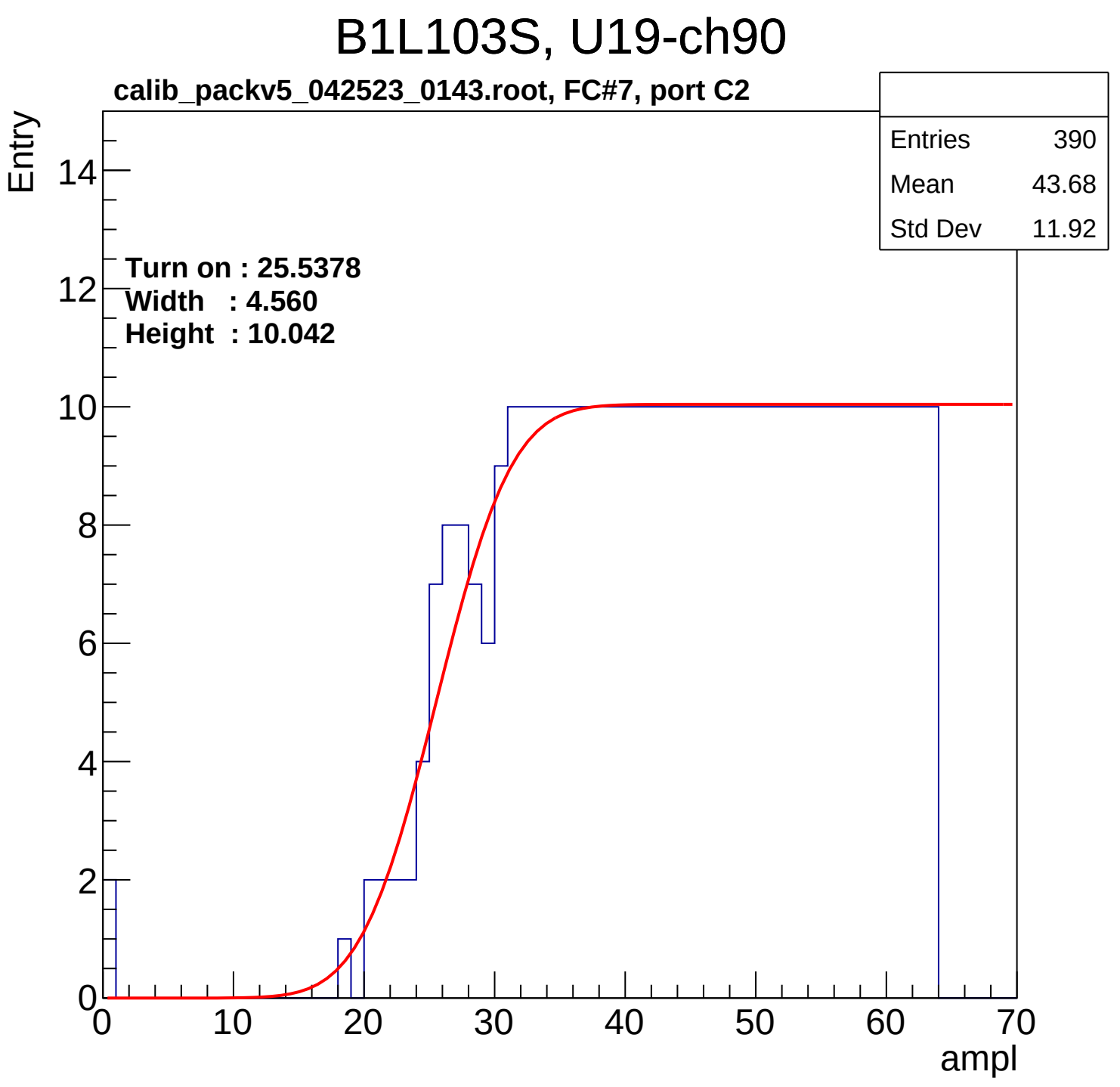
B1L103S, U19-ch90
calib_packv5_042523_0143.root, FC#7, port C2
Entries 390
Mean 43.68
Std Dev 11.92
Turn on : 25.5378
Width : 4.560
Height : 10.042
Entry
ampl
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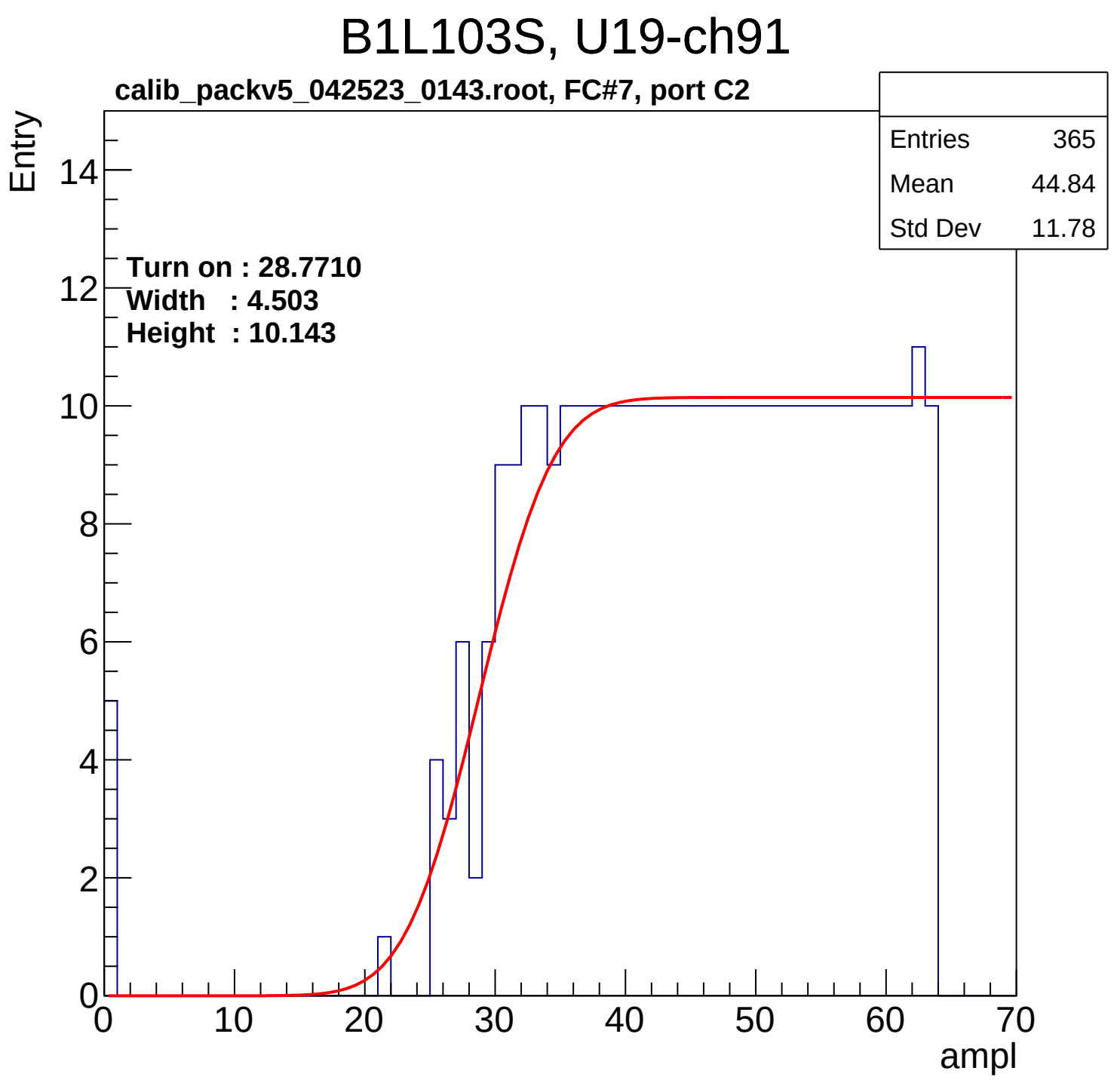
B1L103S, U19-ch91
calib_packv5_042523_0143.root, FC#7, port C2
Entries 365
Mean 44.84
Std Dev 11.78
Turn on : 28.7710
Width : 4.503
Height : 10.143
Entry
ampl
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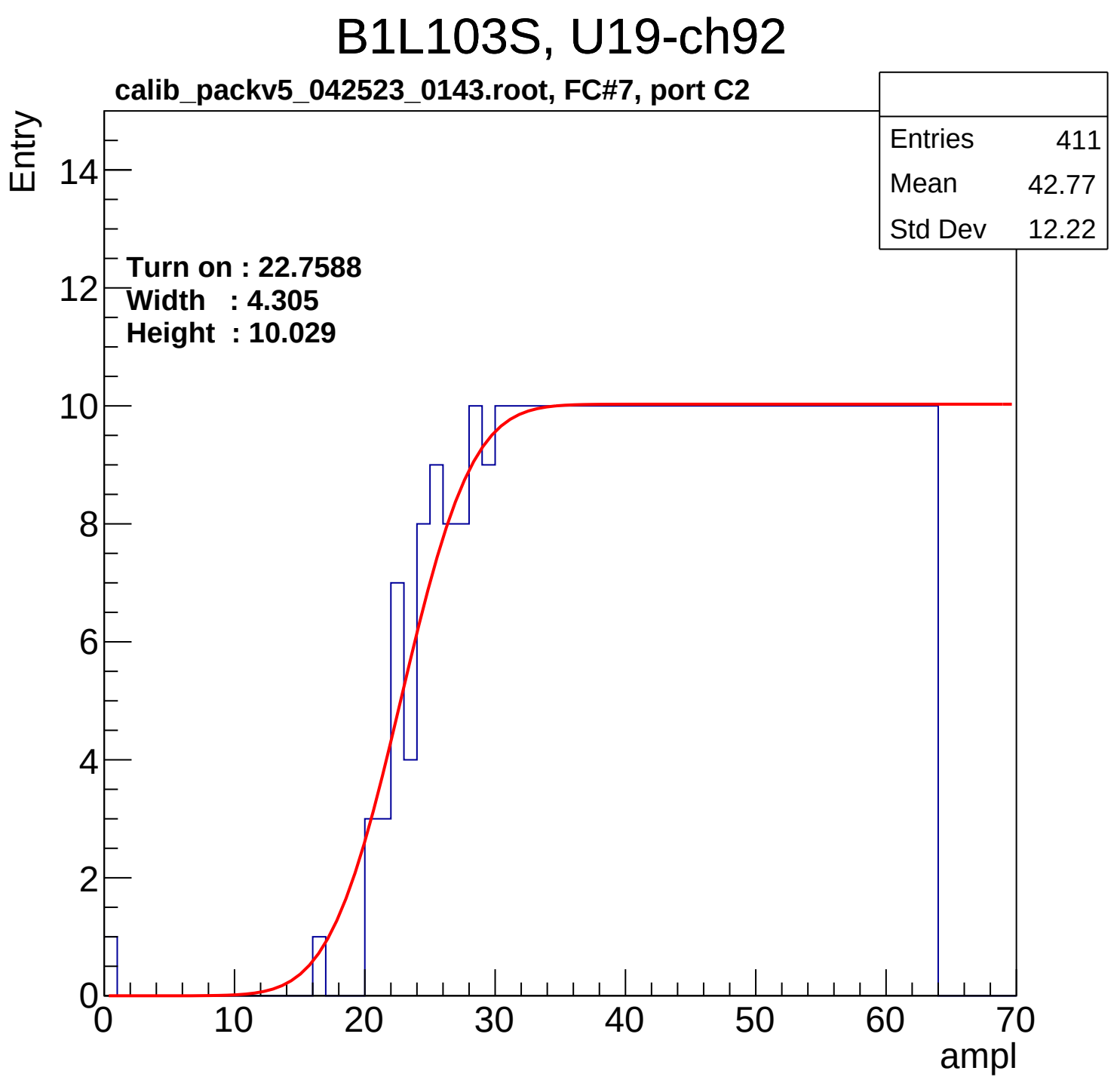
B1L103S, U19-ch92
calib_packv5_042523_0143.root, FC#7, port C2
Entries 411
Mean 42.77
Std Dev 12.22
Turn on : 22.7588
Width : 4.305
Height : 10.029
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ampl
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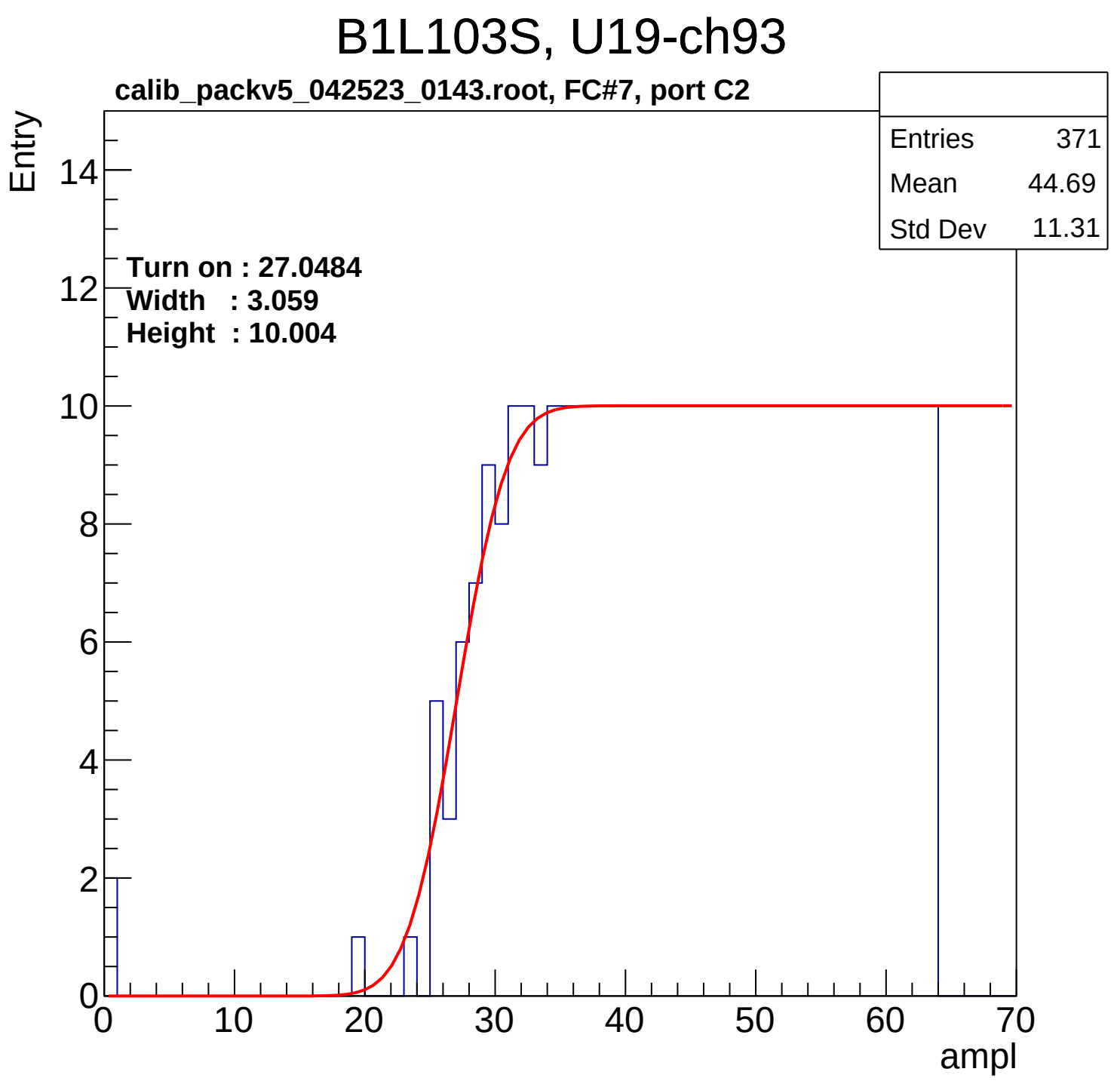
B1L103S, U19-ch93
calib_packv5_042523_0143.root, FC#7, port C2
Entries 371
Mean 44.69
Std Dev 11.31
Turn on : 27.0484
Width : 3.059
Height : 10.004
Entry
ampl
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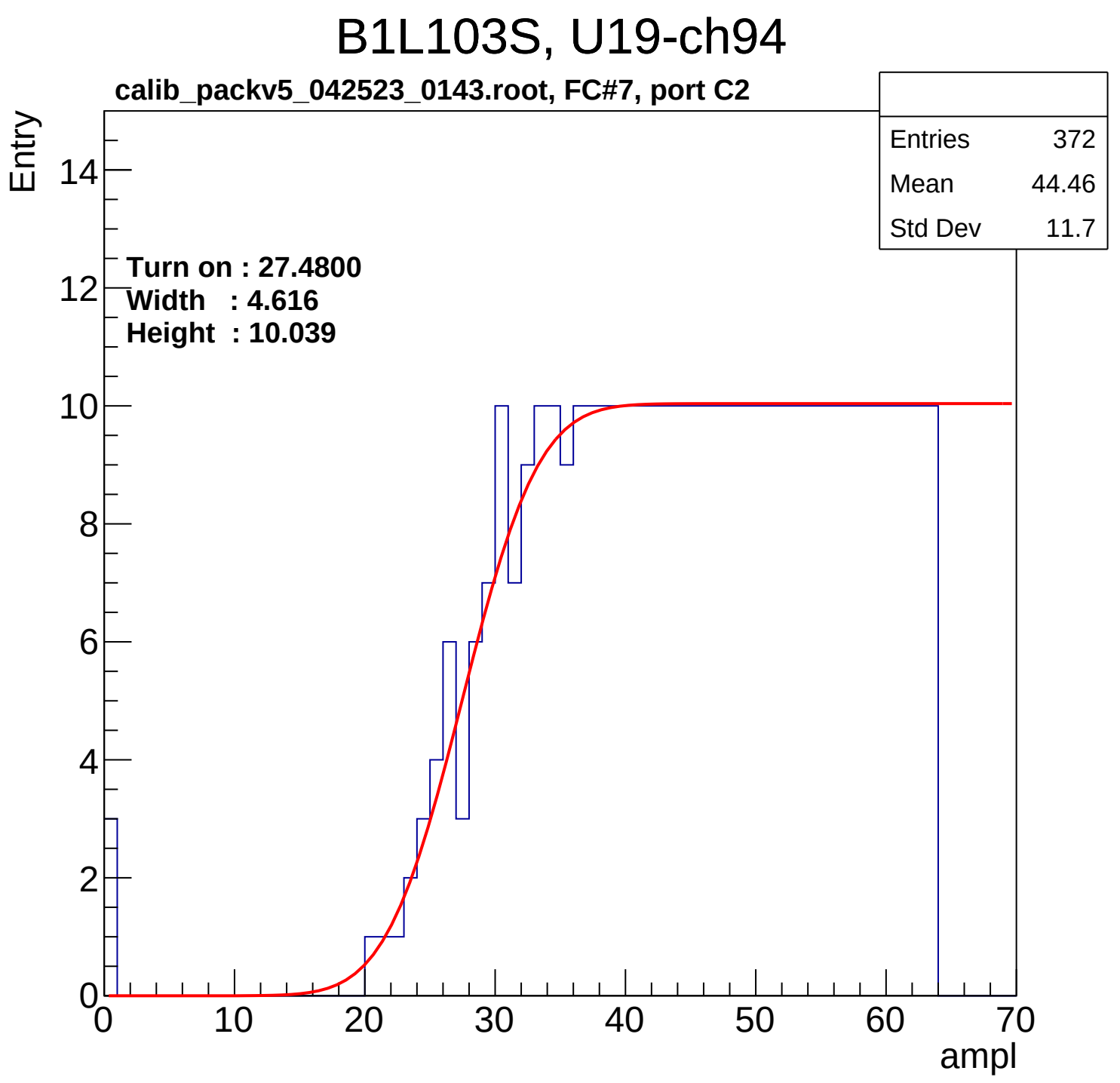
B1L103S, U19-ch94
calib_packv5_042523_0143.root, FC#7, port C2
Entries 372
Mean 44.46
Std Dev 11.7
Turn on : 27.4800
Width : 4.616
Height : 10.039
Entry
ampl
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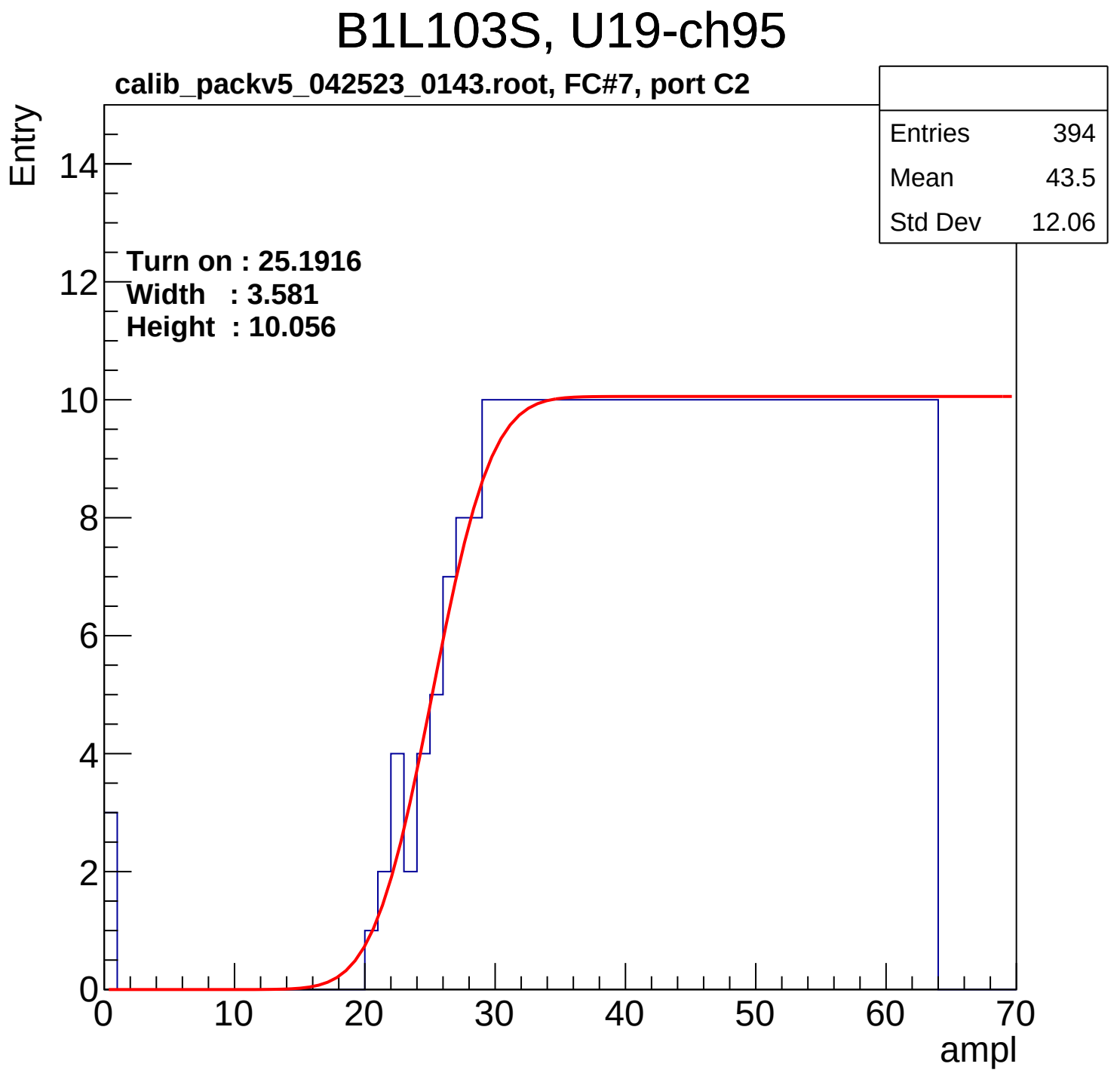
B1L103S, U19-ch95
calib_packv5_042523_0143.root, FC#7, port C2
Entries 394
Mean 43.5
Std Dev 12.06
Turn on : 25.1916
Width : 3.581
Height : 10.056
Entry
ampl
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6
8
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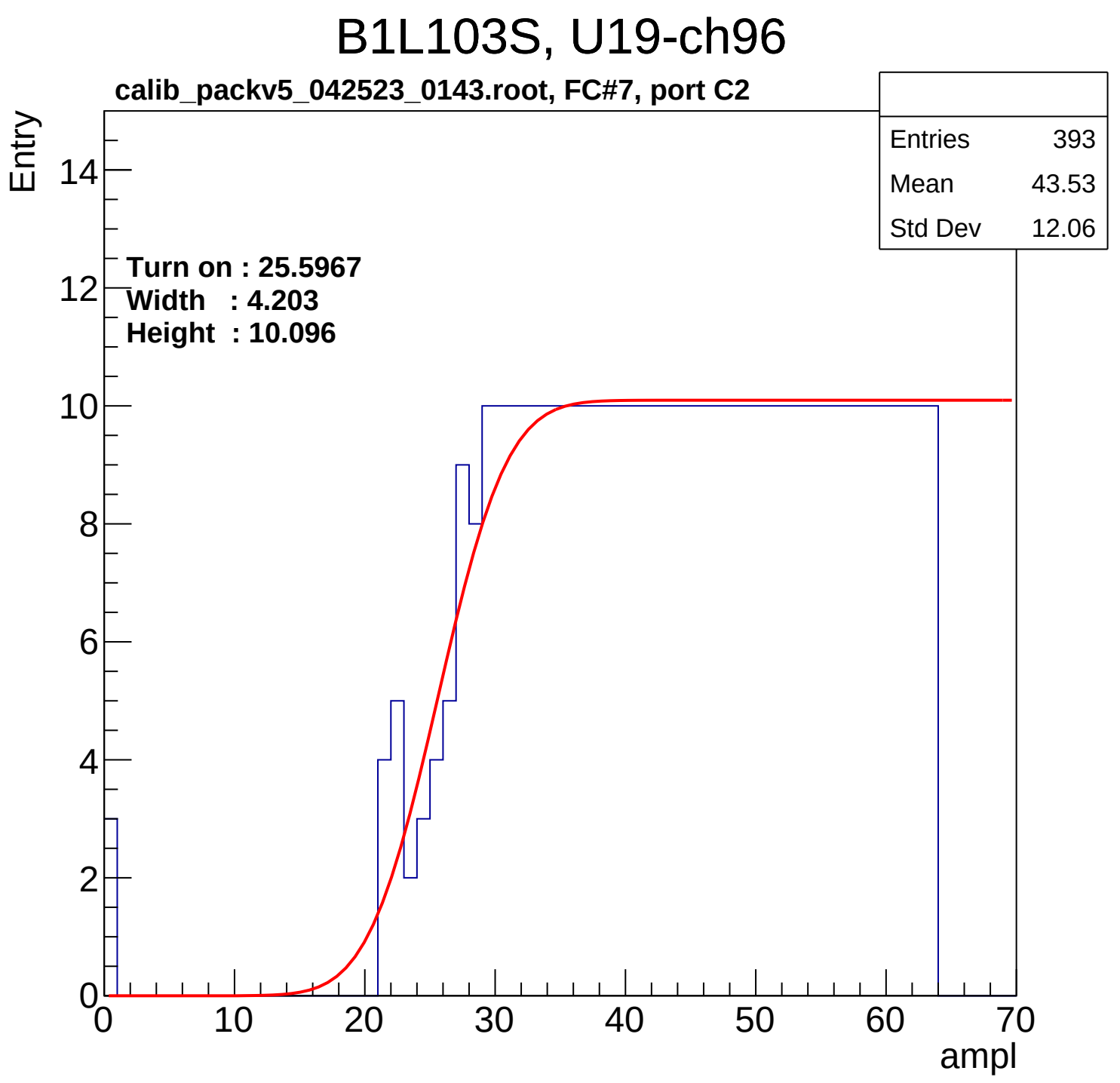
B1L103S, U19-ch96
calib_packv5_042523_0143.root, FC#7, port C2
Entries 393
Mean 43.53
Std Dev 12.06
Turn on : 25.5967
Width : 4.203
Height : 10.096
Entry
ampl
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6
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10
12
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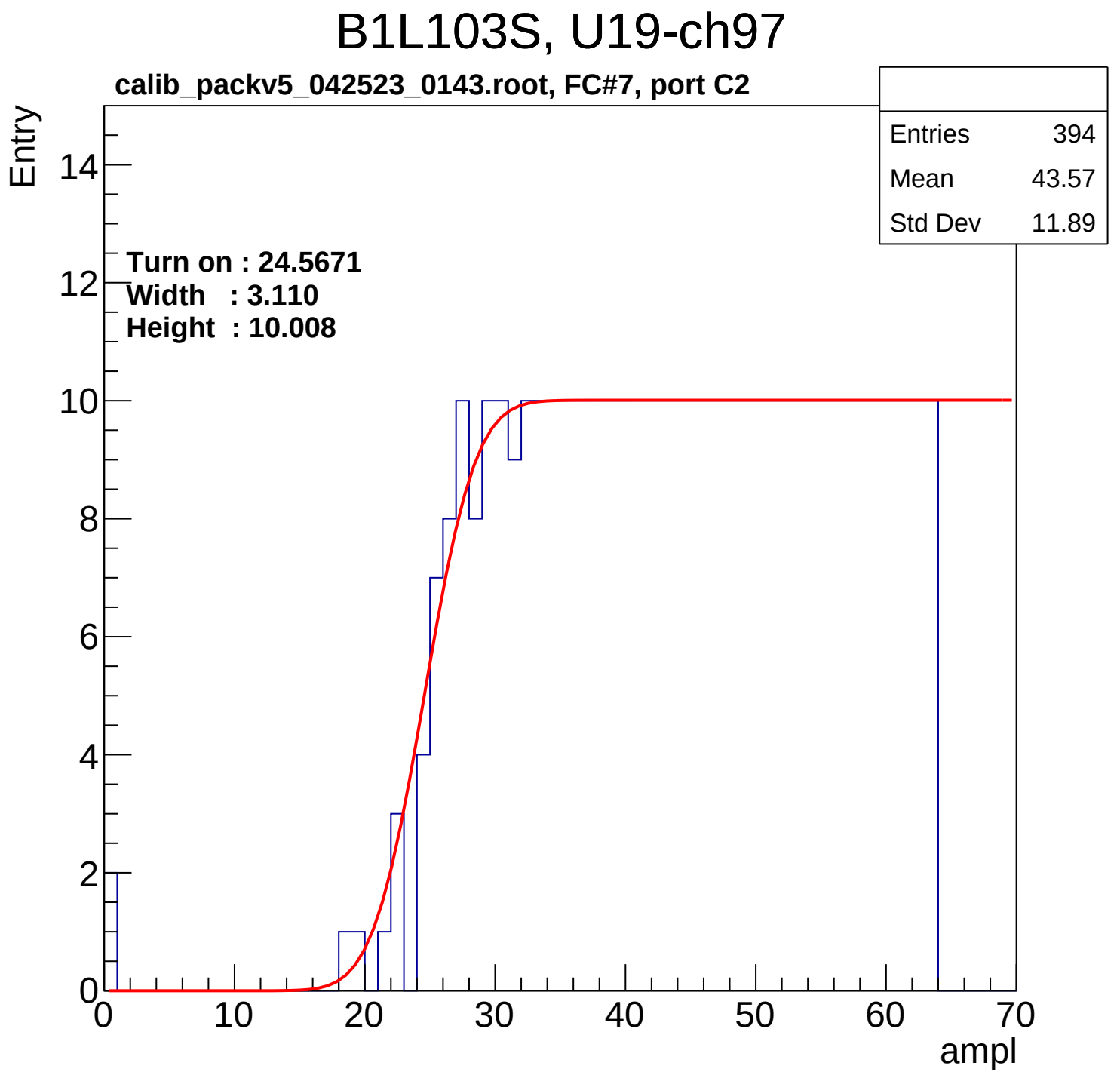
B1L103S, U19-ch97
calib_packv5_042523_0143.root, FC#7, port C2
Entries 394
Mean 43.57
Std Dev 11.89
Turn on : 24.5671
Width : 3.110
Height : 10.008
Entry
ampl
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6
8
10
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0
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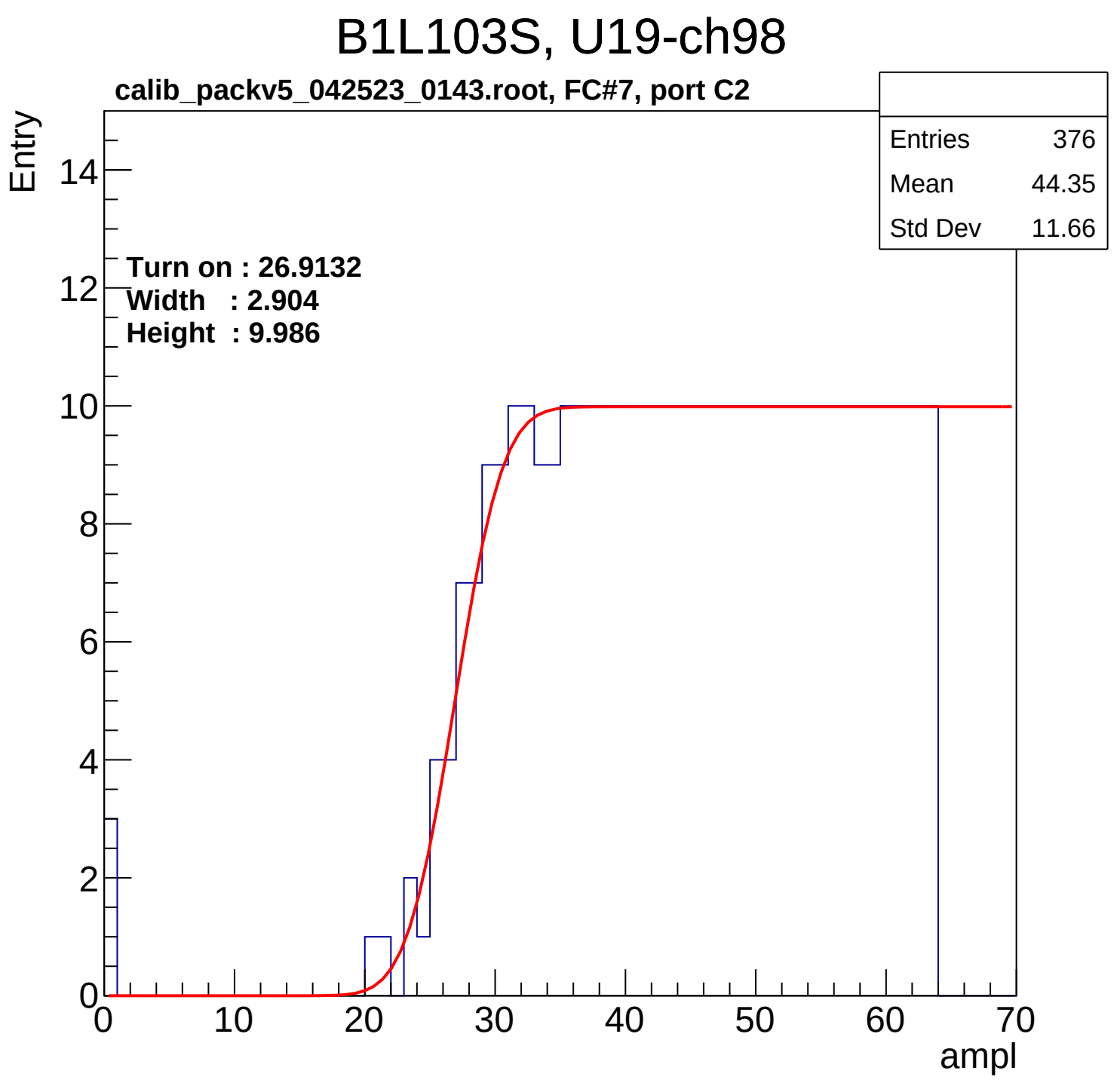
B1L103S, U19-ch98
calib_packv5_042523_0143.root, FC#7, port C2
Entries 376
Mean 44.35
Std Dev 11.66
Turn on : 26.9132
Width : 2.904
Height : 9.986
Entry
ampl
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2
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6
8
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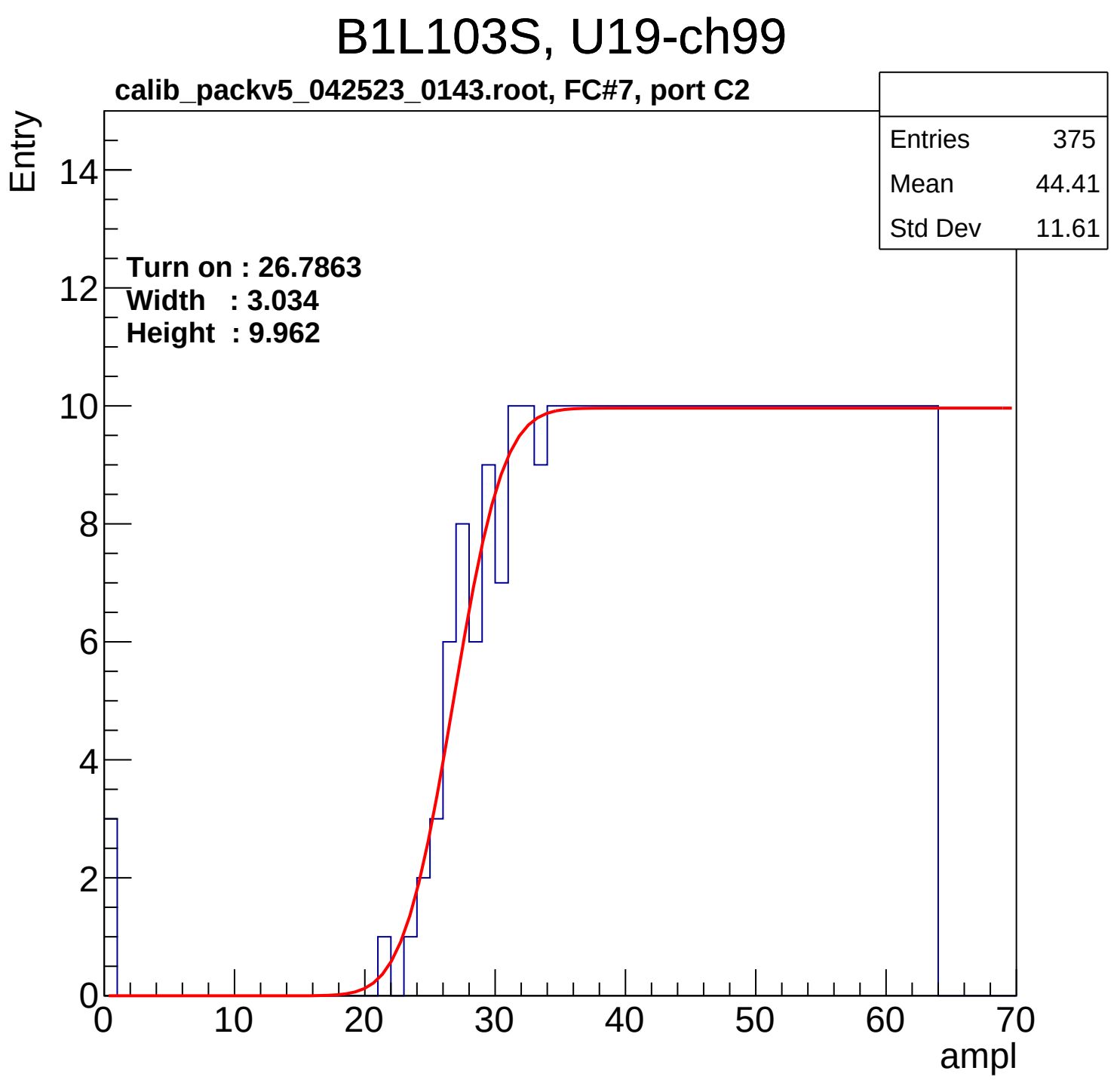
B1L103S, U19-ch99
calib_packv5_042523_0143.root, FC#7, port C2
Entries 375
Mean 44.41
Std Dev 11.61
Turn on : 26.7863
Width : 3.034
Height : 9.962
Entry
ampl
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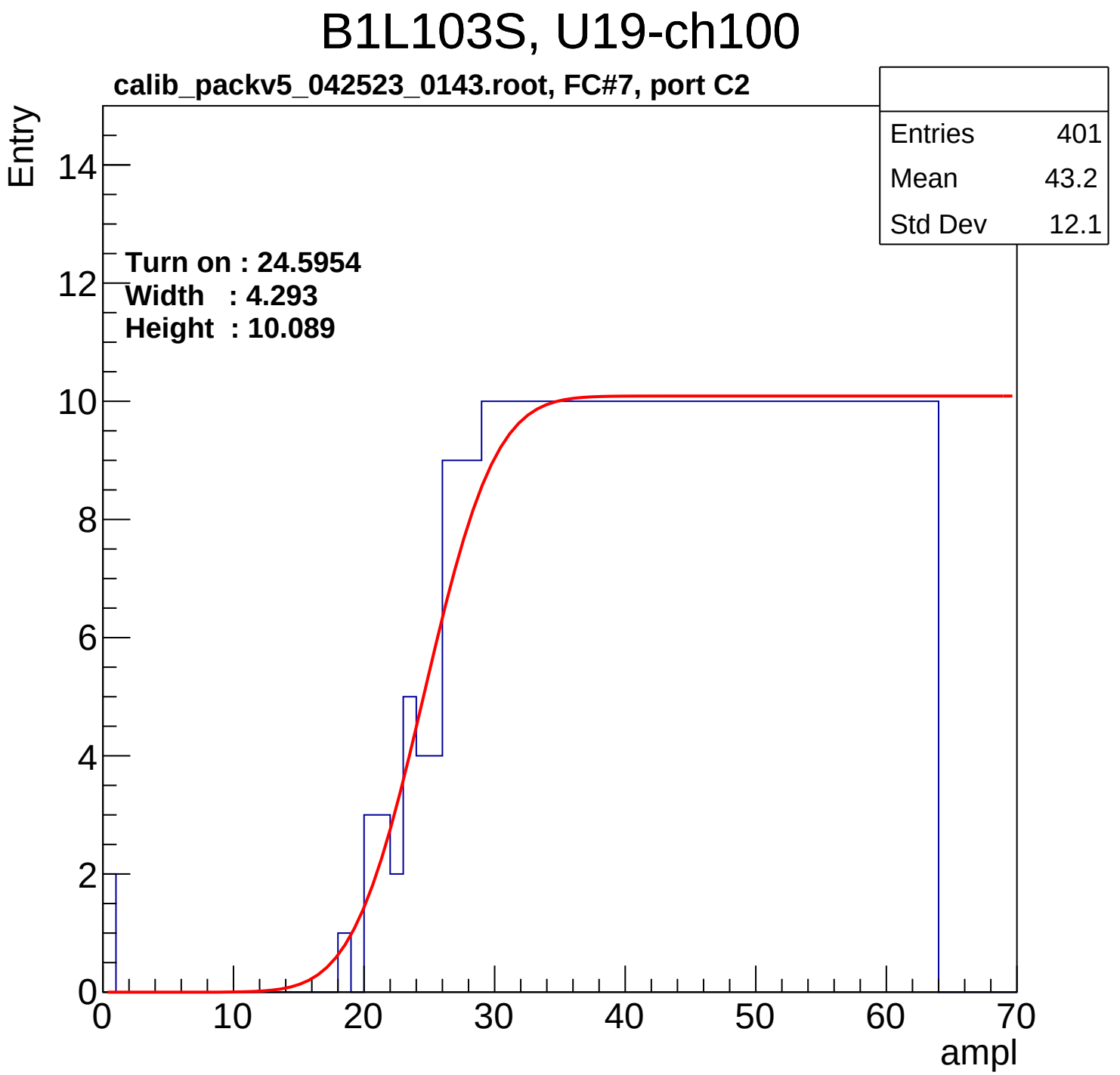
B1L103S, U19-ch100
calib_packv5_042523_0143.root, FC#7, port C2
Entries 401
Mean 43.2
Std Dev 12.1
Turn on : 24.5954
Width : 4.293
Height : 10.089
Entry
ampl
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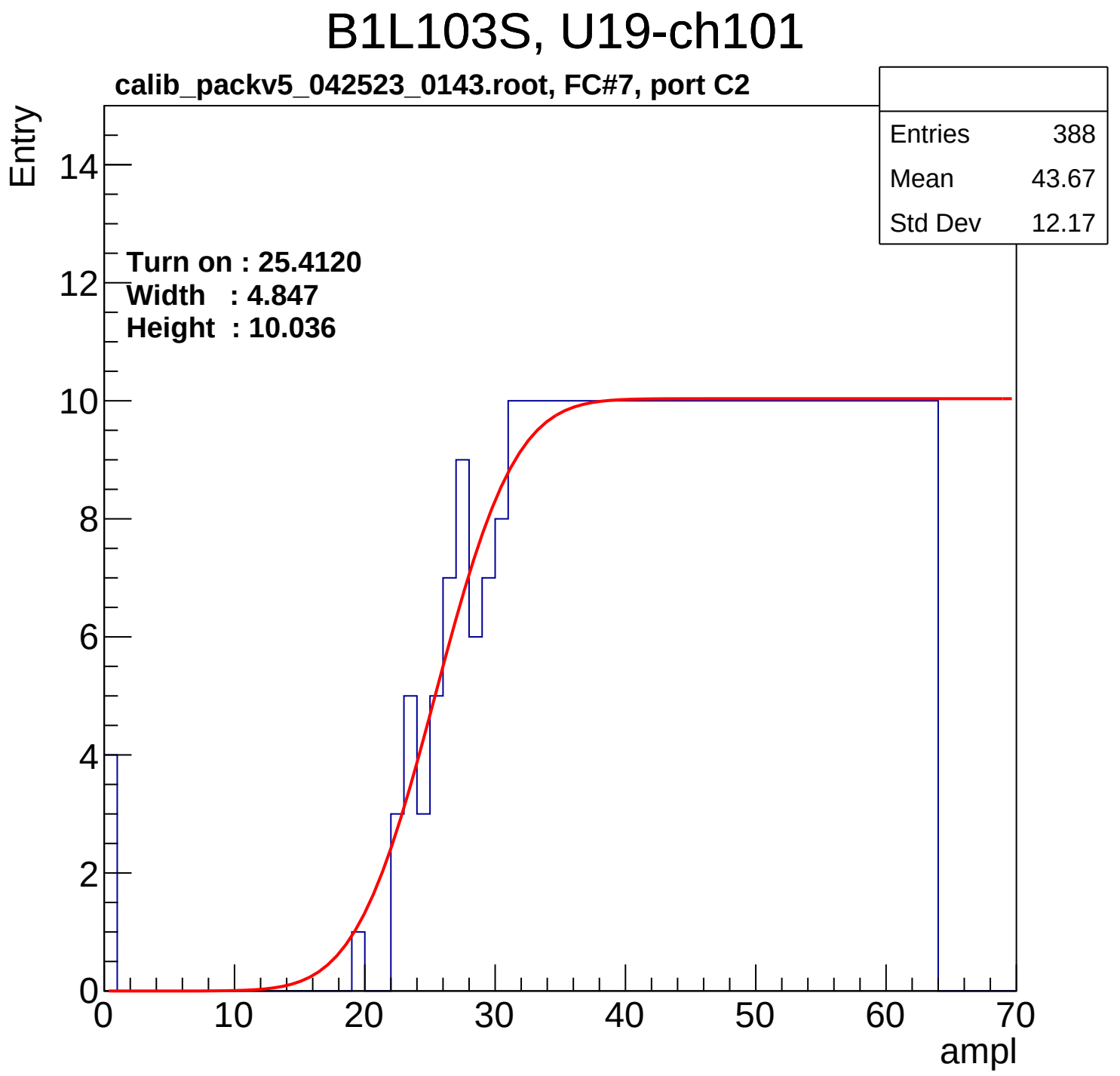
B1L103S, U19-ch101
calib_packv5_042523_0143.root, FC#7, port C2
Entries 388
Mean 43.67
Std Dev 12.17
Turn on : 25.4120
Width : 4.847
Height : 10.036
Entry
ampl
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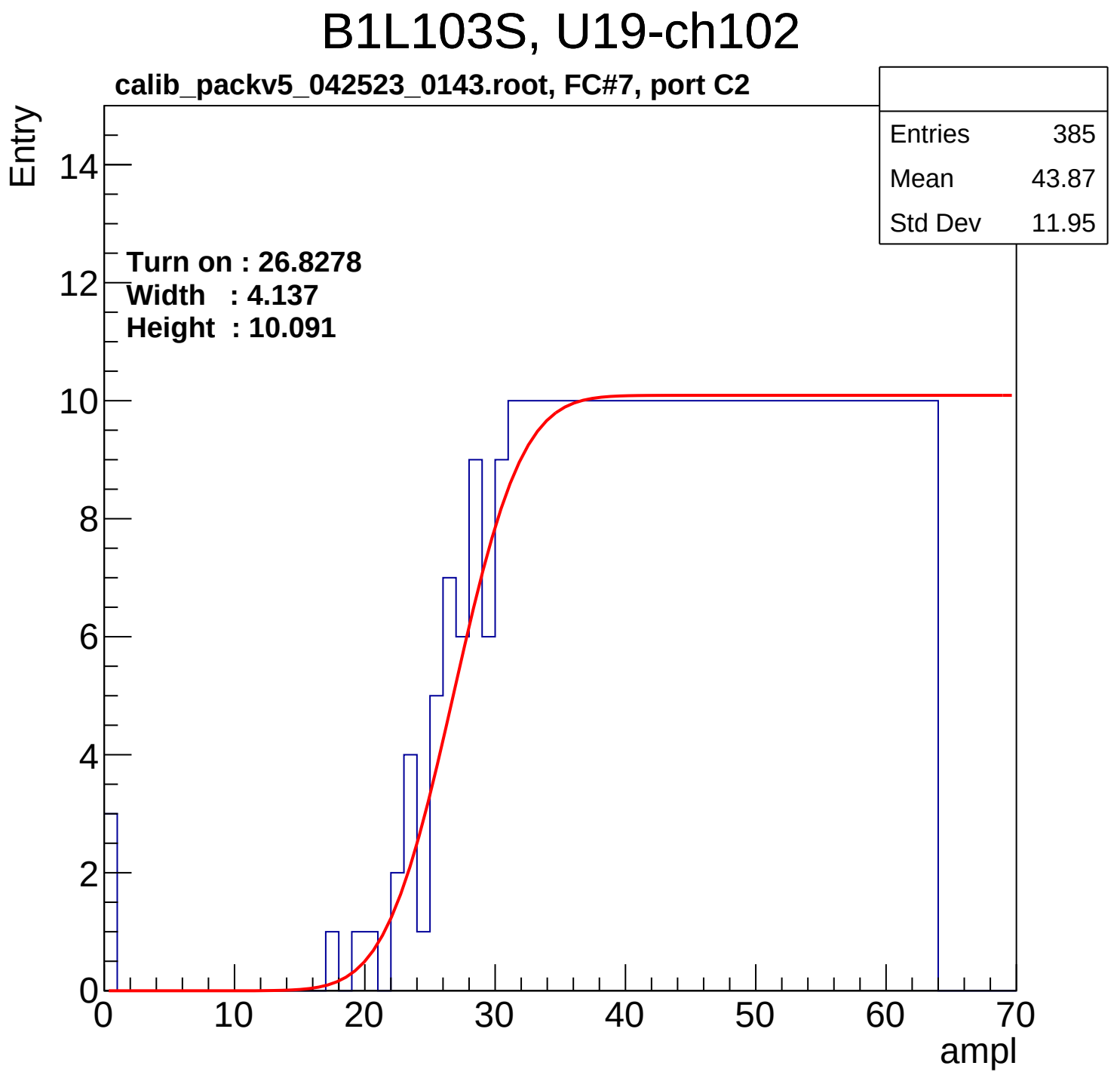
B1L103S, U19-ch102
calib_packv5_042523_0143.root, FC#7, port C2
Entries 385
Mean 43.87
Std Dev 11.95
Turn on : 26.8278
Width : 4.137
Height : 10.091
Entry
ampl
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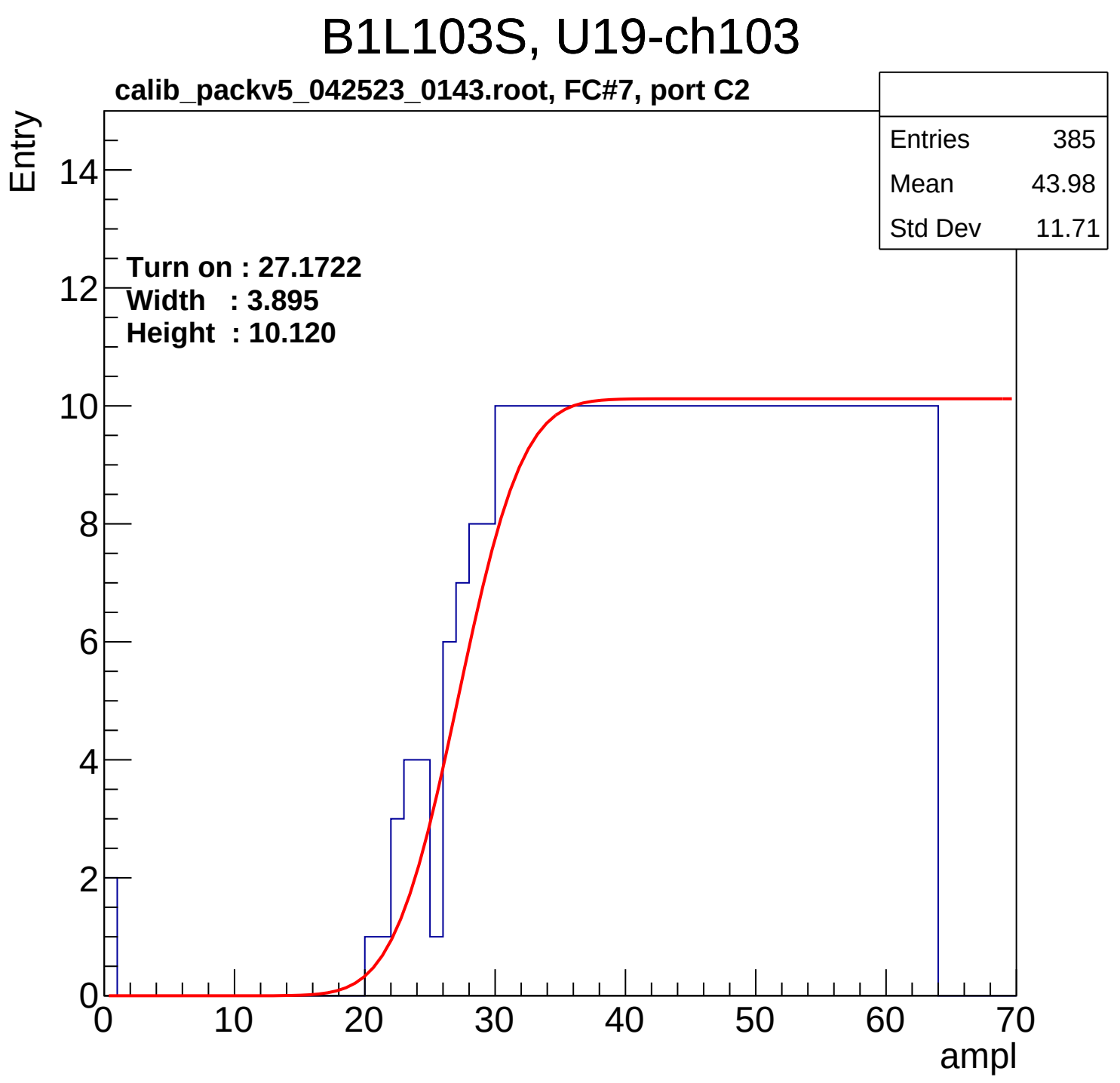
B1L103S, U19-ch103
calib_packv5_042523_0143.root, FC#7, port C2
Entries 385
Mean 43.98
Std Dev 11.71
Turn on : 27.1722
Width : 3.895
Height : 10.120
Entry
ampl
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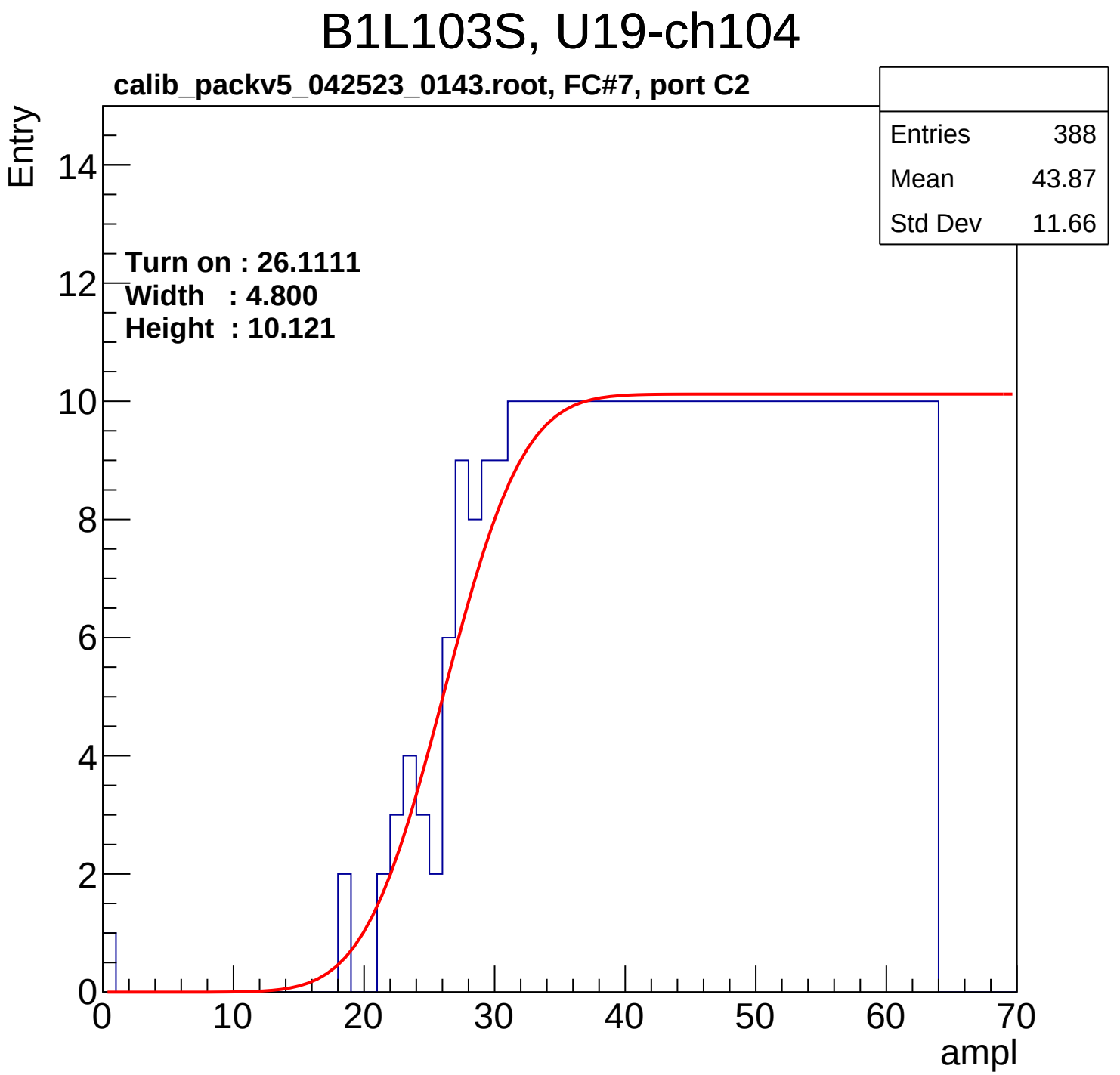
B1L103S, U19-ch104
calib_packv5_042523_0143.root, FC#7, port C2
Entries 388
Mean 43.87
Std Dev 11.66
Turn on : 26.1111
Width : 4.800
Height : 10.121
Entry
ampl
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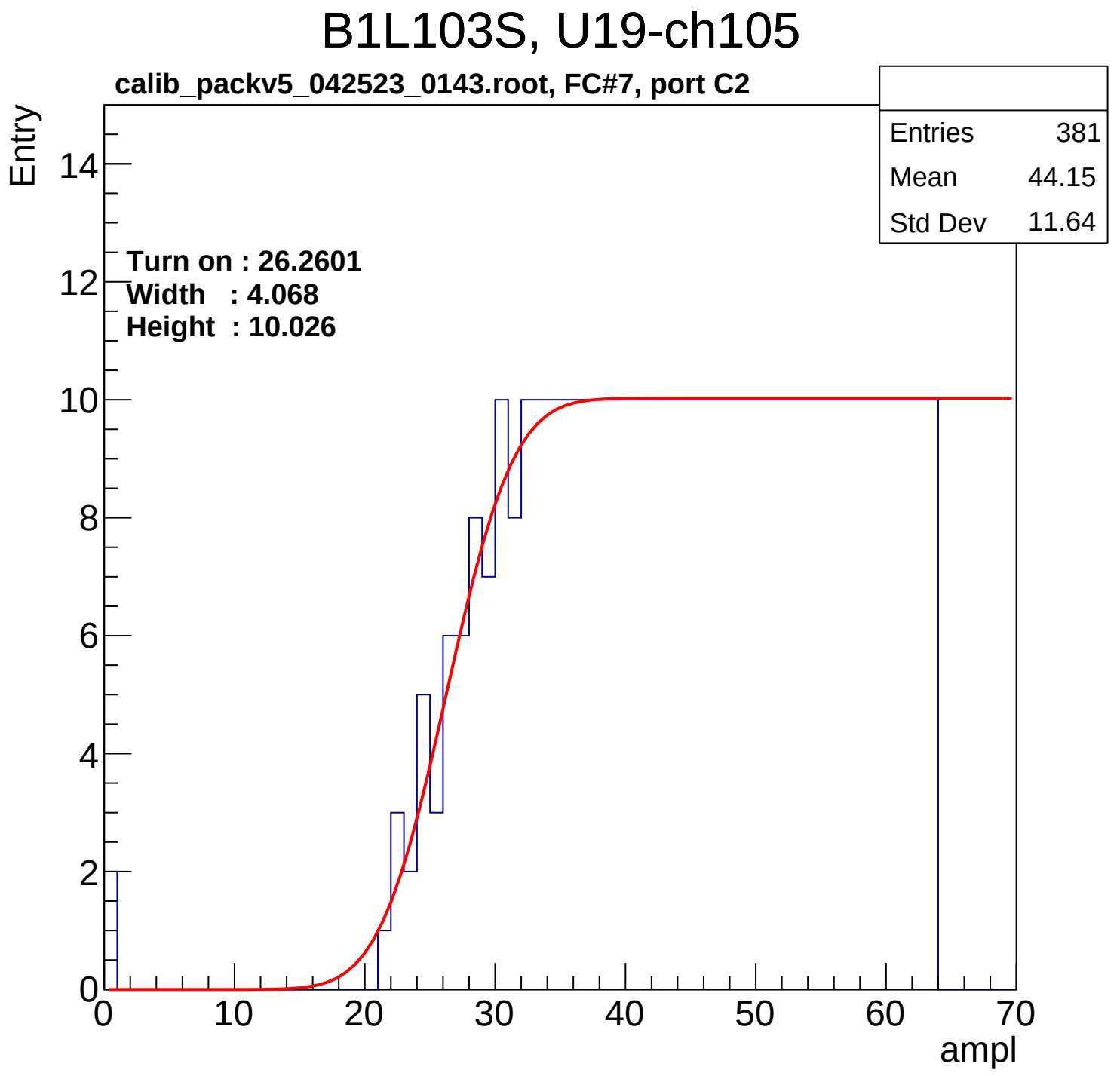
B1L103S, U19-ch105
calib_packv5_042523_0143.root, FC#7, port C2
Entries 381
Mean 44.15
Std Dev 11.64
Turn on : 26.2601
Width : 4.068
Height : 10.026
Entry
ampl
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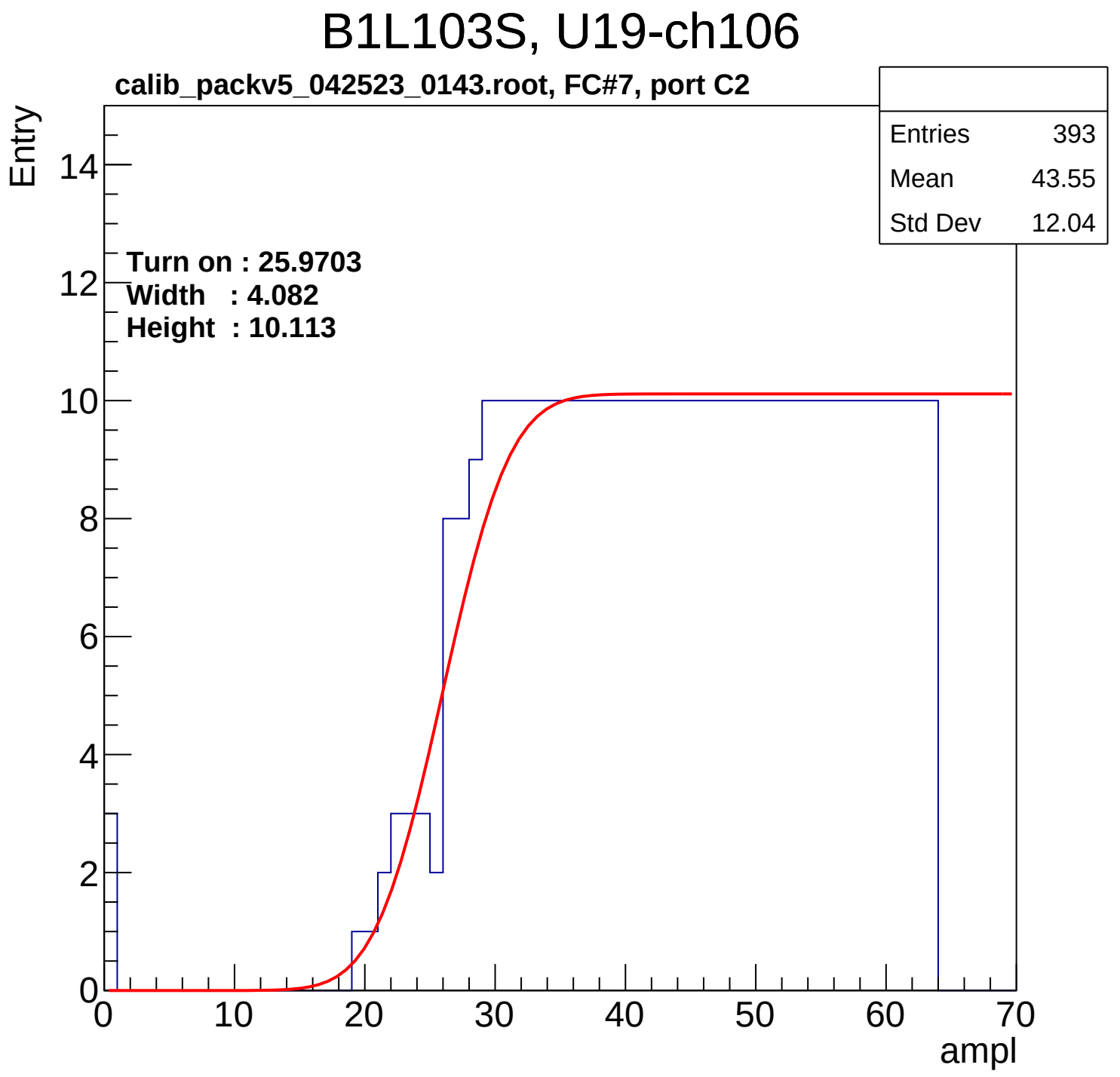
B1L103S, U19-ch106
calib_packv5_042523_0143.root, FC#7, port C2
Entries 393
Mean 43.55
Std Dev 12.04
Turn on : 25.9703
Width : 4.082
Height : 10.113
Entry
ampl
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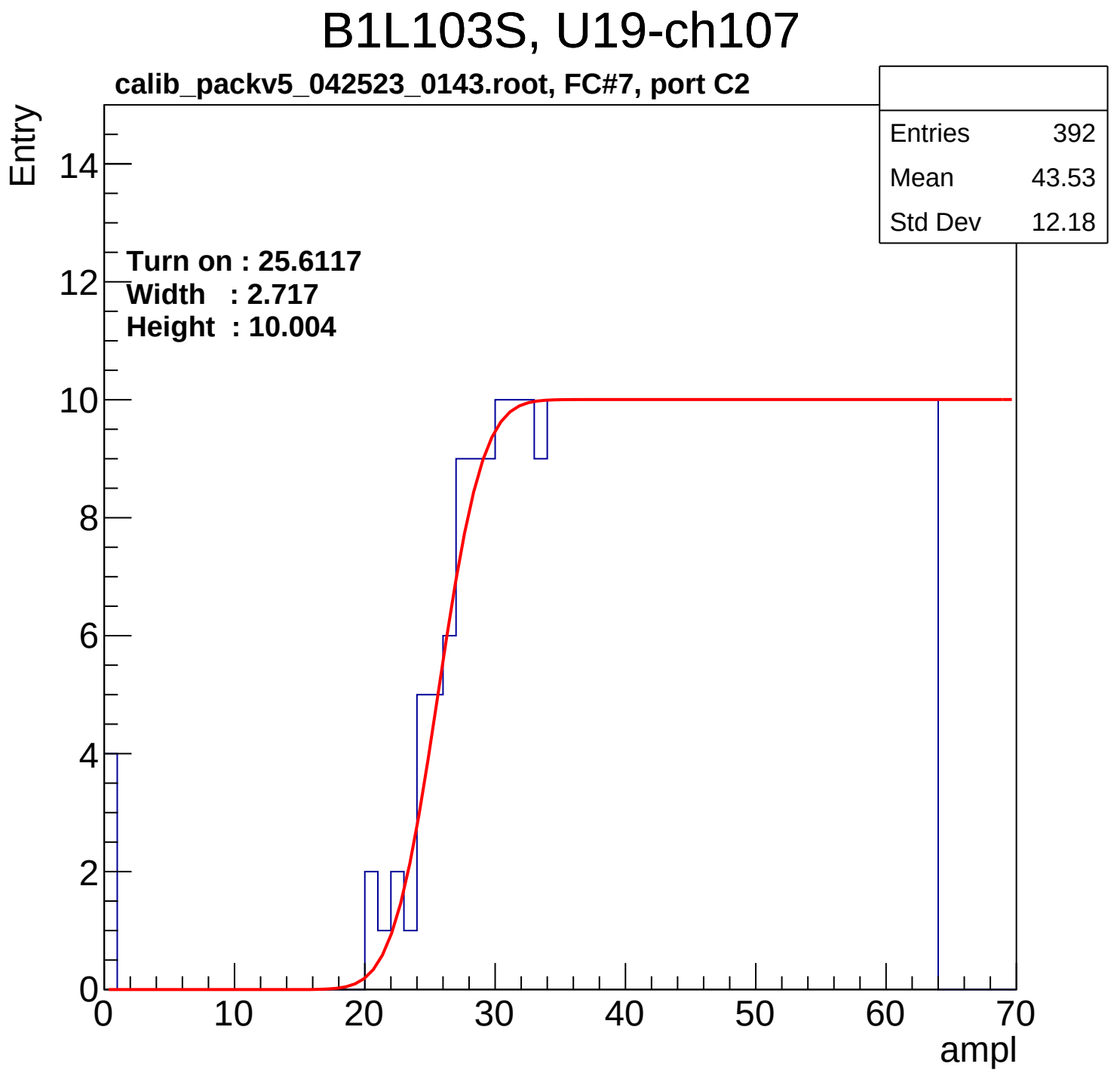
B1L103S, U19-ch107
calib_packv5_042523_0143.root, FC#7, port C2
Entries 392
Mean 43.53
Std Dev 12.18
Turn on : 25.6117
Width : 2.717
Height : 10.004
Entry
ampl
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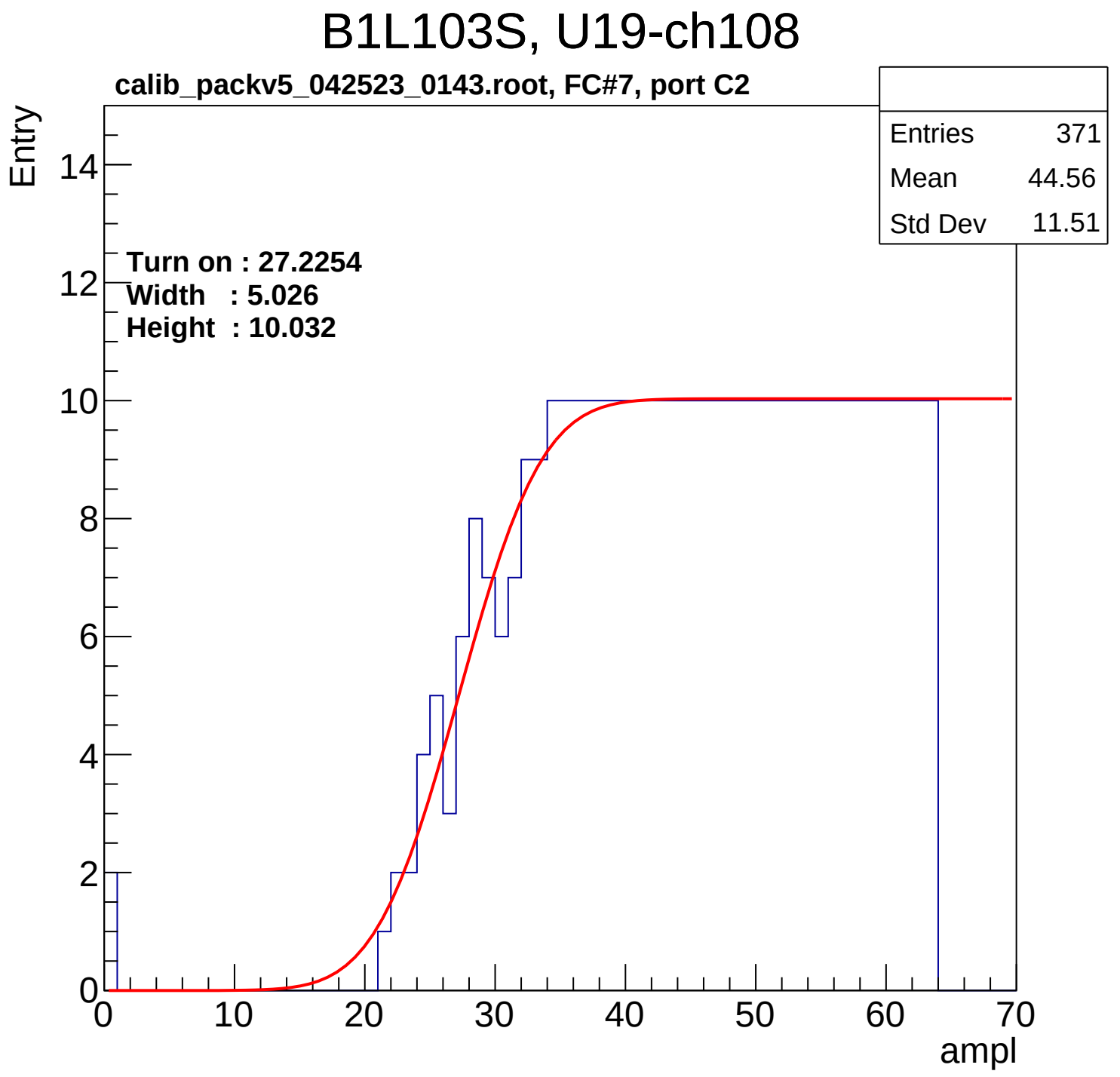
B1L103S, U19-ch108
calib_packv5_042523_0143.root, FC#7, port C2
Entries 371
Mean 44.56
Std Dev 11.51
Turn on : 27.2254
Width : 5.026
Height : 10.032
Entry
ampl
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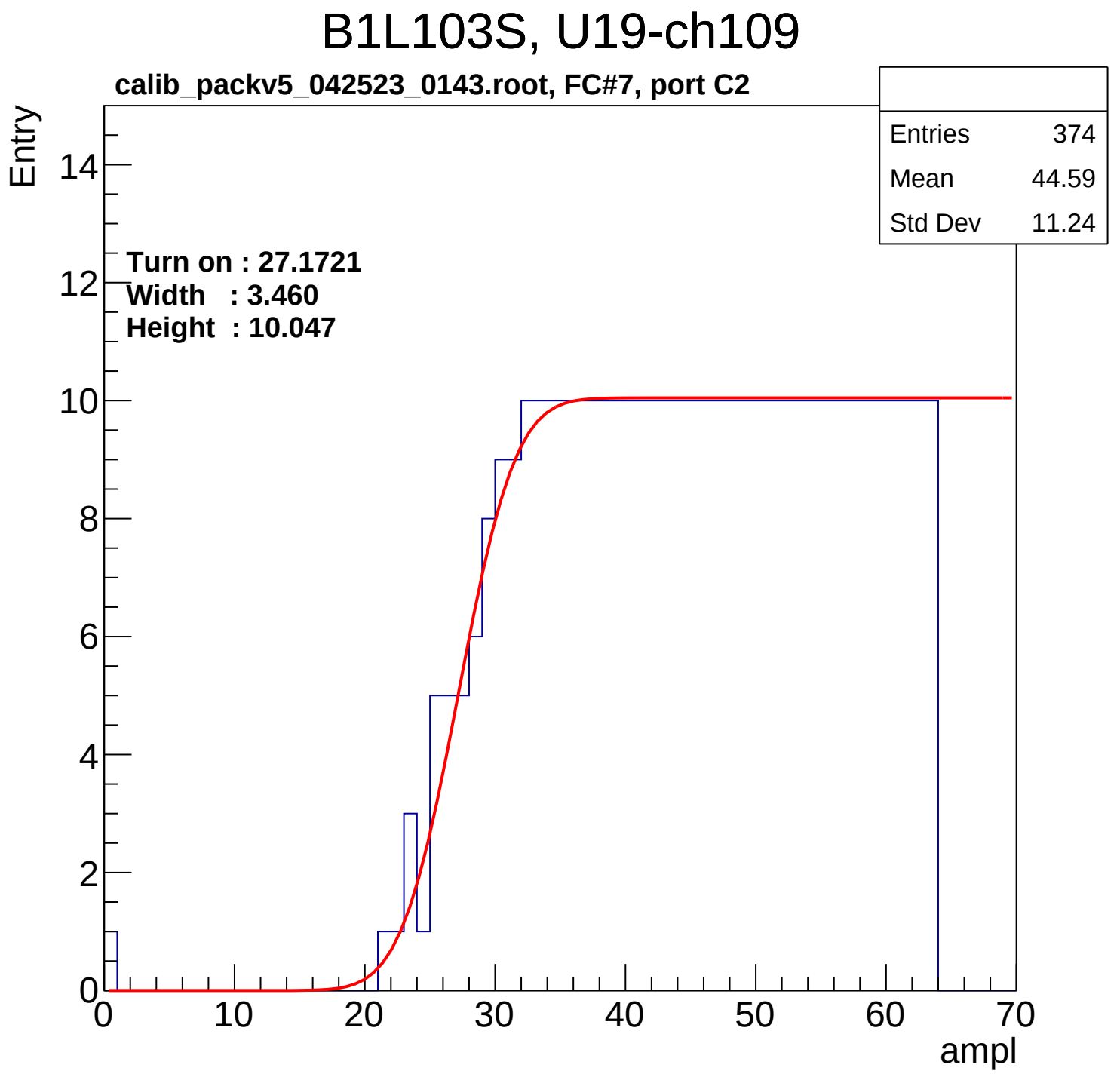
B1L103S, U19-ch109
calib_packv5_042523_0143.root, FC#7, port C2
Entries 374
Mean 44.59
Std Dev 11.24
Turn on : 27.1721
Width : 3.460
Height : 10.047
Entry
ampl
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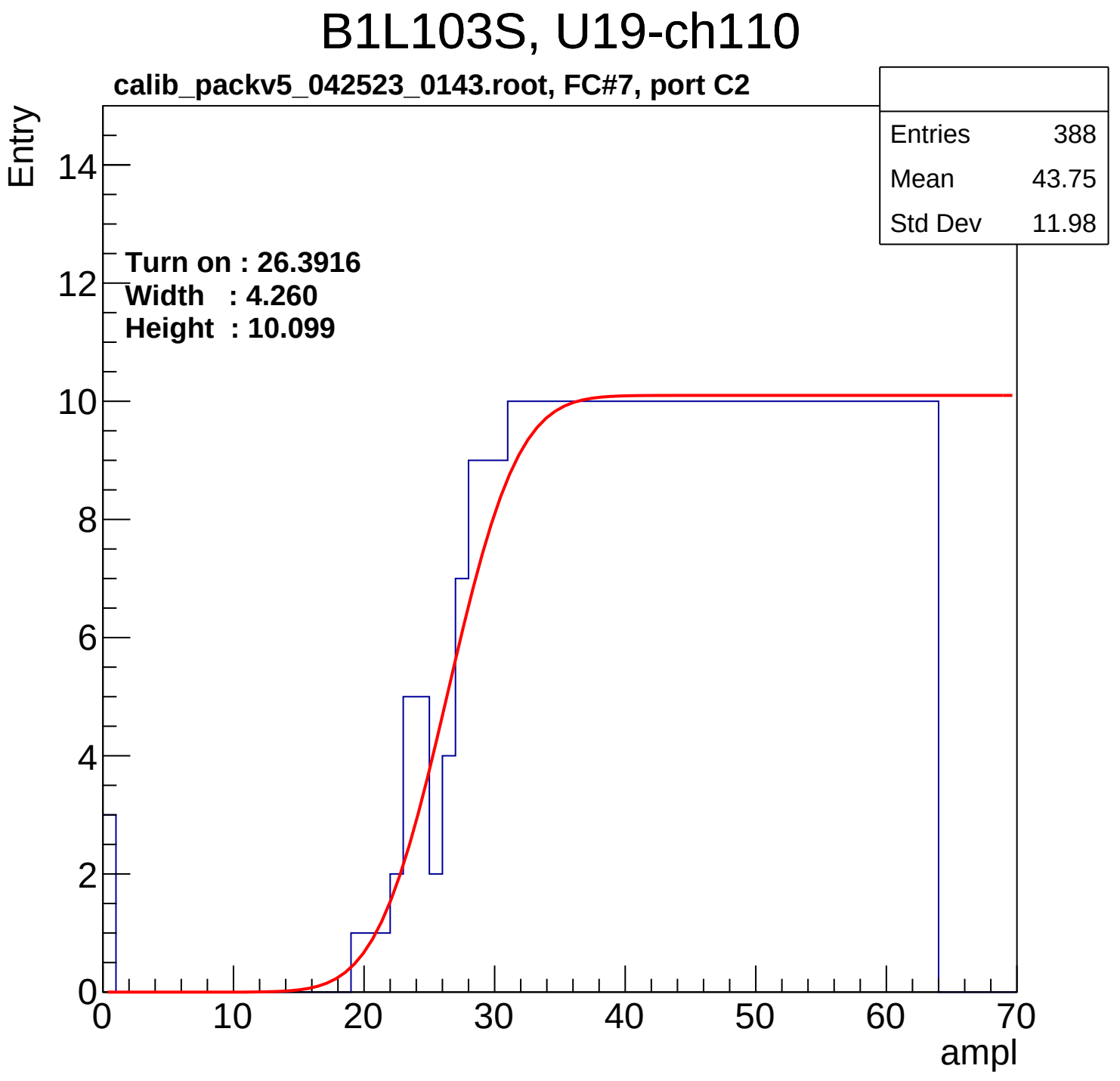
B1L103S, U19-ch110
calib_packv5_042523_0143.root, FC#7, port C2
Entries 388
Mean 43.75
Std Dev 11.98
Turn on : 26.3916
Width : 4.260
Height : 10.099
Entry
ampl
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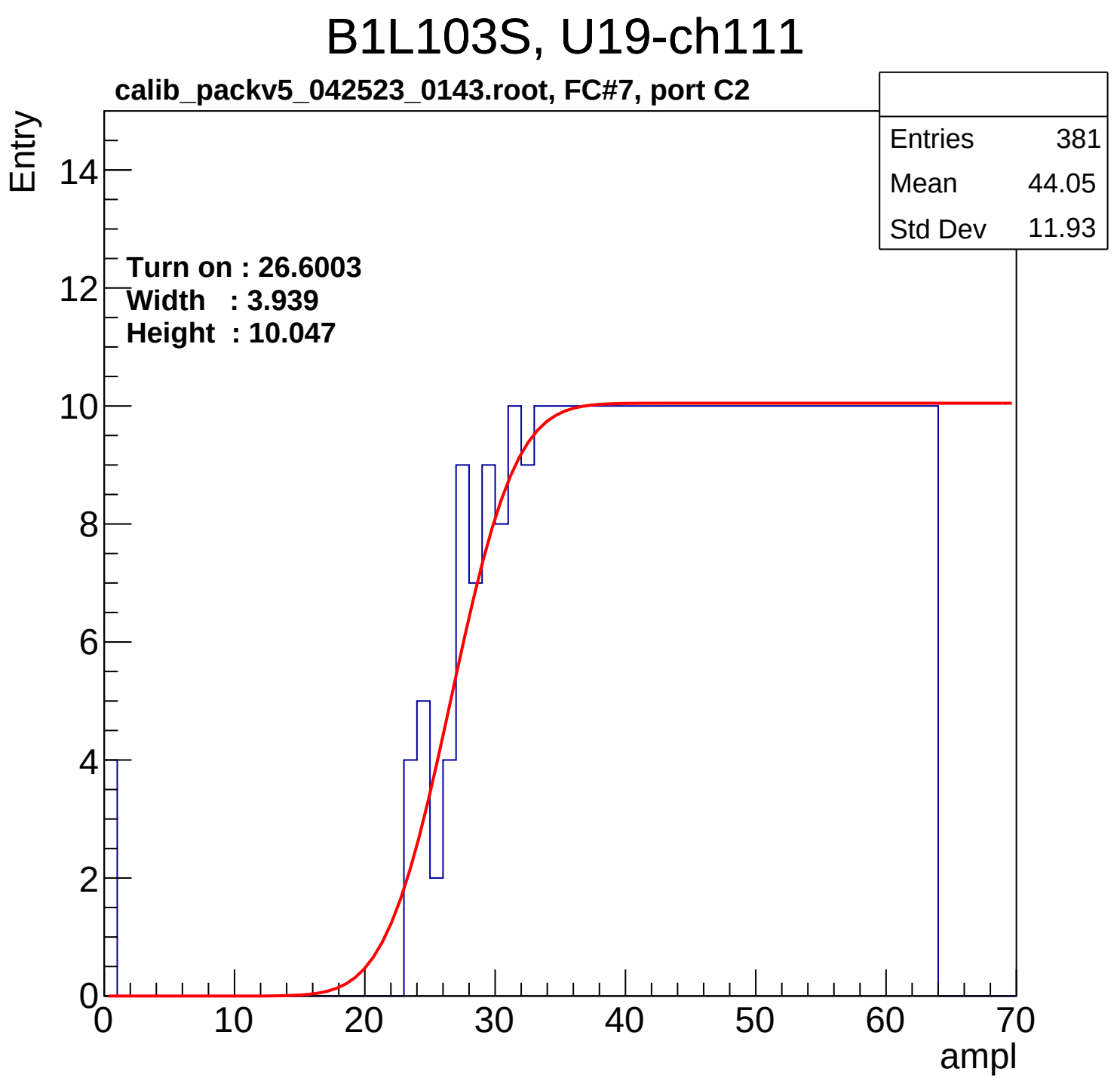
B1L103S, U19-ch111
calib_packv5_042523_0143.root, FC#7, port C2
Entries 381
Mean 44.05
Std Dev 11.93
Turn on : 26.6003
Width : 3.939
Height : 10.047
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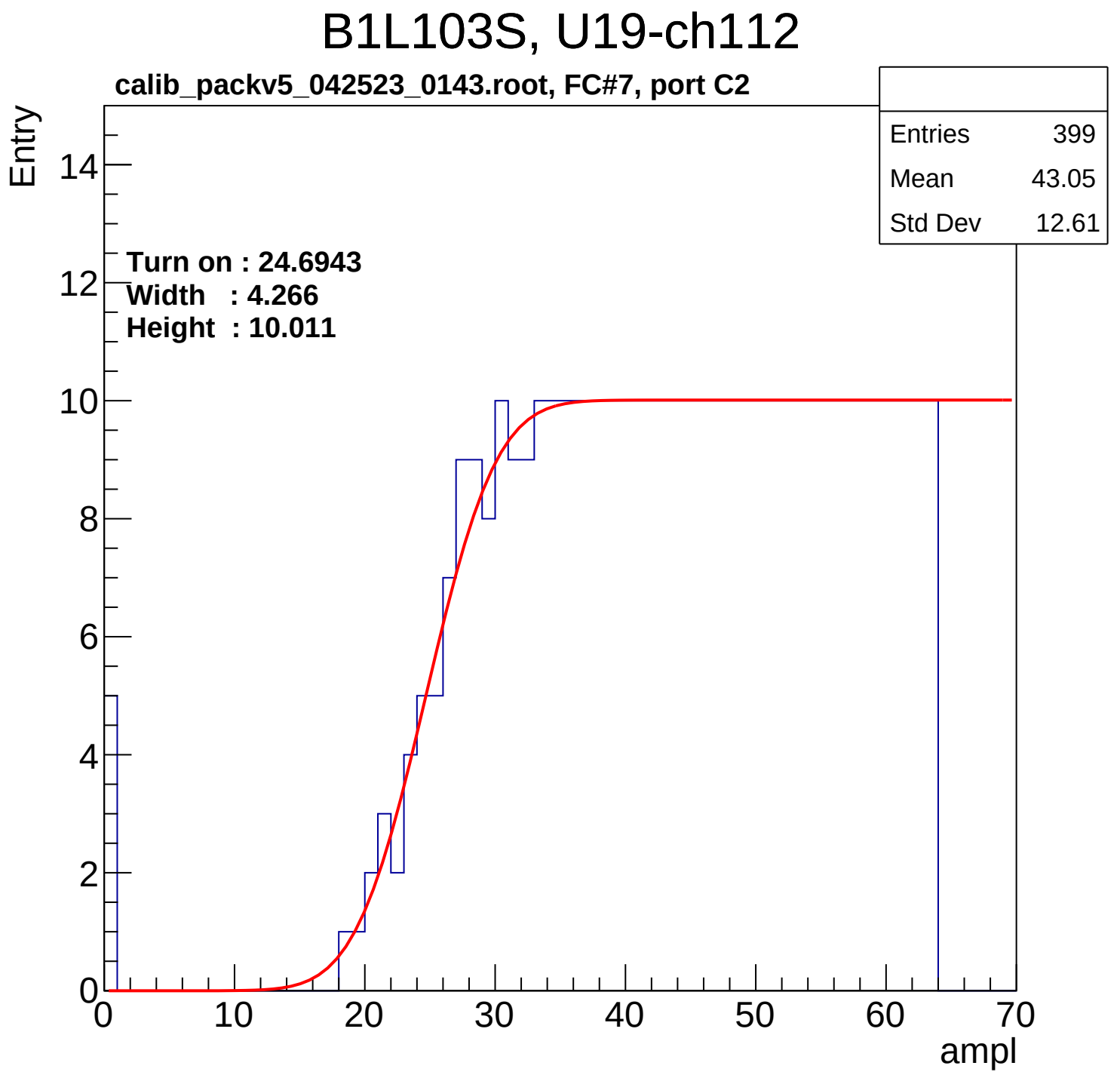
B1L103S, U19-ch112
calib_packv5_042523_0143.root, FC#7, port C2
Entries 399
Mean 43.05
Std Dev 12.61
Turn on : 24.6943
Width : 4.266
Height : 10.011
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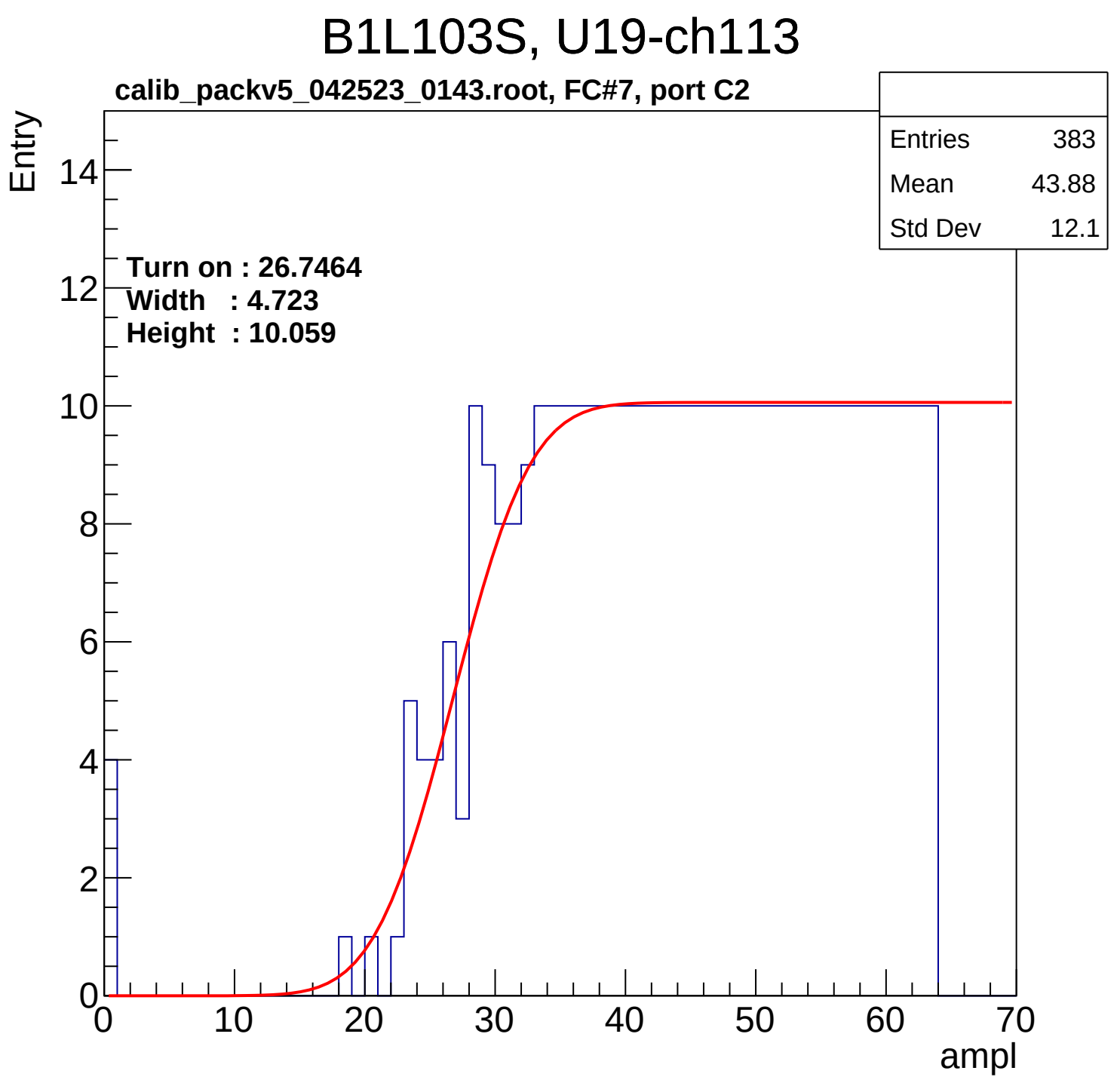
B1L103S, U19-ch113
calib_packv5_042523_0143.root, FC#7, port C2
Entries 383
Mean 43.88
Std Dev 12.1
Turn on : 26.7464
Width : 4.723
Height : 10.059
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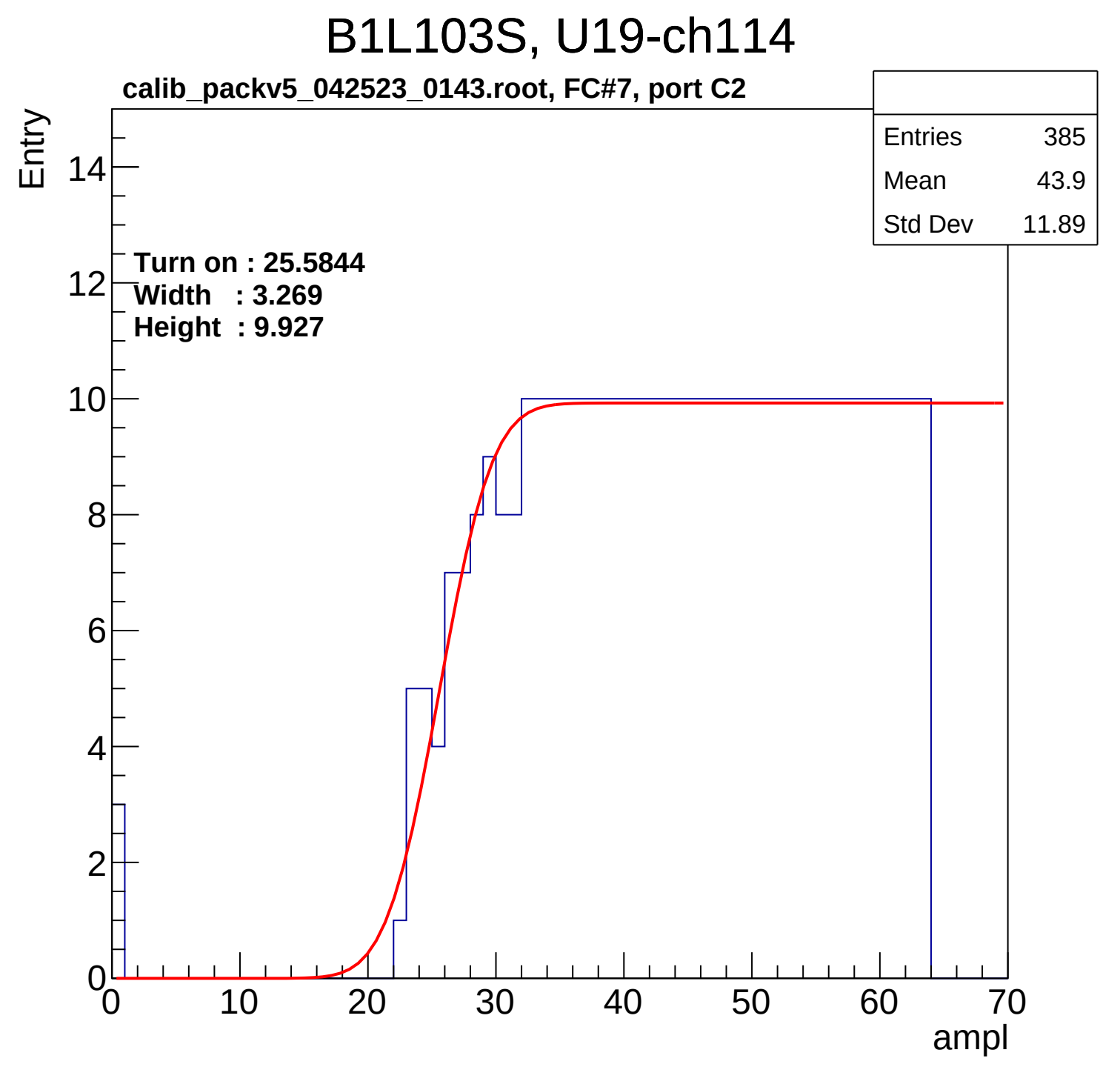
B1L103S, U19-ch114
calib_packv5_042523_0143.root, FC#7, port C2
Entries 385
Mean 43.9
Std Dev 11.89
Turn on : 25.5844
Width : 3.269
Height : 9.927
Entry
ampl
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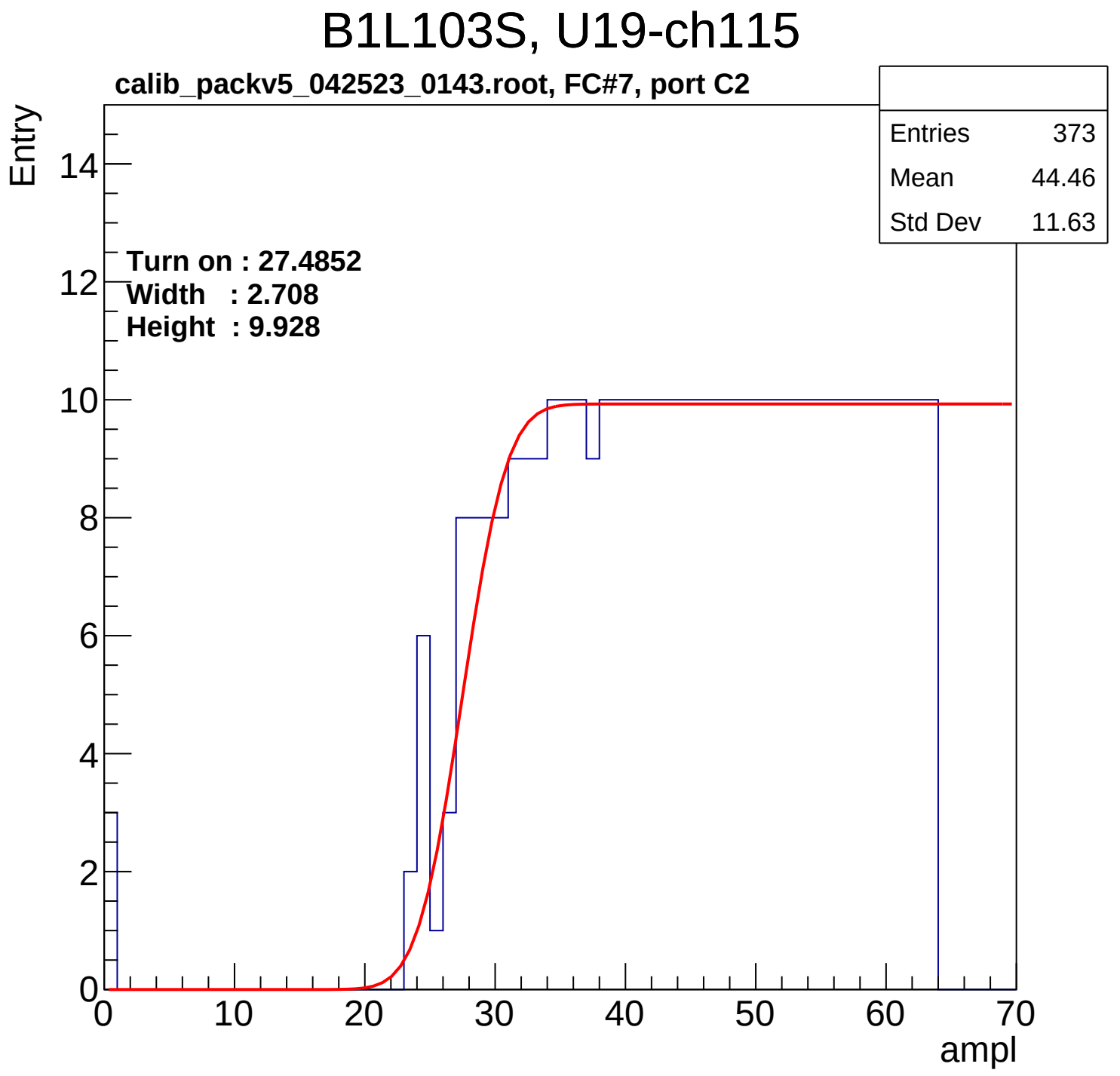
B1L103S, U19-ch115
calib_packv5_042523_0143.root, FC#7, port C2
Entries 373
Mean 44.46
Std Dev 11.63
Turn on : 27.4852
Width : 2.708
Height : 9.928
Entry
ampl
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6
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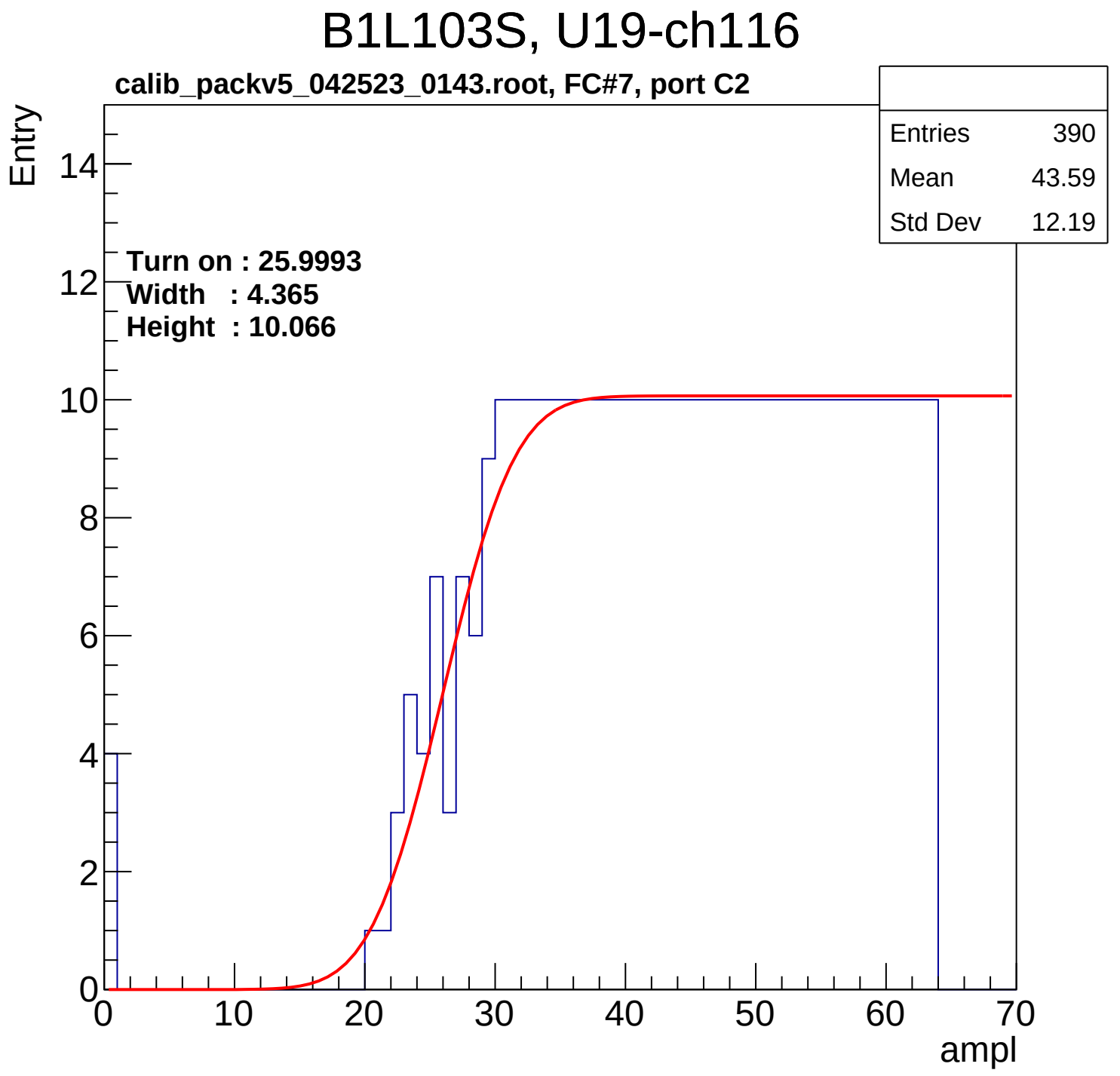
B1L103S, U19-ch116
calib_packv5_042523_0143.root, FC#7, port C2
Entries 390
Mean 43.59
Std Dev 12.19
Turn on : 25.9993
Width : 4.365
Height : 10.066
Entry
ampl
0
2
4
6
8
10
12
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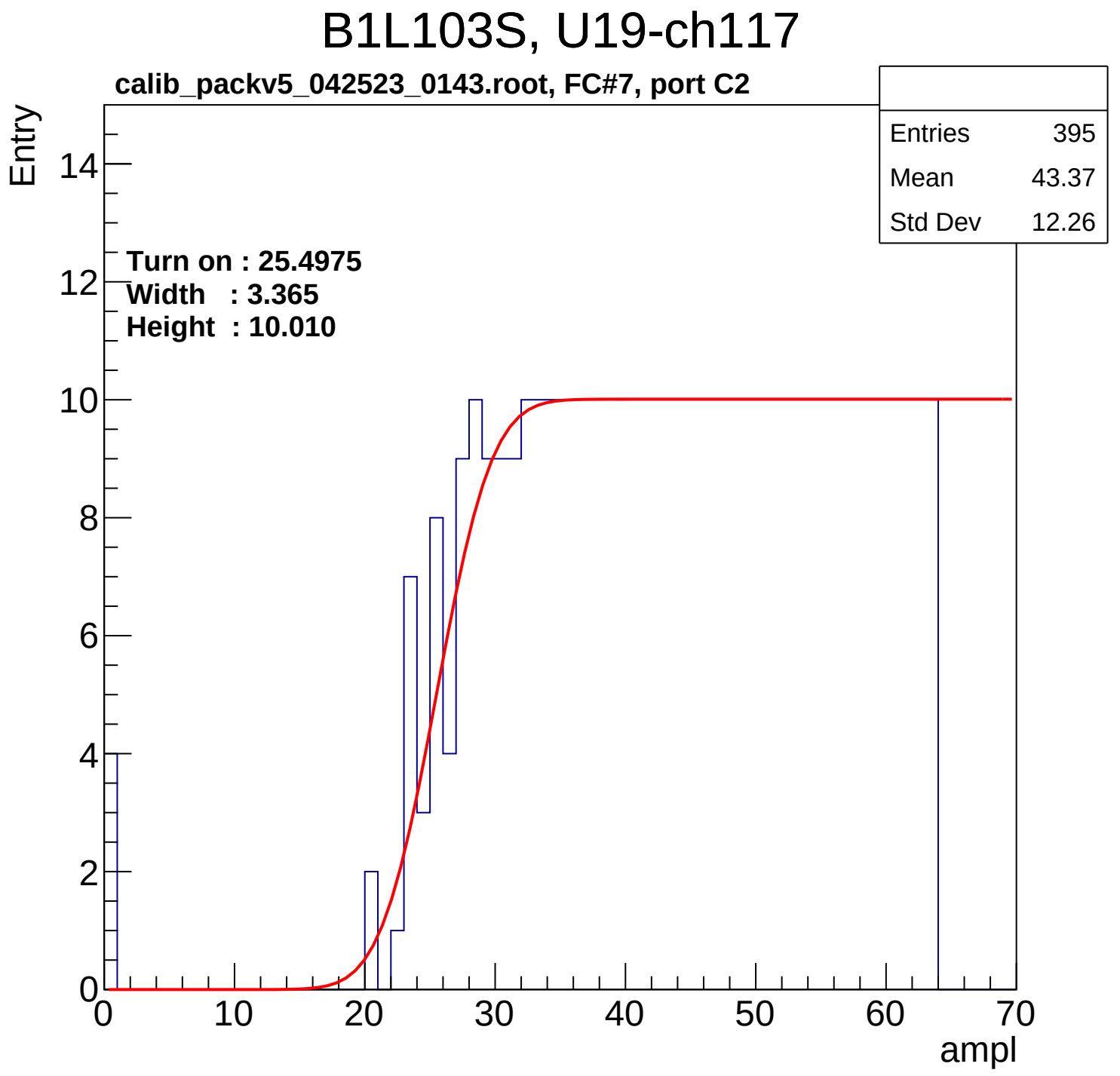
B1L103S, U19-ch117
calib_packv5_042523_0143.root, FC#7, port C2
Entries 395
Mean 43.37
Std Dev 12.26
Turn on : 25.4975
Width : 3.365
Height : 10.010
Entry
ampl
0
2
4
6
8
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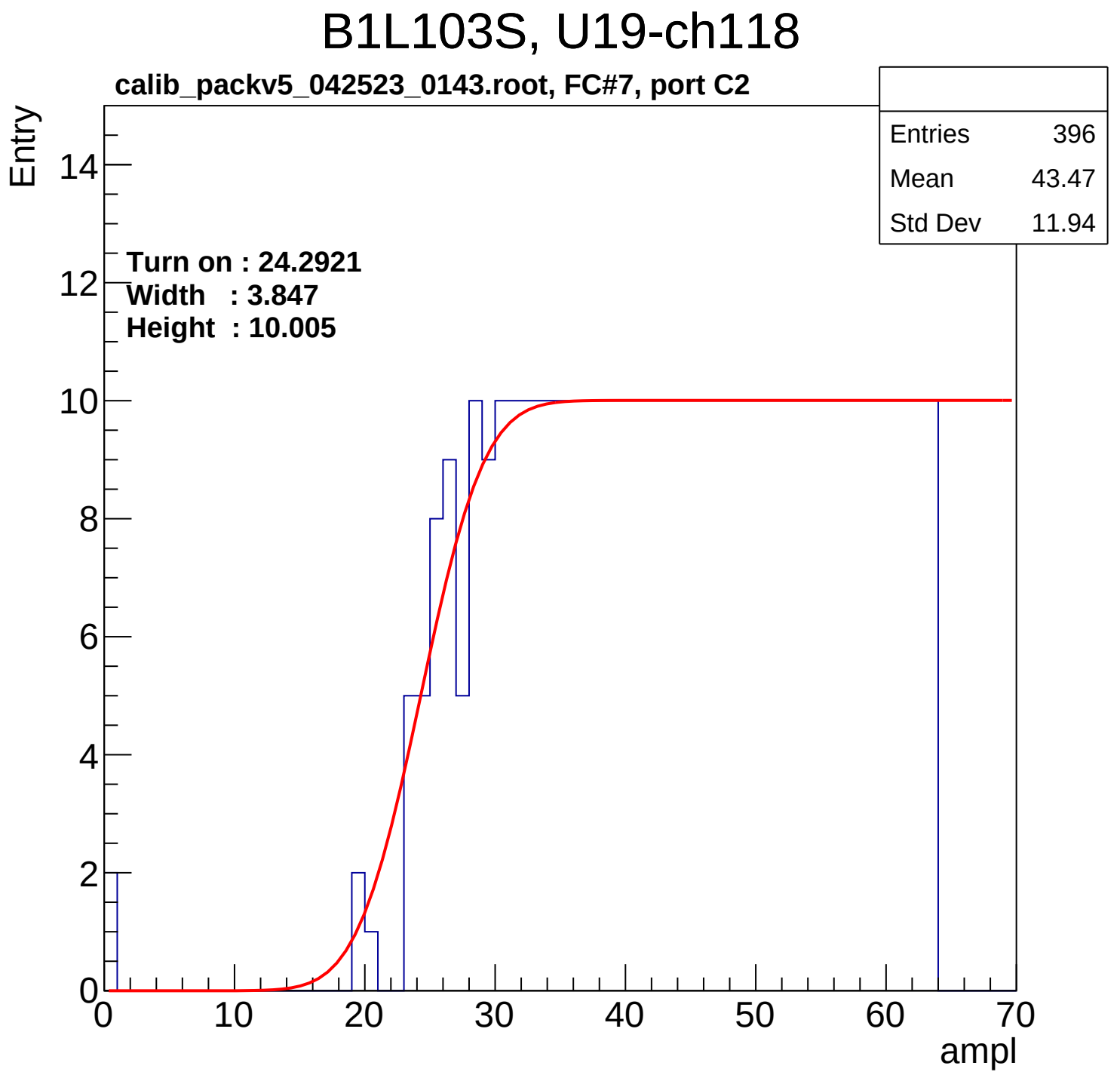
B1L103S, U19-ch118
calib_packv5_042523_0143.root, FC#7, port C2
Entries 396
Mean 43.47
Std Dev 11.94
Turn on : 24.2921
Width : 3.847
Height : 10.005
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
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60
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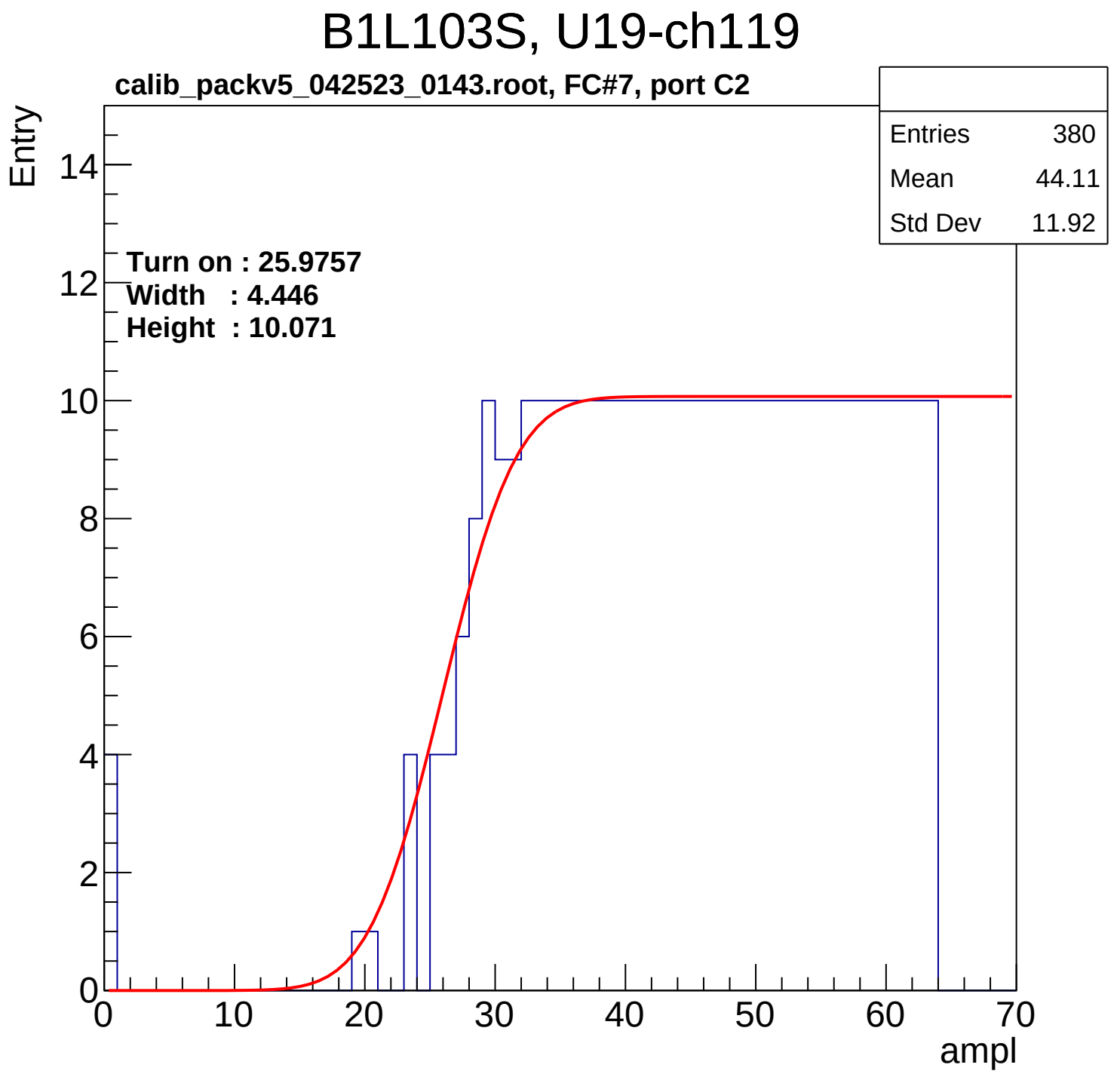
B1L103S, U19-ch119
calib_packv5_042523_0143.root, FC#7, port C2
Entries 380
Mean 44.11
Std Dev 11.92
Turn on : 25.9757
Width : 4.446
Height : 10.071
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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40
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60
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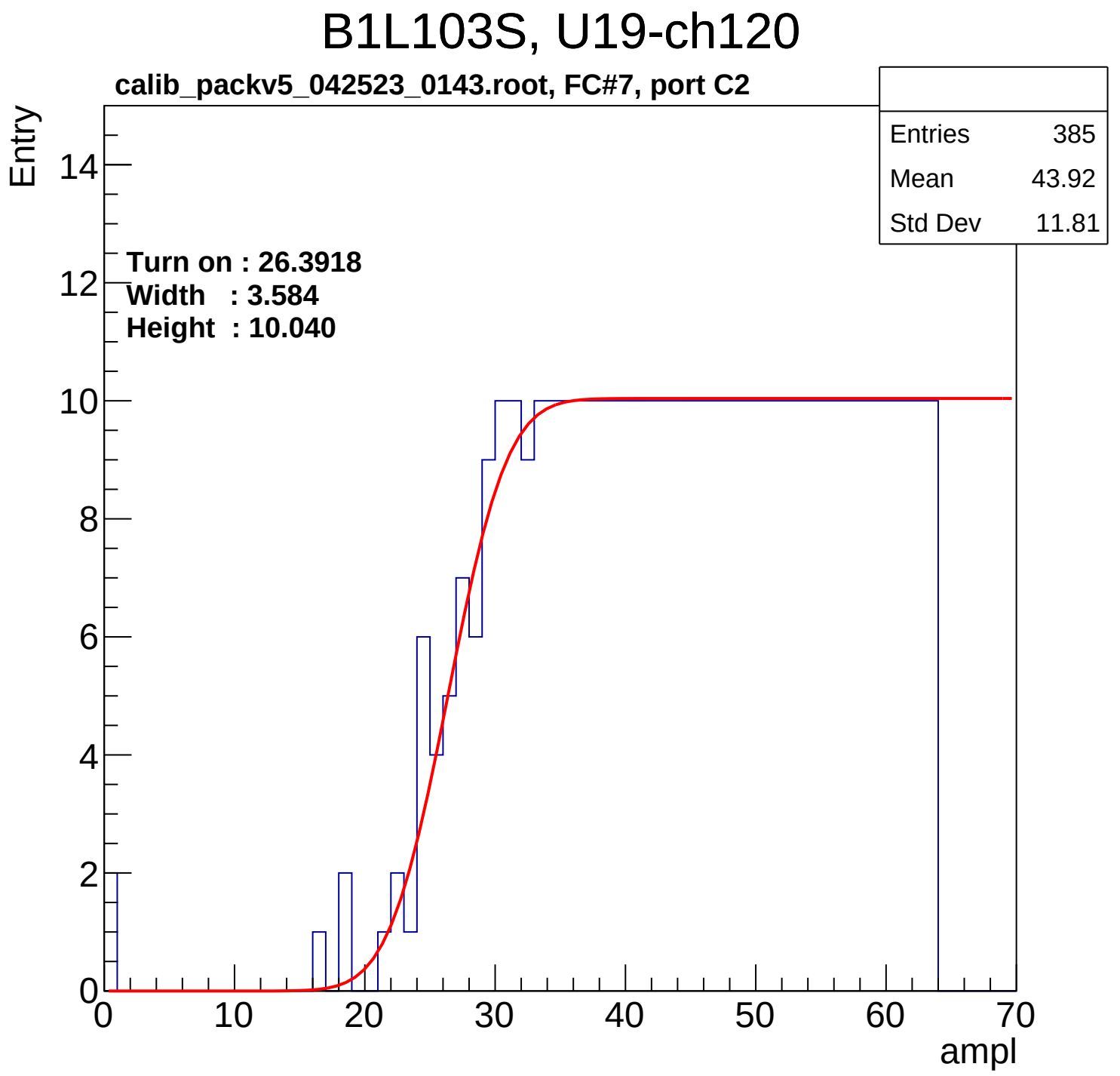
B1L103S, U19-ch120
calib_packv5_042523_0143.root, FC#7, port C2
Entries 385
Mean 43.92
Std Dev 11.81
Turn on : 26.3918
Width : 3.584
Height : 10.040
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
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60
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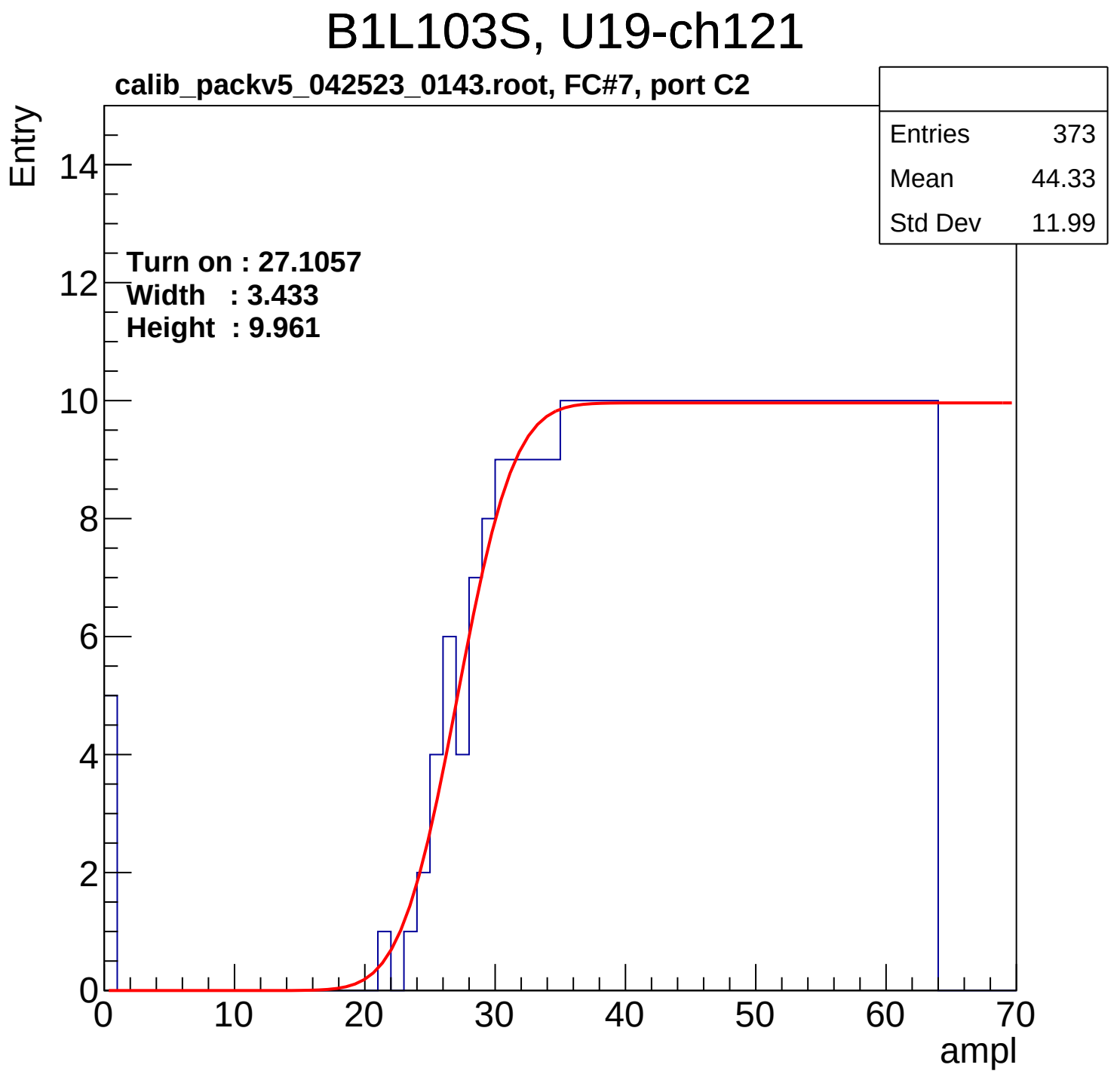
B1L103S, U19-ch121
calib_packv5_042523_0143.root, FC#7, port C2
Entries 373
Mean 44.33
Std Dev 11.99
Turn on : 27.1057
Width : 3.433
Height : 9.961
Entry
ampl
0
2
4
6
8
10
12
14
0
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20
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40
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60
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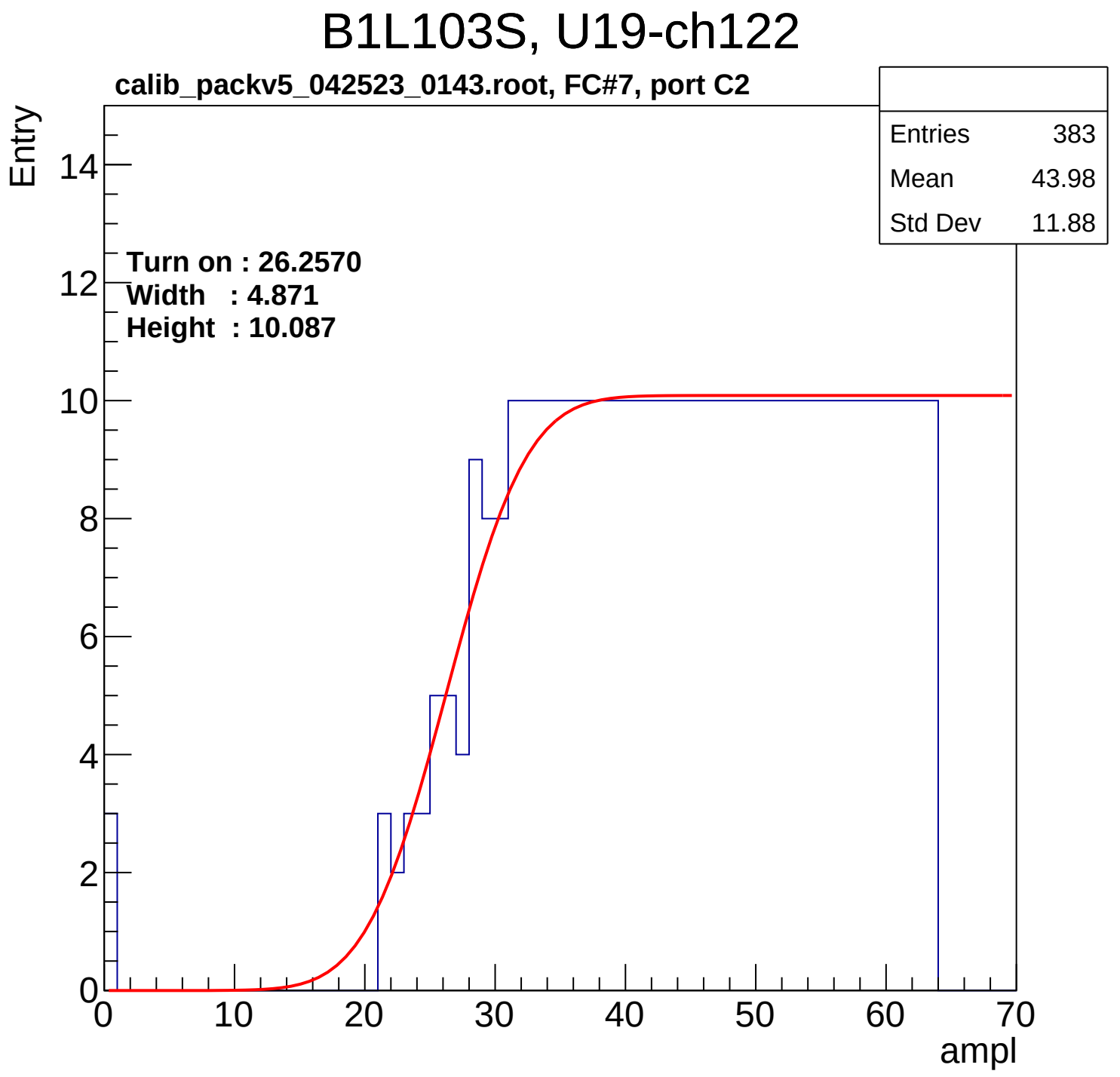
B1L103S, U19-ch122
calib_packv5_042523_0143.root, FC#7, port C2
Entries 383
Mean 43.98
Std Dev 11.88
Turn on : 26.2570
Width : 4.871
Height : 10.087
Entry
ampl
0
2
4
6
8
10
12
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20
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40
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60
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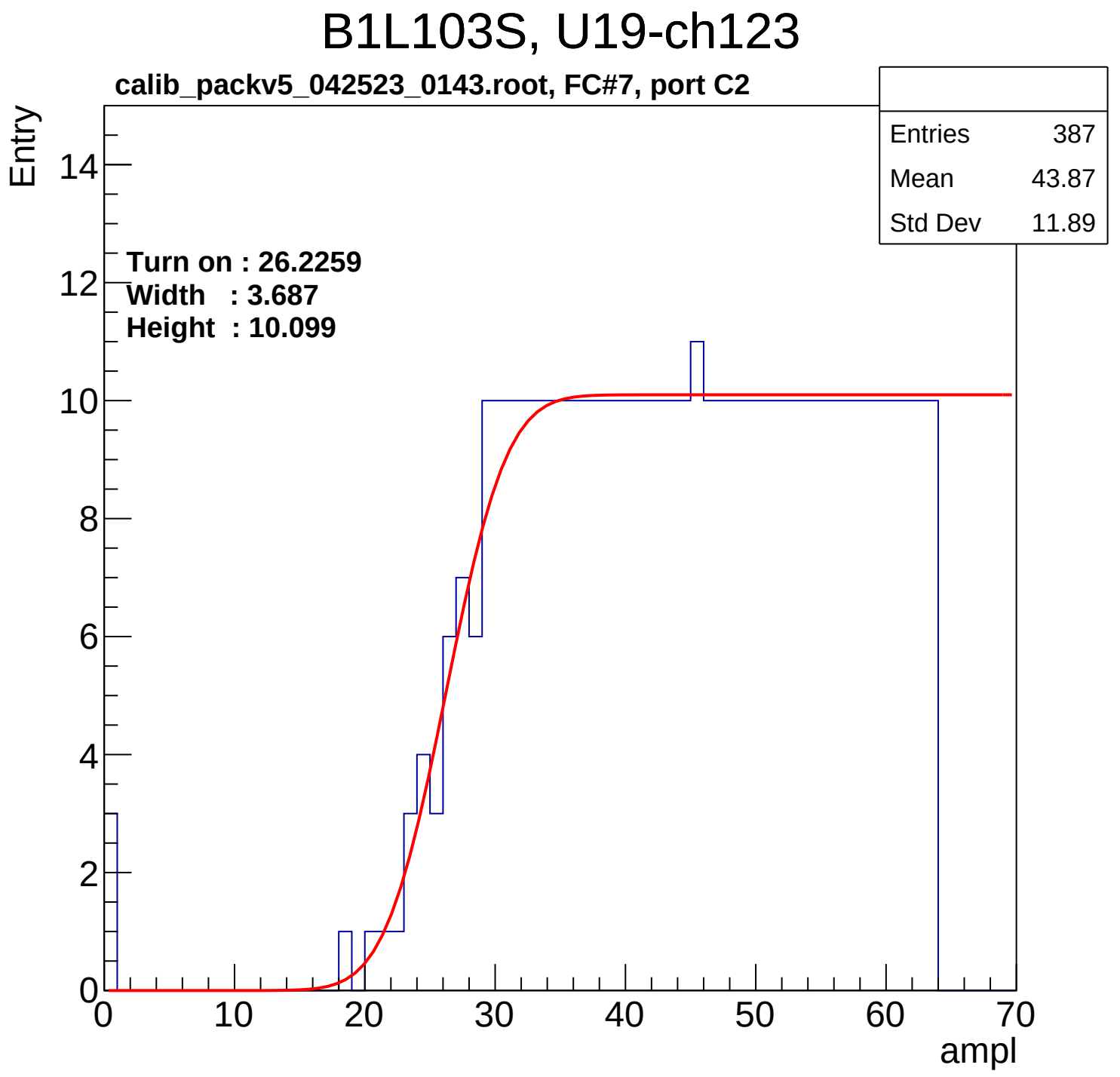
B1L103S, U19-ch123
calib_packv5_042523_0143.root, FC#7, port C2
Entries 387
Mean 43.87
Std Dev 11.89
Turn on : 26.2259
Width : 3.687
Height : 10.099
Entry
ampl
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4
6
8
10
12
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0
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20
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40
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60
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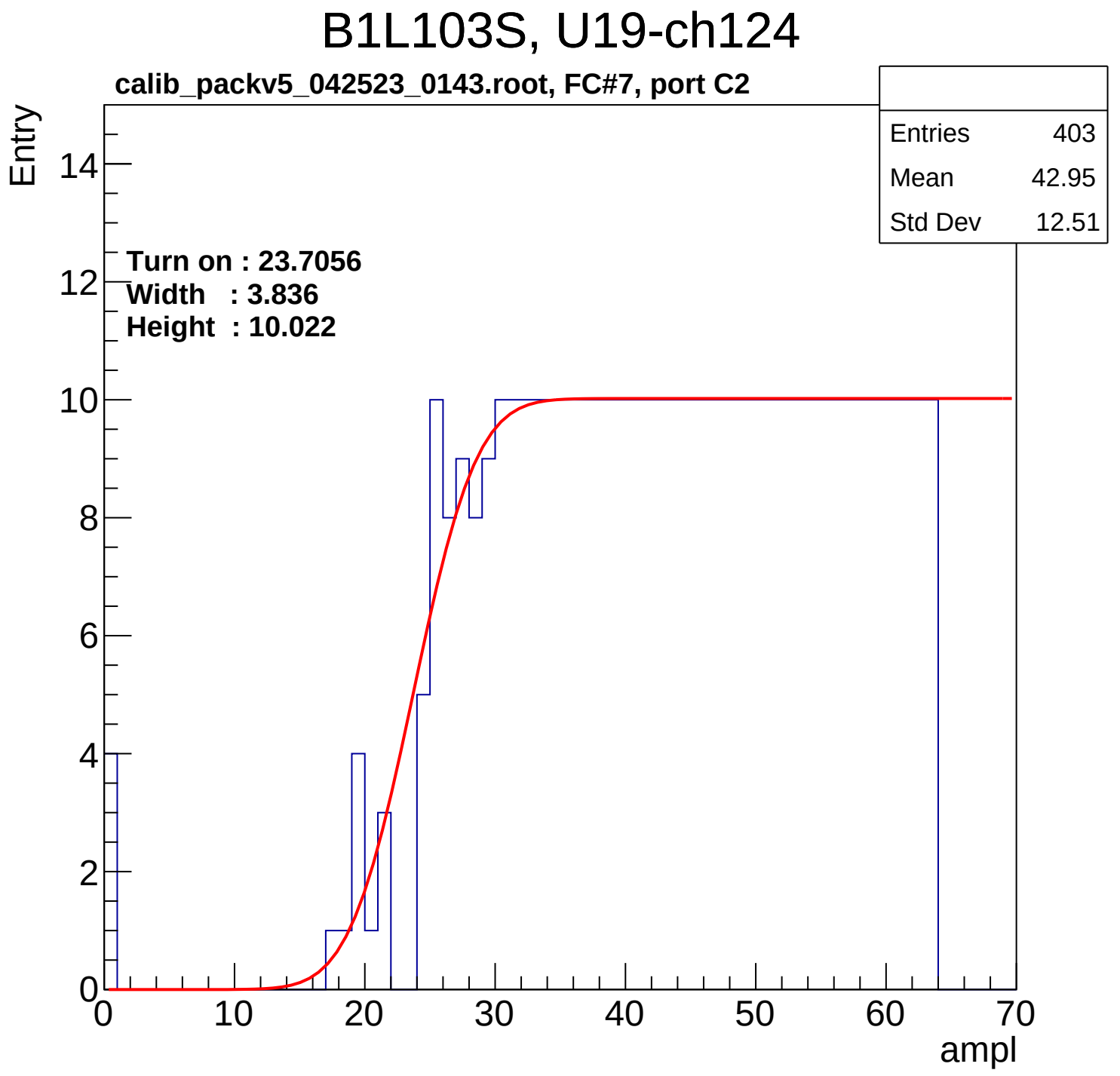
B1L103S, U19-ch124
calib_packv5_042523_0143.root, FC#7, port C2
Entries 403
Mean 42.95
Std Dev 12.51
Turn on : 23.7056
Width : 3.836
Height : 10.022
Entry
ampl
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2
4
6
8
10
12
14
0
10
20
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40
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60
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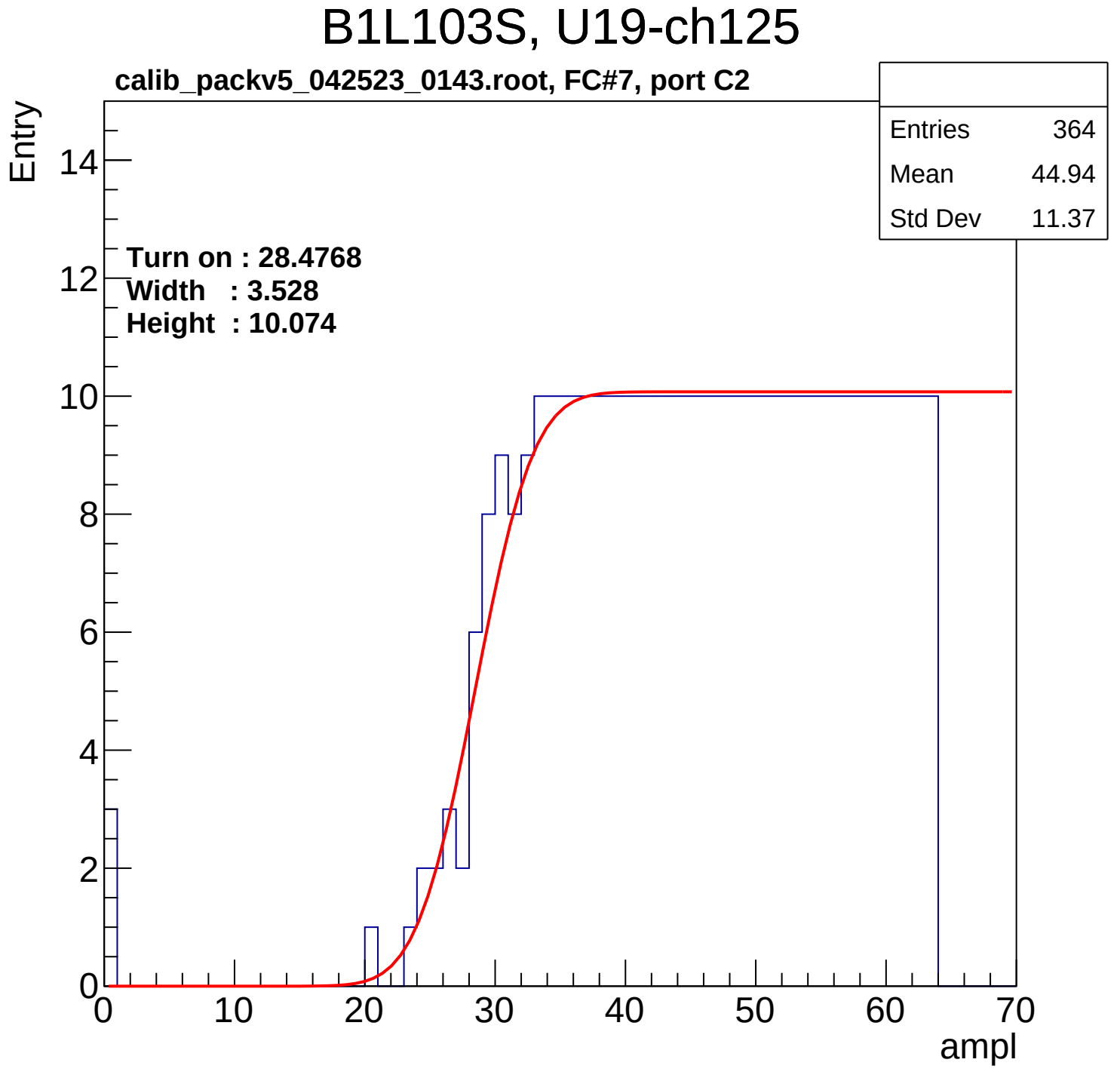
B1L103S, U19-ch125
calib_packv5_042523_0143.root, FC#7, port C2
Entries 364
Mean 44.94
Std Dev 11.37
Turn on : 28.4768
Width : 3.528
Height : 10.074
Entry
ampl
0
2
4
6
8
10
12
14
0
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20
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40
50
60
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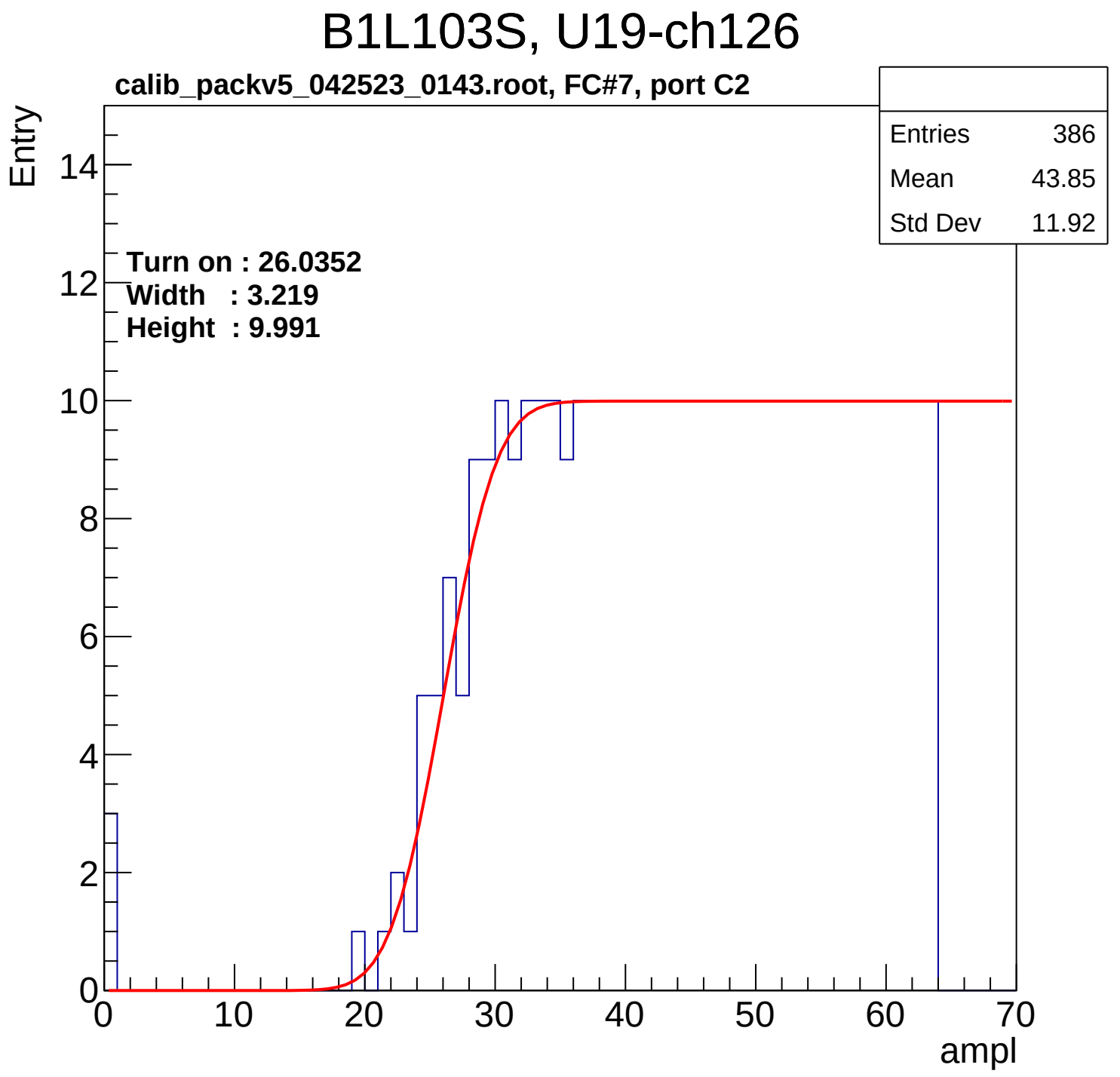
B1L103S, U19-ch126
calib_packv5_042523_0143.root, FC#7, port C2
Entries 386
Mean 43.85
Std Dev 11.92
Turn on : 26.0352
Width : 3.219
Height : 9.991
Entry
ampl
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2
4
6
8
10
12
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0
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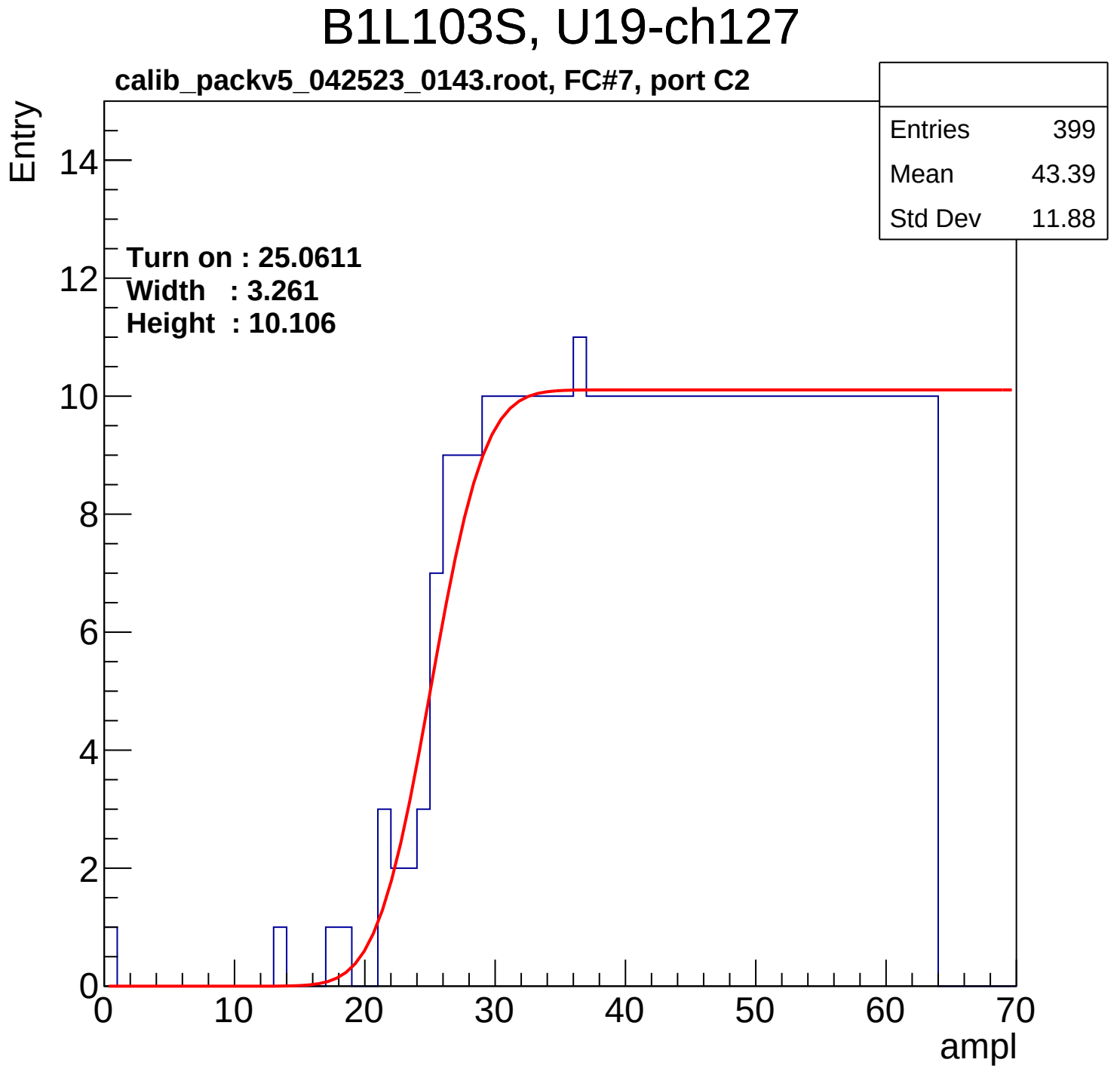
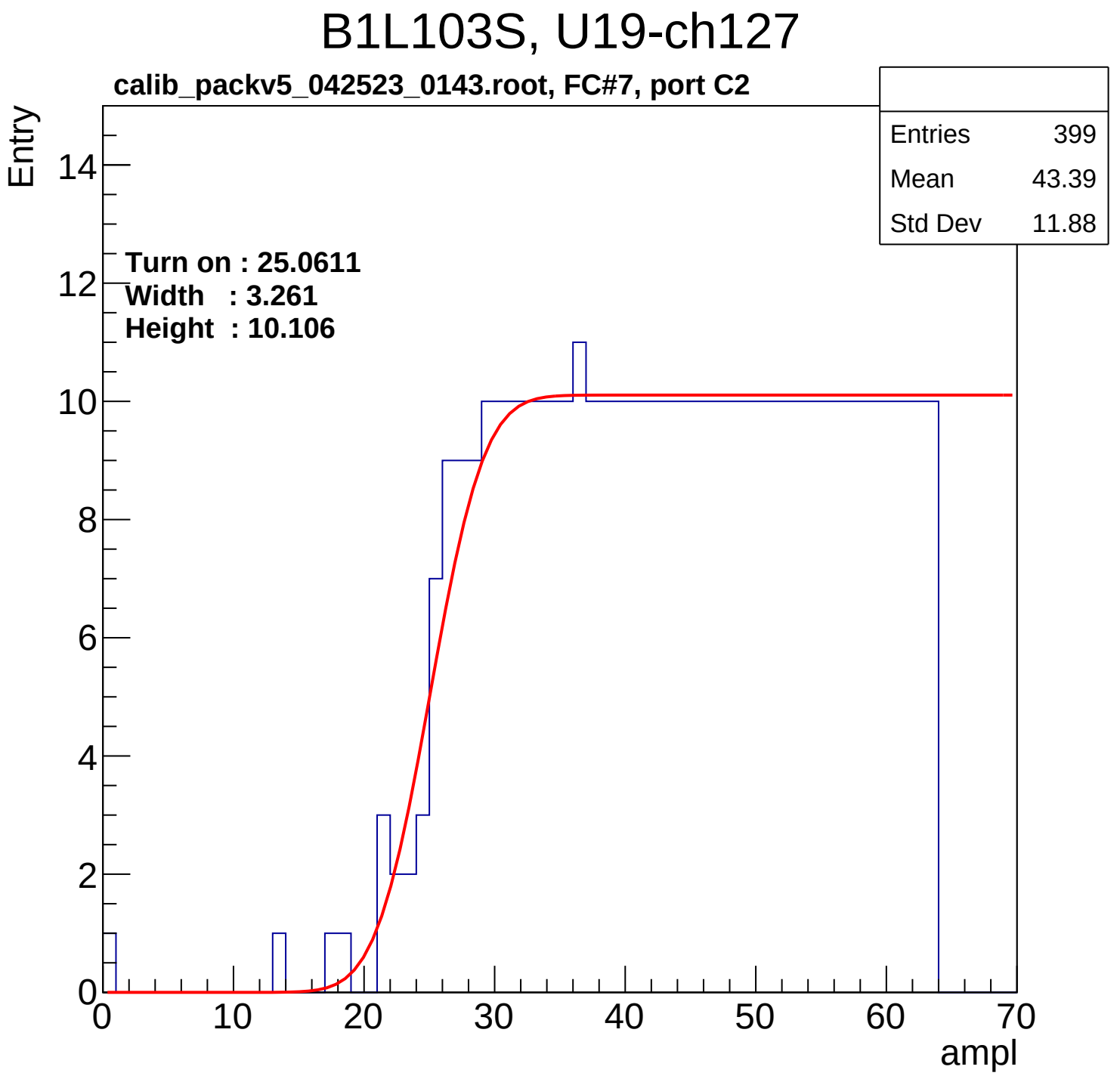

B1L103S, U19-ch127
calib_packv5_042523_0143.root, FC#7, port C2
Entries 399
Mean 43.39
Std Dev 11.88
Turn on : 25.0611
Width : 3.261
Height : 10.106
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L103S, U19-ch127
calib_packv5_042523_0143.root, FC#7, port C2
Entries 399
Mean 43.39
Std Dev 11.88
Turn on : 25.0611
Width : 3.261
Height : 10.106
Entry
ampl
0
2
4
6
8
10
12
14
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20
30
40
50
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