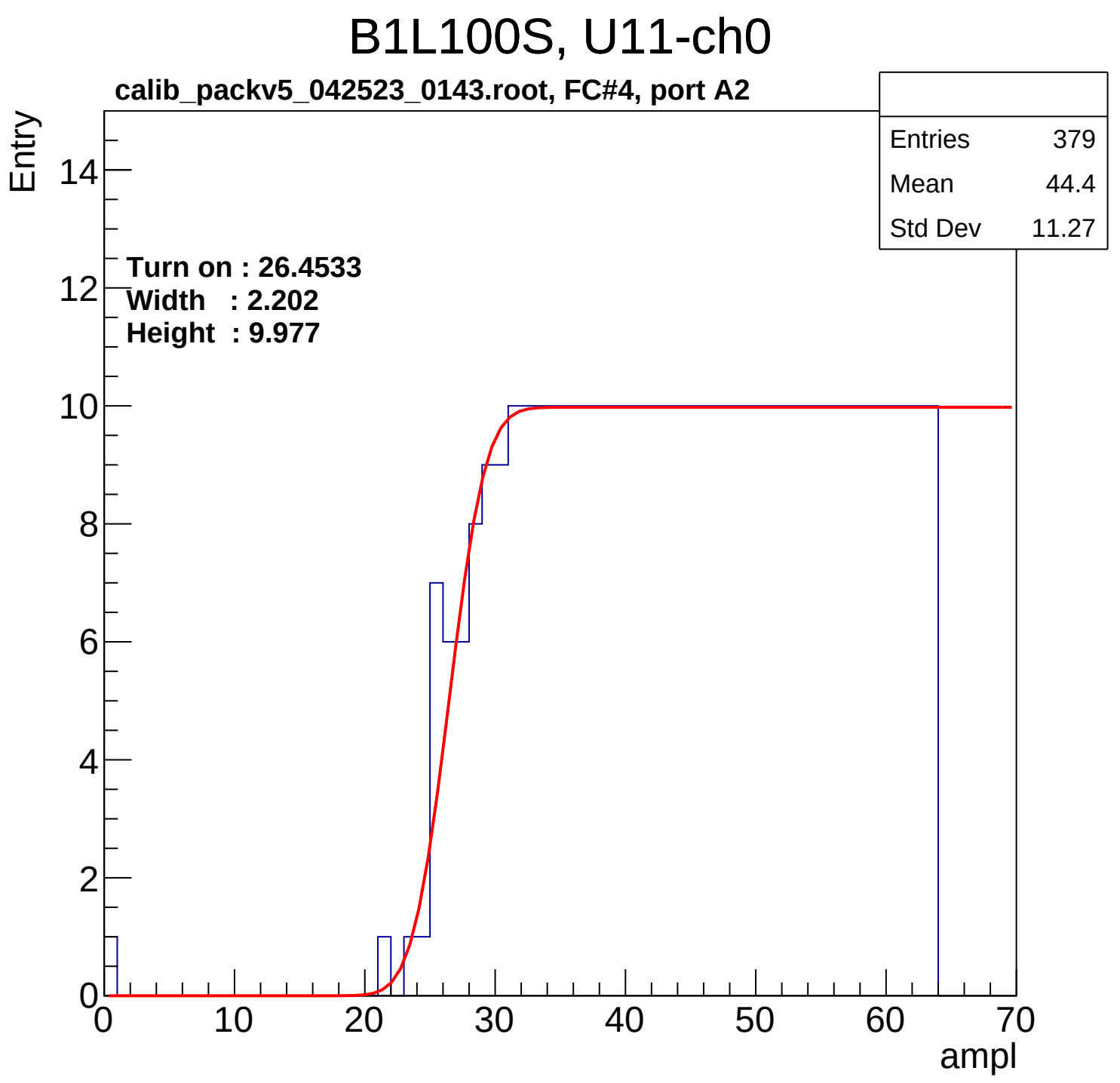
B1L100S, U11-ch0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 379
Mean 44.4
Std Dev 11.27
Turn on : 26.4533
Width : 2.202
Height : 9.977
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ampl
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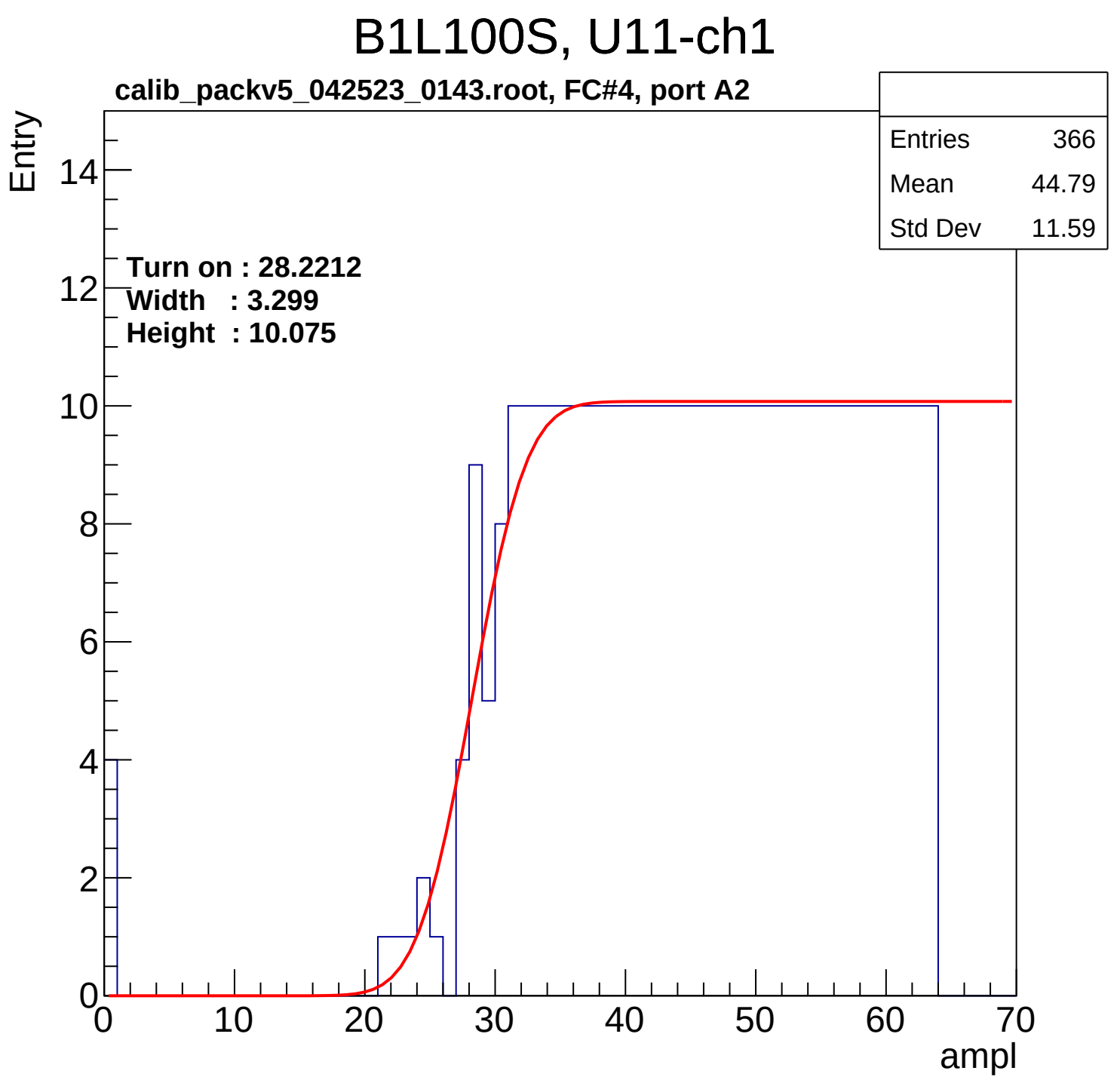
B1L100S, U11-ch1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 366
Mean 44.79
Std Dev 11.59
Turn on : 28.2212
Width : 3.299
Height : 10.075
Entry
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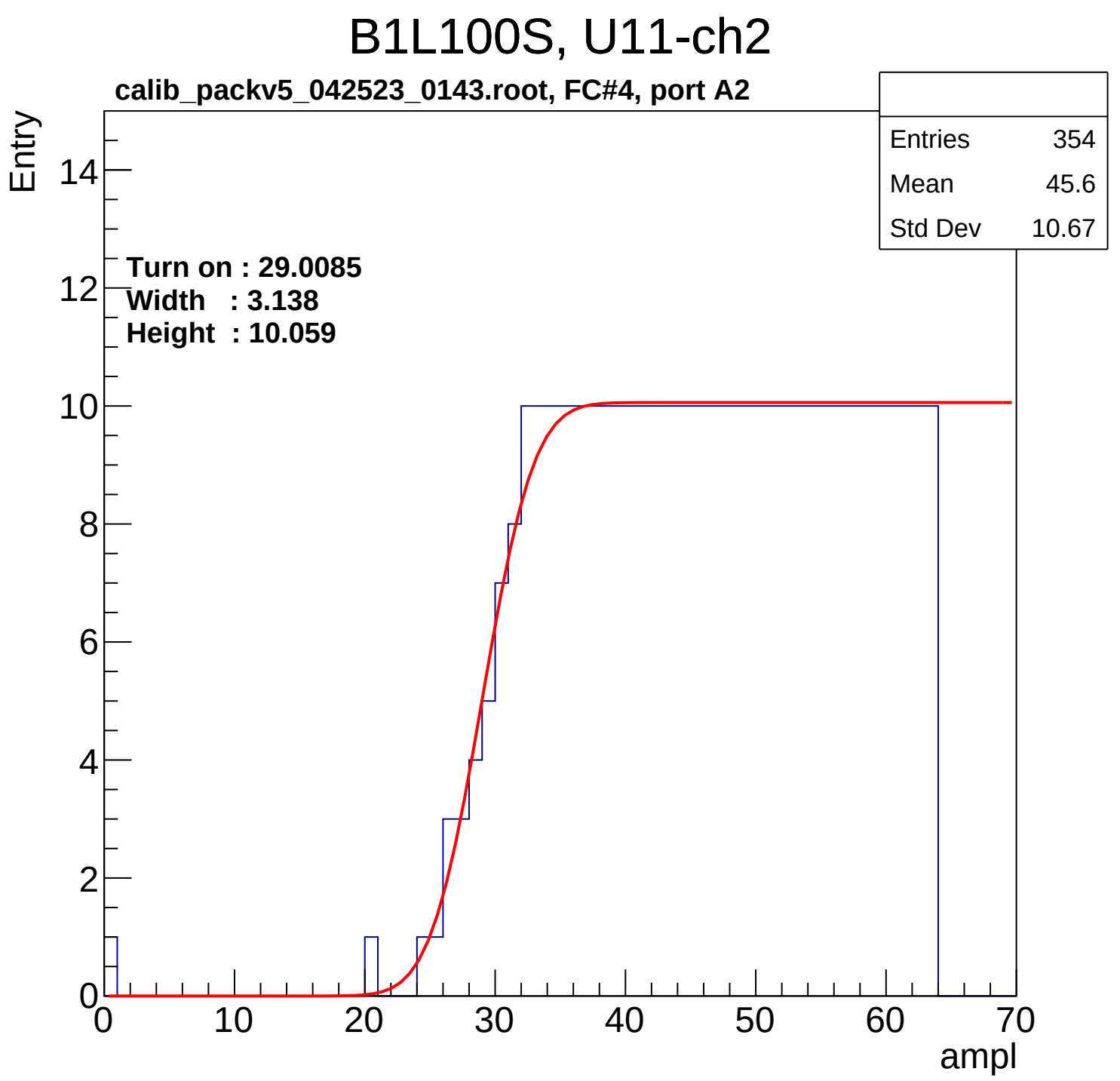
B1L100S, U11-ch2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 354
Mean 45.6
Std Dev 10.67
Turn on : 29.0085
Width : 3.138
Height : 10.059
Entry
ampl
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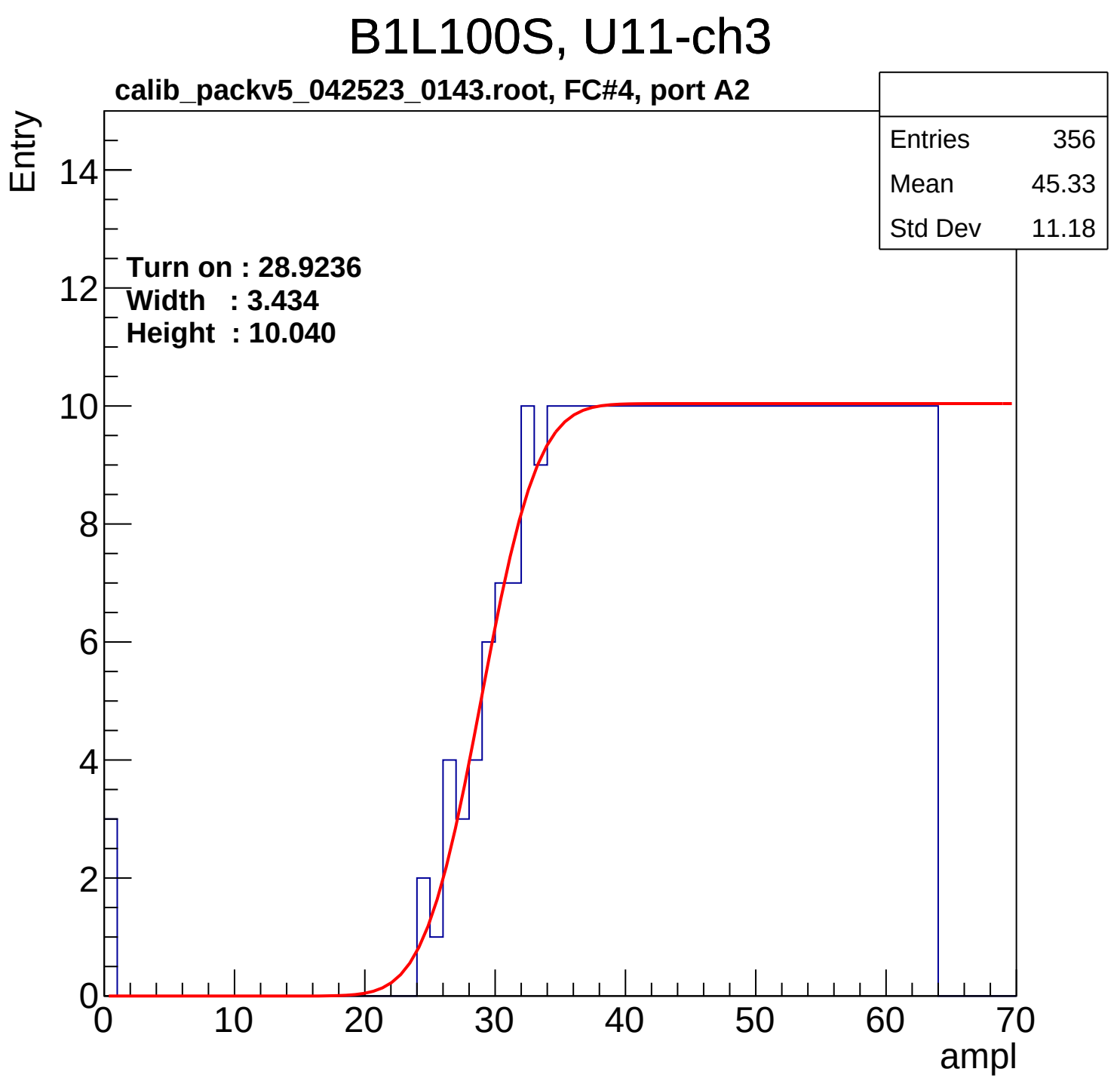
B1L100S, U11-ch3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 356
Mean 45.33
Std Dev 11.18
Turn on : 28.9236
Width : 3.434
Height : 10.040
Entry
ampl
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6
8
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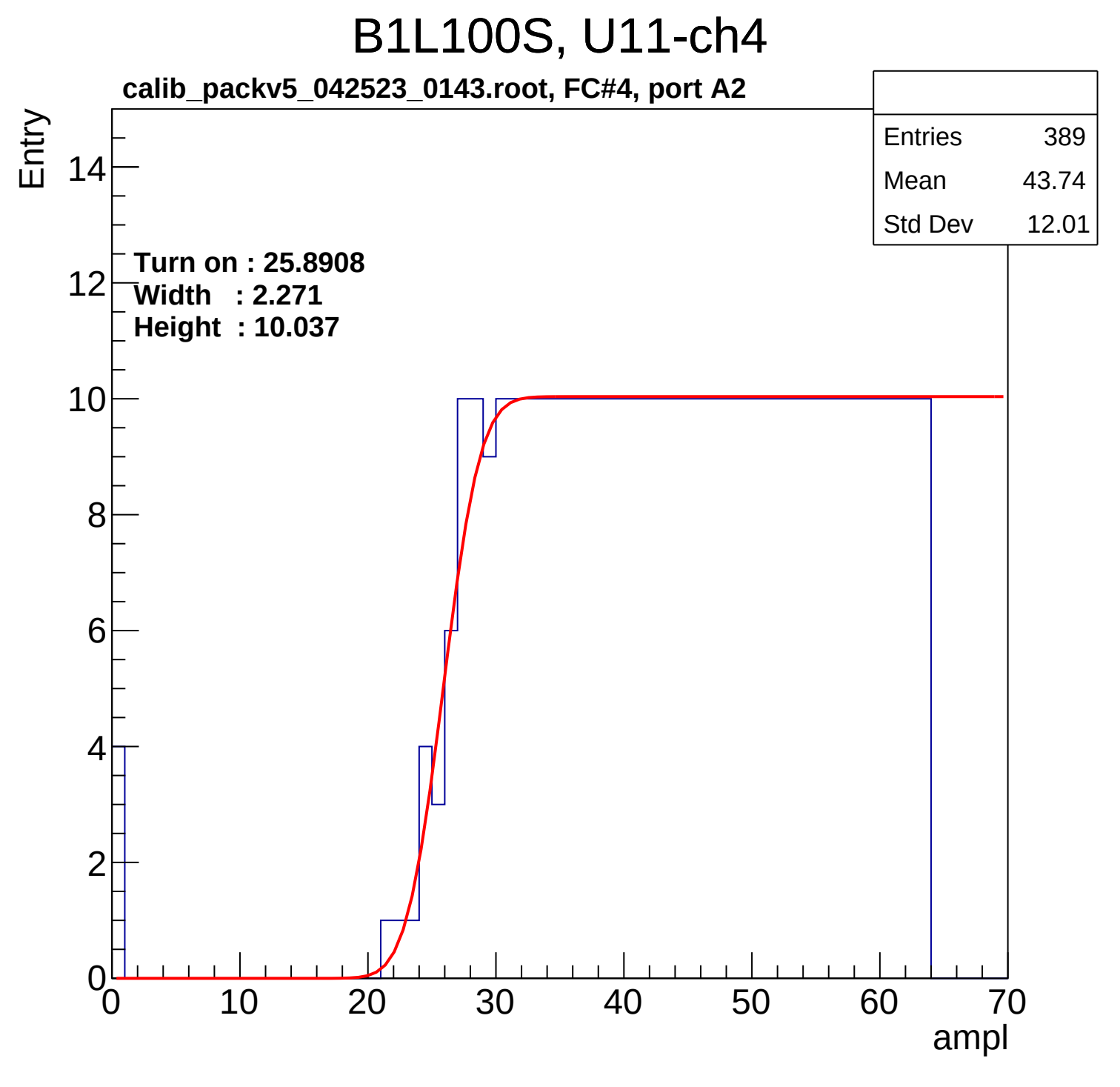
B1L100S, U11-ch4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 389
Mean 43.74
Std Dev 12.01
Turn on : 25.8908
Width : 2.271
Height : 10.037
Entry
ampl
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2
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6
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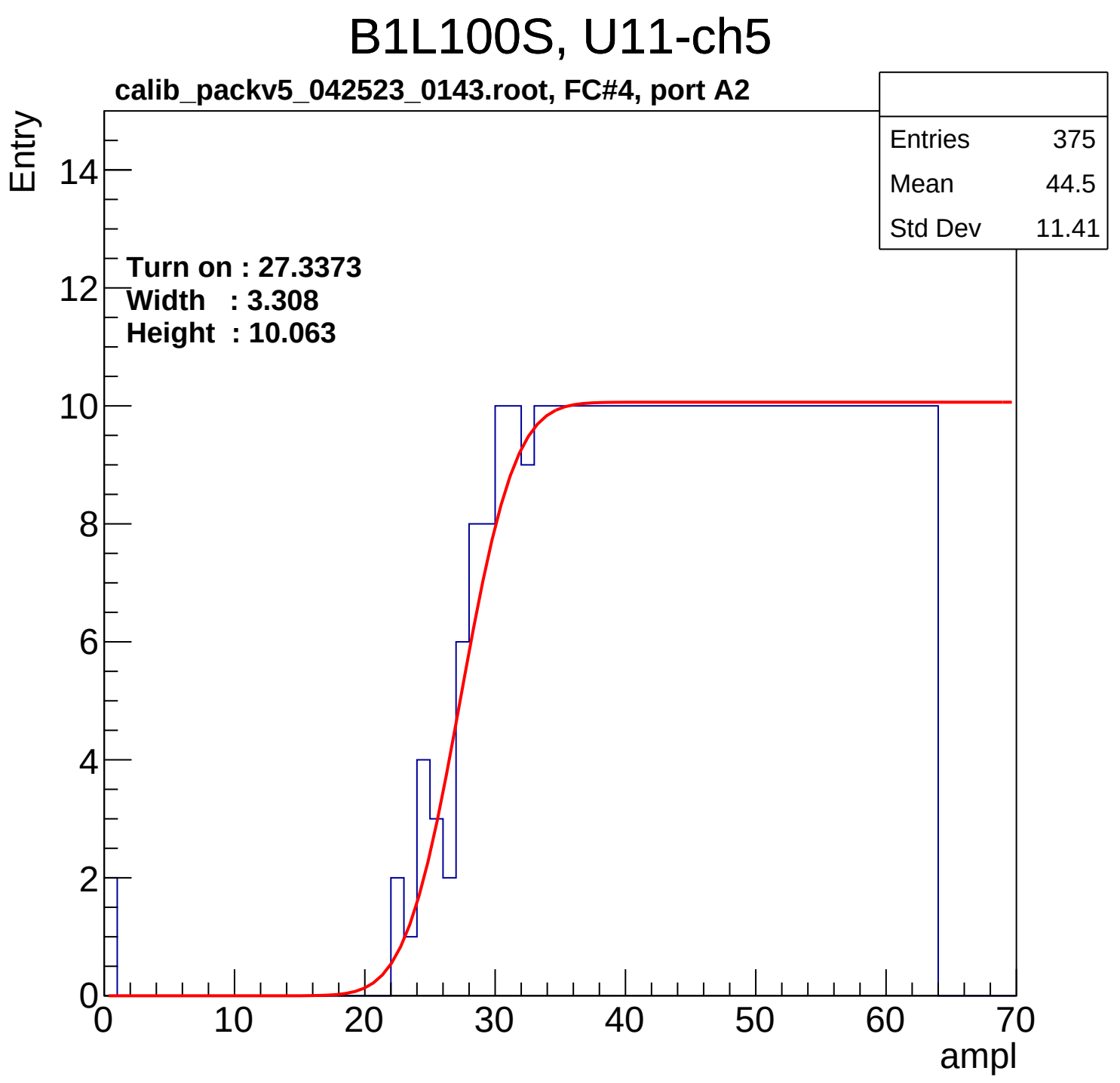
B1L100S, U11-ch5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 375
Mean 44.5
Std Dev 11.41
Turn on : 27.3373
Width : 3.308
Height : 10.063
Entry
ampl
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2
4
6
8
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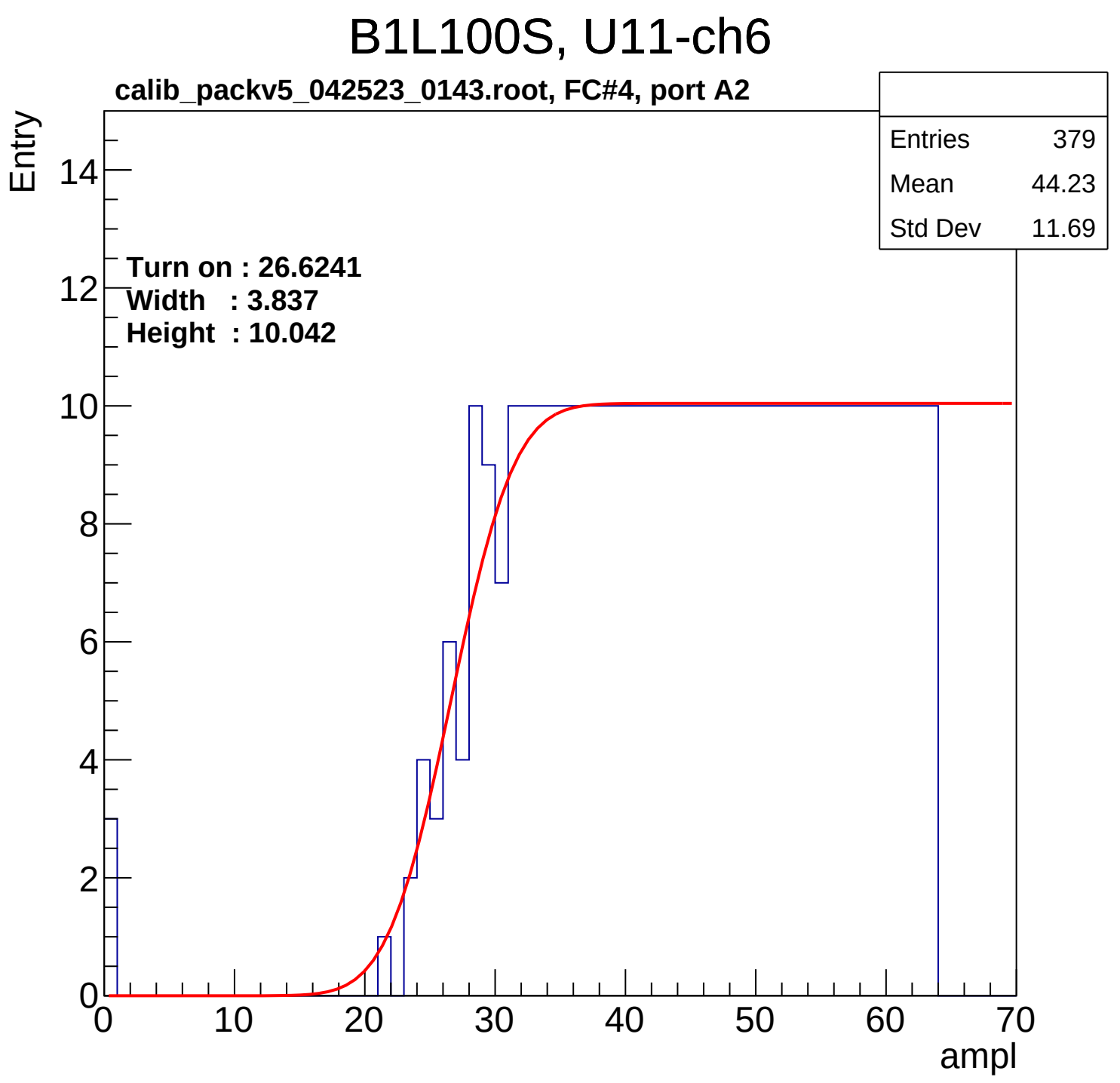
B1L100S, U11-ch6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 379
Mean 44.23
Std Dev 11.69
Turn on : 26.6241
Width : 3.837
Height : 10.042
Entry
ampl
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6
8
10
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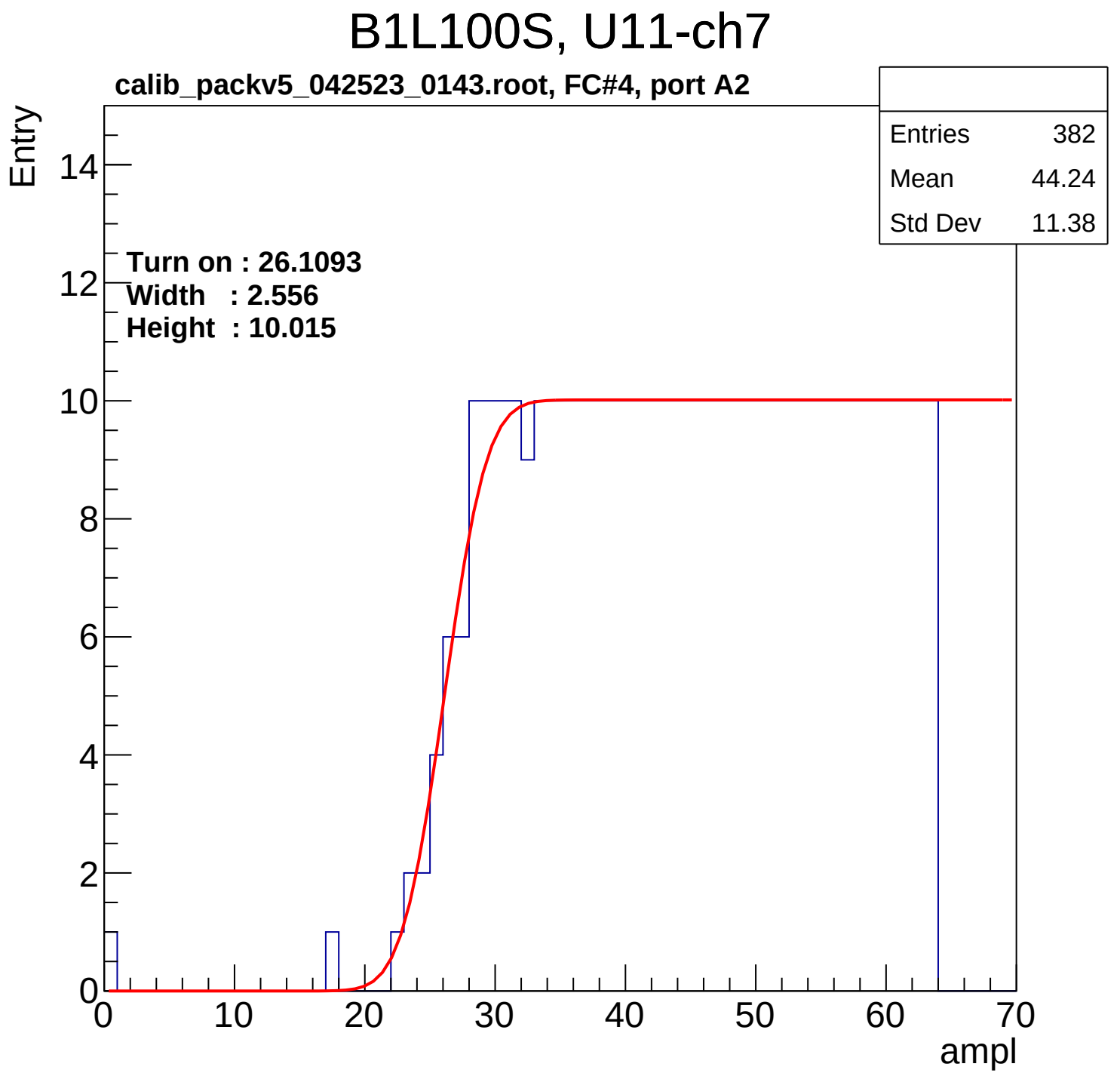
B1L100S, U11-ch7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 382
Mean 44.24
Std Dev 11.38
Turn on : 26.1093
Width : 2.556
Height : 10.015
Entry
ampl
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2
4
6
8
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12
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0
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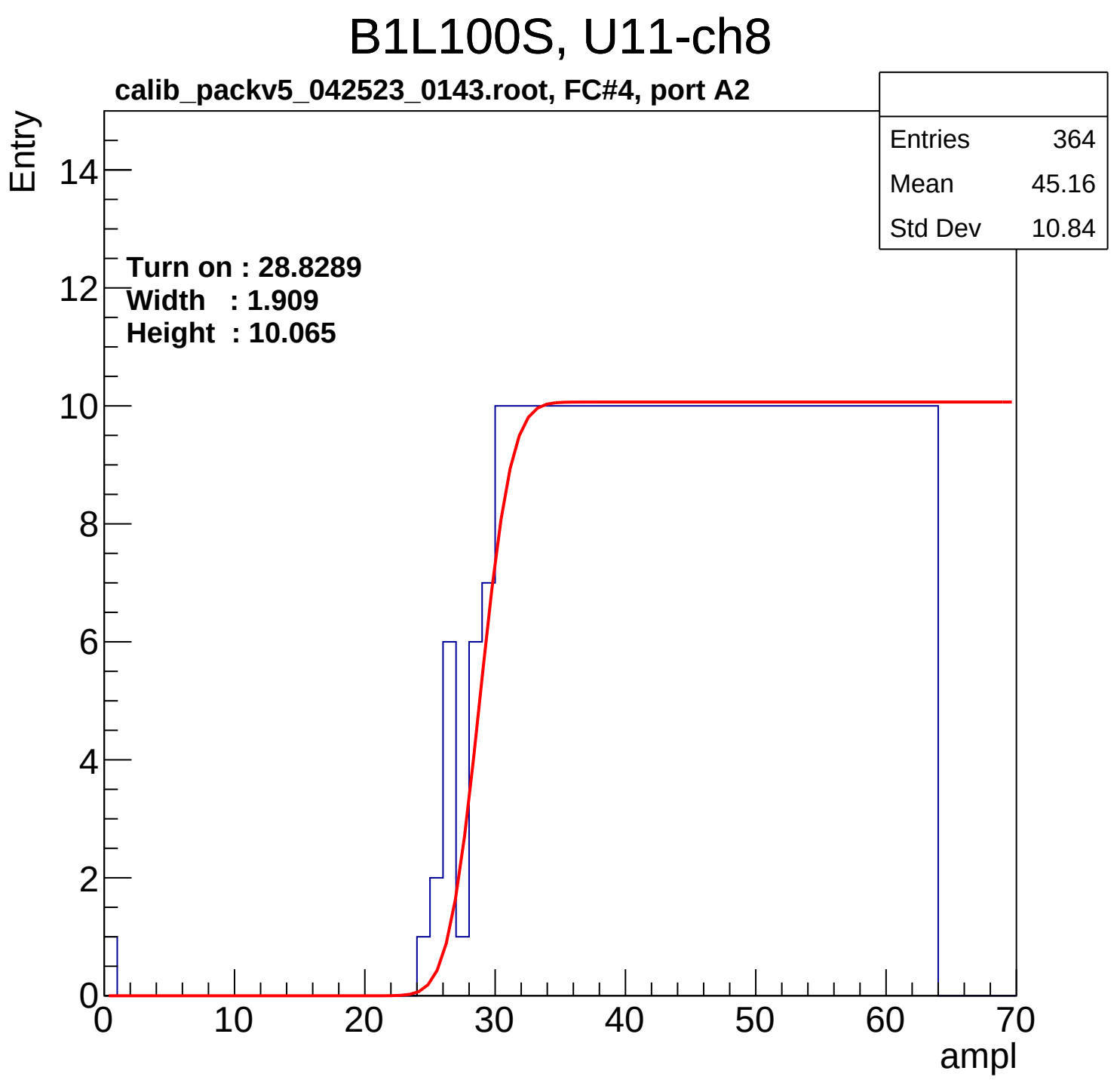
B1L100S, U11-ch8
calib_packv5_042523_0143.root, FC#4, port A2
Entries 364
Mean 45.16
Std Dev 10.84
Turn on : 28.8289
Width : 1.909
Height : 10.065
Entry
ampl
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2
4
6
8
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12
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0
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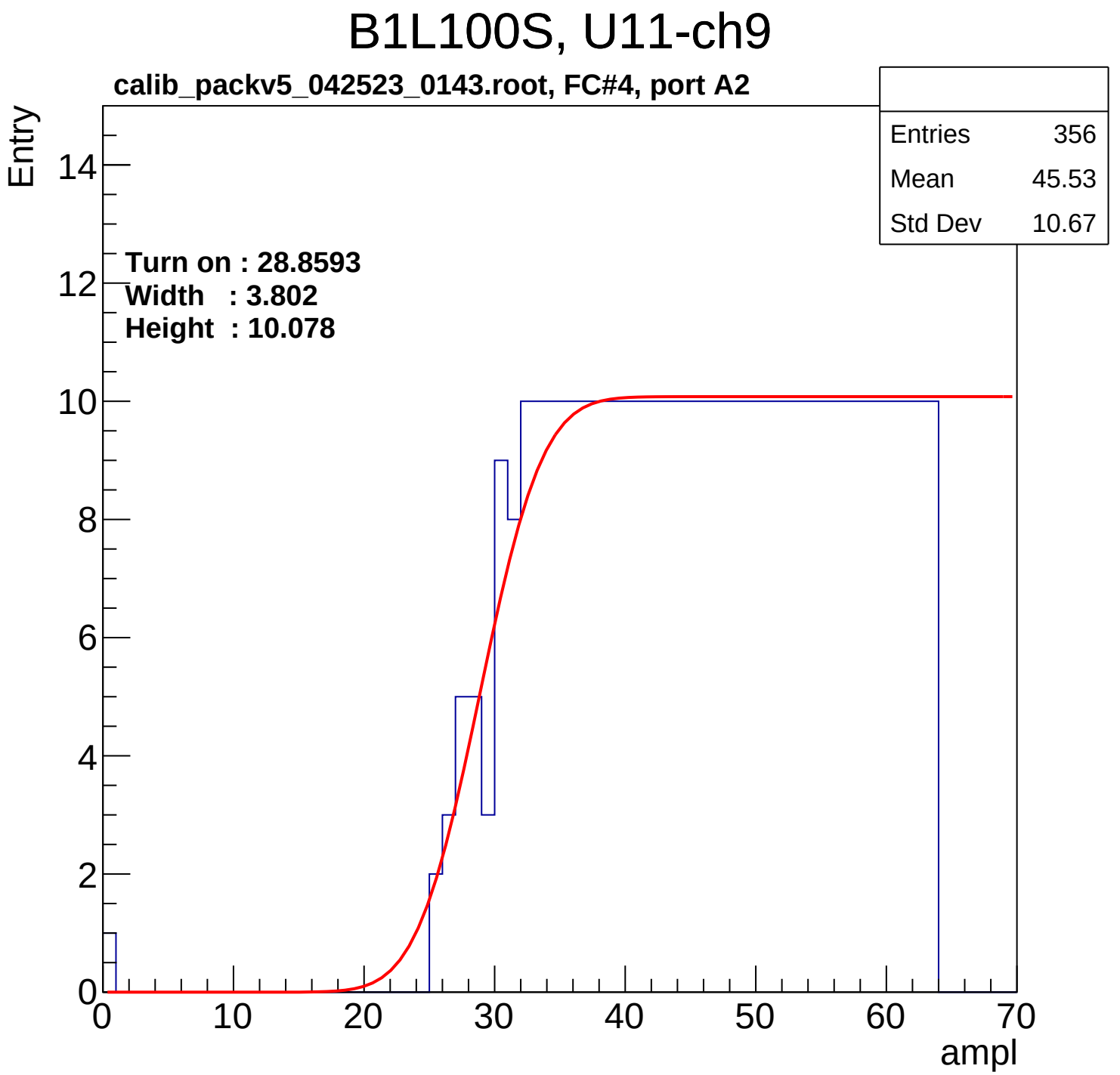
B1L100S, U11-ch9
calib_packv5_042523_0143.root, FC#4, port A2
Entries 356
Mean 45.53
Std Dev 10.67
Turn on : 28.8593
Width : 3.802
Height : 10.078
Entry
ampl
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4
6
8
10
12
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0
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20
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60
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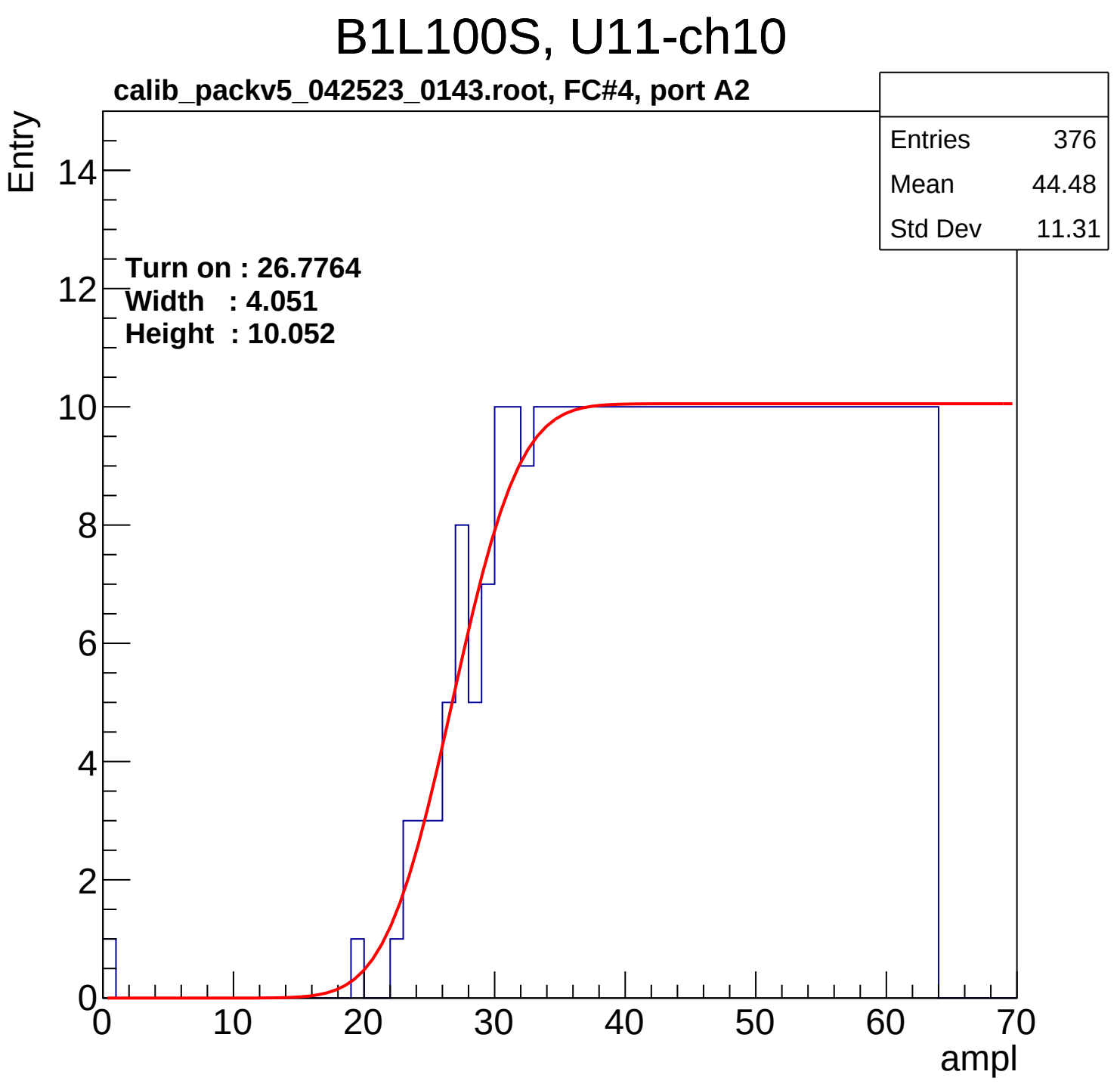
B1L100S, U11-ch10
calib_packv5_042523_0143.root, FC#4, port A2
Entries 376
Mean 44.48
Std Dev 11.31
Turn on : 26.7764
Width : 4.051
Height : 10.052
Entry
ampl
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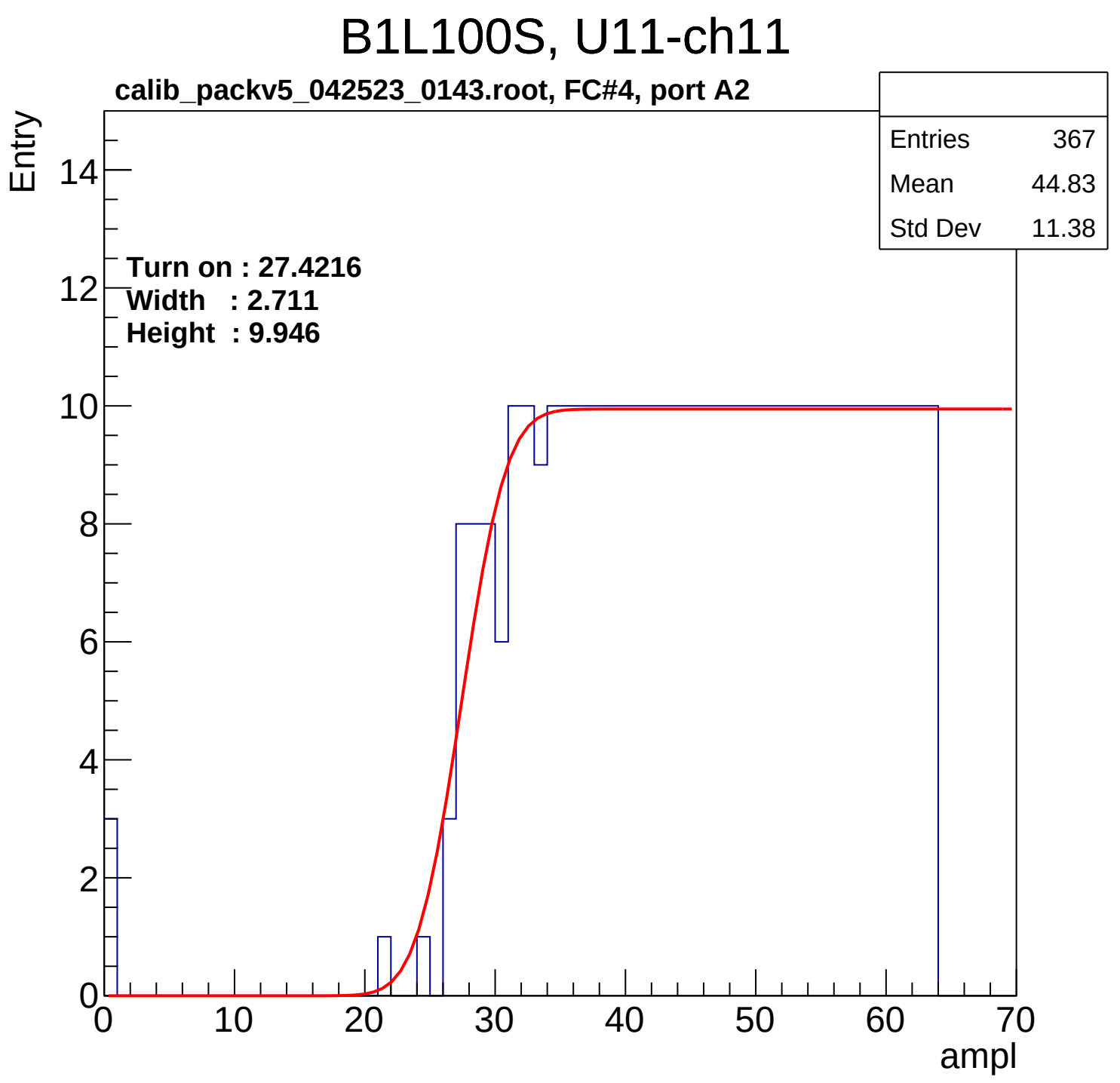
B1L100S, U11-ch11
calib_packv5_042523_0143.root, FC#4, port A2
Entries 367
Mean 44.83
Std Dev 11.38
Turn on : 27.4216
Width : 2.711
Height : 9.946
Entry
ampl
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4
6
8
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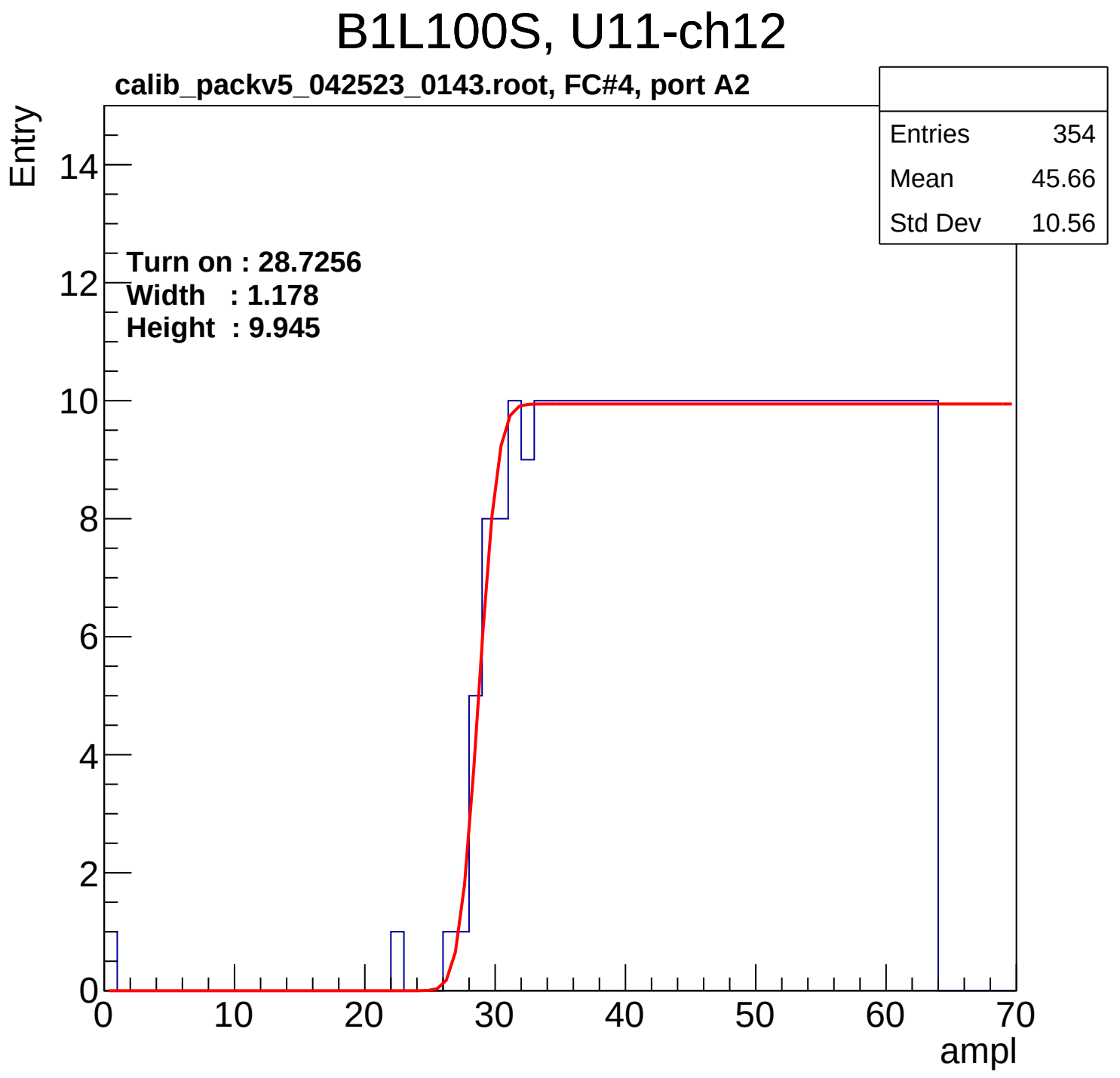
B1L100S, U11-ch12
calib_packv5_042523_0143.root, FC#4, port A2
Entries 354
Mean 45.66
Std Dev 10.56
Turn on : 28.7256
Width : 1.178
Height : 9.945
Entry
ampl
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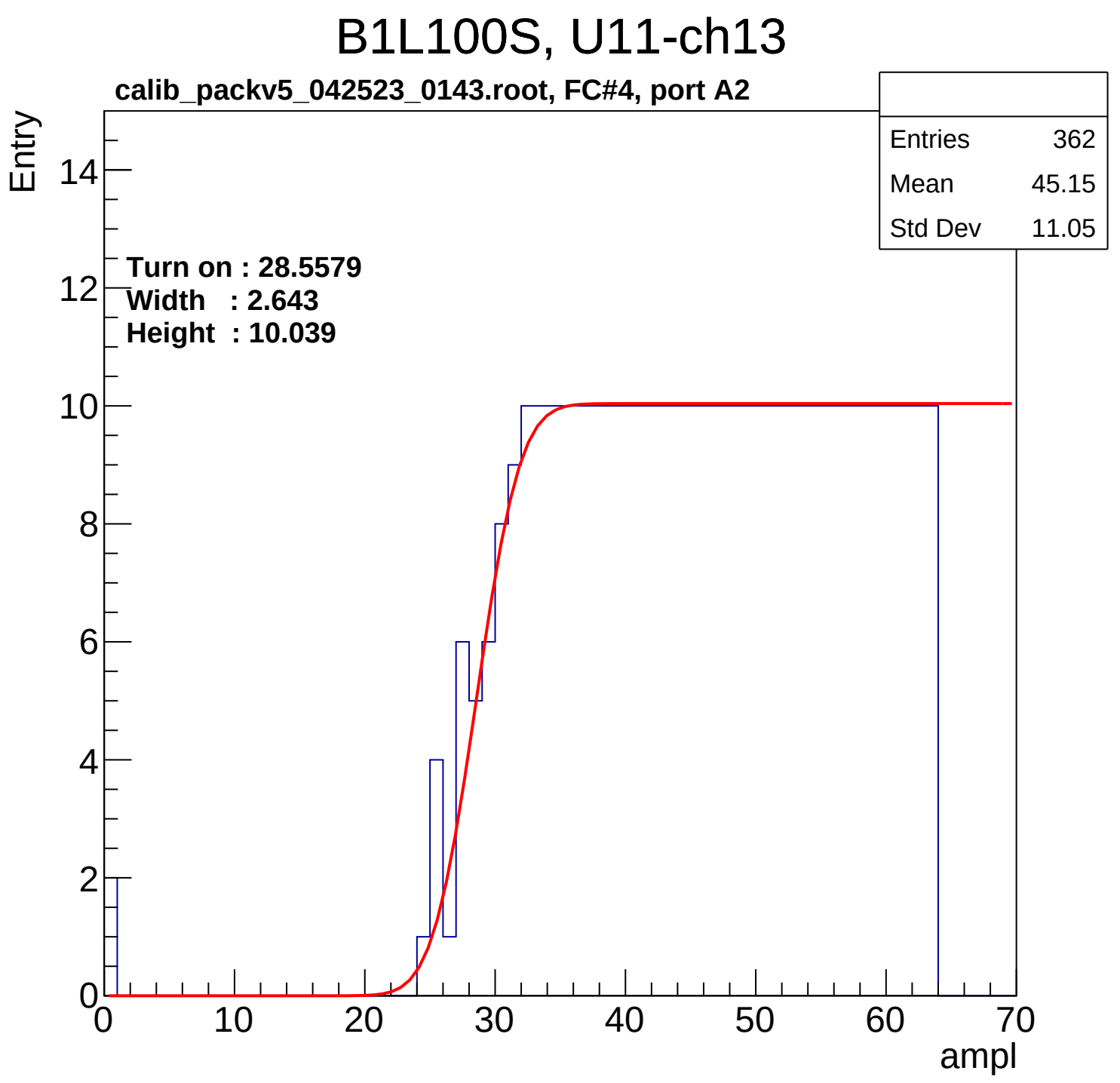
B1L100S, U11-ch13
calib_packv5_042523_0143.root, FC#4, port A2
Entries 362
Mean 45.15
Std Dev 11.05
Turn on : 28.5579
Width : 2.643
Height : 10.039
Entry
ampl
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6
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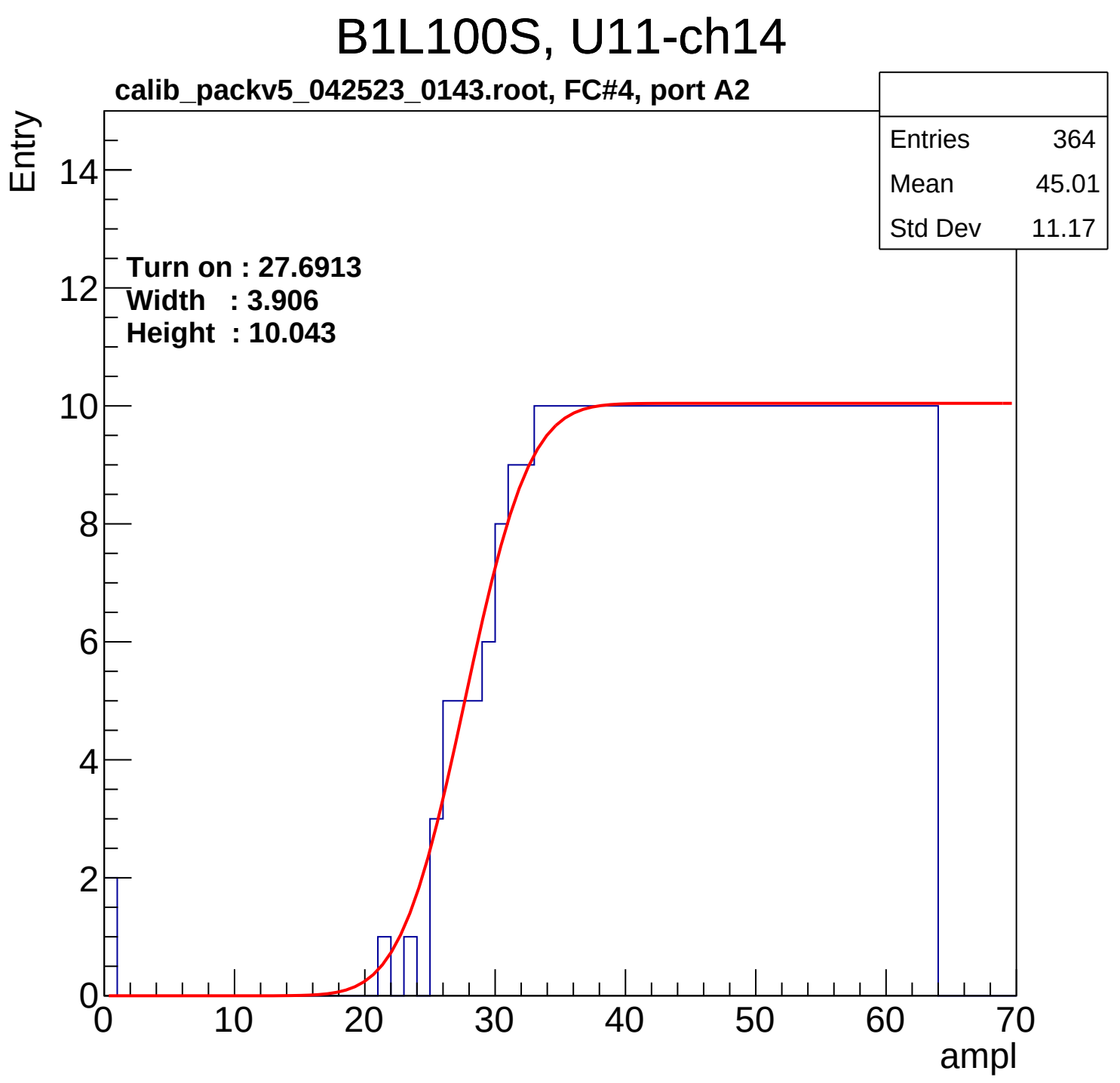
B1L100S, U11-ch14
calib_packv5_042523_0143.root, FC#4, port A2
Entries 364
Mean 45.01
Std Dev 11.17
Turn on : 27.6913
Width : 3.906
Height : 10.043
Entry
ampl
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6
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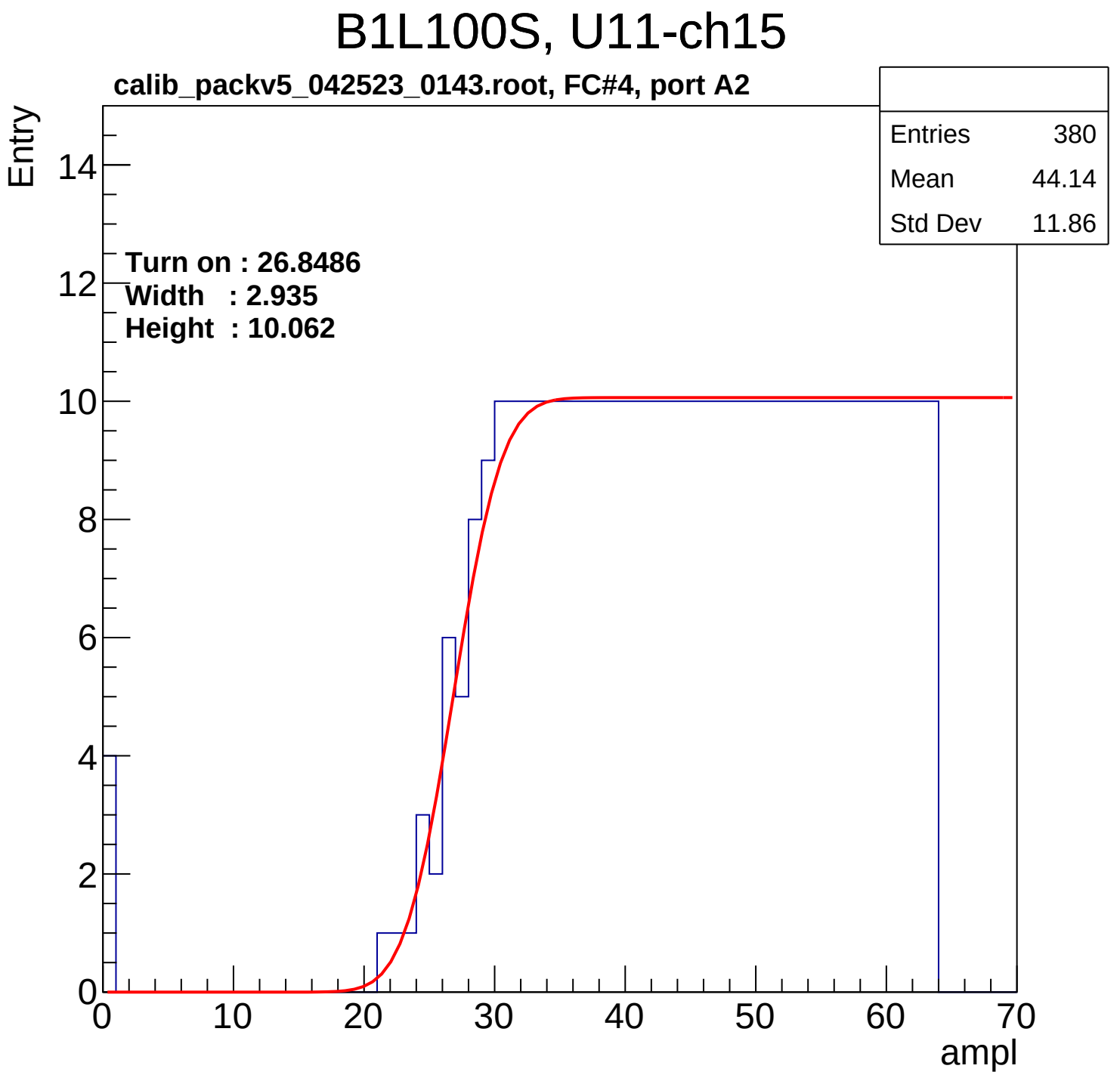
B1L100S, U11-ch15
calib_packv5_042523_0143.root, FC#4, port A2
Entries 380
Mean 44.14
Std Dev 11.86
Turn on : 26.8486
Width : 2.935
Height : 10.062
Entry
ampl
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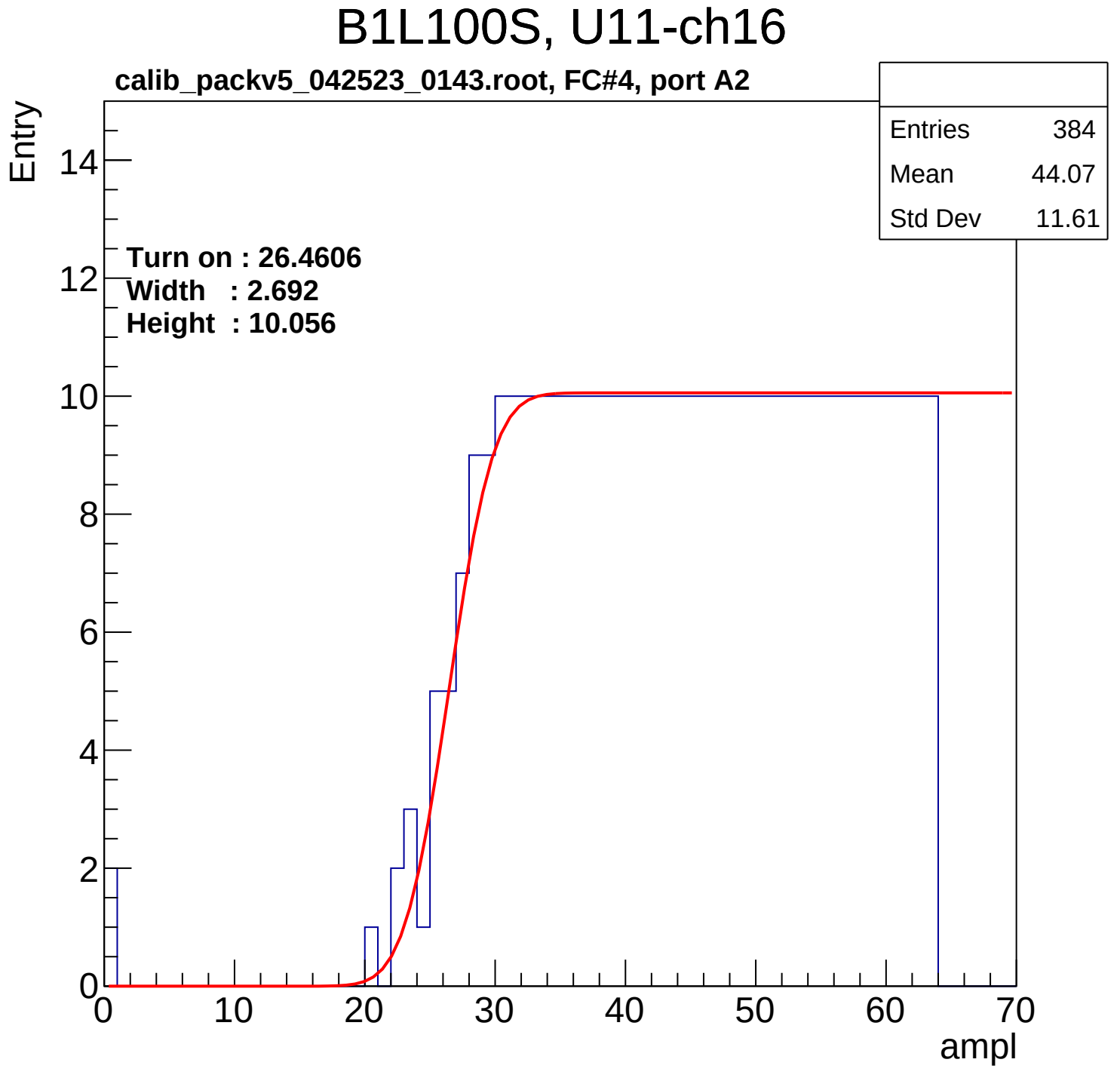
B1L100S, U11-ch16
calib_packv5_042523_0143.root, FC#4, port A2
Entries 384
Mean 44.07
Std Dev 11.61
Turn on : 26.4606
Width : 2.692
Height : 10.056
Entry
ampl
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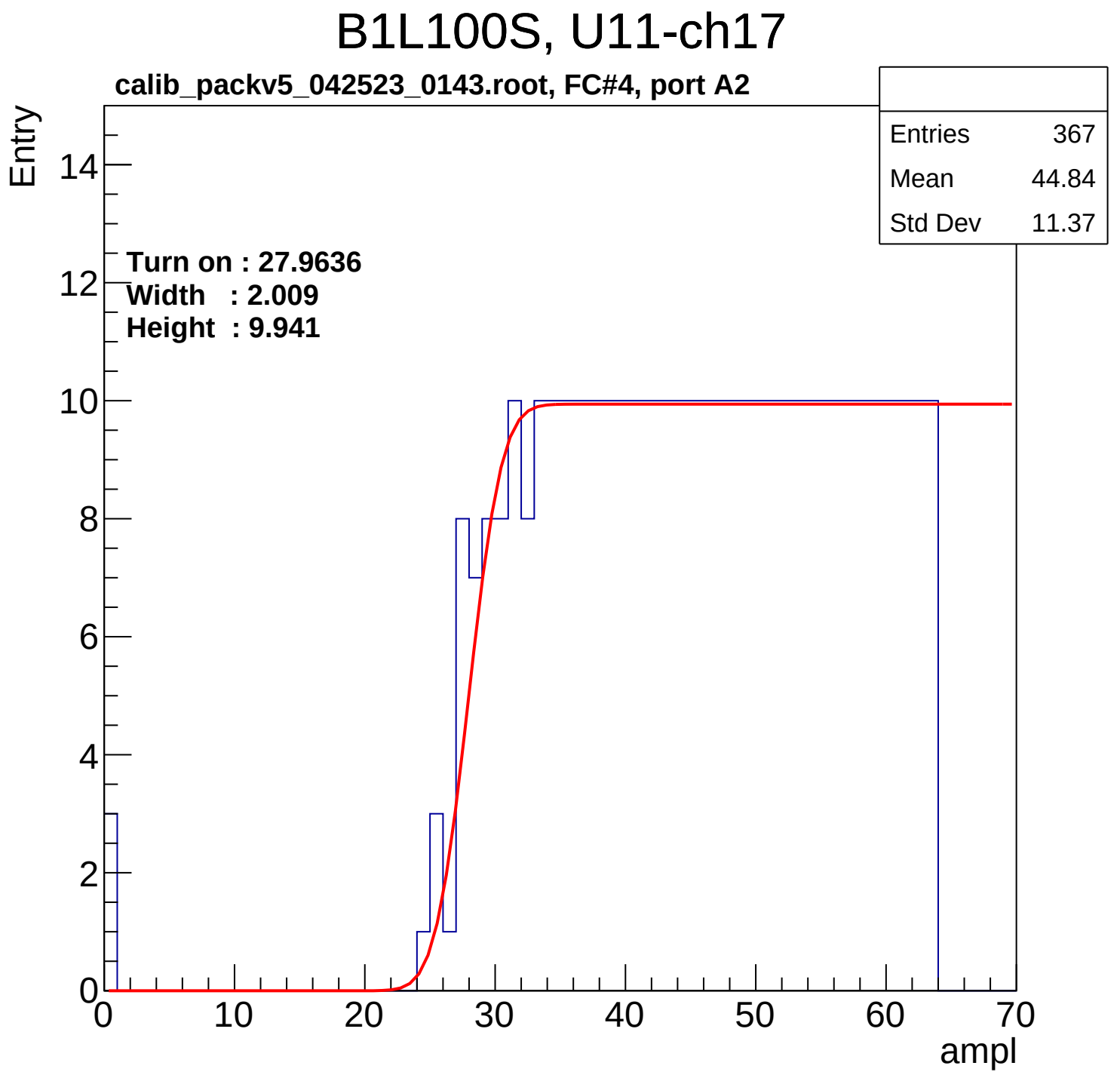
B1L100S, U11-ch17
calib_packv5_042523_0143.root, FC#4, port A2
Entries 367
Mean 44.84
Std Dev 11.37
Turn on : 27.9636
Width : 2.009
Height : 9.941
Entry
ampl
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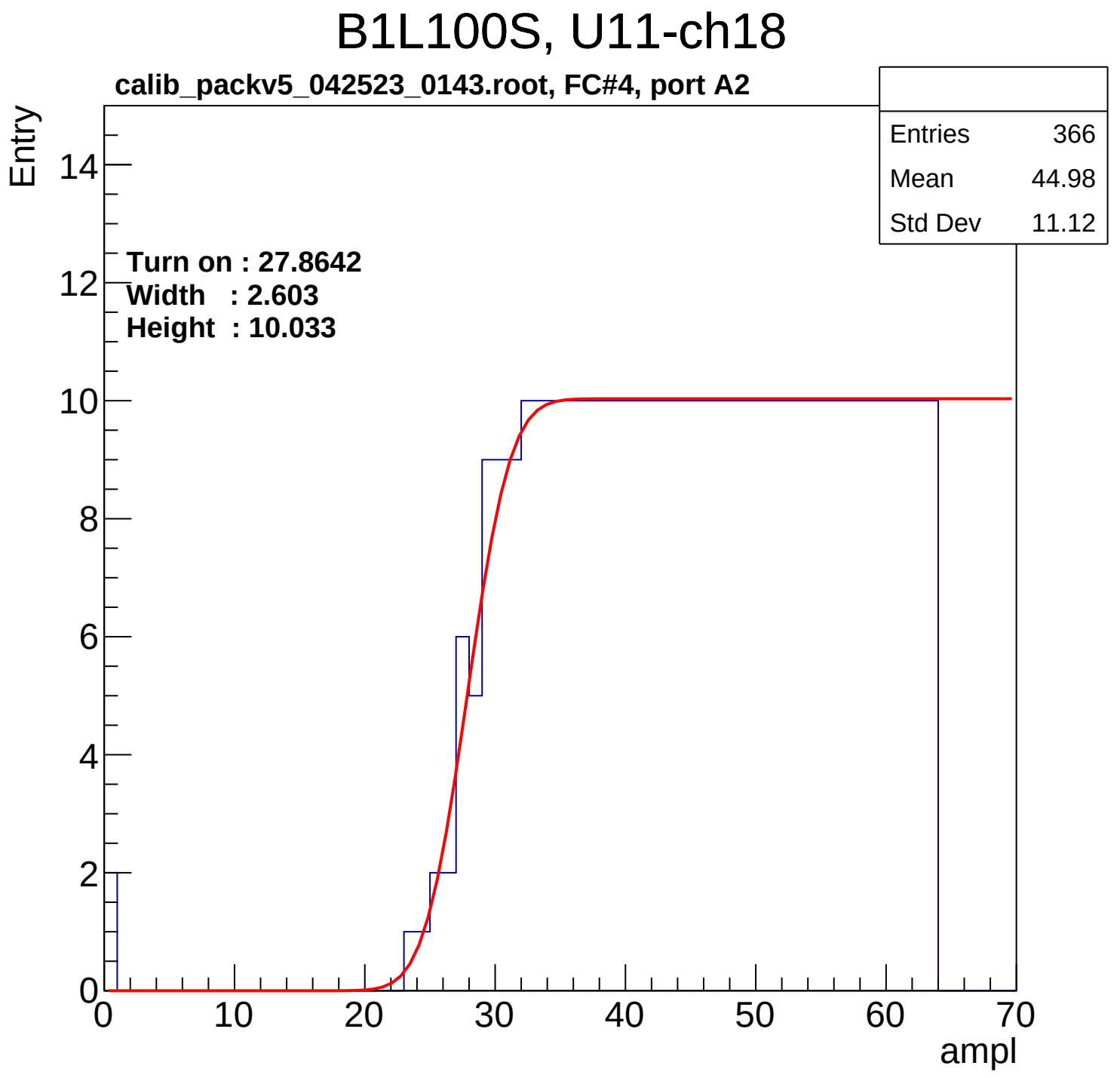
B1L100S, U11-ch18
calib_packv5_042523_0143.root, FC#4, port A2
Entries 366
Mean 44.98
Std Dev 11.12
Turn on : 27.8642
Width : 2.603
Height : 10.033
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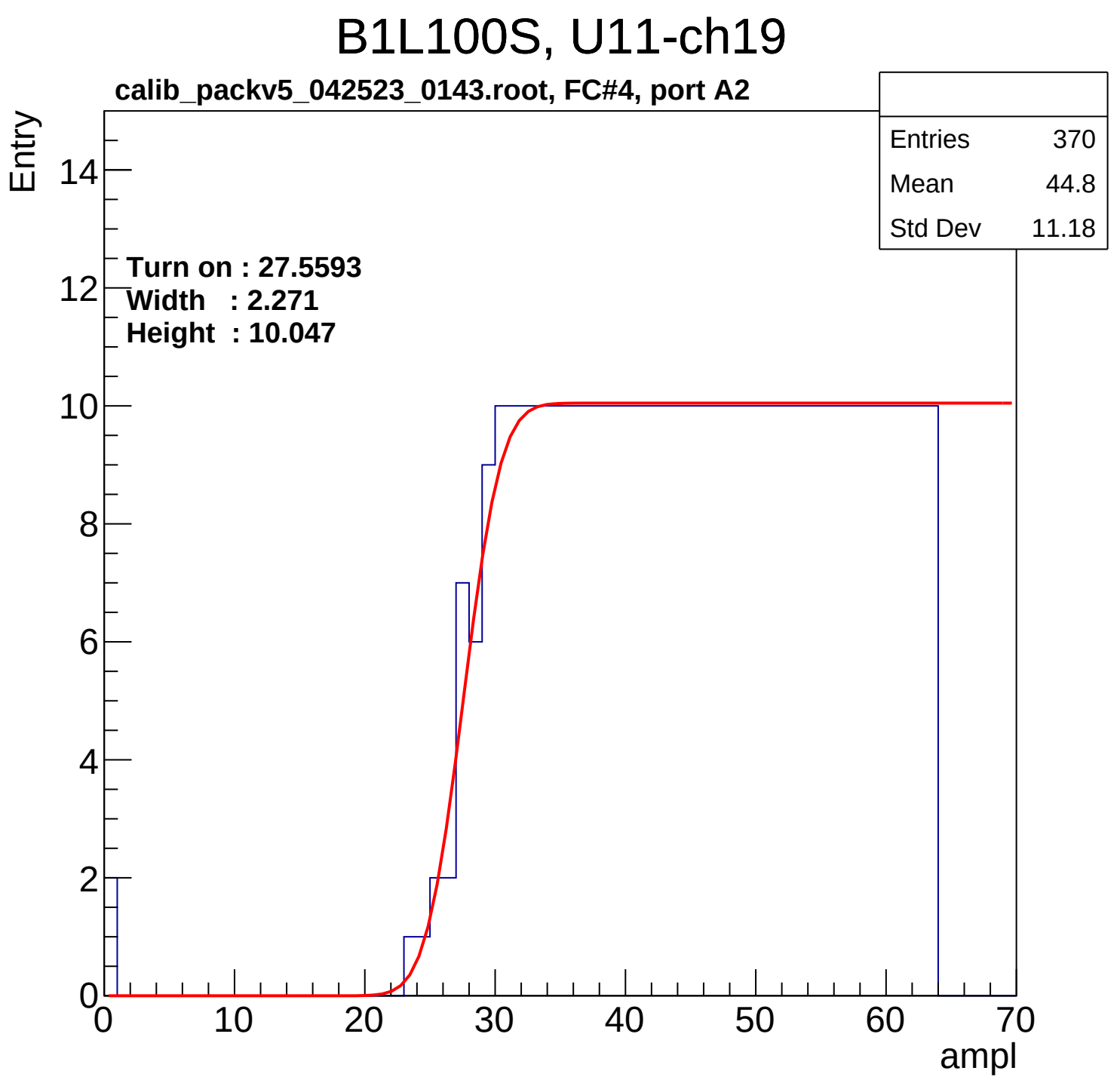
B1L100S, U11-ch19
calib_packv5_042523_0143.root, FC#4, port A2
Entries 370
Mean 44.8
Std Dev 11.18
Turn on : 27.5593
Width : 2.271
Height : 10.047
Entry
ampl
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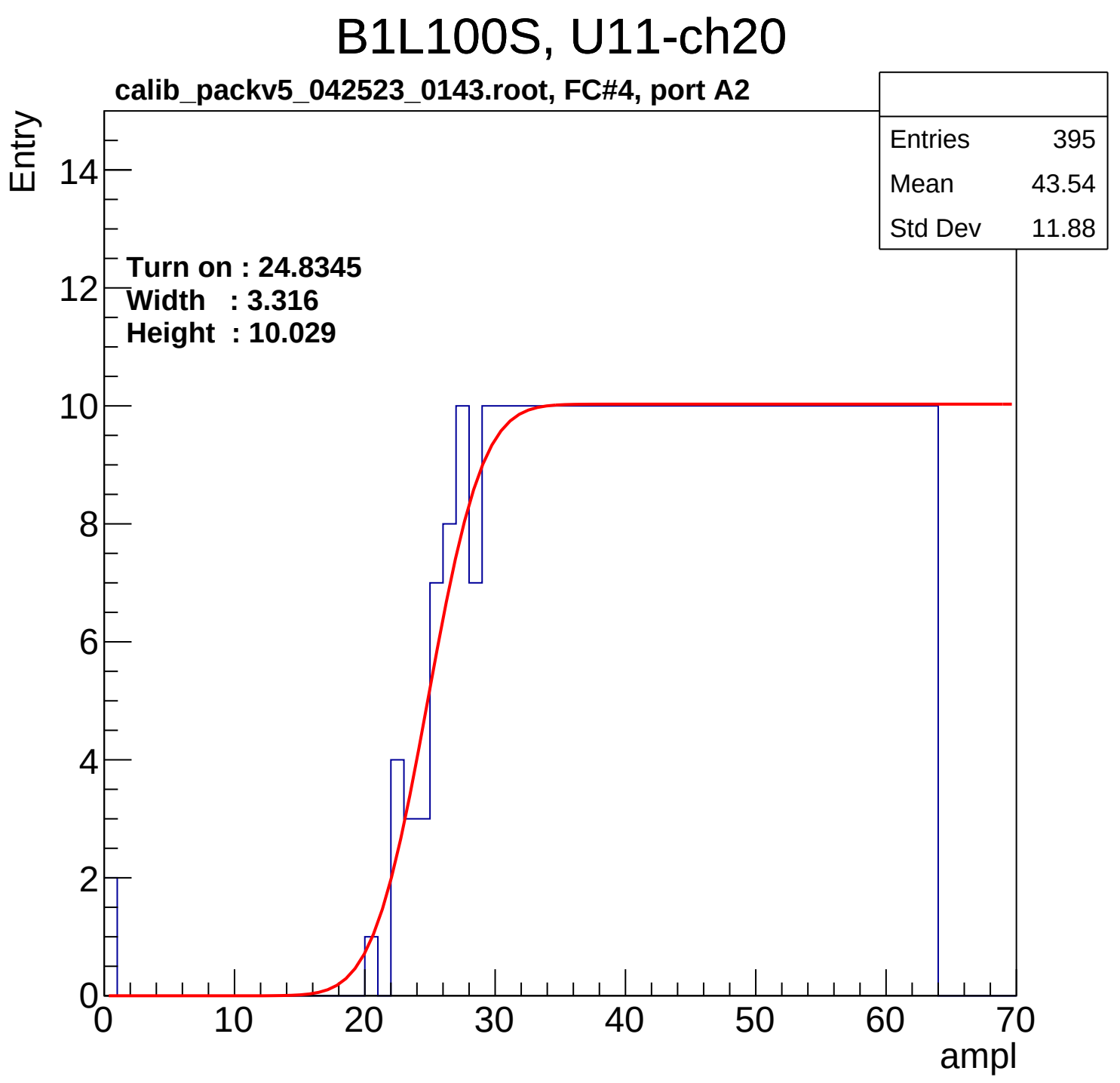
B1L100S, U11-ch20
calib_packv5_042523_0143.root, FC#4, port A2
Entries 395
Mean 43.54
Std Dev 11.88
Turn on : 24.8345
Width : 3.316
Height : 10.029
Entry
ampl
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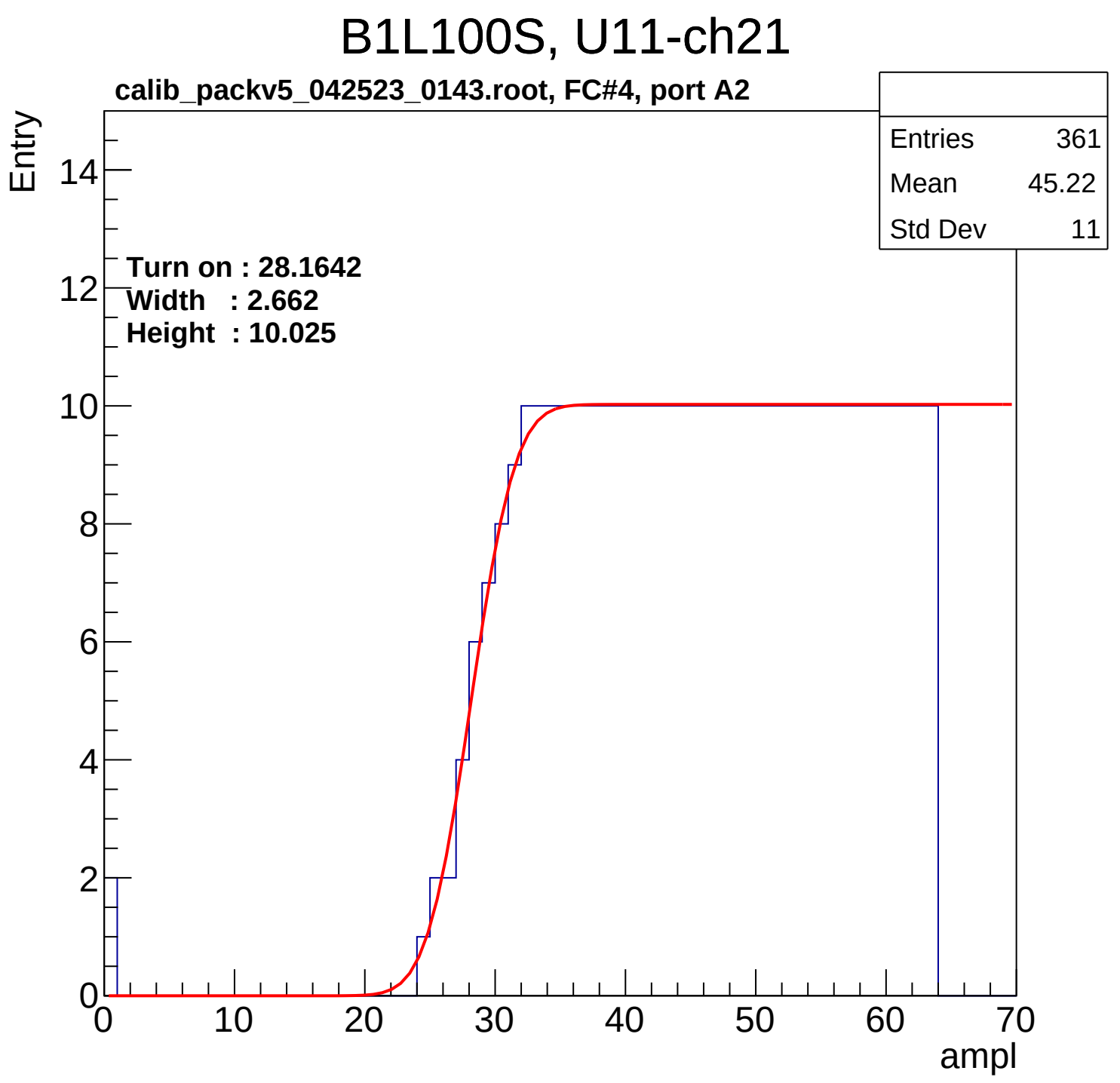
B1L100S, U11-ch21
calib_packv5_042523_0143.root, FC#4, port A2
Entries 361
Mean 45.22
Std Dev 11
Turn on : 28.1642
Width : 2.662
Height : 10.025
Entry
ampl
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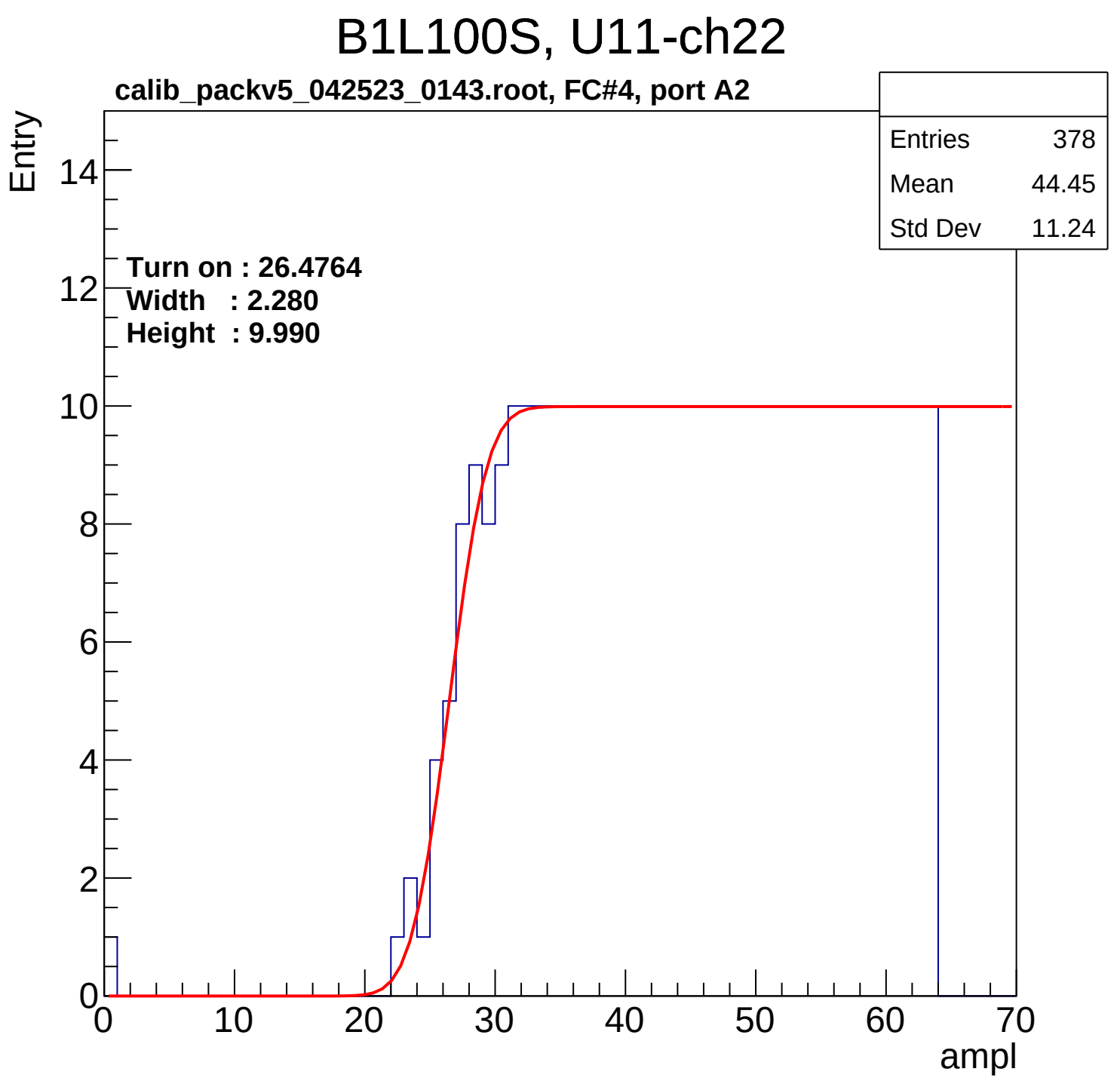
B1L100S, U11-ch22
calib_packv5_042523_0143.root, FC#4, port A2
Entries 378
Mean 44.45
Std Dev 11.24
Turn on : 26.4764
Width : 2.280
Height : 9.990
Entry
ampl
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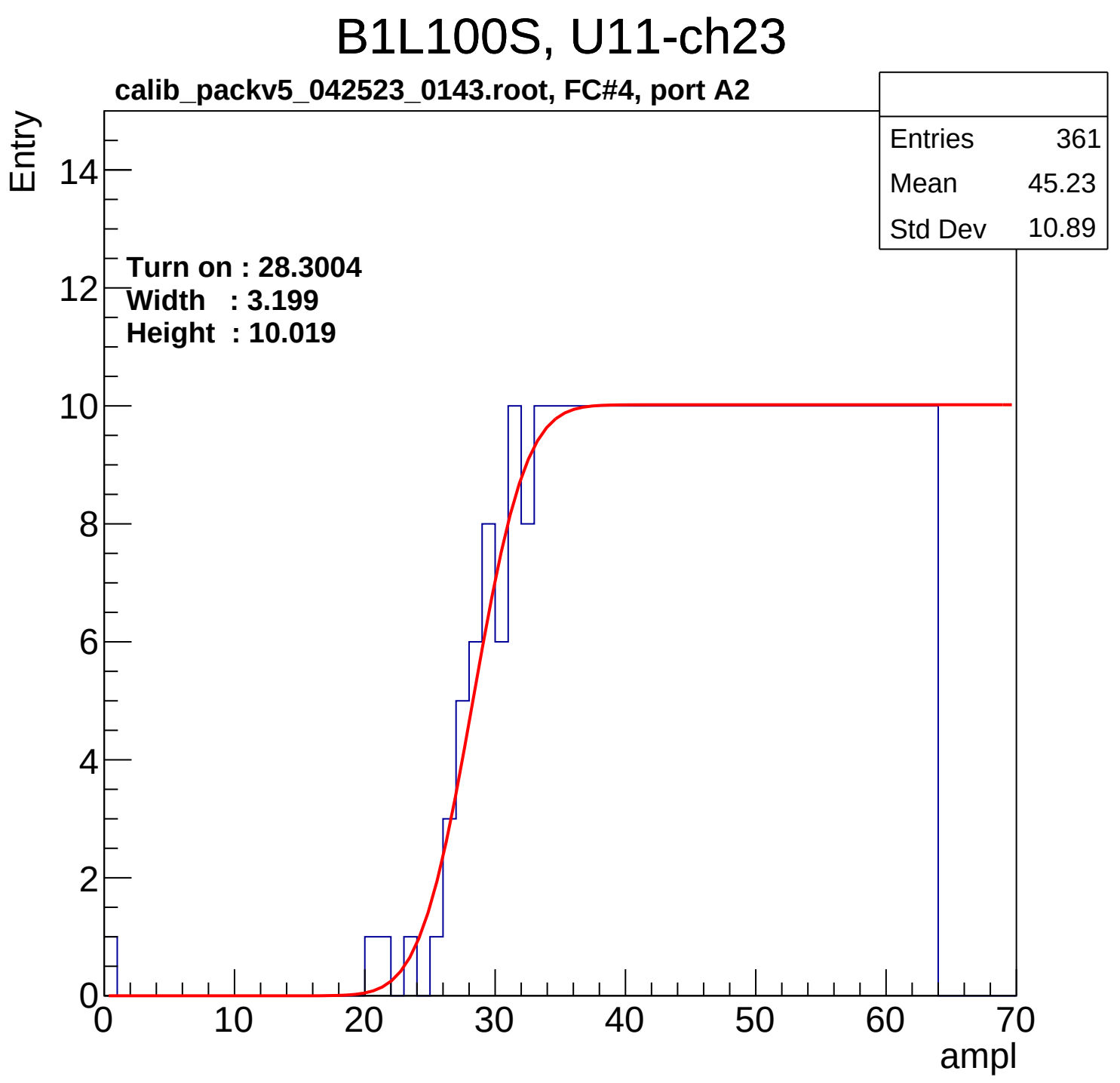
B1L100S, U11-ch23
calib_packv5_042523_0143.root, FC#4, port A2
Entries 361
Mean 45.23
Std Dev 10.89
Turn on : 28.3004
Width : 3.199
Height : 10.019
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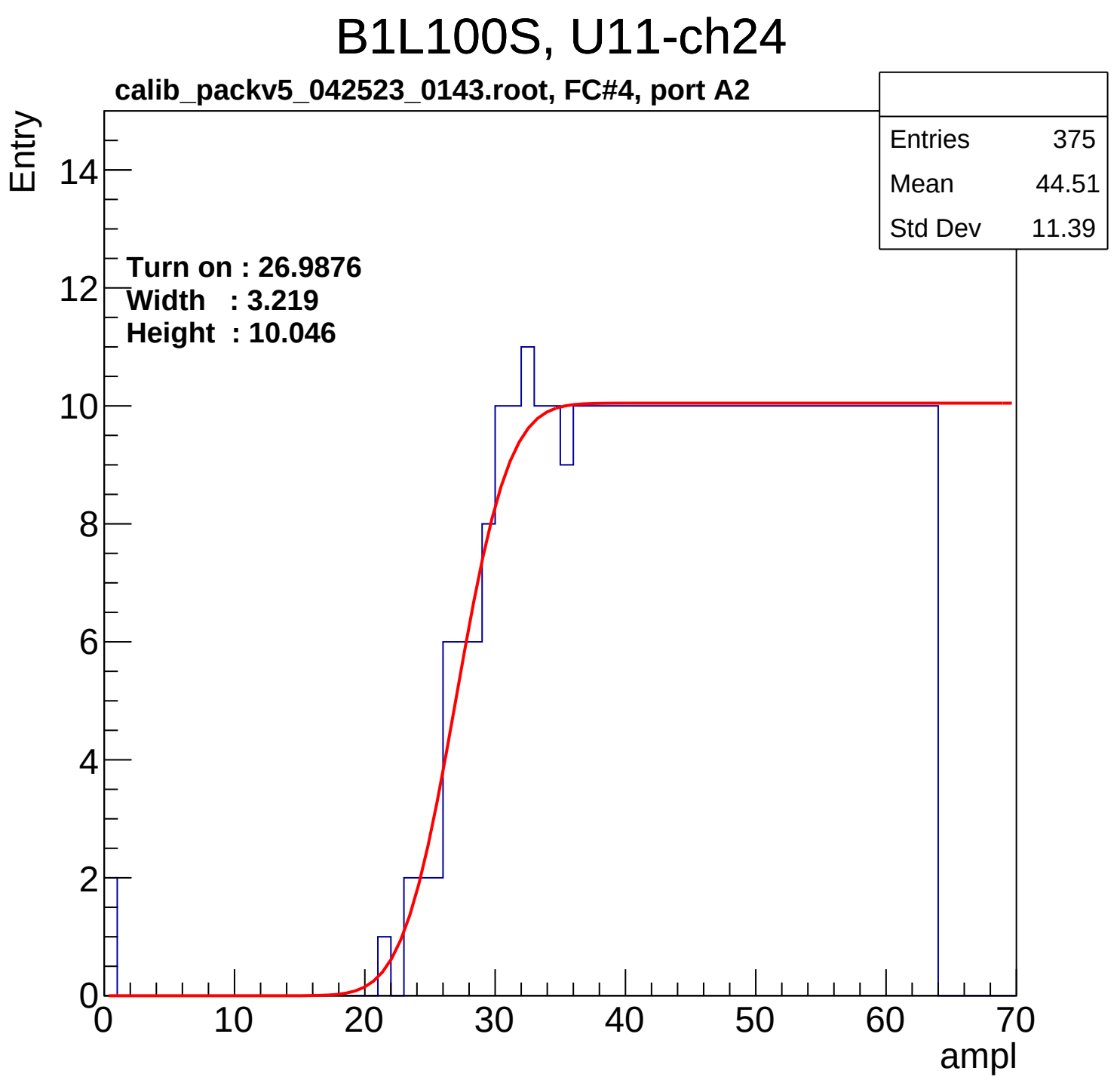
B1L100S, U11-ch24
calib_packv5_042523_0143.root, FC#4, port A2
Entries 375
Mean 44.51
Std Dev 11.39
Turn on : 26.9876
Width : 3.219
Height : 10.046
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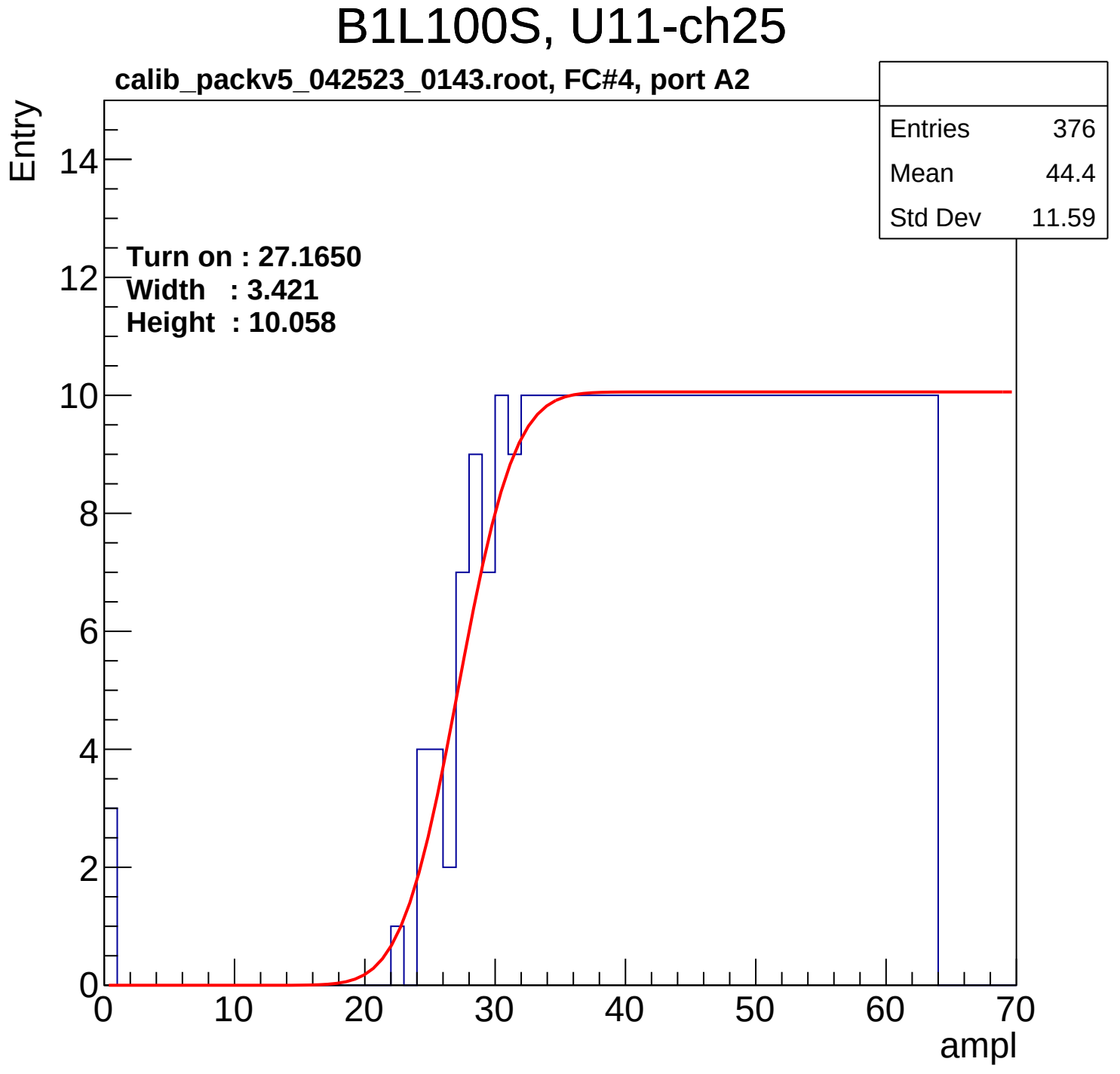
B1L100S, U11-ch25
calib_packv5_042523_0143.root, FC#4, port A2
Entries 376
Mean 44.4
Std Dev 11.59
Turn on : 27.1650
Width : 3.421
Height : 10.058
Entry
ampl
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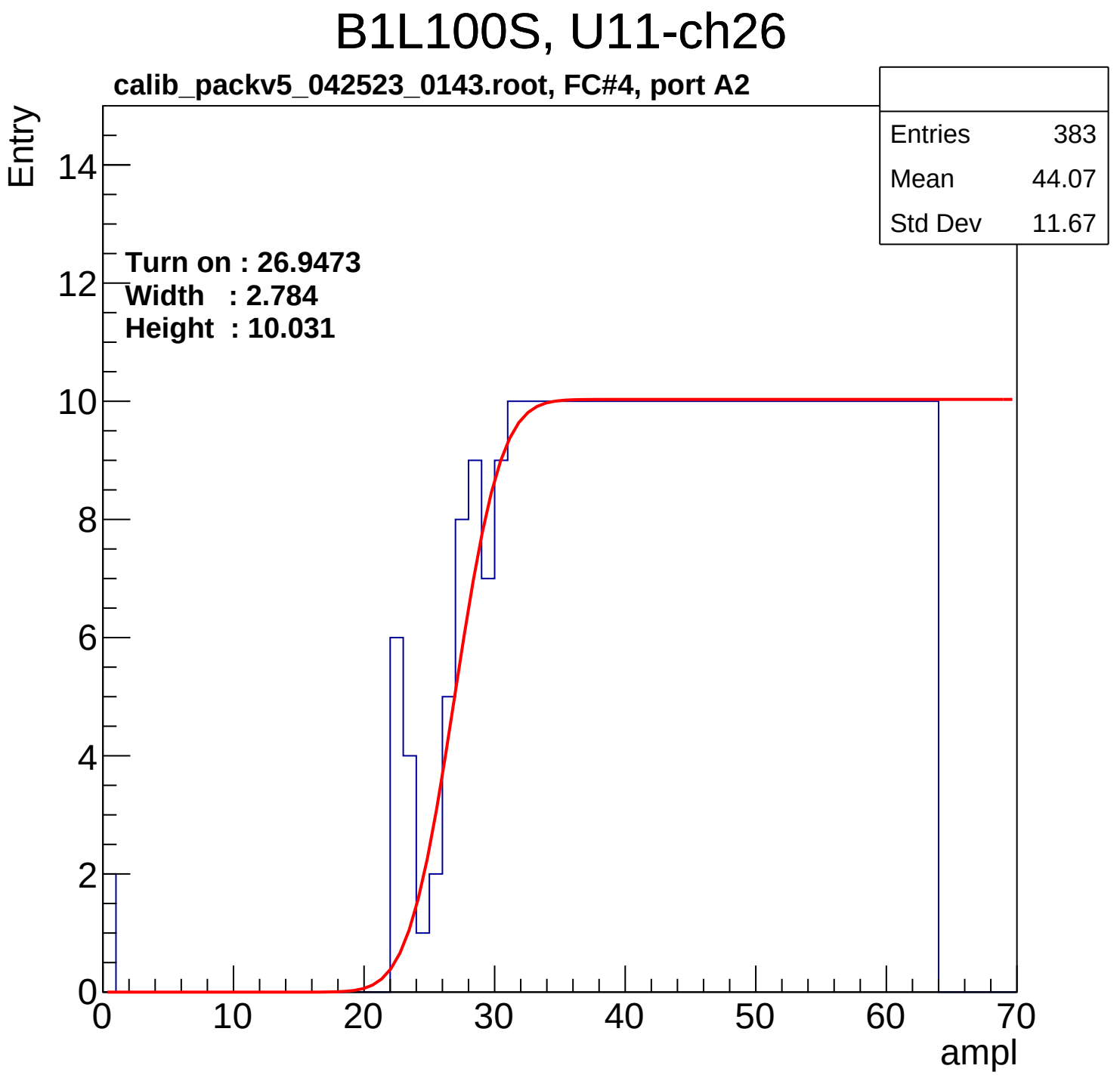
B1L100S, U11-ch26
calib_packv5_042523_0143.root, FC#4, port A2
Entries 383
Mean 44.07
Std Dev 11.67
Turn on : 26.9473
Width : 2.784
Height : 10.031
Entry
ampl
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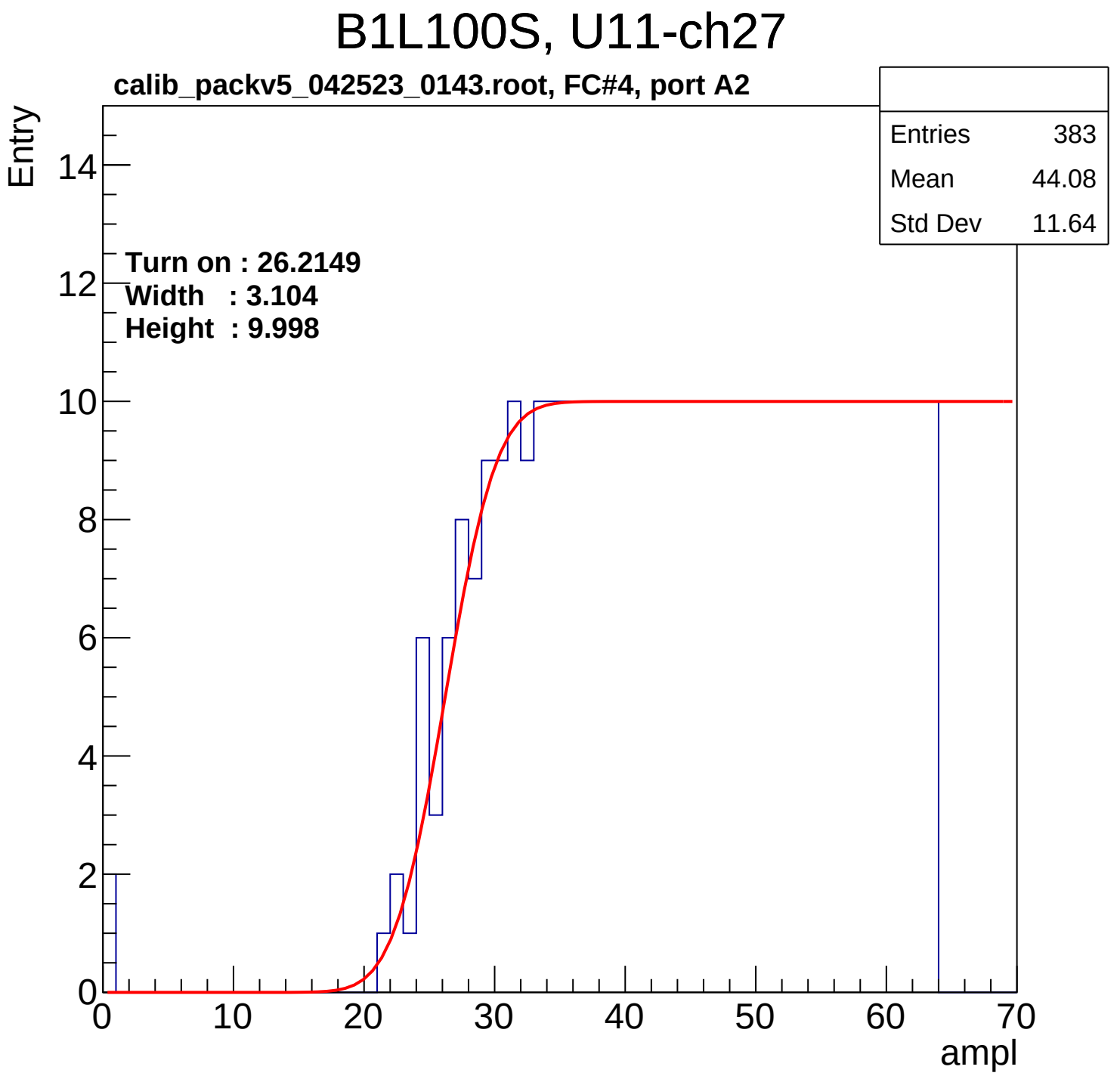
B1L100S, U11-ch27
calib_packv5_042523_0143.root, FC#4, port A2
Entries 383
Mean 44.08
Std Dev 11.64
Turn on : 26.2149
Width : 3.104
Height : 9.998
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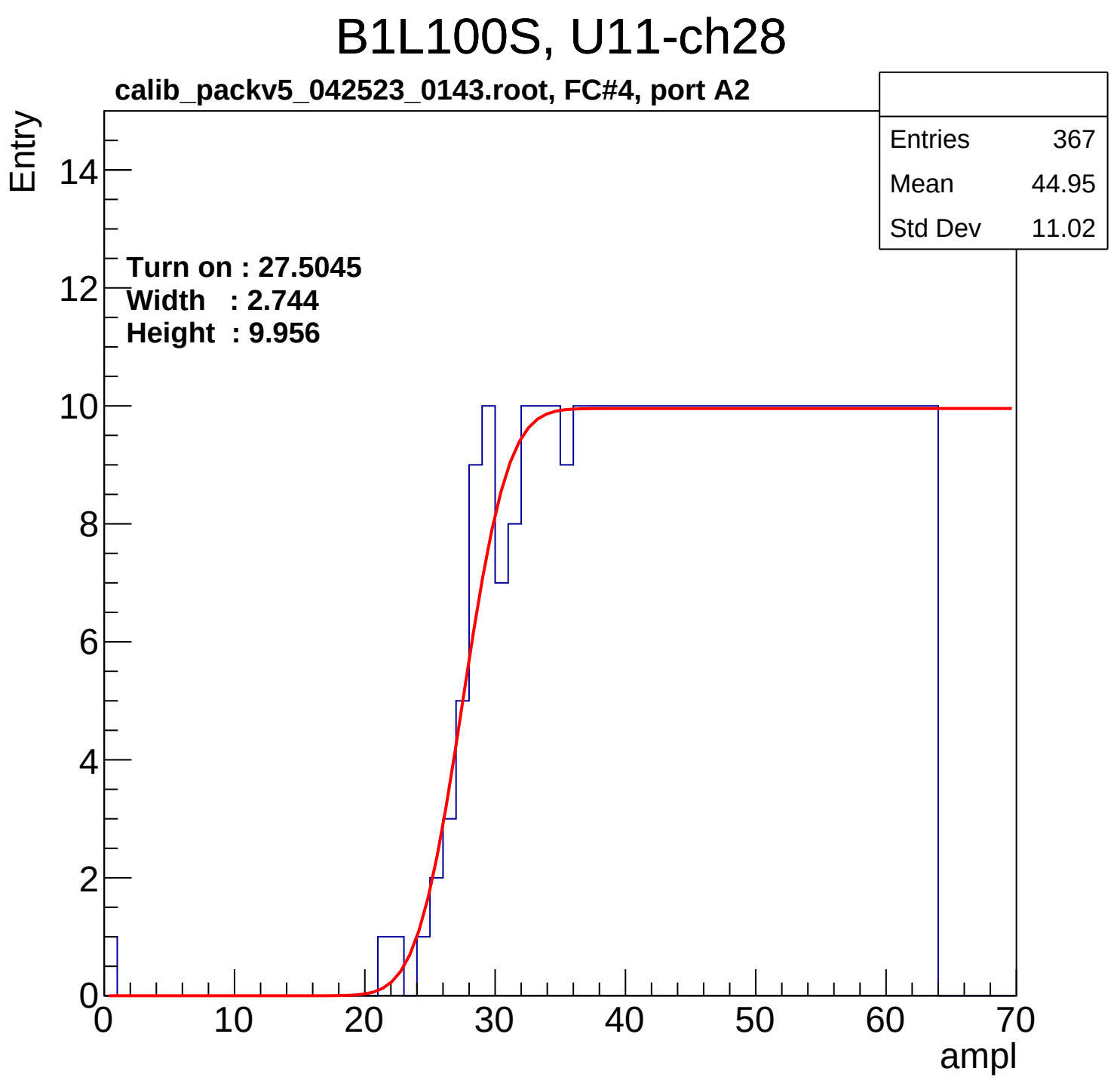
B1L100S, U11-ch28
calib_packv5_042523_0143.root, FC#4, port A2
Entries 367
Mean 44.95
Std Dev 11.02
Turn on : 27.5045
Width : 2.744
Height : 9.956
Entry
ampl
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4
6
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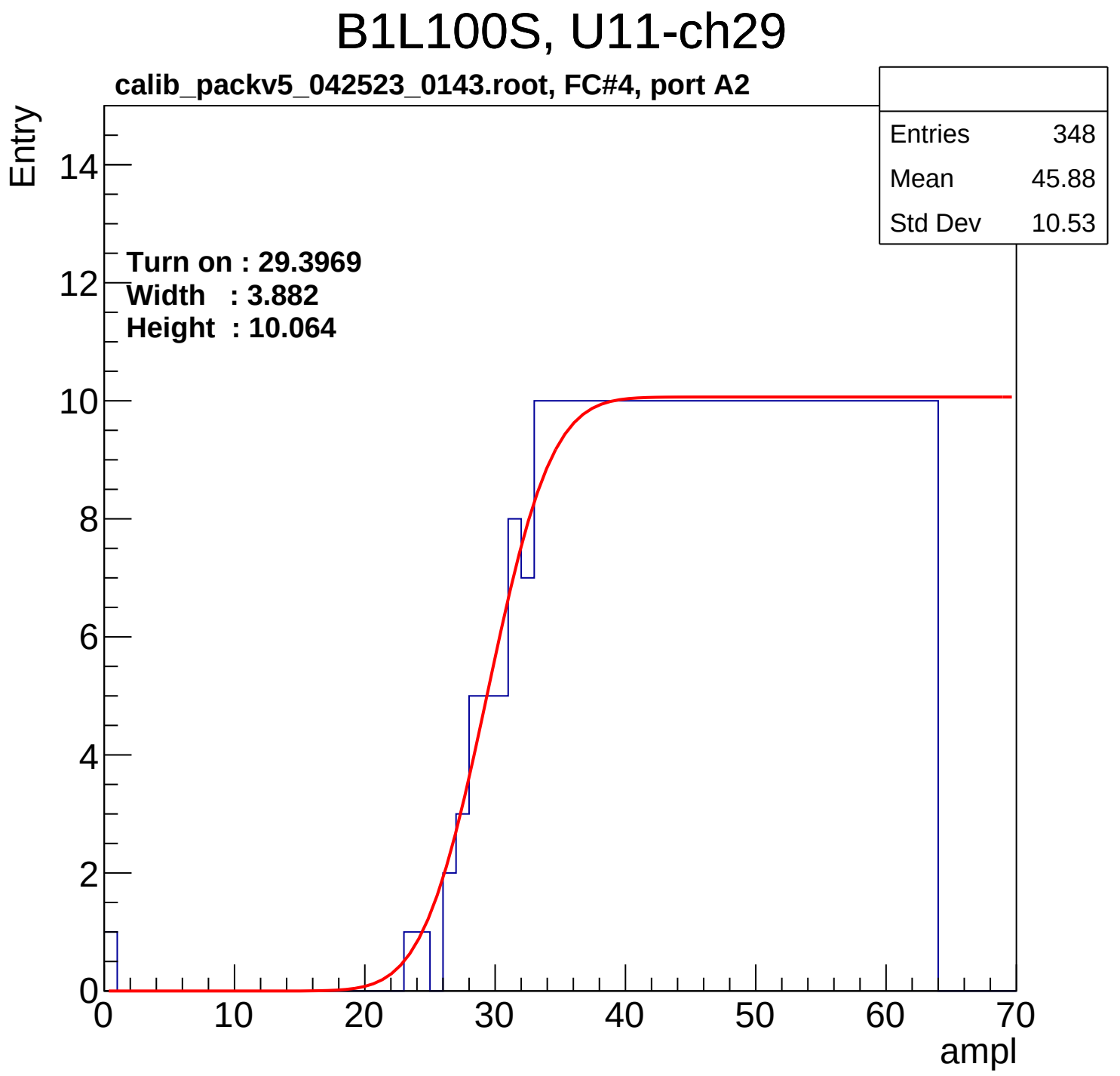
B1L100S, U11-ch29
calib_packv5_042523_0143.root, FC#4, port A2
Entries 348
Mean 45.88
Std Dev 10.53
Turn on : 29.3969
Width : 3.882
Height : 10.064
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ampl
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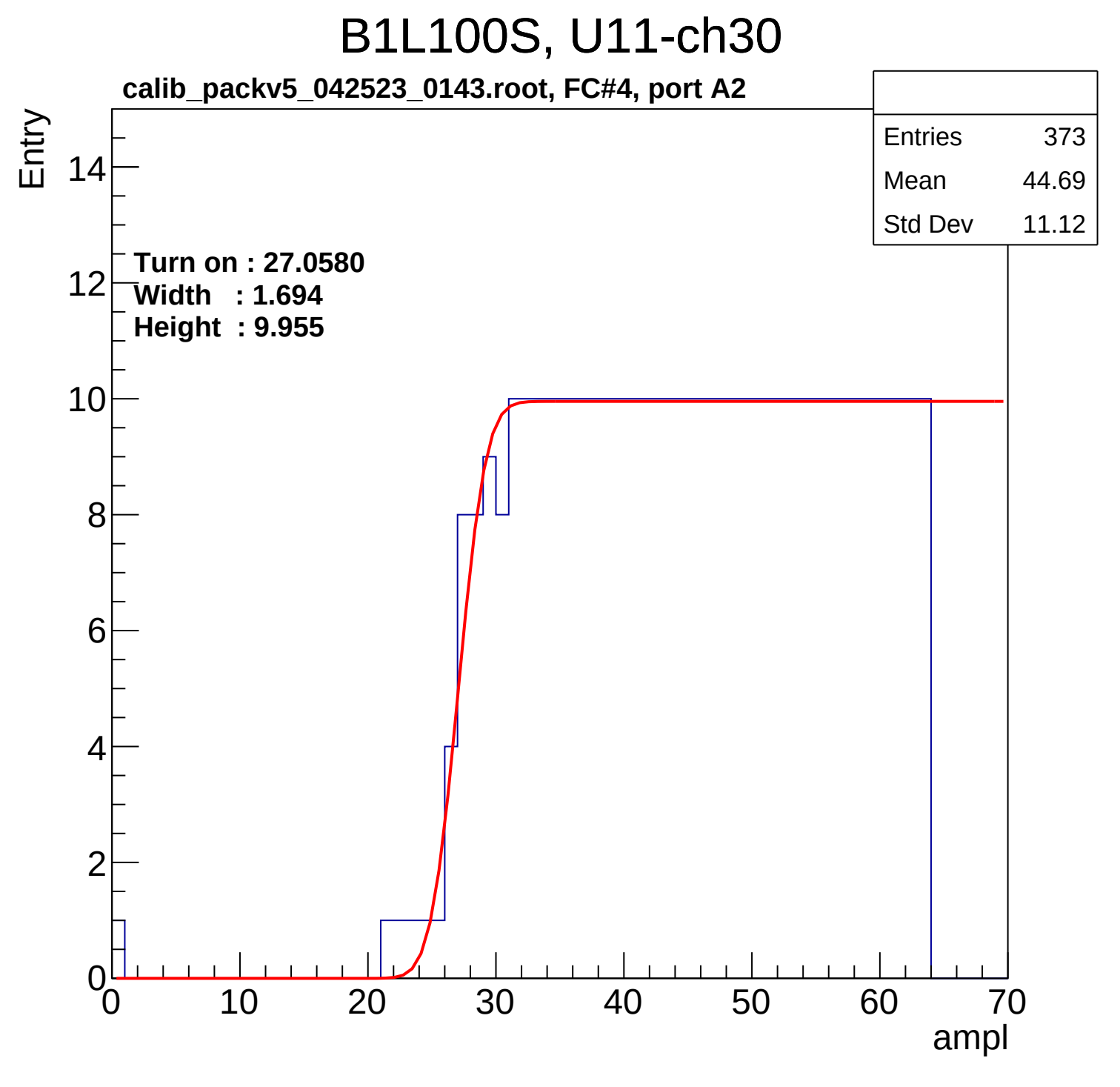
B1L100S, U11-ch30
calib_packv5_042523_0143.root, FC#4, port A2
Entries 373
Mean 44.69
Std Dev 11.12
Turn on : 27.0580
Width : 1.694
Height : 9.955
Entry
ampl
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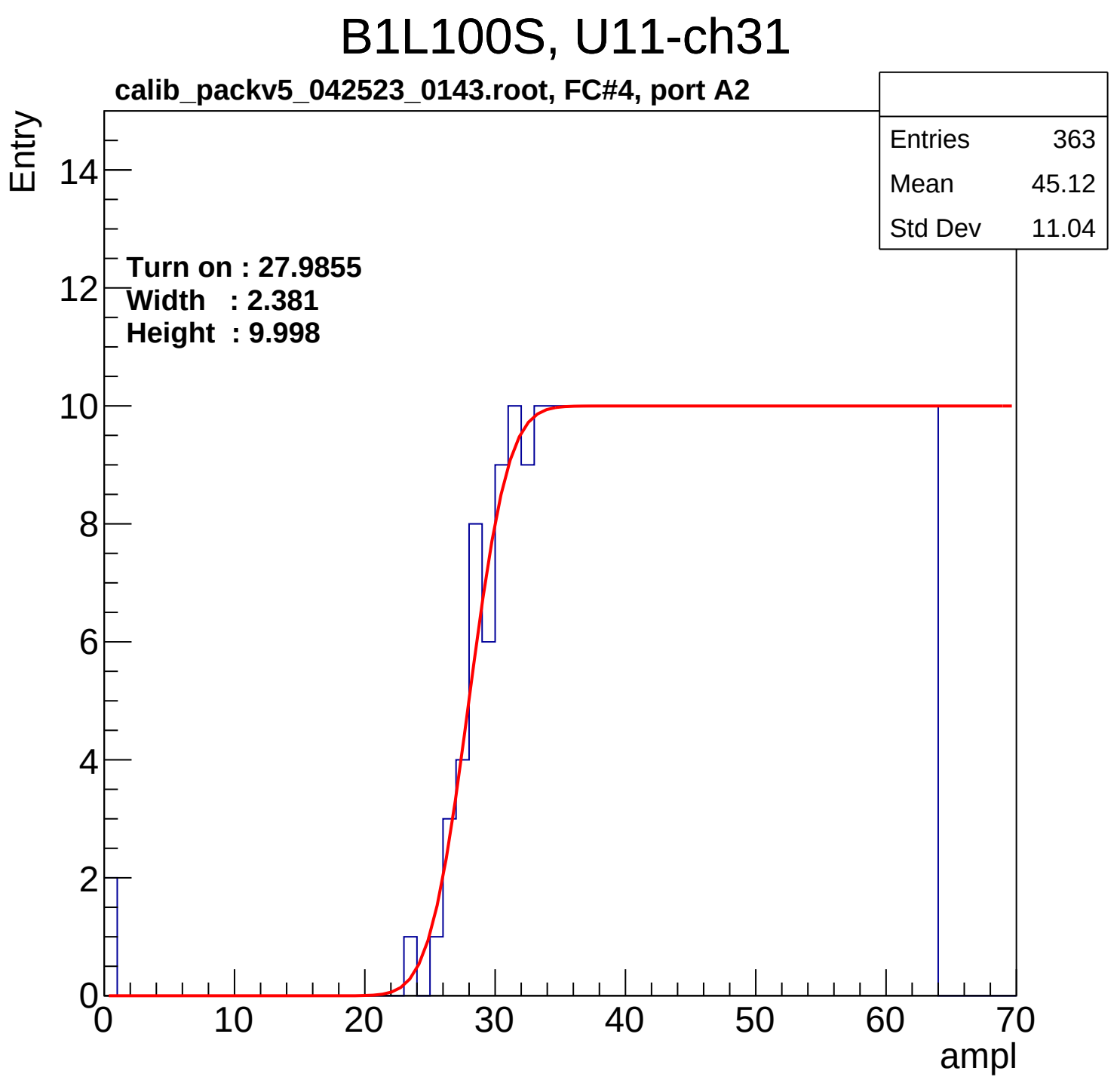
B1L100S, U11-ch31
calib_packv5_042523_0143.root, FC#4, port A2
Entries 363
Mean 45.12
Std Dev 11.04
Turn on : 27.9855
Width : 2.381
Height : 9.998
Entry
ampl
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2
4
6
8
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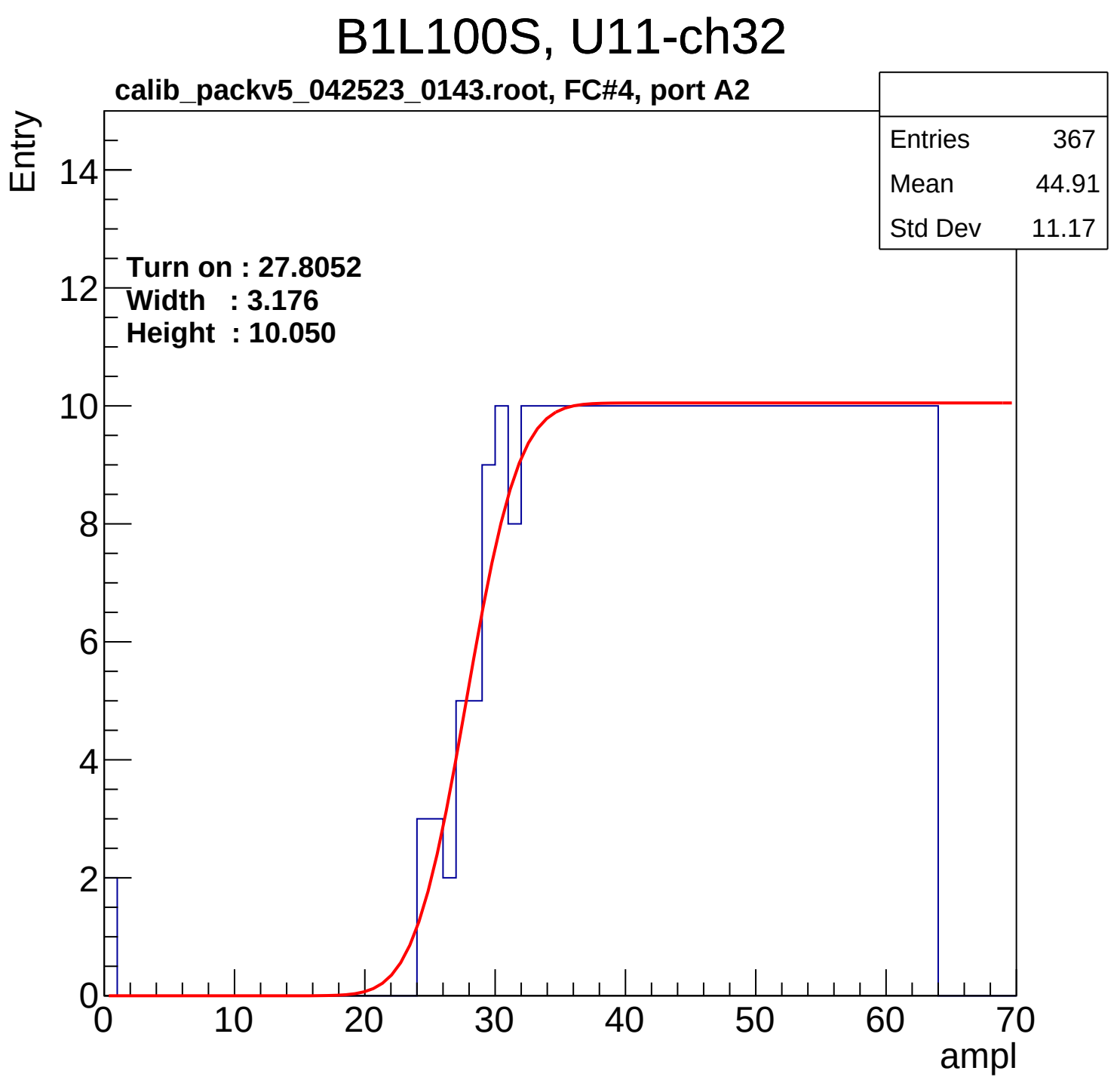
B1L100S, U11-ch32
calib_packv5_042523_0143.root, FC#4, port A2
Entries 367
Mean 44.91
Std Dev 11.17
Turn on : 27.8052
Width : 3.176
Height : 10.050
Entry
ampl
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2
4
6
8
10
12
14
0
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60
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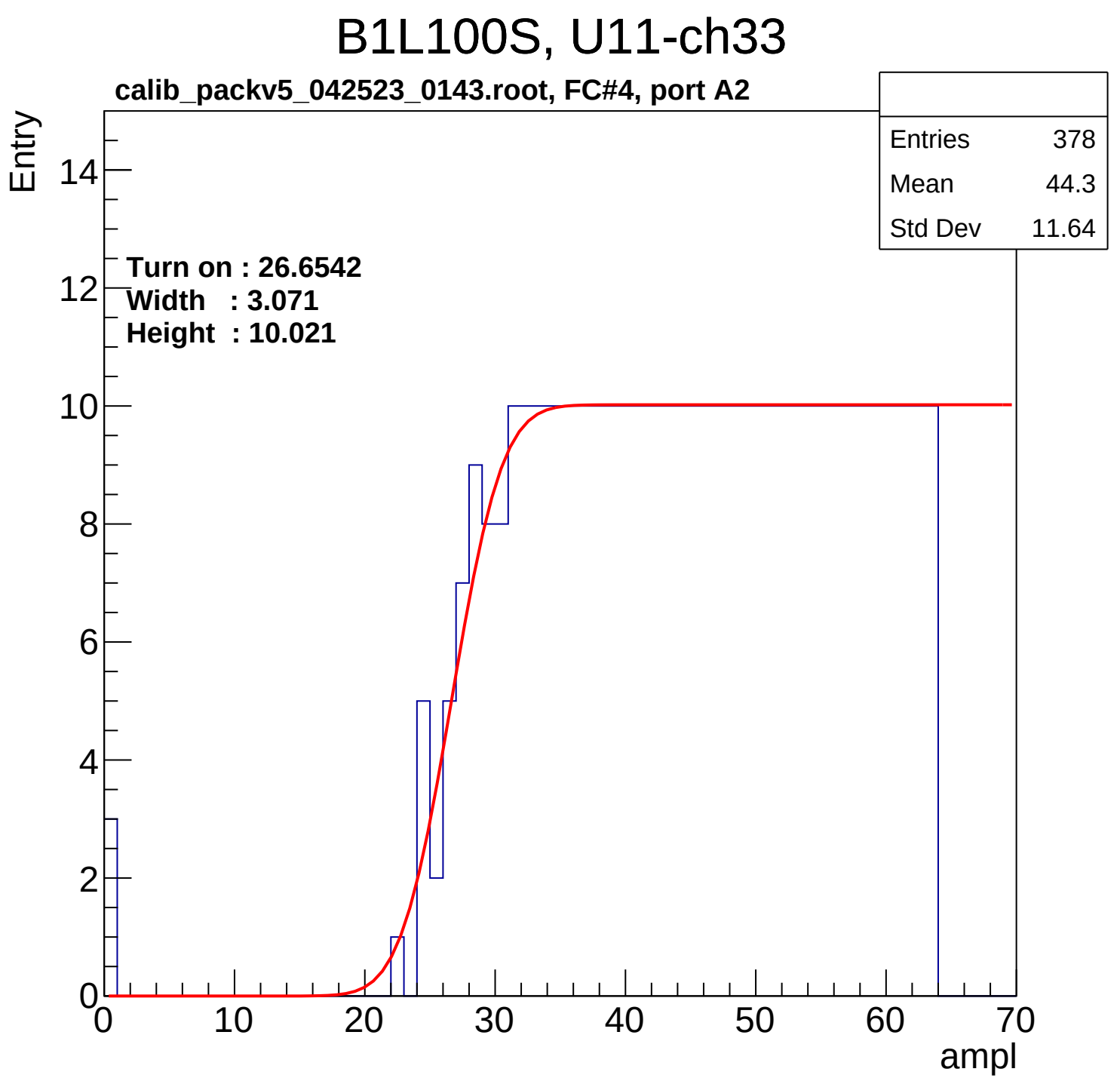
B1L100S, U11-ch33
calib_packv5_042523_0143.root, FC#4, port A2
Entries 378
Mean 44.3
Std Dev 11.64
Turn on : 26.6542
Width : 3.071
Height : 10.021
Entry
ampl
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2
4
6
8
10
12
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0
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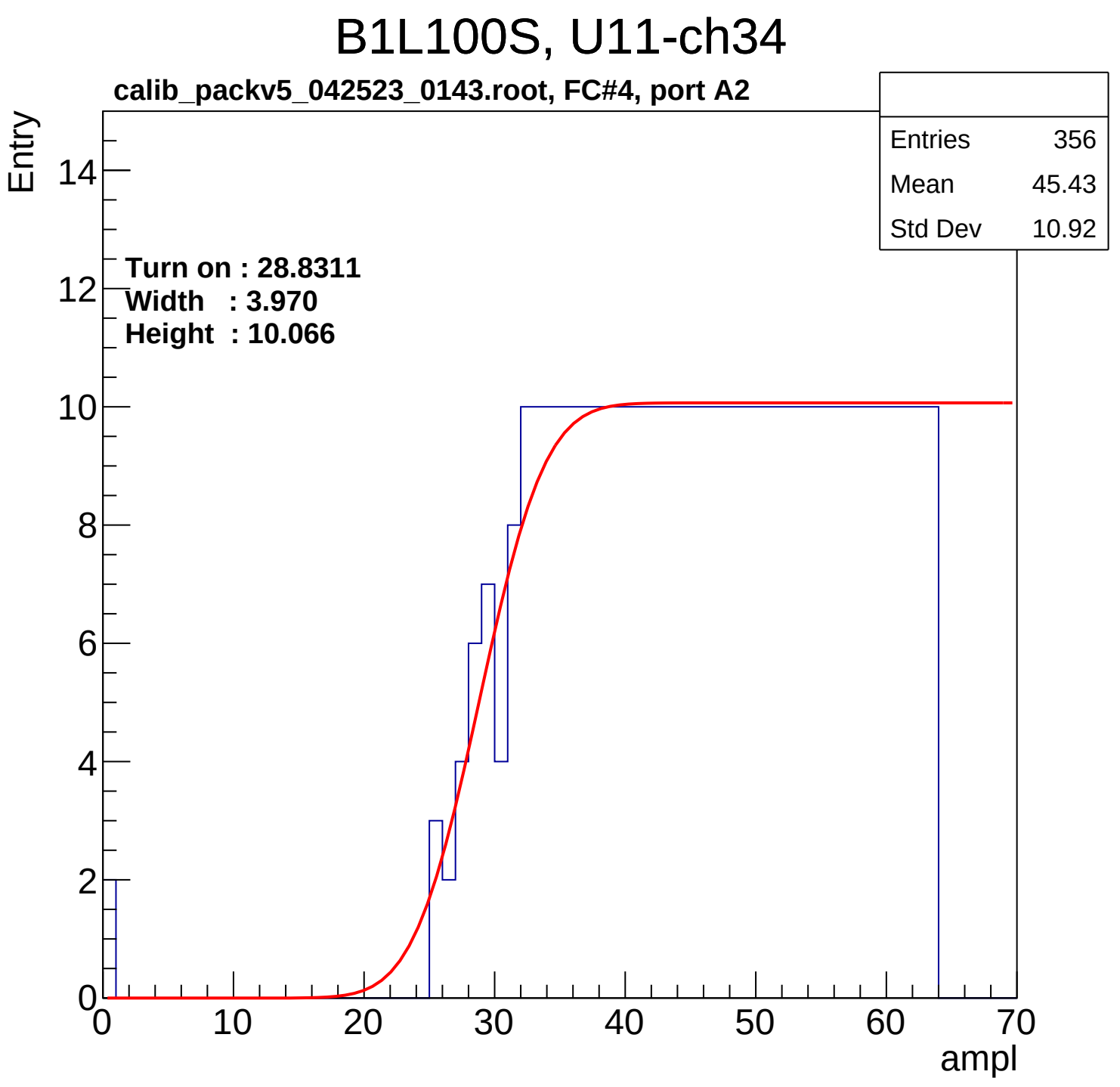
B1L100S, U11-ch34
calib_packv5_042523_0143.root, FC#4, port A2
Entries 356
Mean 45.43
Std Dev 10.92
Turn on : 28.8311
Width : 3.970
Height : 10.066
Entry
ampl
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4
6
8
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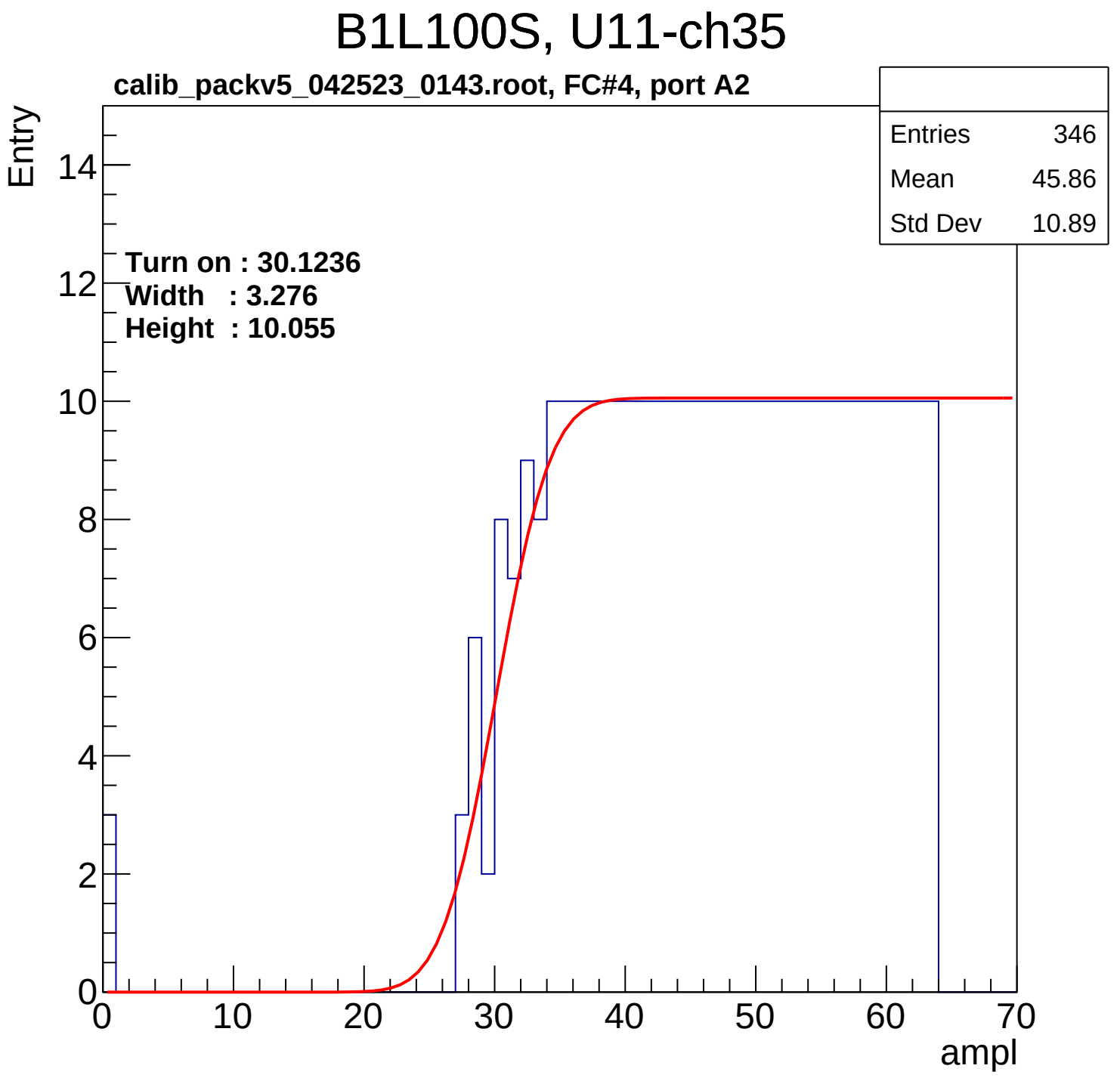
B1L100S, U11-ch35
calib_packv5_042523_0143.root, FC#4, port A2
Entries 346
Mean 45.86
Std Dev 10.89
Turn on : 30.1236
Width : 3.276
Height : 10.055
Entry
ampl
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6
8
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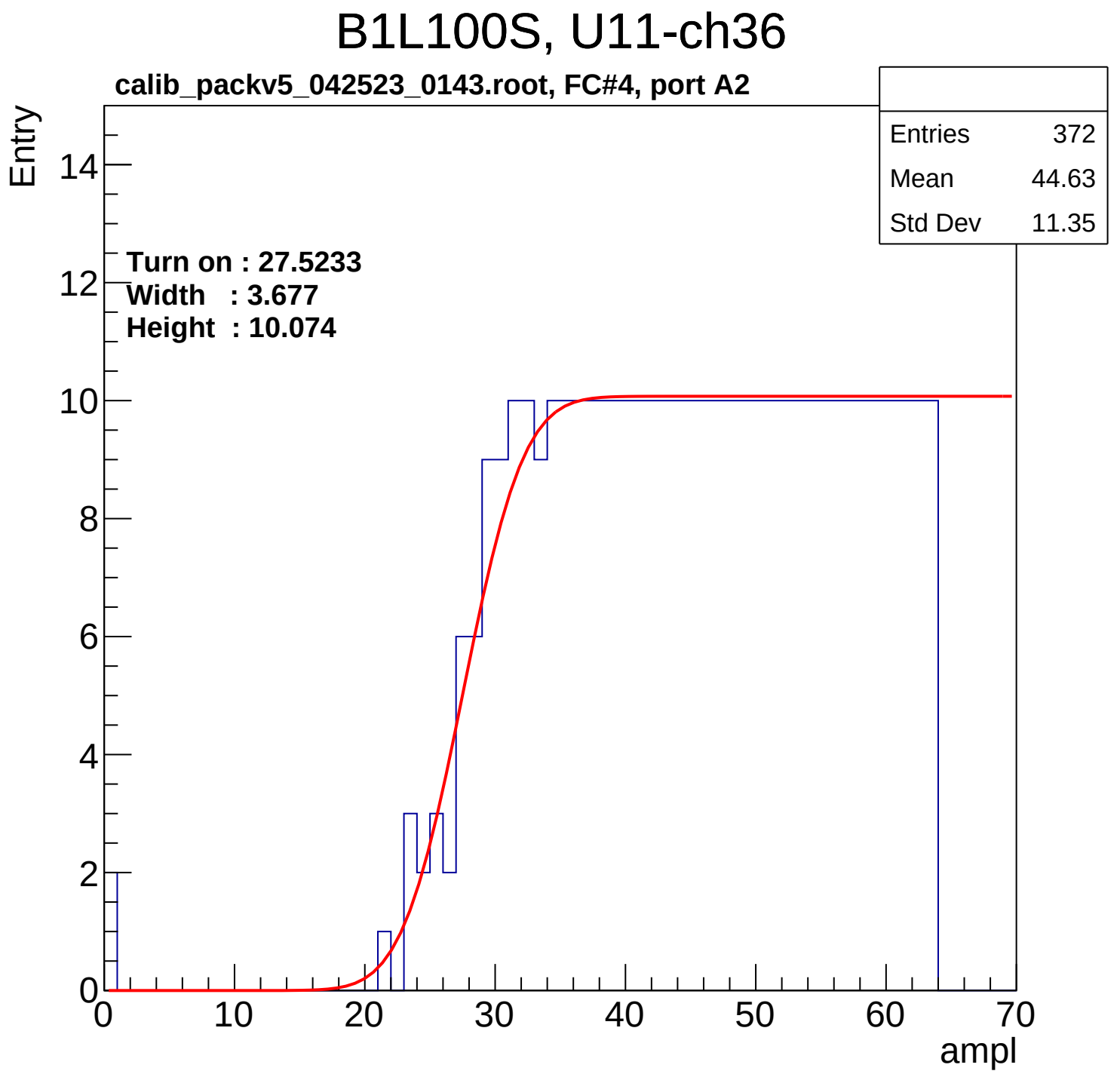
B1L100S, U11-ch36
calib_packv5_042523_0143.root, FC#4, port A2
Entries 372
Mean 44.63
Std Dev 11.35
Turn on : 27.5233
Width : 3.677
Height : 10.074
Entry
ampl
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2
4
6
8
10
12
14
0
10
20
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40
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60
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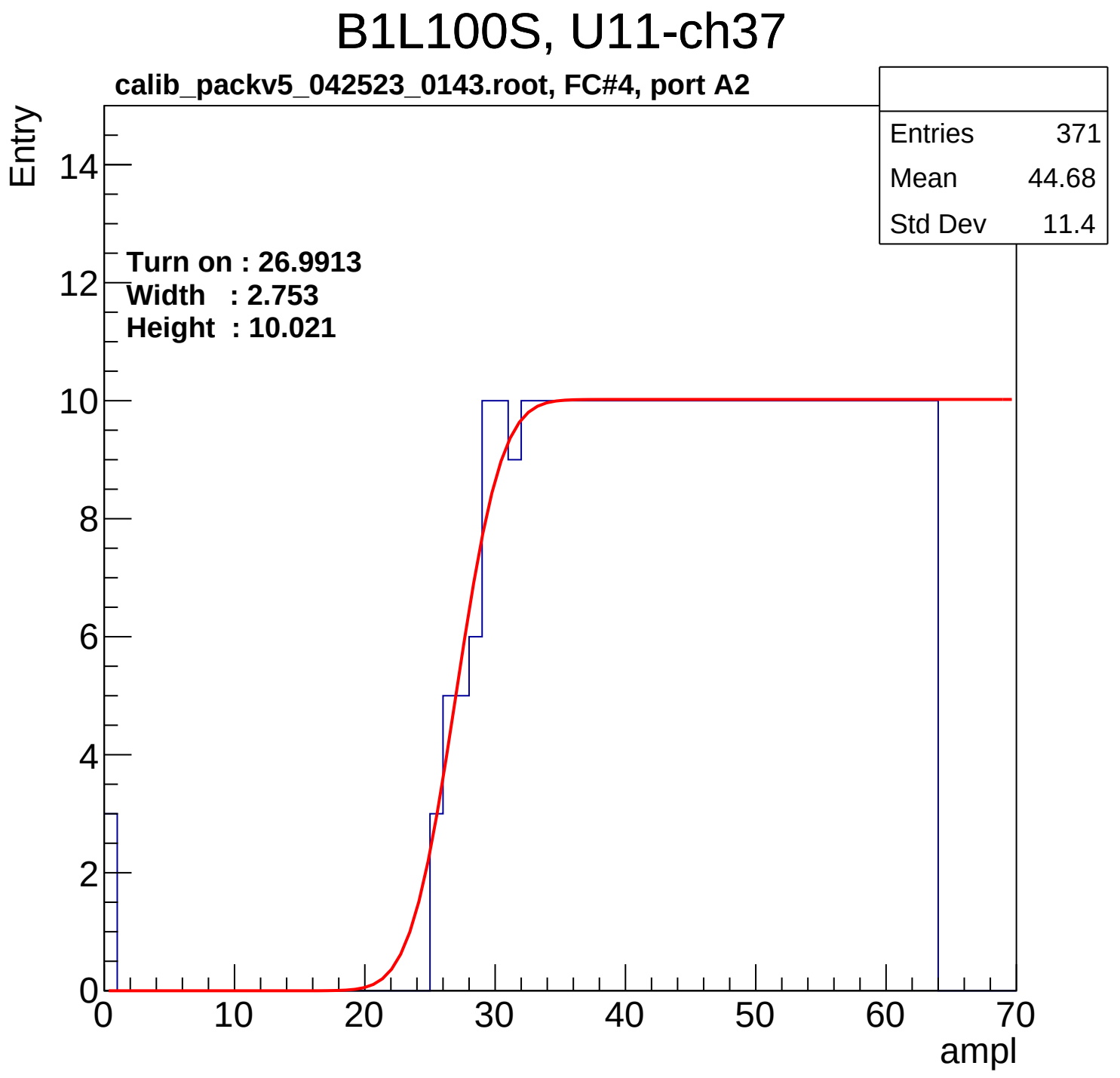
B1L100S, U11-ch37
calib_packv5_042523_0143.root, FC#4, port A2
Entries 371
Mean 44.68
Std Dev 11.4
Turn on : 26.9913
Width : 2.753
Height : 10.021
Entry
ampl
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2
4
6
8
10
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0
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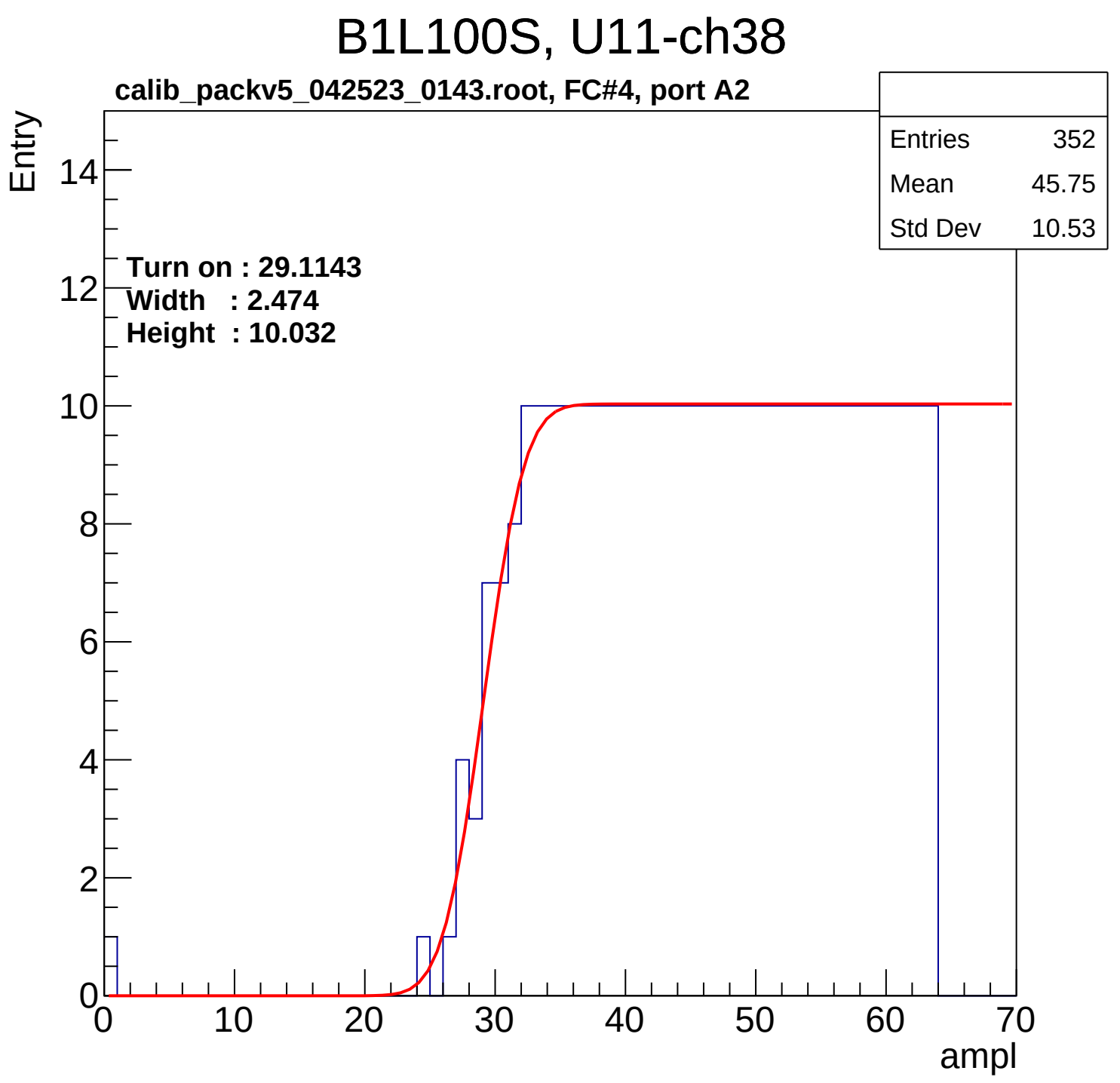
B1L100S, U11-ch38
calib_packv5_042523_0143.root, FC#4, port A2
Entries 352
Mean 45.75
Std Dev 10.53
Turn on : 29.1143
Width : 2.474
Height : 10.032
Entry
ampl
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2
4
6
8
10
12
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0
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20
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60
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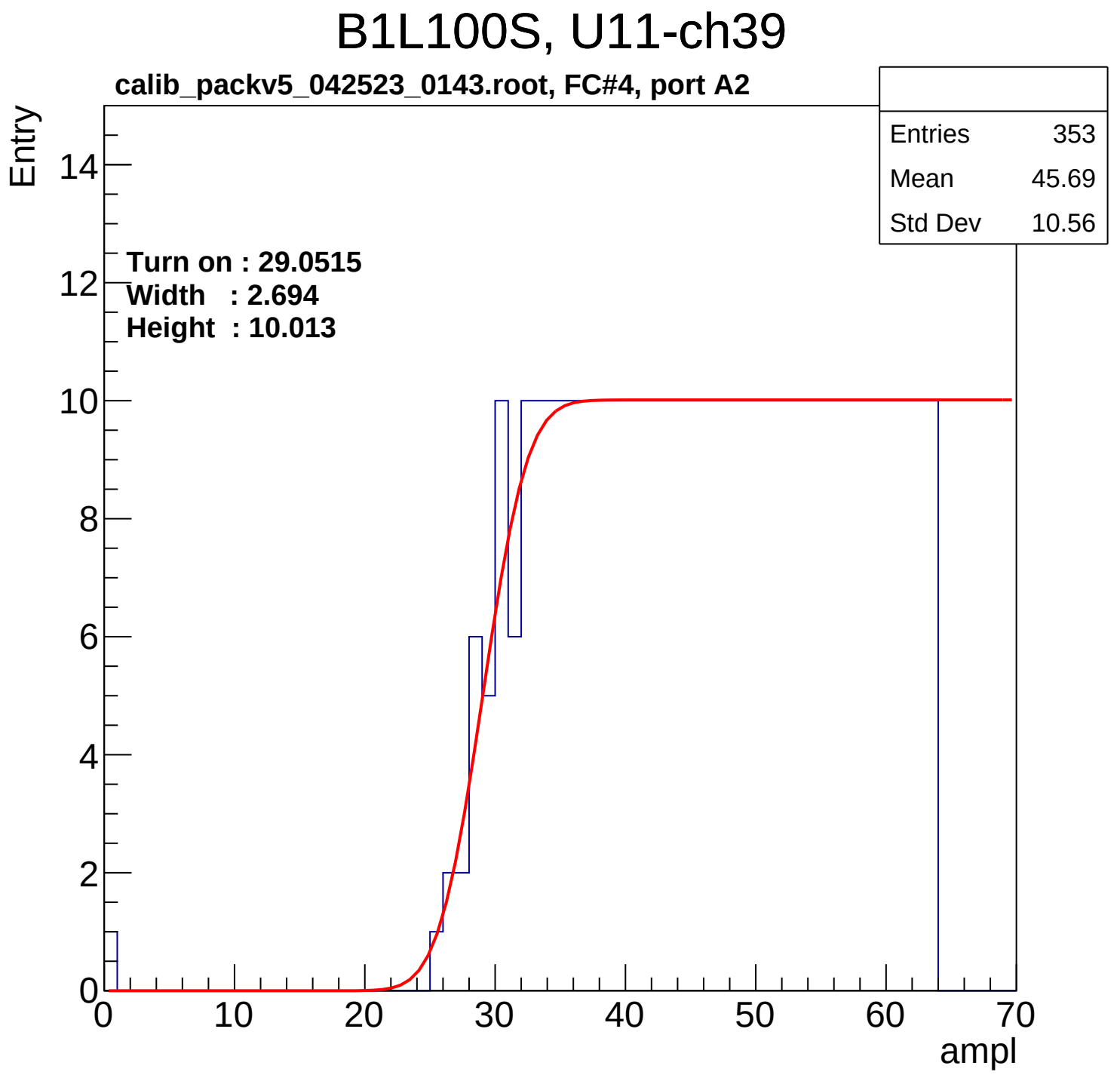
B1L100S, U11-ch39
calib_packv5_042523_0143.root, FC#4, port A2
Entries 353
Mean 45.69
Std Dev 10.56
Turn on : 29.0515
Width : 2.694
Height : 10.013
Entry
ampl
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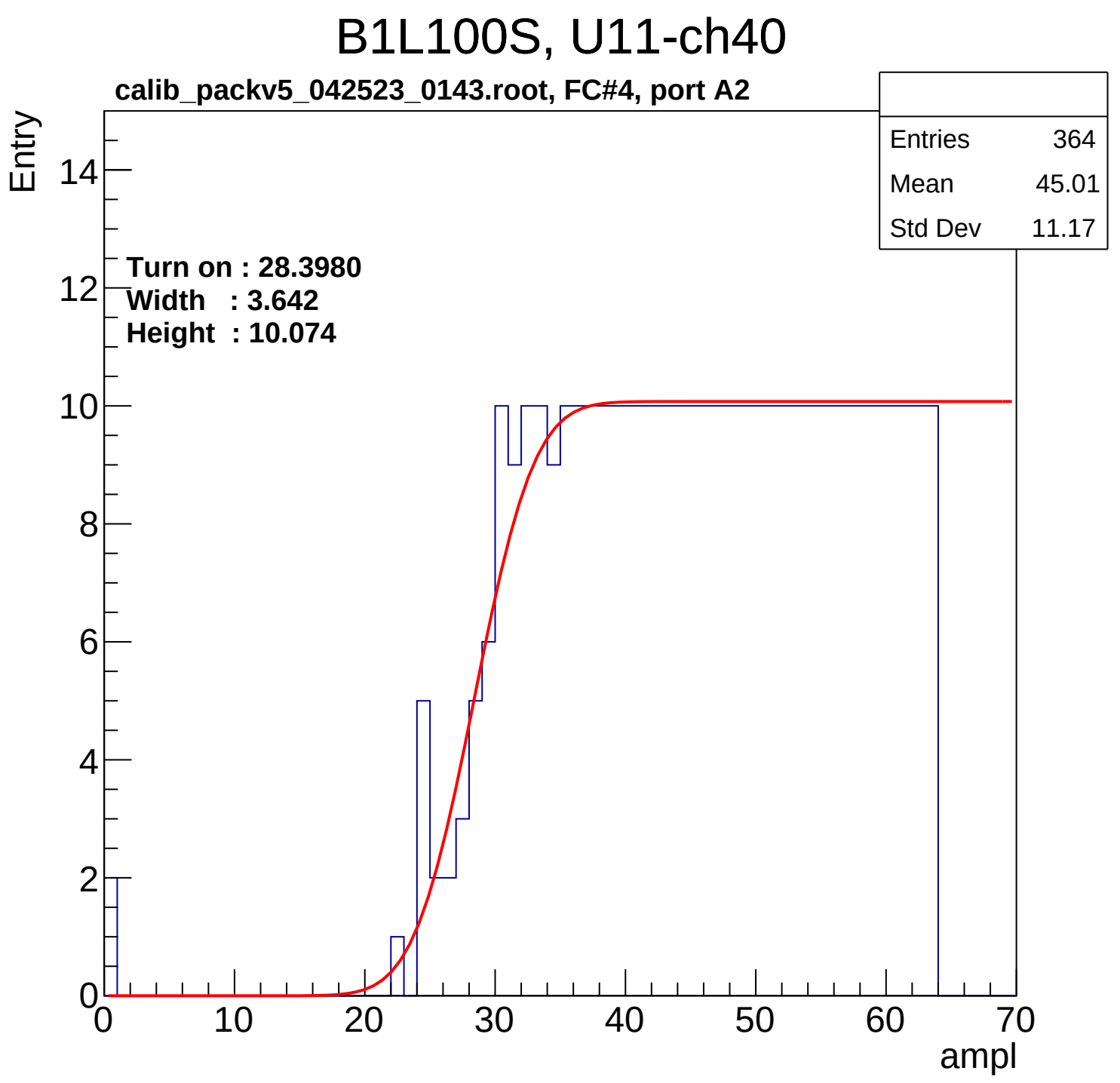
B1L100S, U11-ch40
calib_packv5_042523_0143.root, FC#4, port A2
Entries 364
Mean 45.01
Std Dev 11.17
Turn on : 28.3980
Width : 3.642
Height : 10.074
Entry
ampl
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6
8
10
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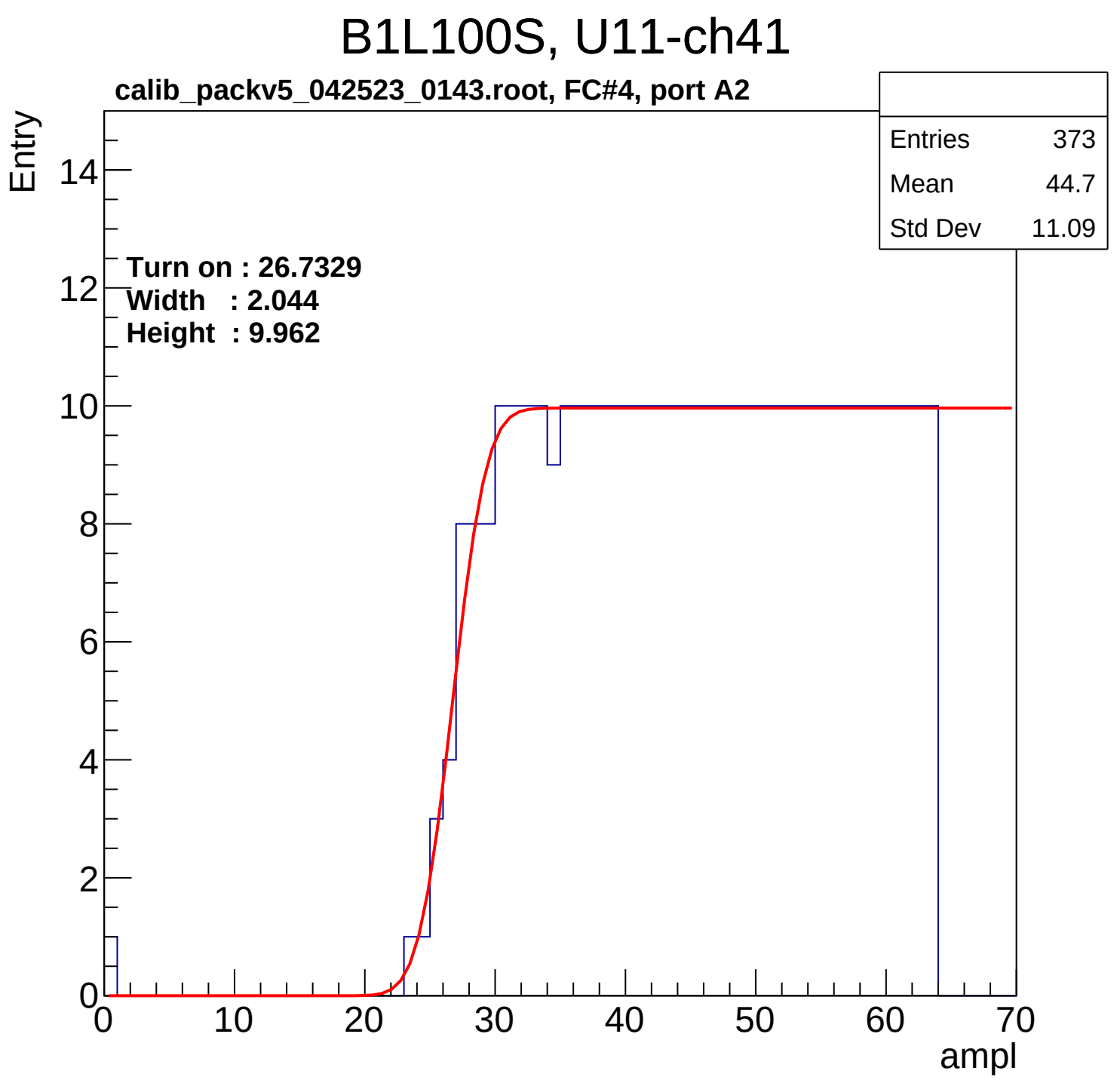
B1L100S, U11-ch41
calib_packv5_042523_0143.root, FC#4, port A2
Entries 373
Mean 44.7
Std Dev 11.09
Turn on : 26.7329
Width : 2.044
Height : 9.962
Entry
ampl
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6
8
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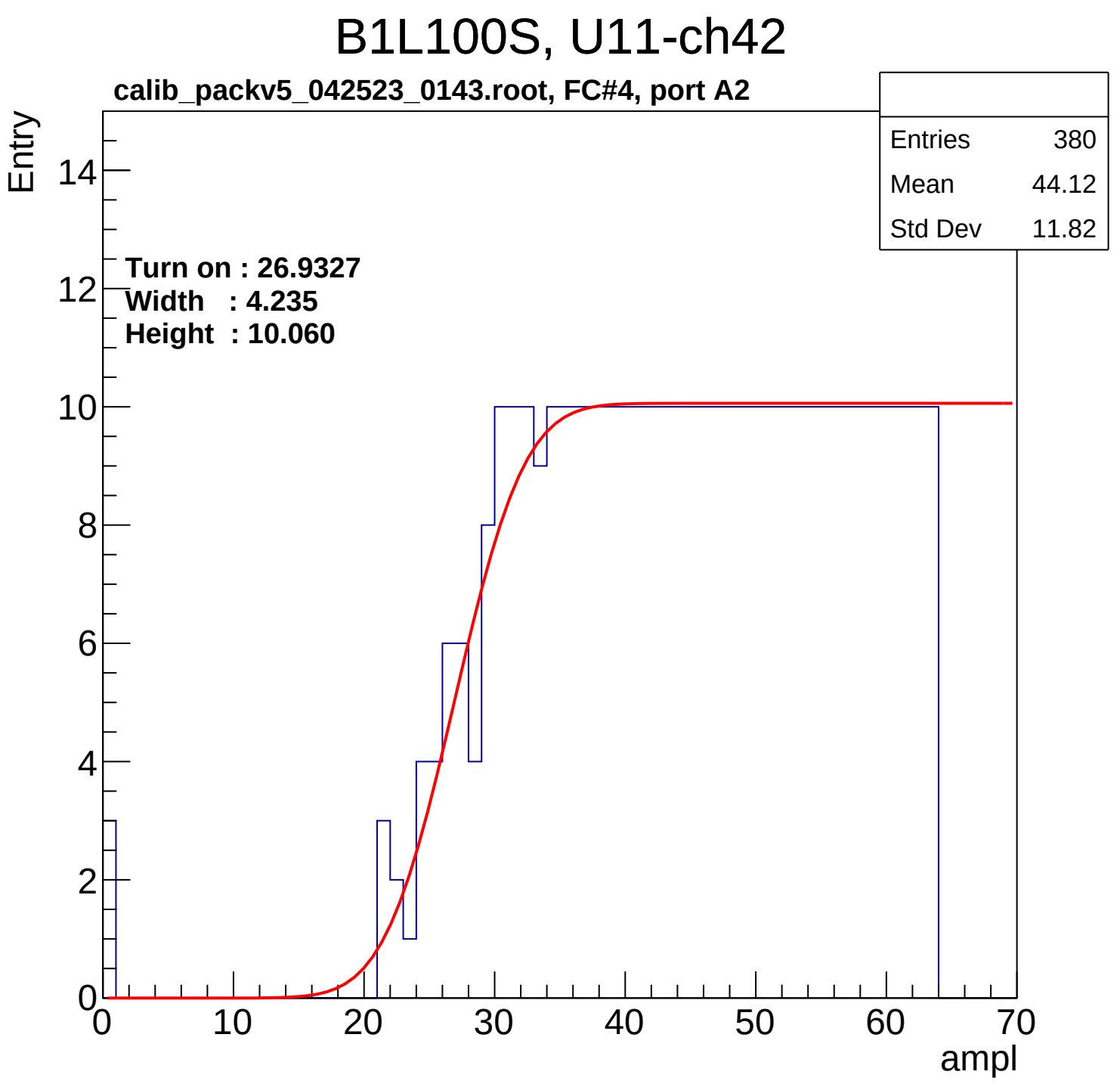
B1L100S, U11-ch42
calib_packv5_042523_0143.root, FC#4, port A2
Entries 380
Mean 44.12
Std Dev 11.82
Turn on : 26.9327
Width : 4.235
Height : 10.060
Entry
ampl
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4
6
8
10
12
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20
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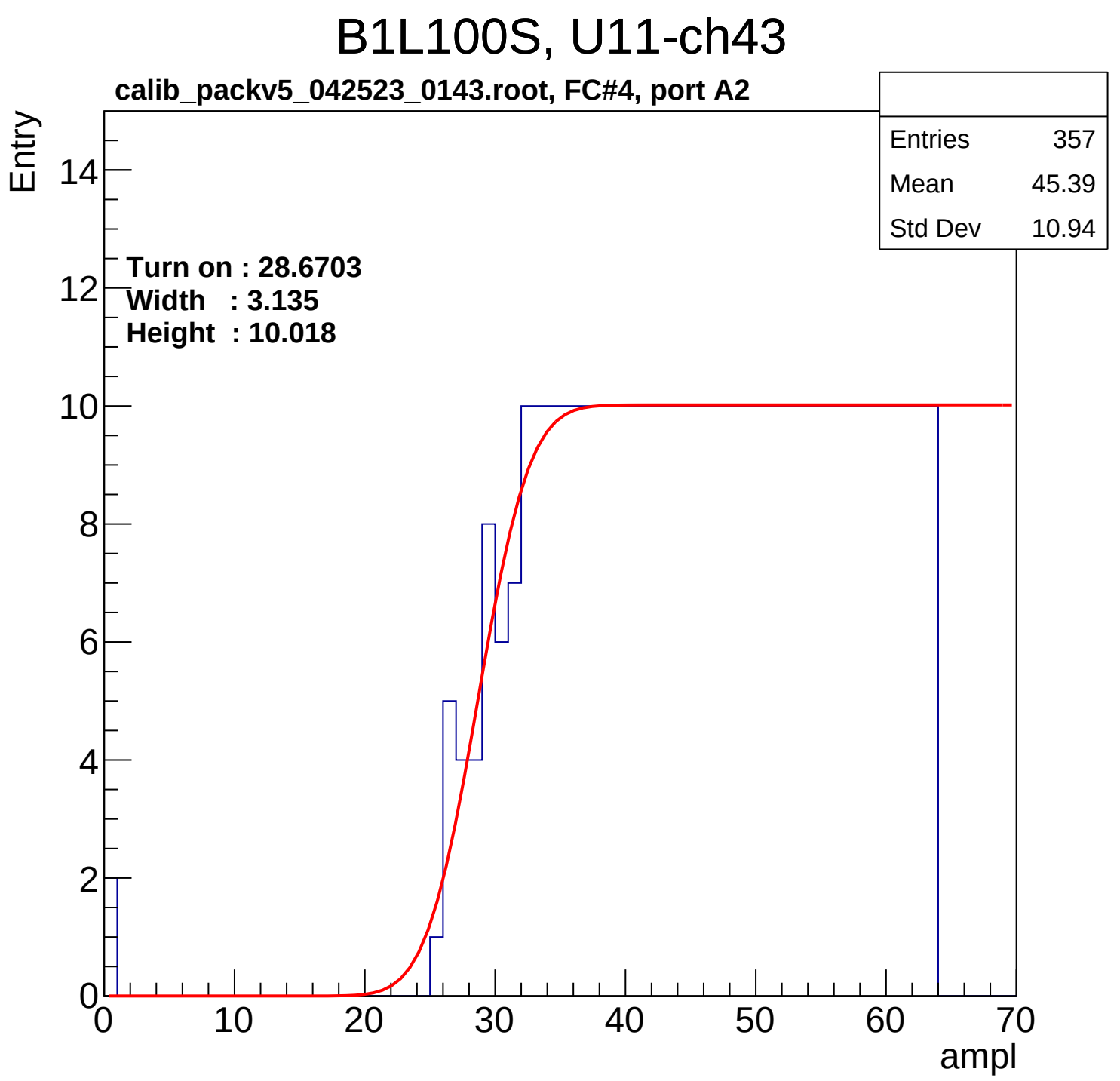
B1L100S, U11-ch43
calib_packv5_042523_0143.root, FC#4, port A2
Entries 357
Mean 45.39
Std Dev 10.94
Turn on : 28.6703
Width : 3.135
Height : 10.018
Entry
ampl
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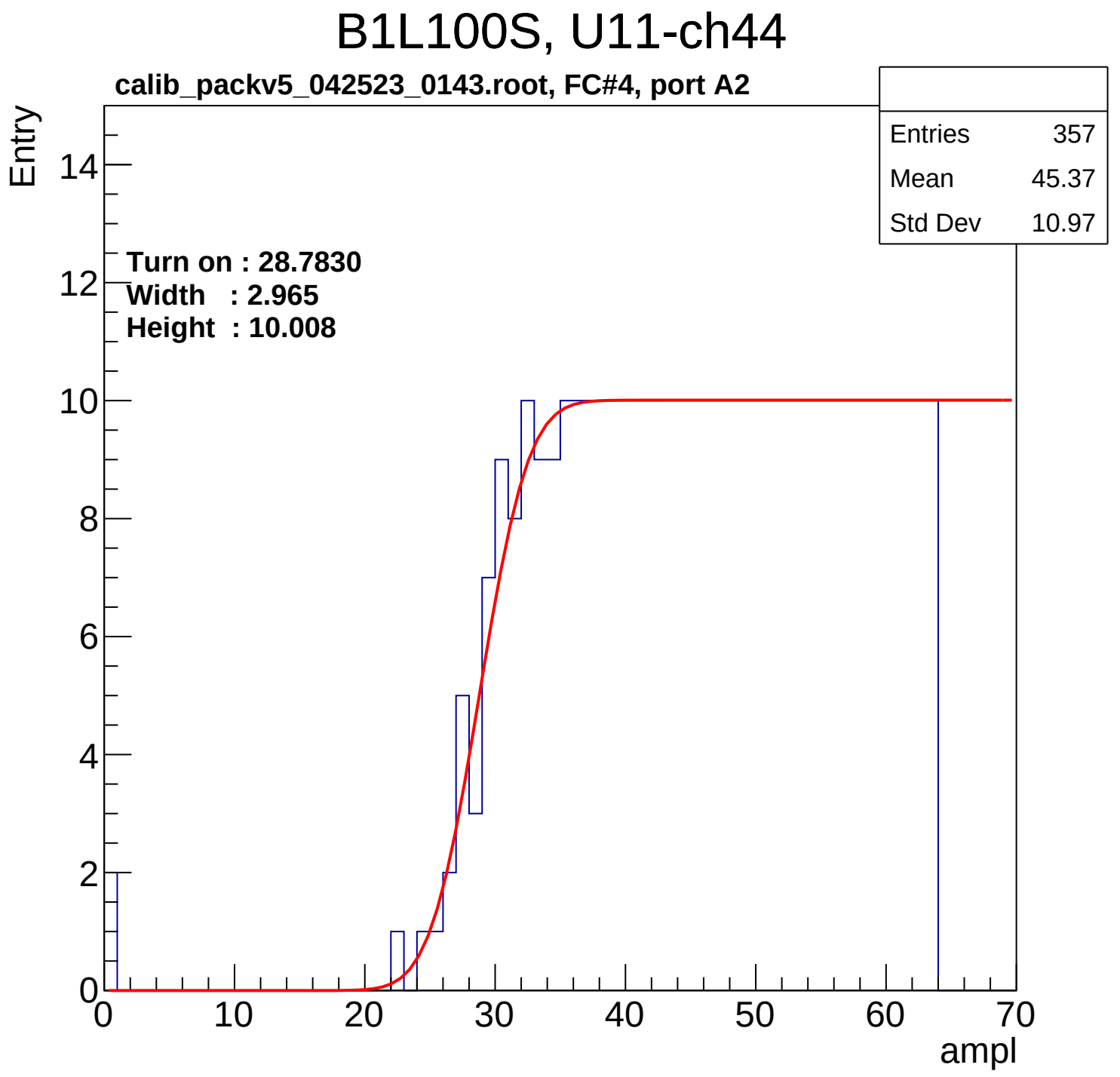
B1L100S, U11-ch44
calib_packv5_042523_0143.root, FC#4, port A2
Entries 357
Mean 45.37
Std Dev 10.97
Turn on : 28.7830
Width : 2.965
Height : 10.008
Entry
ampl
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0
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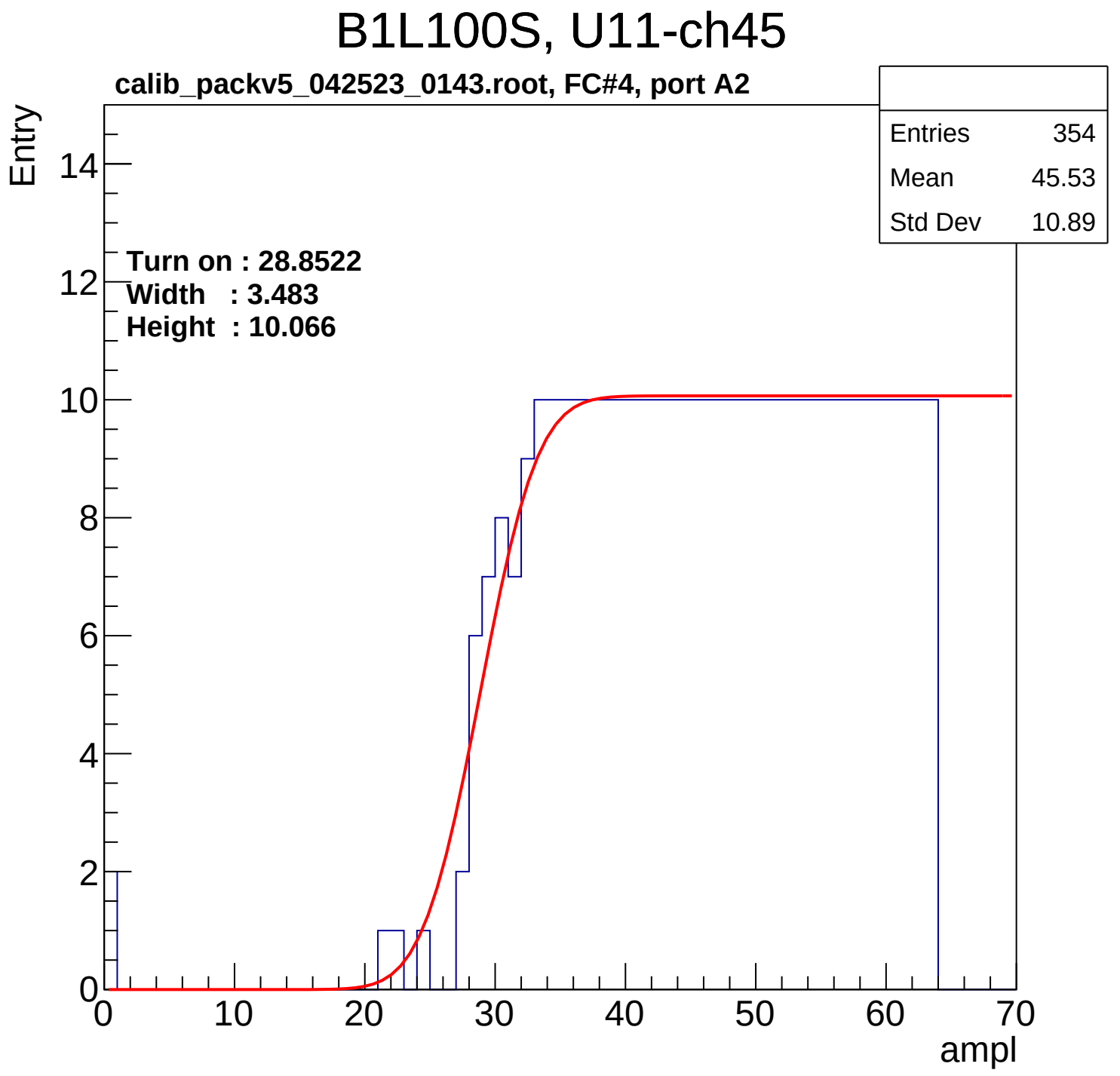
B1L100S, U11-ch45
calib_packv5_042523_0143.root, FC#4, port A2
Entries 354
Mean 45.53
Std Dev 10.89
Turn on : 28.8522
Width : 3.483
Height : 10.066
Entry
ampl
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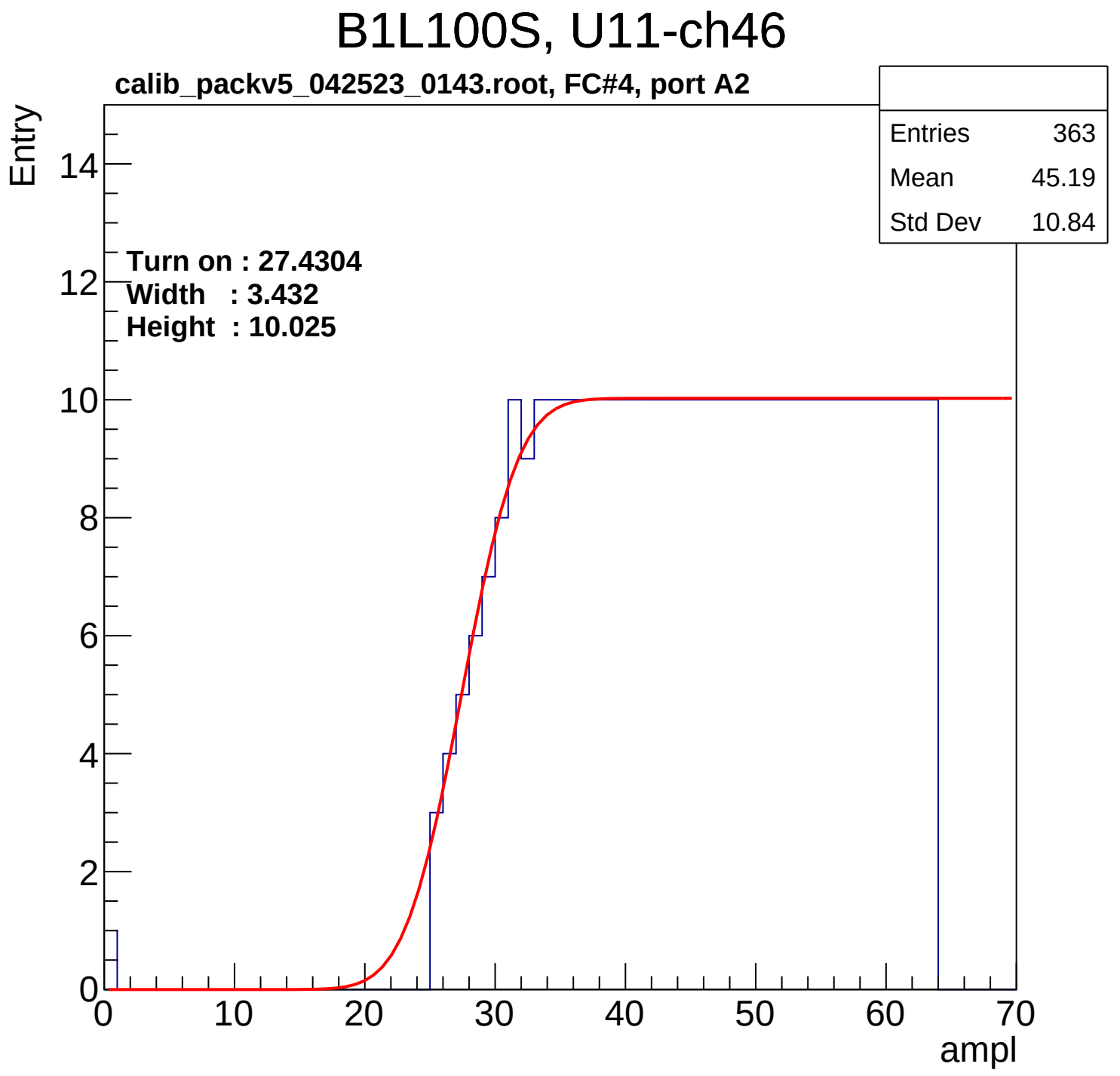
B1L100S, U11-ch46
calib_packv5_042523_0143.root, FC#4, port A2
Entries 363
Mean 45.19
Std Dev 10.84
Turn on : 27.4304
Width : 3.432
Height : 10.025
Entry
ampl
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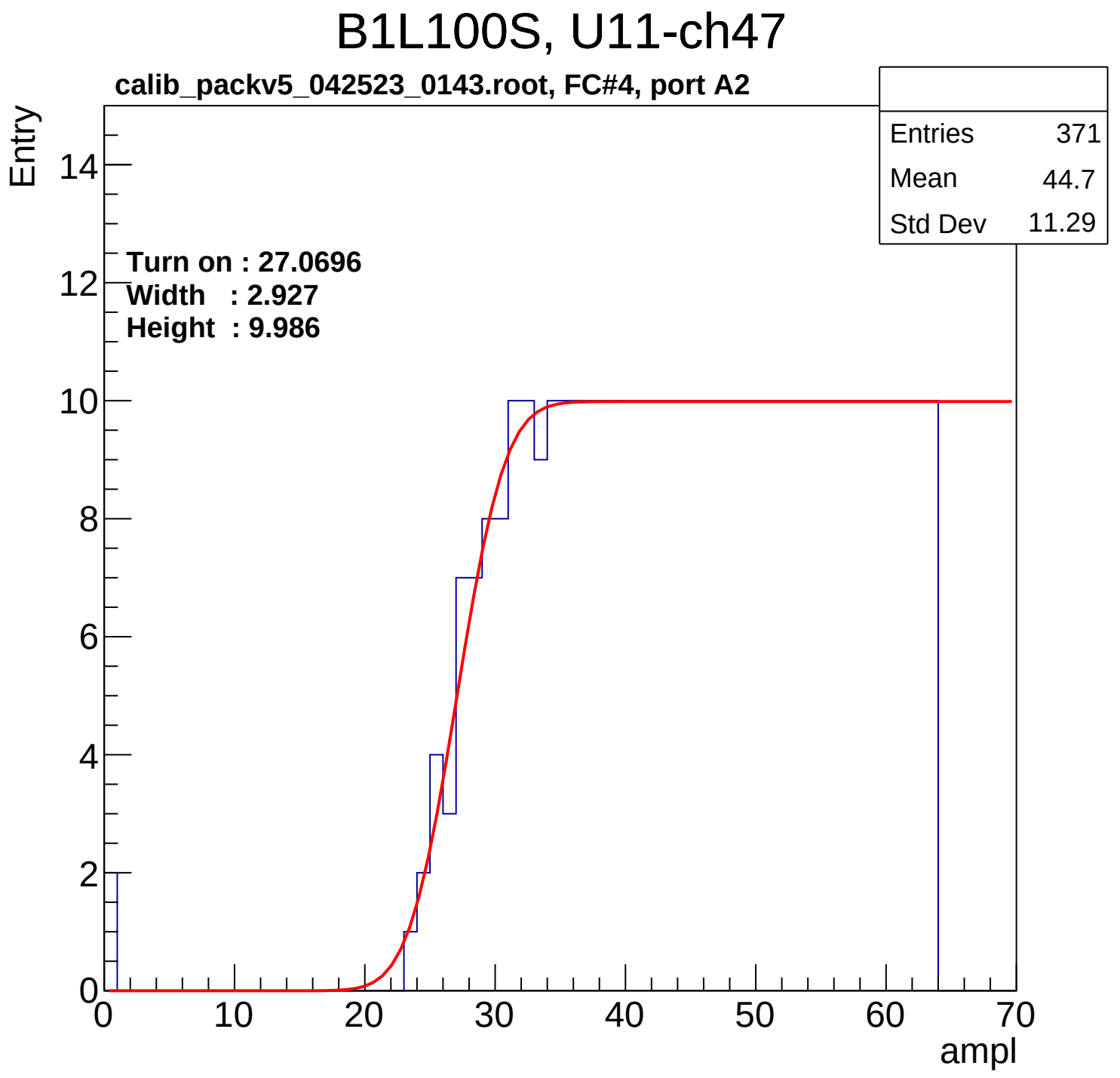
B1L100S, U11-ch47
calib_packv5_042523_0143.root, FC#4, port A2
Entries 371
Mean 44.7
Std Dev 11.29
Turn on : 27.0696
Width : 2.927
Height : 9.986
Entry
ampl
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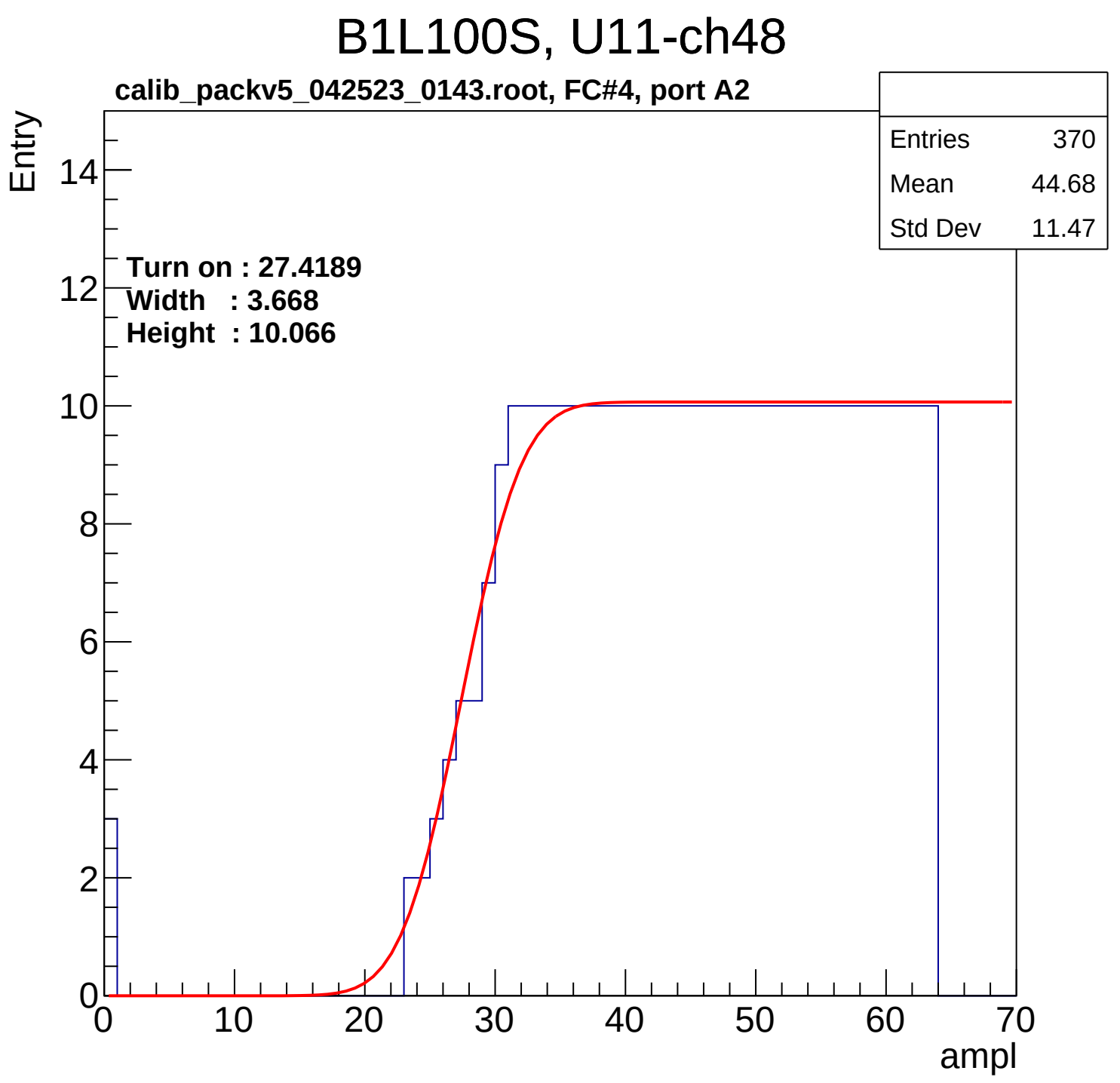
B1L100S, U11-ch48
calib_packv5_042523_0143.root, FC#4, port A2
Entries 370
Mean 44.68
Std Dev 11.47
Turn on : 27.4189
Width : 3.668
Height : 10.066
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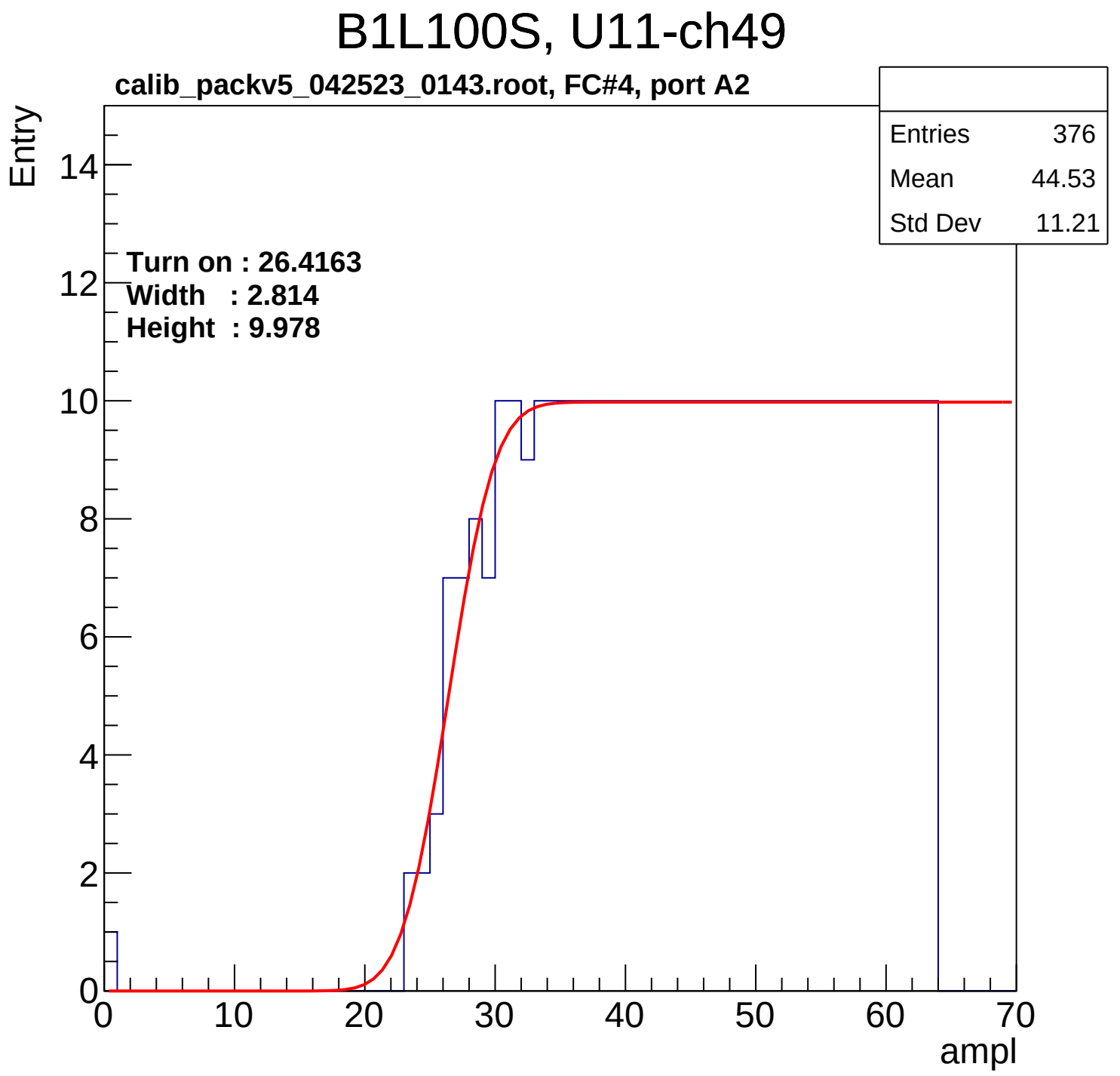
B1L100S, U11-ch49
calib_packv5_042523_0143.root, FC#4, port A2
Entries 376
Mean 44.53
Std Dev 11.21
Turn on : 26.4163
Width : 2.814
Height : 9.978
Entry
ampl
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2
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6
8
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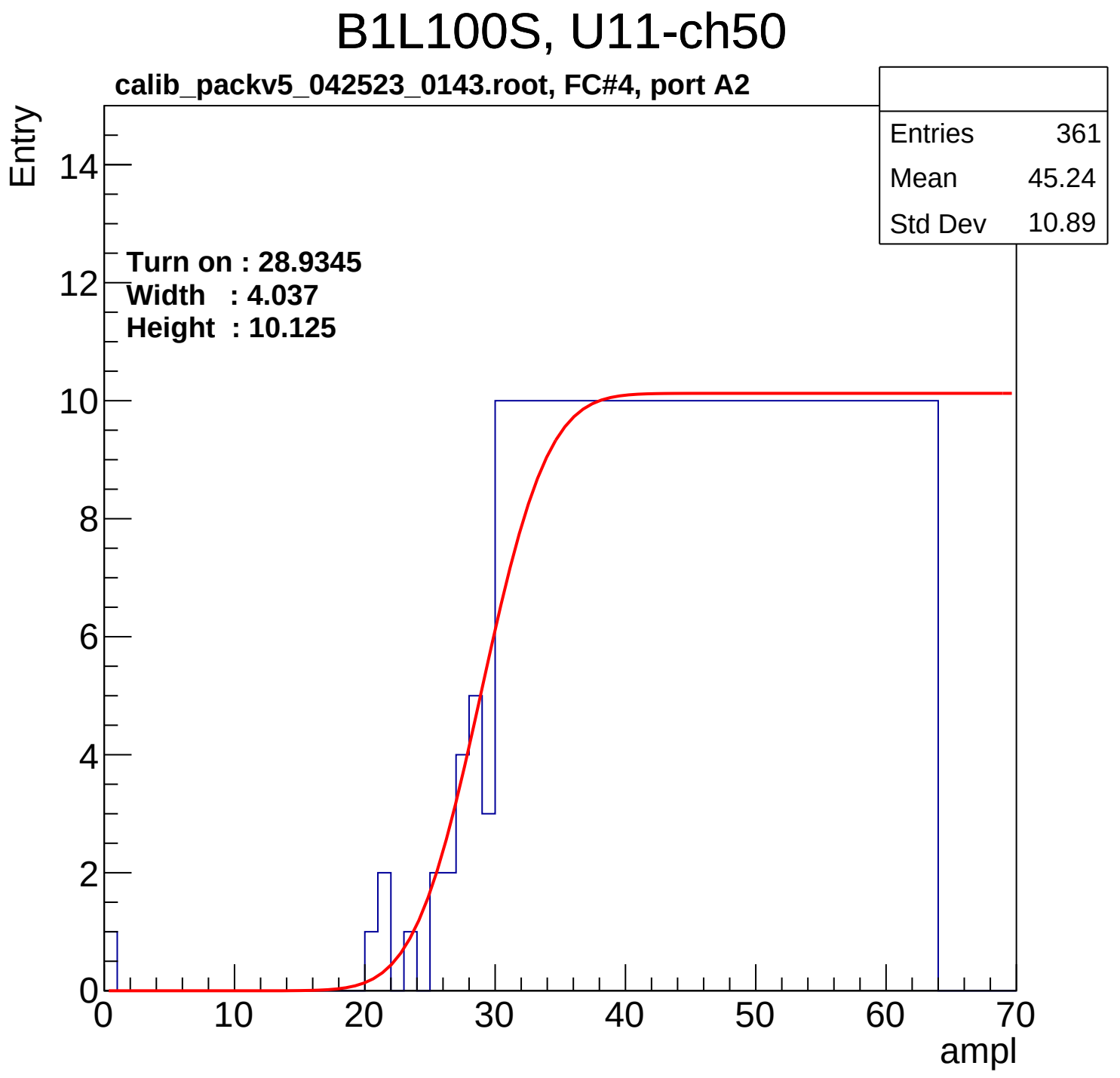
B1L100S, U11-ch50
calib_packv5_042523_0143.root, FC#4, port A2
Entries 361
Mean 45.24
Std Dev 10.89
Turn on : 28.9345
Width : 4.037
Height : 10.125
Entry
ampl
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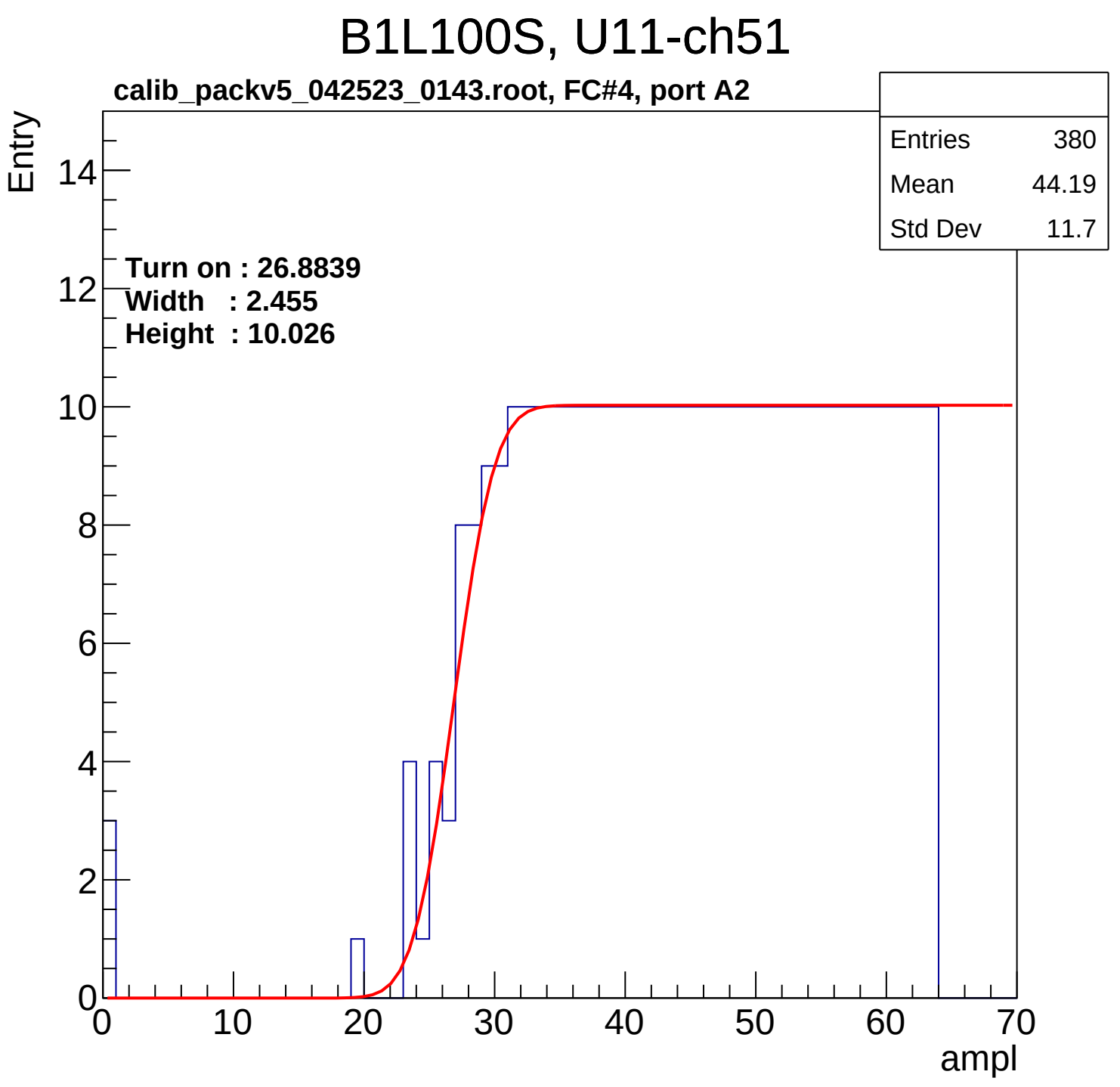
B1L100S, U11-ch51
calib_packv5_042523_0143.root, FC#4, port A2
Entries 380
Mean 44.19
Std Dev 11.7
Turn on : 26.8839
Width : 2.455
Height : 10.026
Entry
ampl
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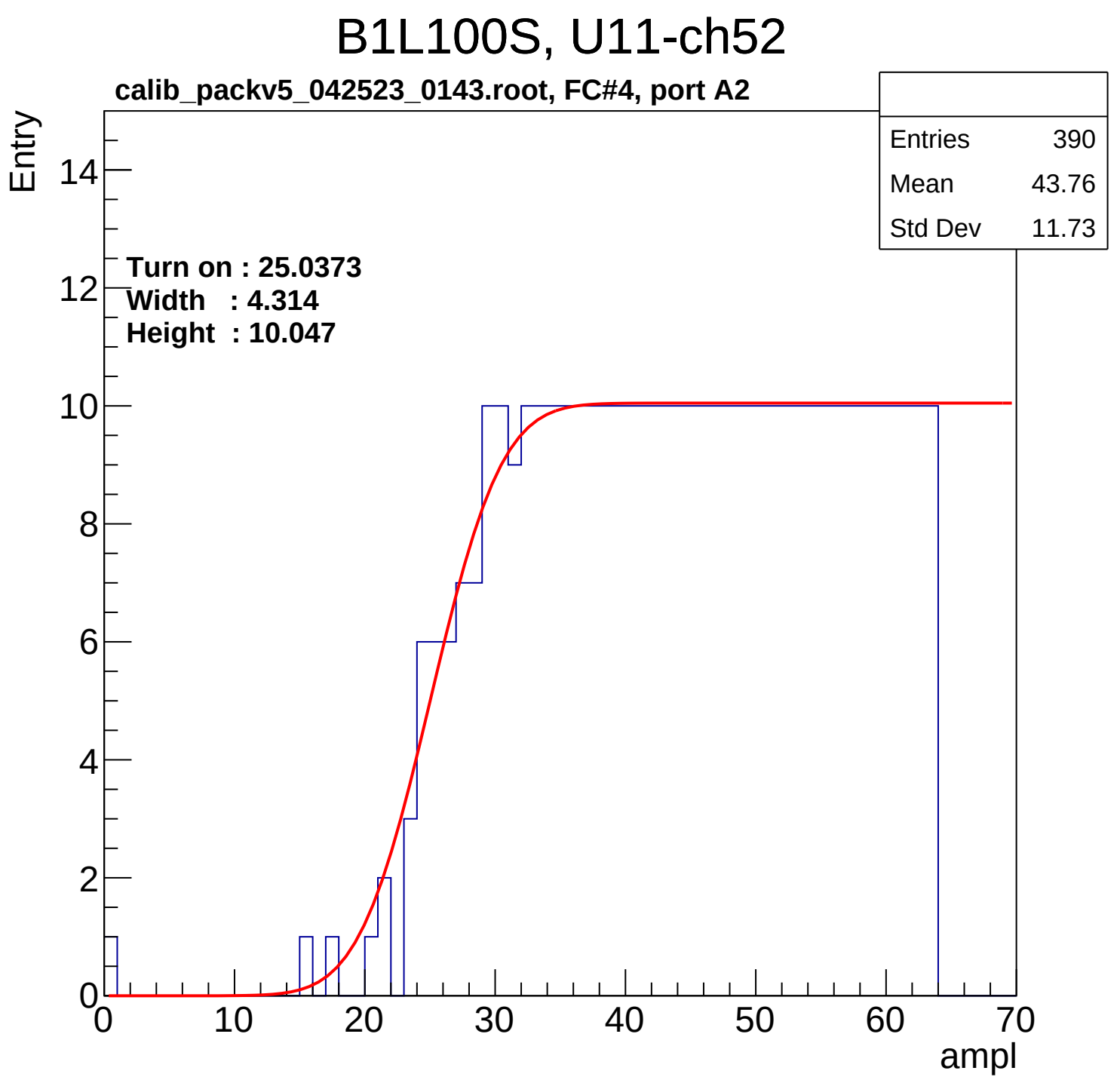
B1L100S, U11-ch52
calib_packv5_042523_0143.root, FC#4, port A2
Entries 390
Mean 43.76
Std Dev 11.73
Turn on : 25.0373
Width : 4.314
Height : 10.047
Entry
ampl
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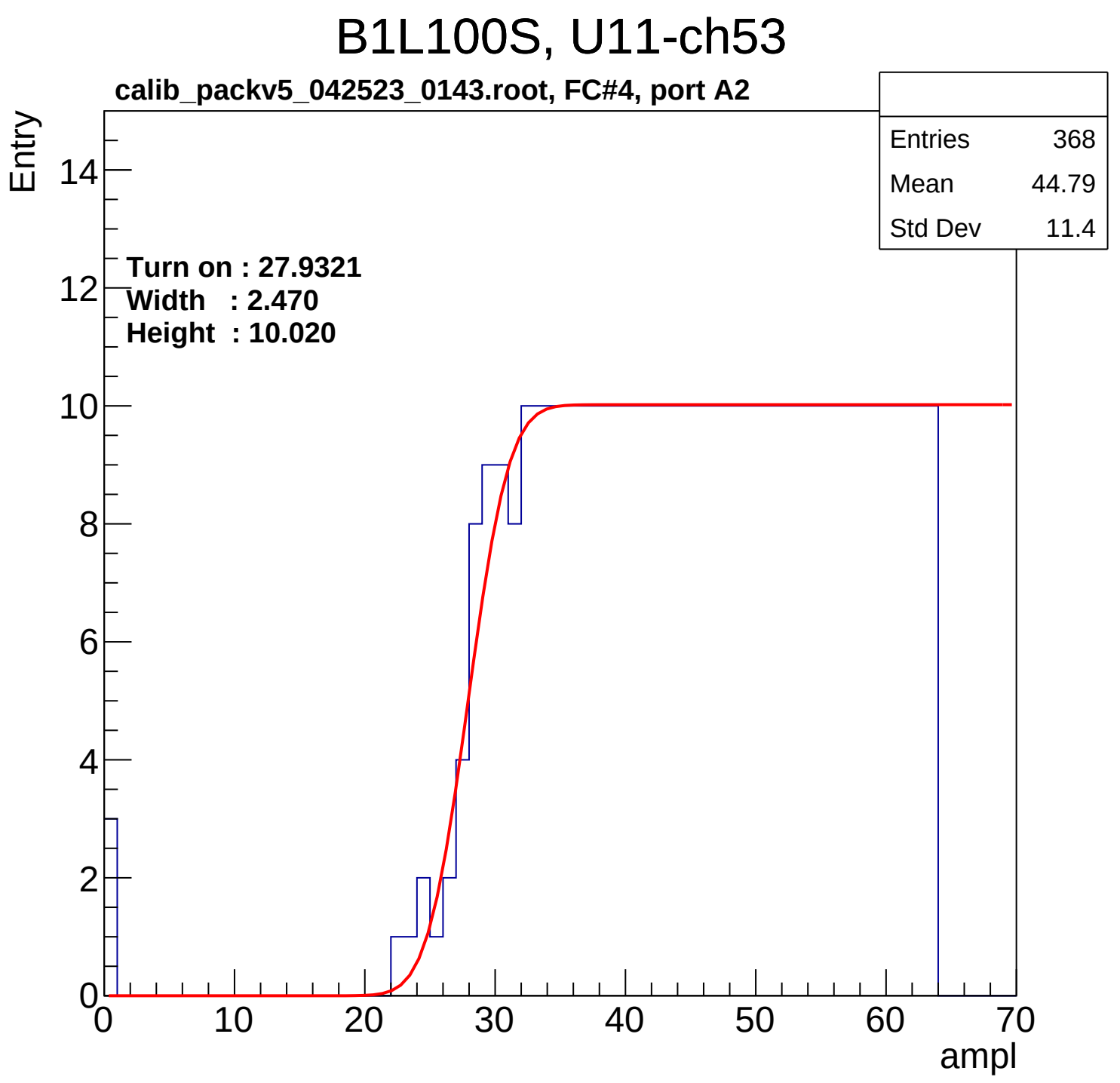
B1L100S, U11-ch53
calib_packv5_042523_0143.root, FC#4, port A2
Entries 368
Mean 44.79
Std Dev 11.4
Turn on : 27.9321
Width : 2.470
Height : 10.020
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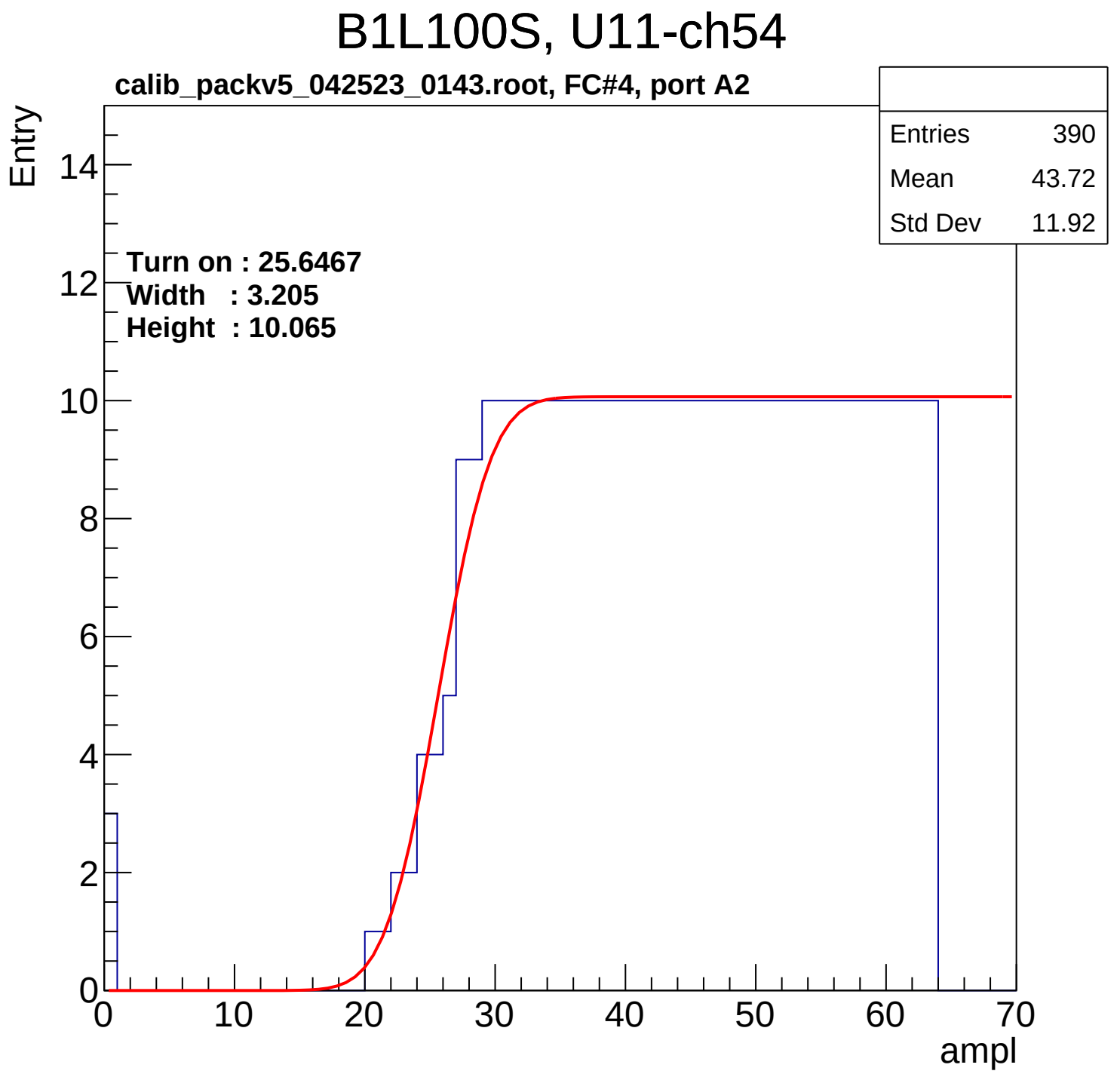
B1L100S, U11-ch54
calib_packv5_042523_0143.root, FC#4, port A2
Entries 390
Mean 43.72
Std Dev 11.92
Turn on : 25.6467
Width : 3.205
Height : 10.065
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ampl
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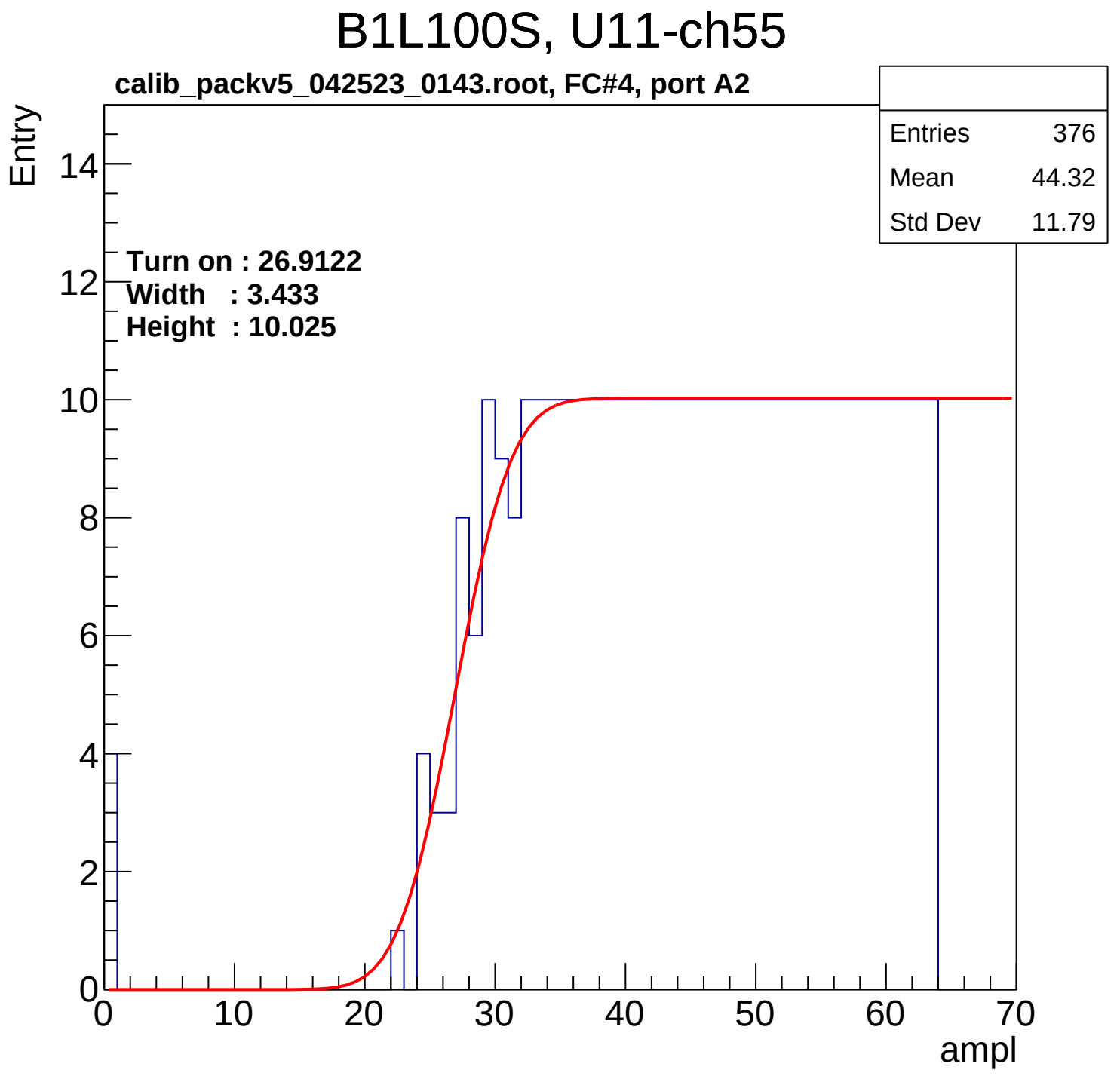
B1L100S, U11-ch55
calib_packv5_042523_0143.root, FC#4, port A2
Entries 376
Mean 44.32
Std Dev 11.79
Turn on : 26.9122
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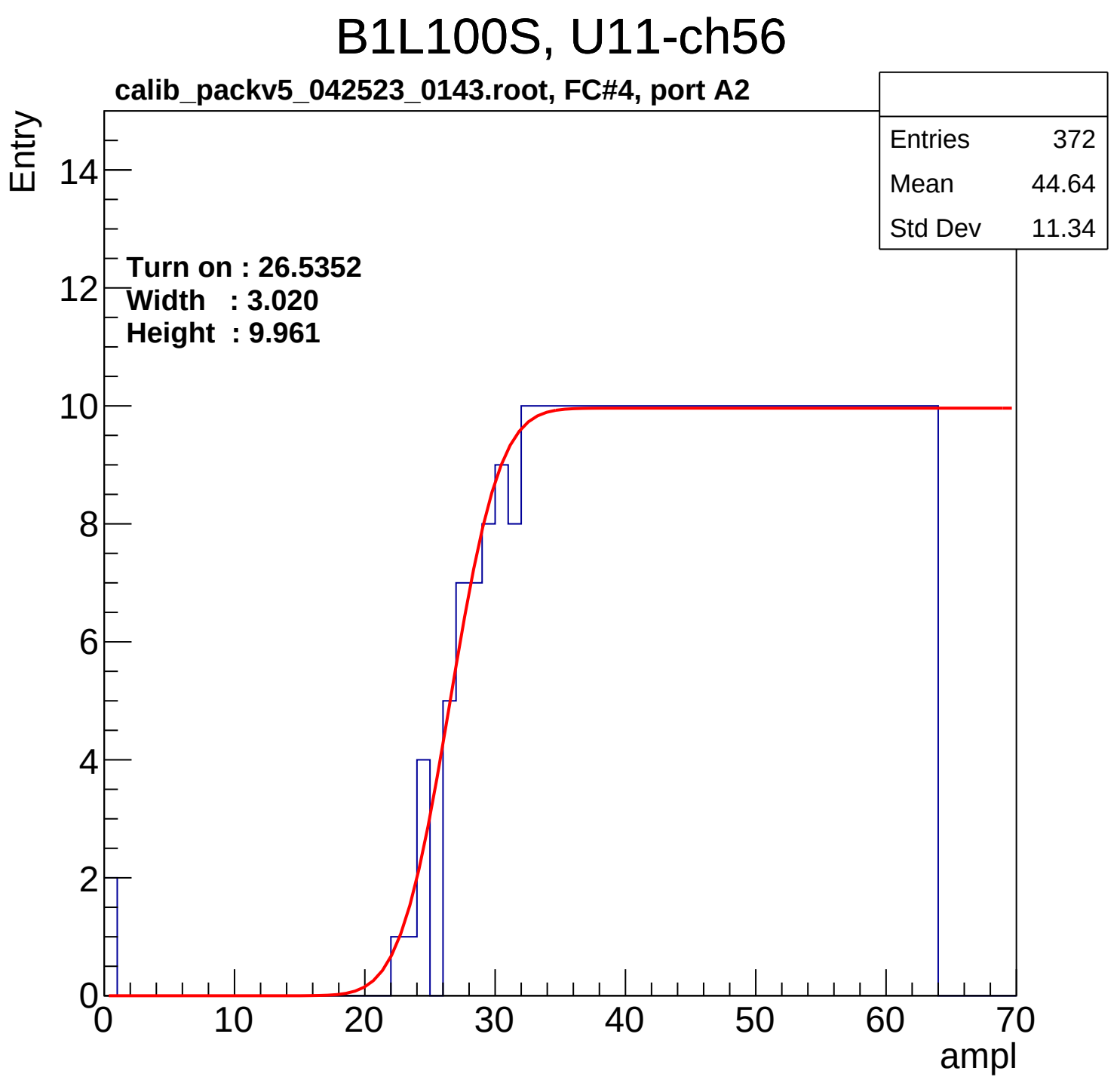
B1L100S, U11-ch56
calib_packv5_042523_0143.root, FC#4, port A2
Entries 372
Mean 44.64
Std Dev 11.34
Turn on : 26.5352
Width : 3.020
Height : 9.961
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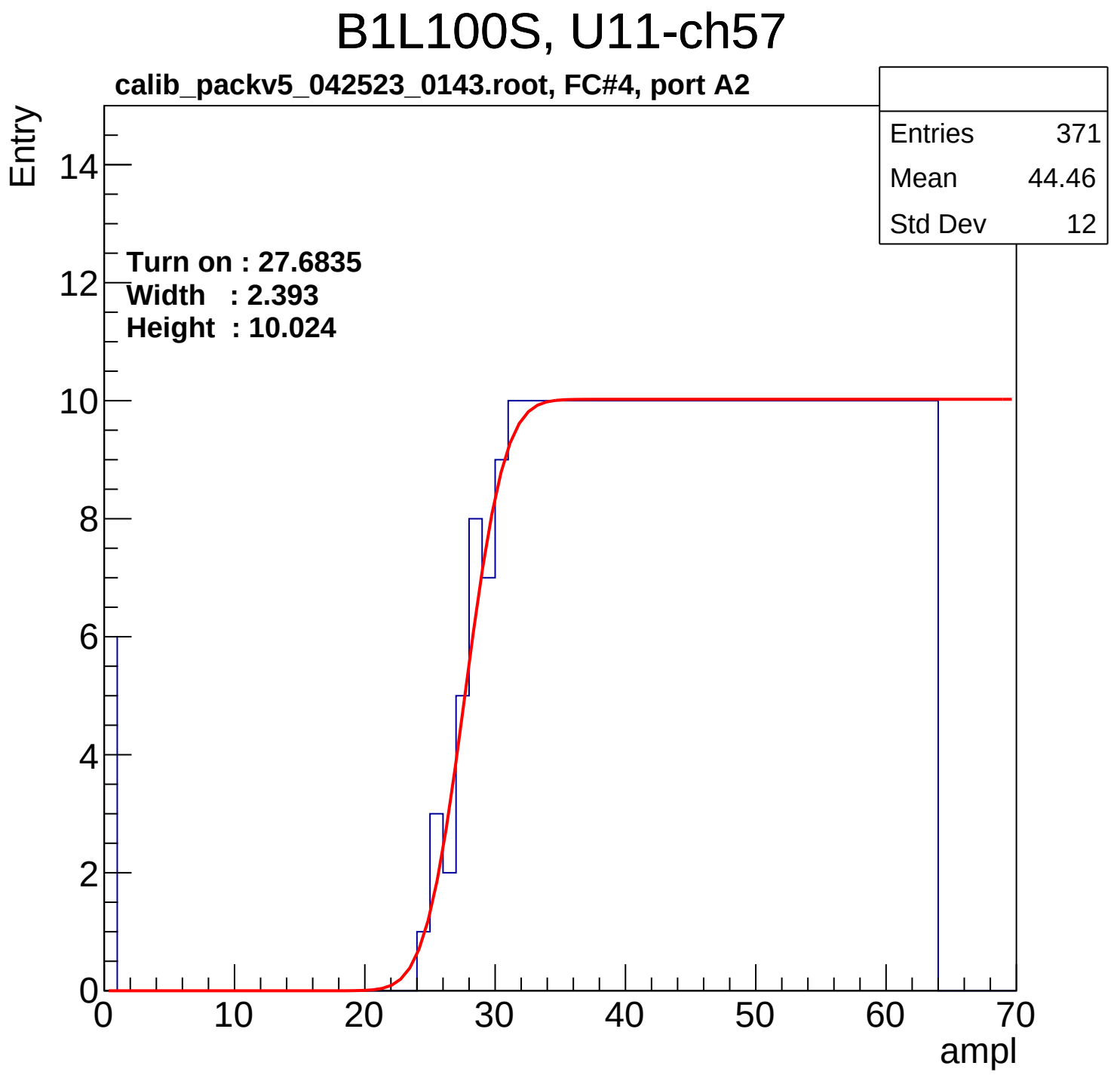
B1L100S, U11-ch57
calib_packv5_042523_0143.root, FC#4, port A2
Entries 371
Mean 44.46
Std Dev 12
Turn on : 27.6835
Width : 2.393
Height : 10.024
Entry
ampl
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6
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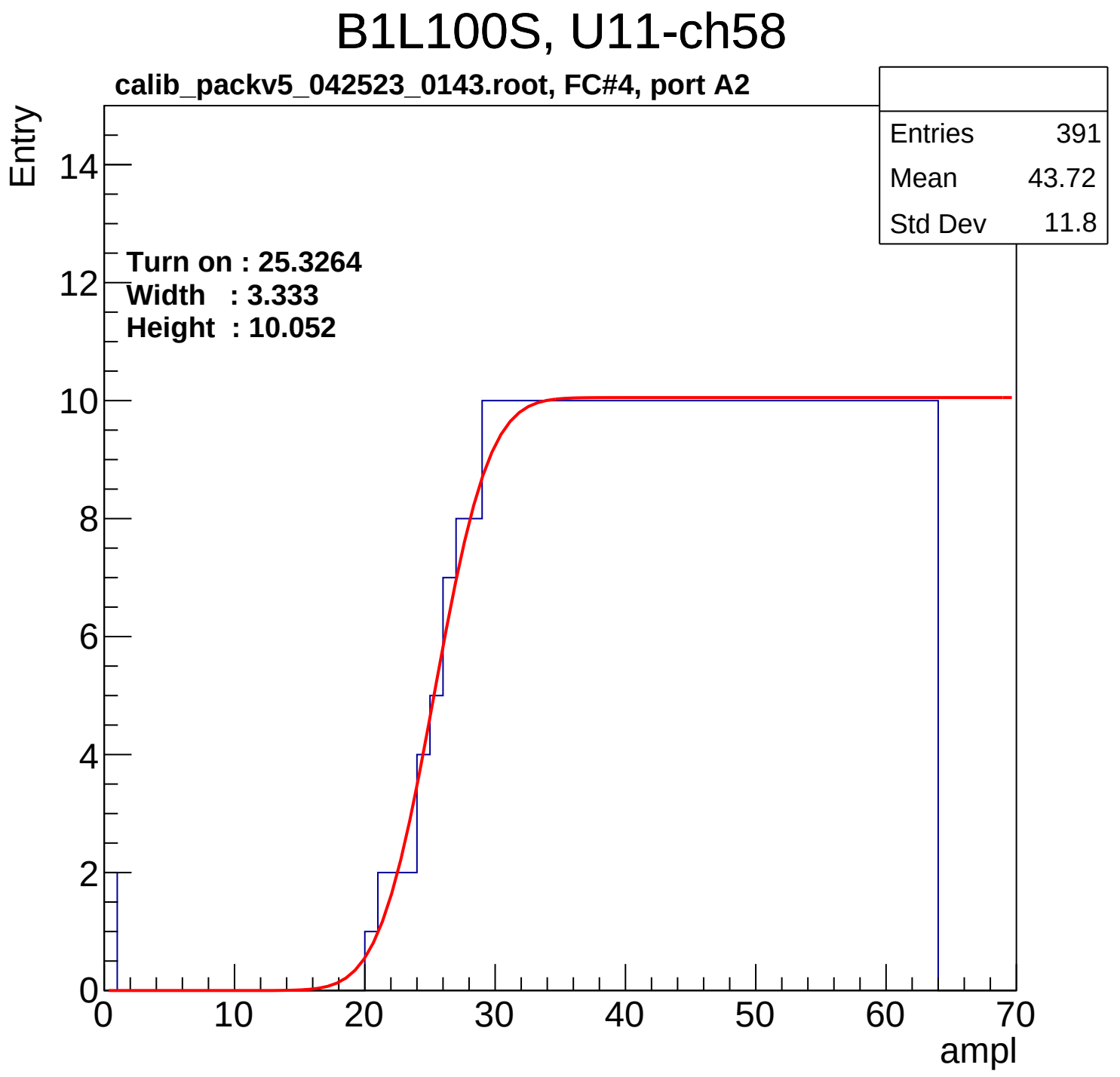
B1L100S, U11-ch58
calib_packv5_042523_0143.root, FC#4, port A2
Entries 391
Mean 43.72
Std Dev 11.8
Turn on : 25.3264
Width : 3.333
Height : 10.052
Entry
ampl
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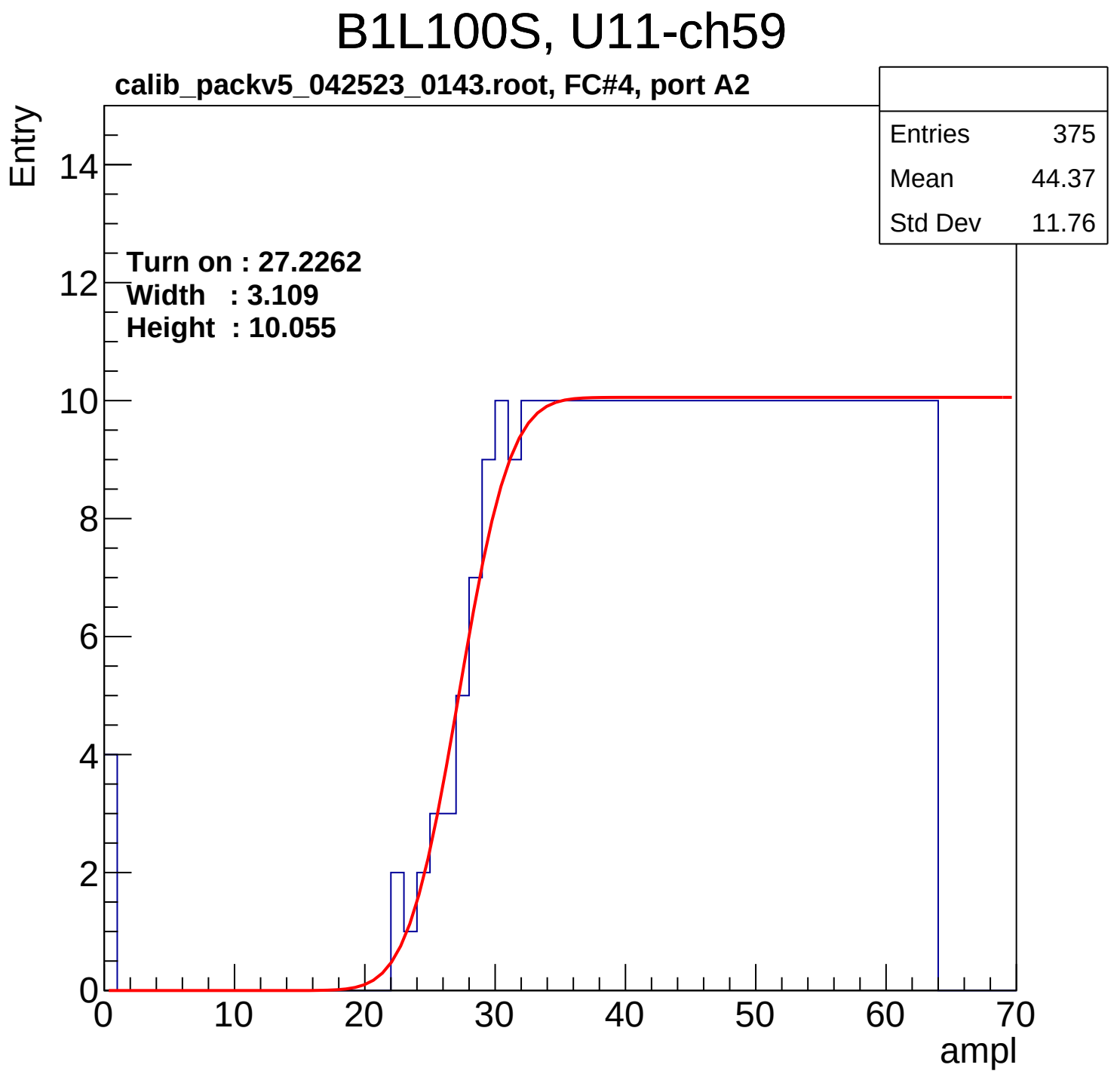
B1L100S, U11-ch59
calib_packv5_042523_0143.root, FC#4, port A2
Entries 375
Mean 44.37
Std Dev 11.76
Turn on : 27.2262
Width : 3.109
Height : 10.055
Entry
ampl
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2
4
6
8
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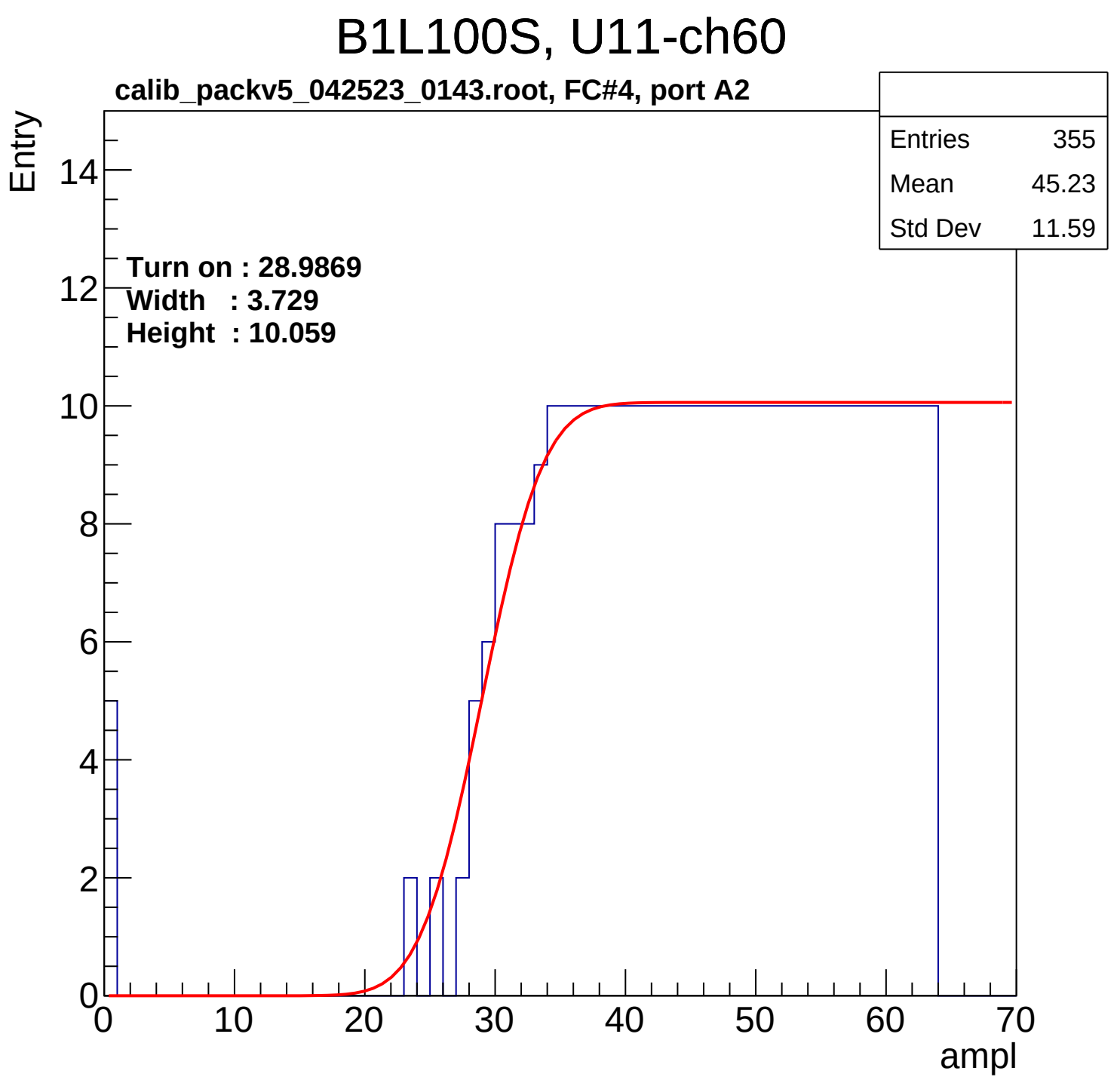
B1L100S, U11-ch60
calib_packv5_042523_0143.root, FC#4, port A2
Entries 355
Mean 45.23
Std Dev 11.59
Turn on : 28.9869
Width : 3.729
Height : 10.059
Entry
ampl
0
2
4
6
8
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0
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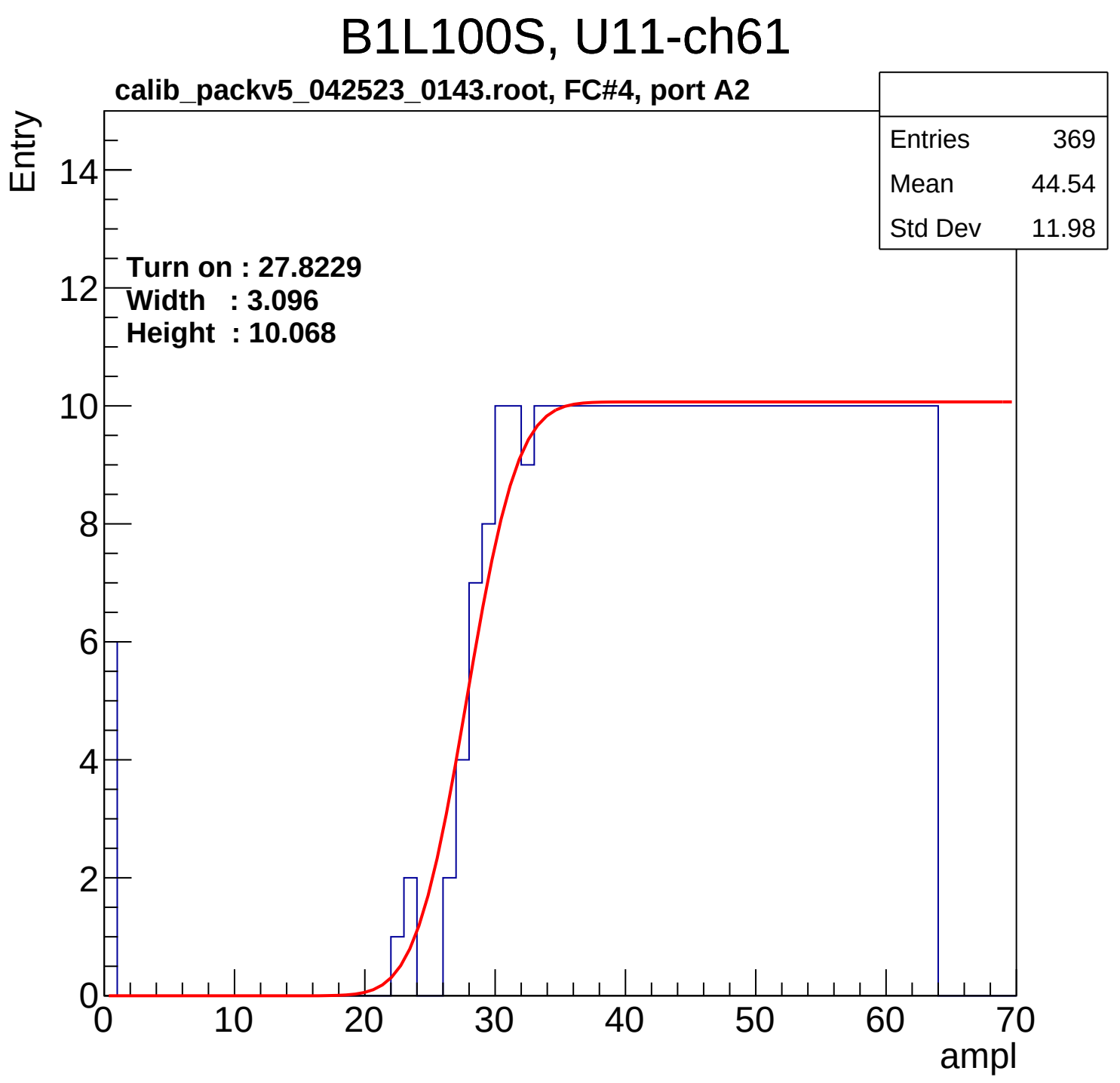
B1L100S, U11-ch61
calib_packv5_042523_0143.root, FC#4, port A2
Entries 369
Mean 44.54
Std Dev 11.98
Turn on : 27.8229
Width : 3.096
Height : 10.068
Entry
ampl
0
2
4
6
8
10
12
14
0
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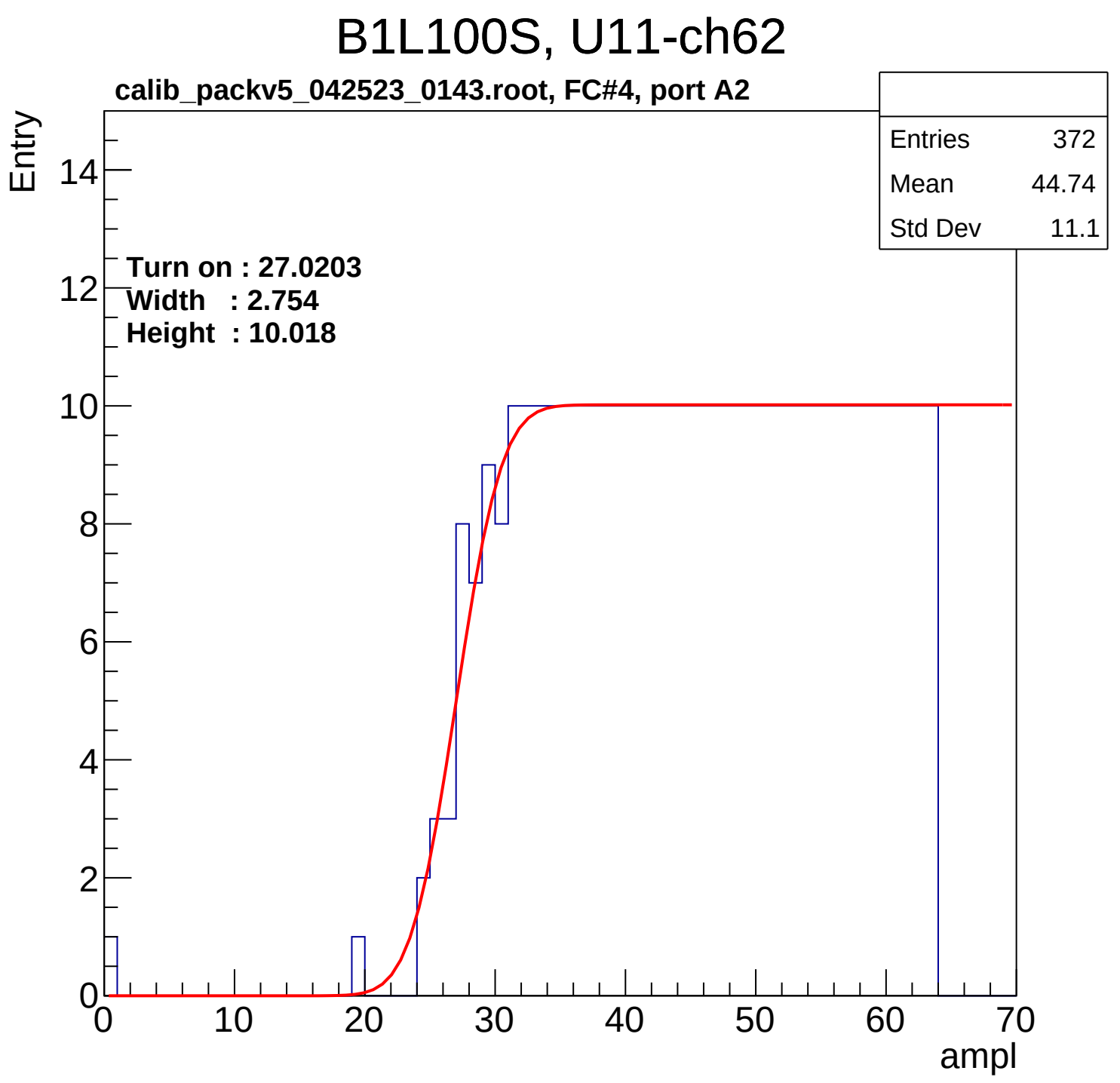
B1L100S, U11-ch62
calib_packv5_042523_0143.root, FC#4, port A2
Entries 372
Mean 44.74
Std Dev 11.1
Turn on : 27.0203
Width : 2.754
Height : 10.018
Entry
ampl
0
2
4
6
8
10
12
14
0
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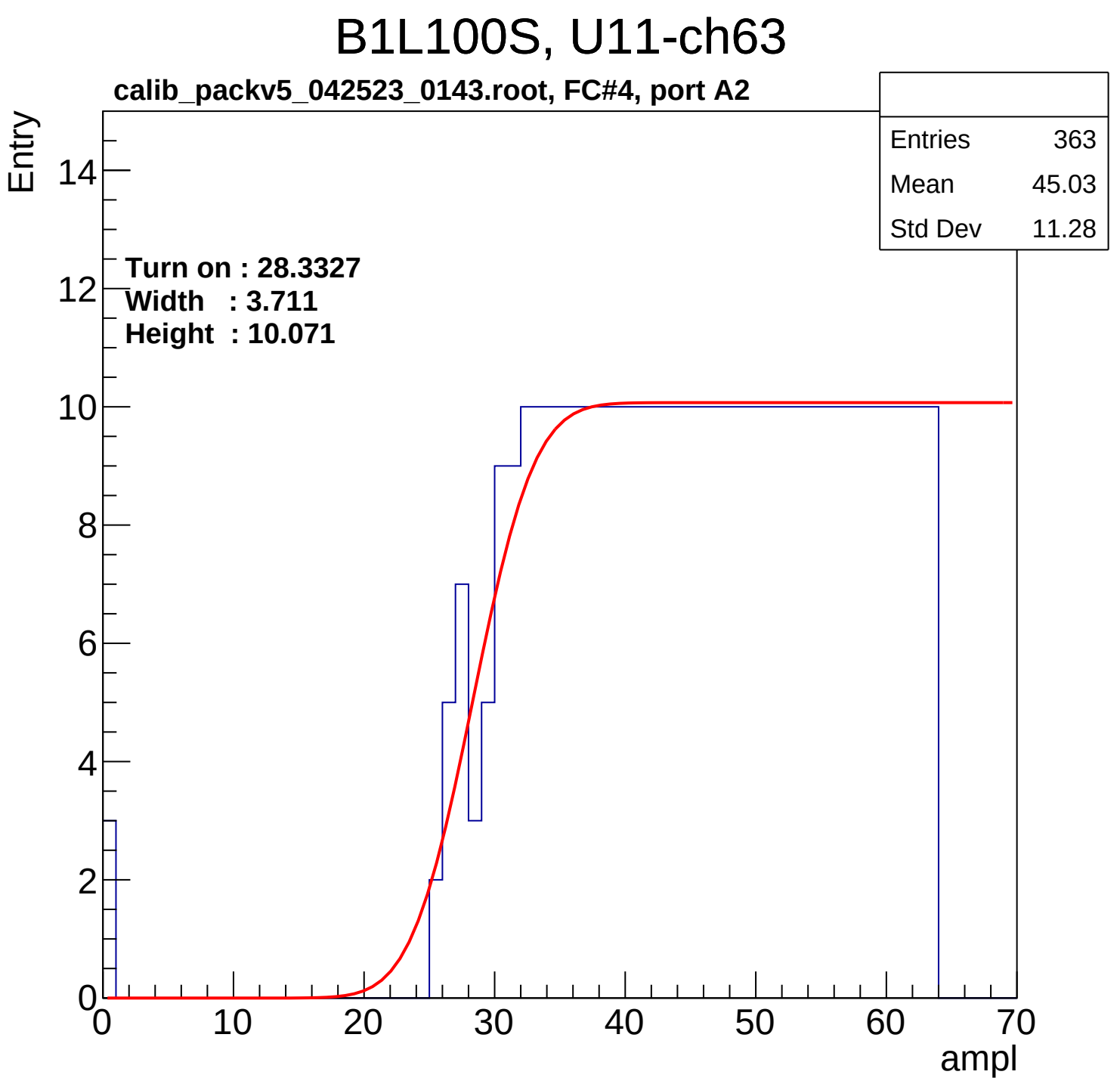
B1L100S, U11-ch63
calib_packv5_042523_0143.root, FC#4, port A2
Entries 363
Mean 45.03
Std Dev 11.28
Turn on : 28.3327
Width : 3.711
Height : 10.071
Entry
ampl
0
2
4
6
8
10
12
14
0
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60
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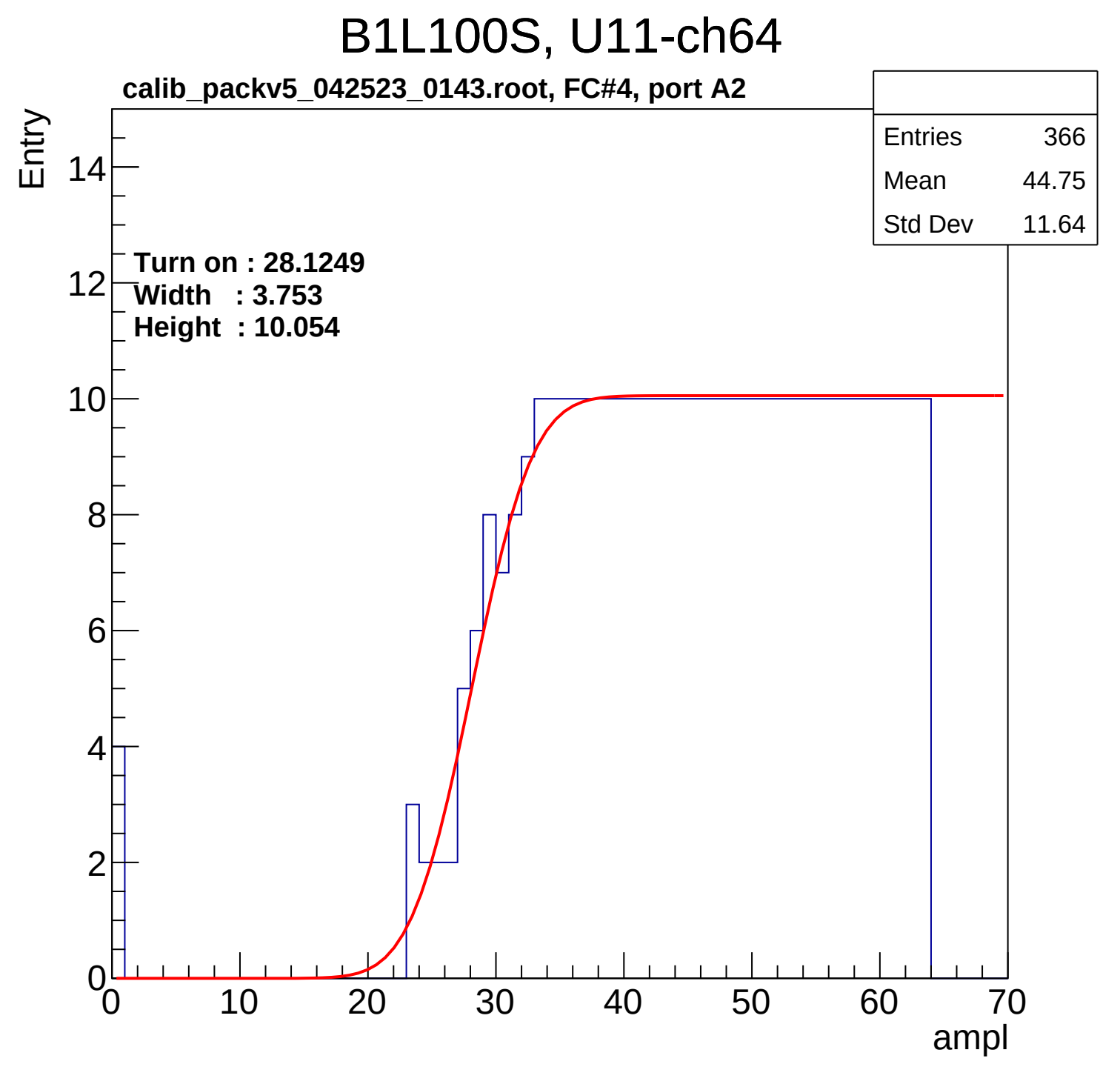
B1L100S, U11-ch64
calib_packv5_042523_0143.root, FC#4, port A2
Entries 366
Mean 44.75
Std Dev 11.64
Turn on : 28.1249
Width : 3.753
Height : 10.054
Entry
ampl
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2
4
6
8
10
12
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0
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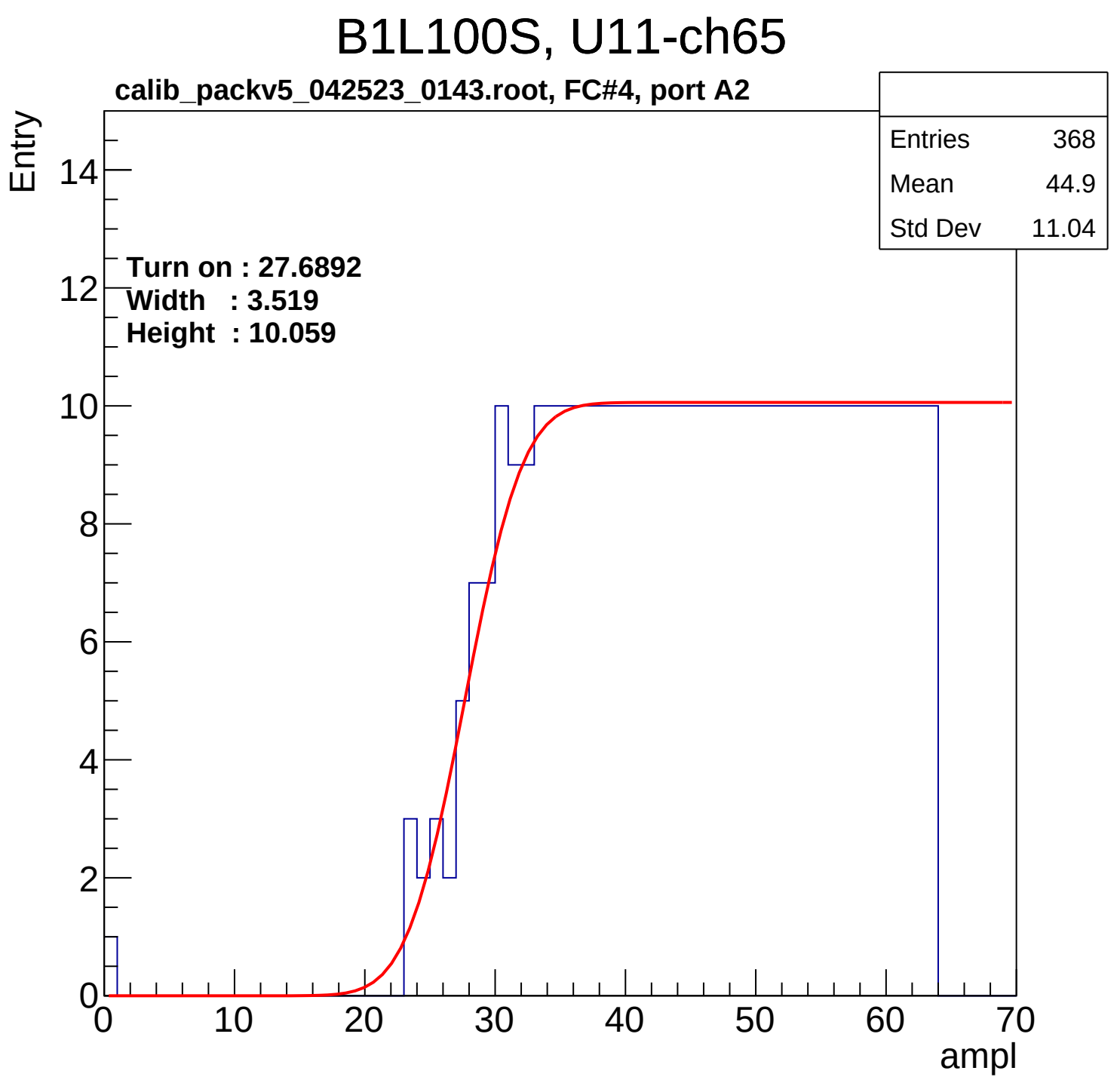
B1L100S, U11-ch65
calib_packv5_042523_0143.root, FC#4, port A2
Entries 368
Mean 44.9
Std Dev 11.04
Turn on : 27.6892
Width : 3.519
Height : 10.059
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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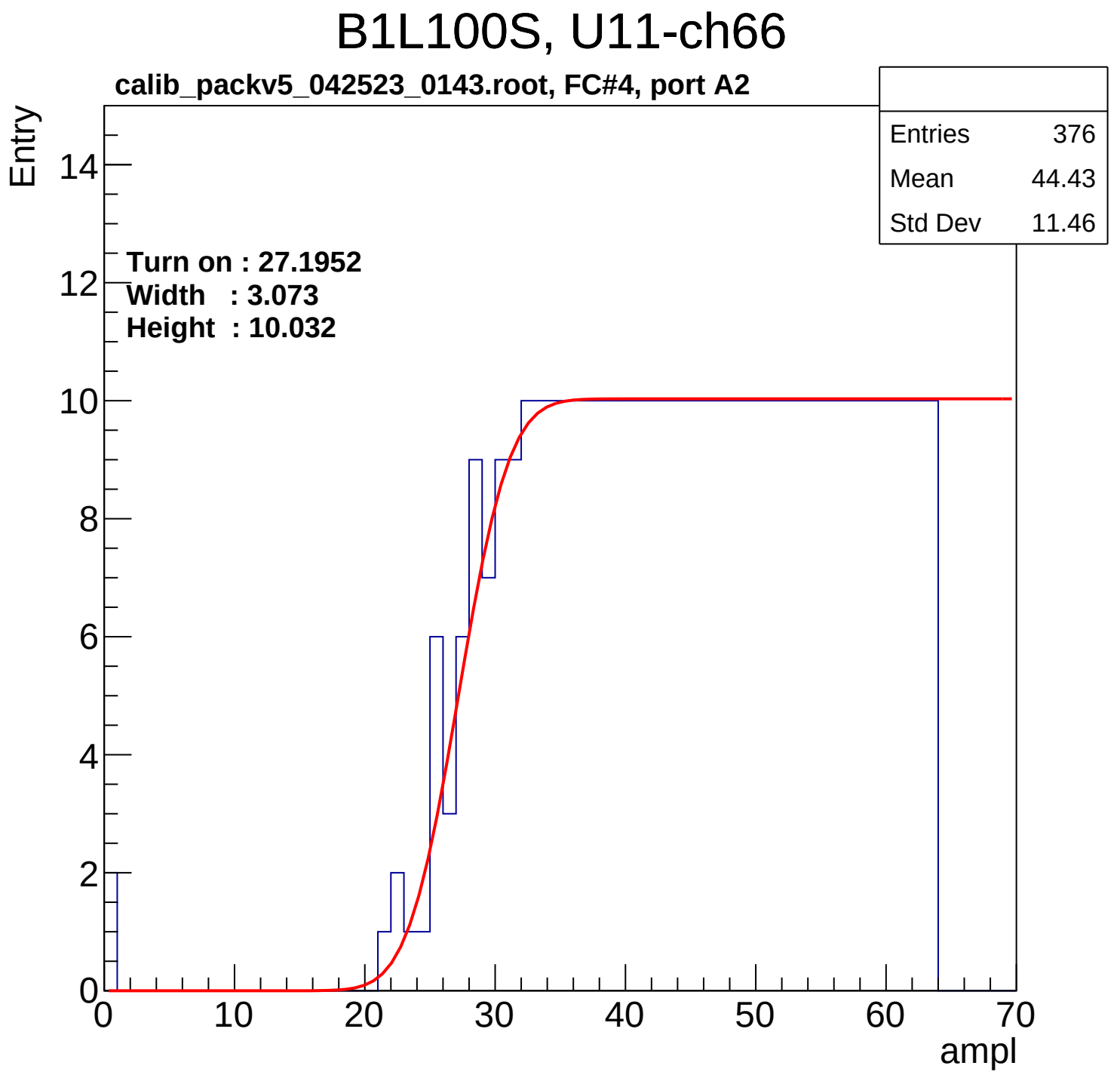
B1L100S, U11-ch66
calib_packv5_042523_0143.root, FC#4, port A2
Entries 376
Mean 44.43
Std Dev 11.46
Turn on : 27.1952
Width : 3.073
Height : 10.032
Entry
ampl
0
2
4
6
8
10
12
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0
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20
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60
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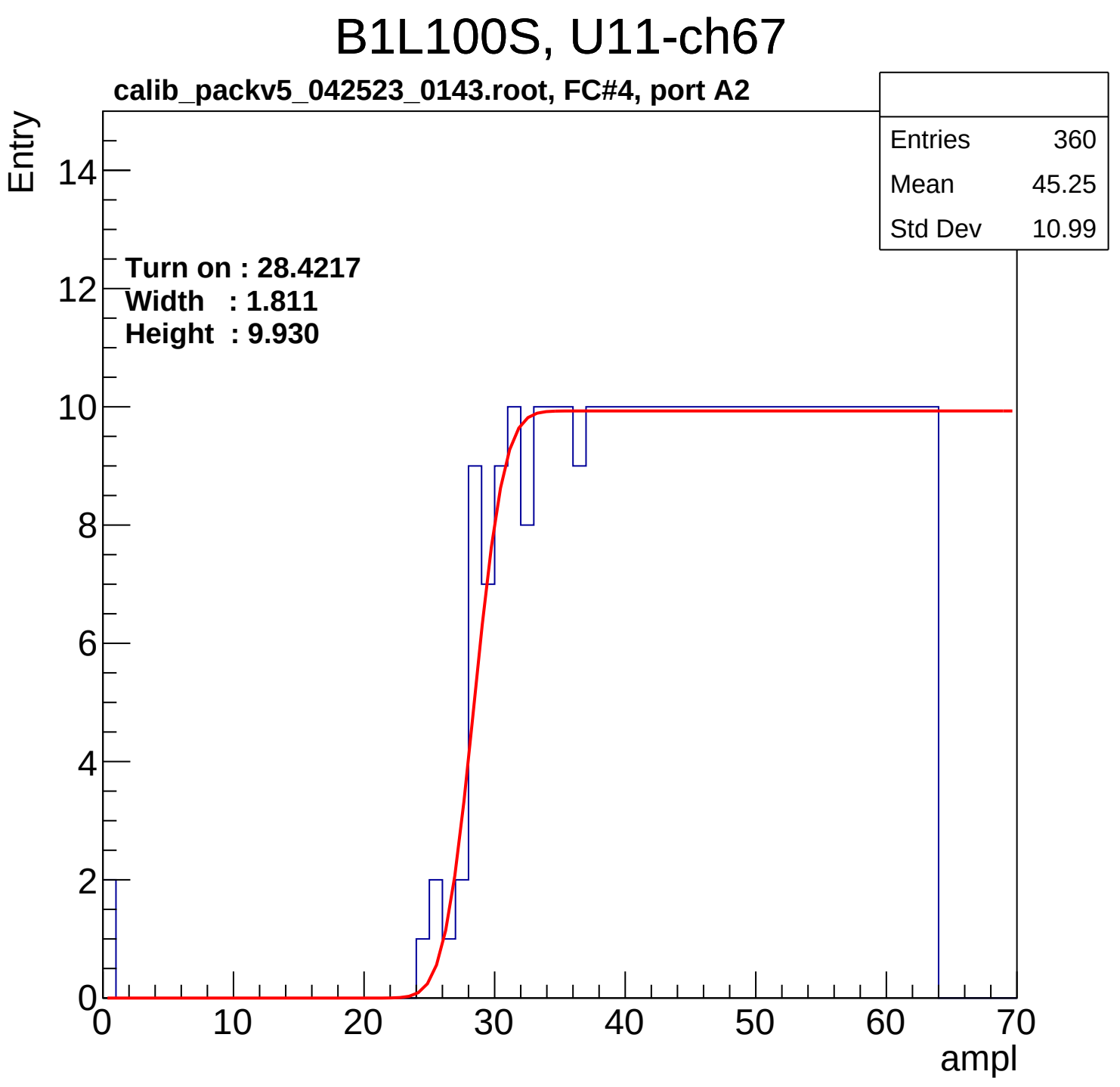
B1L100S, U11-ch67
calib_packv5_042523_0143.root, FC#4, port A2
Entries 360
Mean 45.25
Std Dev 10.99
Turn on : 28.4217
Width : 1.811
Height : 9.930
Entry
ampl
0
2
4
6
8
10
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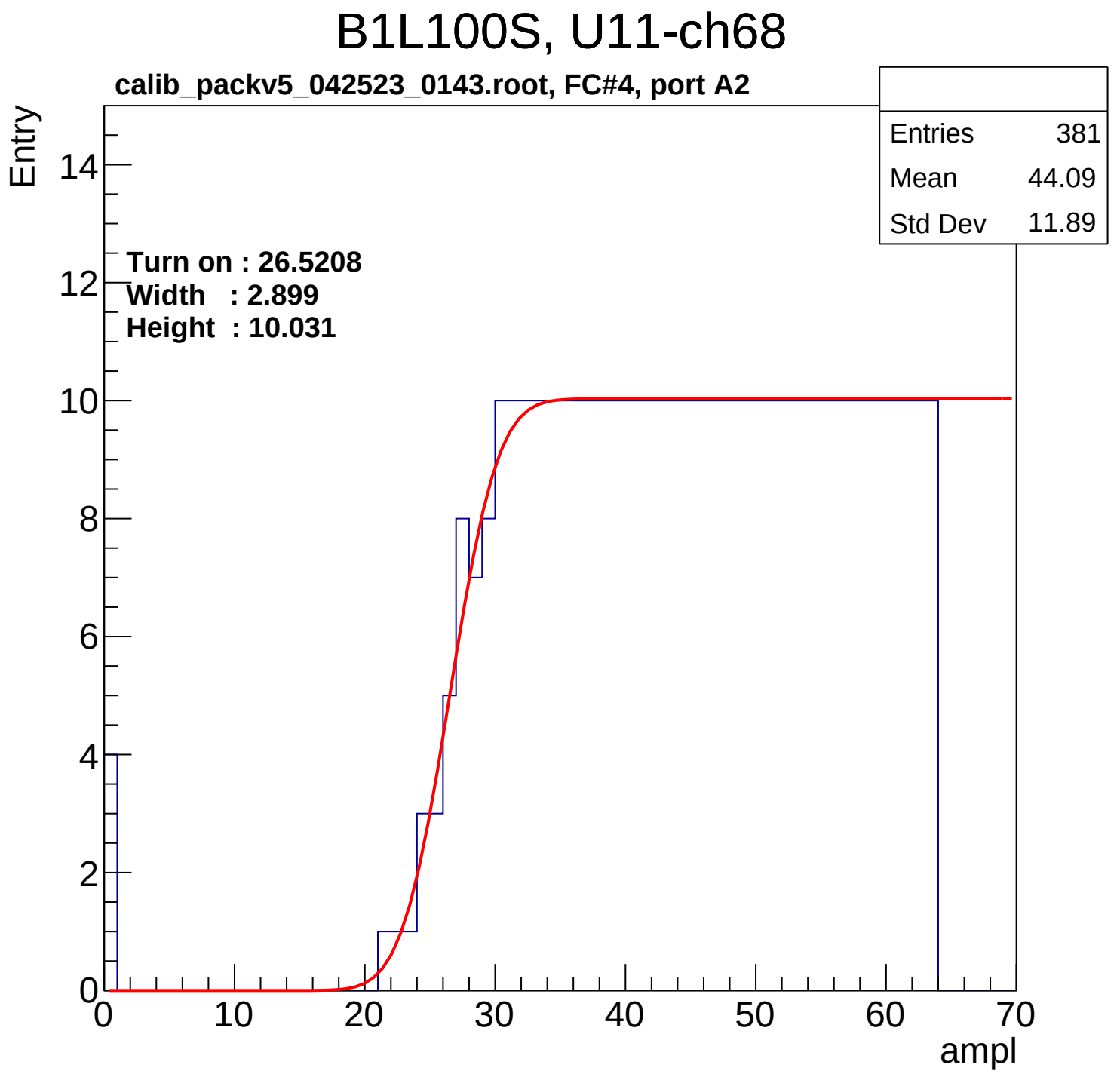
B1L100S, U11-ch68
calib_packv5_042523_0143.root, FC#4, port A2
Entries 381
Mean 44.09
Std Dev 11.89
Turn on : 26.5208
Width : 2.899
Height : 10.031
Entry
ampl
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2
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6
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12
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0
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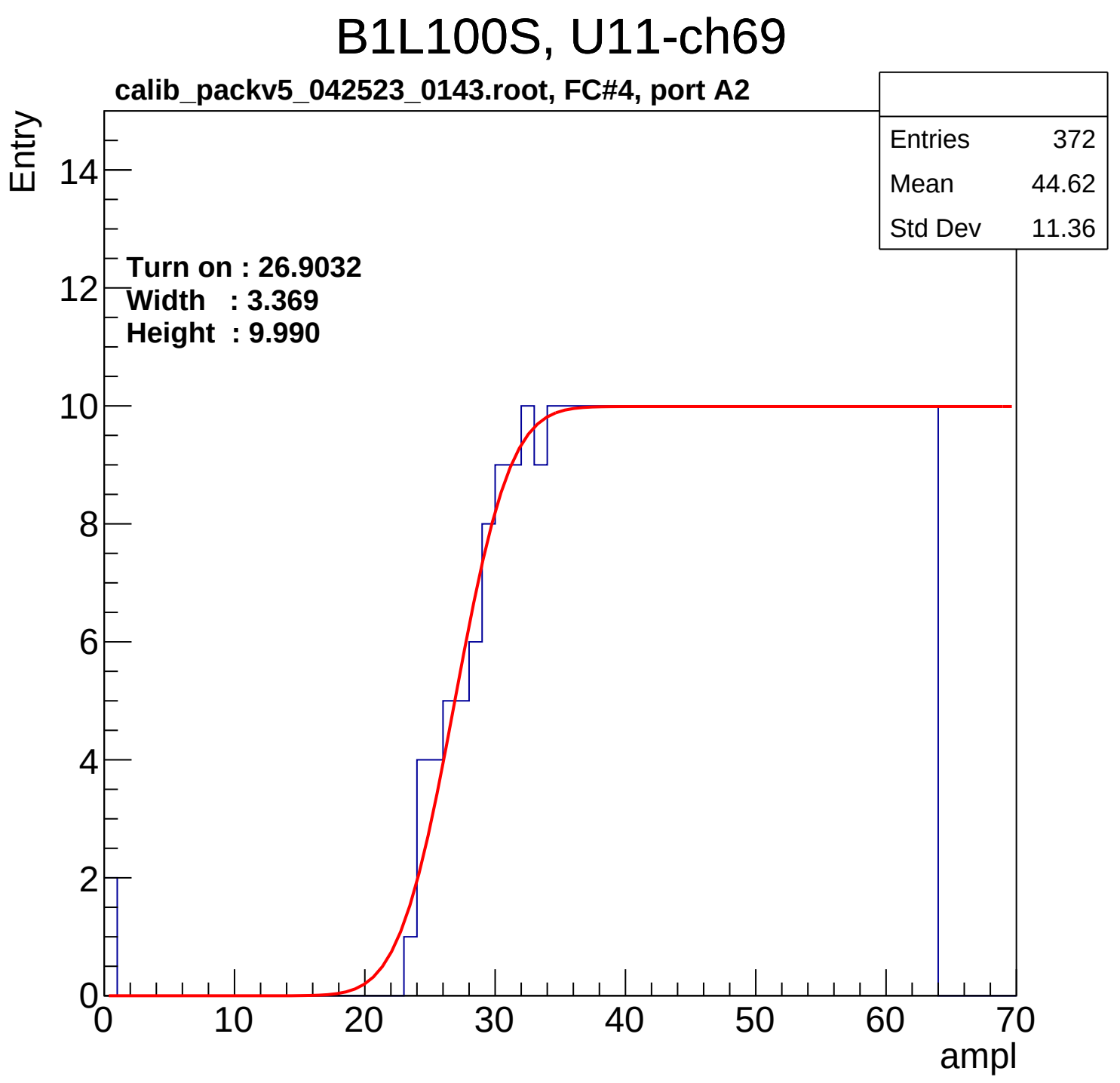
B1L100S, U11-ch69
calib_packv5_042523_0143.root, FC#4, port A2
Entries 372
Mean 44.62
Std Dev 11.36
Turn on : 26.9032
Width : 3.369
Height : 9.990
Entry
ampl
0
2
4
6
8
10
12
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0
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20
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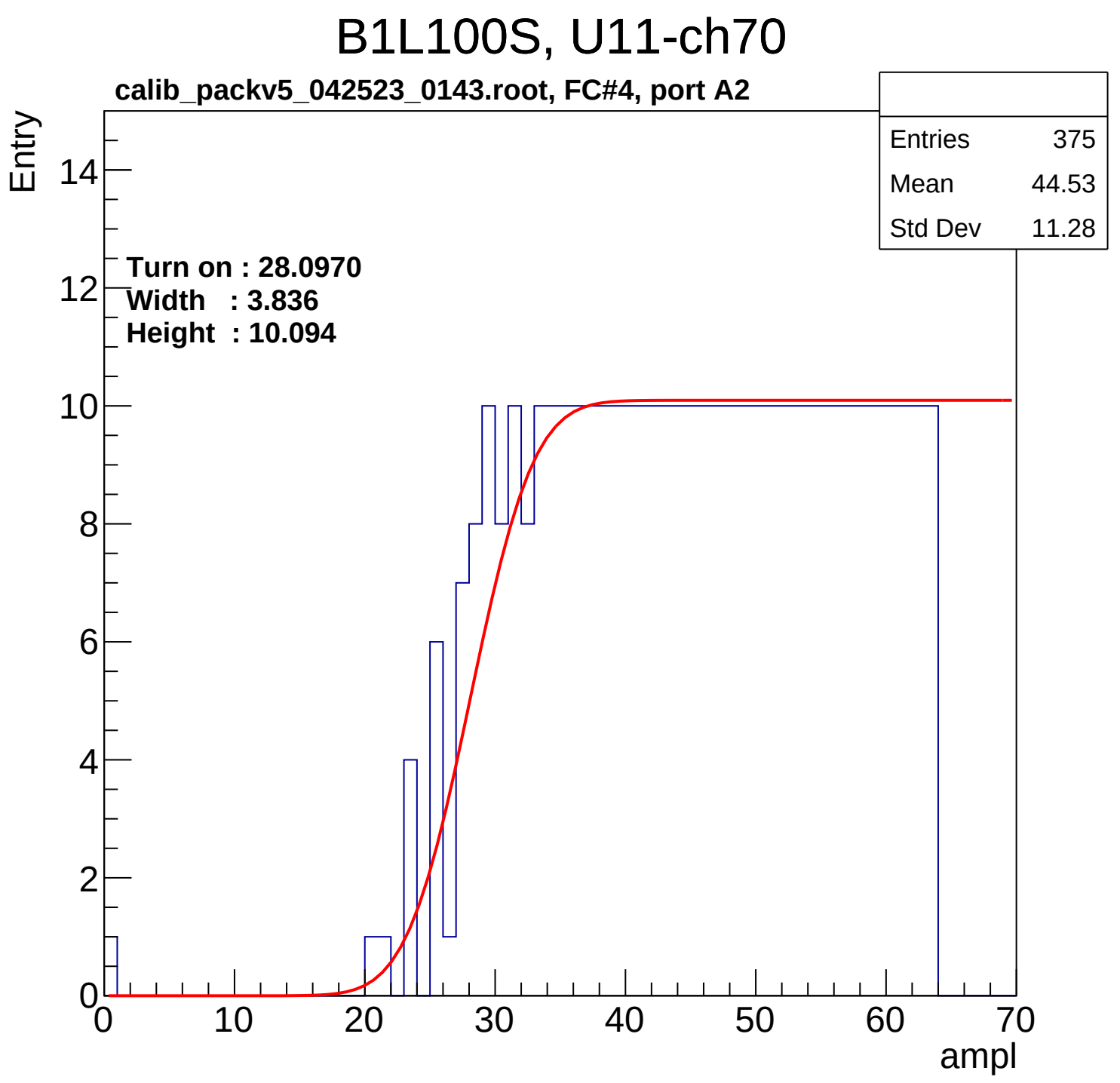
B1L100S, U11-ch70
calib_packv5_042523_0143.root, FC#4, port A2
Entries 375
Mean 44.53
Std Dev 11.28
Turn on : 28.0970
Width : 3.836
Height : 10.094
Entry
ampl
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6
8
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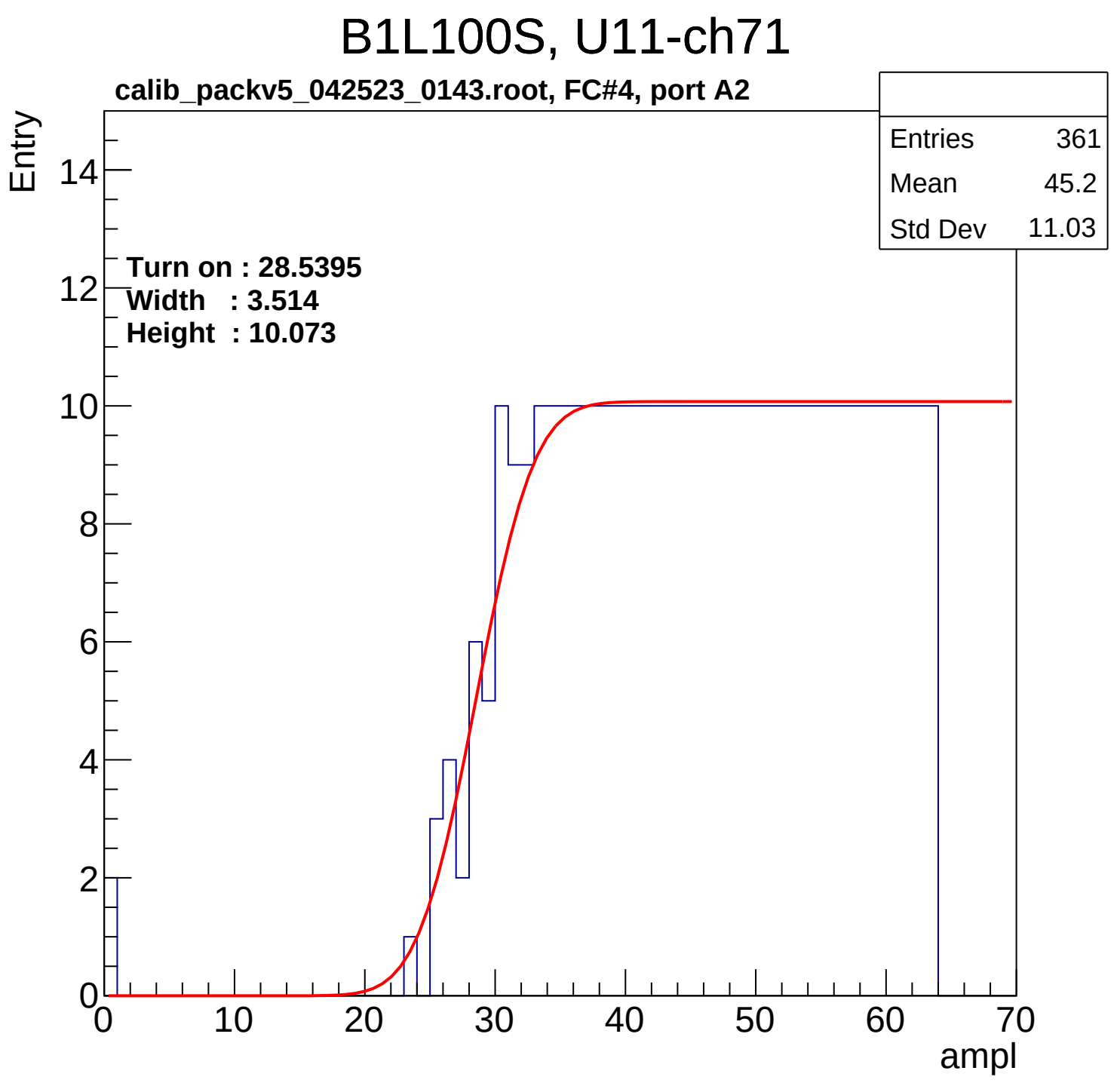
B1L100S, U11-ch71
calib_packv5_042523_0143.root, FC#4, port A2
Entries 361
Mean 45.2
Std Dev 11.03
Turn on : 28.5395
Width : 3.514
Height : 10.073
Entry
ampl
0
2
4
6
8
10
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0
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60
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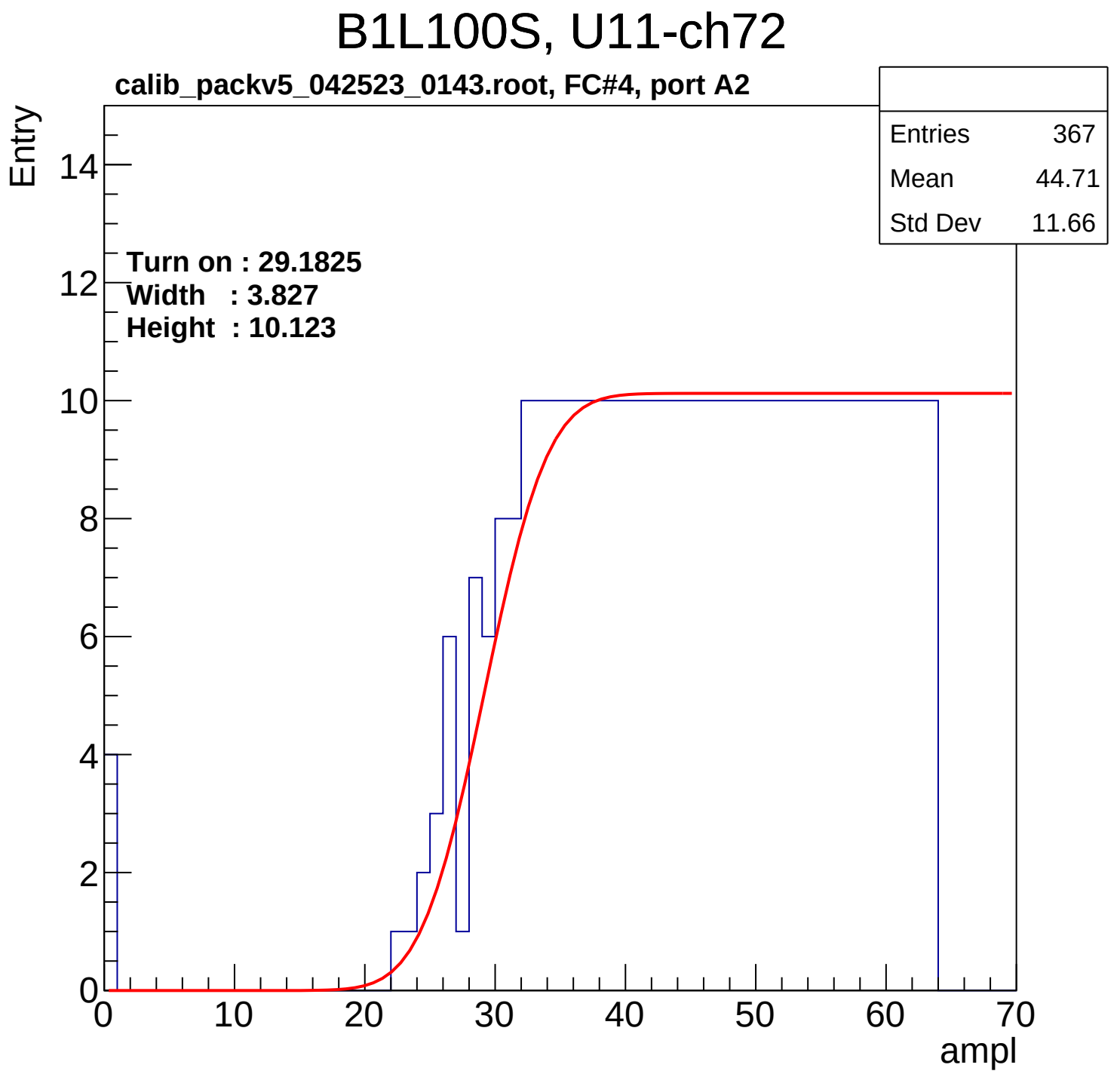
B1L100S, U11-ch72
calib_packv5_042523_0143.root, FC#4, port A2
Entries 367
Mean 44.71
Std Dev 11.66
Turn on : 29.1825
Width : 3.827
Height : 10.123
Entry
ampl
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6
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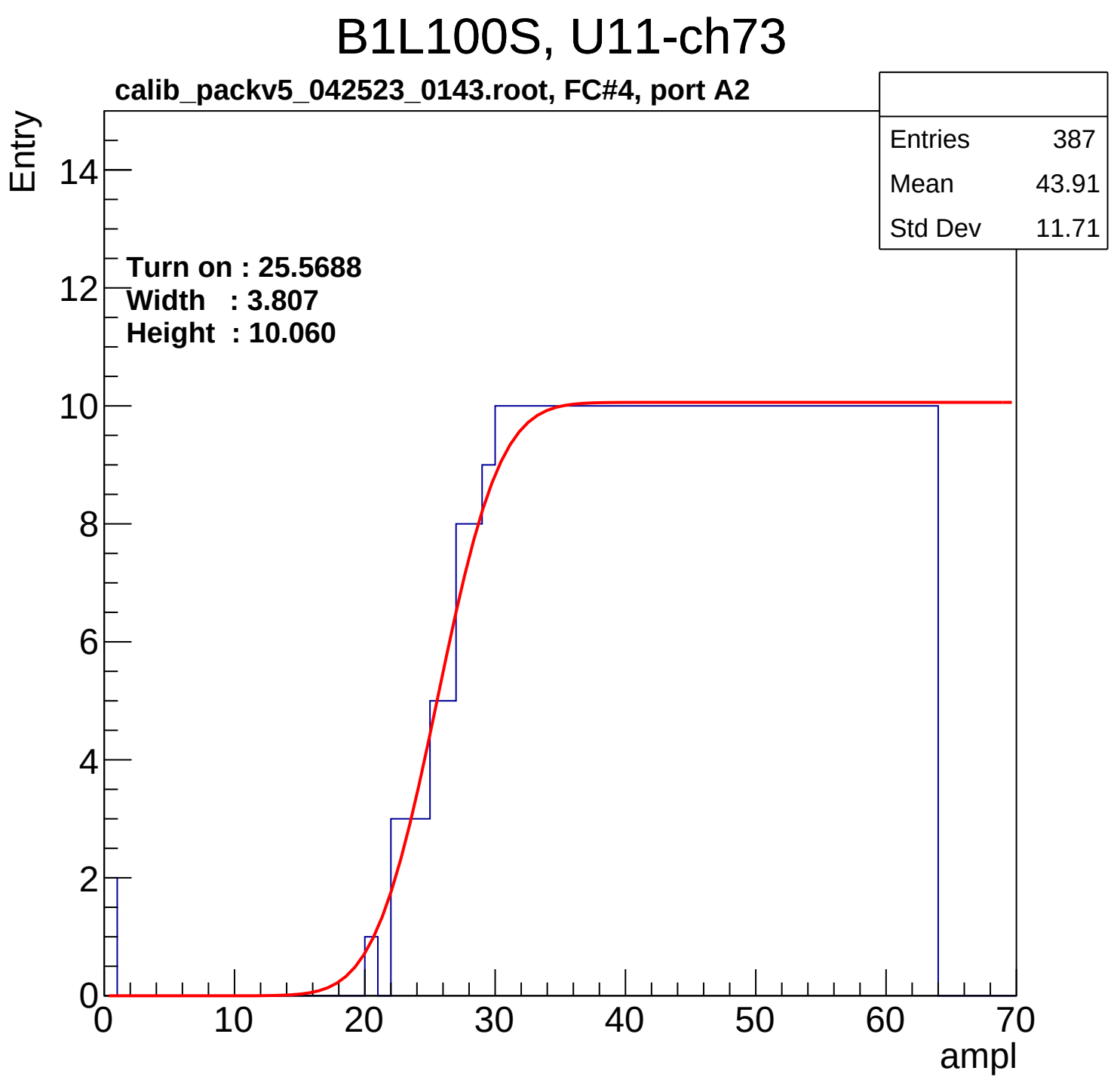
B1L100S, U11-ch73
calib_packv5_042523_0143.root, FC#4, port A2
Entries 387
Mean 43.91
Std Dev 11.71
Turn on : 25.5688
Width : 3.807
Height : 10.060
Entry
ampl
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8
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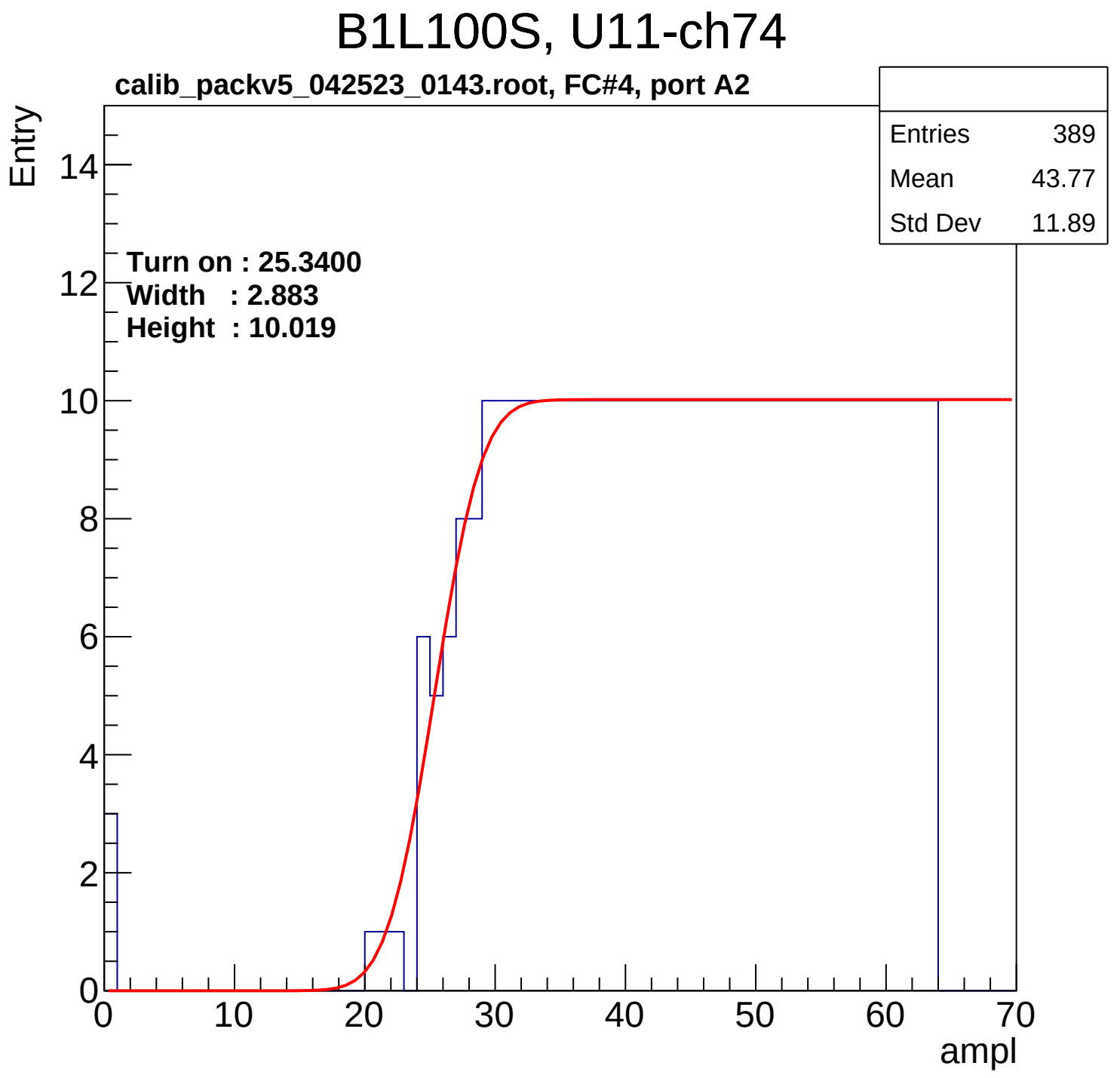
B1L100S, U11-ch74
calib_packv5_042523_0143.root, FC#4, port A2
Entries 389
Mean 43.77
Std Dev 11.89
Turn on : 25.3400
Width : 2.883
Height : 10.019
Entry
ampl
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6
8
10
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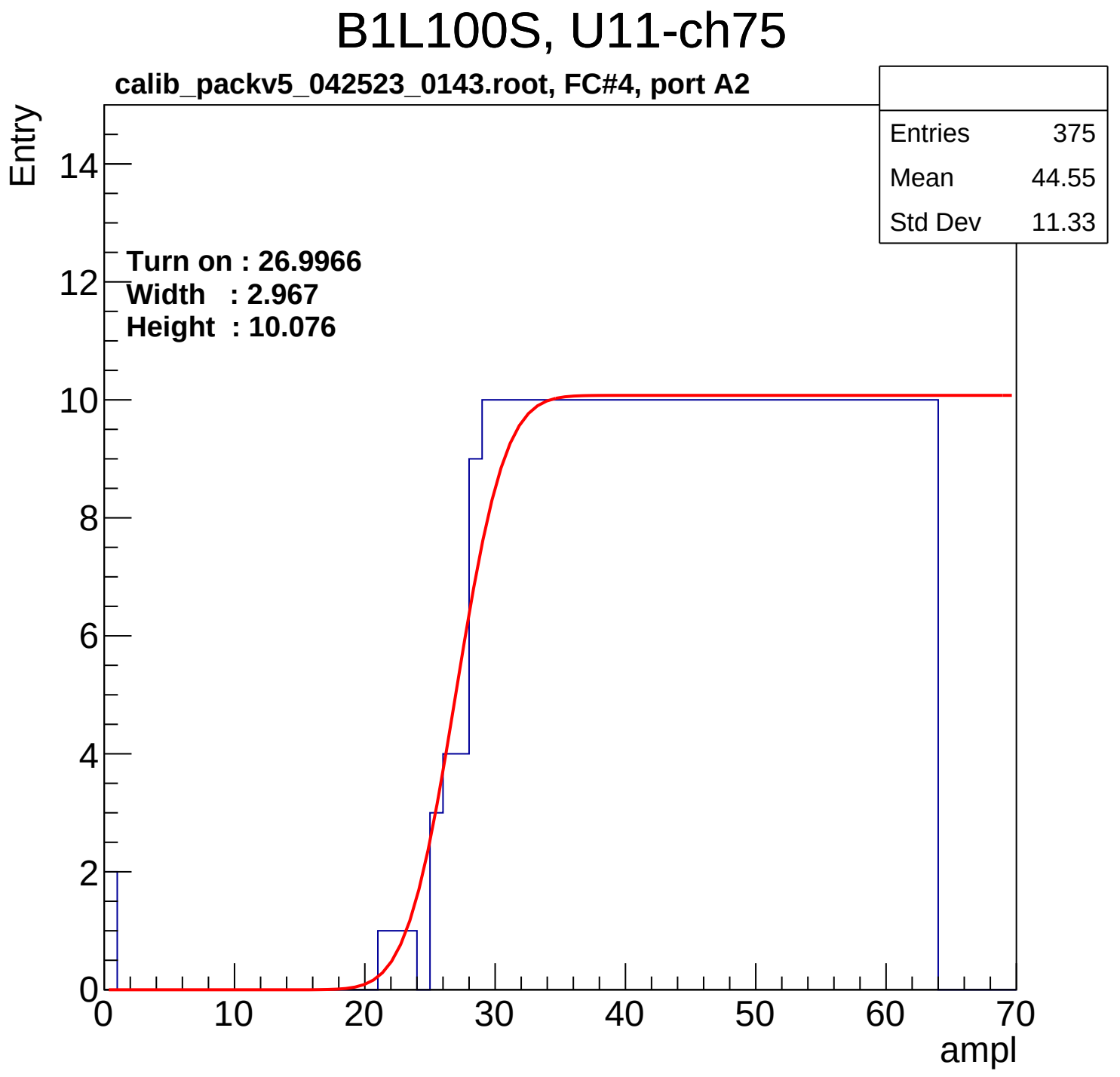
B1L100S, U11-ch75
calib_packv5_042523_0143.root, FC#4, port A2
Entries 375
Mean 44.55
Std Dev 11.33
Turn on : 26.9966
Width : 2.967
Height : 10.076
Entry
ampl
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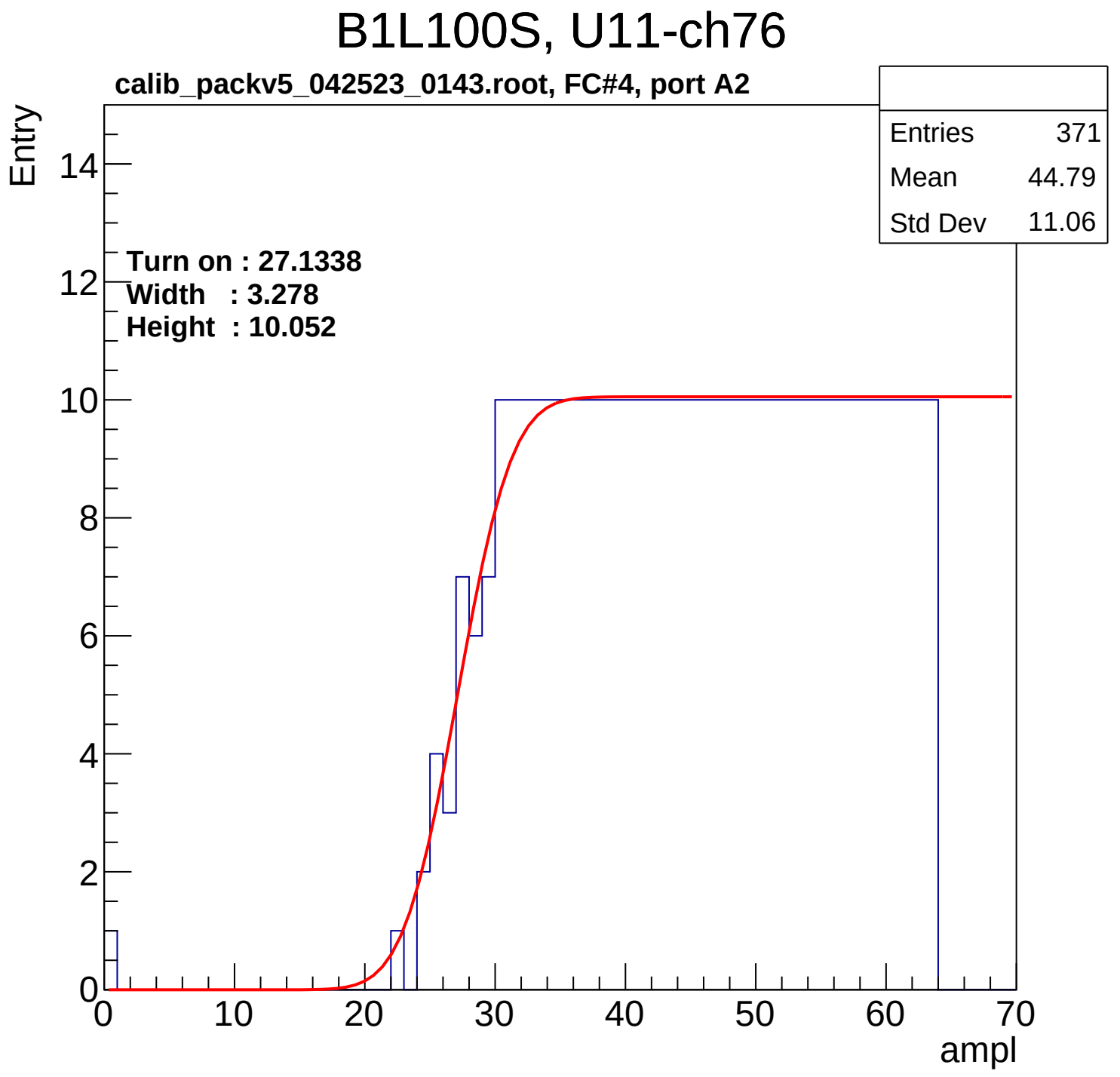
B1L100S, U11-ch76
calib_packv5_042523_0143.root, FC#4, port A2
Entries 371
Mean 44.79
Std Dev 11.06
Turn on : 27.1338
Width : 3.278
Height : 10.052
Entry
ampl
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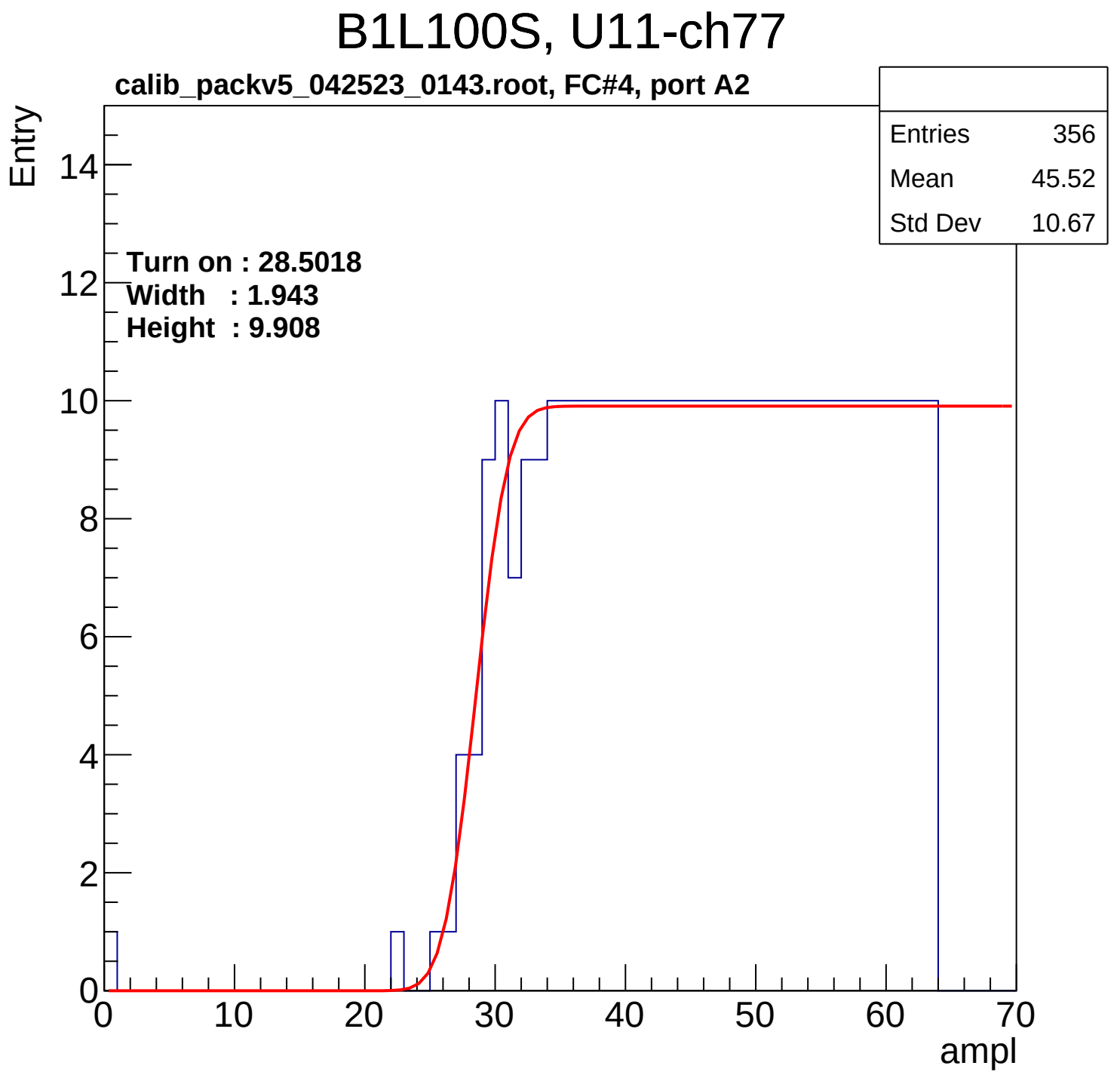
B1L100S, U11-ch77
calib_packv5_042523_0143.root, FC#4, port A2
Entries 356
Mean 45.52
Std Dev 10.67
Turn on : 28.5018
Width : 1.943
Height : 9.908
Entry
ampl
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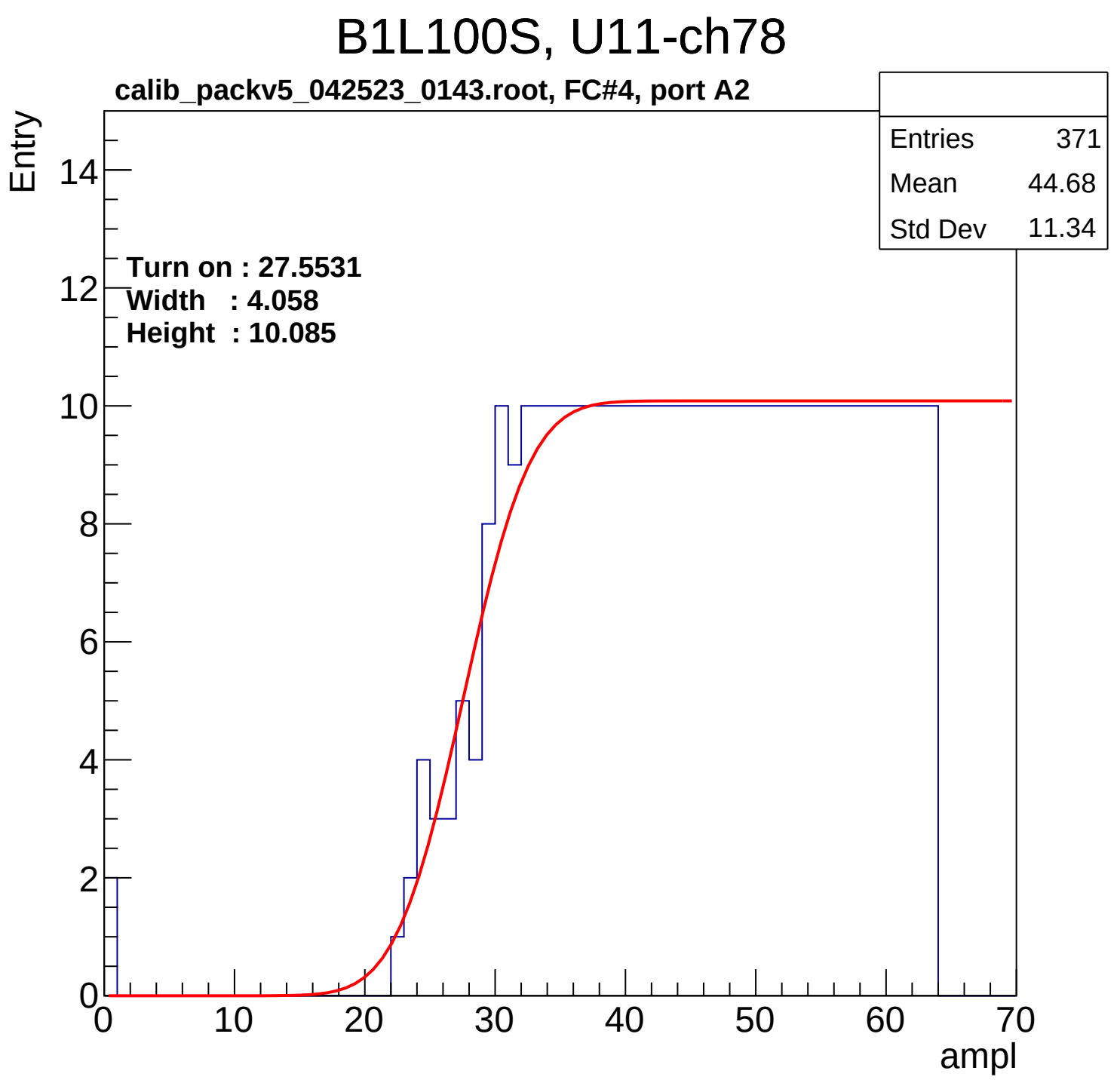
B1L100S, U11-ch78
calib_packv5_042523_0143.root, FC#4, port A2
Entries 371
Mean 44.68
Std Dev 11.34
Turn on : 27.5531
Width : 4.058
Height : 10.085
Entry
ampl
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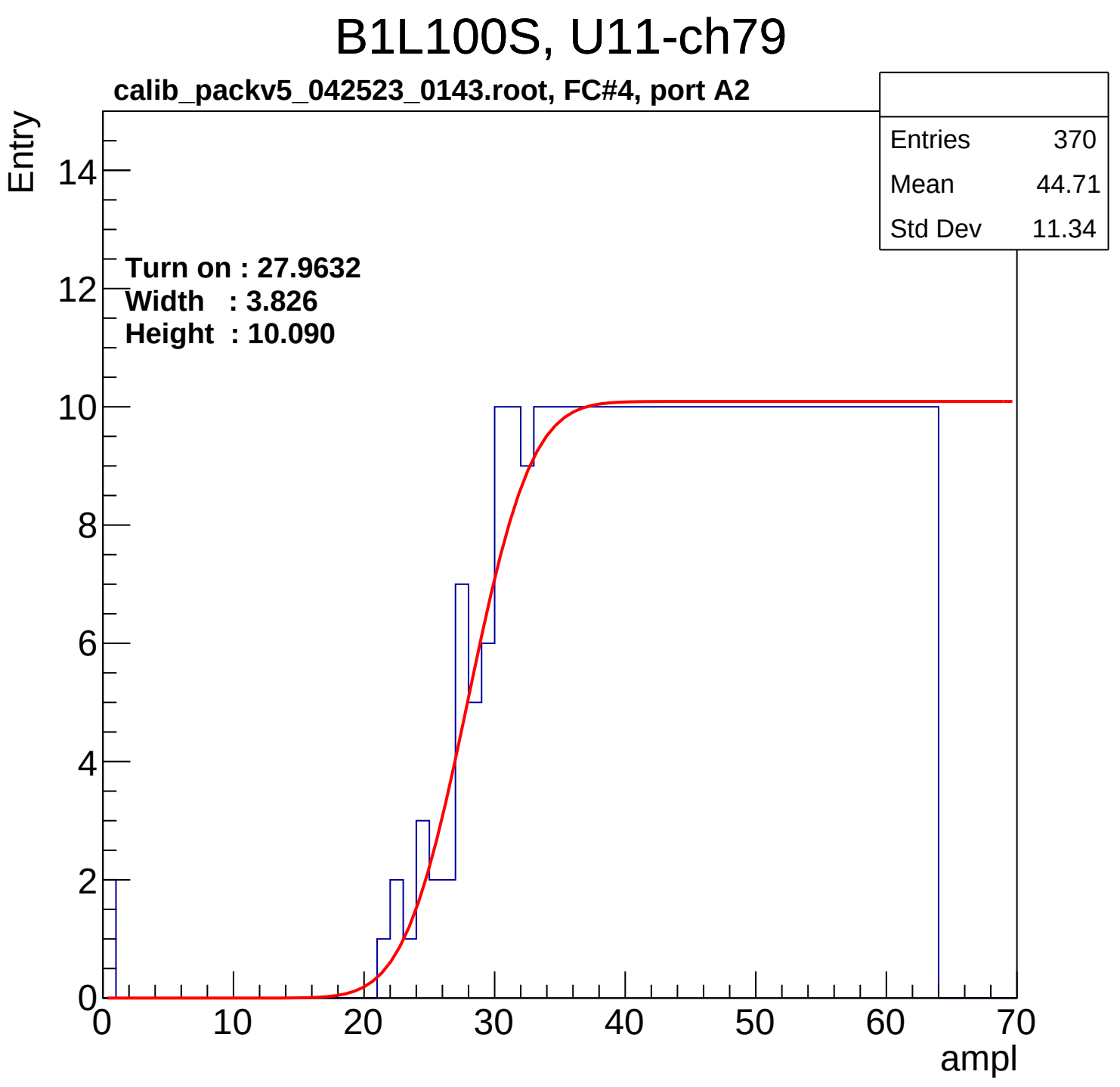
B1L100S, U11-ch79
calib_packv5_042523_0143.root, FC#4, port A2
Entries 370
Mean 44.71
Std Dev 11.34
Turn on : 27.9632
Width : 3.826
Height : 10.090
Entry
ampl
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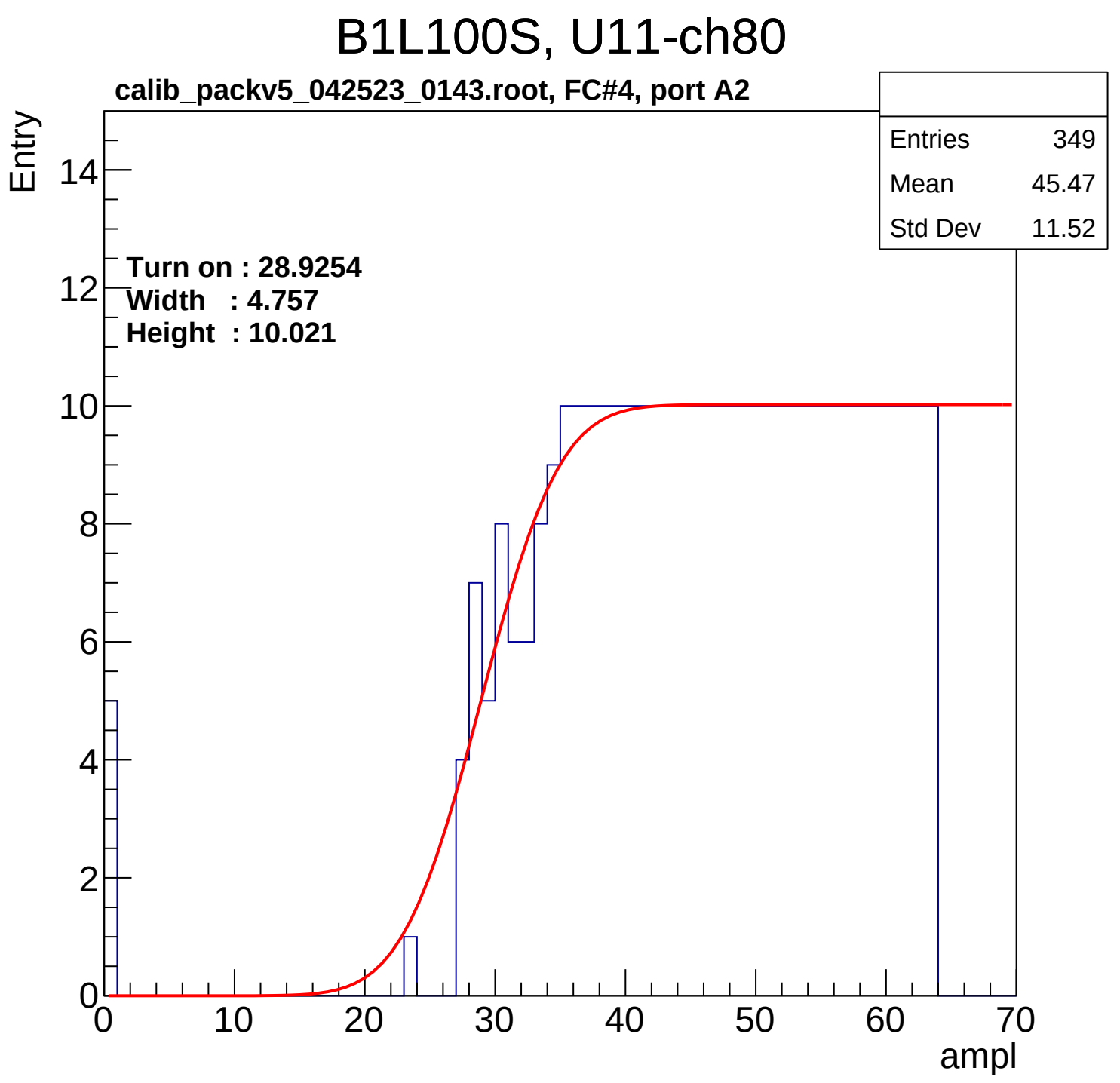
B1L100S, U11-ch80
calib_packv5_042523_0143.root, FC#4, port A2
Entries 349
Mean 45.47
Std Dev 11.52
Turn on : 28.9254
Width : 4.757
Height : 10.021
Entry
ampl
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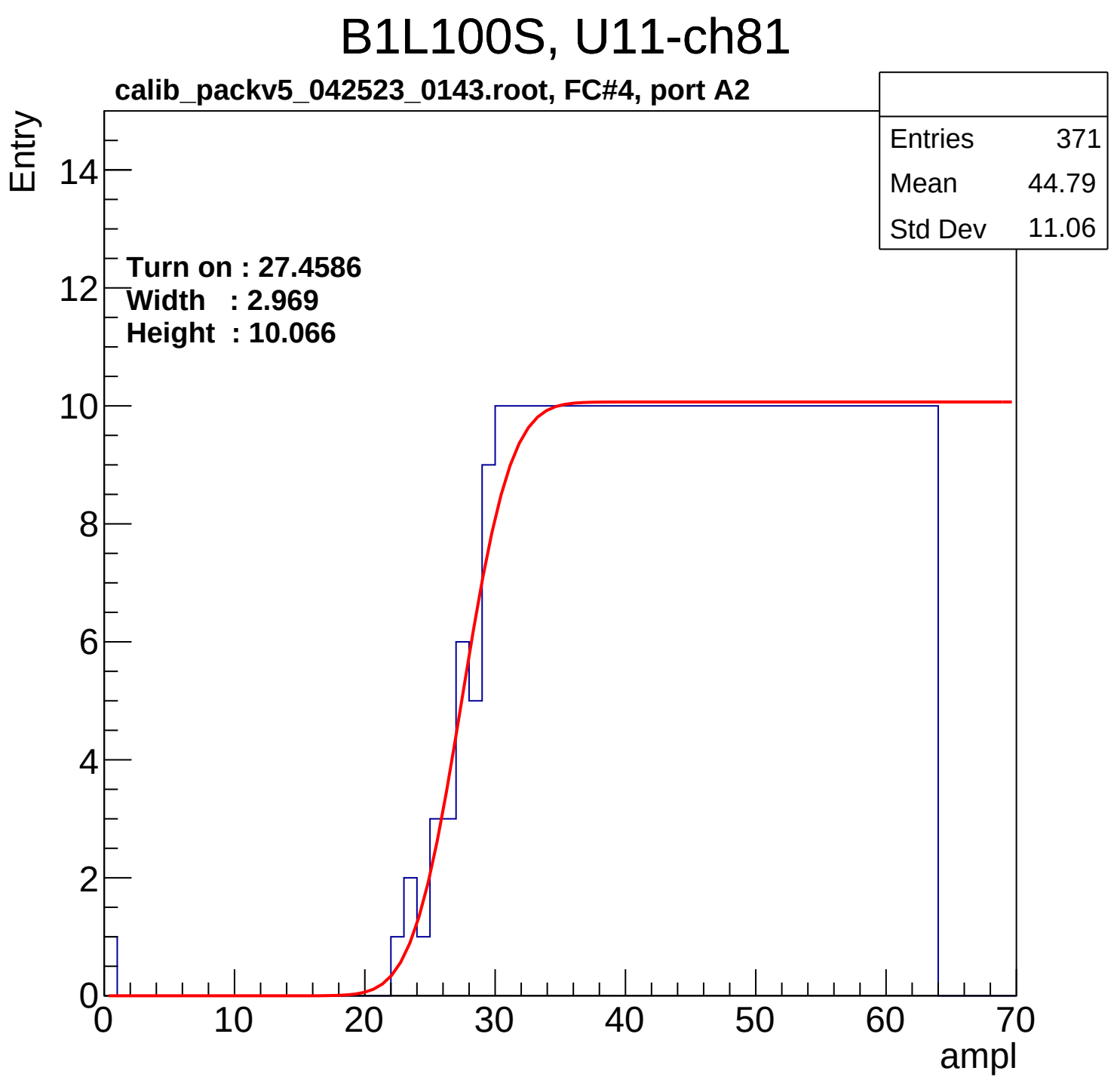
B1L100S, U11-ch81
calib_packv5_042523_0143.root, FC#4, port A2
Entries 371
Mean 44.79
Std Dev 11.06
Turn on : 27.4586
Width : 2.969
Height : 10.066
Entry
ampl
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2
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6
8
10
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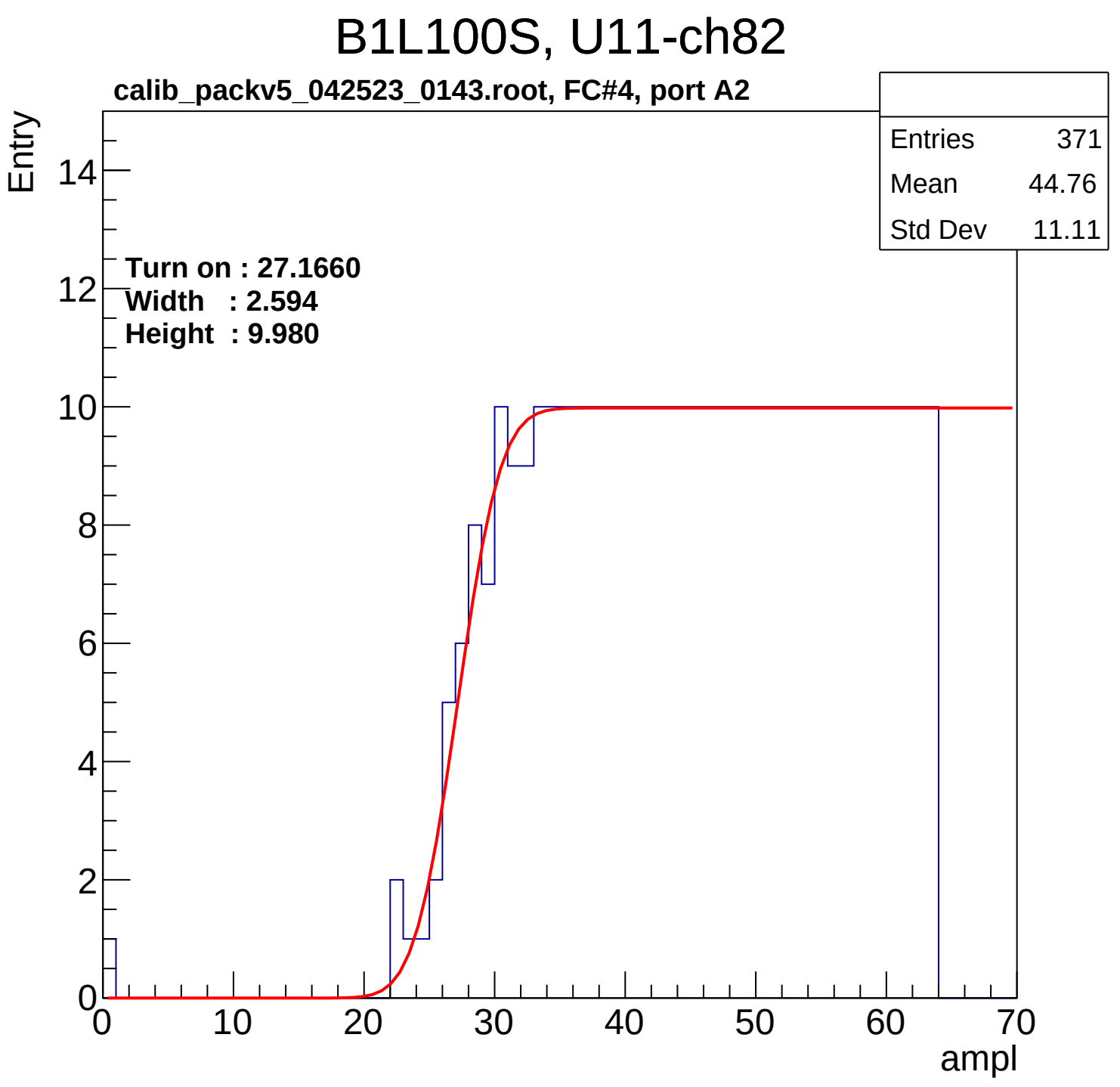
B1L100S, U11-ch82
calib_packv5_042523_0143.root, FC#4, port A2
Entries 371
Mean 44.76
Std Dev 11.11
Turn on : 27.1660
Width : 2.594
Height : 9.980
Entry
ampl
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6
8
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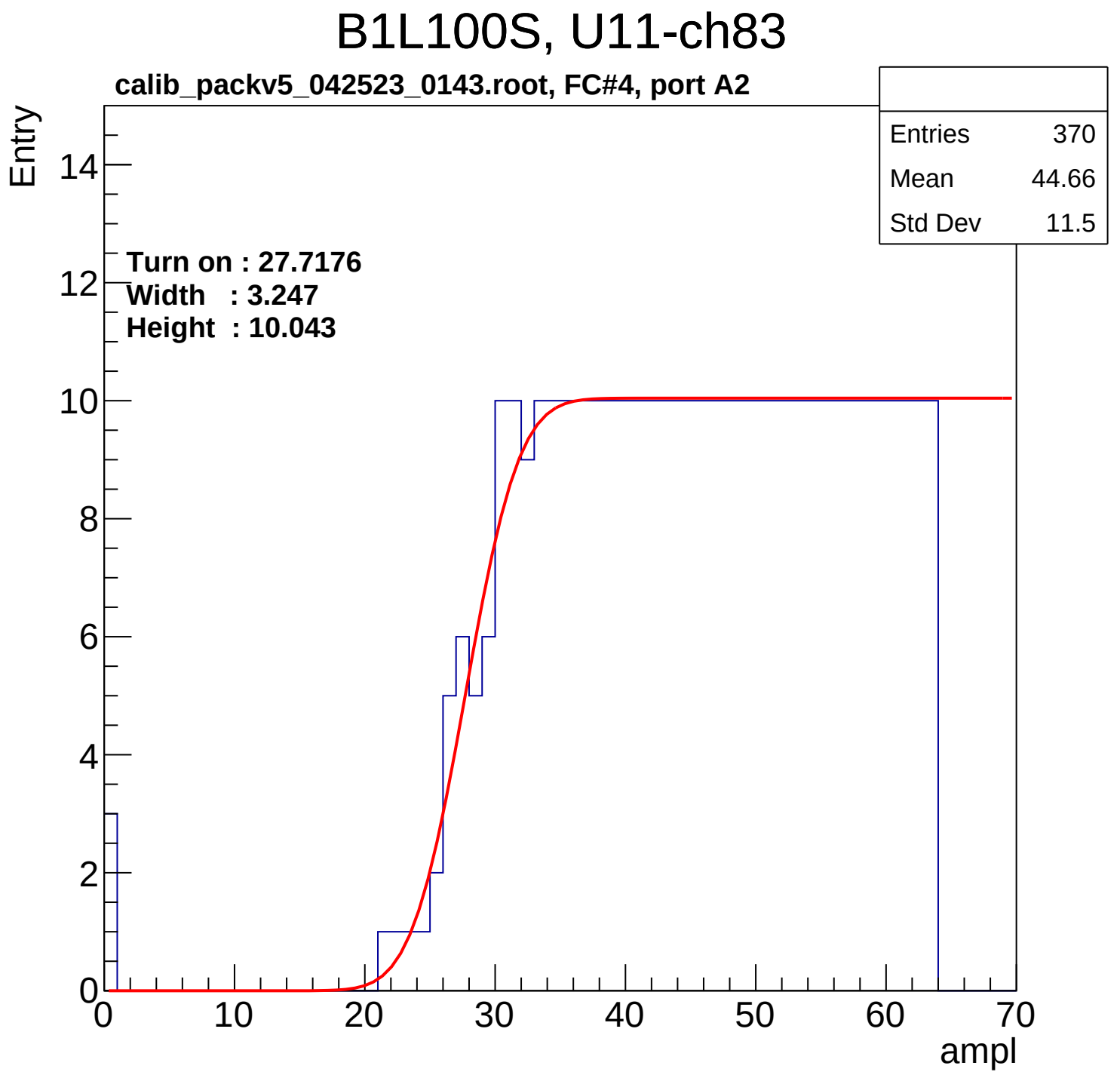
B1L100S, U11-ch83
calib_packv5_042523_0143.root, FC#4, port A2
Entries 370
Mean 44.66
Std Dev 11.5
Turn on : 27.7176
Width : 3.247
Height : 10.043
Entry
ampl
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6
8
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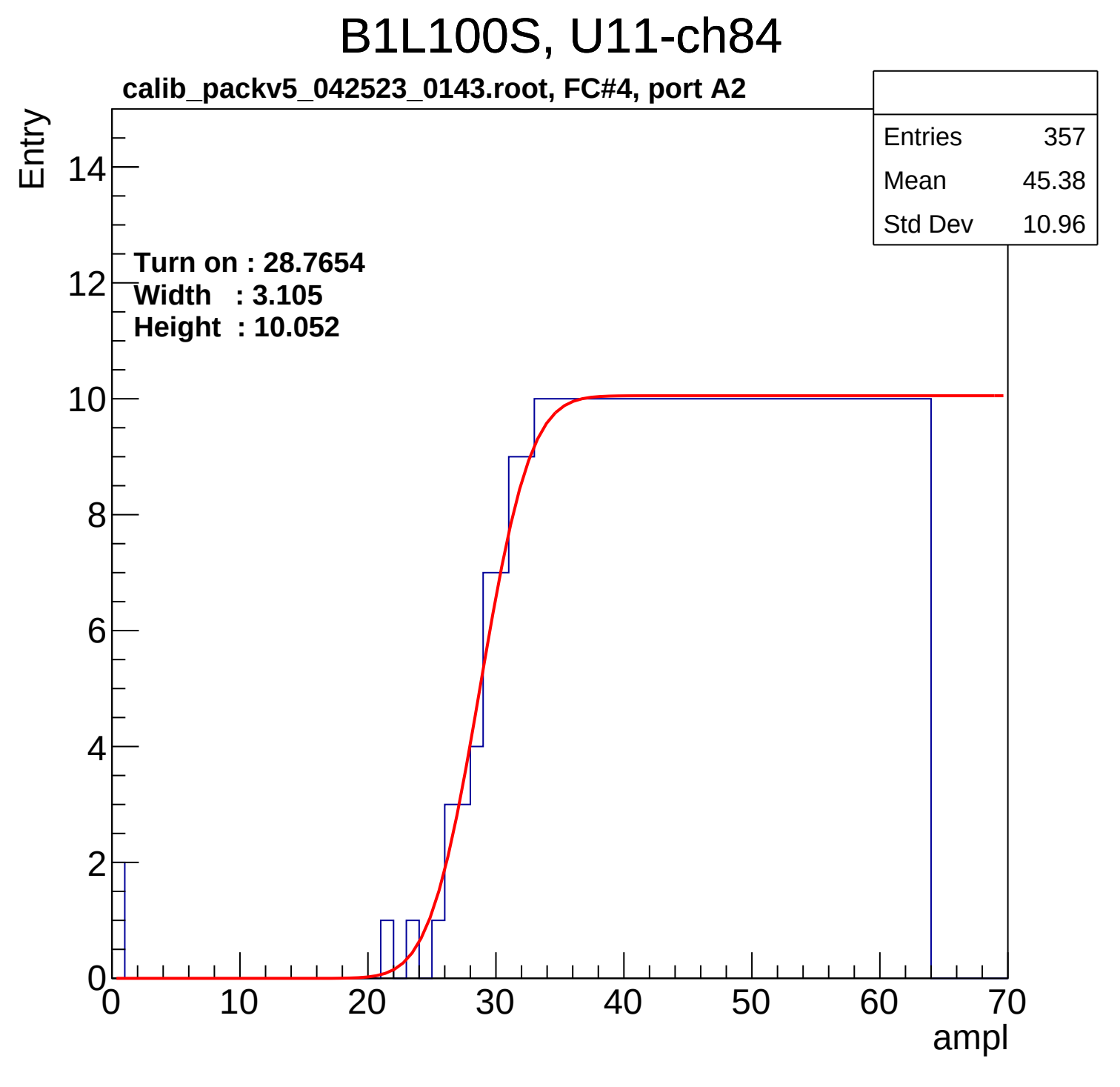
B1L100S, U11-ch84
calib_packv5_042523_0143.root, FC#4, port A2
Entries 357
Mean 45.38
Std Dev 10.96
Turn on : 28.7654
Width : 3.105
Height : 10.052
Entry
ampl
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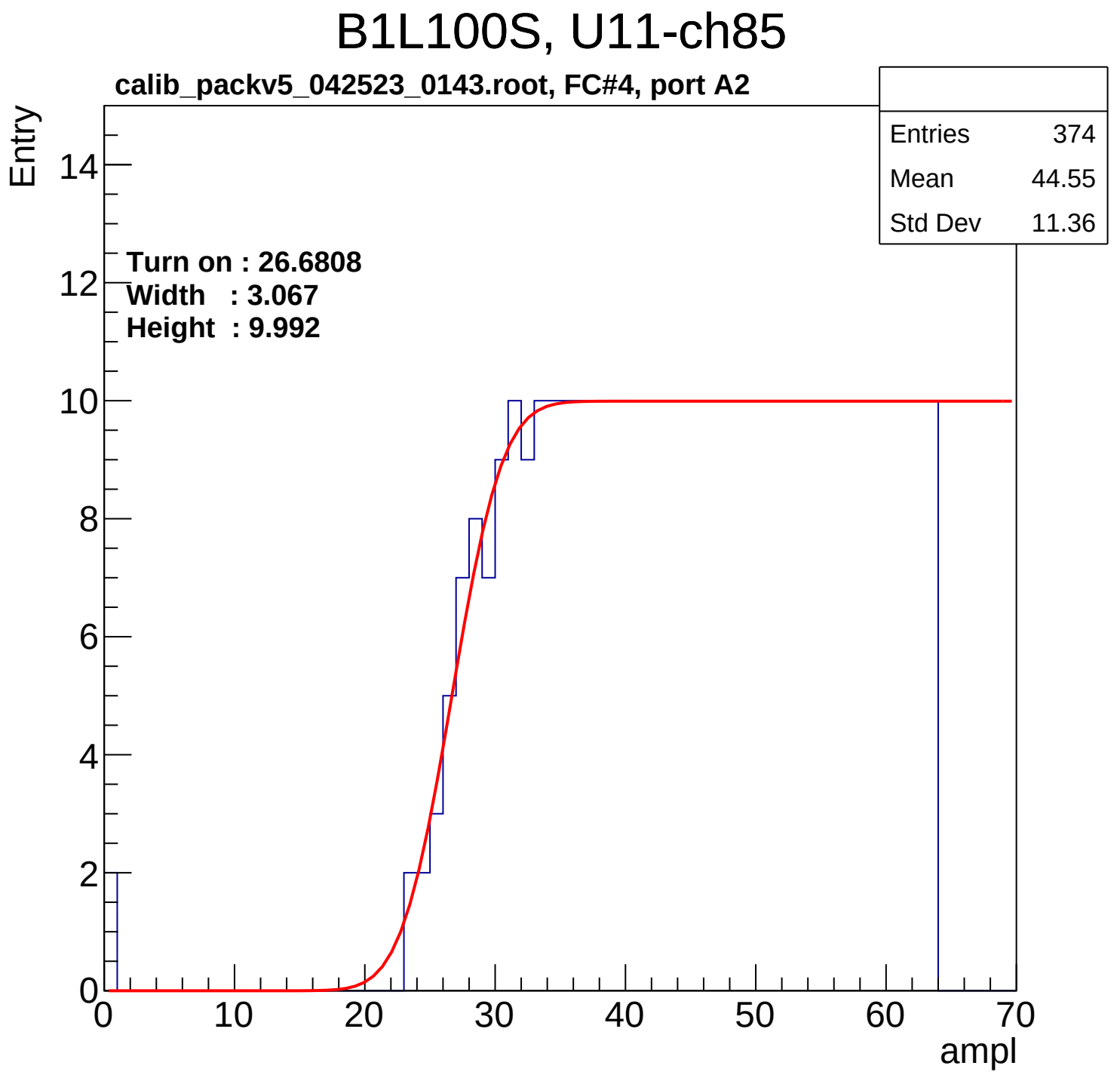
B1L100S, U11-ch85
calib_packv5_042523_0143.root, FC#4, port A2
Entries 374
Mean 44.55
Std Dev 11.36
Turn on : 26.6808
Width : 3.067
Height : 9.992
Entry
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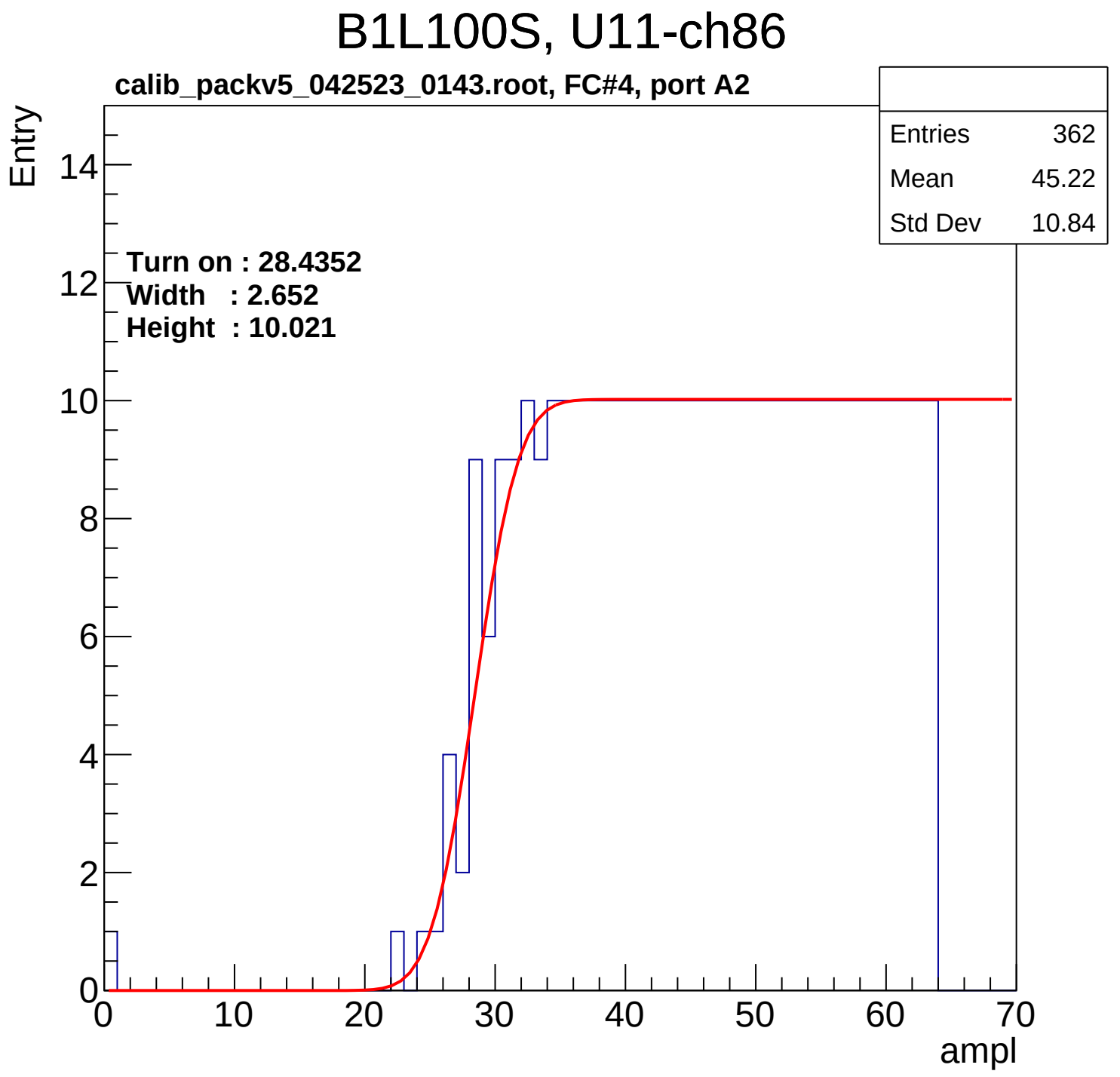
B1L100S, U11-ch86
calib_packv5_042523_0143.root, FC#4, port A2
Entries 362
Mean 45.22
Std Dev 10.84
Turn on : 28.4352
Width : 2.652
Height : 10.021
Entry
ampl
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2
4
6
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10
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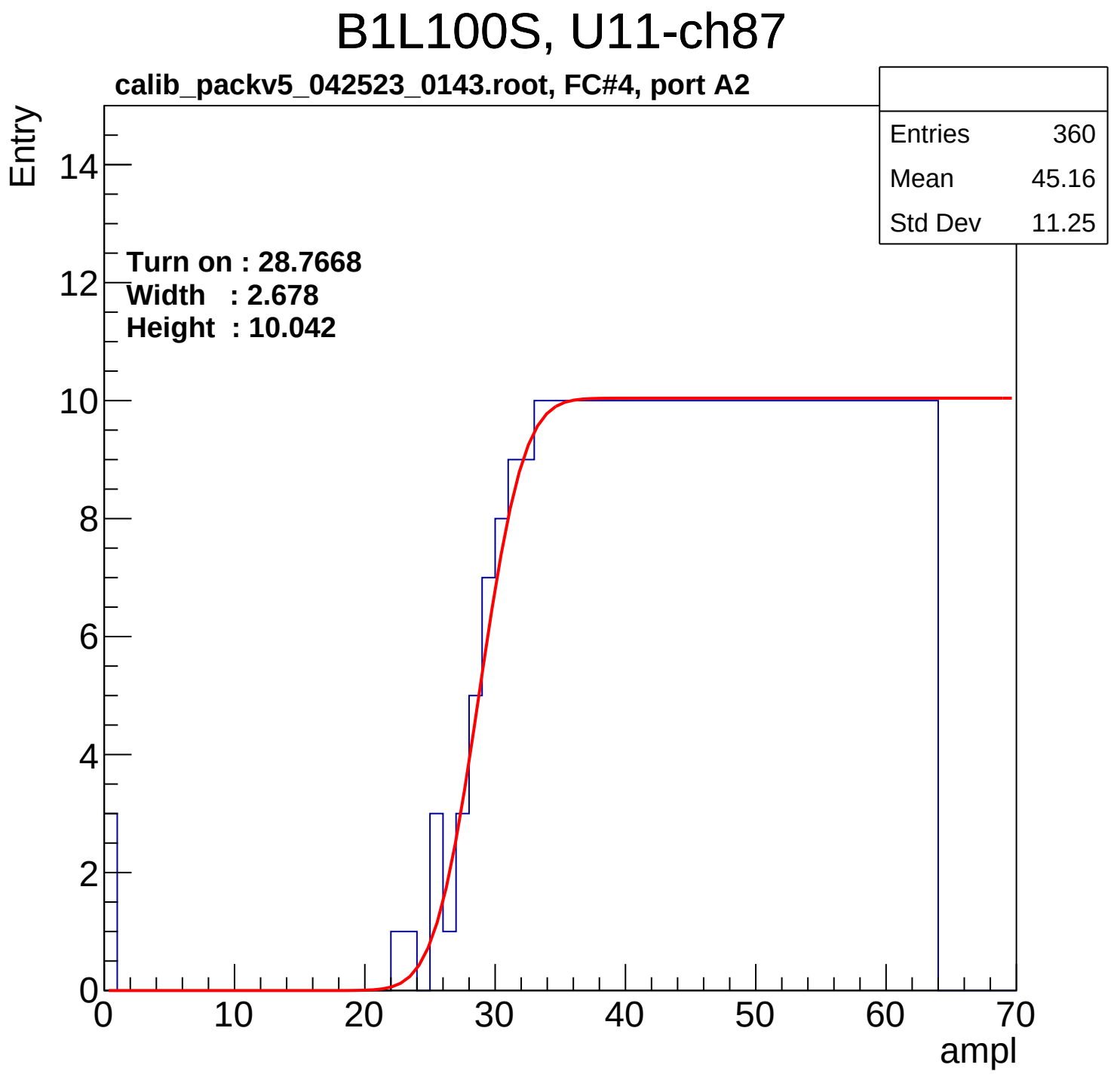
B1L100S, U11-ch87
calib_packv5_042523_0143.root, FC#4, port A2
Entries 360
Mean 45.16
Std Dev 11.25
Turn on : 28.7668
Width : 2.678
Height : 10.042
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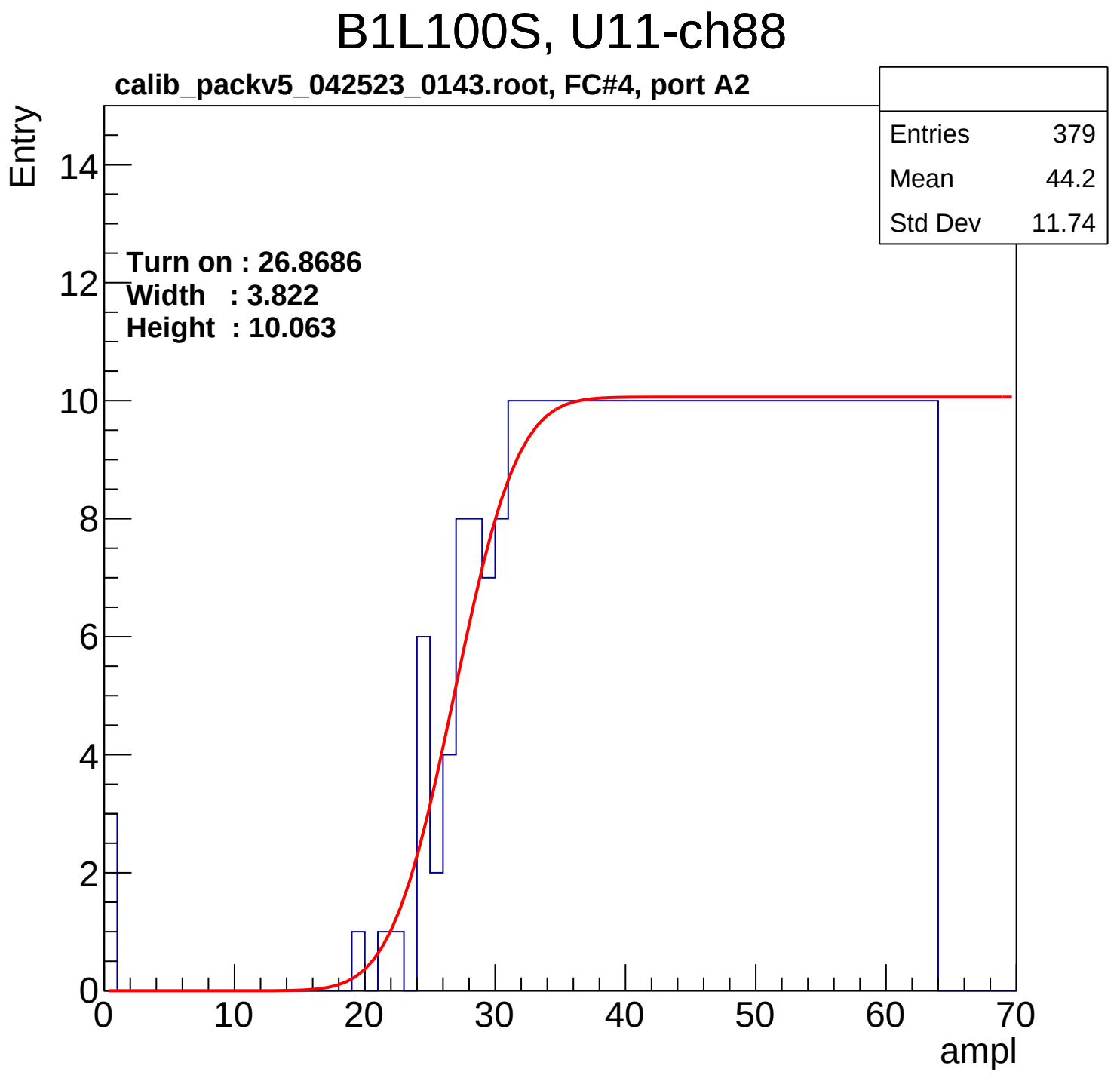
B1L100S, U11-ch88
calib_packv5_042523_0143.root, FC#4, port A2
Entries 379
Mean 44.2
Std Dev 11.74
Turn on : 26.8686
Width : 3.822
Height : 10.063
Entry
ampl
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2
4
6
8
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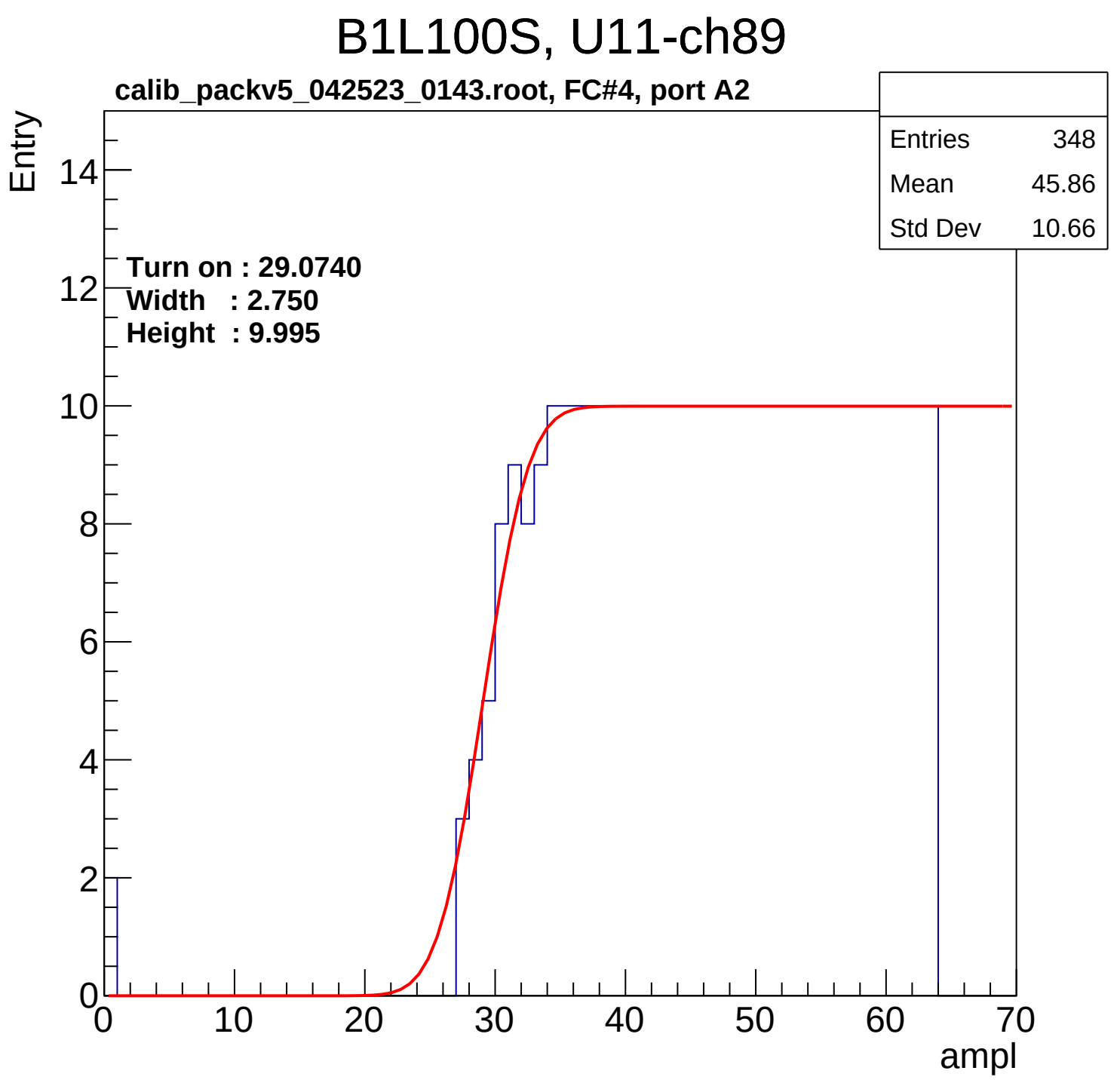
B1L100S, U11-ch89
calib_packv5_042523_0143.root, FC#4, port A2
Entries 348
Mean 45.86
Std Dev 10.66
Turn on : 29.0740
Width : 2.750
Height : 9.995
Entry
ampl
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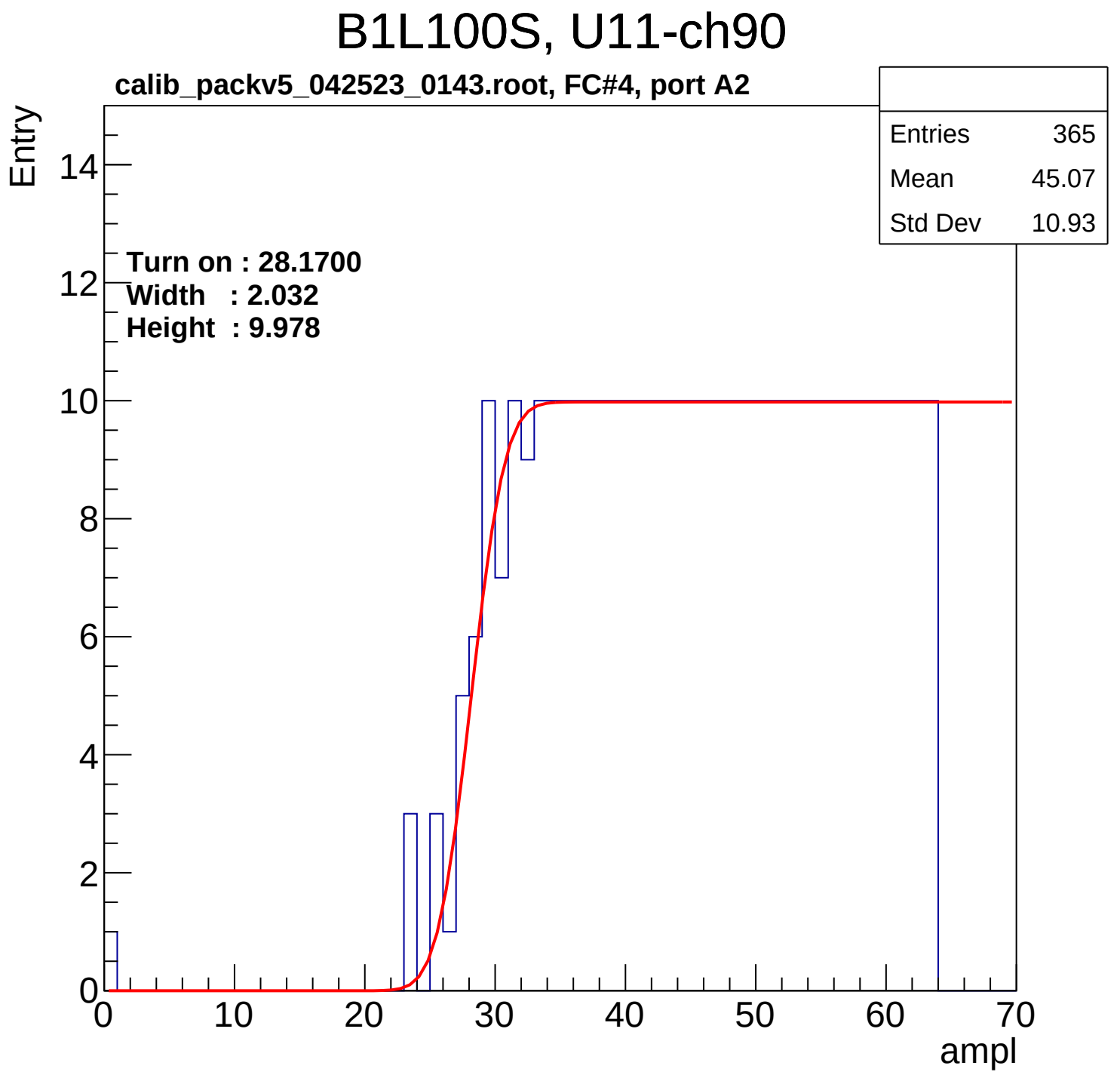
B1L100S, U11-ch90
calib_packv5_042523_0143.root, FC#4, port A2
Entries 365
Mean 45.07
Std Dev 10.93
Turn on : 28.1700
Width : 2.032
Height : 9.978
Entry
ampl
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2
4
6
8
10
12
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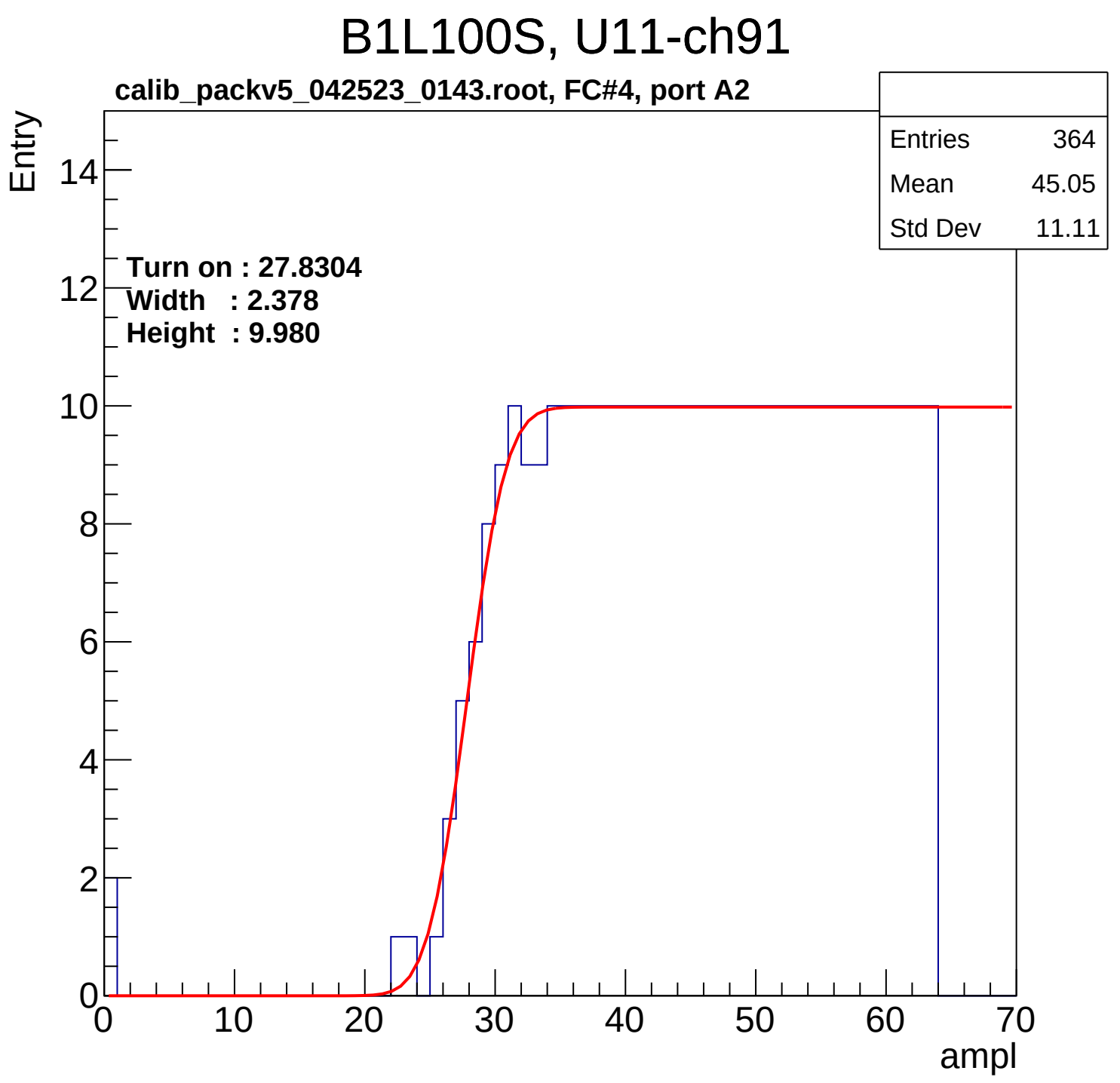
B1L100S, U11-ch91
calib_packv5_042523_0143.root, FC#4, port A2
Entries 364
Mean 45.05
Std Dev 11.11
Turn on : 27.8304
Width : 2.378
Height : 9.980
Entry
ampl
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2
4
6
8
10
12
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0
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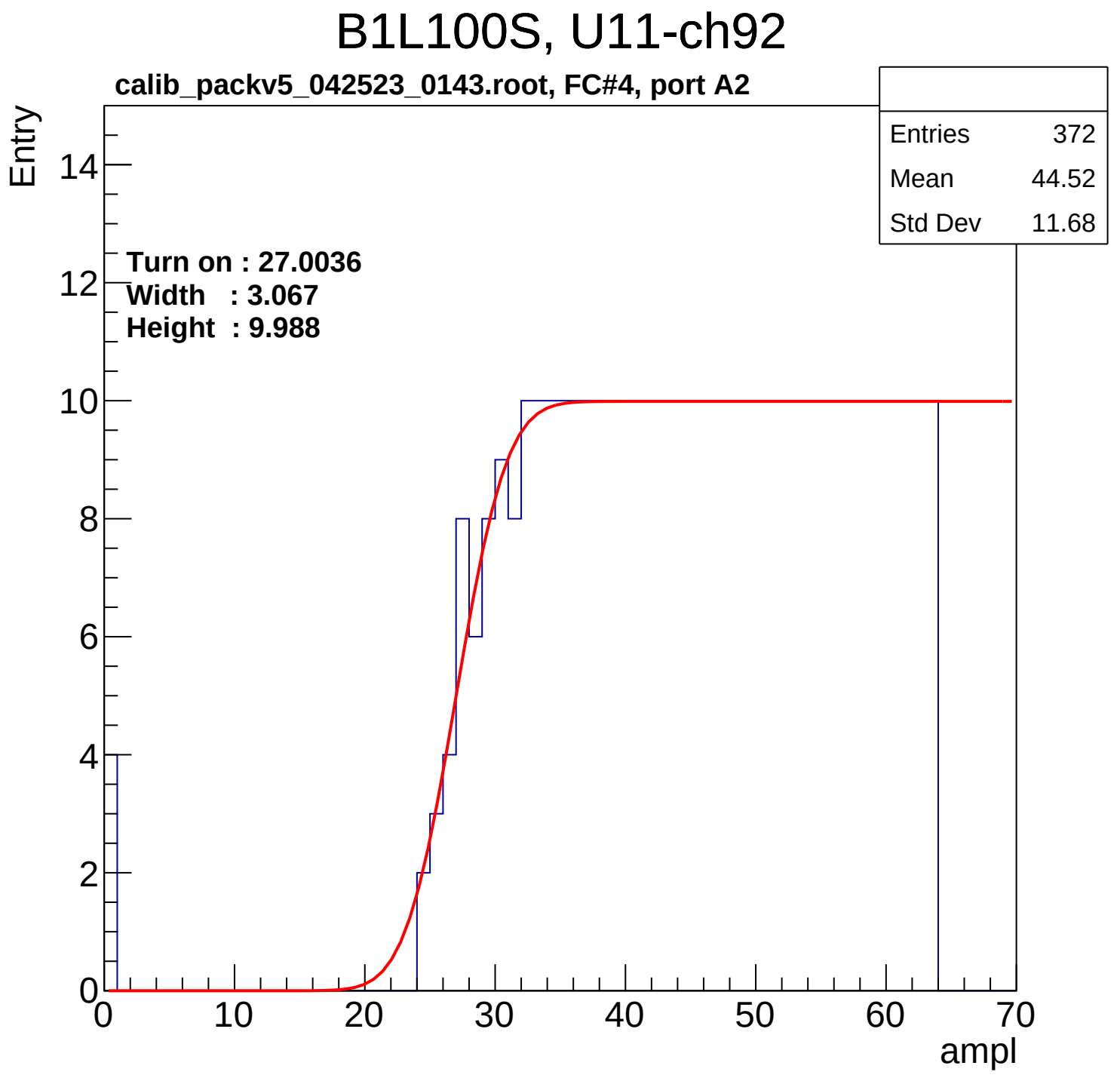
B1L100S, U11-ch92
calib_packv5_042523_0143.root, FC#4, port A2
Entries 372
Mean 44.52
Std Dev 11.68
Turn on : 27.0036
Width : 3.067
Height : 9.988
Entry
ampl
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2
4
6
8
10
12
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0
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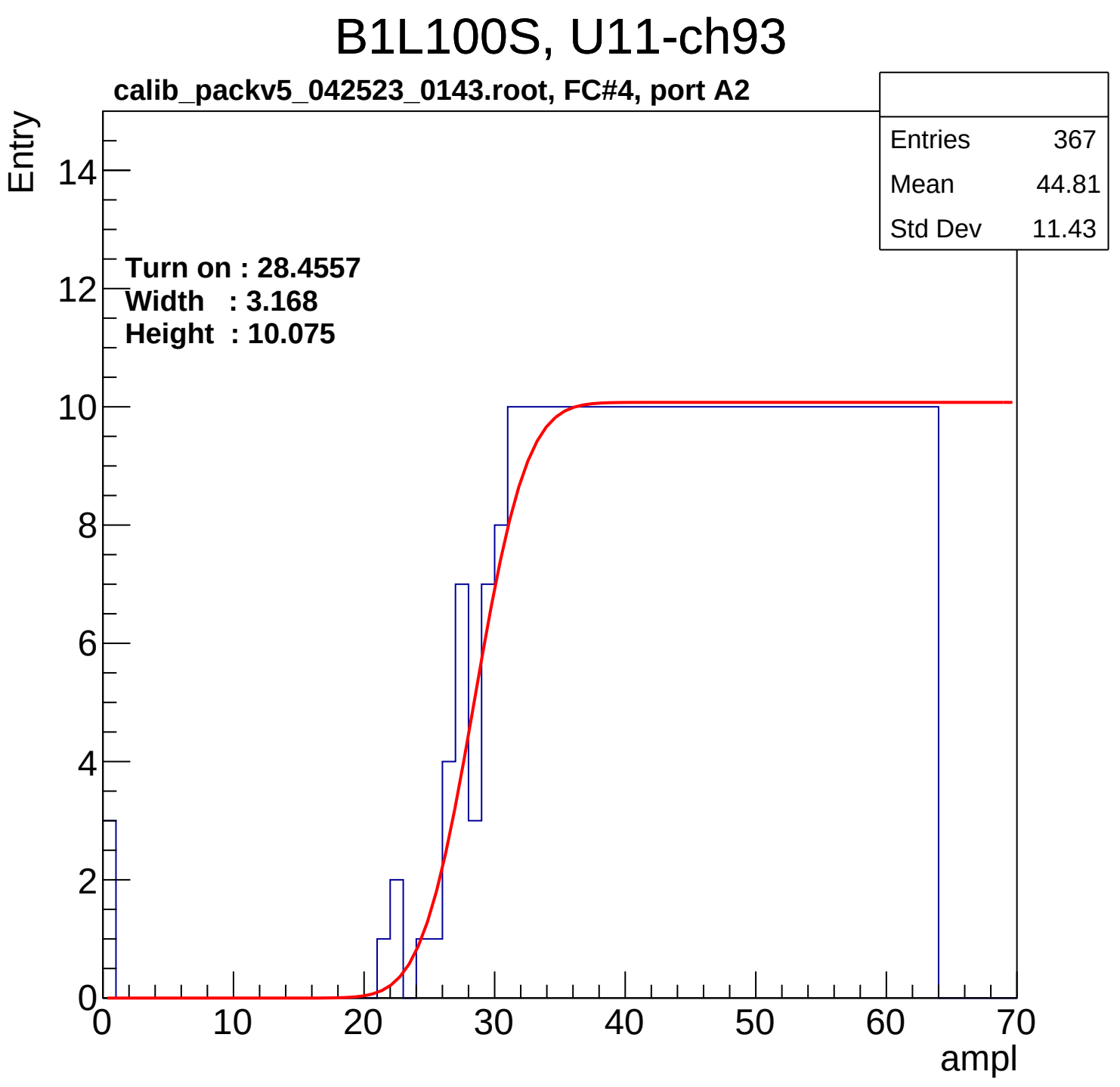
B1L100S, U11-ch93
calib_packv5_042523_0143.root, FC#4, port A2
Entries 367
Mean 44.81
Std Dev 11.43
Turn on : 28.4557
Width : 3.168
Height : 10.075
Entry
ampl
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2
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6
8
10
12
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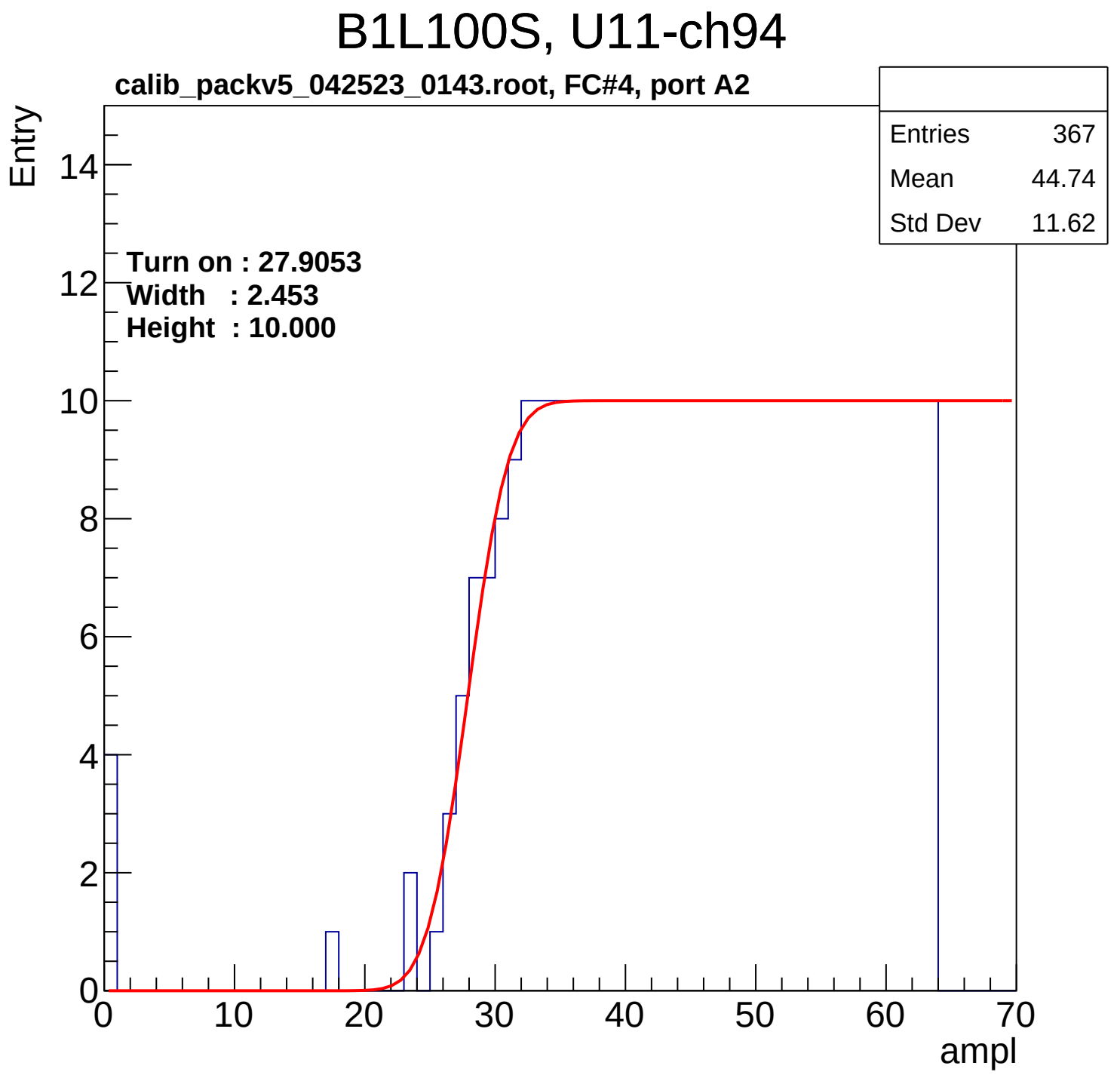
B1L100S, U11-ch94
calib_packv5_042523_0143.root, FC#4, port A2
Entries 367
Mean 44.74
Std Dev 11.62
Turn on : 27.9053
Width : 2.453
Height : 10.000
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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40
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60
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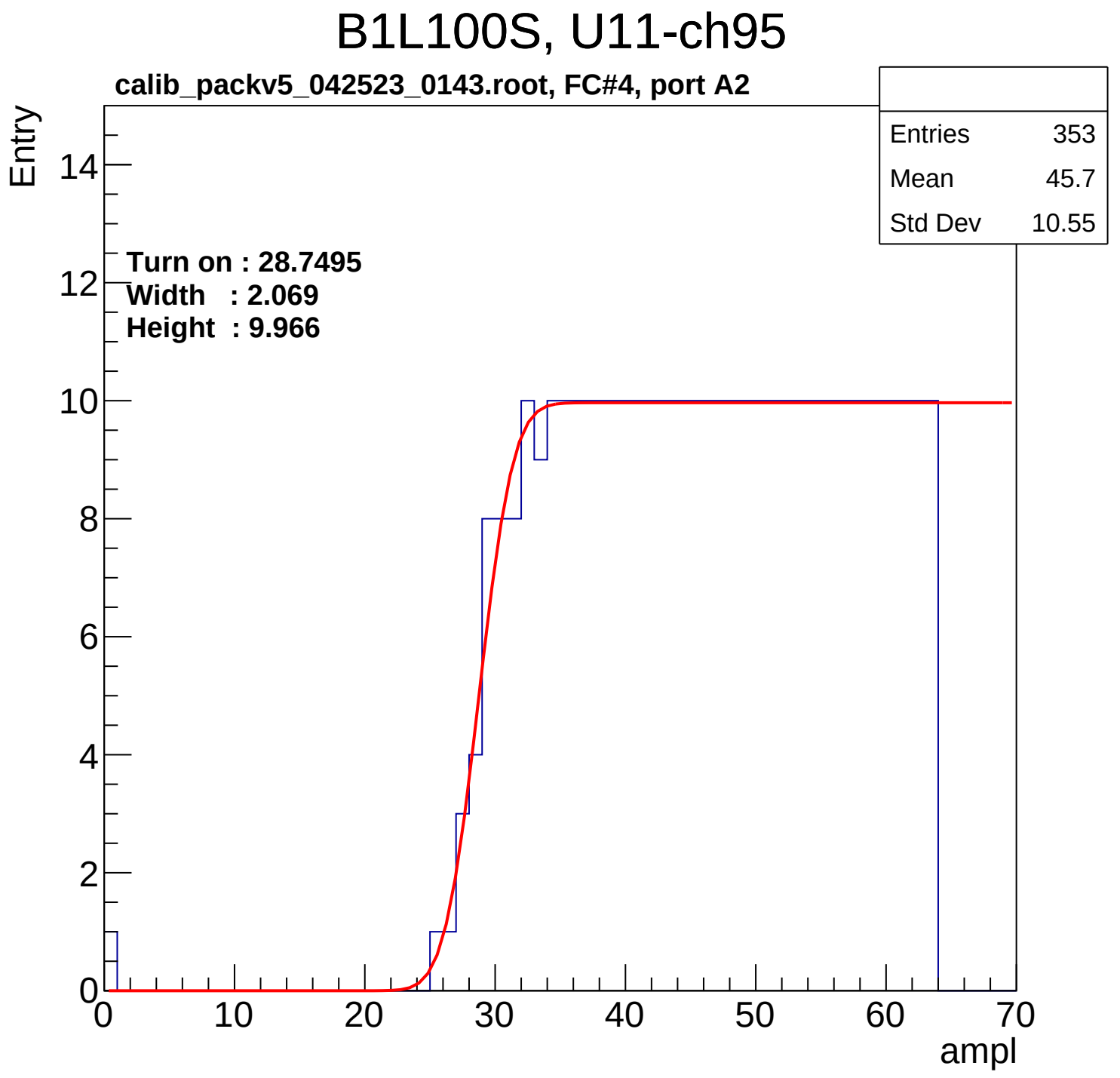
B1L100S, U11-ch95
calib_packv5_042523_0143.root, FC#4, port A2
Entries 353
Mean 45.7
Std Dev 10.55
Turn on : 28.7495
Width : 2.069
Height : 9.966
Entry
ampl
0
2
4
6
8
10
12
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0
10
20
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40
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60
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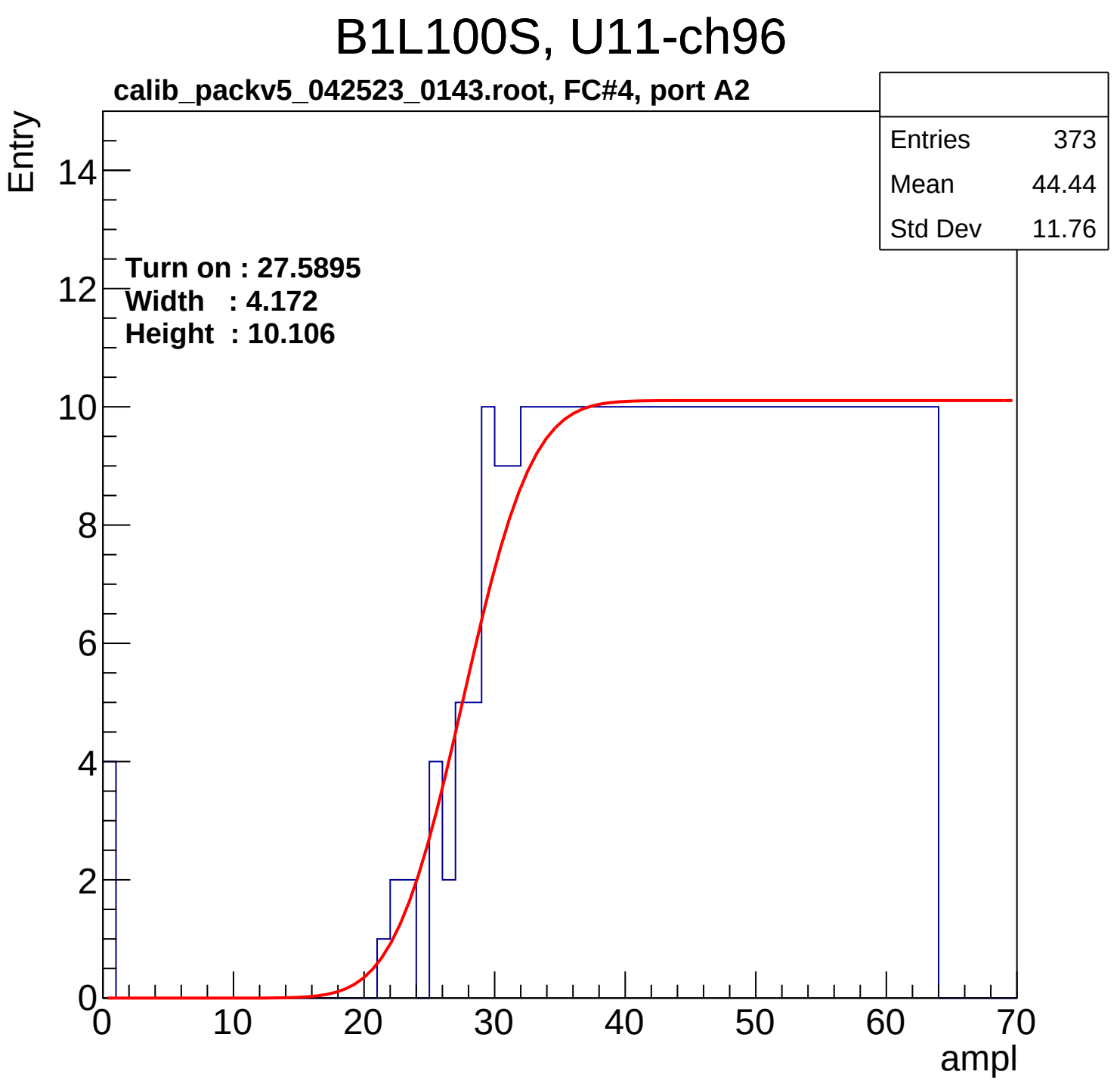
B1L100S, U11-ch96
calib_packv5_042523_0143.root, FC#4, port A2
Entries 373
Mean 44.44
Std Dev 11.76
Turn on : 27.5895
Width : 4.172
Height : 10.106
Entry
ampl
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2
4
6
8
10
12
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0
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60
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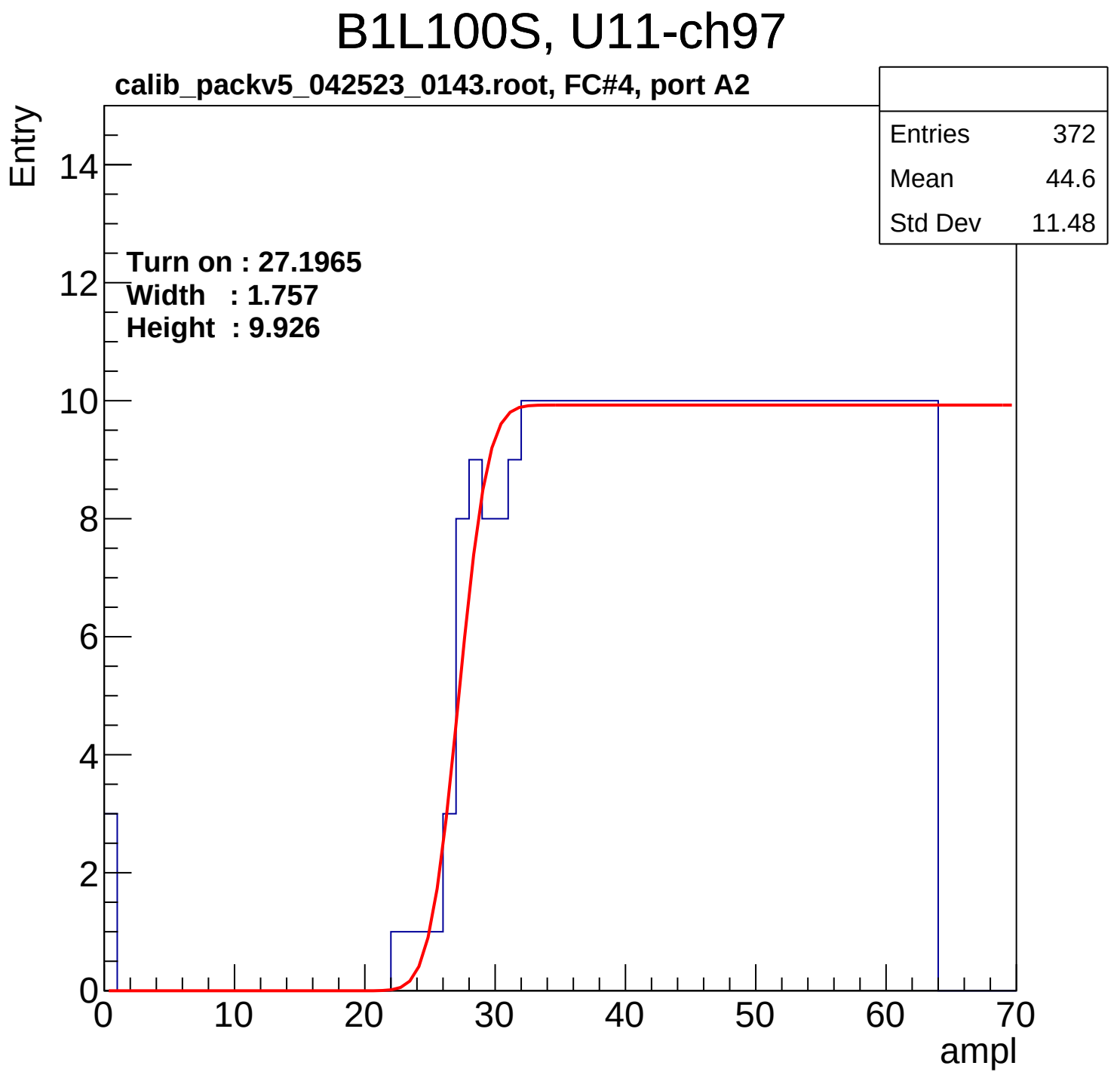
B1L100S, U11-ch97
calib_packv5_042523_0143.root, FC#4, port A2
Entries 372
Mean 44.6
Std Dev 11.48
Turn on : 27.1965
Width : 1.757
Height : 9.926
Entry
ampl
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6
8
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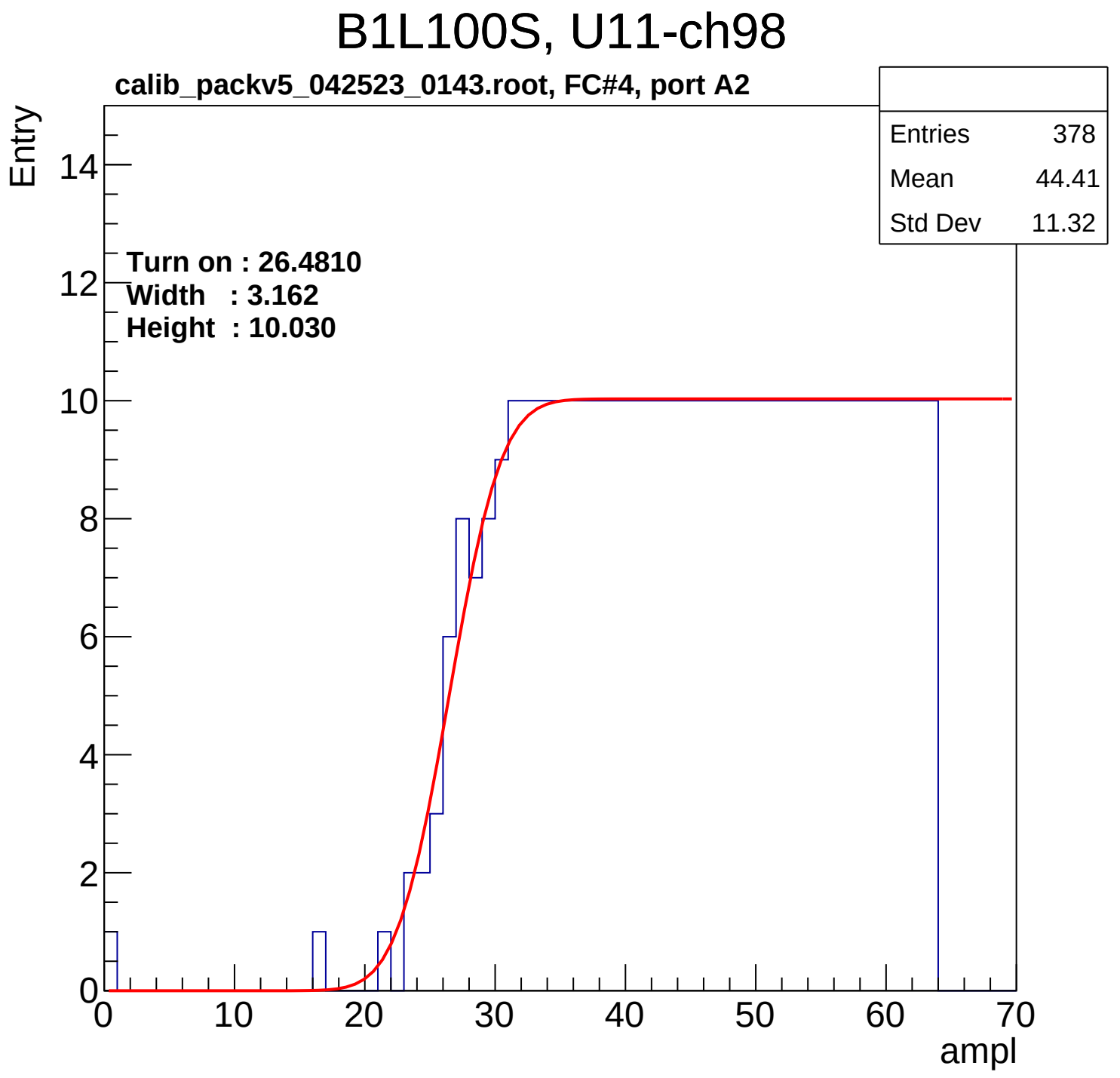
B1L100S, U11-ch98
calib_packv5_042523_0143.root, FC#4, port A2
Entries 378
Mean 44.41
Std Dev 11.32
Turn on : 26.4810
Width : 3.162
Height : 10.030
Entry
ampl
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6
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0
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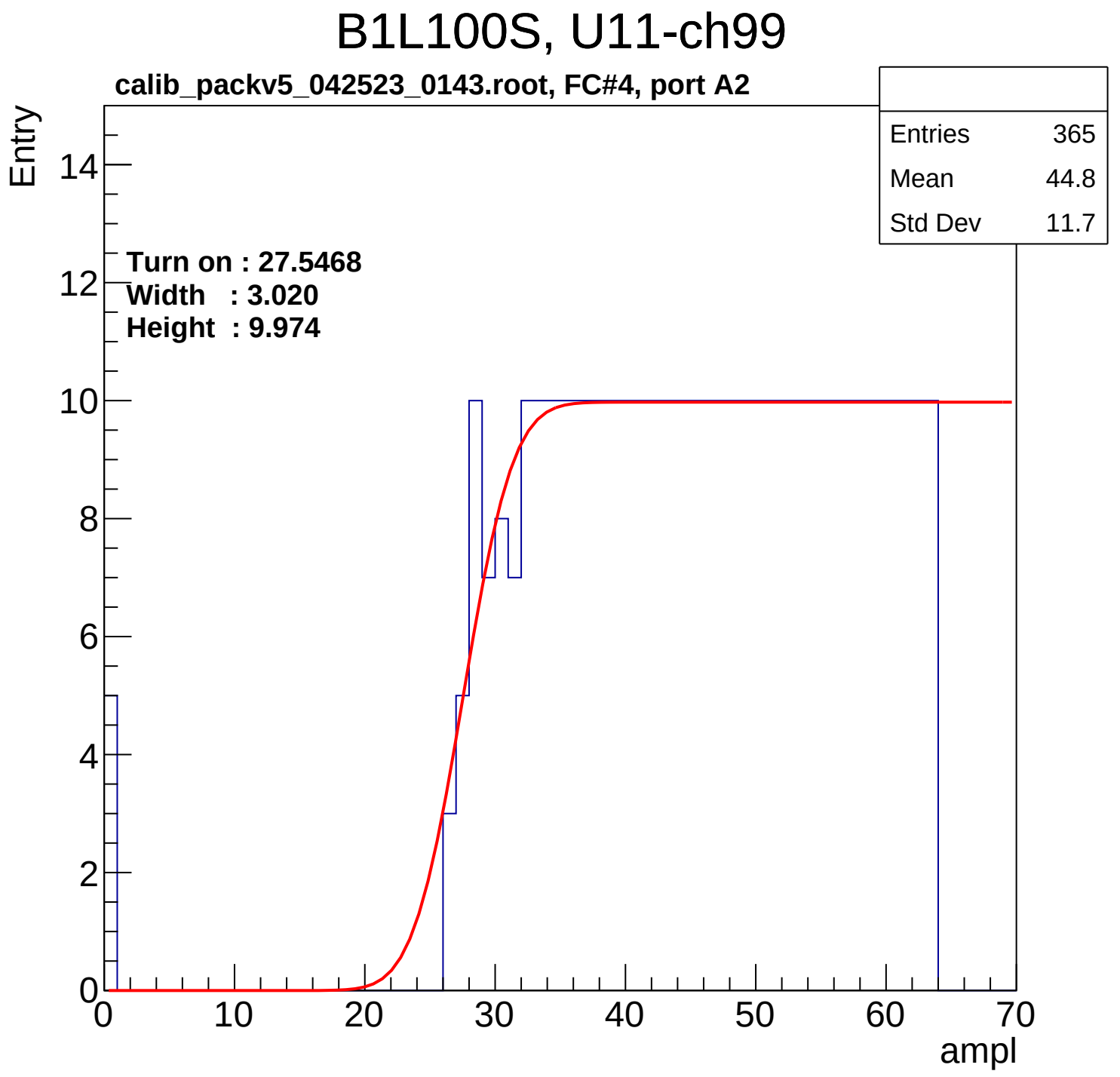
B1L100S, U11-ch99
calib_packv5_042523_0143.root, FC#4, port A2
Entries 365
Mean 44.8
Std Dev 11.7
Turn on : 27.5468
Width : 3.020
Height : 9.974
Entry
ampl
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6
8
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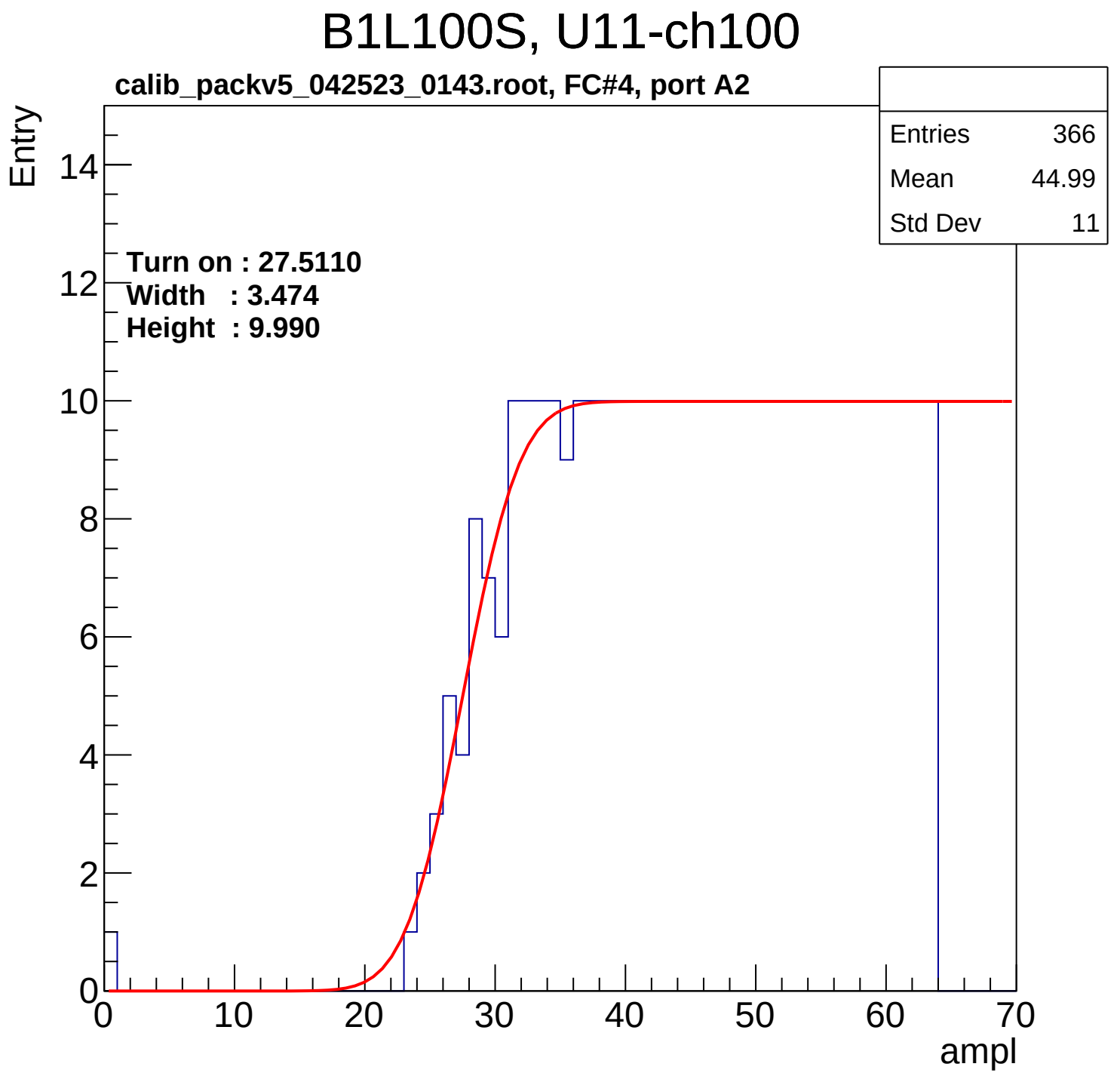
B1L100S, U11-ch100
calib_packv5_042523_0143.root, FC#4, port A2
Entries 366
Mean 44.99
Std Dev 11
Turn on : 27.5110
Width : 3.474
Height : 9.990
Entry
ampl
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6
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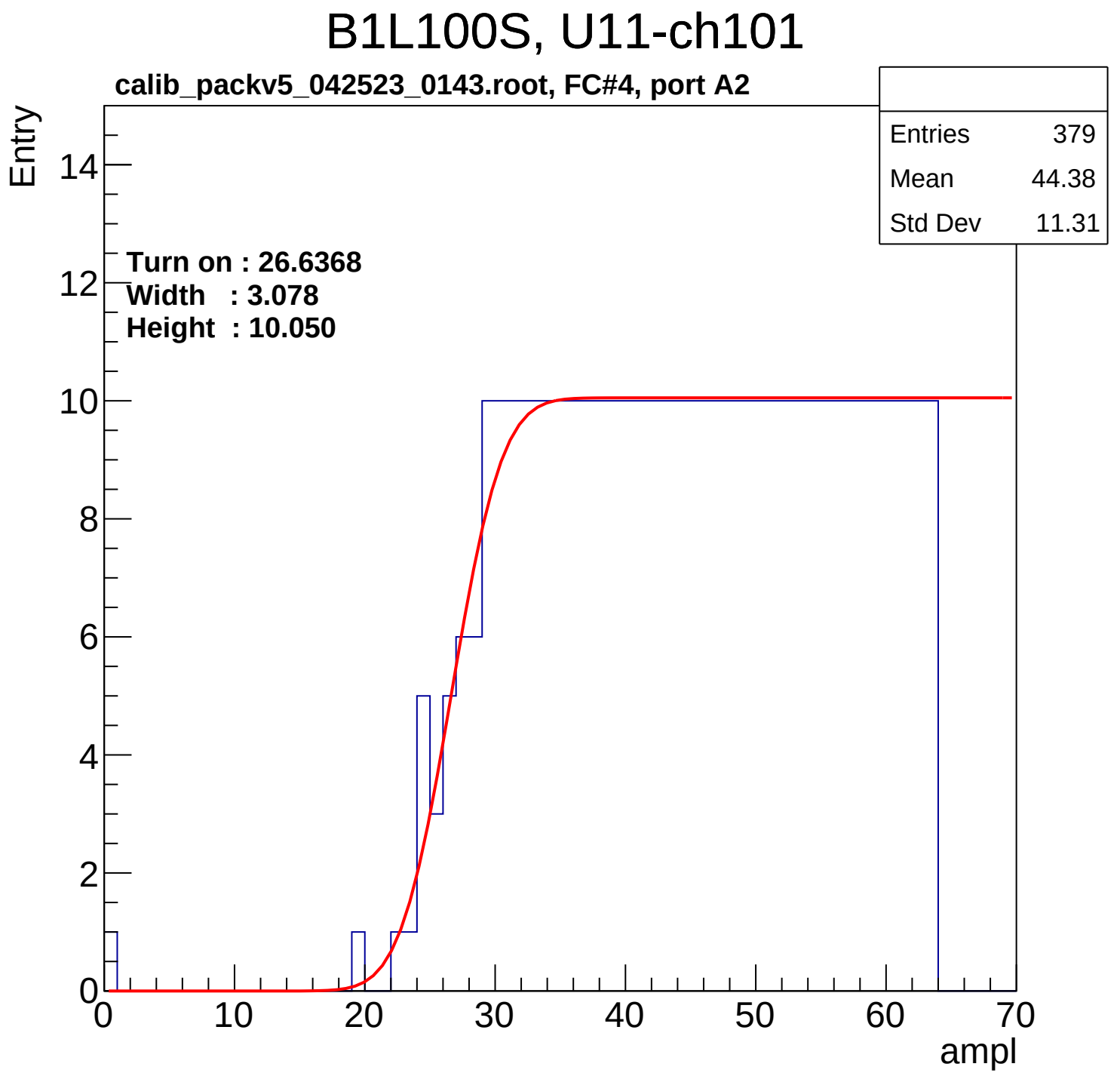
B1L100S, U11-ch101
calib_packv5_042523_0143.root, FC#4, port A2
Entries 379
Mean 44.38
Std Dev 11.31
Turn on : 26.6368
Width : 3.078
Height : 10.050
Entry
ampl
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6
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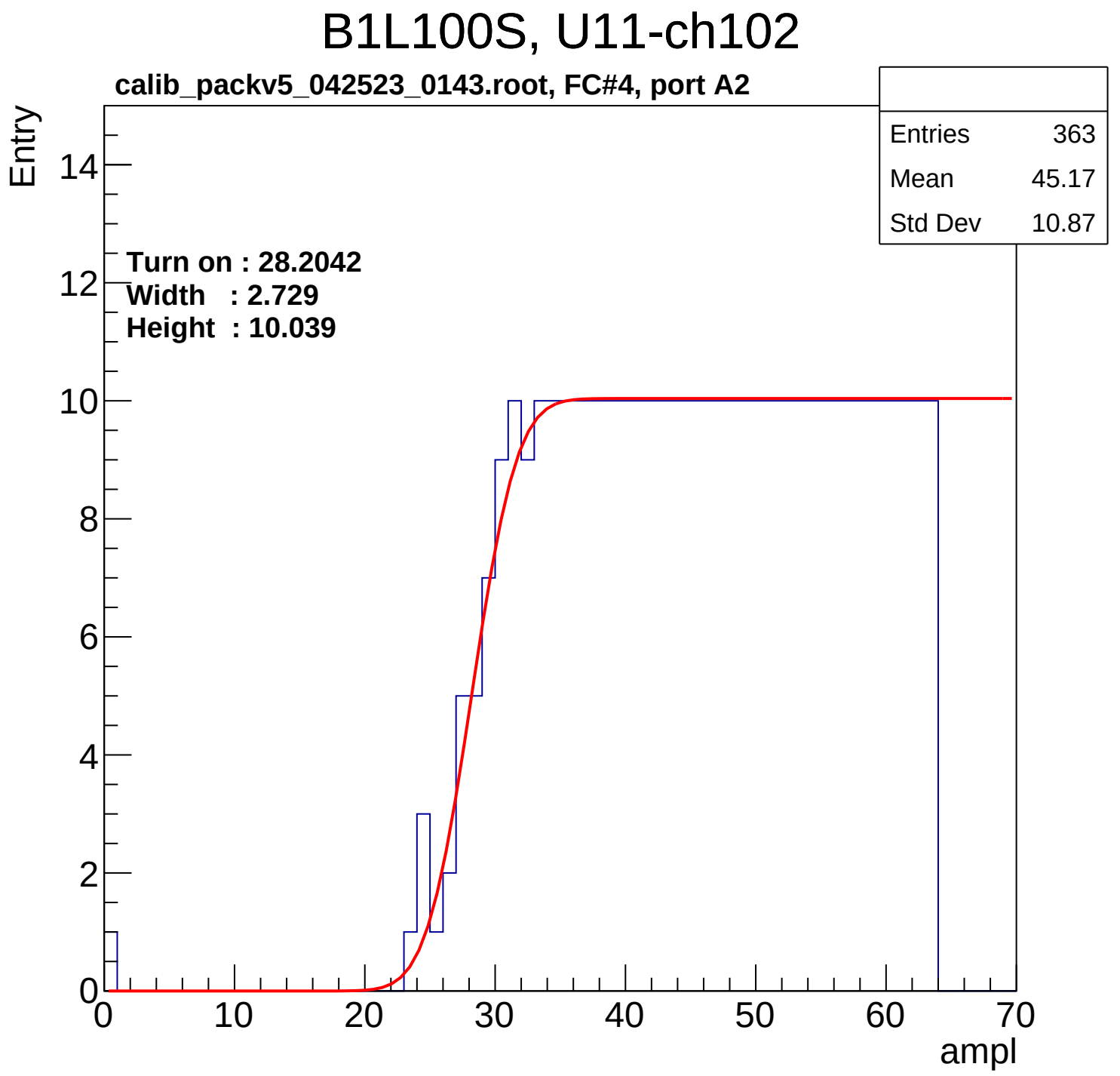
B1L100S, U11-ch102
calib_packv5_042523_0143.root, FC#4, port A2
Entries 363
Mean 45.17
Std Dev 10.87
Turn on : 28.2042
Width : 2.729
Height : 10.039
Entry
ampl
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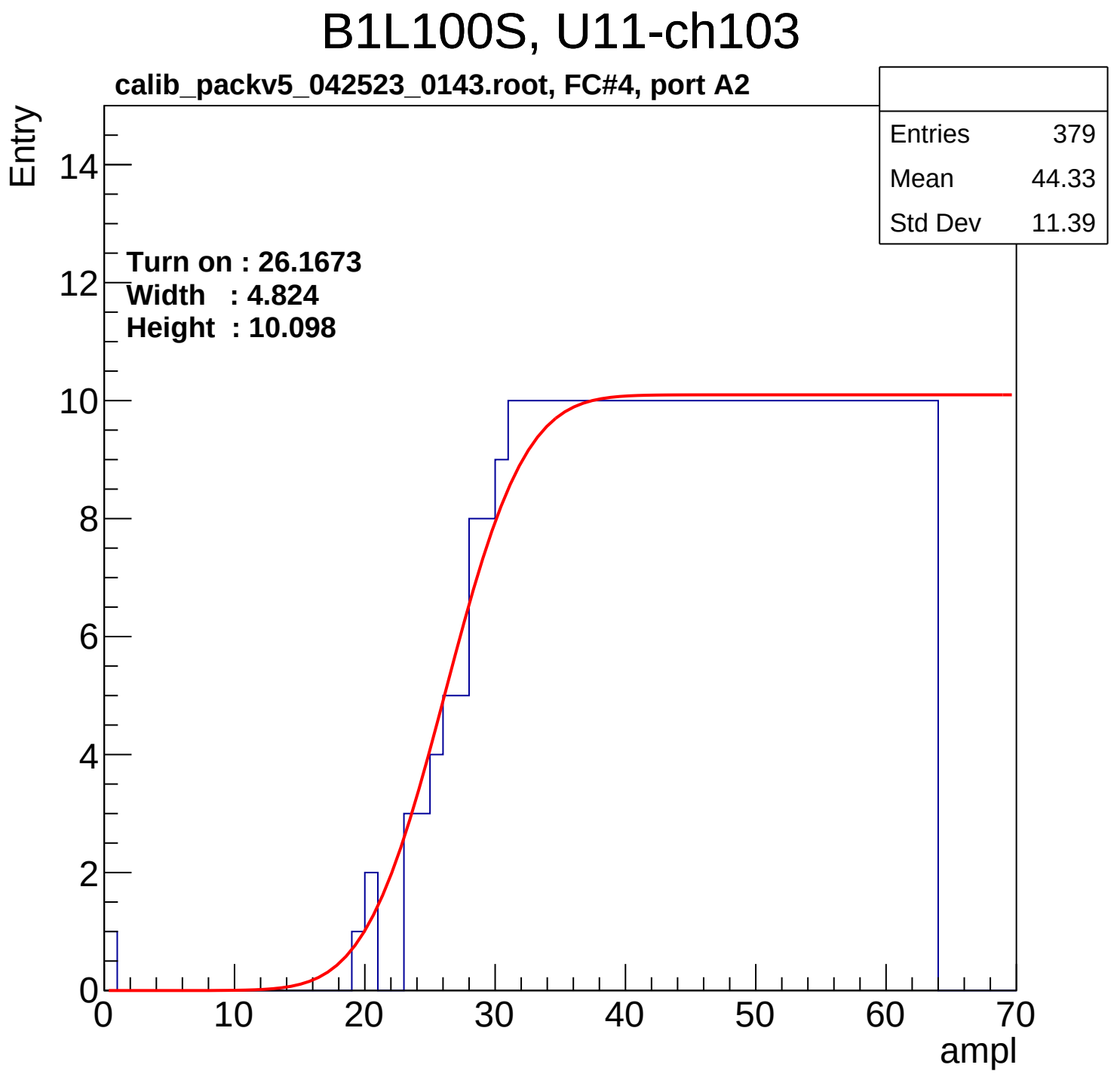
B1L100S, U11-ch103
calib_packv5_042523_0143.root, FC#4, port A2
Entries 379
Mean 44.33
Std Dev 11.39
Turn on : 26.1673
Width : 4.824
Height : 10.098
Entry
ampl
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6
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10
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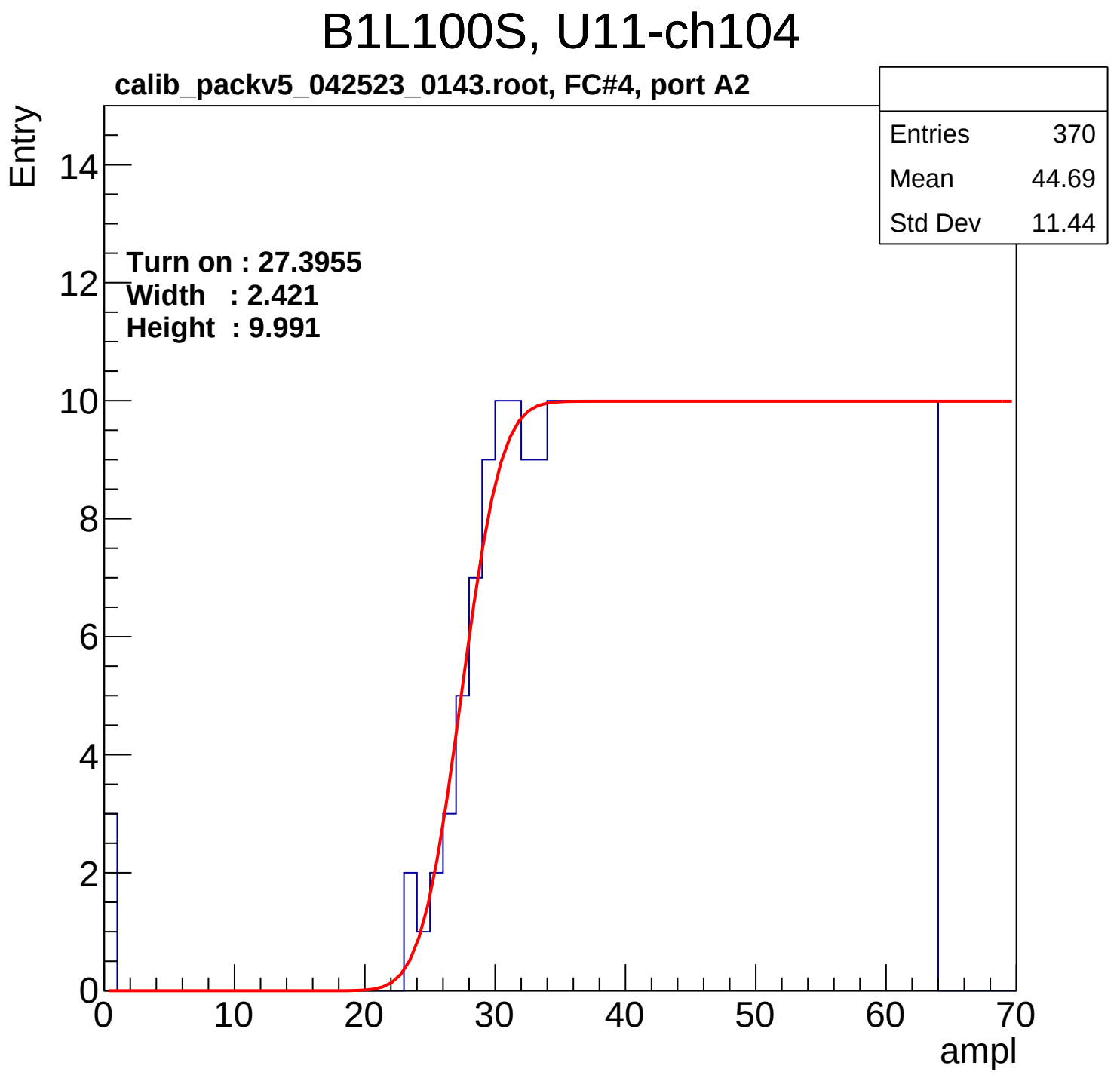
B1L100S, U11-ch104
calib_packv5_042523_0143.root, FC#4, port A2
Entries 370
Mean 44.69
Std Dev 11.44
Turn on : 27.3955
Width : 2.421
Height : 9.991
Entry
ampl
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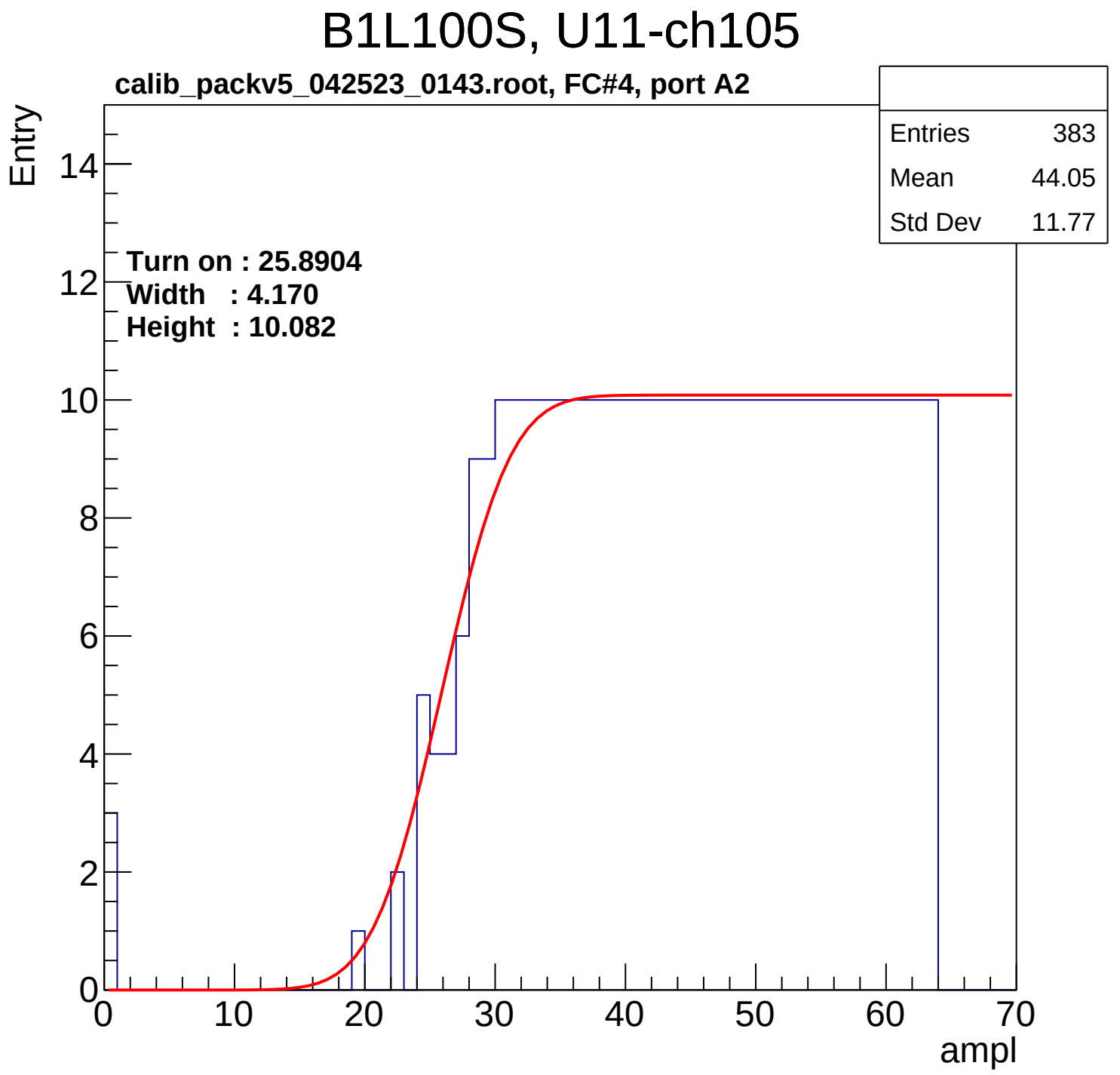
B1L100S, U11-ch105
calib_packv5_042523_0143.root, FC#4, port A2
Entries 383
Mean 44.05
Std Dev 11.77
Turn on : 25.8904
Width : 4.170
Height : 10.082
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ampl
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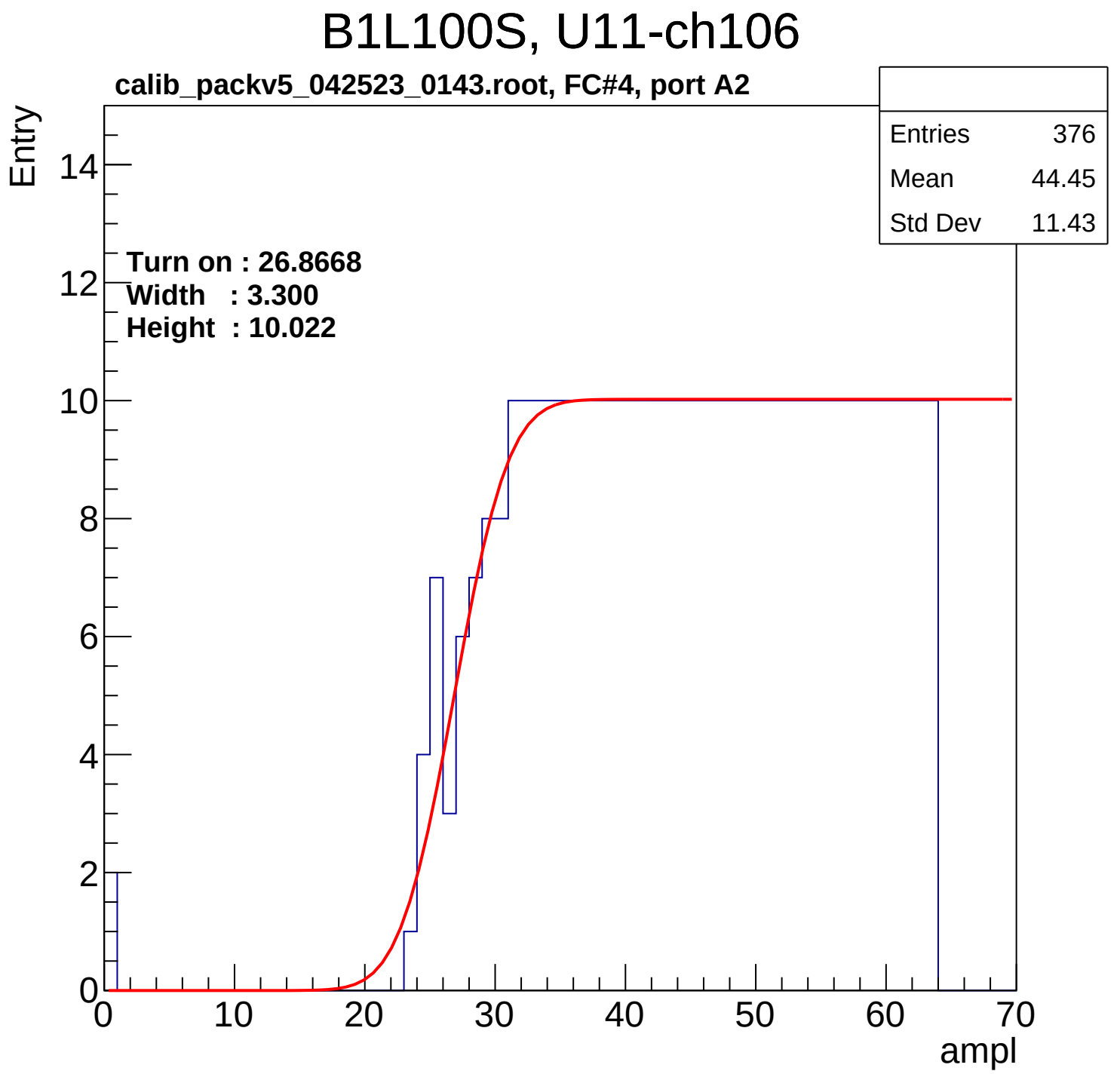
B1L100S, U11-ch106
calib_packv5_042523_0143.root, FC#4, port A2
Entries 376
Mean 44.45
Std Dev 11.43
Turn on : 26.8668
Width : 3.300
Height : 10.022
Entry
ampl
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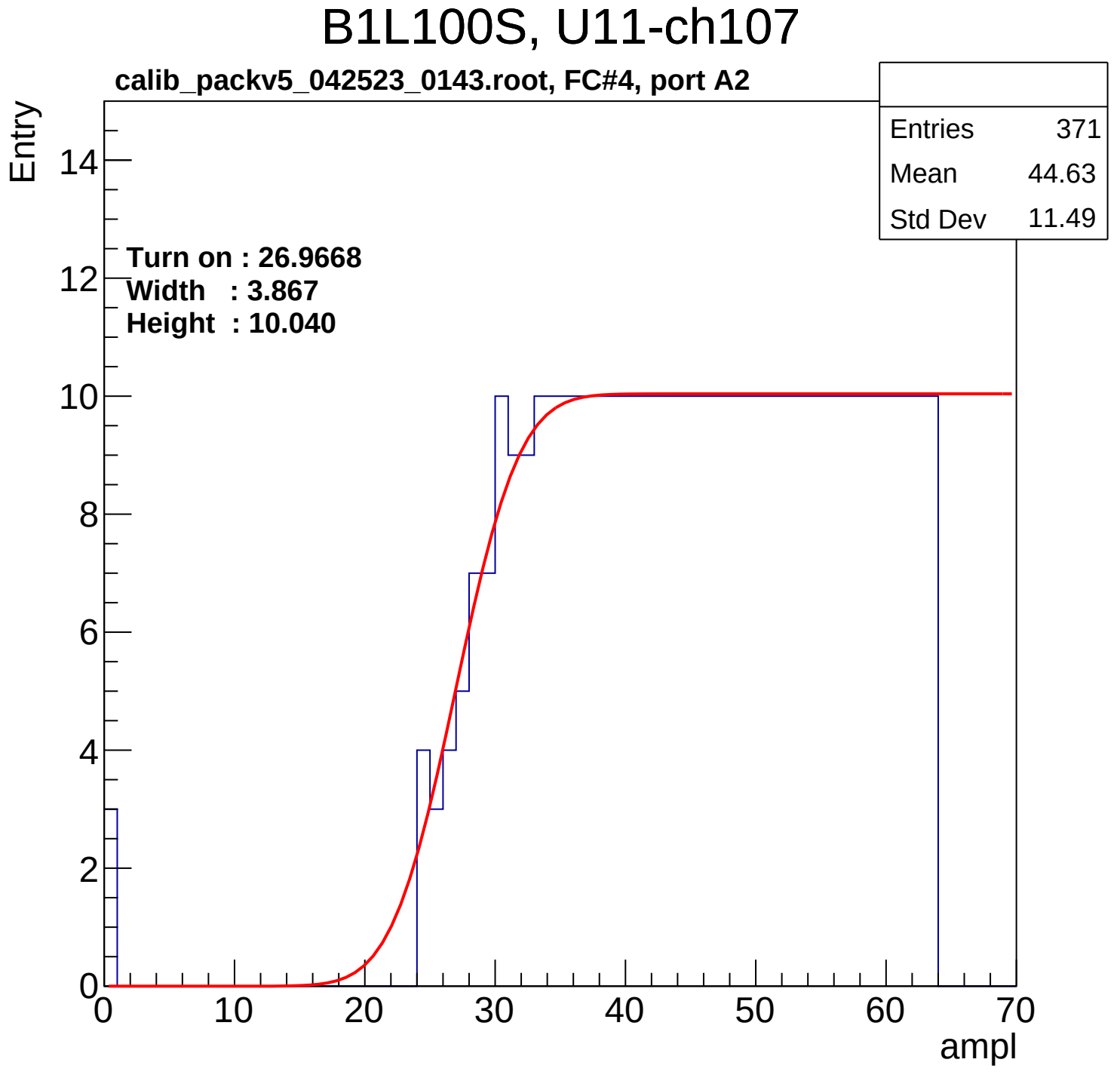
B1L100S, U11-ch107
calib_packv5_042523_0143.root, FC#4, port A2
Entries 371
Mean 44.63
Std Dev 11.49
Turn on : 26.9668
Width : 3.867
Height : 10.040
Entry
ampl
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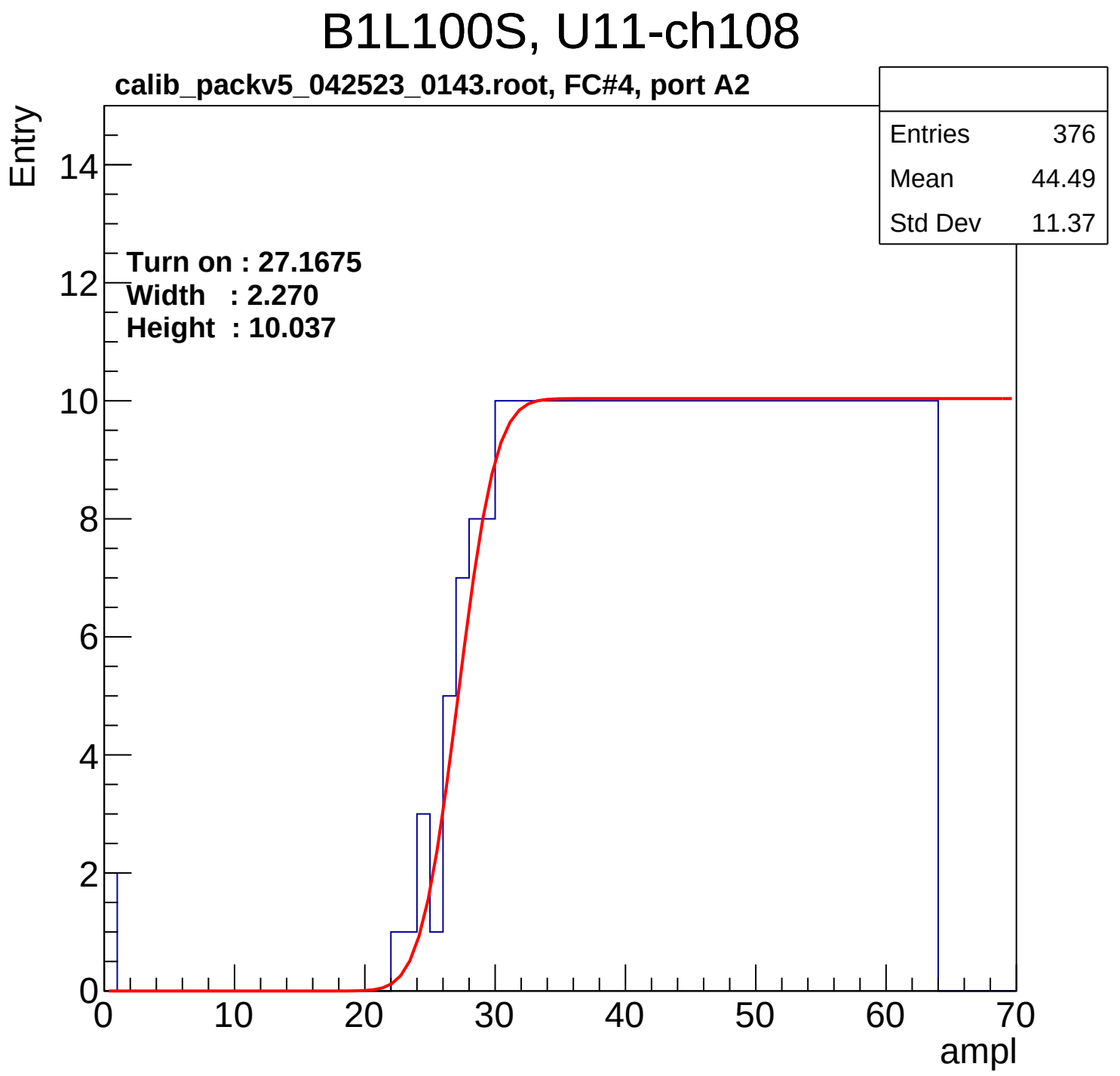
B1L100S, U11-ch108
calib_packv5_042523_0143.root, FC#4, port A2
Entries 376
Mean 44.49
Std Dev 11.37
Turn on : 27.1675
Width : 2.270
Height : 10.037
Entry
ampl
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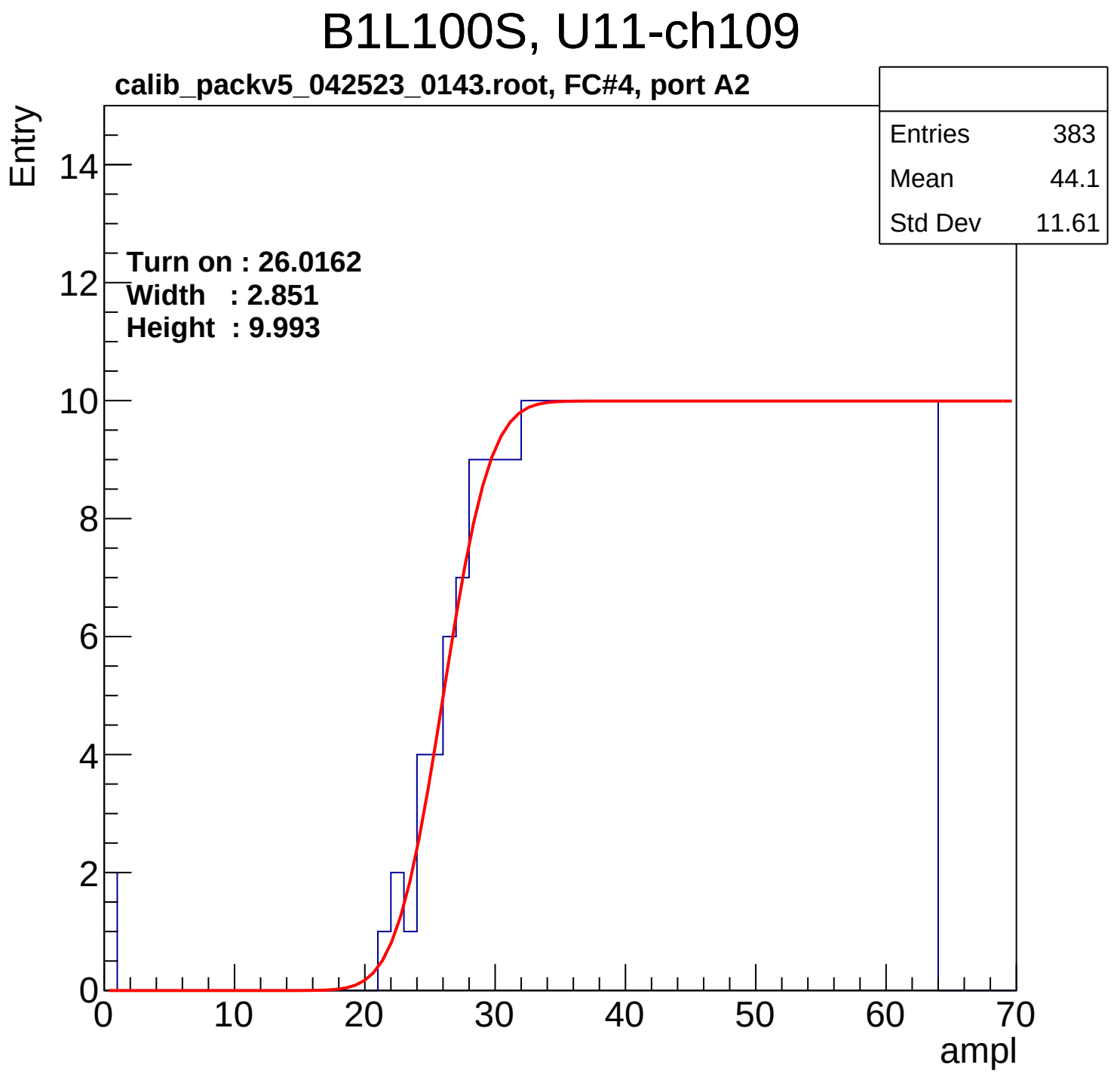
B1L100S, U11-ch109
calib_packv5_042523_0143.root, FC#4, port A2
Entries 383
Mean 44.1
Std Dev 11.61
Turn on : 26.0162
Width : 2.851
Height : 9.993
Entry
ampl
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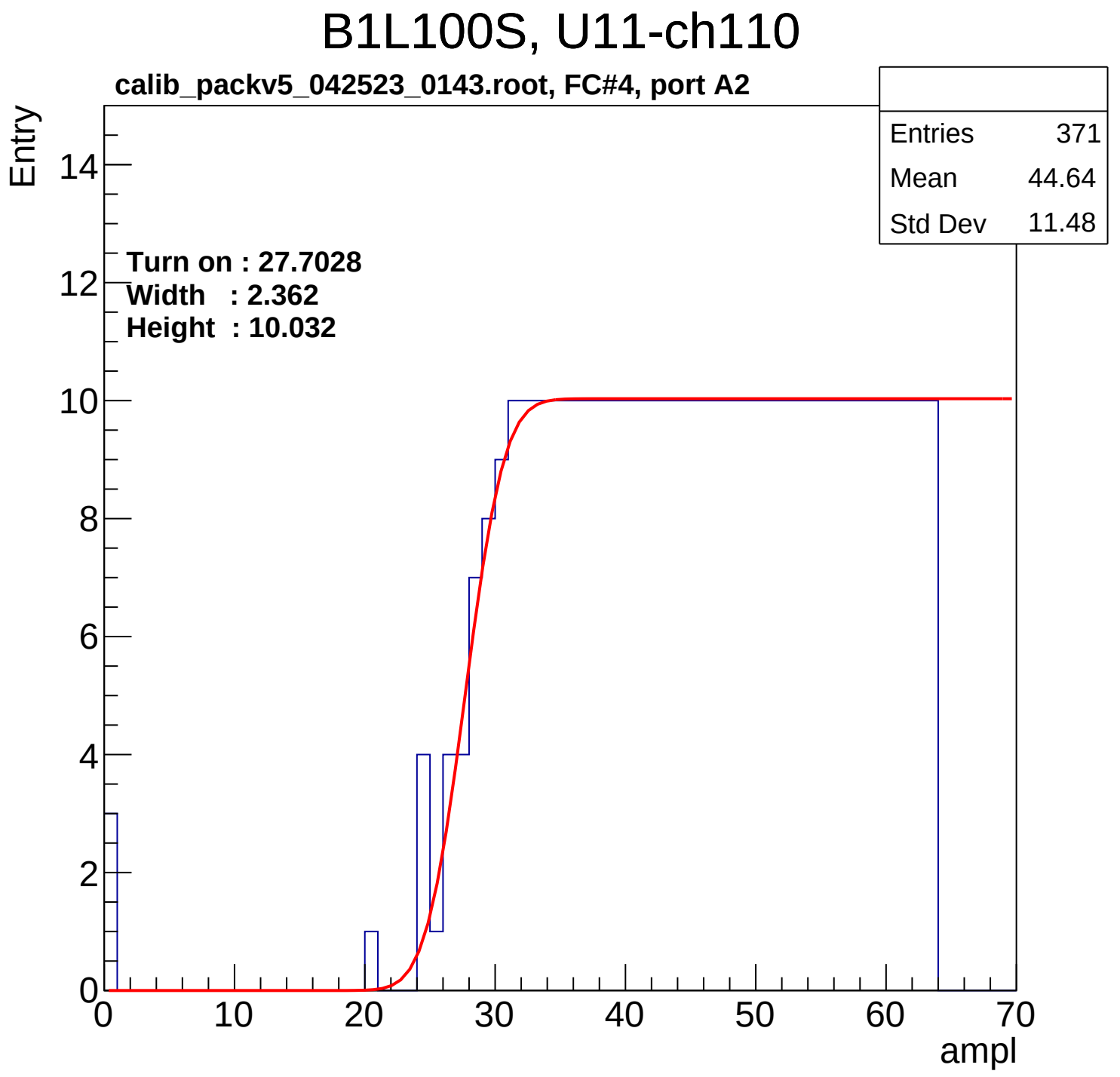
B1L100S, U11-ch110
calib_packv5_042523_0143.root, FC#4, port A2
Entries 371
Mean 44.64
Std Dev 11.48
Turn on : 27.7028
Width : 2.362
Height : 10.032
Entry
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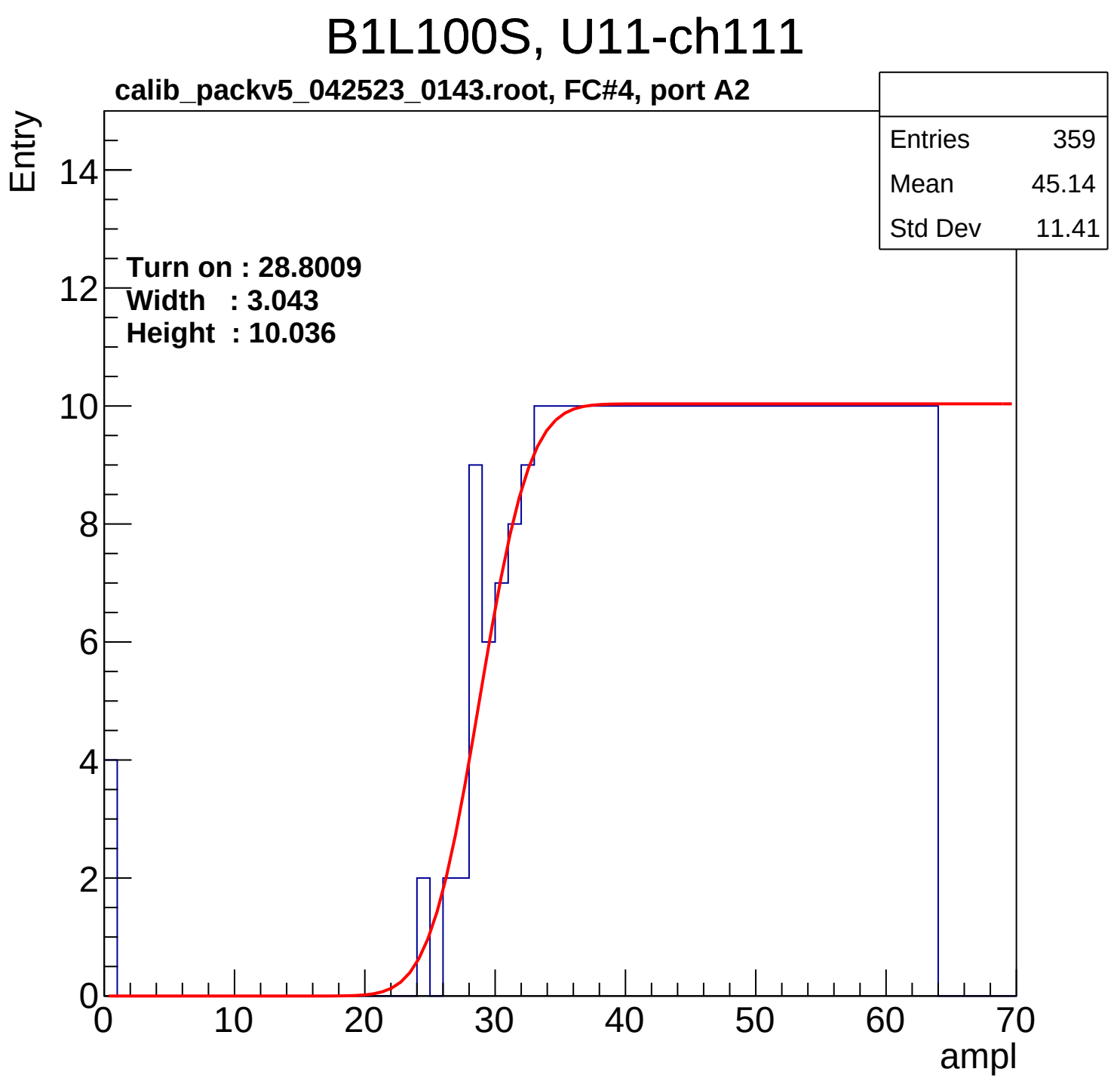
B1L100S, U11-ch111
calib_packv5_042523_0143.root, FC#4, port A2
Entries 359
Mean 45.14
Std Dev 11.41
Turn on : 28.8009
Width : 3.043
Height : 10.036
Entry
ampl
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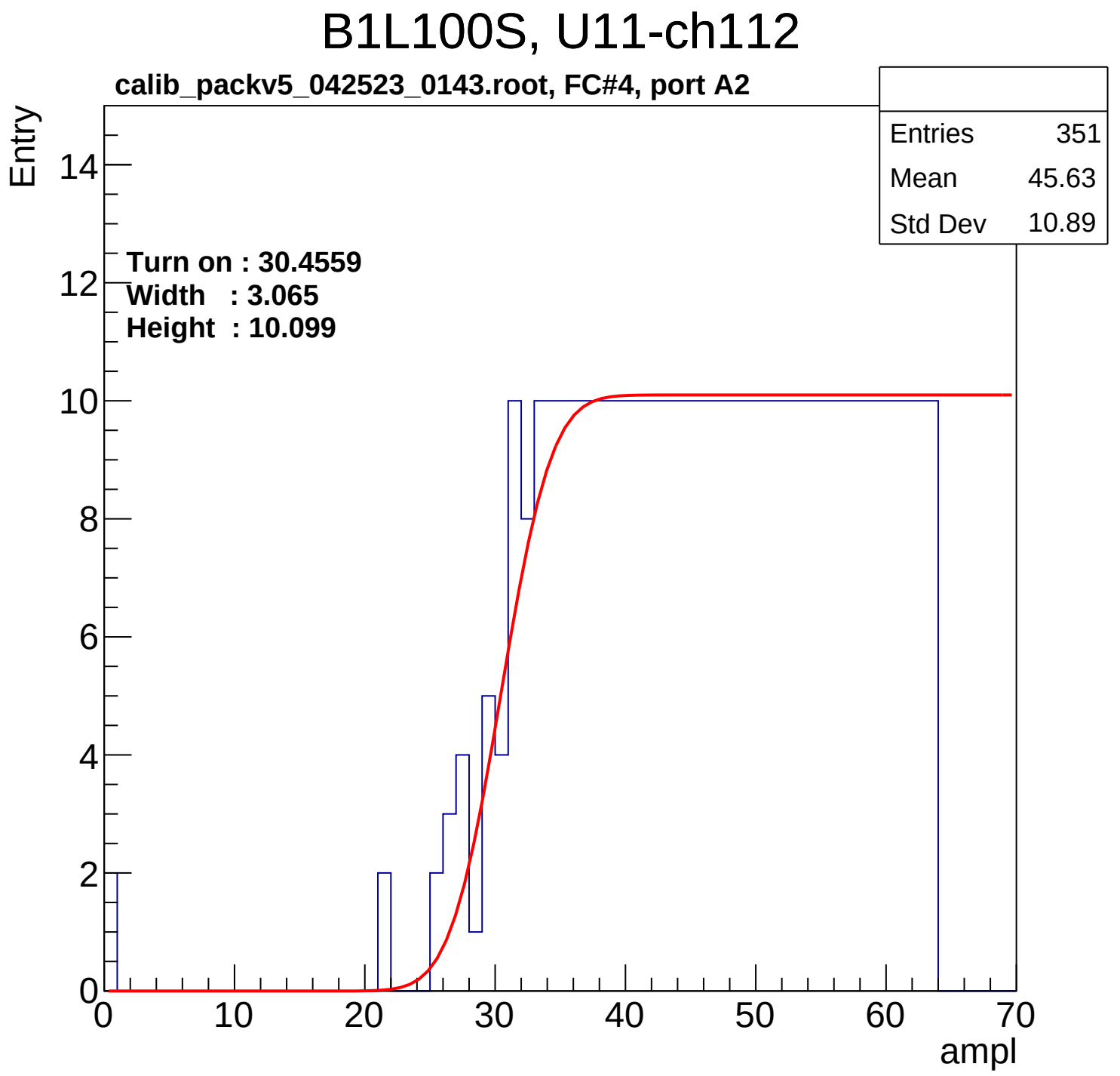
B1L100S, U11-ch112
calib_packv5_042523_0143.root, FC#4, port A2
Entries 351
Mean 45.63
Std Dev 10.89
Turn on : 30.4559
Width : 3.065
Height : 10.099
Entry
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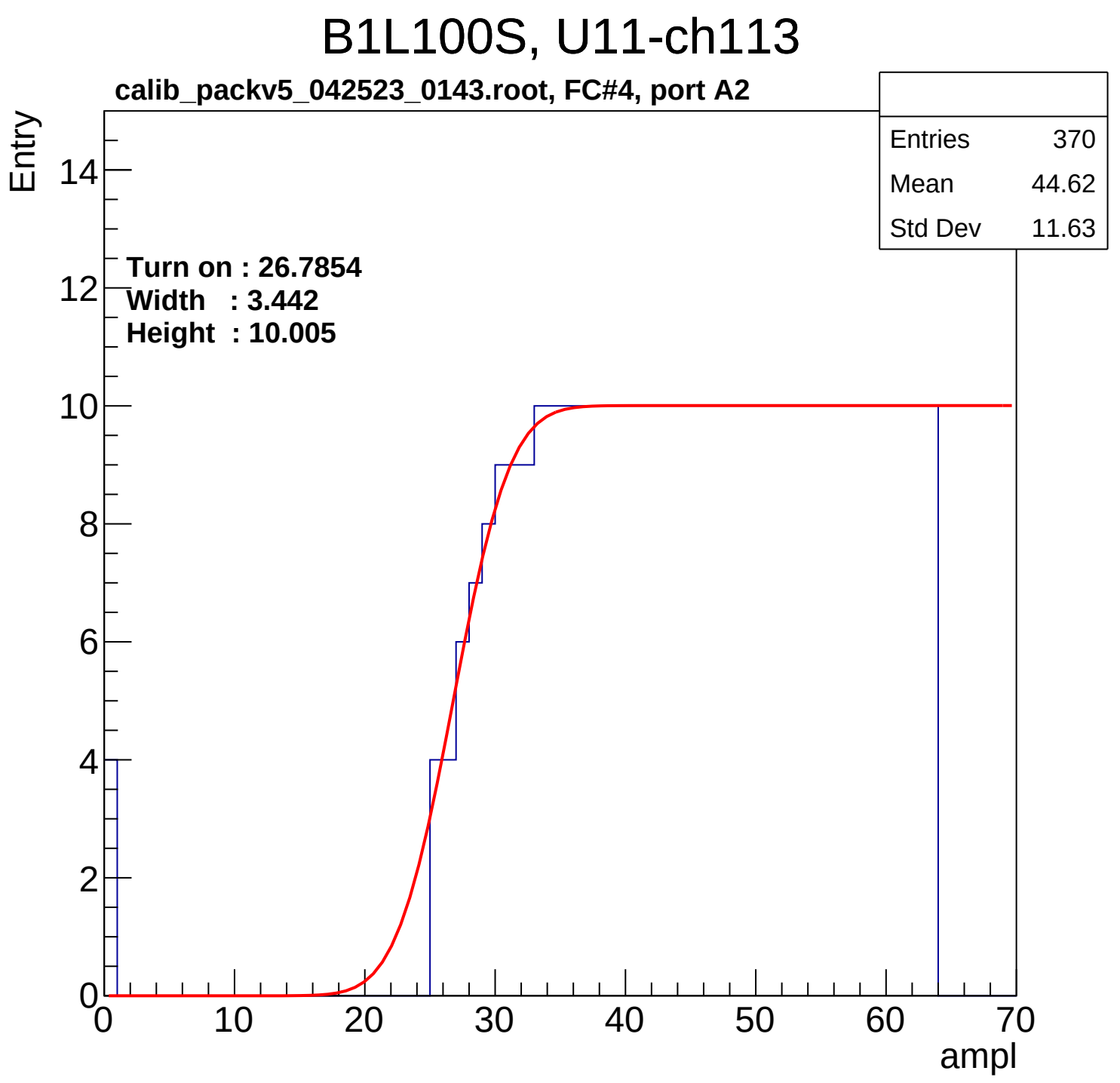
B1L100S, U11-ch113
calib_packv5_042523_0143.root, FC#4, port A2
Entries 370
Mean 44.62
Std Dev 11.63
Turn on : 26.7854
Width : 3.442
Height : 10.005
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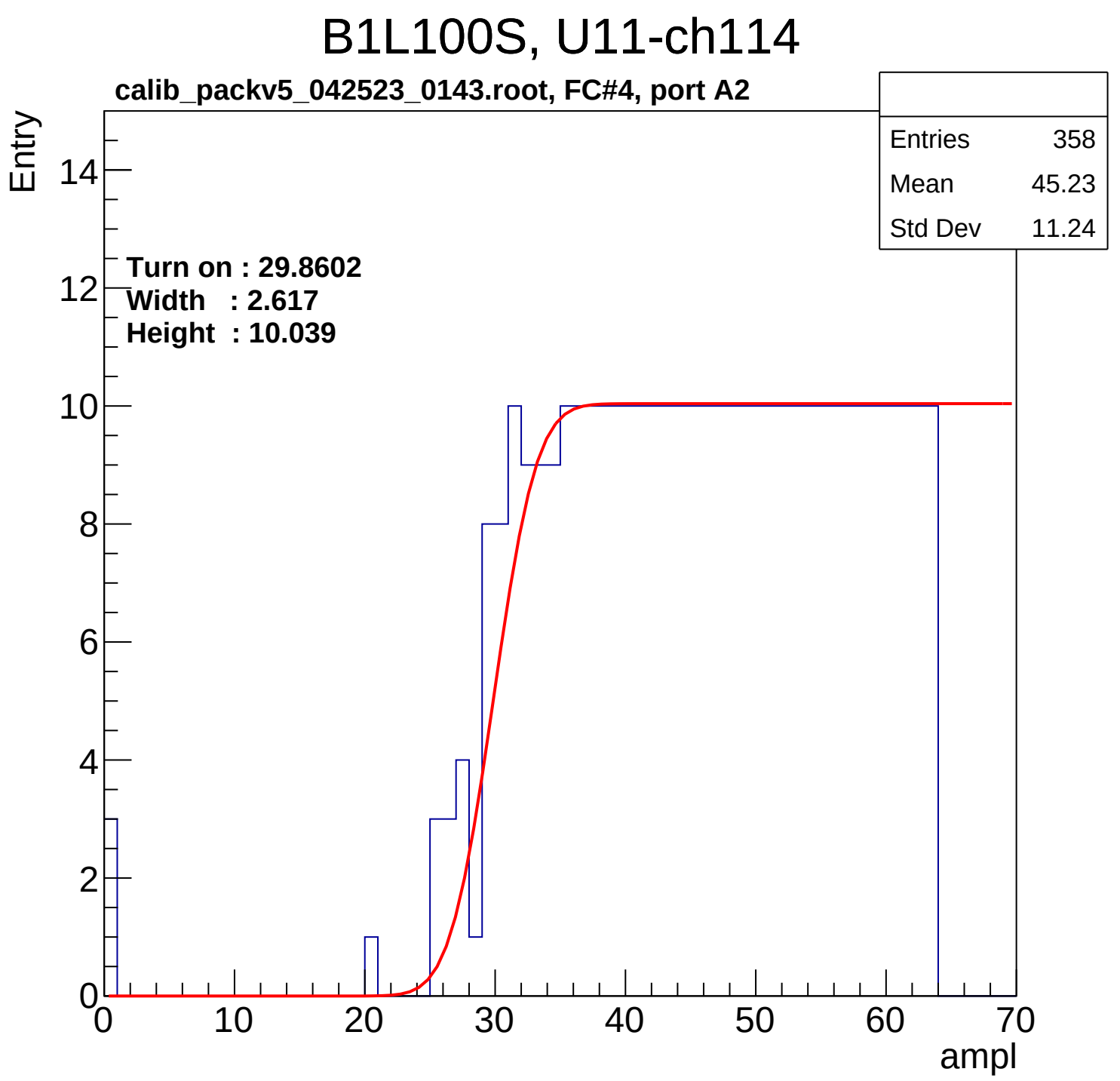
B1L100S, U11-ch114
calib_packv5_042523_0143.root, FC#4, port A2
Entries 358
Mean 45.23
Std Dev 11.24
Turn on : 29.8602
Width : 2.617
Height : 10.039
Entry
ampl
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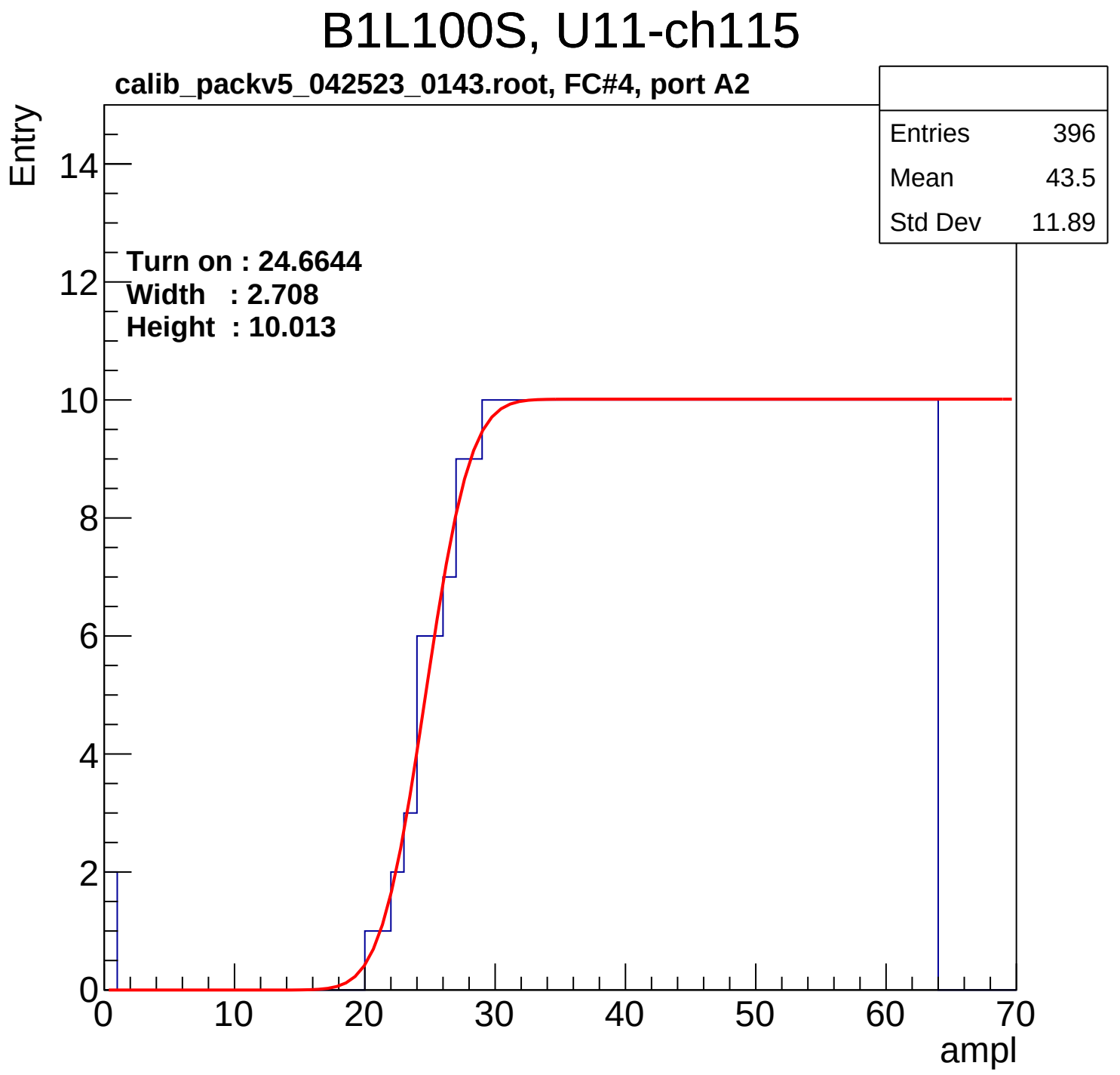
B1L100S, U11-ch115
calib_packv5_042523_0143.root, FC#4, port A2
Entries 396
Mean 43.5
Std Dev 11.89
Turn on : 24.6644
Width : 2.708
Height : 10.013
Entry
ampl
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4
6
8
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12
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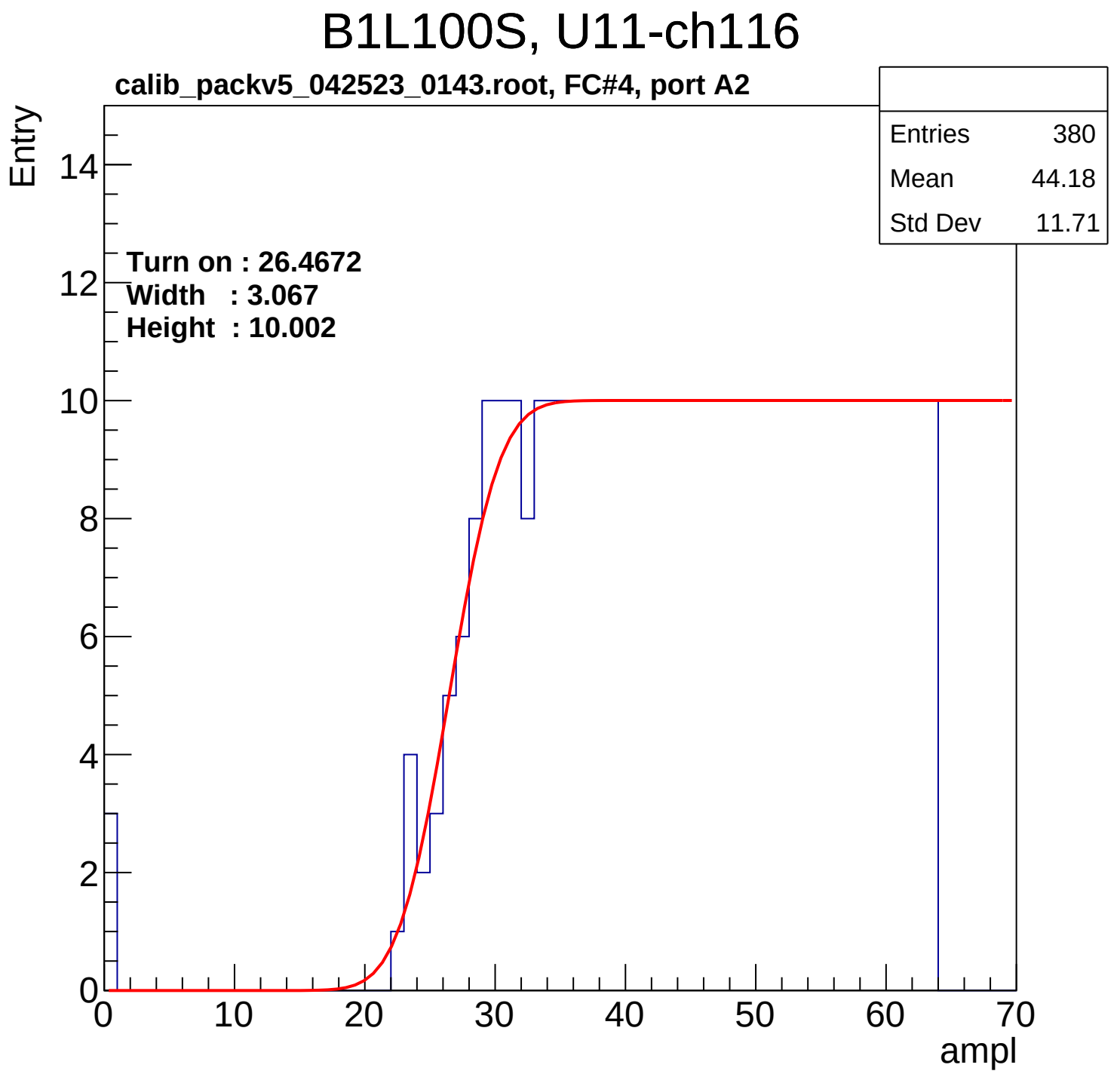
B1L100S, U11-ch116
calib_packv5_042523_0143.root, FC#4, port A2
Entries 380
Mean 44.18
Std Dev 11.71
Turn on : 26.4672
Width : 3.067
Height : 10.002
Entry
ampl
0
2
4
6
8
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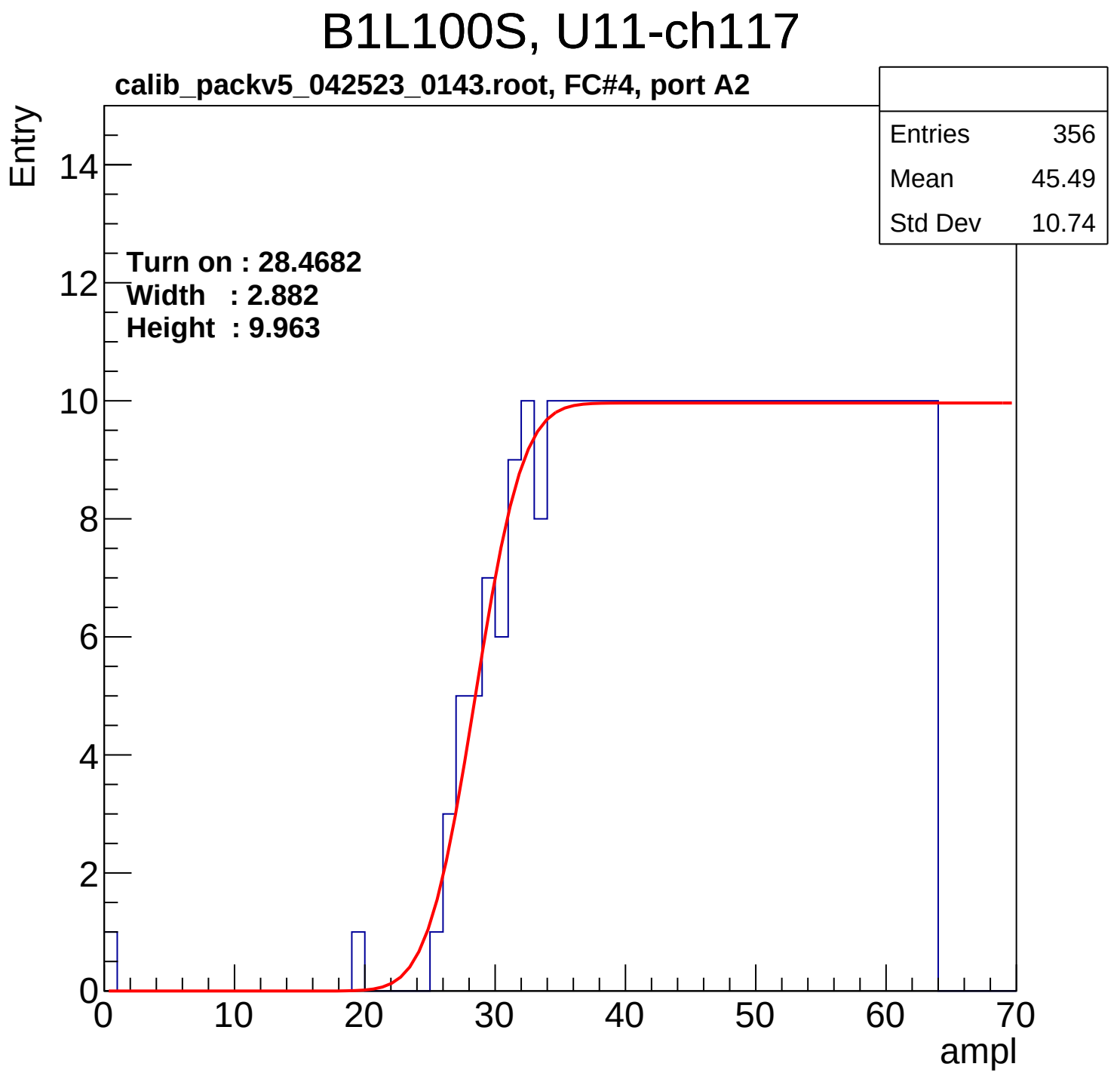
B1L100S, U11-ch117
calib_packv5_042523_0143.root, FC#4, port A2
Entries 356
Mean 45.49
Std Dev 10.74
Turn on : 28.4682
Width : 2.882
Height : 9.963
Entry
ampl
0
2
4
6
8
10
12
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0
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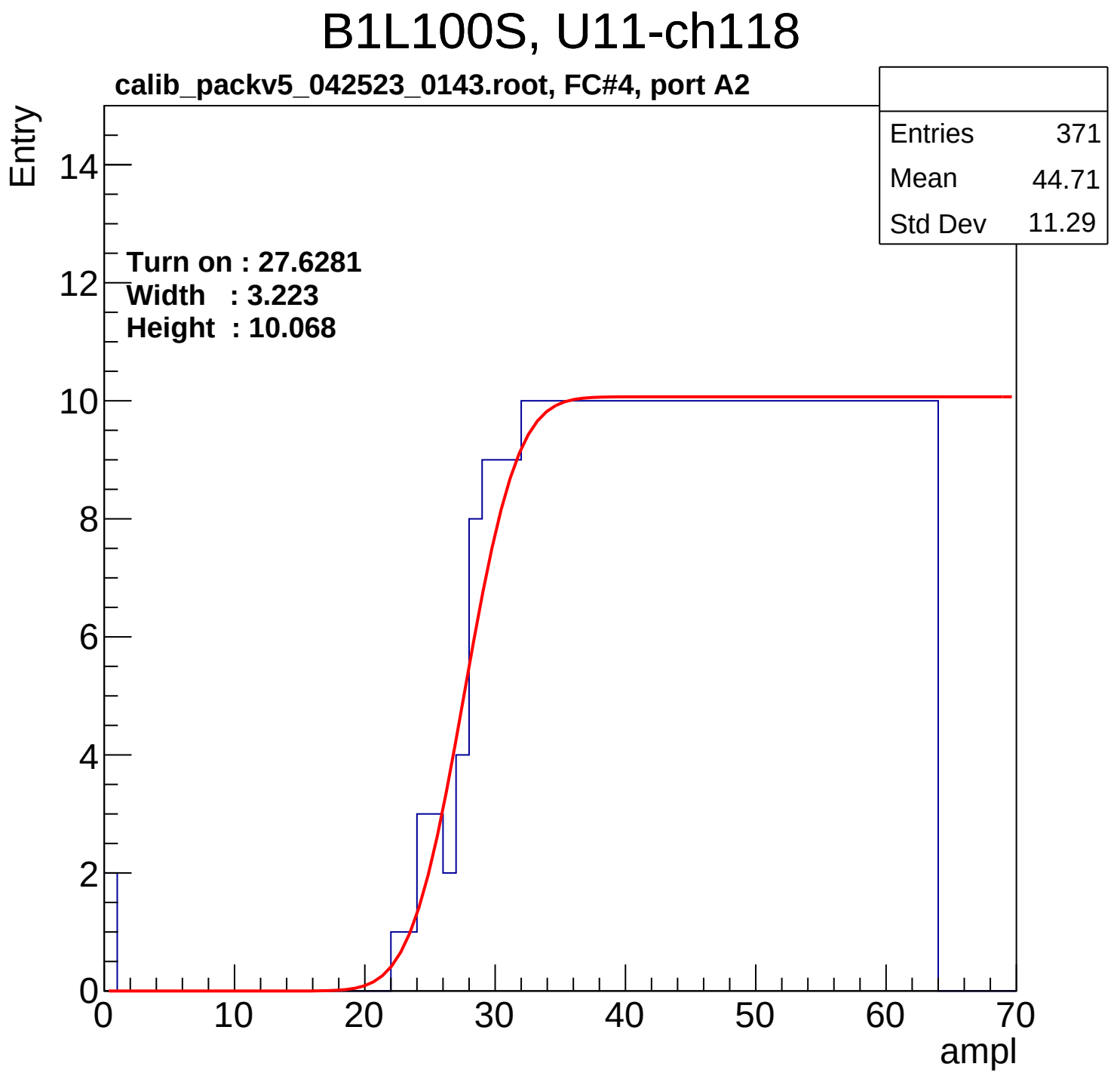
B1L100S, U11-ch118
calib_packv5_042523_0143.root, FC#4, port A2
Entries 371
Mean 44.71
Std Dev 11.29
Turn on : 27.6281
Width : 3.223
Height : 10.068
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
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60
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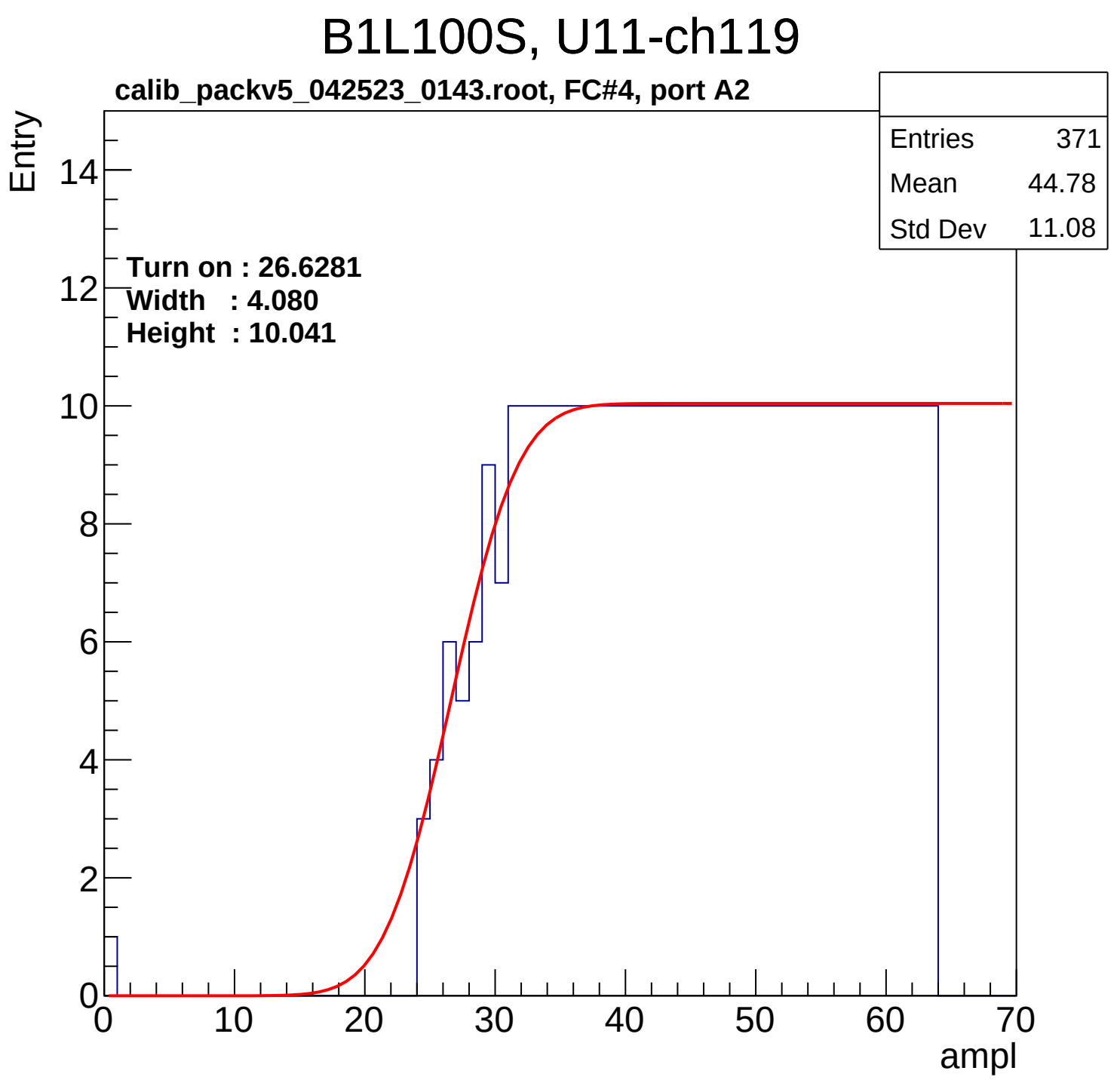
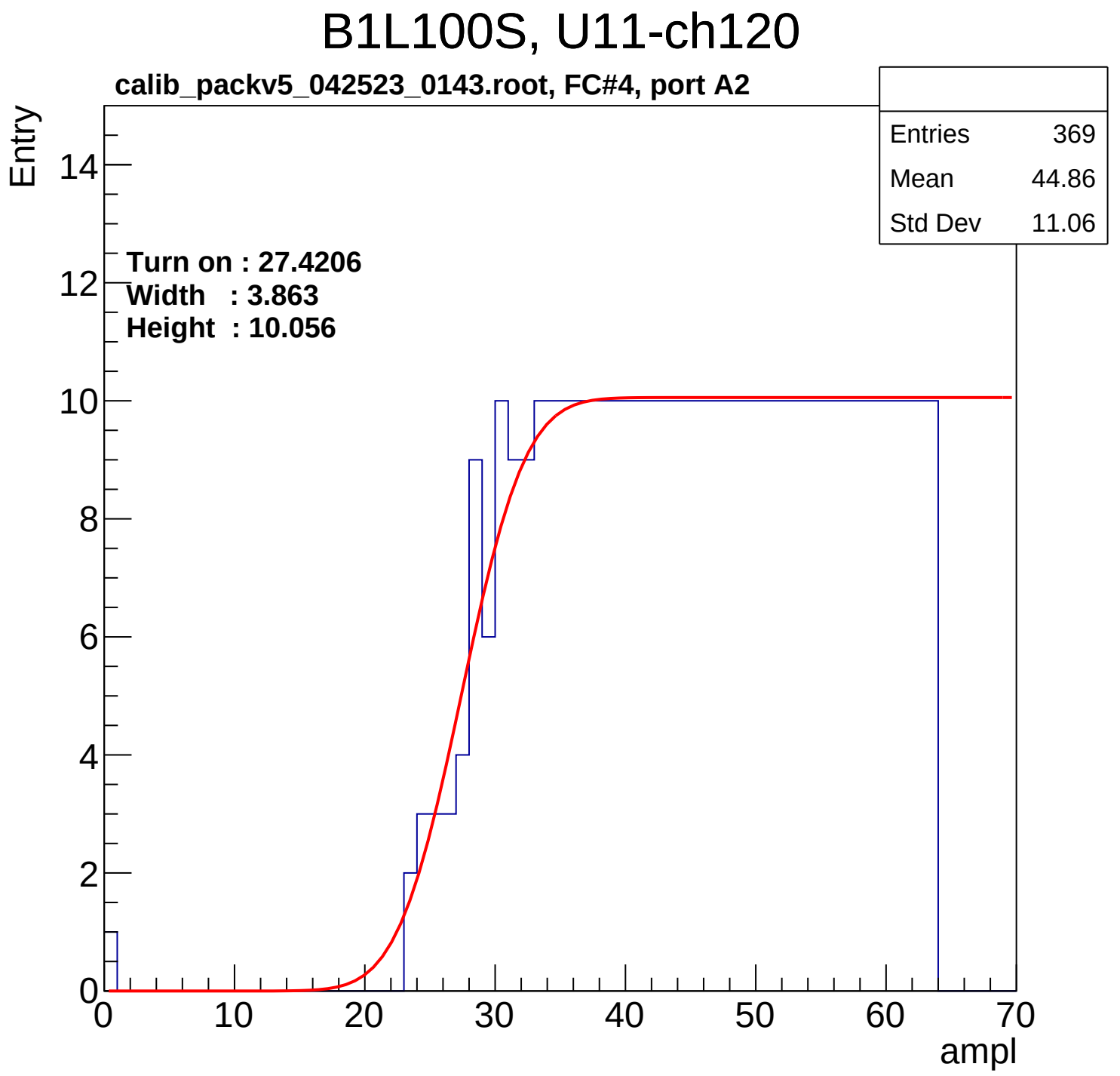
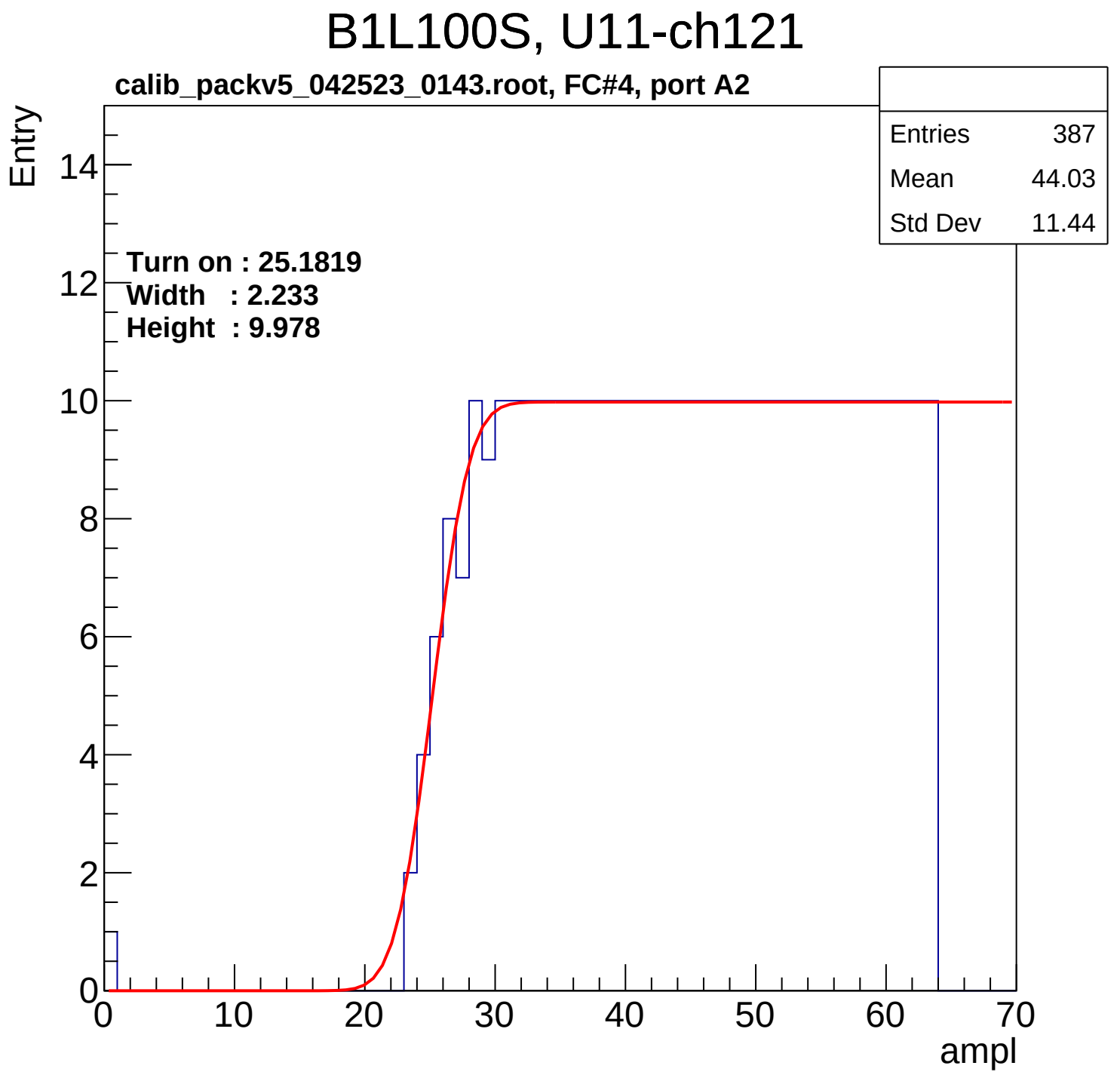
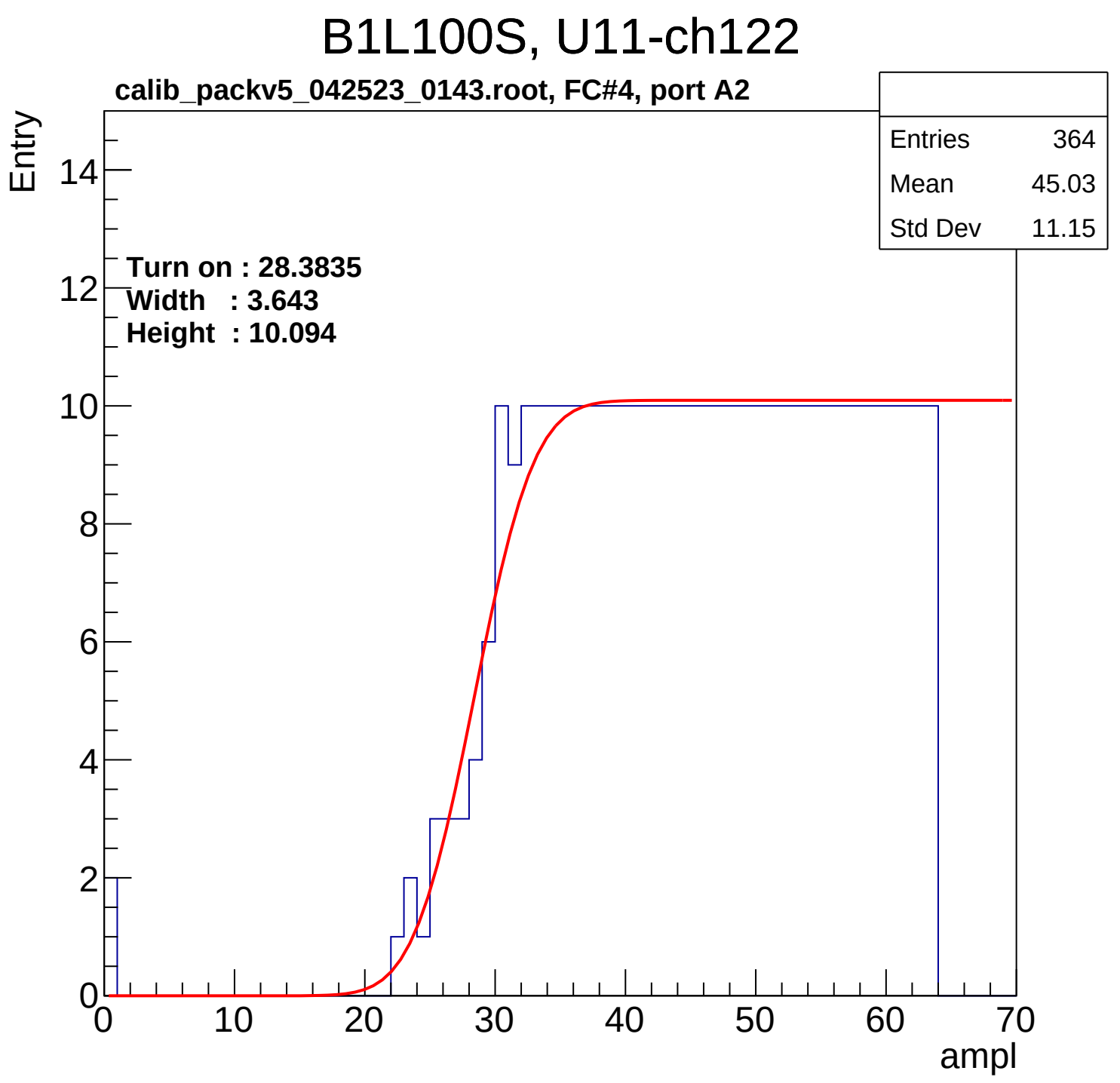
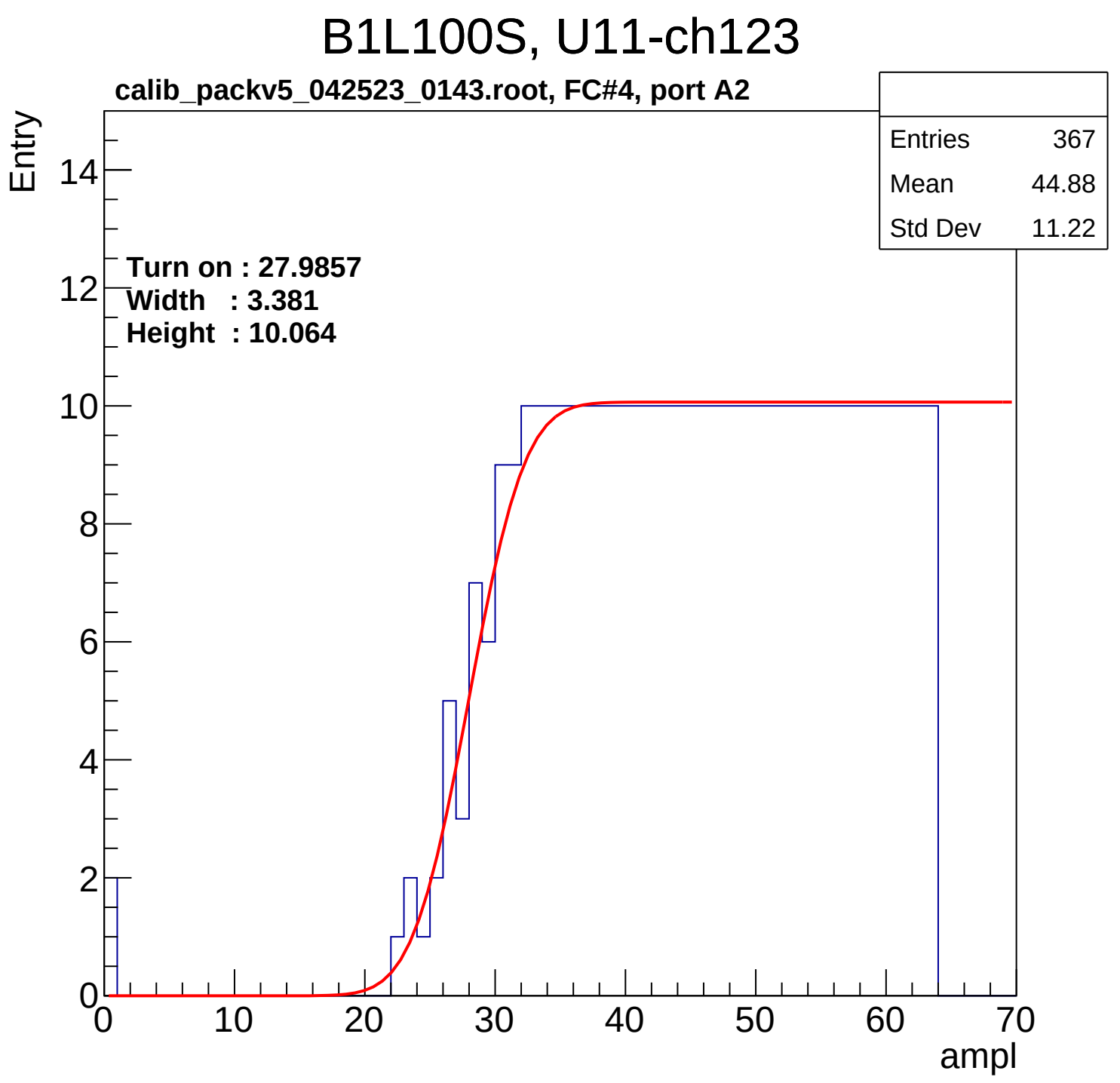

B1L100S, U11-ch119
calib_packv5_042523_0143.root, FC#4, port A2
Entries 371
Mean 44.78
Std Dev 11.08
Turn on : 26.6281
Width : 4.080
Height : 10.041
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L100S, U11-ch120
calib_packv5_042523_0143.root, FC#4, port A2
Entries 369
Mean 44.86
Std Dev 11.06
Turn on : 27.4206
Width : 3.863
Height : 10.056
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L100S, U11-ch121
calib_packv5_042523_0143.root, FC#4, port A2
Entries 387
Mean 44.03
Std Dev 11.44
Turn on : 25.1819
Width : 2.233
Height : 9.978
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L100S, U11-ch122
calib_packv5_042523_0143.root, FC#4, port A2
Entries 364
Mean 45.03
Std Dev 11.15
Turn on : 28.3835
Width : 3.643
Height : 10.094
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L100S, U11-ch123
calib_packv5_042523_0143.root, FC#4, port A2
Entries 367
Mean 44.88
Std Dev 11.22
Turn on : 27.9857
Width : 3.381
Height : 10.064
Entry
ampl
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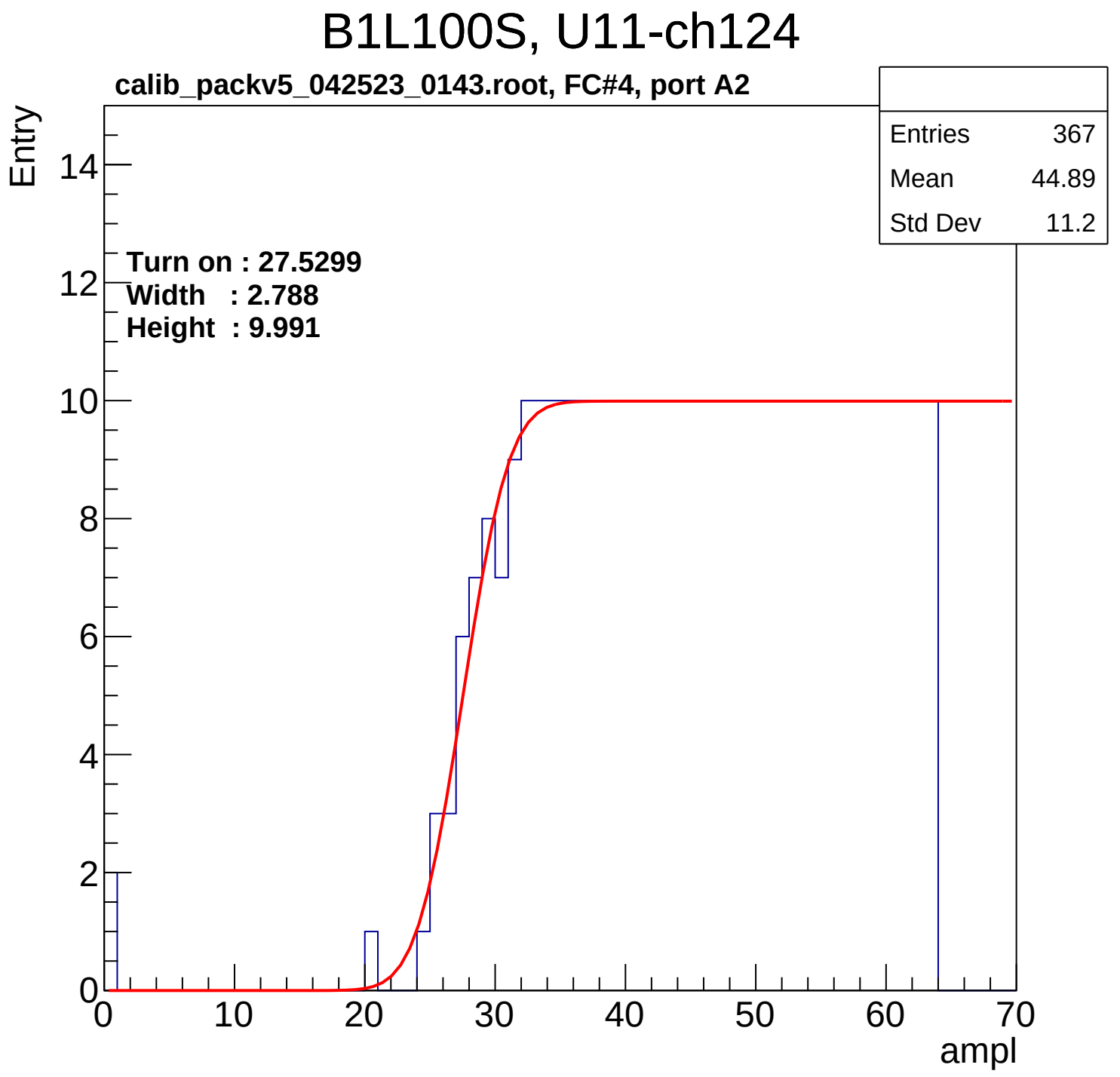
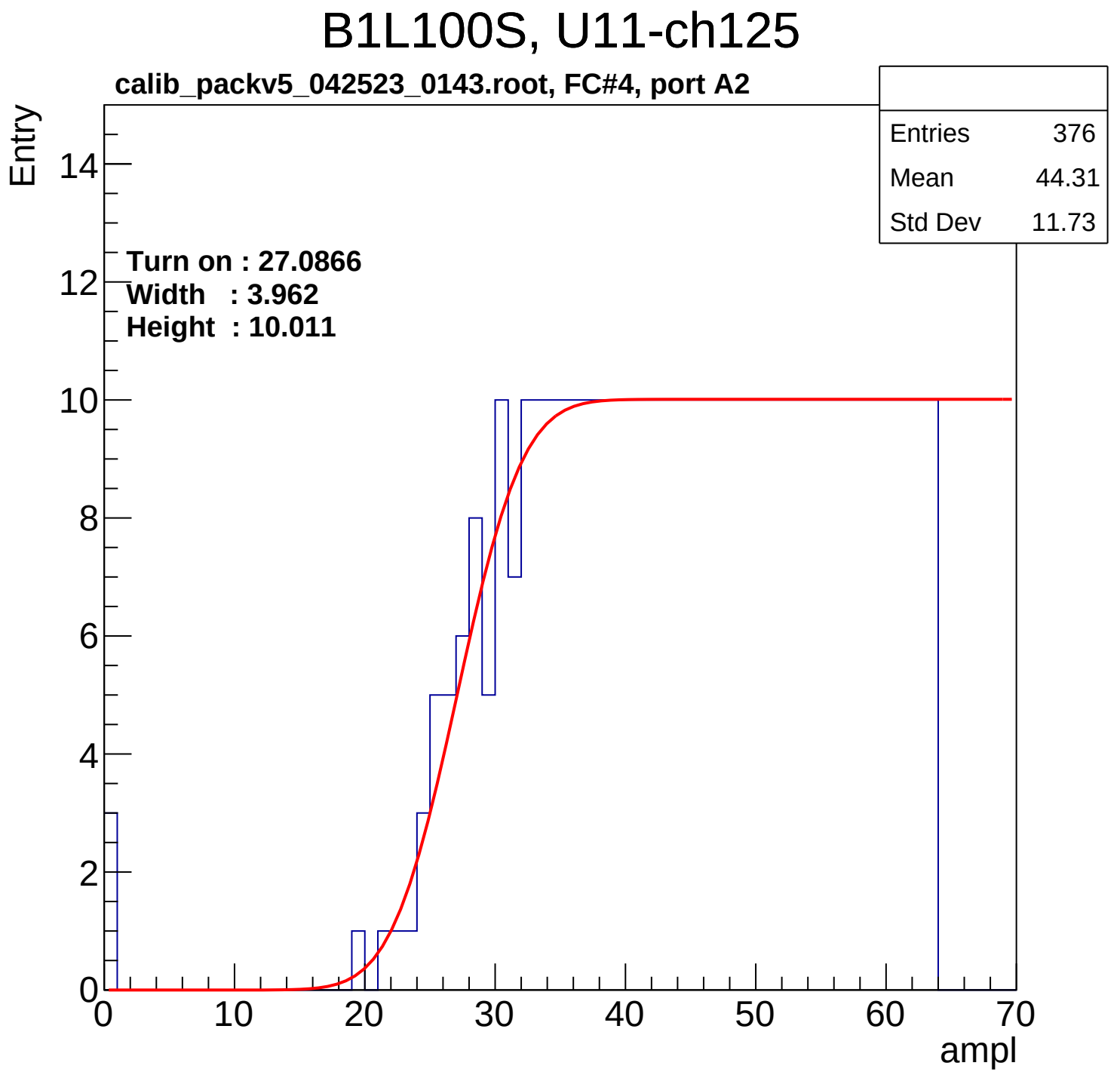
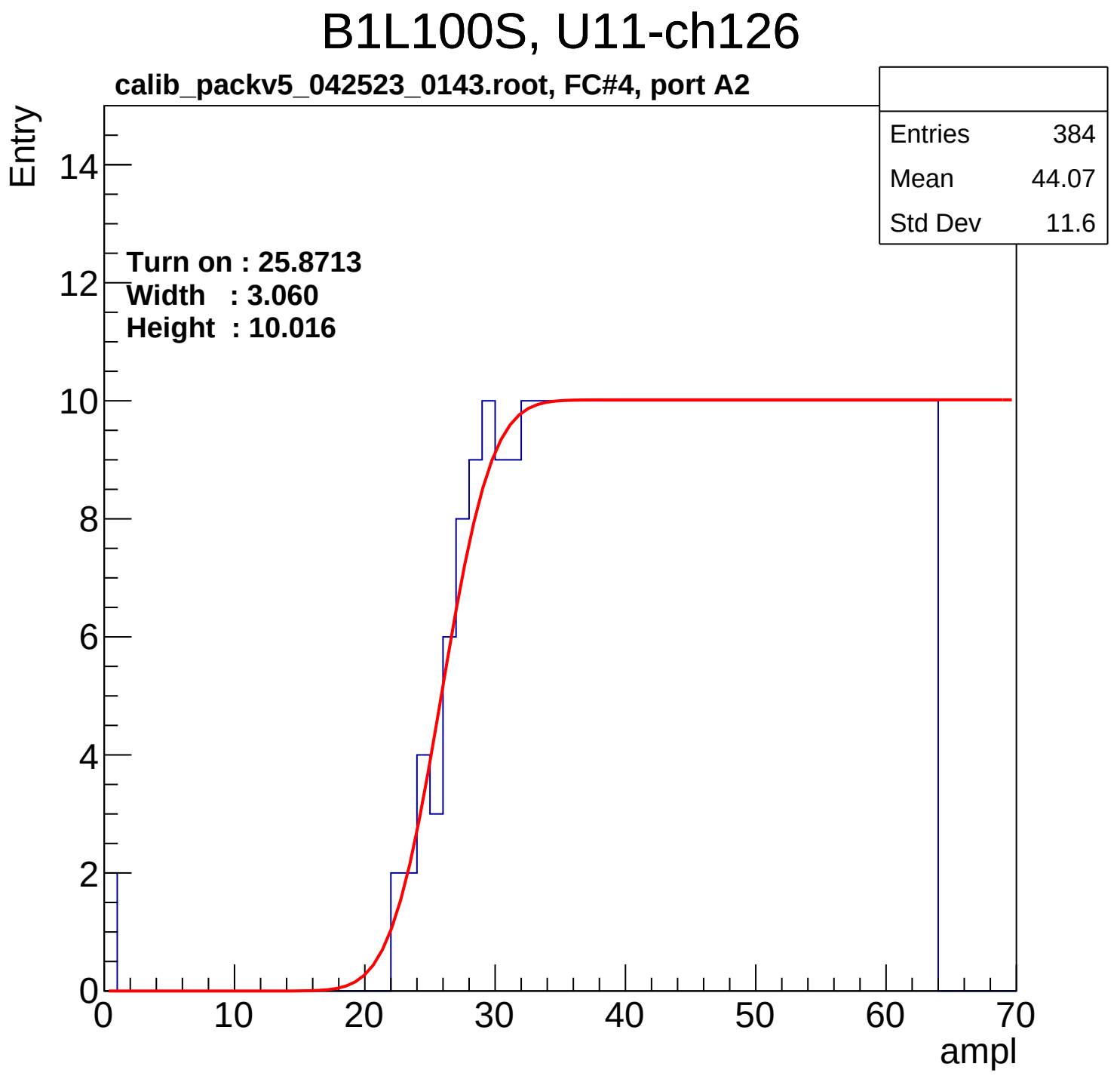
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L100S, U11-ch124
calib_packv5_042523_0143.root, FC#4, port A2
Entries 367
Mean 44.89
Std Dev 11.2
Turn on : 27.5299
Width : 2.788
Height : 9.991
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L100S, U11-ch125
calib_packv5_042523_0143.root, FC#4, port A2
Entries 376
Mean 44.31
Std Dev 11.73
Turn on : 27.0866
Width : 3.962
Height : 10.011
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L100S, U11-ch126
calib_packv5_042523_0143.root, FC#4, port A2
Entries 384
Mean 44.07
Std Dev 11.6
Turn on : 25.8713
Width : 3.060
Height : 10.016
Entry
ampl
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2
4
6
8
10
12
14
0
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20
30
40
50
60
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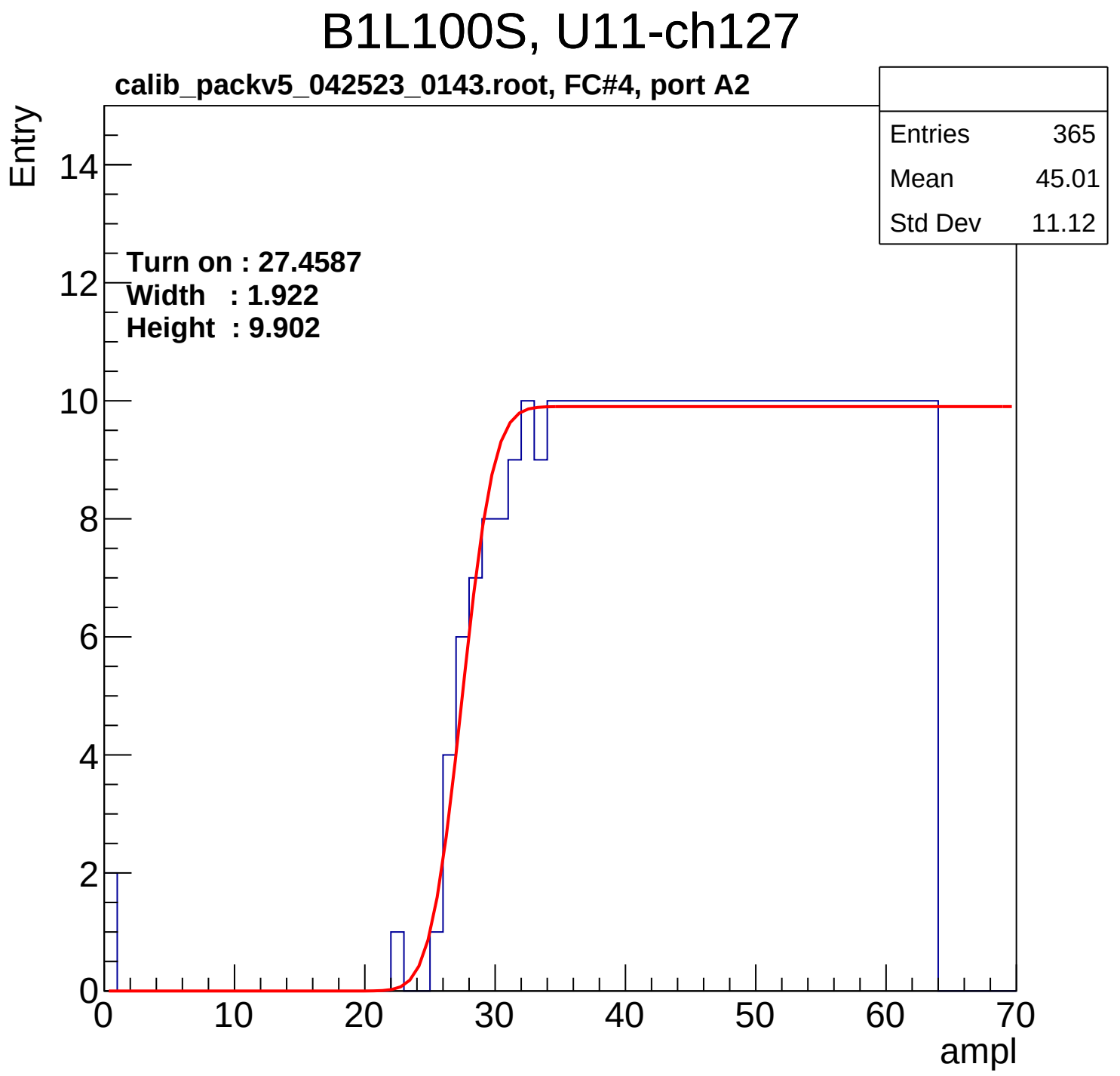
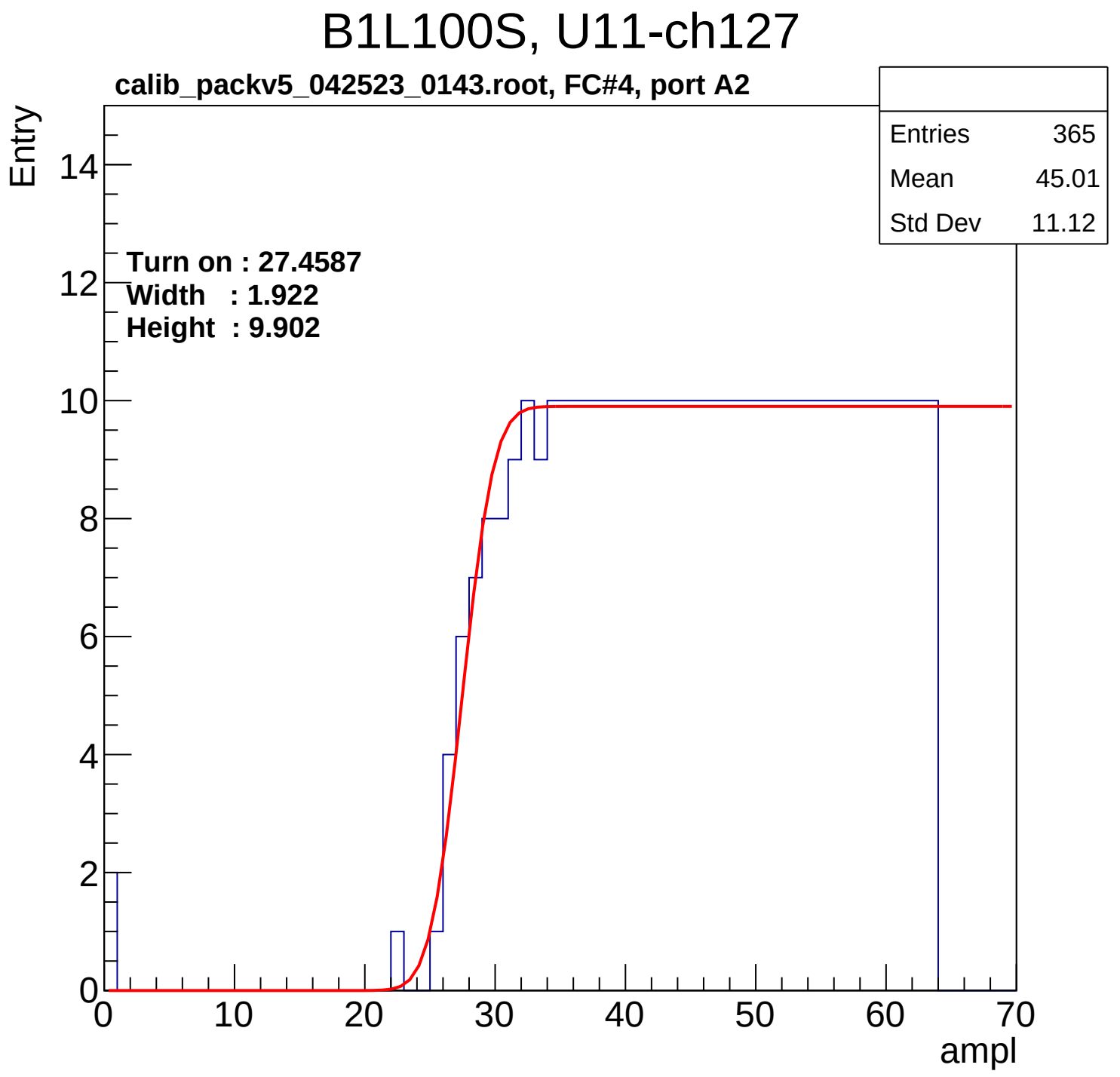

B1L100S, U11-ch127
calib_packv5_042523_0143.root, FC#4, port A2
Entries 365
Mean 45.01
Std Dev 11.12
Turn on : 27.4587
Width : 1.922
Height : 9.902
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L100S, U11-ch127
calib_packv5_042523_0143.root, FC#4, port A2
Entries 365
Mean 45.01
Std Dev 11.12
Turn on : 27.4587
Width : 1.922
Height : 9.902
Entry
ampl
0
2
4
6
8
10
12
14
0
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20
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40
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60
70