

B1L101S, U17-ch0

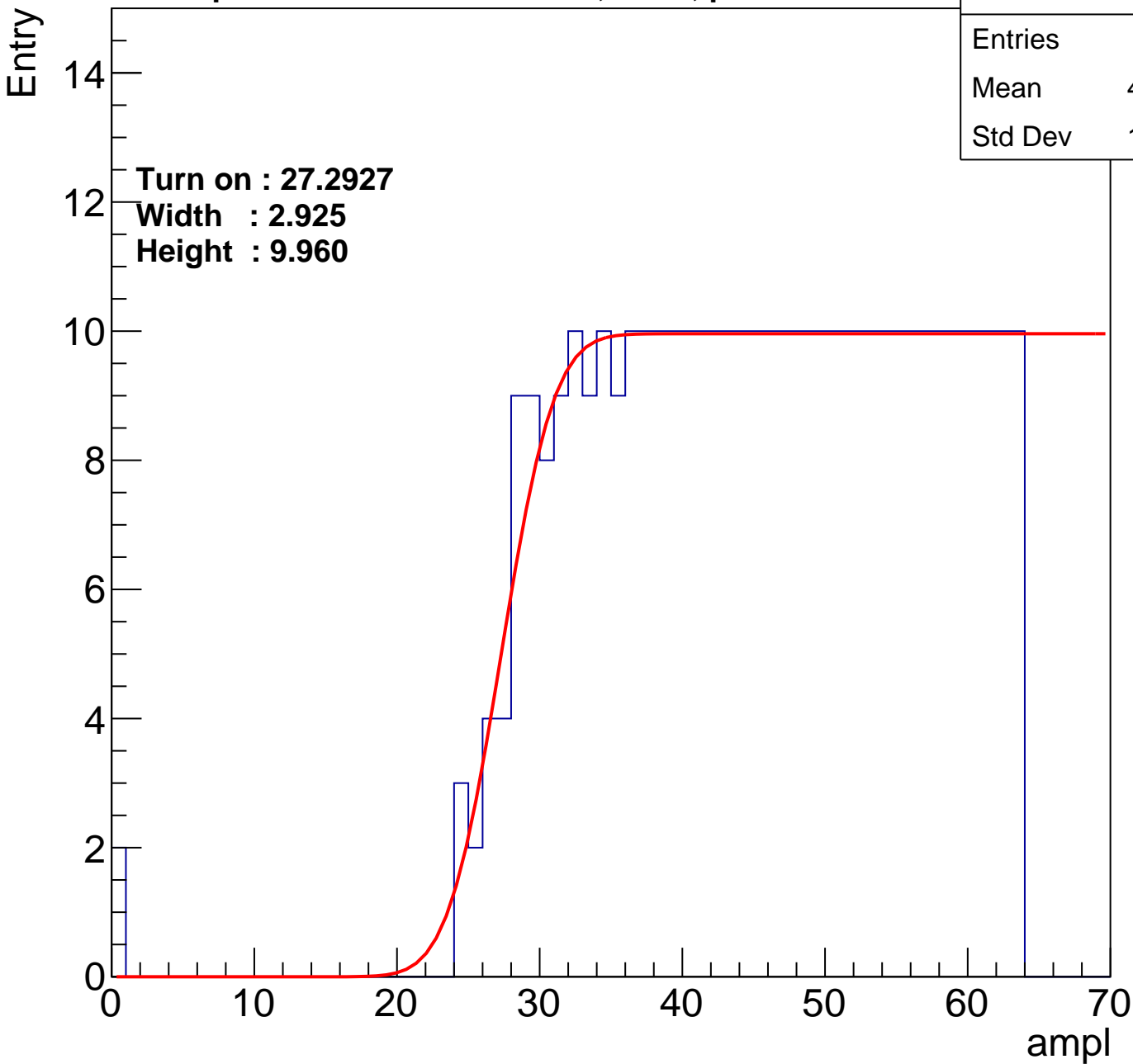
calib_packv5_042523_0143.root, FC#0, port D2

Turn on : 27.2927

Width : 2.925

Height : 9.960

Entries	368
Mean	44.83
Std Dev	11.23



B1L101S, U17-ch1

calib_packv5_042523_0143.root, FC#0, port D2

Entries	375
Mean	44.55
Std Dev	11.32

Turn on : 26.5542

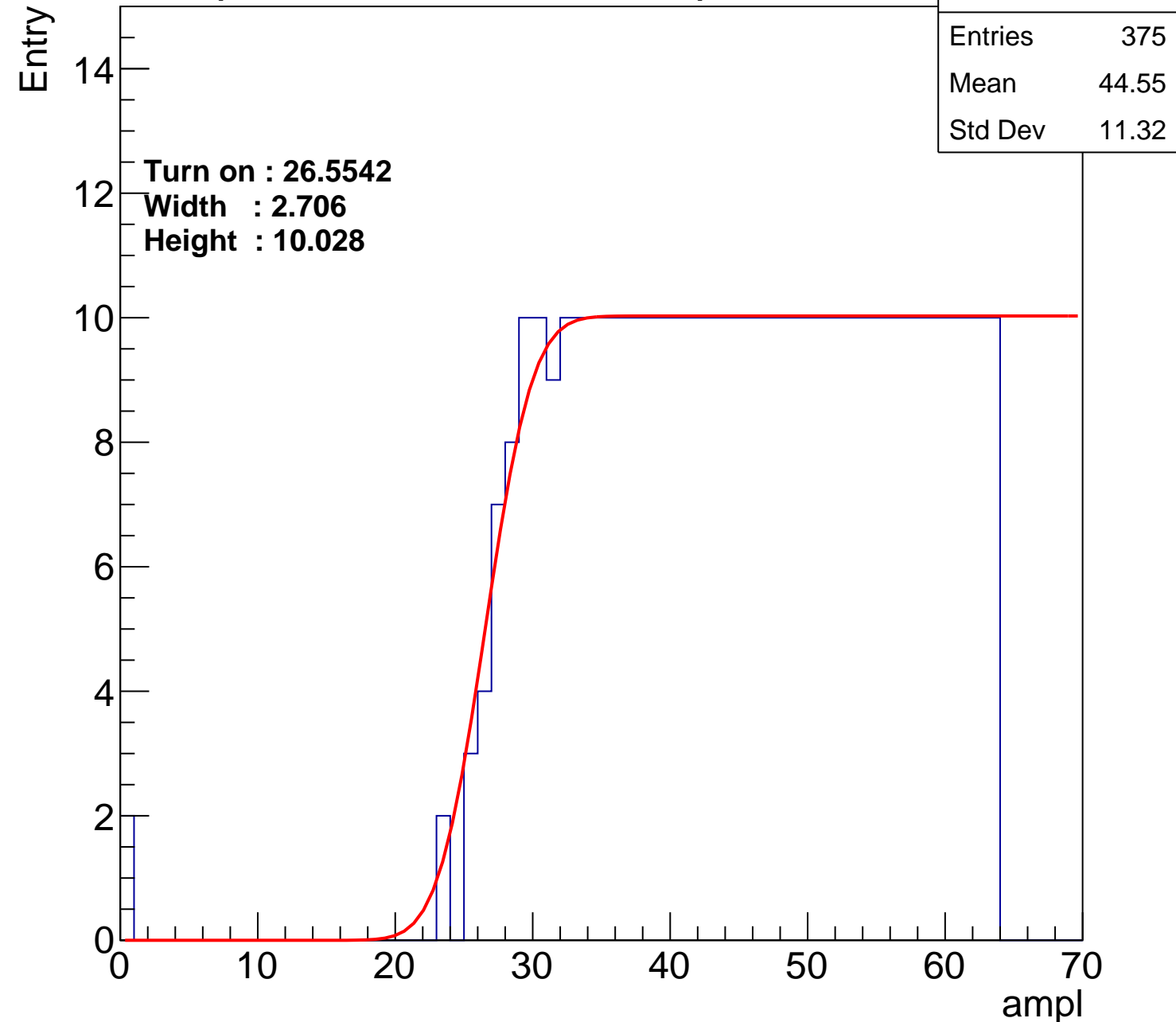
Width : 2.706

Height : 10.028

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U17-ch2

calib_packv5_042523_0143.root, FC#0, port D2

Entries	384
Mean	43.97
Std Dev	11.91

Turn on : 26.3657

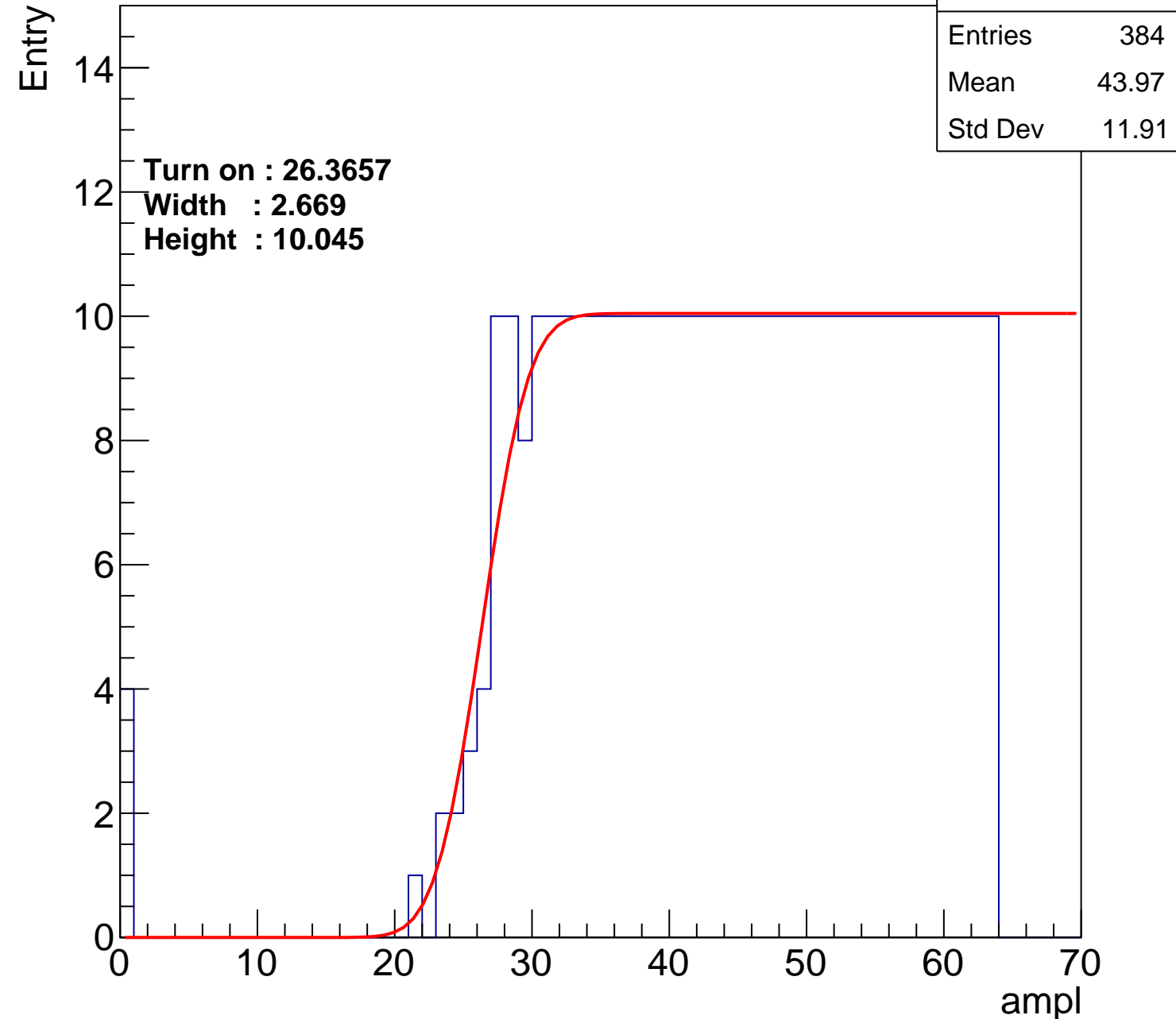
Width : 2.669

Height : 10.045

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U17-ch3

calib_packv5_042523_0143.root, FC#0, port D2

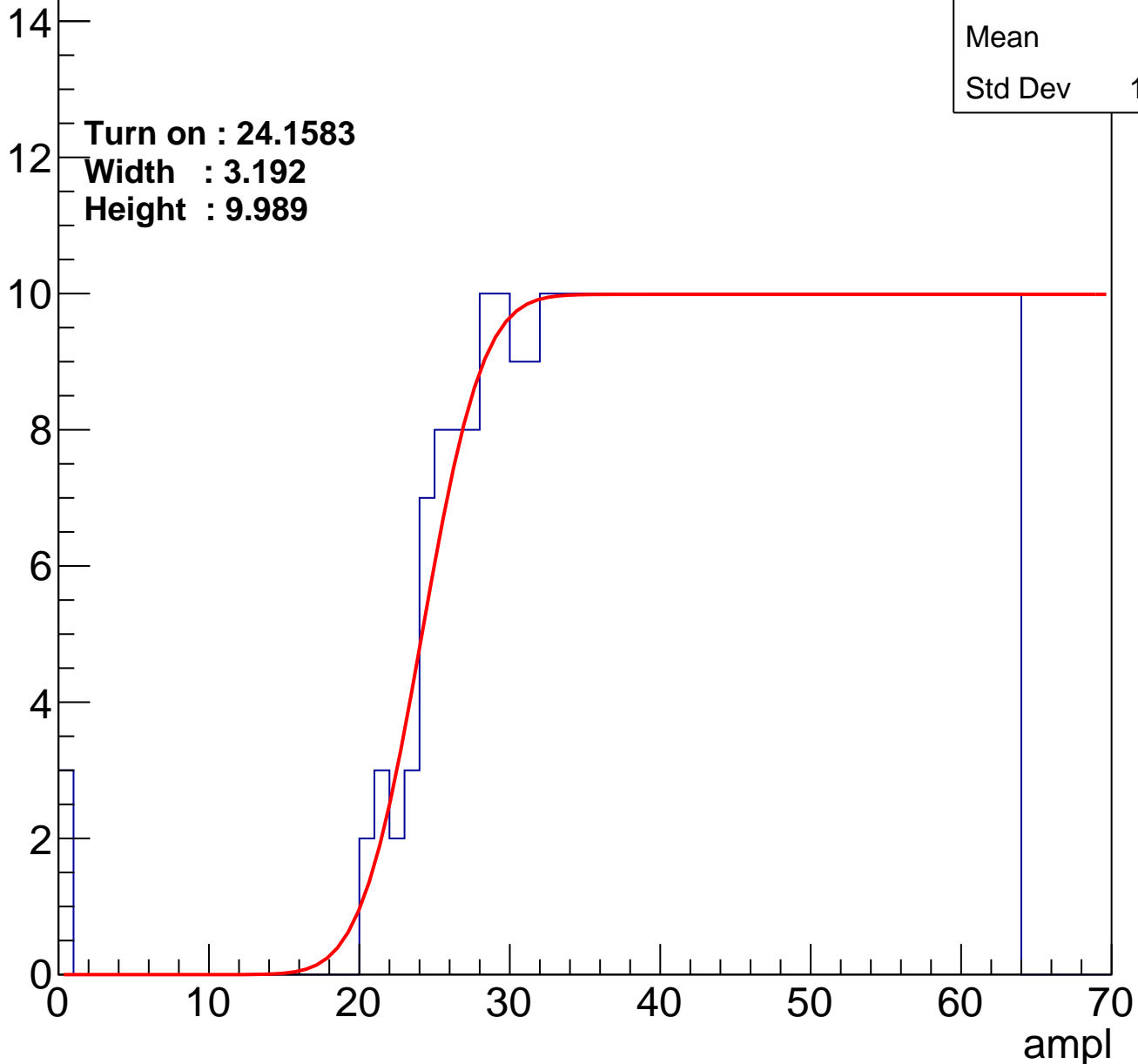
Entries	402
Mean	43.1
Std Dev	12.26

Turn on : 24.1583

Width : 3.192

Height : 9.989

Entry



B1L101S, U17-ch4

calib_packv5_042523_0143.root, FC#0, port D2

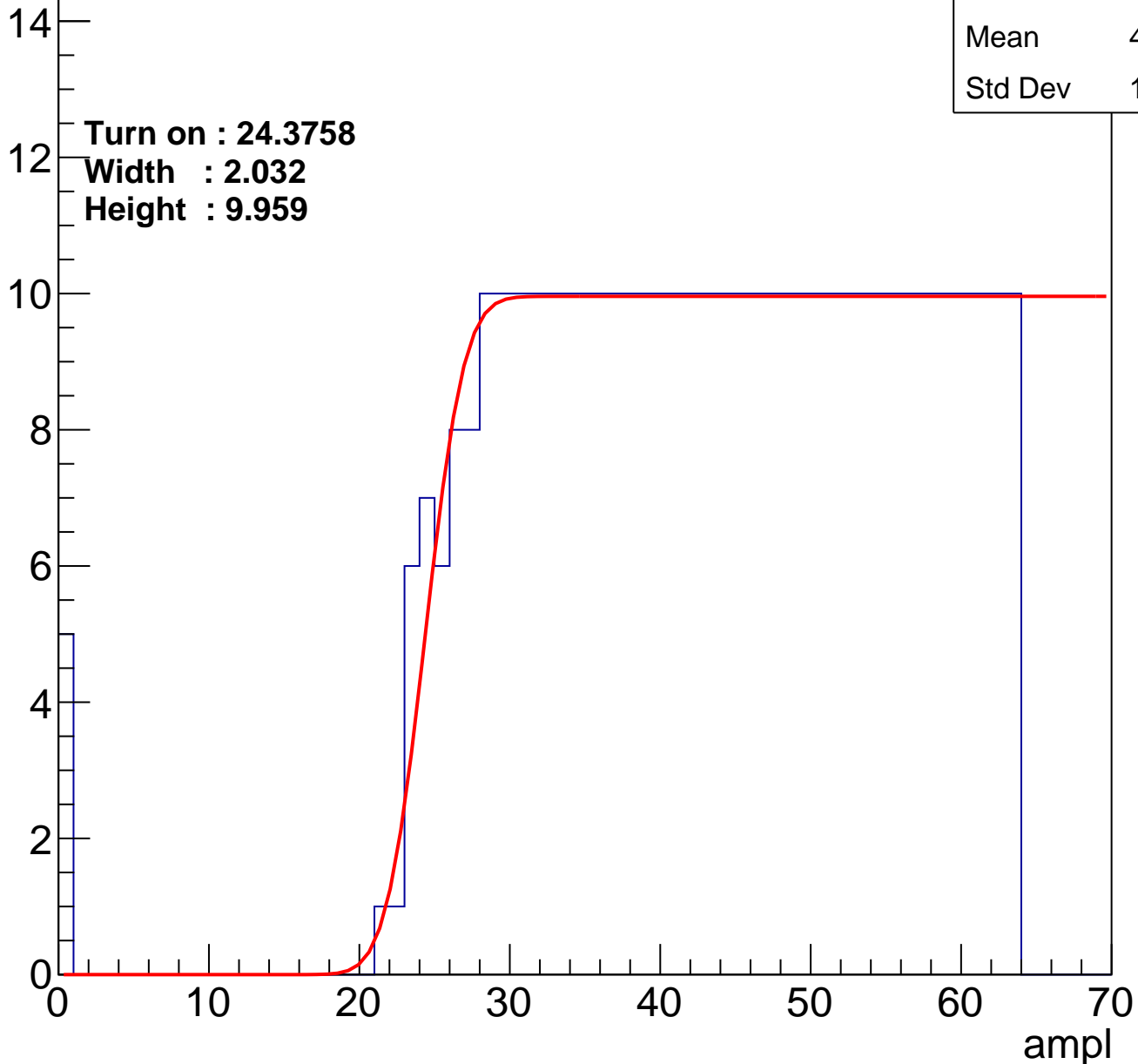
Entries	402
Mean	43.04
Std Dev	12.47

Turn on : 24.3758

Width : 2.032

Height : 9.959

Entry



B1L101S, U17-ch5

calib_packv5_042523_0143.root, FC#0, port D2

Entries	382
Mean	44.07
Std Dev	11.81

Turn on : 26.9287

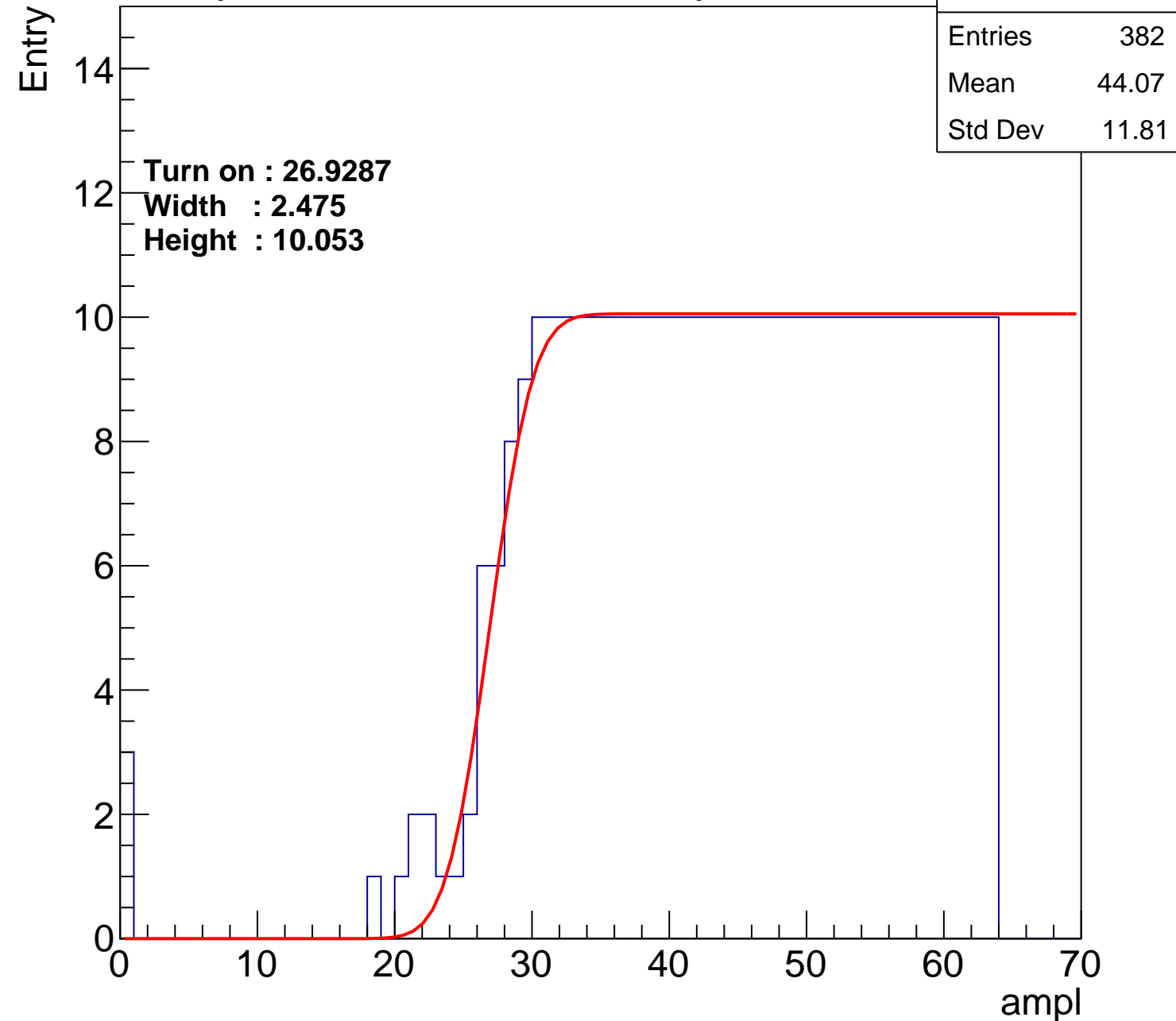
Width : 2.475

Height : 10.053

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U17-ch6

calib_packv5_042523_0143.root, FC#0, port D2

Entries	375
Mean	44.3
Std Dev	11.95

Turn on : 26.7224

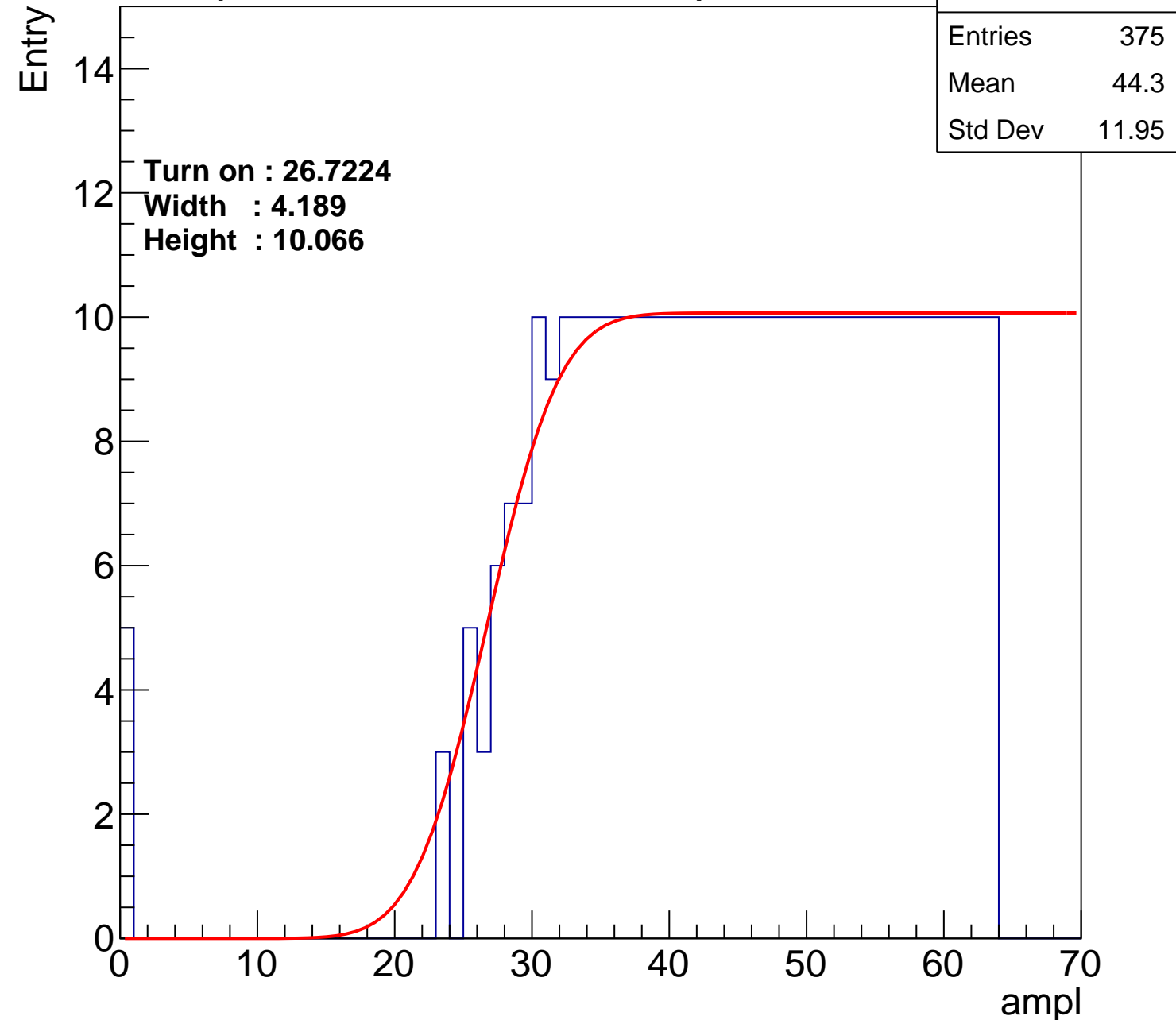
Width : 4.189

Height : 10.066

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U17-ch7

calib_packv5_042523_0143.root, FC#0, port D2

Entries	395
Mean	43.33
Std Dev	12.39

Turn on : 26.1828

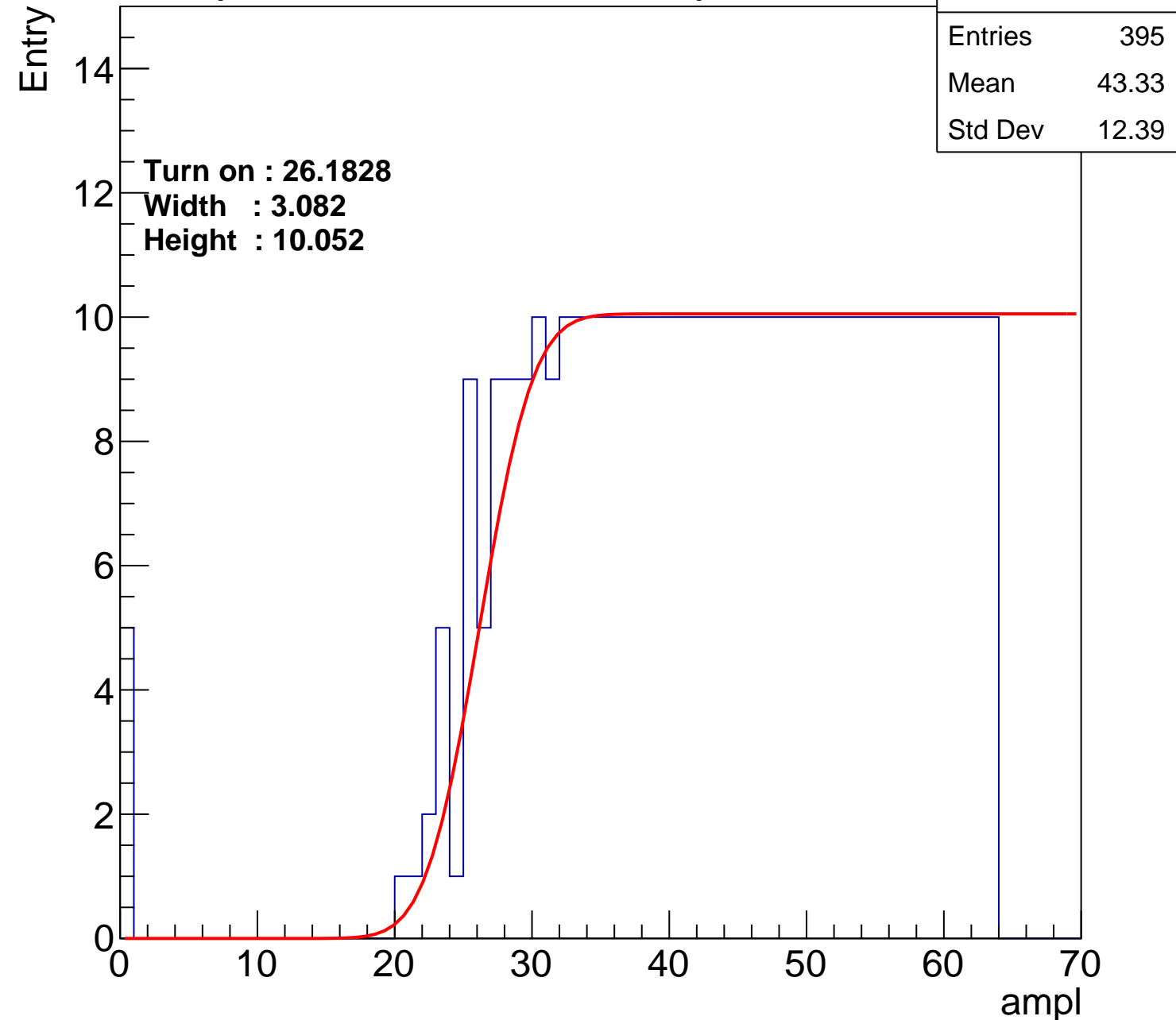
Width : 3.082

Height : 10.052

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U17-ch8

calib_packv5_042523_0143.root, FC#0, port D2

Entries	374
Mean	44.52
Std Dev	11.42

Turn on : 27.3562

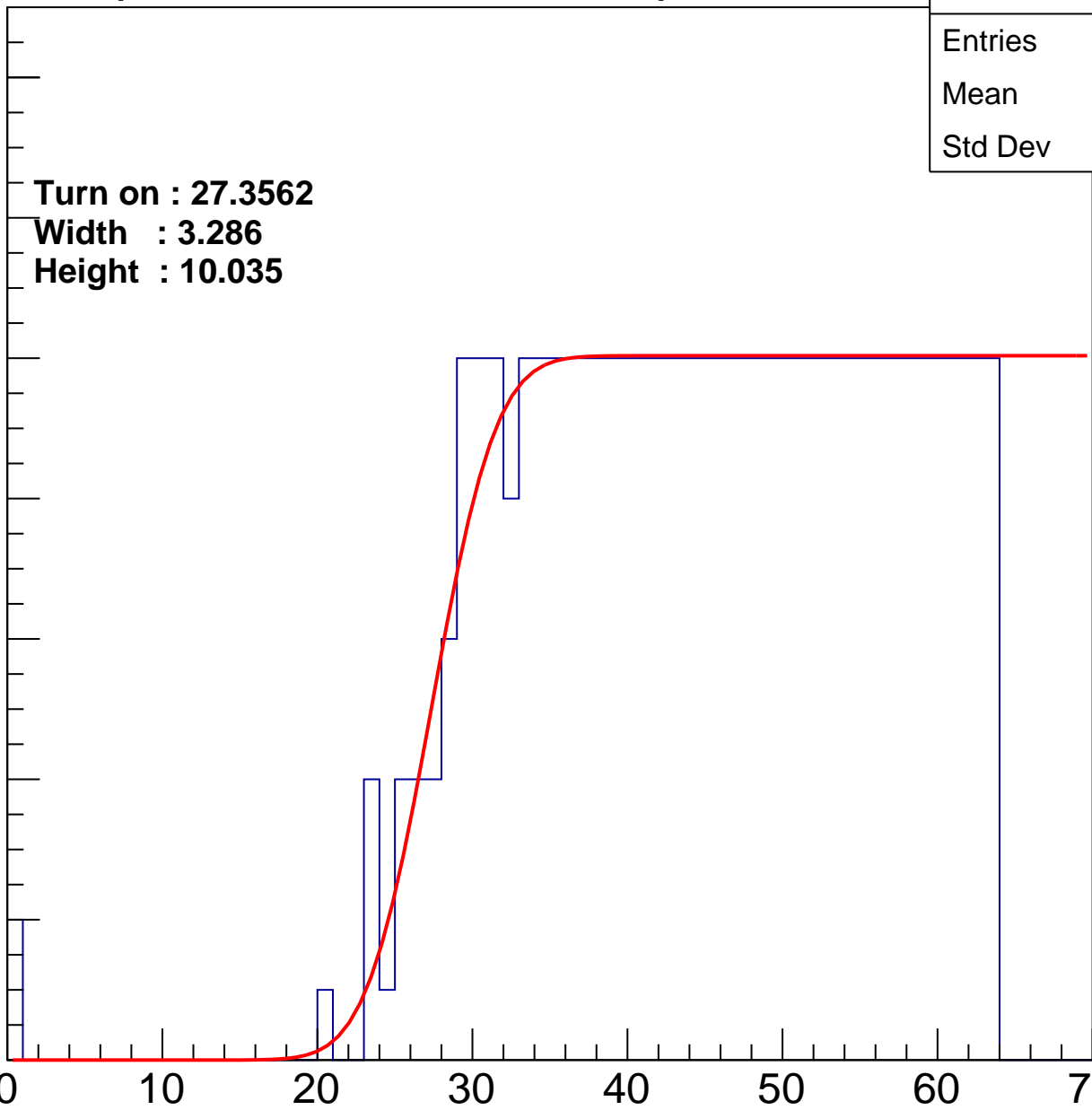
Width : 3.286

Height : 10.035

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U17-ch9

calib_packv5_042523_0143.root, FC#0, port D2

Entries	374
Mean	44.51
Std Dev	11.45

Turn on : 27.4419

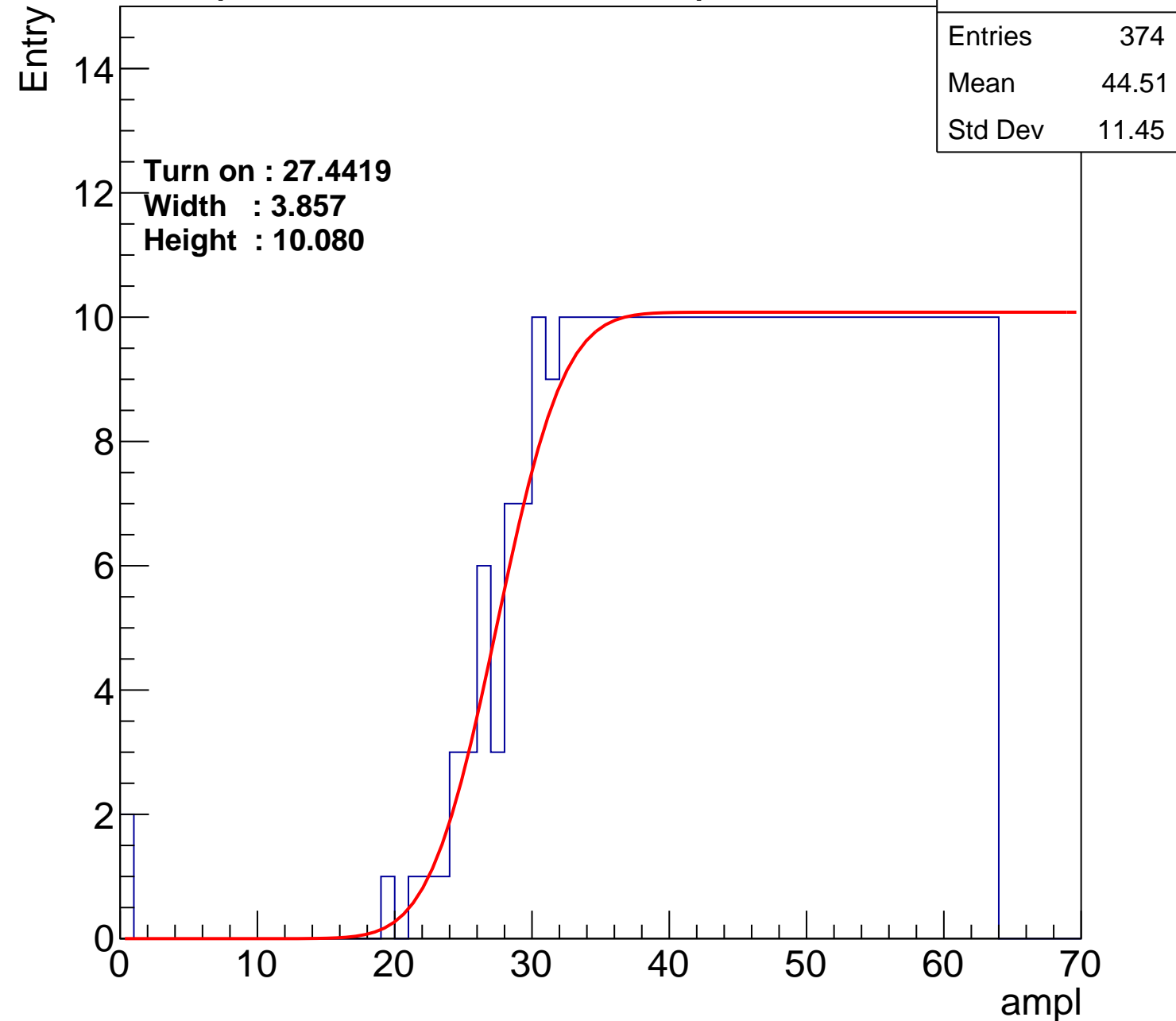
Width : 3.857

Height : 10.080

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U17-ch10

calib_packv5_042523_0143.root, FC#0, port D2

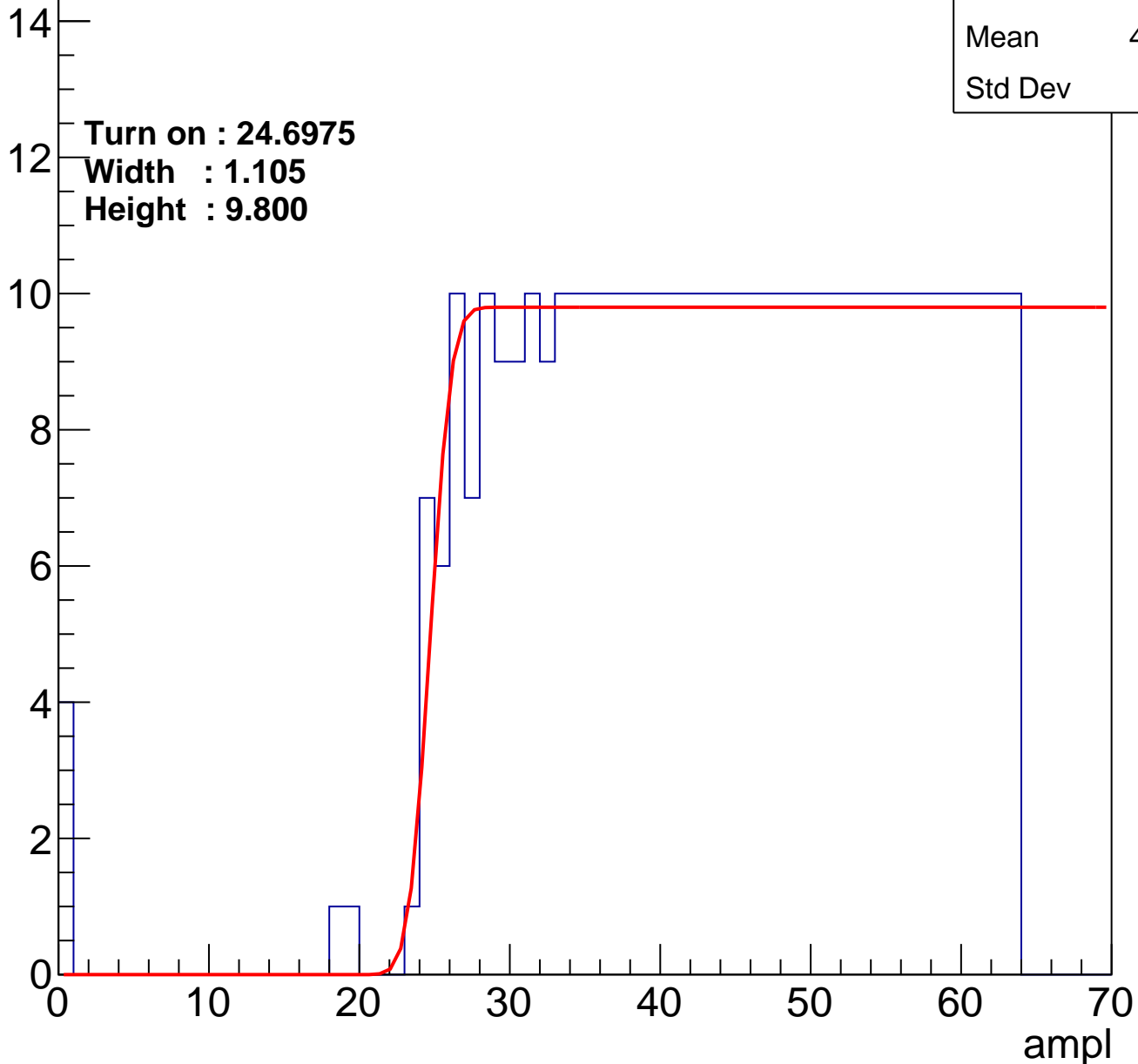
Entries	394
Mean	43.44
Std Dev	12.2

Turn on : 24.6975

Width : 1.105

Height : 9.800

Entry



B1L101S, U17-ch11

calib_packv5_042523_0143.root, FC#0, port D2

Entries	366
Mean	44.6
Std Dev	12.13

Turn on : 28.7671

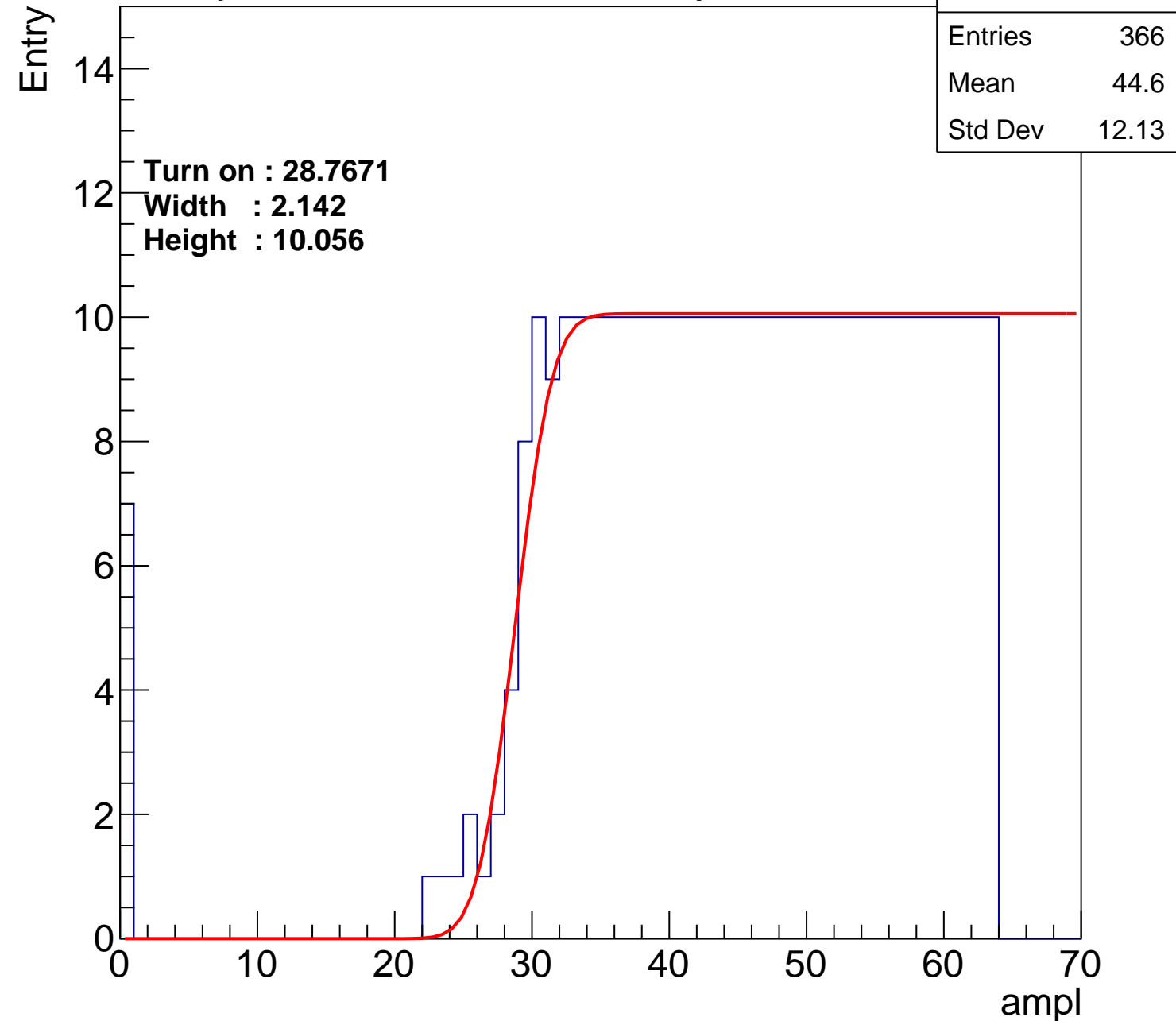
Width : 2.142

Height : 10.056

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U17-ch12

calib_packv5_042523_0143.root, FC#0, port D2

Entries	360
Mean	45.15
Std Dev	11.26

Turn on : 28.7821

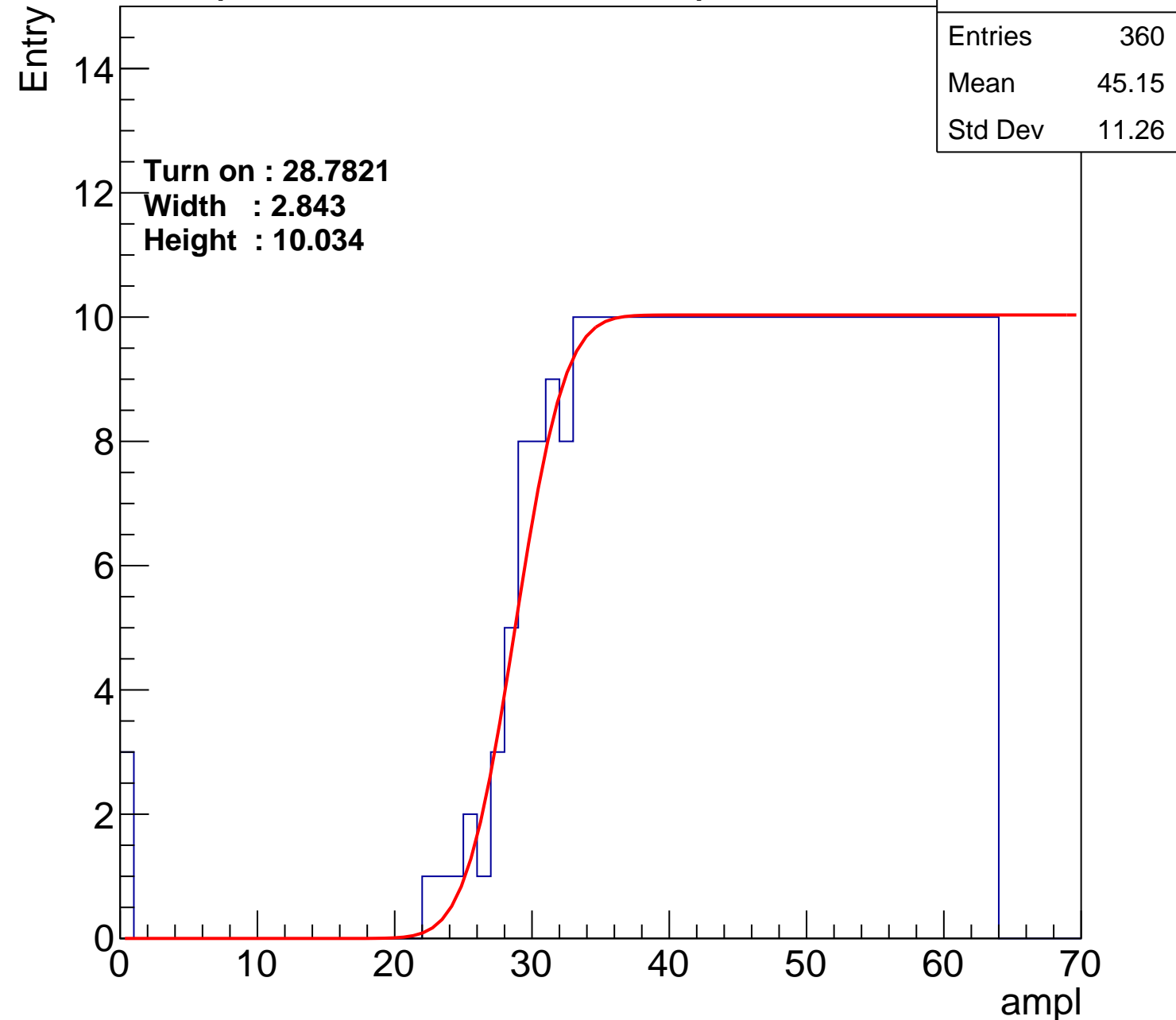
Width : 2.843

Height : 10.034

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U17-ch13

calib_packv5_042523_0143.root, FC#0, port D2

Entries	350
Mean	45.82
Std Dev	10.51

Turn on : 29.0107

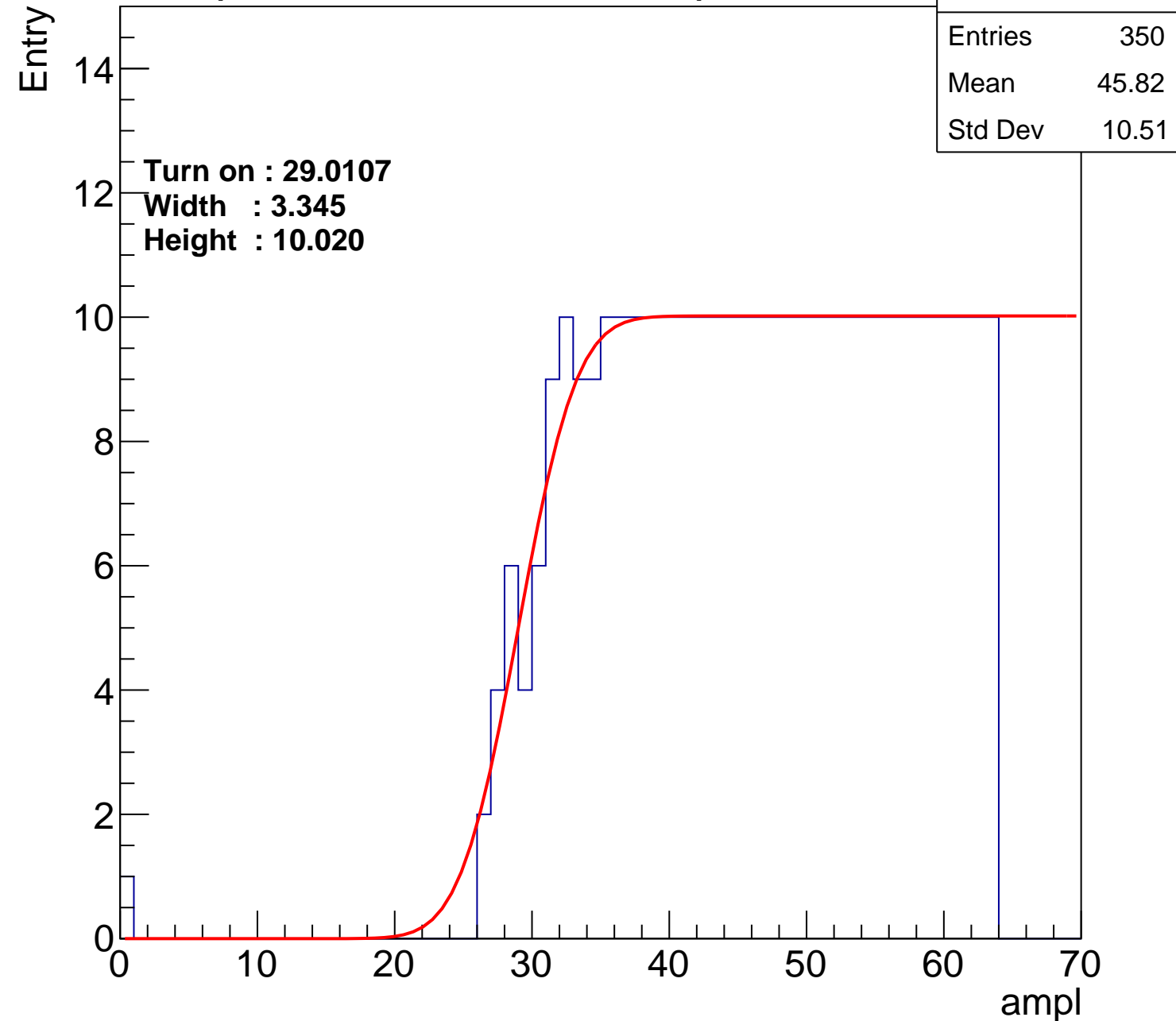
Width : 3.345

Height : 10.020

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U17-ch14

calib_packv5_042523_0143.root, FC#0, port D2

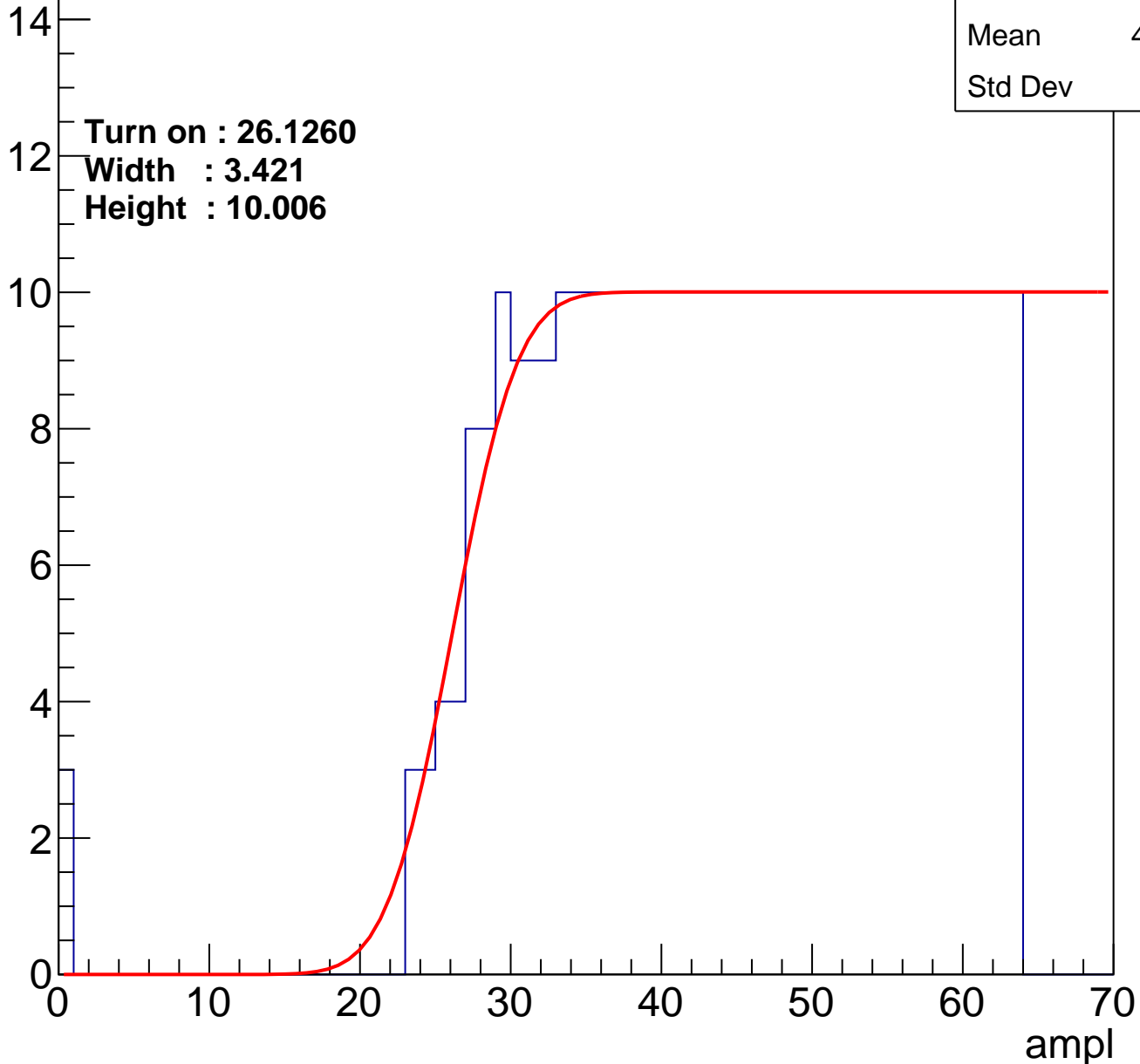
Entries	380
Mean	44.19
Std Dev	11.7

Turn on : 26.1260

Width : 3.421

Height : 10.006

Entry



B1L101S, U17-ch15

calib_packv5_042523_0143.root, FC#0, port D2

Entries	354
Mean	45.48
Std Dev	11.05

Turn on : 29.2953

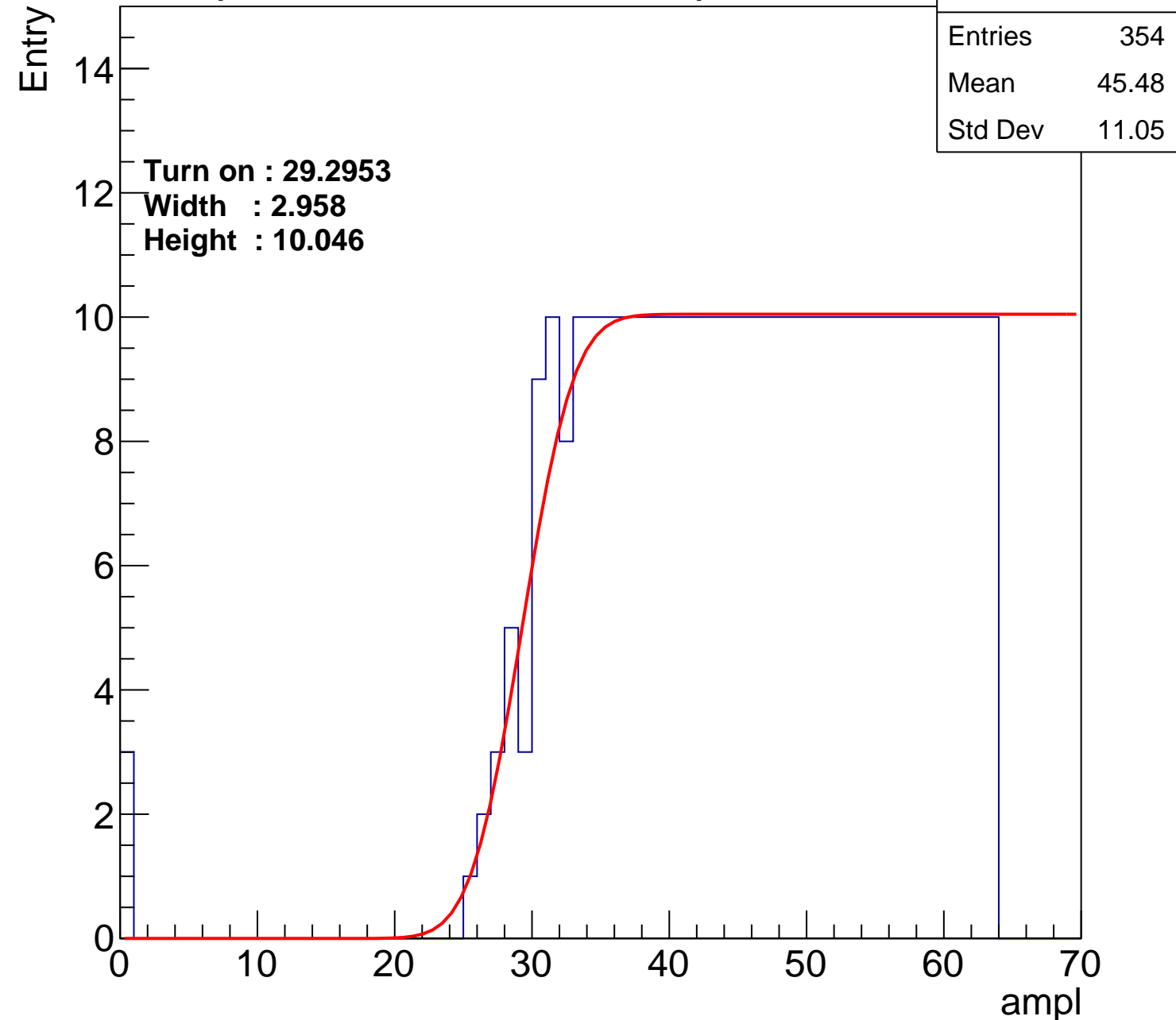
Width : 2.958

Height : 10.046

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U17-ch16

calib_packv5_042523_0143.root, FC#0, port D2

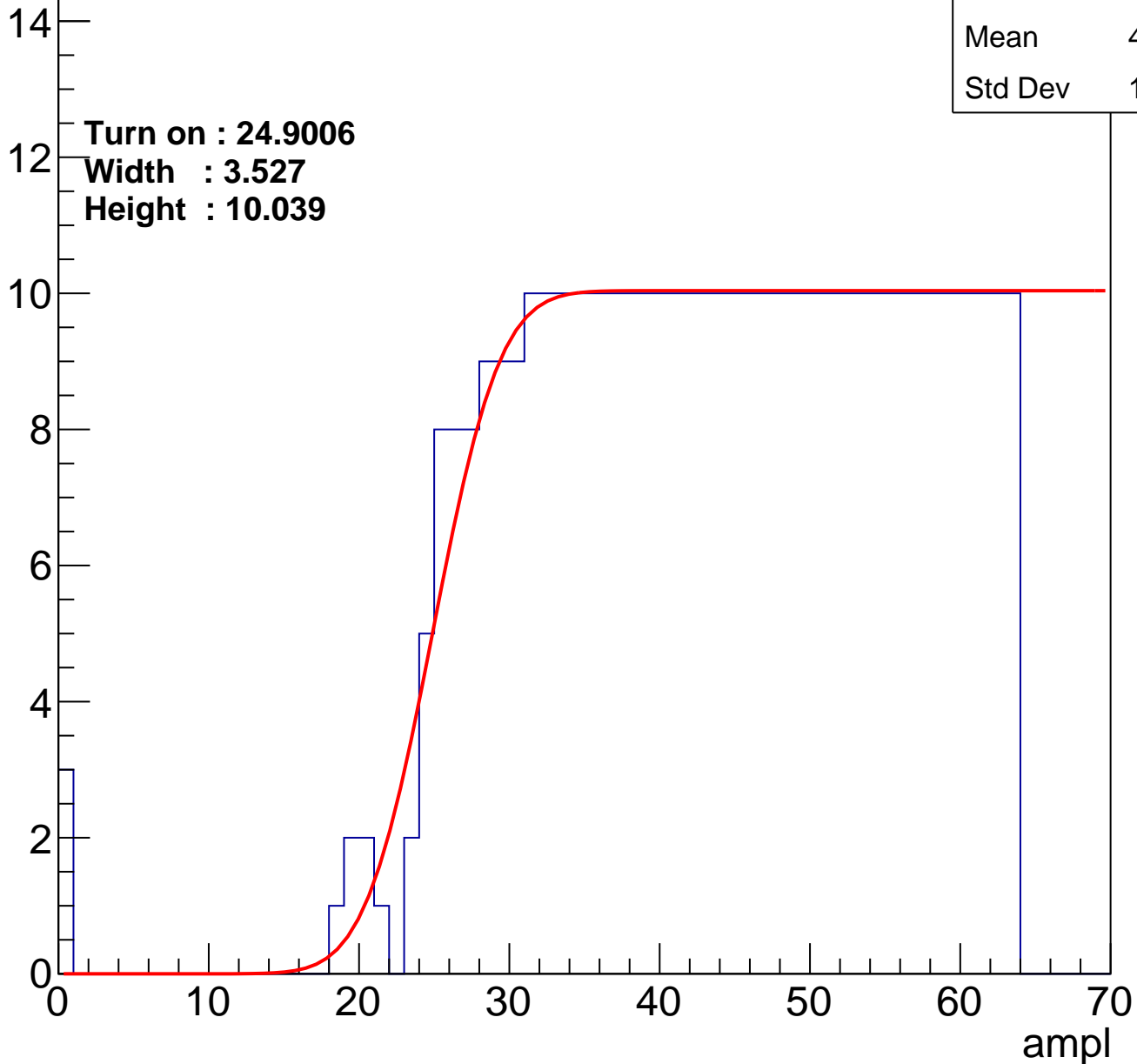
Entries	397
Mean	43.32
Std Dev	12.18

Turn on : 24.9006

Width : 3.527

Height : 10.039

Entry



B1L101S, U17-ch17

calib_packv5_042523_0143.root, FC#0, port D2

Entries	379
Mean	44.18
Std Dev	11.84

Turn on : 26.7620

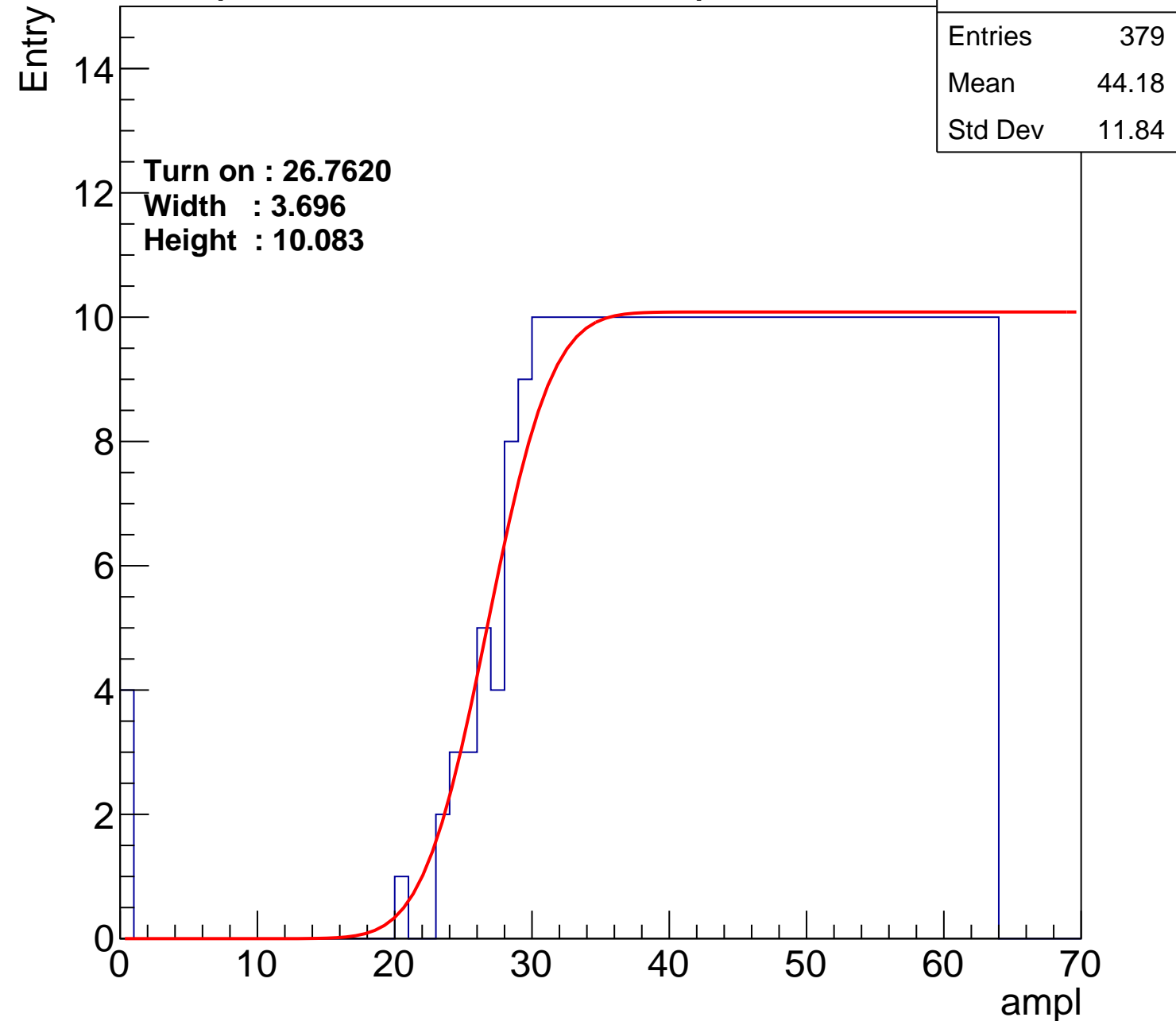
Width : 3.696

Height : 10.083

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U17-ch18

calib_packv5_042523_0143.root, FC#0, port D2

Entries	378
Mean	44.39
Std Dev	11.34

Turn on : 27.2804

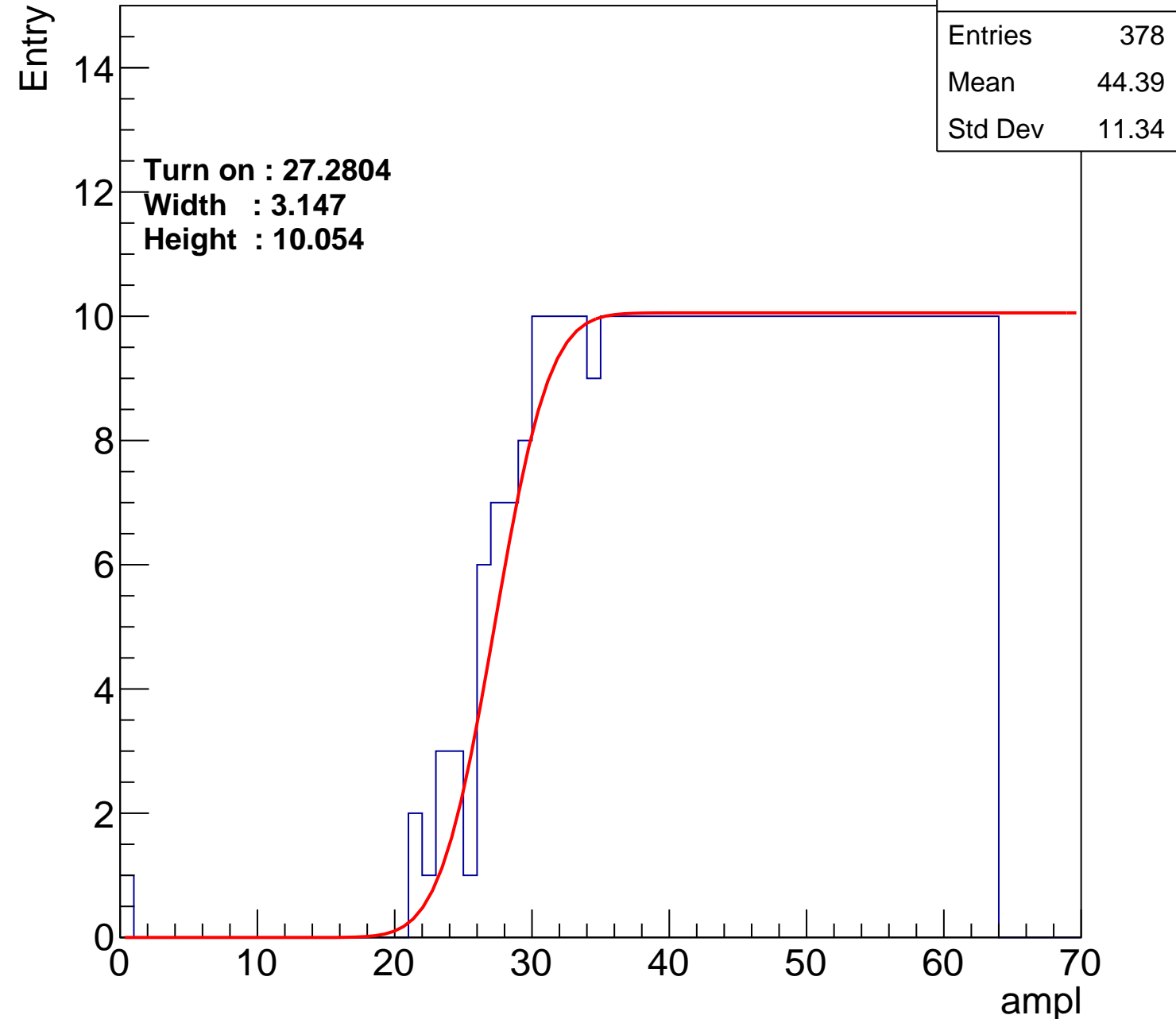
Width : 3.147

Height : 10.054

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U17-ch19

calib_packv5_042523_0143.root, FC#0, port D2

Entries	383
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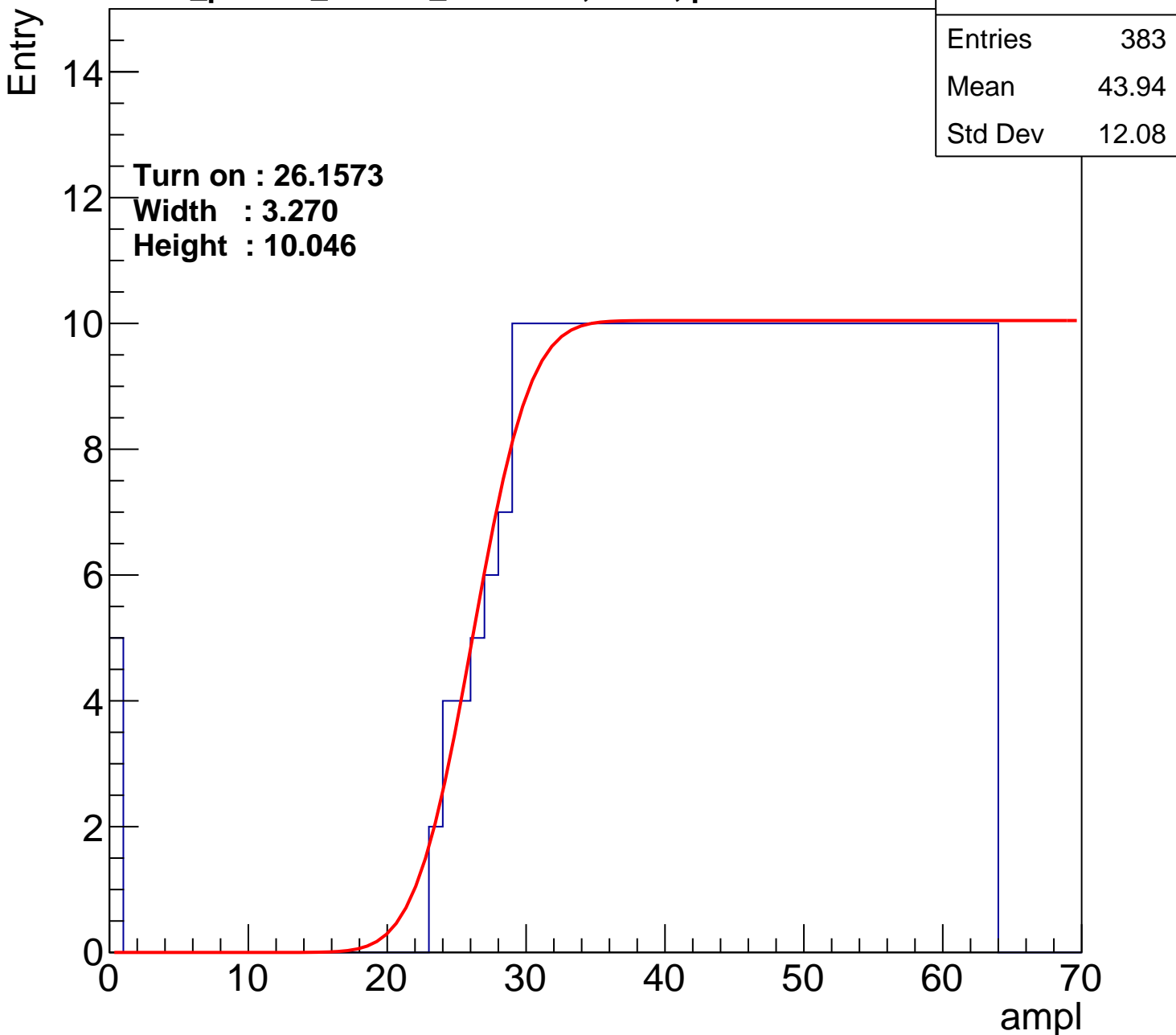
Mean	43.94
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Std Dev	12.08
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Turn on : 26.1573

Width : 3.270

Height : 10.046



B1L101S, U17-ch20

calib_packv5_042523_0143.root, FC#0, port D2

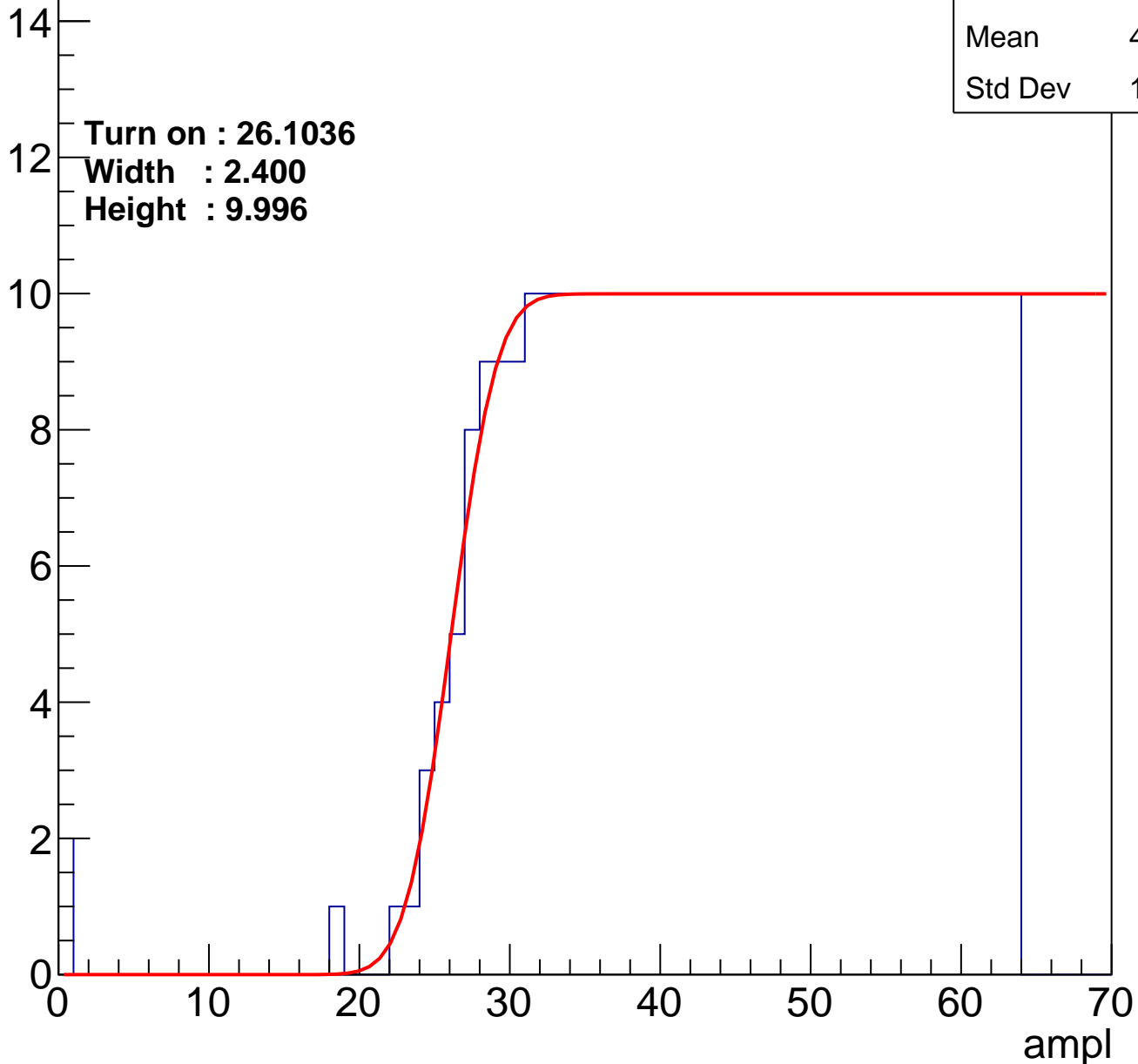
Entries	382
Mean	44.17
Std Dev	11.56

Turn on : 26.1036

Width : 2.400

Height : 9.996

Entry



B1L101S, U17-ch21

calib_packv5_042523_0143.root, FC#0, port D2

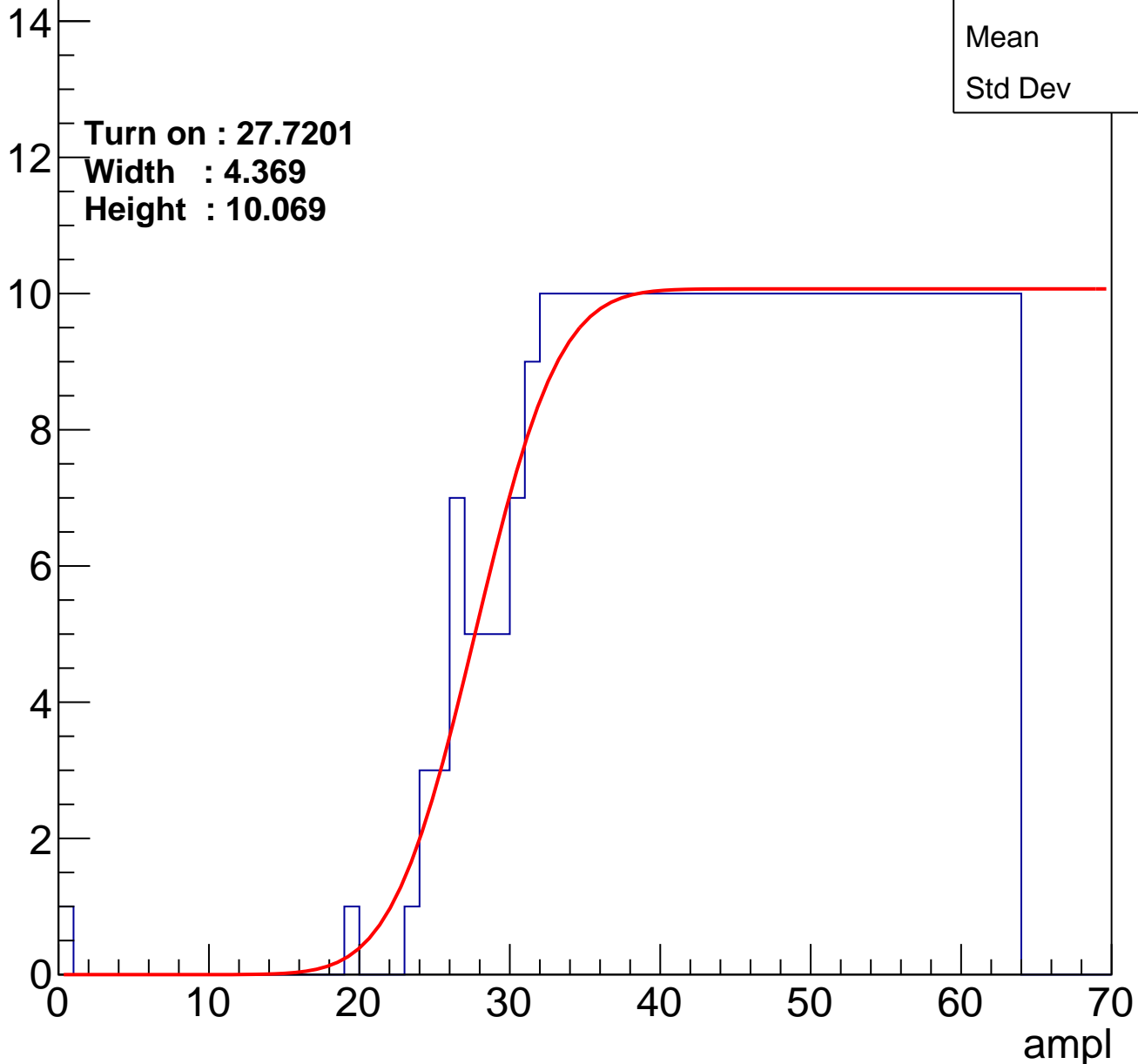
Entries	367
Mean	44.9
Std Dev	11.1

Turn on : 27.7201

Width : 4.369

Height : 10.069

Entry



B1L101S, U17-ch22

calib_packv5_042523_0143.root, FC#0, port D2

Entries	373
Mean	44.4
Std Dev	11.89

Turn on : 27.1205

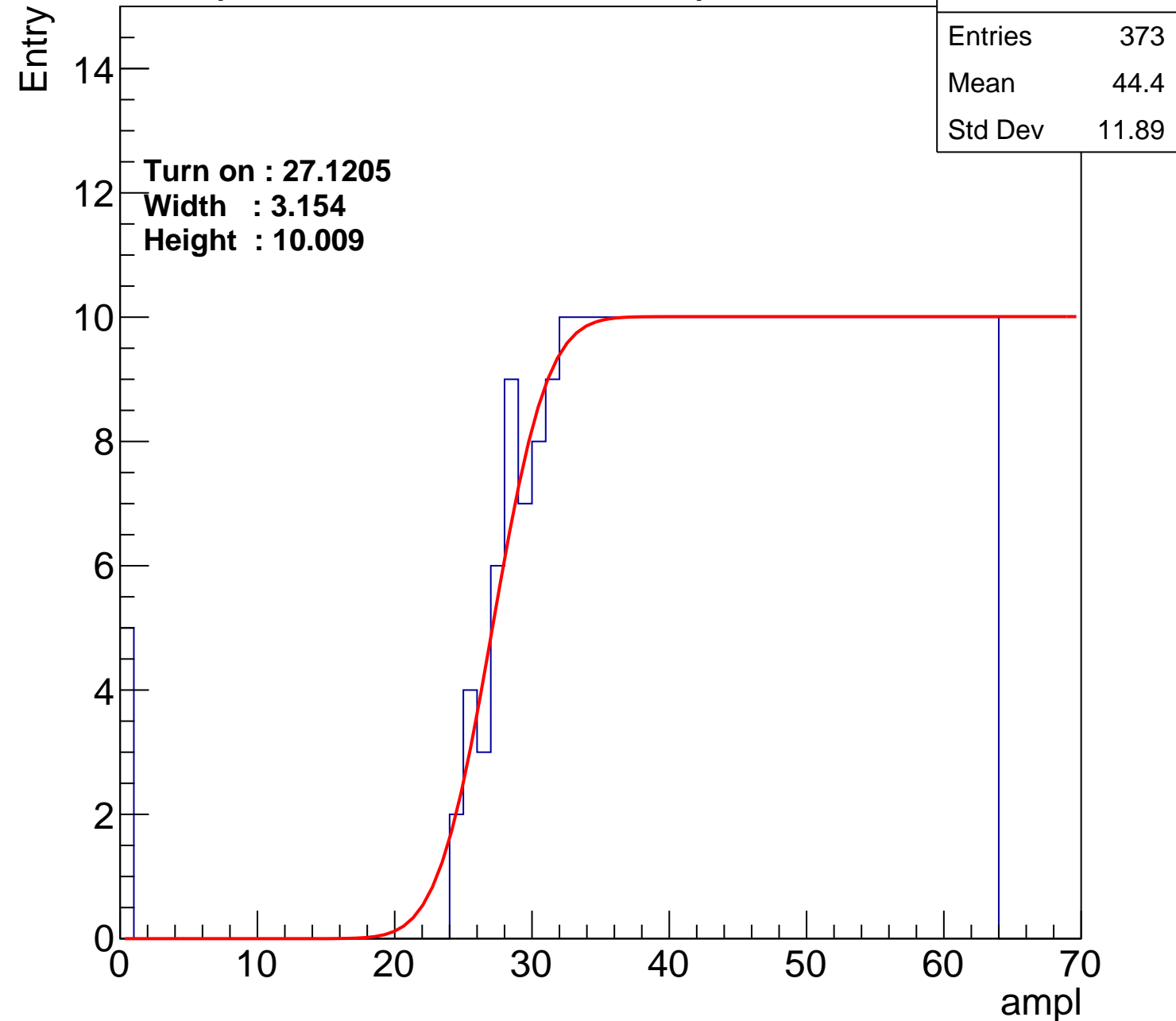
Width : 3.154

Height : 10.009

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U17-ch23

calib_packv5_042523_0143.root, FC#0, port D2

Entries	379
Mean	44.21
Std Dev	11.79

Turn on : 26.6775

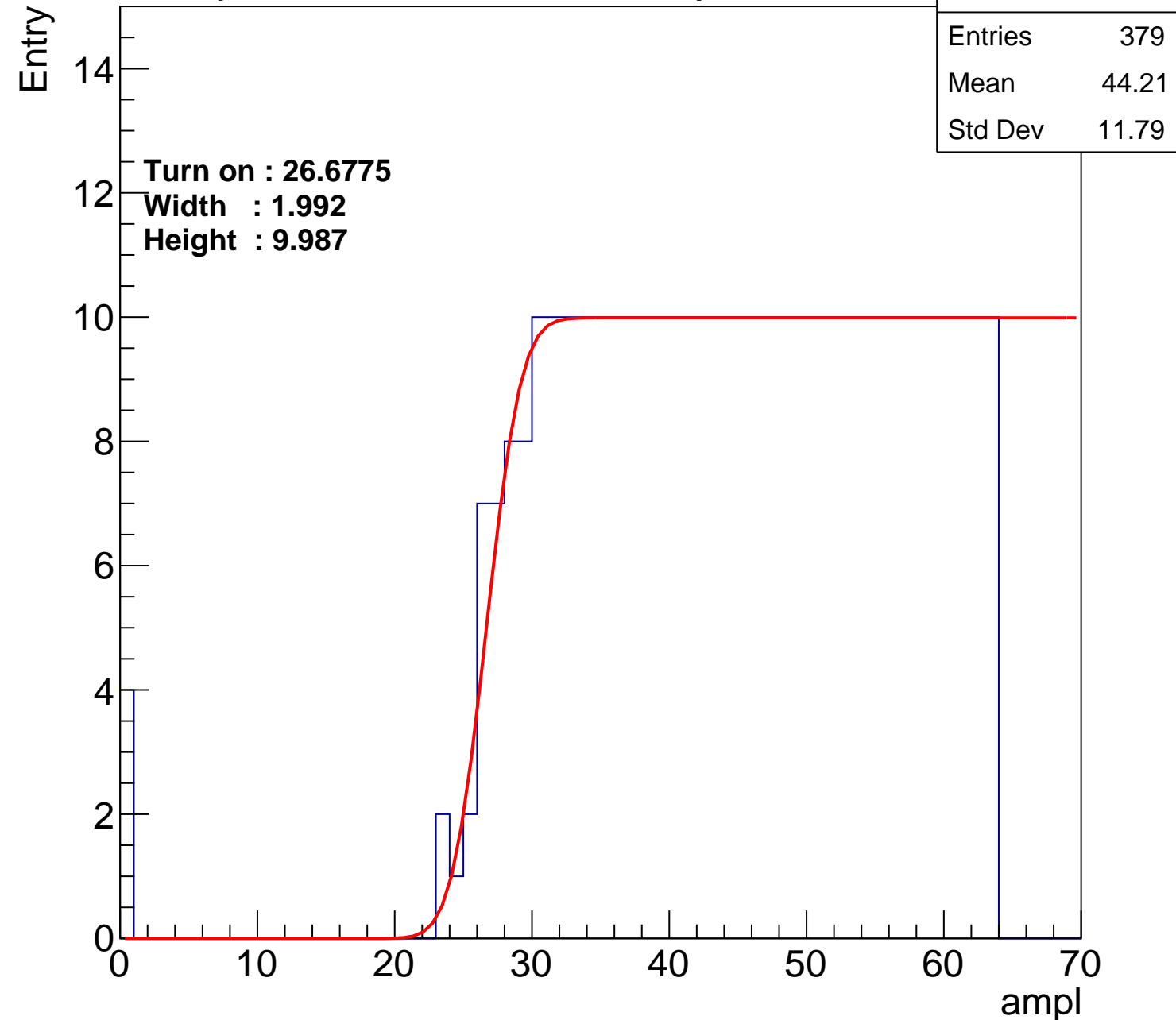
Width : 1.992

Height : 9.987

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U17-ch24

calib_packv5_042523_0143.root, FC#0, port D2

Entries	386
Mean	44.02
Std Dev	11.6

Turn on : 26.0248

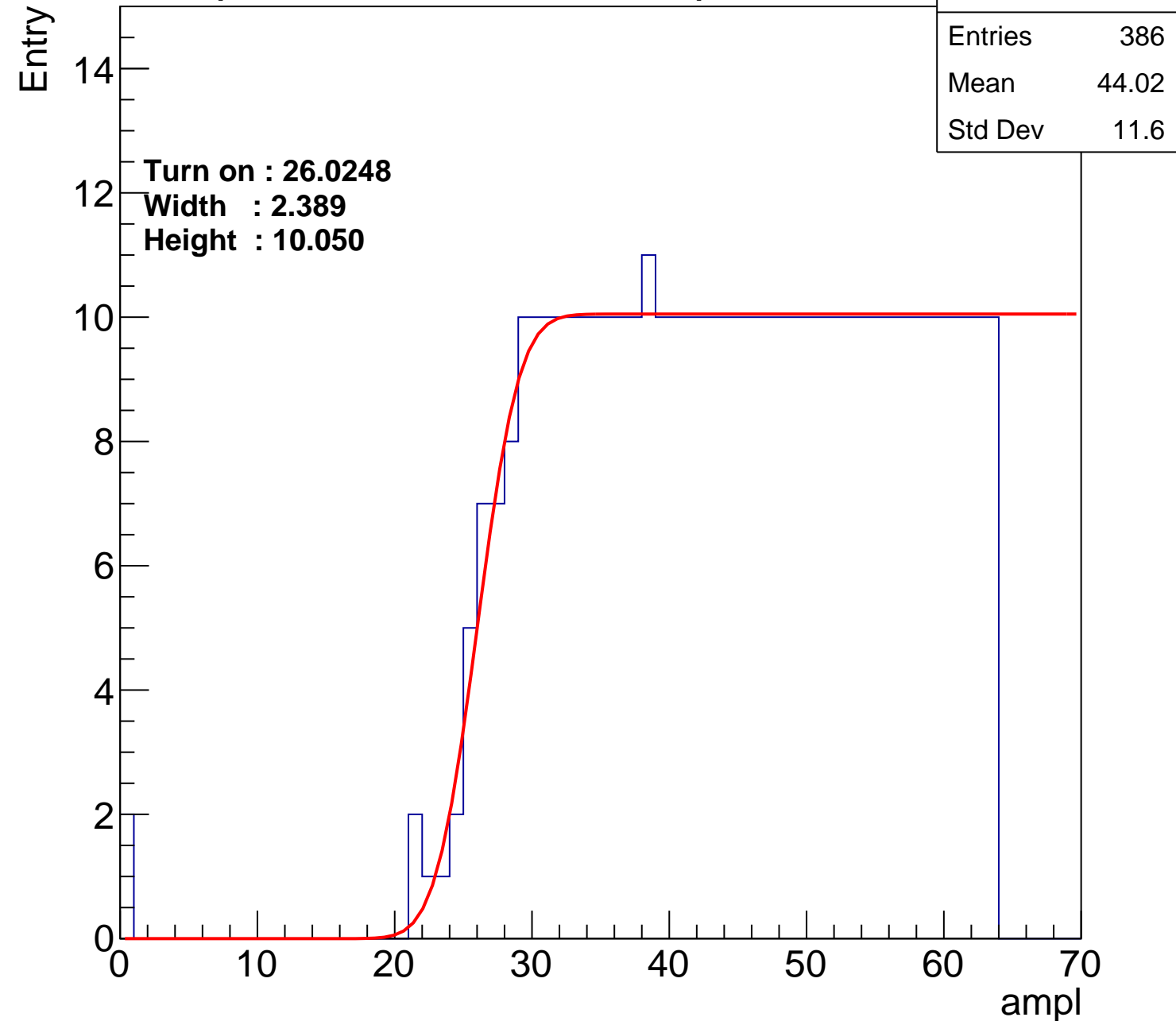
Width : 2.389

Height : 10.050

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U17-ch25

calib_packv5_042523_0143.root, FC#0, port D2

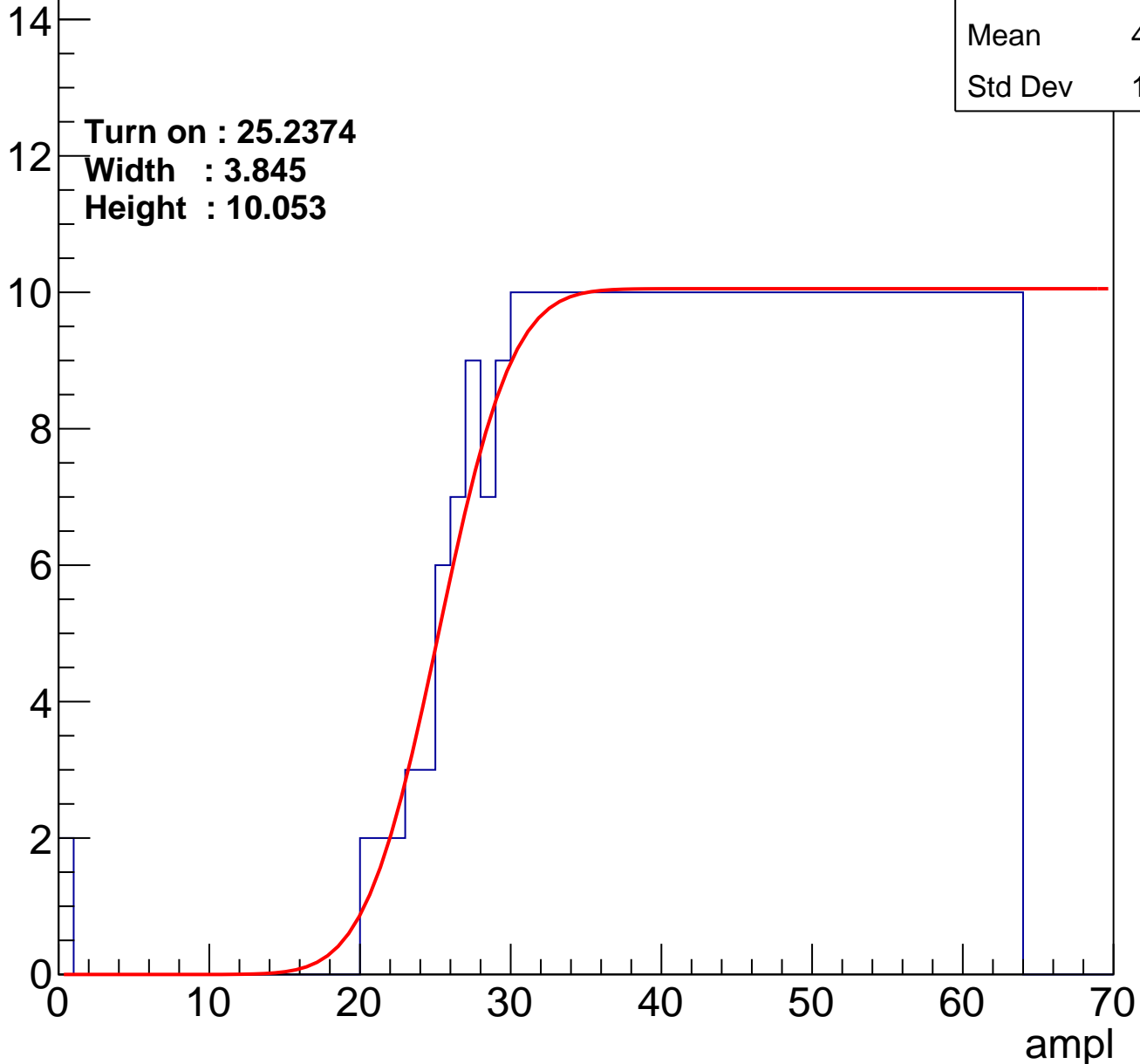
Entries	392
Mean	43.65
Std Dev	11.87

Turn on : 25.2374

Width : 3.845

Height : 10.053

Entry



B1L101S, U17-ch26

calib_packv5_042523_0143.root, FC#0, port D2

Entries	387
Mean	44
Std Dev	11.5

Turn on : 26.9384

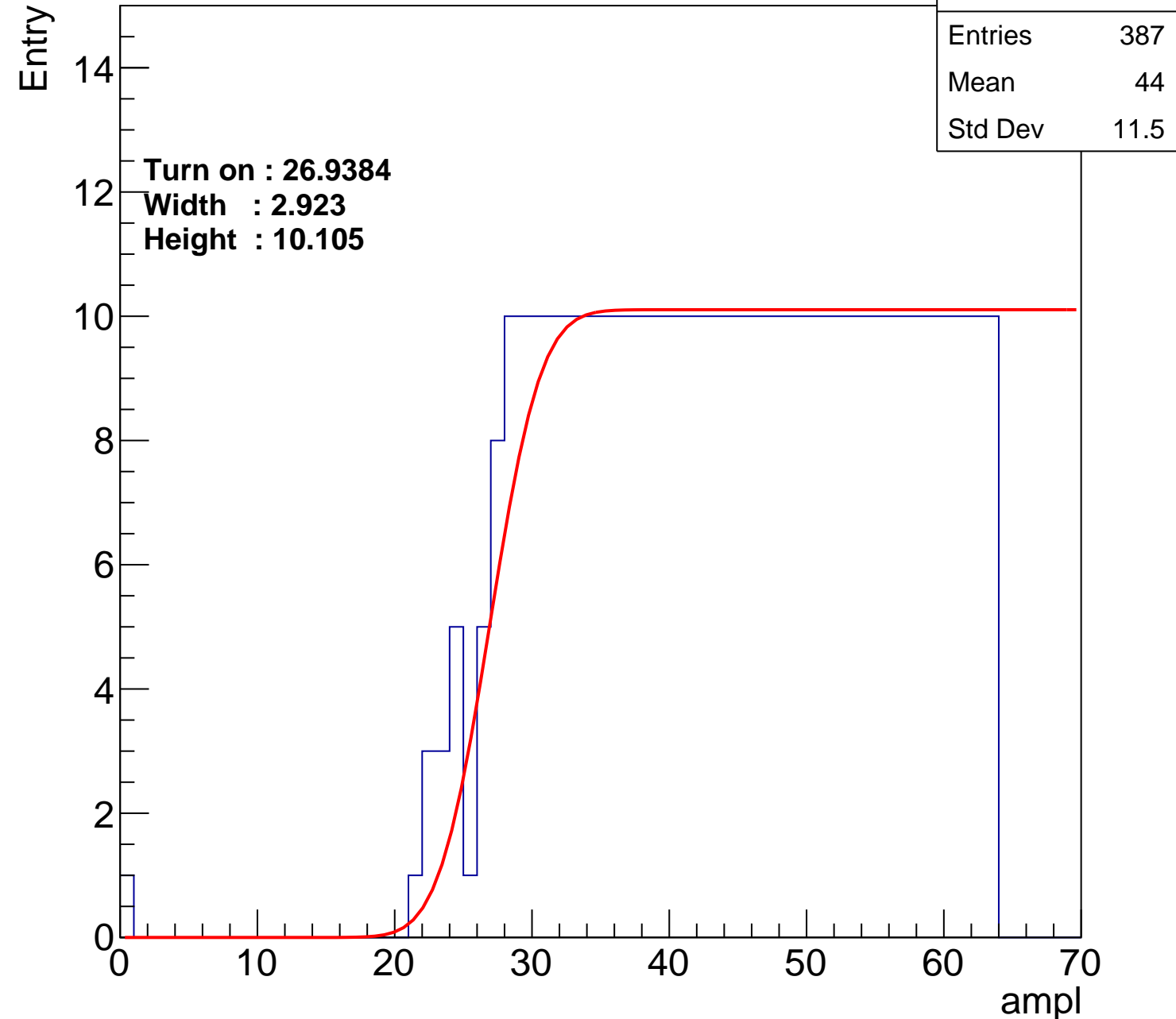
Width : 2.923

Height : 10.105

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U17-ch27

calib_packv5_042523_0143.root, FC#0, port D2

Entries	359
Mean	45.22
Std Dev	11.21

Turn on : 28.6363

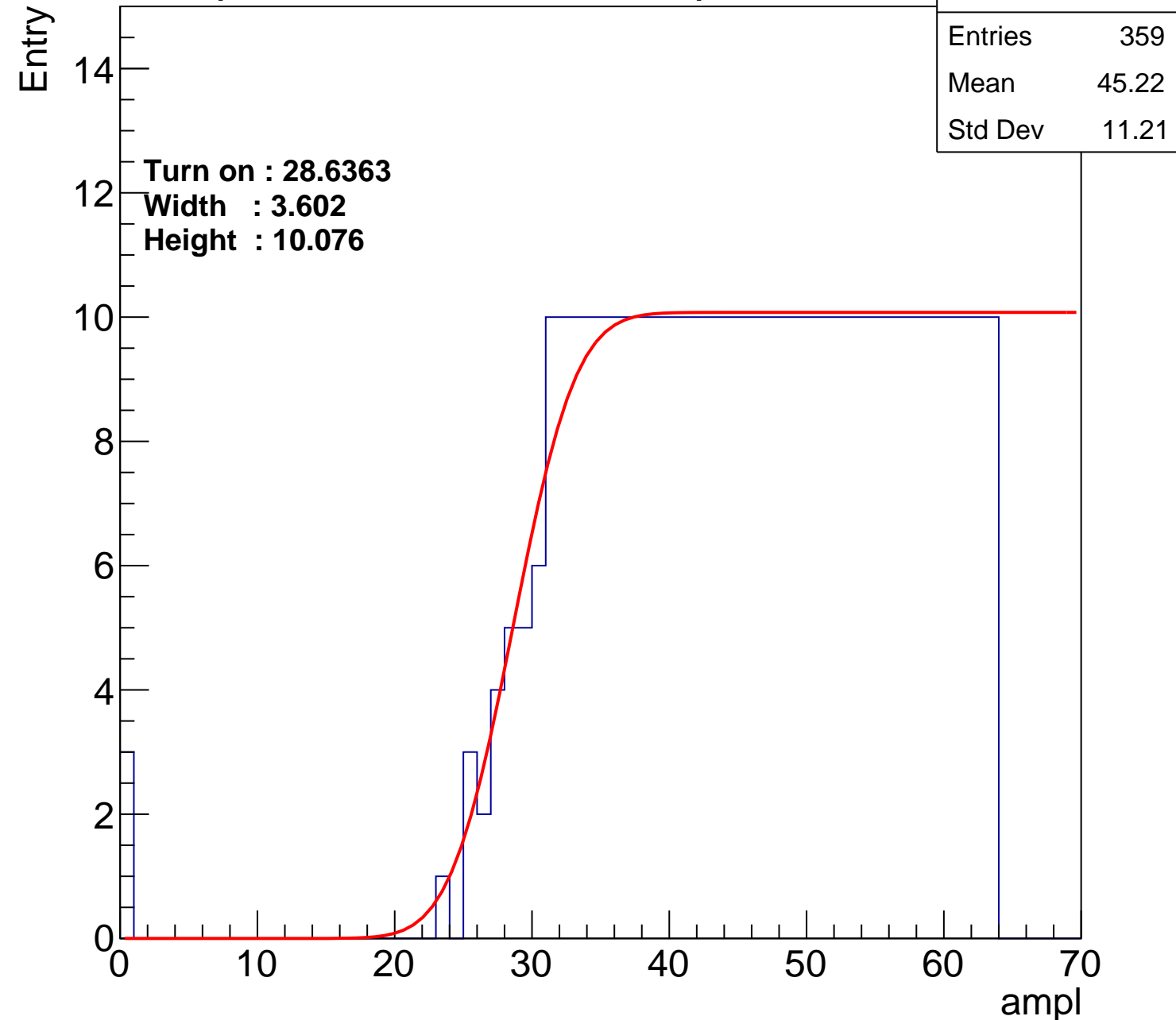
Width : 3.602

Height : 10.076

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U17-ch28

calib_packv5_042523_0143.root, FC#0, port D2

Entries	394
Mean	43.44
Std Dev	12.21

Turn on : 25.3455

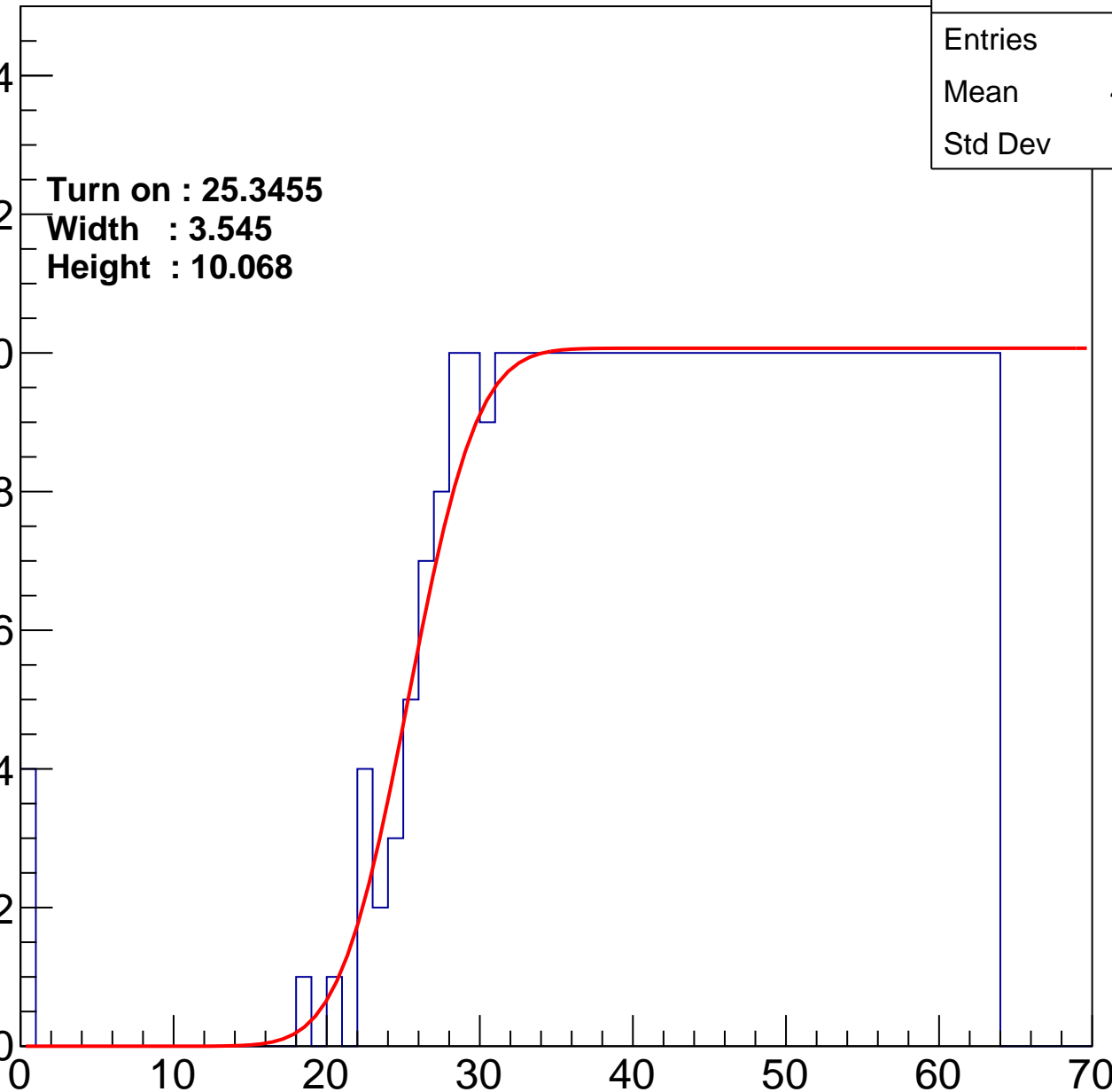
Width : 3.545

Height : 10.068

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U17-ch29

calib_packv5_042523_0143.root, FC#0, port D2

Entries	380
Mean	44.09
Std Dev	11.93

Turn on : 26.9942

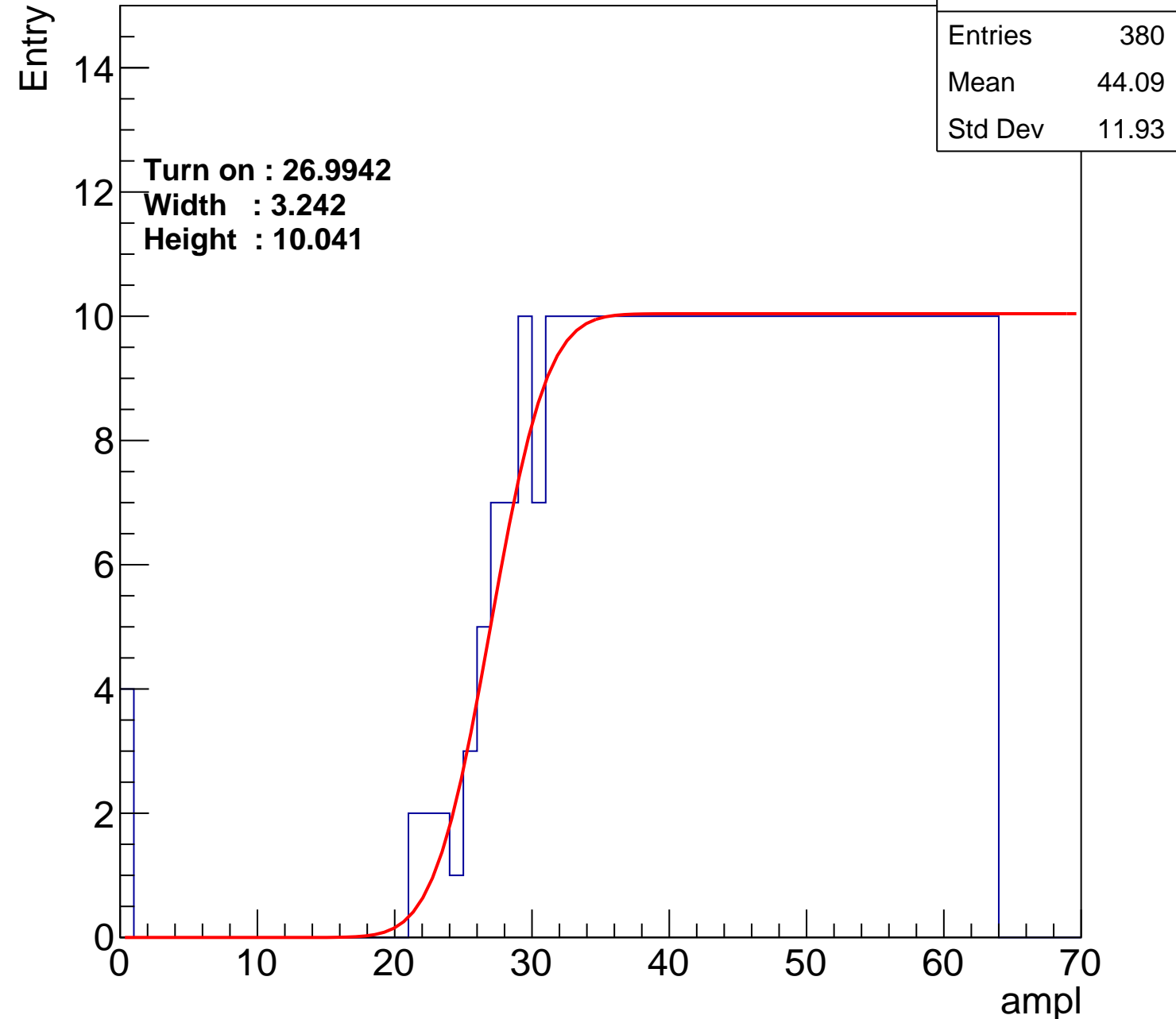
Width : 3.242

Height : 10.041

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U17-ch30

calib_packv5_042523_0143.root, FC#0, port D2

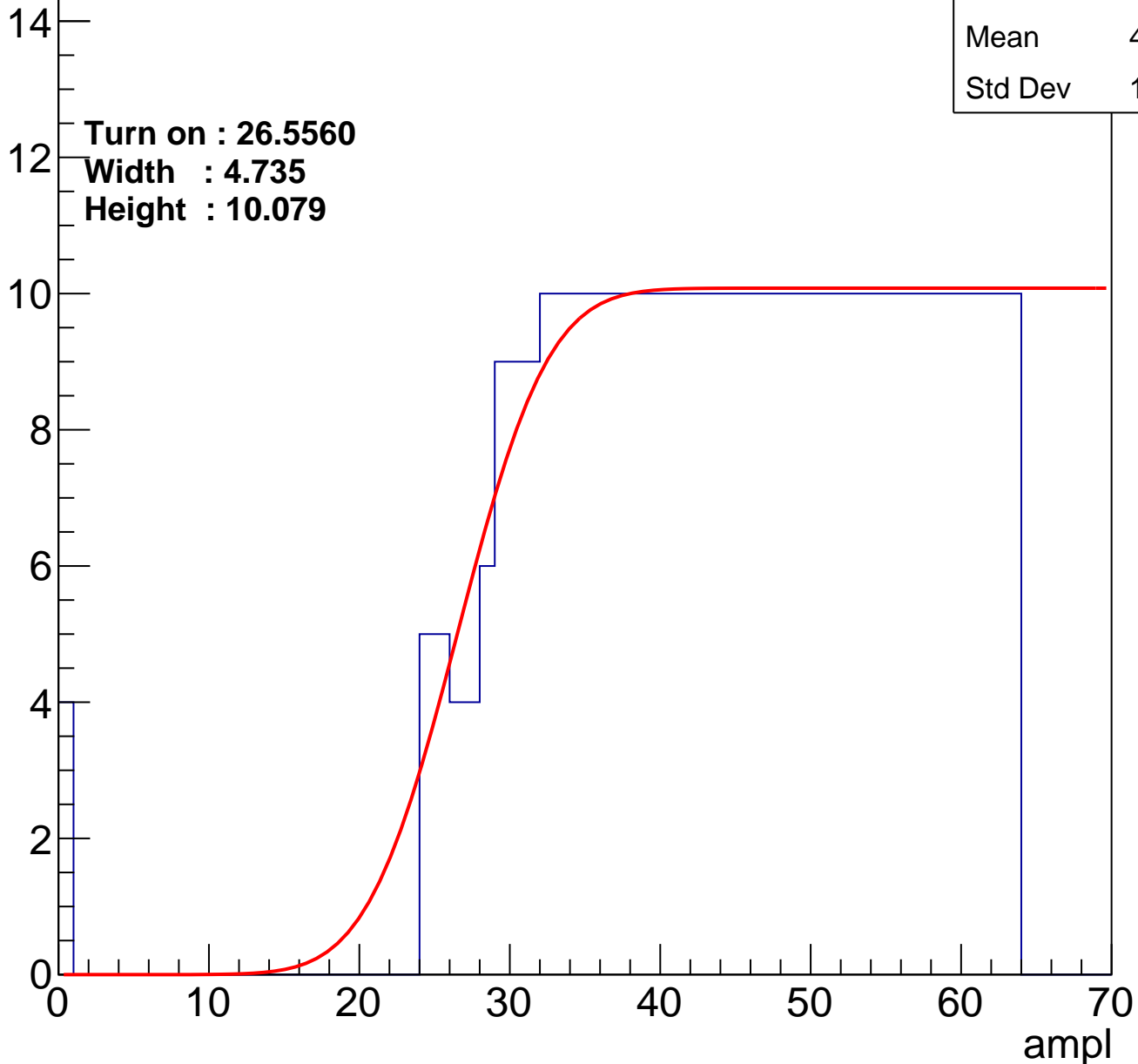
Entries	375
Mean	44.36
Std Dev	11.78

Turn on : 26.5560

Width : 4.735

Height : 10.079

Entry



B1L101S, U17-ch31

calib_packv5_042523_0143.root, FC#0, port D2

Entries	364
Mean	45.03
Std Dev	11.14

Turn on : 28.1326

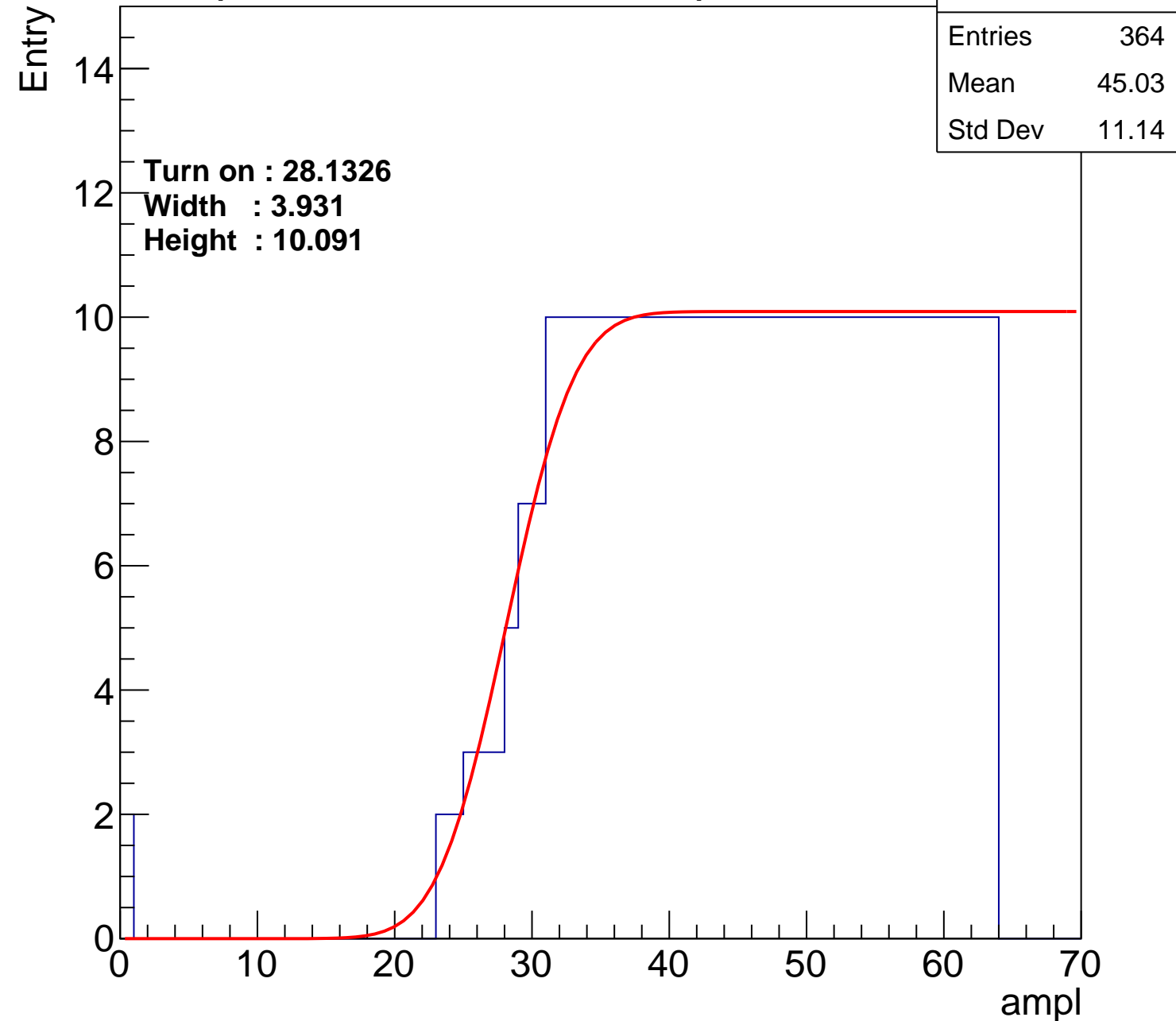
Width : 3.931

Height : 10.091

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U17-ch32

calib_packv5_042523_0143.root, FC#0, port D2

Entries	374
Mean	44.42
Std Dev	11.74

Turn on : 27.5442

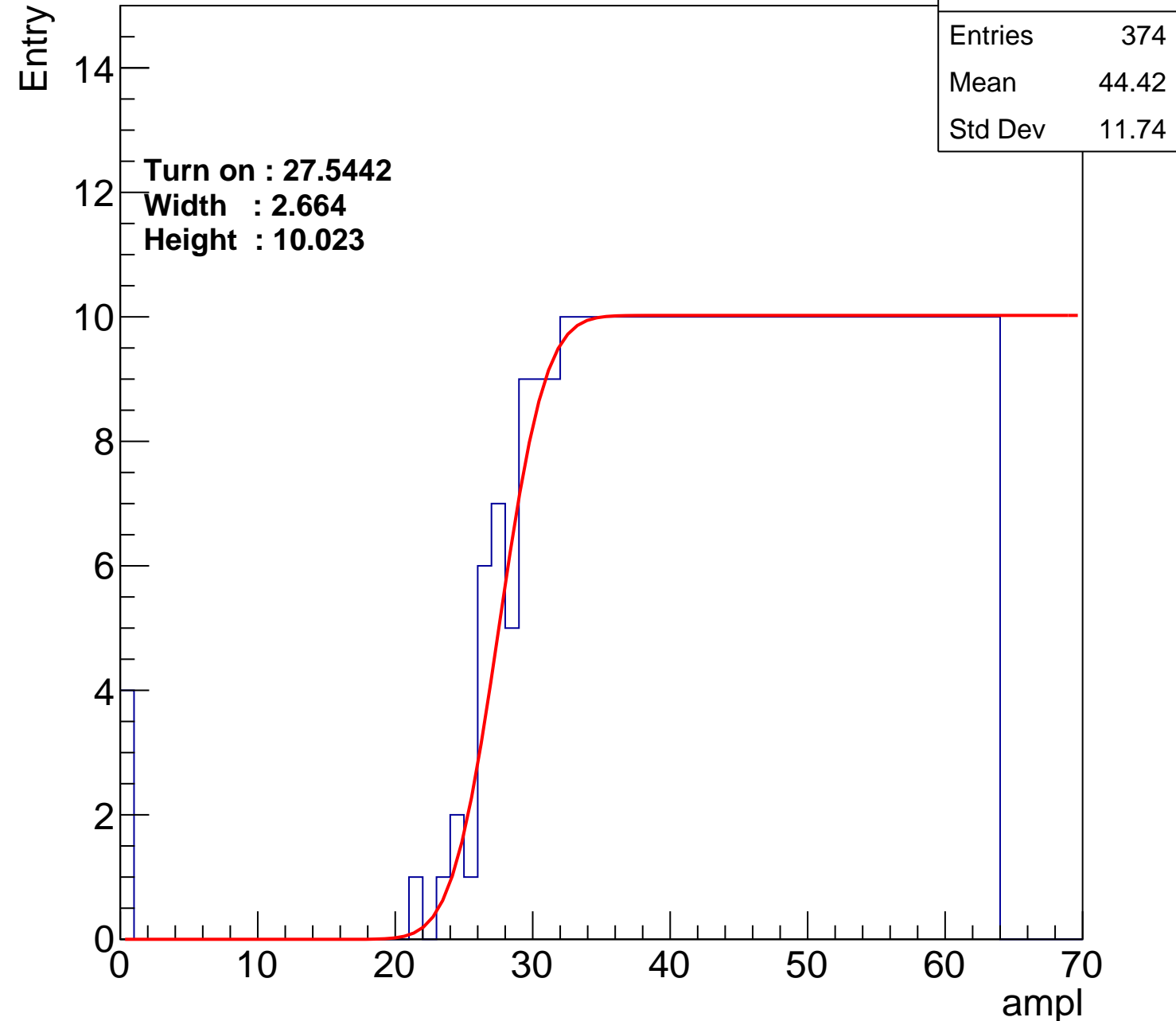
Width : 2.664

Height : 10.023

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U17-ch33

calib_packv5_042523_0143.root, FC#0, port D2

Entries	368
Mean	44.66
Std Dev	11.77

Turn on : 27.9406

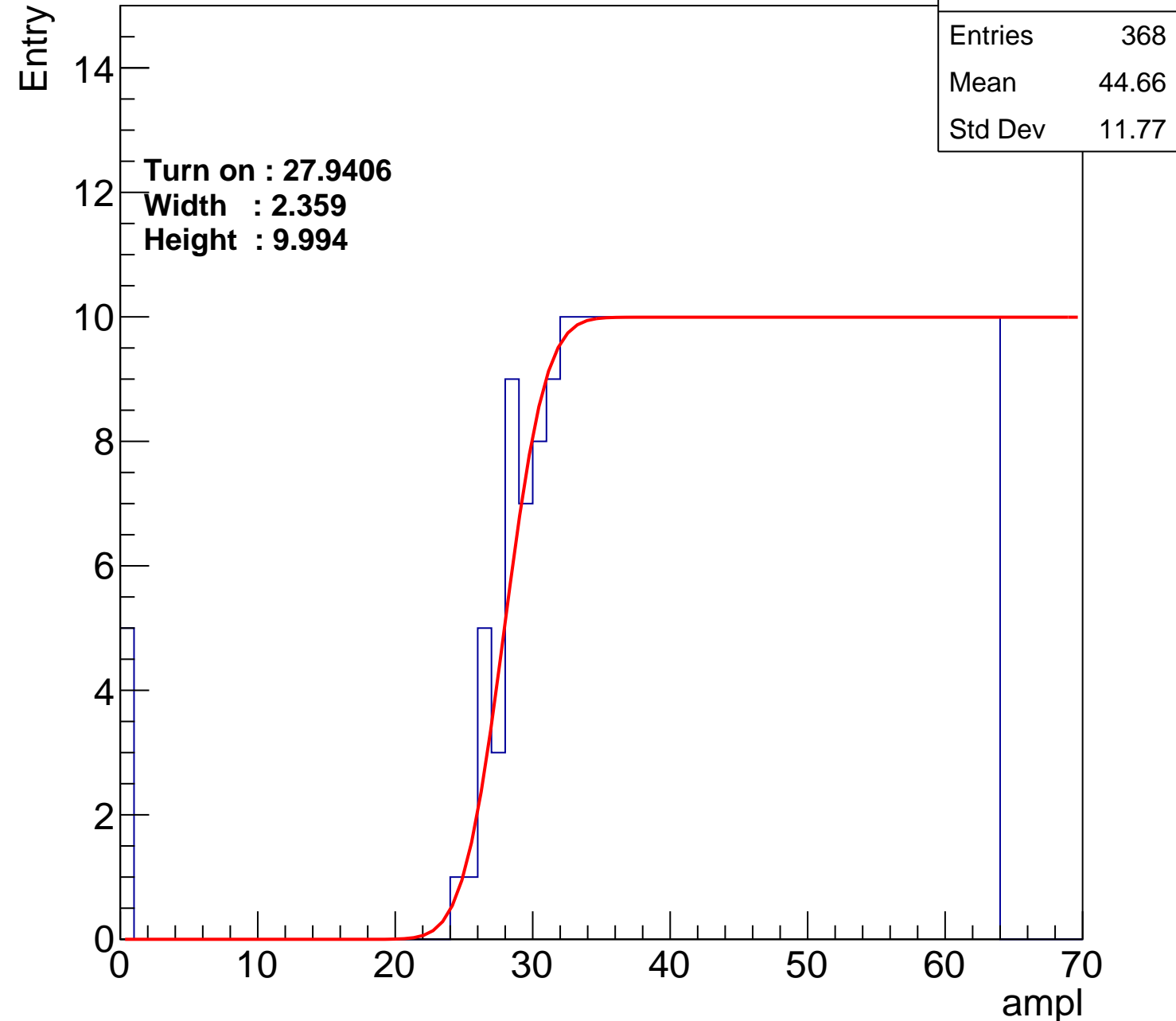
Width : 2.359

Height : 9.994

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U17-ch34

calib_packv5_042523_0143.root, FC#0, port D2

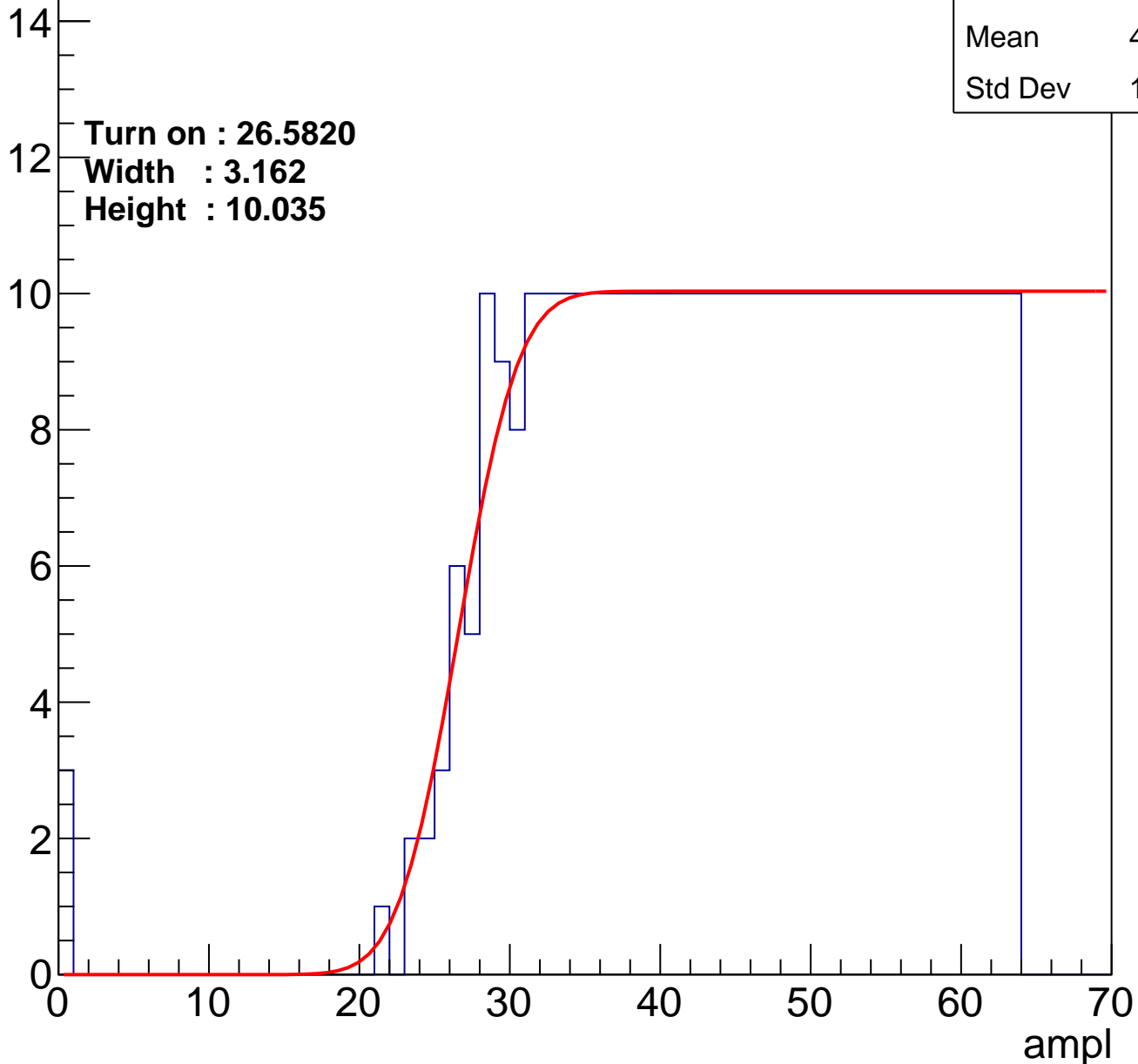
Entries	379
Mean	44.25
Std Dev	11.66

Turn on : 26.5820

Width : 3.162

Height : 10.035

Entry



B1L101S, U17-ch35

calib_packv5_042523_0143.root, FC#0, port D2

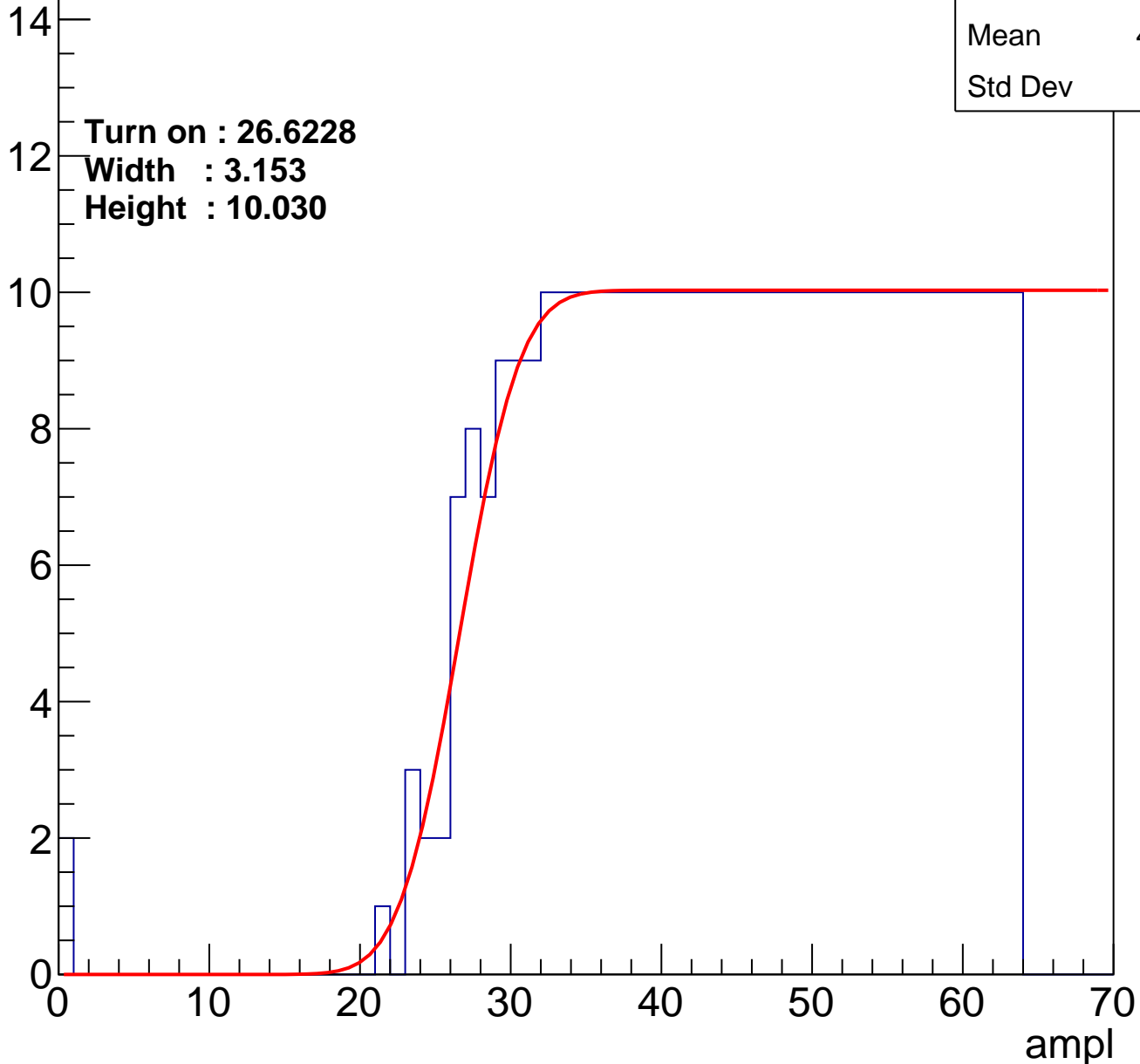
Entries	379
Mean	44.31
Std Dev	11.5

Turn on : 26.6228

Width : 3.153

Height : 10.030

Entry



B1L101S, U17-ch36

calib_packv5_042523_0143.root, FC#0, port D2

Entries	372
Mean	44.65
Std Dev	11.32

Turn on : 27.4045

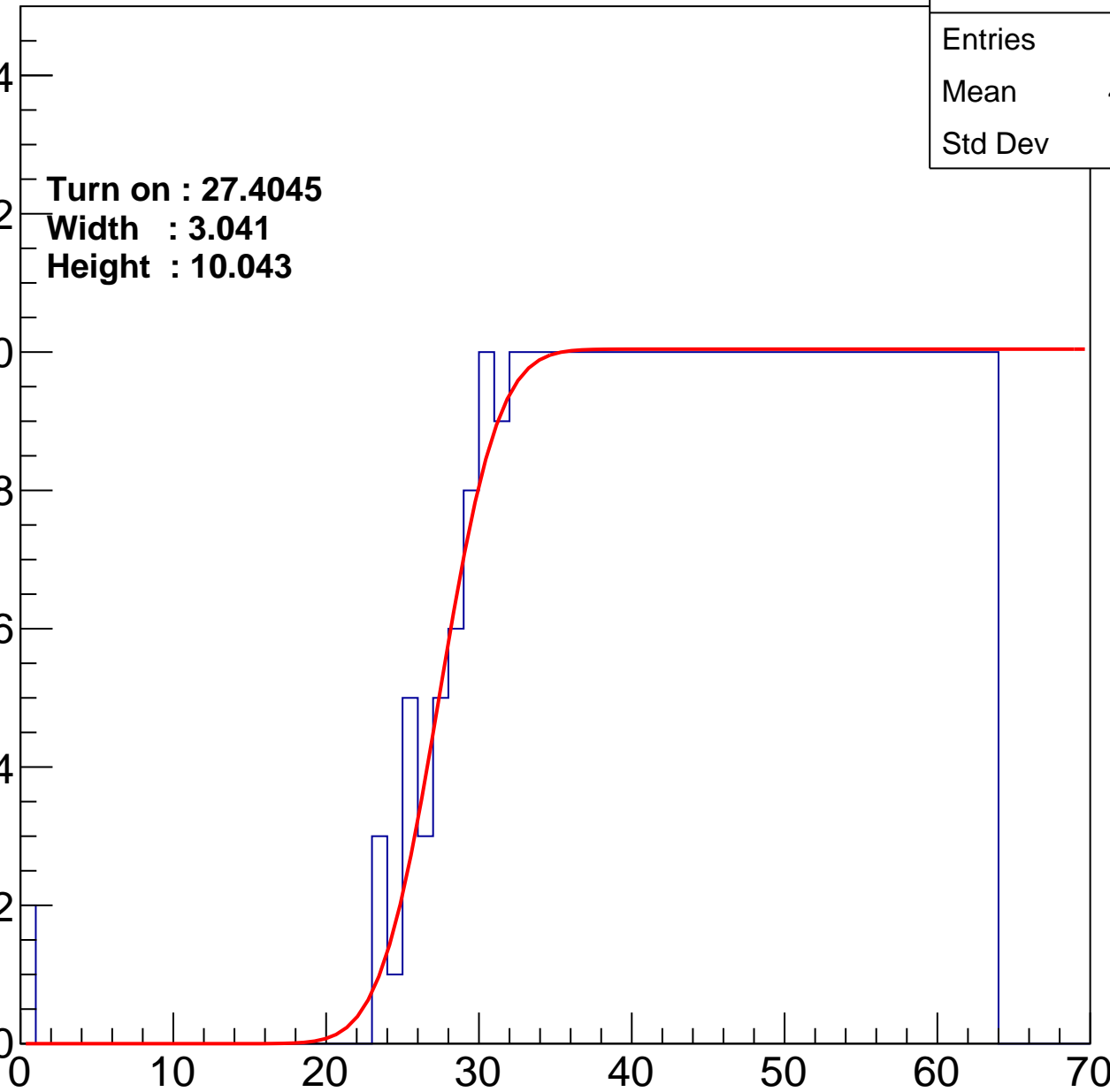
Width : 3.041

Height : 10.043

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U17-ch37

calib_packv5_042523_0143.root, FC#0, port D2

Entries	370
Mean	44.55
Std Dev	11.82

Turn on : 28.1840

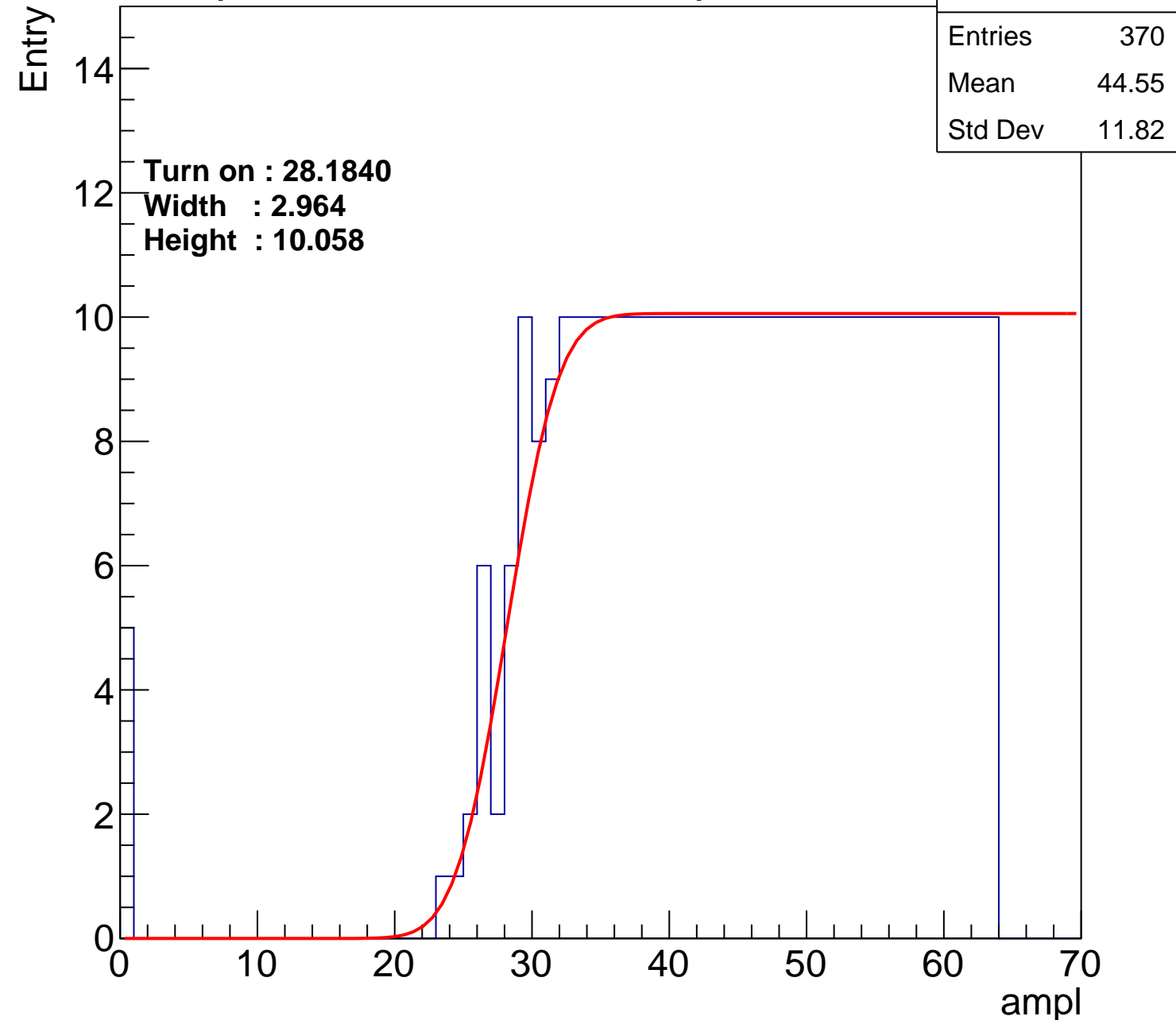
Width : 2.964

Height : 10.058

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U17-ch38

calib_packv5_042523_0143.root, FC#0, port D2

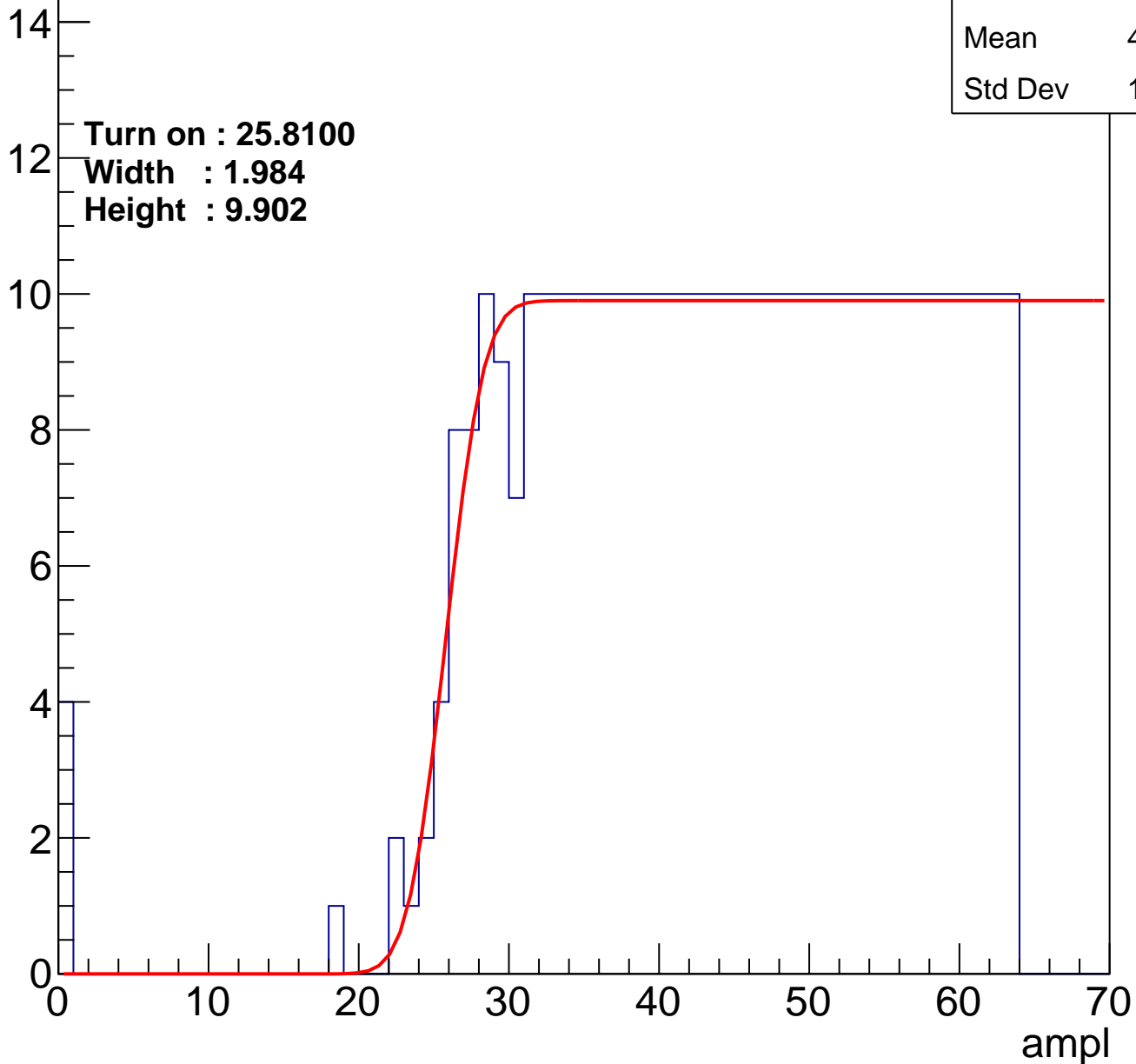
Entries	386
Mean	43.83
Std Dev	12.02

Turn on : 25.8100

Width : 1.984

Height : 9.902

Entry



B1L101S, U17-ch39

calib_packv5_042523_0143.root, FC#0, port D2

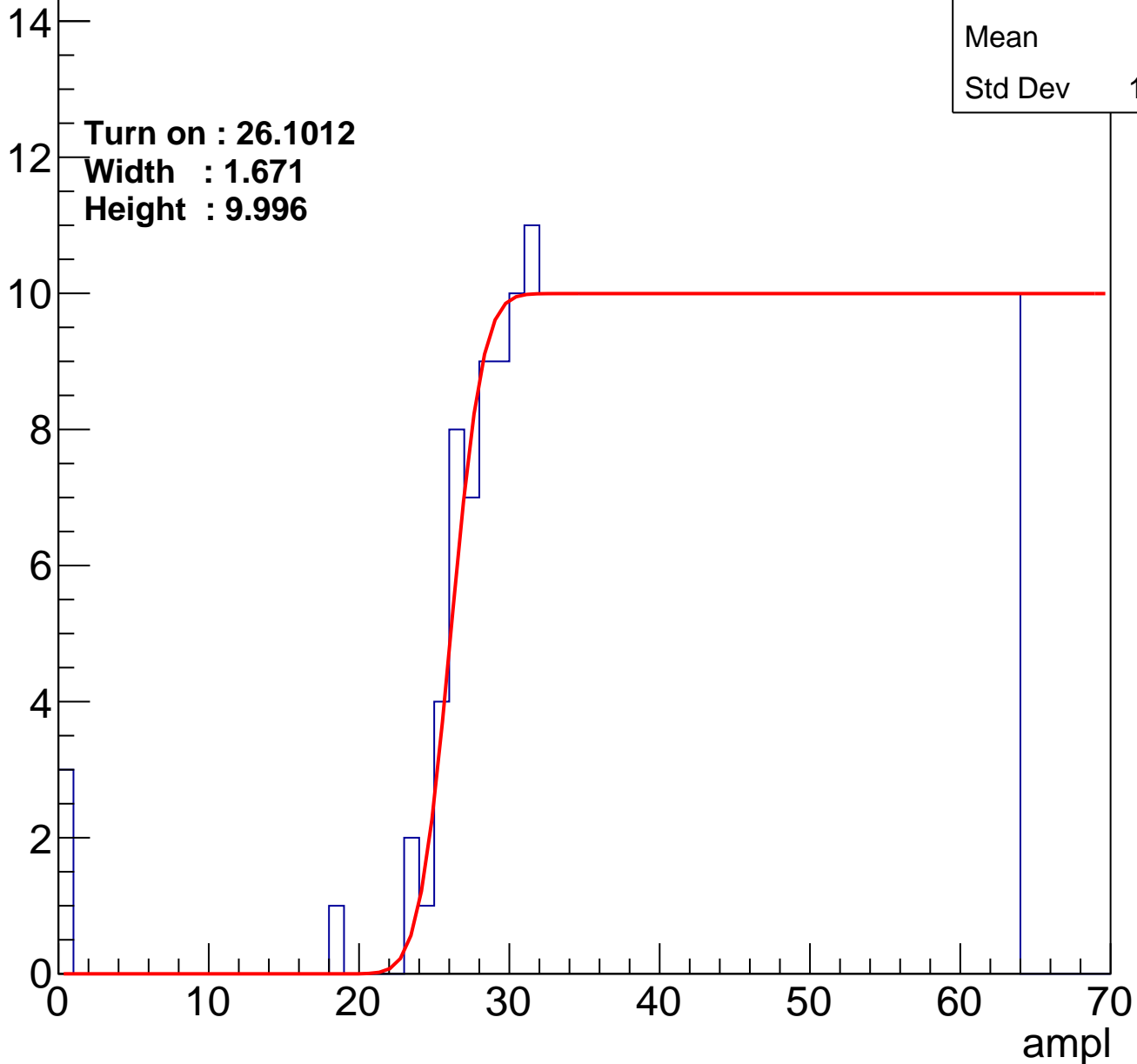
Entries	385
Mean	44
Std Dev	11.75

Turn on : 26.1012

Width : 1.671

Height : 9.996

Entry



calib_packv5_042523_0143.root, FC#0, port D2

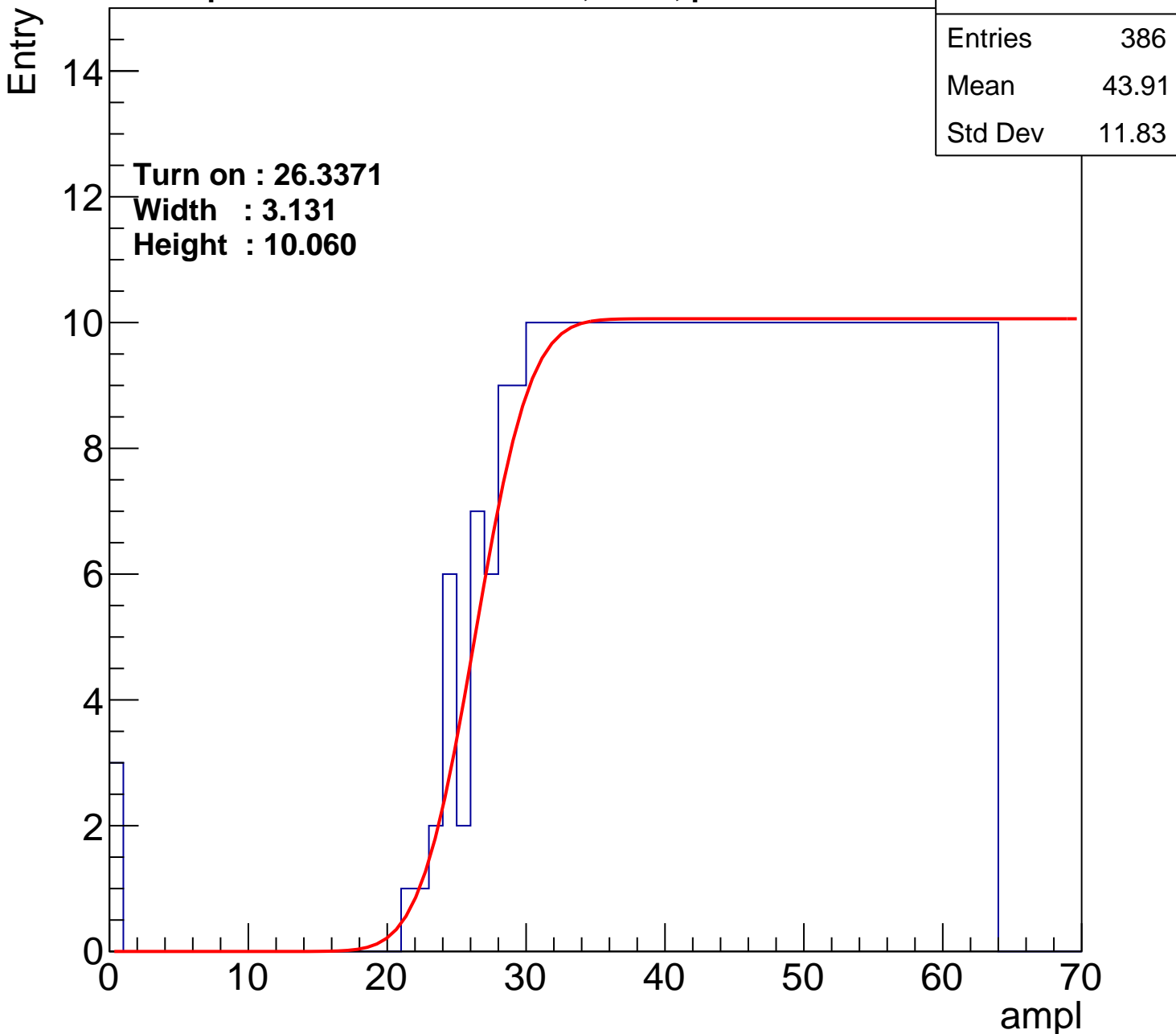
Entries	386
Mean	43.91
Std Dev	11.83

Mean	43.91
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Std Dev	11.83
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Width : 3.131

Height : 10.060



B1L101S, U17-ch41

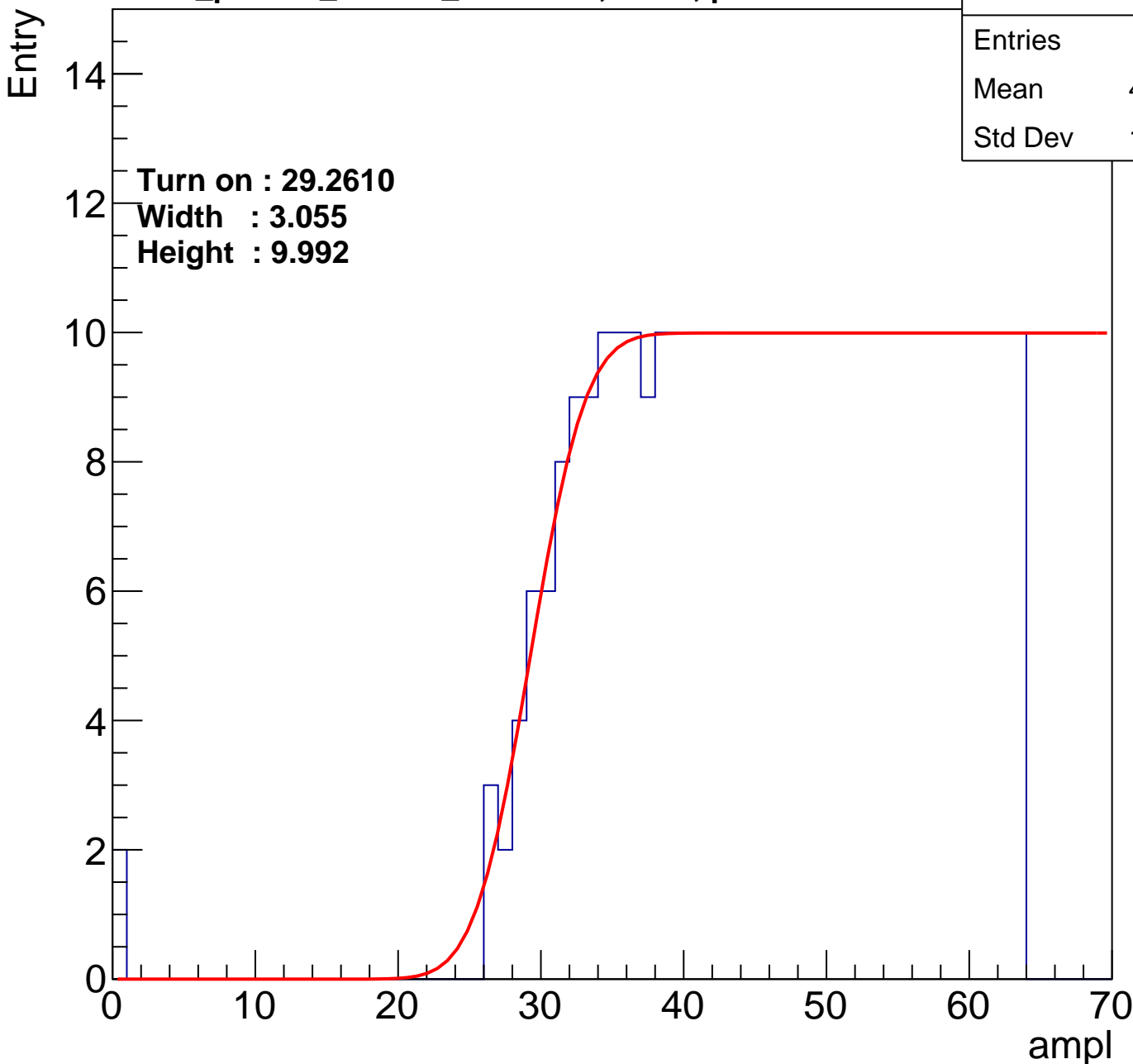
calib_packv5_042523_0143.root, FC#0, port D2

Entries	348
Mean	45.82
Std Dev	10.73

Turn on : 29.2610

Width : 3.055

Height : 9.992



B1L101S, U17-ch42

calib_packv5_042523_0143.root, FC#0, port D2

Entries	388
Mean	43.77
Std Dev	11.94

Turn on : 25.8792

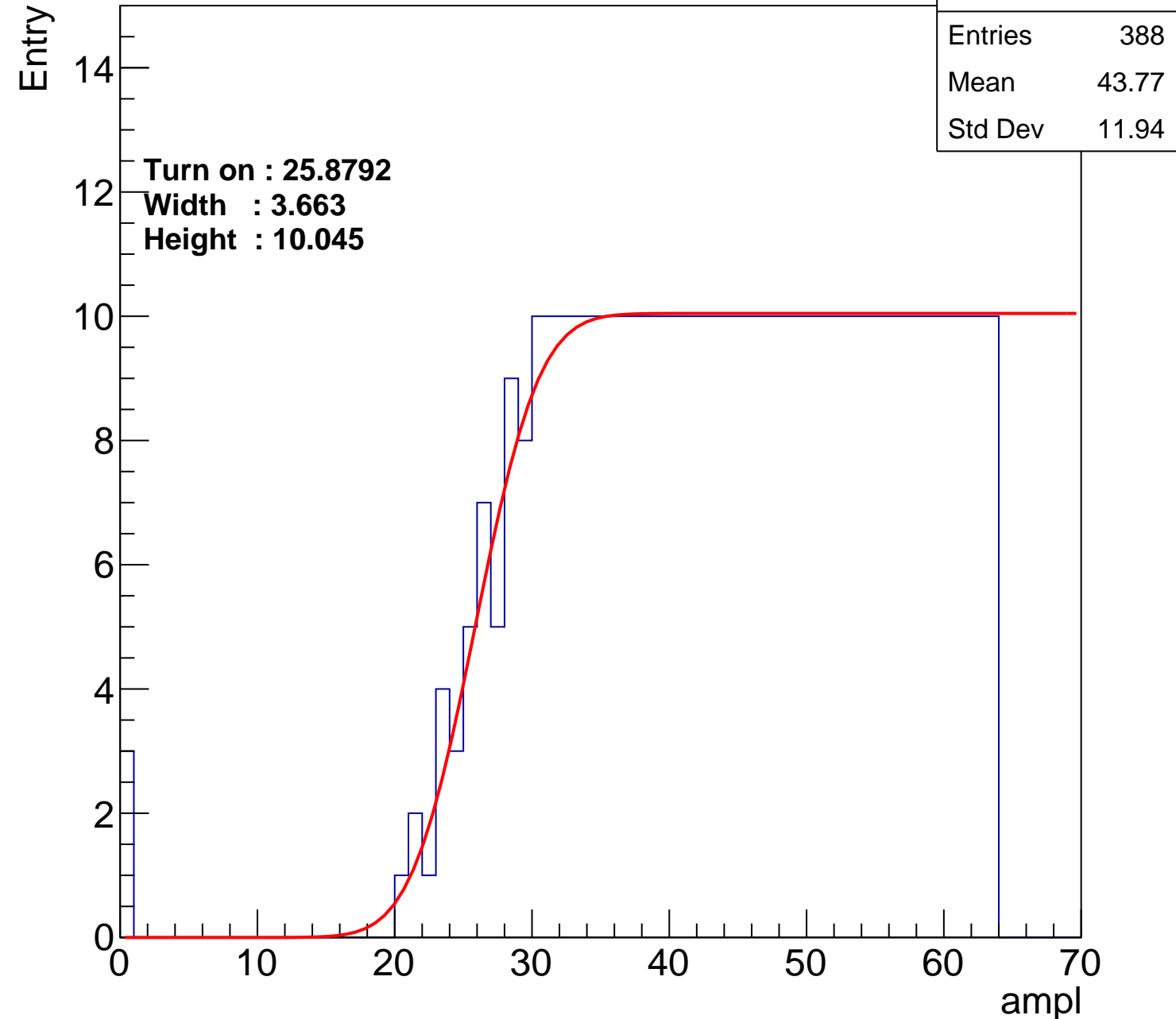
Width : 3.663

Height : 10.045

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U17-ch43

calib_packv5_042523_0143.root, FC#0, port D2

Entries	375
Mean	44.59
Std Dev	11.17

Turn on : 26.7707

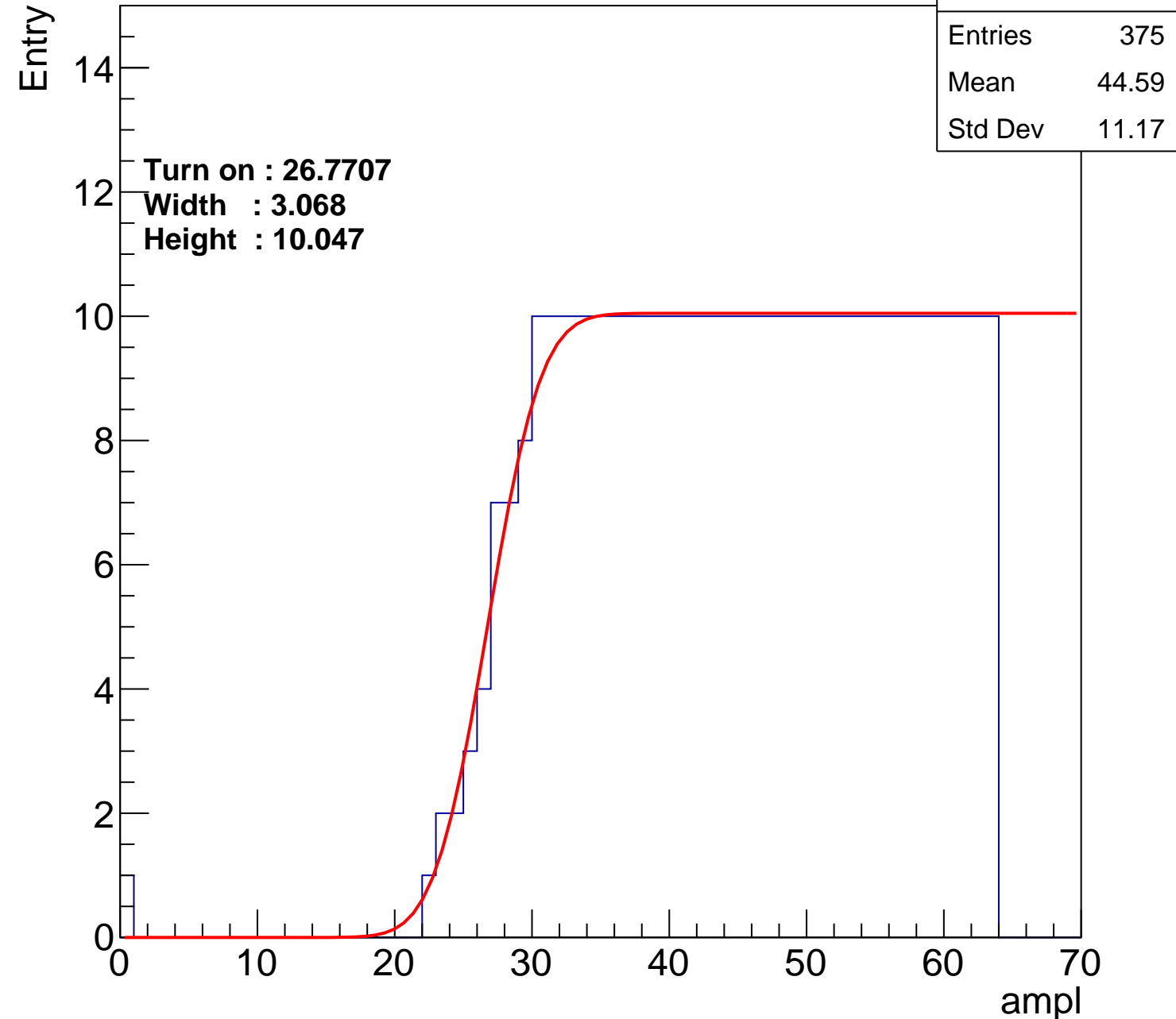
Width : 3.068

Height : 10.047

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U17-ch44

calib_packv5_042523_0143.root, FC#0, port D2

Entries	378
Mean	44.19
Std Dev	11.89

Turn on : 27.0669

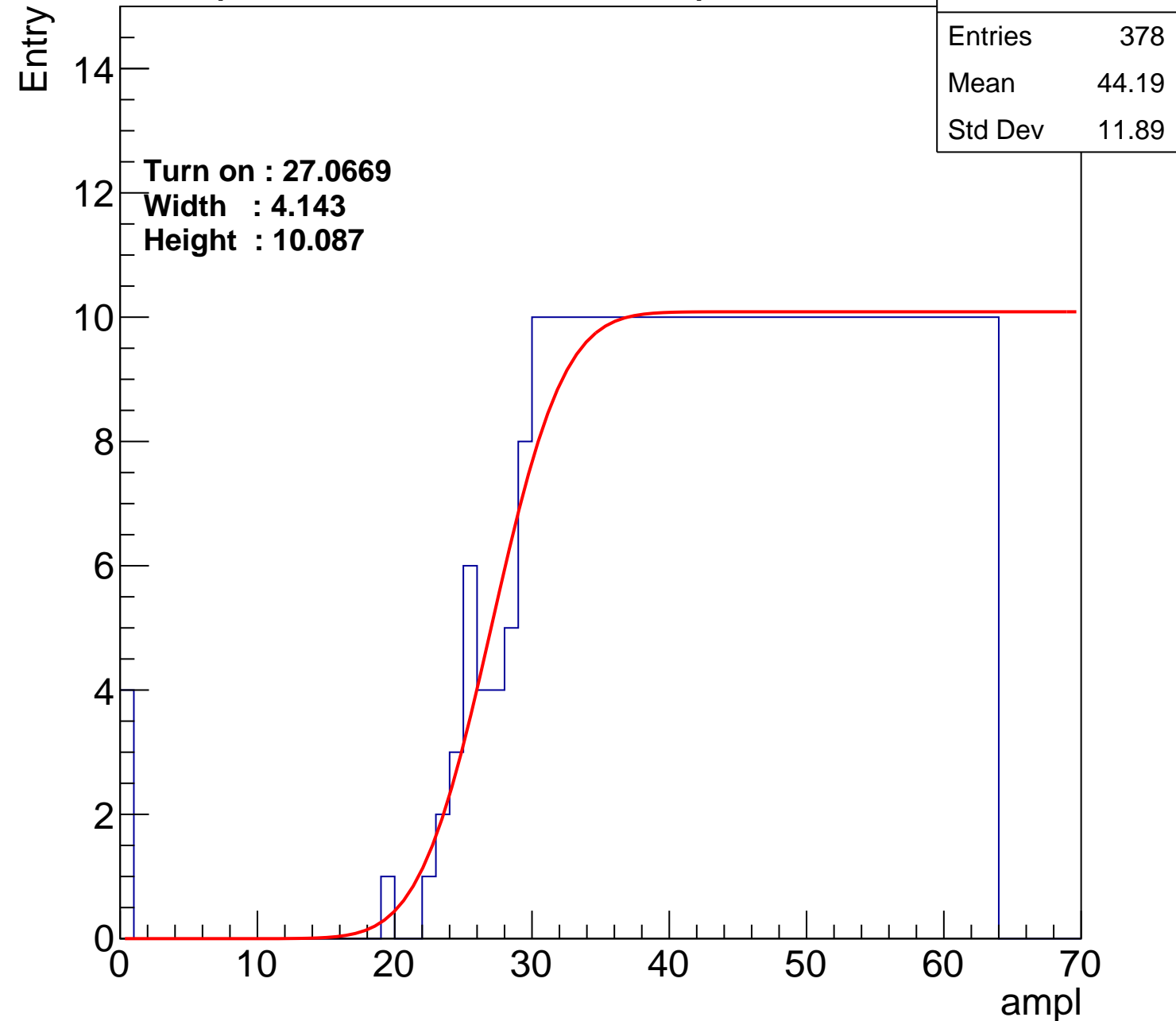
Width : 4.143

Height : 10.087

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U17-ch45

calib_packv5_042523_0143.root, FC#0, port D2

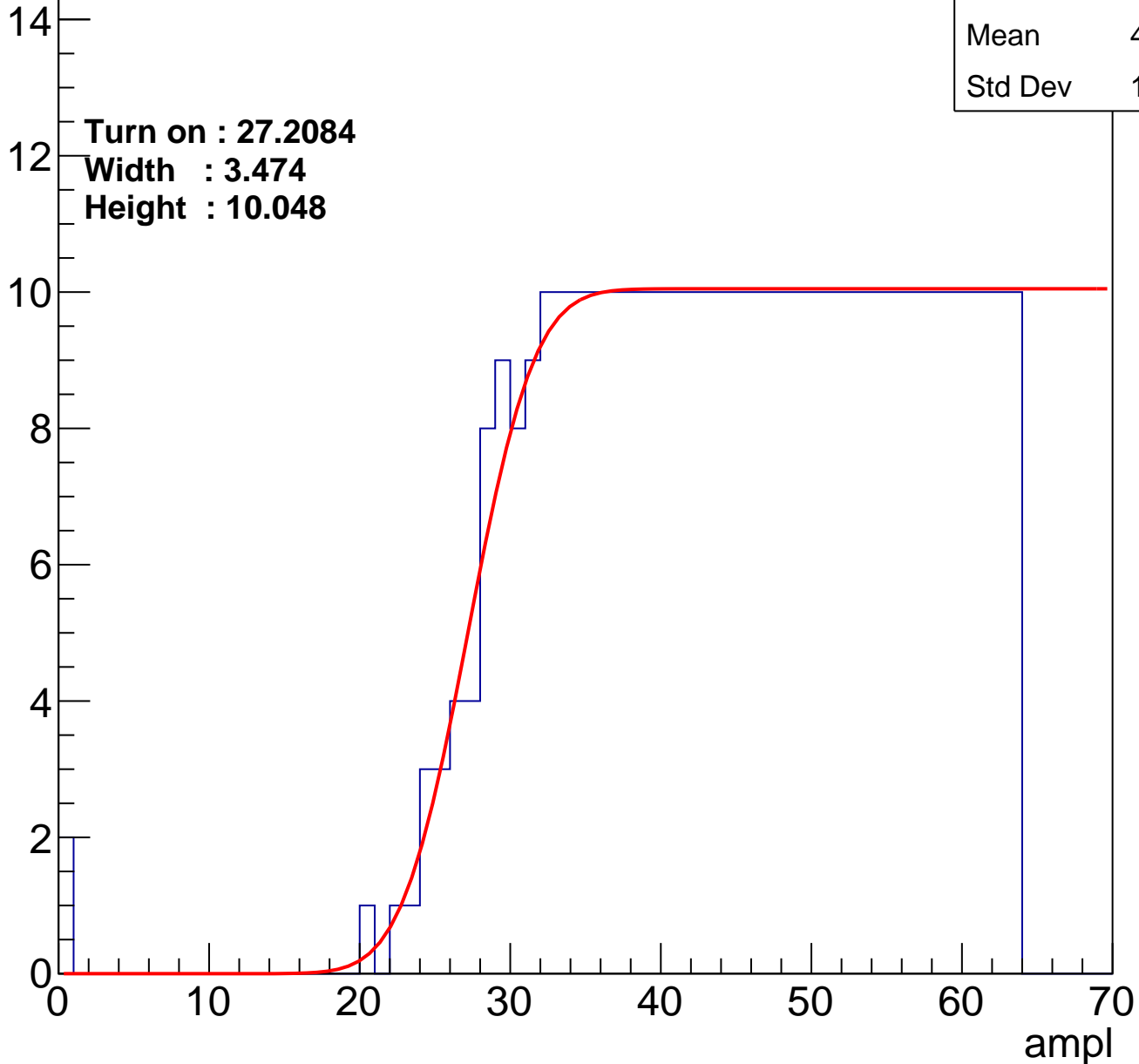
Entries	373
Mean	44.58
Std Dev	11.38

Turn on : 27.2084

Width : 3.474

Height : 10.048

Entry



B1L101S, U17-ch46

calib_packv5_042523_0143.root, FC#0, port D2

Entries	361
Mean	44.99
Std Dev	11.52

Turn on : 28.2888

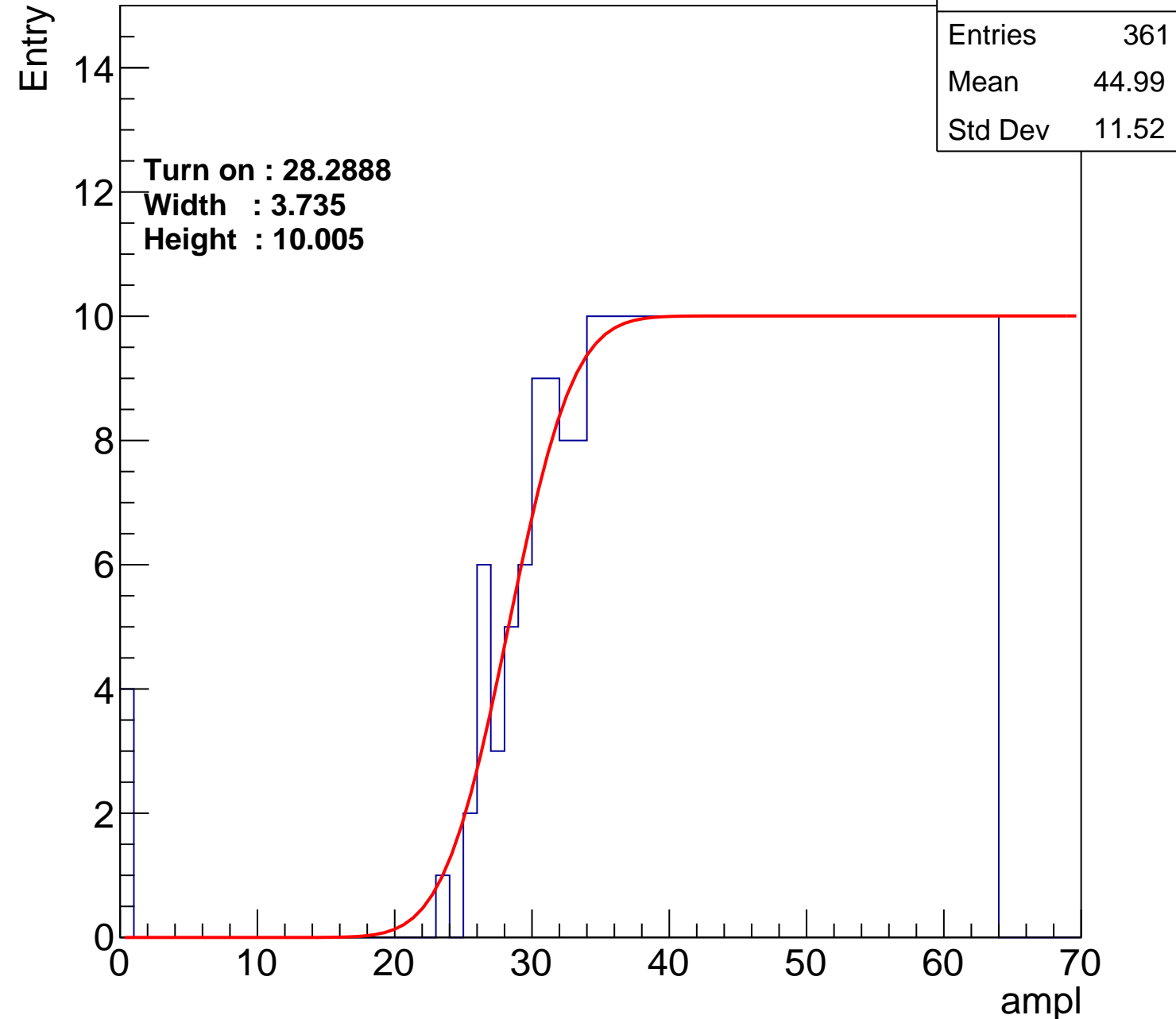
Width : 3.735

Height : 10.005

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U17-ch47

calib_packv5_042523_0143.root, FC#0, port D2

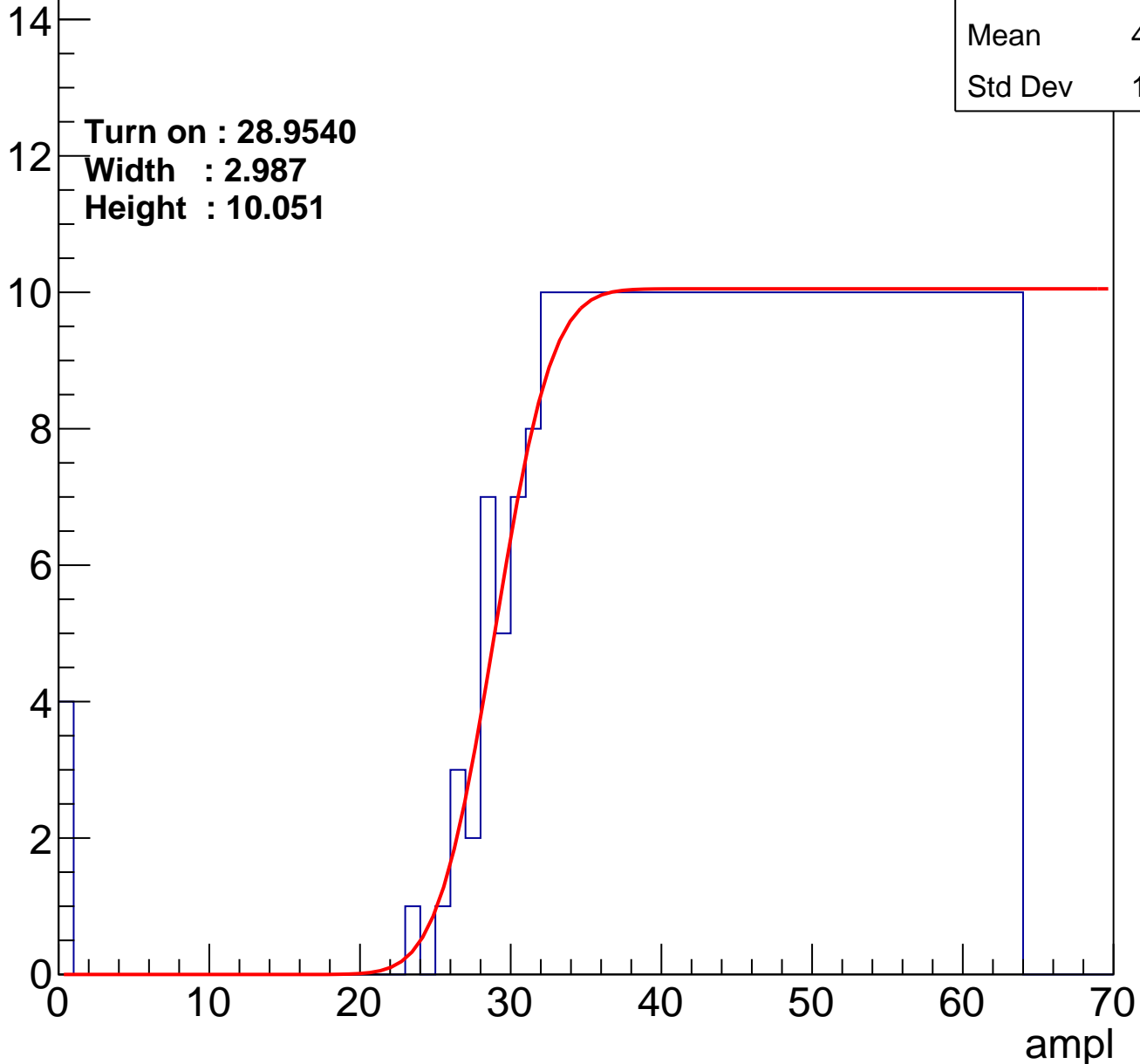
Entries	358
Mean	45.19
Std Dev	11.39

Turn on : 28.9540

Width : 2.987

Height : 10.051

Entry



B1L101S, U17-ch48

calib_packv5_042523_0143.root, FC#0, port D2

Entries	378
Mean	44.25
Std Dev	11.72

Turn on : 27.2255

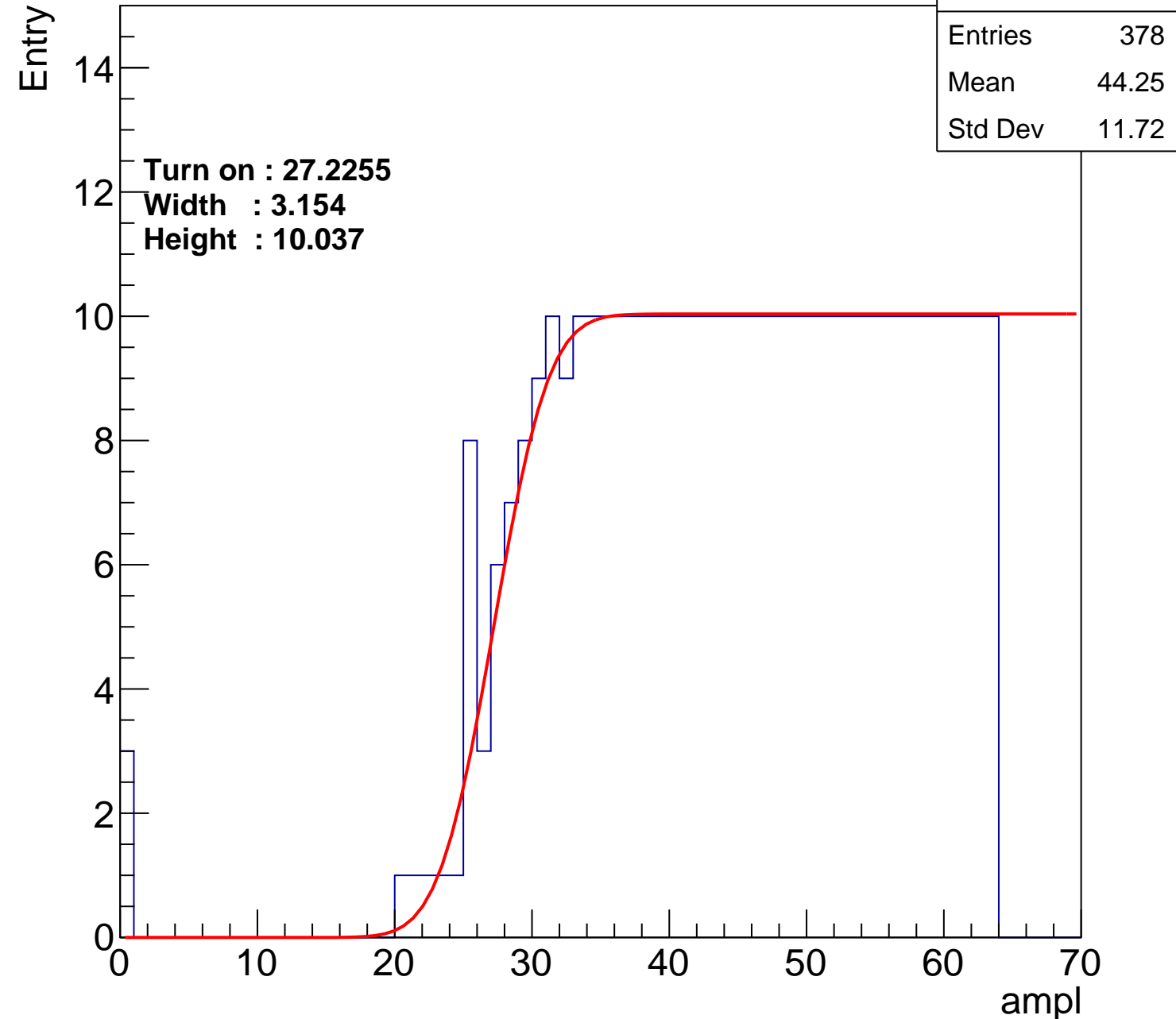
Width : 3.154

Height : 10.037

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U17-ch49

calib_packv5_042523_0143.root, FC#0, port D2

Entries	361
Mean	45.09
Std Dev	11.29

Turn on : 28.3615

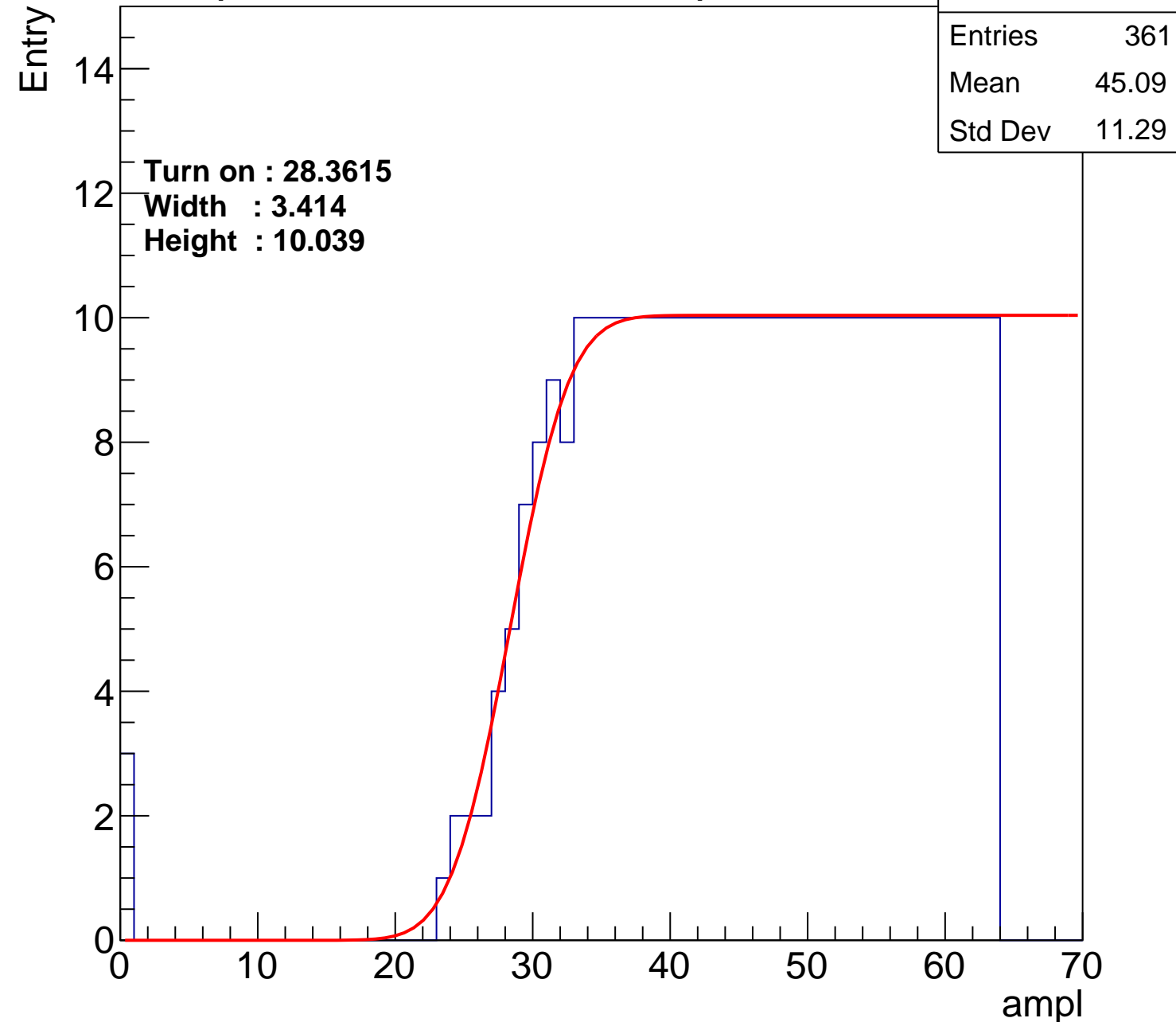
Width : 3.414

Height : 10.039

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U17-ch50

calib_packv5_042523_0143.root, FC#0, port D2

Entries	368
Mean	44.8
Std Dev	11.29

Turn on : 28.3039

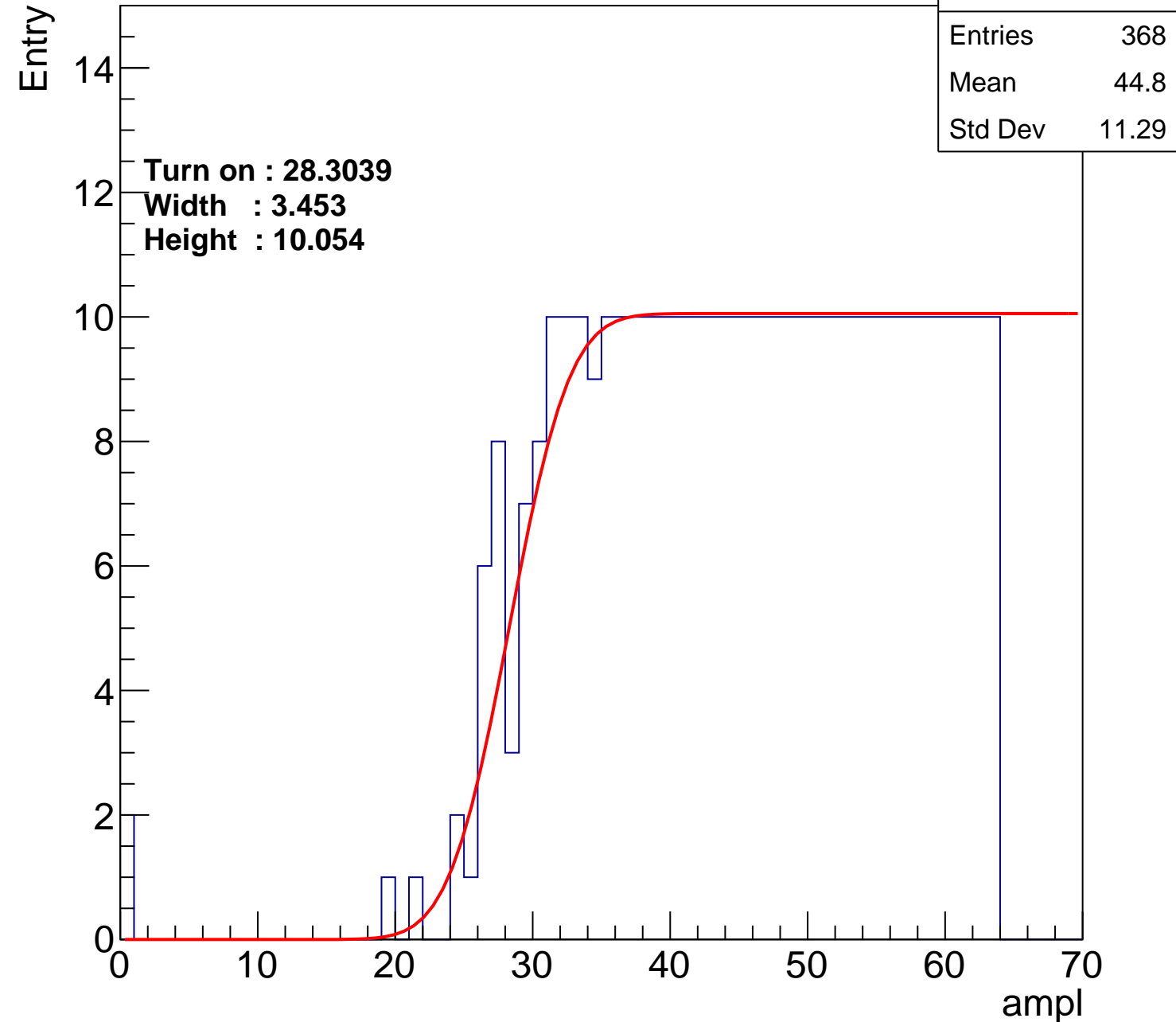
Width : 3.453

Height : 10.054

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U17-ch51

calib_packv5_042523_0143.root, FC#0, port D2

Entries	359
Mean	45.28
Std Dev	11

Turn on : 28.4010

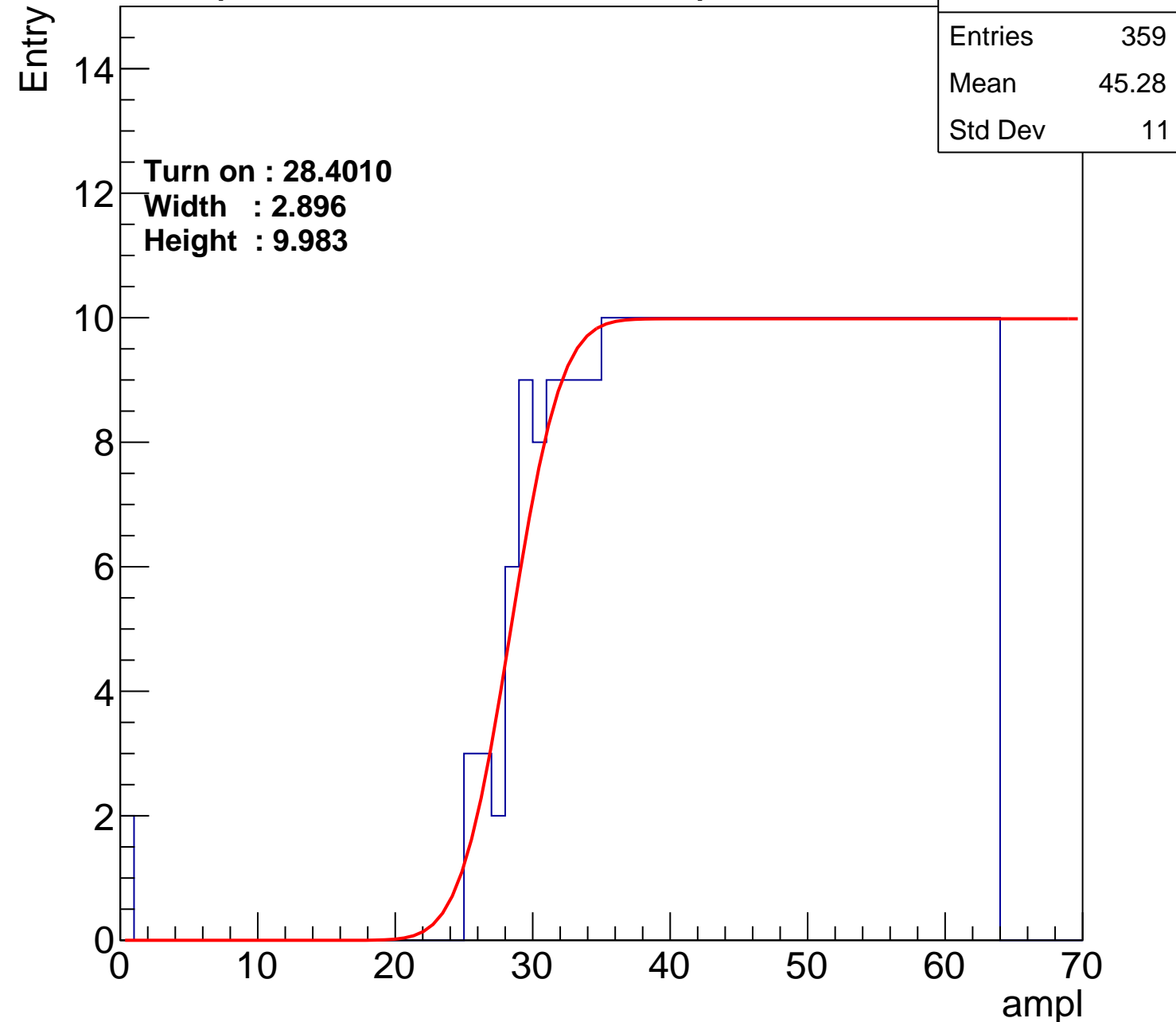
Width : 2.896

Height : 9.983

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U17-ch52

calib_packv5_042523_0143.root, FC#0, port D2

Entries	380
Mean	44.19
Std Dev	11.61

Turn on : 25.6727

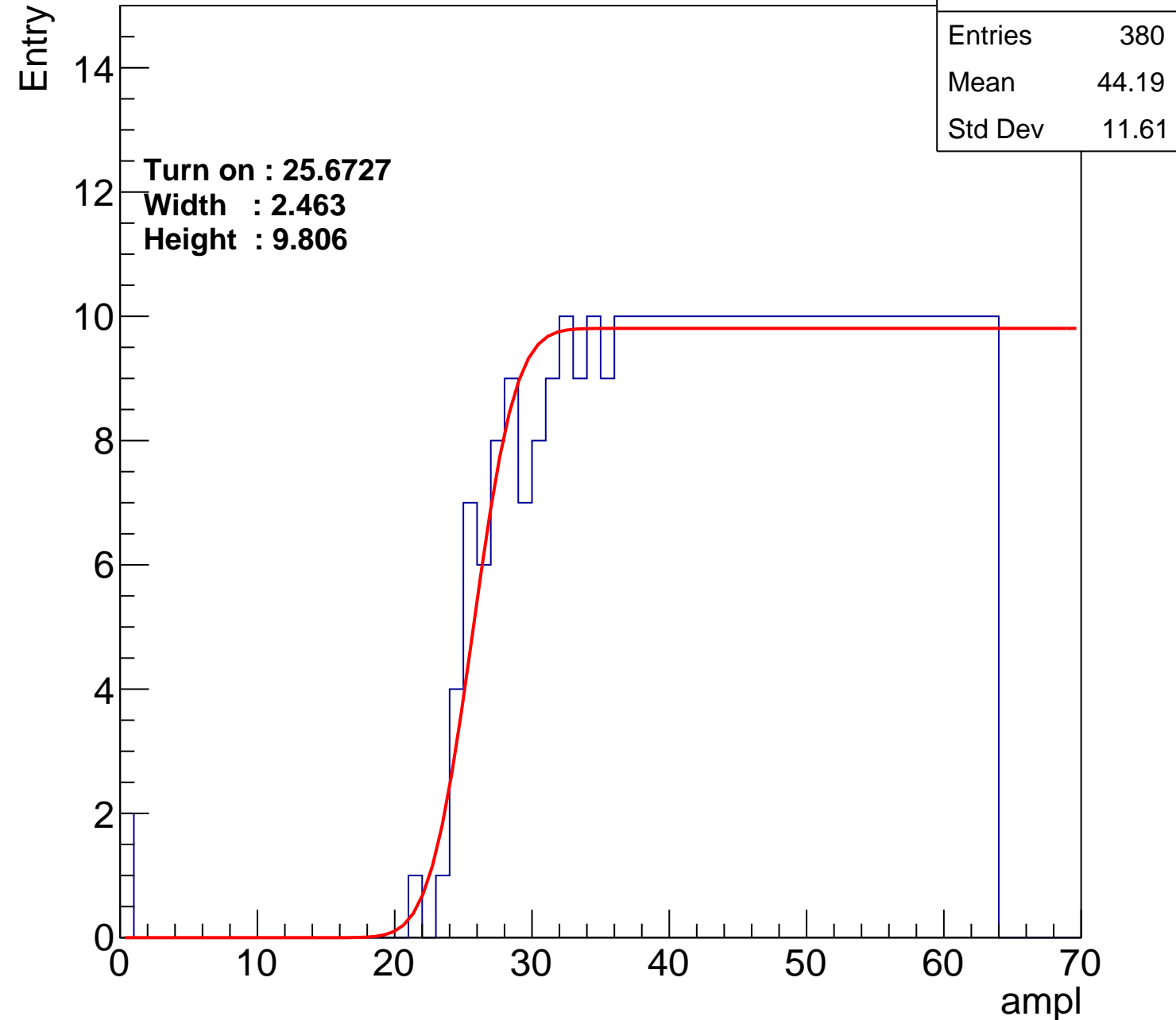
Width : 2.463

Height : 9.806

Entry

14
12
10
8
6
4
2
0

ampl



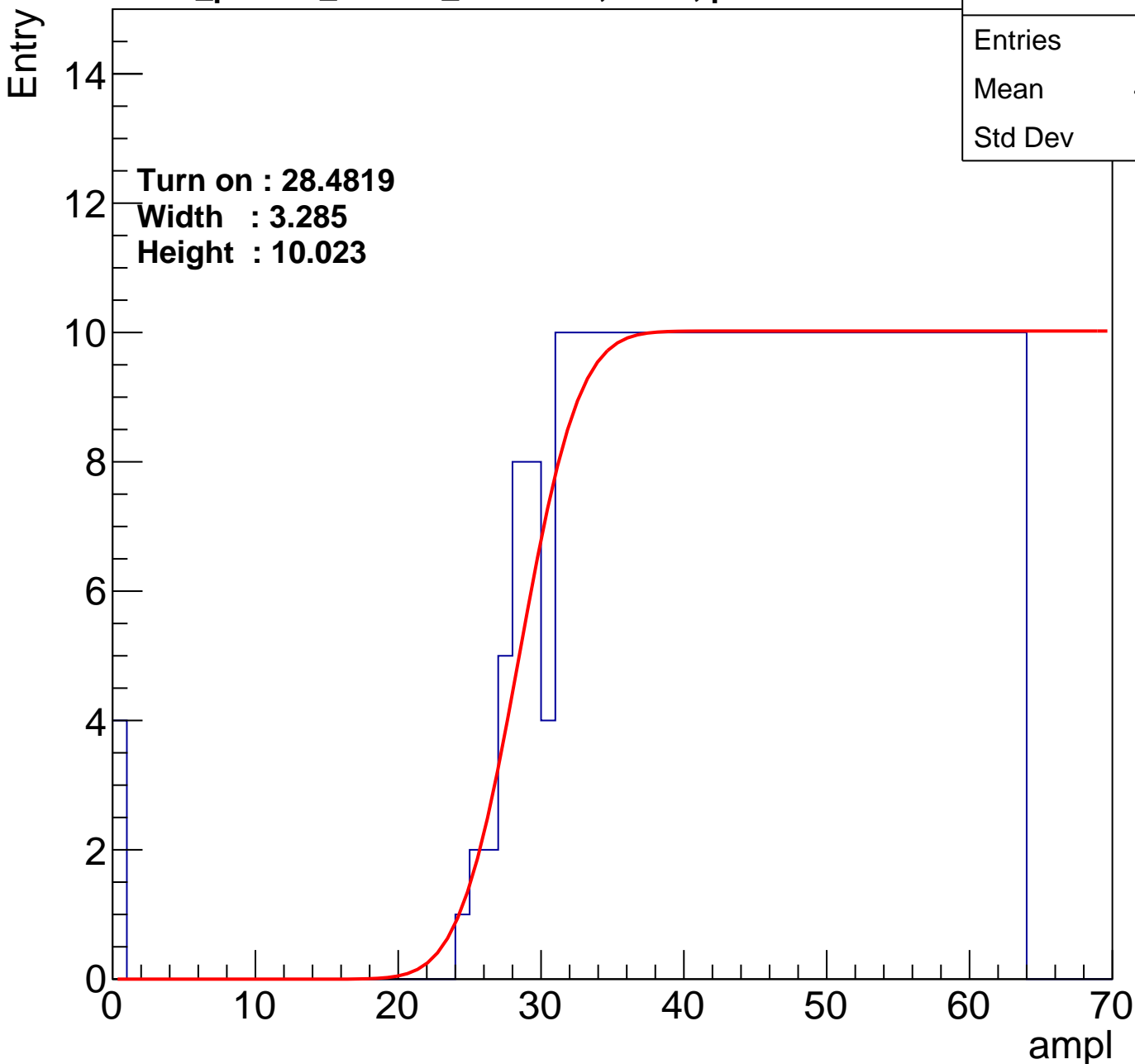
calib_packv5_042523_0143.root, FC#0, port D2

calib_packv5_042523_0143.root, FC#0, port D2

Entries	364
Mean	44.91
Std Dev	11.5

Width : 3.285

Height : 10.023



B1L101S, U17-ch54

calib_packv5_042523_0143.root, FC#0, port D2

Entries	373
Mean	44.56
Std Dev	11.4

Turn on : 26.7200

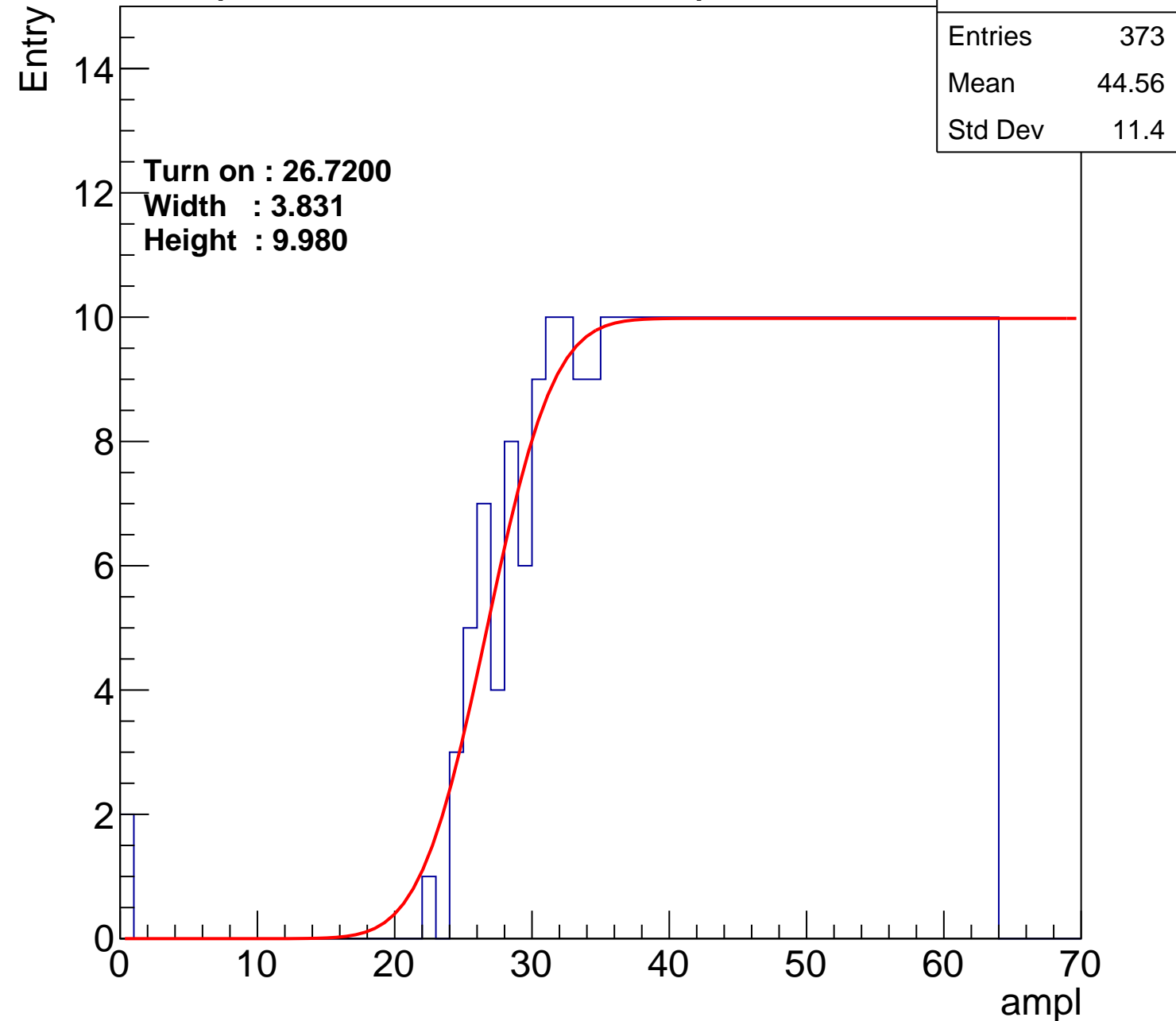
Width : 3.831

Height : 9.980

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U17-ch55

calib_packv5_042523_0143.root, FC#0, port D2

Entries	368
Mean	44.75
Std Dev	11.46

Turn on : 28.2488

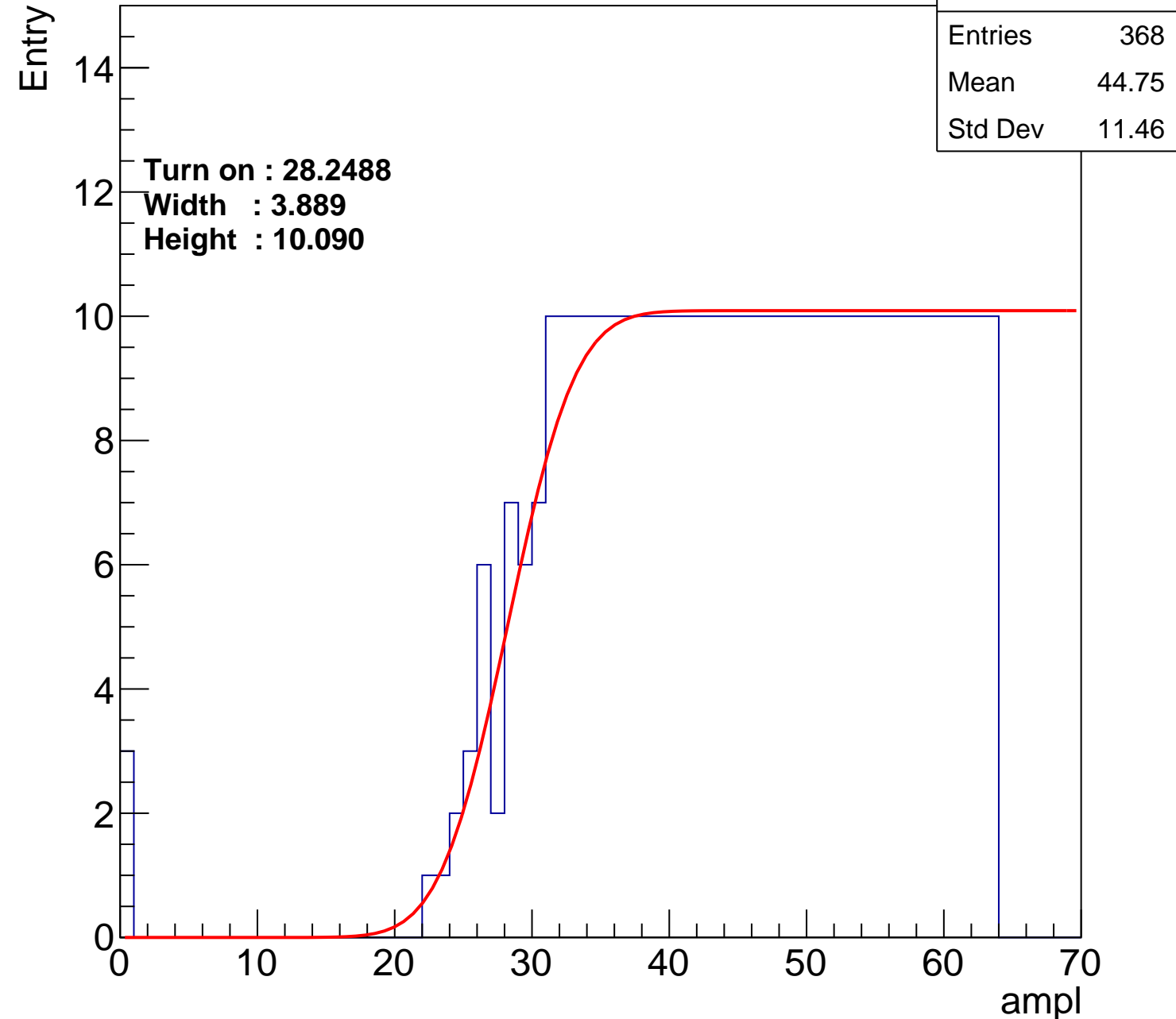
Width : 3.889

Height : 10.090

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U17-ch56

calib_packv5_042523_0143.root, FC#0, port D2

Entries	393
Mean	43.57
Std Dev	12.02

Turn on : 25.3369

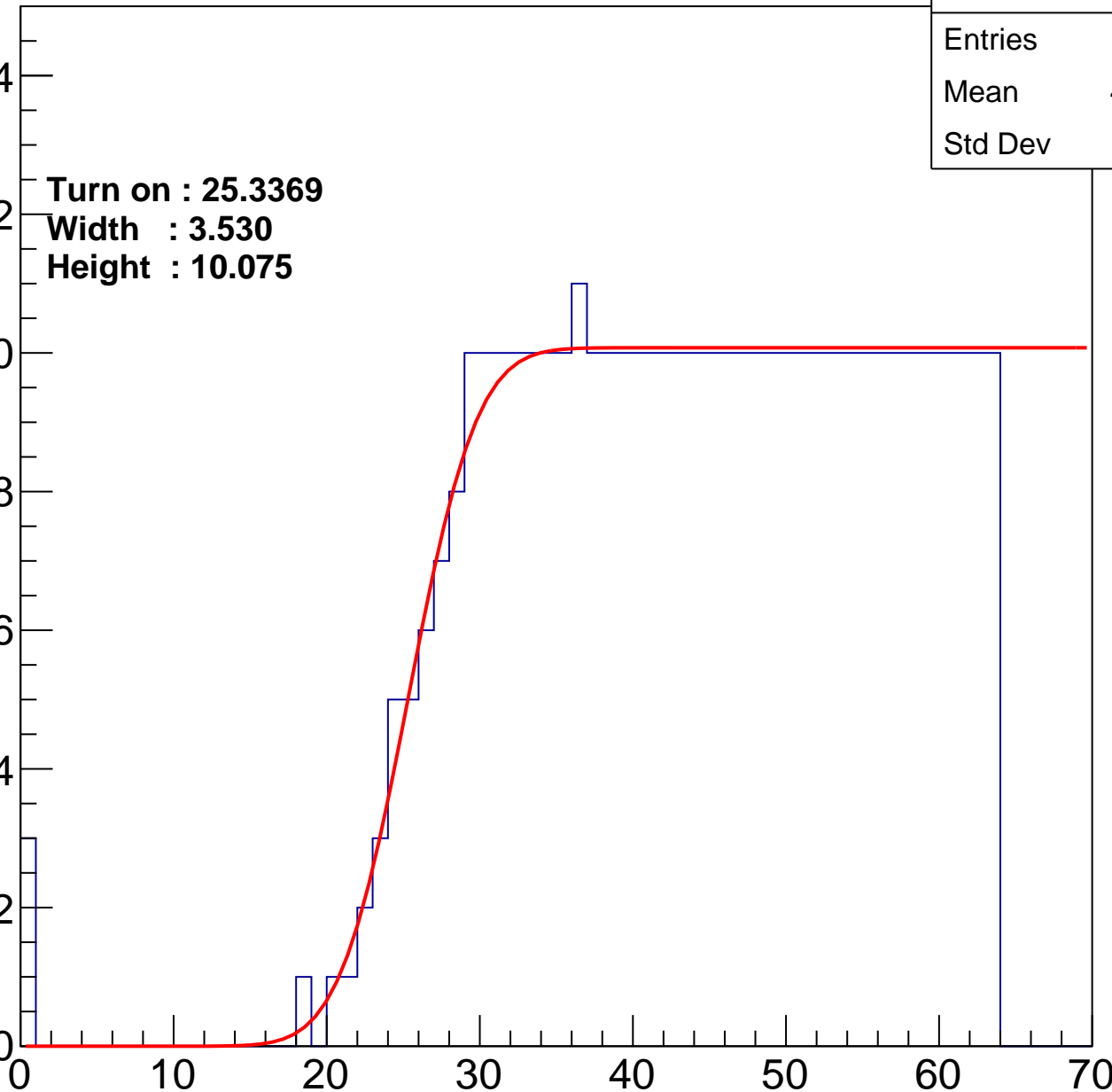
Width : 3.530

Height : 10.075

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U17-ch57

calib_packv5_042523_0143.root, FC#0, port D2

Entries	382
Mean	44.11
Std Dev	11.73

Turn on : 26.4420

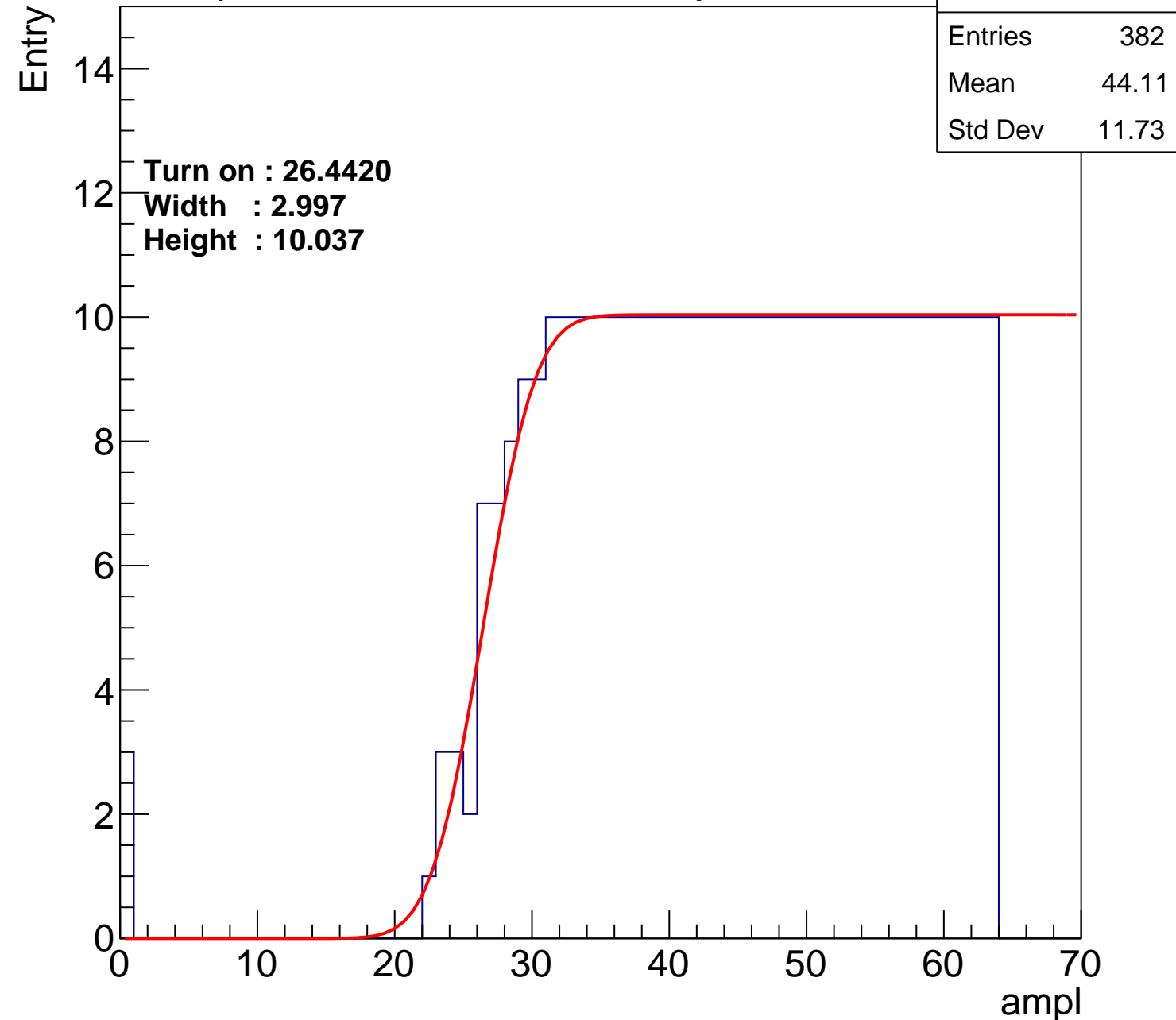
Width : 2.997

Height : 10.037

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U17-ch58

calib_packv5_042523_0143.root, FC#0, port D2

Entries	373
Mean	44.42
Std Dev	11.8

Turn on : 27.2624

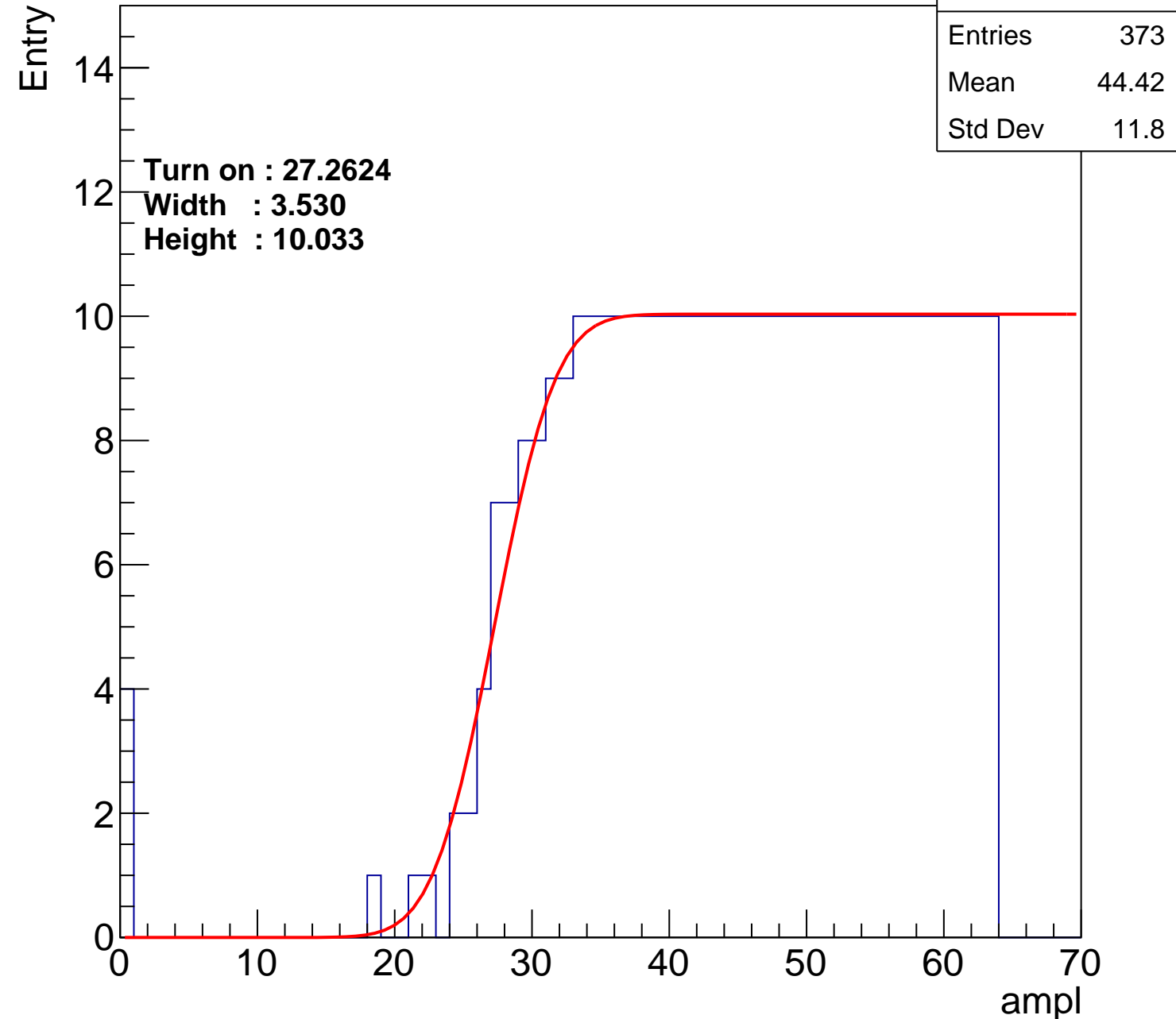
Width : 3.530

Height : 10.033

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U17-ch59

calib_packv5_042523_0143.root, FC#0, port D2

Entries	347
Mean	45.78
Std Dev	10.96

Turn on : 30.0426

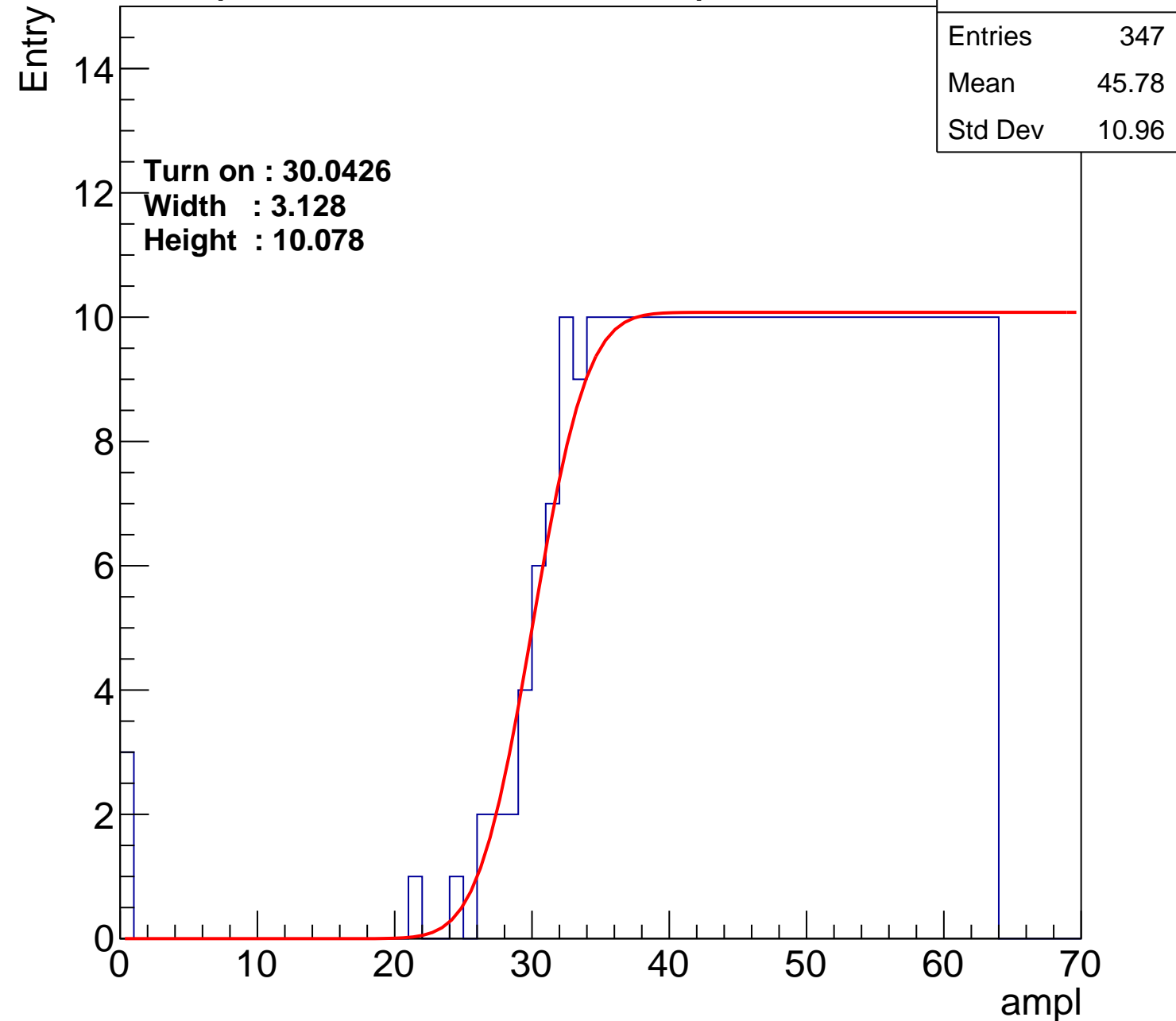
Width : 3.128

Height : 10.078

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U17-ch60

calib_packv5_042523_0143.root, FC#0, port D2

Entries	393
Mean	43.33
Std Dev	12.56

Turn on : 25.6830

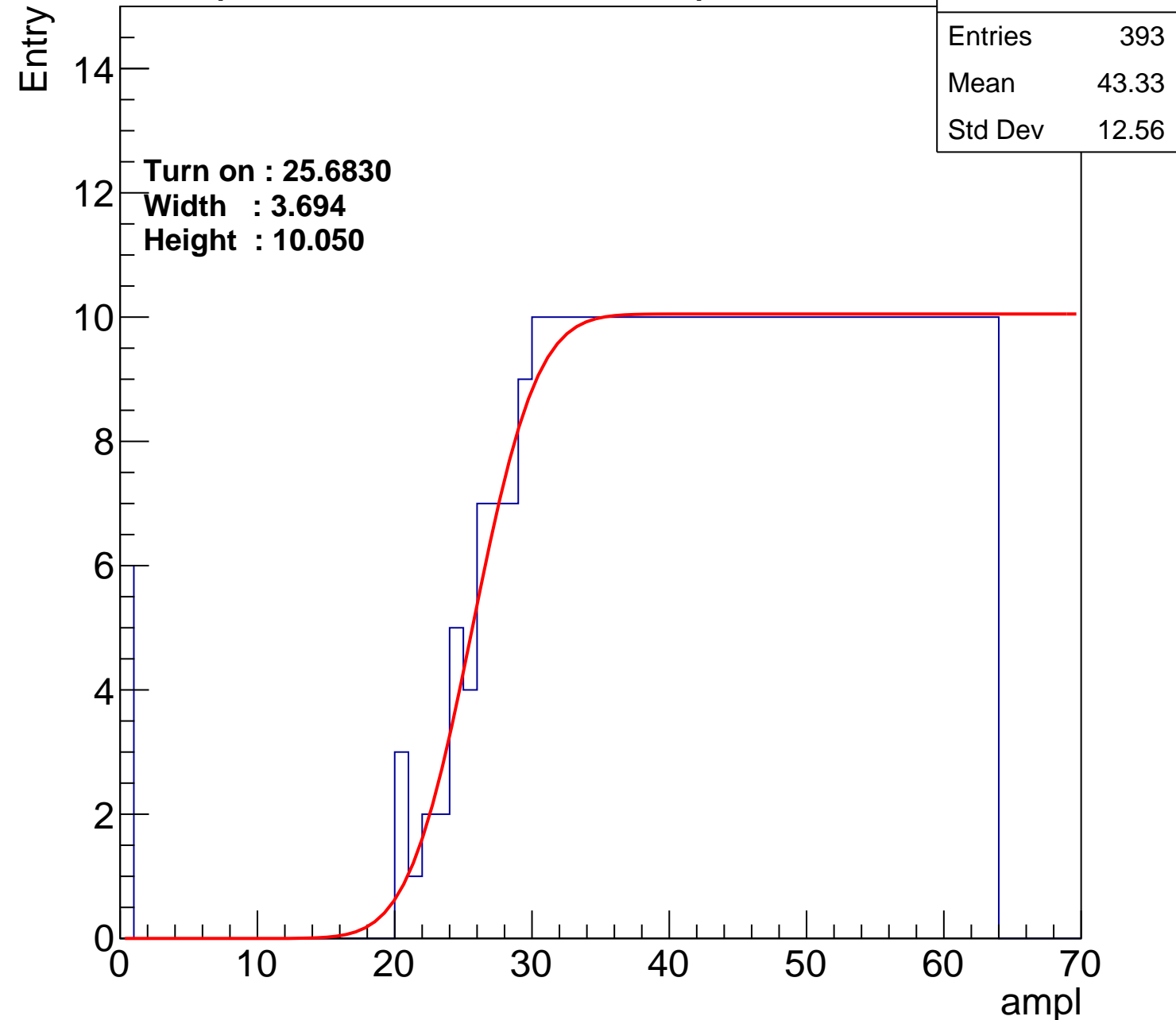
Width : 3.694

Height : 10.050

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U17-ch61

calib_packv5_042523_0143.root, FC#0, port D2

Entries	374
Mean	44.56
Std Dev	11.36

Turn on : 26.9731

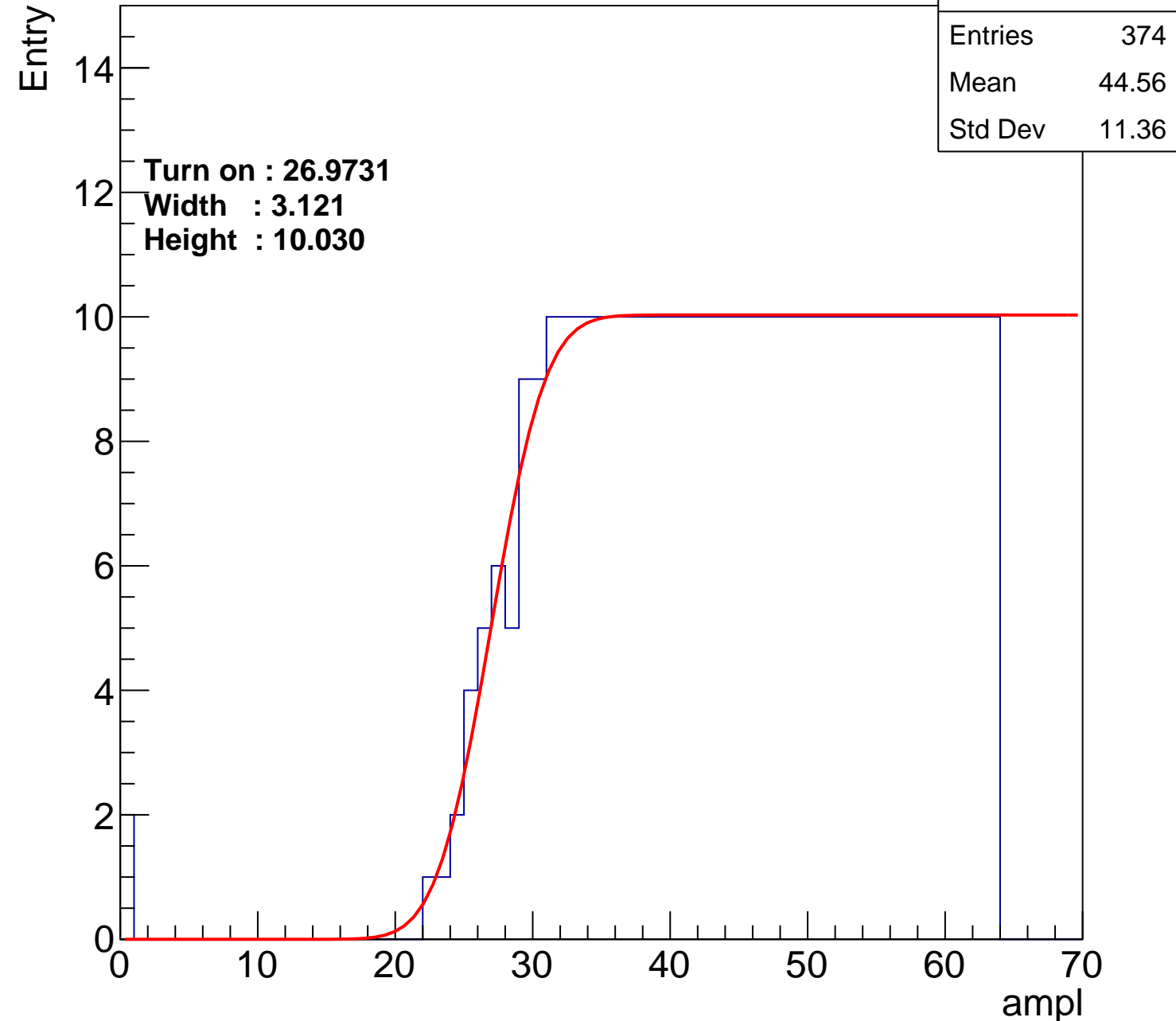
Width : 3.121

Height : 10.030

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U17-ch62

calib_packv5_042523_0143.root, FC#0, port D2

Entries	390
Mean	43.53
Std Dev	12.34

Turn on : 24.8773

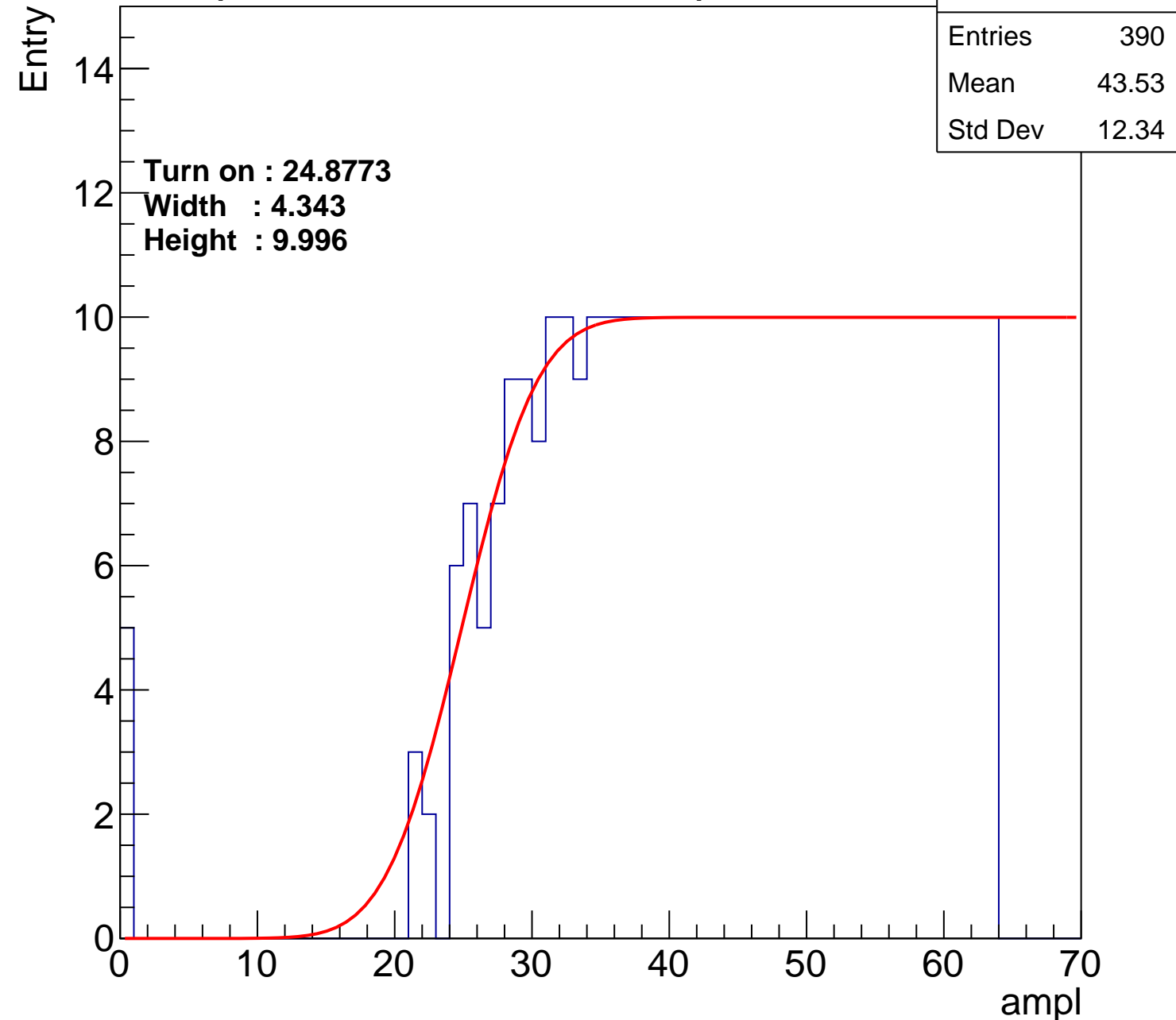
Width : 4.343

Height : 9.996

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U17-ch63

calib_packv5_042523_0143.root, FC#0, port D2

Entries	397
Mean	43.23
Std Dev	12.44

Turn on : 25.2456

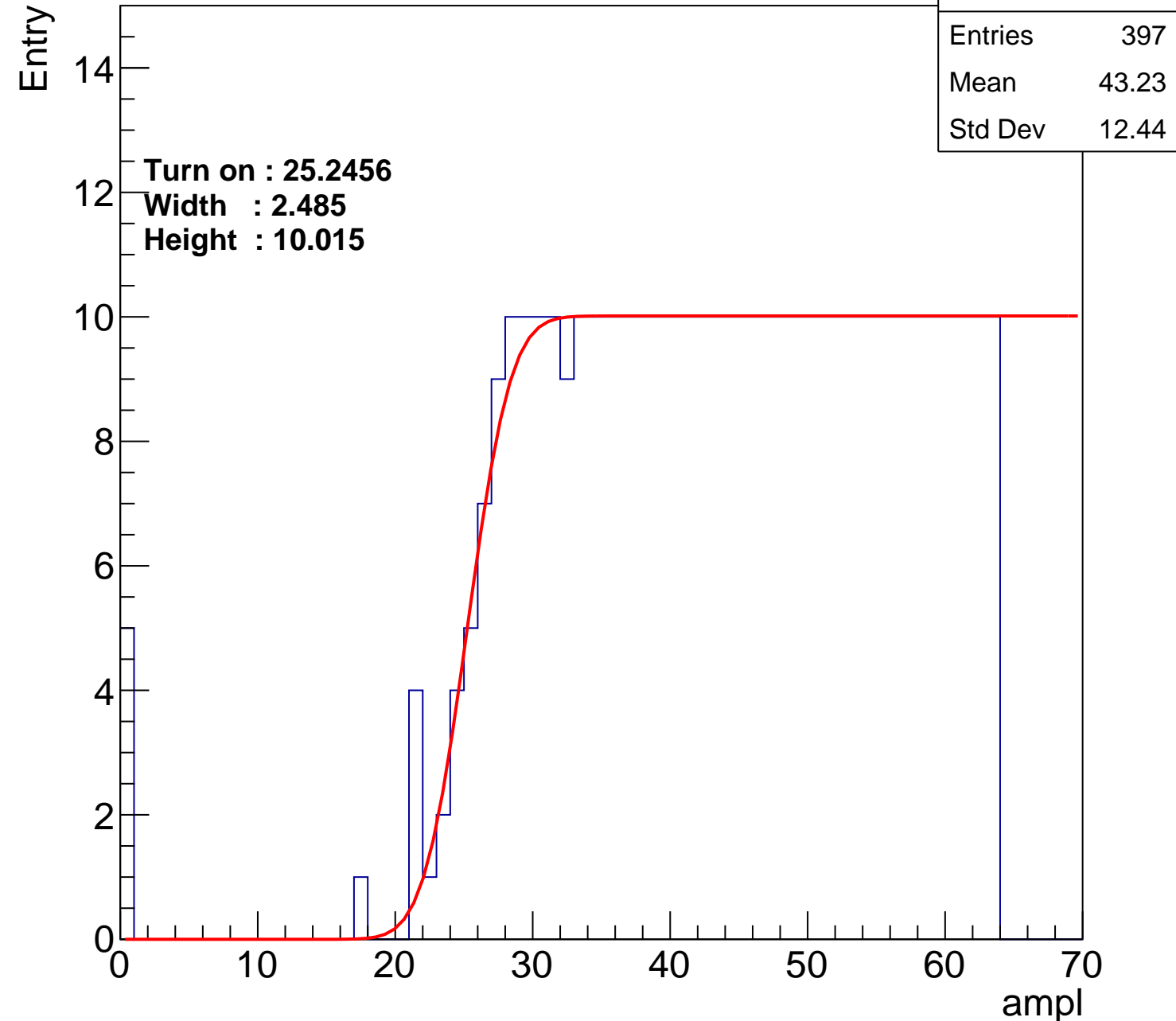
Width : 2.485

Height : 10.015

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U17-ch64

calib_packv5_042523_0143.root, FC#0, port D2

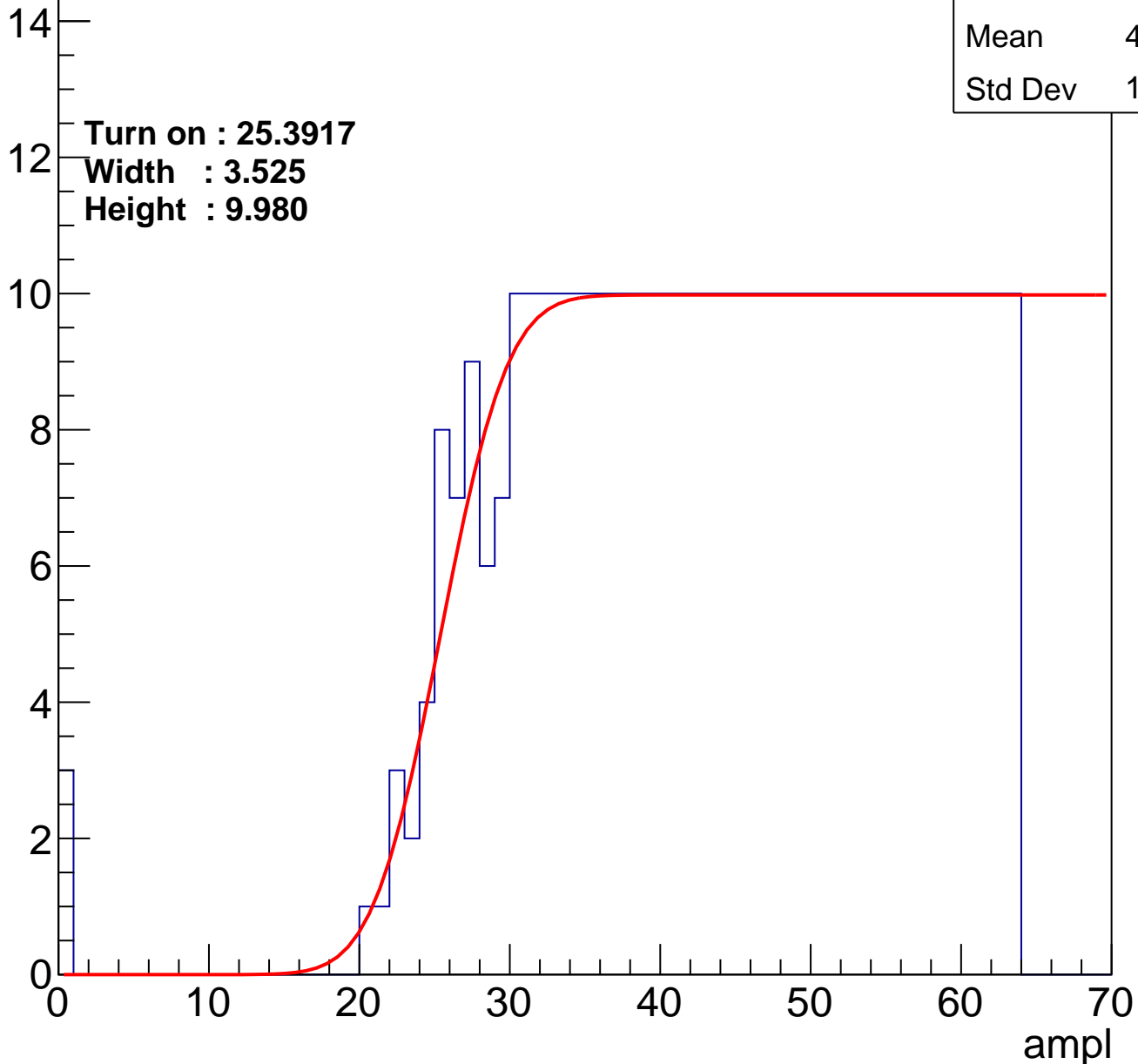
Entries	391
Mean	43.62
Std Dev	12.02

Turn on : 25.3917

Width : 3.525

Height : 9.980

Entry



B1L101S, U17-ch65

calib_packv5_042523_0143.root, FC#0, port D2

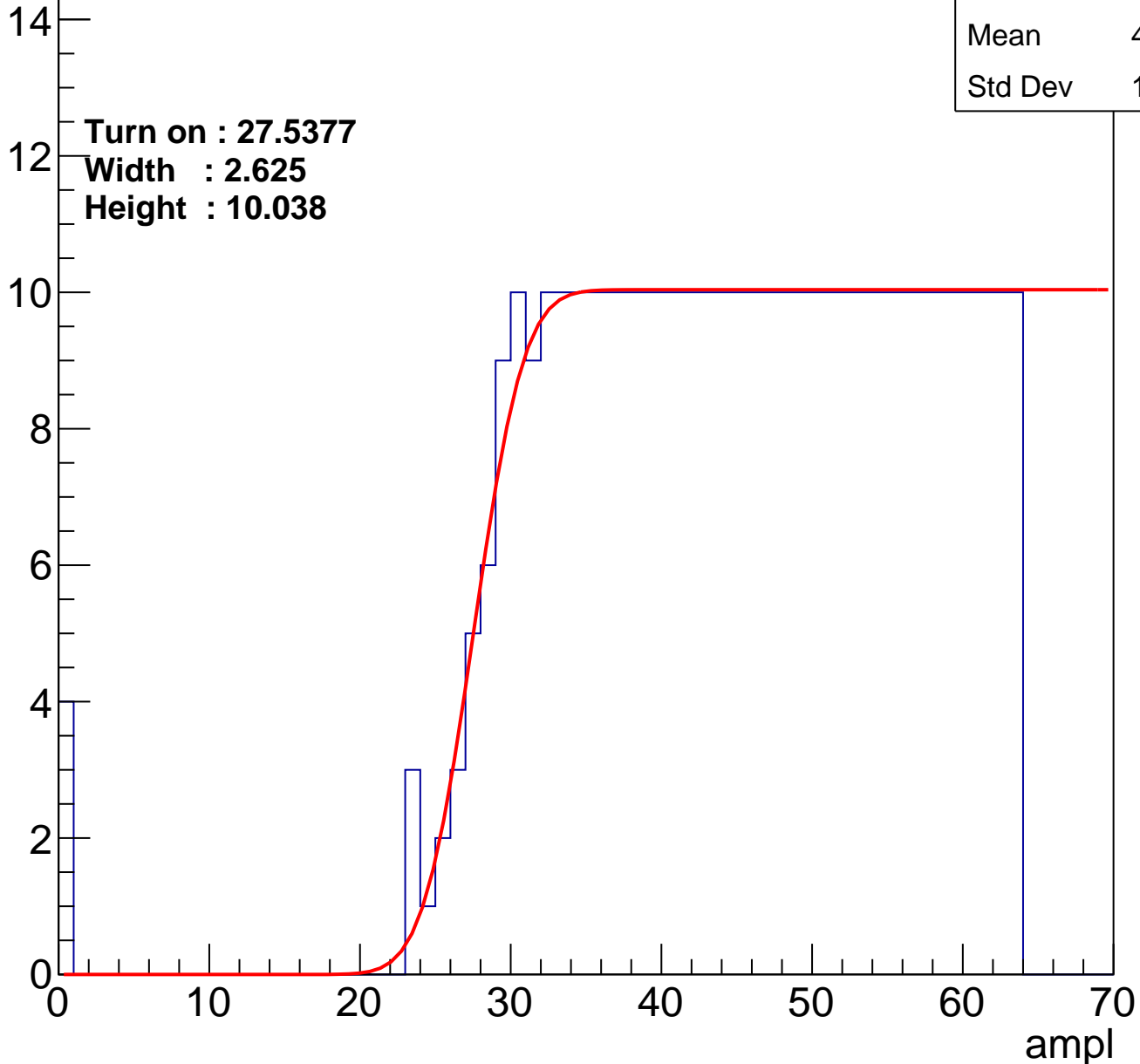
Entries	372
Mean	44.53
Std Dev	11.68

Turn on : 27.5377

Width : 2.625

Height : 10.038

Entry



B1L101S, U17-ch66

calib_packv5_042523_0143.root, FC#0, port D2

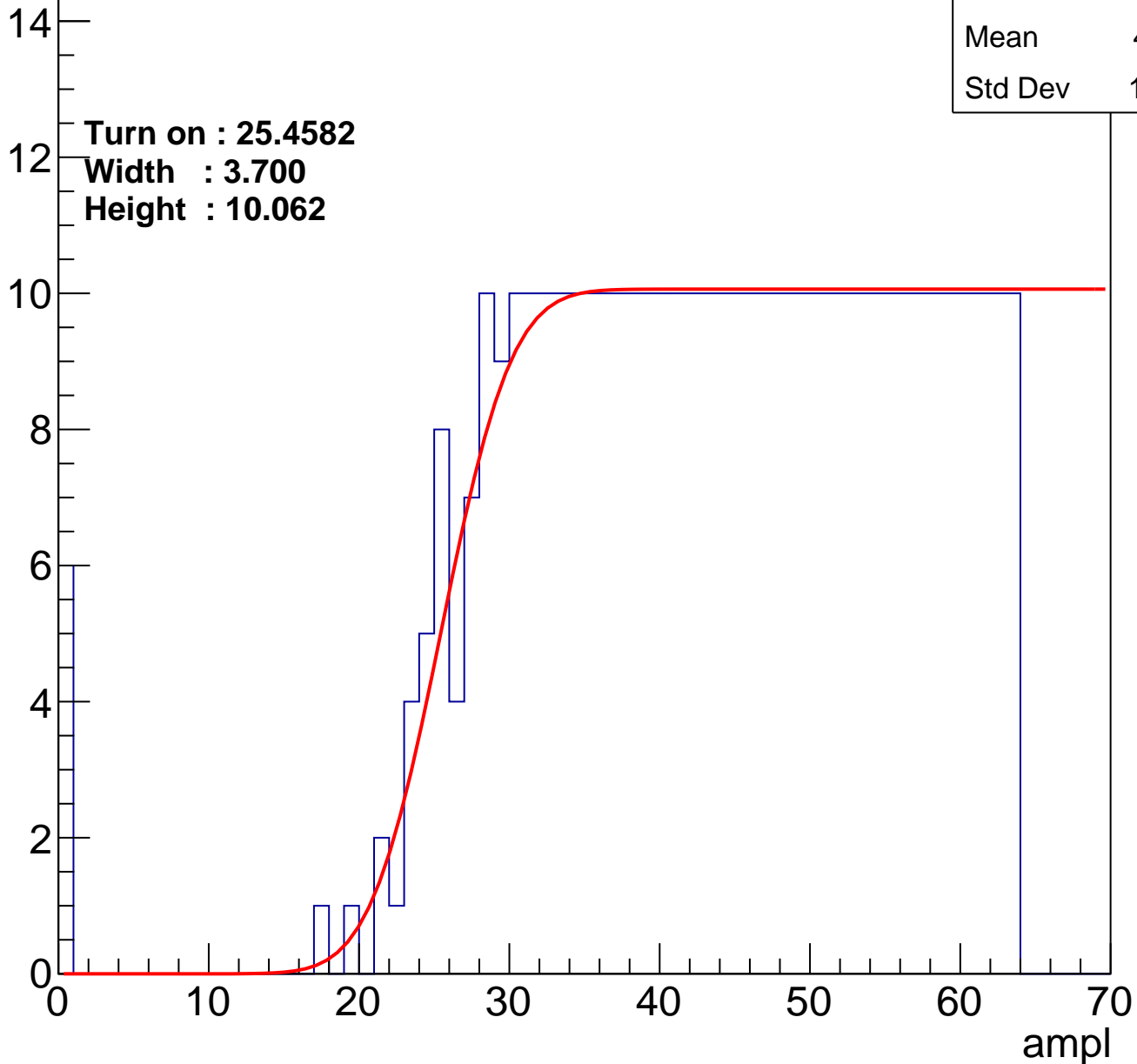
Entries	398
Mean	43.11
Std Dev	12.64

Turn on : 25.4582

Width : 3.700

Height : 10.062

Entry



B1L101S, U17-ch67

calib_packv5_042523_0143.root, FC#0, port D2

Entries	376
Mean	44.45
Std Dev	11.44

Turn on : 27.2952

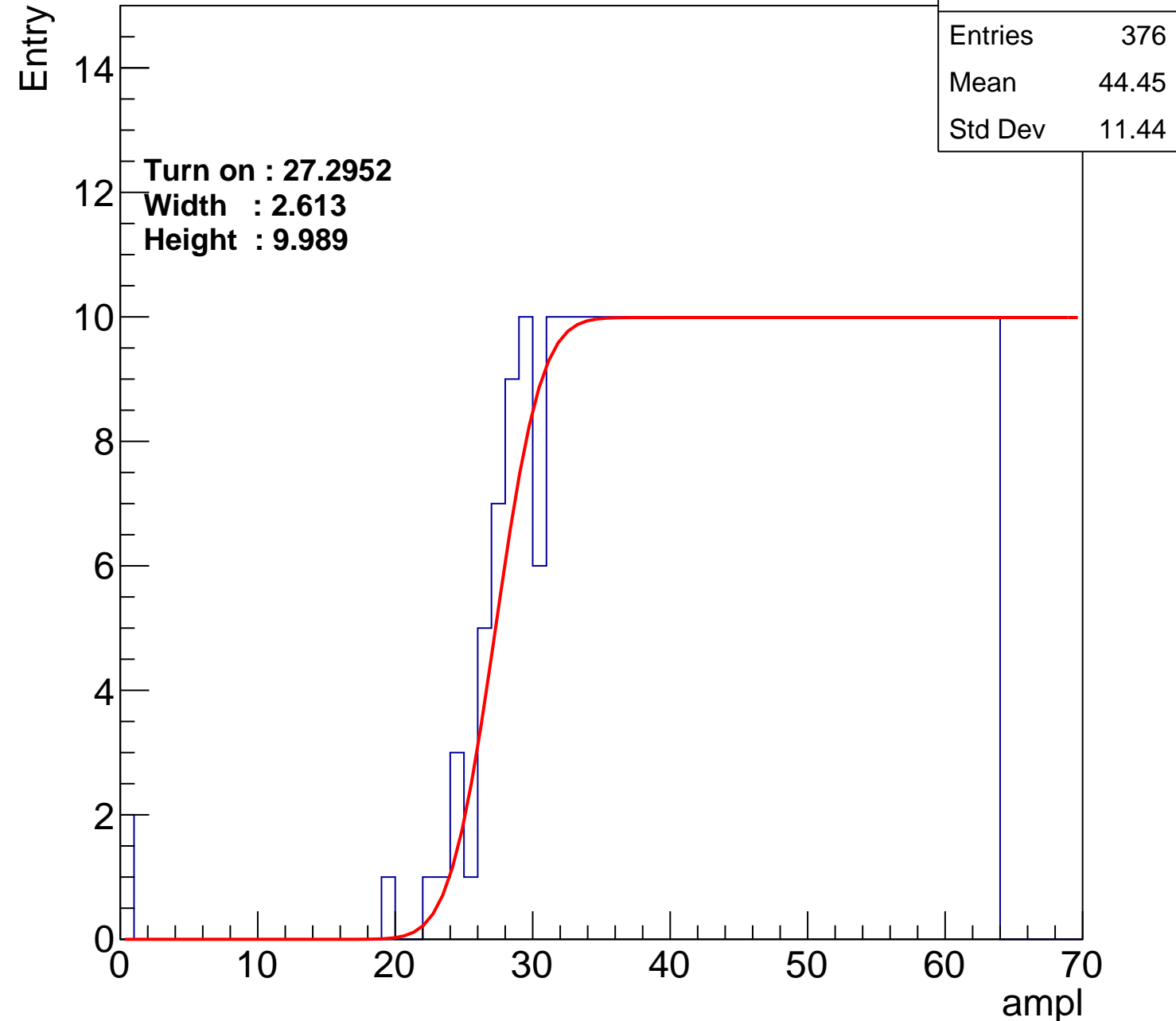
Width : 2.613

Height : 9.989

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U17-ch68

calib_packv5_042523_0143.root, FC#0, port D2

Entries	381
Mean	44.12
Std Dev	11.75

Turn on : 26.5180

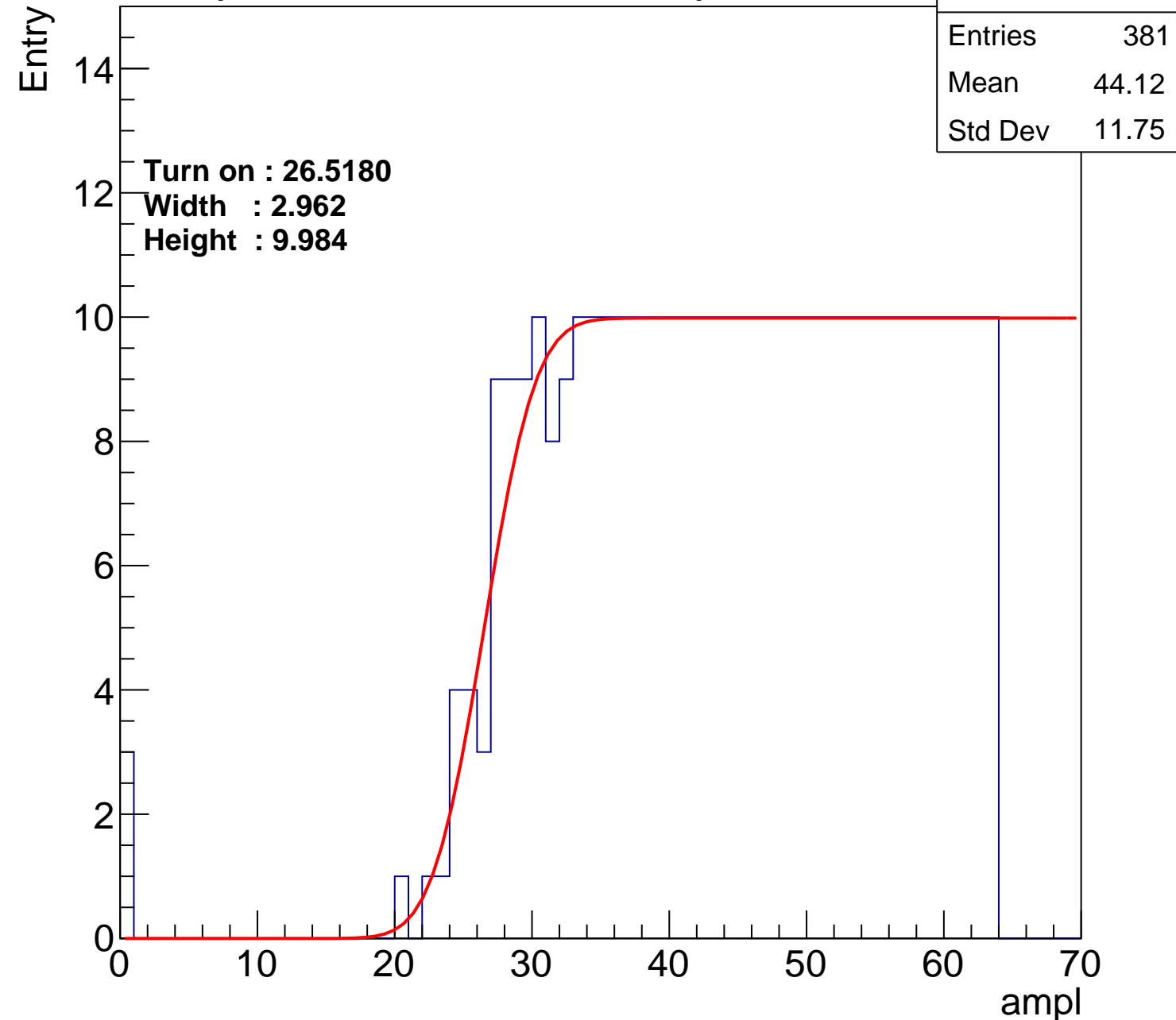
Width : 2.962

Height : 9.984

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U17-ch69

calib_packv5_042523_0143.root, FC#0, port D2

Entries	377
Mean	44.35
Std Dev	11.61

Turn on : 26.4964

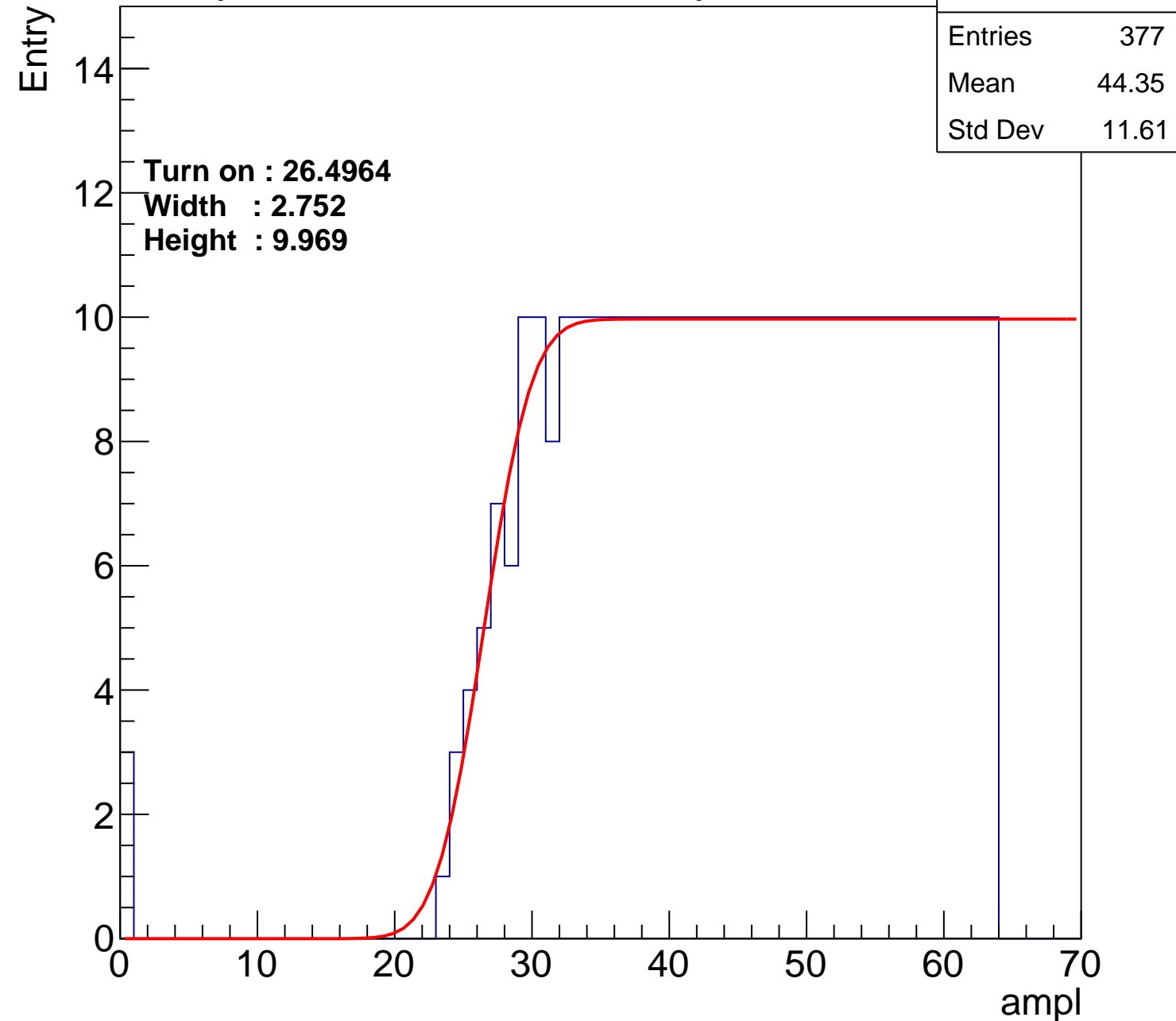
Width : 2.752

Height : 9.969

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U17-ch70

calib_packv5_042523_0143.root, FC#0, port D2

Entries	392
Mean	43.59
Std Dev	12.02

Turn on : 25.3037

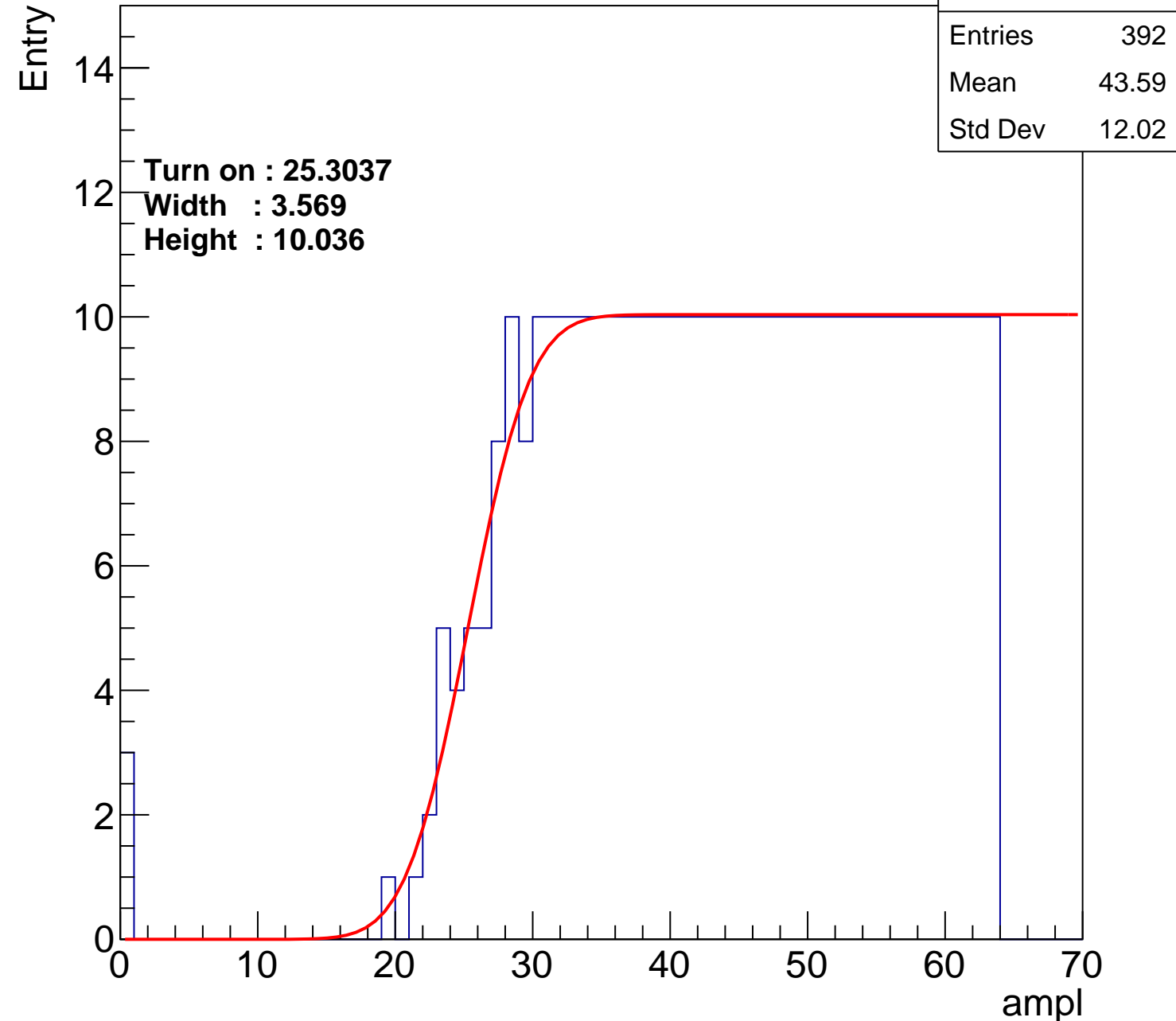
Width : 3.569

Height : 10.036

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U17-ch71

calib_packv5_042523_0143.root, FC#0, port D2

Entries	379
Mean	44.15
Std Dev	11.9

Turn on : 26.8725

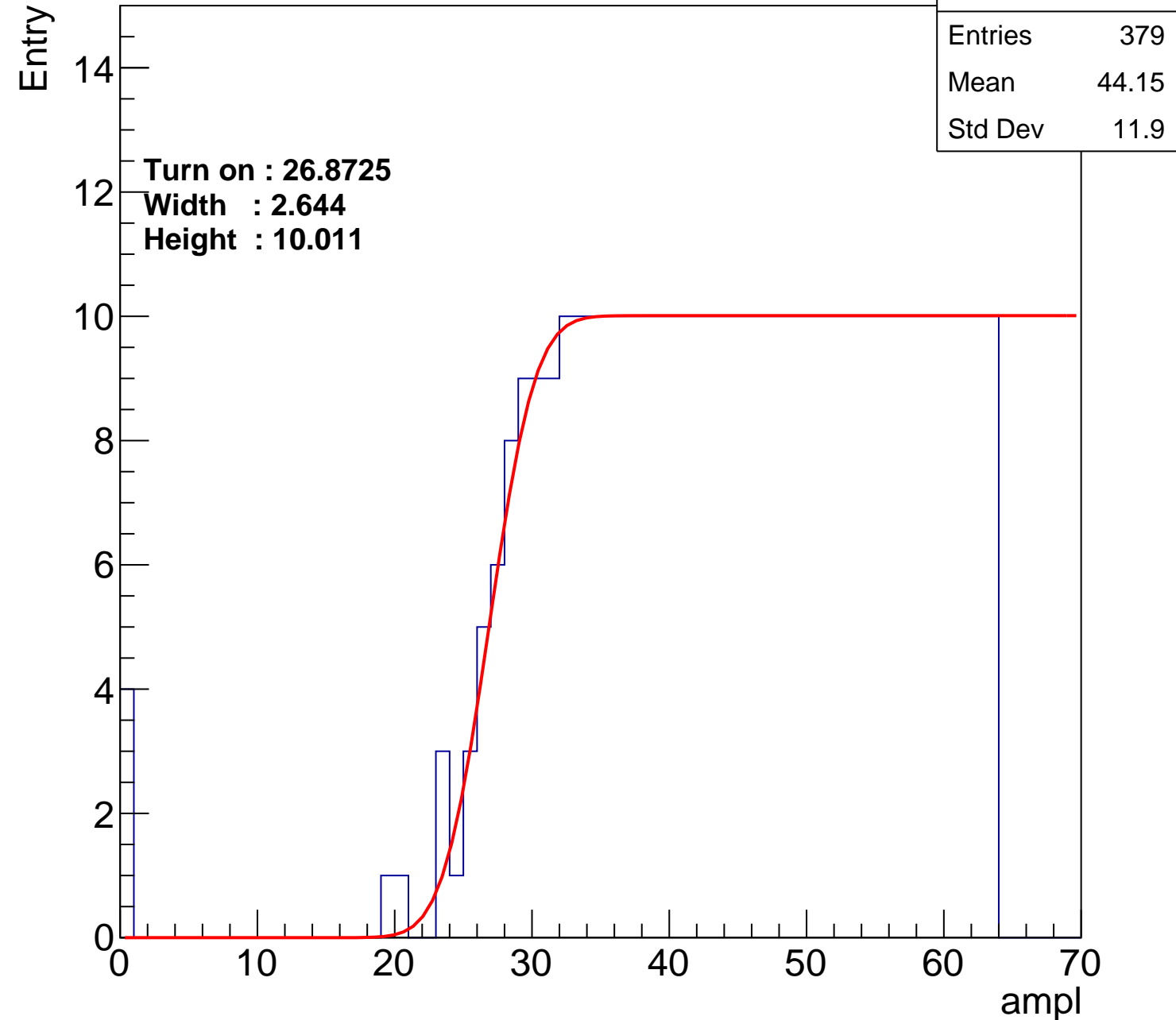
Width : 2.644

Height : 10.011

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U17-ch72

calib_packv5_042523_0143.root, FC#0, port D2

Entries	384
Mean	44.01
Std Dev	11.78

Turn on : 25.8791

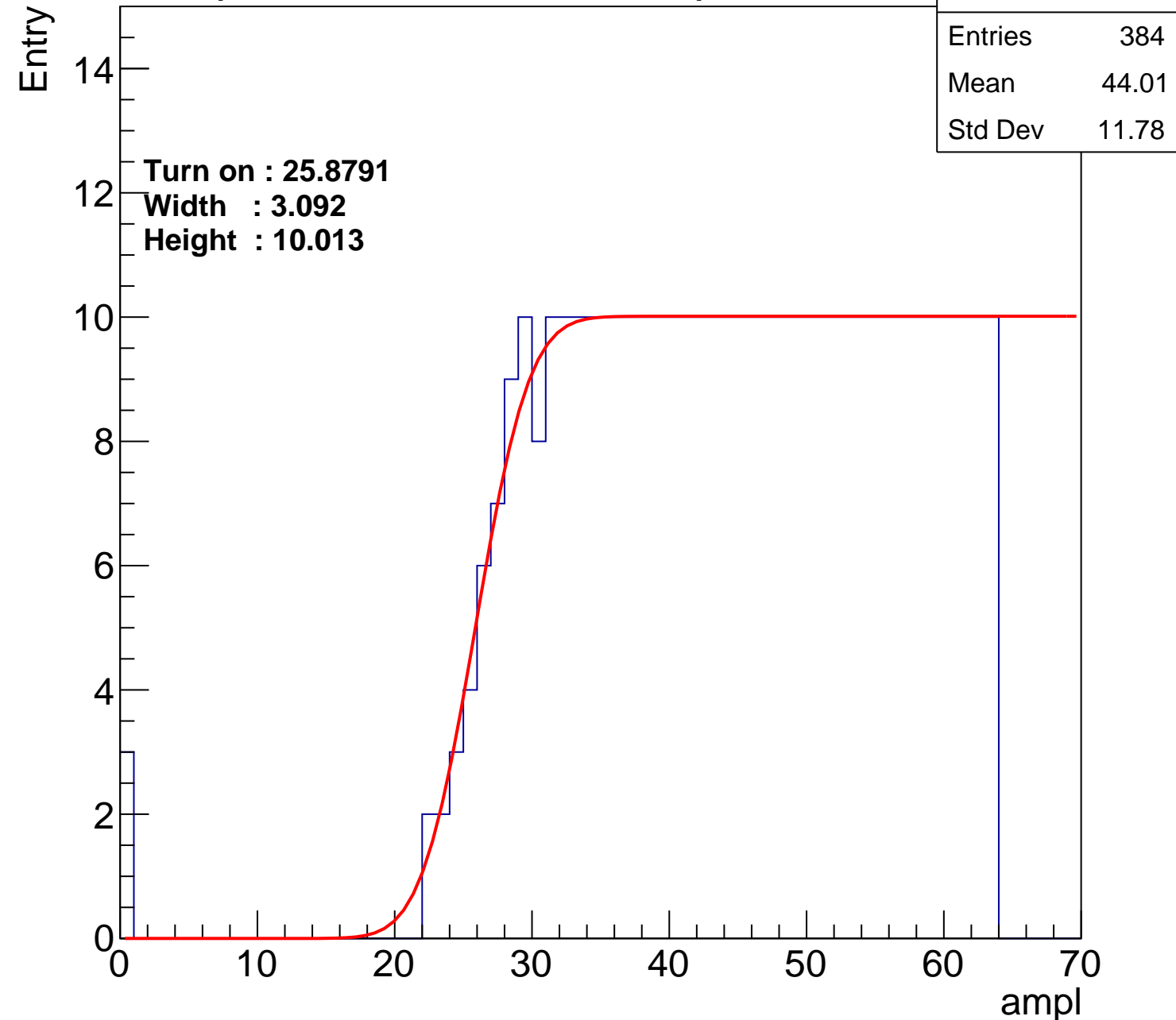
Width : 3.092

Height : 10.013

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U17-ch73

calib_packv5_042523_0143.root, FC#0, port D2

Entries	382
Mean	44.09
Std Dev	11.76

Turn on : 25.9333

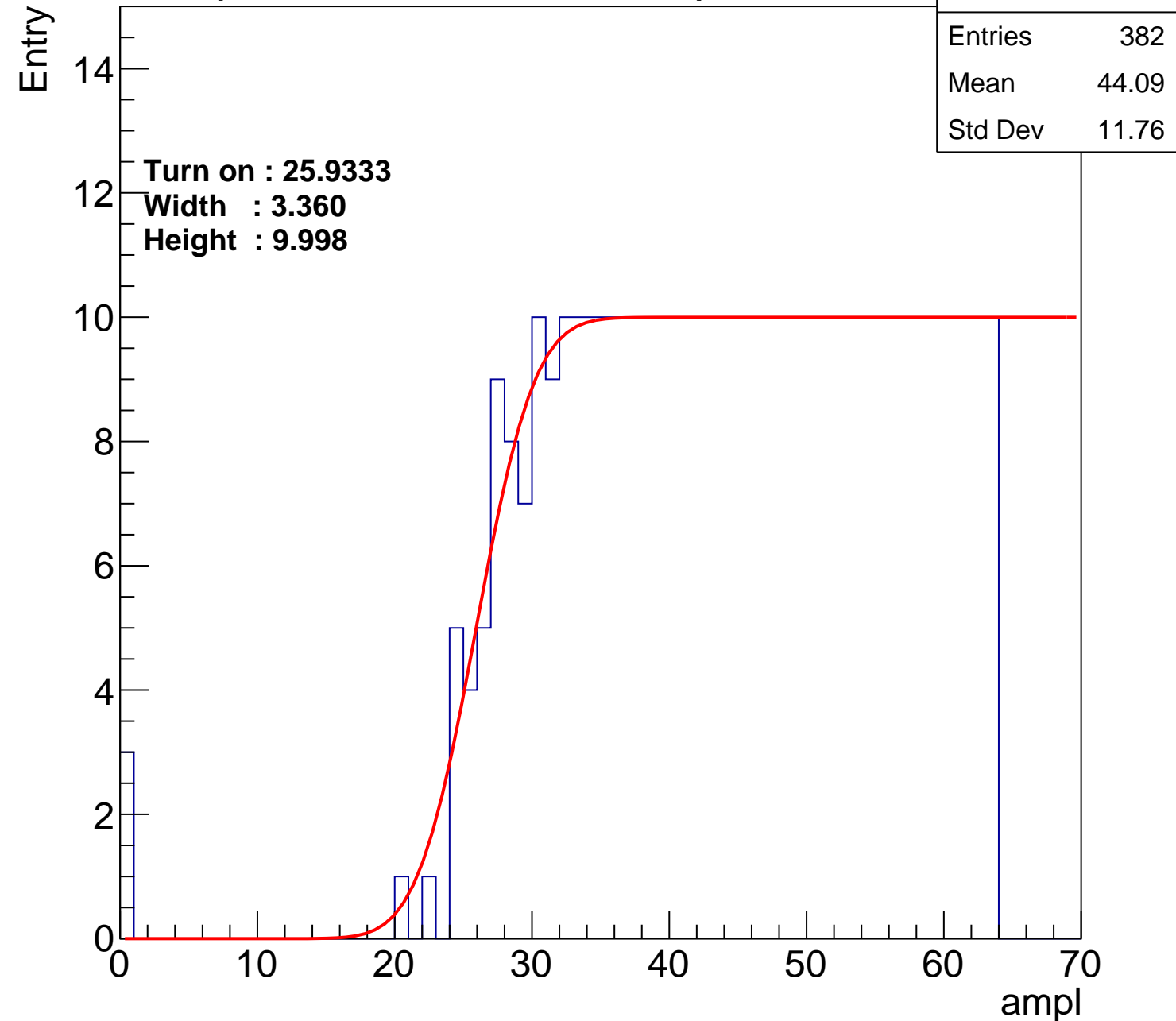
Width : 3.360

Height : 9.998

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U17-ch74

calib_packv5_042523_0143.root, FC#0, port D2

Entries	387
Mean	43.91
Std Dev	11.7

Turn on : 25.5506

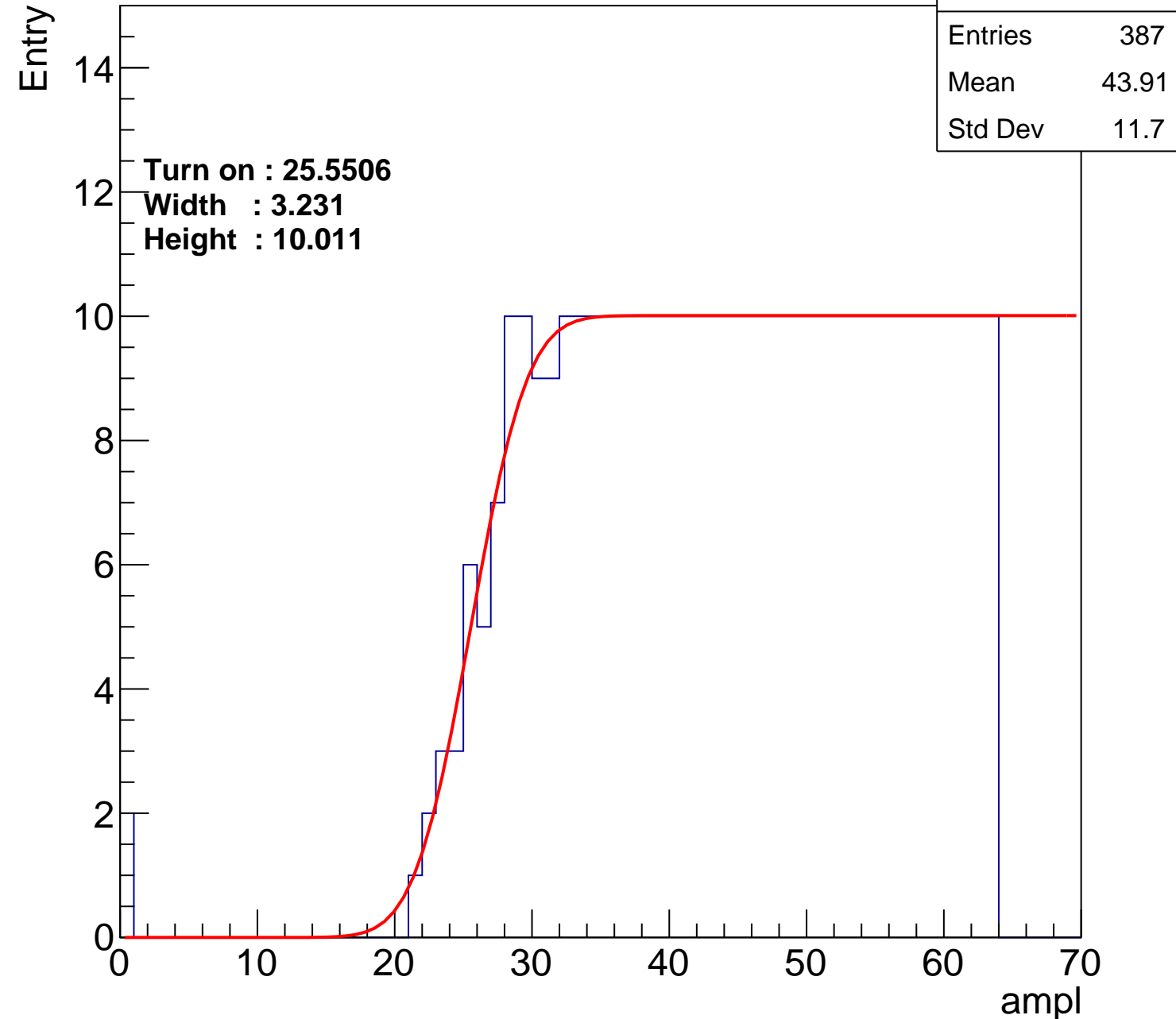
Width : 3.231

Height : 10.011

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U17-ch75

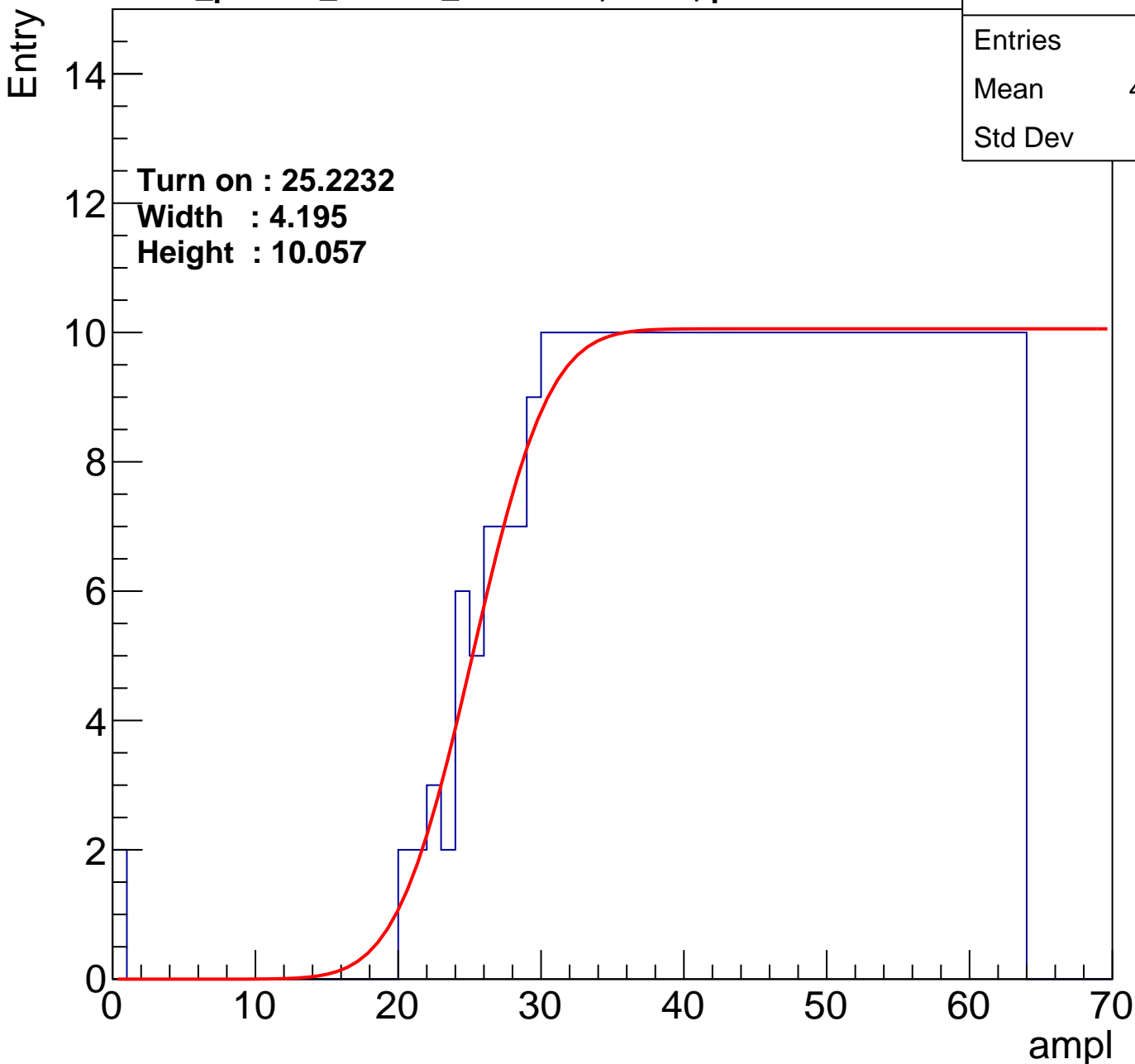
calib_packv5_042523_0143.root, FC#0, port D2

Entries	392
Mean	43.62
Std Dev	11.9

Turn on : 25.2232

Width : 4.195

Height : 10.057



B1L101S, U17-ch76

calib_packv5_042523_0143.root, FC#0, port D2

Entries	400
Mean	43.13
Std Dev	12.34

Turn on : 25.3186

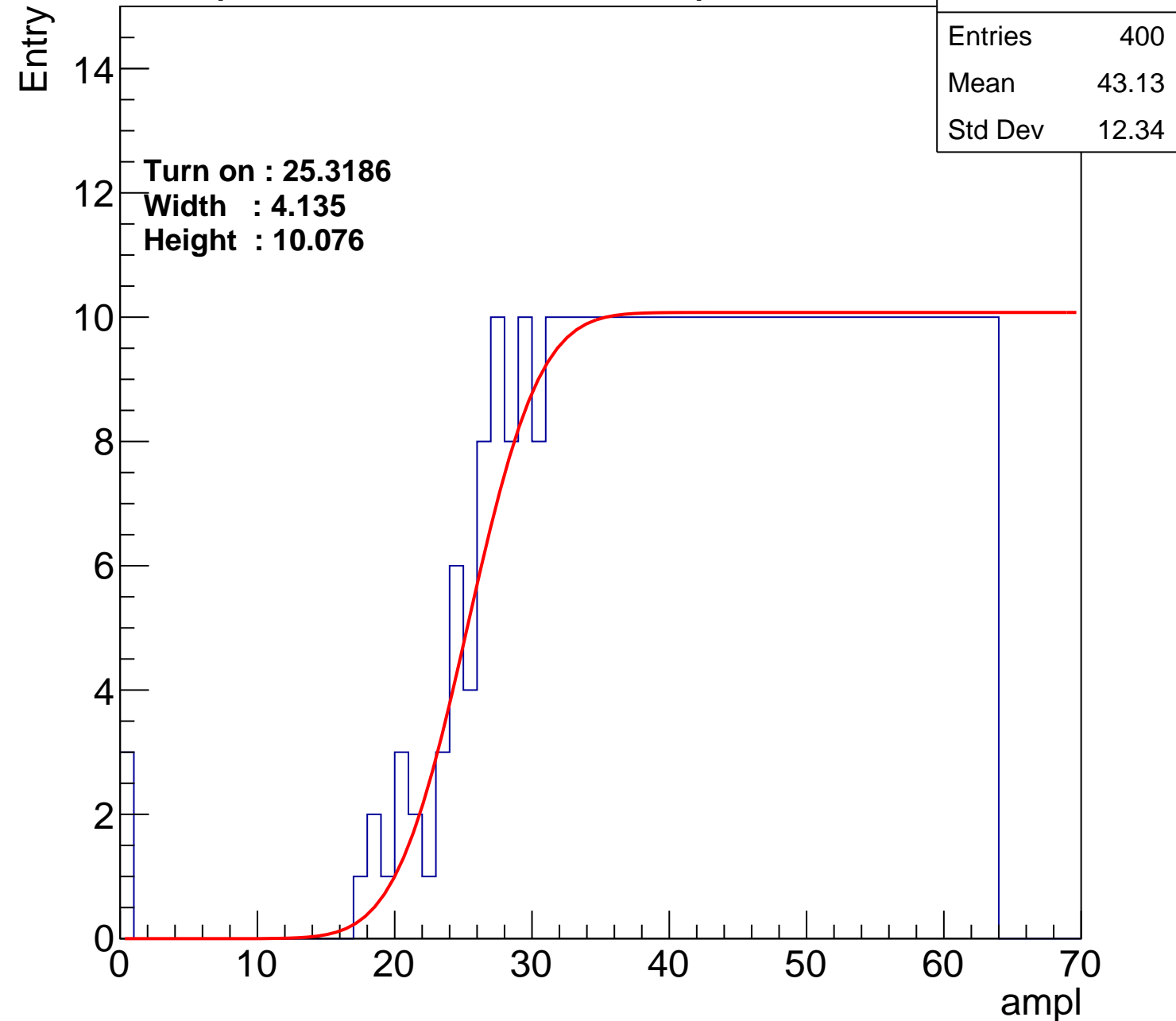
Width : 4.135

Height : 10.076

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U17-ch77

calib_packv5_042523_0143.root, FC#0, port D2

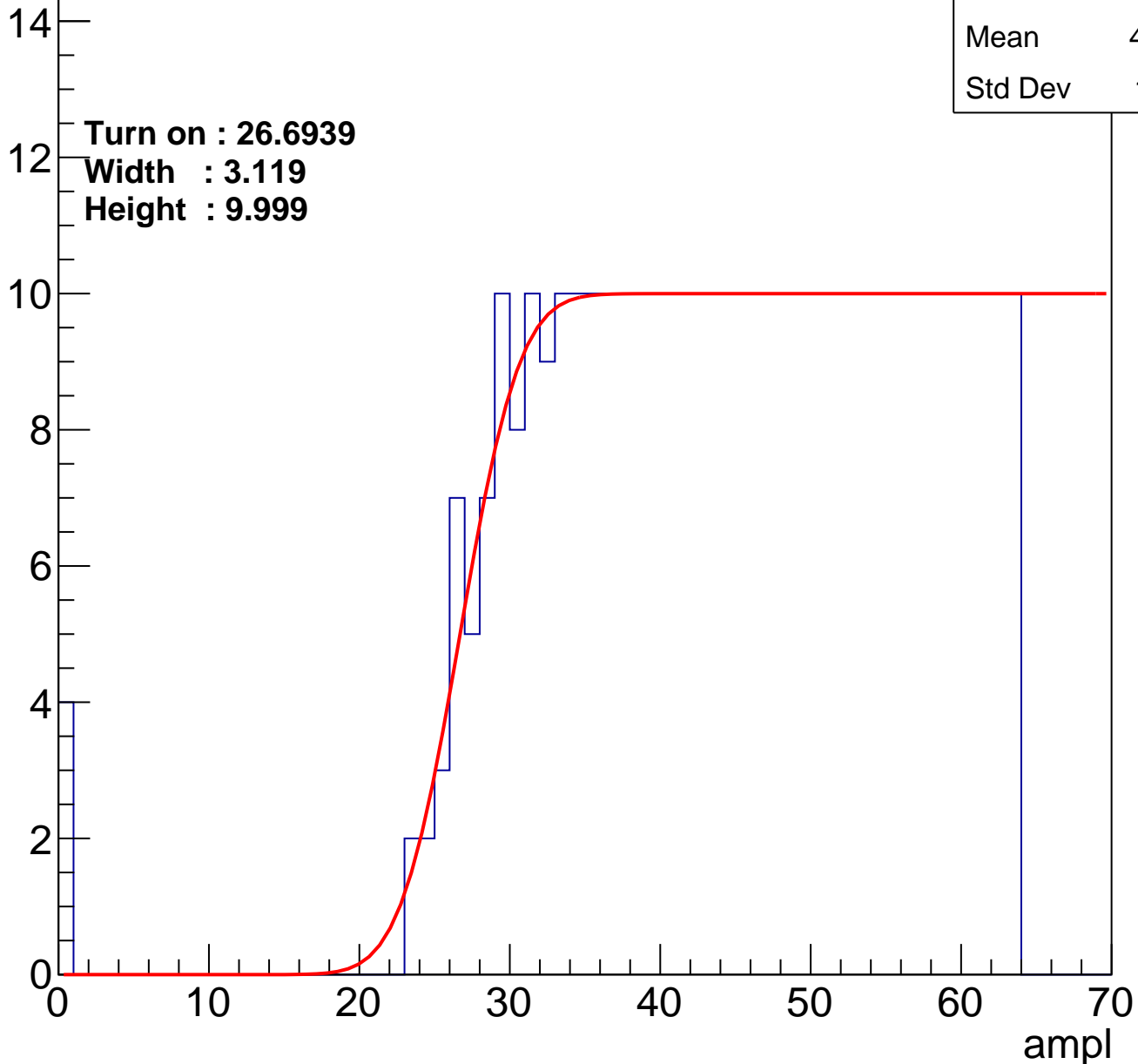
Entries	377
Mean	44.27
Std Dev	11.81

Turn on : 26.6939

Width : 3.119

Height : 9.999

Entry



B1L101S, U17-ch78

calib_packv5_042523_0143.root, FC#0, port D2

Entries	390
Mean	43.6
Std Dev	12.24

Turn on : 25.7803

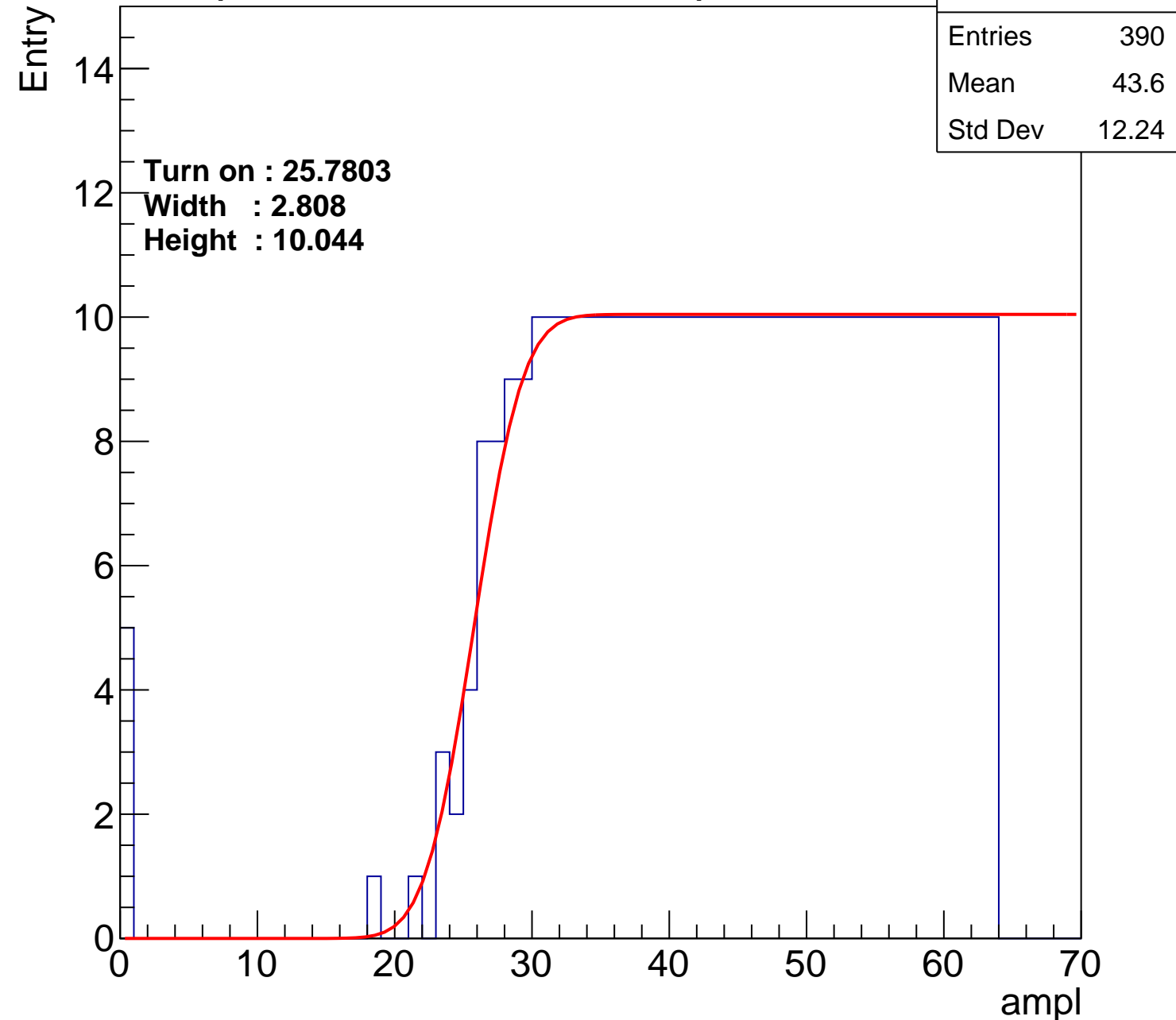
Width : 2.808

Height : 10.044

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U17-ch79

calib_packv5_042523_0143.root, FC#0, port D2

Entries	380
Mean	44.21
Std Dev	11.67

Turn on : 26.6346

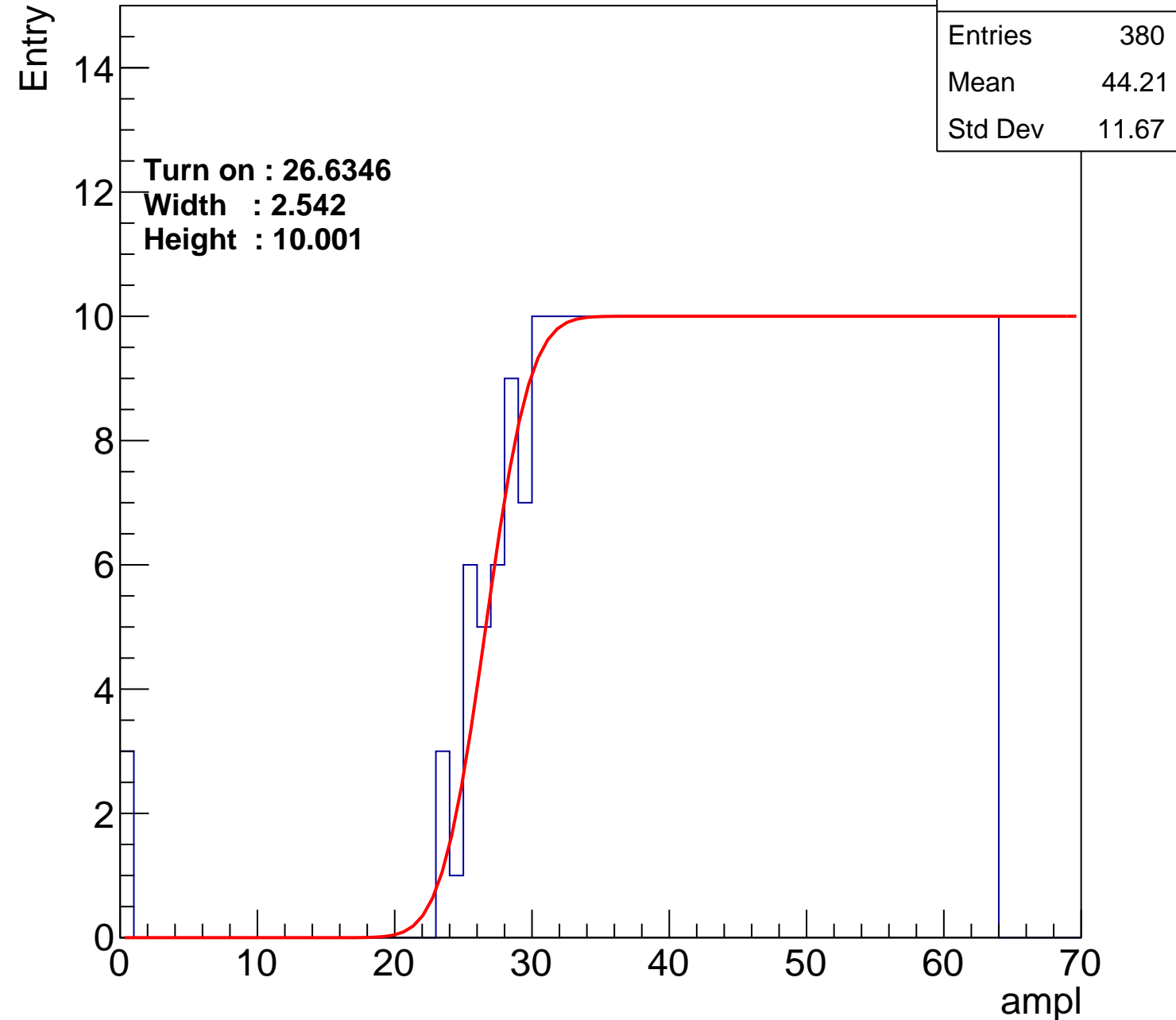
Width : 2.542

Height : 10.001

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U17-ch80

calib_packv5_042523_0143.root, FC#0, port D2

Entries	381
Mean	44.24
Std Dev	11.51

Turn on : 26.7958

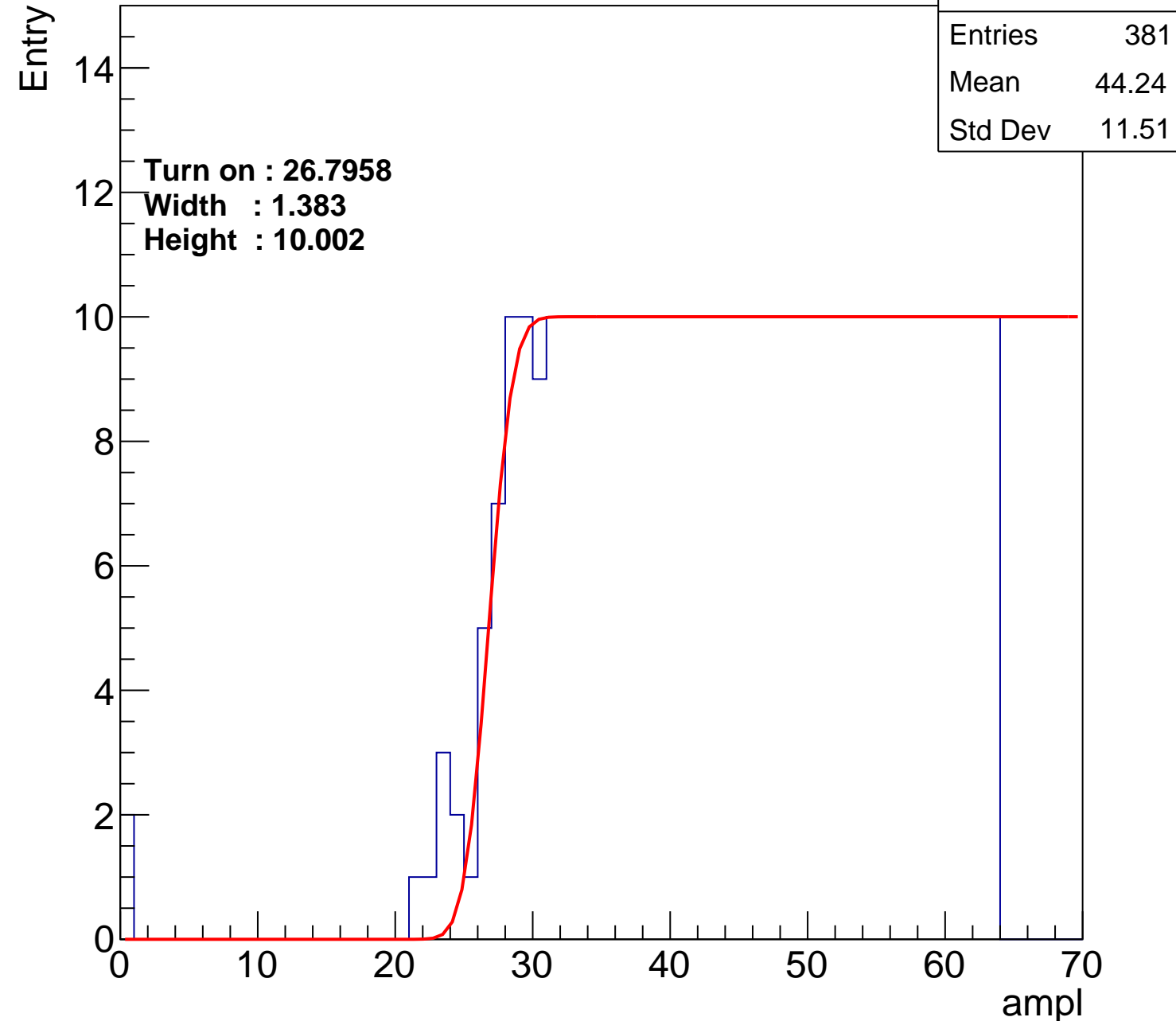
Width : 1.383

Height : 10.002

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U17-ch81

calib_packv5_042523_0143.root, FC#0, port D2

Entries	369
Mean	44.71
Std Dev	11.39

Turn on : 28.6481

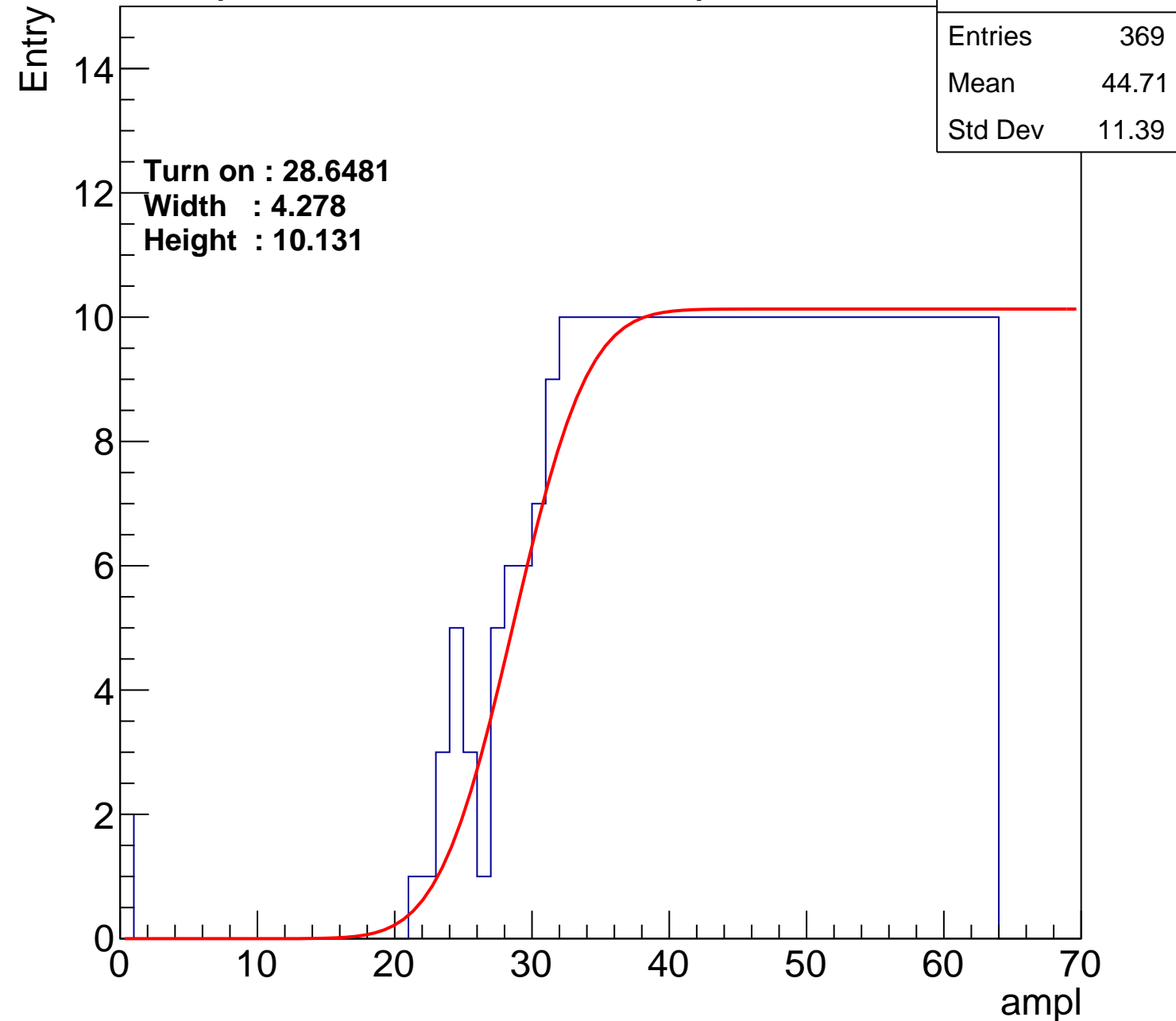
Width : 4.278

Height : 10.131

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U17-ch82

calib_packv5_042523_0143.root, FC#0, port D2

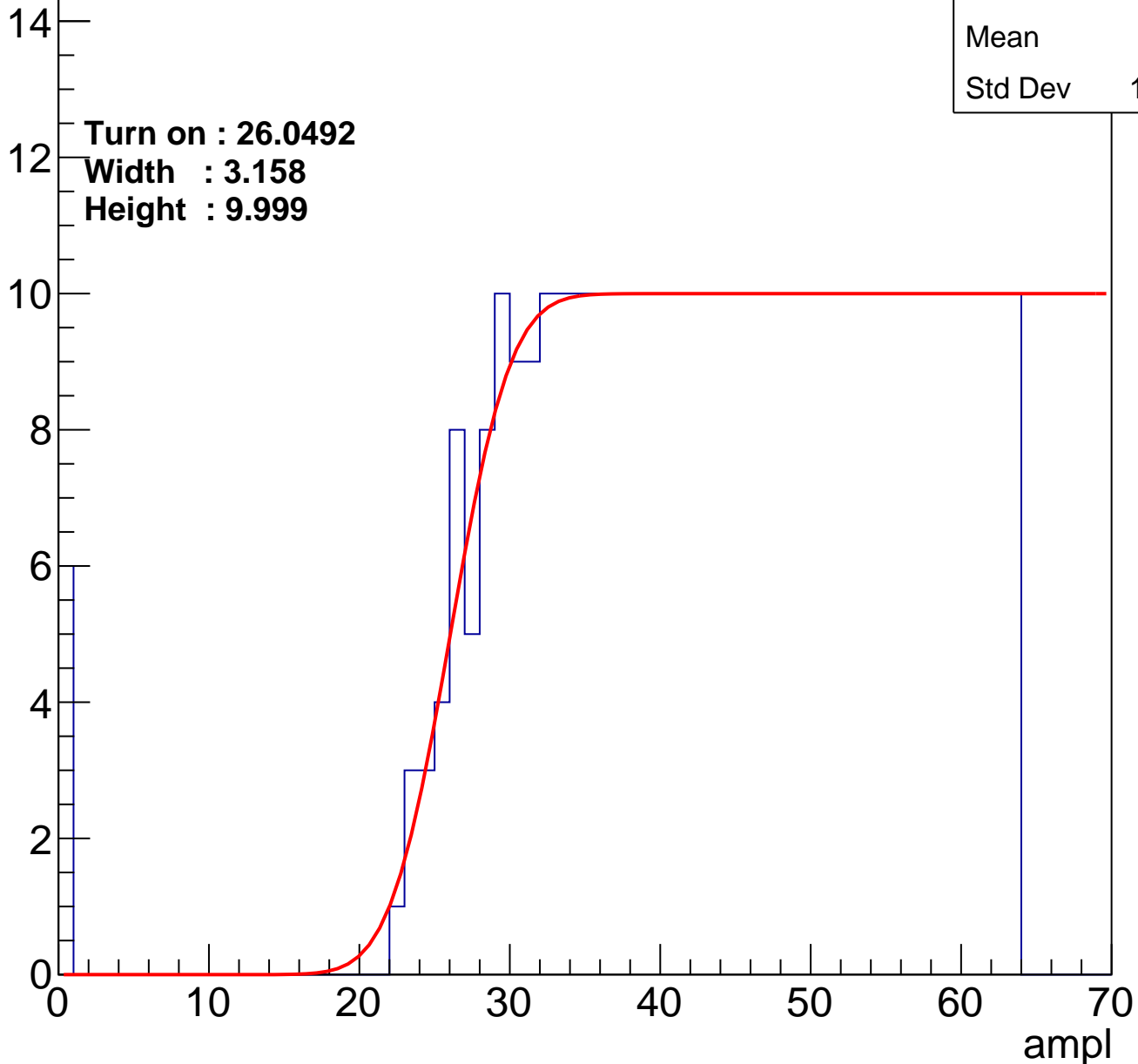
Entries	386
Mean	43.7
Std Dev	12.35

Turn on : 26.0492

Width : 3.158

Height : 9.999

Entry



B1L101S, U17-ch83

calib_packv5_042523_0143.root, FC#0, port D2

Entries	369
Mean	44.66
Std Dev	11.63

Turn on : 27.7354

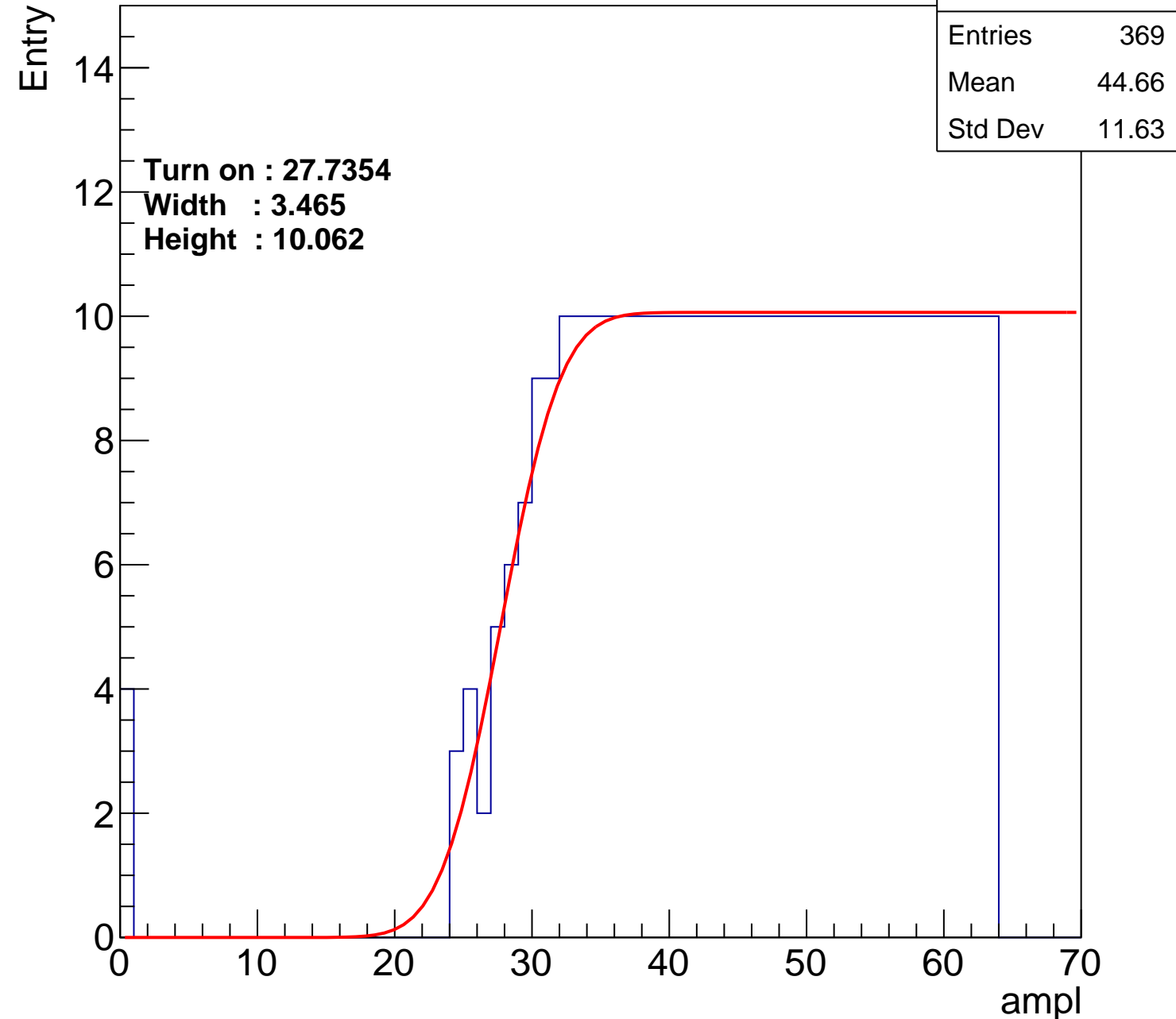
Width : 3.465

Height : 10.062

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U17-ch84

calib_packv5_042523_0143.root, FC#0, port D2

Entries	405
Mean	42.94
Std Dev	12.41

Turn on : 24.0796

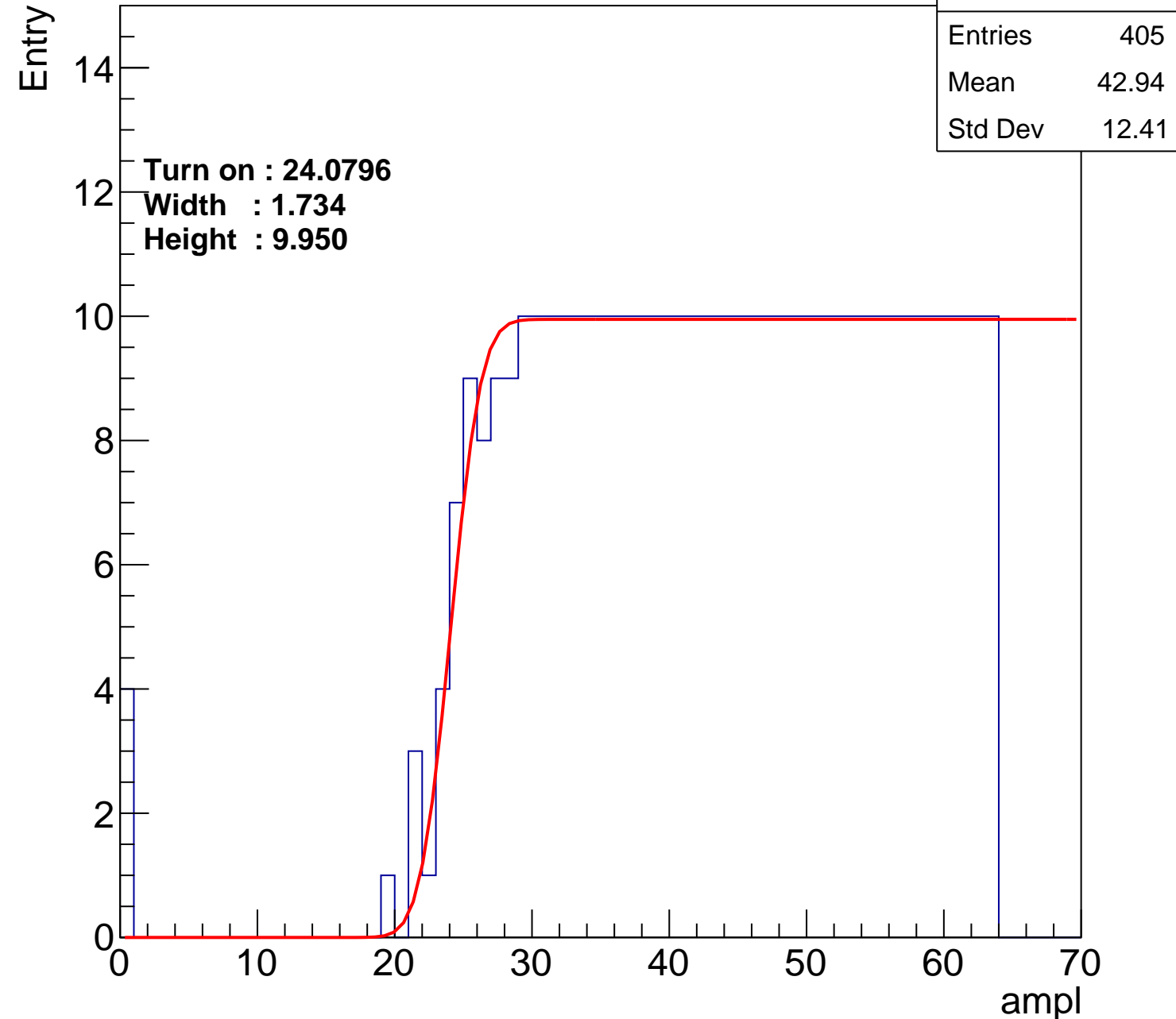
Width : 1.734

Height : 9.950

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U17-ch85

calib_packv5_042523_0143.root, FC#0, port D2

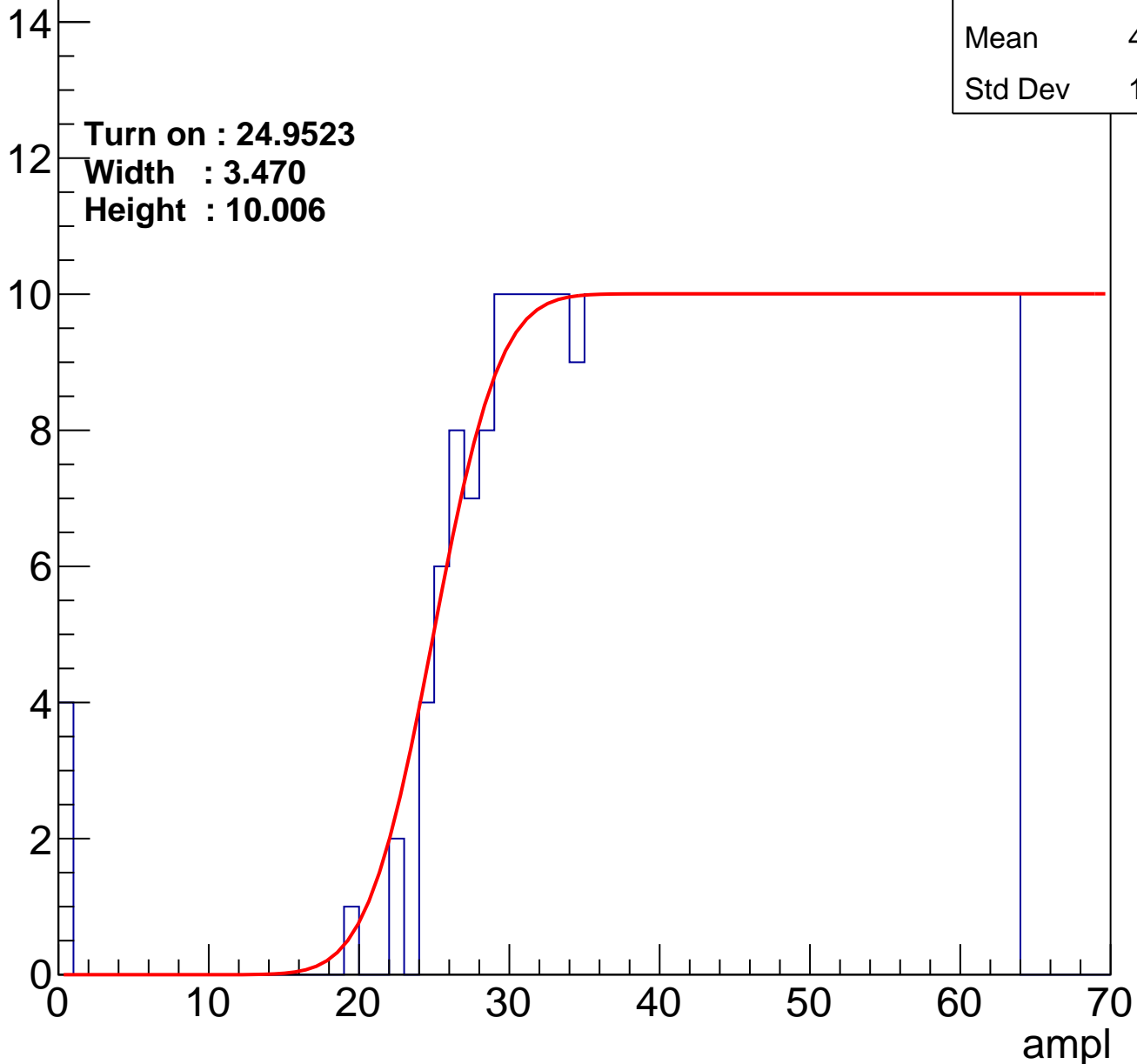
Entries	389
Mean	43.69
Std Dev	12.08

Turn on : 24.9523

Width : 3.470

Height : 10.006

Entry



B1L101S, U17-ch86

calib_packv5_042523_0143.root, FC#0, port D2

Entries	373
Mean	44.4
Std Dev	11.9

Turn on : 27.5526

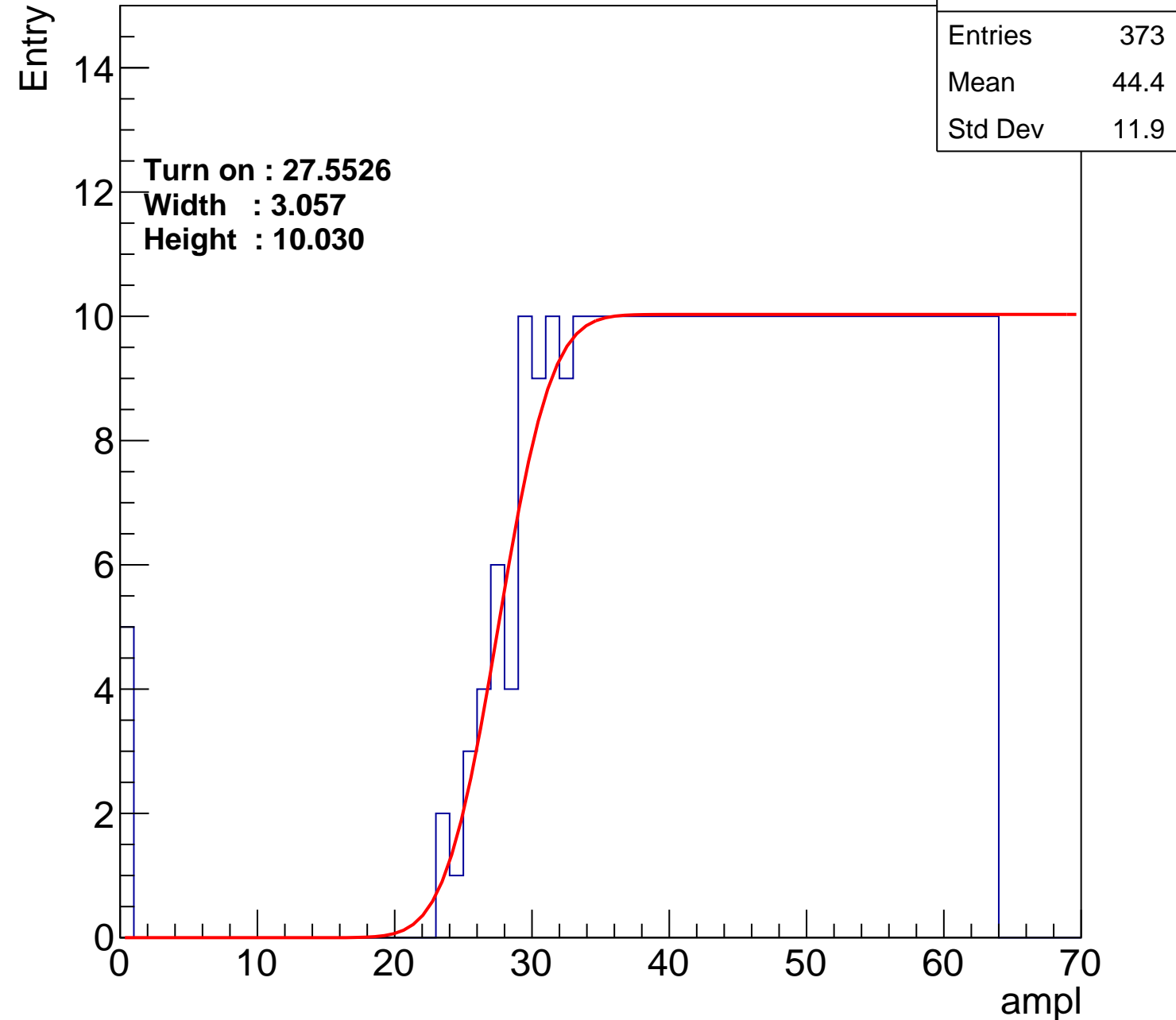
Width : 3.057

Height : 10.030

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U17-ch87

calib_packv5_042523_0143.root, FC#0, port D2

Entries	377
Mean	44.45
Std Dev	11.38

Turn on : 26.7289

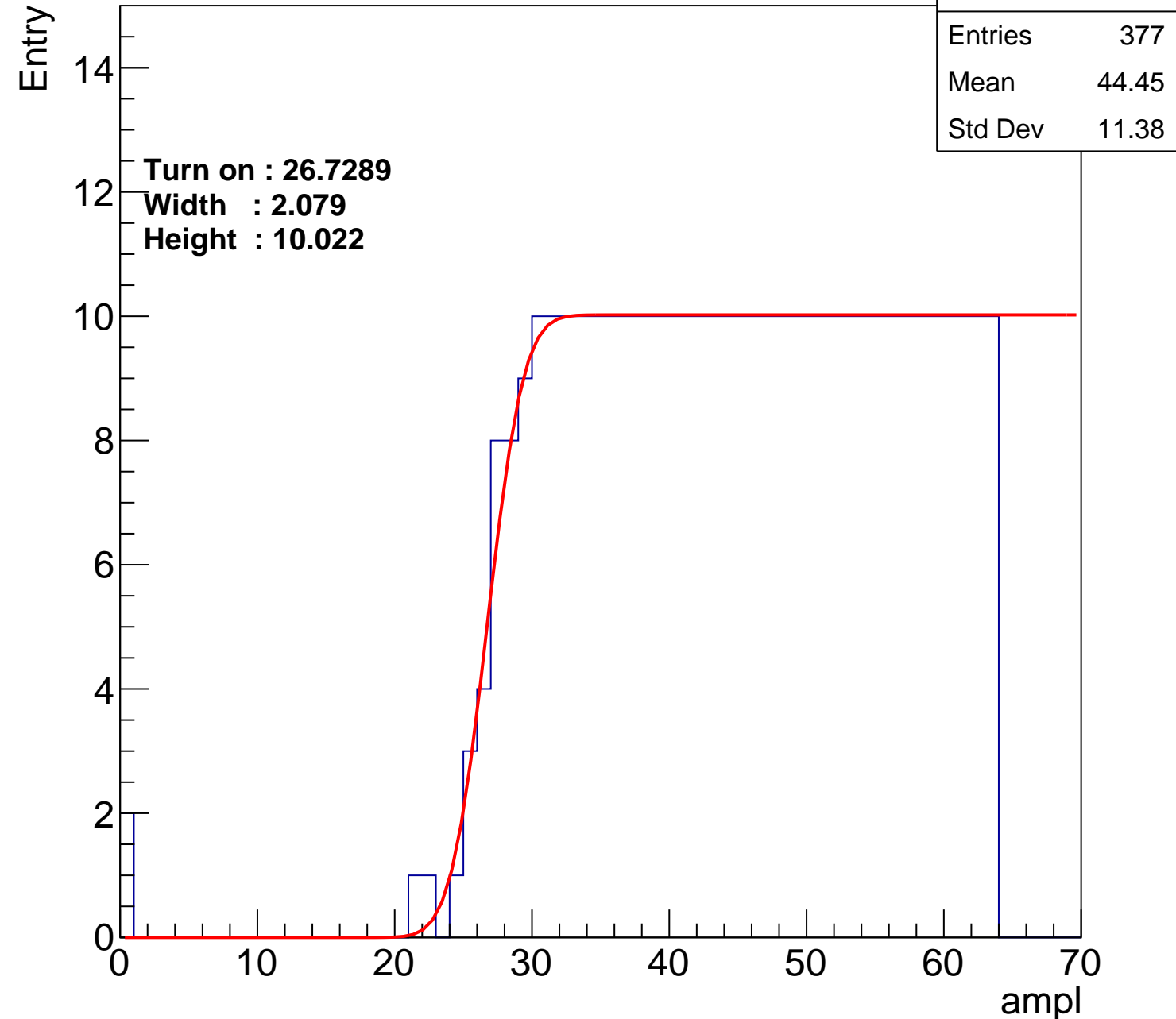
Width : 2.079

Height : 10.022

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U17-ch88

calib_packv5_042523_0143.root, FC#0, port D2

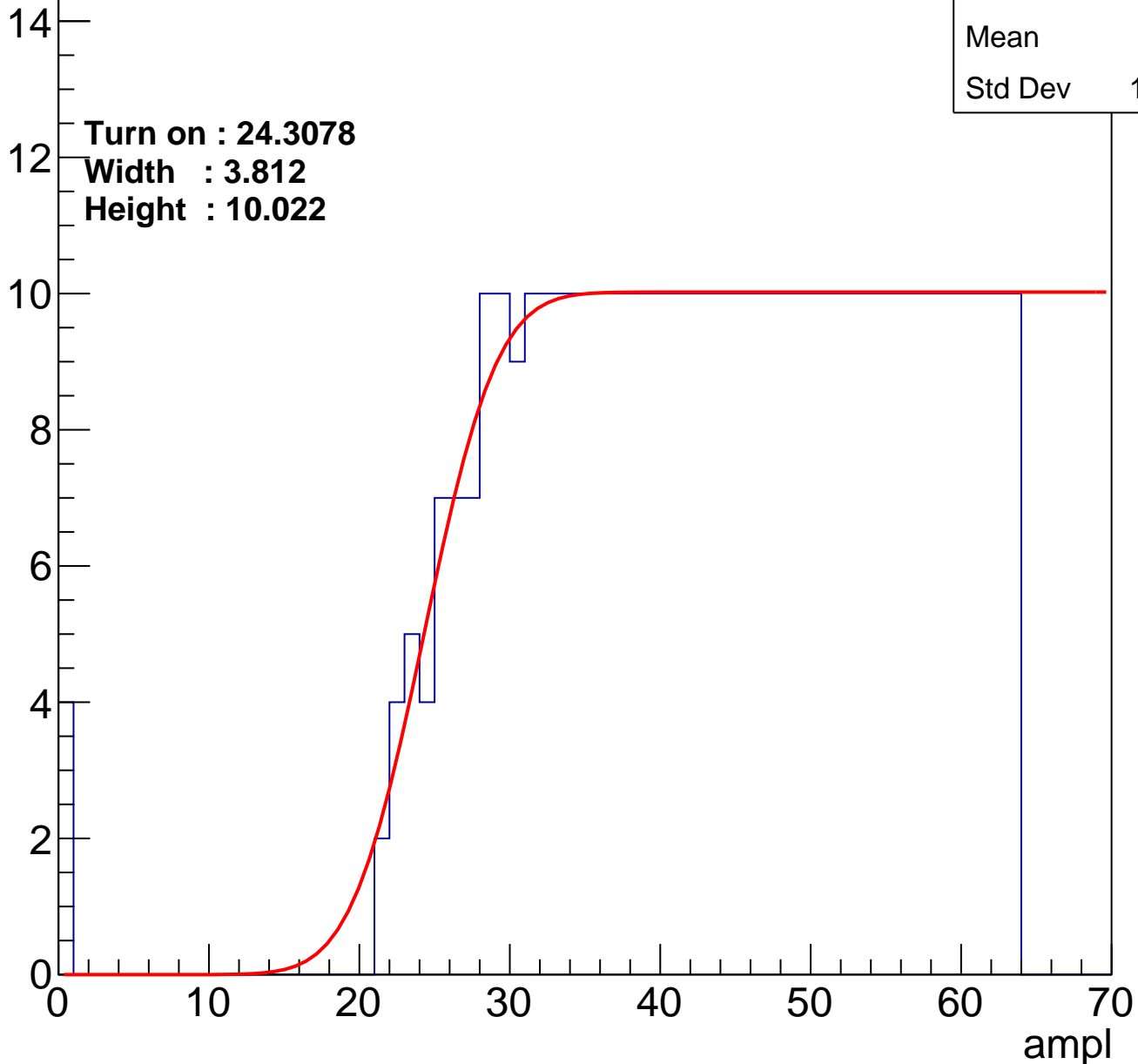
Entries	399
Mean	43.2
Std Dev	12.32

Turn on : 24.3078

Width : 3.812

Height : 10.022

Entry



B1L101S, U17-ch89

calib_packv5_042523_0143.root, FC#0, port D2

Entries	373
Mean	44.45
Std Dev	11.76

Turn on : 26.9430

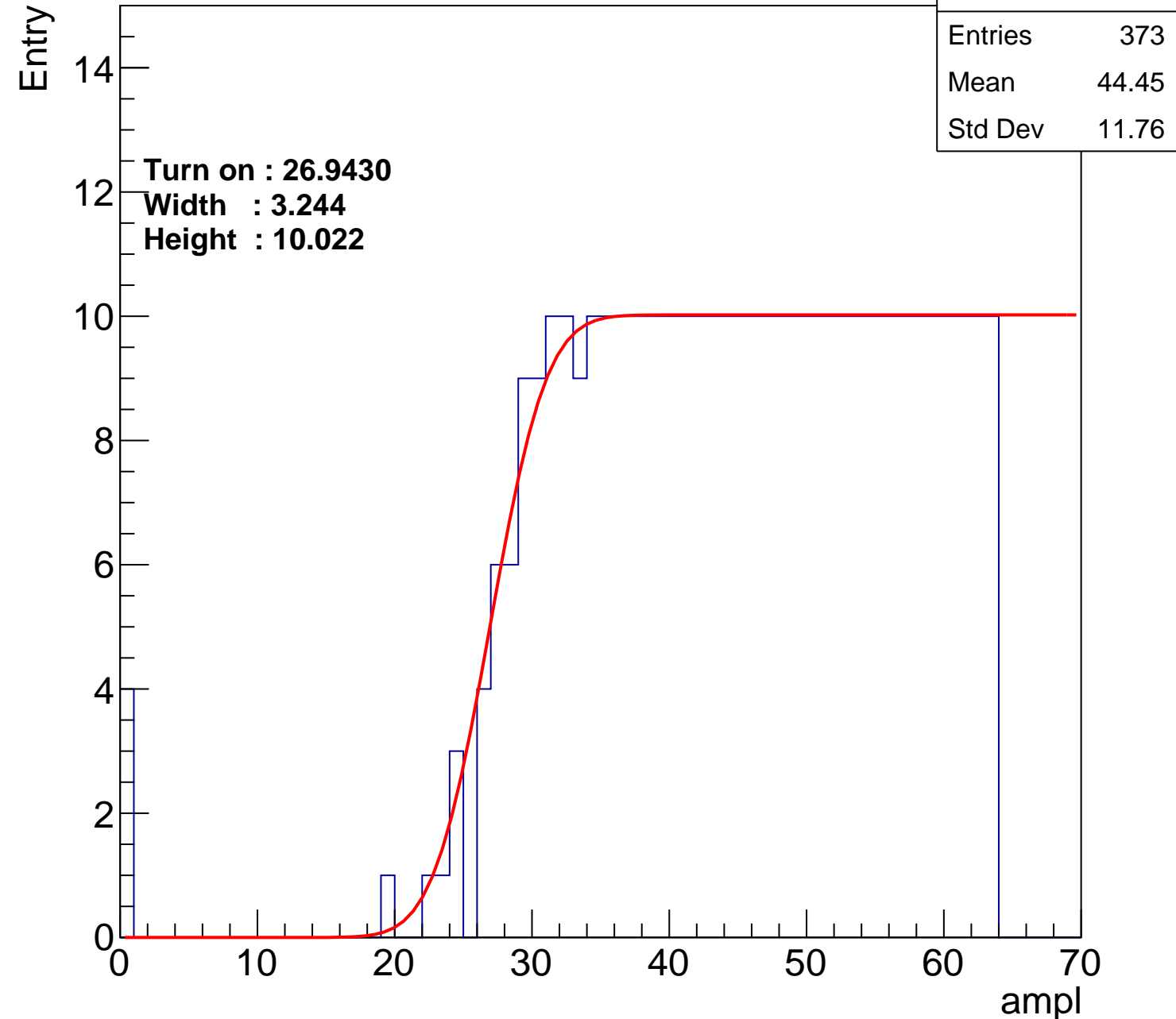
Width : 3.244

Height : 10.022

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U17-ch90

calib_packv5_042523_0143.root, FC#0, port D2

Entries	374
Mean	44.48
Std Dev	11.57

Turn on : 27.5030

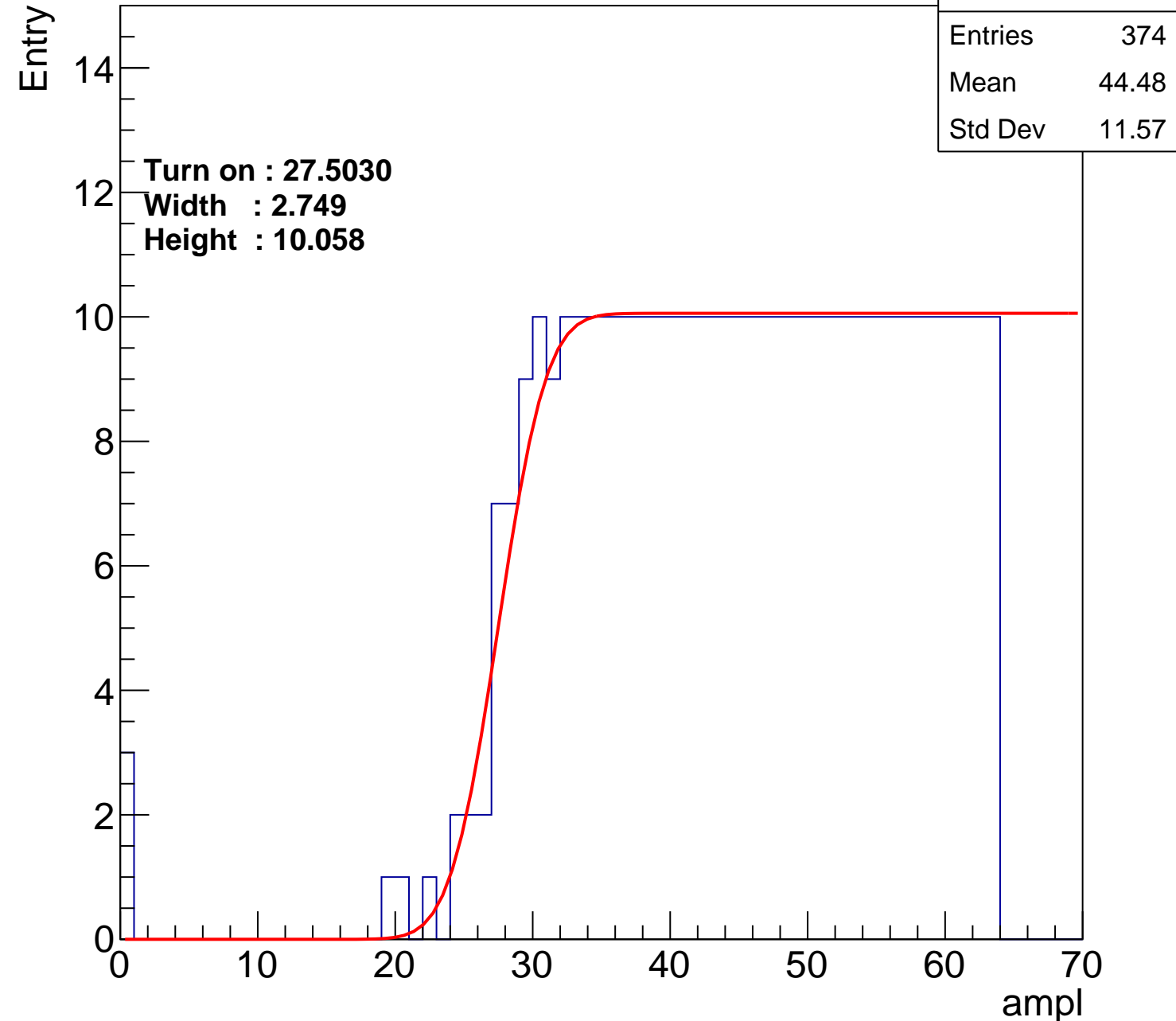
Width : 2.749

Height : 10.058

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U17-ch91

calib_packv5_042523_0143.root, FC#0, port D2

Entries	356
Mean	45.3
Std Dev	11.32

Turn on : 28.3700

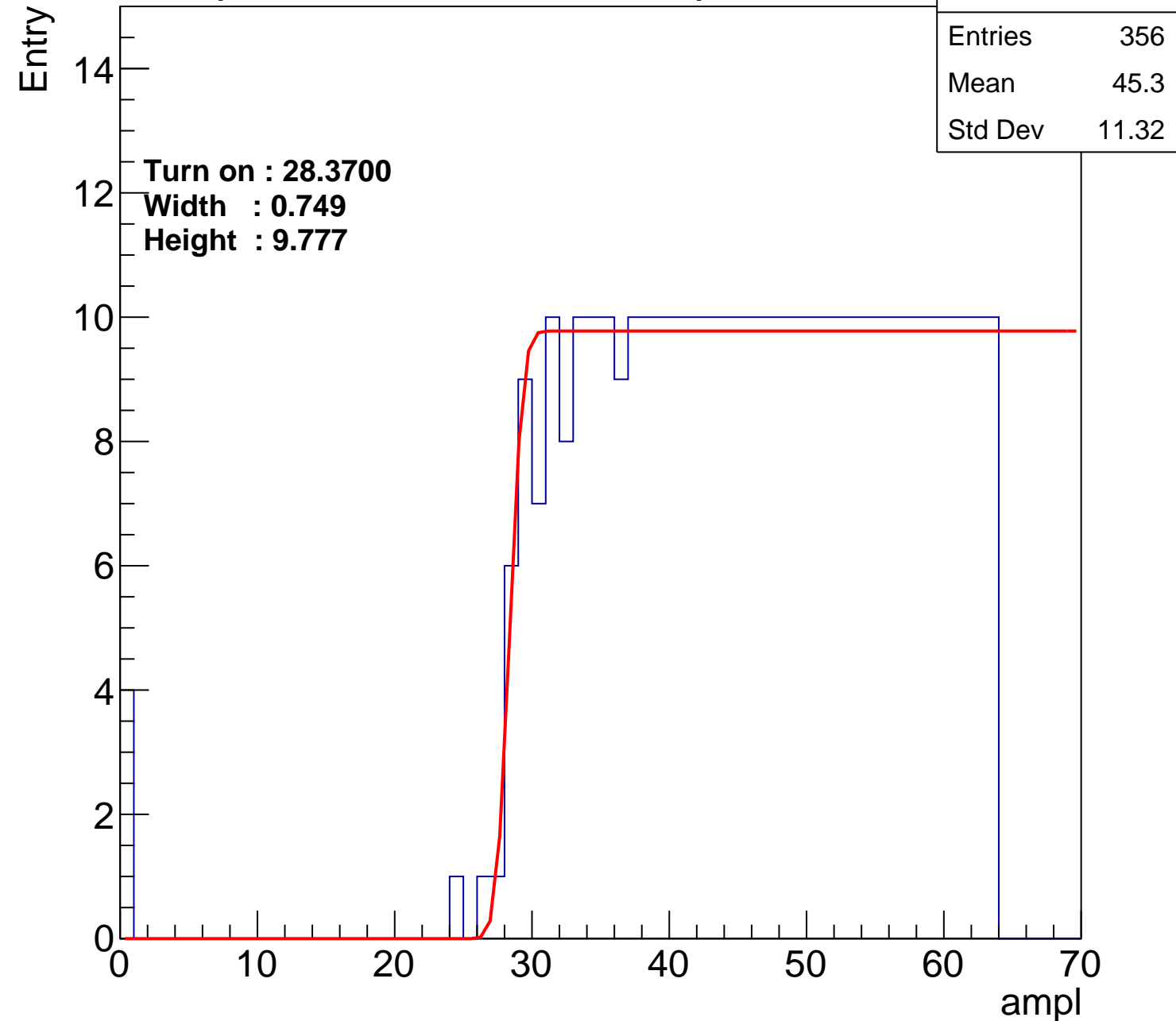
Width : 0.749

Height : 9.777

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U17-ch92

calib_packv5_042523_0143.root, FC#0, port D2

Entries	383
Mean	43.94
Std Dev	12.07

Turn on : 25.3499

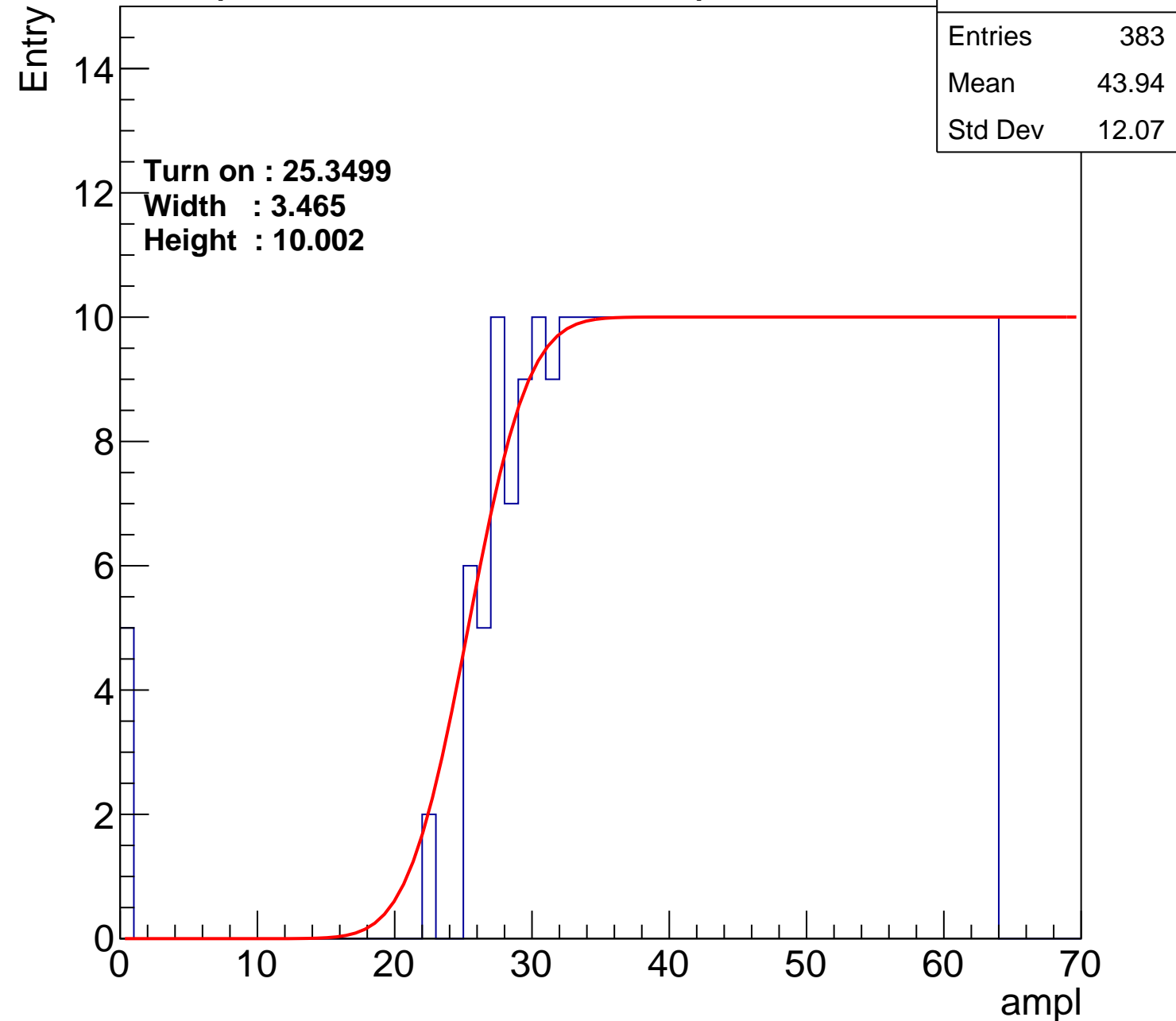
Width : 3.465

Height : 10.002

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U17-ch93

calib_packv5_042523_0143.root, FC#0, port D2

Entries	370
Mean	44.52
Std Dev	11.8

Turn on : 28.3003

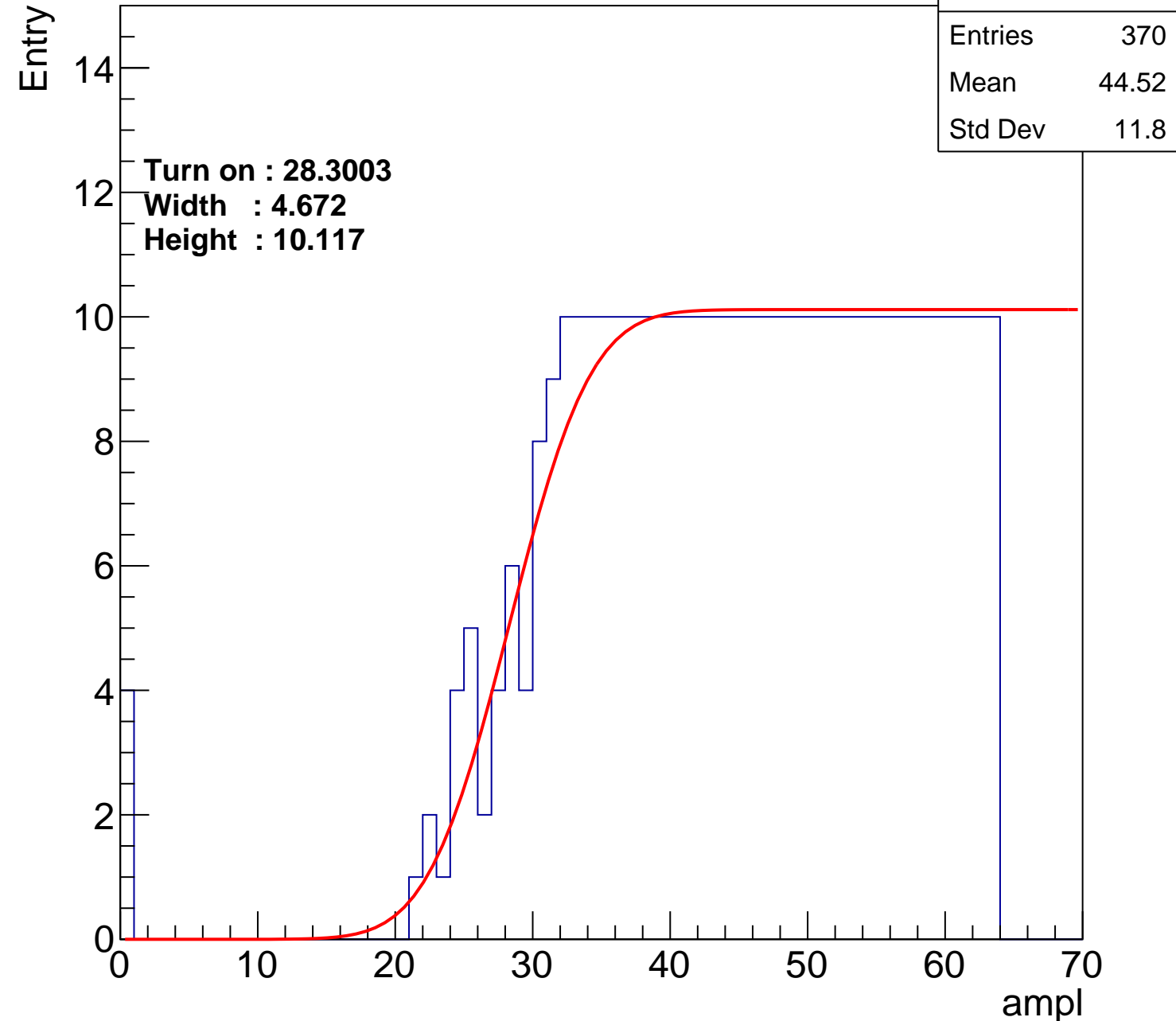
Width : 4.672

Height : 10.117

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U17-ch94

calib_packv5_042523_0143.root, FC#0, port D2

Entries	387
Mean	43.79
Std Dev	11.98

Turn on : 25.9417

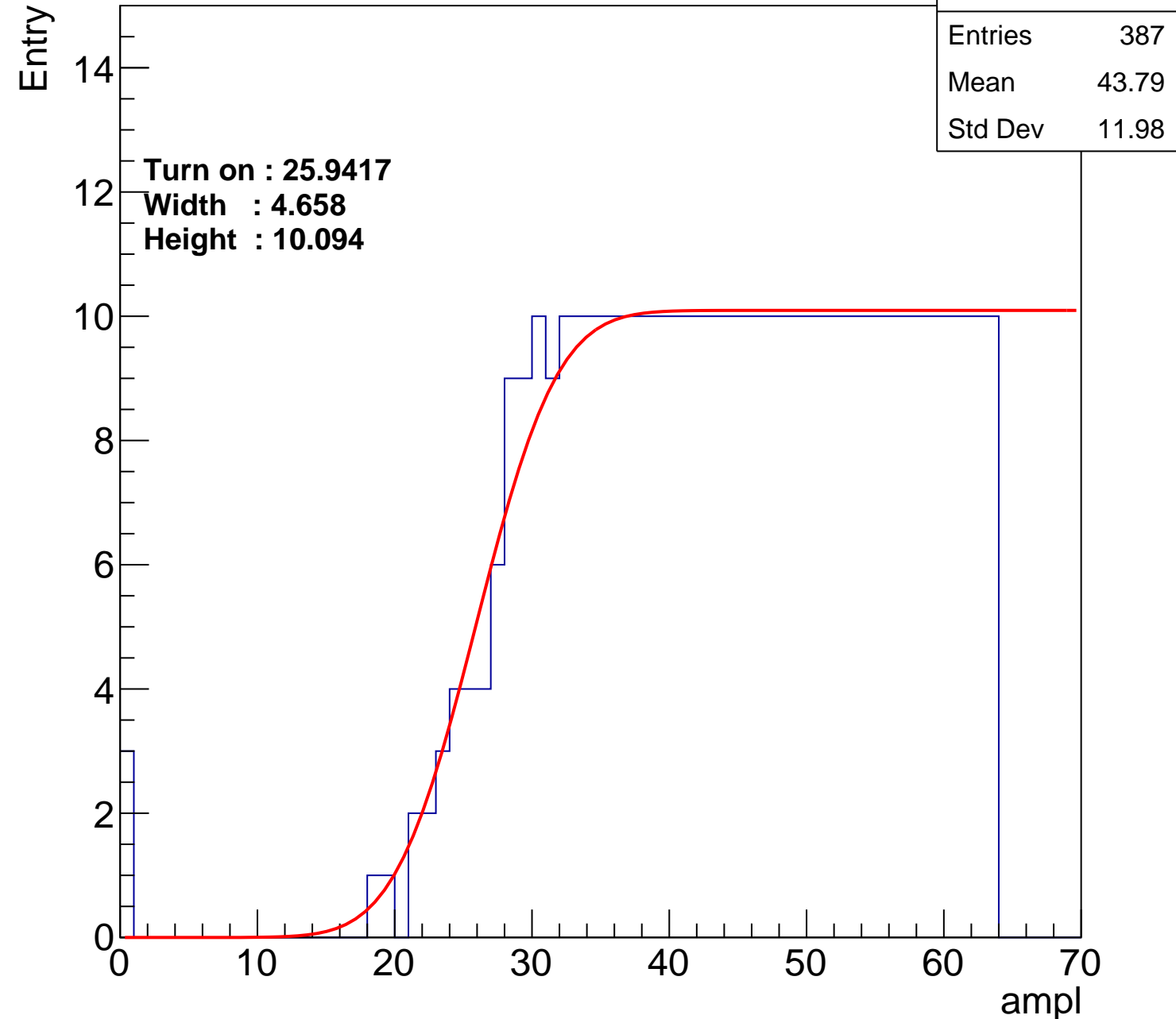
Width : 4.658

Height : 10.094

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U17-ch95

calib_packv5_042523_0143.root, FC#0, port D2

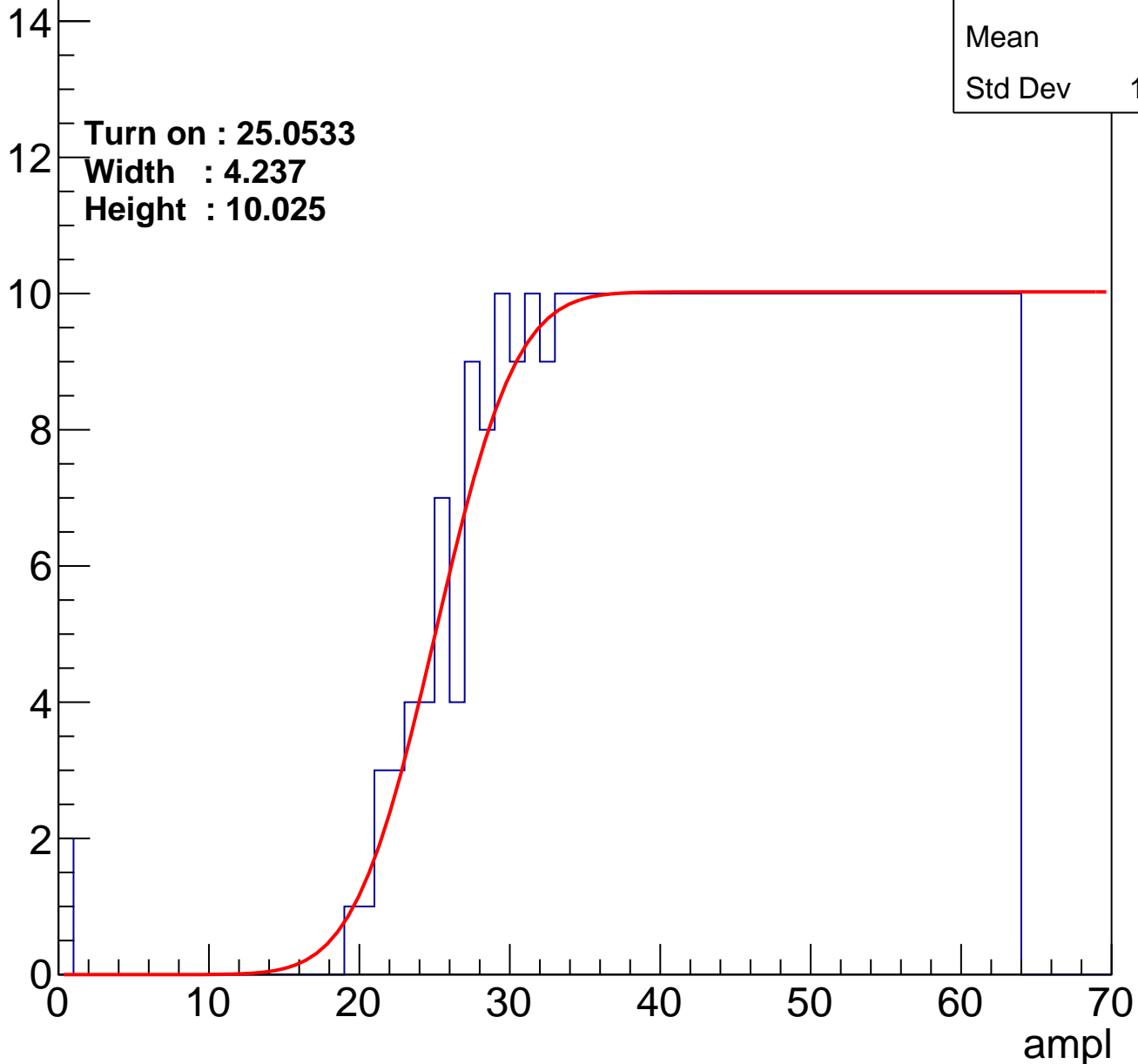
Entries	394
Mean	43.5
Std Dev	11.99

Turn on : 25.0533

Width : 4.237

Height : 10.025

Entry



B1L101S, U17-ch96

calib_packv5_042523_0143.root, FC#0, port D2

Entries	393
Mean	43.5
Std Dev	12.32

Turn on : 25.7244

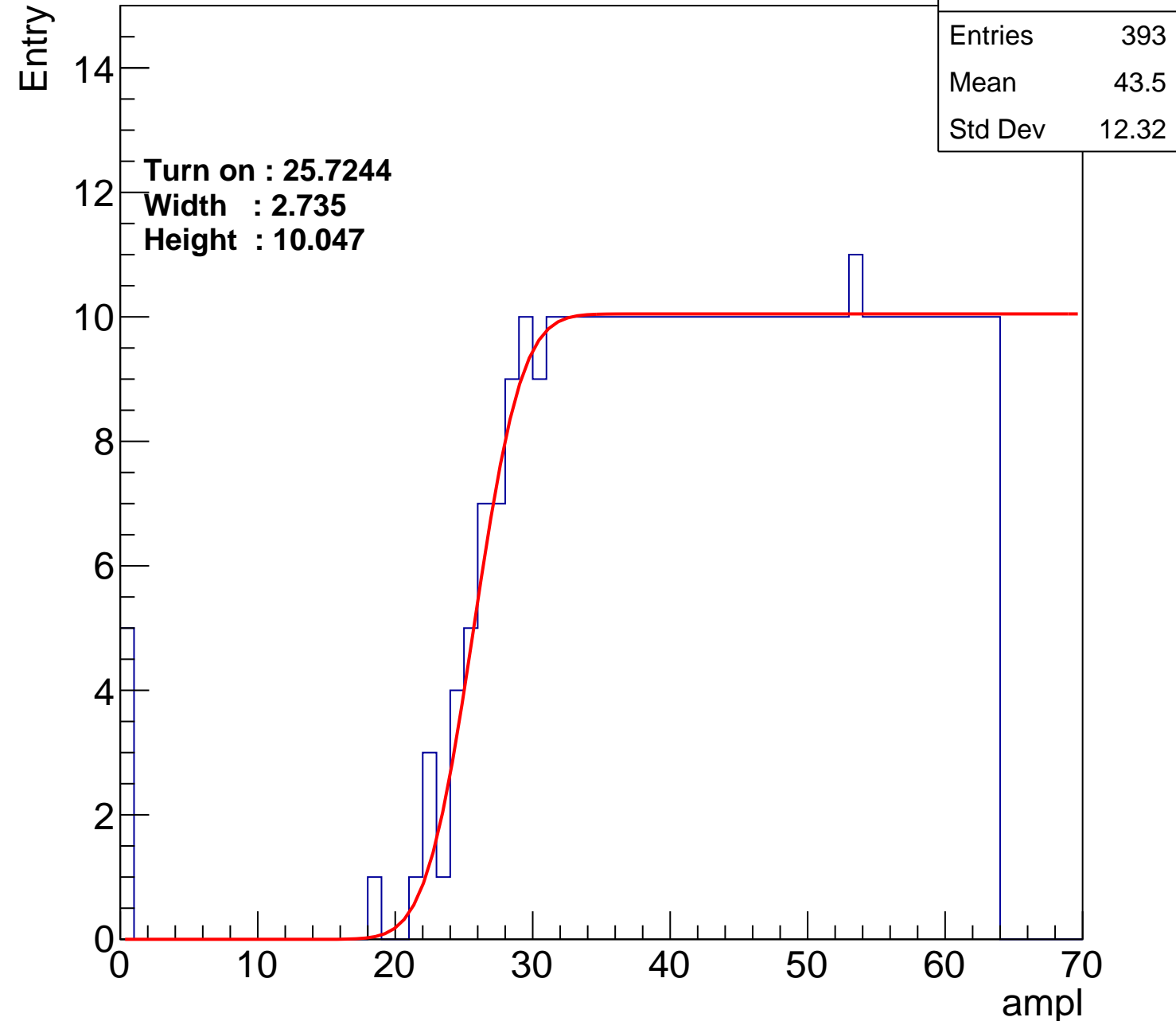
Width : 2.735

Height : 10.047

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U17-ch97

calib_packv5_042523_0143.root, FC#0, port D2

Entries	362
Mean	45.08
Std Dev	11.26

Turn on : 28.5026

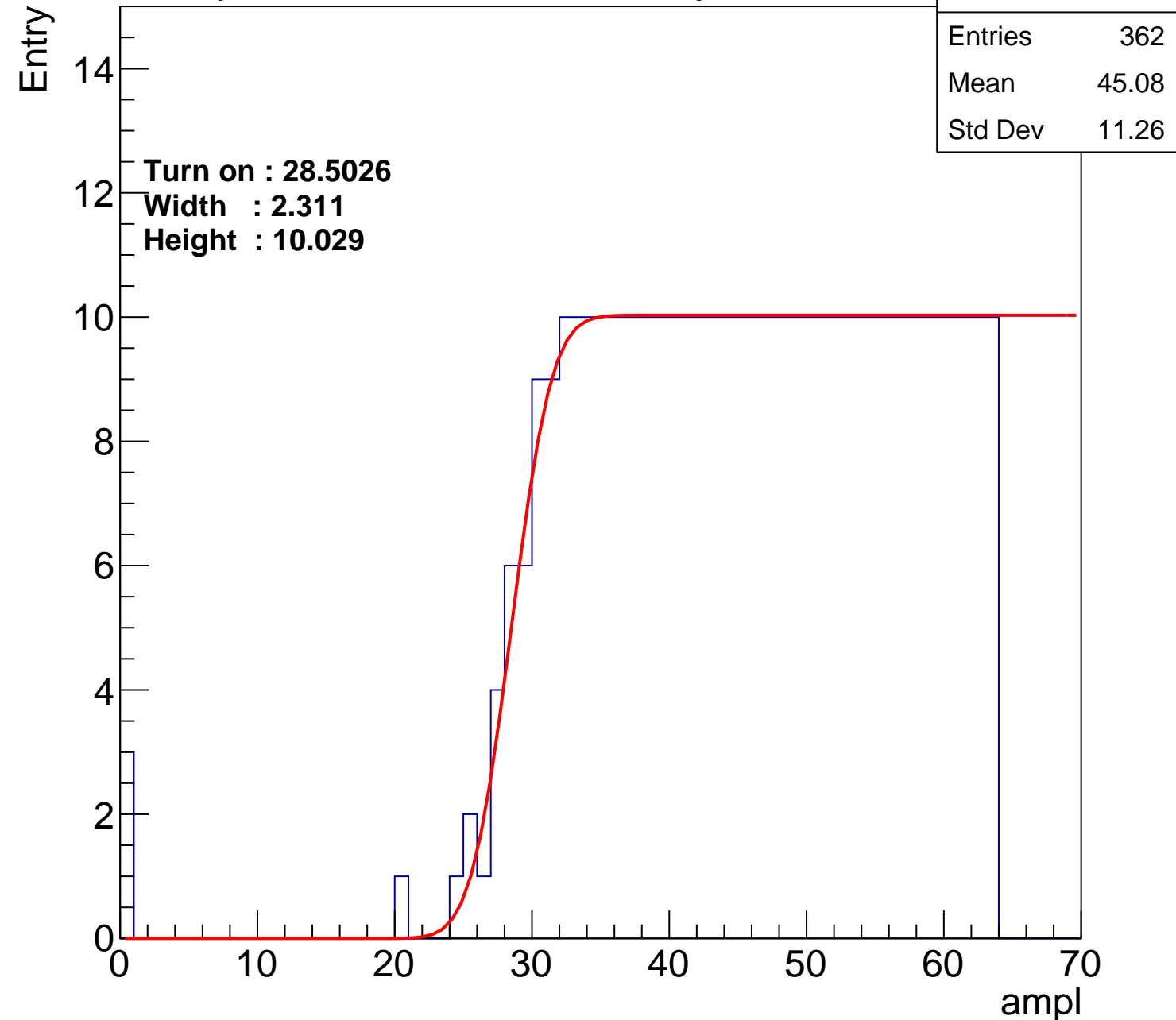
Width : 2.311

Height : 10.029

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U17-ch98

calib_packv5_042523_0143.root, FC#0, port D2

Entries	390
Mean	43.7
Std Dev	11.95

Turn on : 25.2819

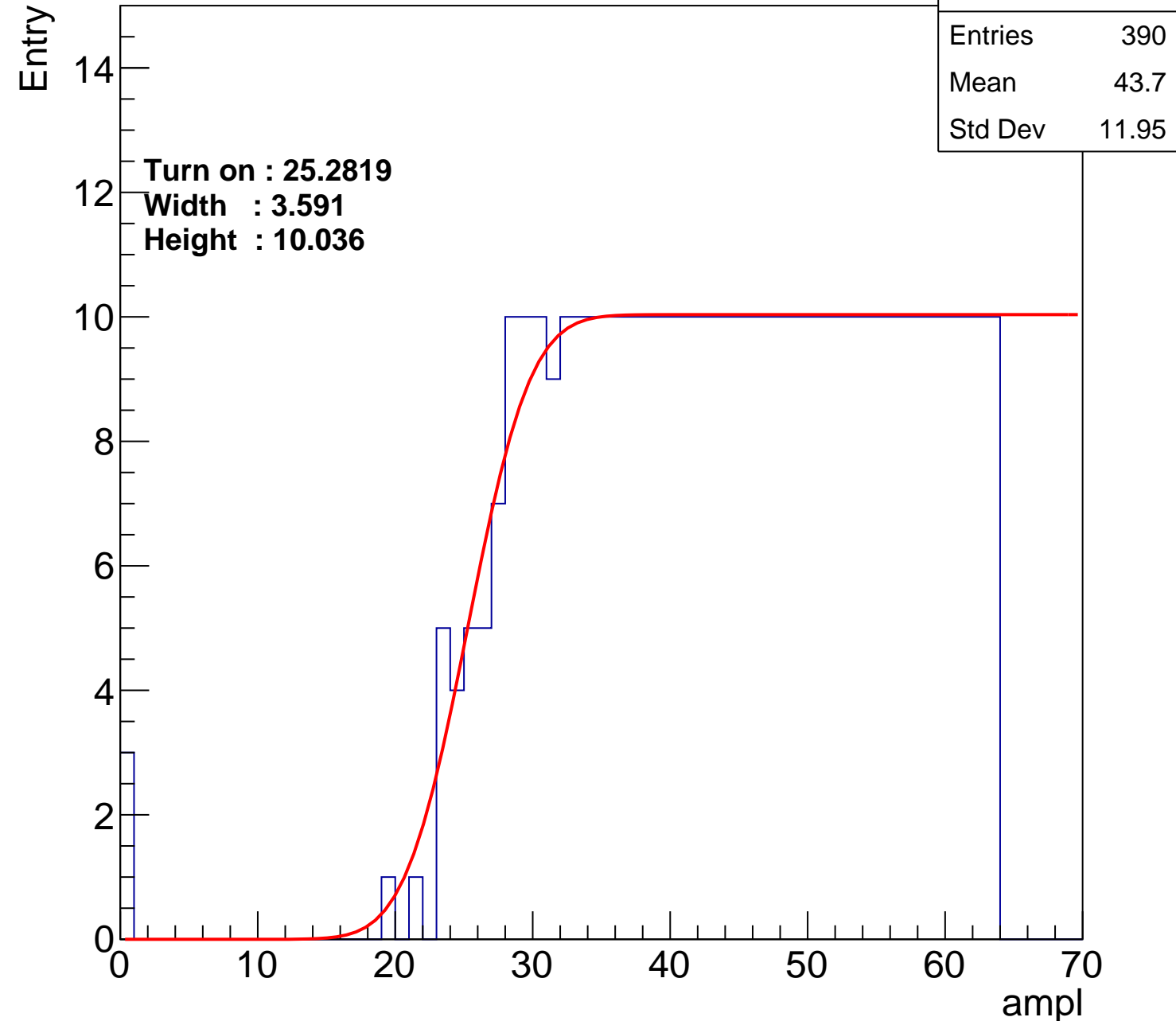
Width : 3.591

Height : 10.036

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U17-ch99

calib_packv5_042523_0143.root, FC#0, port D2

Entries	359
Mean	45.08
Std Dev	11.6

Turn on : 28.6645

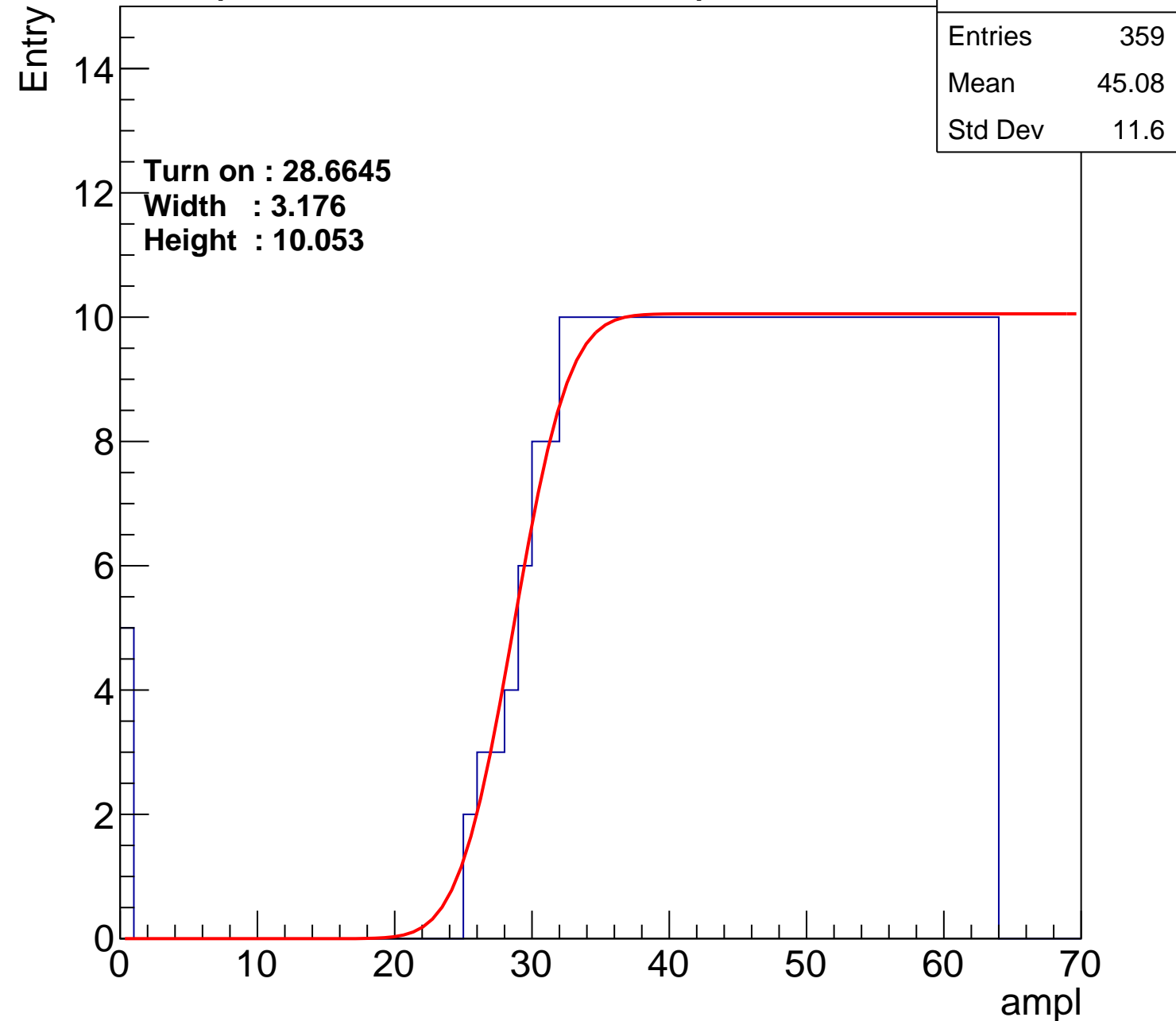
Width : 3.176

Height : 10.053

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U17-ch100

calib_packv5_042523_0143.root, FC#0, port D2

Entries	375
Mean	44.33
Std Dev	11.81

Turn on : 26.8175

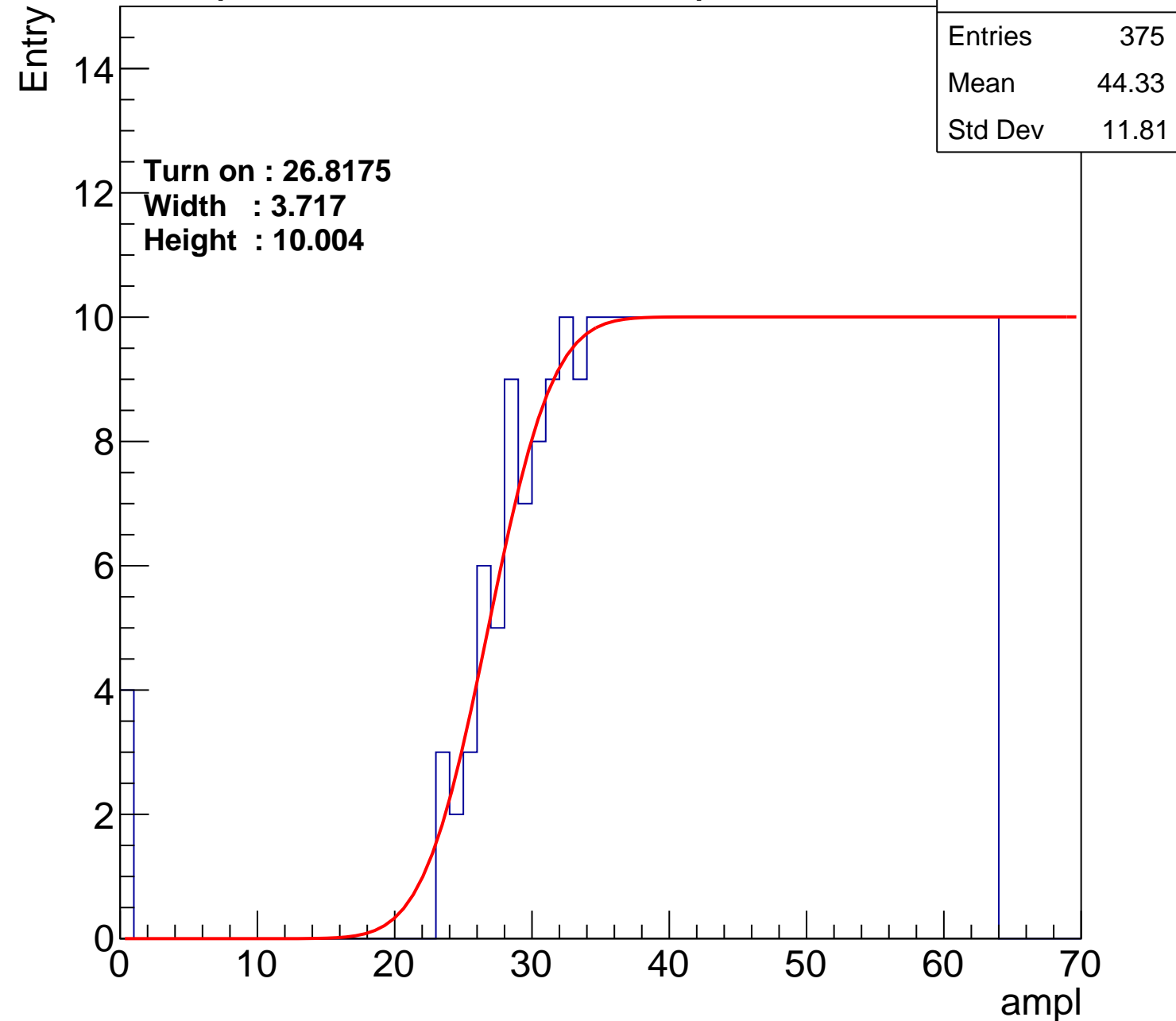
Width : 3.717

Height : 10.004

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U17-ch101

calib_packv5_042523_0143.root, FC#0, port D2

Entries	388
Mean	43.49
Std Dev	12.69

Turn on : 26.0623

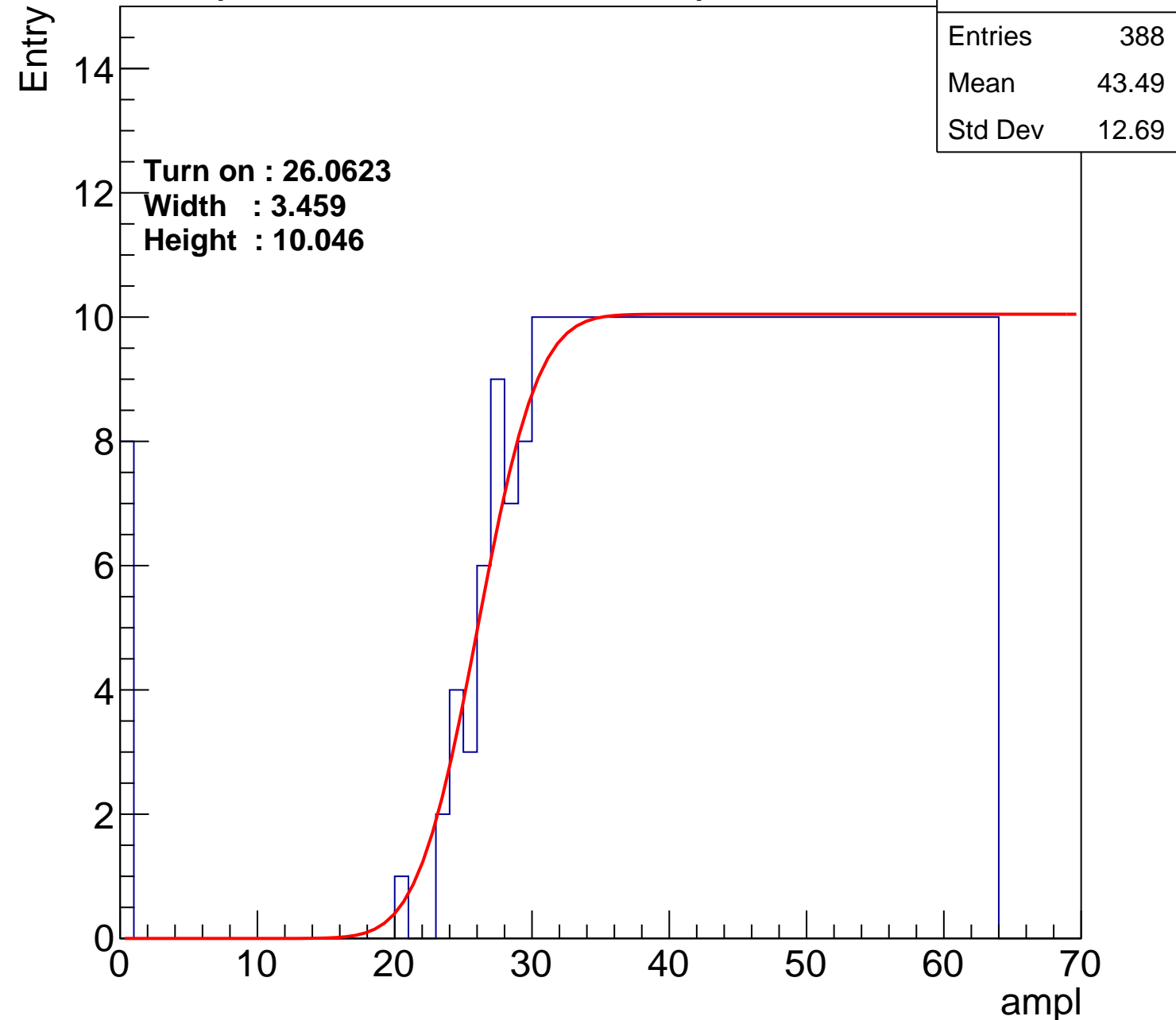
Width : 3.459

Height : 10.046

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U17-ch102

calib_packv5_042523_0143.root, FC#0, port D2

Entries	411
Mean	42.54
Std Dev	12.78

Turn on : 24.0066

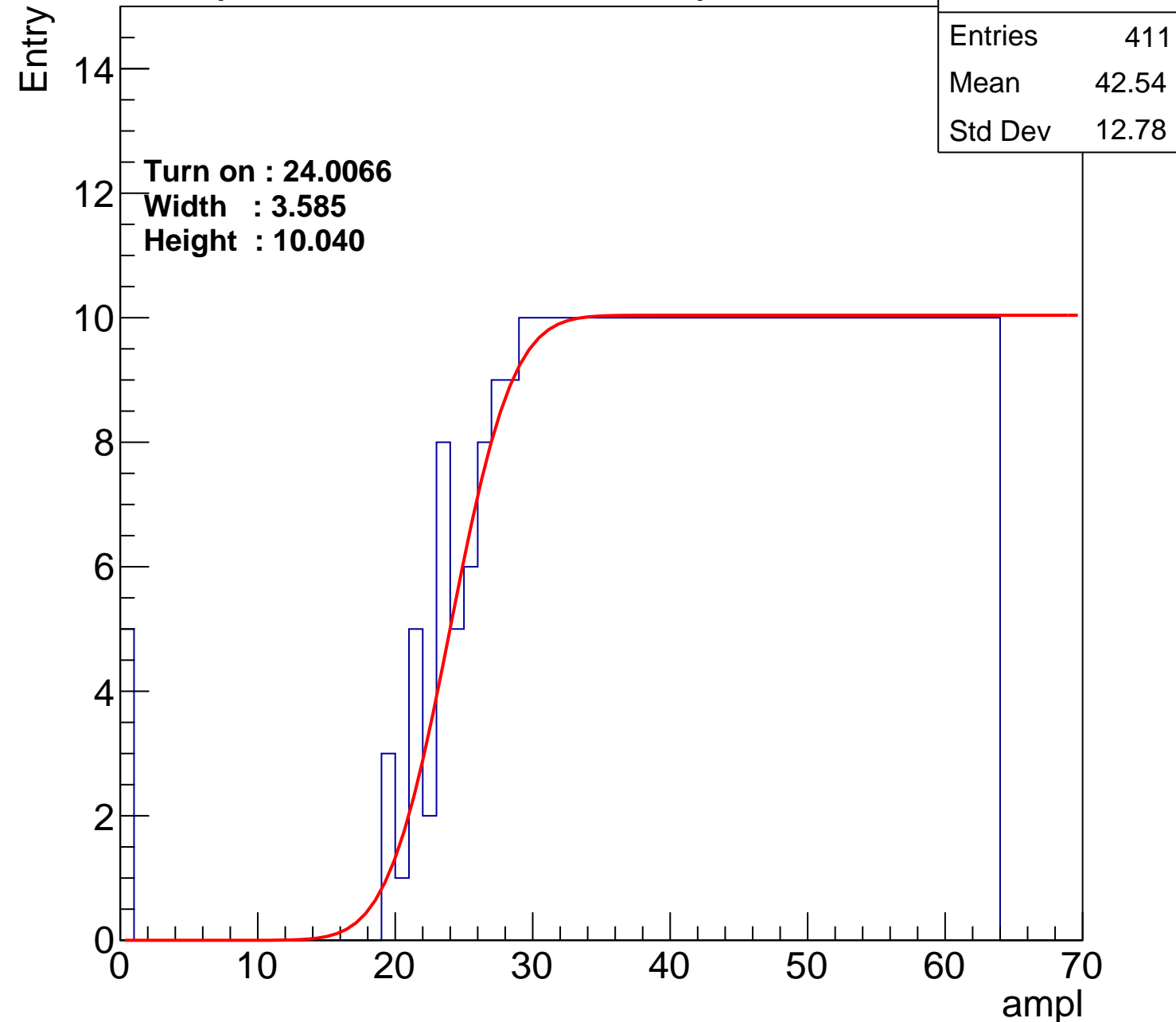
Width : 3.585

Height : 10.040

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U17-ch103

calib_packv5_042523_0143.root, FC#0, port D2

Entries	351
Mean	45.41
Std Dev	11.52

Turn on : 30.2412

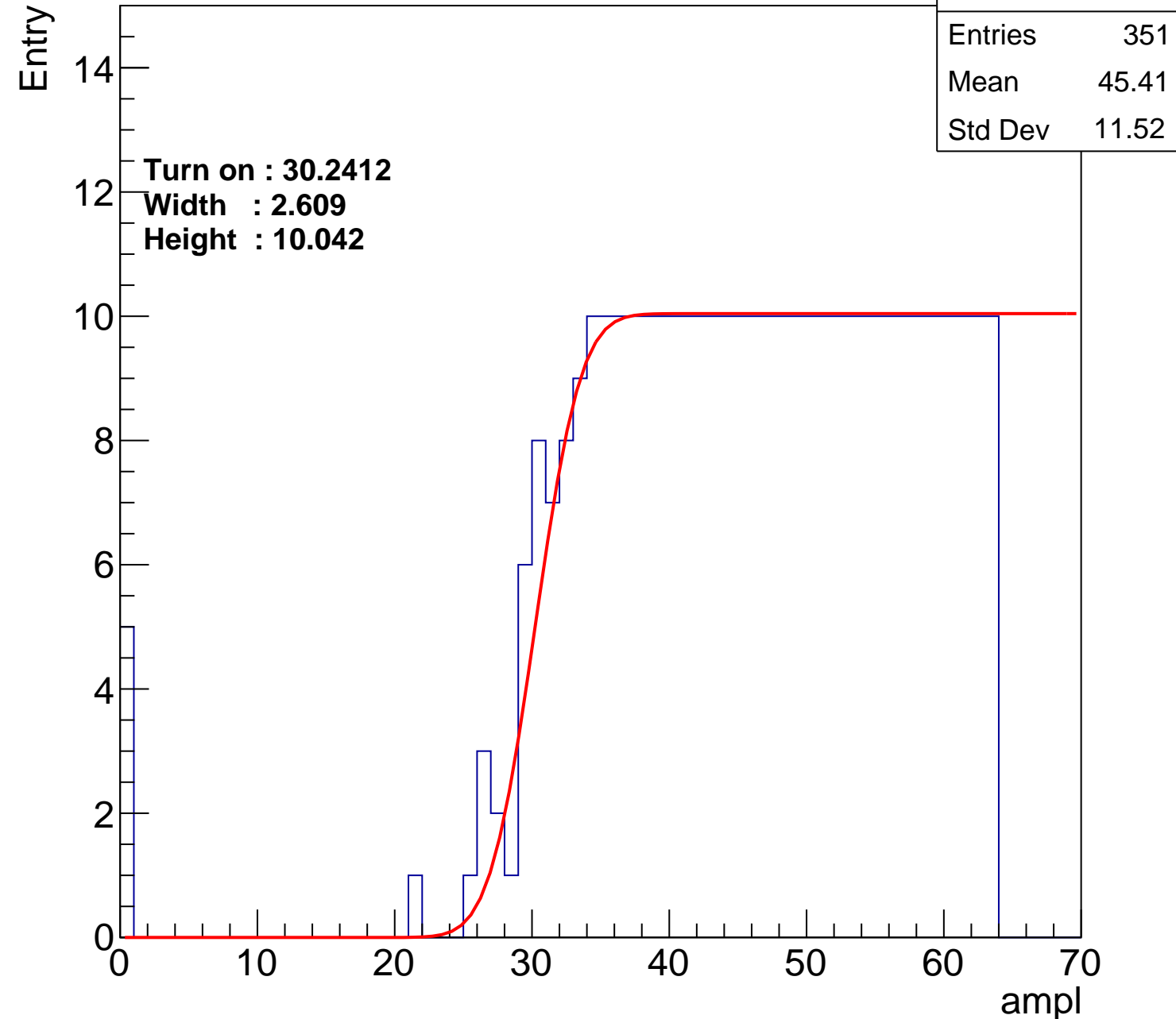
Width : 2.609

Height : 10.042

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U17-ch104

calib_packv5_042523_0143.root, FC#0, port D2

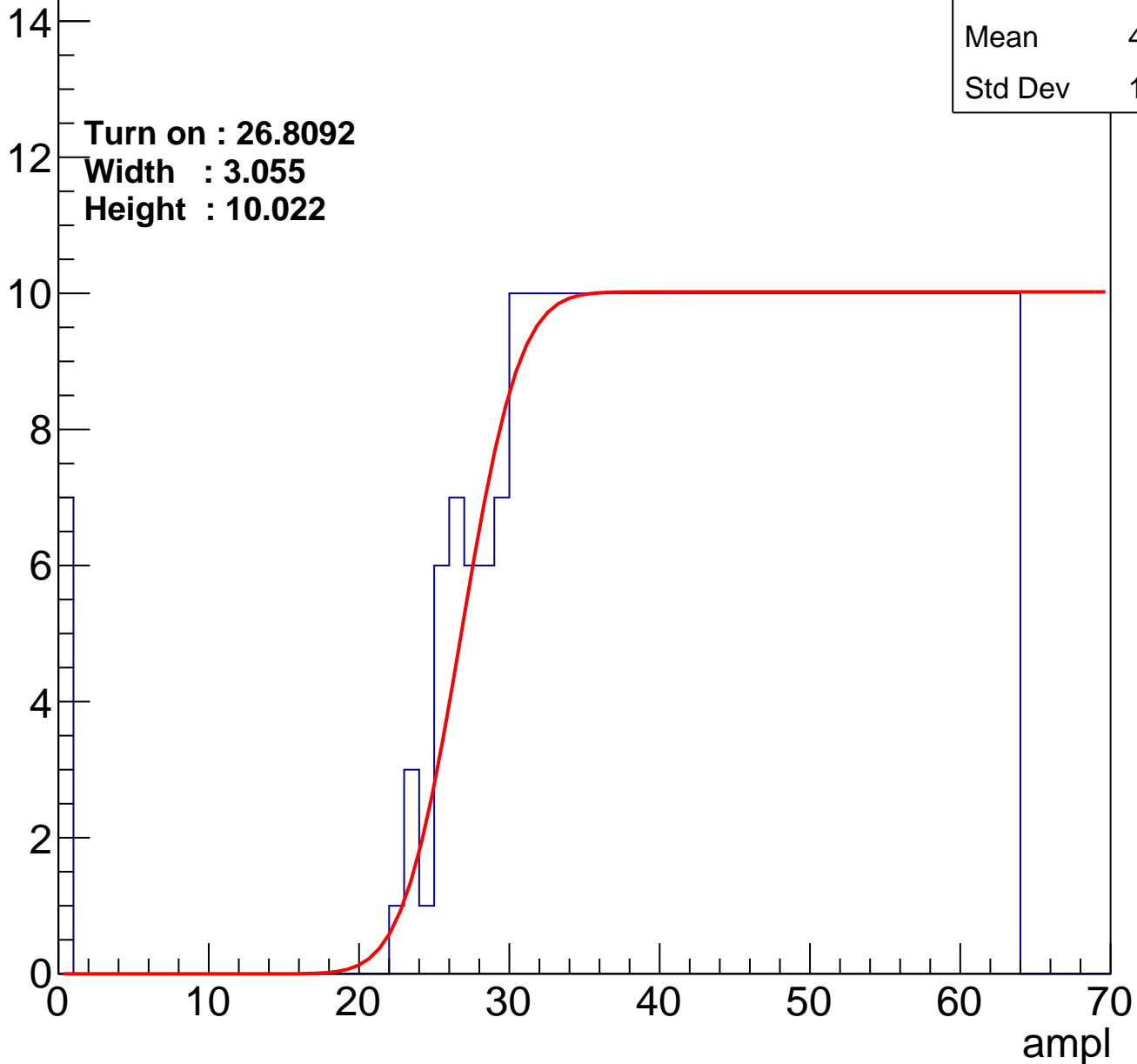
Entries	384
Mean	43.72
Std Dev	12.49

Turn on : 26.8092

Width : 3.055

Height : 10.022

Entry



B1L101S, U17-ch105

calib_packv5_042523_0143.root, FC#0, port D2

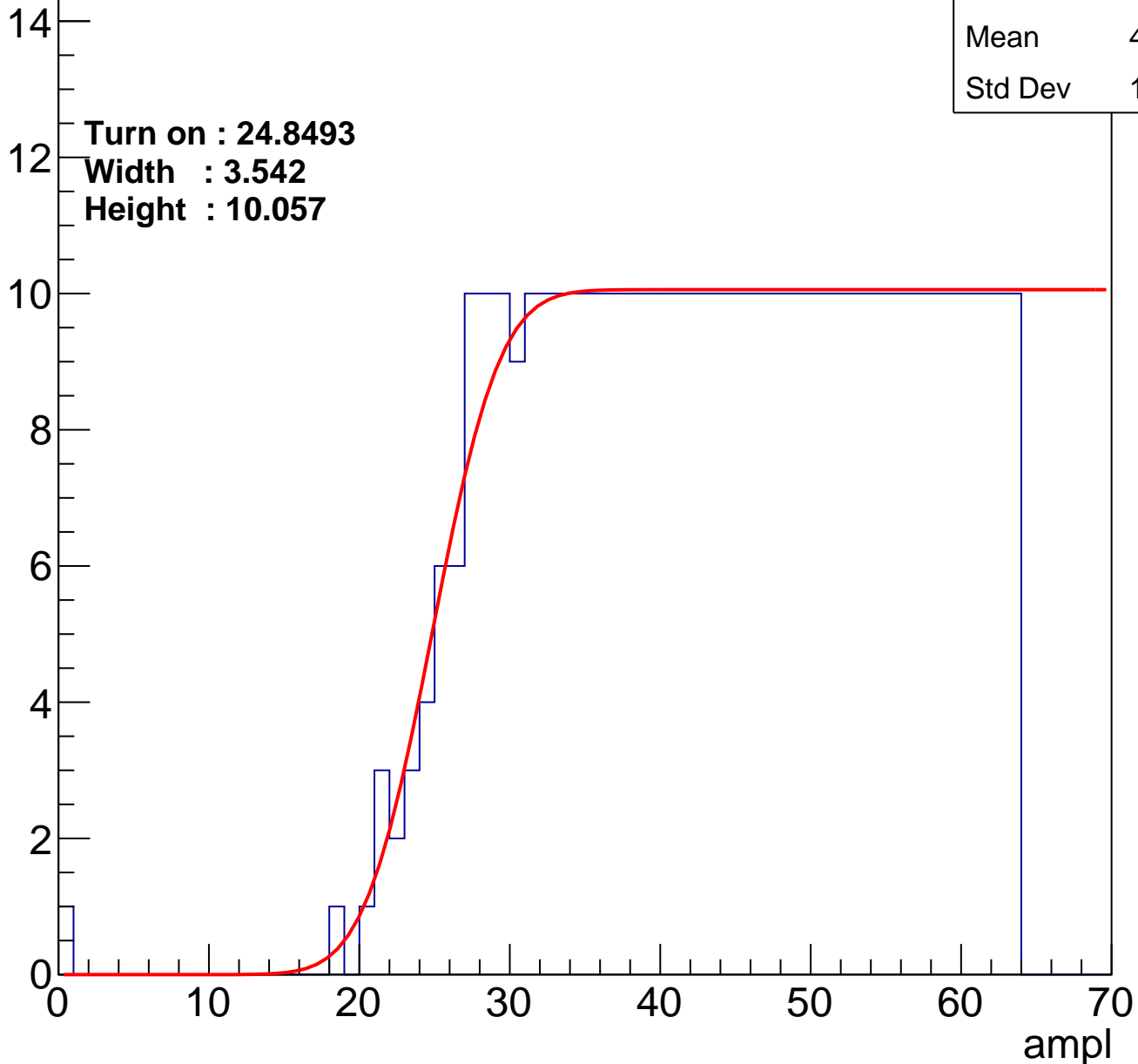
Entries	396
Mean	43.53
Std Dev	11.79

Turn on : 24.8493

Width : 3.542

Height : 10.057

Entry



B1L101S, U17-ch106

calib_packv5_042523_0143.root, FC#0, port D2

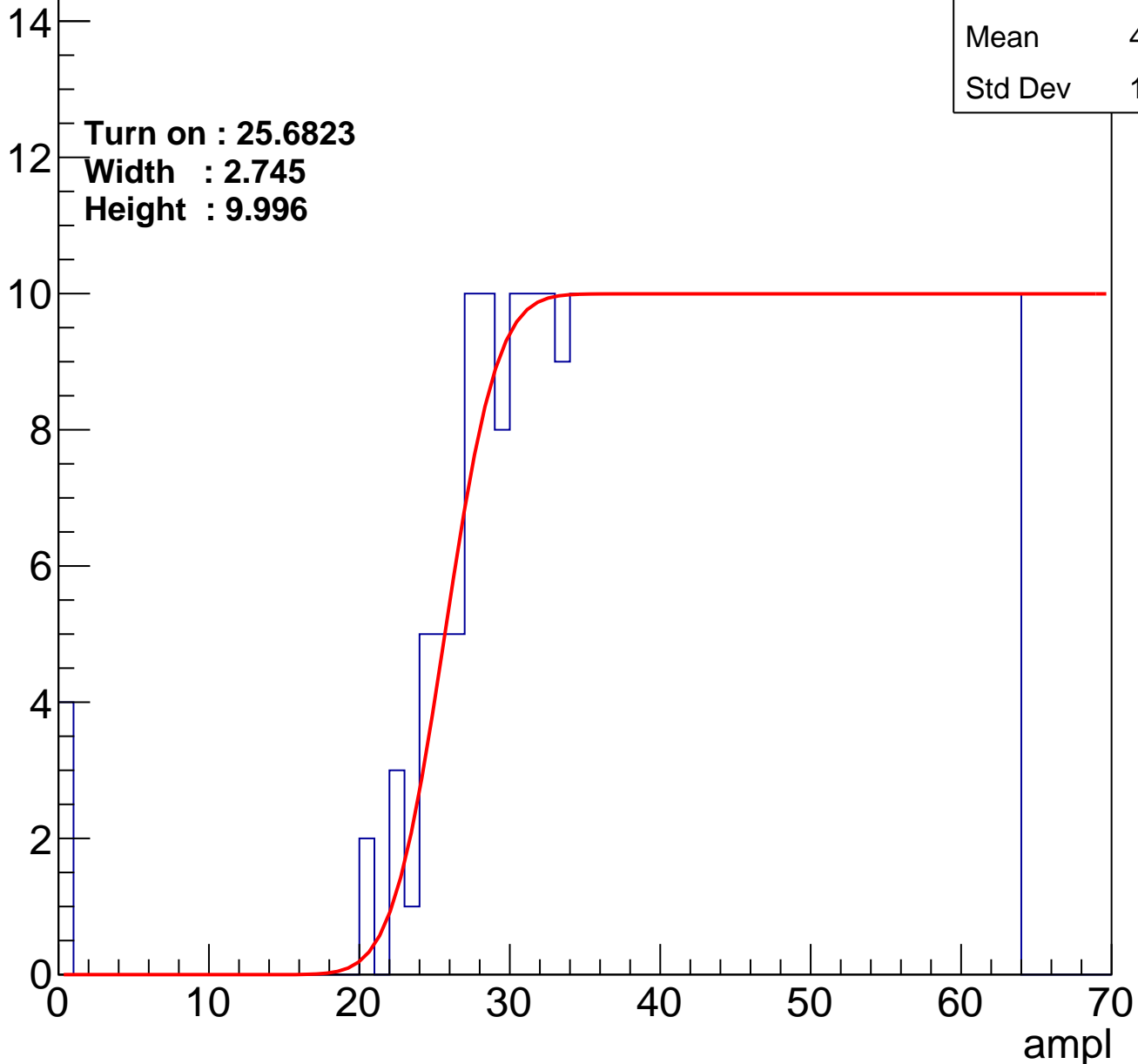
Entries	392
Mean	43.53
Std Dev	12.17

Turn on : 25.6823

Width : 2.745

Height : 9.996

Entry



B1L101S, U17-ch107

calib_packv5_042523_0143.root, FC#0, port D2

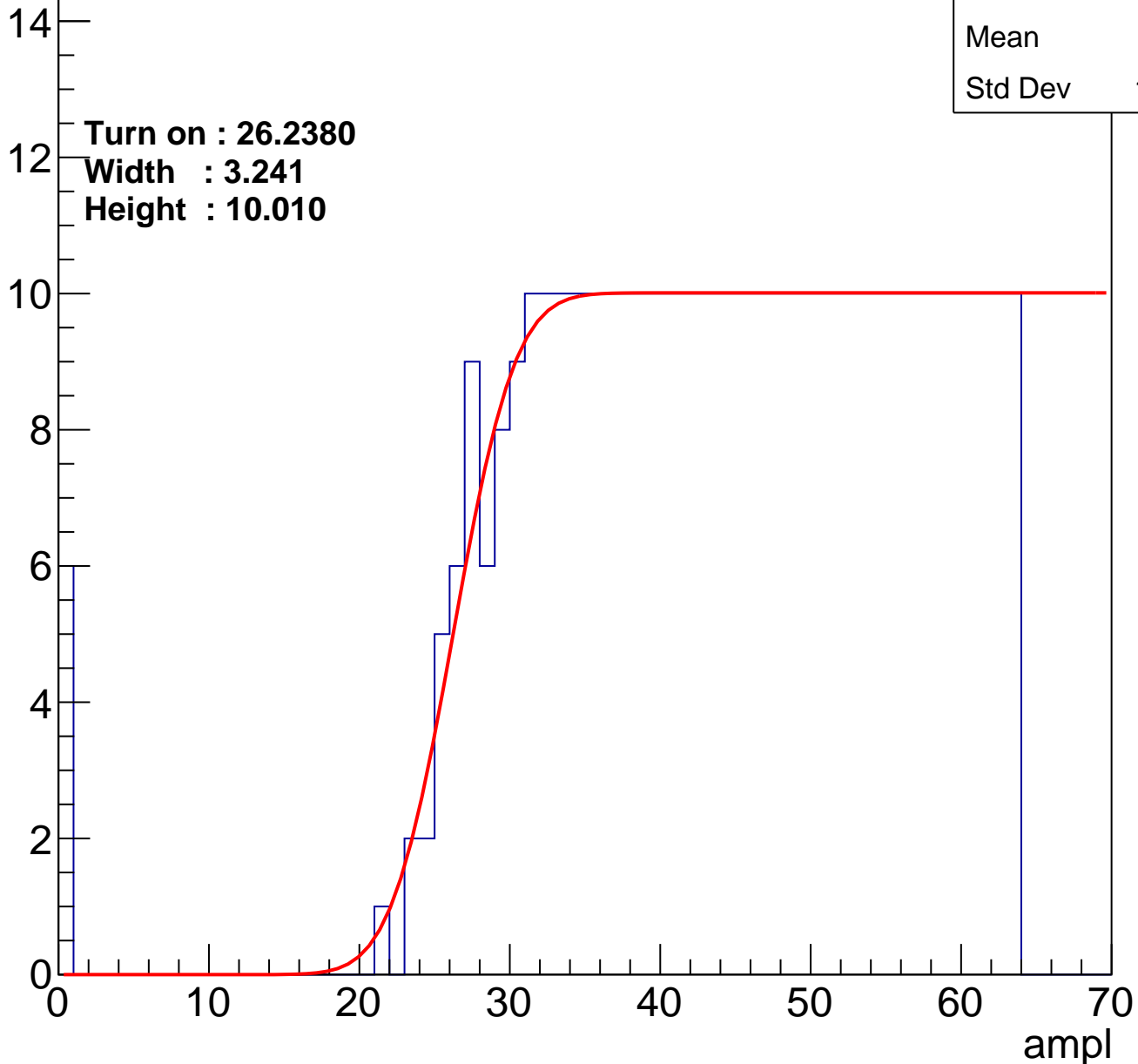
Entries	384
Mean	43.8
Std Dev	12.31

Turn on : 26.2380

Width : 3.241

Height : 10.010

Entry



B1L101S, U17-ch108

calib_packv5_042523_0143.root, FC#0, port D2

Entries	373
Mean	44.18
Std Dev	12.38

Turn on : 28.7320

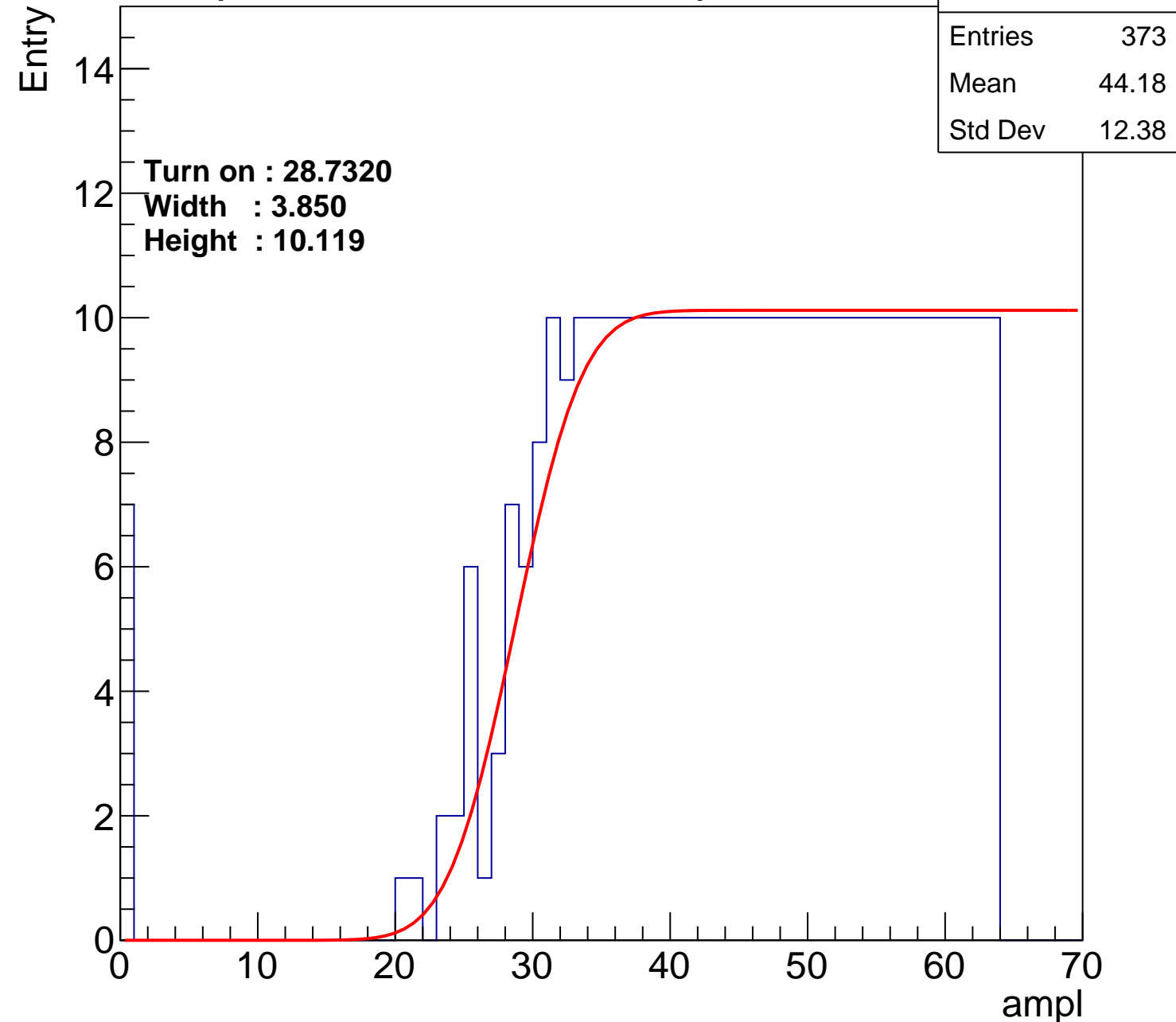
Width : 3.850

Height : 10.119

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U17-ch109

calib_packv5_042523_0143.root, FC#0, port D2

Entries	369
Mean	44.72
Std Dev	11.37

Turn on : 28.1823

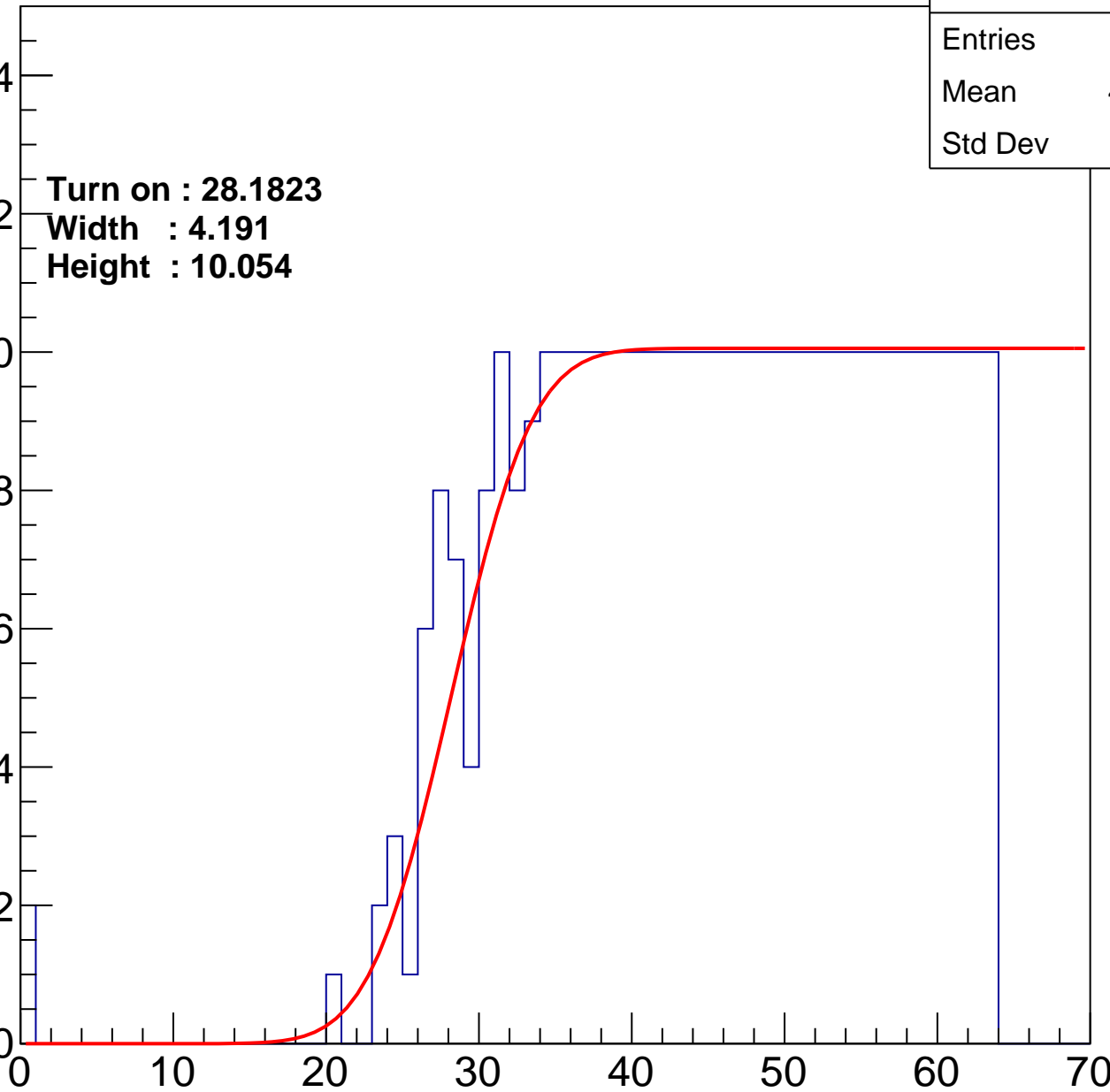
Width : 4.191

Height : 10.054

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U17-ch110

calib_packv5_042523_0143.root, FC#0, port D2

Entries	381
Mean	44.12
Std Dev	11.77

Turn on : 26.7298

Width : 2.878

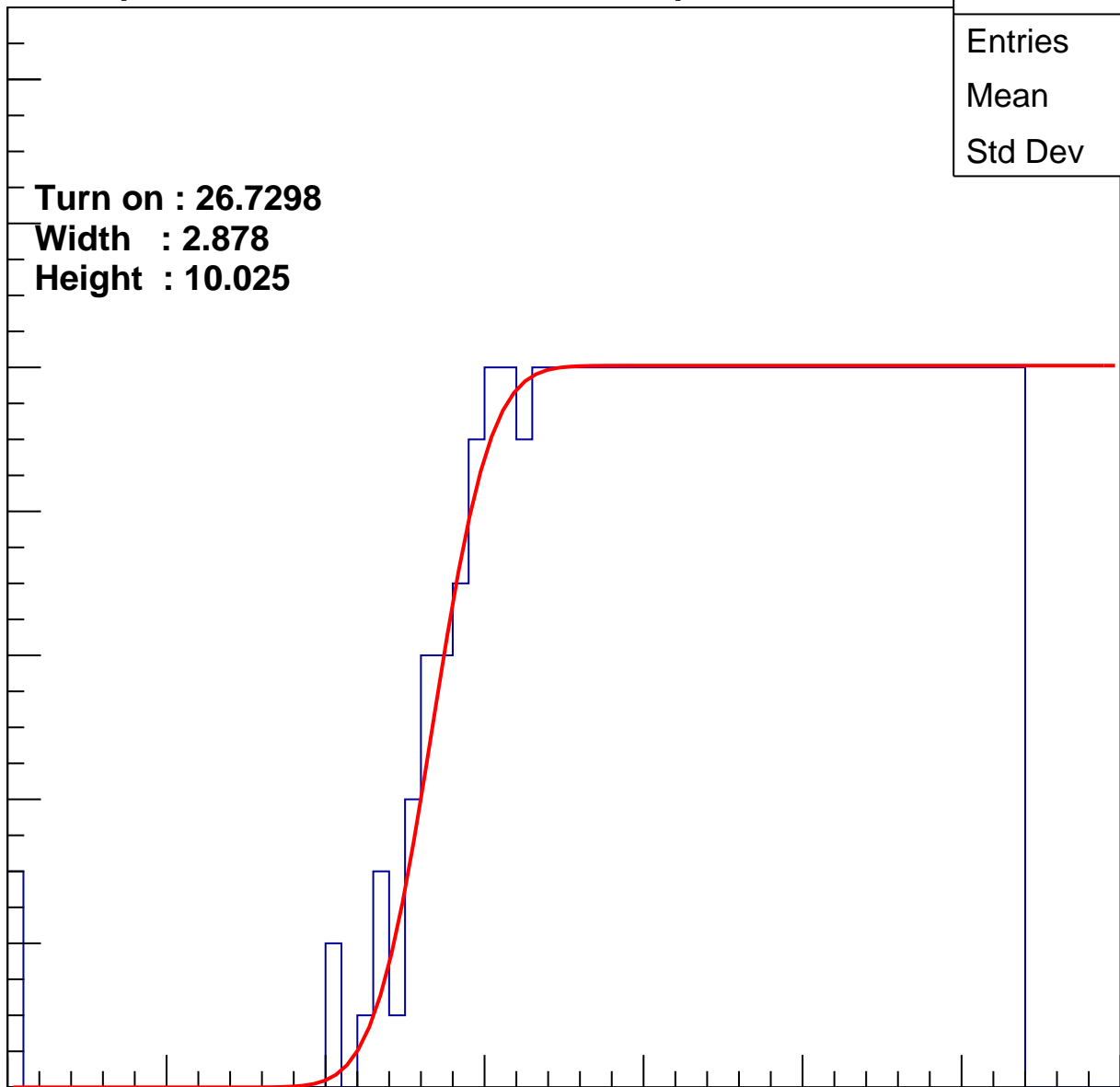
Height : 10.025

Entry

14
12
10
8
6
4
2
0

ampl

0 10 20 30 40 50 60 70



B1L101S, U17-ch111

calib_packv5_042523_0143.root, FC#0, port D2

Entries	369
Mean	44.73
Std Dev	11.43

Turn on : 27.2989

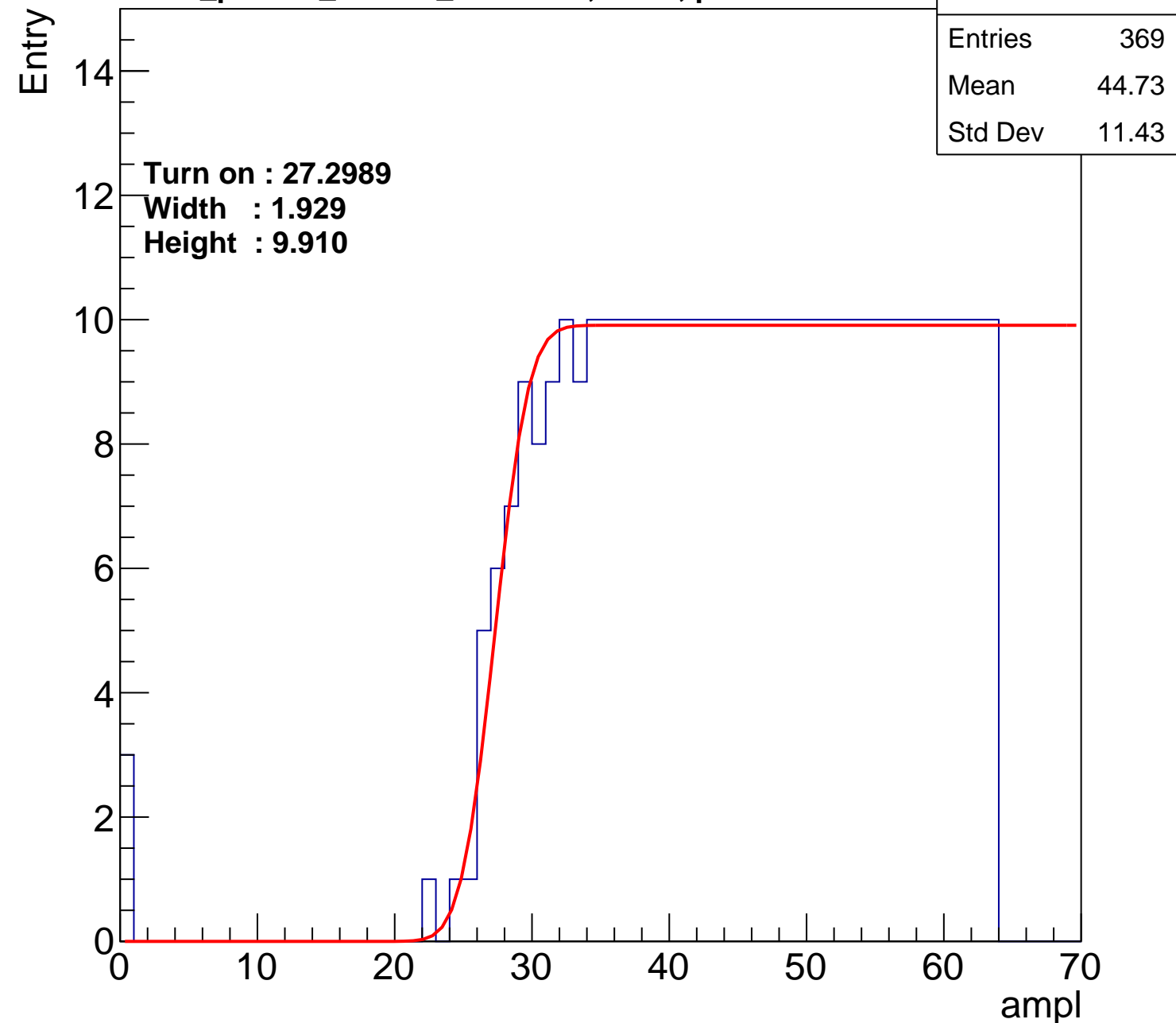
Width : 1.929

Height : 9.910

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U17-ch112

calib_packv5_042523_0143.root, FC#0, port D2

Entries	388
Mean	43.71
Std Dev	12.1

Turn on : 25.3210

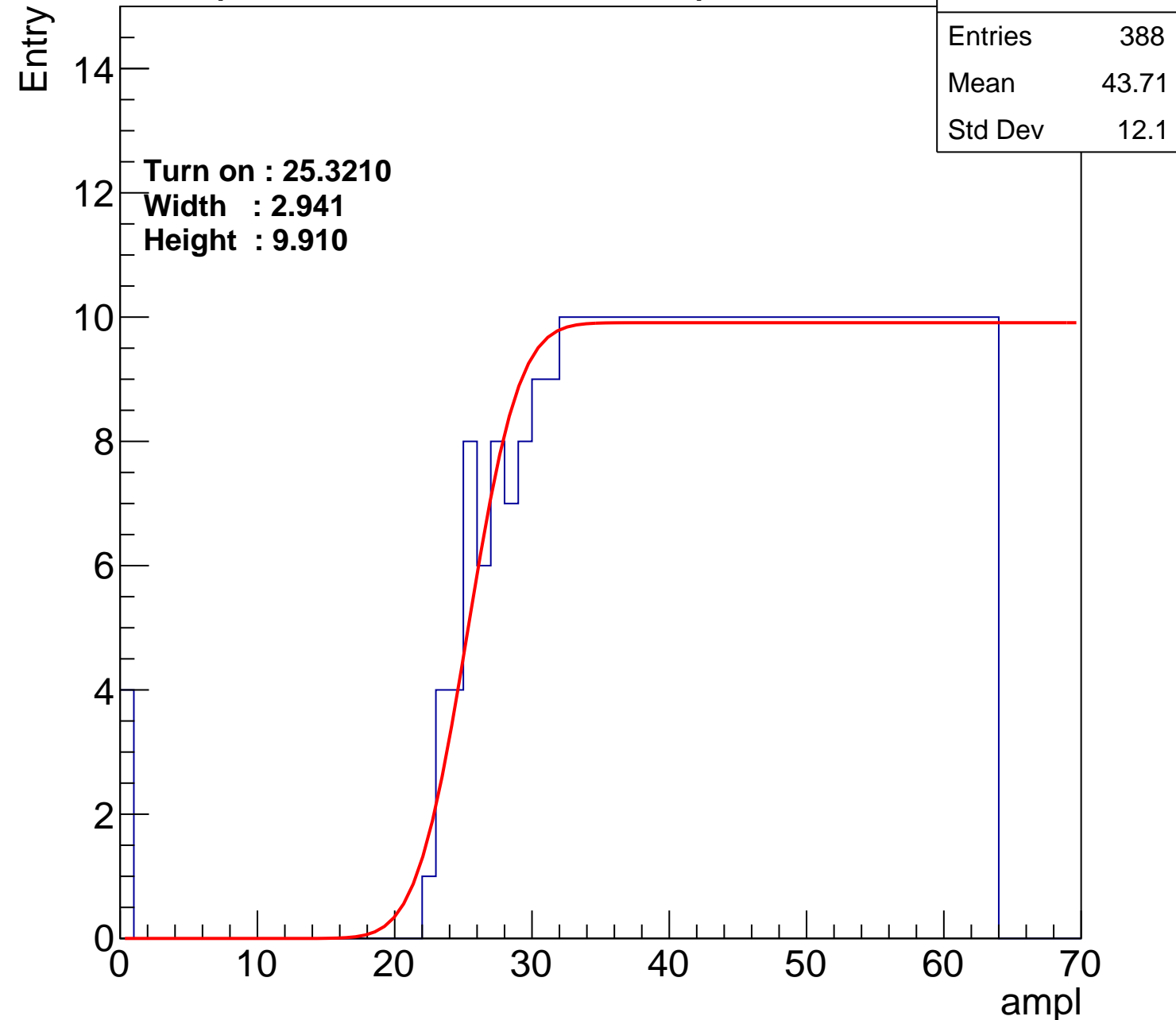
Width : 2.941

Height : 9.910

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U17-ch113

calib_packv5_042523_0143.root, FC#0, port D2

Entries	372
Mean	44.48
Std Dev	11.76

Turn on : 28.3153

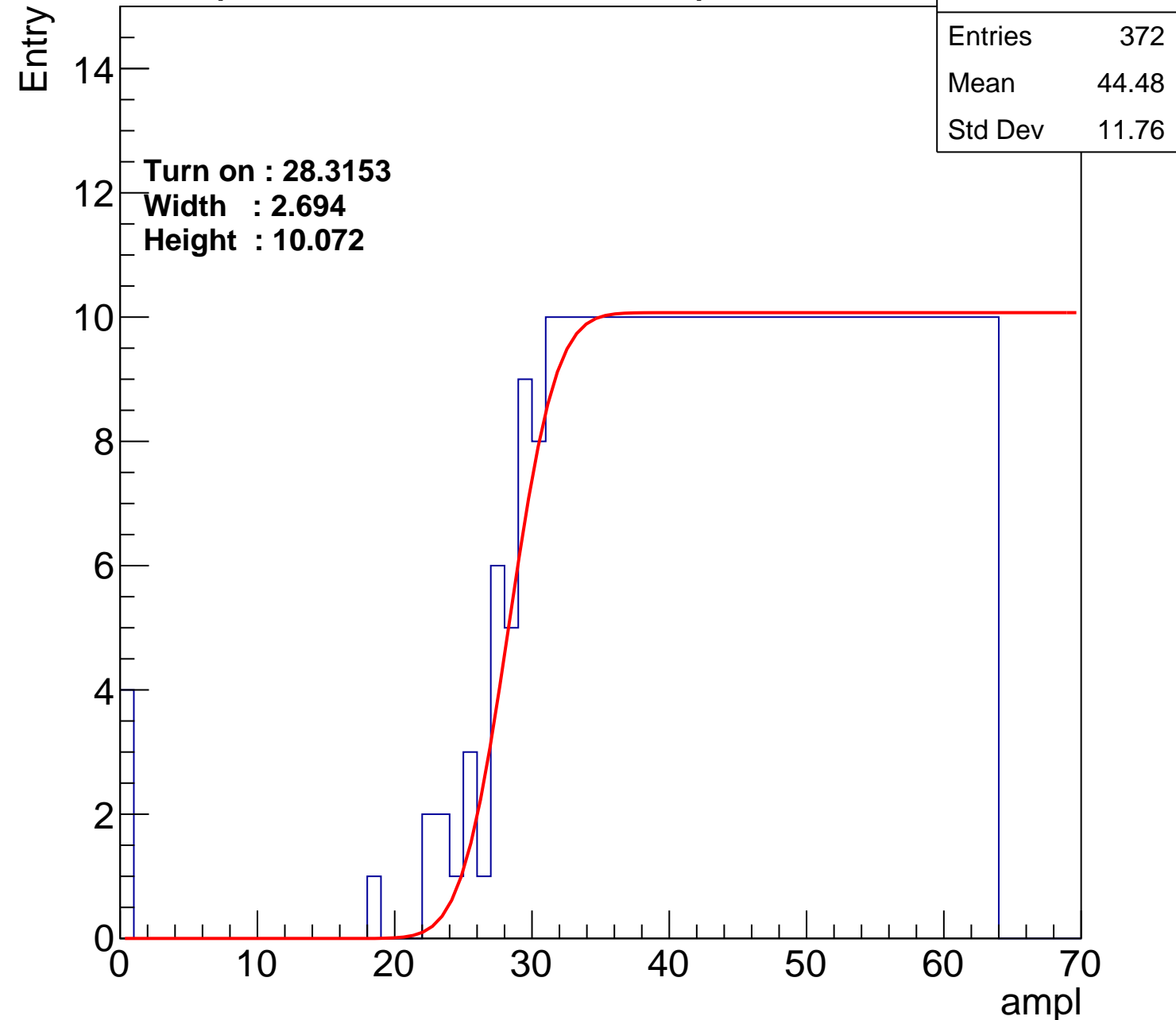
Width : 2.694

Height : 10.072

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U17-ch114

calib_packv5_042523_0143.root, FC#0, port D2

Entries	378
Mean	44.11
Std Dev	12.08

Turn on : 26.3568

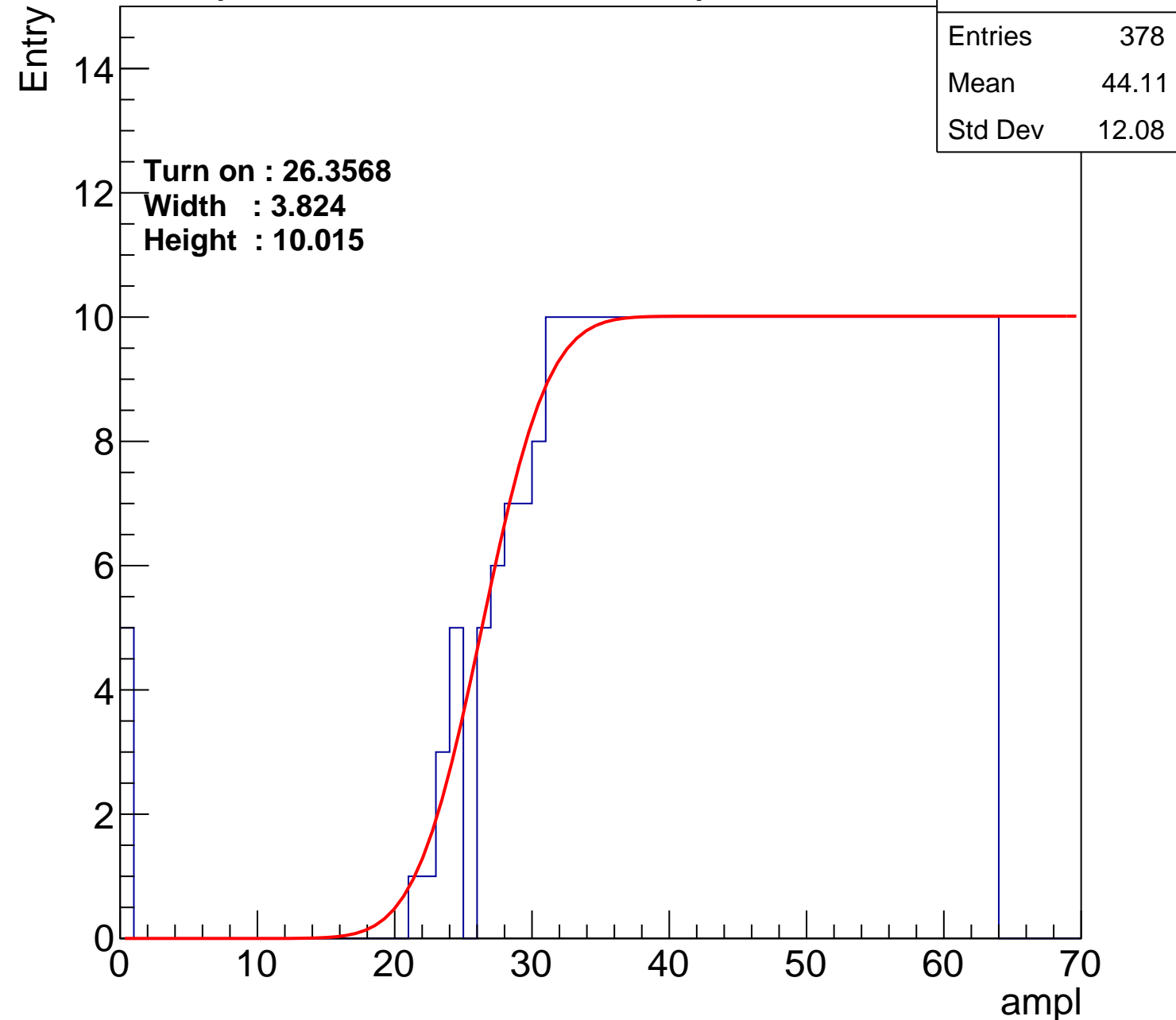
Width : 3.824

Height : 10.015

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U17-ch115

calib_packv5_042523_0143.root, FC#0, port D2

Entries	374
Mean	44.51
Std Dev	11.44

Turn on : 26.9372

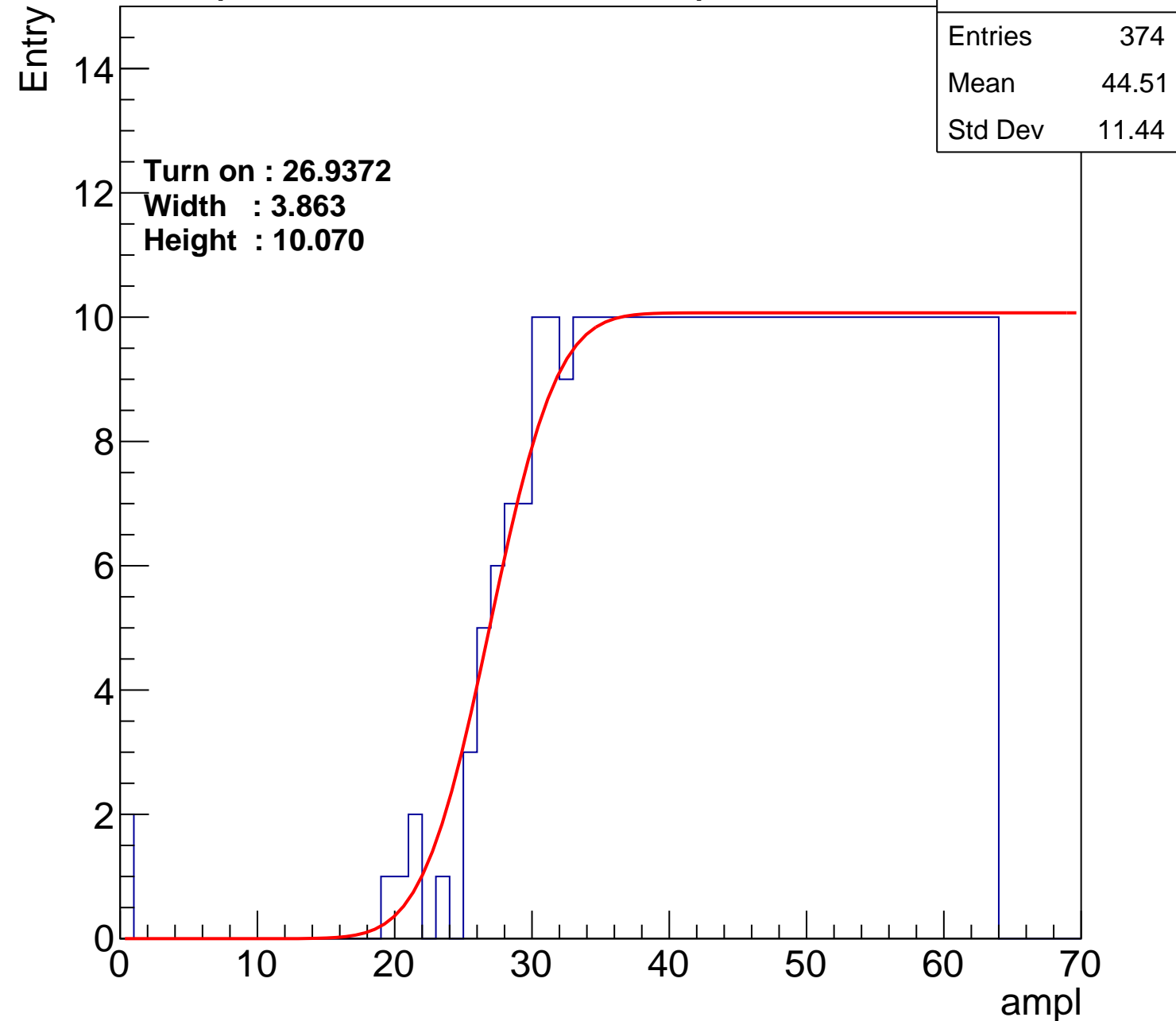
Width : 3.863

Height : 10.070

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U17-ch116

calib_packv5_042523_0143.root, FC#0, port D2

Entries	390
Mean	43.69
Std Dev	11.97

Turn on : 25.5095

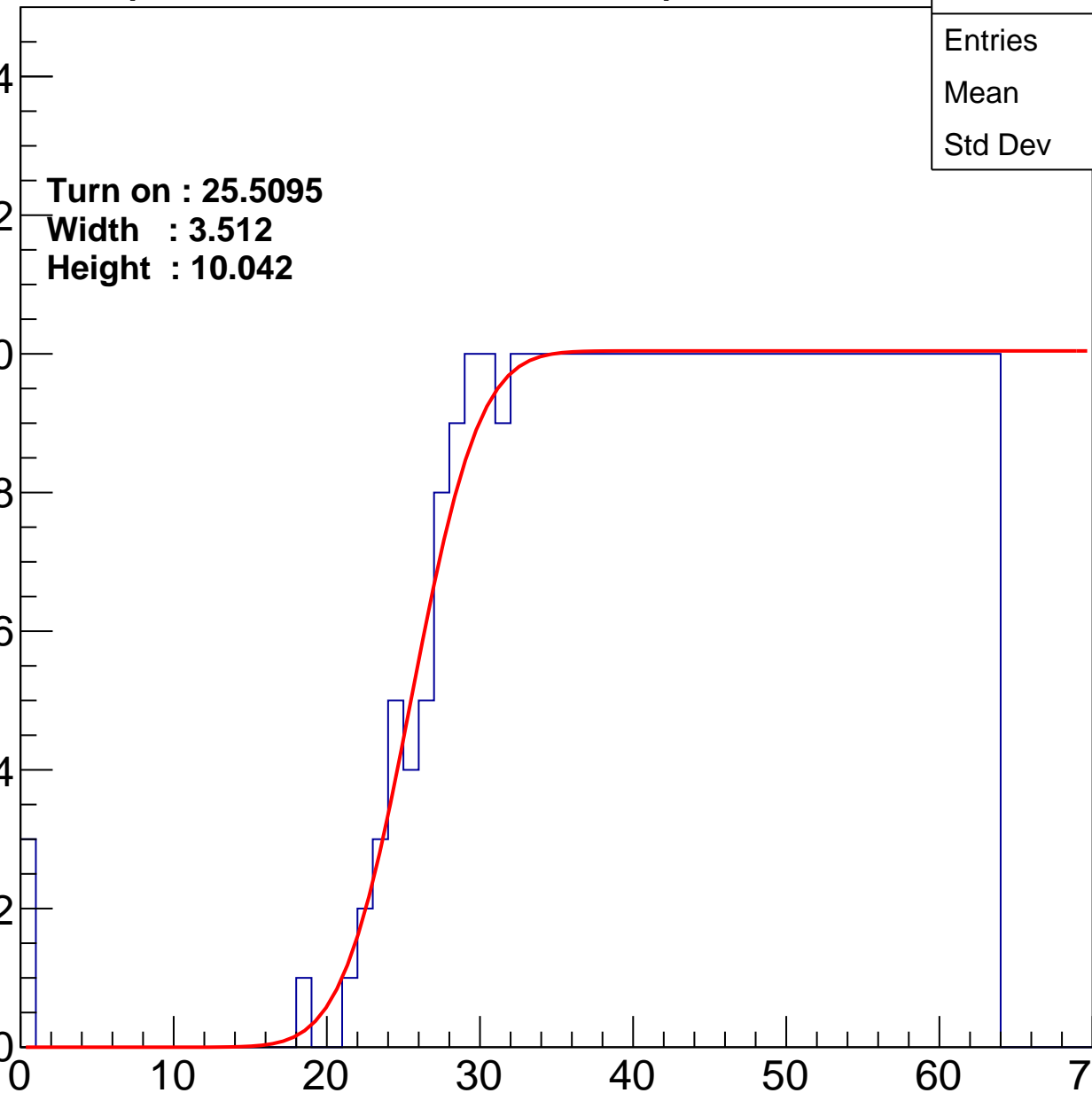
Width : 3.512

Height : 10.042

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U17-ch117

calib_packv5_042523_0143.root, FC#0, port D2

Entries	370
Mean	44.51
Std Dev	11.88

Turn on : 27.4125

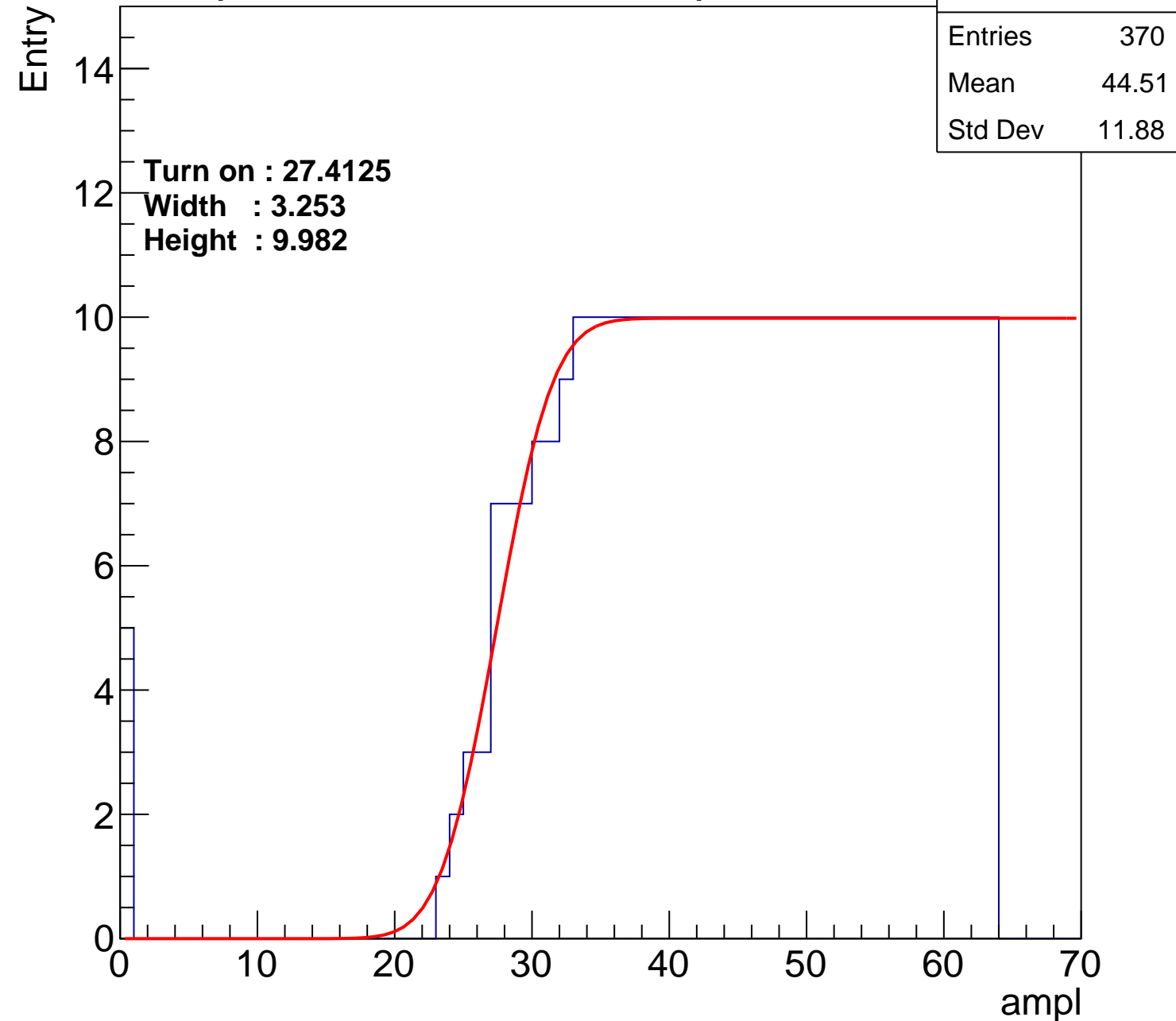
Width : 3.253

Height : 9.982

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U17-ch118

calib_packv5_042523_0143.root, FC#0, port D2

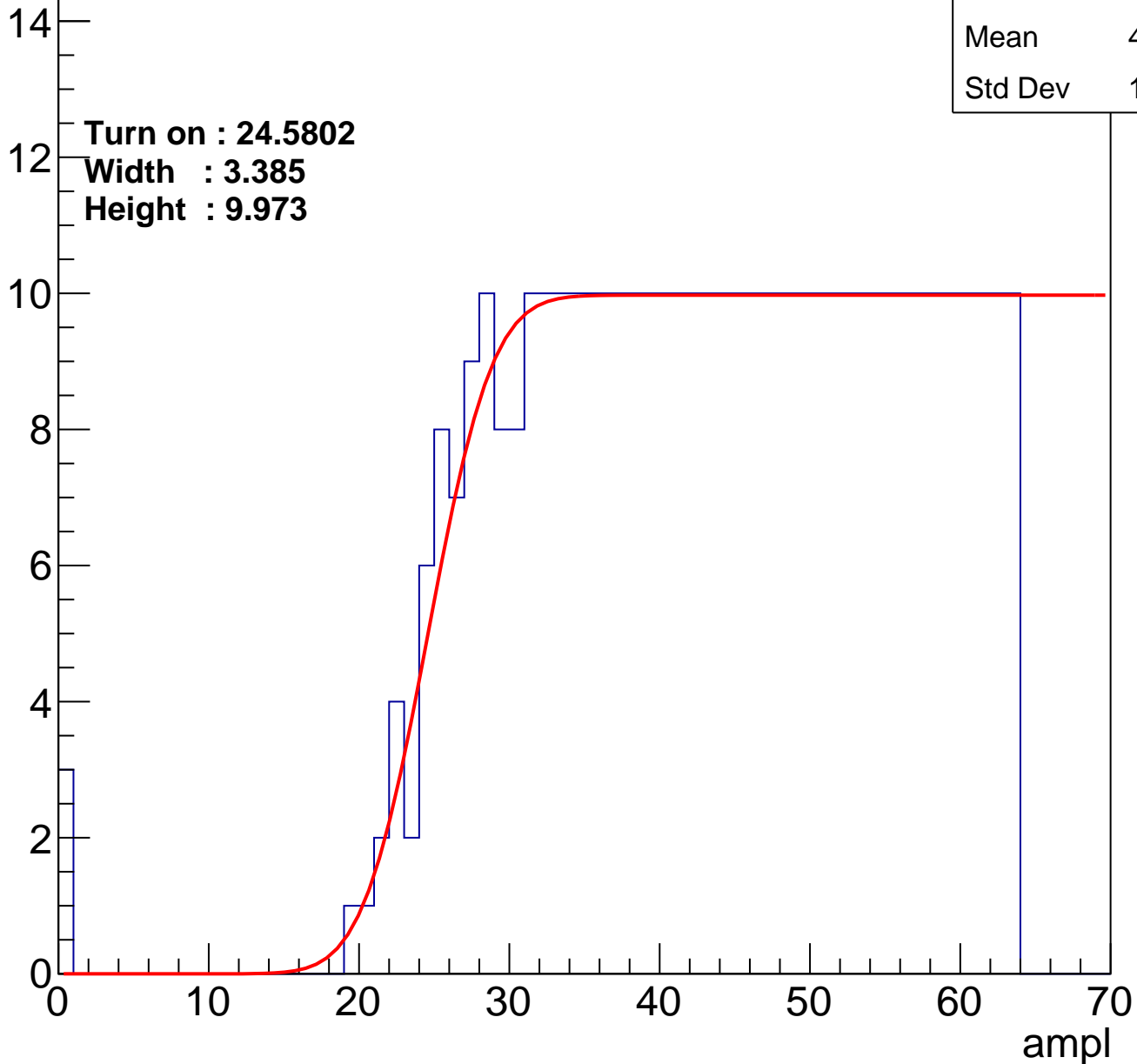
Entries	399
Mean	43.22
Std Dev	12.22

Turn on : 24.5802

Width : 3.385

Height : 9.973

Entry



B1L101S, U17-ch119

calib_packv5_042523_0143.root, FC#0, port D2

Entries	365
Mean	44.74
Std Dev	11.71

Turn on : 29.4429

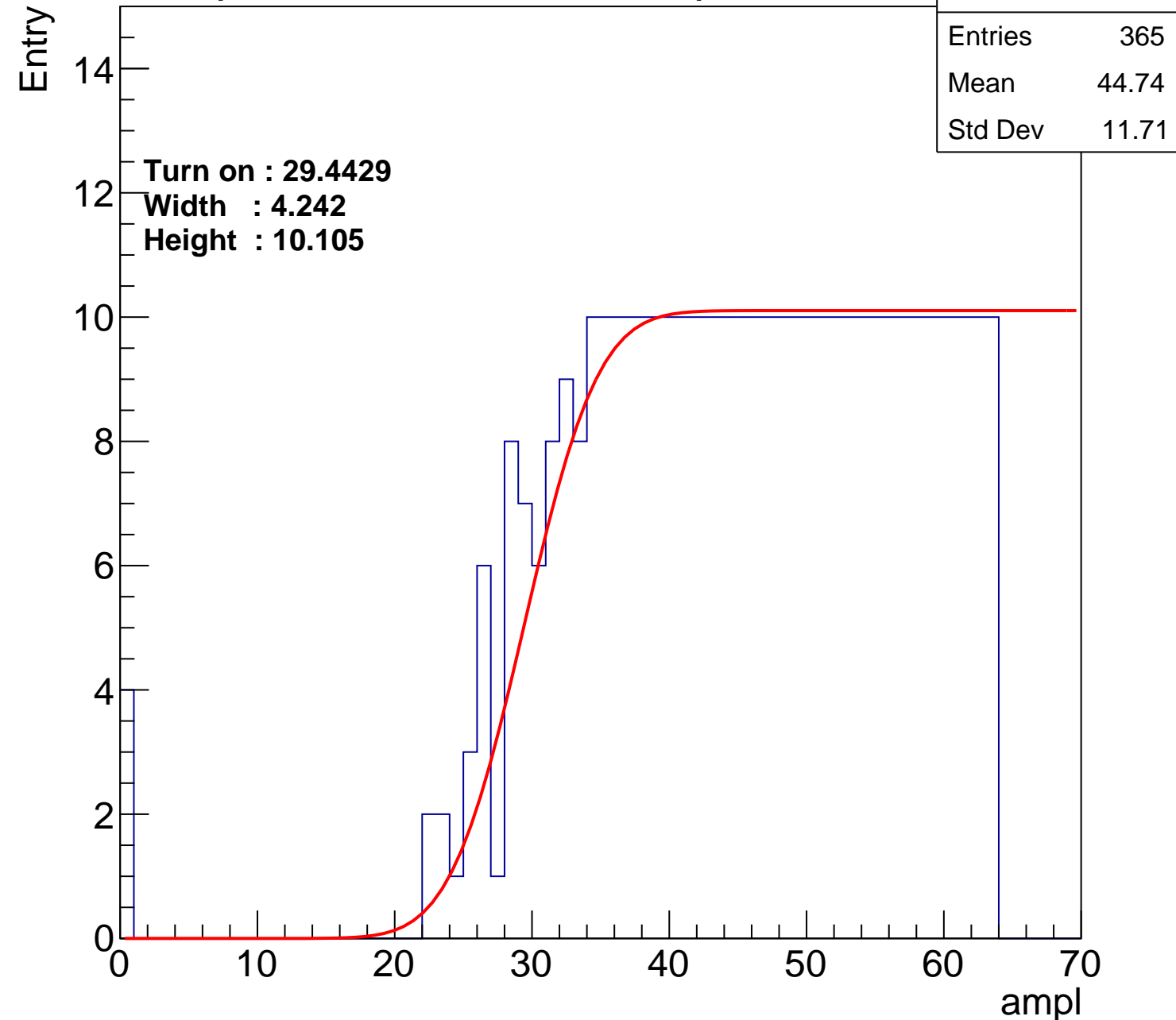
Width : 4.242

Height : 10.105

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U17-ch120

calib_packv5_042523_0143.root, FC#0, port D2

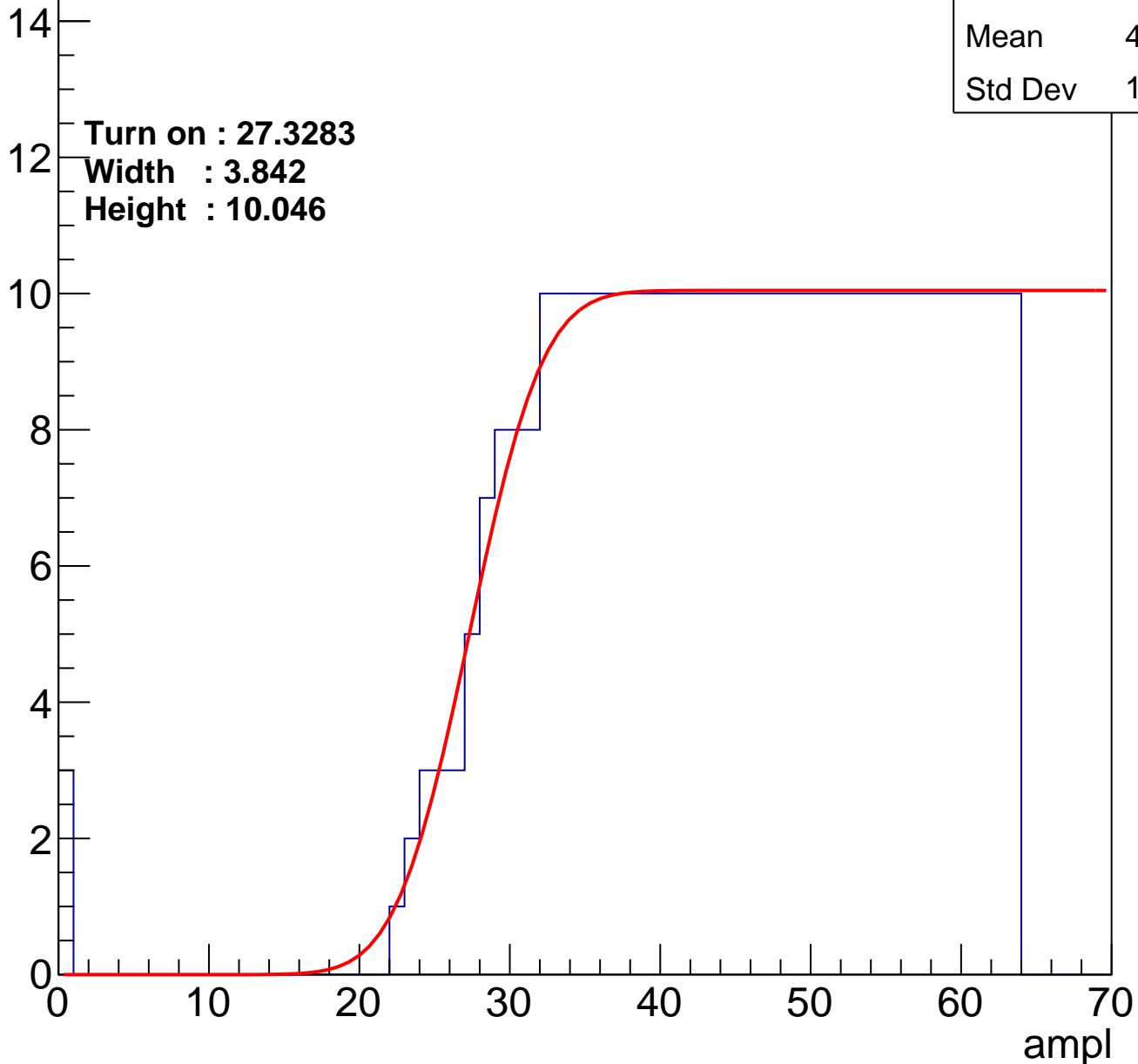
Entries	371
Mean	44.59
Std Dev	11.55

Turn on : 27.3283

Width : 3.842

Height : 10.046

Entry



B1L101S, U17-ch121

calib_packv5_042523_0143.root, FC#0, port D2

Entries	387
Mean	43.59
Std Dev	12.53

Turn on : 25.9427

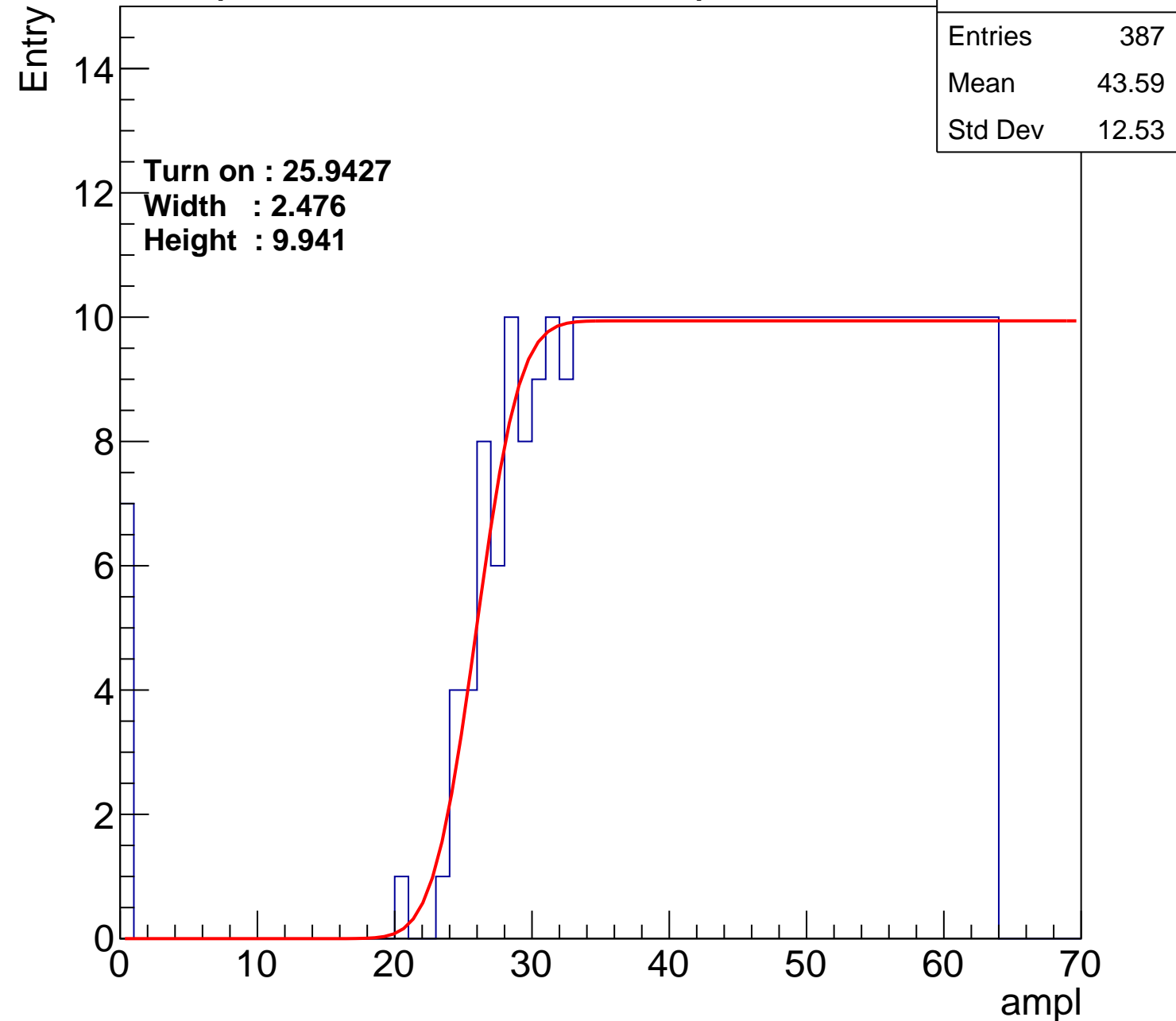
Width : 2.476

Height : 9.941

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U17-ch122

calib_packv5_042523_0143.root, FC#0, port D2

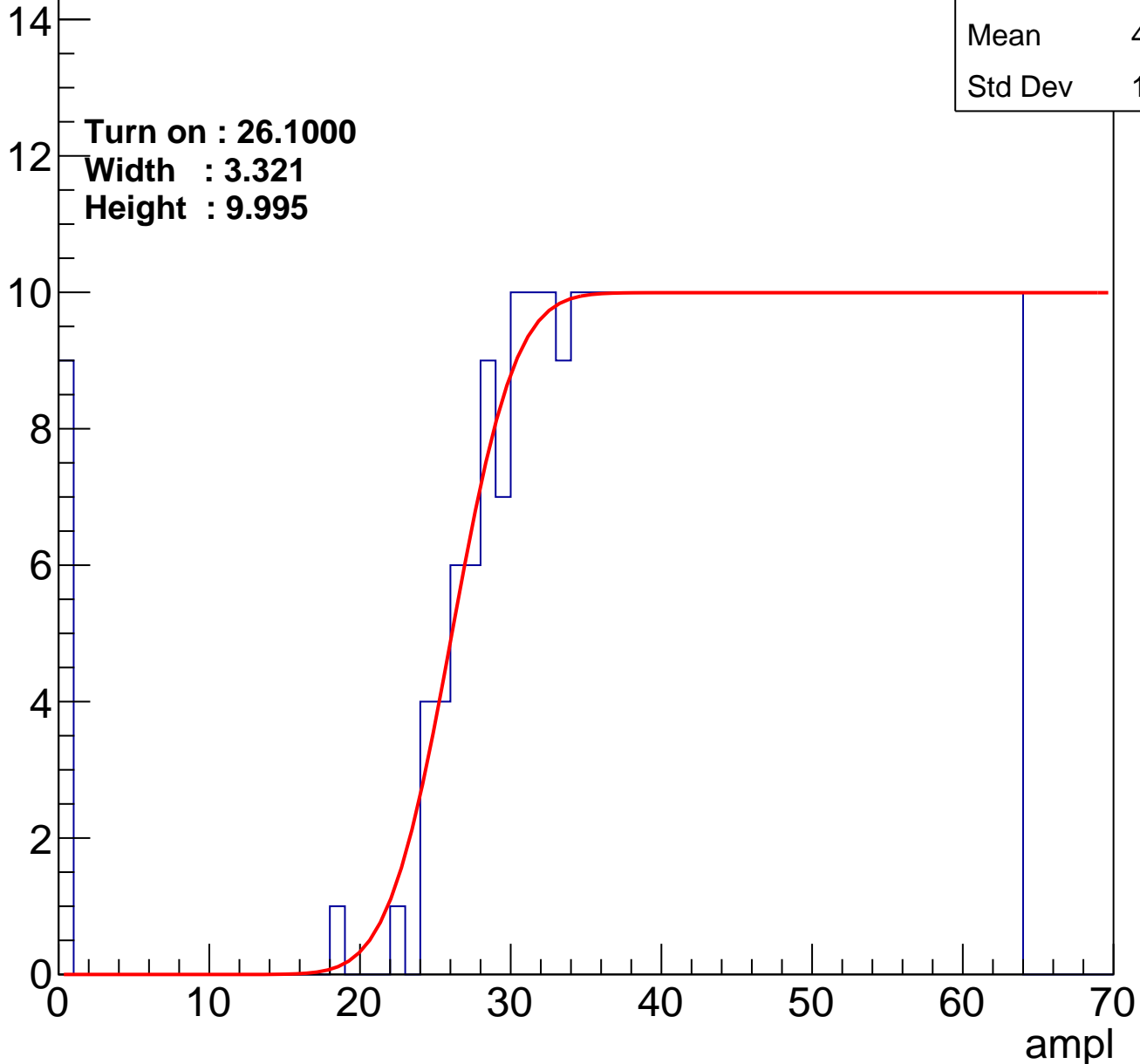
Entries	386
Mean	43.49
Std Dev	12.86

Turn on : 26.1000

Width : 3.321

Height : 9.995

Entry



B1L101S, U17-ch123

calib_packv5_042523_0143.root, FC#0, port D2

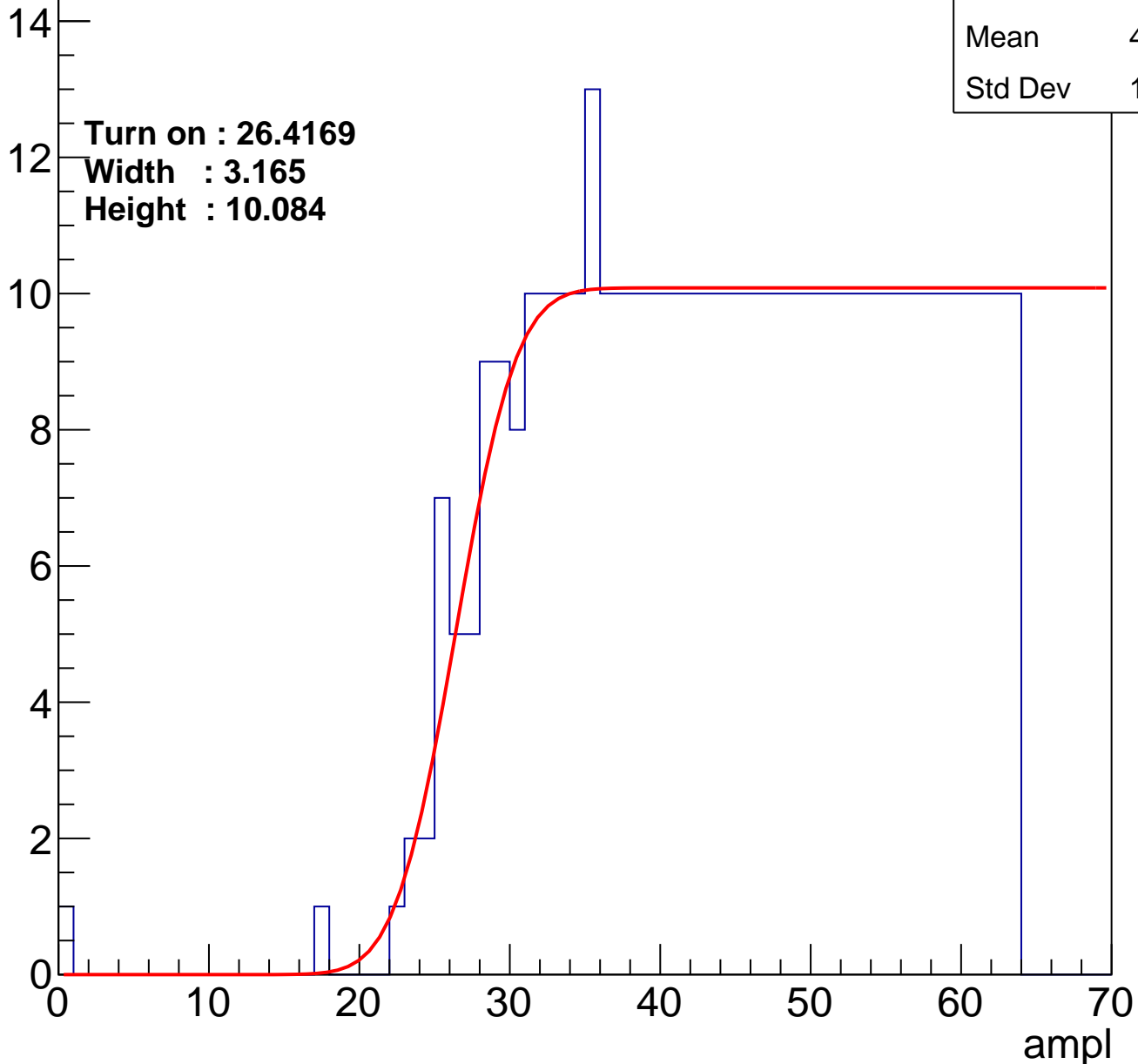
Entries	383
Mean	44.23
Std Dev	11.36

Turn on : 26.4169

Width : 3.165

Height : 10.084

Entry



B1L101S, U17-ch124

calib_packv5_042523_0143.root, FC#0, port D2

Entries	376
Mean	44.29
Std Dev	11.83

Turn on : 27.2920

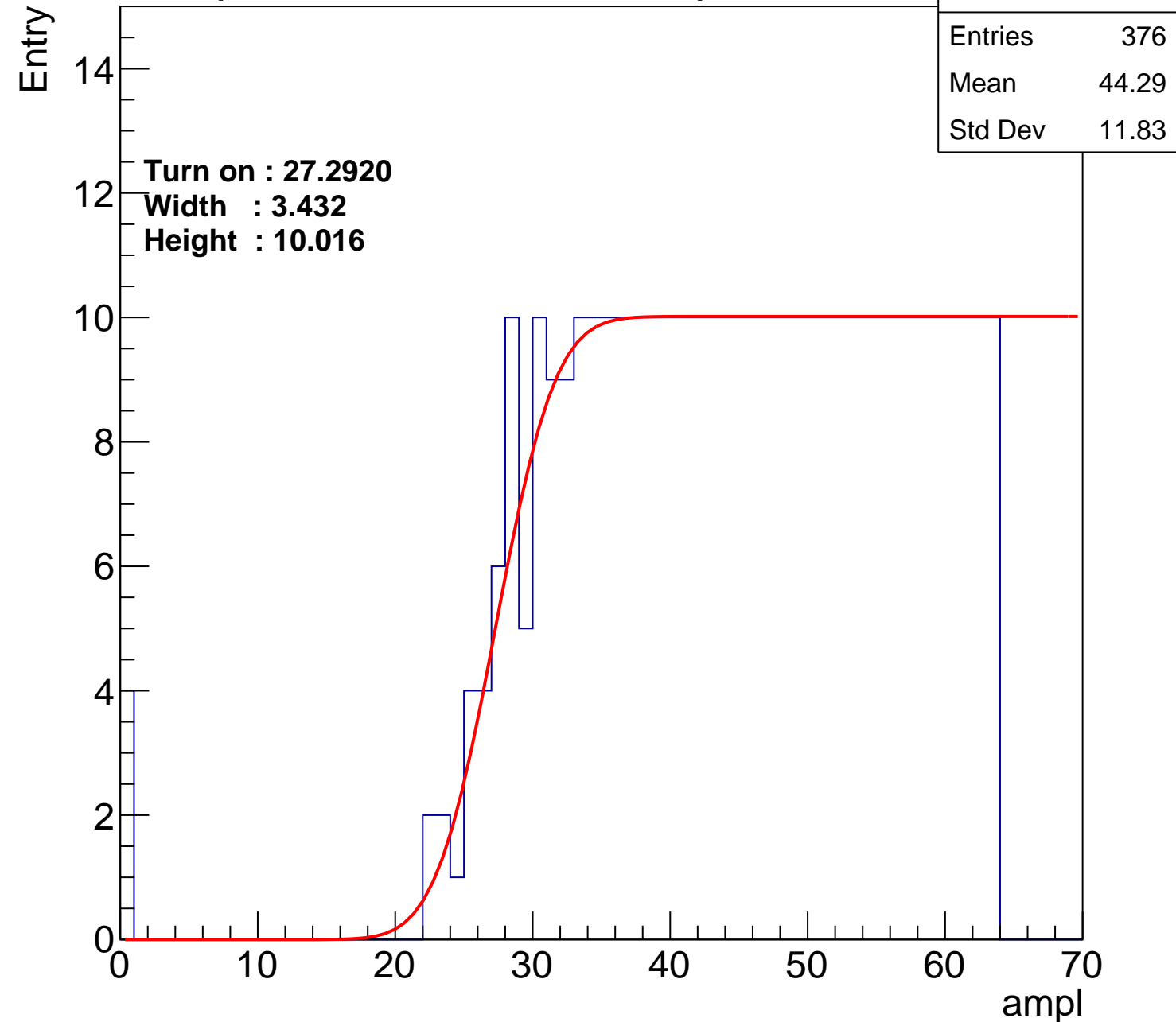
Width : 3.432

Height : 10.016

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U17-ch125

calib_packv5_042523_0143.root, FC#0, port D2

Entries	374
Mean	44.55
Std Dev	11.38

Turn on : 26.8397

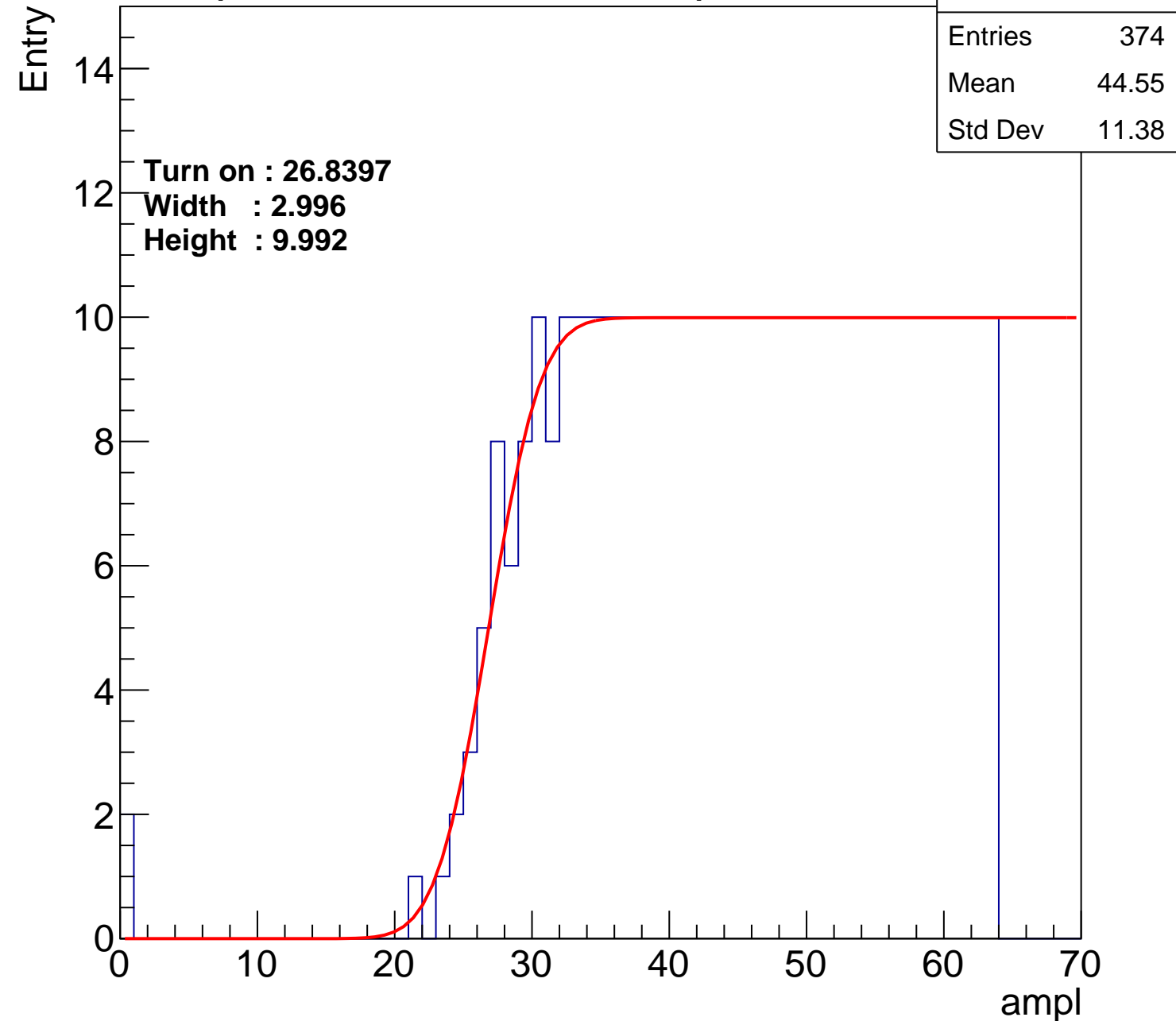
Width : 2.996

Height : 9.992

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U17-ch126

calib_packv5_042523_0143.root, FC#0, port D2

Entries	383
Mean	44.05
Std Dev	11.99

Turn on : 27.1017

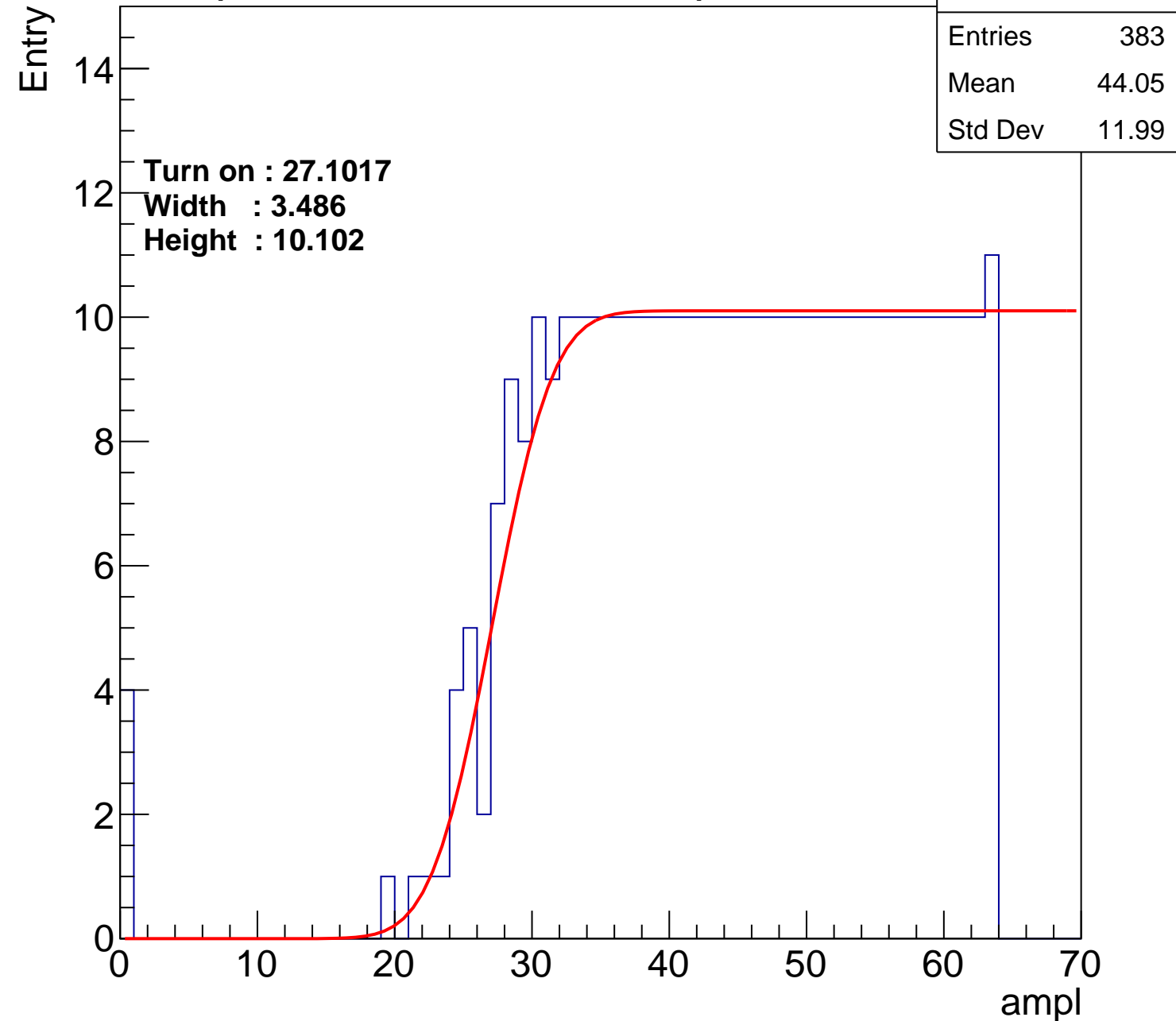
Width : 3.486

Height : 10.102

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U17-ch127

calib_packv5_042523_0143.root, FC#0, port D2

Entries	384
Mean	44.01
Std Dev	11.71

Turn on : 26.0850

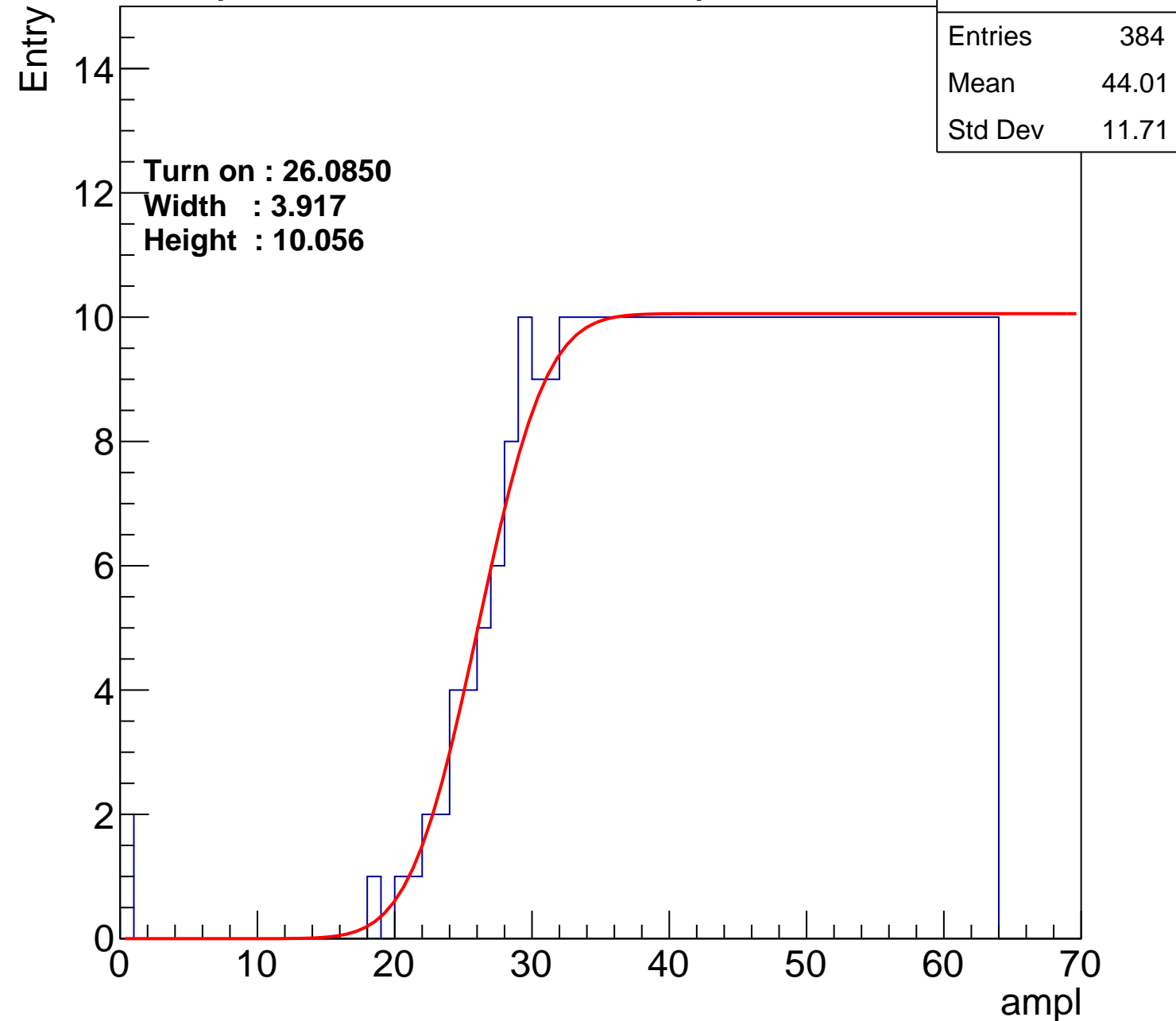
Width : 3.917

Height : 10.056

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U17-ch127

calib_packv5_042523_0143.root, FC#0, port D2

Entries	384
Mean	44.01
Std Dev	11.71

Turn on : 26.0850

Width : 3.917

Height : 10.056

Entry

14
12
10
8
6
4
2
0

ampl

