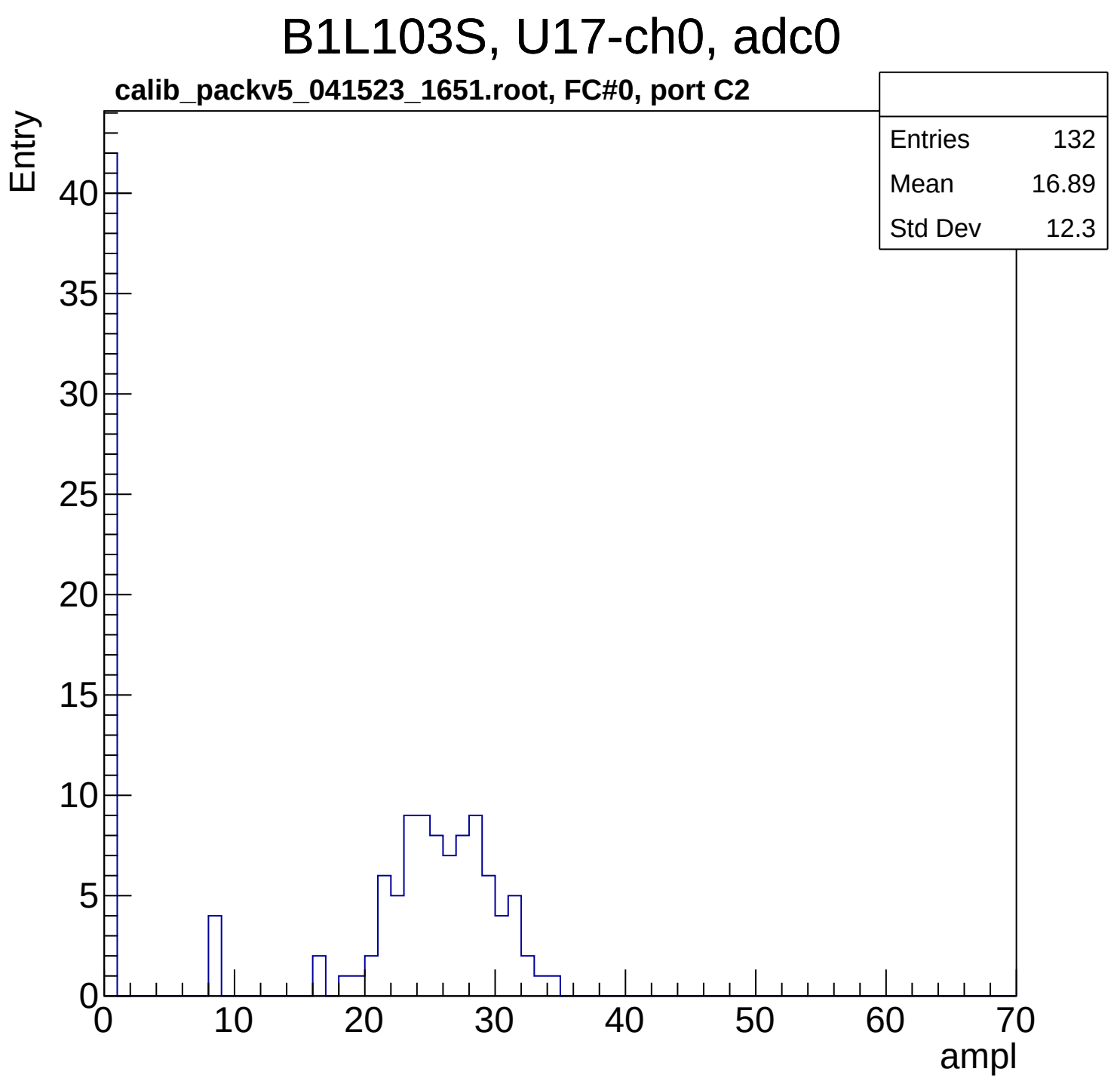
B1L103S, U17-ch0, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 132
Mean 16.89
Std Dev 12.3
Entry
0
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10
15
20
25
30
35
40
0
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20
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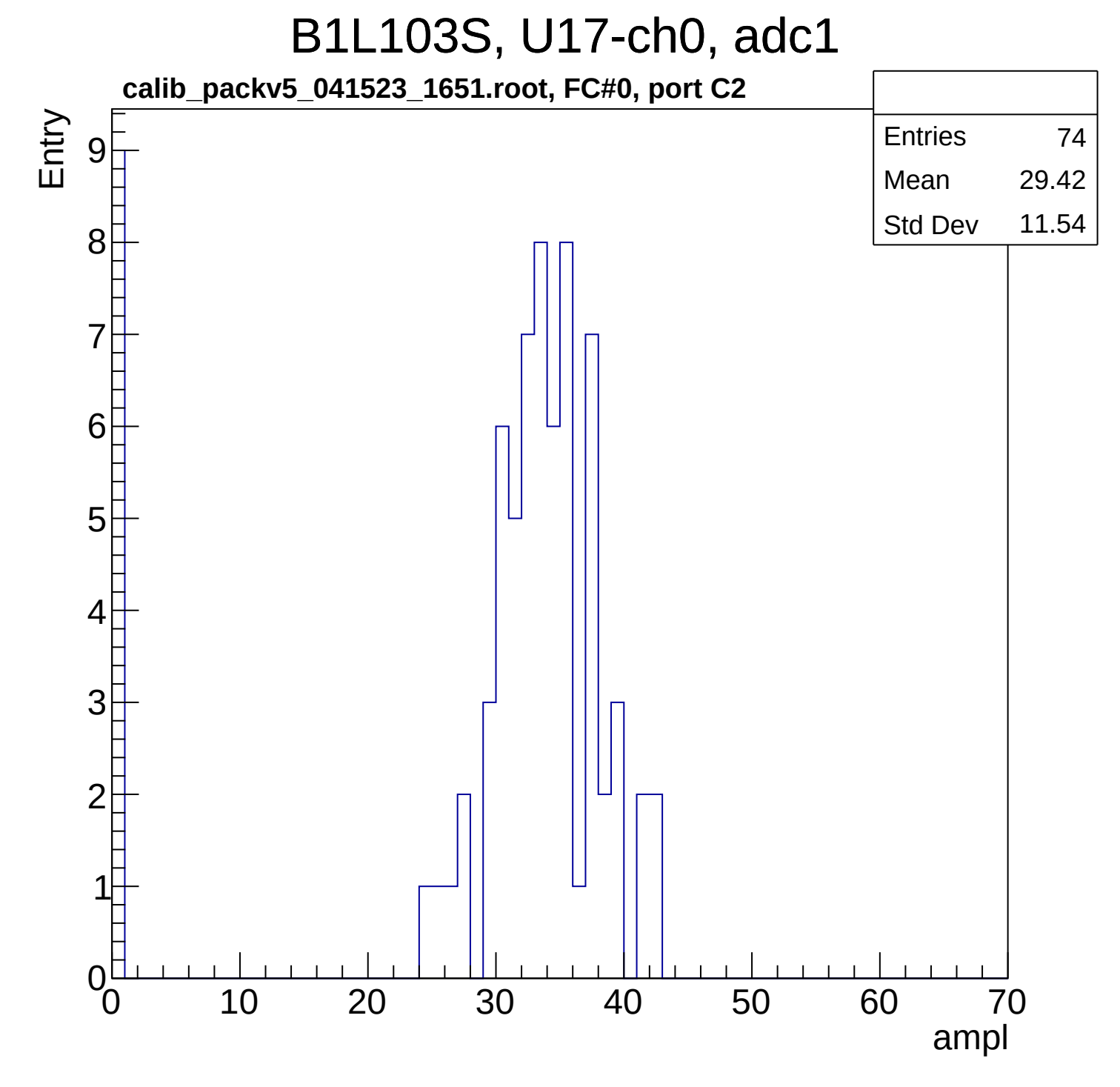
50
60
70
ampl


B1L103S, U17-ch0, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 29.42
Std Dev 11.54
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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40
50
60
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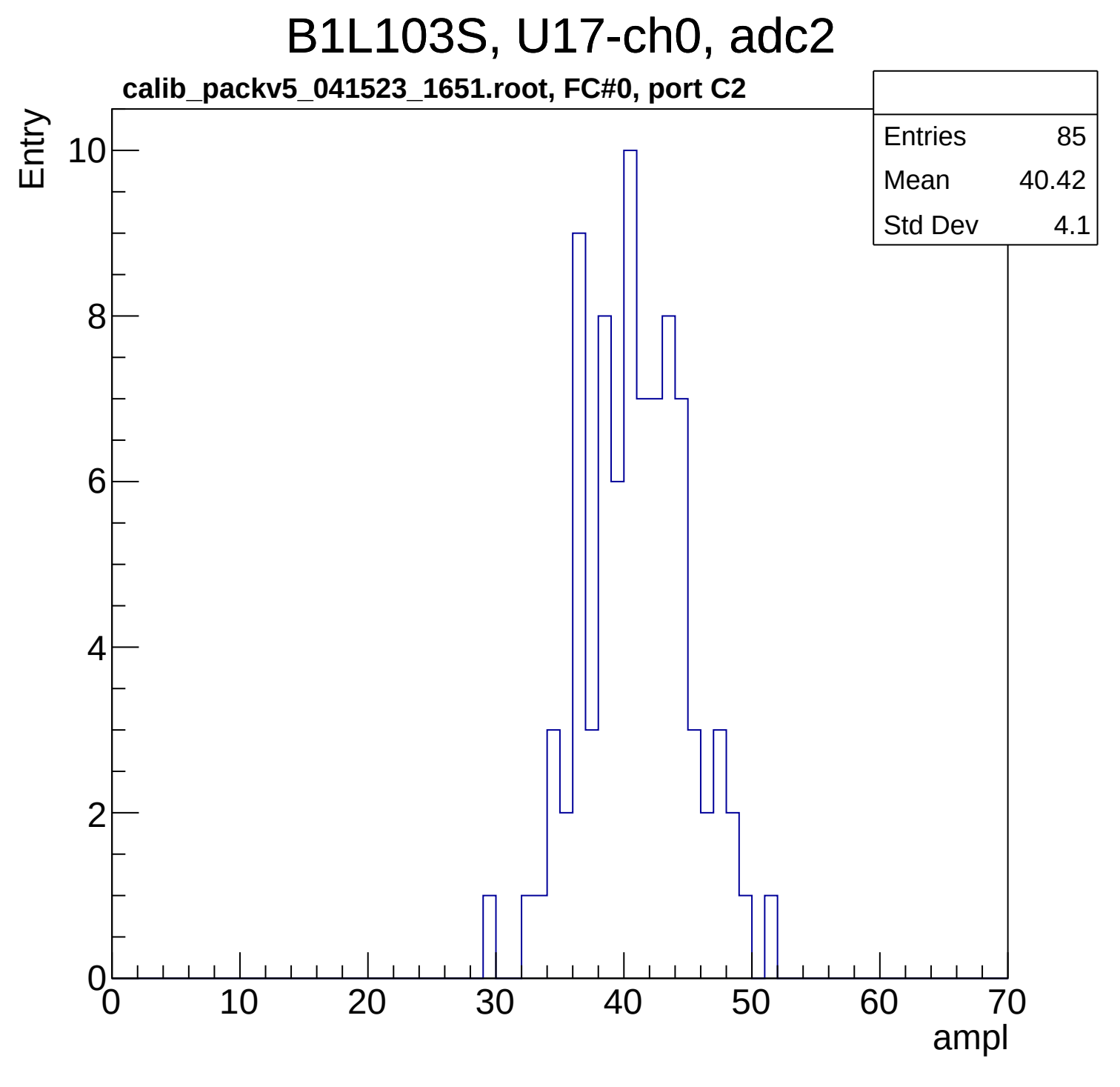
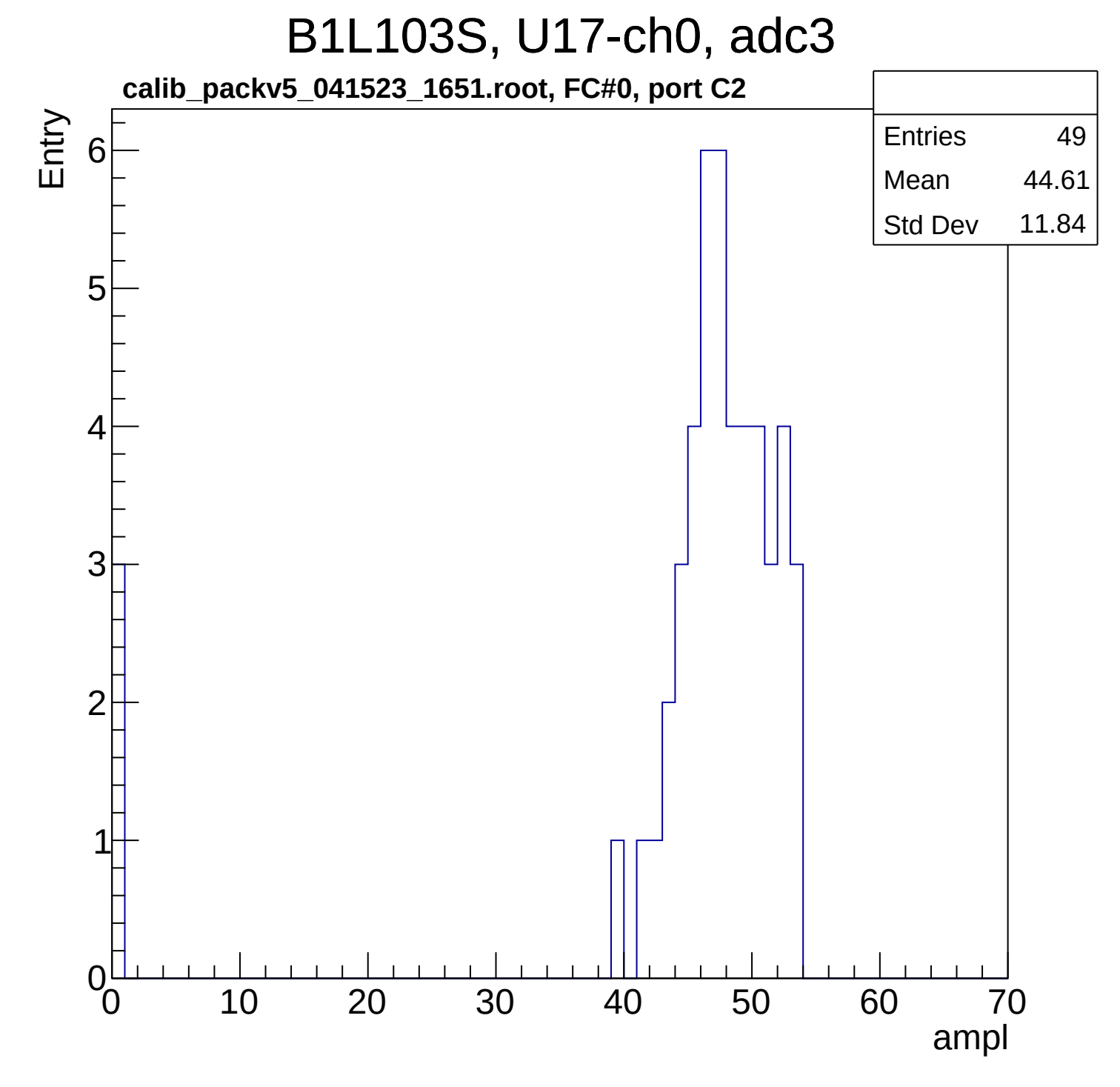
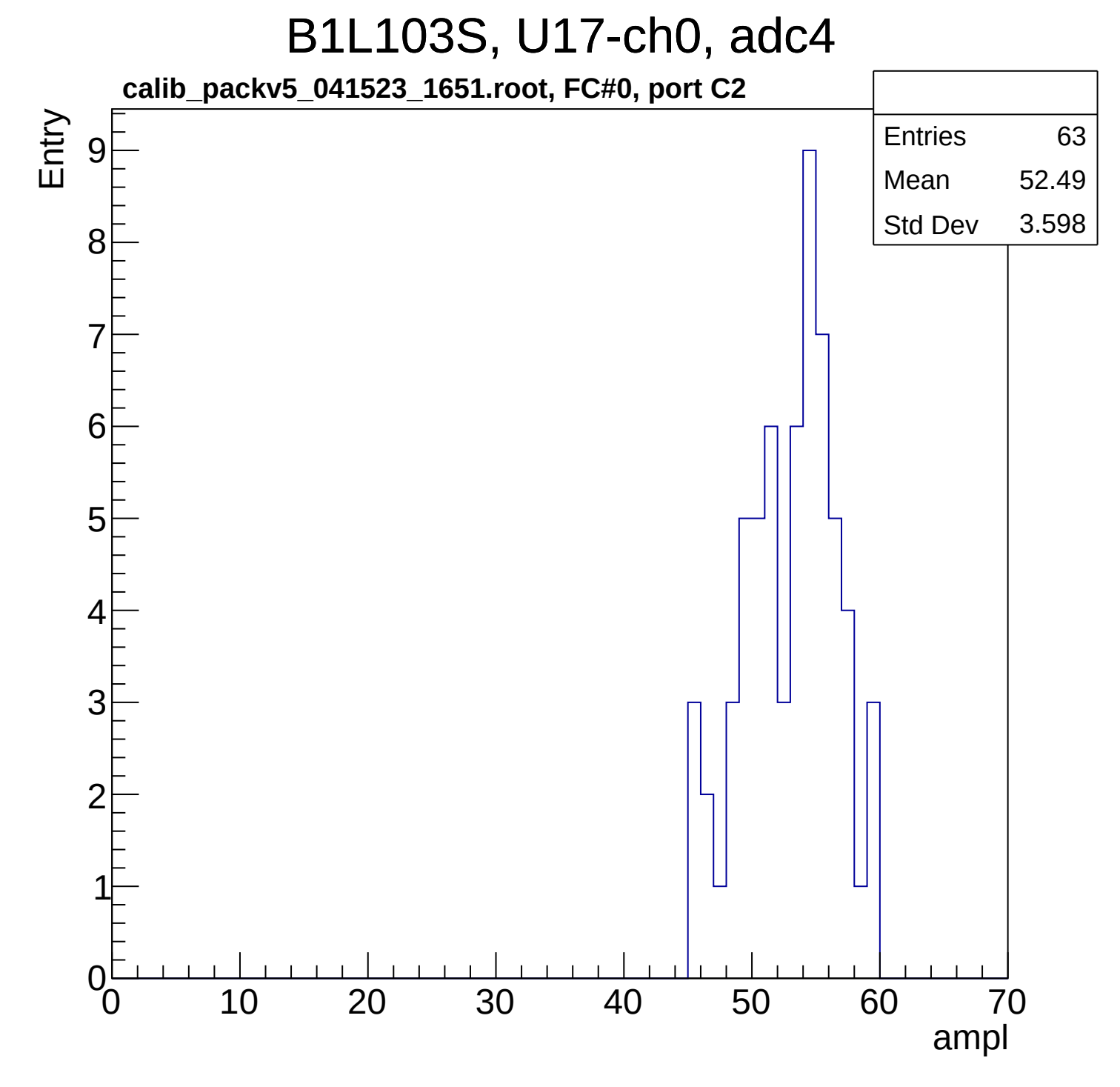

B1L103S, U17-ch0, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 40.42
Std Dev 4.1
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U17-ch0, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 44.61
Std Dev 11.84
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U17-ch0, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 52.49
Std Dev 3.598
Entry
ampl
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2
3
4
5
6
7
8
9
0
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30
40
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60
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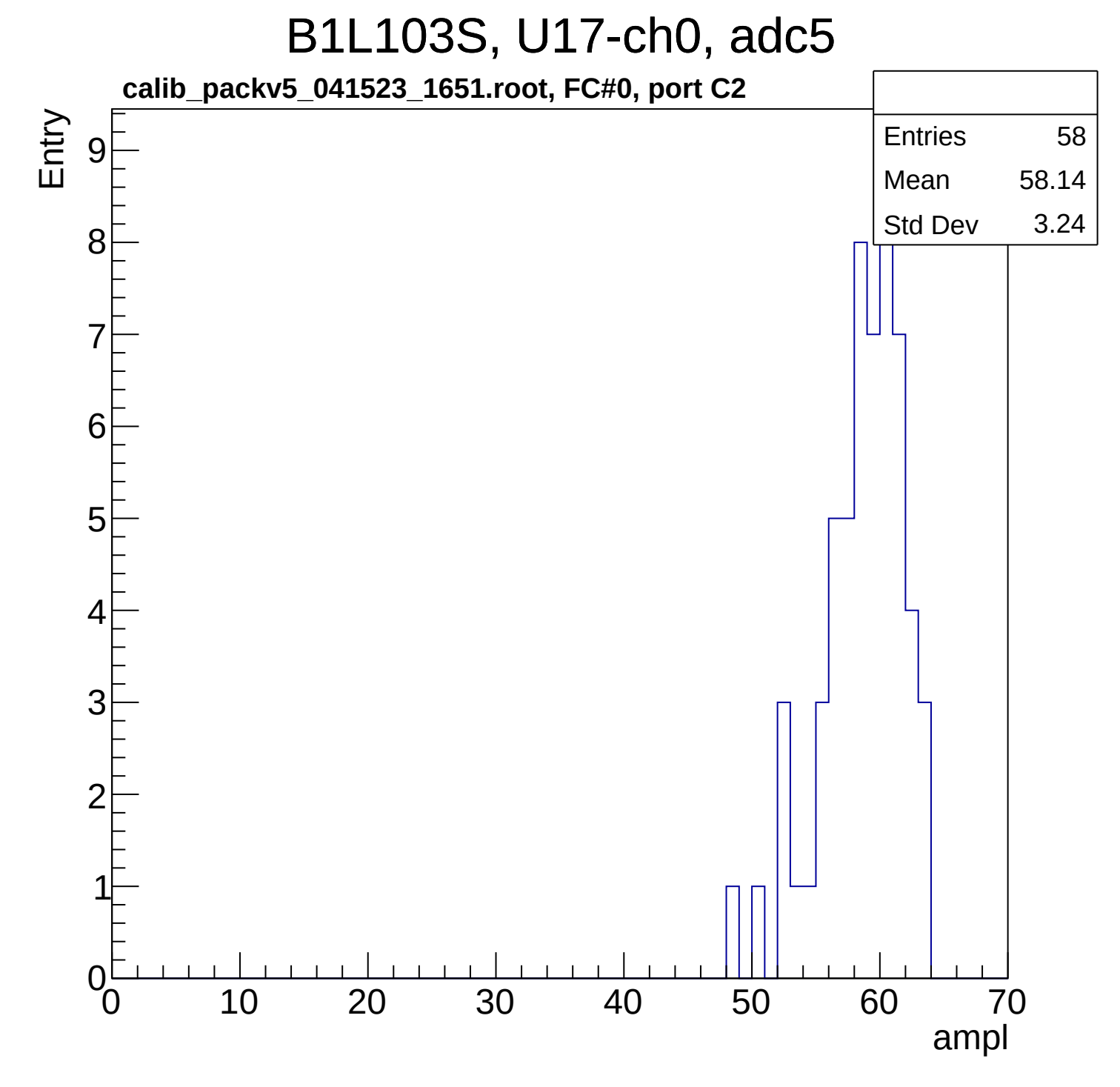
B1L103S, U17-ch0, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 58.14
Std Dev 3.24
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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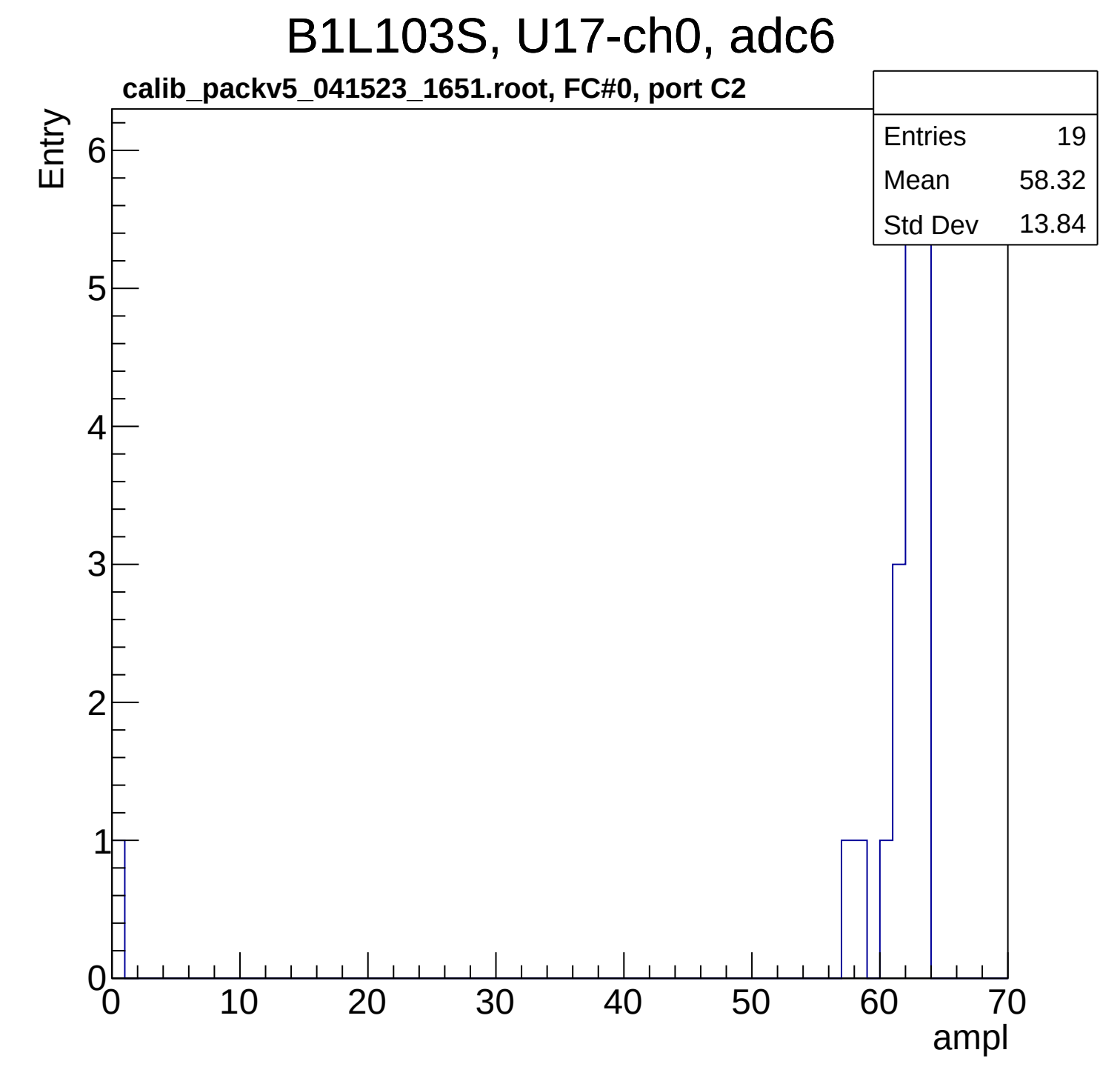
B1L103S, U17-ch0, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 58.32
Std Dev 13.84
Entry
ampl
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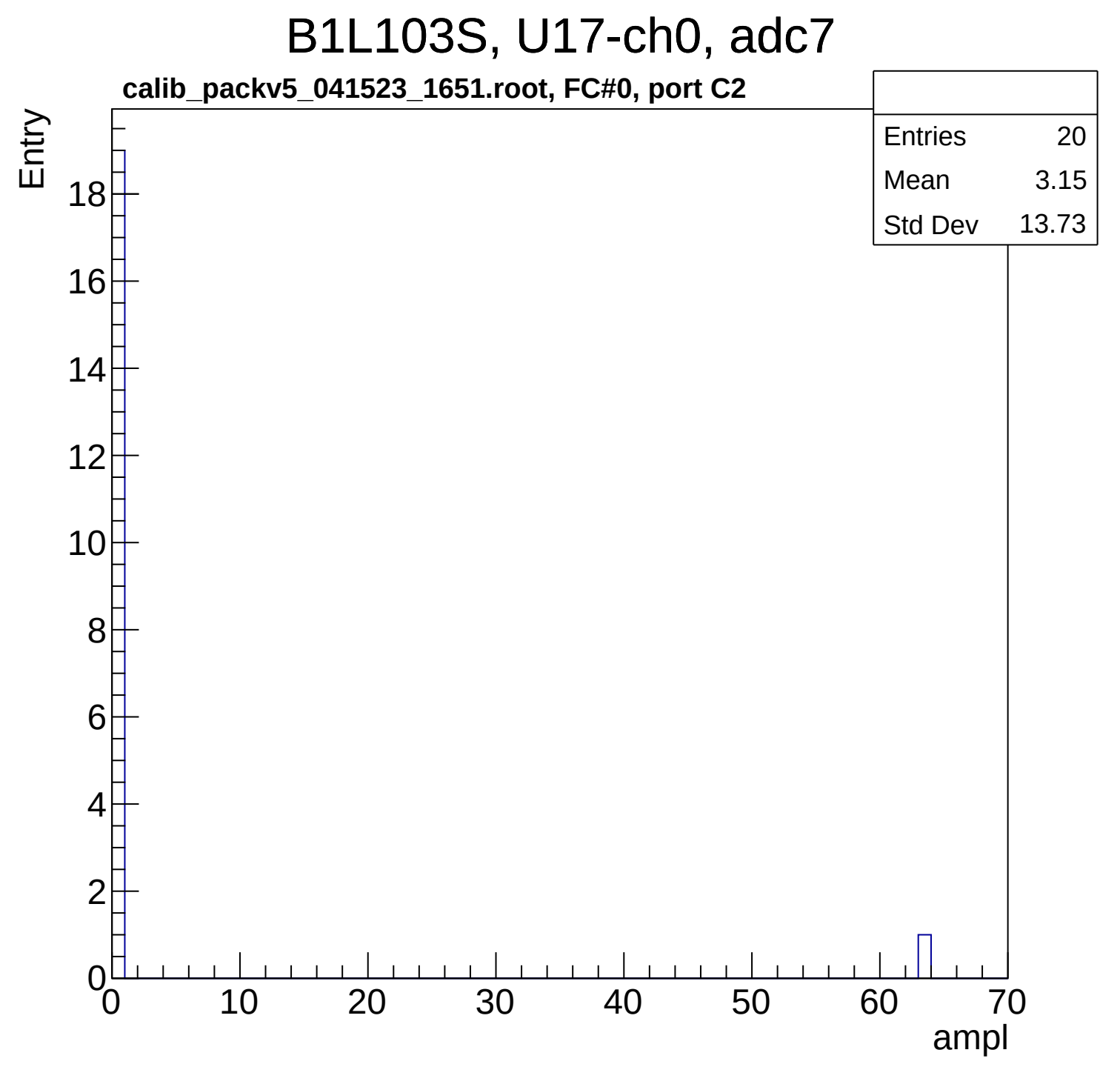
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U17-ch0, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
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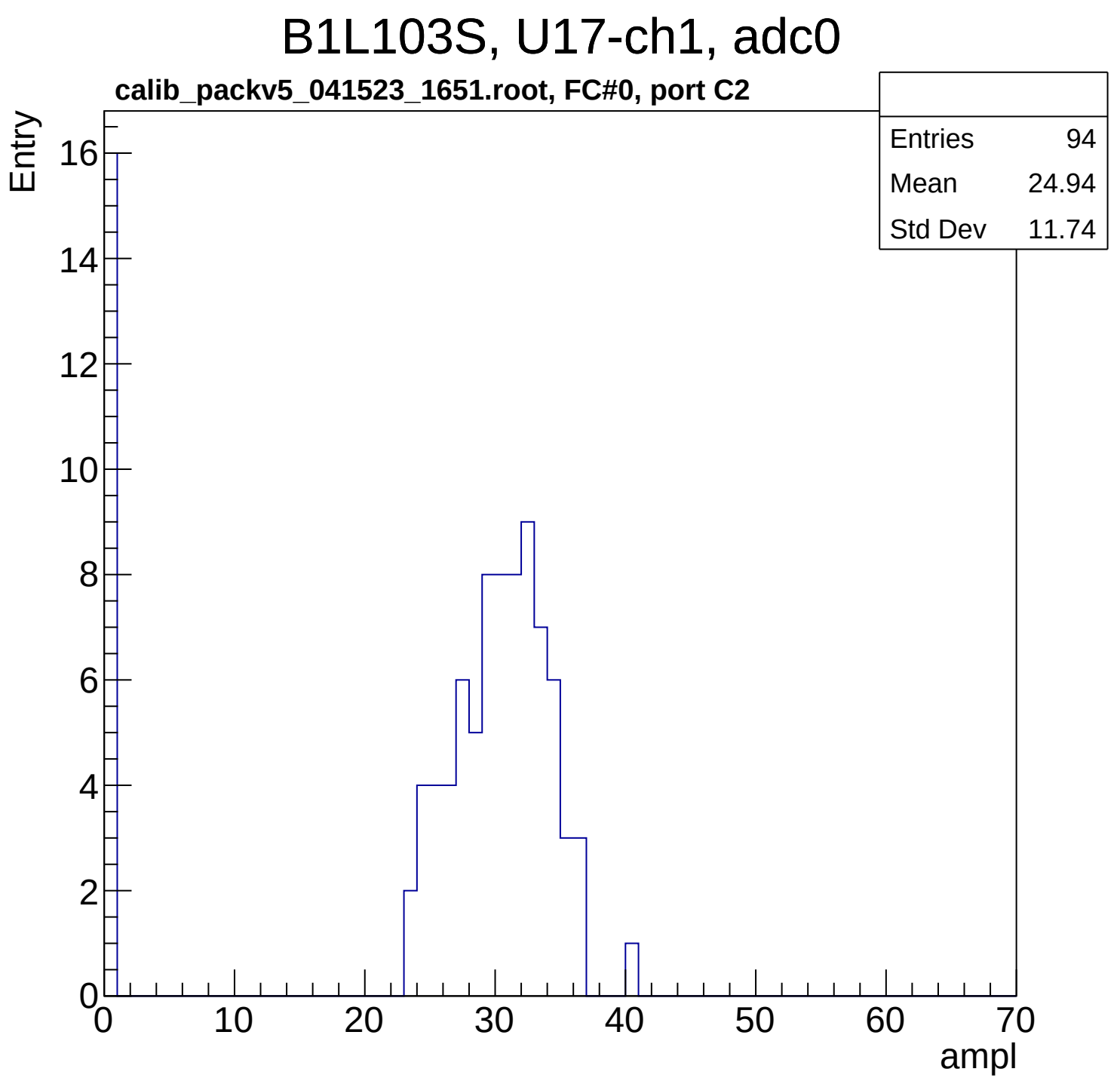
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch1, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 94
Mean 24.94
Std Dev 11.74
Entry
ampl
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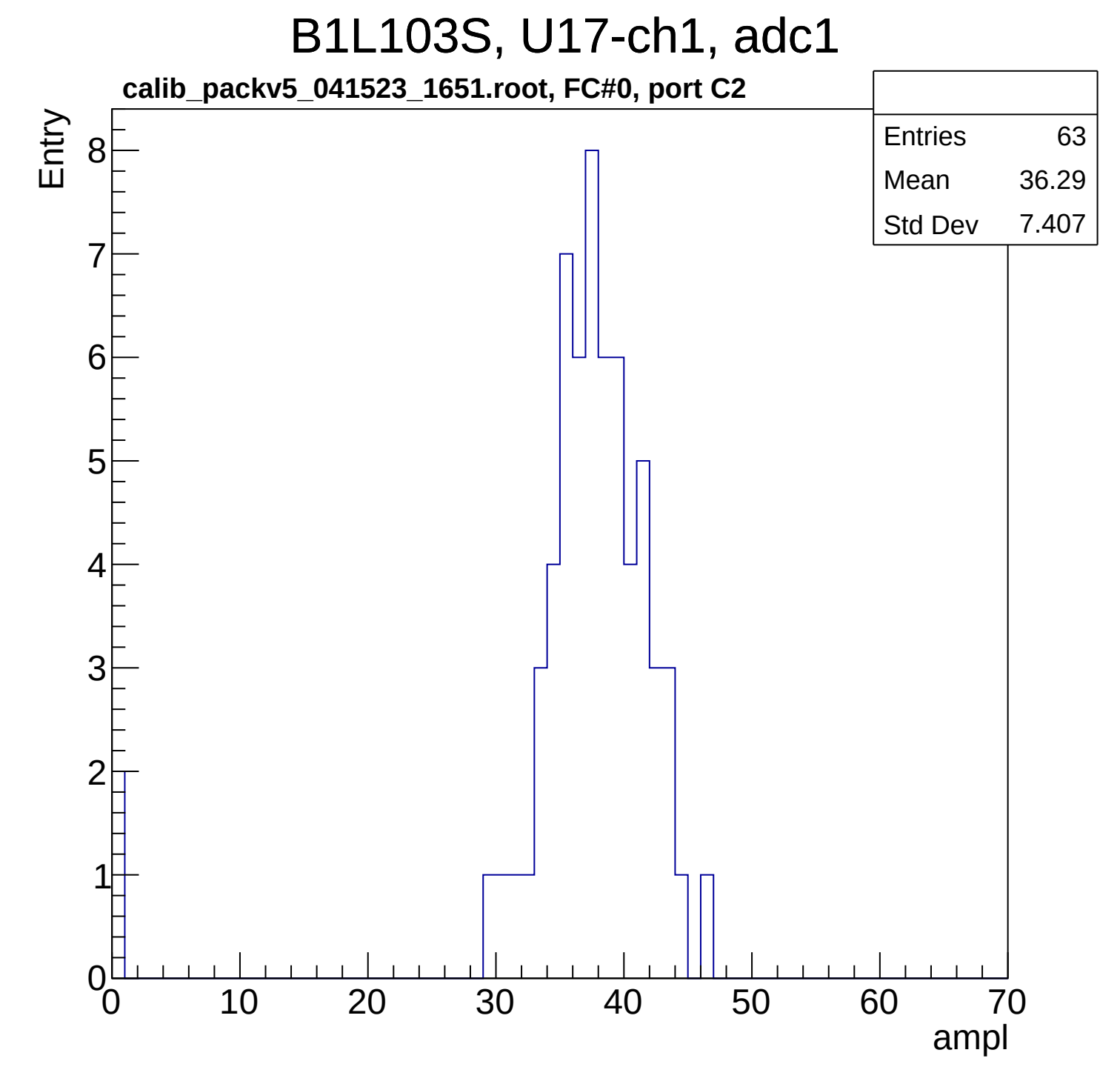
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70


B1L103S, U17-ch1, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 36.29
Std Dev 7.407
Entry
ampl
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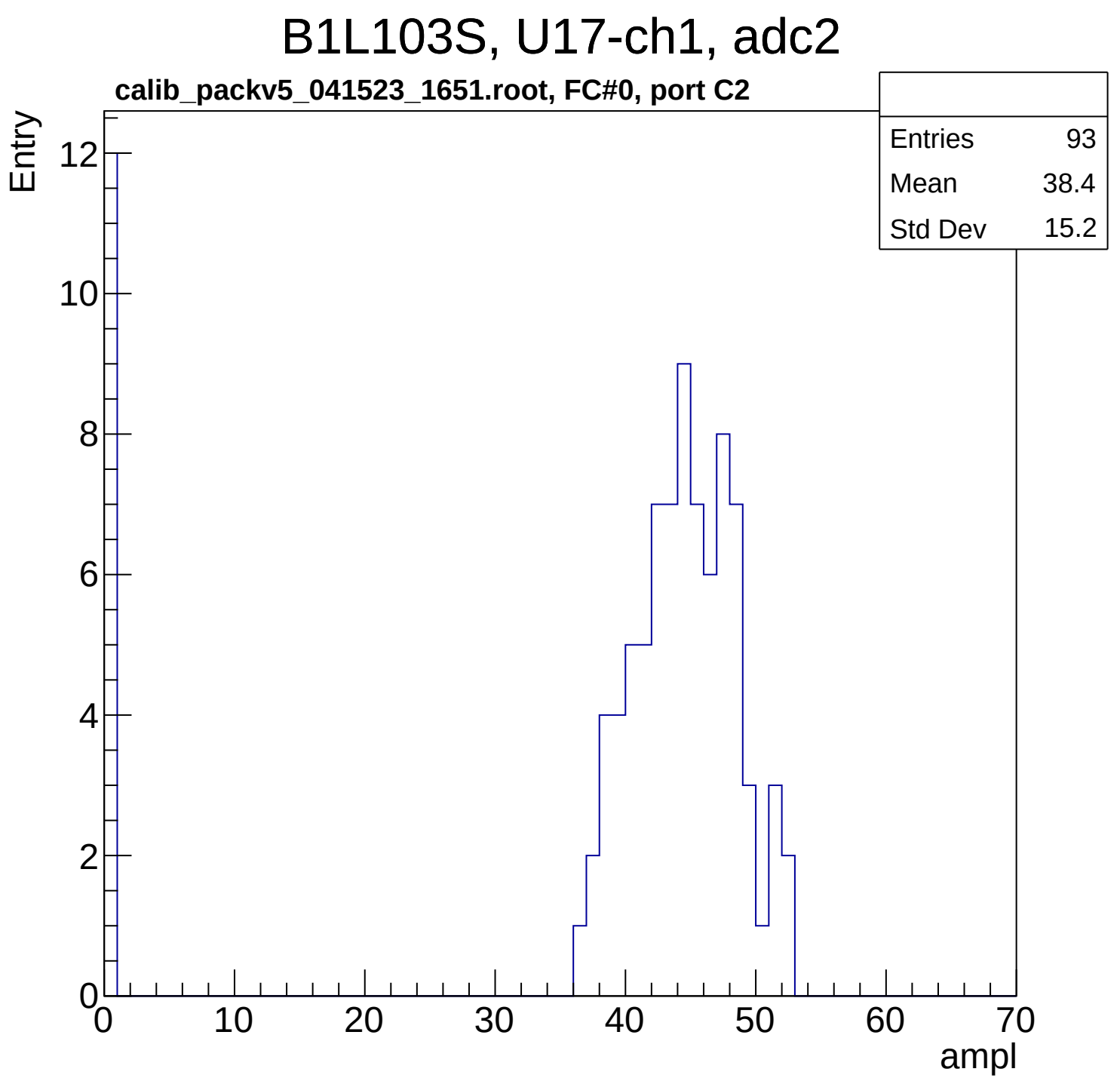
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U17-ch1, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 93
Mean 38.4
Std Dev 15.2
Entry
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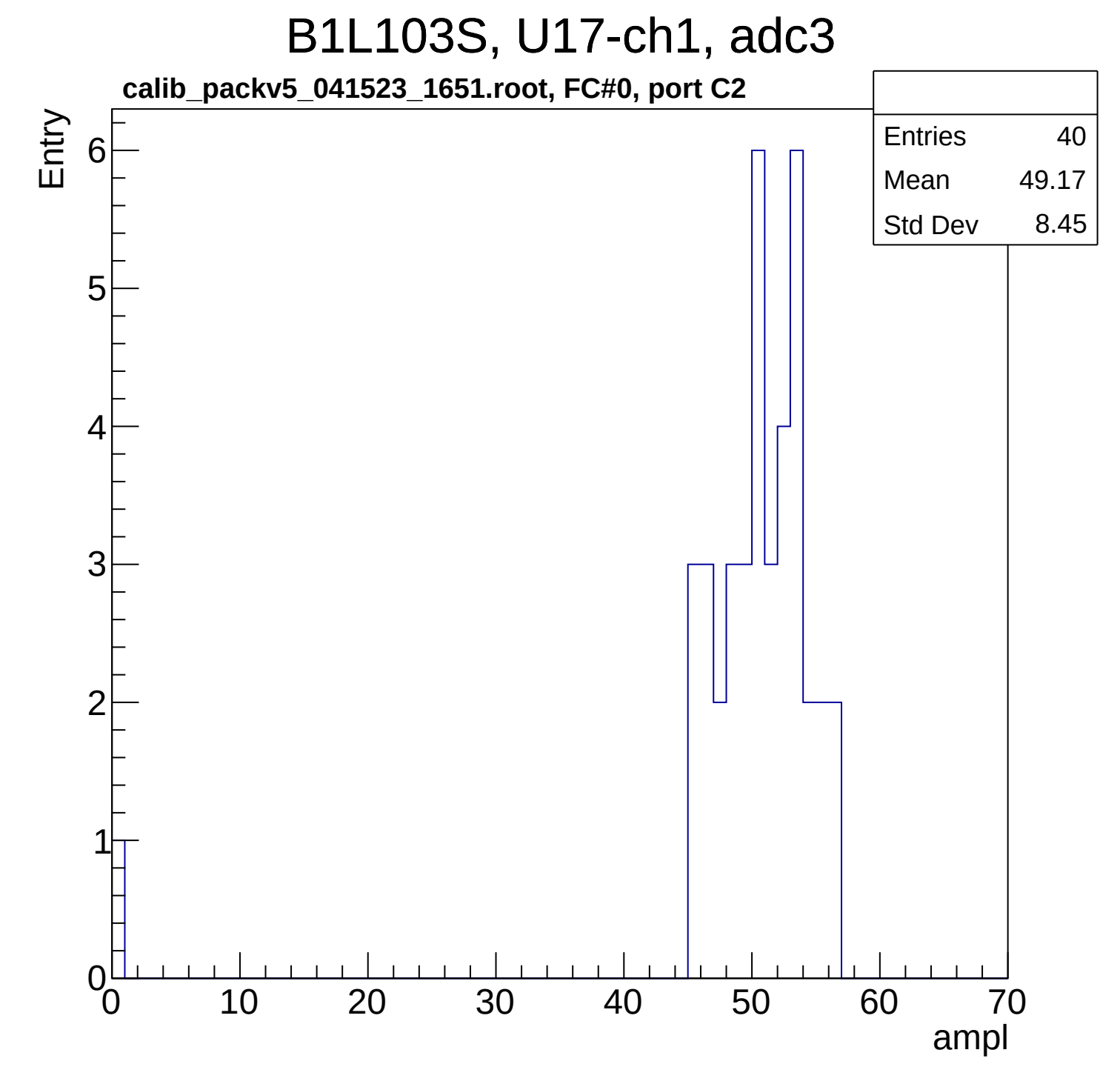
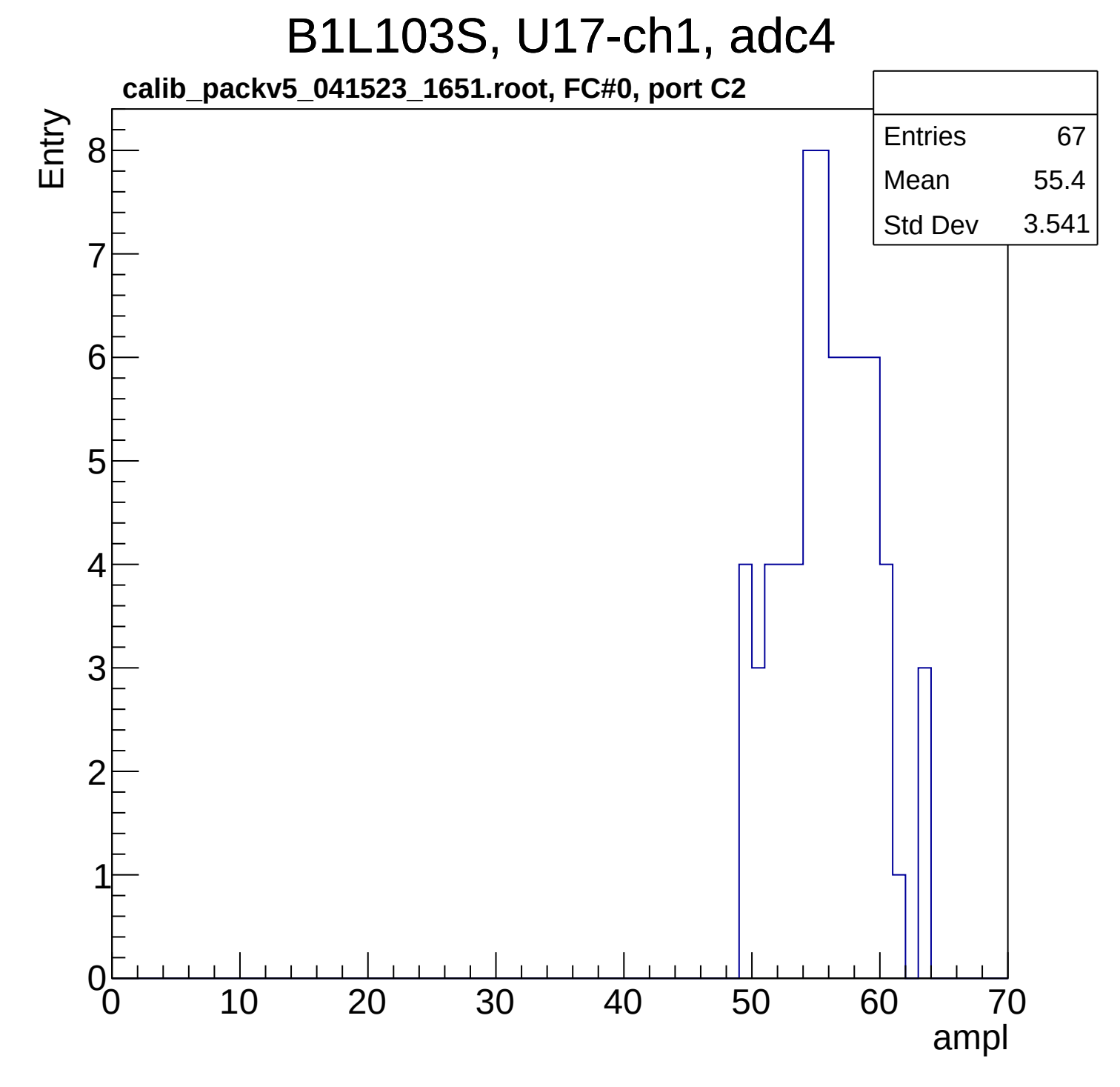
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch1, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 40
Mean 49.17
Std Dev 8.45
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U17-ch1, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 55.4
Std Dev 3.541
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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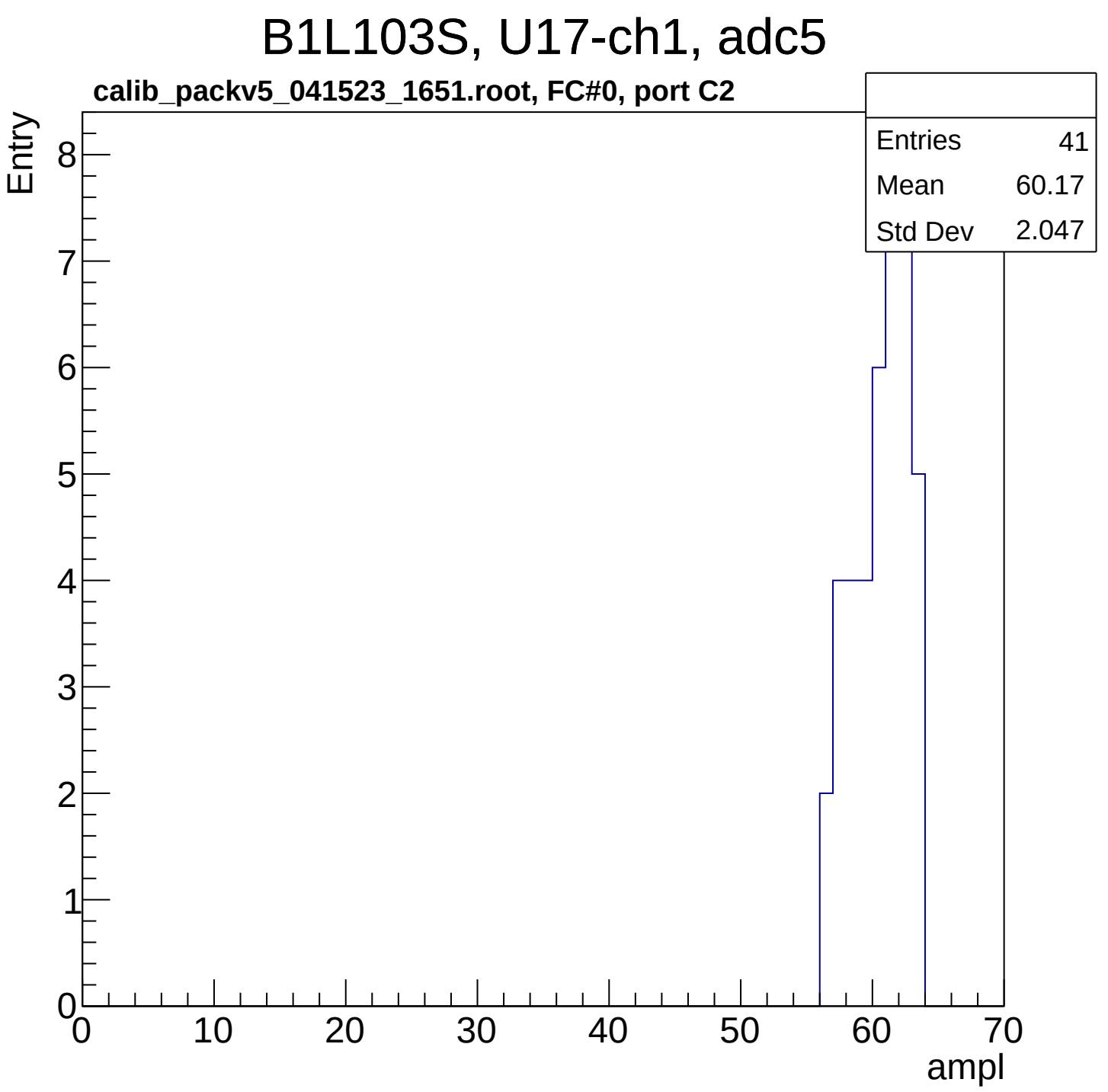
B1L103S, U17-ch1, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 41
Mean 60.17
Std Dev 2.047
Entry
ampl
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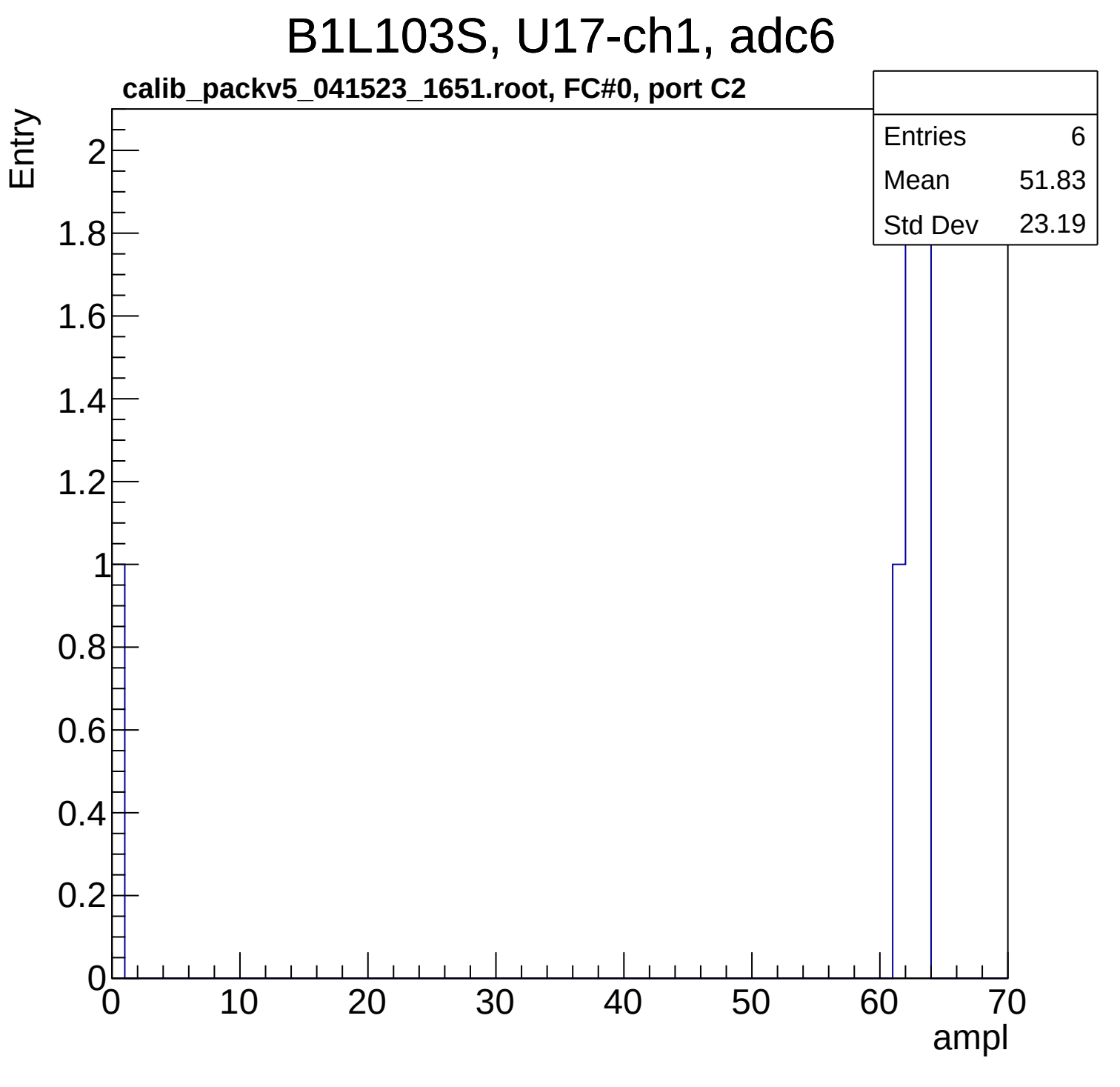
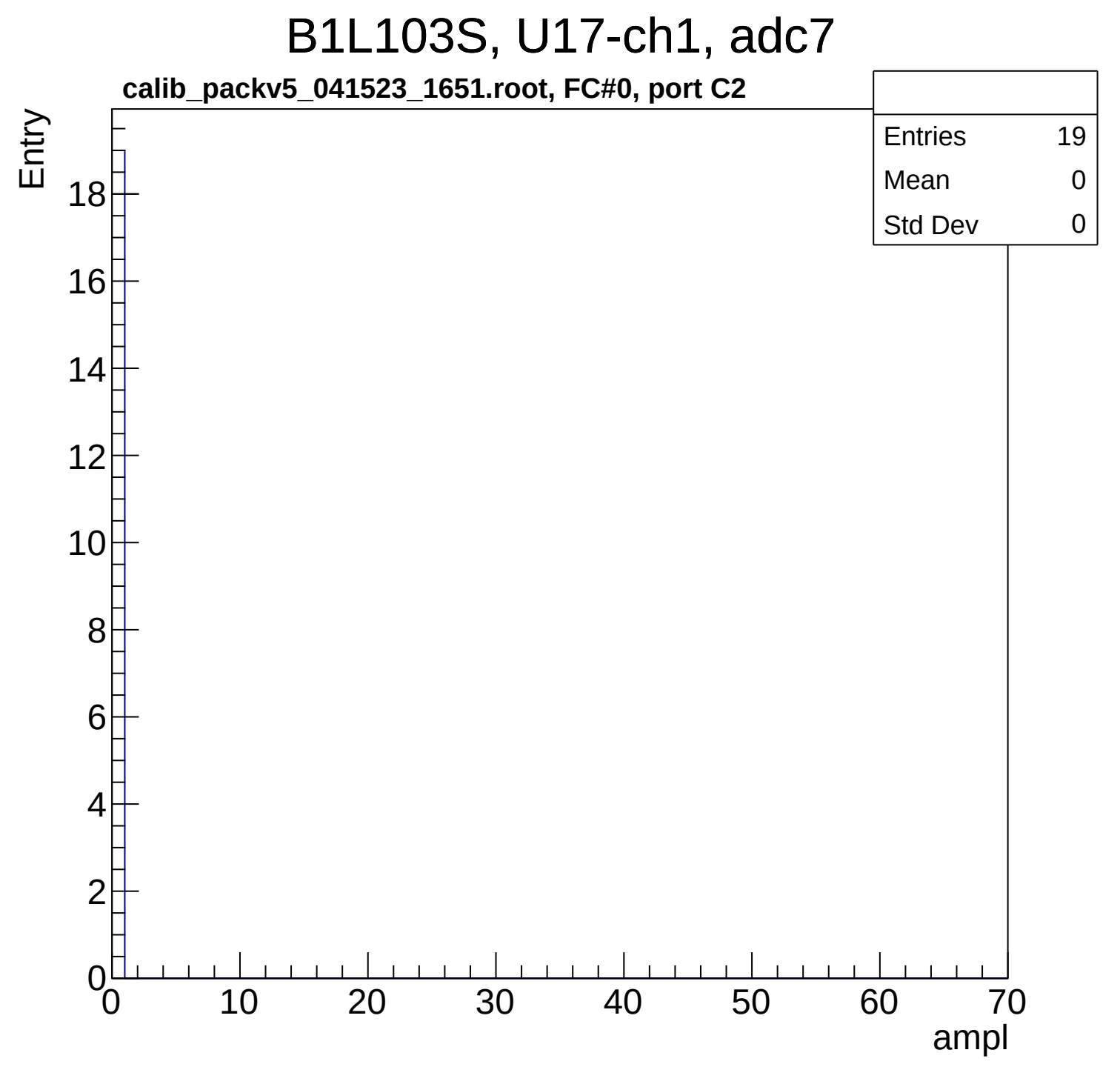
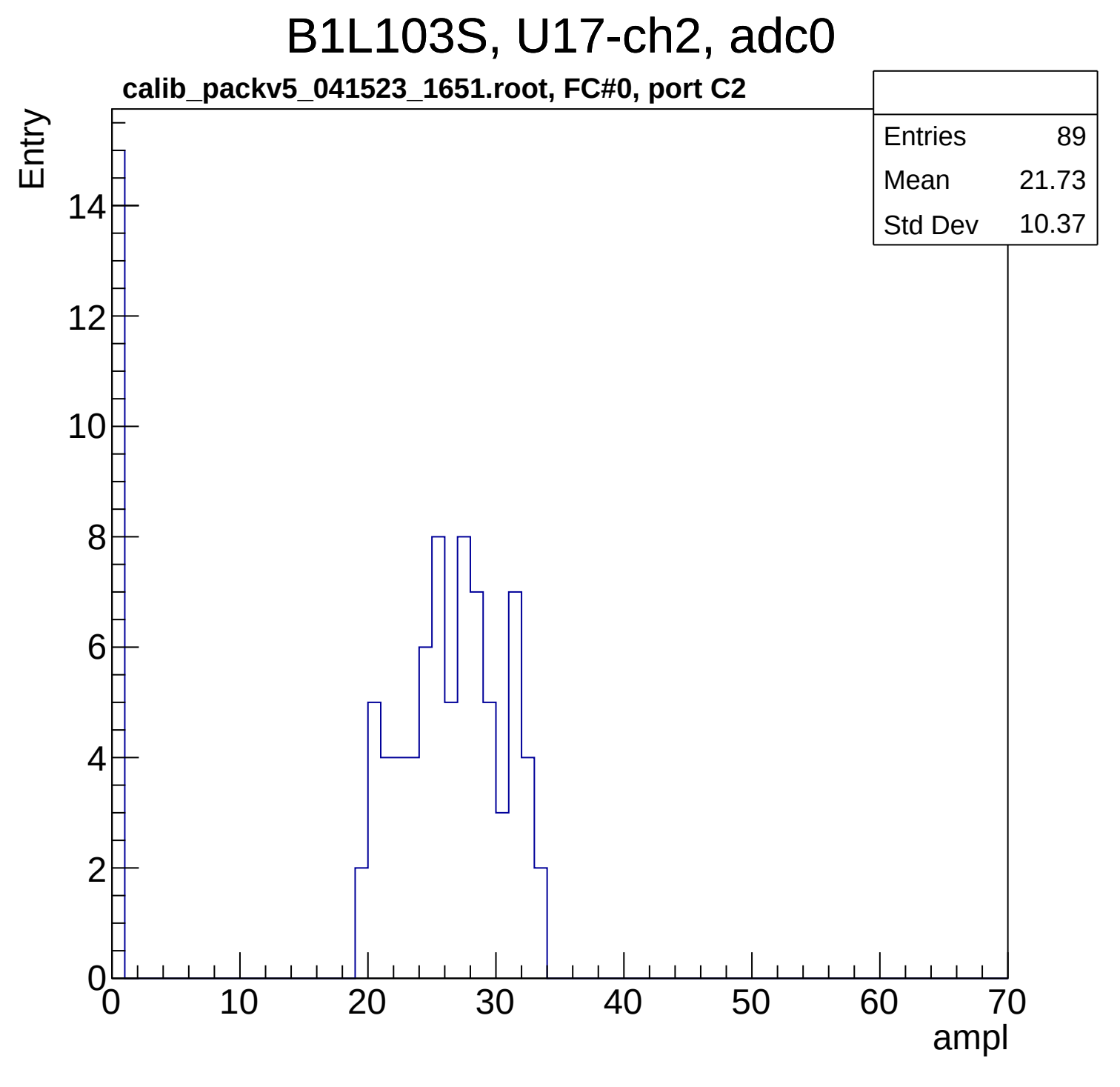
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U17-ch1, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 51.83
Std Dev 23.19
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U17-ch1, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch2, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 89
Mean 21.73
Std Dev 10.37
Entry
ampl
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2
4
6
8
10
12
14
0
10
20
30
40
50
60
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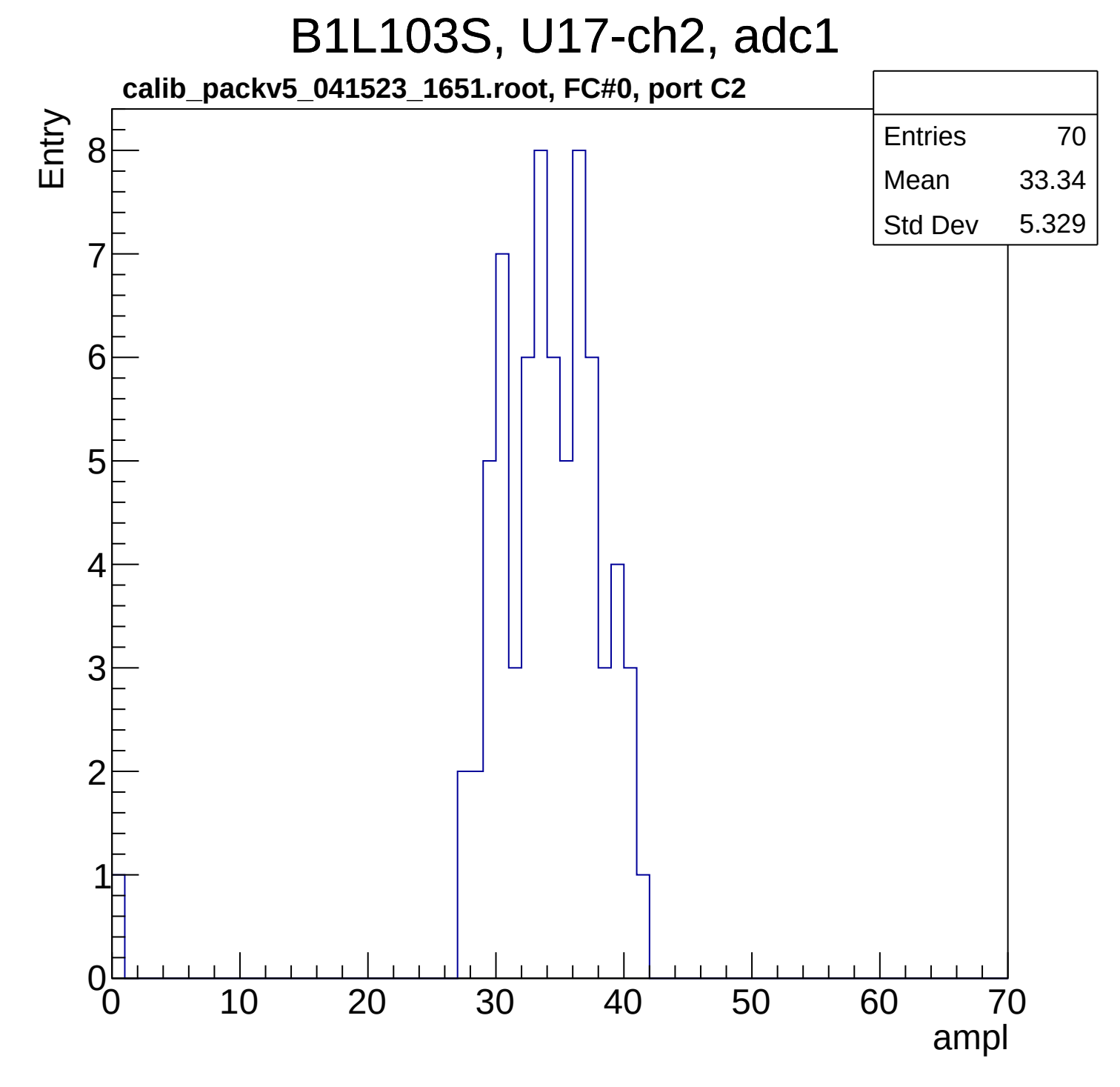
B1L103S, U17-ch2, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 33.34
Std Dev 5.329
Entry
ampl
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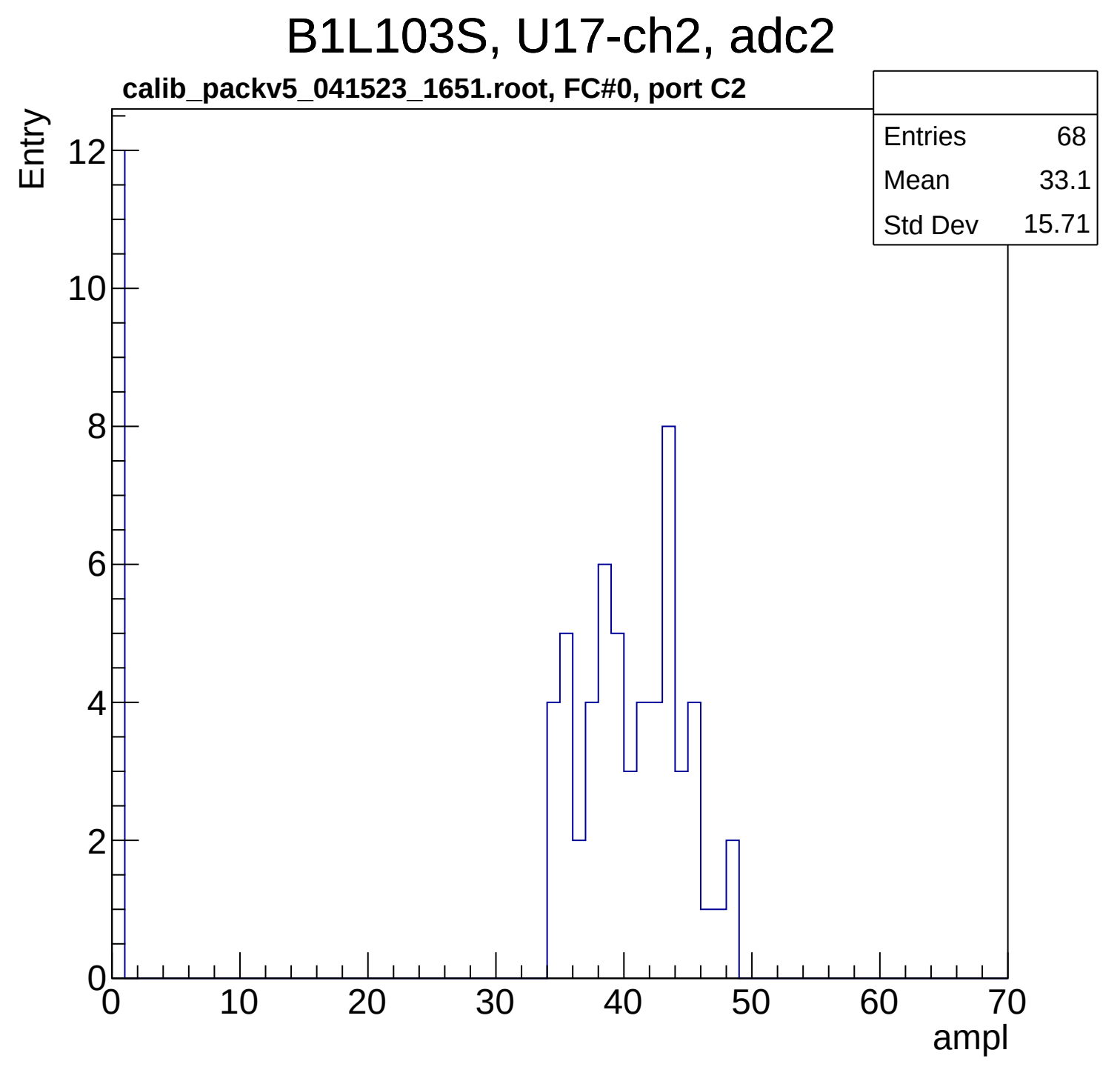
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U17-ch2, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 33.1
Std Dev 15.71
Entry
ampl
0
2
4
6
8
10
12
0
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20
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40
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60
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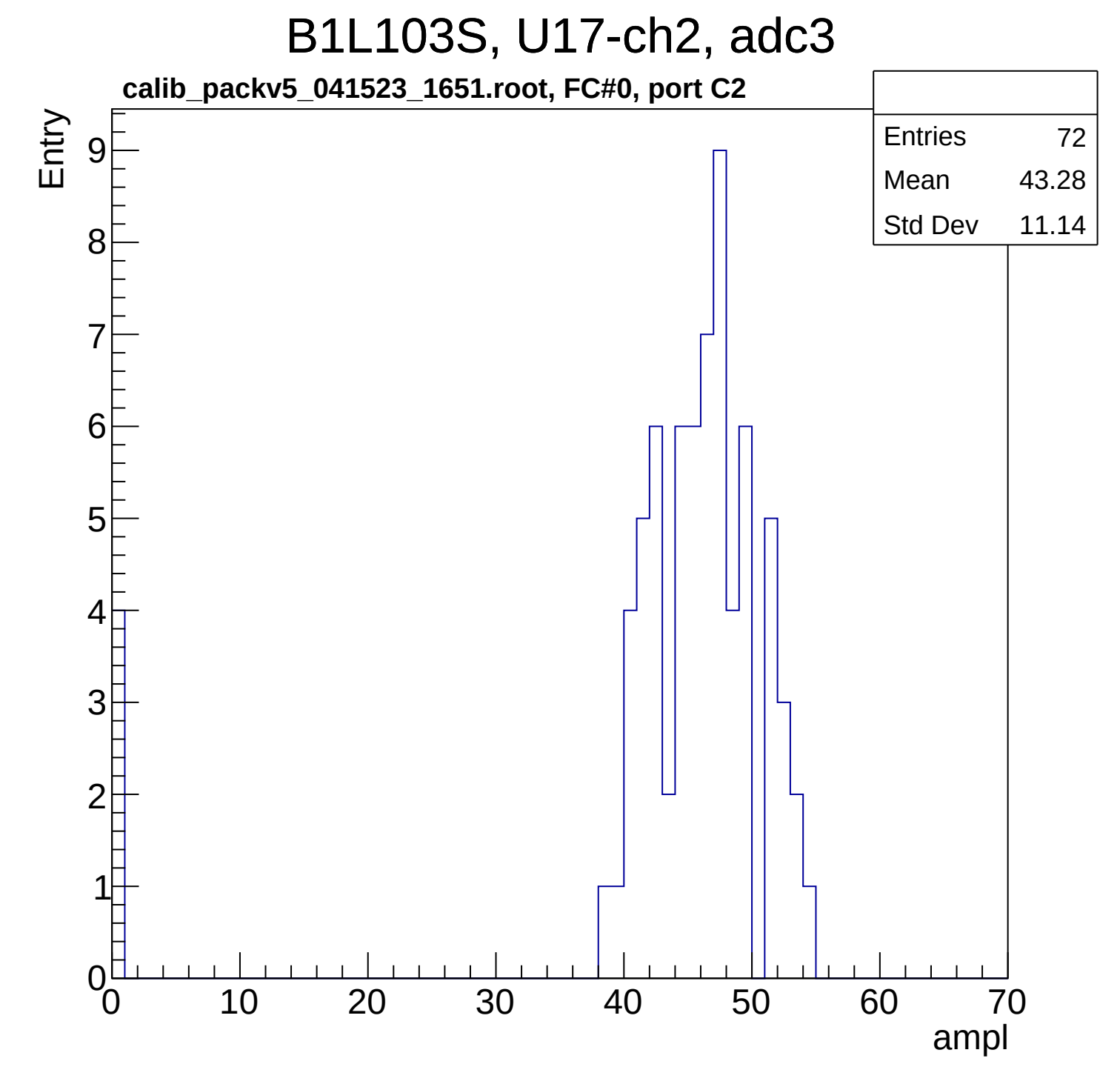
B1L103S, U17-ch2, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 43.28
Std Dev 11.14
Entry
ampl
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3
4
5
6
7
8
9
0
10
20
30
40
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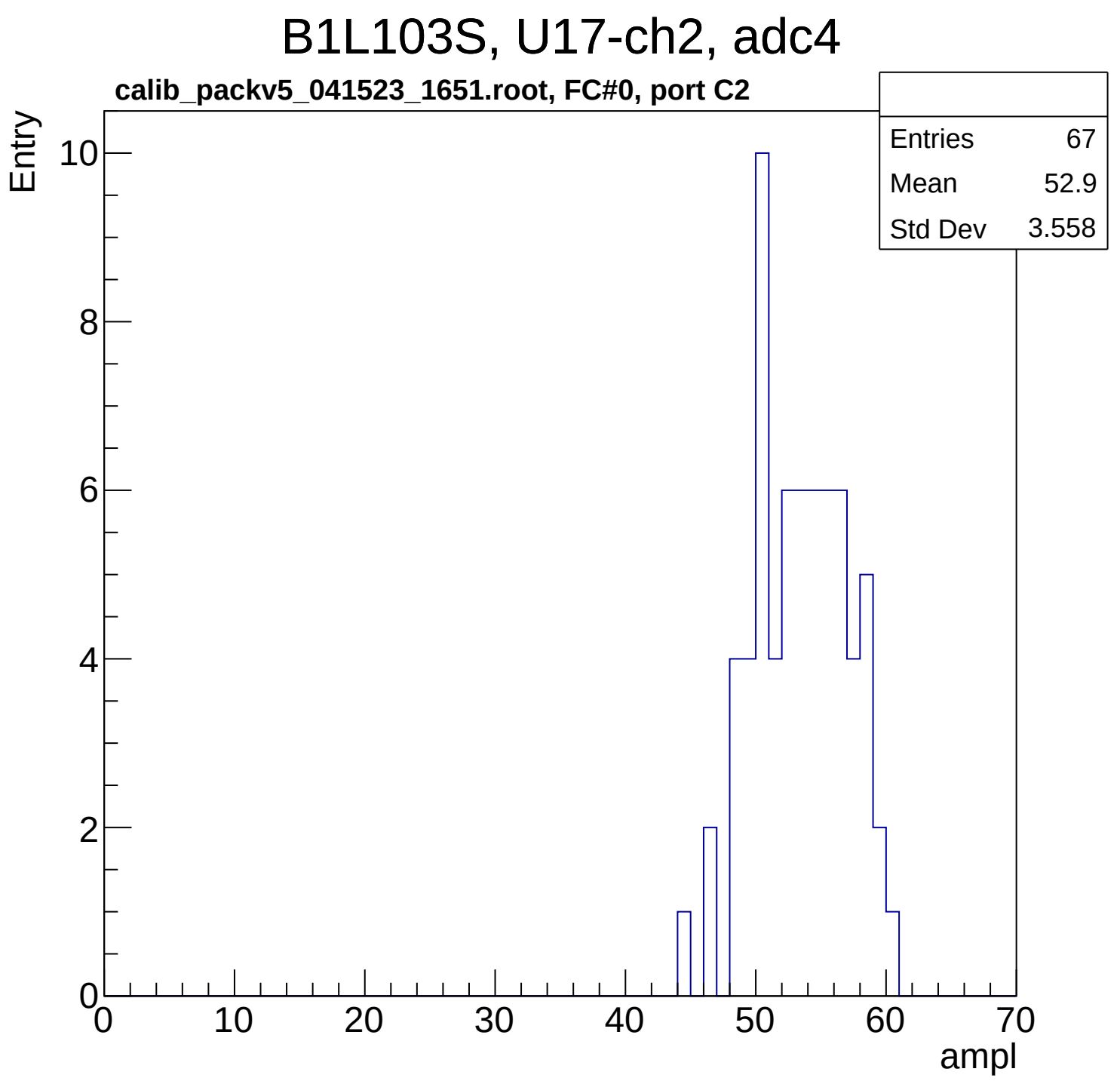
B1L103S, U17-ch2, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 52.9
Std Dev 3.558
Entry
ampl
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2
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10
0
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60
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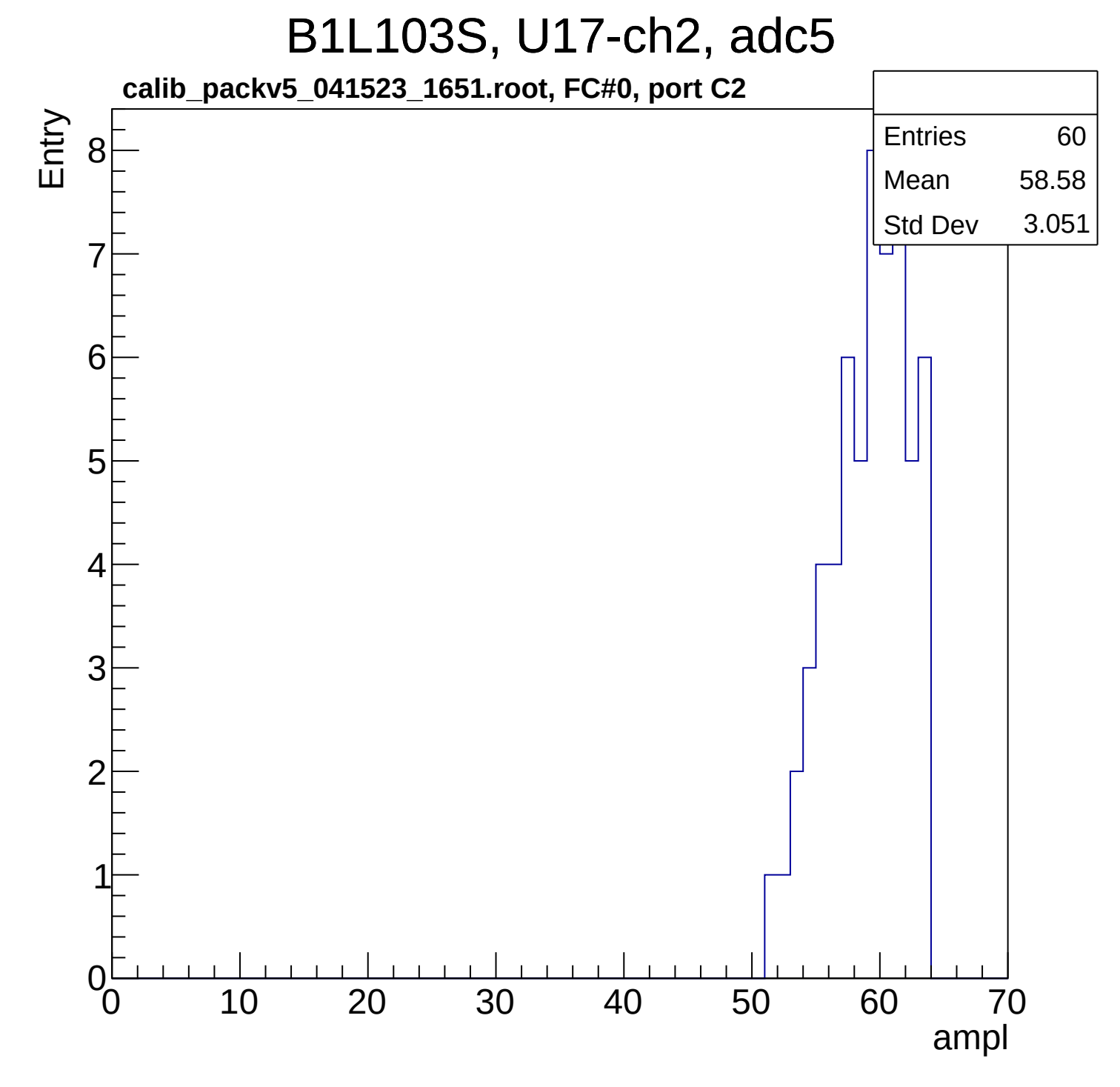
B1L103S, U17-ch2, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 58.58
Std Dev 3.051
Entry
ampl
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2
3
4
5
6
7
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0
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20
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60
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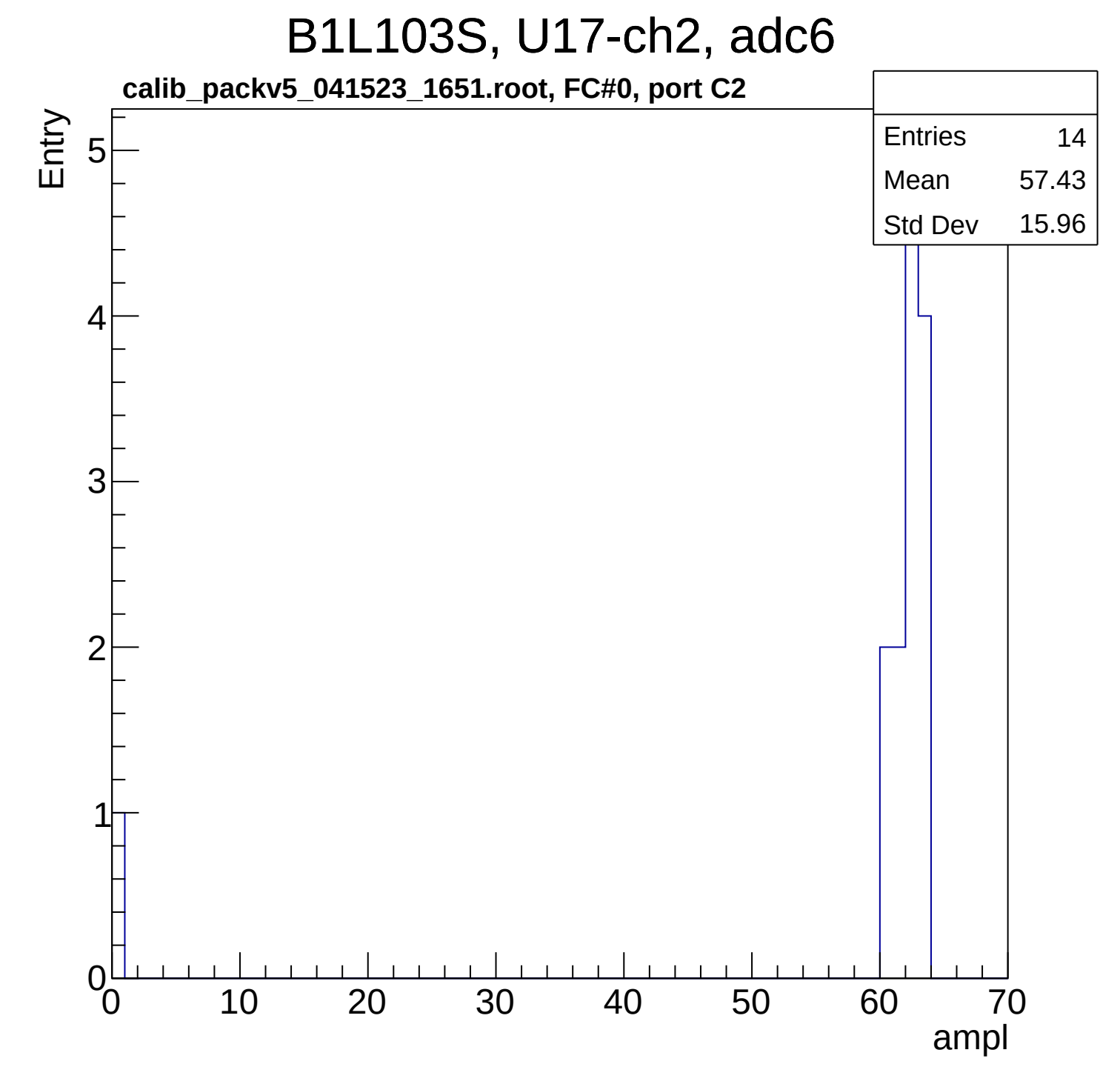
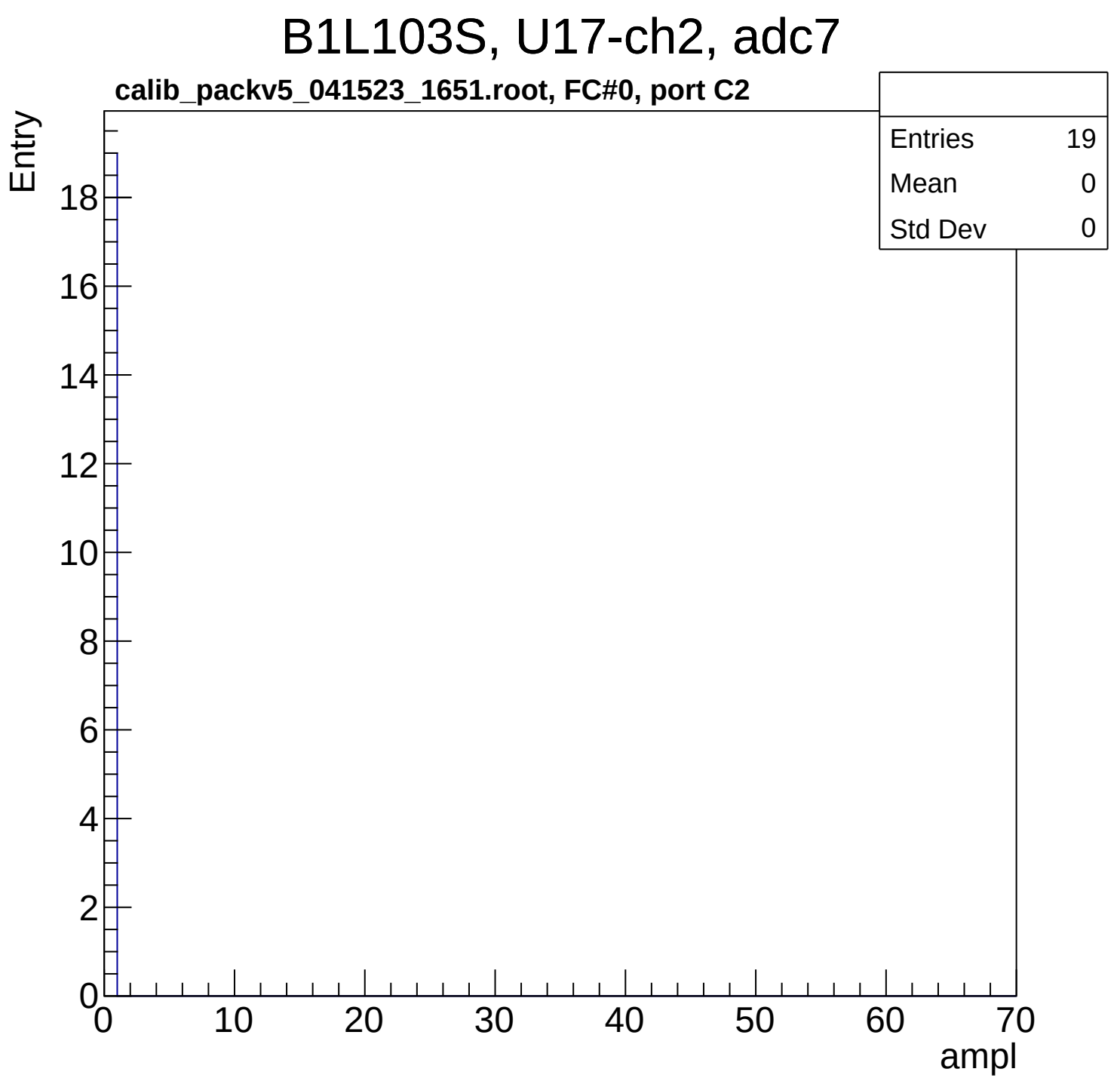

B1L103S, U17-ch2, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 14
Mean 57.43
Std Dev 15.96
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U17-ch2, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
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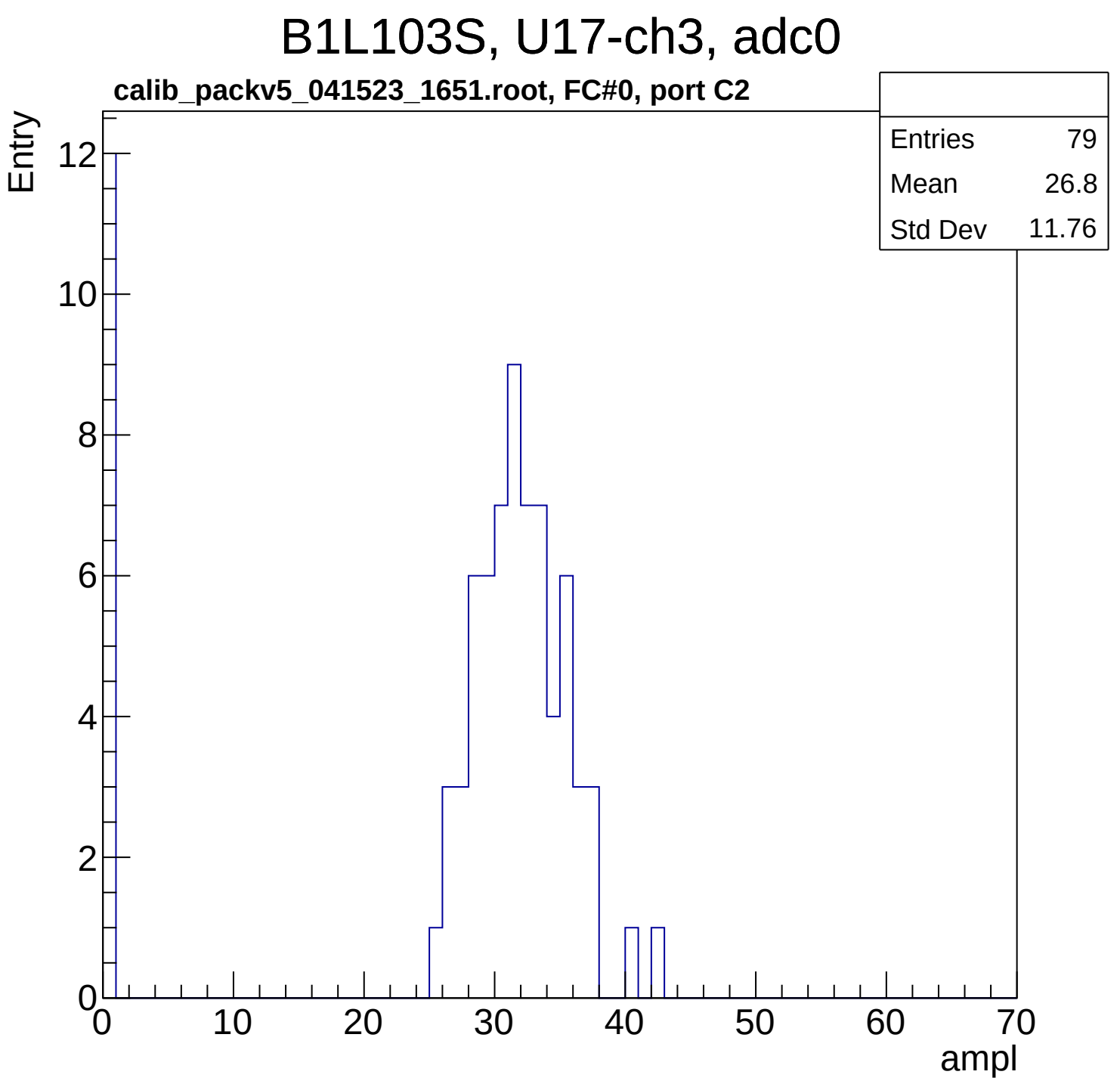
50
60
70
ampl


B1L103S, U17-ch3, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 26.8
Std Dev 11.76
Entry
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8
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10
20
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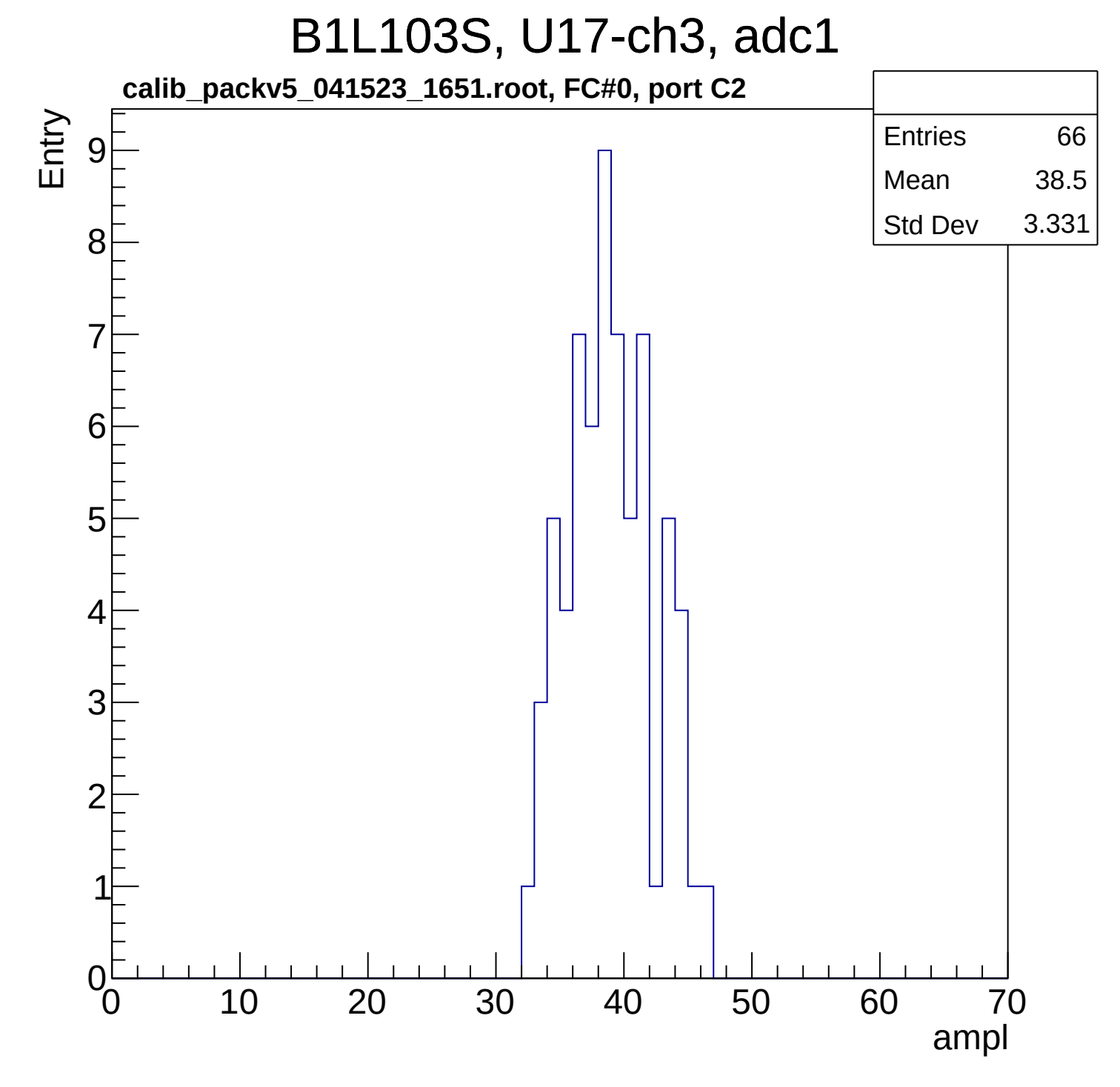
60
70
ampl


B1L103S, U17-ch3, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 38.5
Std Dev 3.331
Entry
ampl
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3
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0
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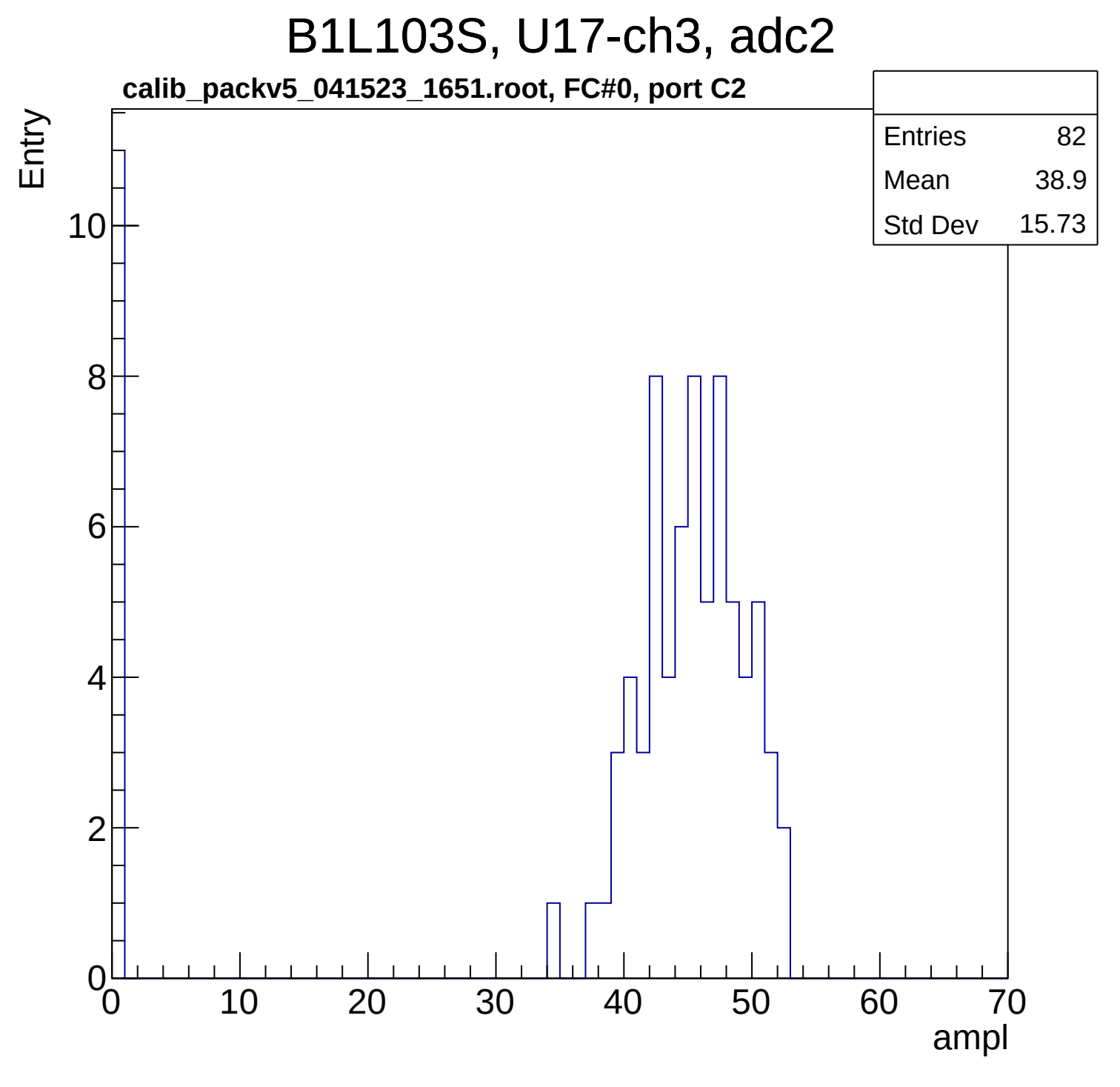
60
70


B1L103S, U17-ch3, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 38.9
Std Dev 15.73
Entry
0
2
4
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10
0
10
20
30
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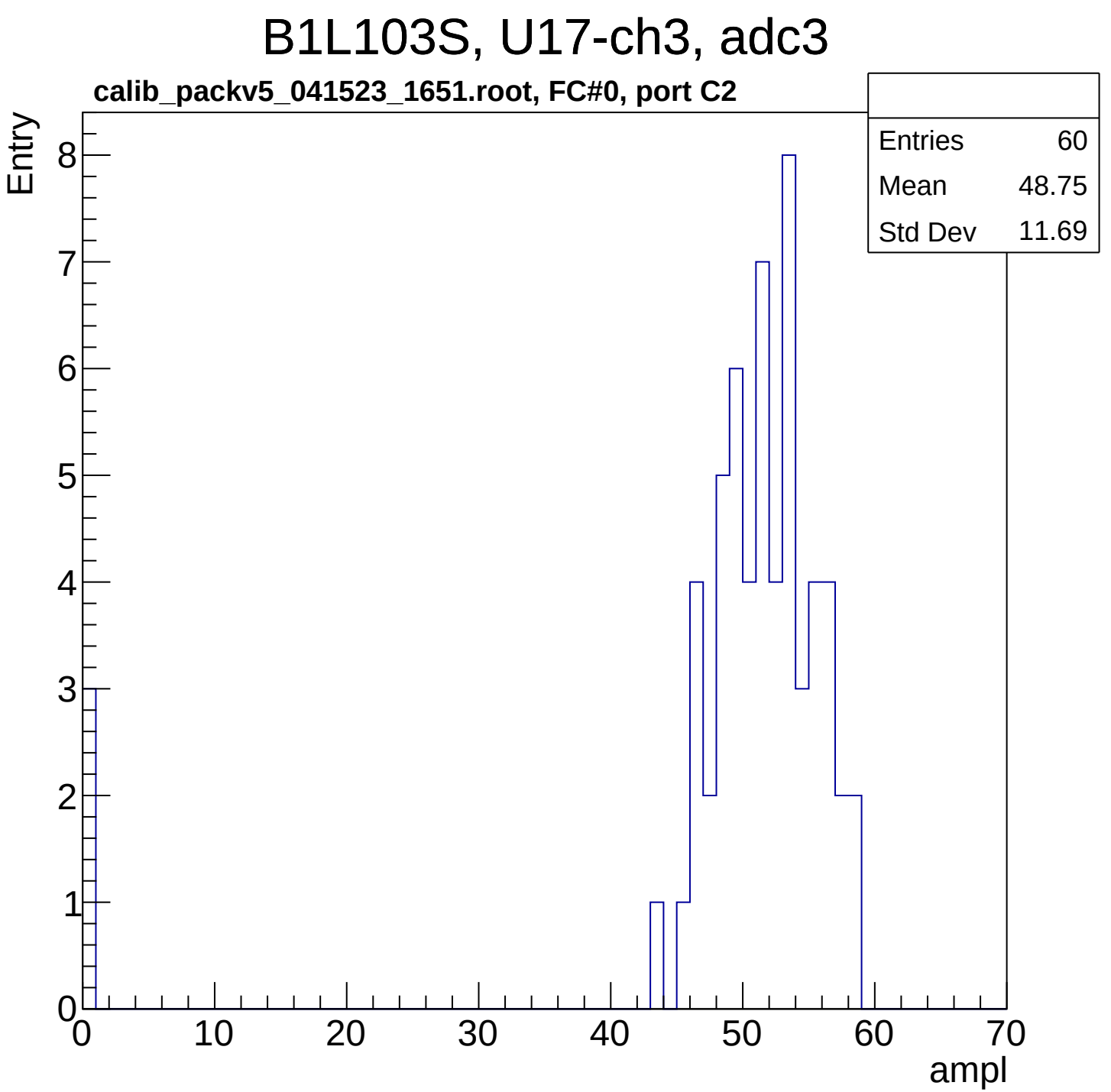
50
60
70
ampl


B1L103S, U17-ch3, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 48.75
Std Dev 11.69
Entry
ampl
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0
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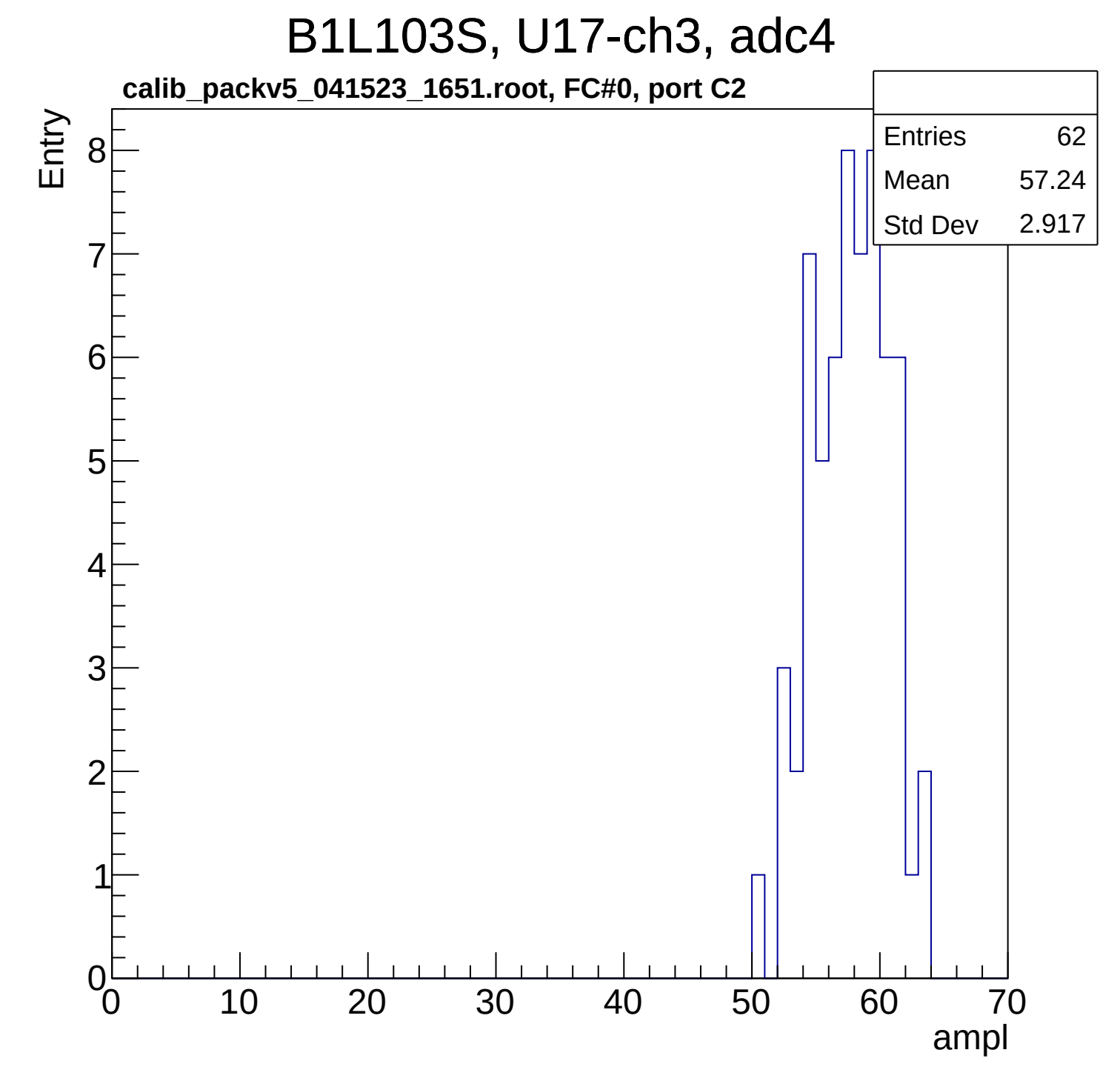
60
70


B1L103S, U17-ch3, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 57.24
Std Dev 2.917
Entry
ampl
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60
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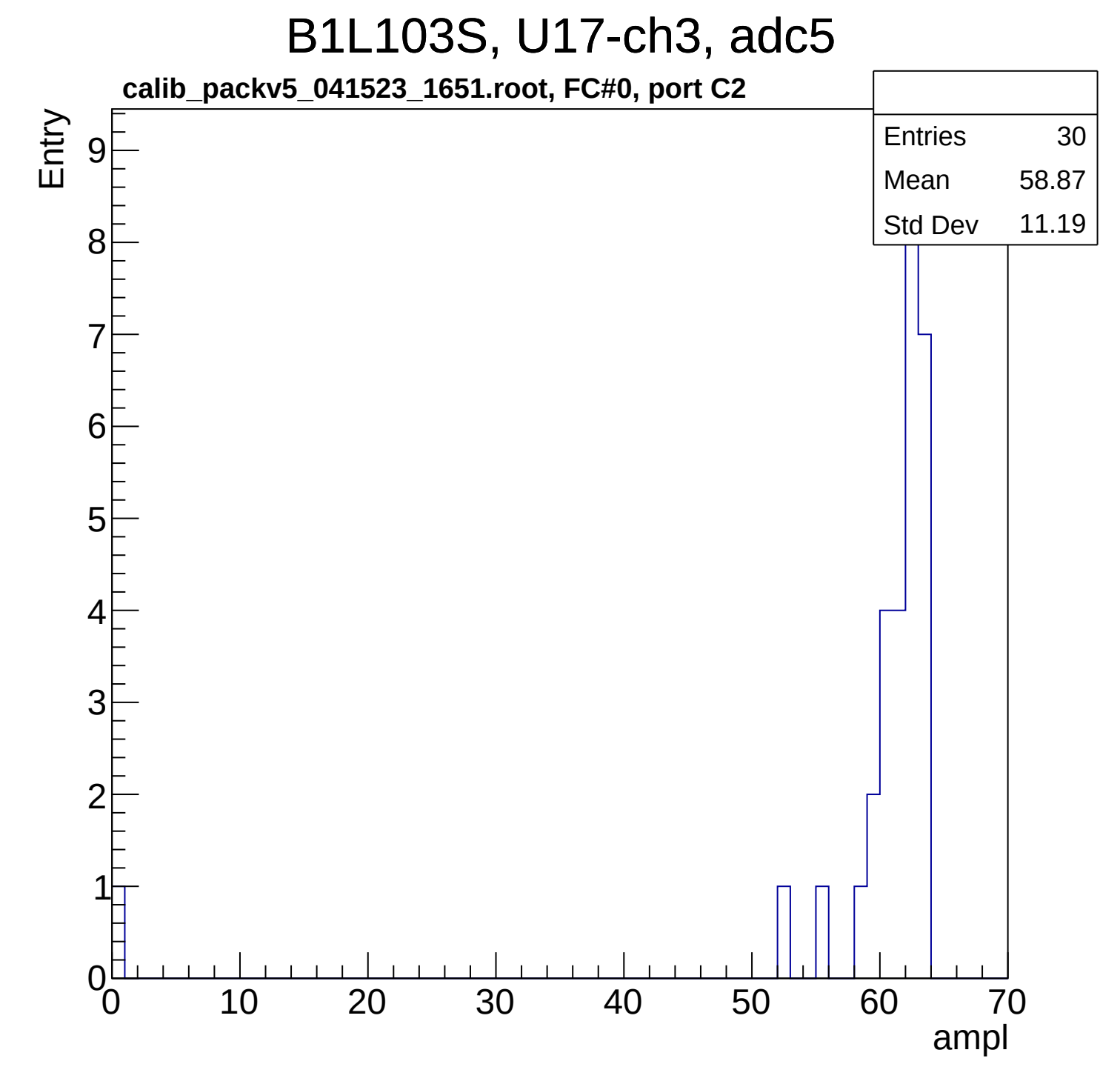
B1L103S, U17-ch3, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 30
Mean 58.87
Std Dev 11.19
Entry
ampl
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4
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60
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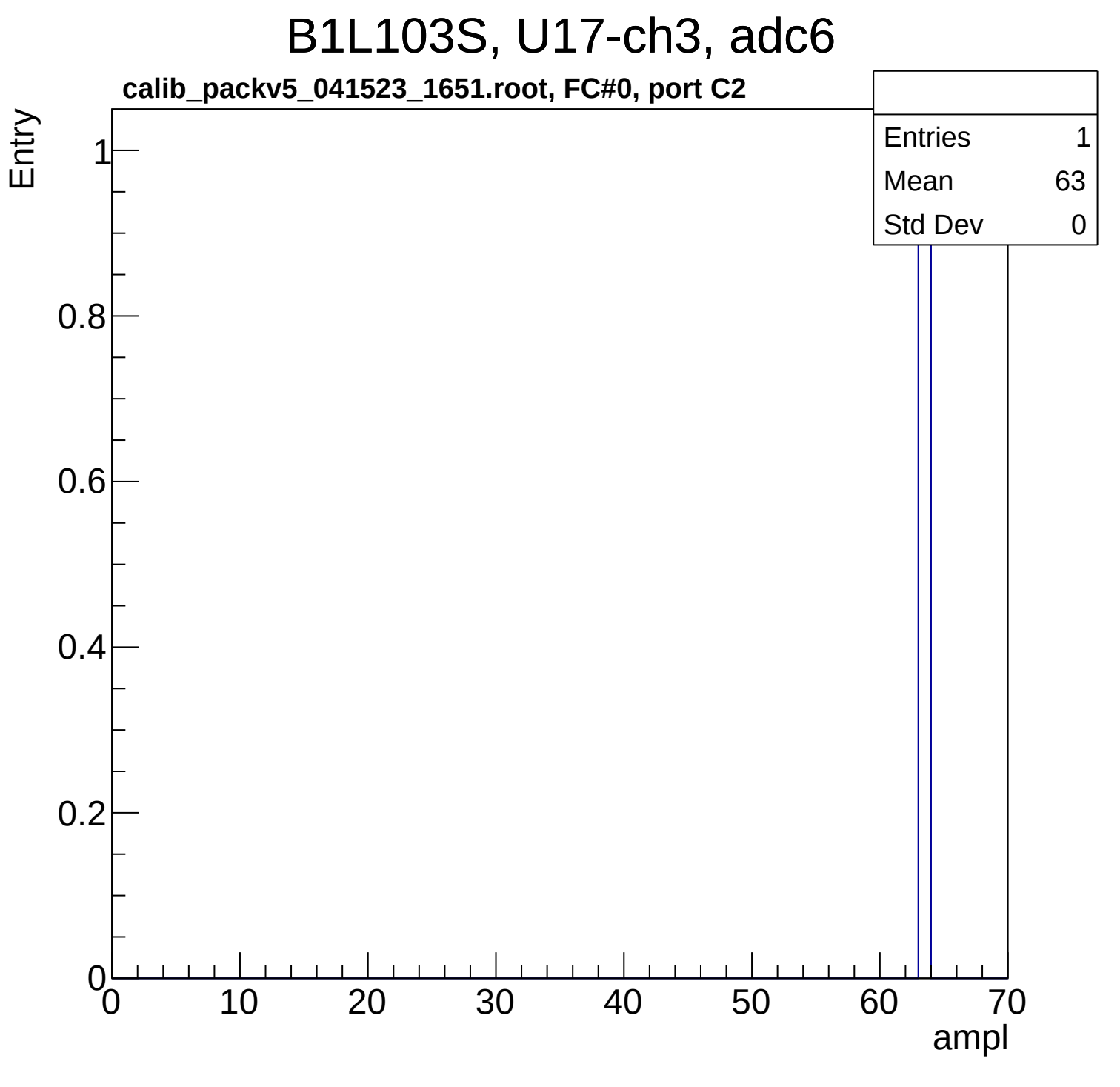
B1L103S, U17-ch3, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 1
Mean 63
Std Dev 0
Entry
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0.6
0.4
0.2
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0
10
20
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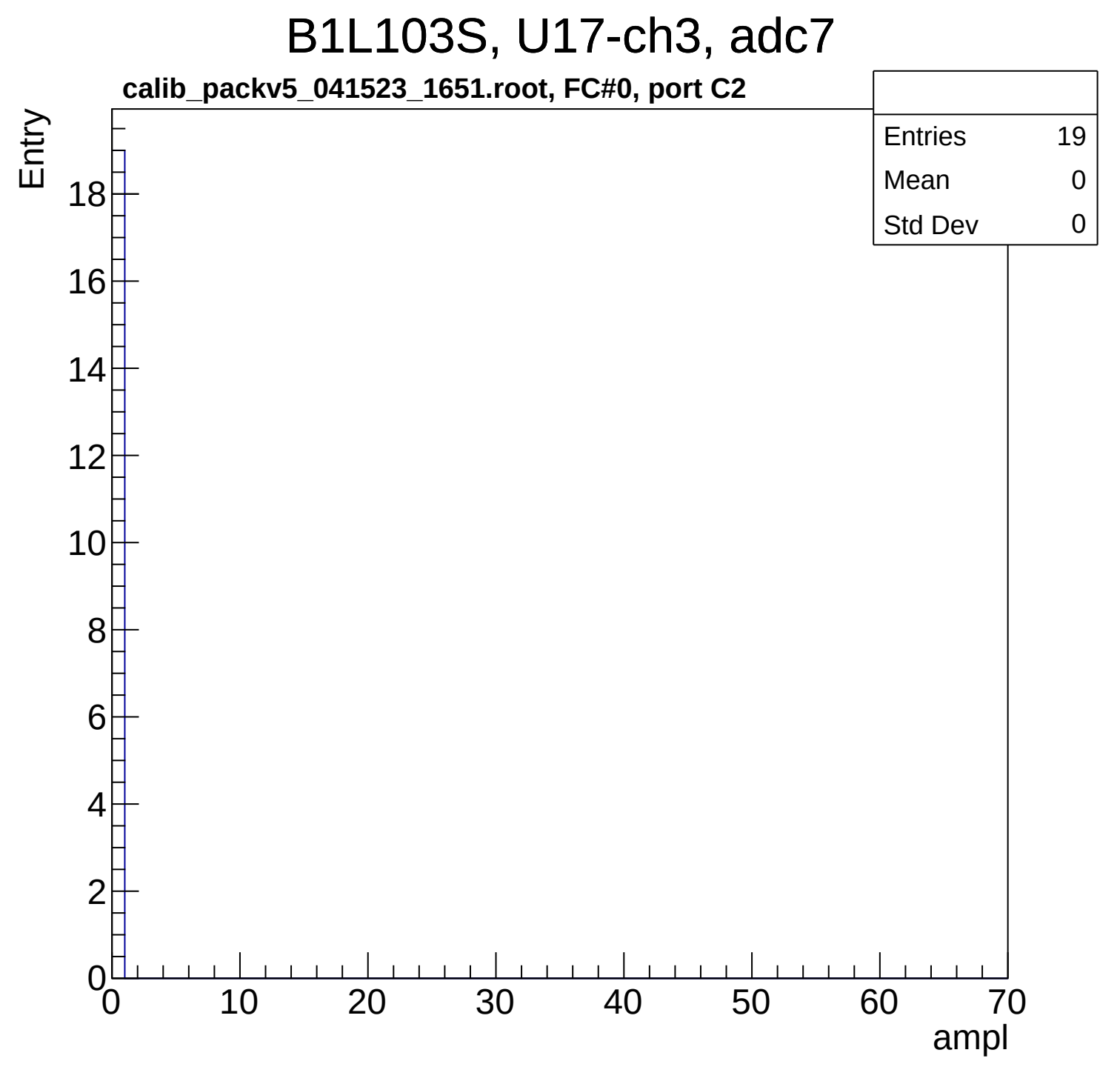
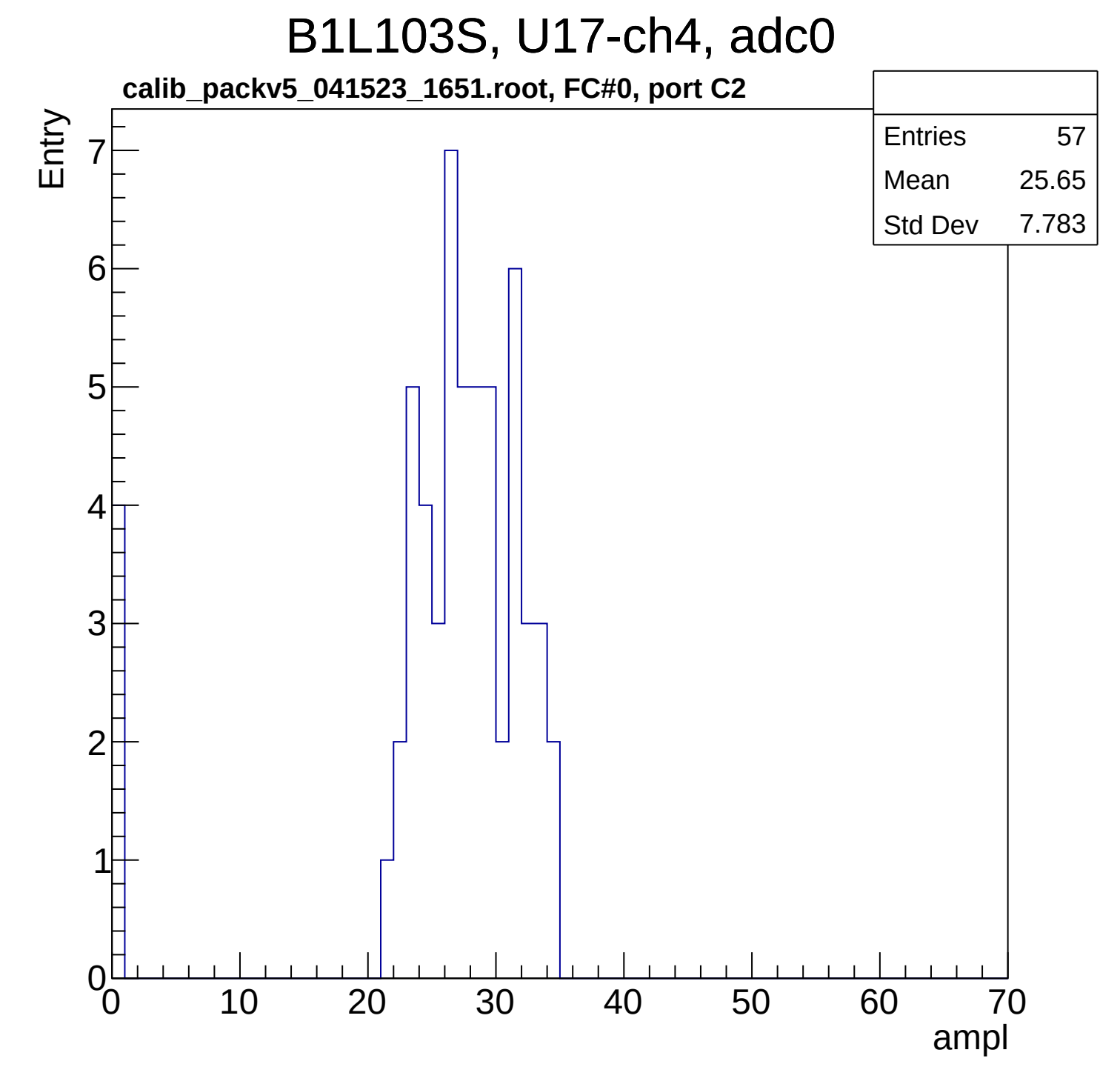
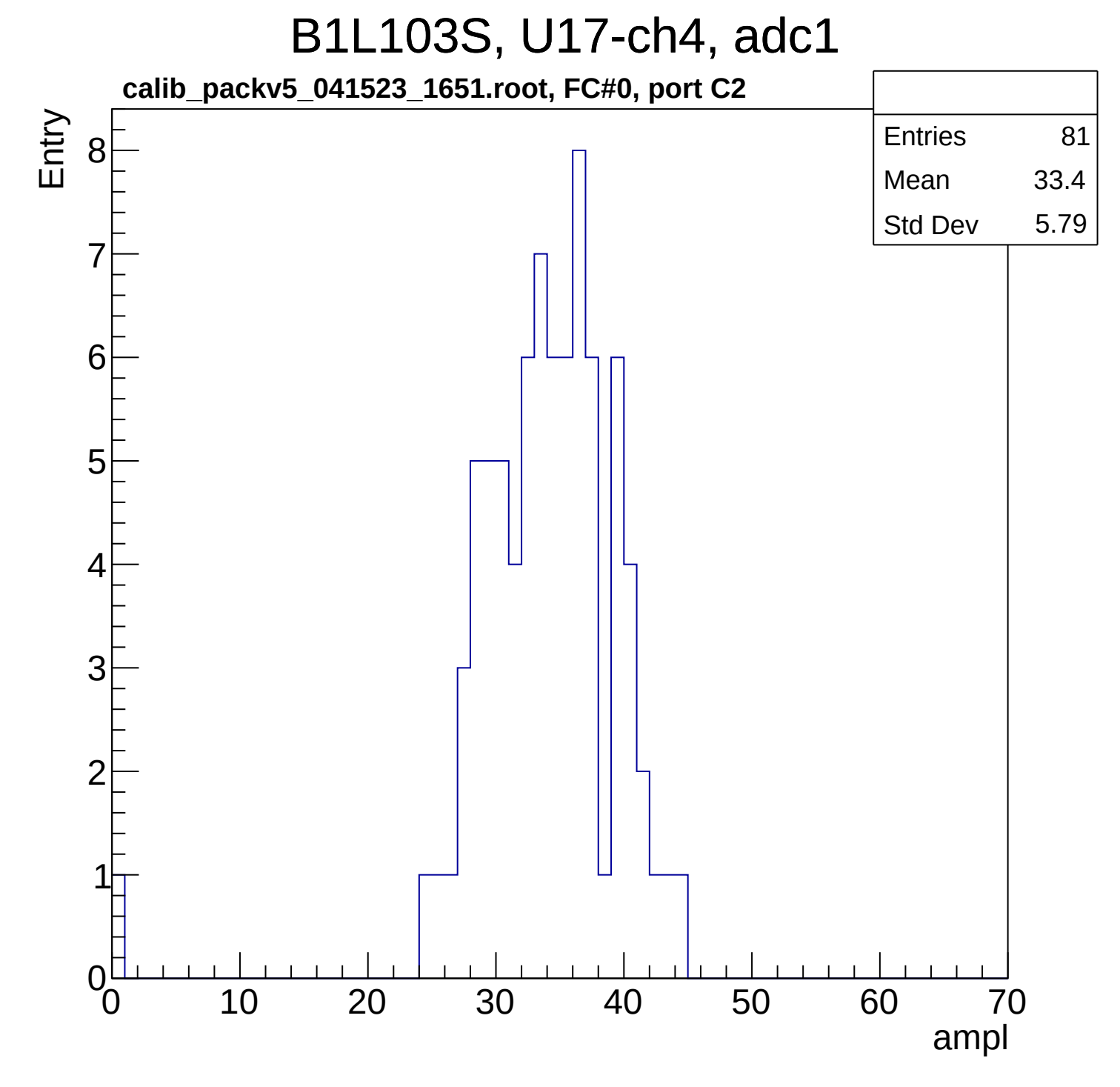
40
50
60
70
ampl


B1L103S, U17-ch3, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch4, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 25.65
Std Dev 7.783
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U17-ch4, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 33.4
Std Dev 5.79
Entry
ampl
0
1
2
3
4
5
6
7
8
0
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20
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40
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60
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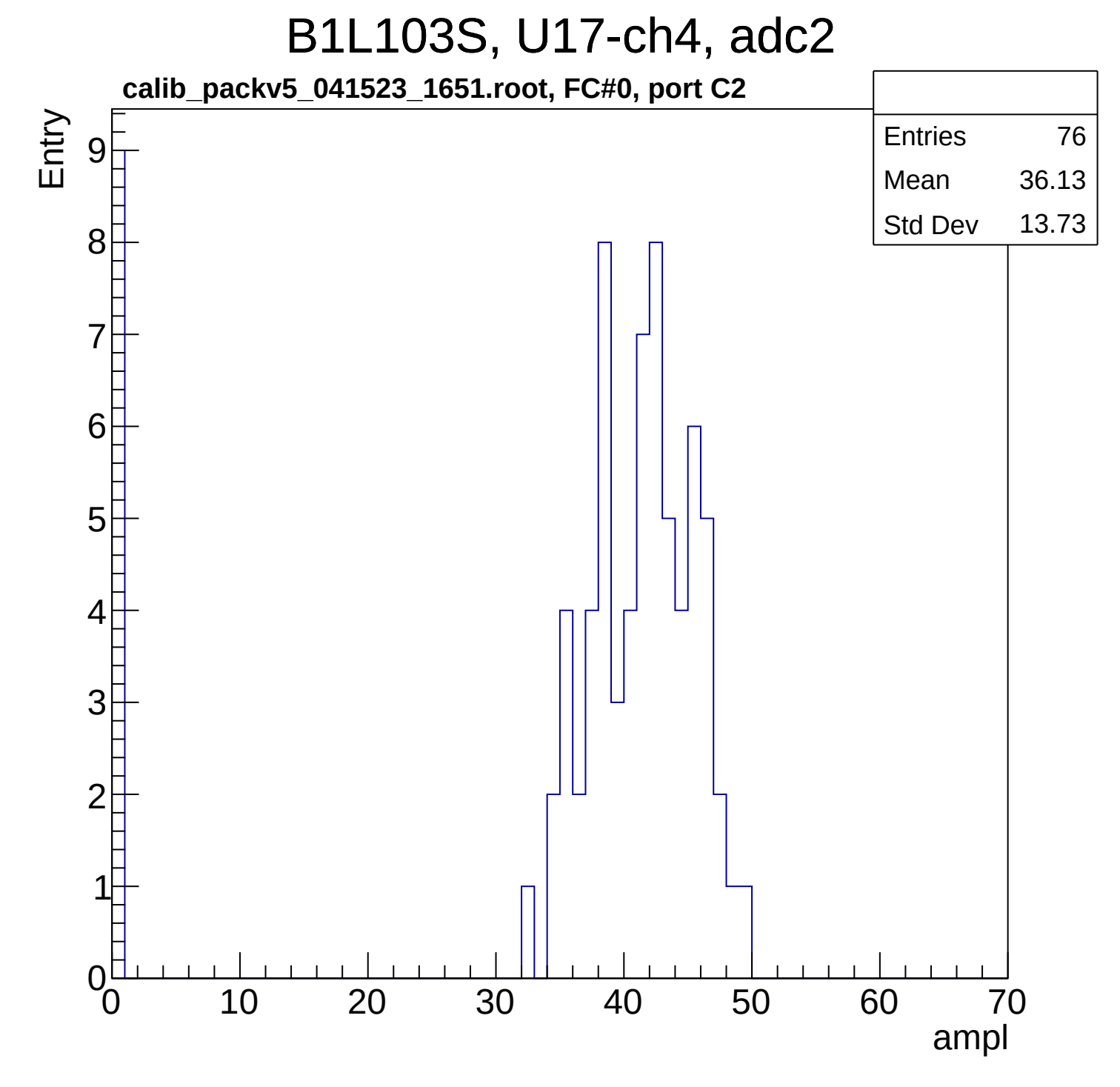
B1L103S, U17-ch4, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 36.13
Std Dev 13.73
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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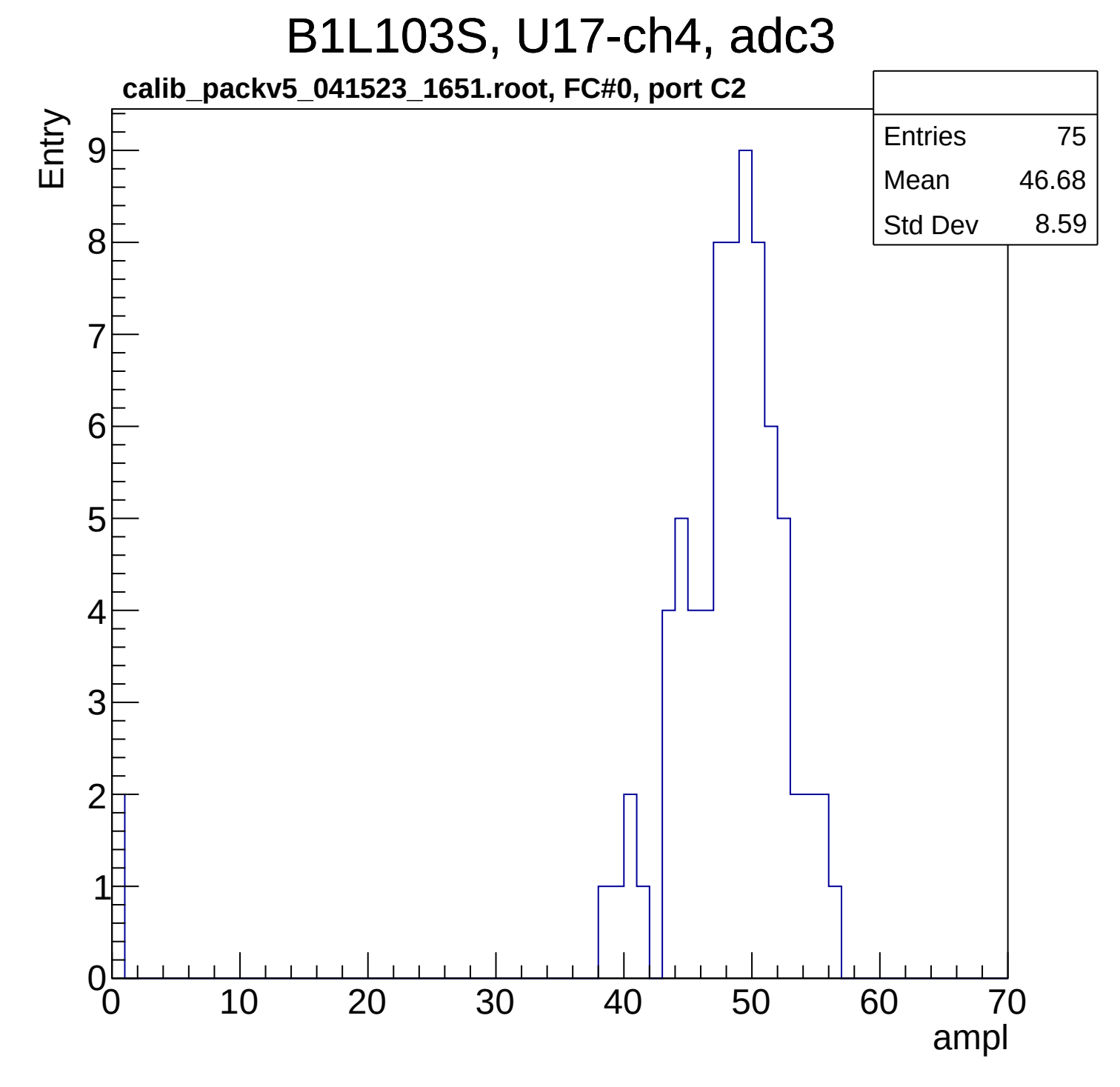
B1L103S, U17-ch4, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 46.68
Std Dev 8.59
Entry
ampl
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2
3
4
5
6
7
8
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0
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20
30
40
50
60
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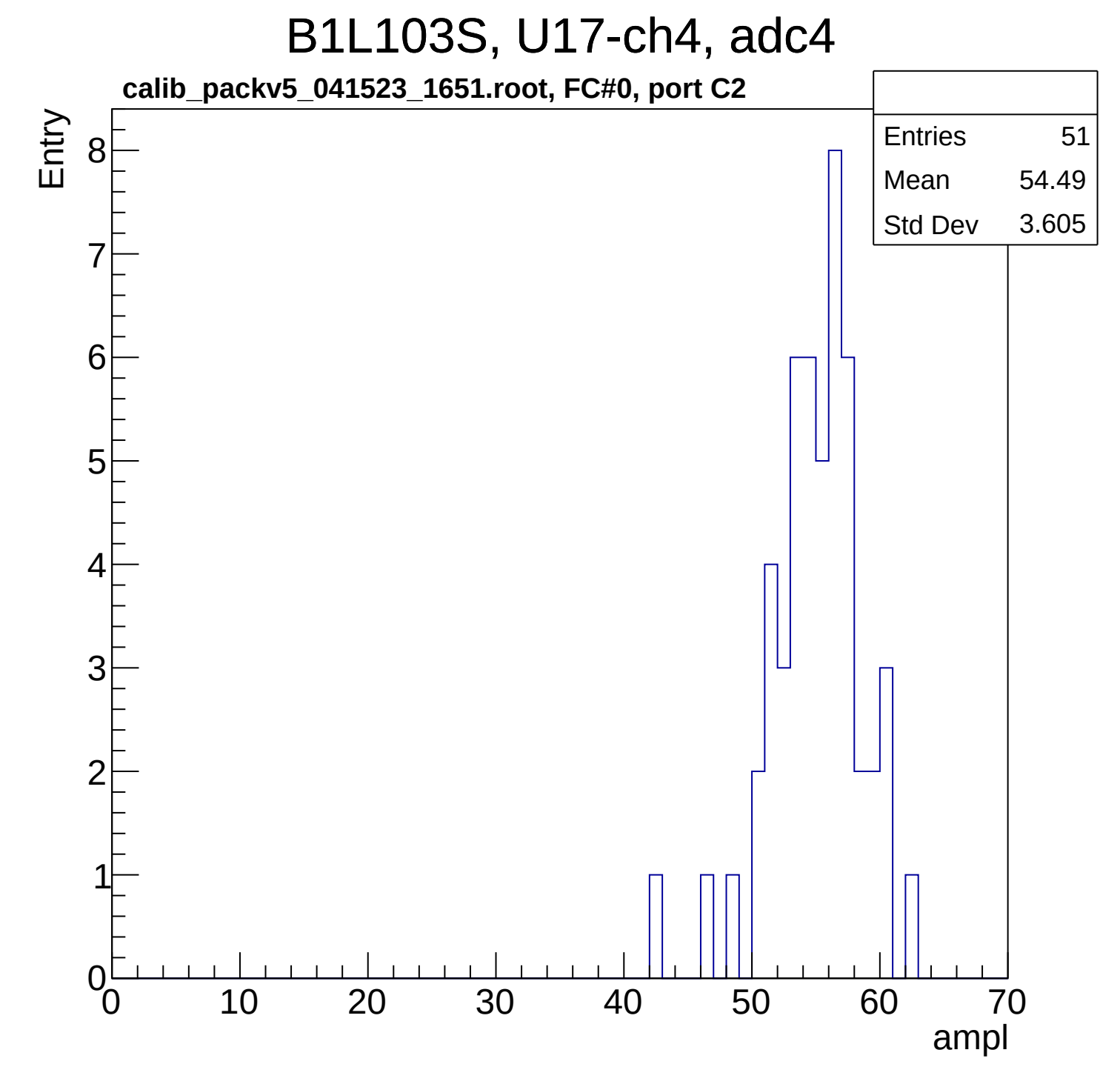
B1L103S, U17-ch4, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 54.49
Std Dev 3.605
Entry
ampl
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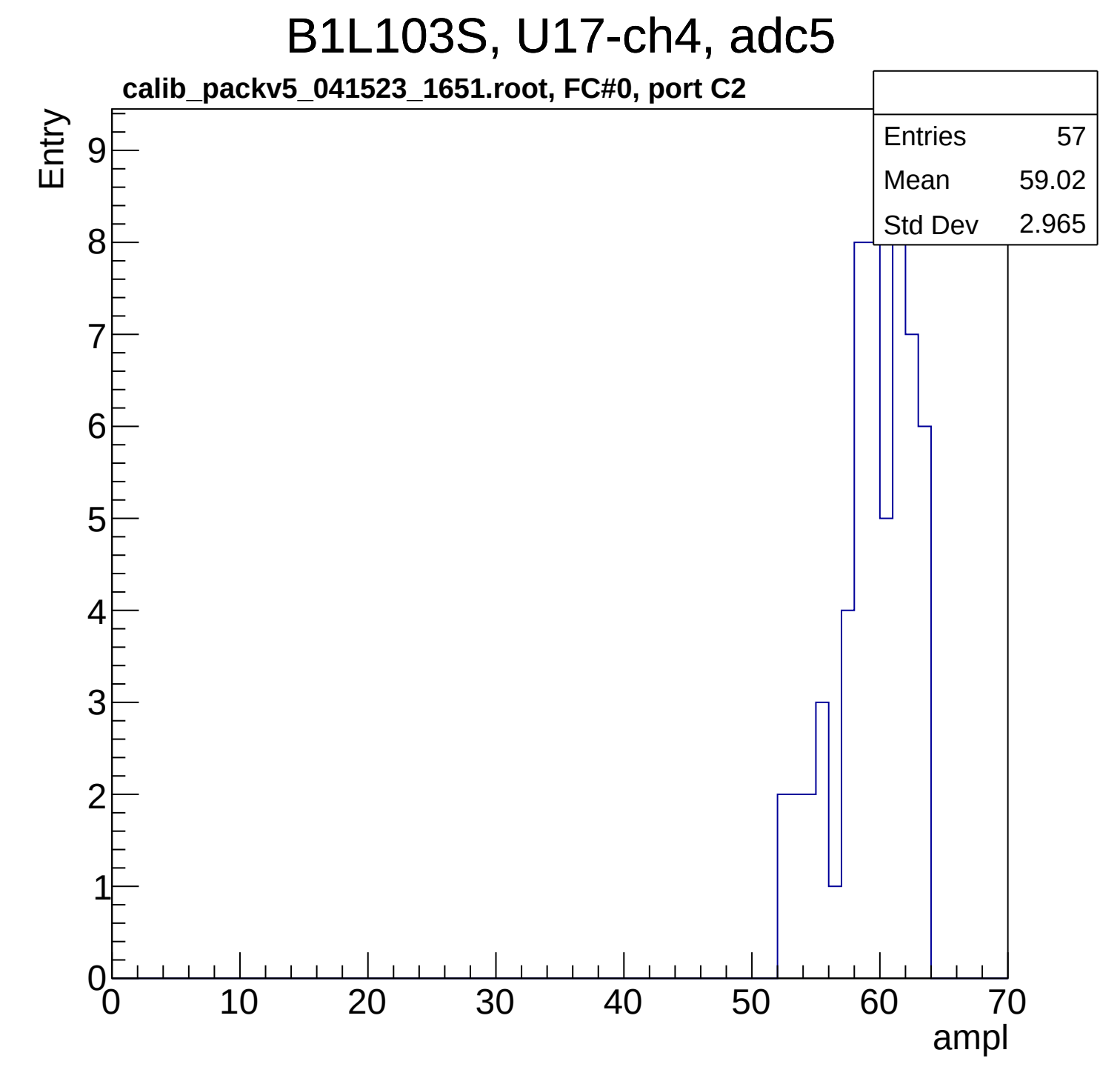
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U17-ch4, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 59.02
Std Dev 2.965
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
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20
30
40
50
60
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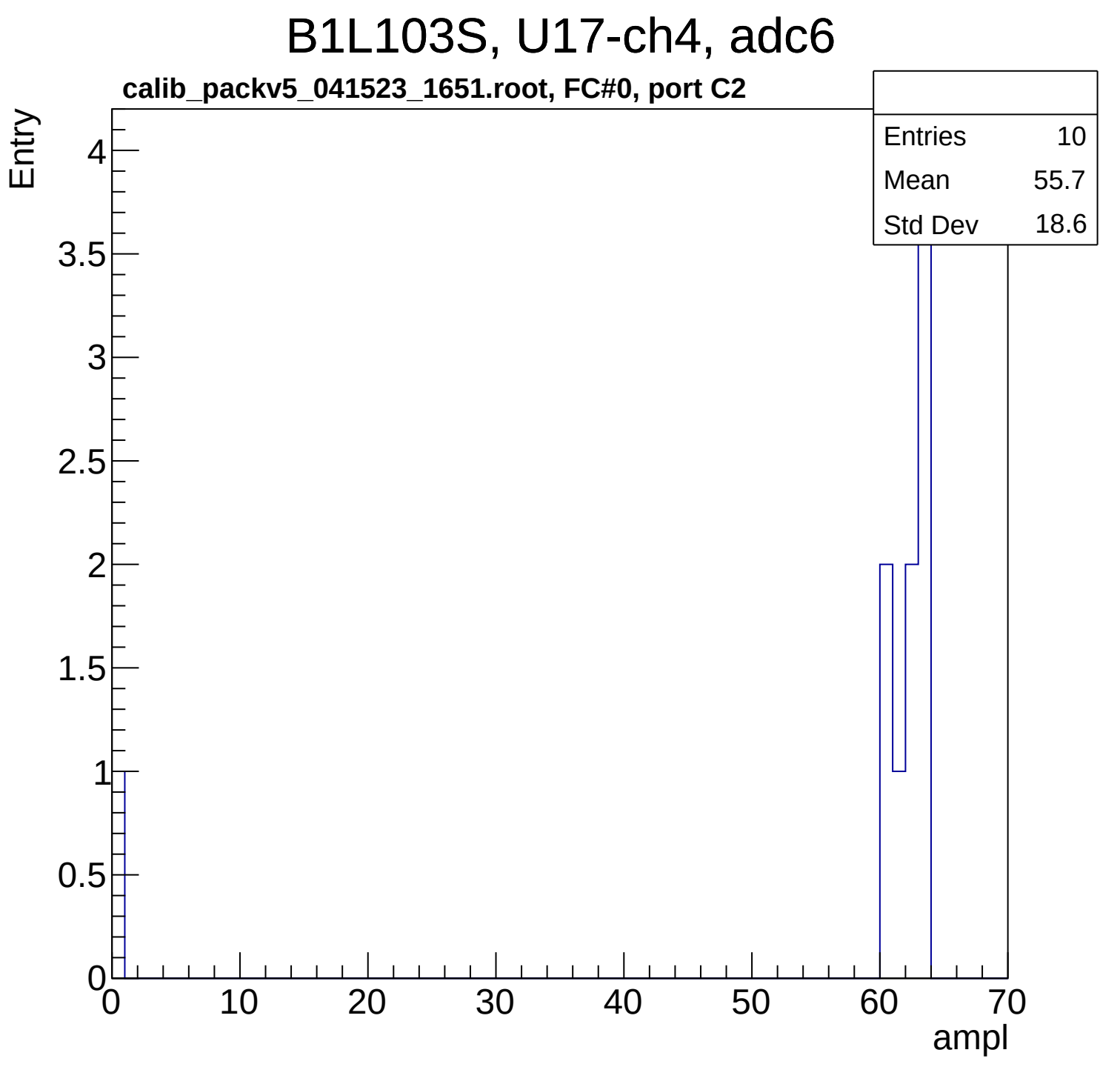
B1L103S, U17-ch4, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 55.7
Std Dev 18.6
Entry
ampl
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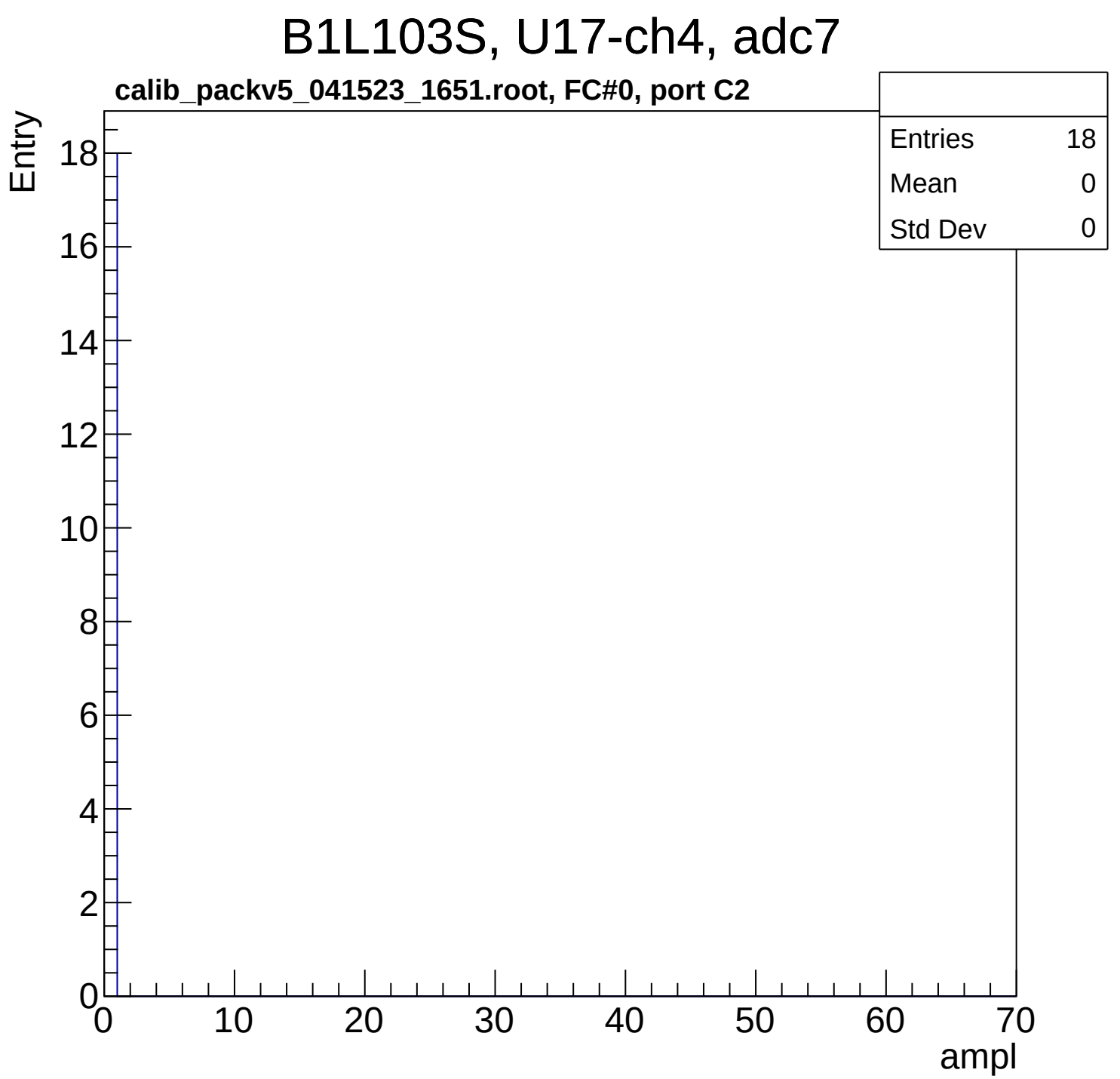
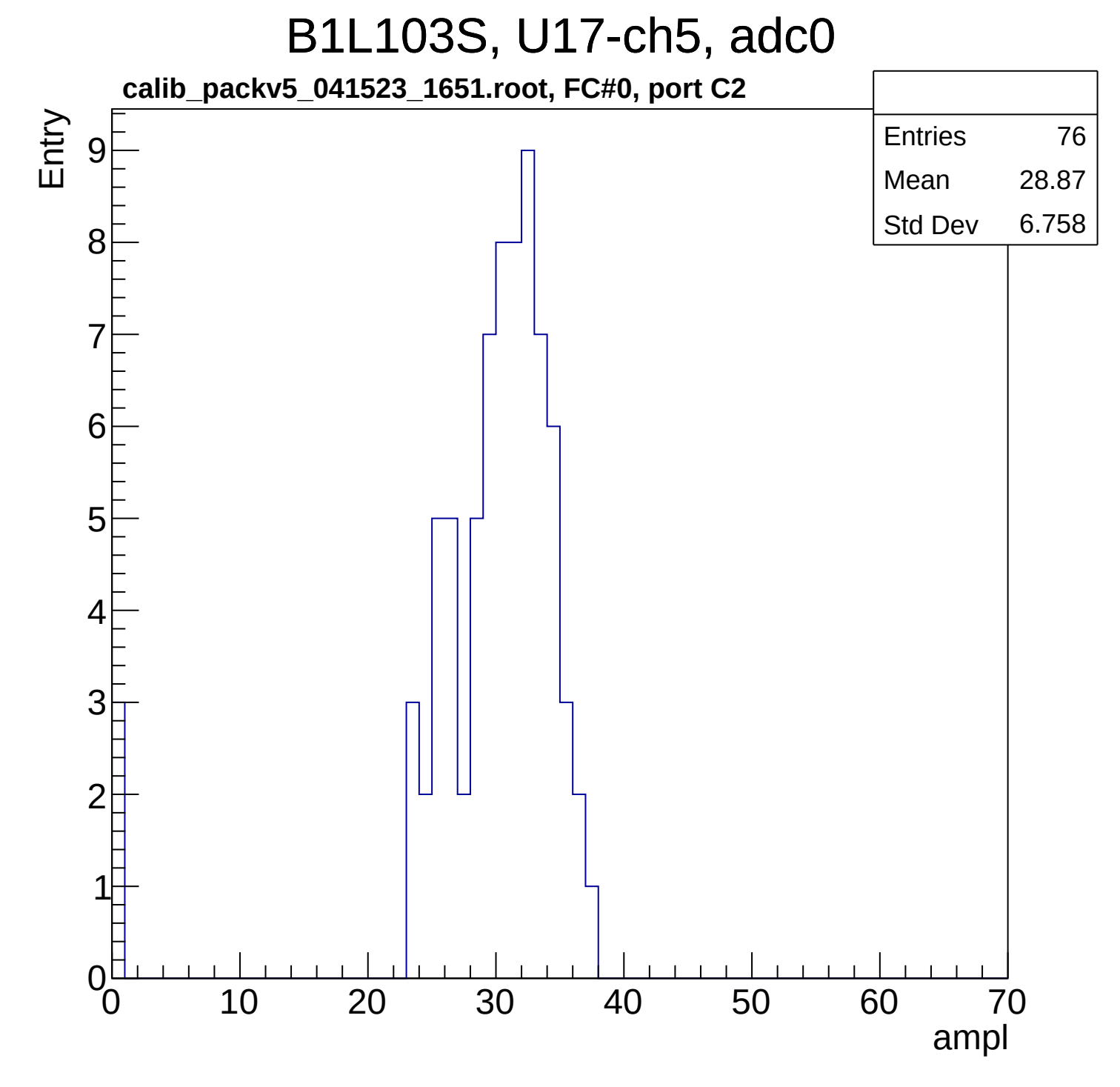
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U17-ch4, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch5, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 28.87
Std Dev 6.758
Entry
ampl
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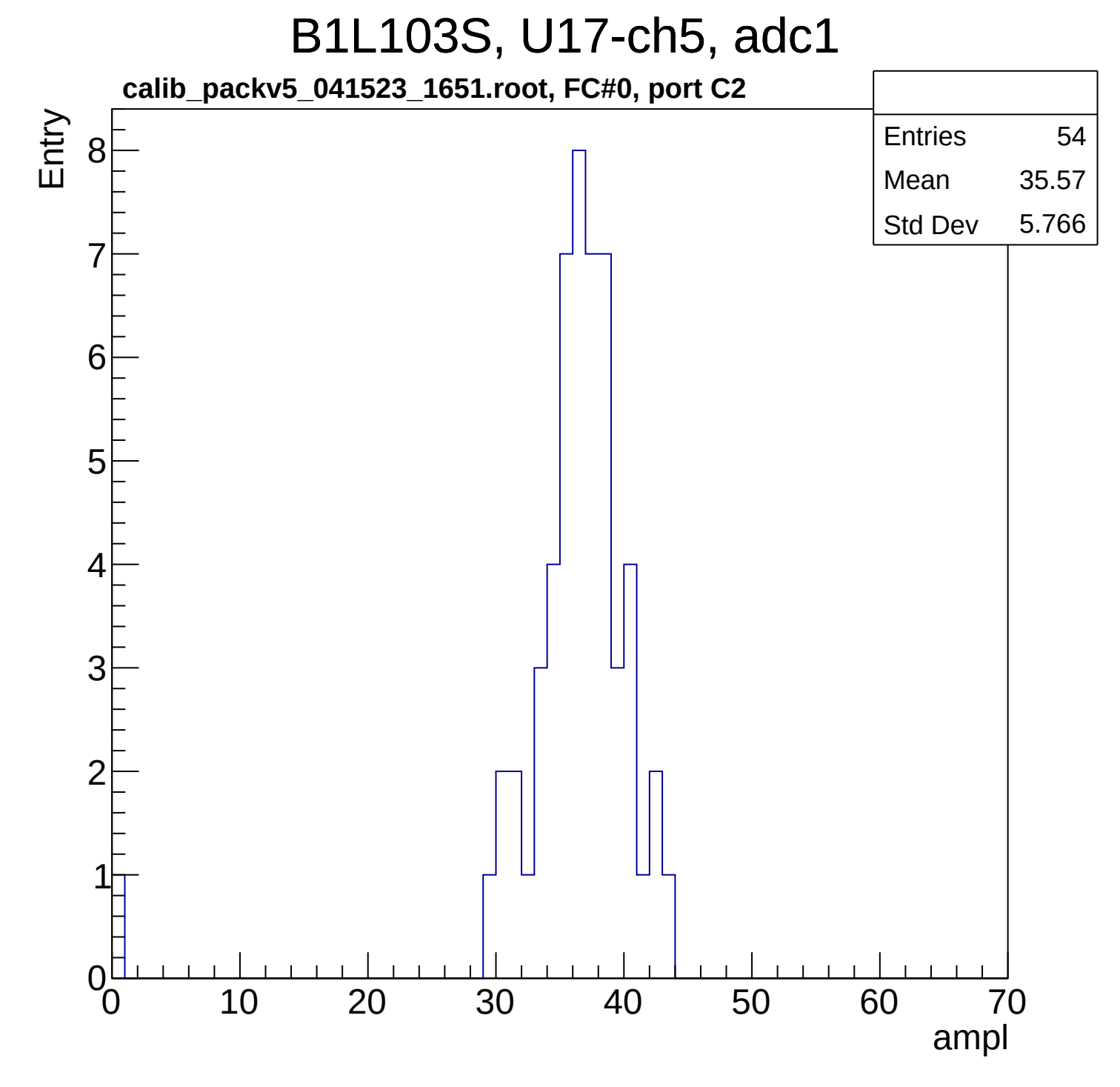
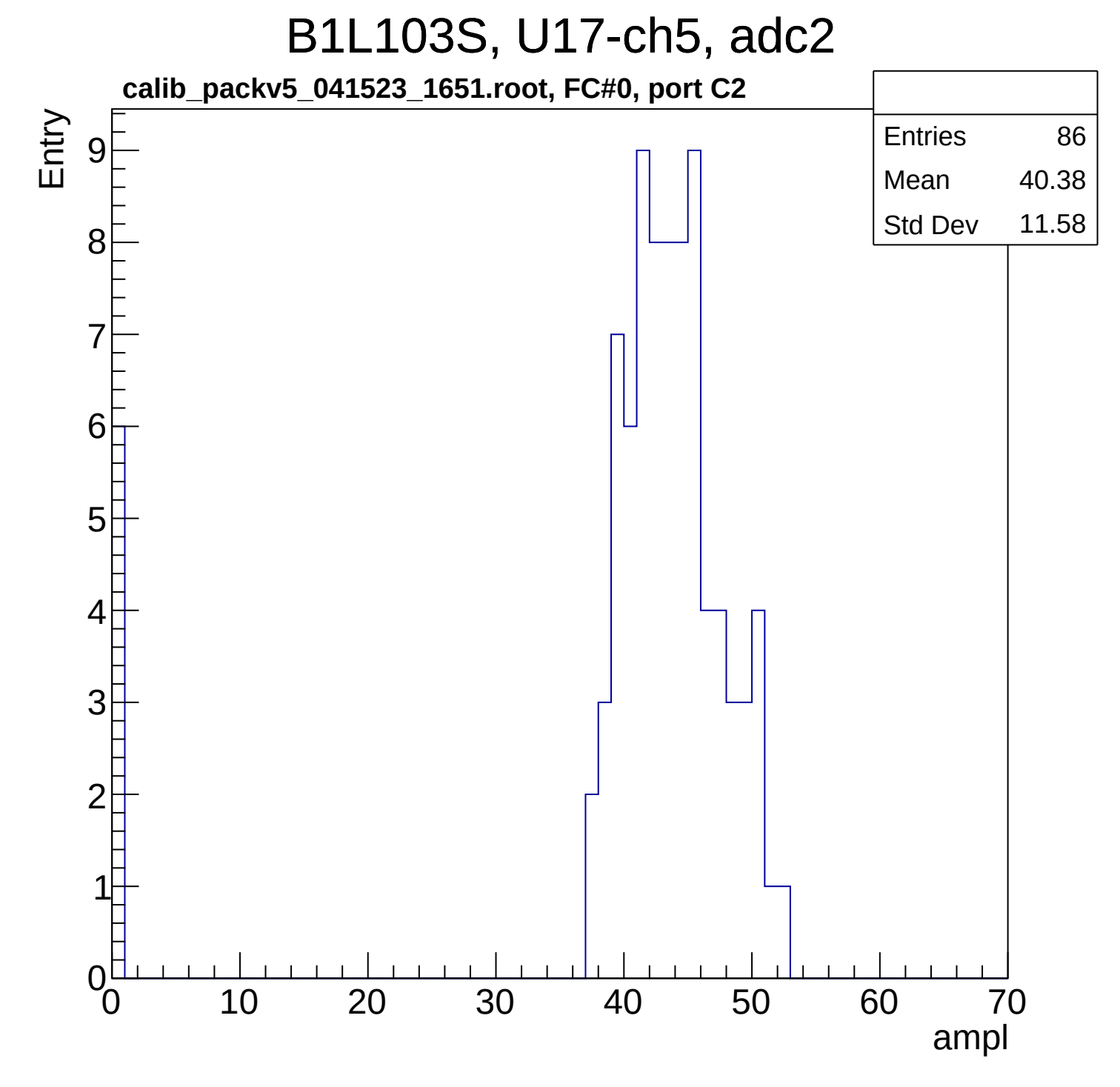
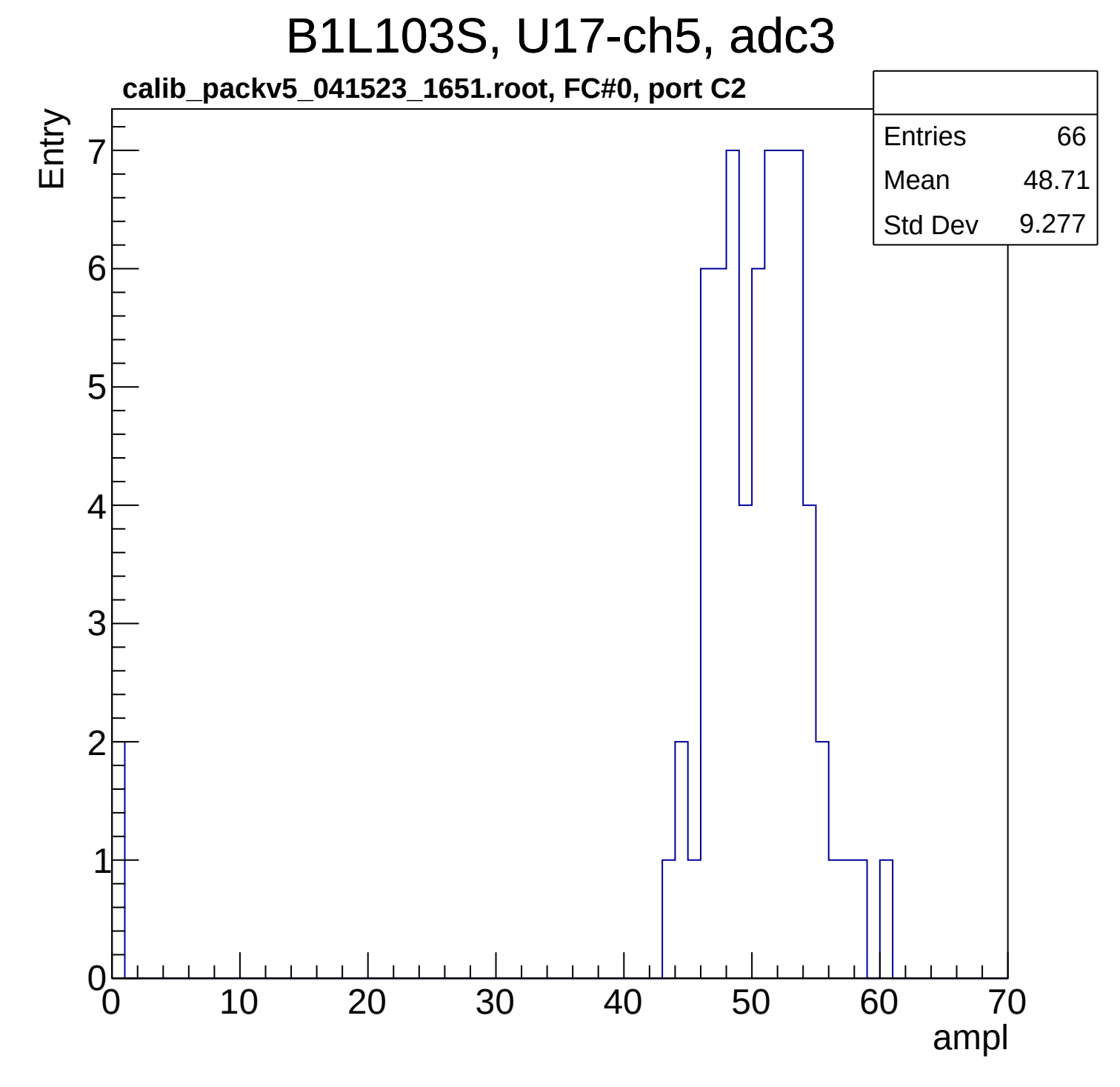
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U17-ch5, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 35.57
Std Dev 5.766
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U17-ch5, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 40.38
Std Dev 11.58
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U17-ch5, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 48.71
Std Dev 9.277
Entry
ampl
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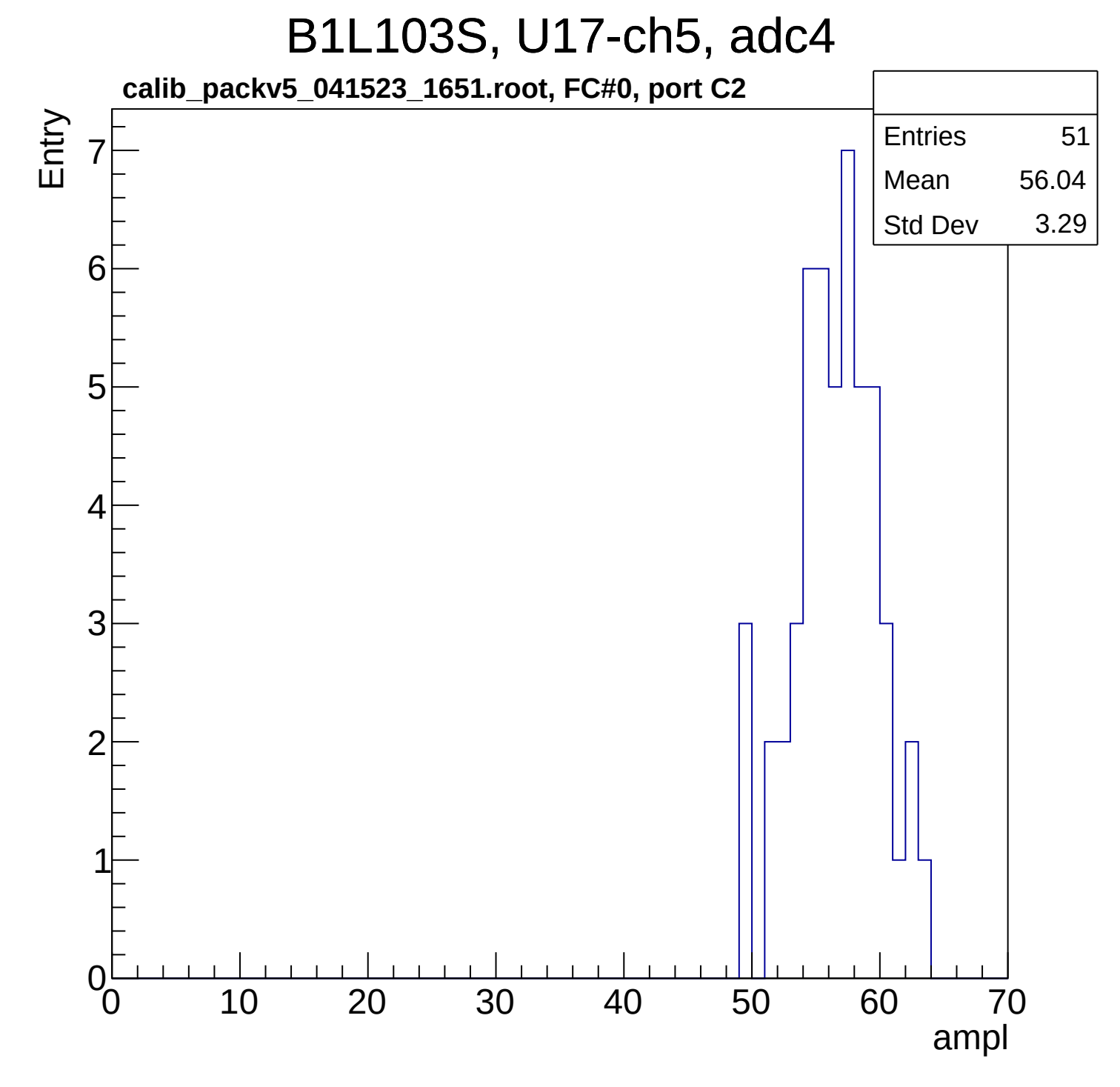
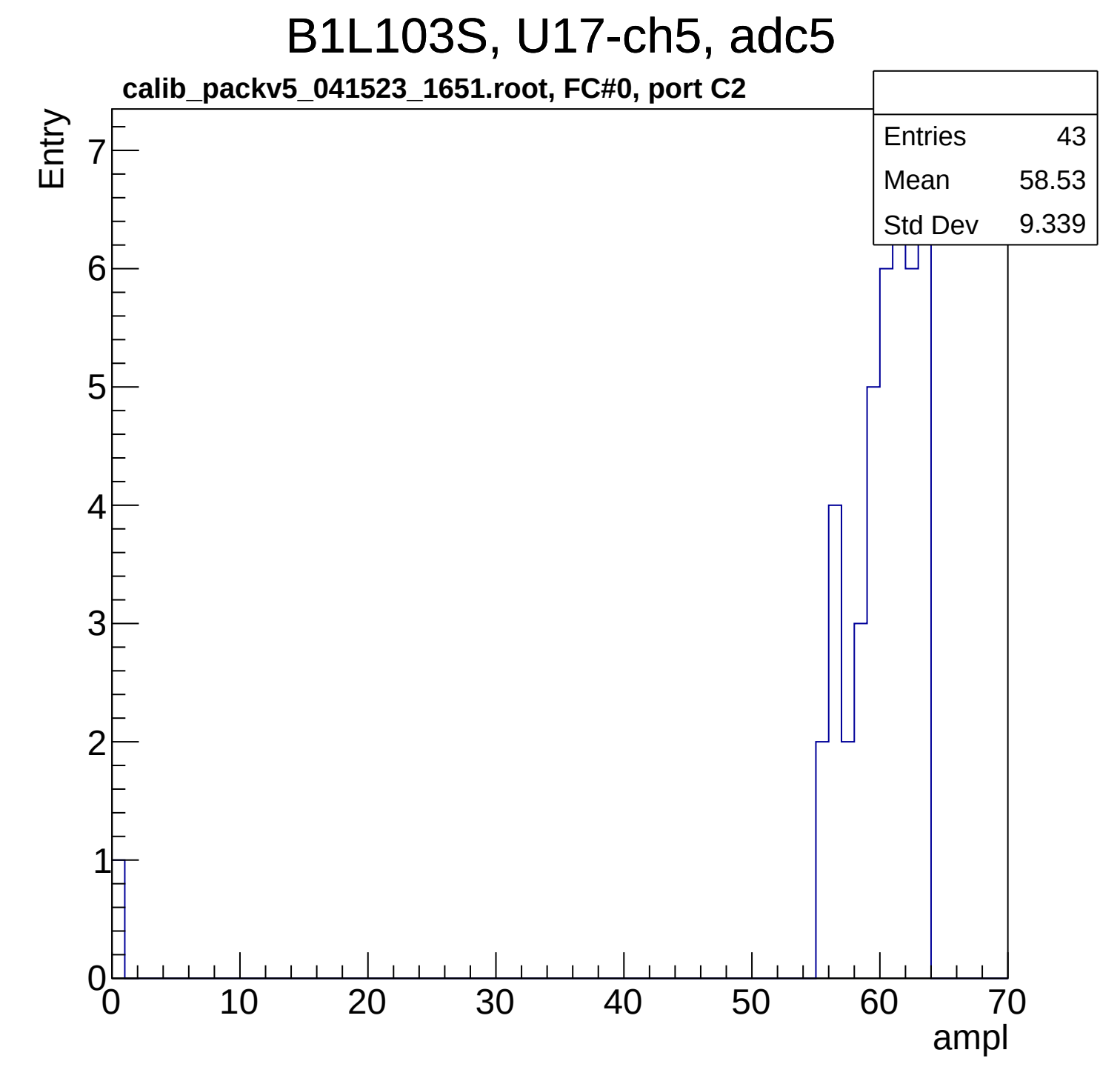
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U17-ch5, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 56.04
Std Dev 3.29
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U17-ch5, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 43
Mean 58.53
Std Dev 9.339
Entry
ampl
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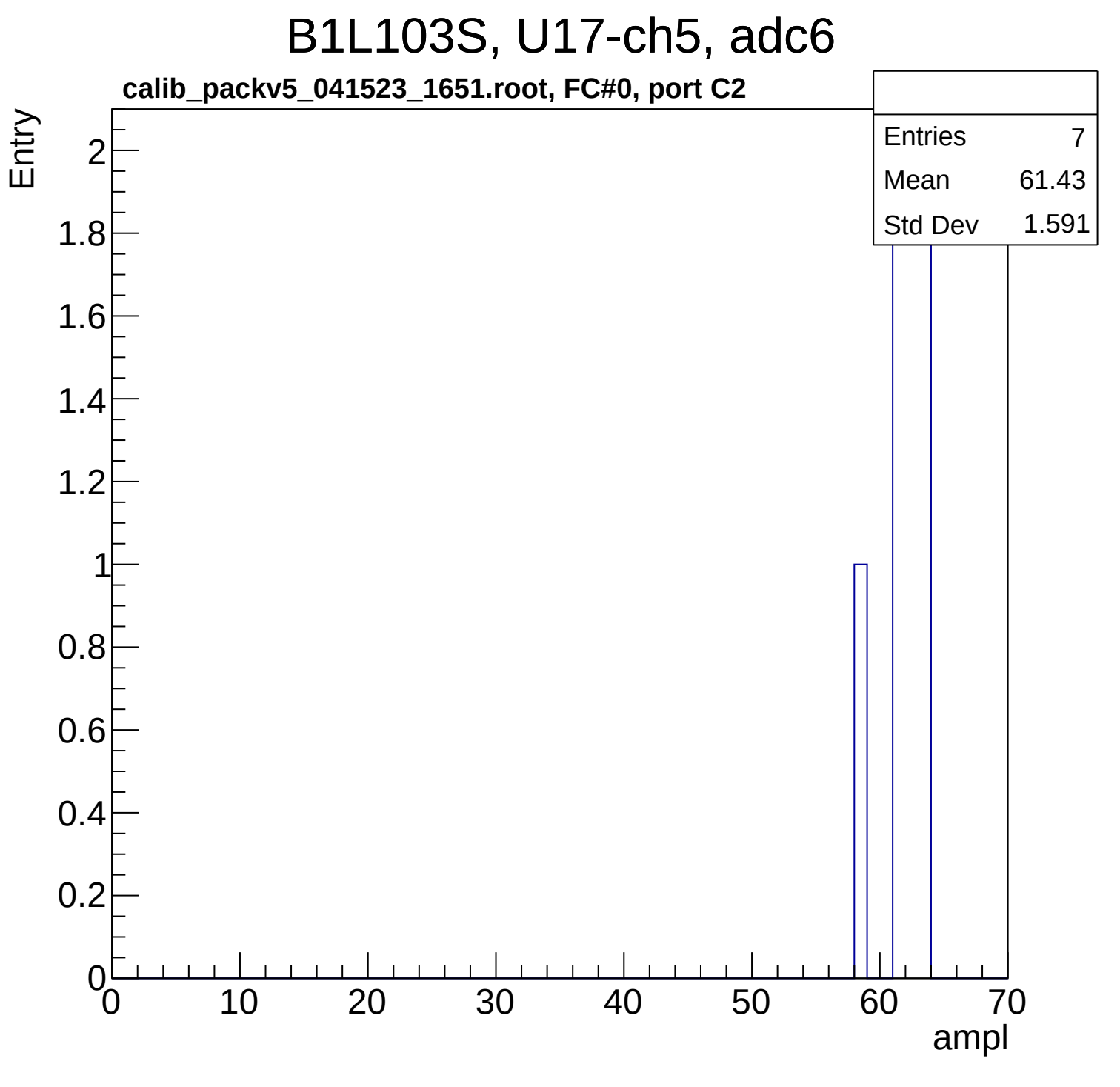
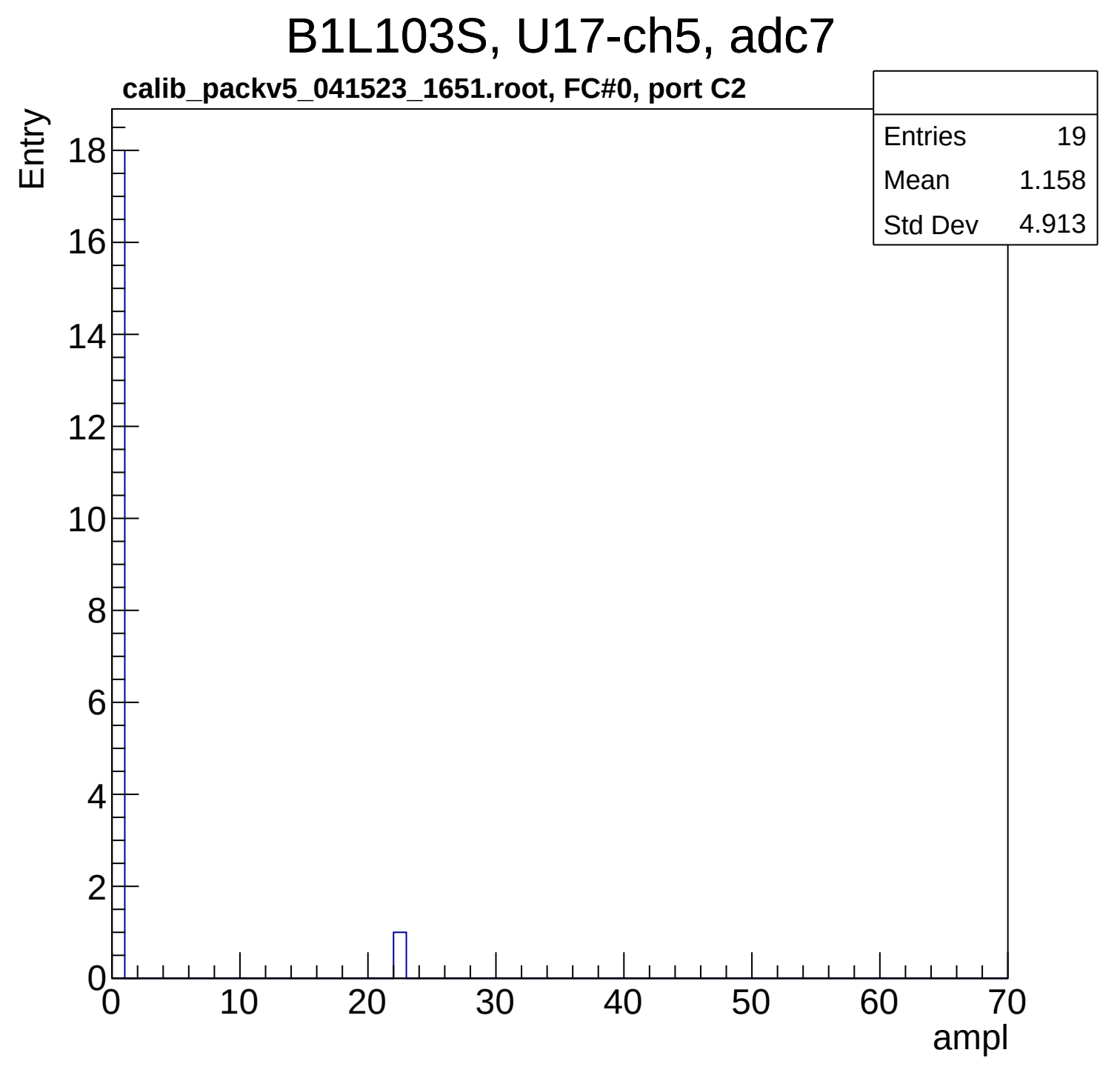
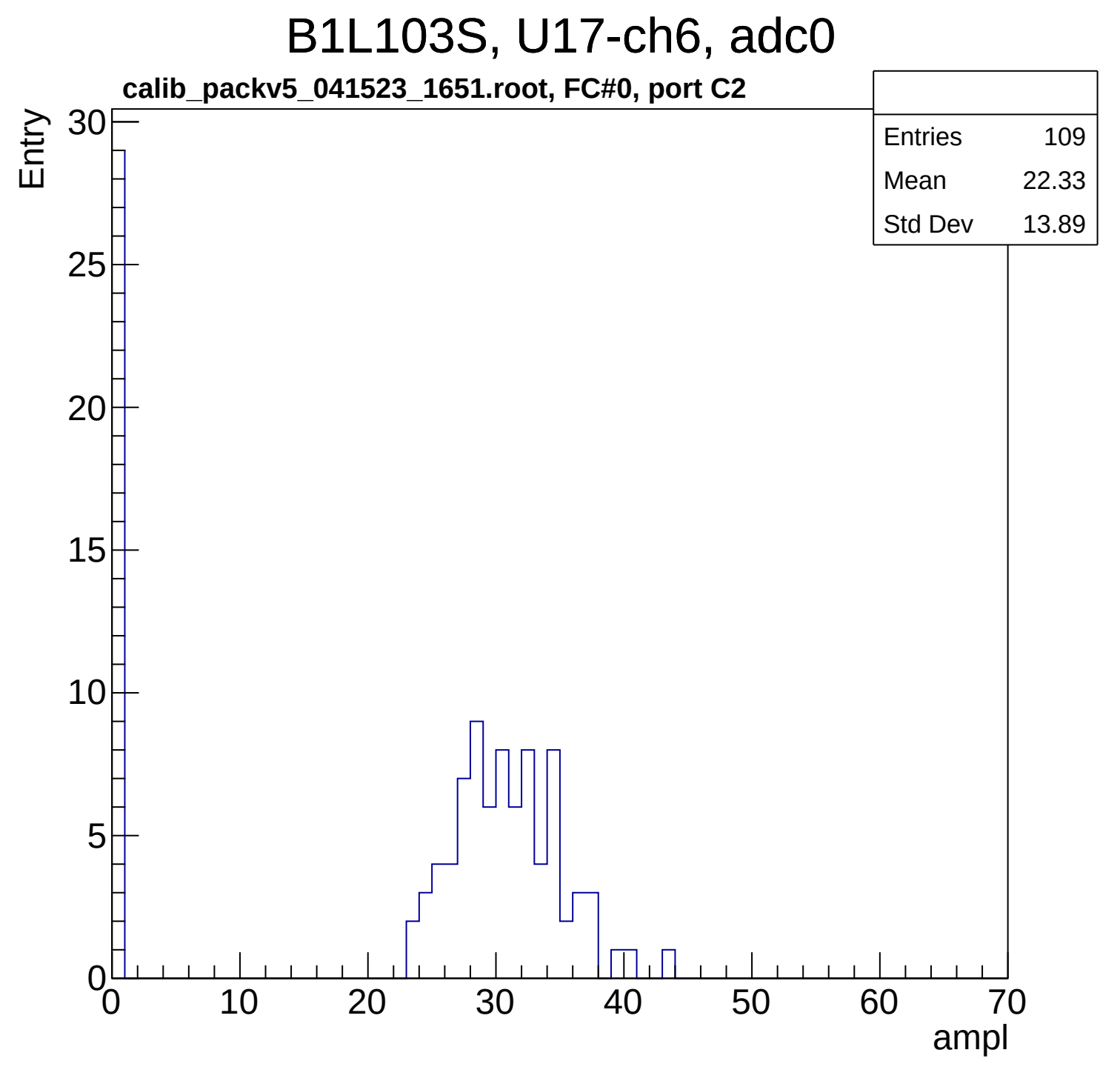
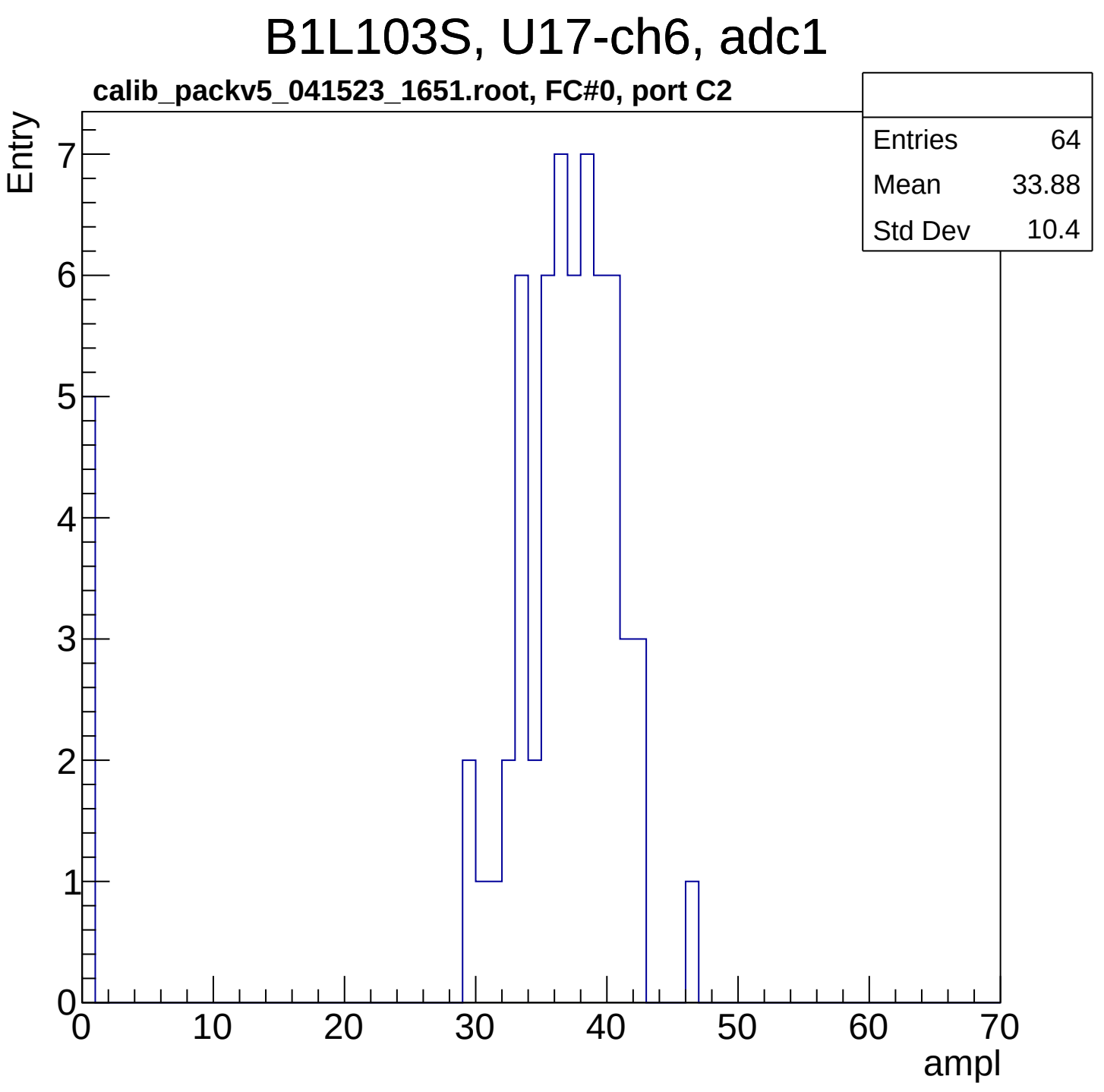
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U17-ch5, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 61.43
Std Dev 1.591
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U17-ch5, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.158
Std Dev 4.913
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70


B1L103S, U17-ch6, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 109
Mean 22.33
Std Dev 13.89
Entry
ampl
0
5
10
15
20
25
30
0
10
20
30
40
50
60
70


B1L103S, U17-ch6, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 33.88
Std Dev 10.4
Entry
ampl
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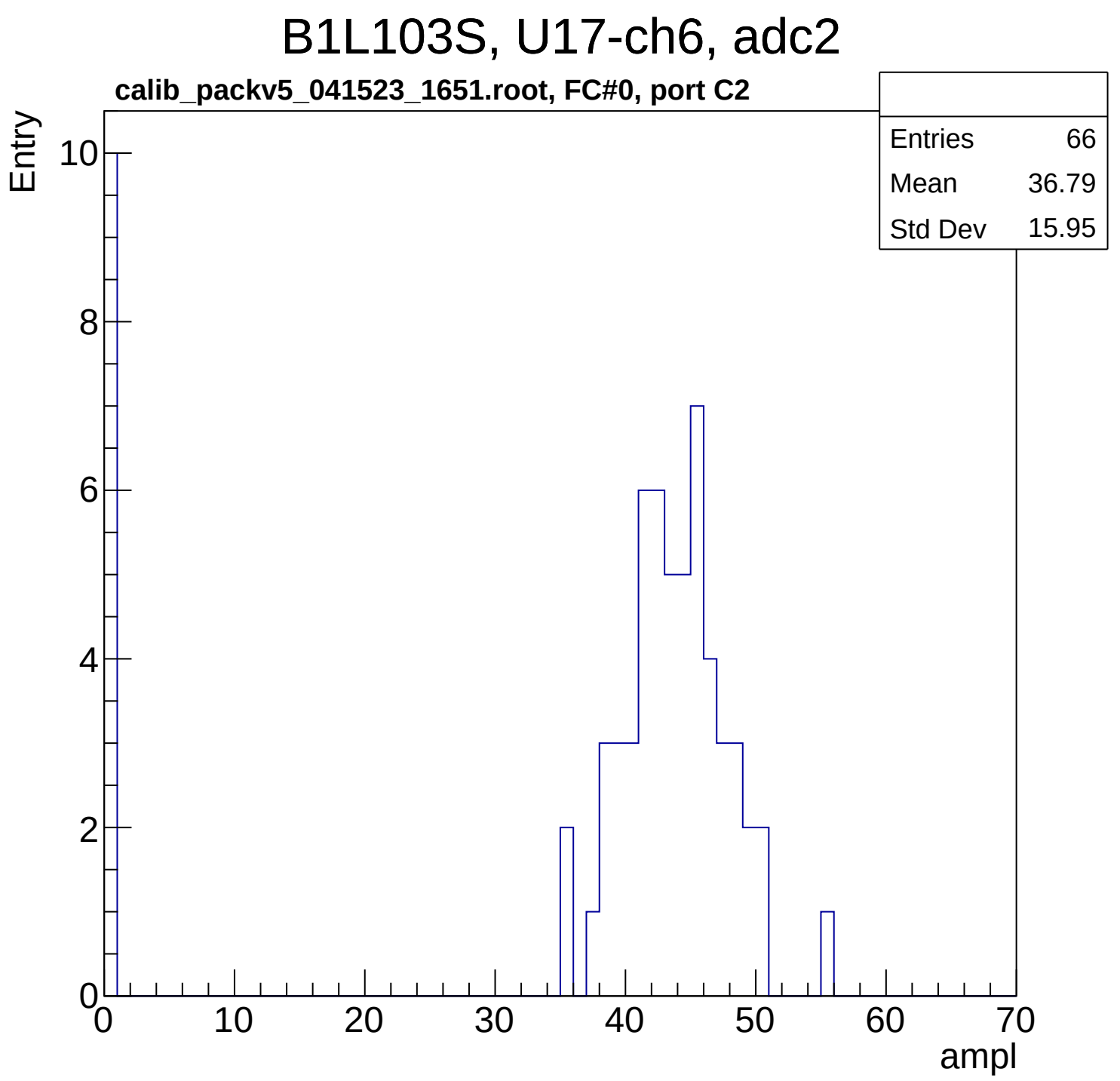
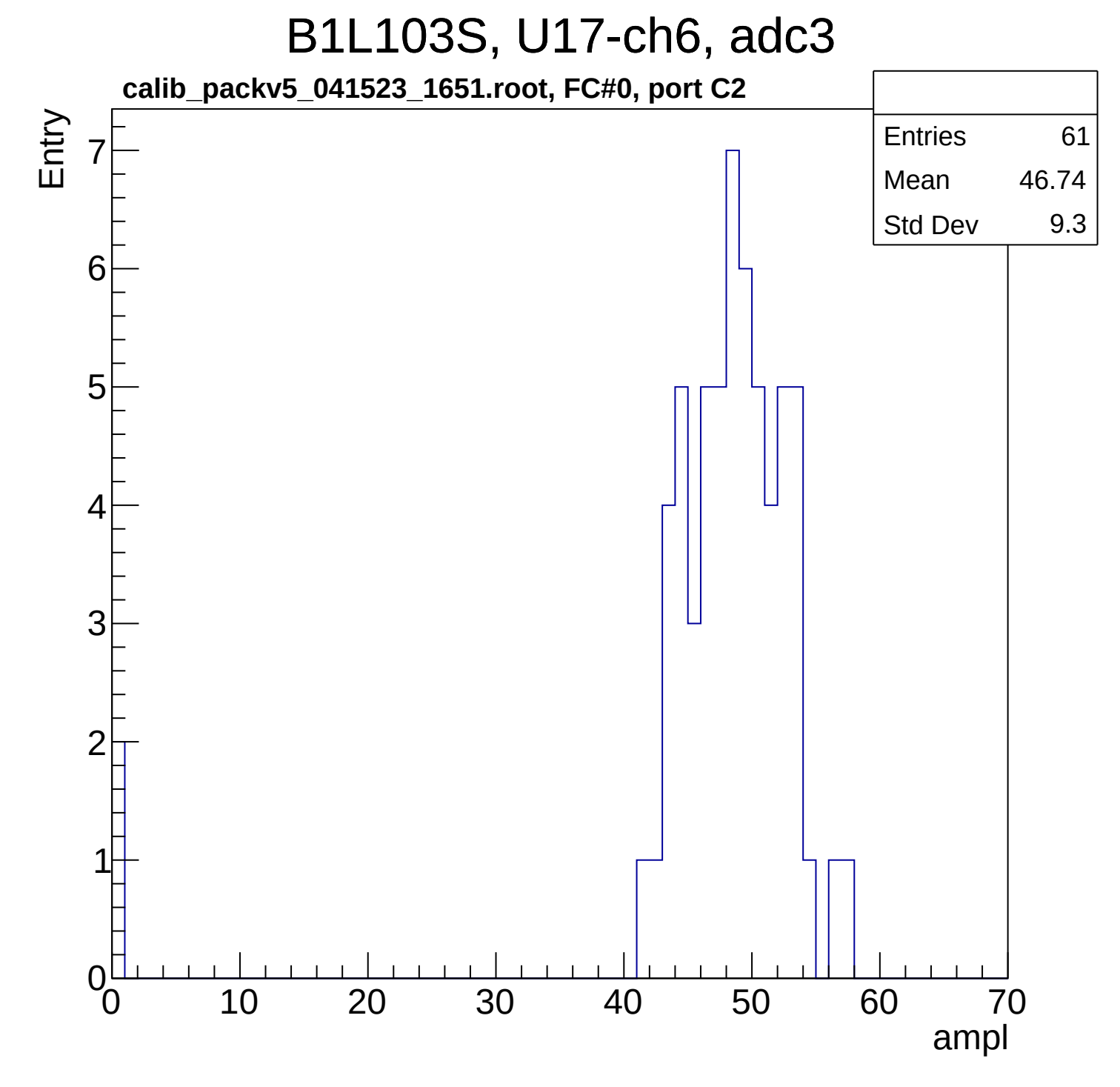
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U17-ch6, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 36.79
Std Dev 15.95
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U17-ch6, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 46.74
Std Dev 9.3
Entry
ampl
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1
2
3
4
5
6
7
0
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20
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40
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60
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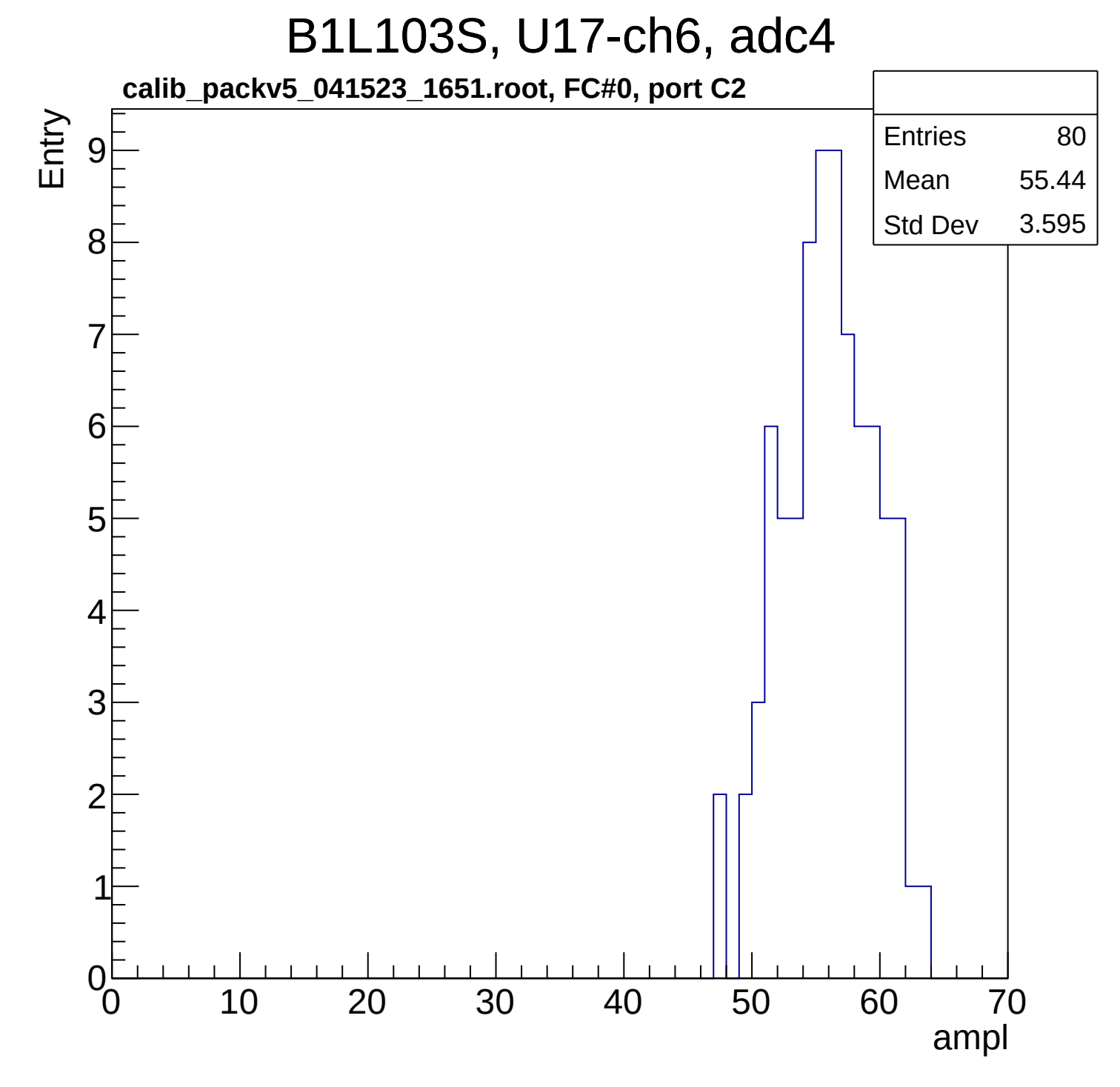
B1L103S, U17-ch6, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 55.44
Std Dev 3.595
Entry
ampl
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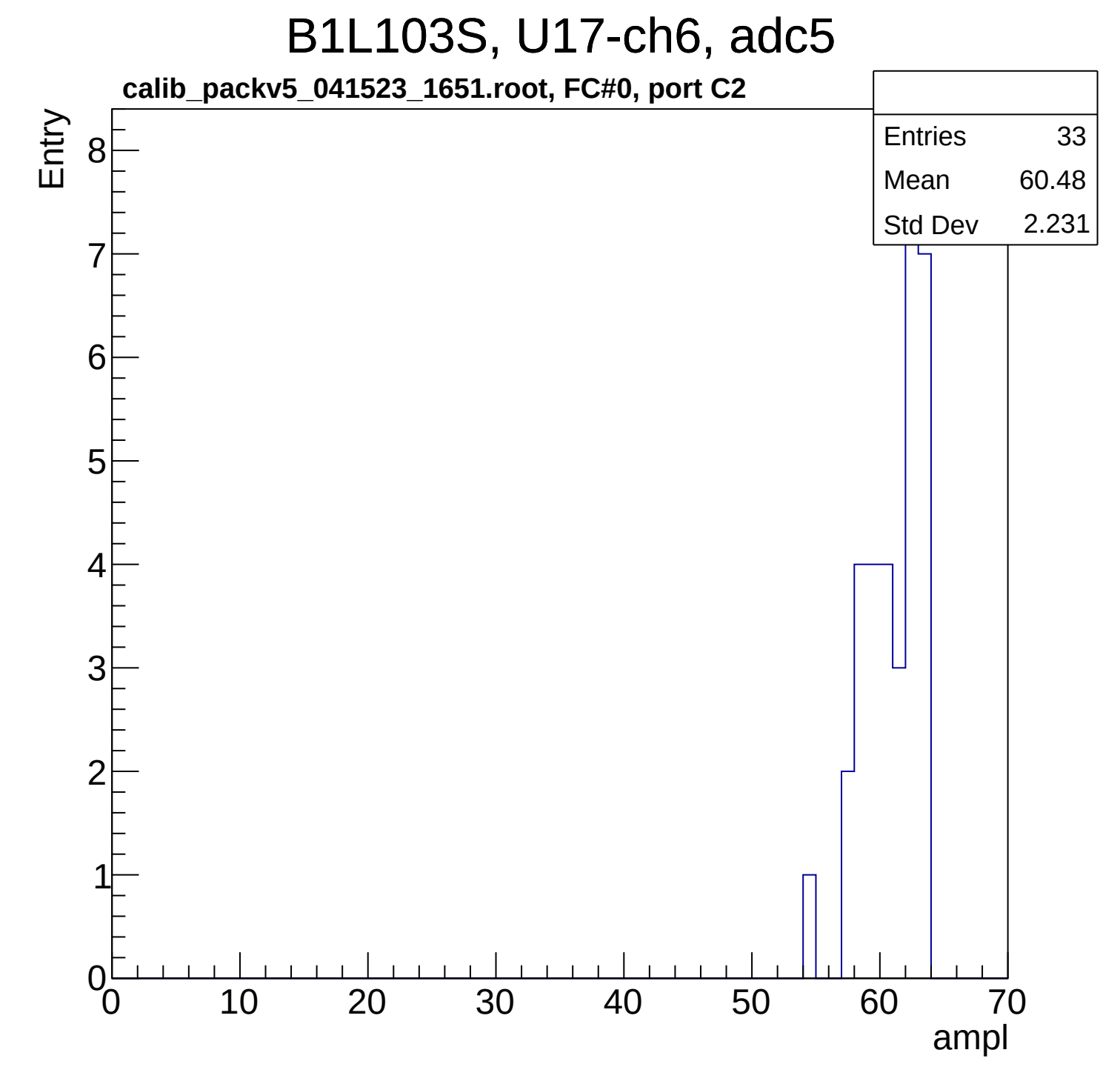
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U17-ch6, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 33
Mean 60.48
Std Dev 2.231
Entry
ampl
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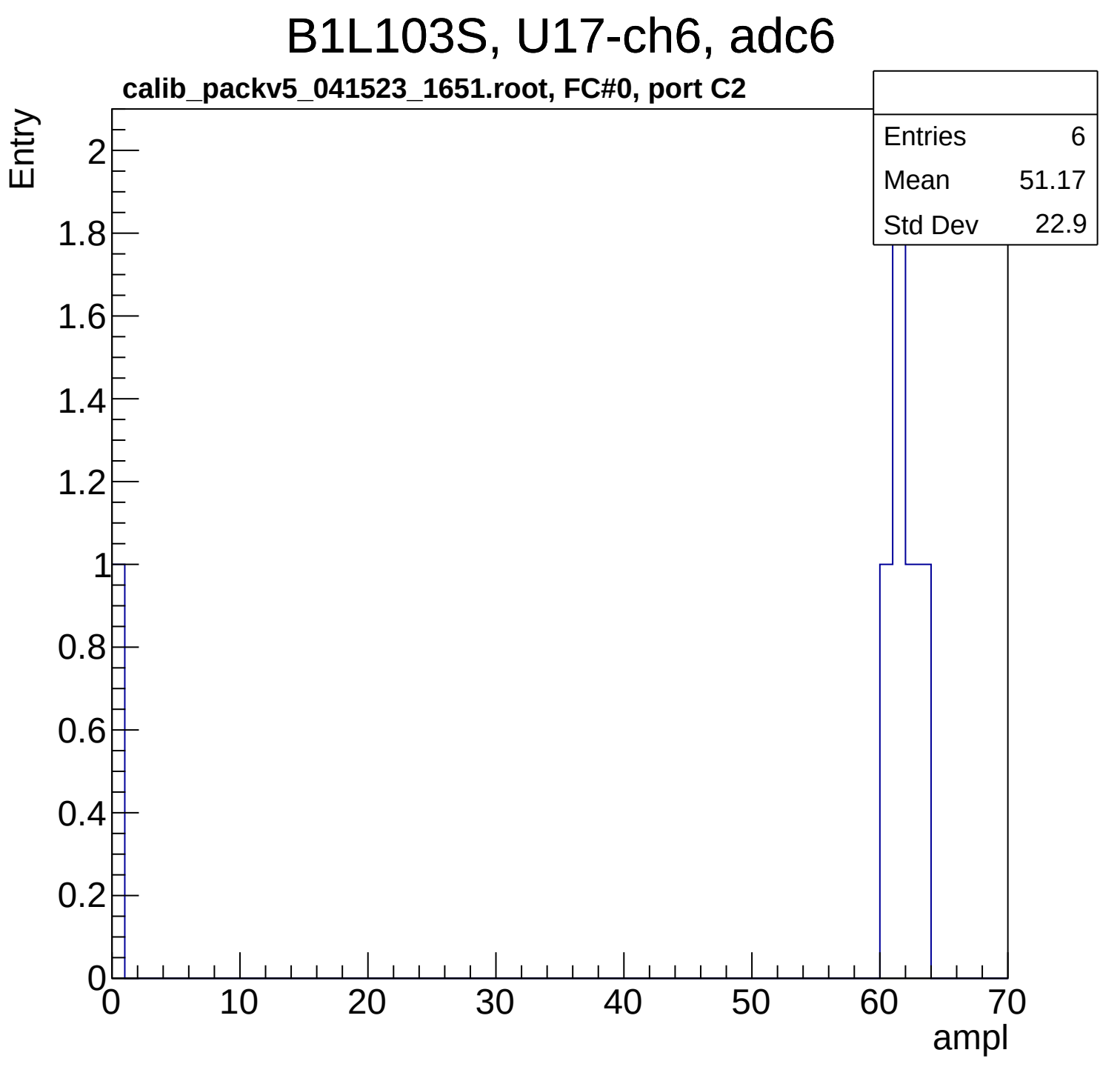
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U17-ch6, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 51.17
Std Dev 22.9
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
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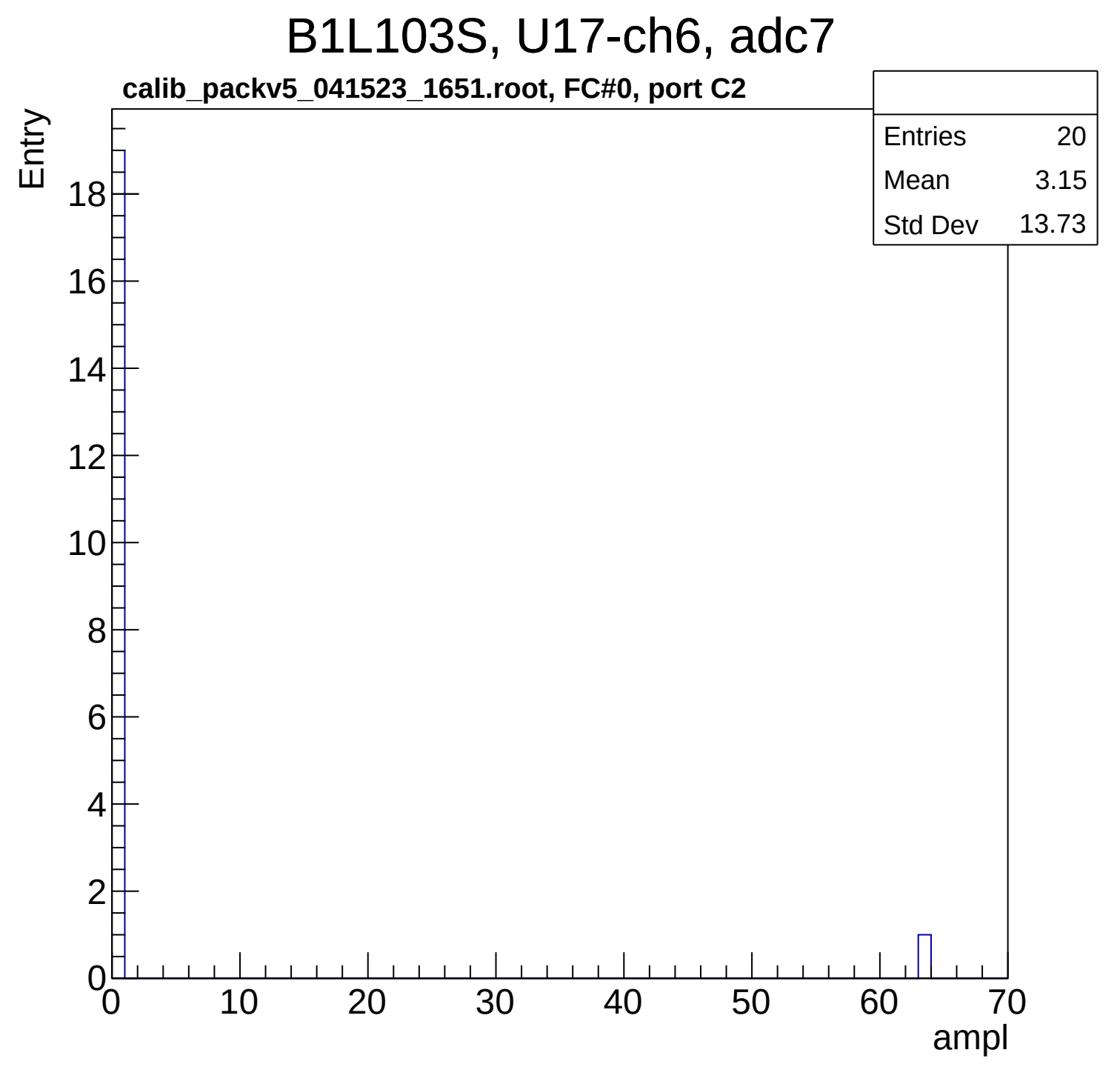
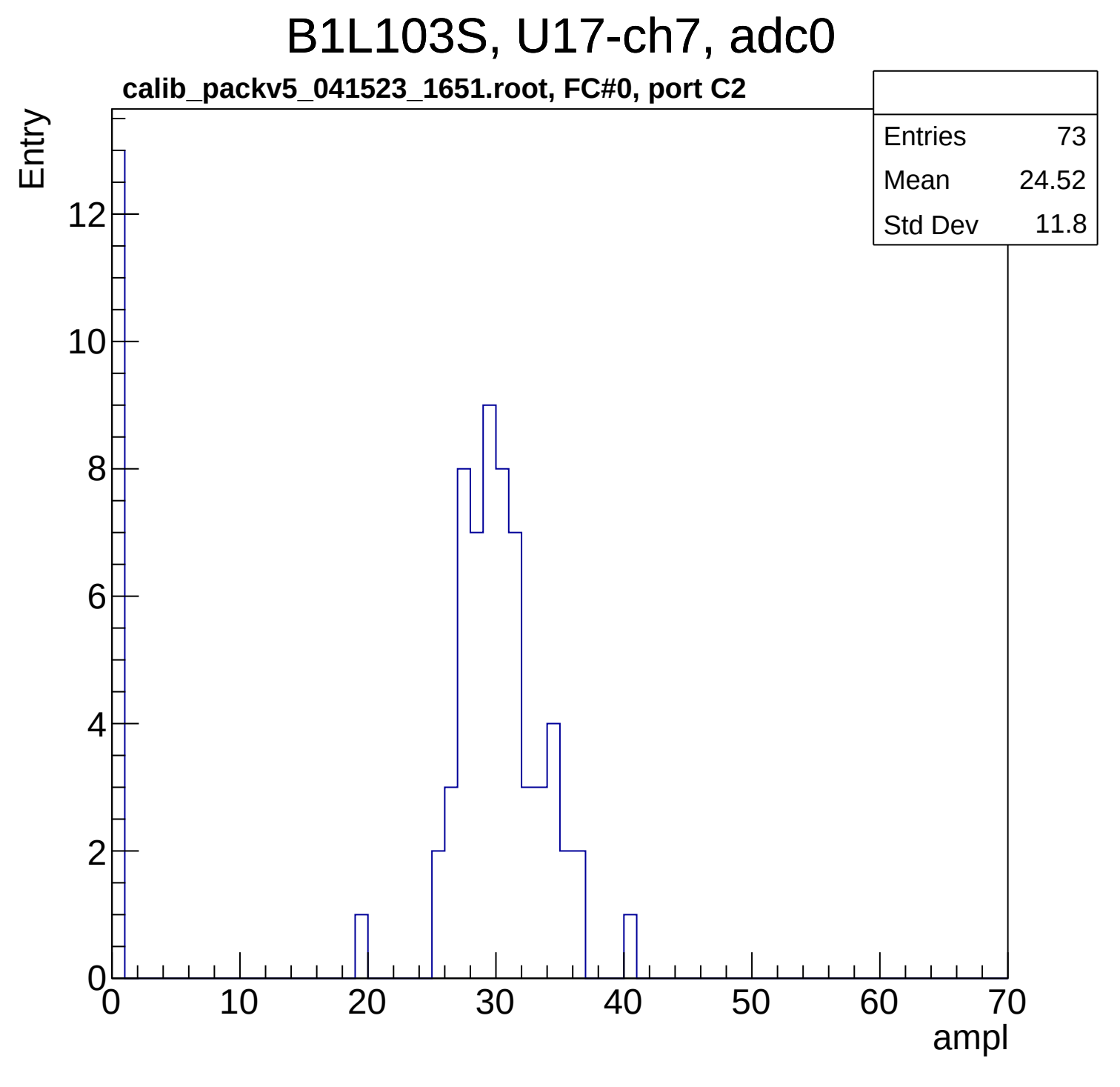

B1L103S, U17-ch6, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch7, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 24.52
Std Dev 11.8
Entry
ampl
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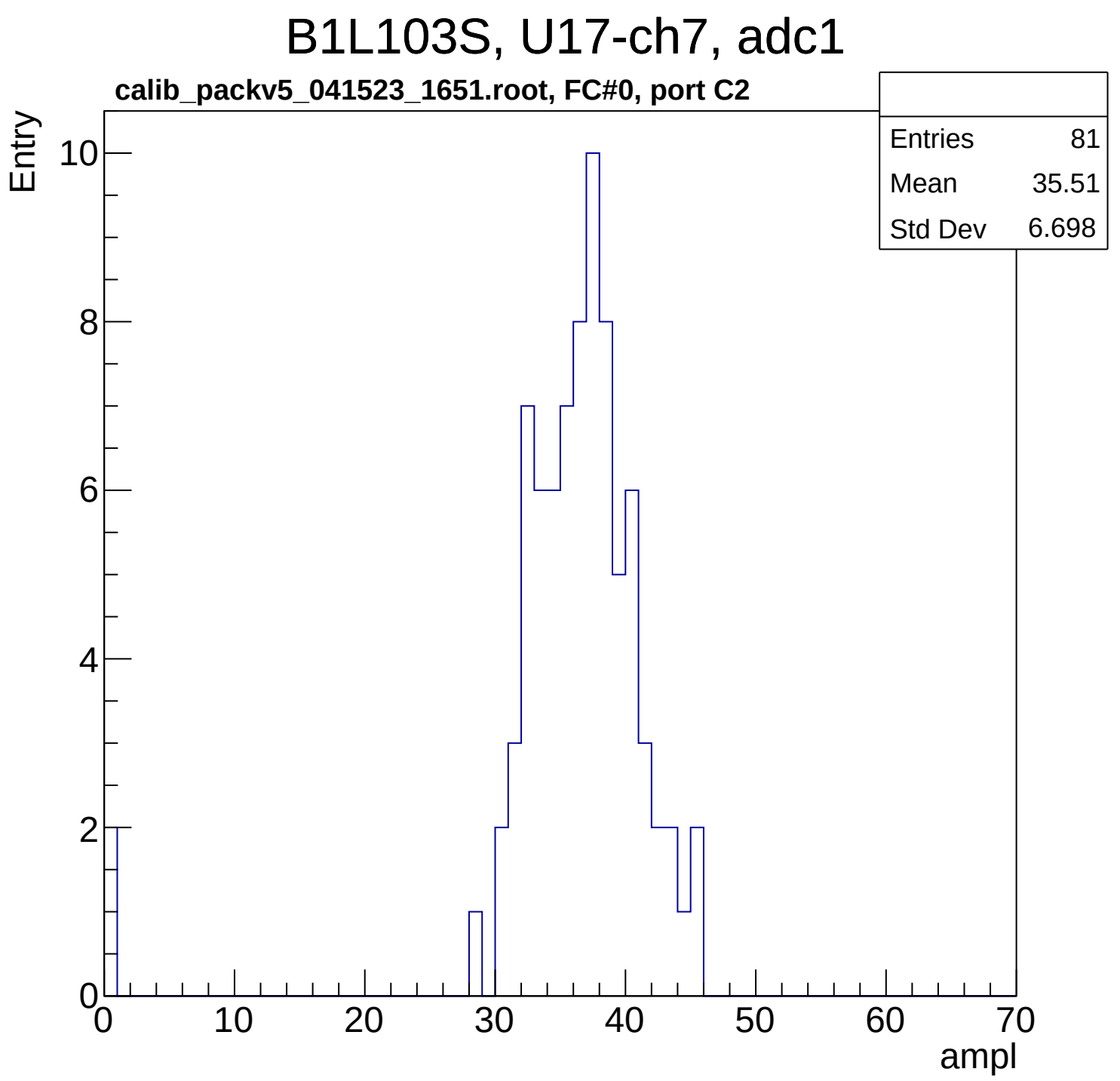
4
6
8
10
12
0
10
20
30
40
50
60
70


B1L103S, U17-ch7, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 35.51
Std Dev 6.698
Entry
ampl
0
2
4
6
8
10
0
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20
30
40
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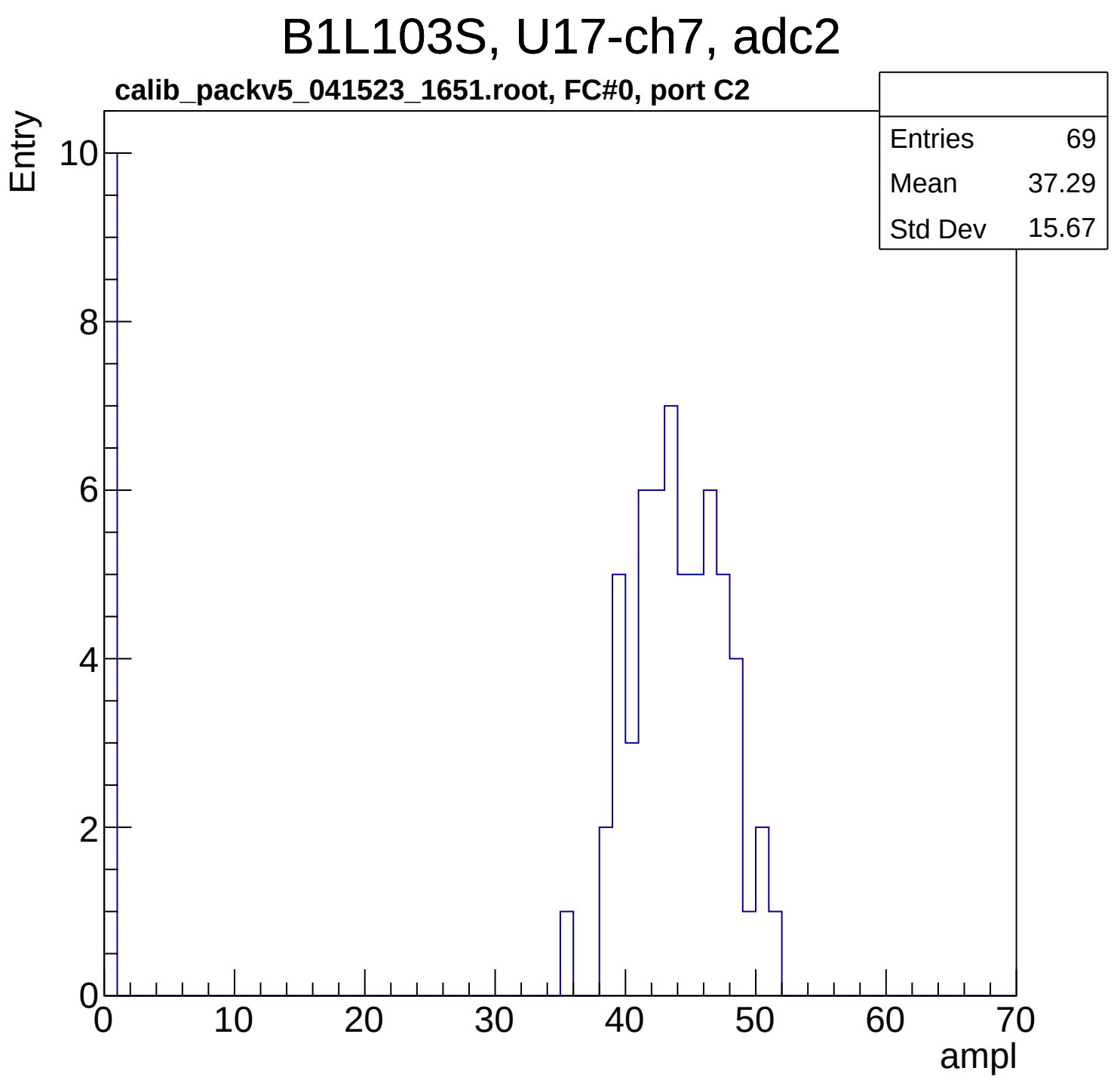
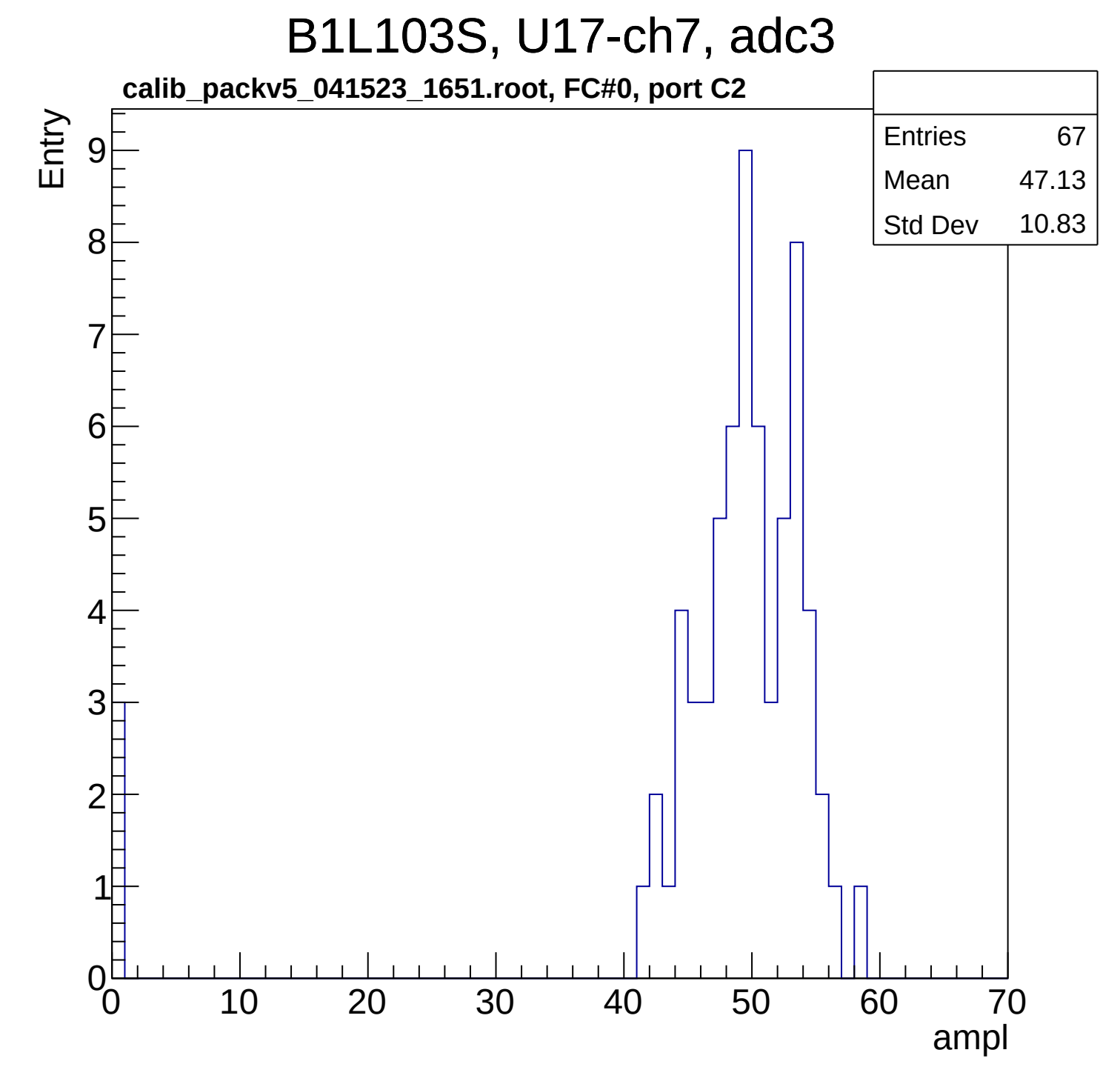
60
70


B1L103S, U17-ch7, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 37.29
Std Dev 15.67
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch7, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 47.13
Std Dev 10.83
Entry
ampl
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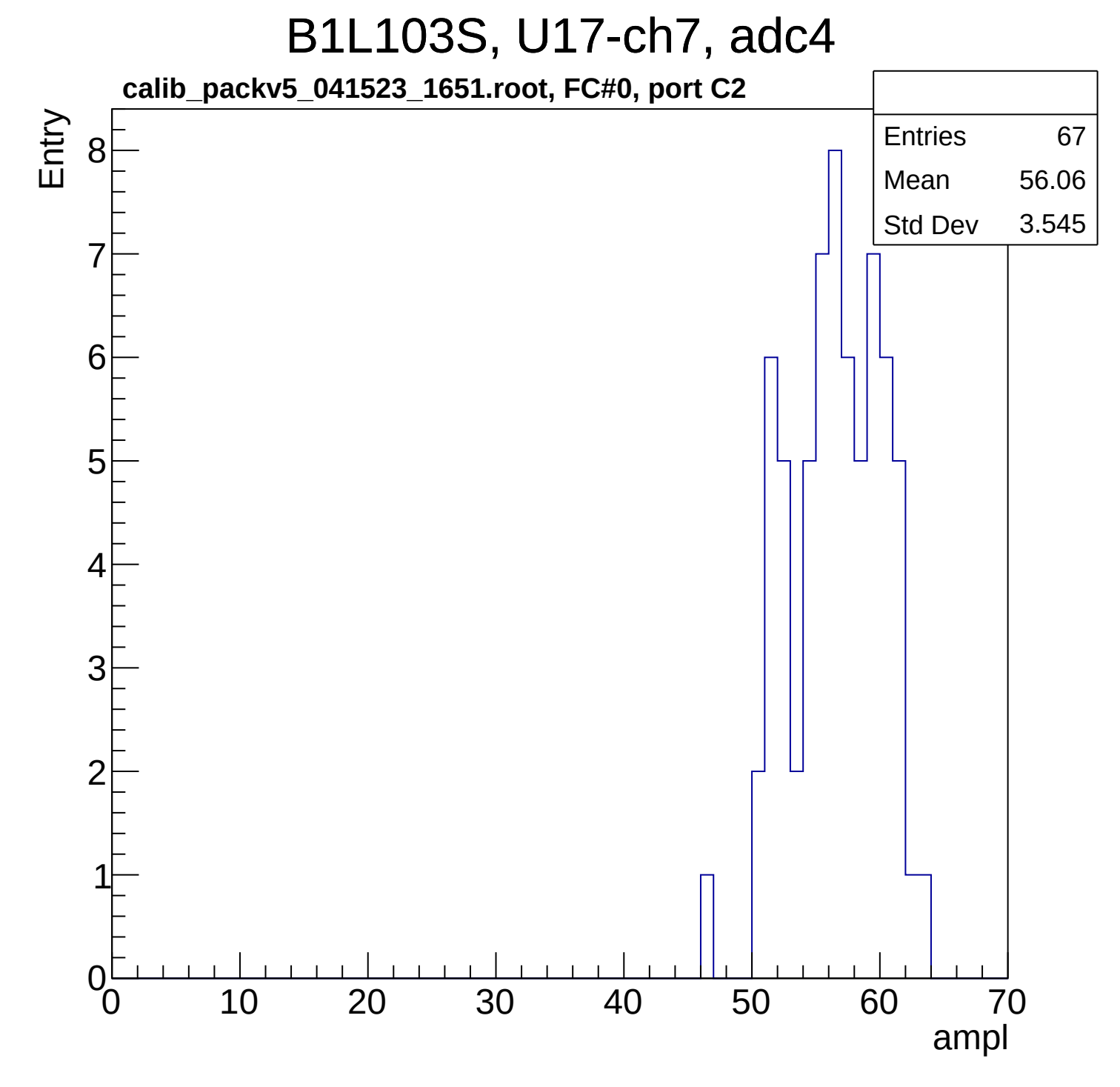
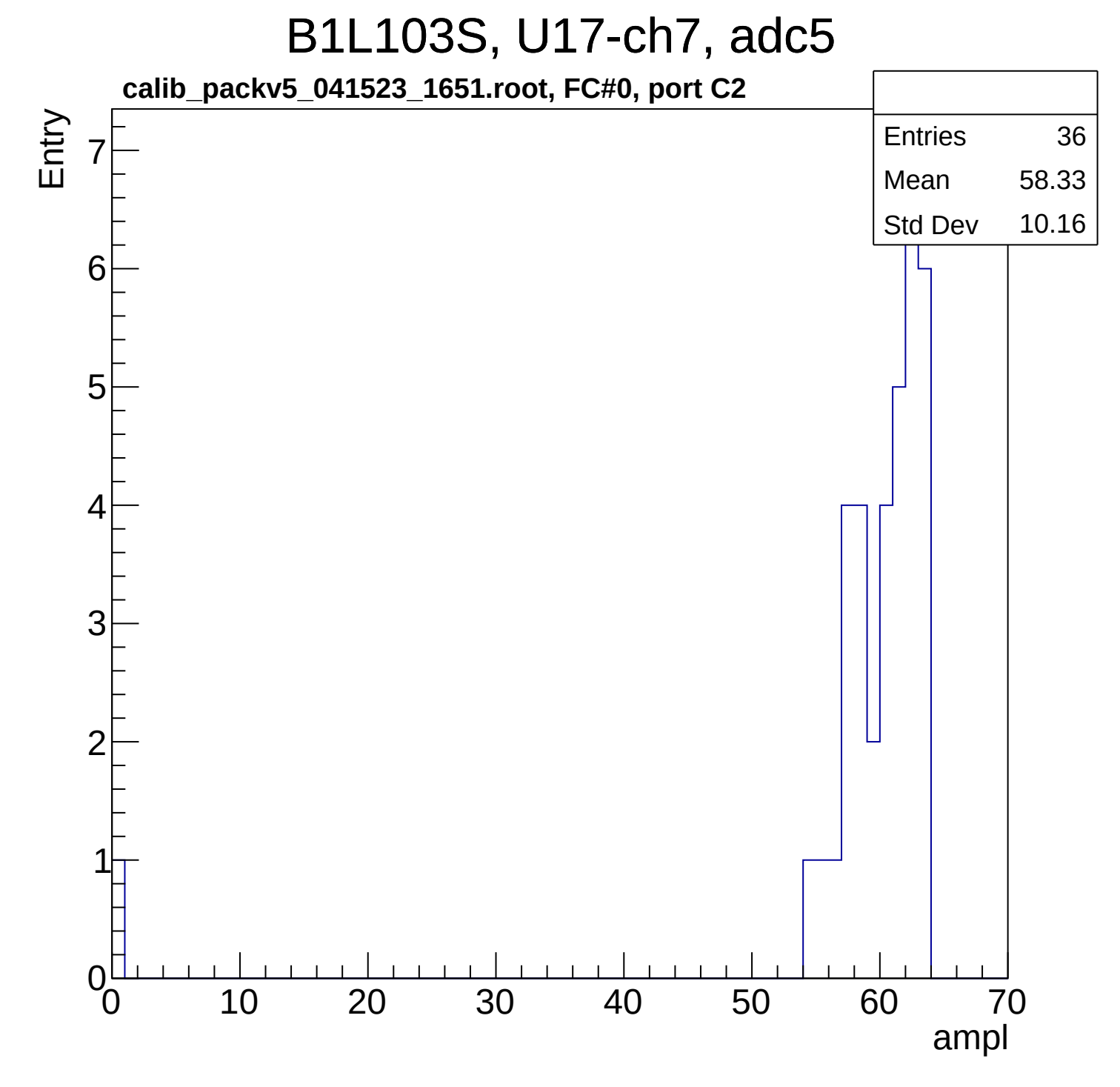
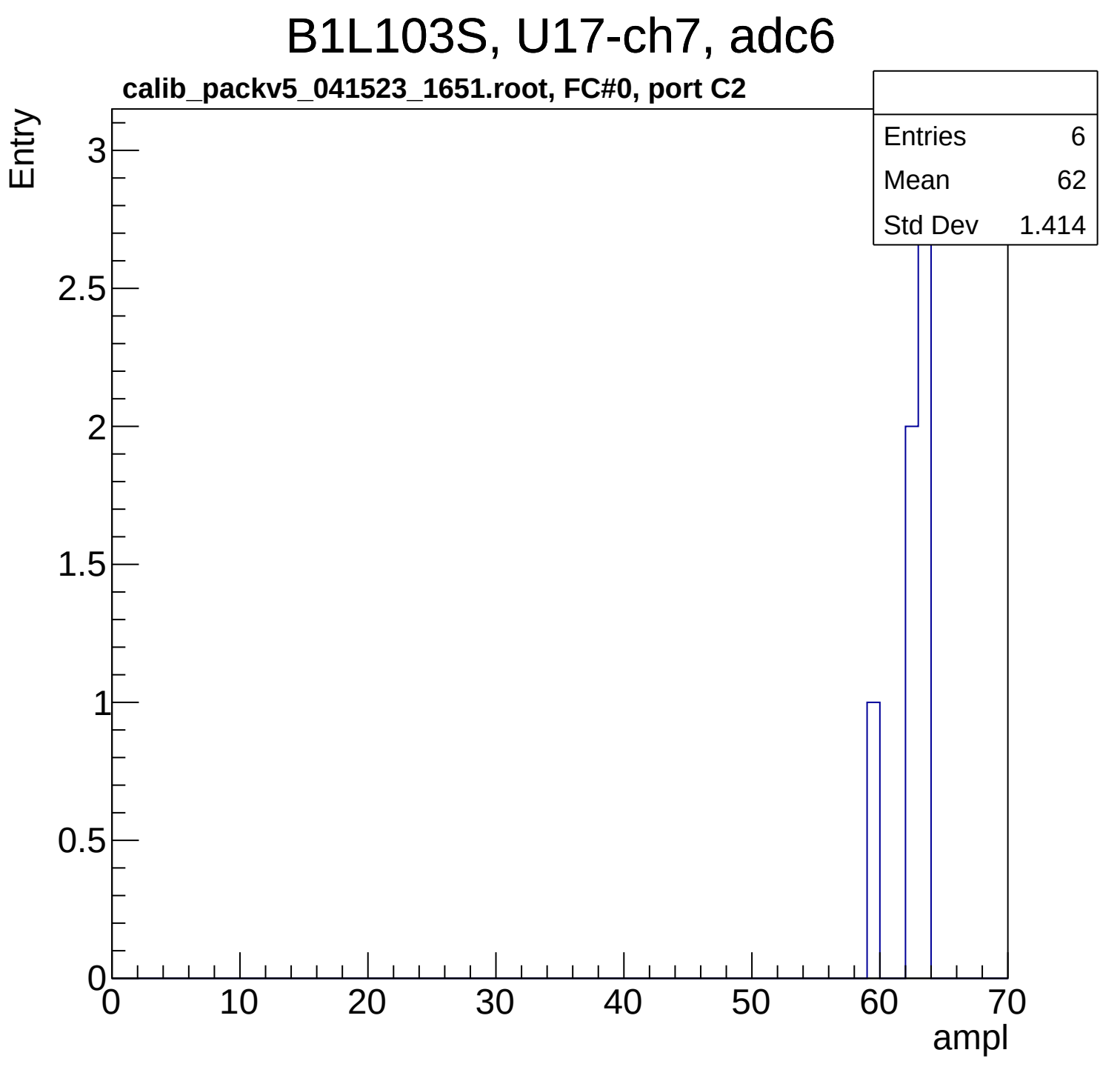
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U17-ch7, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 56.06
Std Dev 3.545
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U17-ch7, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 36
Mean 58.33
Std Dev 10.16
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U17-ch7, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 62
Std Dev 1.414
Entry
ampl
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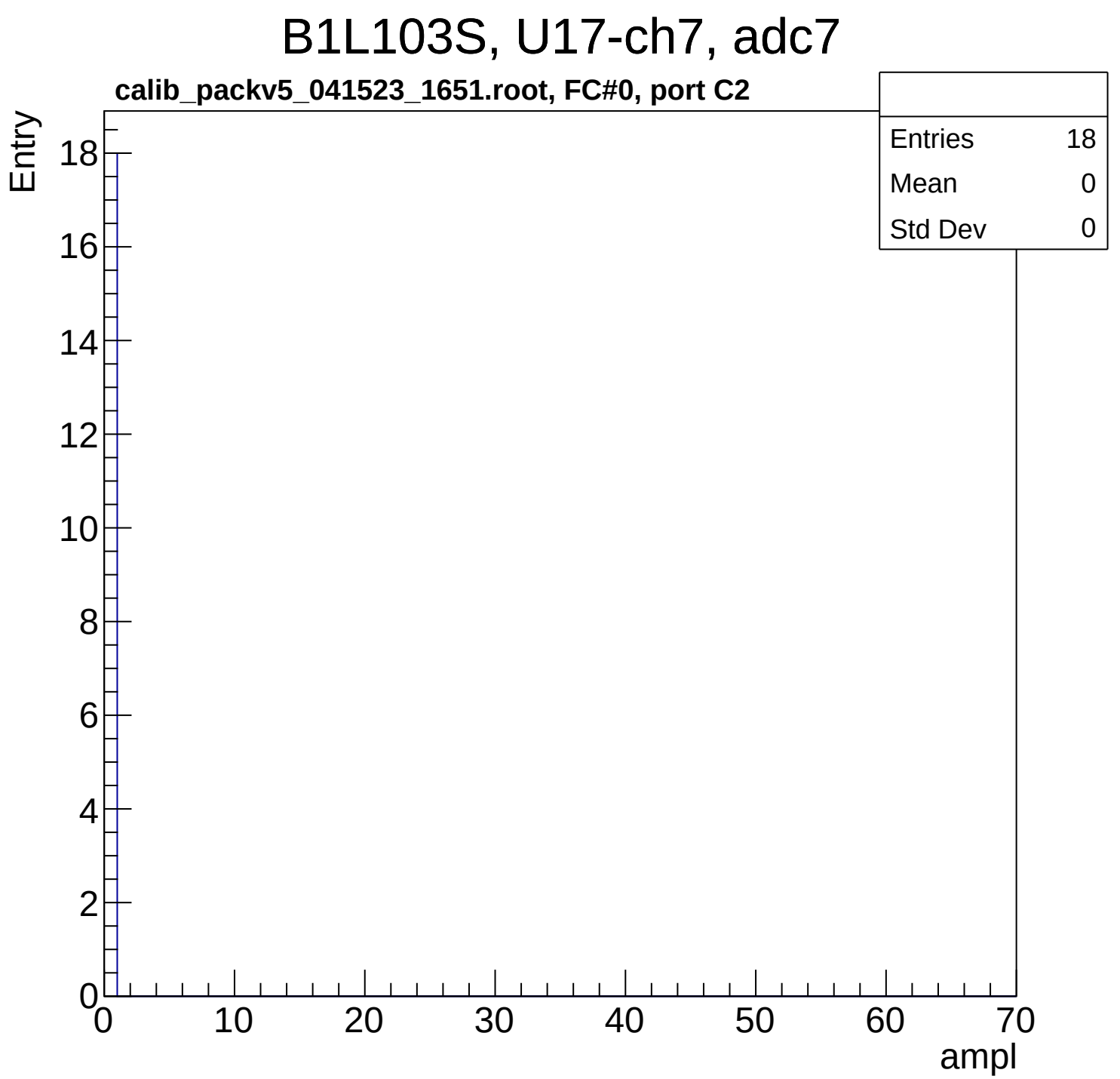
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U17-ch7, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
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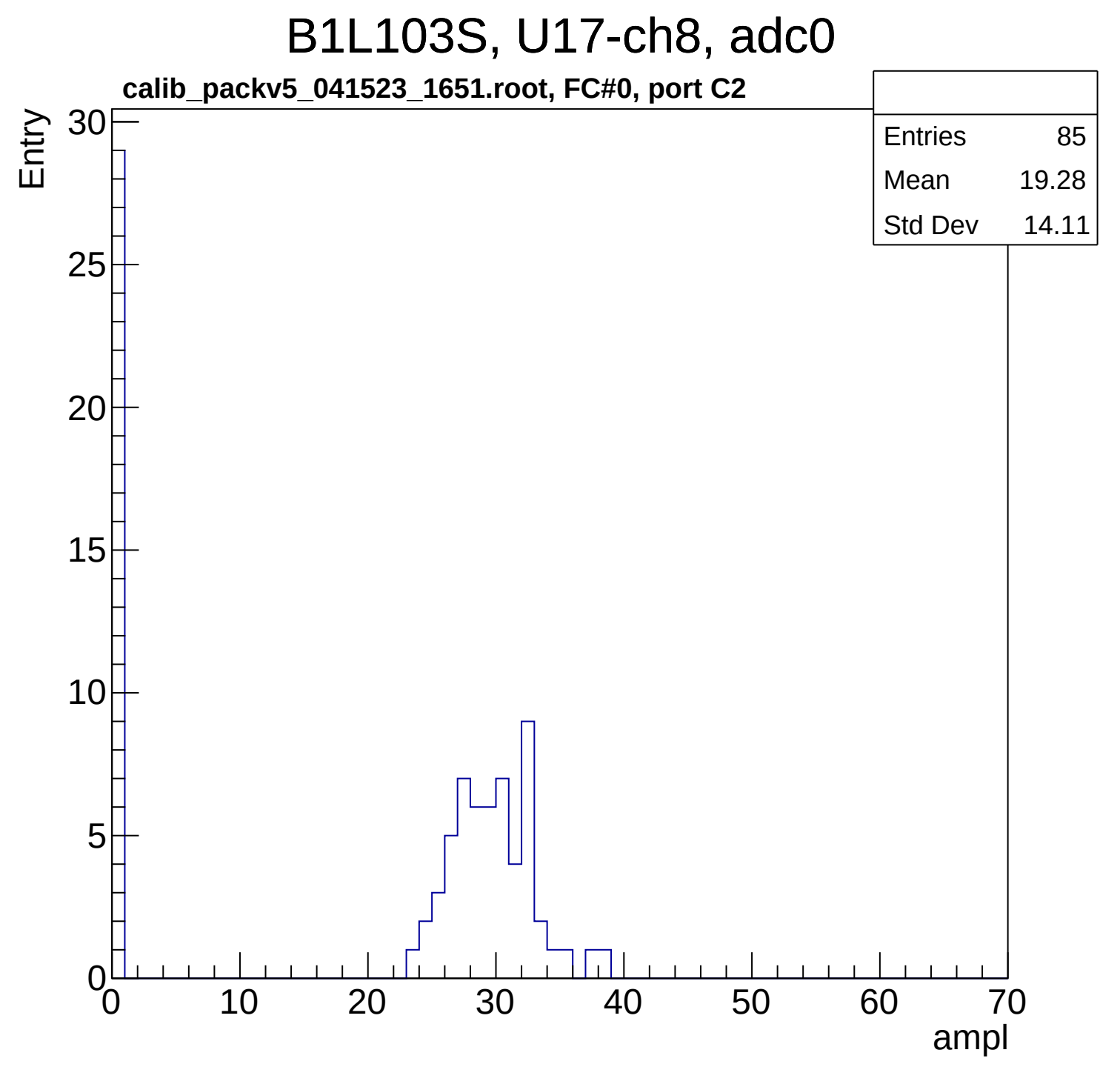
40
50
60
70
ampl


B1L103S, U17-ch8, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 19.28
Std Dev 14.11
Entry
ampl
0
5
10
15
20
25
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0
10
20
30
40
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60
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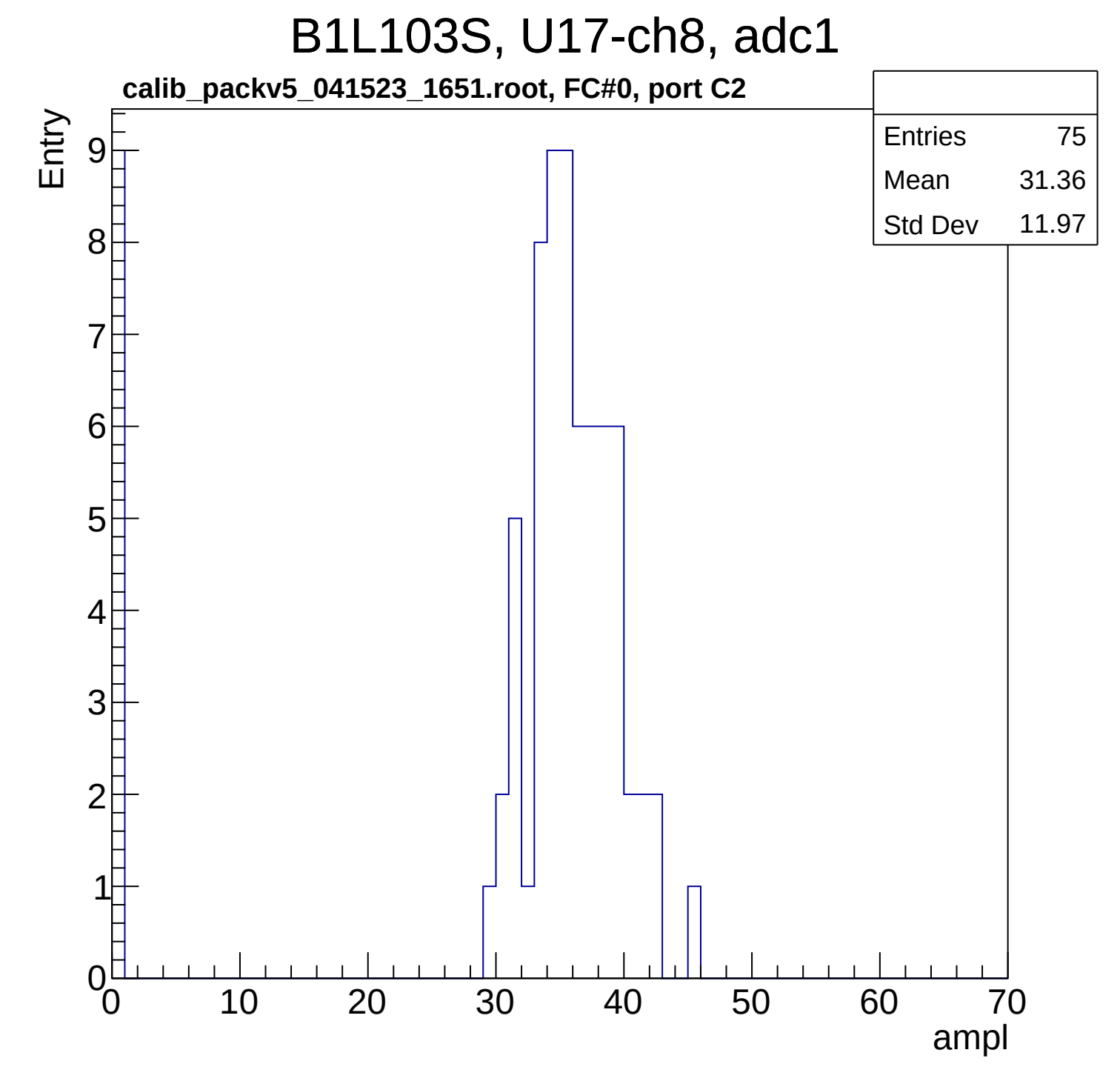
B1L103S, U17-ch8, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 31.36
Std Dev 11.97
Entry
ampl
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2
3
4
5
6
7
8
9
0
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60
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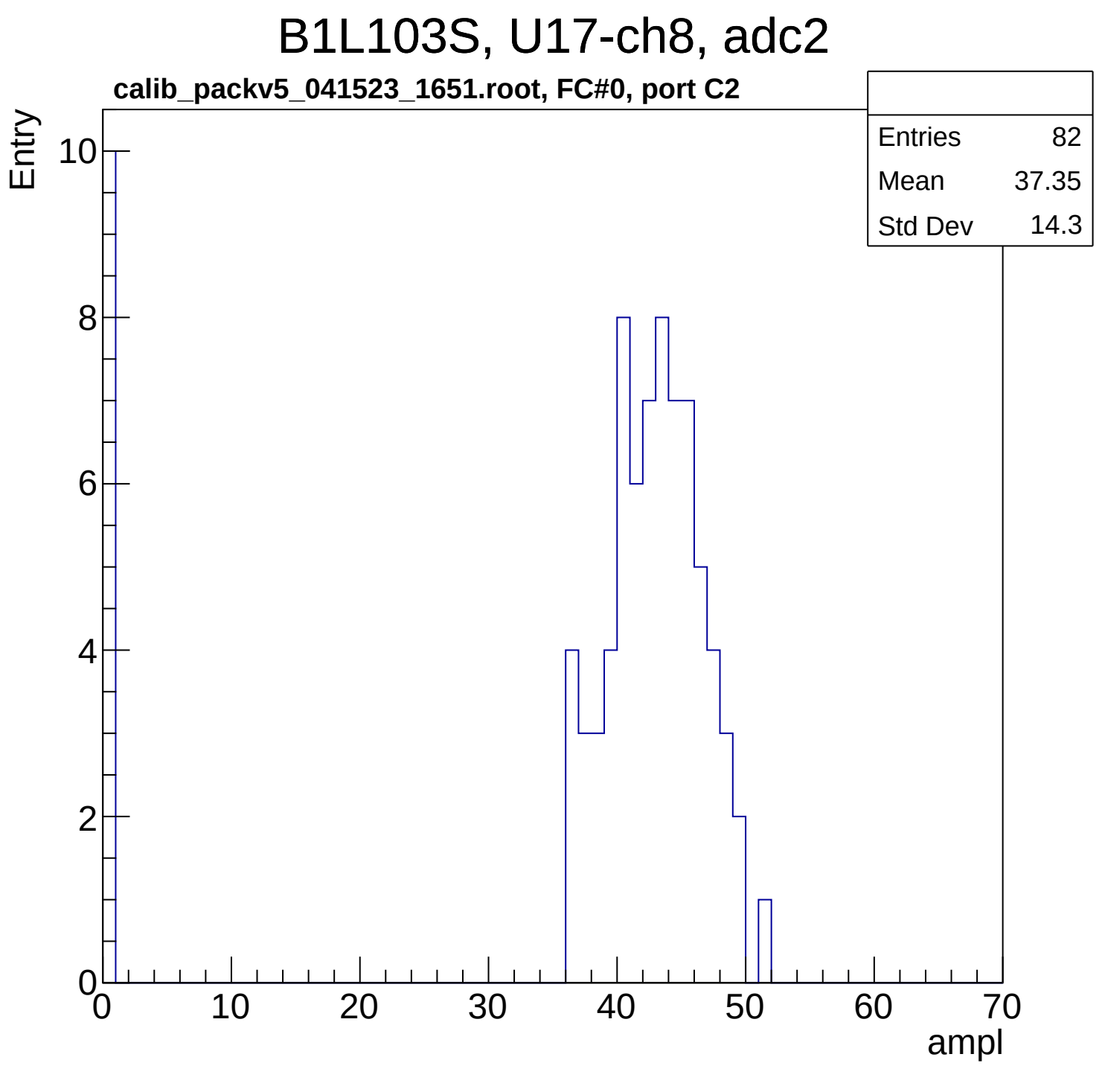
B1L103S, U17-ch8, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 37.35
Std Dev 14.3
Entry
ampl
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4
6
8
10
0
10
20
30
40
50
60
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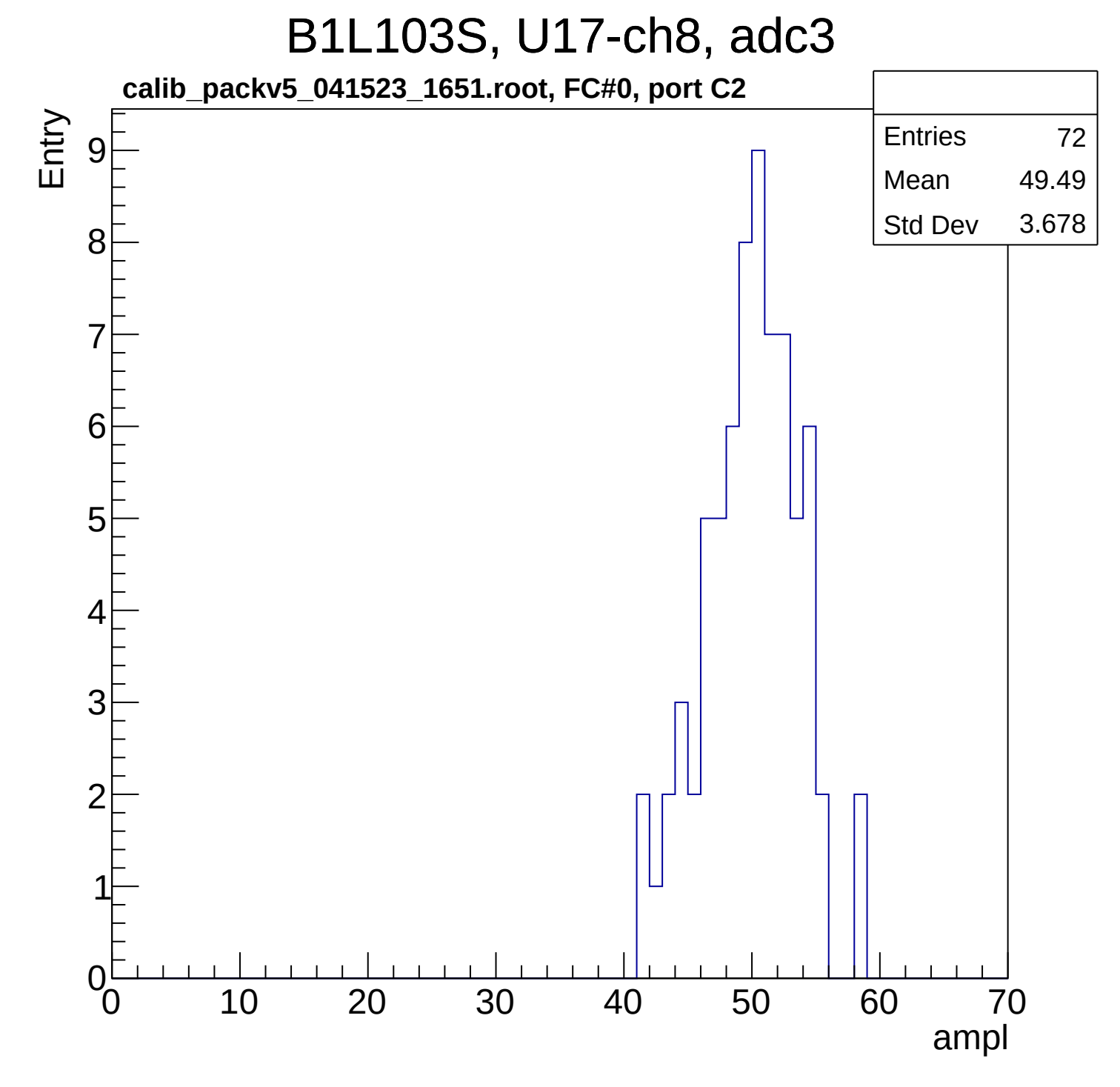
B1L103S, U17-ch8, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 49.49
Std Dev 3.678
Entry
ampl
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6
7
8
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0
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60
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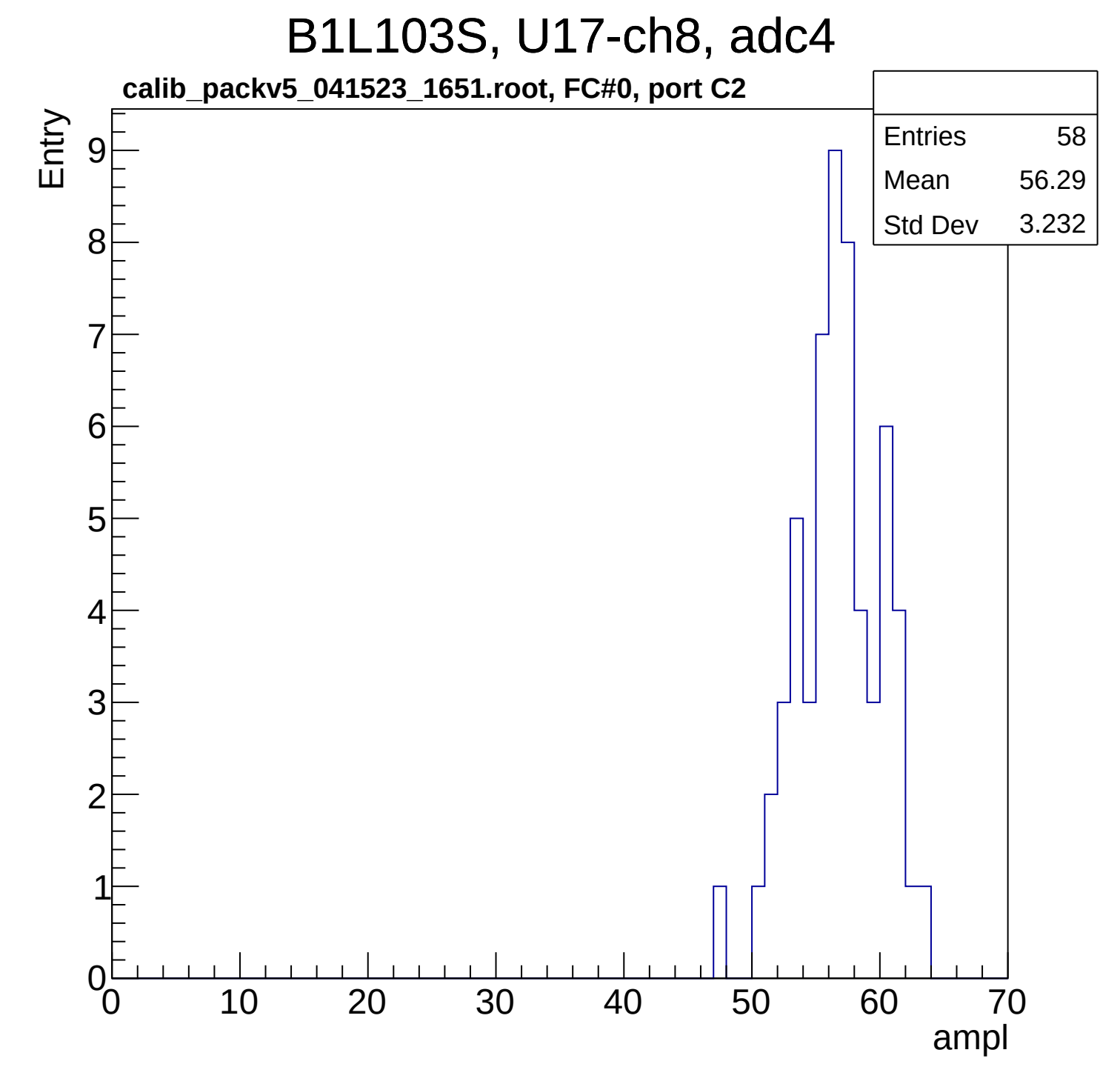
B1L103S, U17-ch8, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 56.29
Std Dev 3.232
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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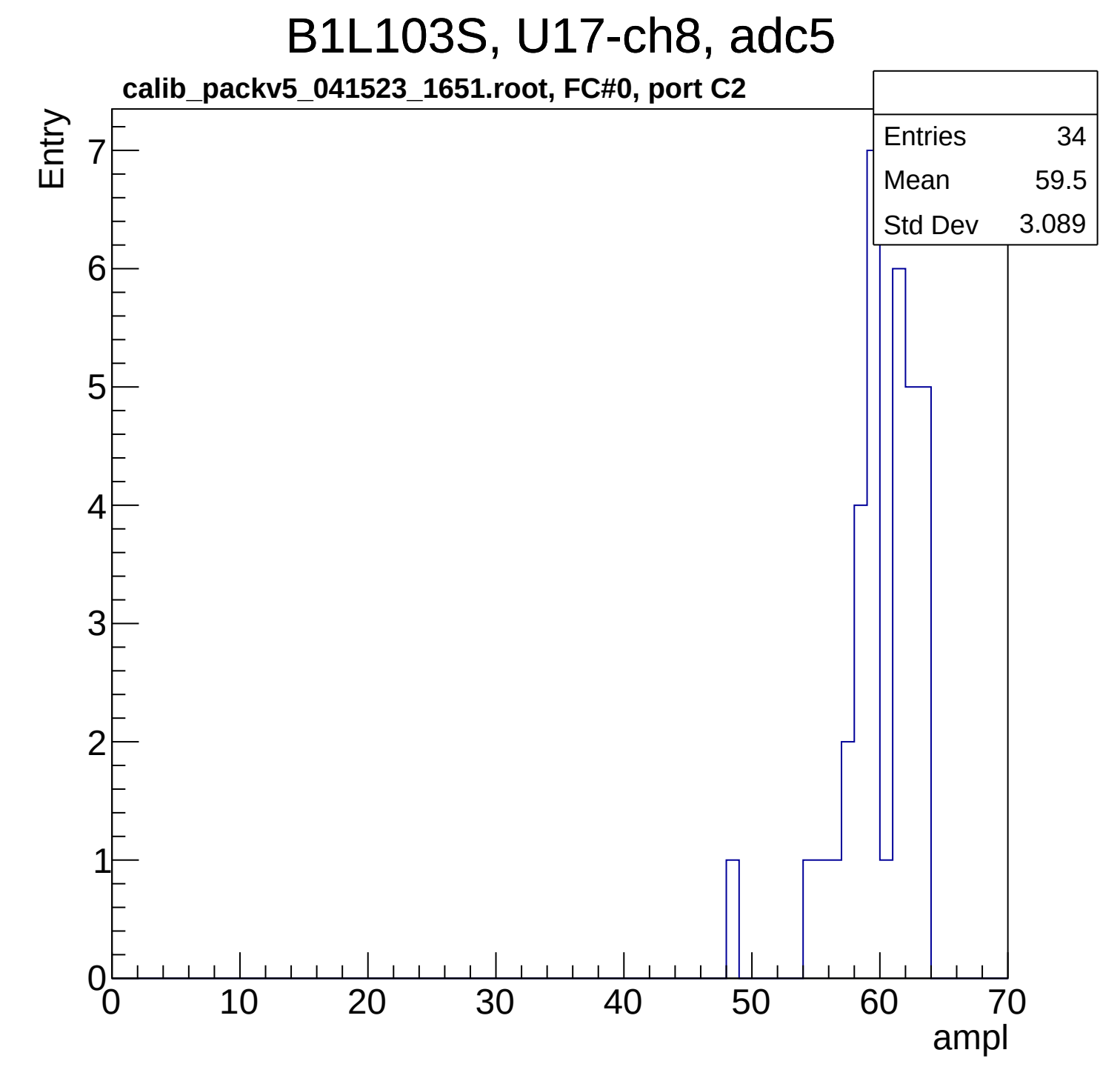
B1L103S, U17-ch8, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 34
Mean 59.5
Std Dev 3.089
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
30
40
50
60
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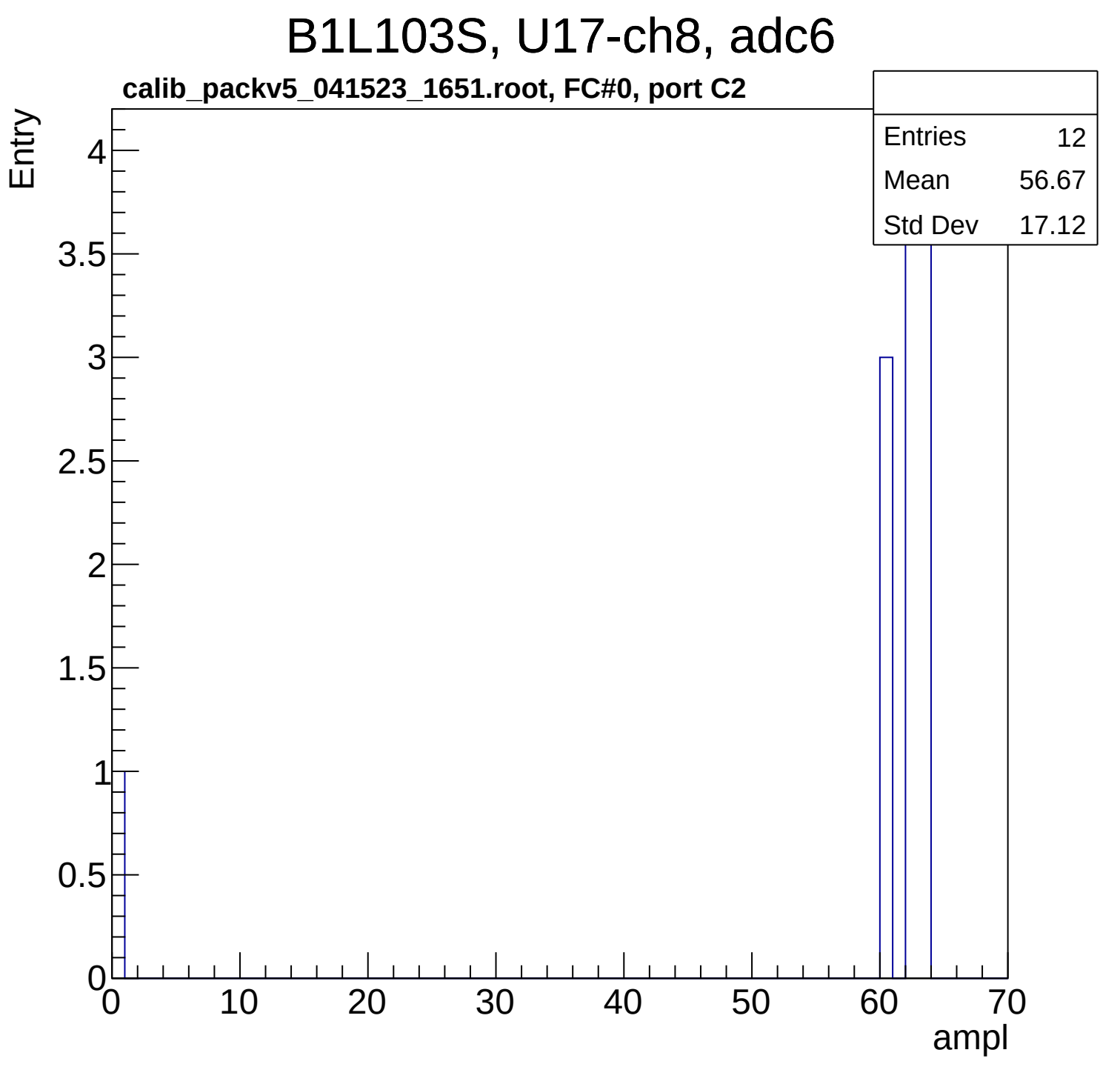
B1L103S, U17-ch8, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 56.67
Std Dev 17.12
Entry
ampl
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1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
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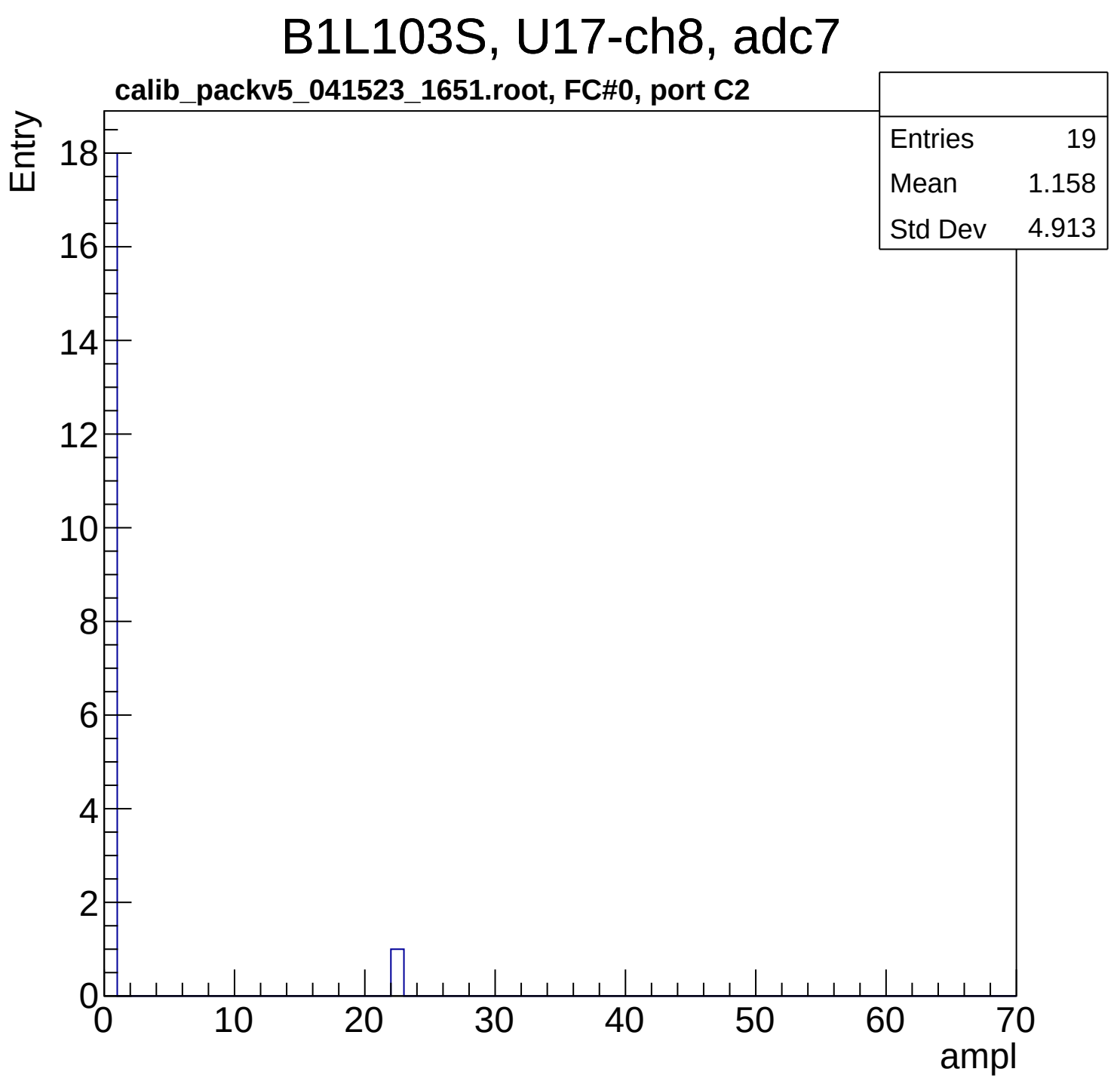
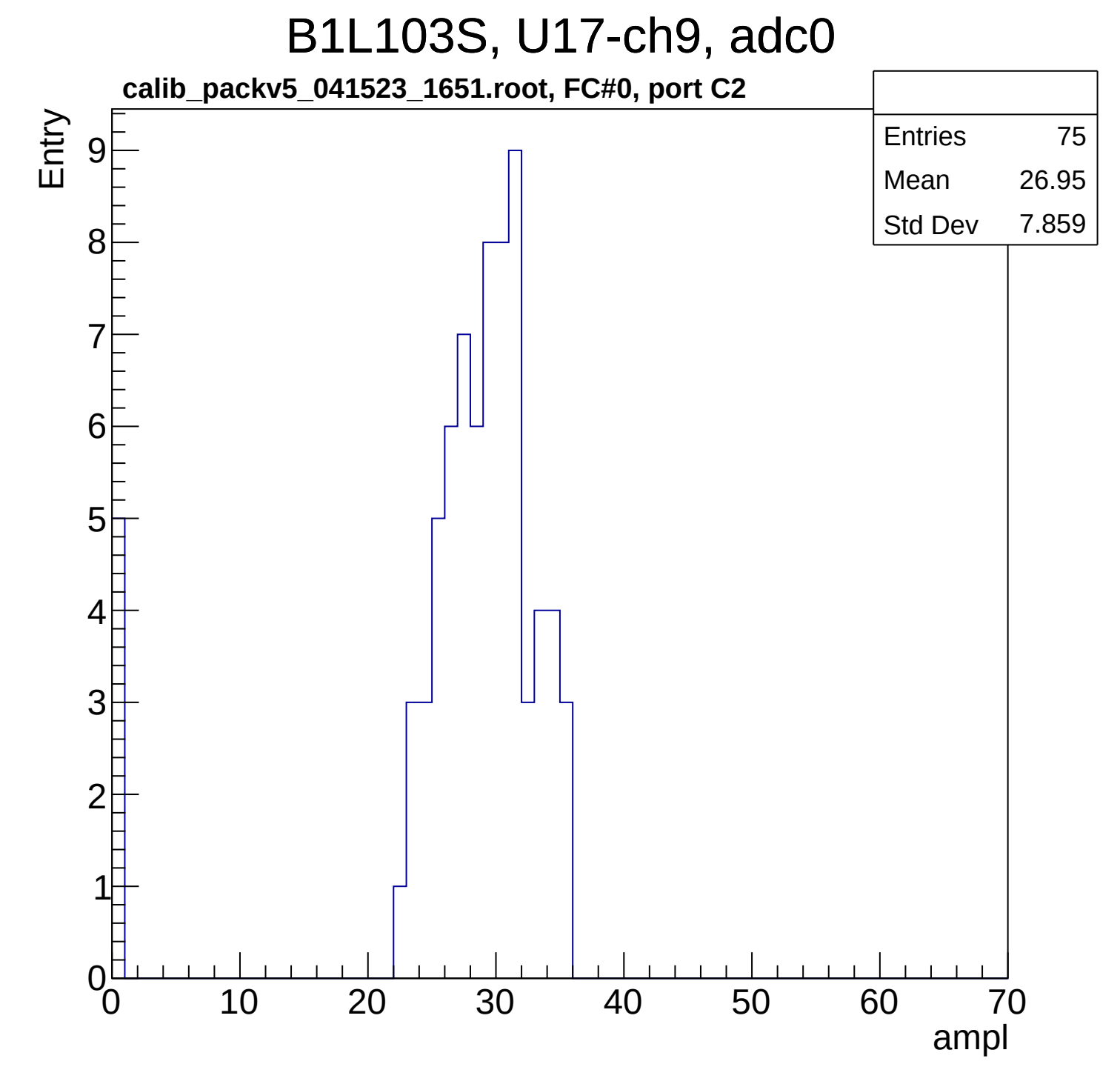

B1L103S, U17-ch8, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.158
Std Dev 4.913
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch9, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 26.95
Std Dev 7.859
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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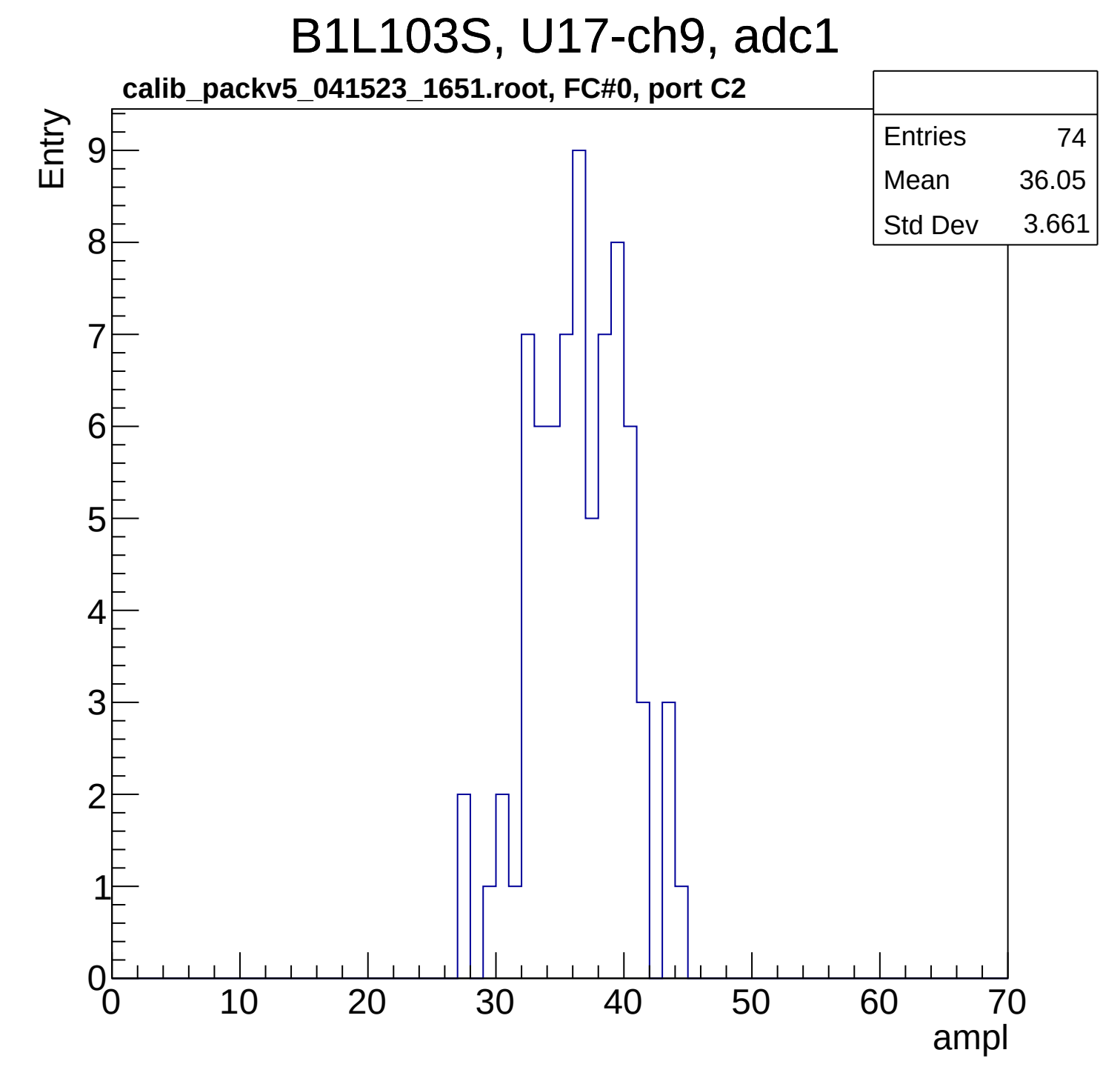
B1L103S, U17-ch9, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 36.05
Std Dev 3.661
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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60
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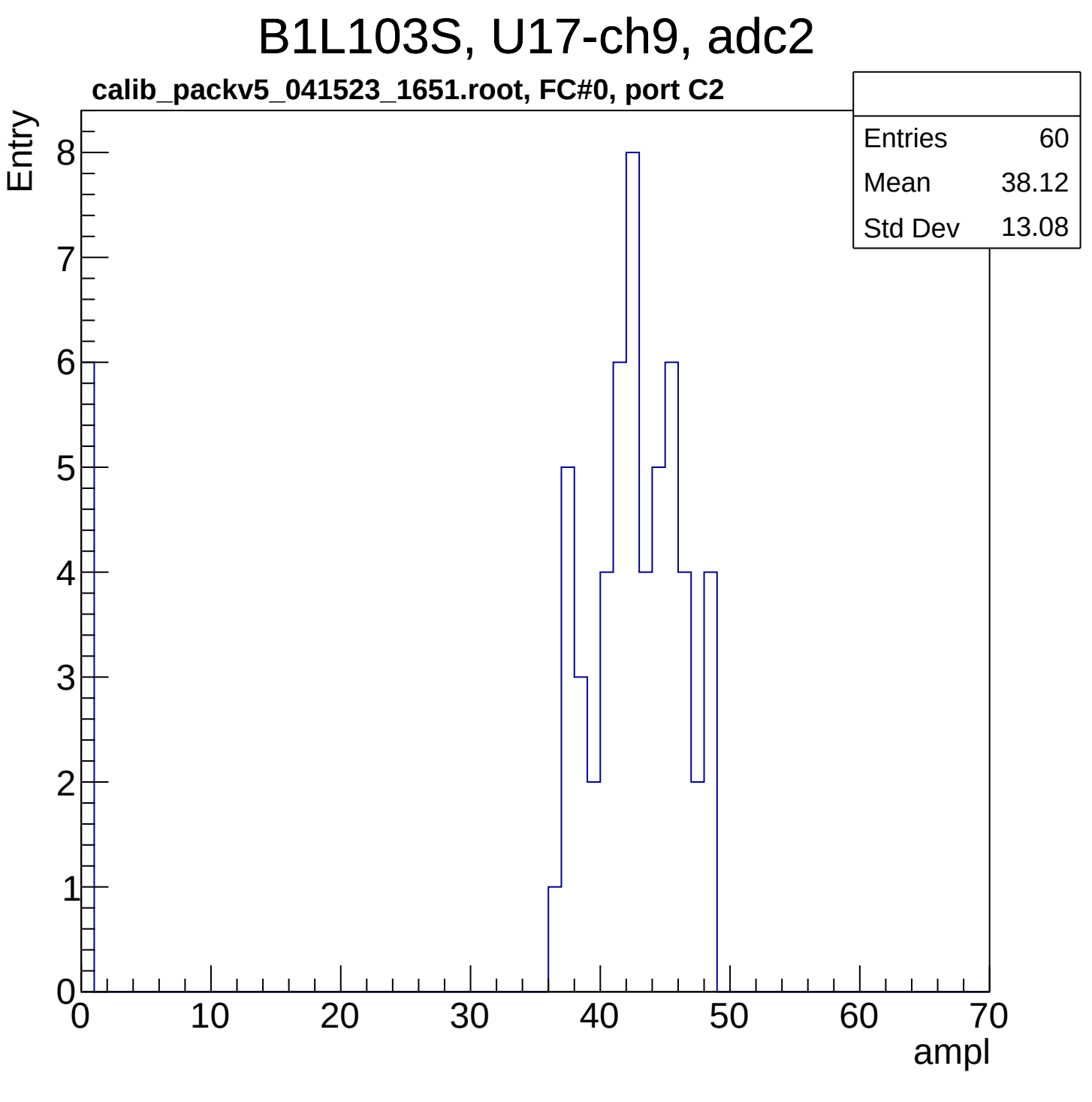
B1L103S, U17-ch9, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 38.12
Std Dev 13.08
Entry
ampl
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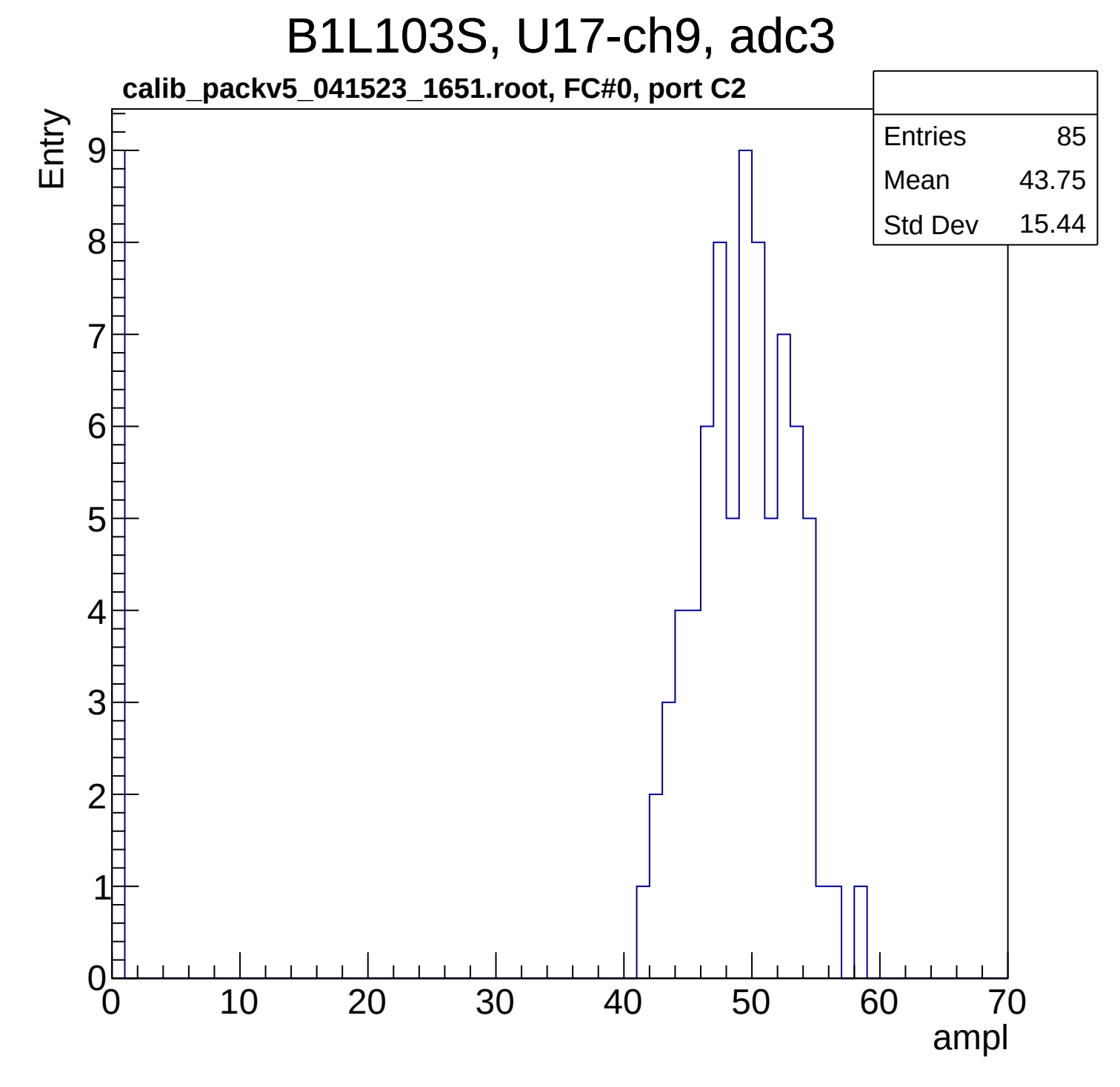
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U17-ch9, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 43.75
Std Dev 15.44
Entry
ampl
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3
4
5
6
7
8
9
0
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60
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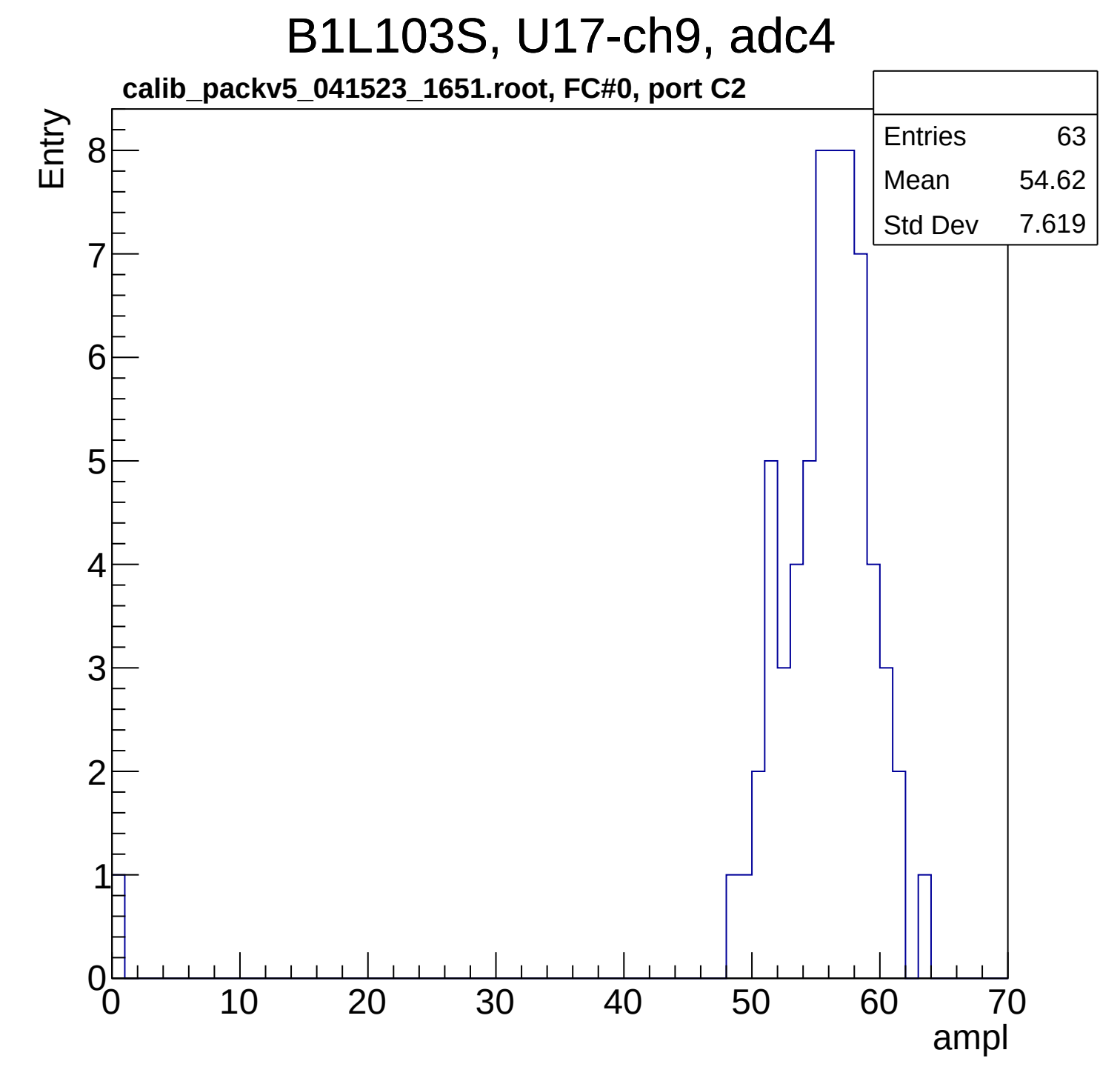
B1L103S, U17-ch9, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 54.62
Std Dev 7.619
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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40
50
60
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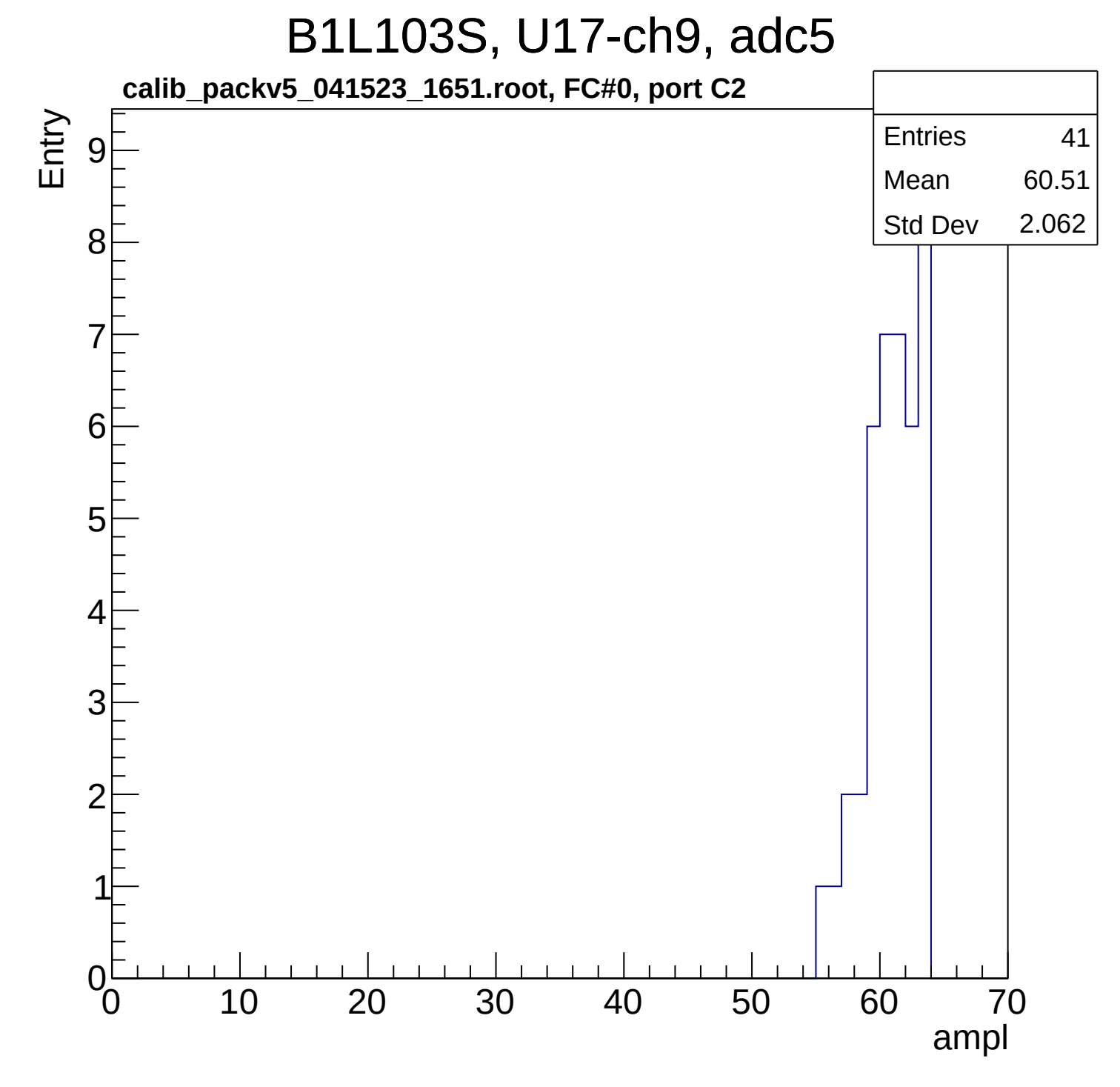
B1L103S, U17-ch9, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 41
Mean 60.51
Std Dev 2.062
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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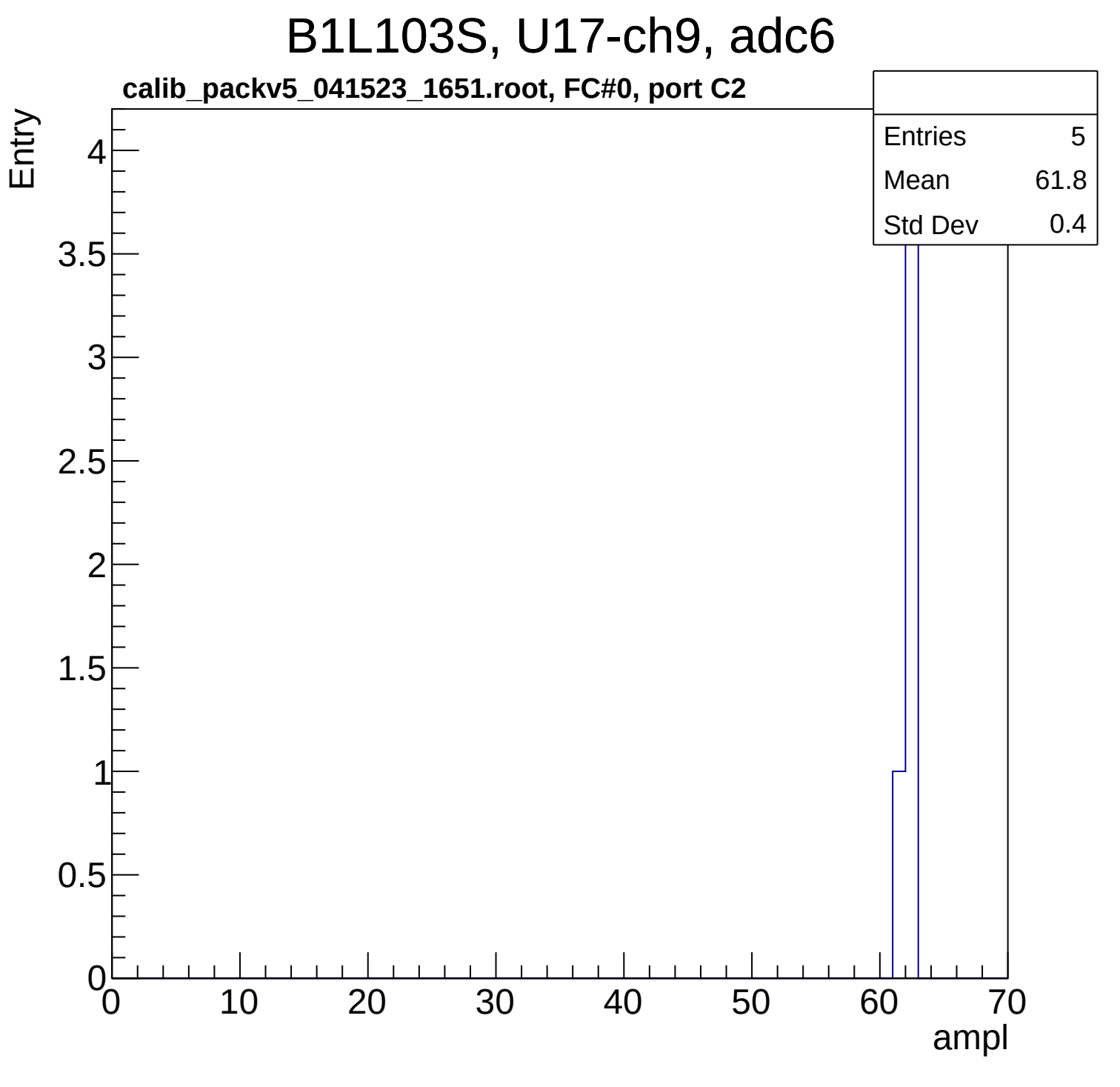
B1L103S, U17-ch9, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 5
Mean 61.8
Std Dev 0.4
Entry
ampl
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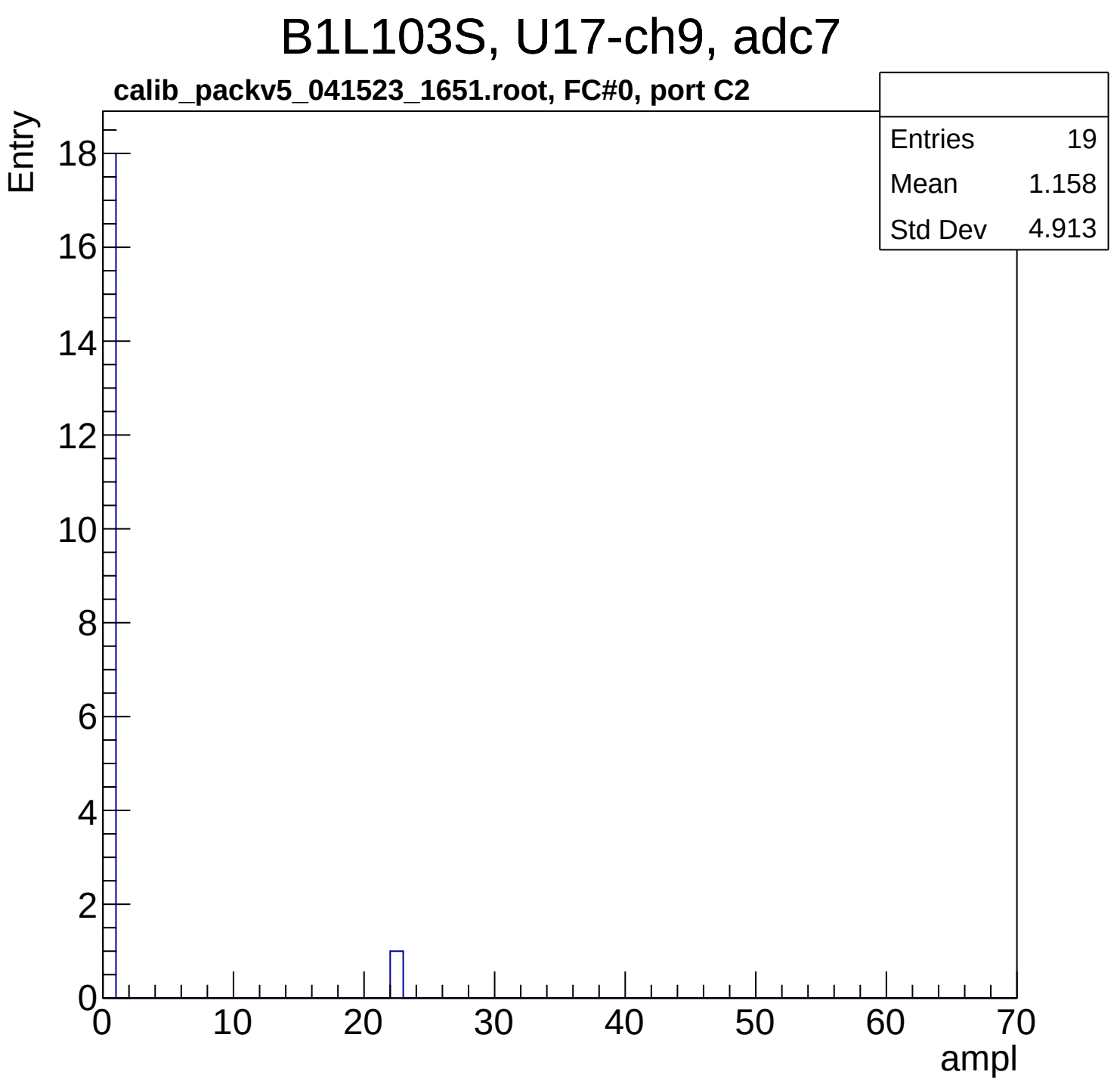
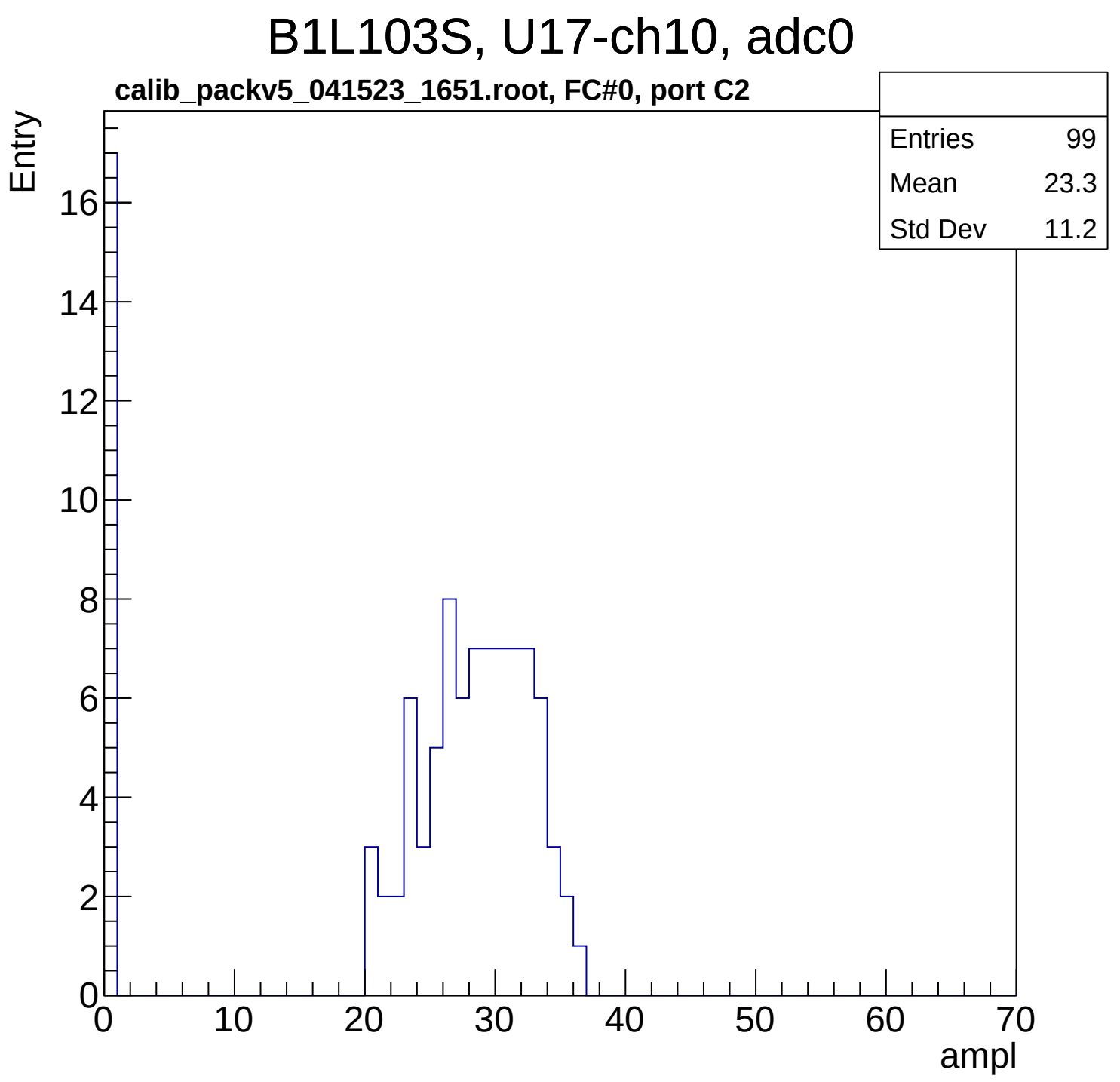
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U17-ch9, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.158
Std Dev 4.913
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch10, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 99
Mean 23.3
Std Dev 11.2
Entry
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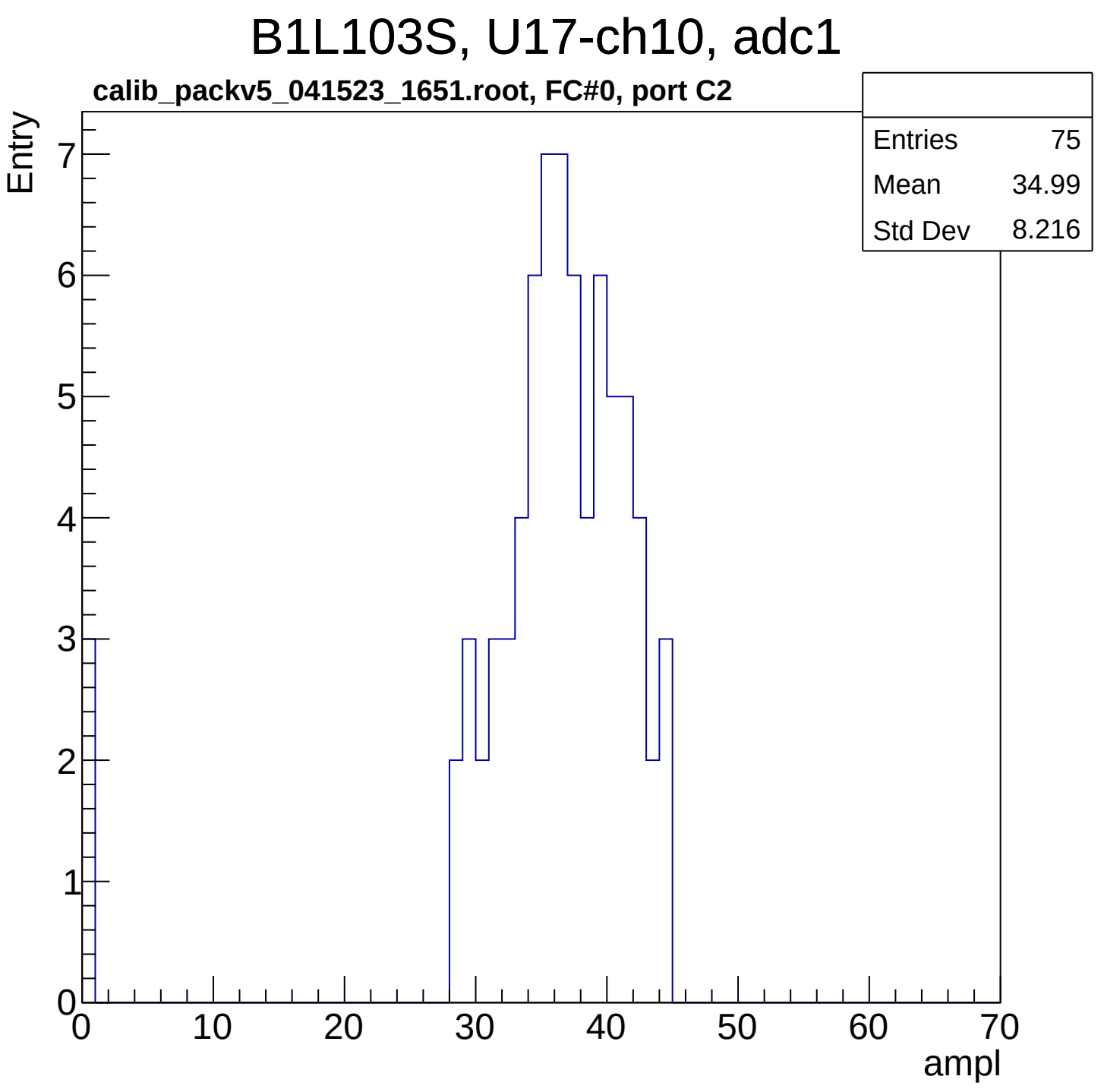
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch10, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 34.99
Std Dev 8.216
Entry
ampl
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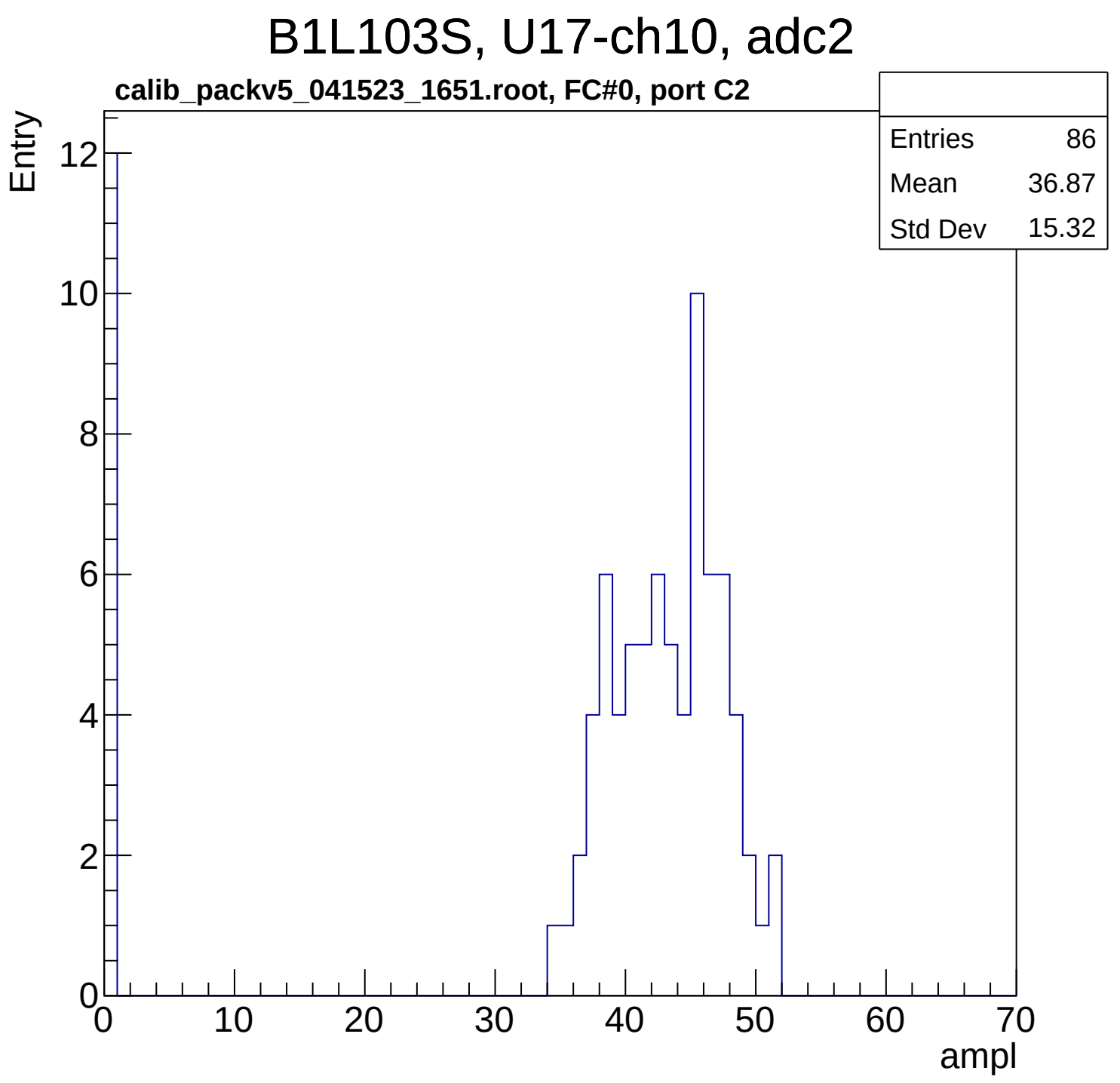
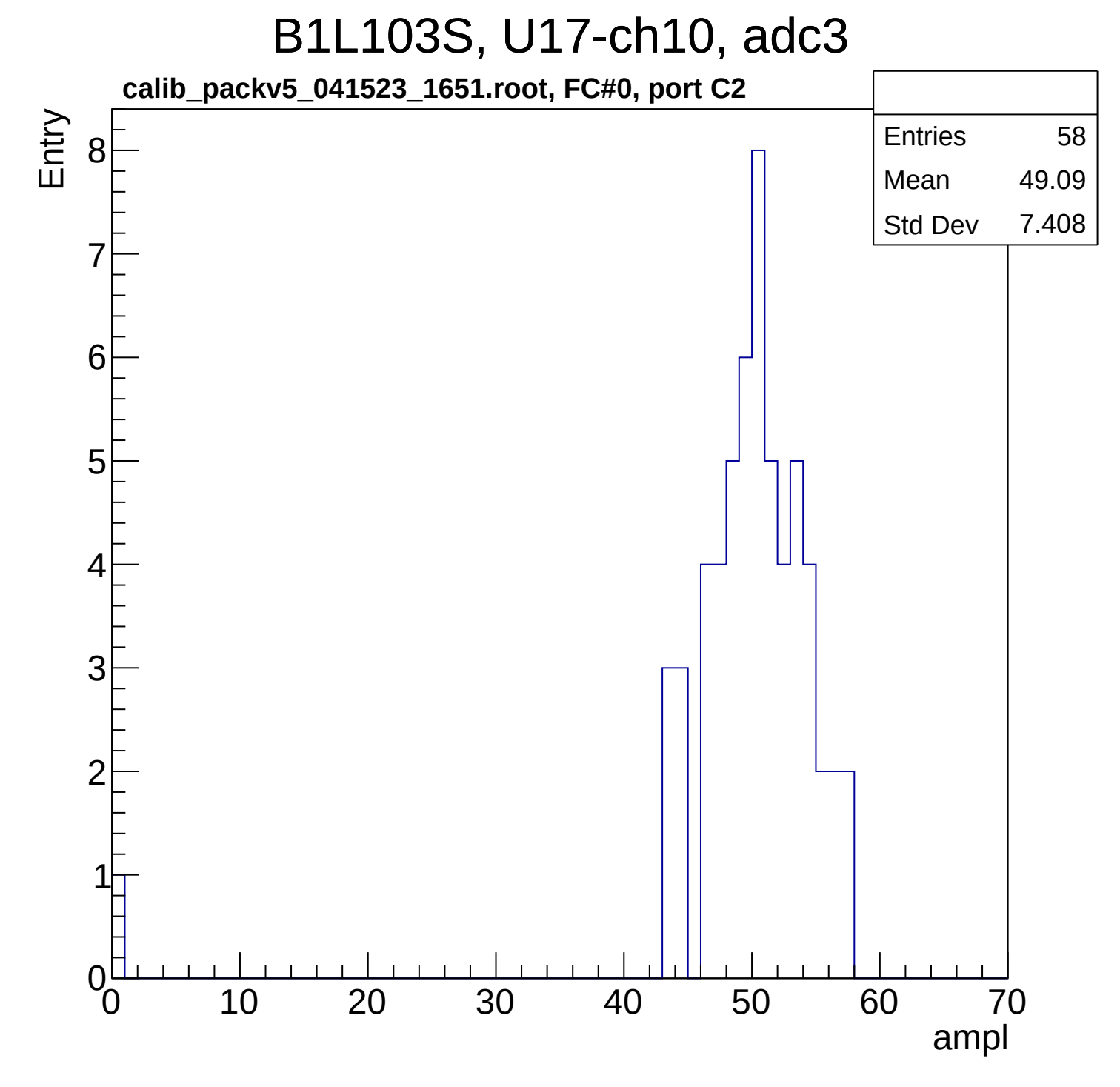
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U17-ch10, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 36.87
Std Dev 15.32
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch10, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 49.09
Std Dev 7.408
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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60
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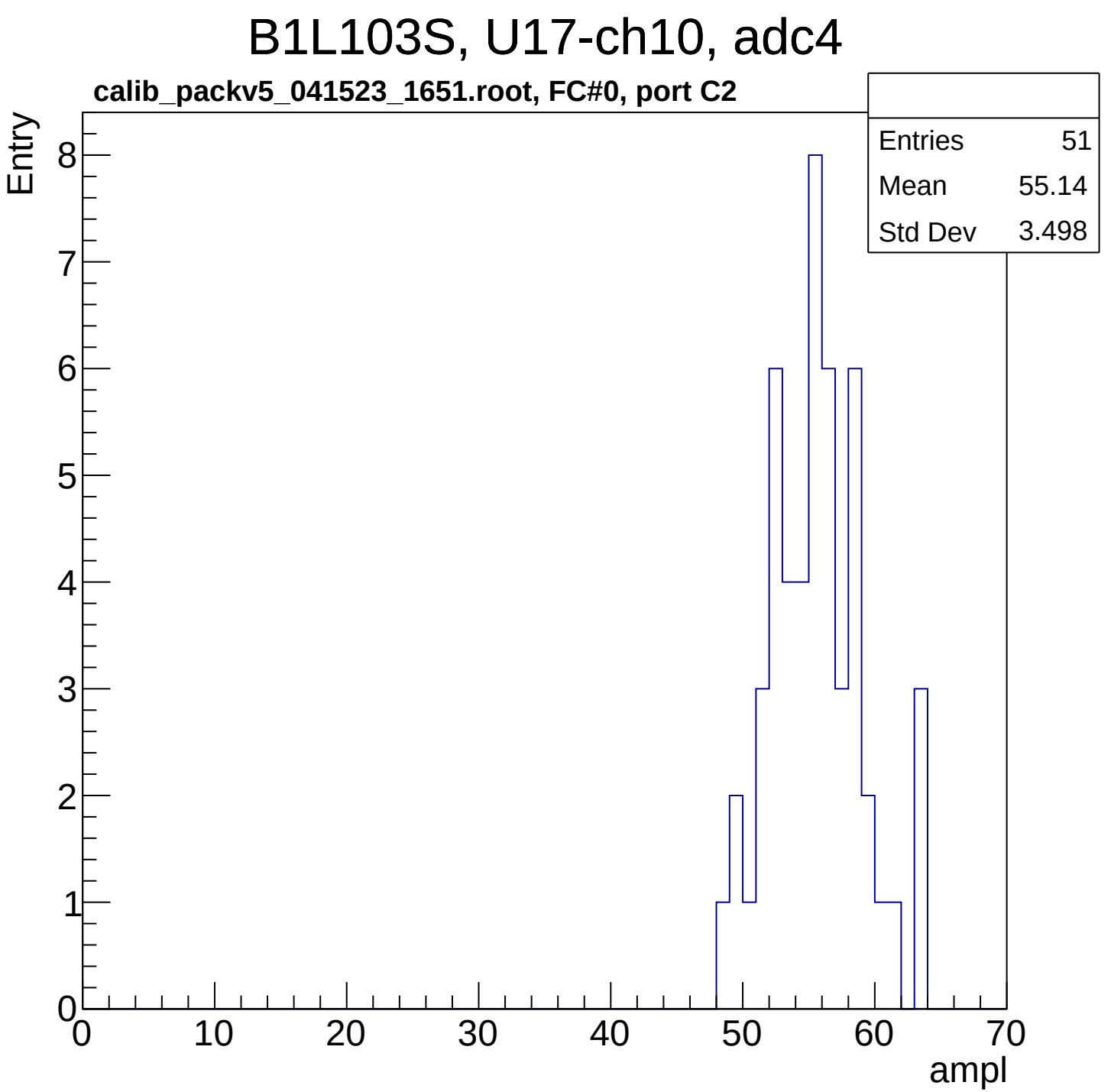
B1L103S, U17-ch10, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 55.14
Std Dev 3.498
Entry
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2
3
4
5
6
7
8
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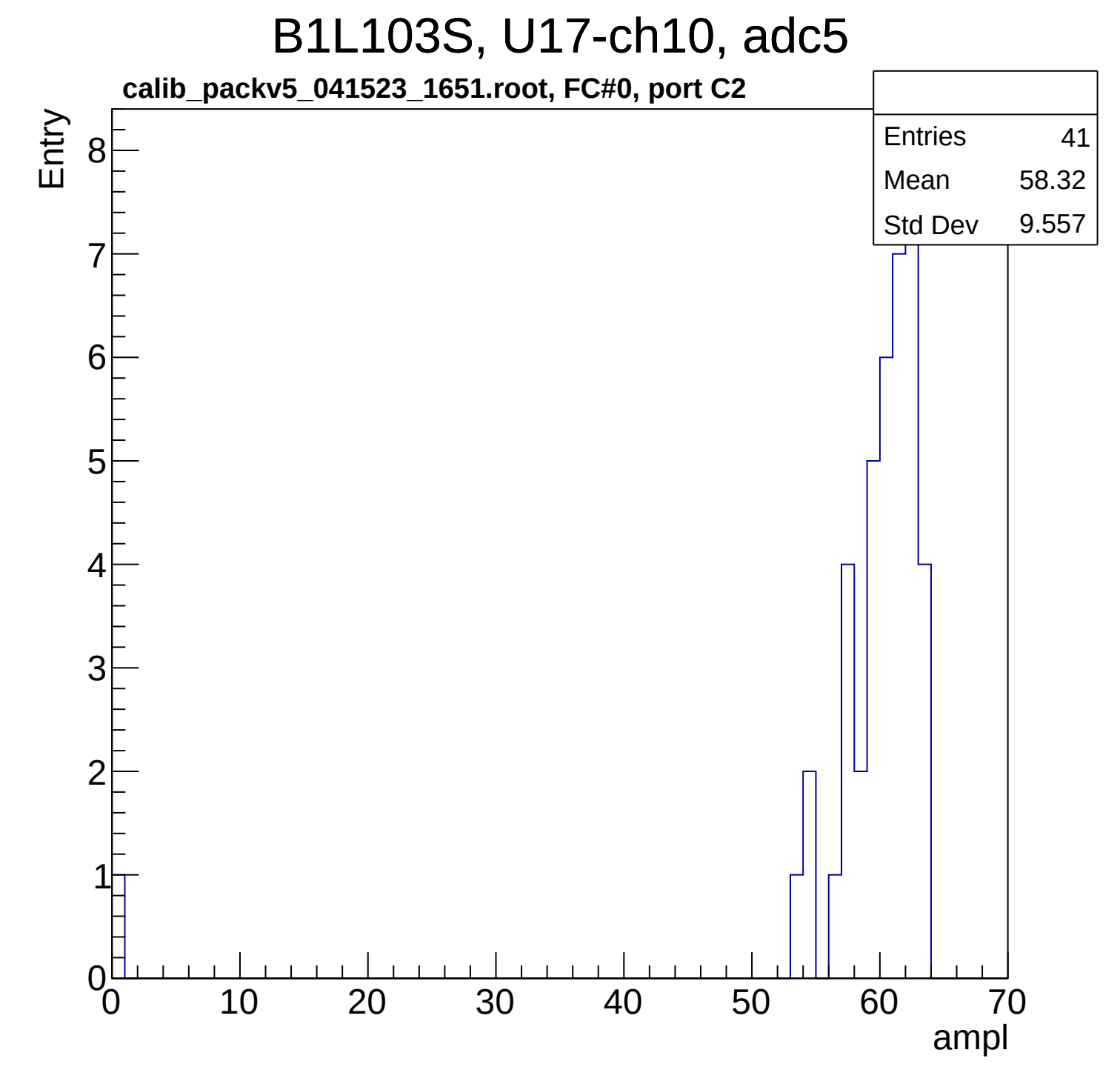
50
60
70
ampl


B1L103S, U17-ch10, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 41
Mean 58.32
Std Dev 9.557
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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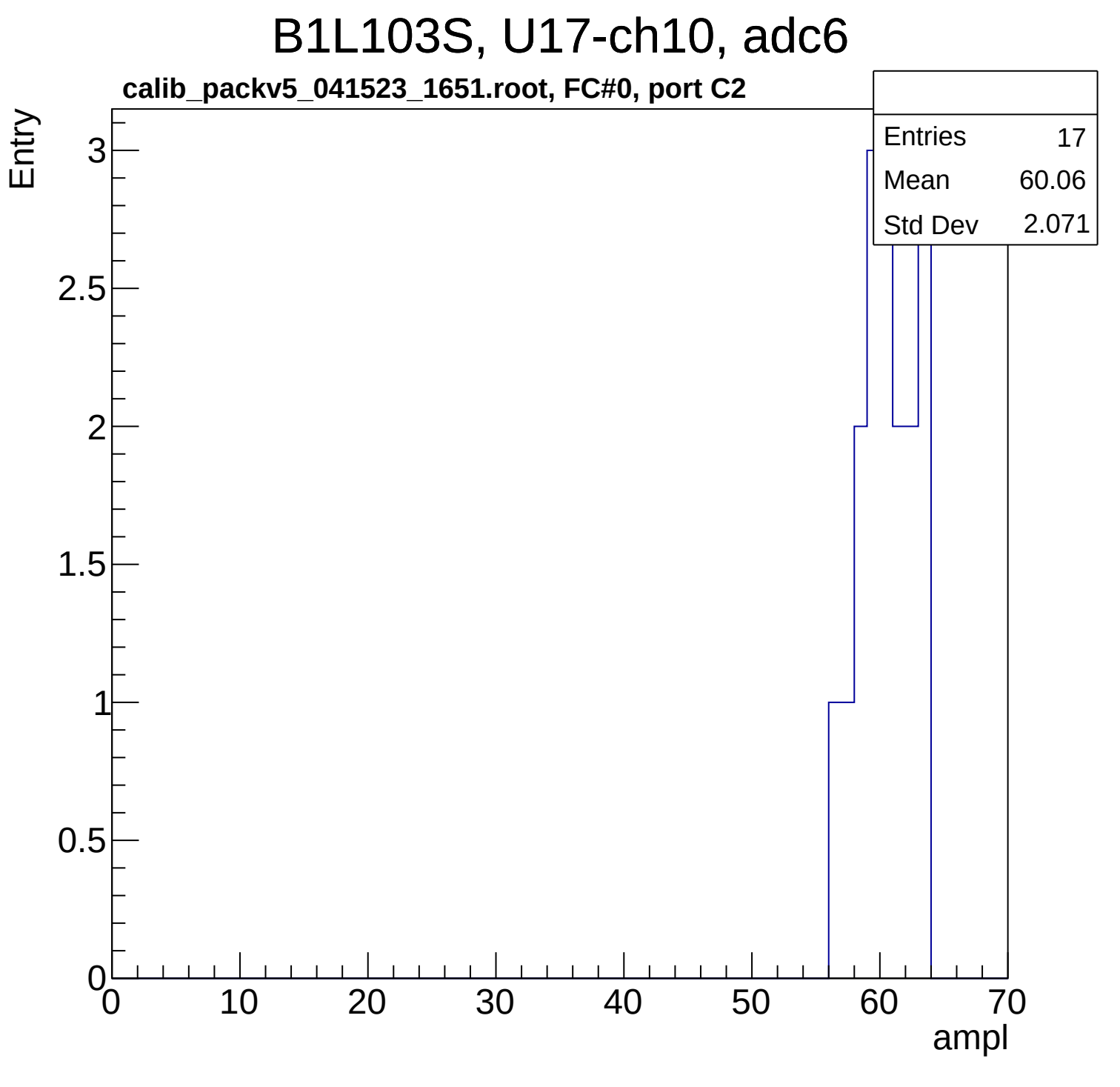
B1L103S, U17-ch10, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 17
Mean 60.06
Std Dev 2.071
Entry
ampl
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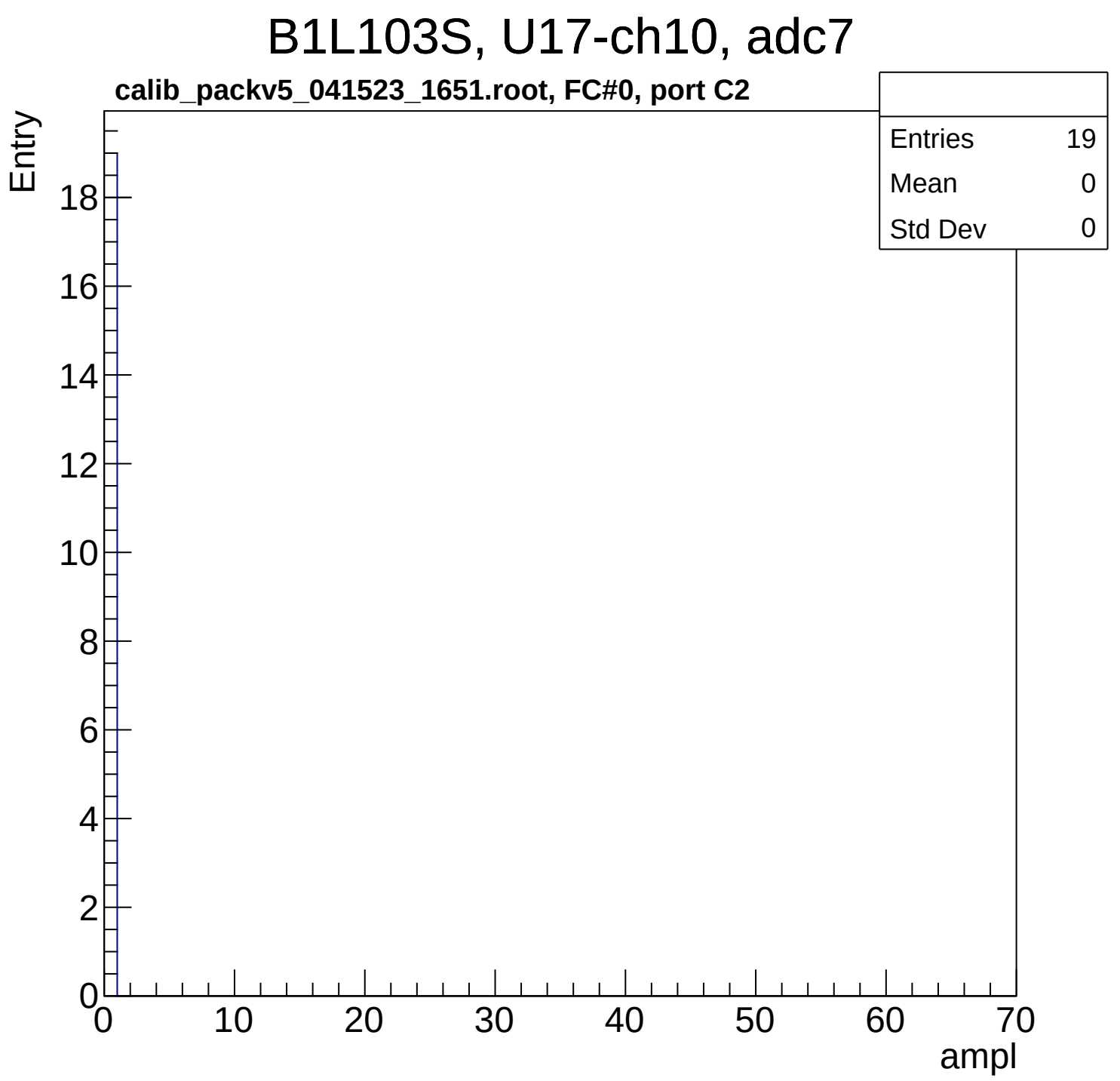
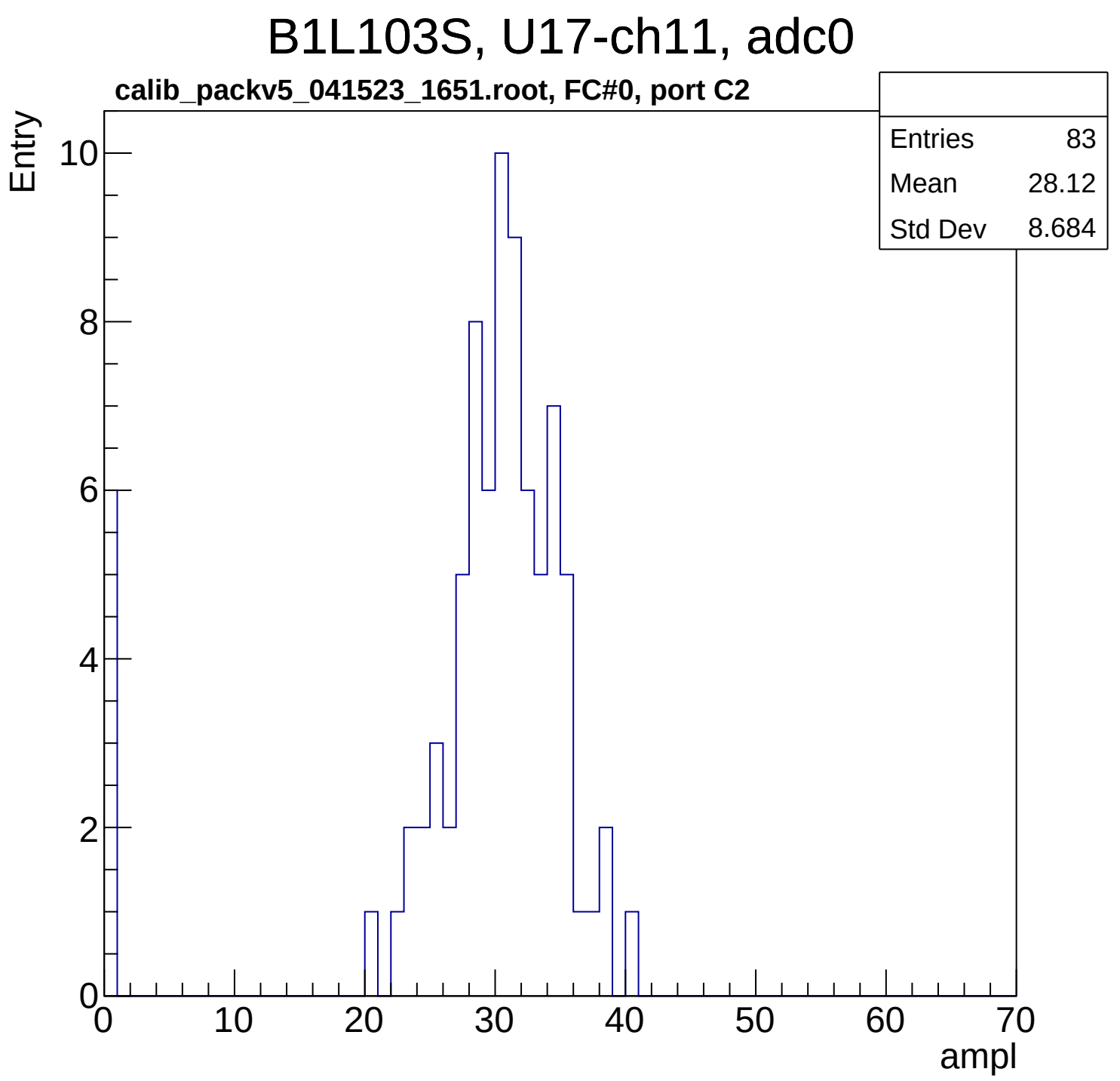
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U17-ch10, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch11, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 28.12
Std Dev 8.684
Entry
ampl
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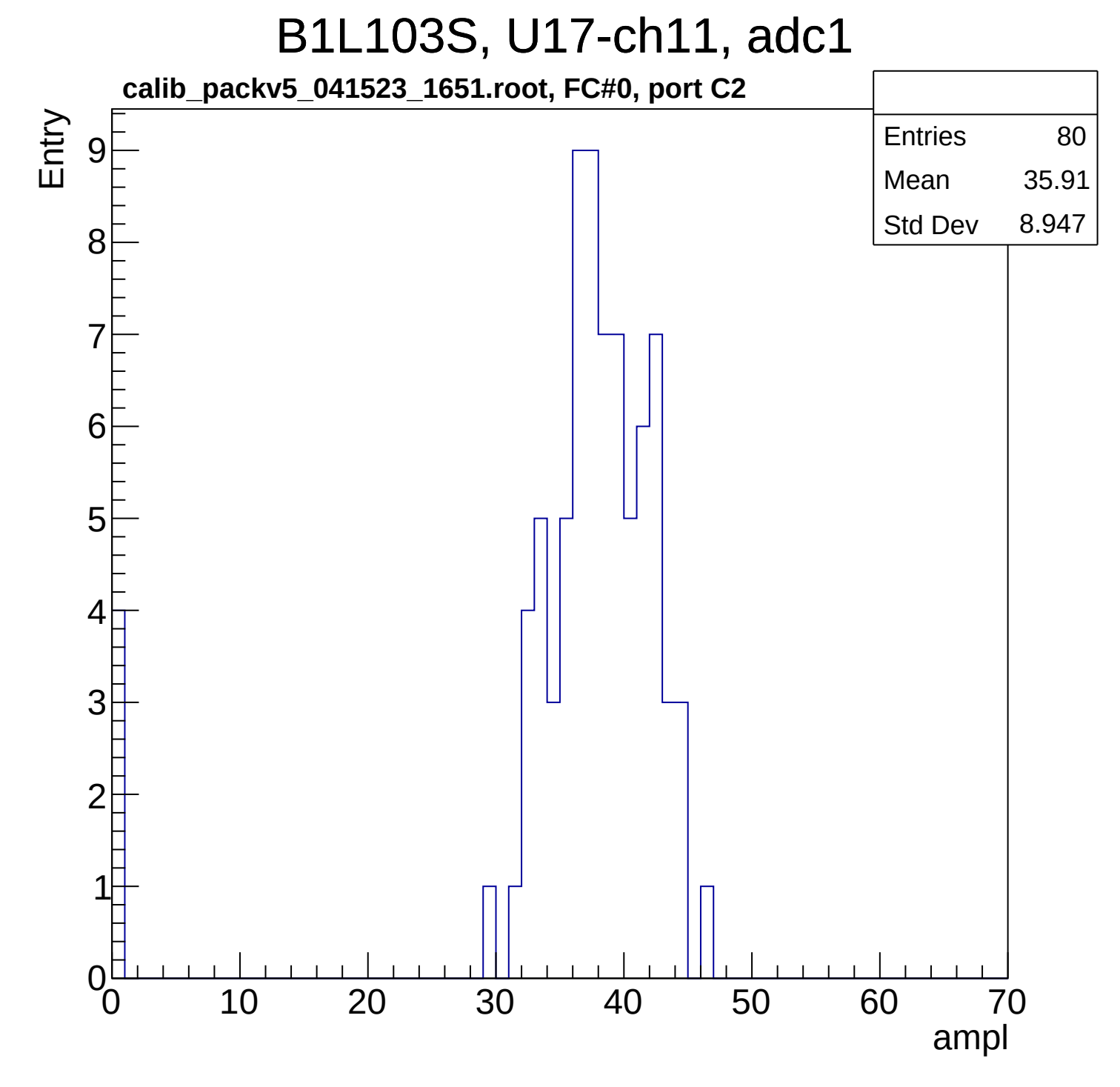
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U17-ch11, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 35.91
Std Dev 8.947
Entry
ampl
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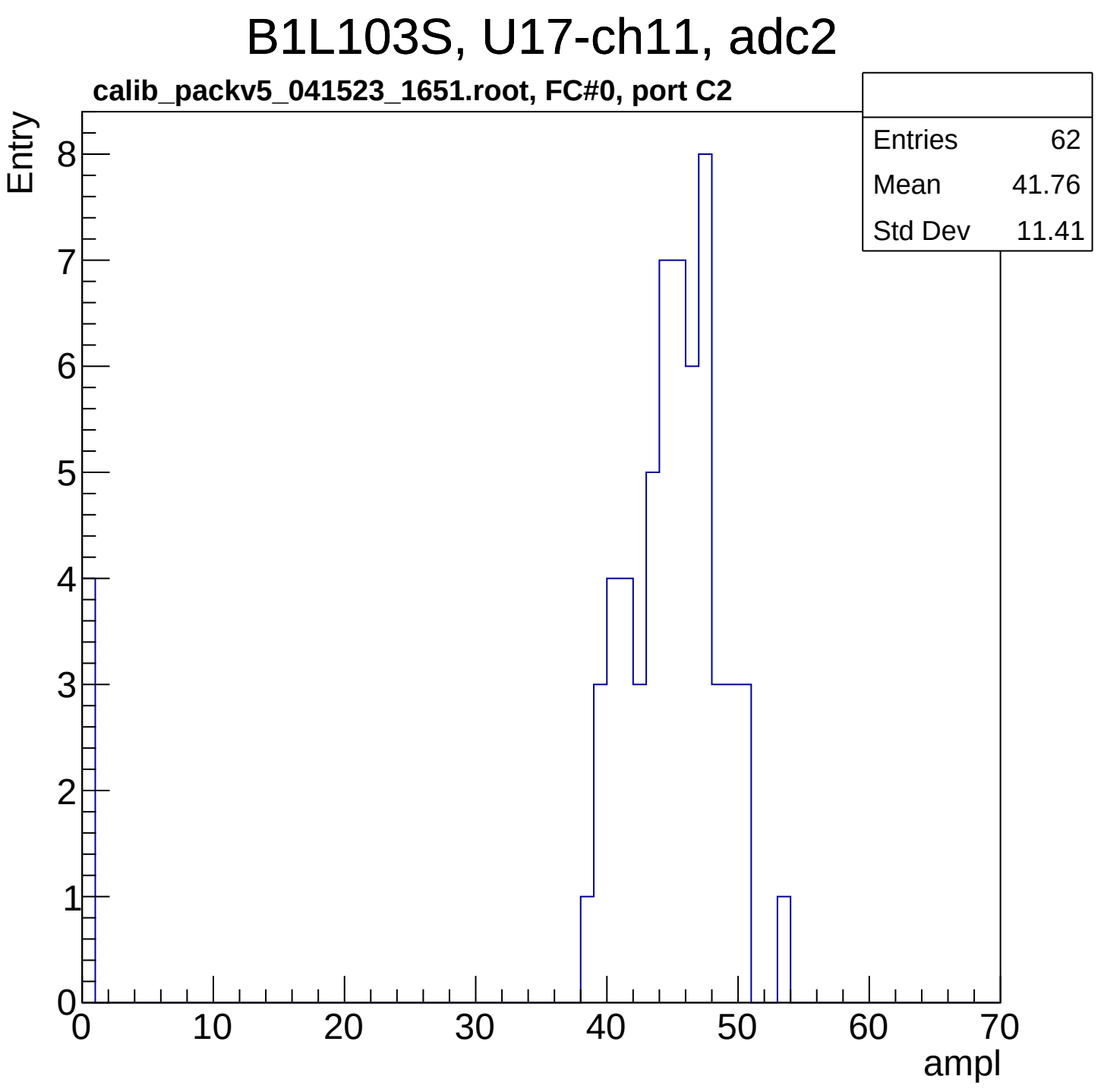
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U17-ch11, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 41.76
Std Dev 11.41
Entry
ampl
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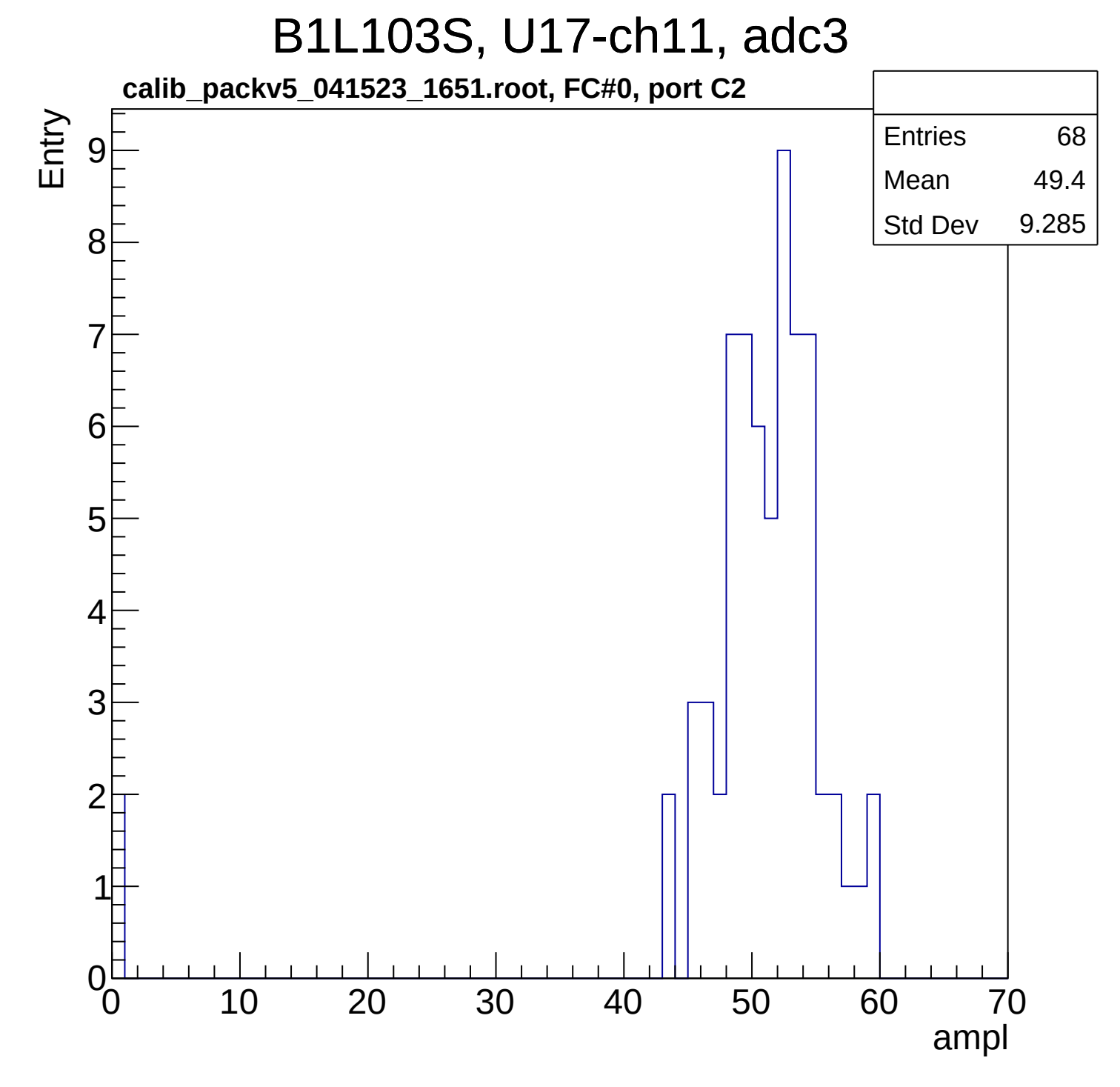
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U17-ch11, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 49.4
Std Dev 9.285
Entry
ampl
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3
4
5
6
7
8
9
0
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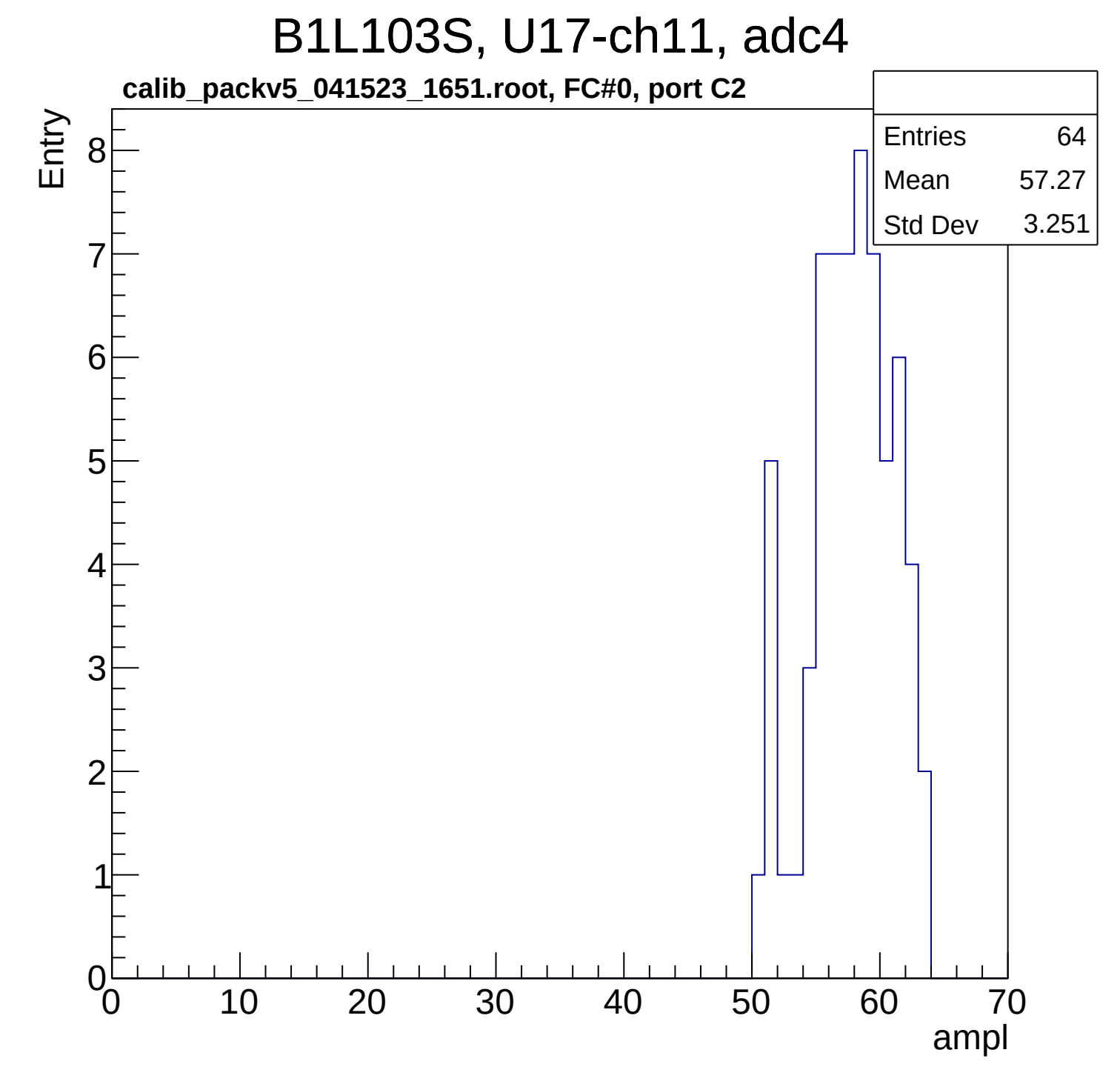
40
50
60
70


B1L103S, U17-ch11, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 57.27
Std Dev 3.251
Entry
ampl
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1
2
3
4
5
6
7
8
0
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60
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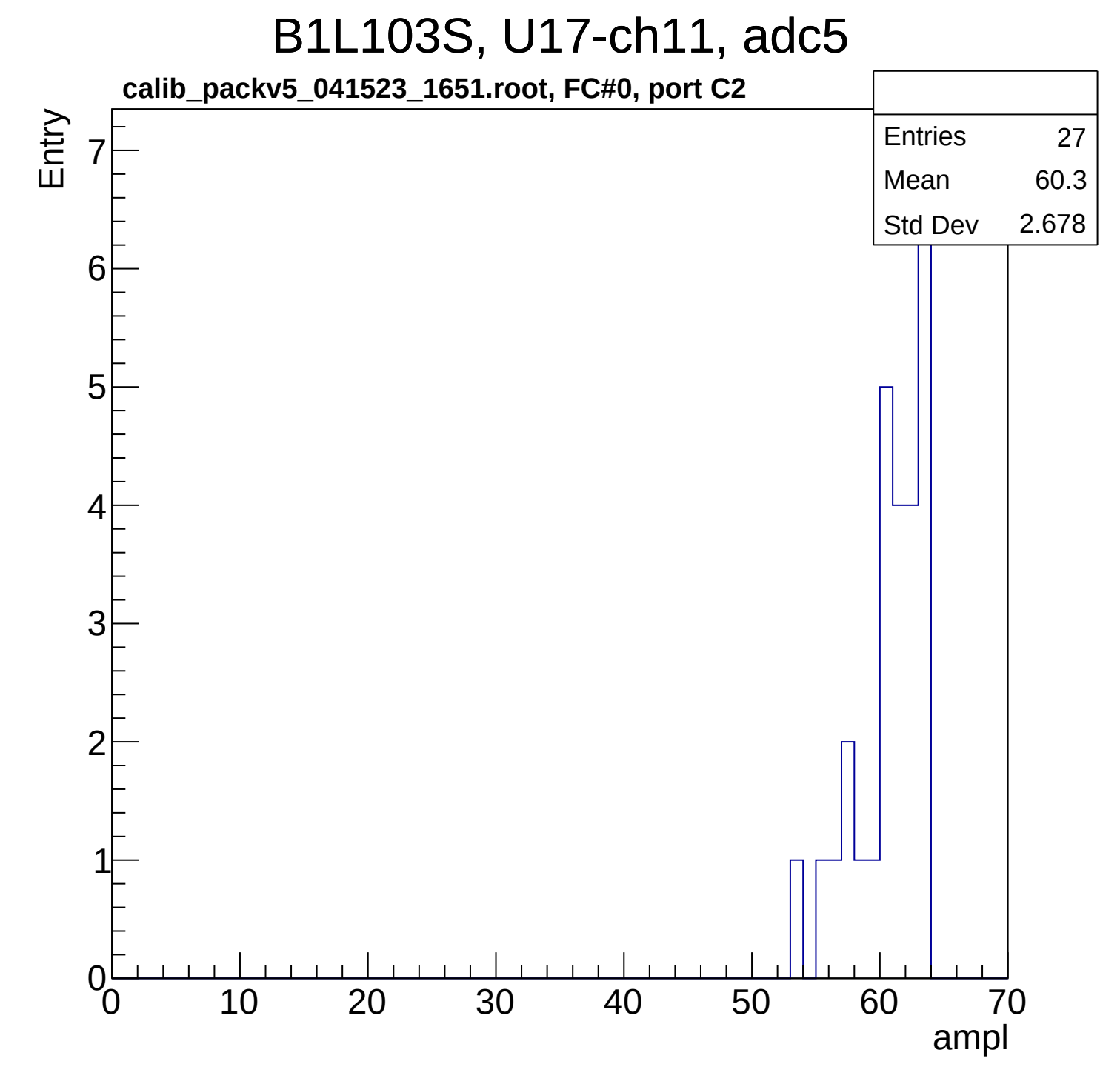
B1L103S, U17-ch11, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 27
Mean 60.3
Std Dev 2.678
Entry
ampl
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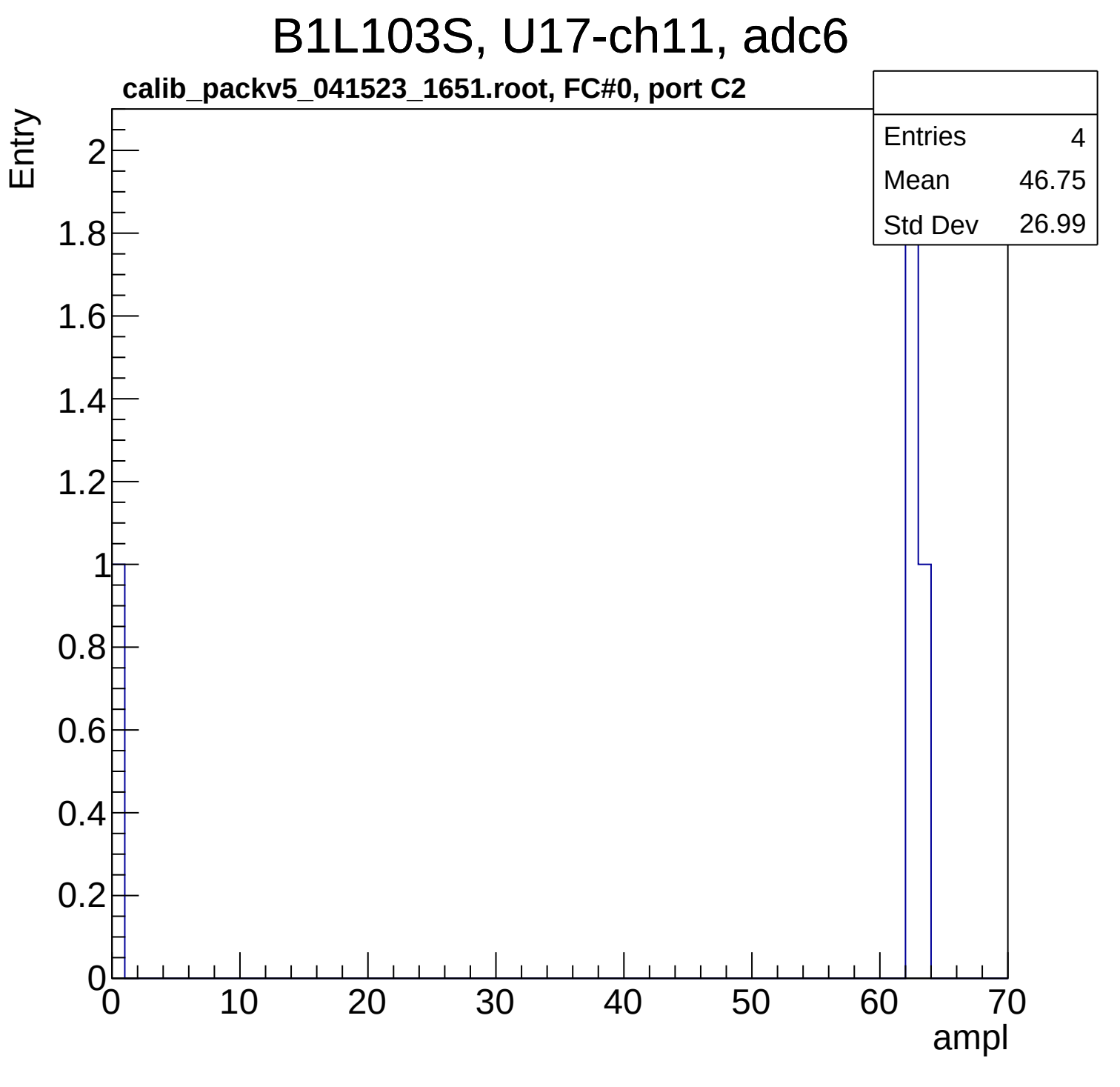
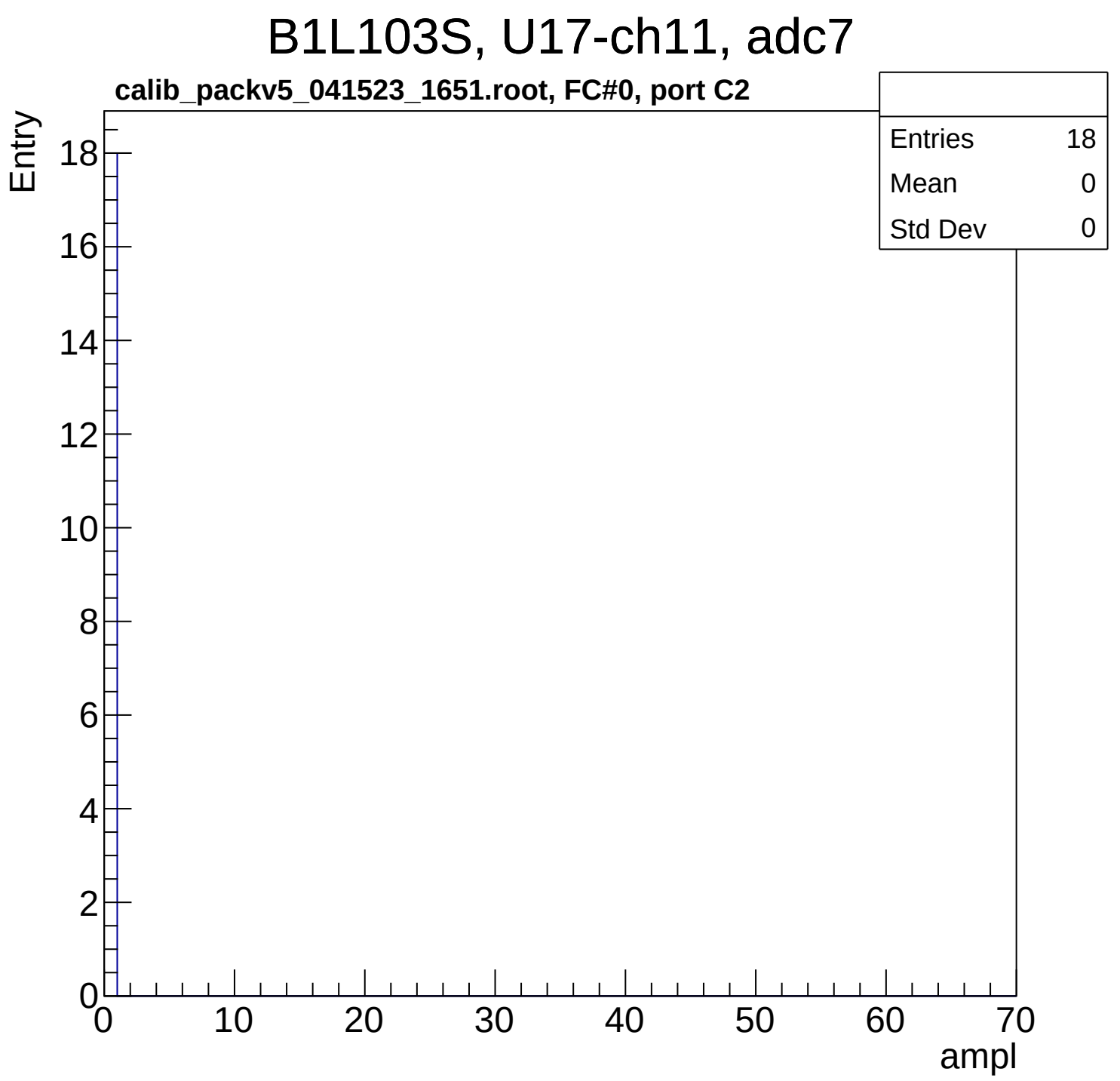
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U17-ch11, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 4
Mean 46.75
Std Dev 26.99
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U17-ch11, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
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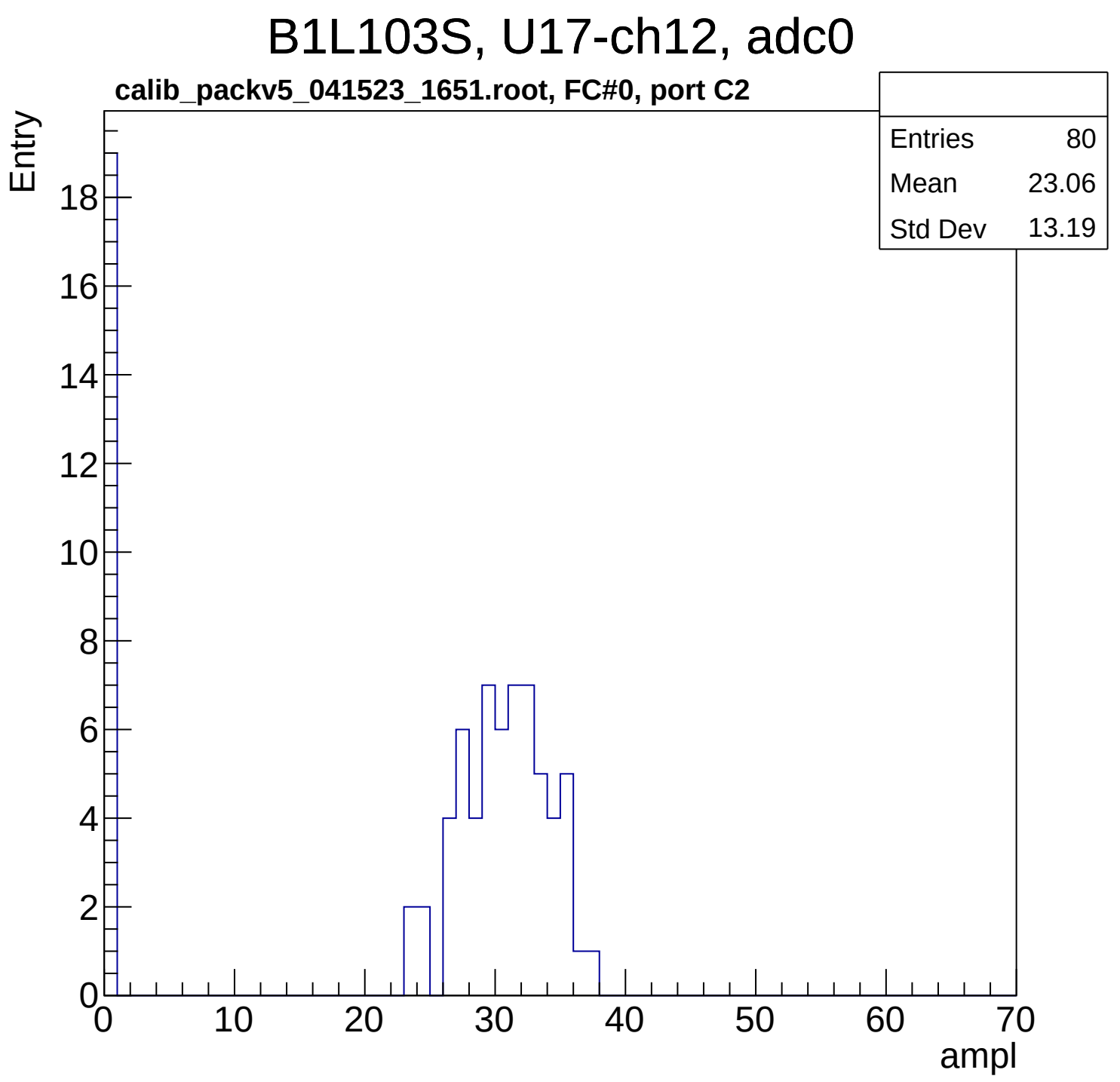
50
60
70
ampl


B1L103S, U17-ch12, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 23.06
Std Dev 13.19
Entry
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2
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6
8
10
12
14
16
18
0
10
20
30
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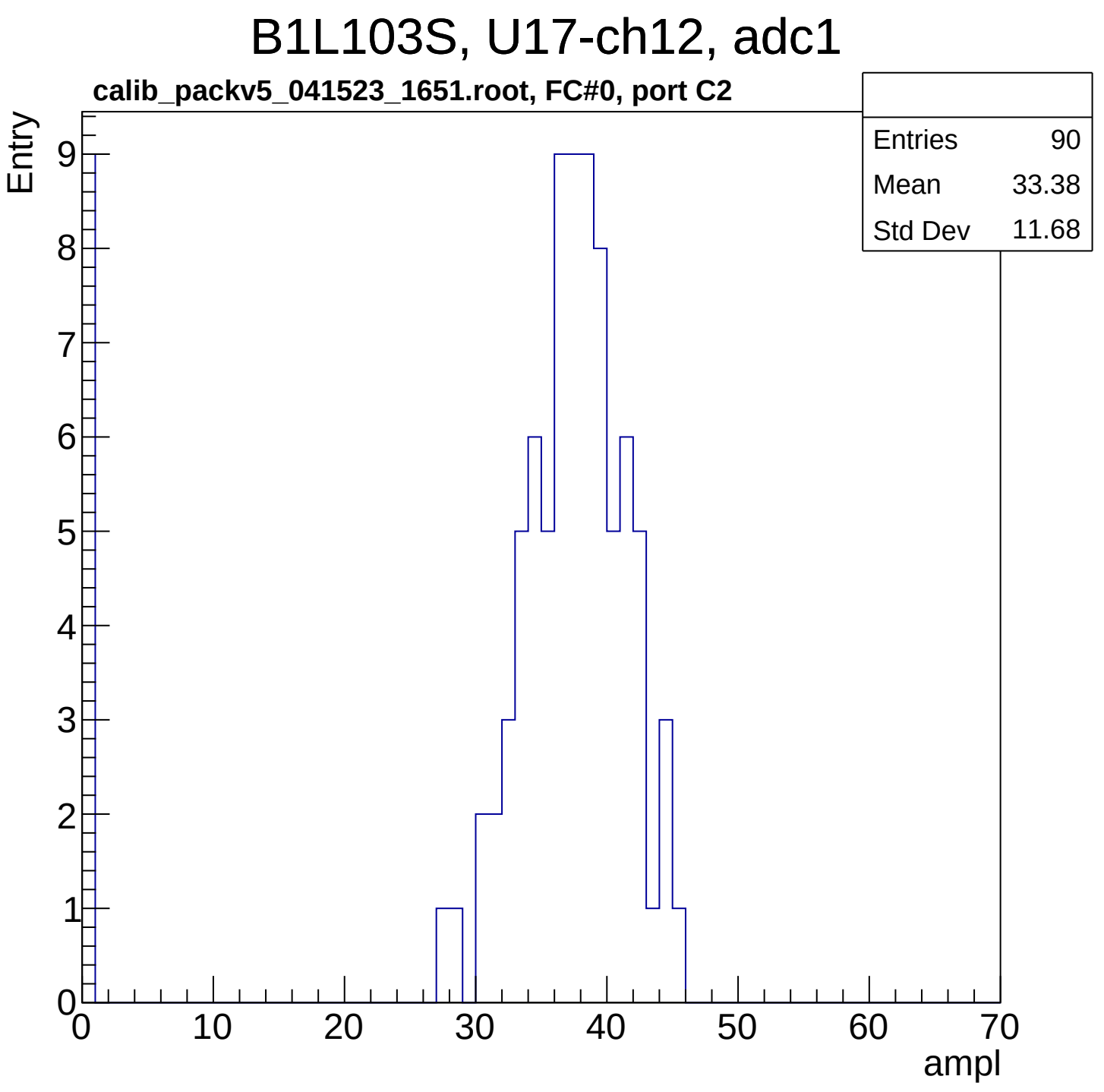
50
60
70
ampl


B1L103S, U17-ch12, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 90
Mean 33.38
Std Dev 11.68
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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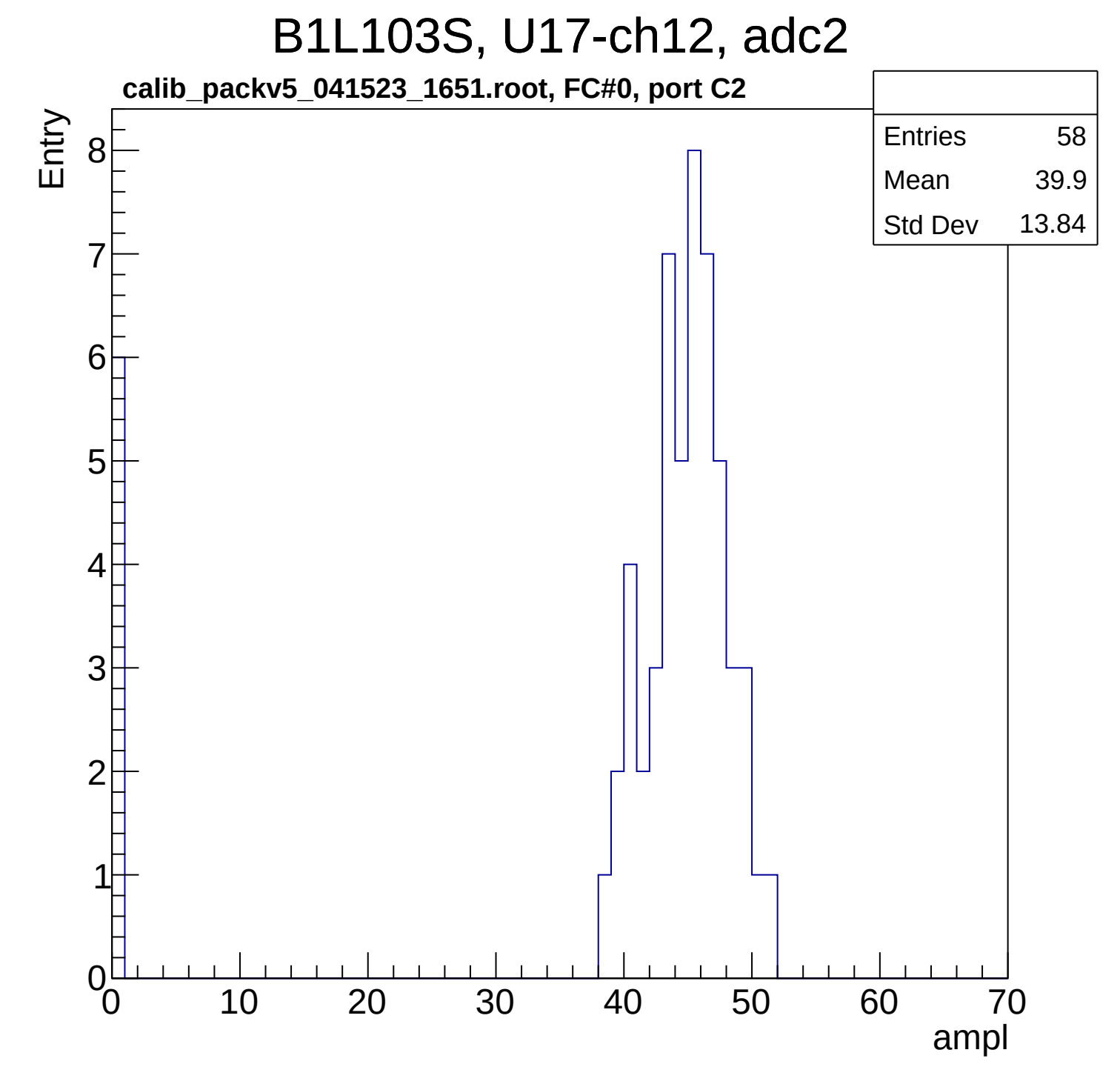
B1L103S, U17-ch12, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 39.9
Std Dev 13.84
Entry
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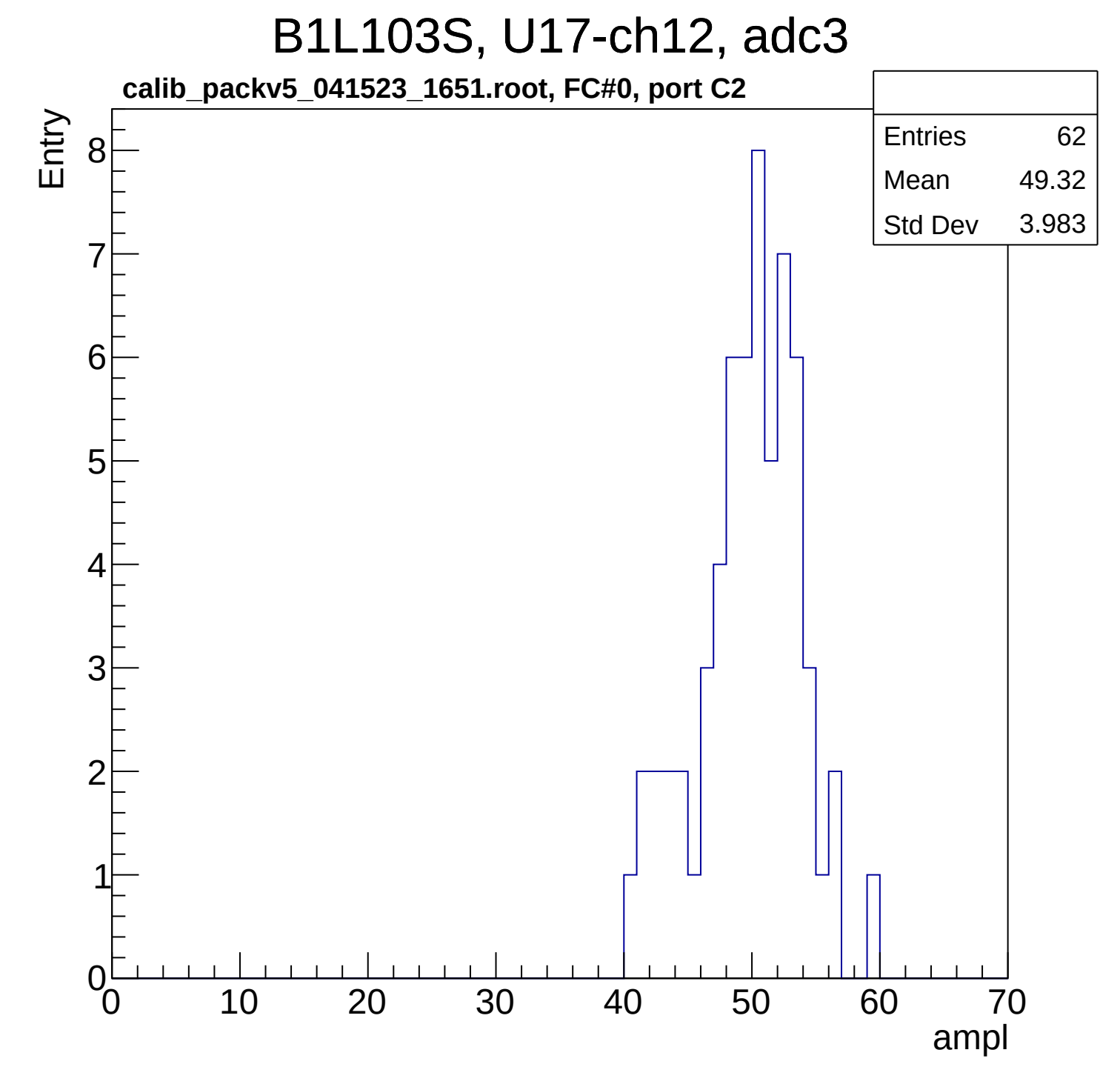
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch12, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 49.32
Std Dev 3.983
Entry
ampl
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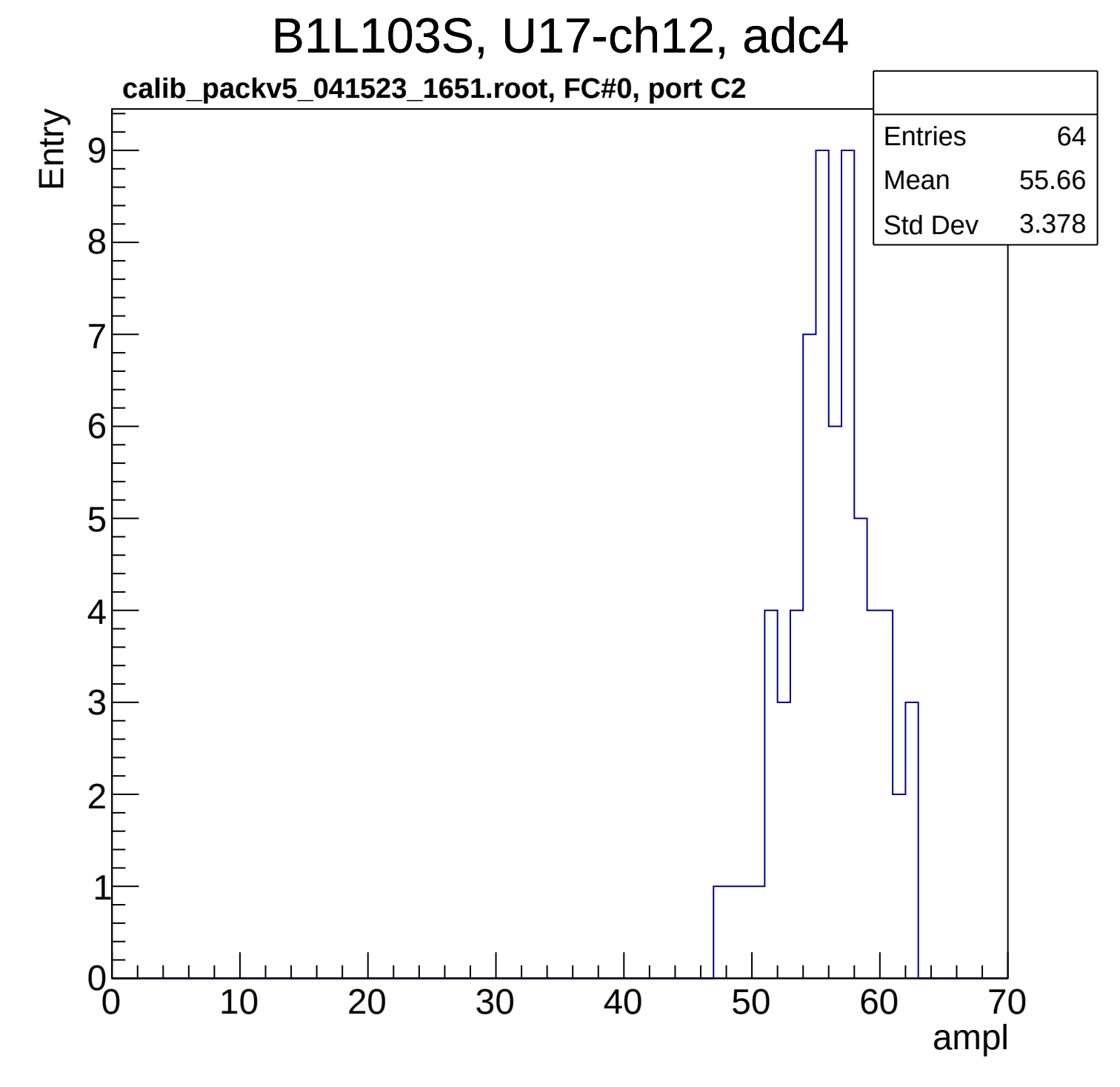
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U17-ch12, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 55.66
Std Dev 3.378
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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40
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60
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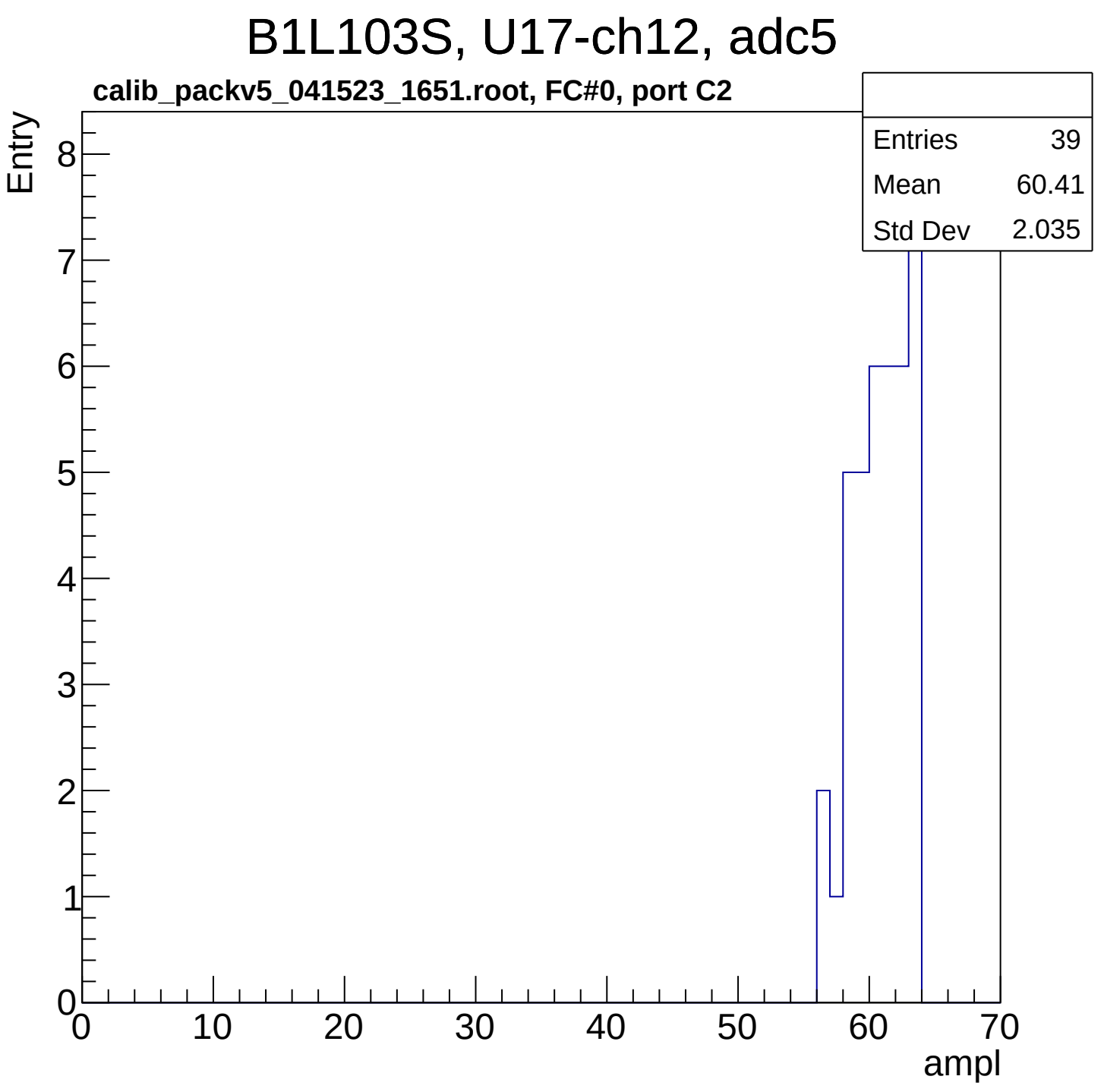
B1L103S, U17-ch12, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 39
Mean 60.41
Std Dev 2.035
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
30
40
50
60
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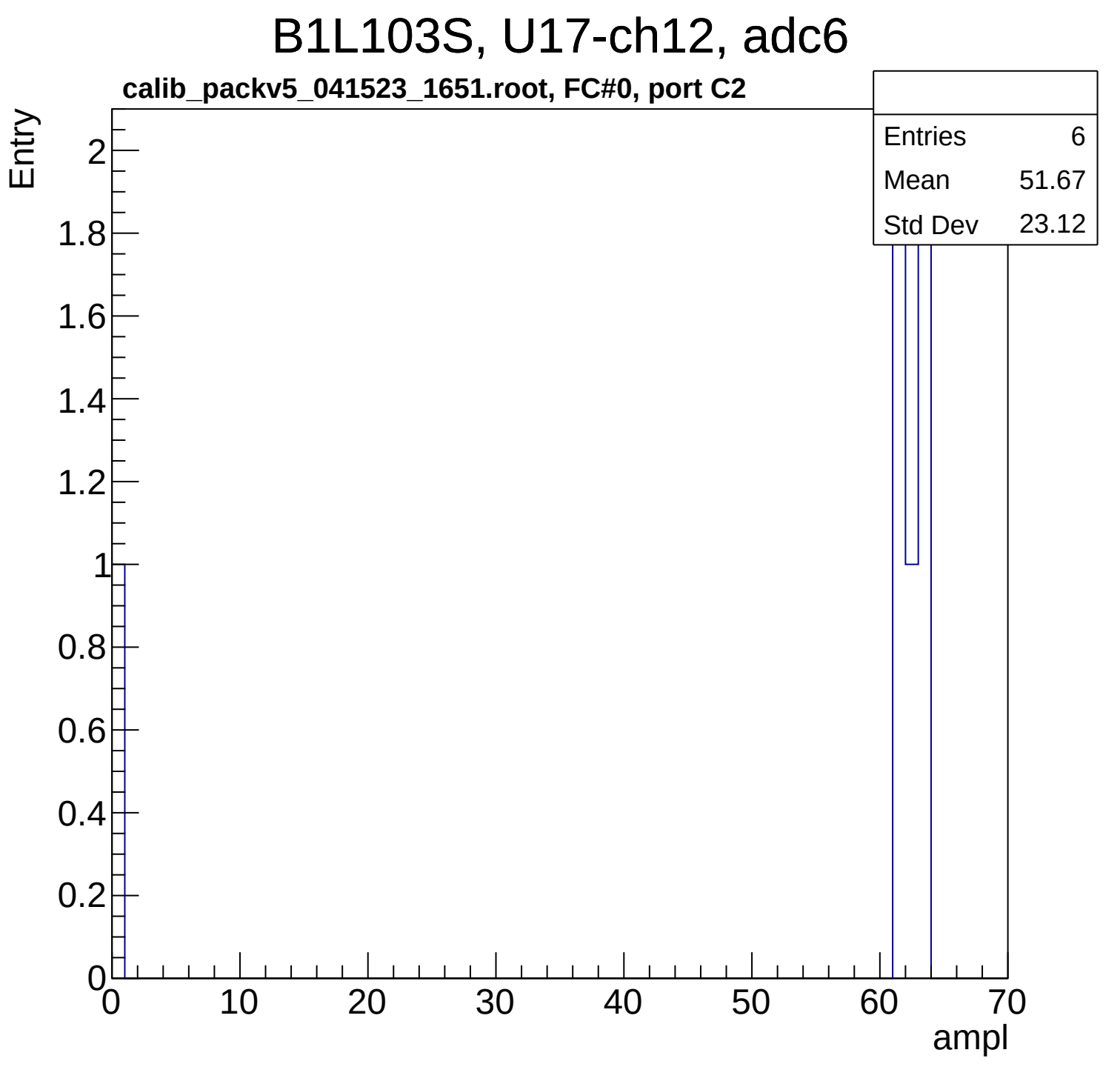
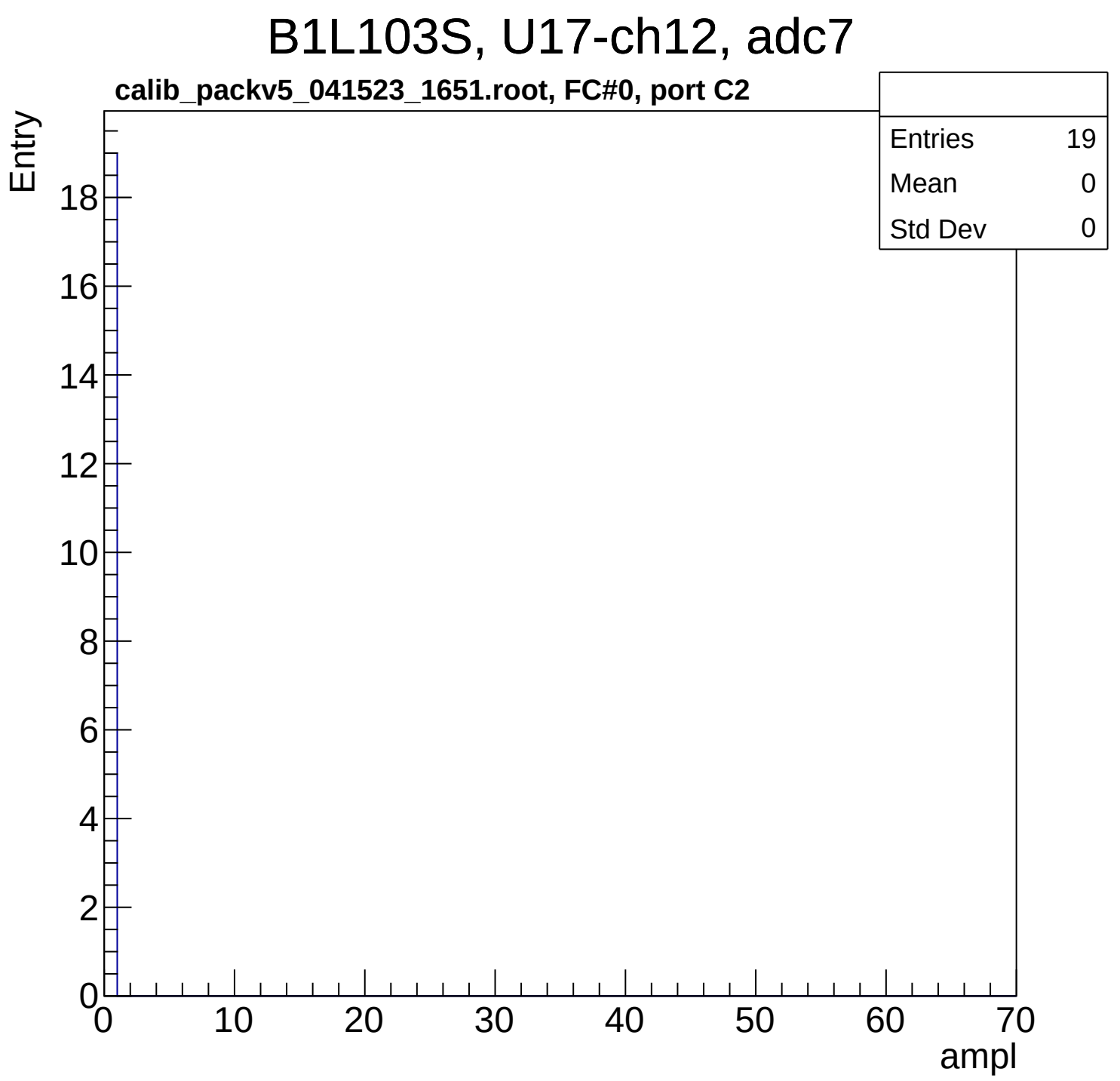
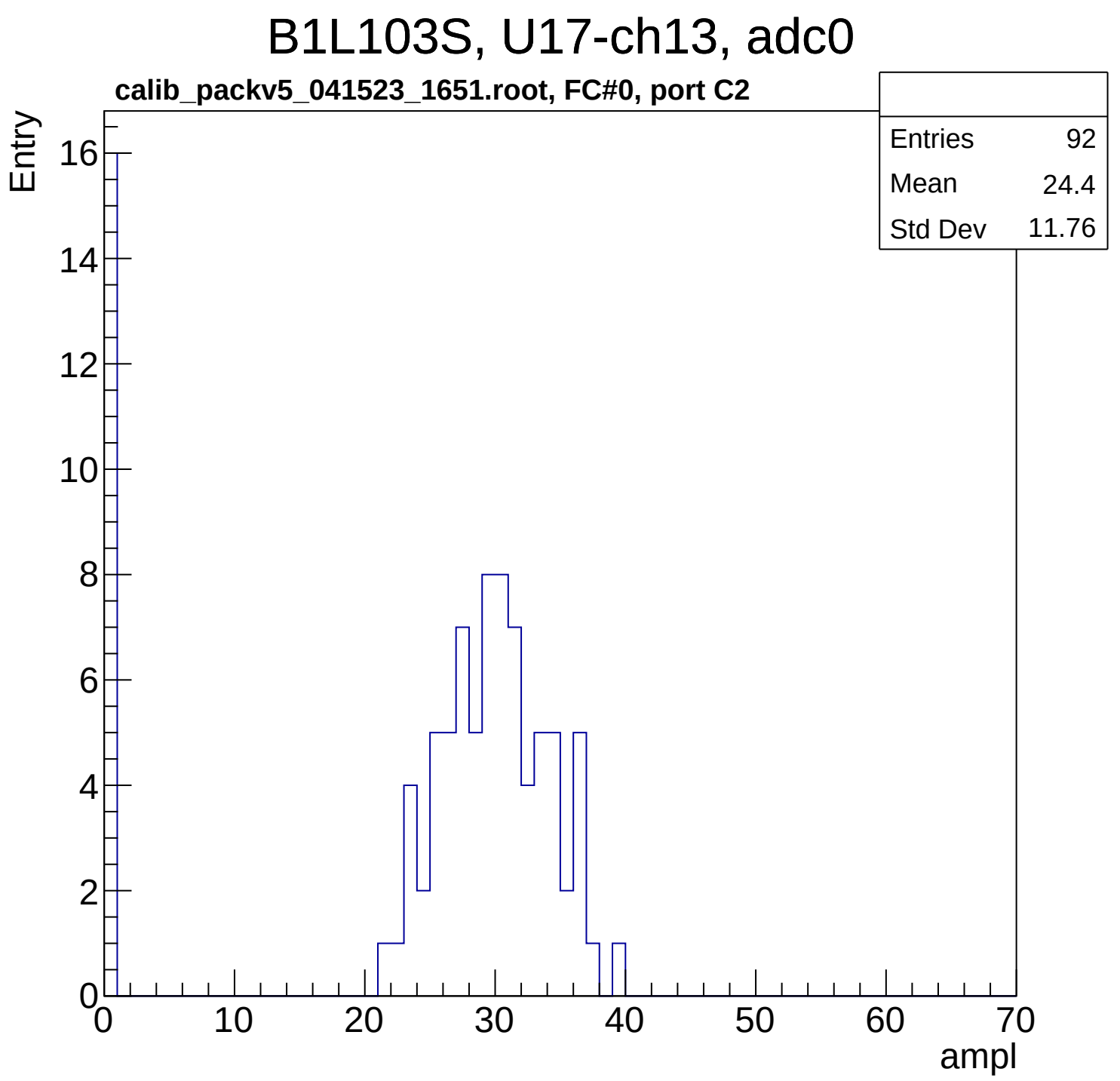

B1L103S, U17-ch12, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 51.67
Std Dev 23.12
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U17-ch12, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch13, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 92
Mean 24.4
Std Dev 11.76
Entry
ampl
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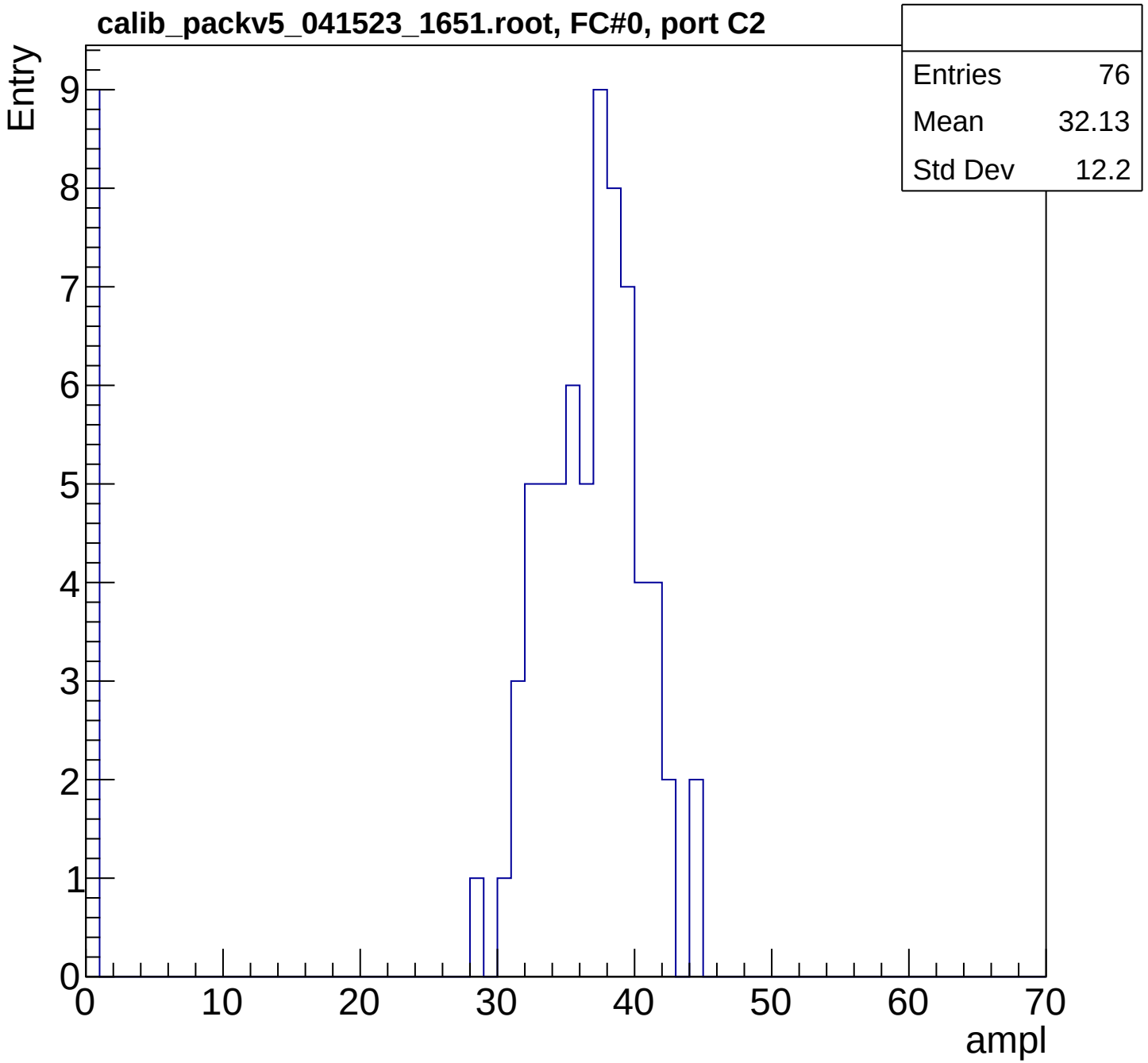
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70


B1L103S, U17-ch13, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 32.13
Std Dev 12.2
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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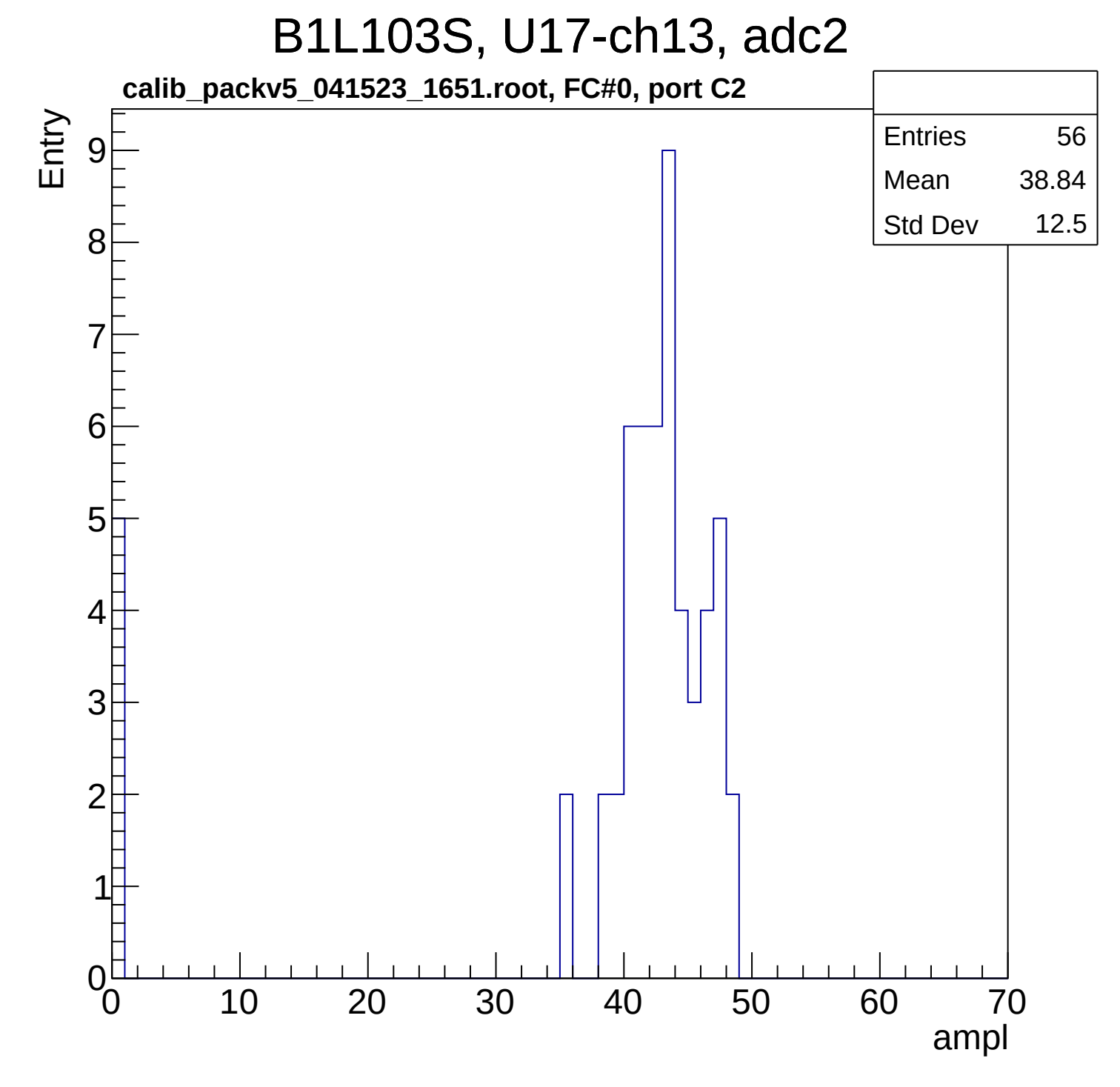
B1L103S, U17-ch13, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 38.84
Std Dev 12.5
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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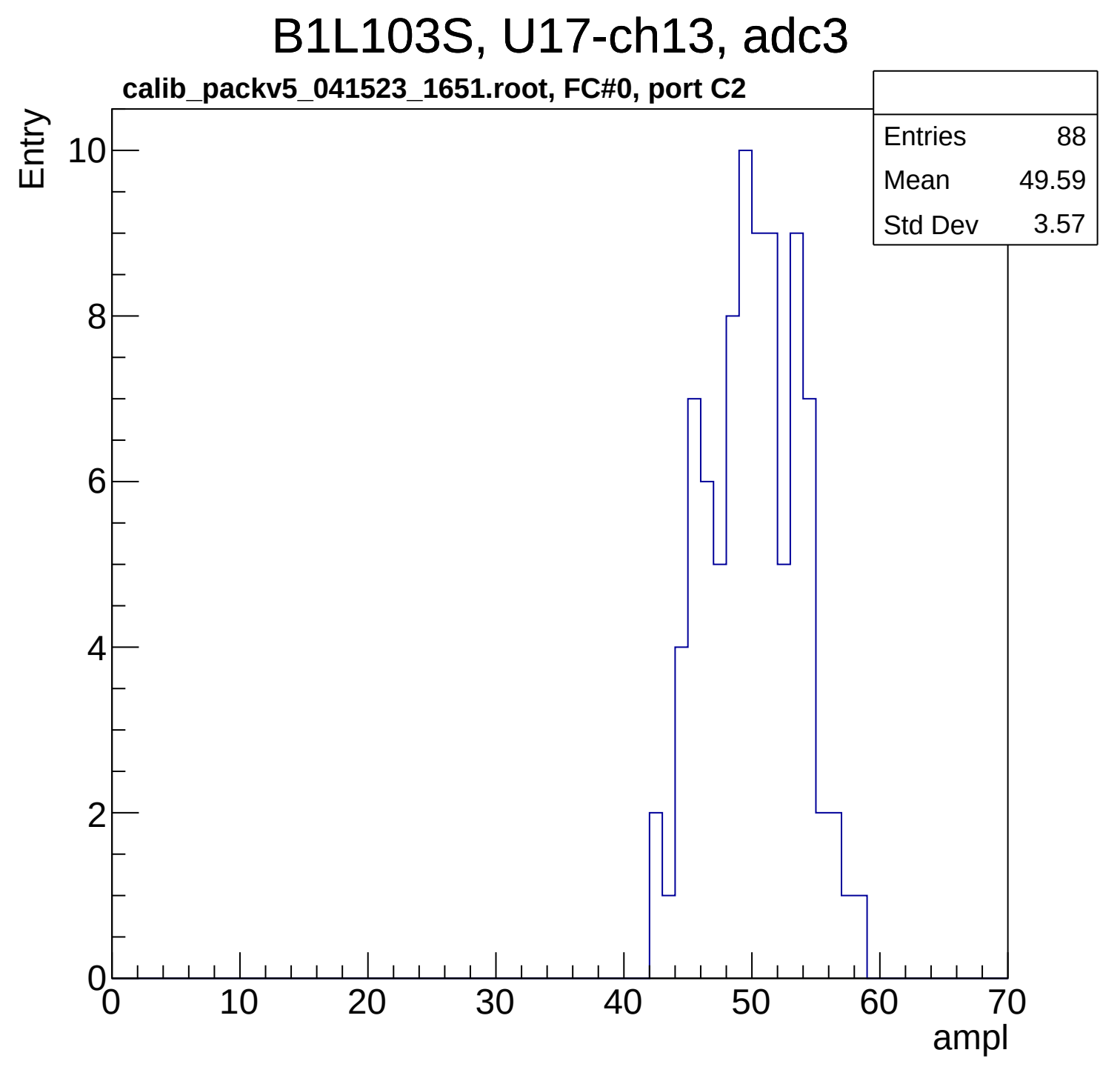
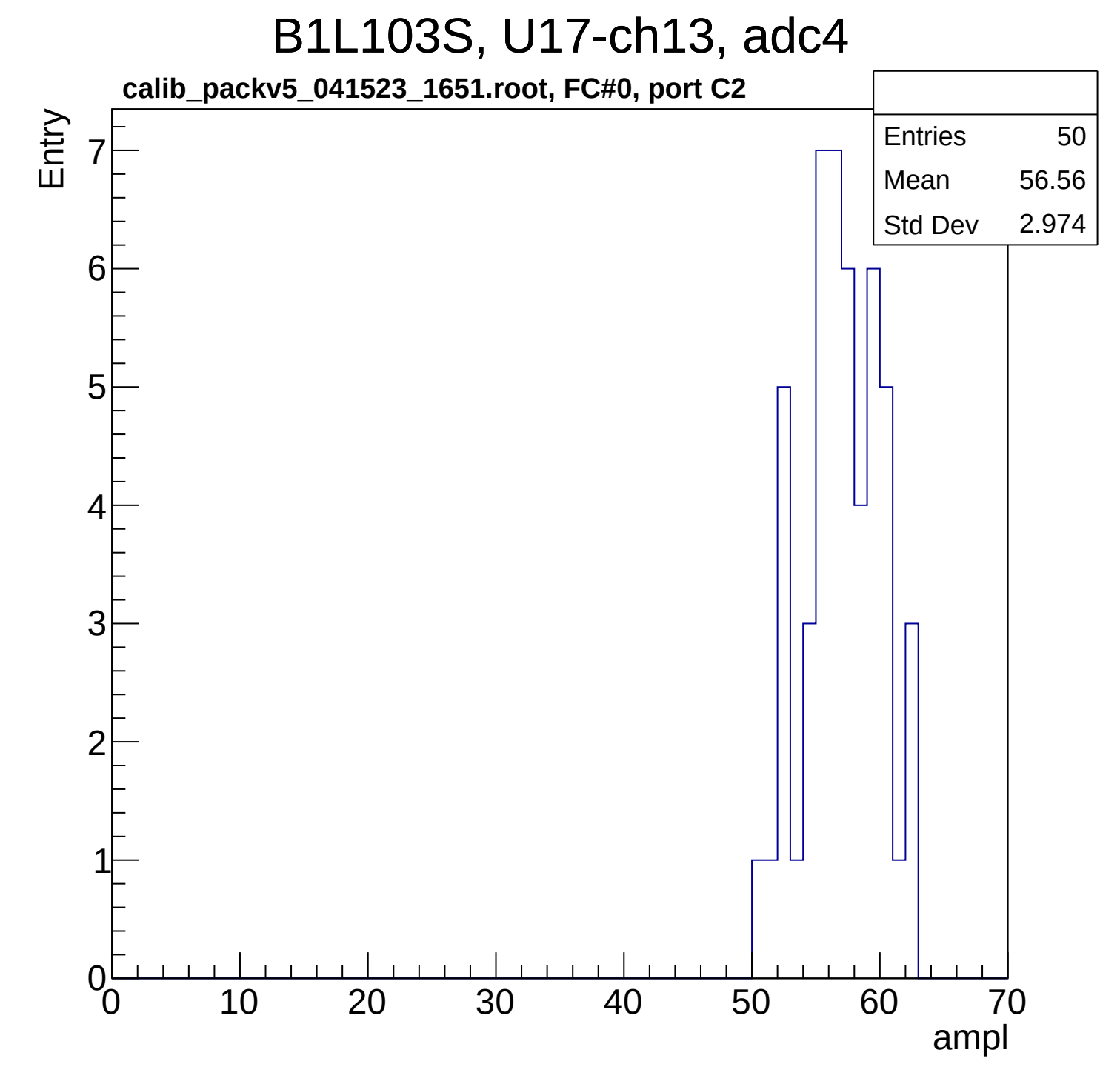

B1L103S, U17-ch13, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 88
Mean 49.59
Std Dev 3.57
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U17-ch13, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 56.56
Std Dev 2.974
Entry
ampl
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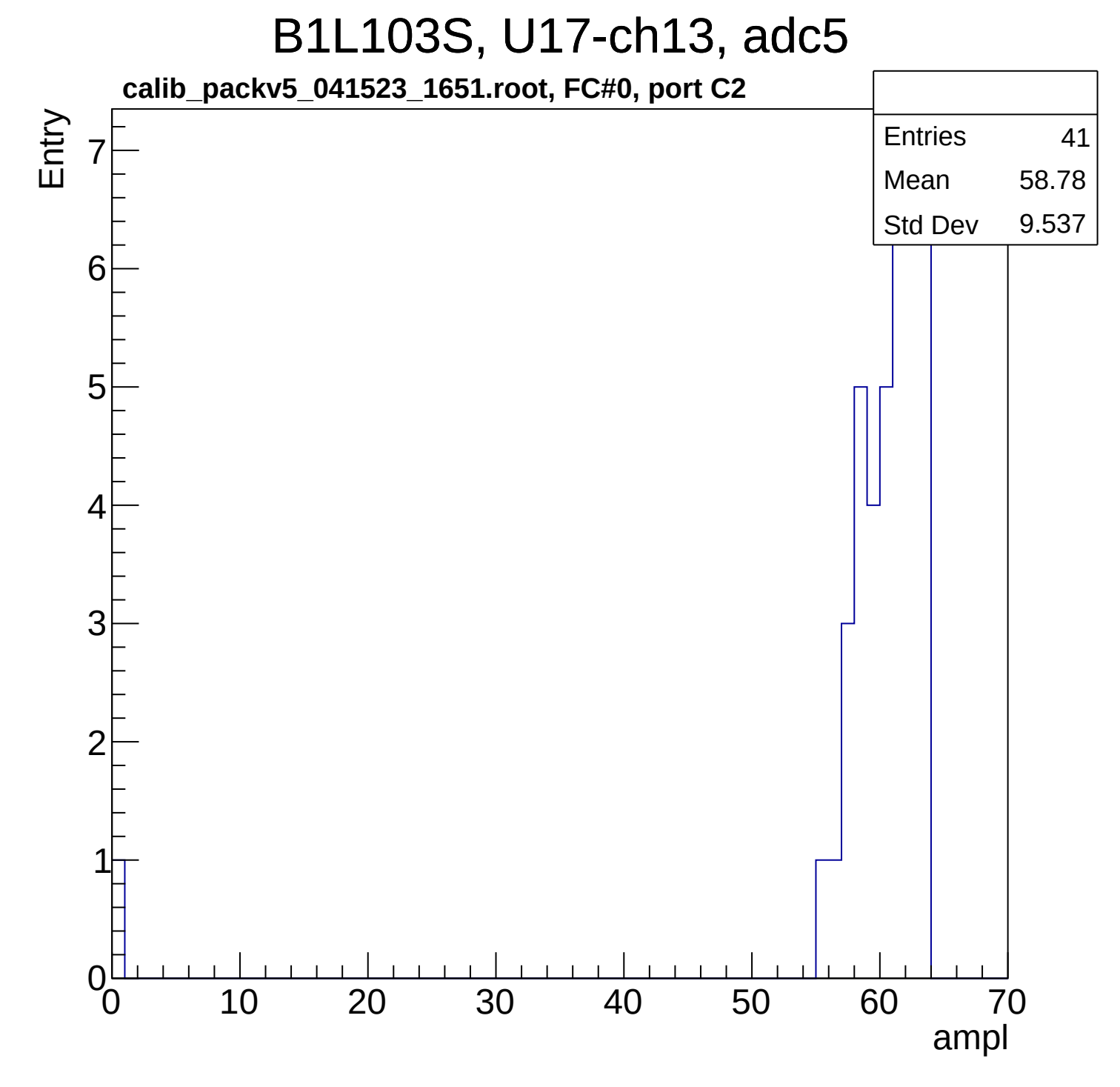
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U17-ch13, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 41
Mean 58.78
Std Dev 9.537
Entry
ampl
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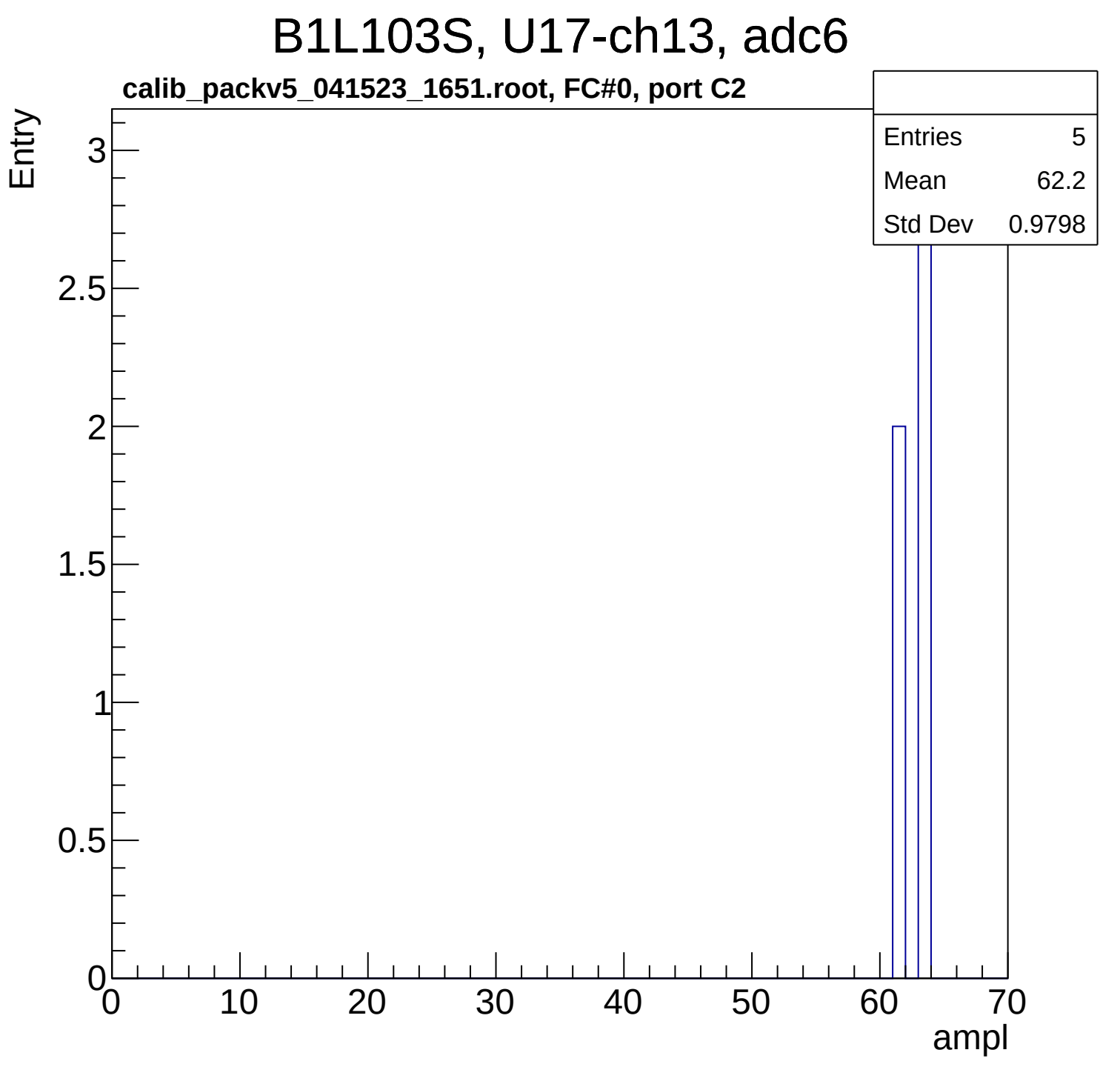
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U17-ch13, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 5
Mean 62.2
Std Dev 0.9798
Entry
ampl
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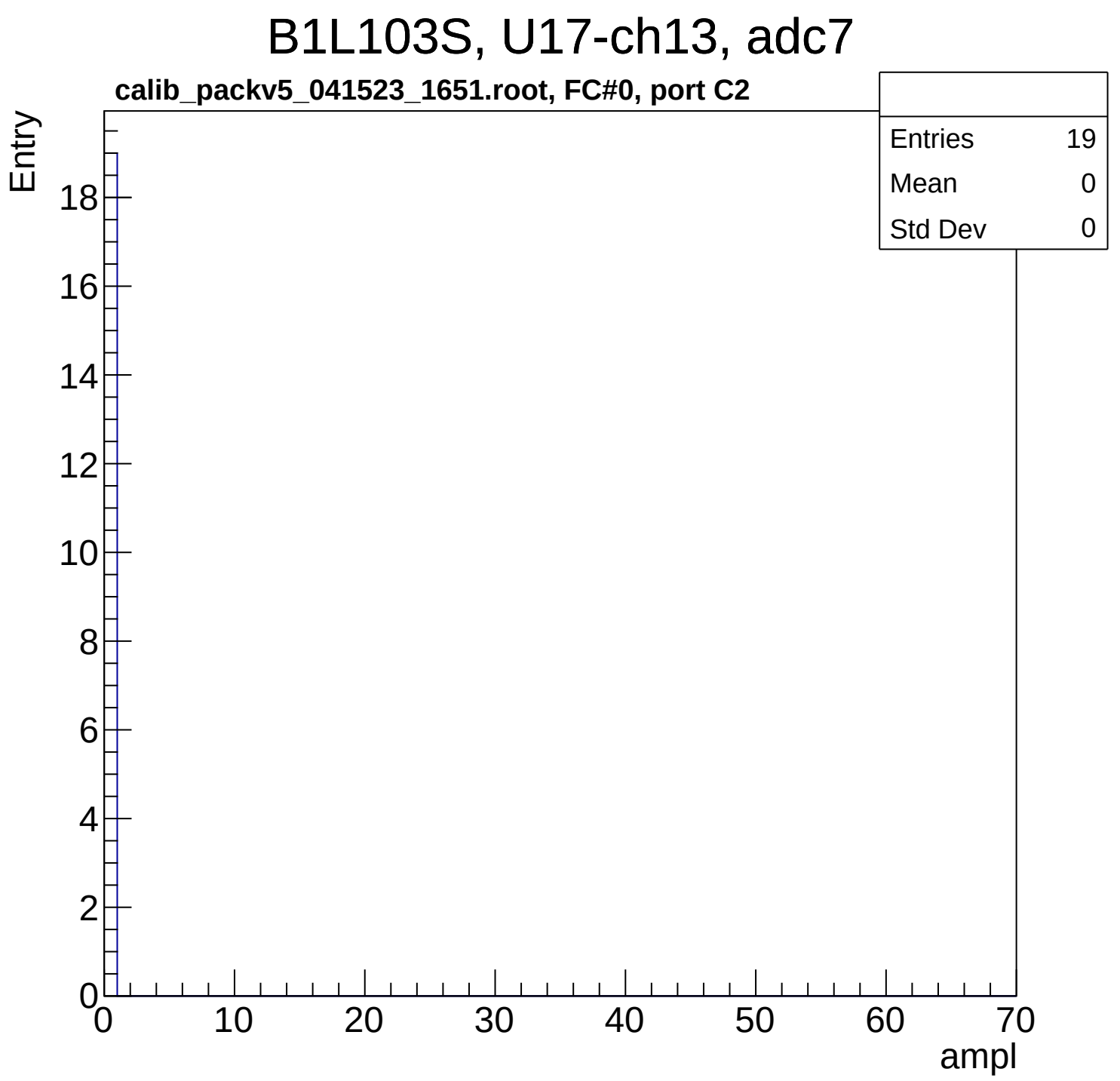
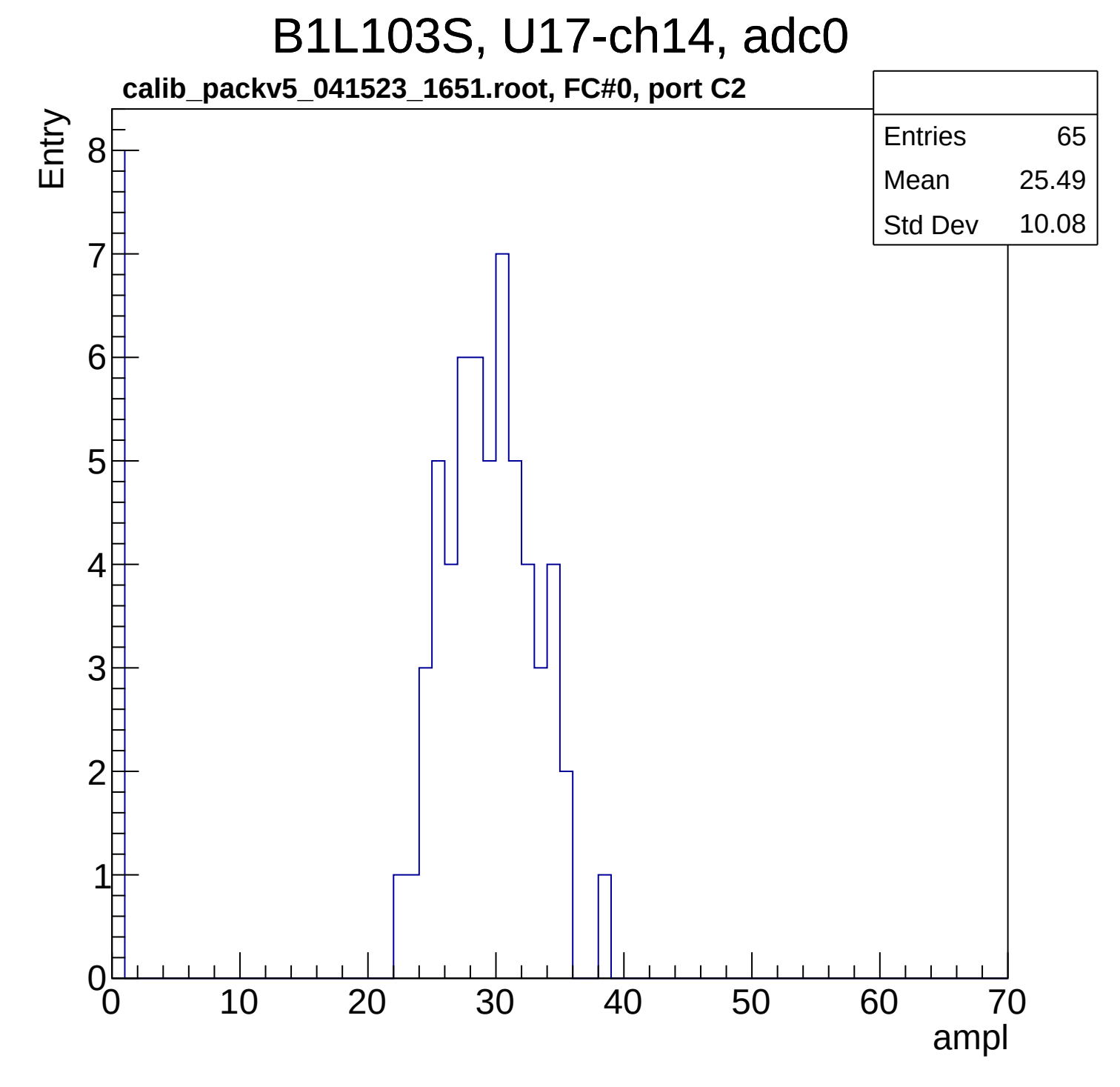
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U17-ch13, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch14, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 25.49
Std Dev 10.08
Entry
ampl
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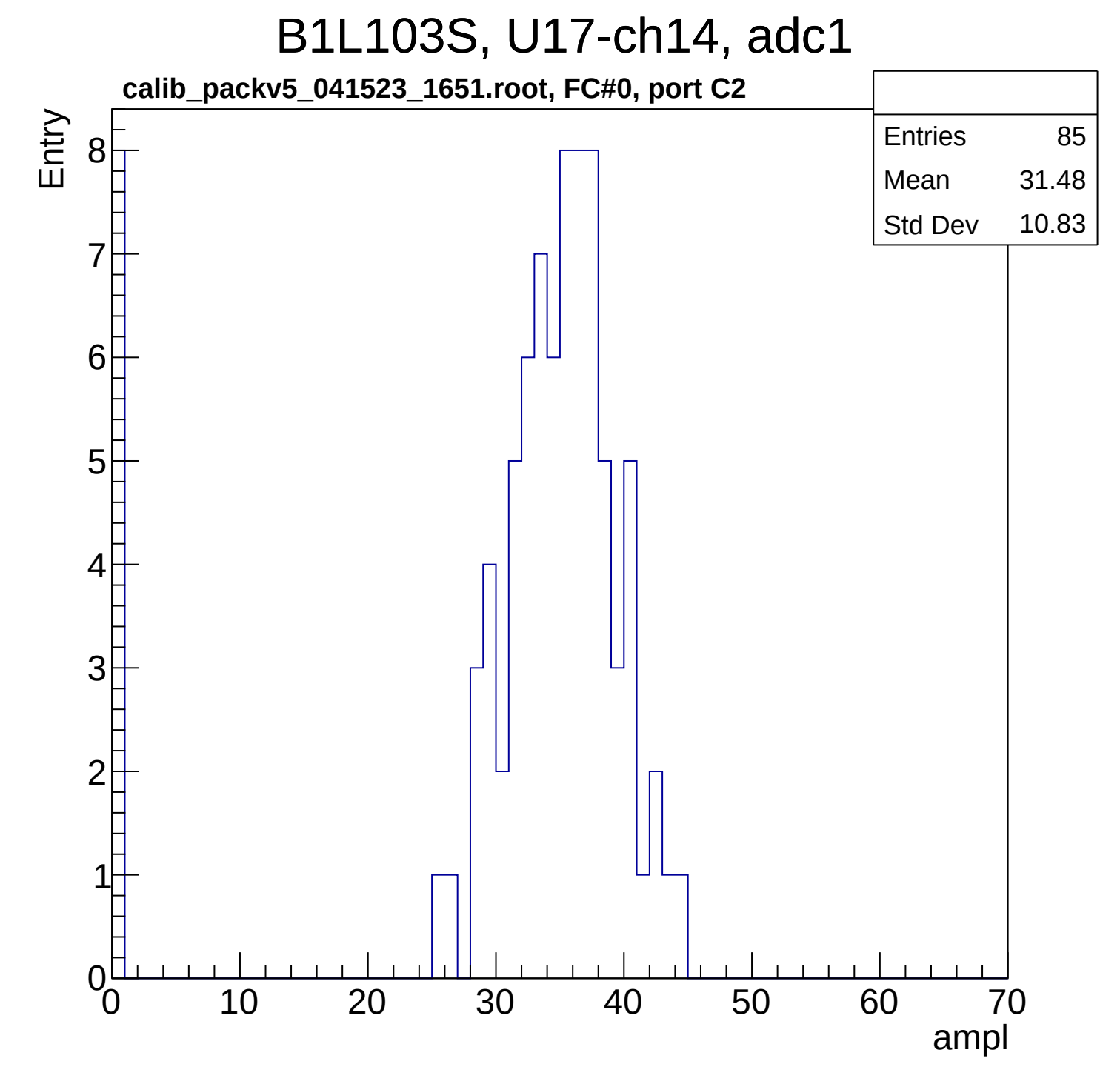
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U17-ch14, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 31.48
Std Dev 10.83
Entry
ampl
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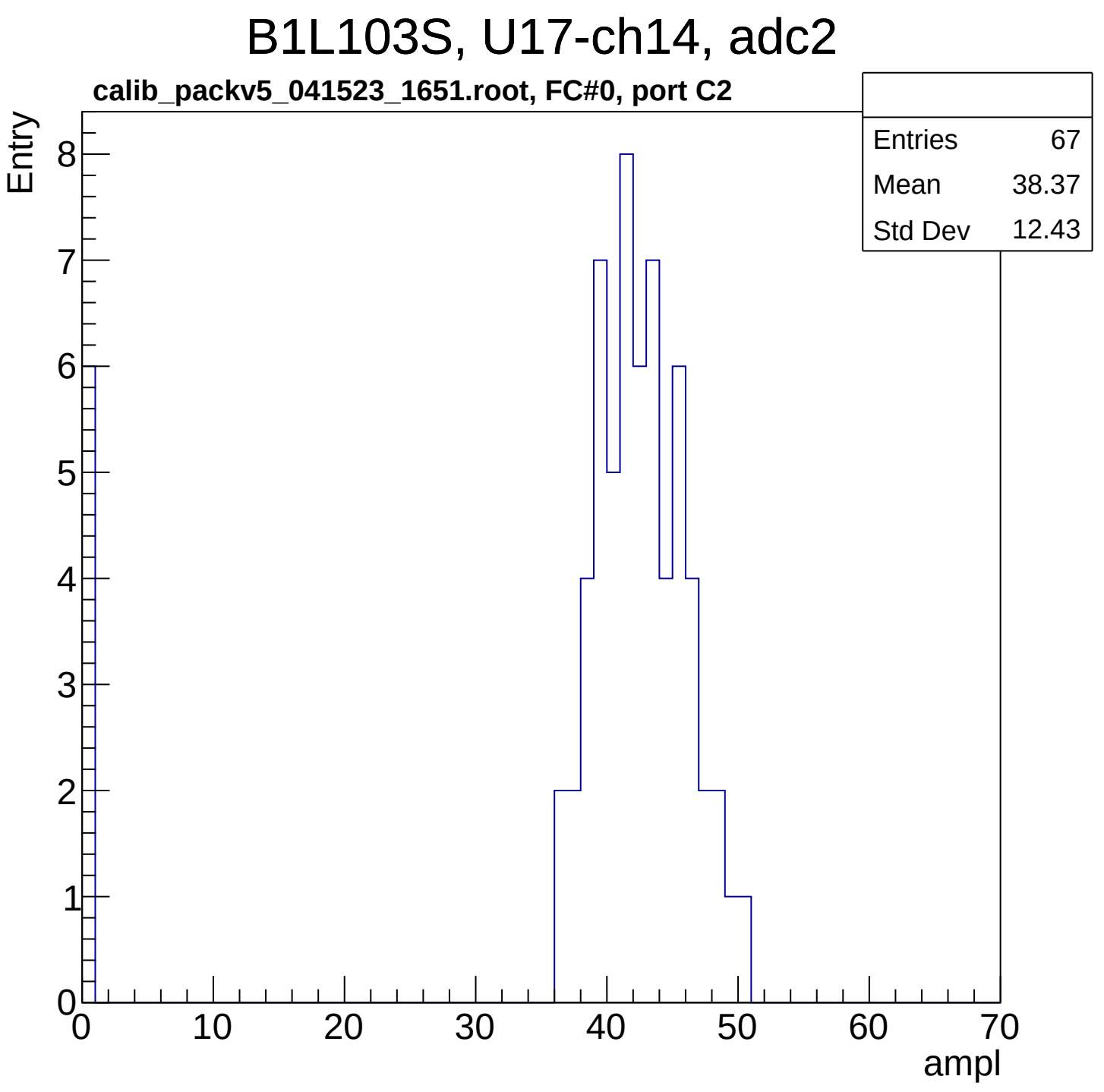
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U17-ch14, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 38.37
Std Dev 12.43
Entry
ampl
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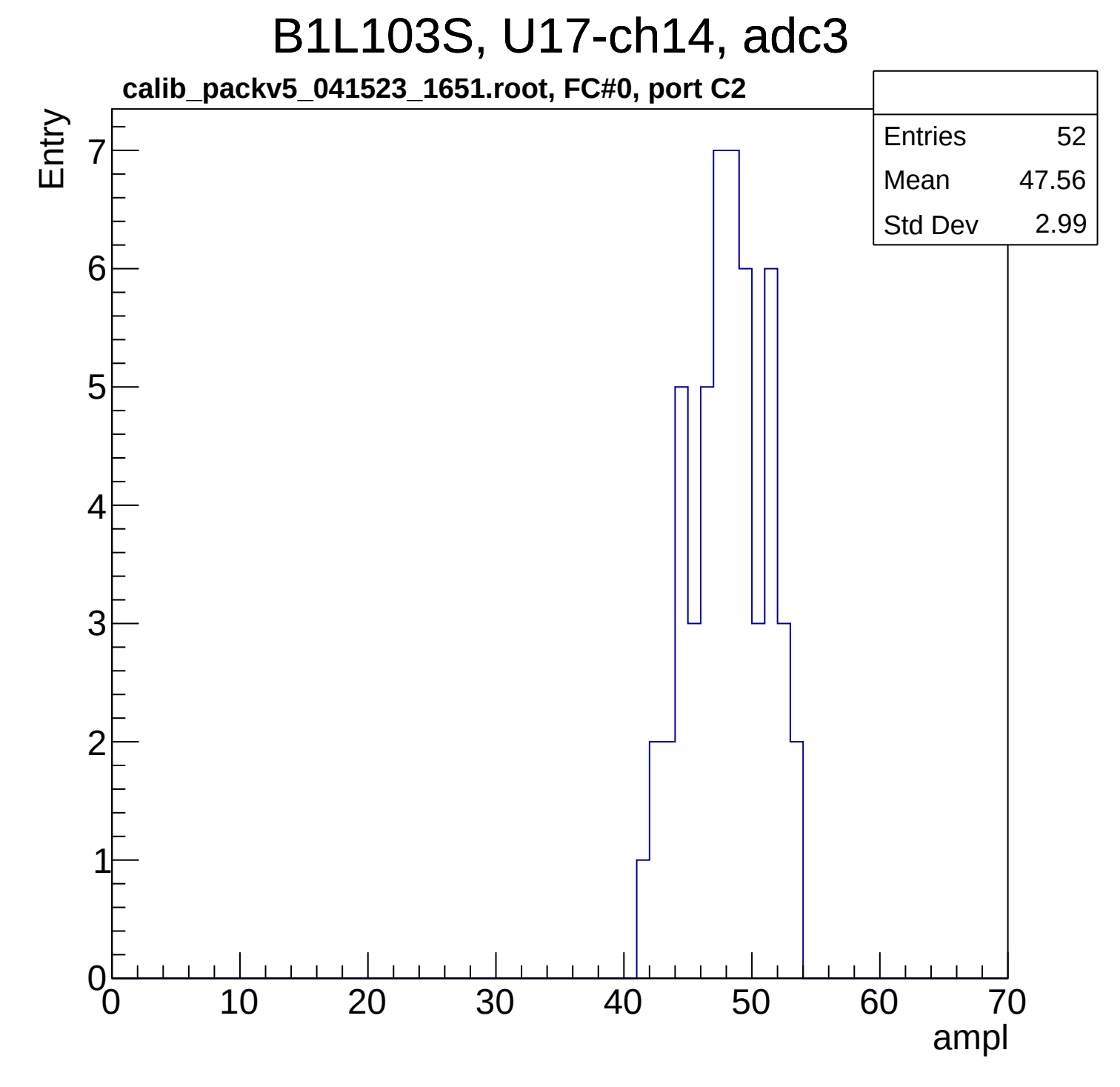
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U17-ch14, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 47.56
Std Dev 2.99
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
30
40
50
60
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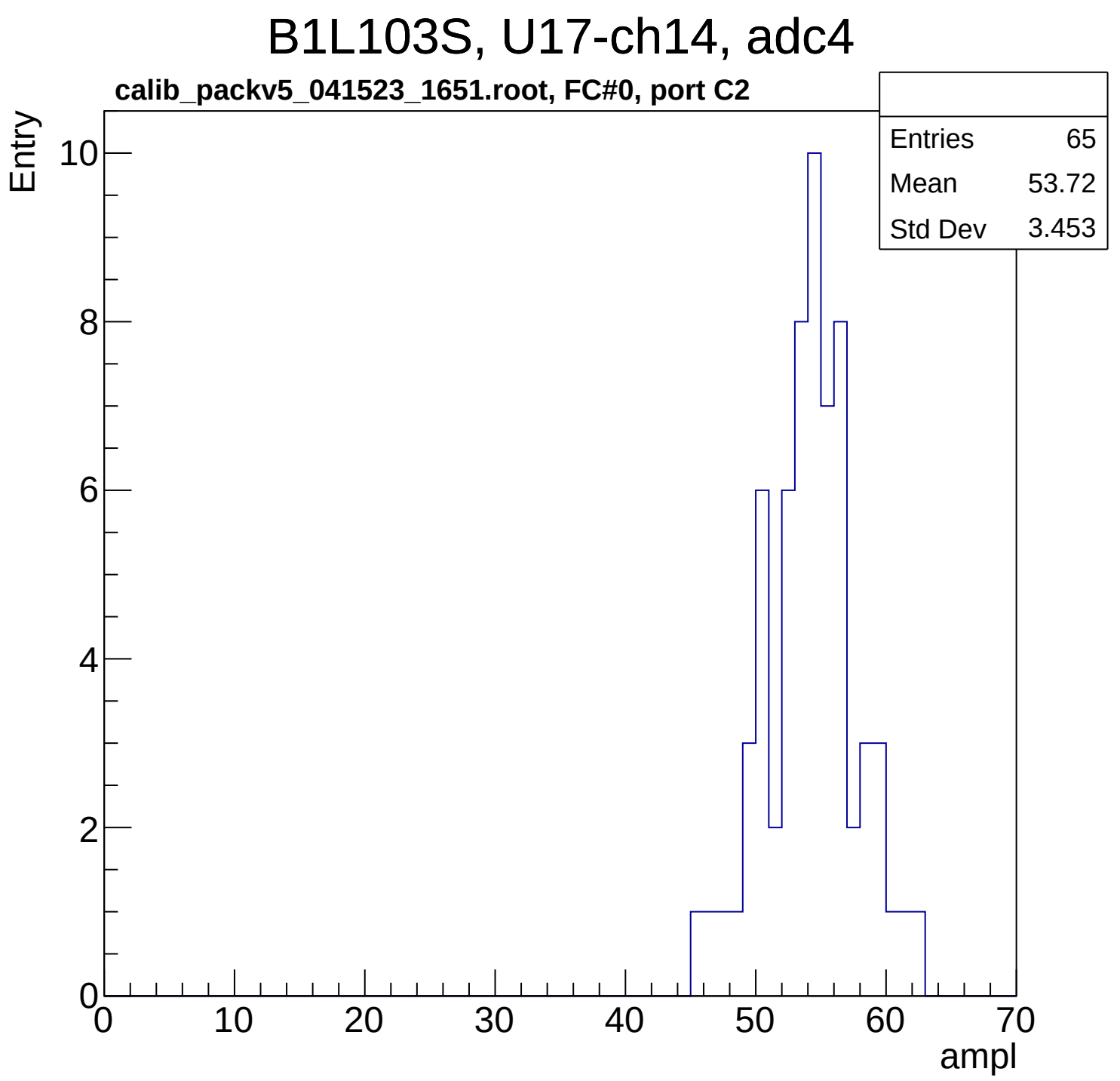
B1L103S, U17-ch14, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 53.72
Std Dev 3.453
Entry
ampl
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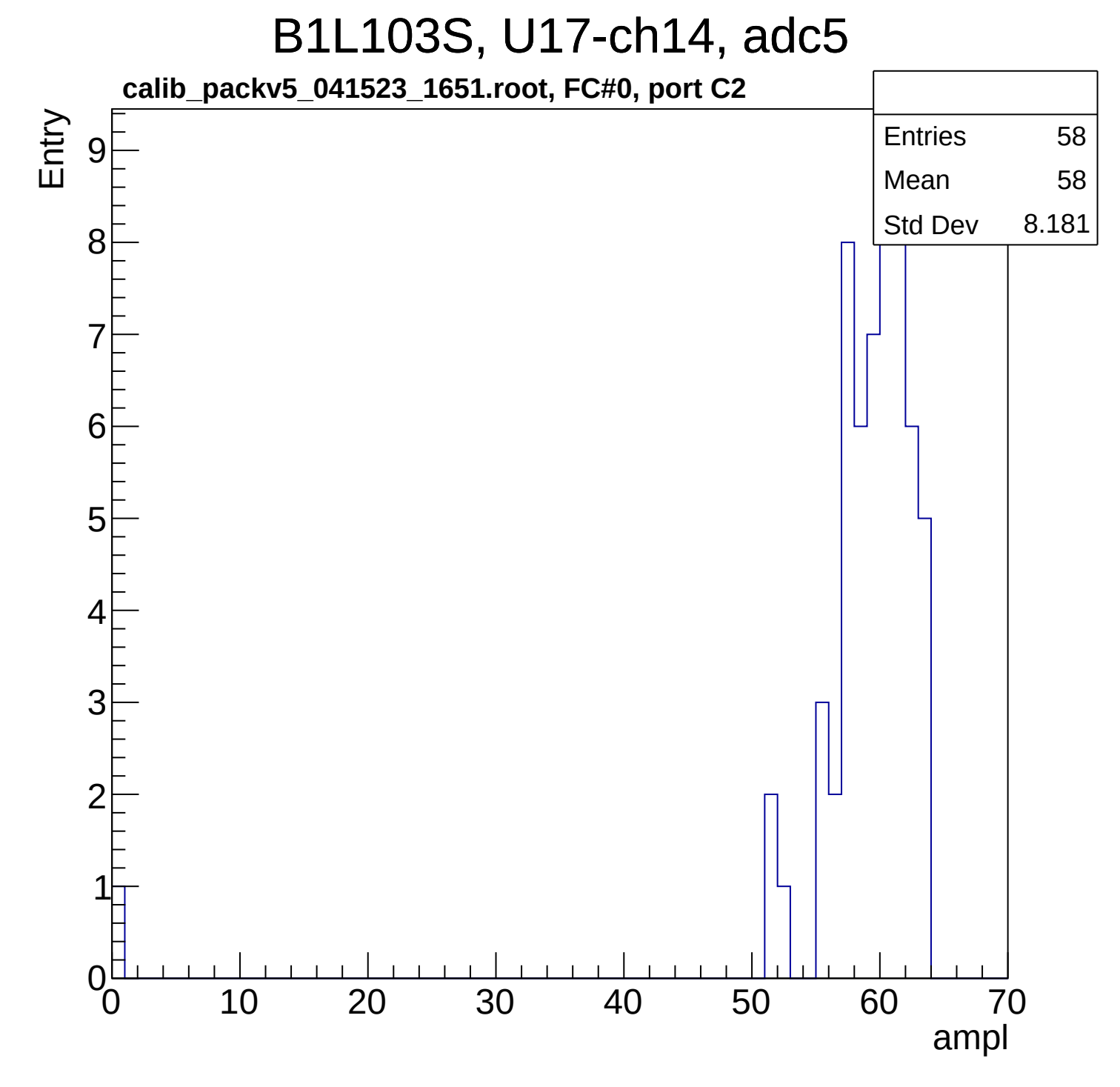
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U17-ch14, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 58
Std Dev 8.181
Entry
ampl
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2
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4
5
6
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8
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0
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40
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60
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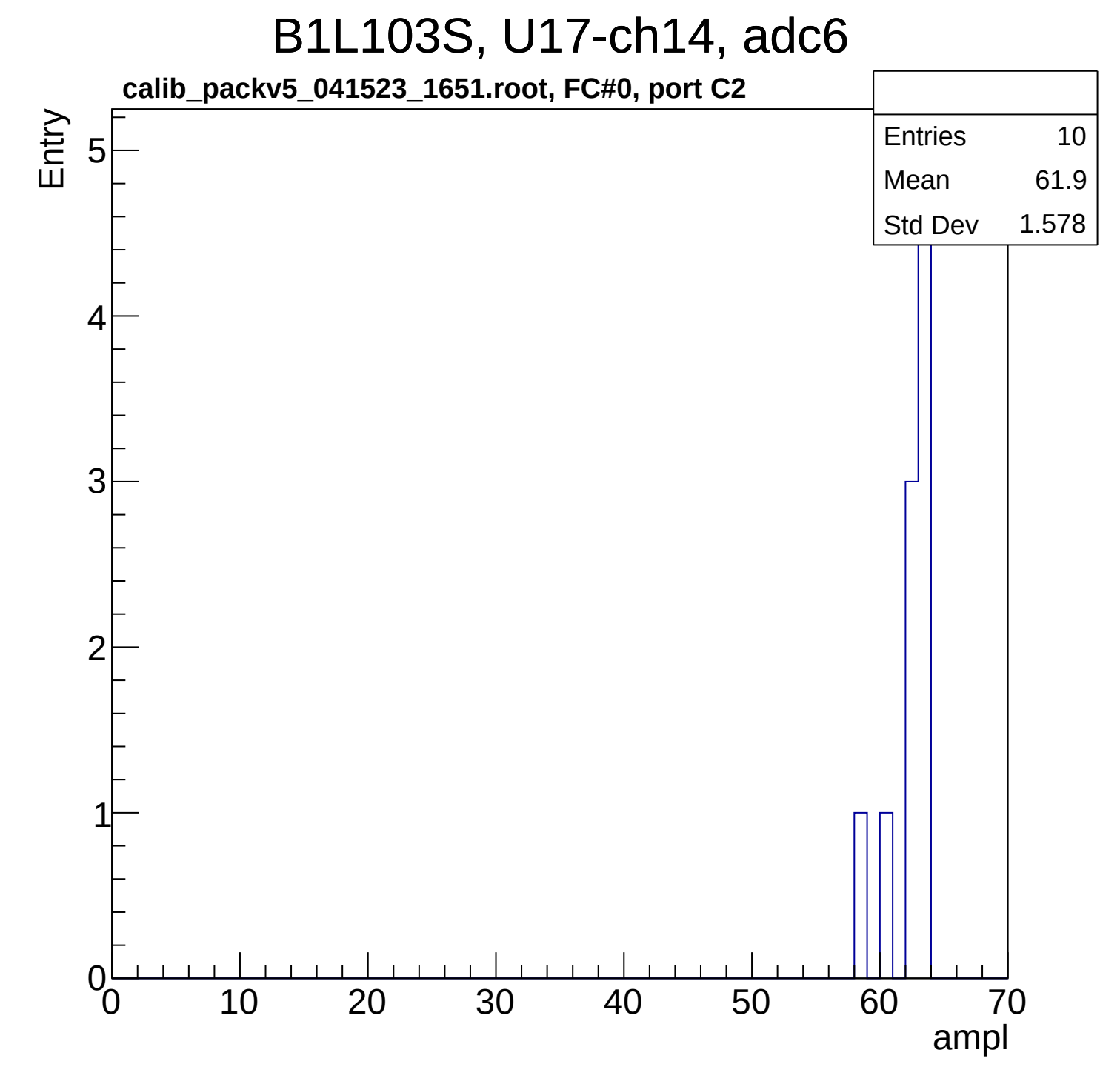
B1L103S, U17-ch14, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 61.9
Std Dev 1.578
Entry
ampl
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1
2
3
4
5
0
10
20
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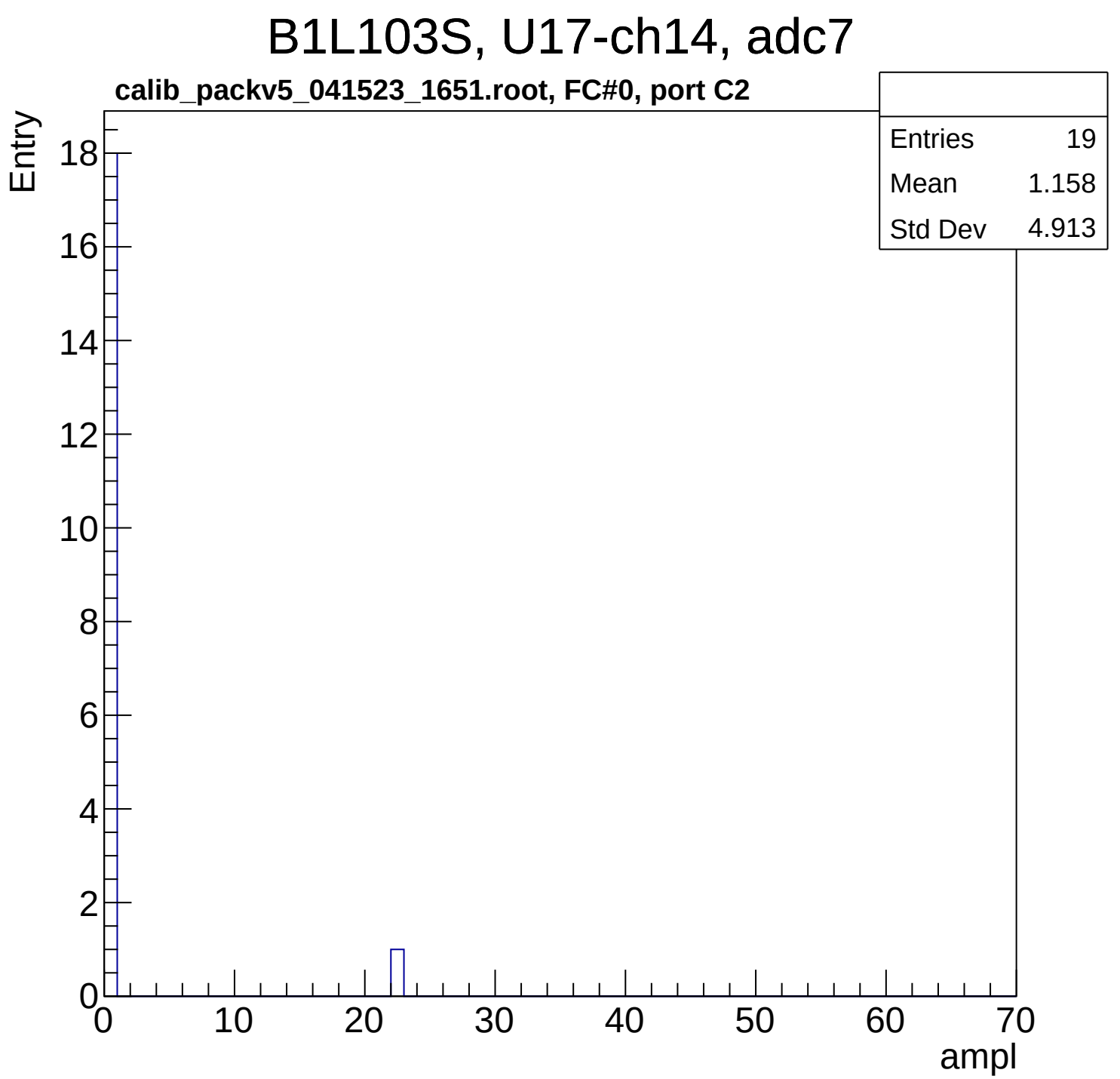
40
50
60
70


B1L103S, U17-ch14, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.158
Std Dev 4.913
Entry
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6
8
10
12
14
16
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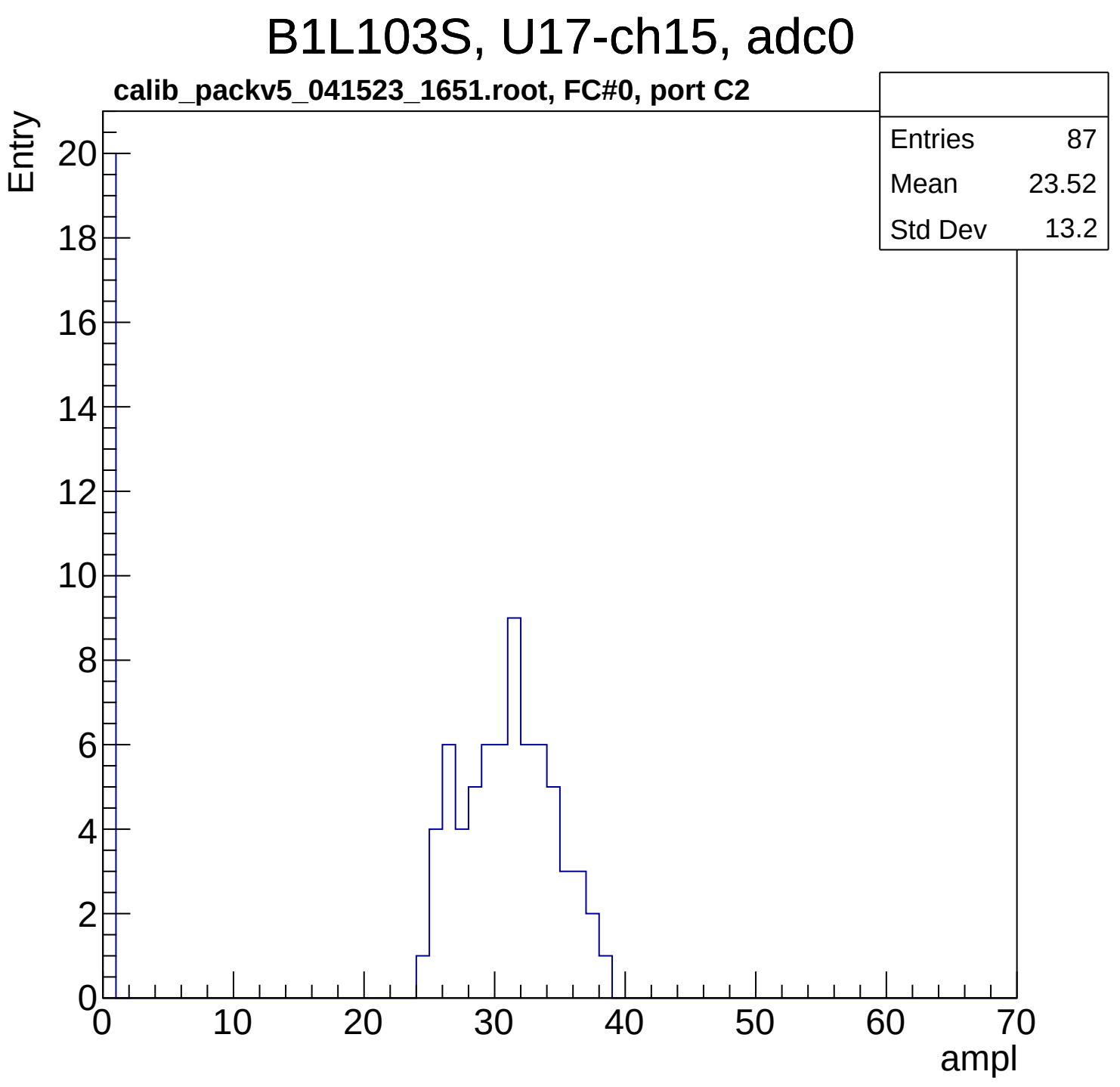
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch15, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 87
Mean 23.52
Std Dev 13.2
Entry
ampl
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6
8
10
12
14
16
18
20
0
10
20
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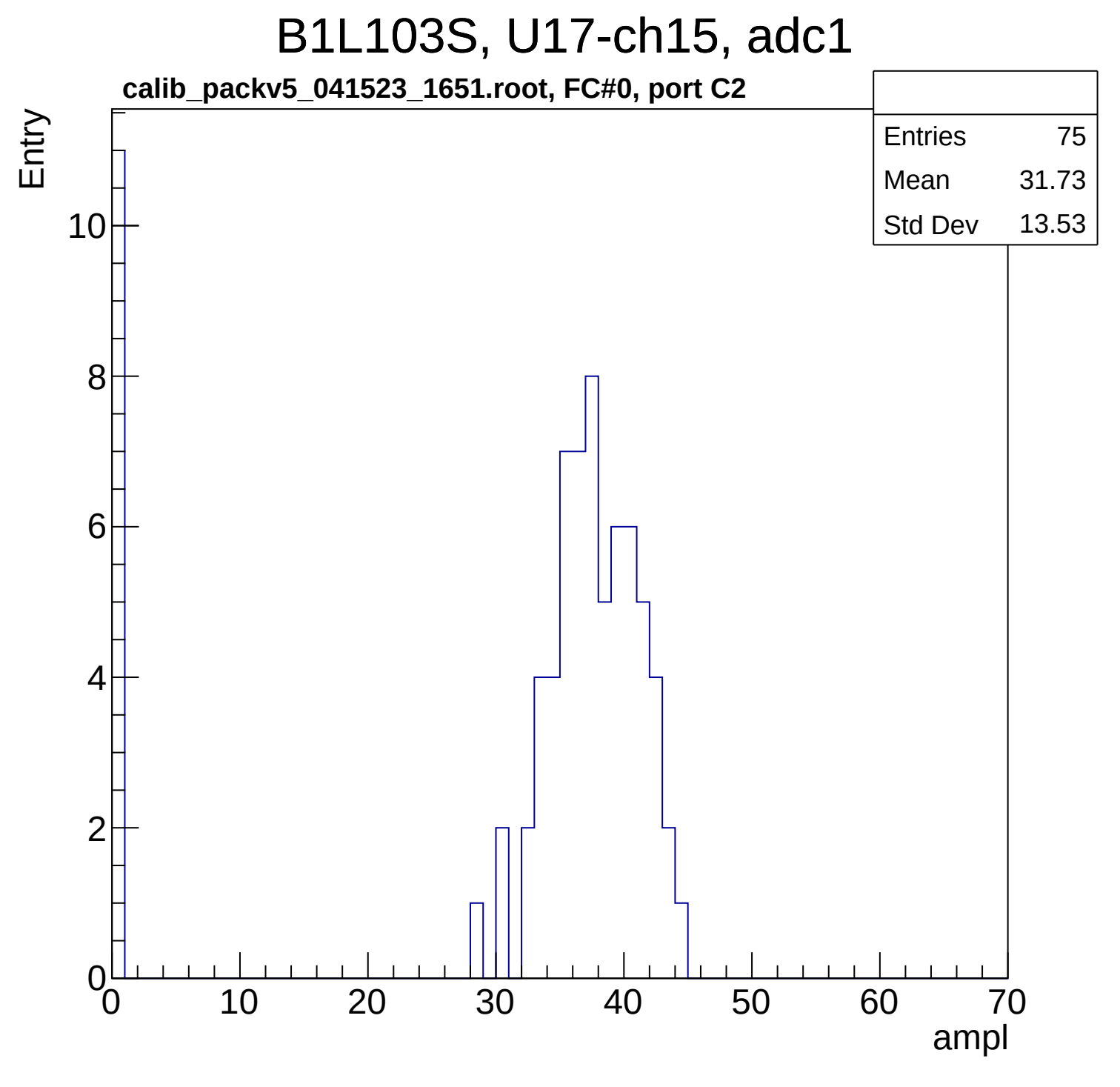
40
50
60
70


B1L103S, U17-ch15, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 31.73
Std Dev 13.53
Entry
0
2
4
6
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10
0
10
20
30
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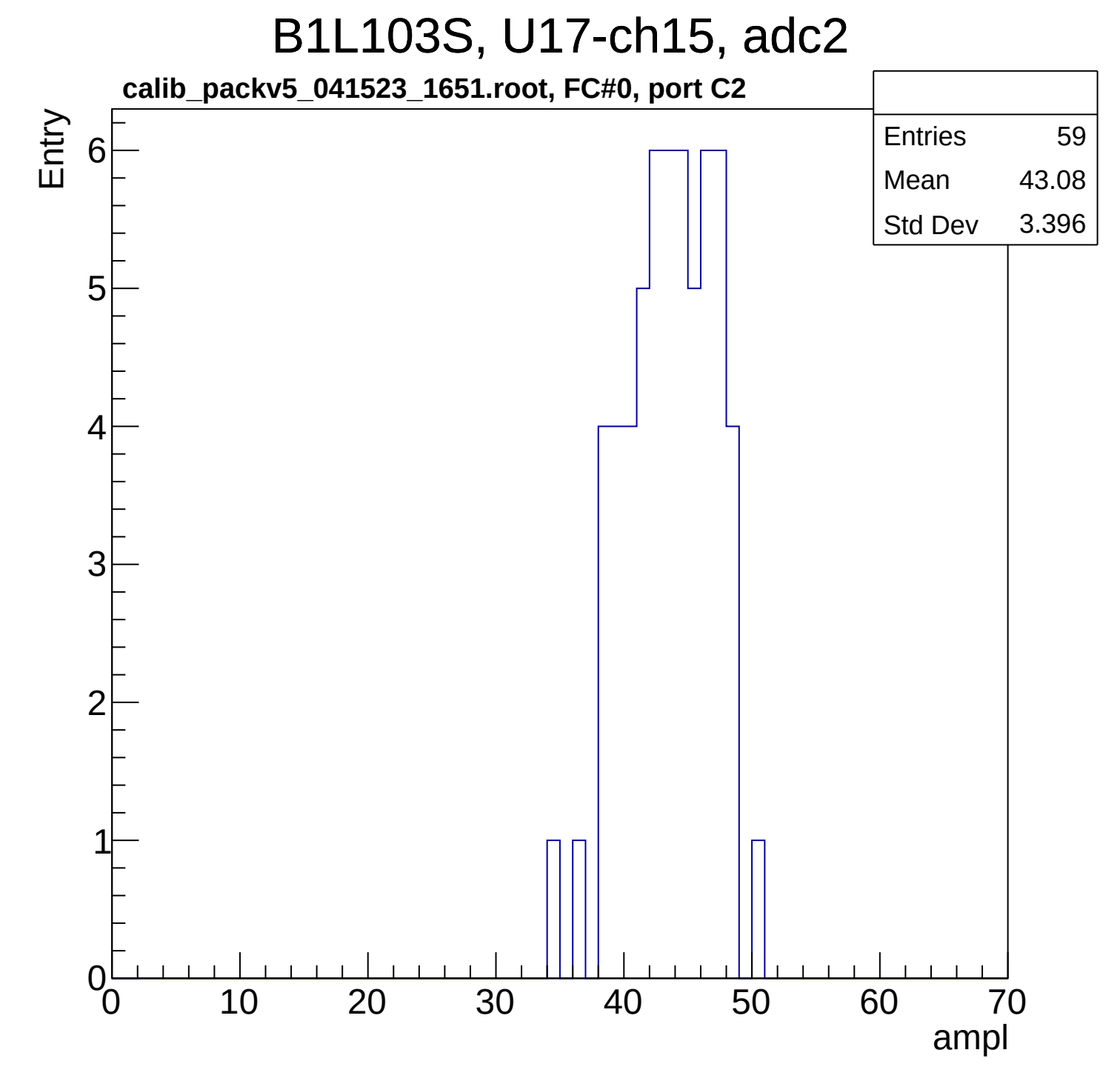
50
60
70
ampl


B1L103S, U17-ch15, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 43.08
Std Dev 3.396
Entry
ampl
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3
4
5
6
0
10
20
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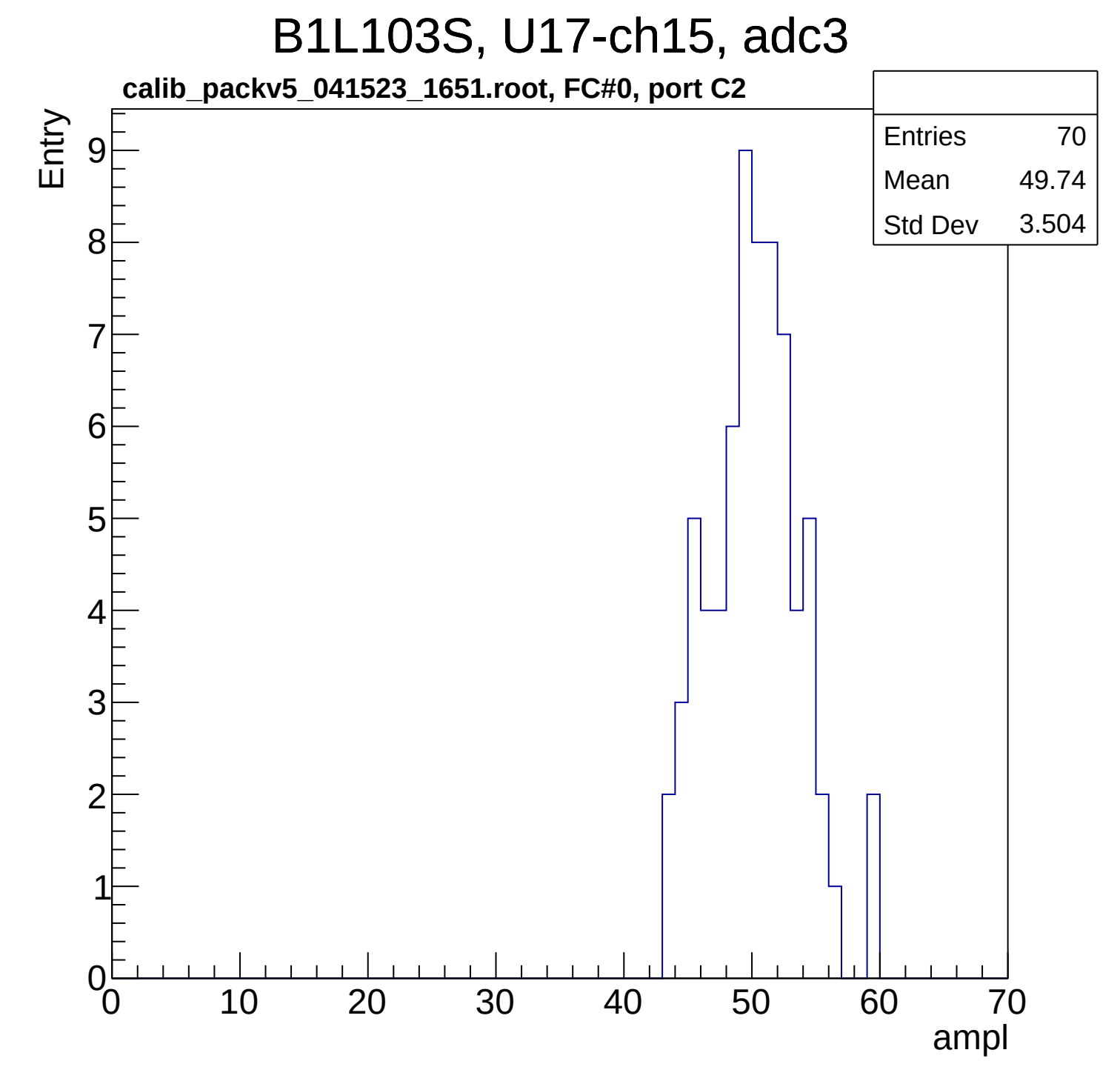
40
50
60
70


B1L103S, U17-ch15, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 49.74
Std Dev 3.504
Entry
ampl
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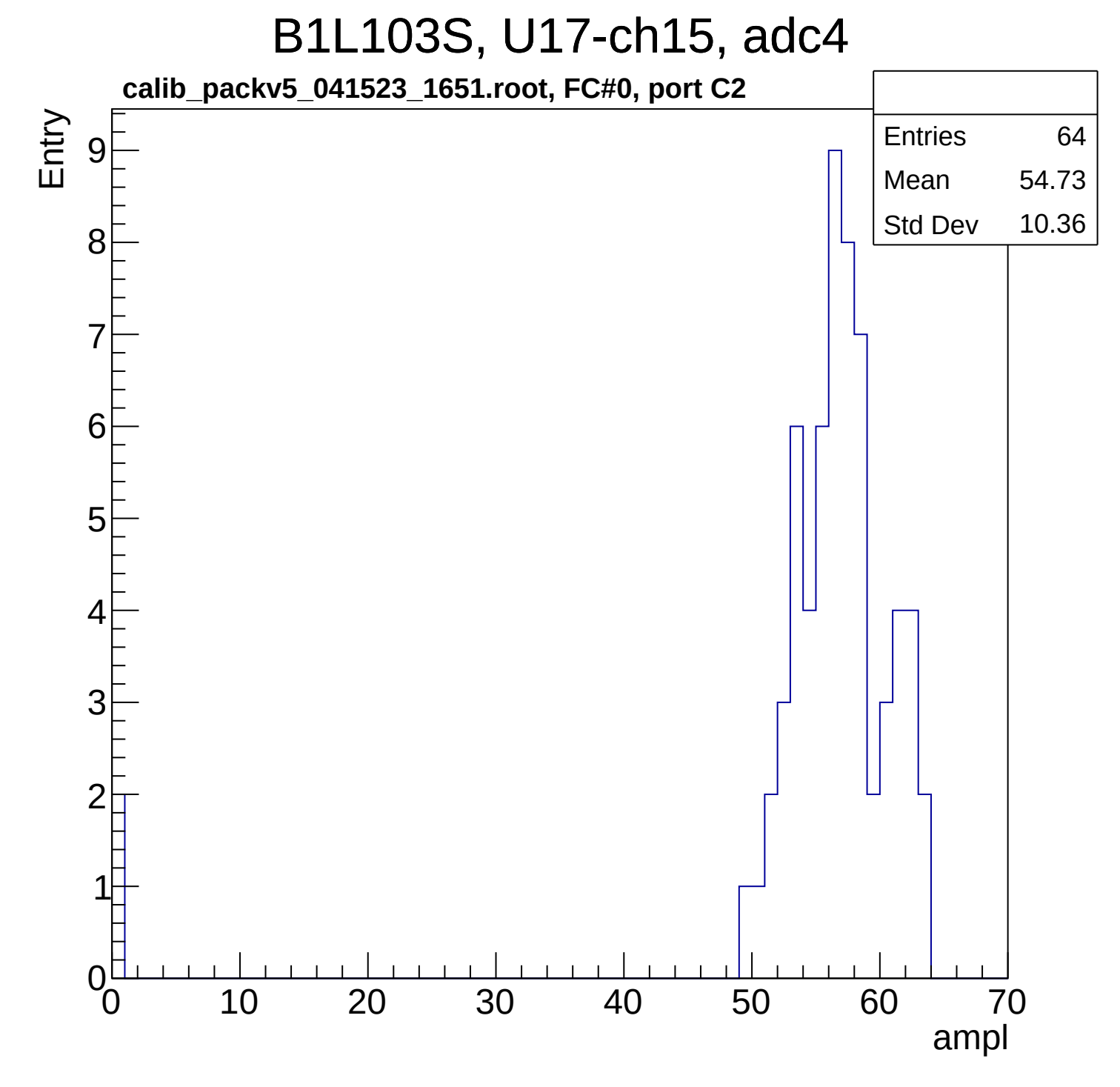
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U17-ch15, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 54.73
Std Dev 10.36
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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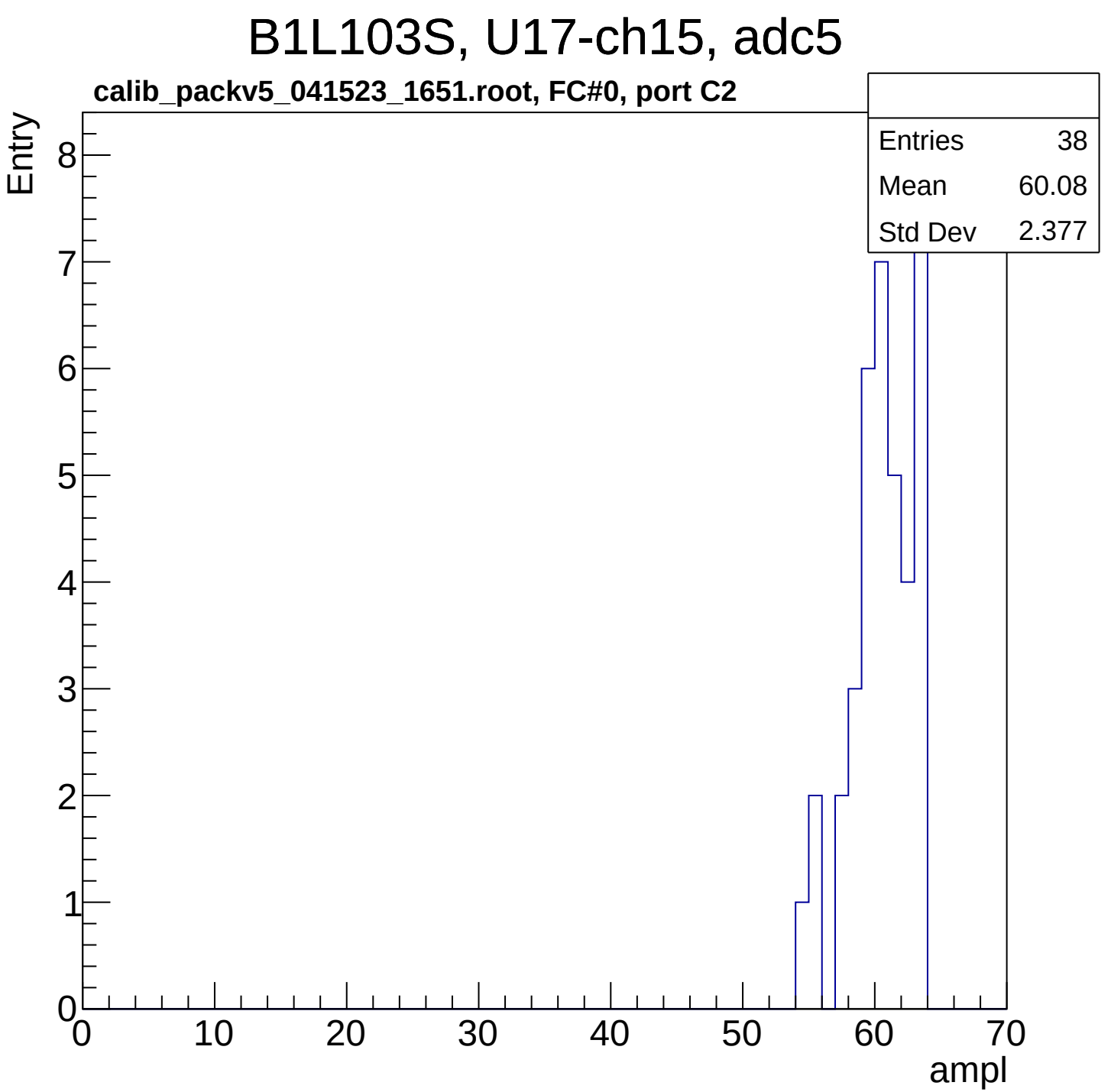
B1L103S, U17-ch15, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 38
Mean 60.08
Std Dev 2.377
Entry
ampl
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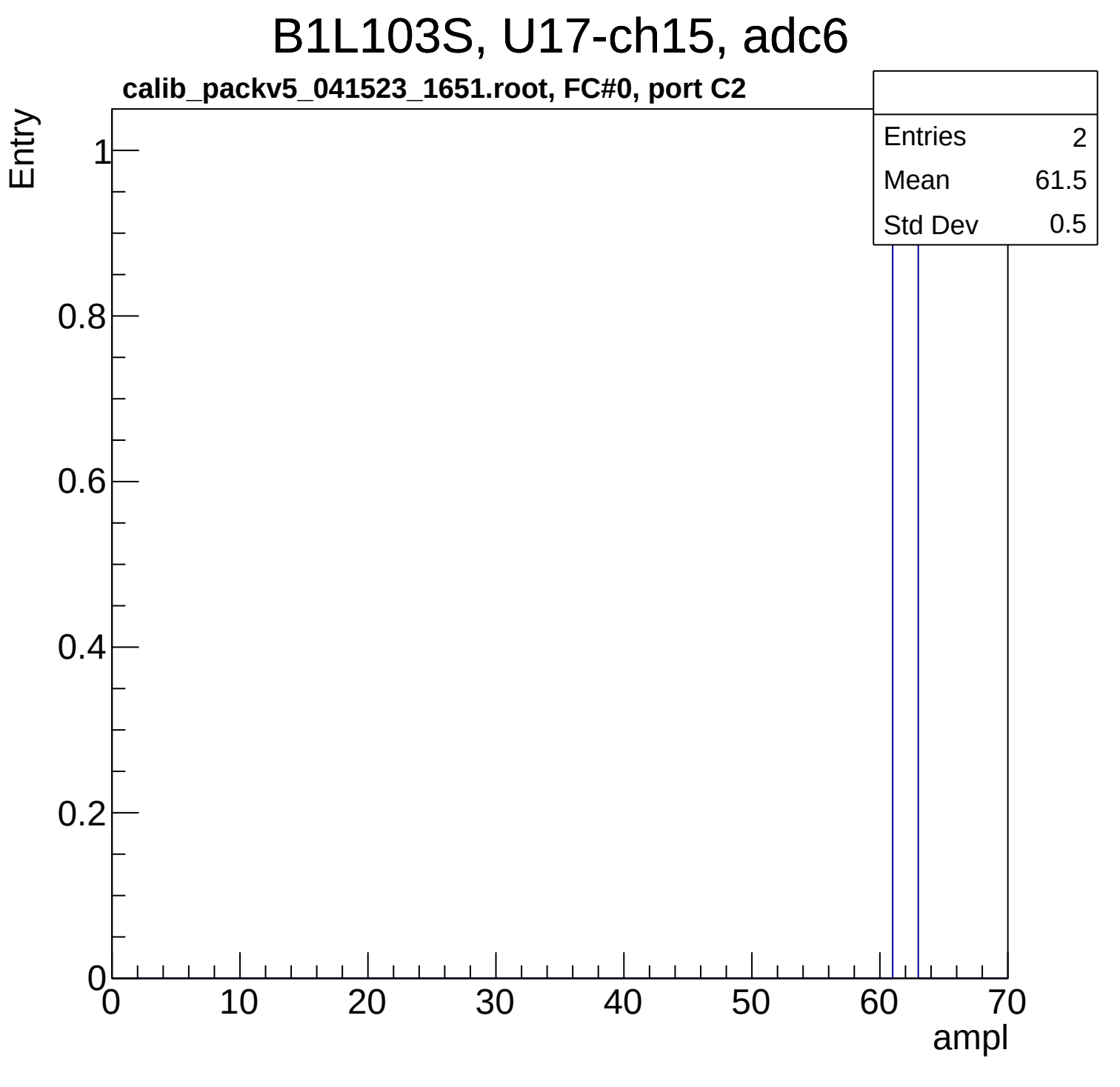
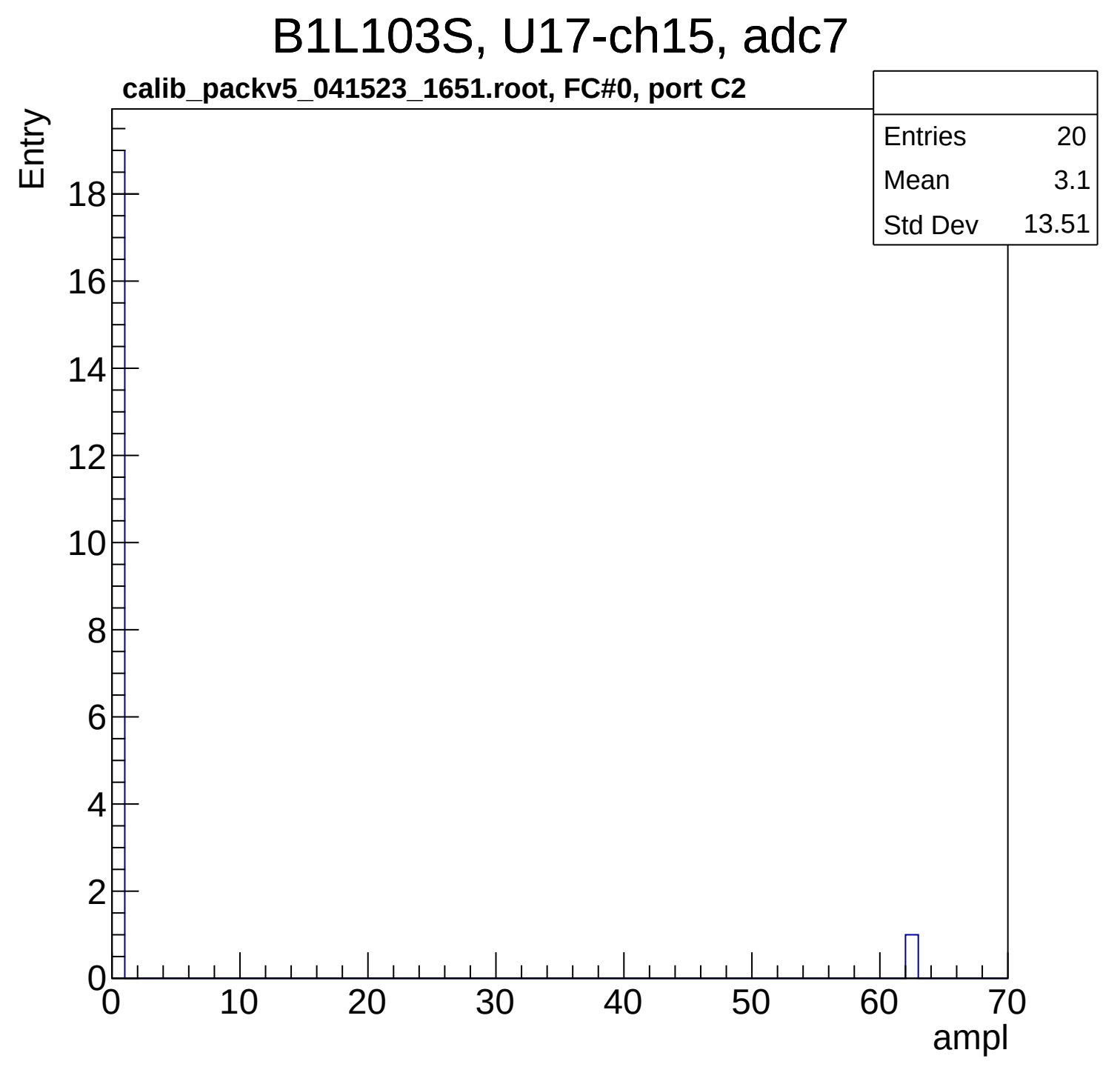
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U17-ch15, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 2
Mean 61.5
Std Dev 0.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch15, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.1
Std Dev 13.51
Entry
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2
4
6
8
10
12
14
16
18
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10
20
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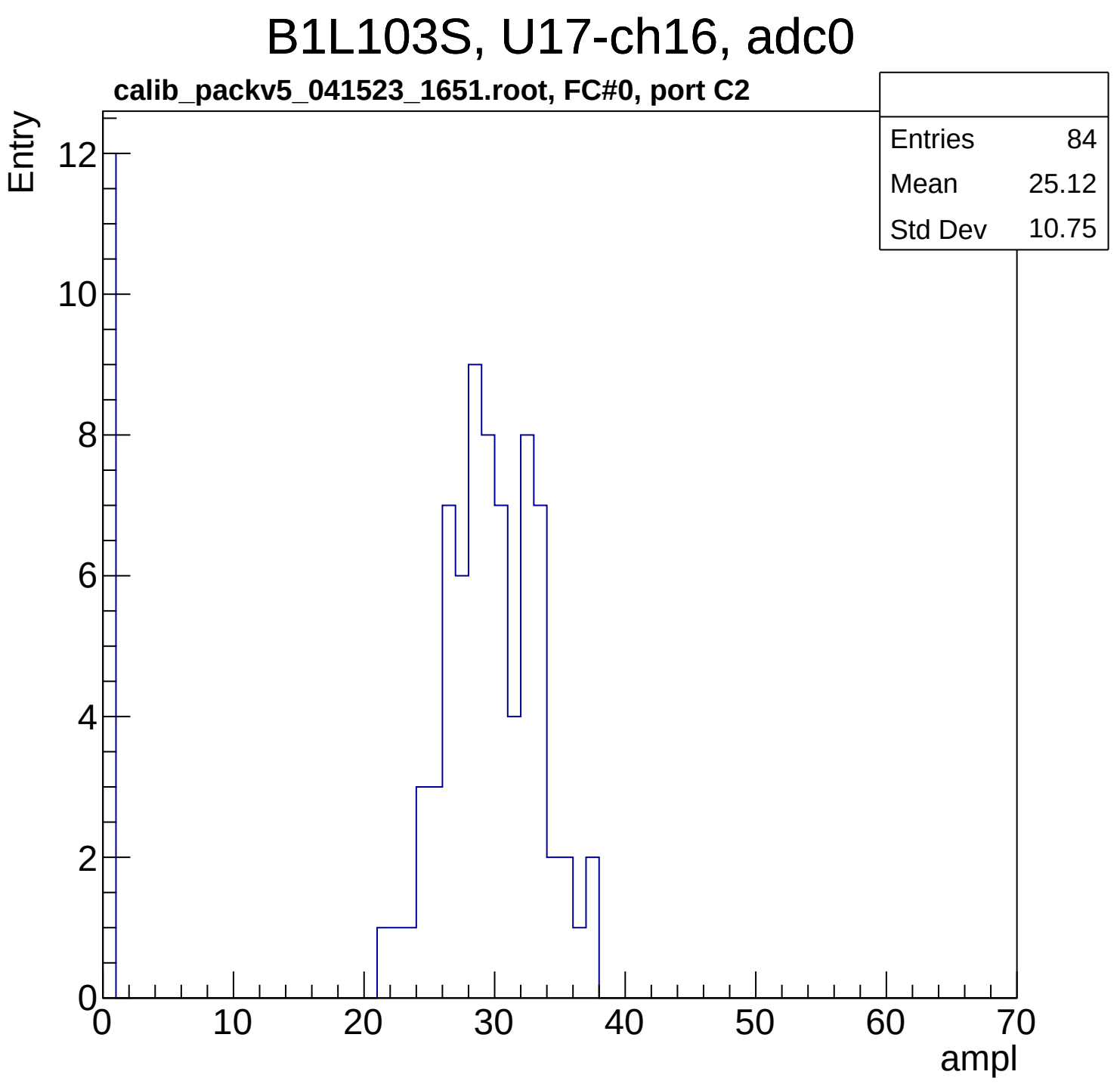
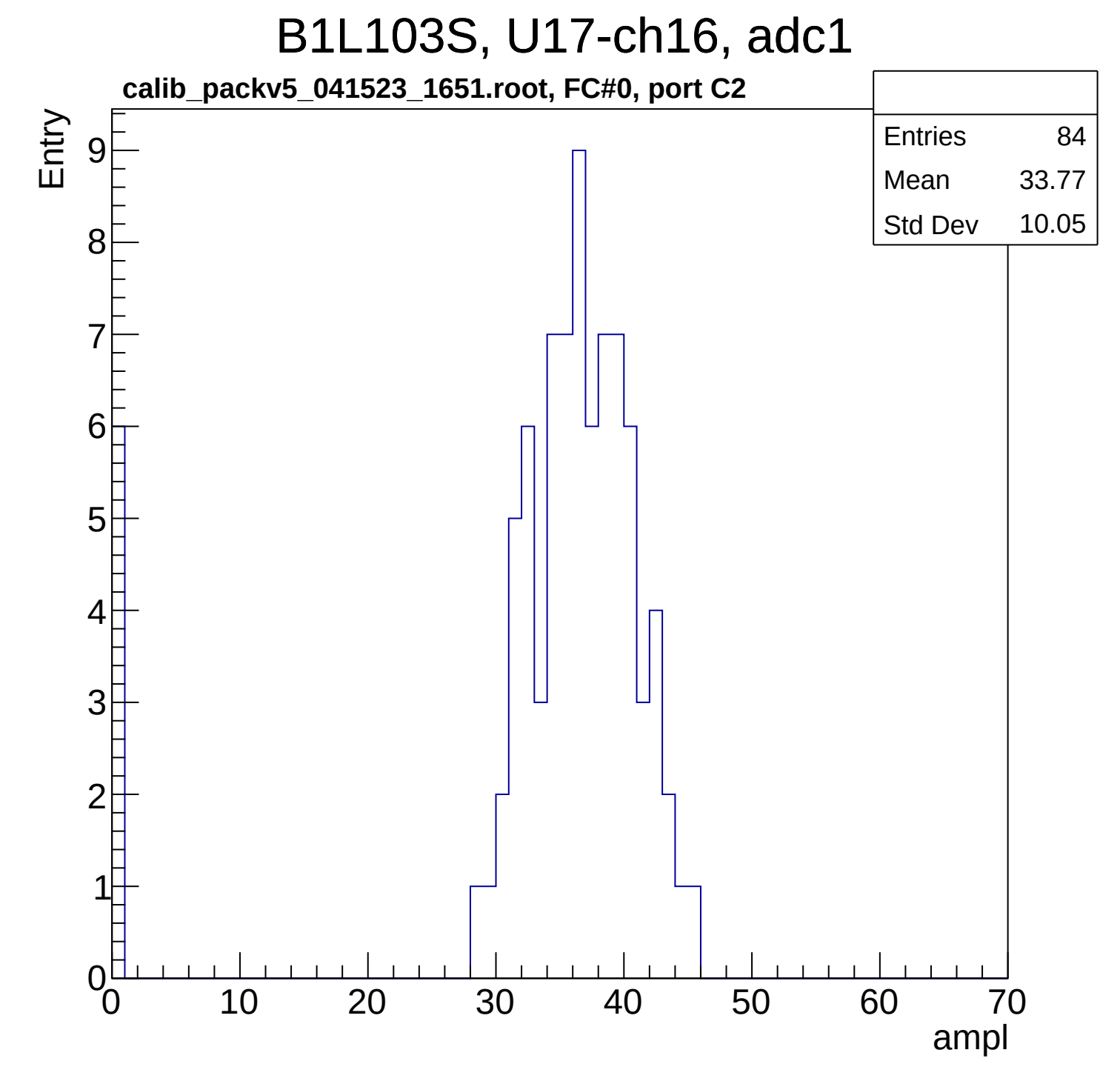
50
60
70
ampl


B1L103S, U17-ch16, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 25.12
Std Dev 10.75
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch16, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 33.77
Std Dev 10.05
Entry
ampl
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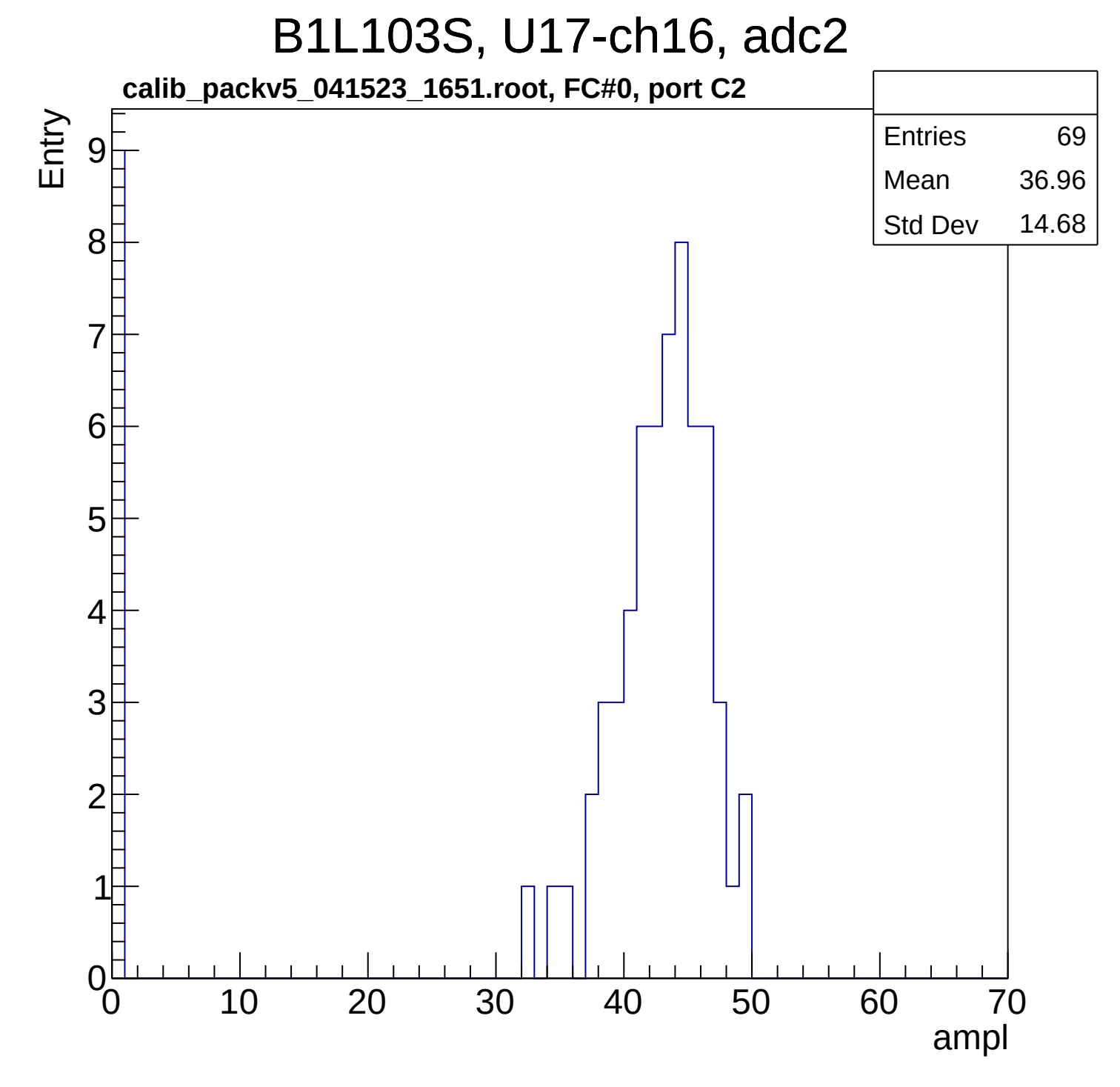
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U17-ch16, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 36.96
Std Dev 14.68
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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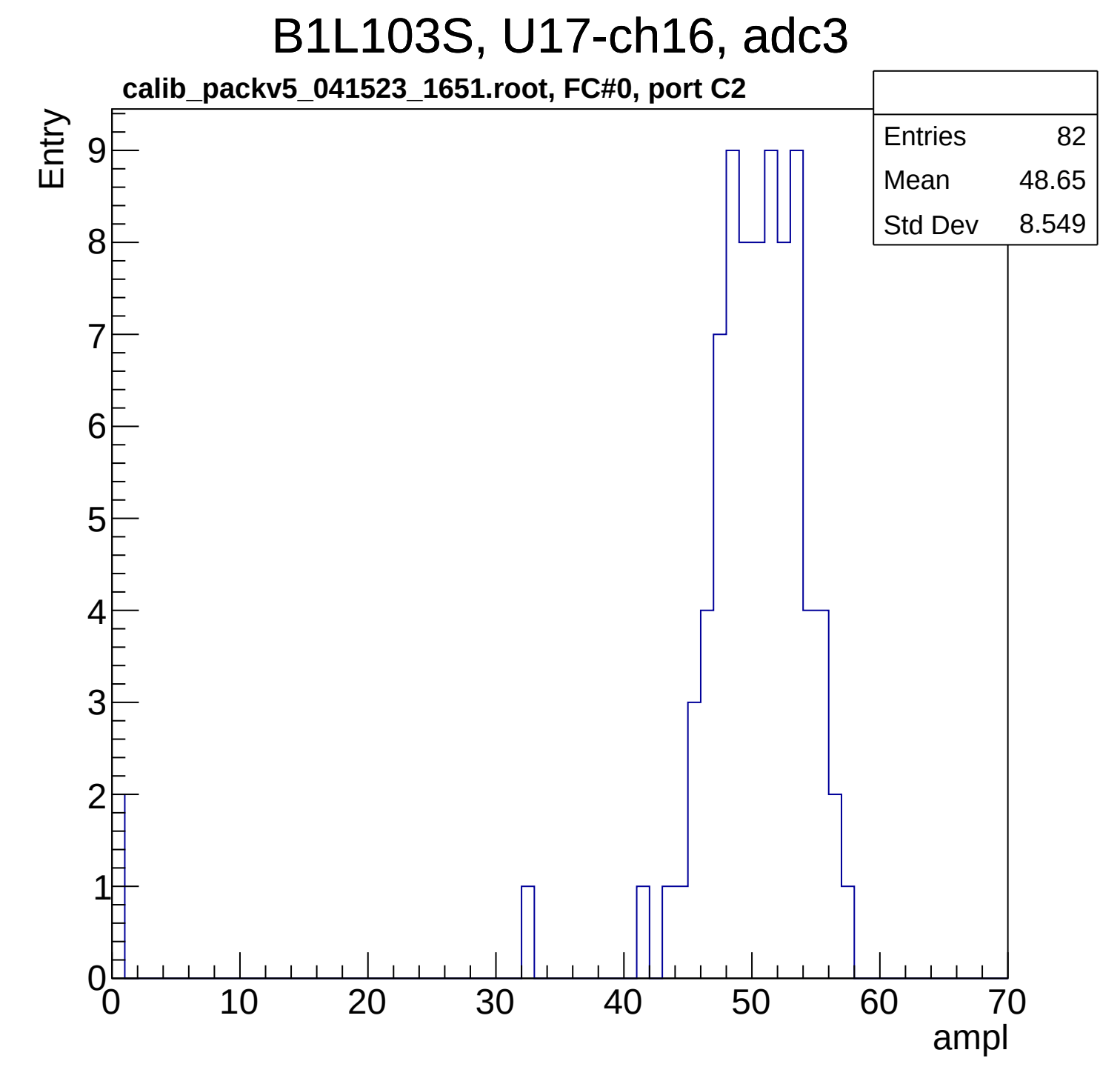
B1L103S, U17-ch16, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 48.65
Std Dev 8.549
Entry
ampl
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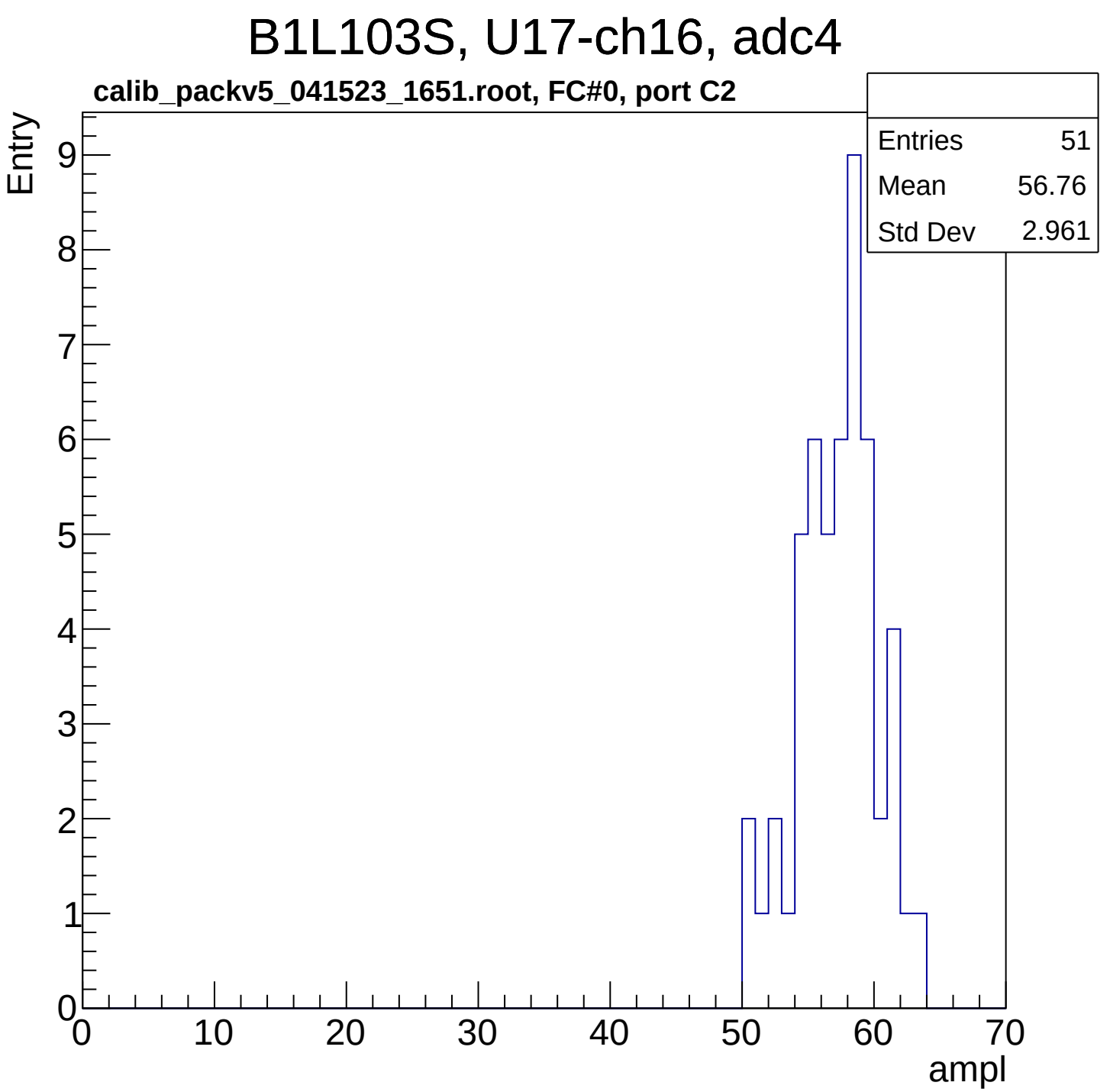
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U17-ch16, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 56.76
Std Dev 2.961
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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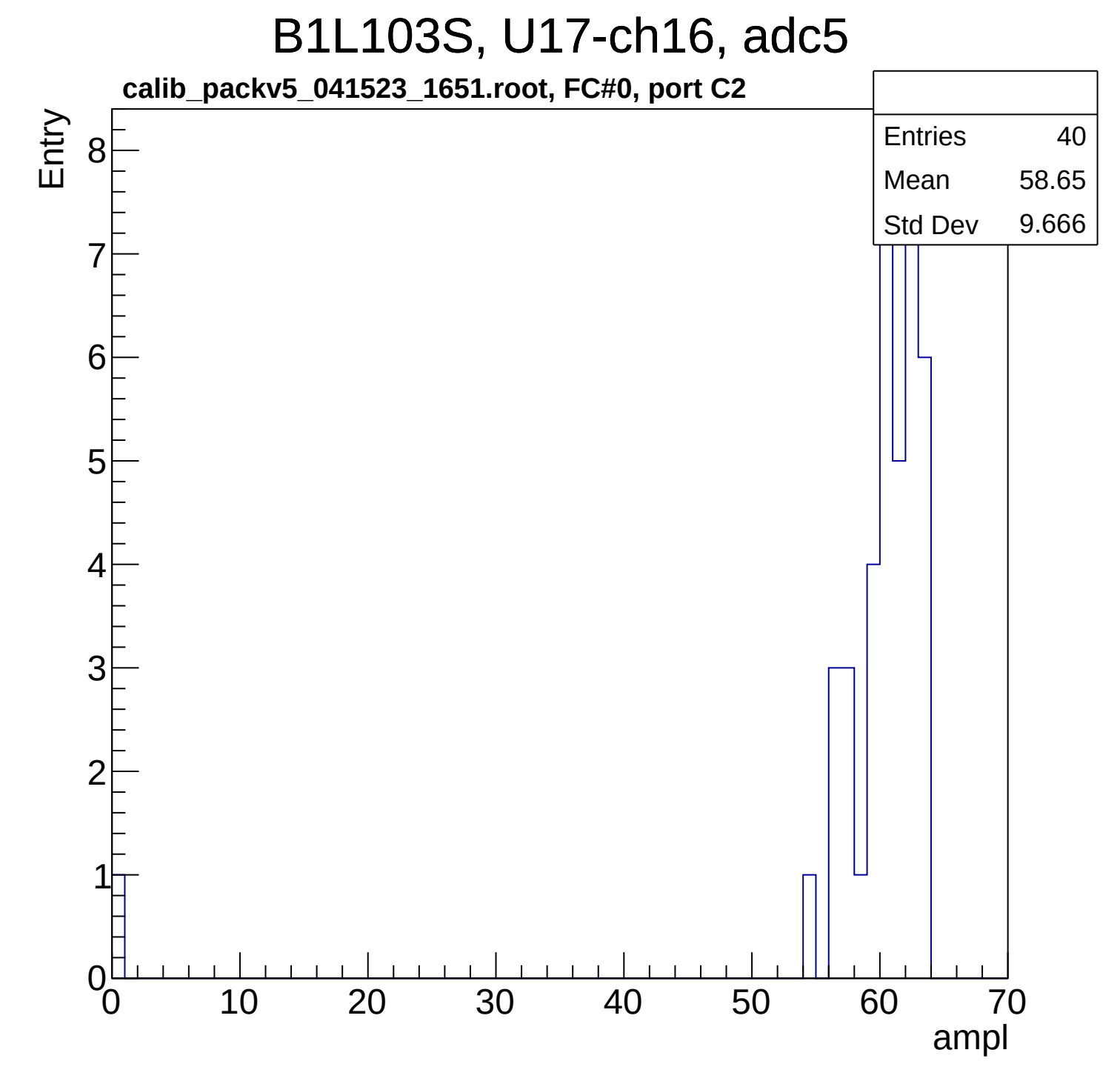
B1L103S, U17-ch16, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 40
Mean 58.65
Std Dev 9.666
Entry
ampl
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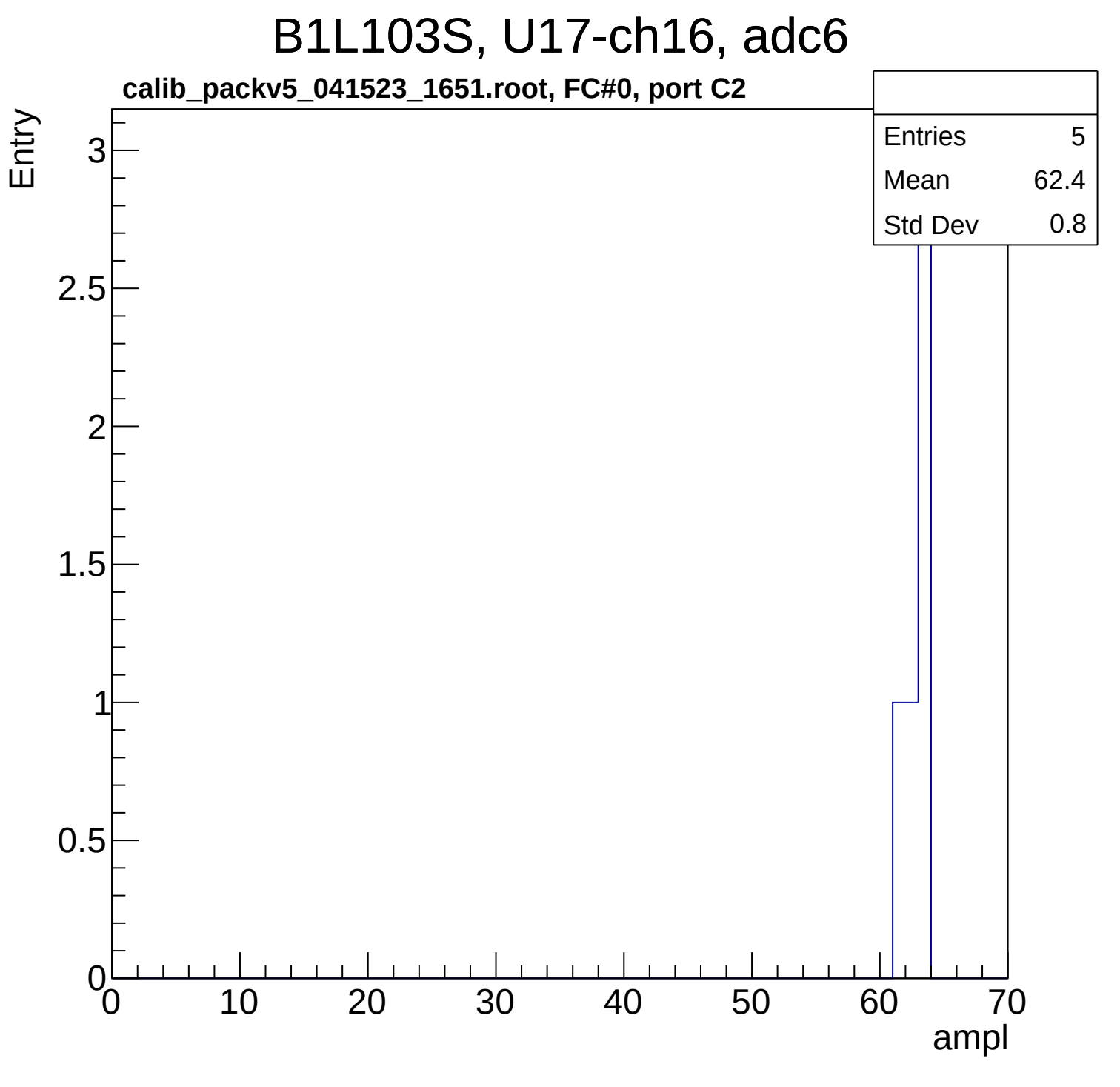
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U17-ch16, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 5
Mean 62.4
Std Dev 0.8
Entry
ampl
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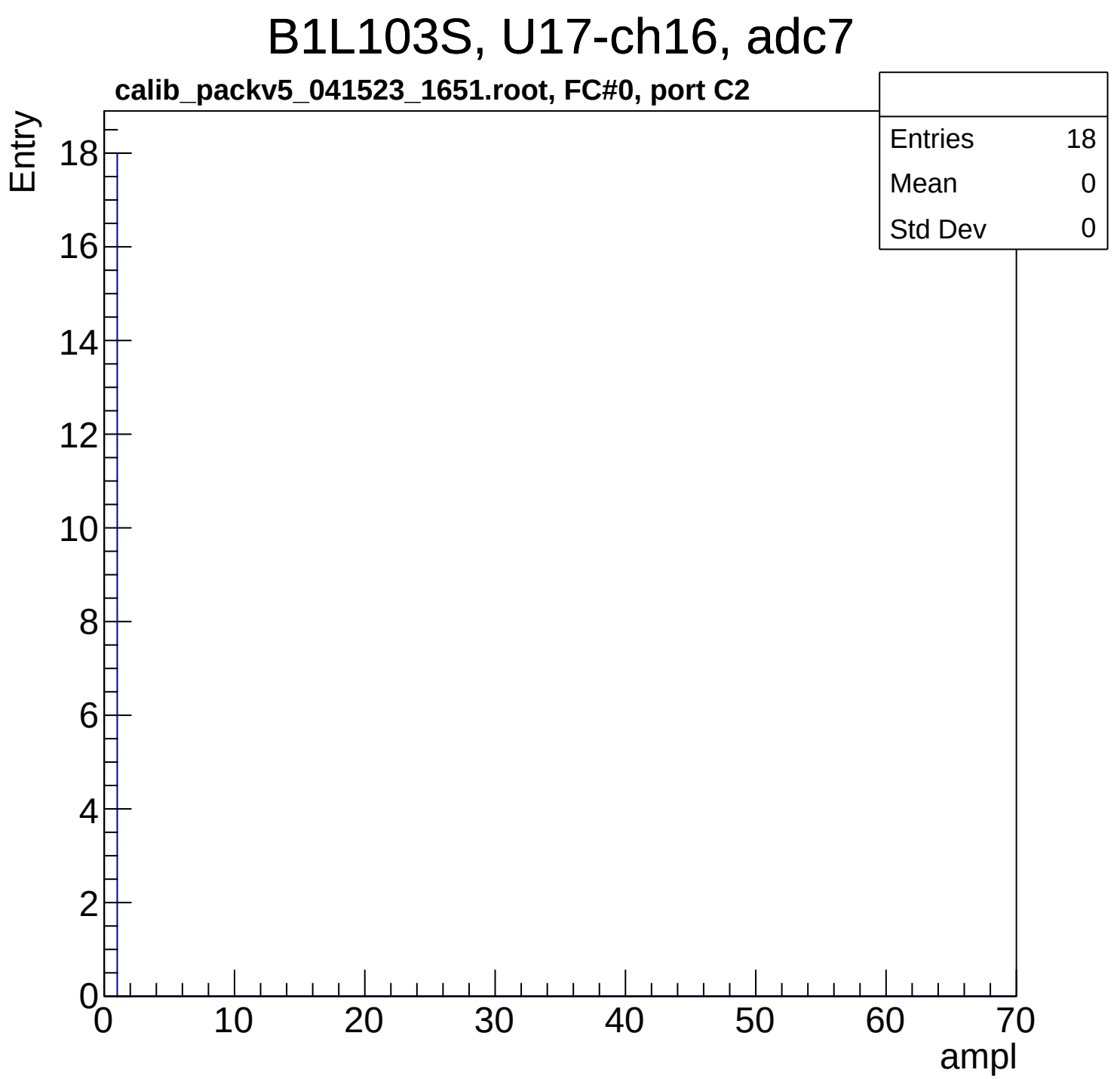
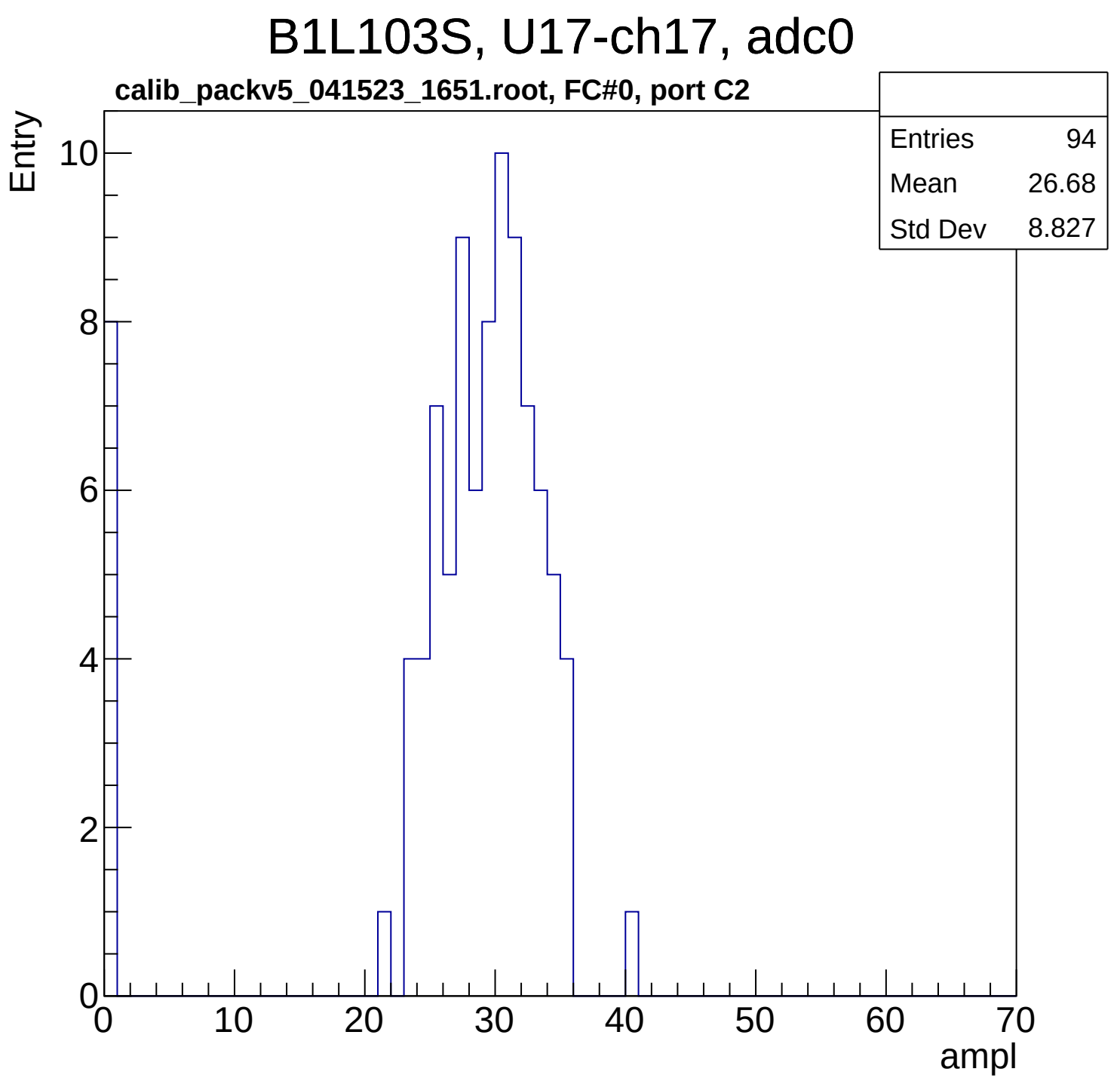
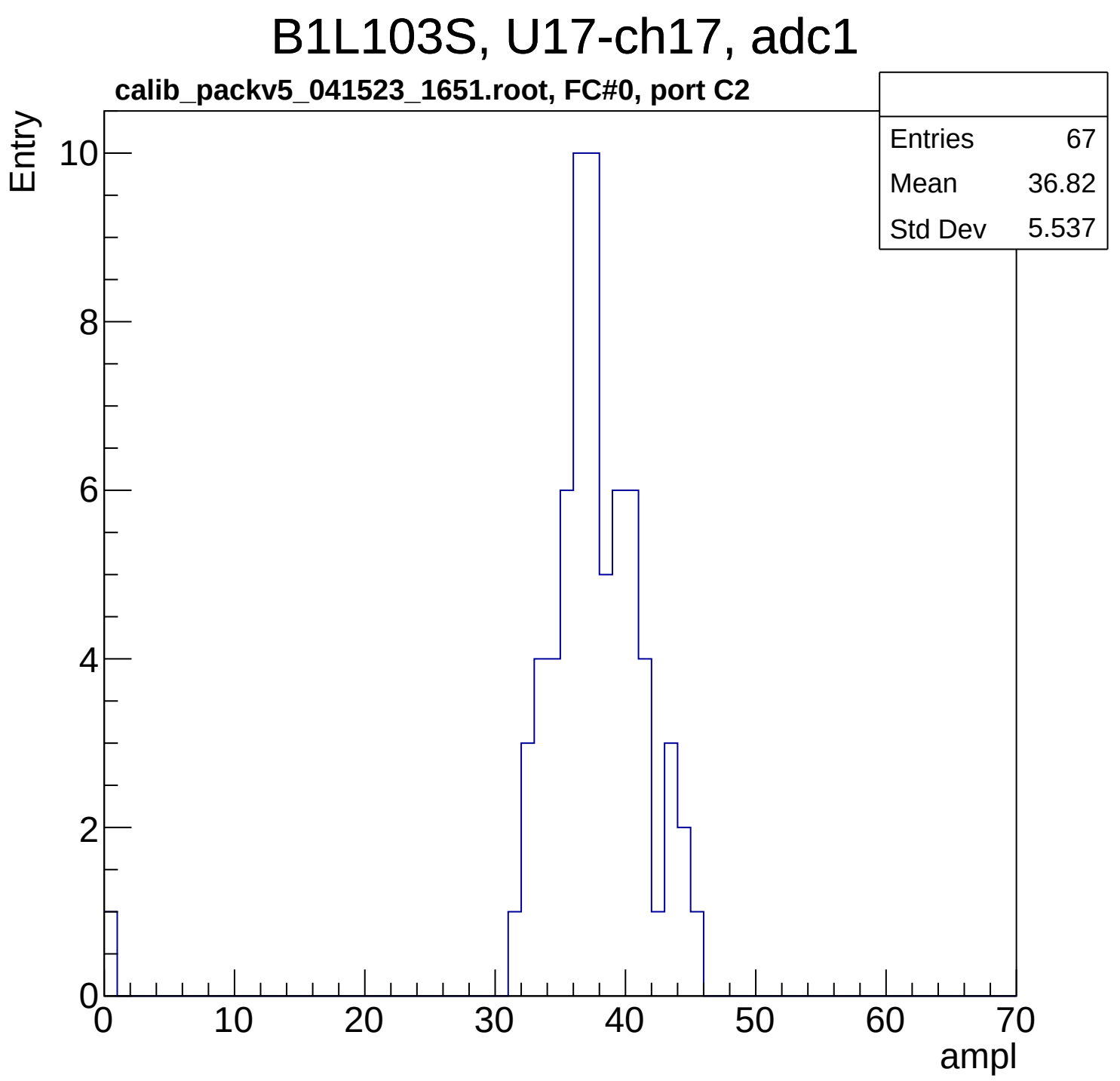
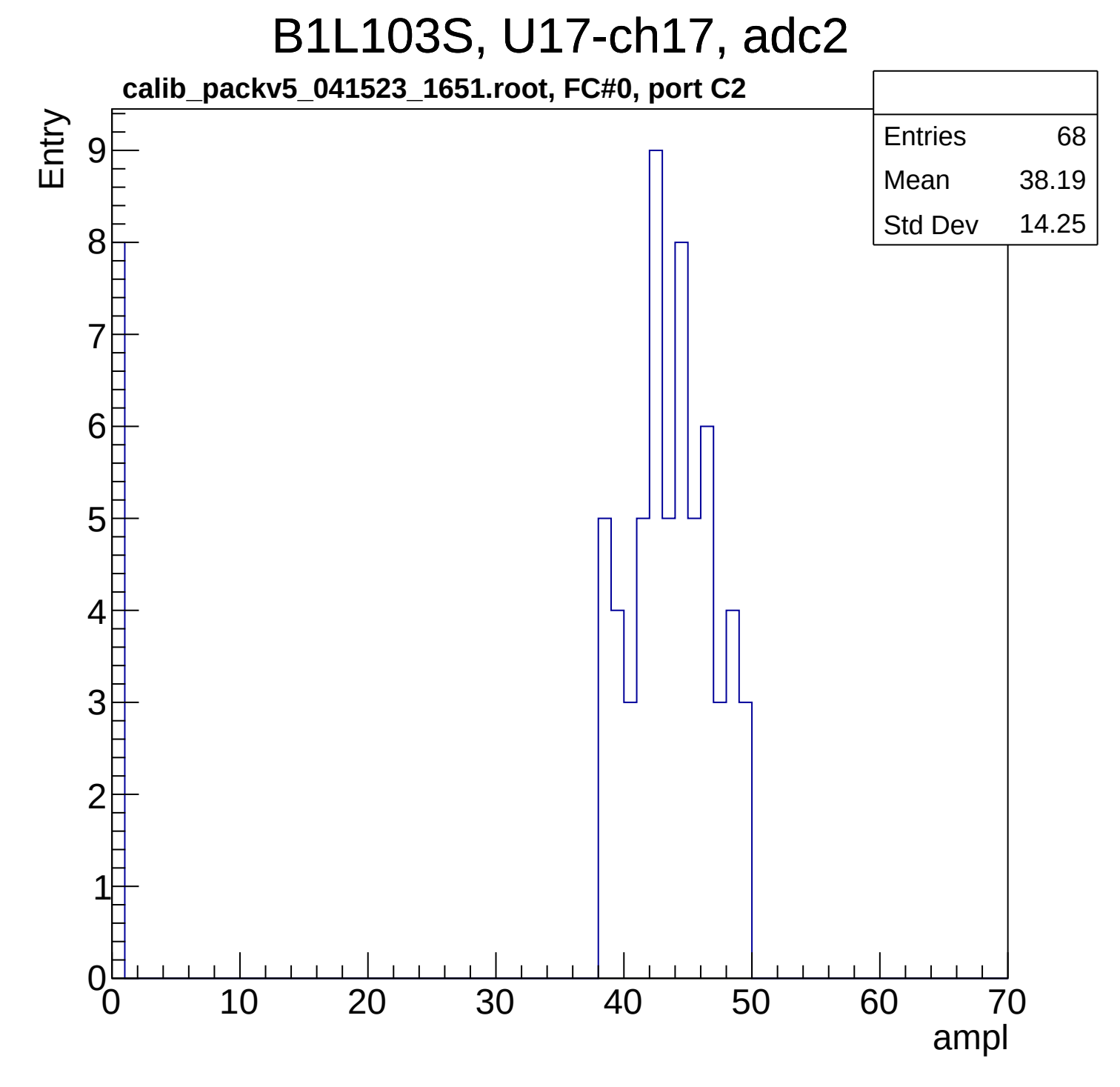
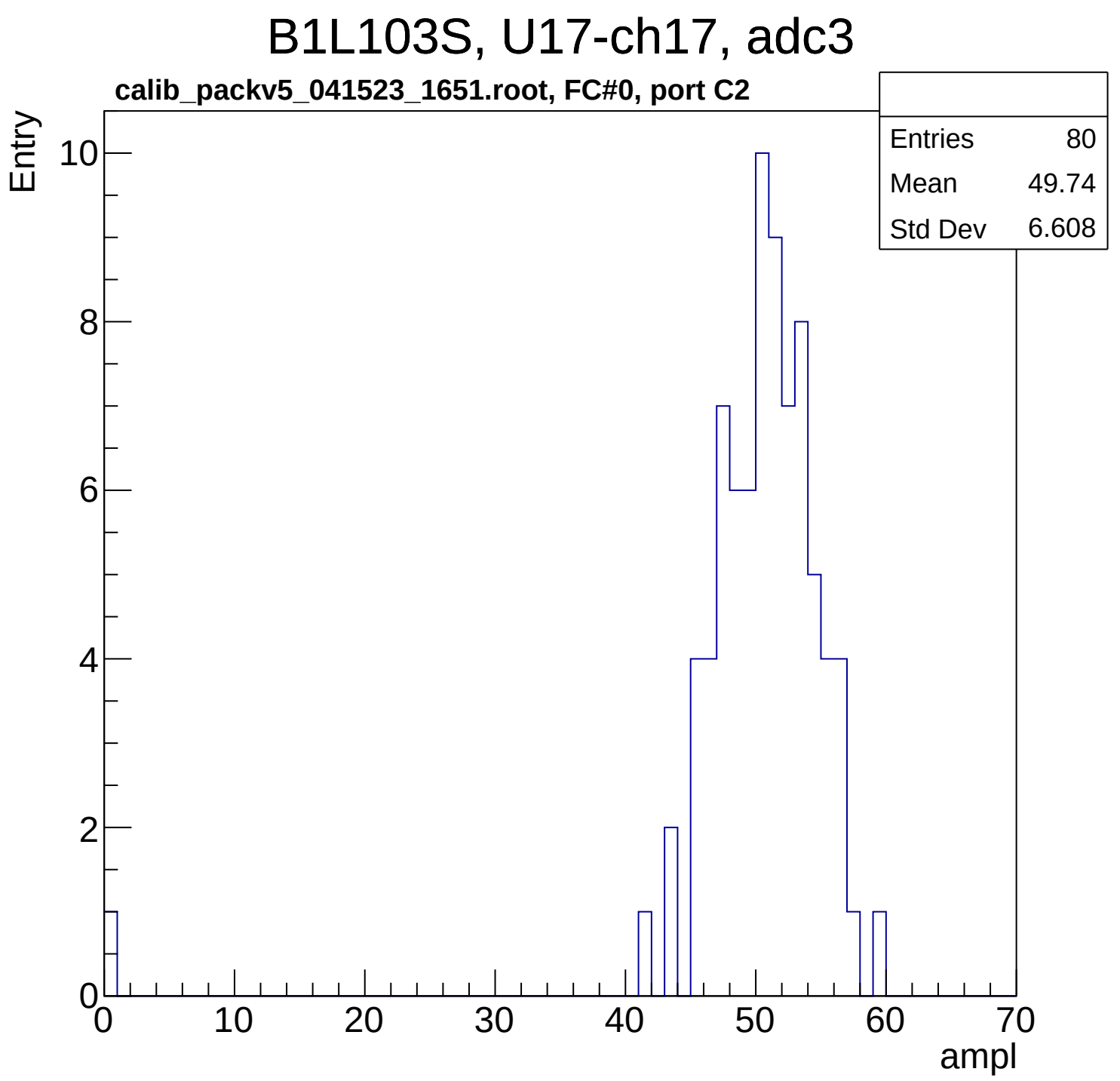
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

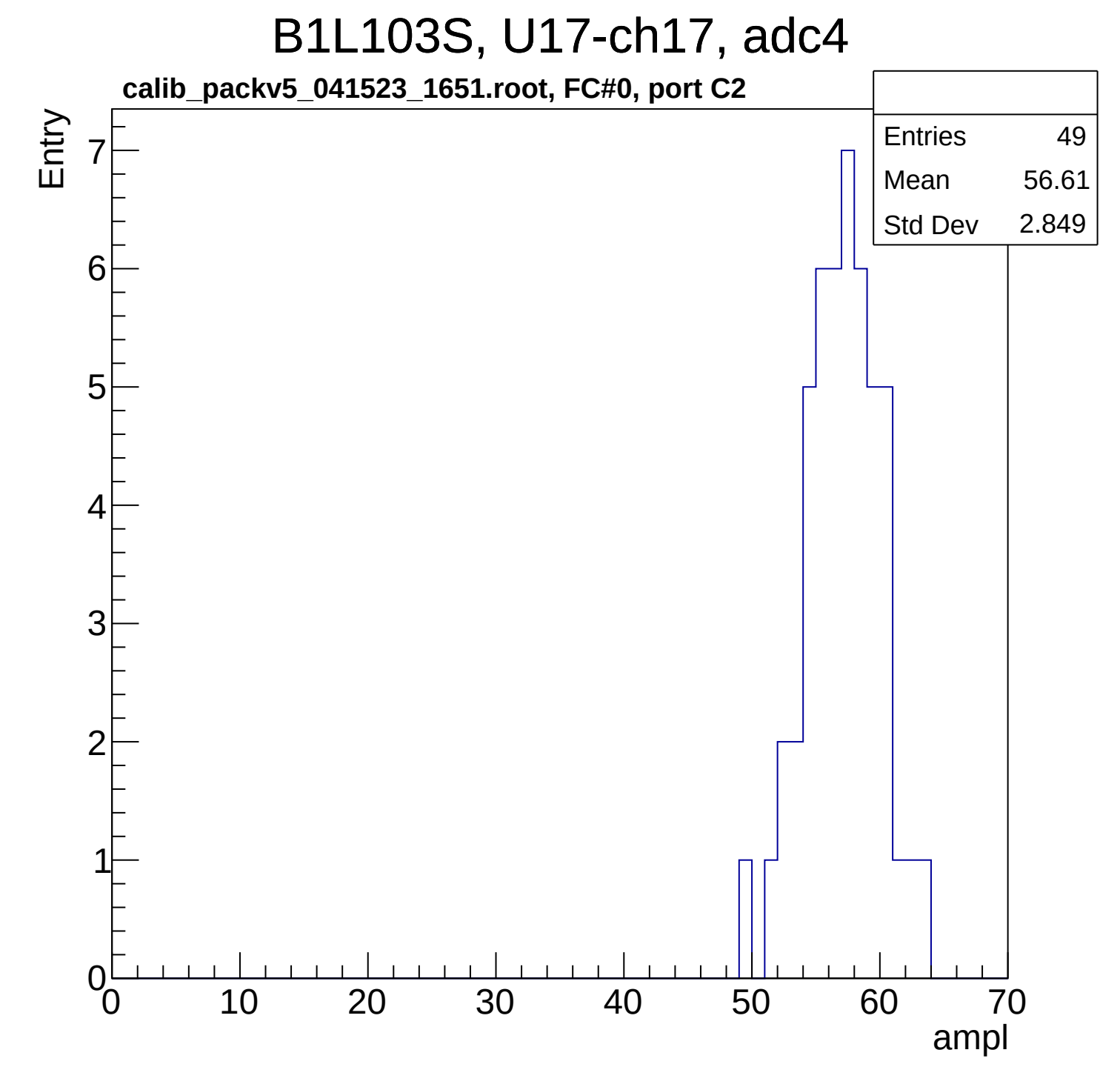

B1L103S, U17-ch16, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

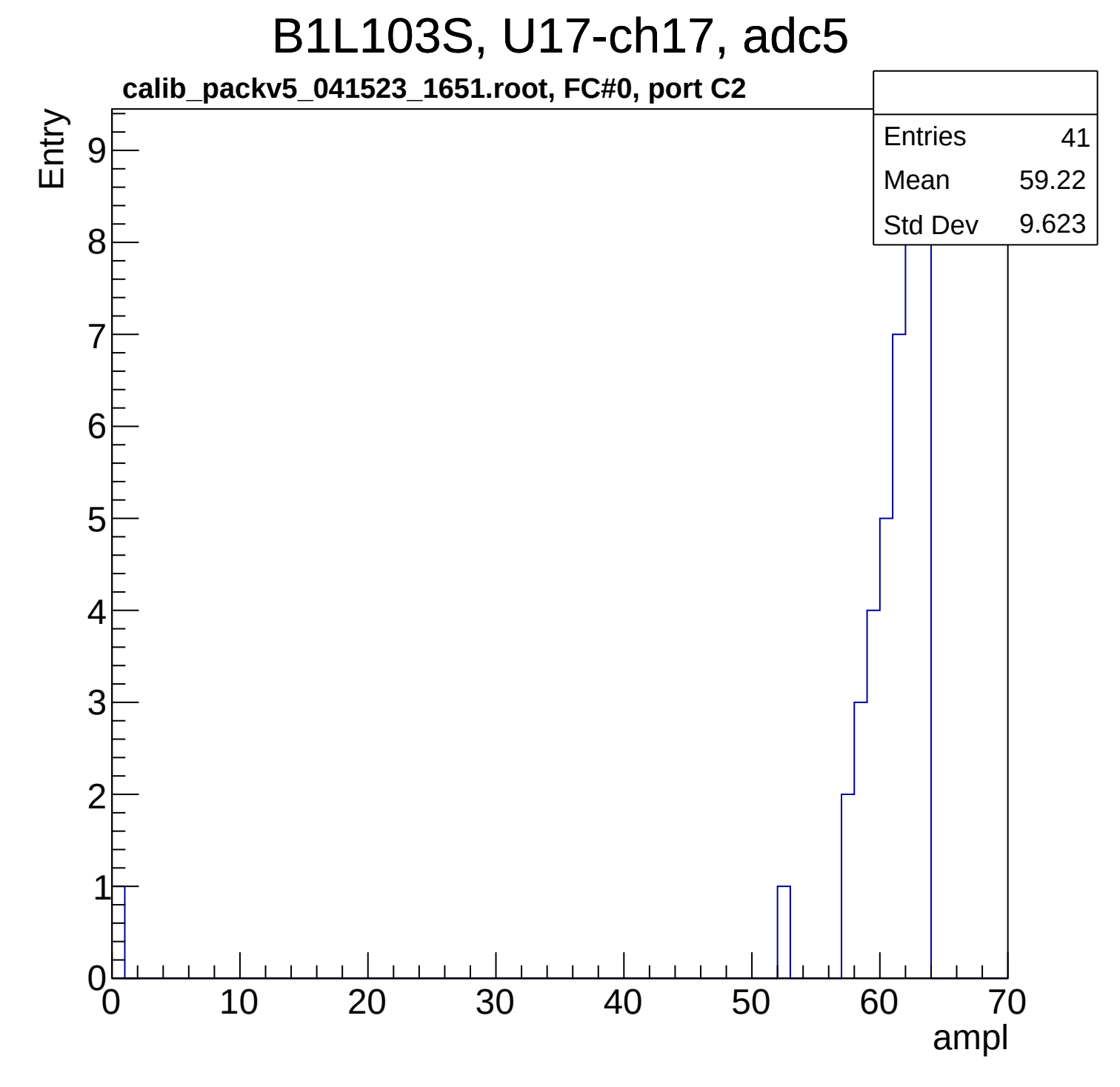

B1L103S, U17-ch17, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 94
Mean 26.68
Std Dev 8.827
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

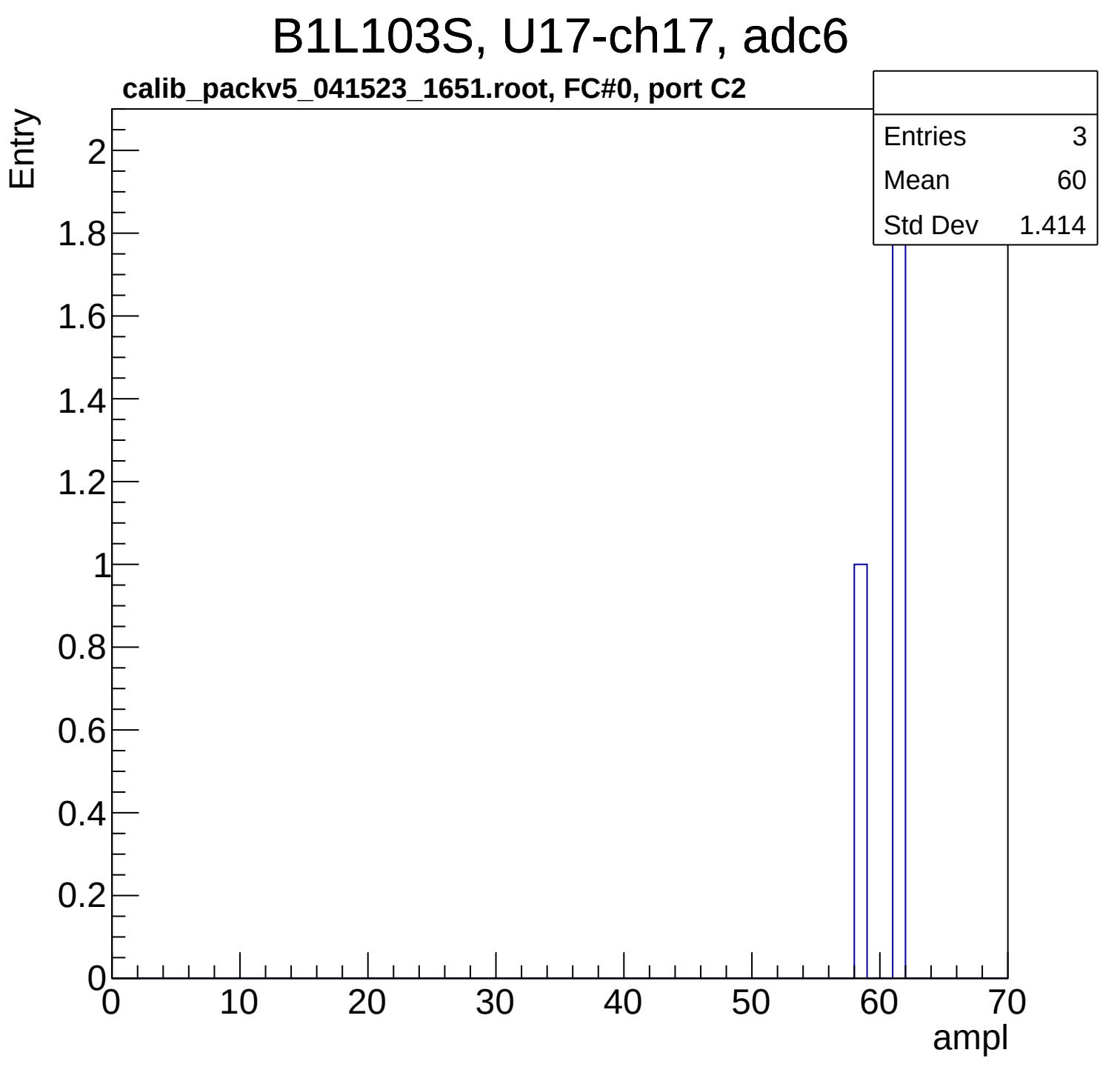

B1L103S, U17-ch17, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 36.82
Std Dev 5.537
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

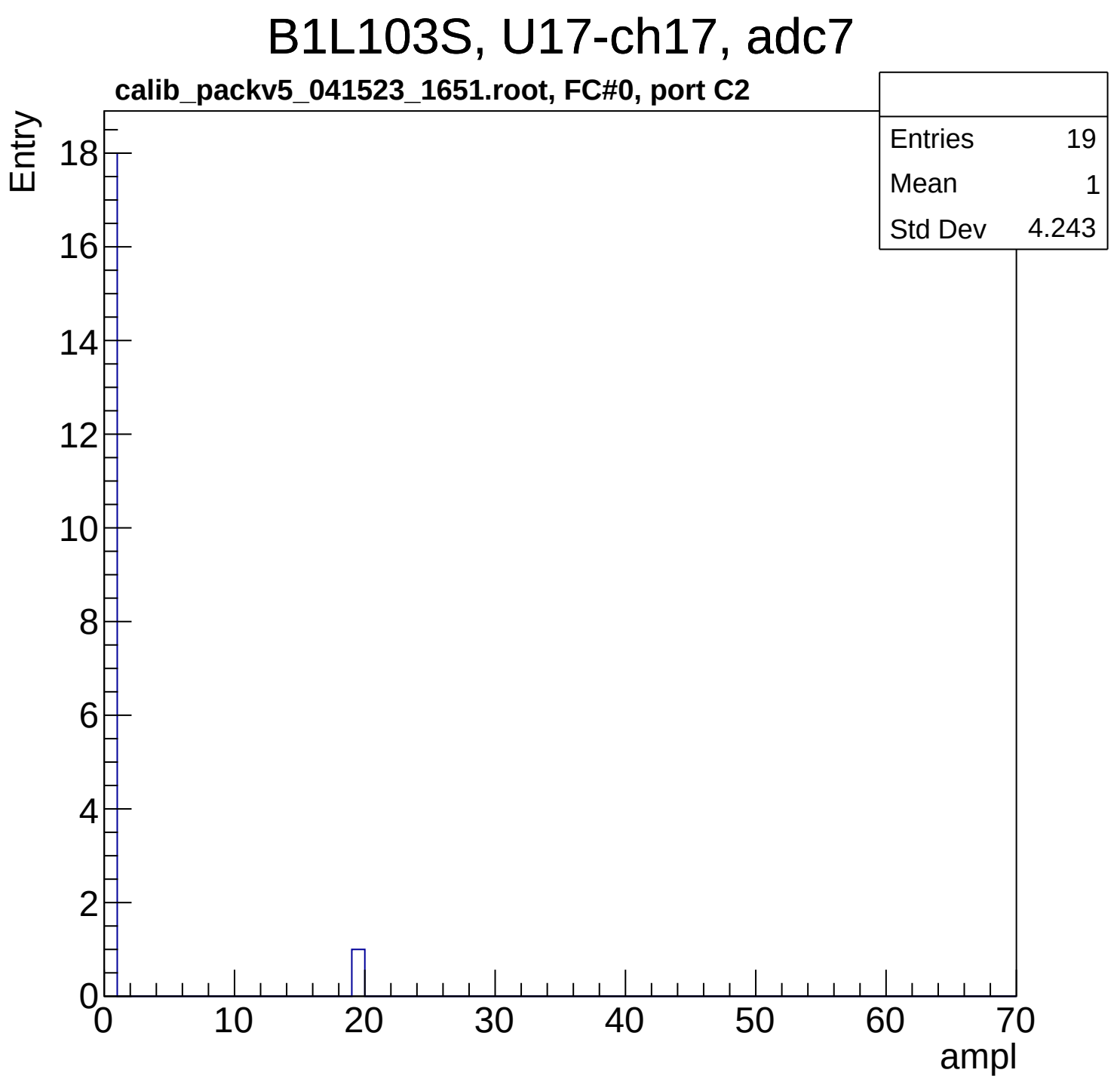

B1L103S, U17-ch17, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 38.19
Std Dev 14.25
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

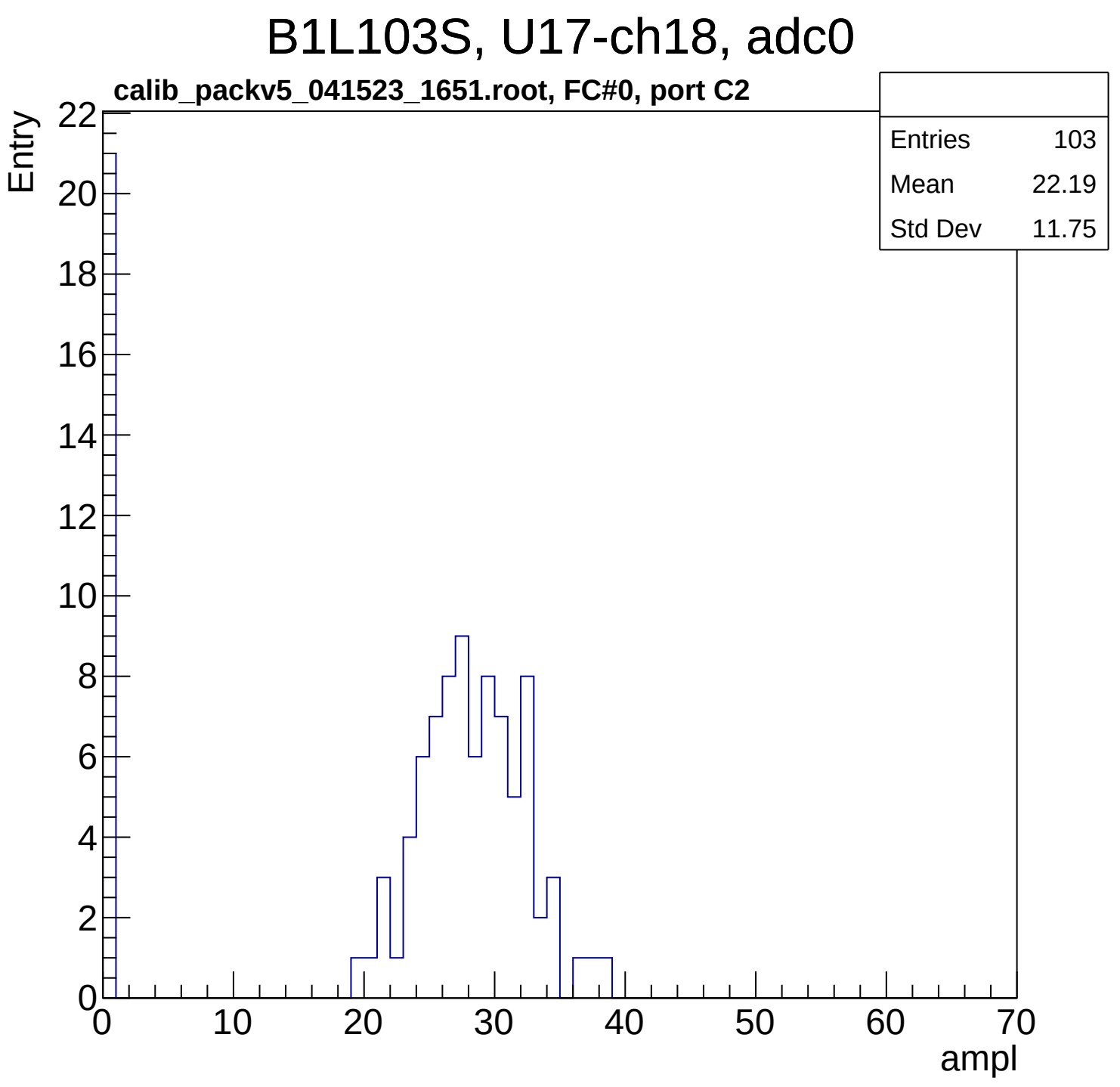

B1L103S, U17-ch17, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 49.74
Std Dev 6.608
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

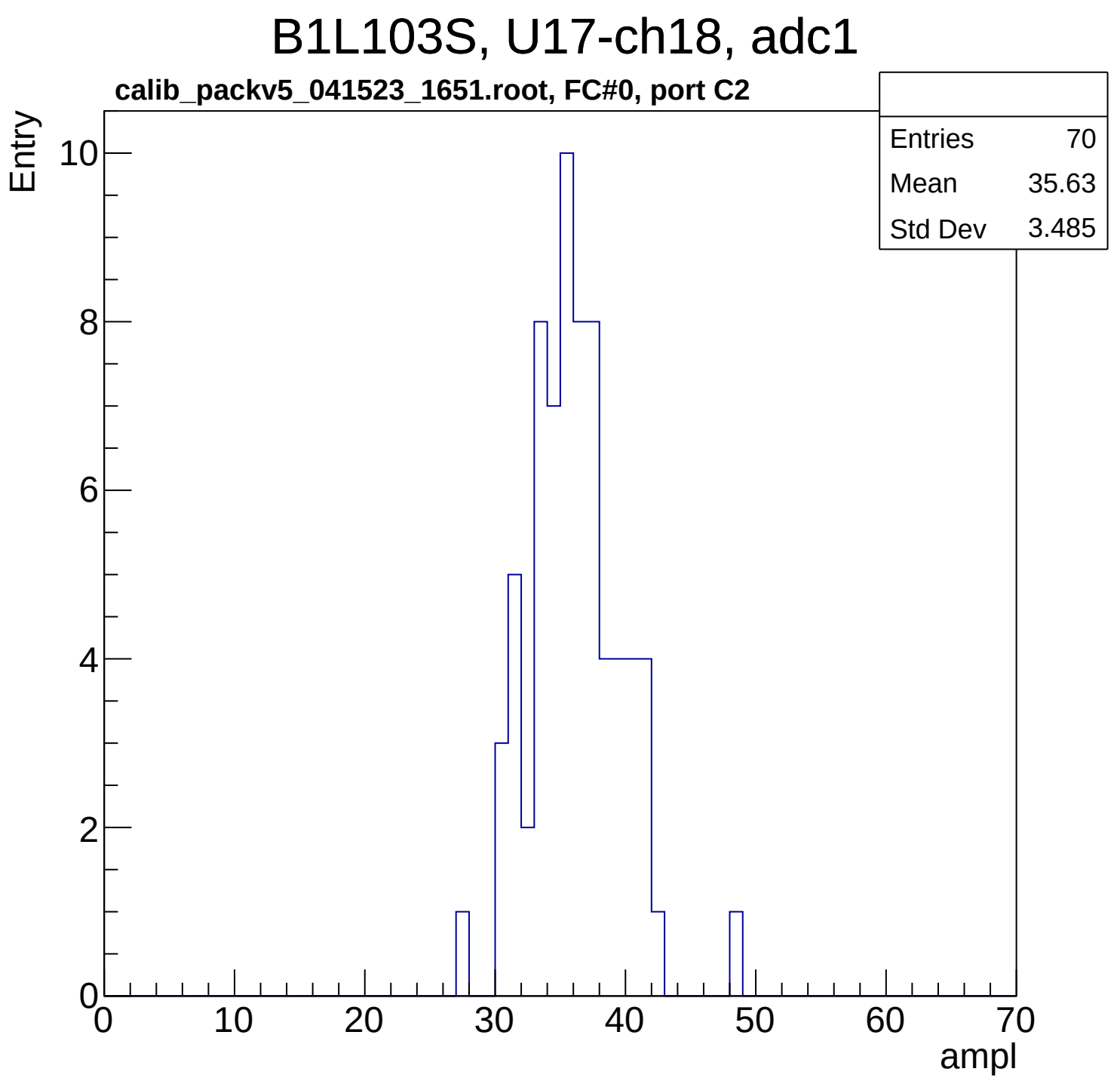

B1L103S, U17-ch17, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 56.61
Std Dev 2.849
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

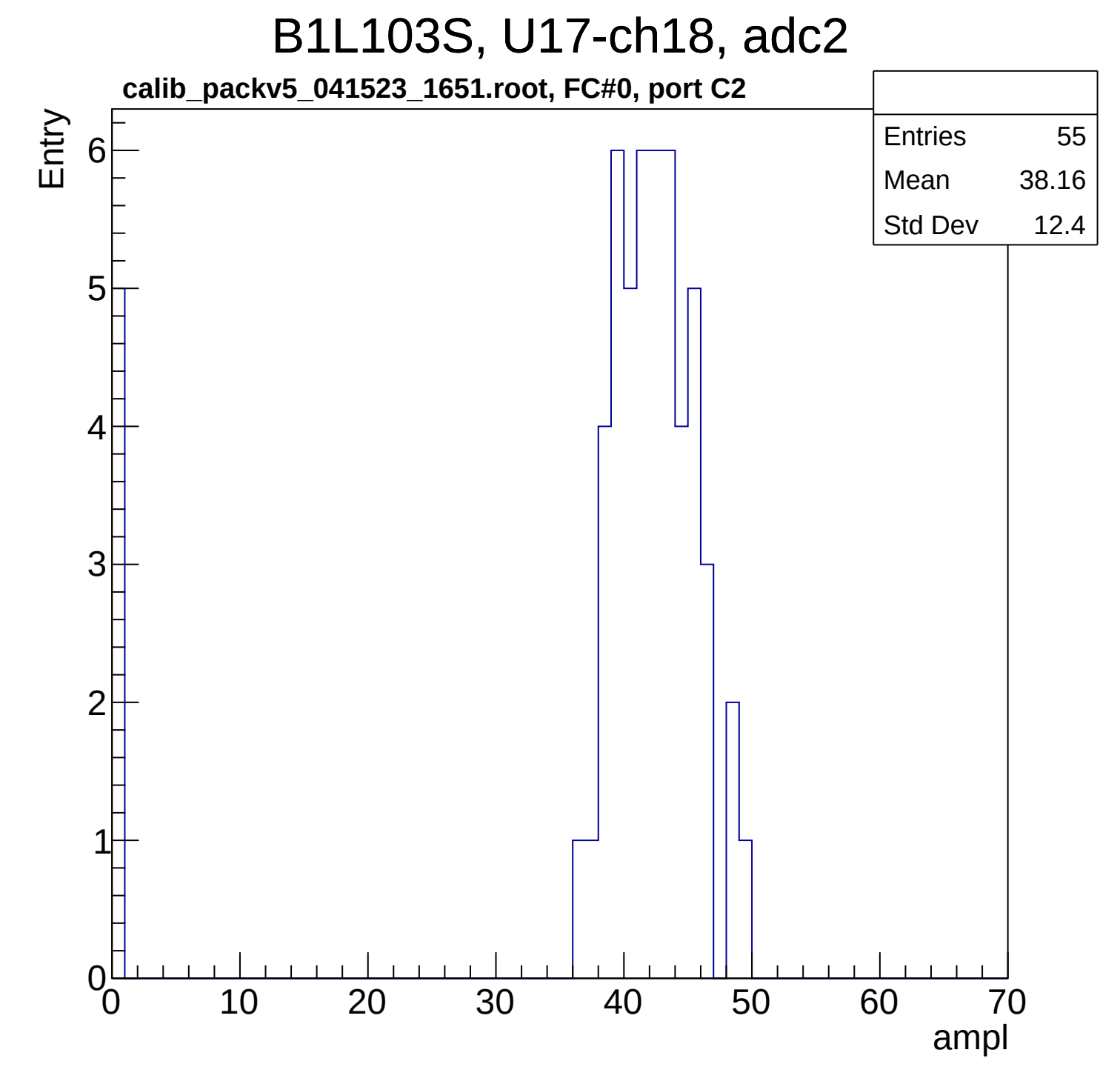

B1L103S, U17-ch17, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 41
Mean 59.22
Std Dev 9.623
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

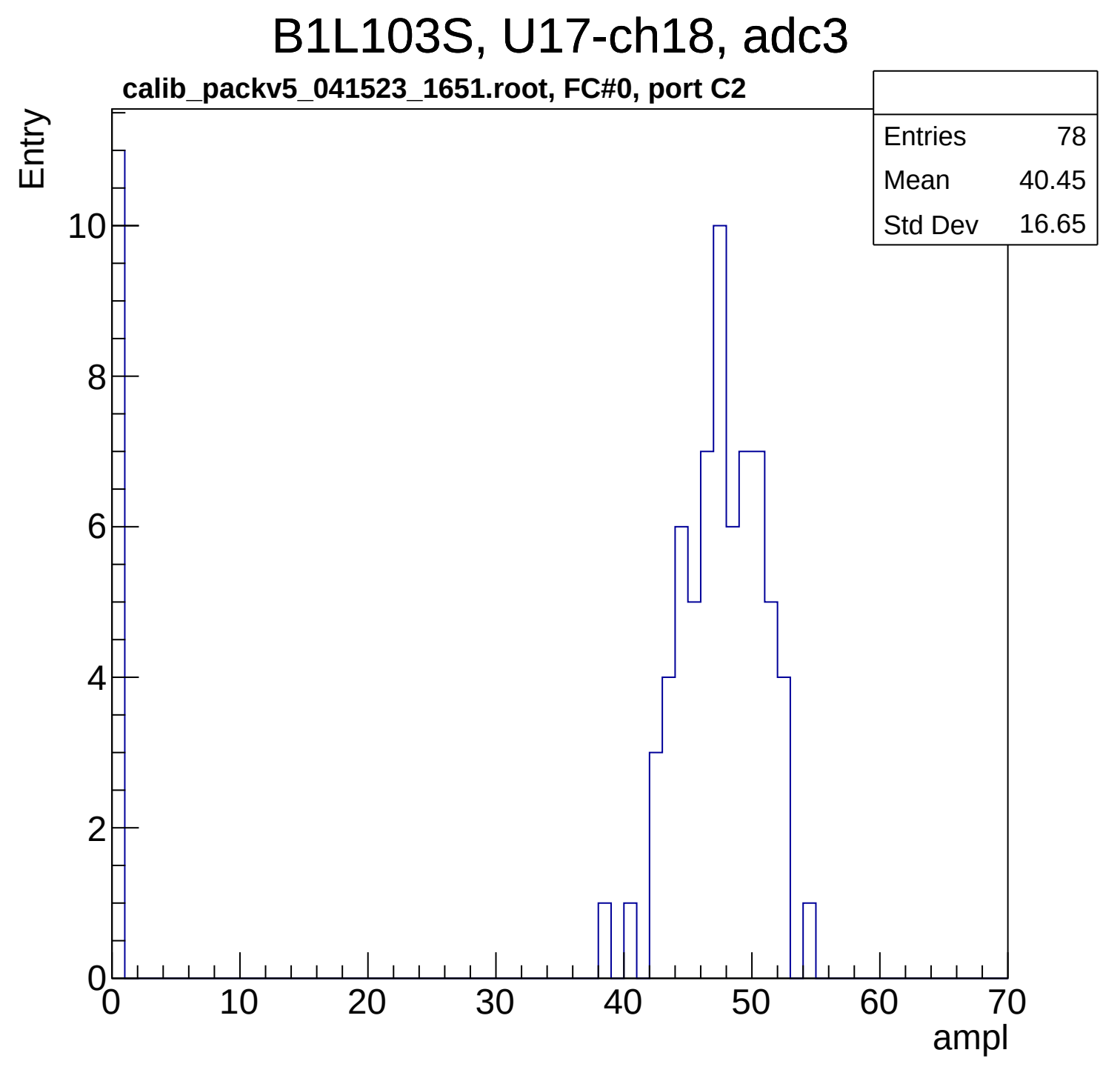

B1L103S, U17-ch17, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 3
Mean 60
Std Dev 1.414
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

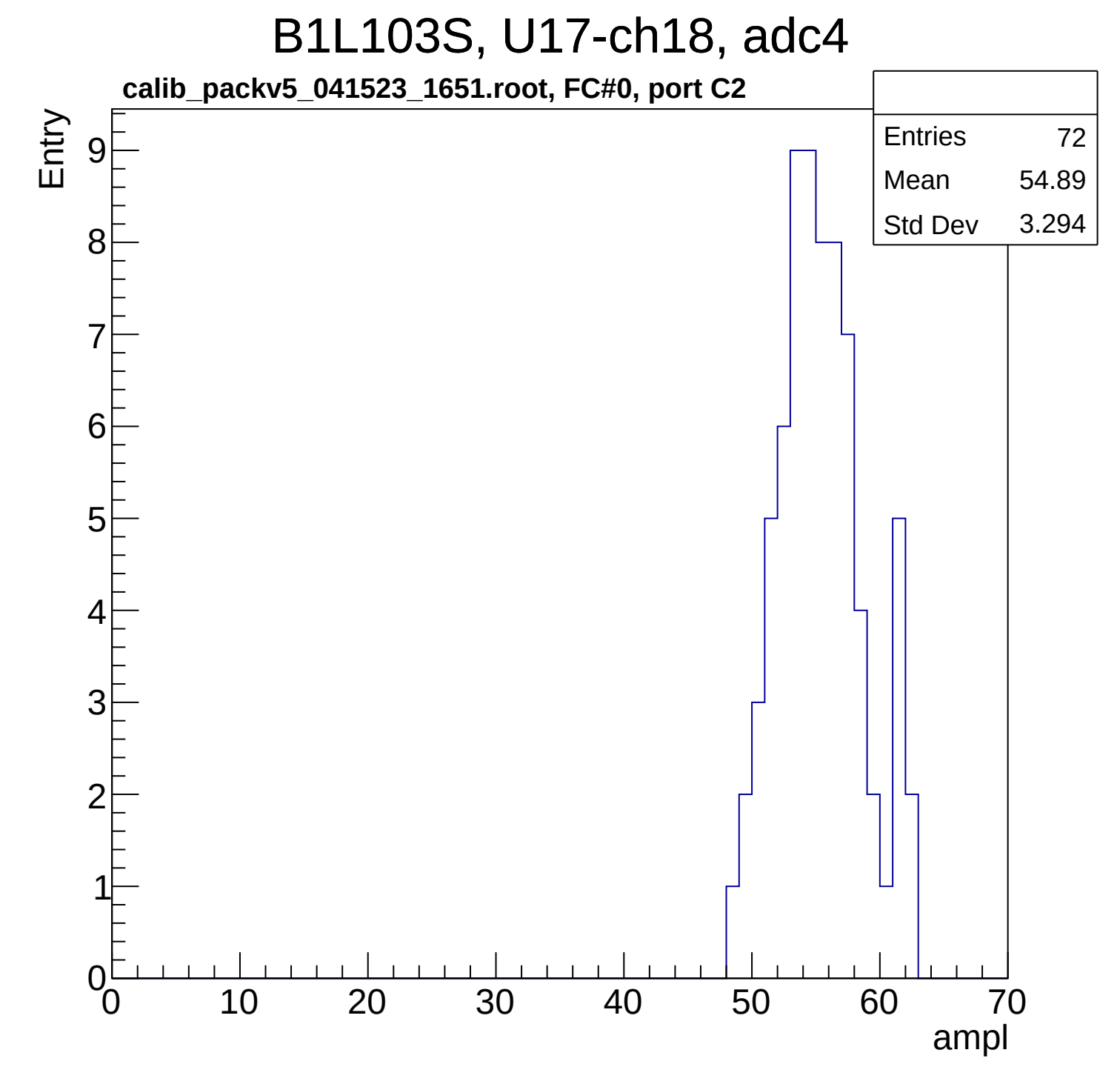

B1L103S, U17-ch17, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1
Std Dev 4.243
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch18, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 103
Mean 22.19
Std Dev 11.75
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
22
0
10
20
30
40
50
60
70


B1L103S, U17-ch18, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 35.63
Std Dev 3.485
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U17-ch18, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 38.16
Std Dev 12.4
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch18, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 40.45
Std Dev 16.65
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch18, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 54.89
Std Dev 3.294
Entry
ampl
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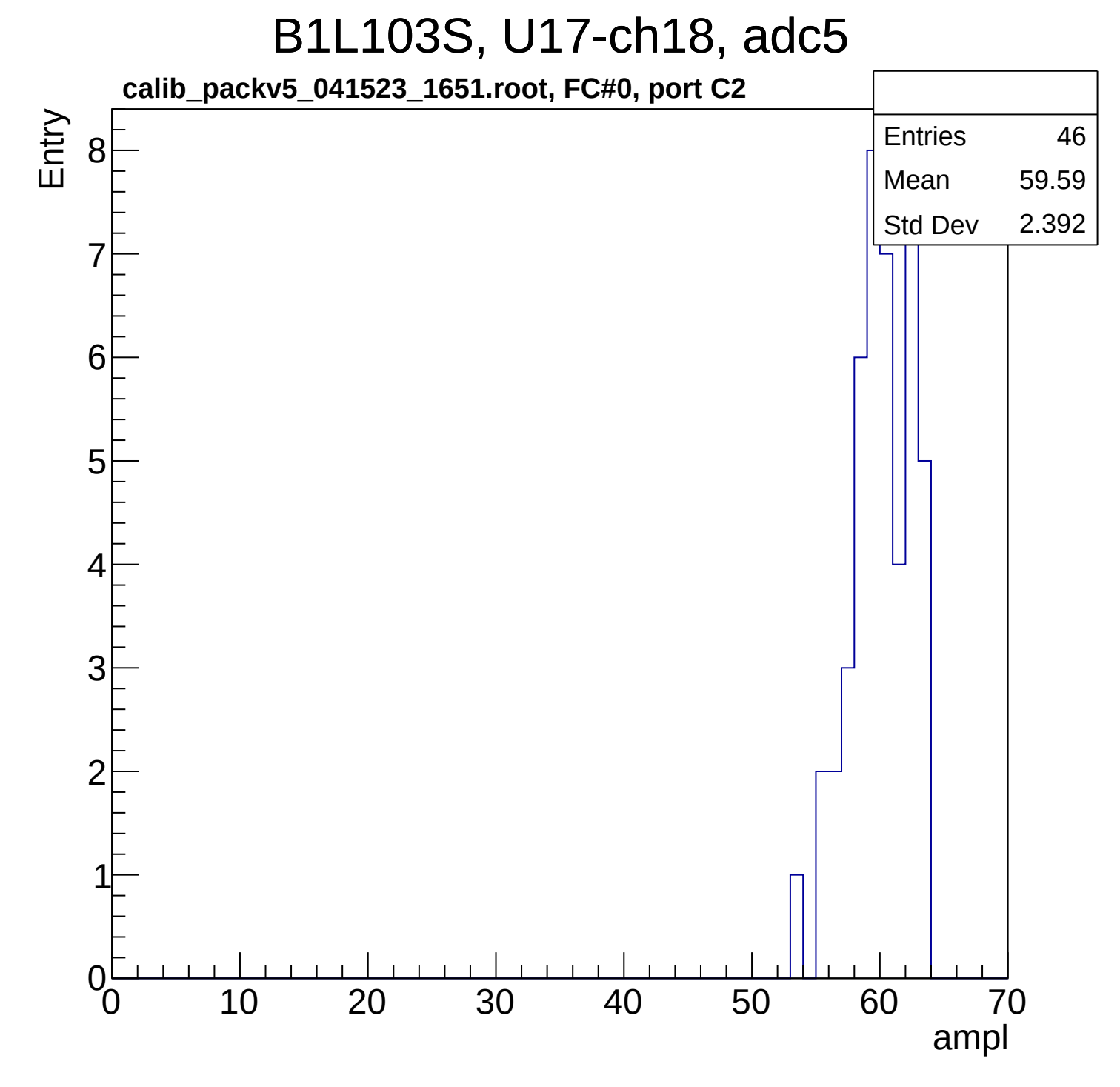
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9


B1L103S, U17-ch18, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 59.59
Std Dev 2.392
Entry
ampl
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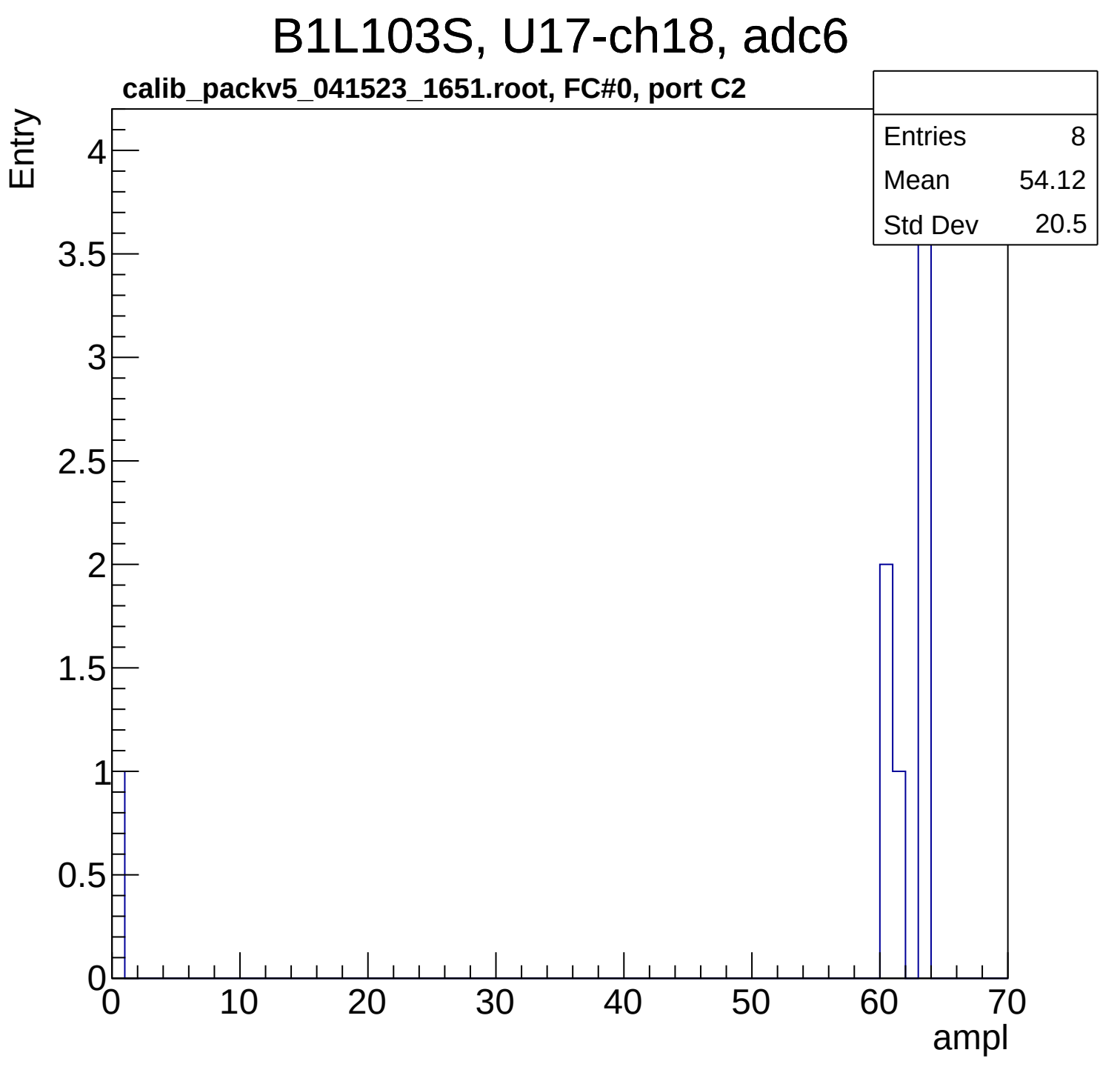
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U17-ch18, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 54.12
Std Dev 20.5
Entry
ampl
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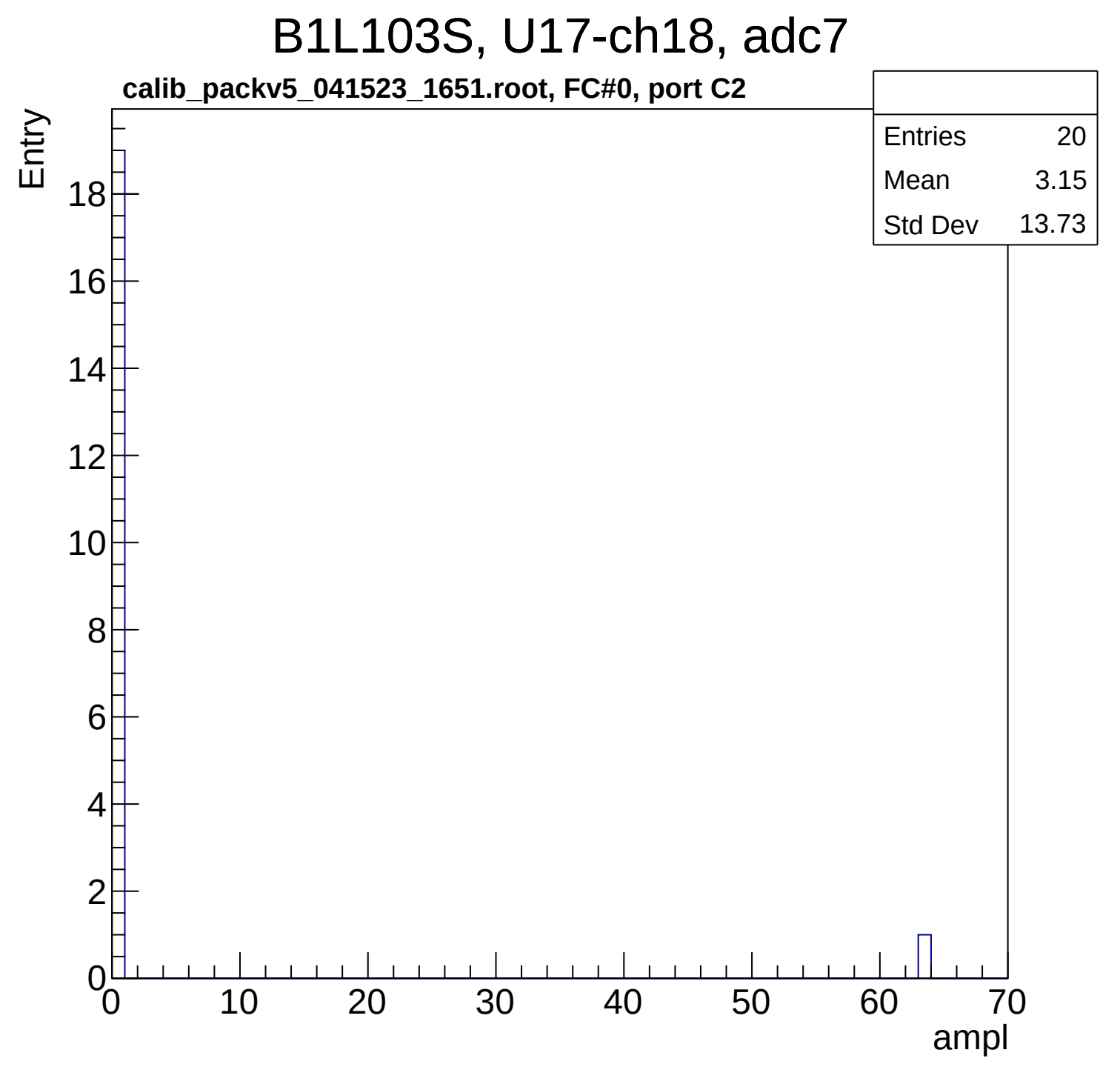
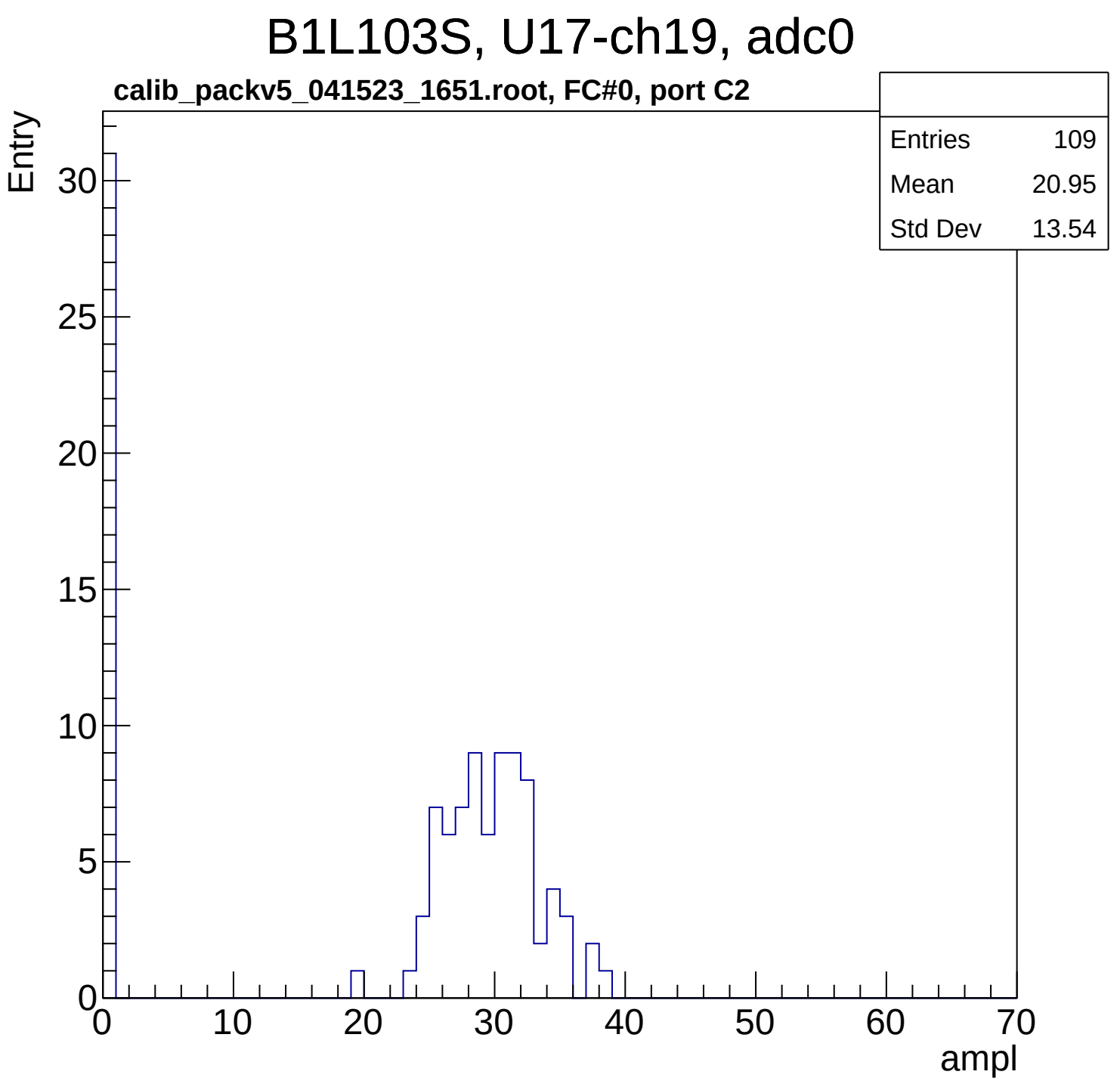
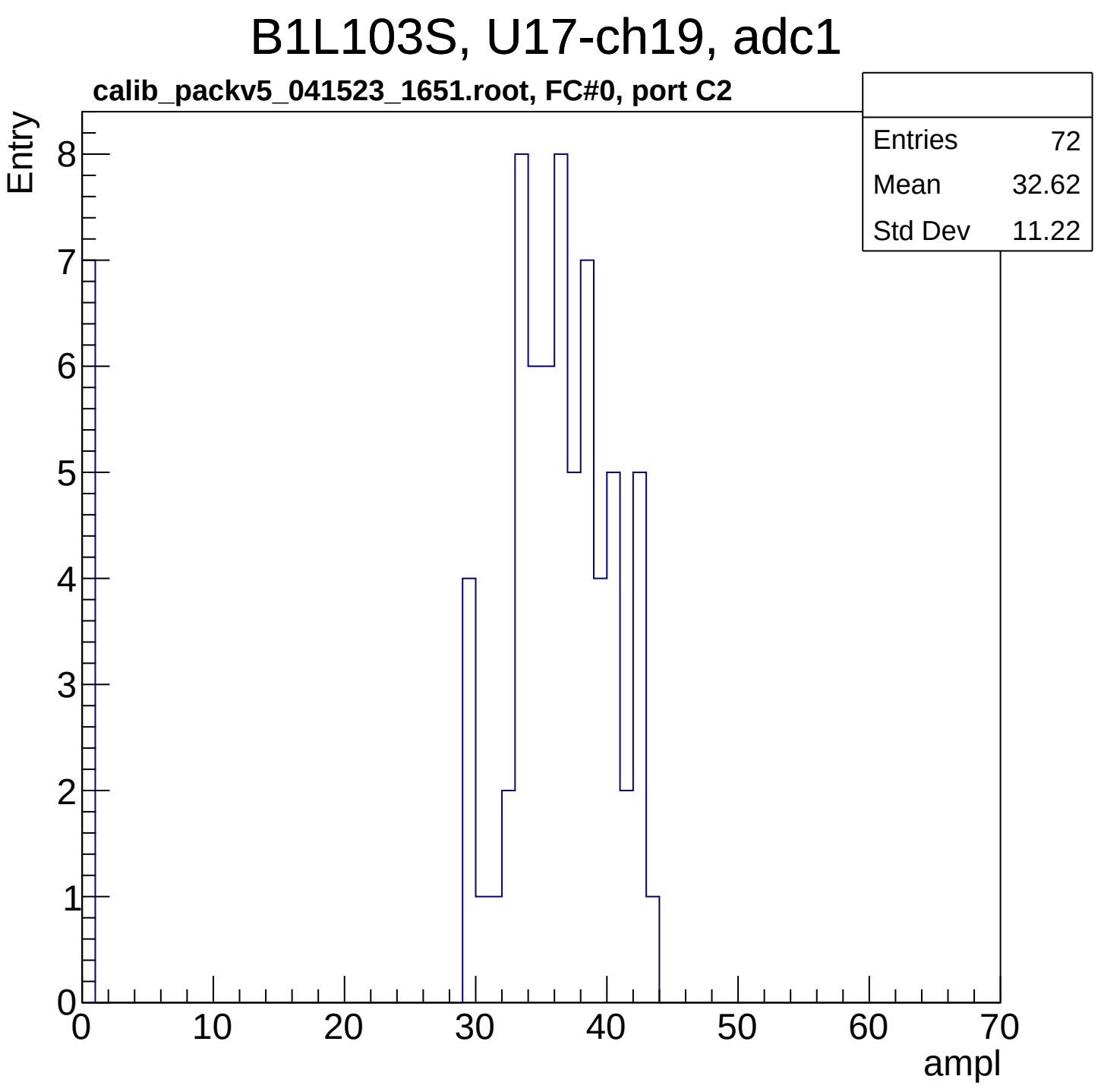
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U17-ch18, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch19, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 109
Mean 20.95
Std Dev 13.54
Entry
0
5
10
15
20
25
30
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch19, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 32.62
Std Dev 11.22
Entry
ampl
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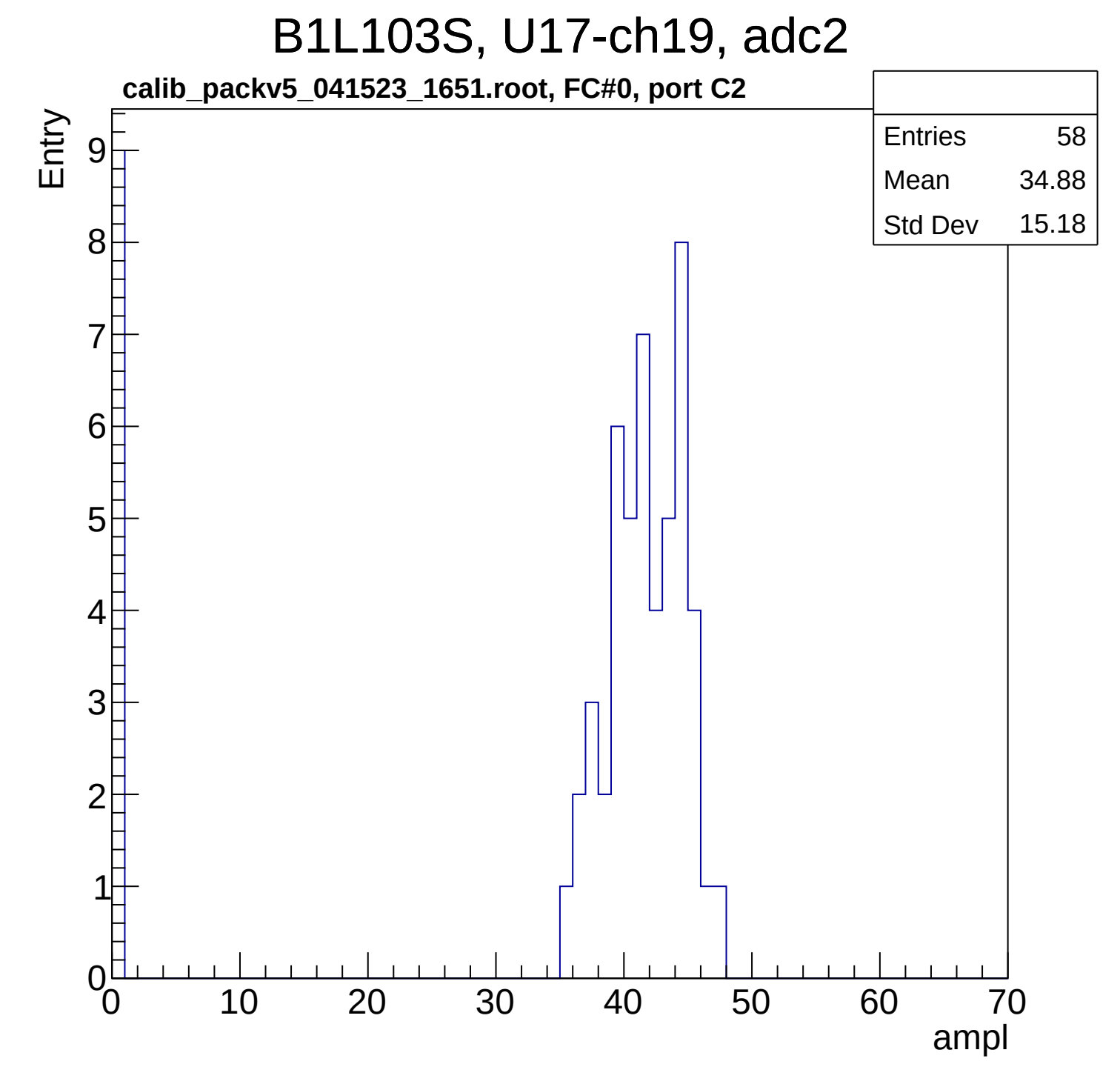
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U17-ch19, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 34.88
Std Dev 15.18
Entry
ampl
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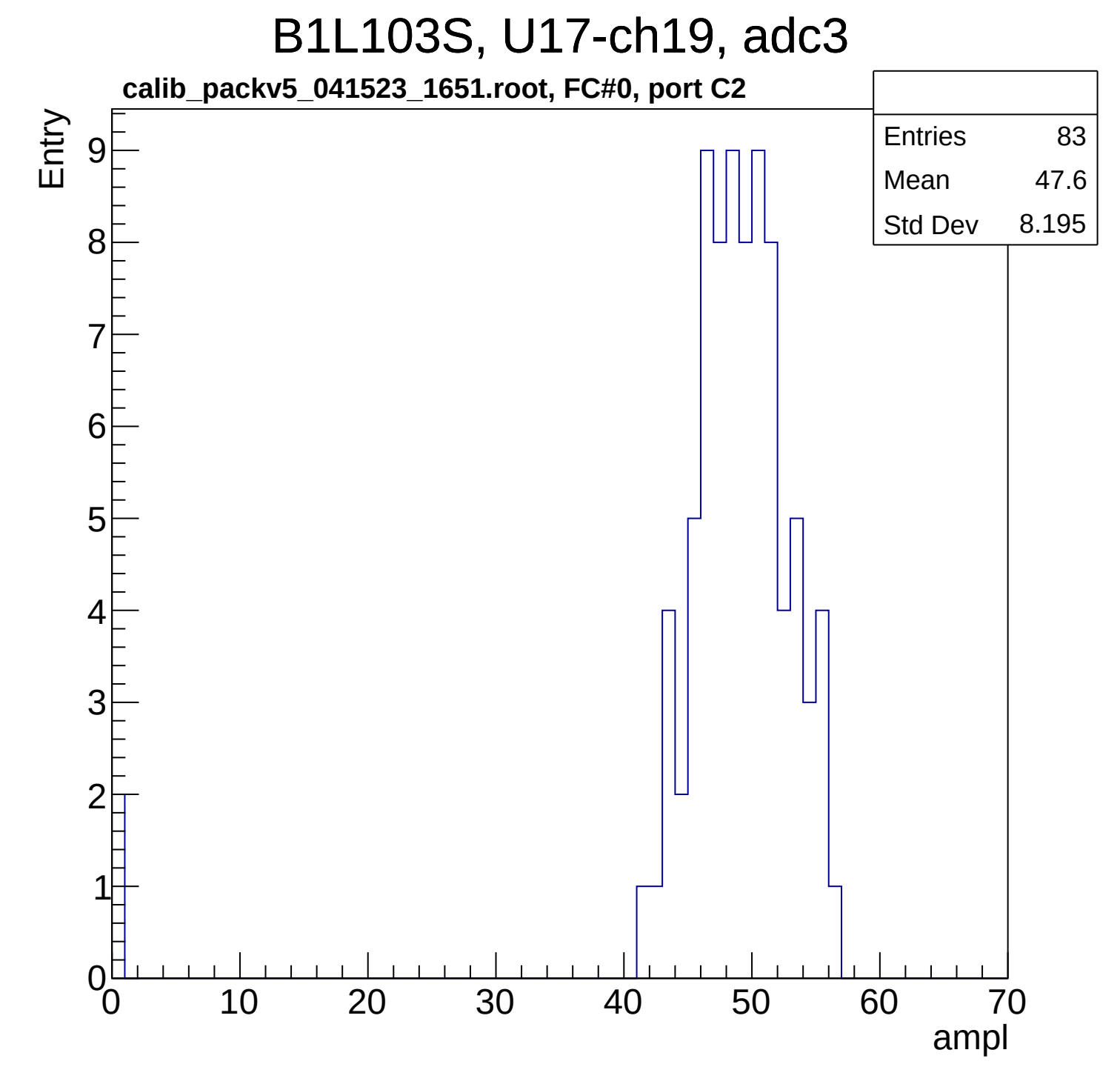
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U17-ch19, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 47.6
Std Dev 8.195
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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40
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60
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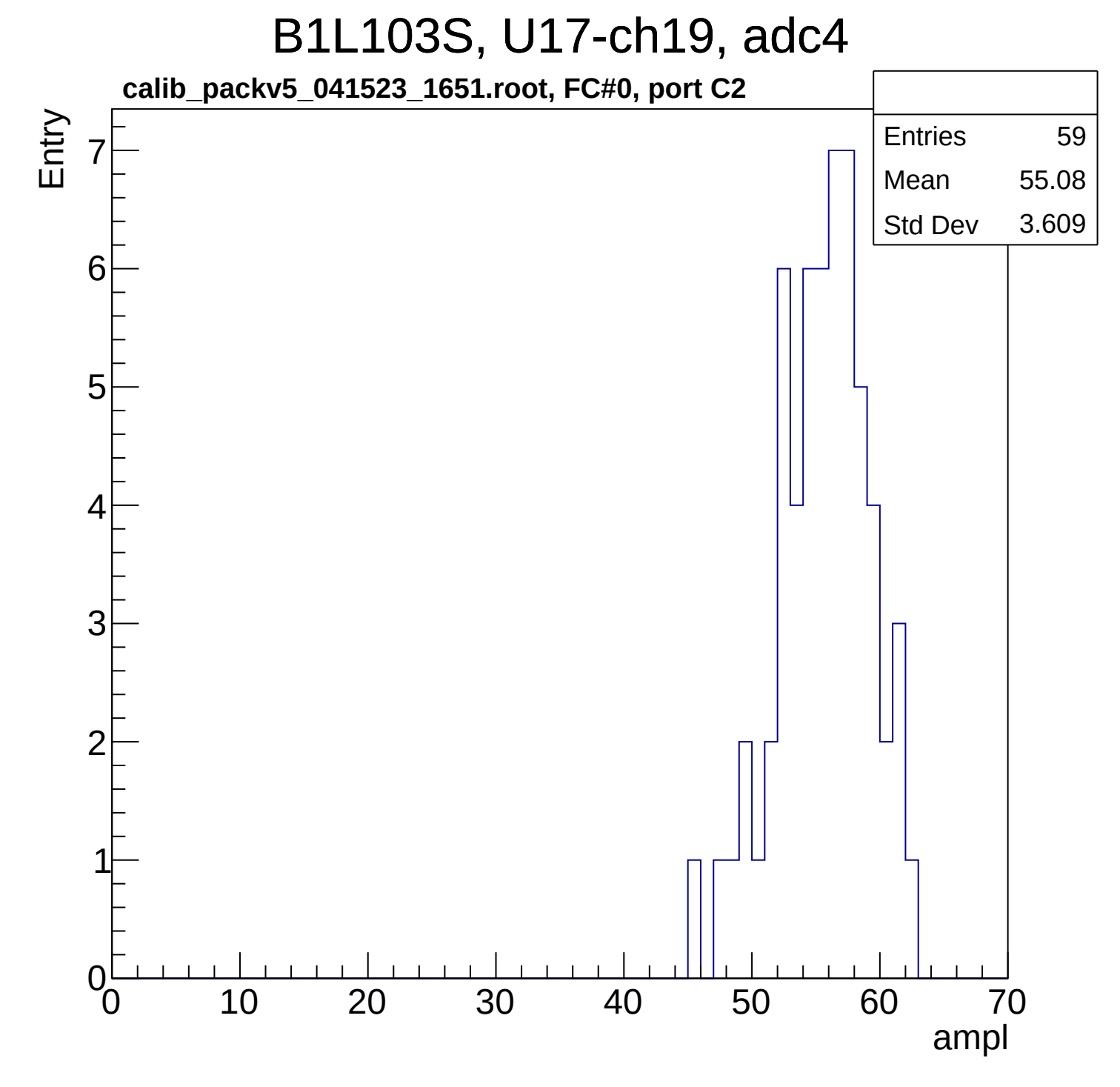
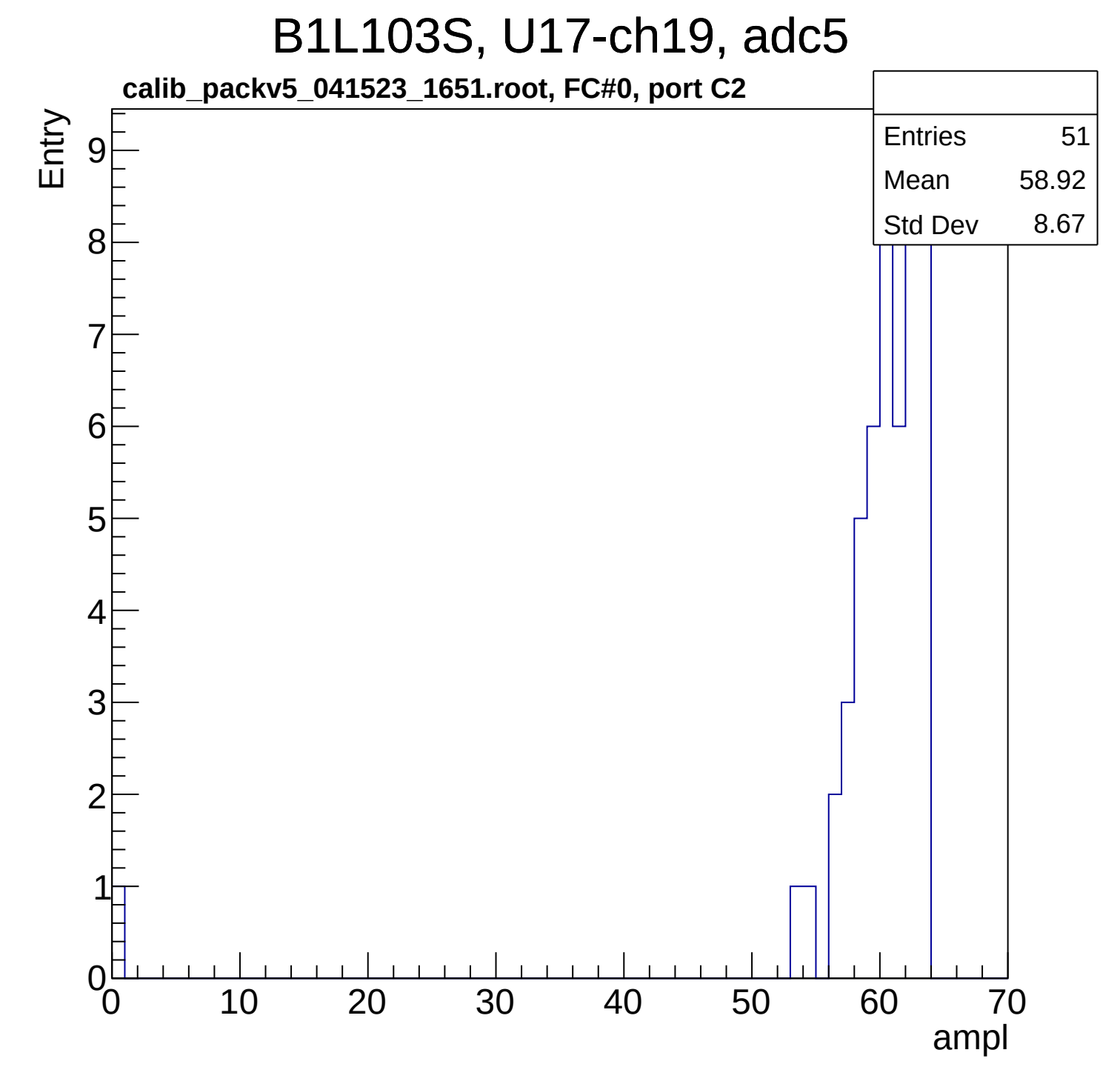
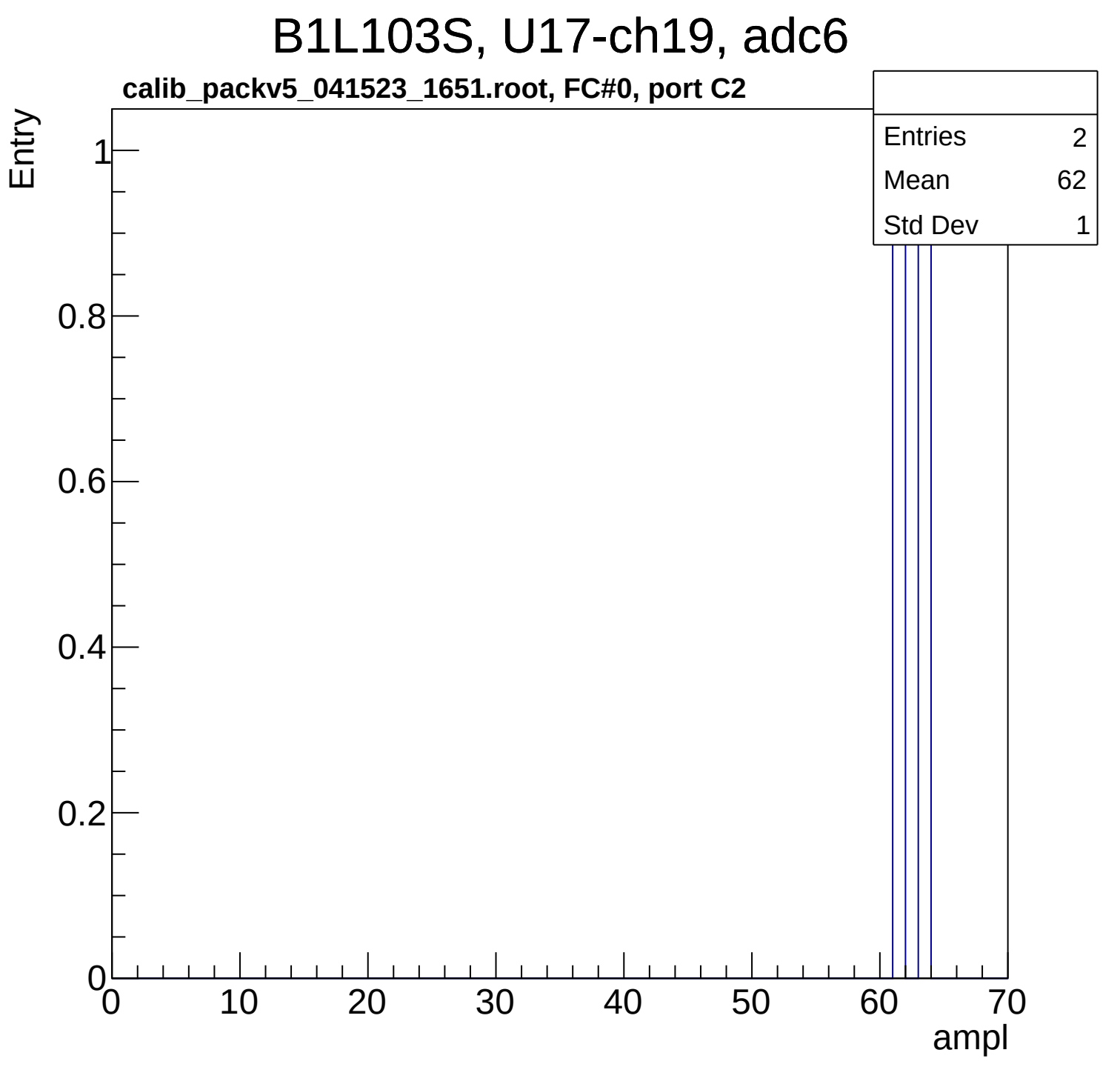

B1L103S, U17-ch19, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 55.08
Std Dev 3.609
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U17-ch19, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 58.92
Std Dev 8.67
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U17-ch19, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 2
Mean 62
Std Dev 1
Entry
1
0.8
0.6
0.4
0.2
0
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10
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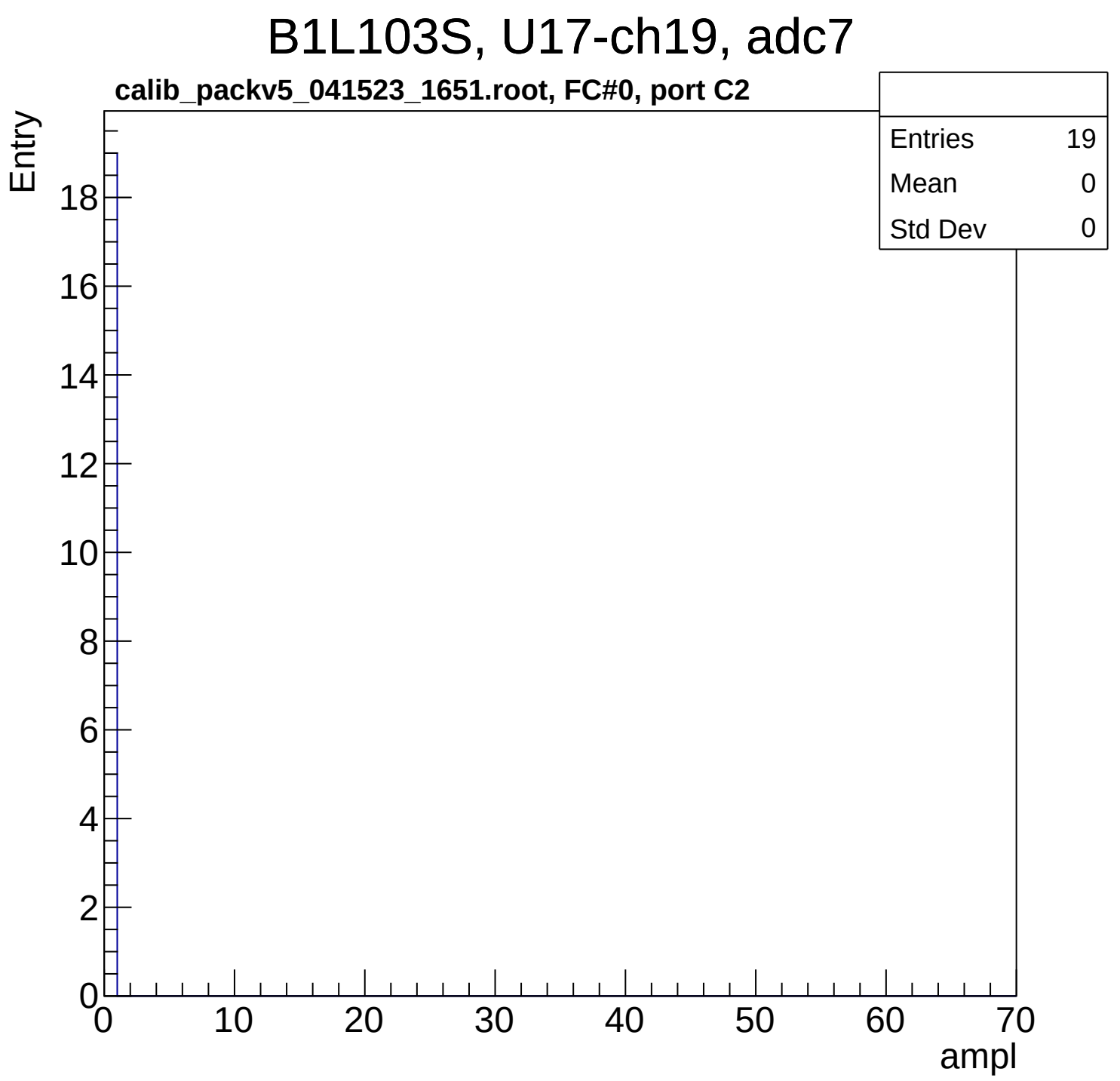
60
70
ampl


B1L103S, U17-ch19, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
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14
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18
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10
20
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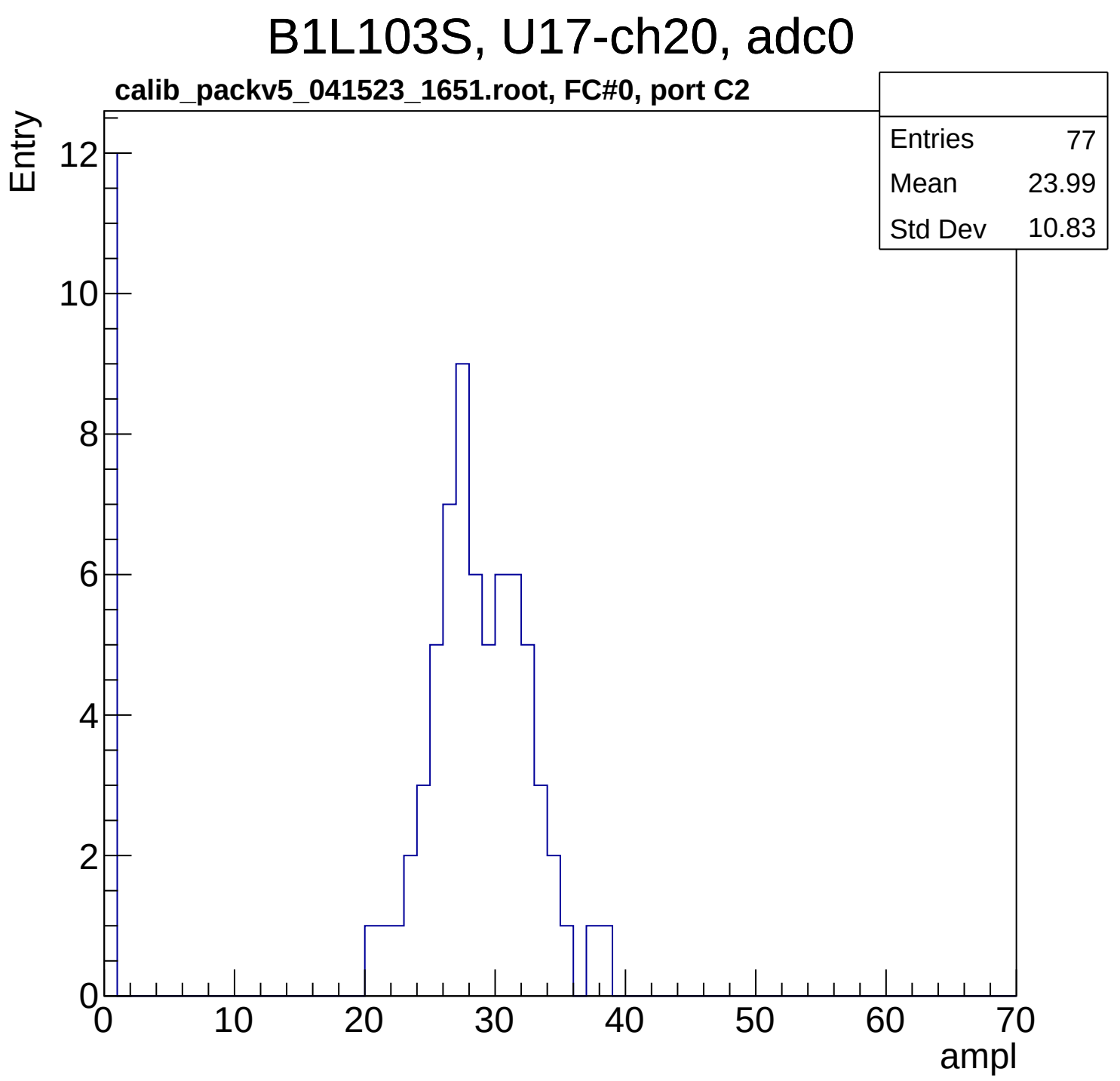
50
60
70
ampl


B1L103S, U17-ch20, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 23.99
Std Dev 10.83
Entry
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4
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8
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12
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30
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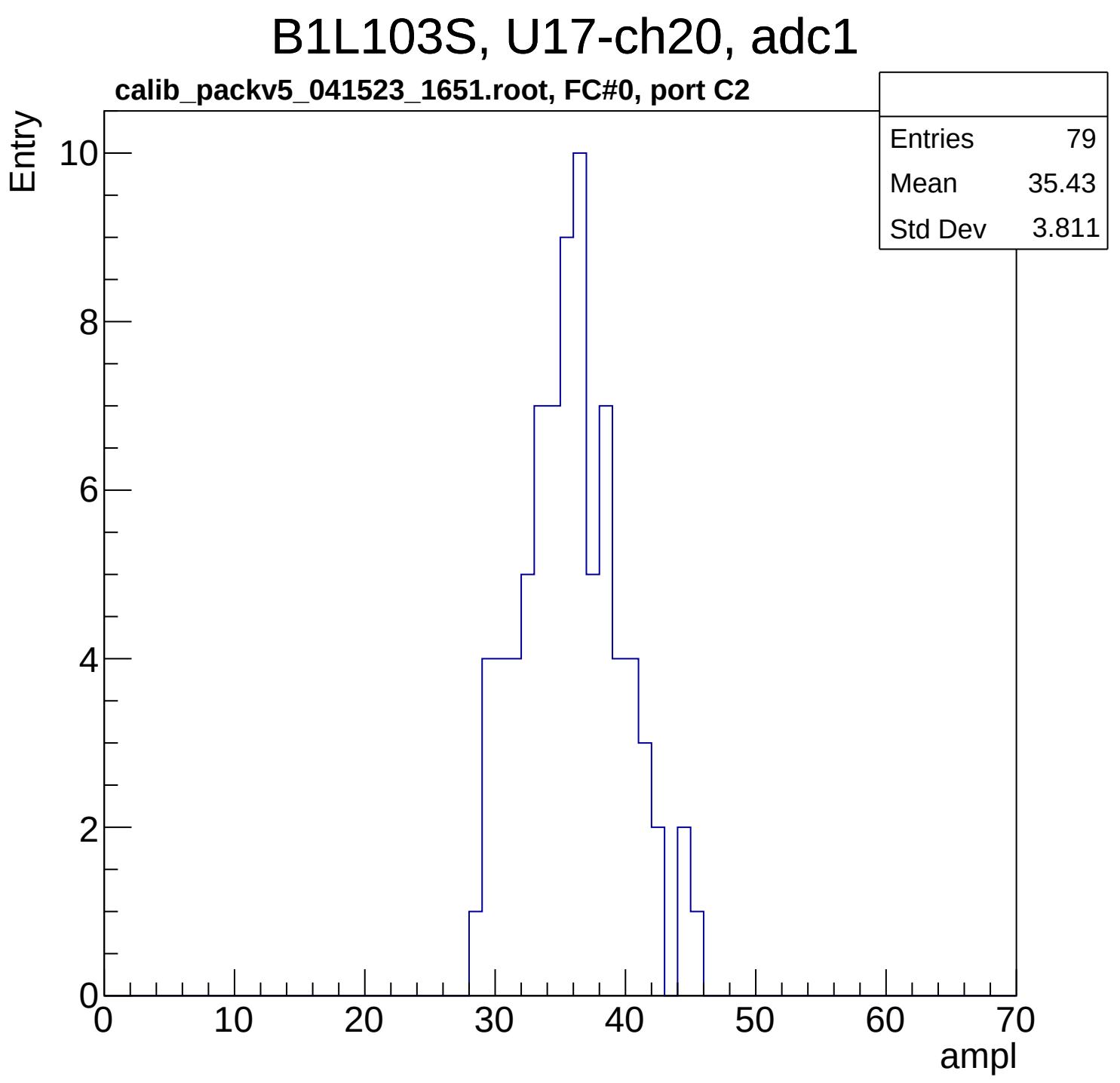
50
60
70
ampl


B1L103S, U17-ch20, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 35.43
Std Dev 3.811
Entry
ampl
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60
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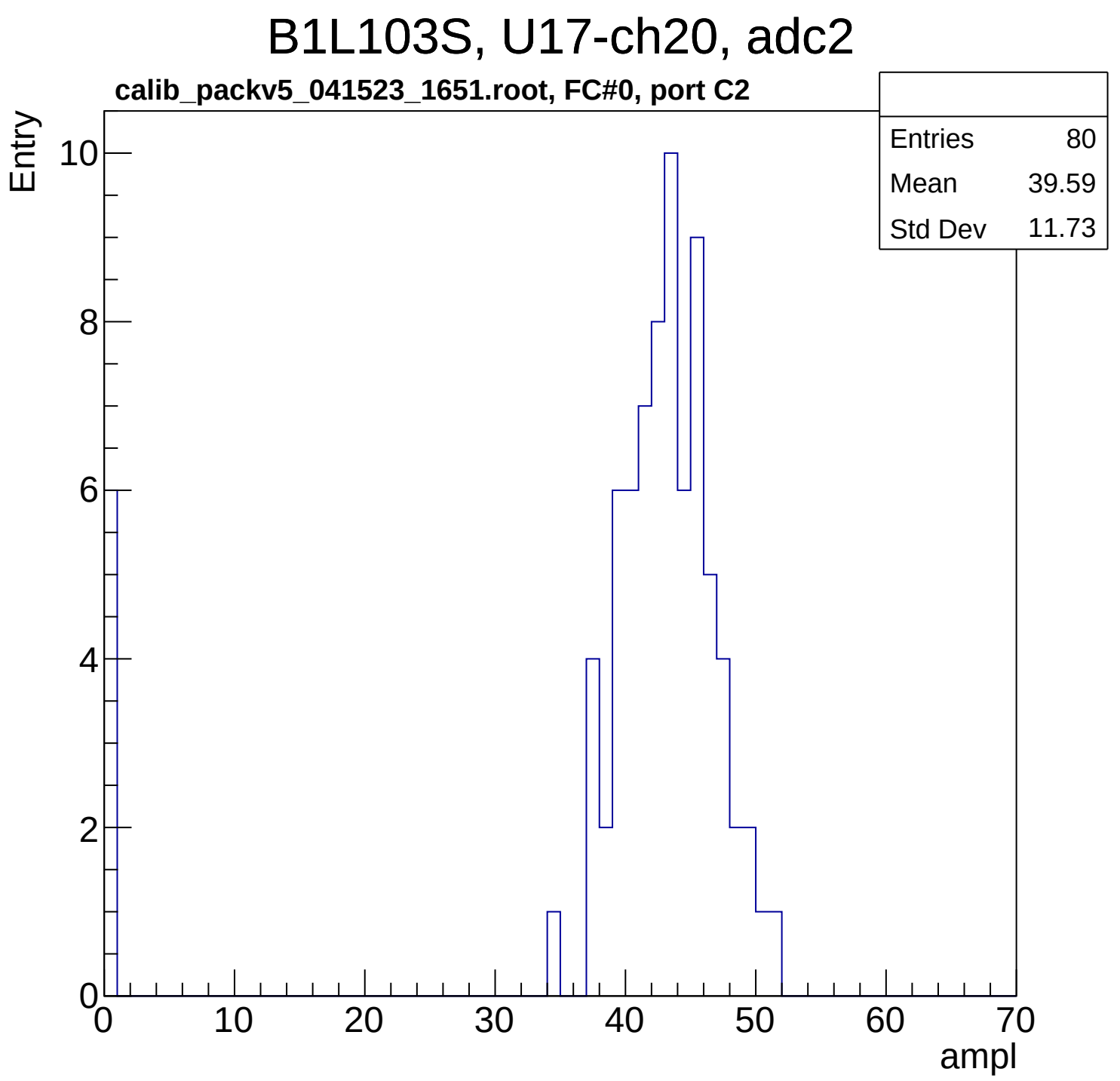
B1L103S, U17-ch20, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 39.59
Std Dev 11.73
Entry
ampl
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4
6
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0
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40
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60
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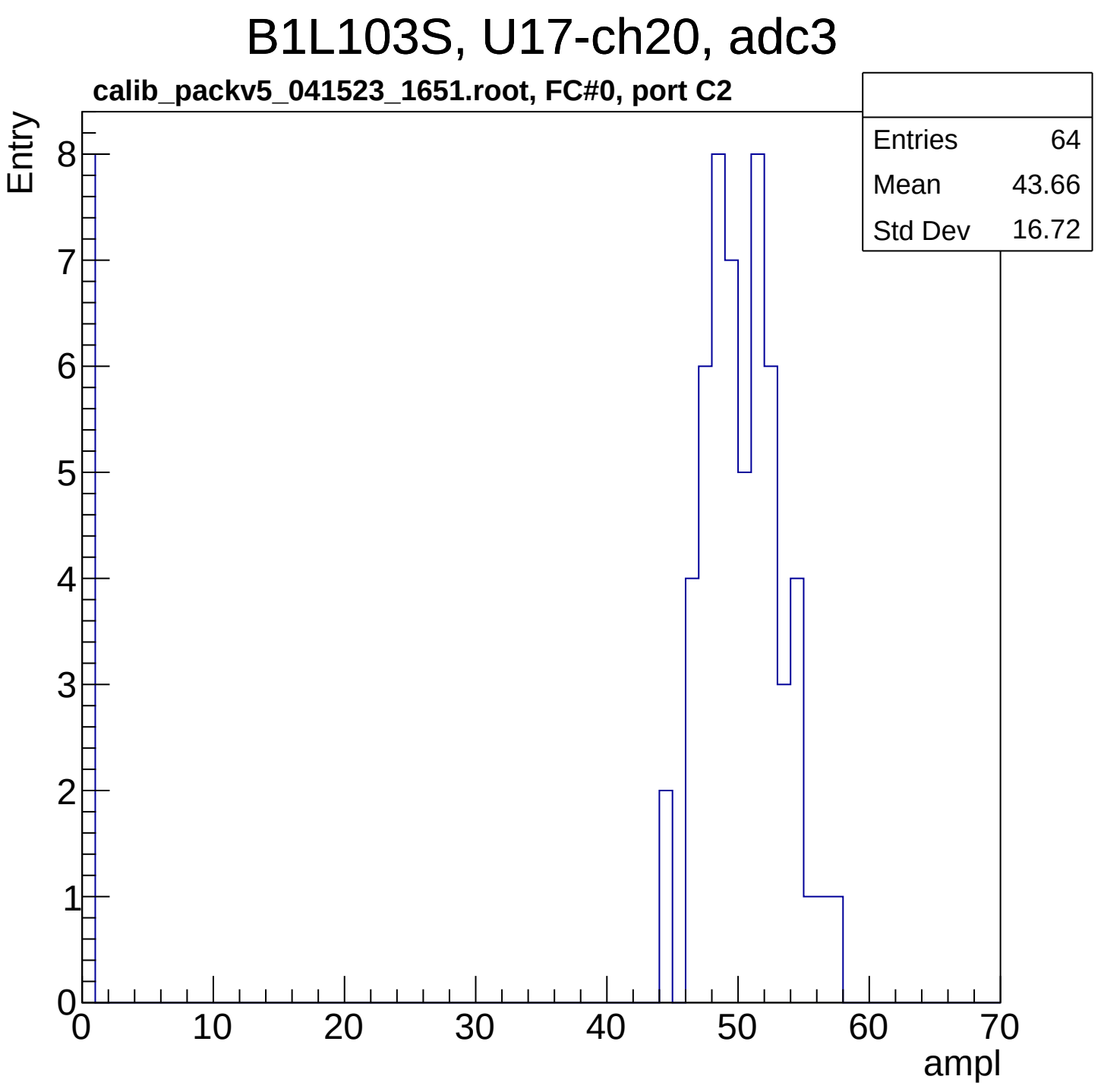
B1L103S, U17-ch20, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 43.66
Std Dev 16.72
Entry
ampl
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1
2
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4
5
6
7
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0
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40
50
60
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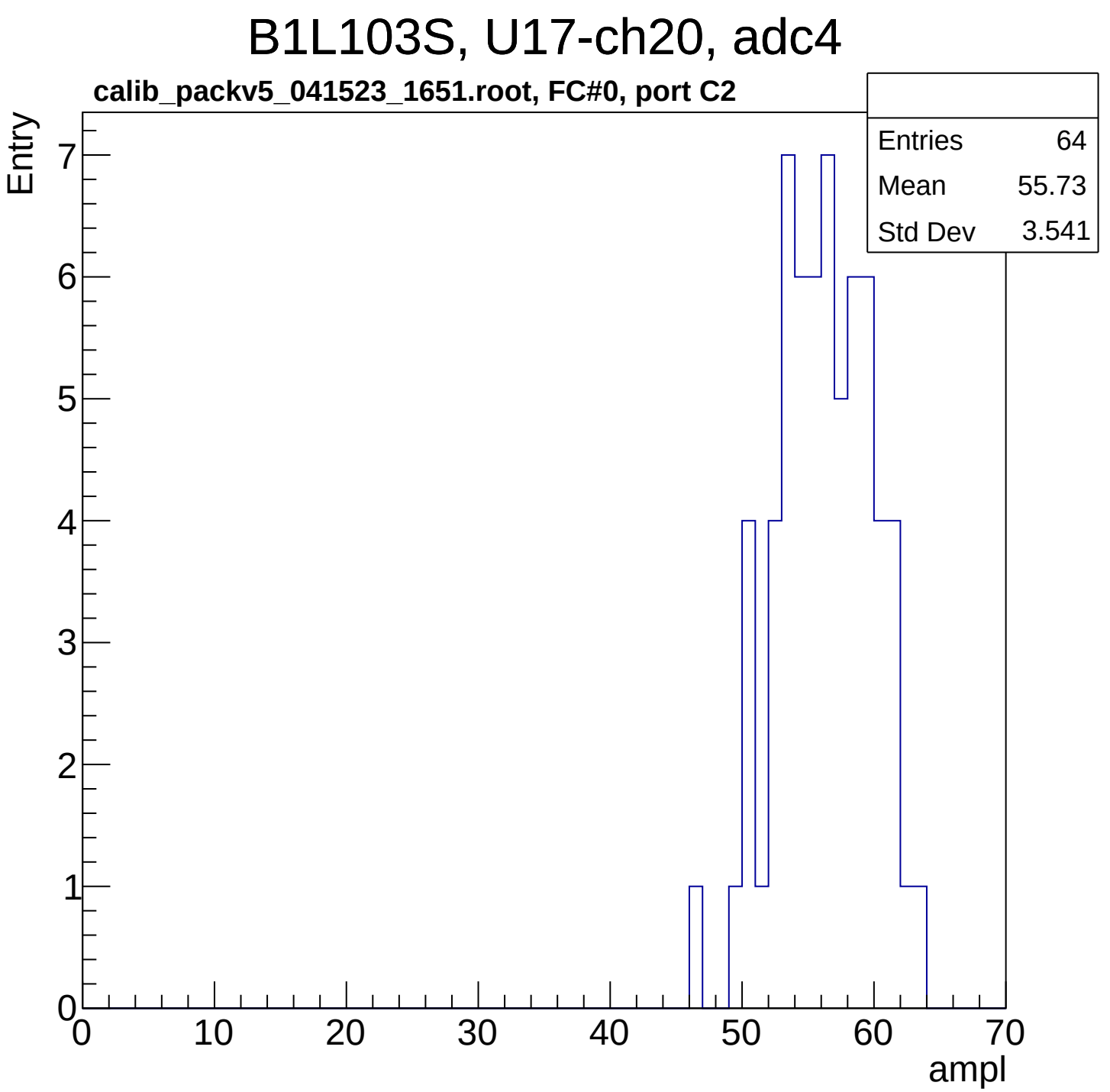
B1L103S, U17-ch20, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 55.73
Std Dev 3.541
Entry
ampl
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1
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4
5
6
7
0
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20
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40
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60
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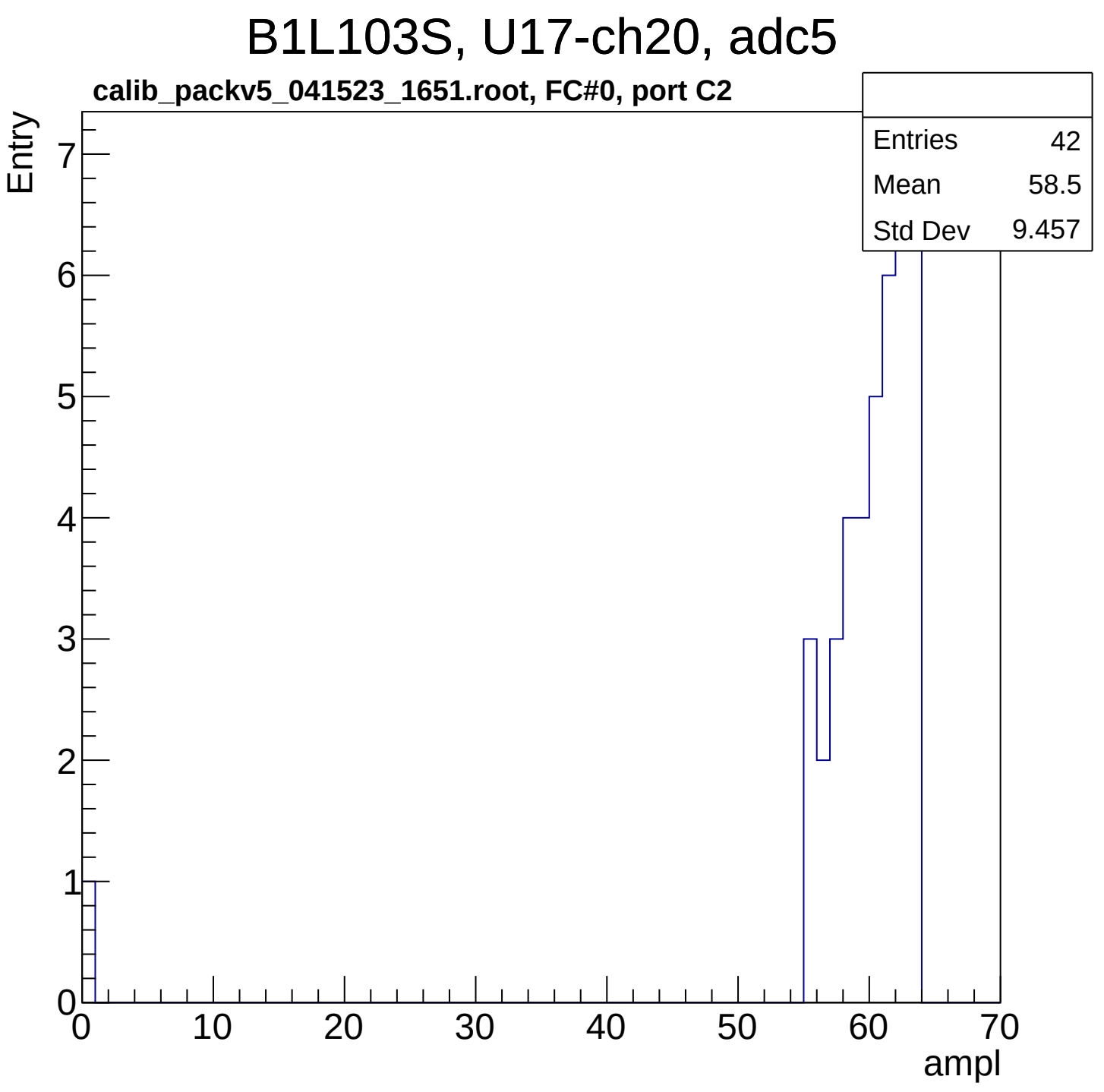
B1L103S, U17-ch20, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 42
Mean 58.5
Std Dev 9.457
Entry
ampl
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1
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3
4
5
6
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0
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40
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60
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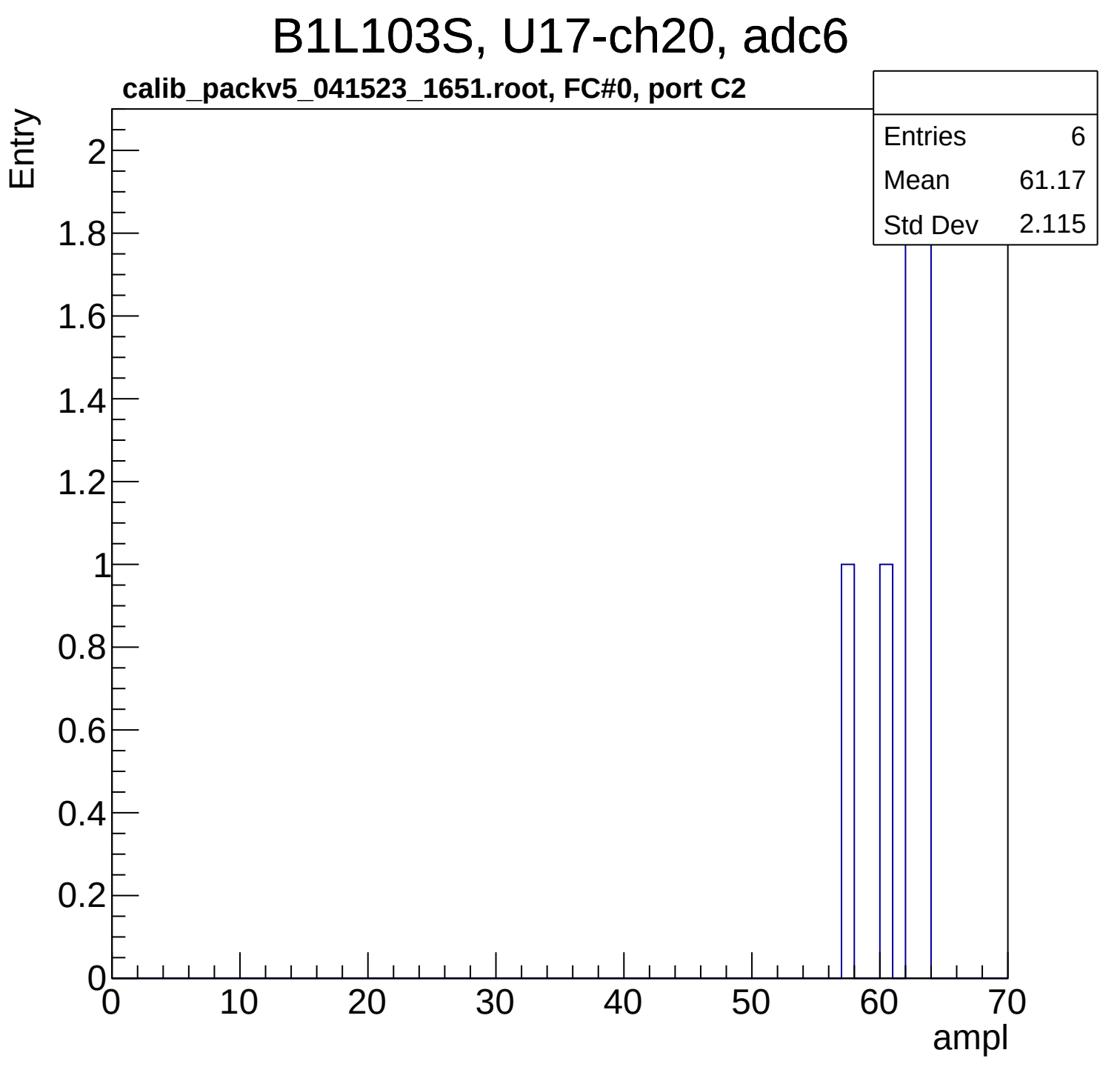
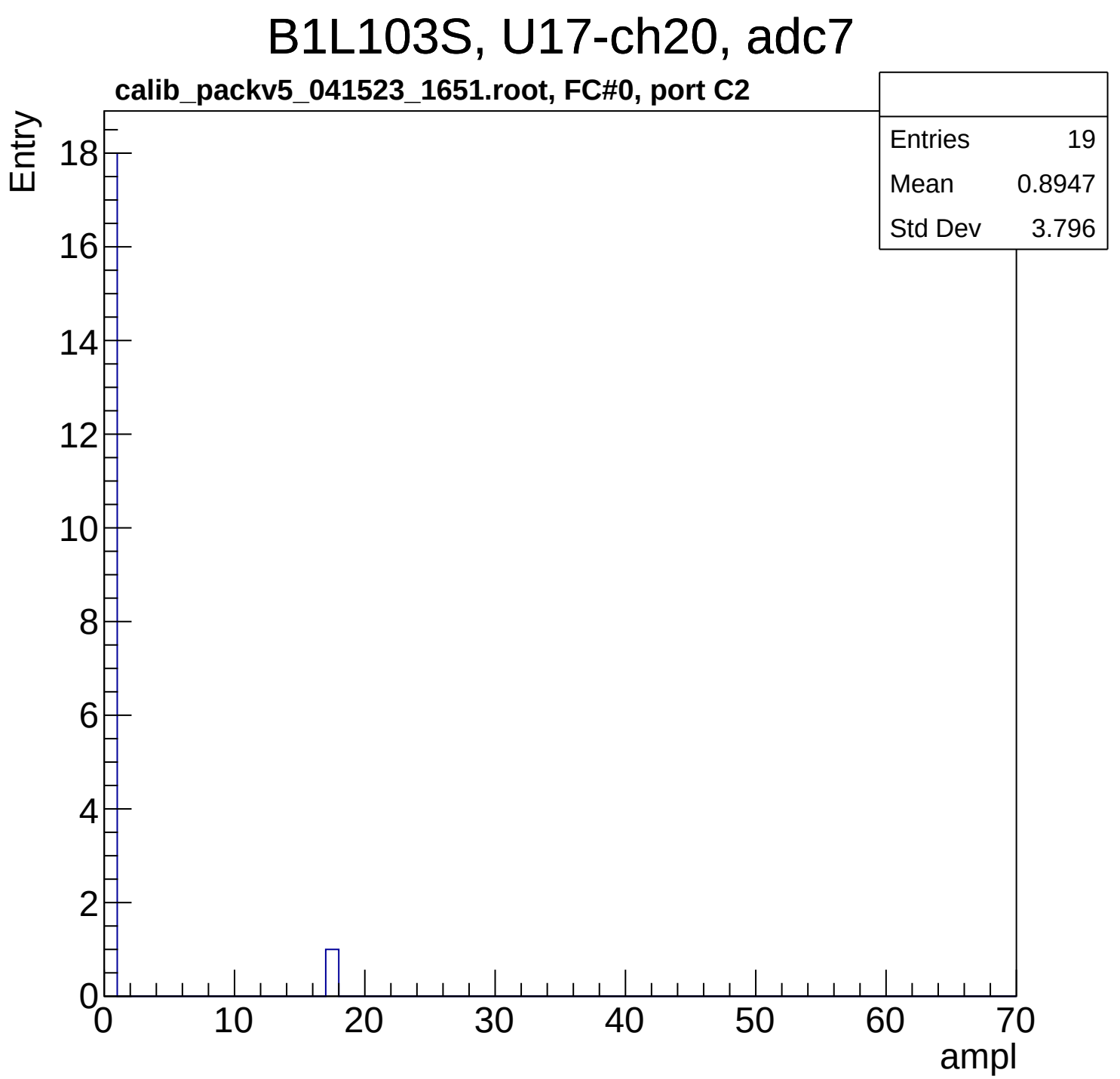
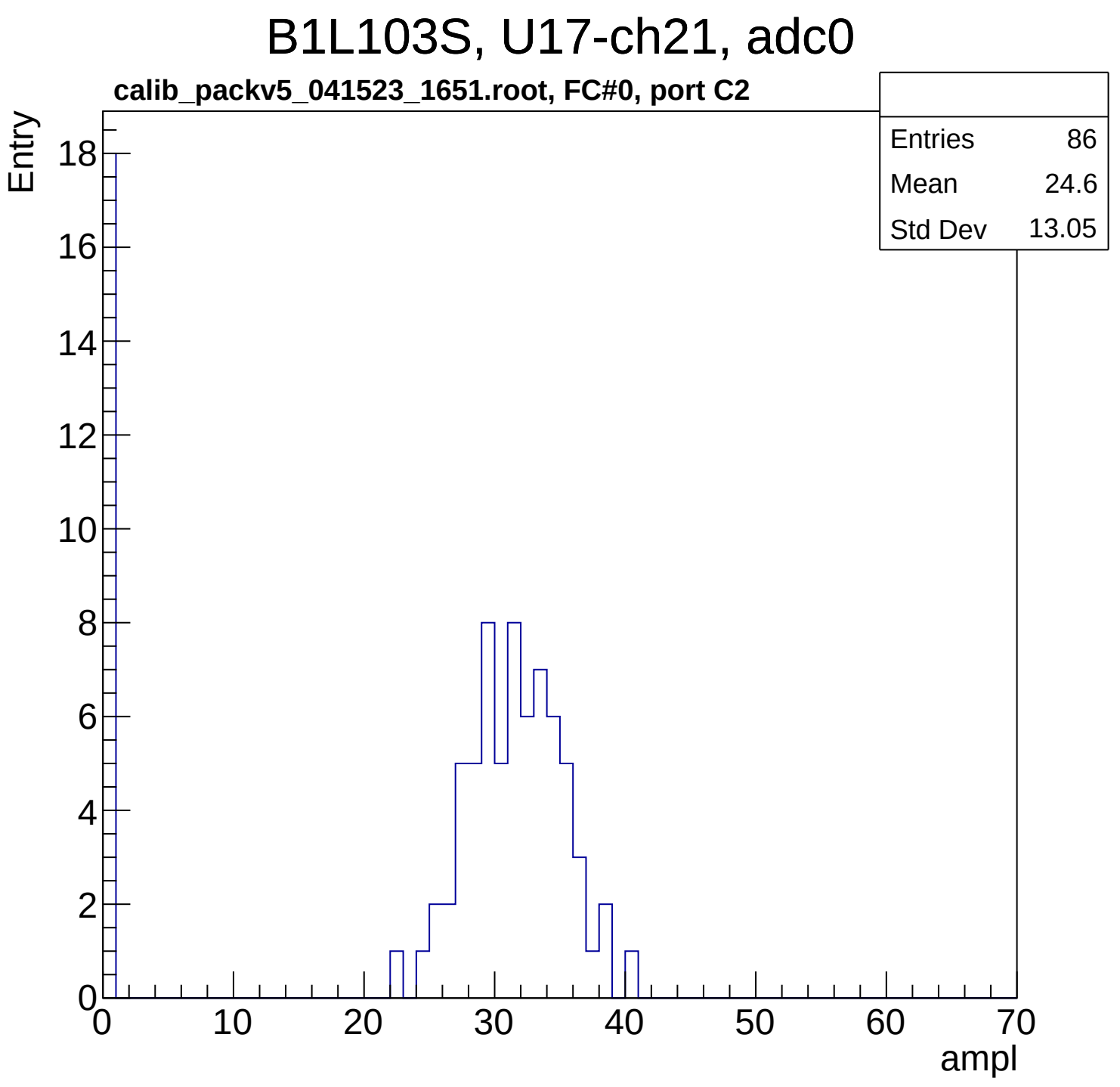
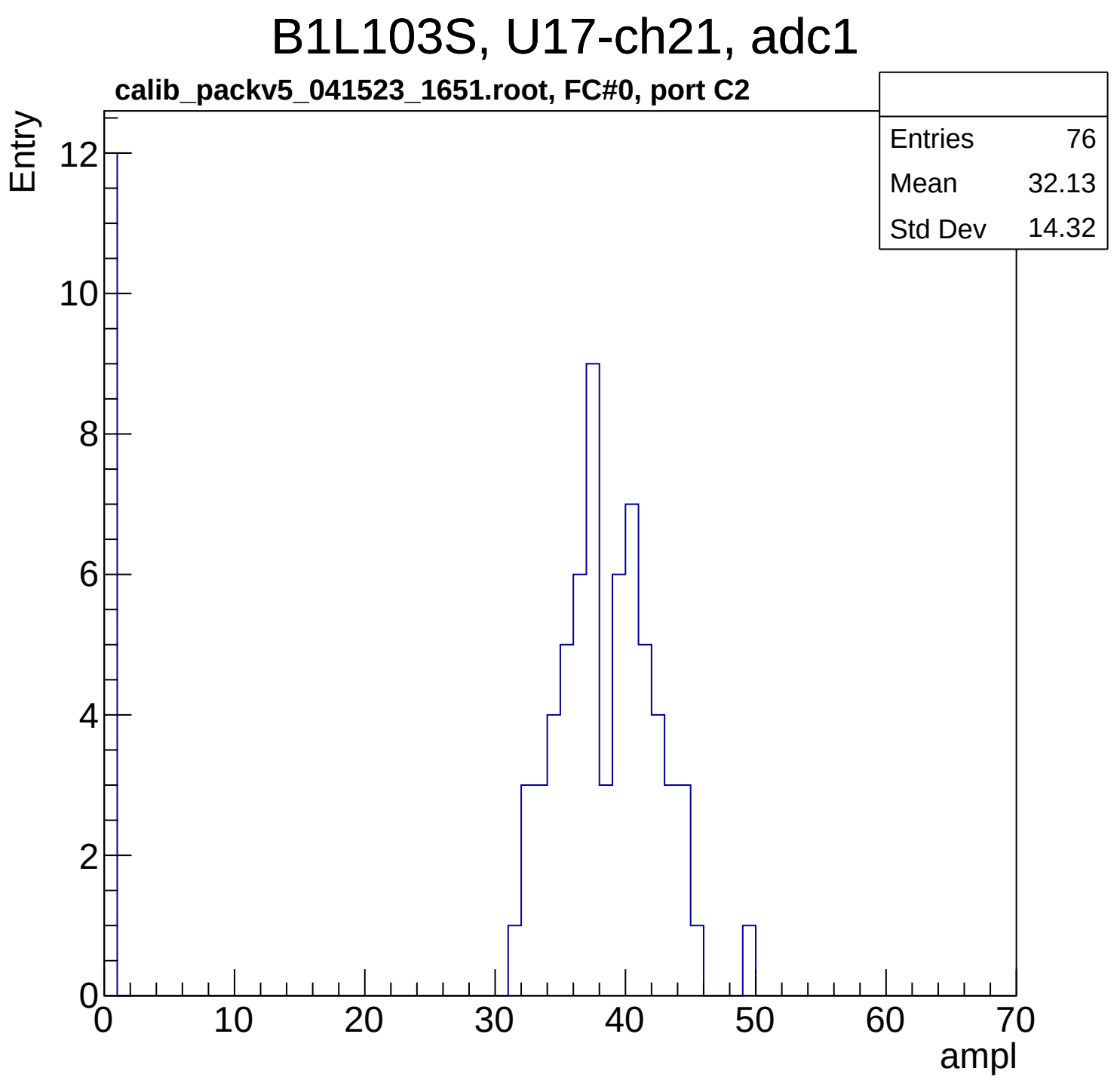
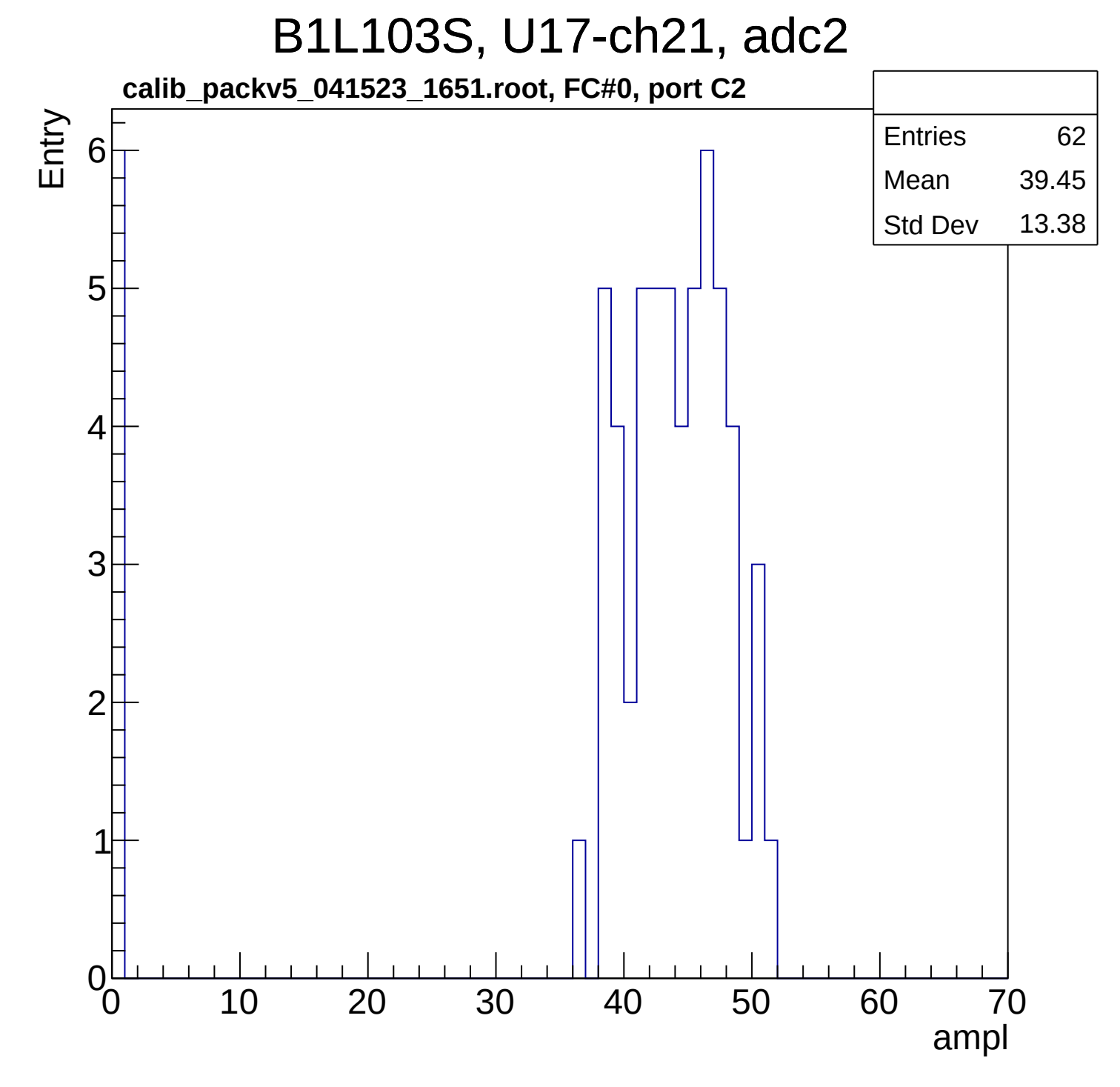

B1L103S, U17-ch20, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 61.17
Std Dev 2.115
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U17-ch20, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0.8947
Std Dev 3.796
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch21, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 24.6
Std Dev 13.05
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch21, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 32.13
Std Dev 14.32
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch21, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 39.45
Std Dev 13.38
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
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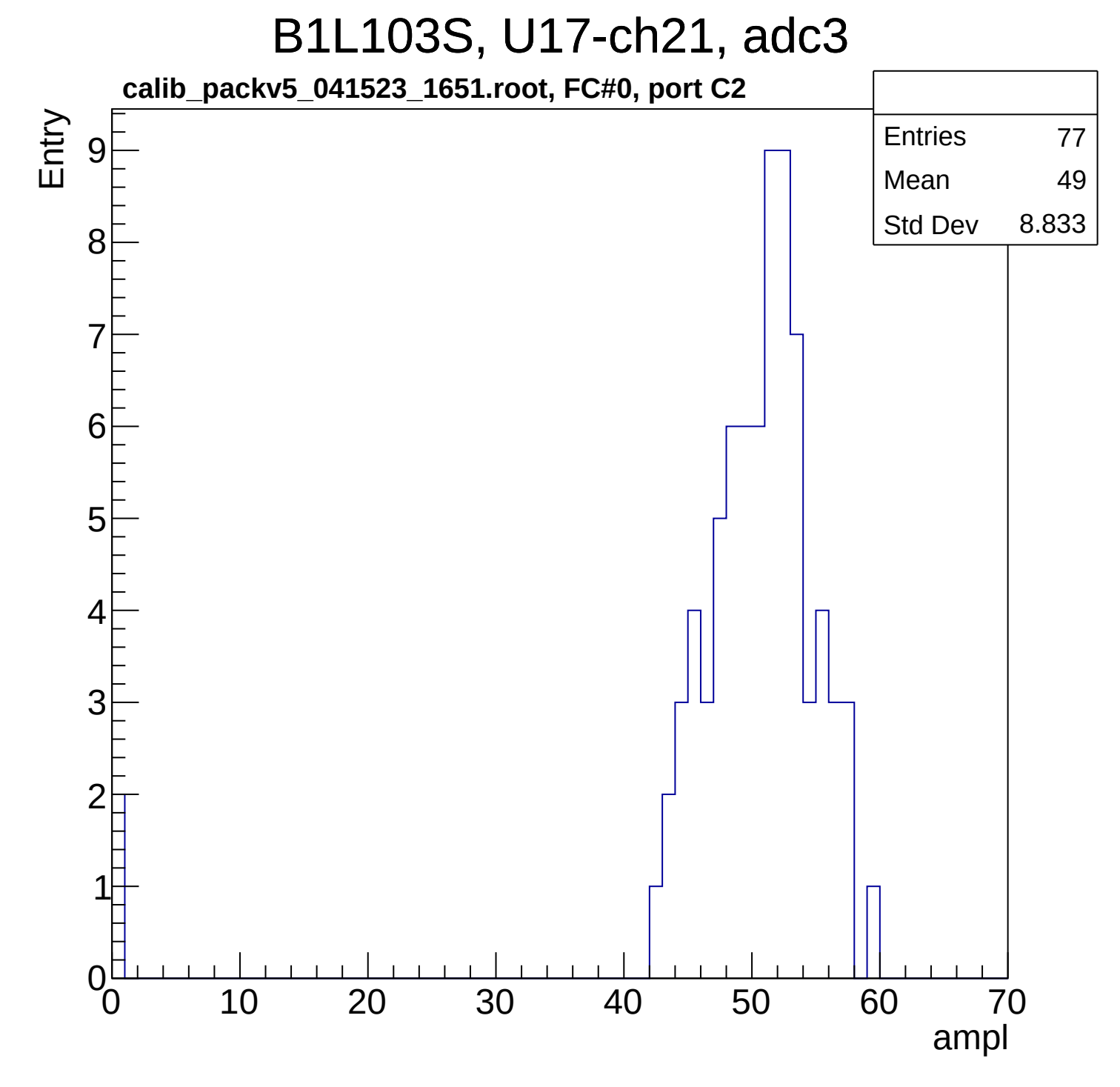
B1L103S, U17-ch21, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 49
Std Dev 8.833
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
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40
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60
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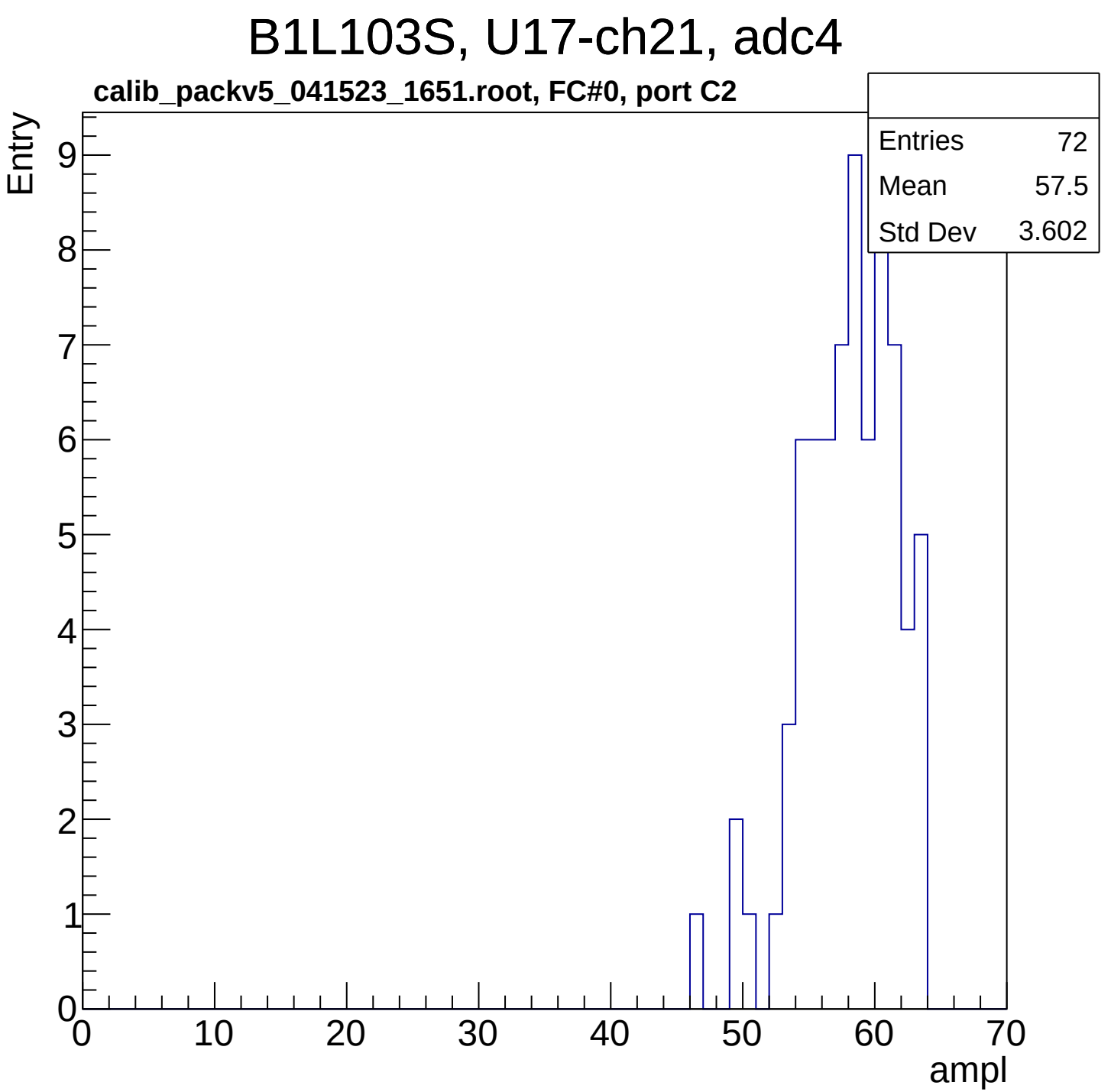
B1L103S, U17-ch21, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 57.5
Std Dev 3.602
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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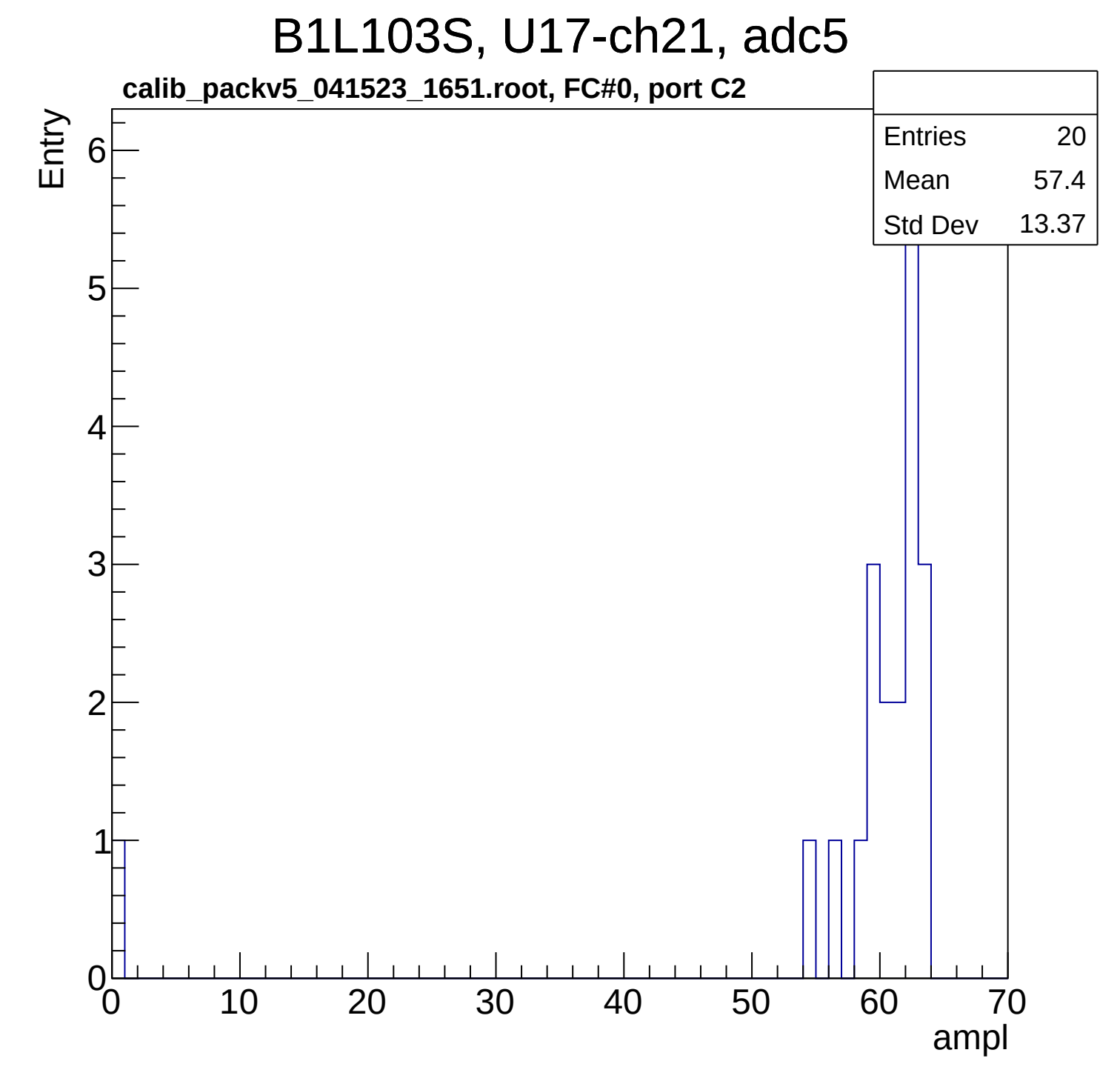
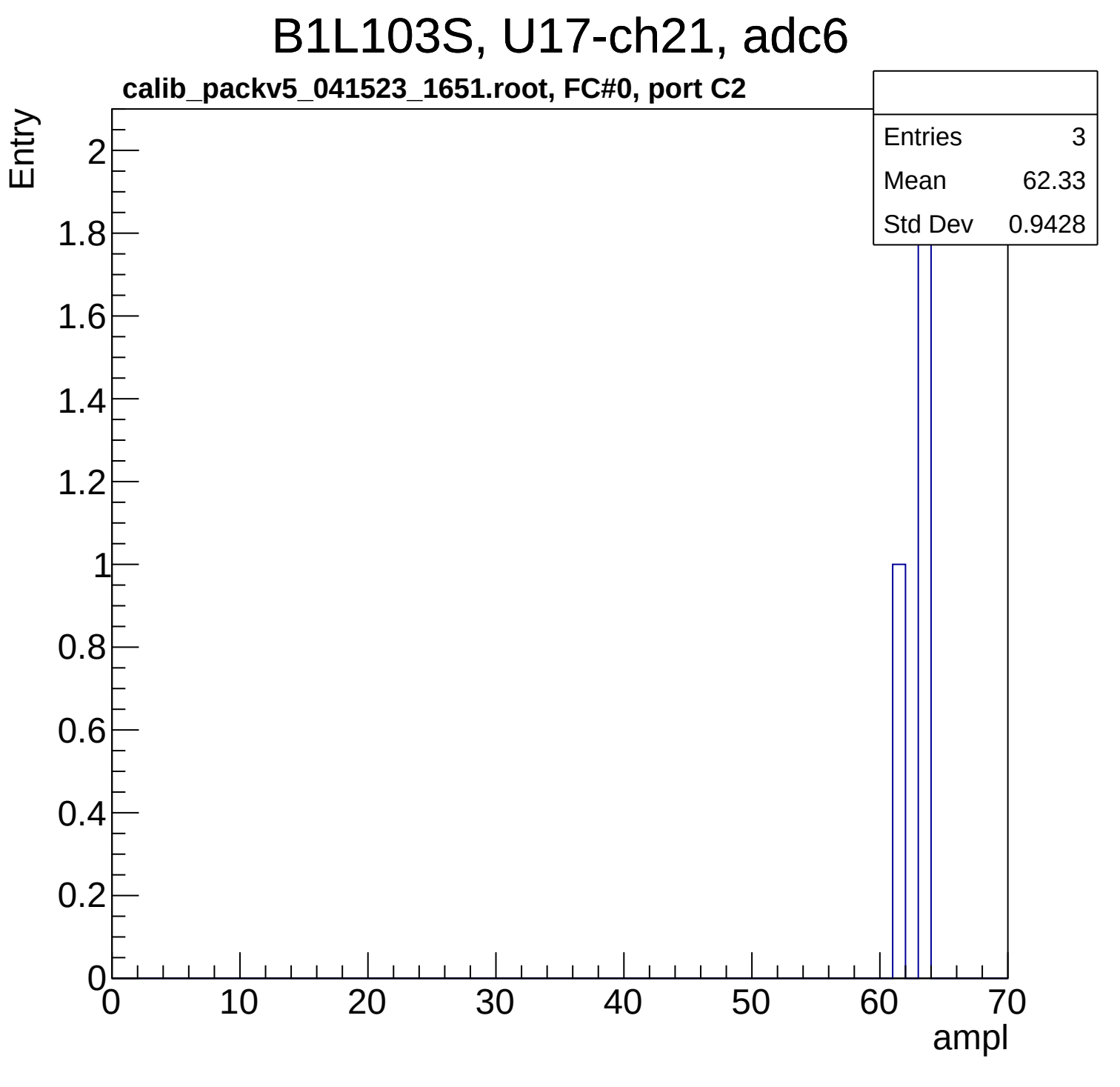
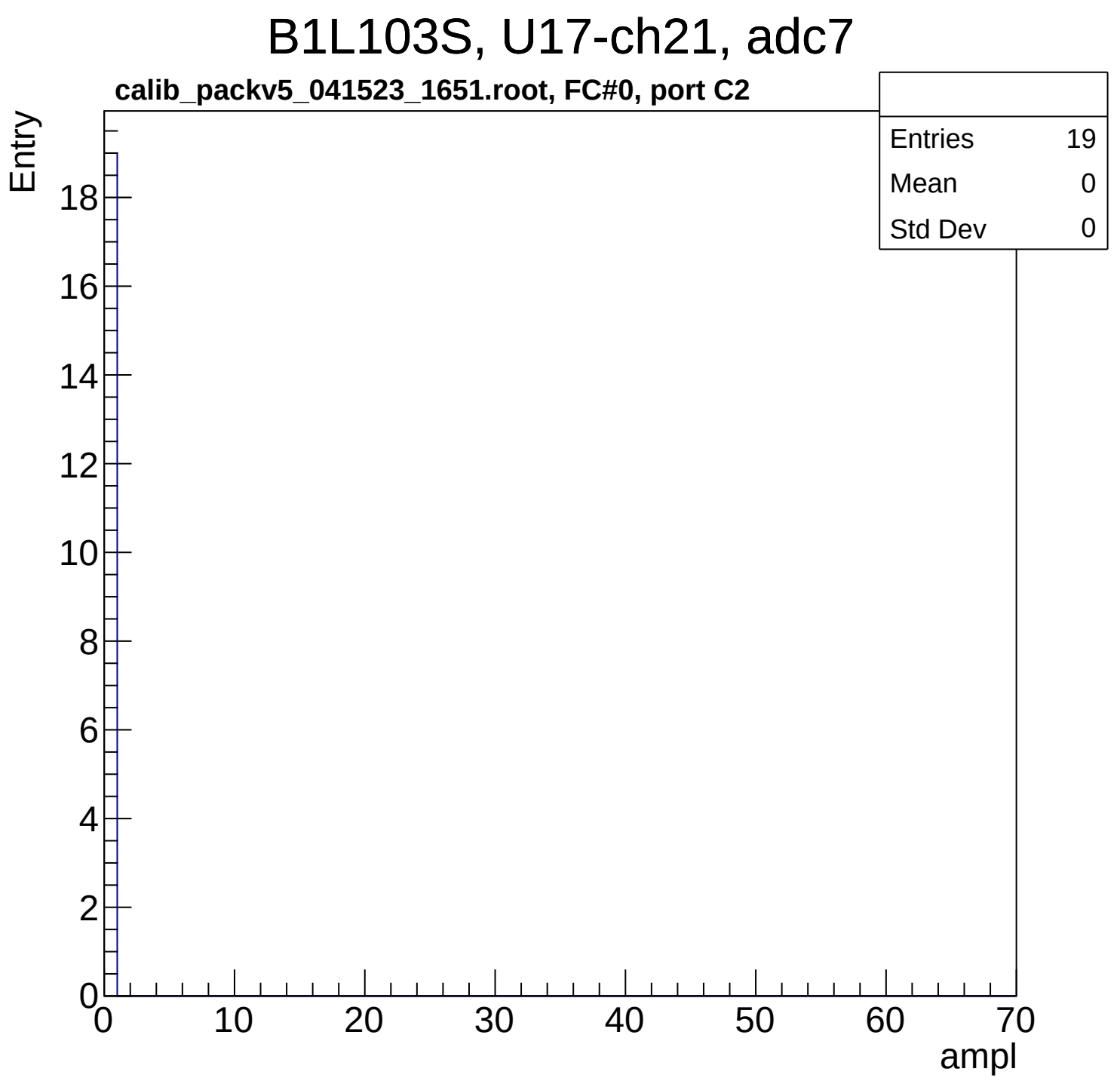
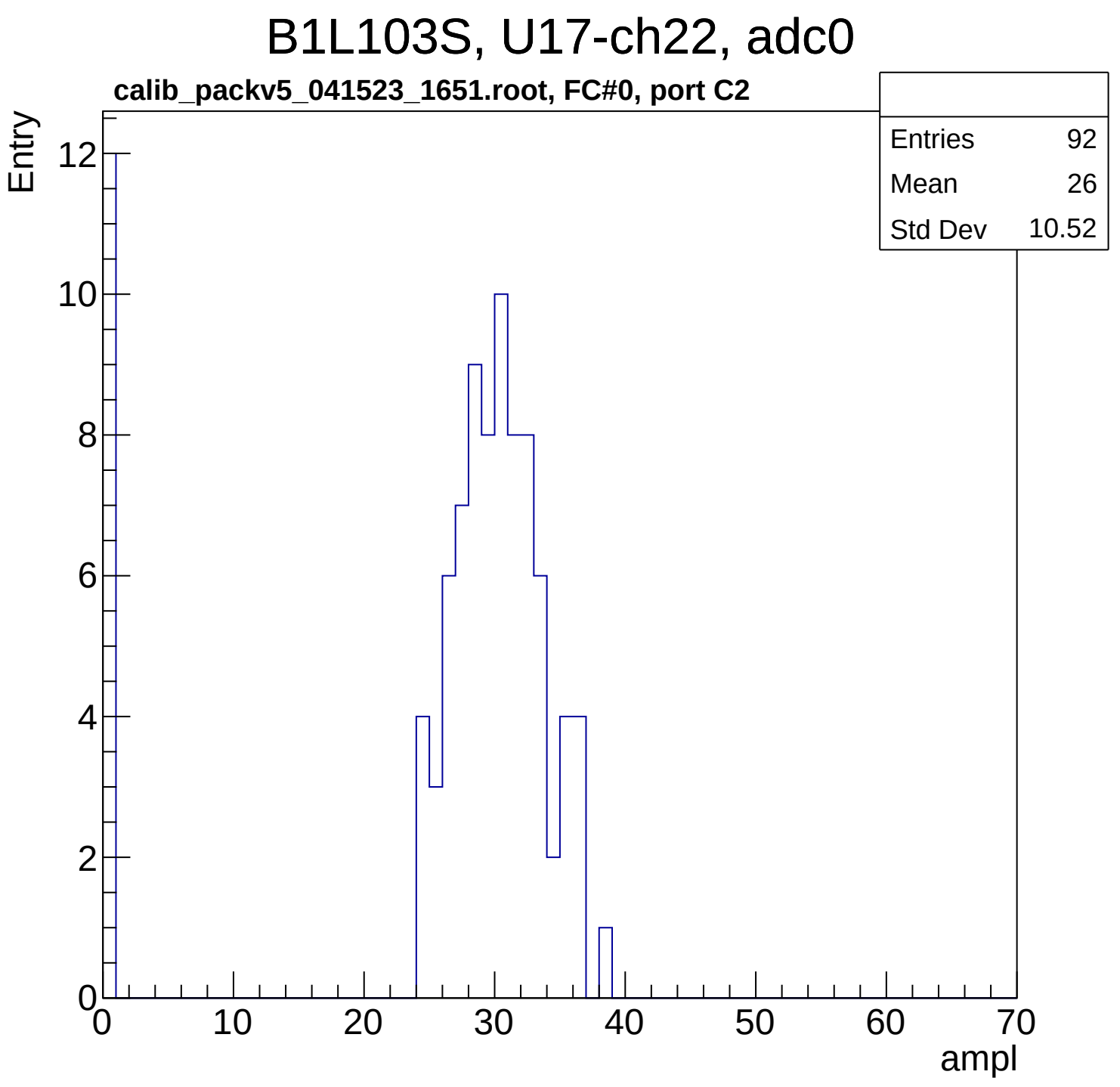
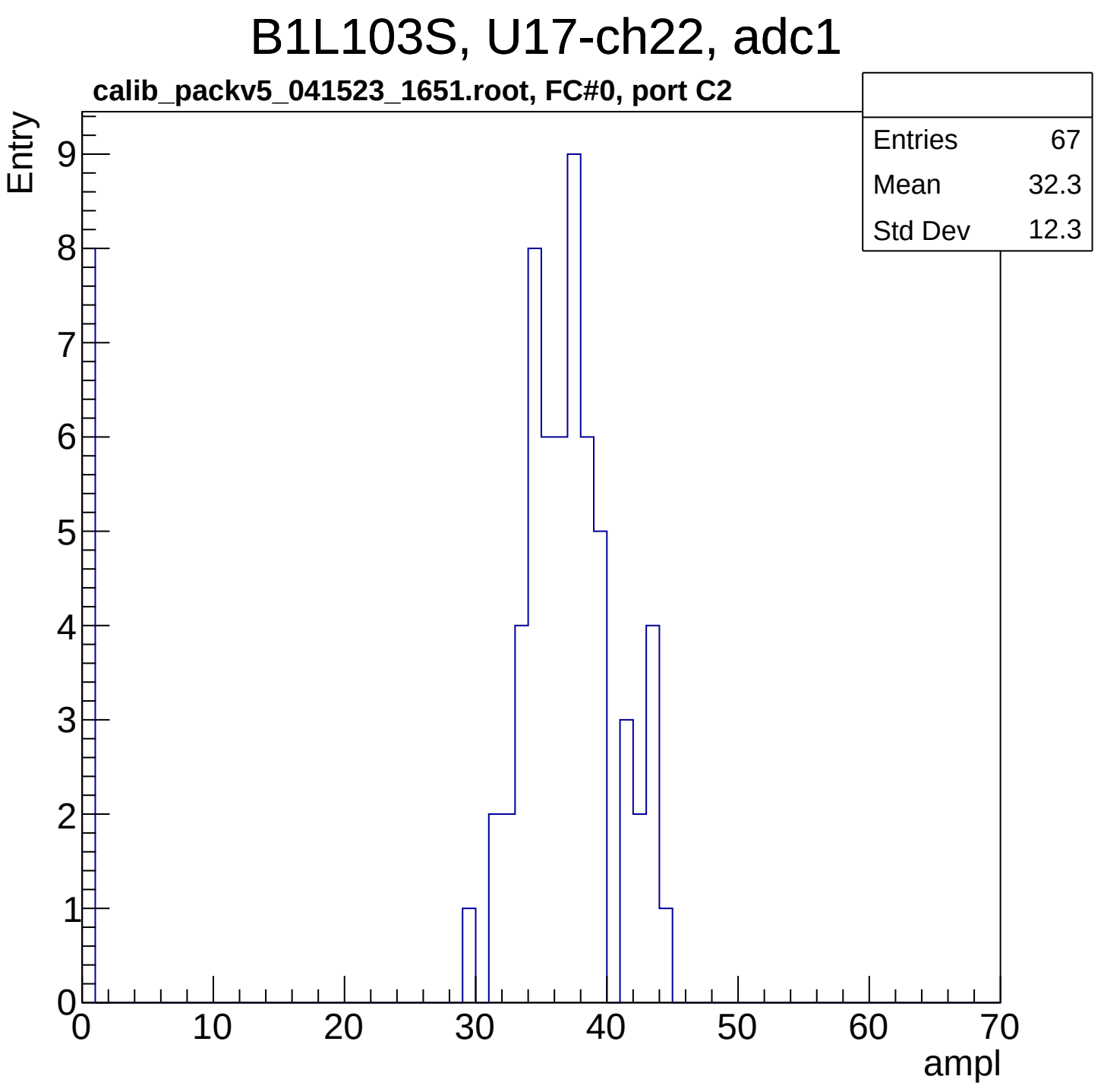

B1L103S, U17-ch21, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 57.4
Std Dev 13.37
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch21, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 3
Mean 62.33
Std Dev 0.9428
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U17-ch21, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch22, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 92
Mean 26
Std Dev 10.52
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch22, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 32.3
Std Dev 12.3
Entry
ampl
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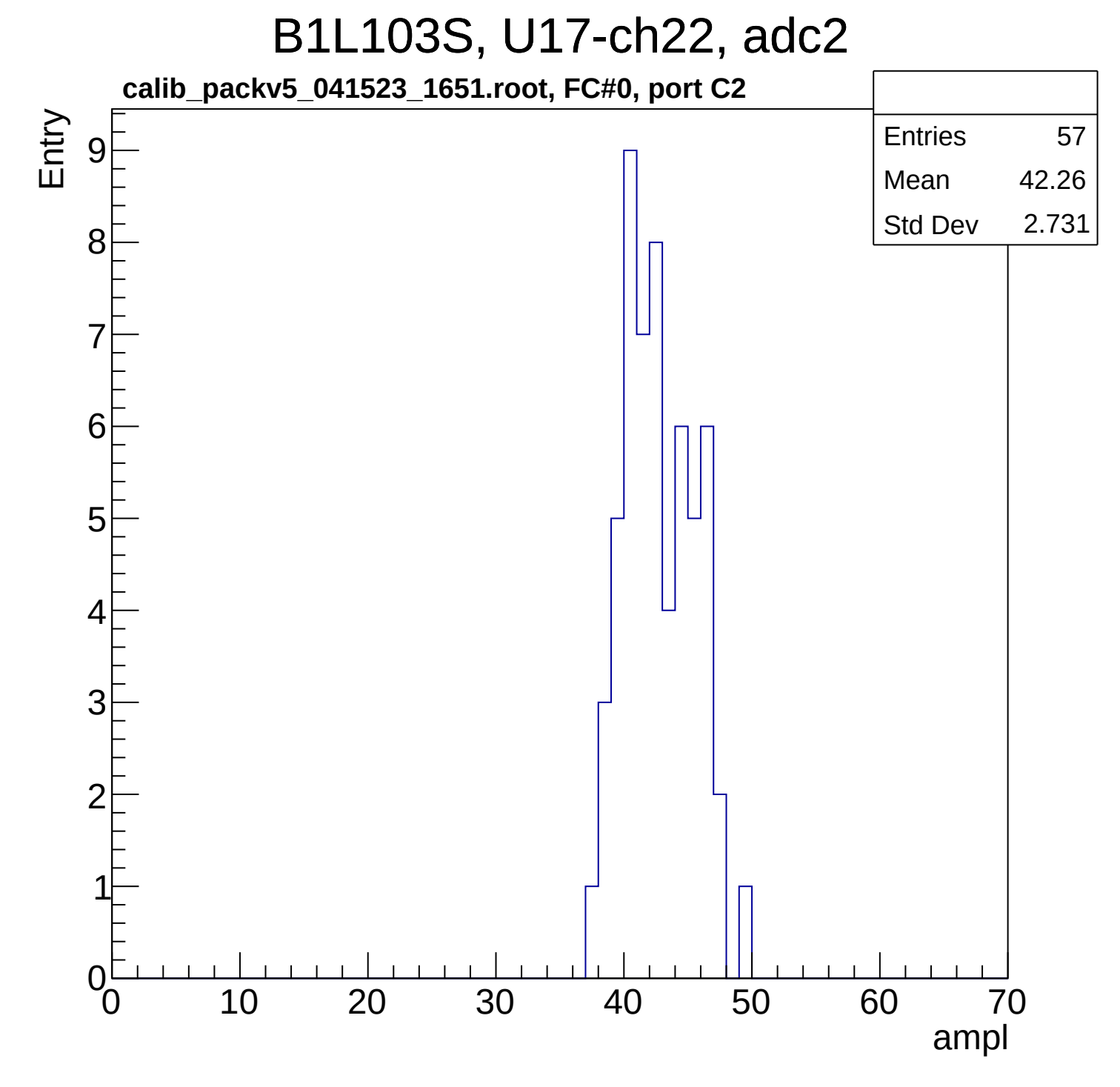
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U17-ch22, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 42.26
Std Dev 2.731
Entry
ampl
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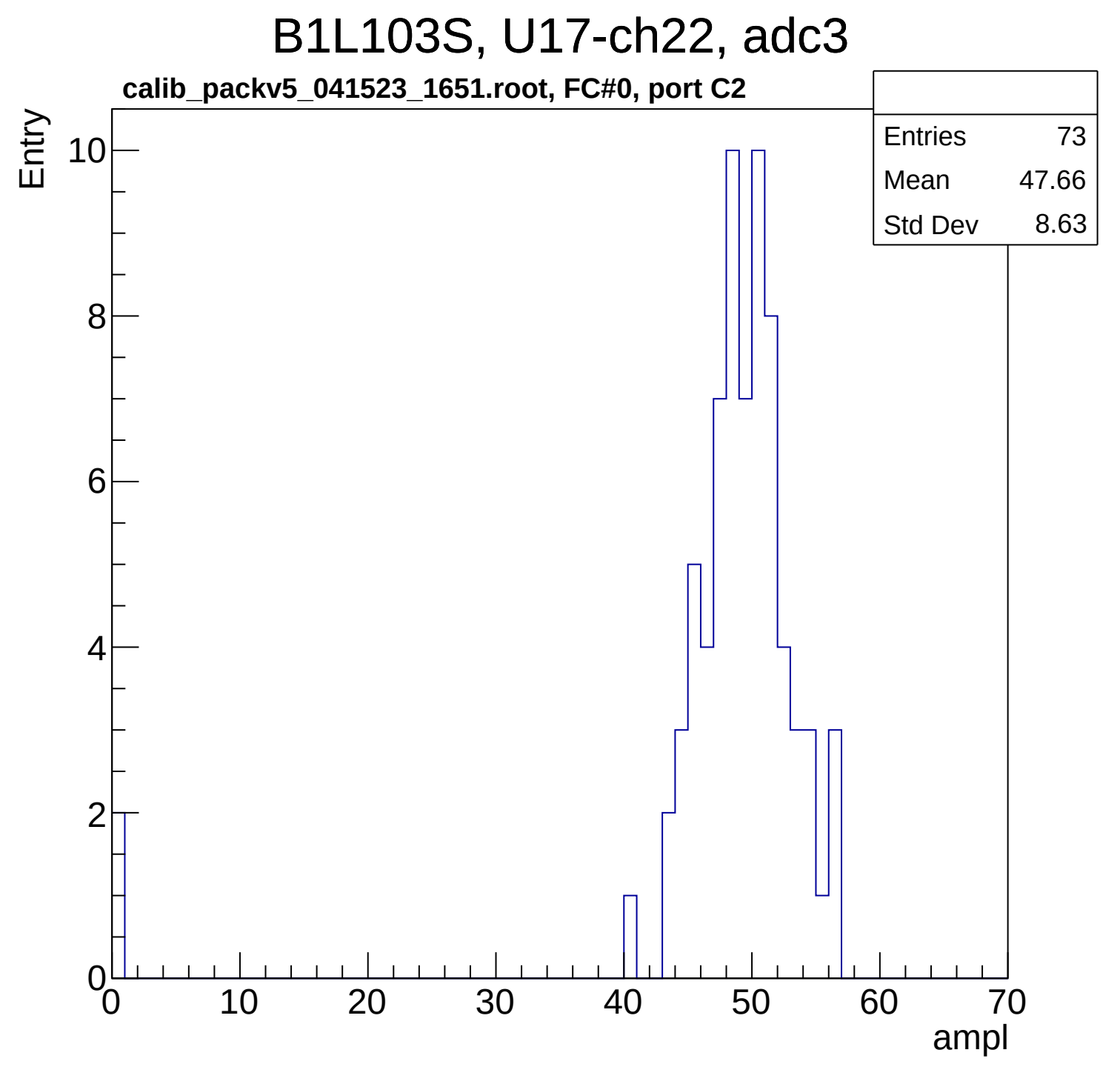
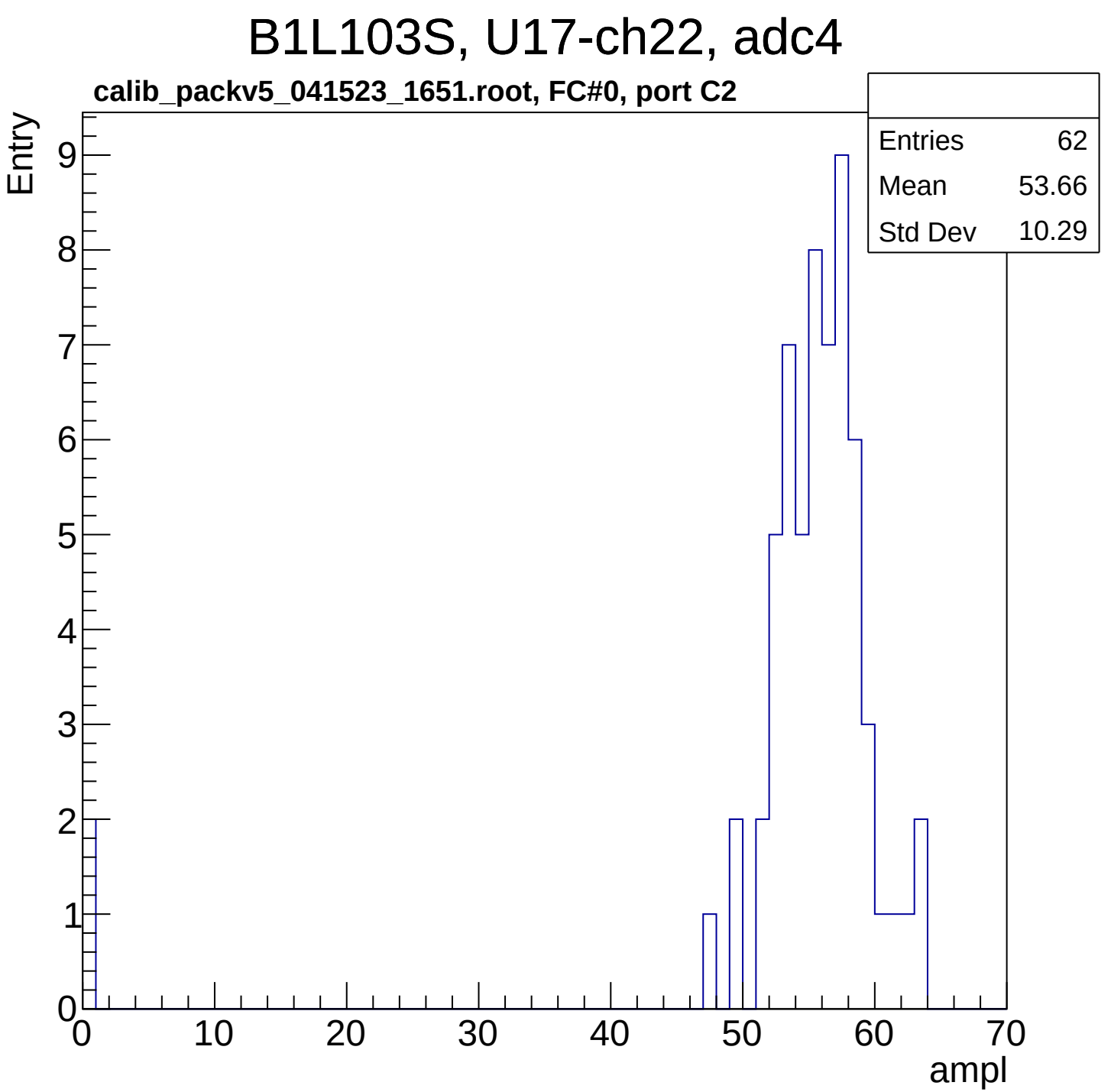
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U17-ch22, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 47.66
Std Dev 8.63
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U17-ch22, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 53.66
Std Dev 10.29
Entry
ampl
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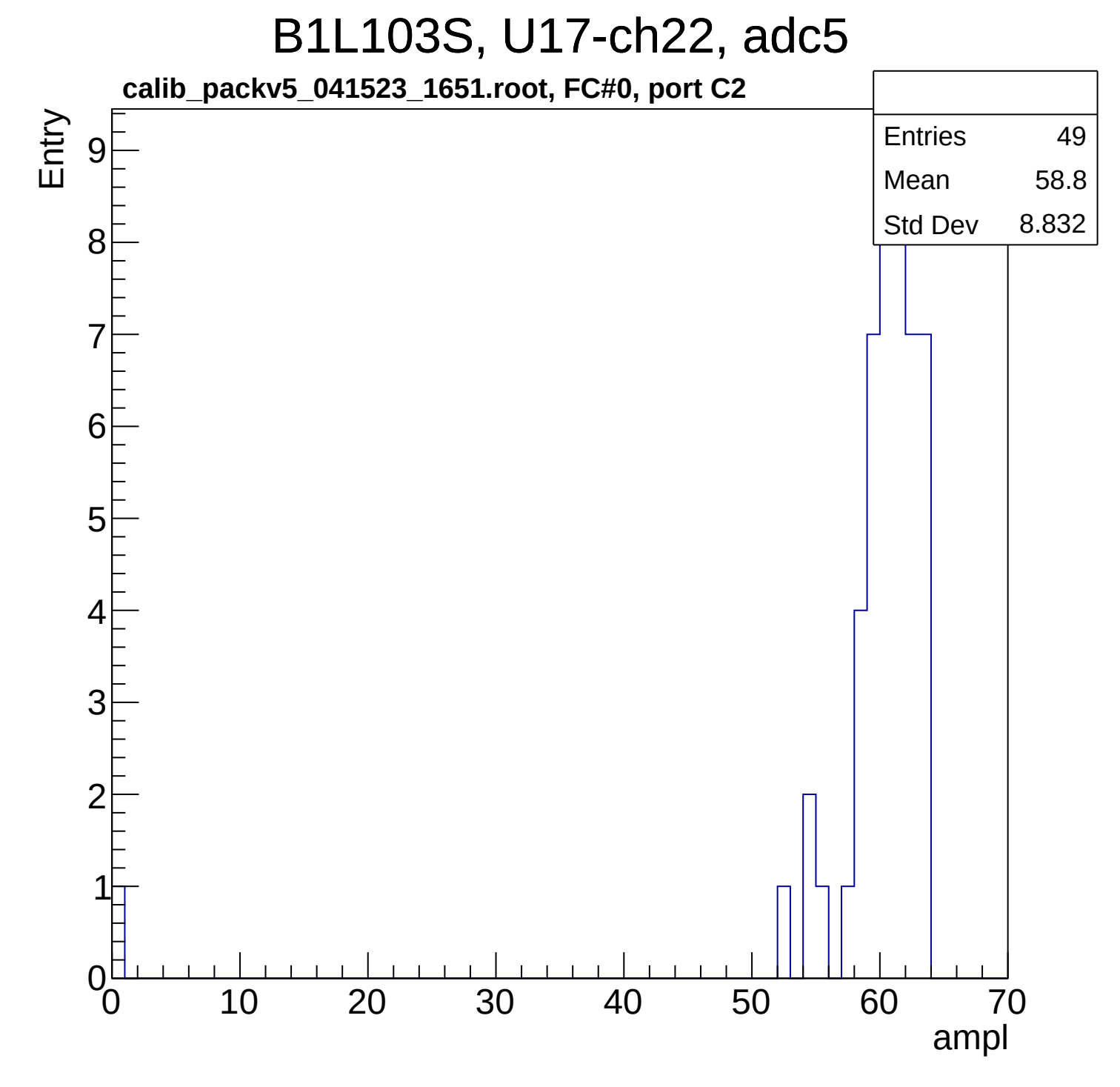
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U17-ch22, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 58.8
Std Dev 8.832
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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40
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60
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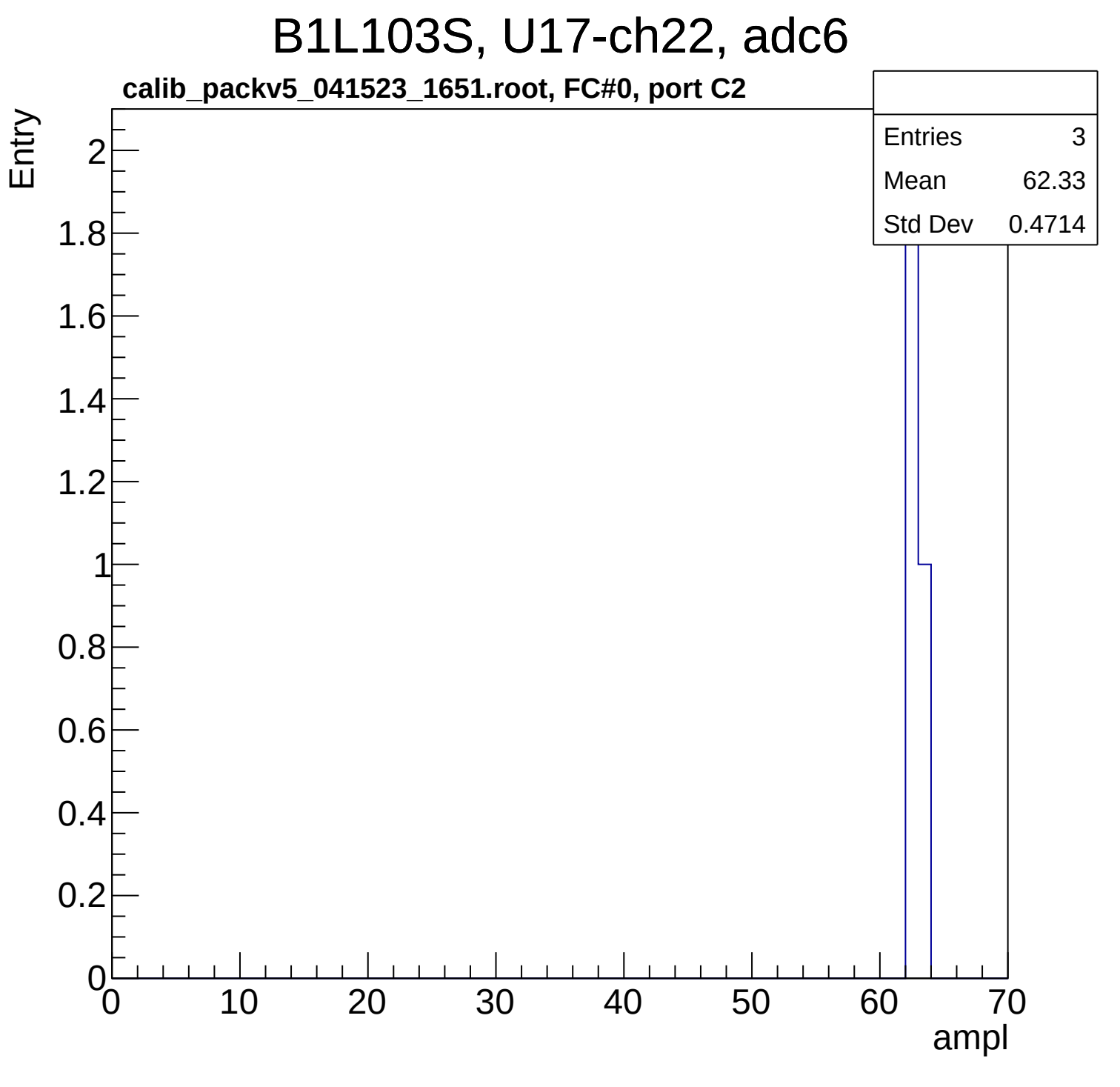
B1L103S, U17-ch22, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 3
Mean 62.33
Std Dev 0.4714
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
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20
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40
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60
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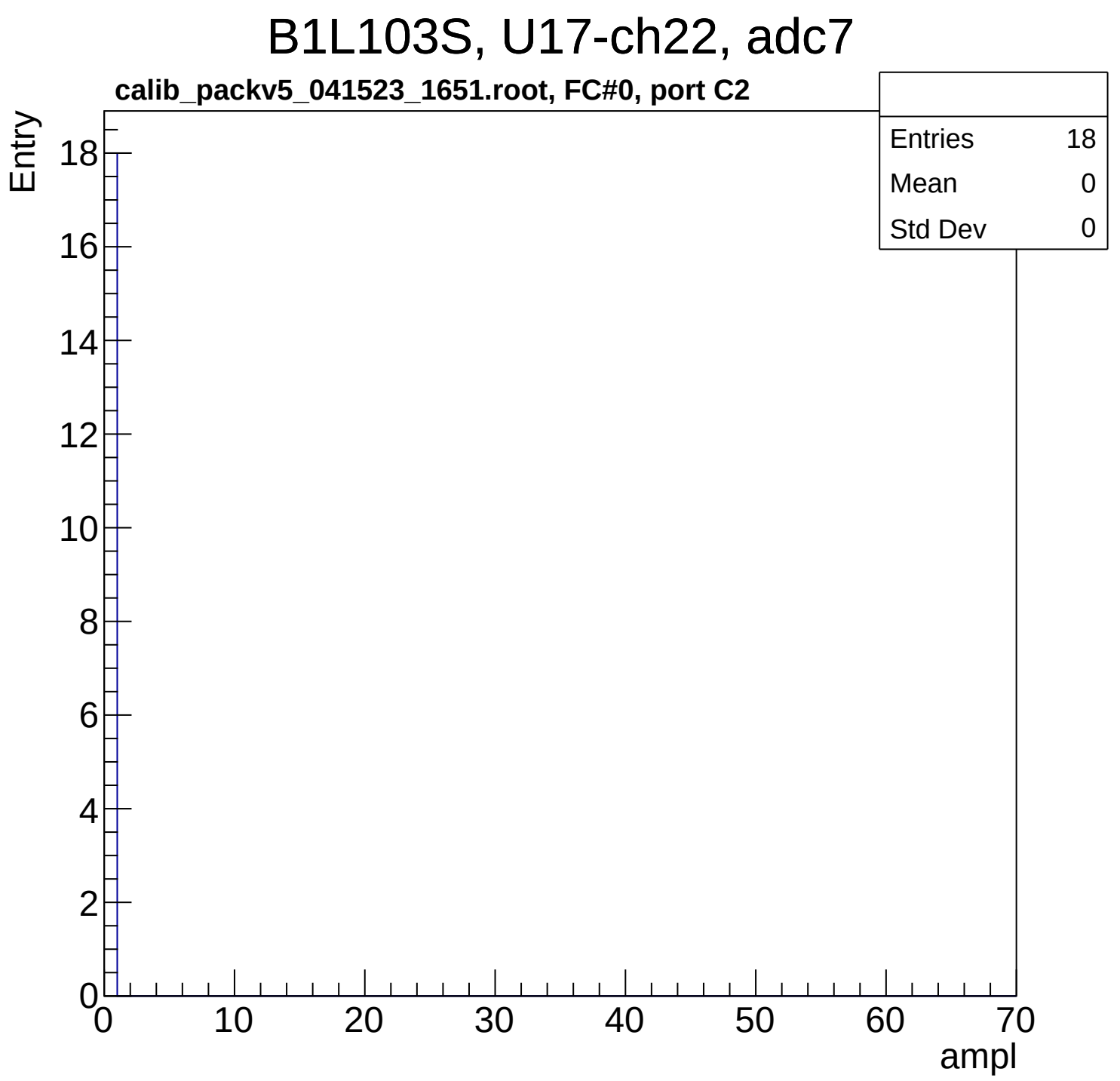
B1L103S, U17-ch22, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
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2
4
6
8
10
12
14
16
18
0
10
20
30
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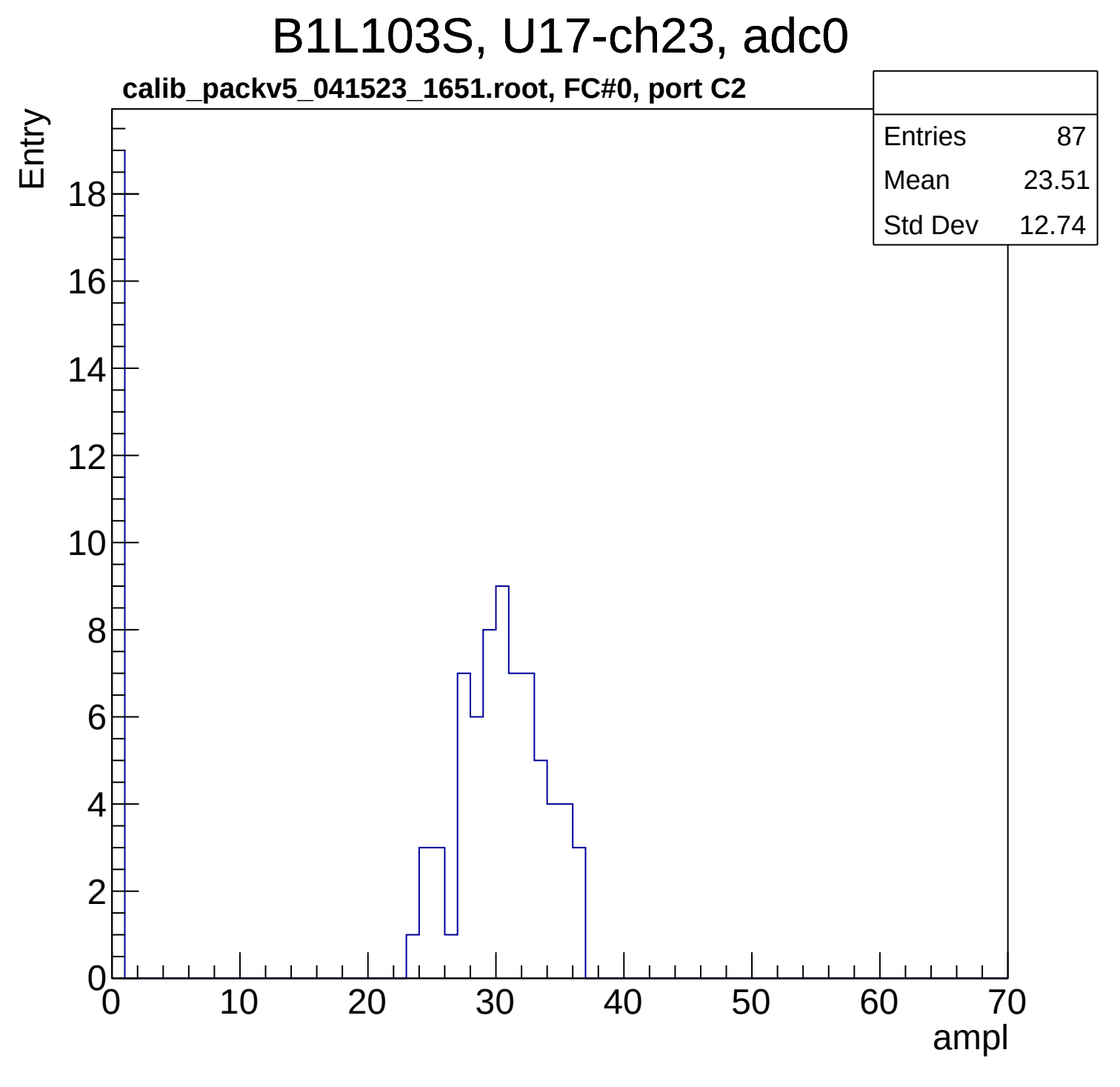
50
60
70
ampl


B1L103S, U17-ch23, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 87
Mean 23.51
Std Dev 12.74
Entry
ampl
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4
6
8
10
12
14
16
18
0
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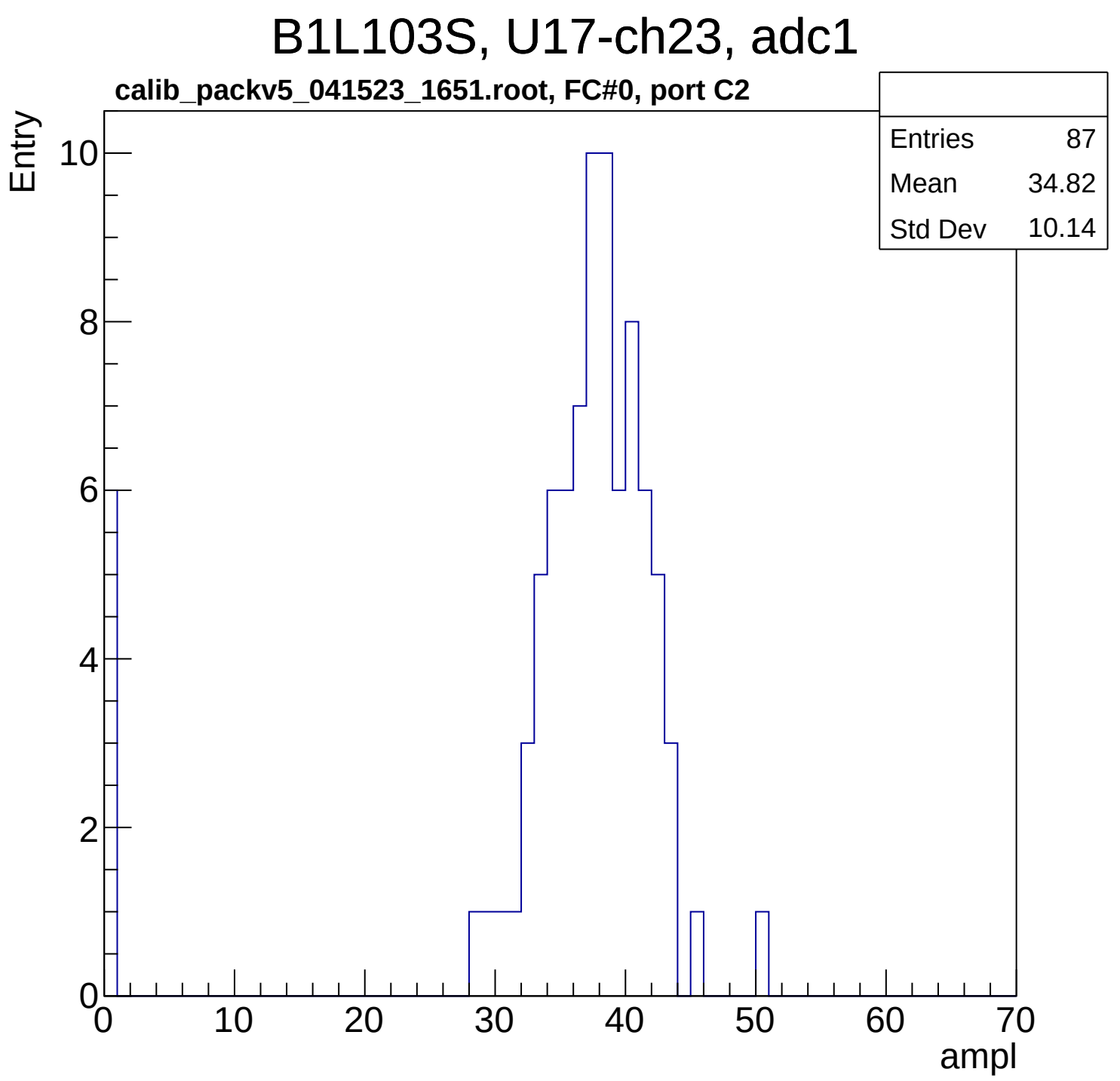
B1L103S, U17-ch23, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 87
Mean 34.82
Std Dev 10.14
Entry
ampl
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6
8
10
0
10
20
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40
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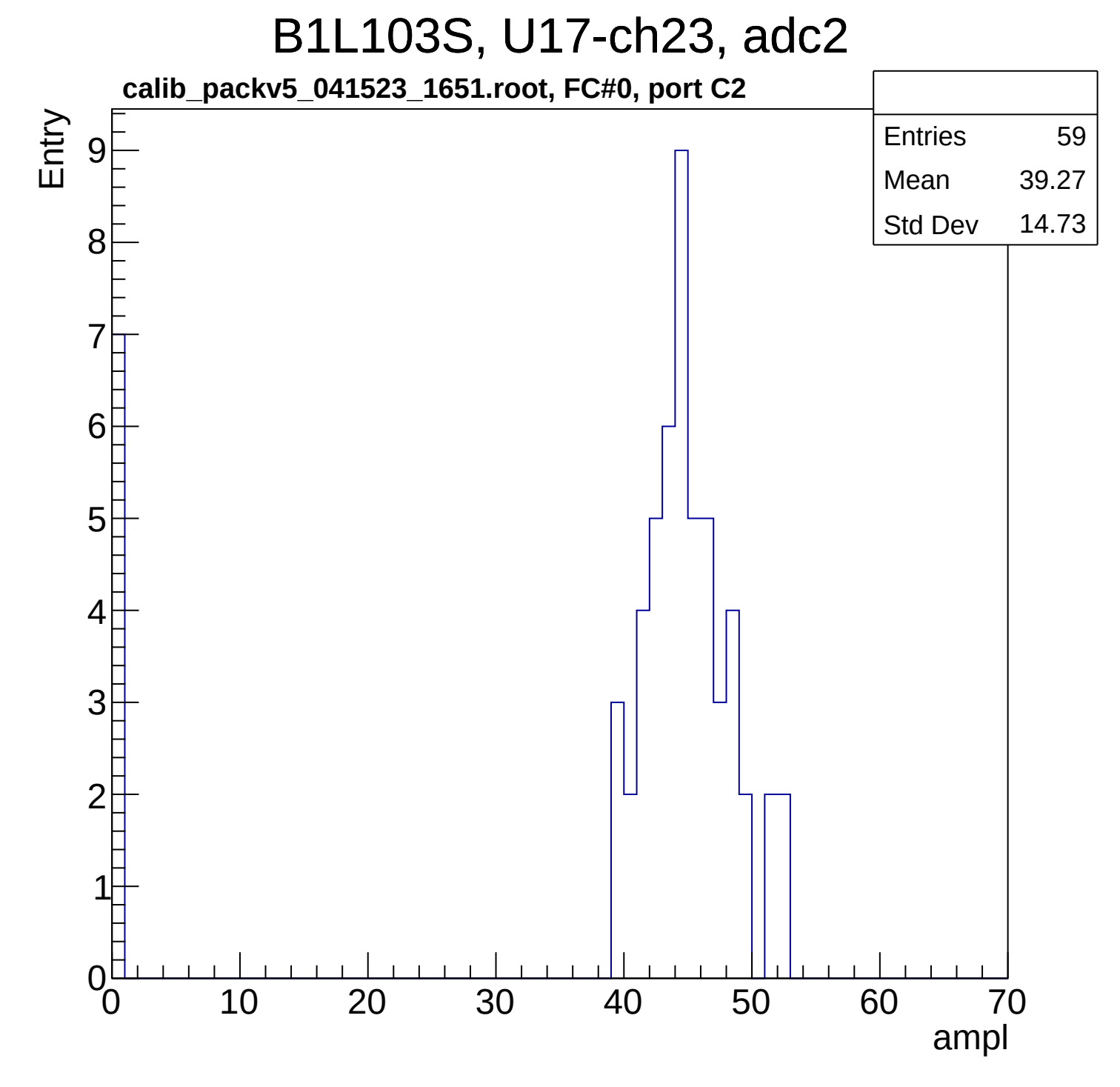
60
70


B1L103S, U17-ch23, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 39.27
Std Dev 14.73
Entry
ampl
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2
3
4
5
6
7
8
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0
10
20
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40
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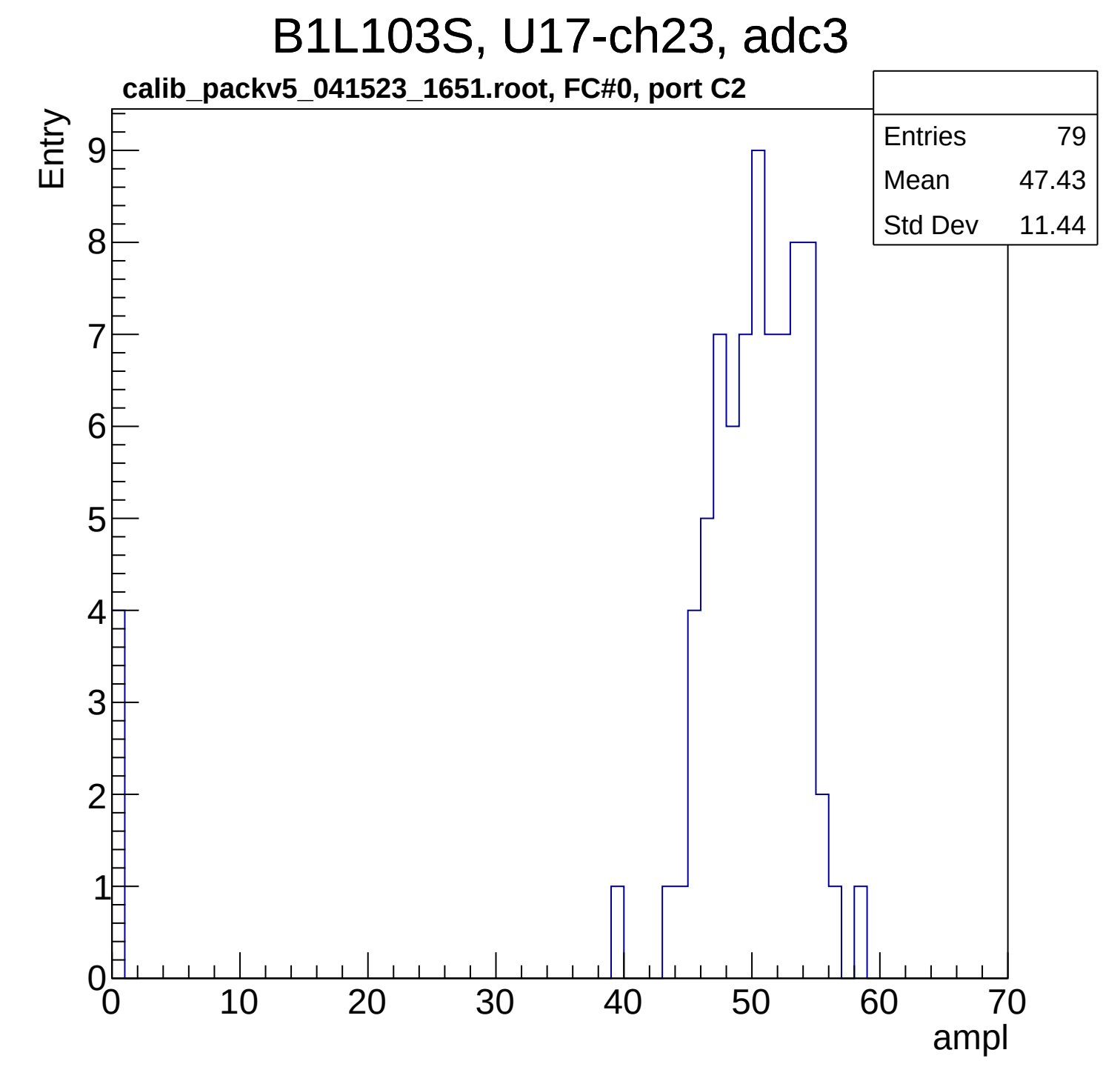
B1L103S, U17-ch23, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 47.43
Std Dev 11.44
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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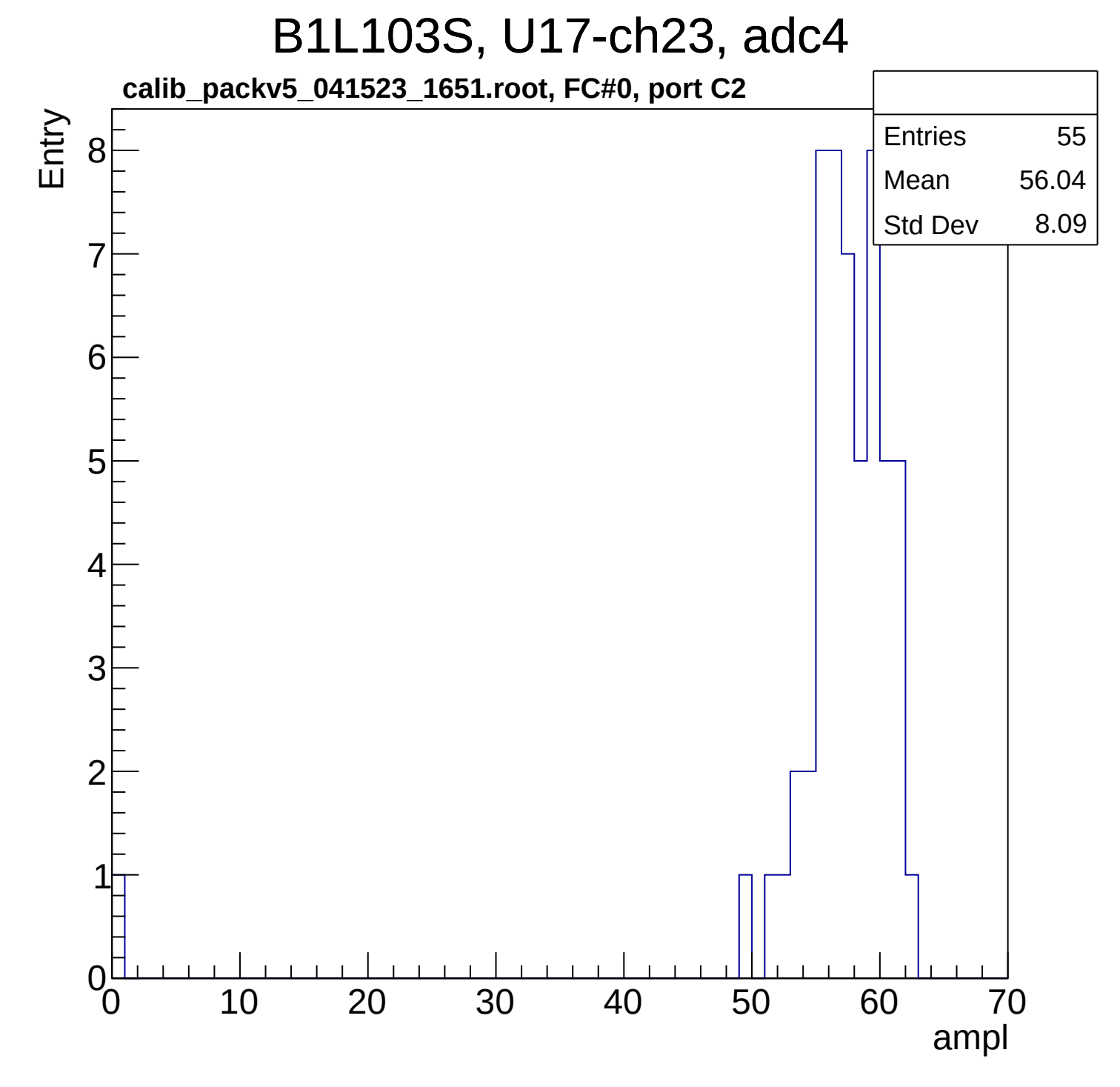
B1L103S, U17-ch23, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 56.04
Std Dev 8.09
Entry
ampl
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1
2
3
4
5
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7
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0
10
20
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40
50
60
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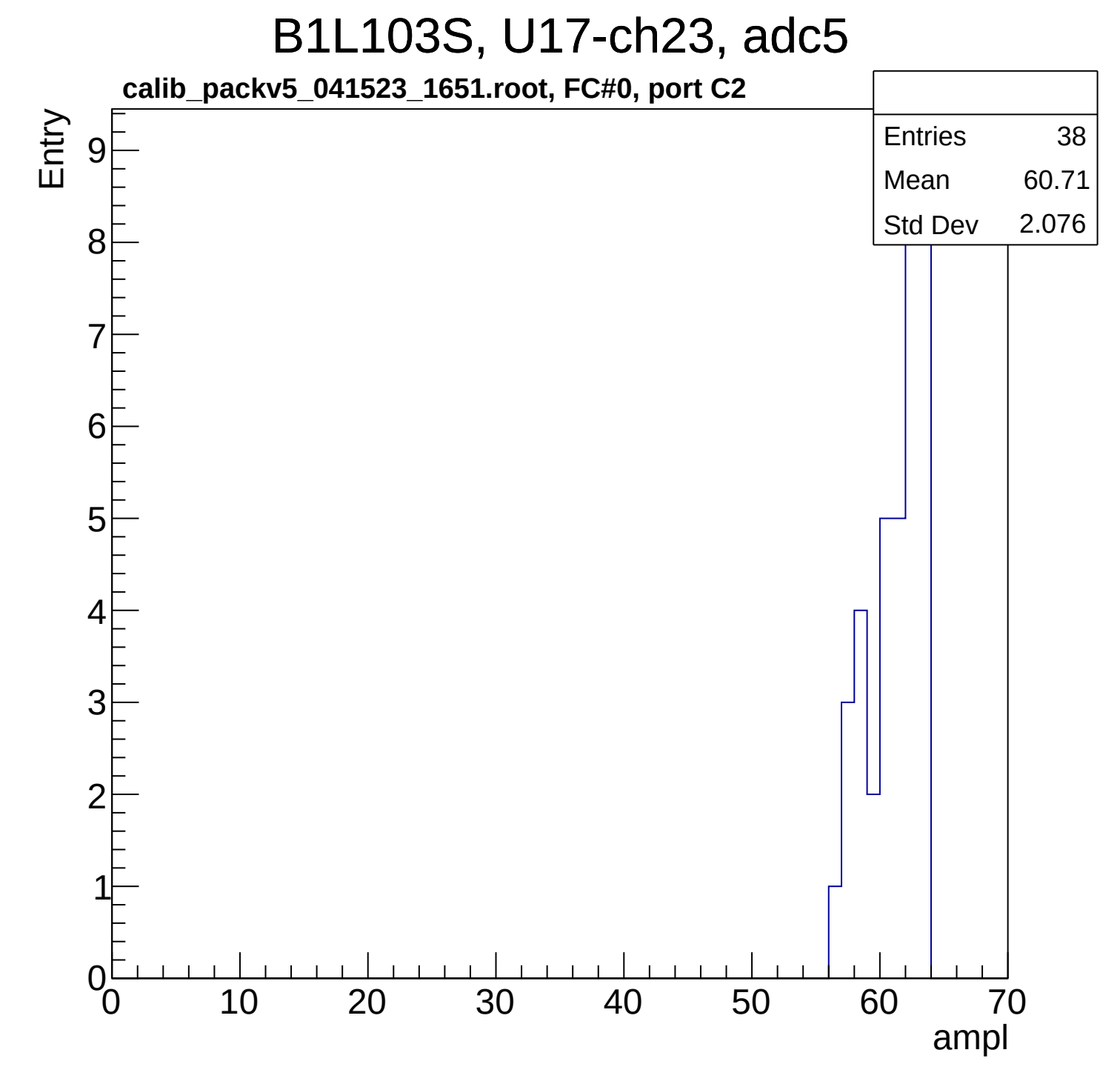
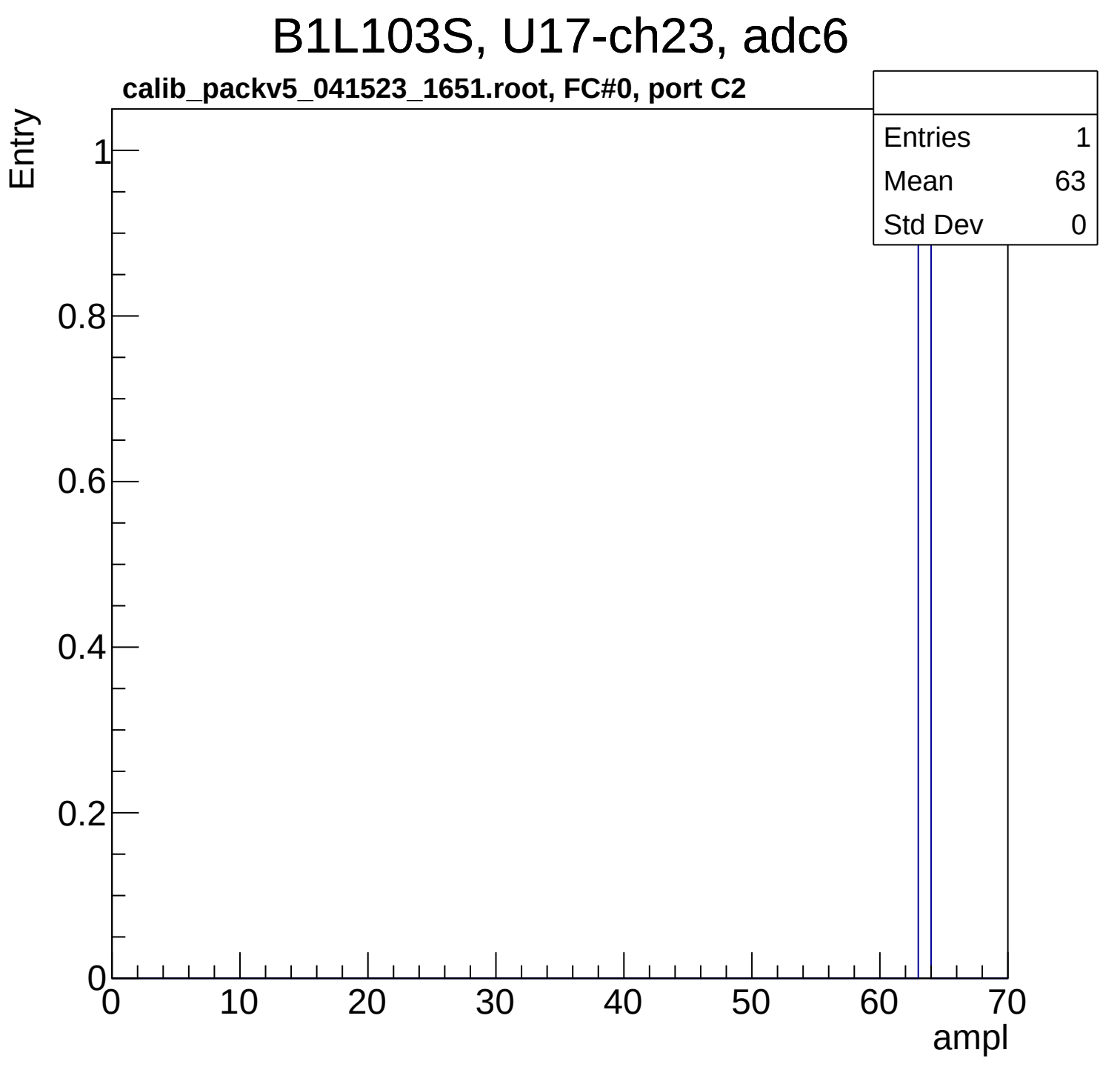

B1L103S, U17-ch23, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 38
Mean 60.71
Std Dev 2.076
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U17-ch23, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 1
Mean 63
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
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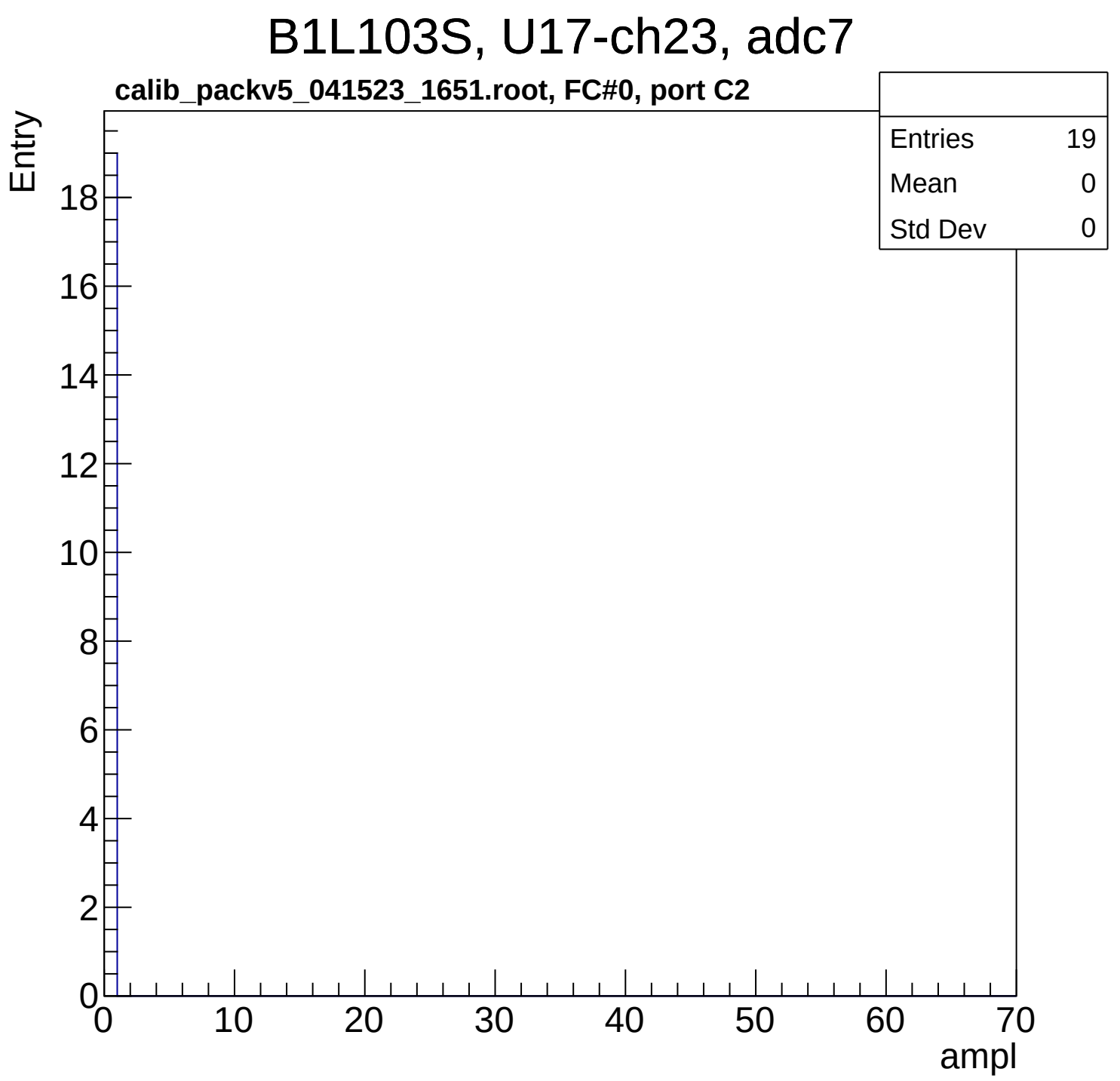
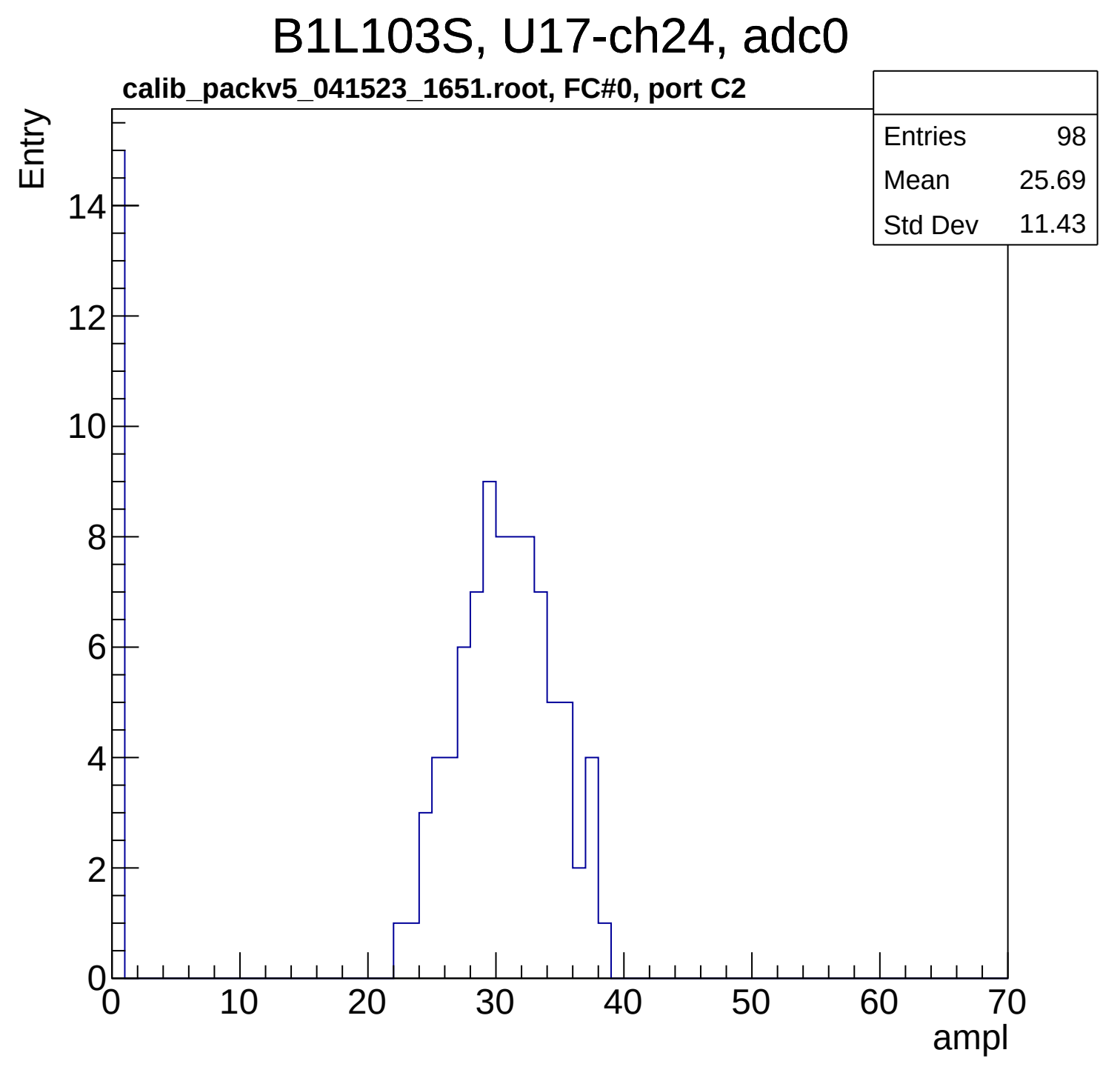
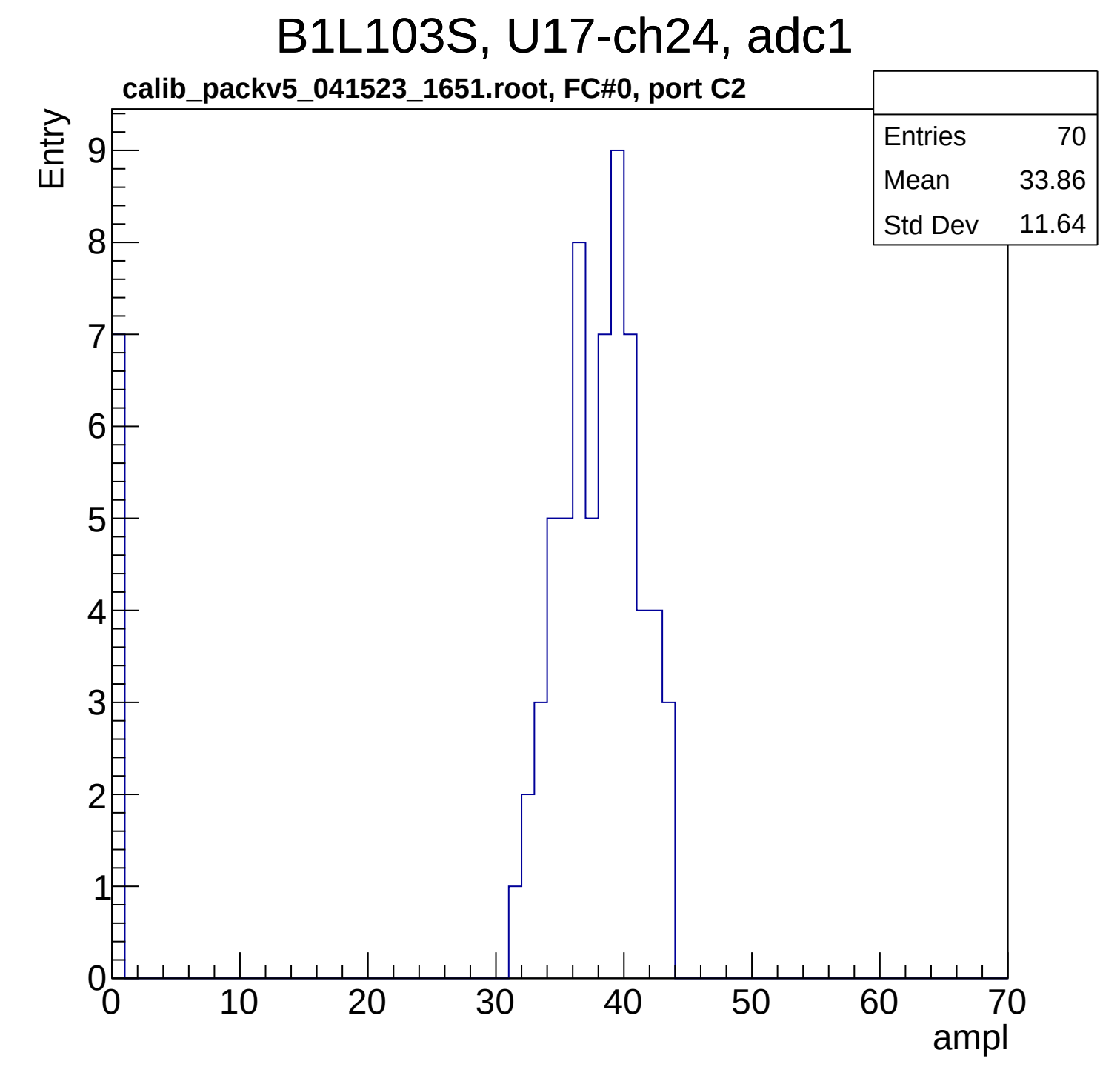
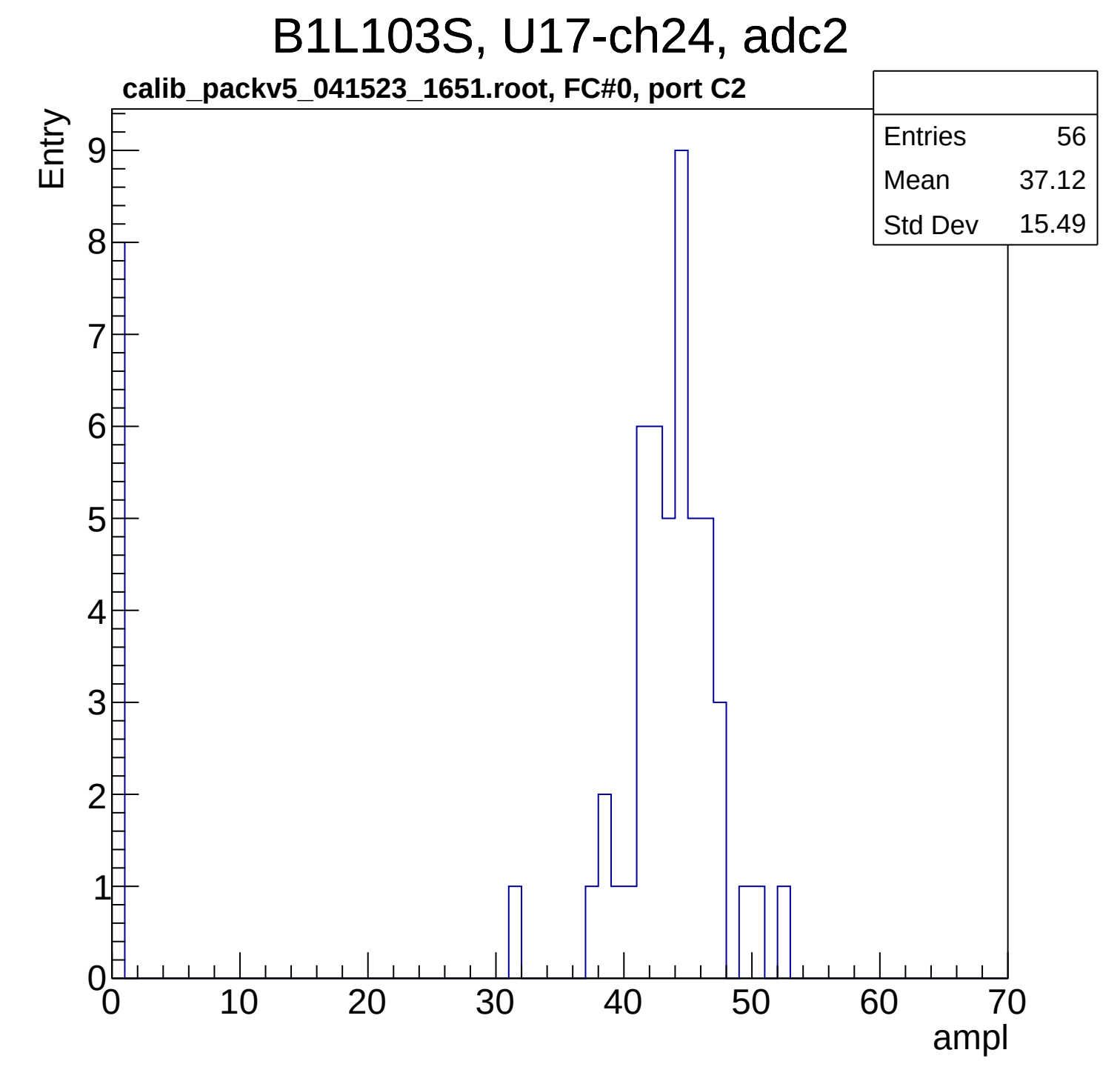
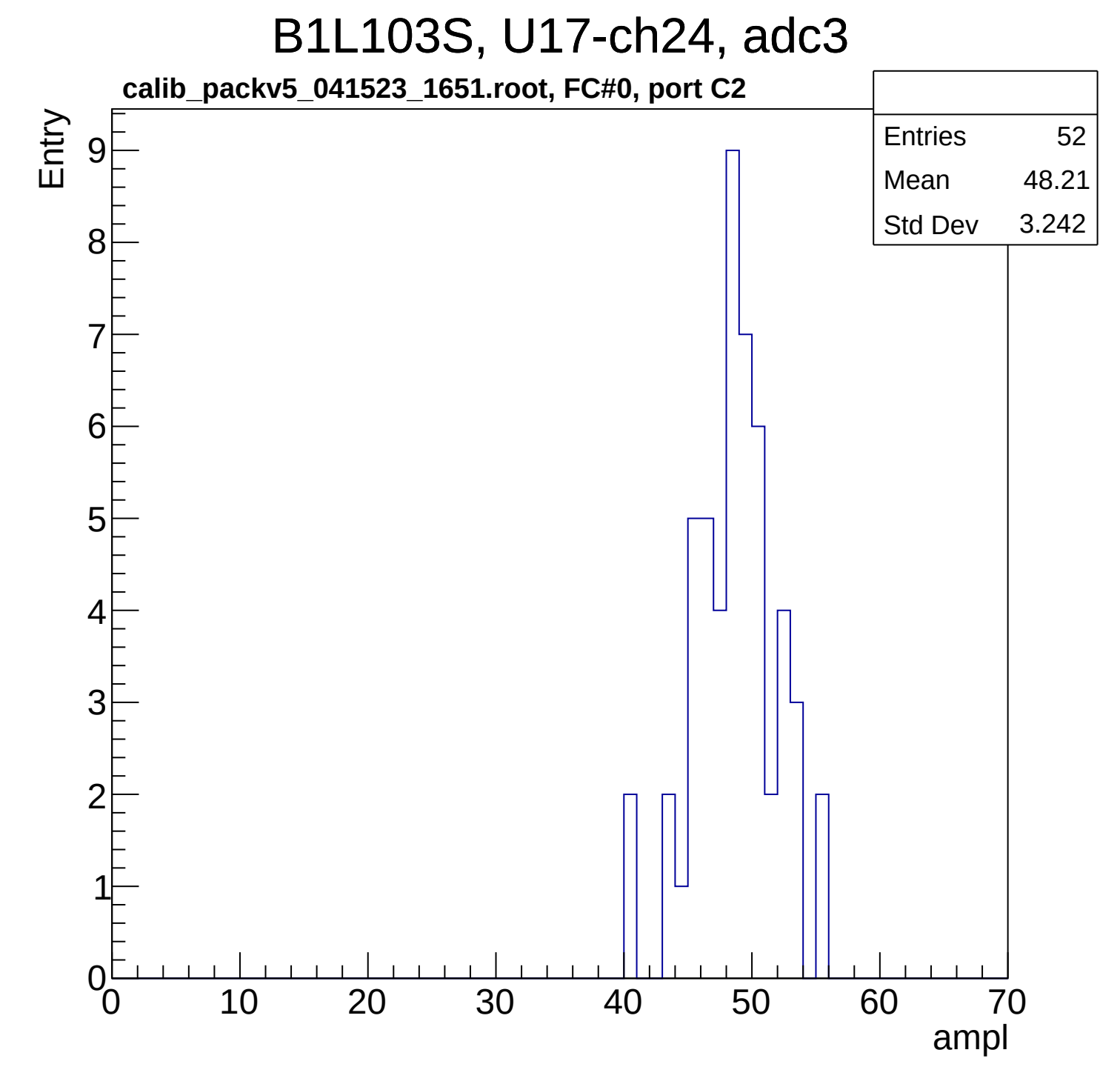
50
60
70
ampl


B1L103S, U17-ch23, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch24, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 98
Mean 25.69
Std Dev 11.43
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch24, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 33.86
Std Dev 11.64
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U17-ch24, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 37.12
Std Dev 15.49
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U17-ch24, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 48.21
Std Dev 3.242
Entry
ampl
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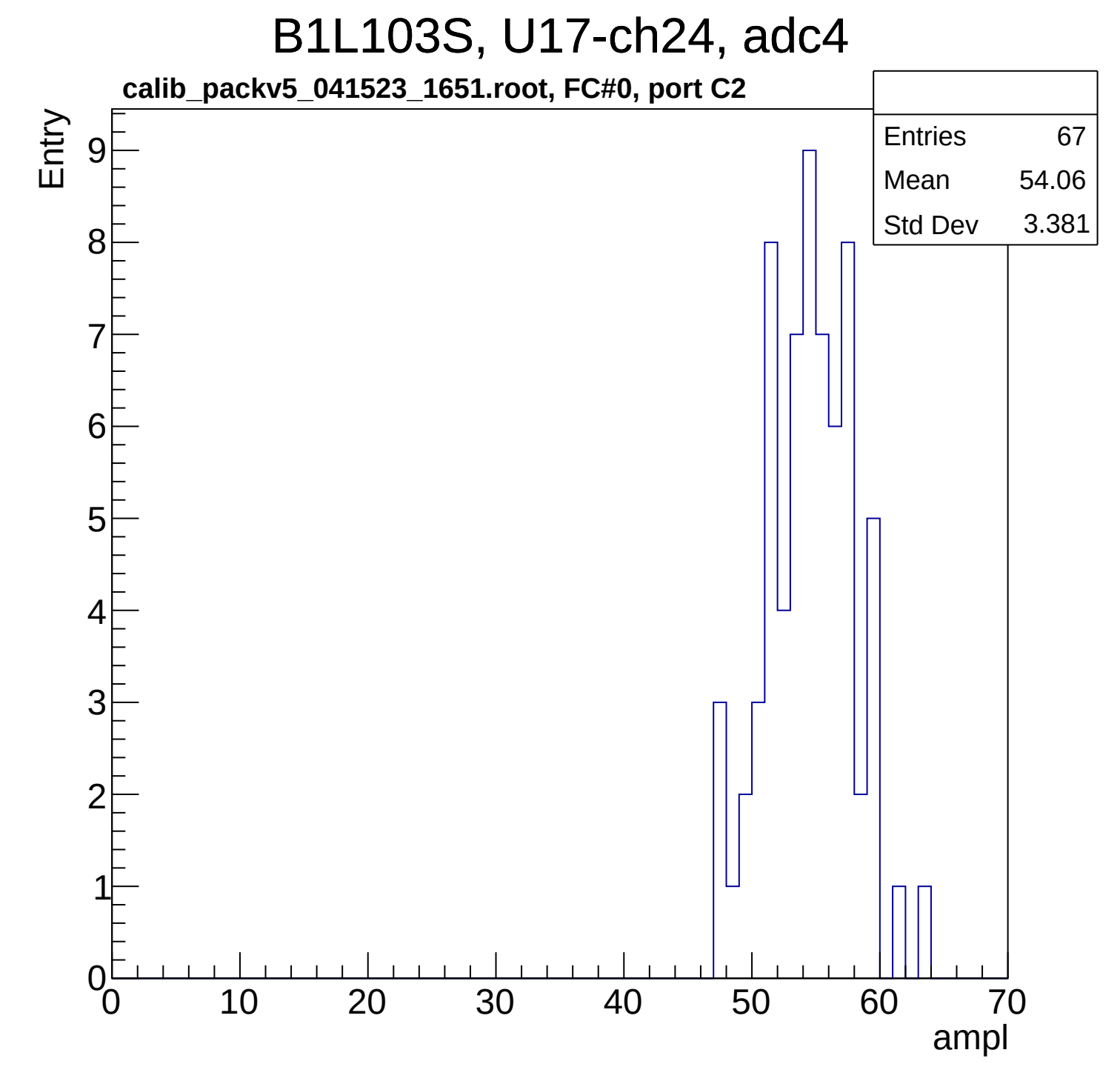
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U17-ch24, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 54.06
Std Dev 3.381
Entry
ampl
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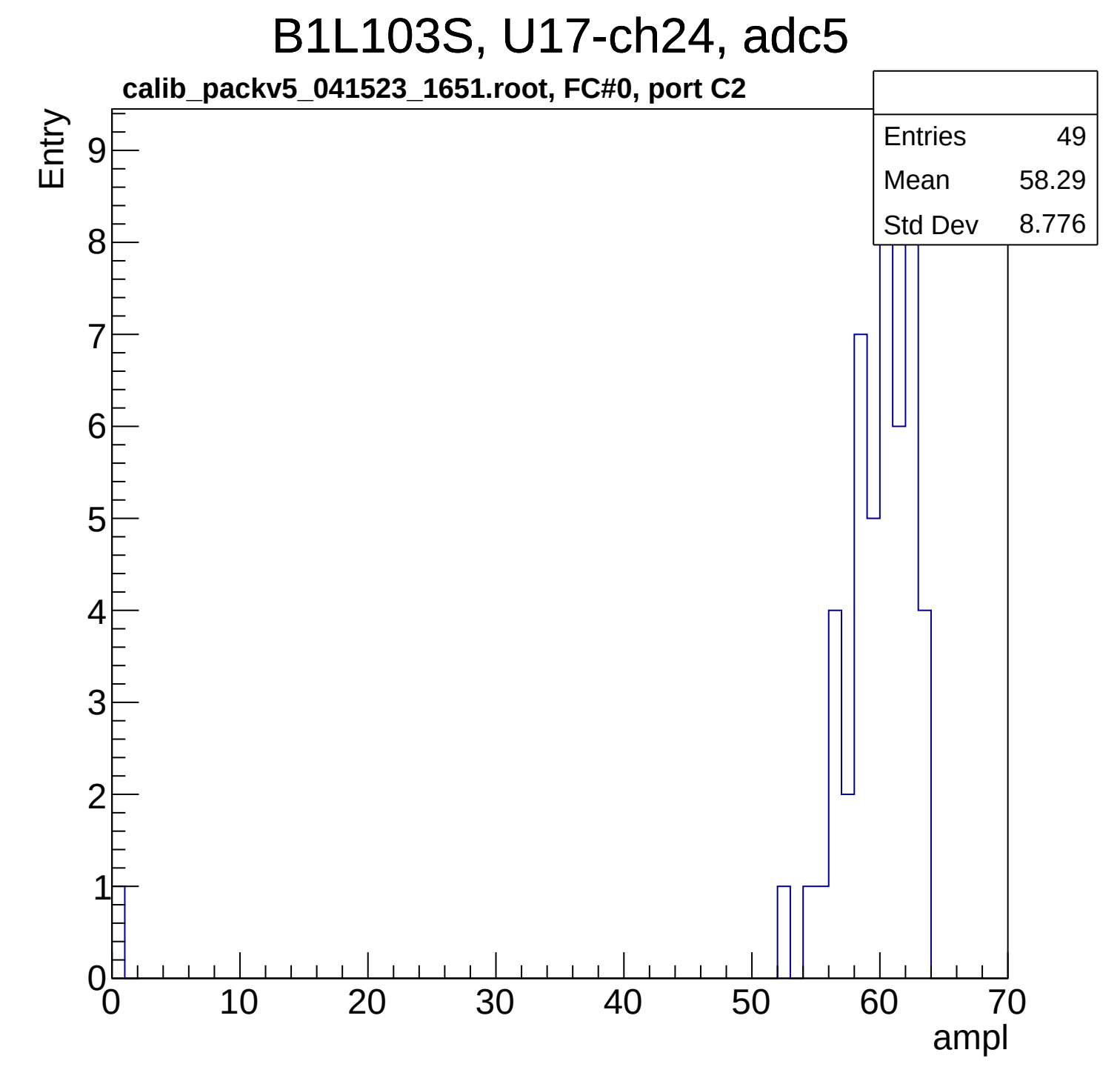
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U17-ch24, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 58.29
Std Dev 8.776
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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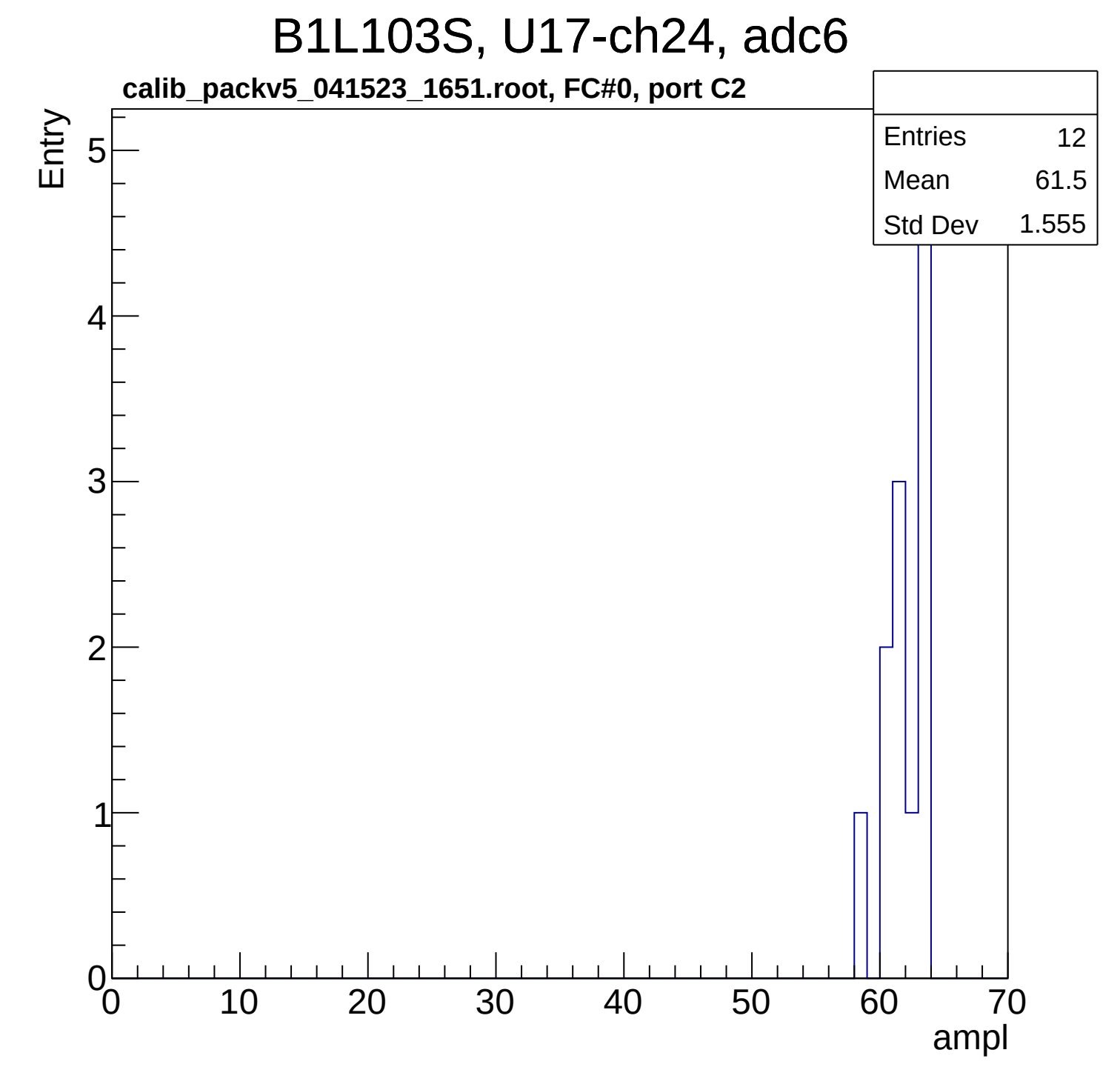
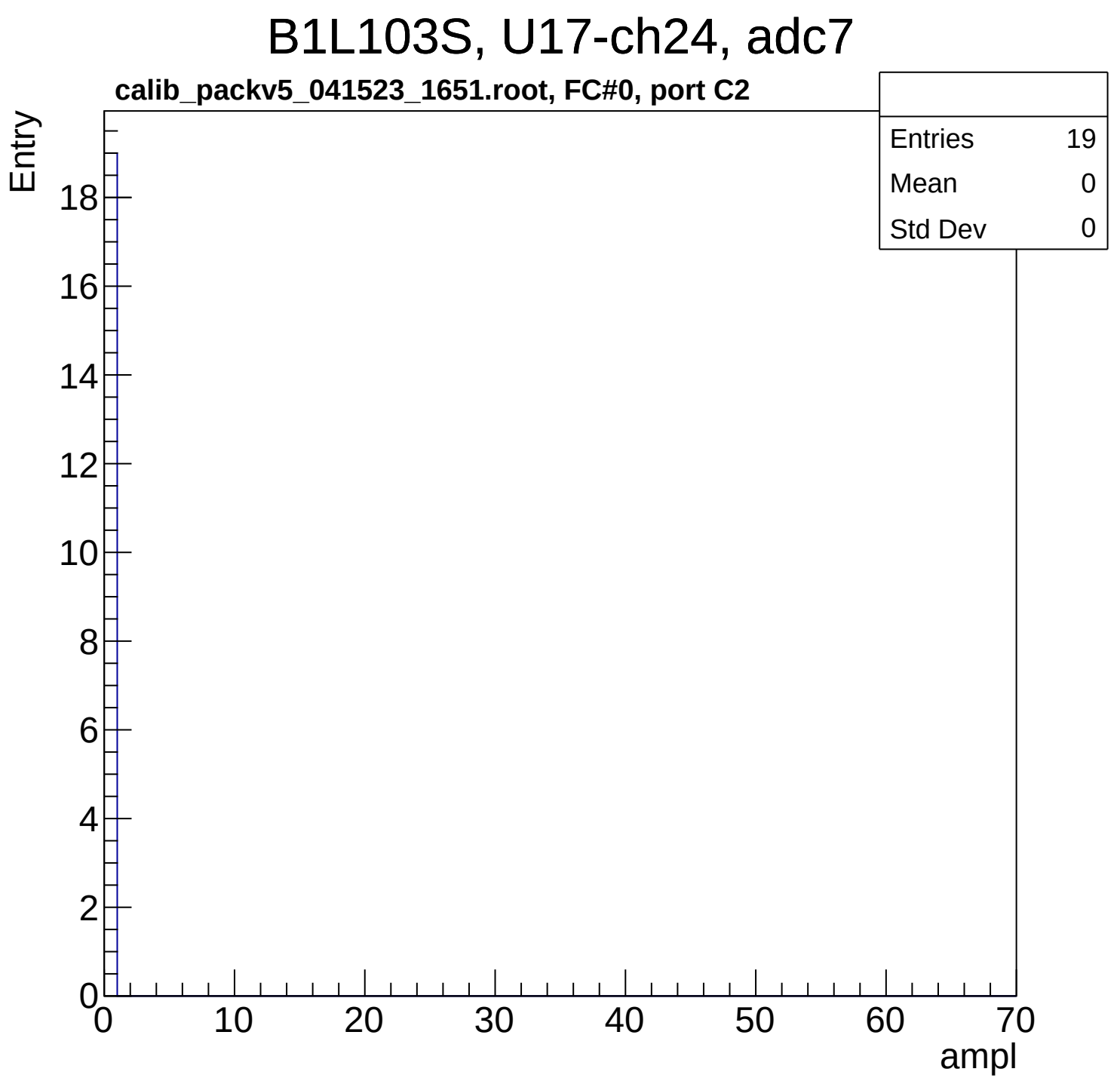
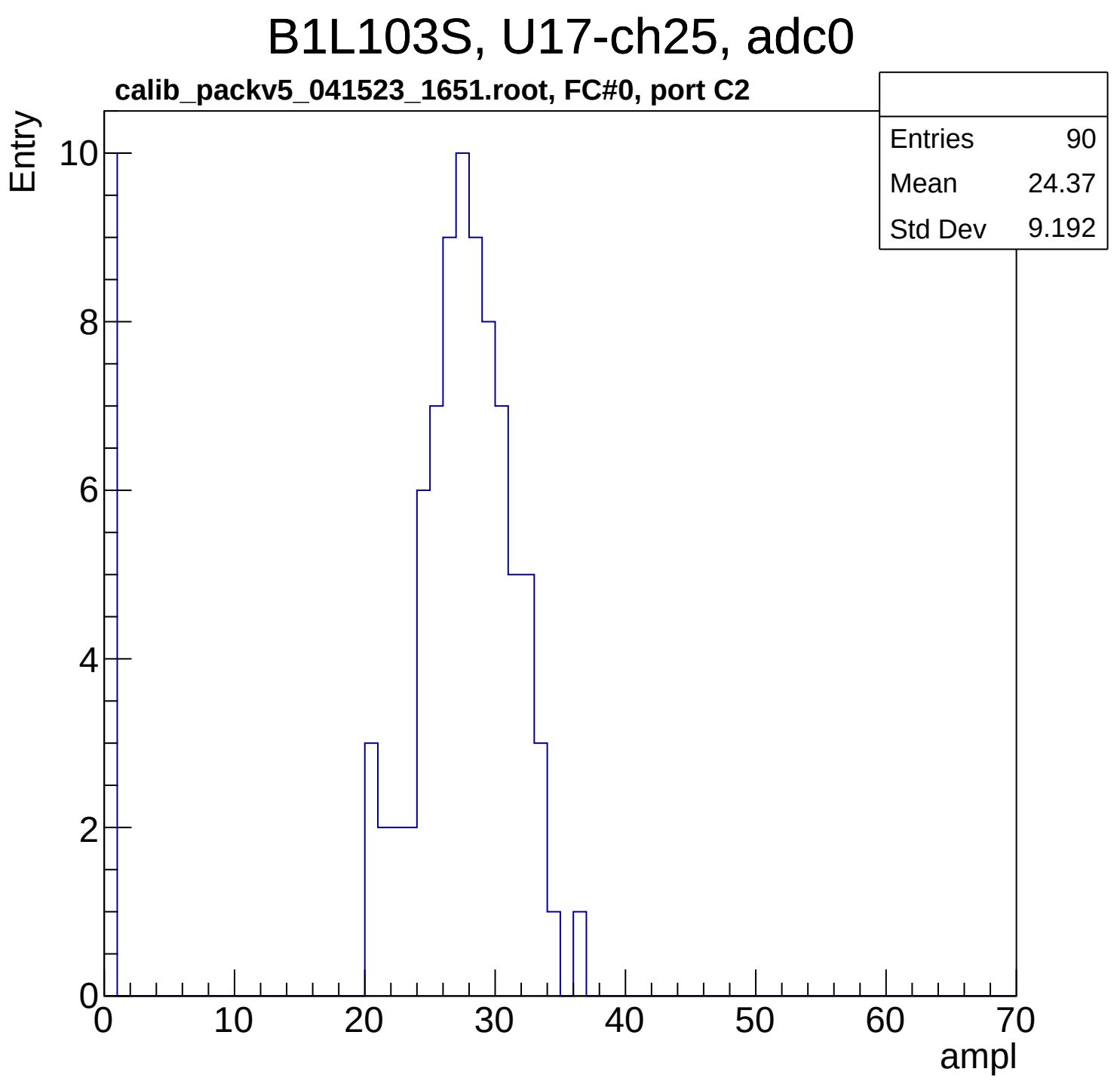
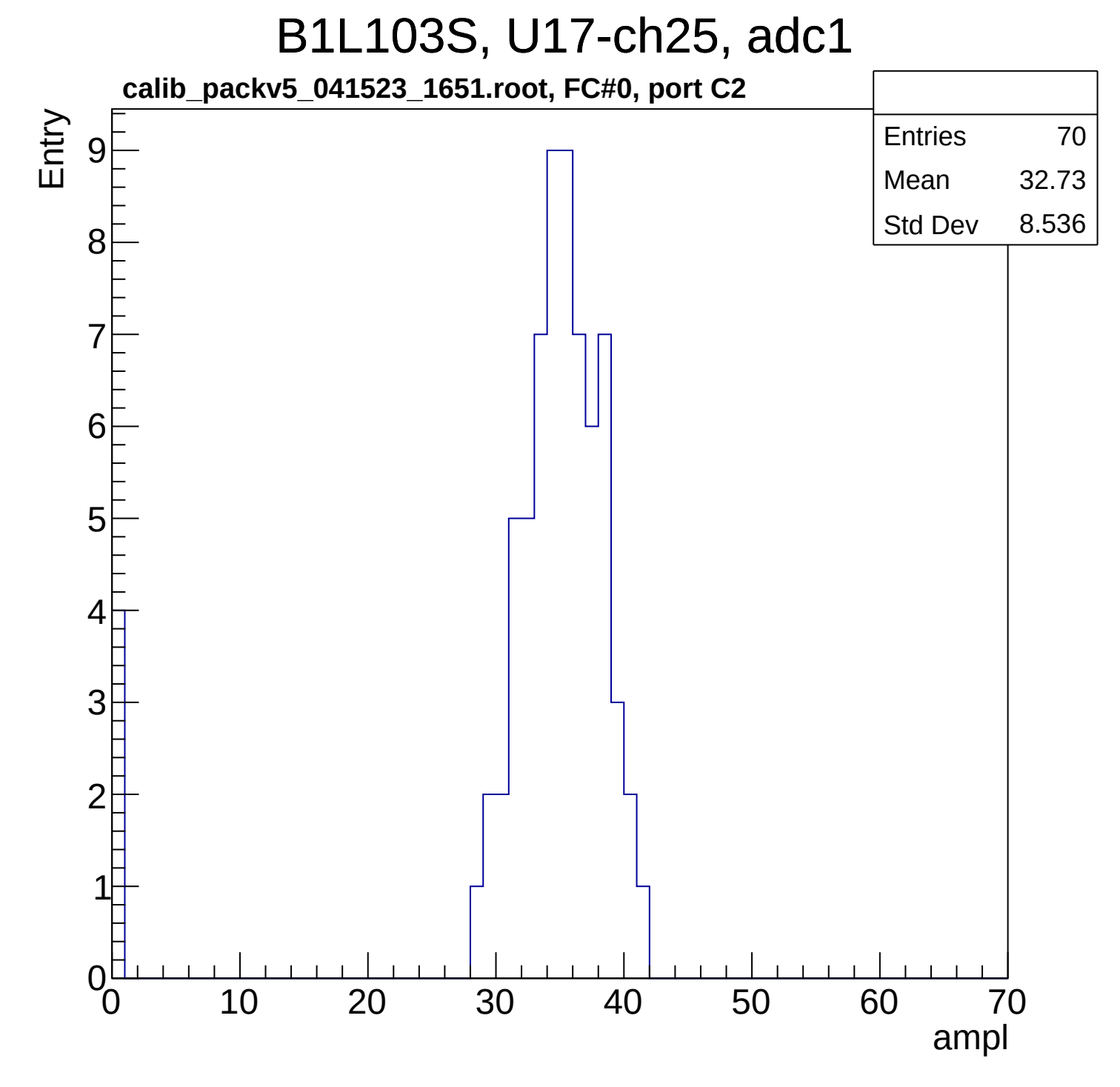

B1L103S, U17-ch24, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 61.5
Std Dev 1.555
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U17-ch24, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch25, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 90
Mean 24.37
Std Dev 9.192
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U17-ch25, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 32.73
Std Dev 8.536
Entry
ampl
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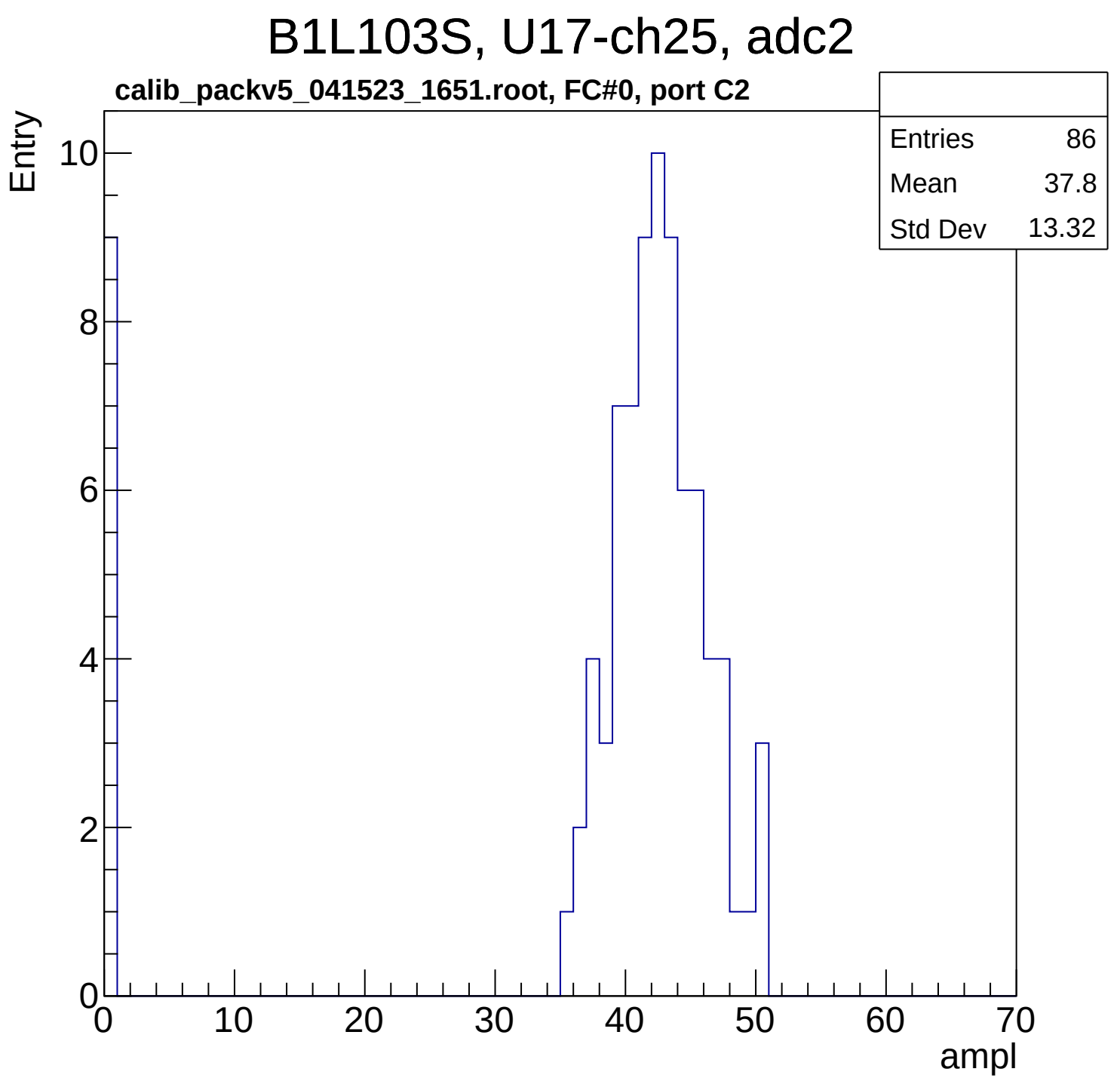
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U17-ch25, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 37.8
Std Dev 13.32
Entry
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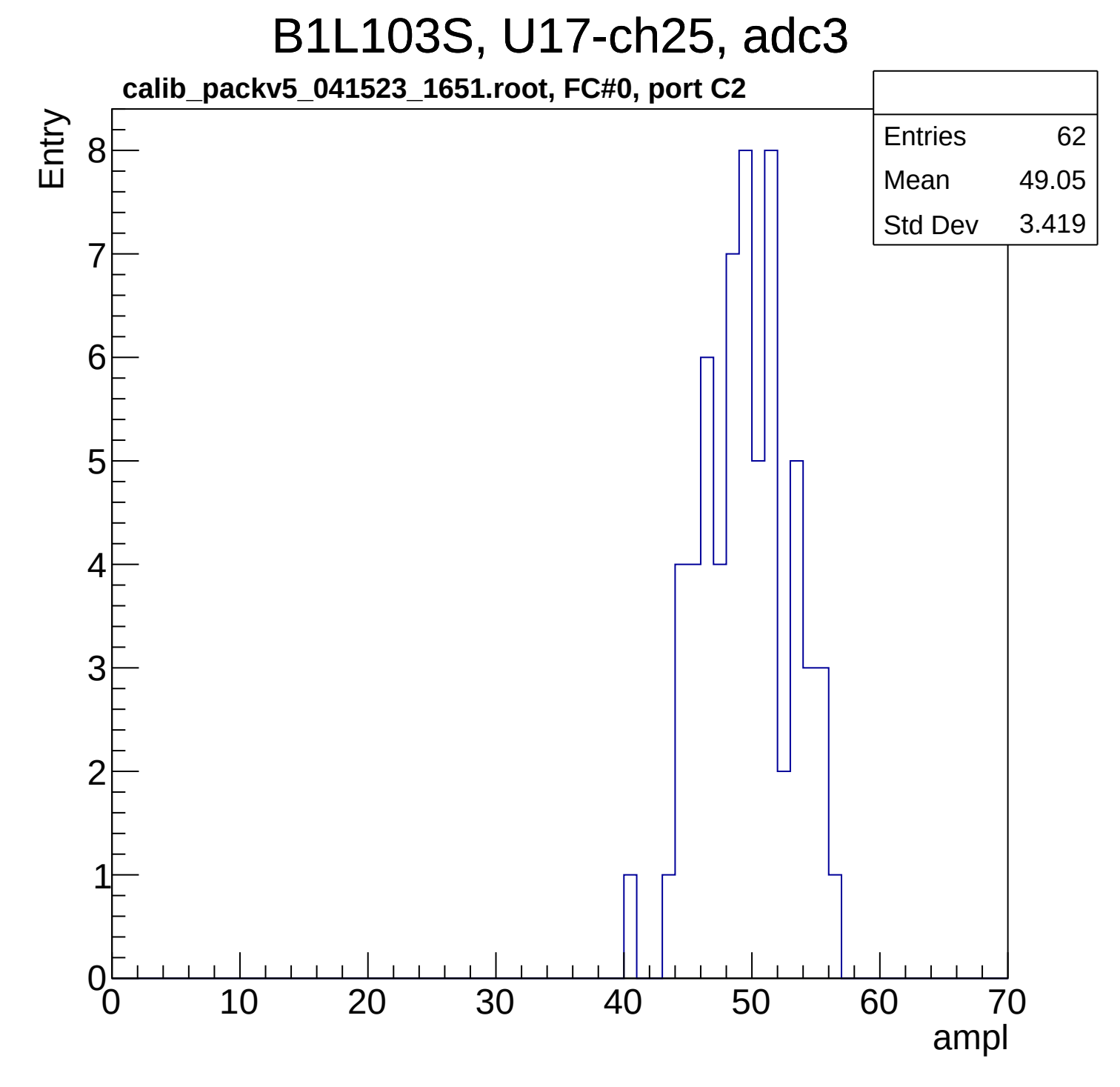
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch25, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 49.05
Std Dev 3.419
Entry
ampl
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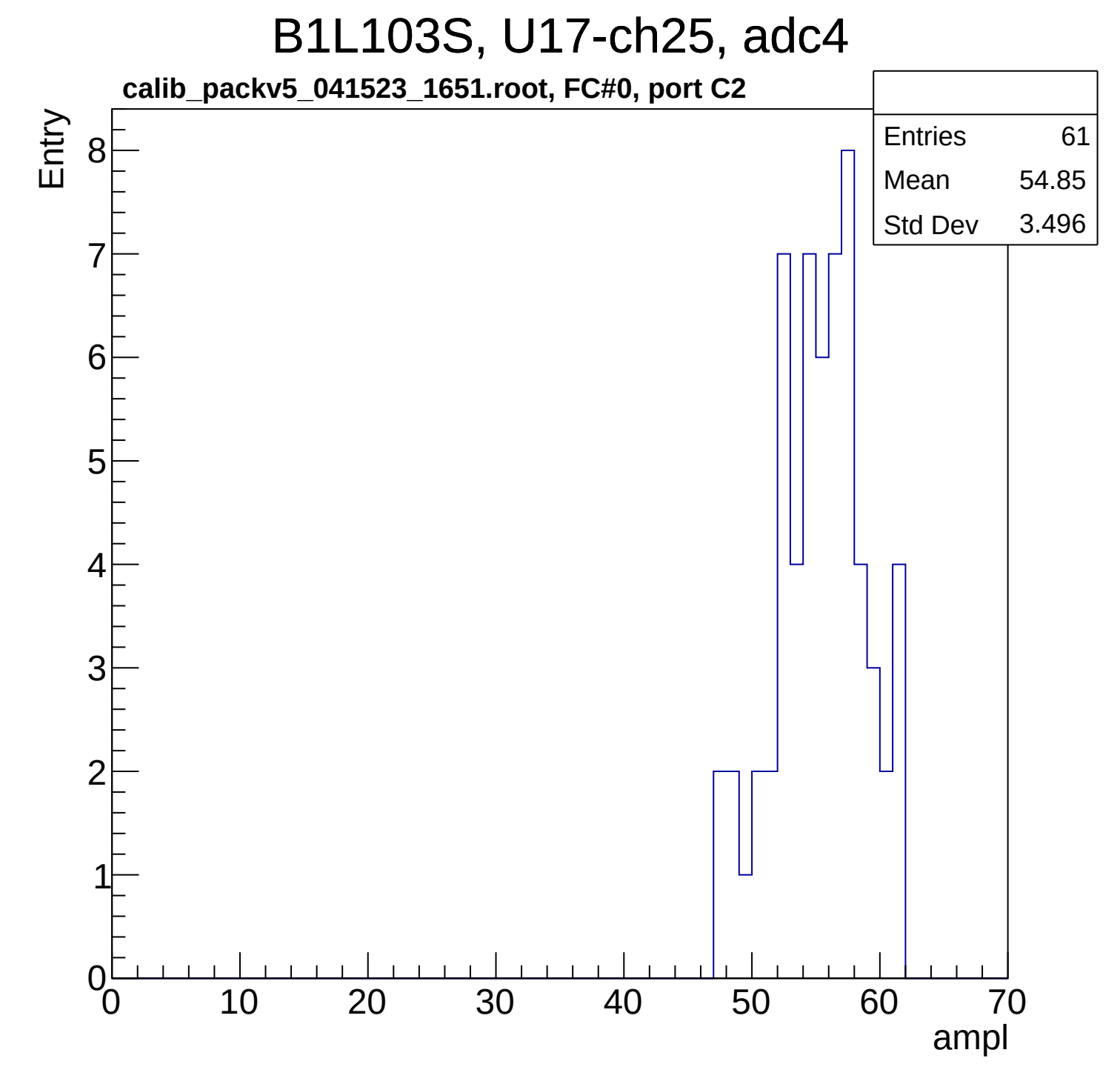
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U17-ch25, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 54.85
Std Dev 3.496
Entry
ampl
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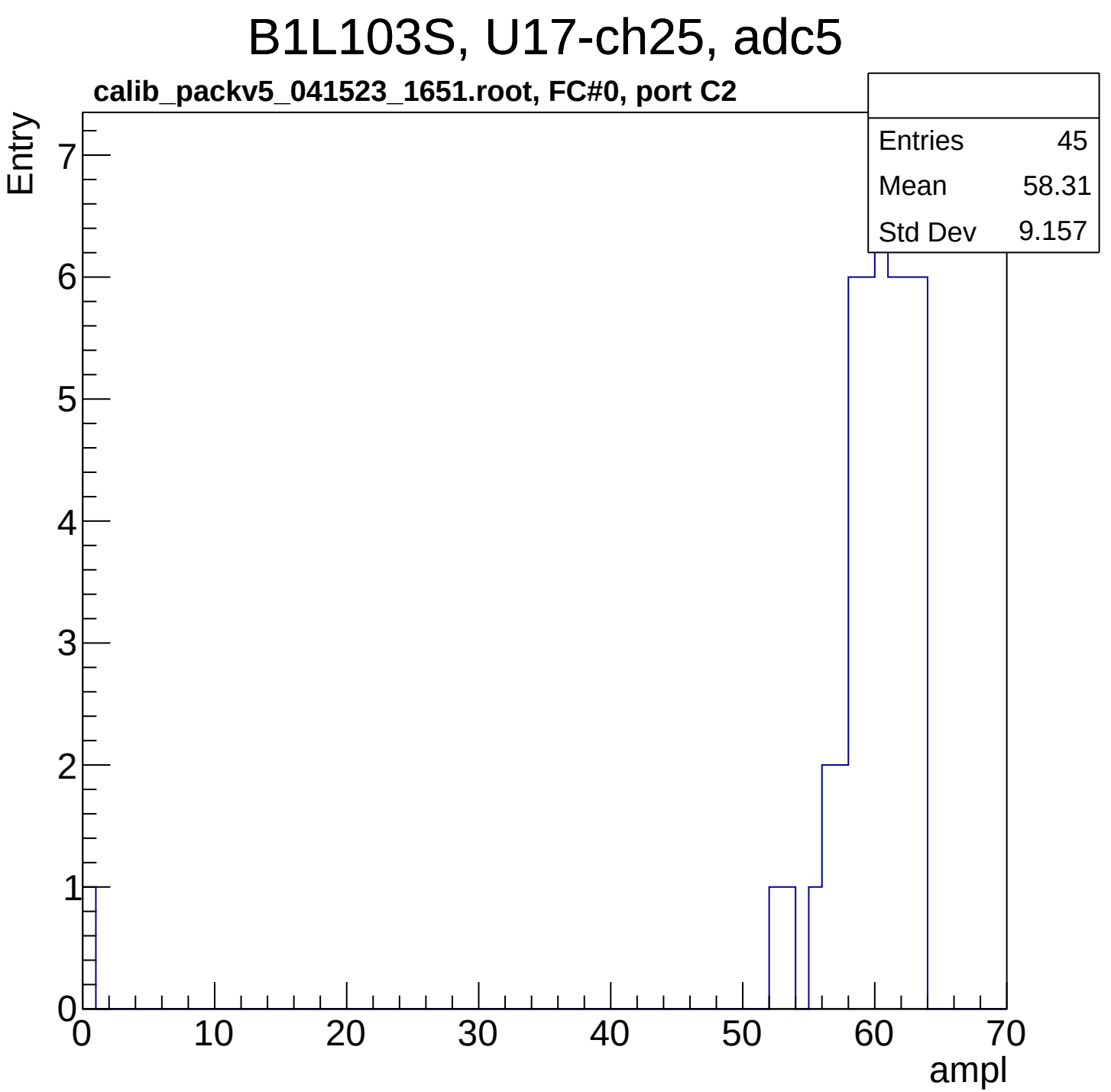
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U17-ch25, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 58.31
Std Dev 9.157
Entry
ampl
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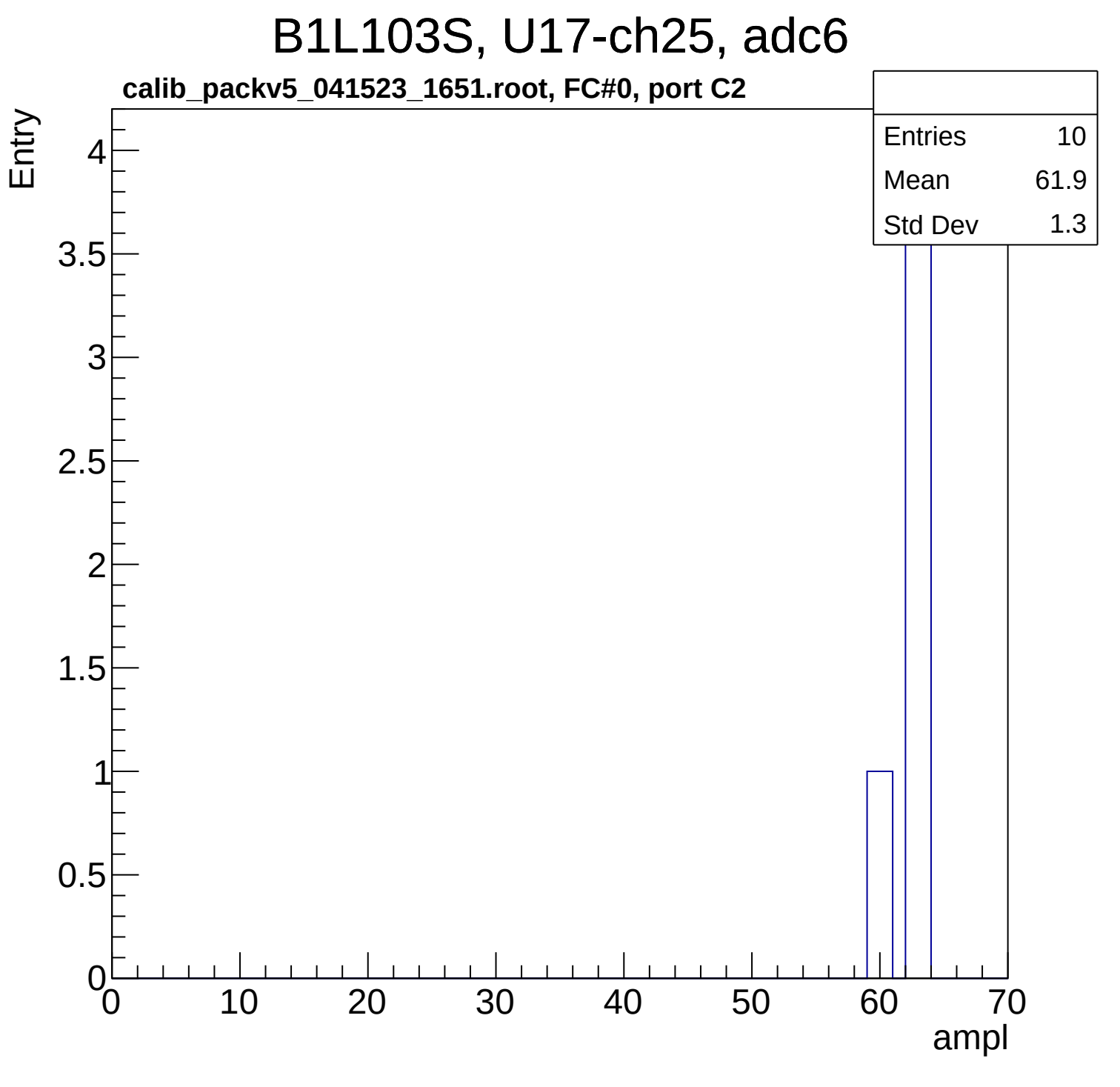
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U17-ch25, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 61.9
Std Dev 1.3
Entry
ampl
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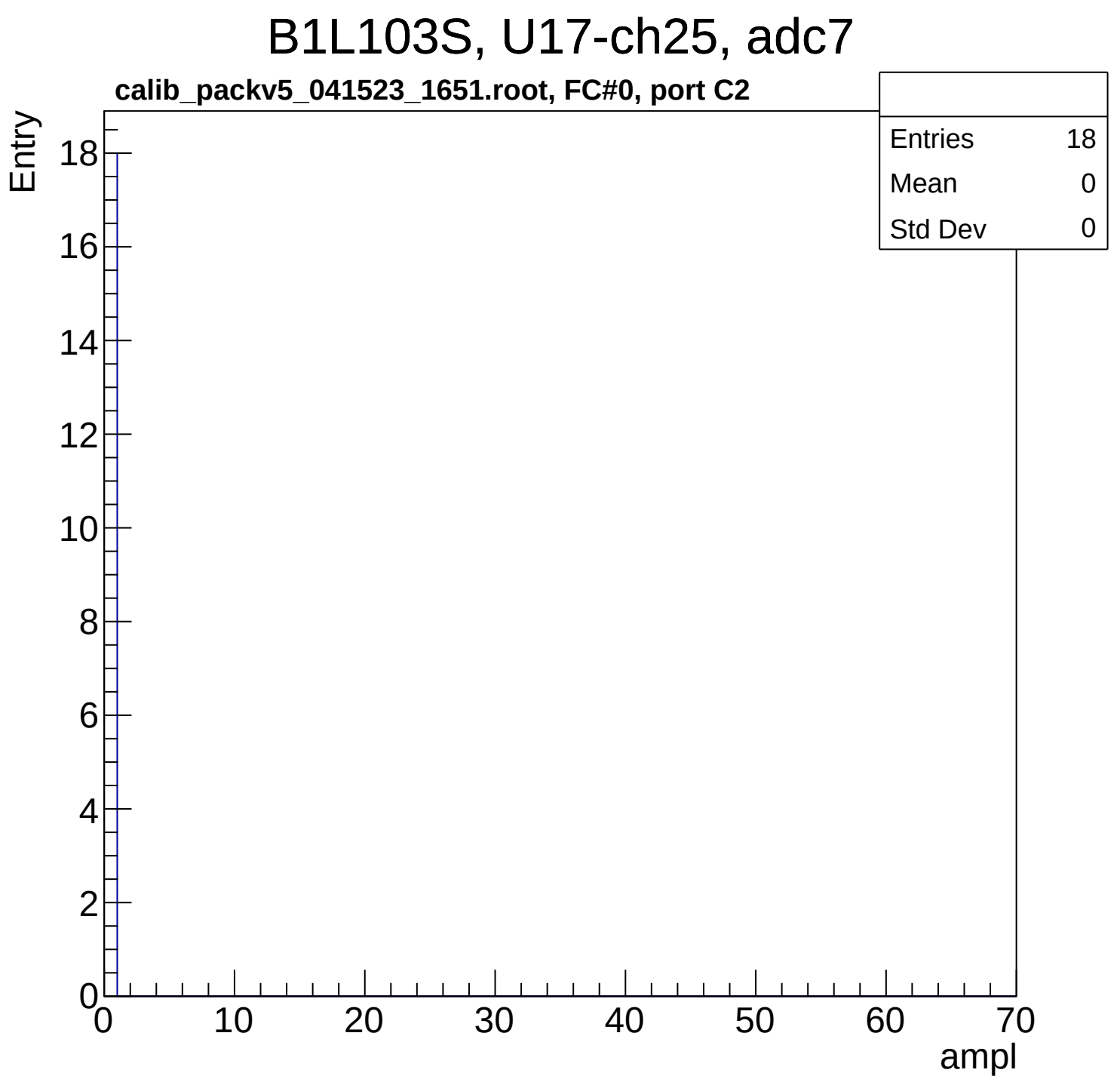
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U17-ch25, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
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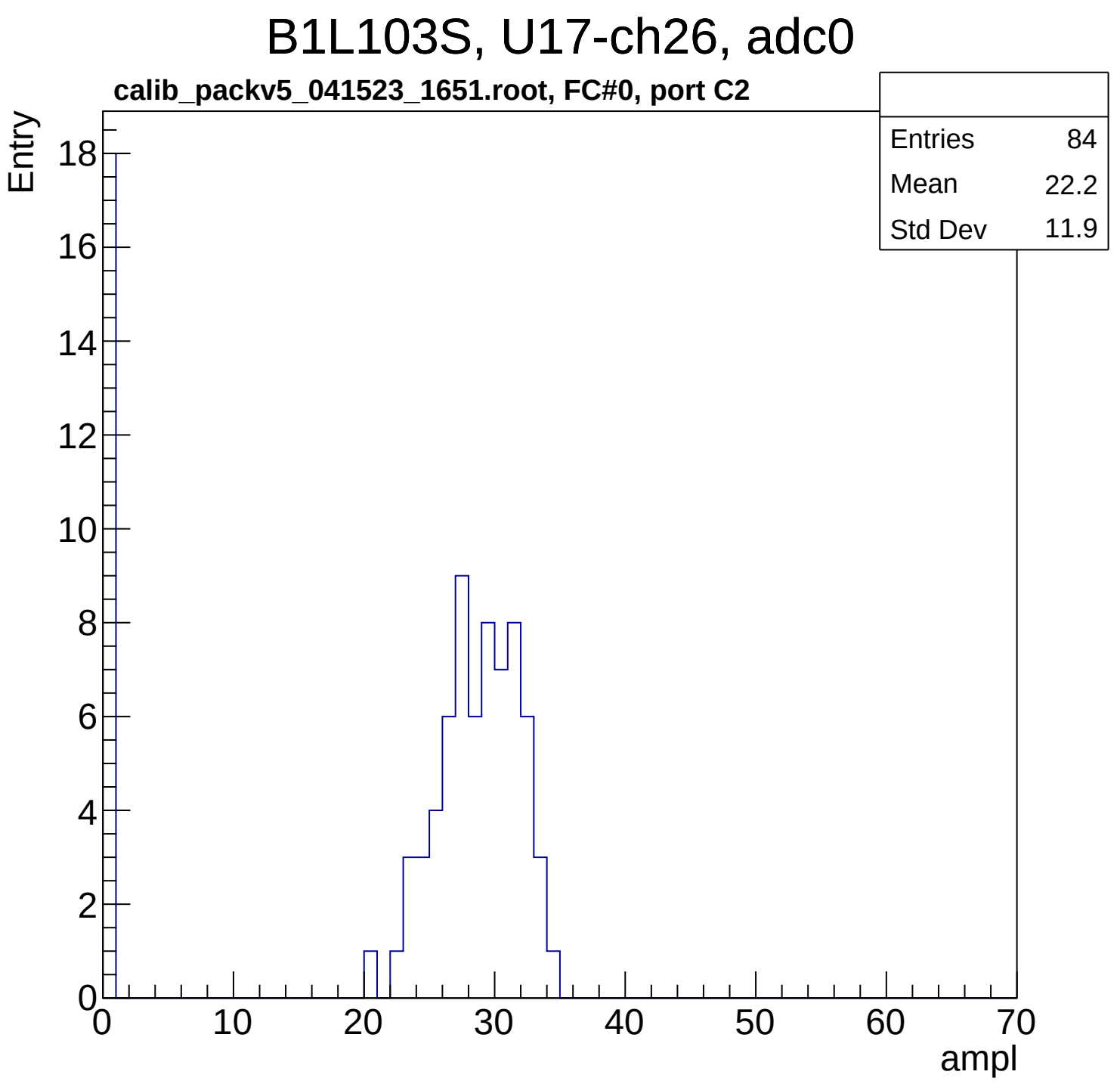
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch26, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 22.2
Std Dev 11.9
Entry
ampl
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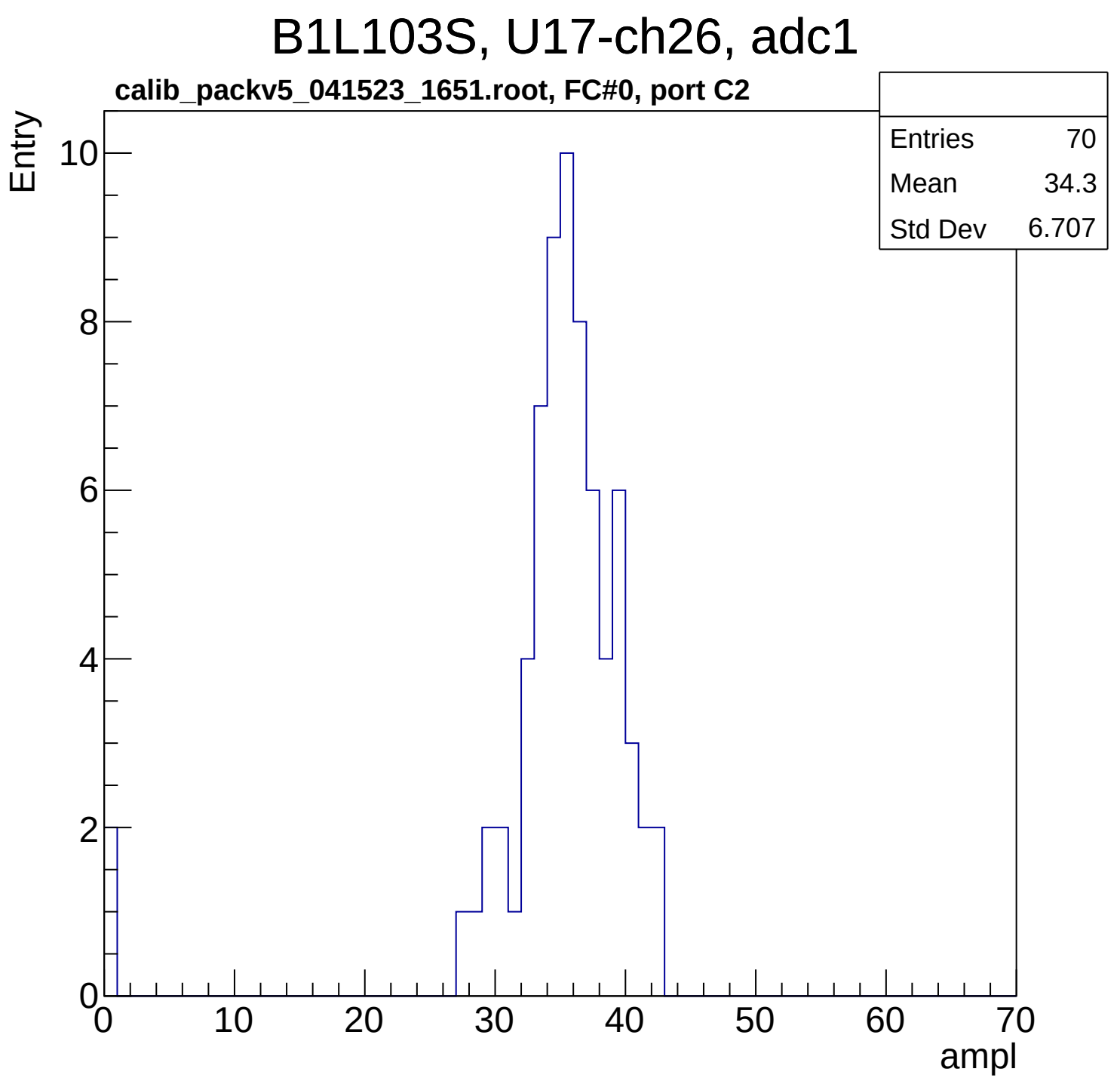
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70


B1L103S, U17-ch26, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 34.3
Std Dev 6.707
Entry
ampl
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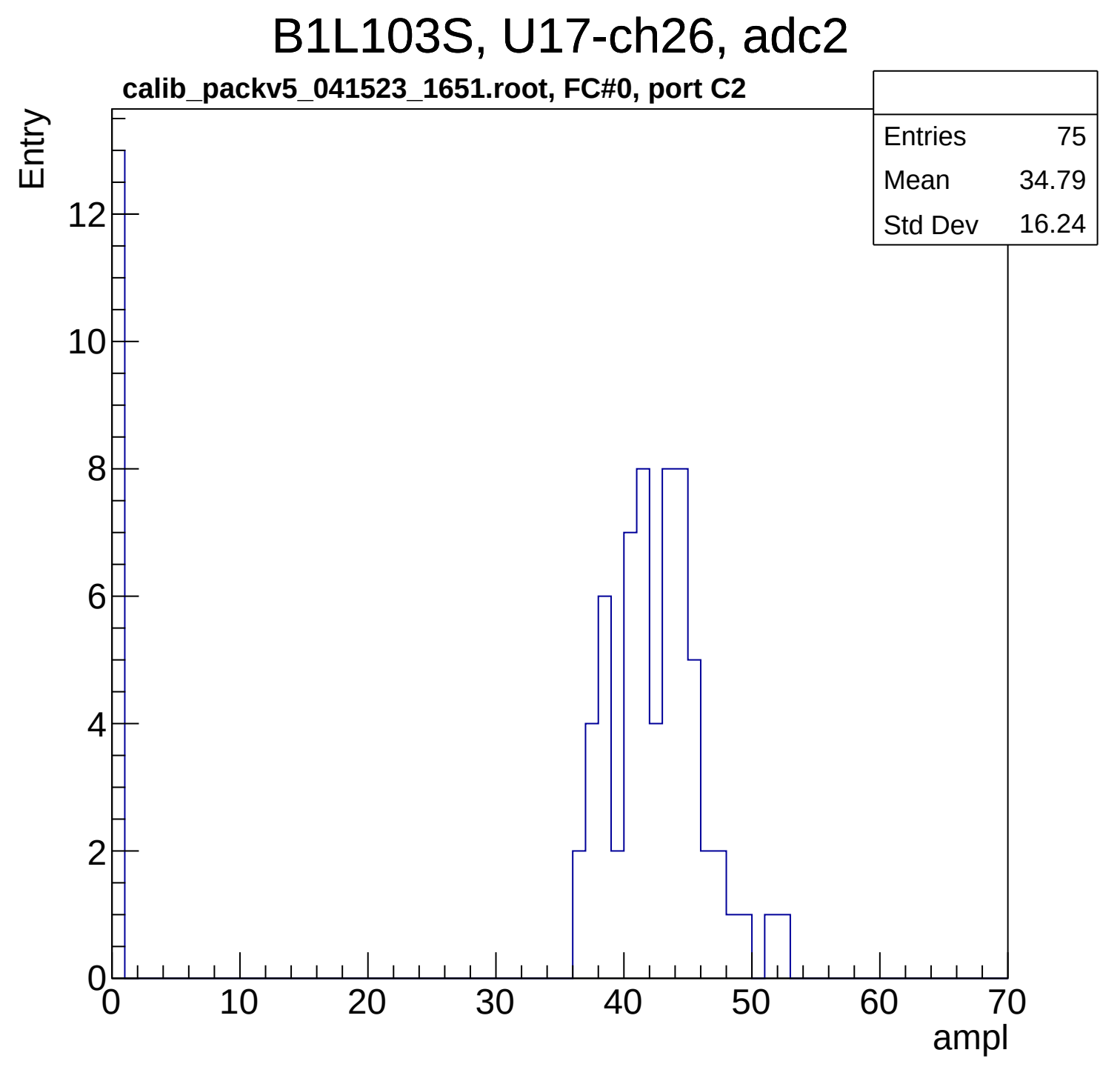
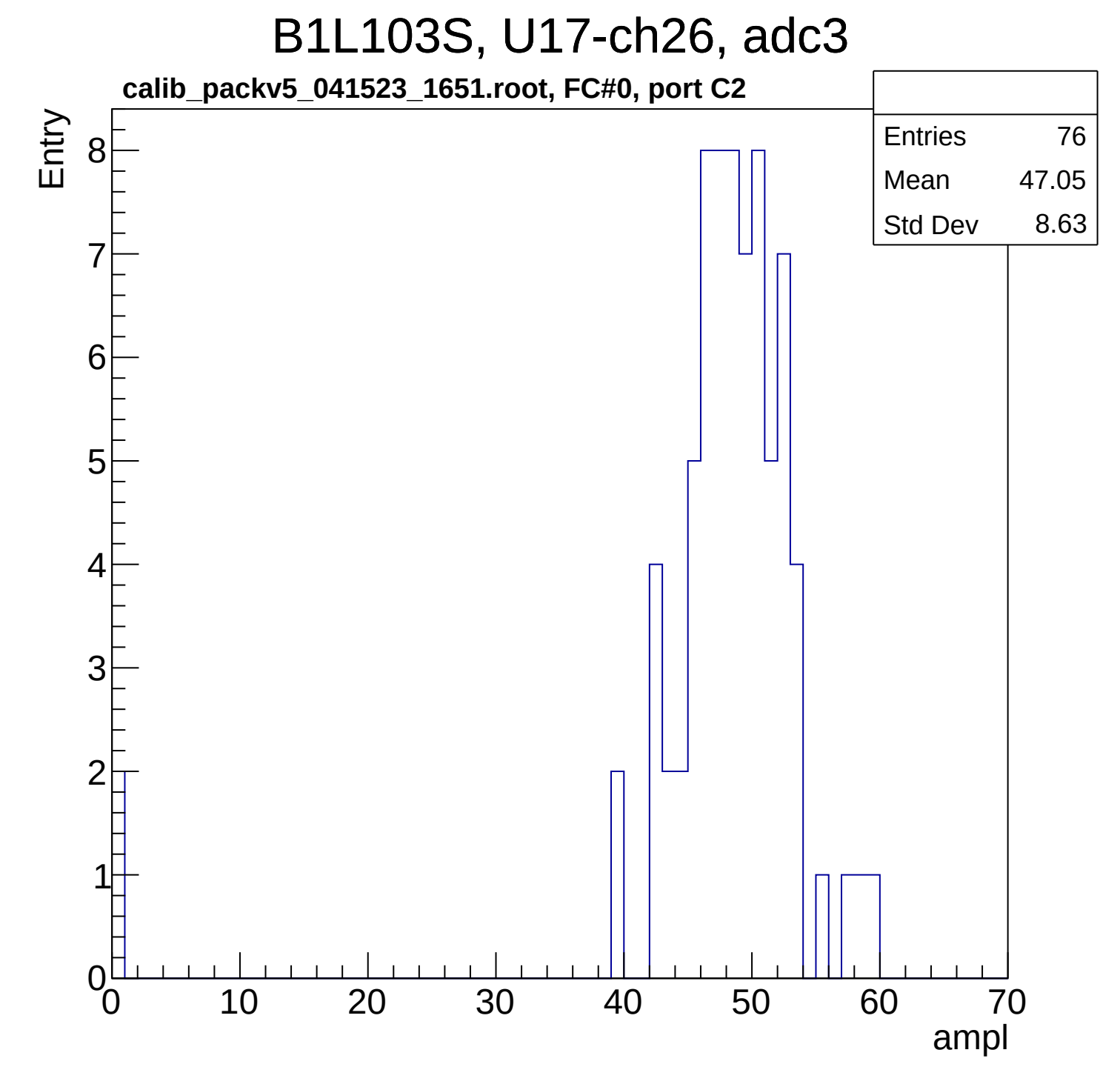
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U17-ch26, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 34.79
Std Dev 16.24
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch26, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 47.05
Std Dev 8.63
Entry
ampl
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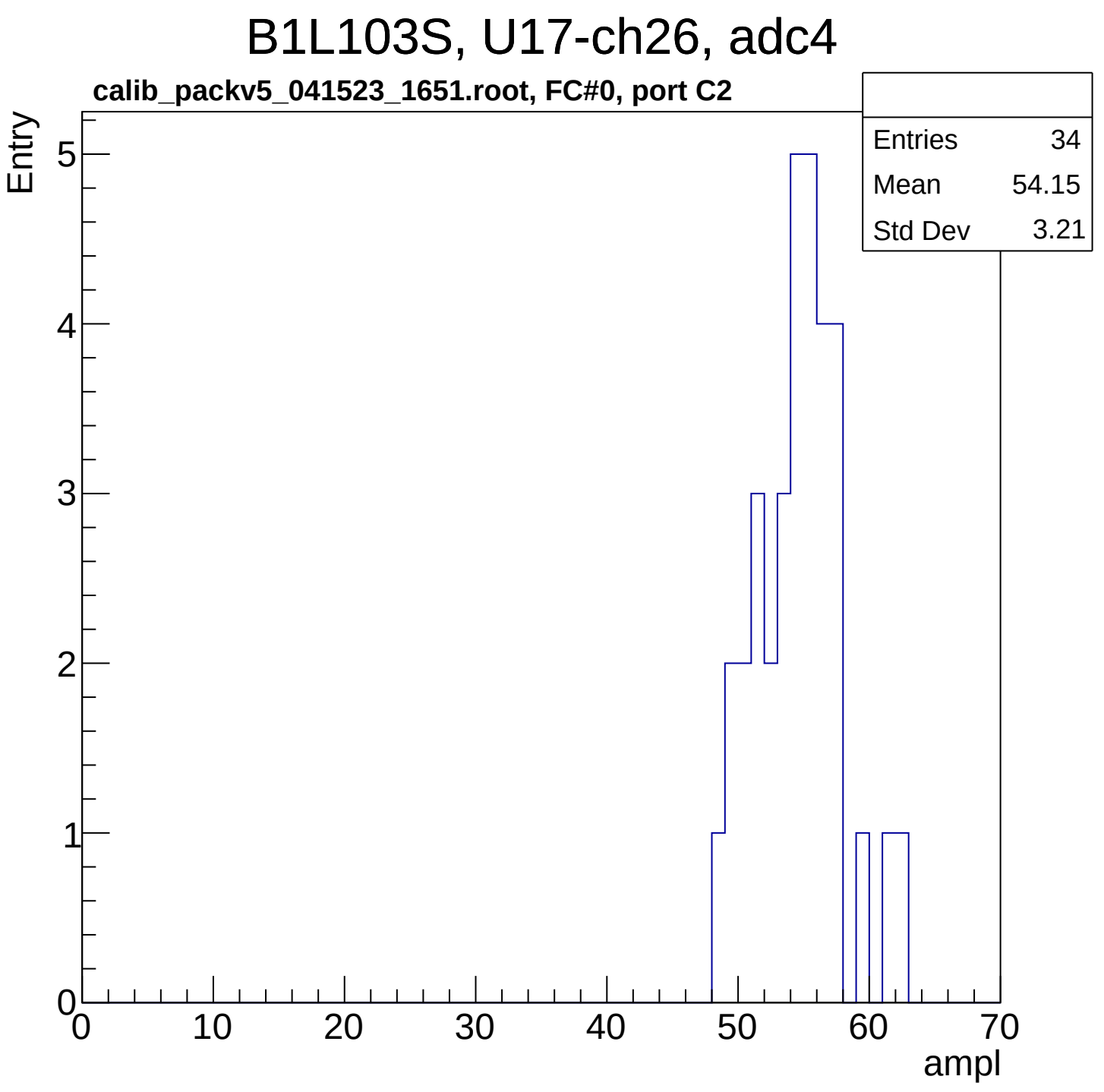
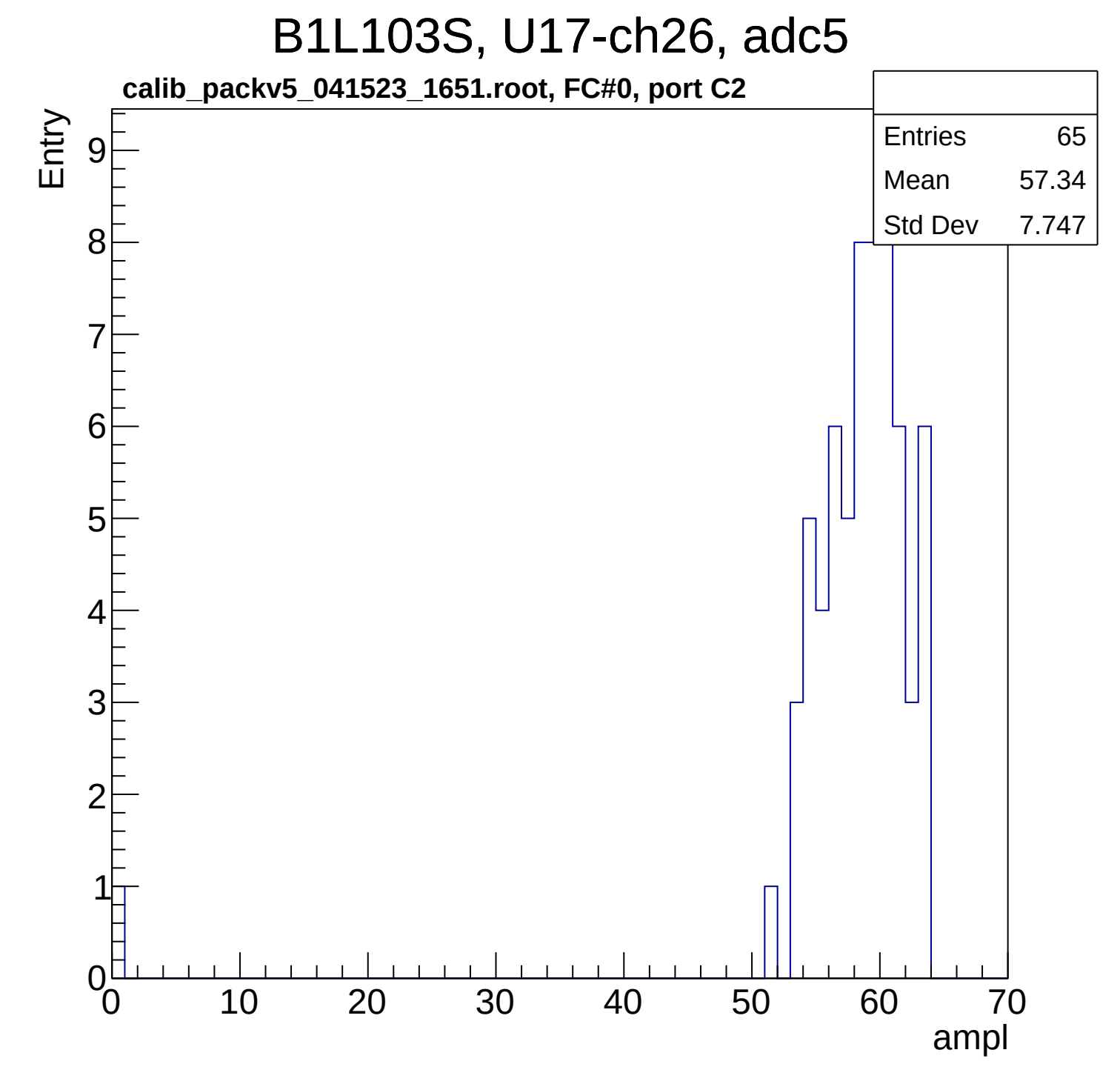
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U17-ch26, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 34
Mean 54.15
Std Dev 3.21
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch26, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 57.34
Std Dev 7.747
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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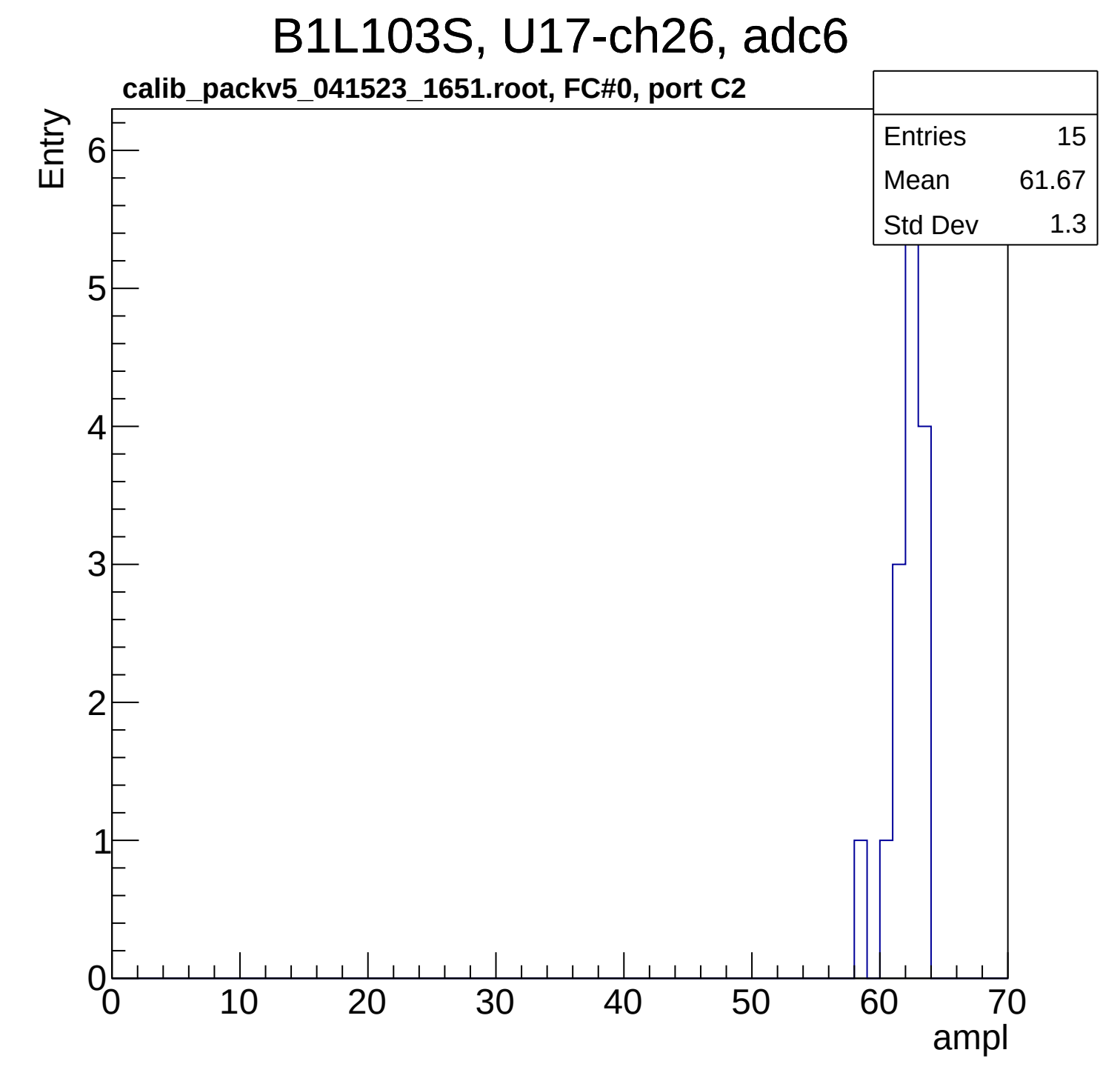
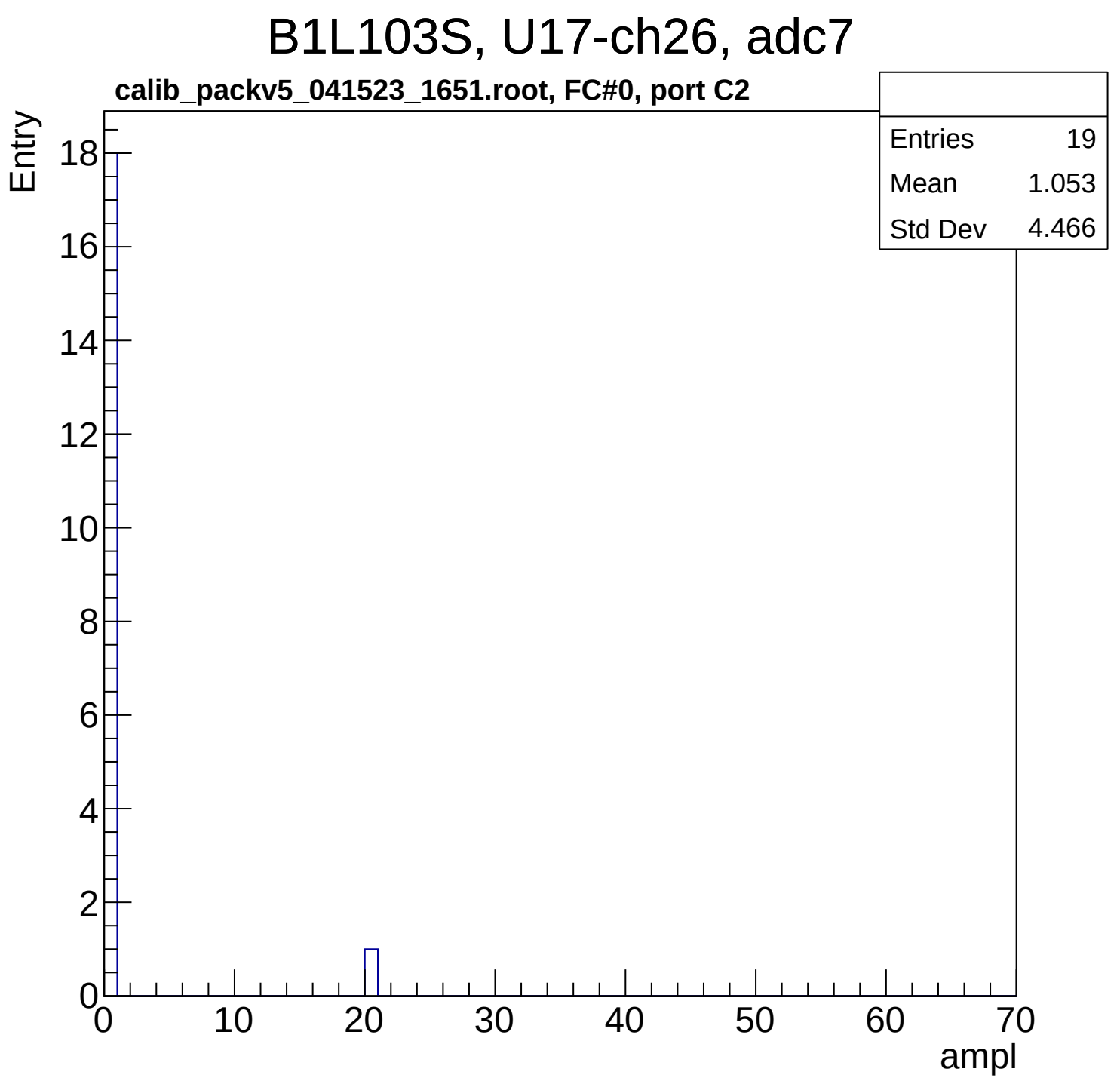
40
50
60
70


B1L103S, U17-ch26, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 15
Mean 61.67
Std Dev 1.3
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U17-ch26, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.053
Std Dev 4.466
Entry
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4
6
8
10
12
14
16
18
0
10
20
30
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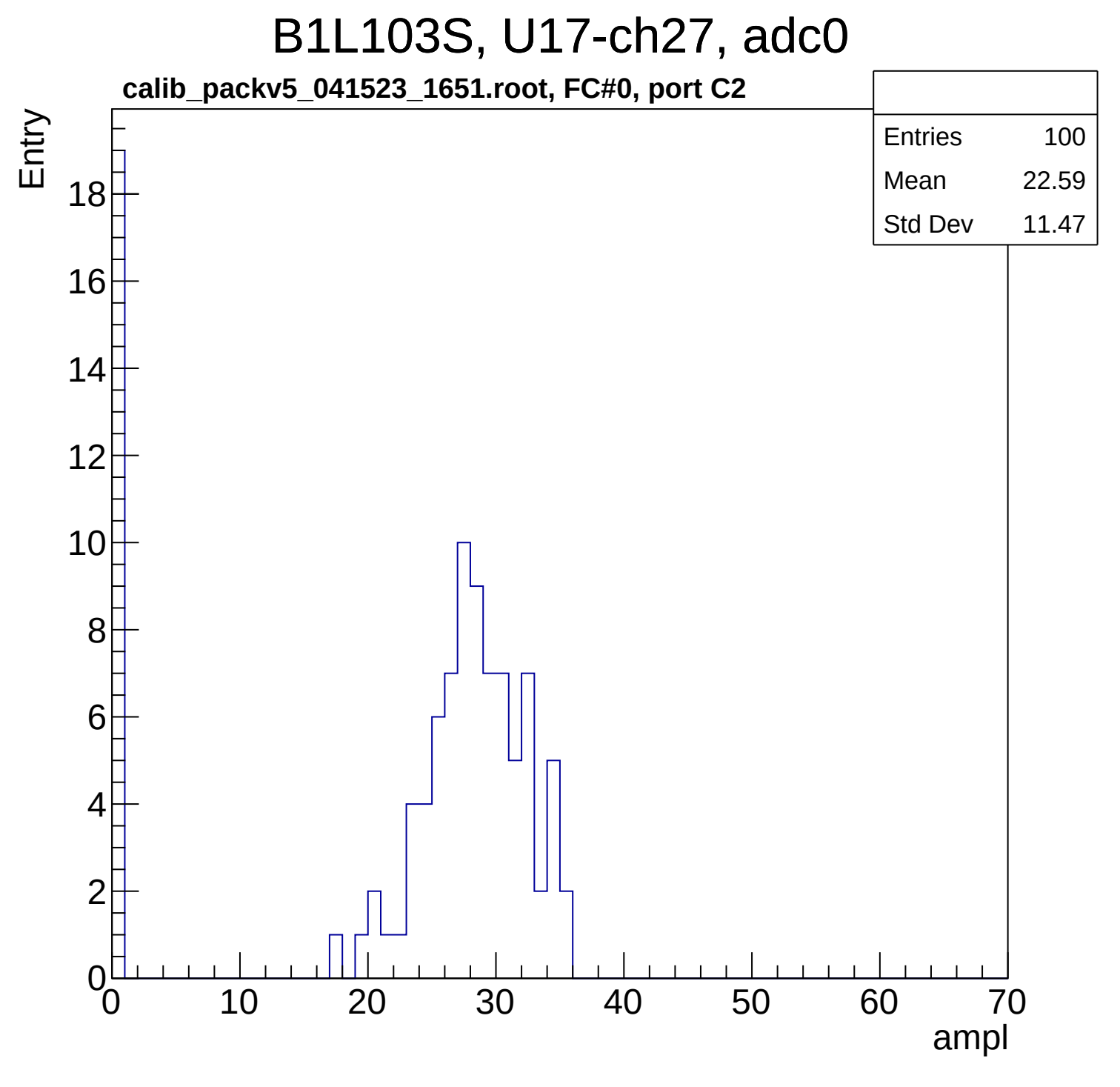
50
60
70
ampl


B1L103S, U17-ch27, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 100
Mean 22.59
Std Dev 11.47
Entry
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4
6
8
10
12
14
16
18
0
10
20
30
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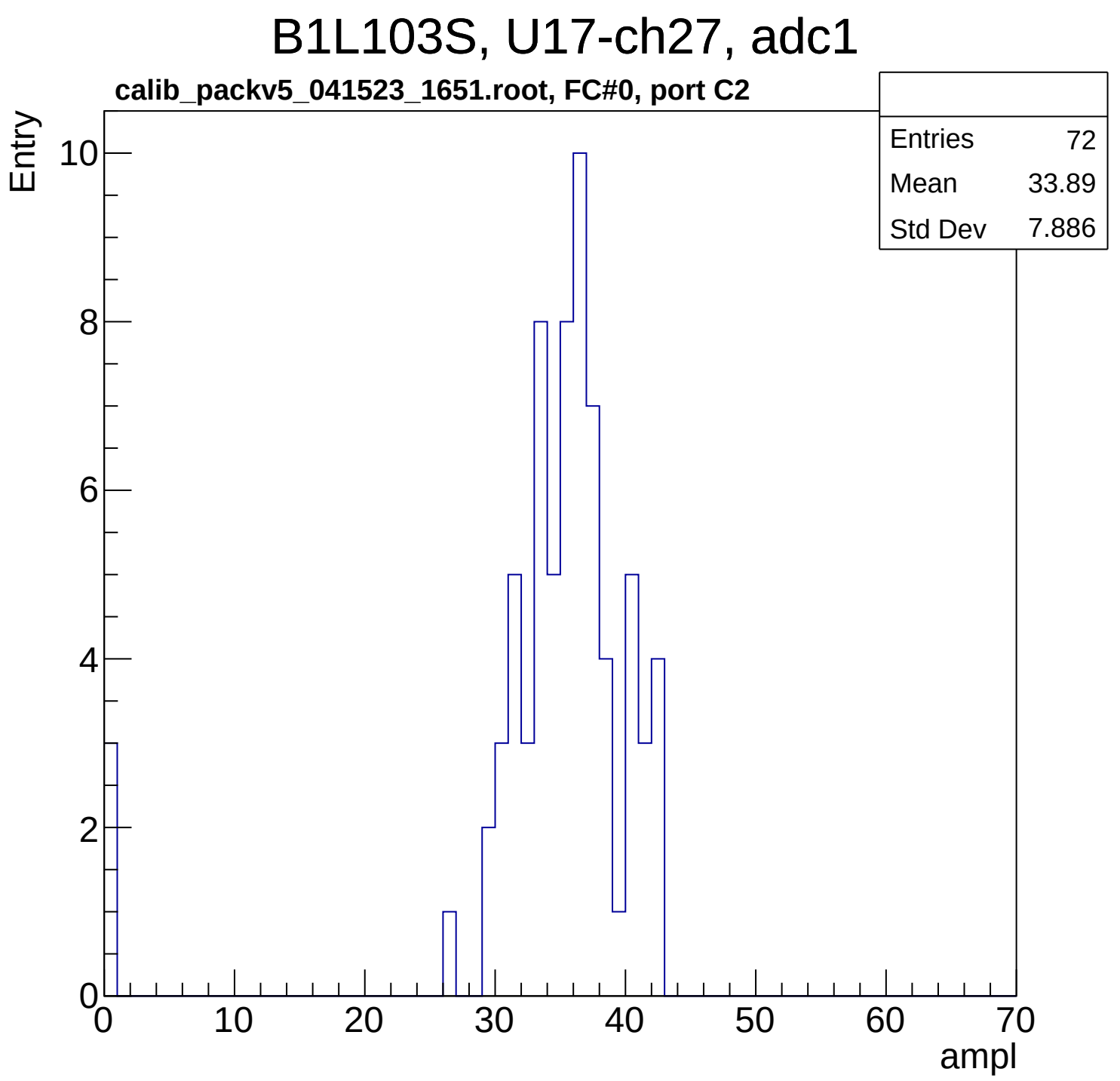
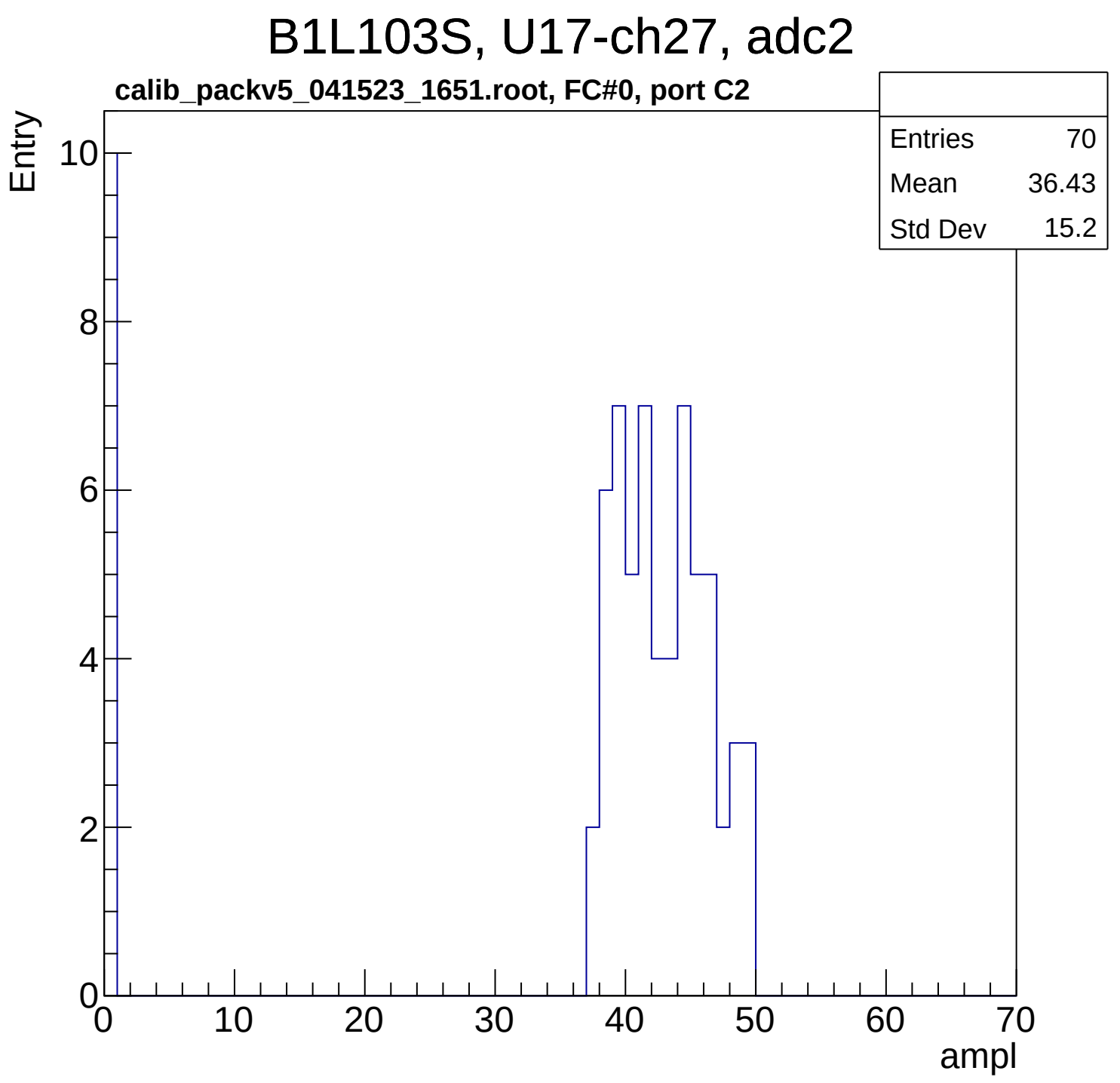
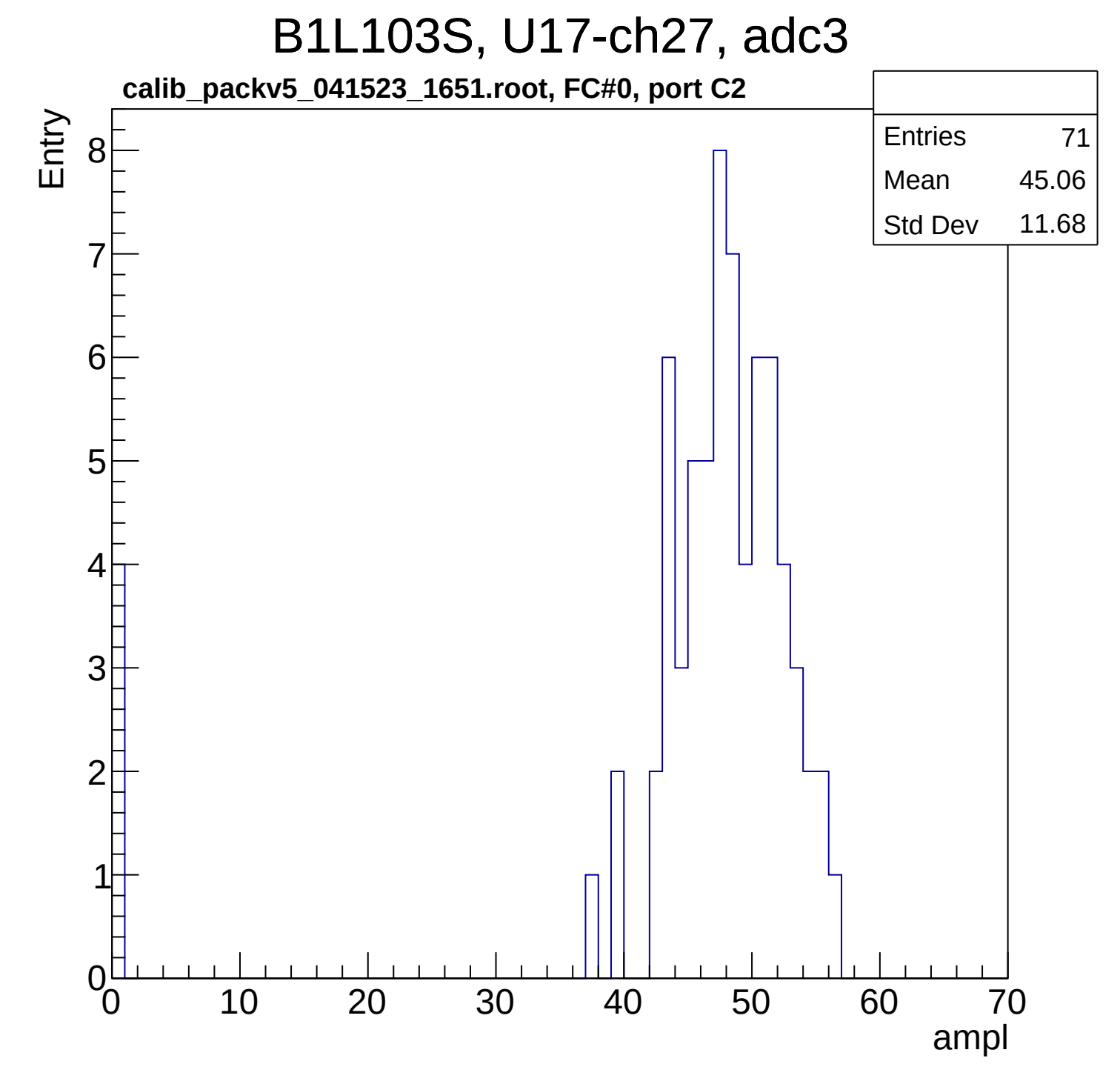
50
60
70
ampl


B1L103S, U17-ch27, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 33.89
Std Dev 7.886
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U17-ch27, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 36.43
Std Dev 15.2
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch27, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 45.06
Std Dev 11.68
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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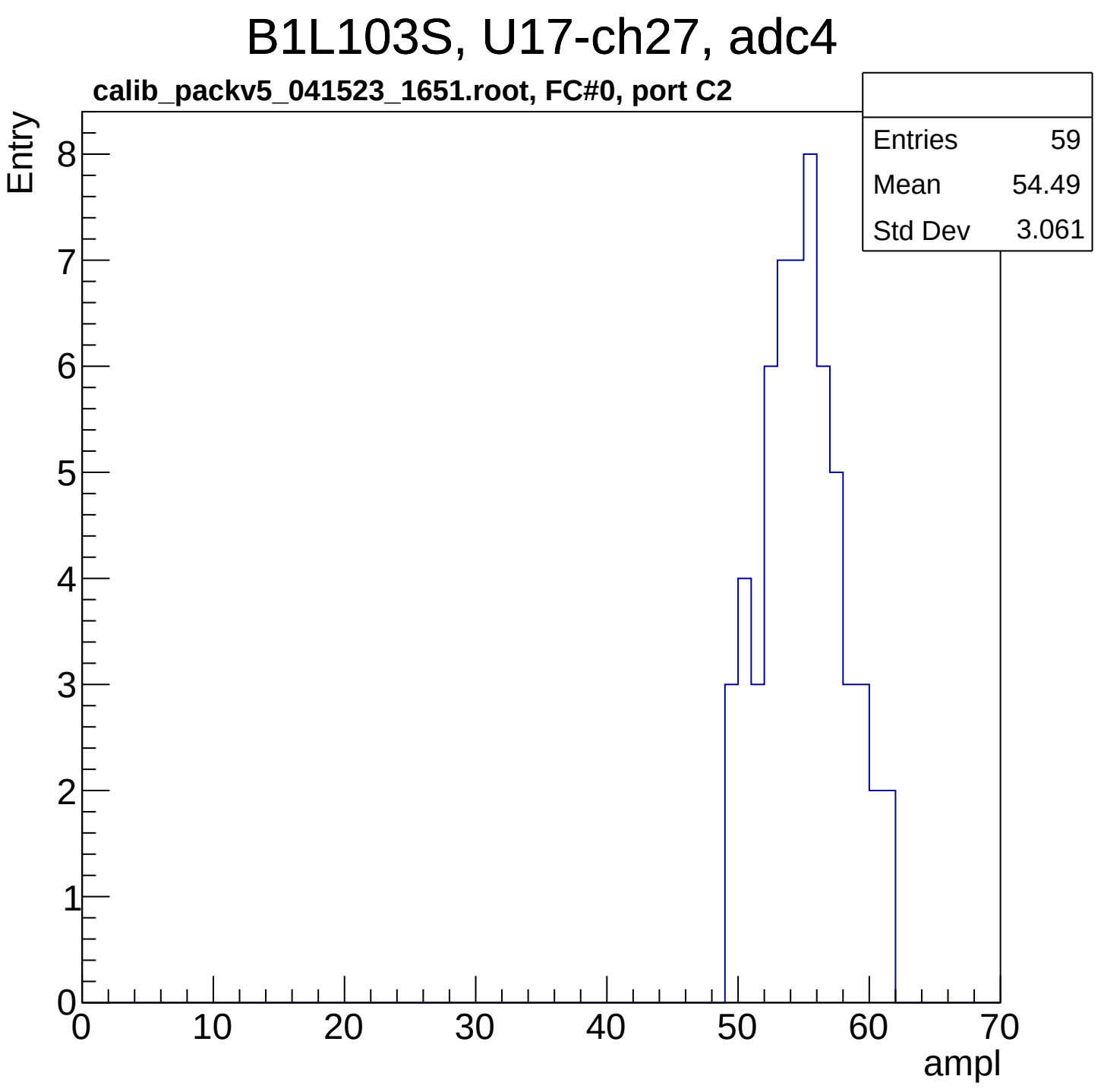
B1L103S, U17-ch27, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 54.49
Std Dev 3.061
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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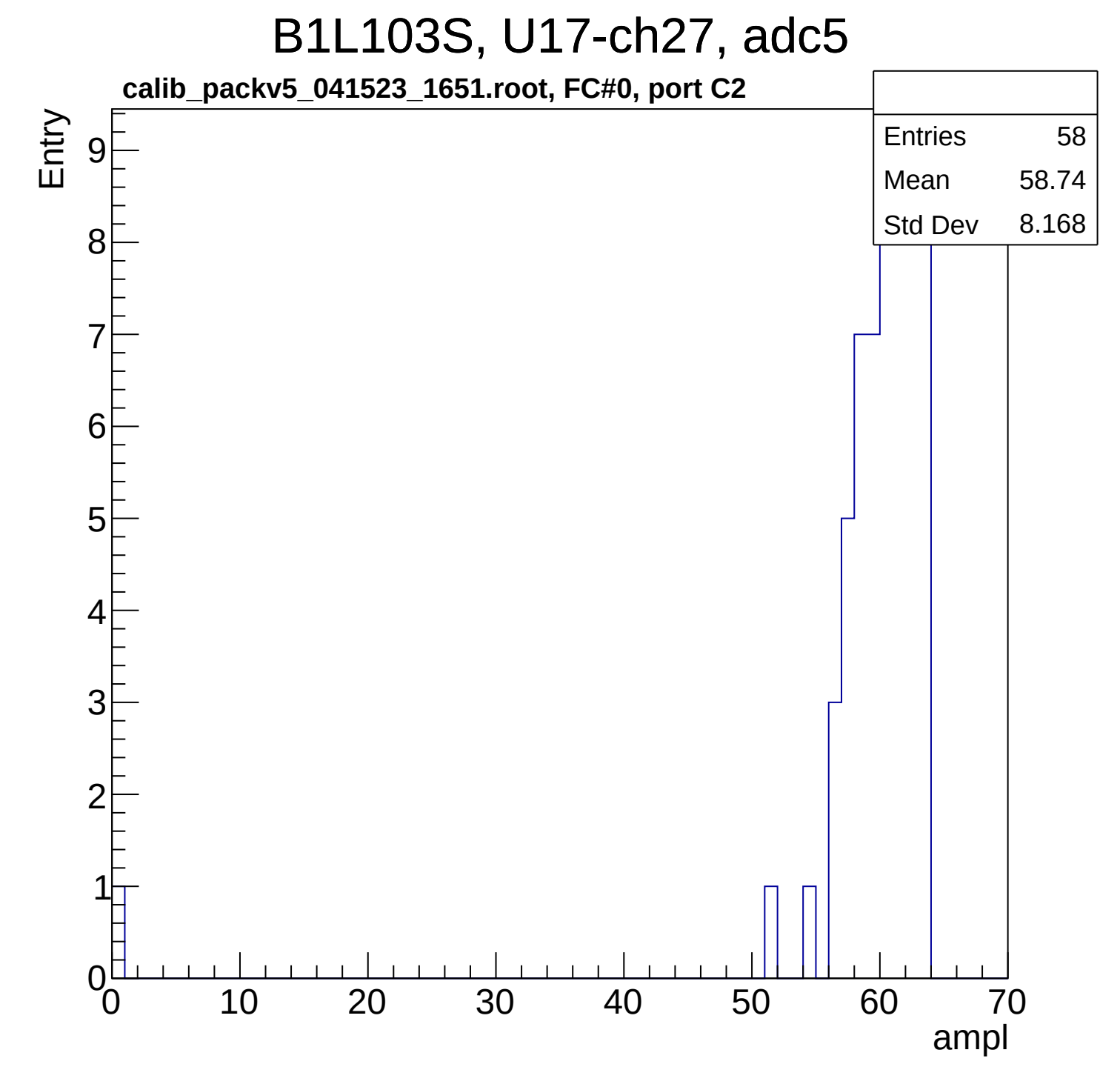
B1L103S, U17-ch27, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 58.74
Std Dev 8.168
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
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40
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60
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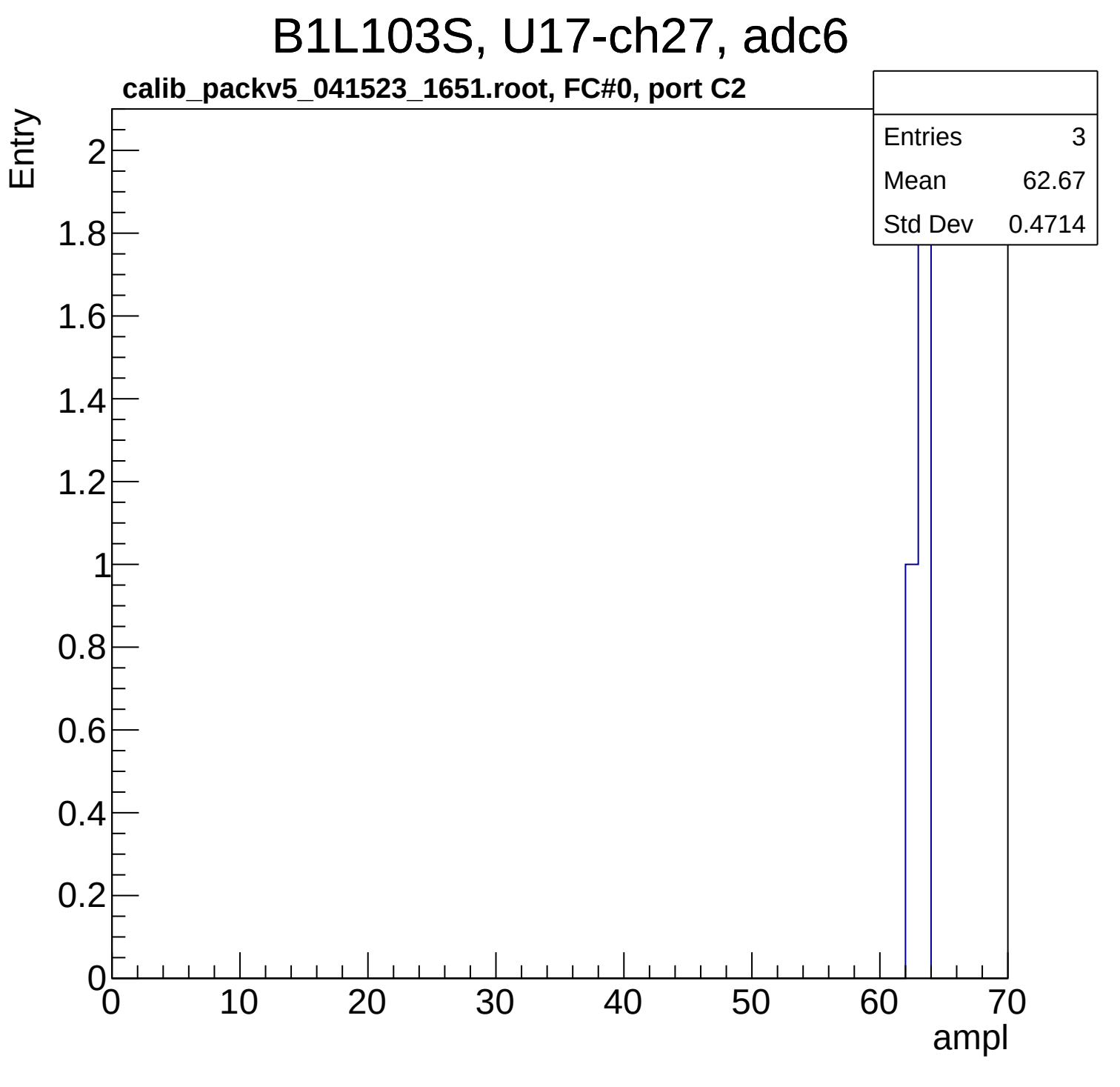
B1L103S, U17-ch27, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 3
Mean 62.67
Std Dev 0.4714
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
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40
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60
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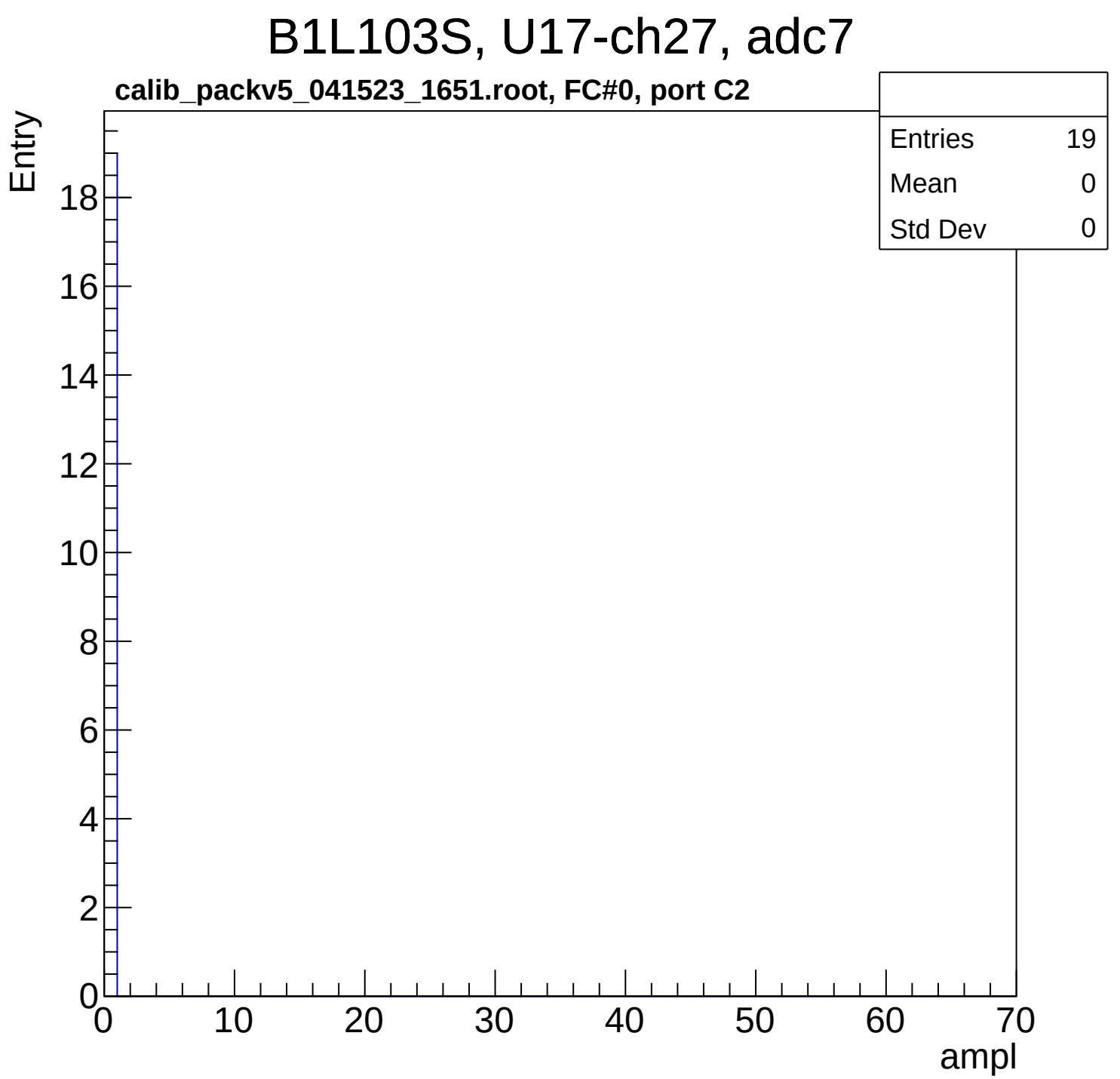
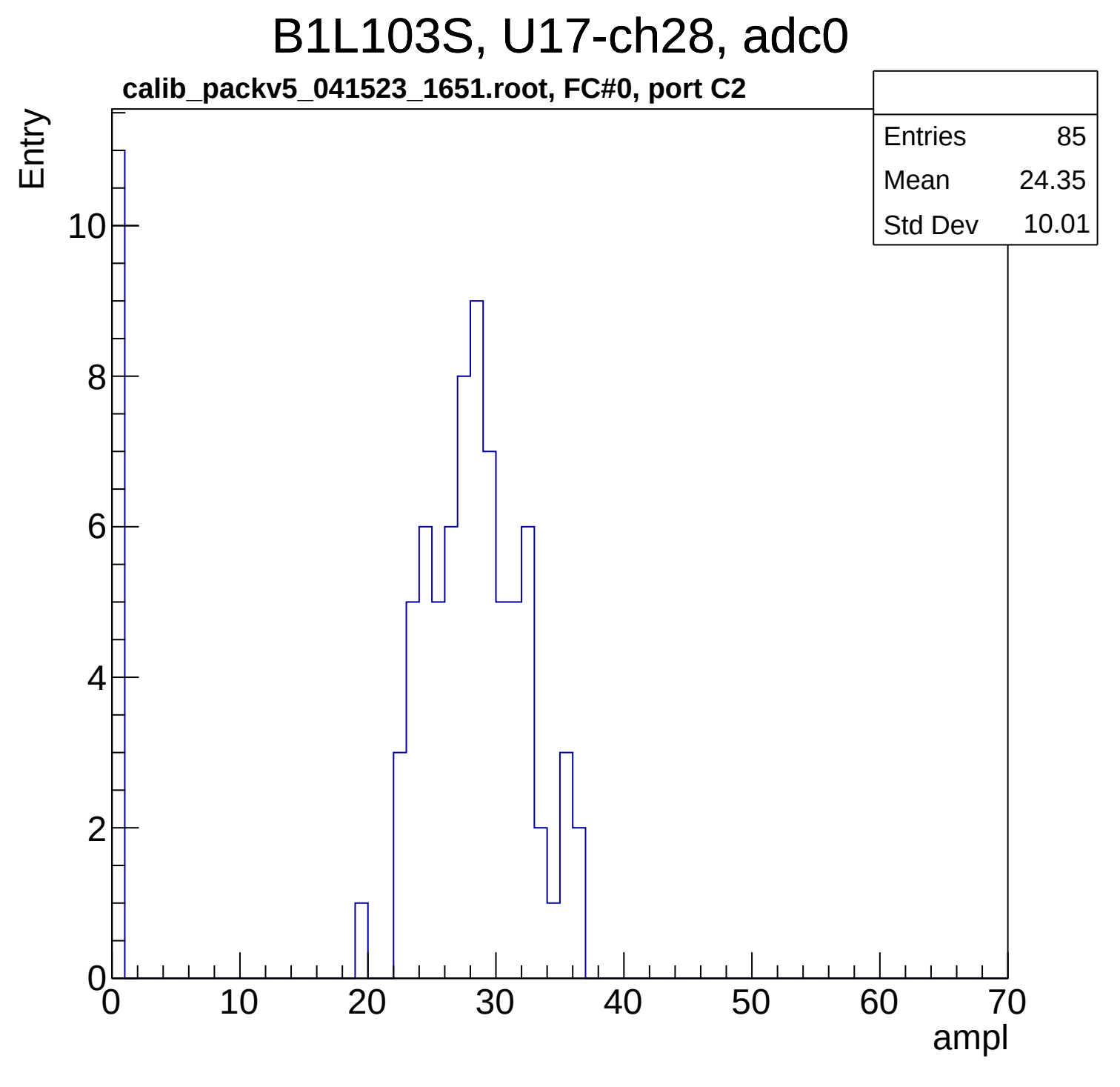
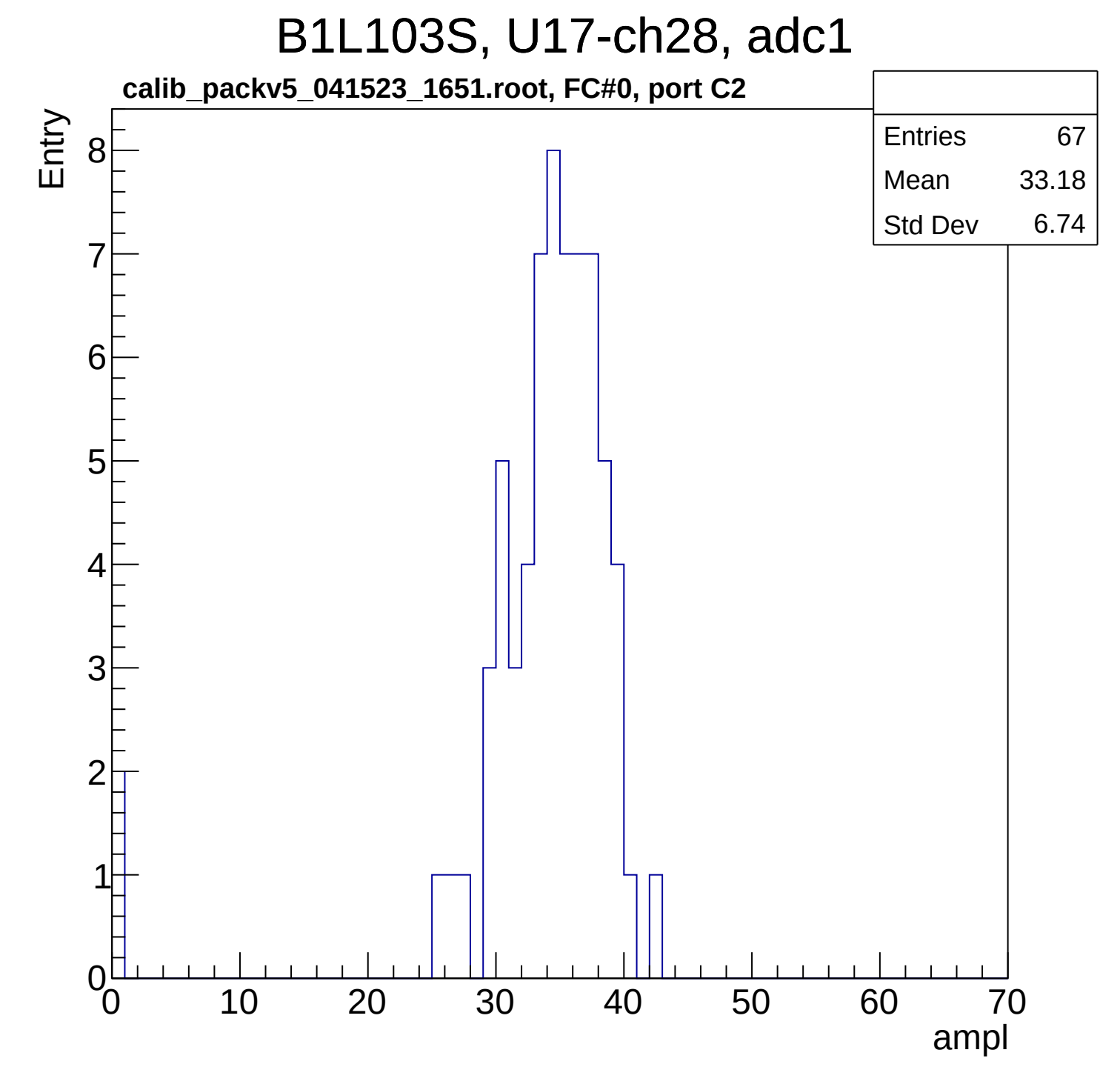
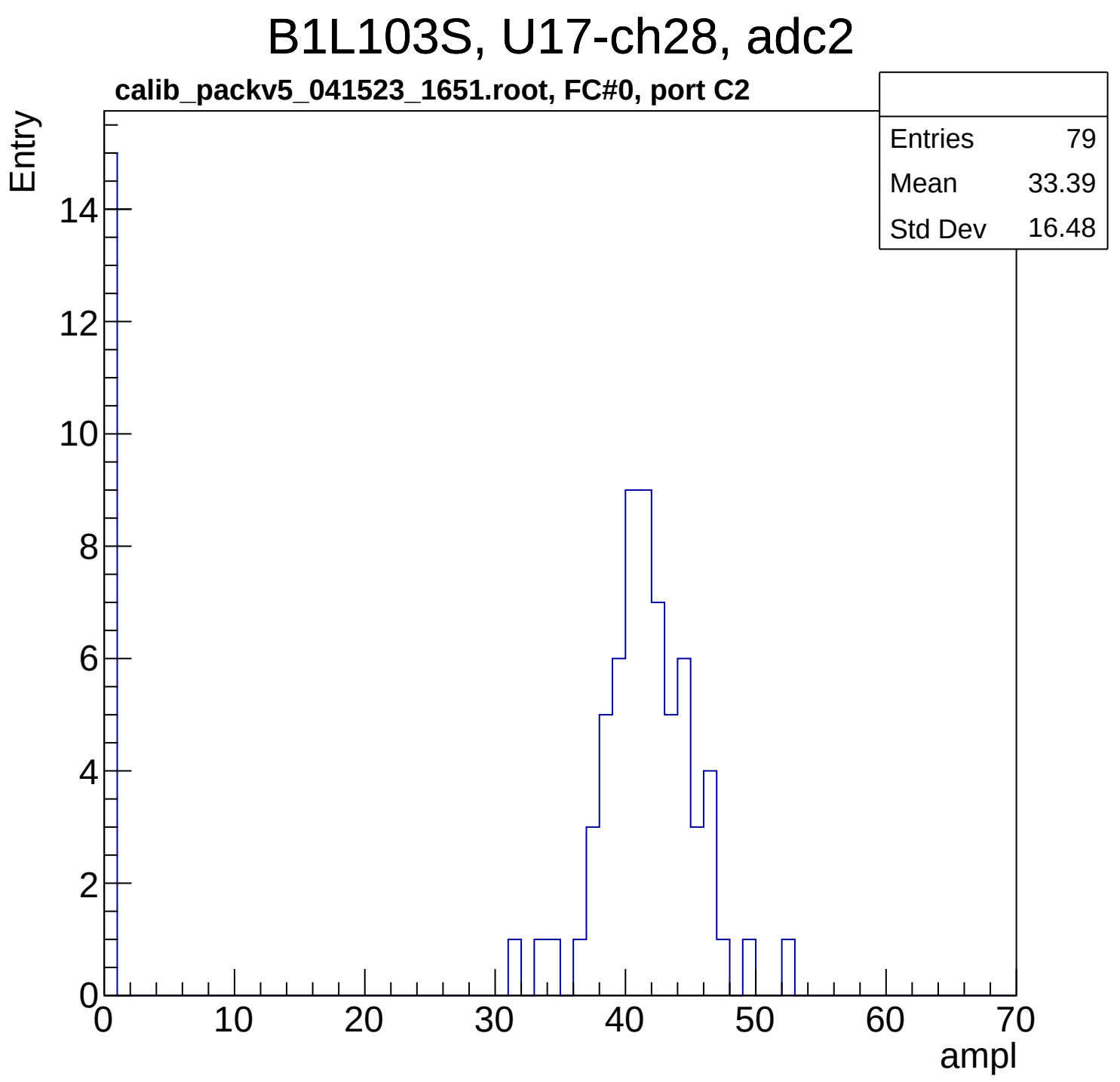
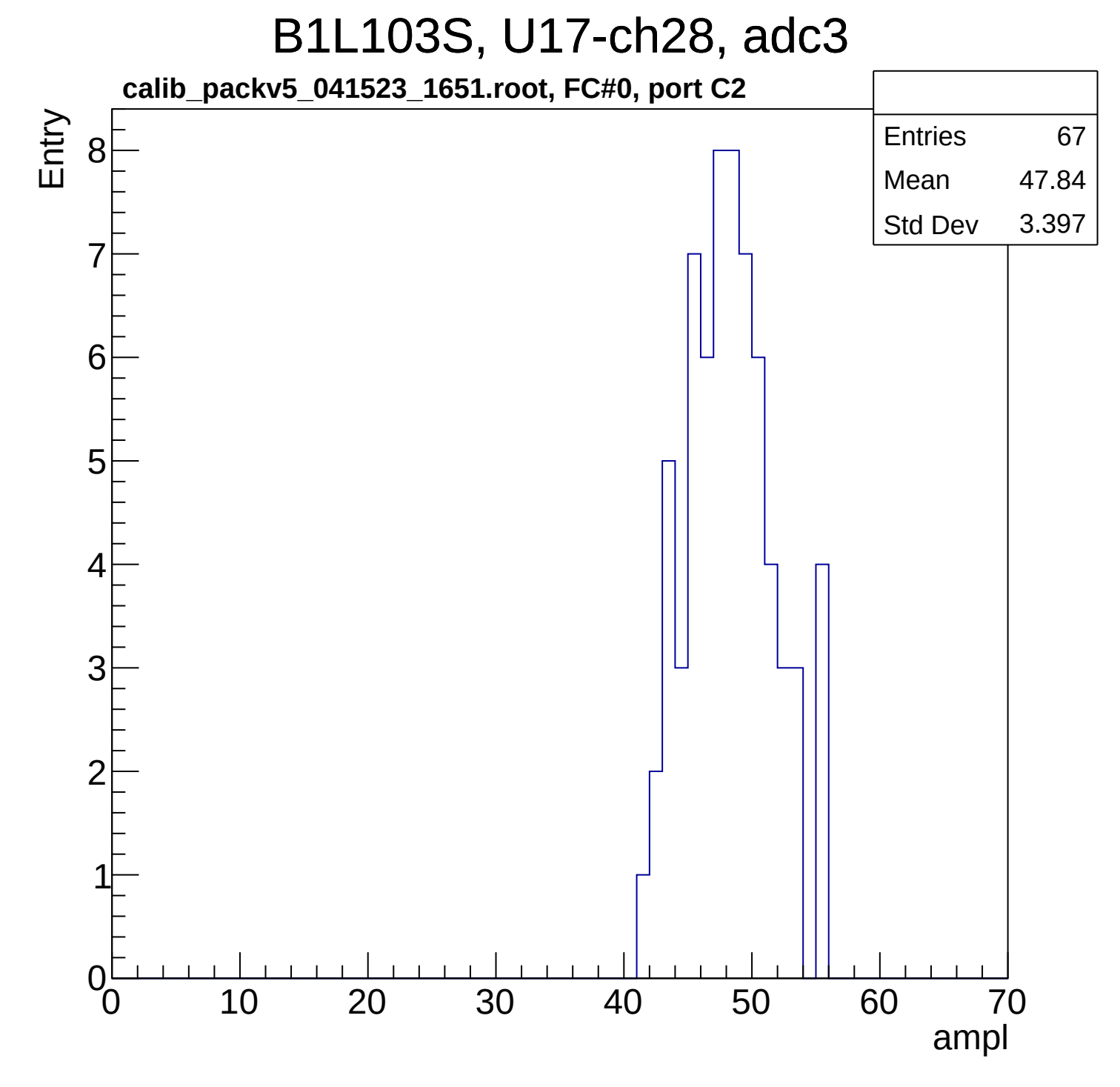

B1L103S, U17-ch27, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch28, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 24.35
Std Dev 10.01
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch28, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 33.18
Std Dev 6.74
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U17-ch28, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 33.39
Std Dev 16.48
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch28, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 47.84
Std Dev 3.397
Entry
ampl
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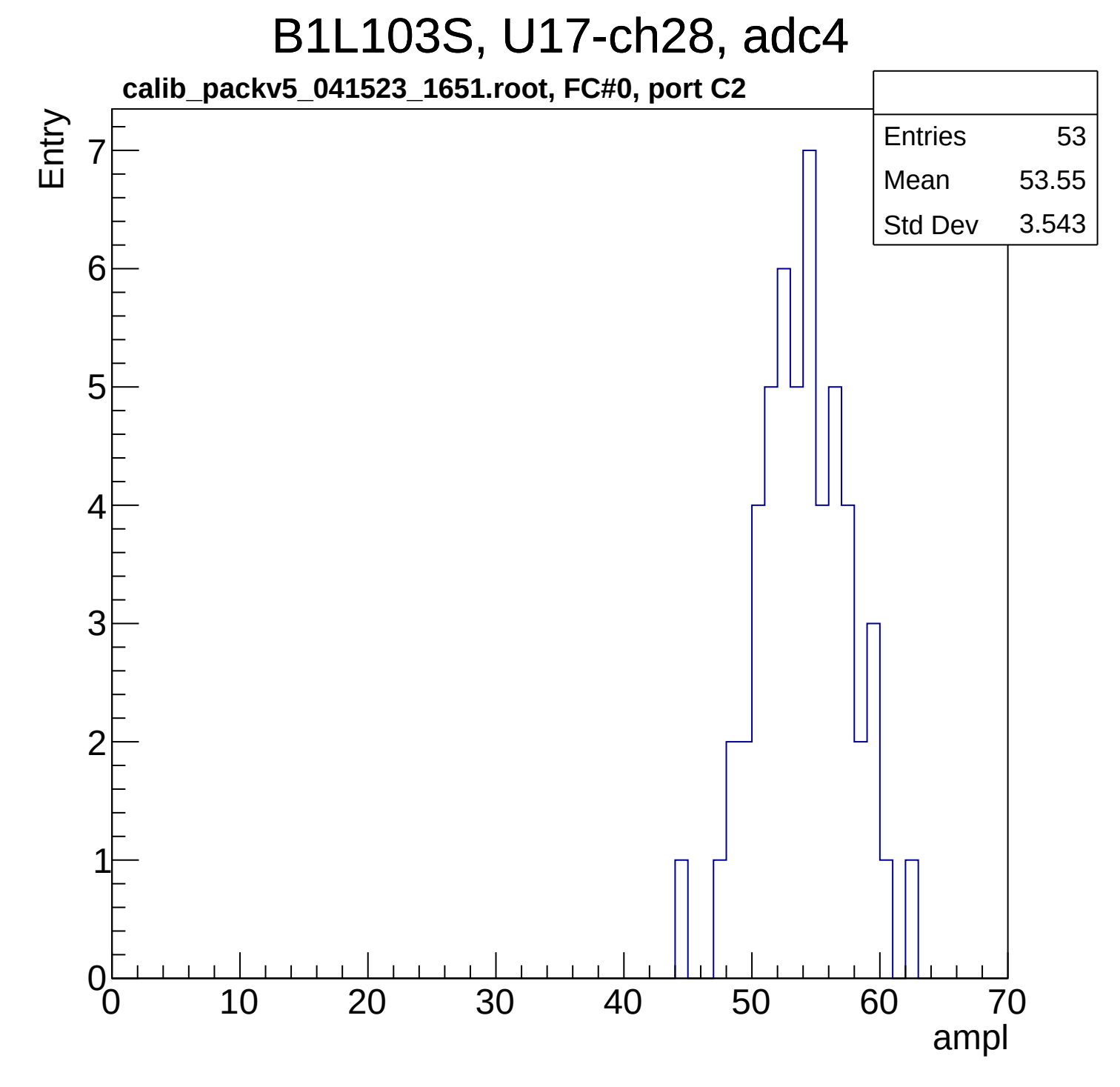
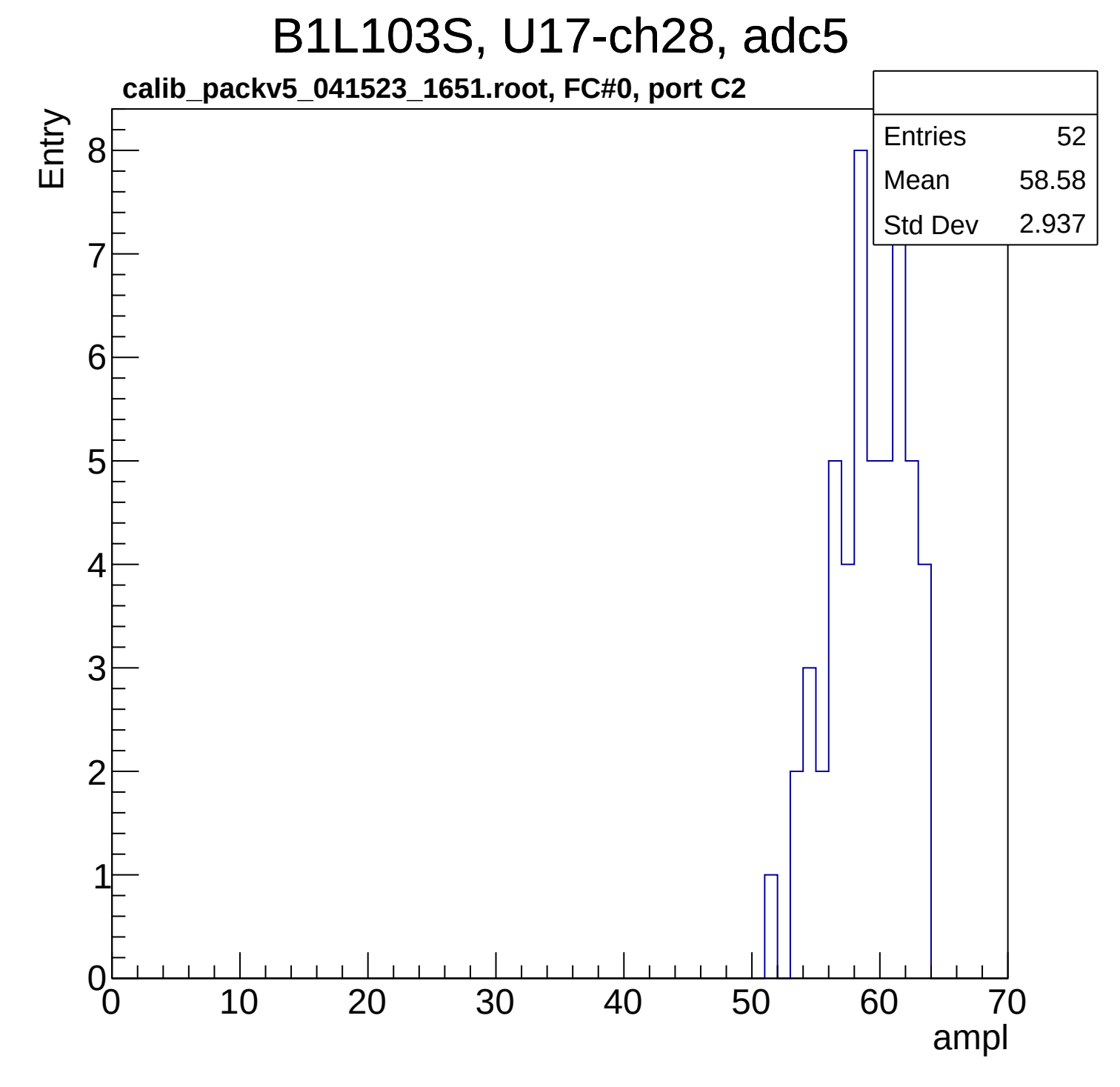
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U17-ch28, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 53.55
Std Dev 3.543
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U17-ch28, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 58.58
Std Dev 2.937
Entry
ampl
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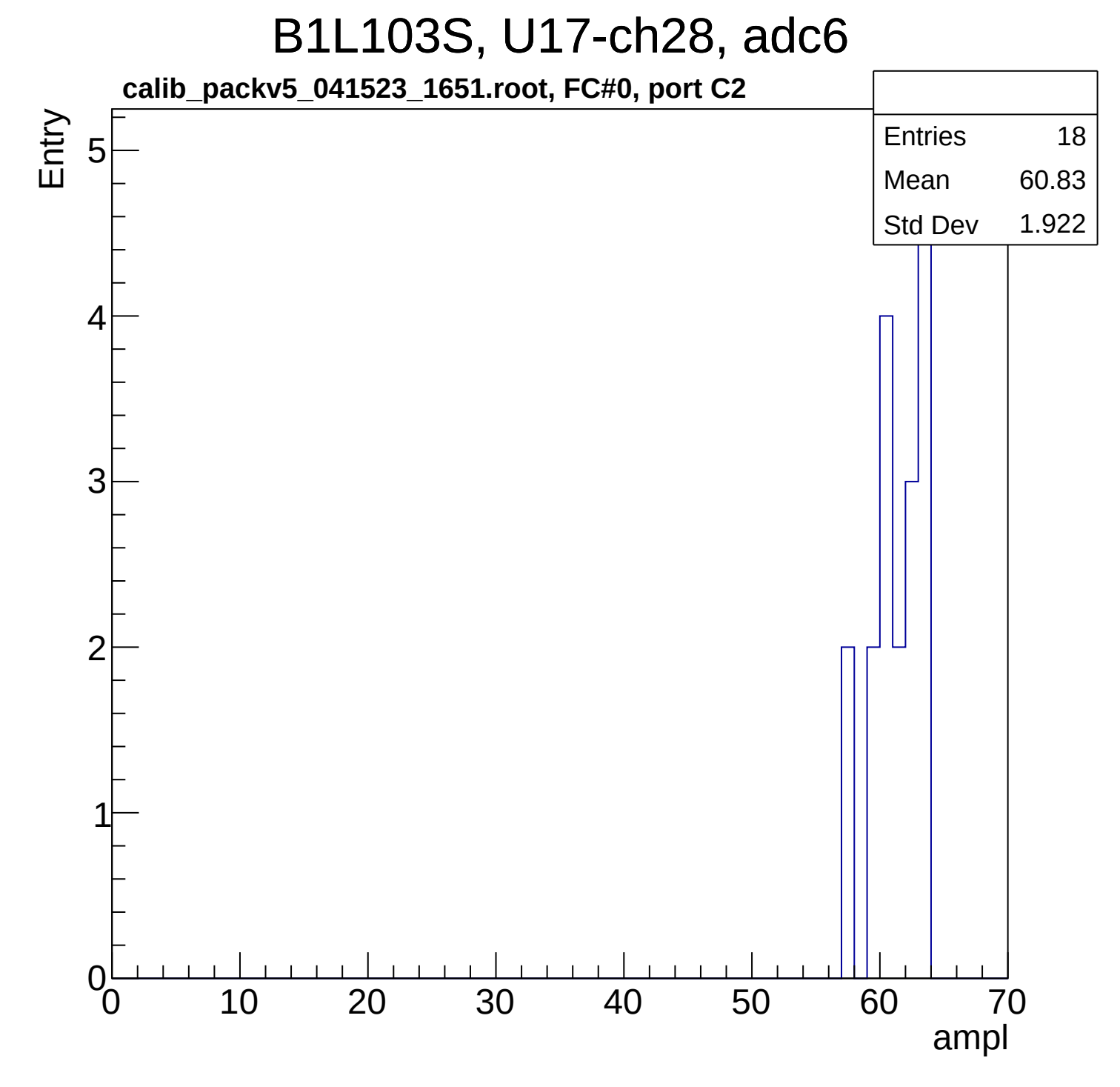
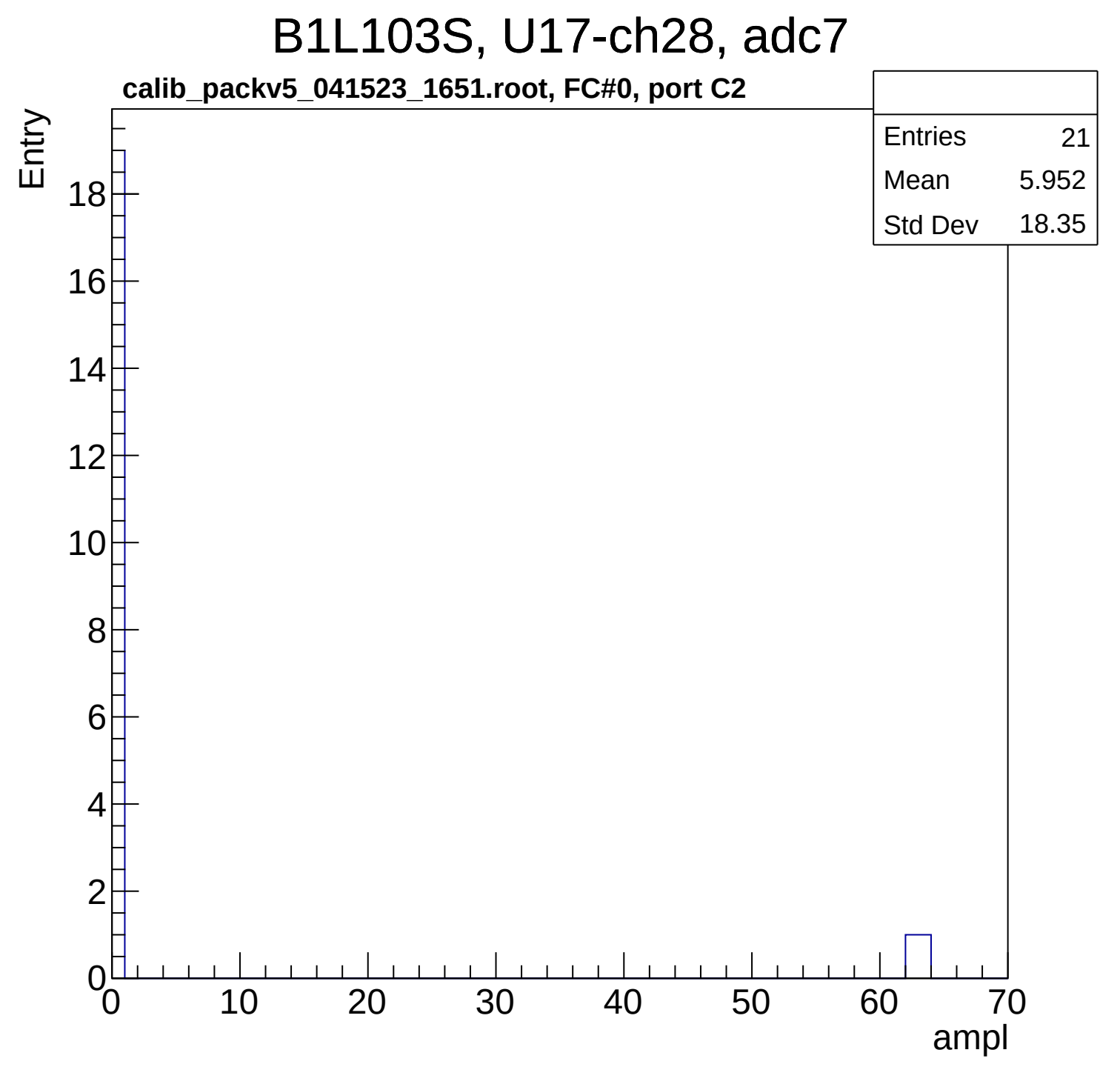
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U17-ch28, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 60.83
Std Dev 1.922
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U17-ch28, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 5.952
Std Dev 18.35
Entry
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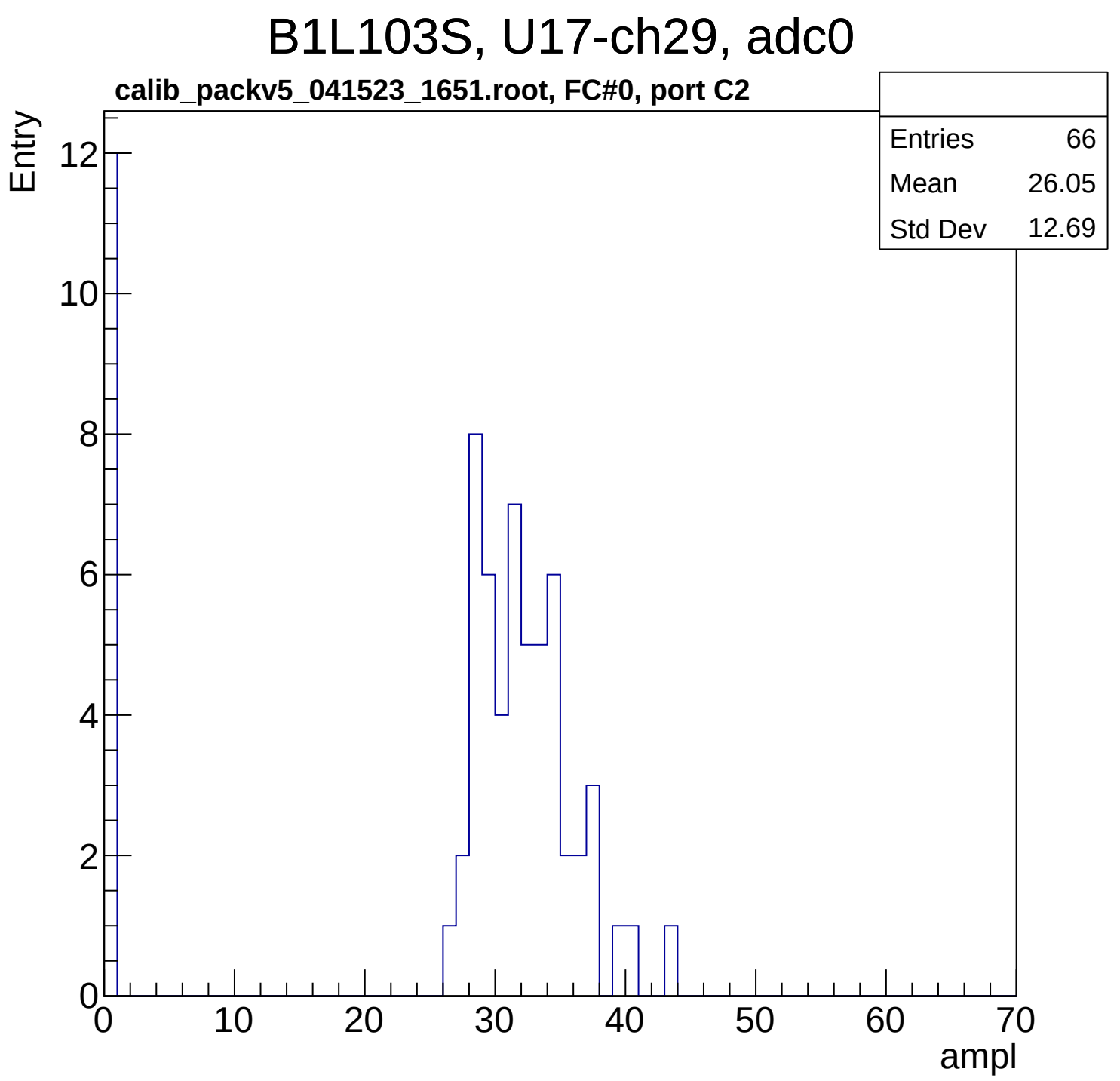
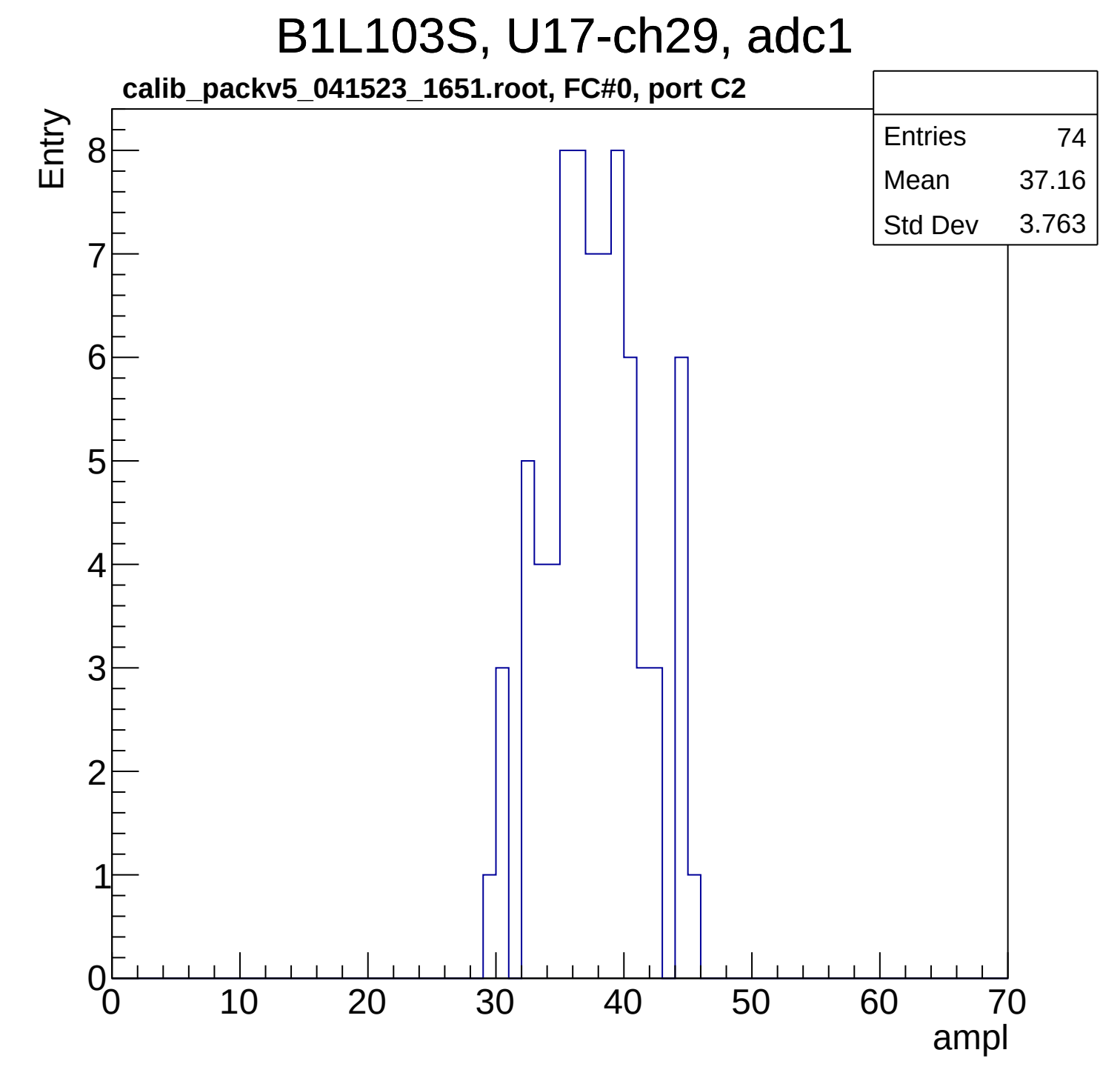
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch29, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 26.05
Std Dev 12.69
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch29, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 37.16
Std Dev 3.763
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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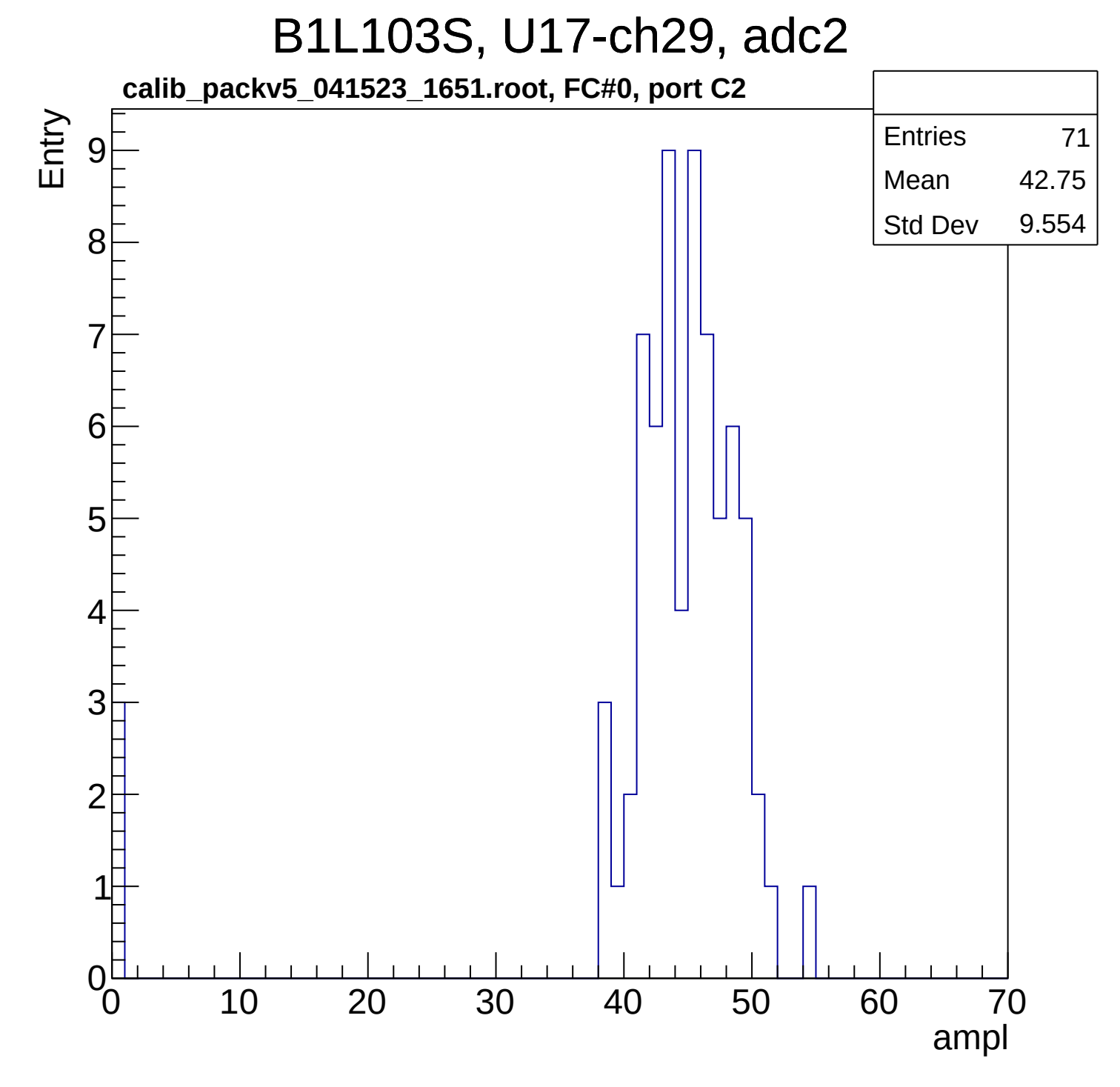
B1L103S, U17-ch29, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 42.75
Std Dev 9.554
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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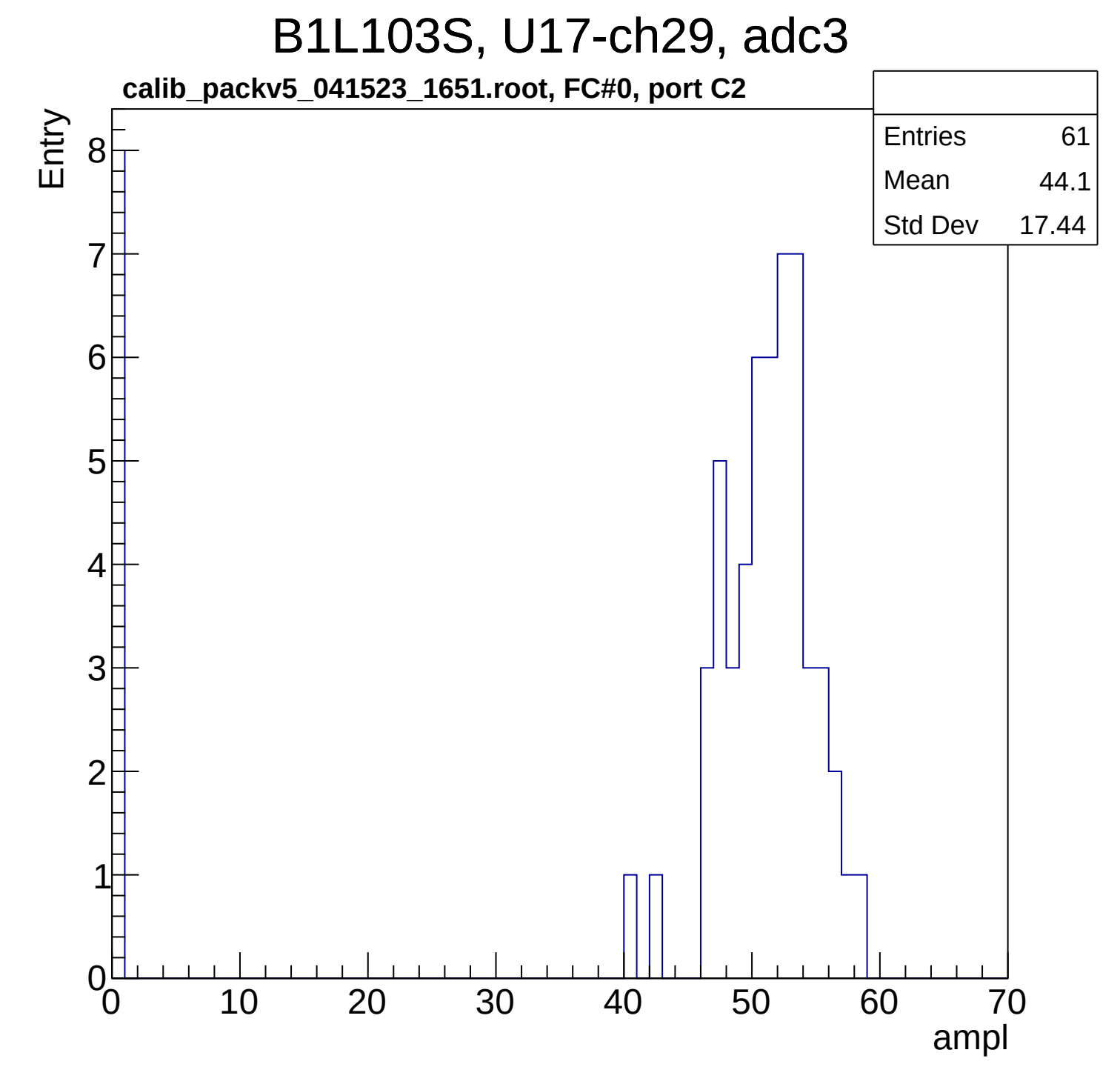
B1L103S, U17-ch29, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 44.1
Std Dev 17.44
Entry
ampl
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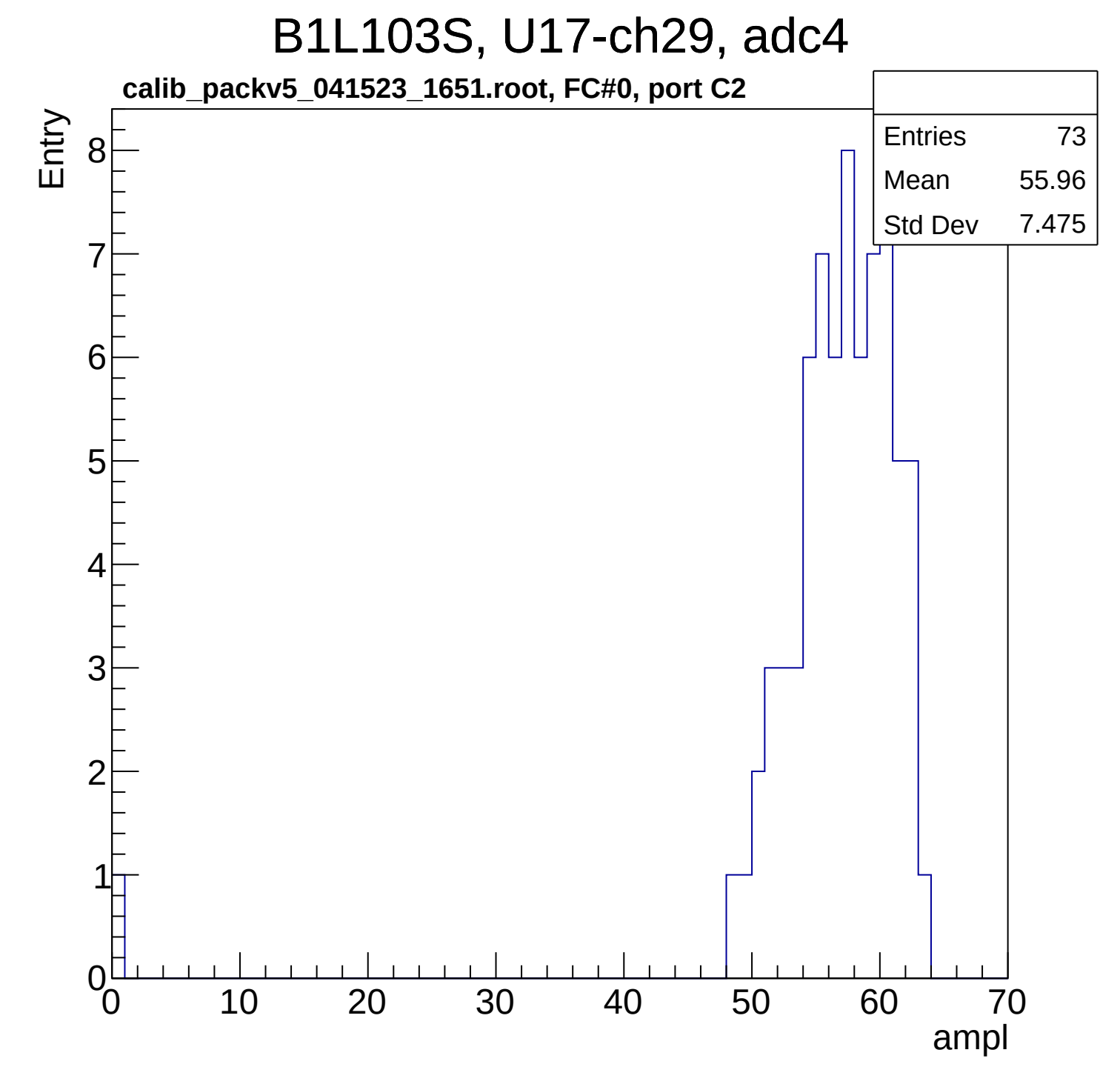
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U17-ch29, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 55.96
Std Dev 7.475
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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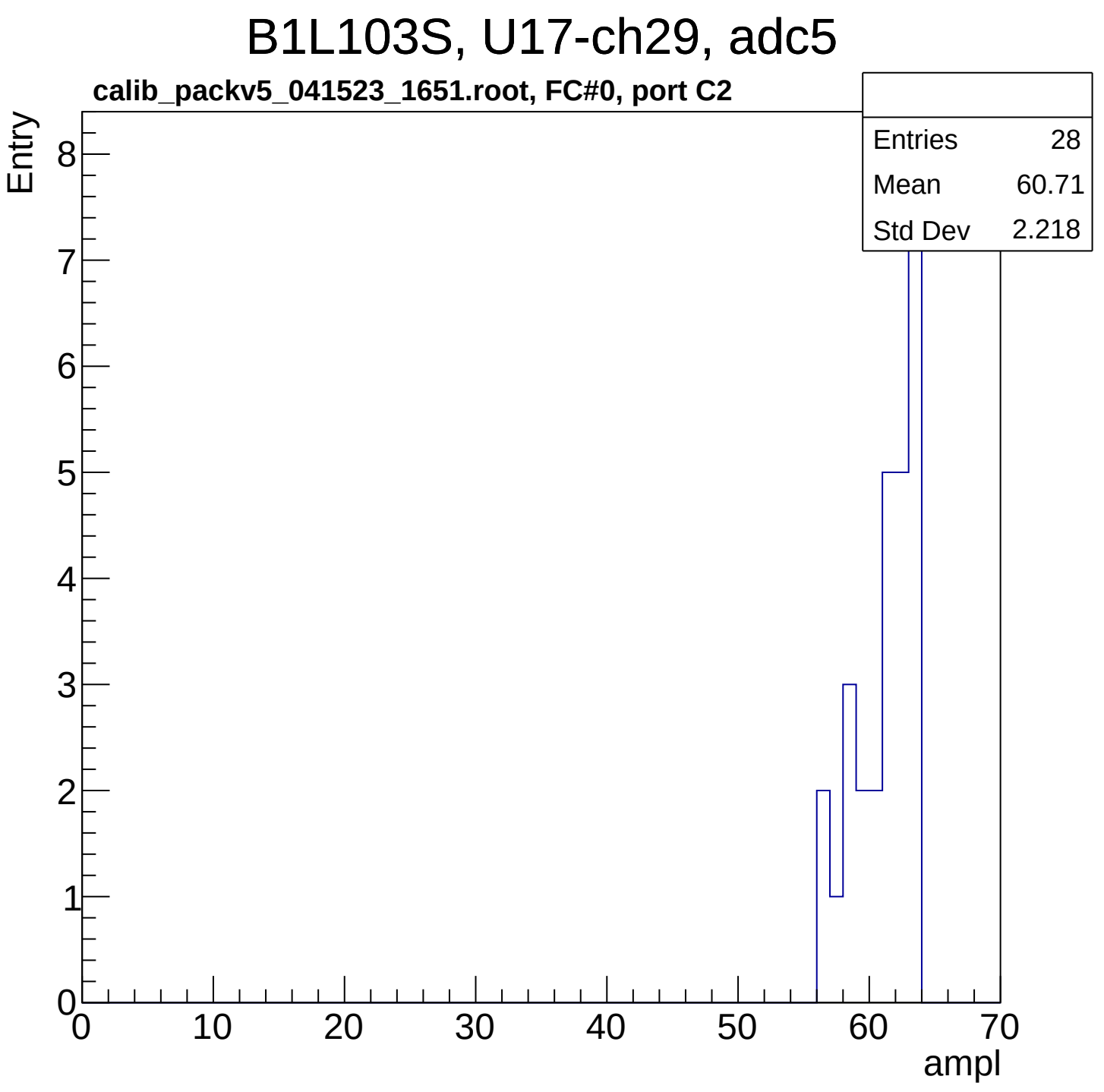
B1L103S, U17-ch29, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 28
Mean 60.71
Std Dev 2.218
Entry
ampl
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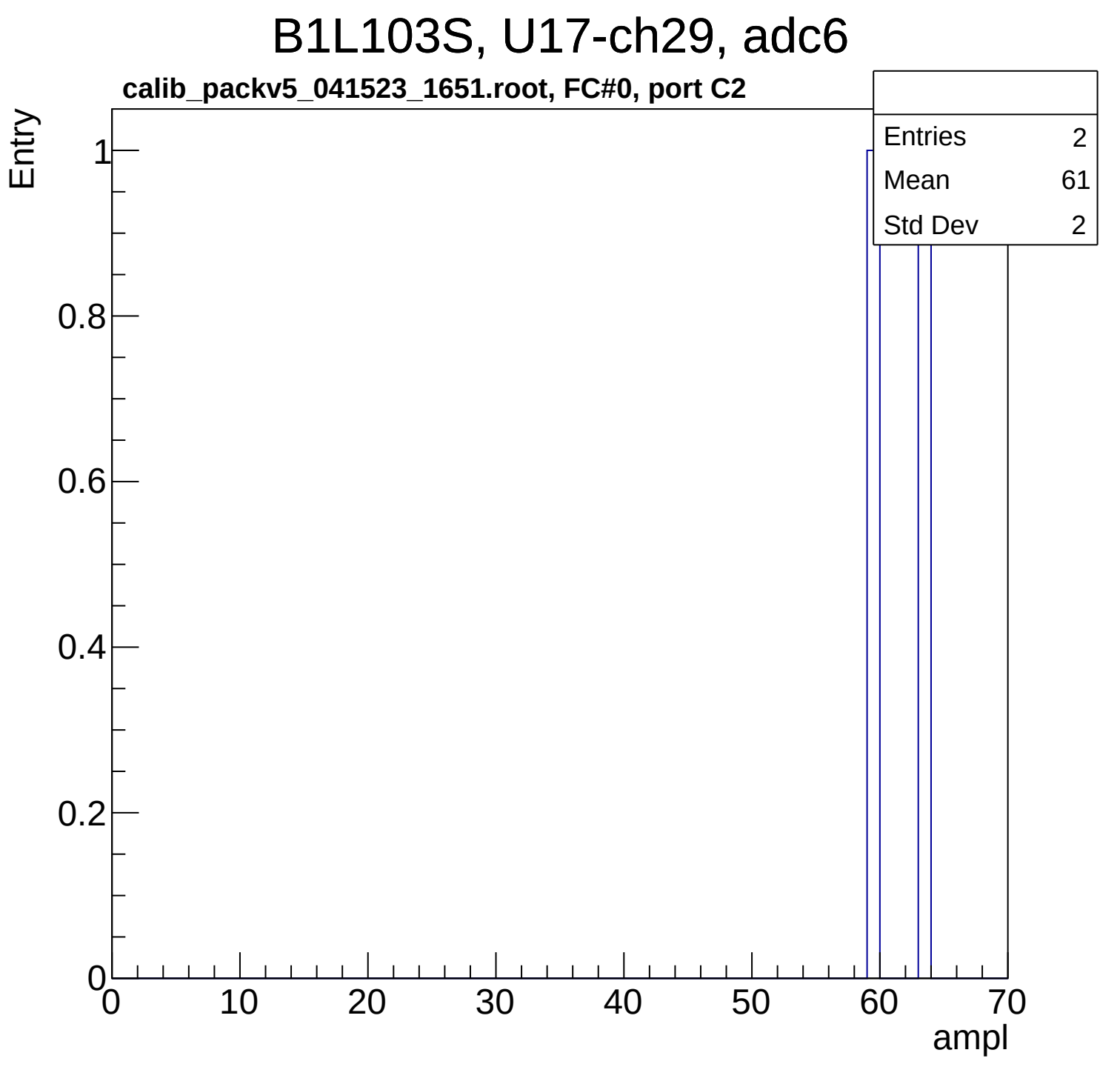
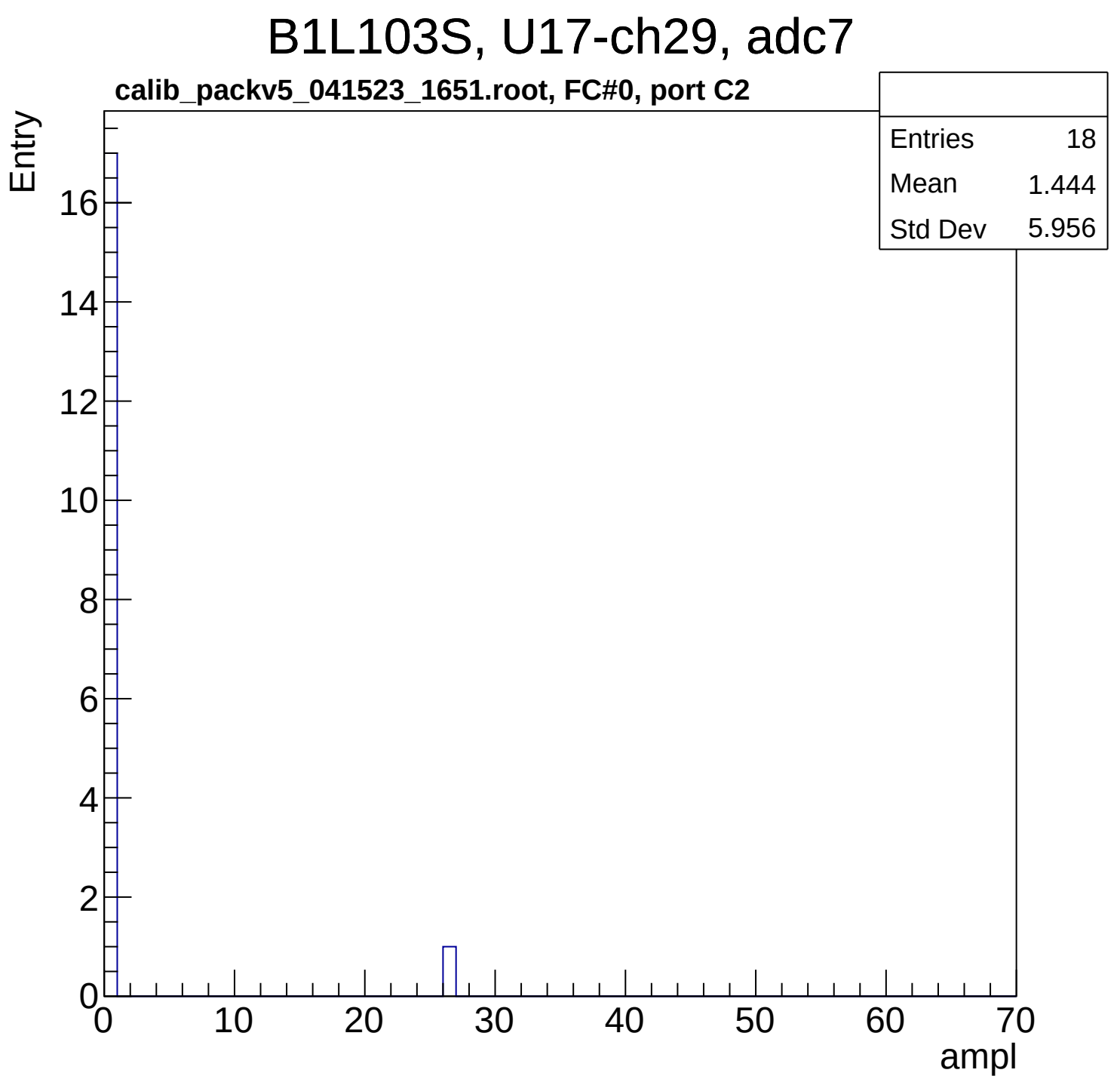
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U17-ch29, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 2
Mean 61
Std Dev 2
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch29, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 1.444
Std Dev 5.956
Entry
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4
6
8
10
12
14
16
0
10
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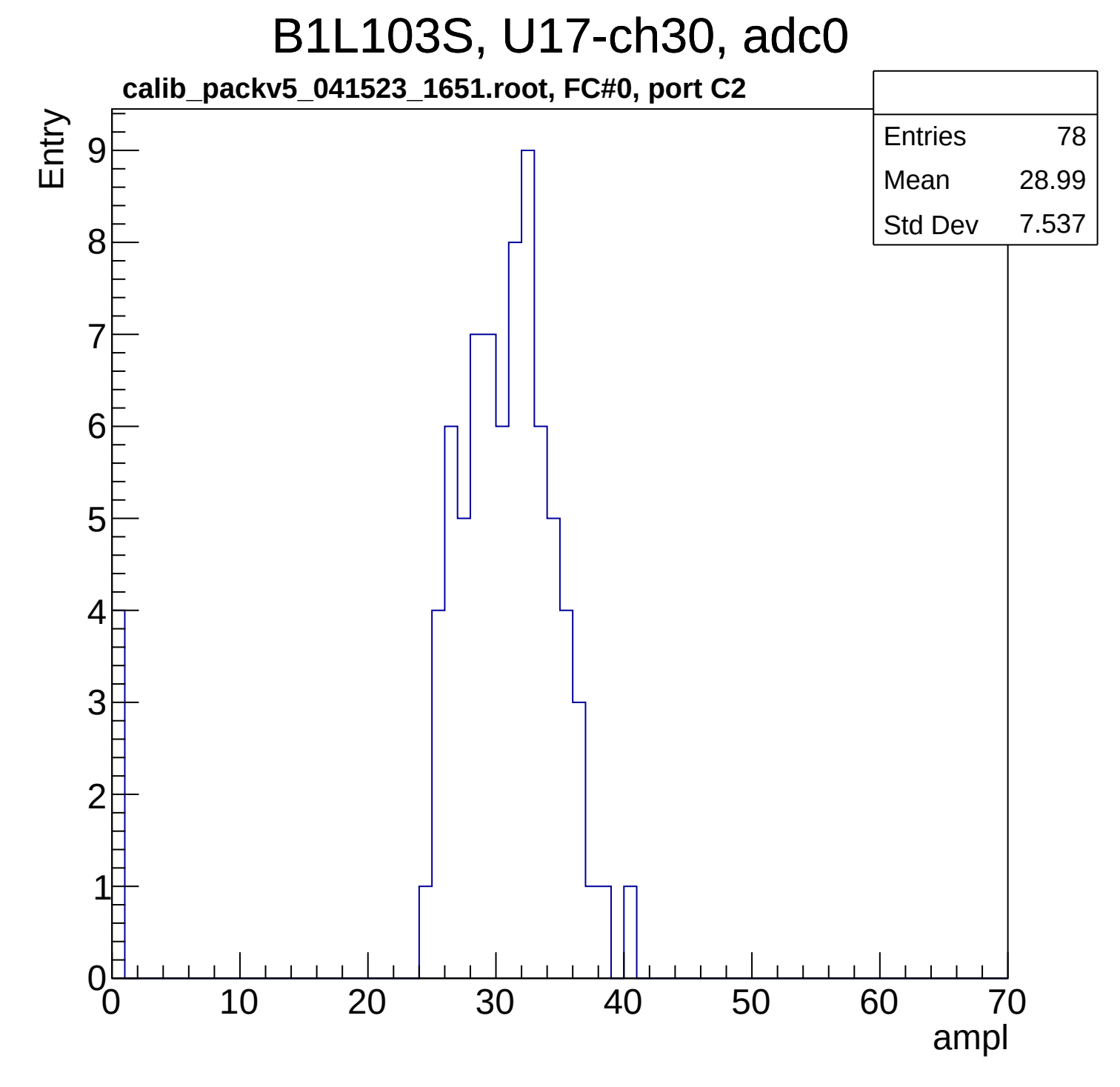
30
40
50
60
70
ampl


B1L103S, U17-ch30, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 28.99
Std Dev 7.537
Entry
ampl
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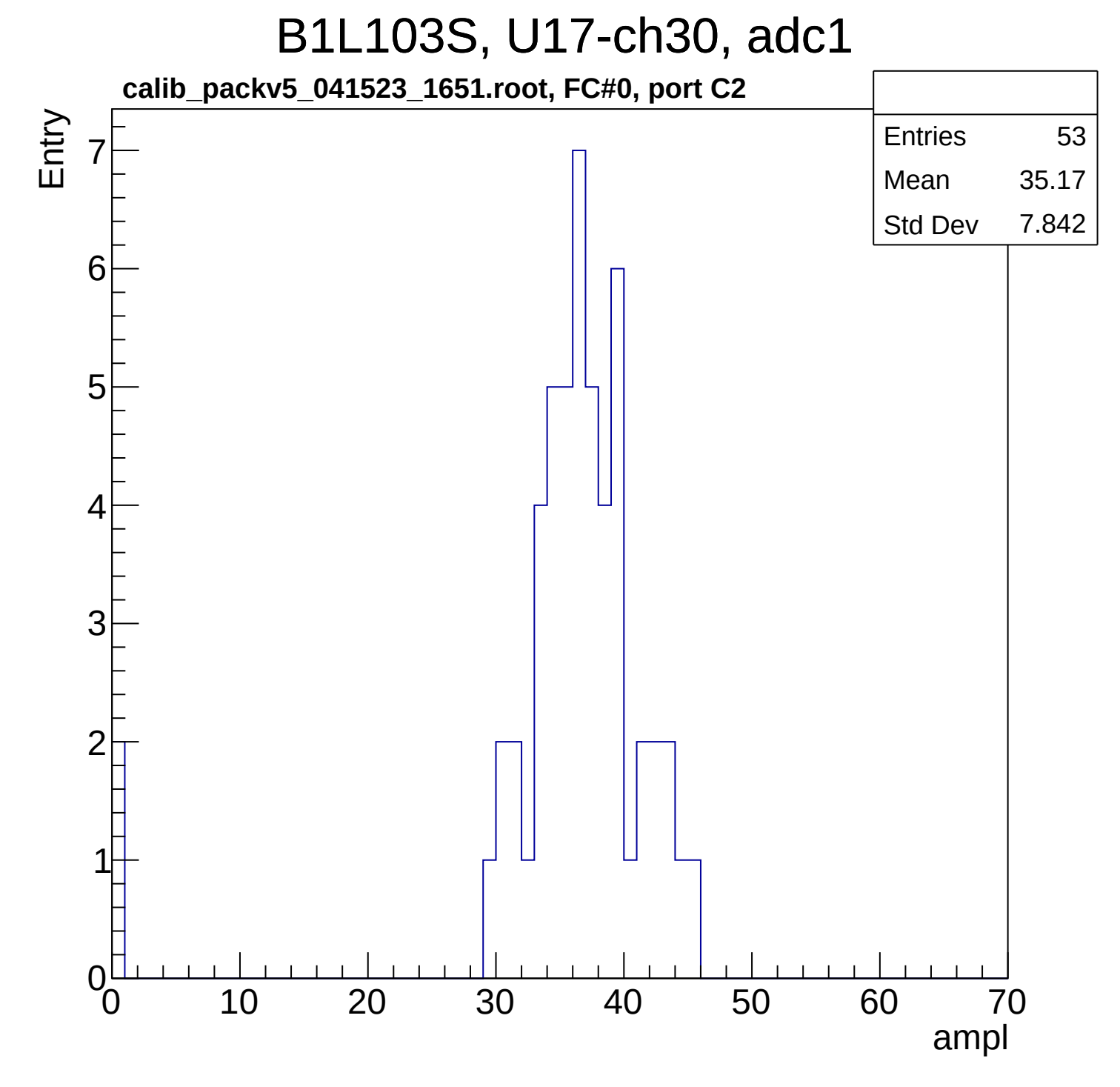
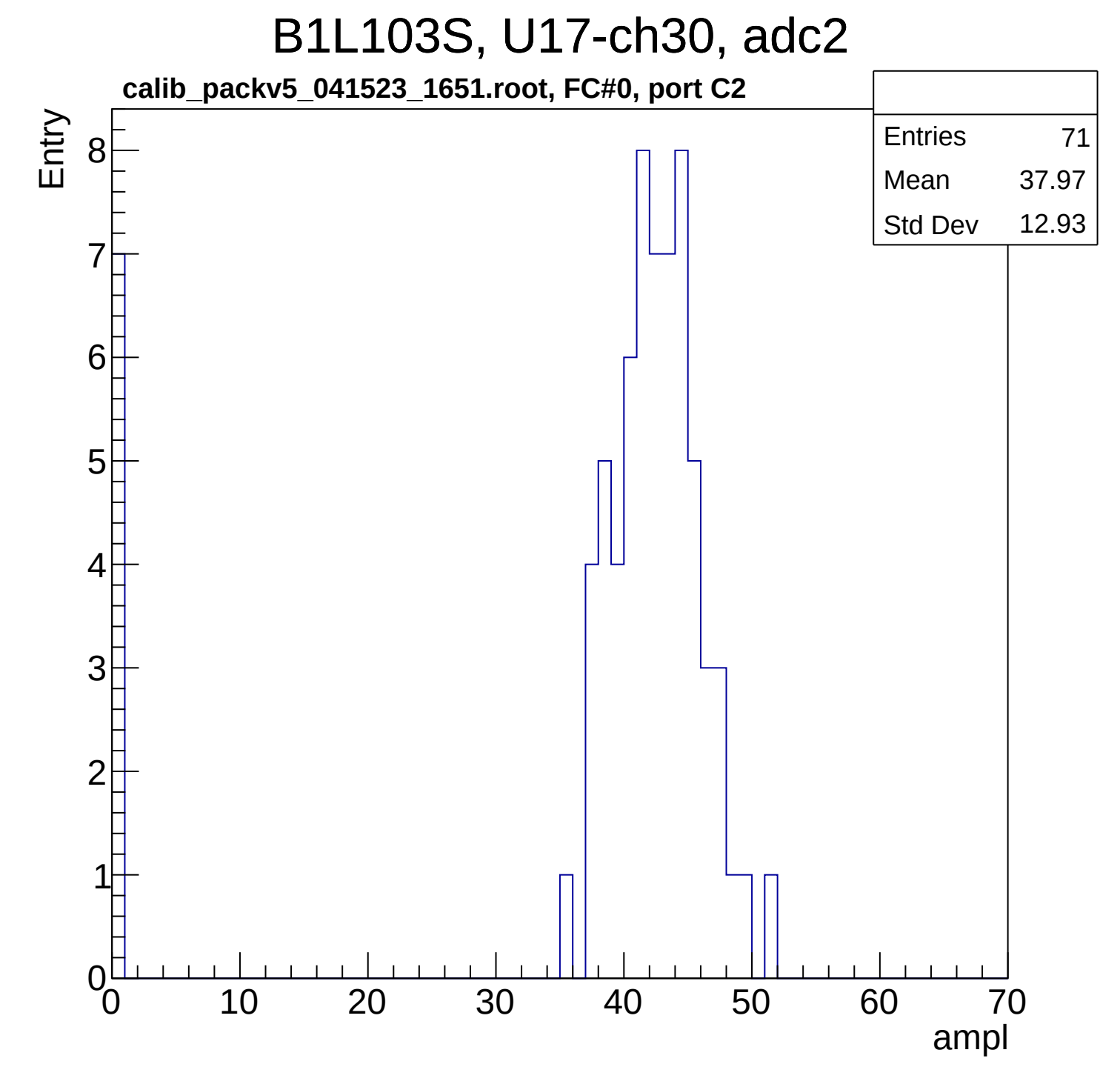
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U17-ch30, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 35.17
Std Dev 7.842
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U17-ch30, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 37.97
Std Dev 12.93
Entry
ampl
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2
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4
5
6
7
8
0
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20
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40
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60
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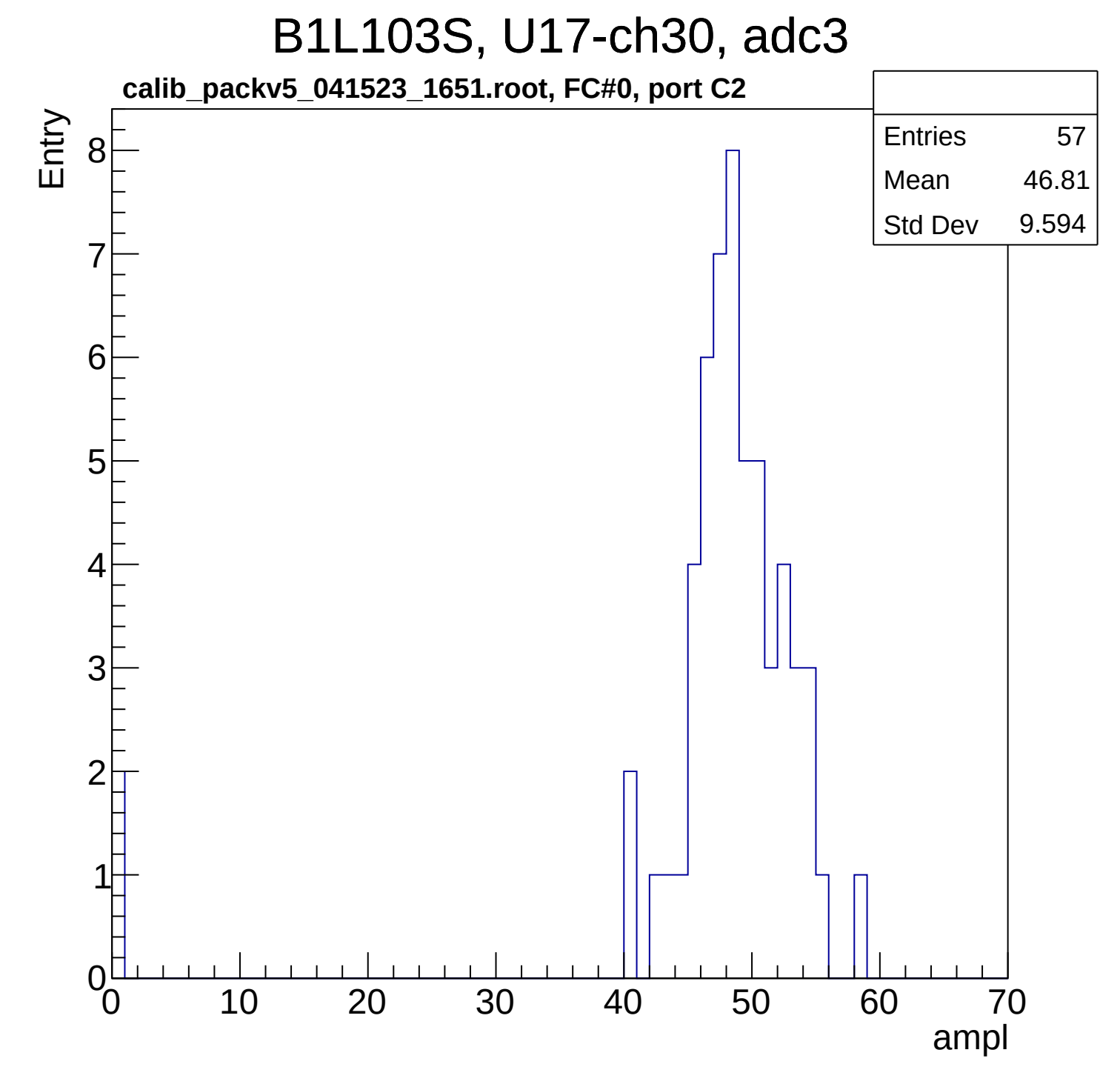
B1L103S, U17-ch30, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 46.81
Std Dev 9.594
Entry
ampl
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2
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4
5
6
7
8
0
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20
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40
50
60
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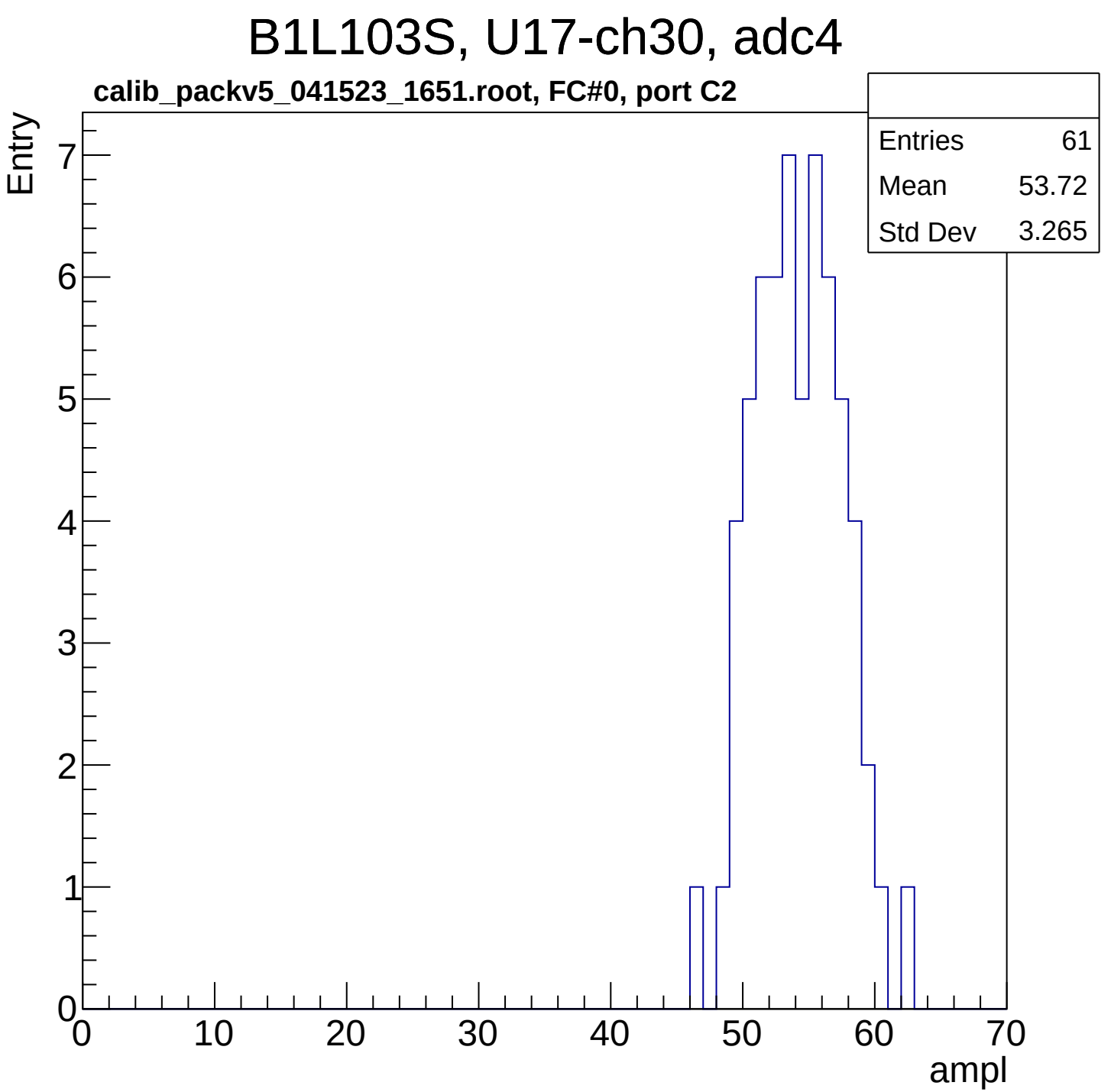
B1L103S, U17-ch30, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 53.72
Std Dev 3.265
Entry
ampl
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1
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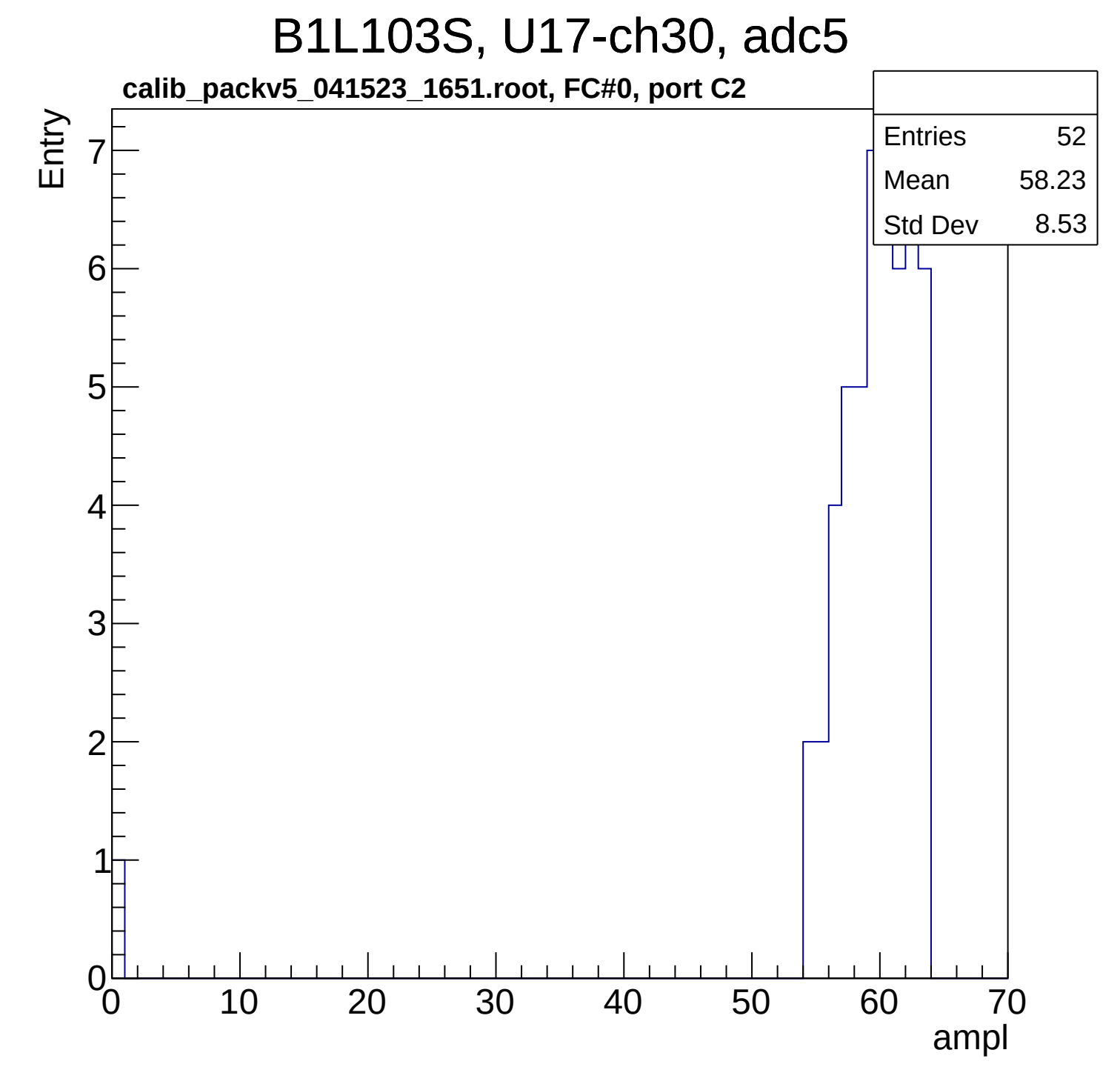
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U17-ch30, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 58.23
Std Dev 8.53
Entry
ampl
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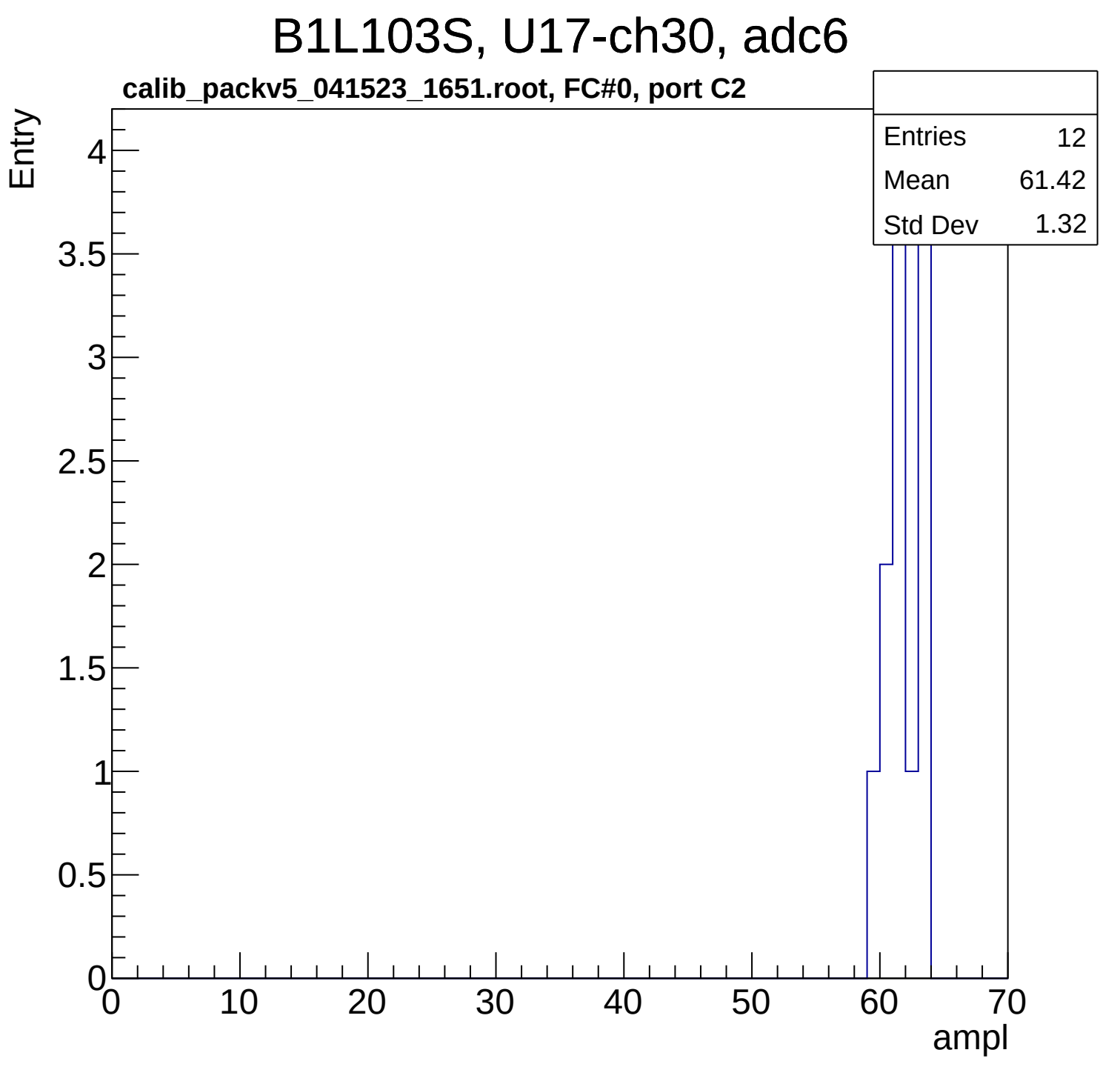
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U17-ch30, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 61.42
Std Dev 1.32
Entry
ampl
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0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
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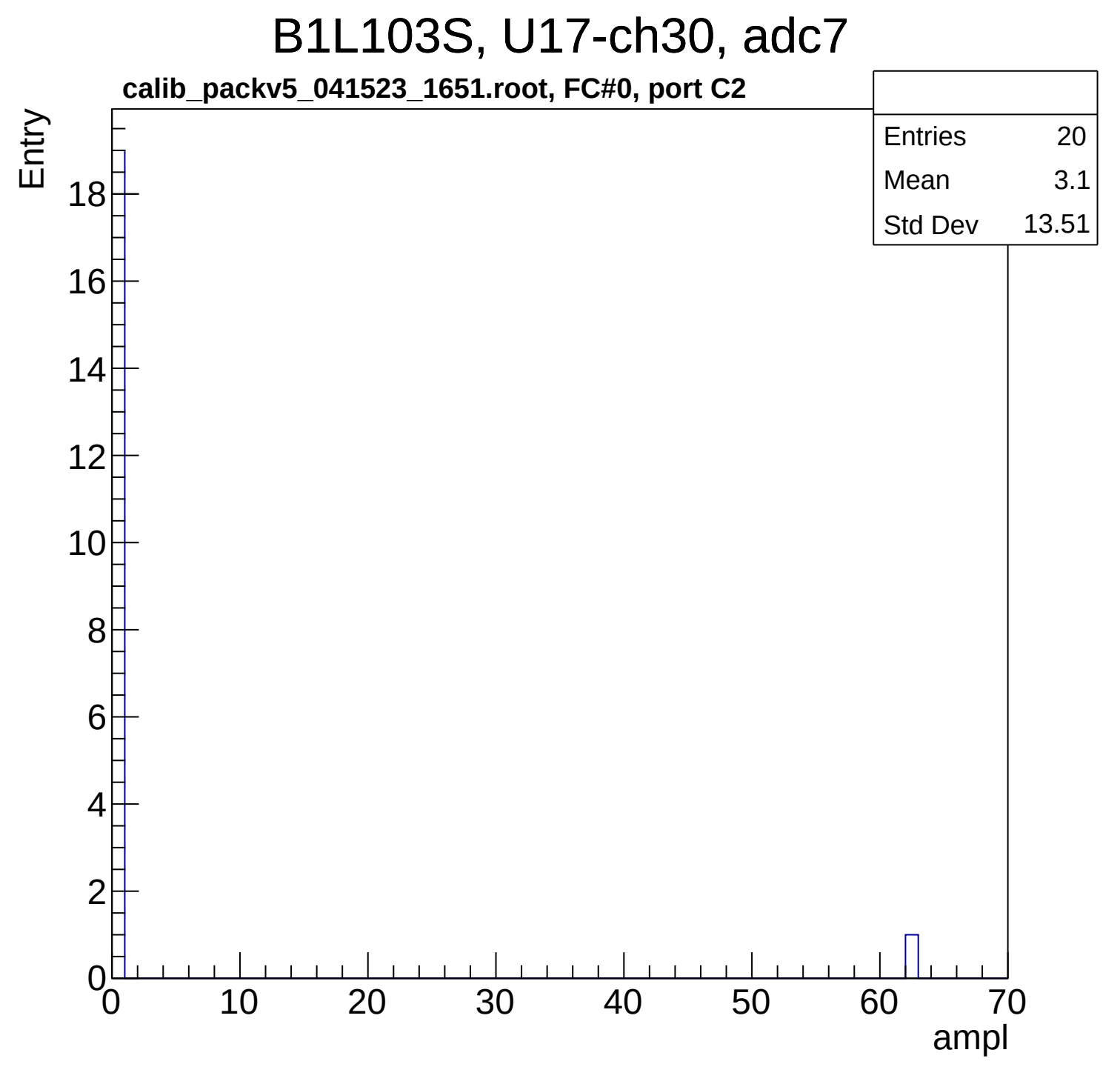
40
50
60
70


B1L103S, U17-ch30, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.1
Std Dev 13.51
Entry
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6
8
10
12
14
16
18
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10
20
30
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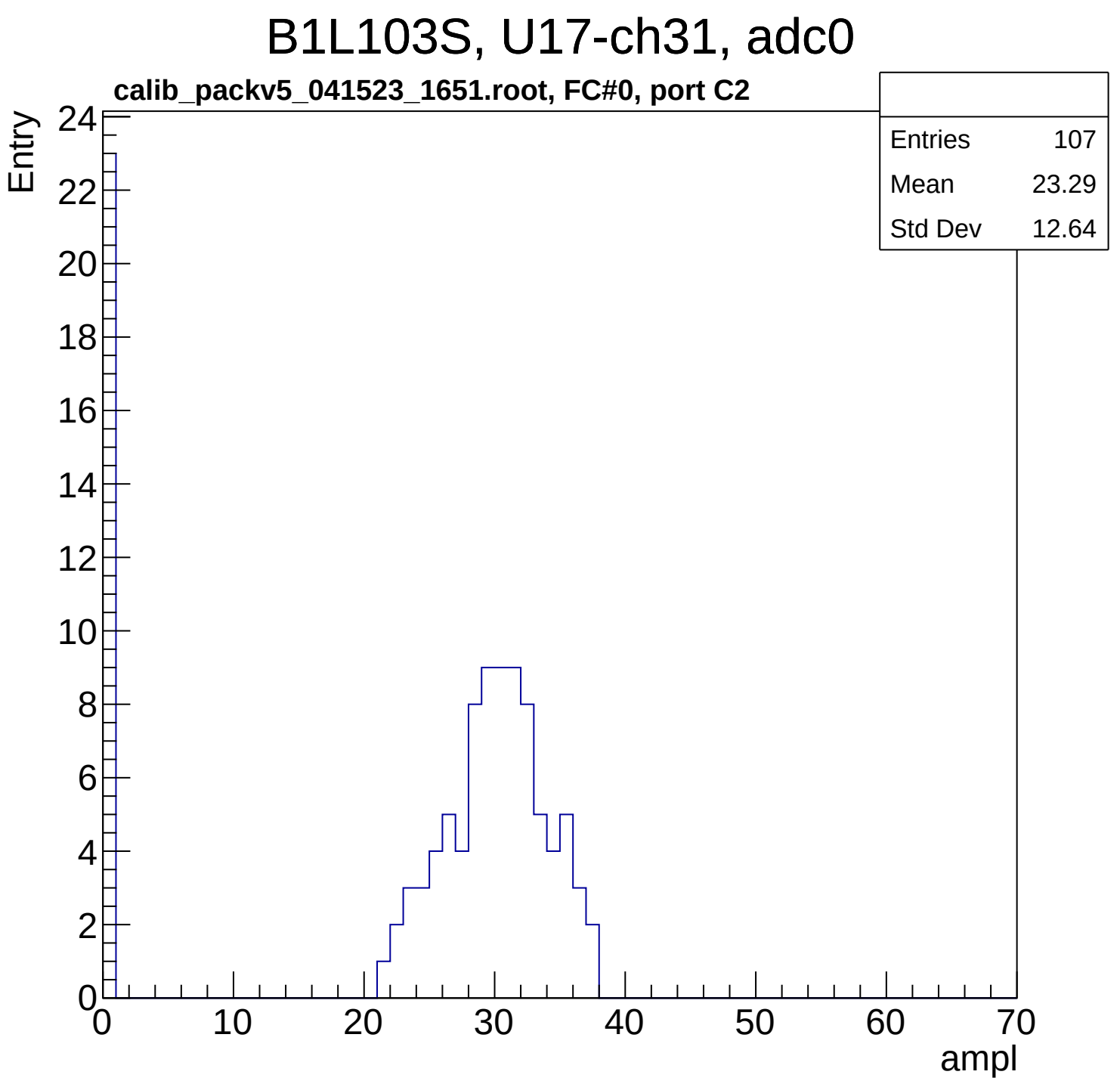
50
60
70
ampl


B1L103S, U17-ch31, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 107
Mean 23.29
Std Dev 12.64
Entry
ampl
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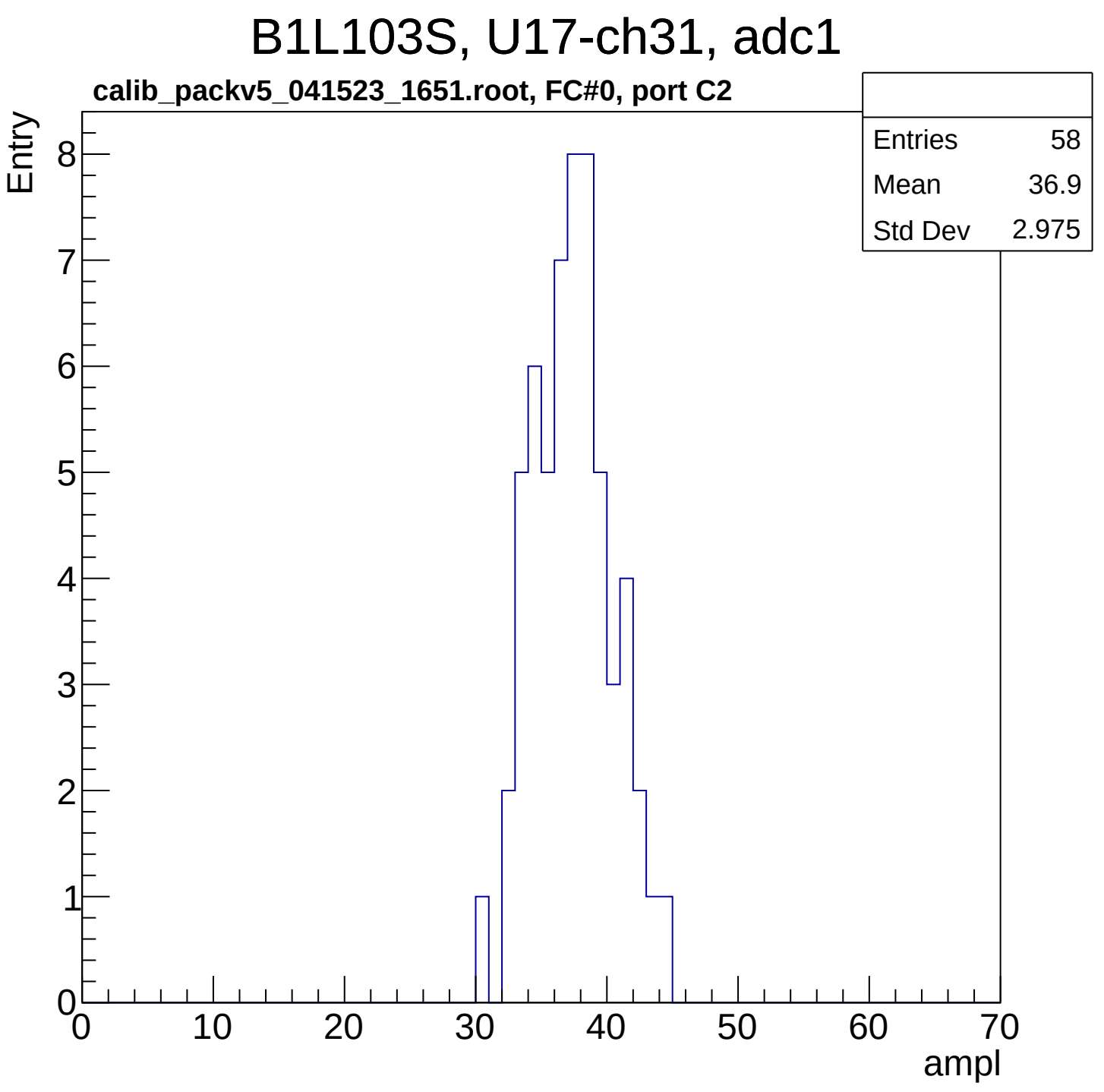
8
10
12
14
16
18
20
22
24
0
10
20
30
40
50
60
70


B1L103S, U17-ch31, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 36.9
Std Dev 2.975
Entry
ampl
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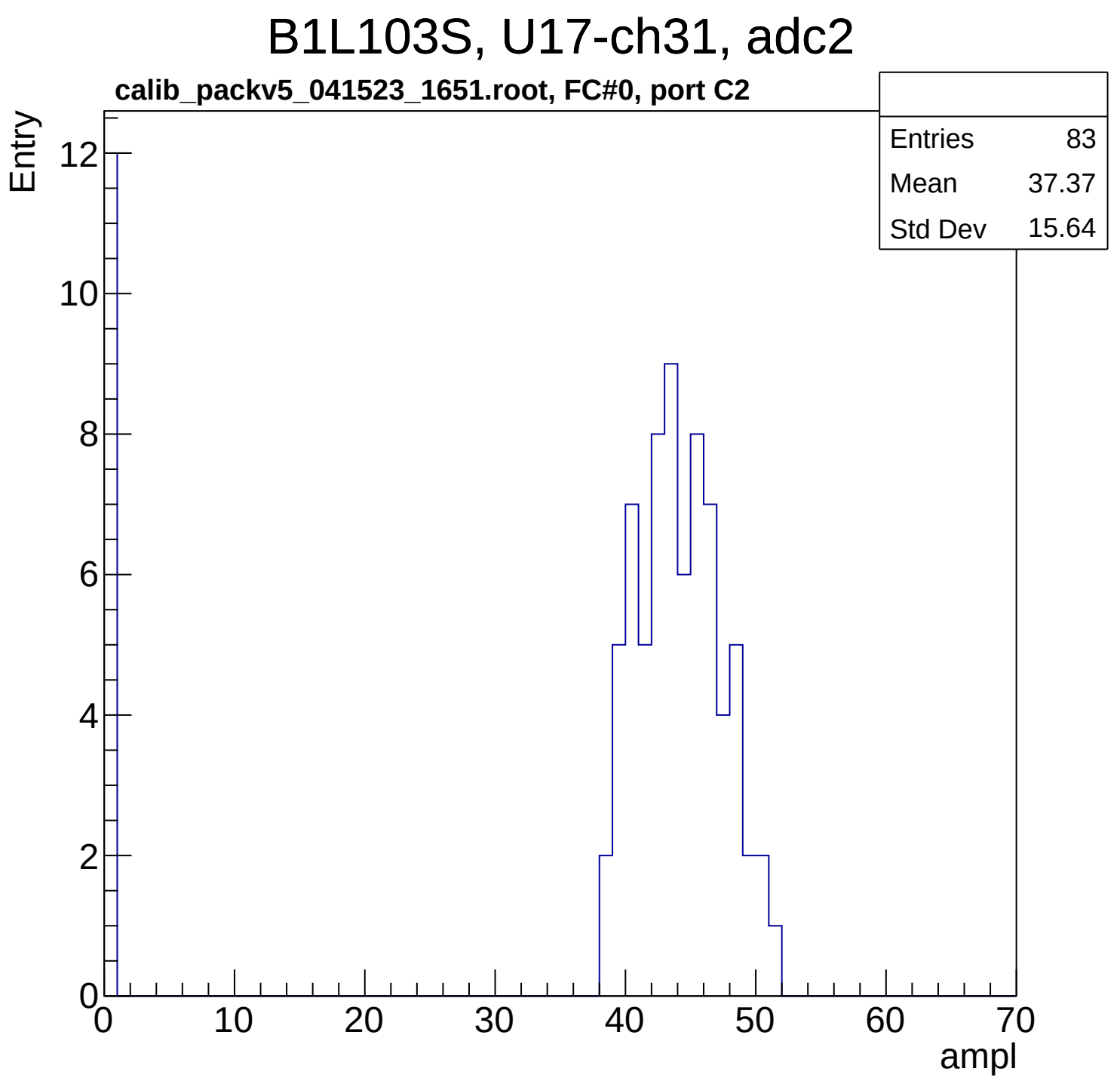
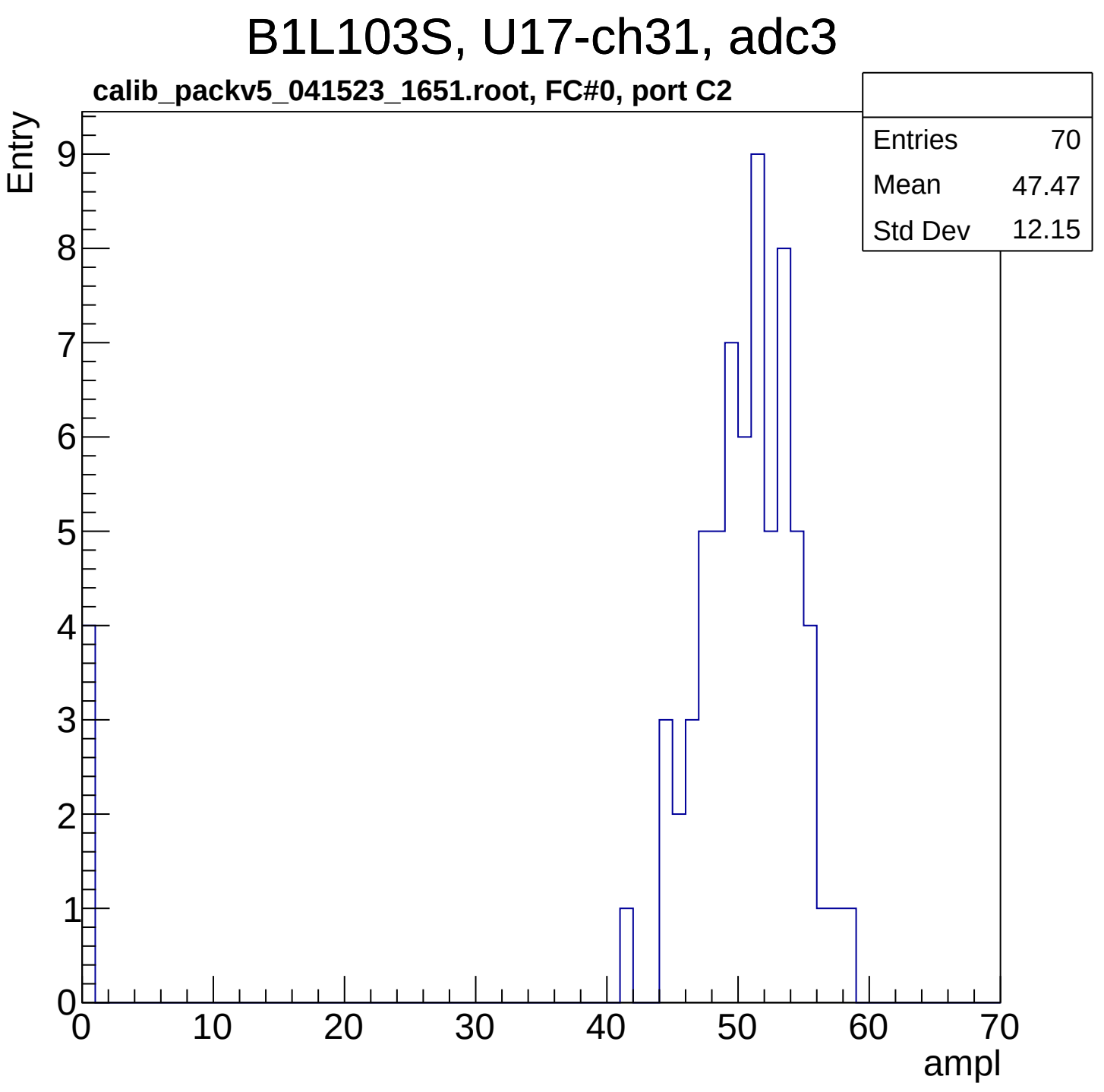
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U17-ch31, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 37.37
Std Dev 15.64
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch31, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 47.47
Std Dev 12.15
Entry
ampl
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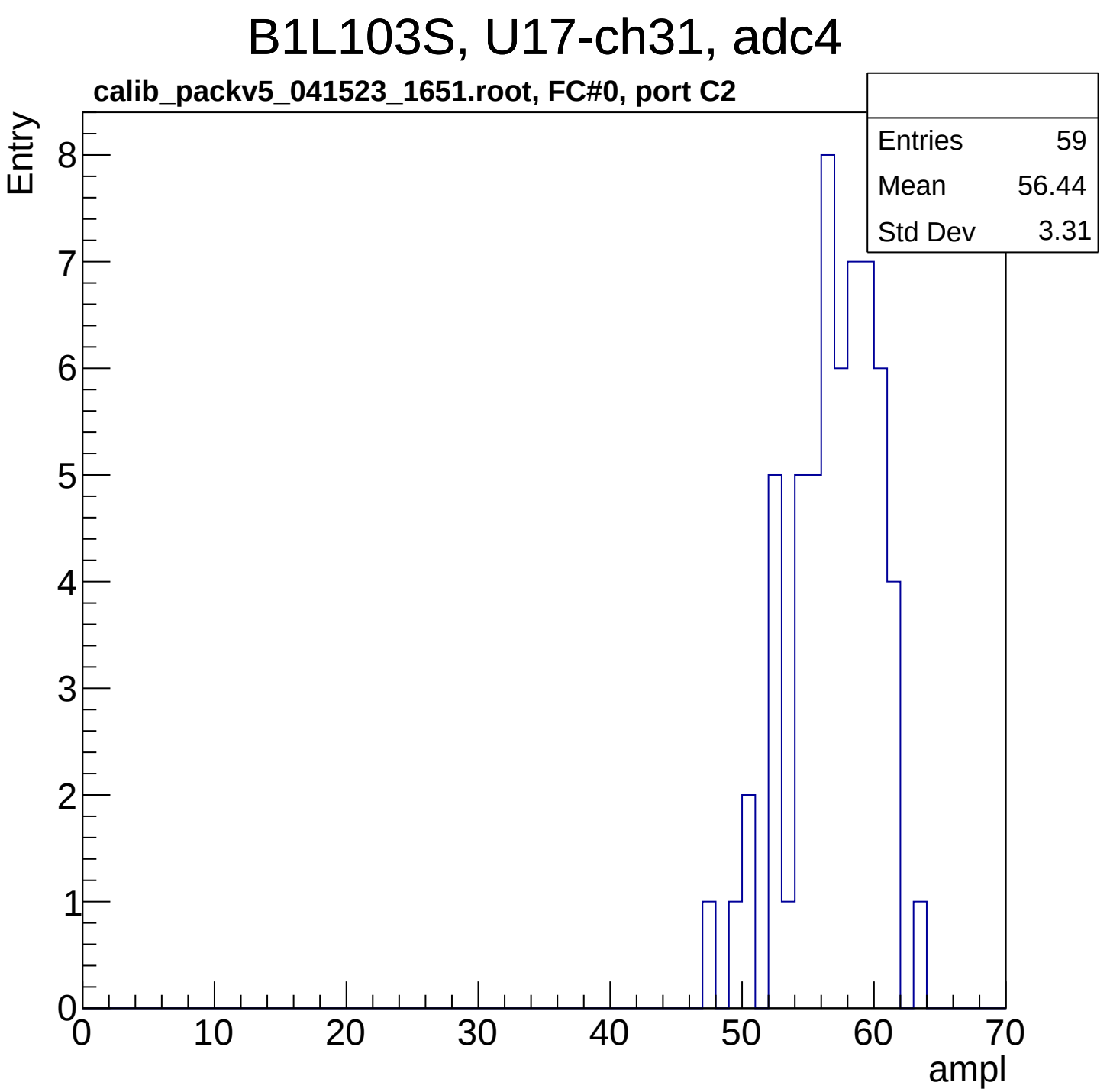
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U17-ch31, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 56.44
Std Dev 3.31
Entry
ampl
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1
2
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5
6
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0
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20
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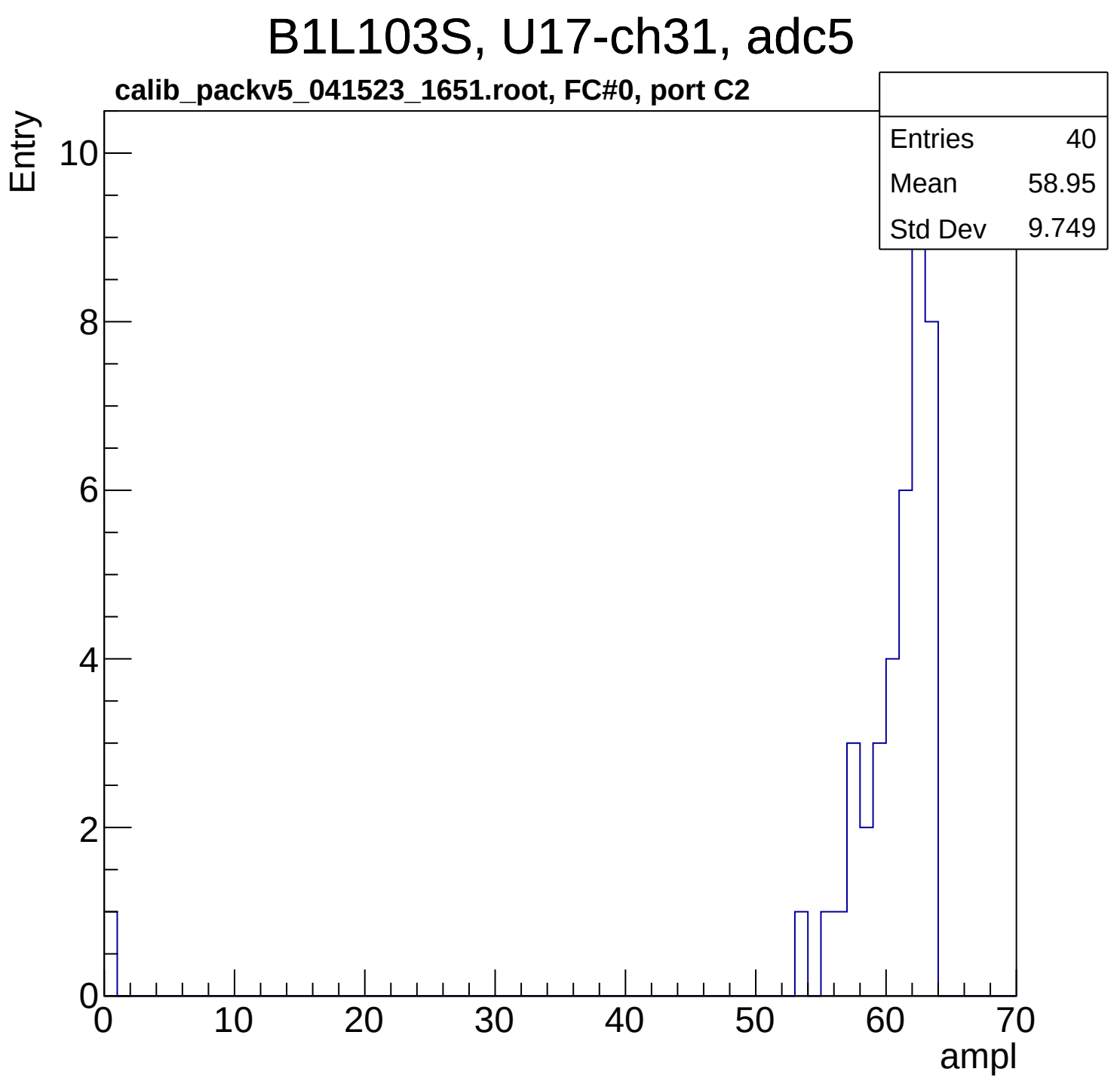
40
50
60
70


B1L103S, U17-ch31, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 40
Mean 58.95
Std Dev 9.749
Entry
ampl
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0
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60
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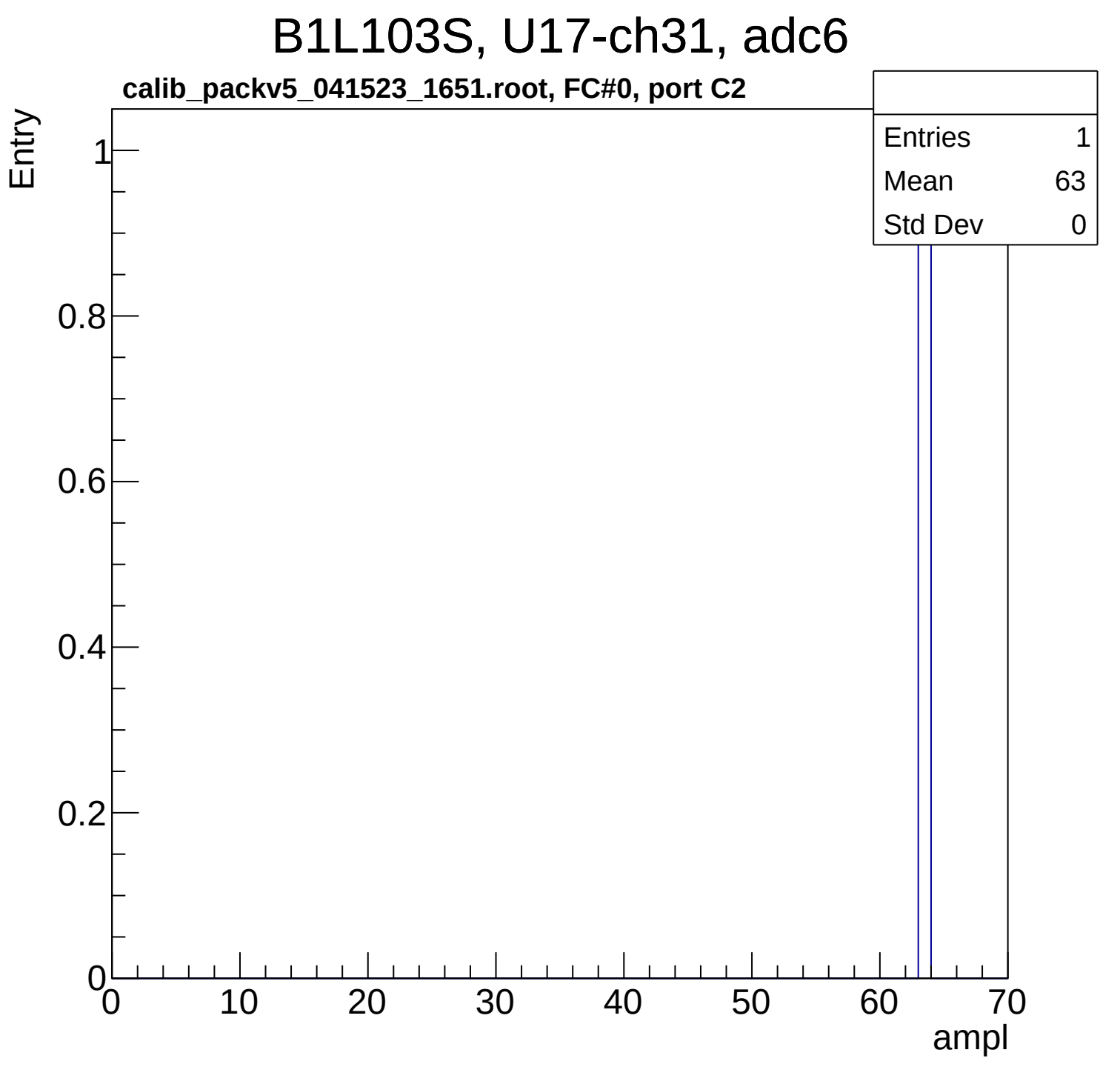
B1L103S, U17-ch31, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 1
Mean 63
Std Dev 0
Entry
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0.8
0.6
0.4
0.2
0
0
10
20
30
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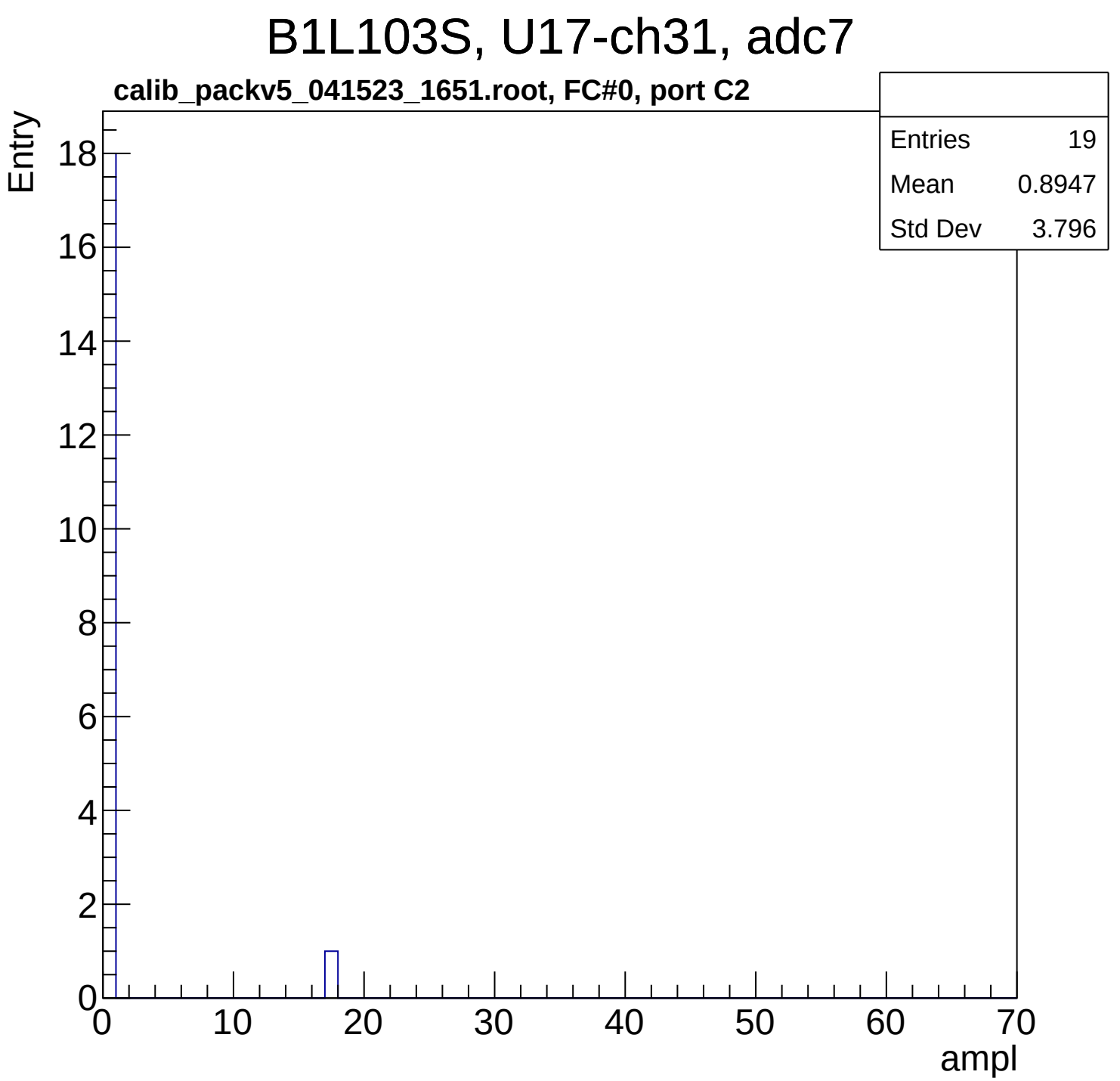
50
60
70
ampl


B1L103S, U17-ch31, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0.8947
Std Dev 3.796
Entry
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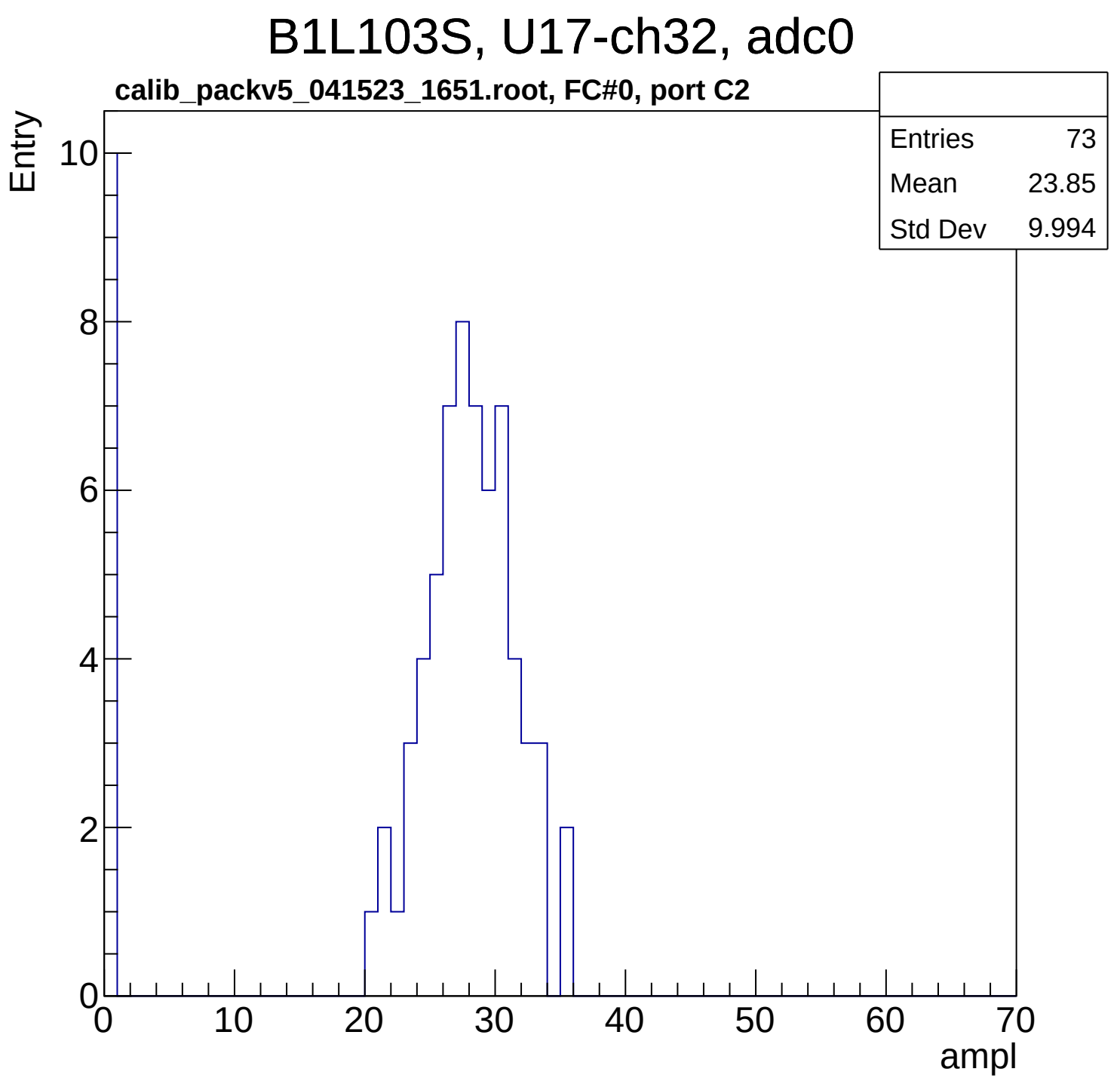
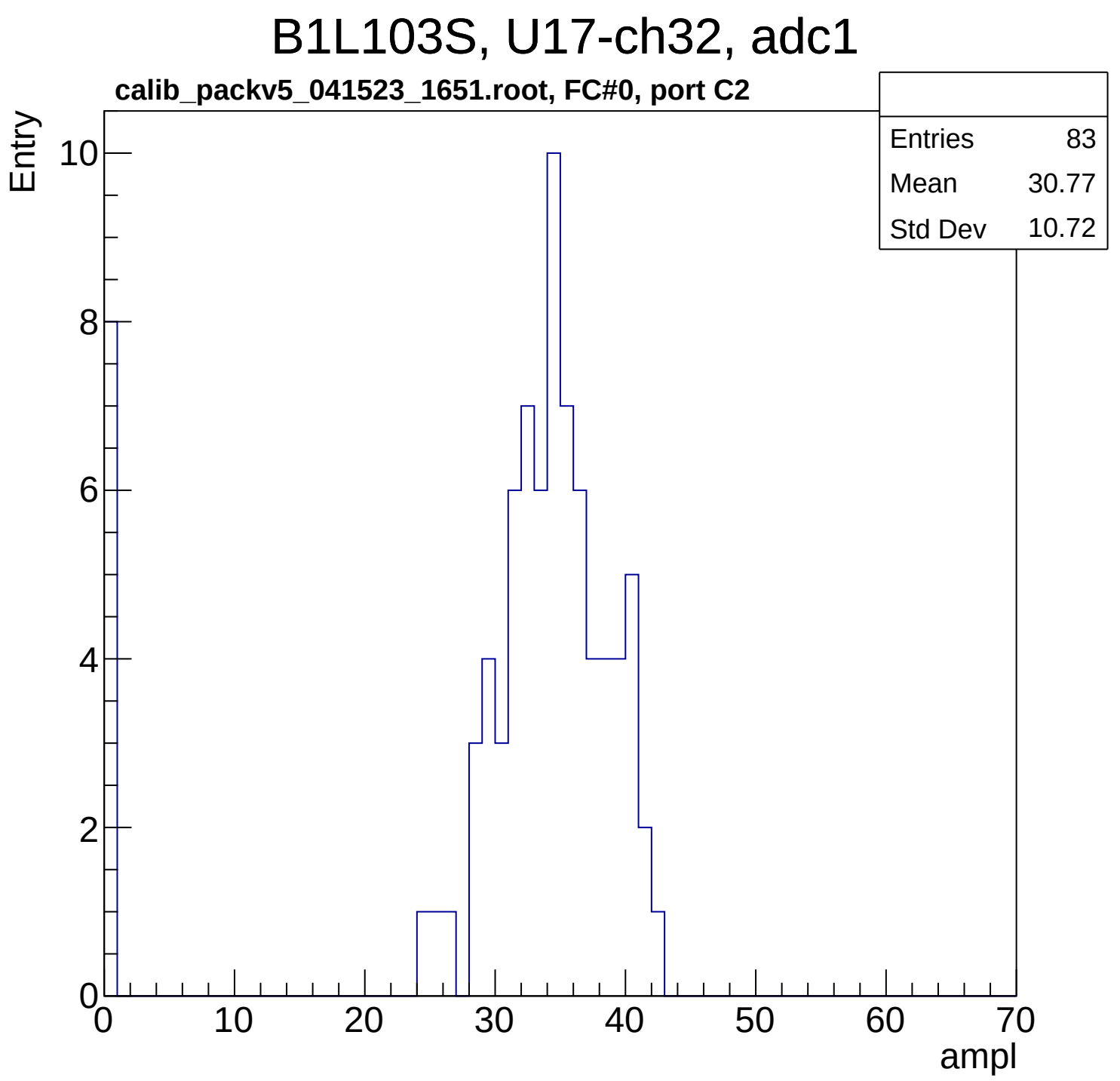
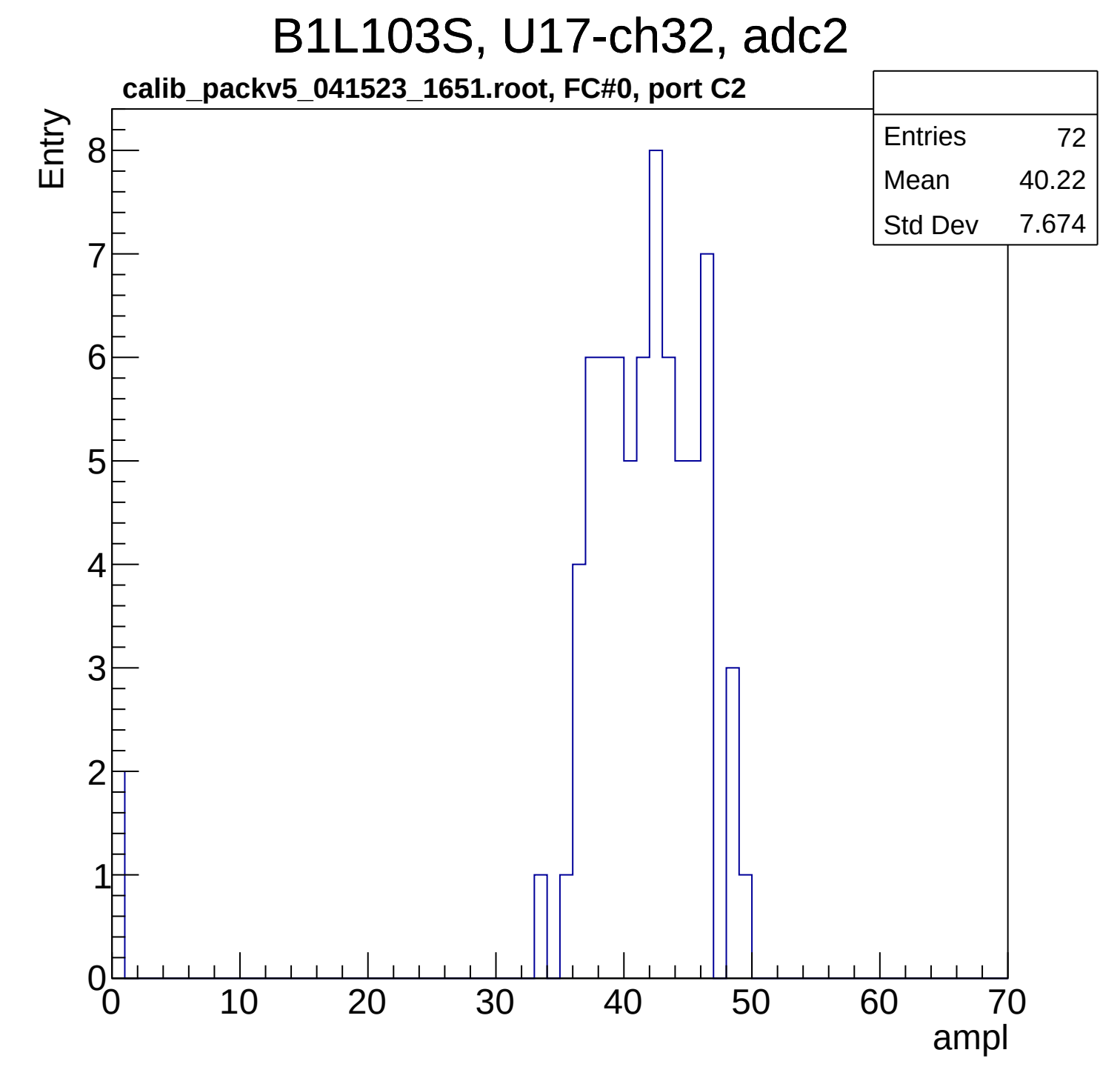
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch32, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 23.85
Std Dev 9.994
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch32, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 30.77
Std Dev 10.72
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch32, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 40.22
Std Dev 7.674
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
30
40
50
60
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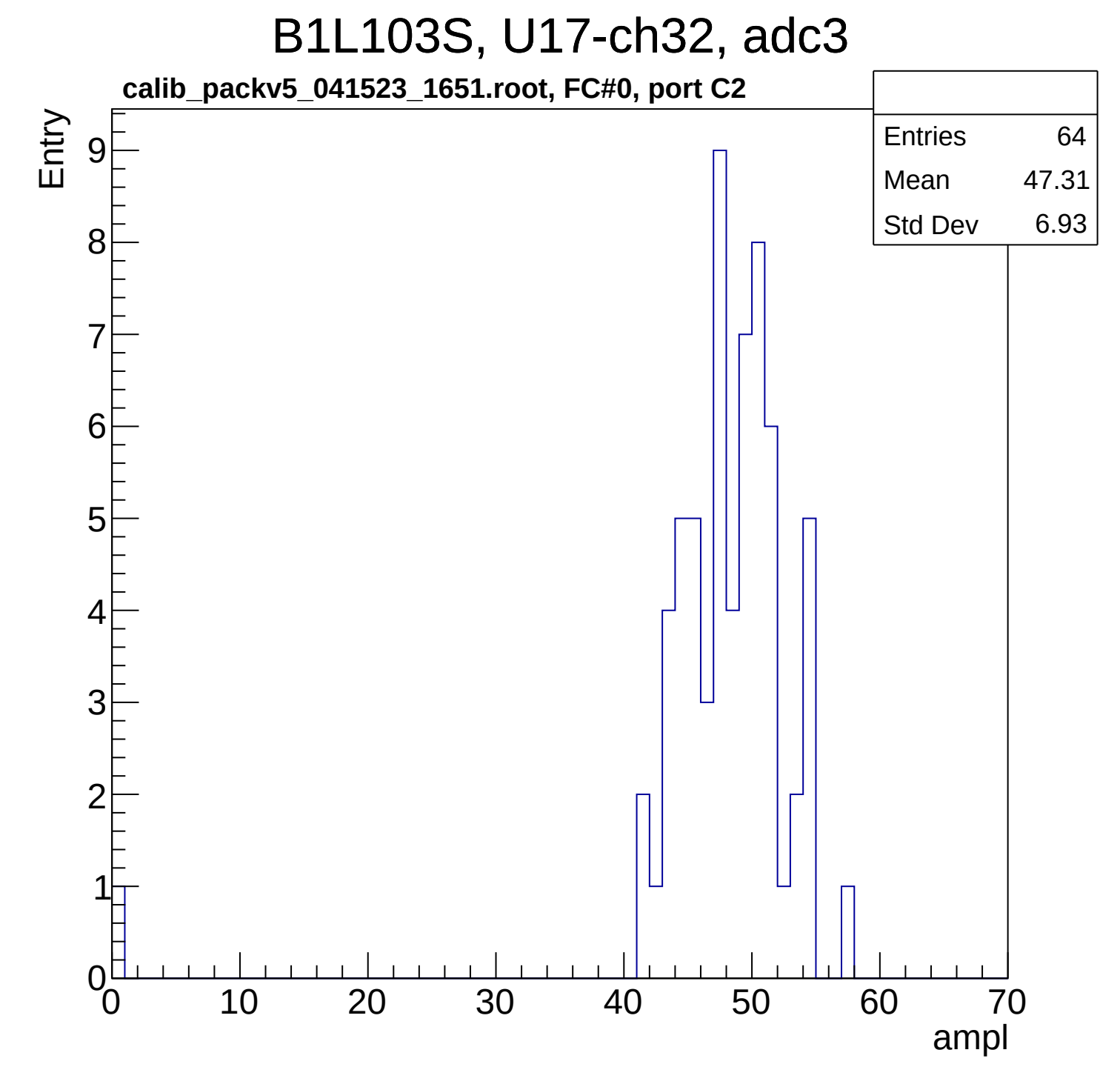
B1L103S, U17-ch32, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 47.31
Std Dev 6.93
Entry
ampl
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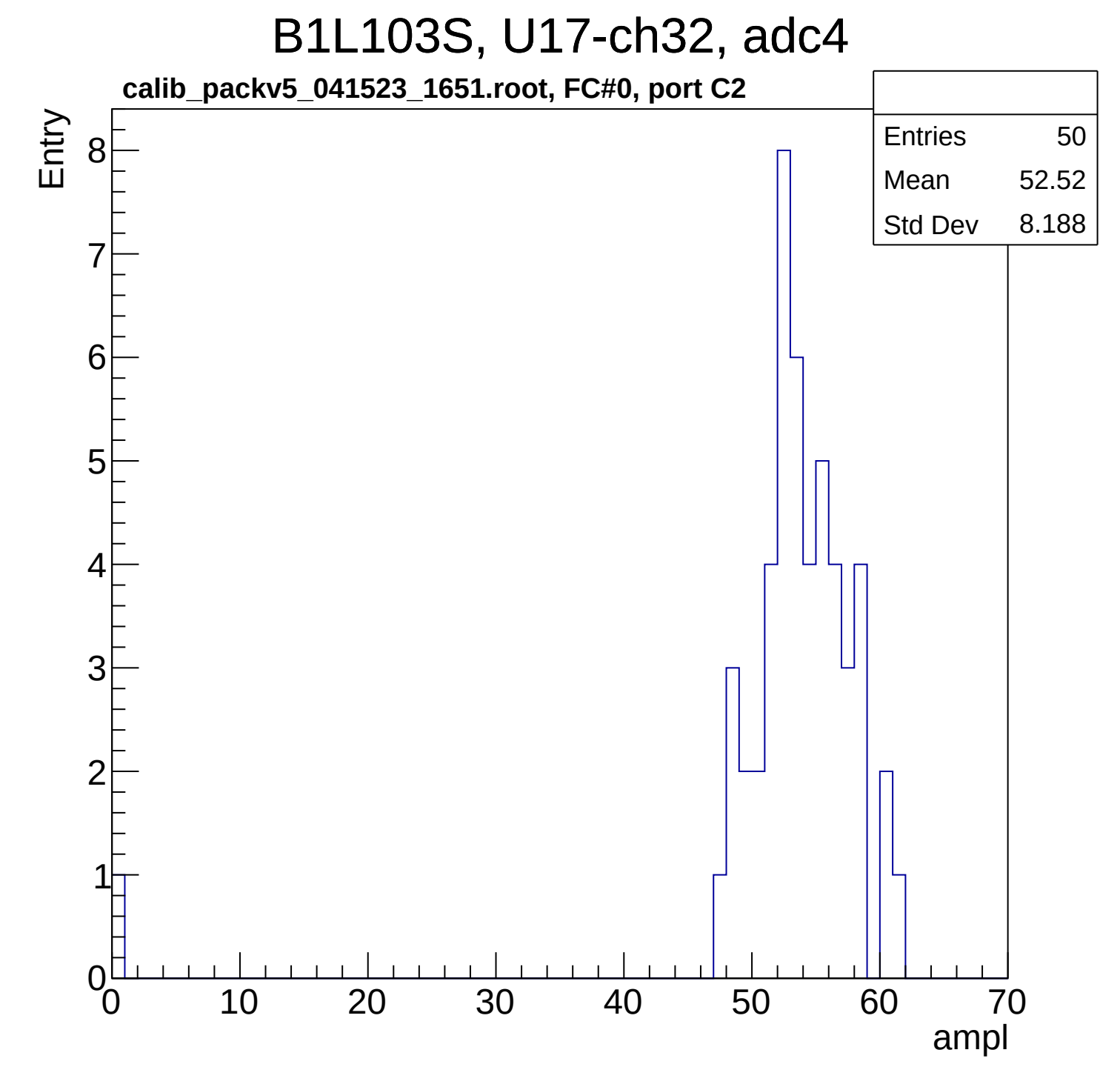
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U17-ch32, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 52.52
Std Dev 8.188
Entry
ampl
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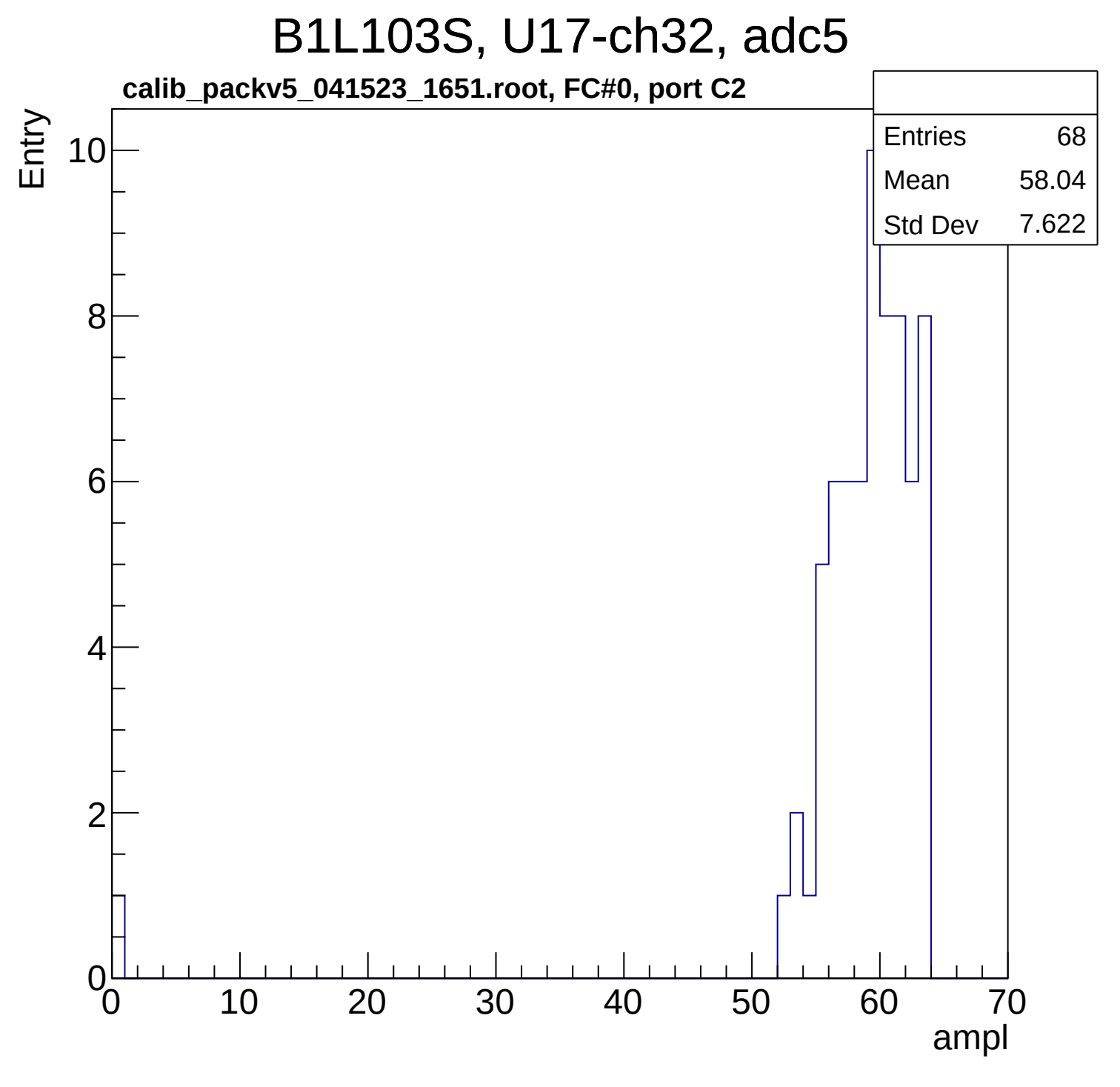
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U17-ch32, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 58.04
Std Dev 7.622
Entry
ampl
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4
6
8
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0
10
20
30
40
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60
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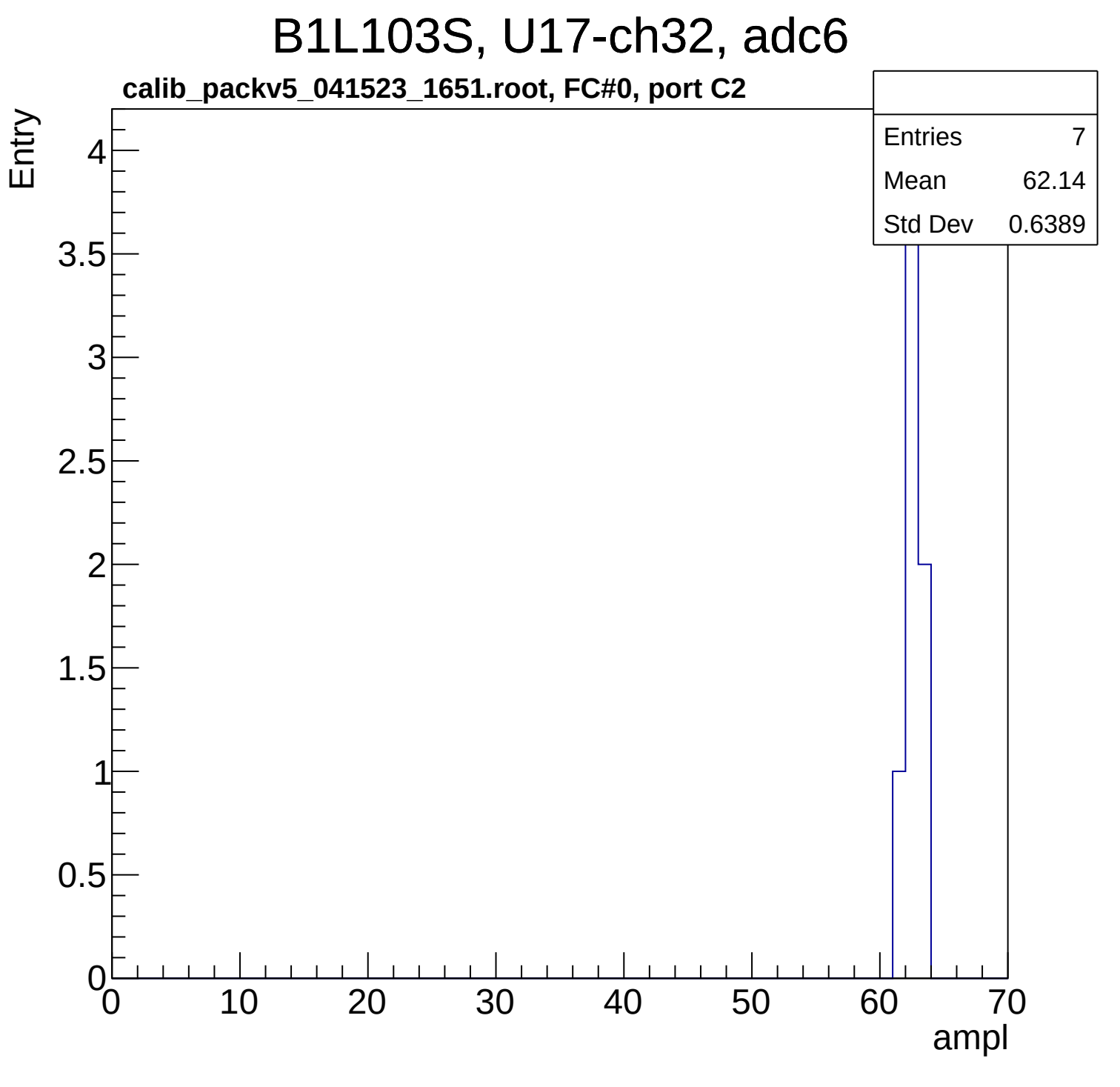
B1L103S, U17-ch32, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 62.14
Std Dev 0.6389
Entry
ampl
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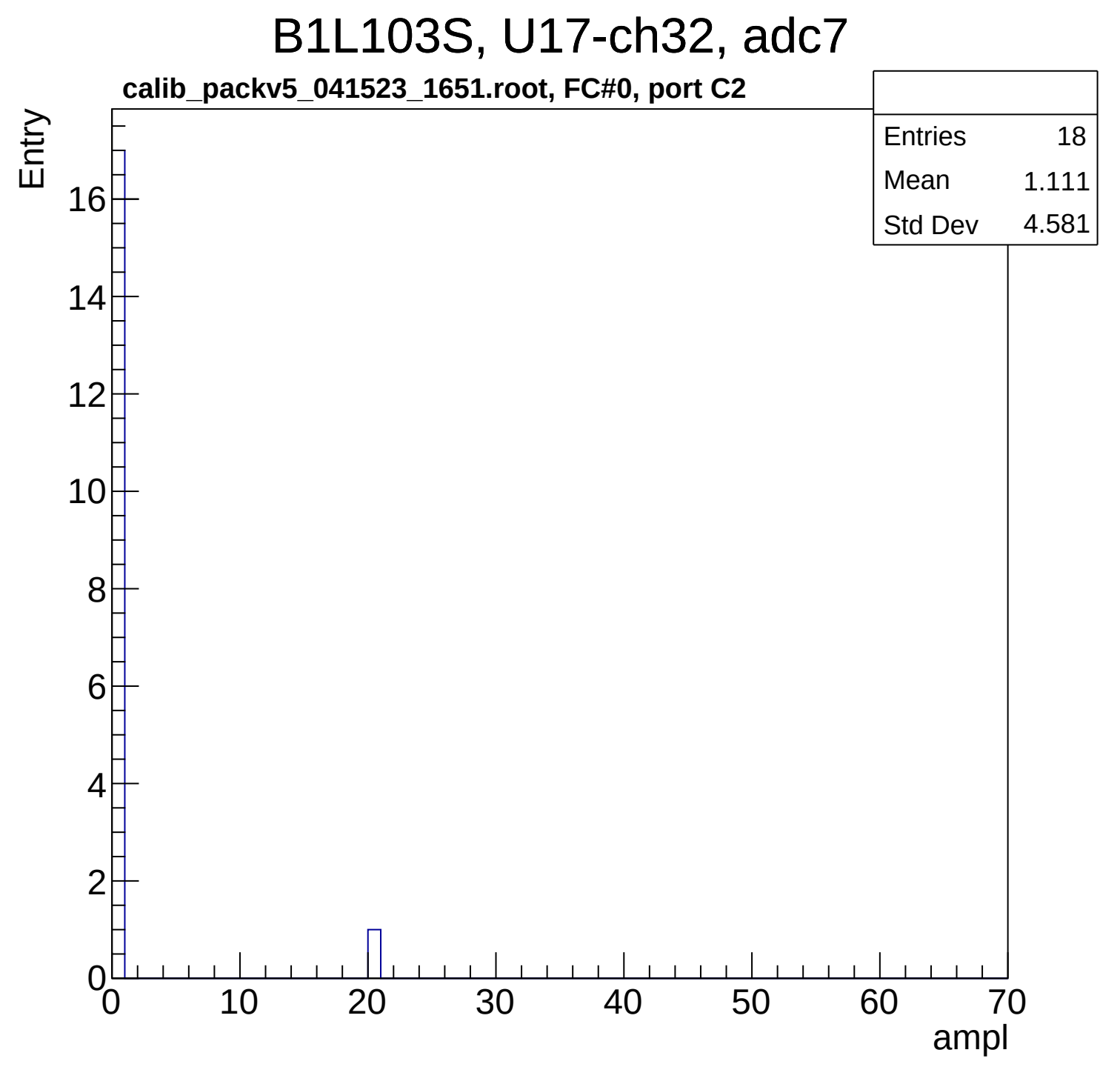
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U17-ch32, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 1.111
Std Dev 4.581
Entry
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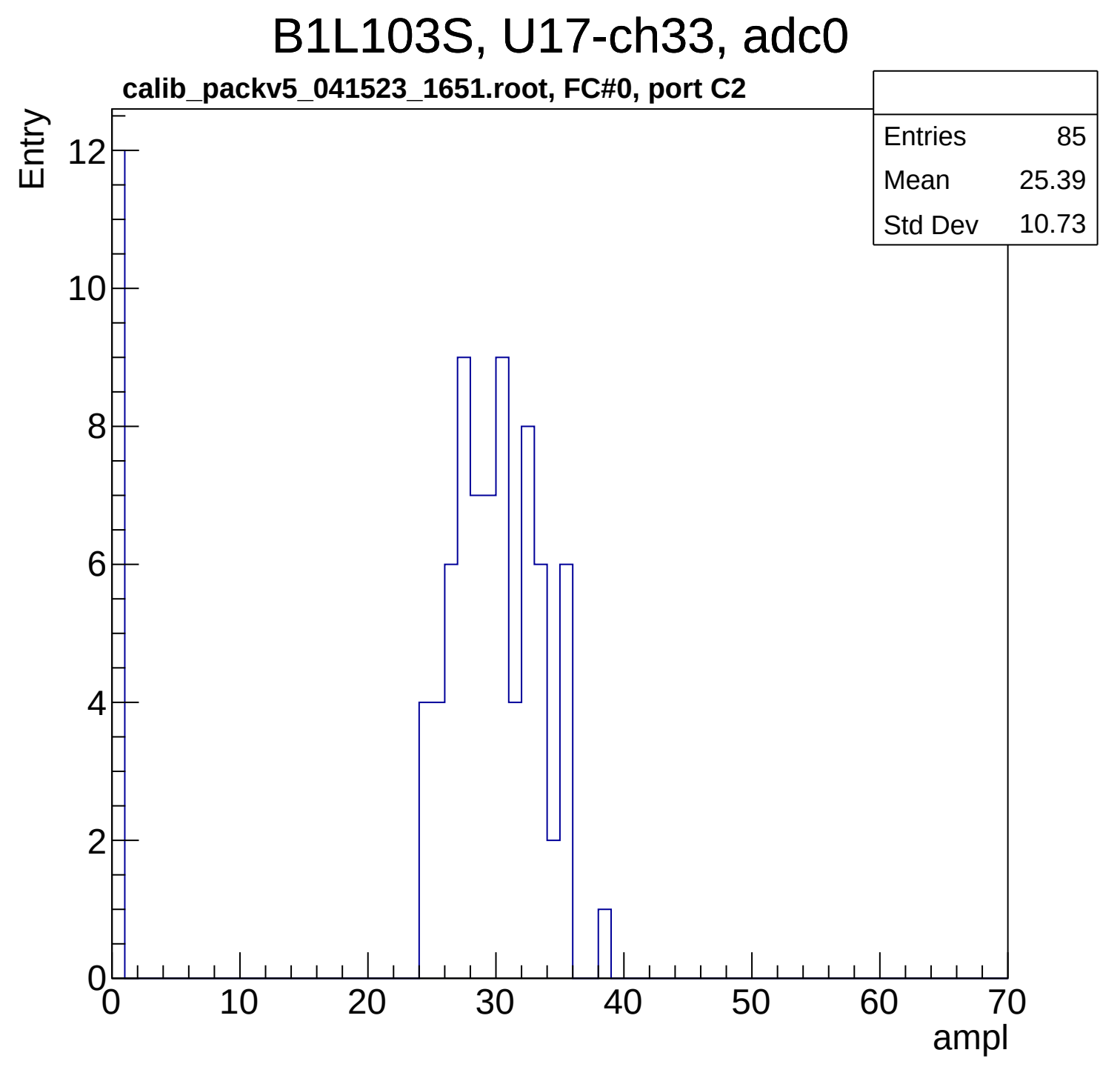
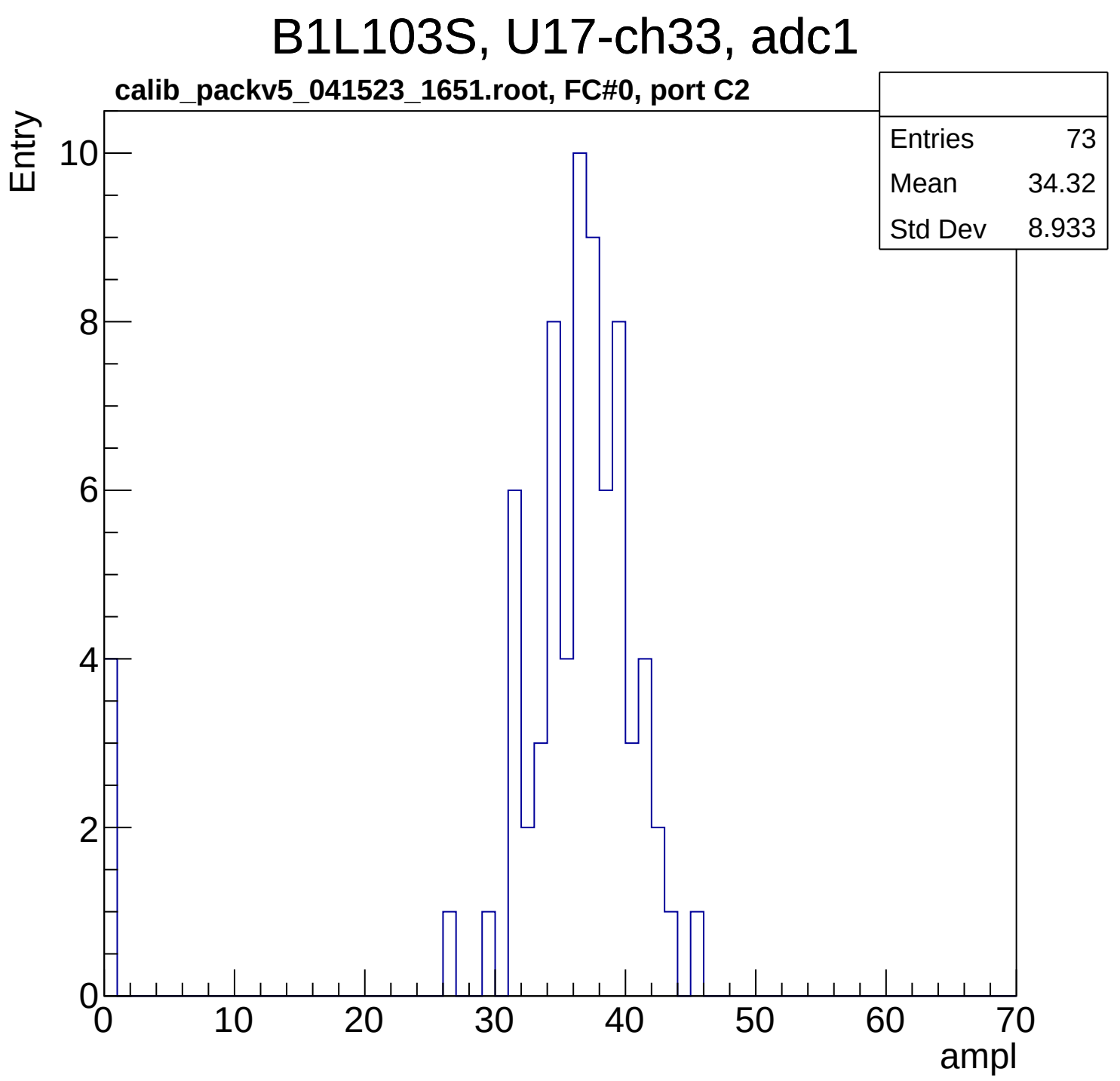
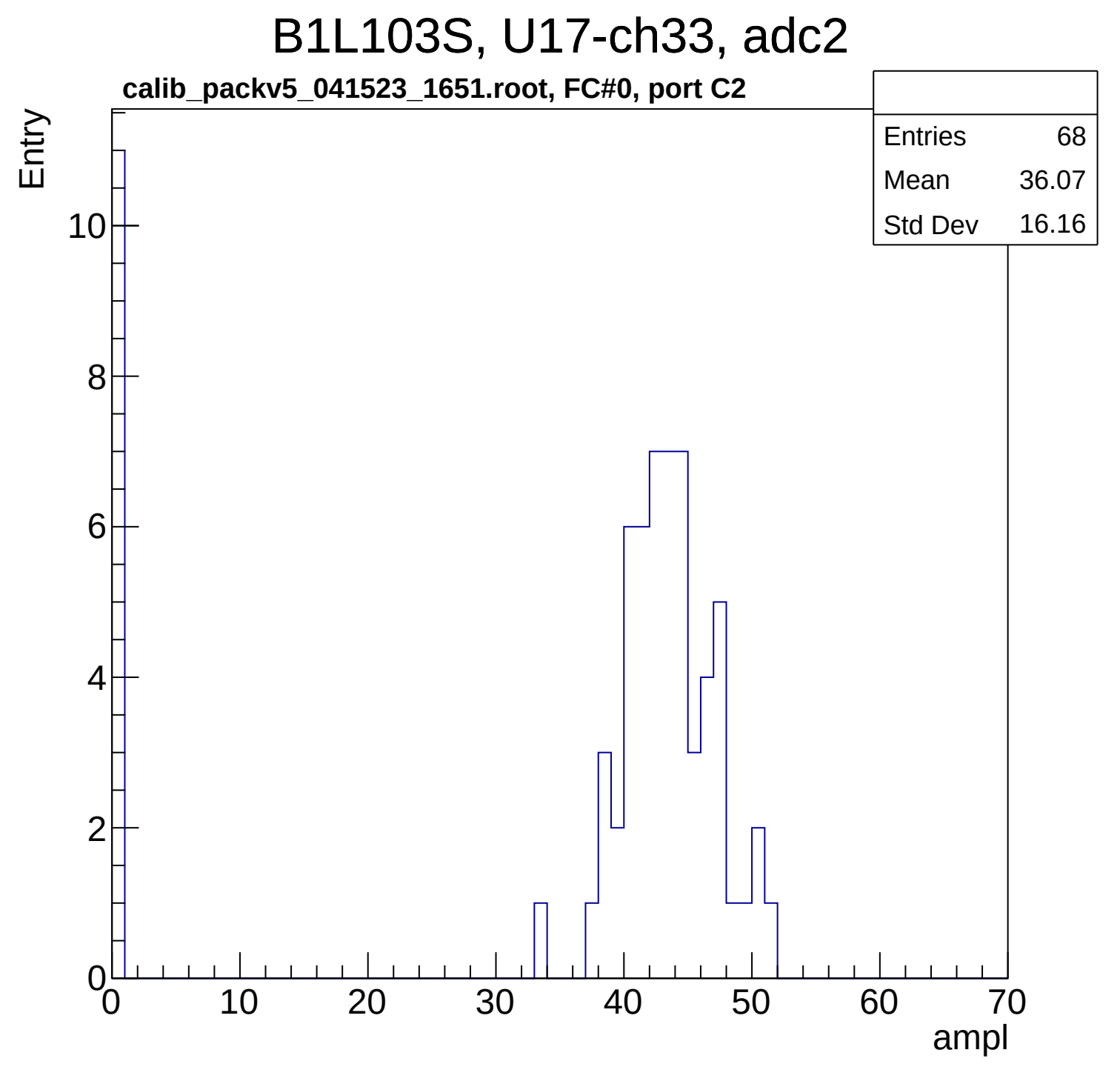
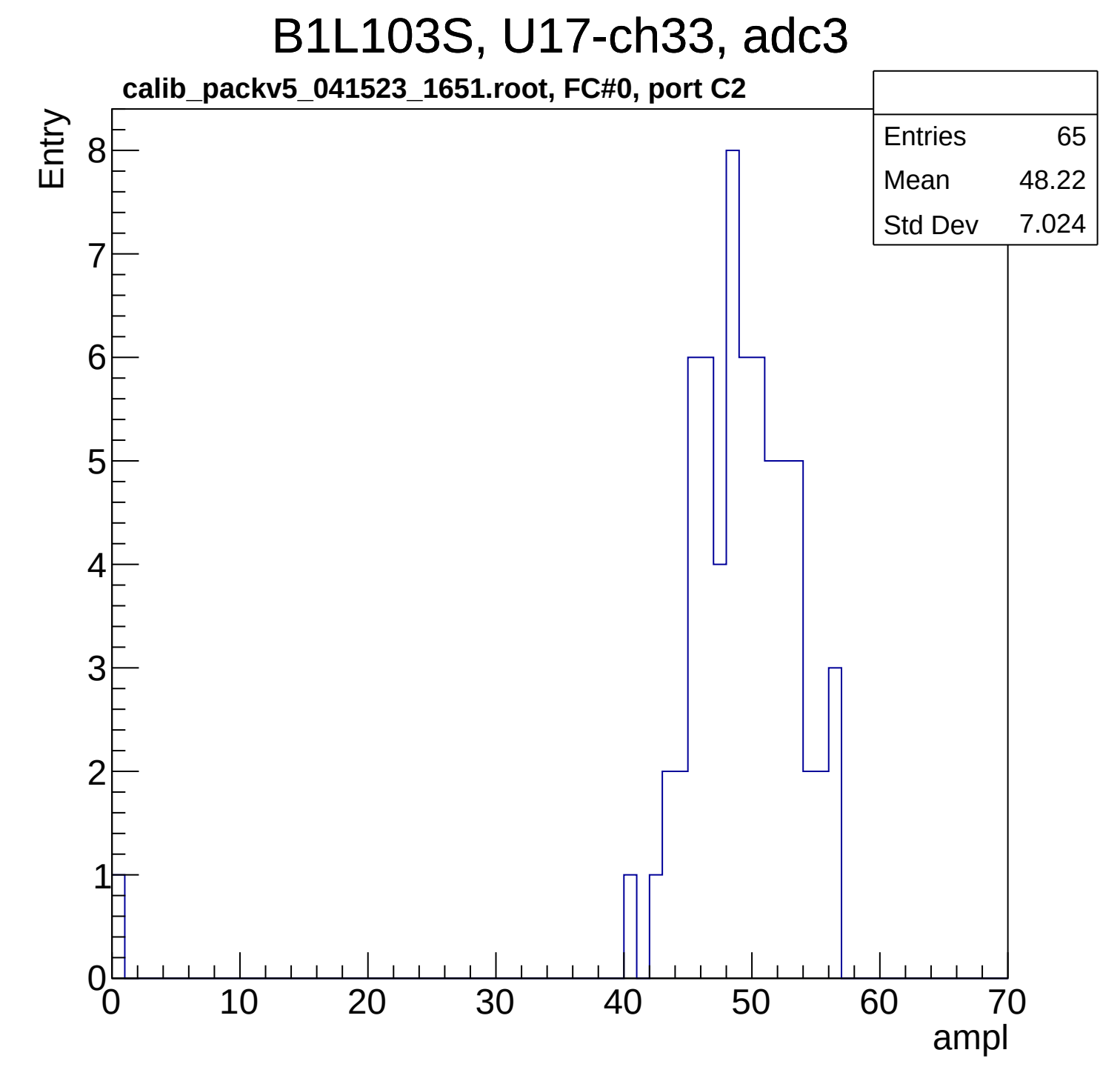
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch33, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 25.39
Std Dev 10.73
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch33, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 34.32
Std Dev 8.933
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch33, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 36.07
Std Dev 16.16
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch33, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 48.22
Std Dev 7.024
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
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60
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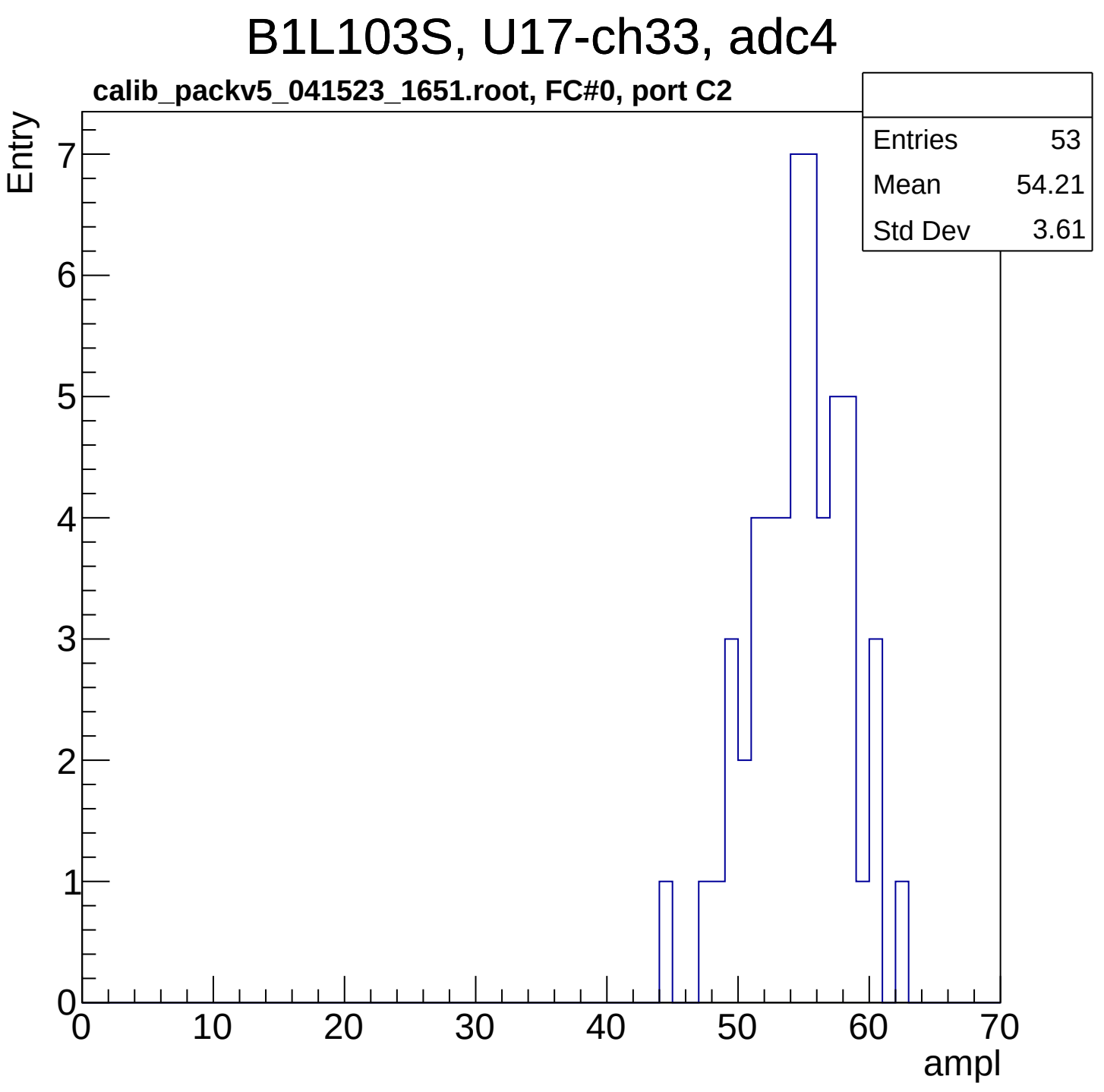
B1L103S, U17-ch33, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 54.21
Std Dev 3.61
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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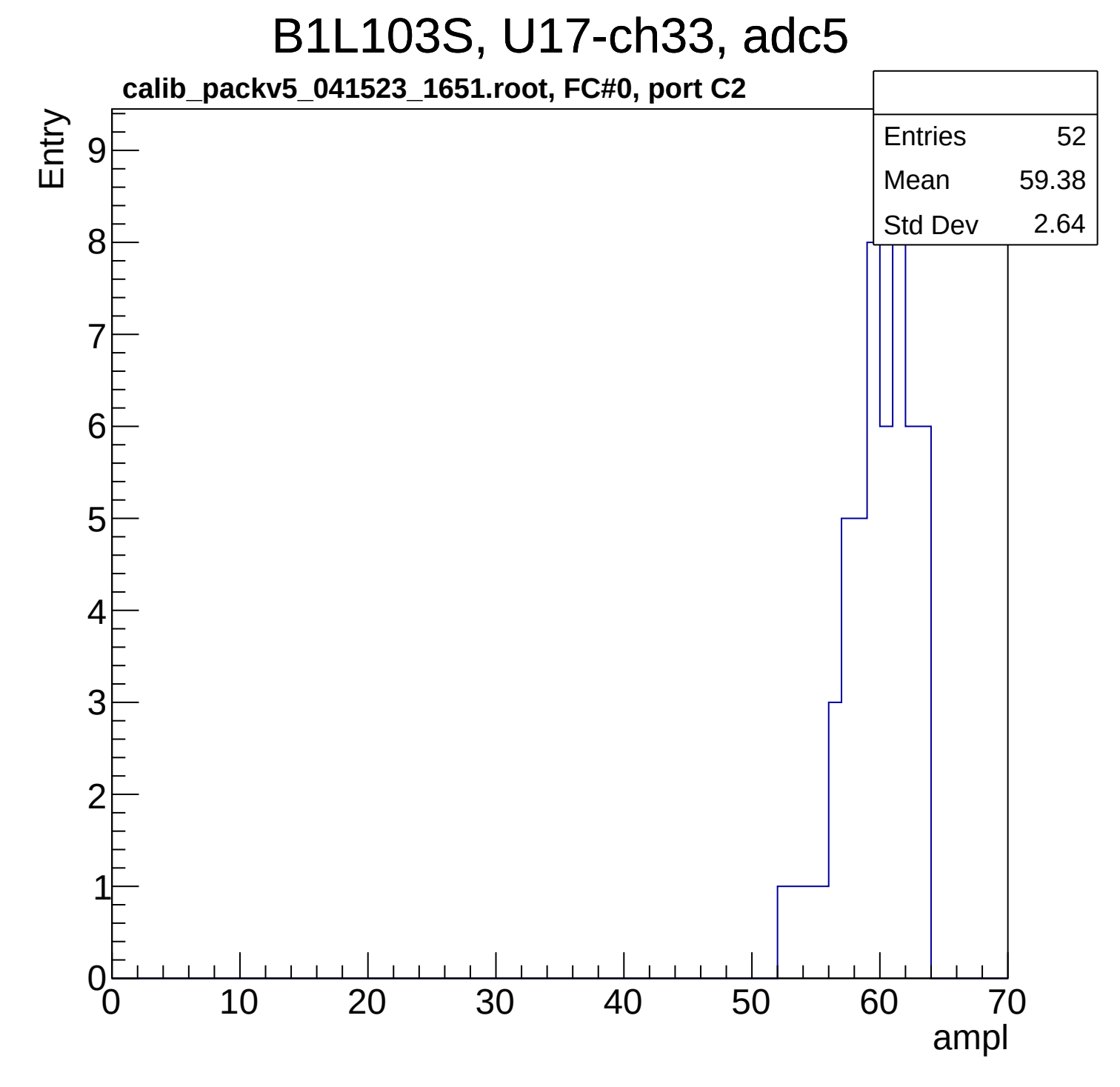
B1L103S, U17-ch33, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 59.38
Std Dev 2.64
Entry
ampl
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2
3
4
5
6
7
8
9
0
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40
50
60
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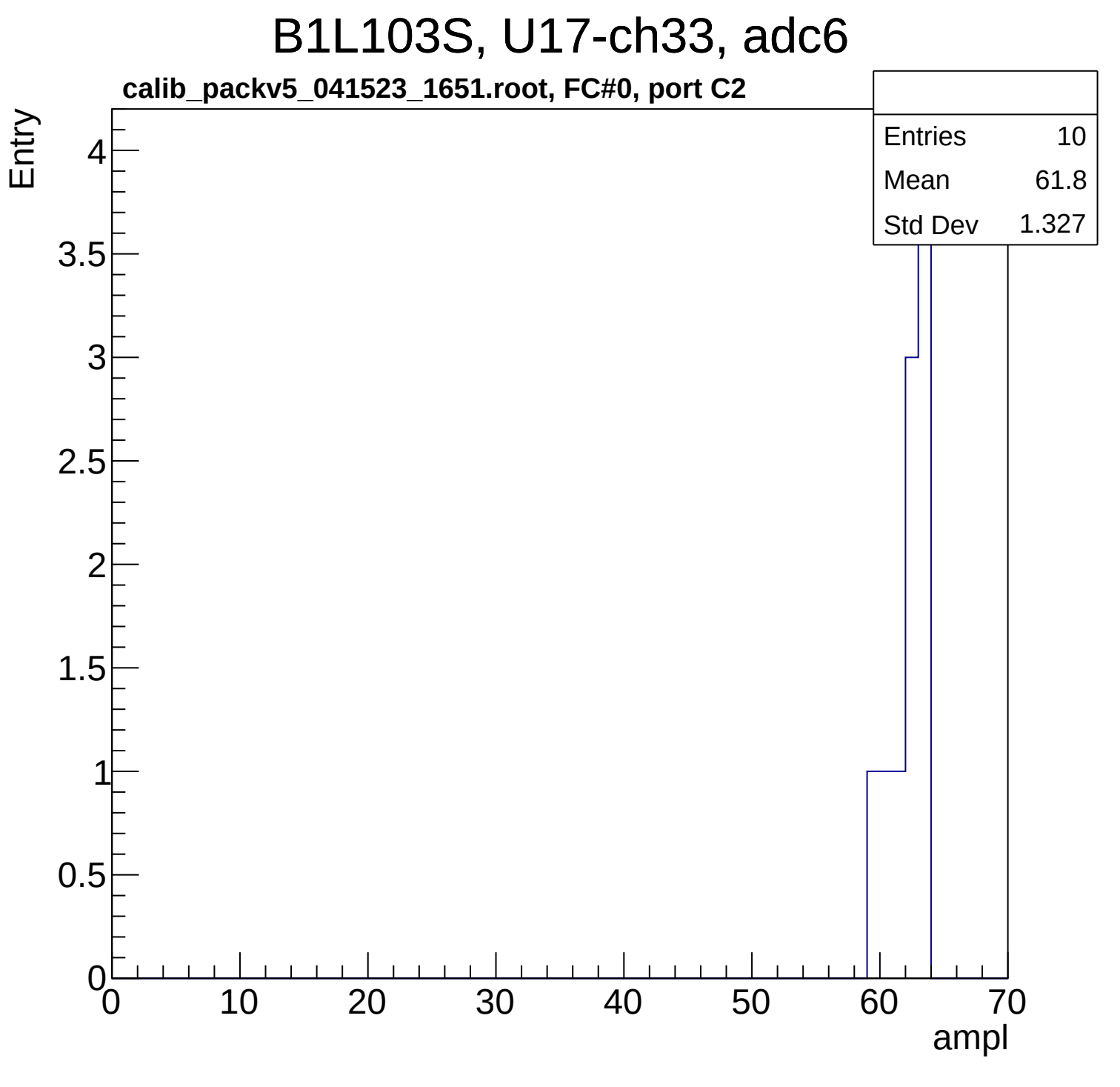
B1L103S, U17-ch33, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 61.8
Std Dev 1.327
Entry
ampl
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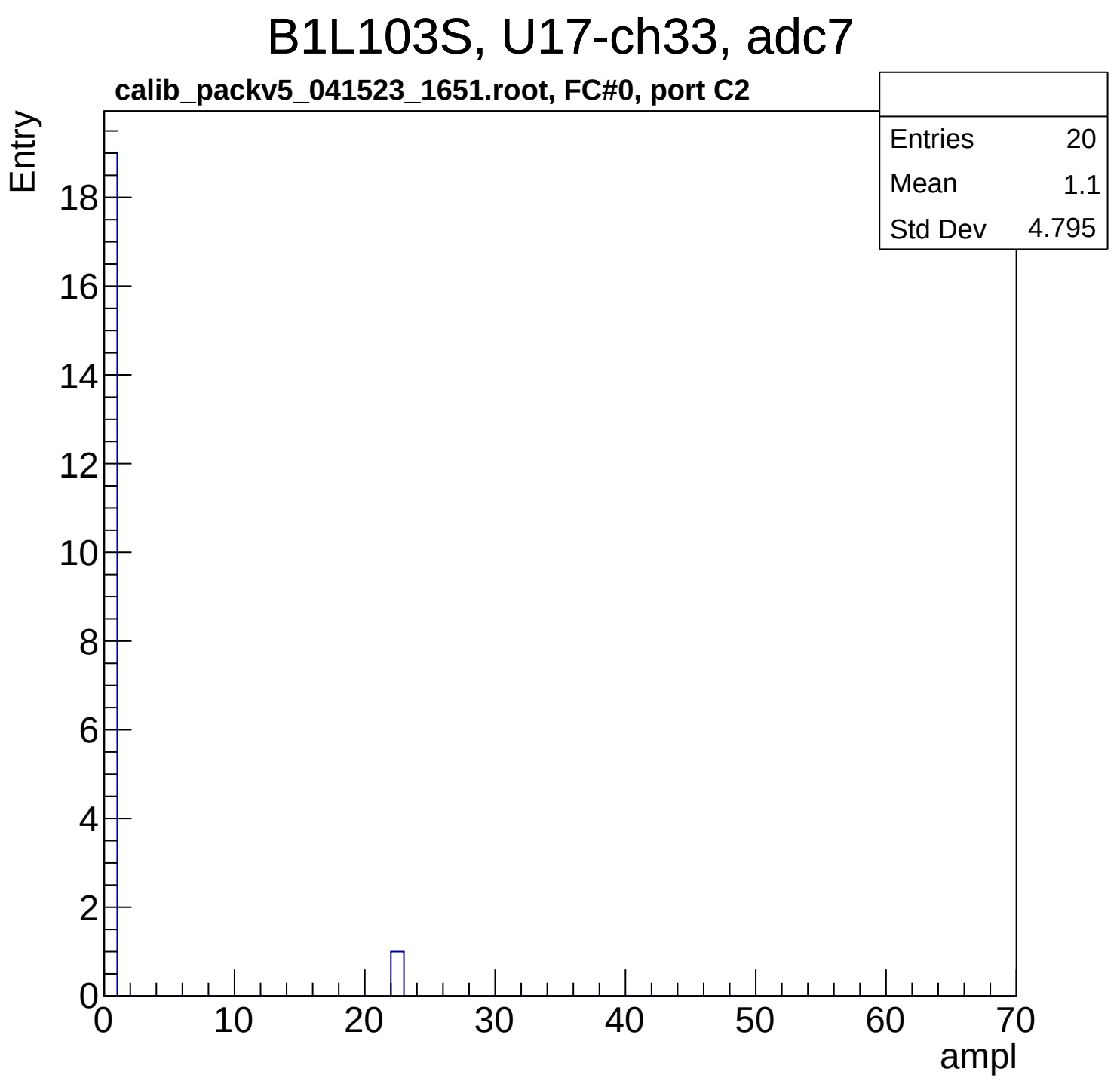
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U17-ch33, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 1.1
Std Dev 4.795
Entry
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6
8
10
12
14
16
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10
20
30
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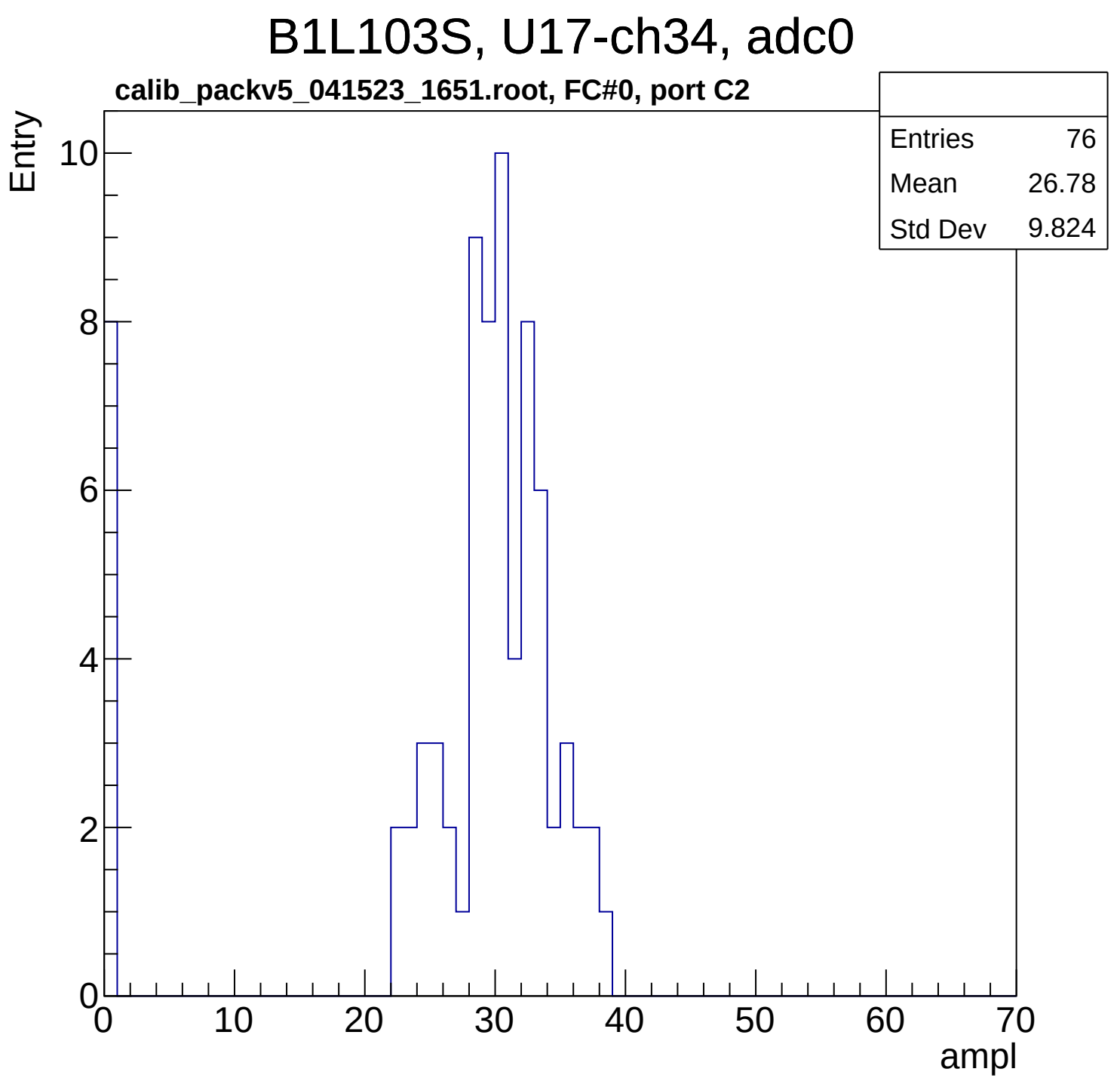
50
60
70
ampl


B1L103S, U17-ch34, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 26.78
Std Dev 9.824
Entry
ampl
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2
4
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8
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0
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20
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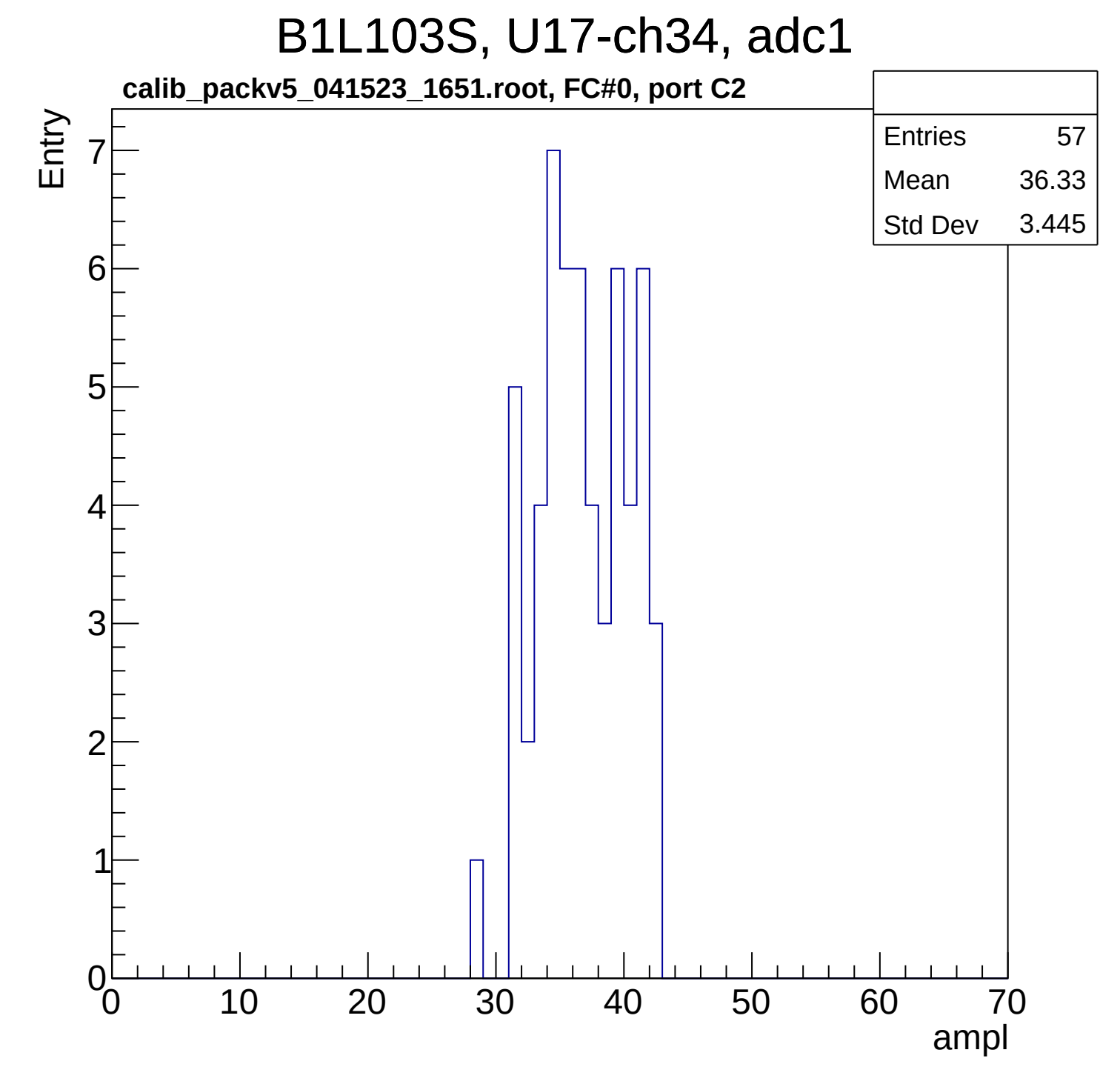
50
60
70


B1L103S, U17-ch34, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 36.33
Std Dev 3.445
Entry
ampl
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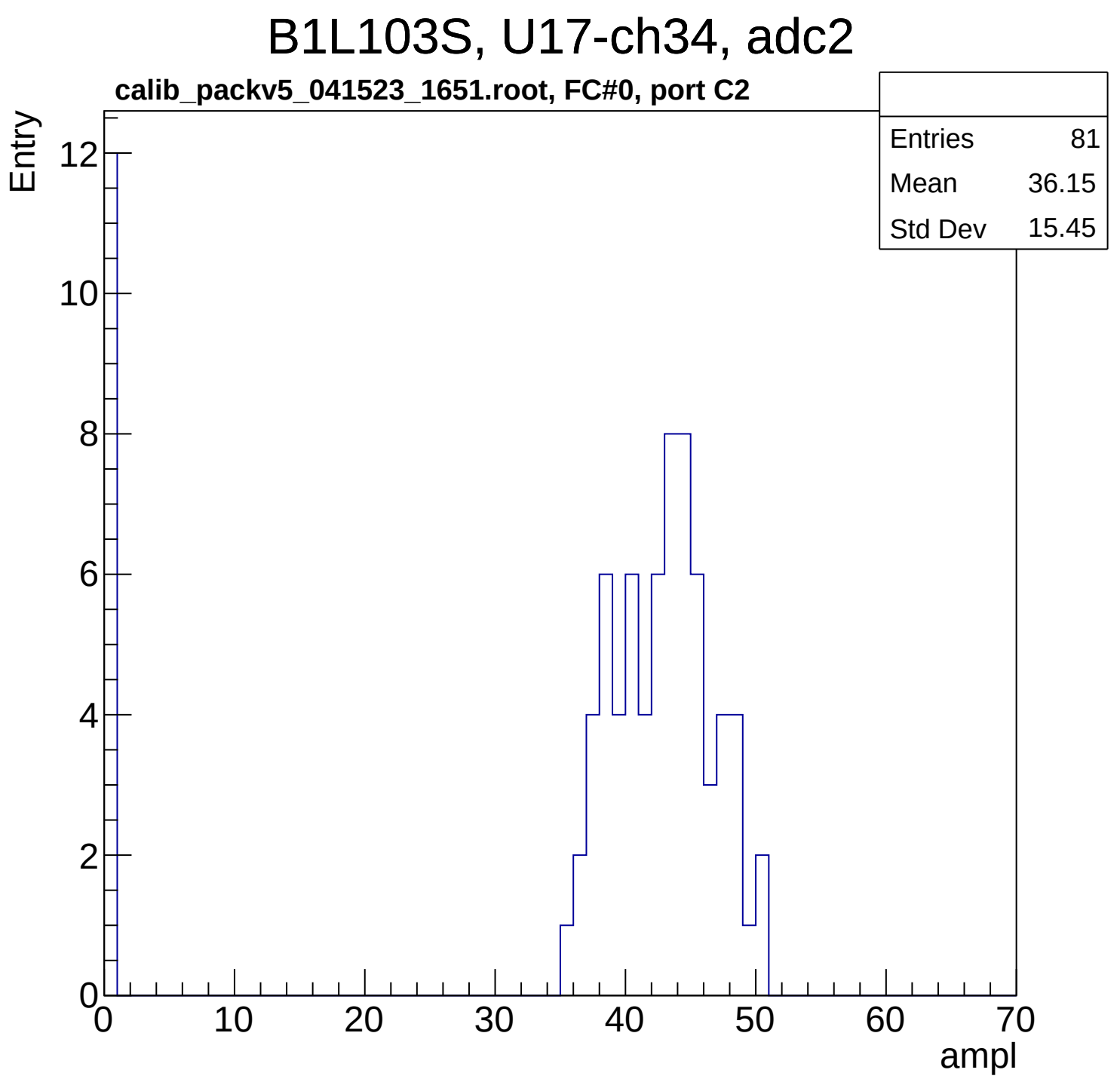
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U17-ch34, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 36.15
Std Dev 15.45
Entry
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4
6
8
10
12
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10
20
30
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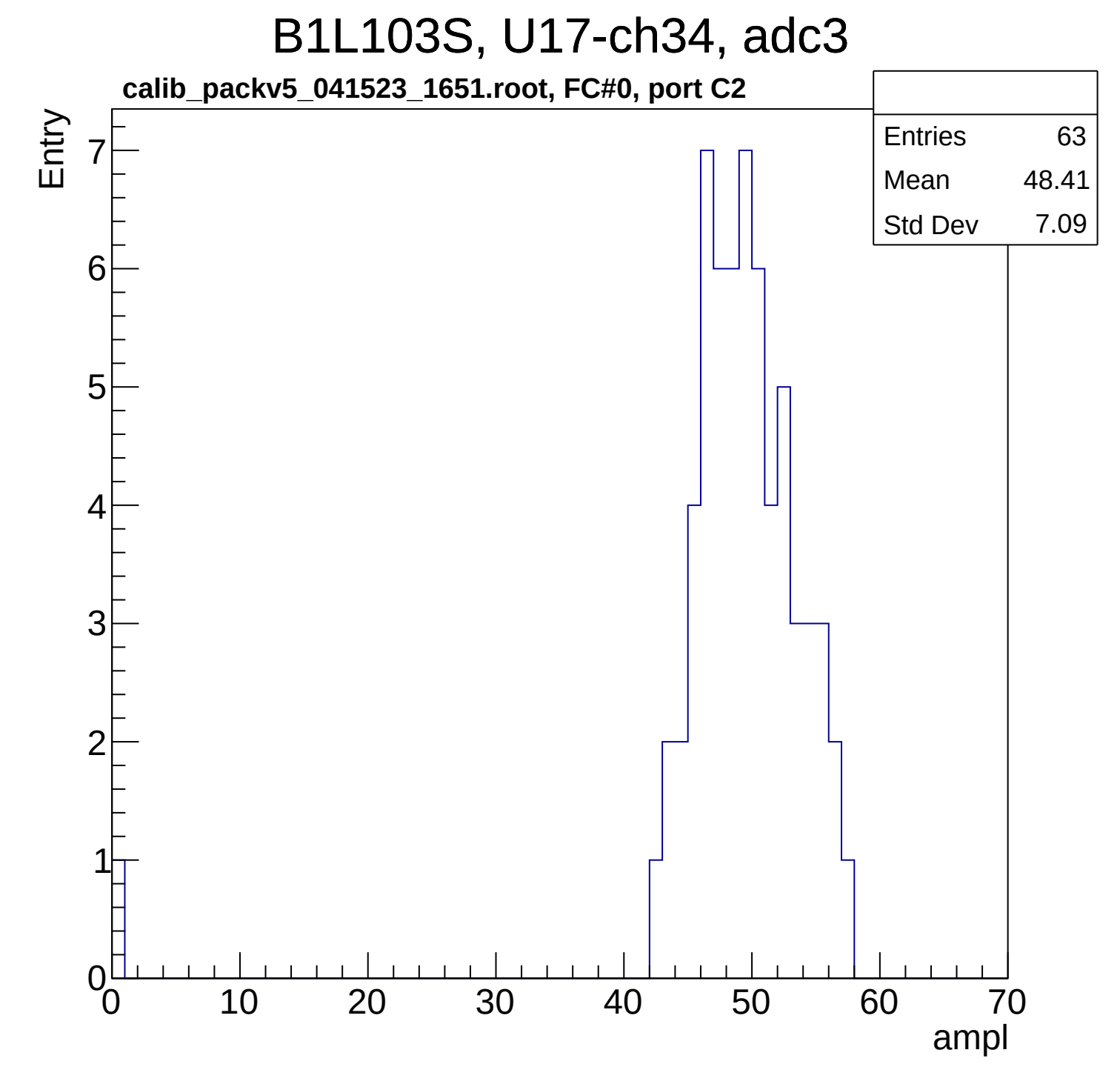
50
60
70
ampl


B1L103S, U17-ch34, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 48.41
Std Dev 7.09
Entry
ampl
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1
2
3
4
5
6
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0
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40
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60
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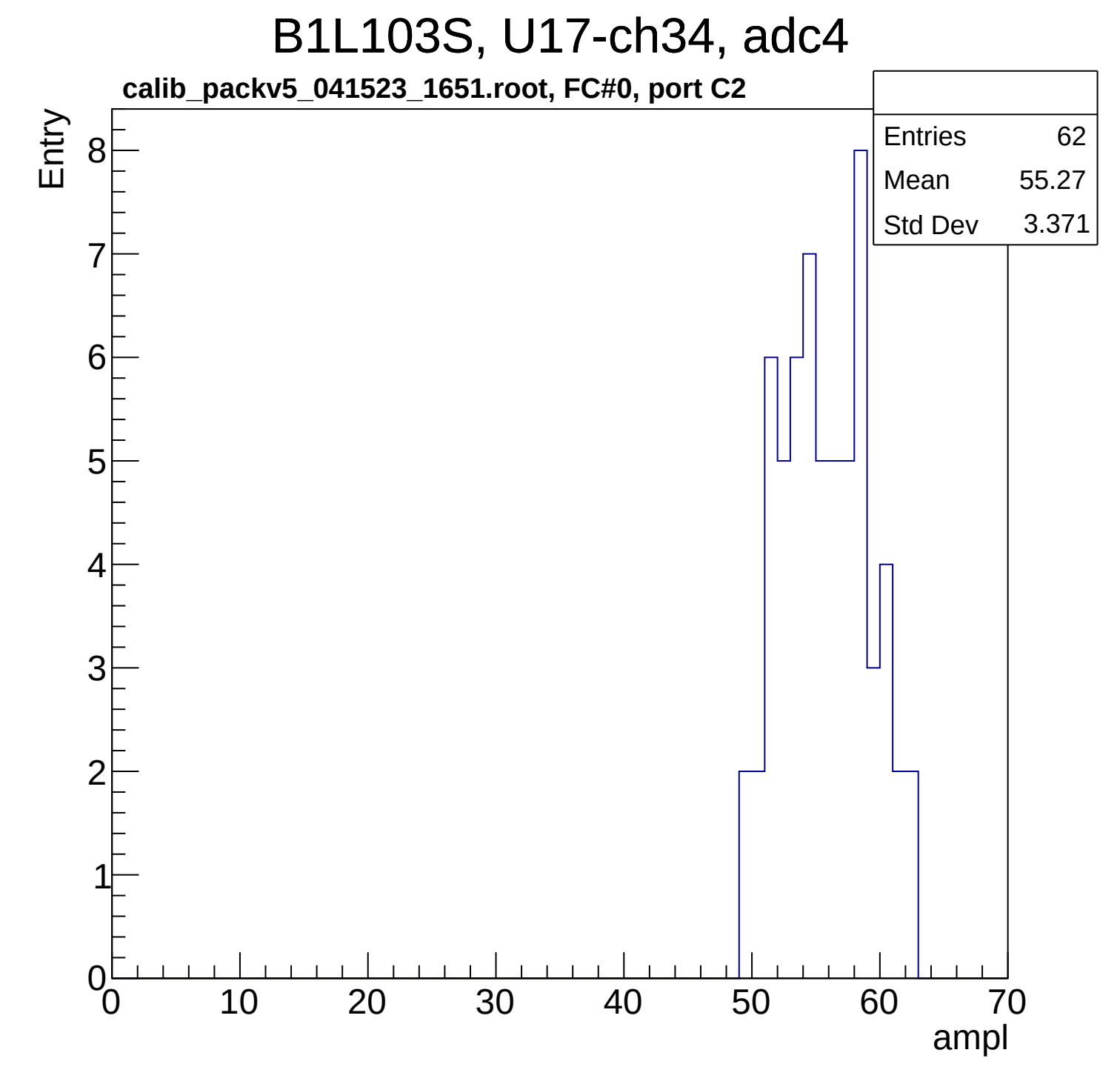
B1L103S, U17-ch34, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 55.27
Std Dev 3.371
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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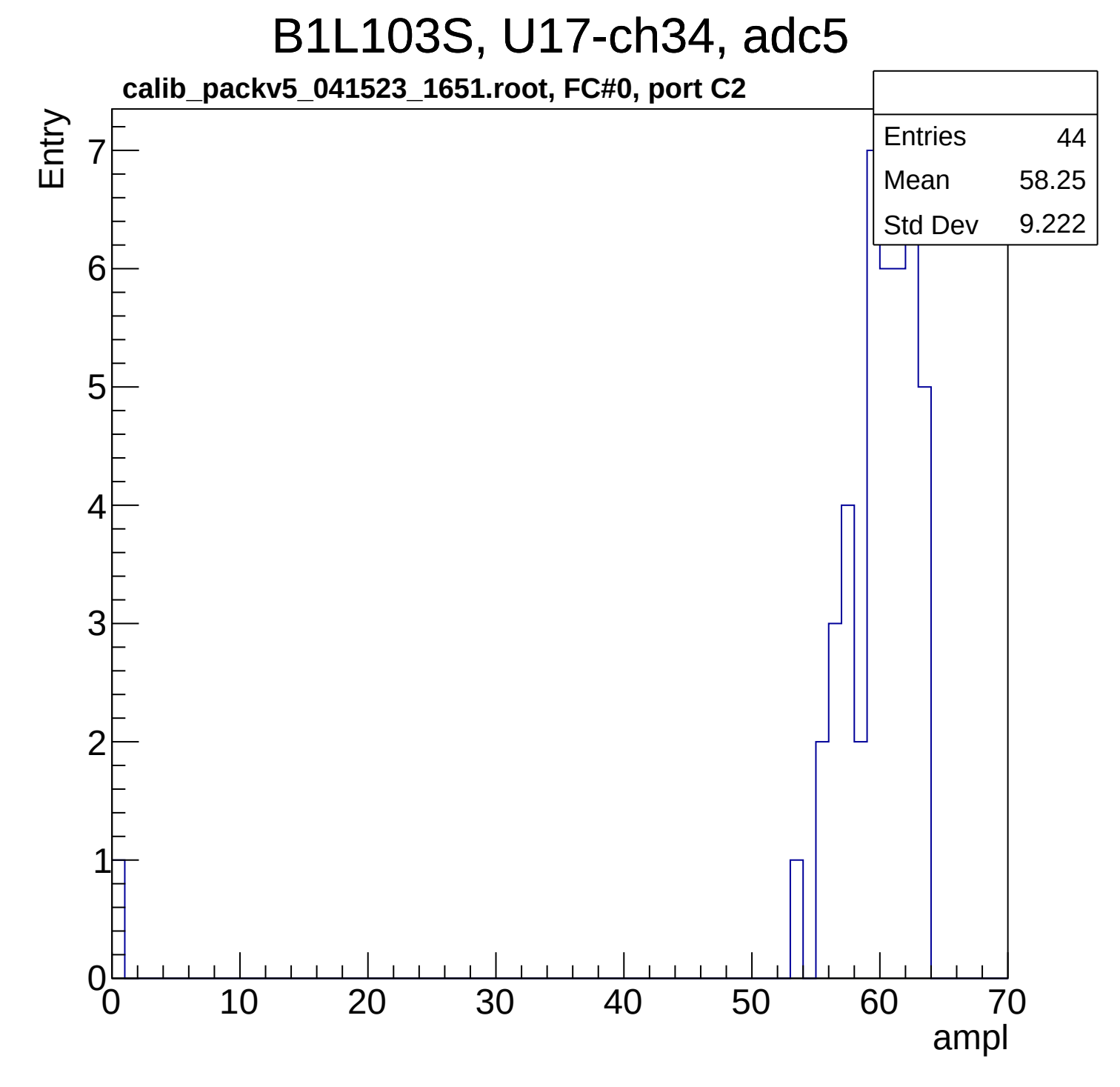
40
50
60
70


B1L103S, U17-ch34, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 58.25
Std Dev 9.222
Entry
ampl
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4
5
6
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0
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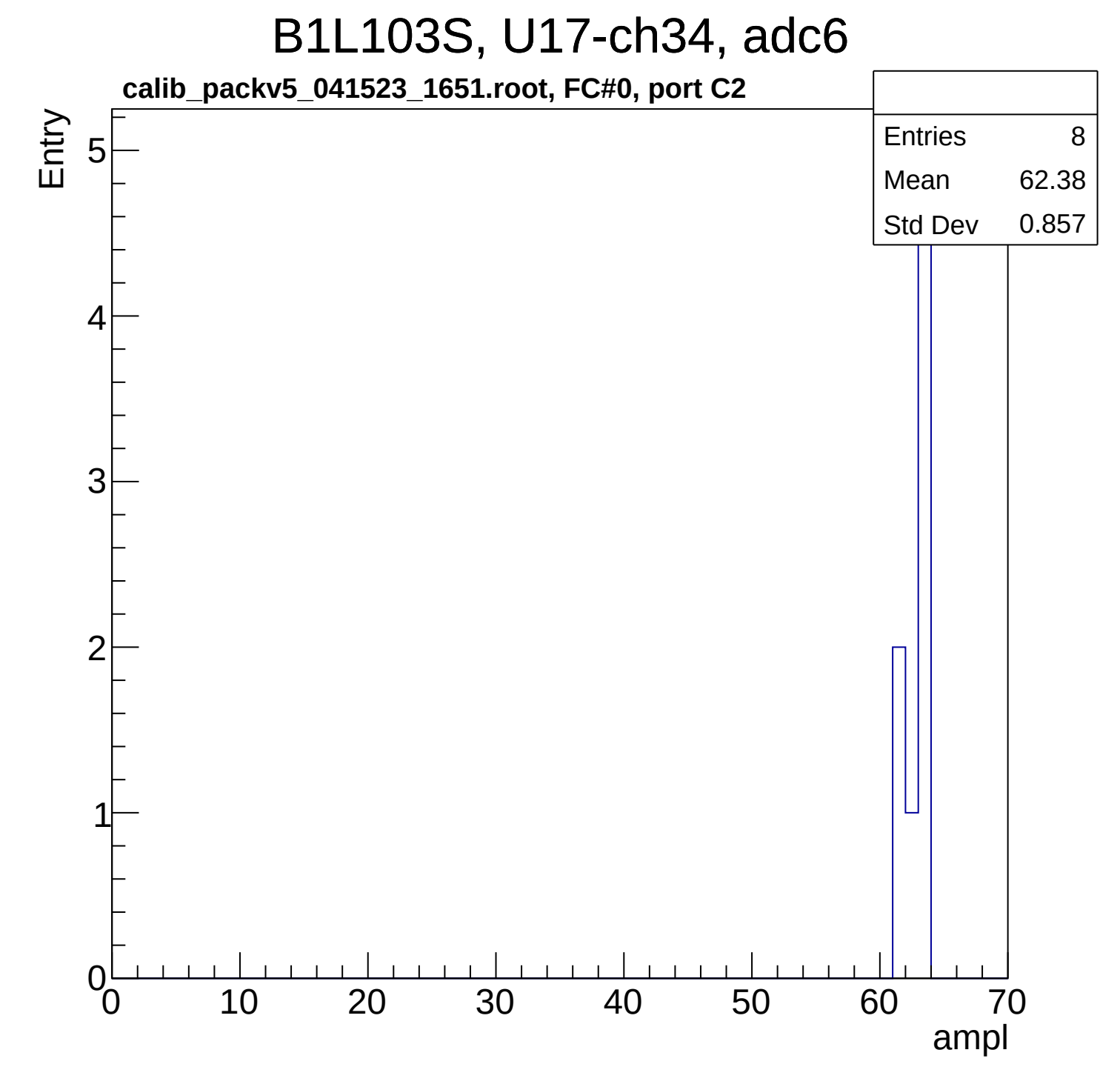
70


B1L103S, U17-ch34, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 62.38
Std Dev 0.857
Entry
ampl
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1
2
3
4
5
0
10
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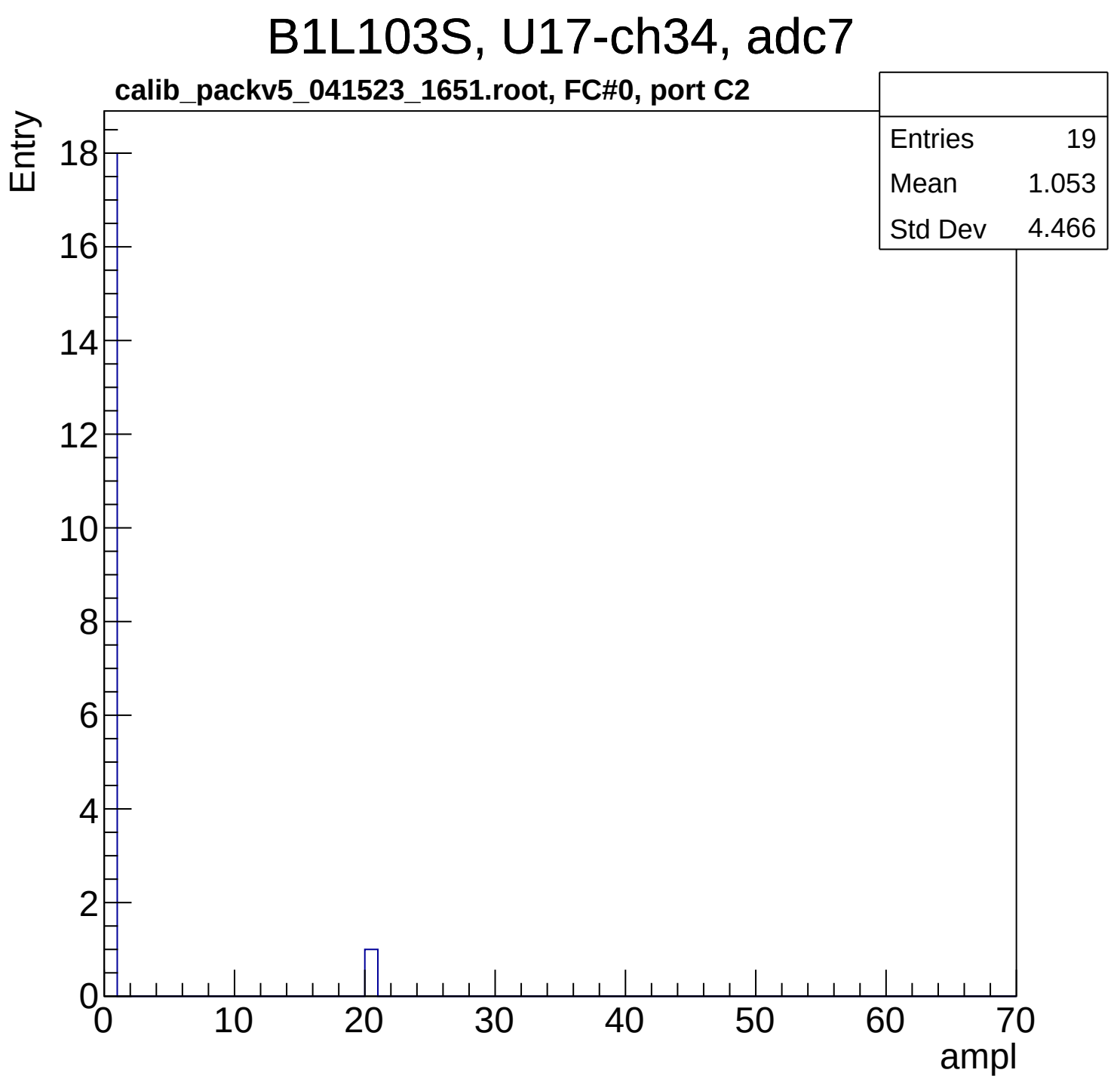
40
50
60
70


B1L103S, U17-ch34, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.053
Std Dev 4.466
Entry
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6
8
10
12
14
16
18
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10
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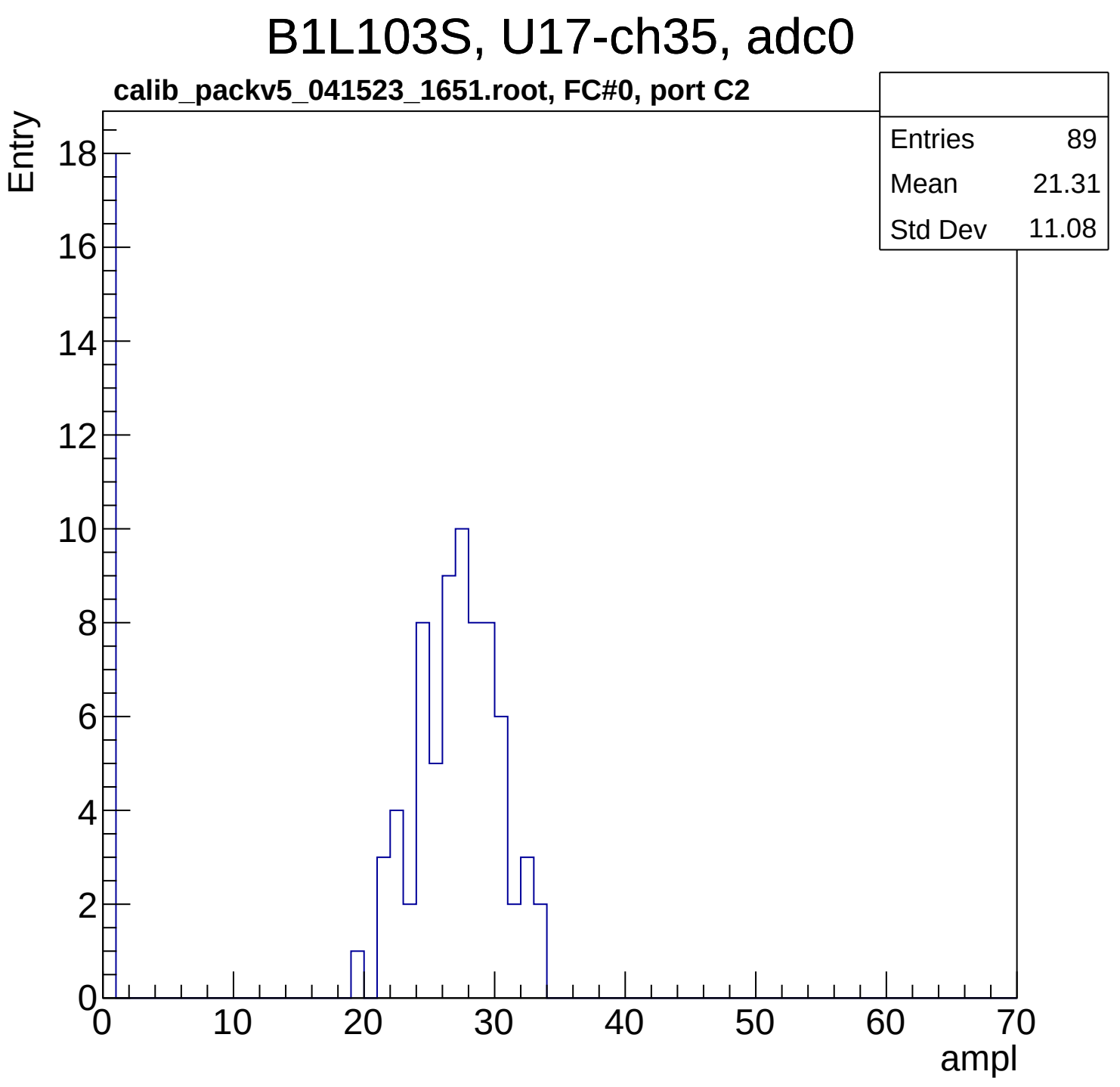
30
40
50
60
70
ampl


B1L103S, U17-ch35, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 89
Mean 21.31
Std Dev 11.08
Entry
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6
8
10
12
14
16
18
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10
20
30
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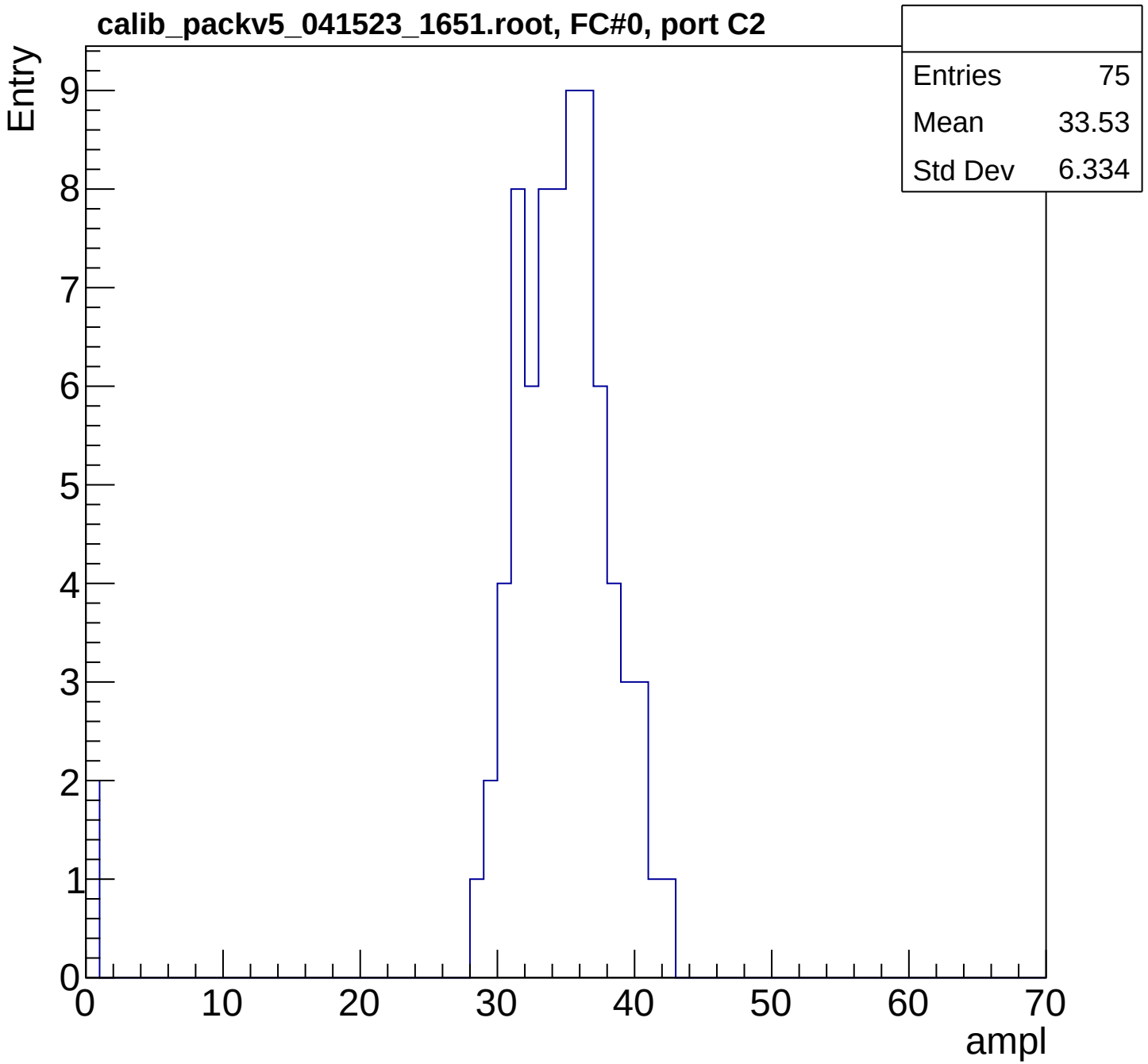
50
60
70
ampl


B1L103S, U17-ch35, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 33.53
Std Dev 6.334
Entry
ampl
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3
4
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6
7
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0
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40
50
60
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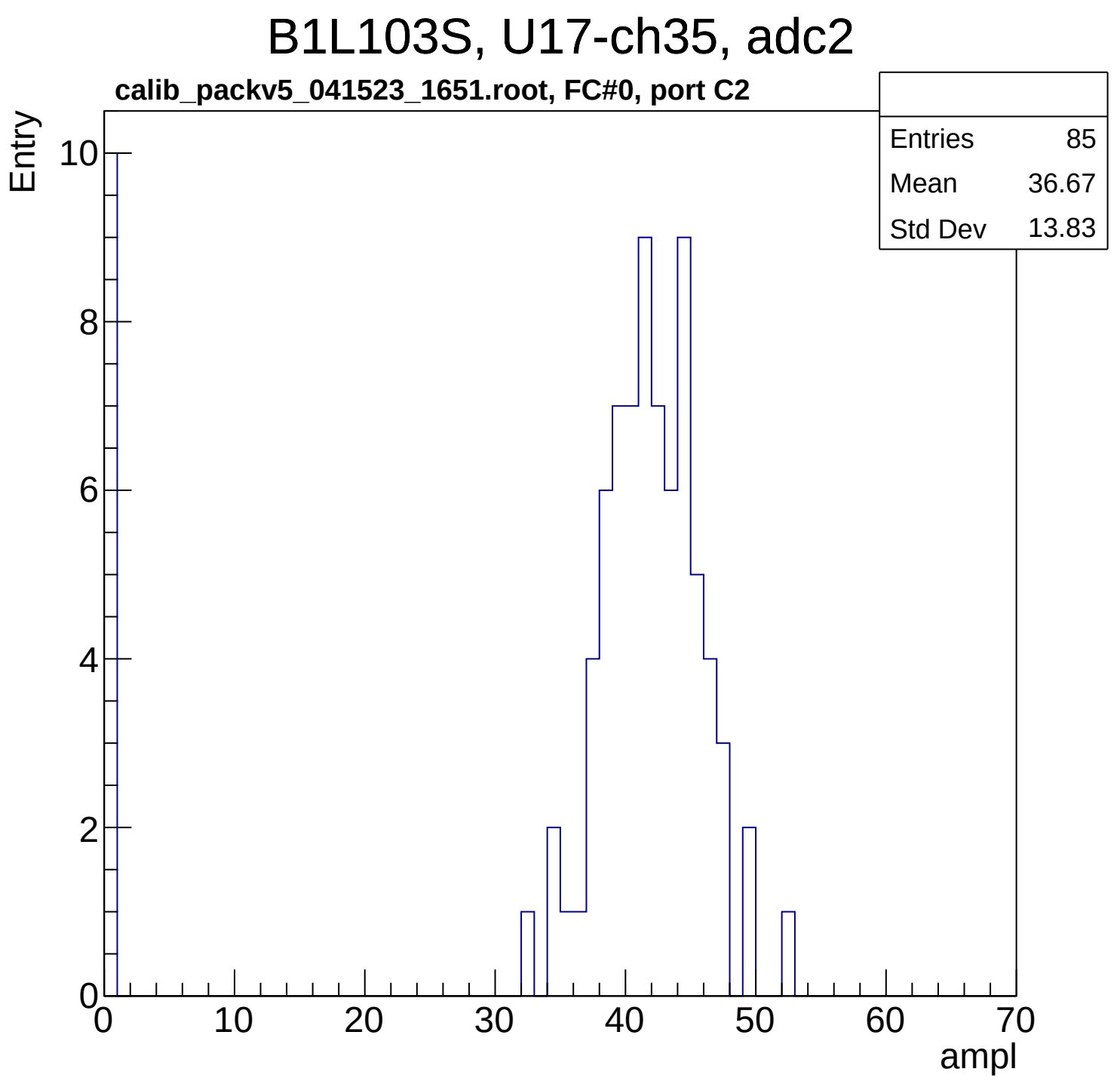
B1L103S, U17-ch35, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 36.67
Std Dev 13.83
Entry
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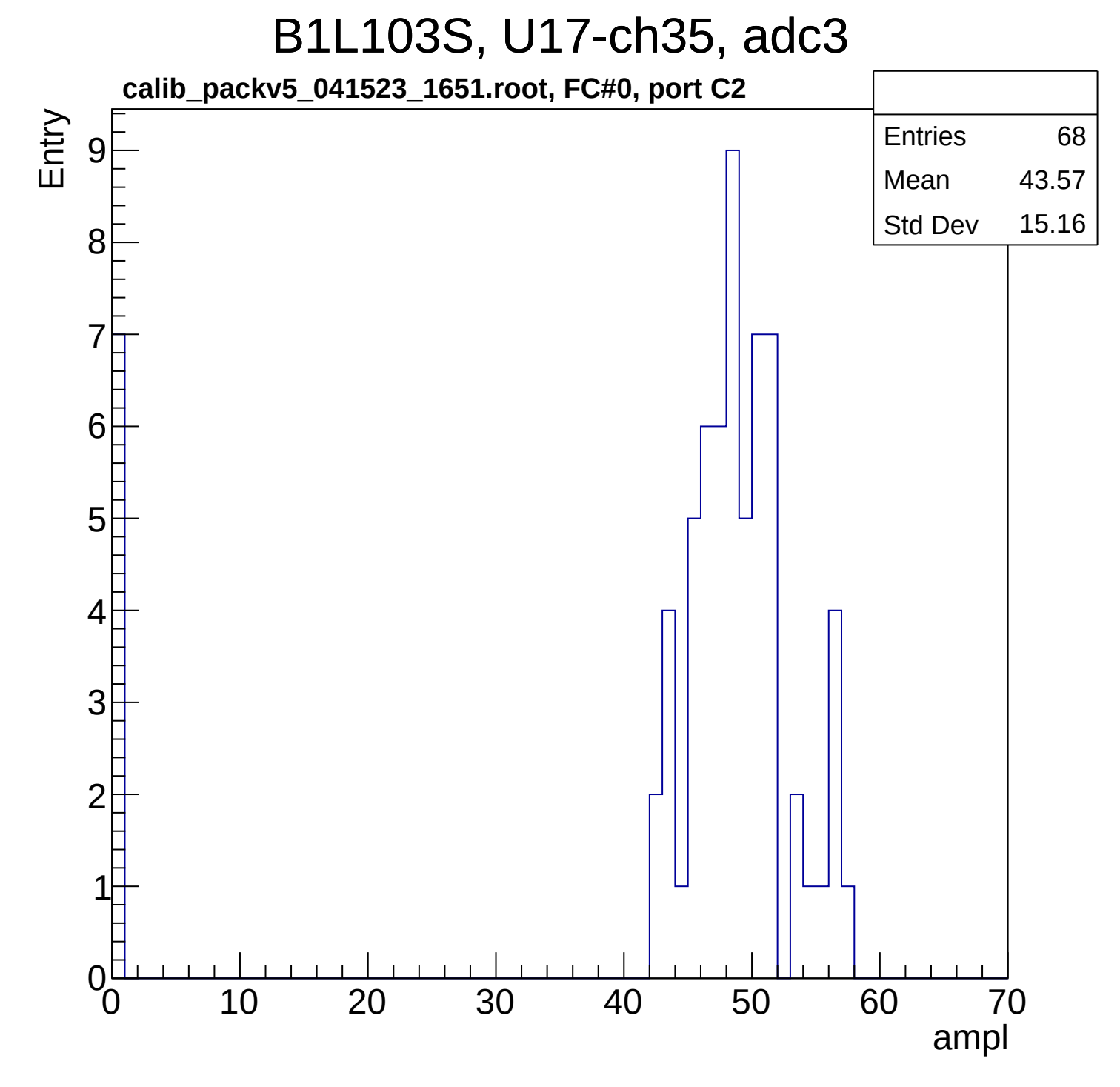
70
ampl


B1L103S, U17-ch35, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 43.57
Std Dev 15.16
Entry
ampl
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9
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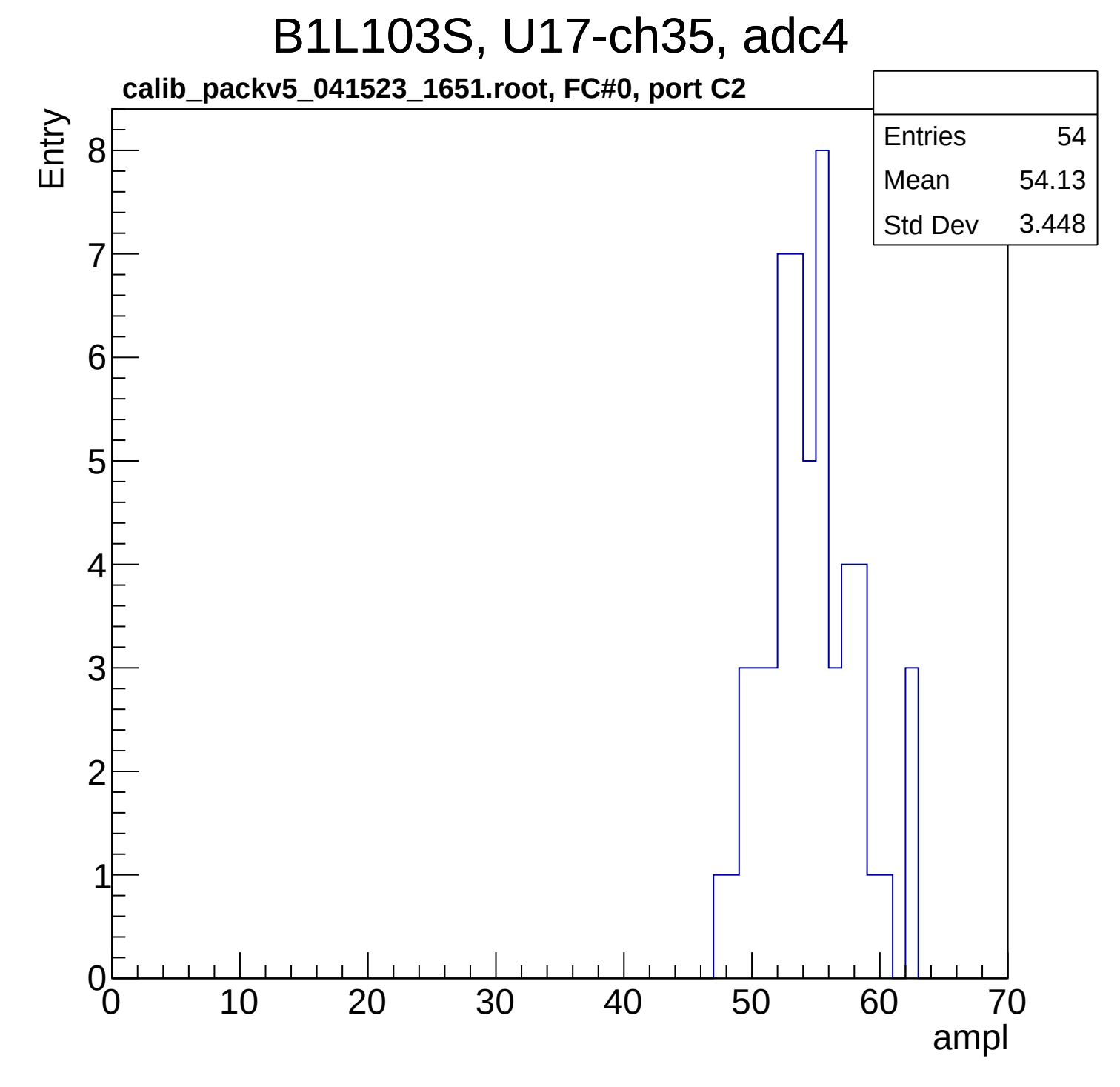
B1L103S, U17-ch35, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 54.13
Std Dev 3.448
Entry
ampl
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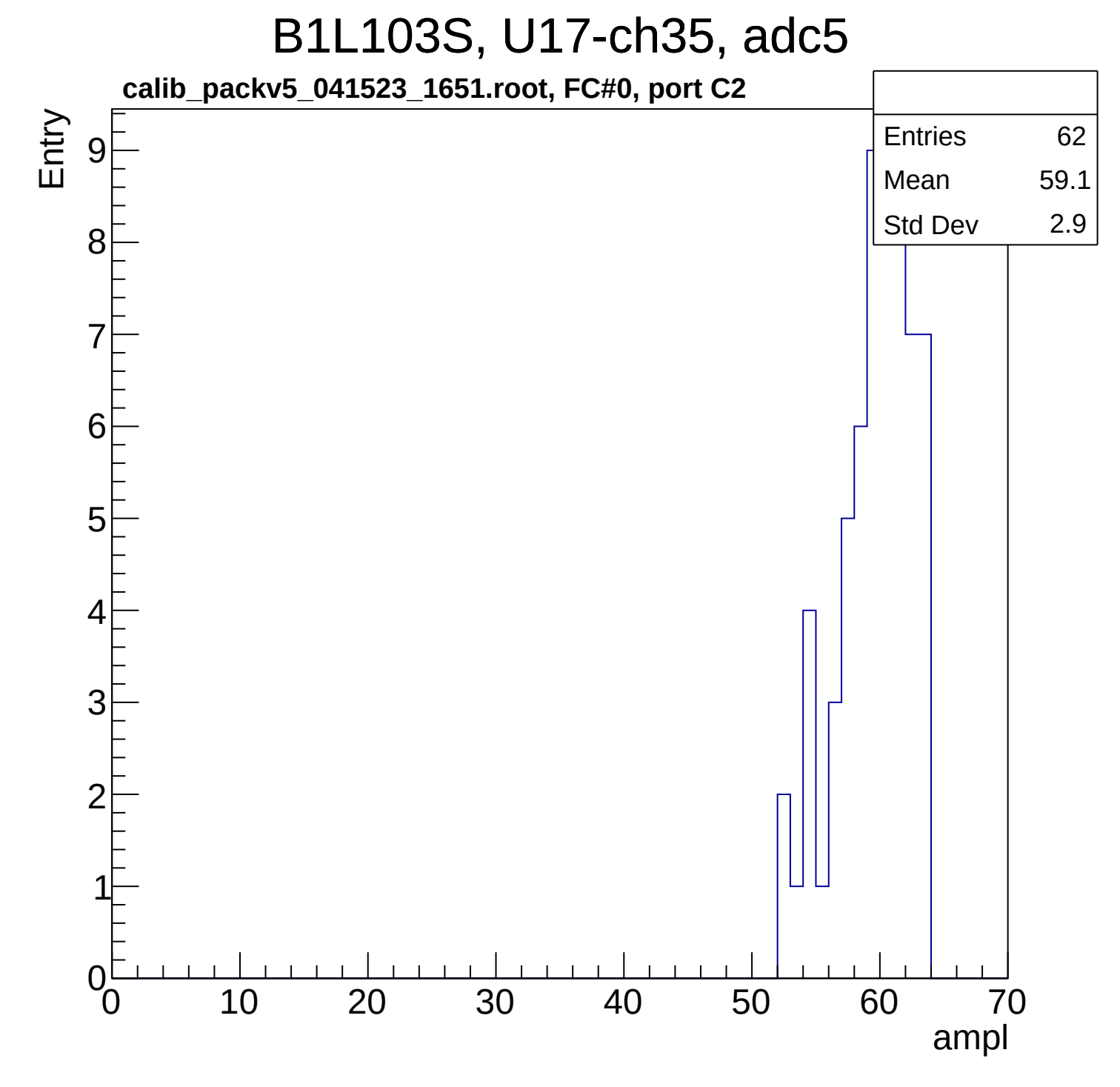
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U17-ch35, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 59.1
Std Dev 2.9
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
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40
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60
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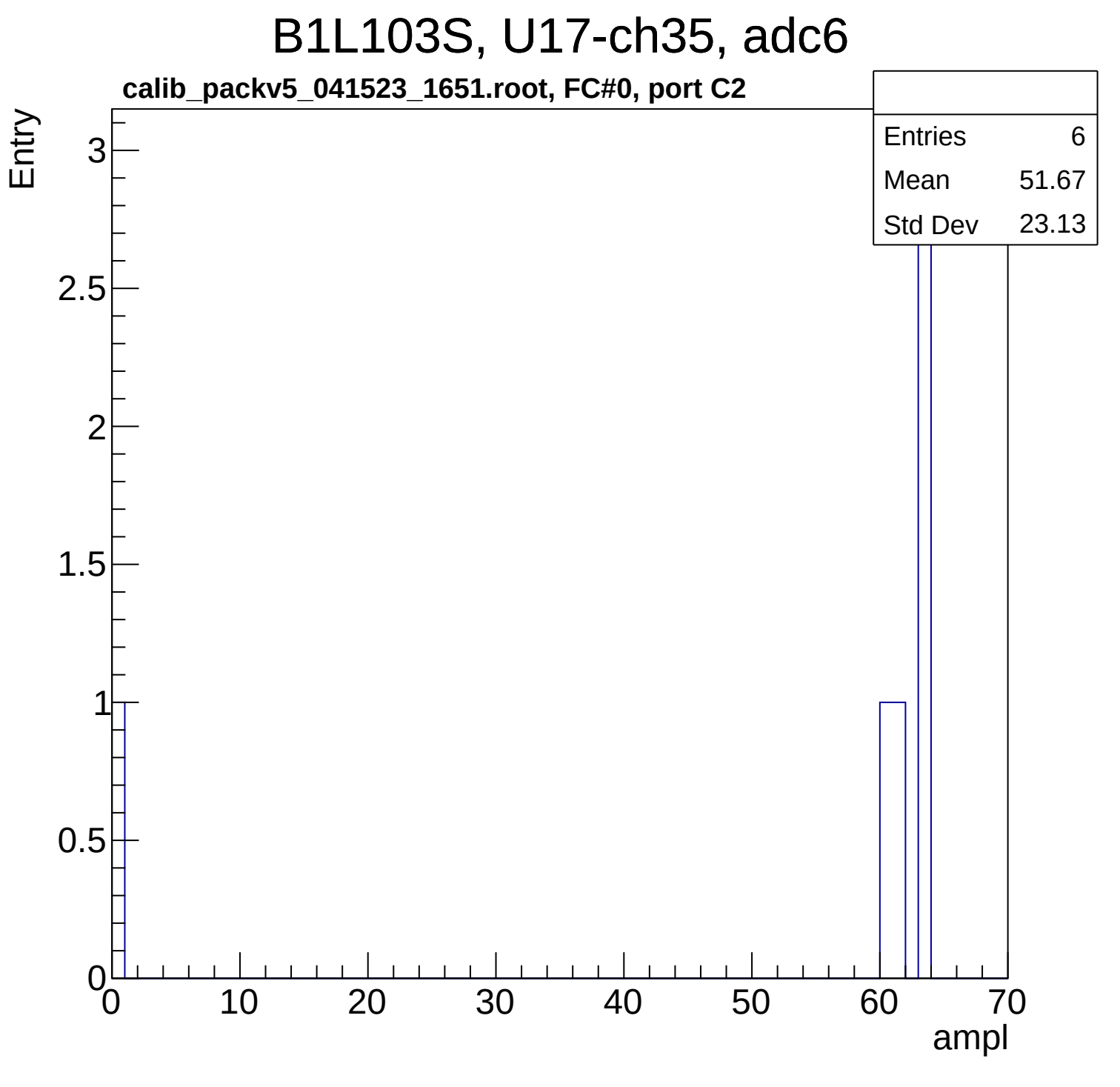
B1L103S, U17-ch35, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 51.67
Std Dev 23.13
Entry
ampl
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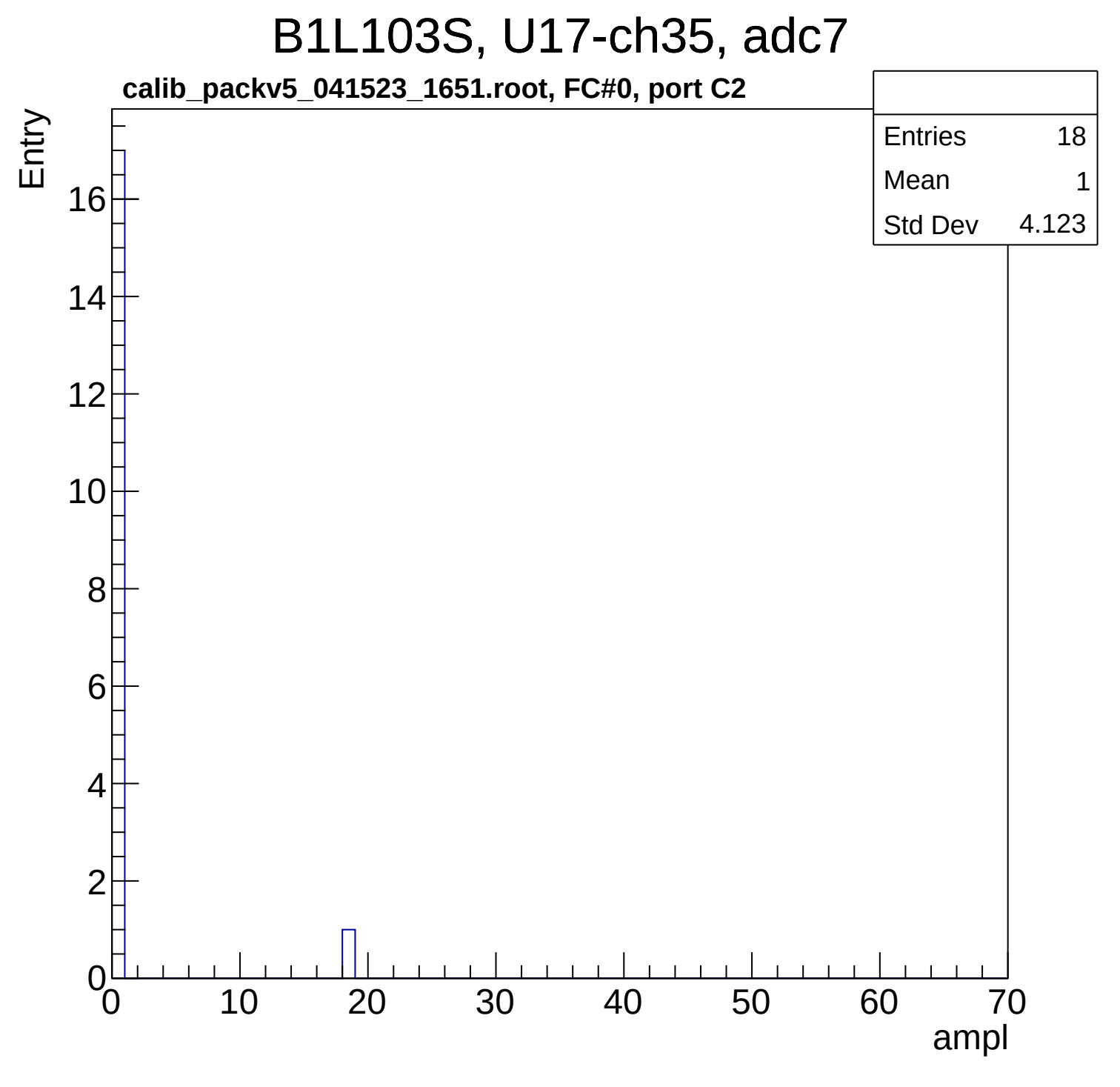
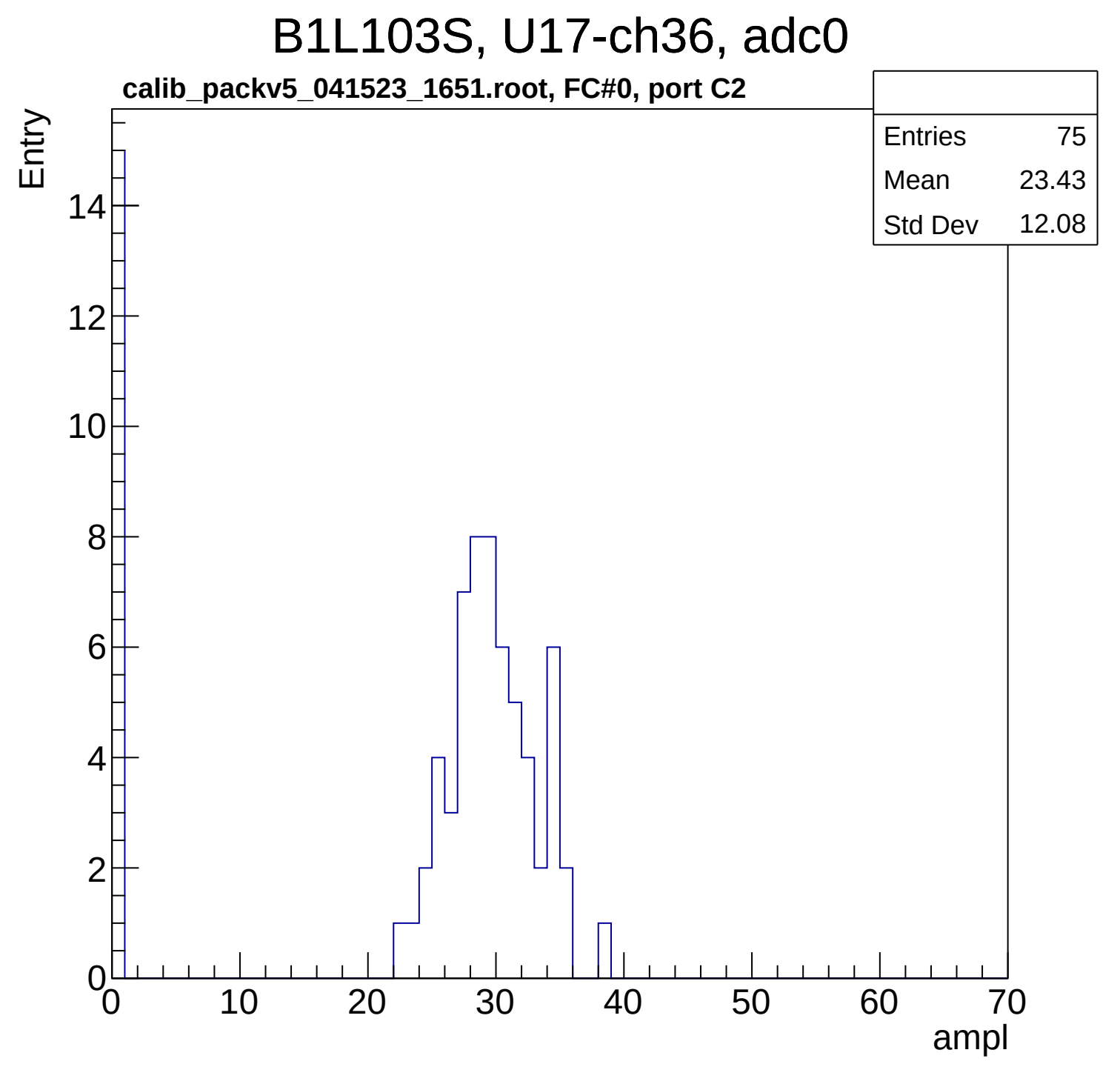
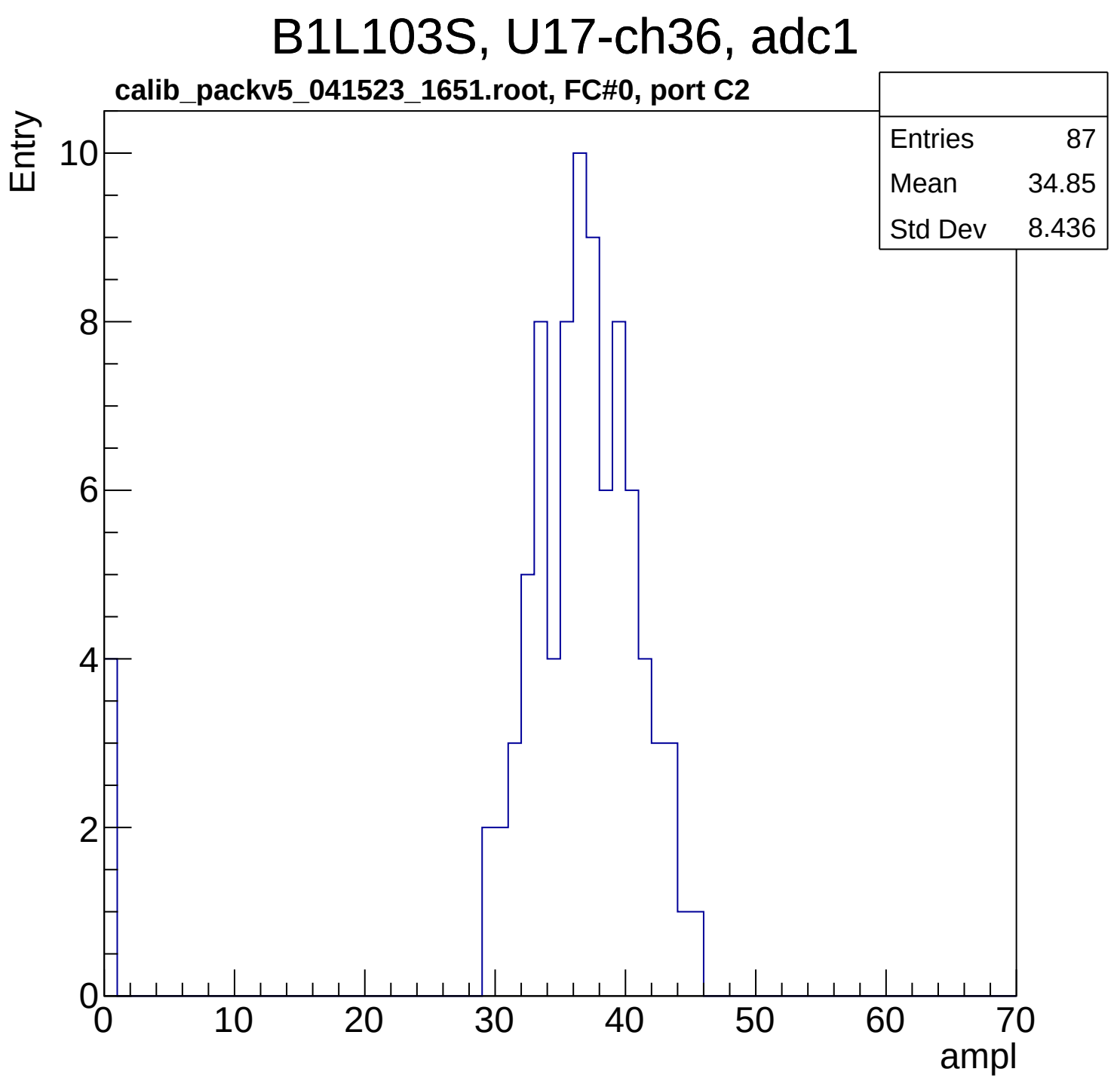
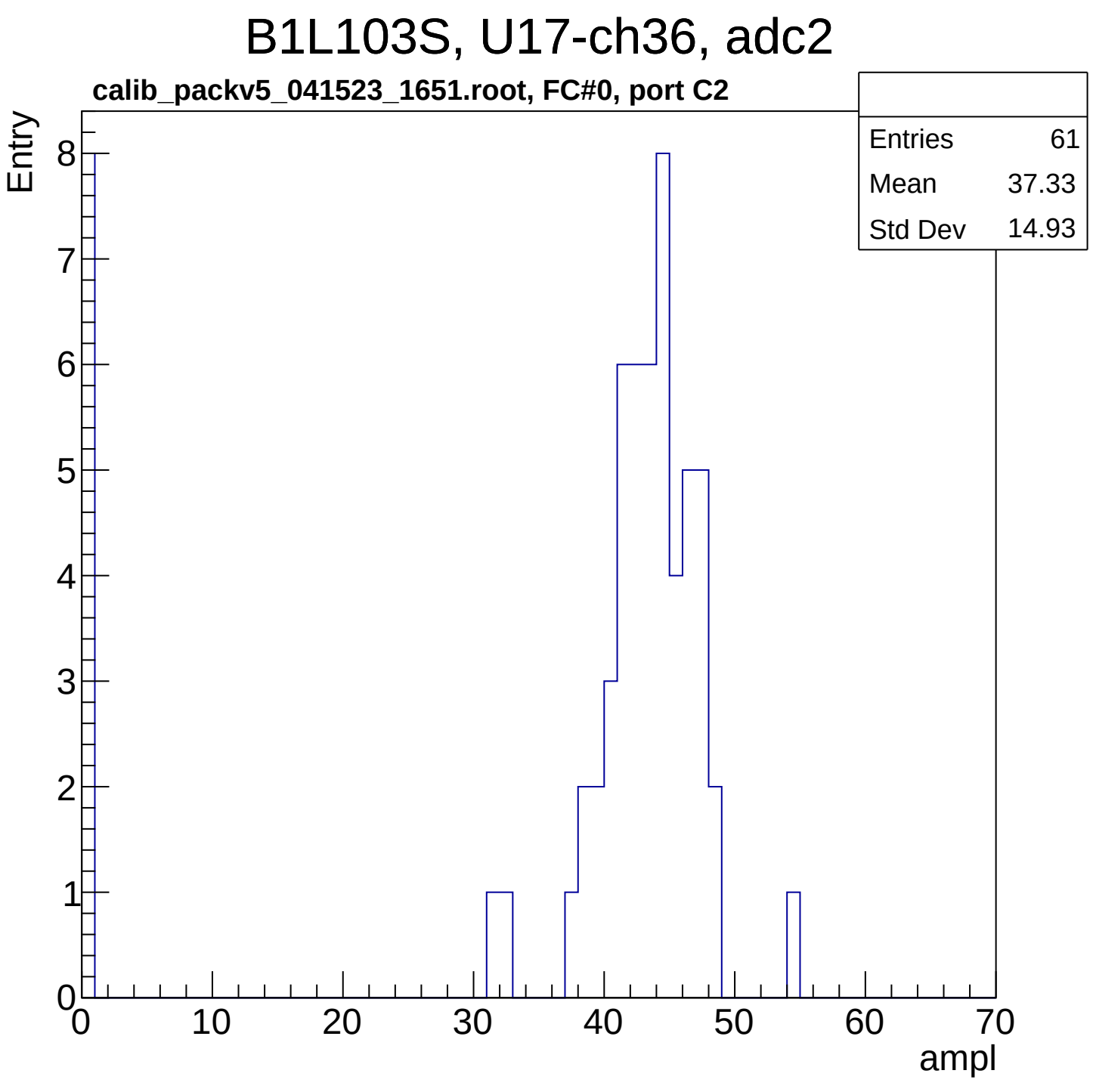
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U17-ch35, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 1
Std Dev 4.123
Entry
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch36, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 23.43
Std Dev 12.08
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch36, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 87
Mean 34.85
Std Dev 8.436
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch36, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 37.33
Std Dev 14.93
Entry
ampl
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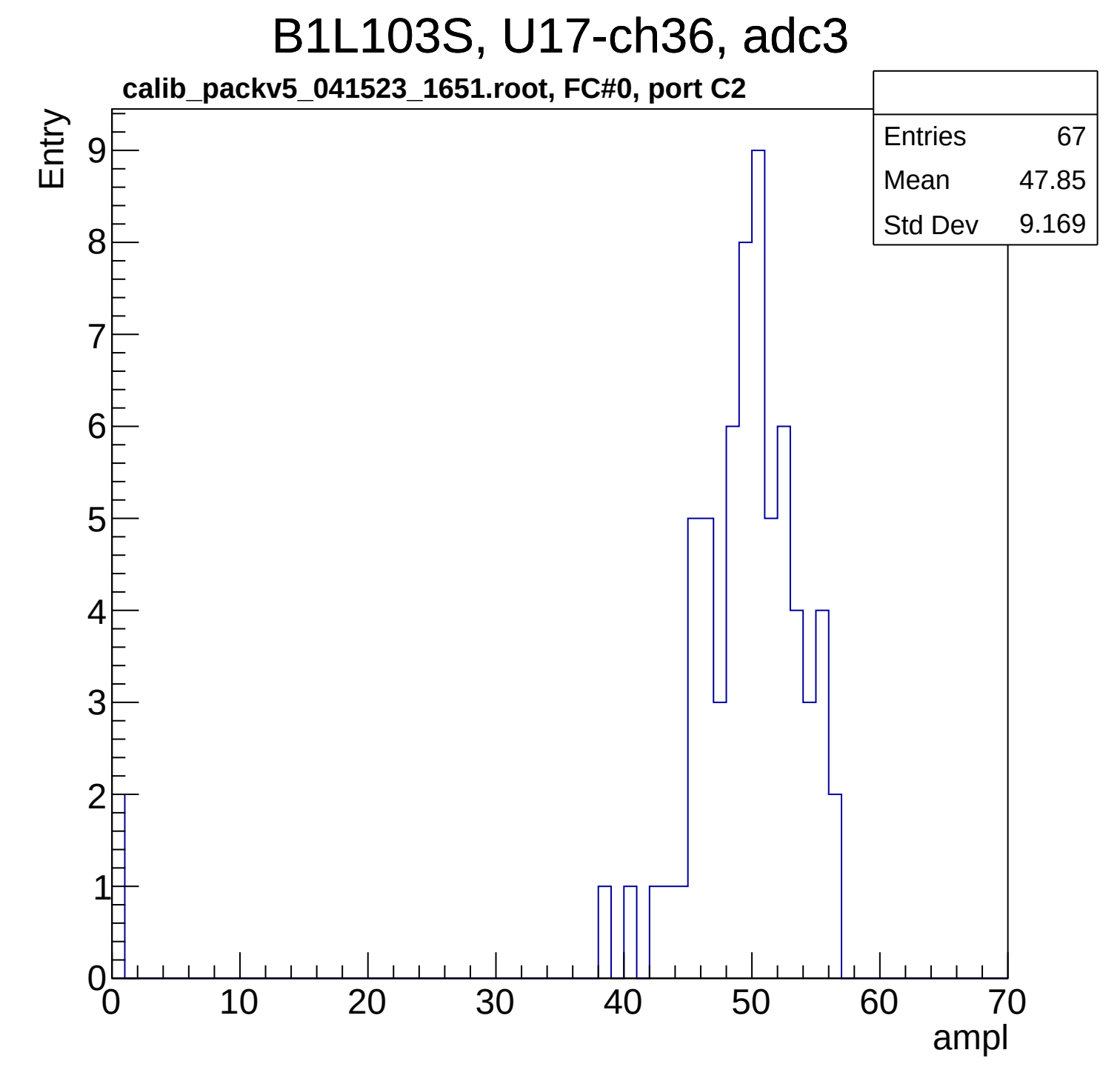
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U17-ch36, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 47.85
Std Dev 9.169
Entry
ampl
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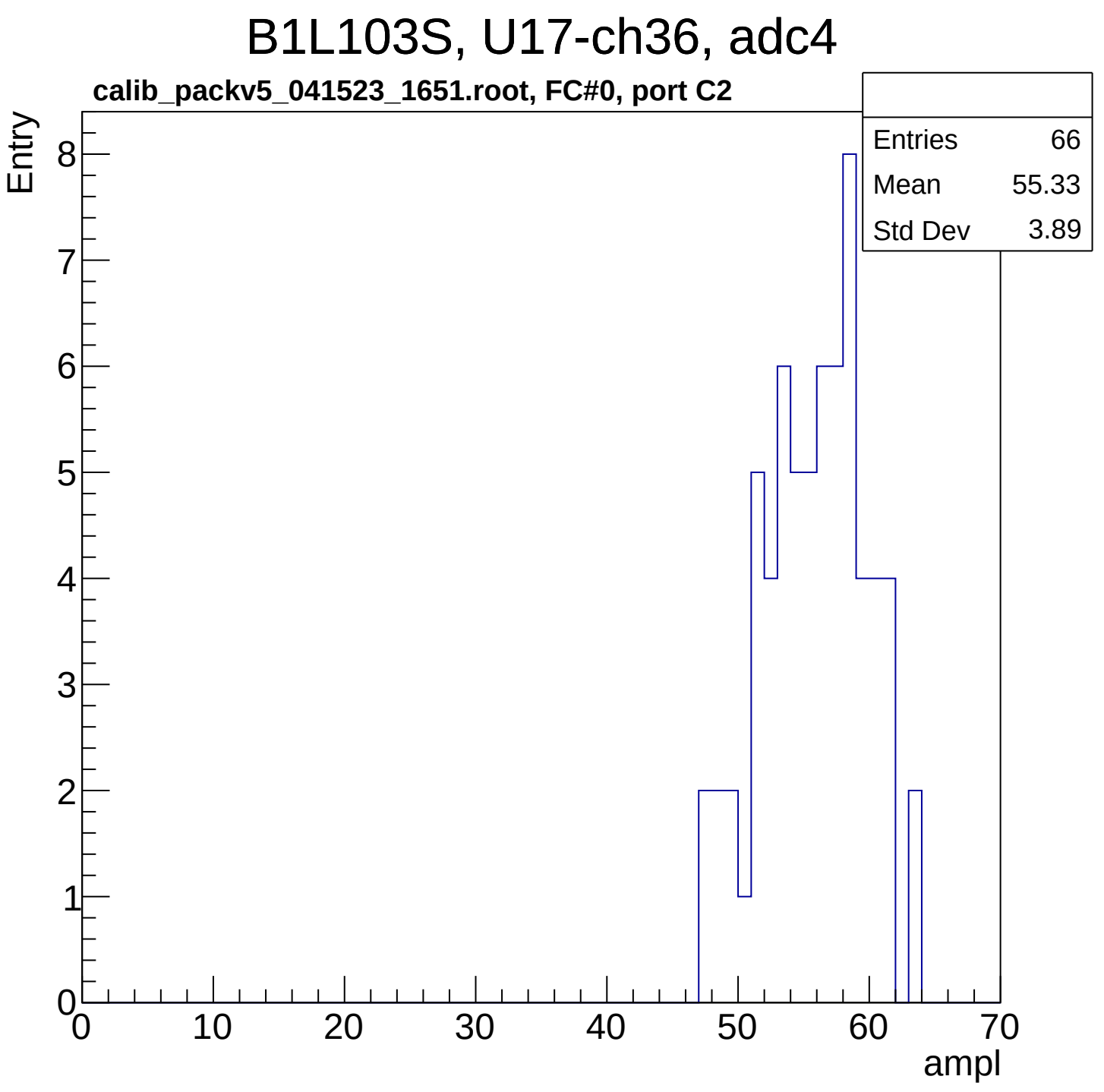
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9


B1L103S, U17-ch36, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 55.33
Std Dev 3.89
Entry
ampl
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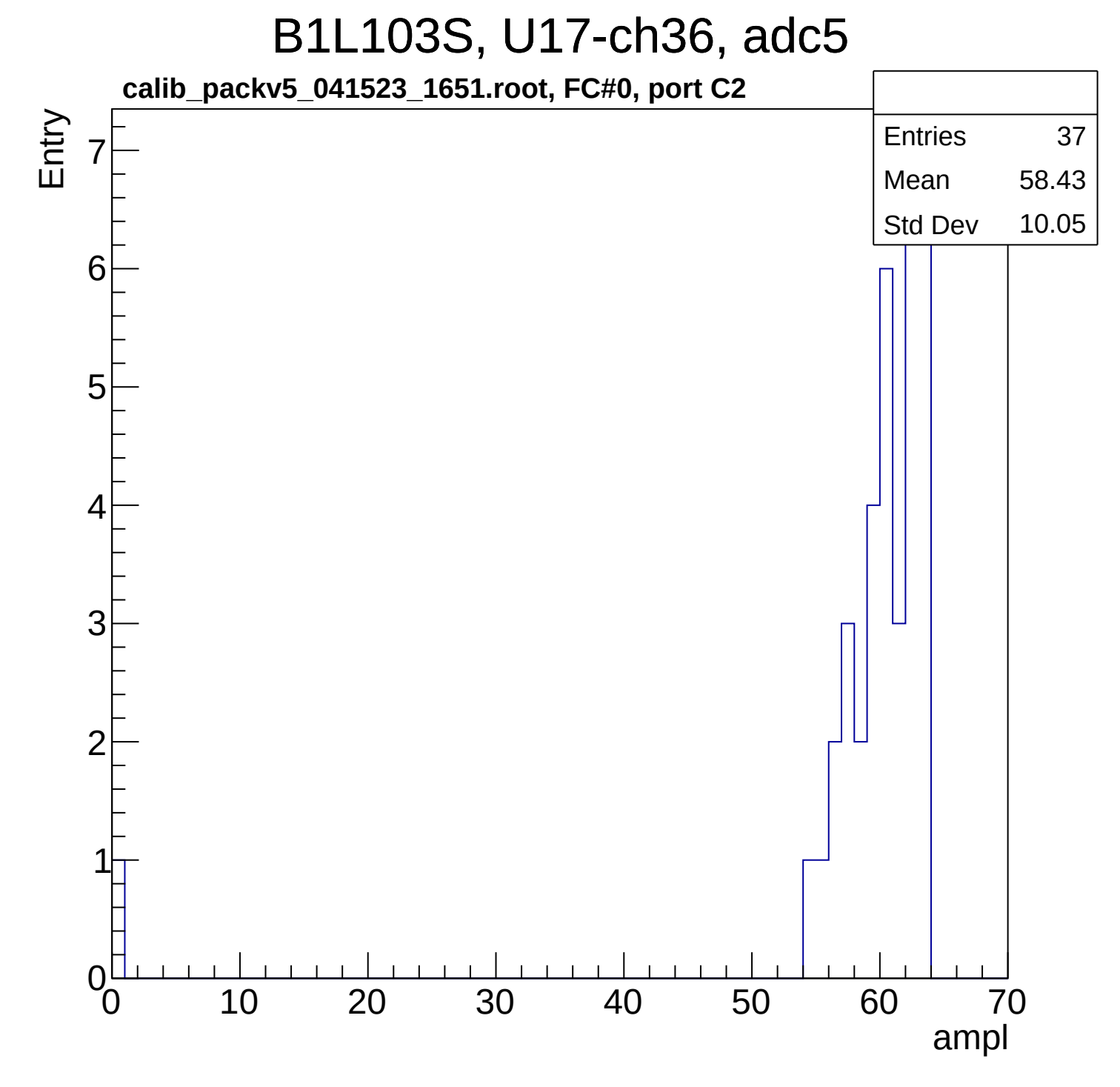
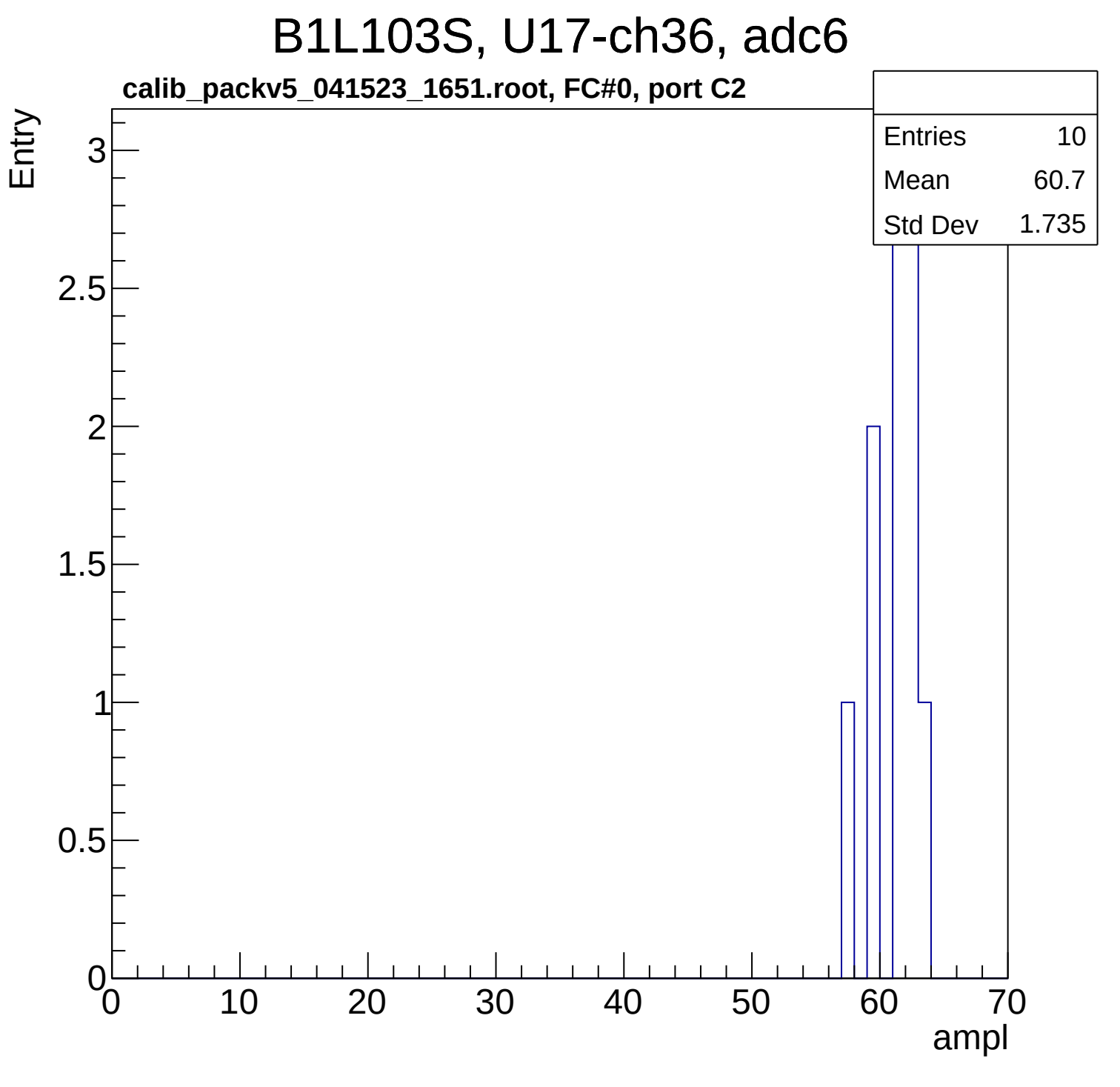
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U17-ch36, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 37
Mean 58.43
Std Dev 10.05
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U17-ch36, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 60.7
Std Dev 1.735
Entry
ampl
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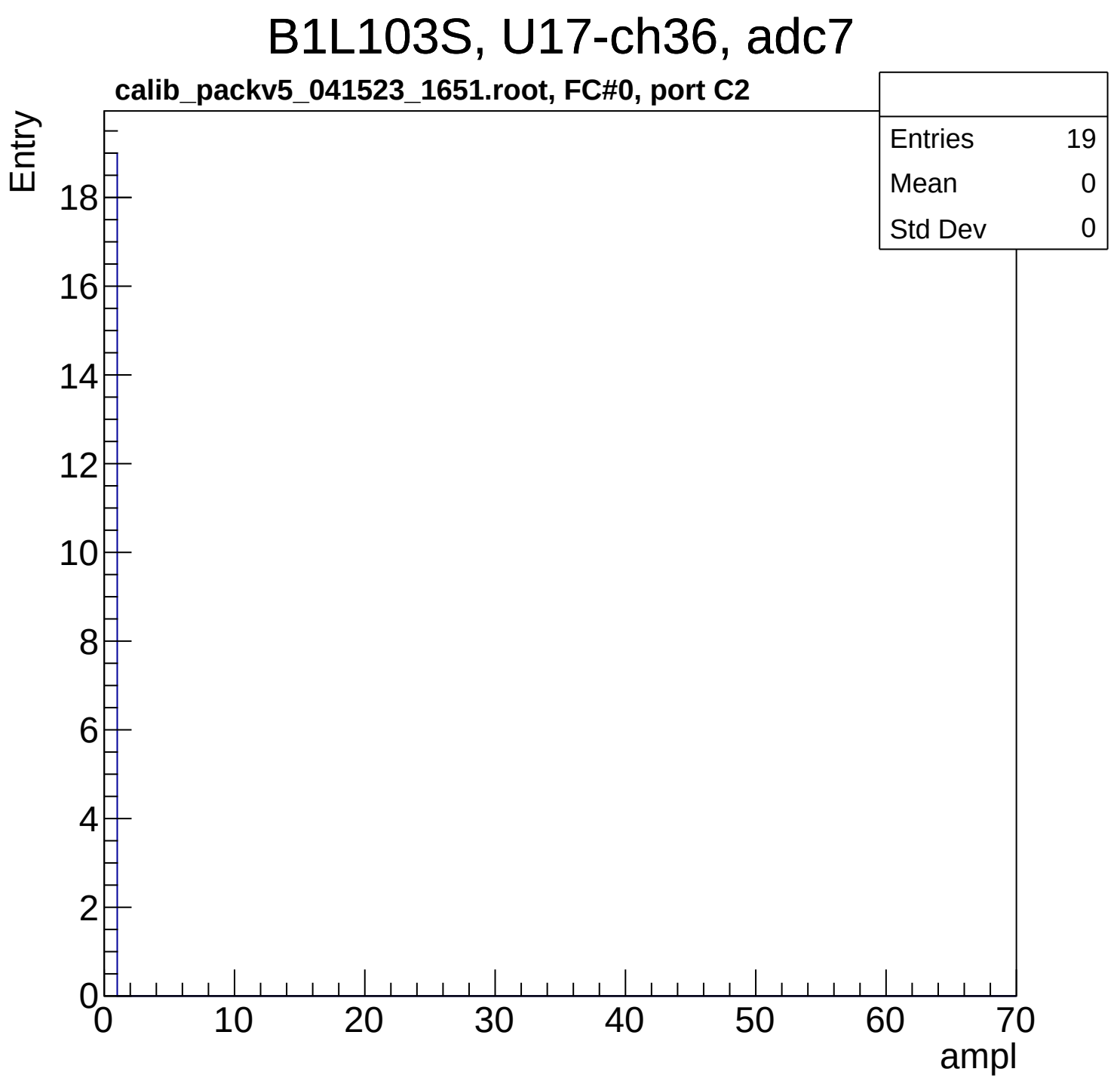
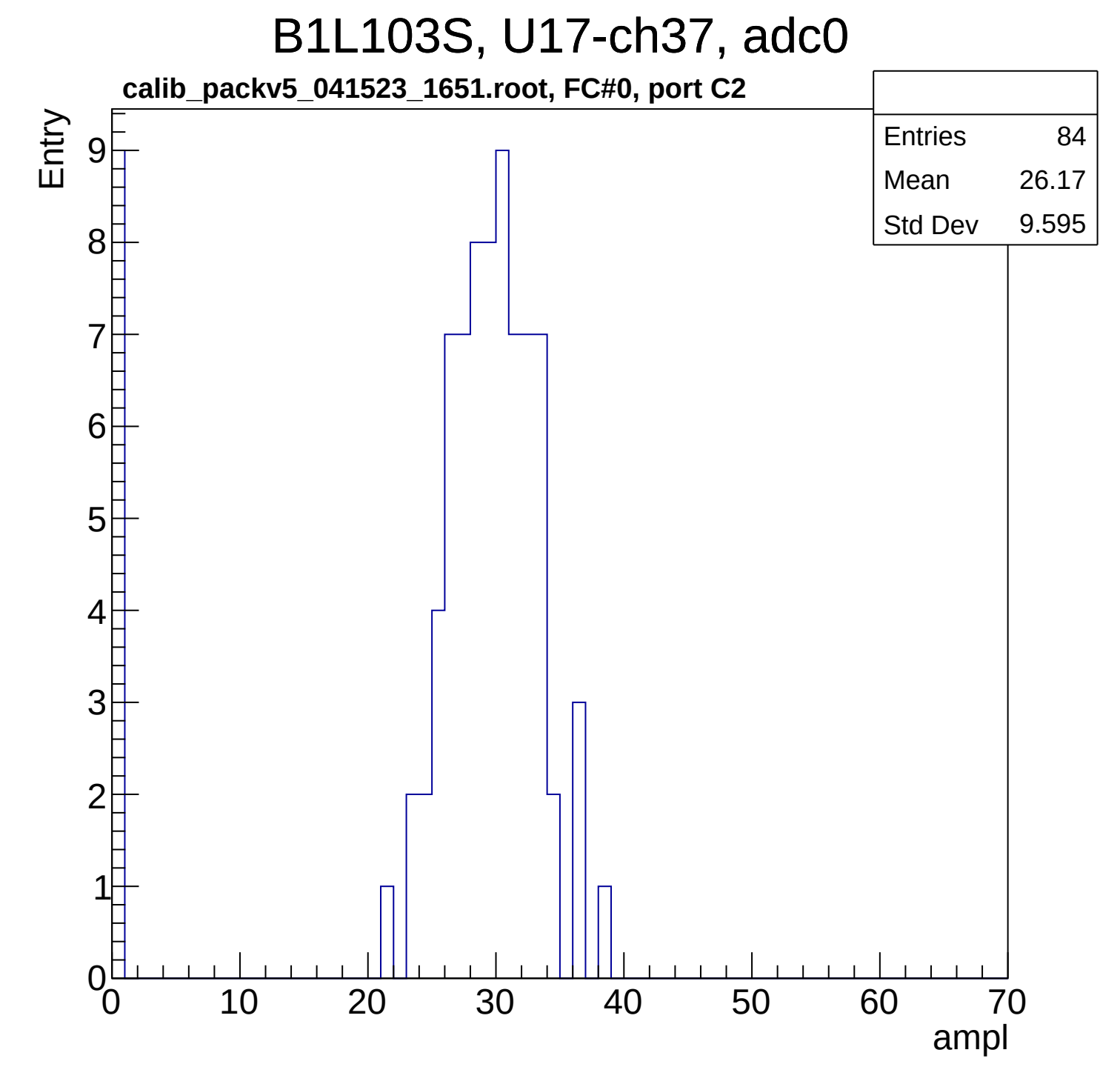
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U17-ch36, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch37, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 26.17
Std Dev 9.595
Entry
ampl
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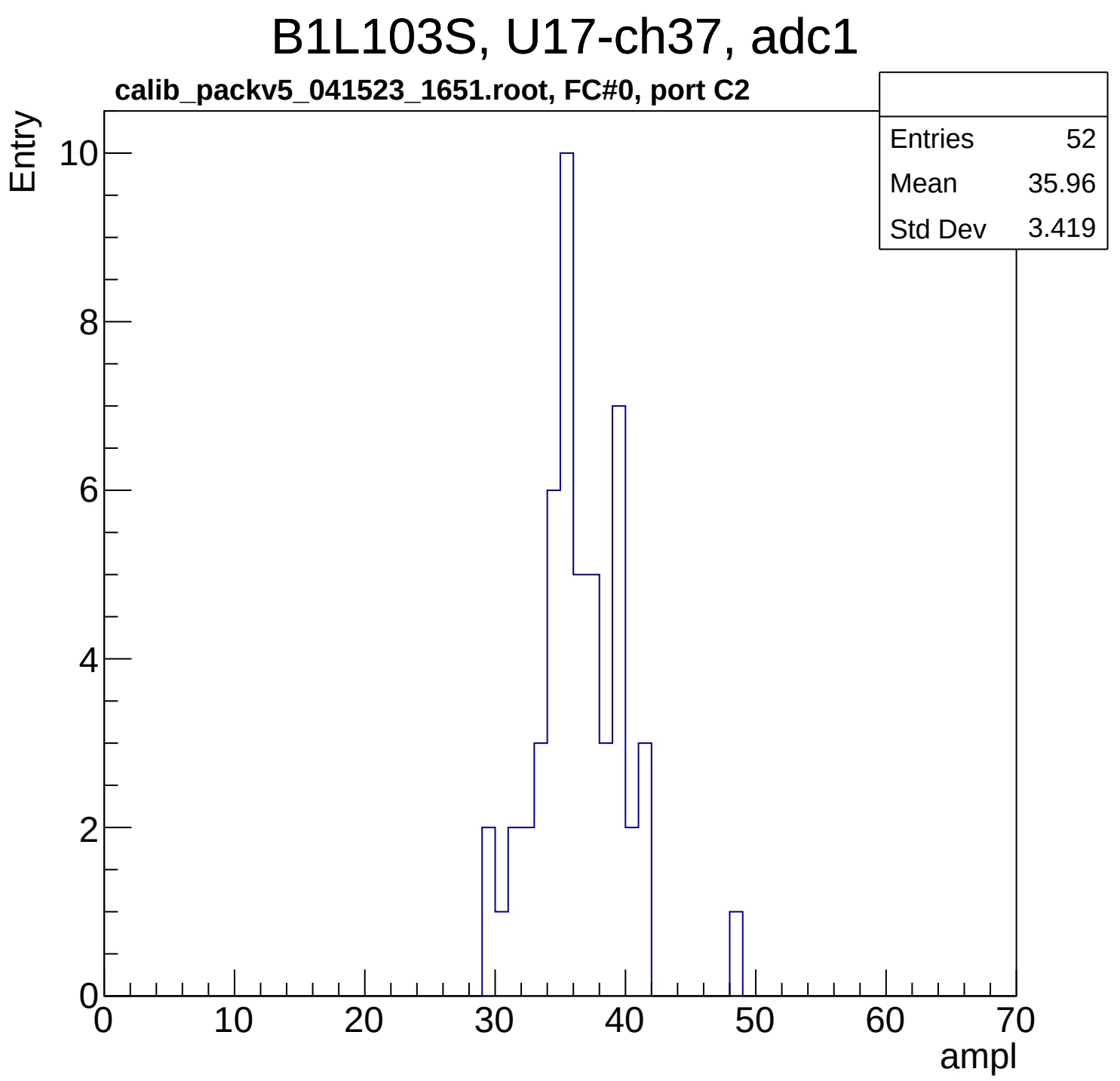
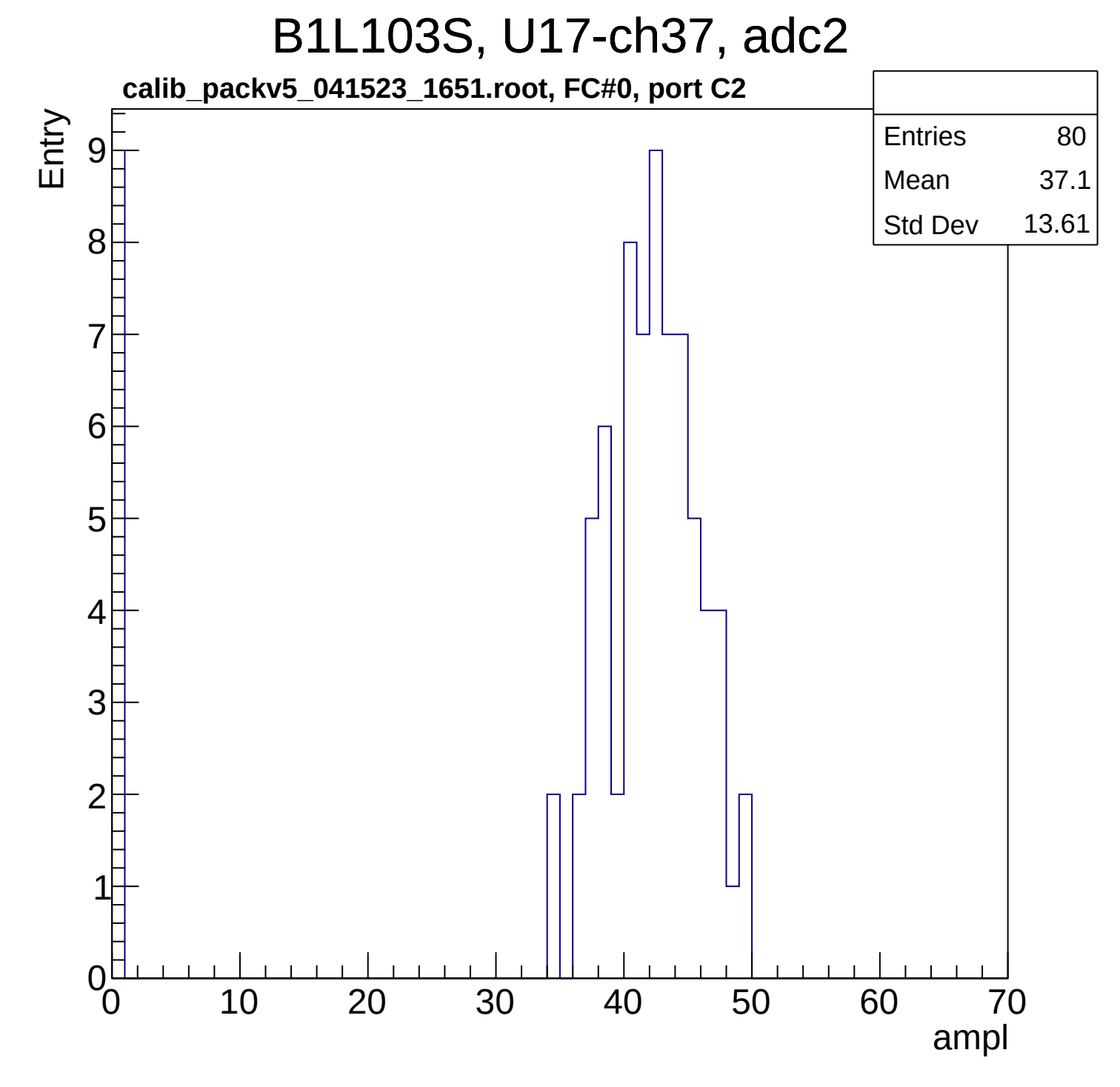
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U17-ch37, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 35.96
Std Dev 3.419
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U17-ch37, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 37.1
Std Dev 13.61
Entry
ampl
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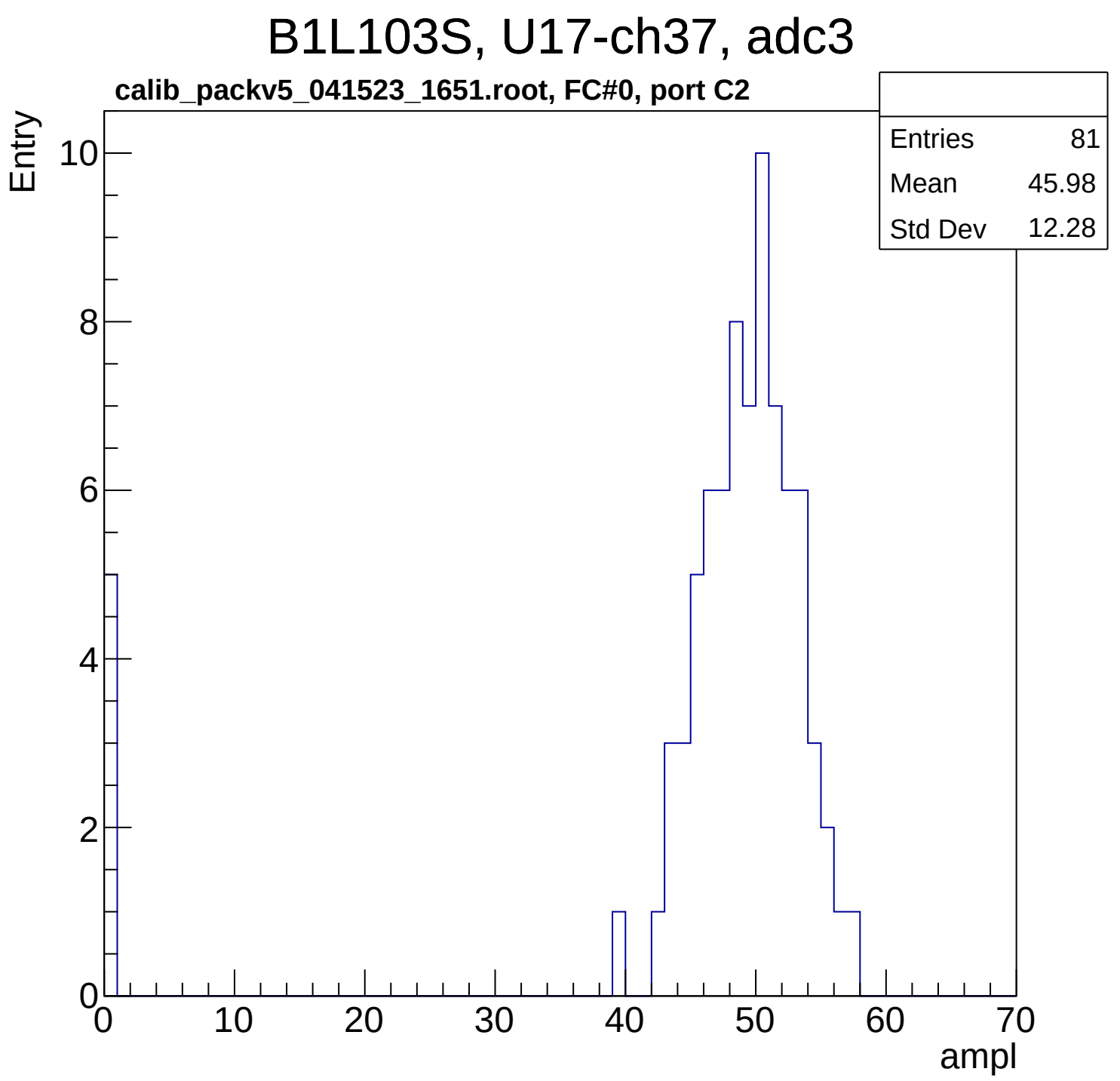
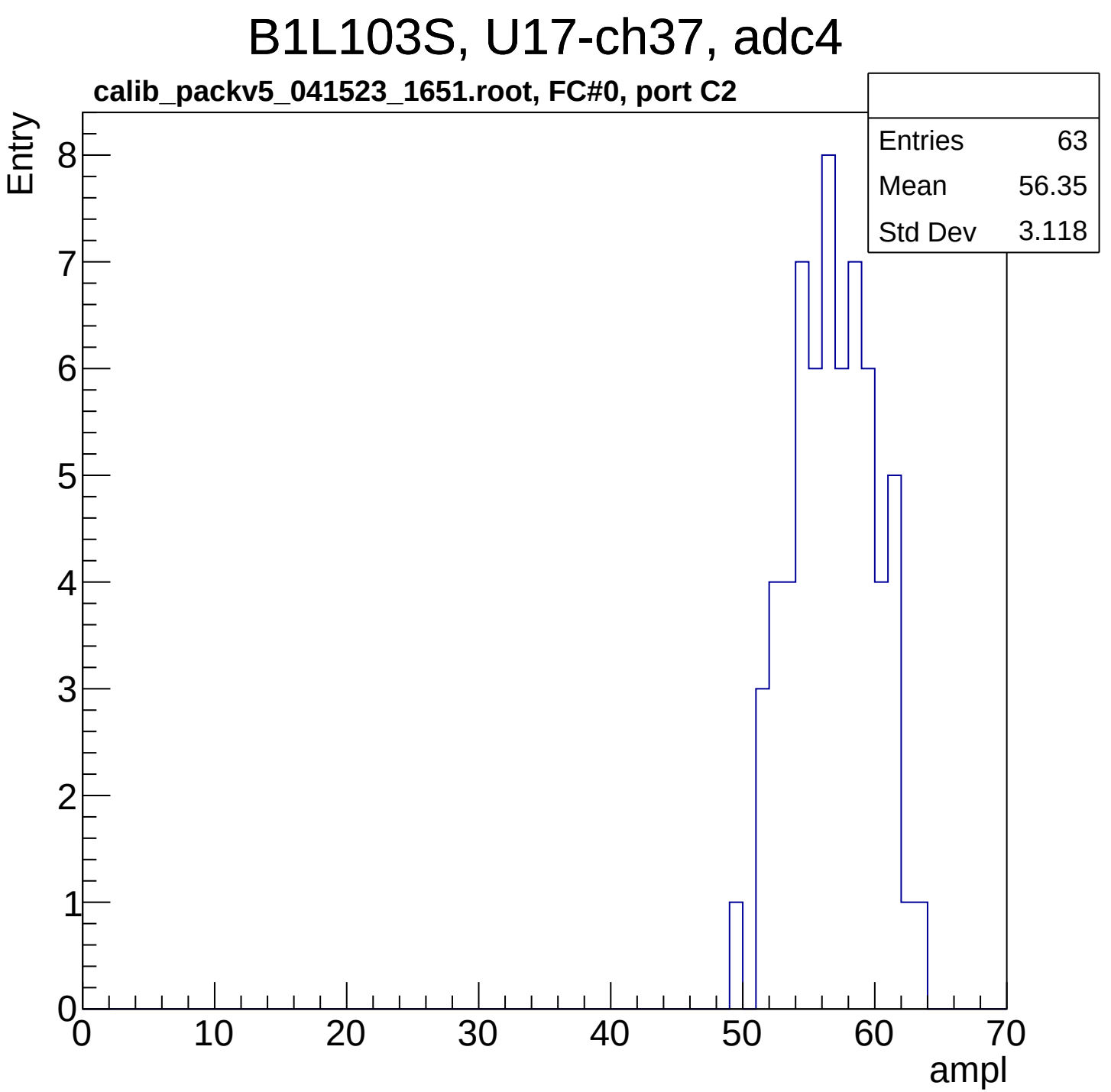
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U17-ch37, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 45.98
Std Dev 12.28
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch37, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 56.35
Std Dev 3.118
Entry
ampl
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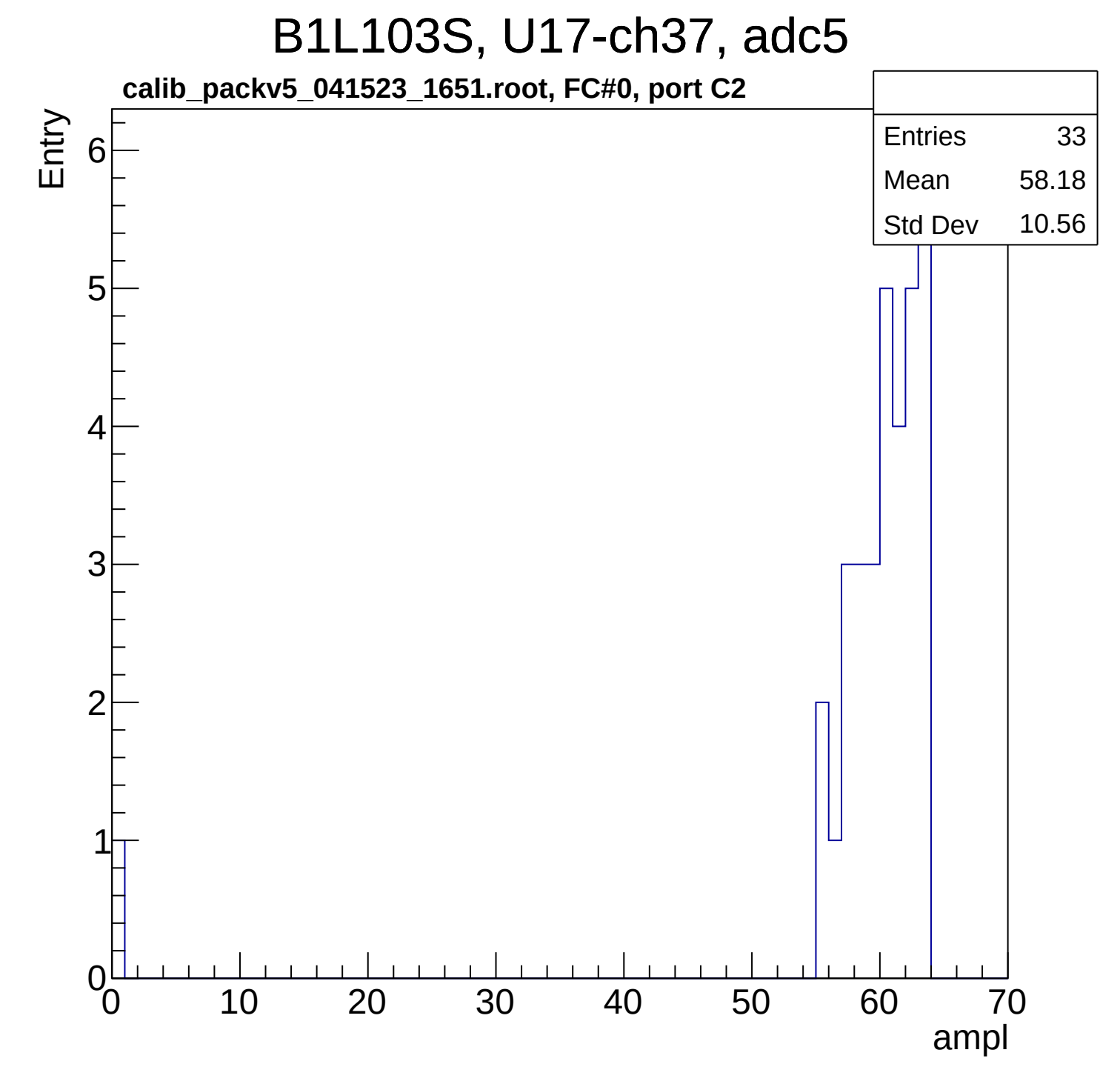
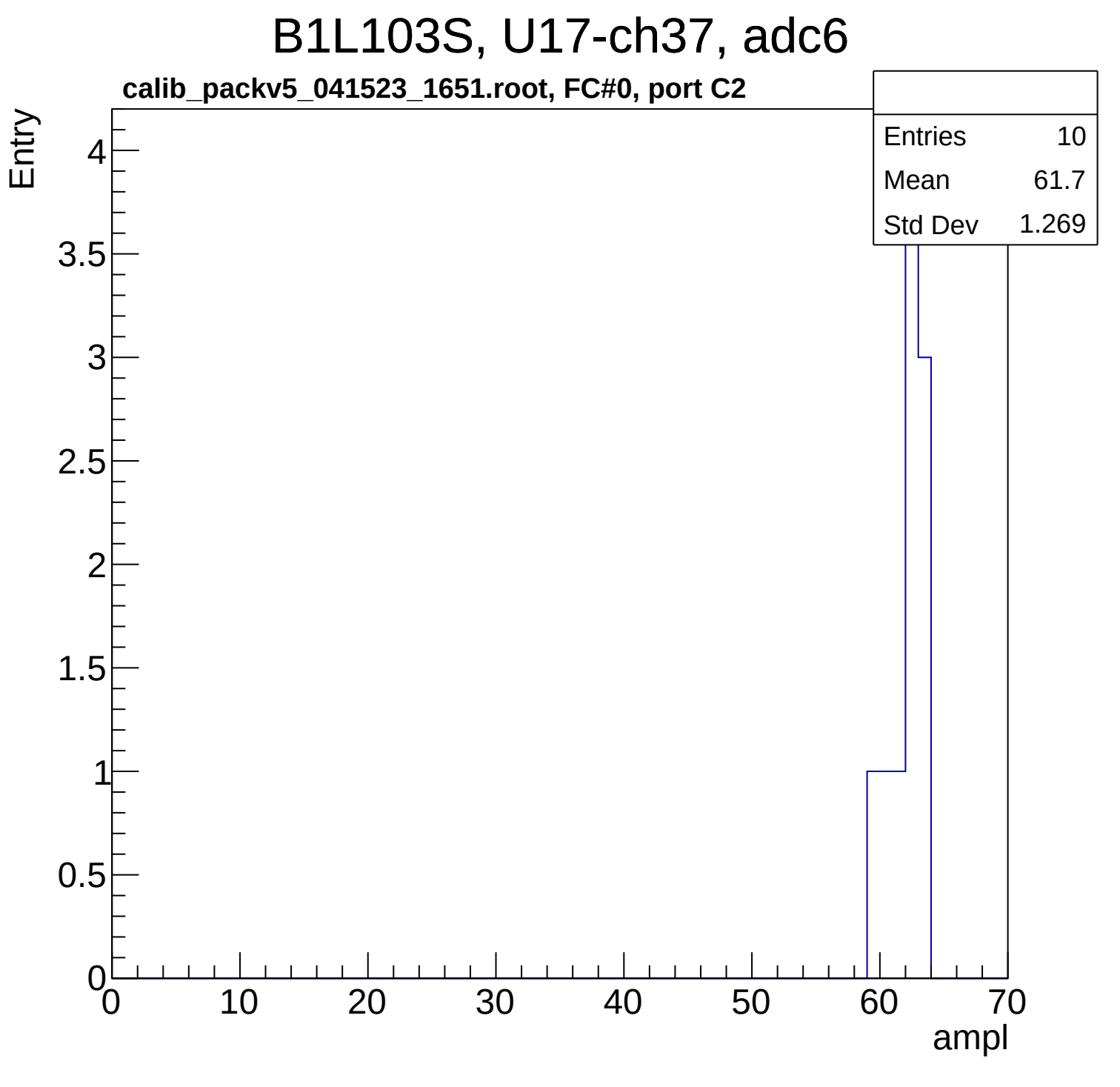
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U17-ch37, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 33
Mean 58.18
Std Dev 10.56
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U17-ch37, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 61.7
Std Dev 1.269
Entry
ampl
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0.5
1
1.5
2
2.5
3
3.5
4
0
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40
50
60
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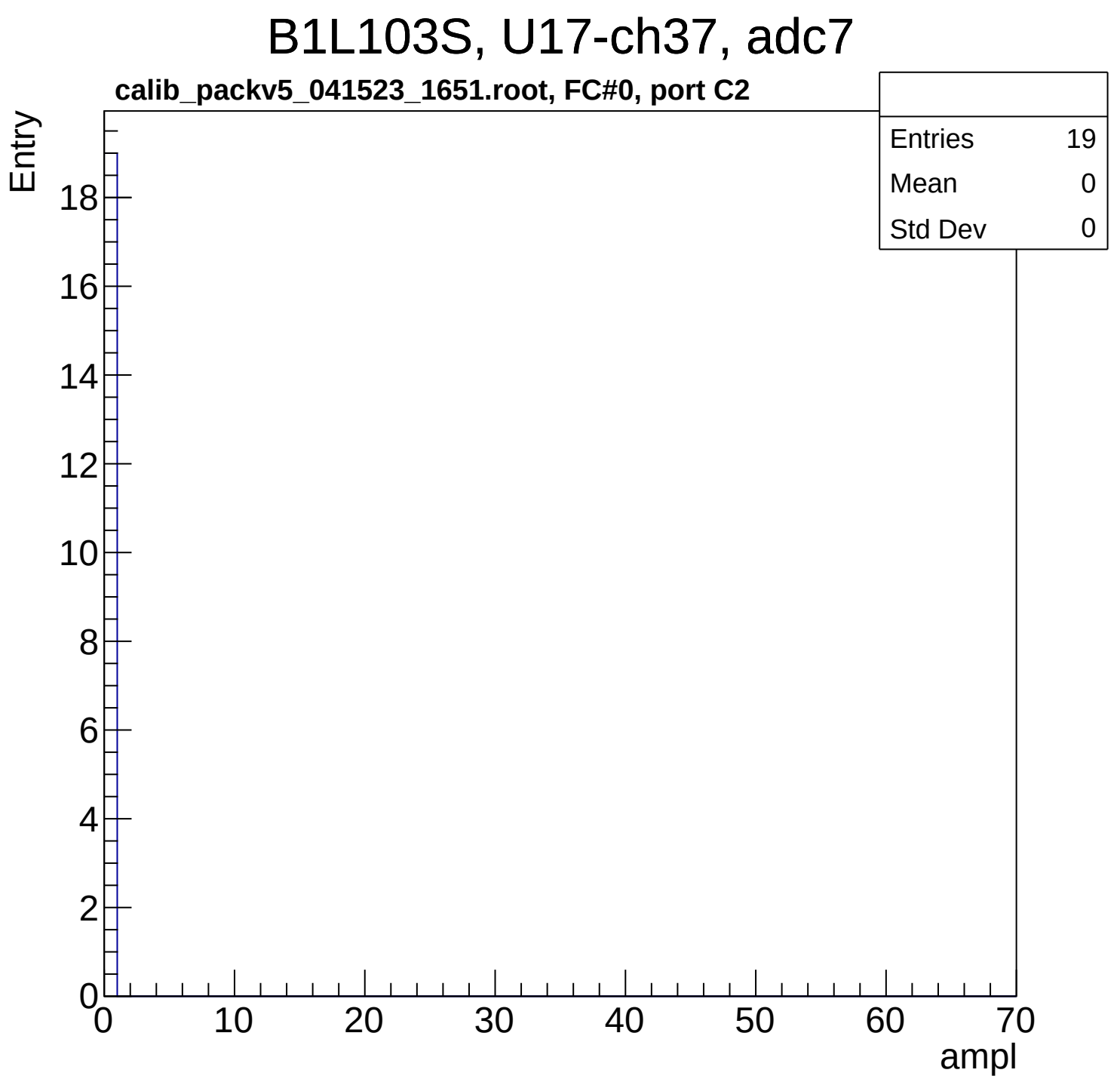
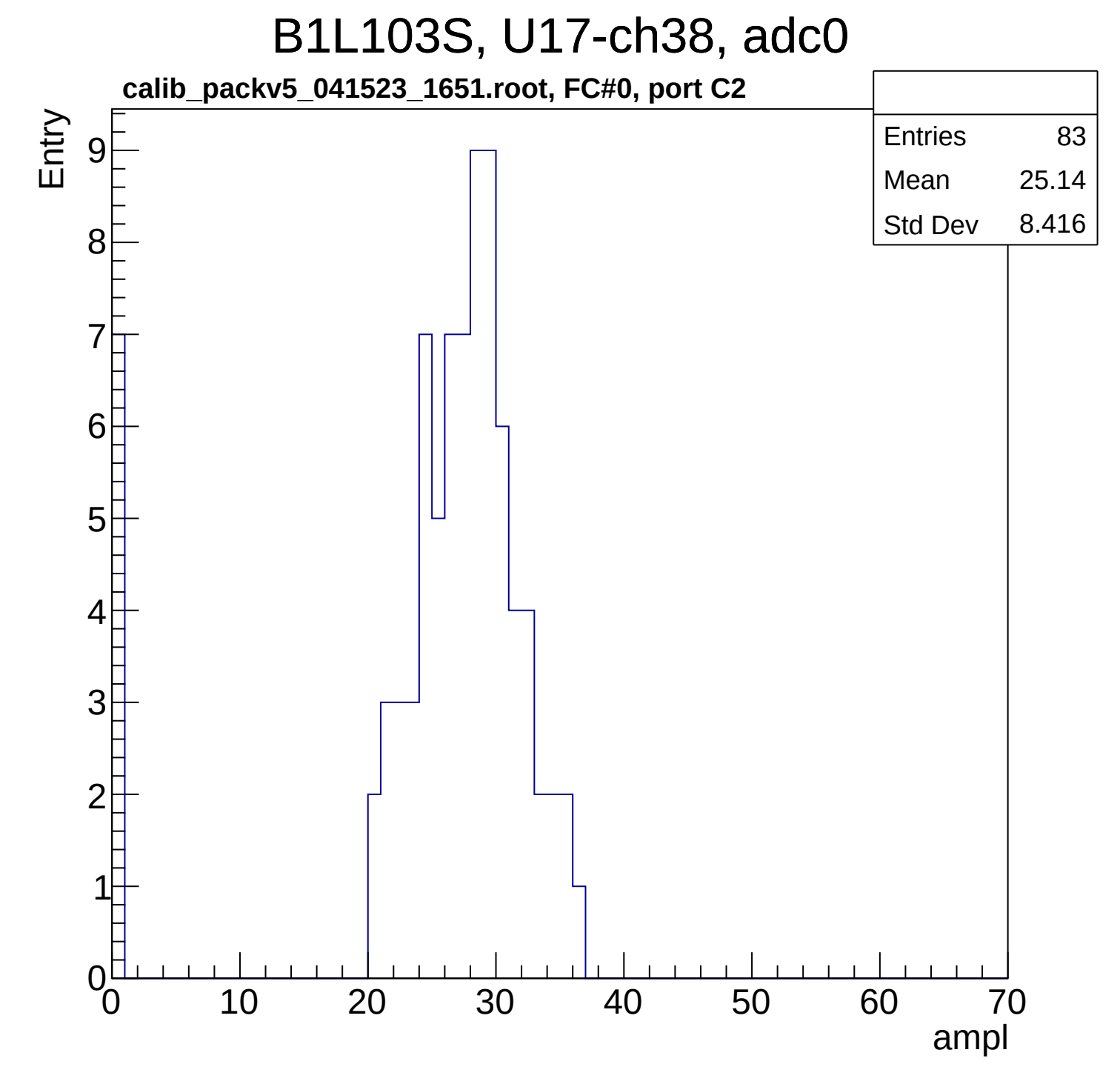

B1L103S, U17-ch37, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch38, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 25.14
Std Dev 8.416
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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50
60
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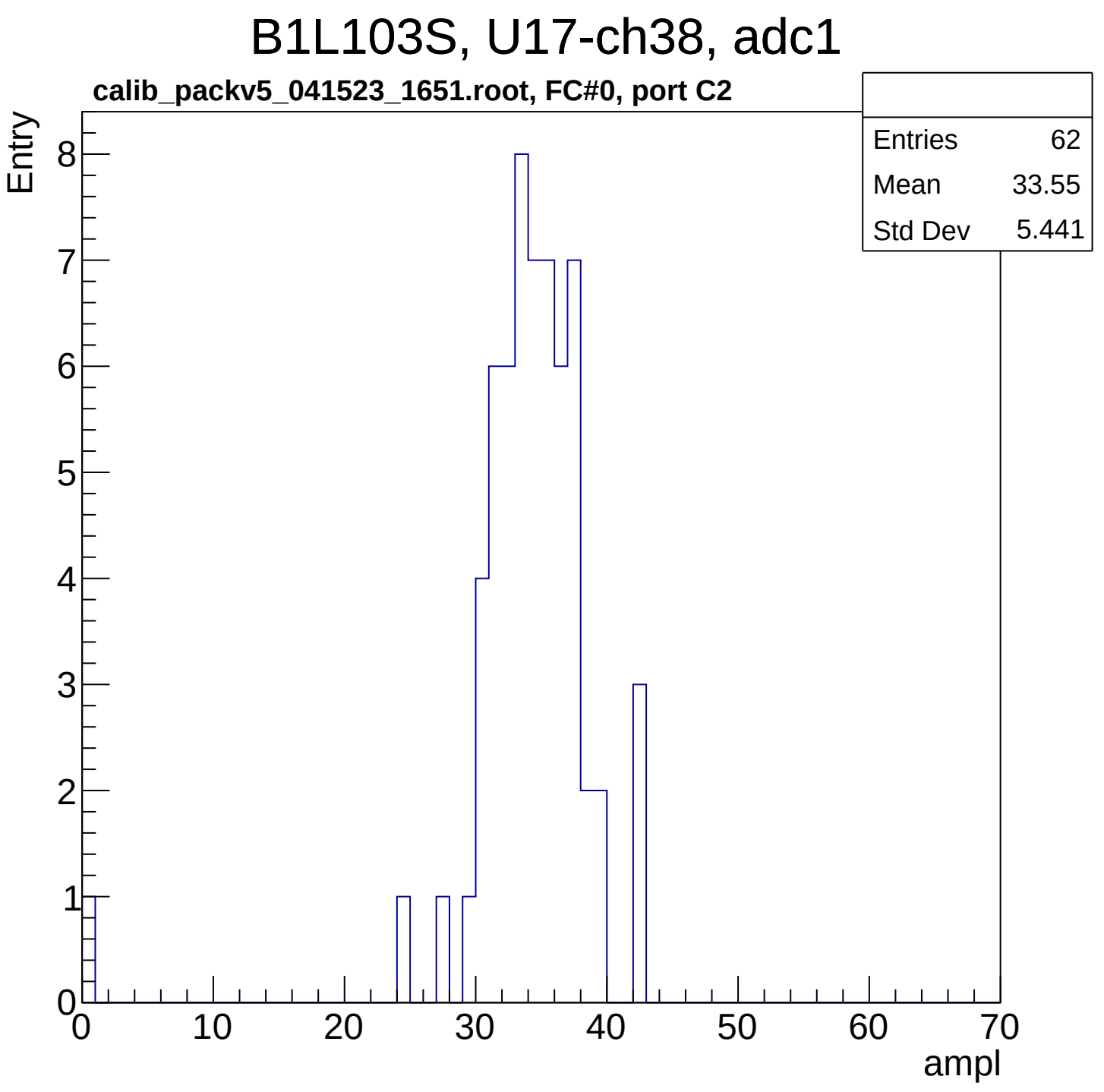
B1L103S, U17-ch38, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 33.55
Std Dev 5.441
Entry
ampl
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1
2
3
4
5
6
7
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0
10
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60
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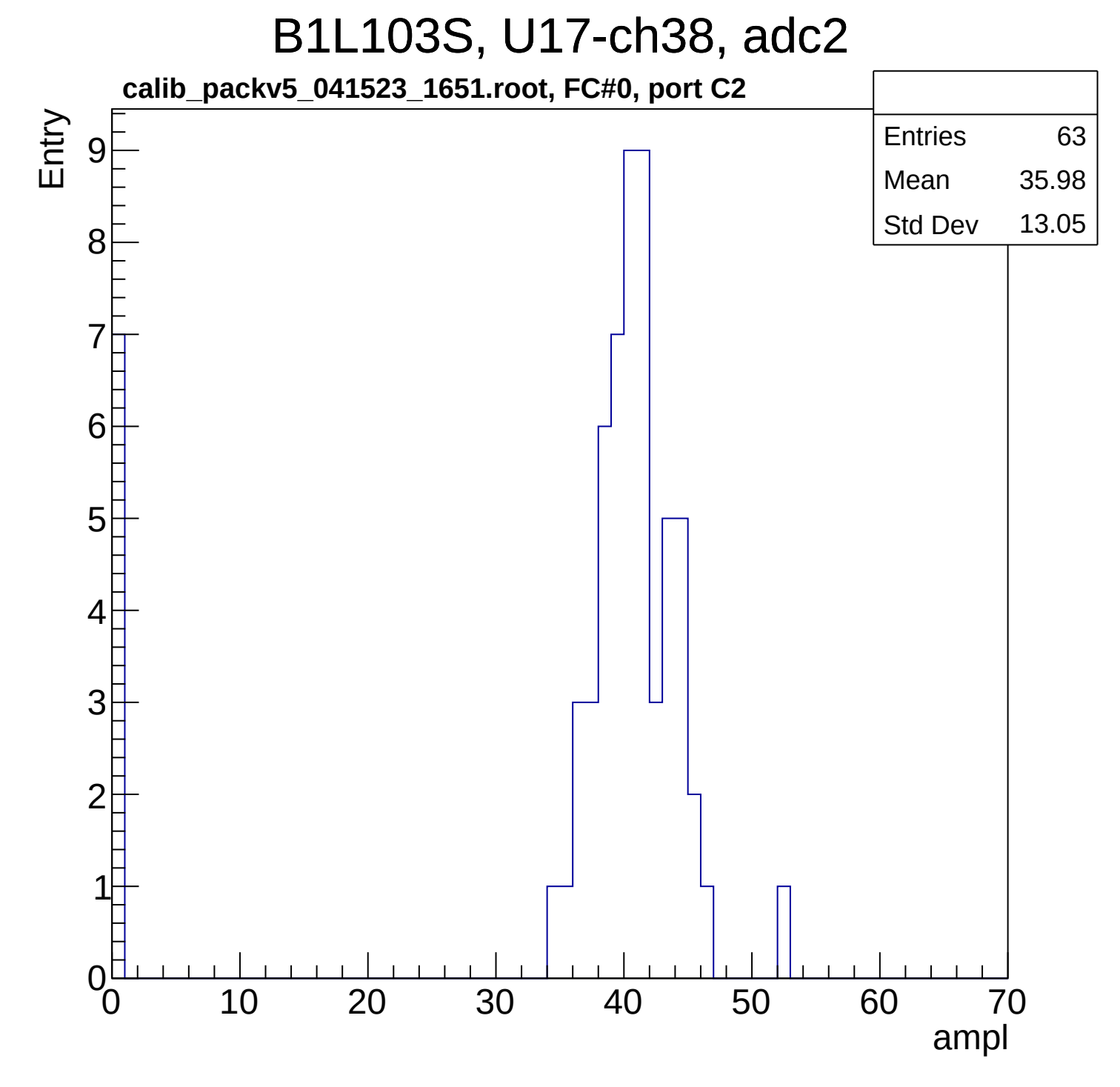
B1L103S, U17-ch38, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 35.98
Std Dev 13.05
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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60
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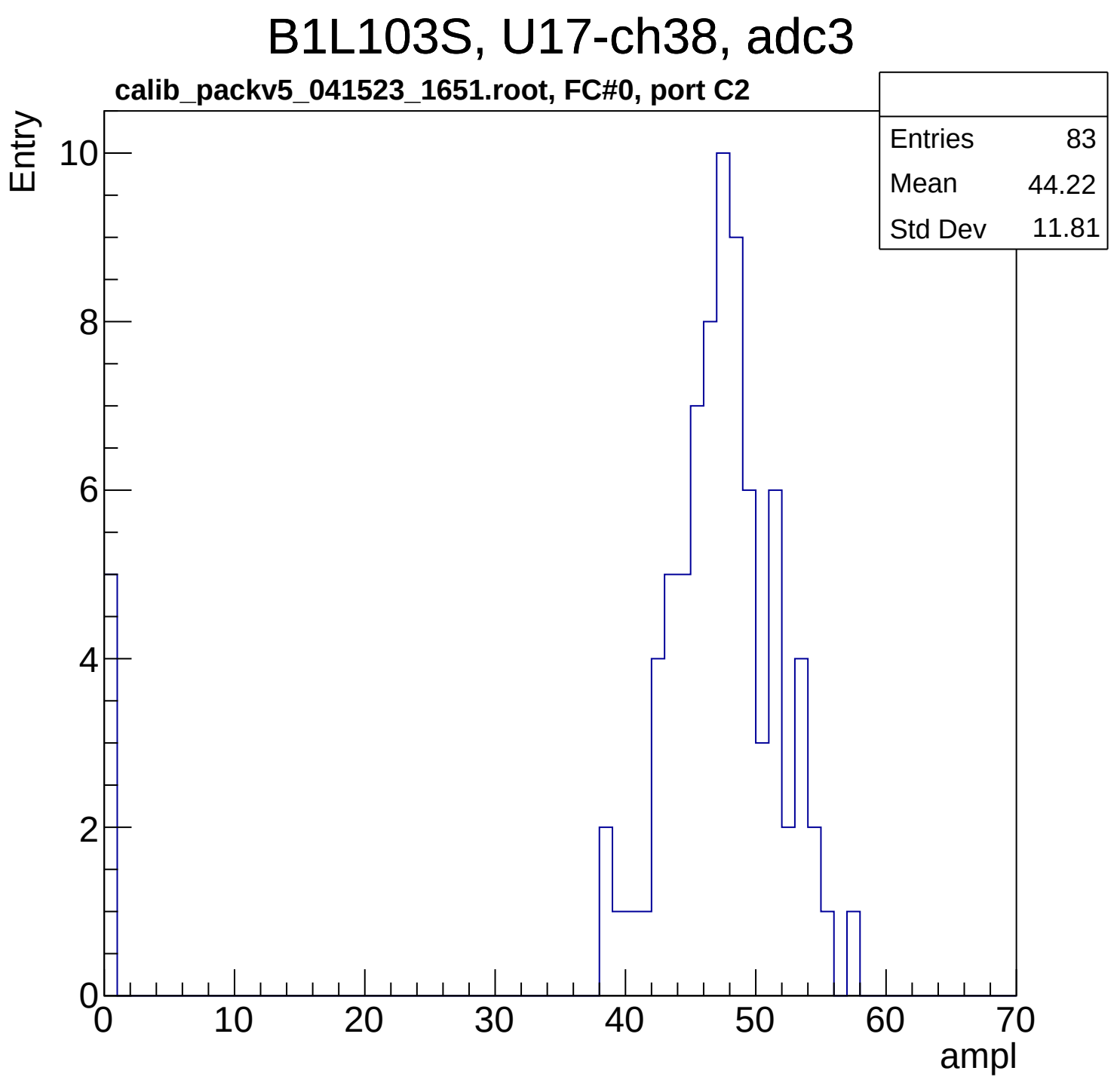
B1L103S, U17-ch38, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 44.22
Std Dev 11.81
Entry
ampl
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4
6
8
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0
10
20
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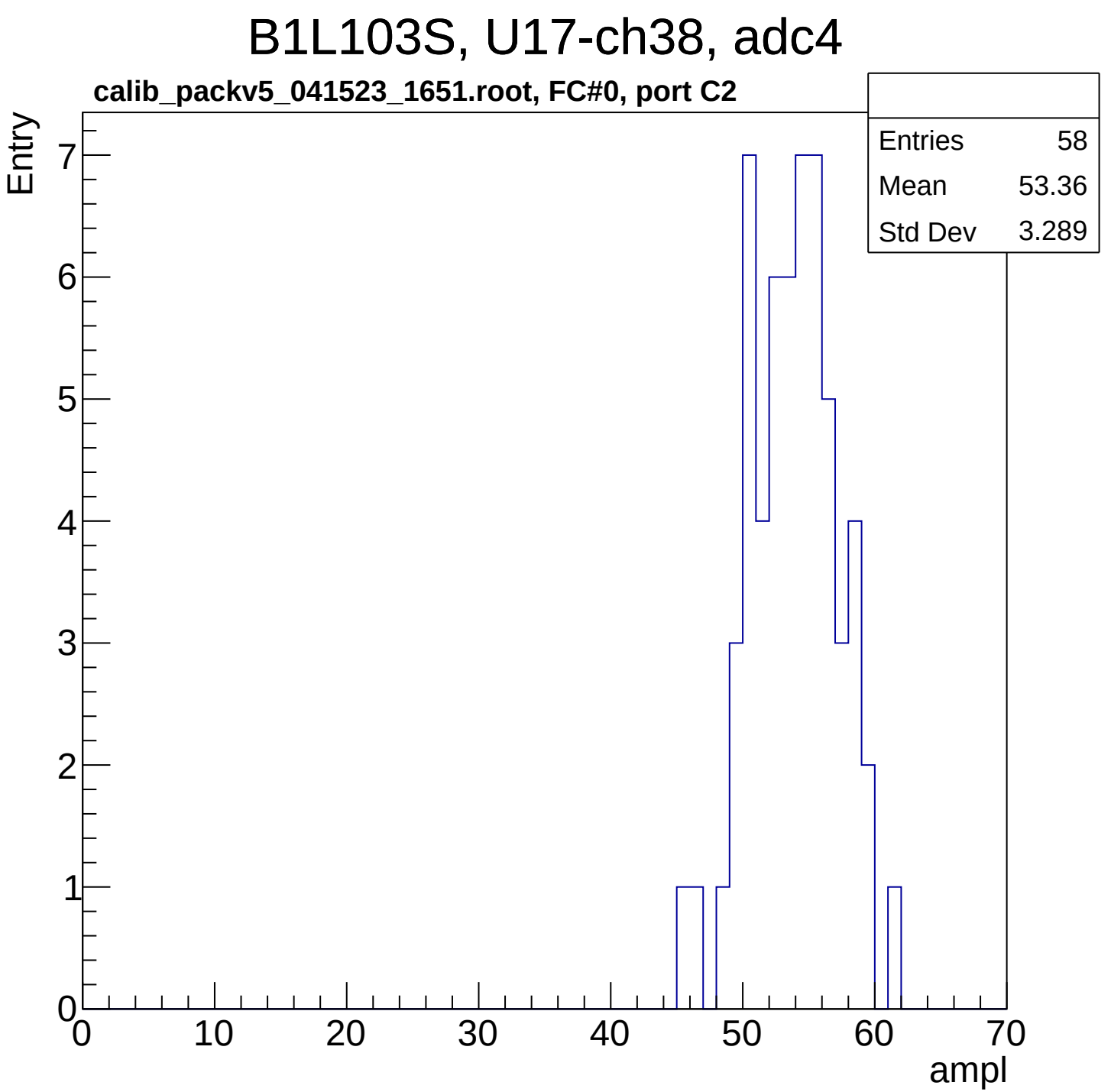
40
50
60
70


B1L103S, U17-ch38, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 53.36
Std Dev 3.289
Entry
ampl
0
1
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3
4
5
6
7
0
10
20
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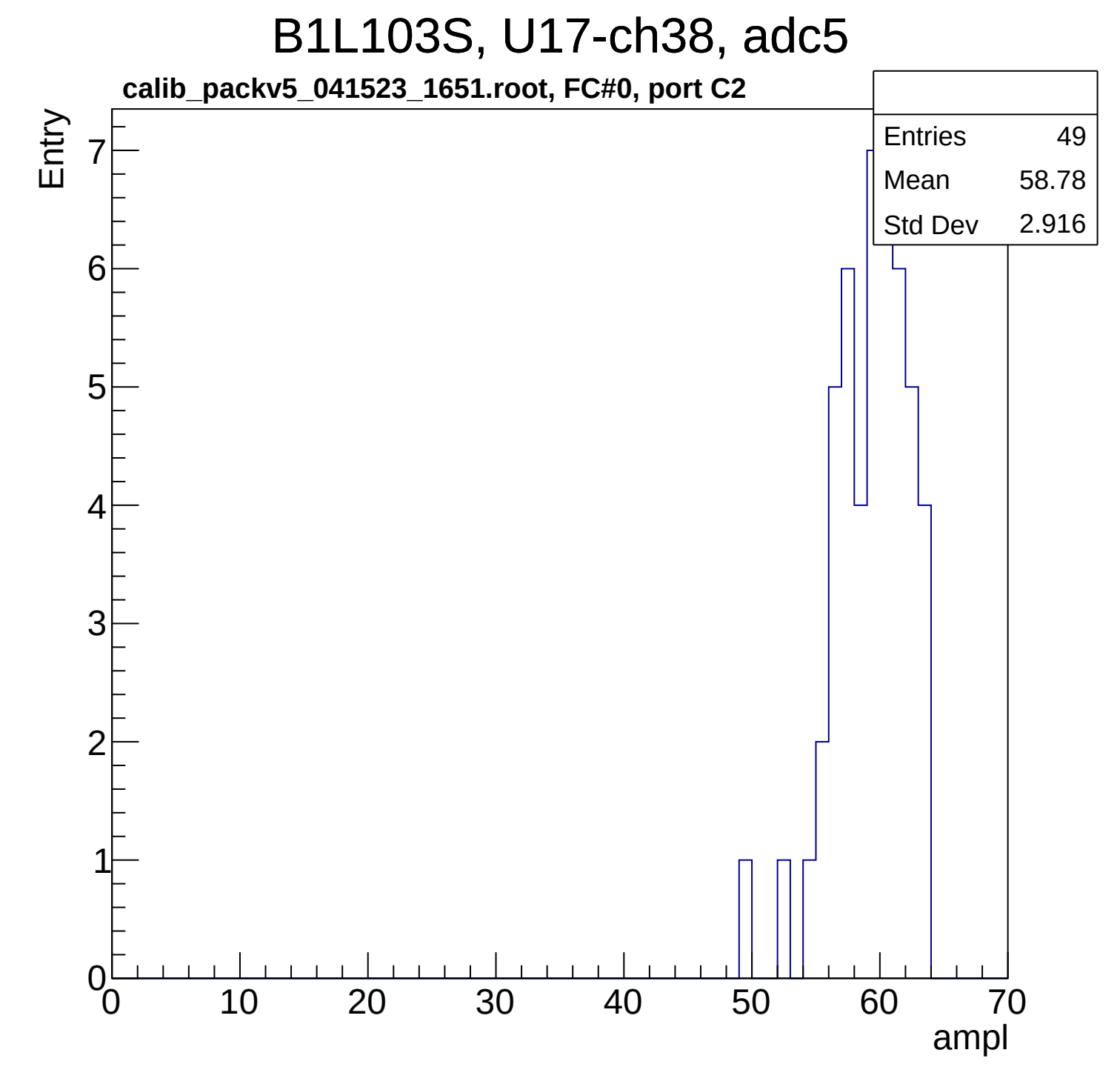
40
50
60
70


B1L103S, U17-ch38, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 58.78
Std Dev 2.916
Entry
ampl
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3
4
5
6
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0
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20
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40
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60
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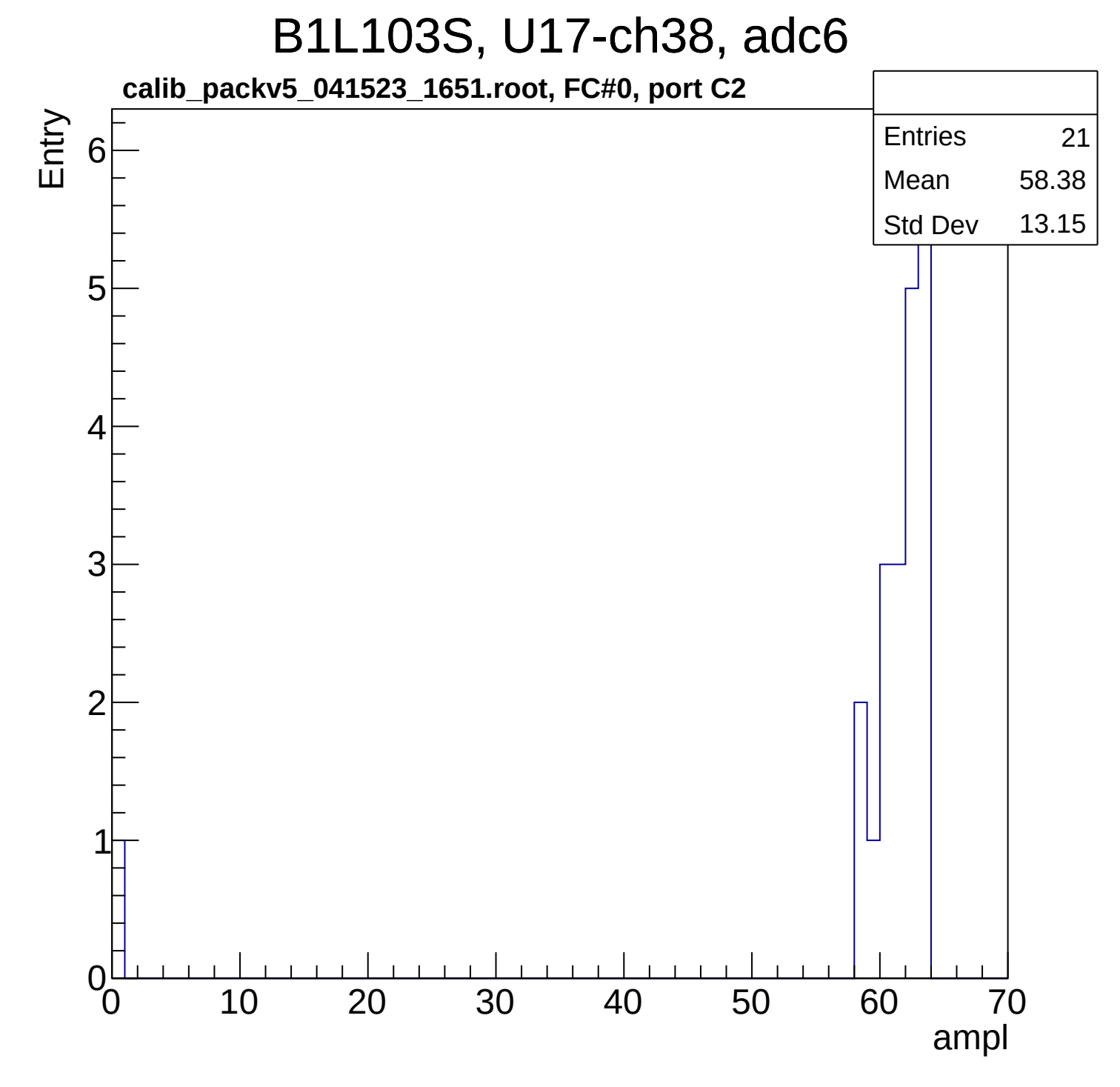
B1L103S, U17-ch38, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 58.38
Std Dev 13.15
Entry
ampl
0
1
2
3
4
5
6
0
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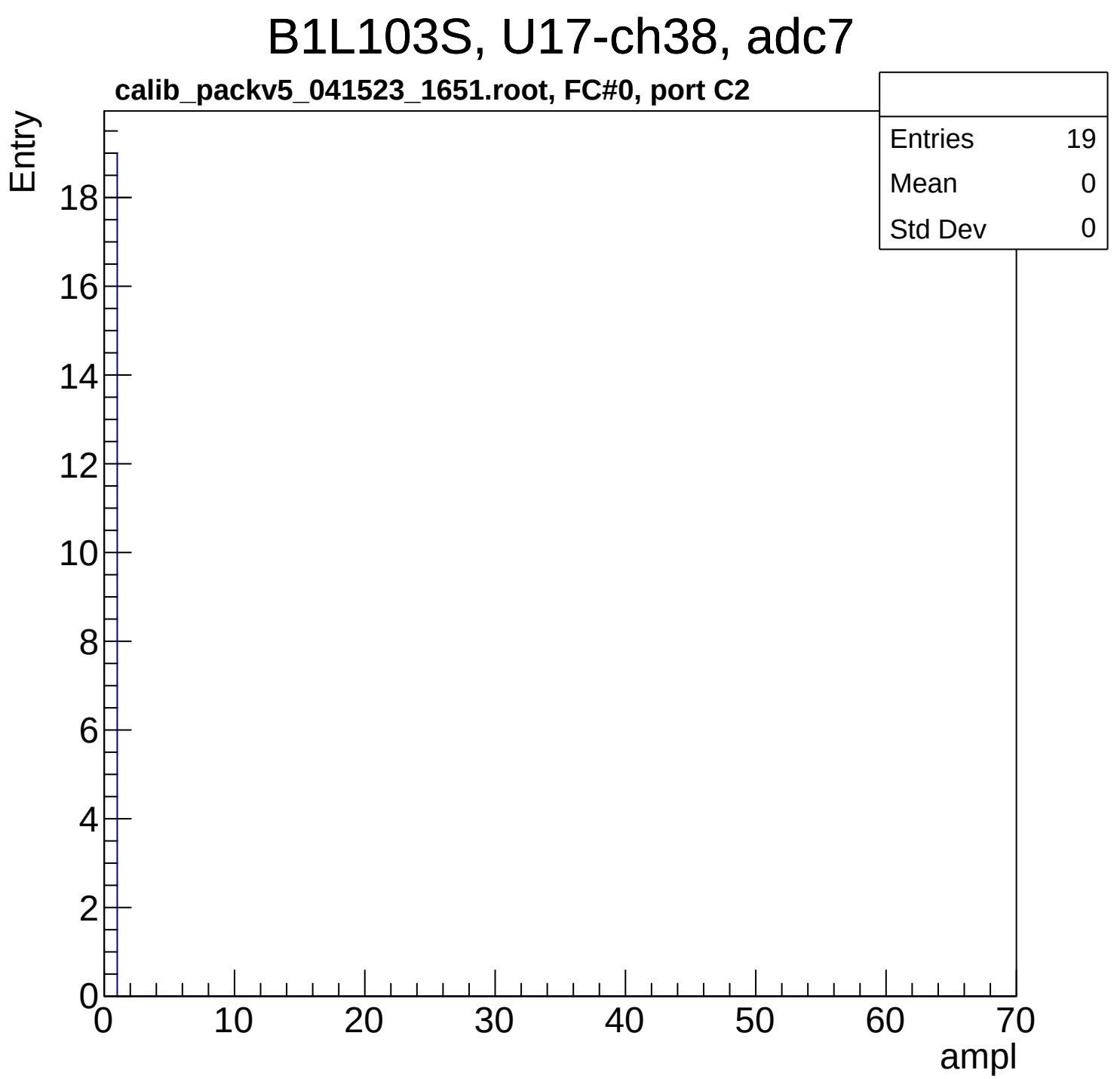
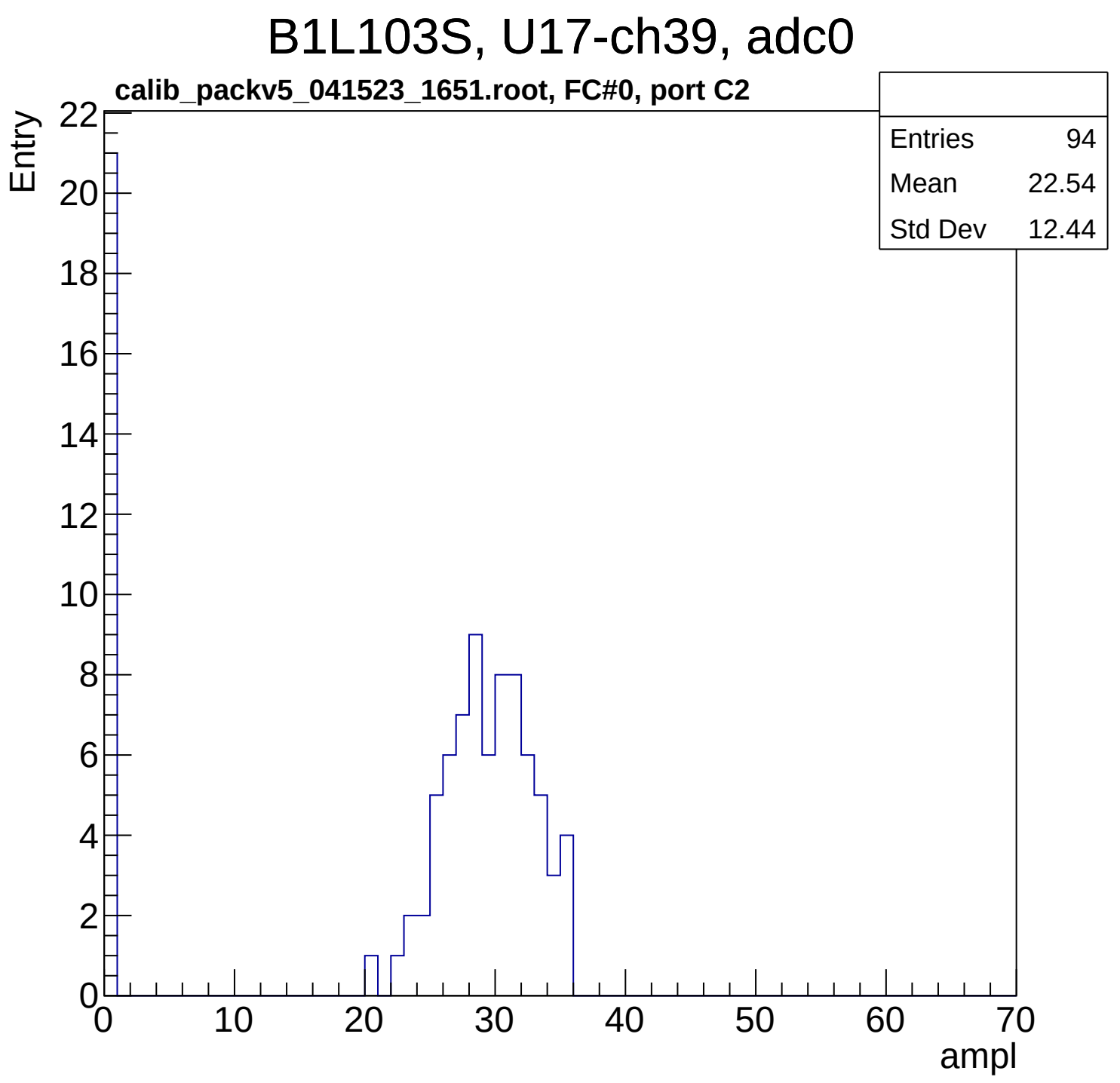
30
40
50
60
70


B1L103S, U17-ch38, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch39, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 94
Mean 22.54
Std Dev 12.44
Entry
ampl
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8
10
12
14
16
18
20
22
0
10
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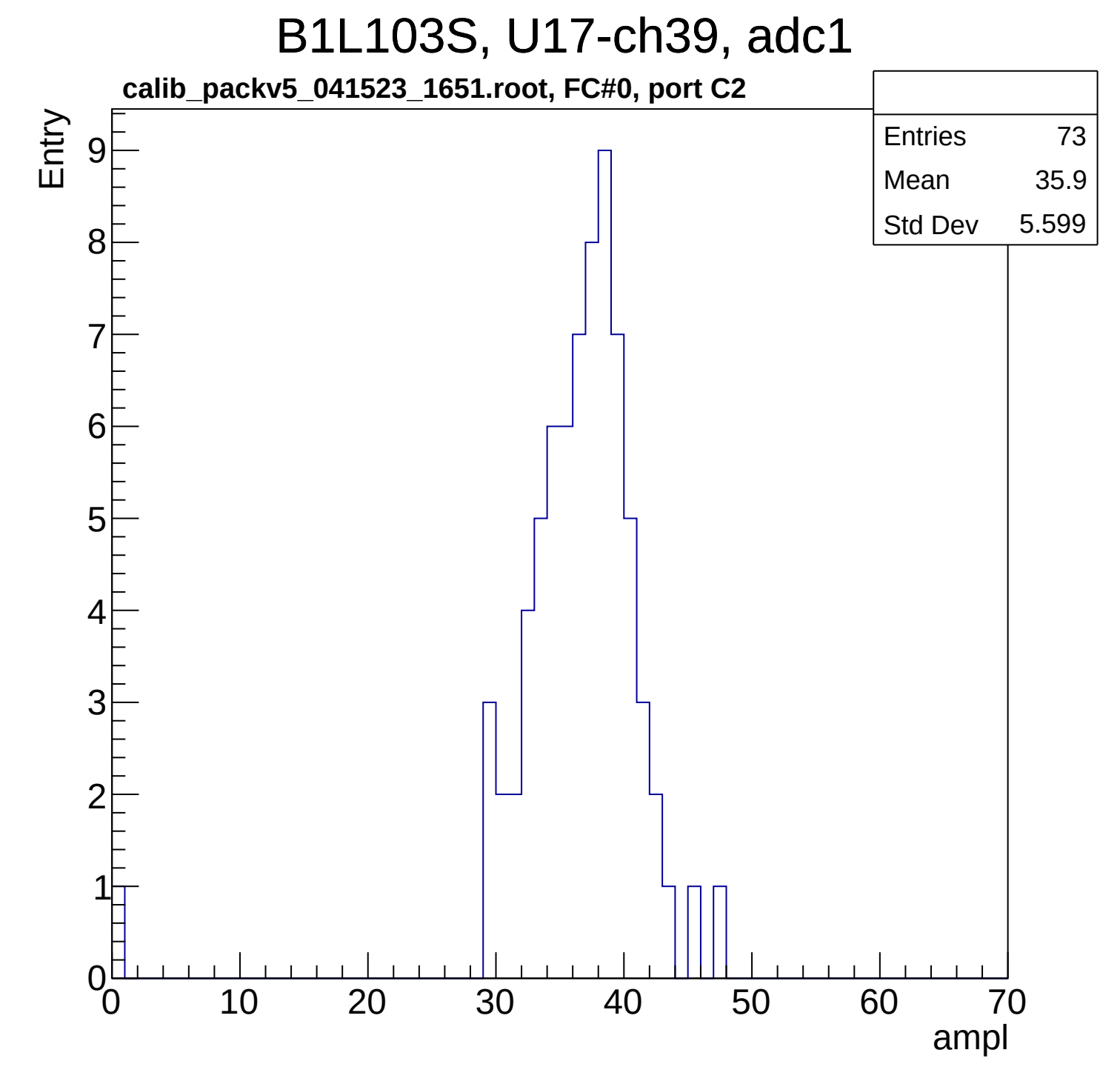
30
40
50
60
70


B1L103S, U17-ch39, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 35.9
Std Dev 5.599
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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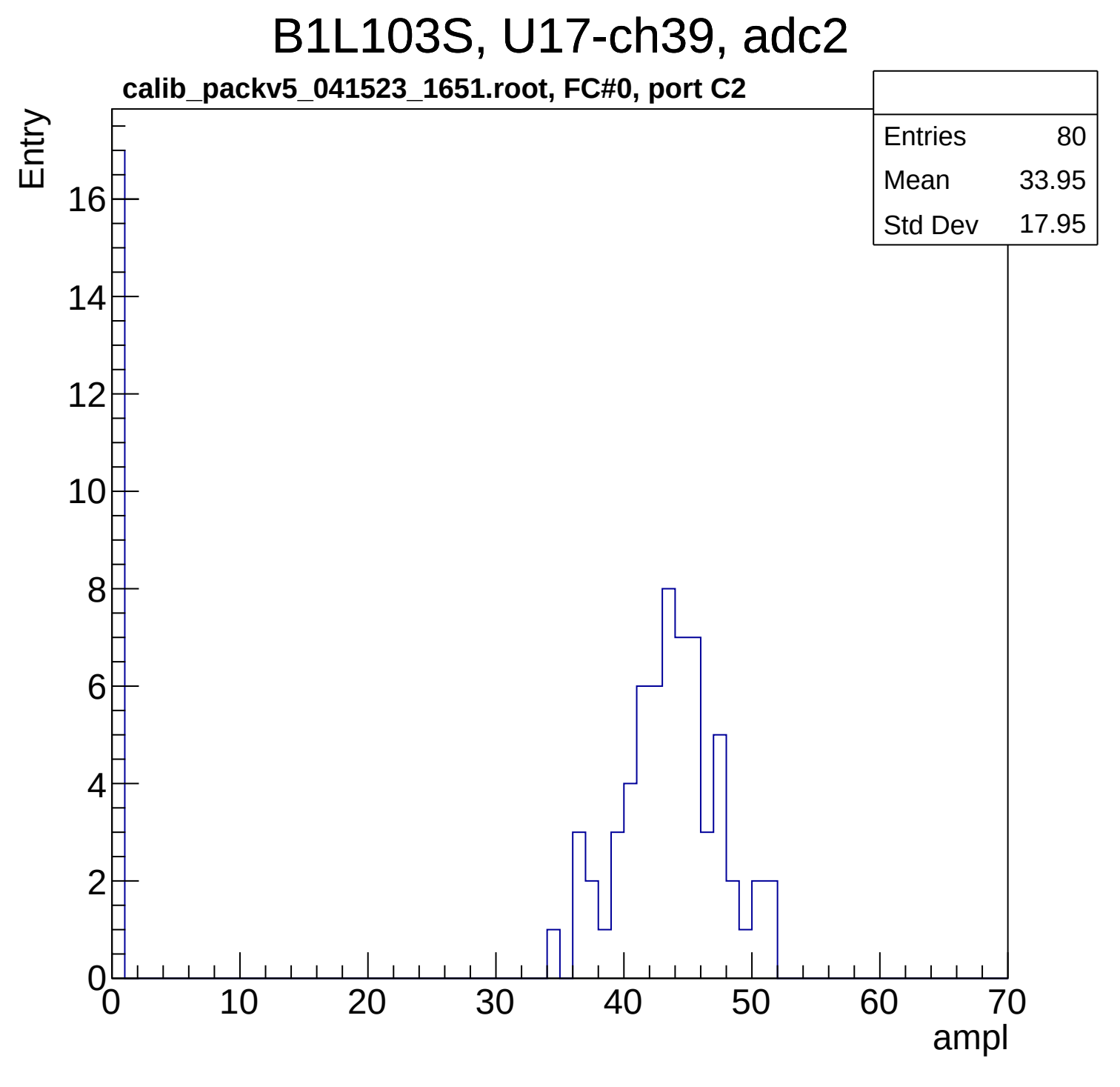
B1L103S, U17-ch39, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 33.95
Std Dev 17.95
Entry
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4
6
8
10
12
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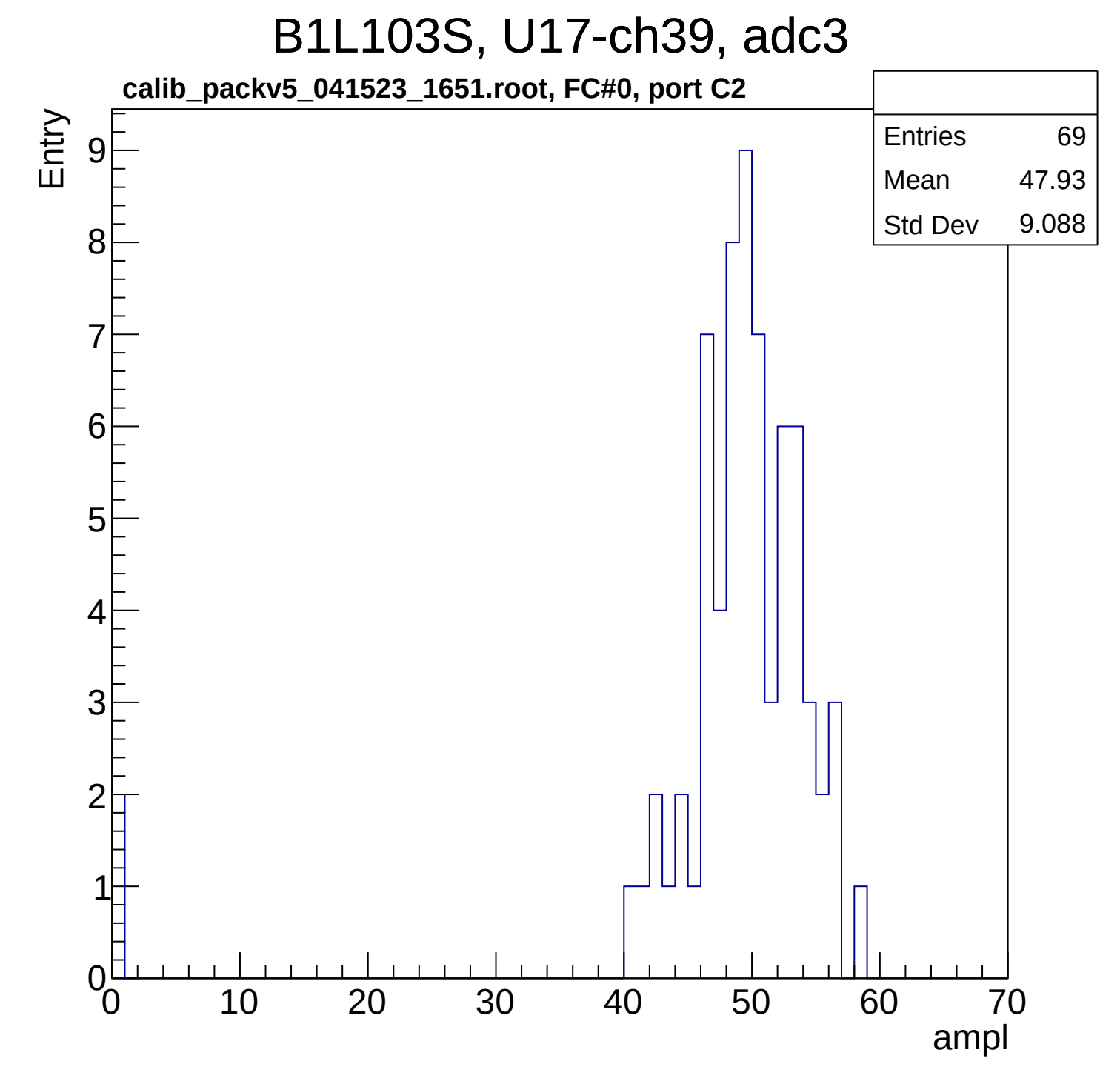
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch39, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 47.93
Std Dev 9.088
Entry
ampl
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3
4
5
6
7
8
9
0
10
20
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40
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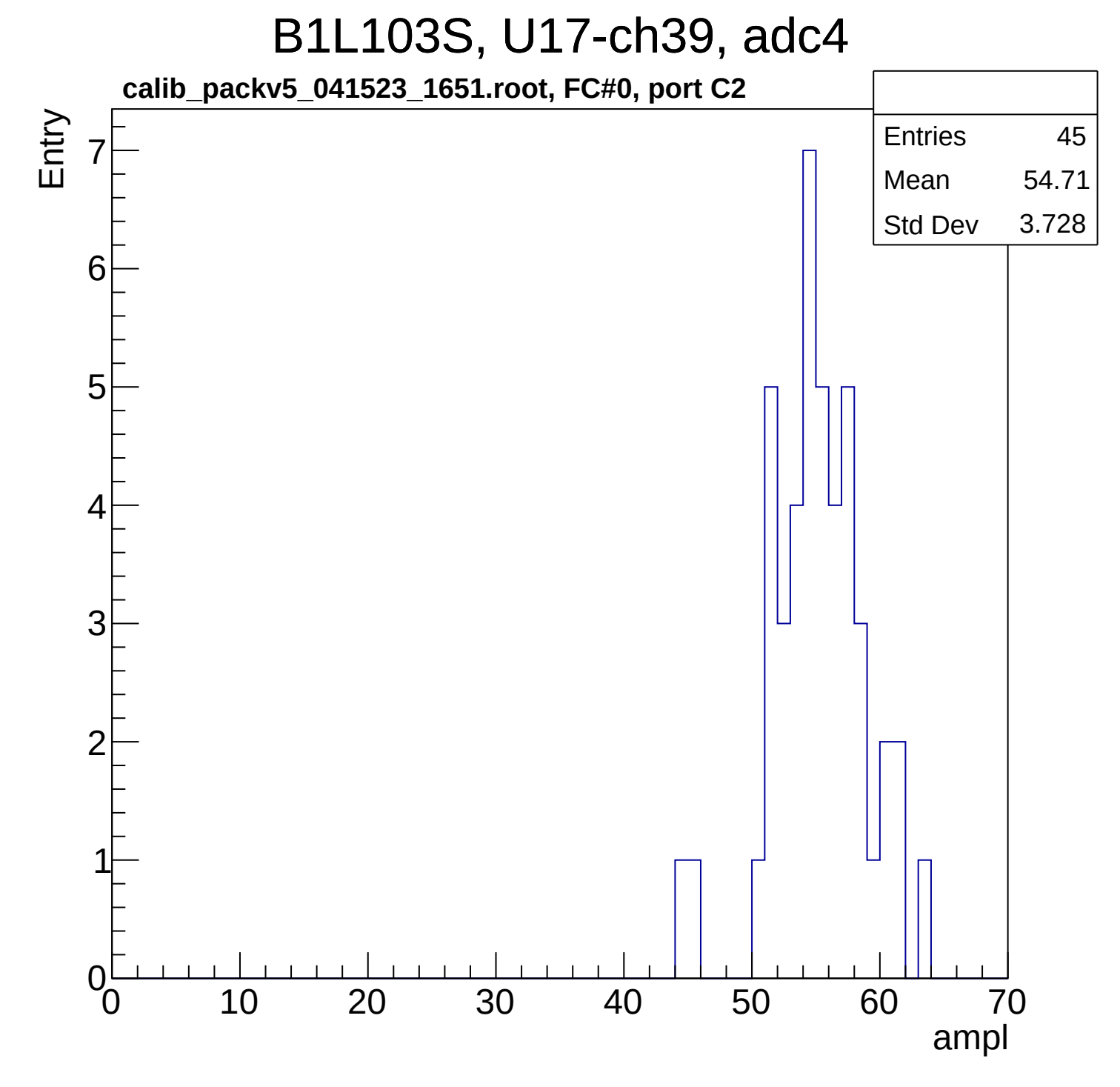
60
70


B1L103S, U17-ch39, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 54.71
Std Dev 3.728
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
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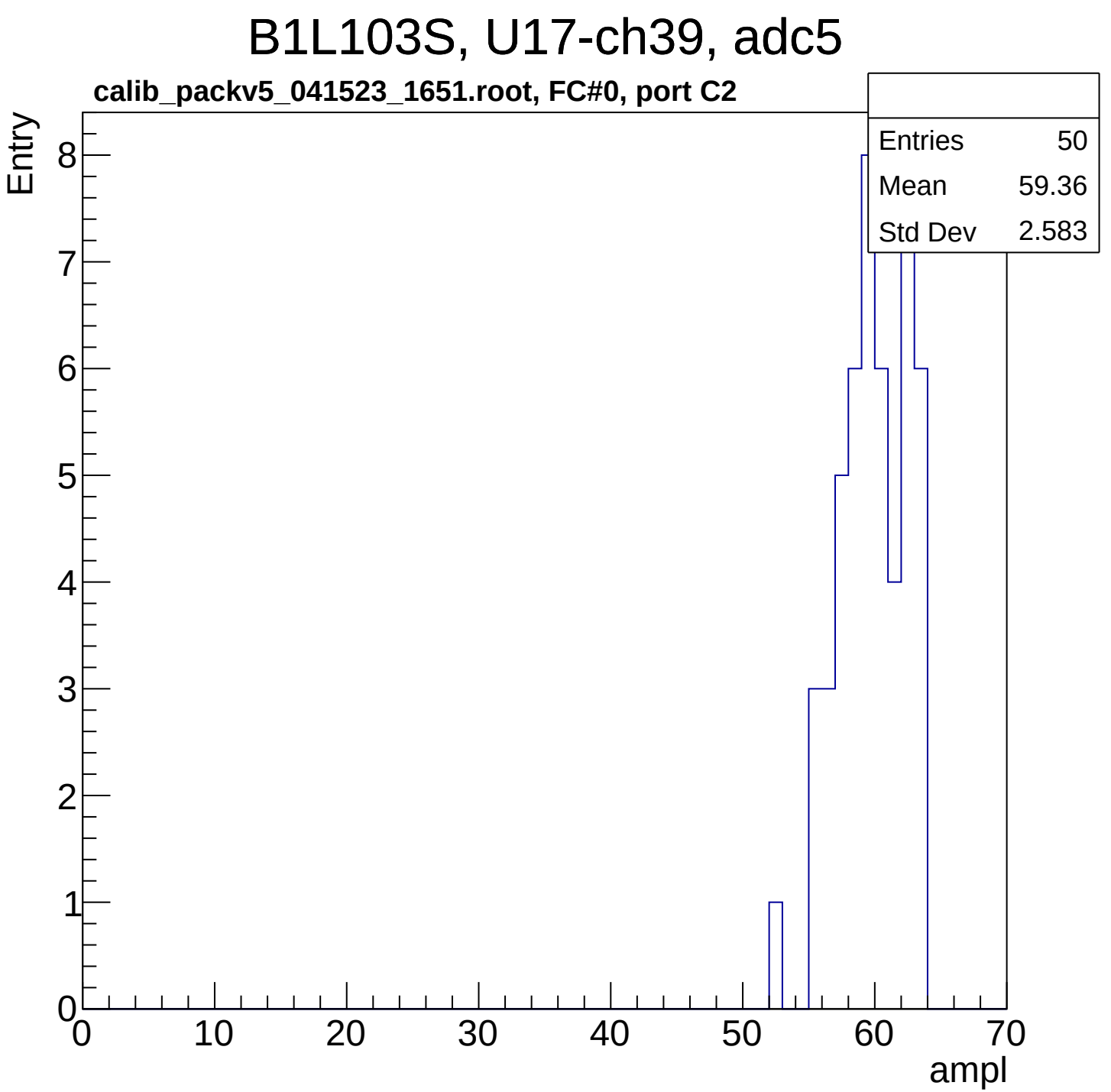
B1L103S, U17-ch39, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 59.36
Std Dev 2.583
Entry
ampl
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5
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7
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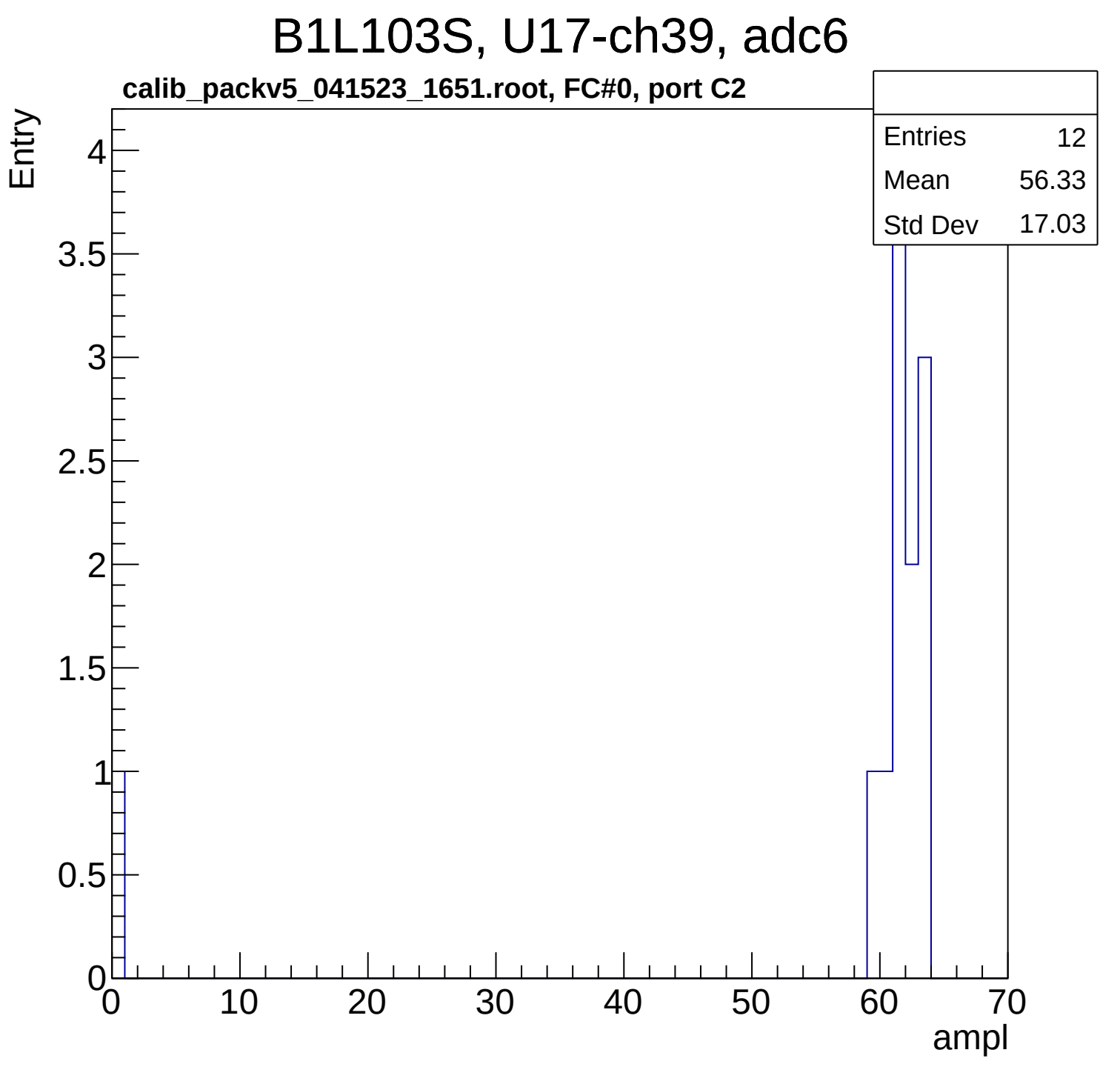
B1L103S, U17-ch39, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 56.33
Std Dev 17.03
Entry
ampl
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0.5
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1.5
2
2.5
3
3.5
4
0
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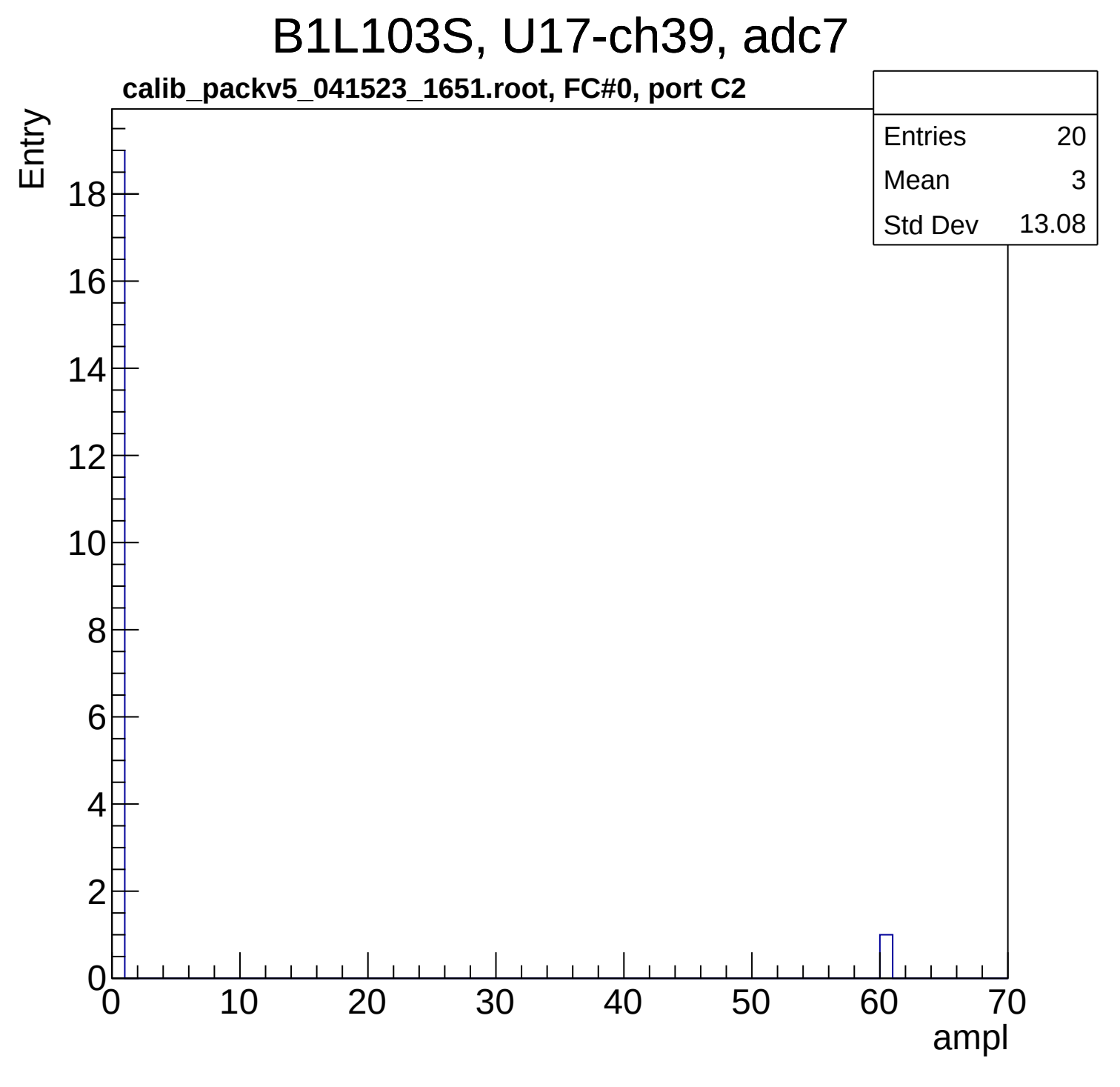
B1L103S, U17-ch39, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3
Std Dev 13.08
Entry
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10
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14
16
18
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10
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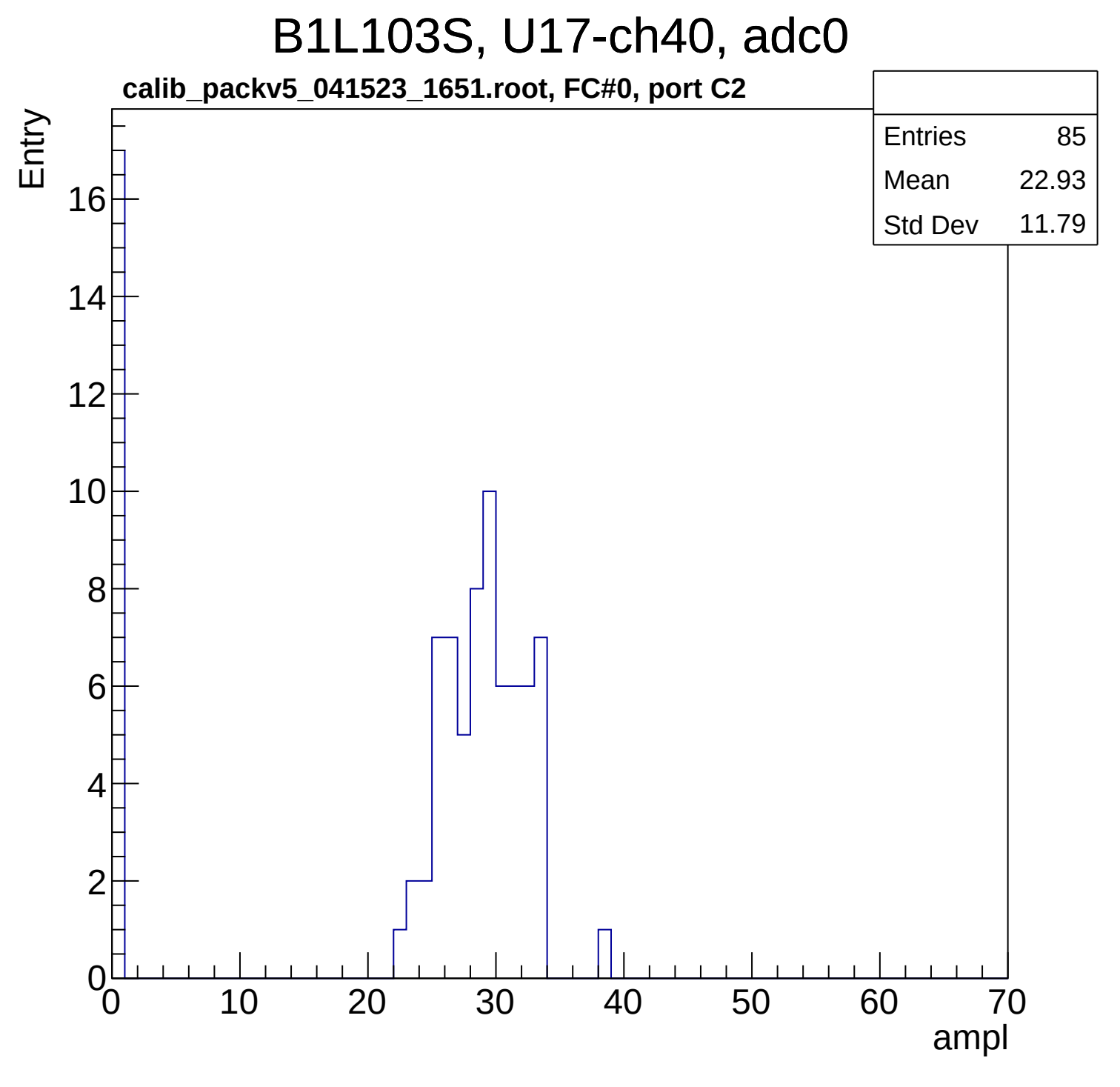
40
50
60
70
ampl


B1L103S, U17-ch40, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 22.93
Std Dev 11.79
Entry
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8
10
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14
16
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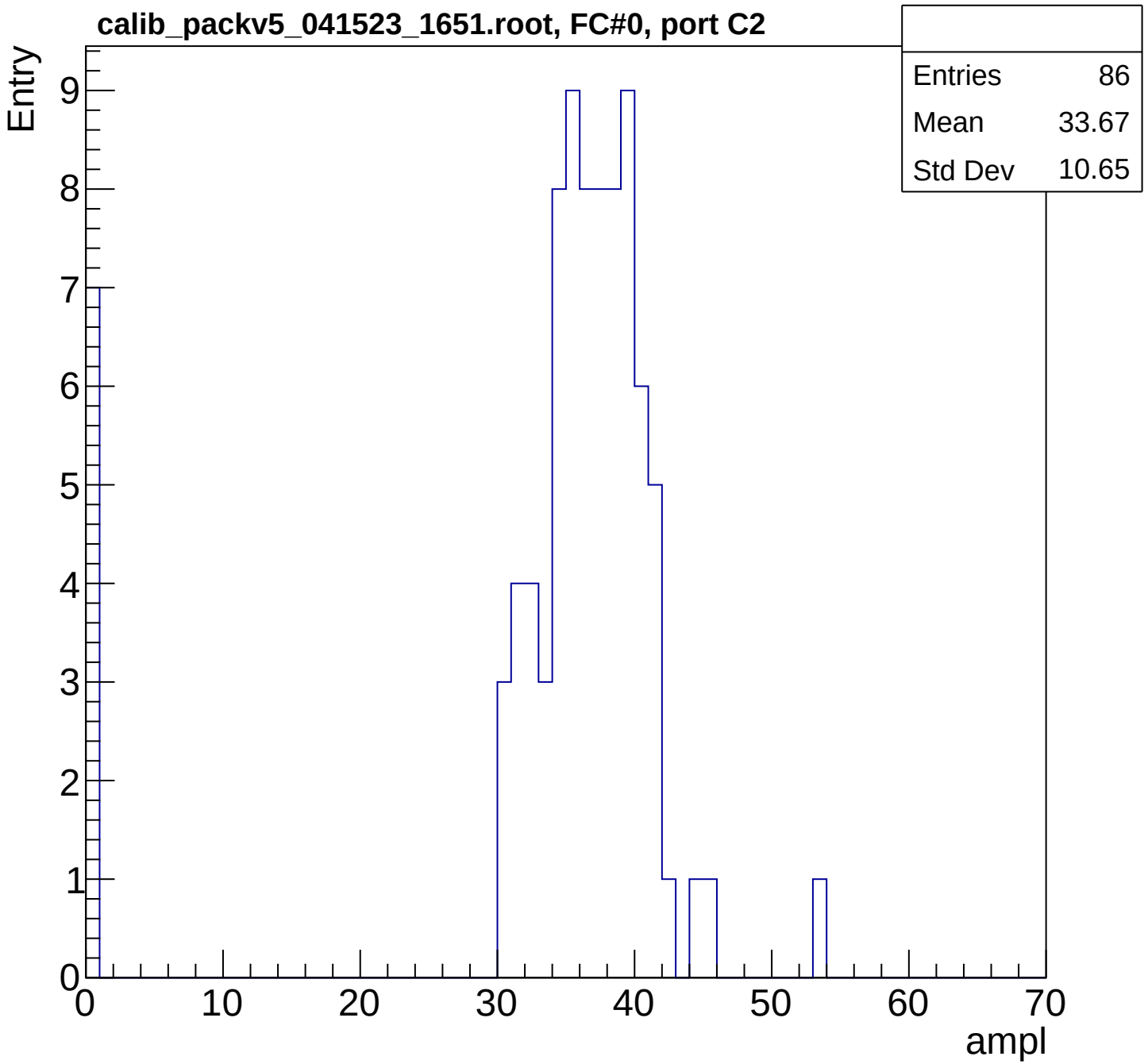
50
60
70
ampl


B1L103S, U17-ch40, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 33.67
Std Dev 10.65
Entry
ampl
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6
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0
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60
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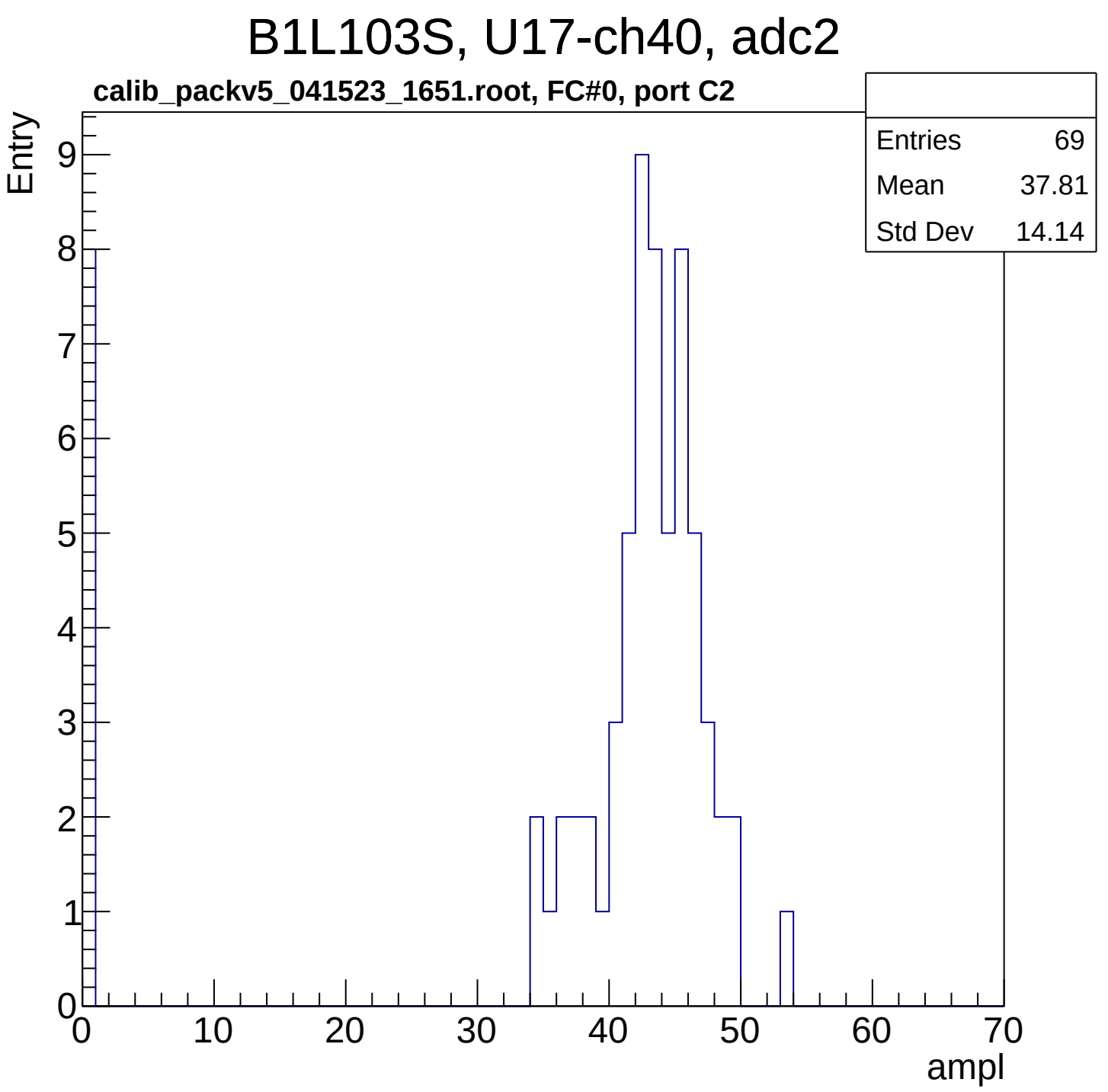
B1L103S, U17-ch40, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 37.81
Std Dev 14.14
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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60
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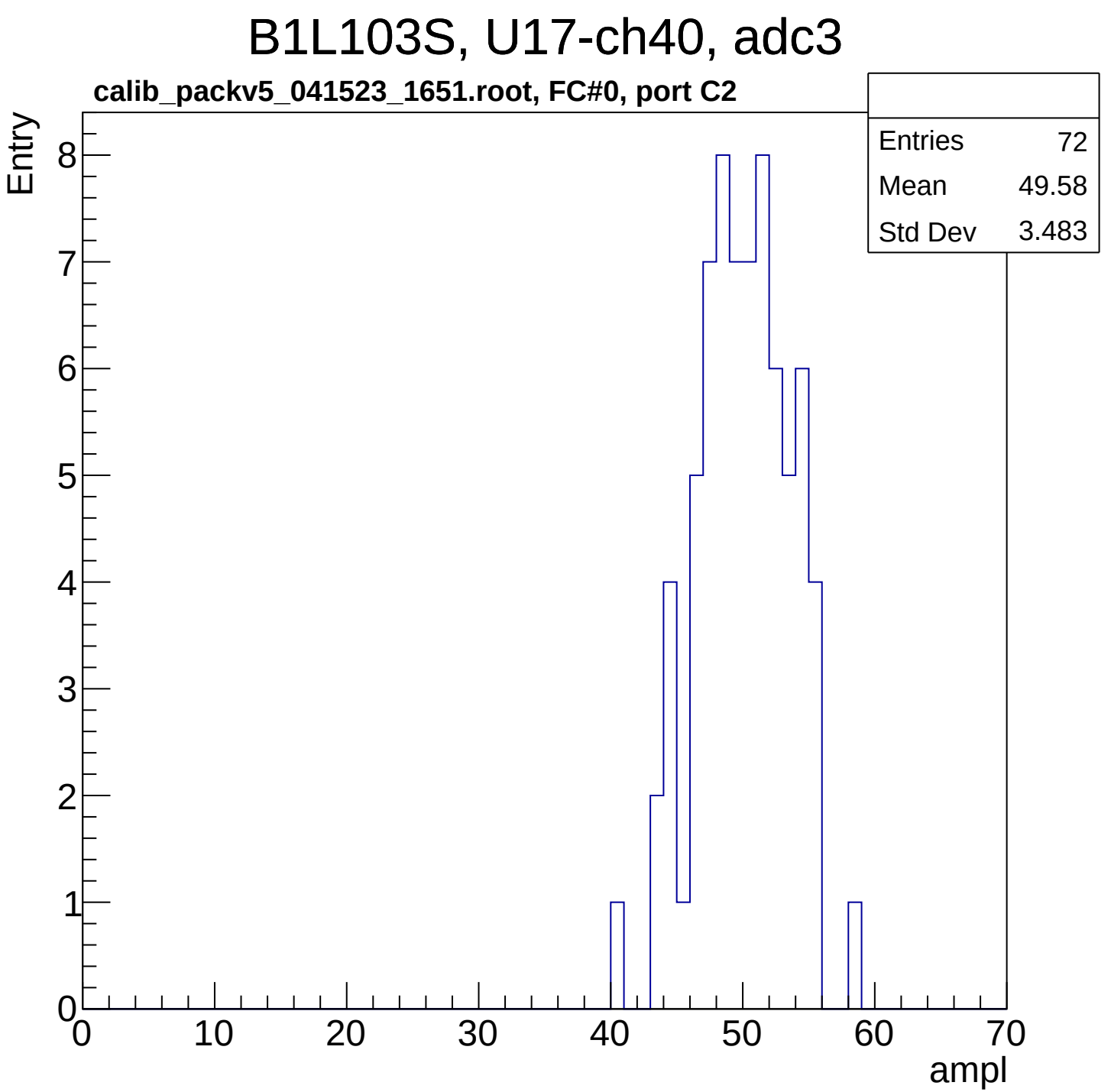
B1L103S, U17-ch40, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 49.58
Std Dev 3.483
Entry
ampl
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5
6
7
8
0
10
20
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40
50
60
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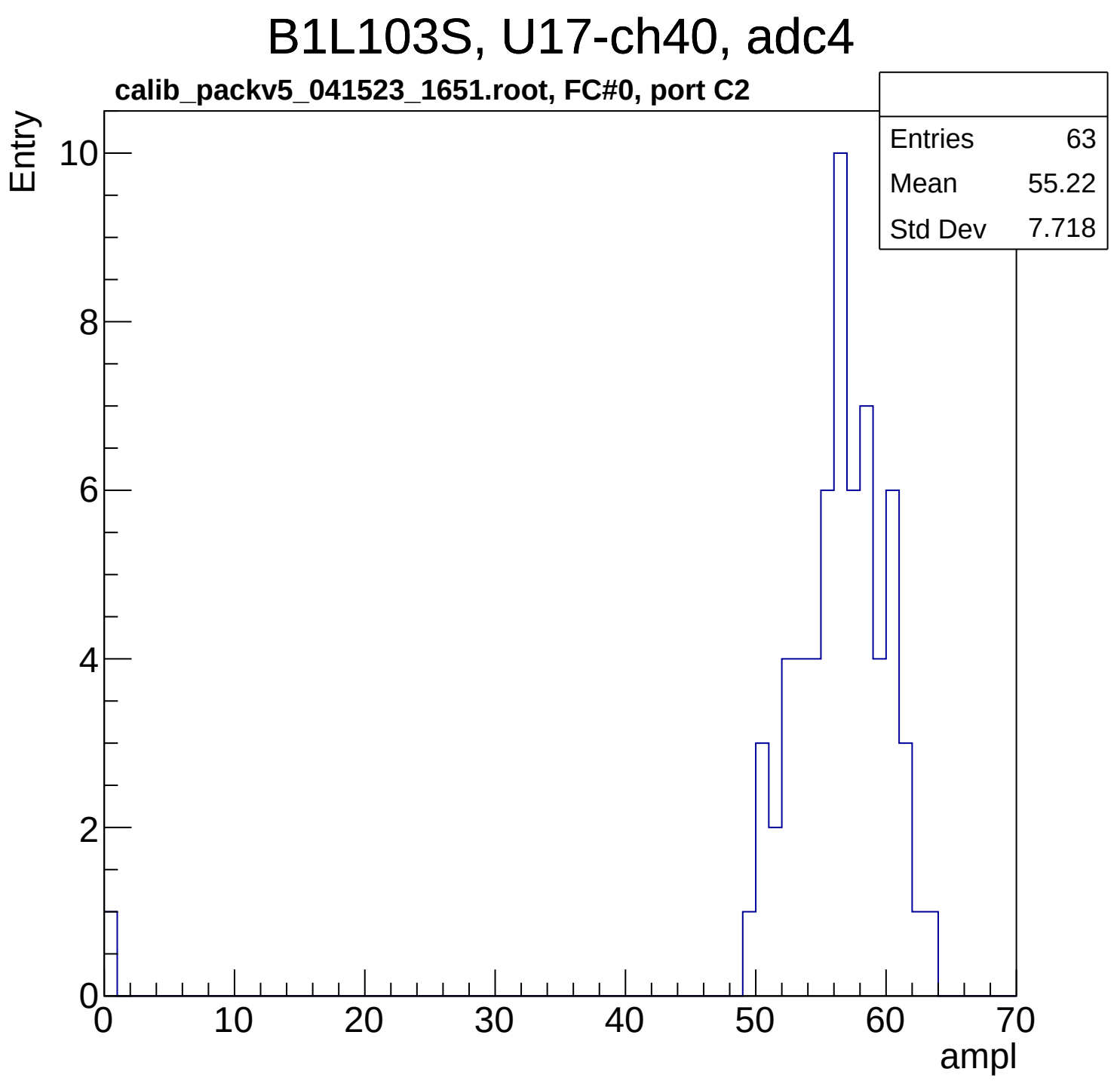
B1L103S, U17-ch40, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 55.22
Std Dev 7.718
Entry
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10
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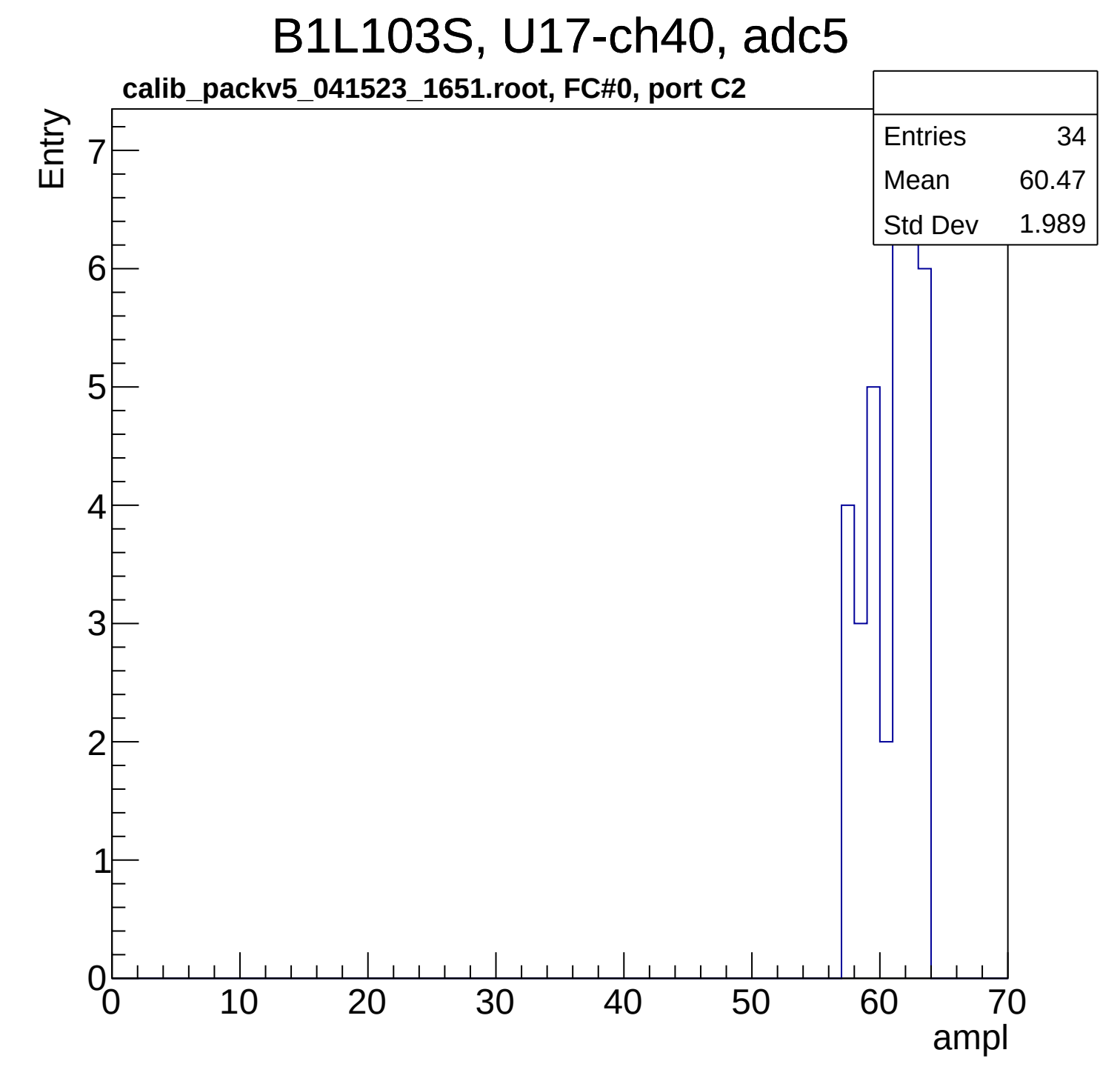
30
40
50
60
70
ampl


B1L103S, U17-ch40, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 34
Mean 60.47
Std Dev 1.989
Entry
ampl
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3
4
5
6
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0
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60
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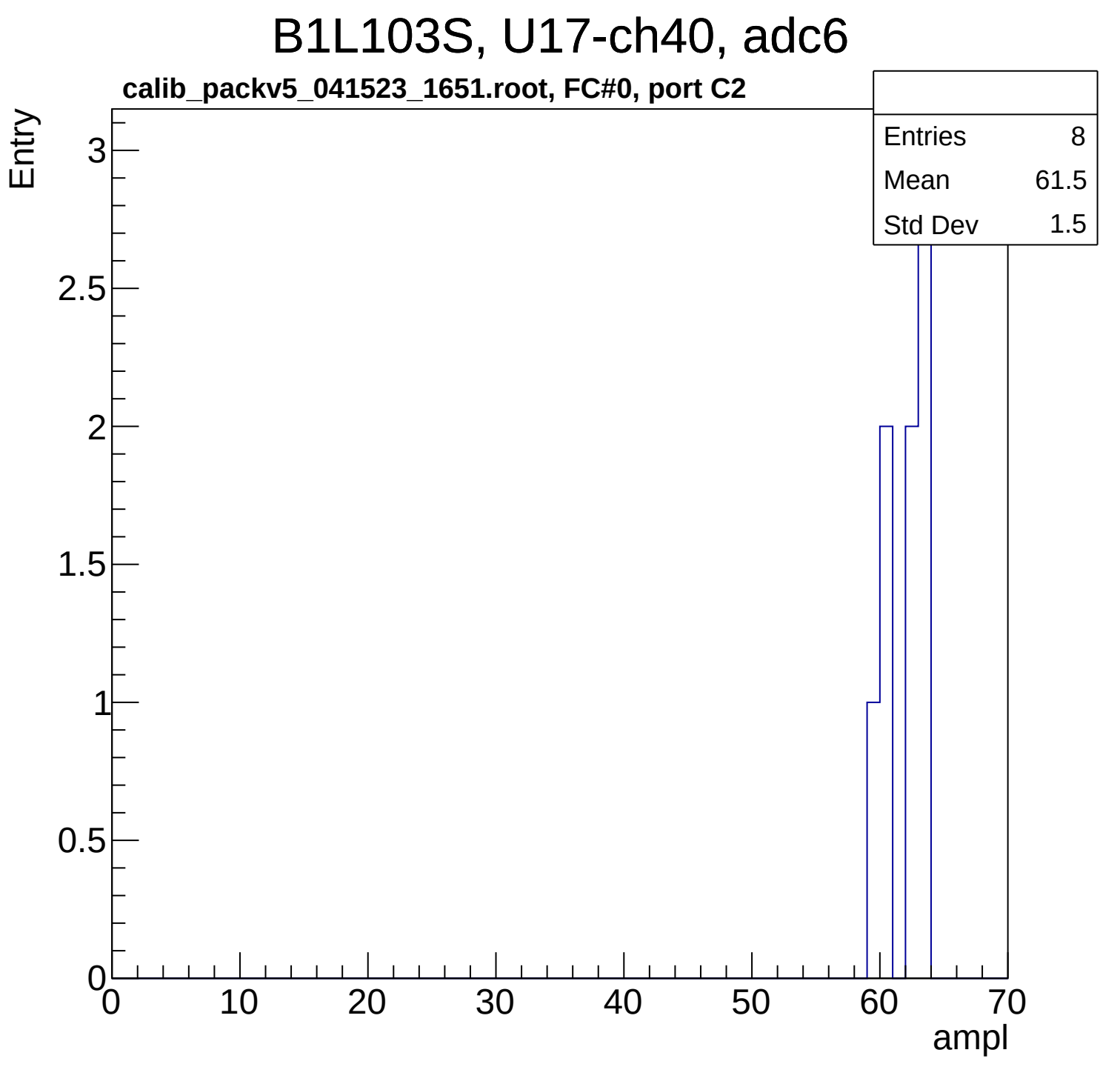
B1L103S, U17-ch40, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 61.5
Std Dev 1.5
Entry
ampl
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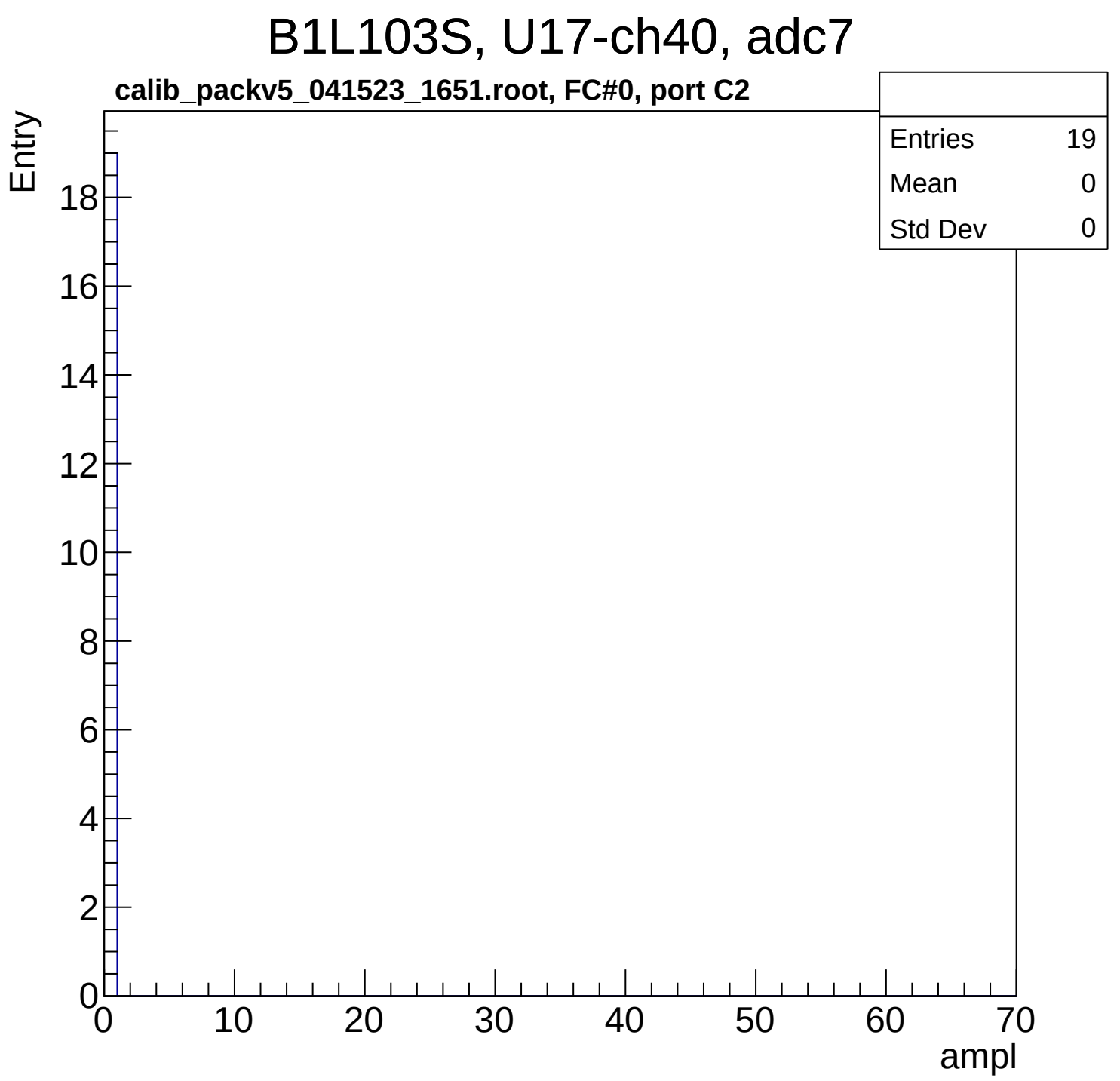
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U17-ch40, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
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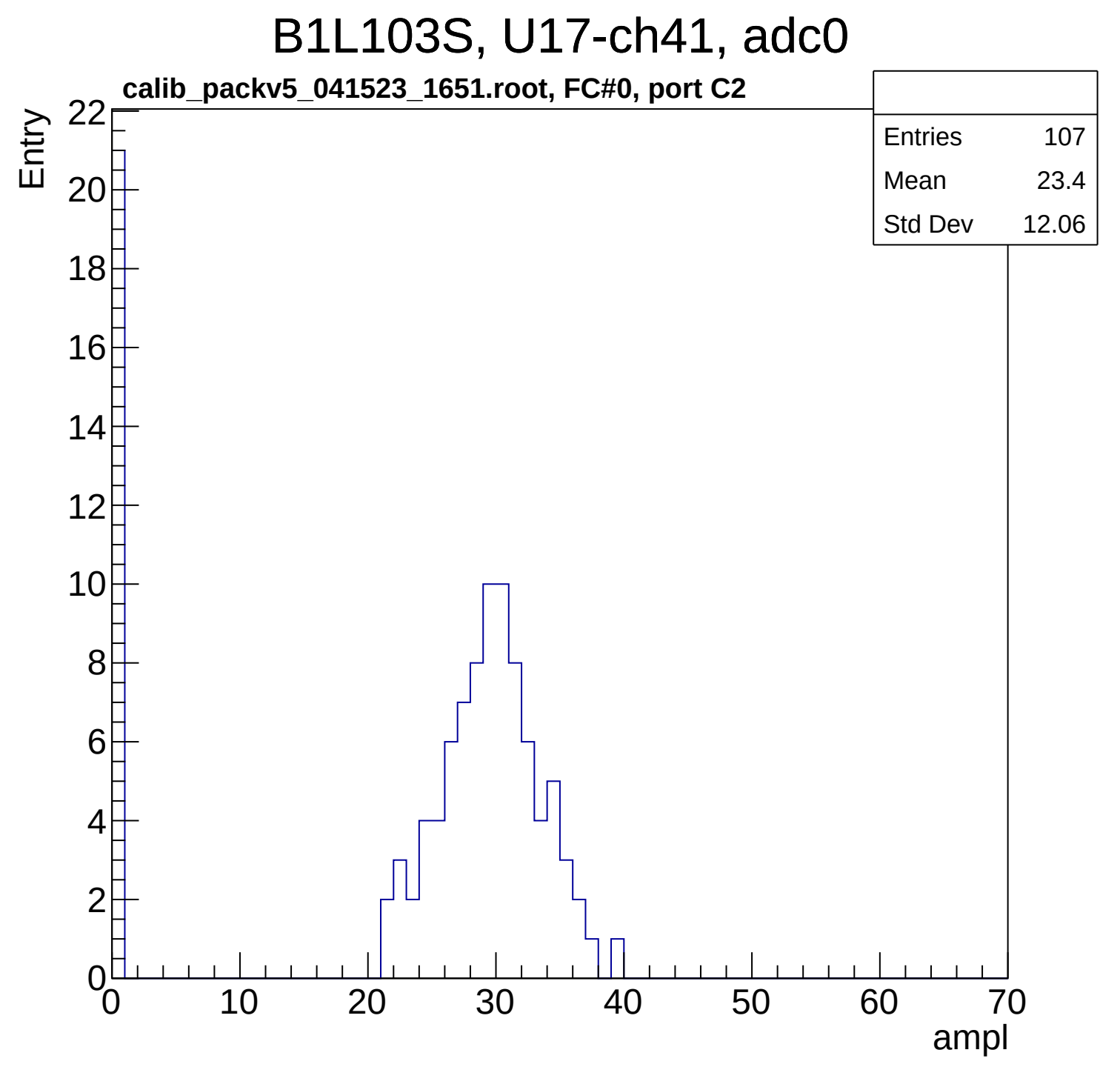
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch41, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 107
Mean 23.4
Std Dev 12.06
Entry
ampl
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8
10
12
14
16
18
20
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0
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60
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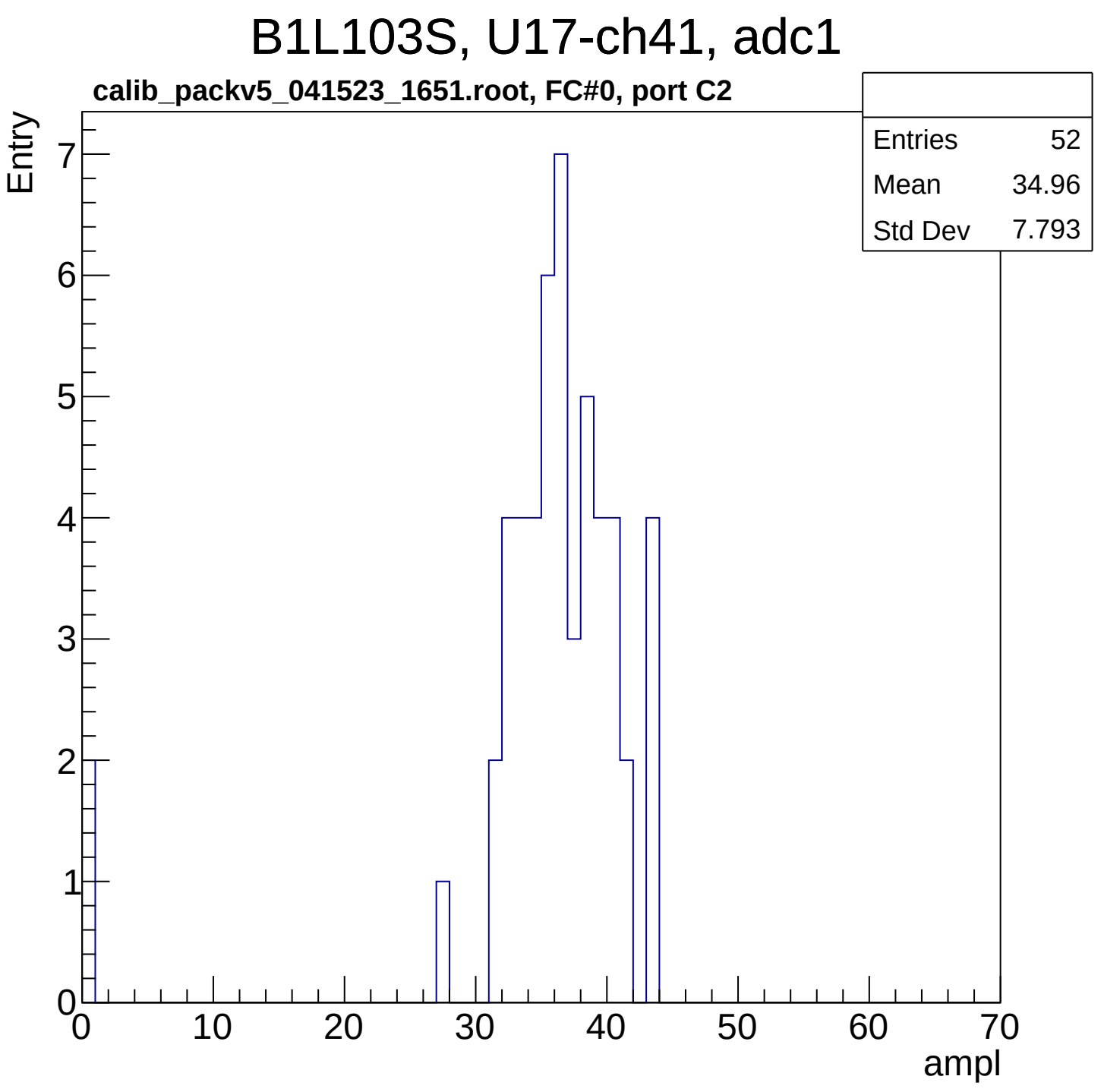
B1L103S, U17-ch41, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 34.96
Std Dev 7.793
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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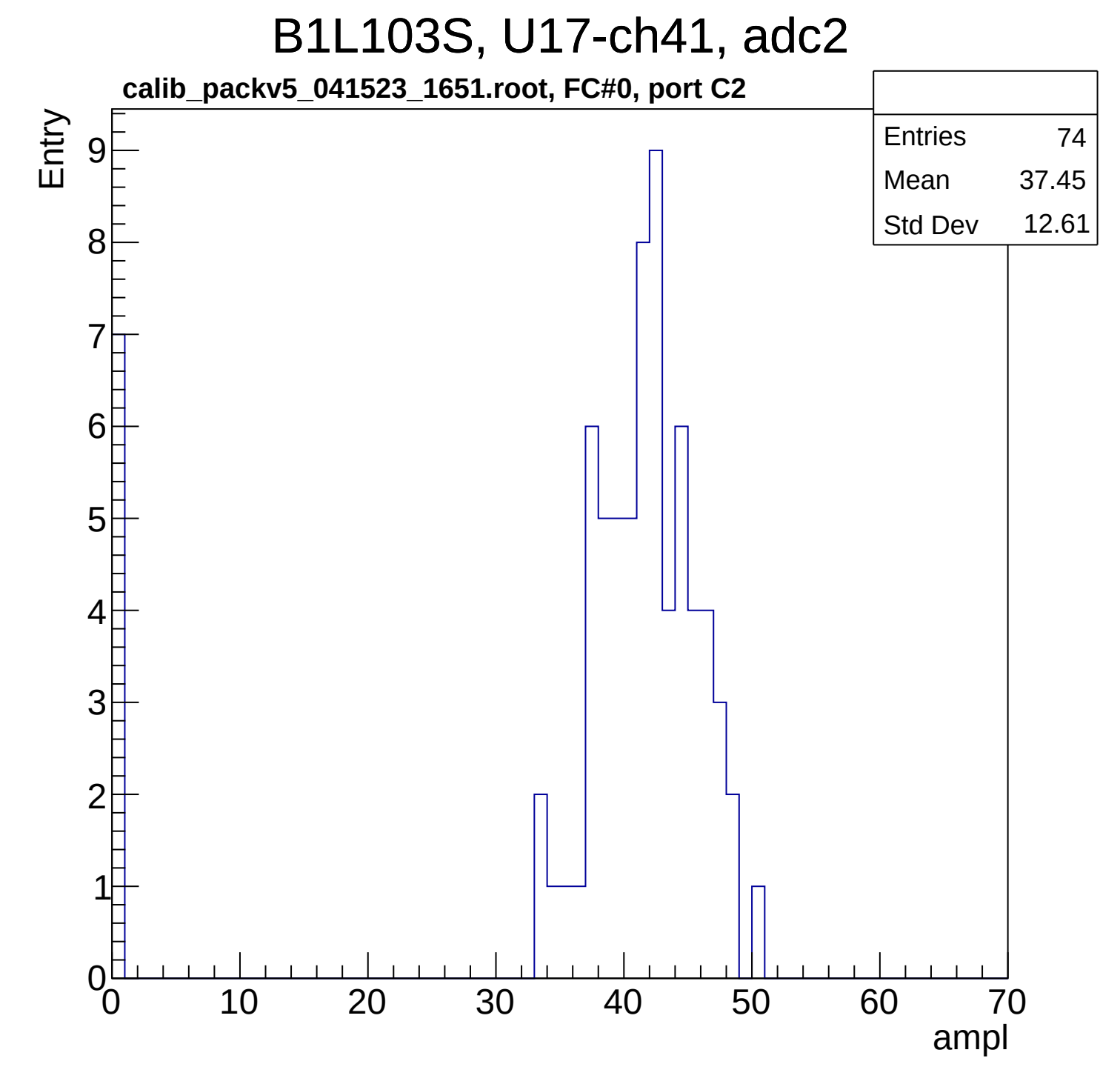
B1L103S, U17-ch41, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 37.45
Std Dev 12.61
Entry
ampl
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3
4
5
6
7
8
9
0
10
20
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40
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60
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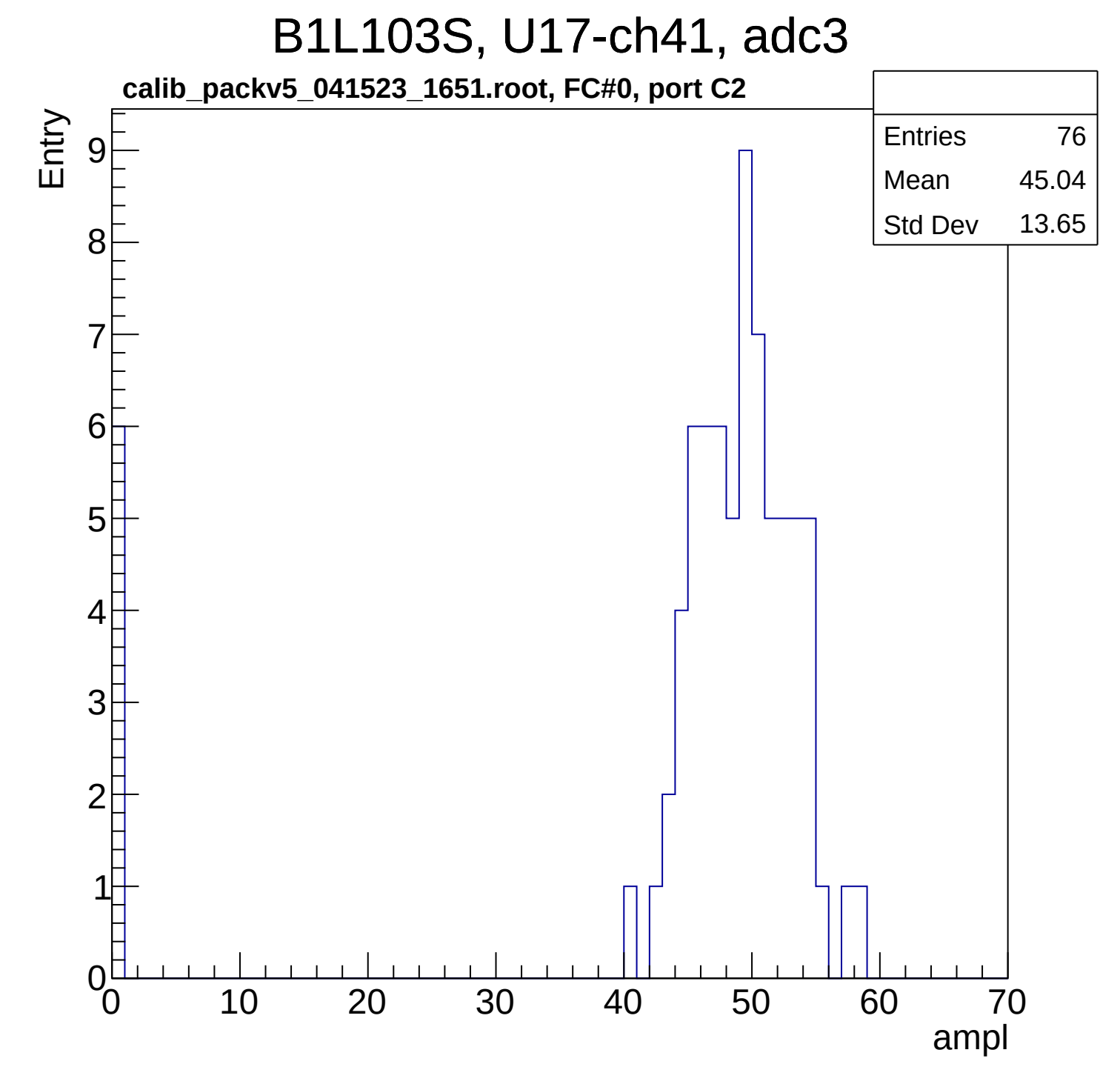
B1L103S, U17-ch41, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 45.04
Std Dev 13.65
Entry
ampl
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2
3
4
5
6
7
8
9
0
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40
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60
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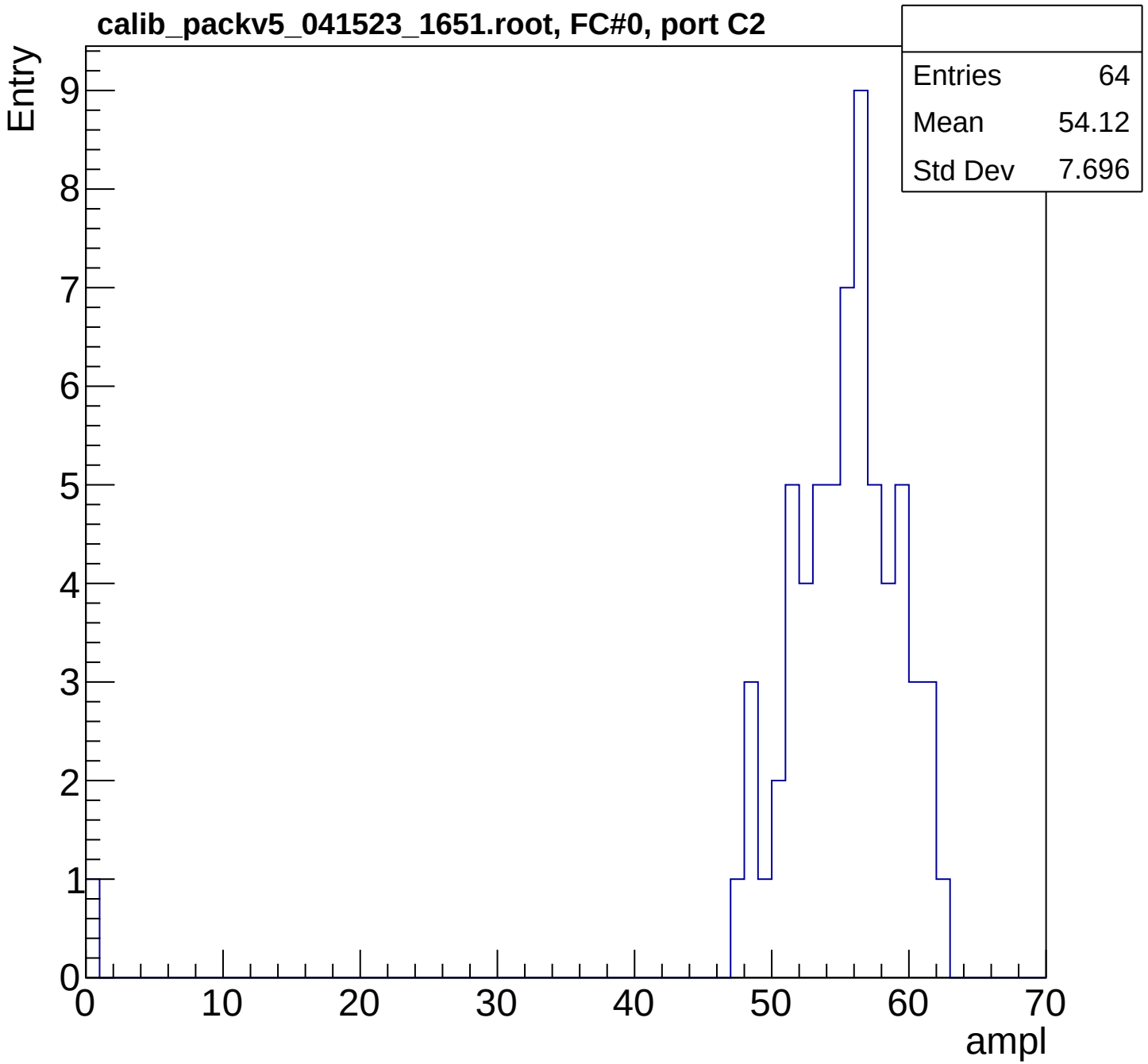
B1L103S, U17-ch41, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 54.12
Std Dev 7.696
Entry
ampl
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3
4
5
6
7
8
9
0
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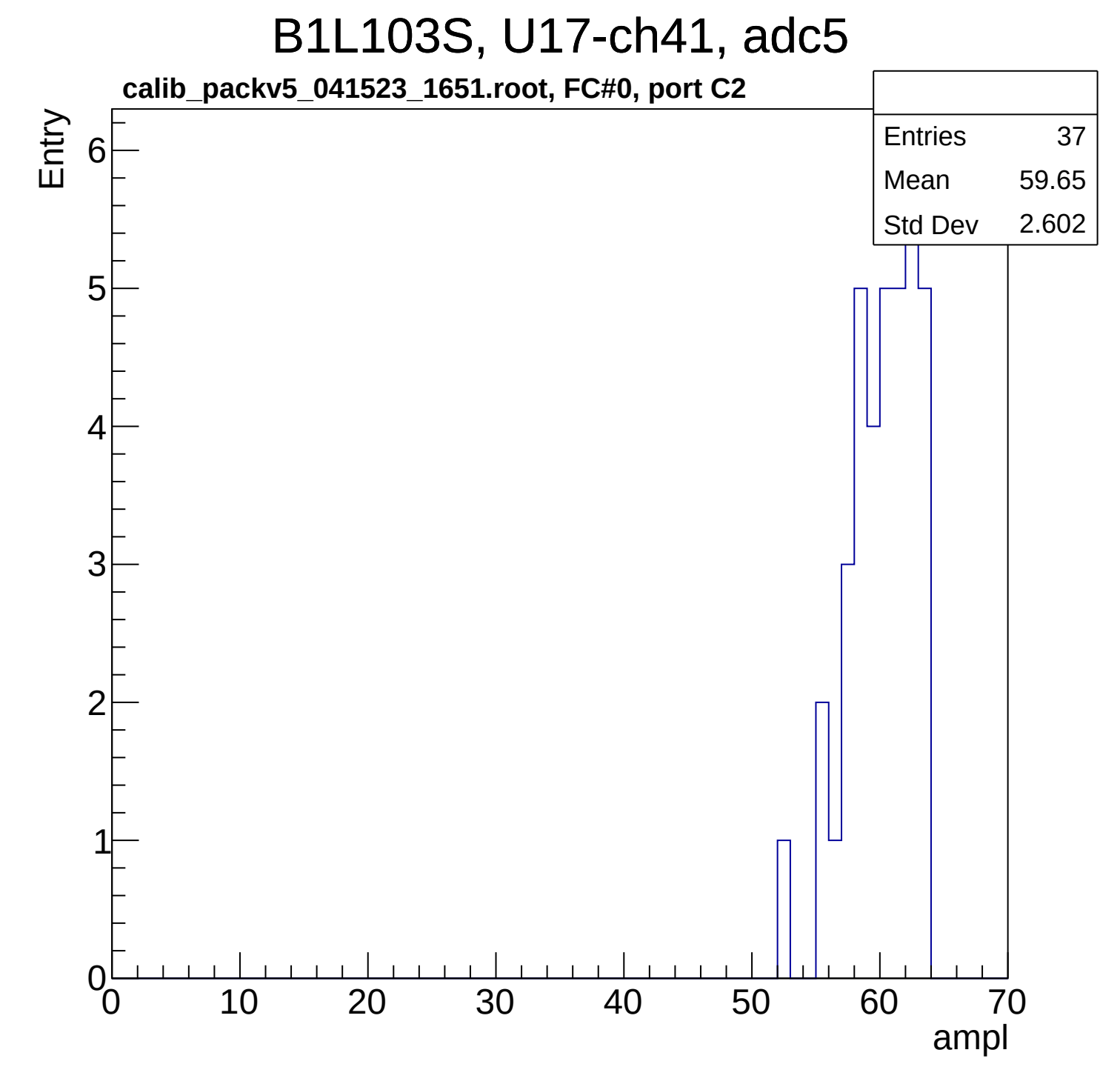
B1L103S, U17-ch41, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 37
Mean 59.65
Std Dev 2.602
Entry
ampl
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3
4
5
6
0
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20
30
40
50
60
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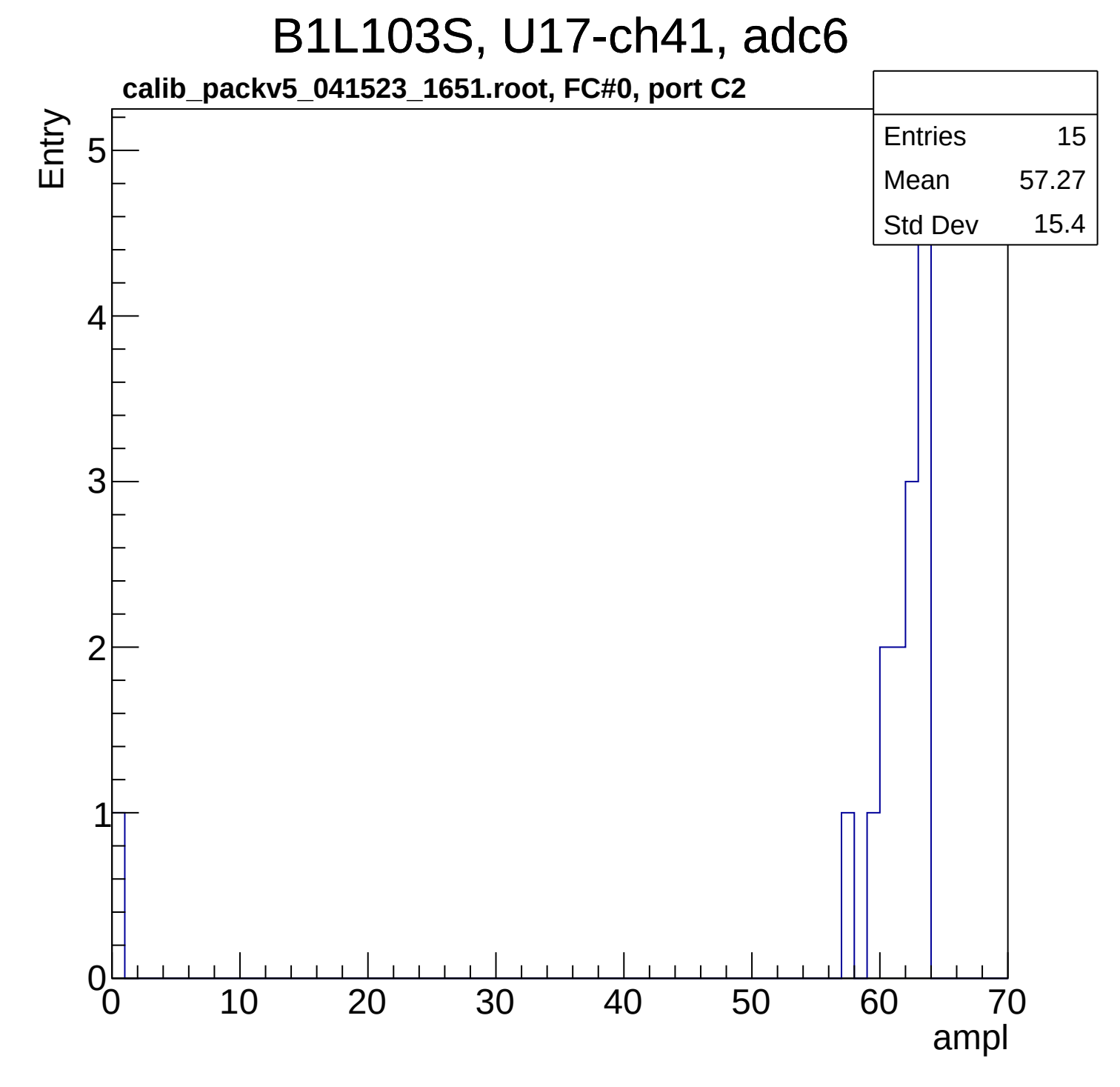
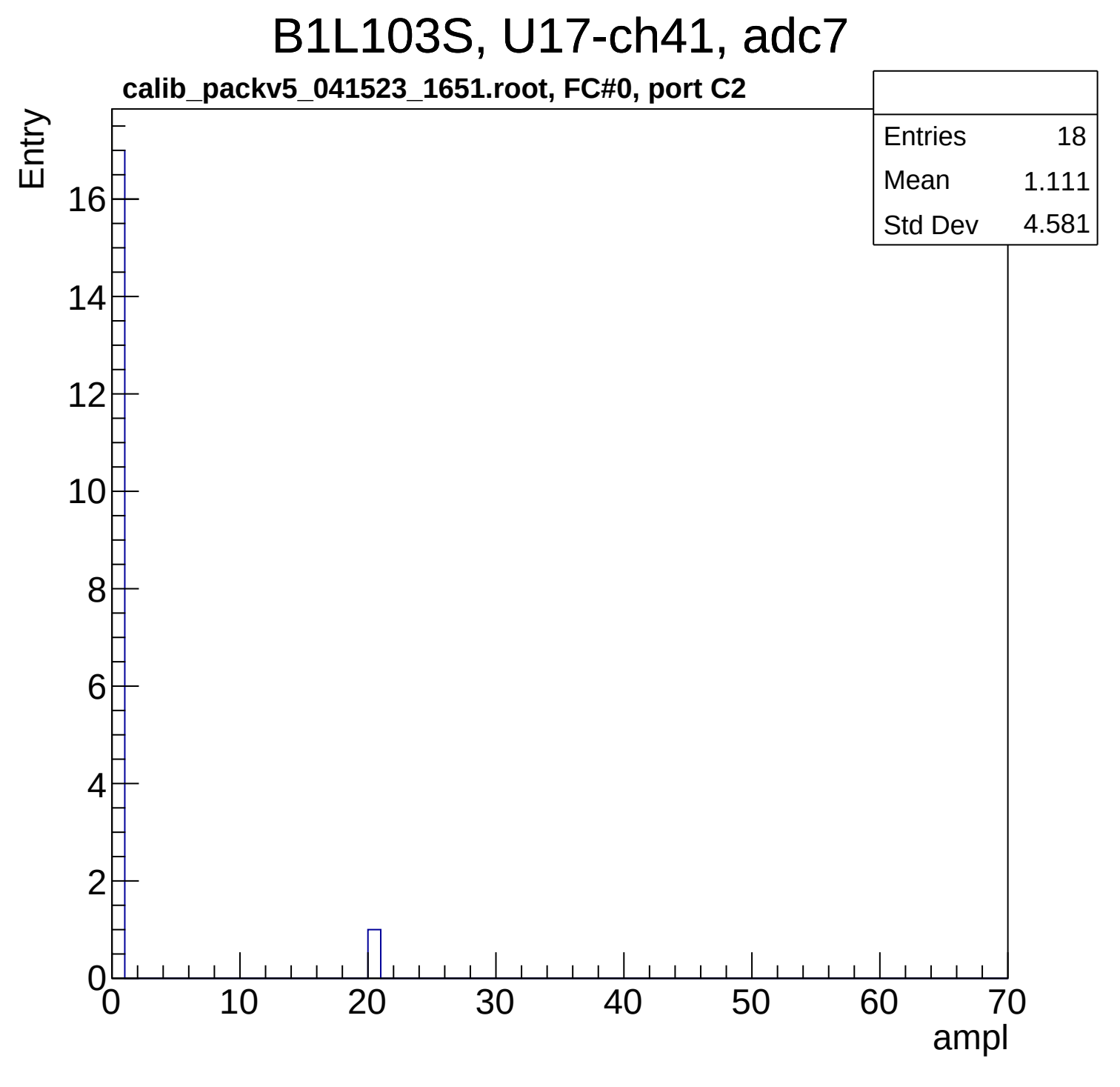

B1L103S, U17-ch41, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 15
Mean 57.27
Std Dev 15.4
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch41, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 1.111
Std Dev 4.581
Entry
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6
8
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12
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16
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10
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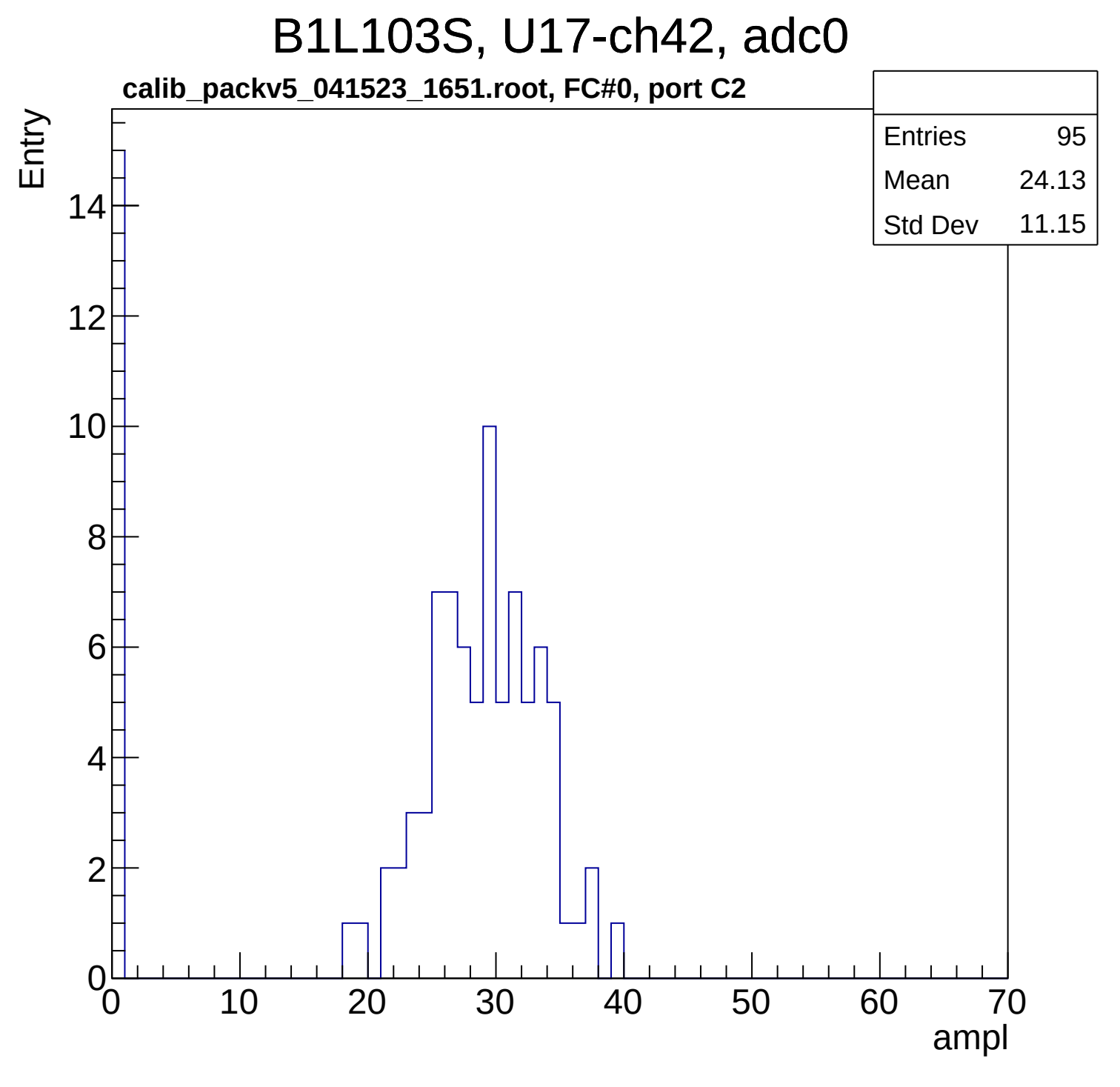
50
60
70
ampl


B1L103S, U17-ch42, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 95
Mean 24.13
Std Dev 11.15
Entry
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10
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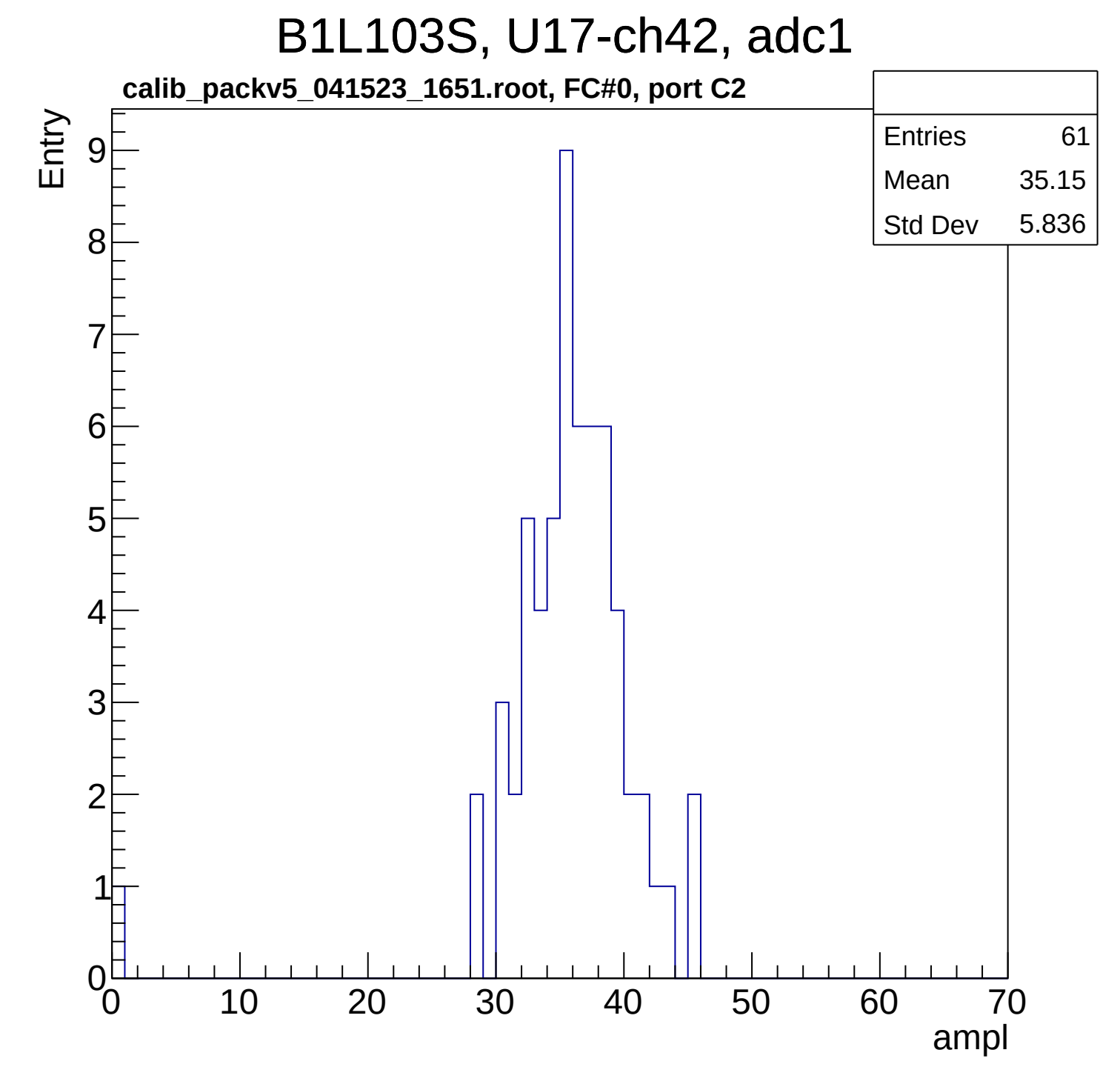
60
70
ampl


B1L103S, U17-ch42, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 35.15
Std Dev 5.836
Entry
ampl
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5
6
7
8
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0
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20
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40
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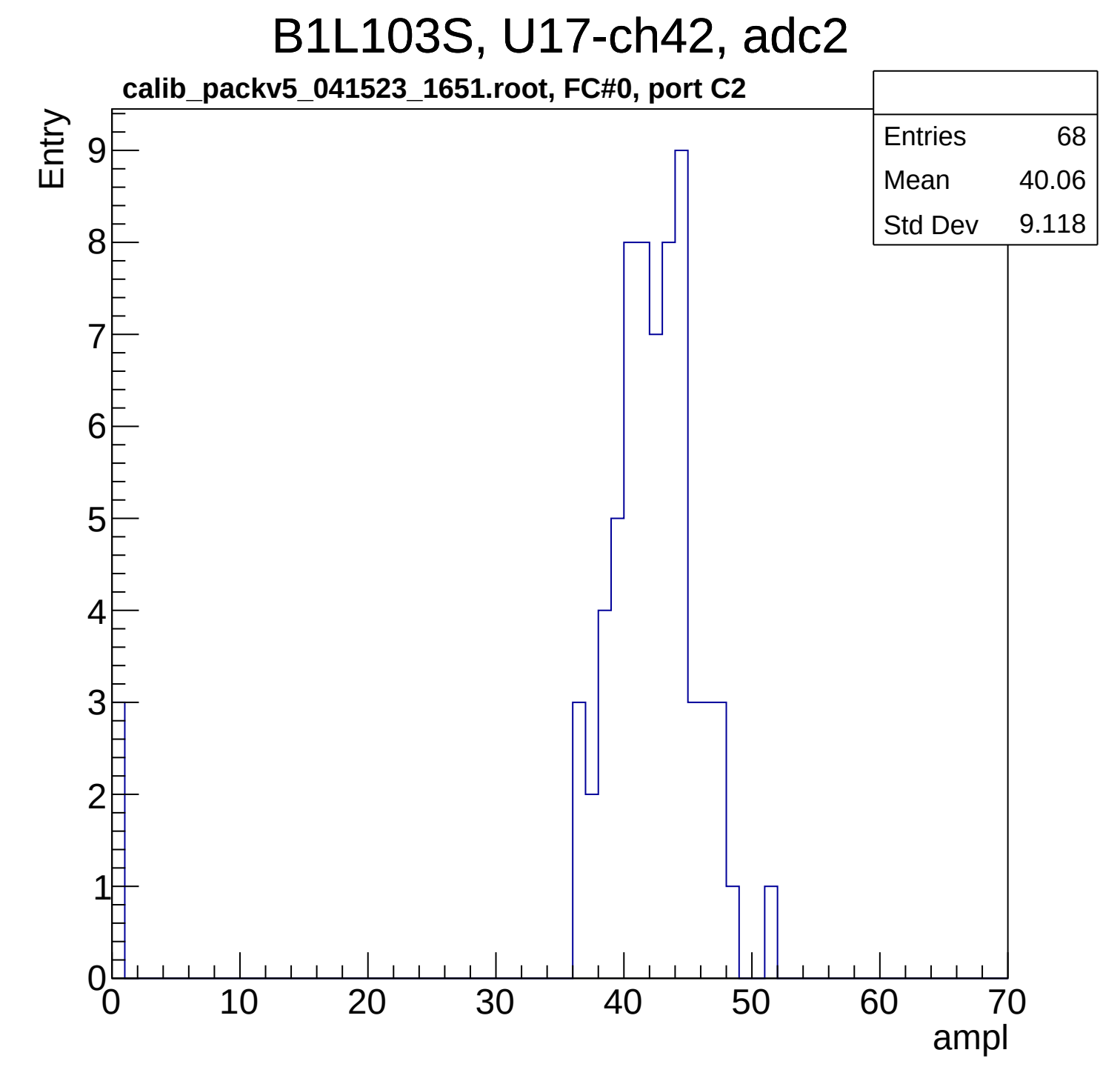
60
70


B1L103S, U17-ch42, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 40.06
Std Dev 9.118
Entry
ampl
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6
7
8
9
0
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40
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60
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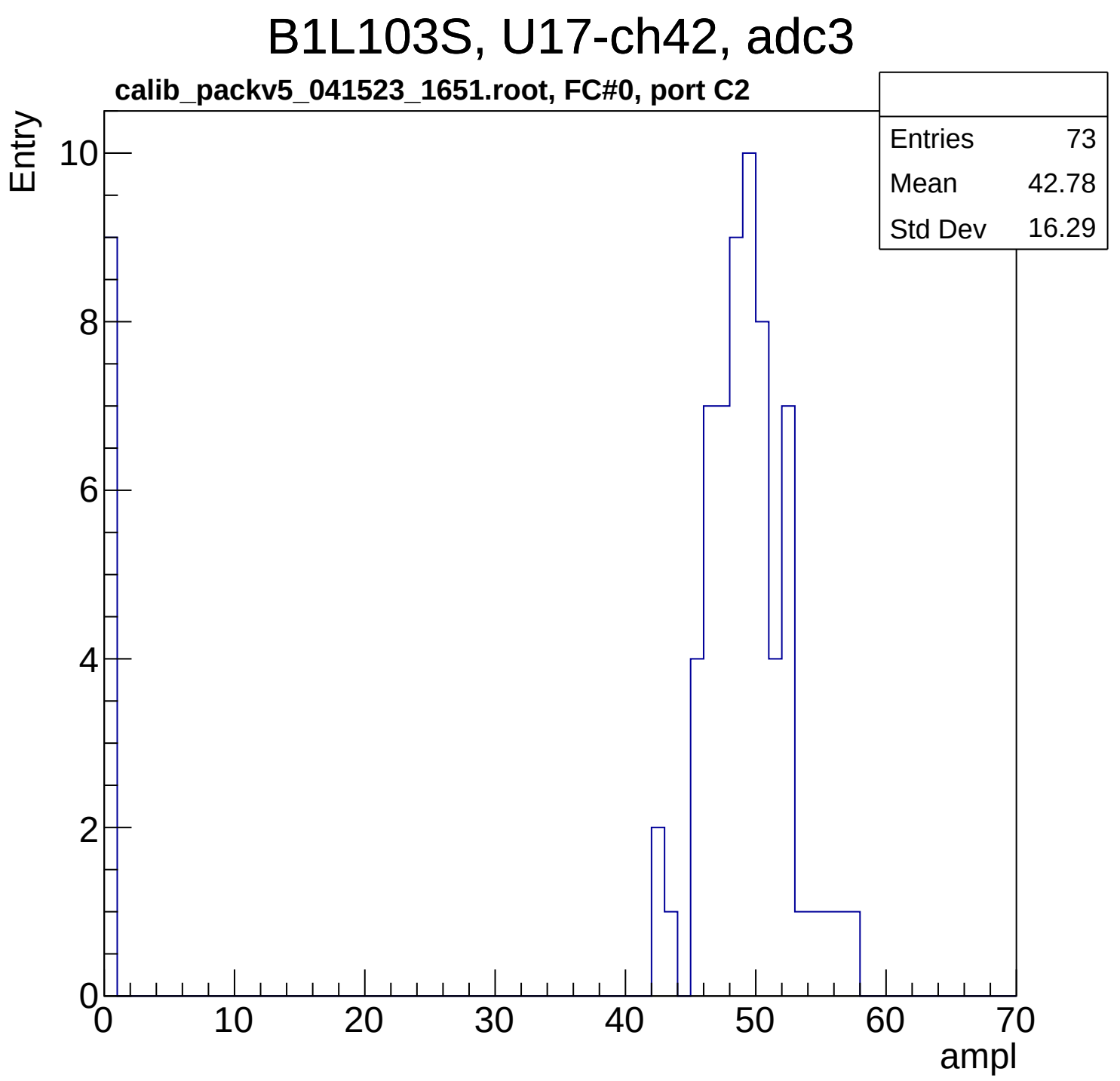
B1L103S, U17-ch42, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 42.78
Std Dev 16.29
Entry
ampl
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2
4
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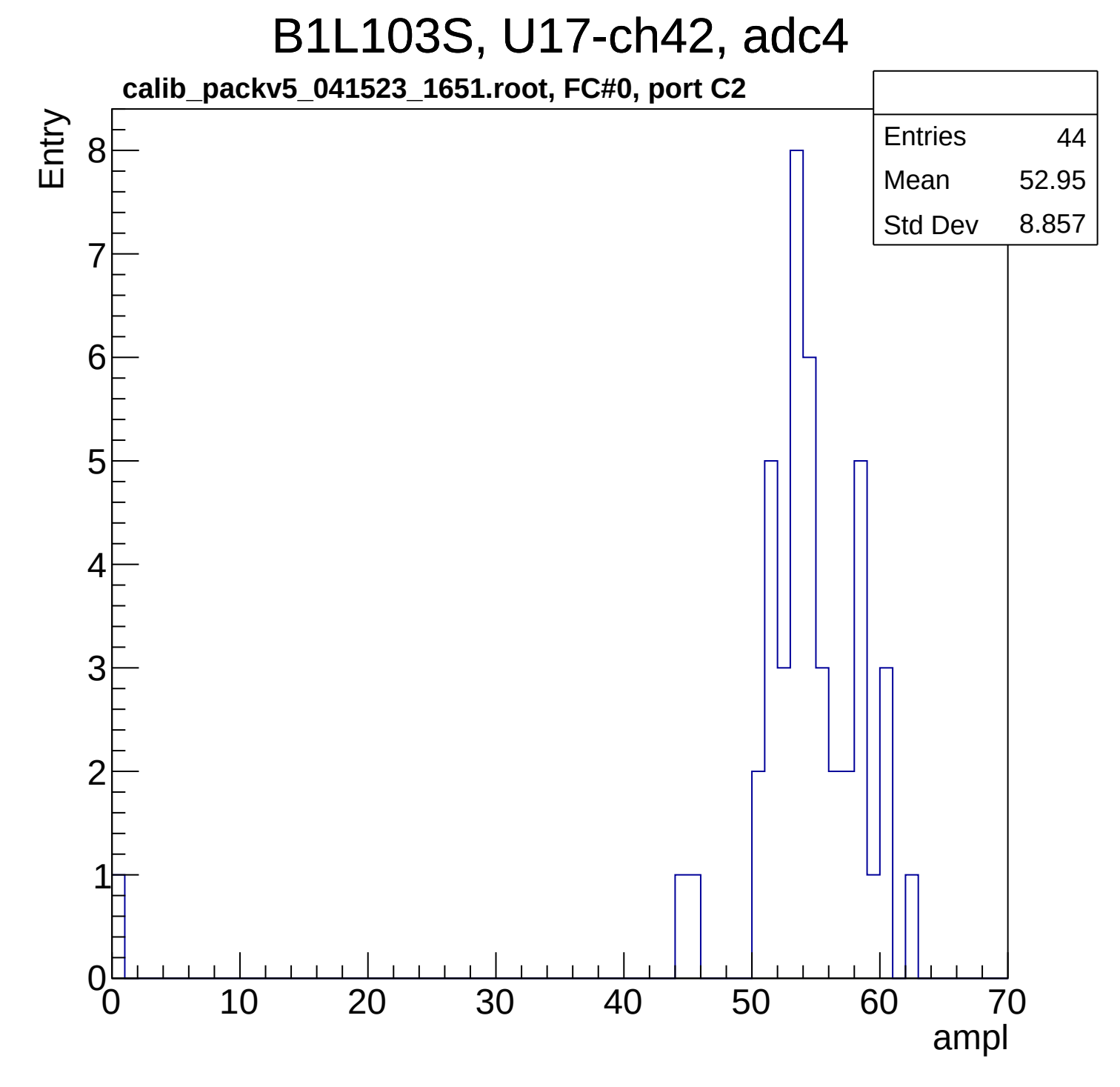
8
10
0
10
20
30
40
50
60
70


B1L103S, U17-ch42, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 52.95
Std Dev 8.857
Entry
ampl
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4
5
6
7
8
0
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20
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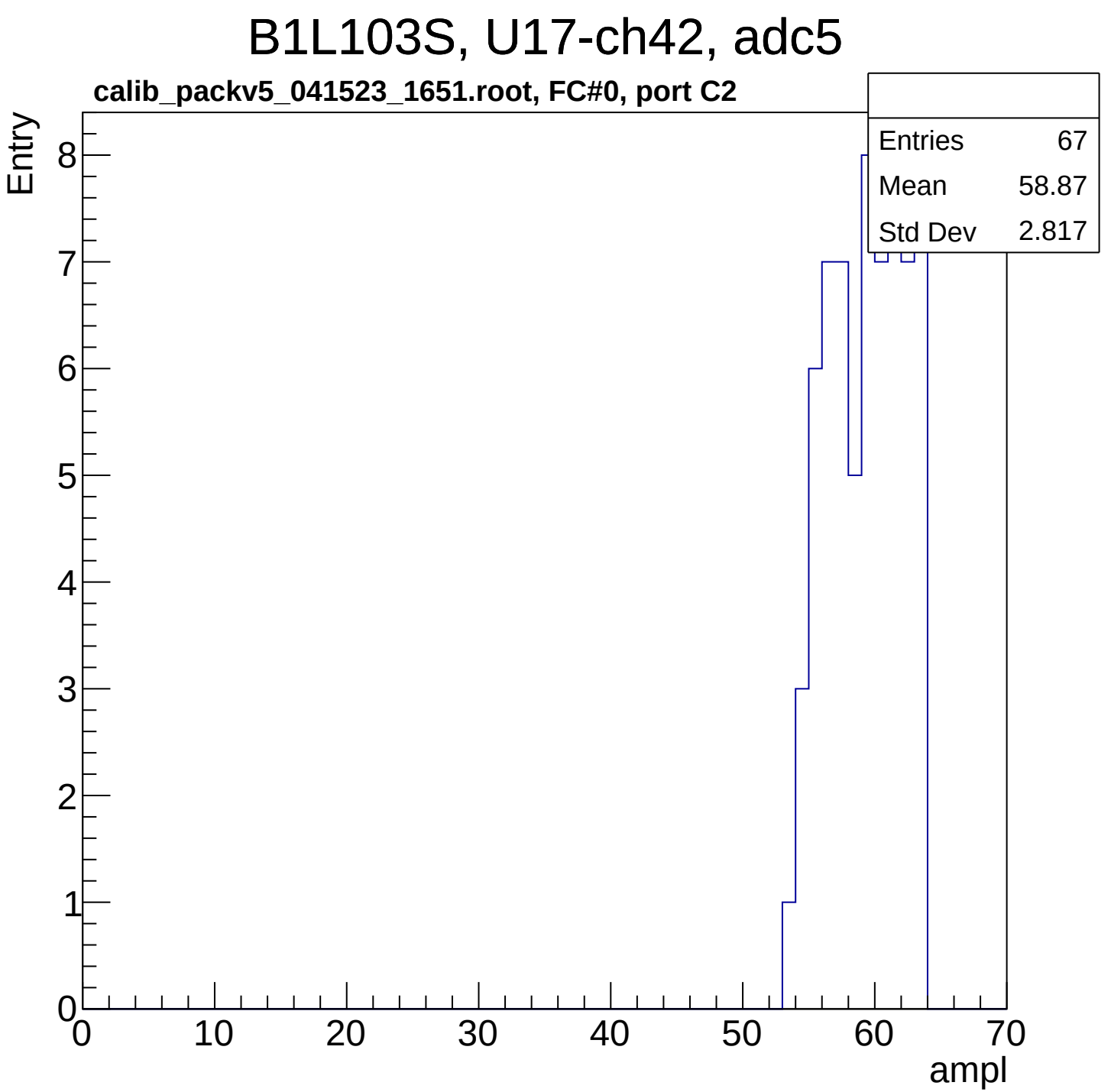
40
50
60
70


B1L103S, U17-ch42, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 58.87
Std Dev 2.817
Entry
ampl
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4
5
6
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60
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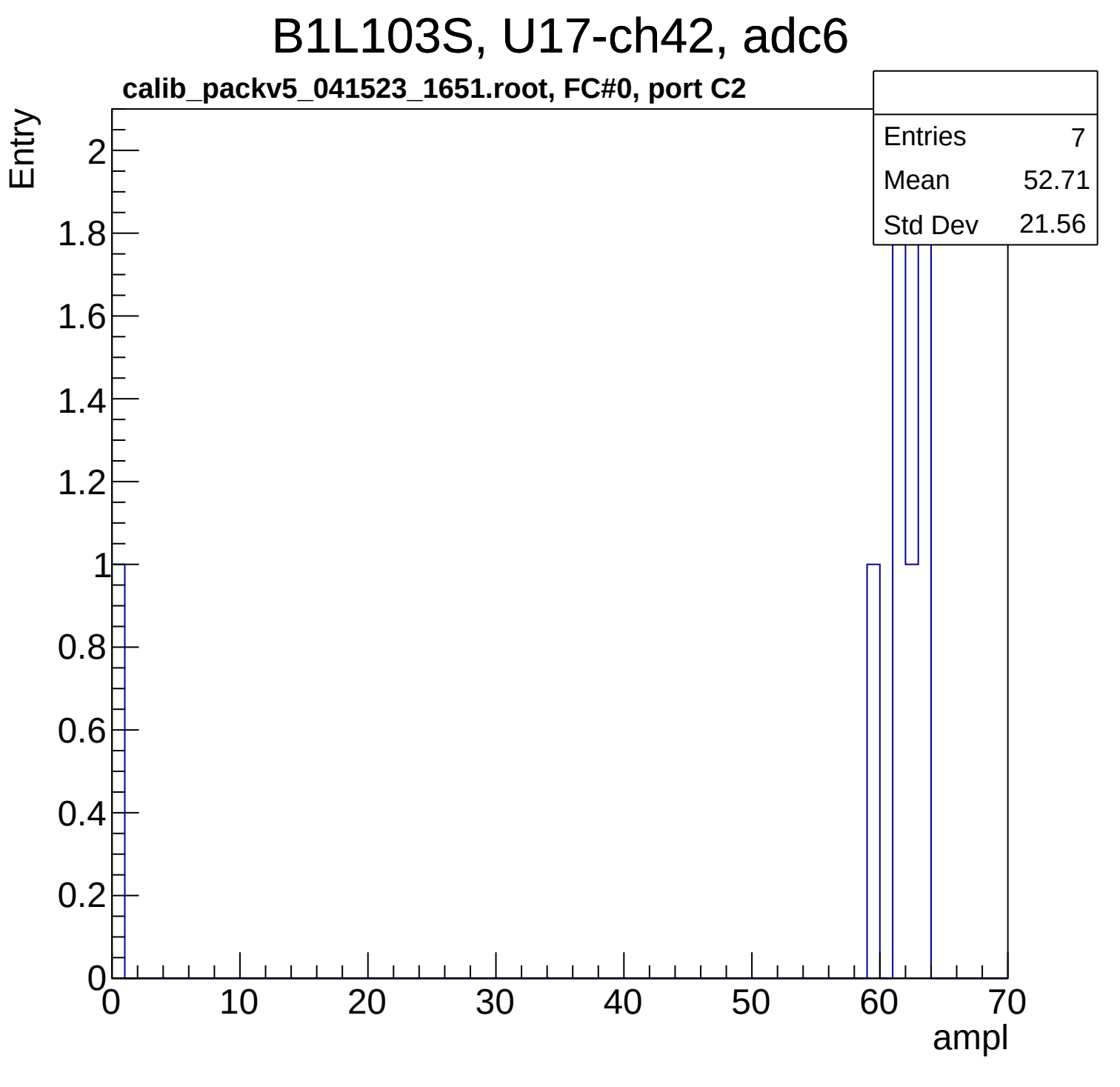
B1L103S, U17-ch42, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 52.71
Std Dev 21.56
Entry
ampl
0
0.2
0.4
0.6
0.8
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1.2
1.4
1.6
1.8
2
0
10
20
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60
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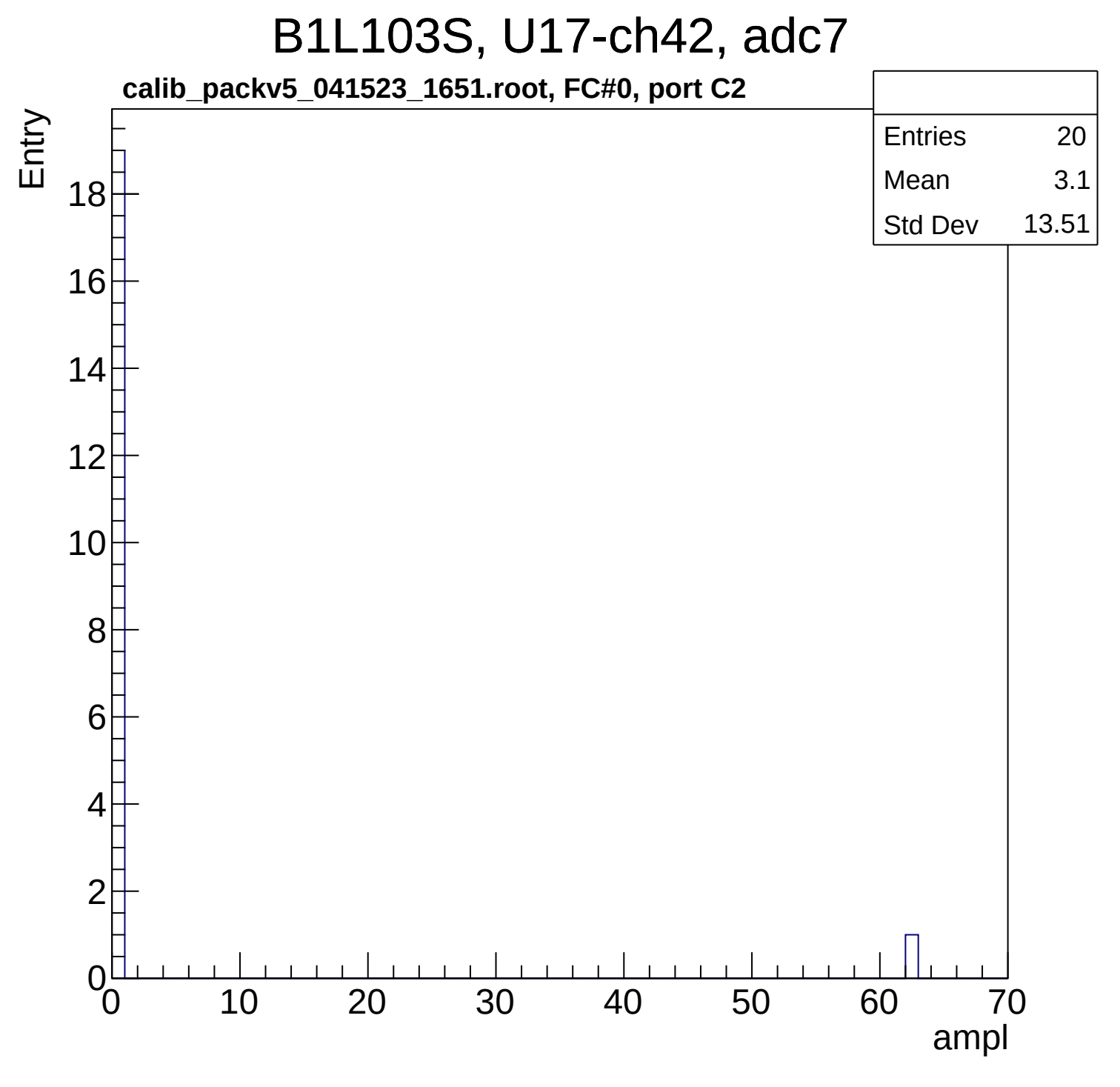
B1L103S, U17-ch42, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.1
Std Dev 13.51
Entry
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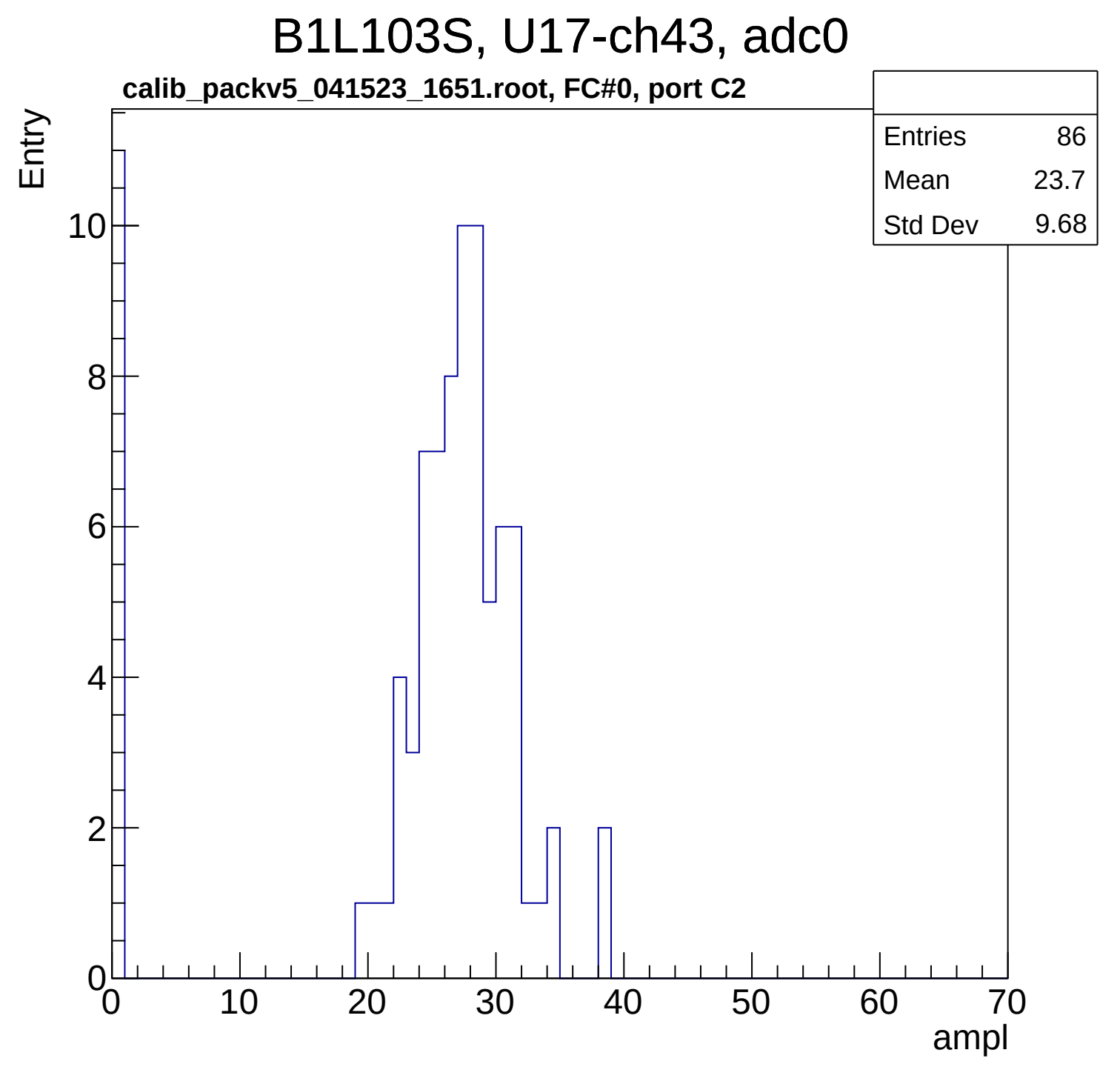
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch43, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 23.7
Std Dev 9.68
Entry
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2
4
6
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10
0
10
20
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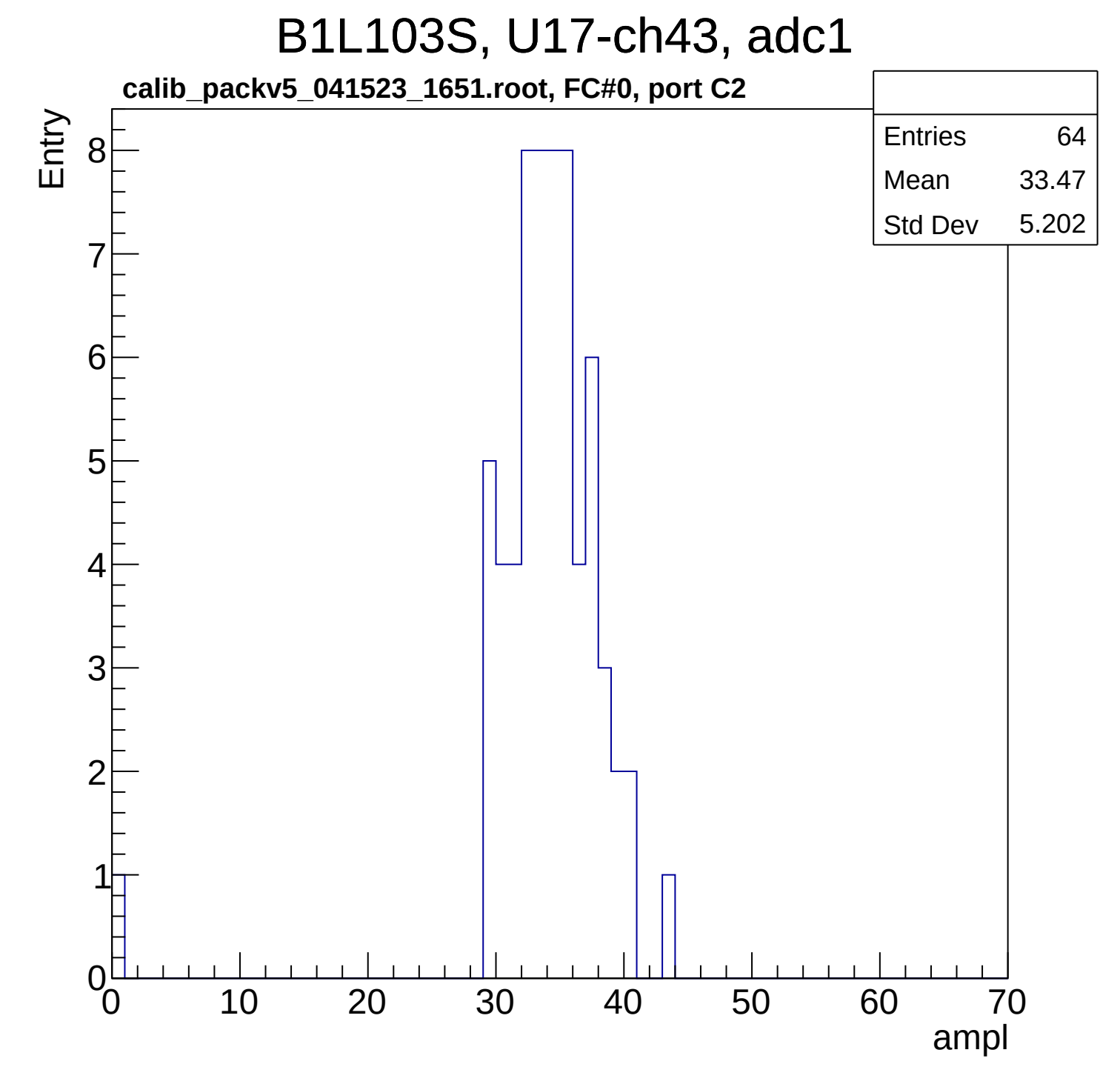
50
60
70
ampl


B1L103S, U17-ch43, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 33.47
Std Dev 5.202
Entry
ampl
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2
3
4
5
6
7
8
0
10
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60
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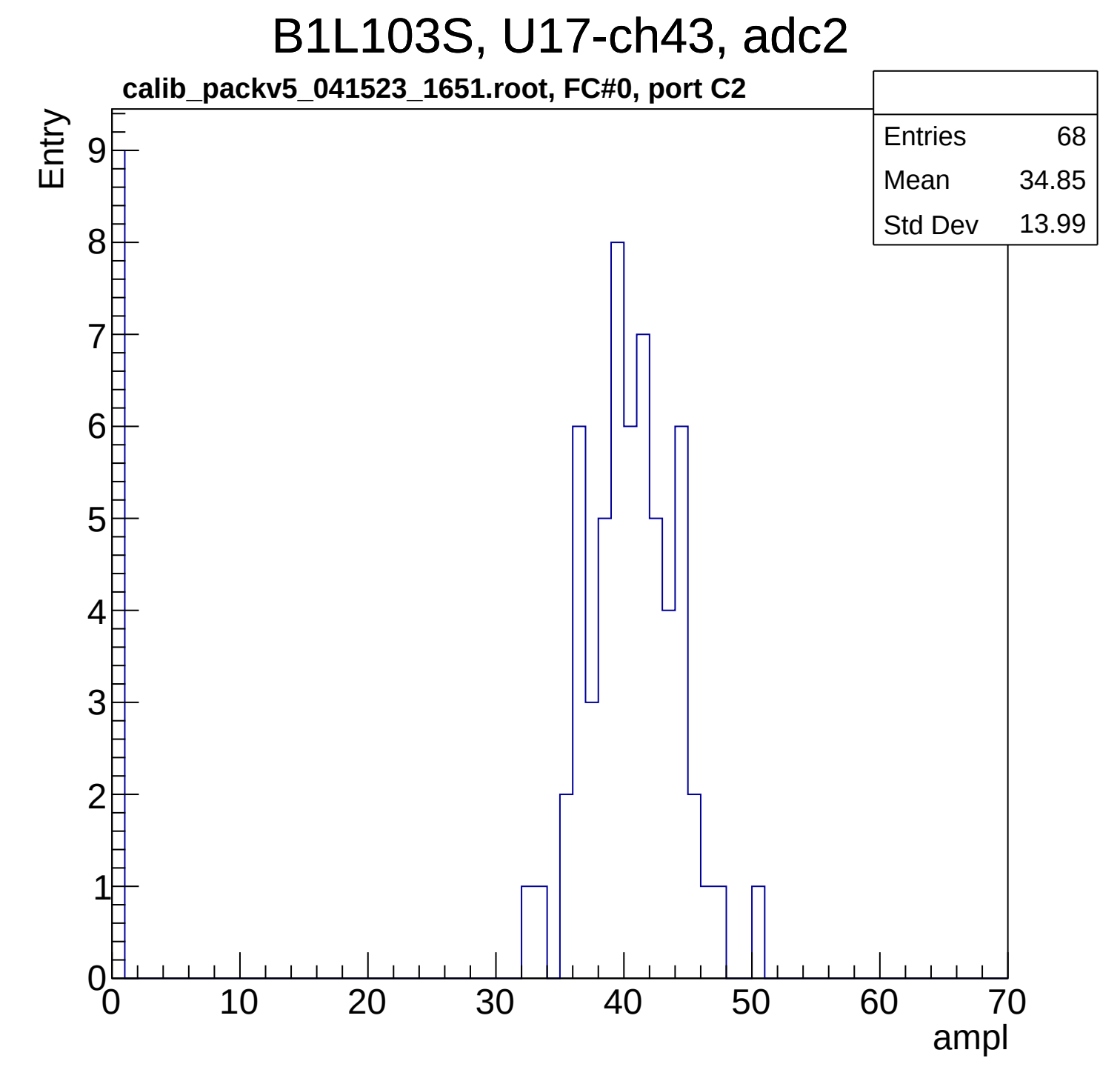
B1L103S, U17-ch43, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 34.85
Std Dev 13.99
Entry
ampl
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2
3
4
5
6
7
8
9
0
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60
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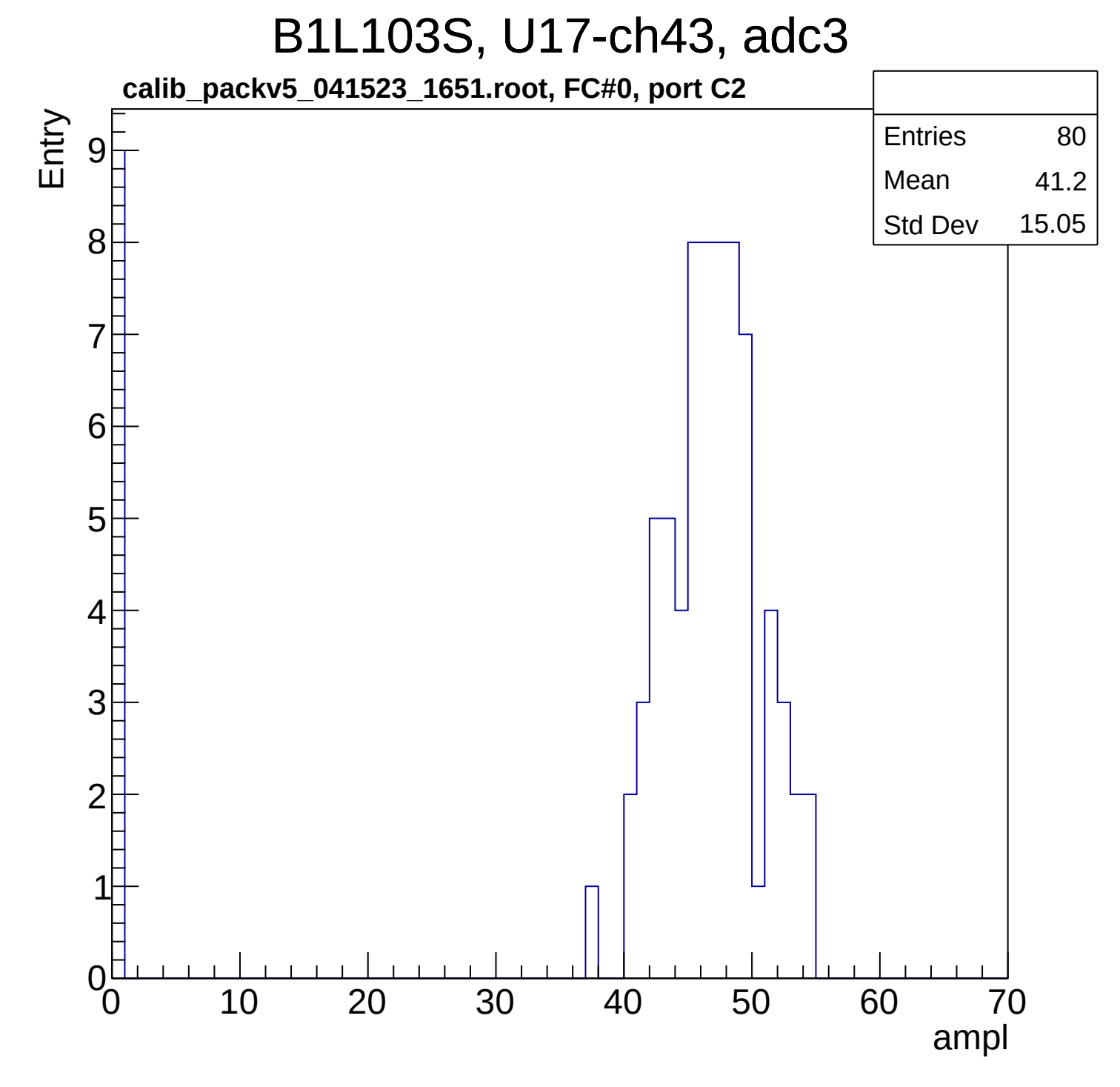
B1L103S, U17-ch43, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 41.2
Std Dev 15.05
Entry
ampl
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3
4
5
6
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8
9
0
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20
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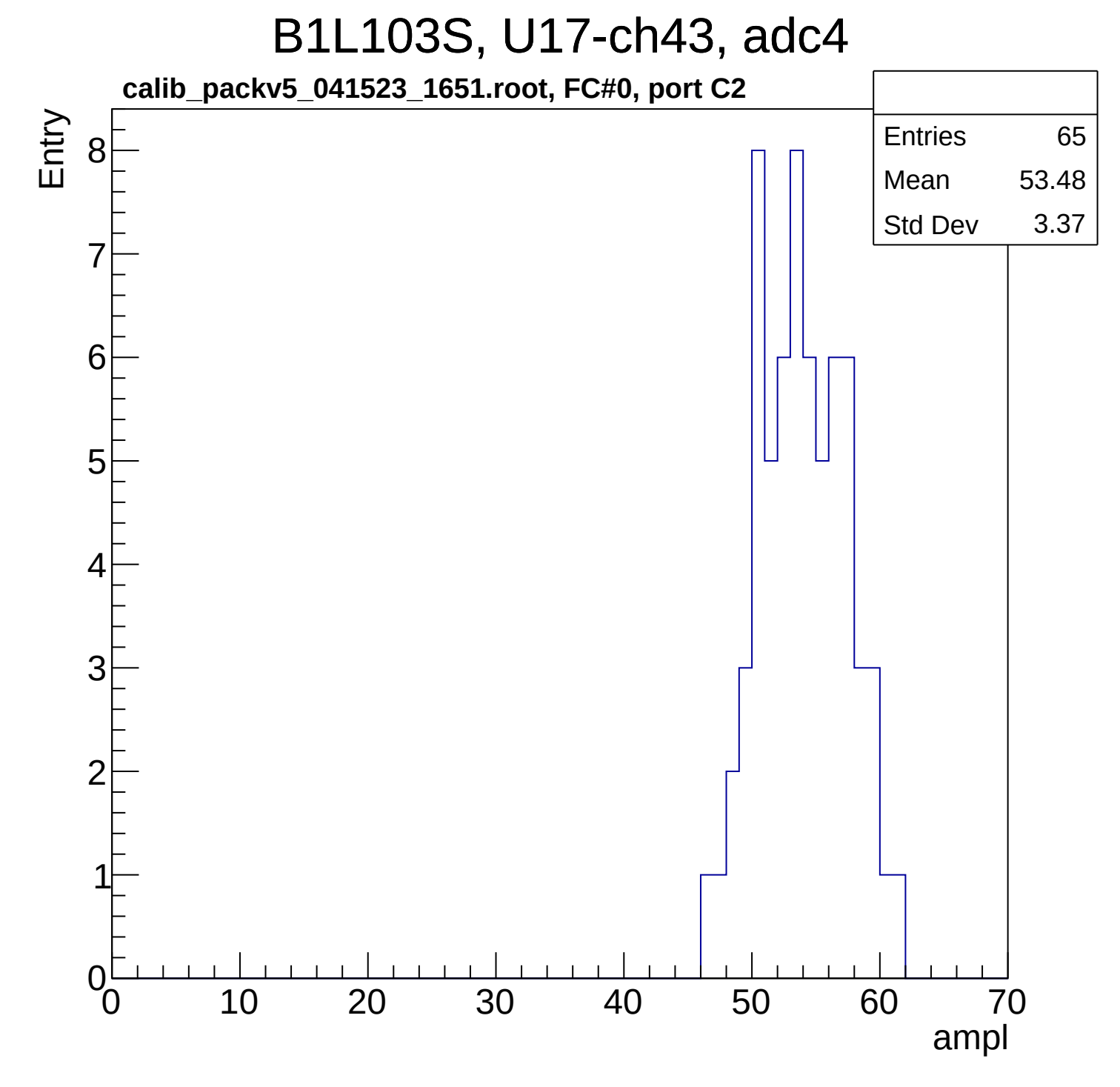
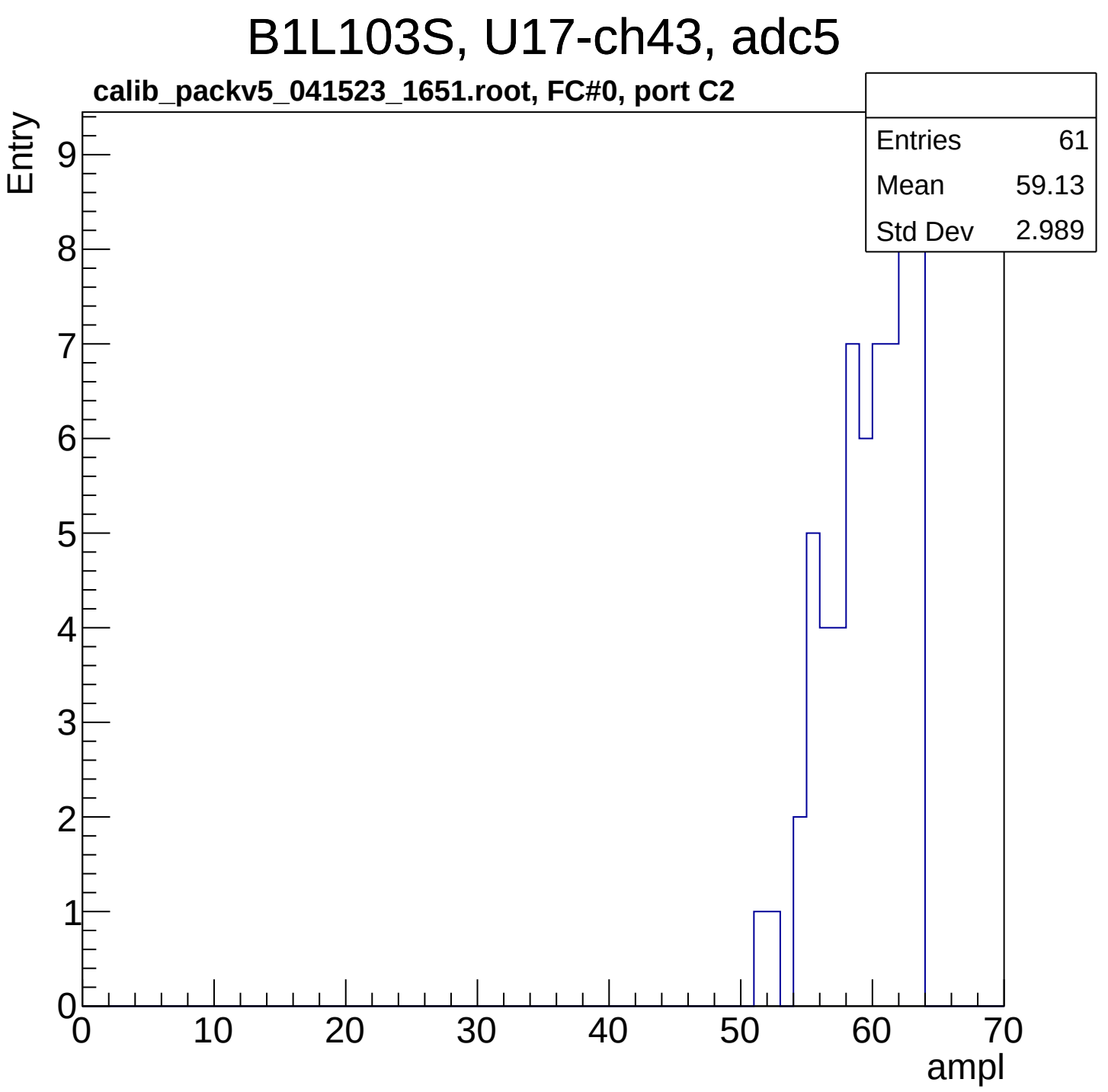

B1L103S, U17-ch43, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 53.48
Std Dev 3.37
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U17-ch43, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 59.13
Std Dev 2.989
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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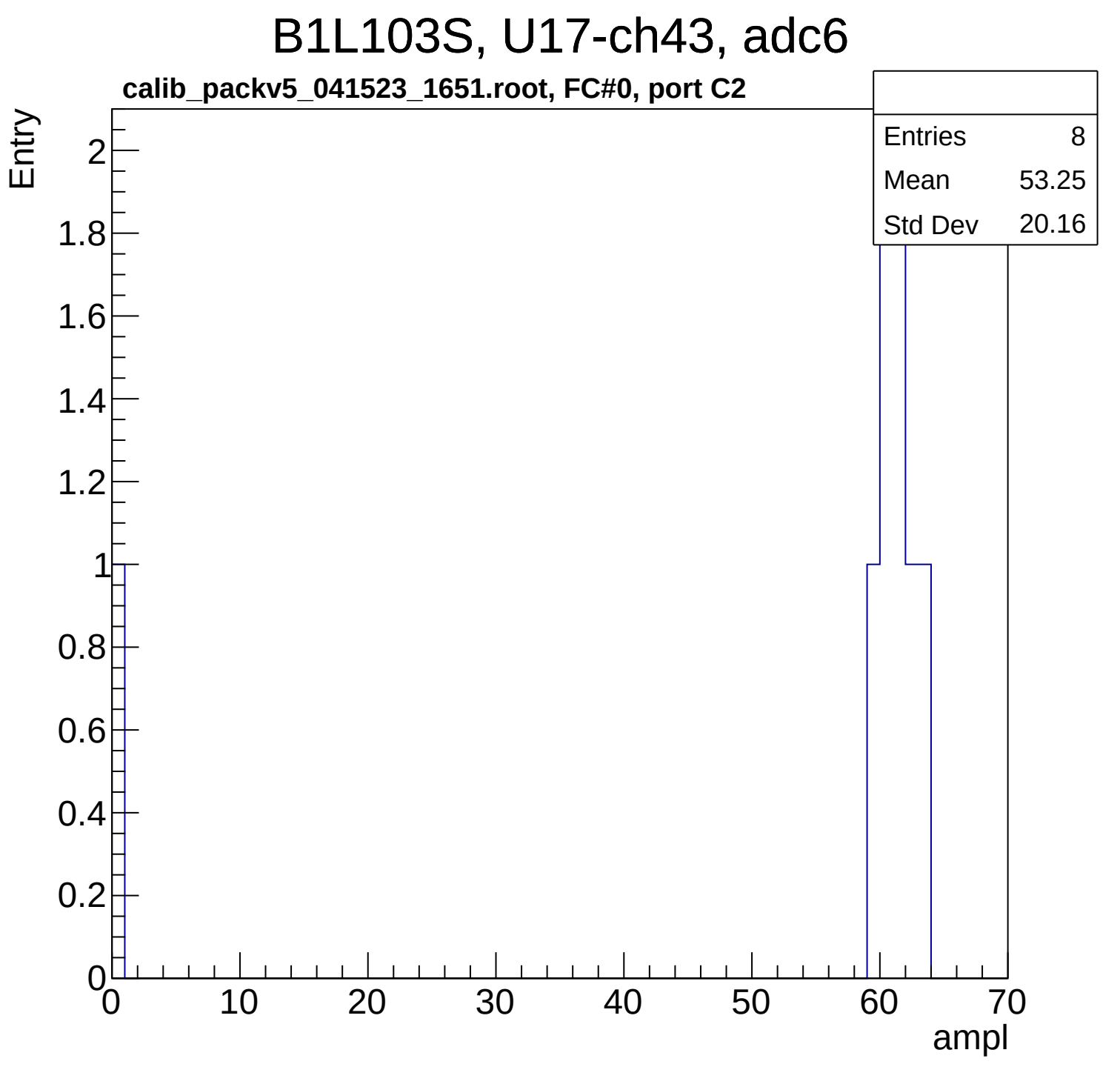
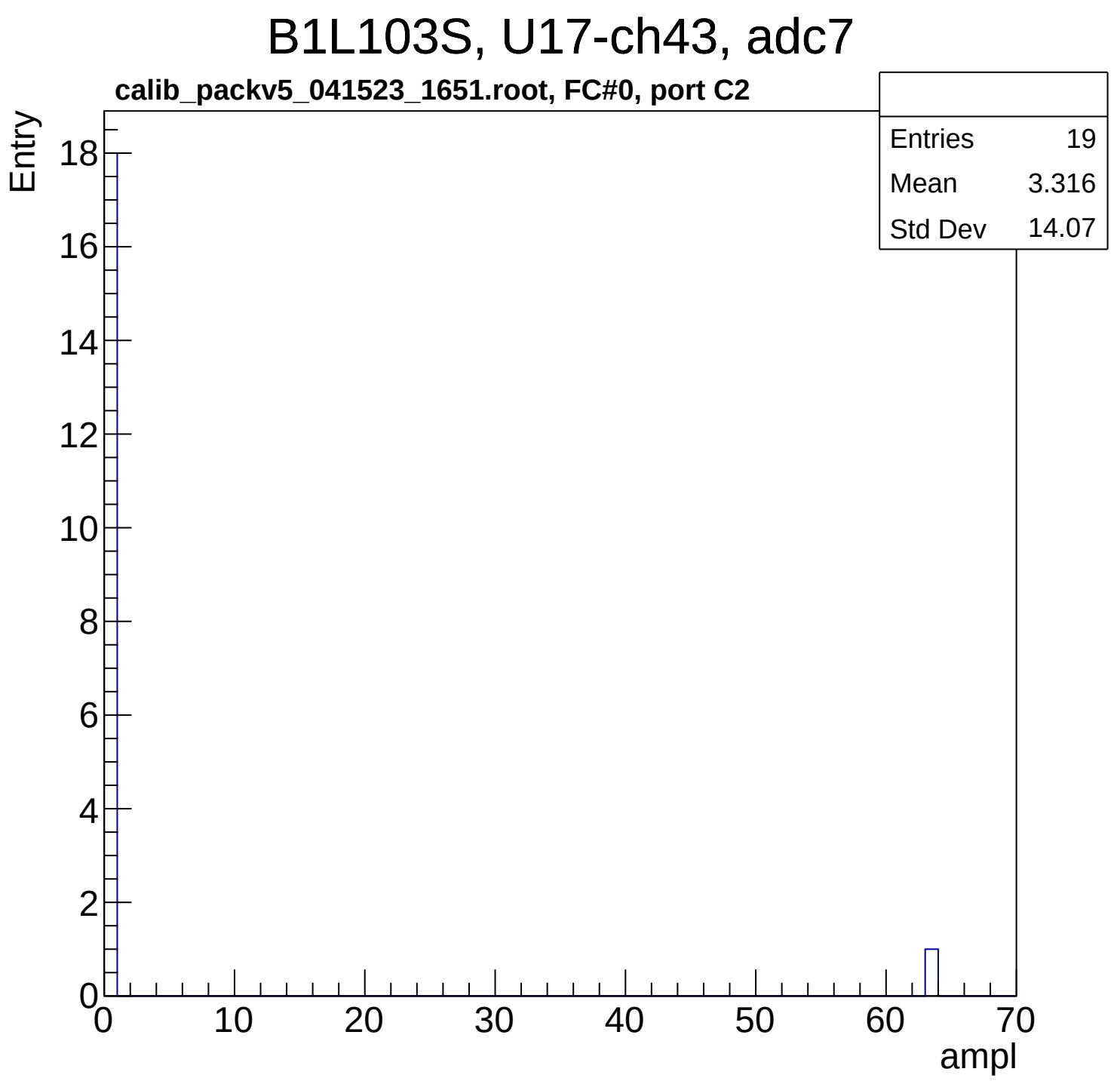

B1L103S, U17-ch43, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 53.25
Std Dev 20.16
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U17-ch43, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 3.316
Std Dev 14.07
Entry
0
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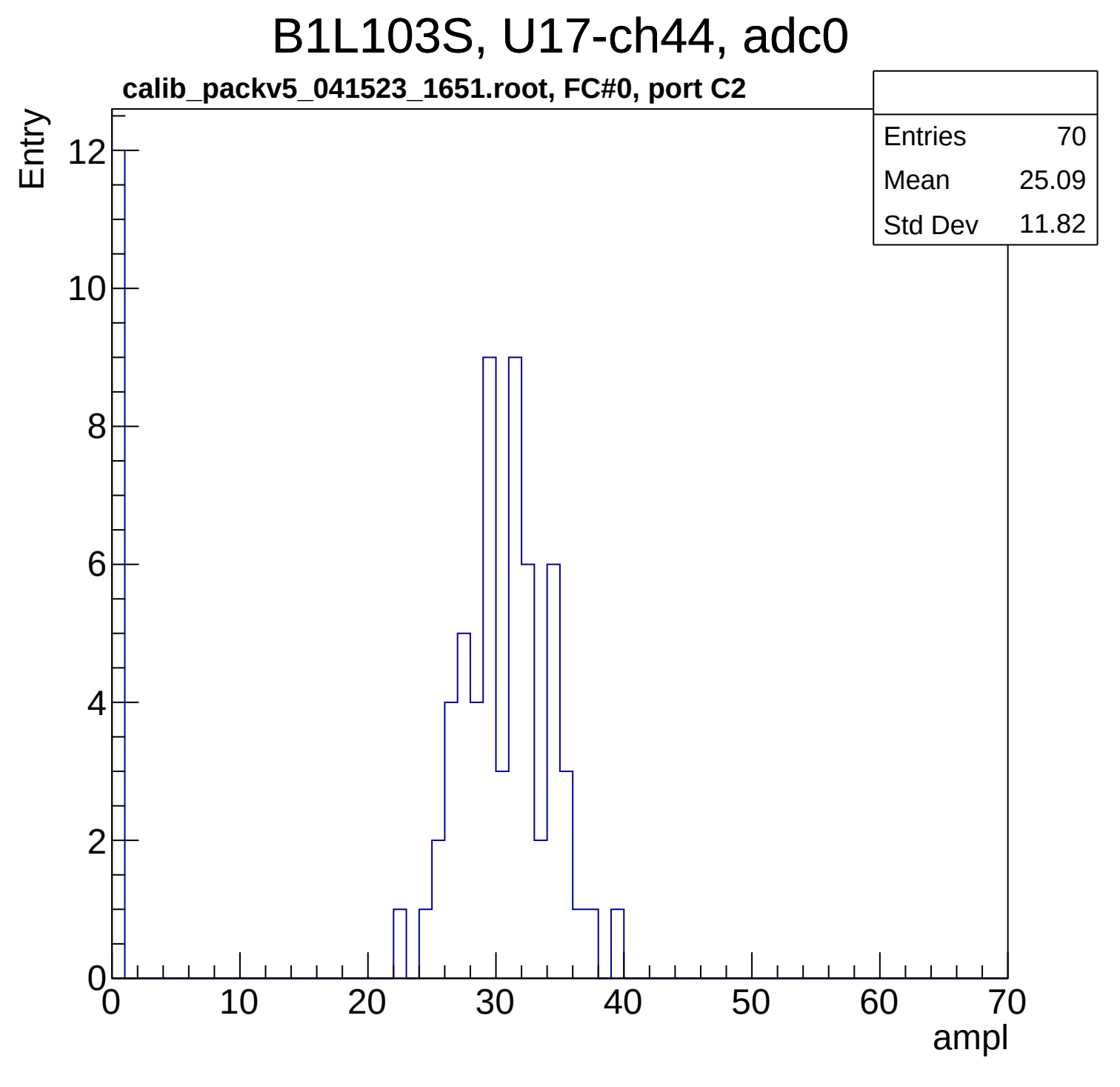
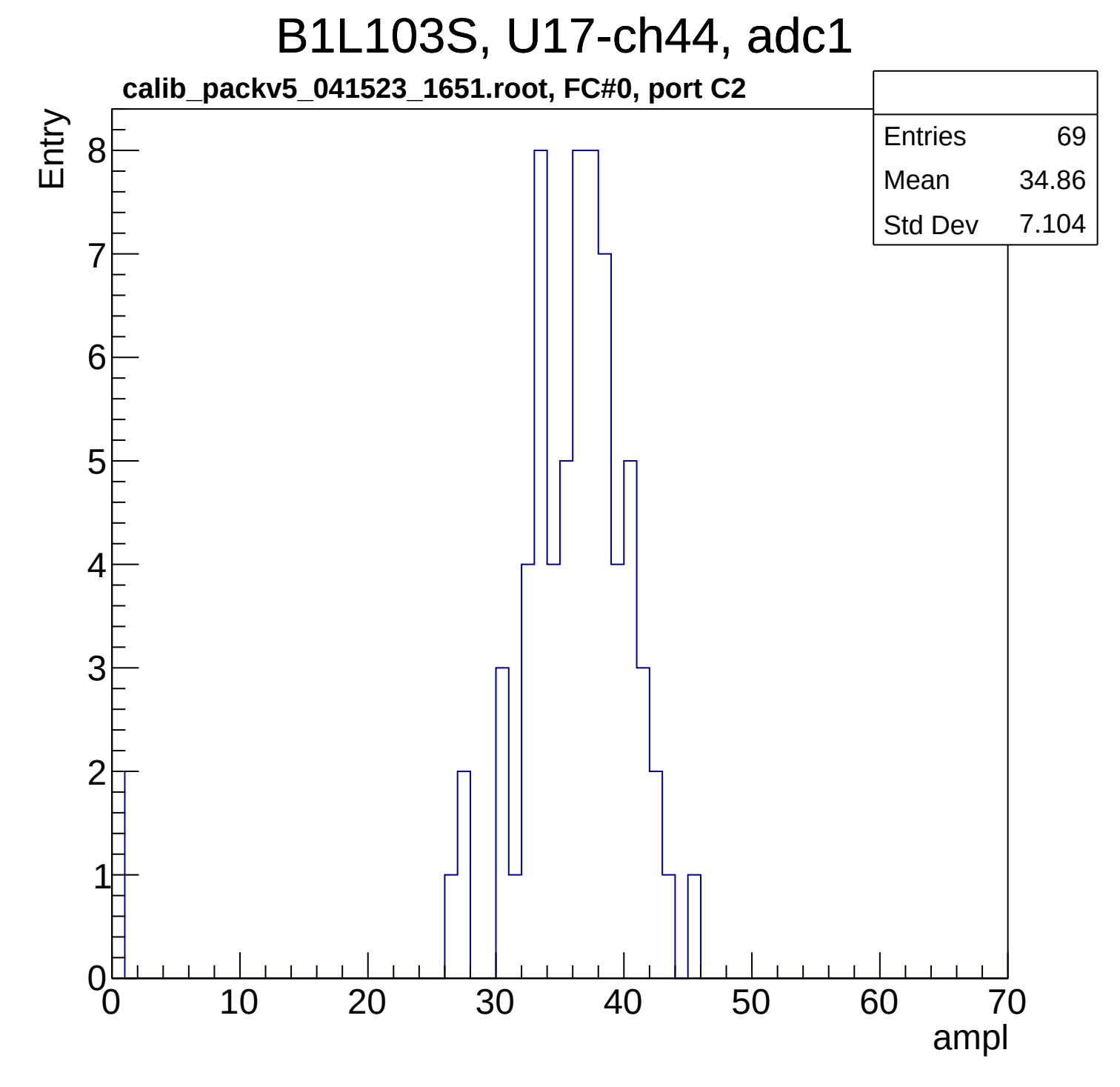
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch44, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 25.09
Std Dev 11.82
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch44, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 34.86
Std Dev 7.104
Entry
ampl
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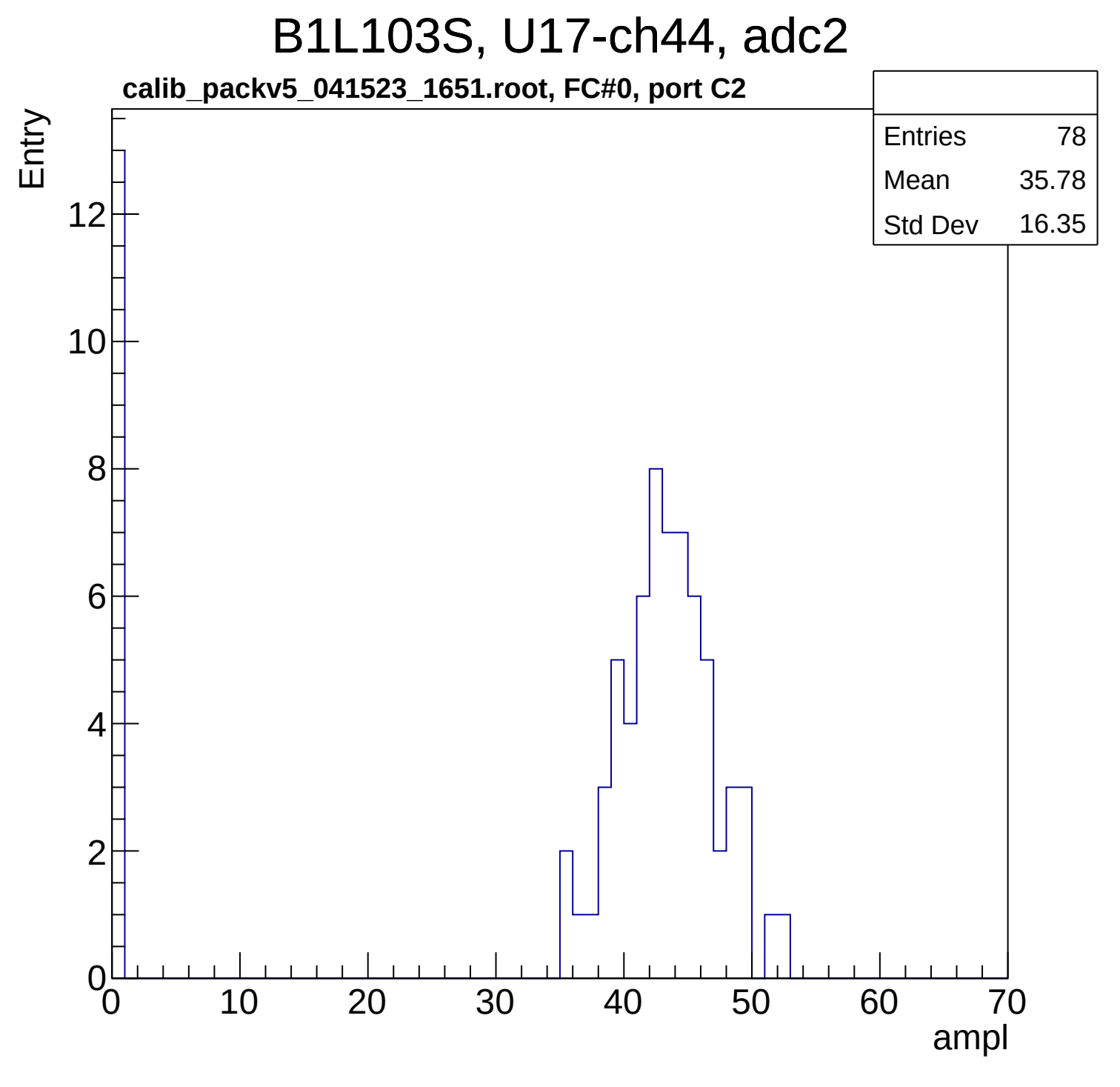
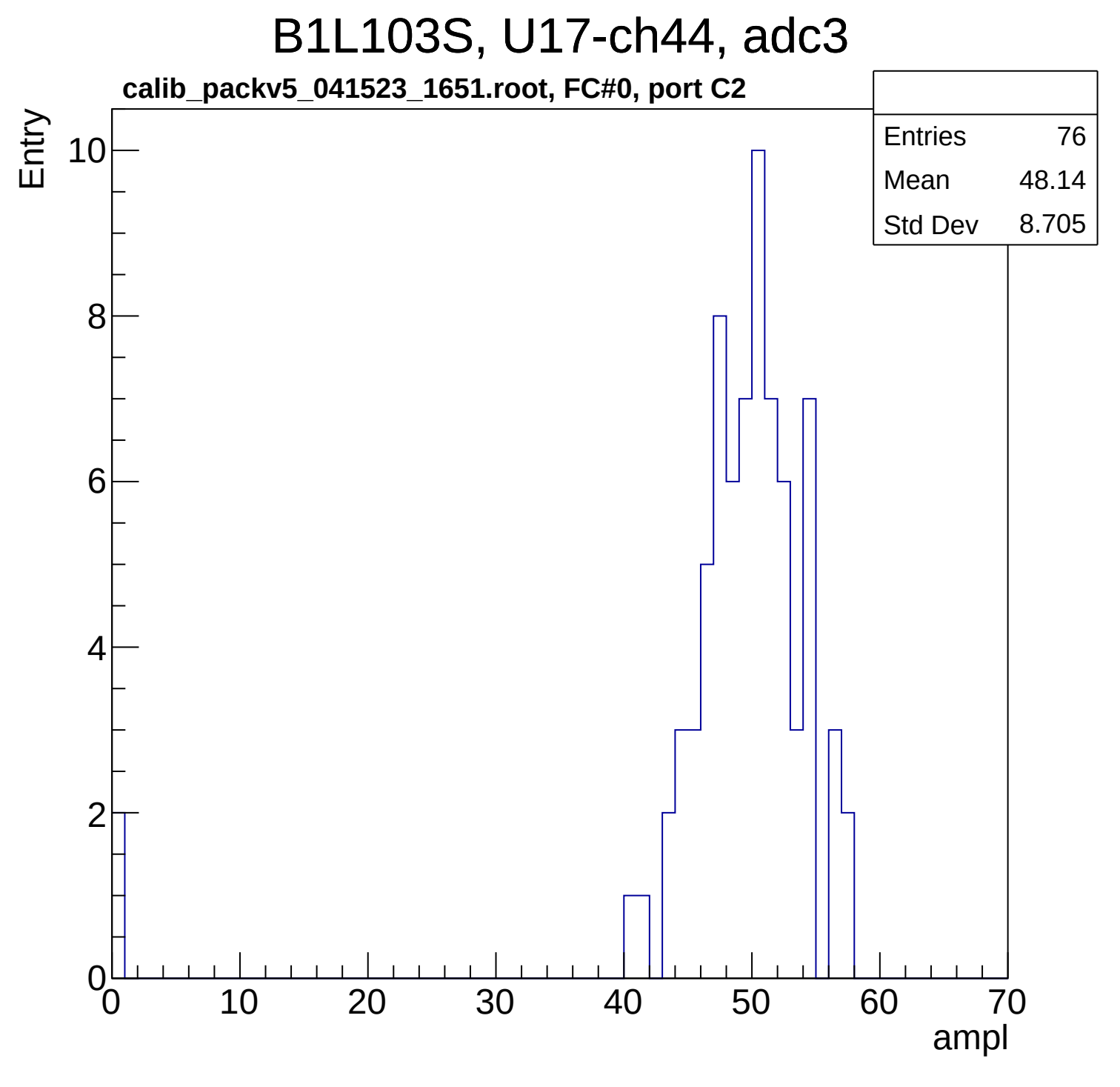
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U17-ch44, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 35.78
Std Dev 16.35
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch44, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 48.14
Std Dev 8.705
Entry
ampl
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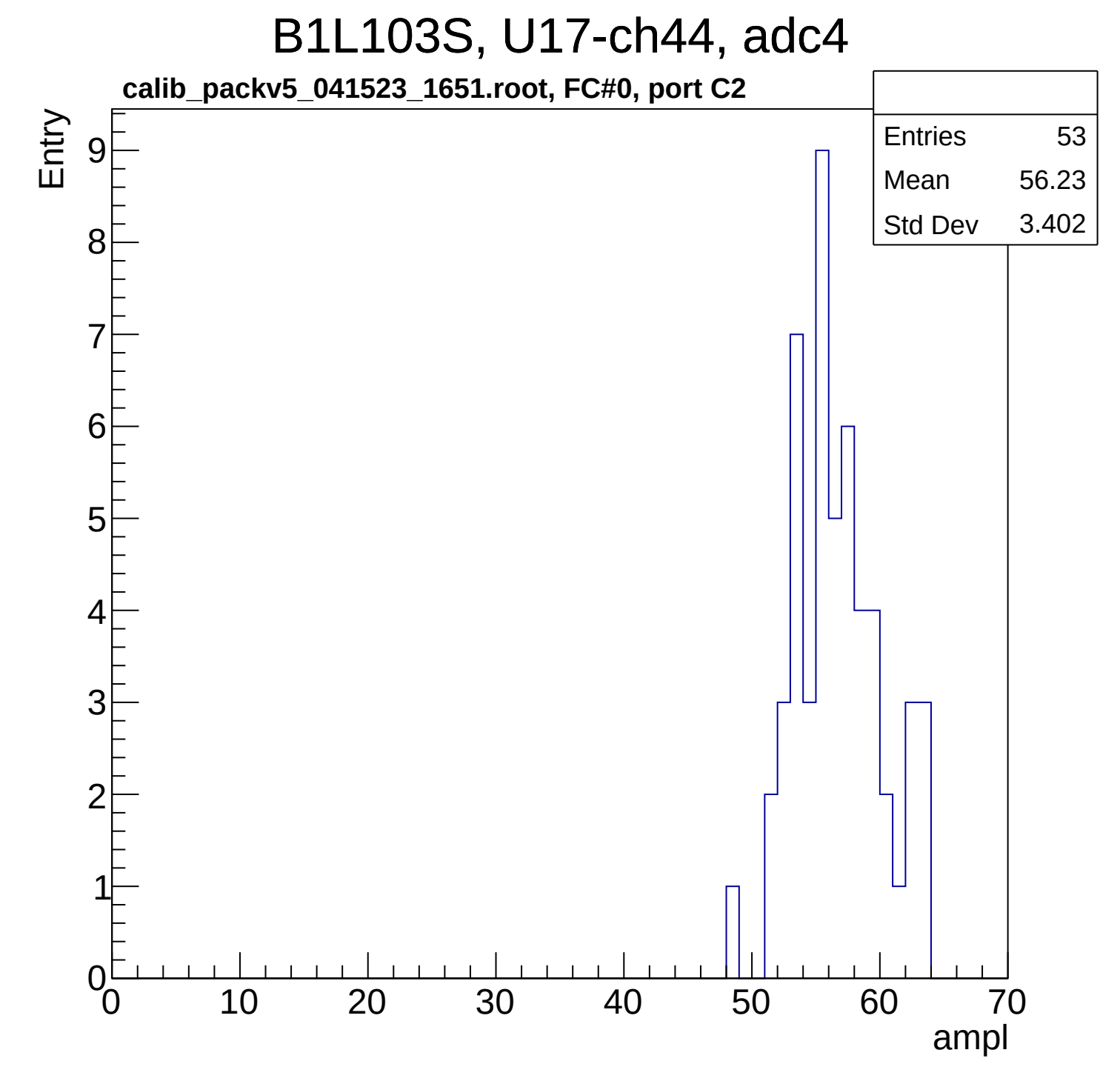
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U17-ch44, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 56.23
Std Dev 3.402
Entry
ampl
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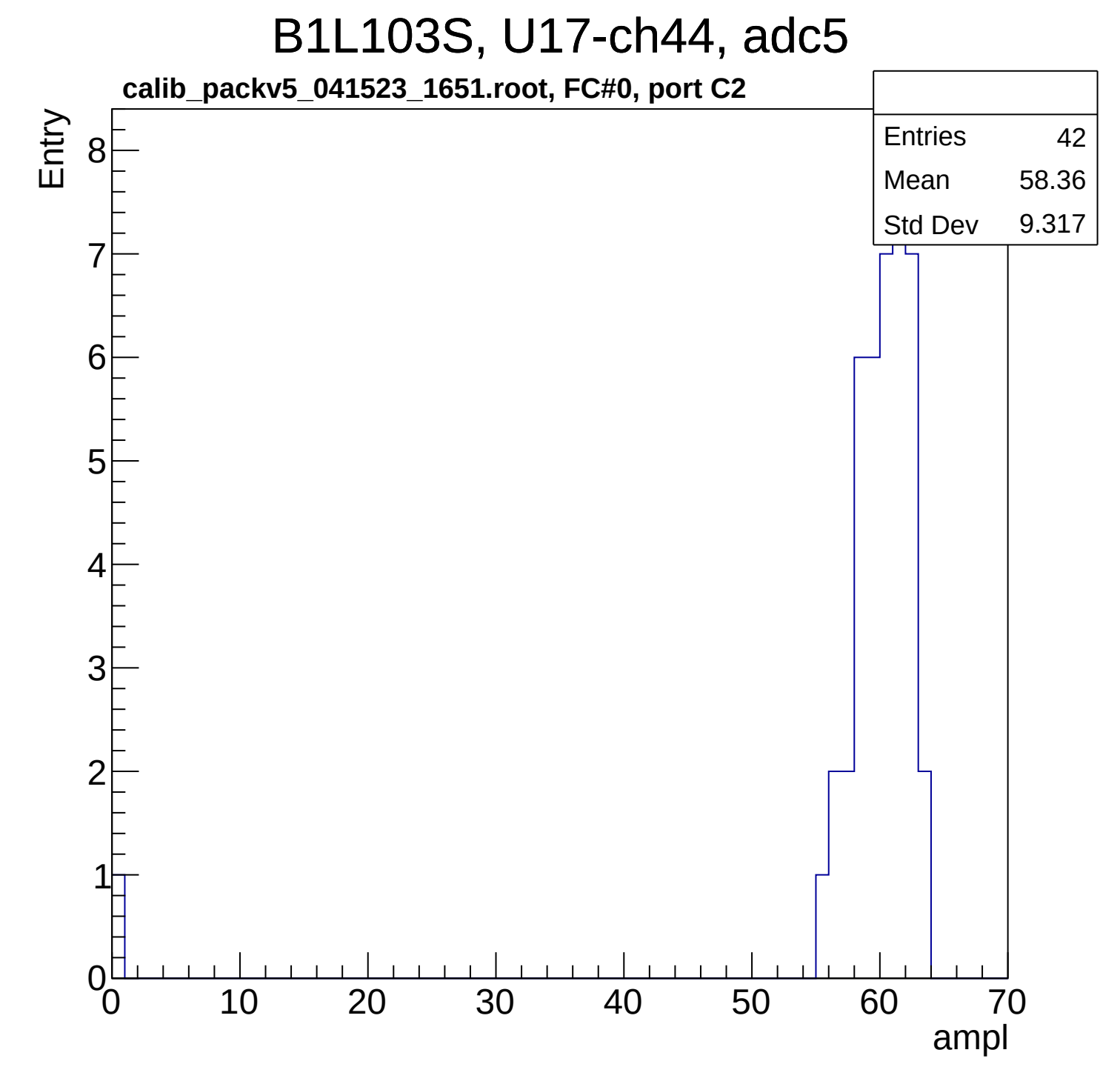
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U17-ch44, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 42
Mean 58.36
Std Dev 9.317
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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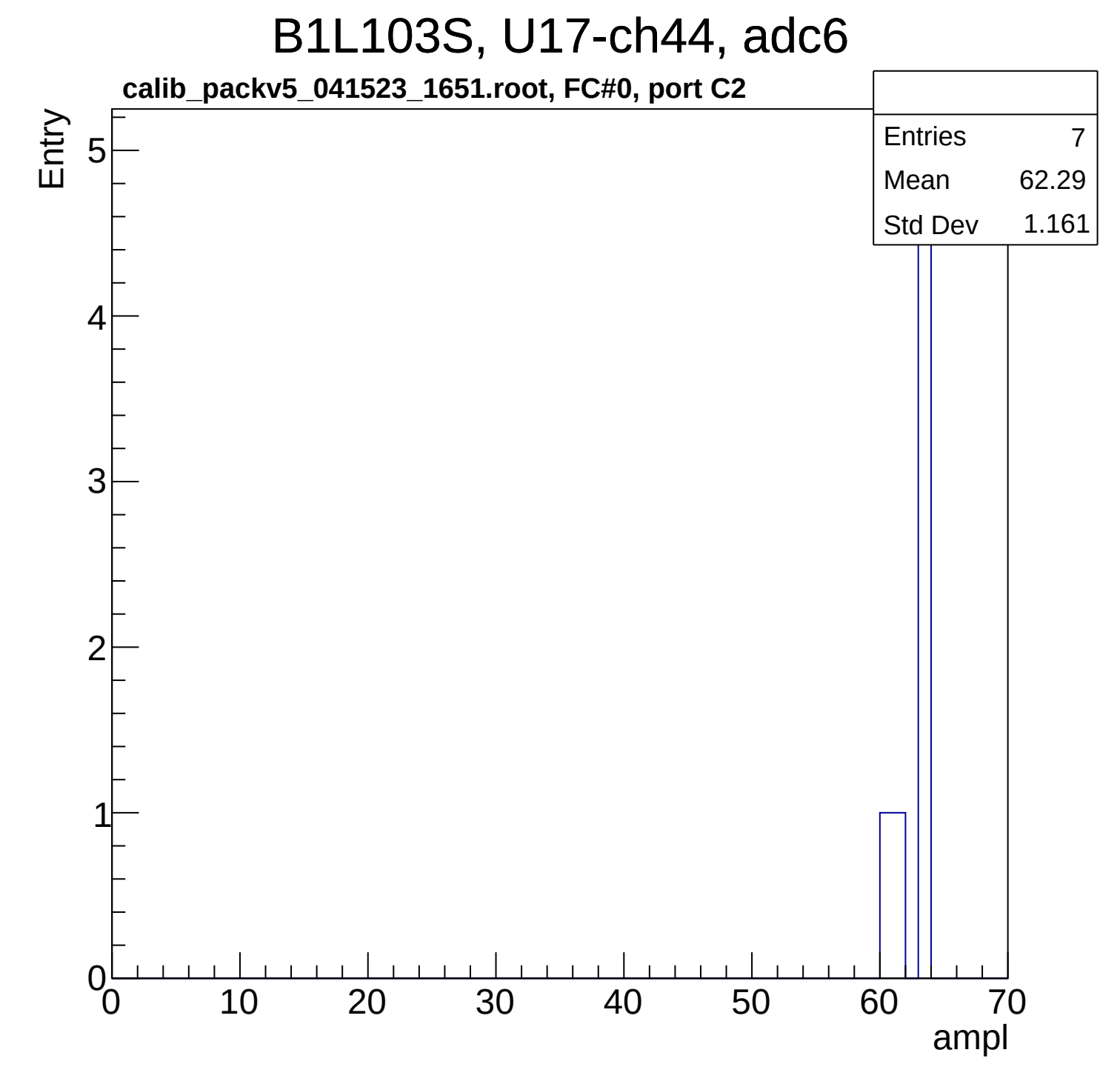
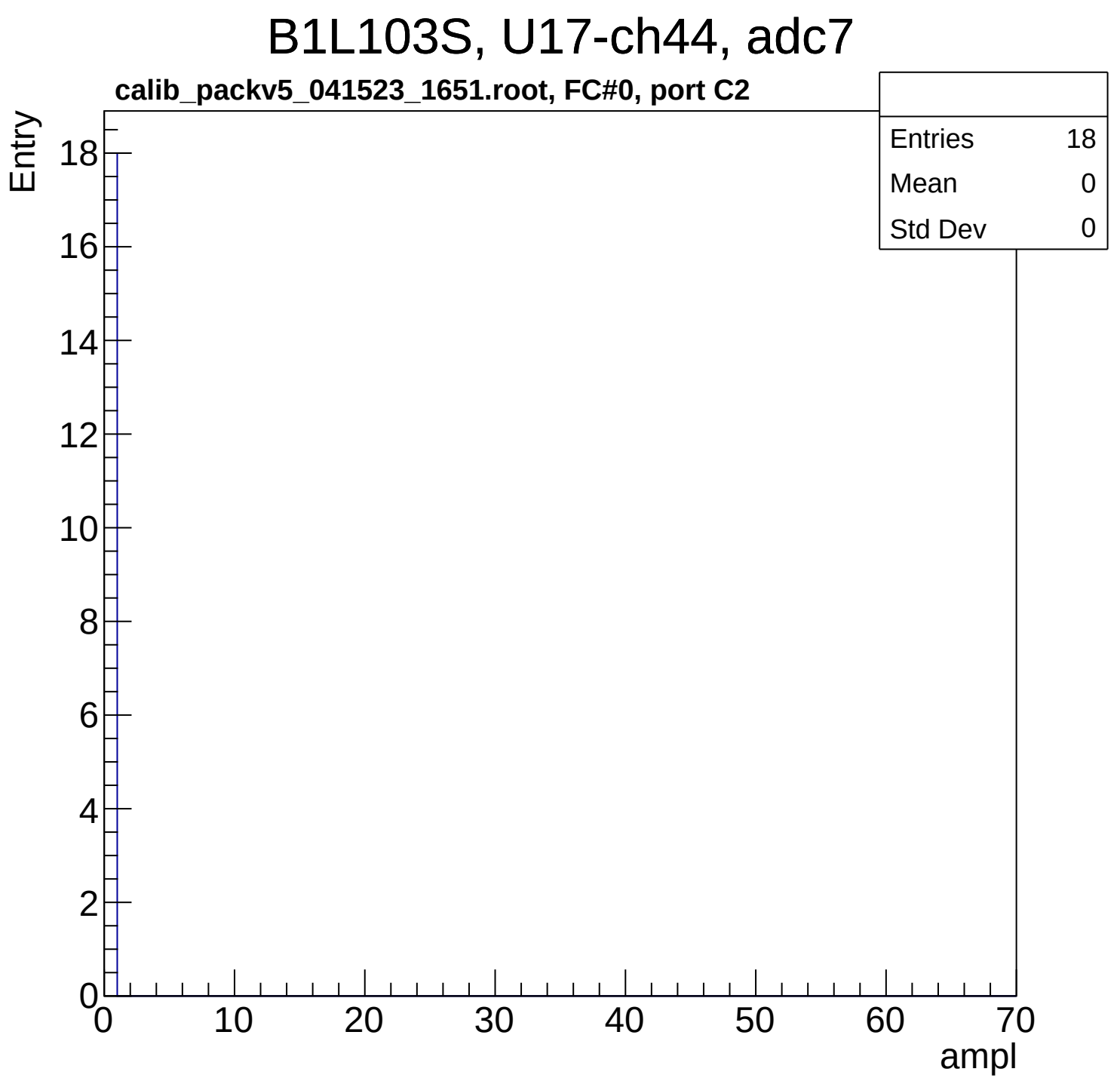
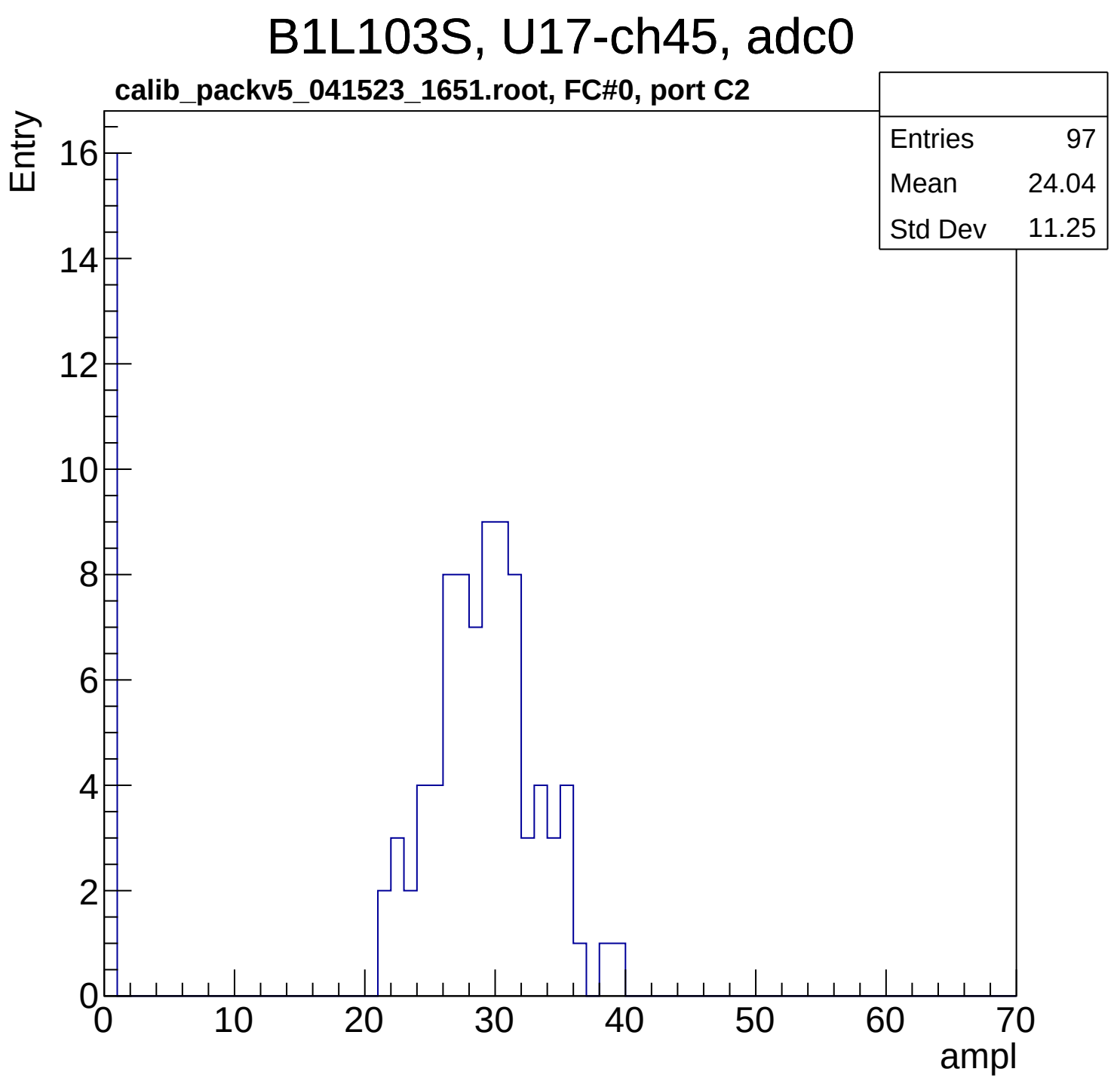

B1L103S, U17-ch44, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 62.29
Std Dev 1.161
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U17-ch44, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch45, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 97
Mean 24.04
Std Dev 11.25
Entry
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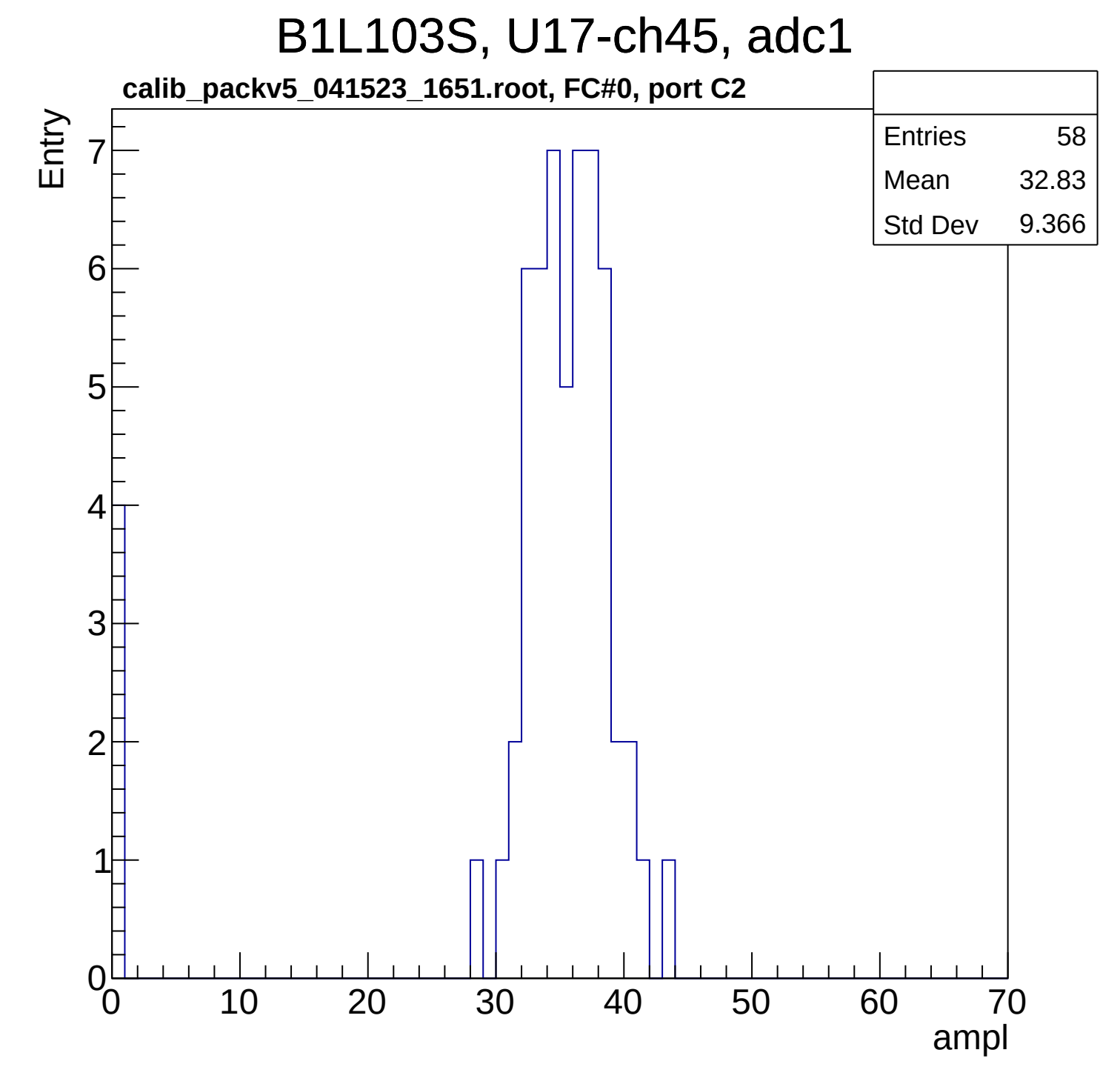
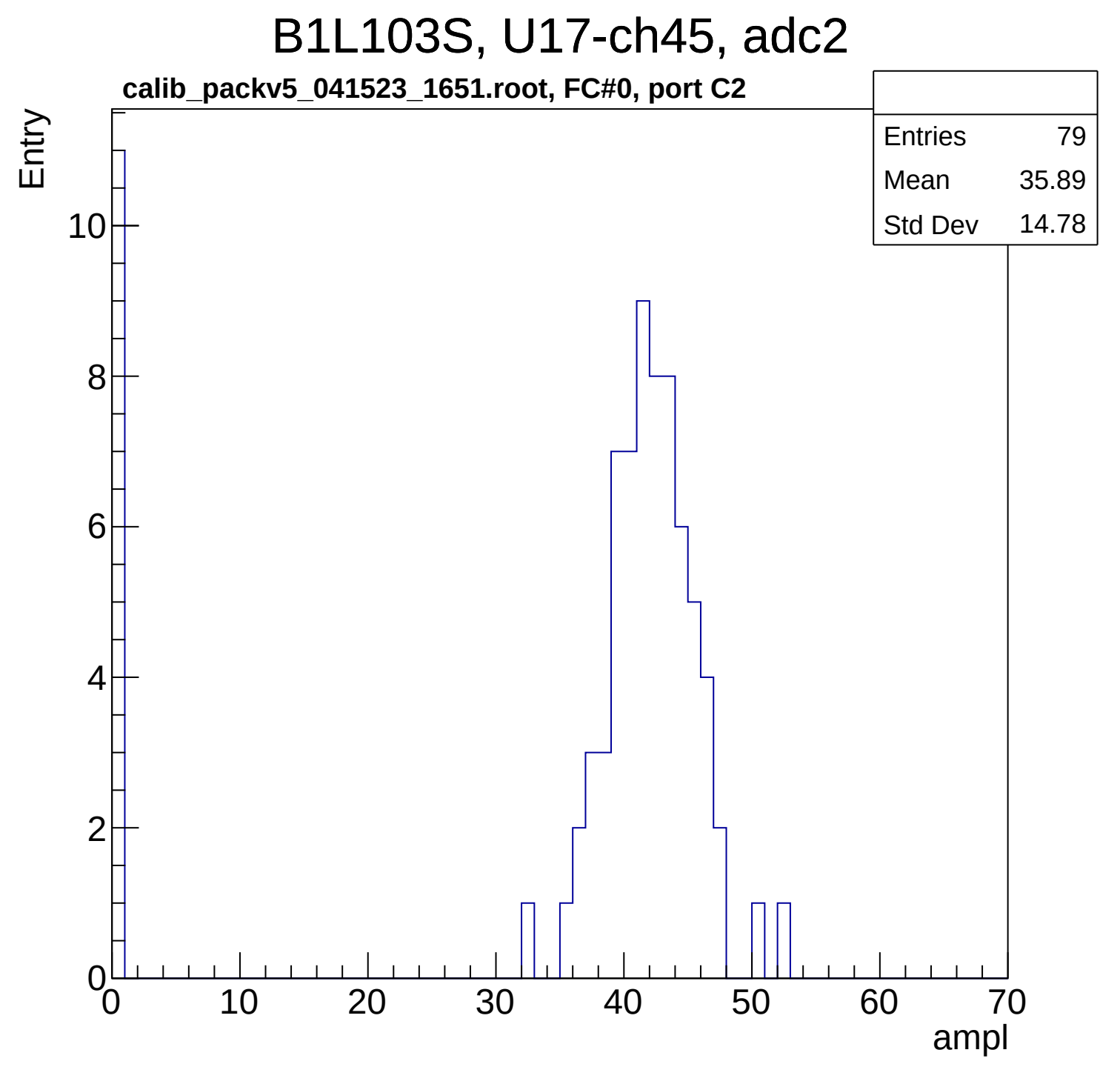
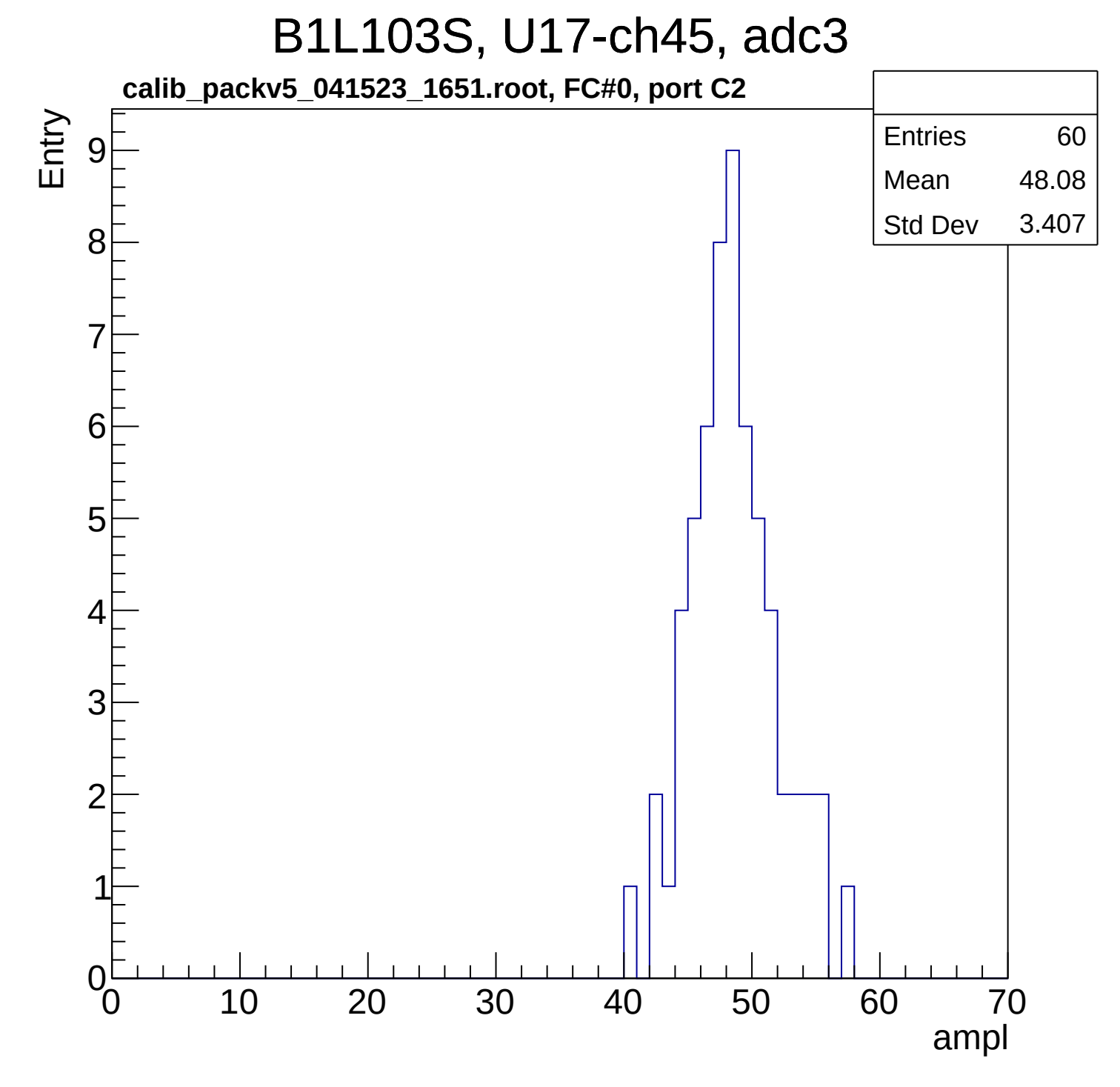
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch45, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 32.83
Std Dev 9.366
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U17-ch45, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 35.89
Std Dev 14.78
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch45, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 48.08
Std Dev 3.407
Entry
ampl
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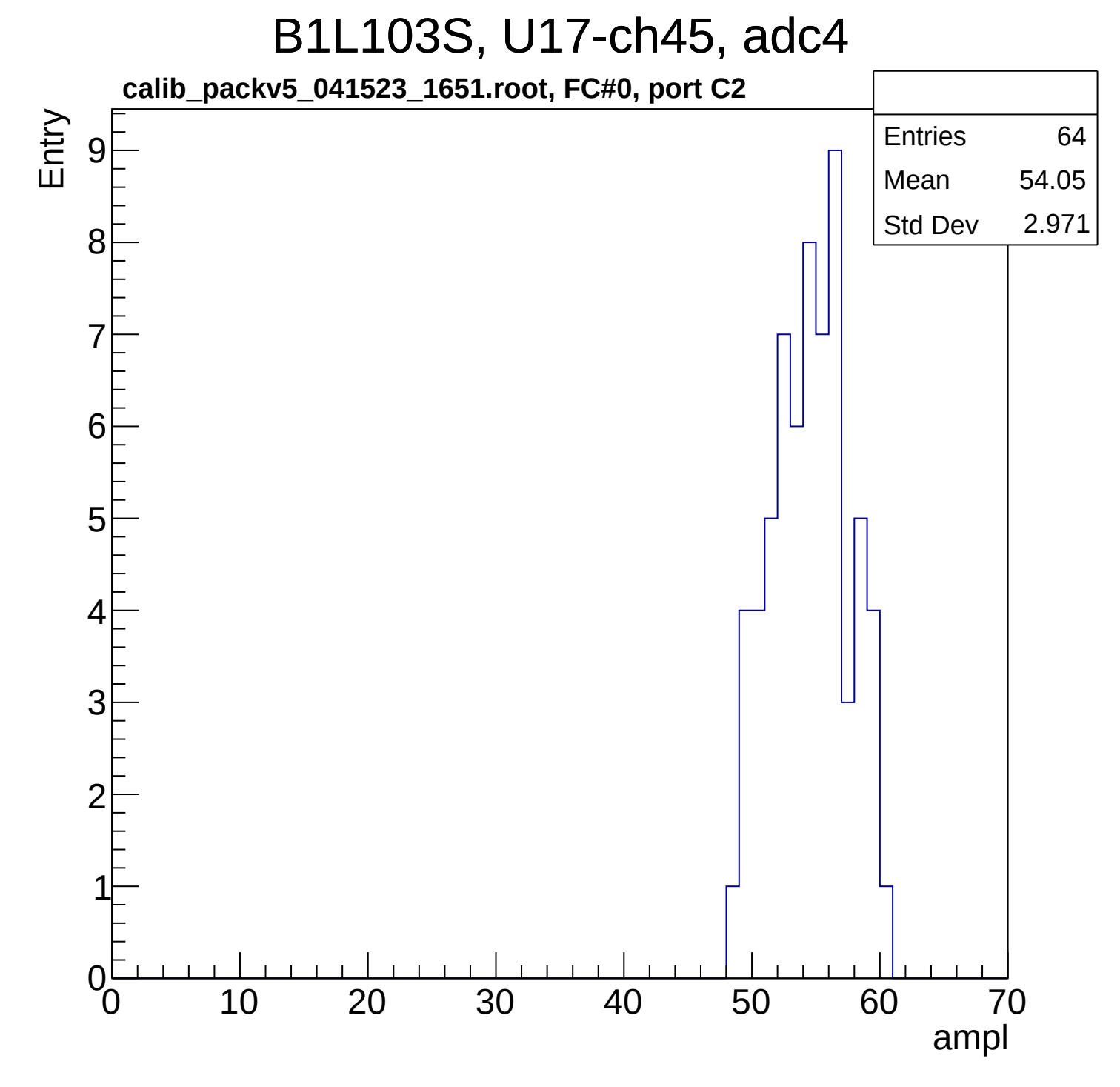
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U17-ch45, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 54.05
Std Dev 2.971
Entry
ampl
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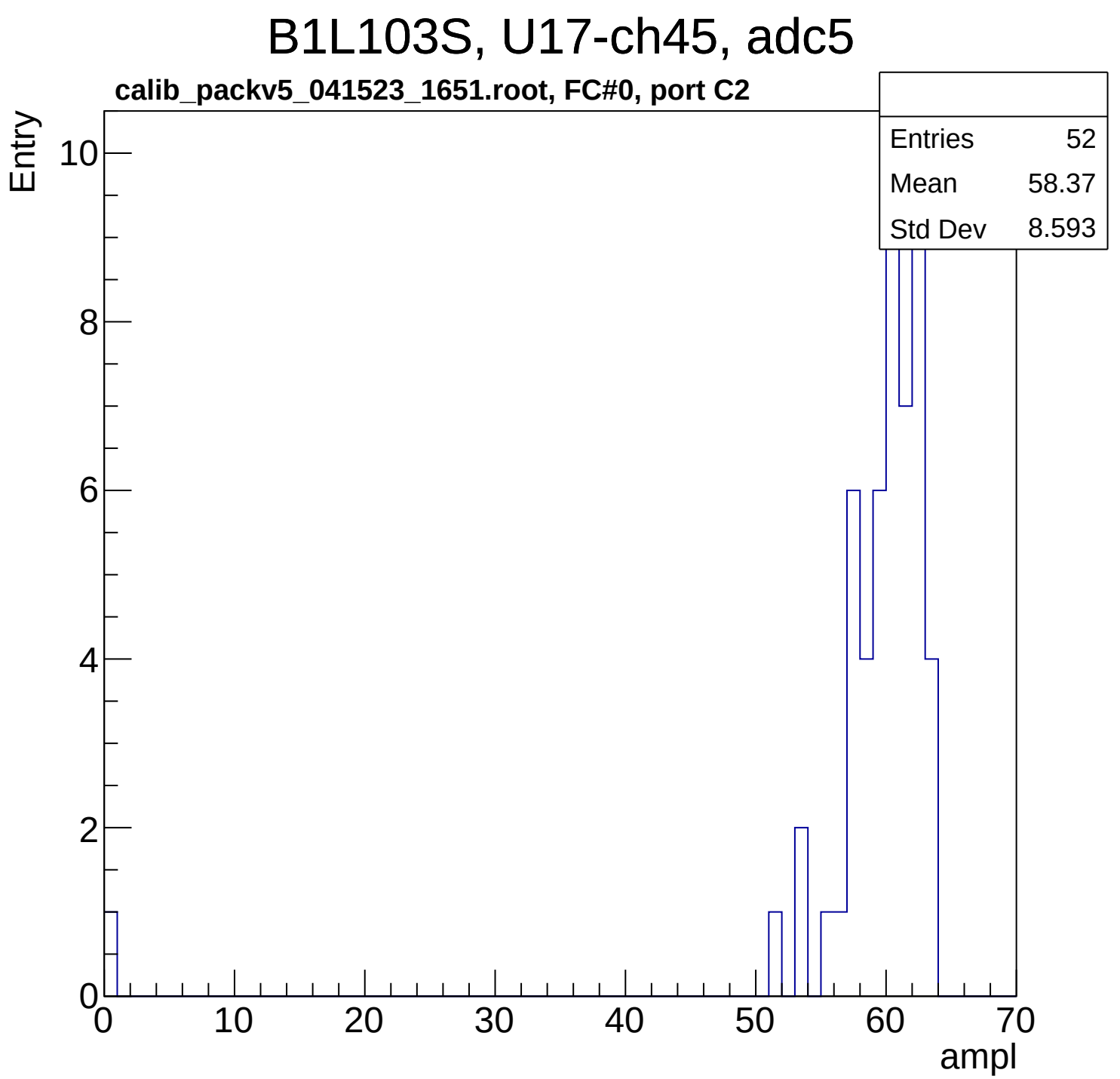
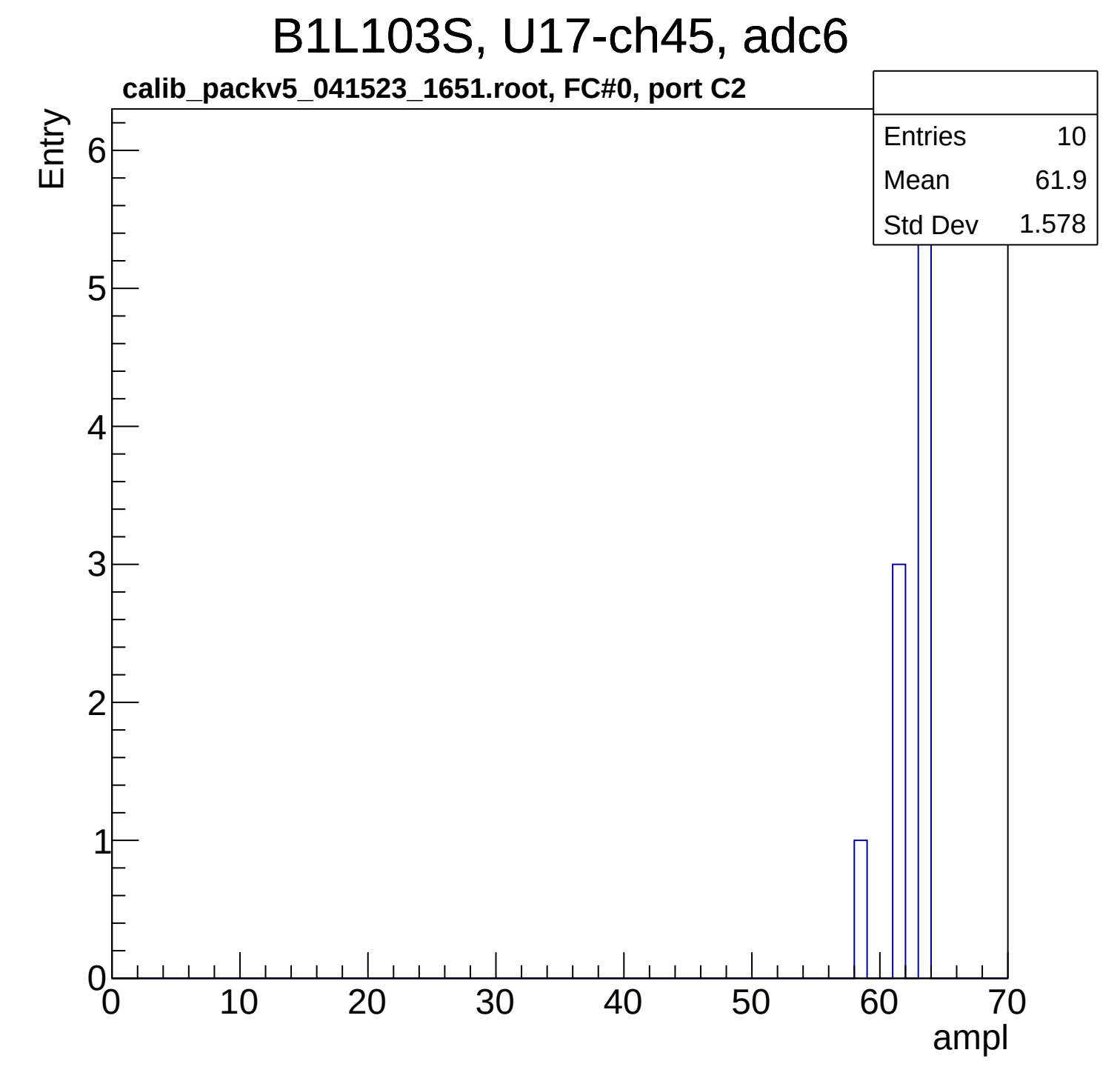
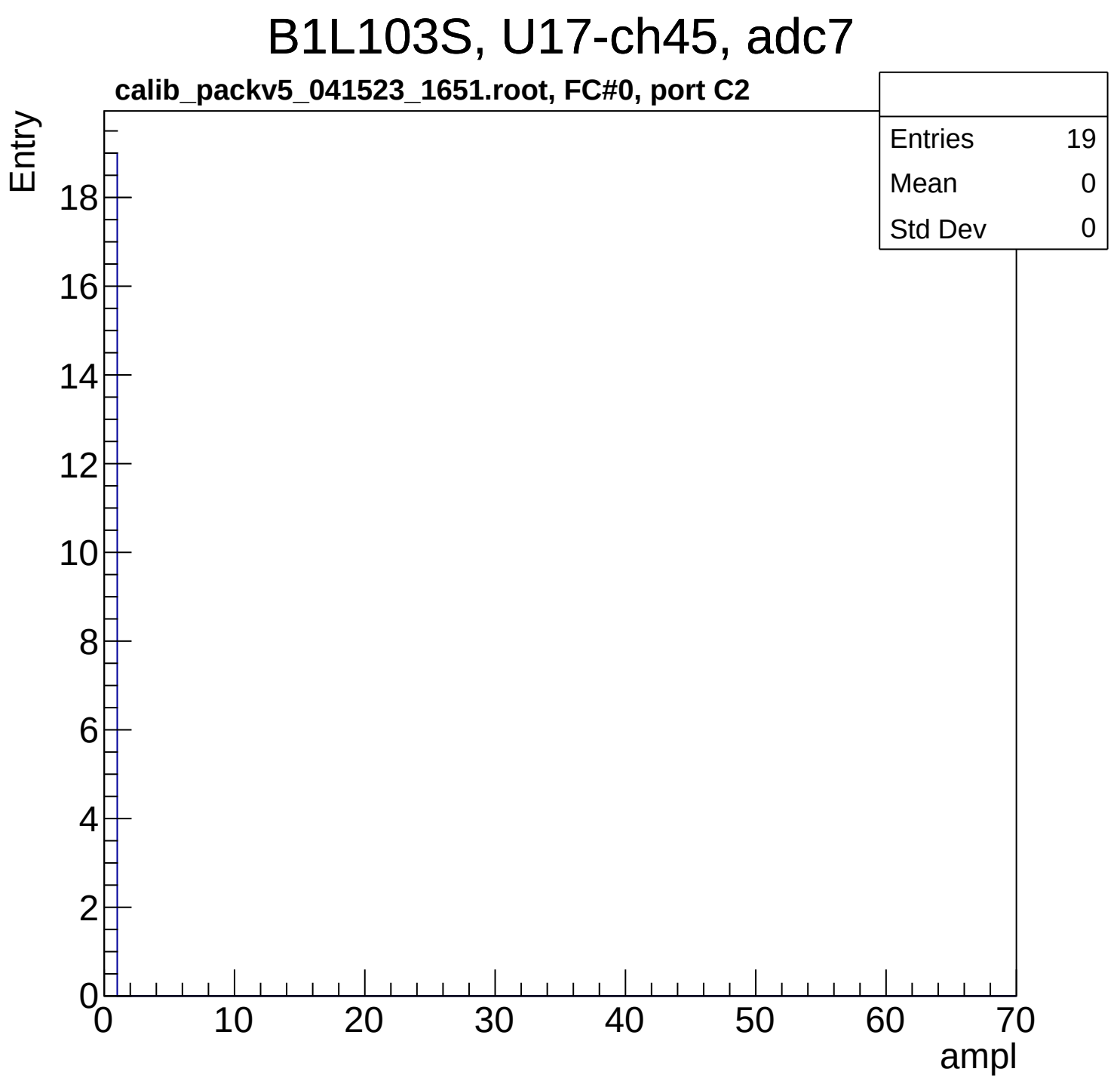
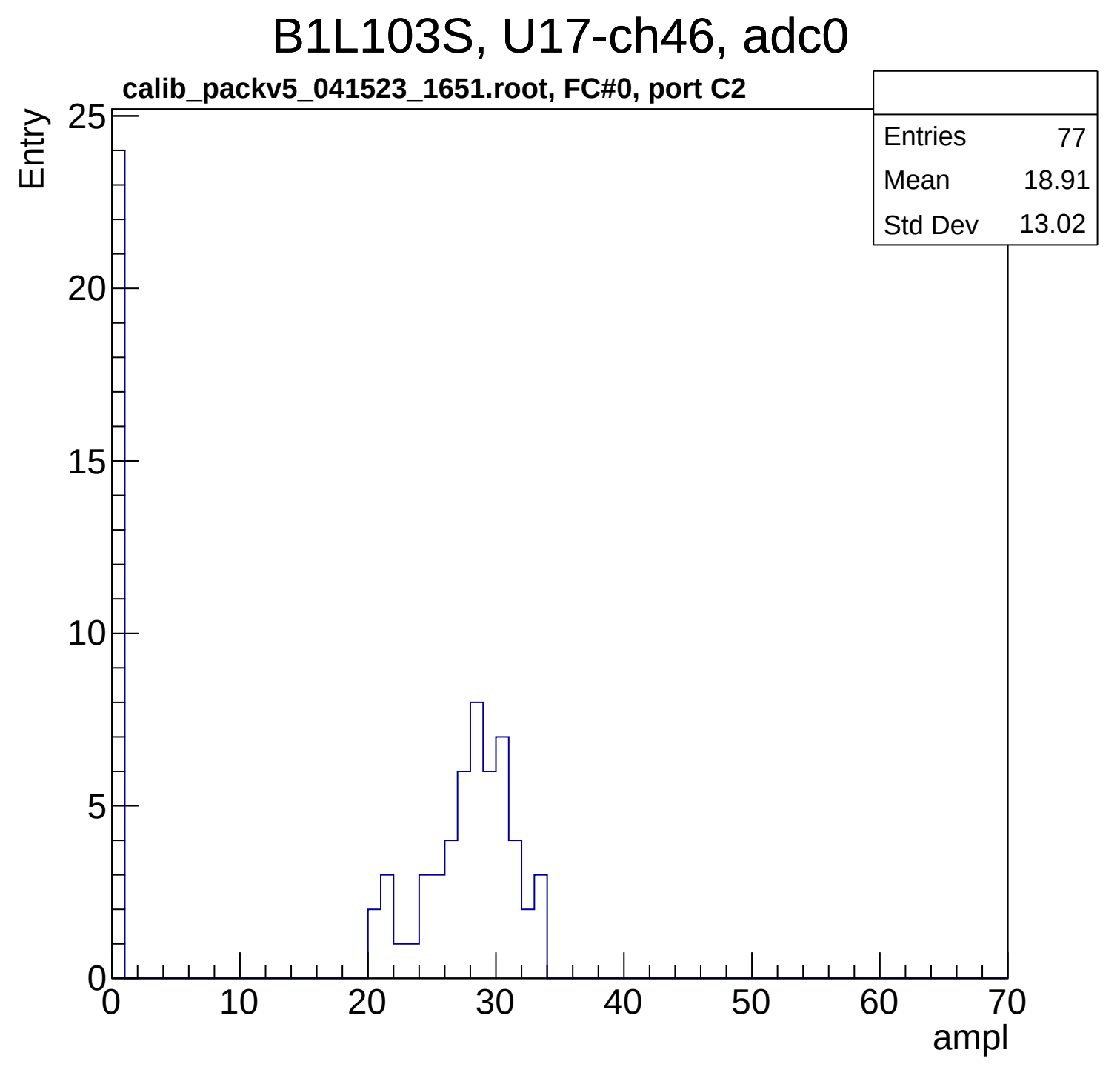
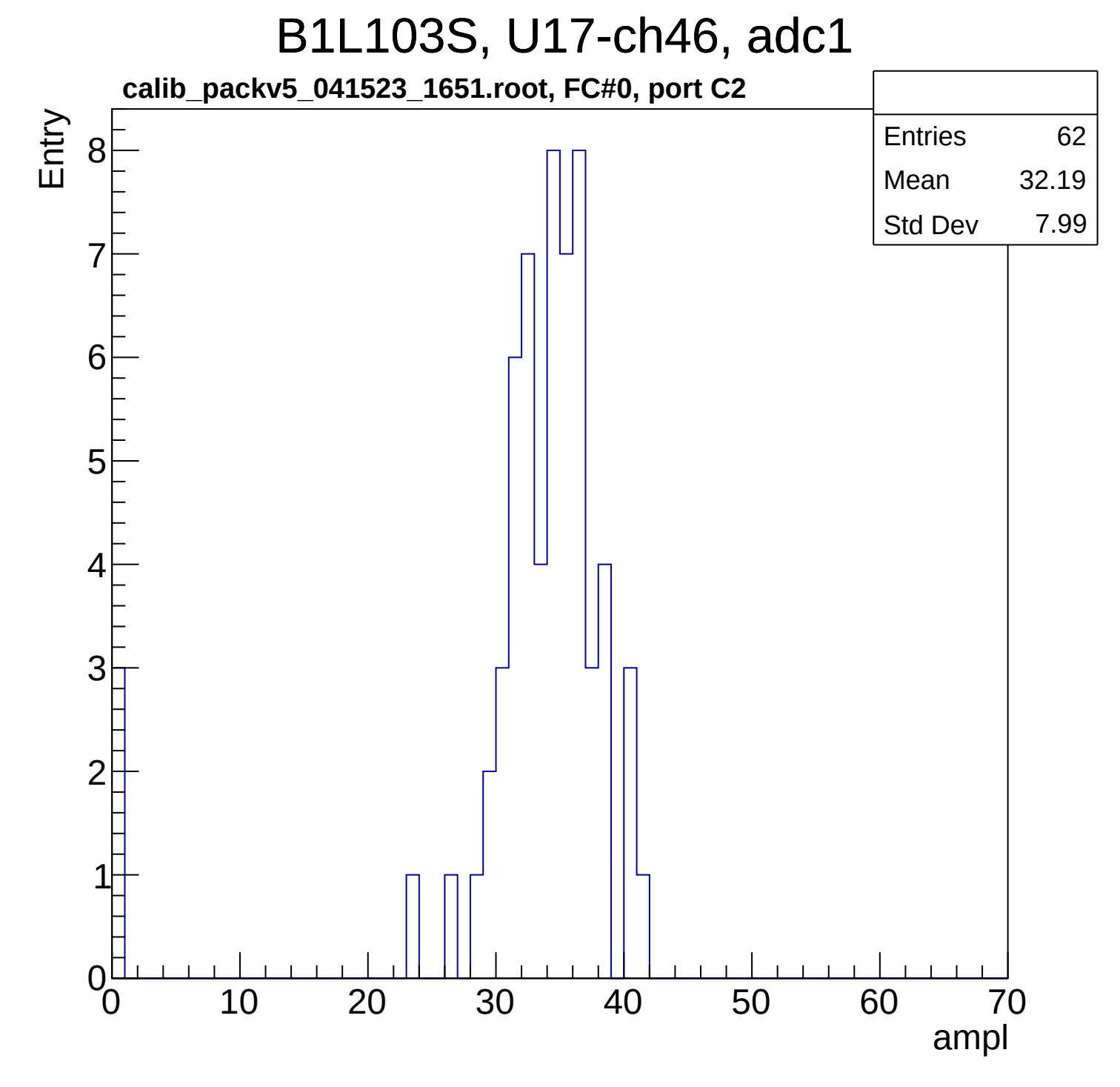
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U17-ch45, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 58.37
Std Dev 8.593
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch45, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 61.9
Std Dev 1.578
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch45, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch46, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 18.91
Std Dev 13.02
Entry
ampl
0
5
10
15
20
25
0
10
20
30
40
50
60
70


B1L103S, U17-ch46, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 32.19
Std Dev 7.99
Entry
ampl
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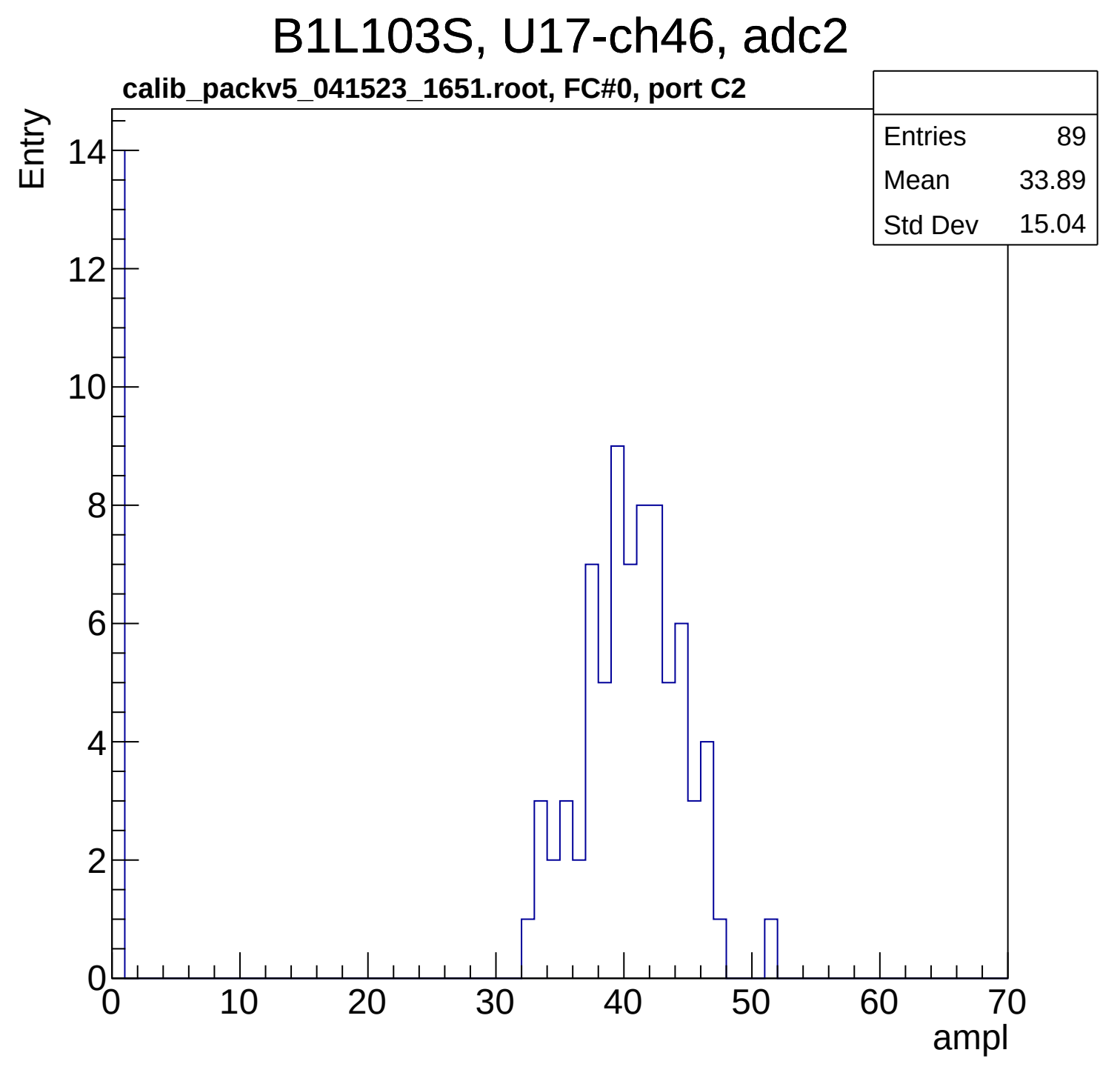
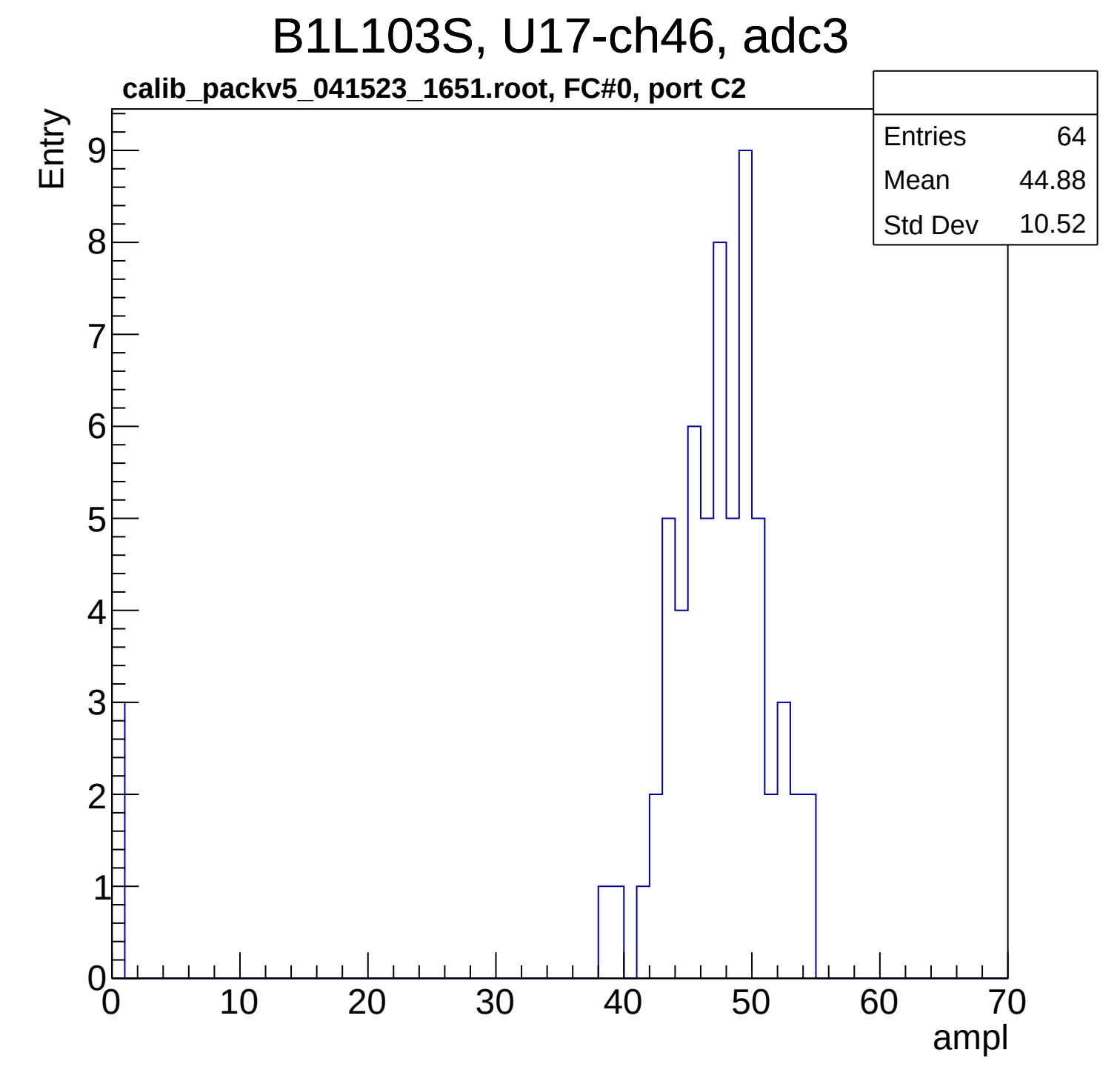
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U17-ch46, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 89
Mean 33.89
Std Dev 15.04
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L103S, U17-ch46, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 44.88
Std Dev 10.52
Entry
ampl
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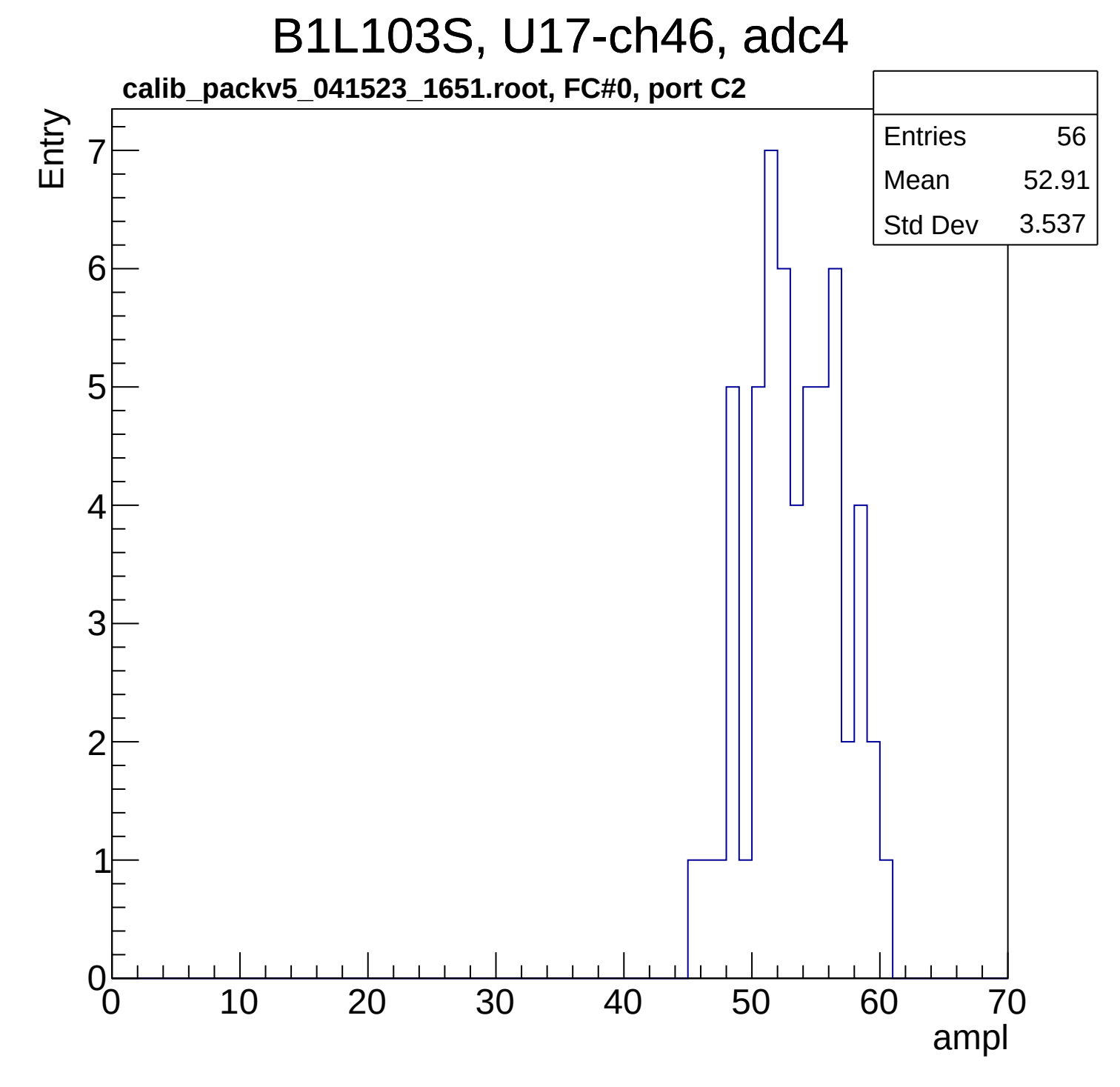
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U17-ch46, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 52.91
Std Dev 3.537
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
30
40
50
60
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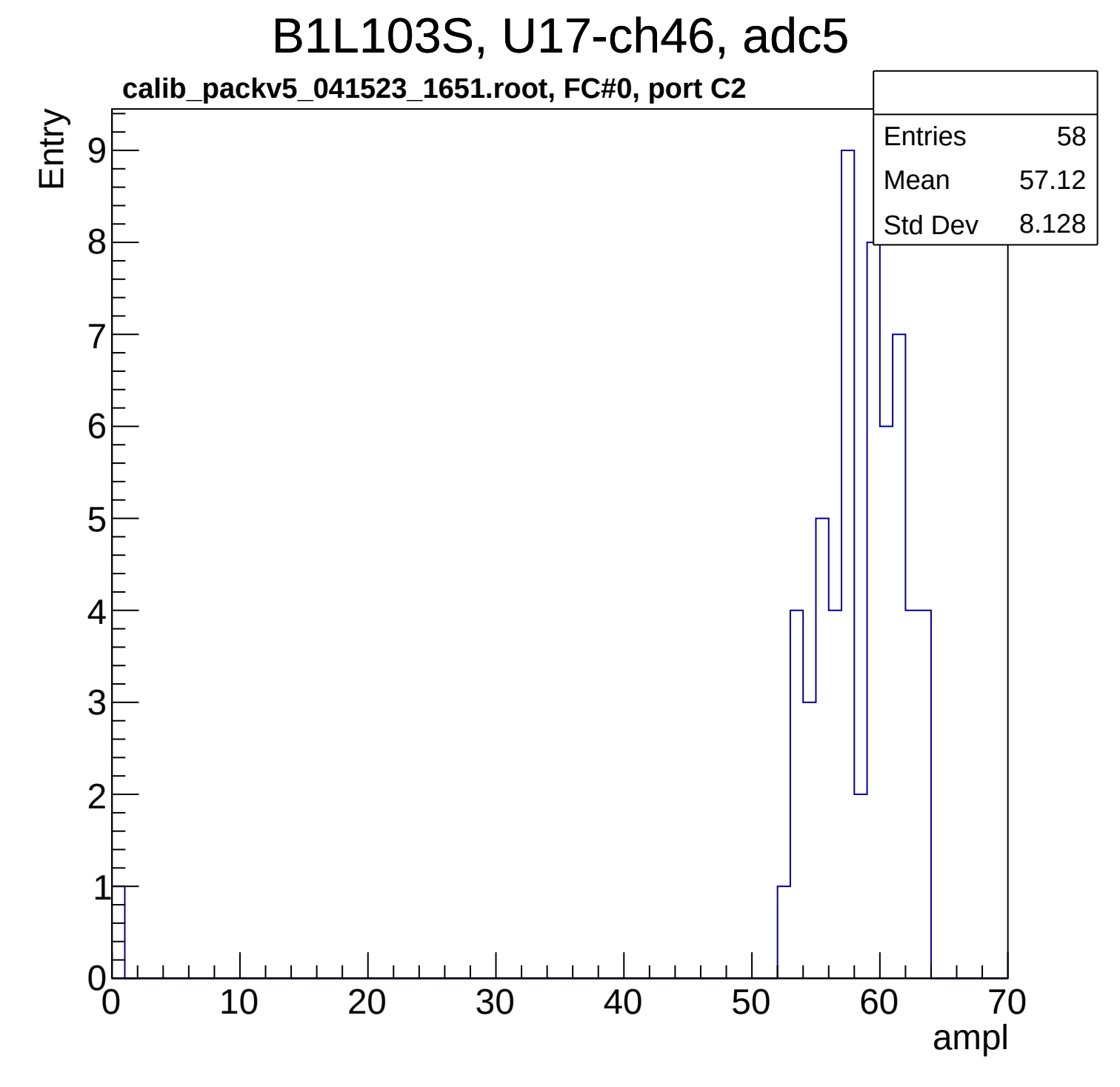
B1L103S, U17-ch46, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 57.12
Std Dev 8.128
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
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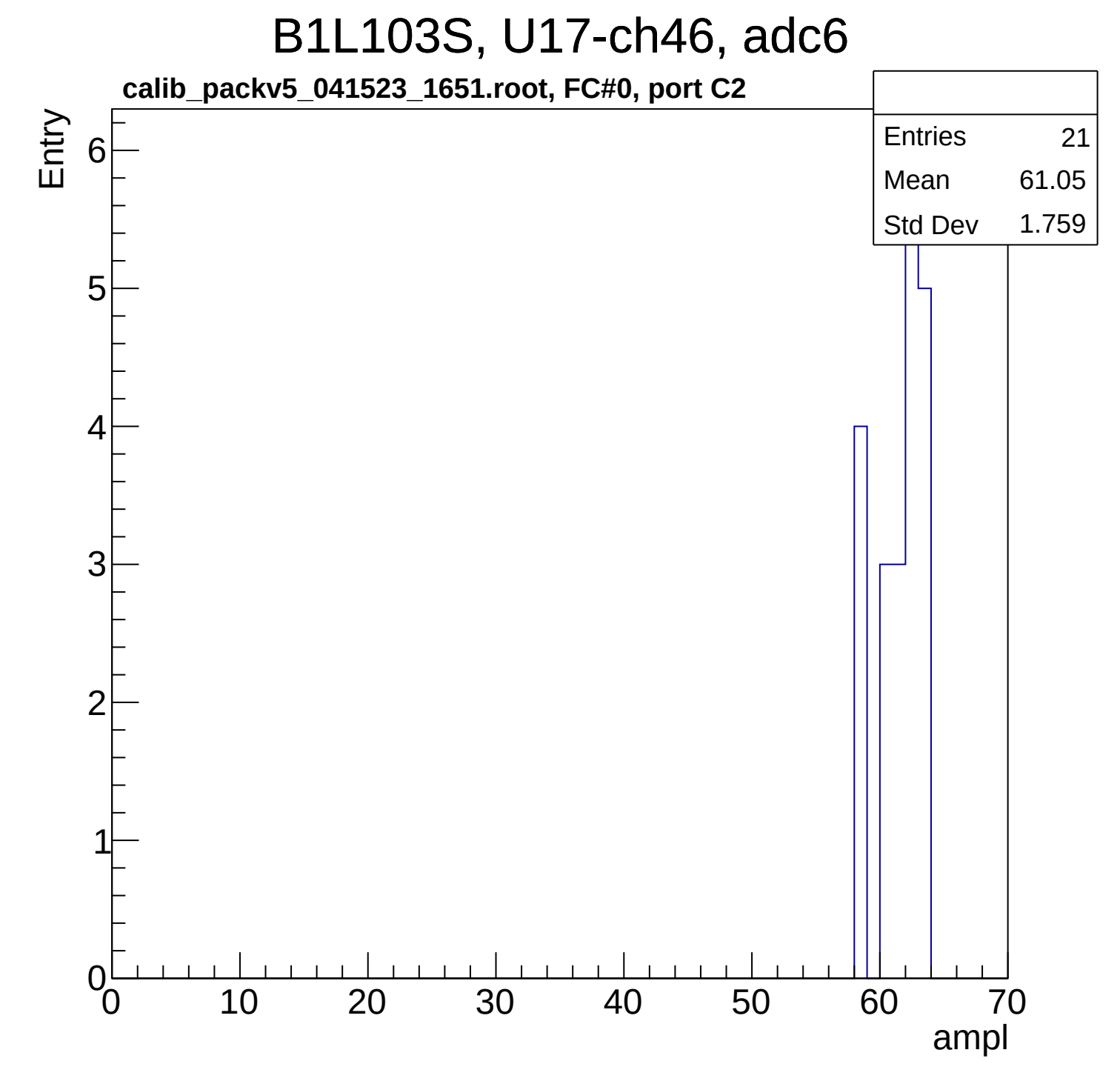
60
70


B1L103S, U17-ch46, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 61.05
Std Dev 1.759
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
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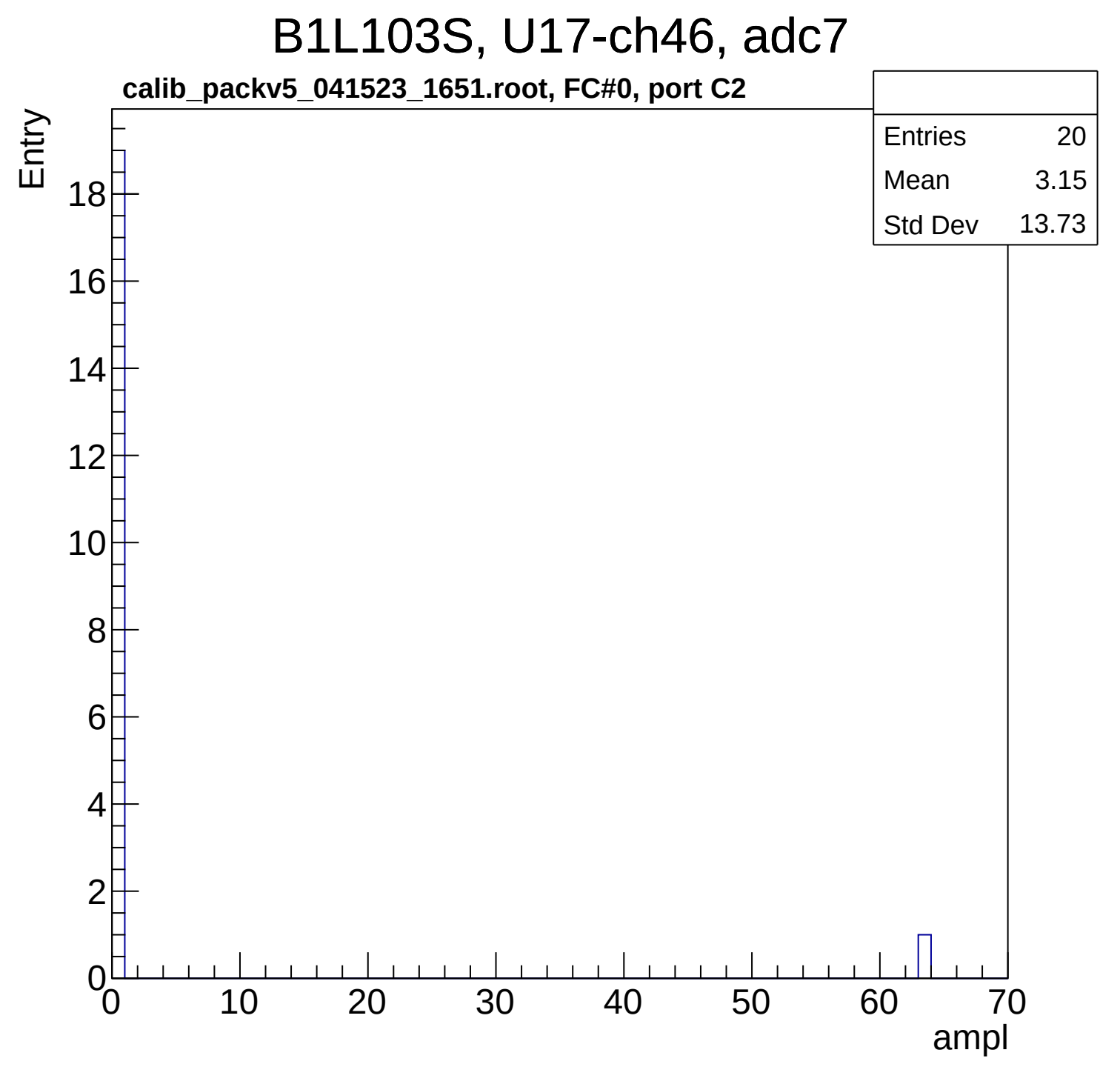
B1L103S, U17-ch46, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
0
2
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6
8
10
12
14
16
18
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10
20
30
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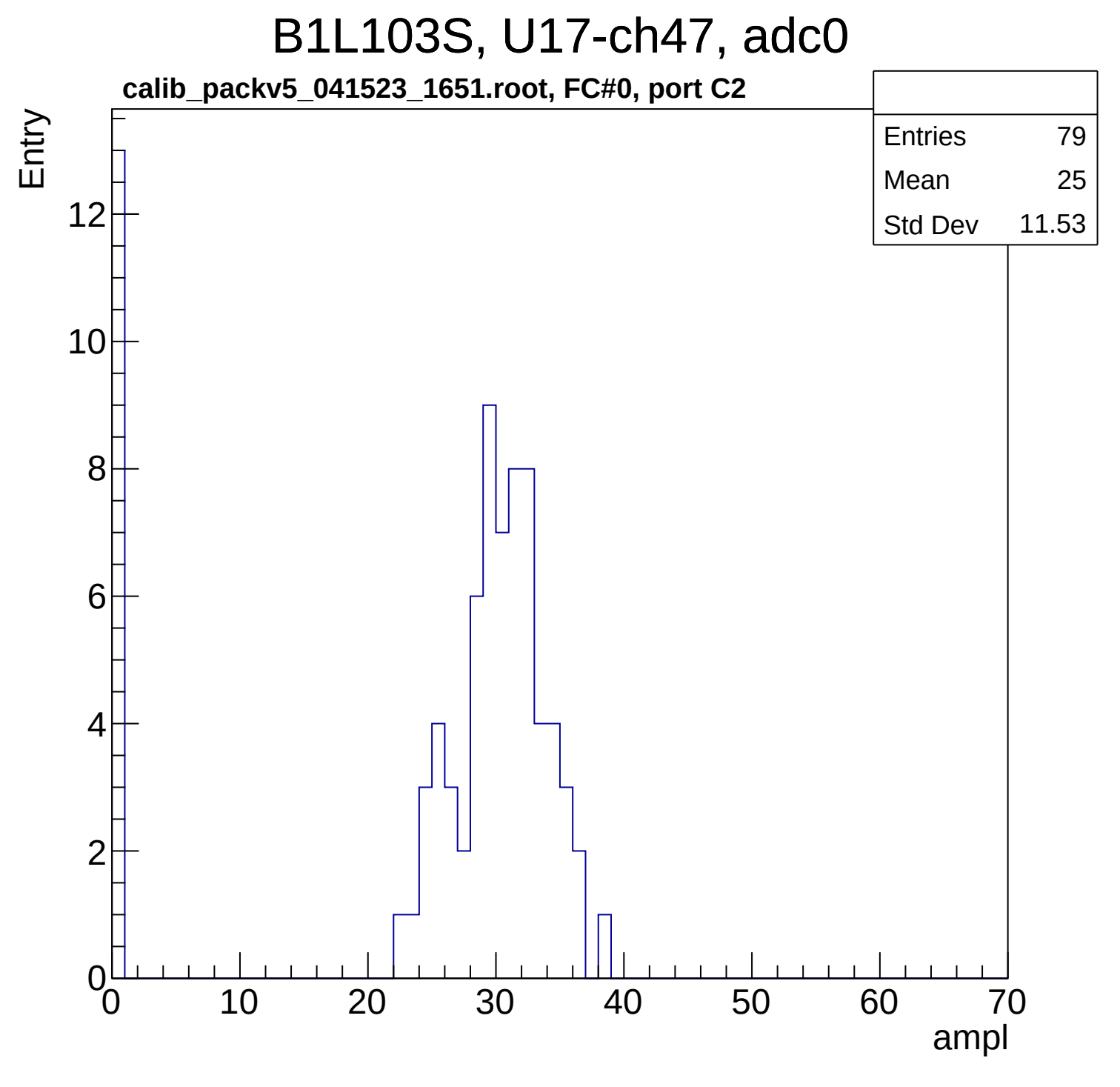
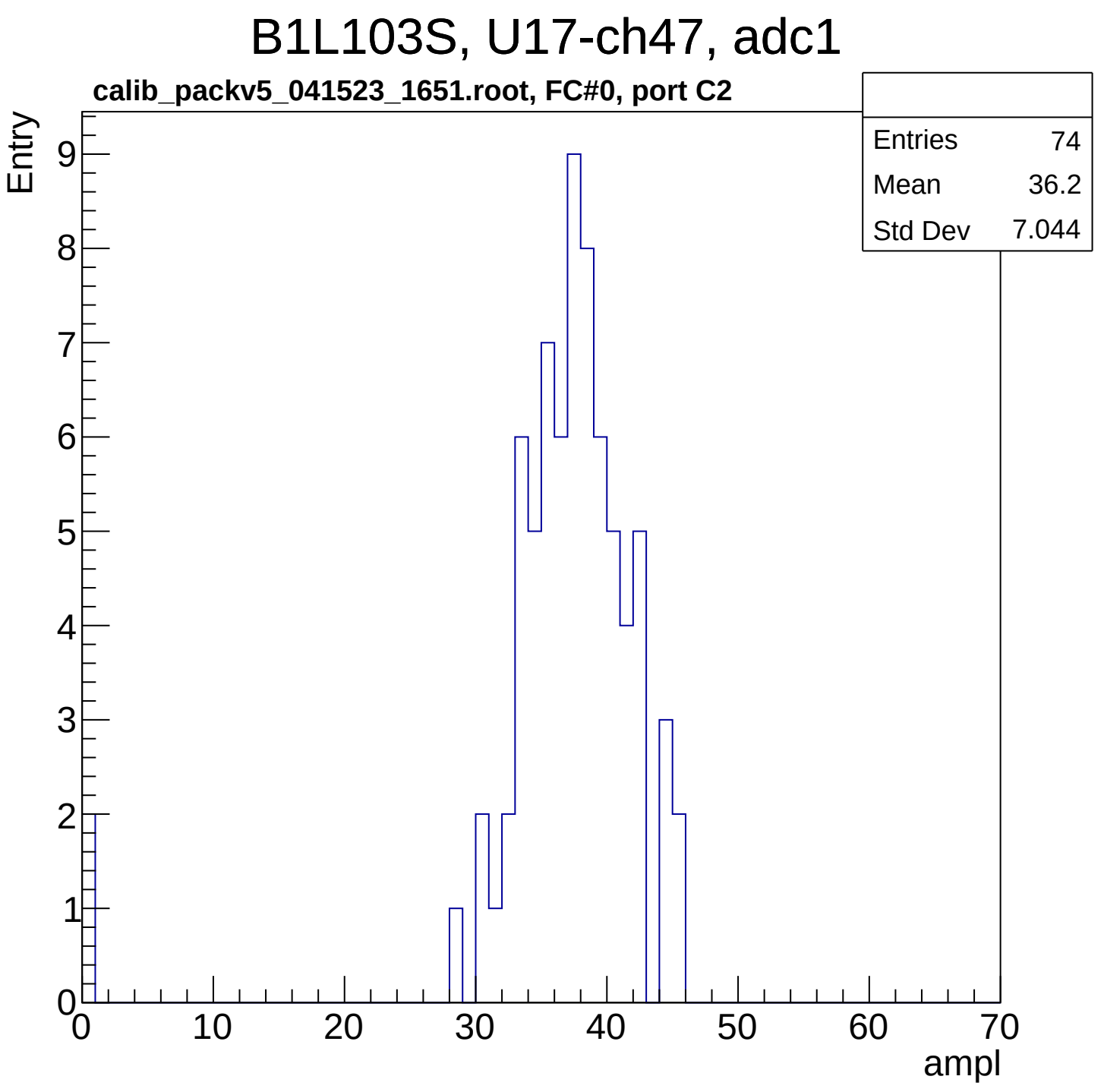
50
60
70
ampl


B1L103S, U17-ch47, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 25
Std Dev 11.53
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch47, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 36.2
Std Dev 7.044
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
50
60
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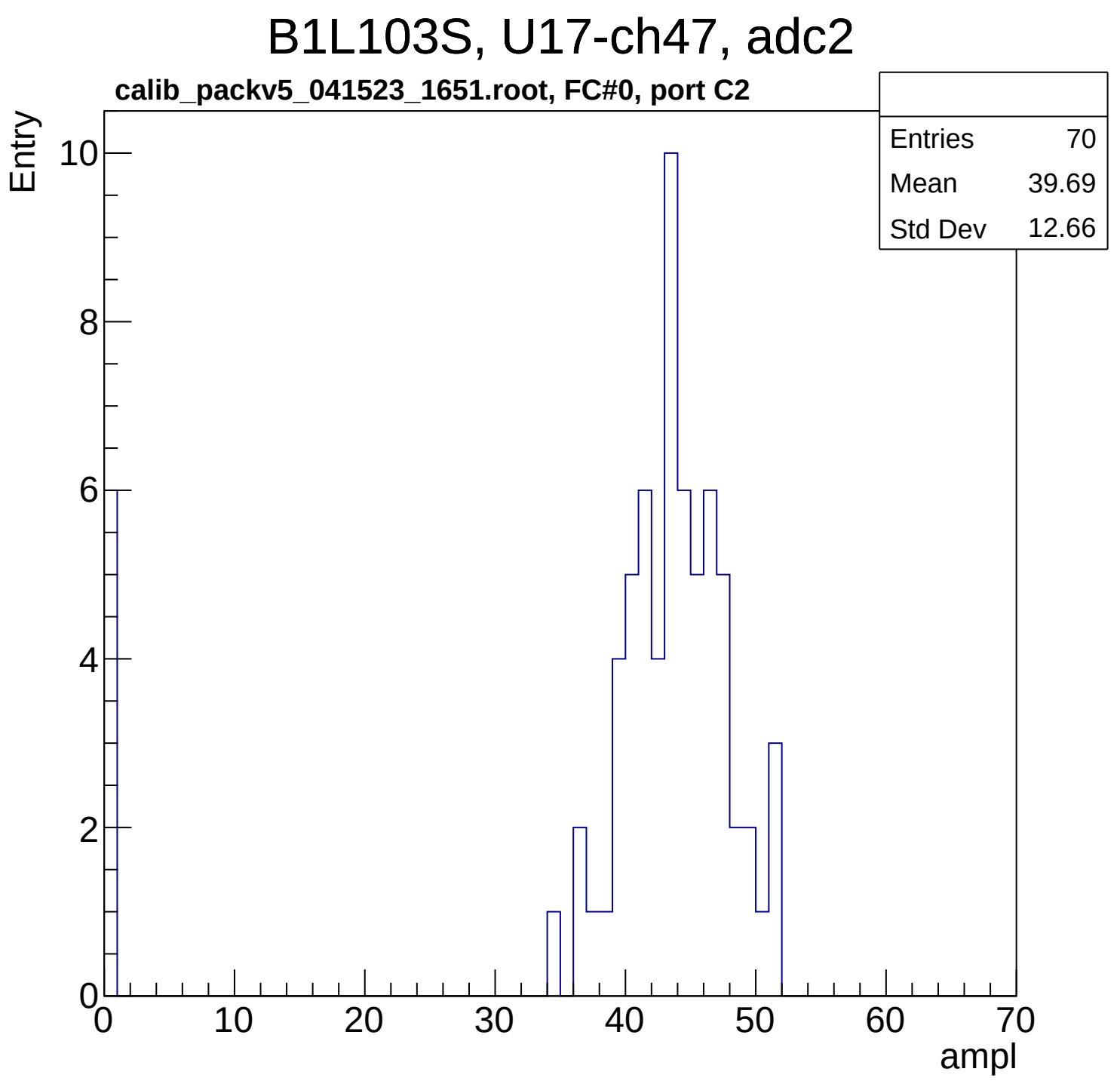
B1L103S, U17-ch47, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 39.69
Std Dev 12.66
Entry
0
2
4
6
8
10
0
10
20
30
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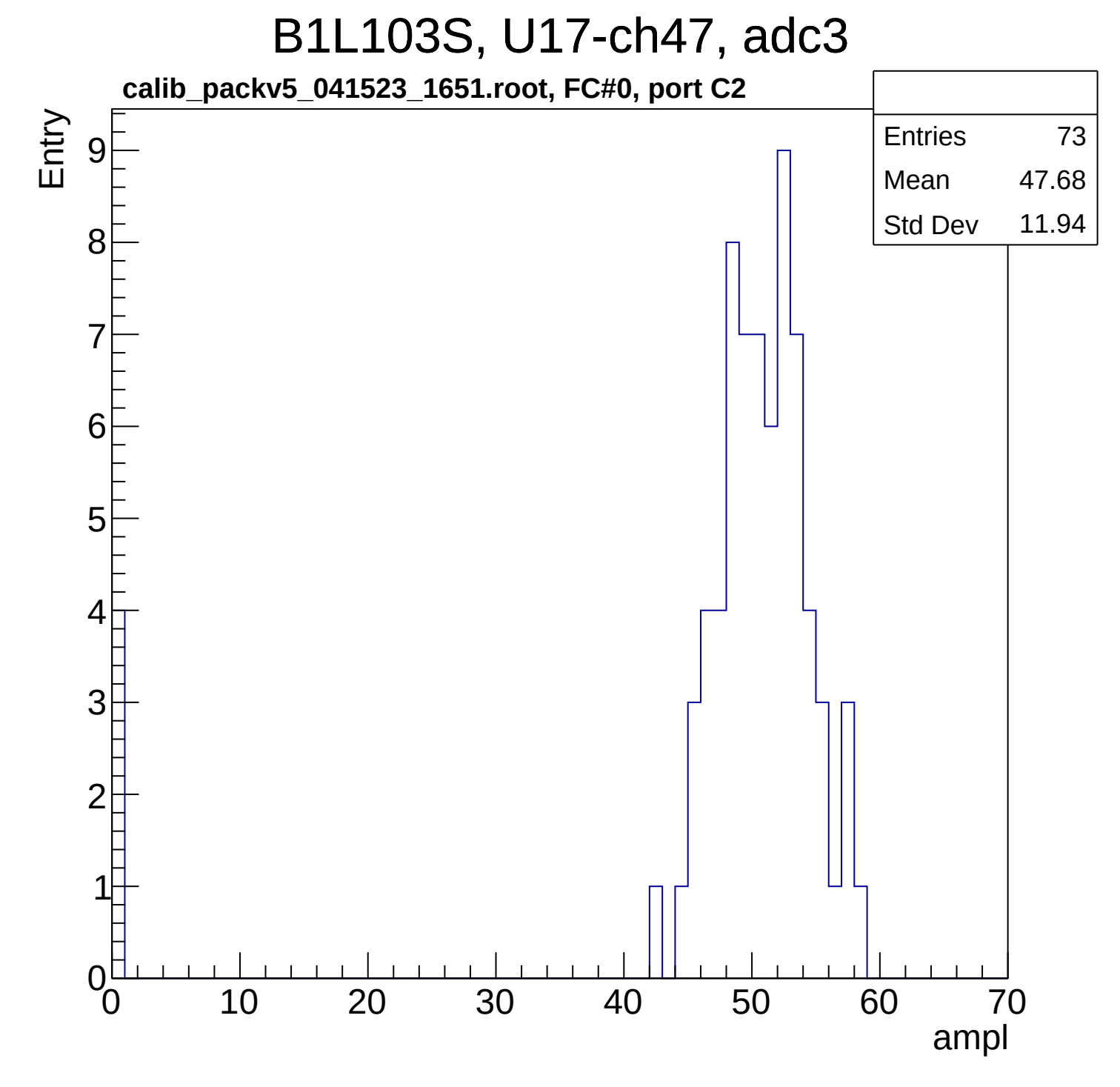
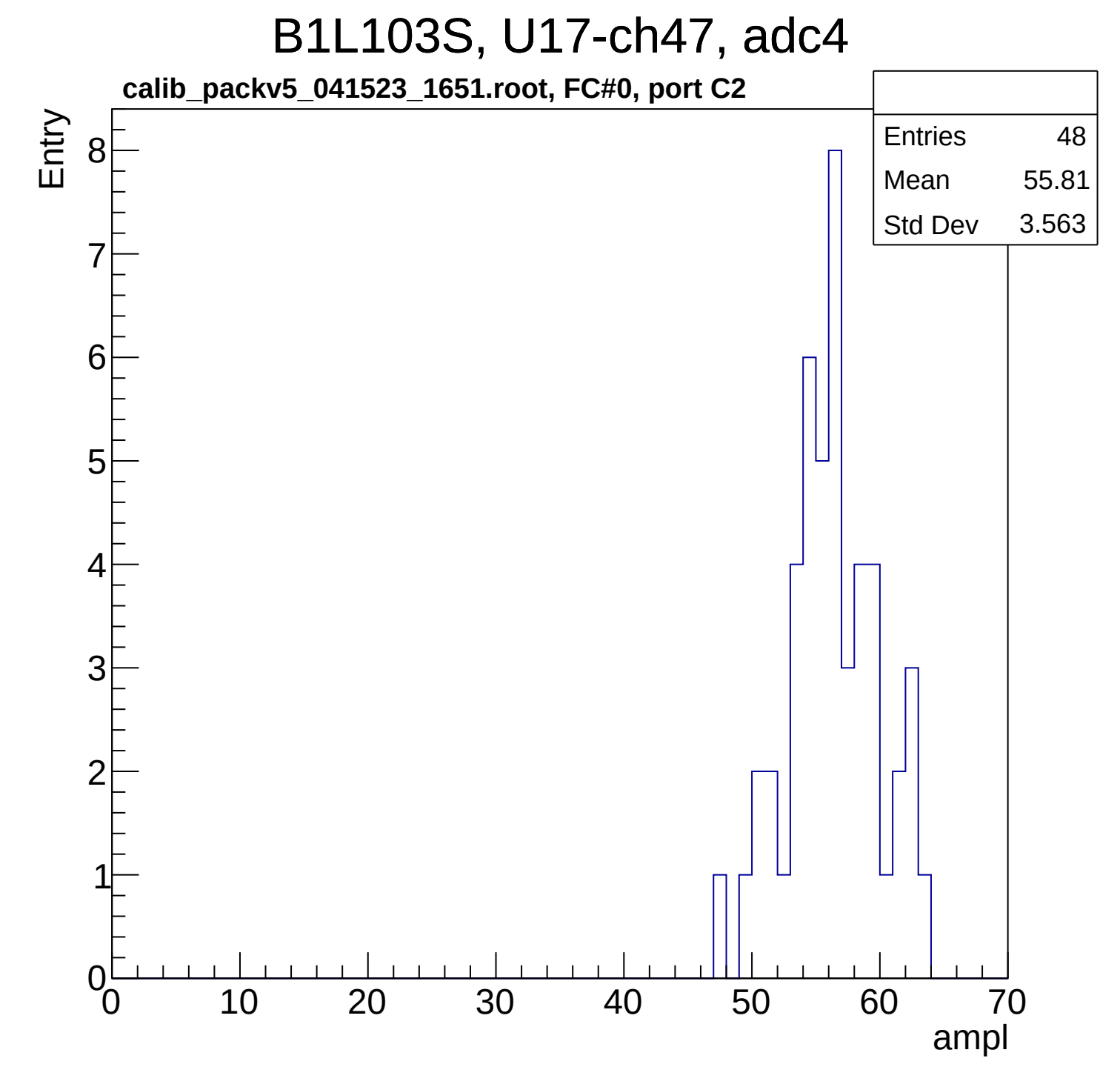
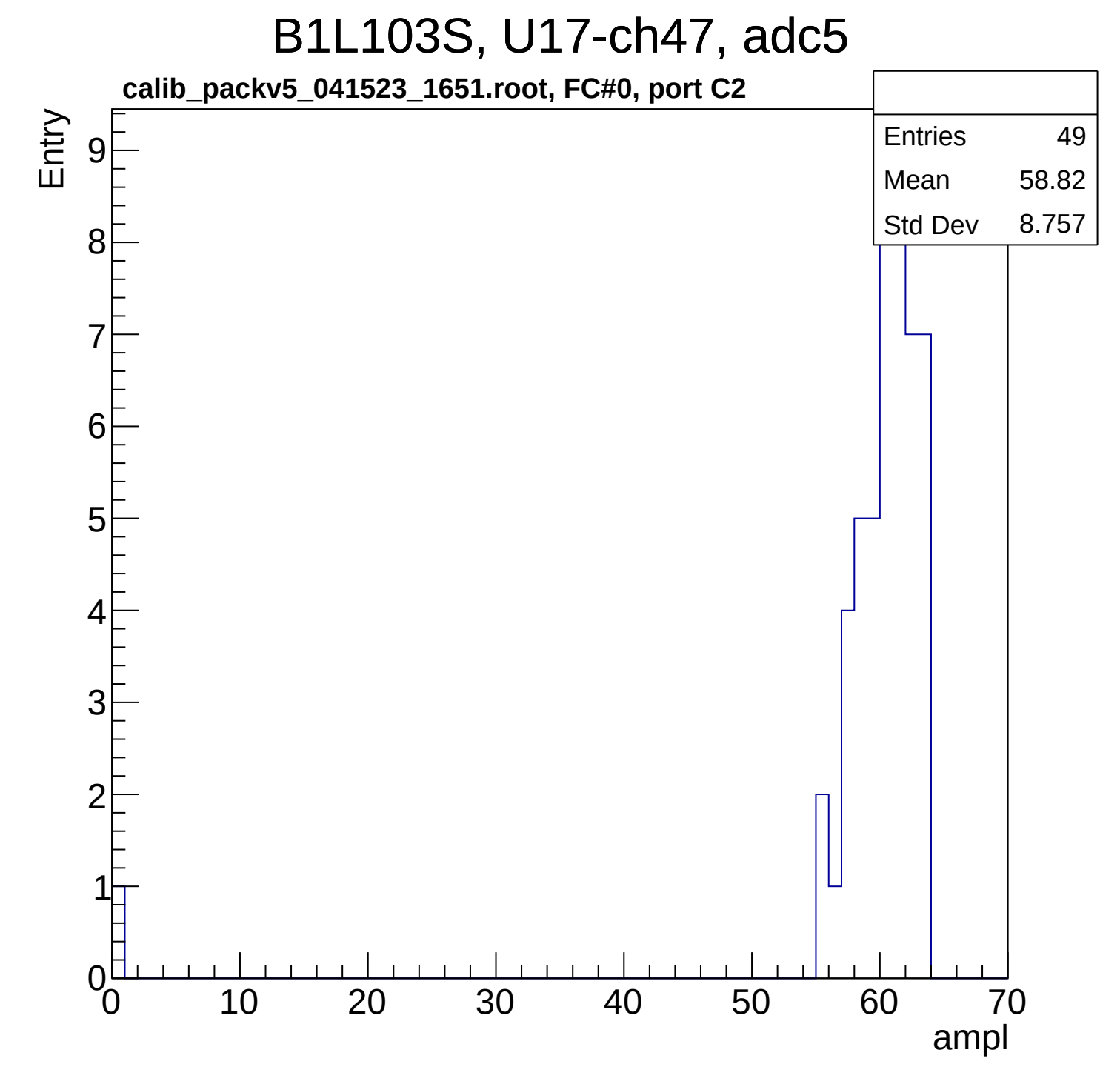
50
60
70
ampl


B1L103S, U17-ch47, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 47.68
Std Dev 11.94
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U17-ch47, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 55.81
Std Dev 3.563
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U17-ch47, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 58.82
Std Dev 8.757
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
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40
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60
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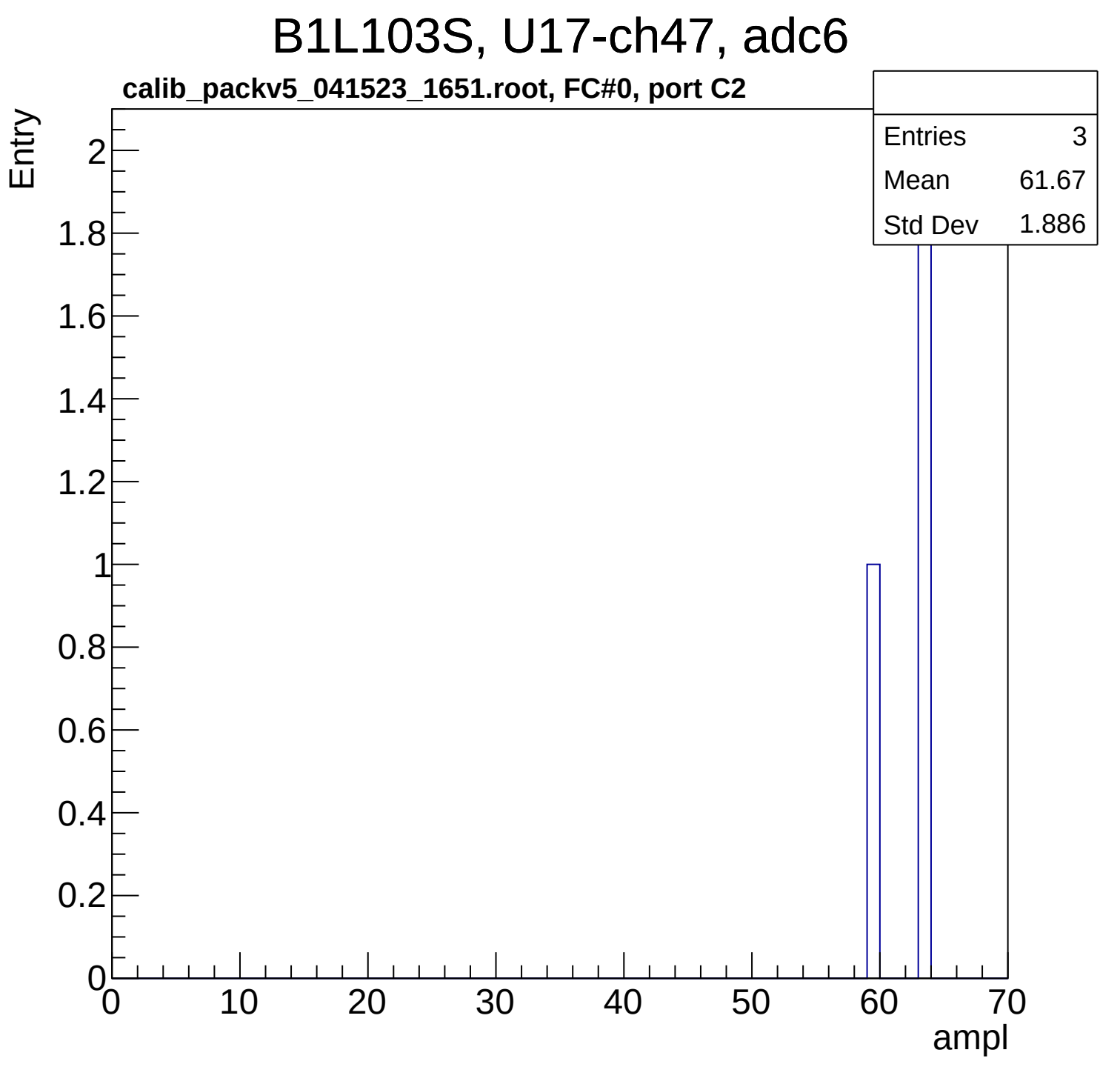
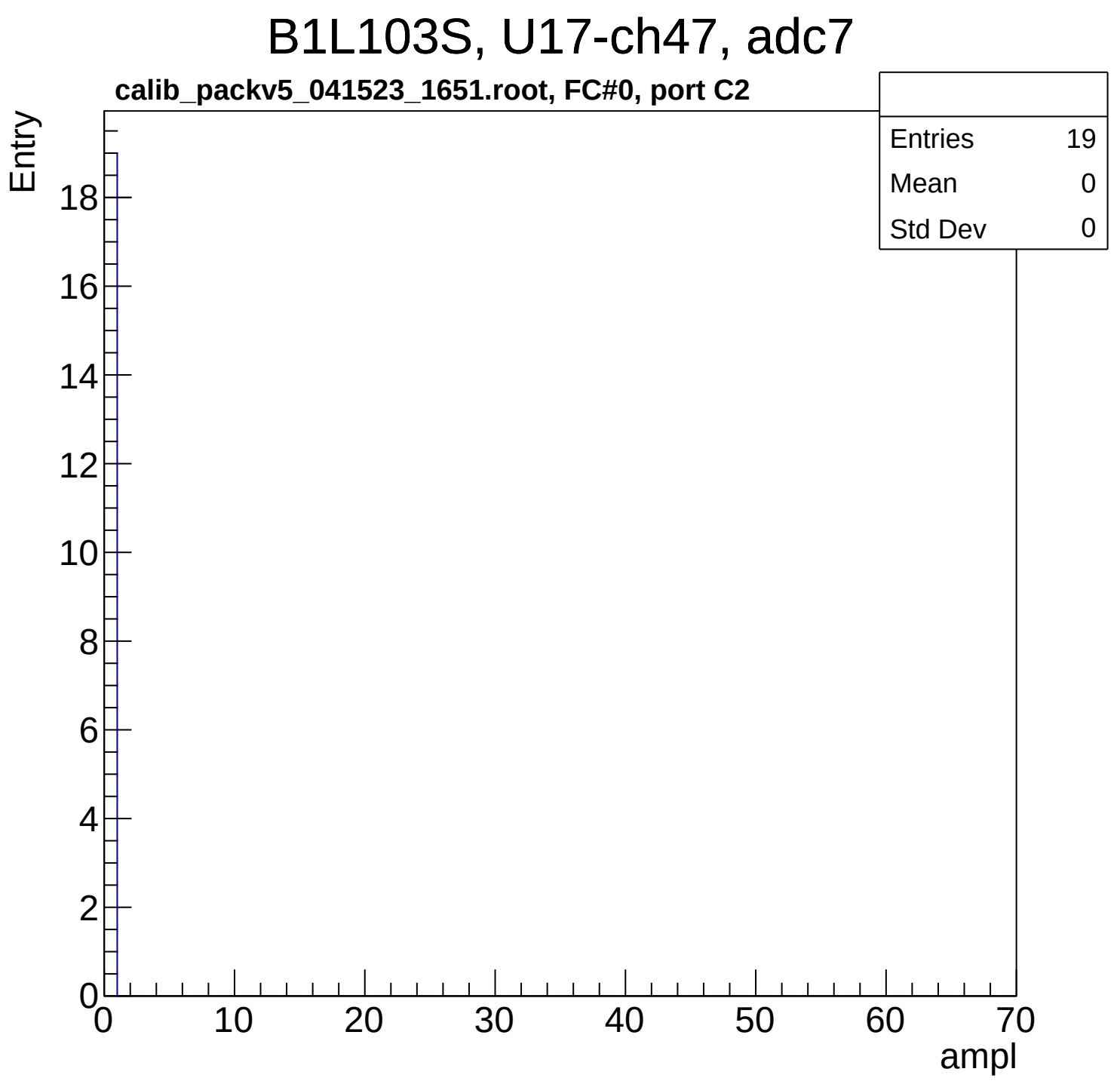
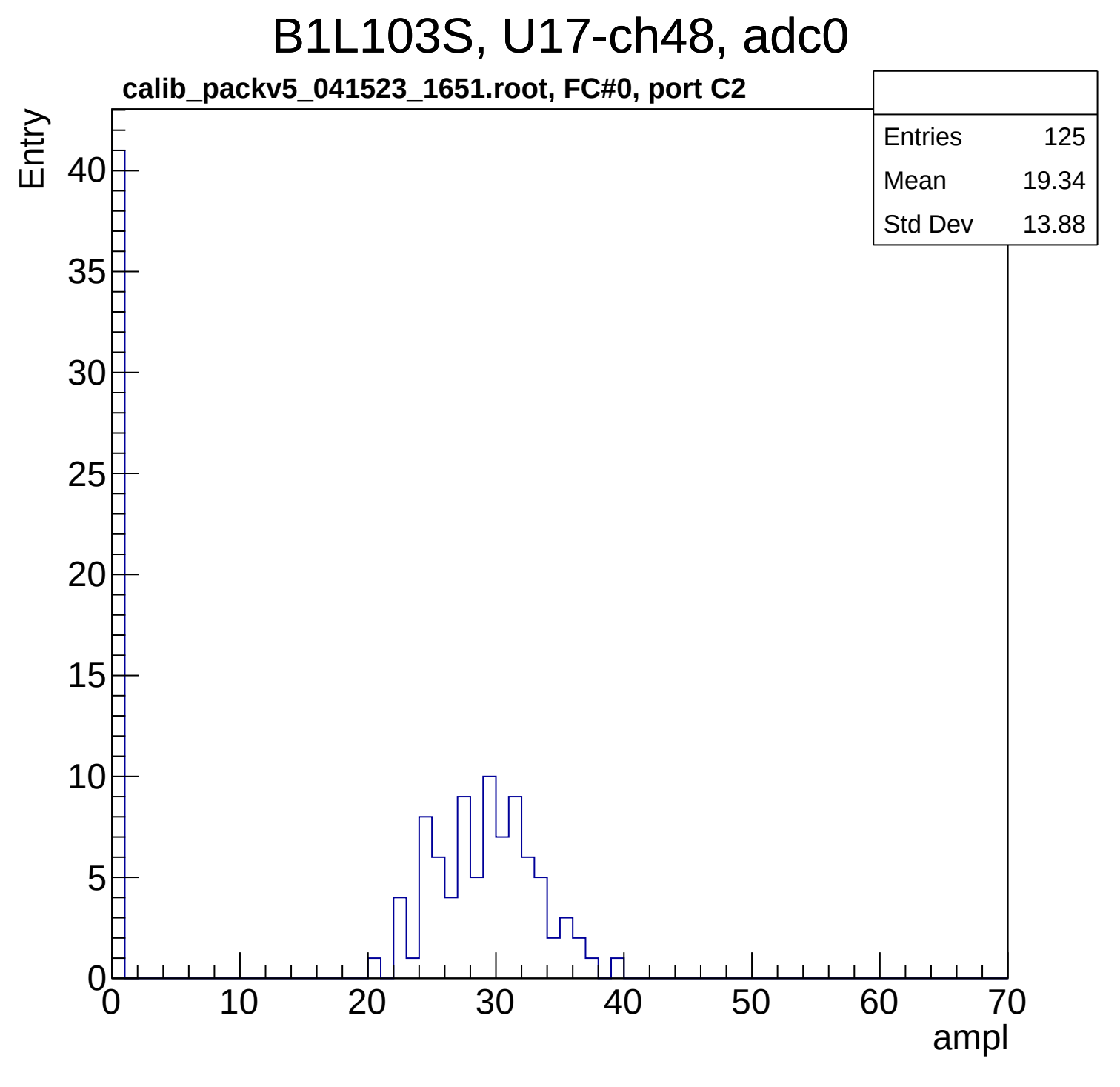
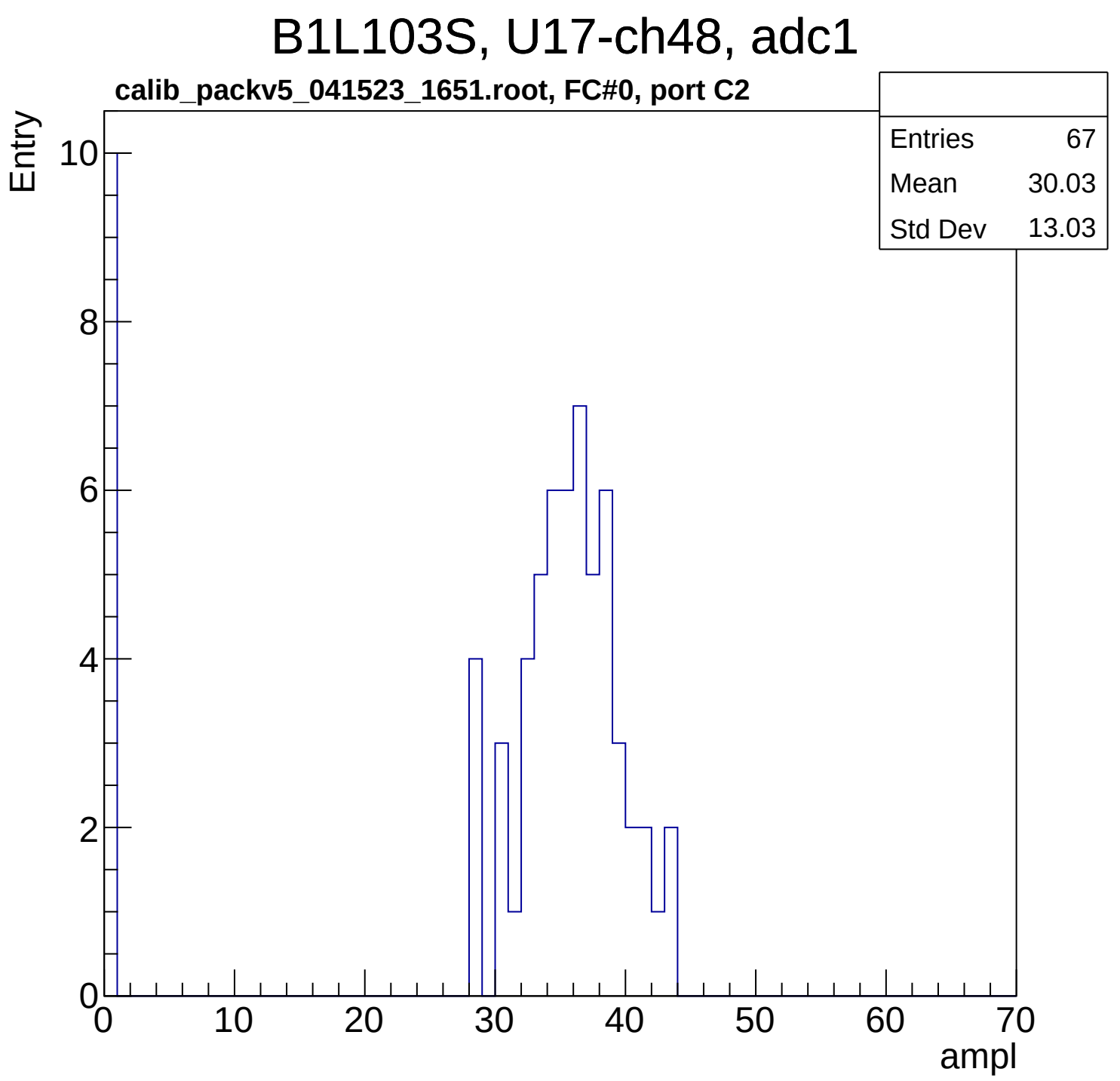
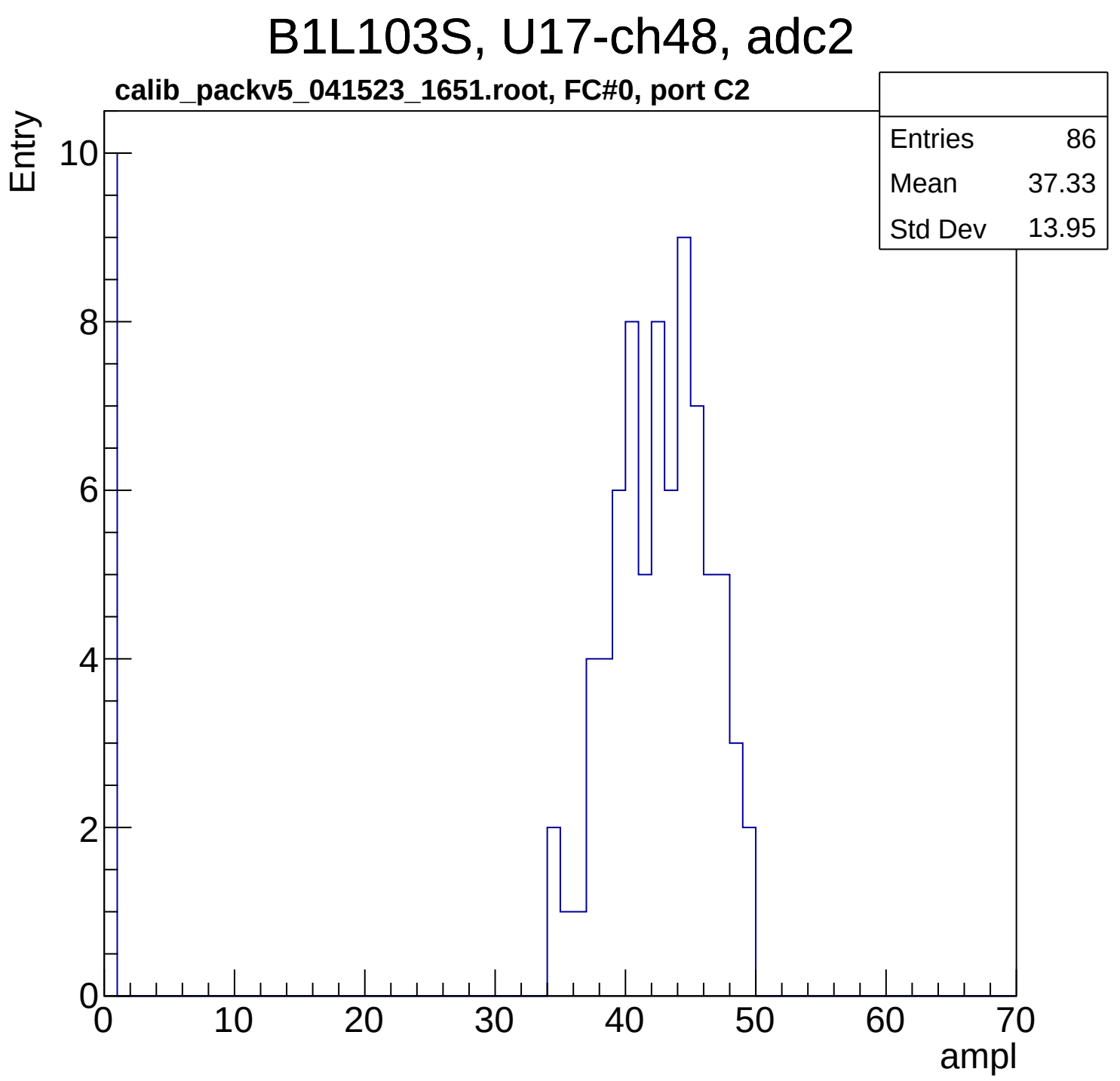
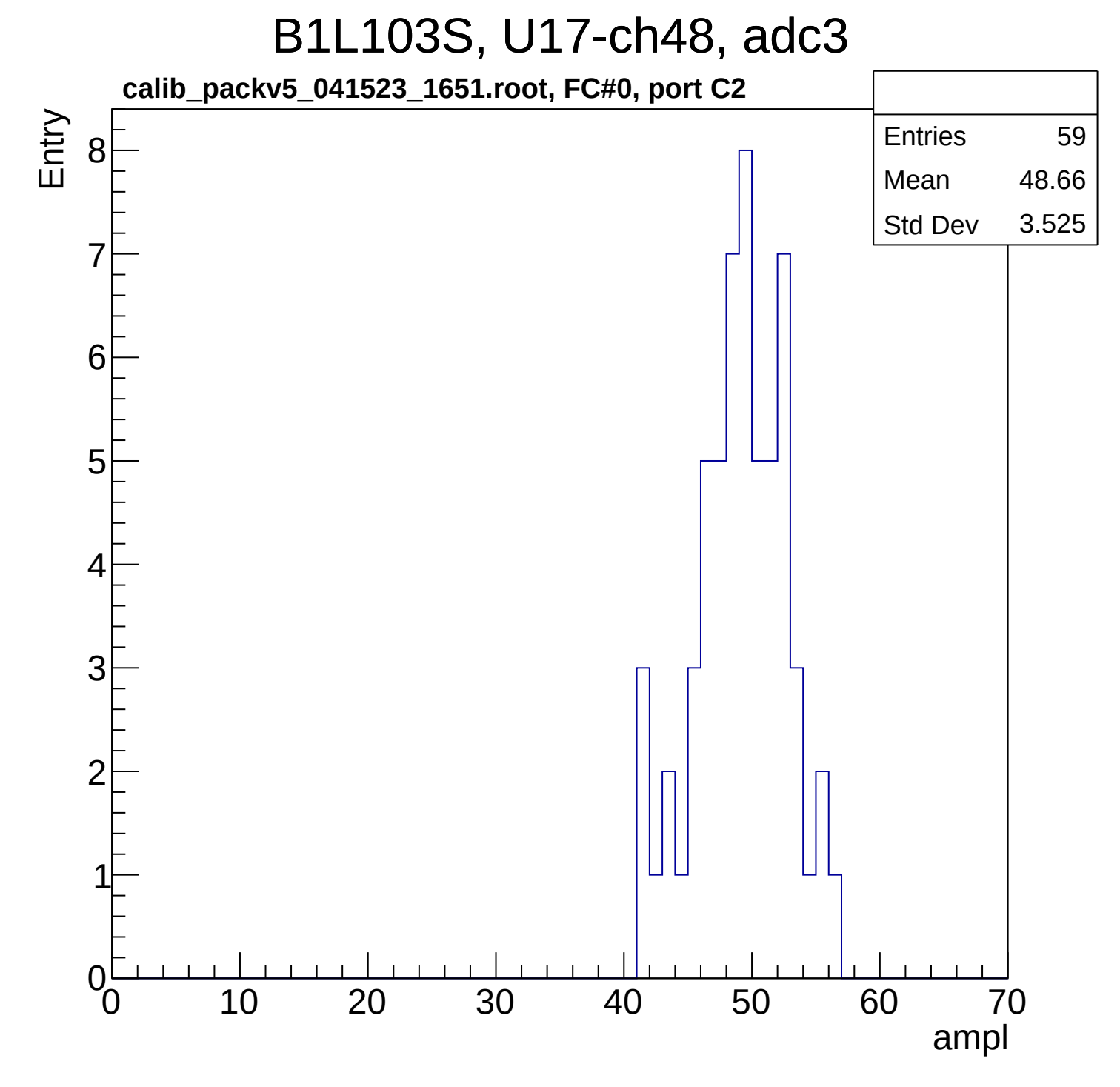

B1L103S, U17-ch47, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 3
Mean 61.67
Std Dev 1.886
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U17-ch47, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch48, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 125
Mean 19.34
Std Dev 13.88
Entry
0
5
10
15
20
25
30
35
40
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch48, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 30.03
Std Dev 13.03
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U17-ch48, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 37.33
Std Dev 13.95
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch48, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 48.66
Std Dev 3.525
Entry
ampl
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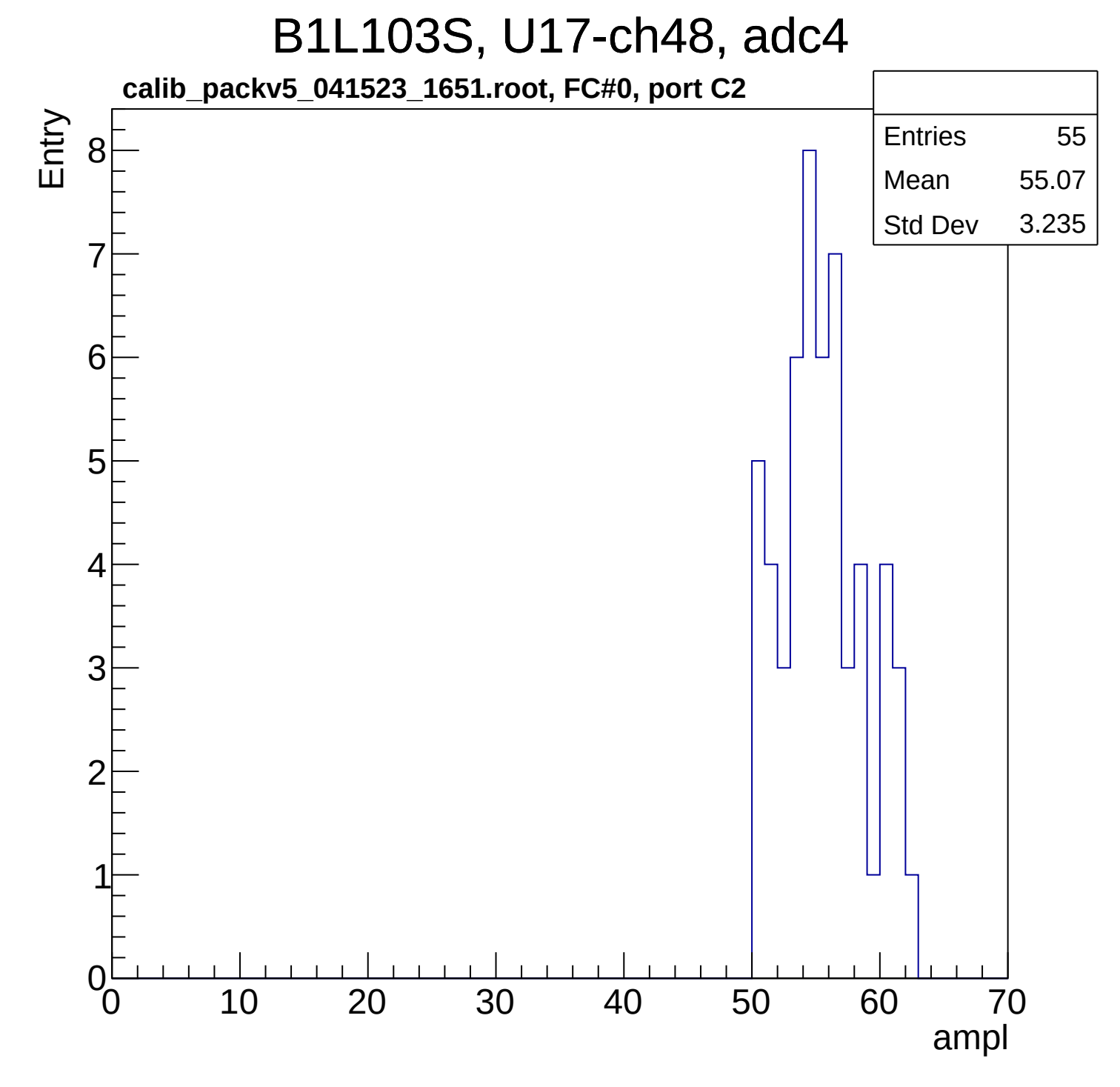
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U17-ch48, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 55.07
Std Dev 3.235
Entry
ampl
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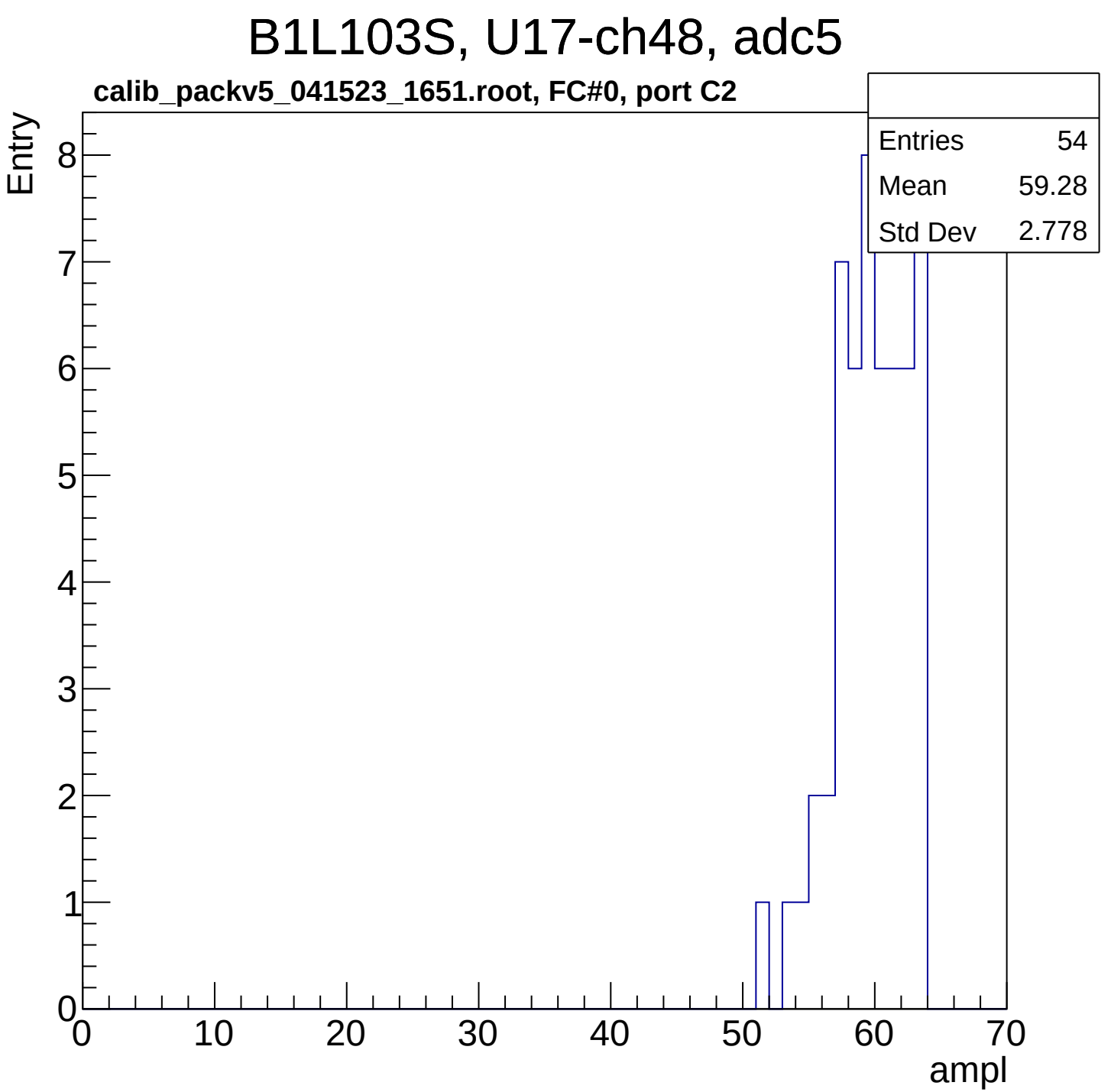
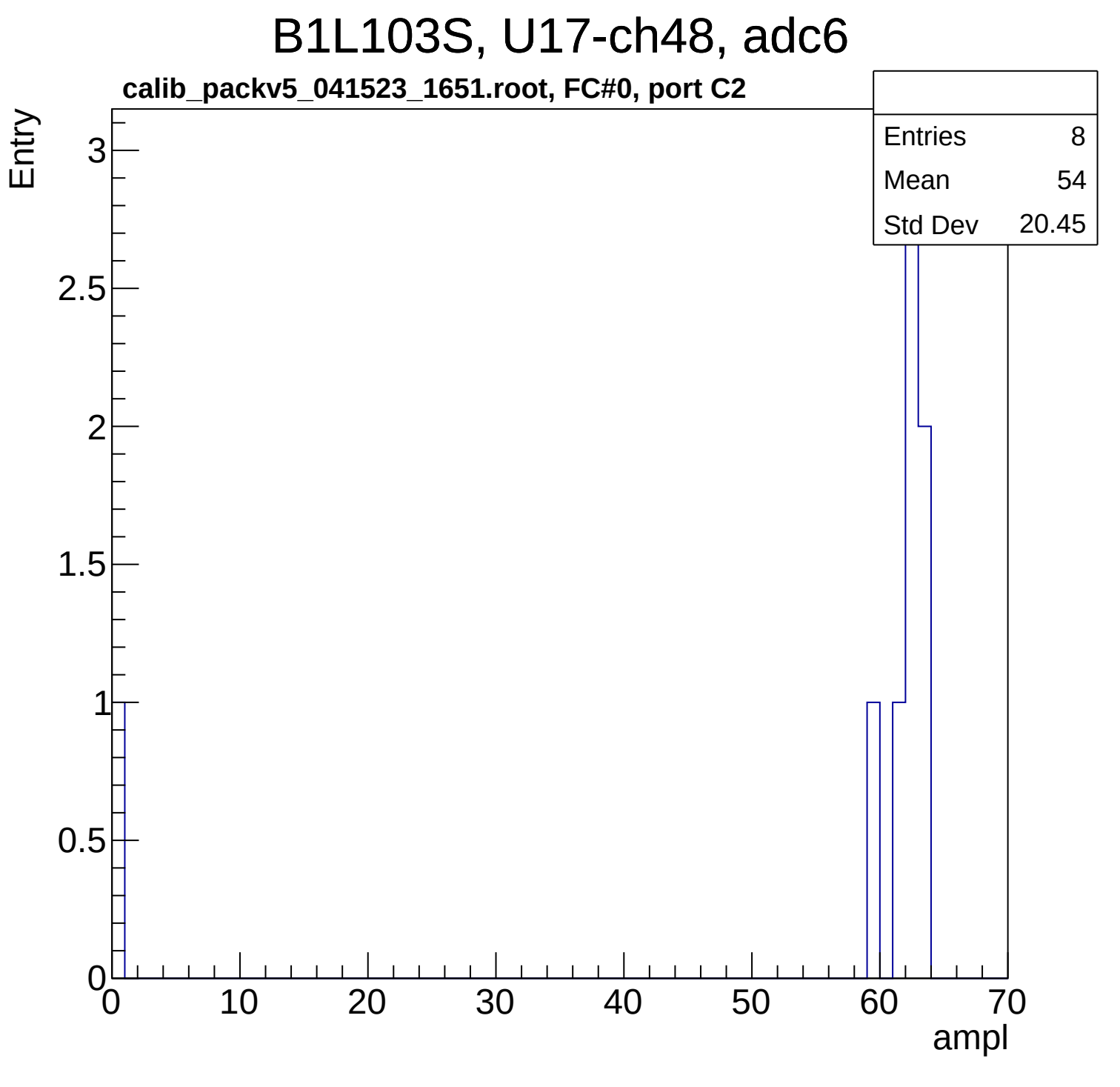
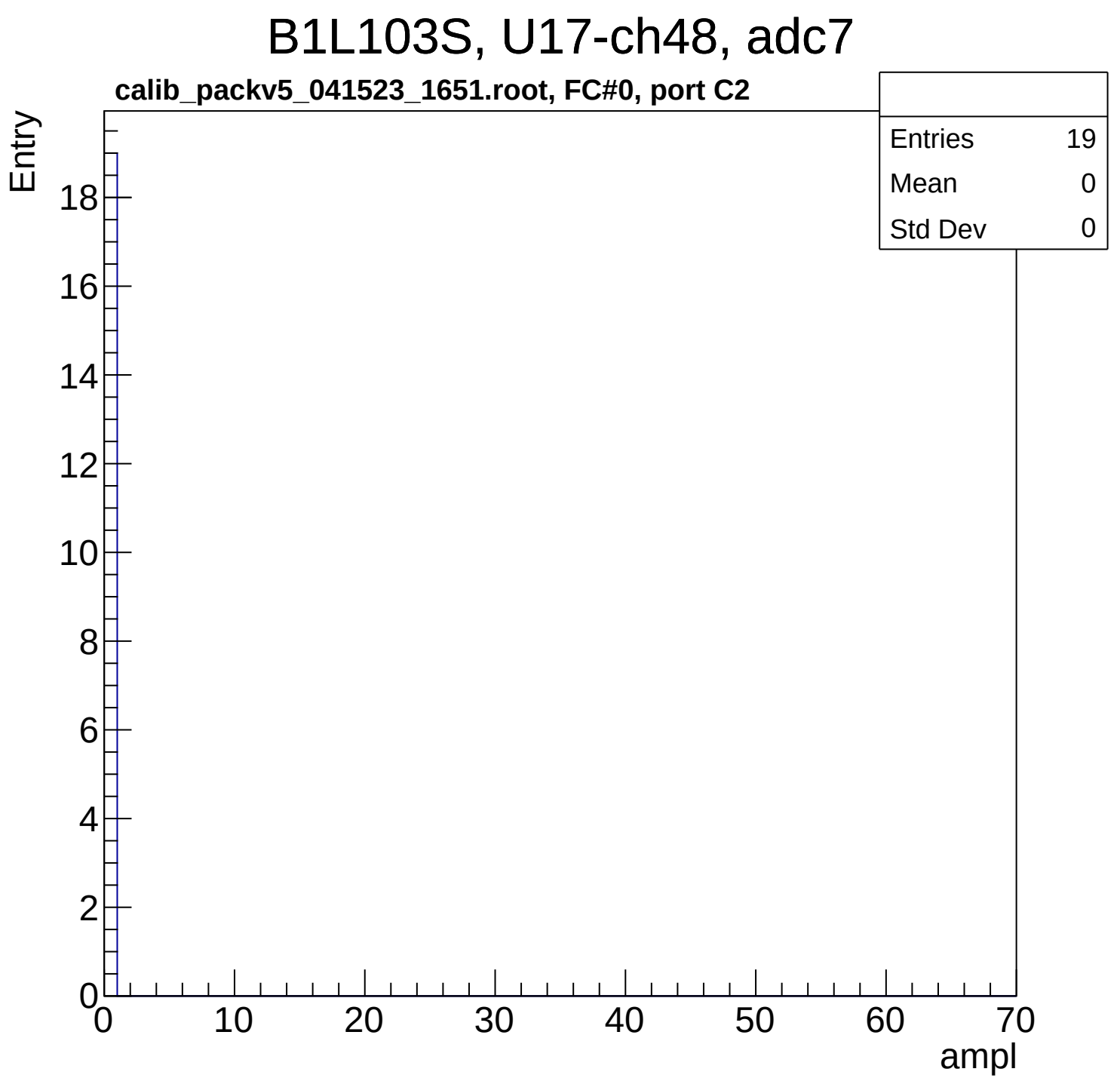
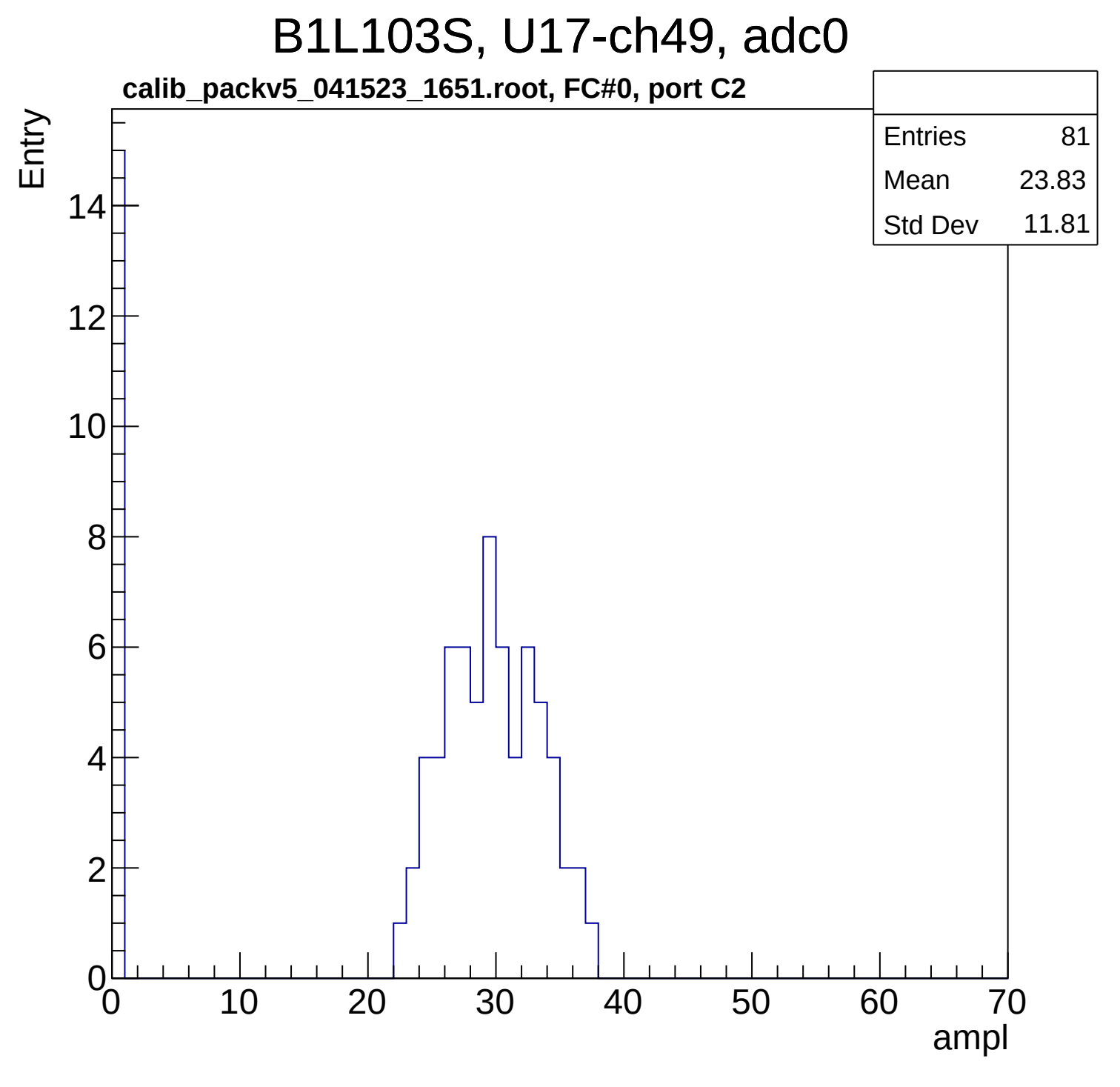
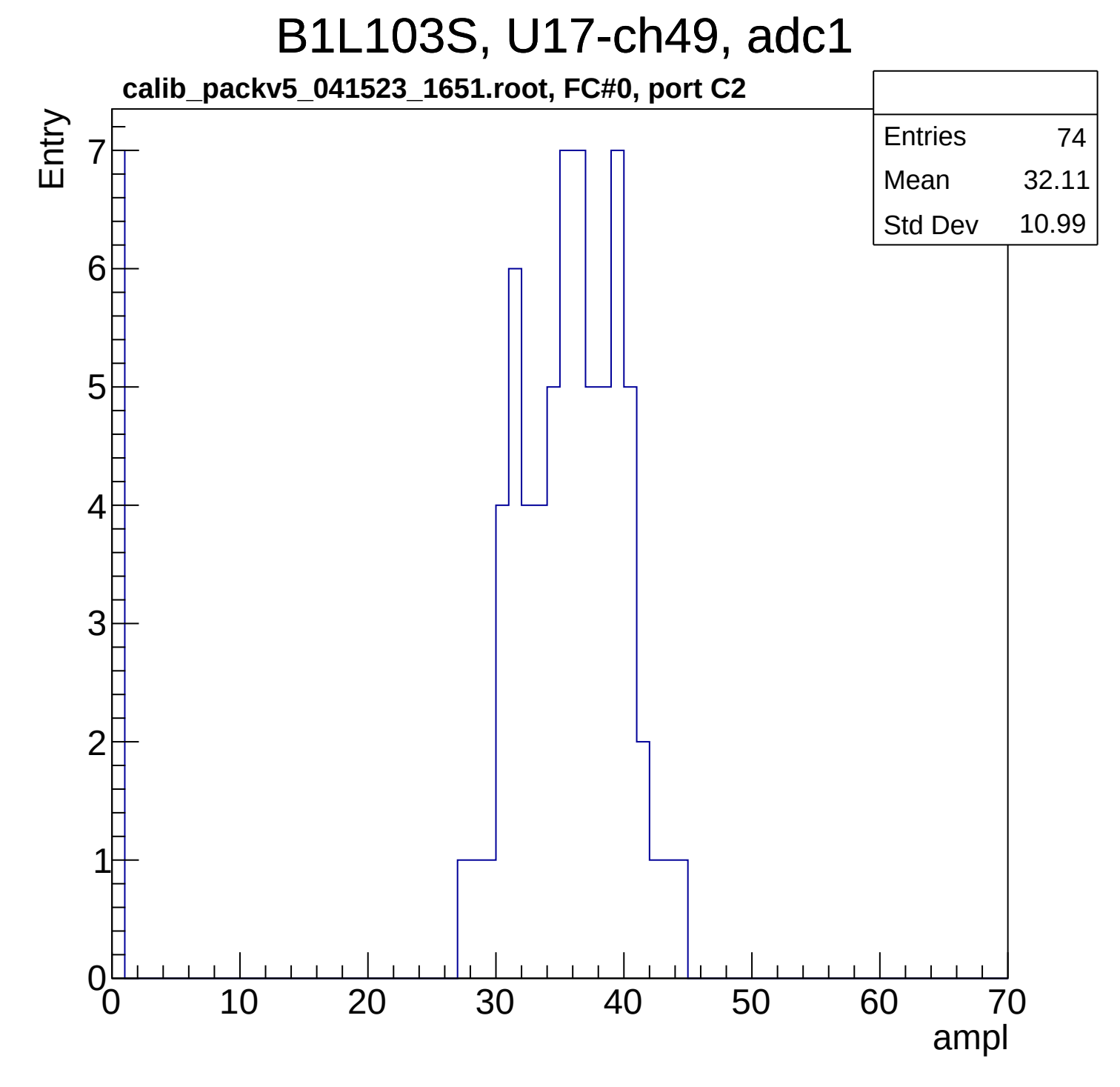
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

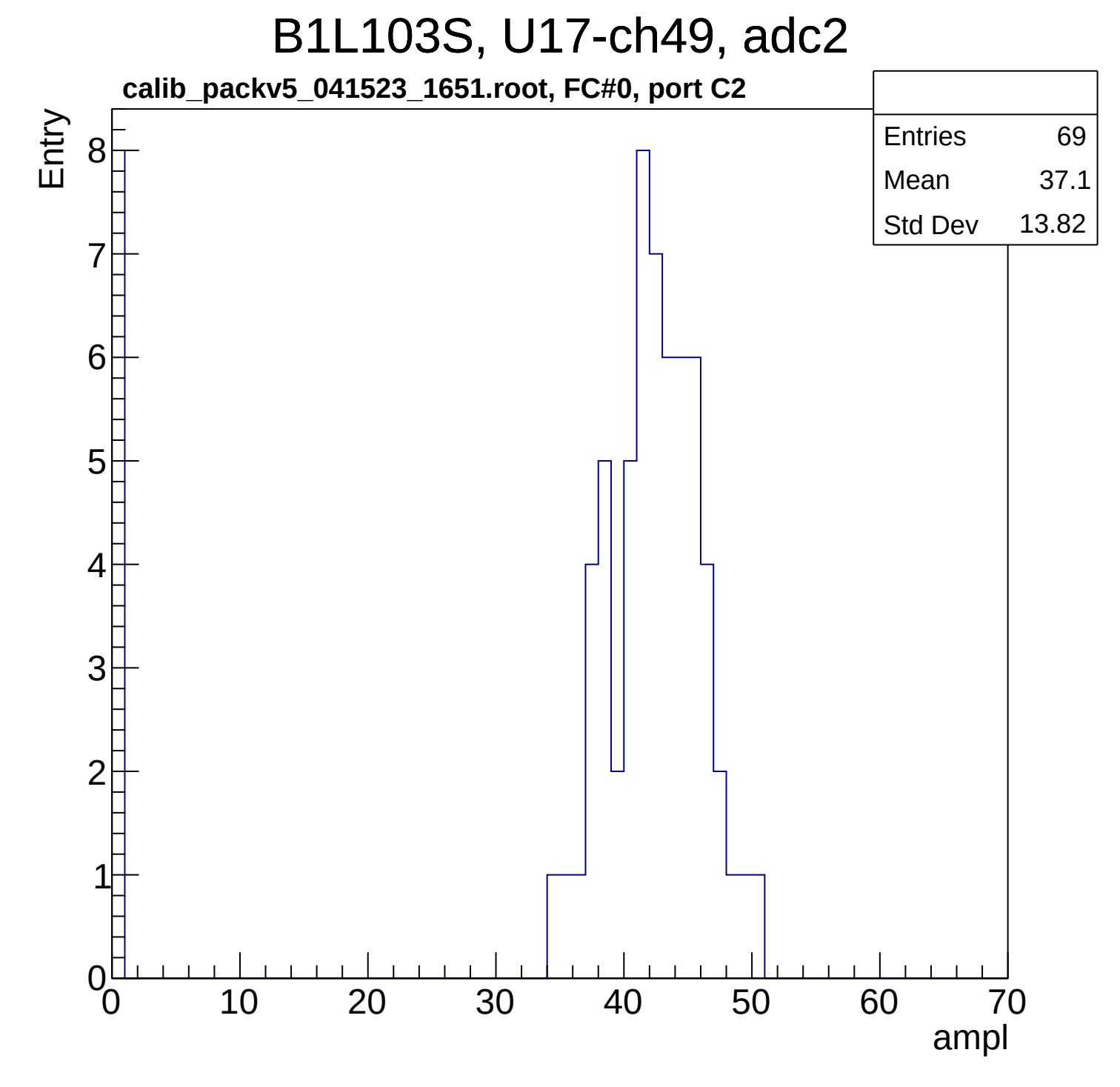

B1L103S, U17-ch48, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 59.28
Std Dev 2.778
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U17-ch48, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 54
Std Dev 20.45
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U17-ch48, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch49, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 23.83
Std Dev 11.81
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch49, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 32.11
Std Dev 10.99
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U17-ch49, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 37.1
Std Dev 13.82
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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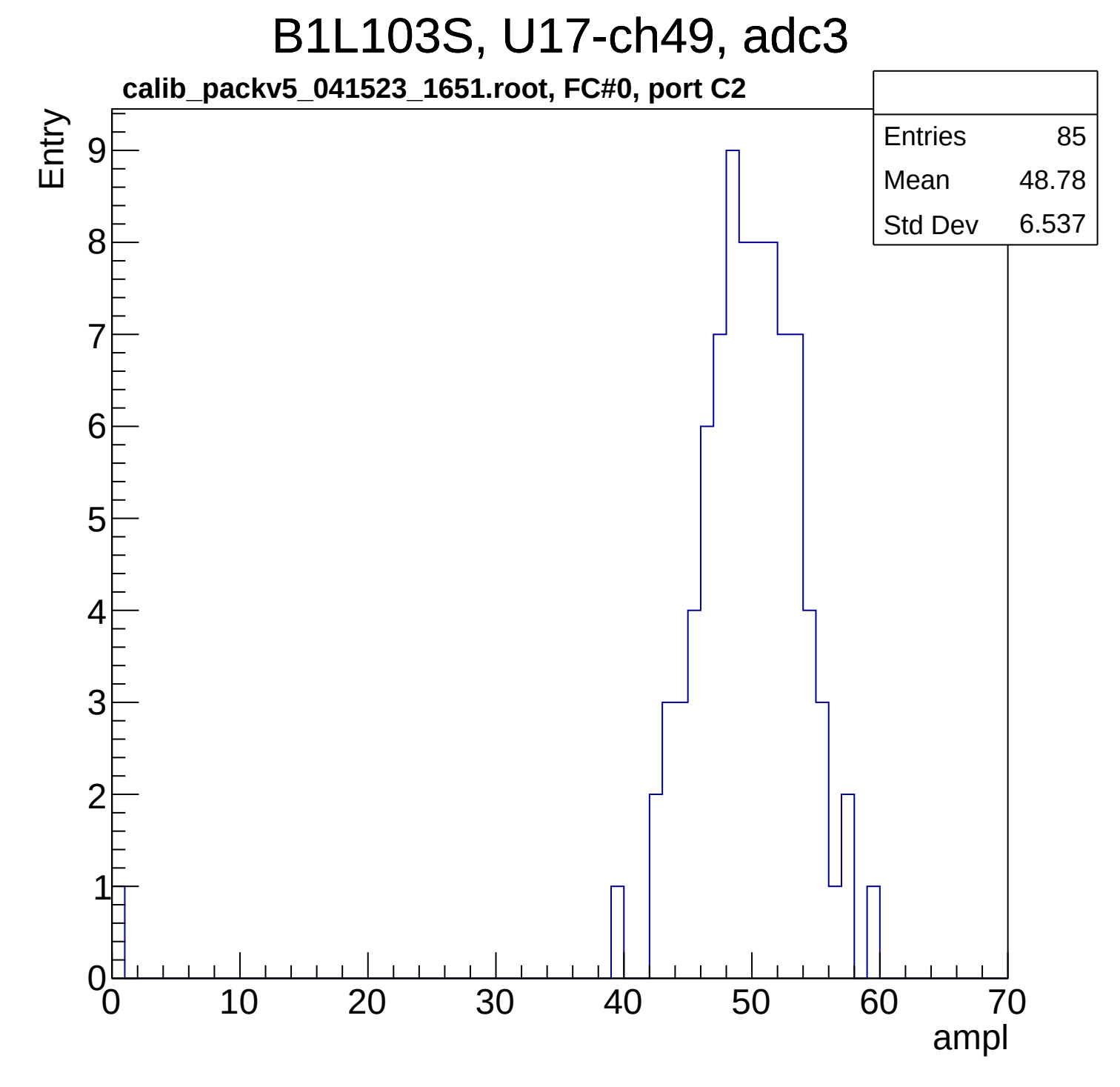
B1L103S, U17-ch49, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 48.78
Std Dev 6.537
Entry
ampl
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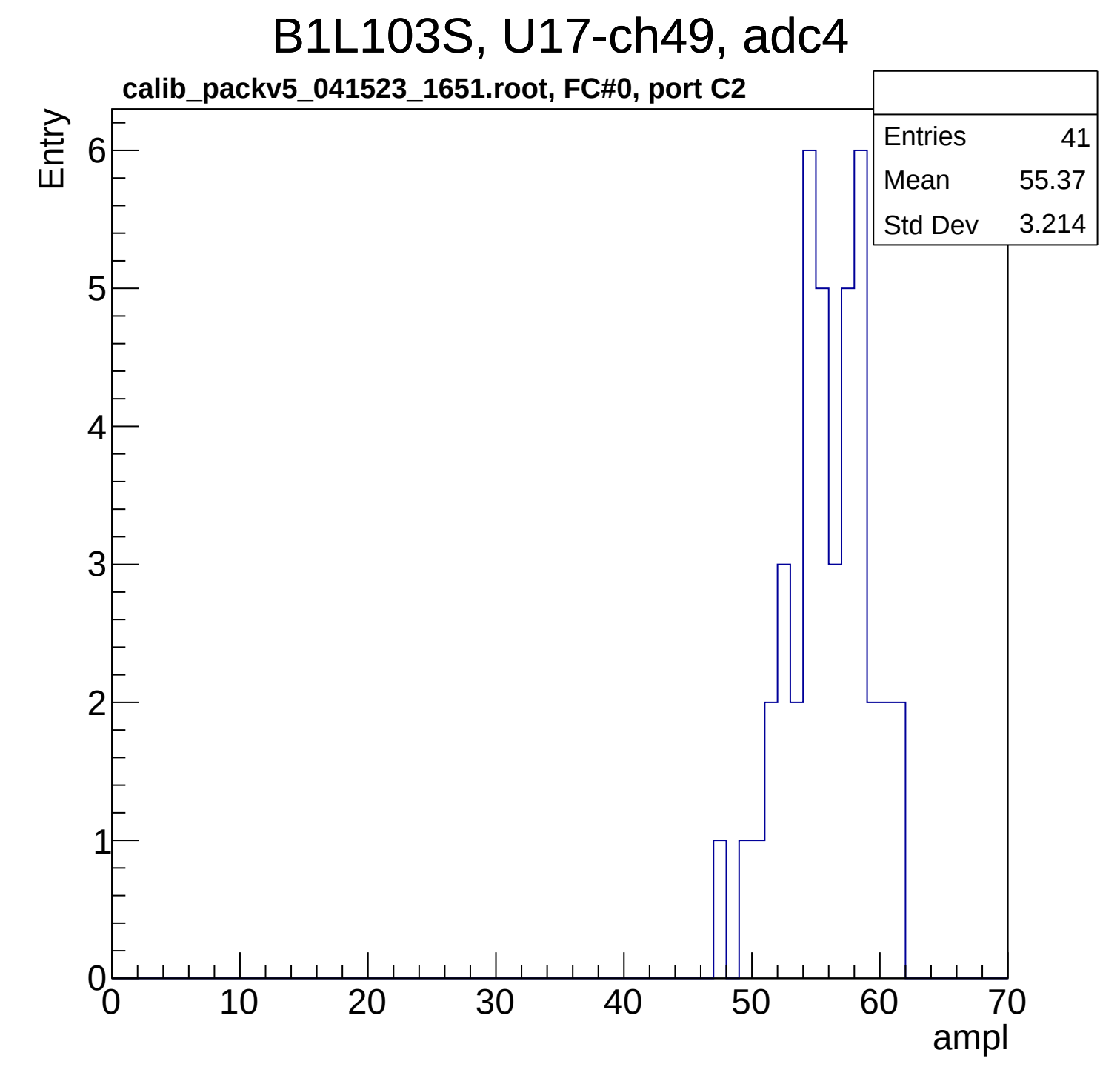
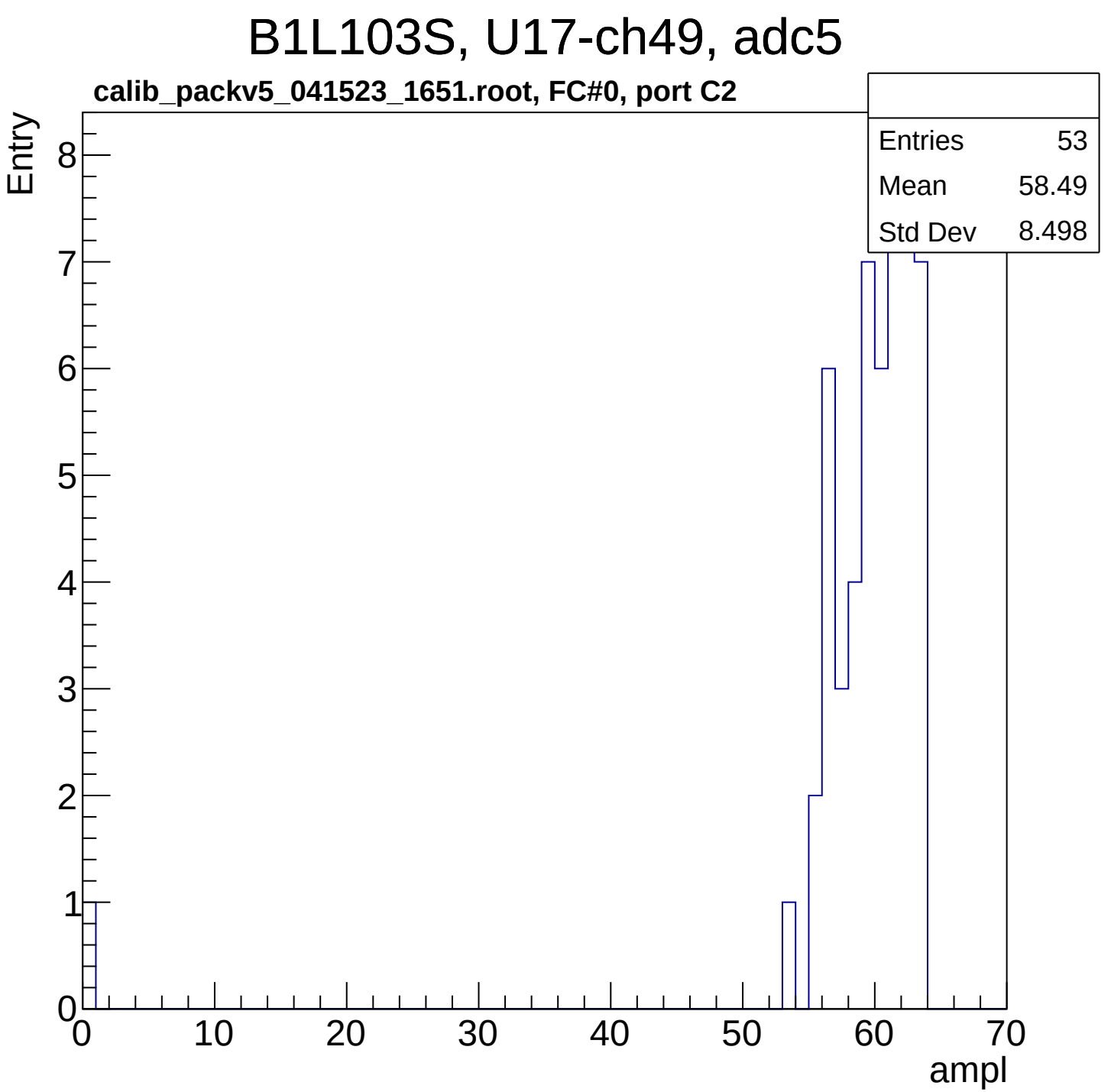
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U17-ch49, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 41
Mean 55.37
Std Dev 3.214
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U17-ch49, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 58.49
Std Dev 8.498
Entry
ampl
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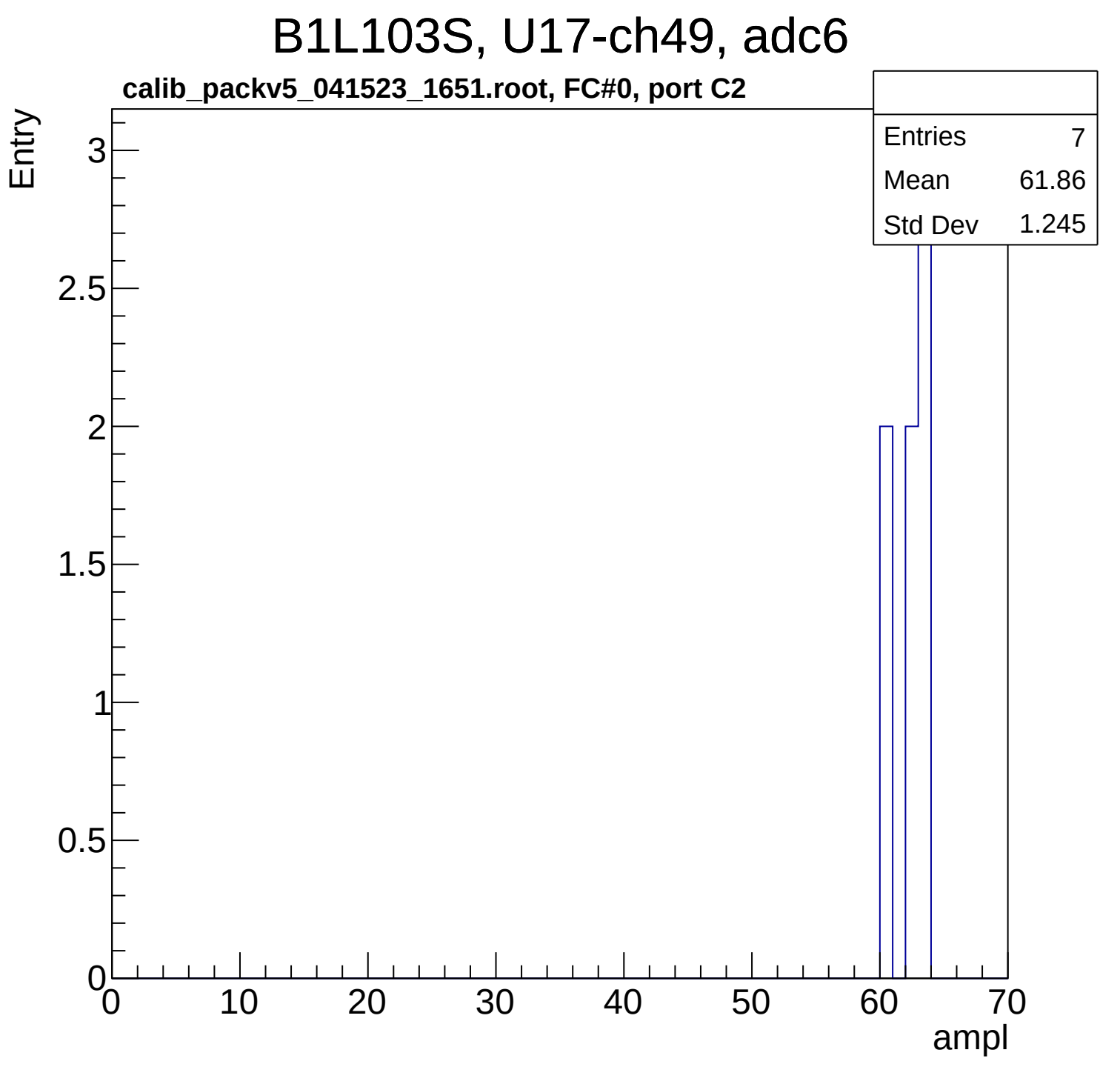
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U17-ch49, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 61.86
Std Dev 1.245
Entry
ampl
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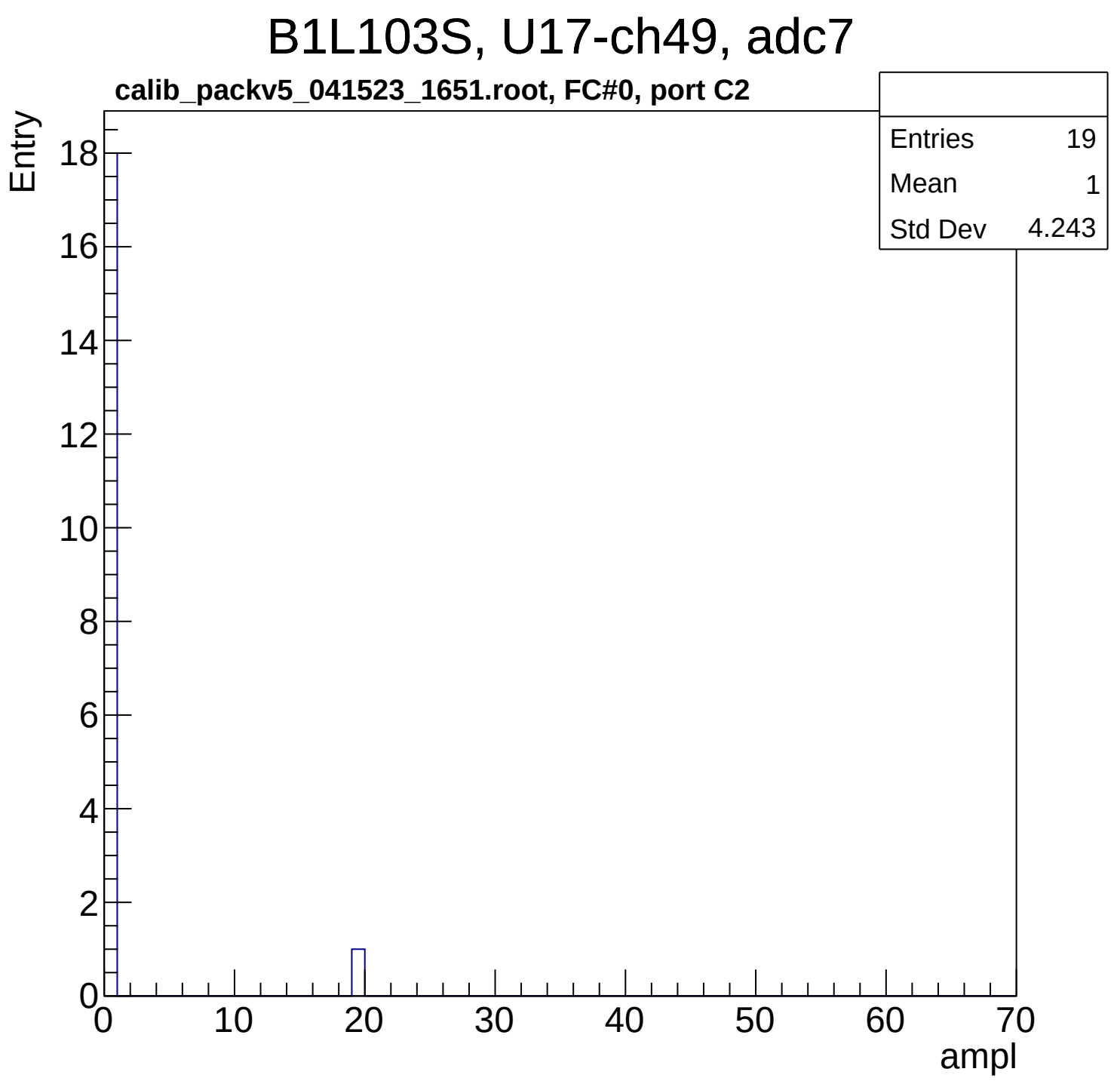
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U17-ch49, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1
Std Dev 4.243
Entry
0
2
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6
8
10
12
14
16
18
0
10
20
30
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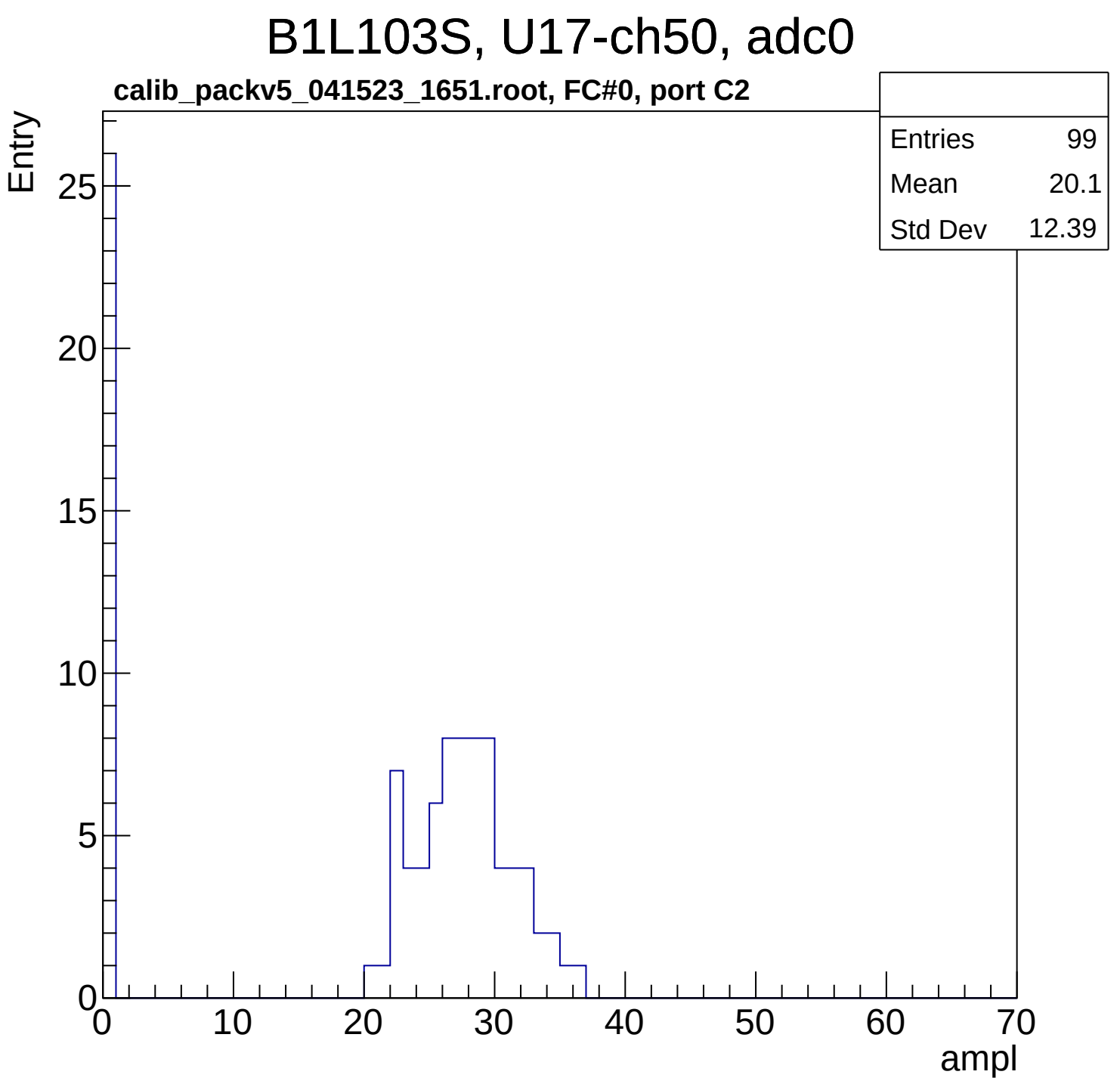
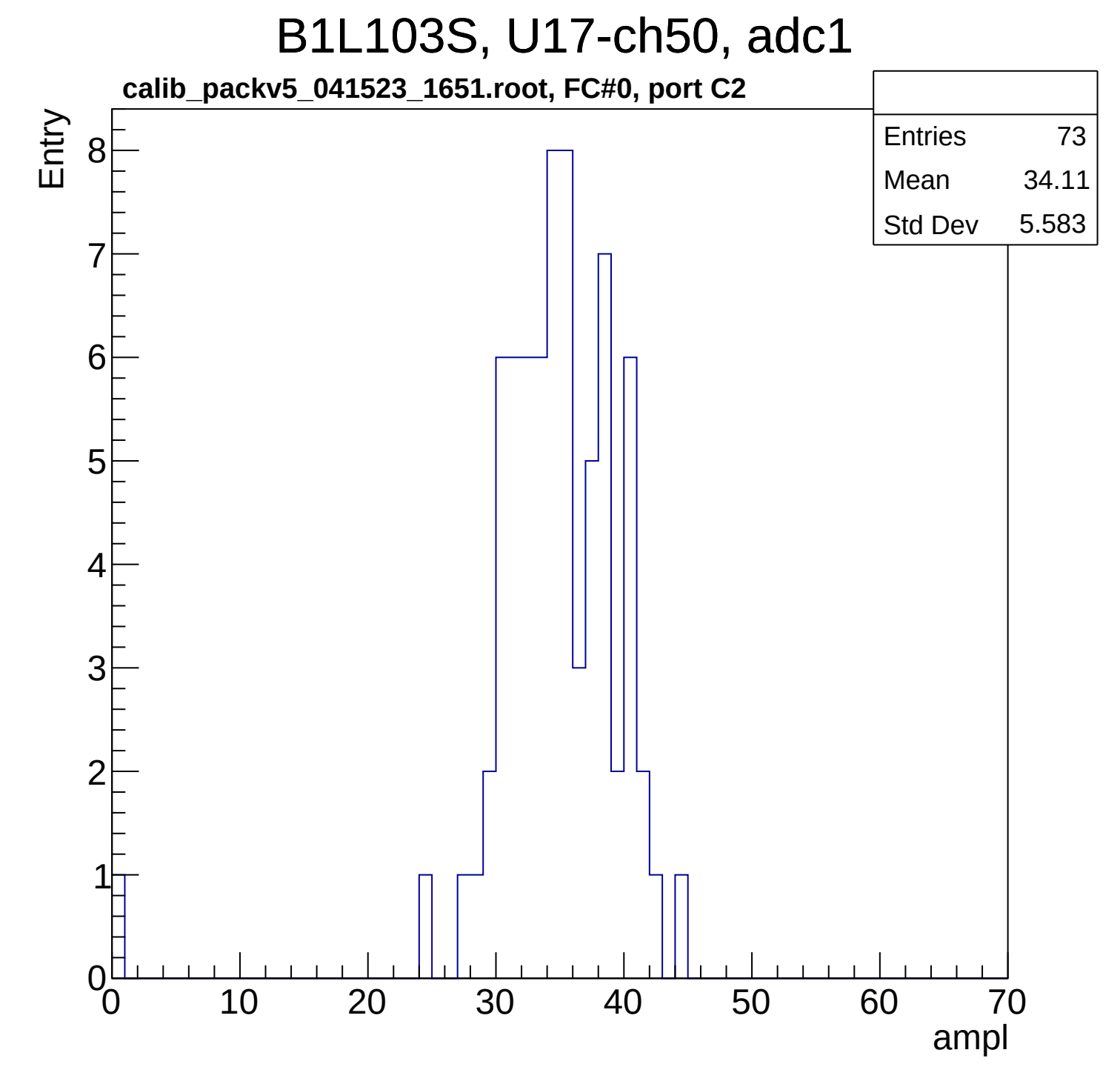
50
60
70
ampl


B1L103S, U17-ch50, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 99
Mean 20.1
Std Dev 12.39
Entry
0
5
10
15
20
25
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch50, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 34.11
Std Dev 5.583
Entry
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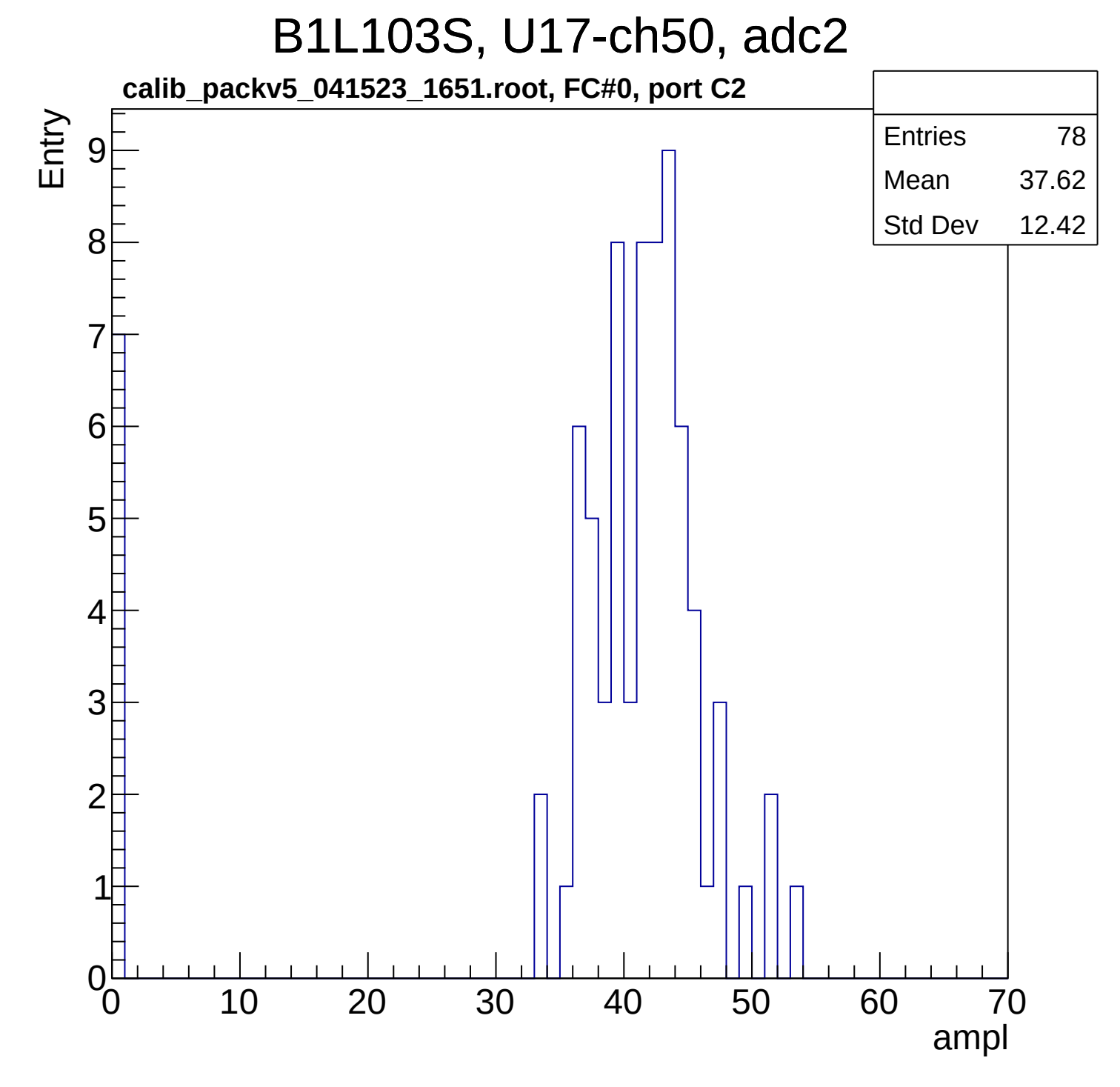
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch50, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 37.62
Std Dev 12.42
Entry
ampl
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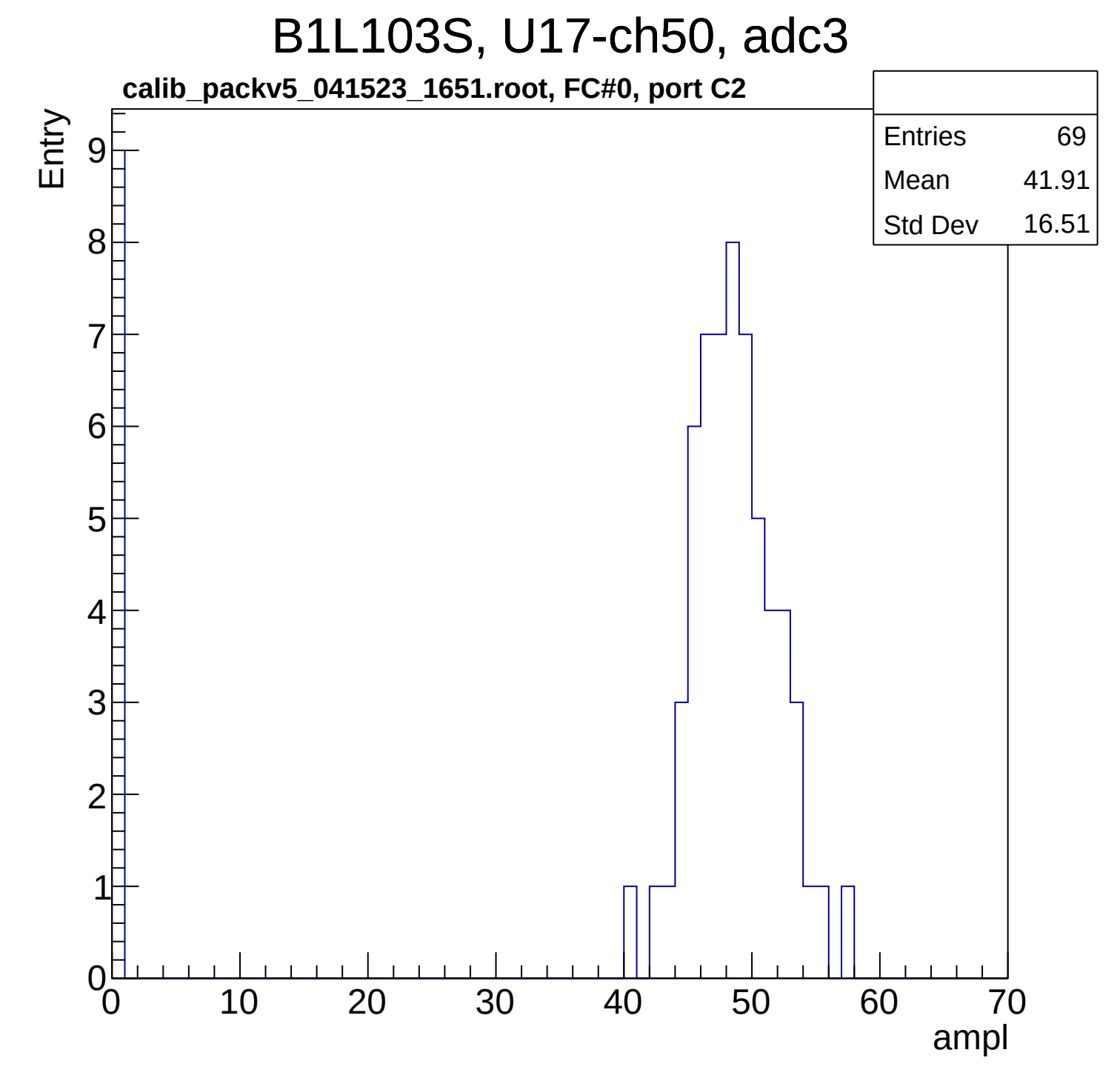
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U17-ch50, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 41.91
Std Dev 16.51
Entry
ampl
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2
3
4
5
6
7
8
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0
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20
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40
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60
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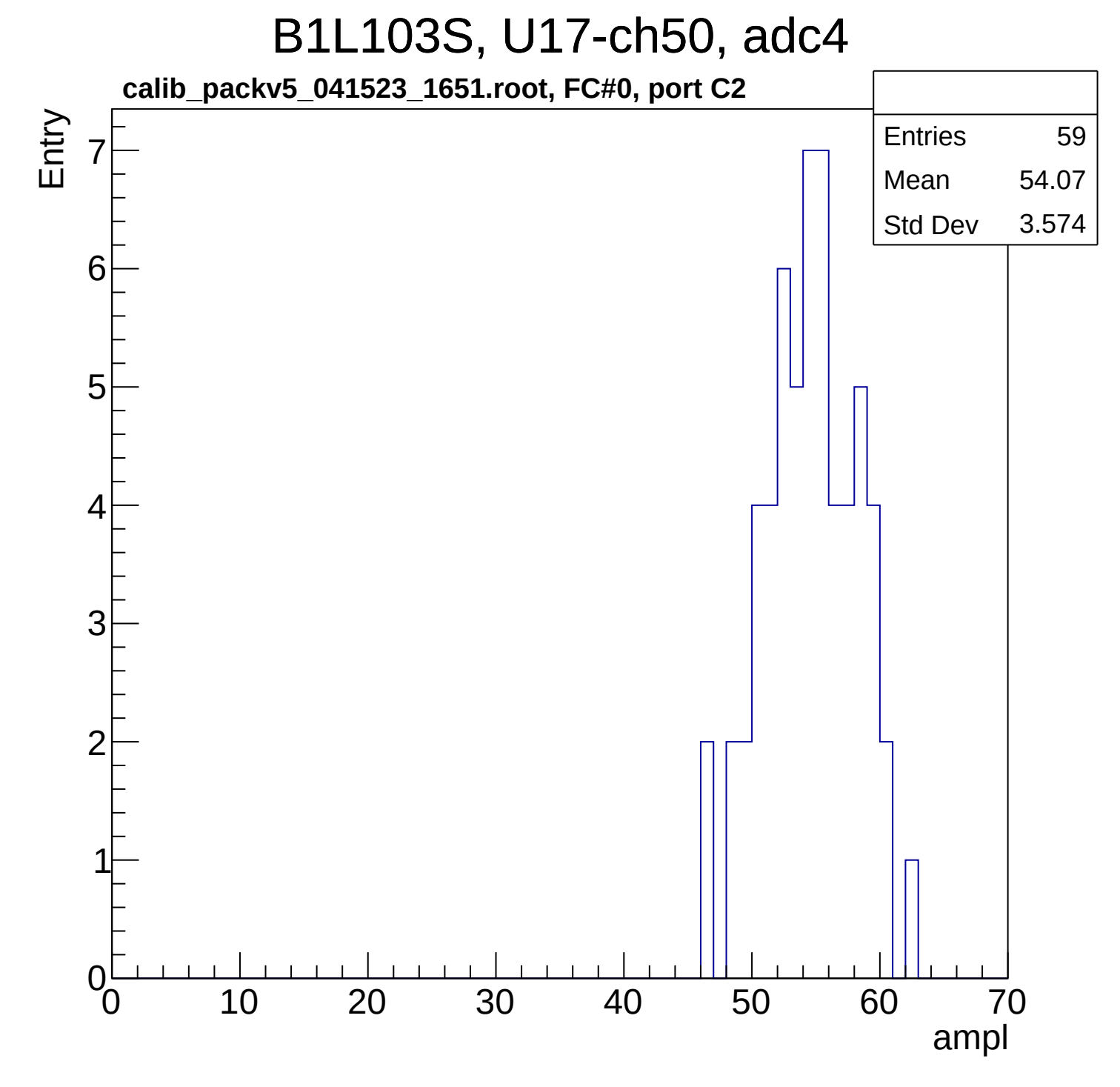
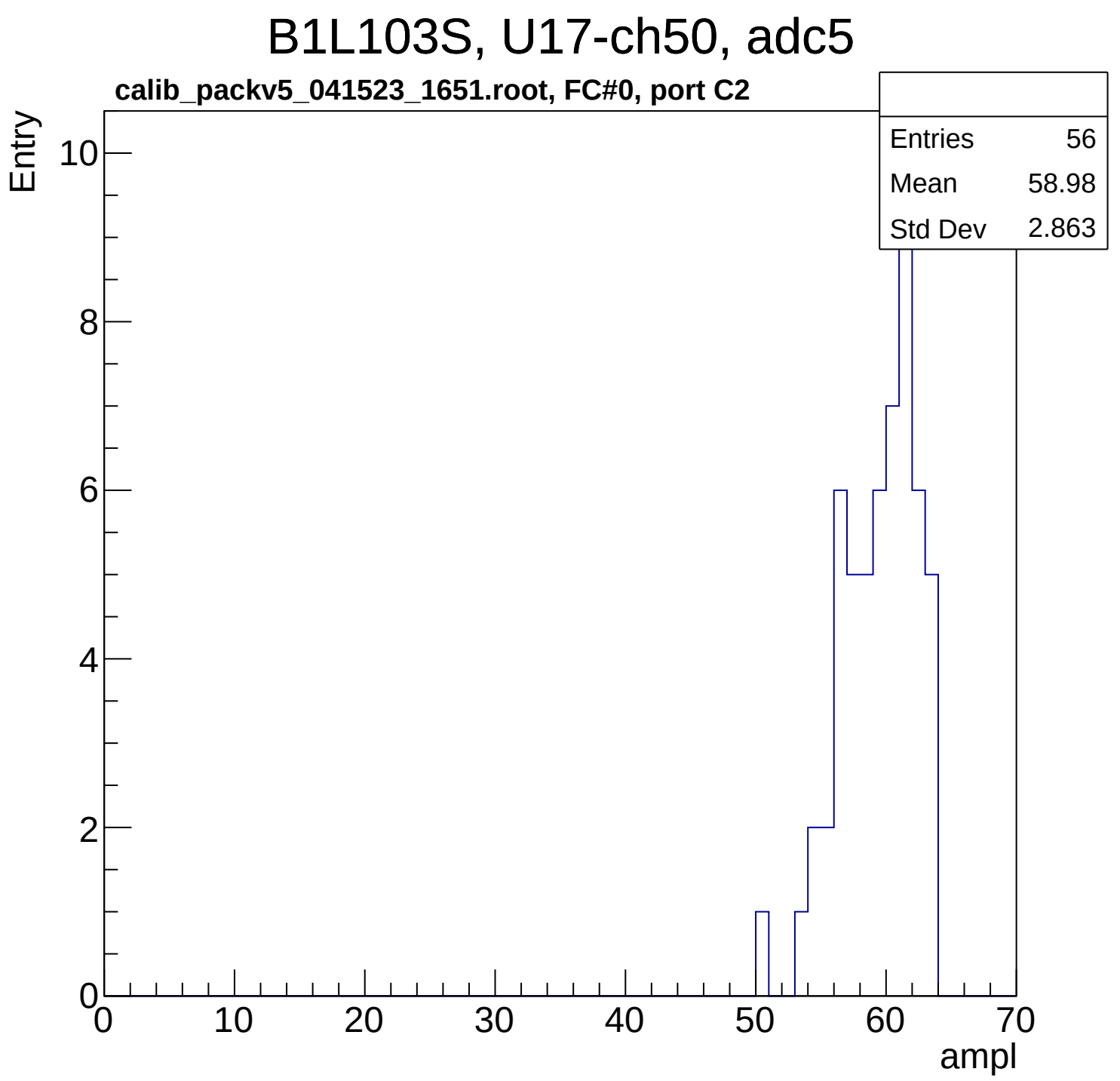

B1L103S, U17-ch50, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 54.07
Std Dev 3.574
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U17-ch50, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 58.98
Std Dev 2.863
Entry
ampl
0
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4
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8
10
0
10
20
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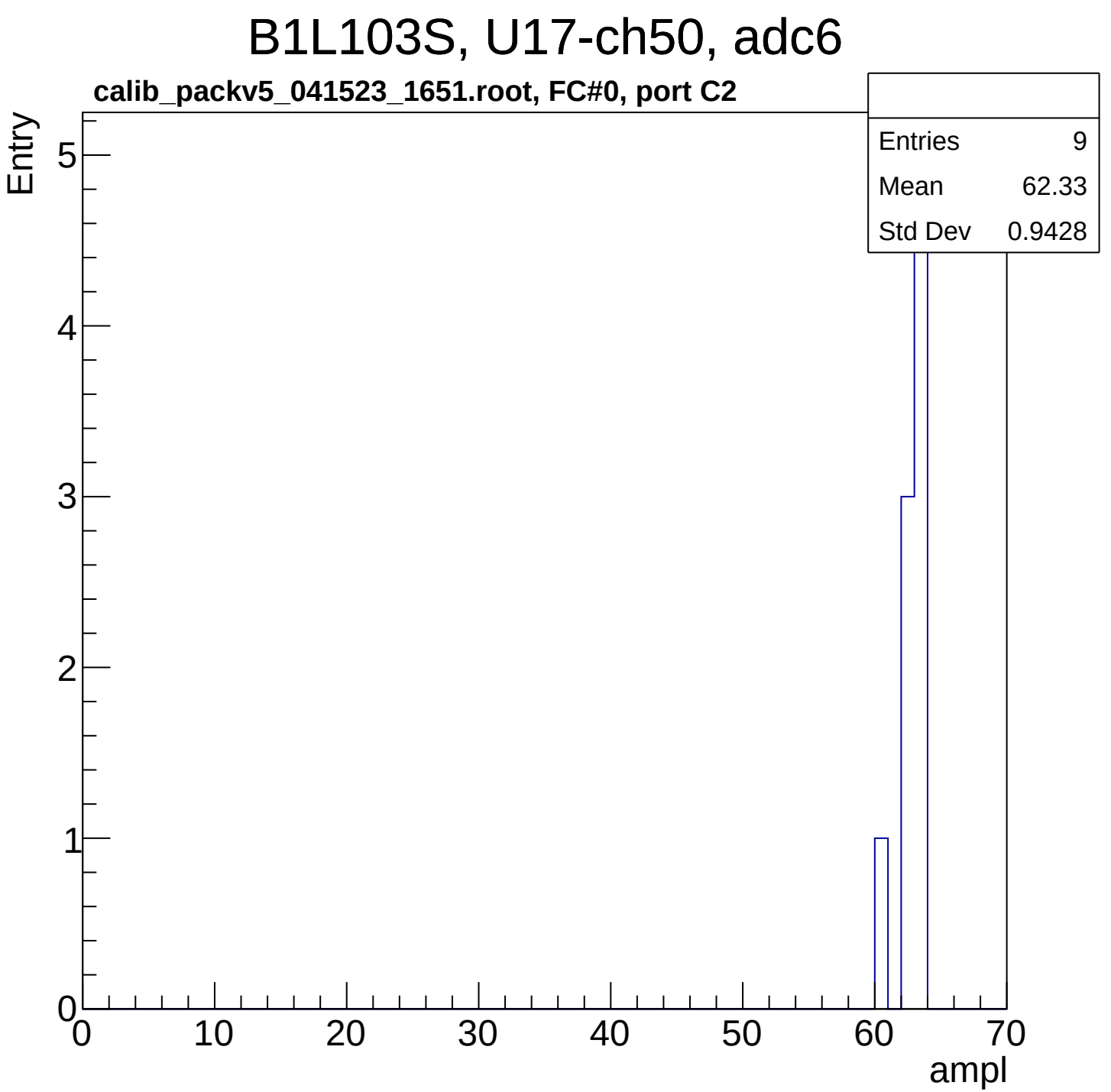
40
50
60
70


B1L103S, U17-ch50, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 9
Mean 62.33
Std Dev 0.9428
Entry
0
1
2
3
4
5
0
10
20
30
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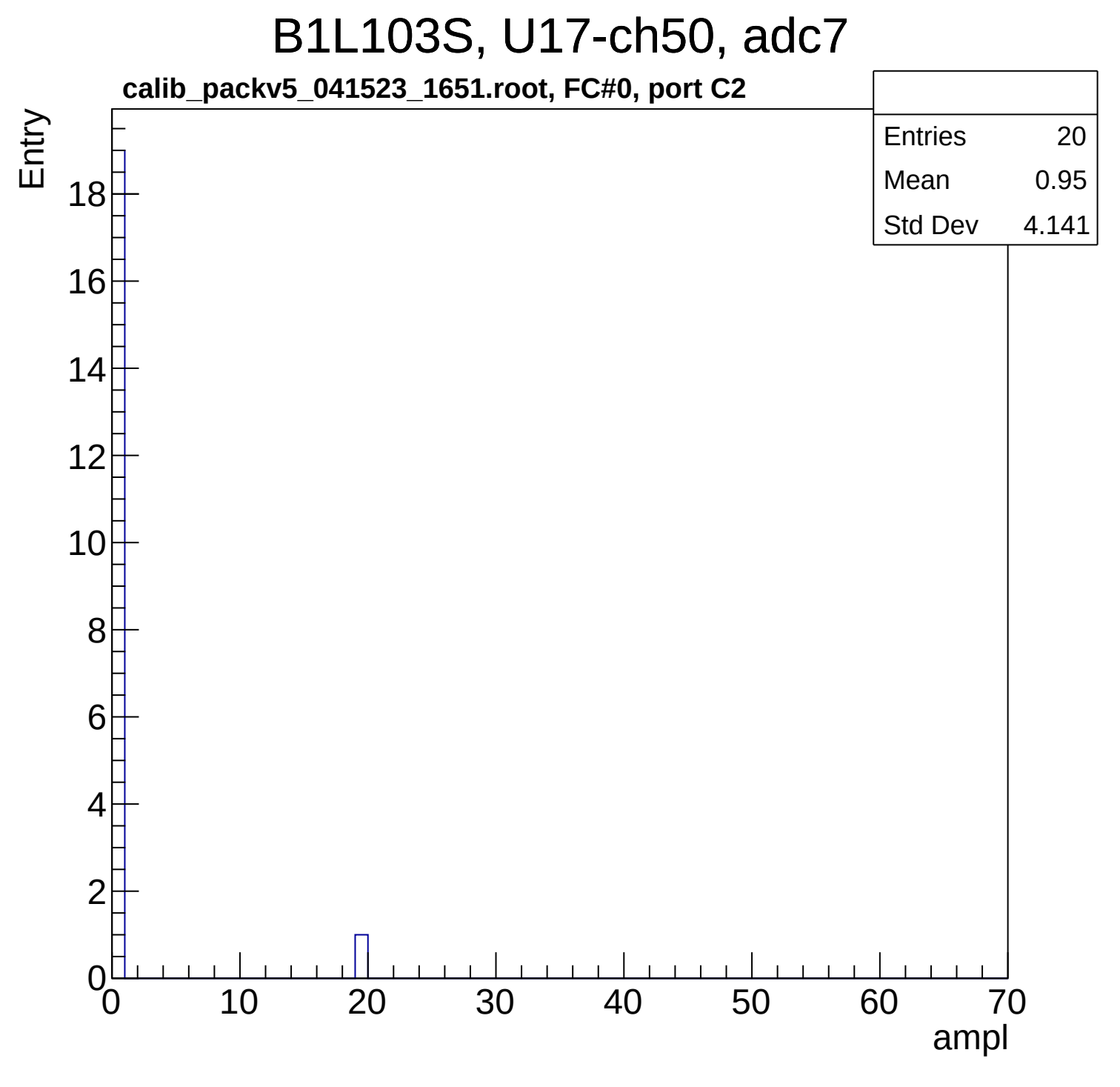
50
60
70
ampl


B1L103S, U17-ch50, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 0.95
Std Dev 4.141
Entry
0
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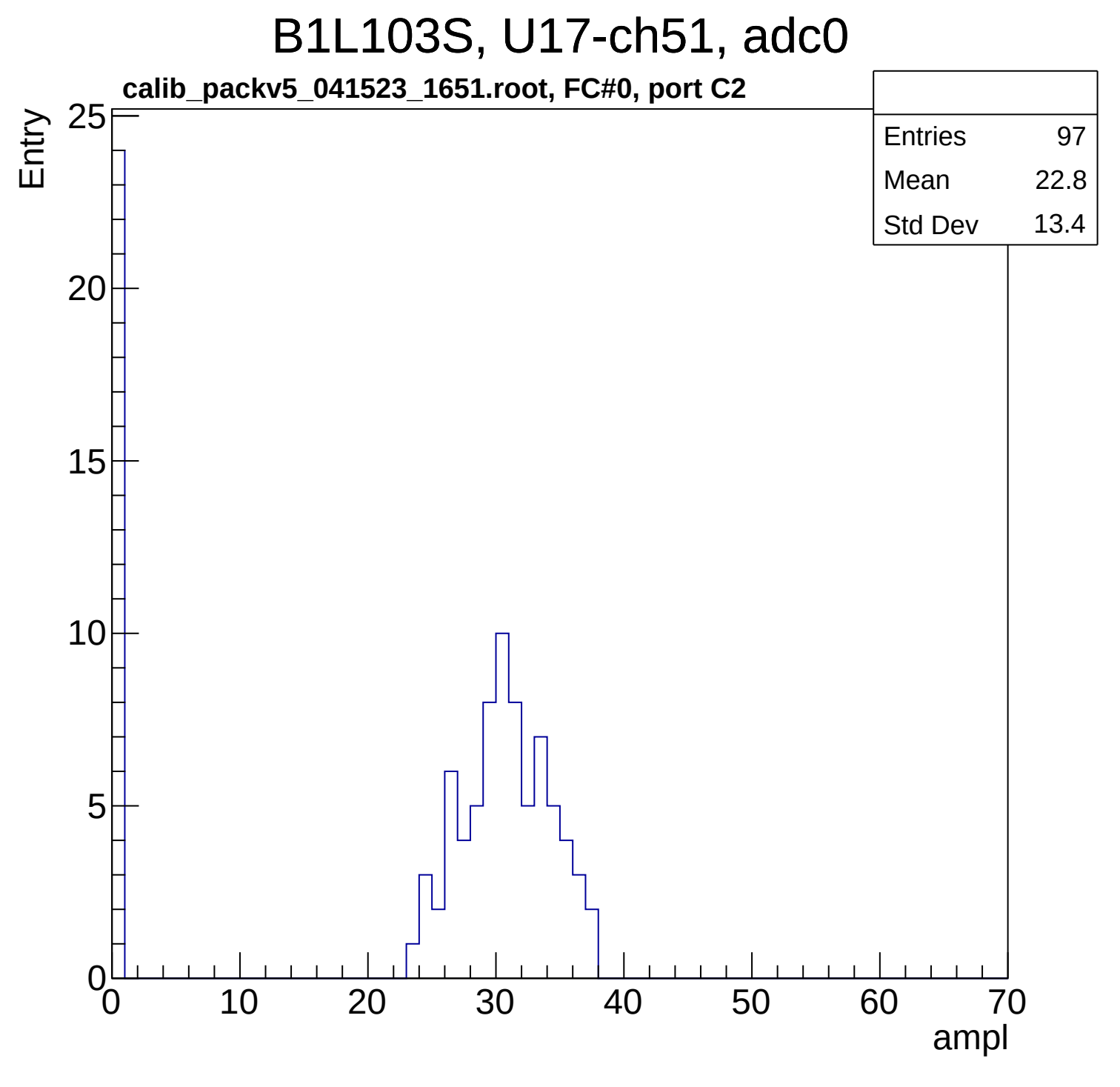
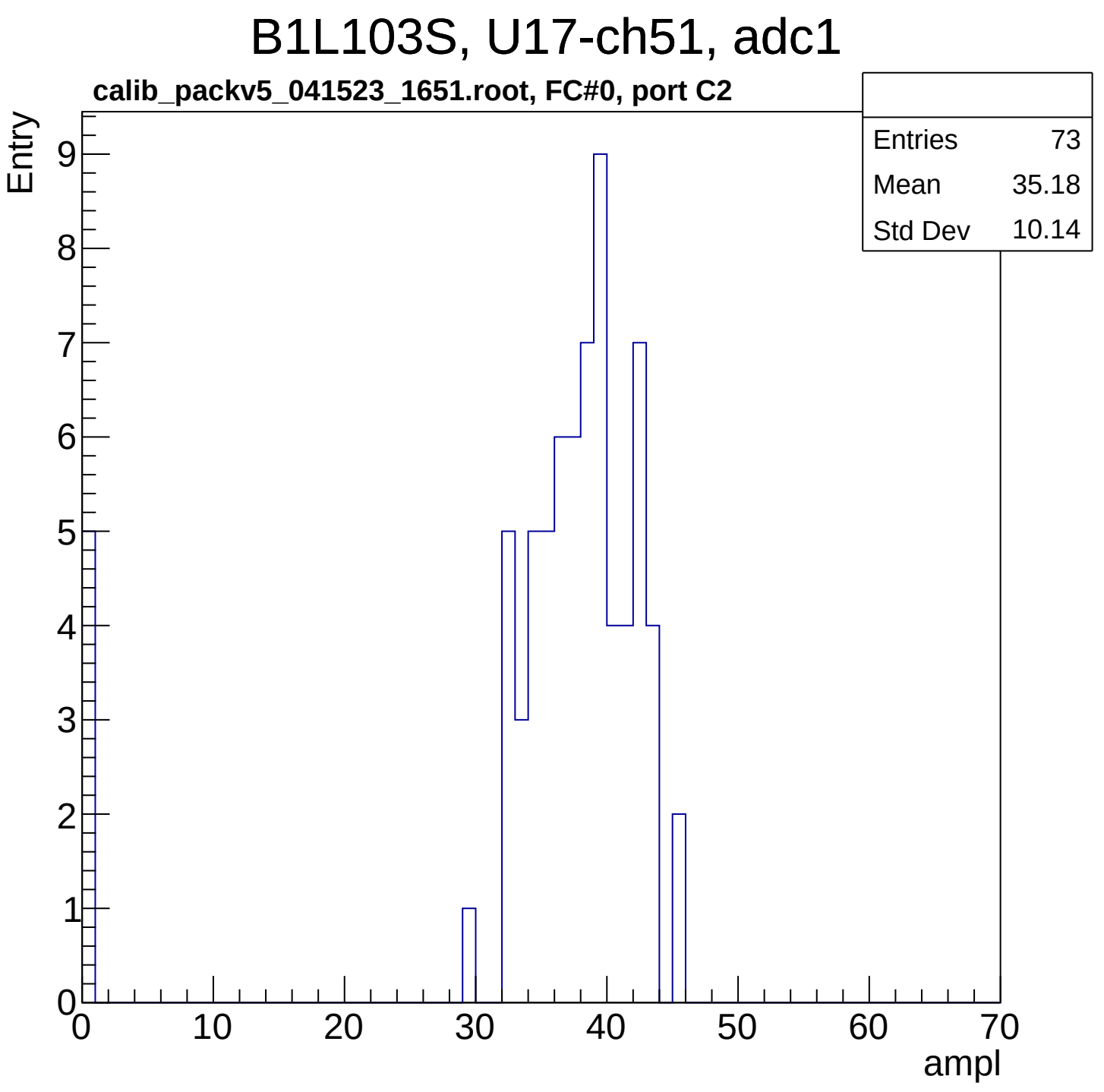
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch51, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 97
Mean 22.8
Std Dev 13.4
Entry
ampl
0
5
10
15
20
25
0
10
20
30
40
50
60
70


B1L103S, U17-ch51, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 35.18
Std Dev 10.14
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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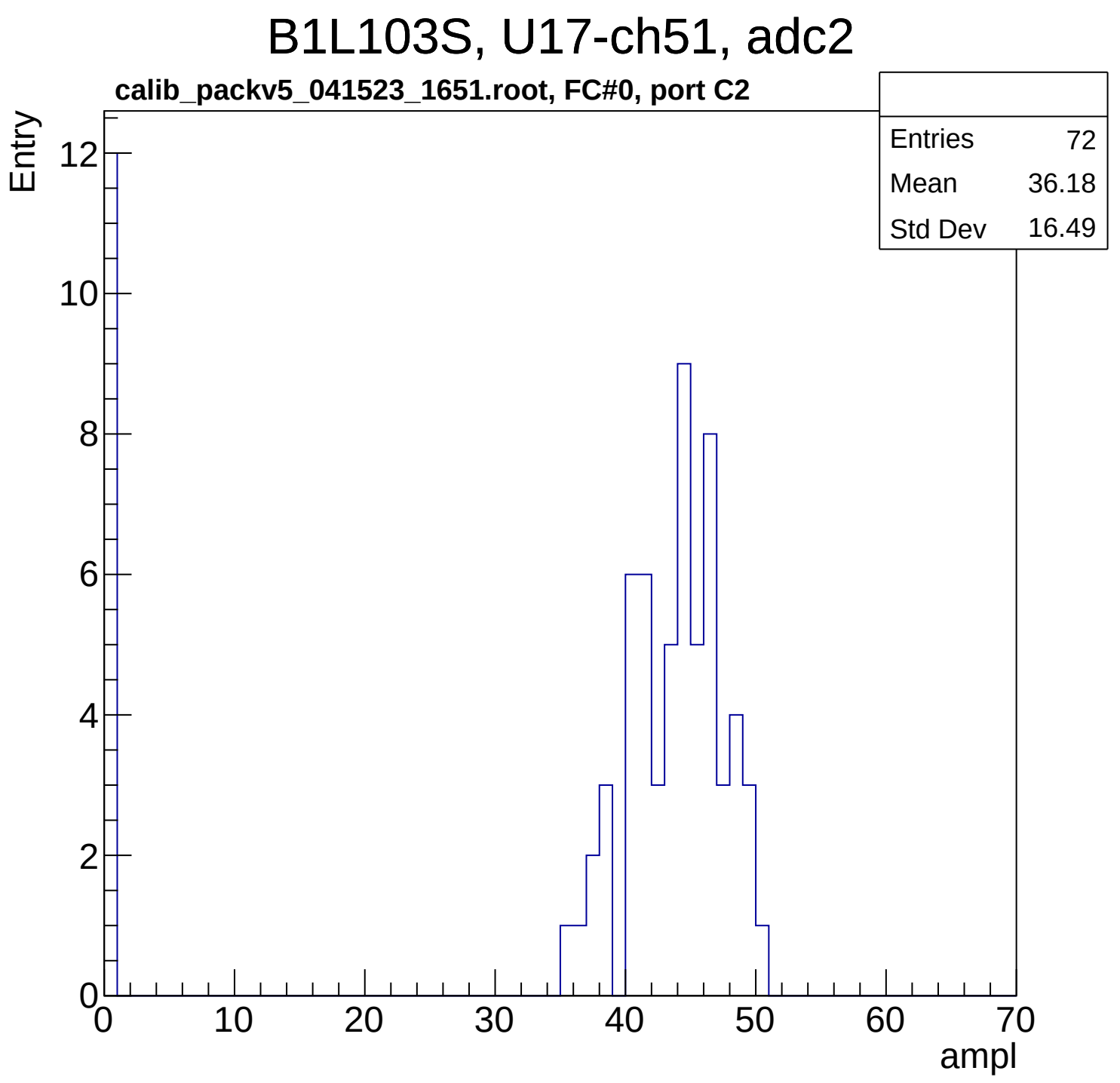
40
50
60
70


B1L103S, U17-ch51, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 36.18
Std Dev 16.49
Entry
0
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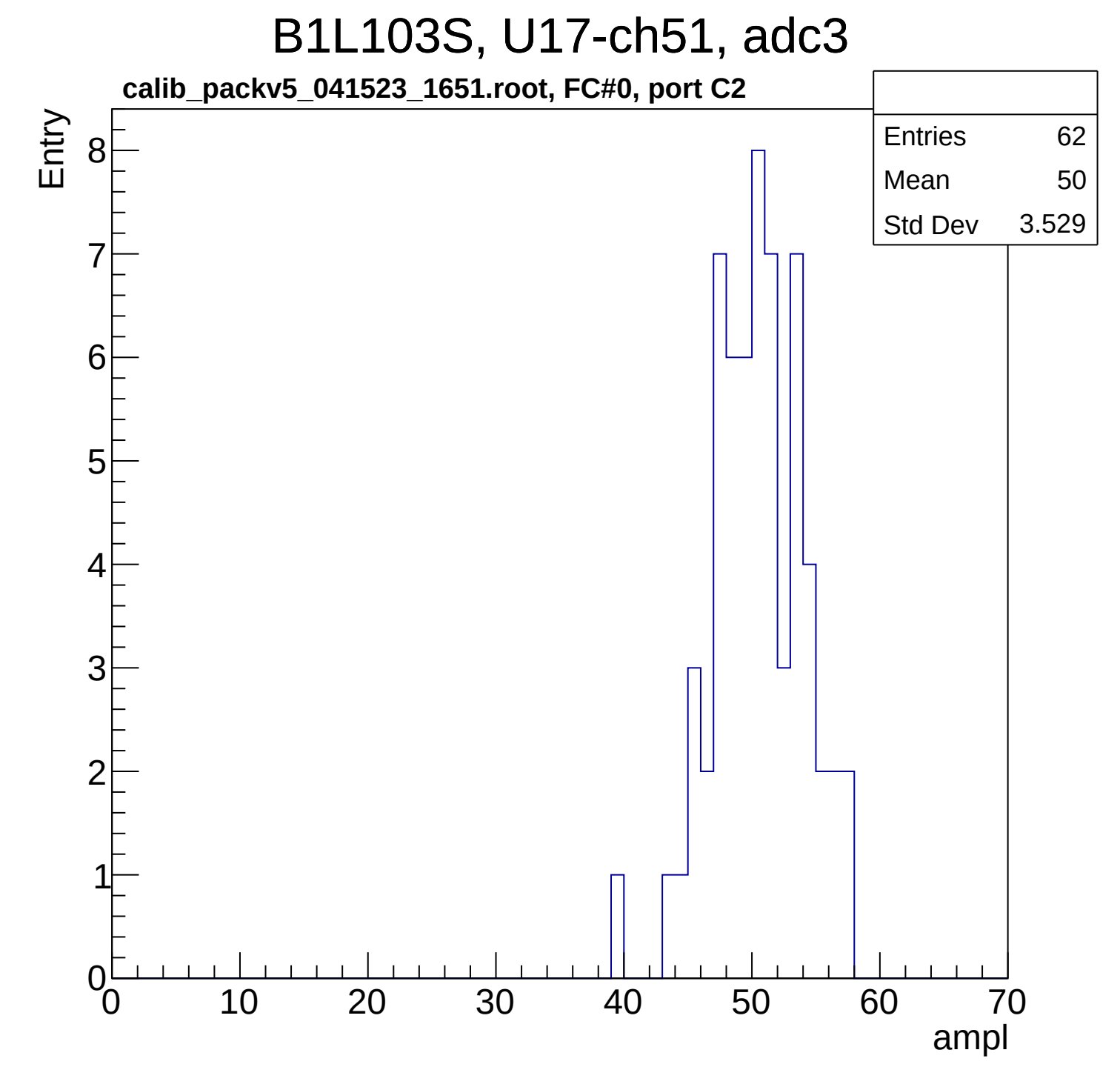
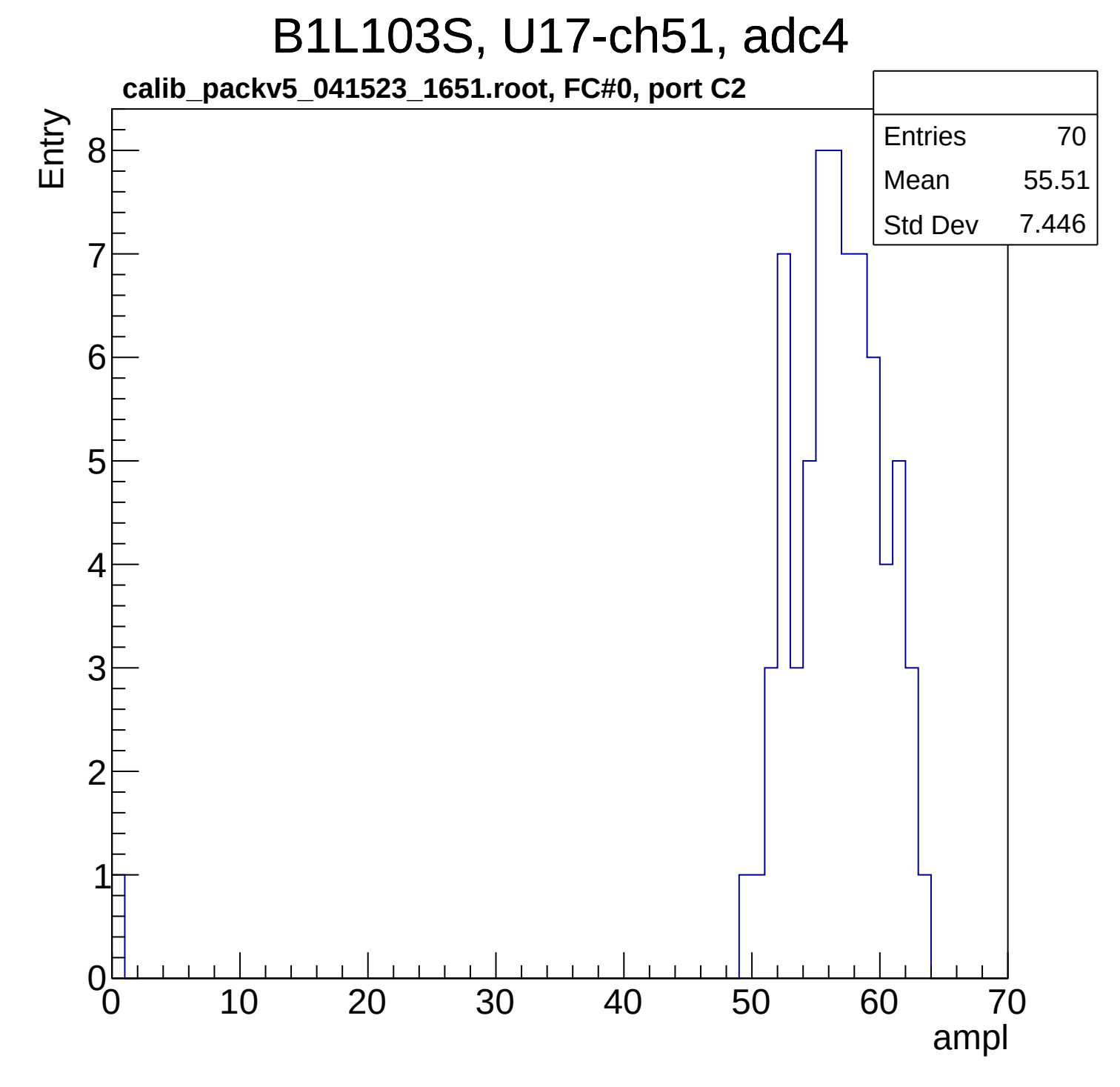
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch51, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 50
Std Dev 3.529
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U17-ch51, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 55.51
Std Dev 7.446
Entry
ampl
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1
2
3
4
5
6
7
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0
10
20
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40
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60
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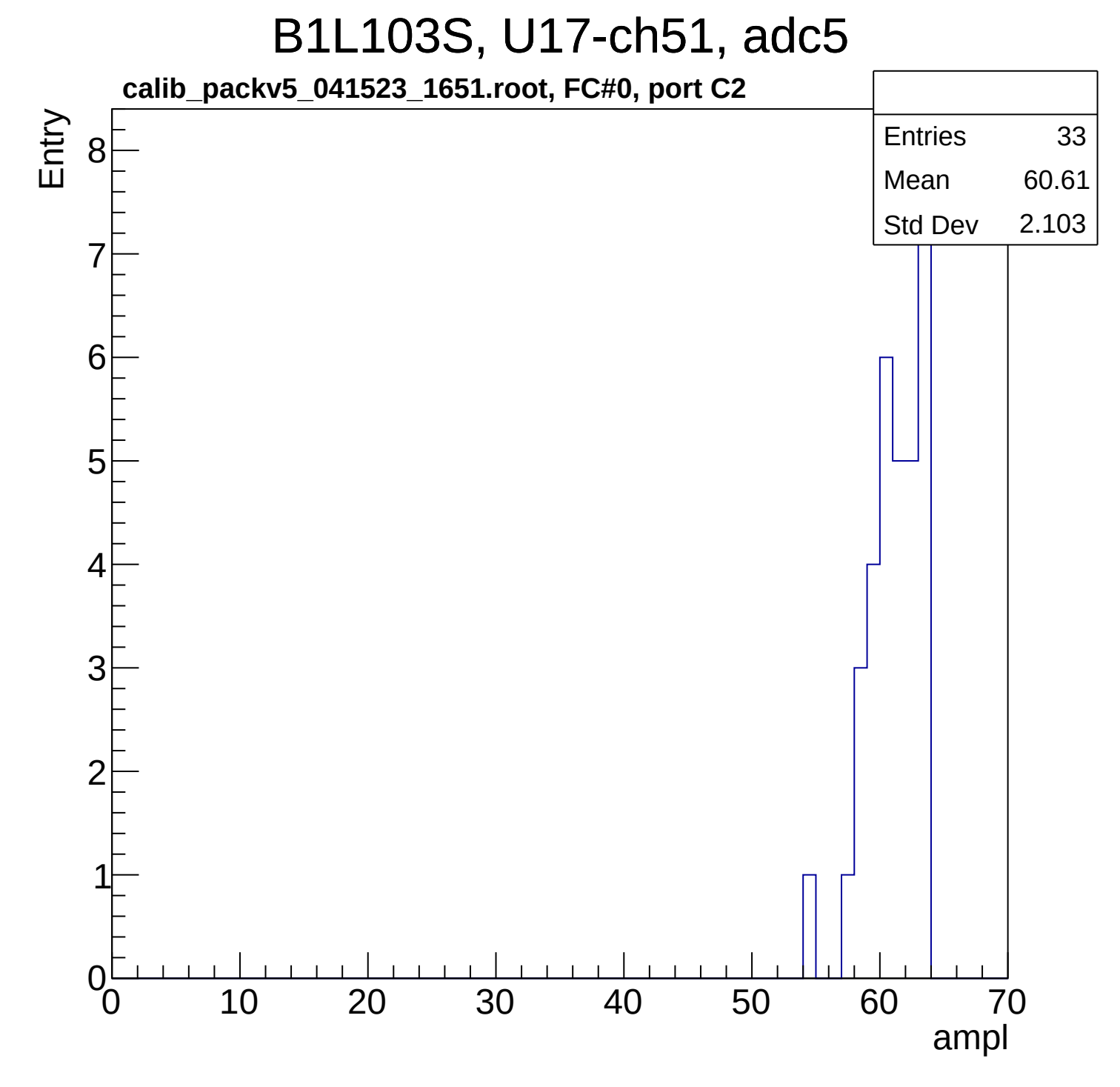
B1L103S, U17-ch51, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 33
Mean 60.61
Std Dev 2.103
Entry
ampl
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4
5
6
7
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0
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40
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60
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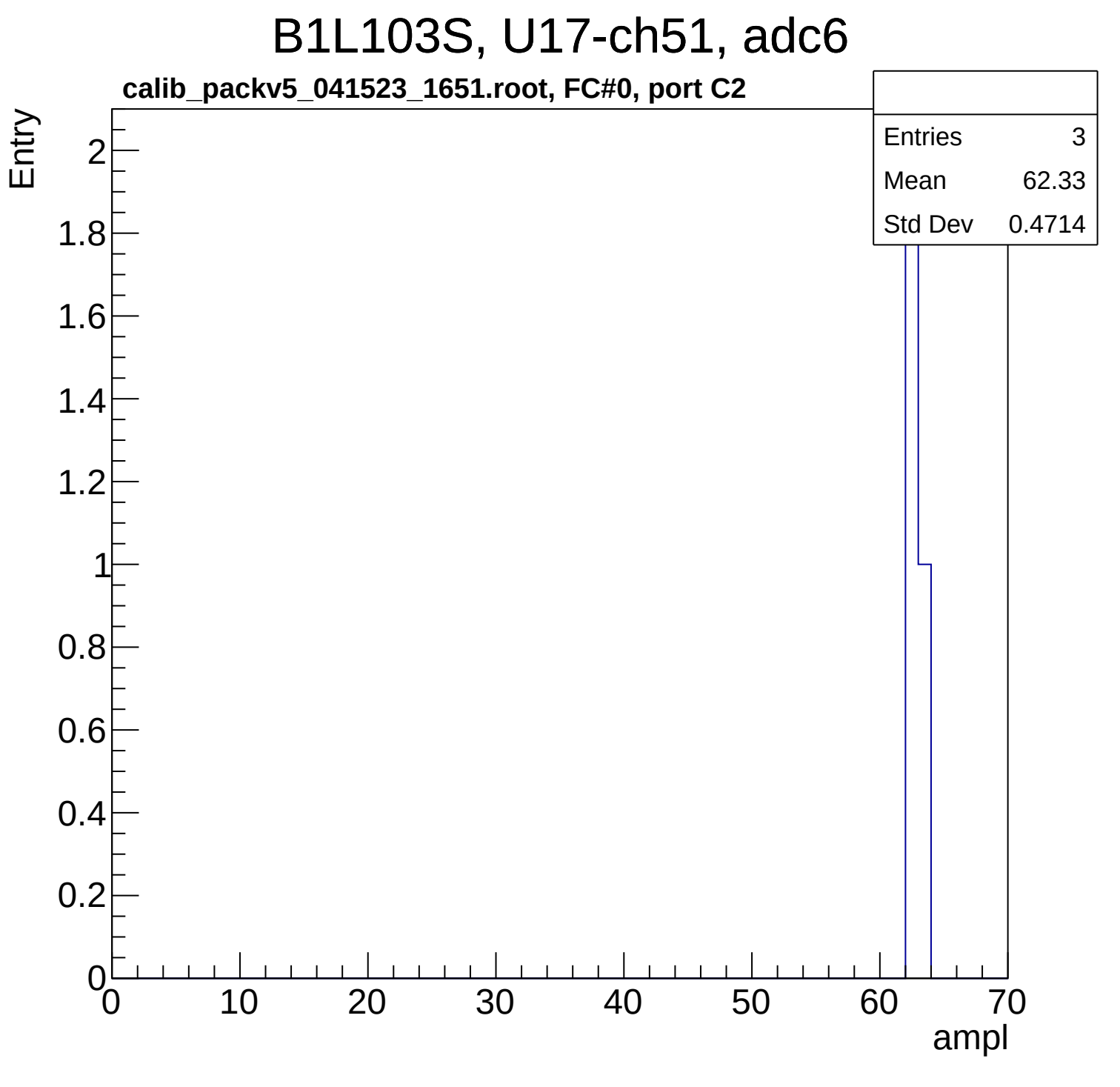
B1L103S, U17-ch51, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 3
Mean 62.33
Std Dev 0.4714
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
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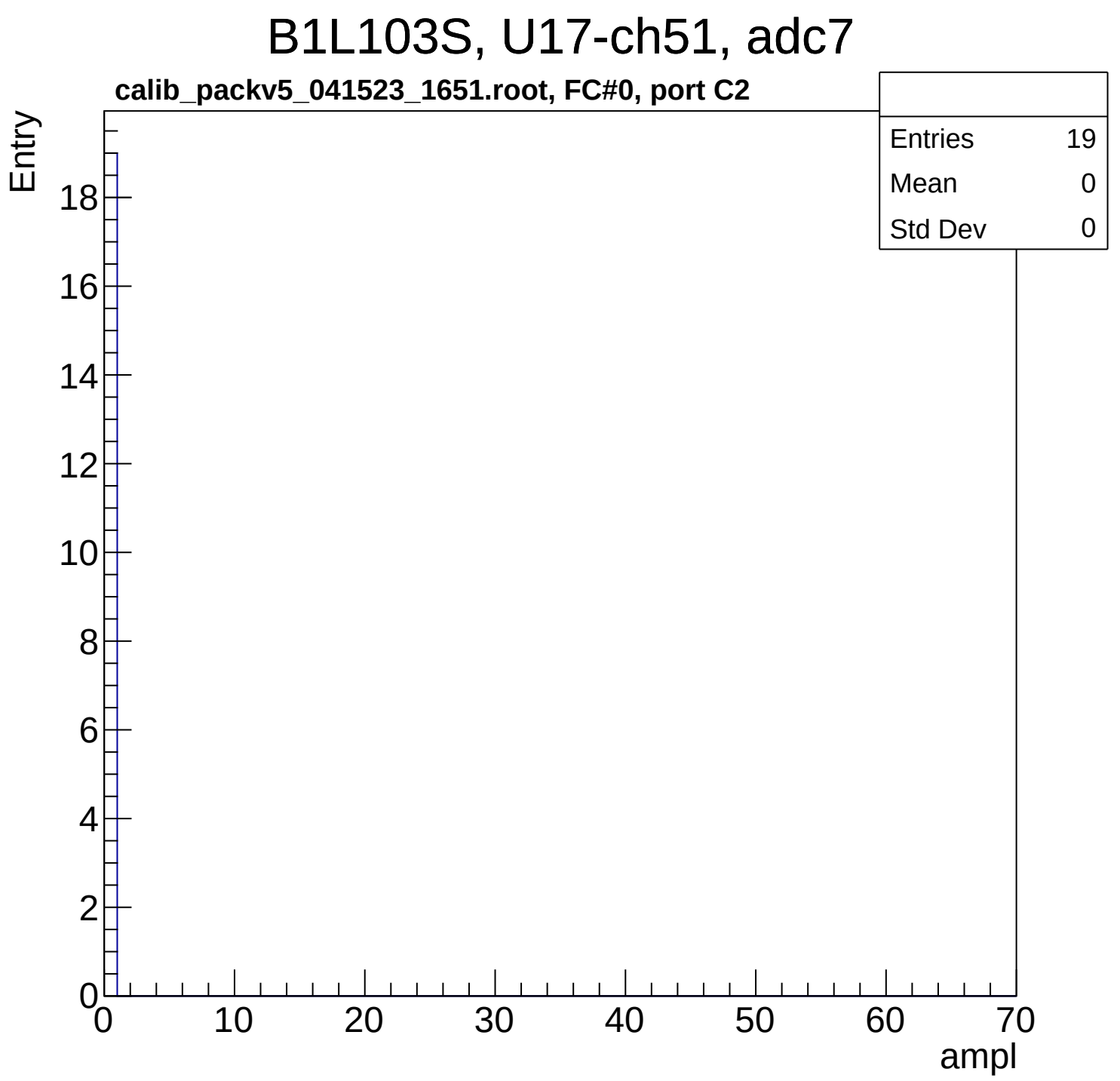
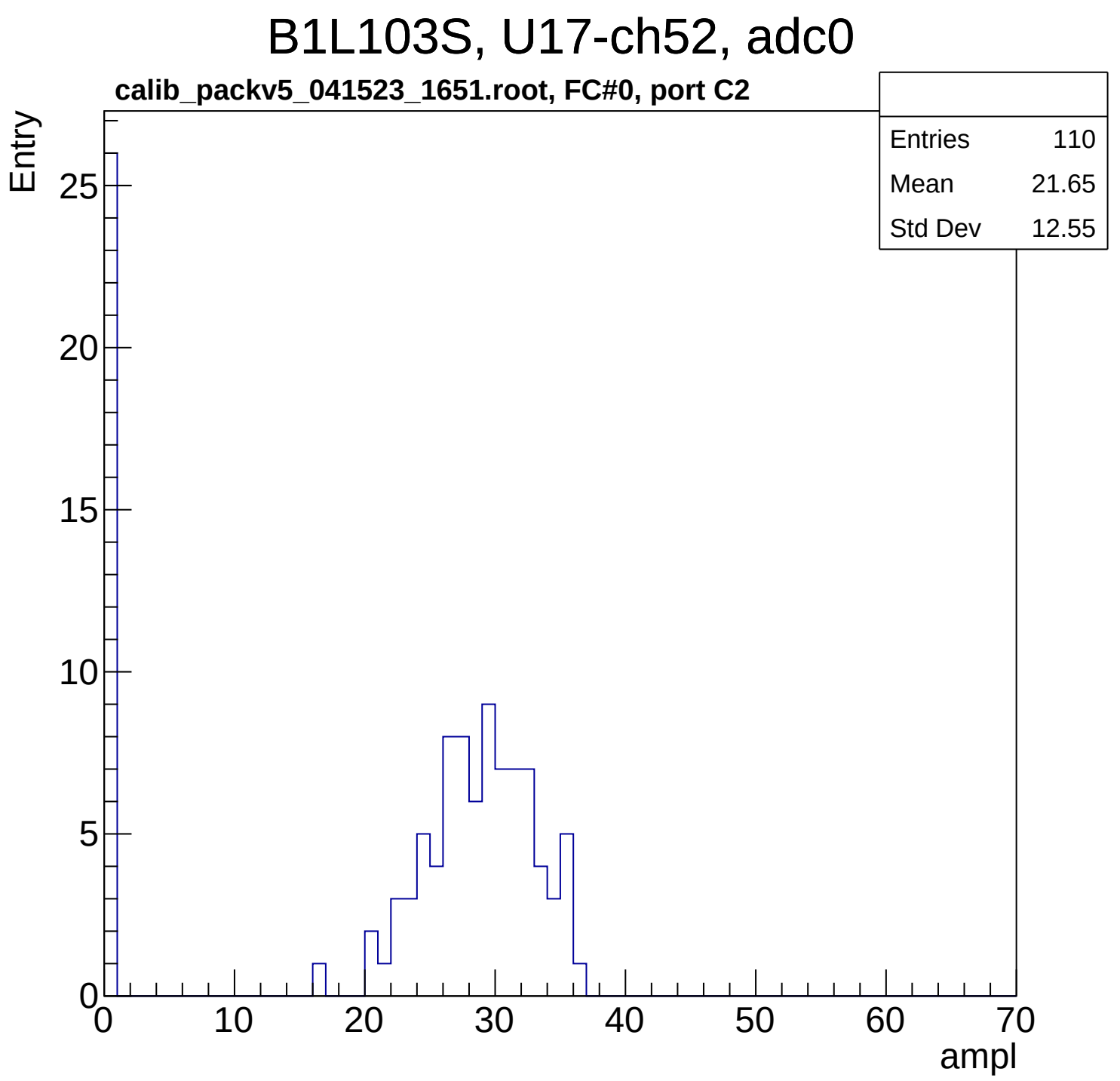
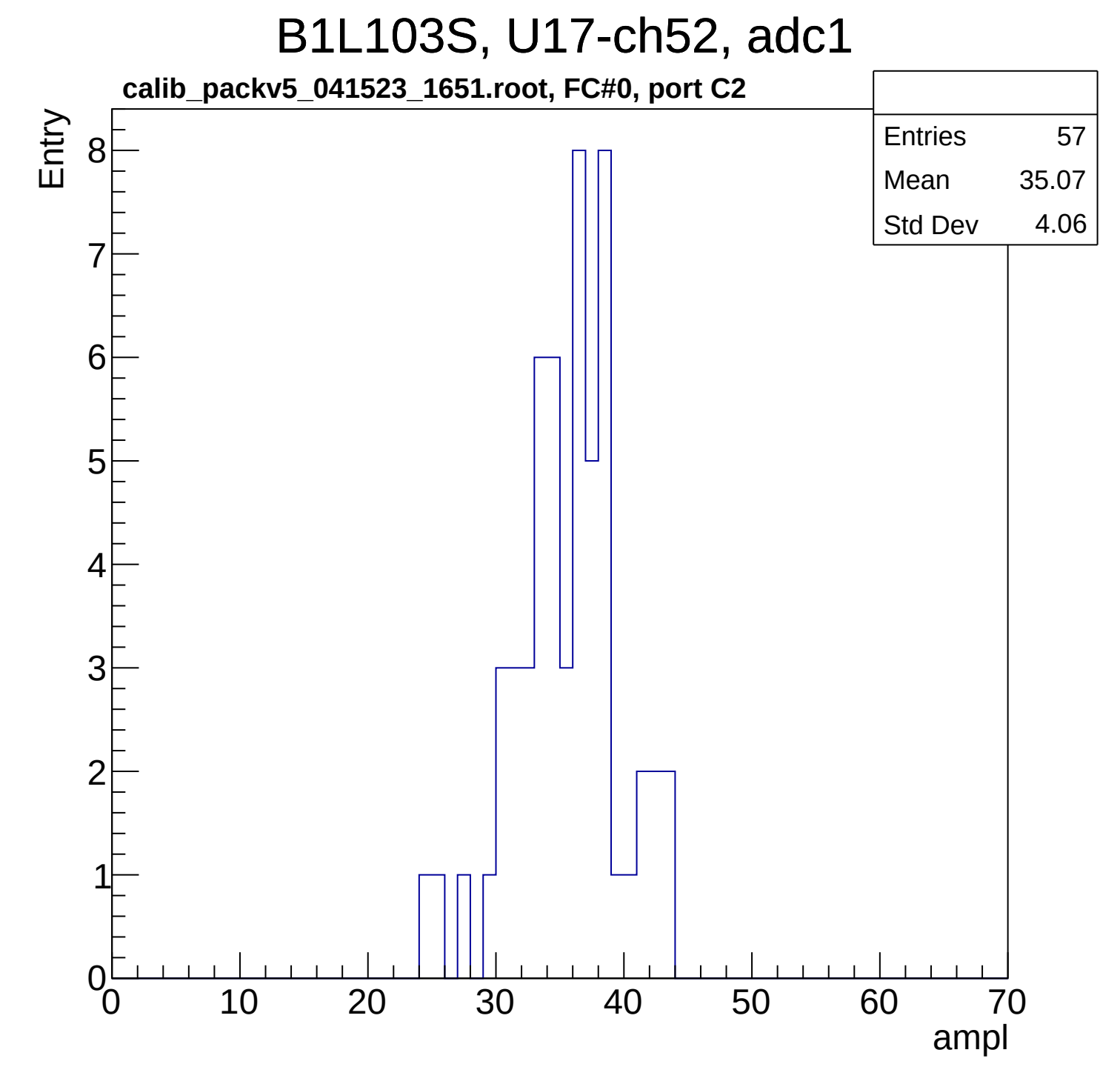

B1L103S, U17-ch51, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch52, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 110
Mean 21.65
Std Dev 12.55
Entry
0
5
10
15
20
25
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch52, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 35.07
Std Dev 4.06
Entry
ampl
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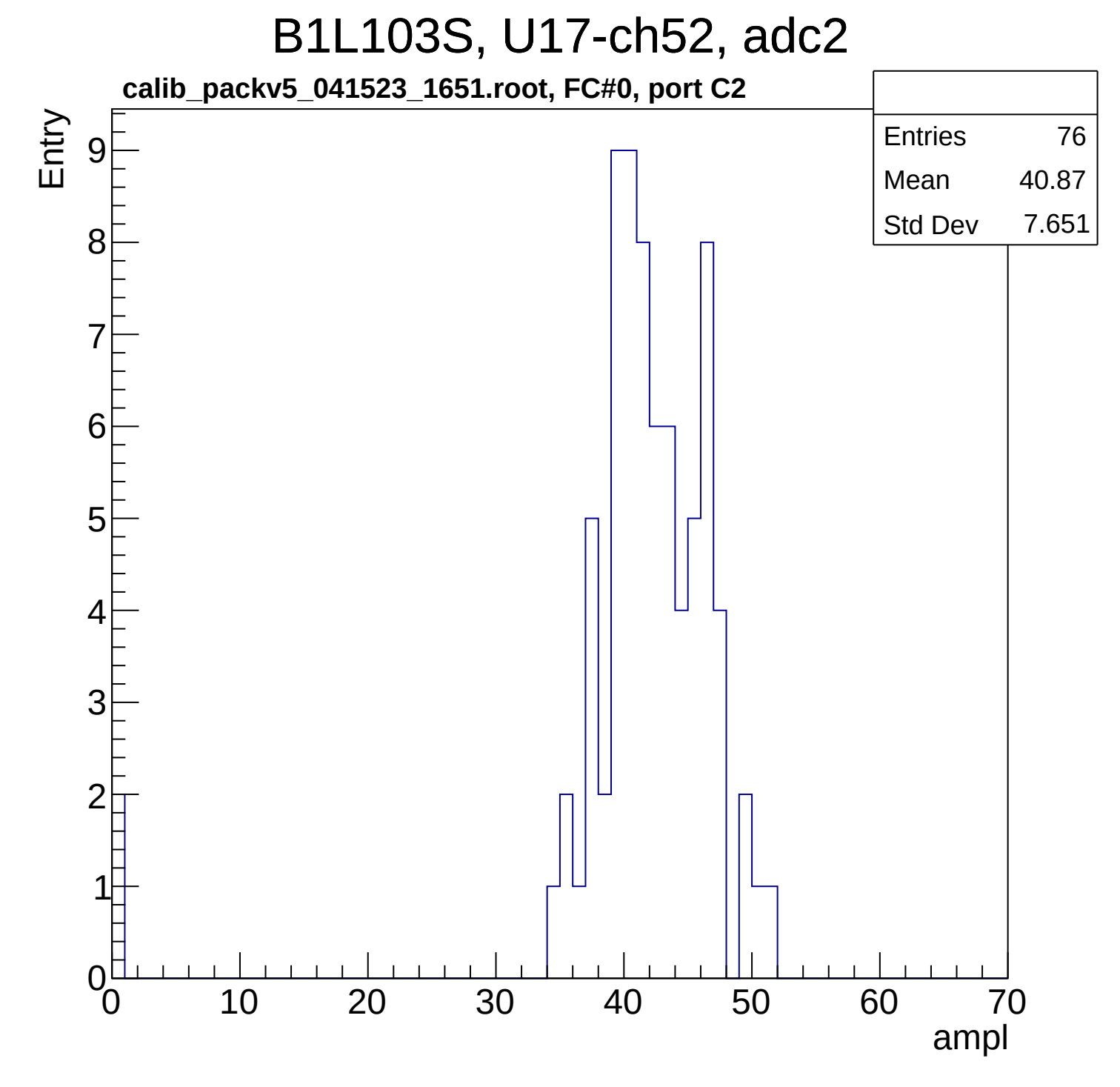
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U17-ch52, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 40.87
Std Dev 7.651
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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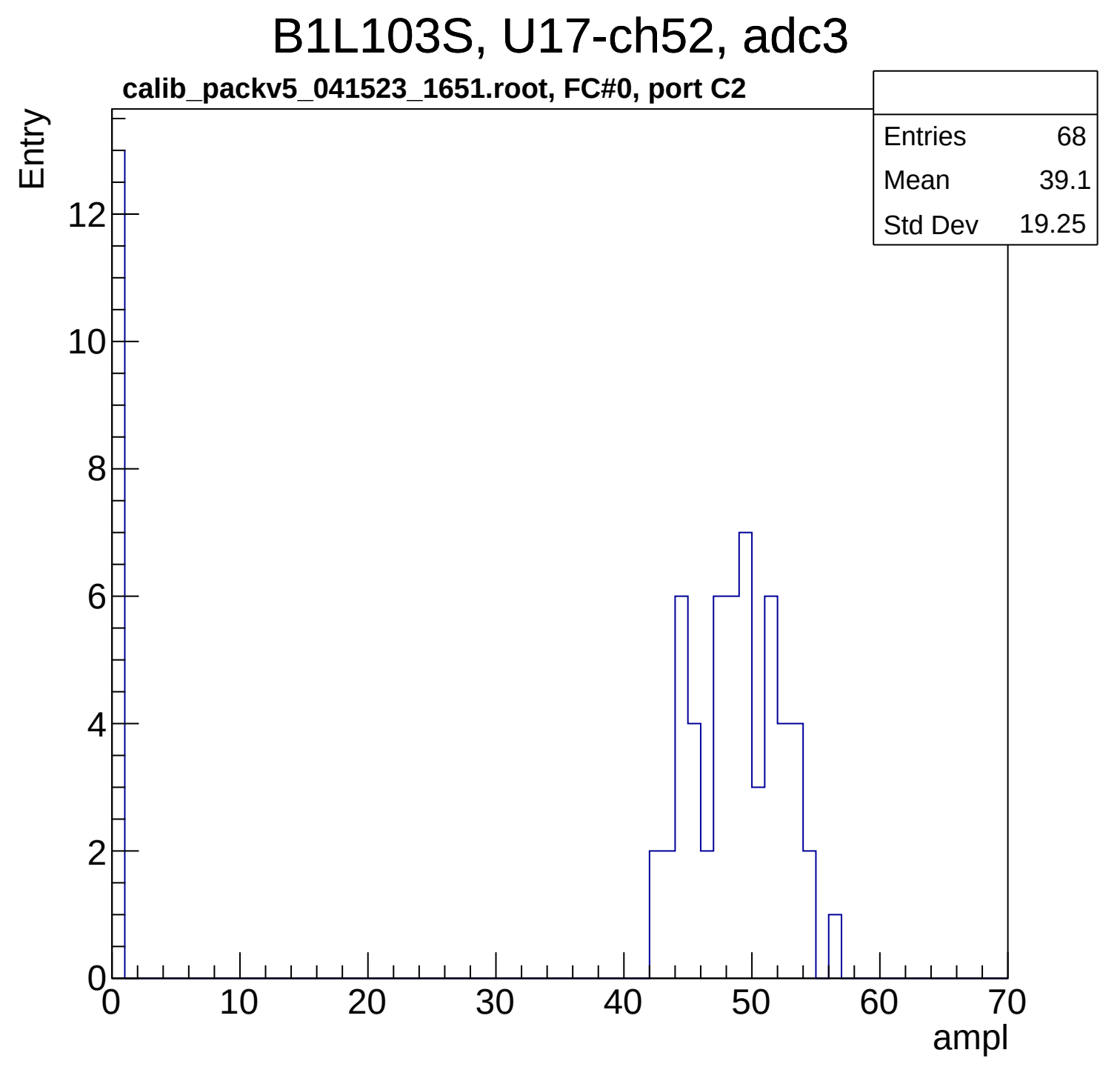
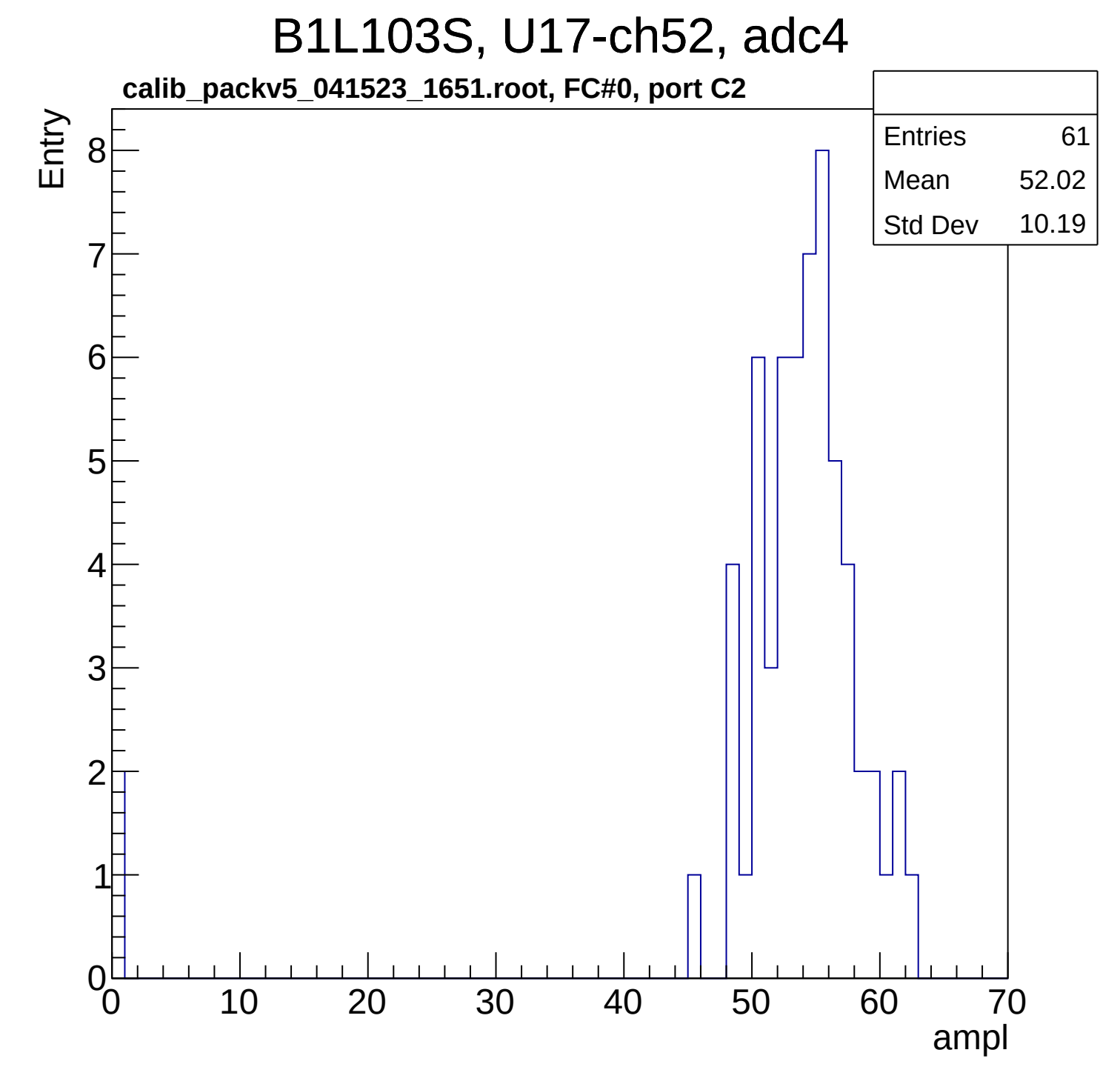

B1L103S, U17-ch52, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 39.1
Std Dev 19.25
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch52, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 52.02
Std Dev 10.19
Entry
ampl
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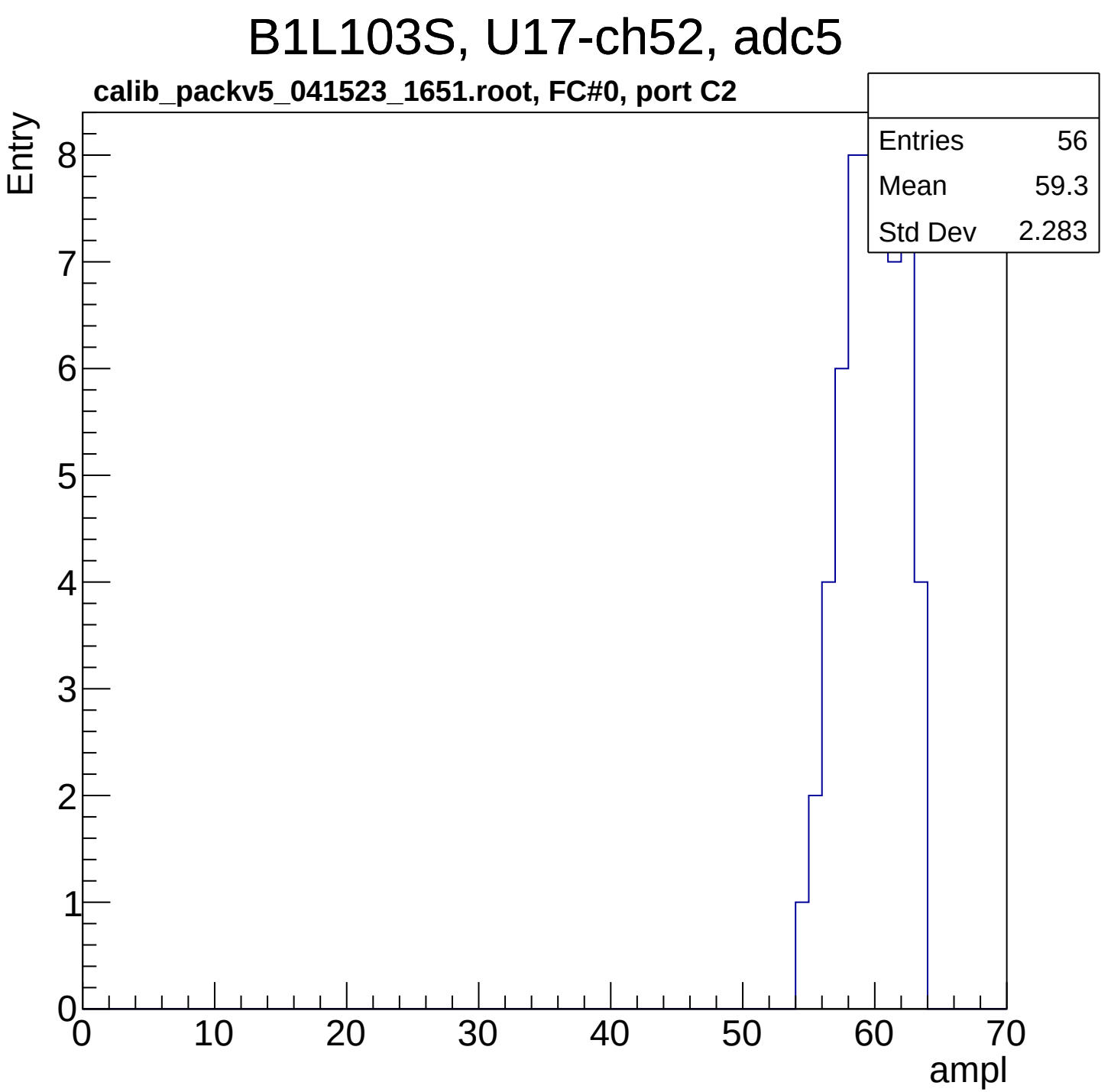
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U17-ch52, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 59.3
Std Dev 2.283
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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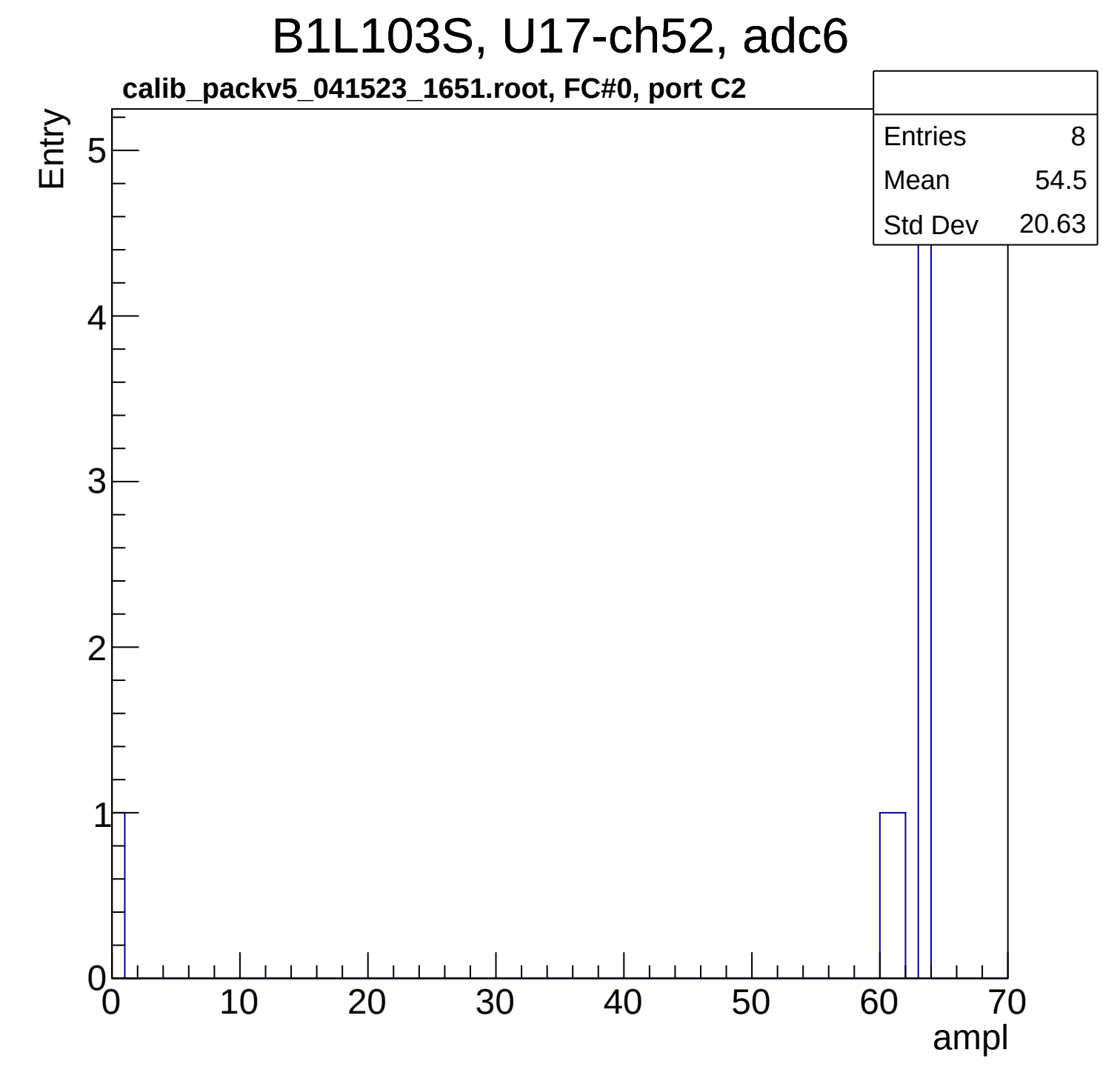
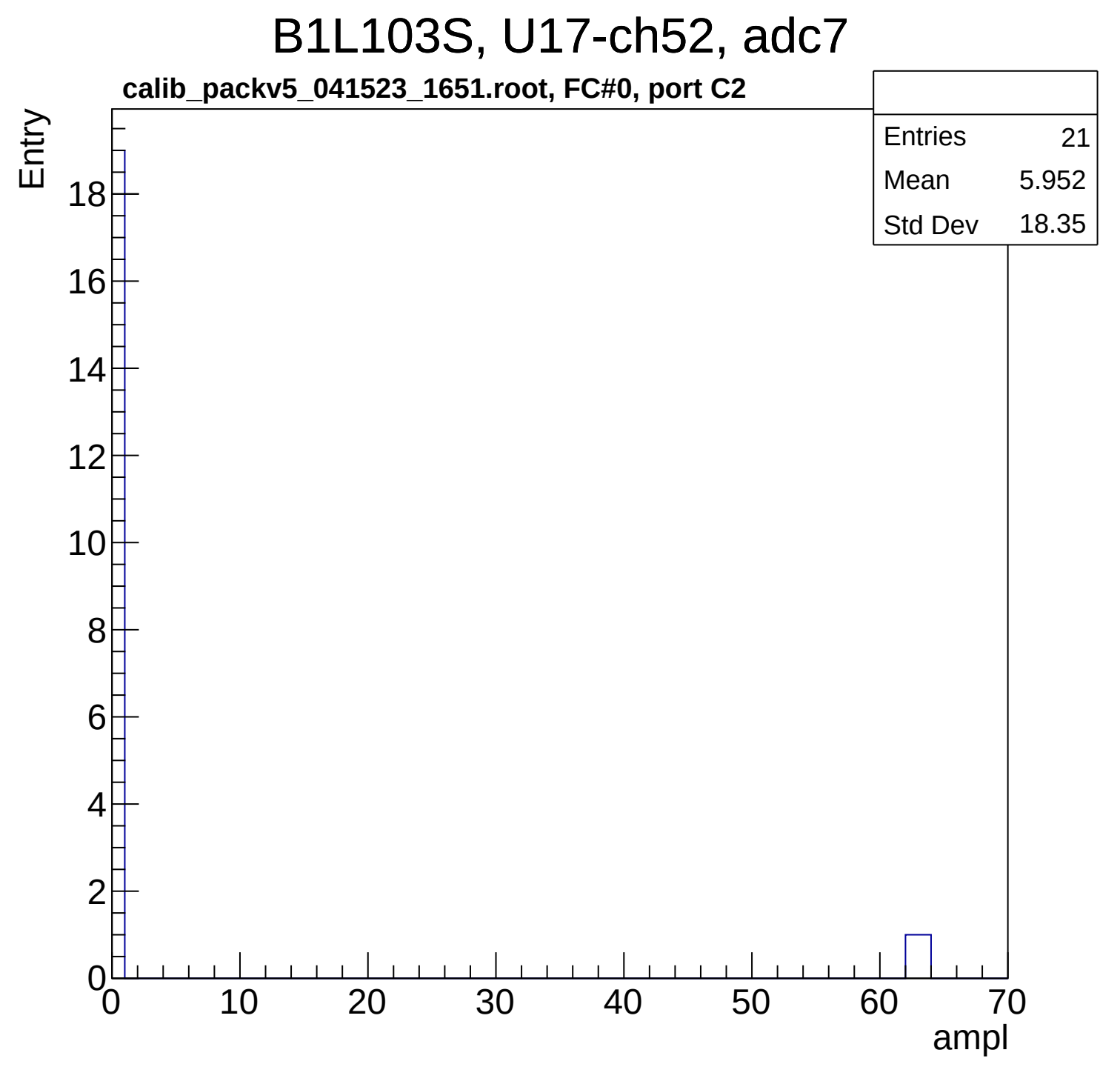

B1L103S, U17-ch52, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 54.5
Std Dev 20.63
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U17-ch52, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 5.952
Std Dev 18.35
Entry
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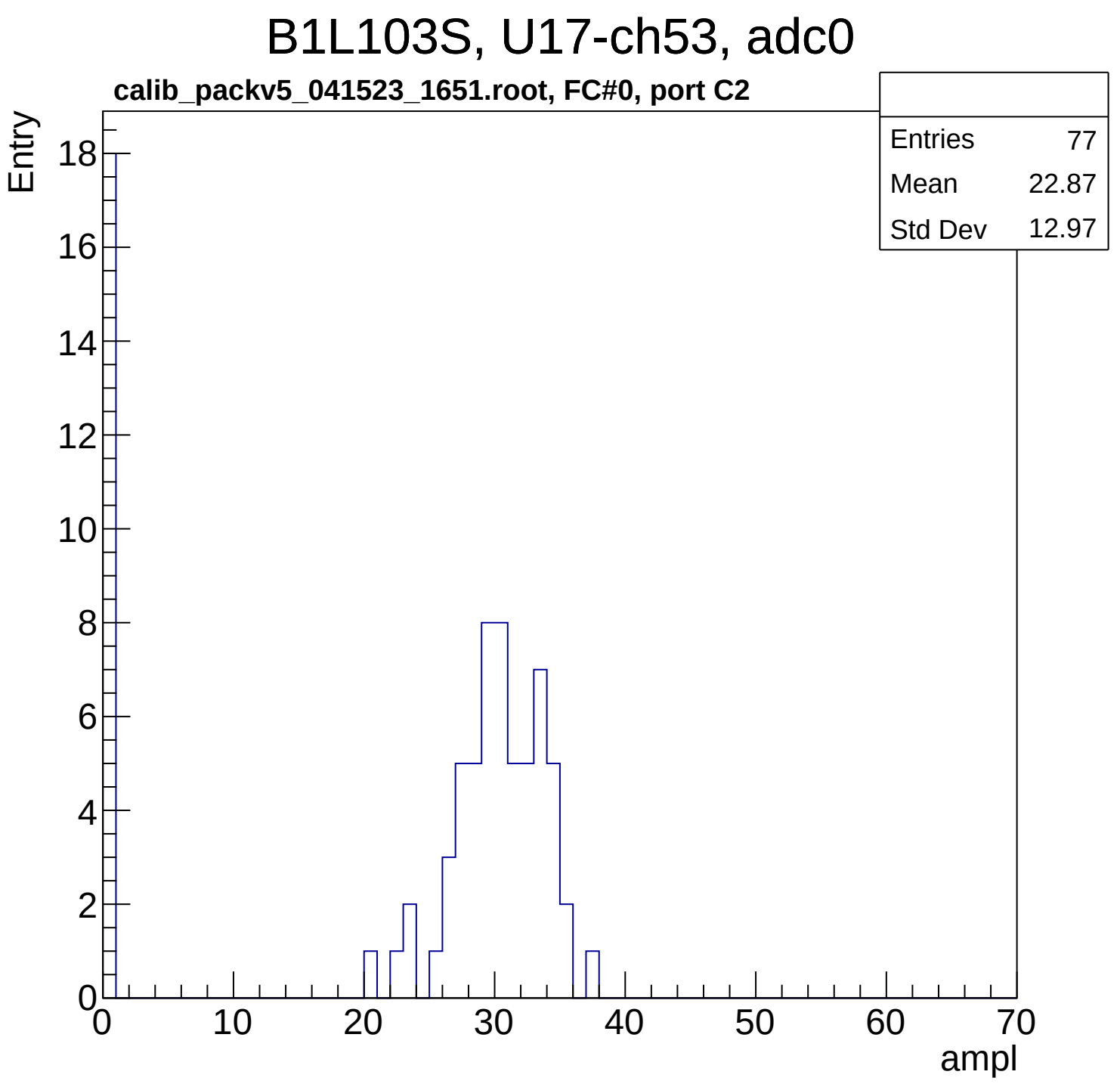
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch53, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 22.87
Std Dev 12.97
Entry
0
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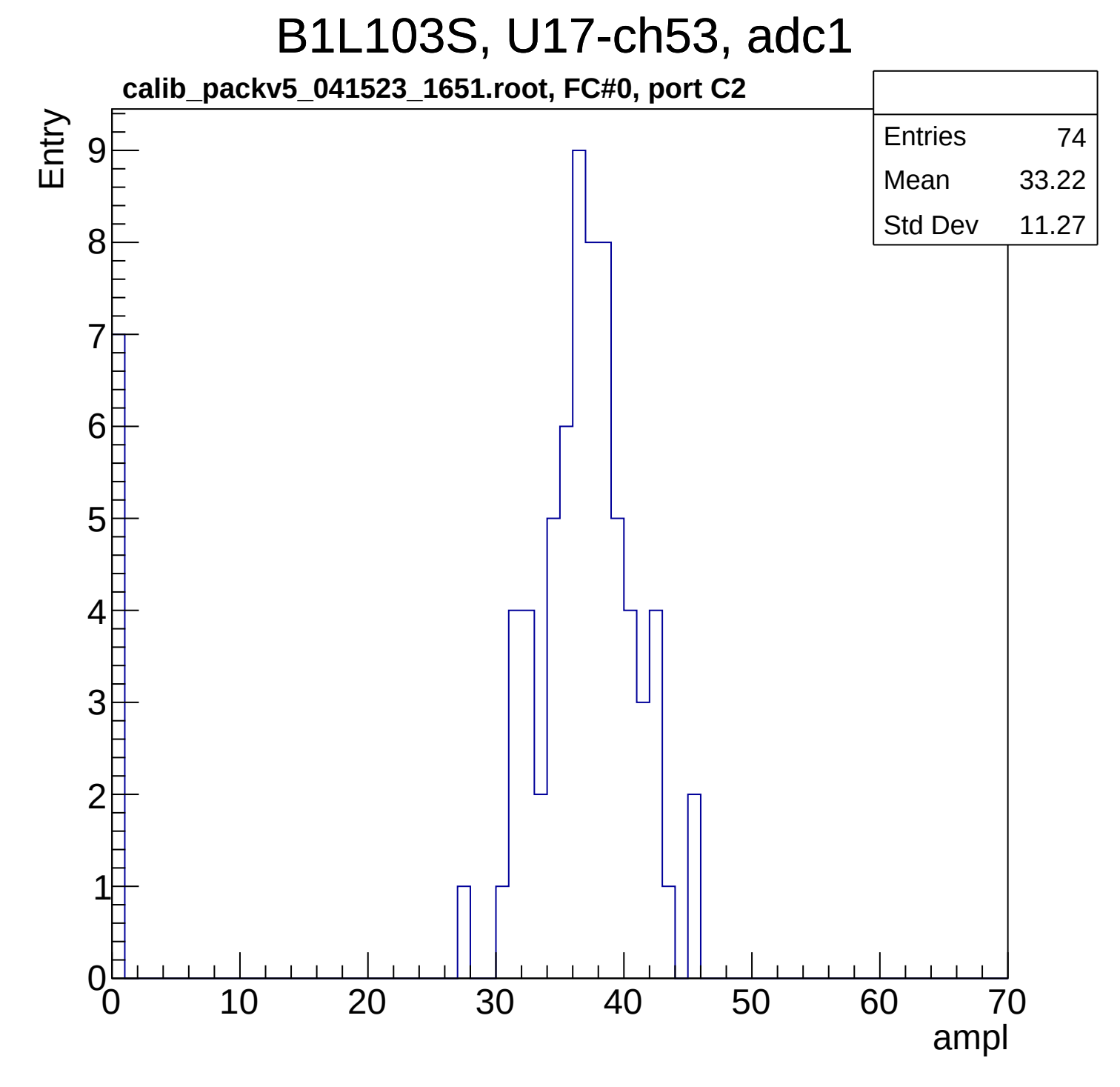
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch53, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 33.22
Std Dev 11.27
Entry
ampl
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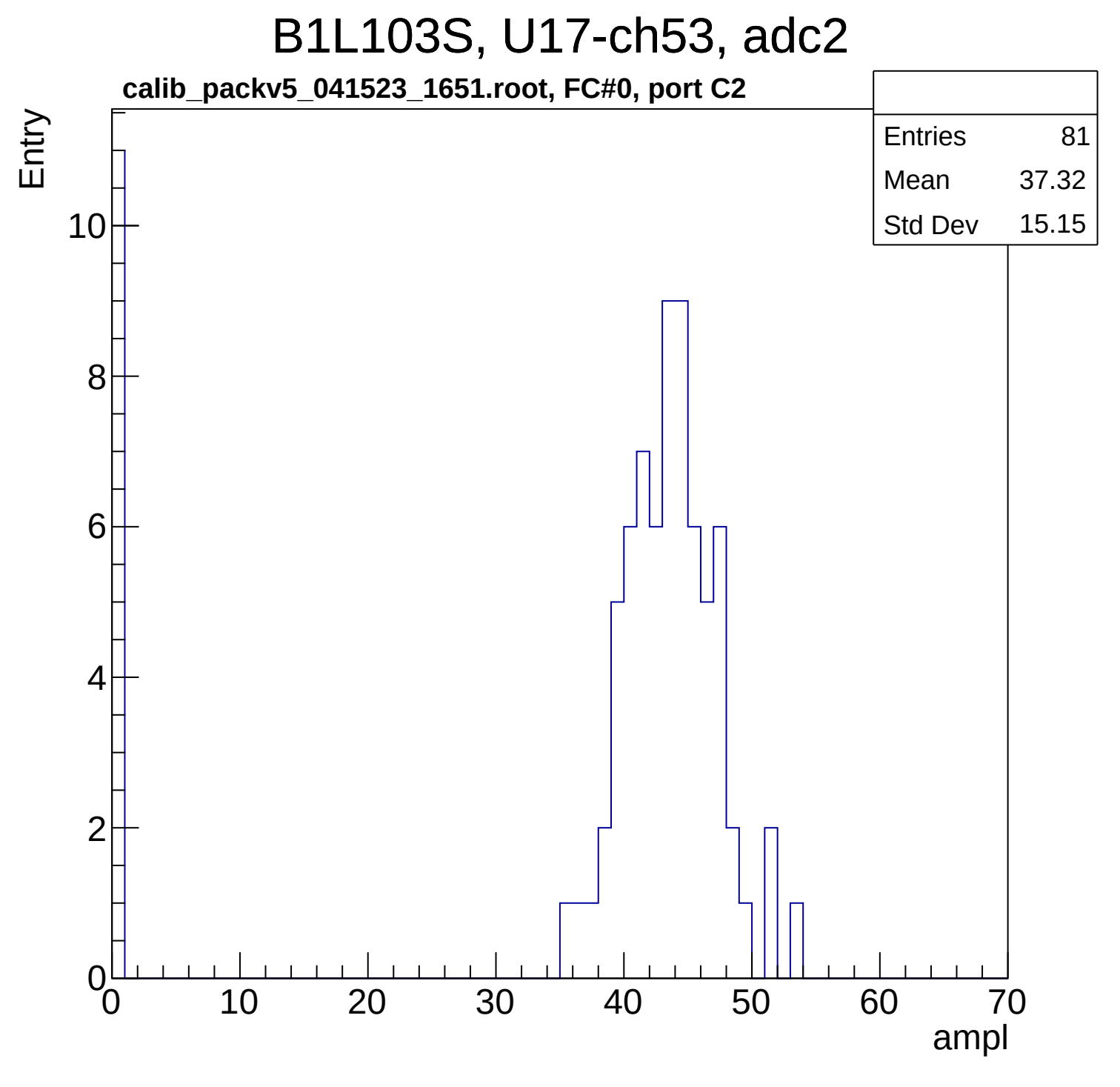
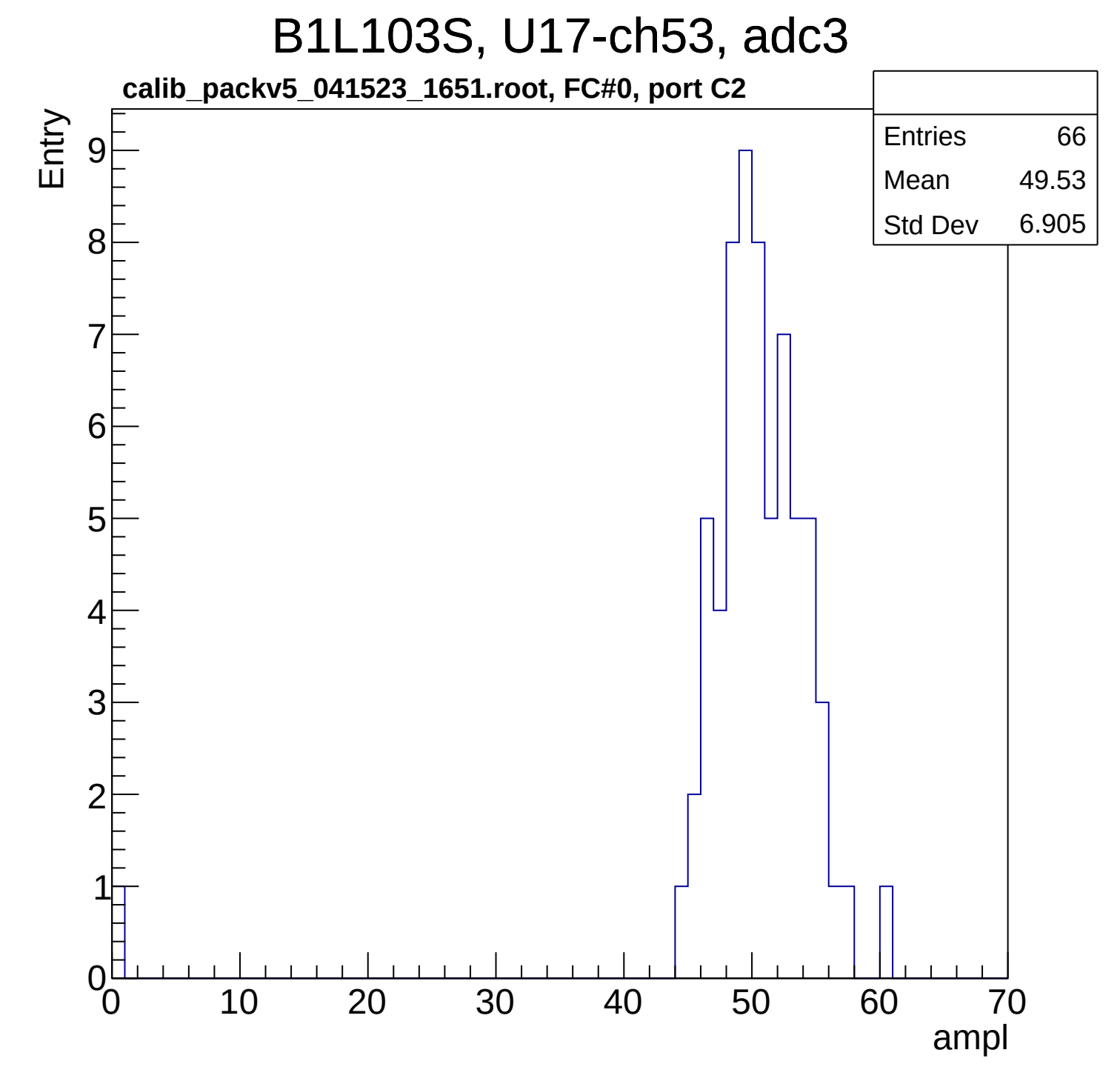
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U17-ch53, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 37.32
Std Dev 15.15
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch53, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 49.53
Std Dev 6.905
Entry
ampl
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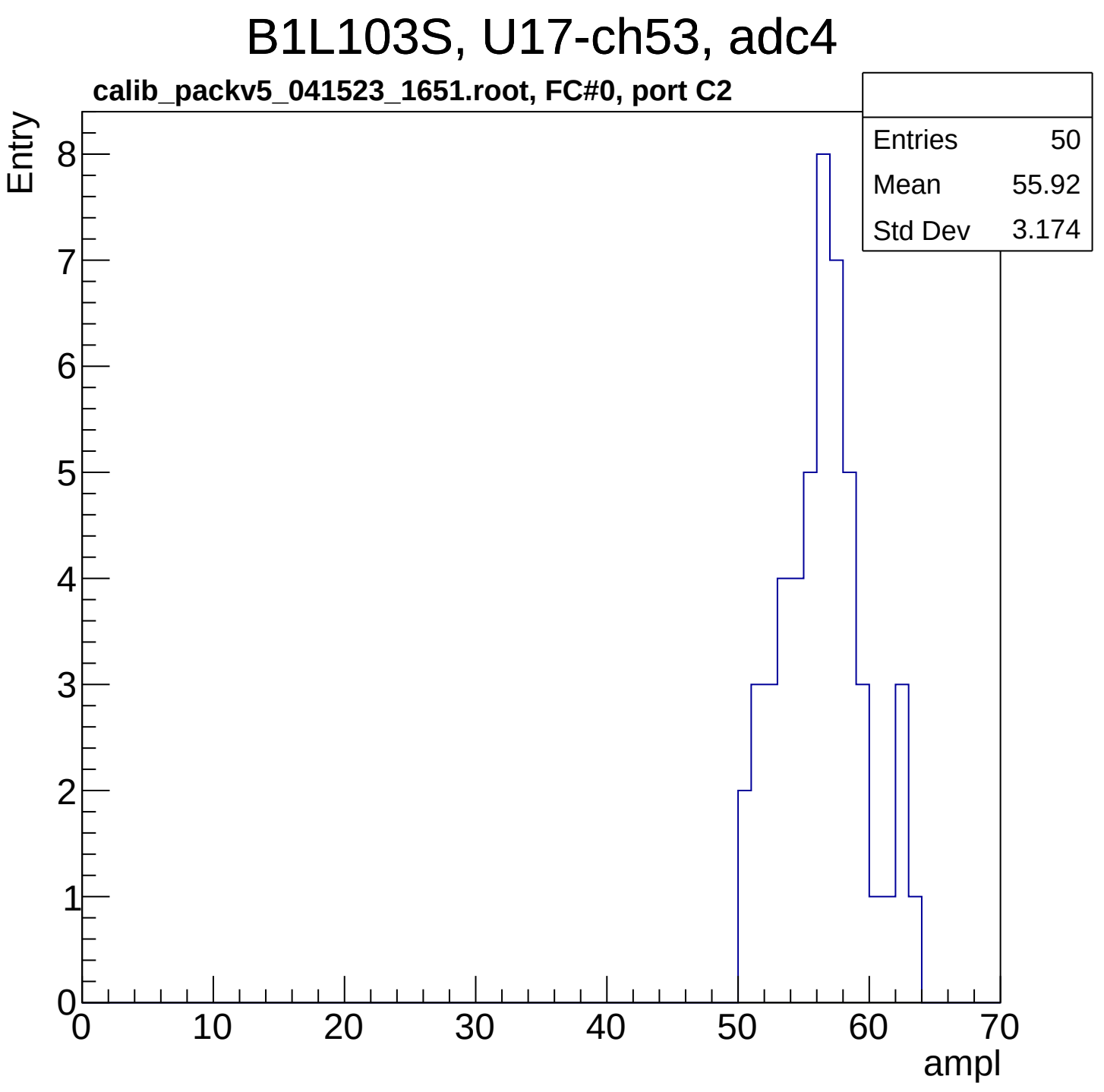
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U17-ch53, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 55.92
Std Dev 3.174
Entry
ampl
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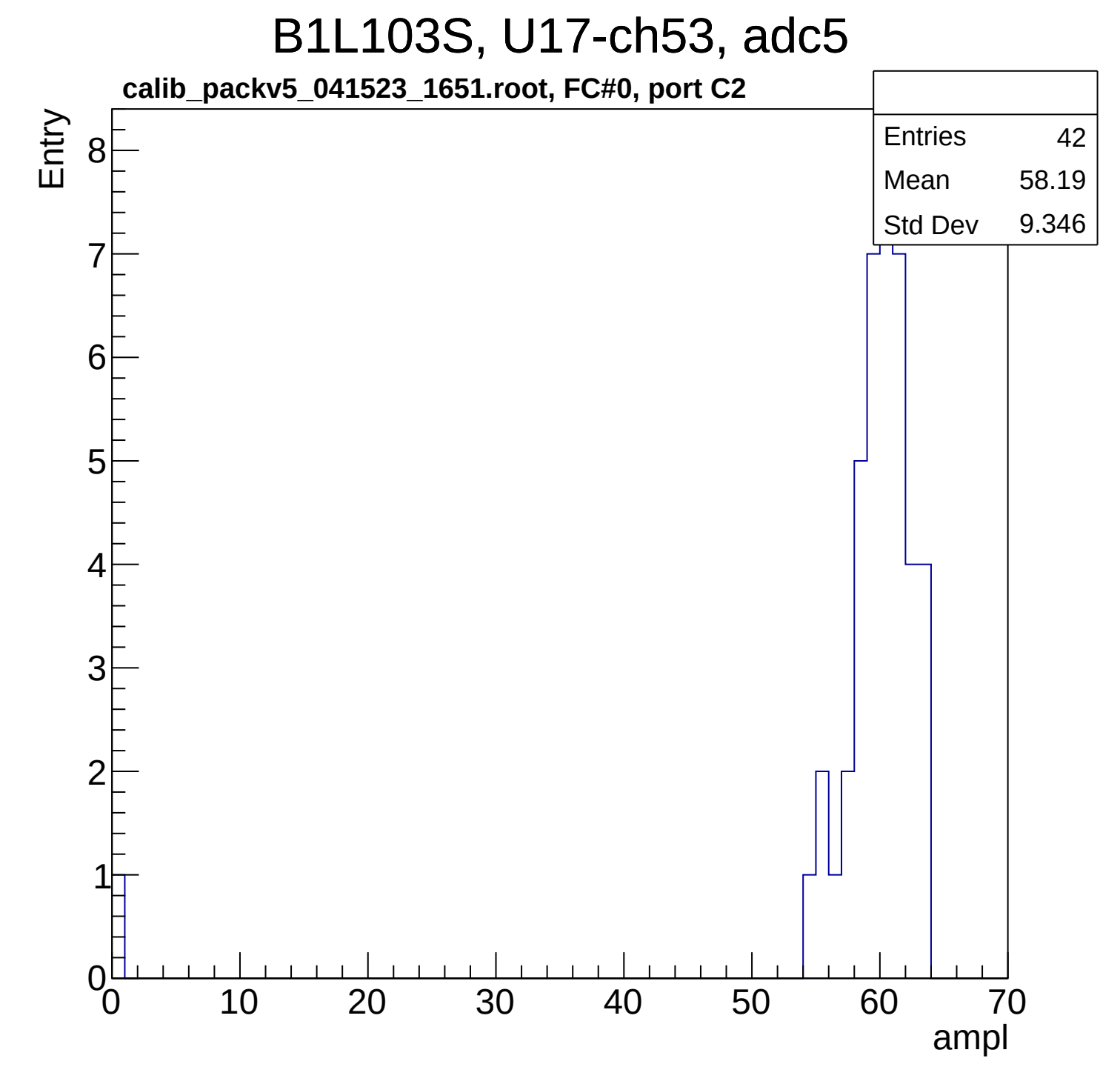
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U17-ch53, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 42
Mean 58.19
Std Dev 9.346
Entry
ampl
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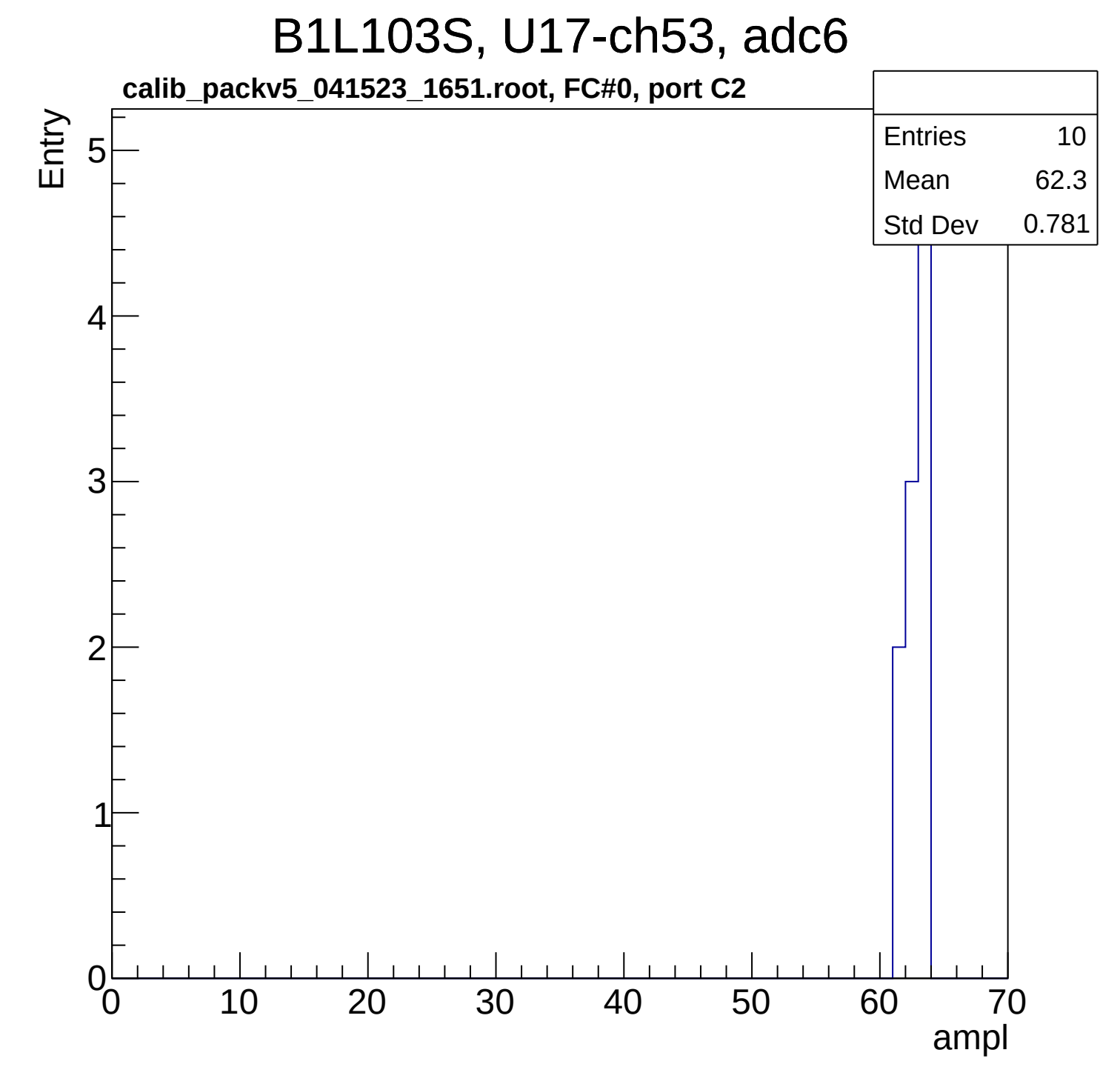
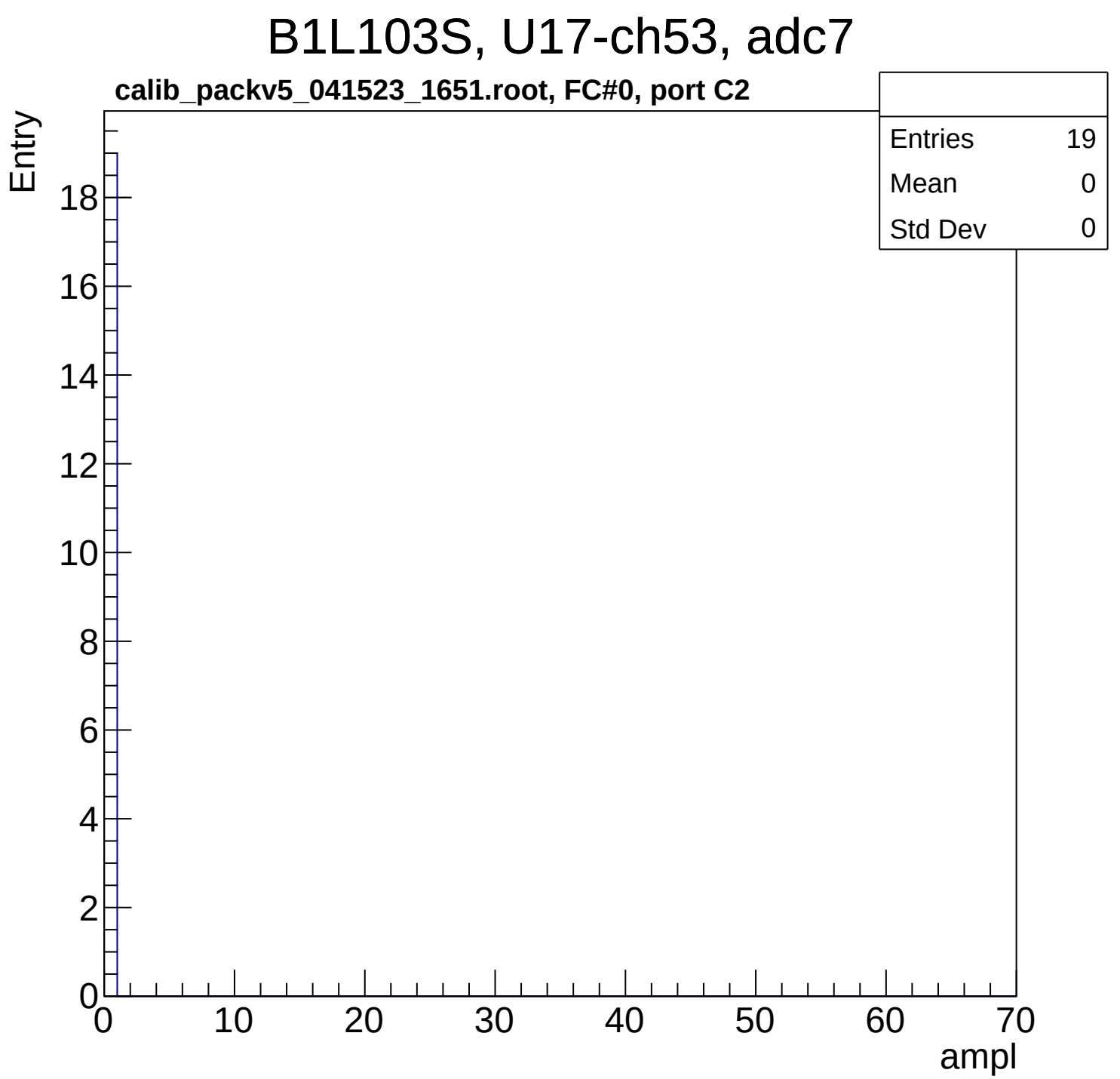
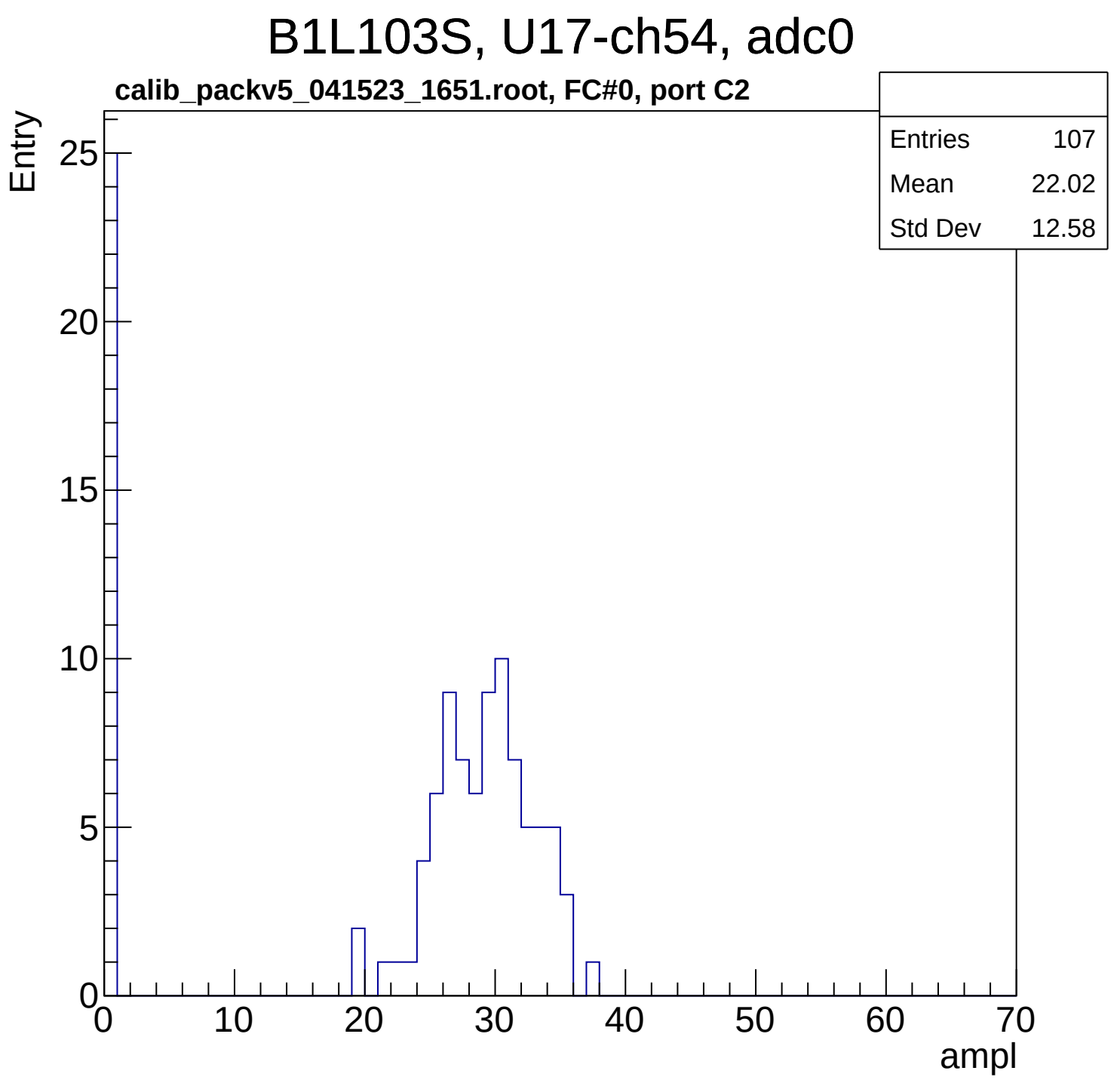
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U17-ch53, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 62.3
Std Dev 0.781
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U17-ch53, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch54, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 107
Mean 22.02
Std Dev 12.58
Entry
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10
15
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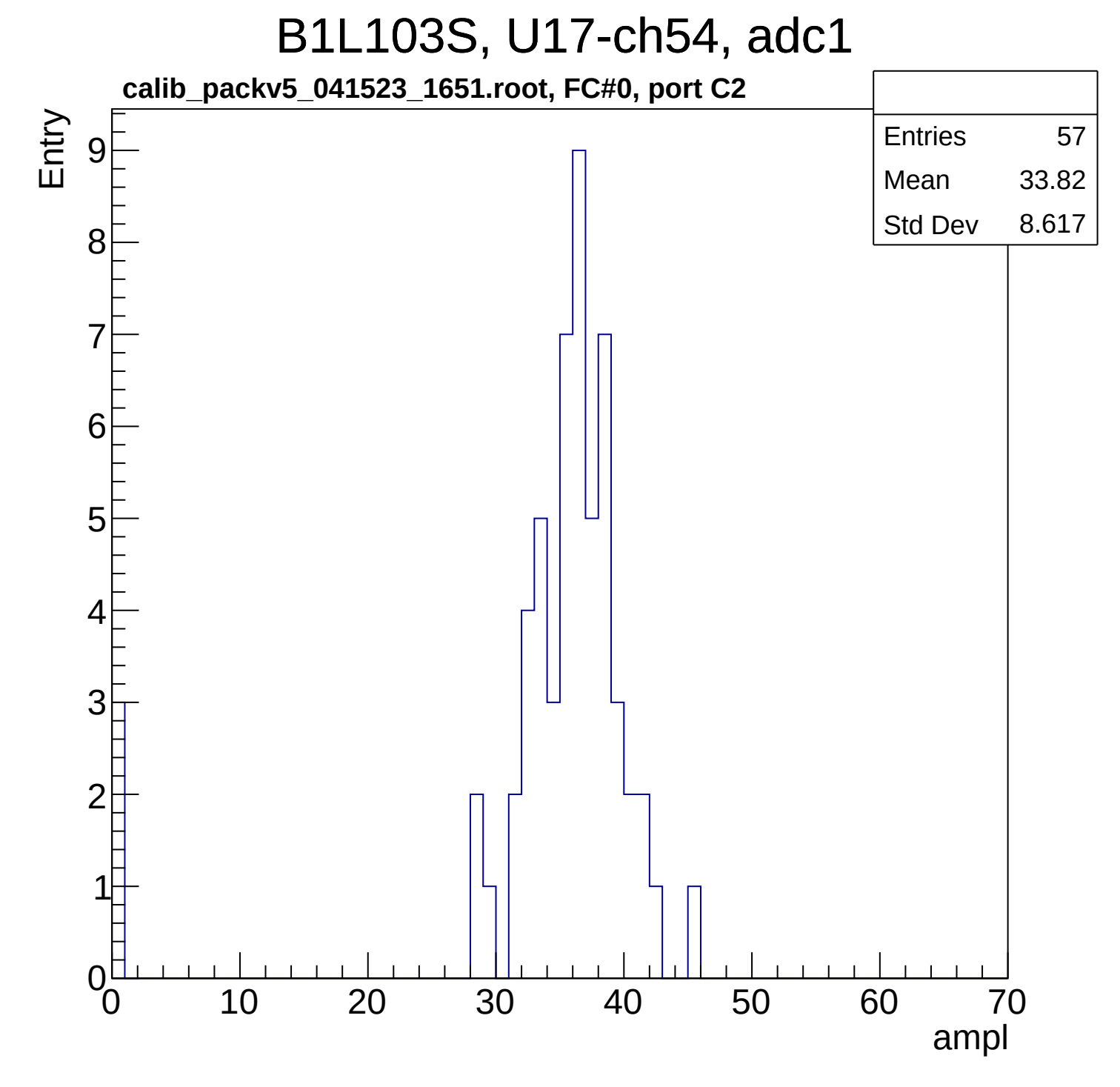
25
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch54, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 33.82
Std Dev 8.617
Entry
ampl
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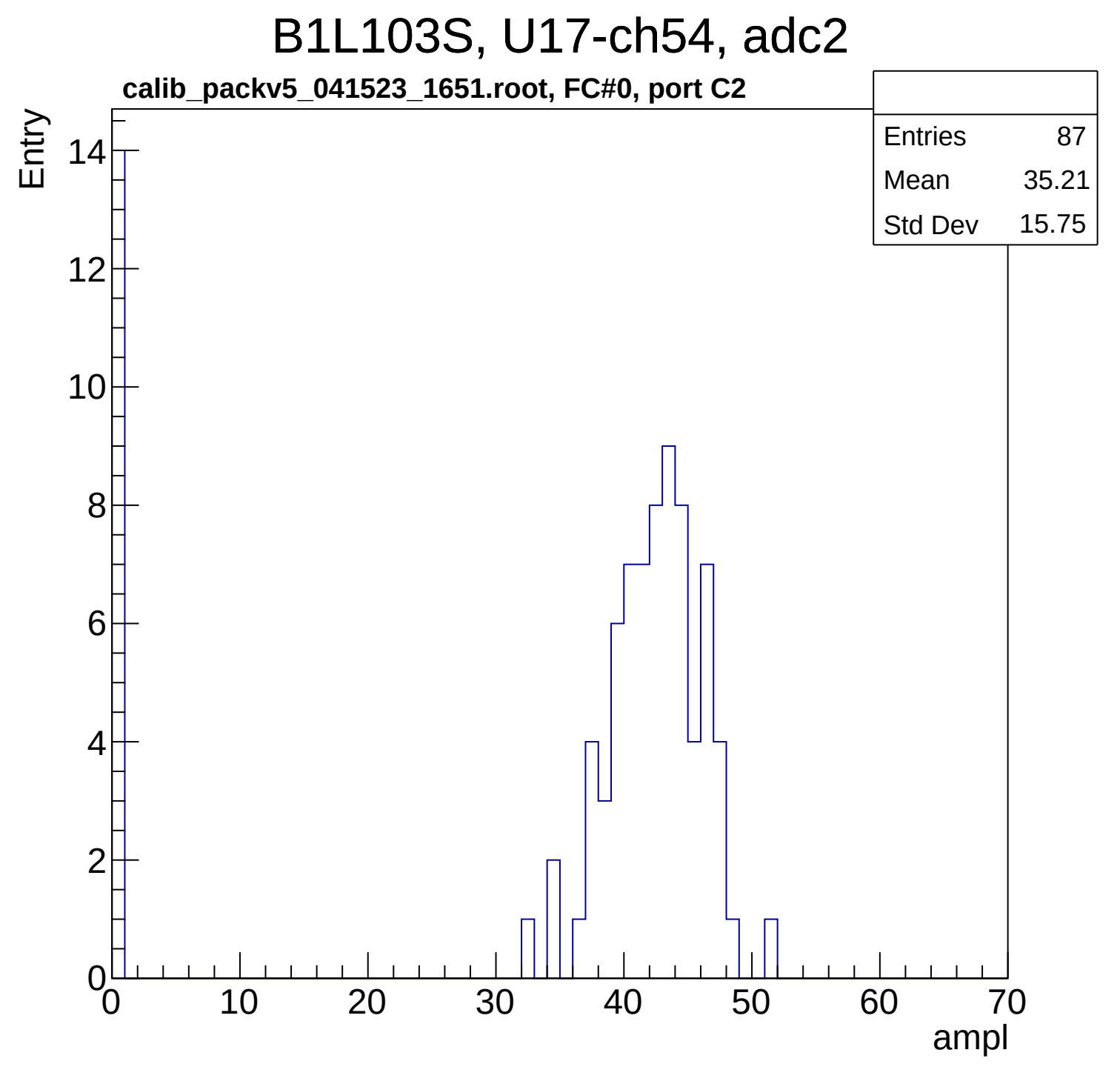
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U17-ch54, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 87
Mean 35.21
Std Dev 15.75
Entry
ampl
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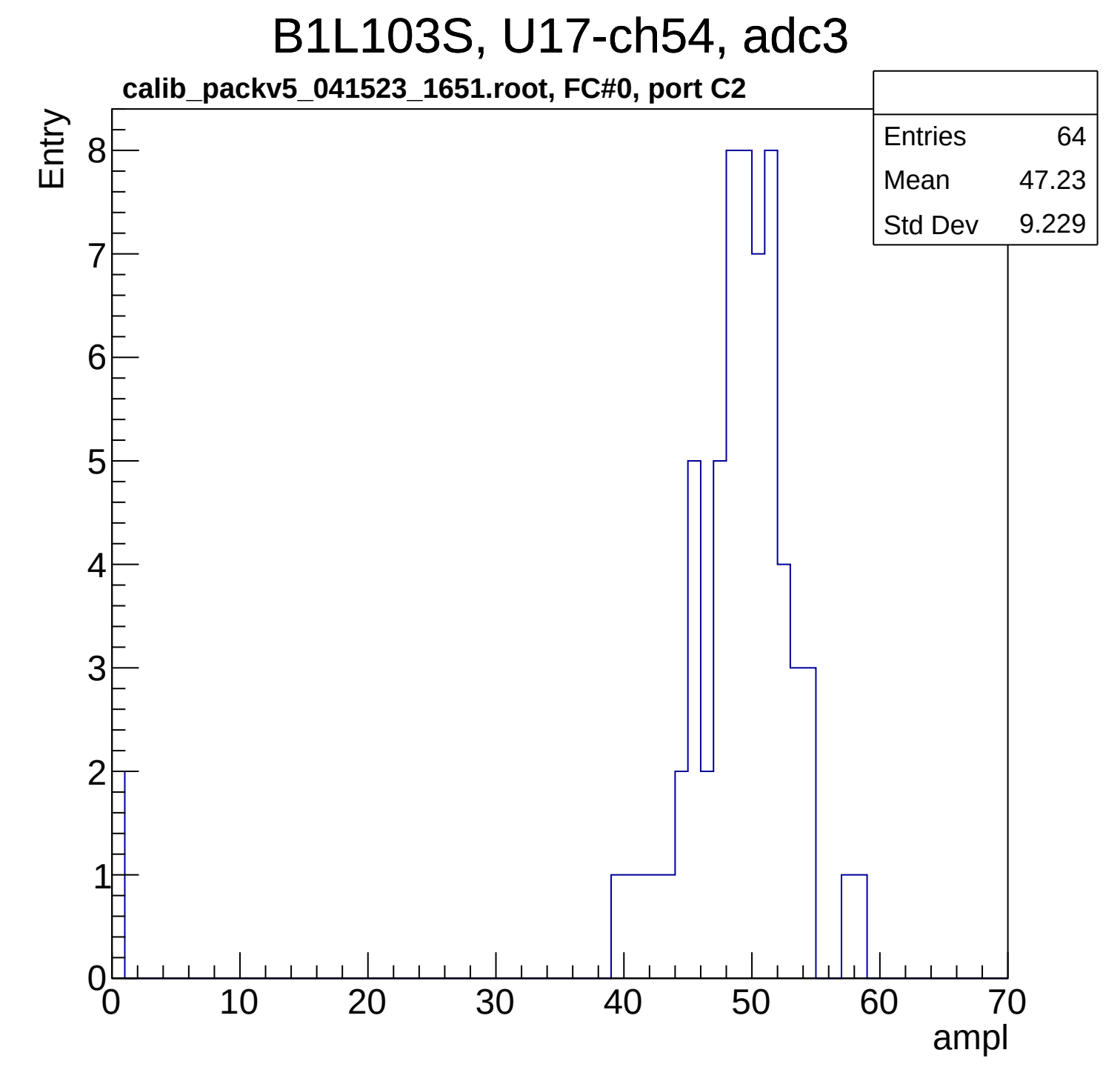
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L103S, U17-ch54, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 47.23
Std Dev 9.229
Entry
ampl
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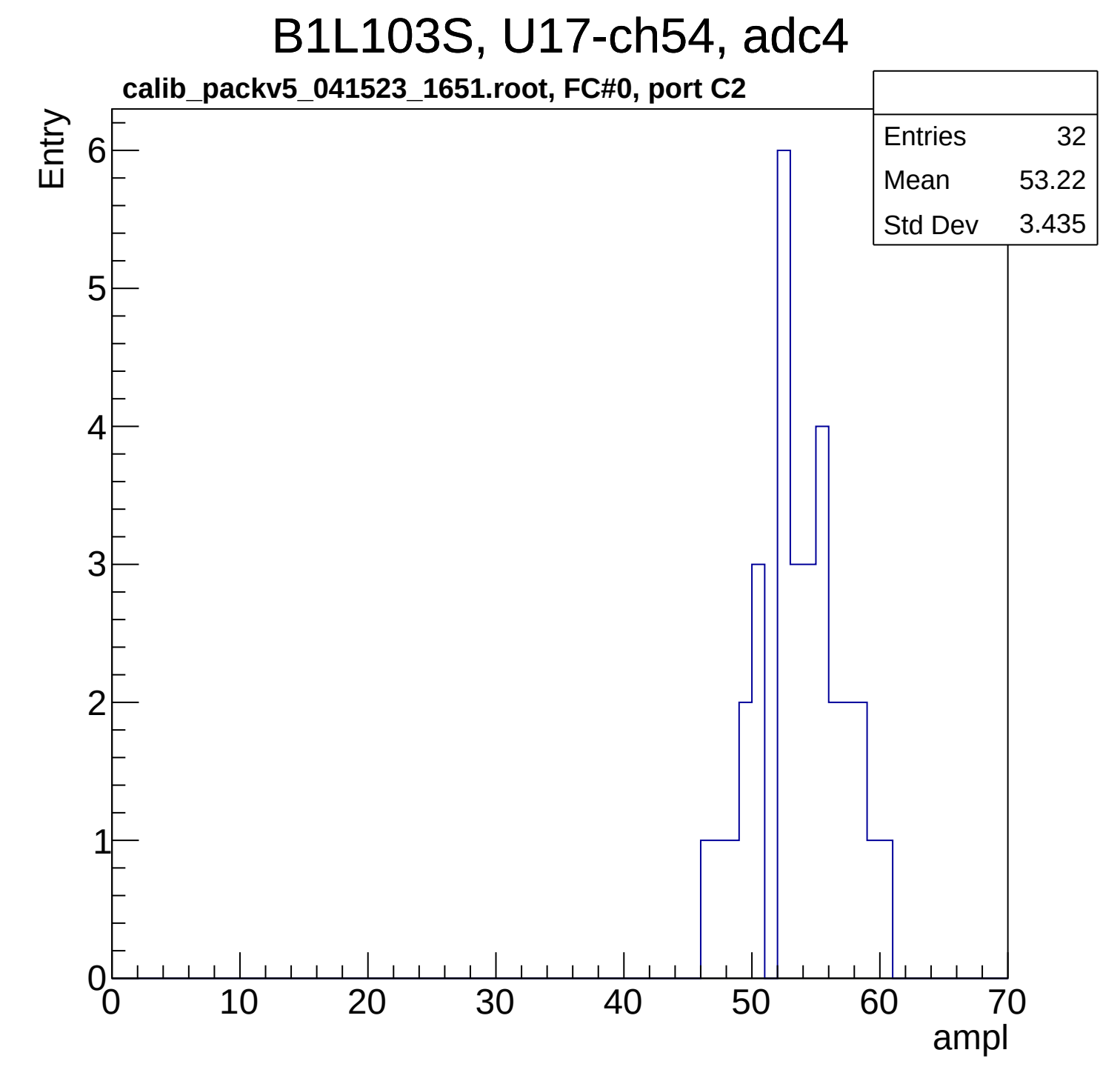
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U17-ch54, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 32
Mean 53.22
Std Dev 3.435
Entry
ampl
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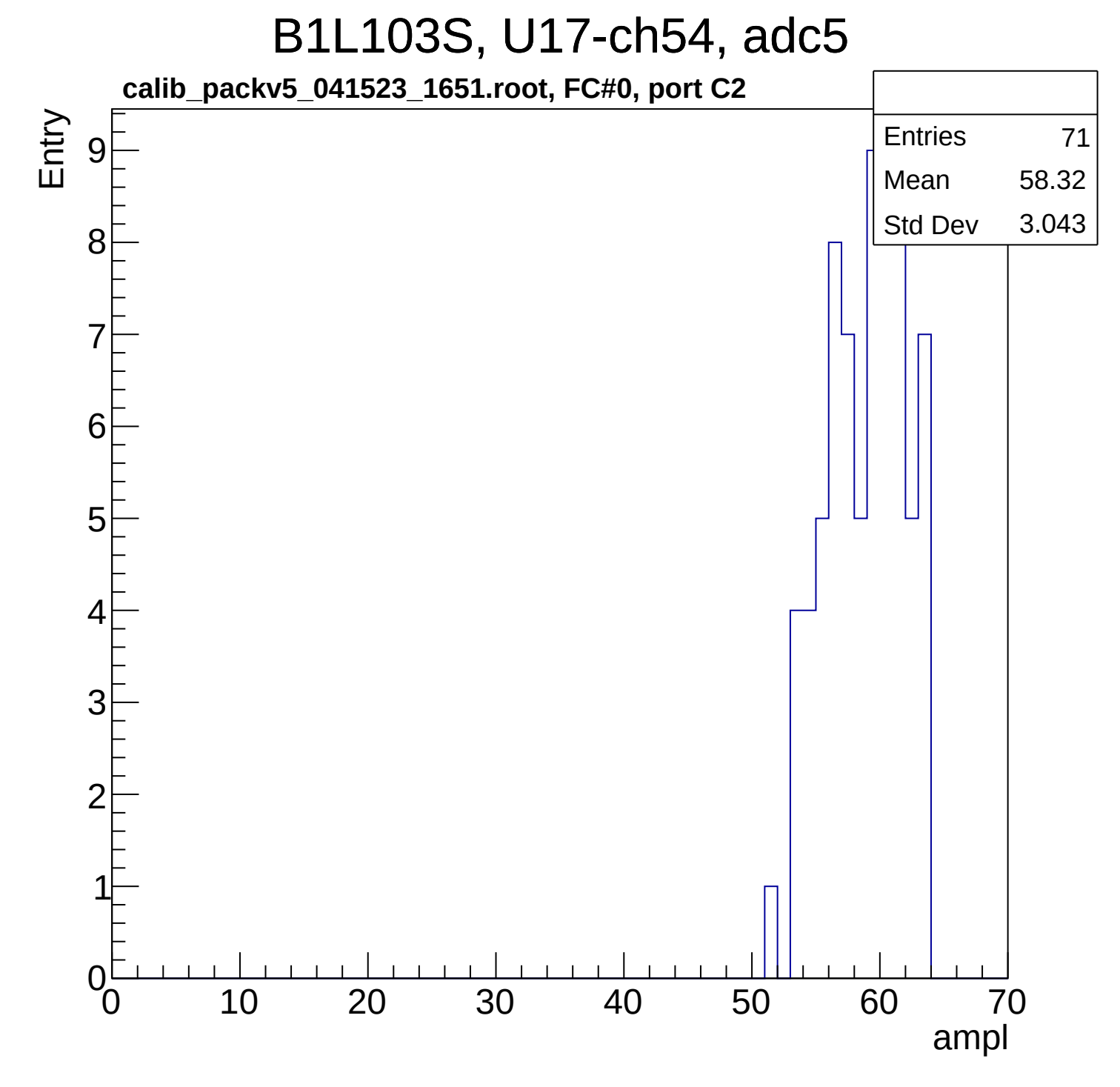
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U17-ch54, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 58.32
Std Dev 3.043
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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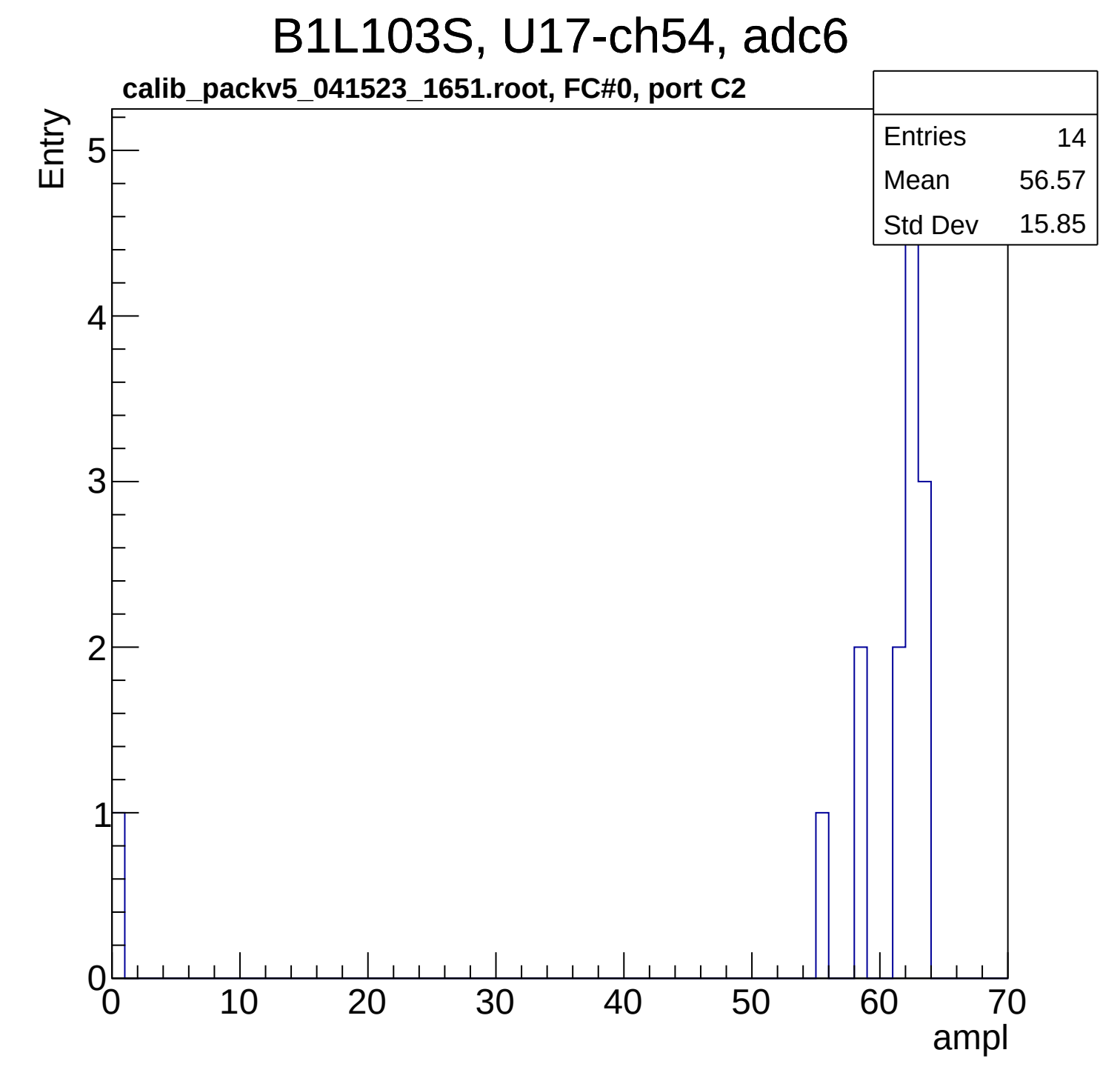
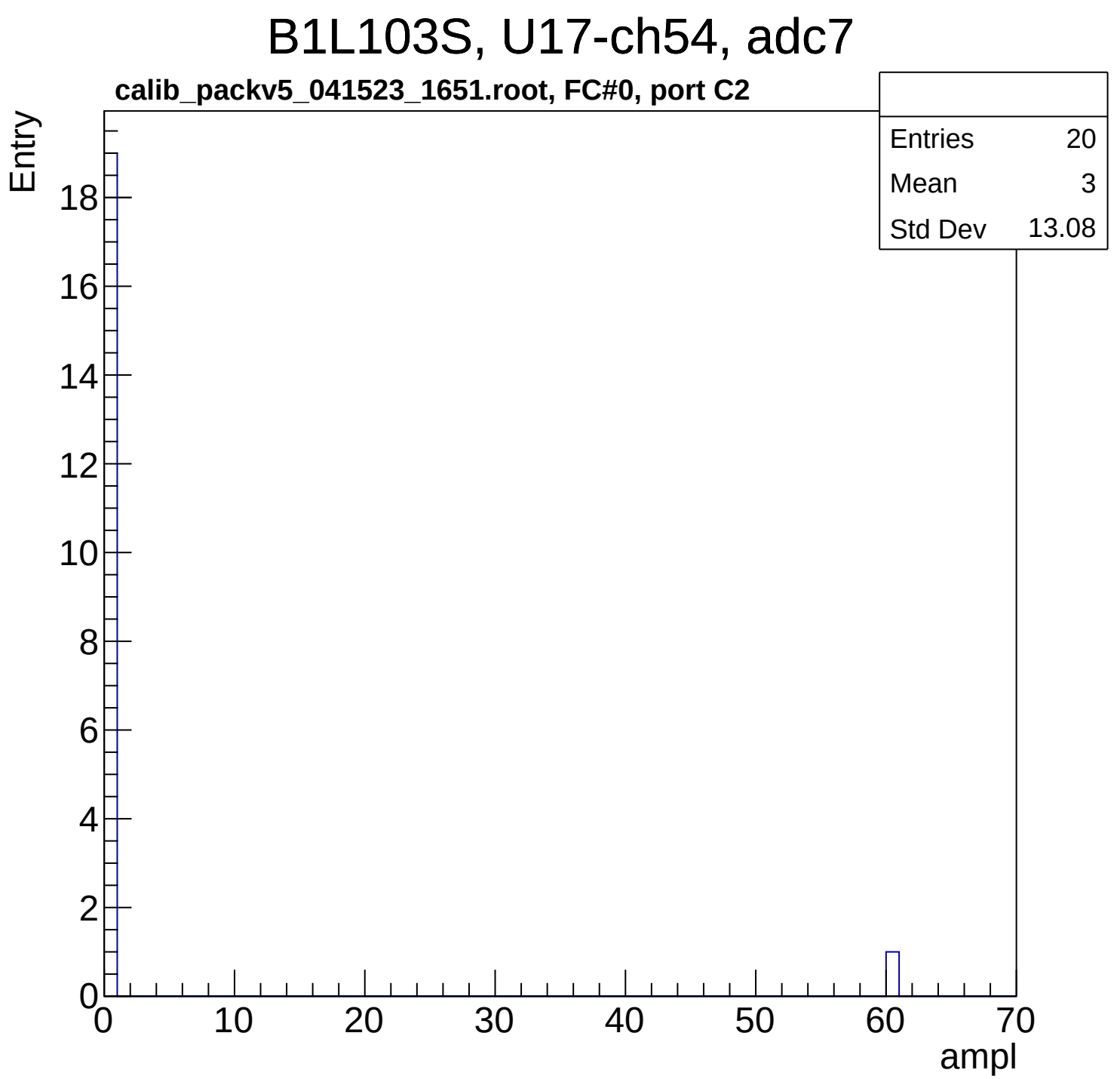

B1L103S, U17-ch54, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 14
Mean 56.57
Std Dev 15.85
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U17-ch54, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3
Std Dev 13.08
Entry
0
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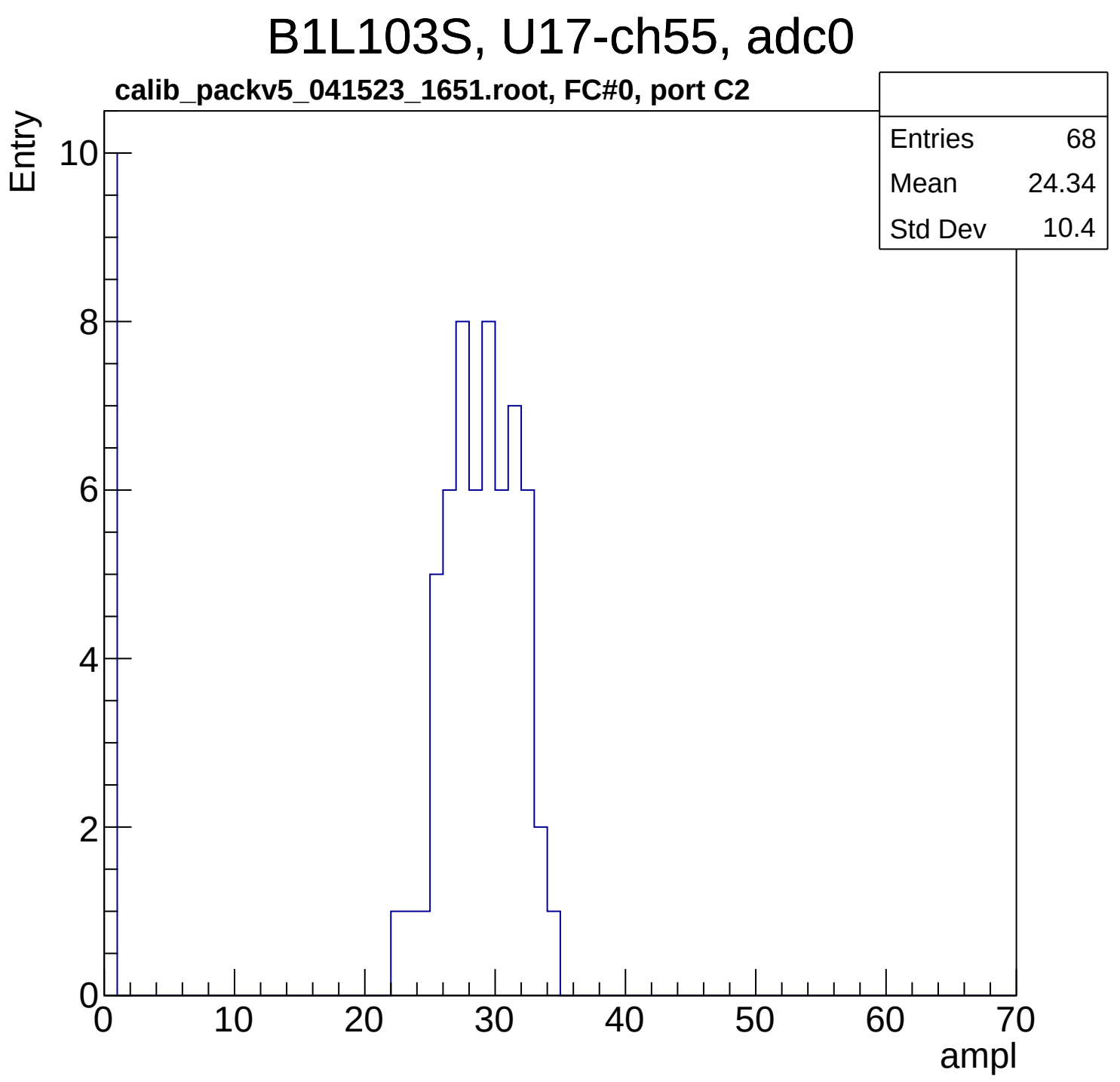
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch55, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 24.34
Std Dev 10.4
Entry
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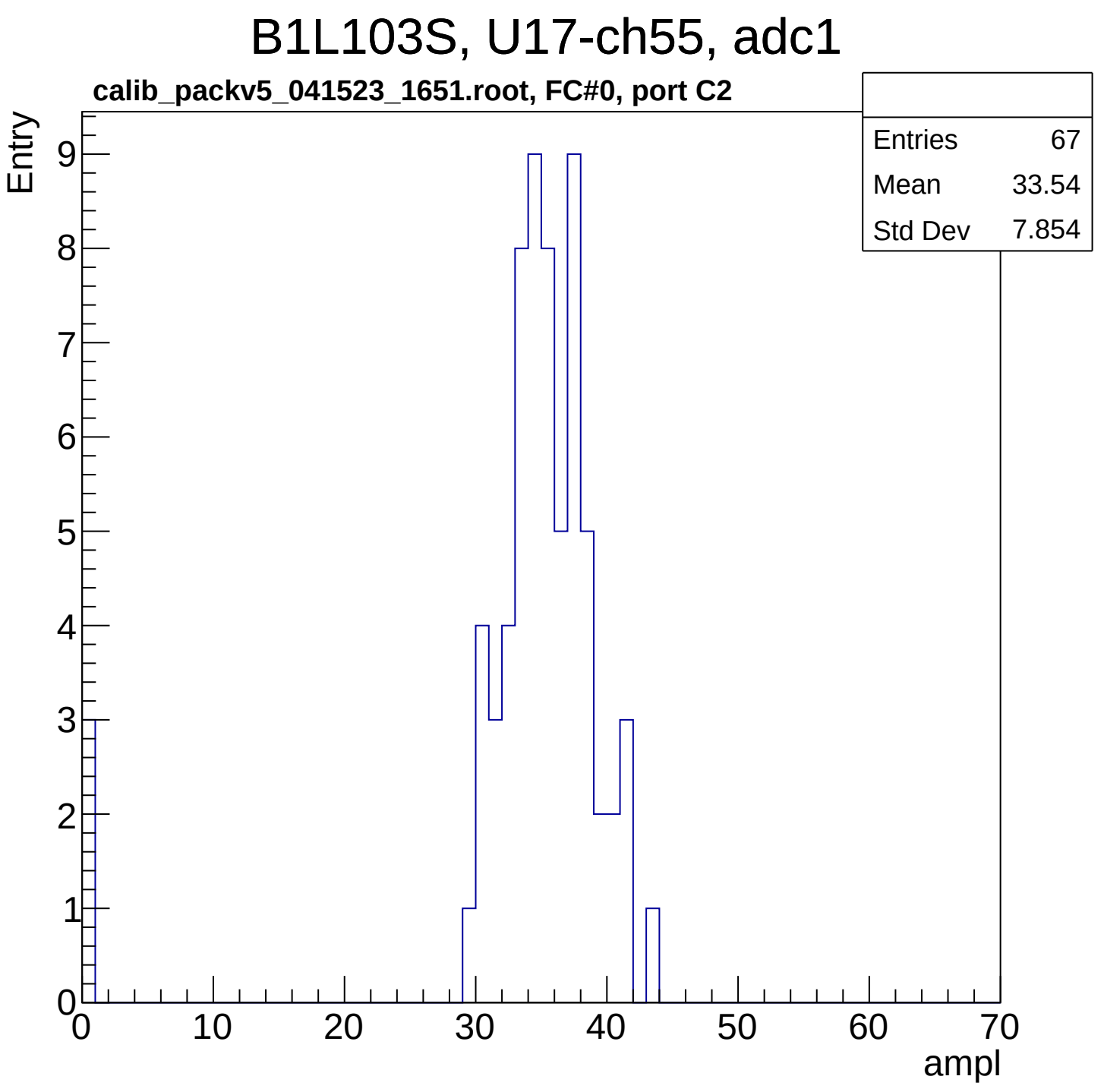
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch55, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 33.54
Std Dev 7.854
Entry
ampl
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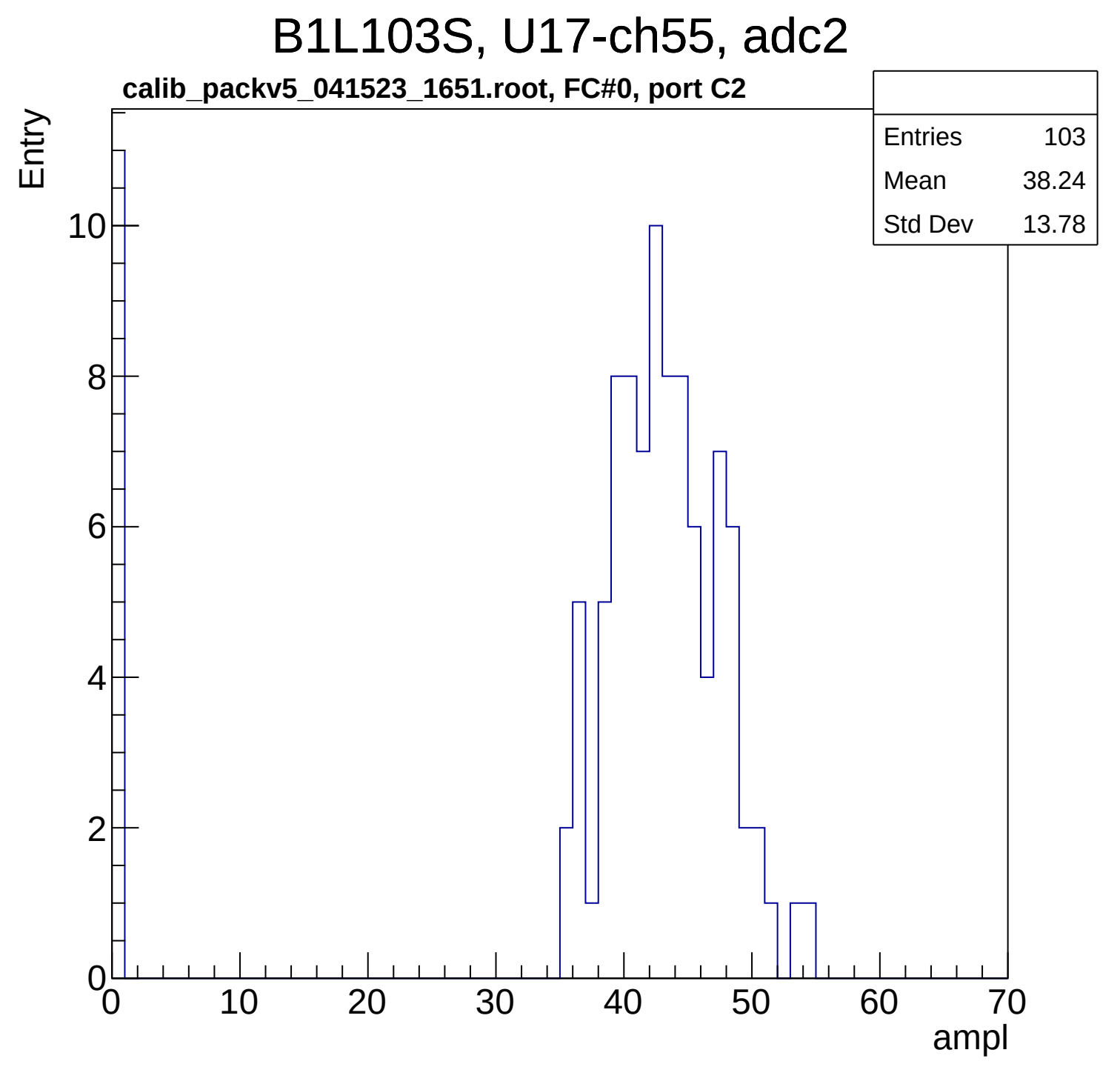
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U17-ch55, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 103
Mean 38.24
Std Dev 13.78
Entry
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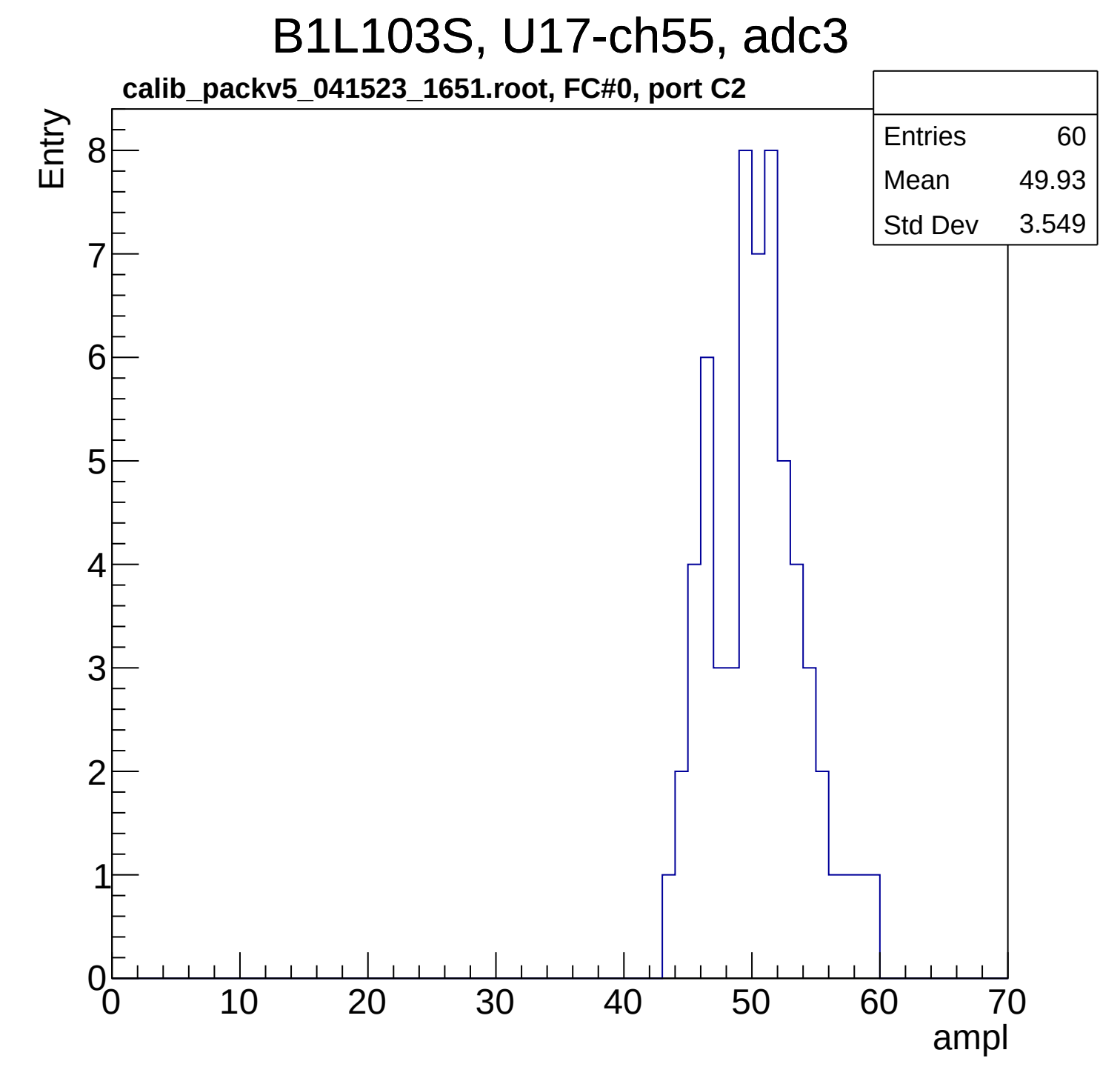
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch55, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 49.93
Std Dev 3.549
Entry
ampl
0
1
2
3
4
5
6
7
8
0
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20
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40
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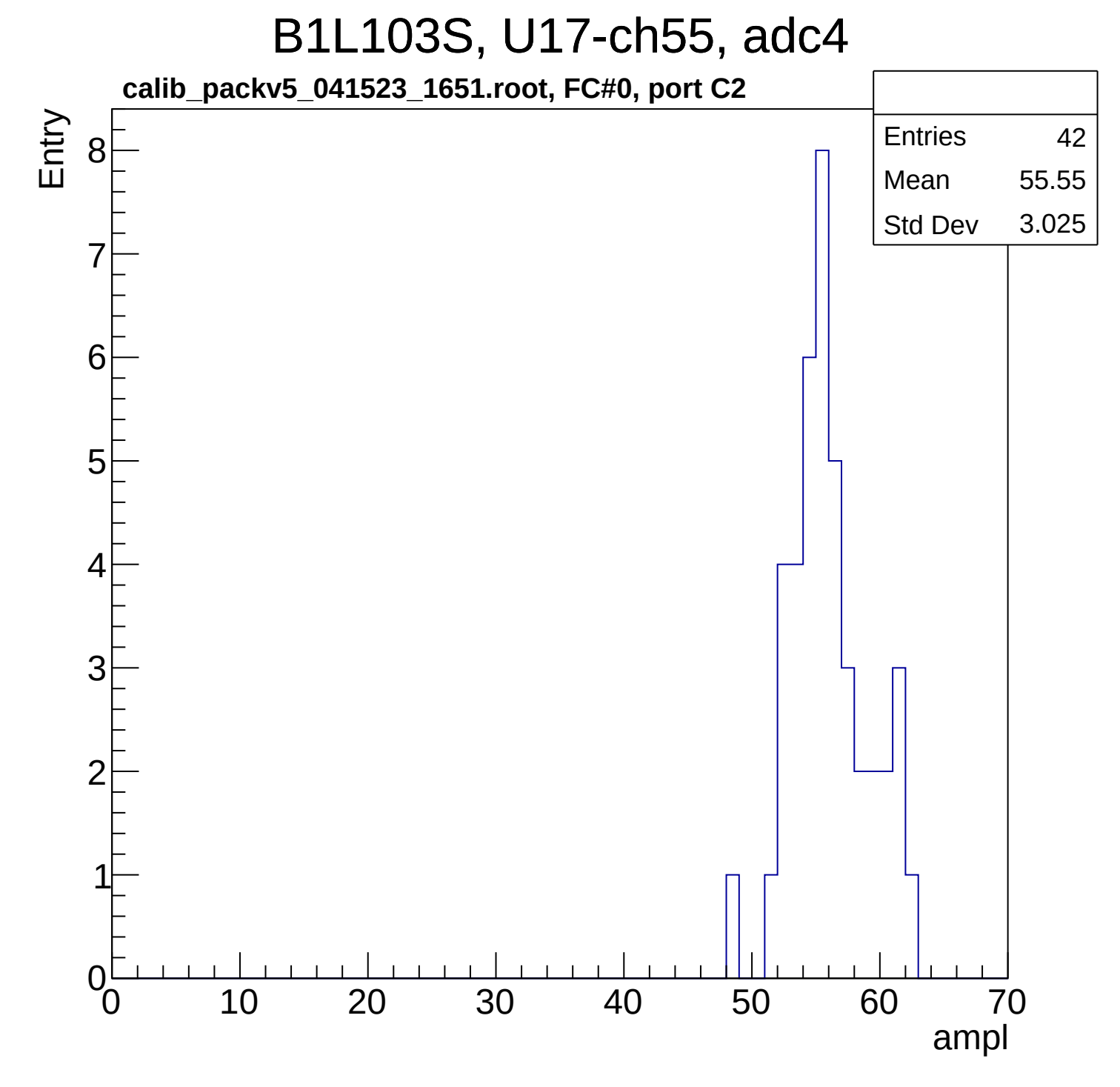
60
70


B1L103S, U17-ch55, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 42
Mean 55.55
Std Dev 3.025
Entry
ampl
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1
2
3
4
5
6
7
8
0
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40
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60
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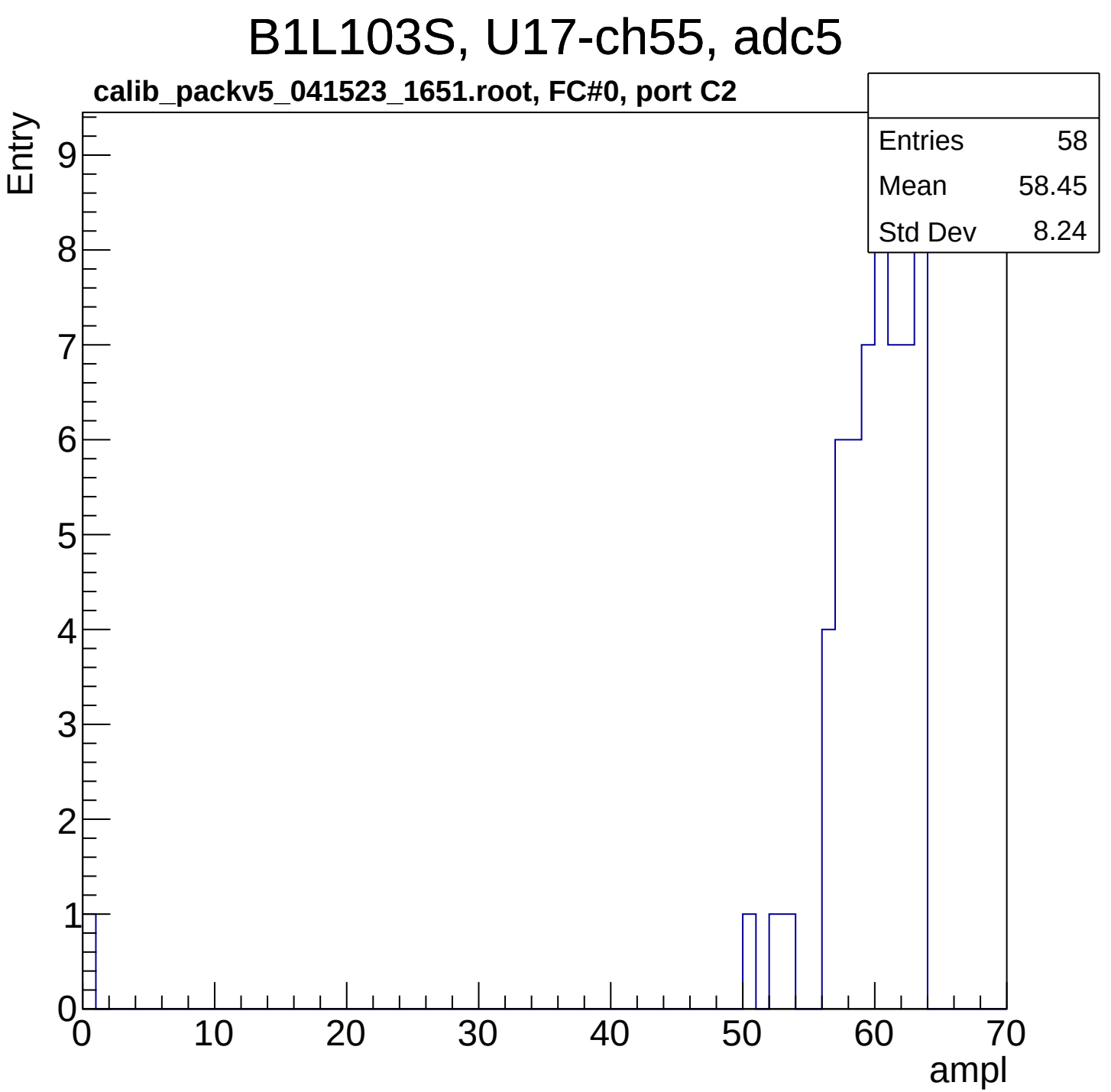
B1L103S, U17-ch55, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 58.45
Std Dev 8.24
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
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20
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40
50
60
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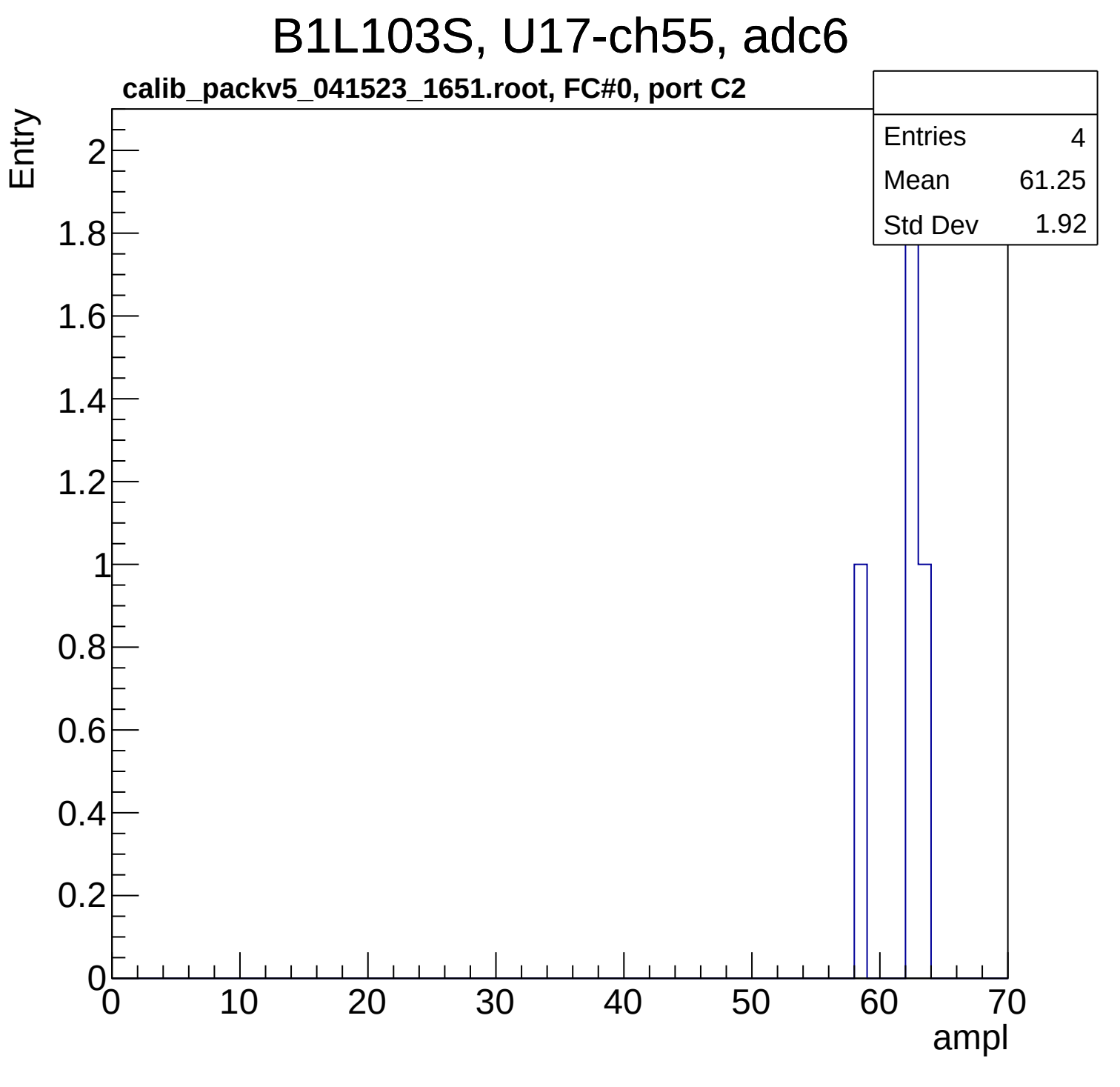
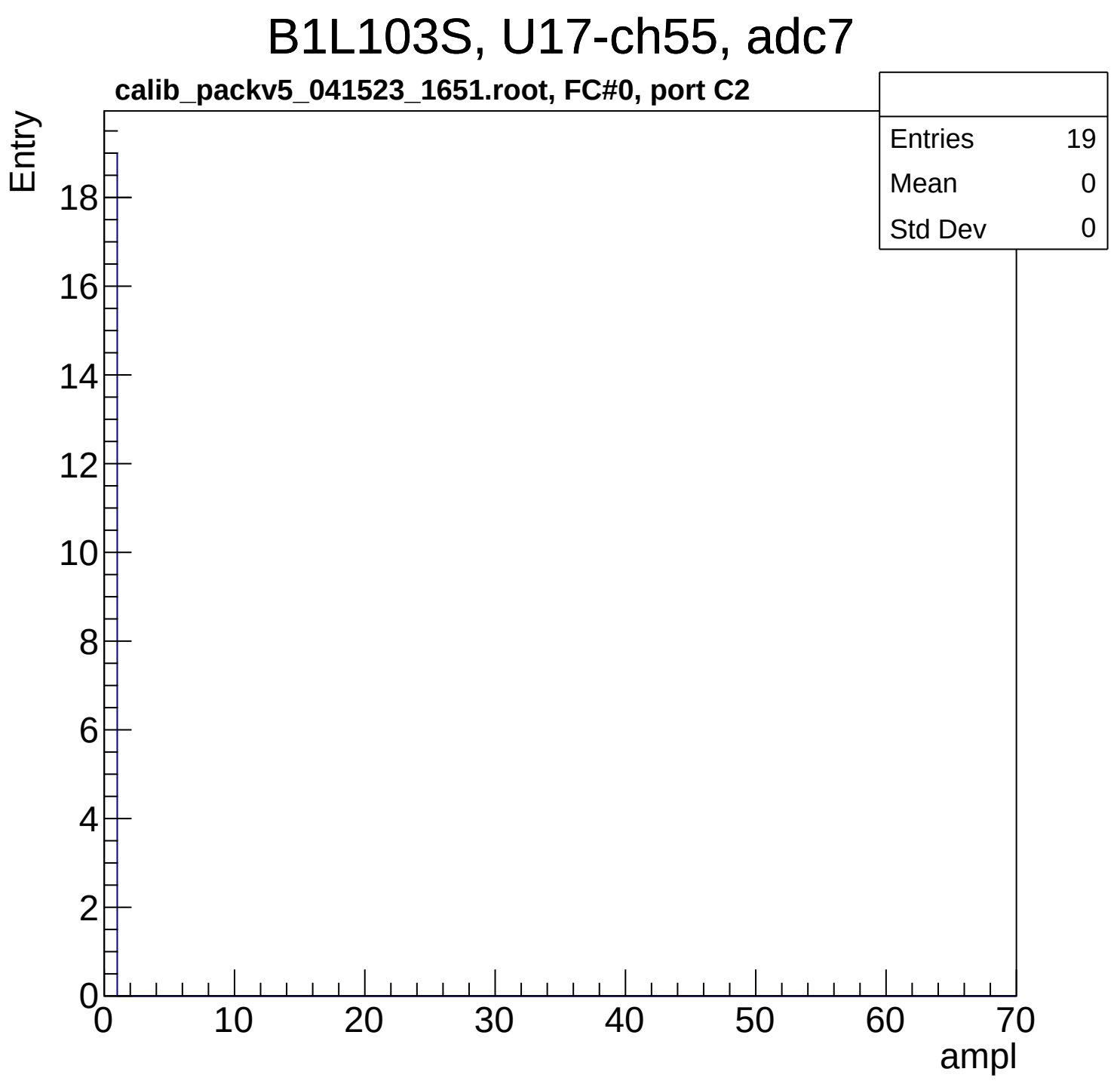
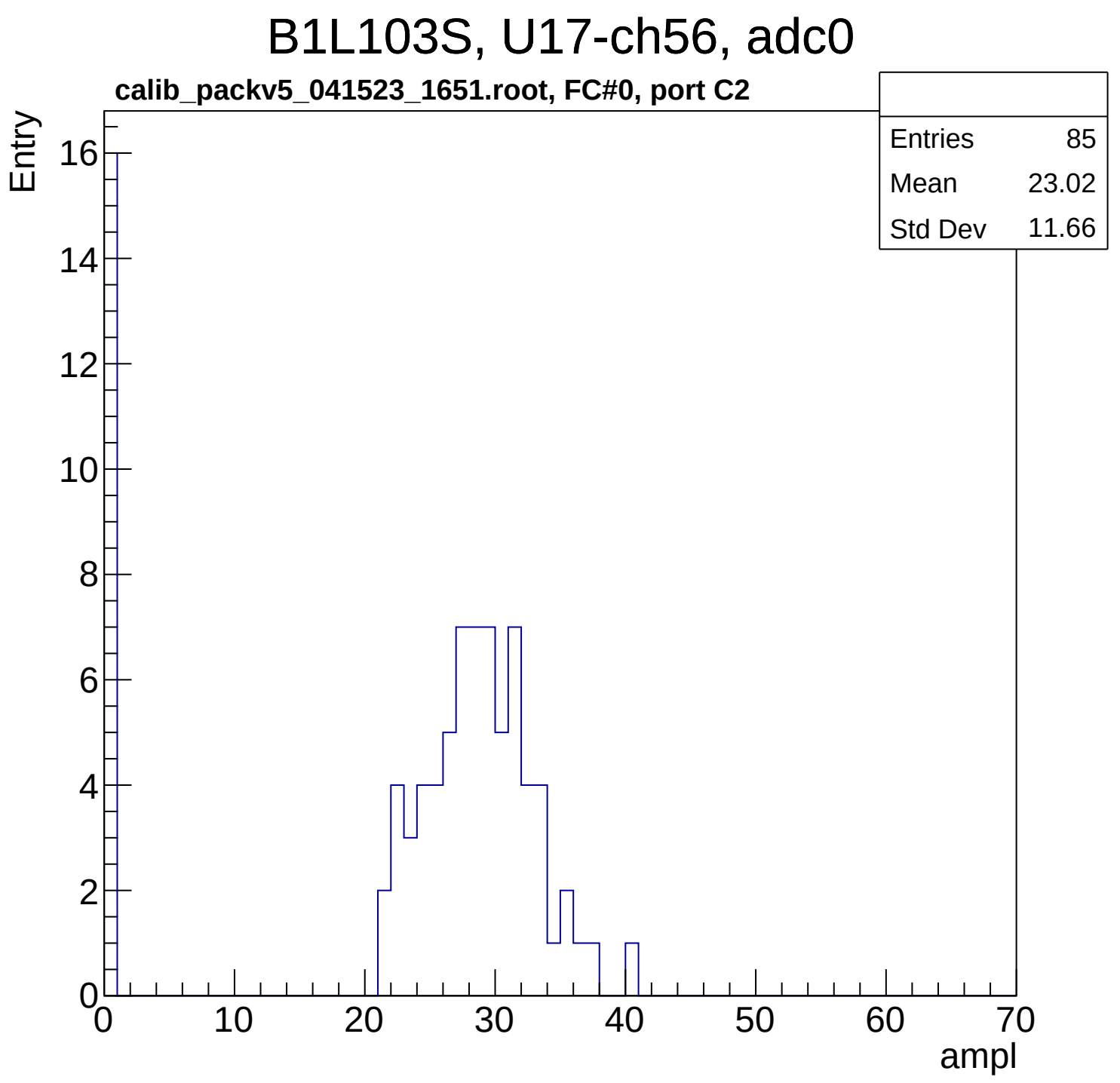

B1L103S, U17-ch55, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 4
Mean 61.25
Std Dev 1.92
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U17-ch55, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch56, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 23.02
Std Dev 11.66
Entry
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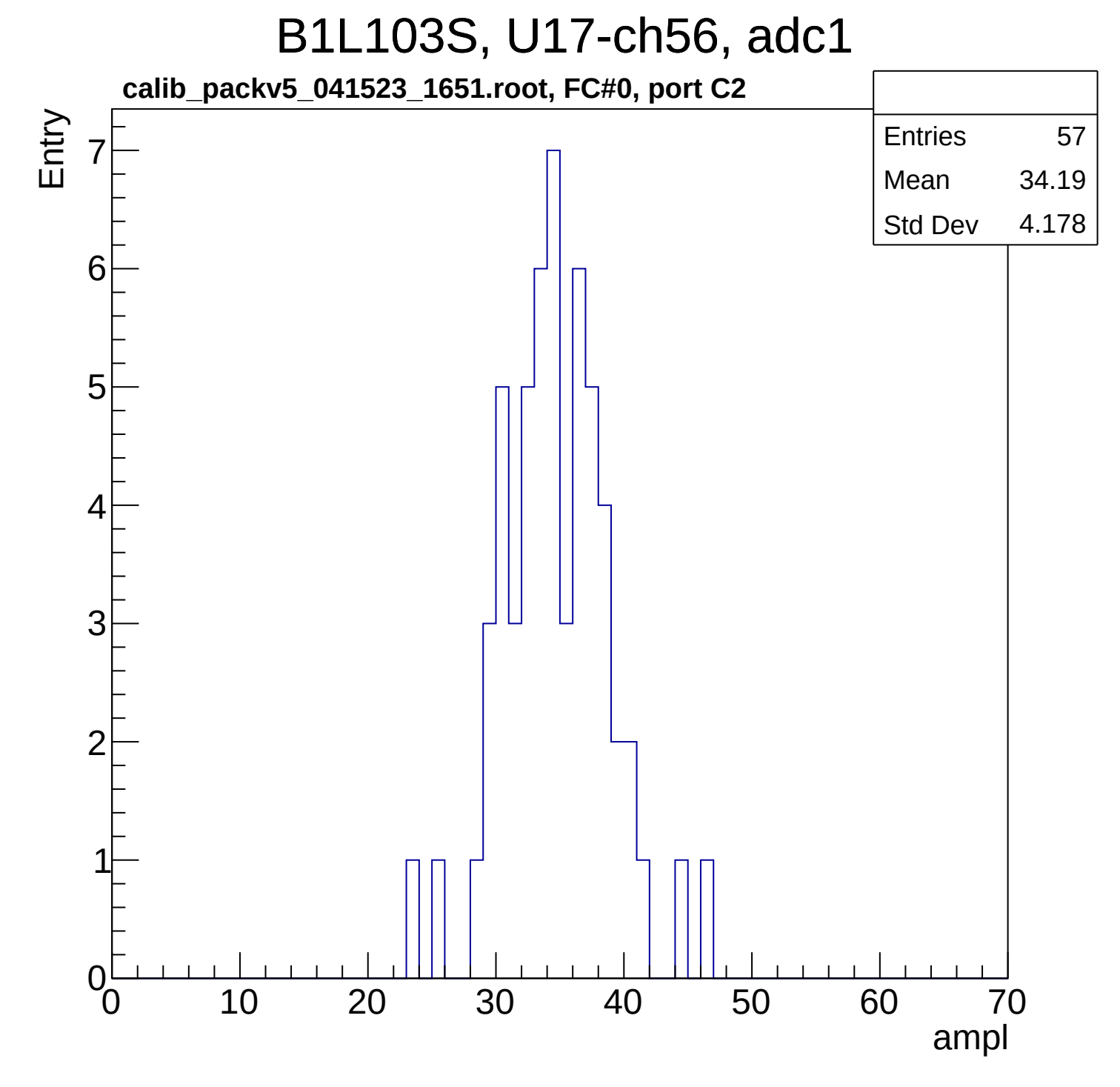
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch56, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 34.19
Std Dev 4.178
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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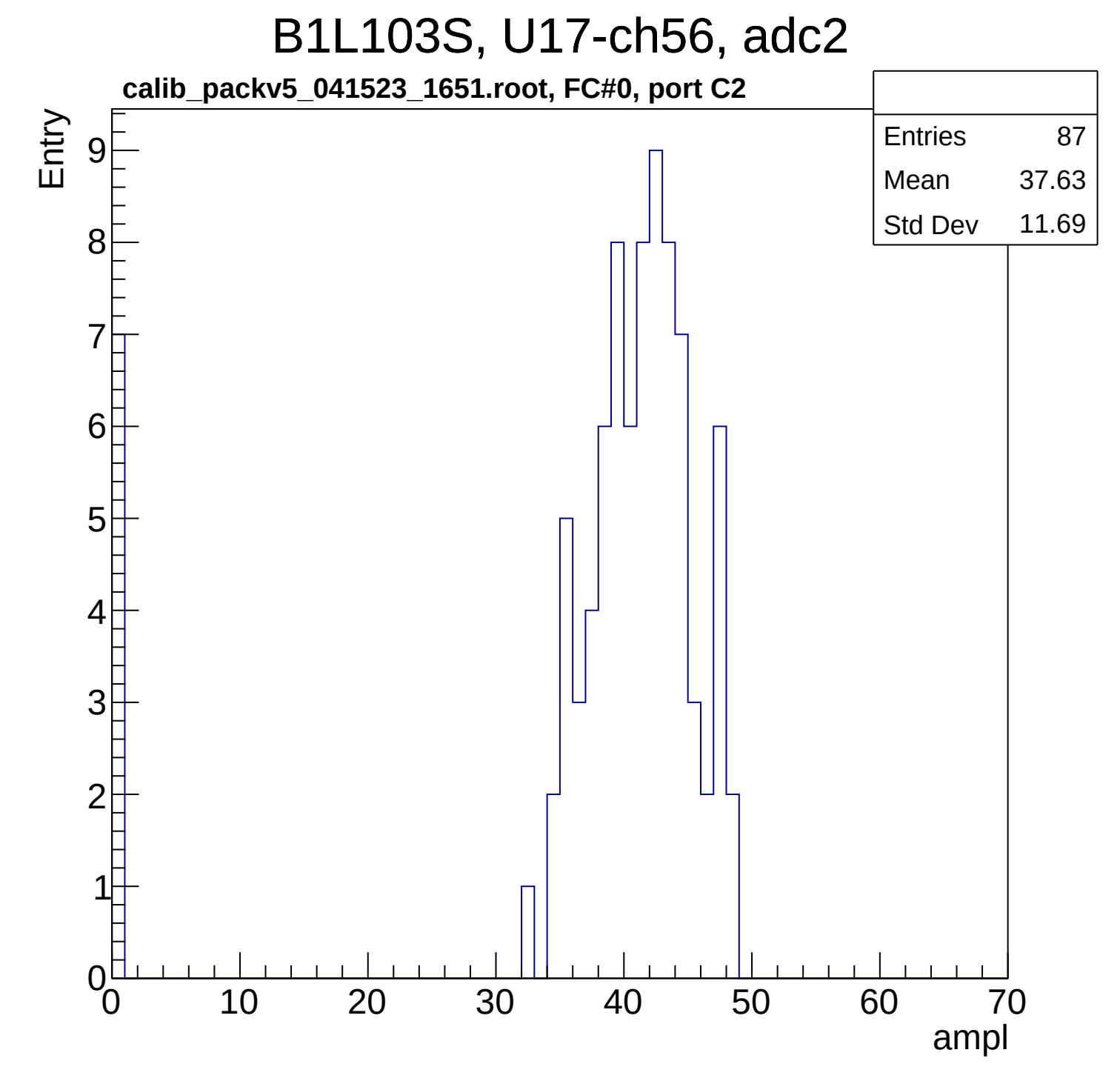
B1L103S, U17-ch56, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 87
Mean 37.63
Std Dev 11.69
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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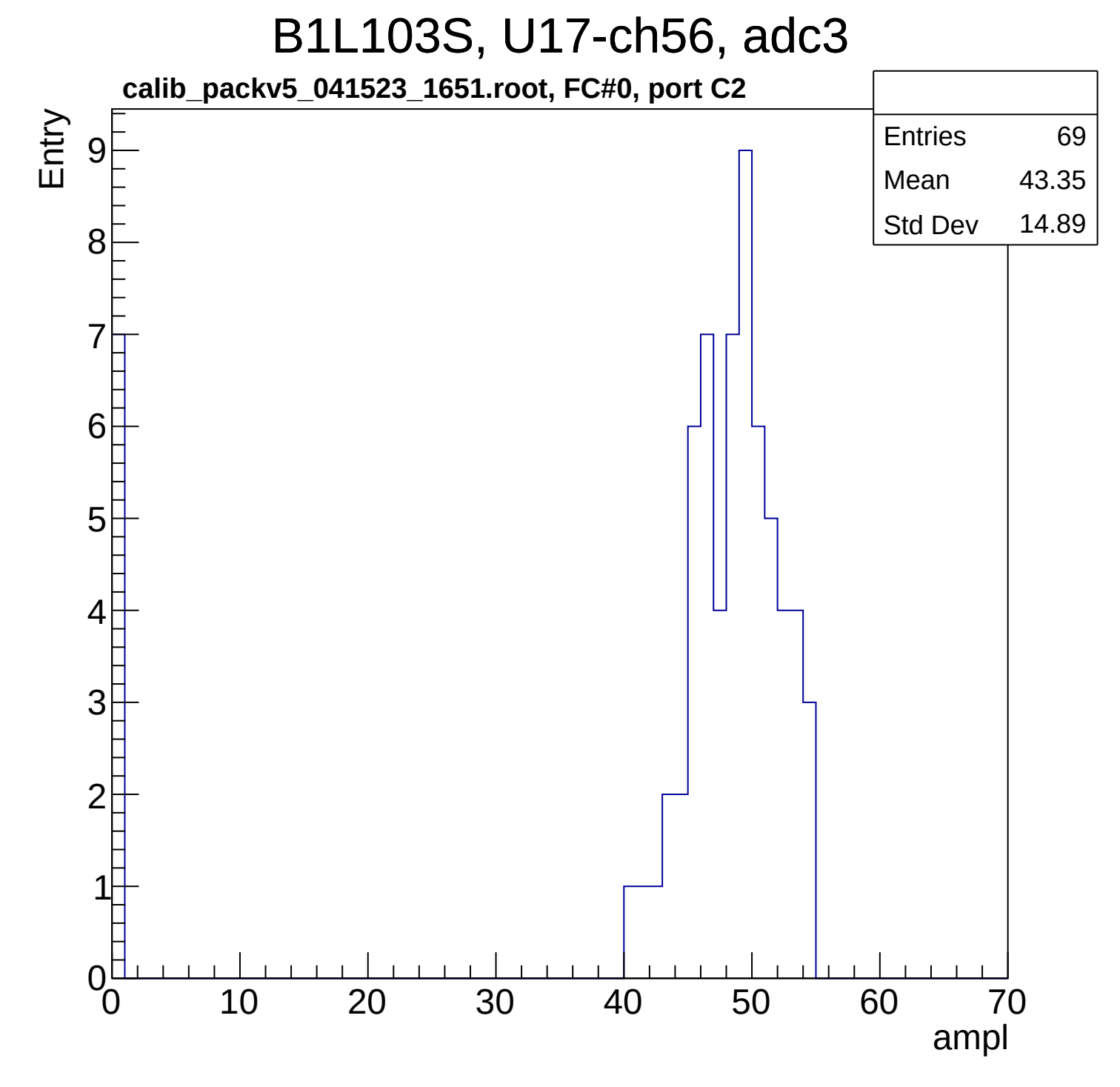
B1L103S, U17-ch56, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 43.35
Std Dev 14.89
Entry
ampl
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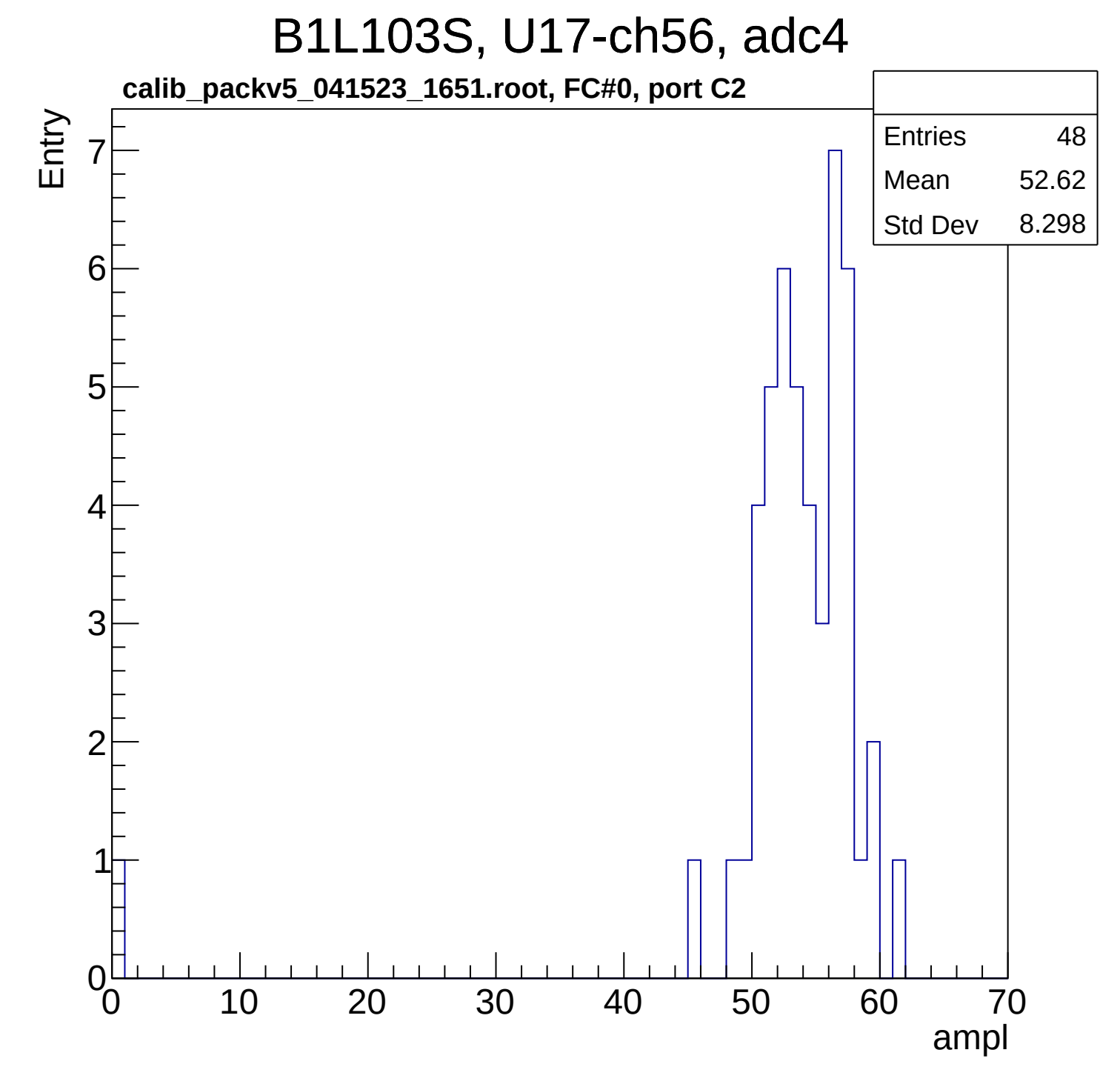
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U17-ch56, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 52.62
Std Dev 8.298
Entry
ampl
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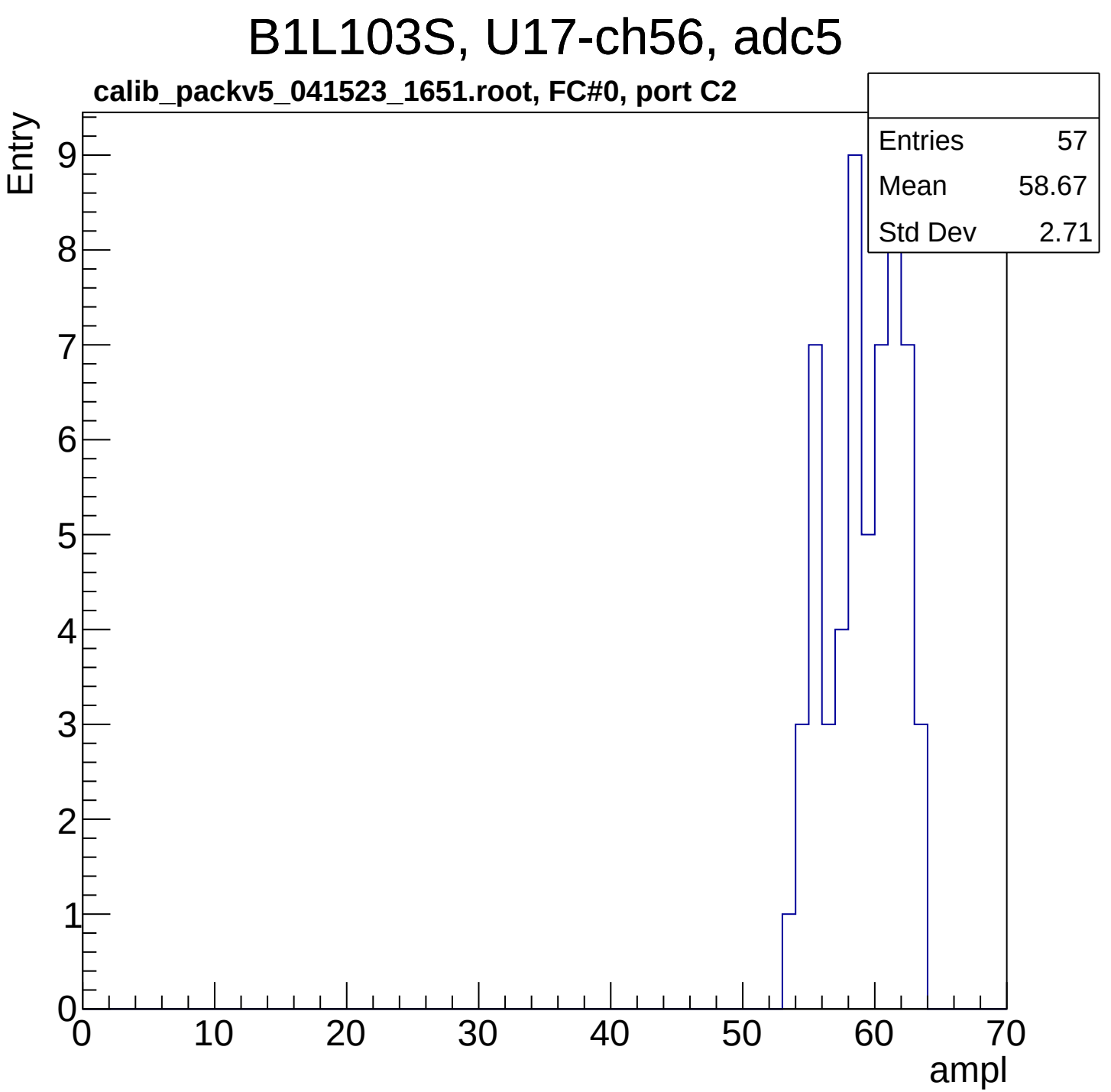
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U17-ch56, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 58.67
Std Dev 2.71
Entry
ampl
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2
3
4
5
6
7
8
9
0
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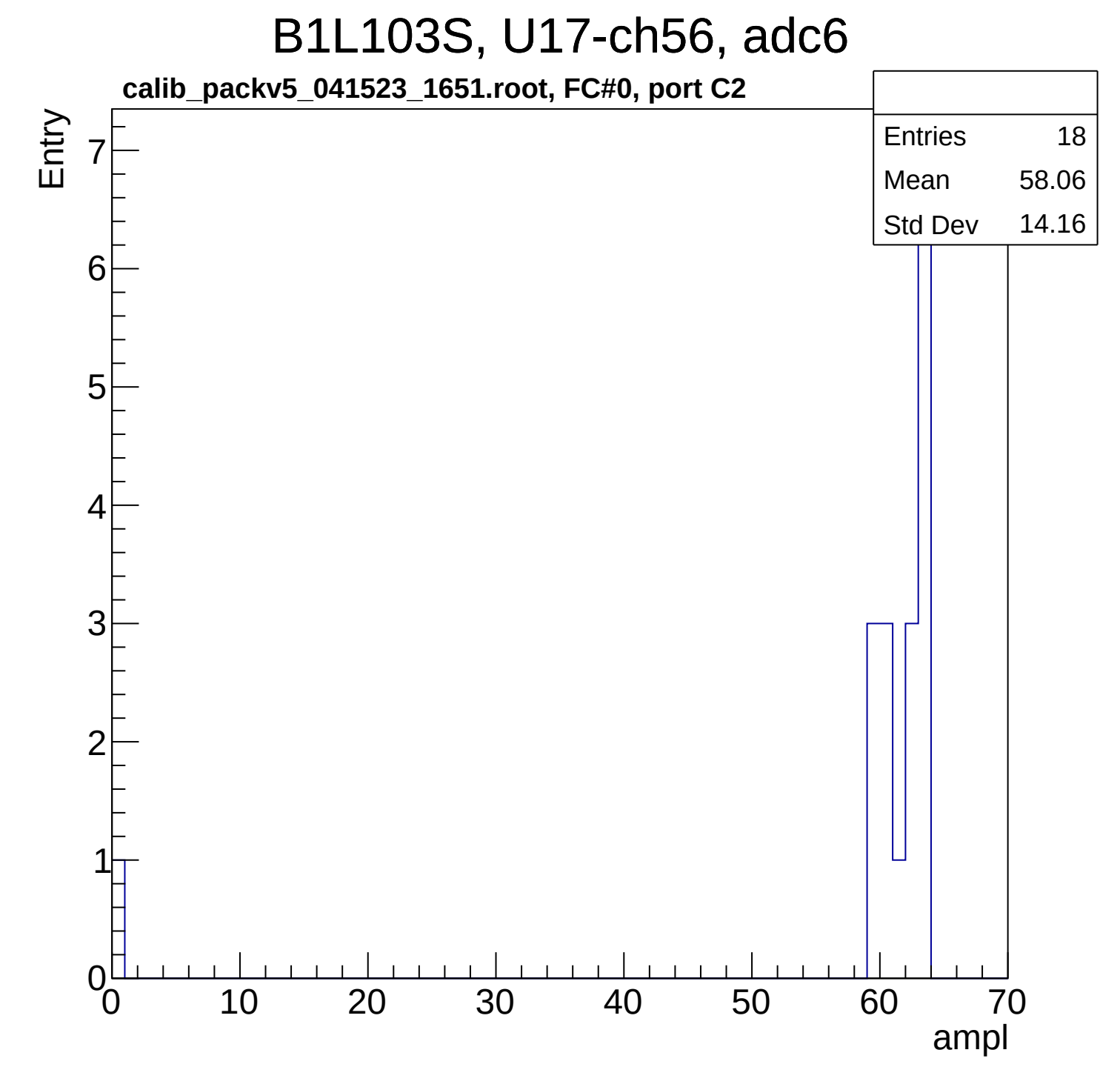
B1L103S, U17-ch56, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 58.06
Std Dev 14.16
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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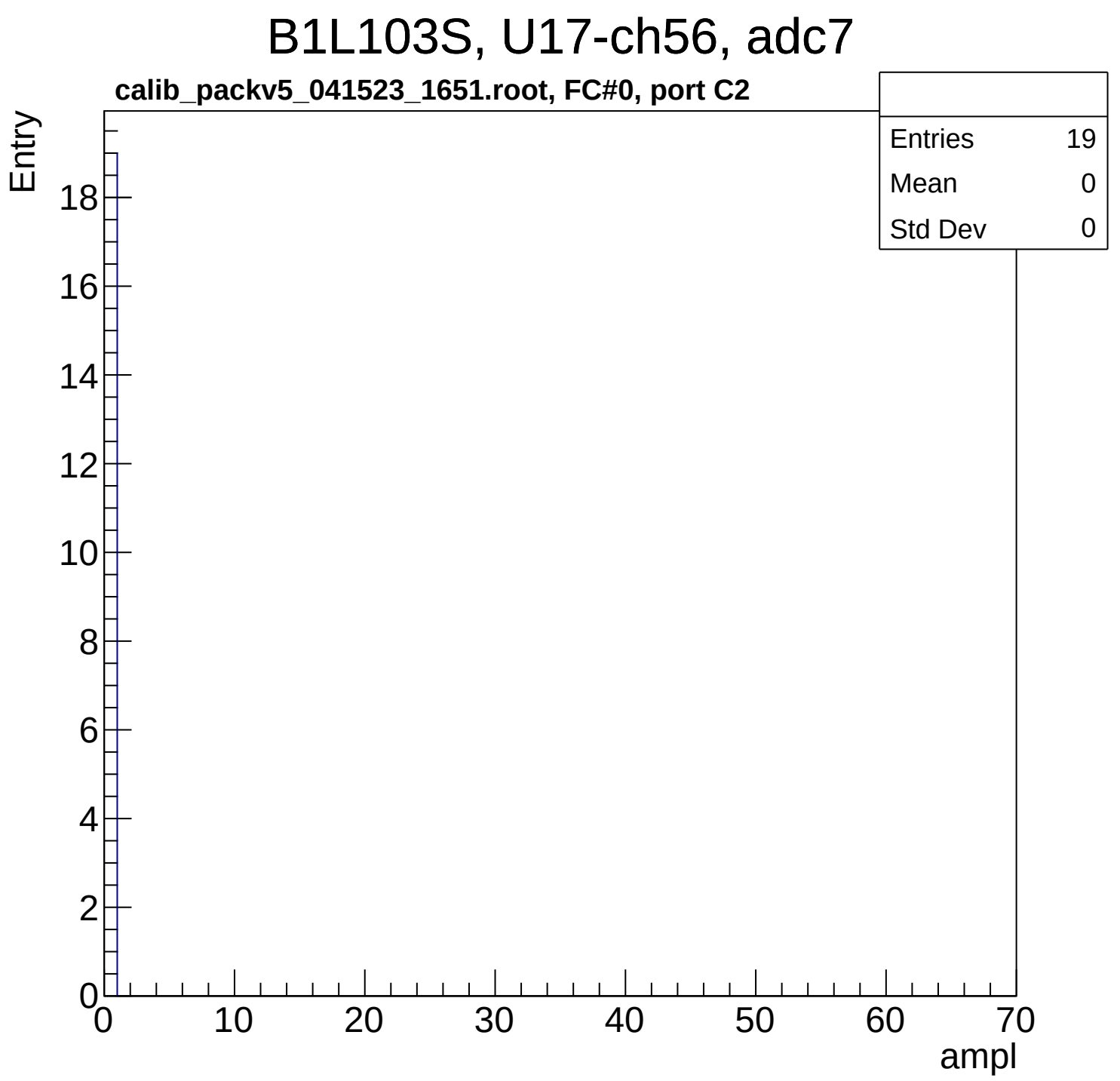
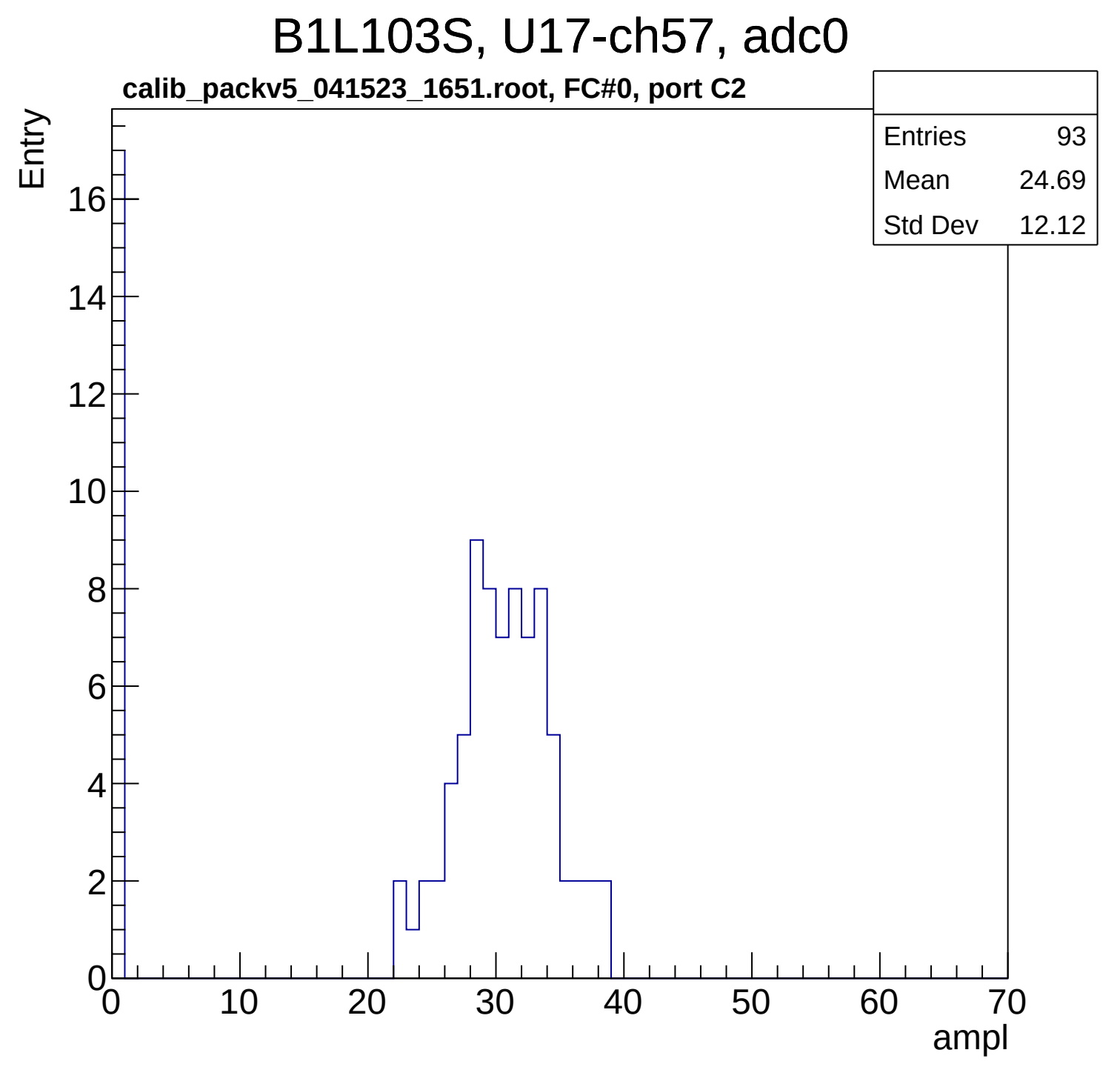

B1L103S, U17-ch56, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch57, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 93
Mean 24.69
Std Dev 12.12
Entry
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6
8
10
12
14
16
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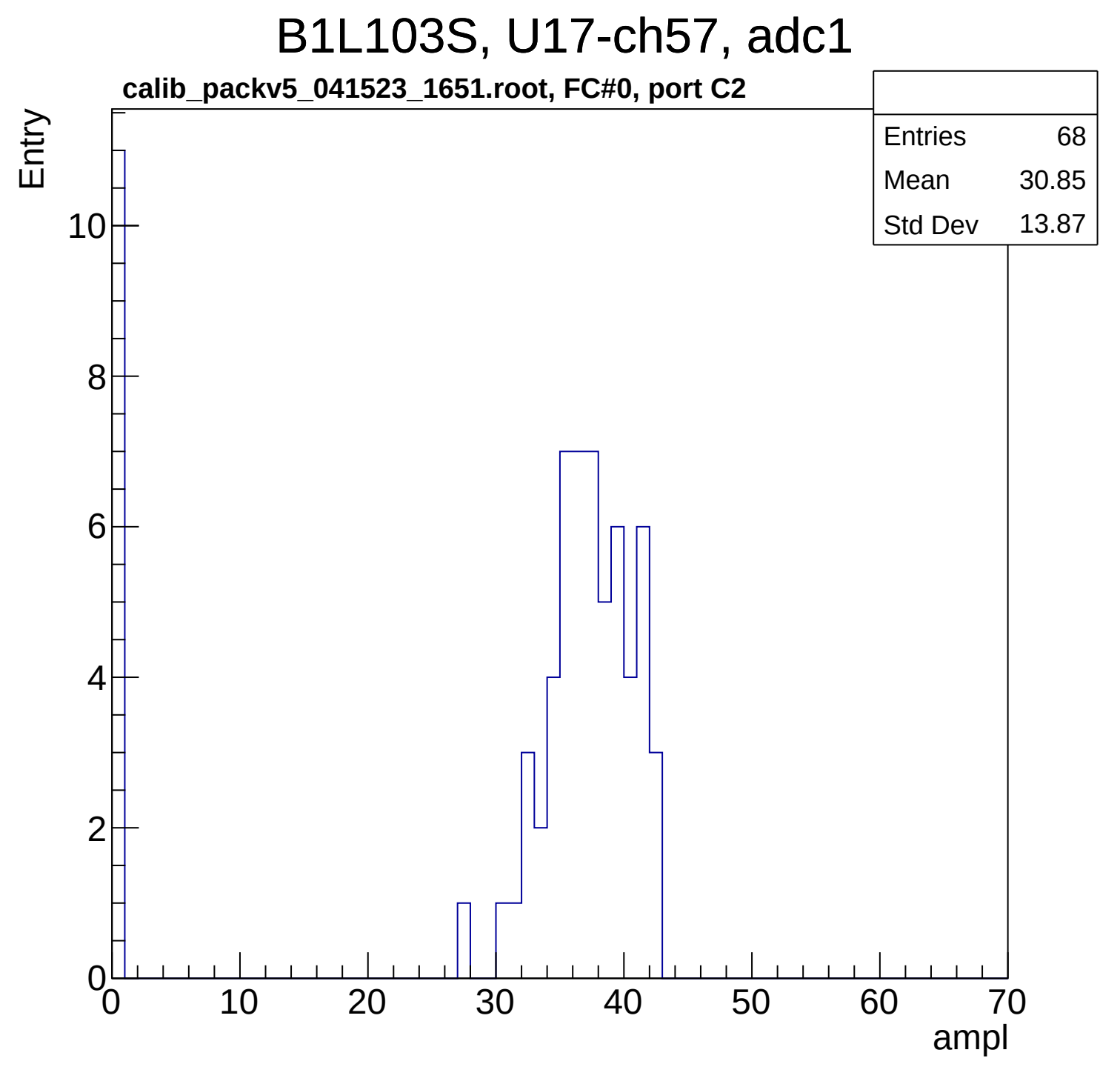
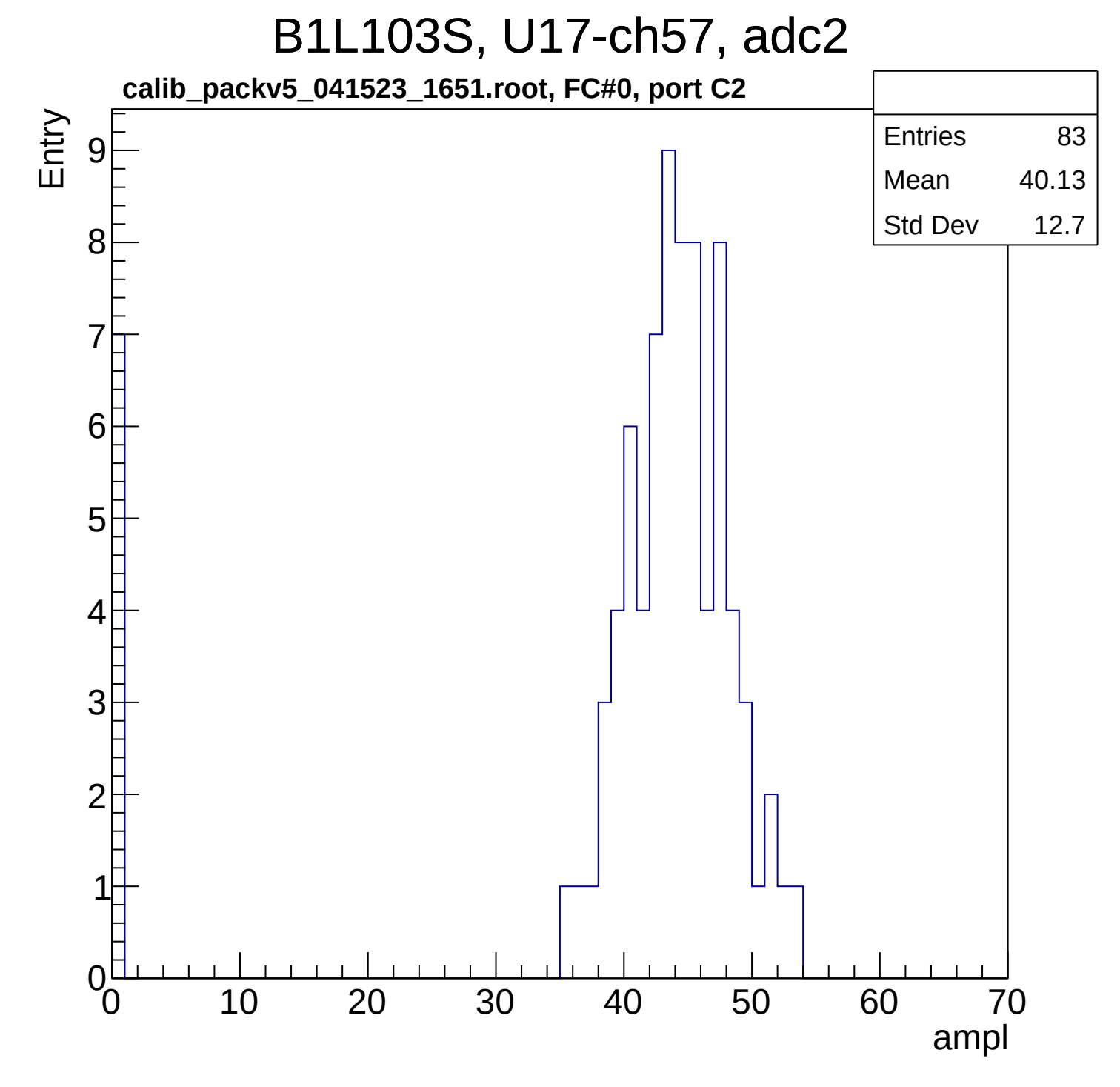
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch57, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 30.85
Std Dev 13.87
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch57, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 40.13
Std Dev 12.7
Entry
ampl
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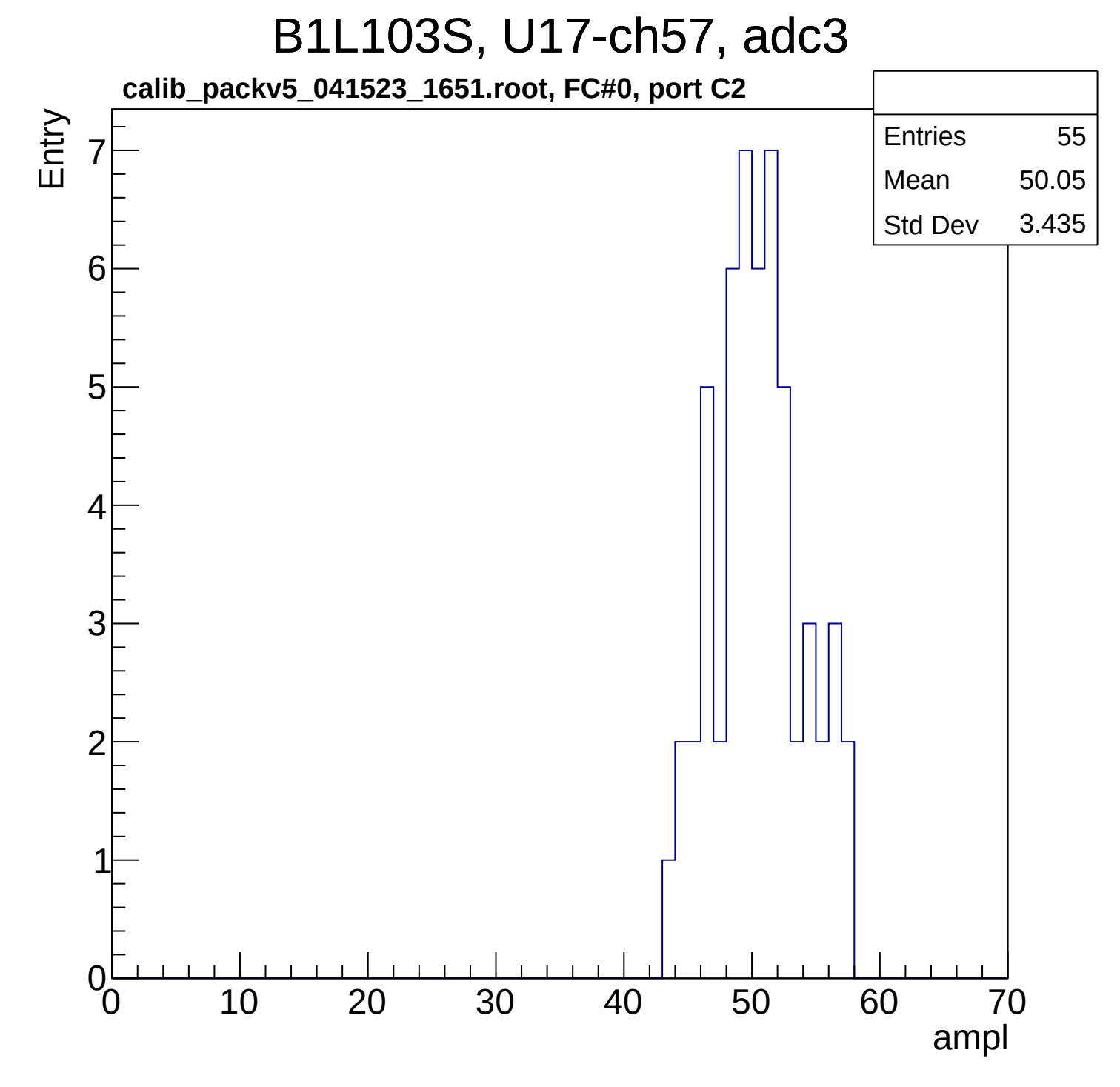
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U17-ch57, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 50.05
Std Dev 3.435
Entry
ampl
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1
2
3
4
5
6
7
0
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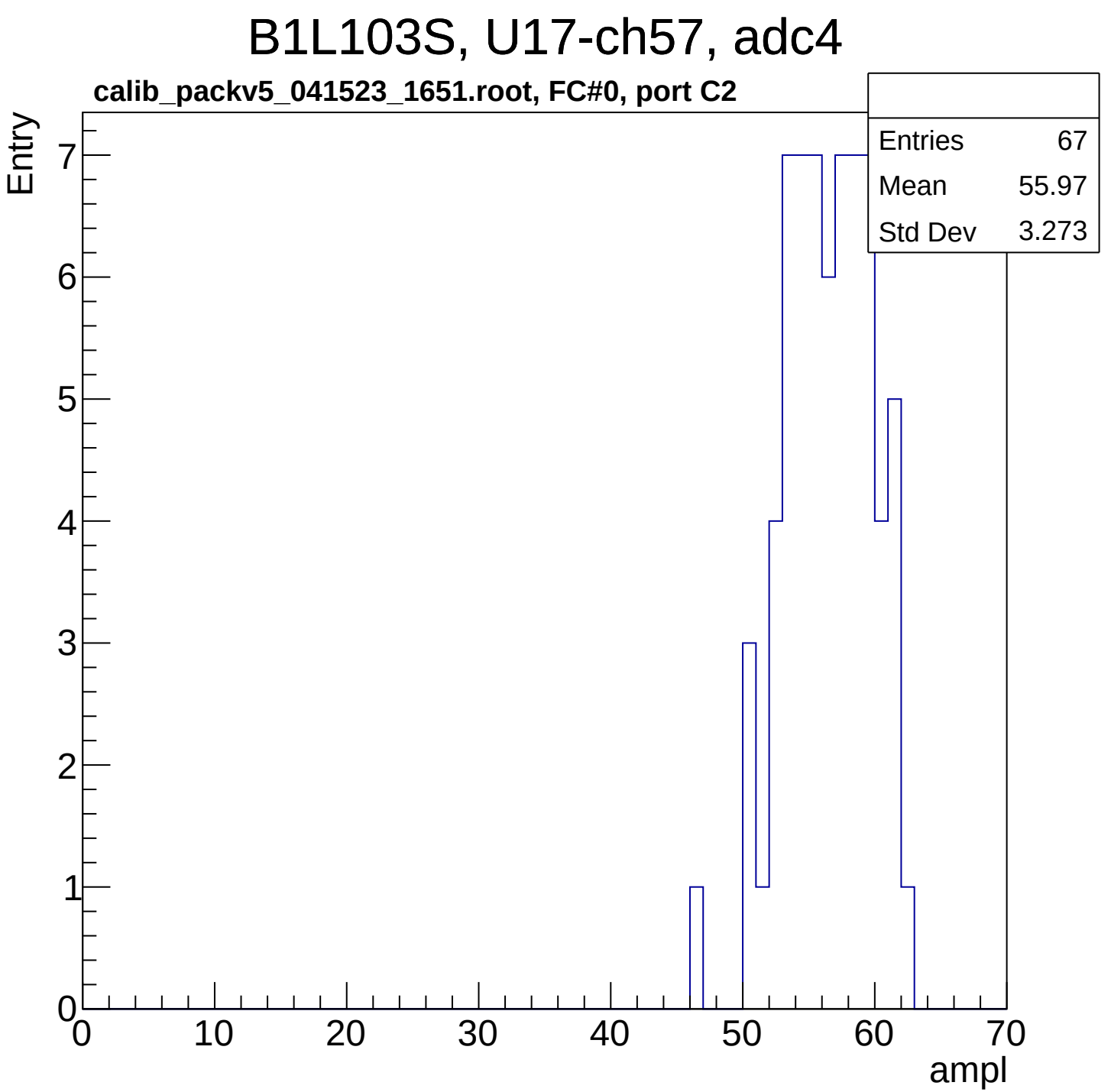
20
30
40
50
60
70


B1L103S, U17-ch57, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 55.97
Std Dev 3.273
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
30
40
50
60
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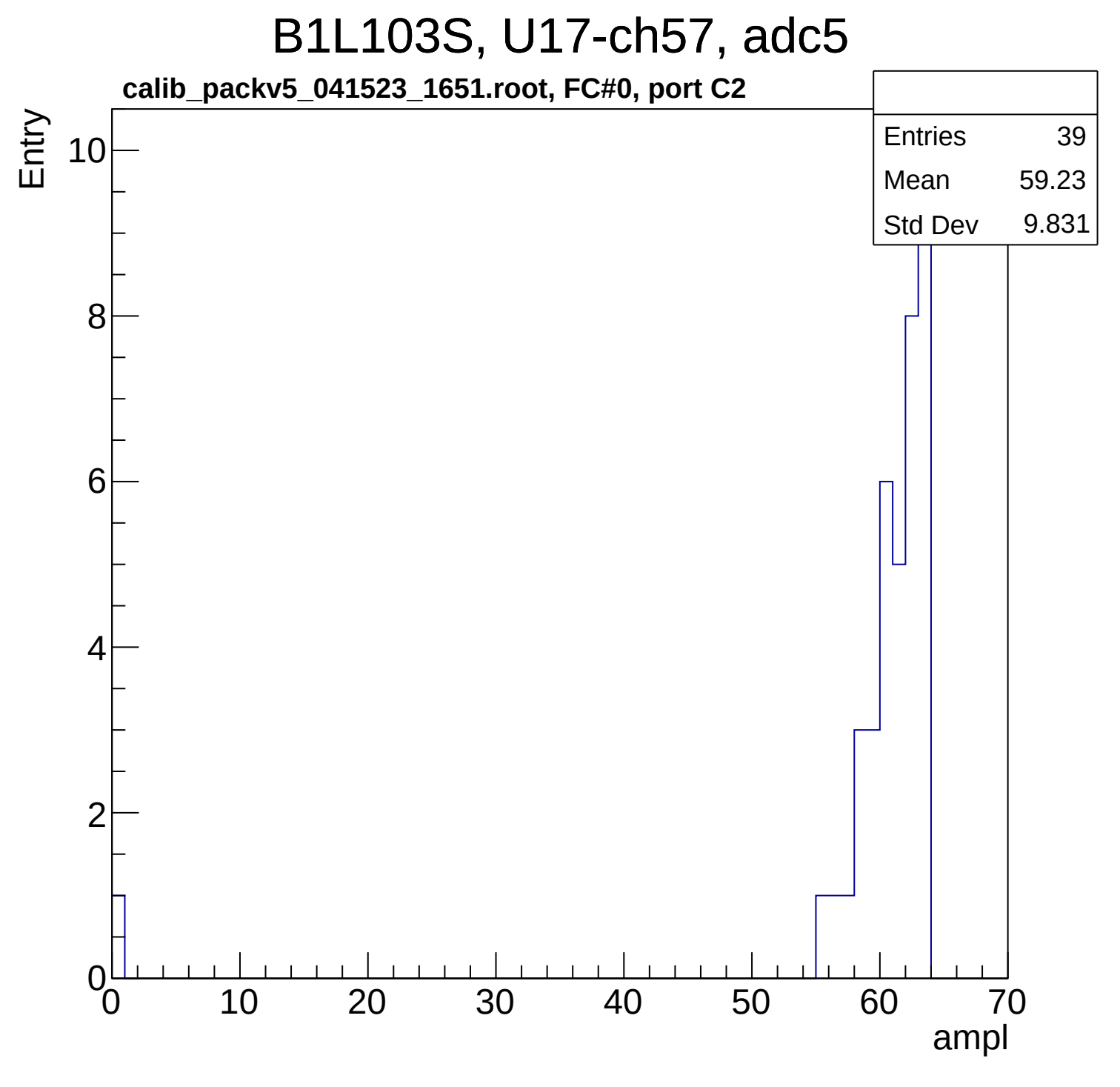
B1L103S, U17-ch57, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 39
Mean 59.23
Std Dev 9.831
Entry
ampl
0
2
4
6
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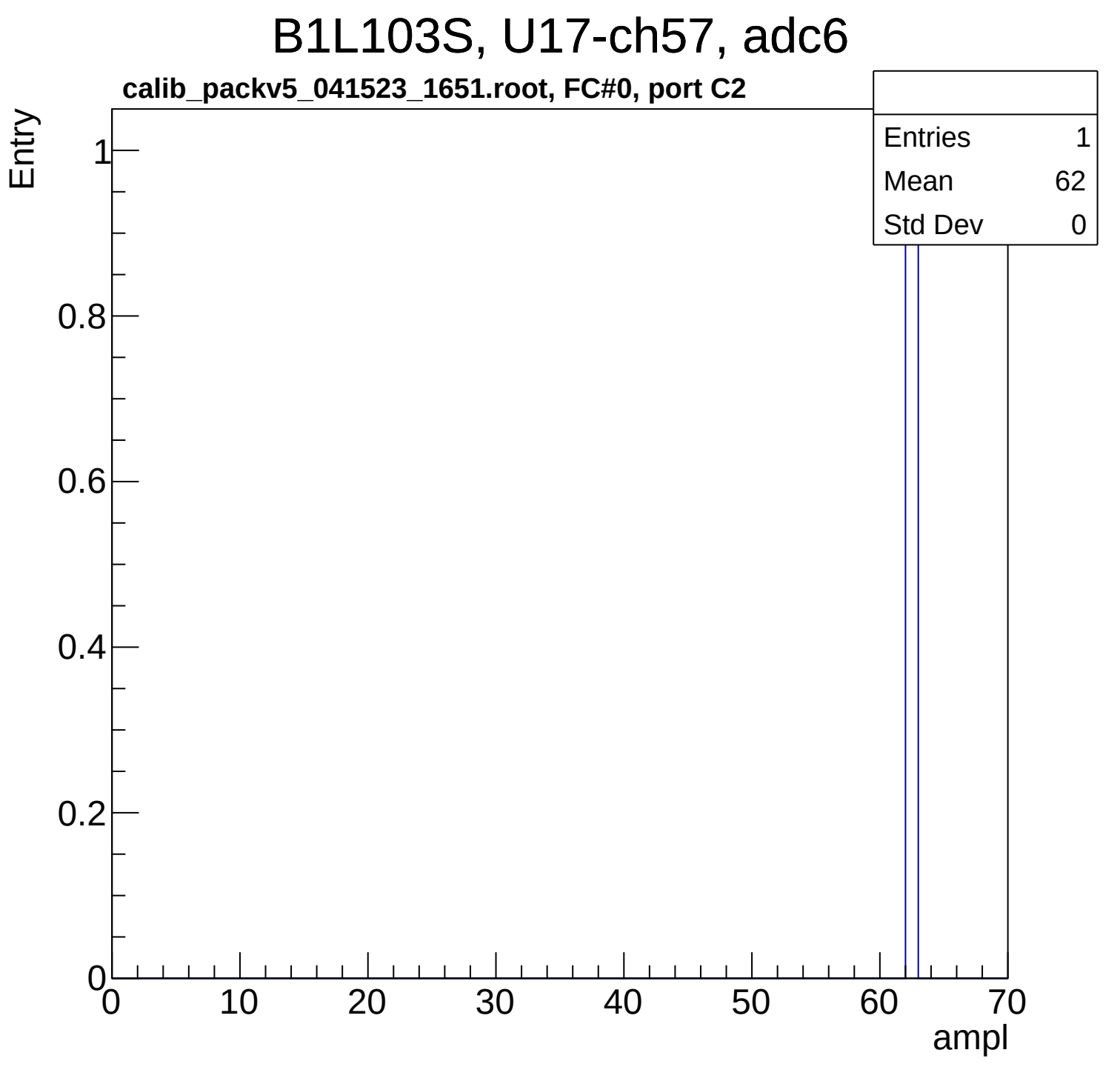
0
10
20
30
40
50
60
70


B1L103S, U17-ch57, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 1
Mean 62
Std Dev 0
Entry
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0.6
0.4
0.2
0
0
10
20
30
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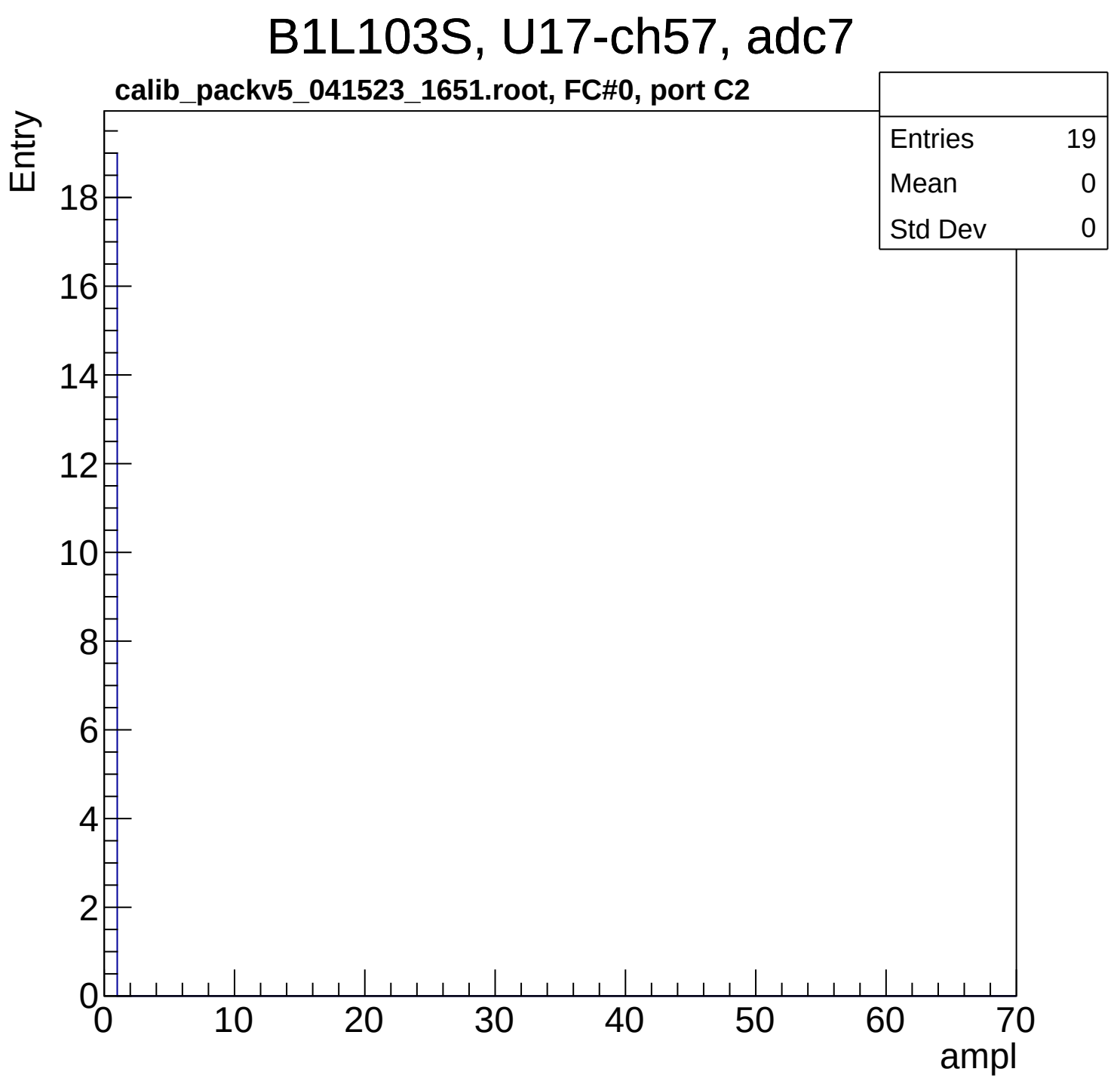
50
60
70
ampl


B1L103S, U17-ch57, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
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10
20
30
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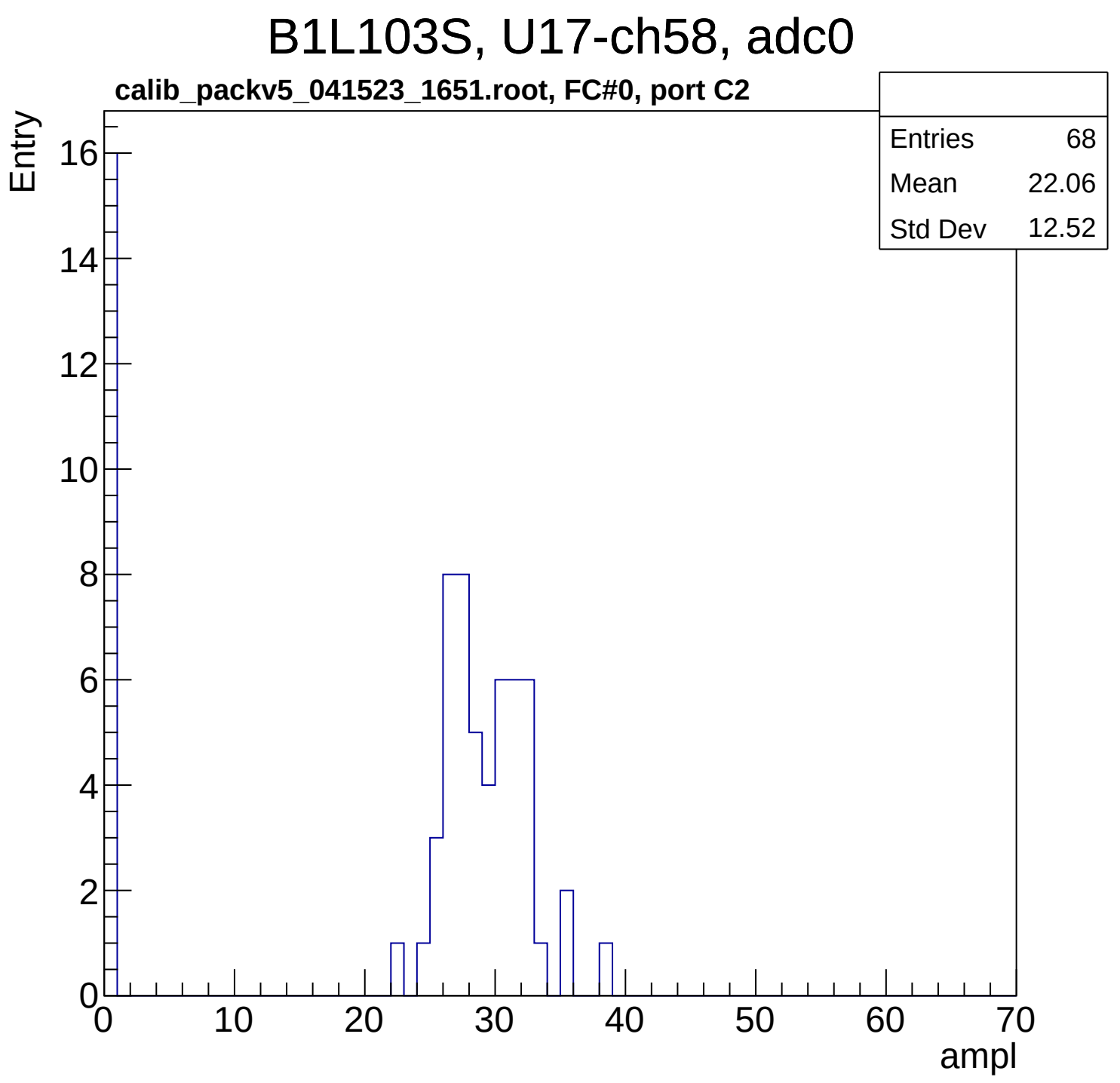
50
60
70
ampl


B1L103S, U17-ch58, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 22.06
Std Dev 12.52
Entry
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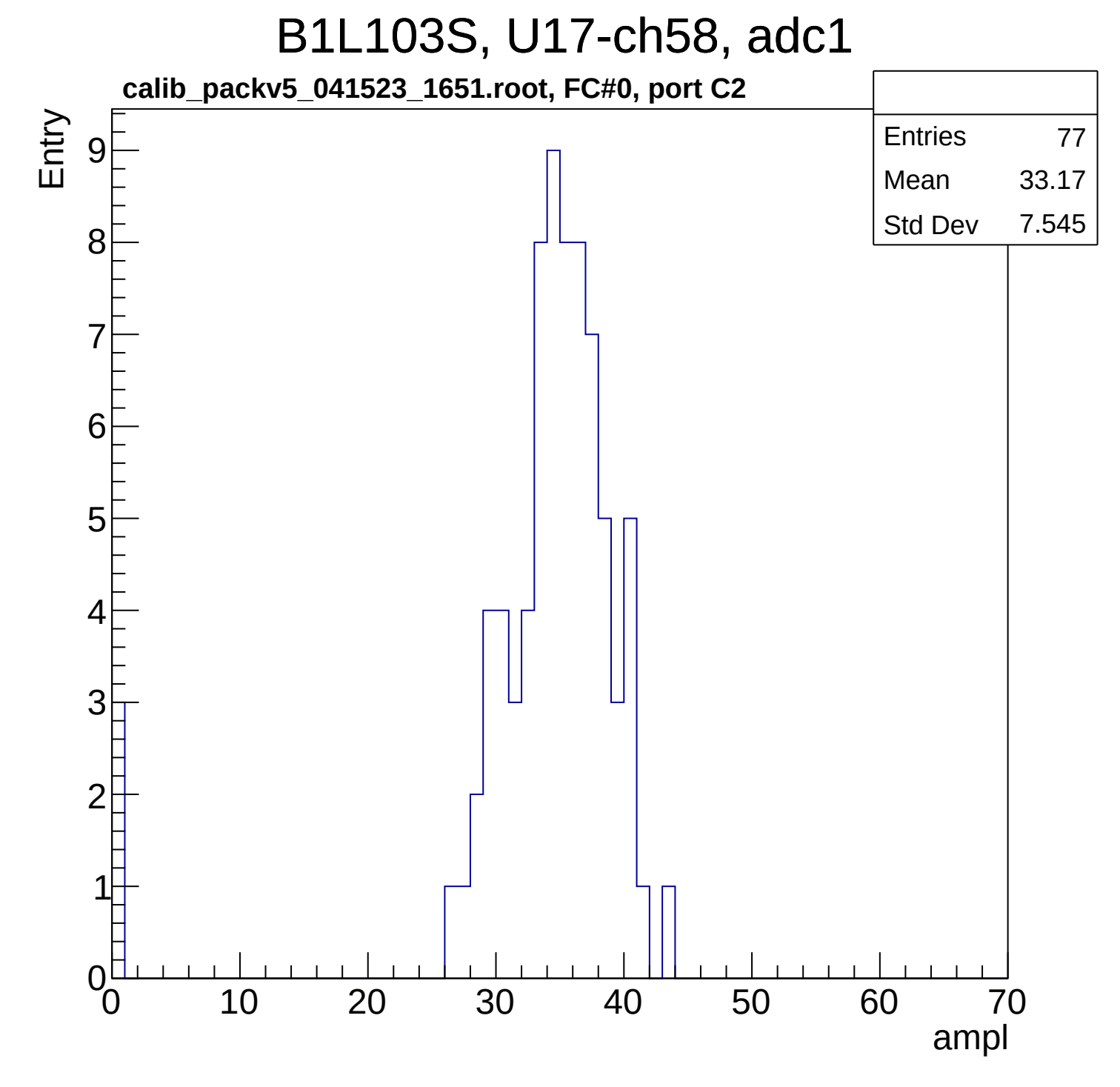
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch58, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 33.17
Std Dev 7.545
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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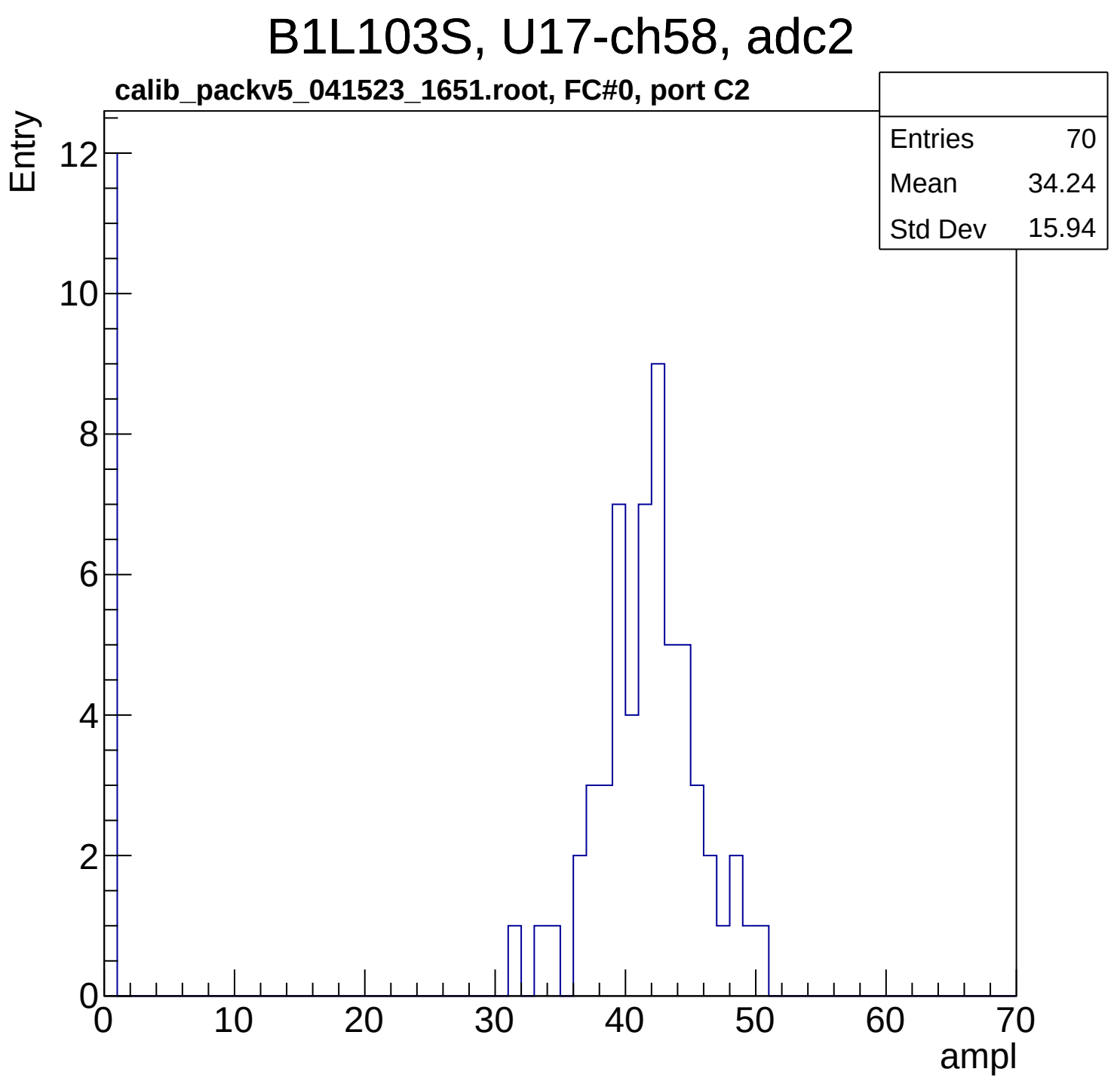
40
50
60
70


B1L103S, U17-ch58, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 34.24
Std Dev 15.94
Entry
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4
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8
10
12
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10
20
30
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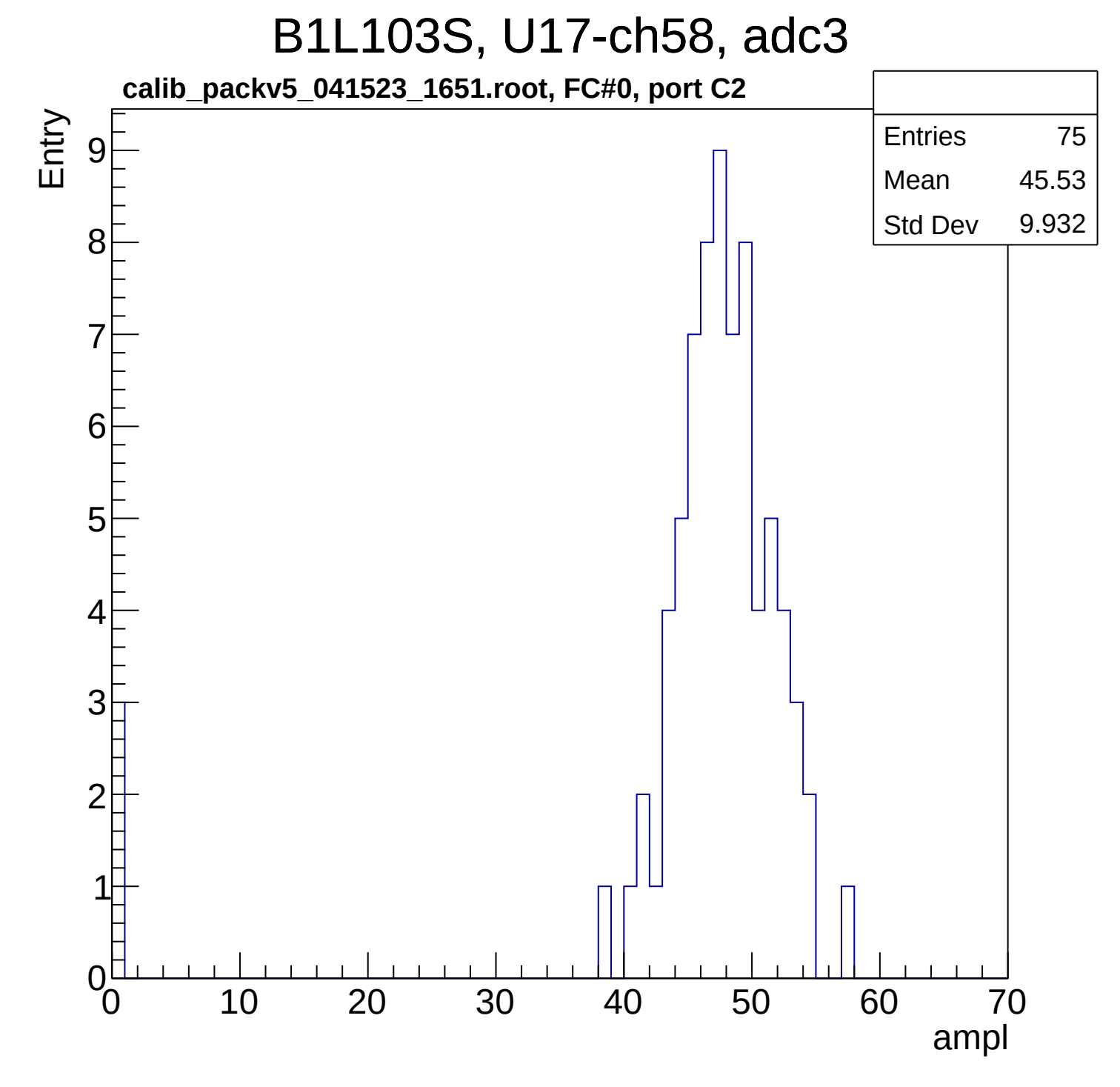
50
60
70
ampl


B1L103S, U17-ch58, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 45.53
Std Dev 9.932
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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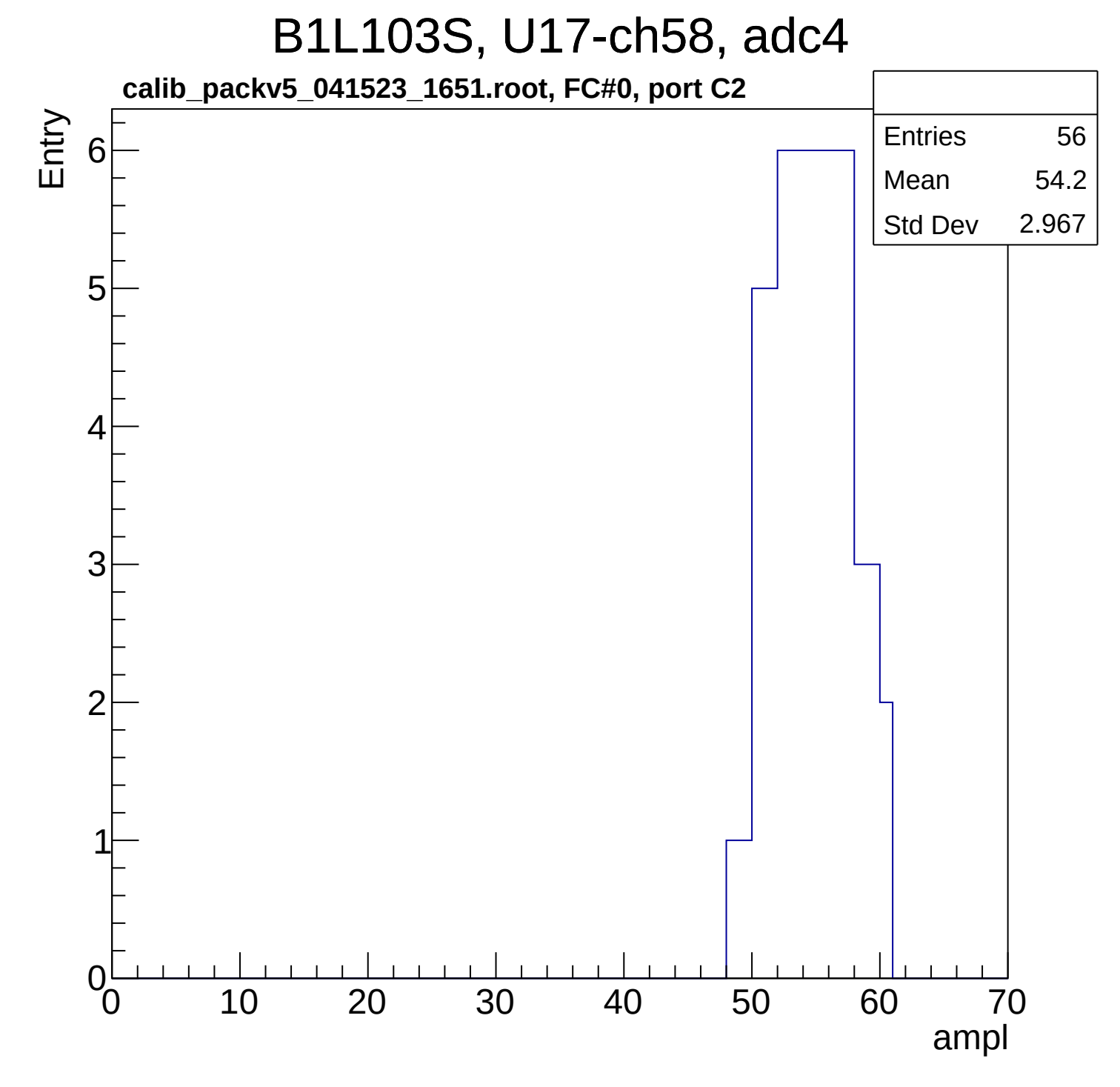
40
50
60
70


B1L103S, U17-ch58, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 54.2
Std Dev 2.967
Entry
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2
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4
5
6
0
10
20
30
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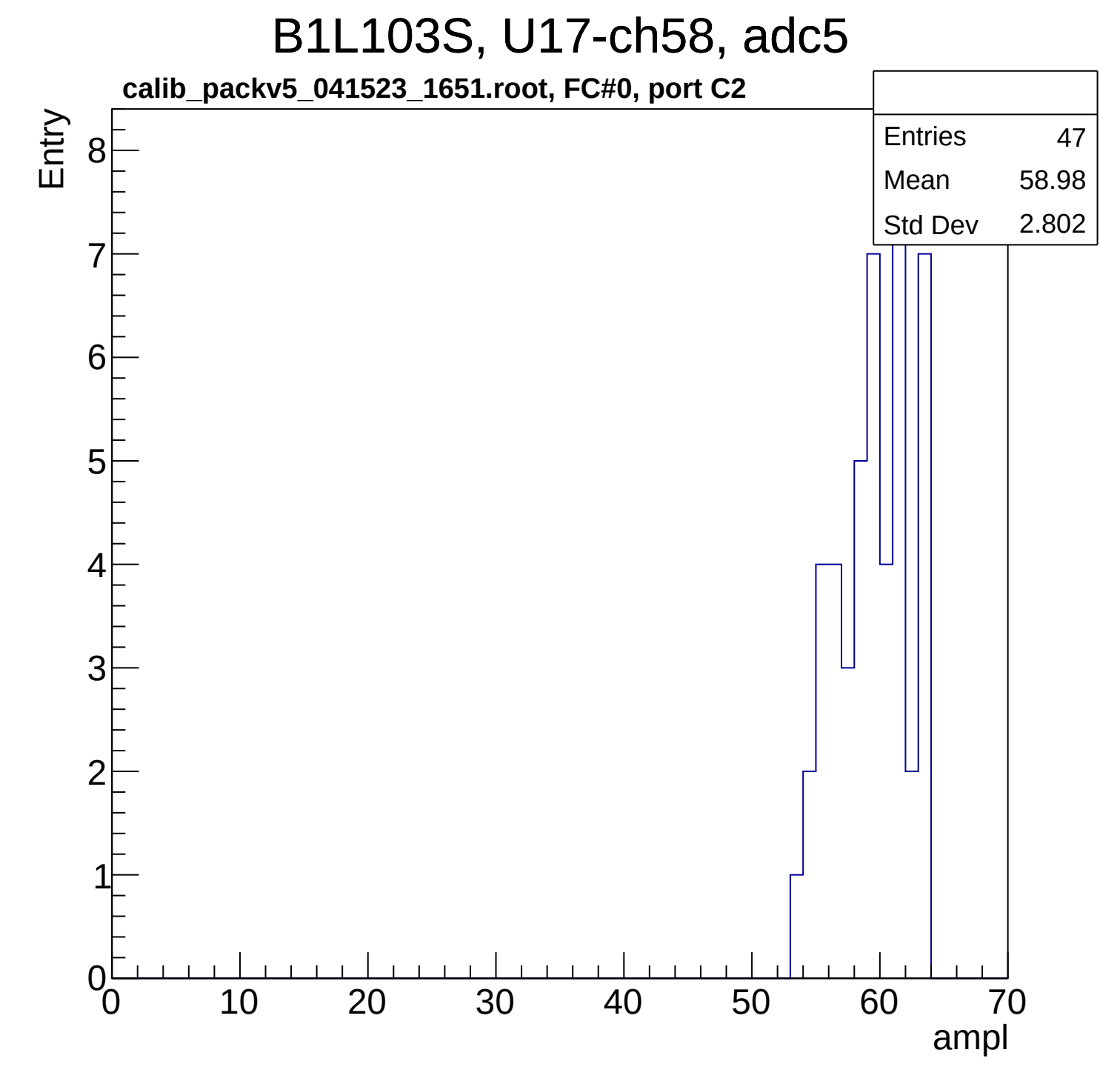
50
60
70
ampl


B1L103S, U17-ch58, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 58.98
Std Dev 2.802
Entry
ampl
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2
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6
7
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60
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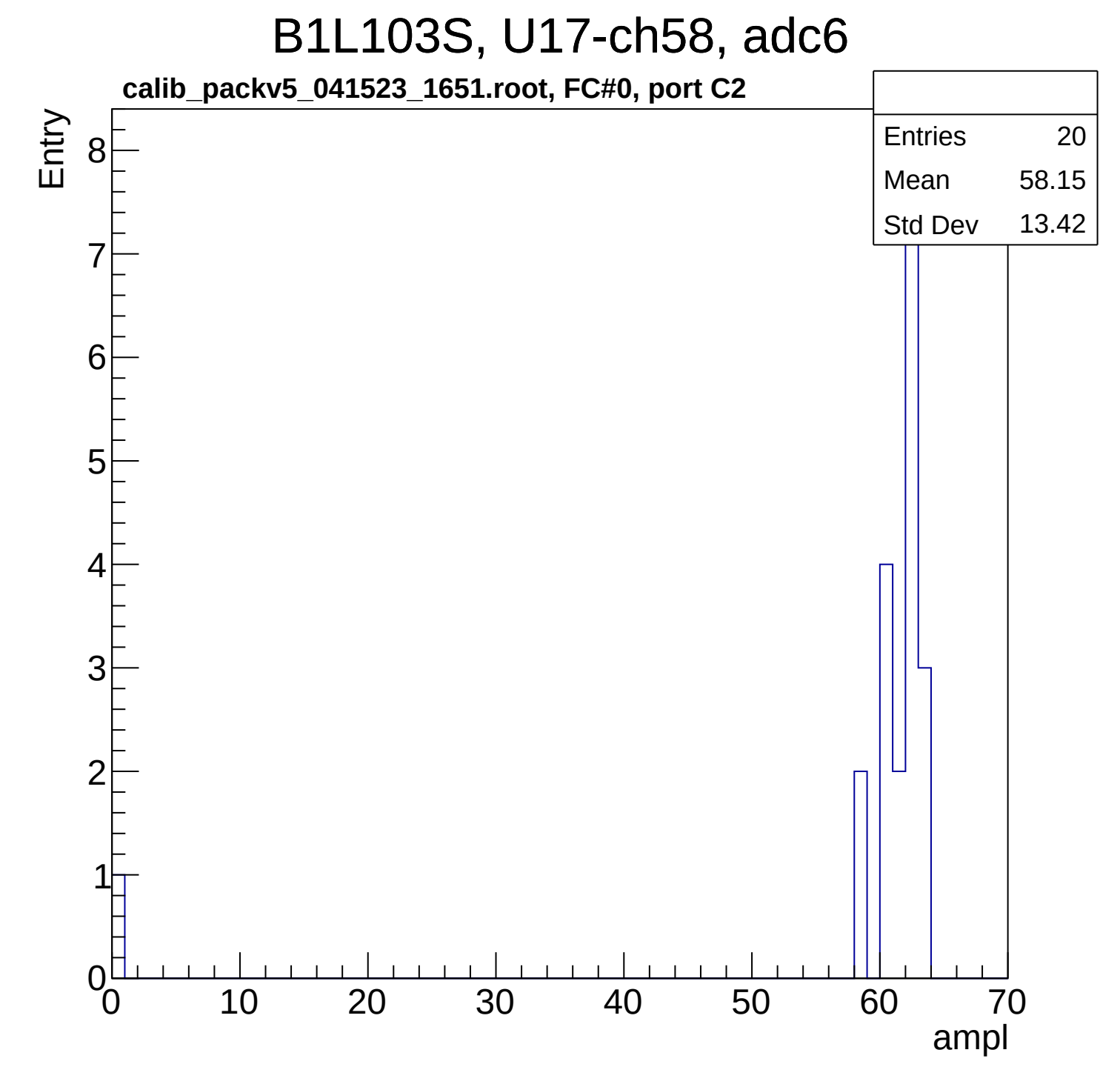
B1L103S, U17-ch58, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 58.15
Std Dev 13.42
Entry
ampl
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2
3
4
5
6
7
8
0
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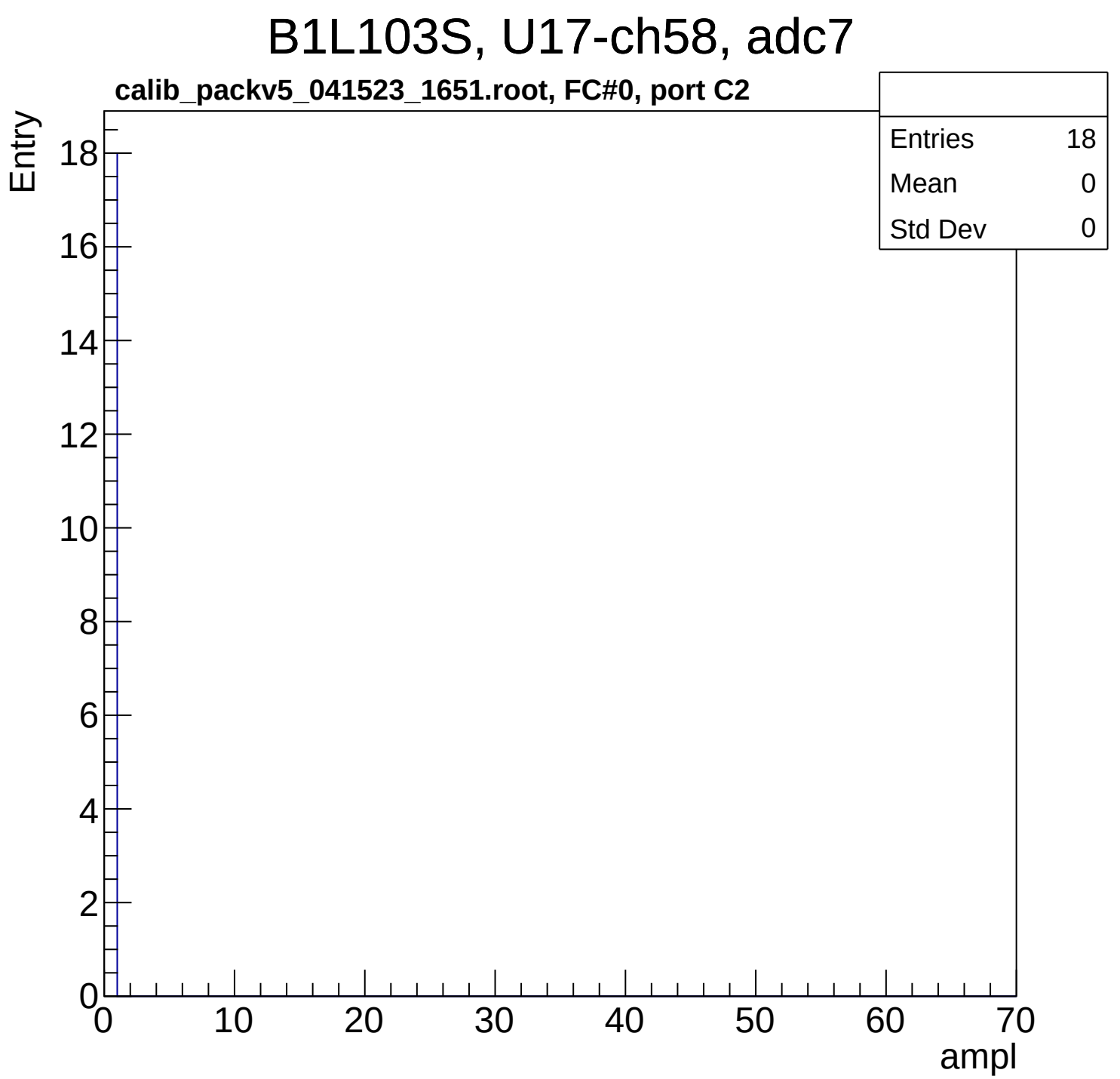
60
70


B1L103S, U17-ch58, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
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6
8
10
12
14
16
18
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10
20
30
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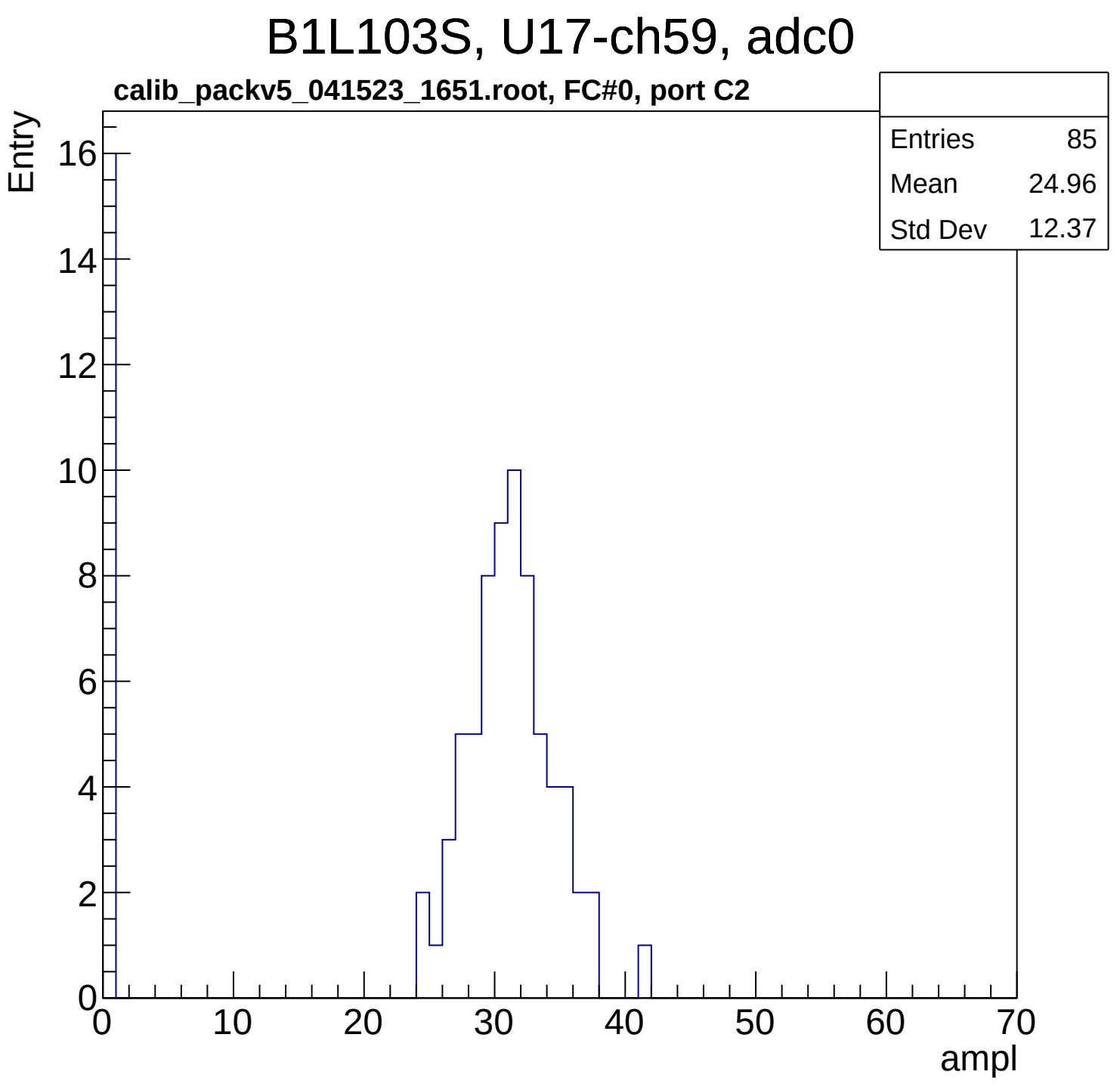
50
60
70
ampl


B1L103S, U17-ch59, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 24.96
Std Dev 12.37
Entry
ampl
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4
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10
12
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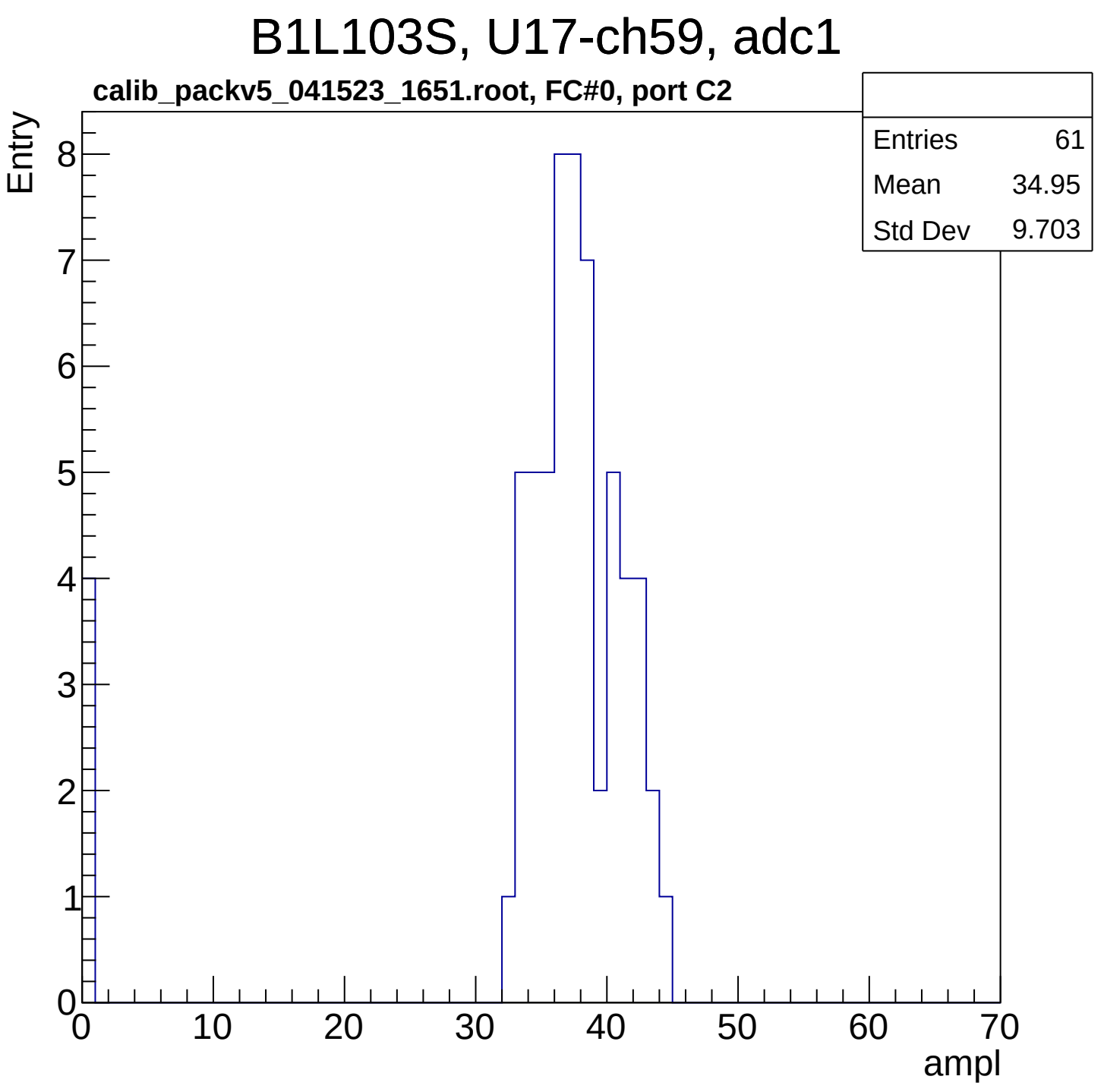
B1L103S, U17-ch59, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 34.95
Std Dev 9.703
Entry
ampl
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2
3
4
5
6
7
8
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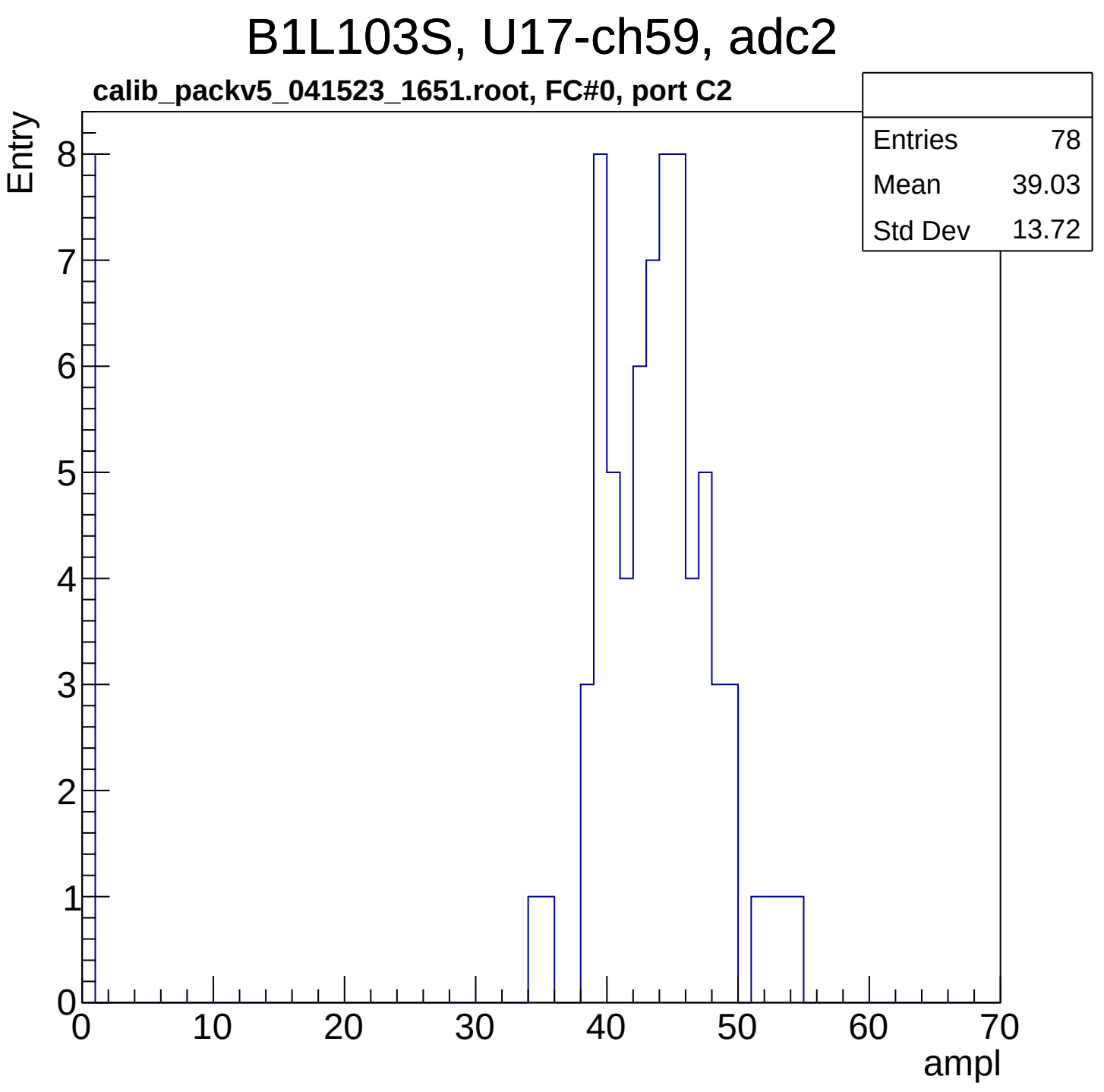
B1L103S, U17-ch59, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 39.03
Std Dev 13.72
Entry
ampl
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3
4
5
6
7
8
0
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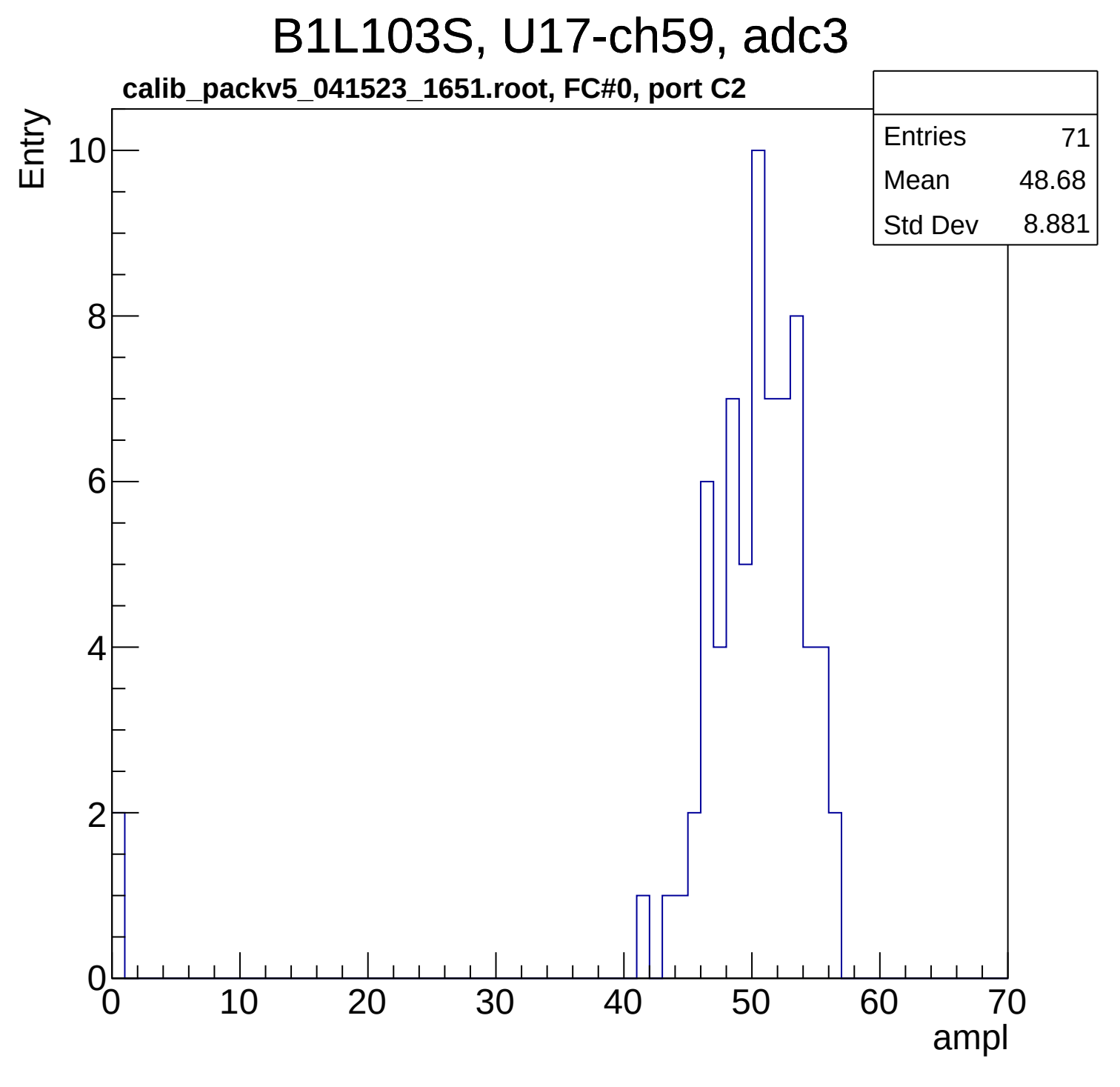
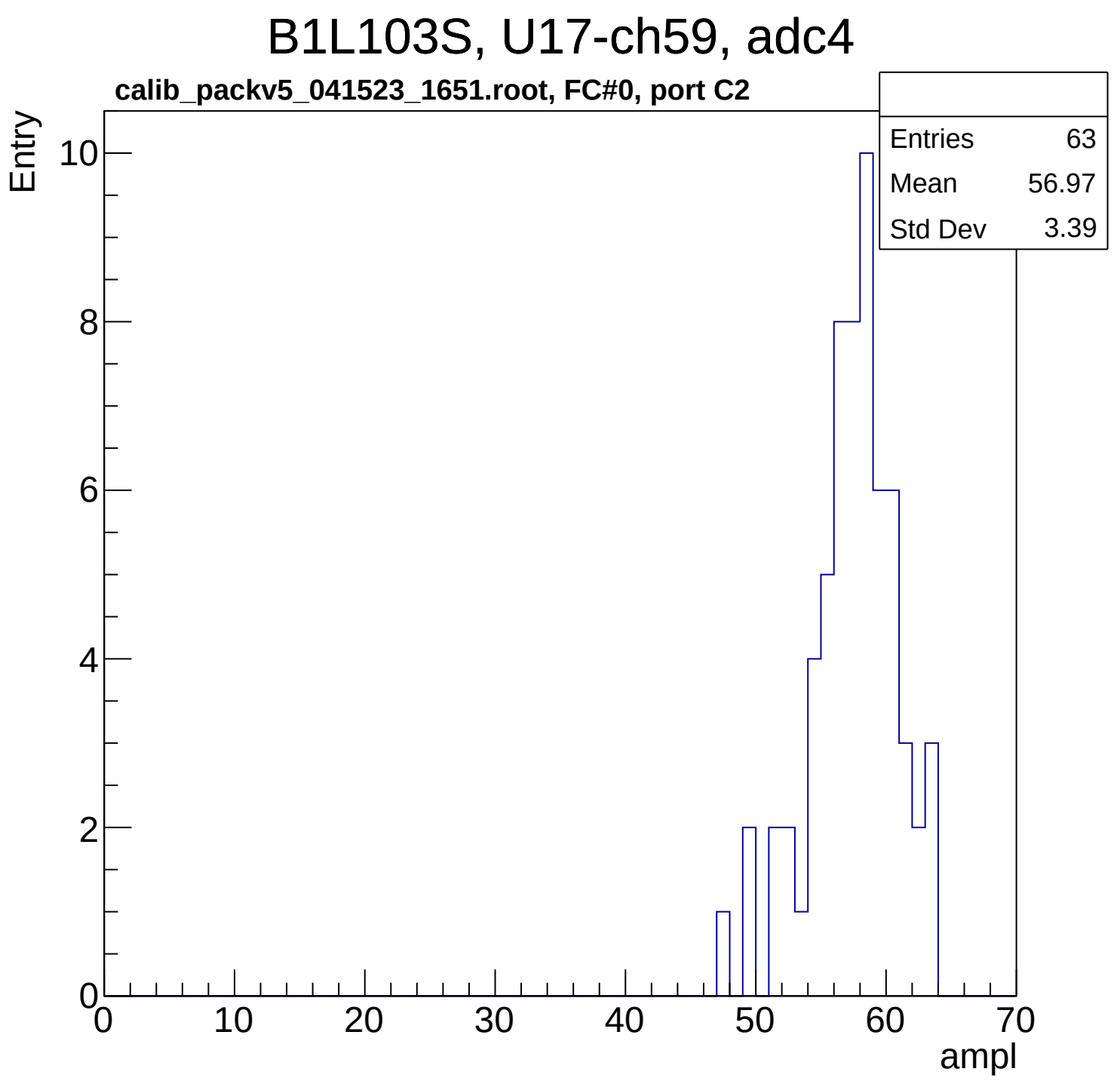
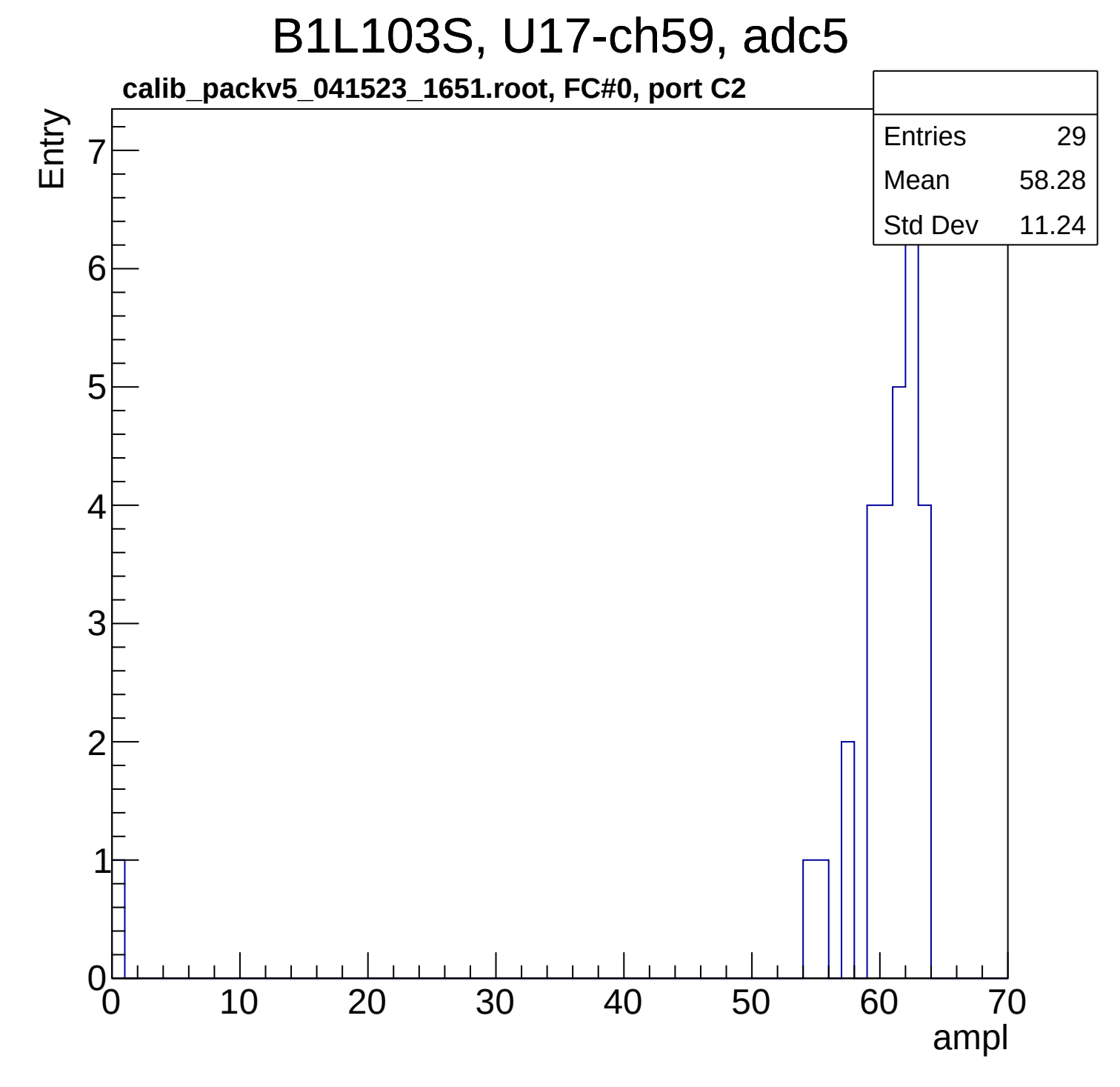
70


B1L103S, U17-ch59, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 48.68
Std Dev 8.881
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U17-ch59, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 56.97
Std Dev 3.39
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch59, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 29
Mean 58.28
Std Dev 11.24
Entry
ampl
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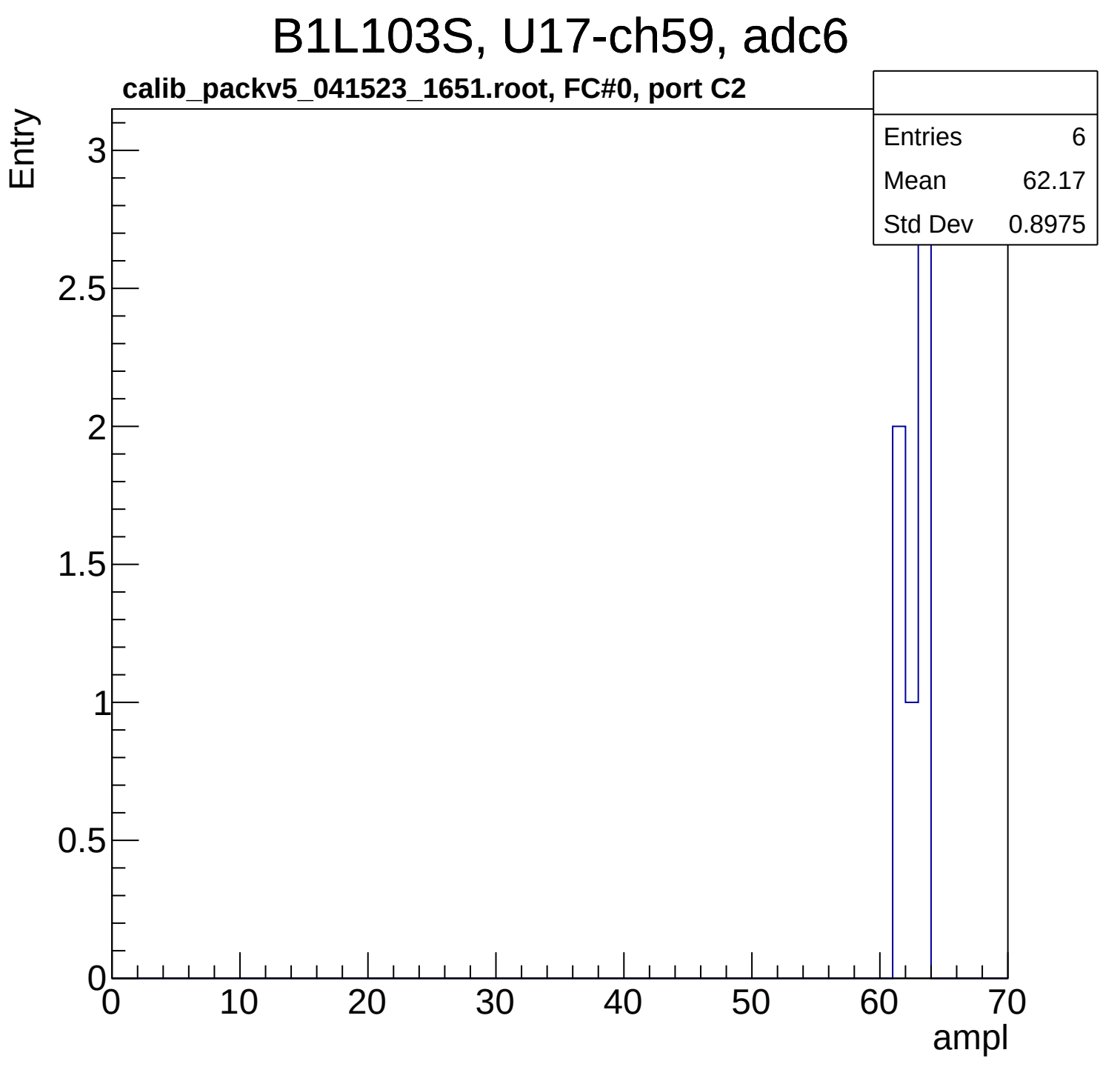
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U17-ch59, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 62.17
Std Dev 0.8975
Entry
ampl
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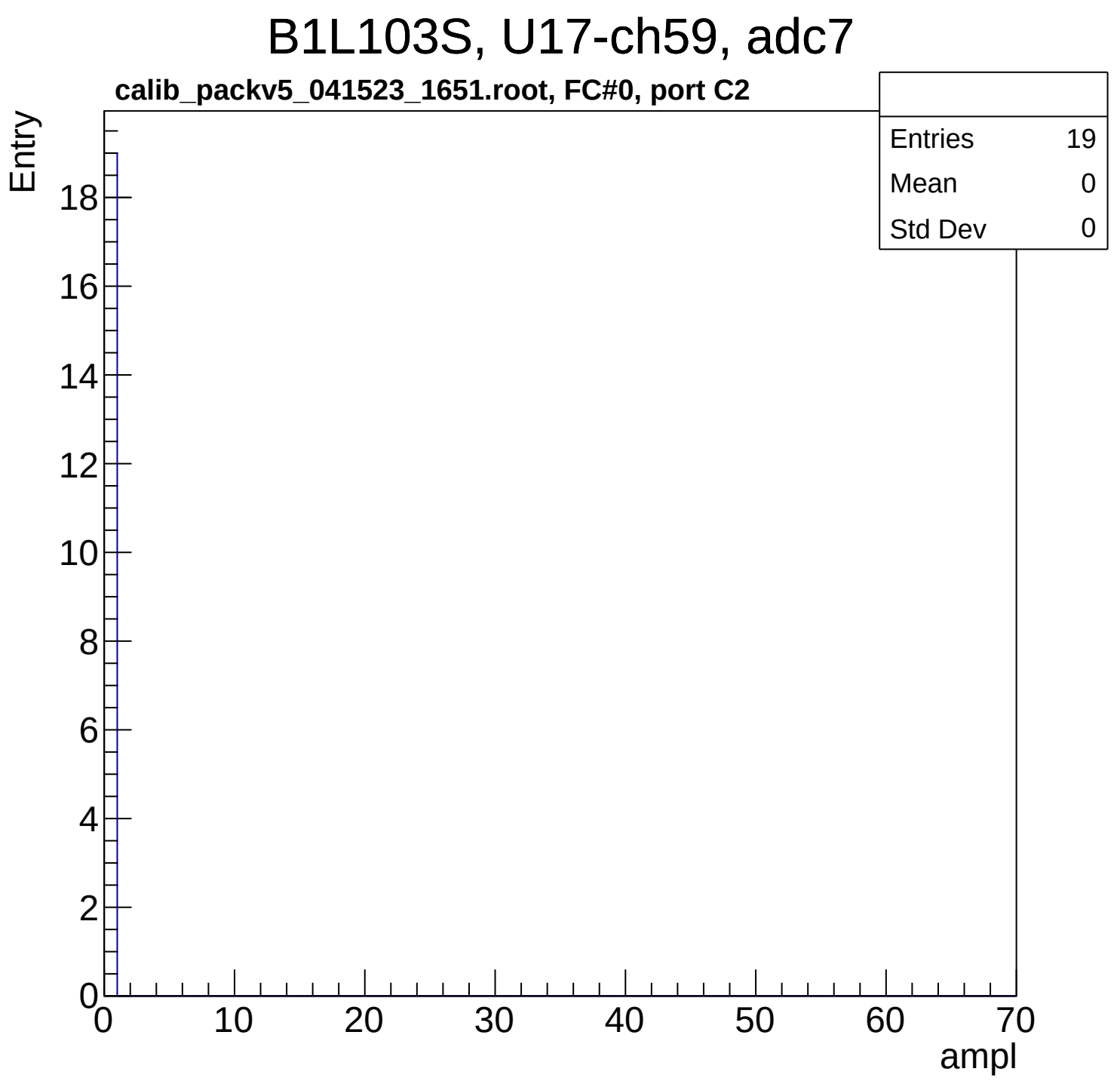
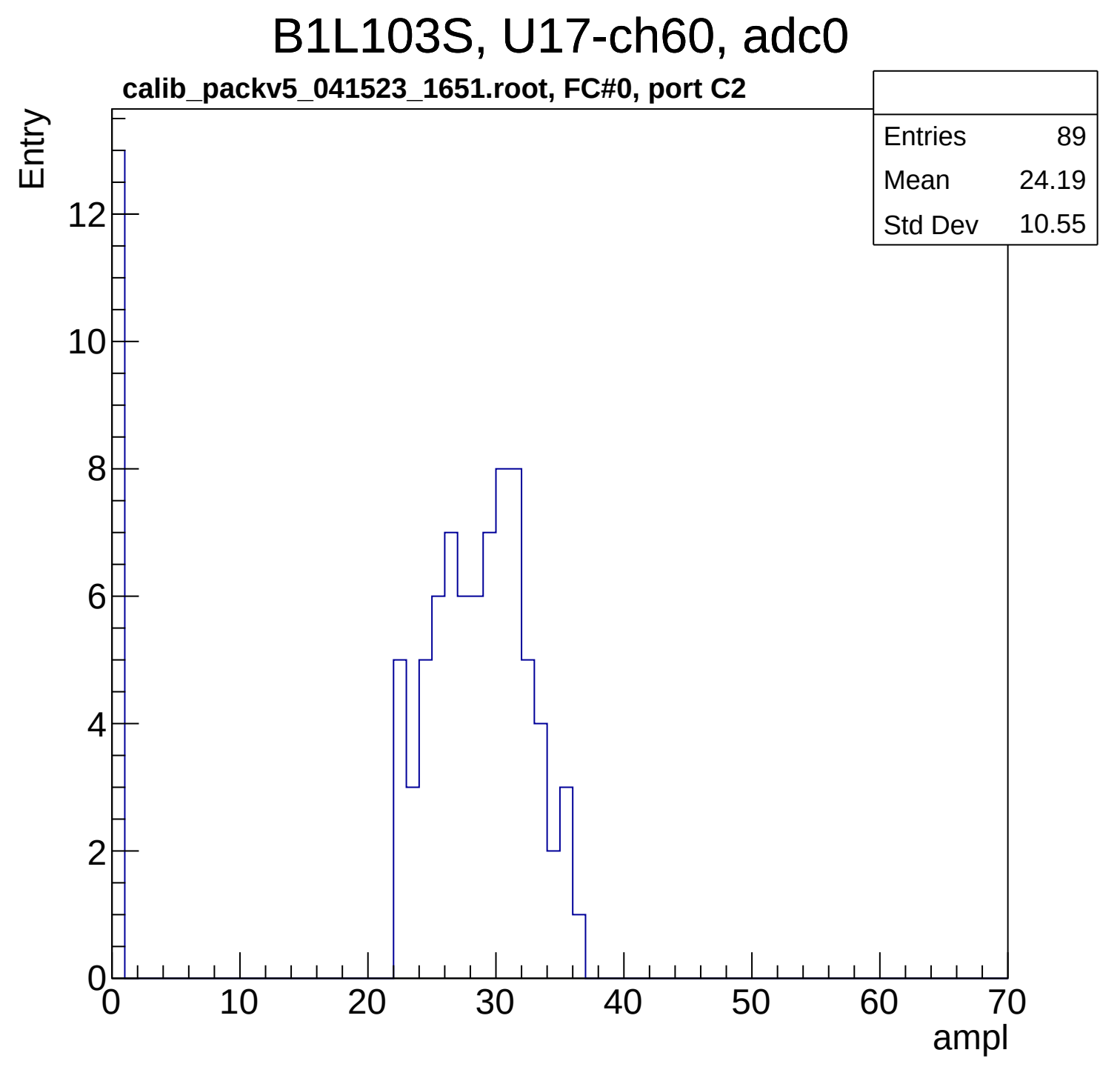
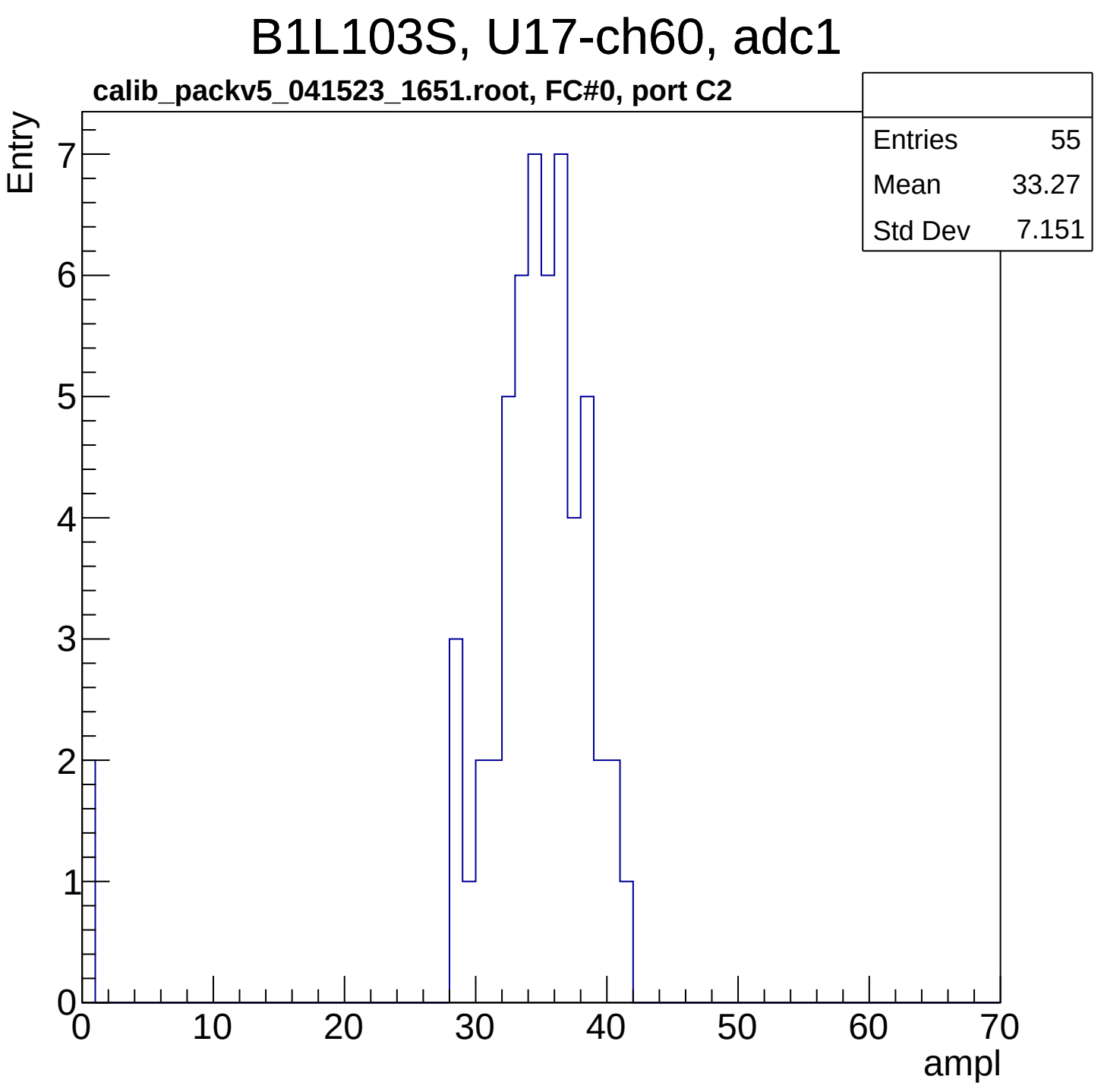
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U17-ch59, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch60, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 89
Mean 24.19
Std Dev 10.55
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70


B1L103S, U17-ch60, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 33.27
Std Dev 7.151
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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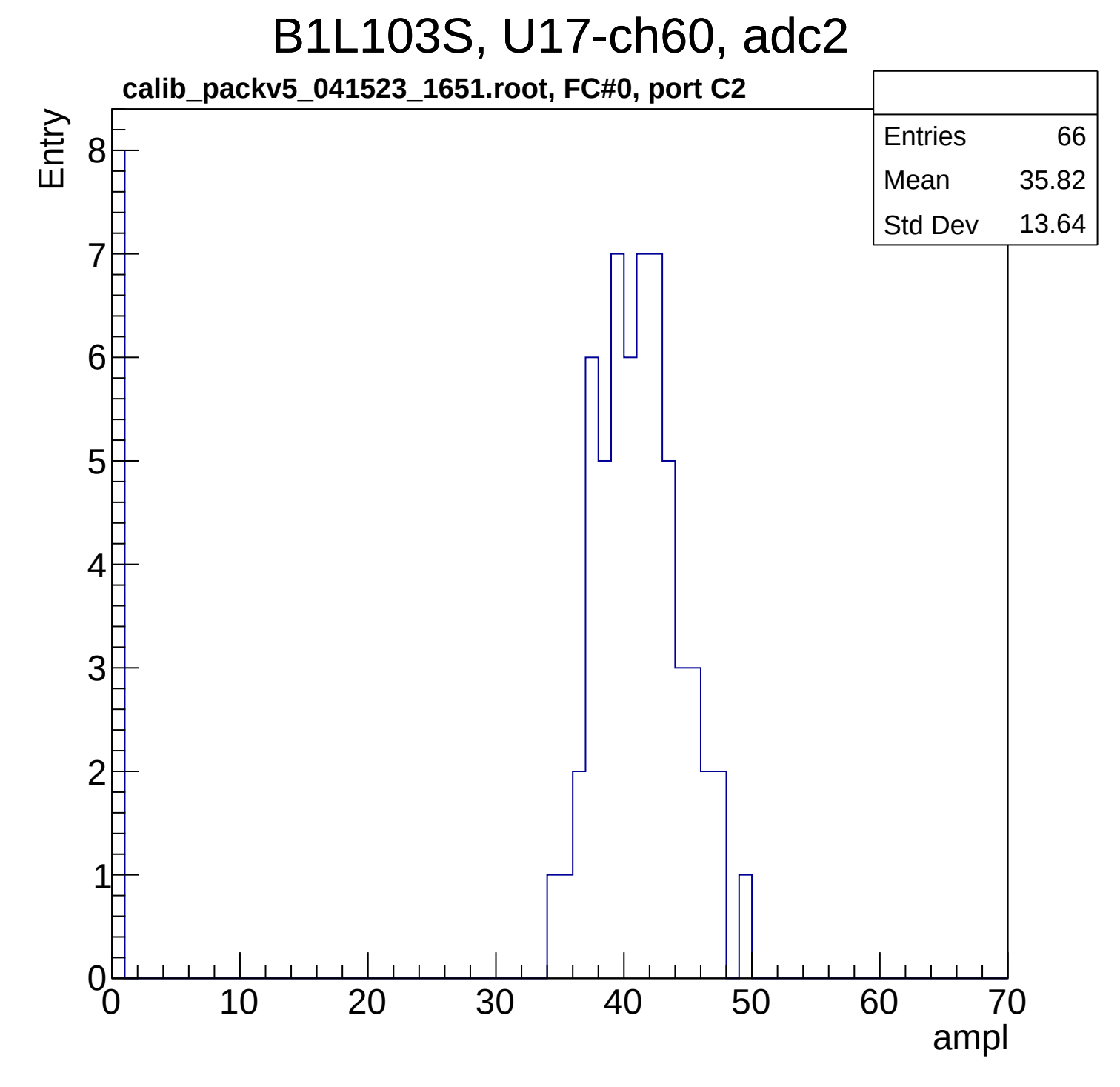
B1L103S, U17-ch60, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 35.82
Std Dev 13.64
Entry
ampl
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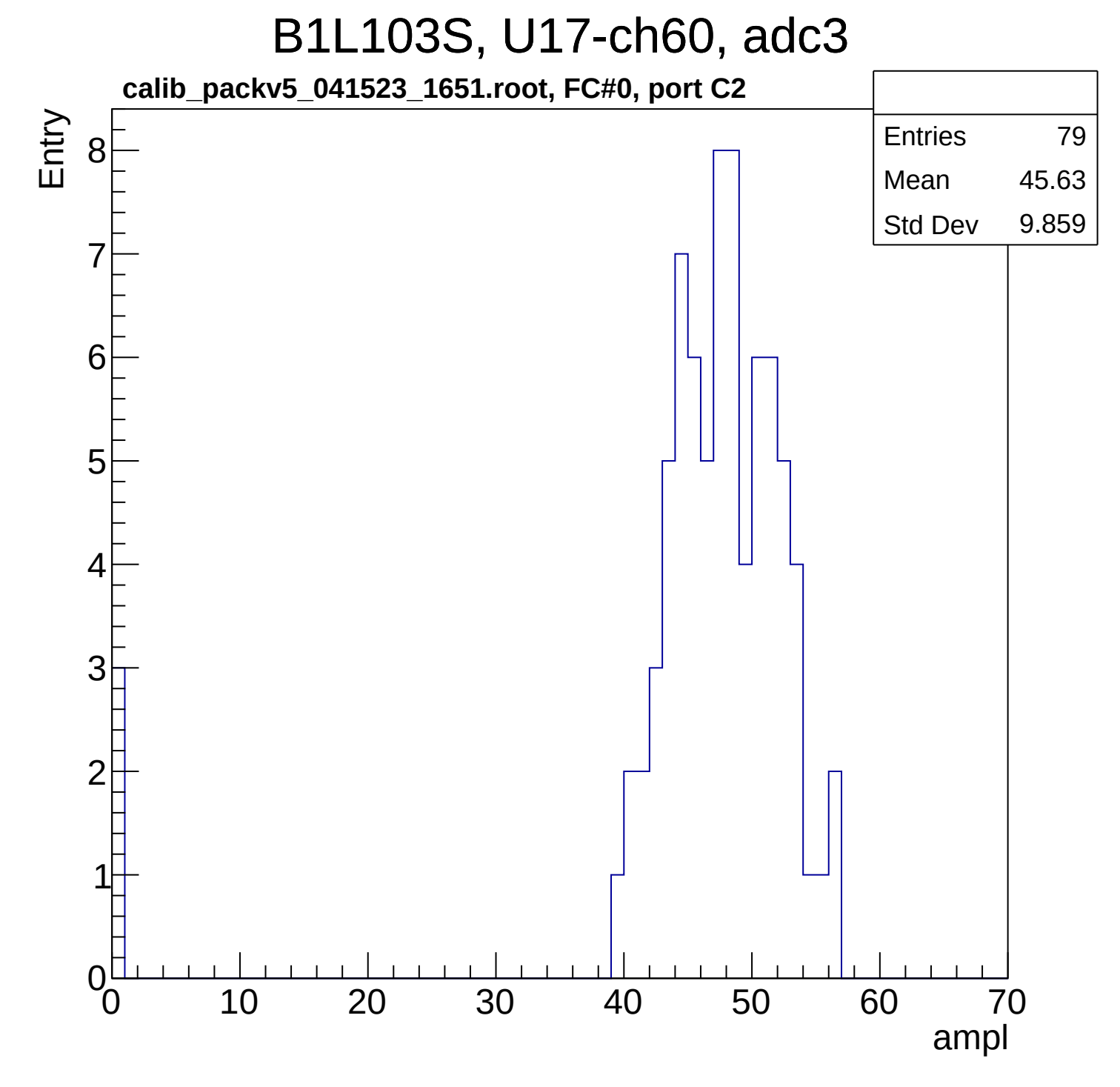
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U17-ch60, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 45.63
Std Dev 9.859
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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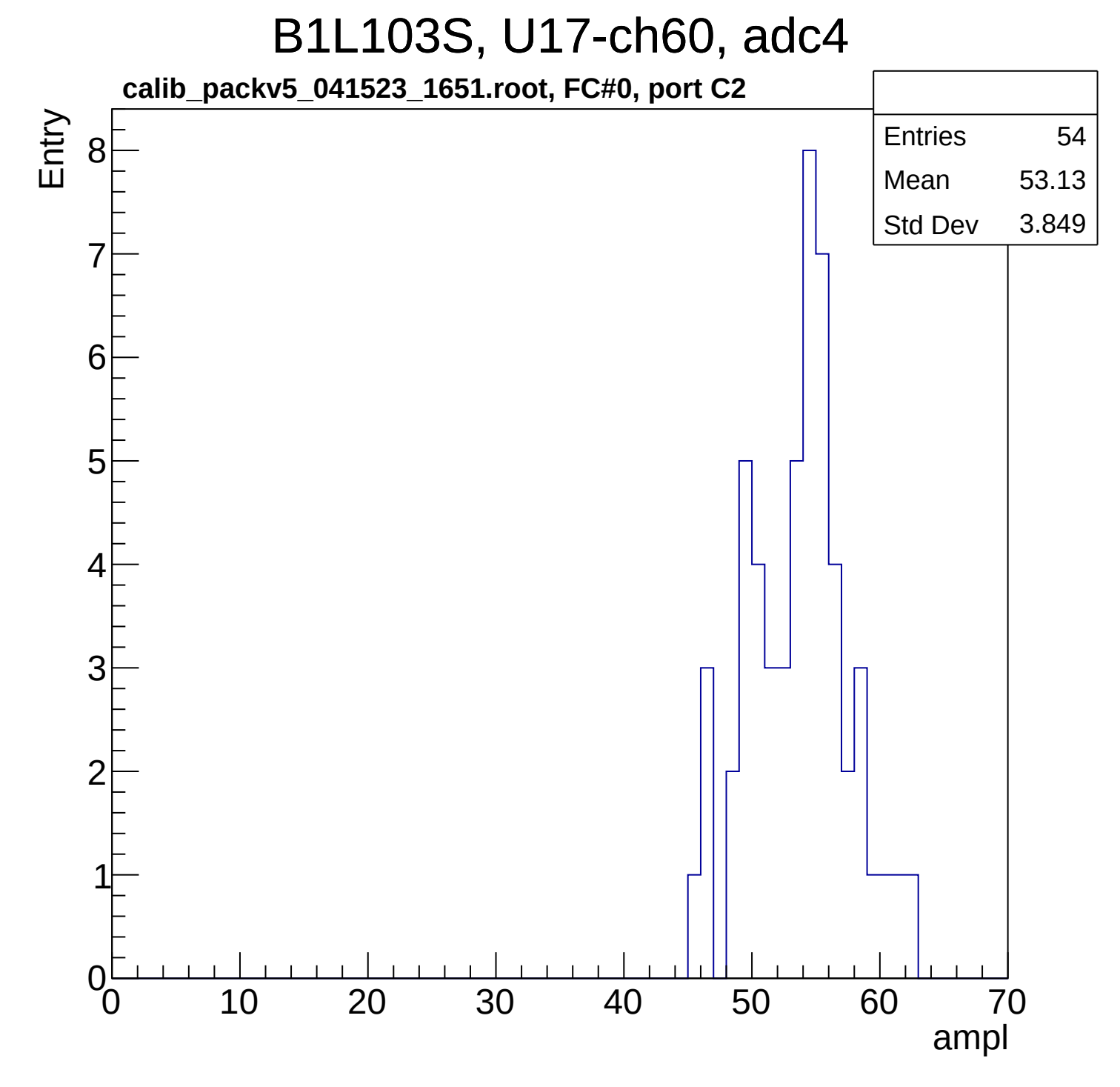
B1L103S, U17-ch60, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 53.13
Std Dev 3.849
Entry
ampl
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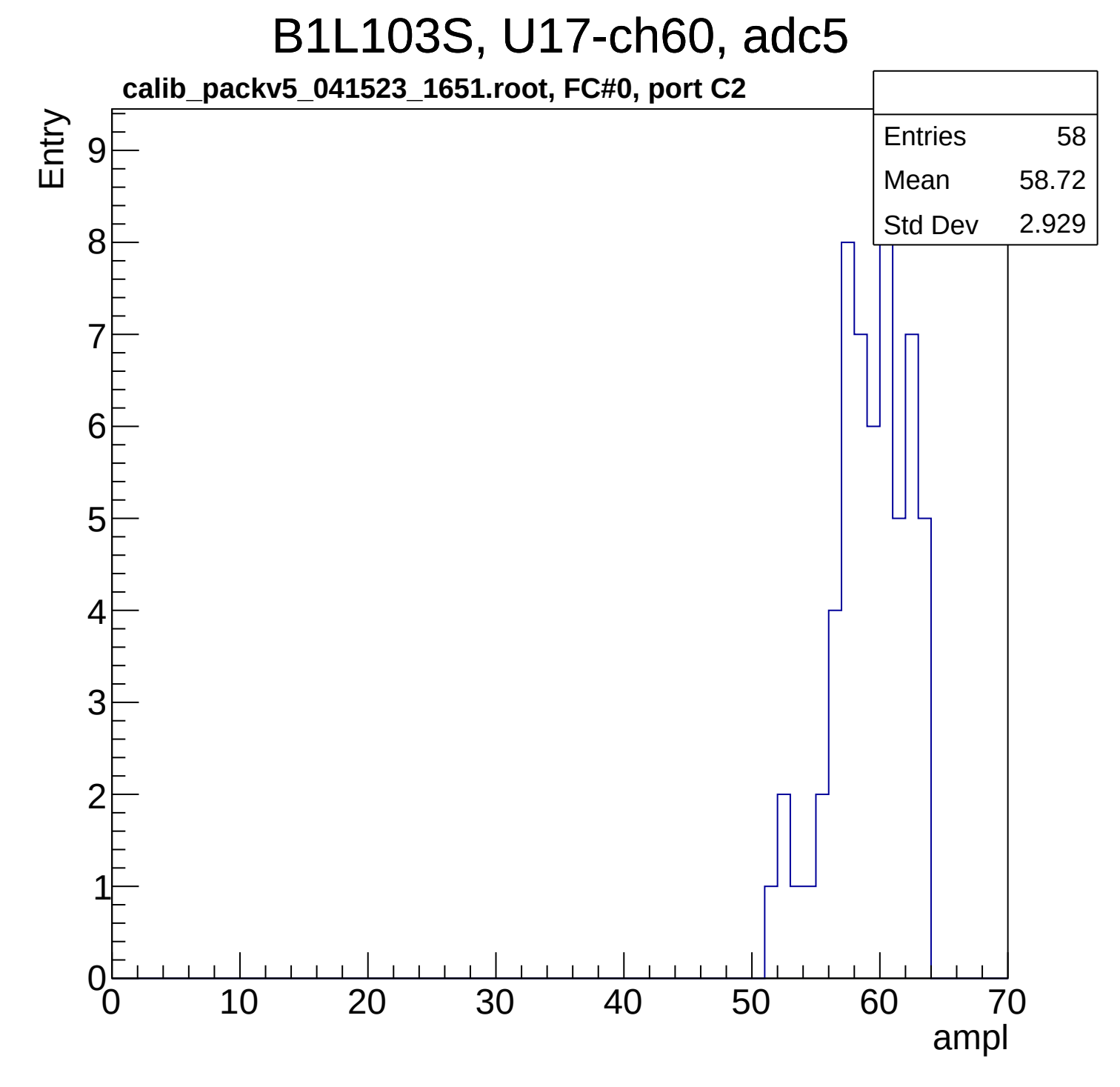
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U17-ch60, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 58.72
Std Dev 2.929
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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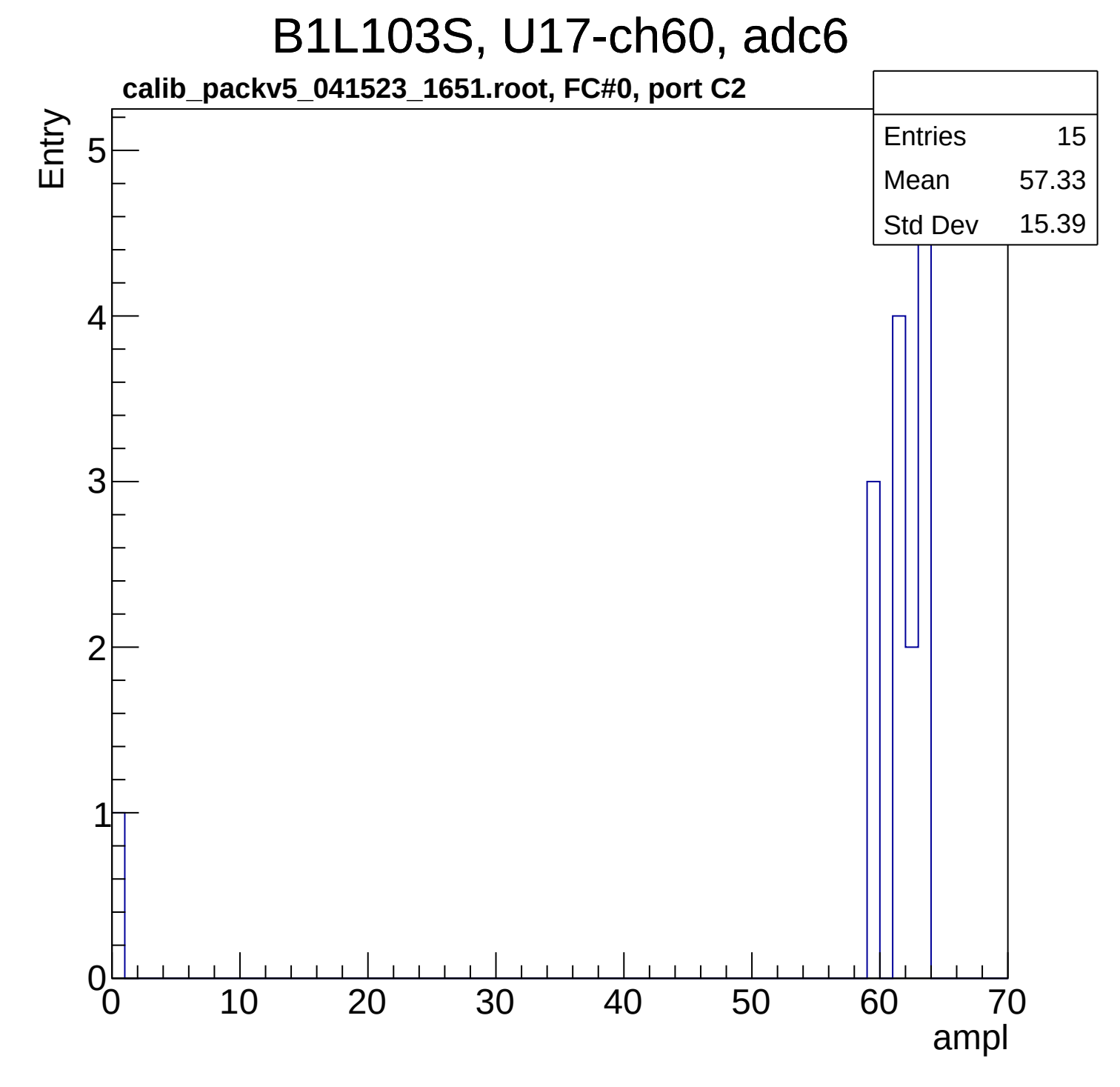
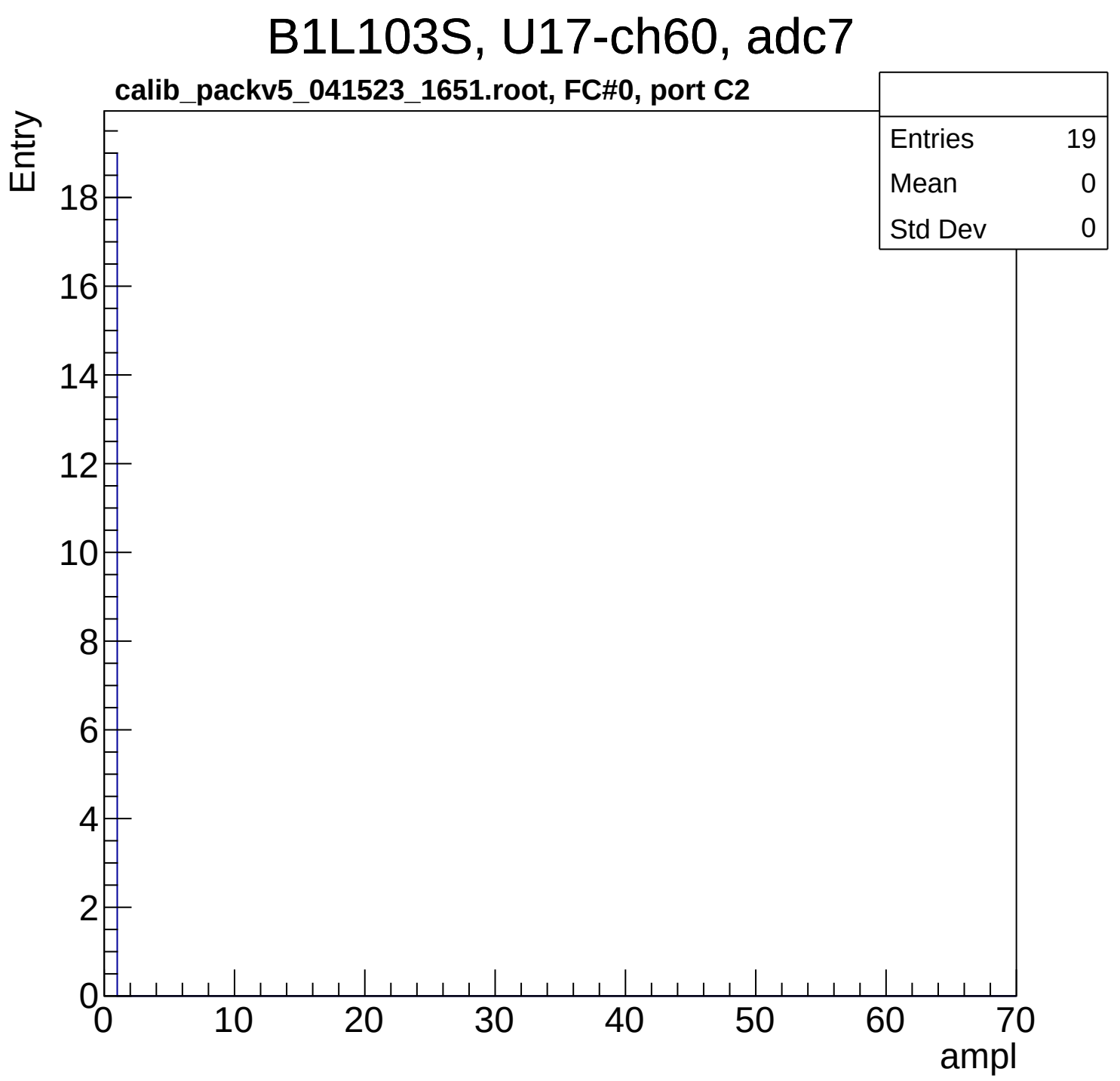
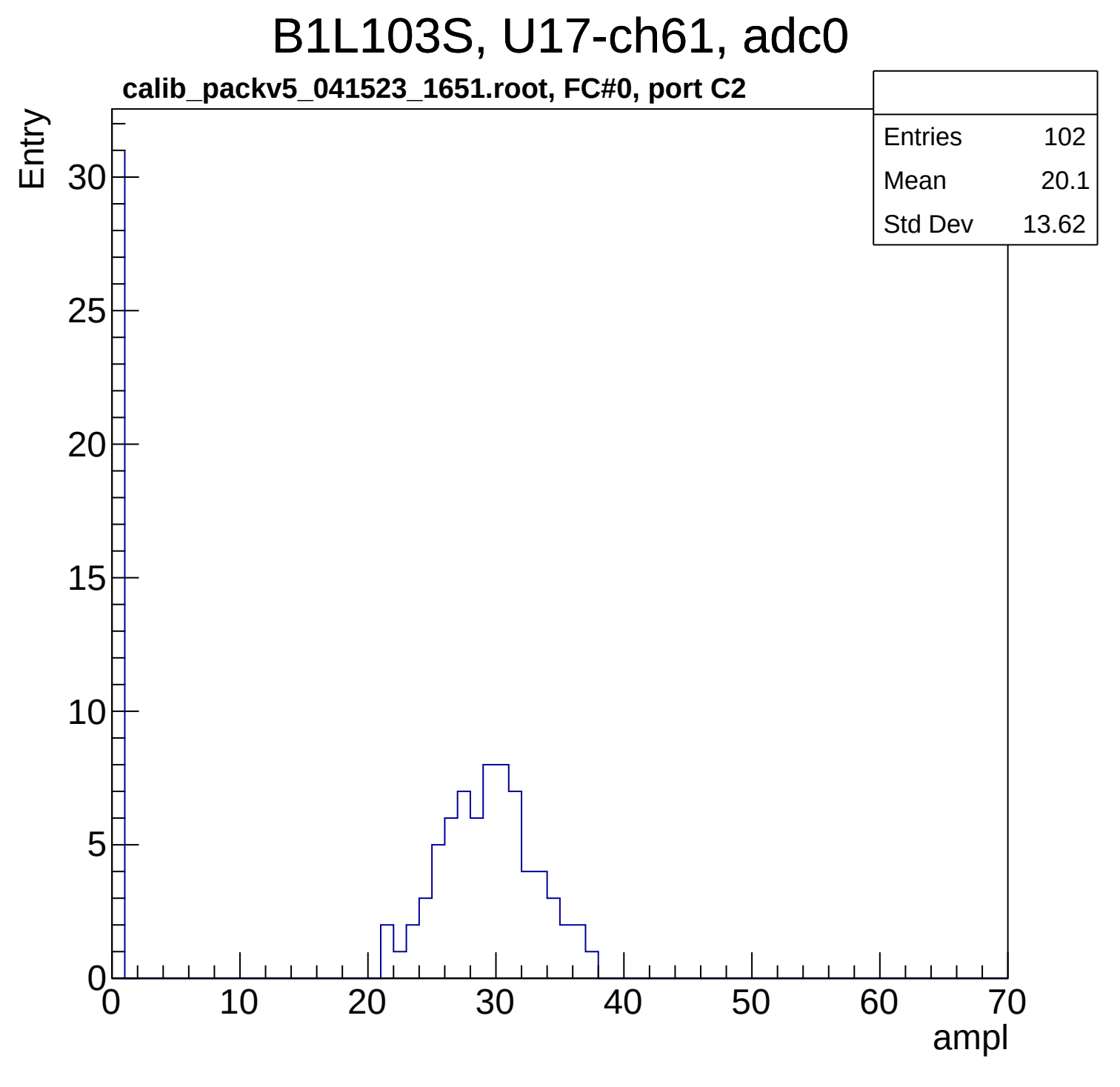
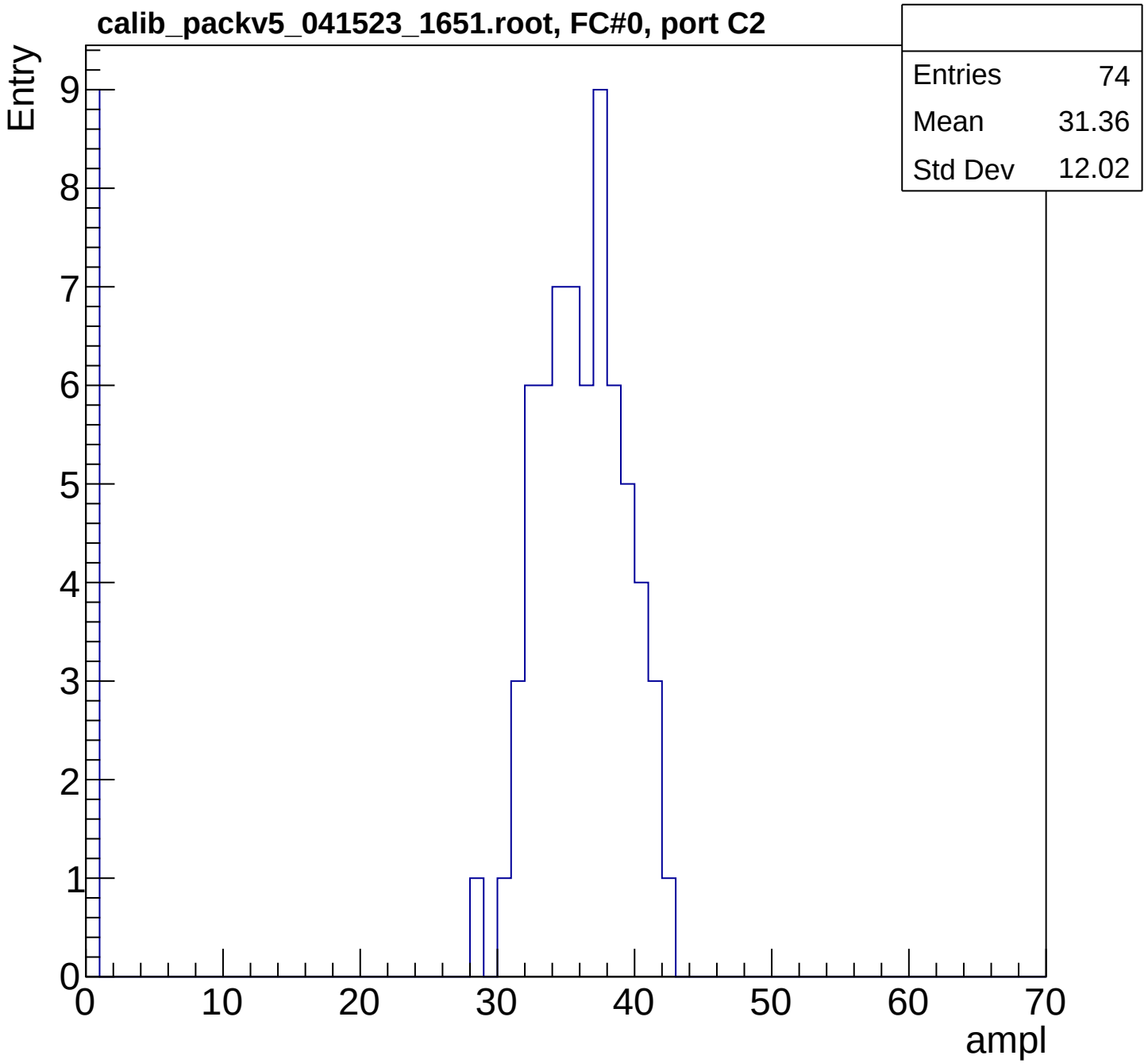

B1L103S, U17-ch60, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 15
Mean 57.33
Std Dev 15.39
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U17-ch60, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch61, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 102
Mean 20.1
Std Dev 13.62
Entry
0
5
10
15
20
25
30
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch61, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 31.36
Std Dev 12.02
Entry
ampl
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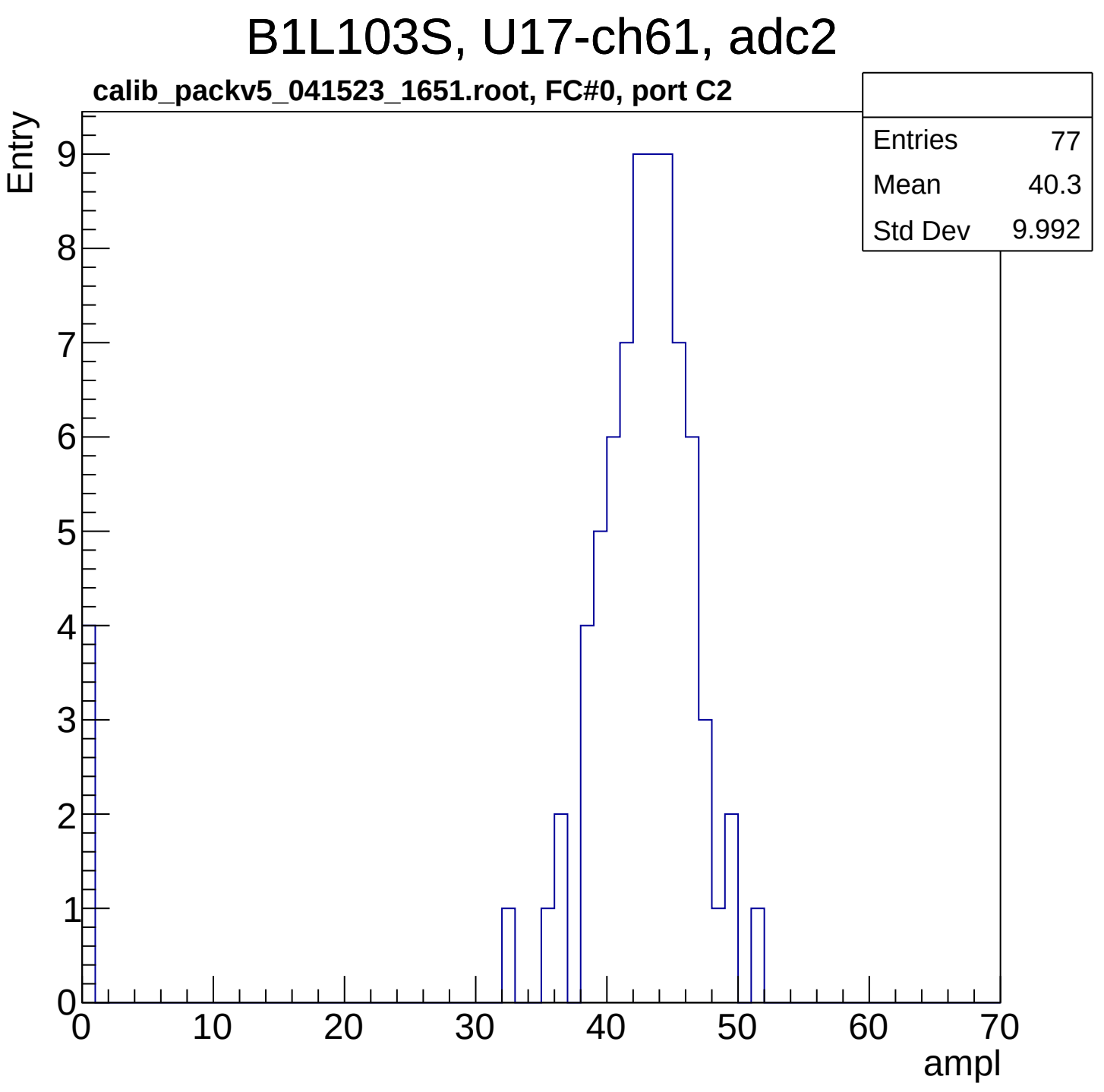
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U17-ch61, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 40.3
Std Dev 9.992
Entry
ampl
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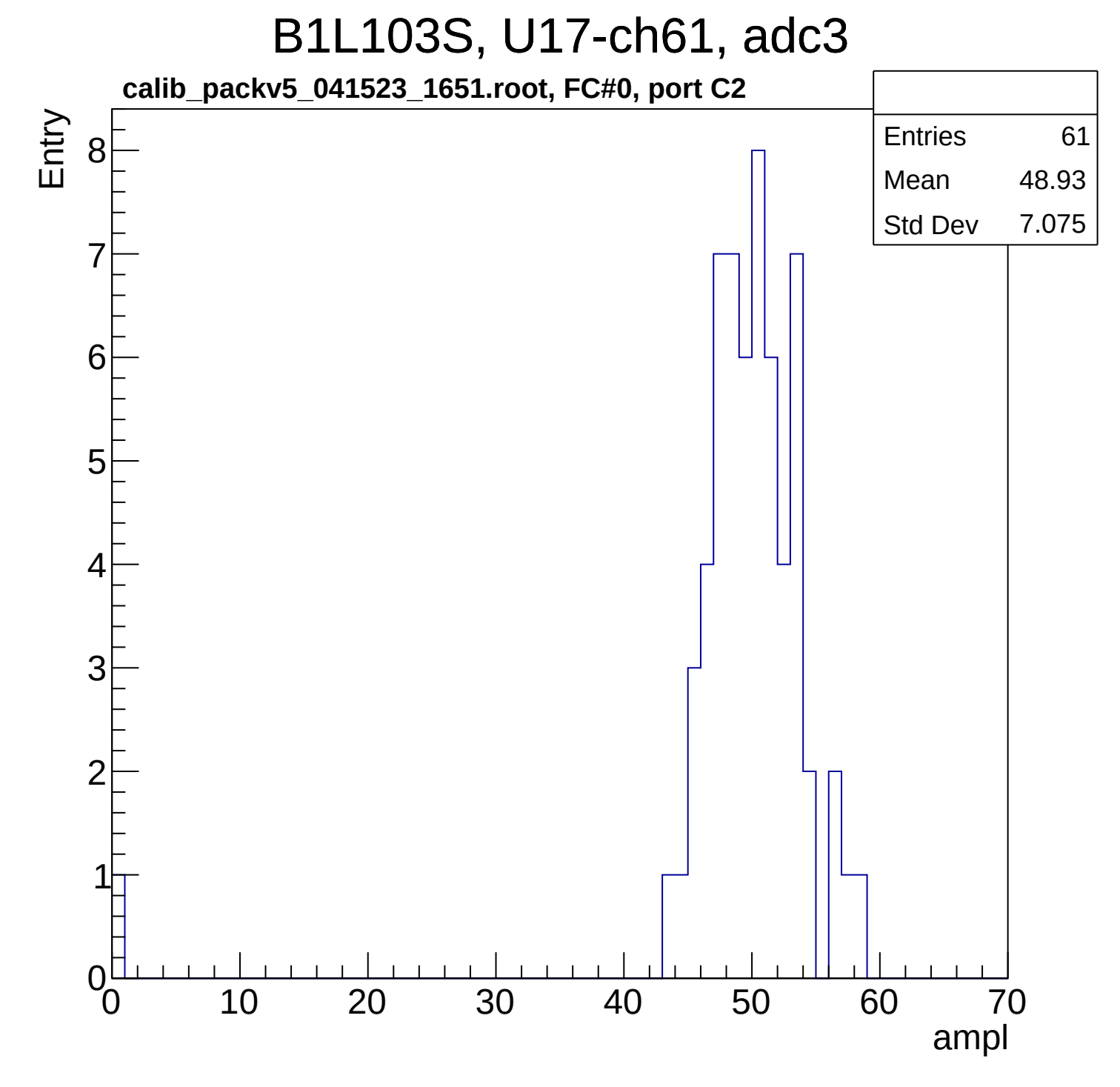
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U17-ch61, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 48.93
Std Dev 7.075
Entry
ampl
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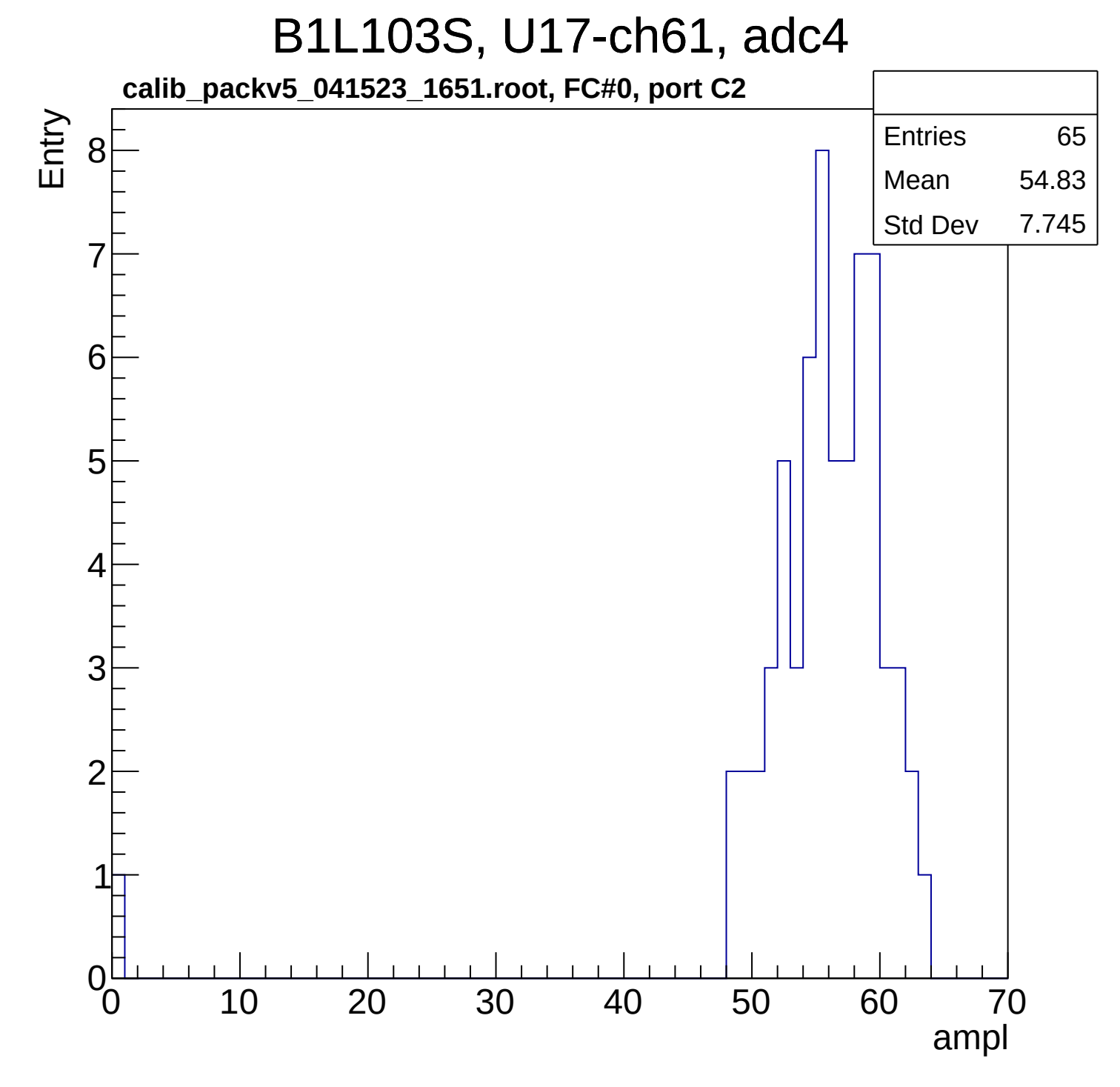
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U17-ch61, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 54.83
Std Dev 7.745
Entry
ampl
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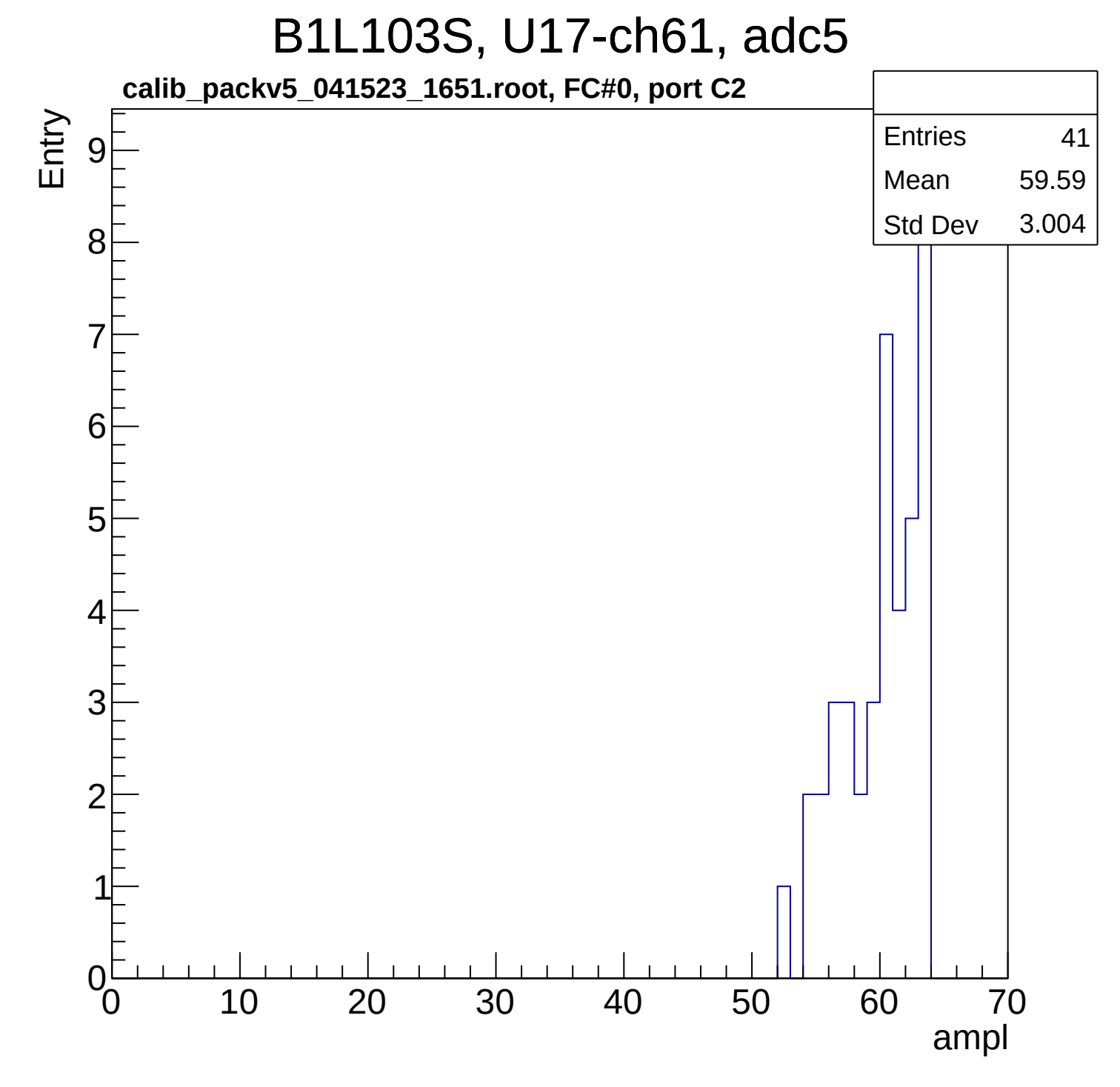
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U17-ch61, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 41
Mean 59.59
Std Dev 3.004
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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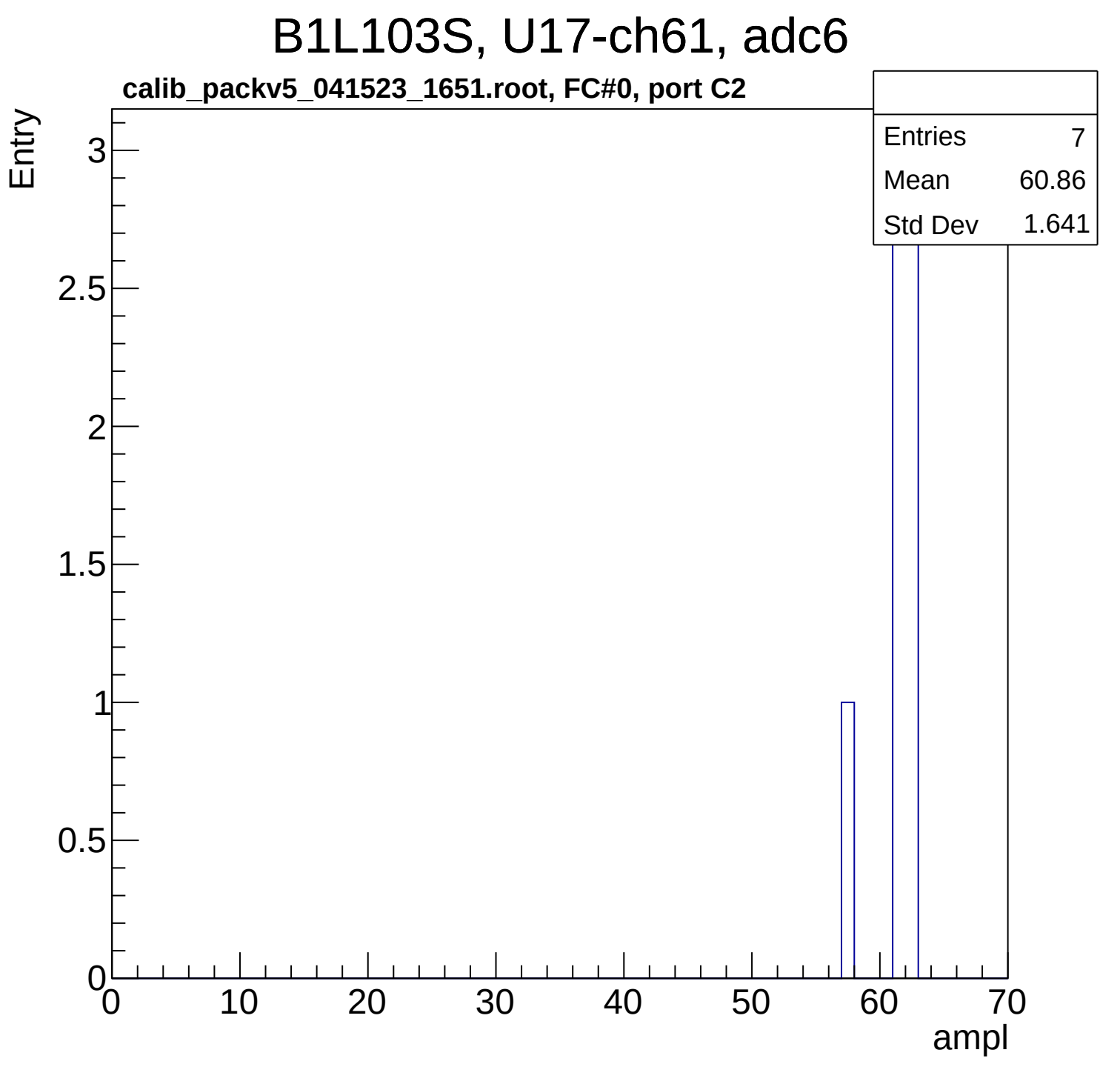
40
50
60
70


B1L103S, U17-ch61, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 60.86
Std Dev 1.641
Entry
ampl
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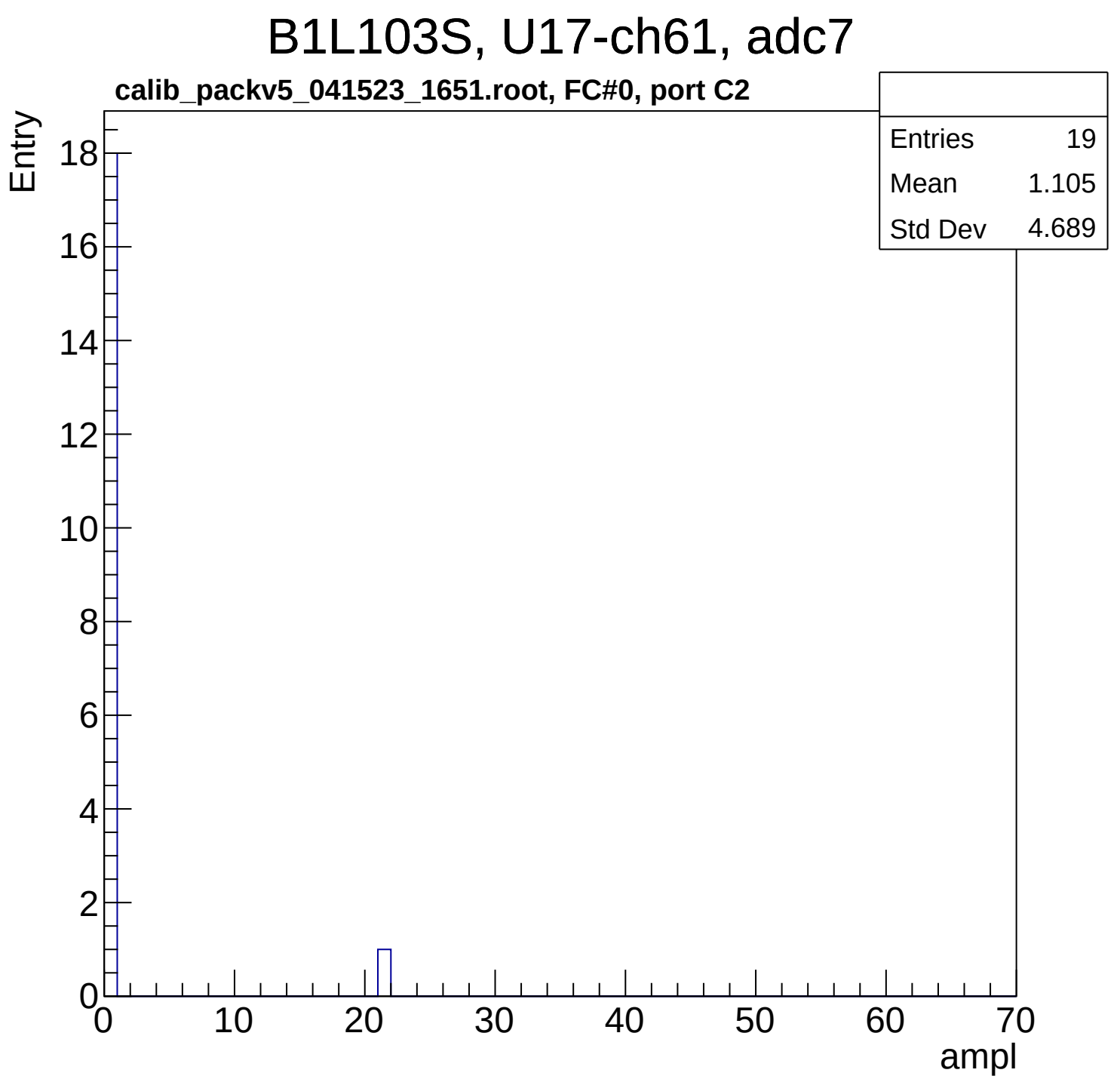
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U17-ch61, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.105
Std Dev 4.689
Entry
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6
8
10
12
14
16
18
0
10
20
30
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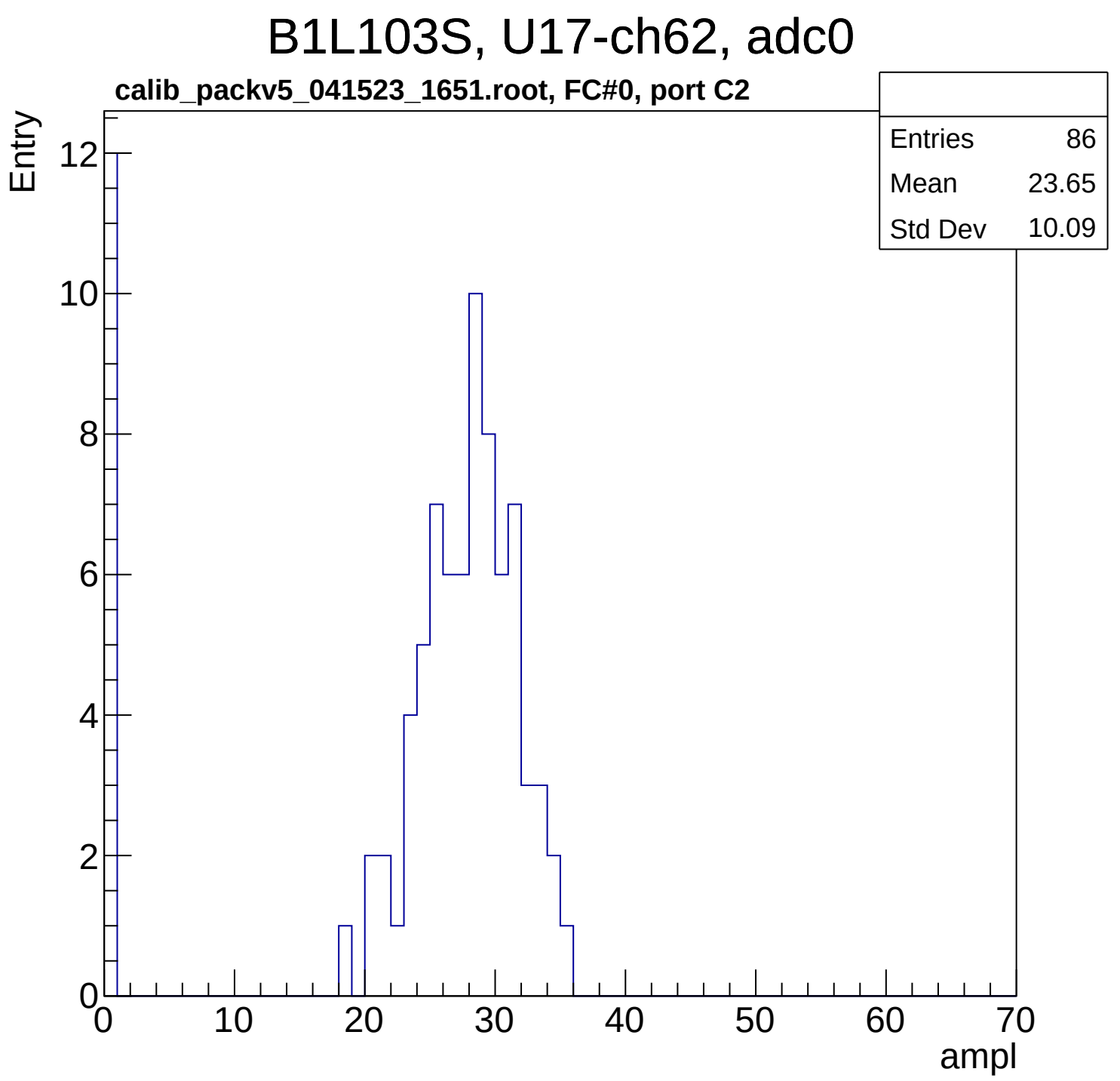
50
60
70
ampl


B1L103S, U17-ch62, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 23.65
Std Dev 10.09
Entry
0
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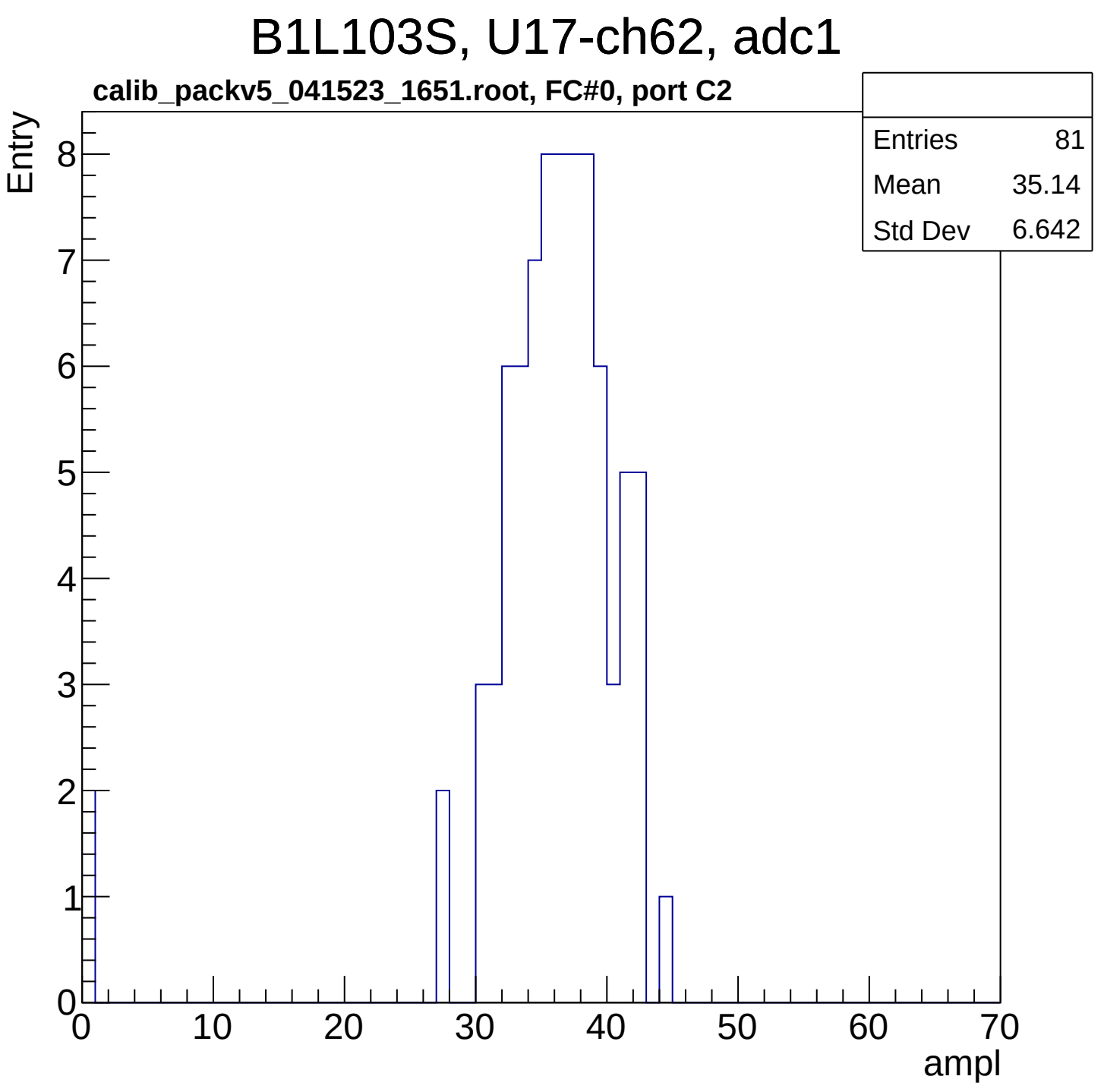
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch62, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 35.14
Std Dev 6.642
Entry
ampl
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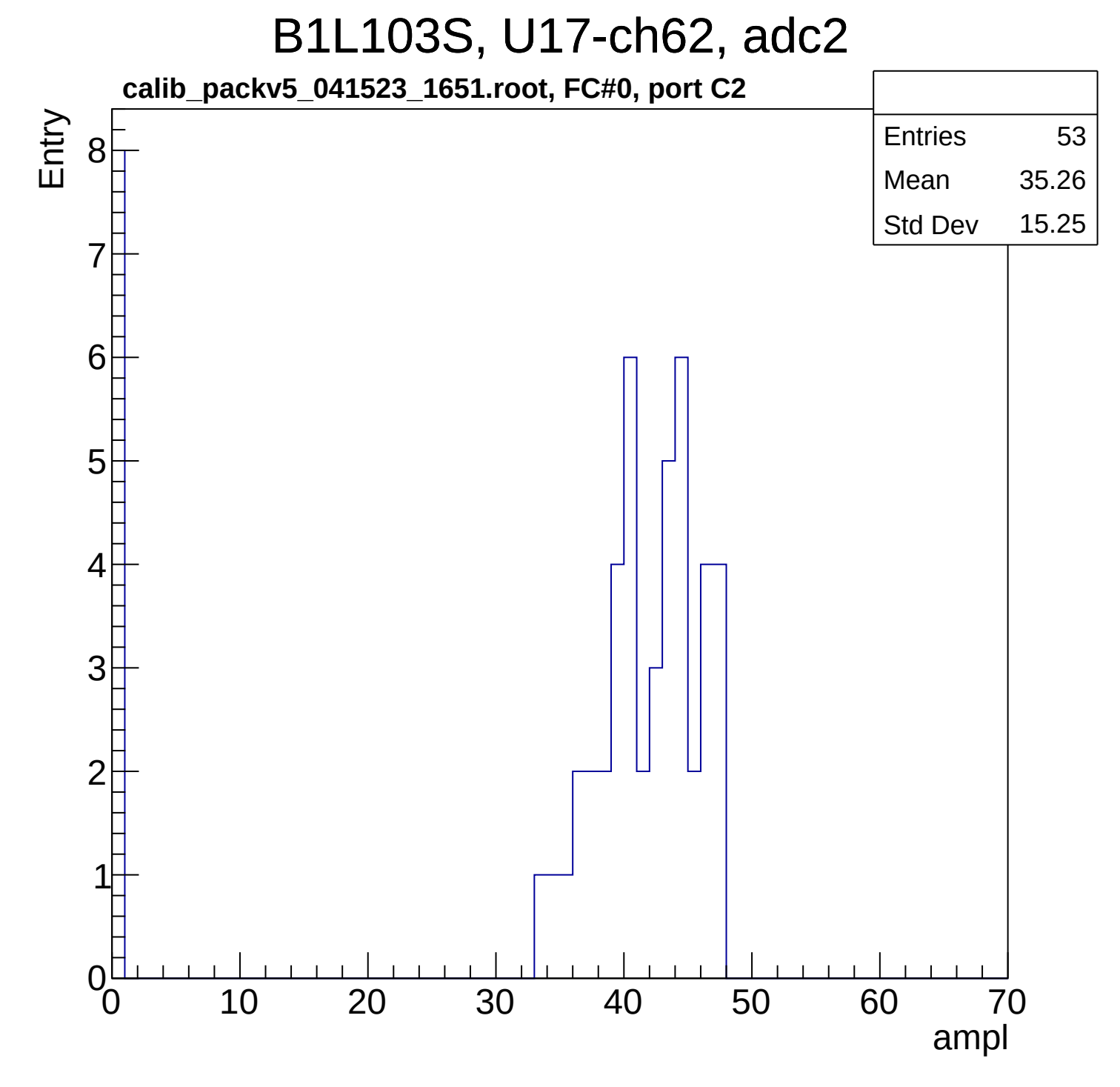
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U17-ch62, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 35.26
Std Dev 15.25
Entry
ampl
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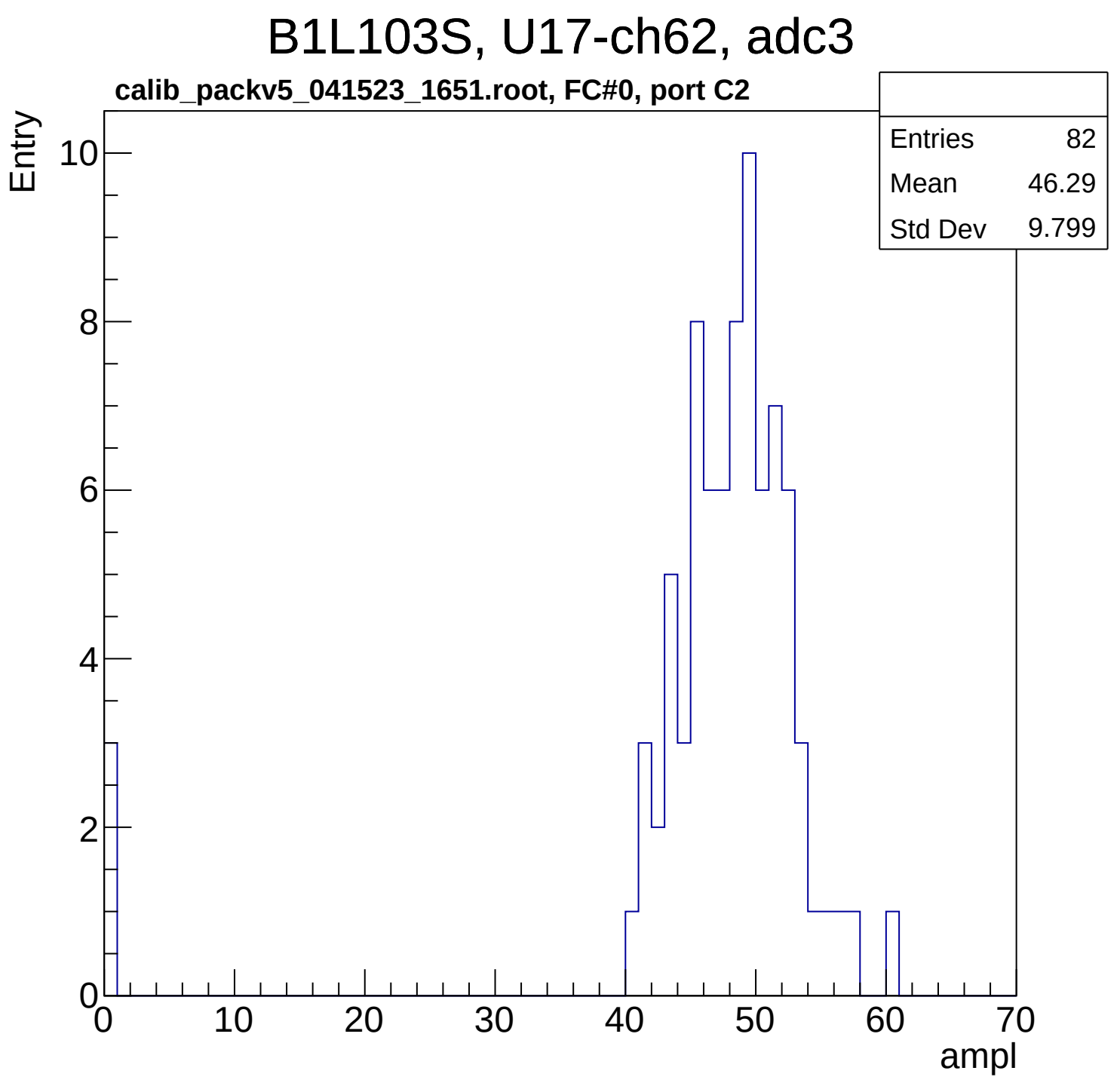
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U17-ch62, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 46.29
Std Dev 9.799
Entry
ampl
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4
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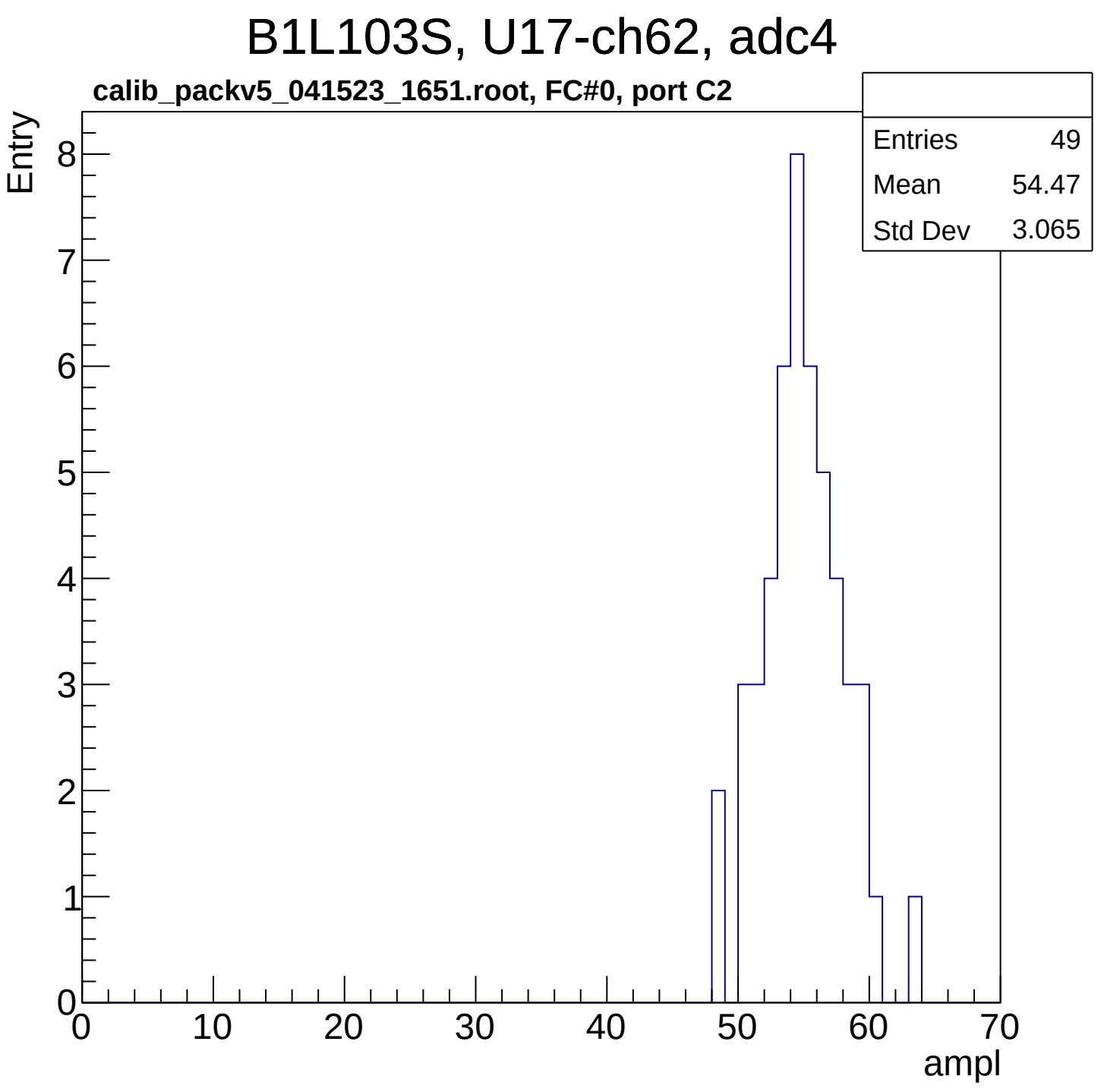
8
10
0
10
20
30
40
50
60
70


B1L103S, U17-ch62, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 54.47
Std Dev 3.065
Entry
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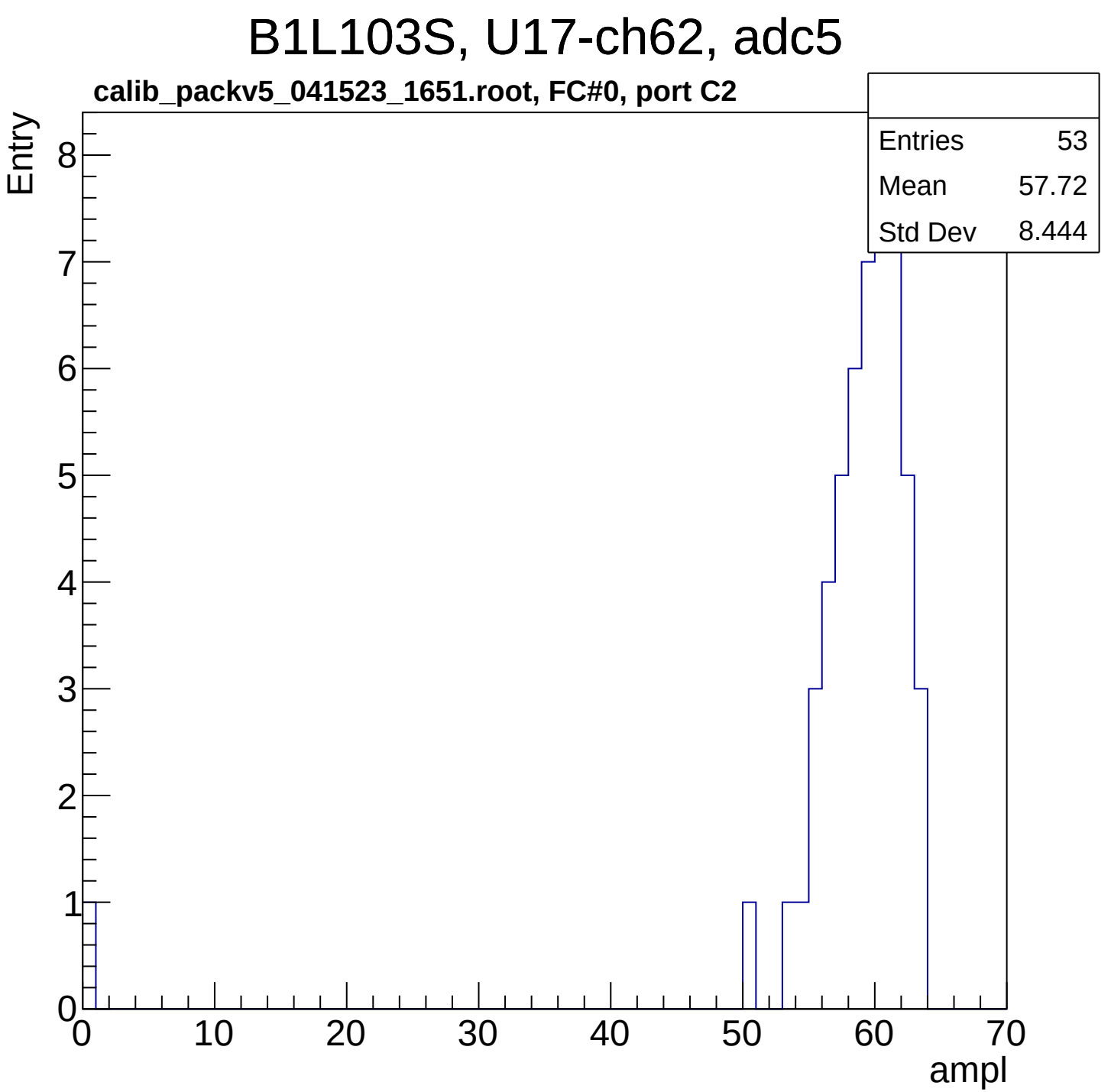
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch62, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 57.72
Std Dev 8.444
Entry
ampl
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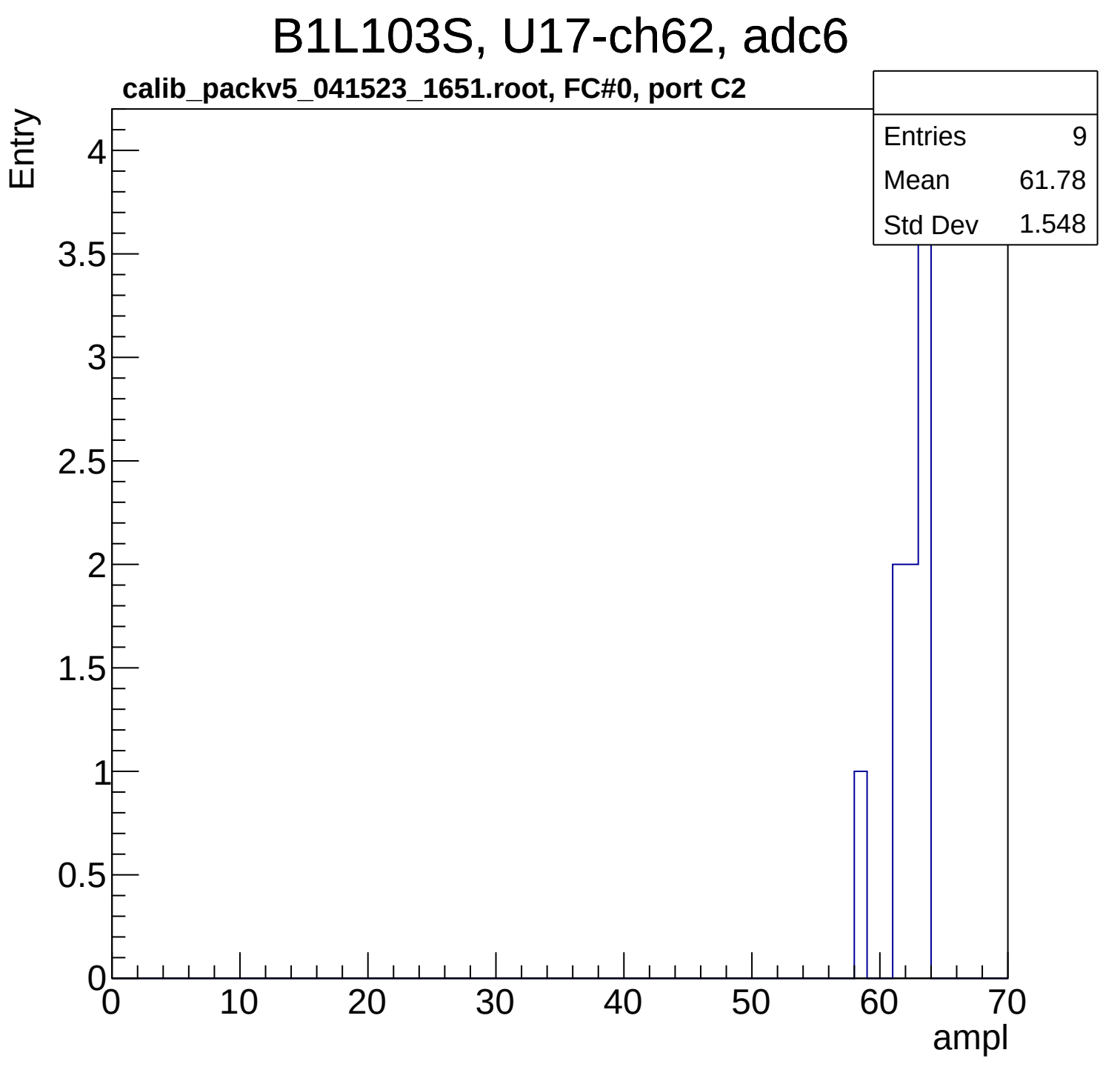
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U17-ch62, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 9
Mean 61.78
Std Dev 1.548
Entry
ampl
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1.5
2
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3.5
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0
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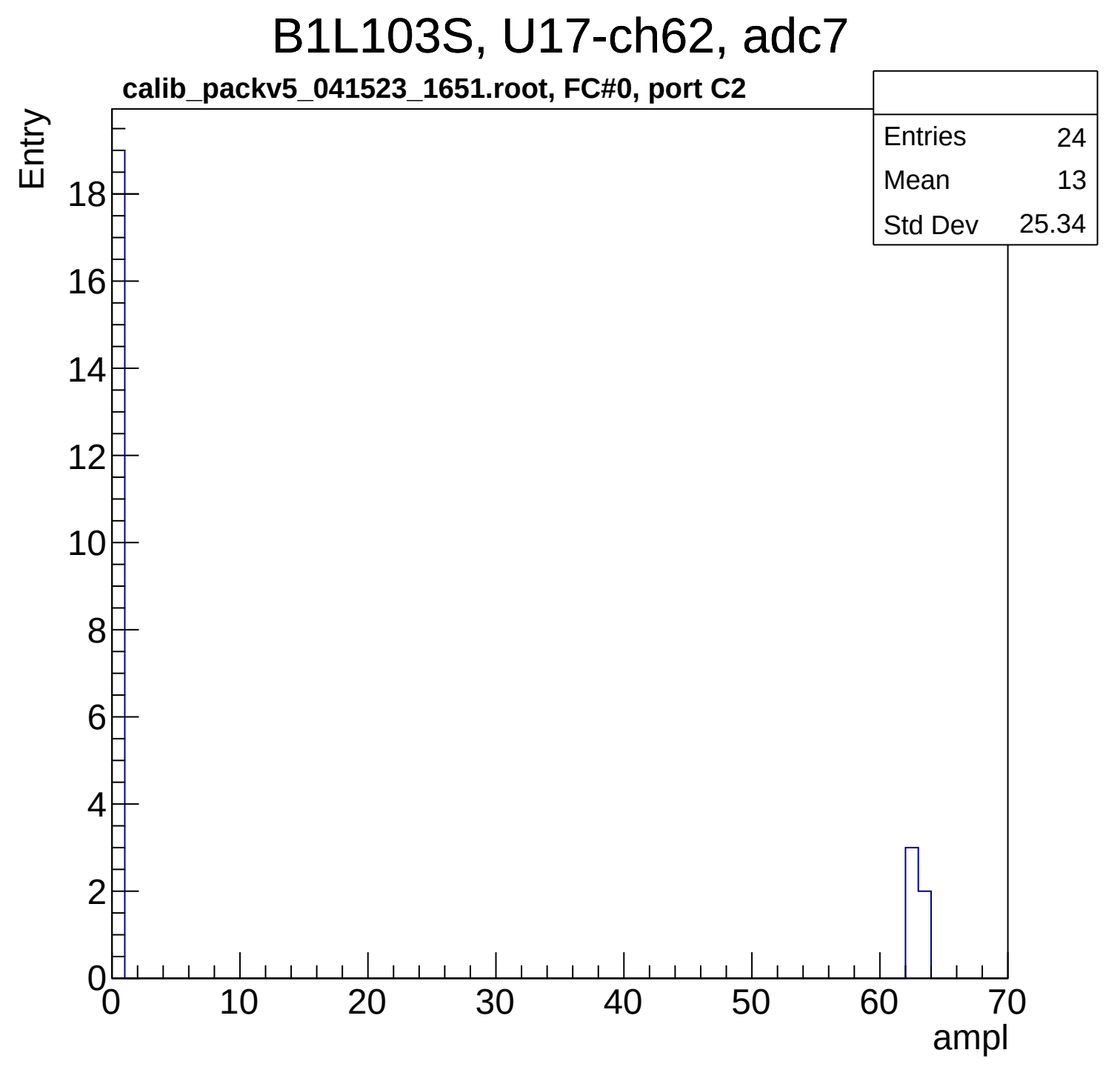
50
60
70


B1L103S, U17-ch62, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 24
Mean 13
Std Dev 25.34
Entry
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6
8
10
12
14
16
18
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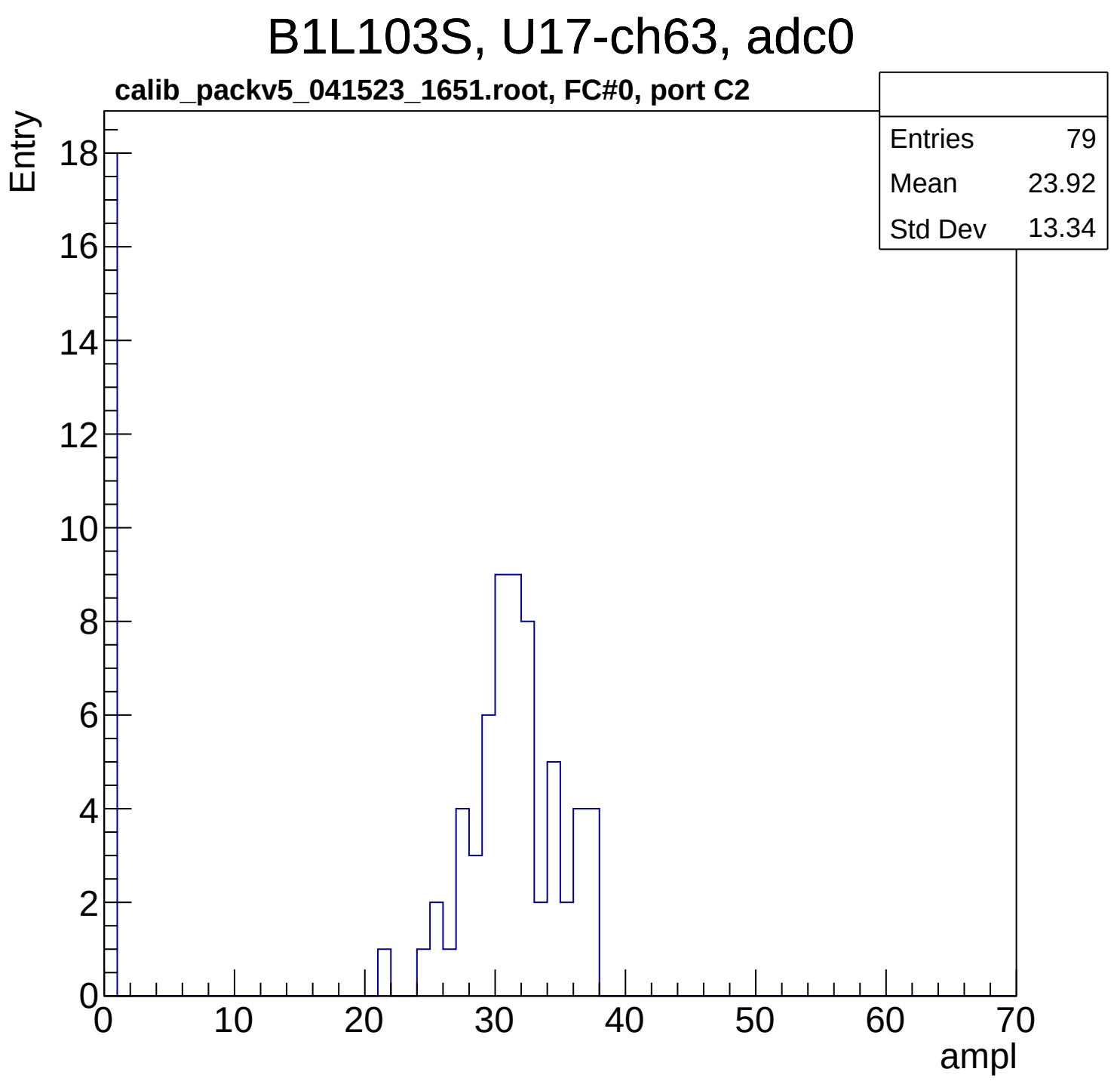
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch63, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 23.92
Std Dev 13.34
Entry
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12
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10
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50
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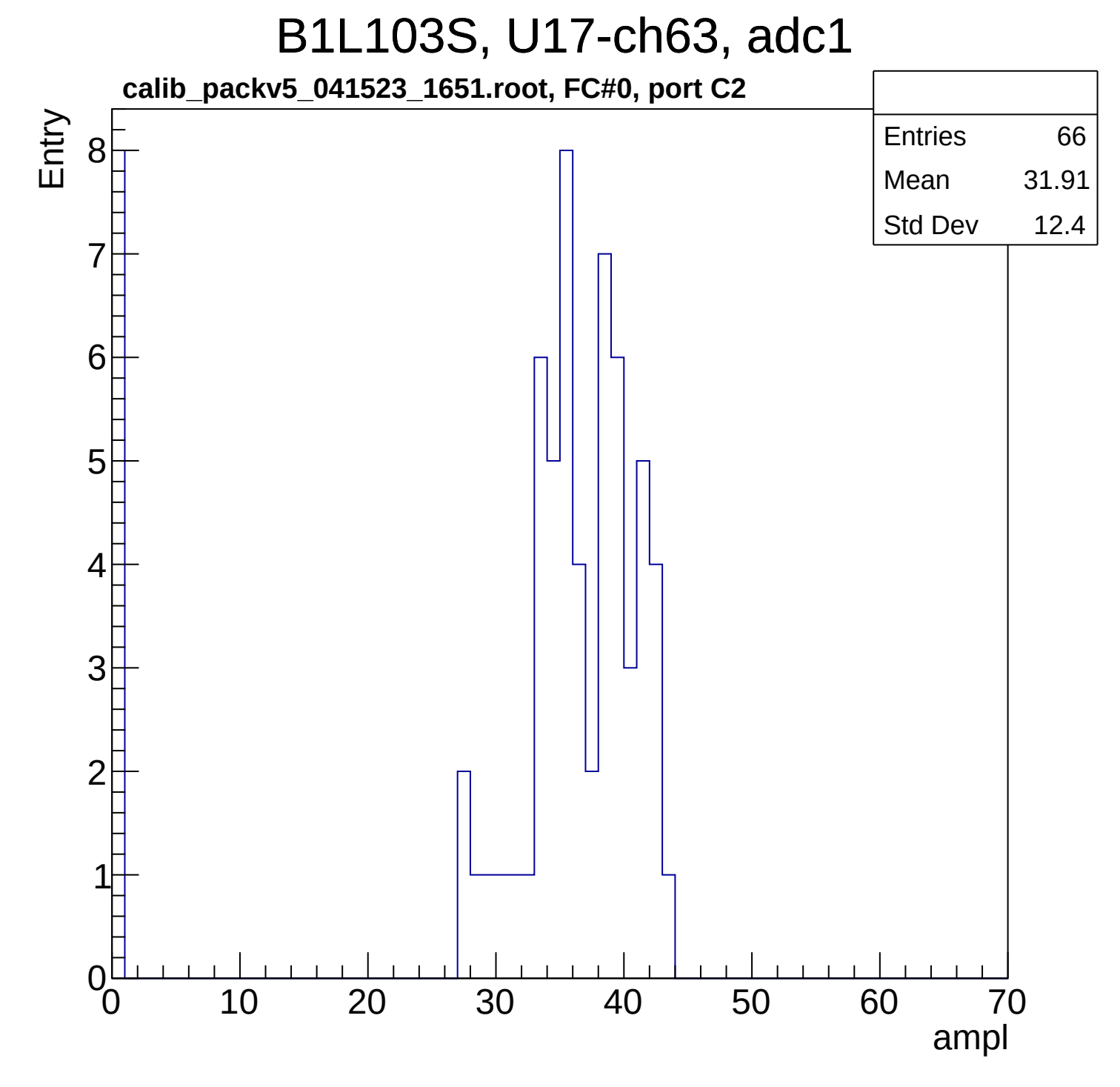
70
ampl


B1L103S, U17-ch63, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 31.91
Std Dev 12.4
Entry
ampl
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1
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3
4
5
6
7
8
0
10
20
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40
50
60
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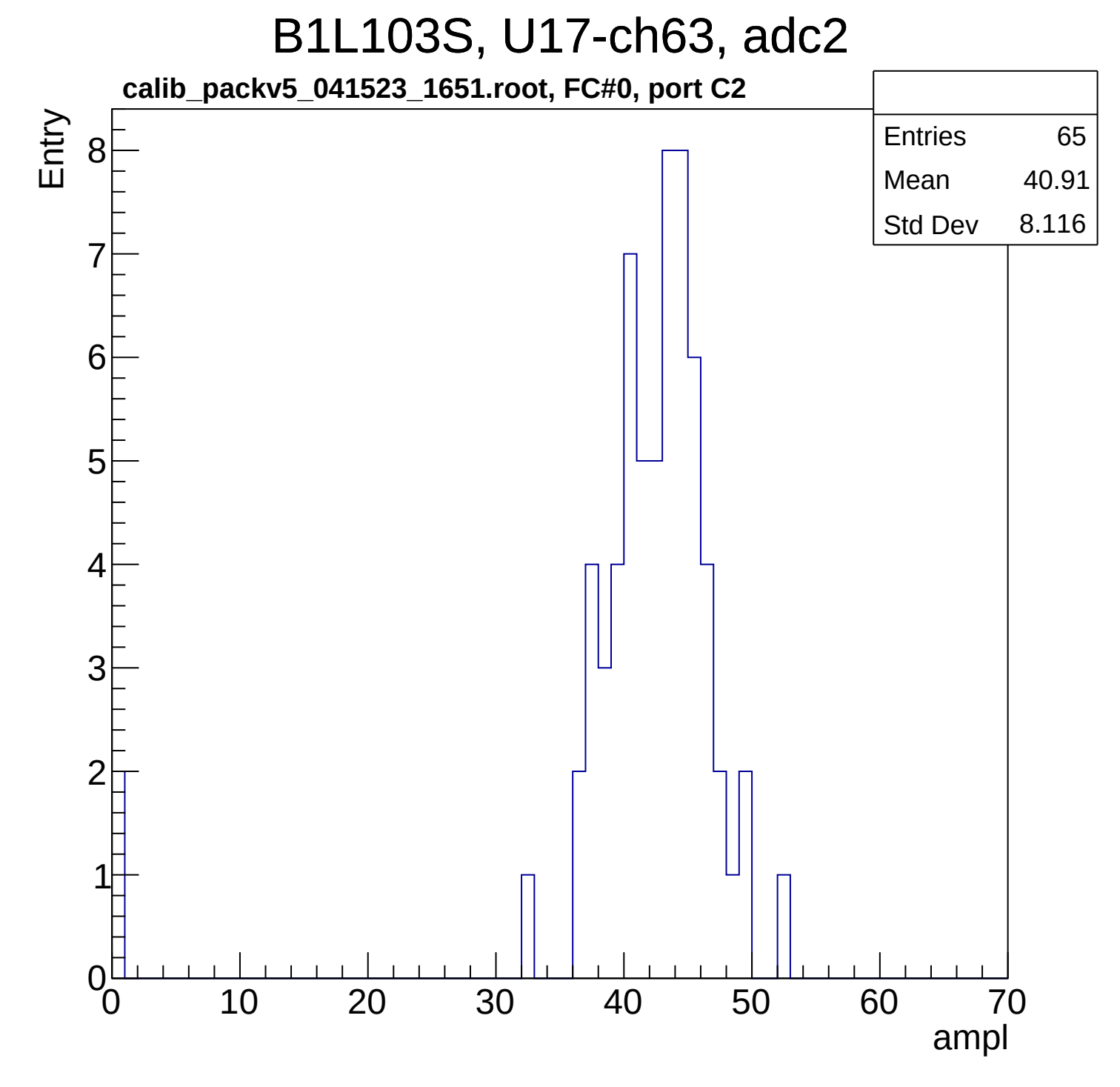
B1L103S, U17-ch63, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 40.91
Std Dev 8.116
Entry
ampl
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2
3
4
5
6
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0
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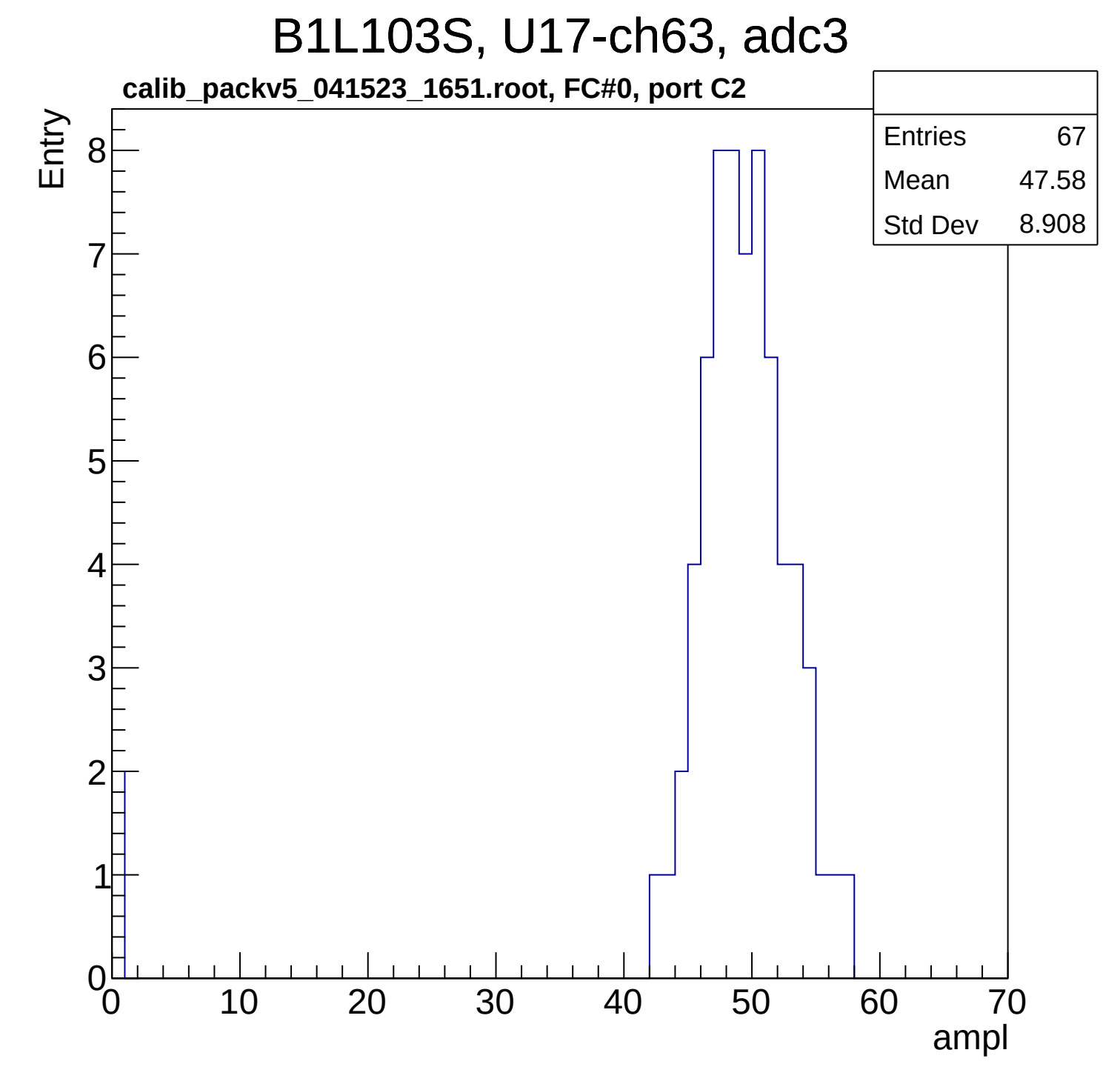
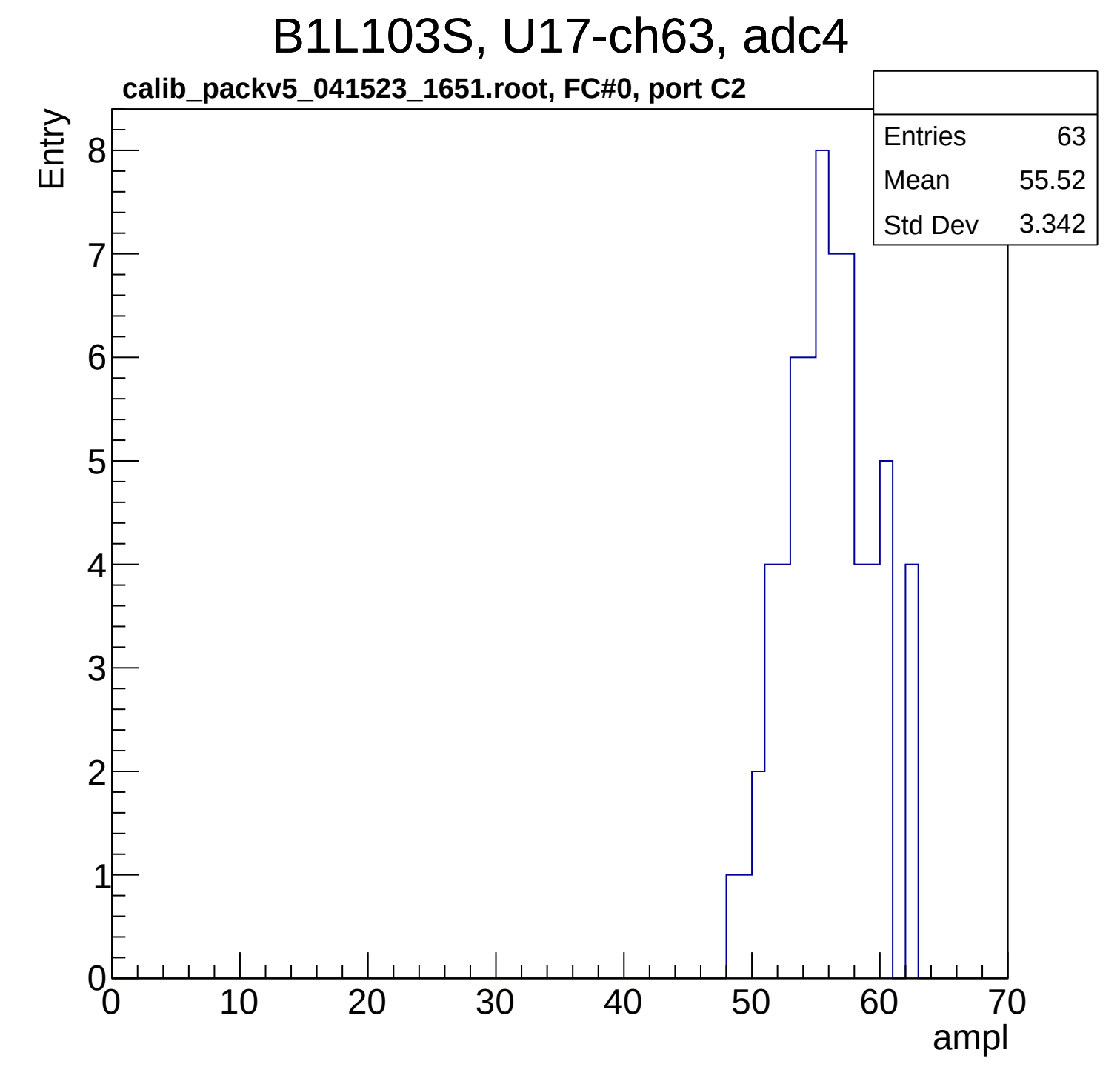
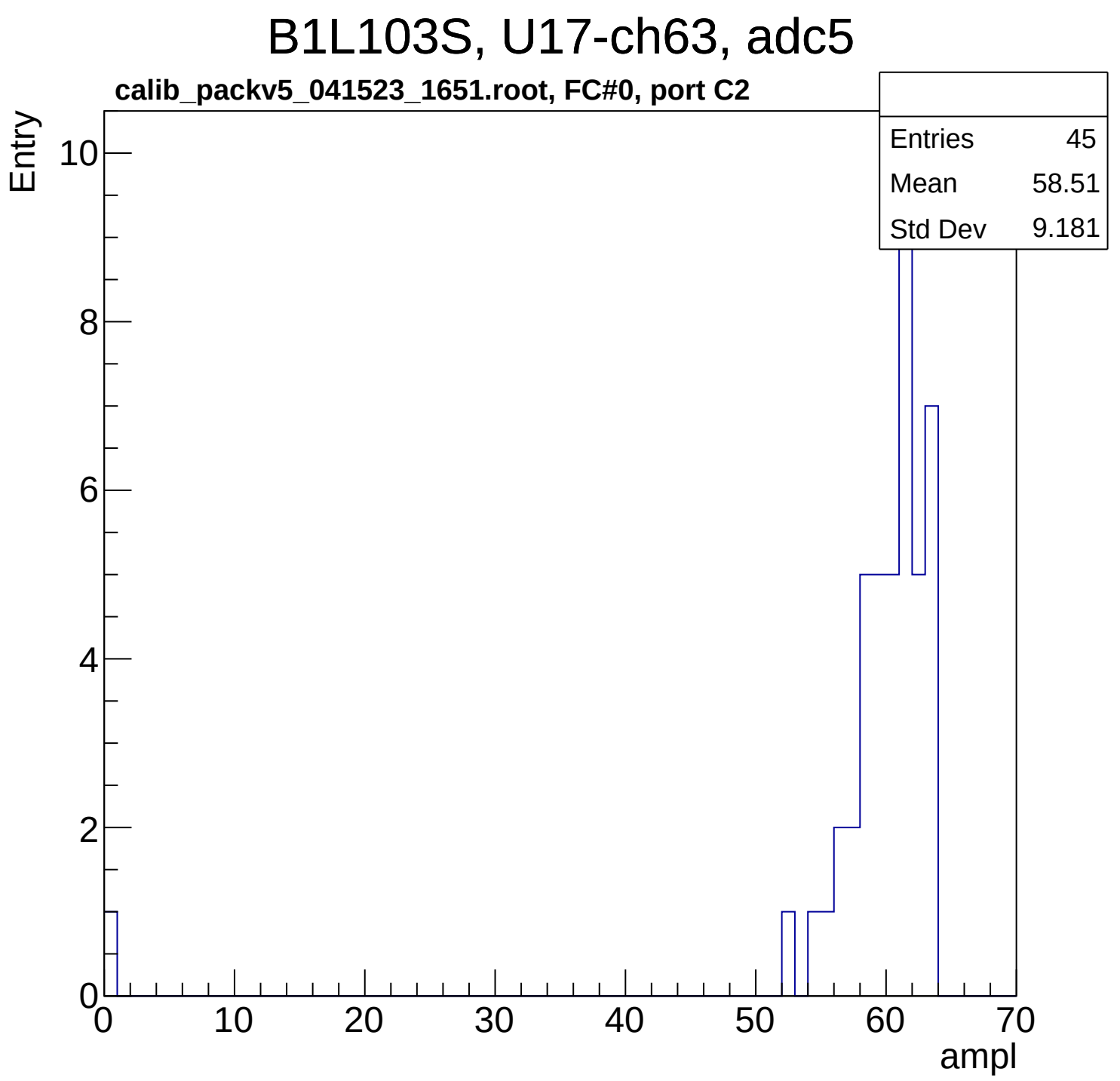
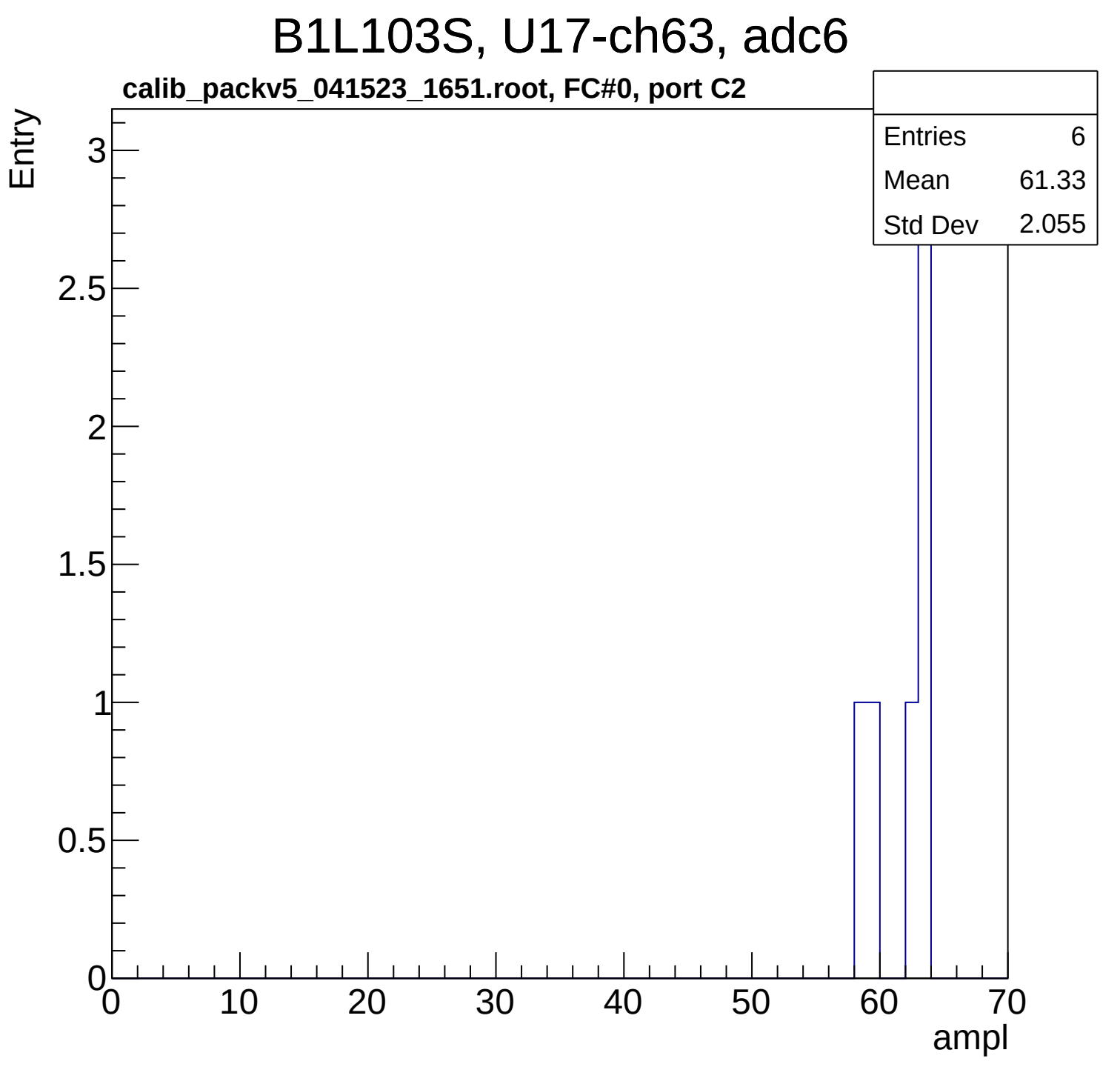
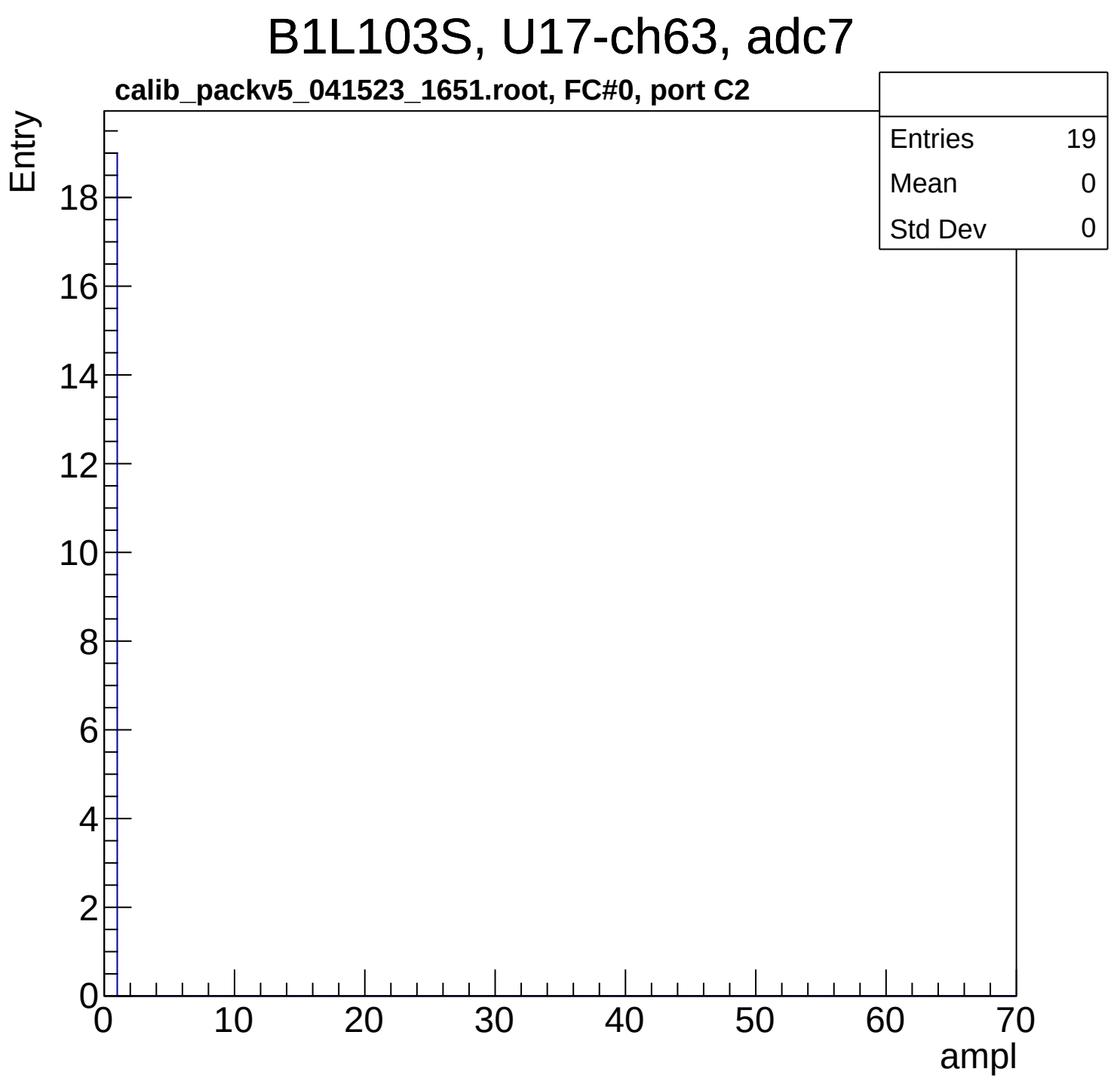
50
60
70

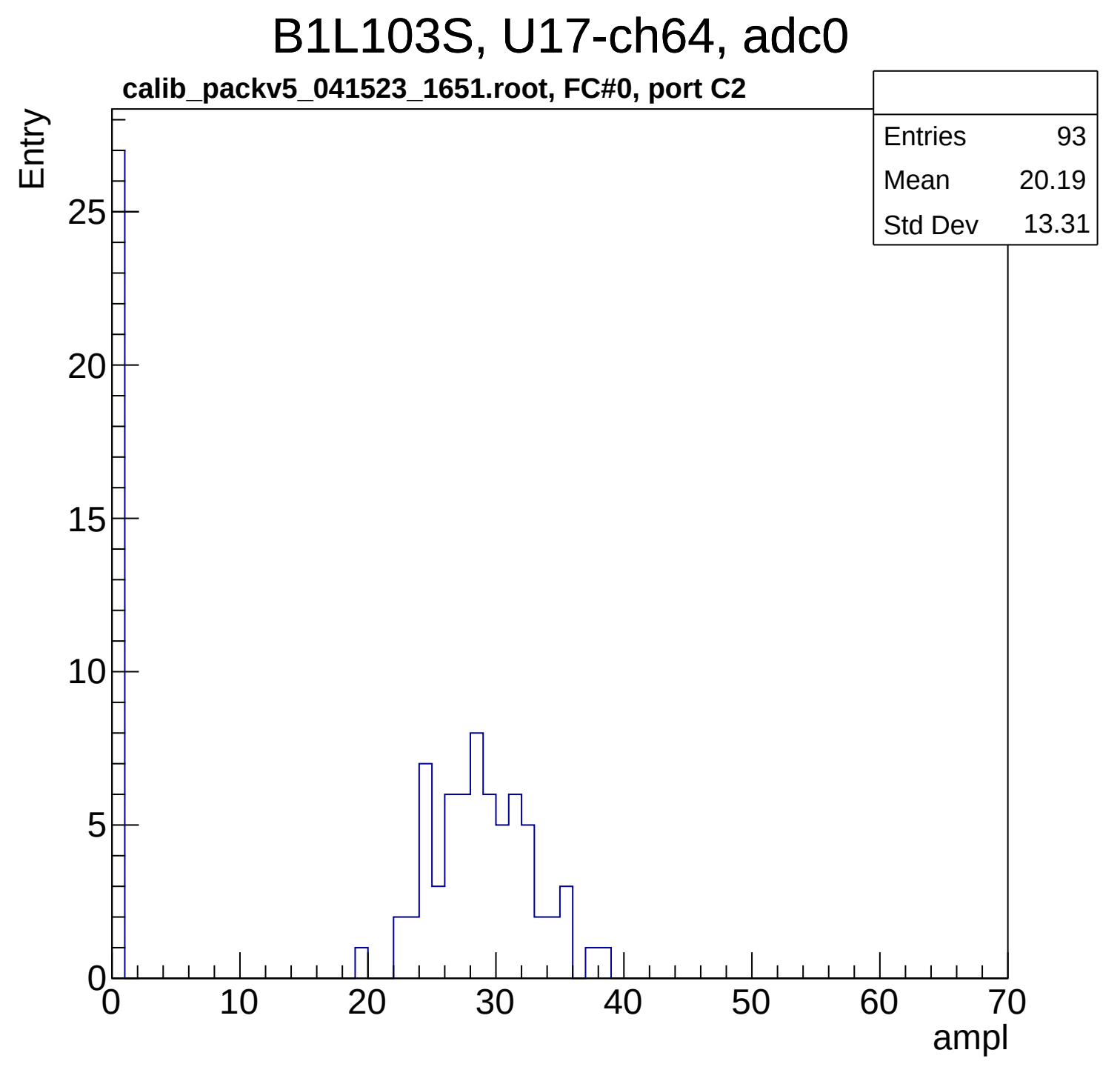

B1L103S, U17-ch63, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 47.58
Std Dev 8.908
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

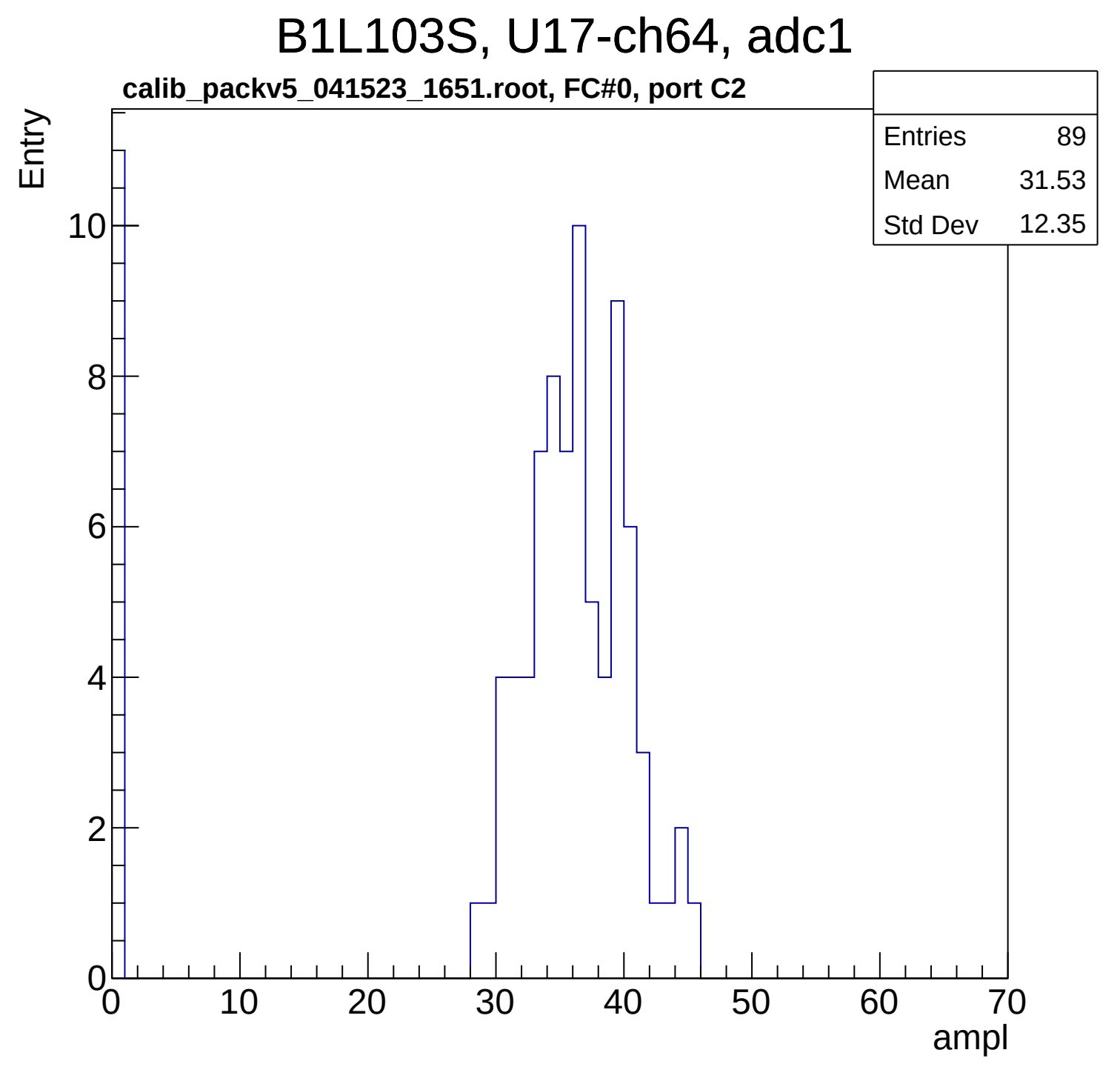

B1L103S, U17-ch63, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 55.52
Std Dev 3.342
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

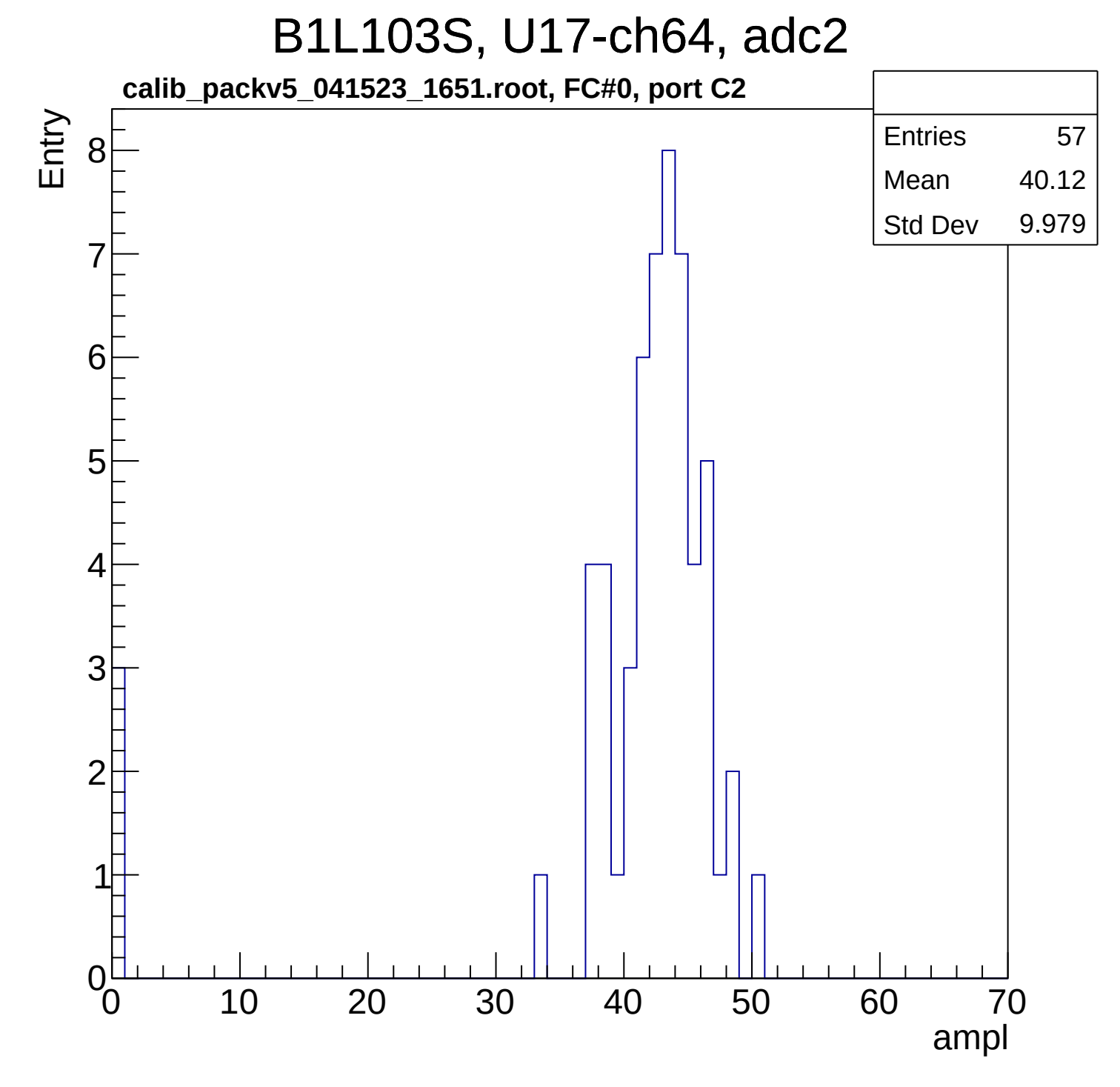

B1L103S, U17-ch63, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 58.51
Std Dev 9.181
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

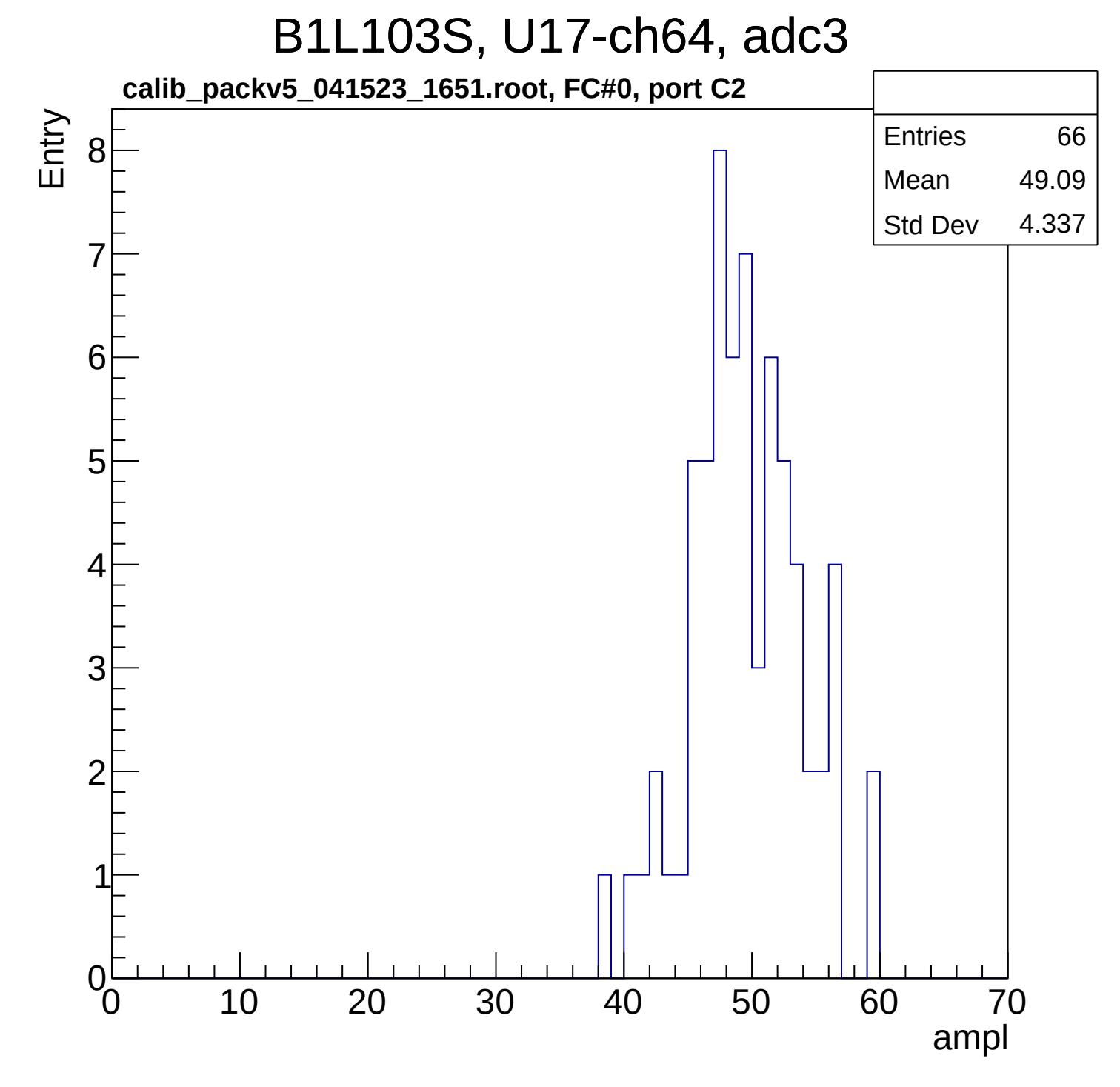

B1L103S, U17-ch63, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 61.33
Std Dev 2.055
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

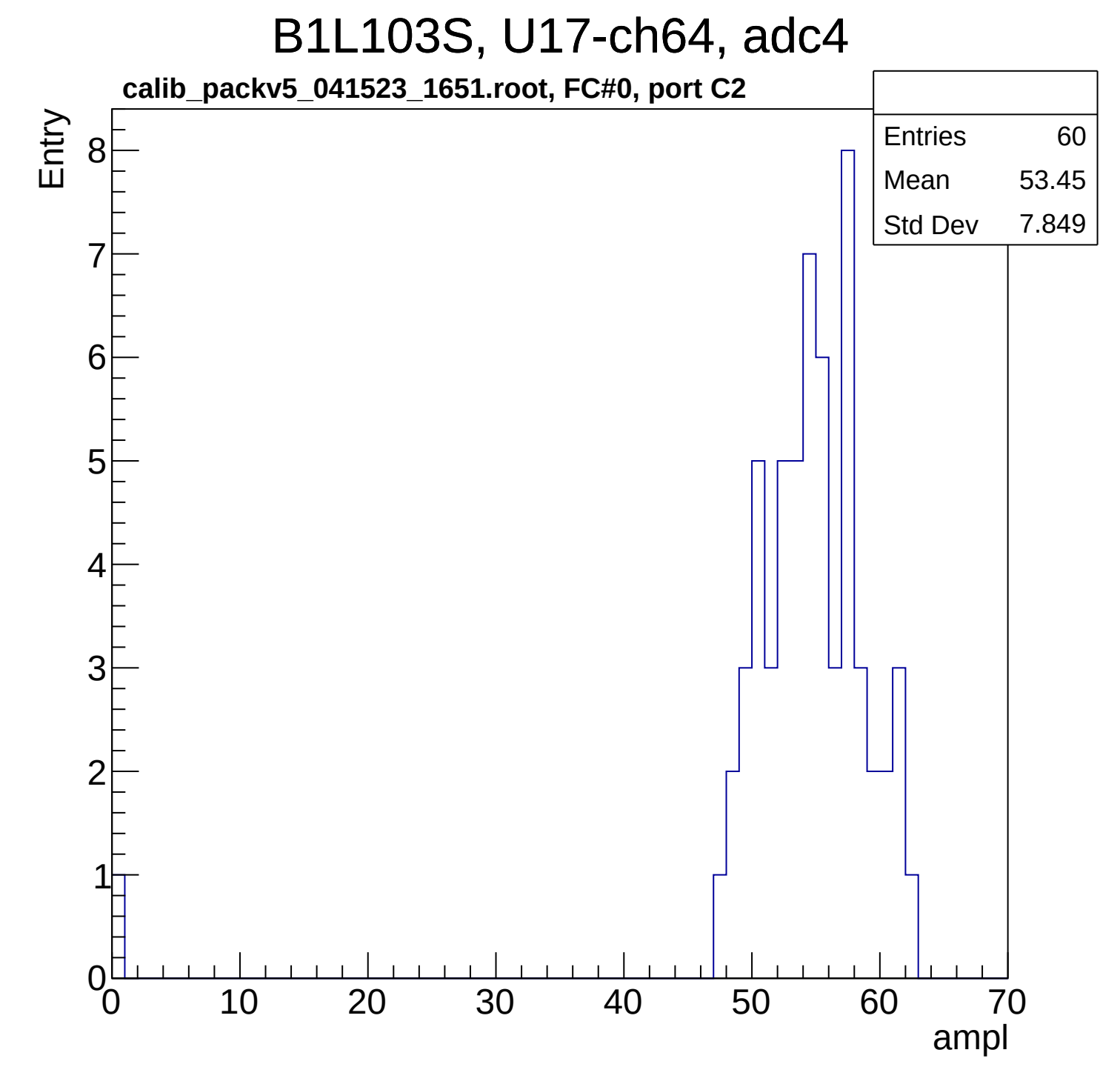

B1L103S, U17-ch63, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

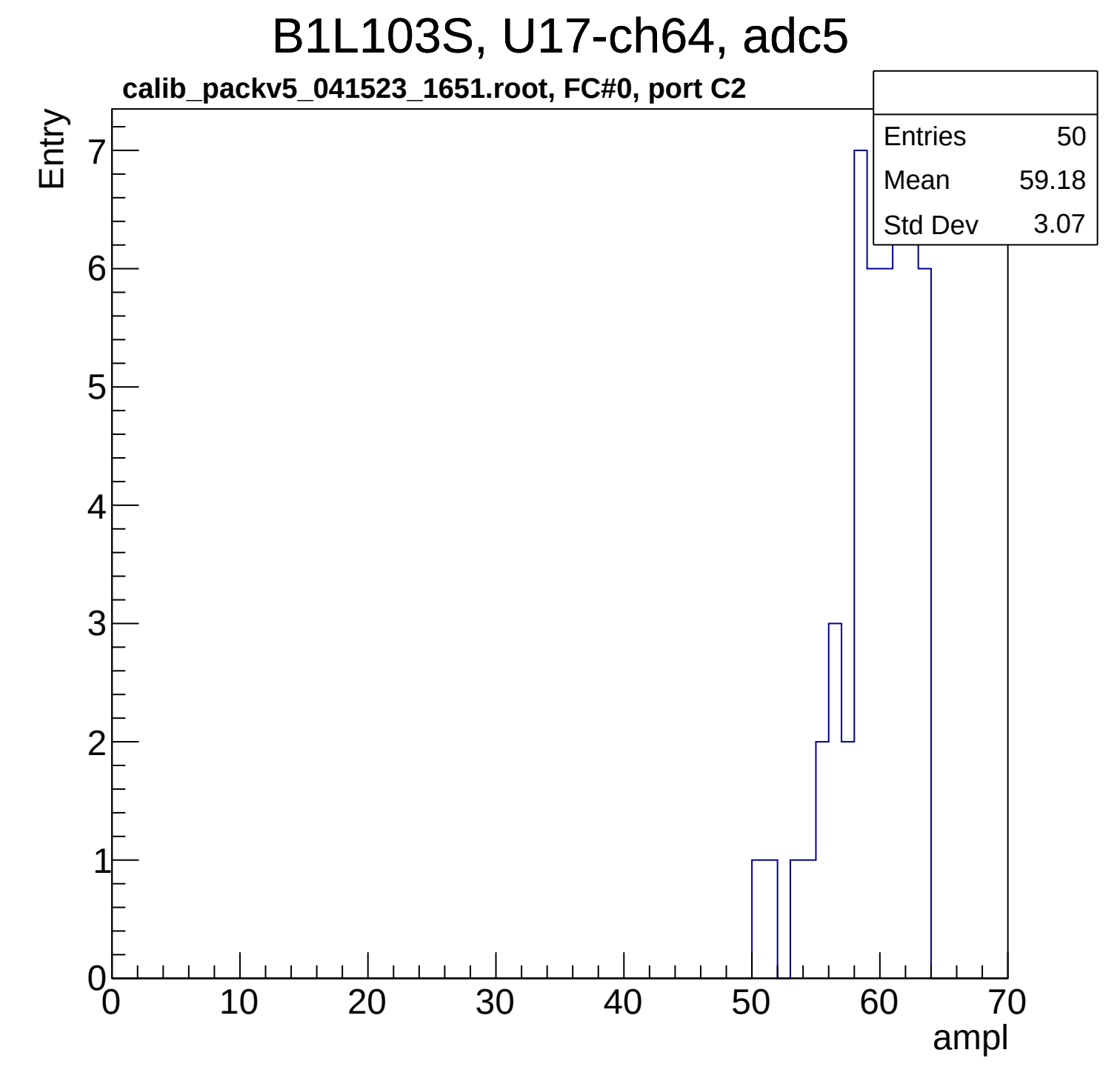

B1L103S, U17-ch64, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 93
Mean 20.19
Std Dev 13.31
Entry
0
5
10
15
20
25
0
10
20
30
40
50
60
70
ampl

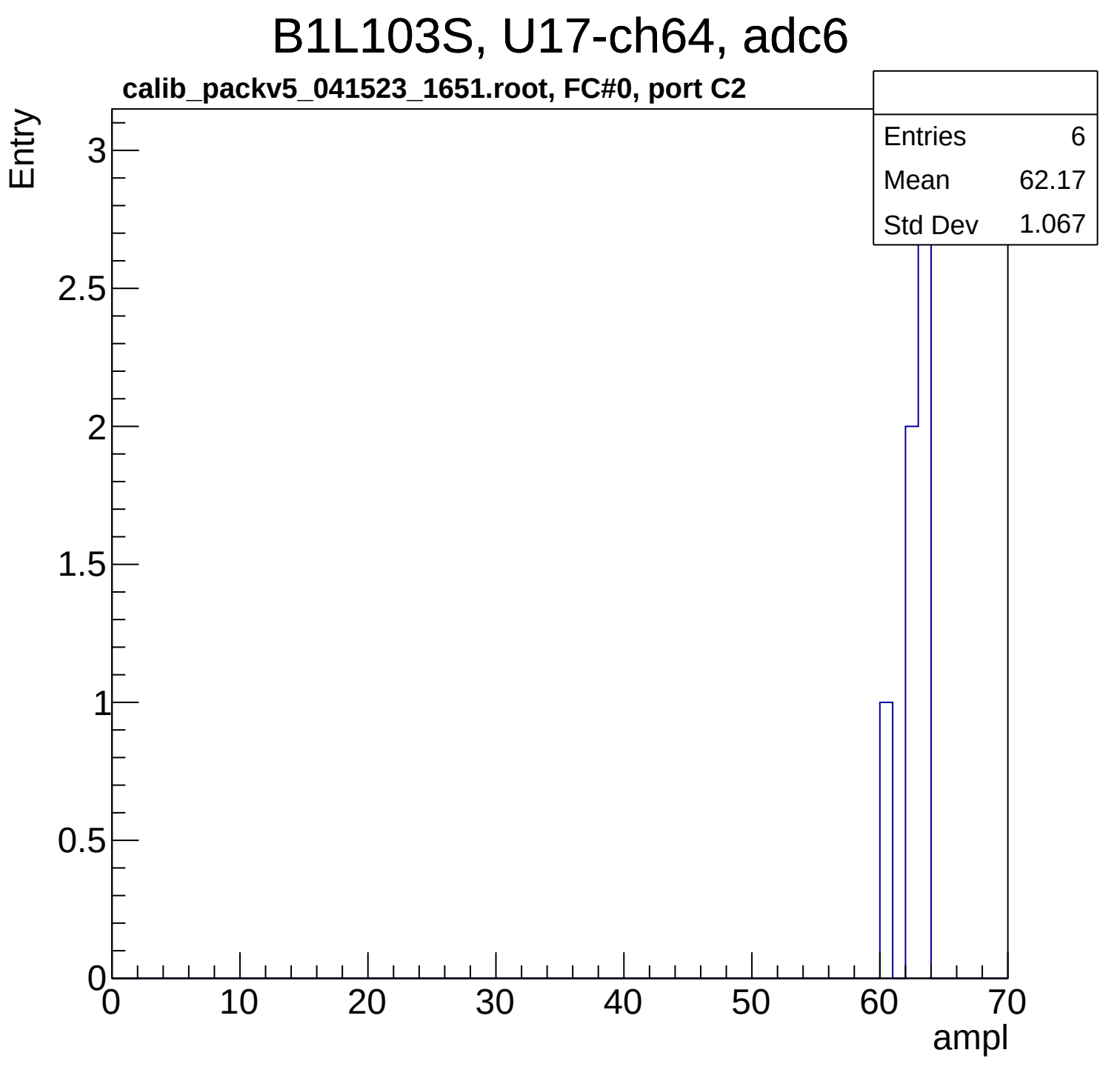

B1L103S, U17-ch64, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 89
Mean 31.53
Std Dev 12.35
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

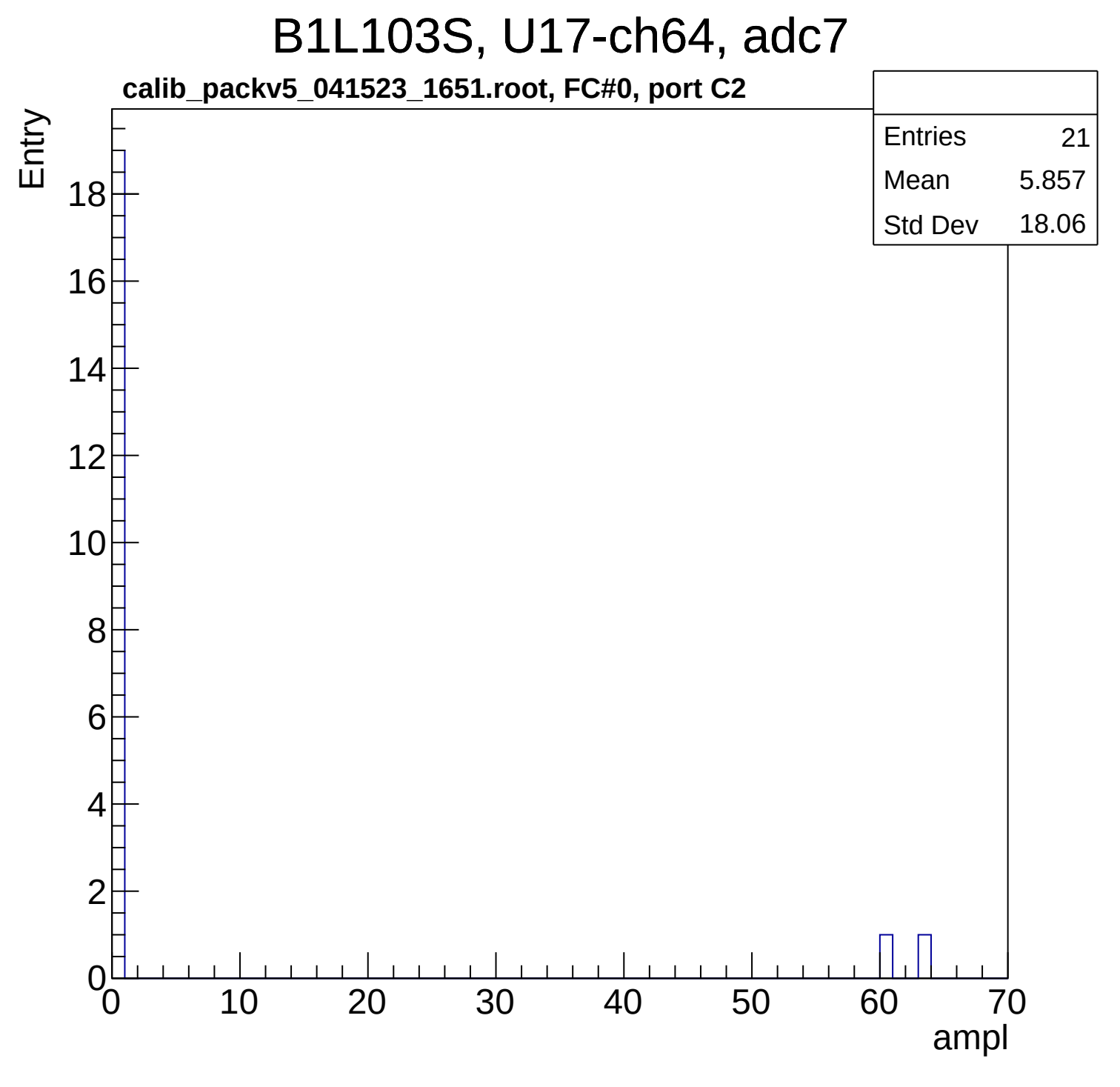

B1L103S, U17-ch64, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 40.12
Std Dev 9.979
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

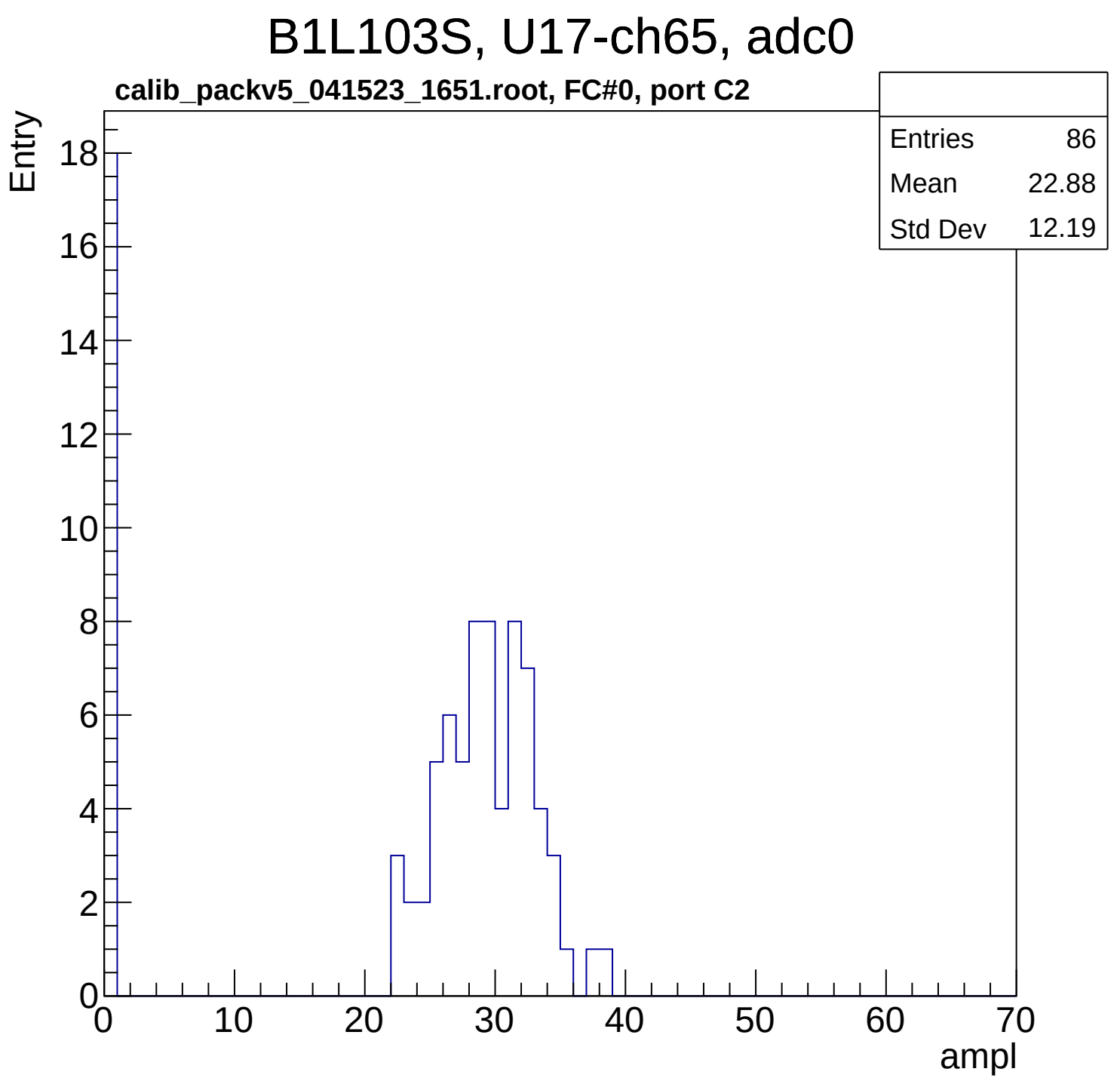

B1L103S, U17-ch64, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 49.09
Std Dev 4.337
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

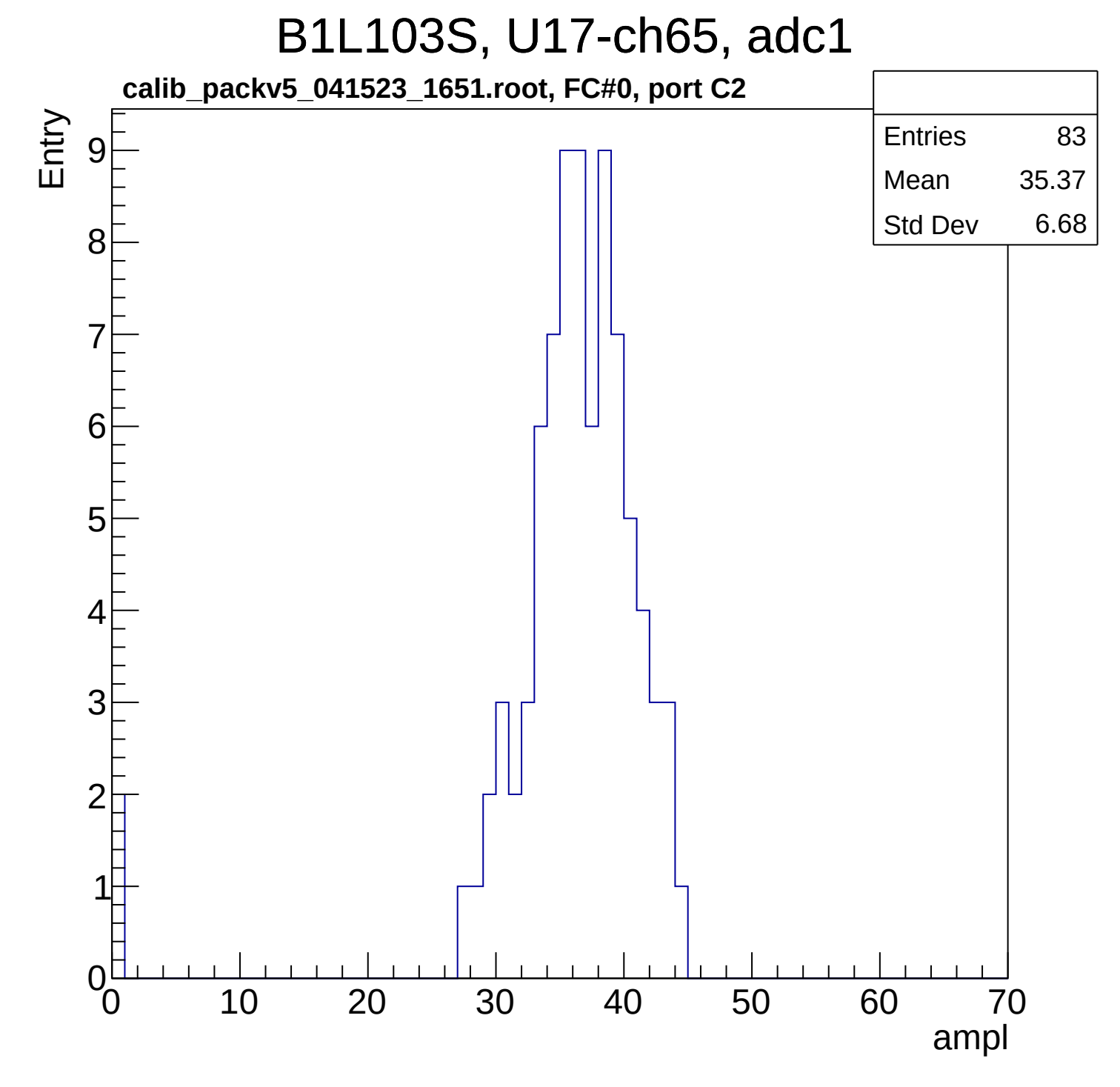

B1L103S, U17-ch64, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 53.45
Std Dev 7.849
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U17-ch64, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 59.18
Std Dev 3.07
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U17-ch64, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 62.17
Std Dev 1.067
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U17-ch64, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 5.857
Std Dev 18.06
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch65, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 22.88
Std Dev 12.19
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch65, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 35.37
Std Dev 6.68
Entry
ampl
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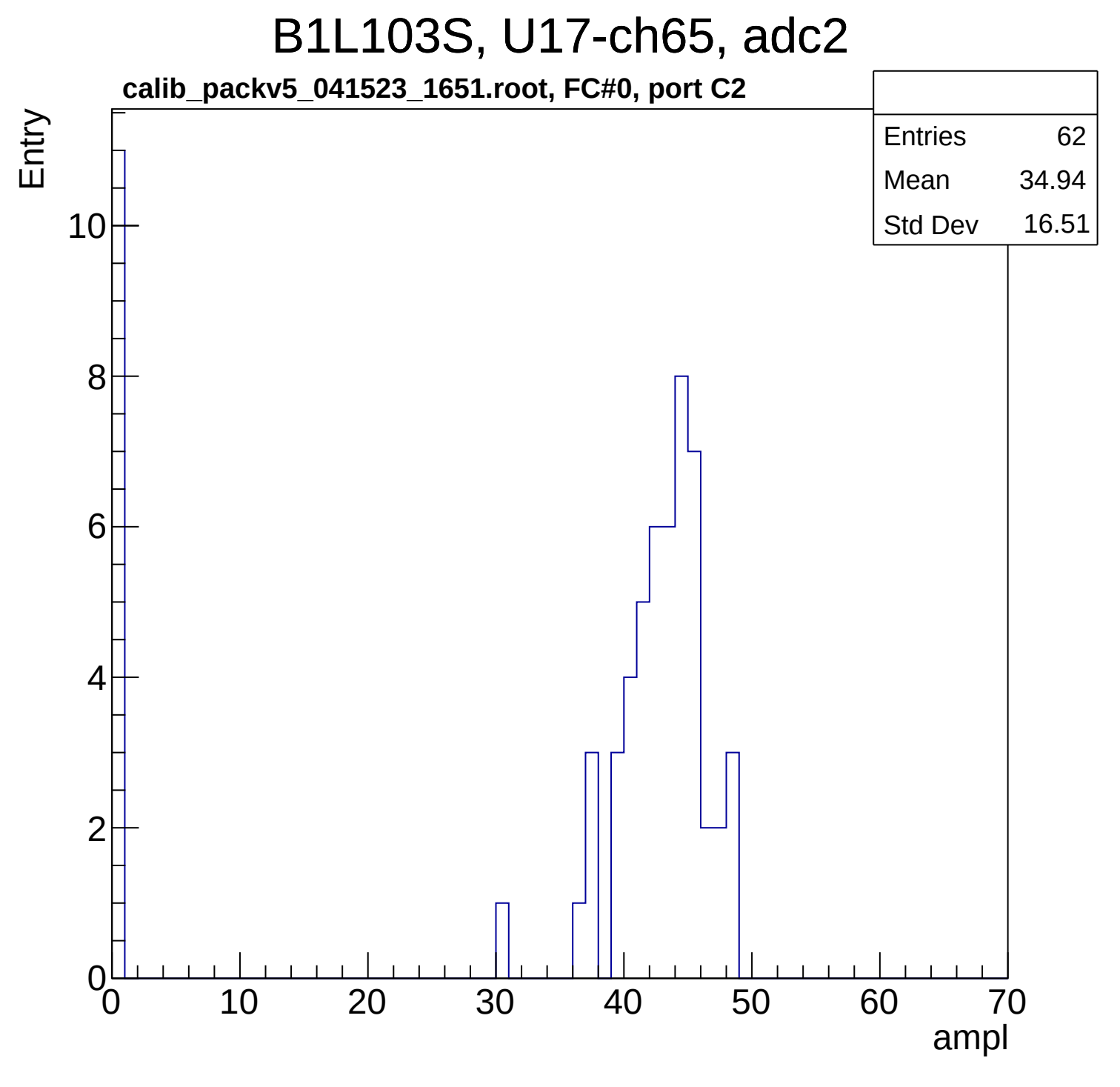
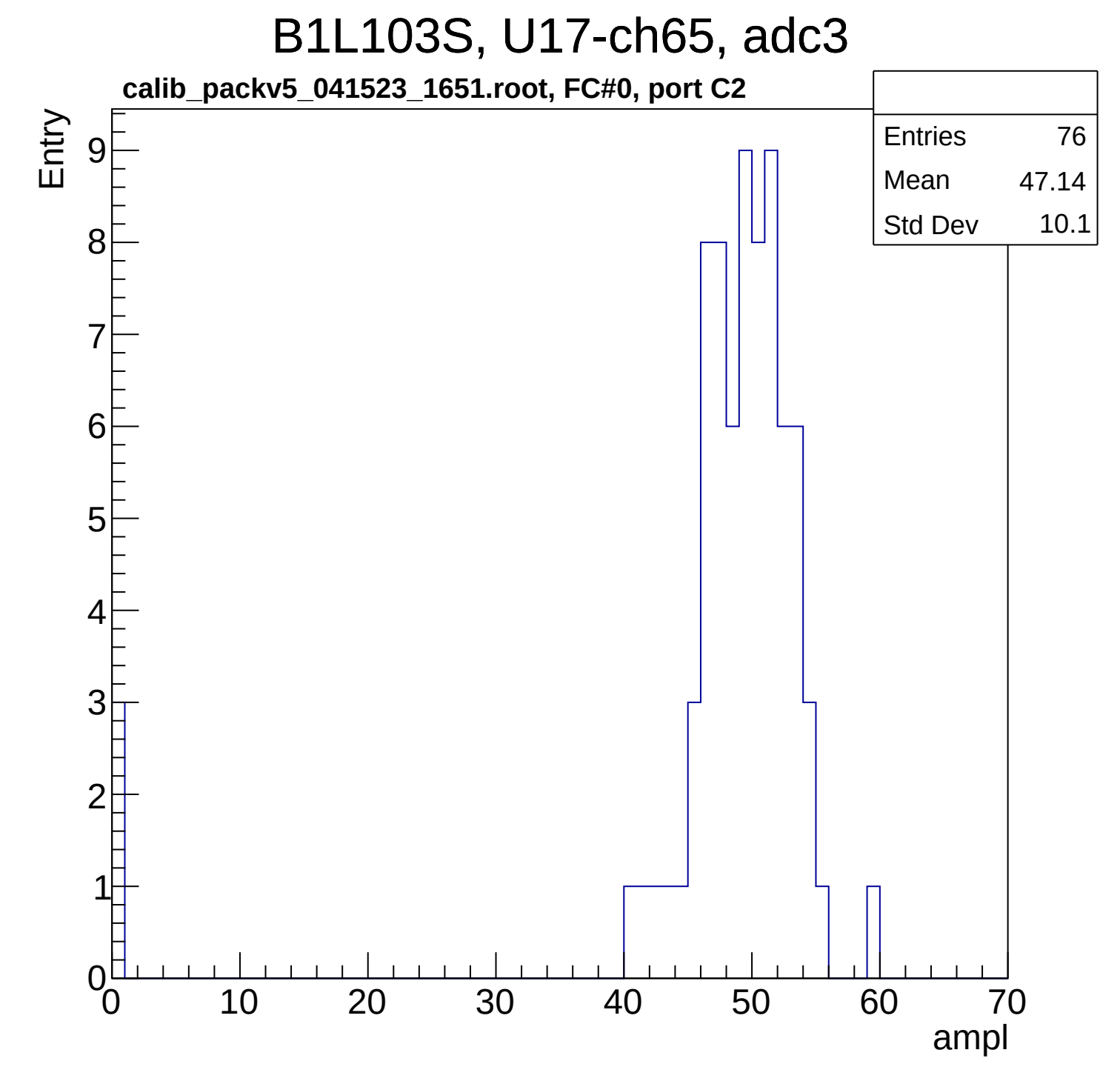
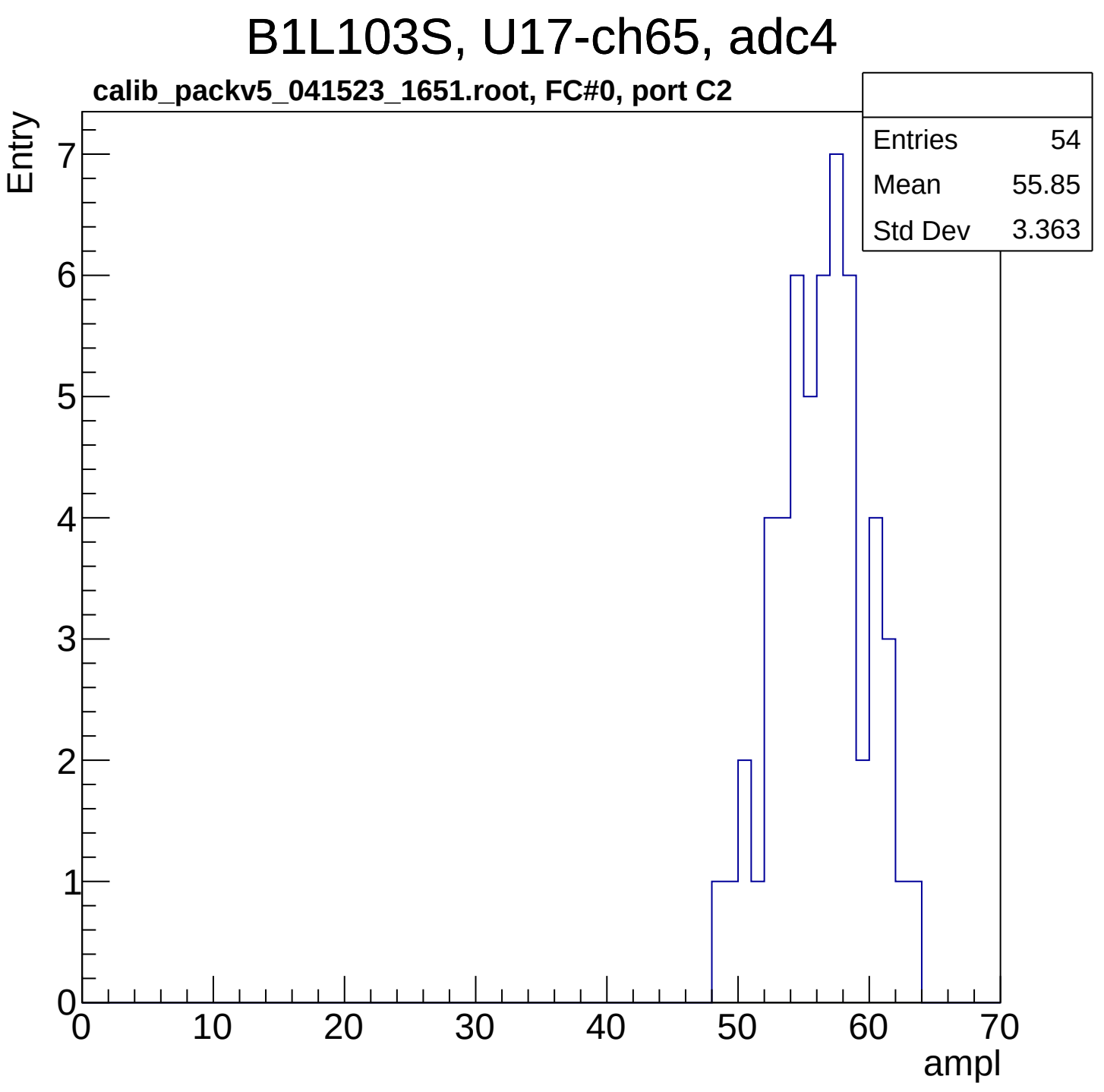
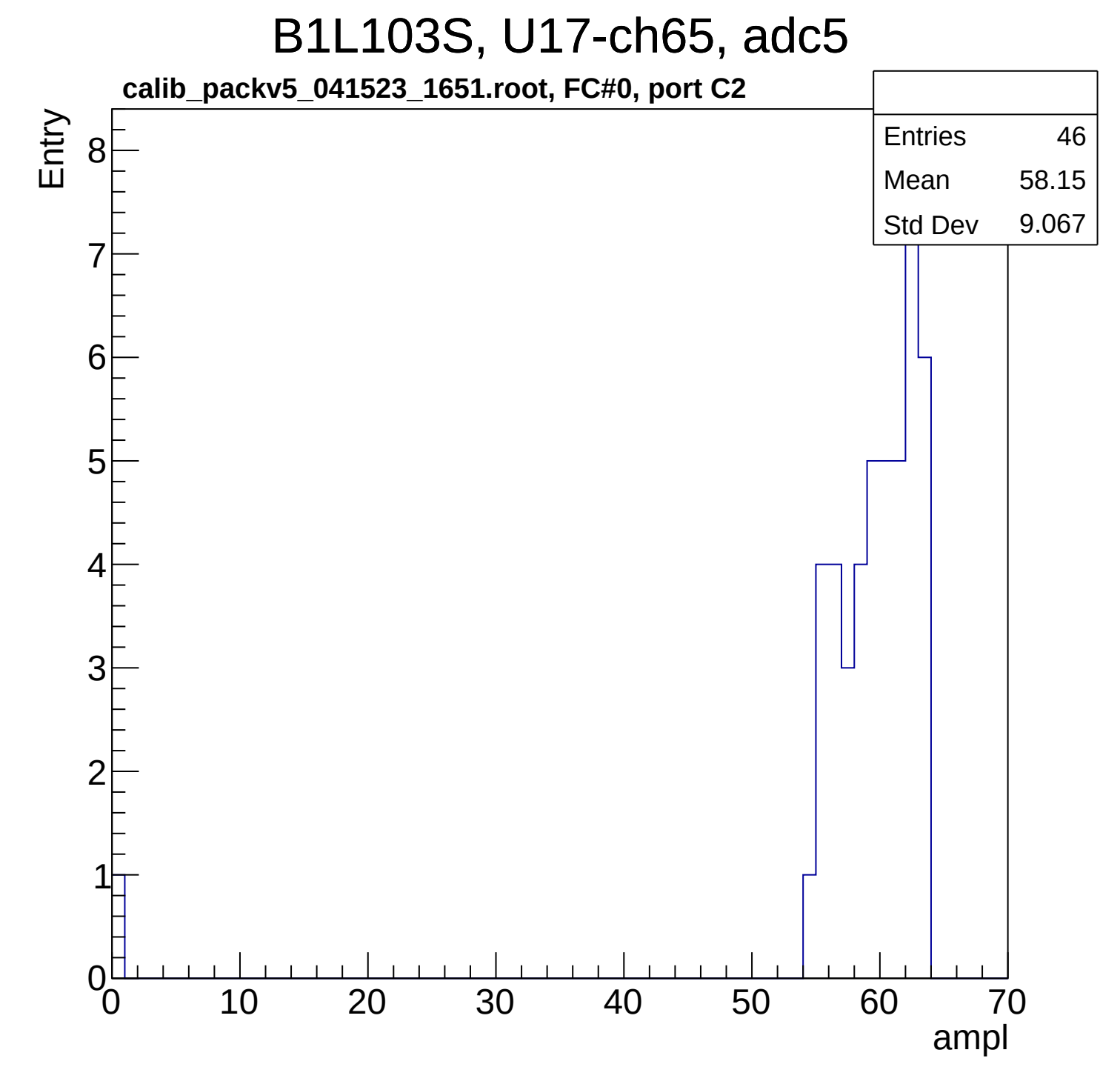
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U17-ch65, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 34.94
Std Dev 16.51
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch65, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 47.14
Std Dev 10.1
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U17-ch65, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 55.85
Std Dev 3.363
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U17-ch65, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 58.15
Std Dev 9.067
Entry
ampl
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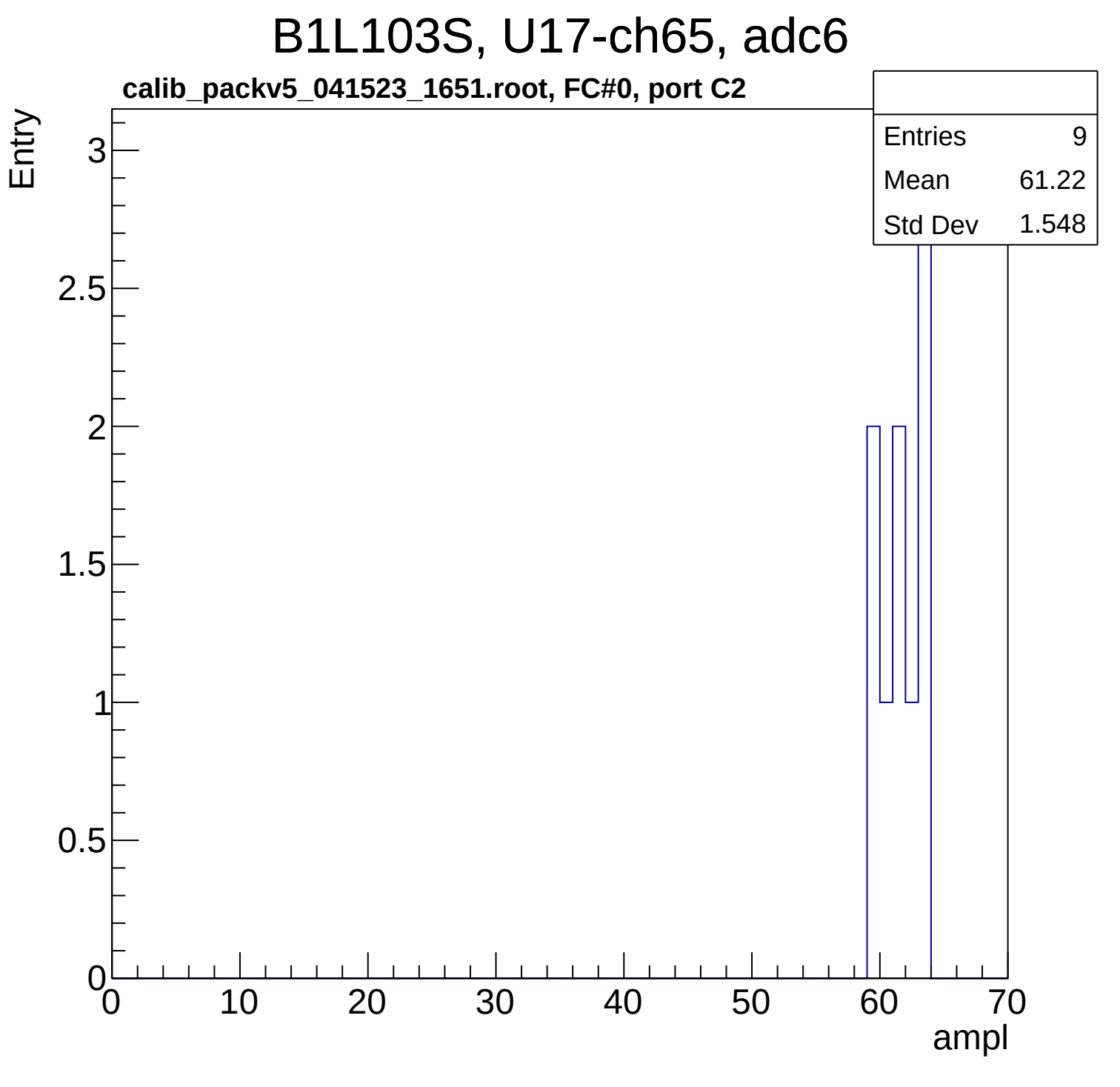
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U17-ch65, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 9
Mean 61.22
Std Dev 1.548
Entry
ampl
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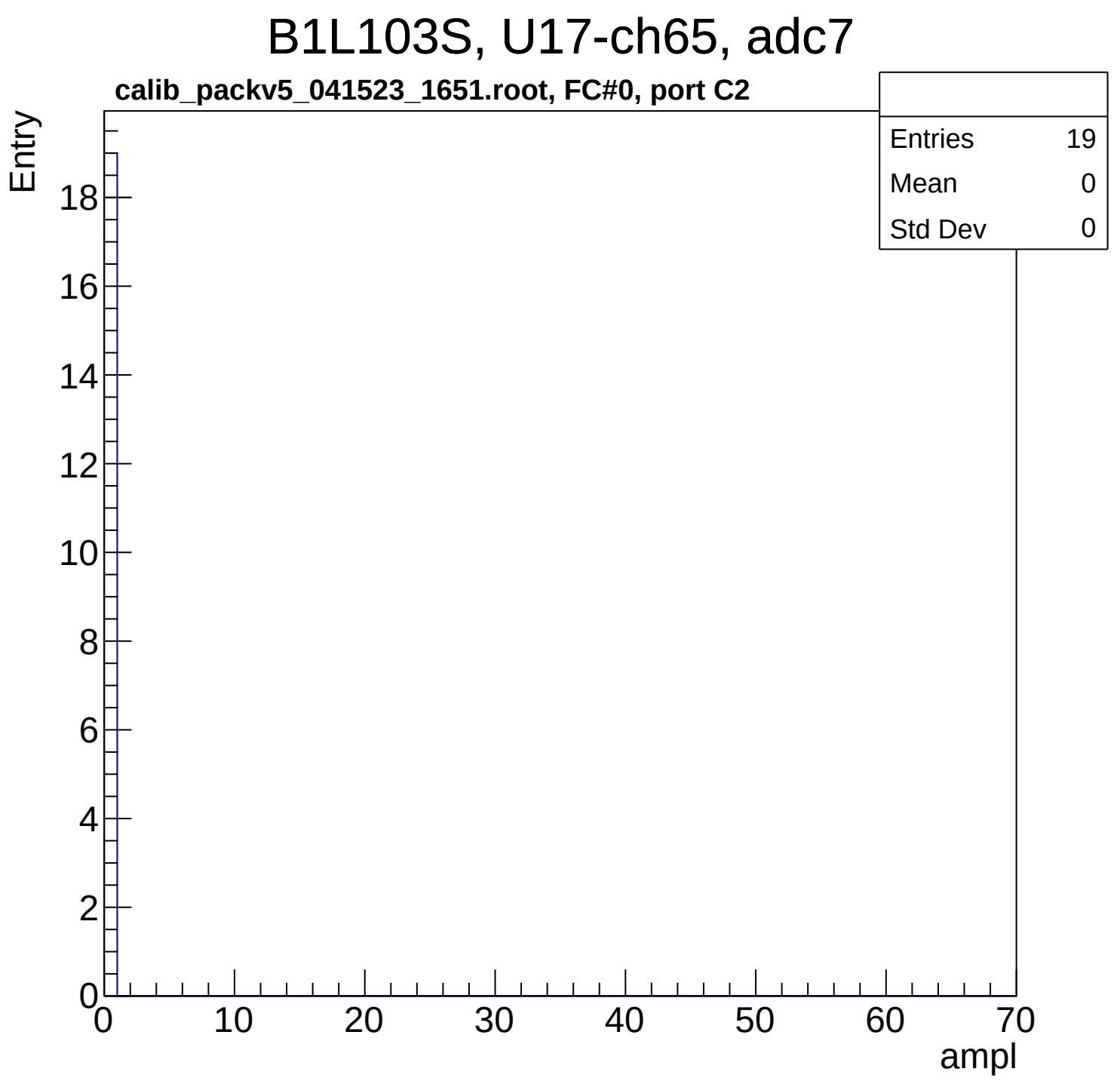
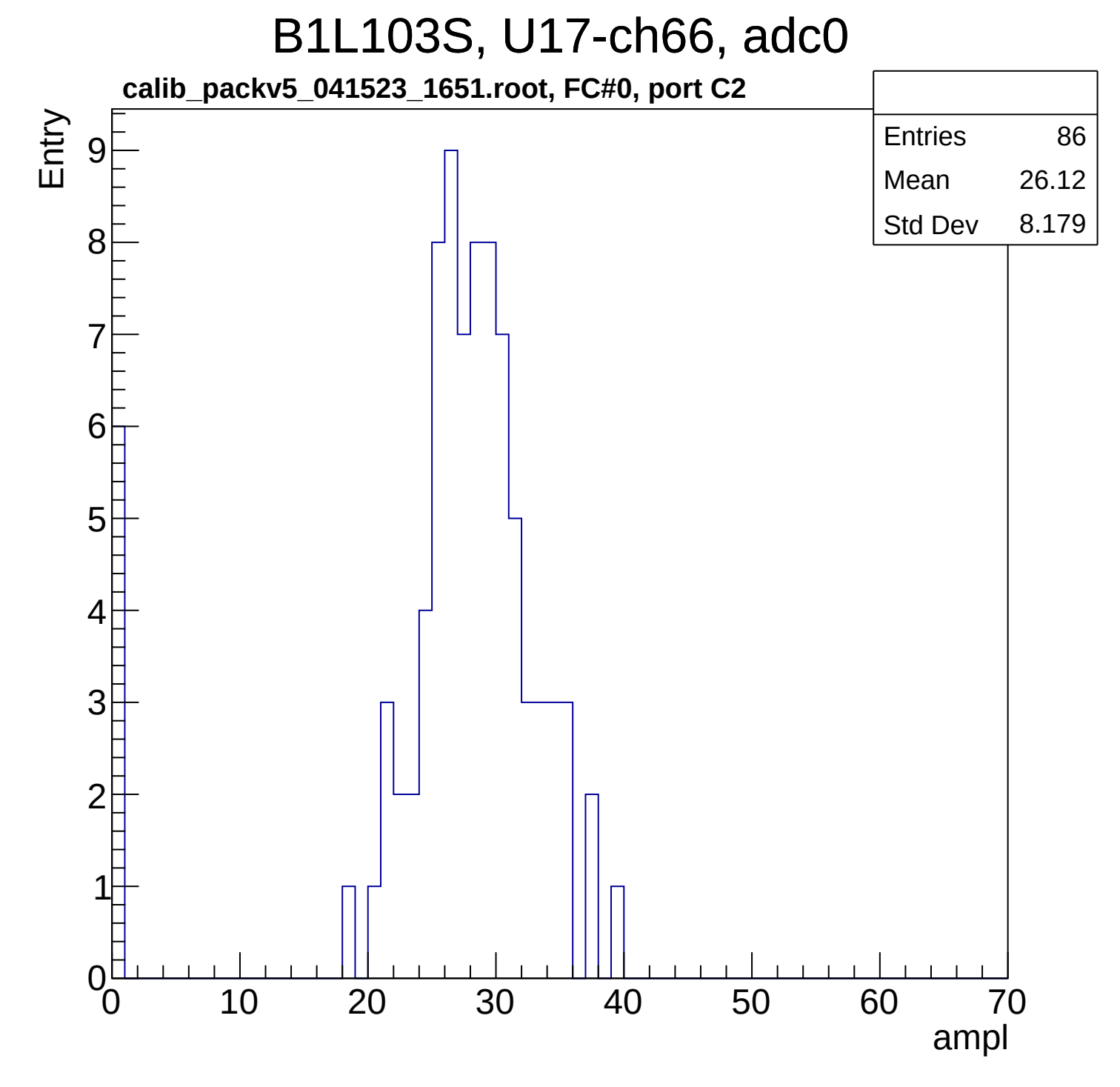
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U17-ch65, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch66, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 26.12
Std Dev 8.179
Entry
ampl
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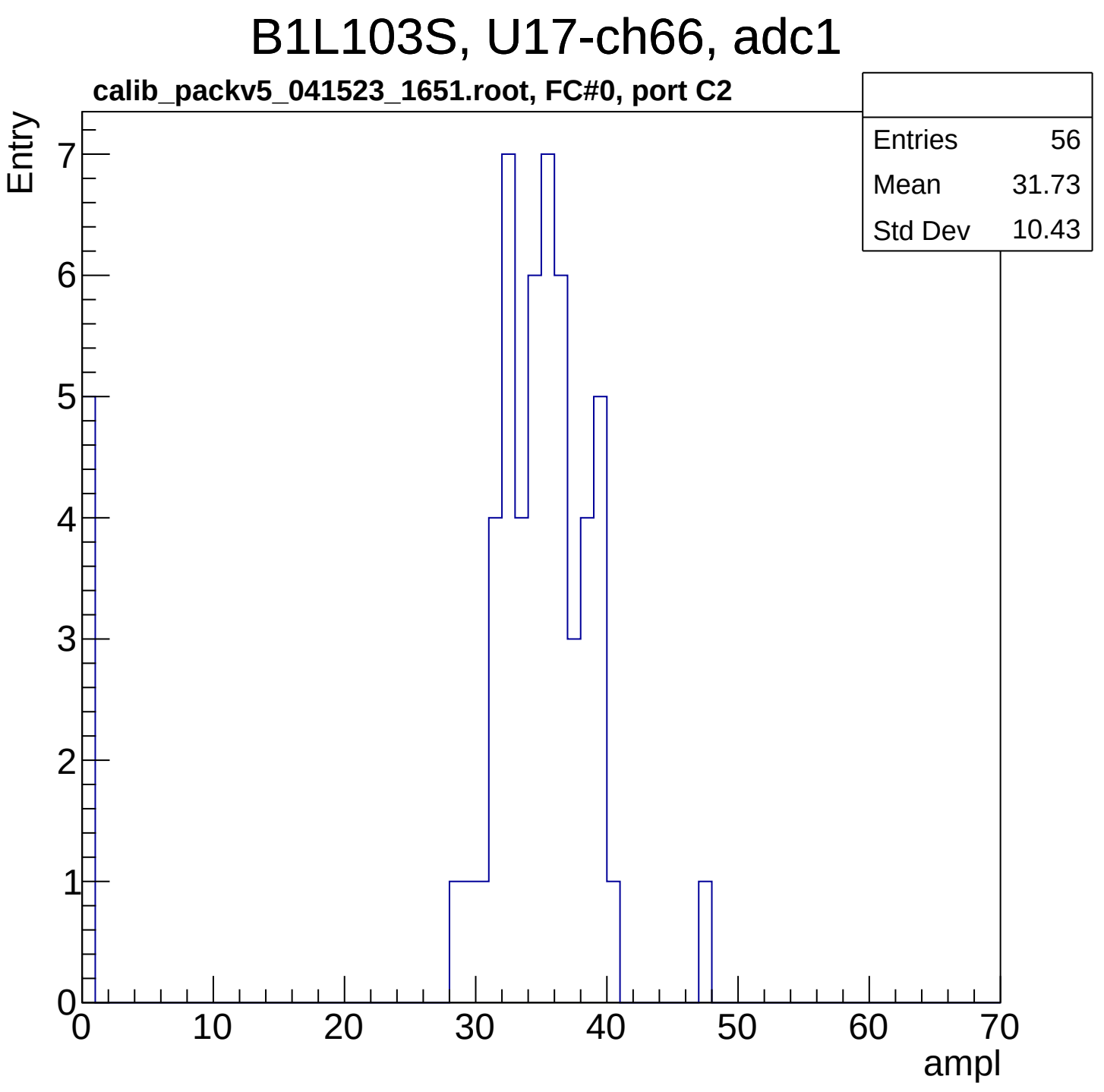
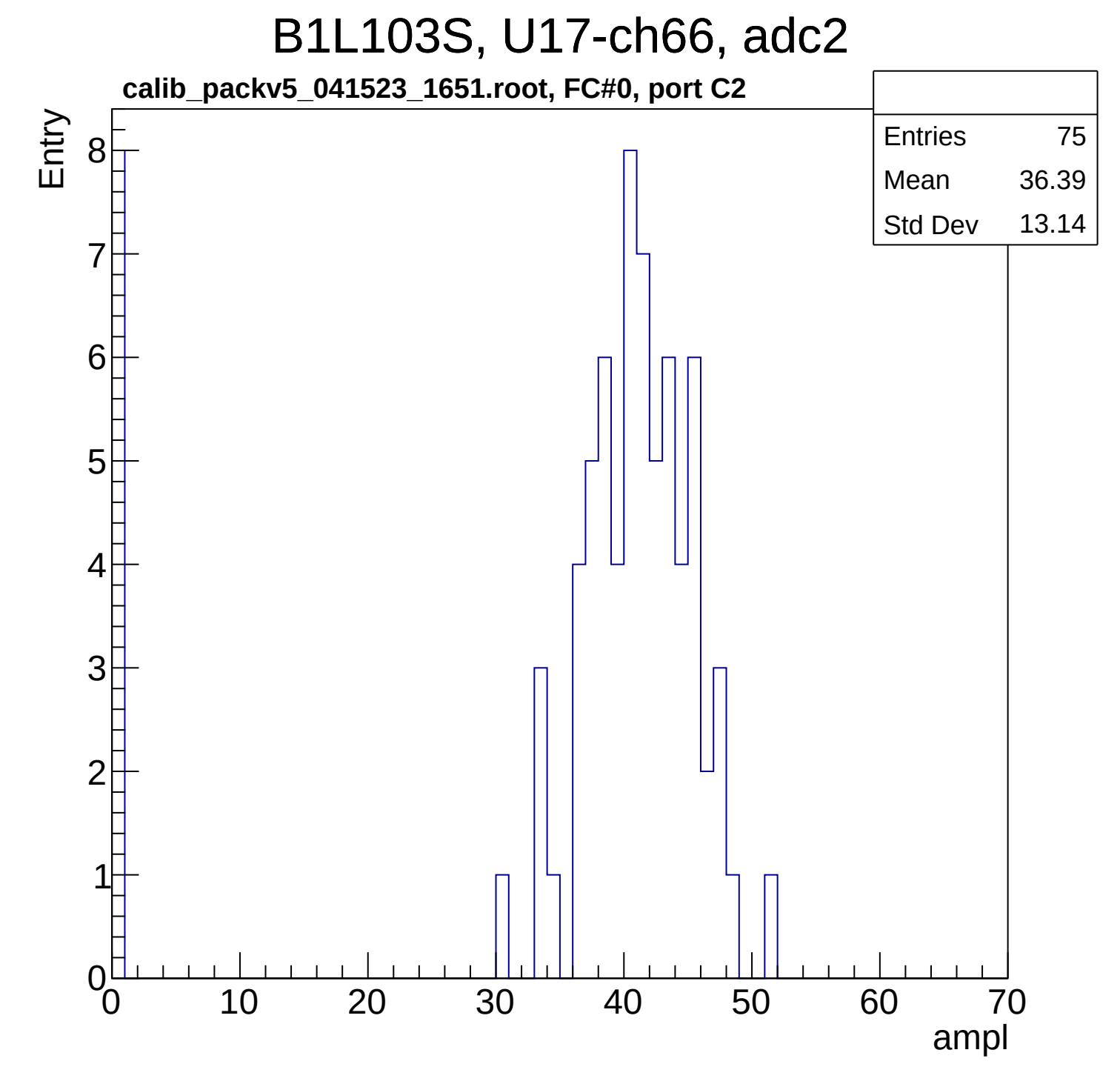
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U17-ch66, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 31.73
Std Dev 10.43
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U17-ch66, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 36.39
Std Dev 13.14
Entry
ampl
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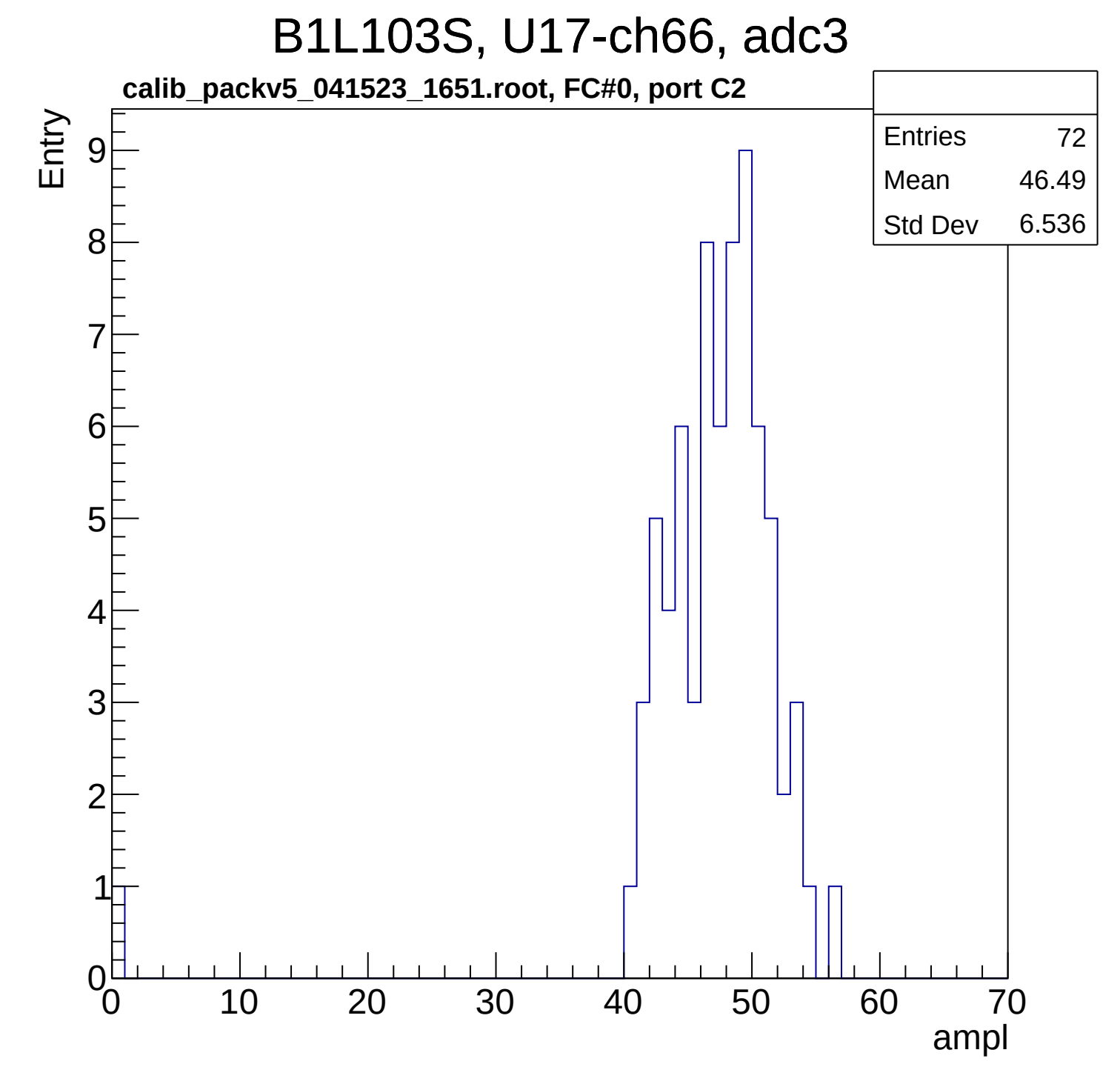
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U17-ch66, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 46.49
Std Dev 6.536
Entry
ampl
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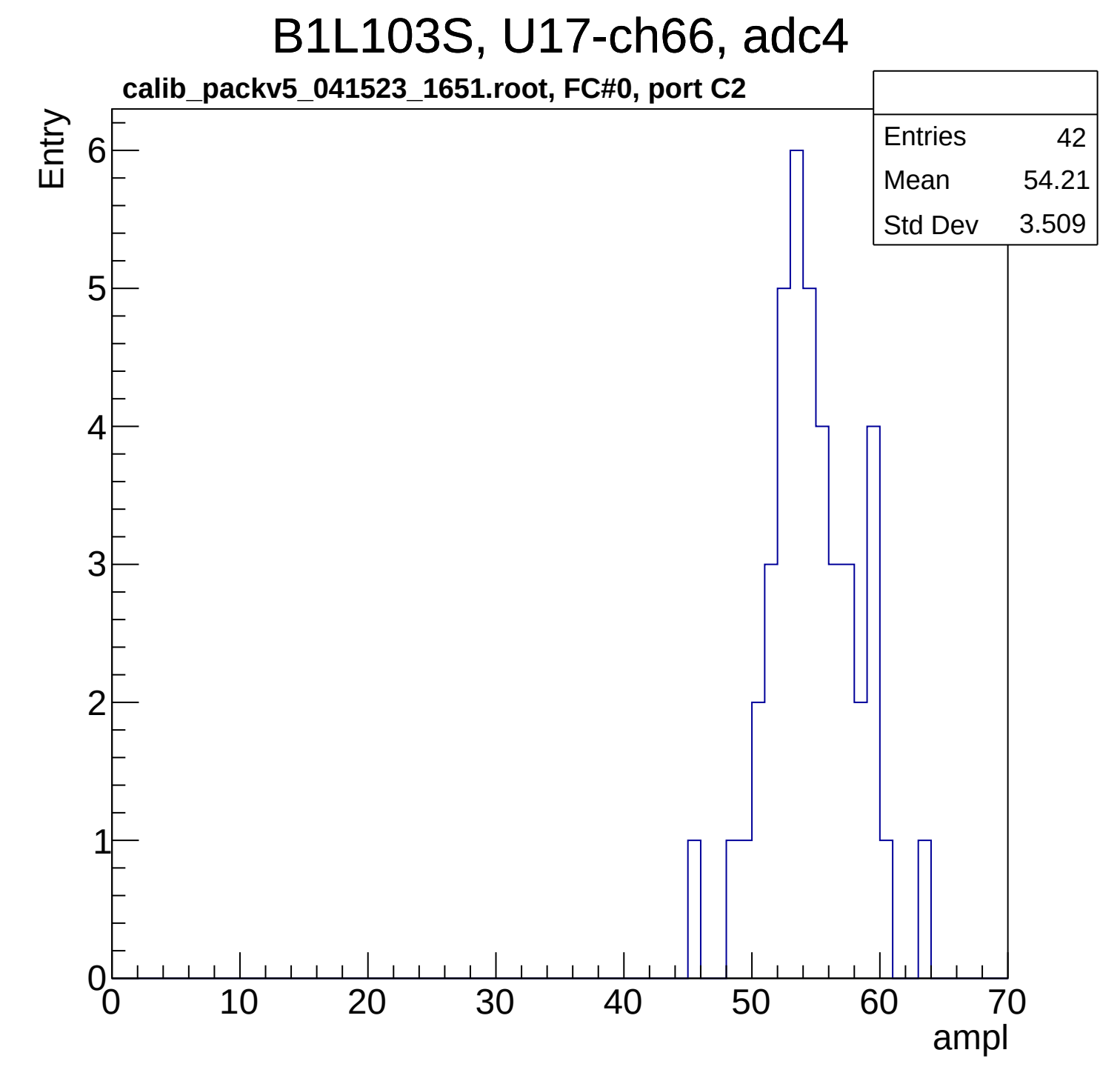
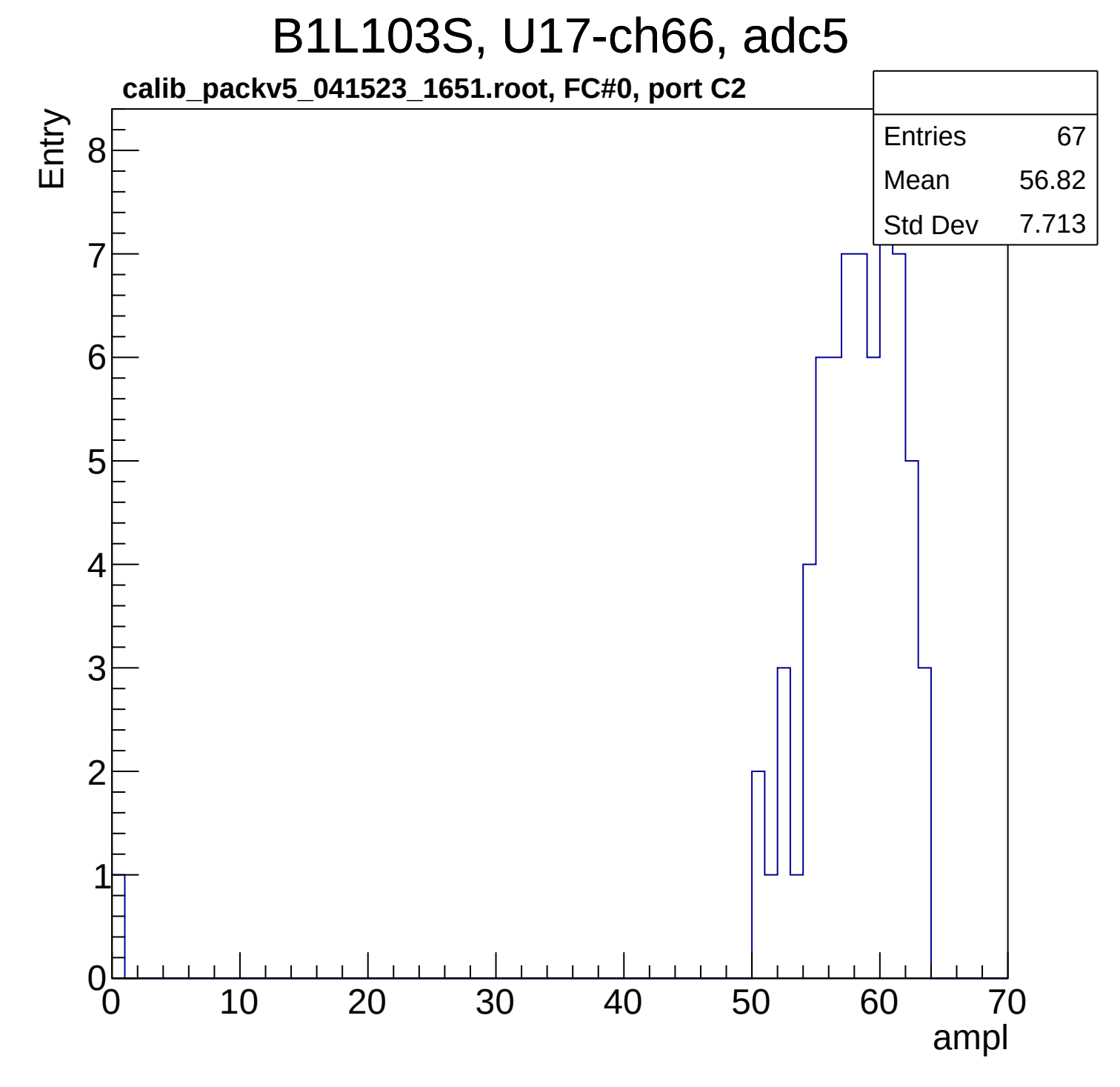
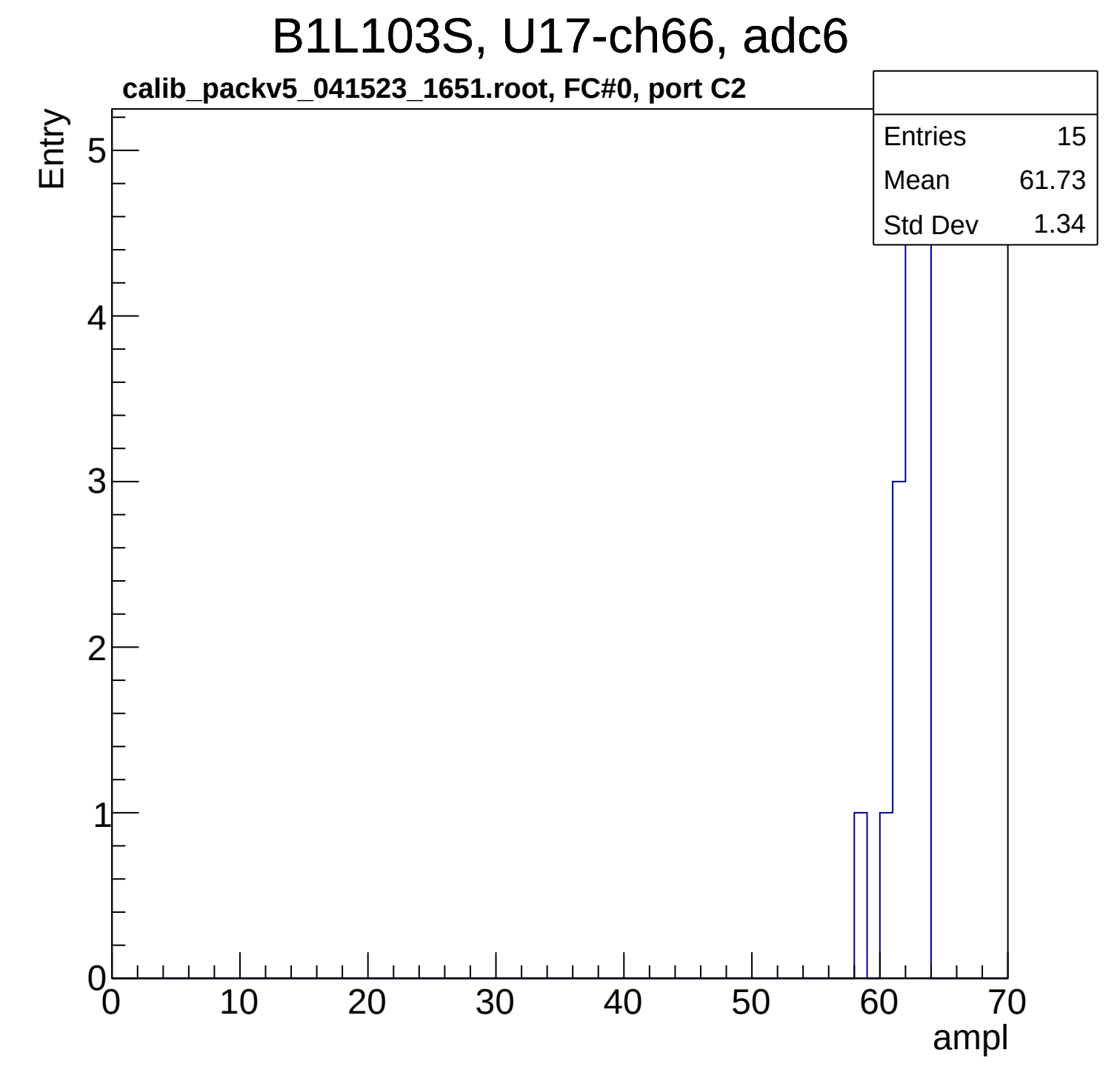
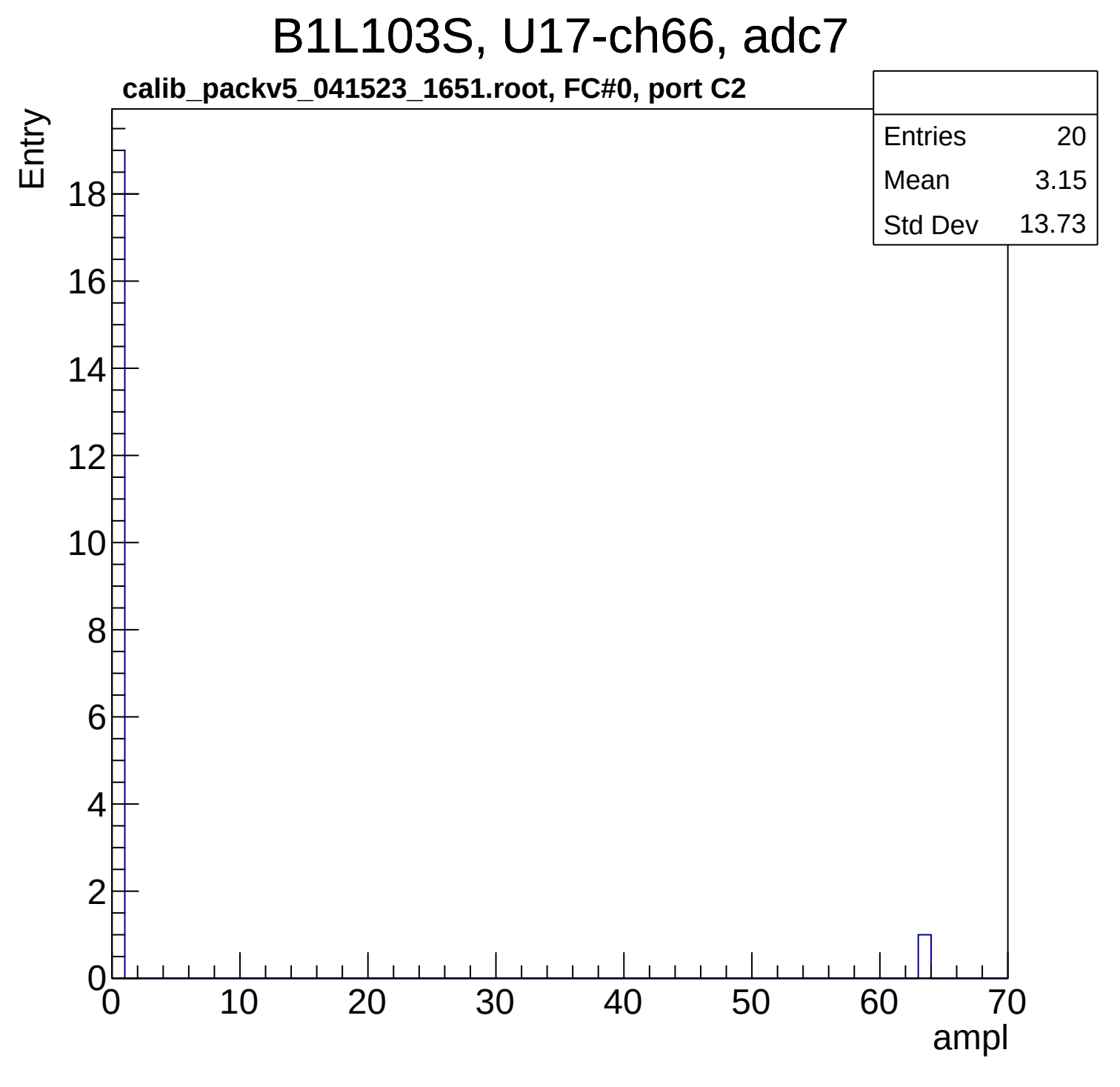
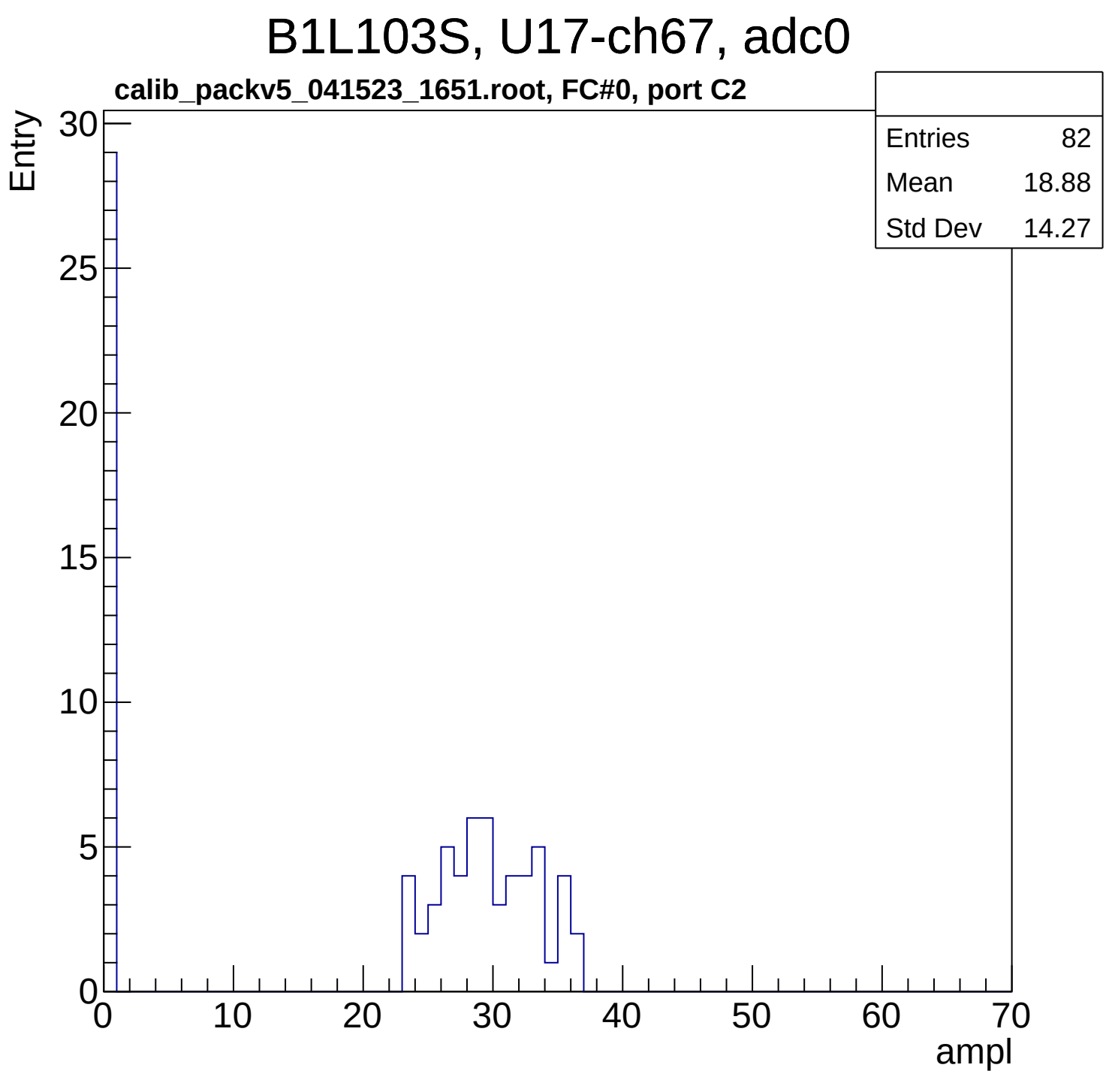
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U17-ch66, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 42
Mean 54.21
Std Dev 3.509
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U17-ch66, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 56.82
Std Dev 7.713
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U17-ch66, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 15
Mean 61.73
Std Dev 1.34
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U17-ch66, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch67, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 18.88
Std Dev 14.27
Entry
ampl
0
5
10
15
20
25
30
0
10
20
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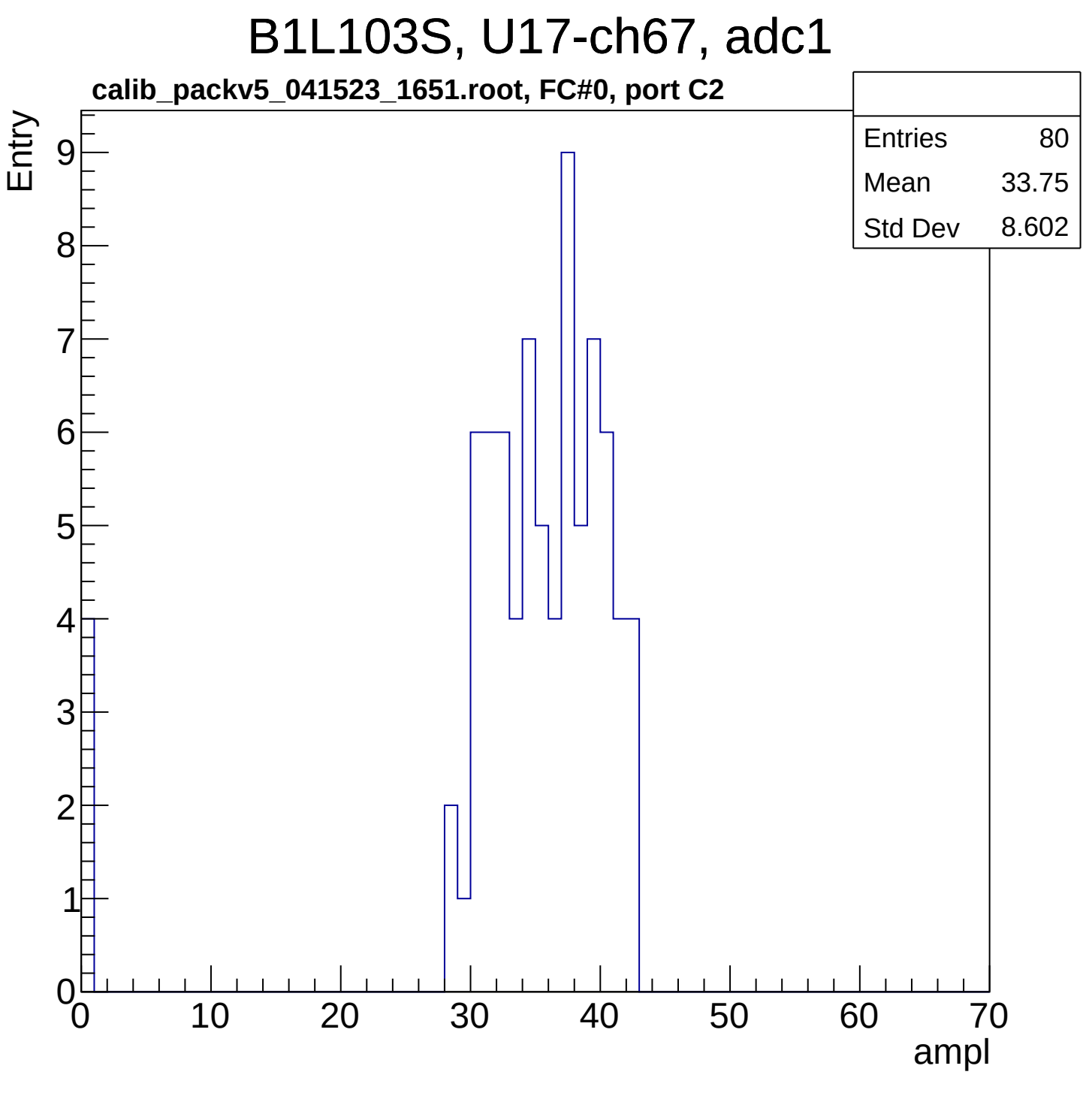
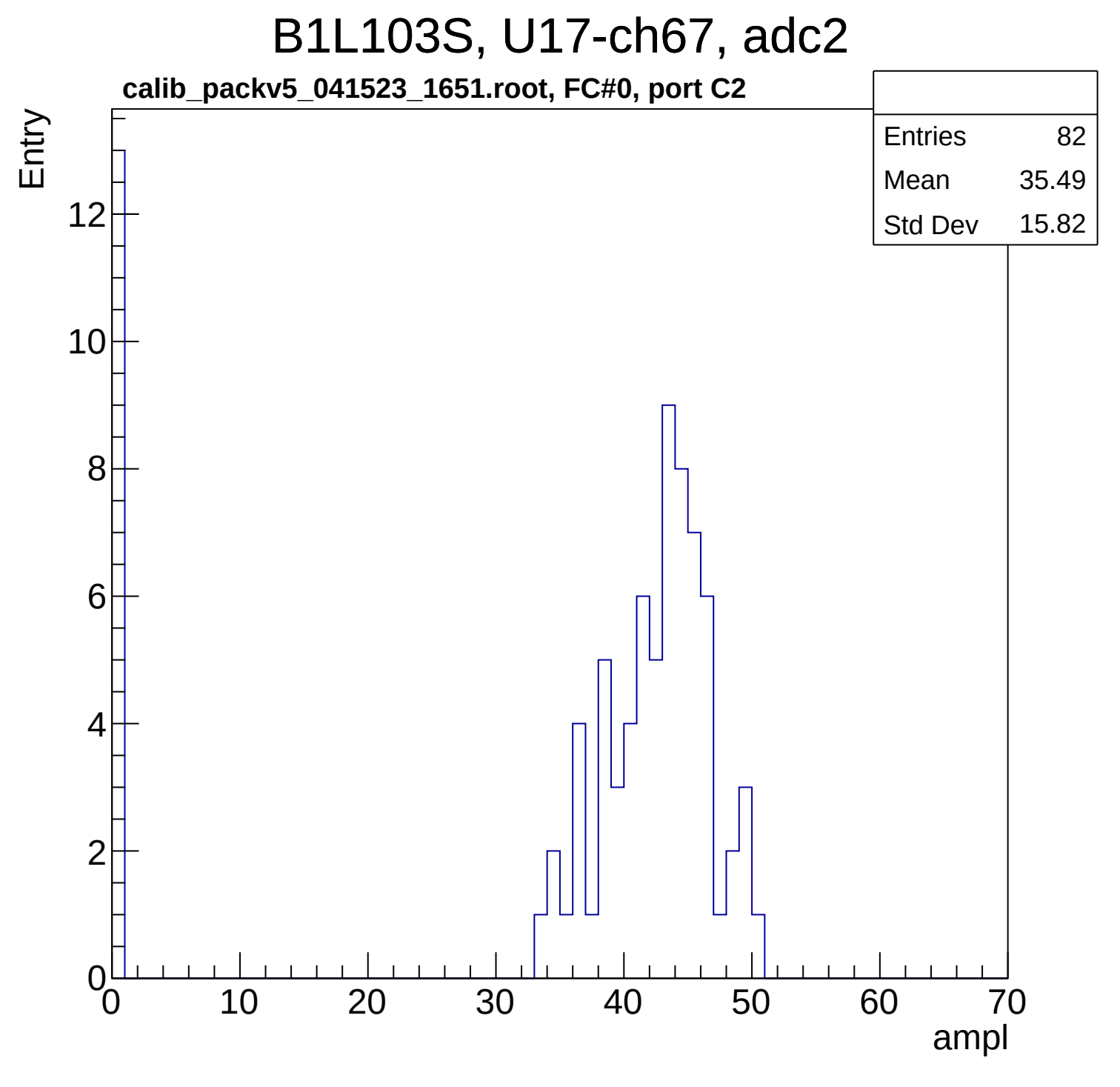
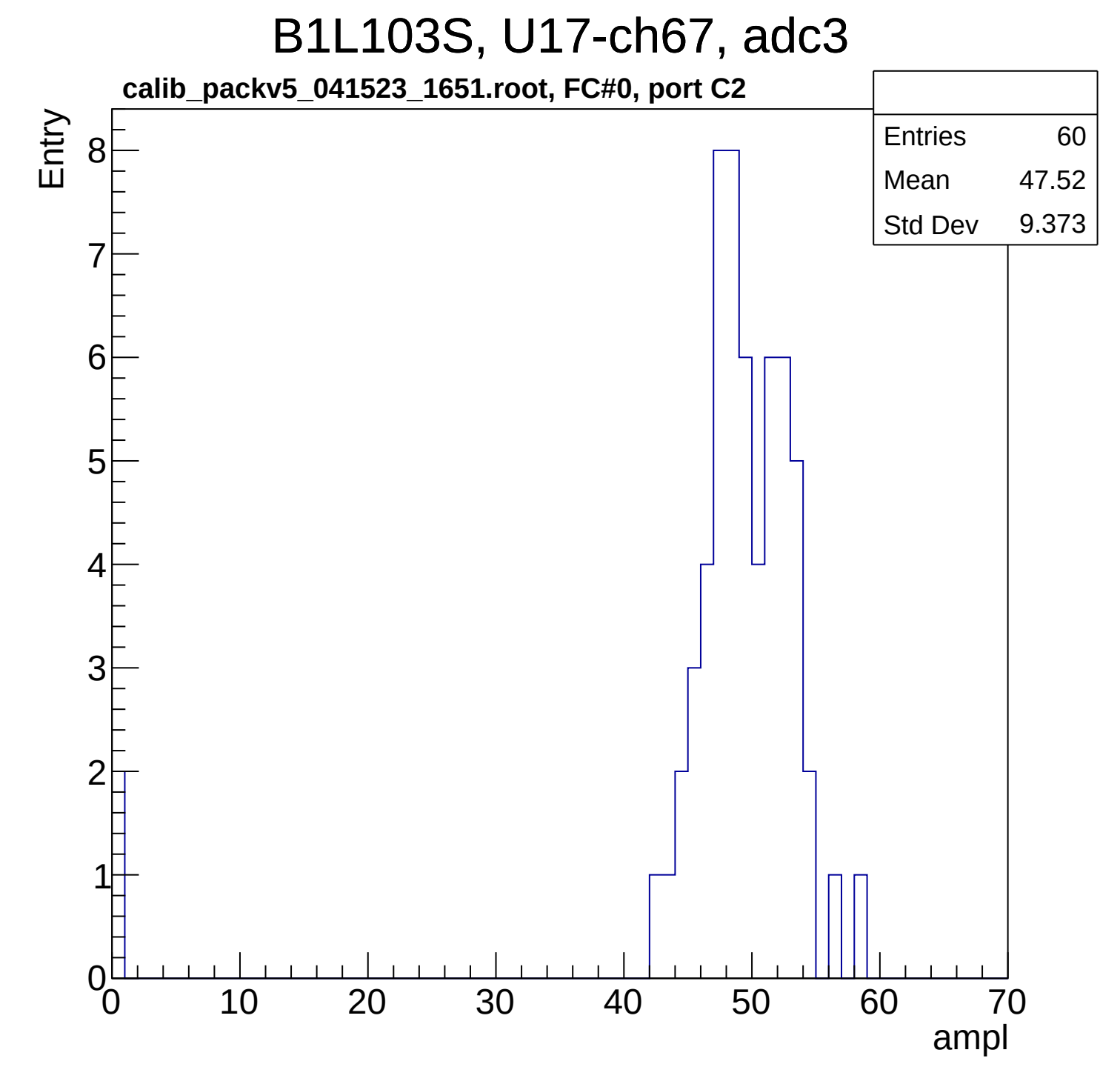
40
50
60
70


B1L103S, U17-ch67, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 33.75
Std Dev 8.602
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U17-ch67, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 35.49
Std Dev 15.82
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch67, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 47.52
Std Dev 9.373
Entry
ampl
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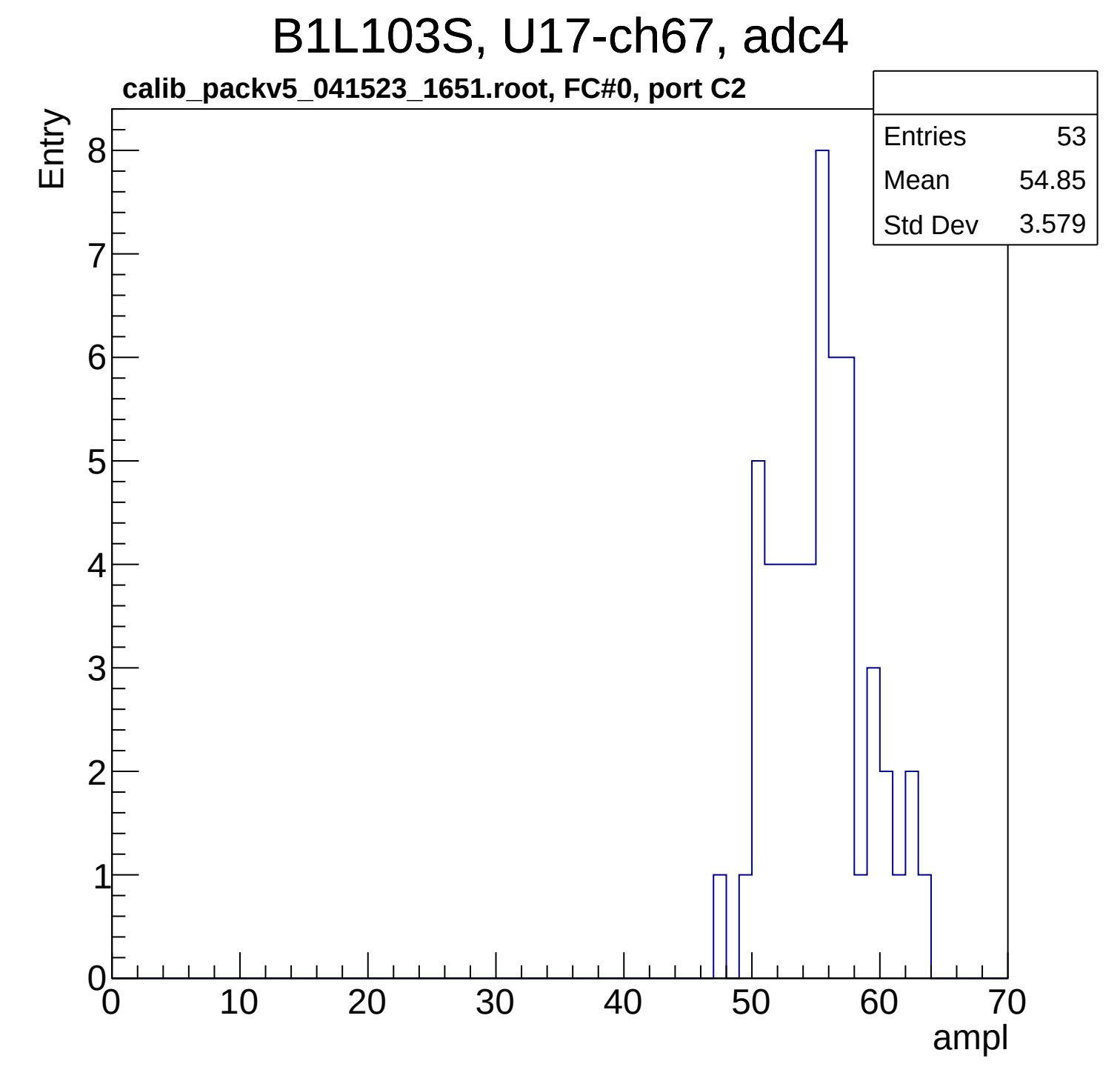
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U17-ch67, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 54.85
Std Dev 3.579
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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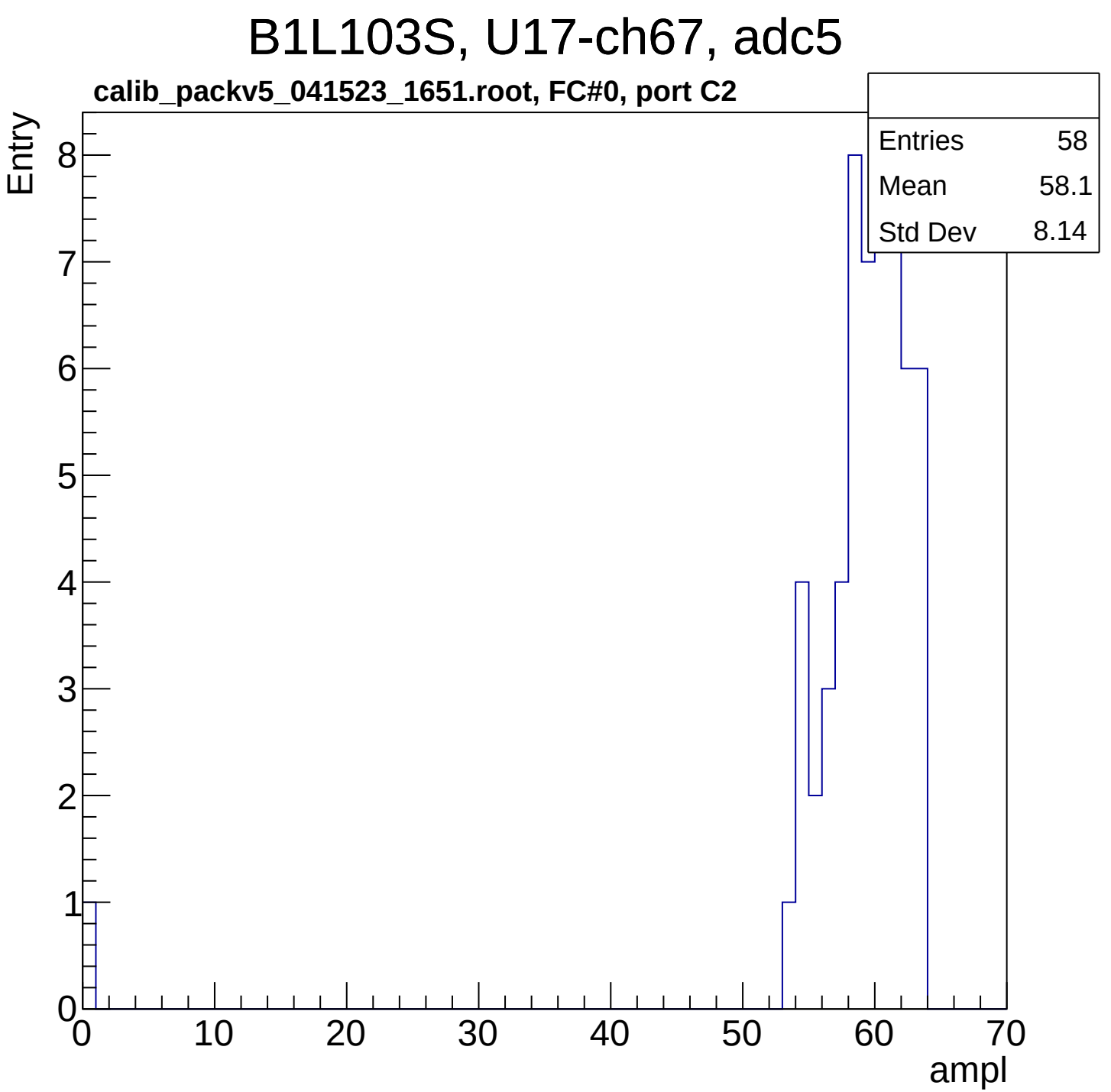
B1L103S, U17-ch67, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 58.1
Std Dev 8.14
Entry
ampl
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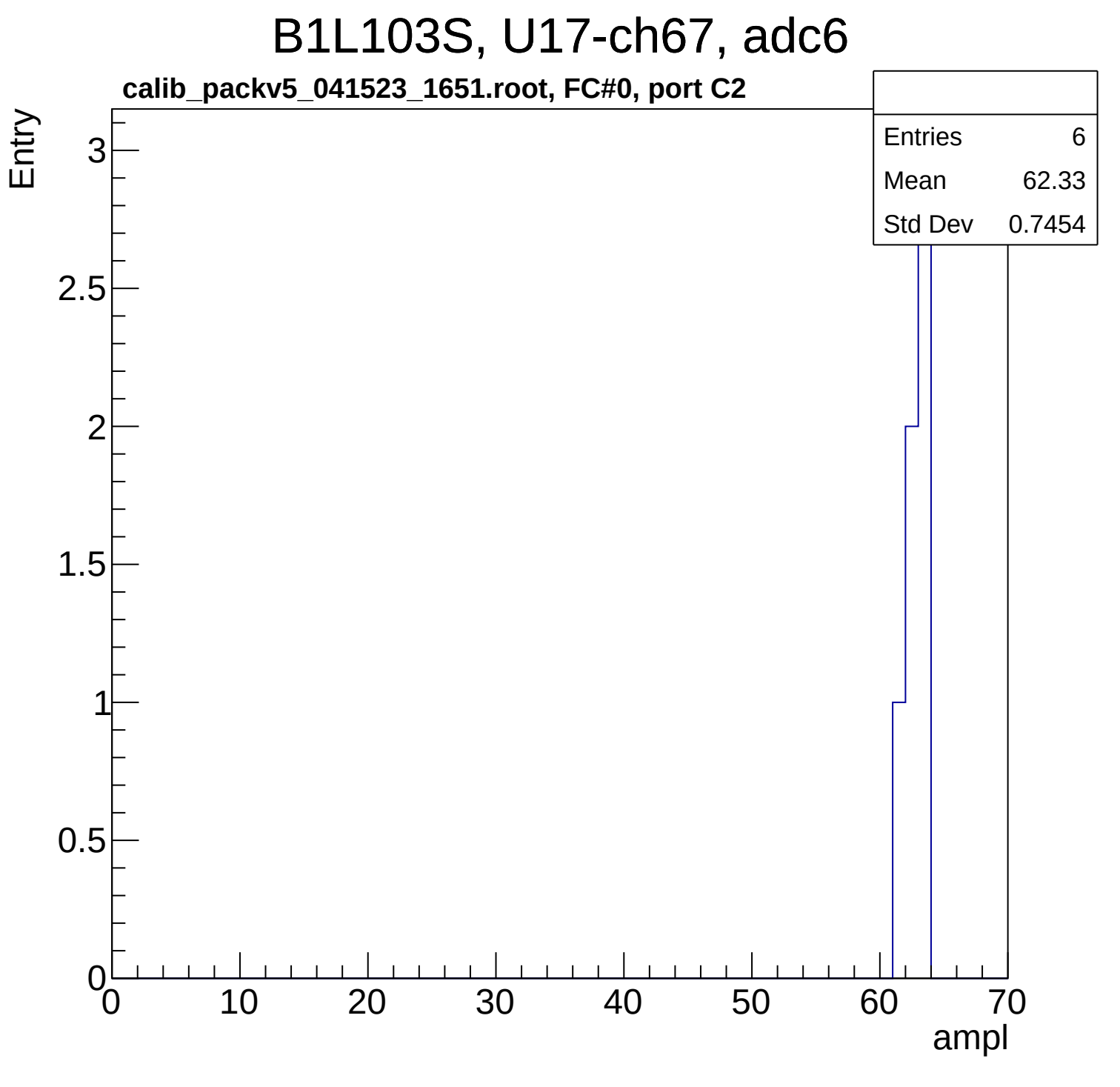
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U17-ch67, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 62.33
Std Dev 0.7454
Entry
ampl
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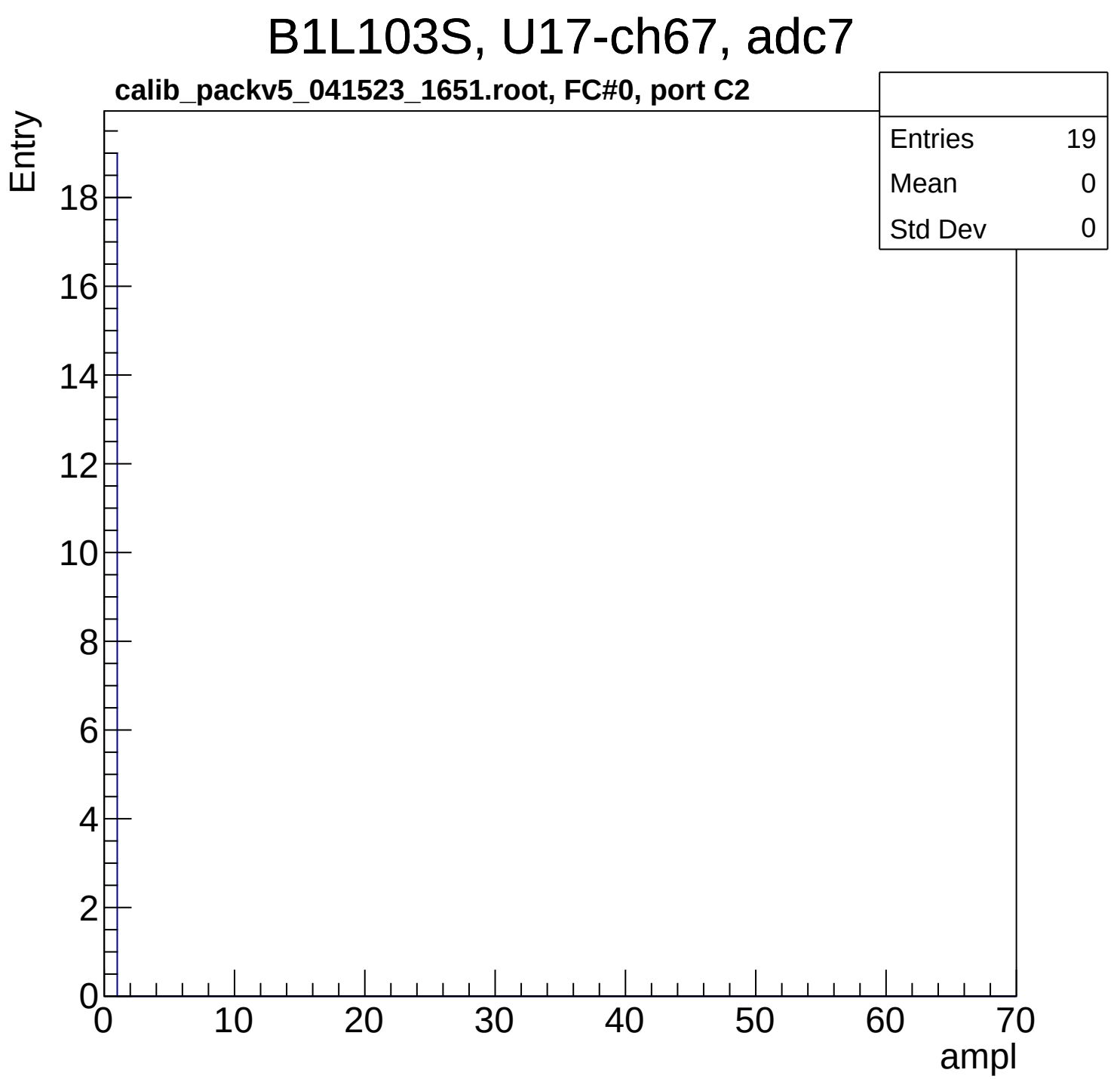
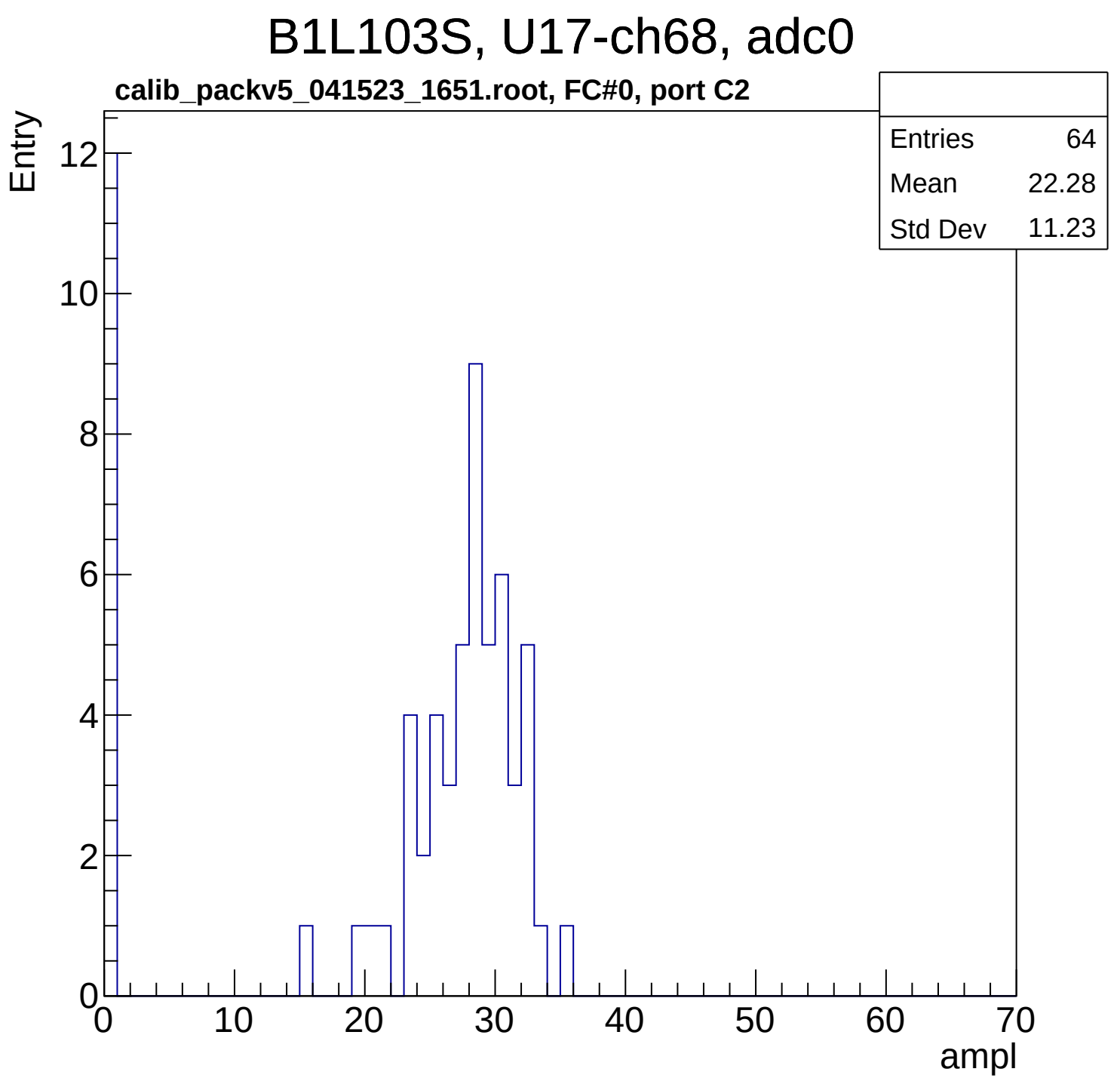
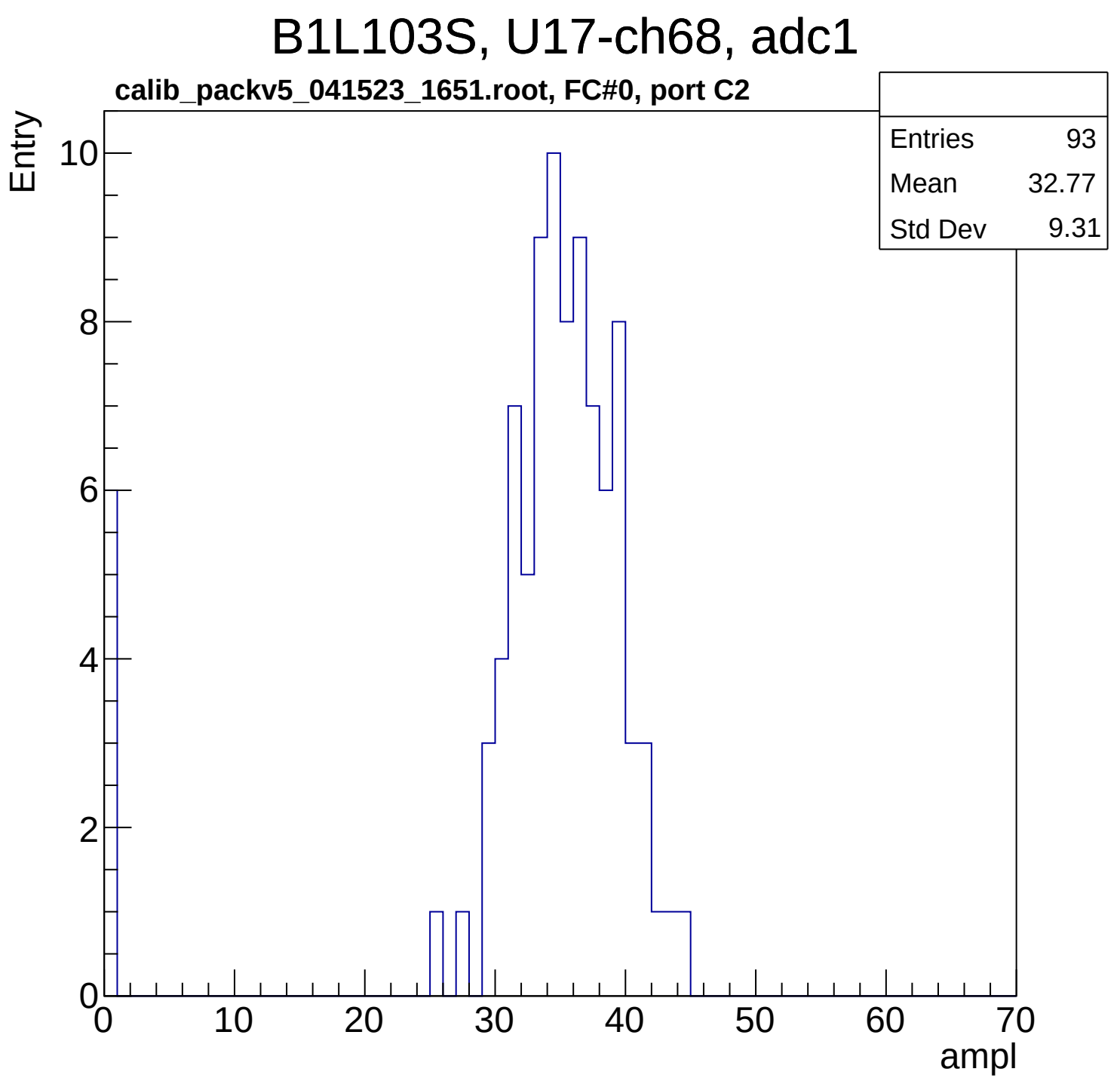
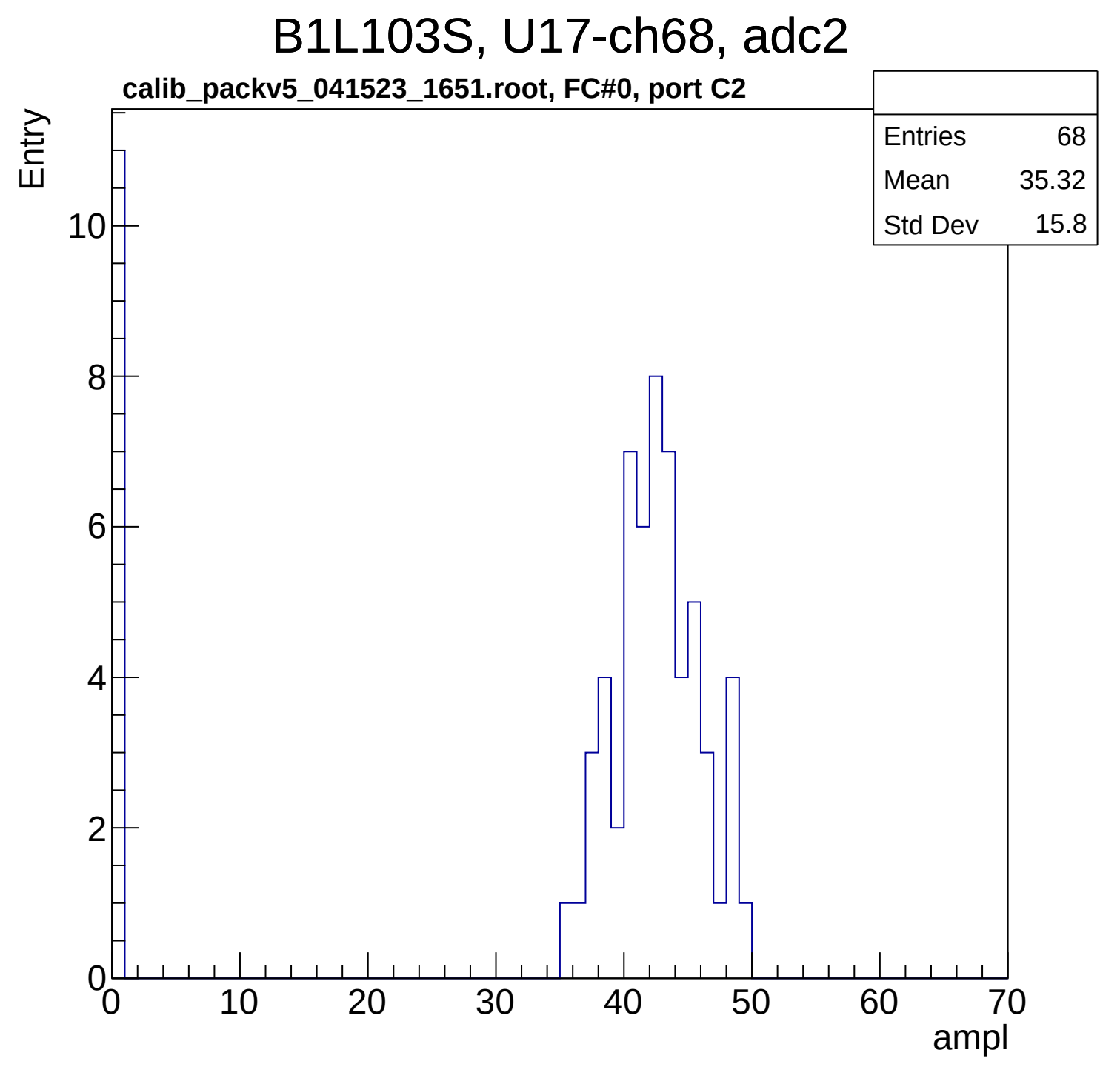
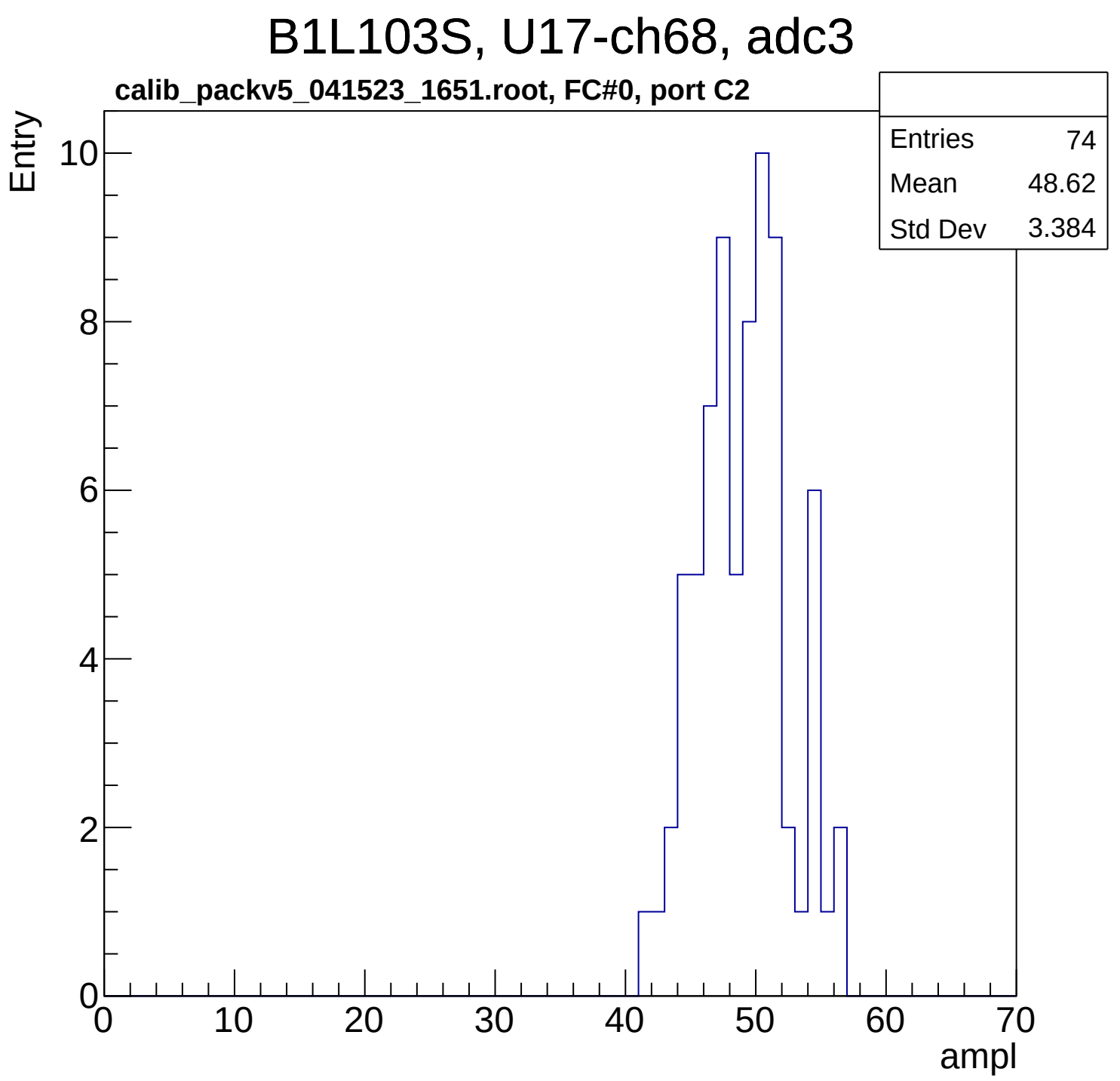
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U17-ch67, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch68, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 22.28
Std Dev 11.23
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch68, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 93
Mean 32.77
Std Dev 9.31
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U17-ch68, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 35.32
Std Dev 15.8
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch68, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 48.62
Std Dev 3.384
Entry
ampl
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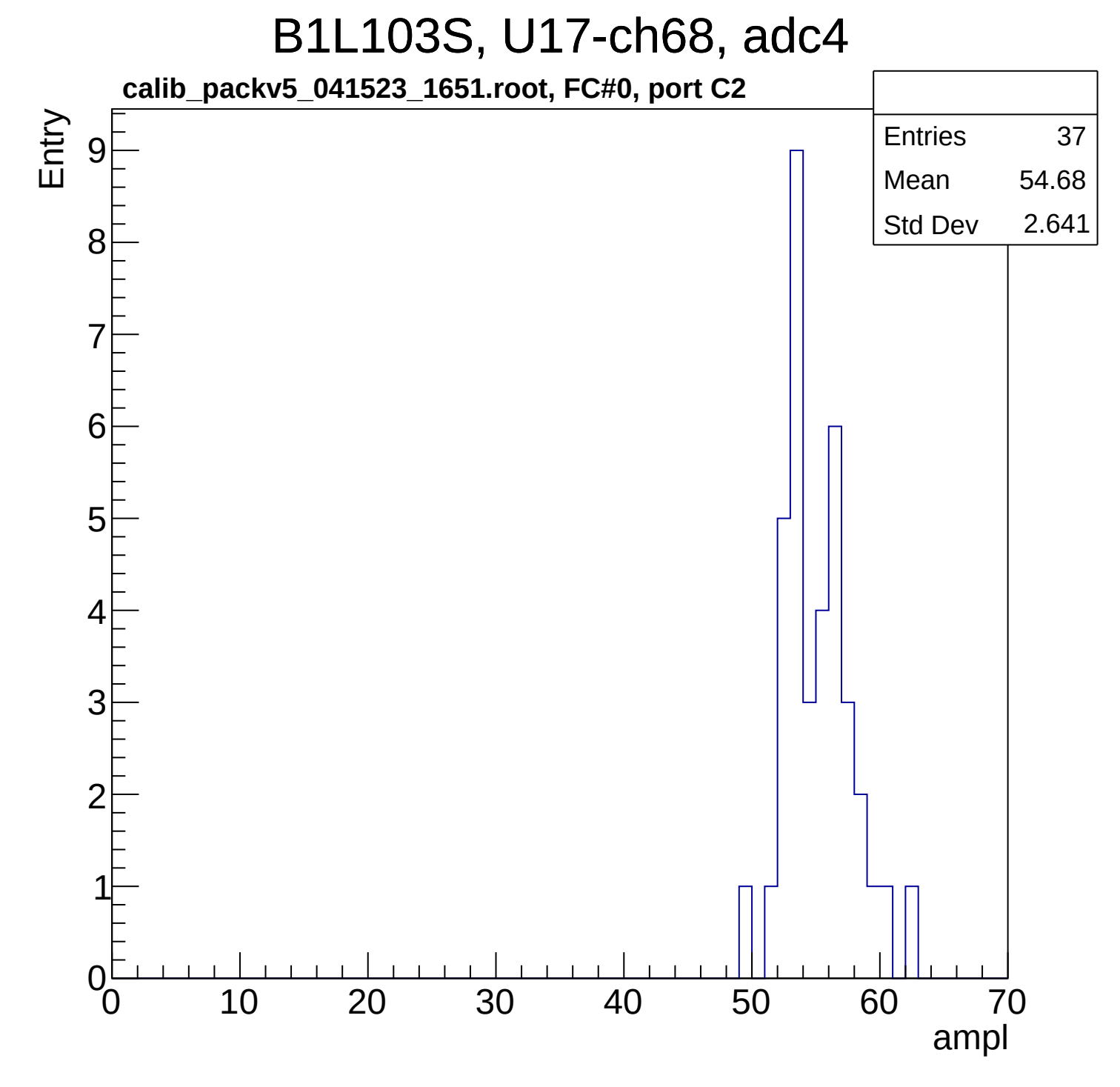
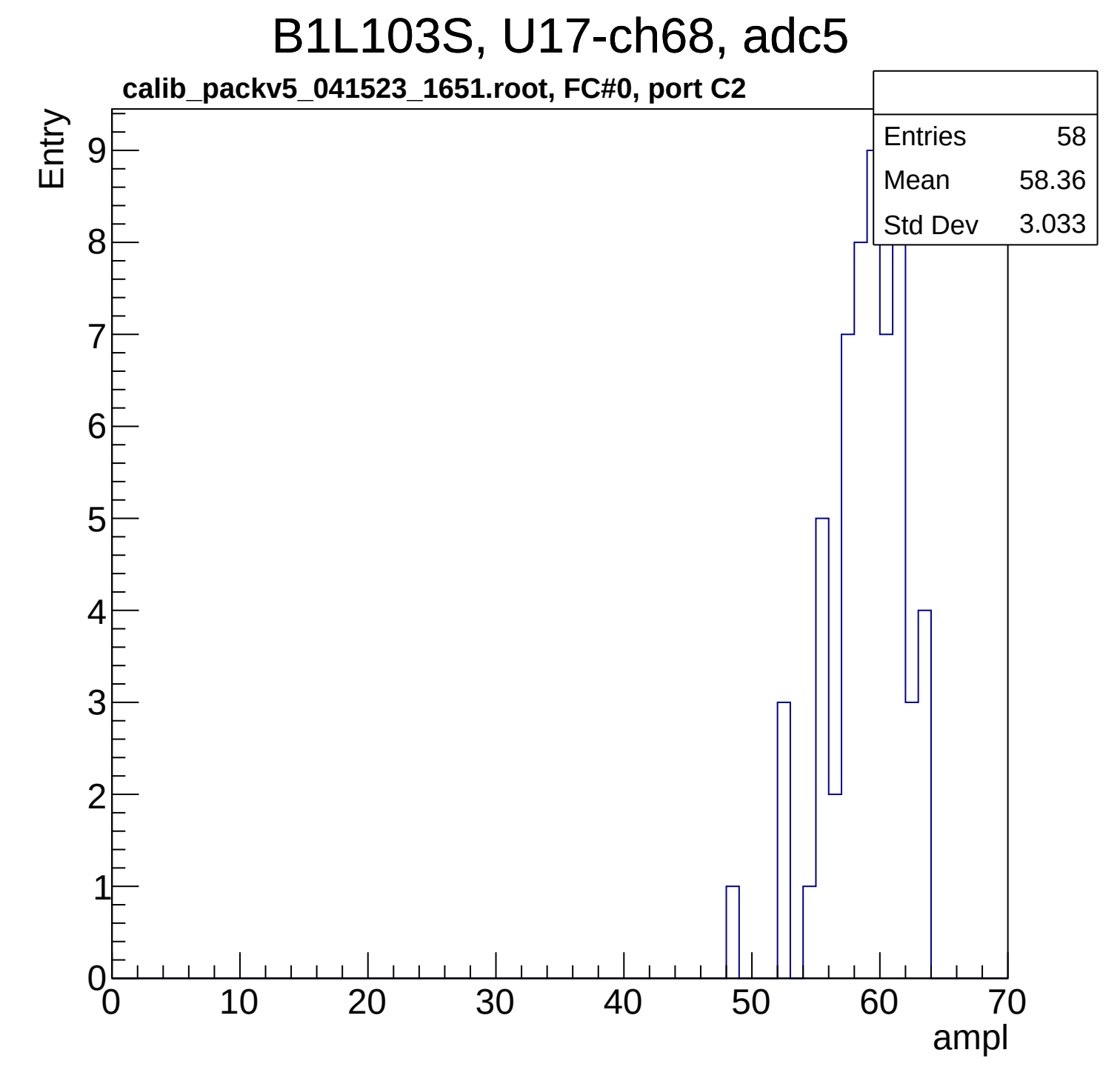
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U17-ch68, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 37
Mean 54.68
Std Dev 2.641
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U17-ch68, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 58.36
Std Dev 3.033
Entry
ampl
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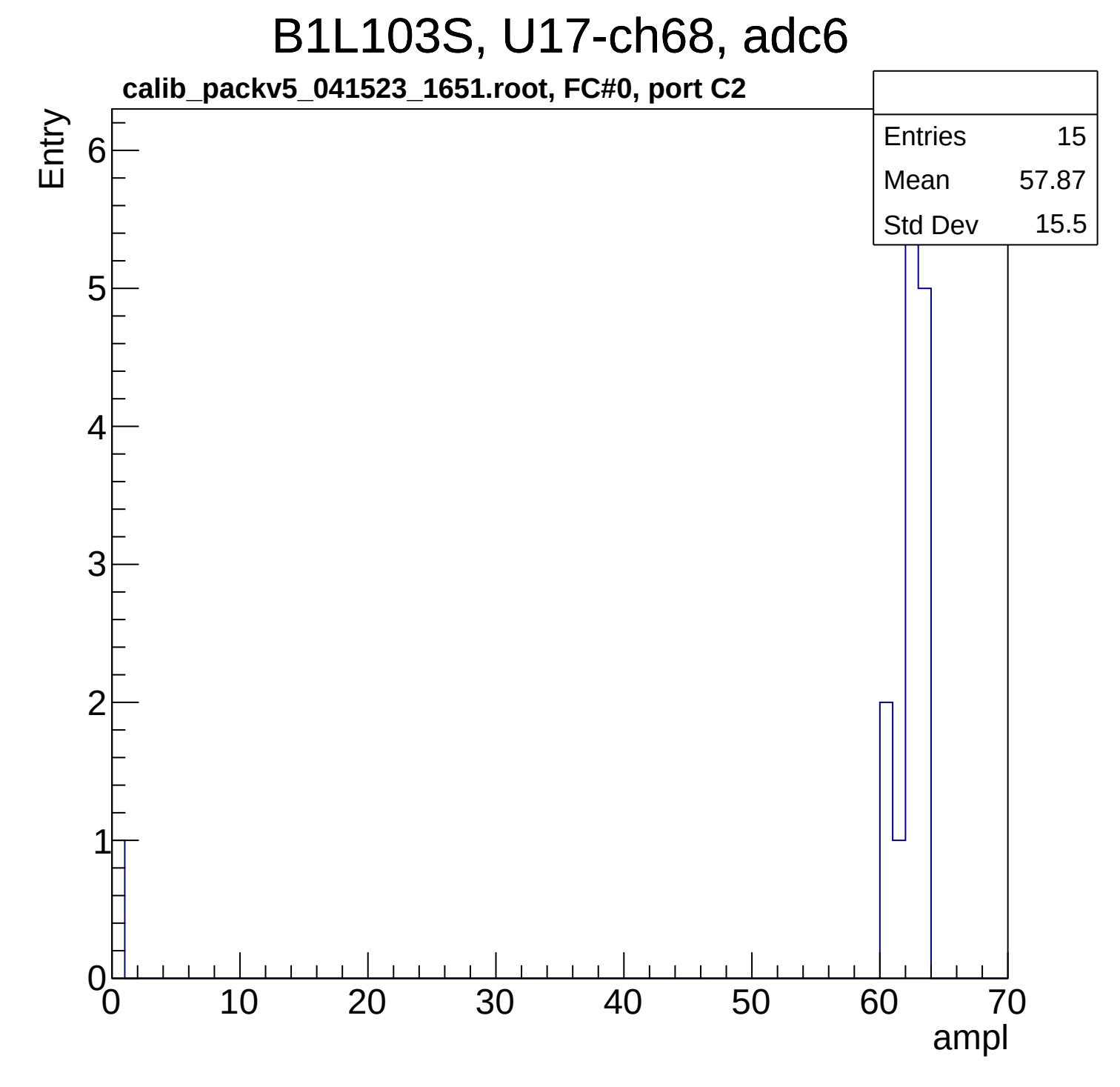
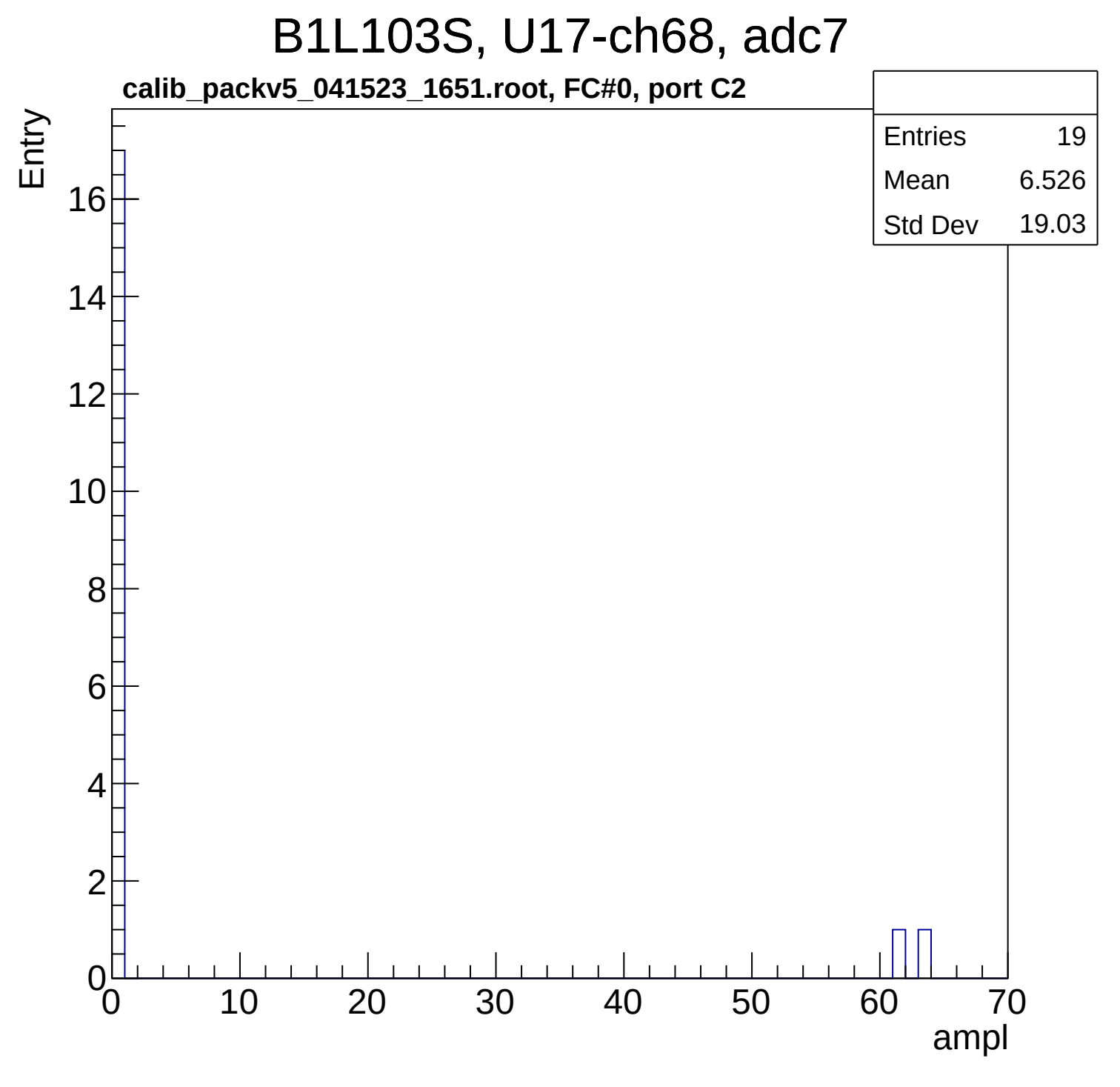
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U17-ch68, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 15
Mean 57.87
Std Dev 15.5
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U17-ch68, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 6.526
Std Dev 19.03
Entry
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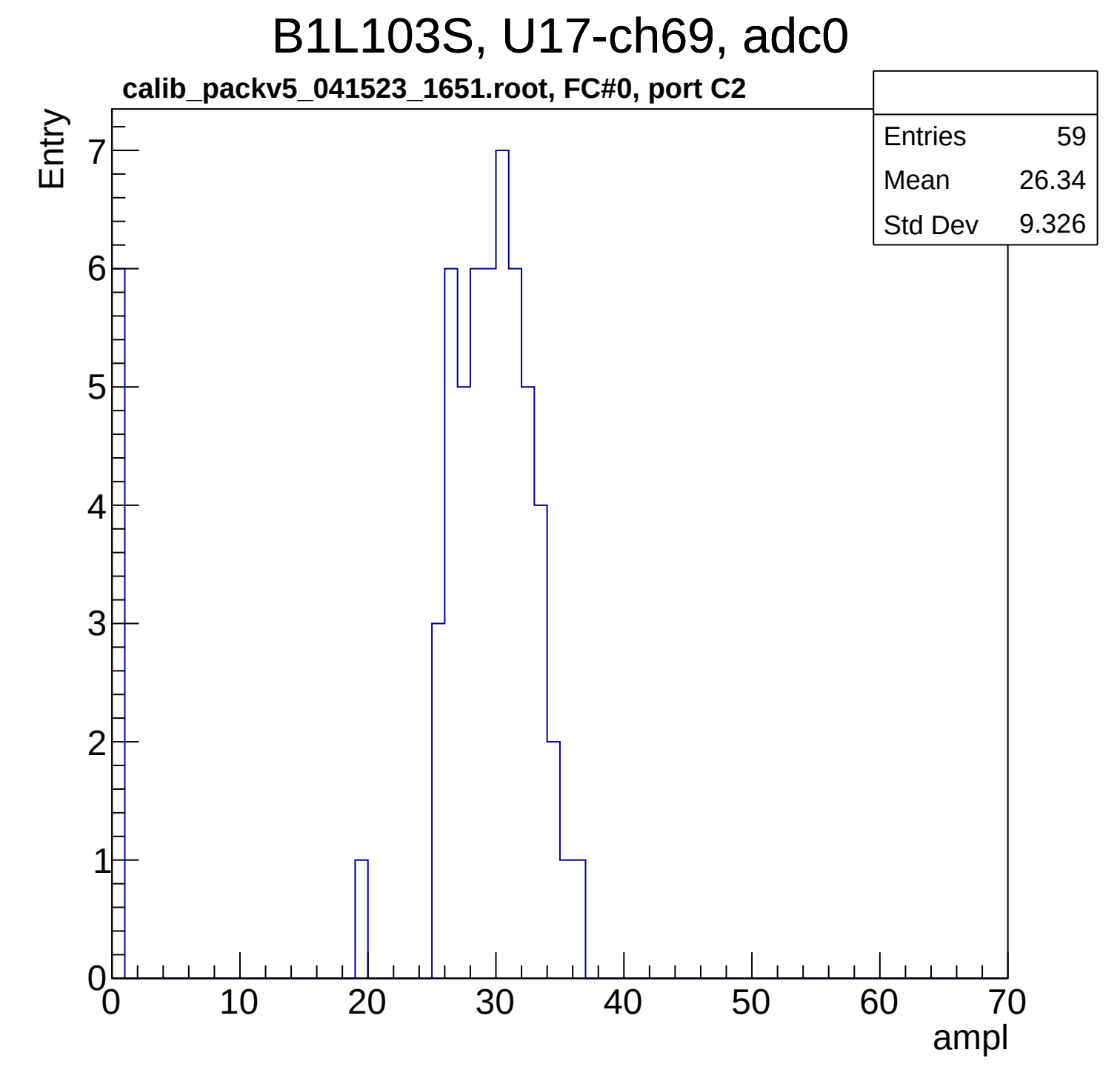
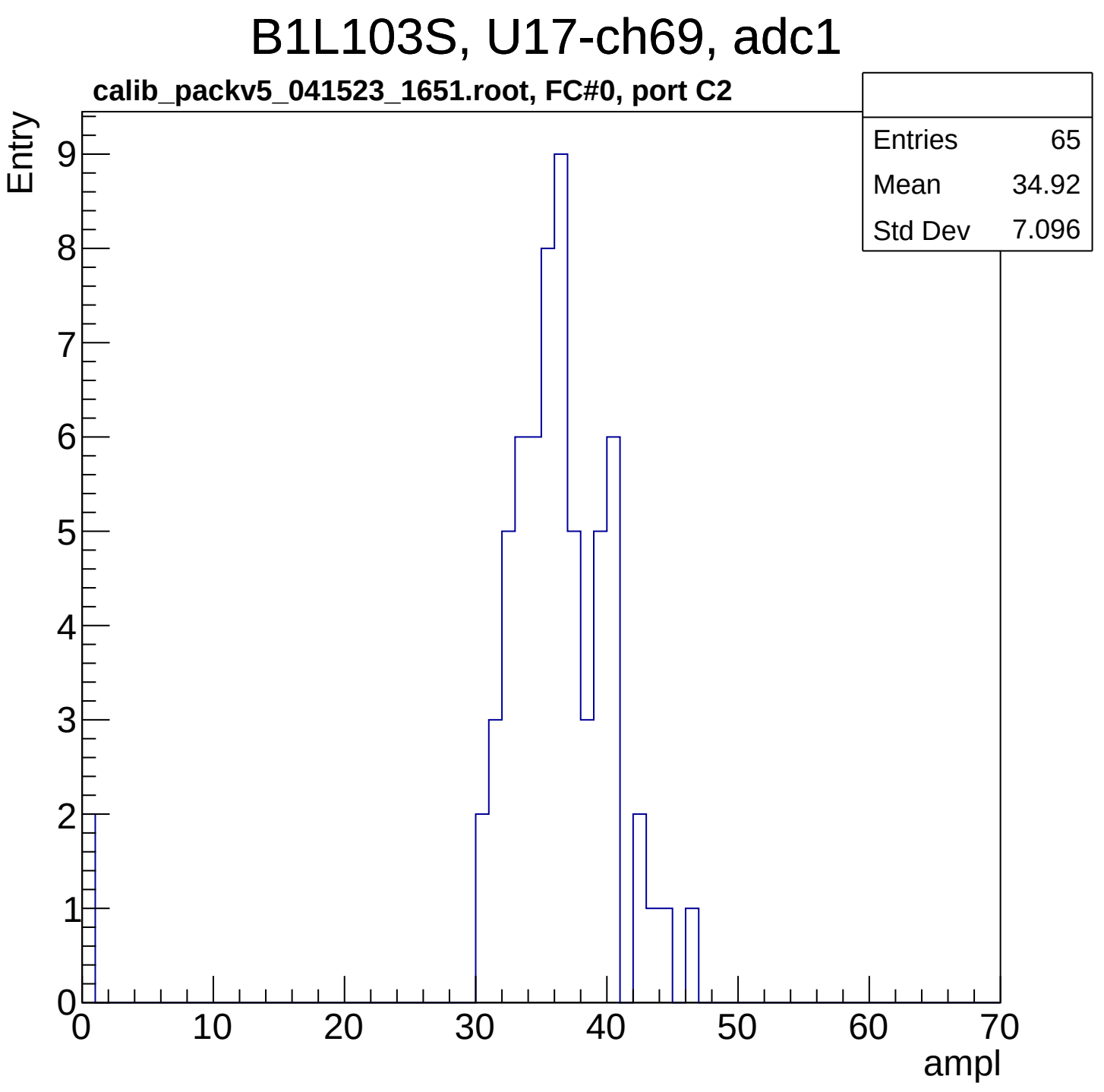
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch69, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 26.34
Std Dev 9.326
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U17-ch69, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 34.92
Std Dev 7.096
Entry
ampl
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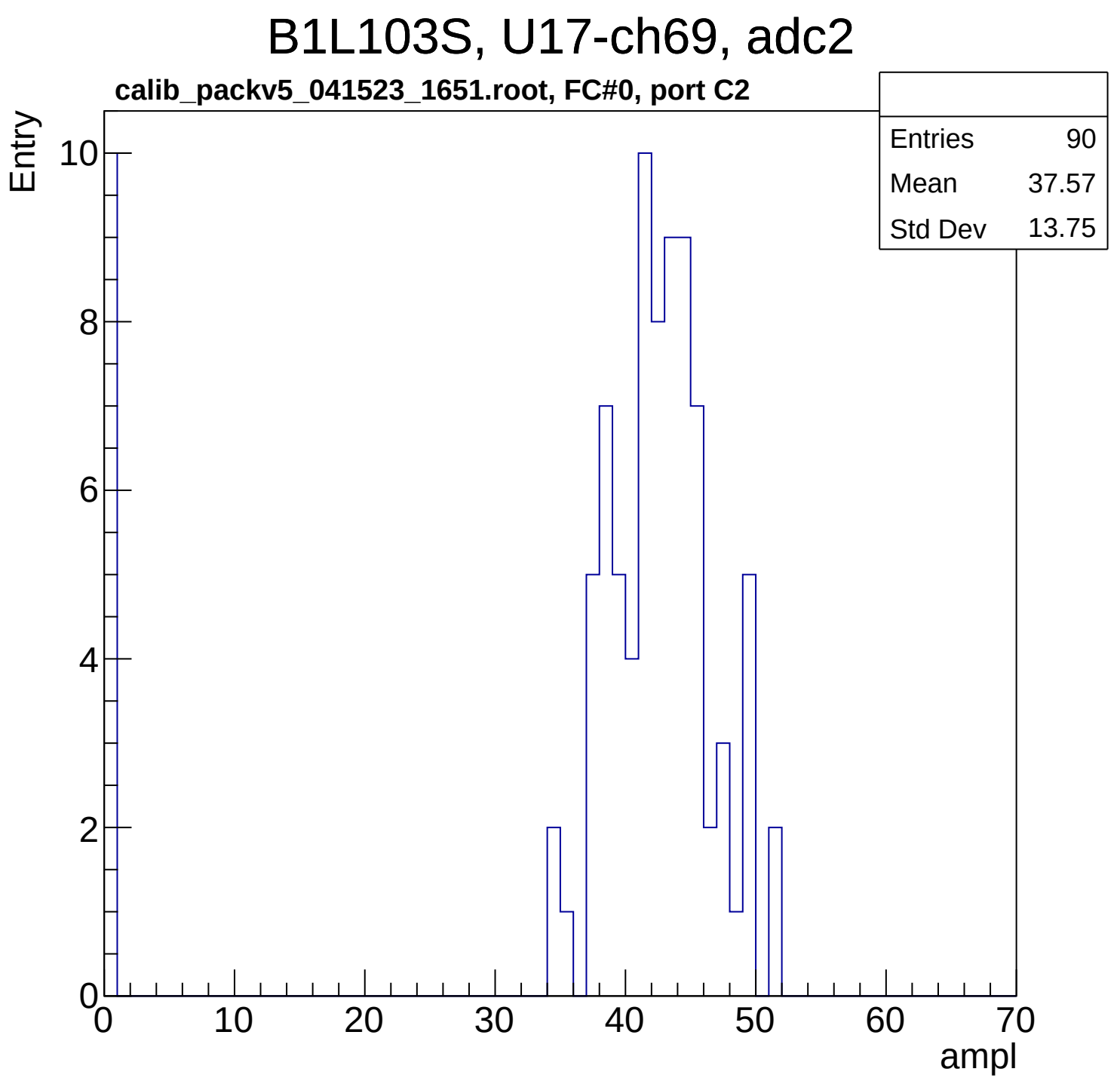
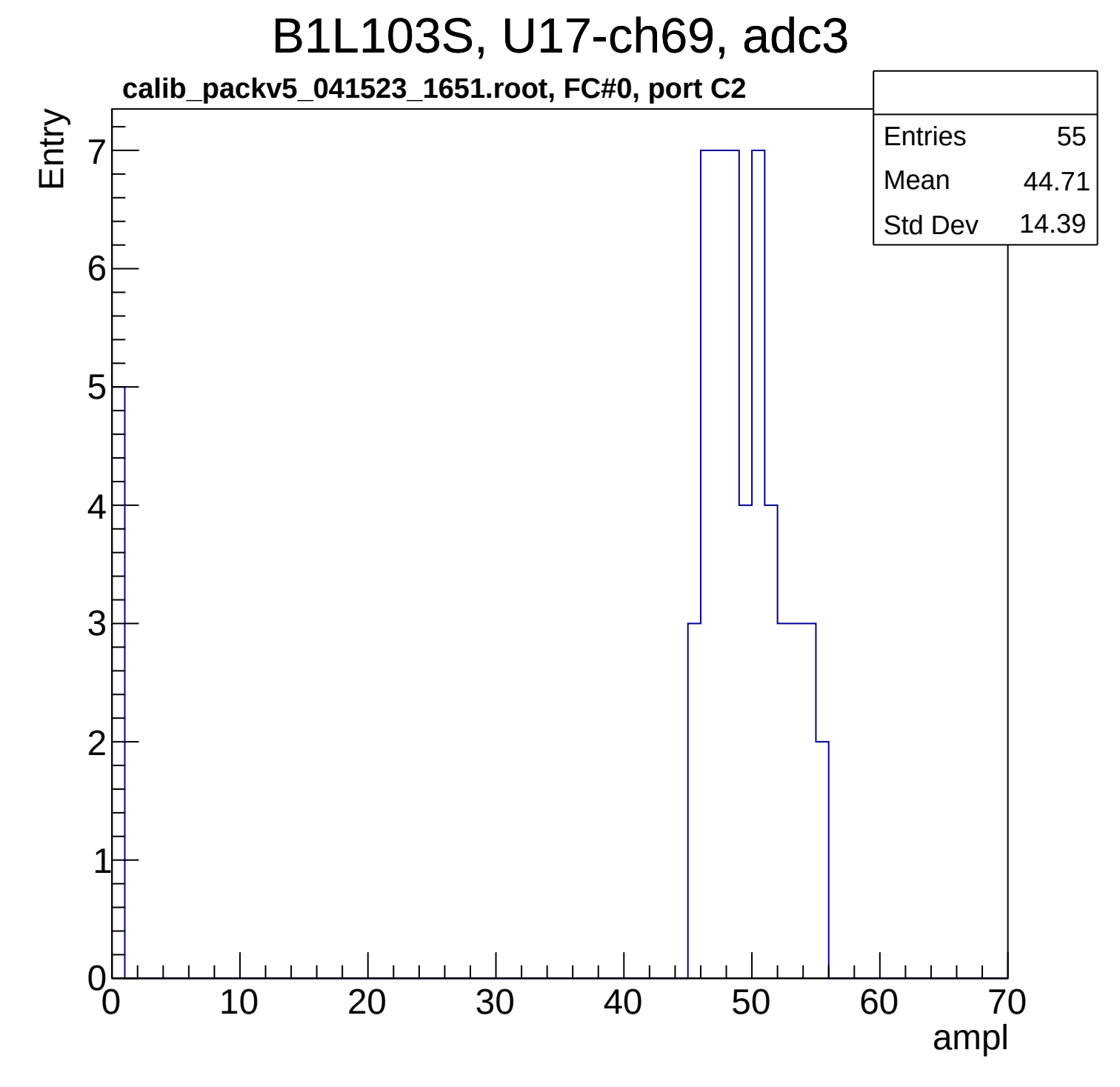
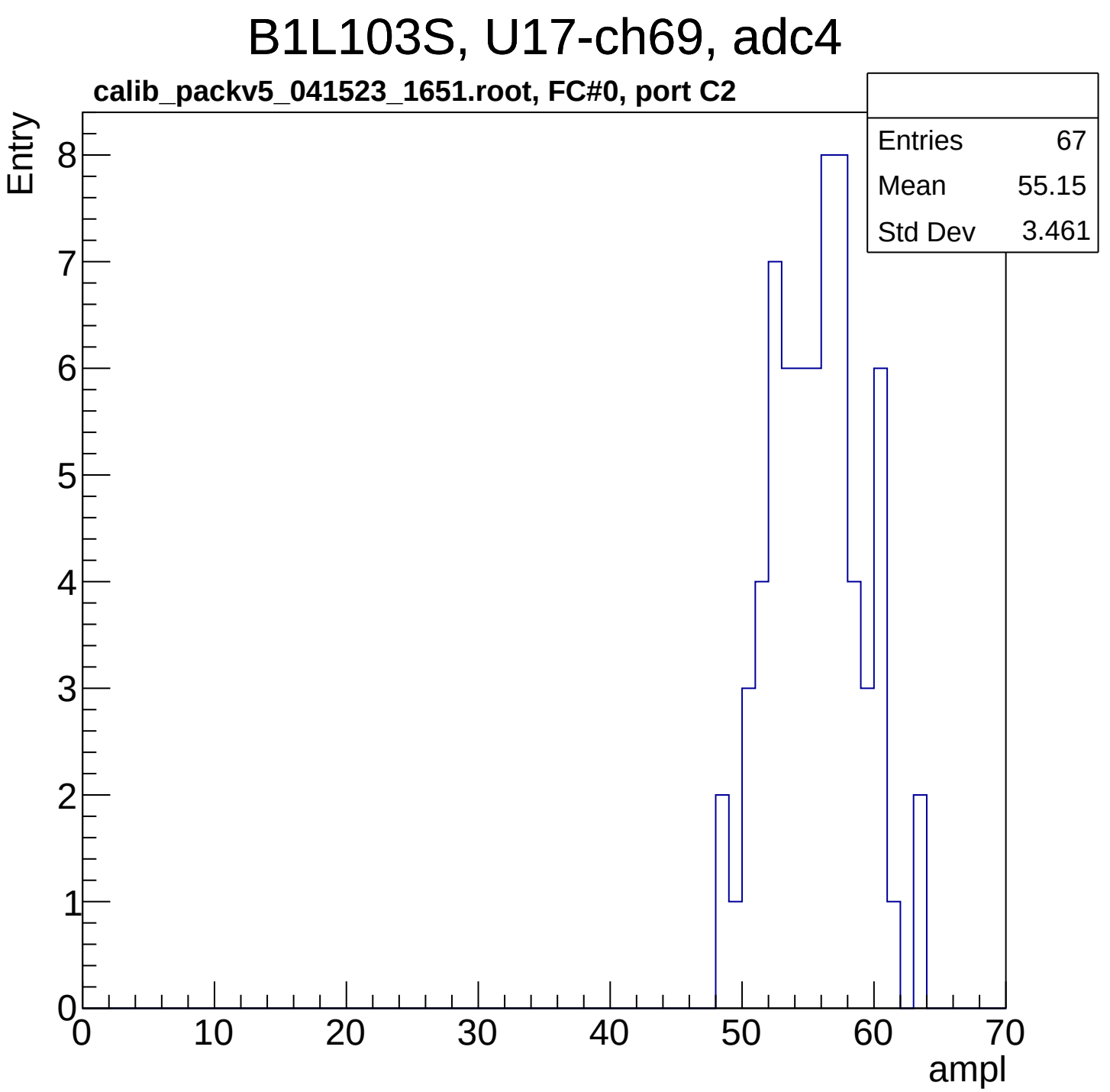
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U17-ch69, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 90
Mean 37.57
Std Dev 13.75
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U17-ch69, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 44.71
Std Dev 14.39
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U17-ch69, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 55.15
Std Dev 3.461
Entry
ampl
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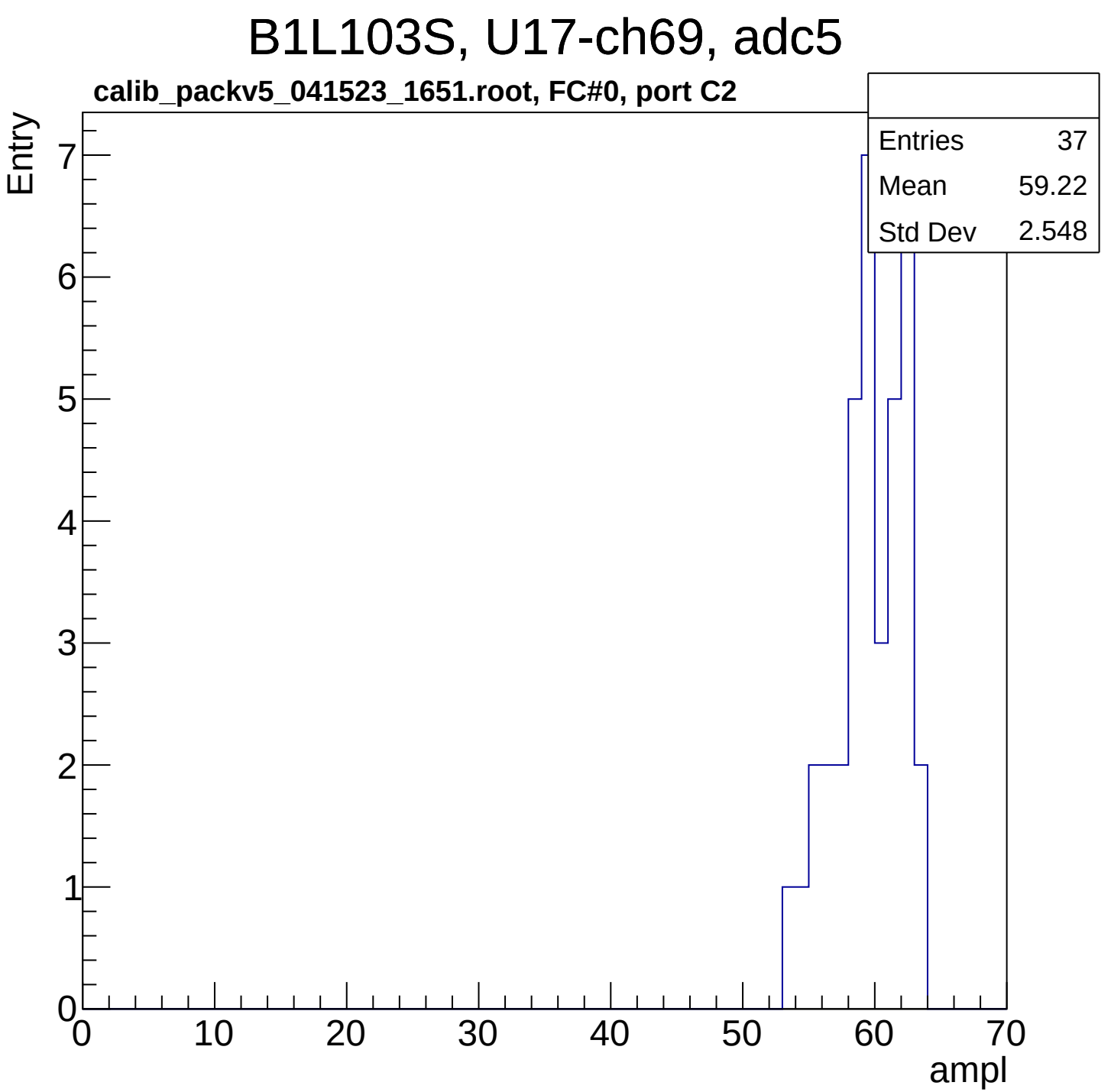
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U17-ch69, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 37
Mean 59.22
Std Dev 2.548
Entry
ampl
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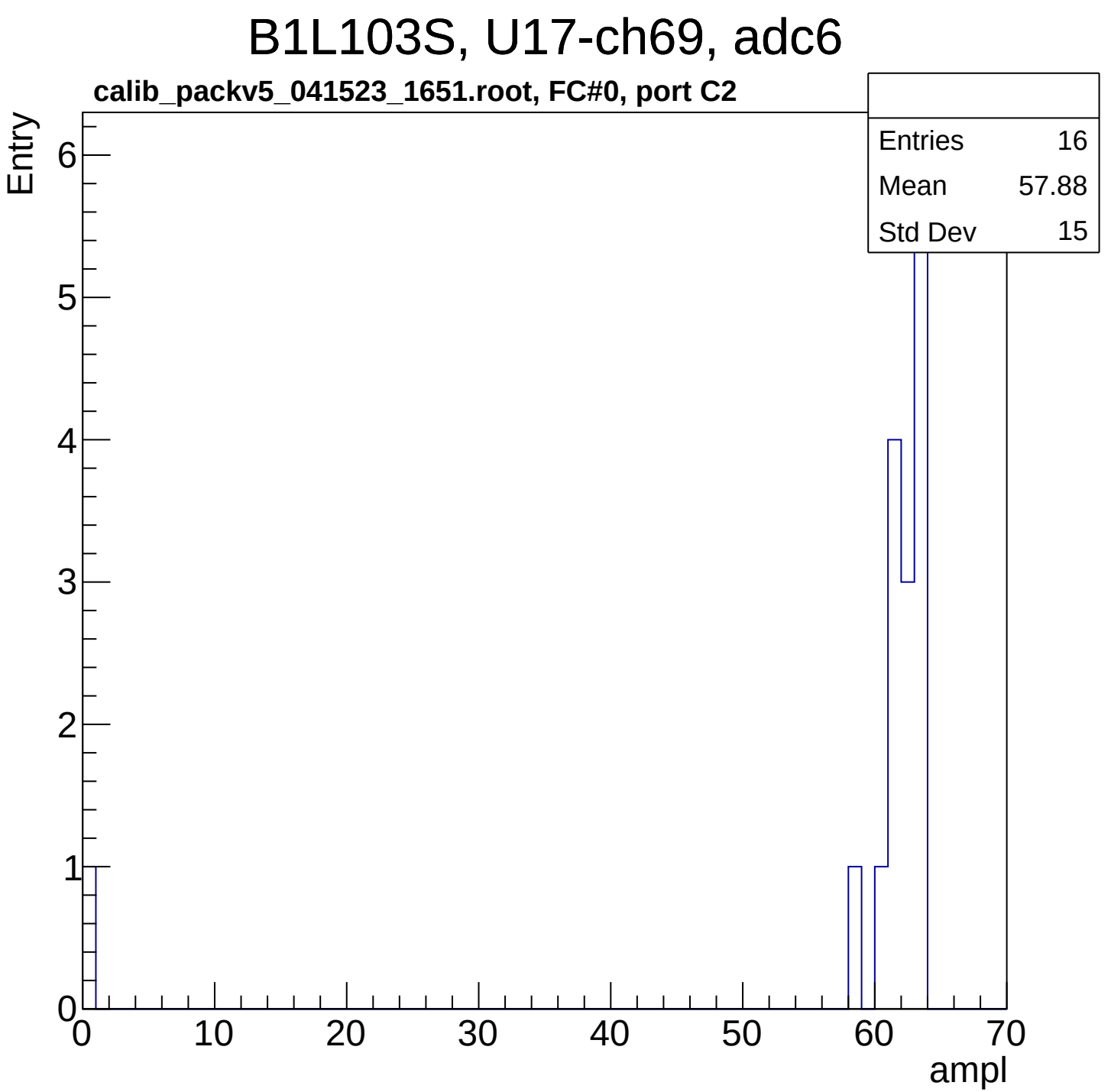
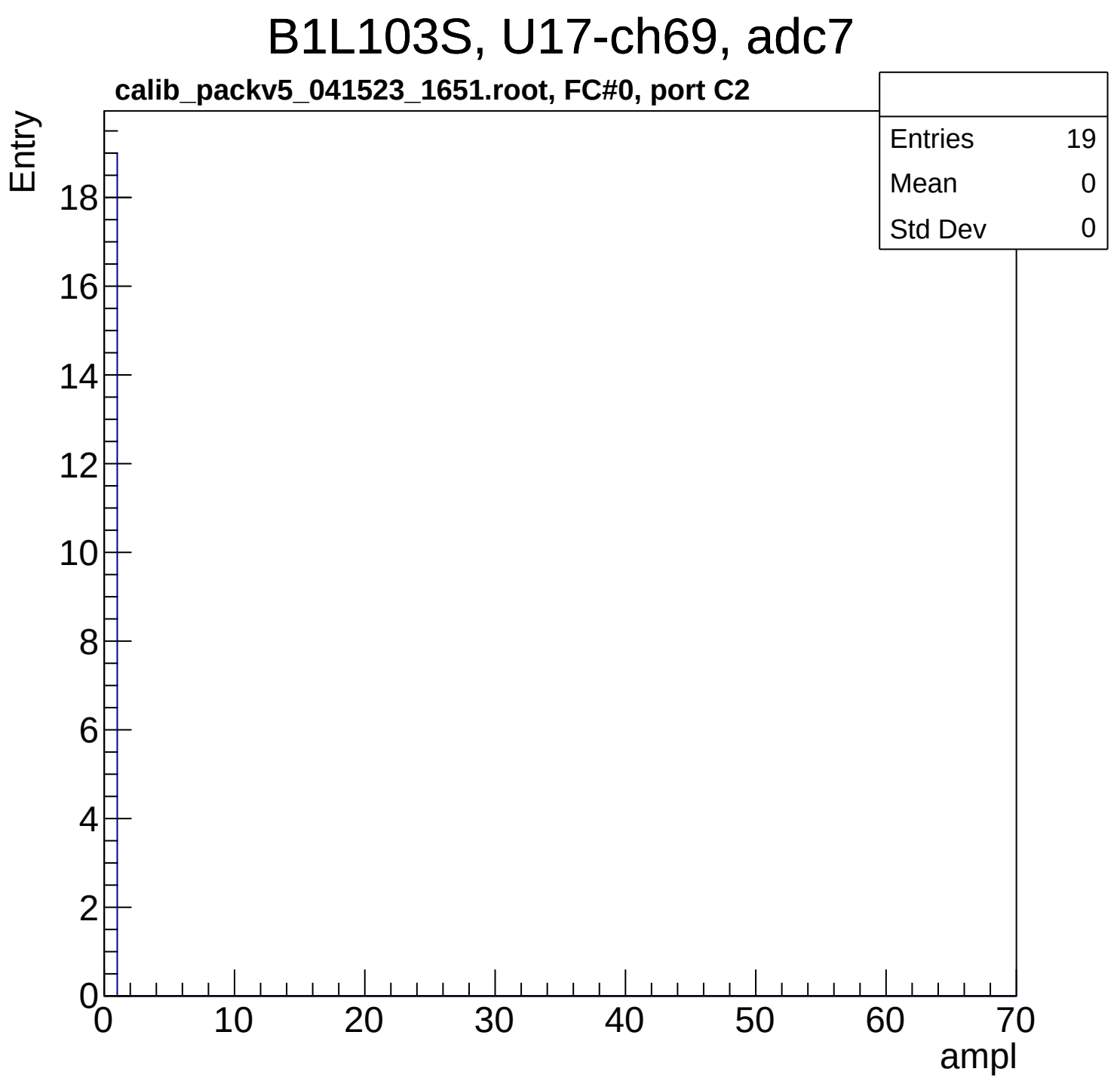
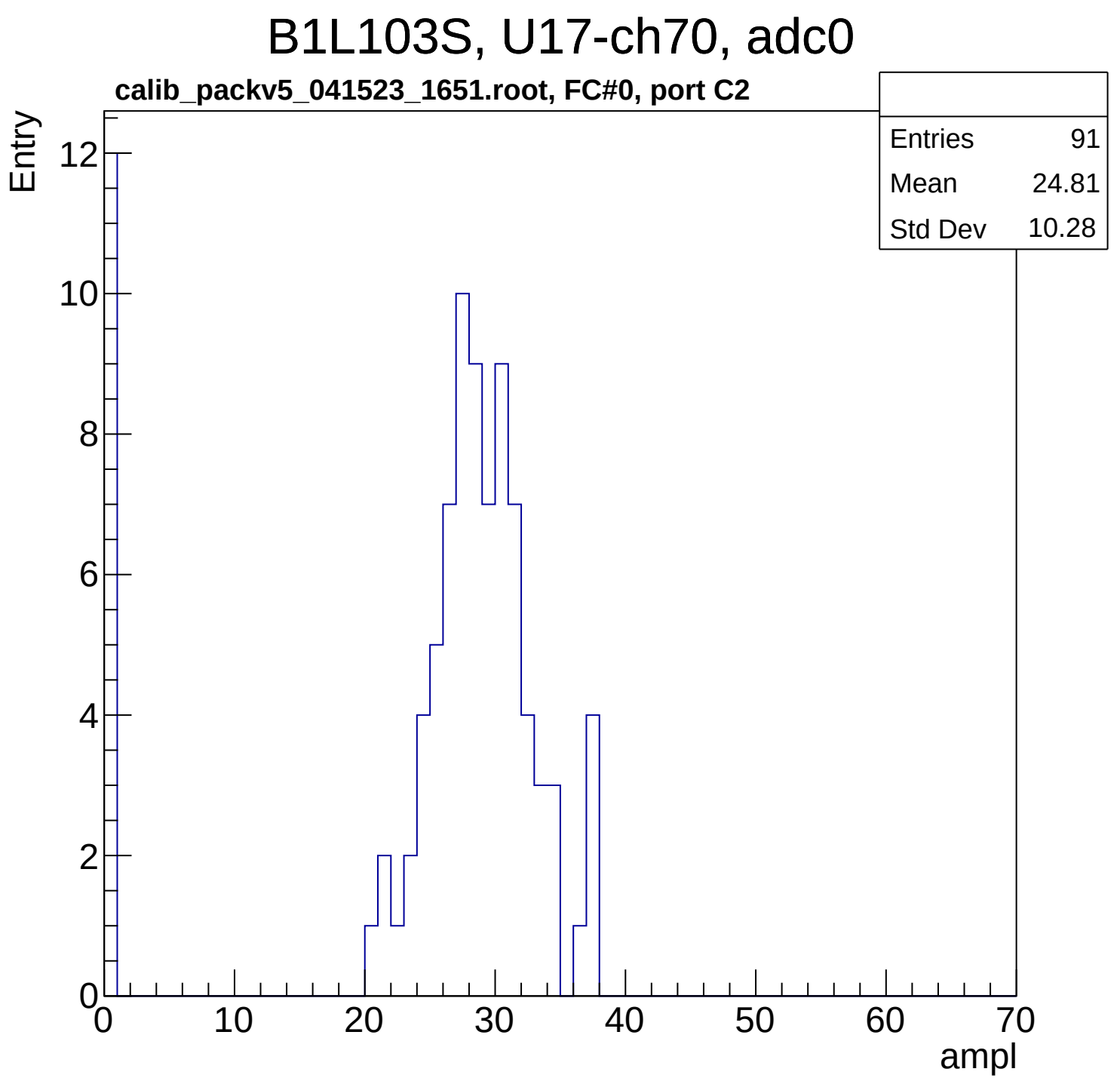
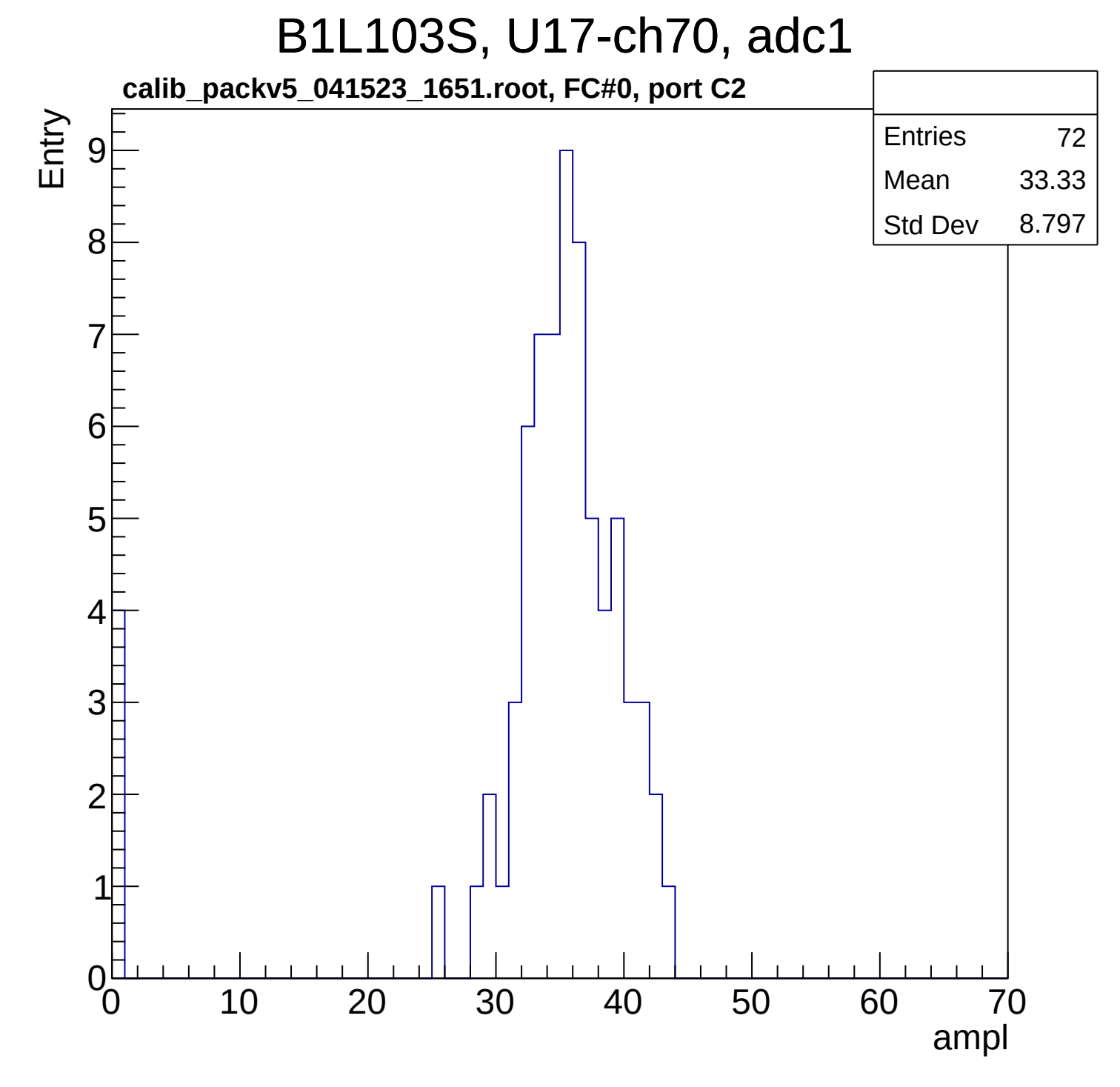
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U17-ch69, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 16
Mean 57.88
Std Dev 15
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U17-ch69, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch70, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 91
Mean 24.81
Std Dev 10.28
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch70, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 33.33
Std Dev 8.797
Entry
ampl
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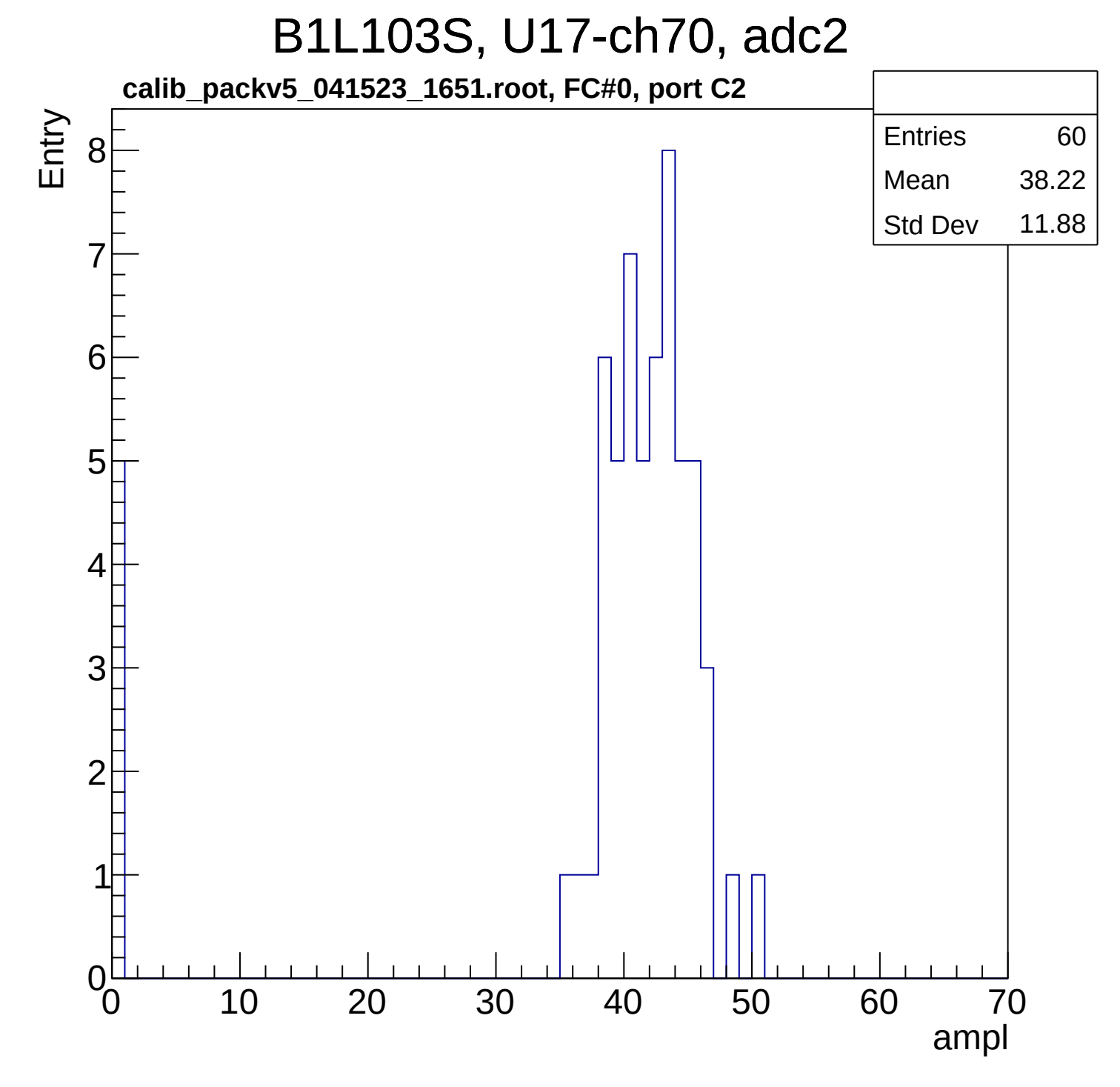
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U17-ch70, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 38.22
Std Dev 11.88
Entry
ampl
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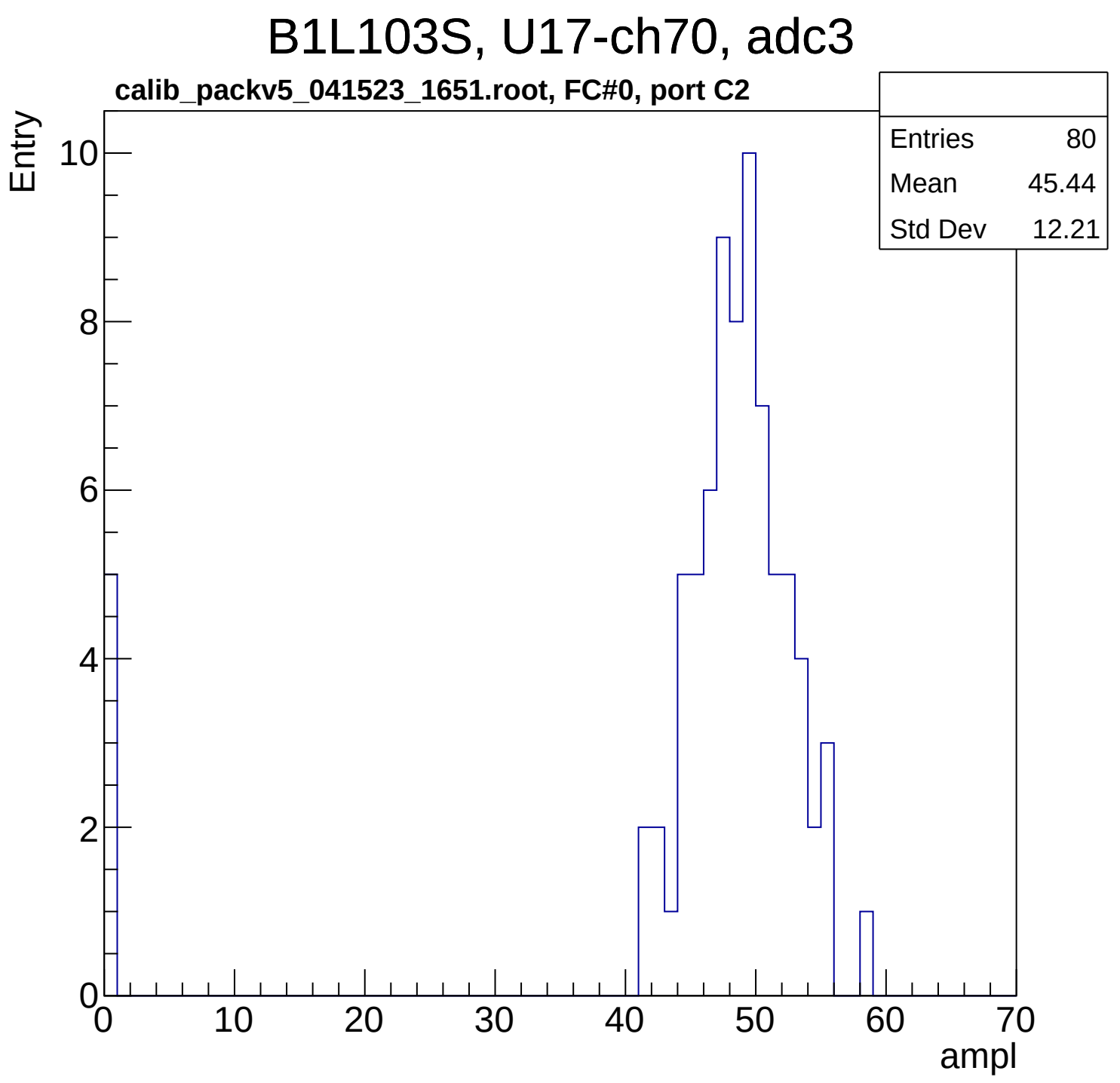
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U17-ch70, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 45.44
Std Dev 12.21
Entry
ampl
0
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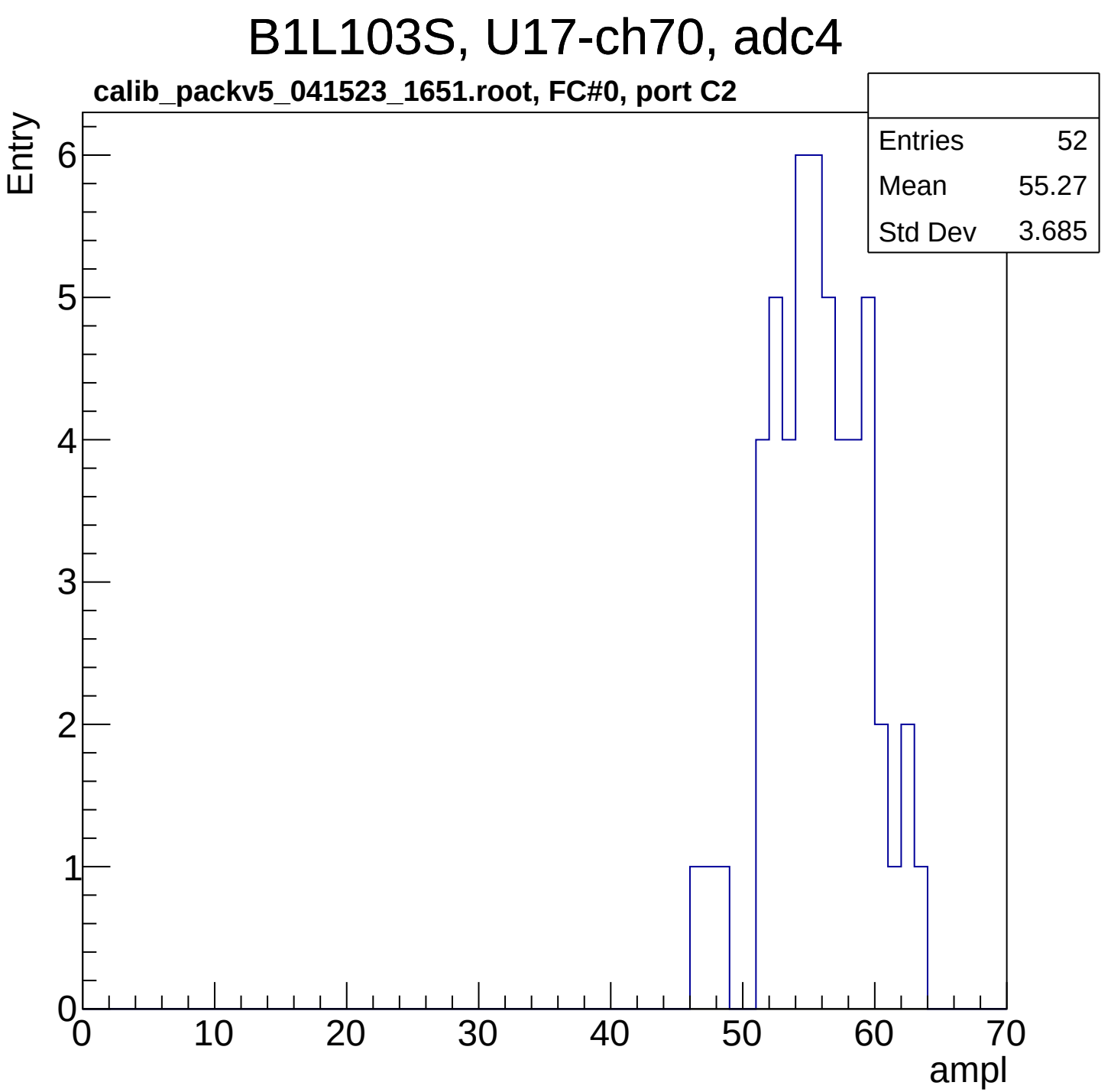
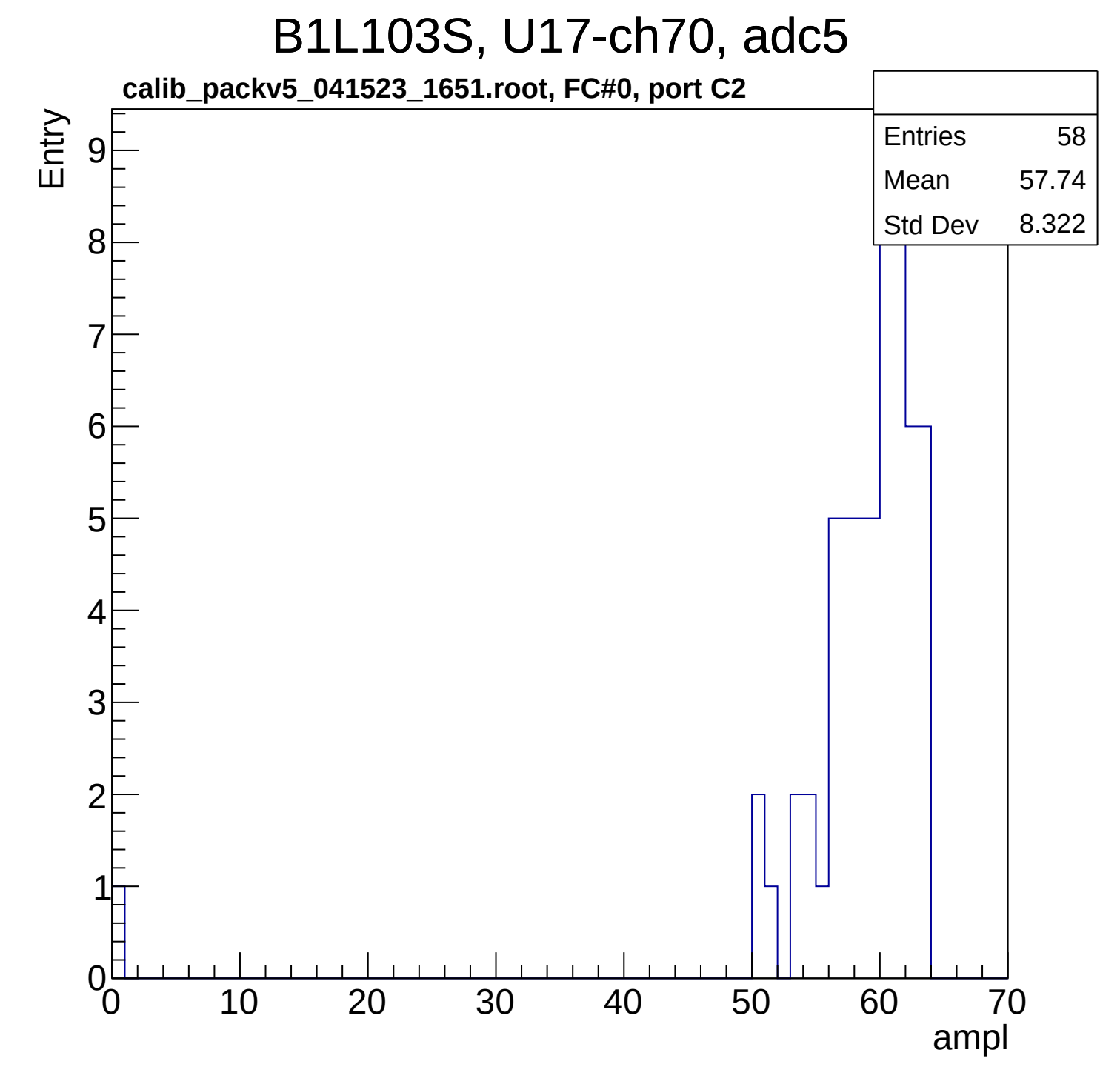
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U17-ch70, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 55.27
Std Dev 3.685
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch70, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 57.74
Std Dev 8.322
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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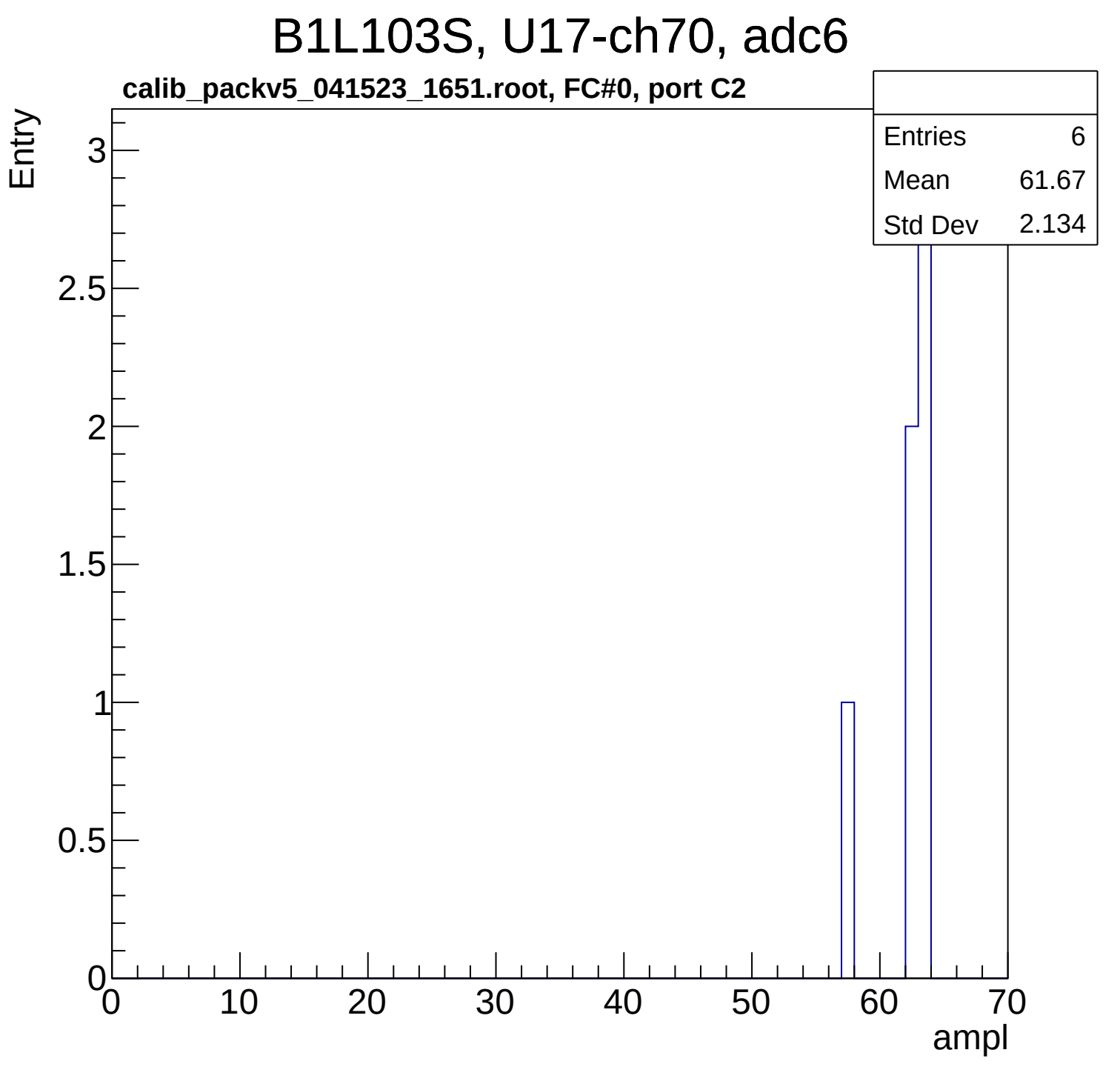
60
70


B1L103S, U17-ch70, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 61.67
Std Dev 2.134
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
10
20
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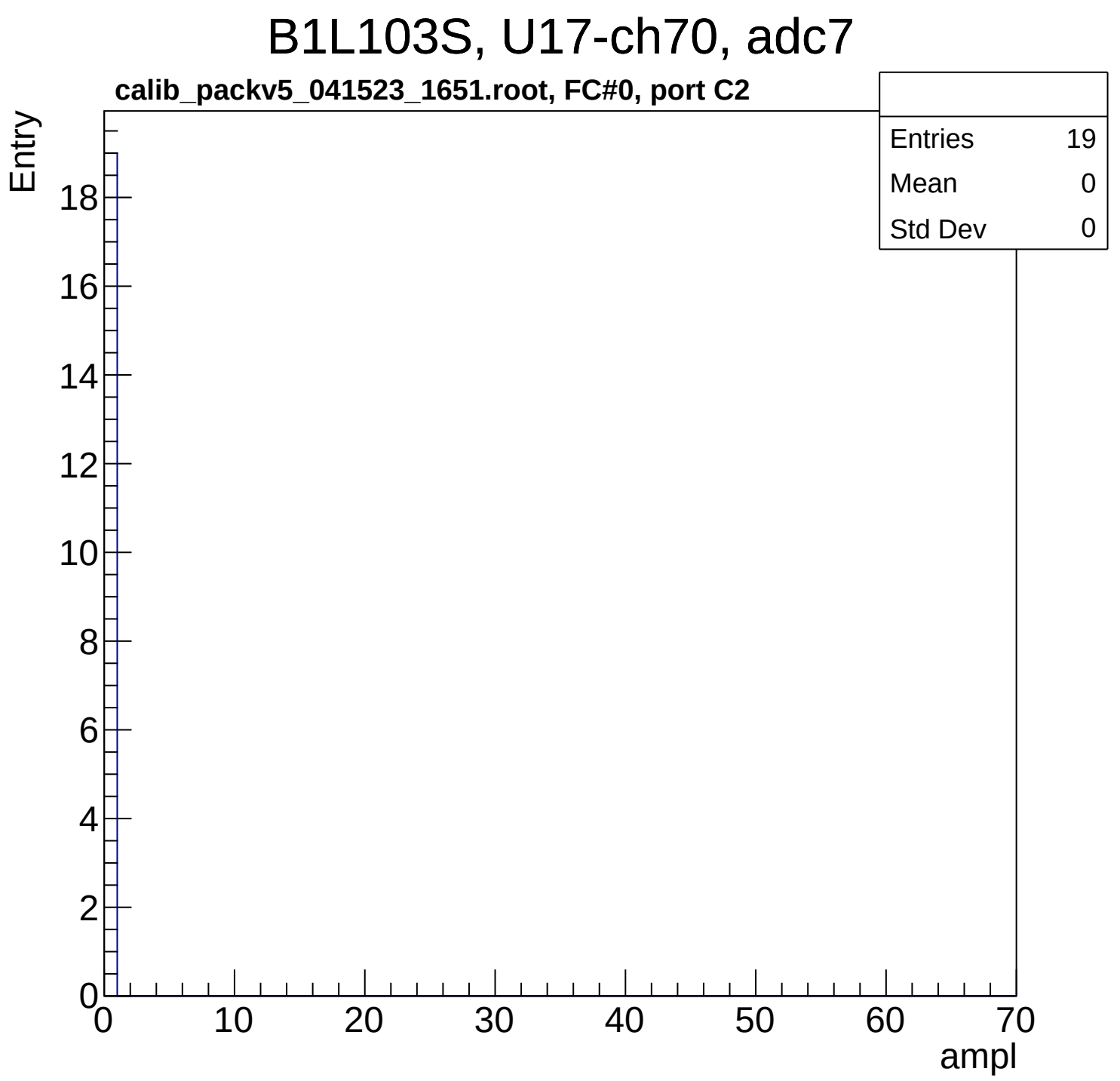
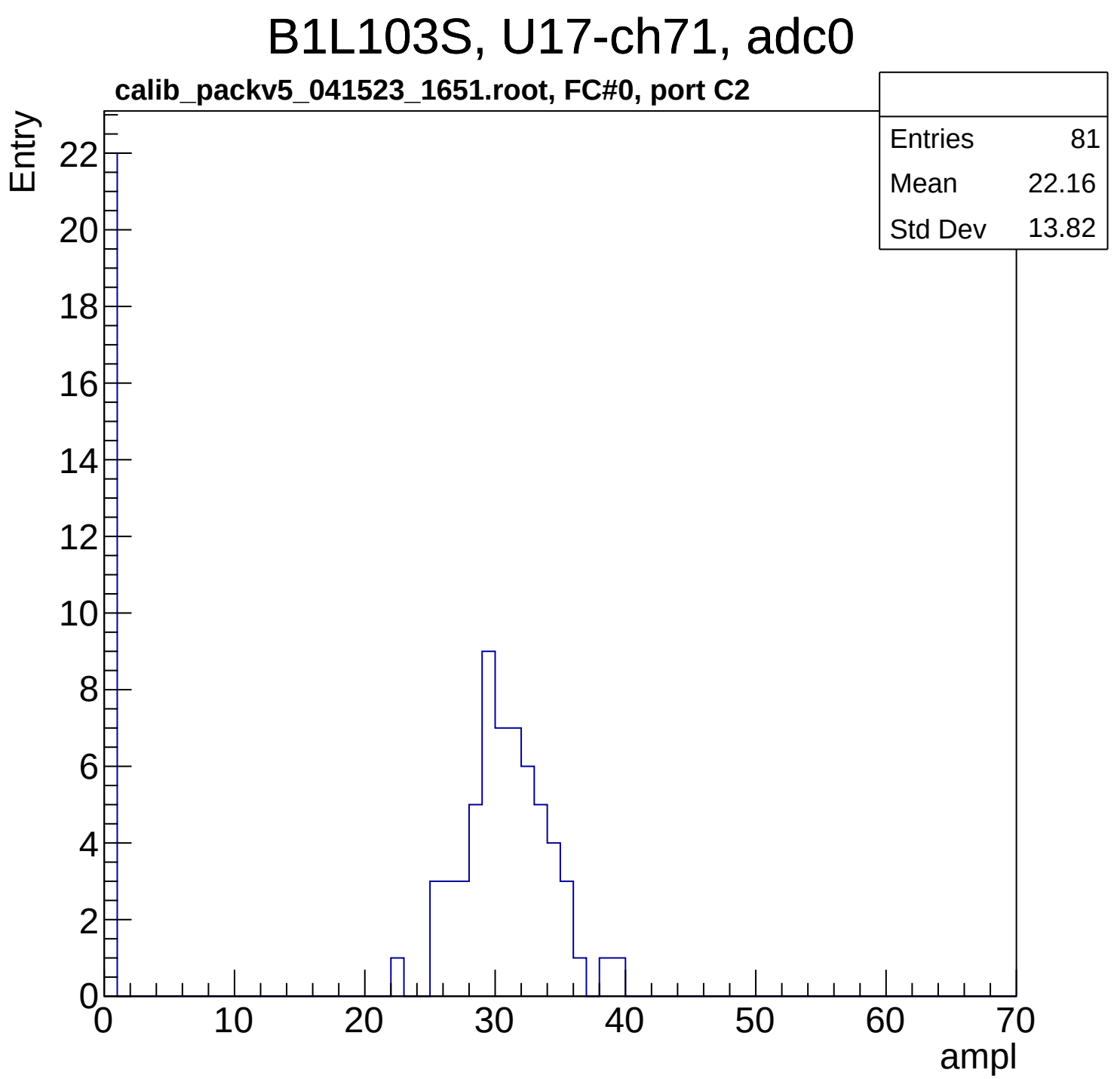
40
50
60
70


B1L103S, U17-ch70, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch71, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 22.16
Std Dev 13.82
Entry
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10
12
14
16
18
20
22
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10
20
30
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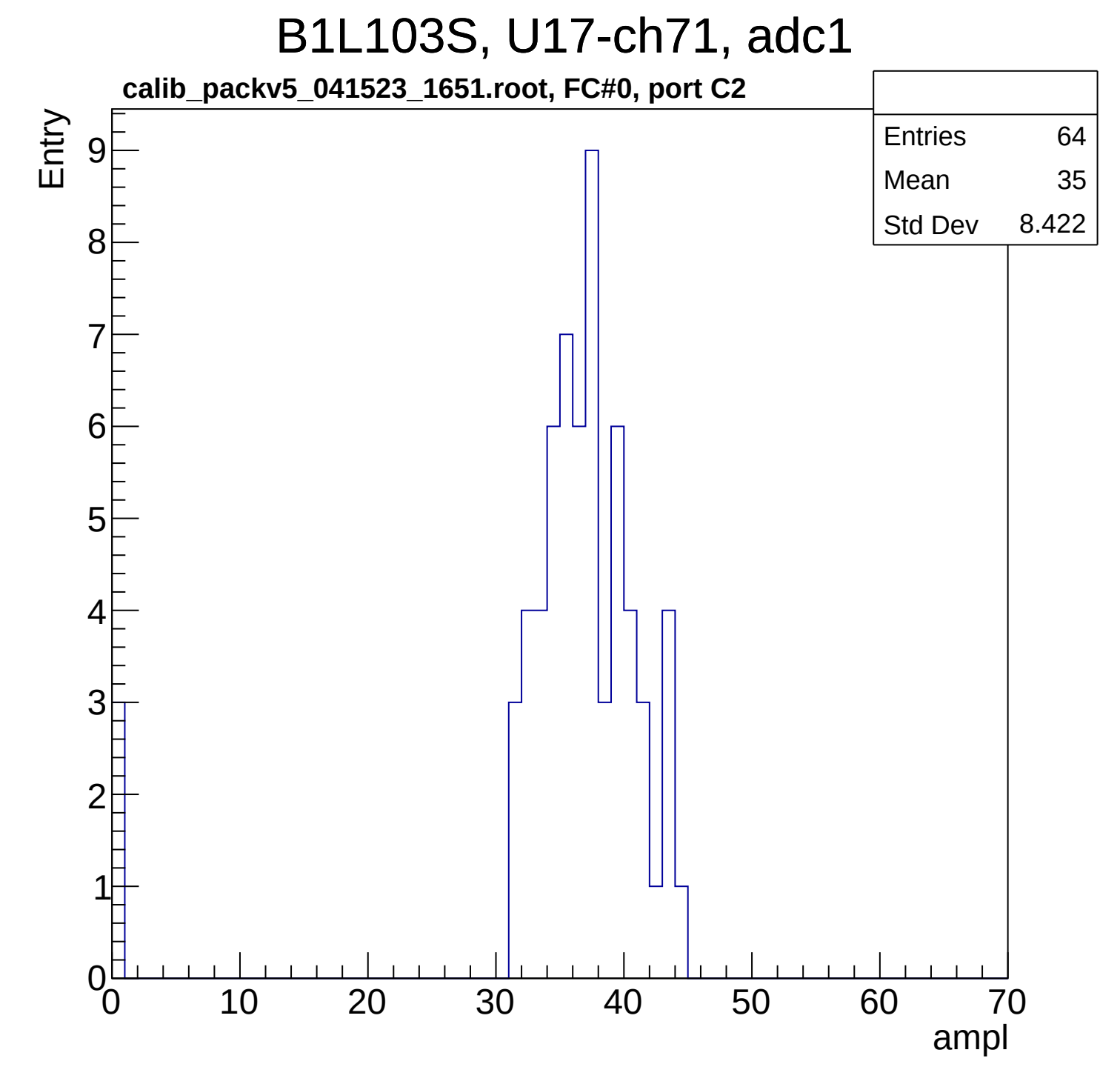
50
60
70
ampl


B1L103S, U17-ch71, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 35
Std Dev 8.422
Entry
ampl
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3
4
5
6
7
8
9
0
10
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40
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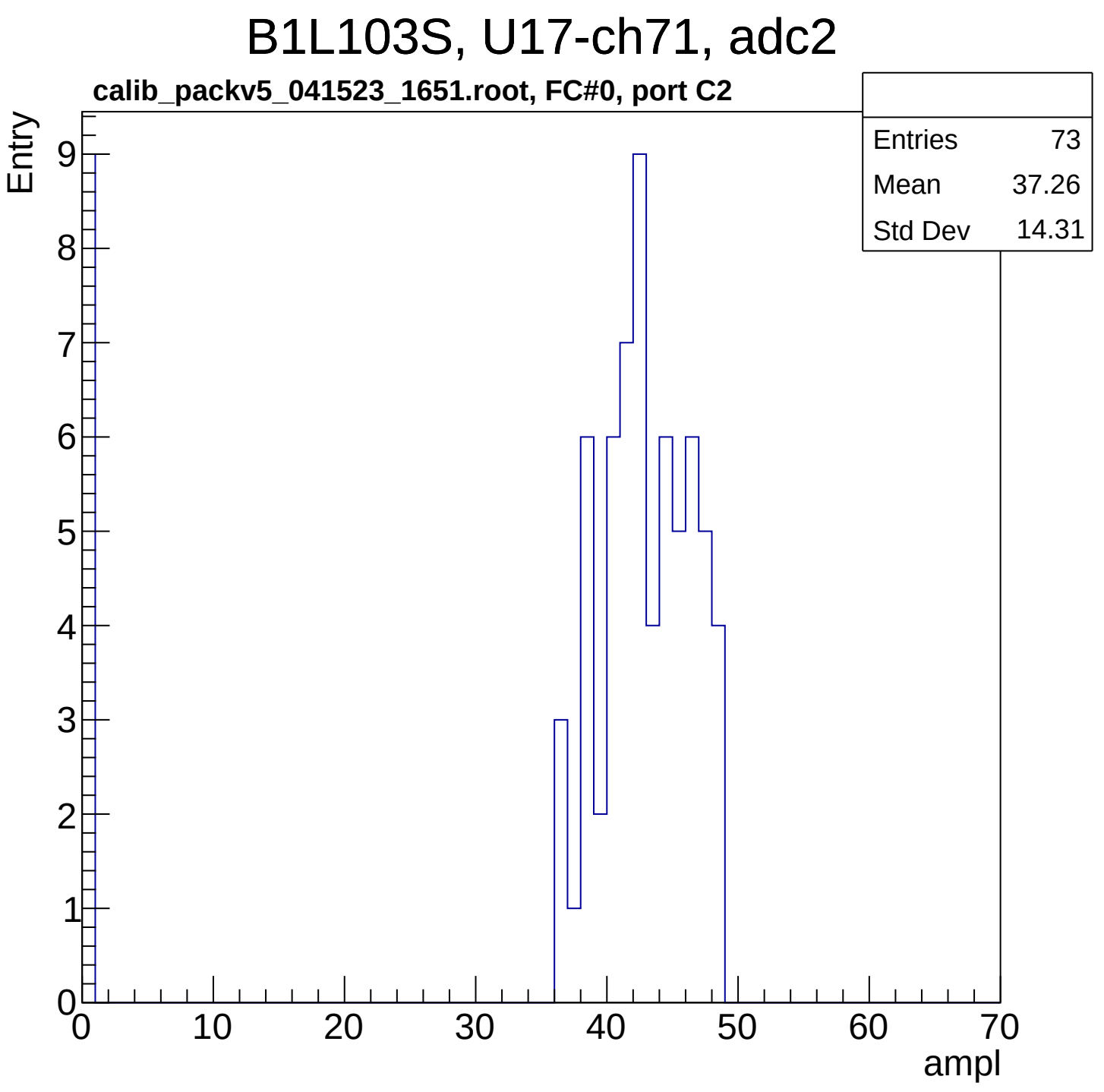
B1L103S, U17-ch71, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 37.26
Std Dev 14.31
Entry
ampl
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3
4
5
6
7
8
9
0
10
20
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40
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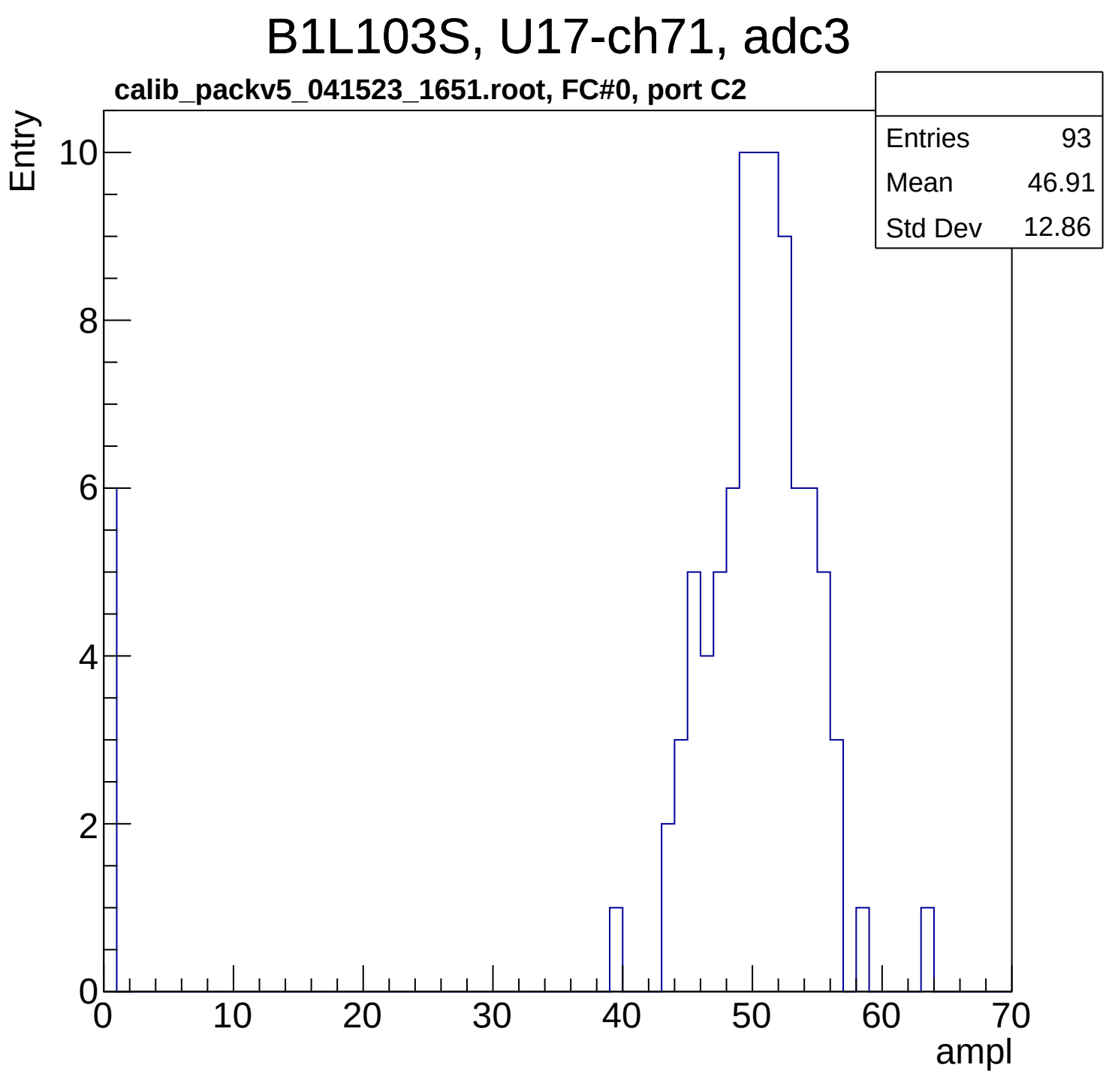
B1L103S, U17-ch71, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 93
Mean 46.91
Std Dev 12.86
Entry
ampl
0
2
4
6
8
10
0
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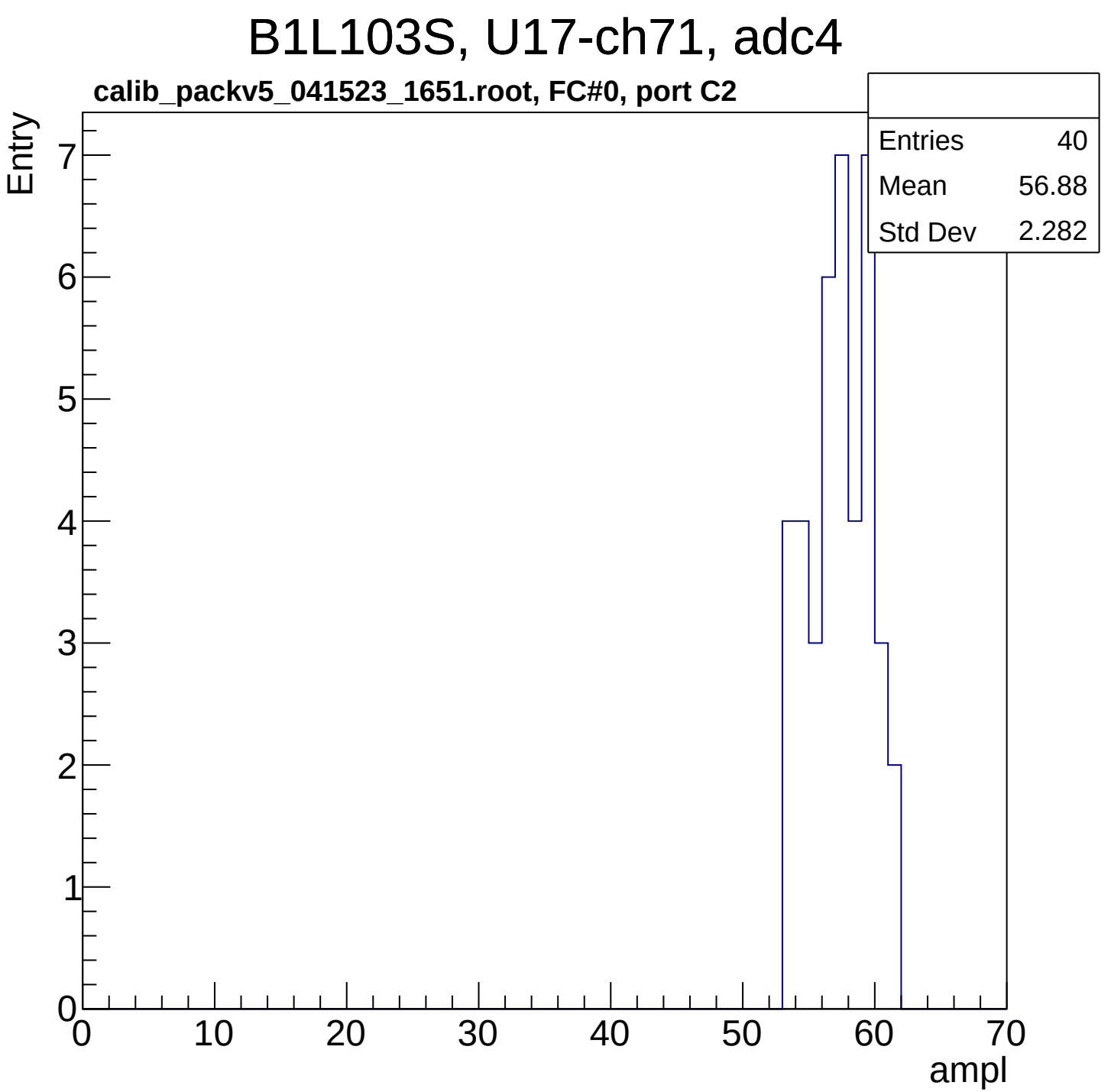
20
30
40
50
60
70


B1L103S, U17-ch71, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 40
Mean 56.88
Std Dev 2.282
Entry
ampl
0
1
2
3
4
5
6
7
0
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20
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40
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60
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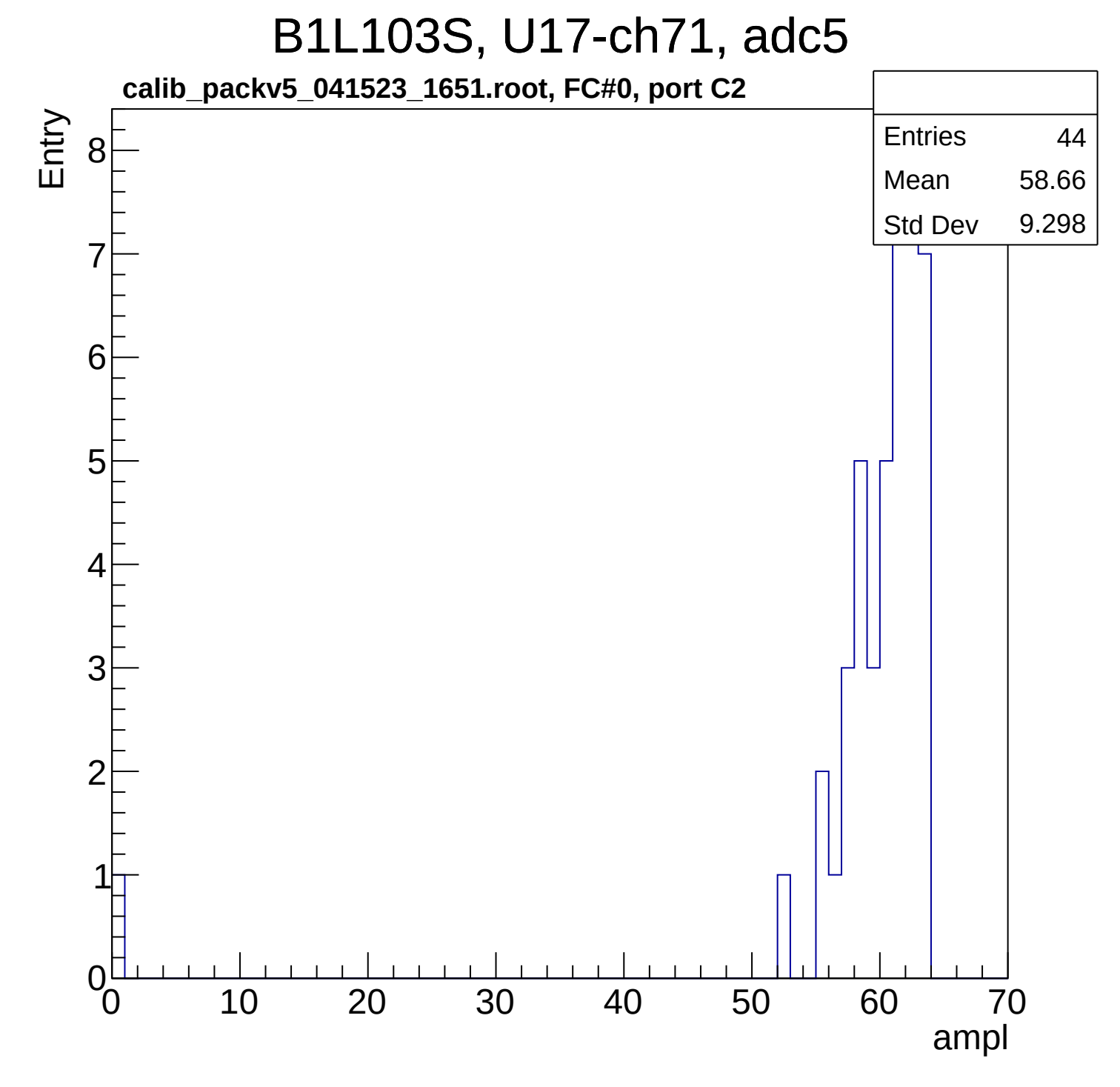
B1L103S, U17-ch71, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 58.66
Std Dev 9.298
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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40
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60
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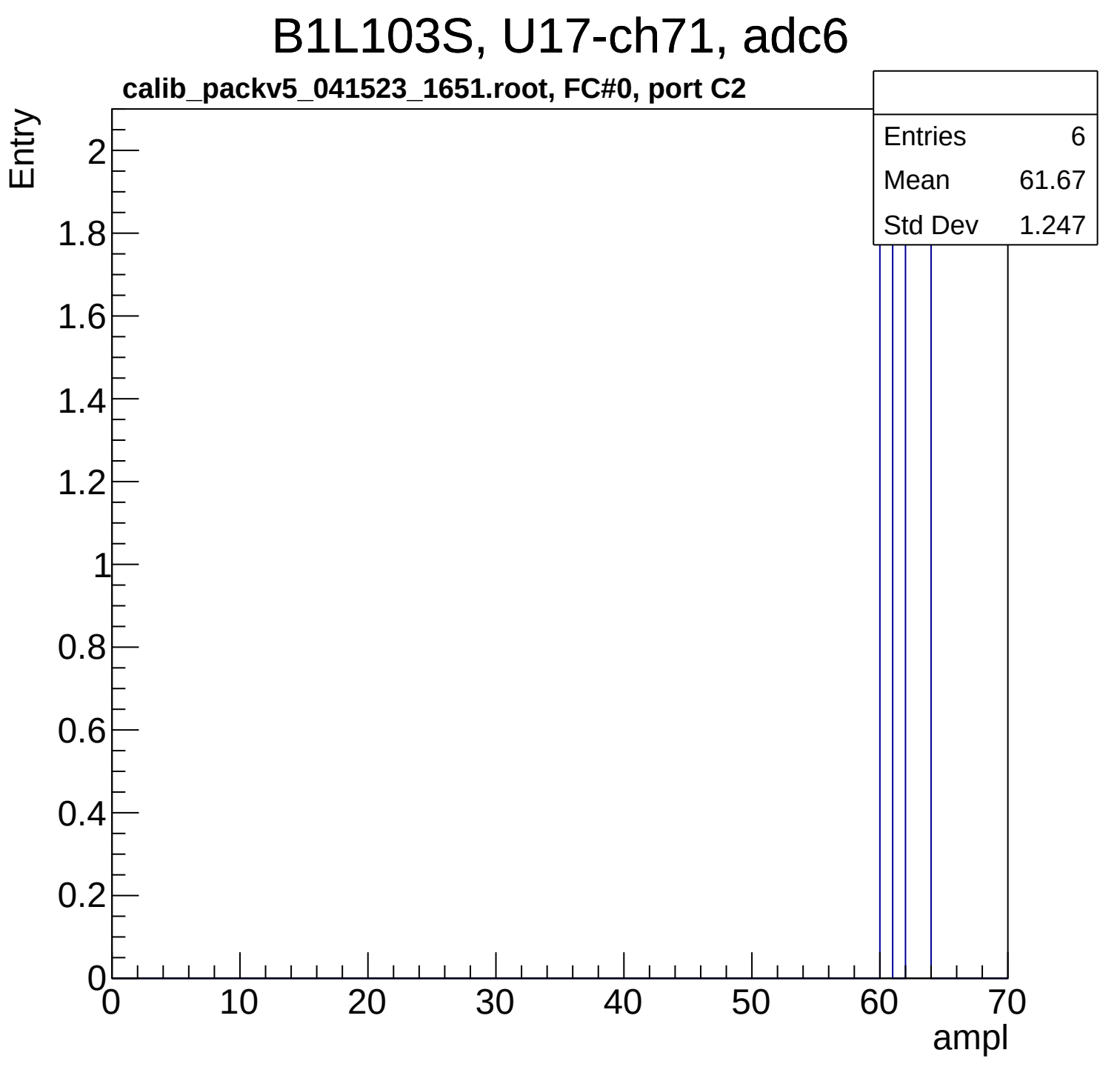
B1L103S, U17-ch71, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 61.67
Std Dev 1.247
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
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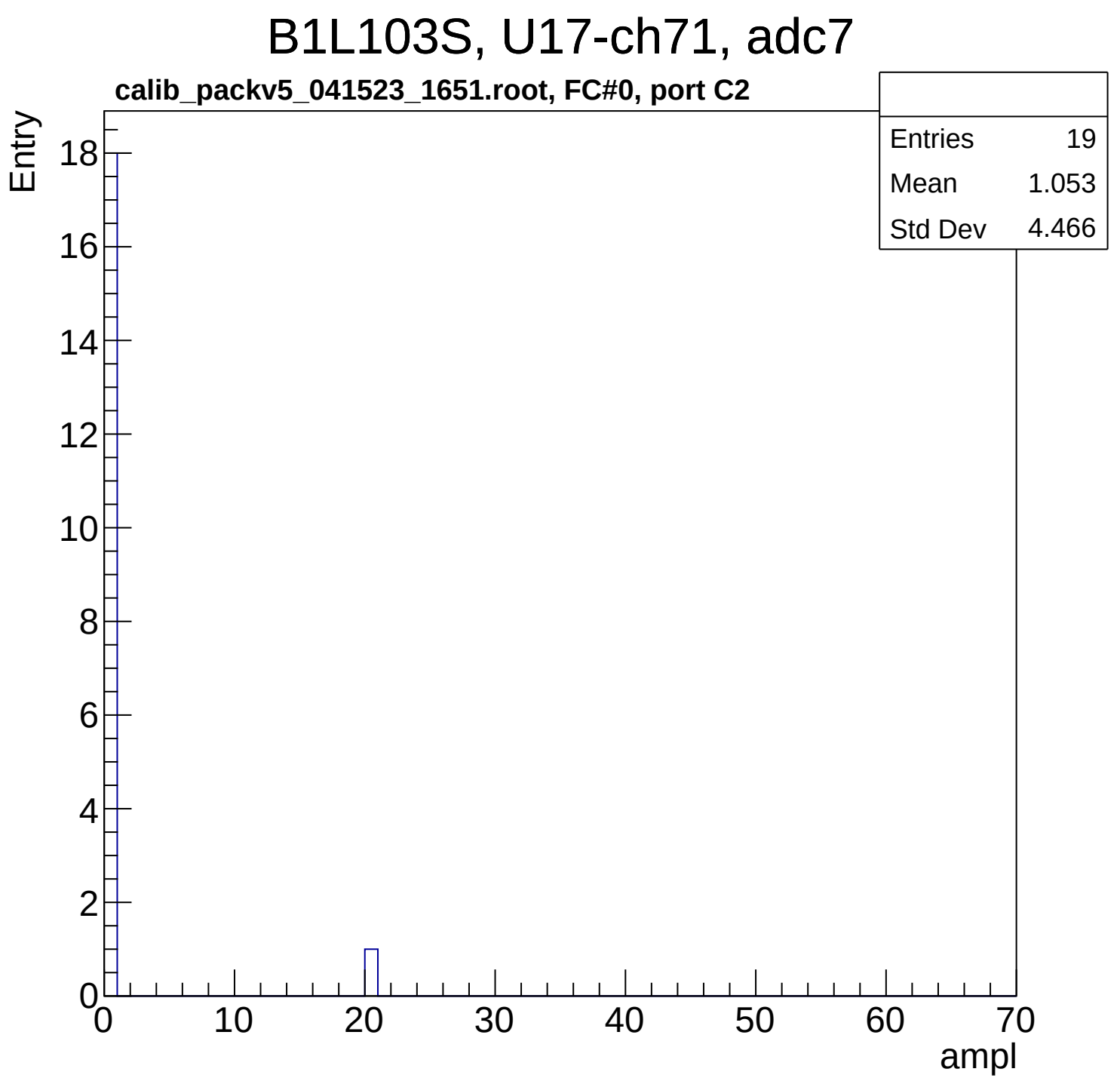
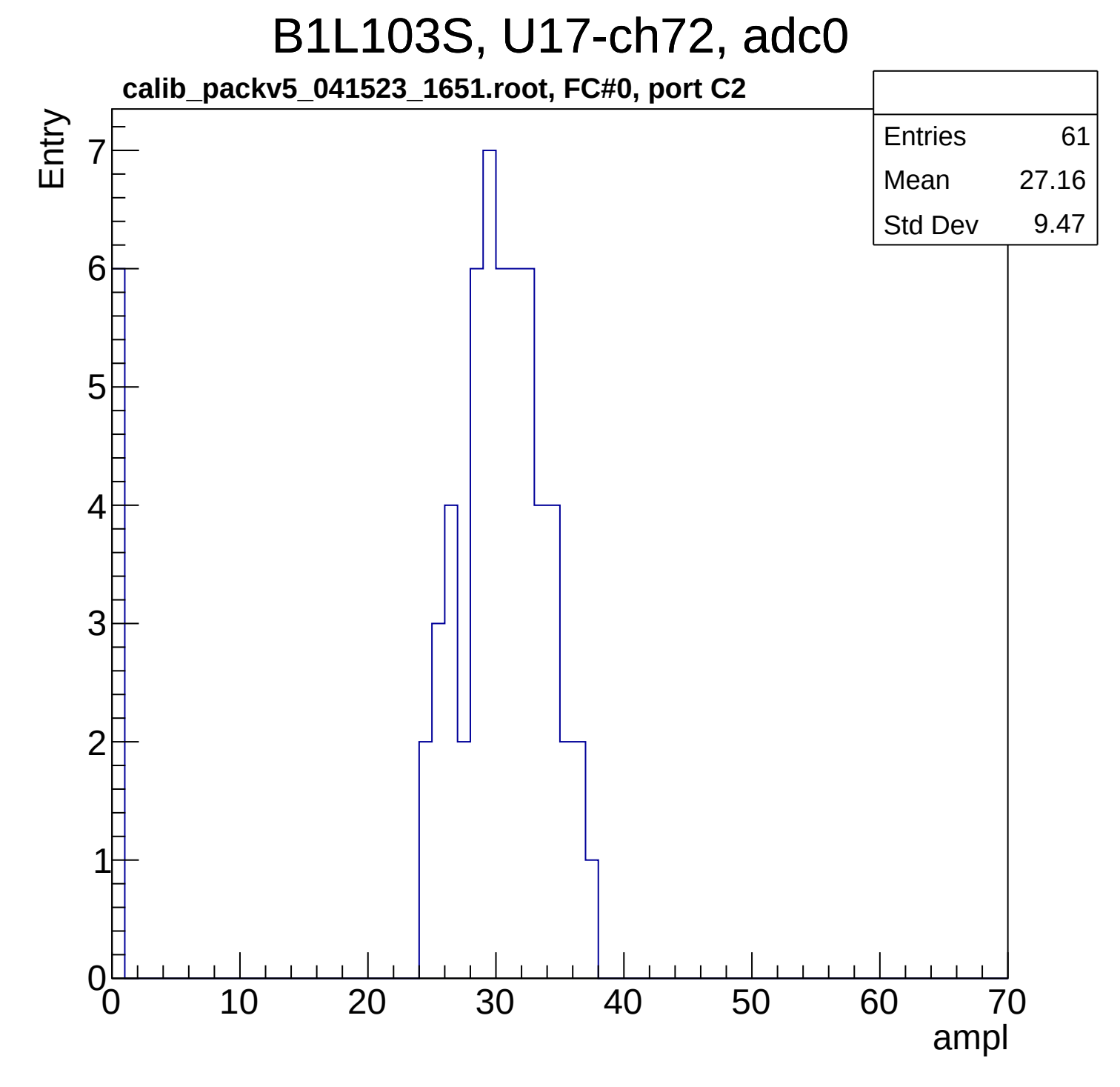

B1L103S, U17-ch71, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.053
Std Dev 4.466
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch72, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 27.16
Std Dev 9.47
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
30
40
50
60
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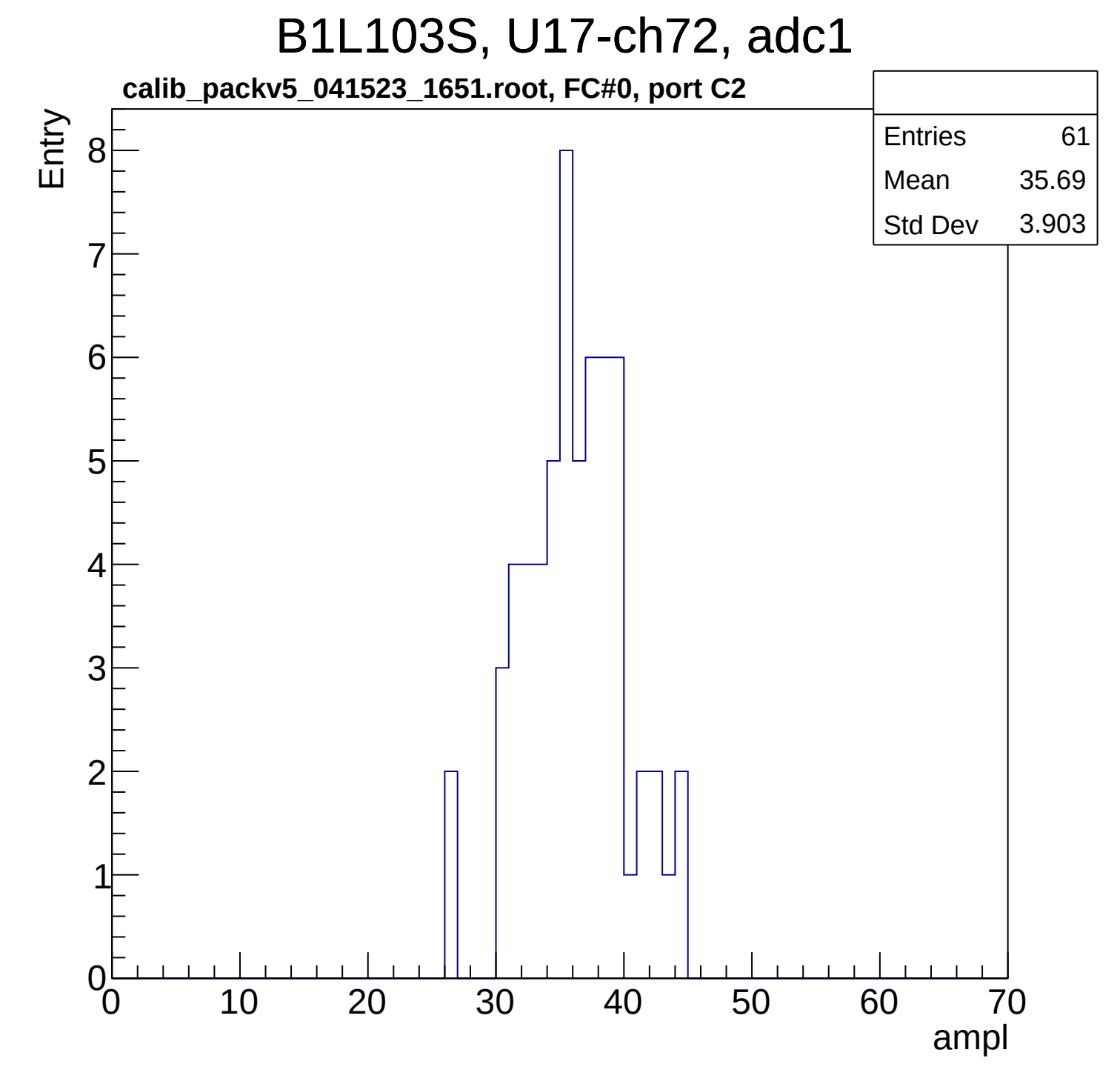
B1L103S, U17-ch72, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 35.69
Std Dev 3.903
Entry
ampl
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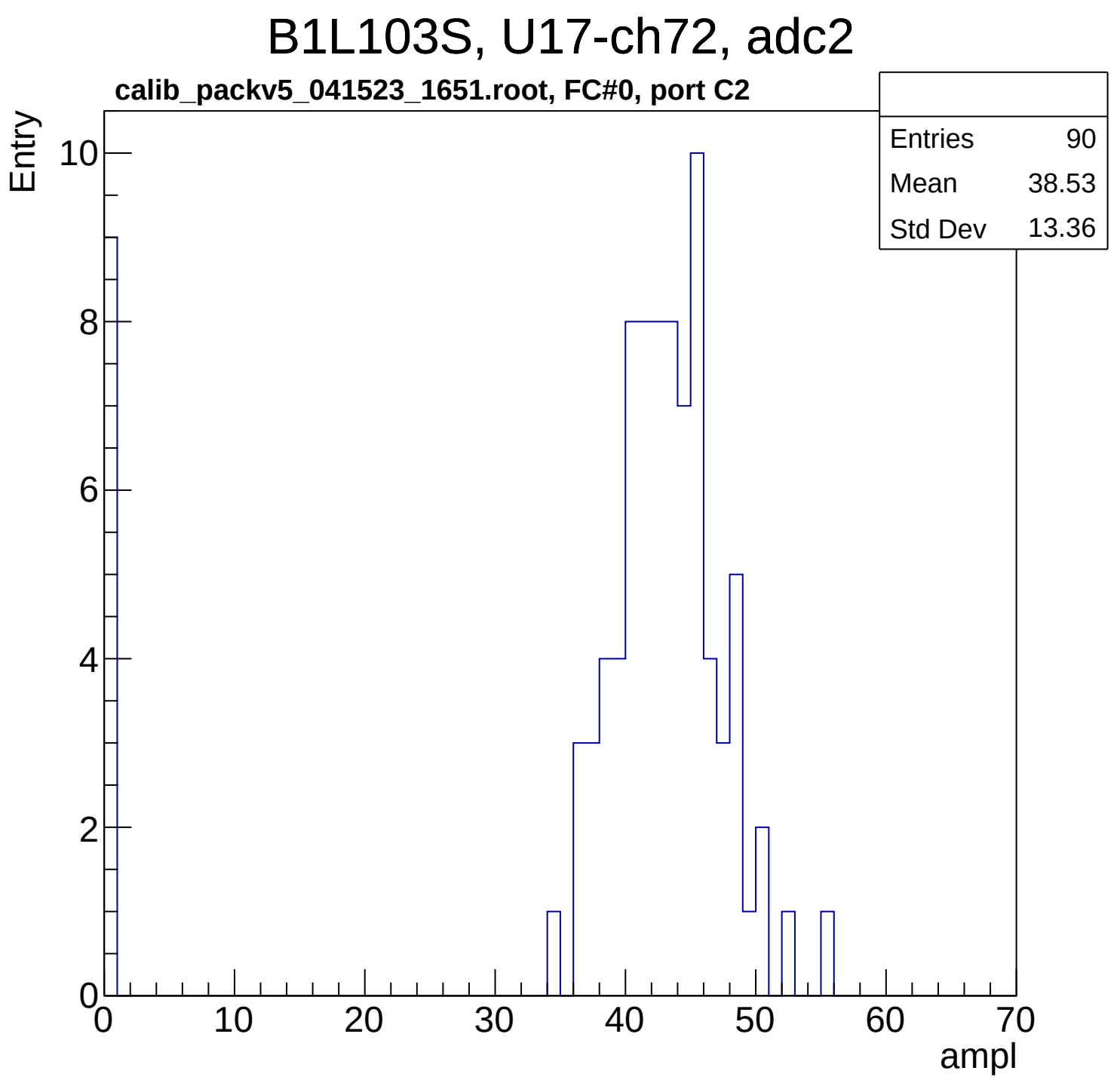
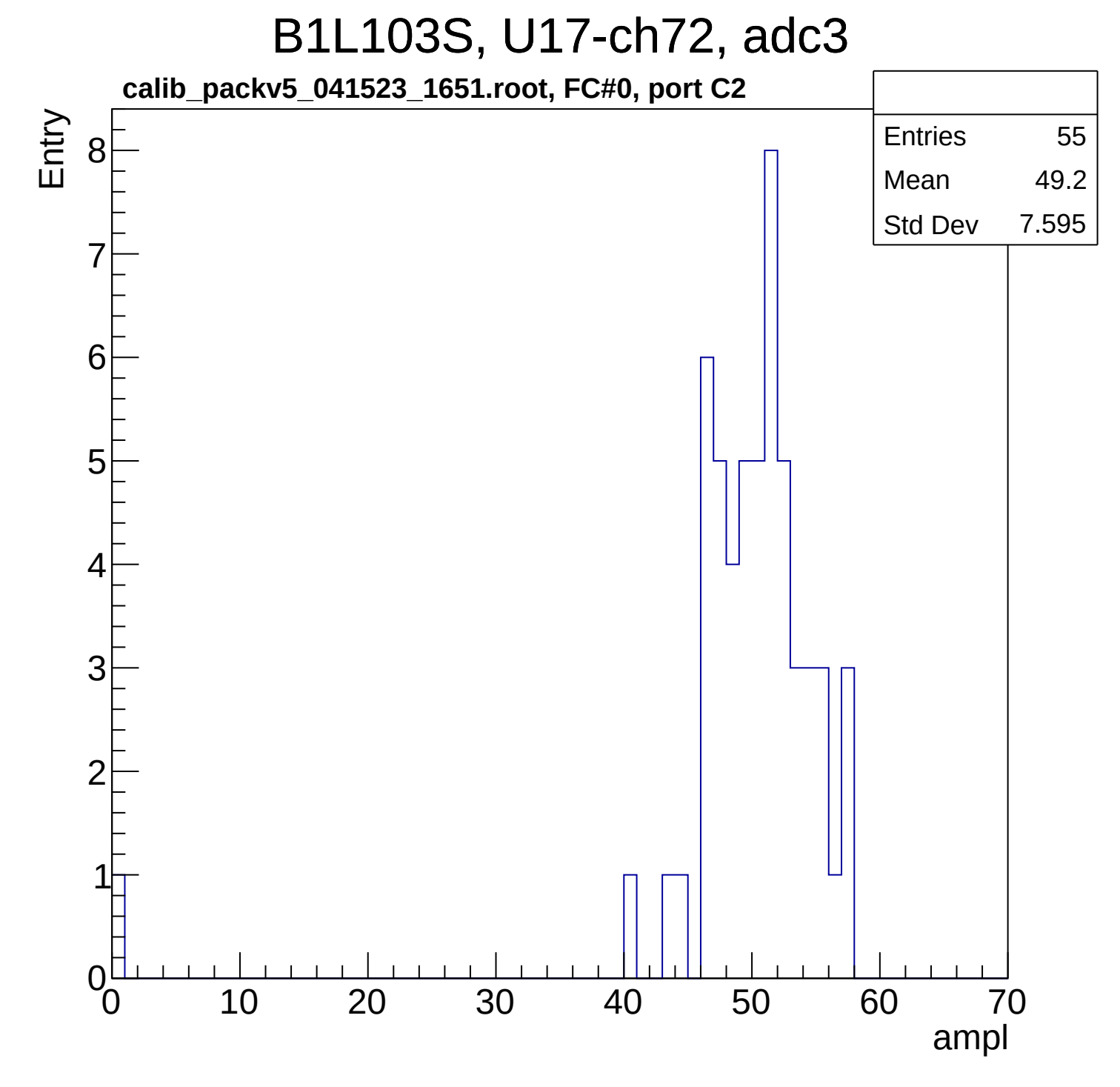
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U17-ch72, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 90
Mean 38.53
Std Dev 13.36
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch72, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 49.2
Std Dev 7.595
Entry
ampl
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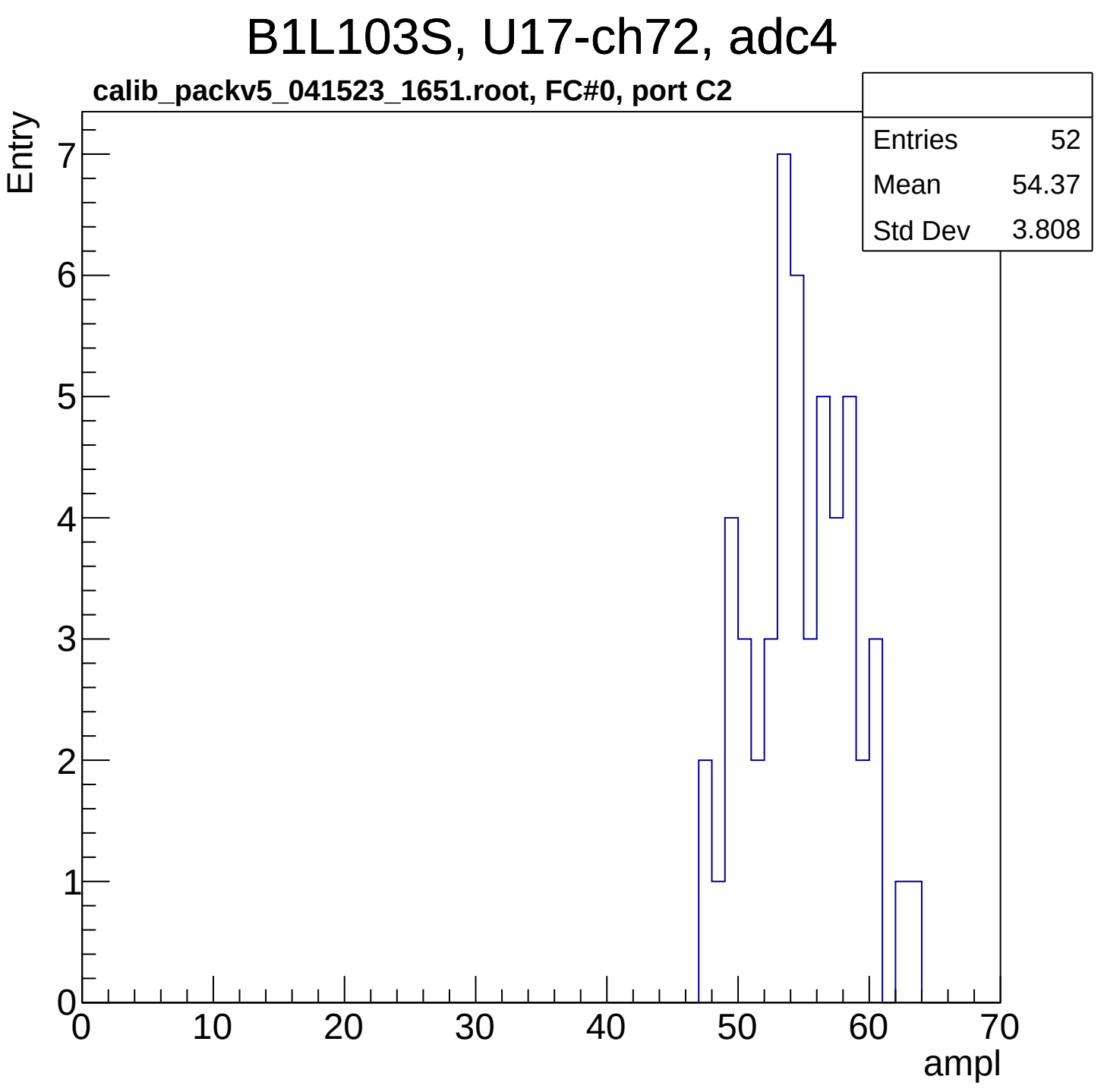
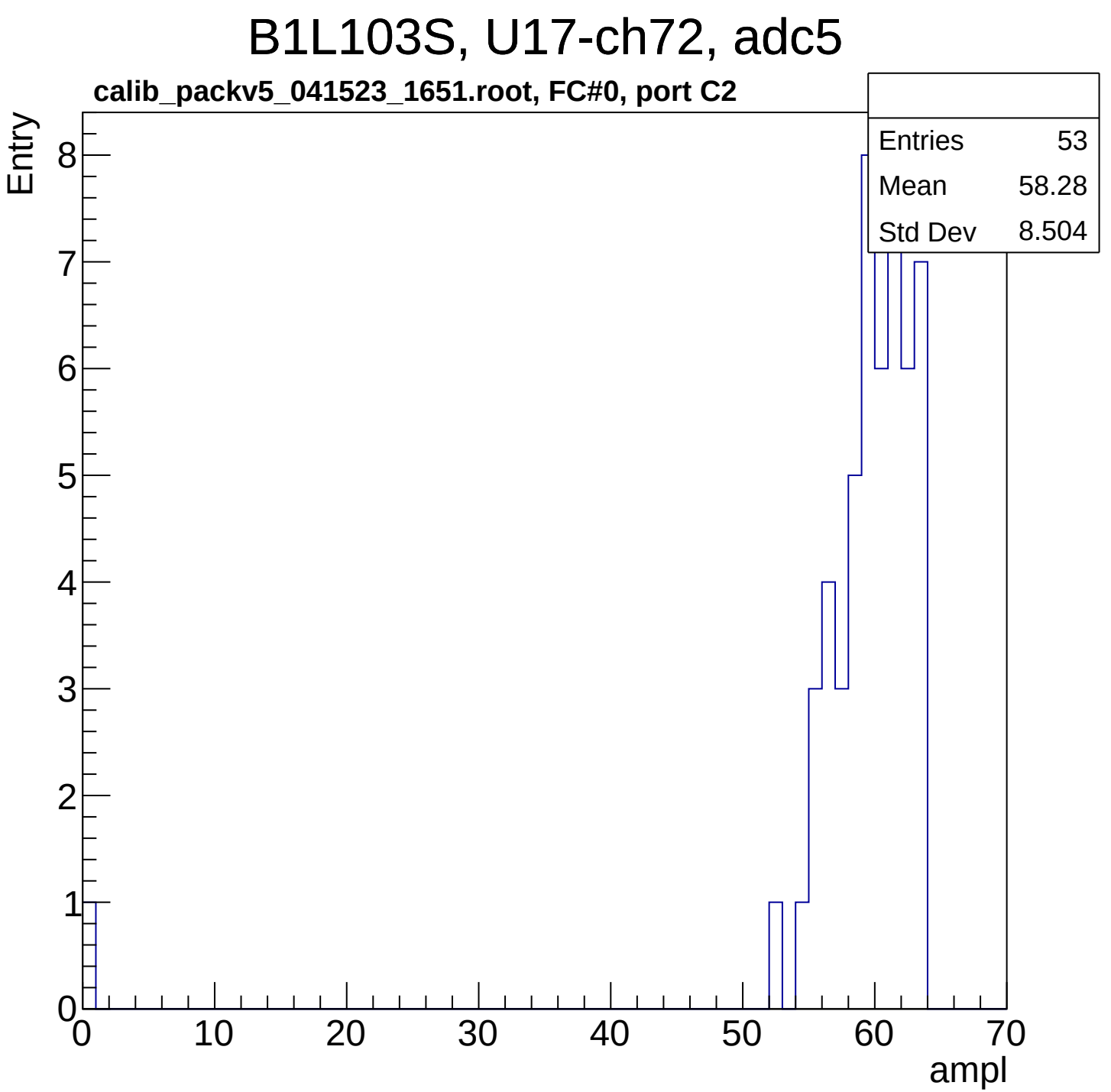
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U17-ch72, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 54.37
Std Dev 3.808
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U17-ch72, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 58.28
Std Dev 8.504
Entry
ampl
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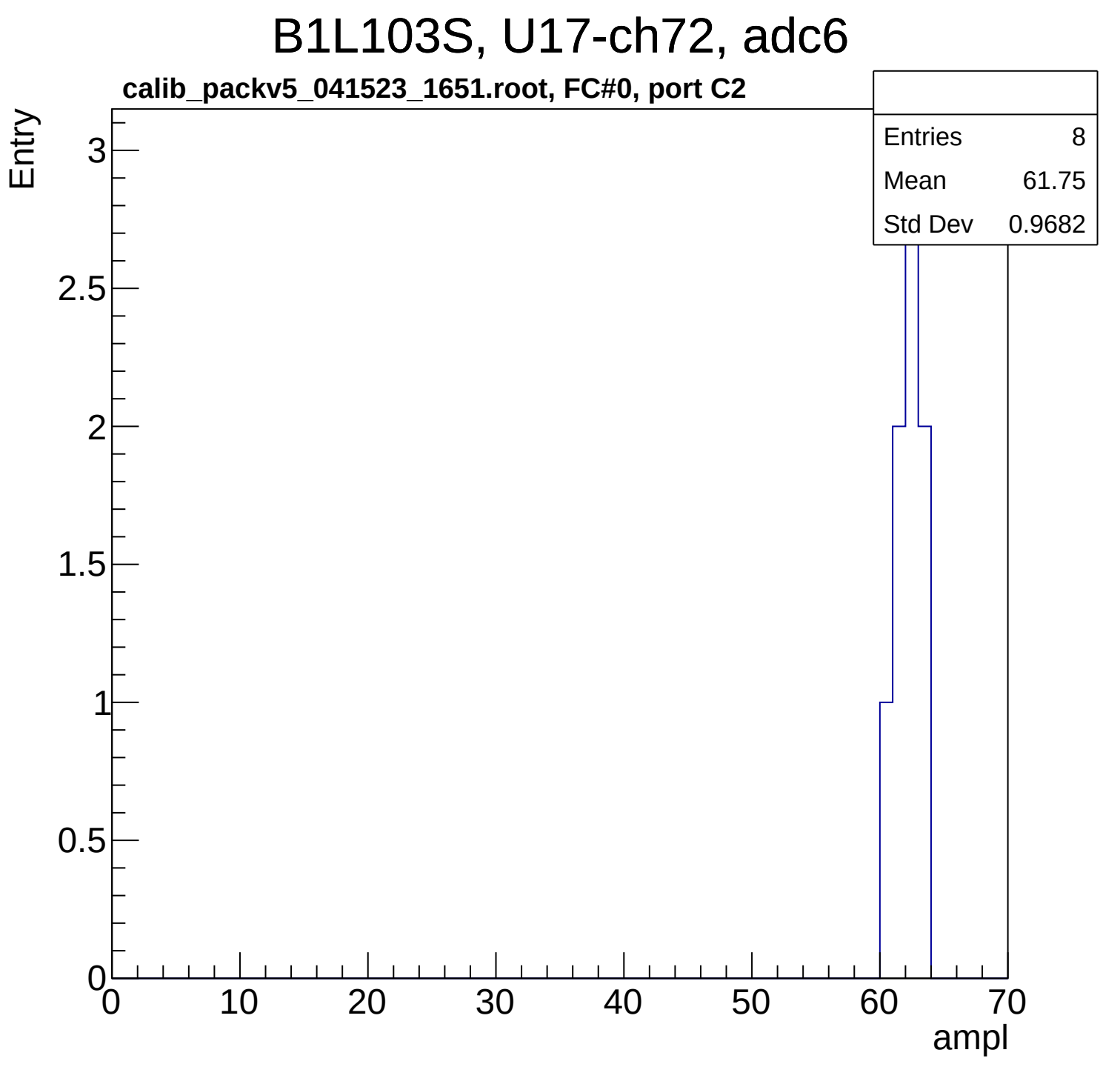
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U17-ch72, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 61.75
Std Dev 0.9682
Entry
ampl
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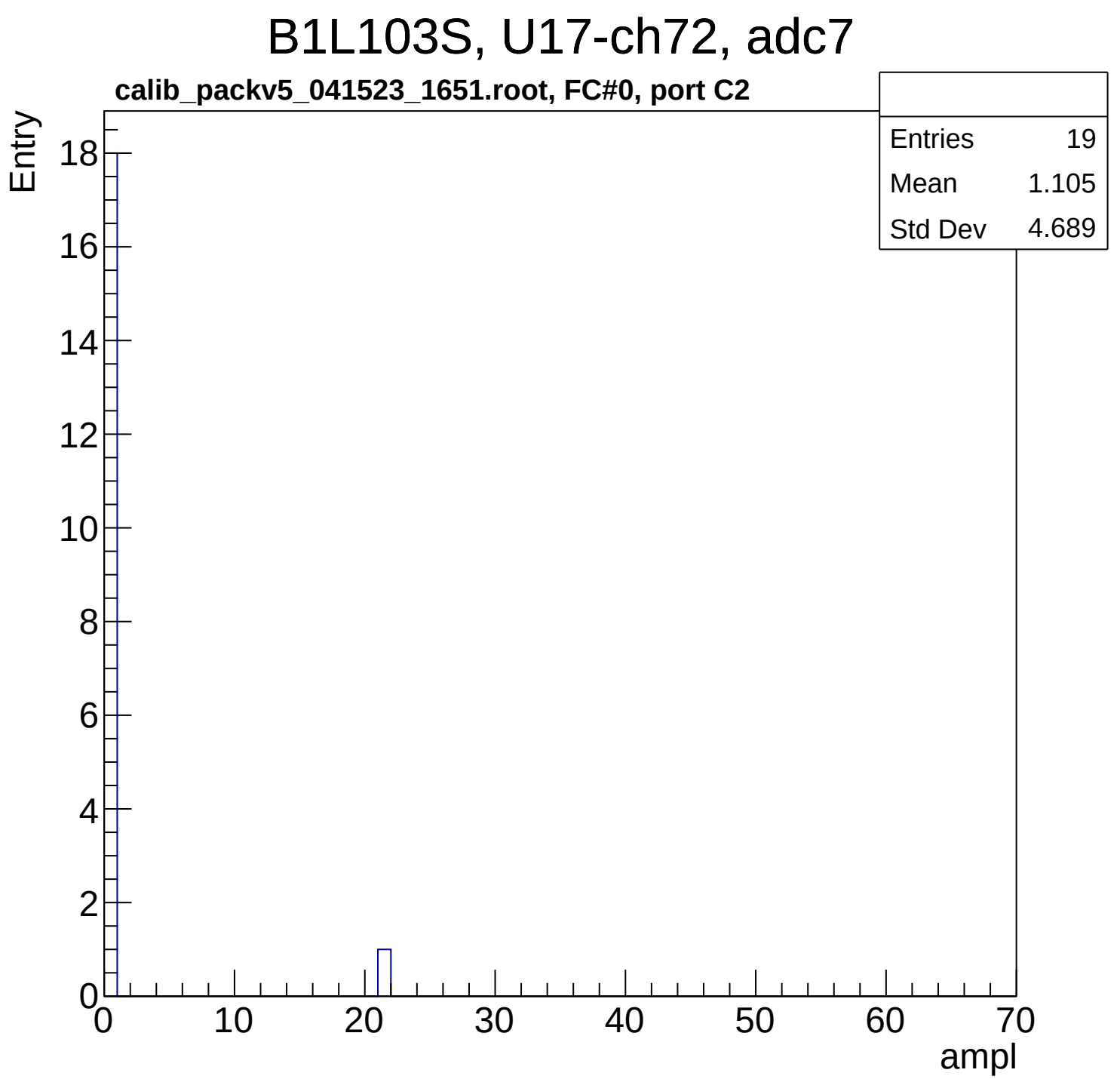
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U17-ch72, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.105
Std Dev 4.689
Entry
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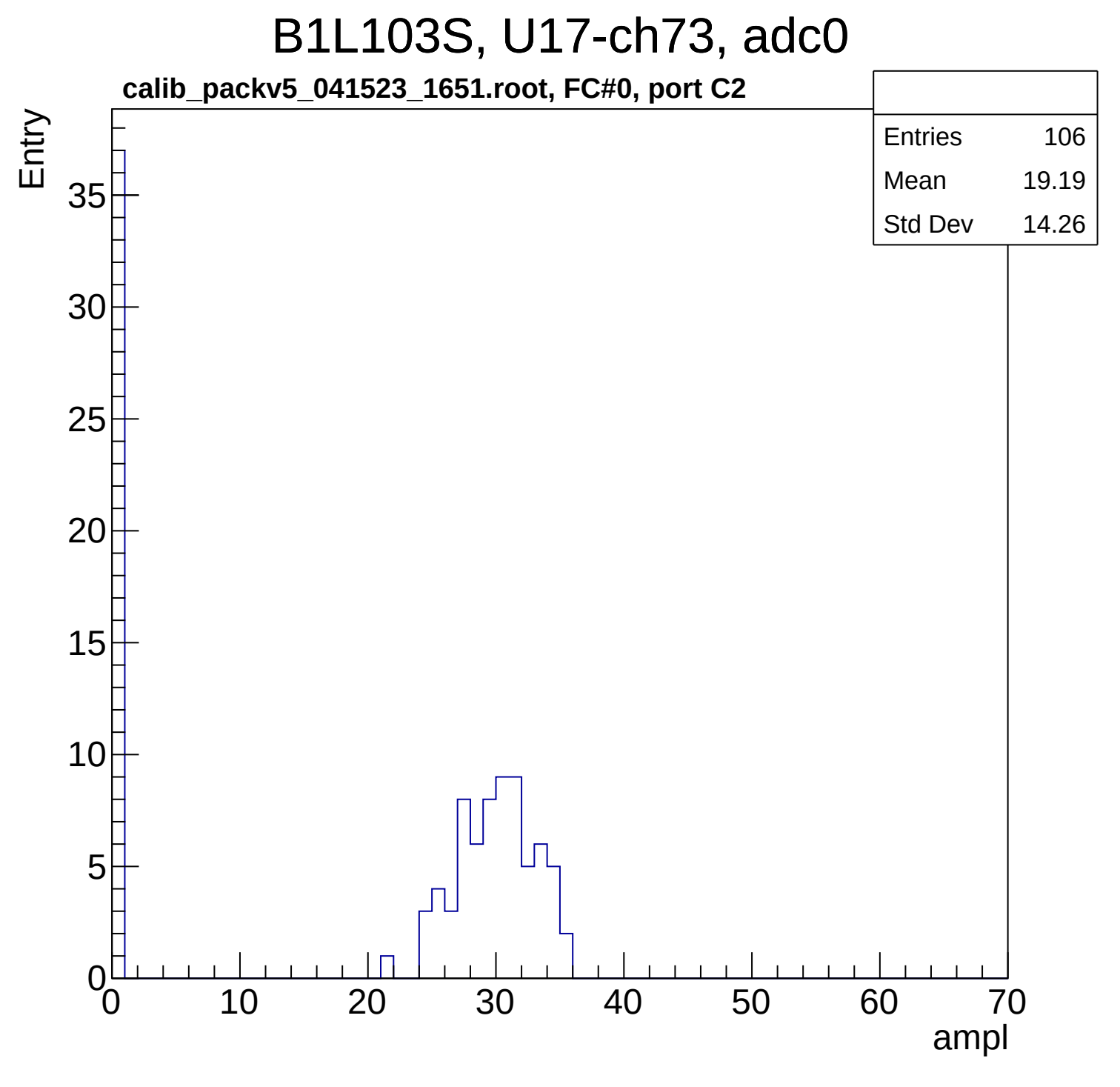
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch73, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 106
Mean 19.19
Std Dev 14.26
Entry
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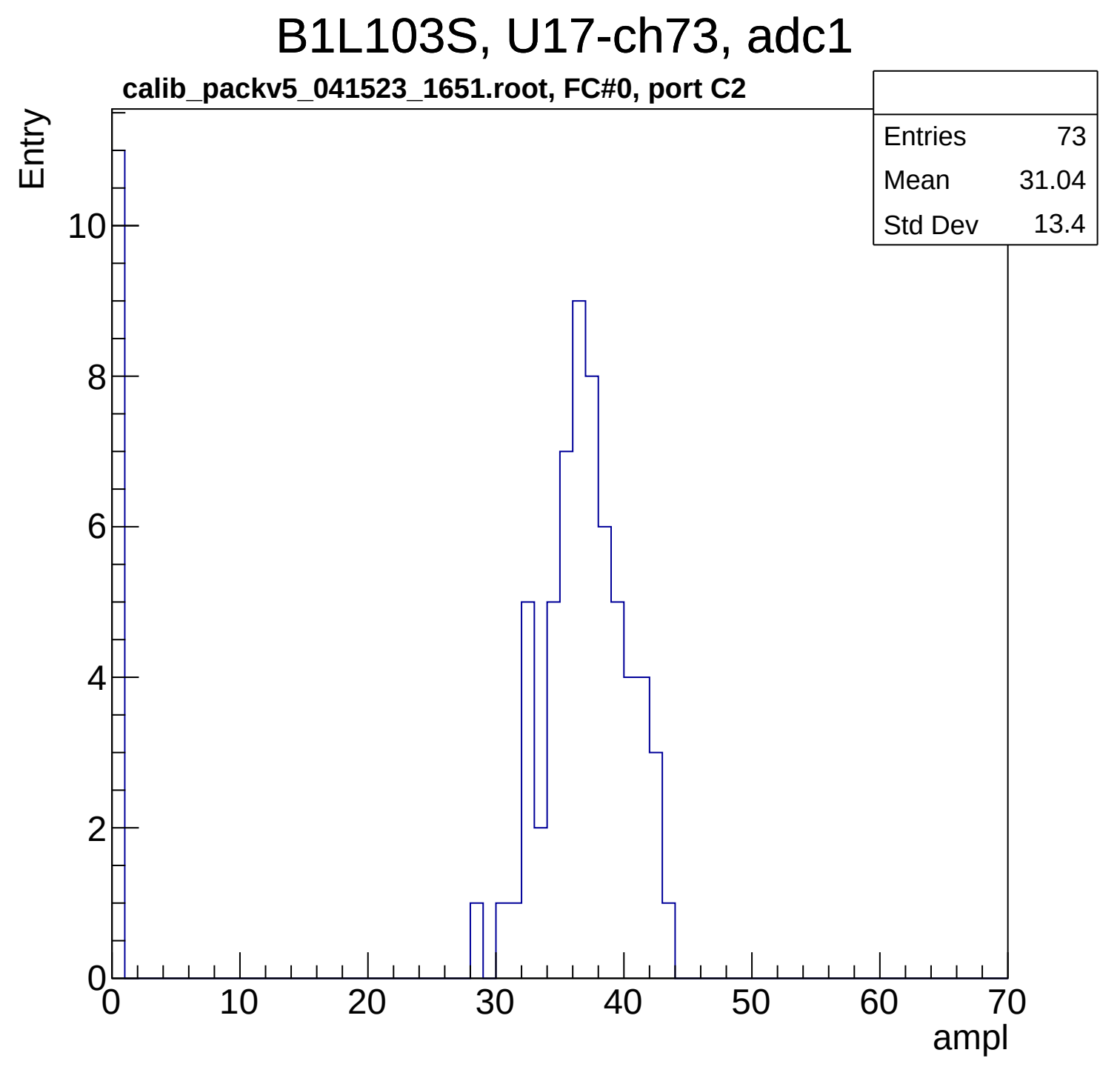
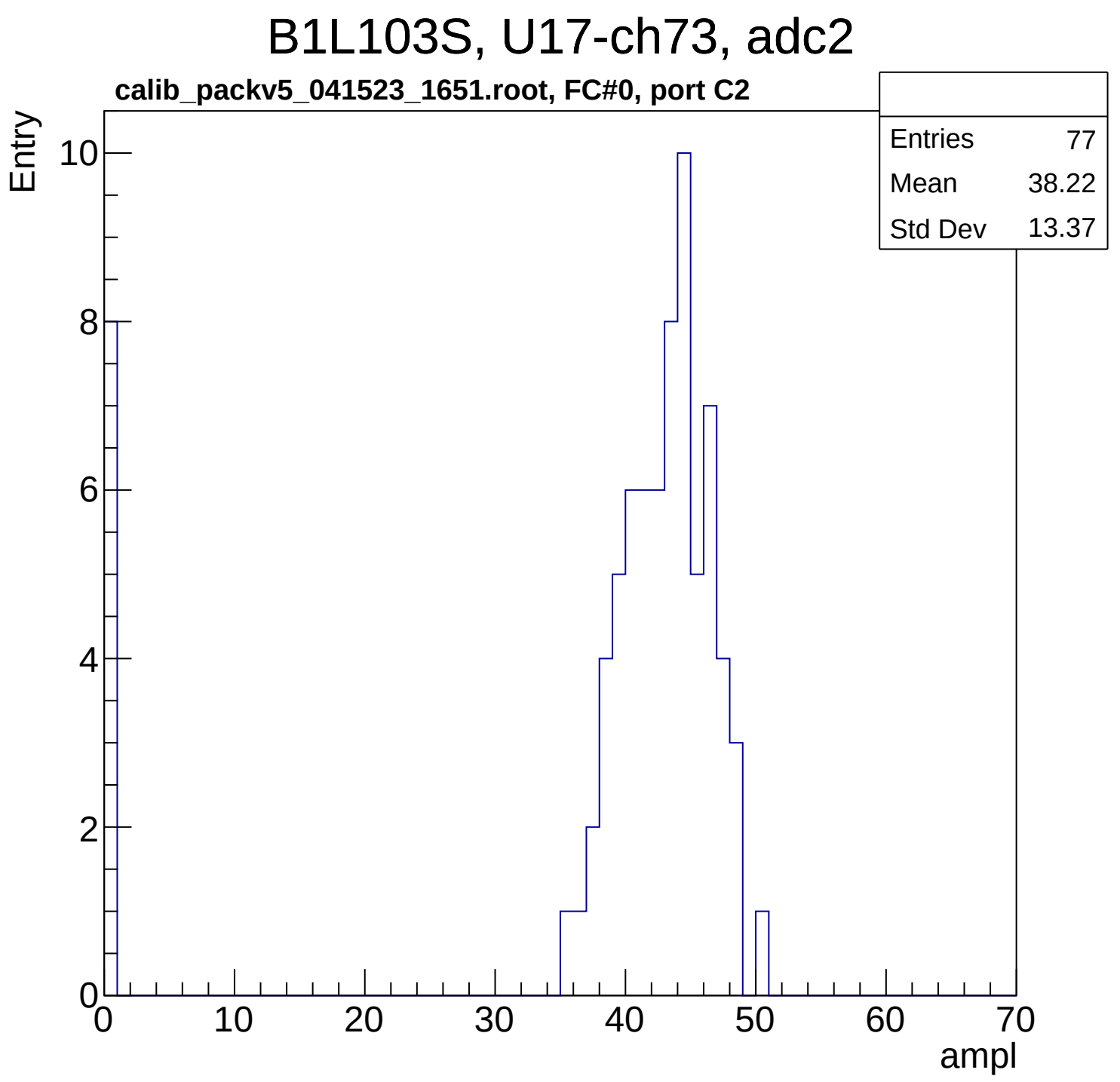
5
10
15
20
25
30
35
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch73, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 31.04
Std Dev 13.4
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch73, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 38.22
Std Dev 13.37
Entry
ampl
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2
4
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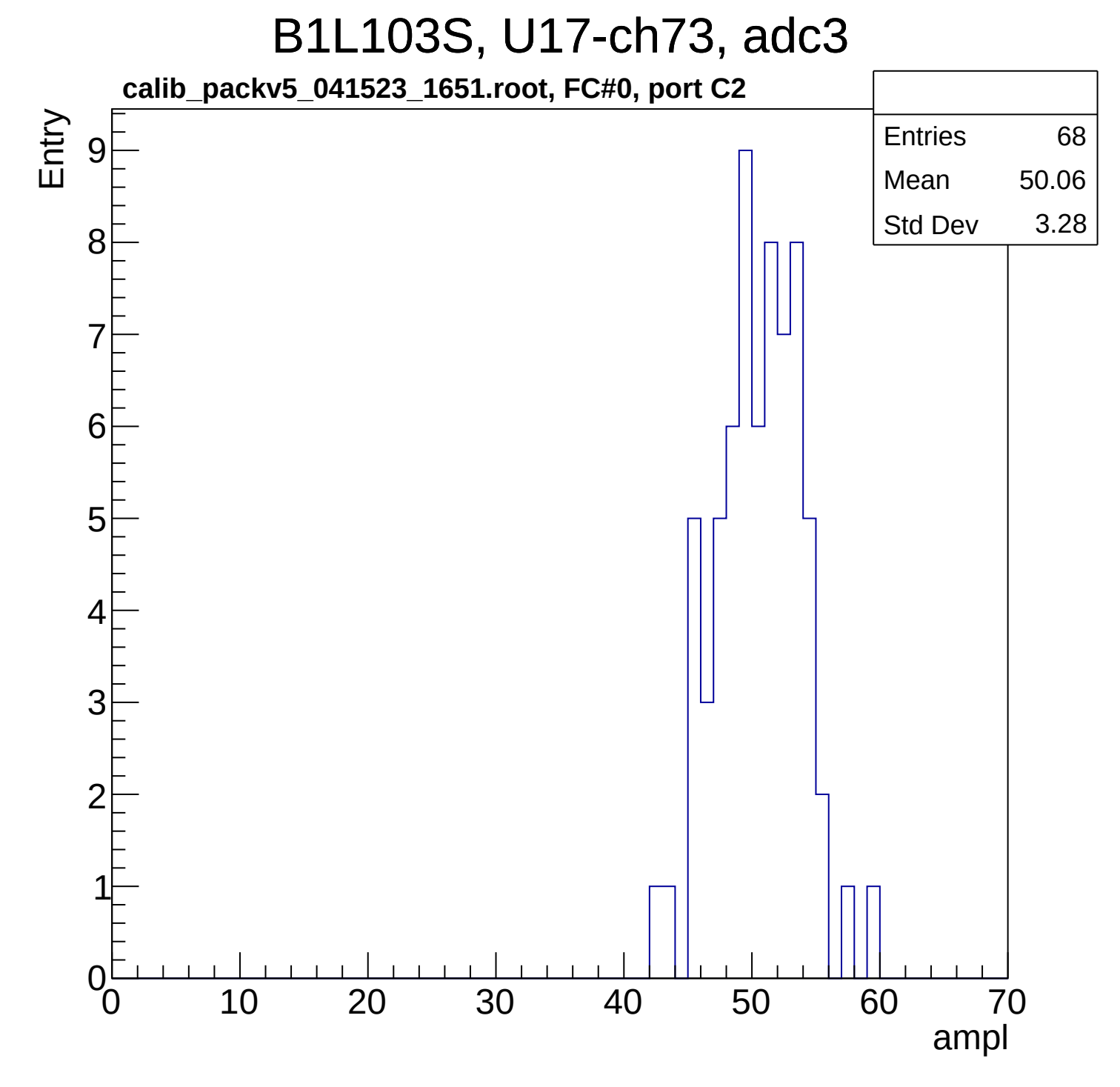
8
10
0
10
20
30
40
50
60
70


B1L103S, U17-ch73, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 50.06
Std Dev 3.28
Entry
ampl
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10
20
30
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50
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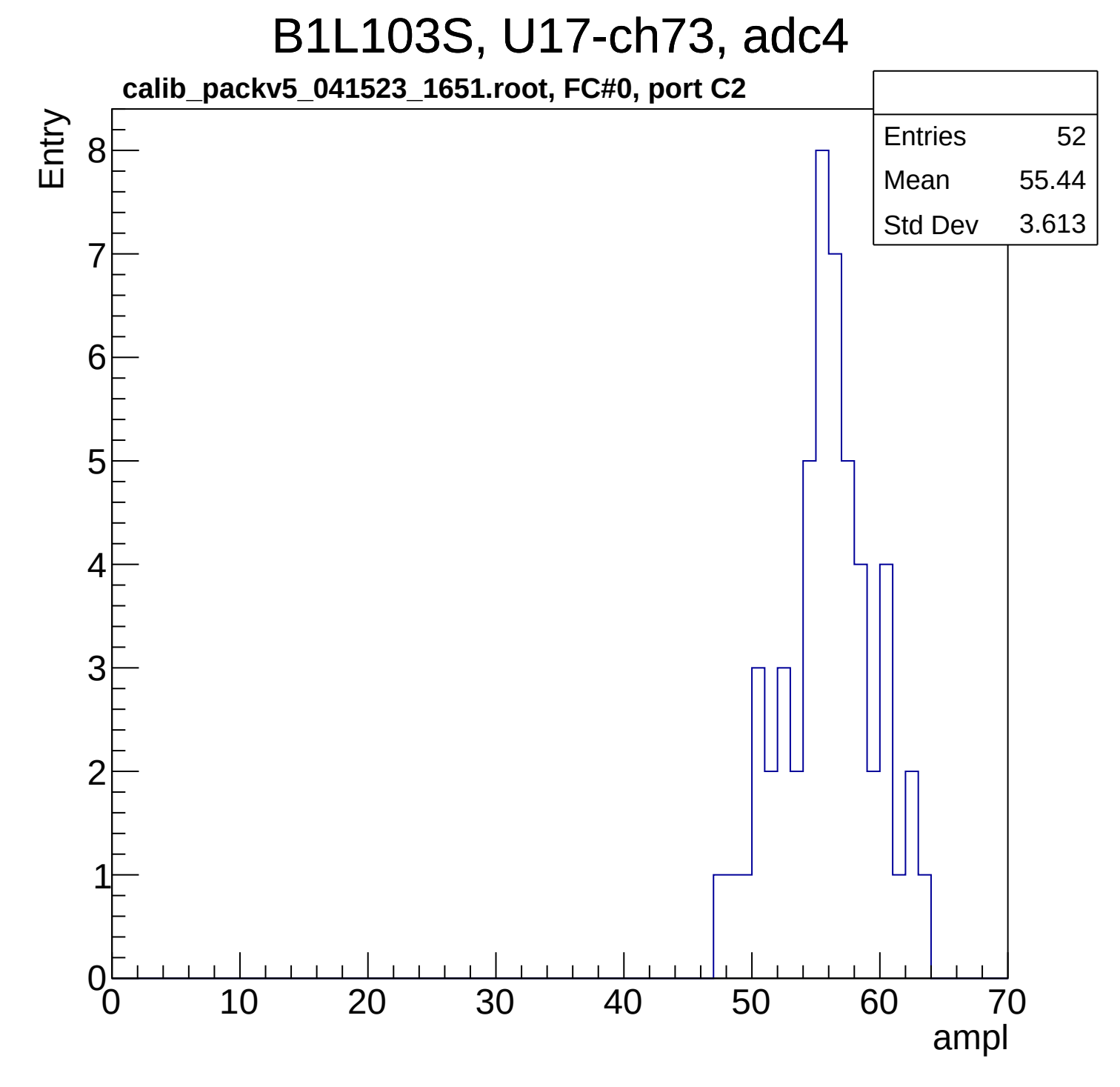
70
1
2
3
4
5
6
7
8
9


B1L103S, U17-ch73, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 55.44
Std Dev 3.613
Entry
ampl
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2
3
4
5
6
7
8
0
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40
50
60
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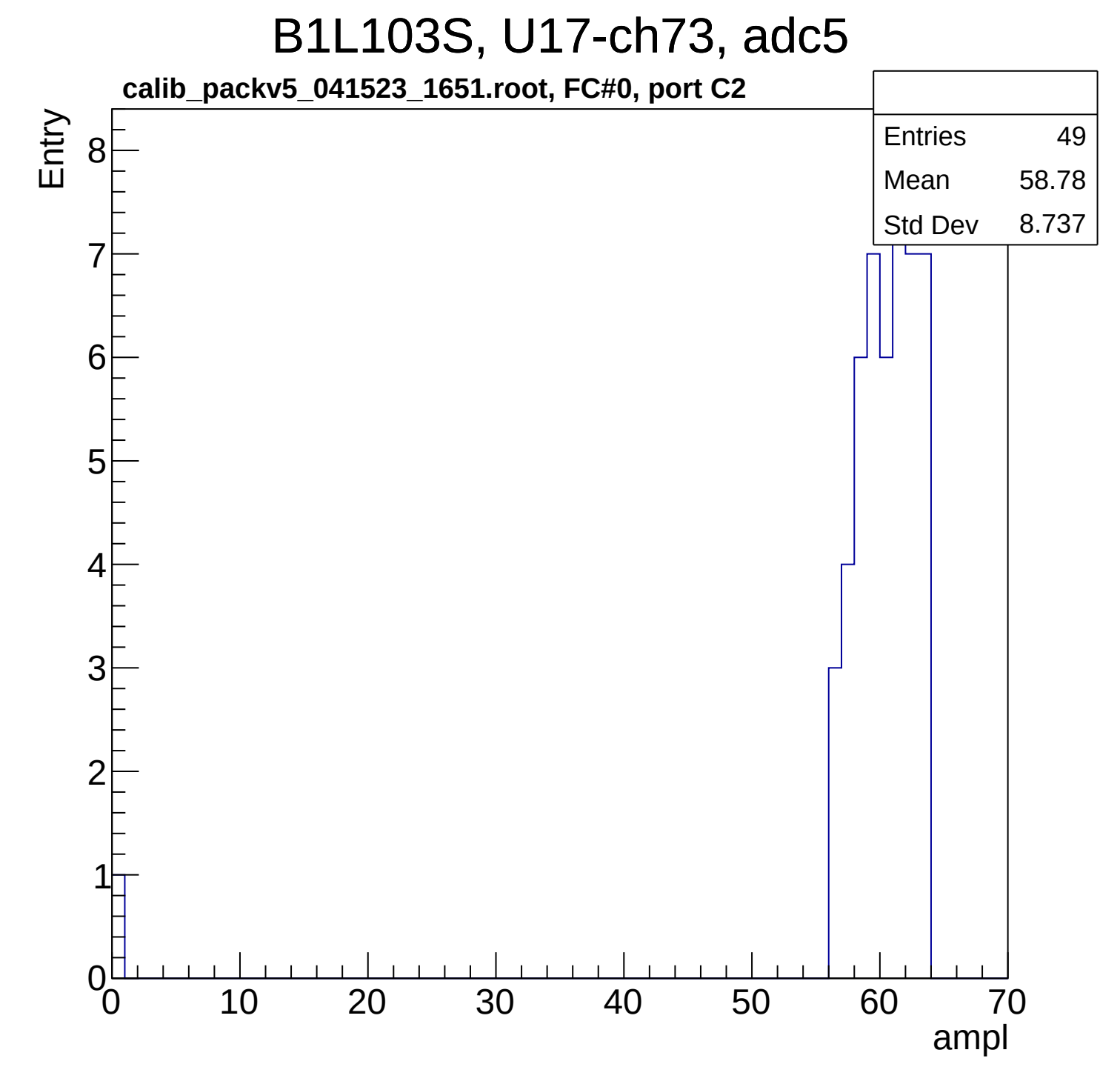
B1L103S, U17-ch73, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 58.78
Std Dev 8.737
Entry
ampl
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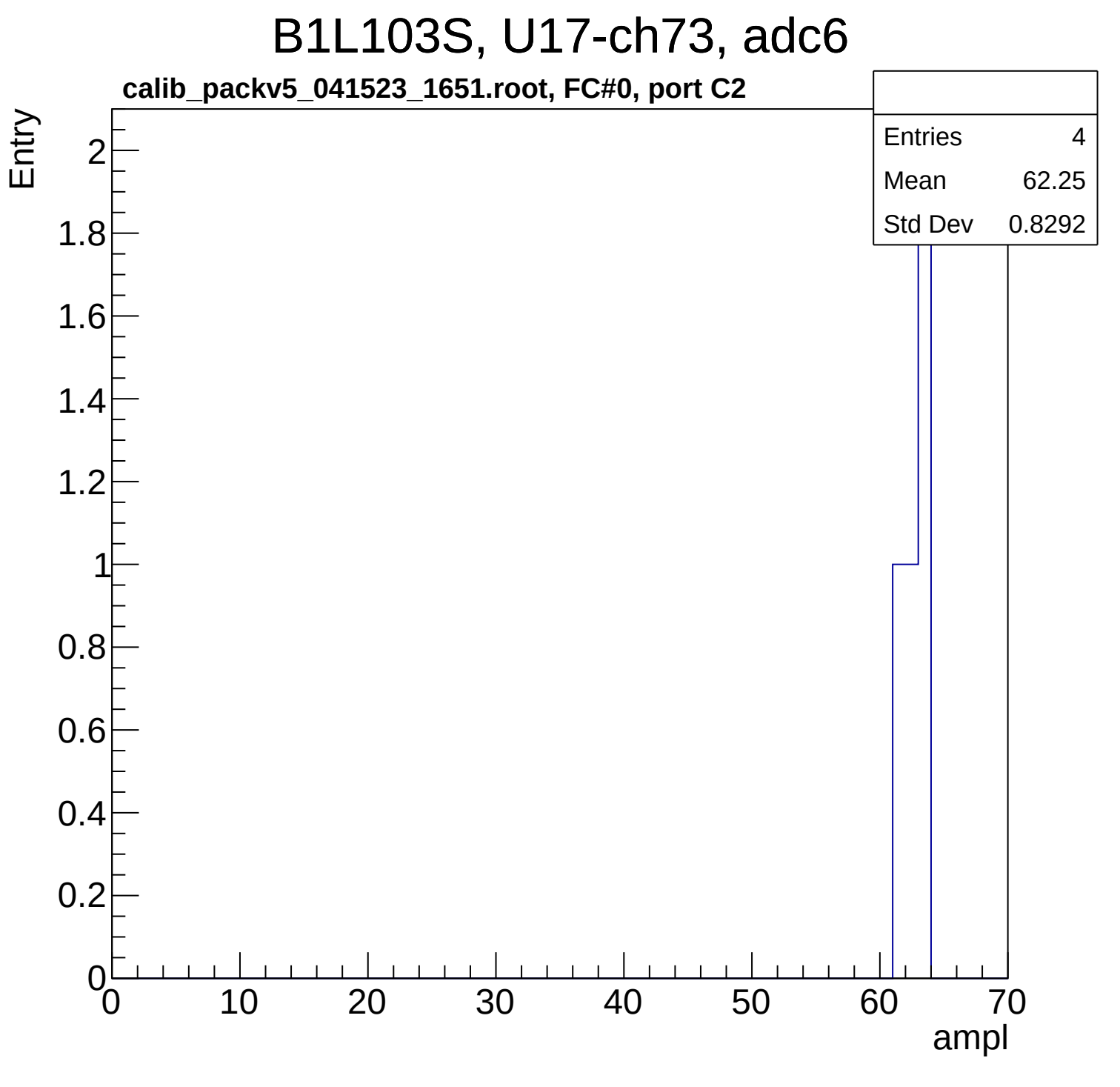
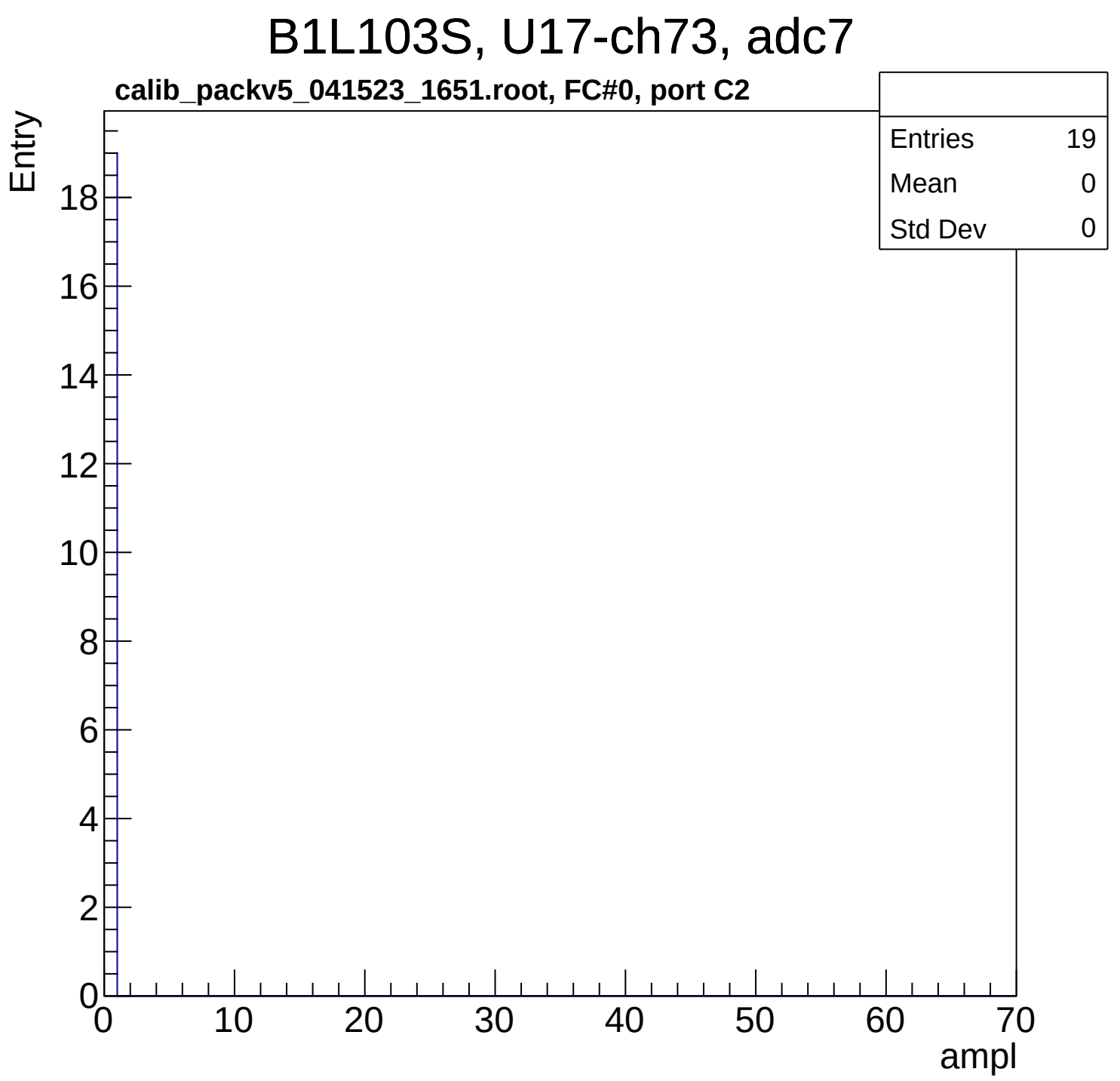
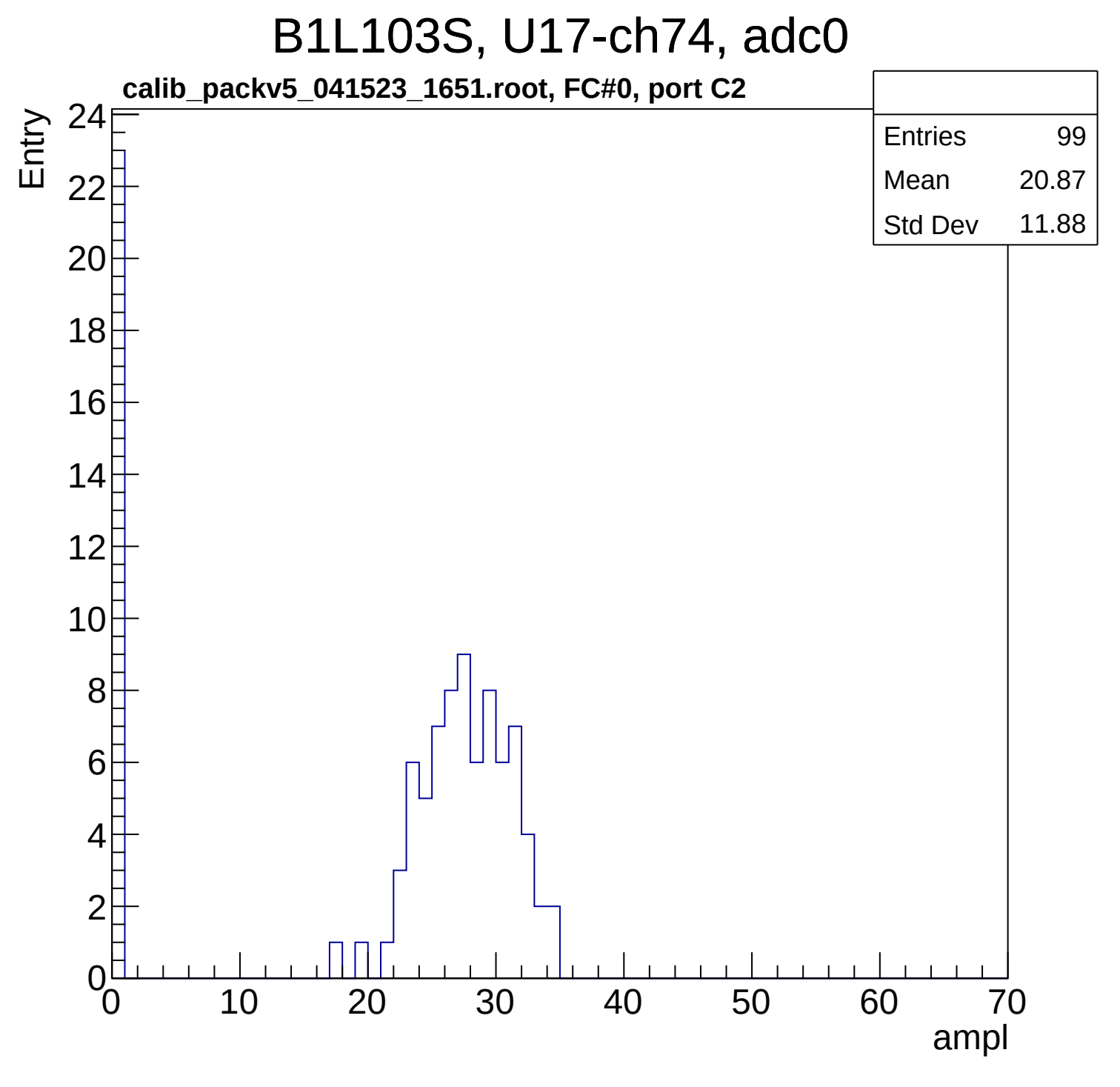
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U17-ch73, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 4
Mean 62.25
Std Dev 0.8292
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U17-ch73, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch74, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 99
Mean 20.87
Std Dev 11.88
Entry
ampl
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2
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10
12
14
16
18
20
22
24
0
10
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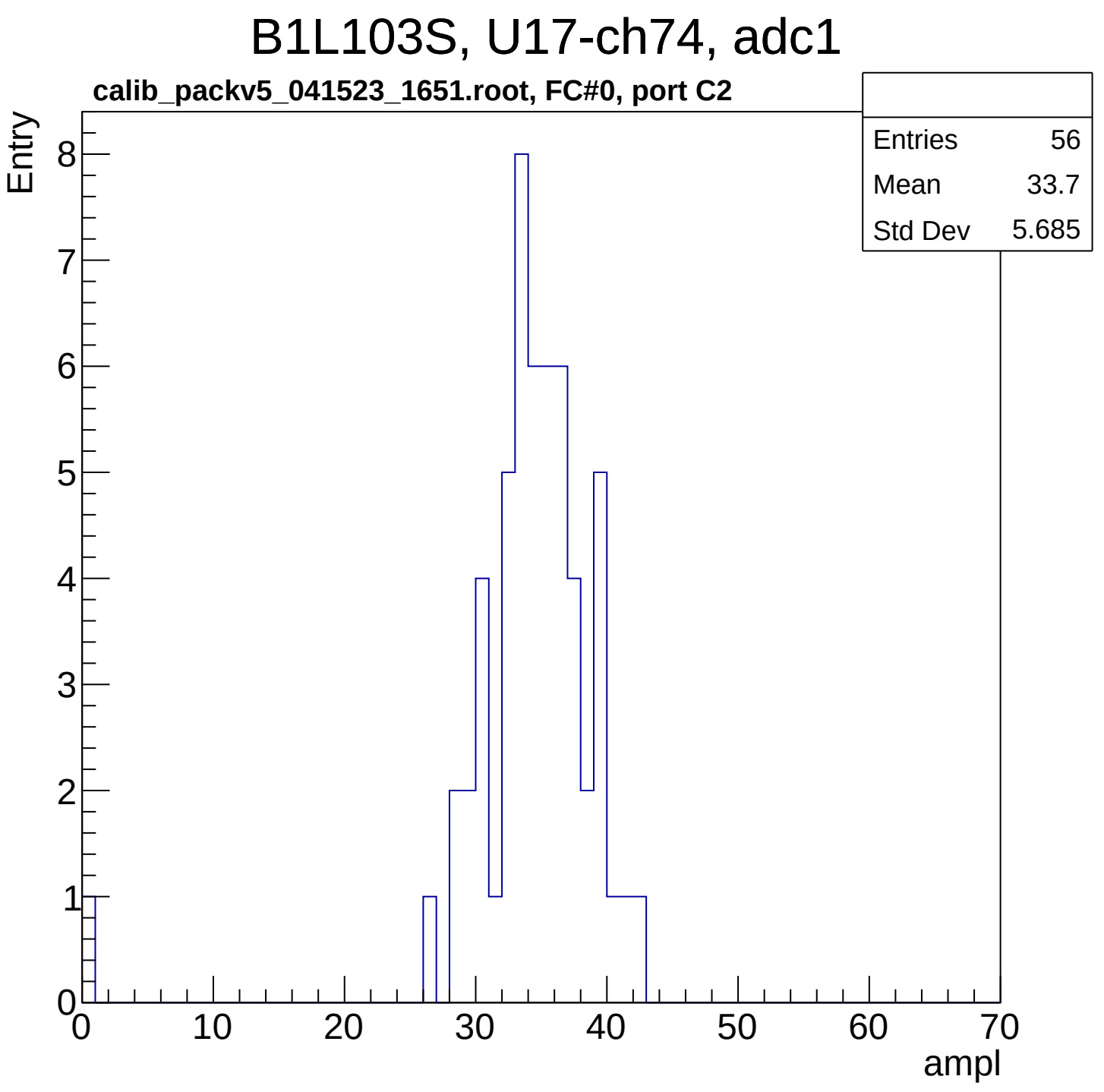
60
70


B1L103S, U17-ch74, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 33.7
Std Dev 5.685
Entry
ampl
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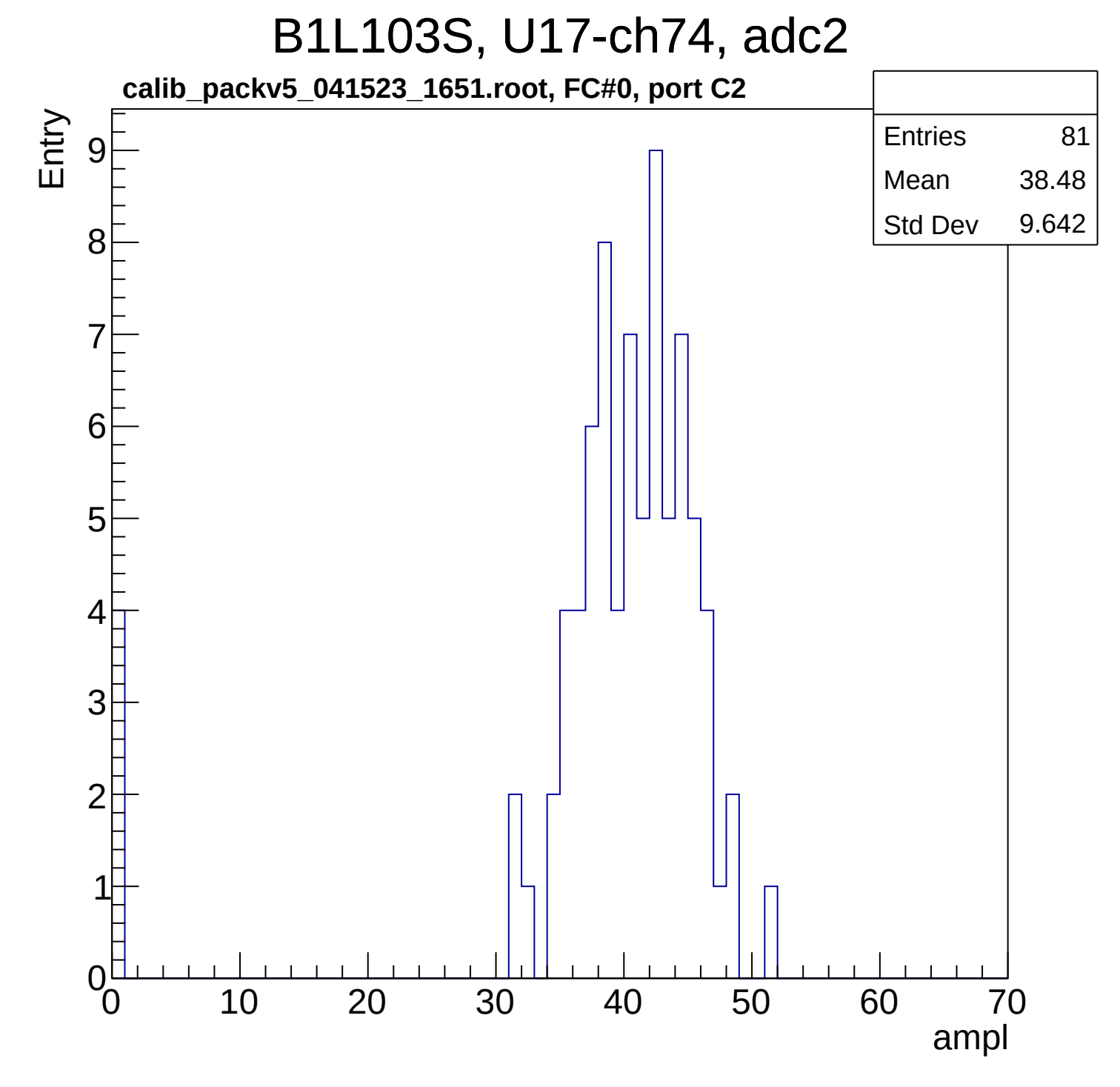
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U17-ch74, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 38.48
Std Dev 9.642
Entry
ampl
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2
3
4
5
6
7
8
9
0
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50
60
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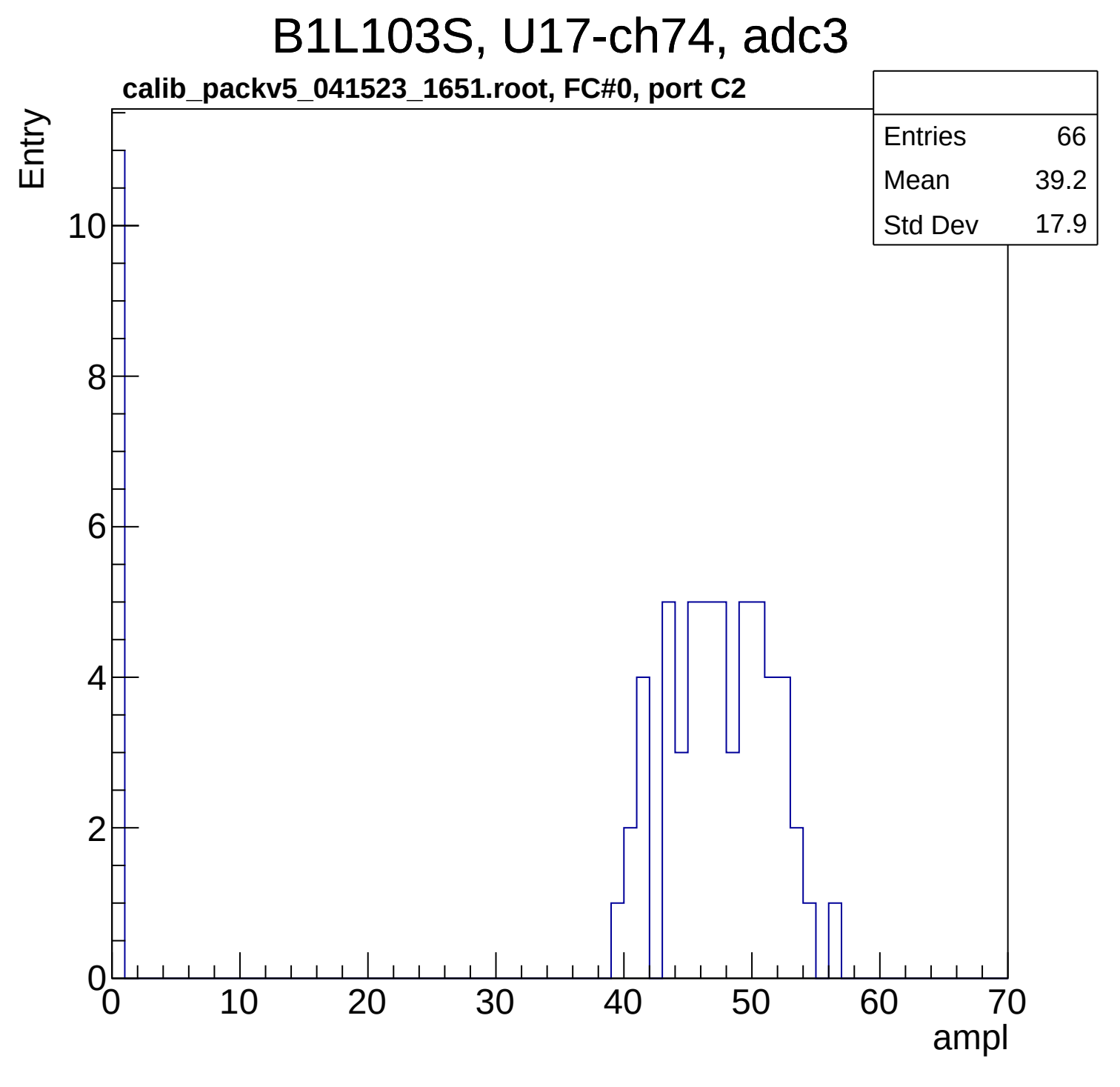
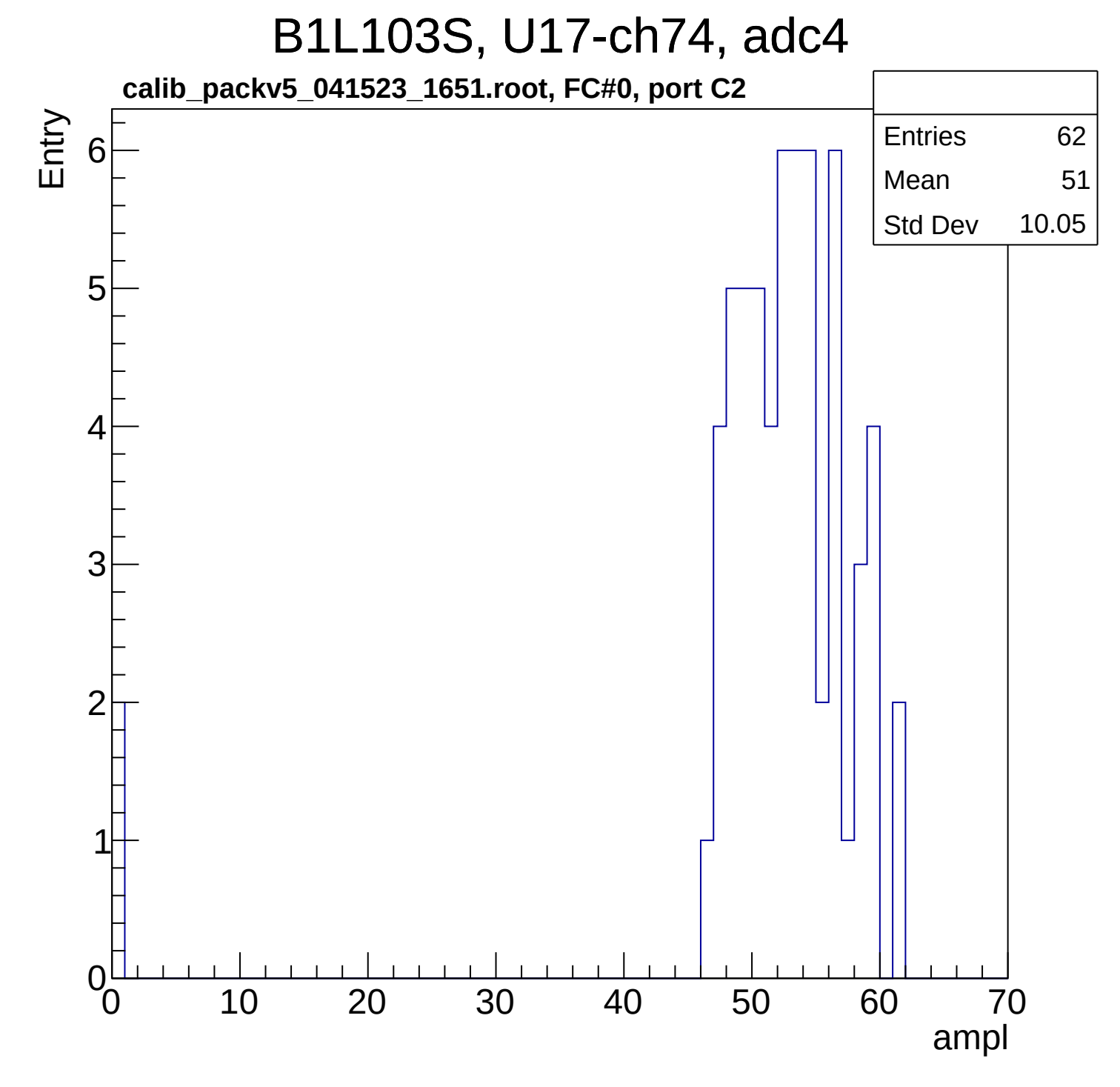

B1L103S, U17-ch74, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 39.2
Std Dev 17.9
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch74, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 51
Std Dev 10.05
Entry
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2
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4
5
6
0
10
20
30
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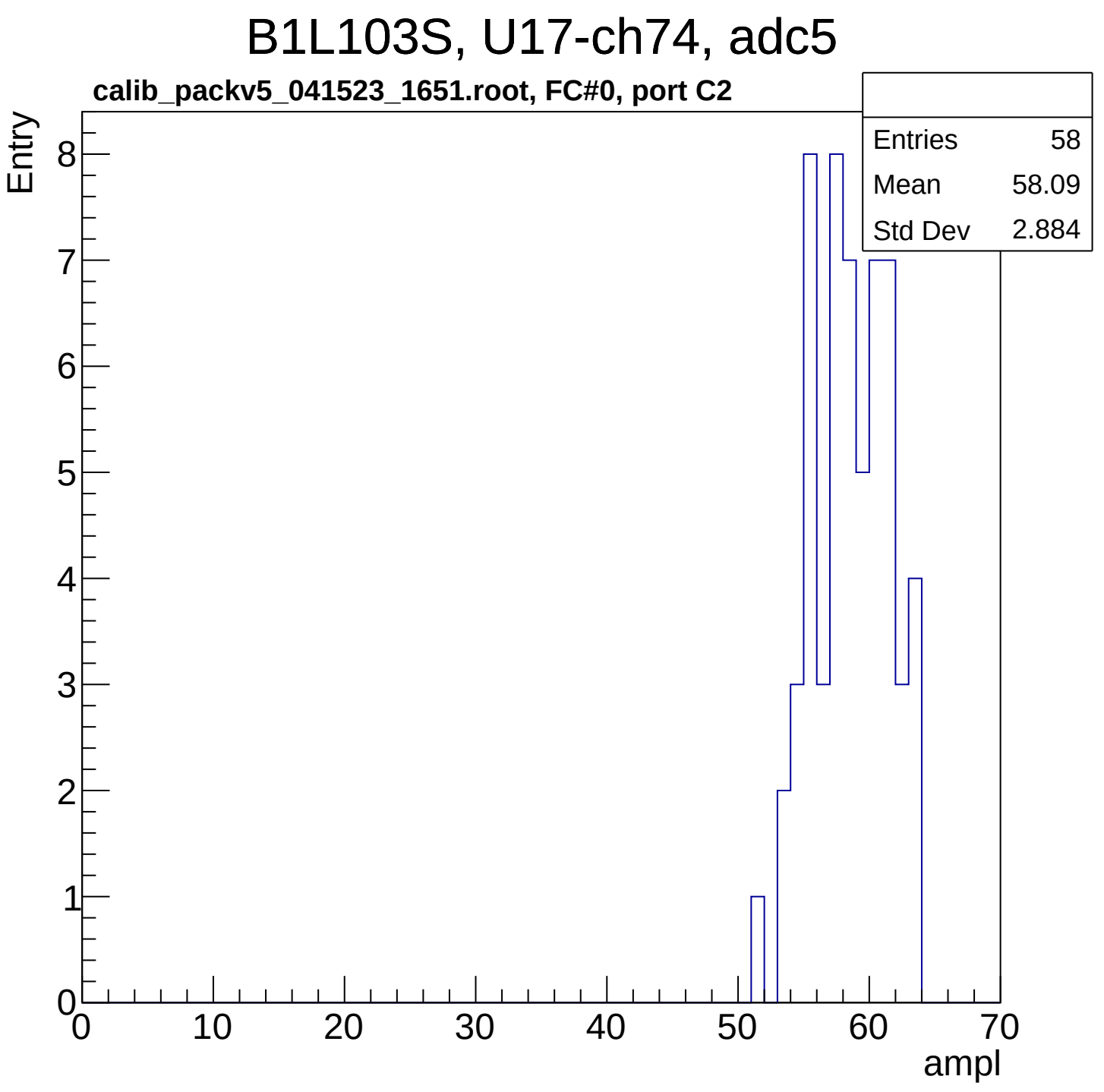
50
60
70
ampl


B1L103S, U17-ch74, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 58.09
Std Dev 2.884
Entry
ampl
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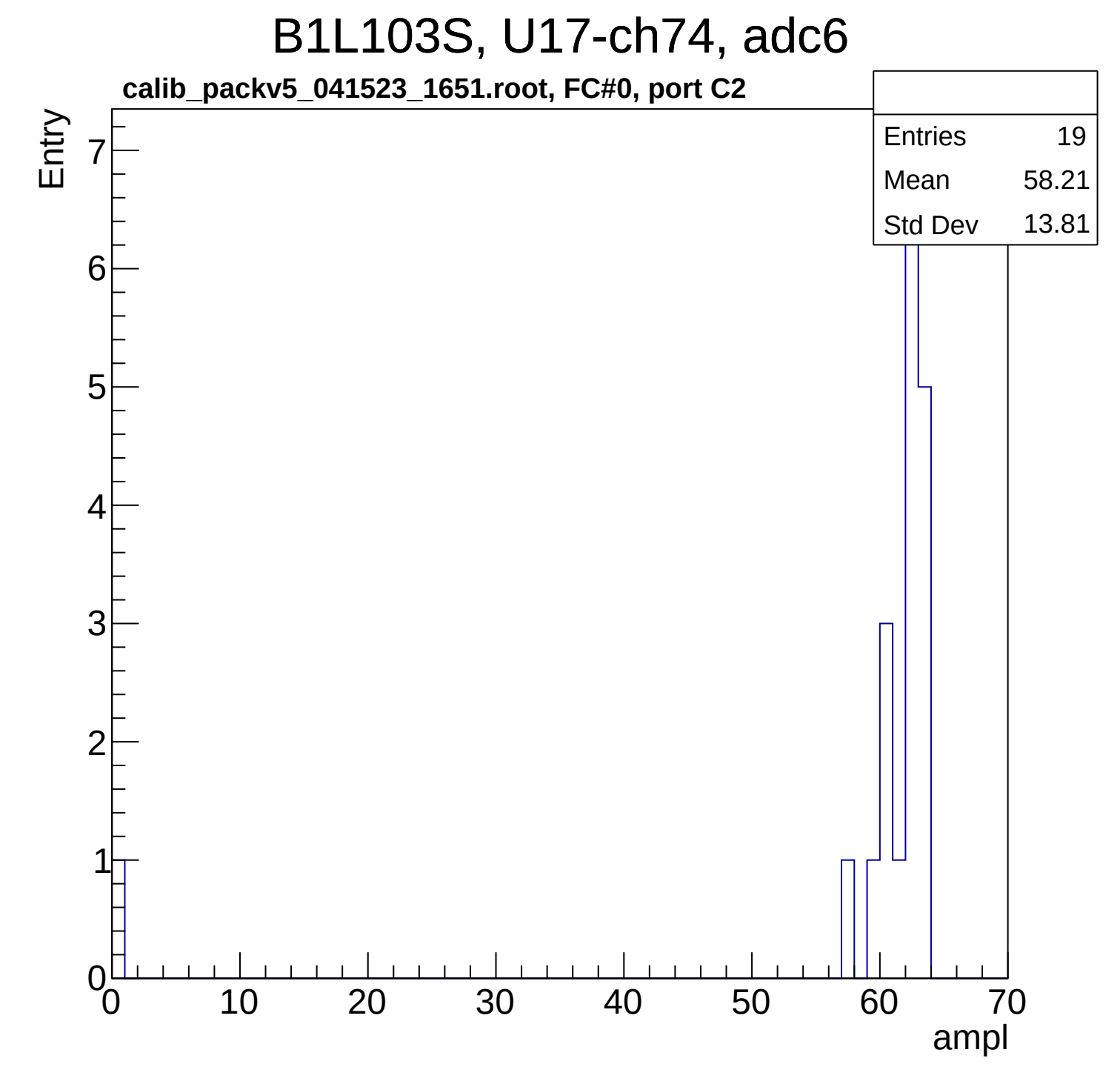
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U17-ch74, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 58.21
Std Dev 13.81
Entry
ampl
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1
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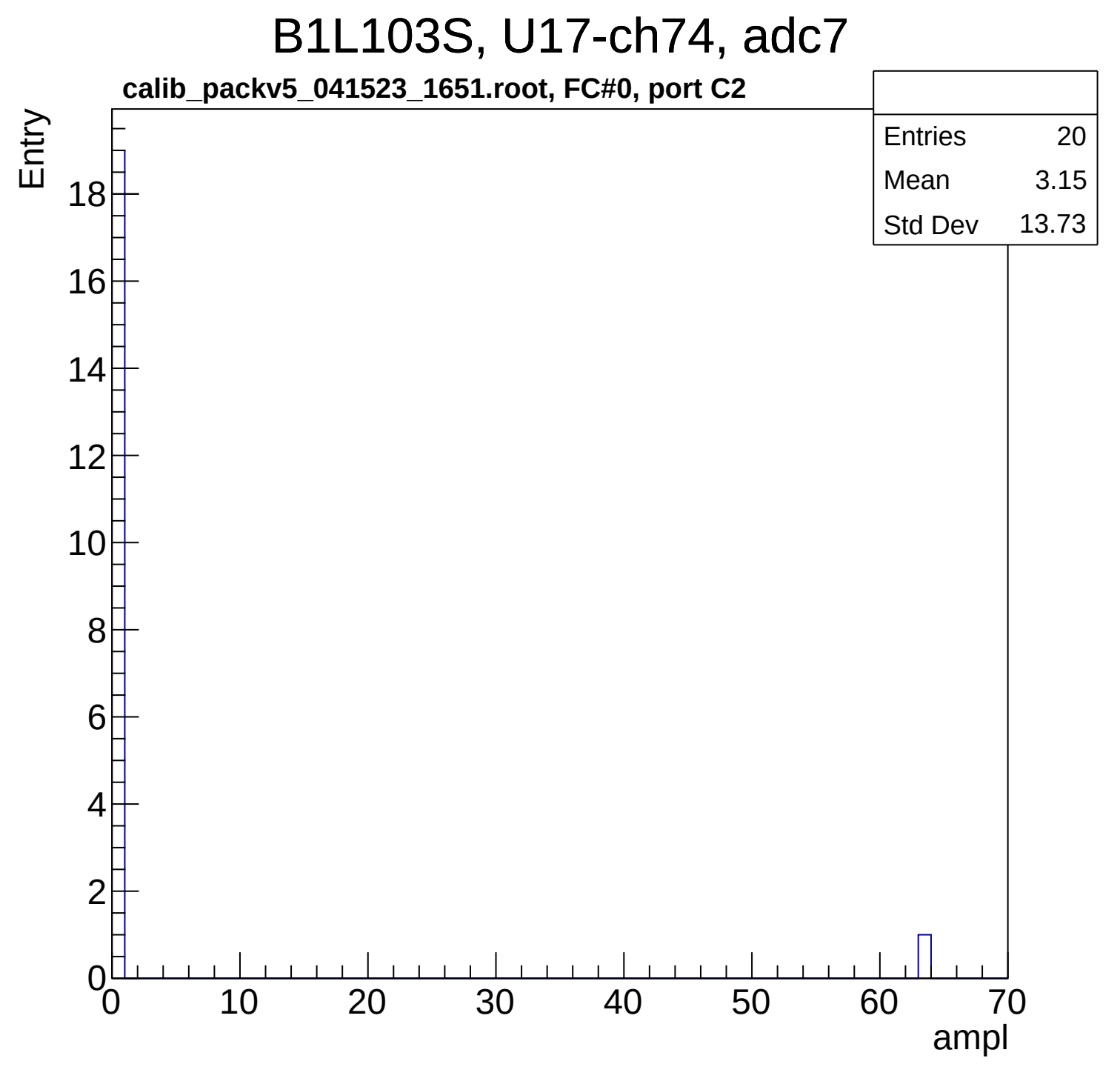
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U17-ch74, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
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2
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6
8
10
12
14
16
18
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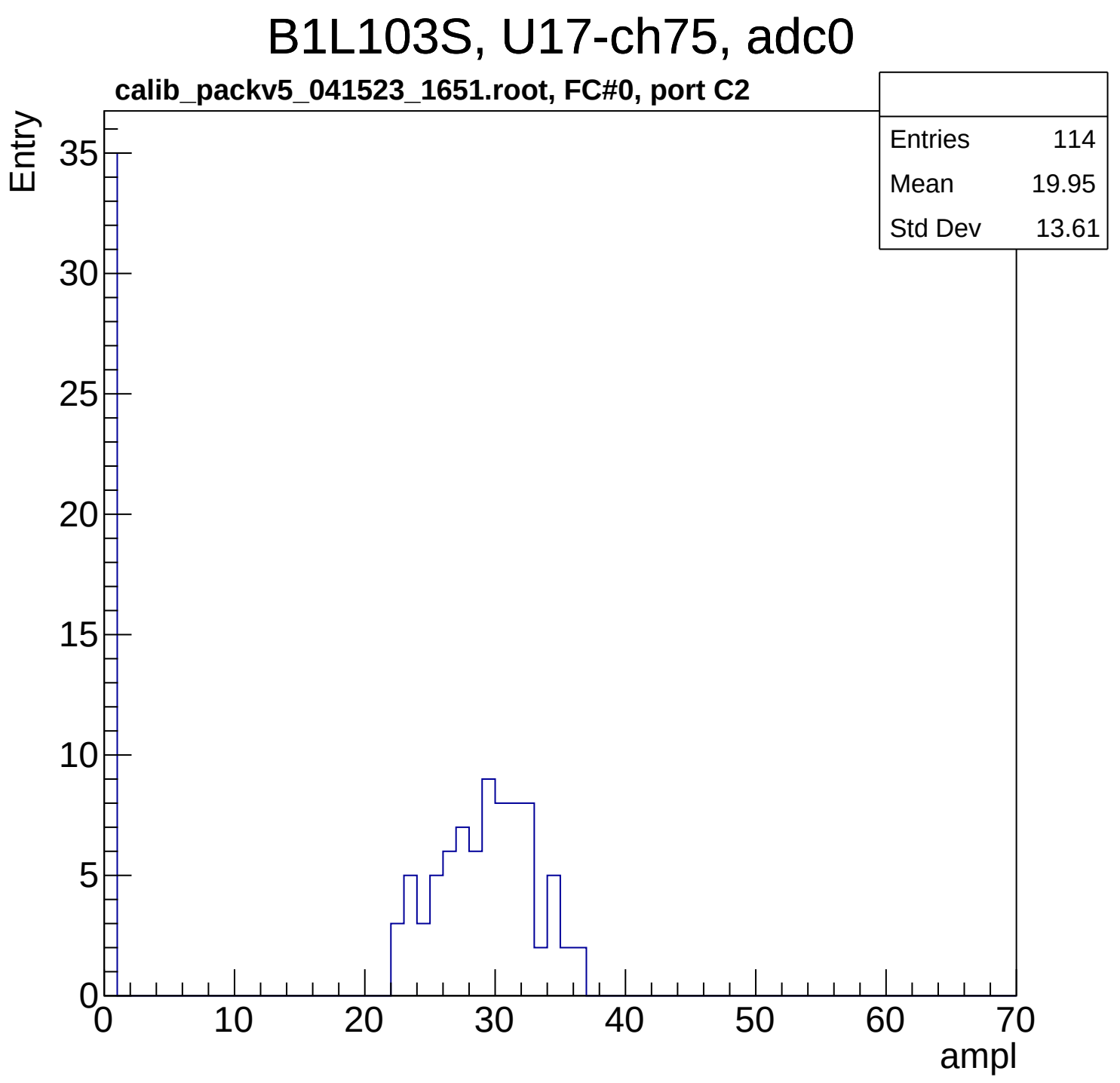
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch75, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 114
Mean 19.95
Std Dev 13.61
Entry
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5
10
15
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25
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35
0
10
20
30
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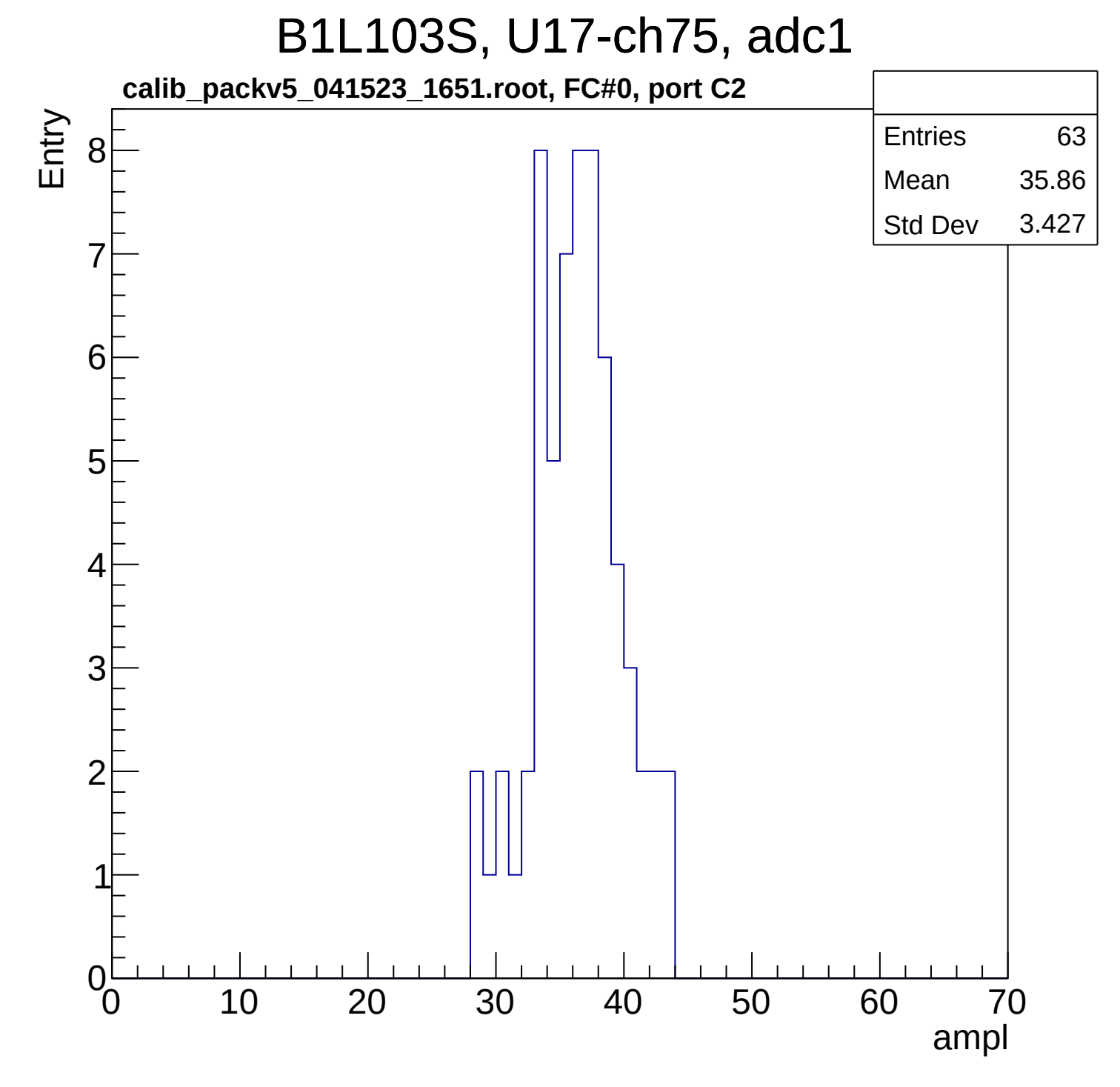
50
60
70
ampl


B1L103S, U17-ch75, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 35.86
Std Dev 3.427
Entry
ampl
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4
5
6
7
8
0
10
20
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40
50
60
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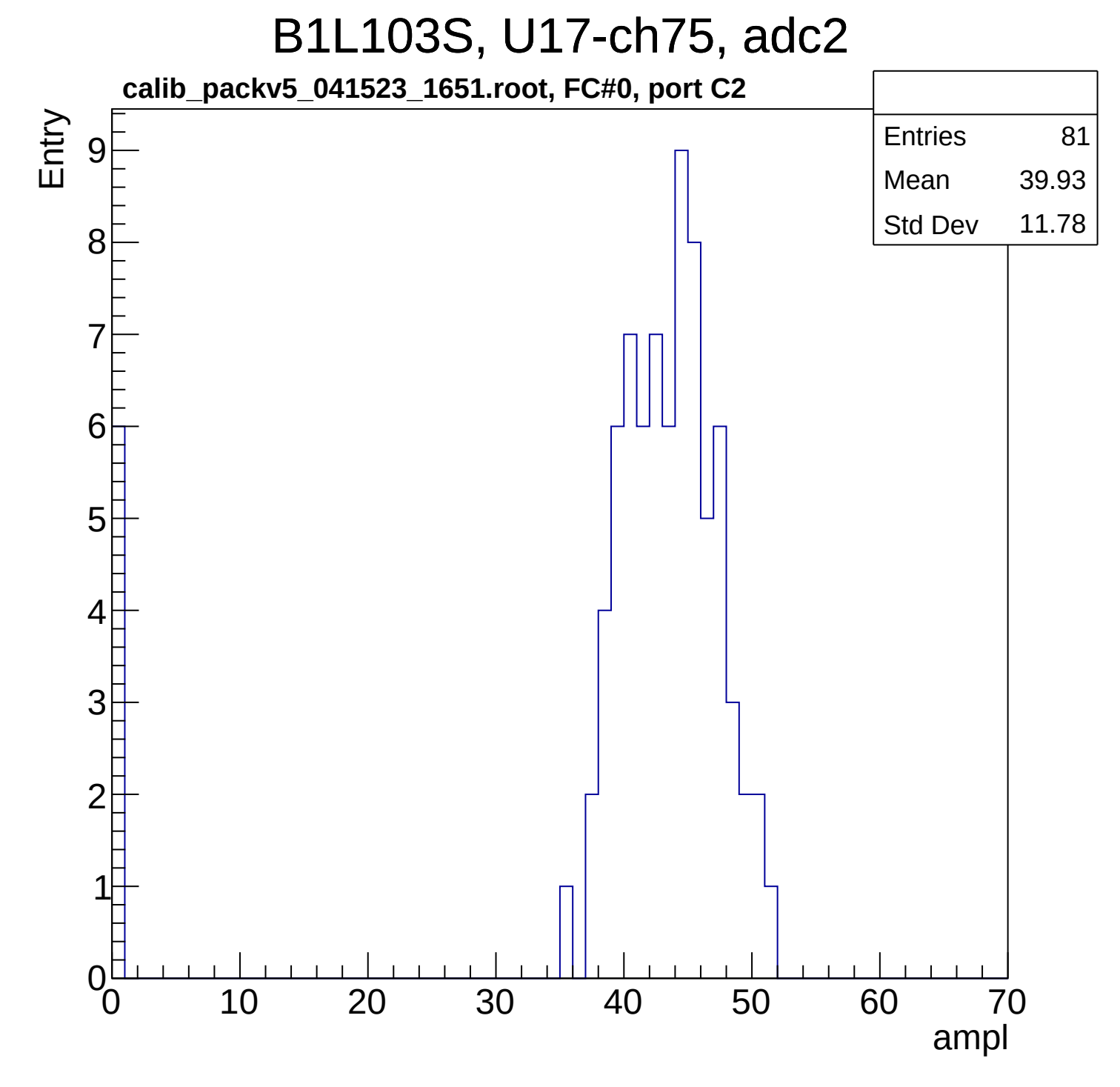
B1L103S, U17-ch75, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 39.93
Std Dev 11.78
Entry
ampl
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0
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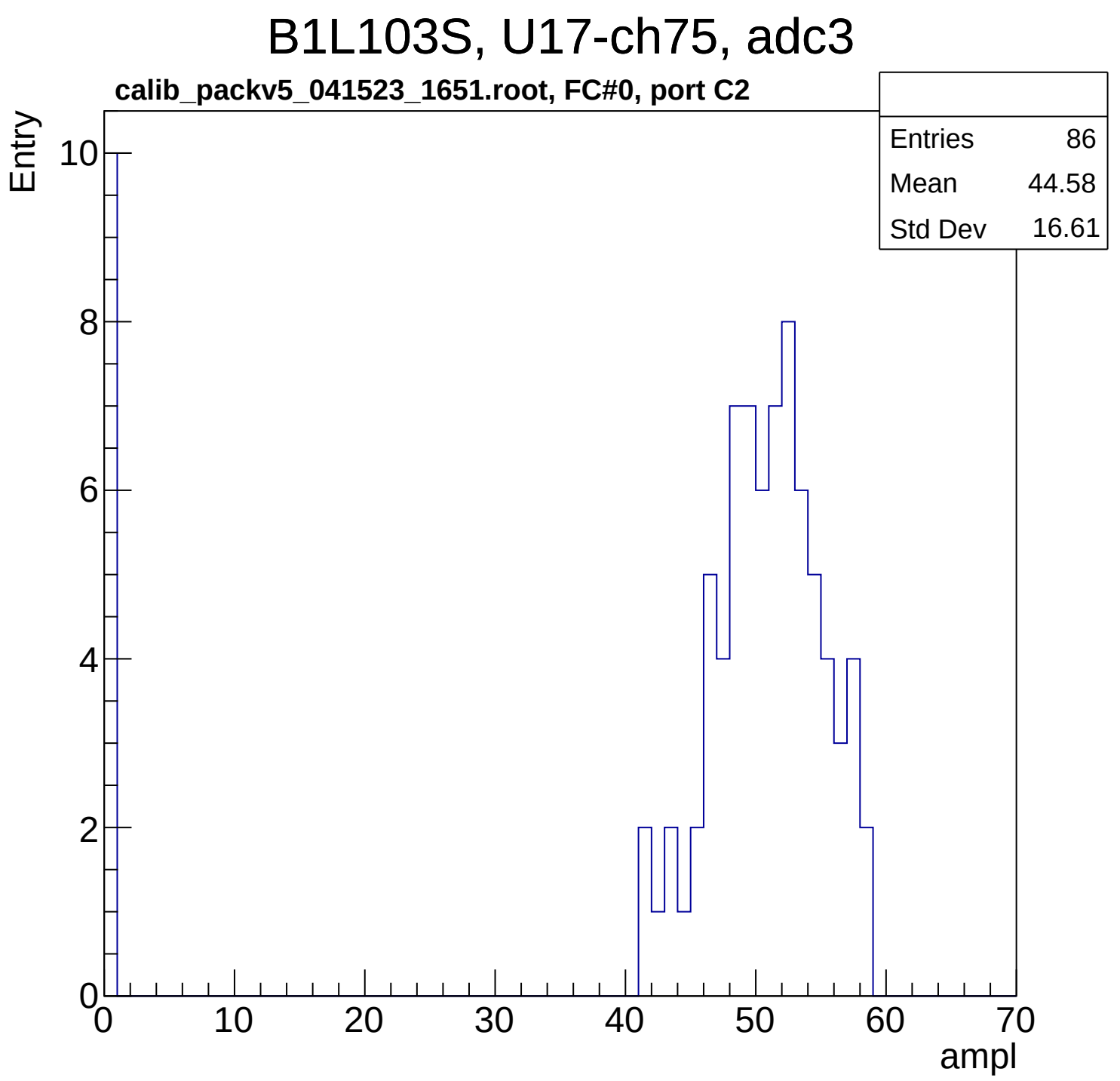
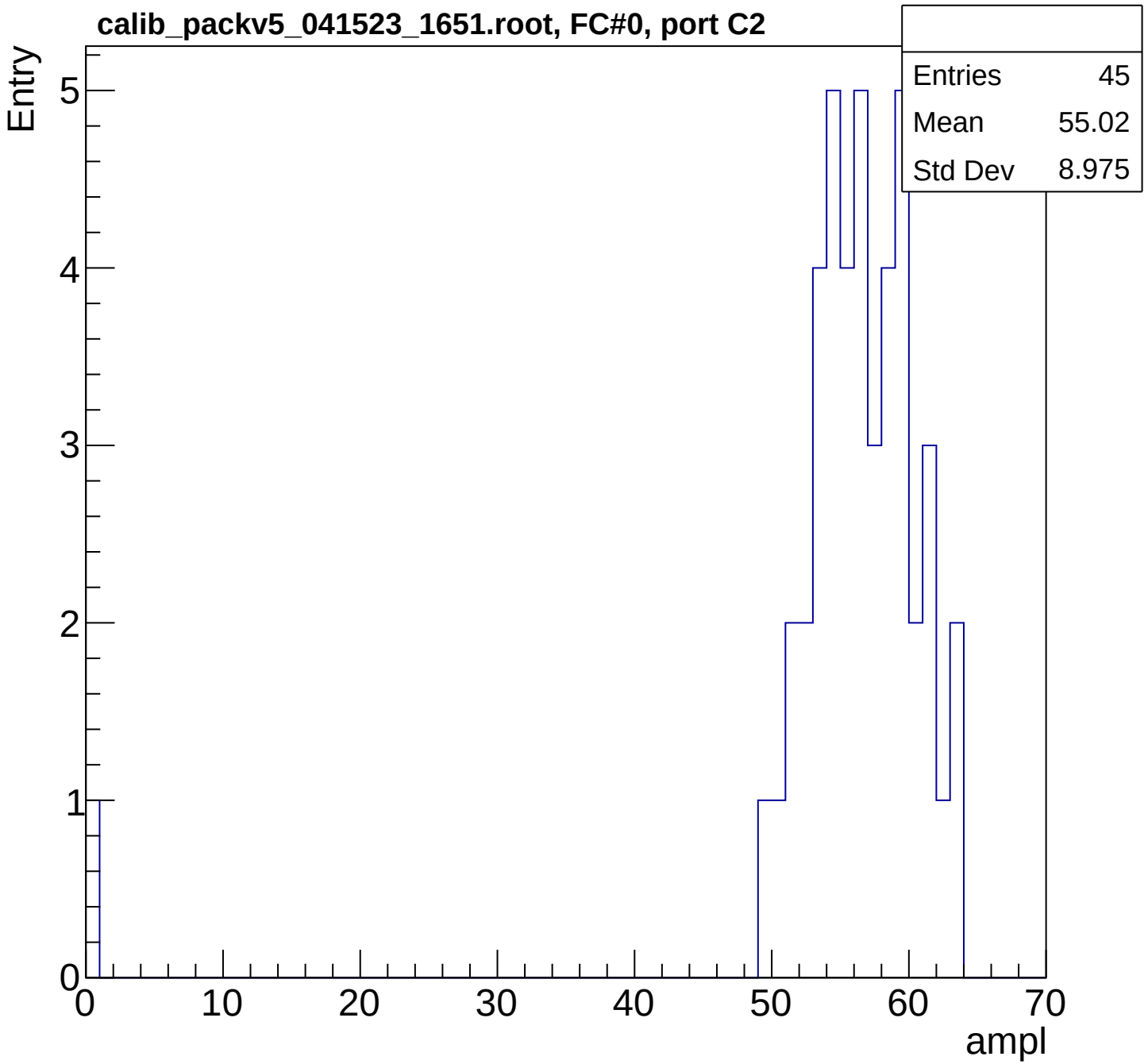
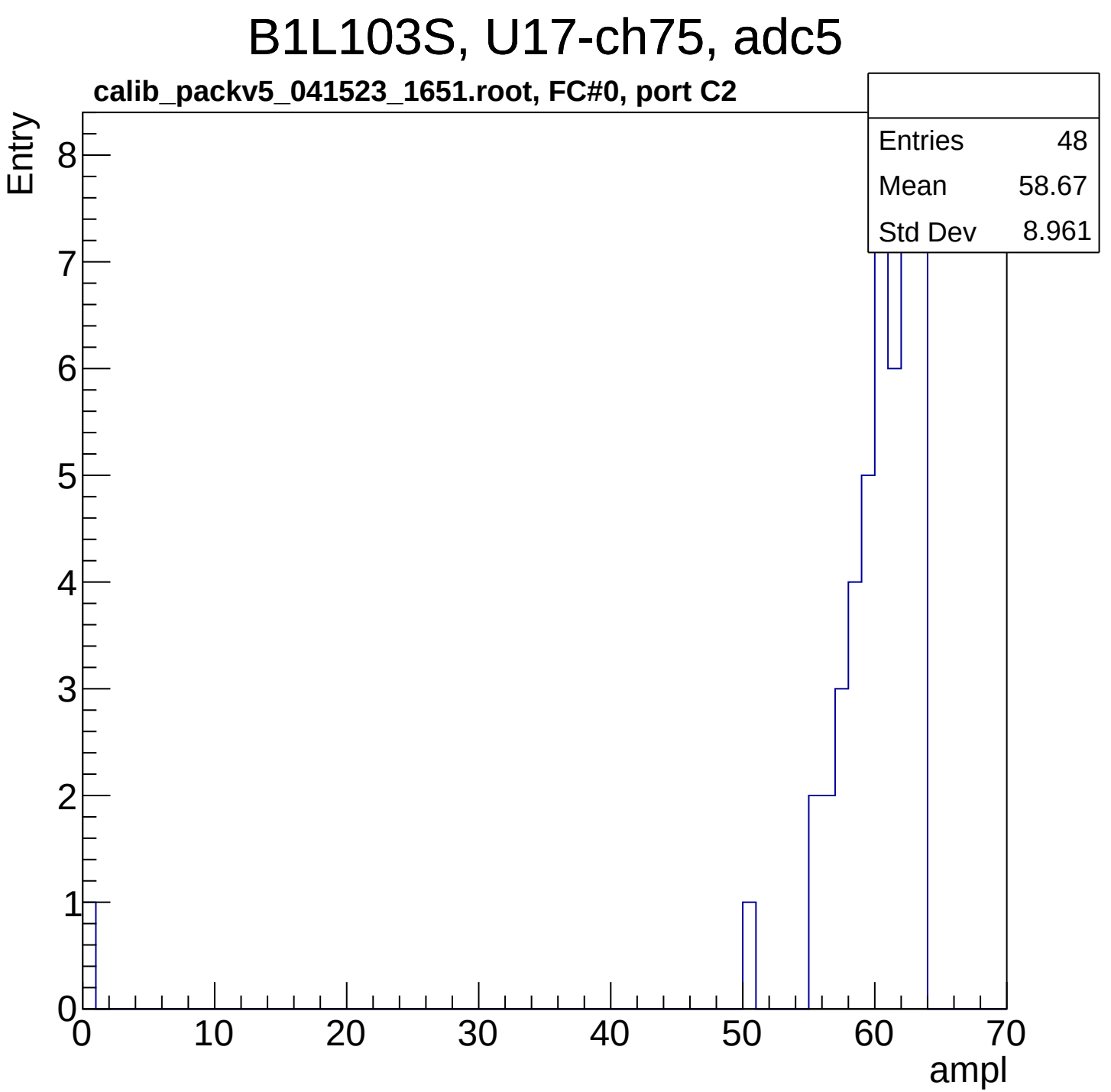

B1L103S, U17-ch75, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 44.58
Std Dev 16.61
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U17-ch75, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 55.02
Std Dev 8.975
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U17-ch75, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 58.67
Std Dev 8.961
Entry
ampl
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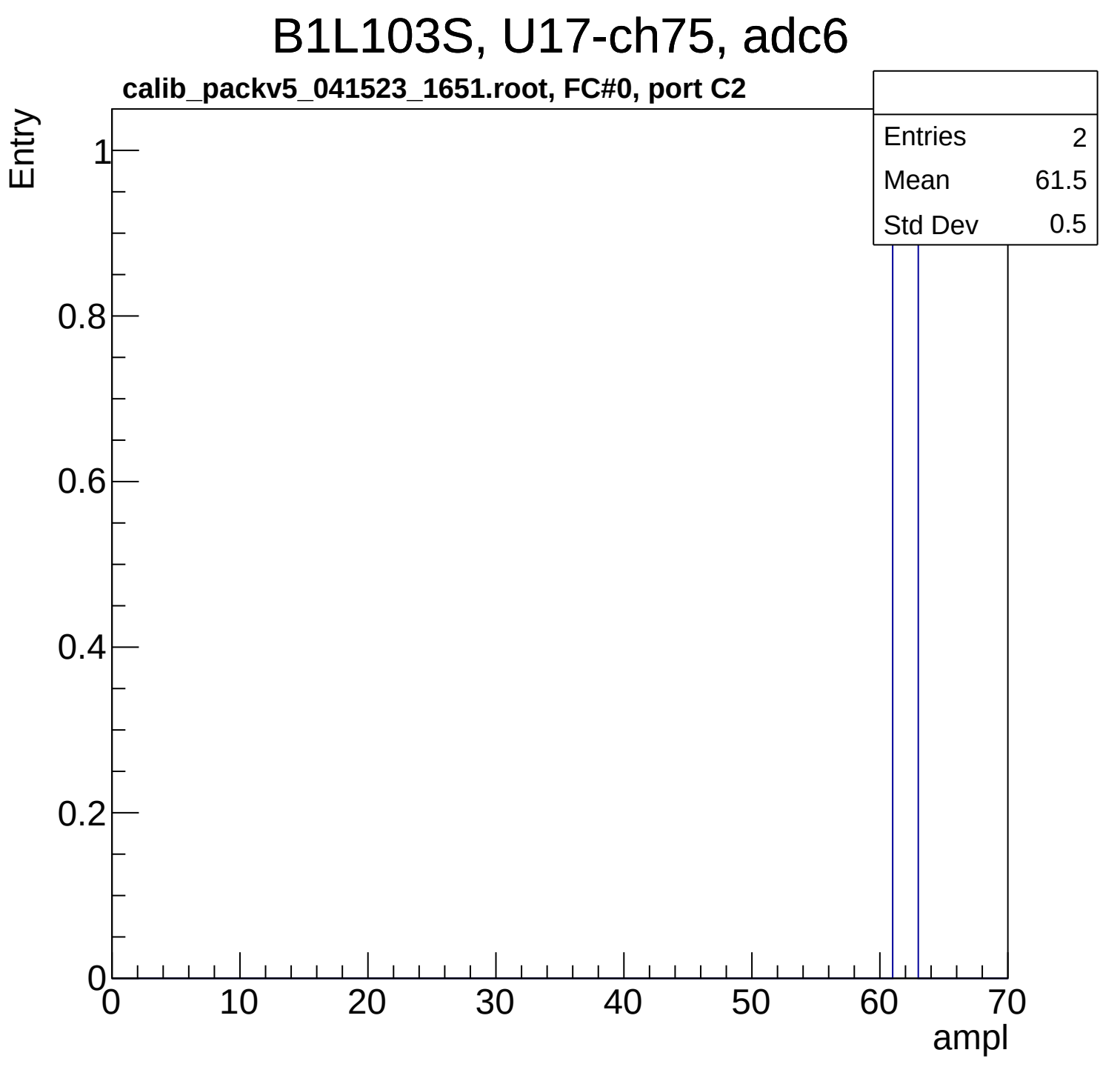
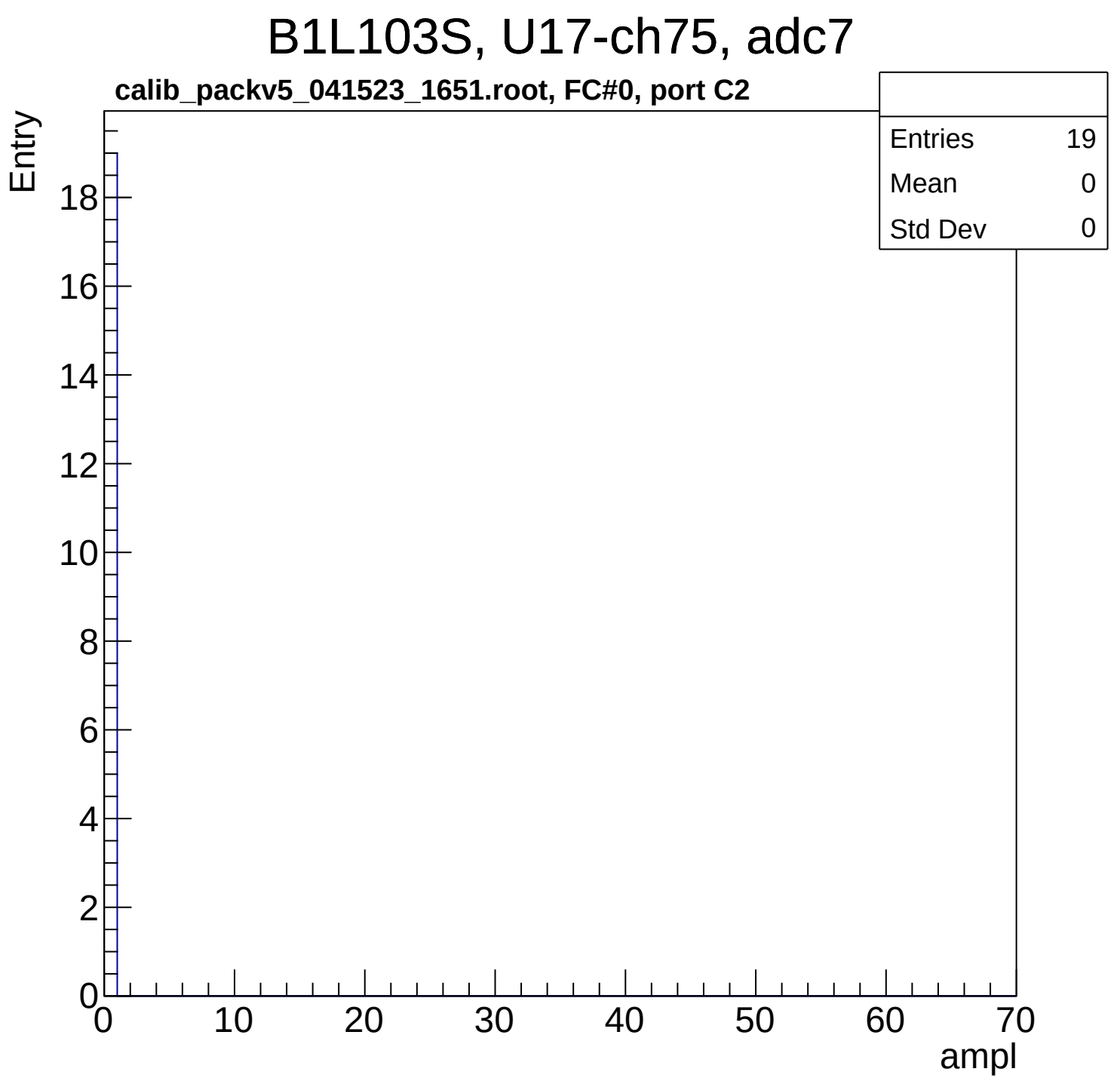
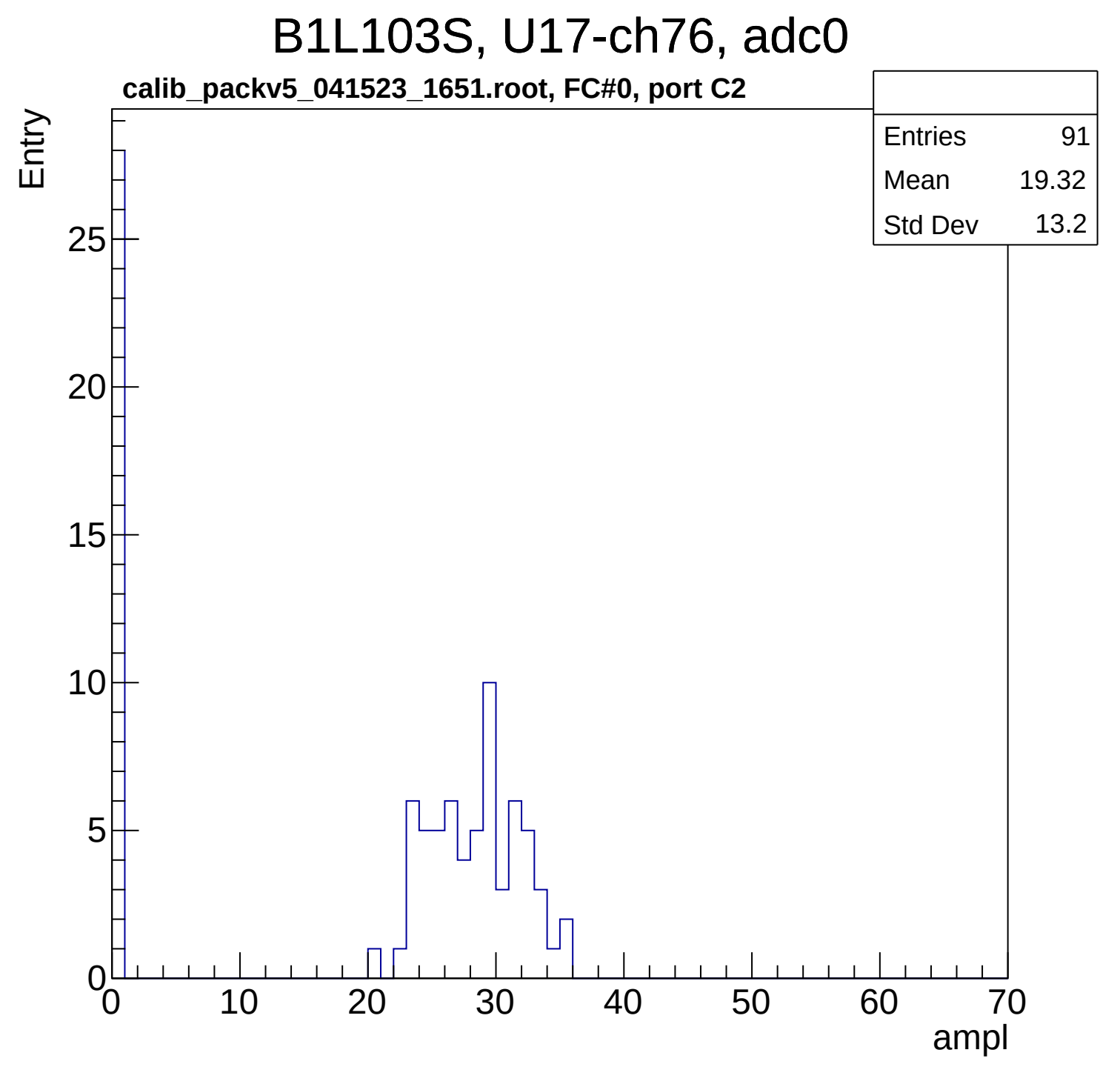
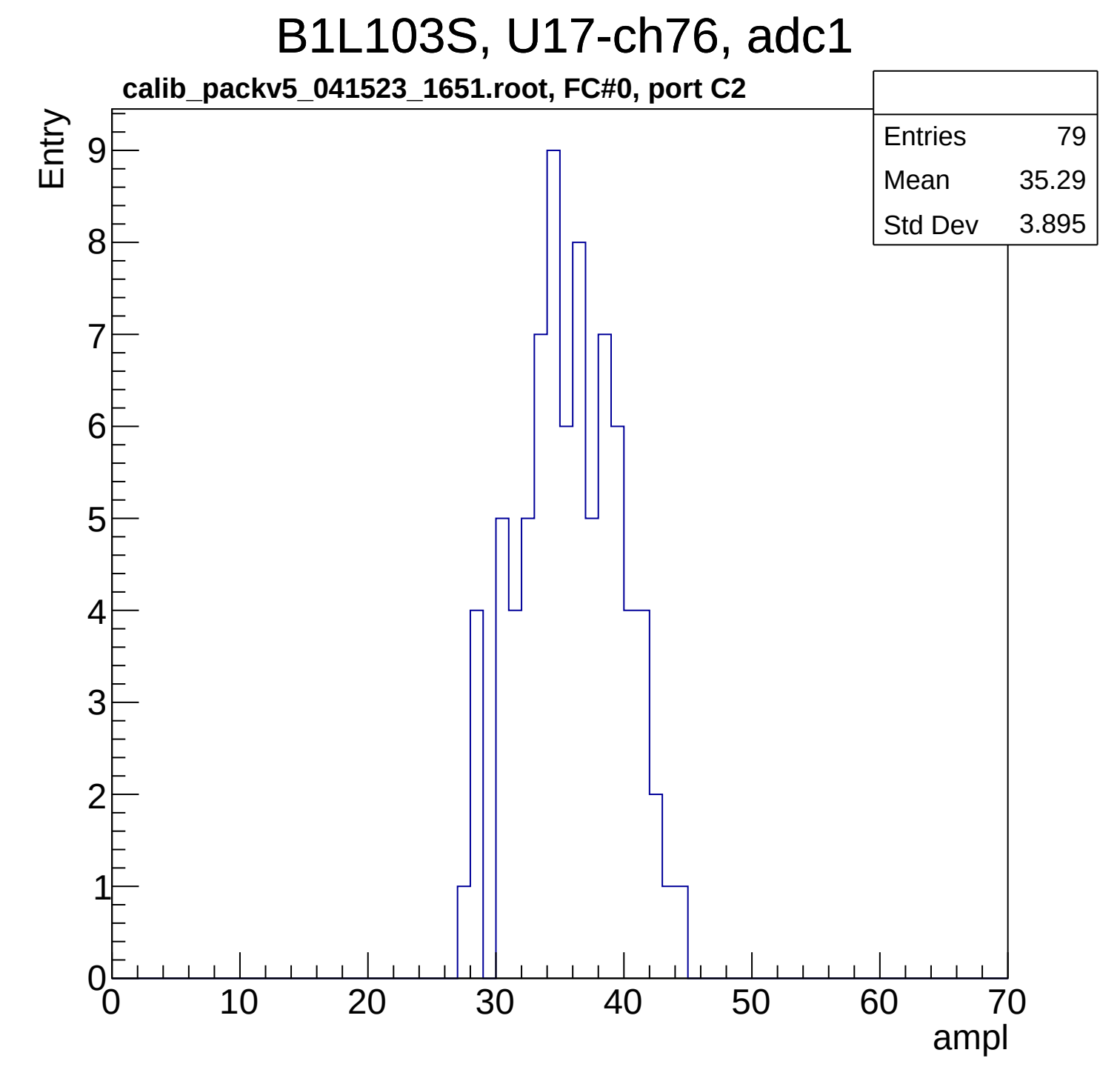
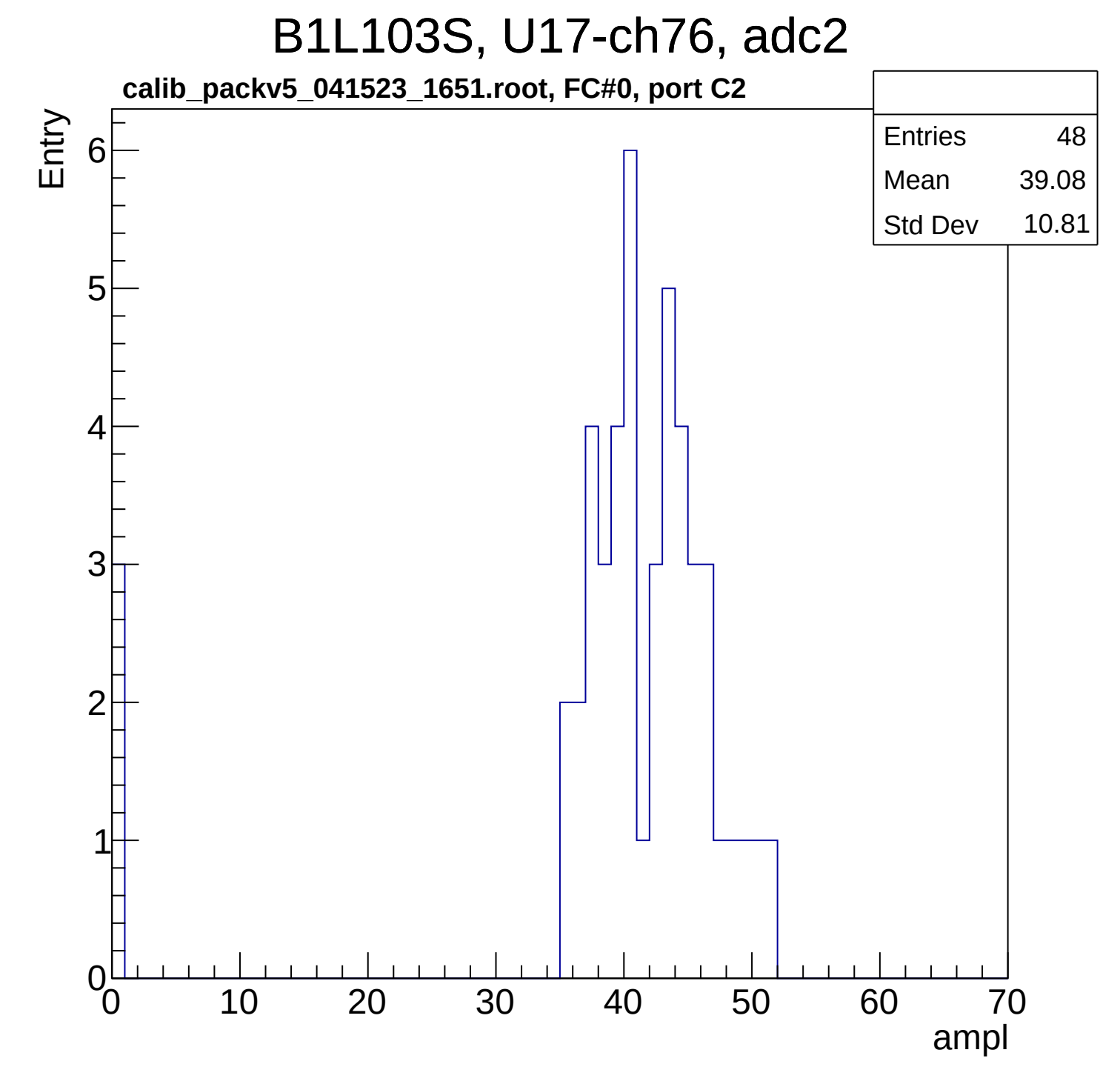
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

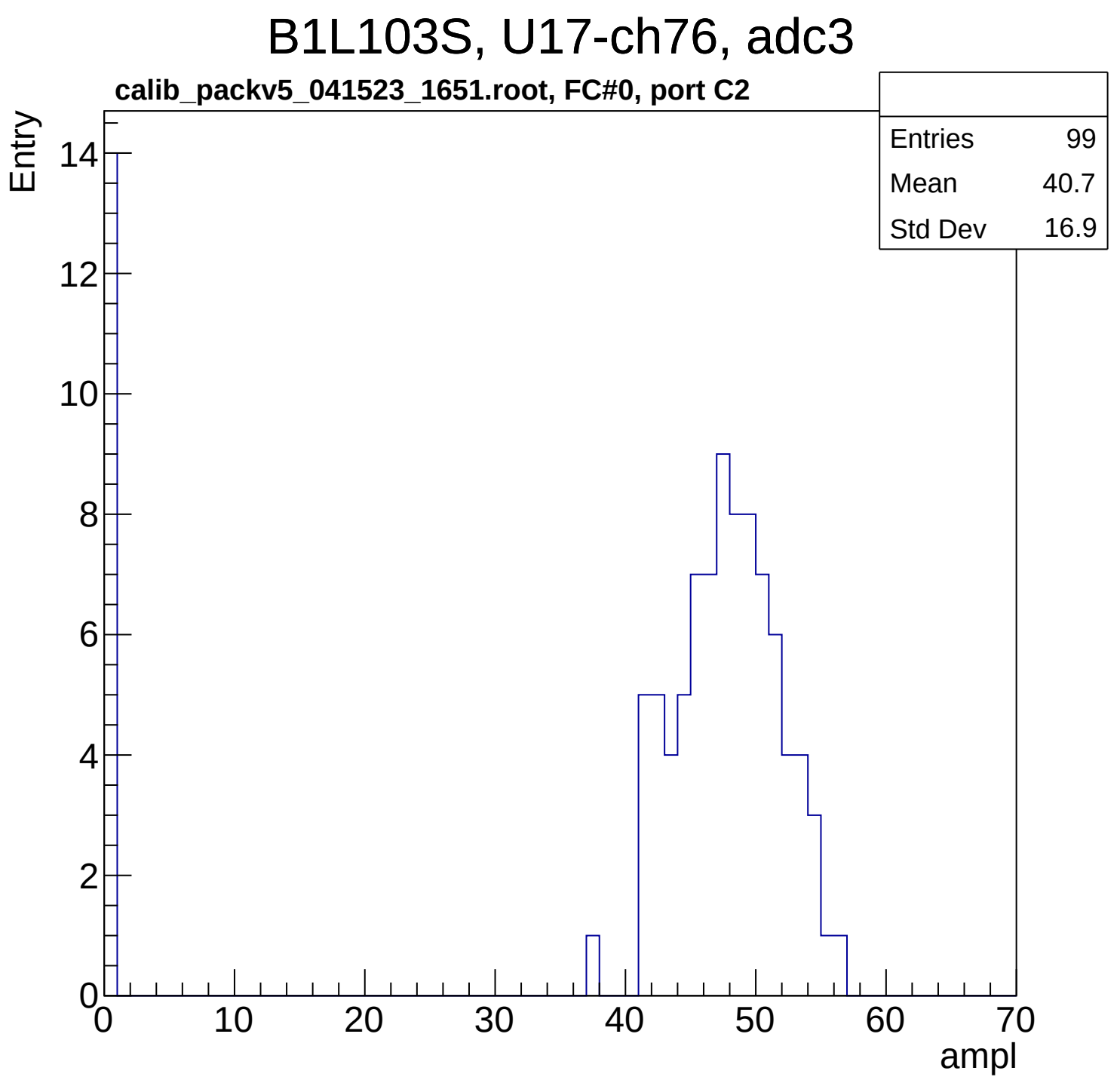

B1L103S, U17-ch75, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 2
Mean 61.5
Std Dev 0.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

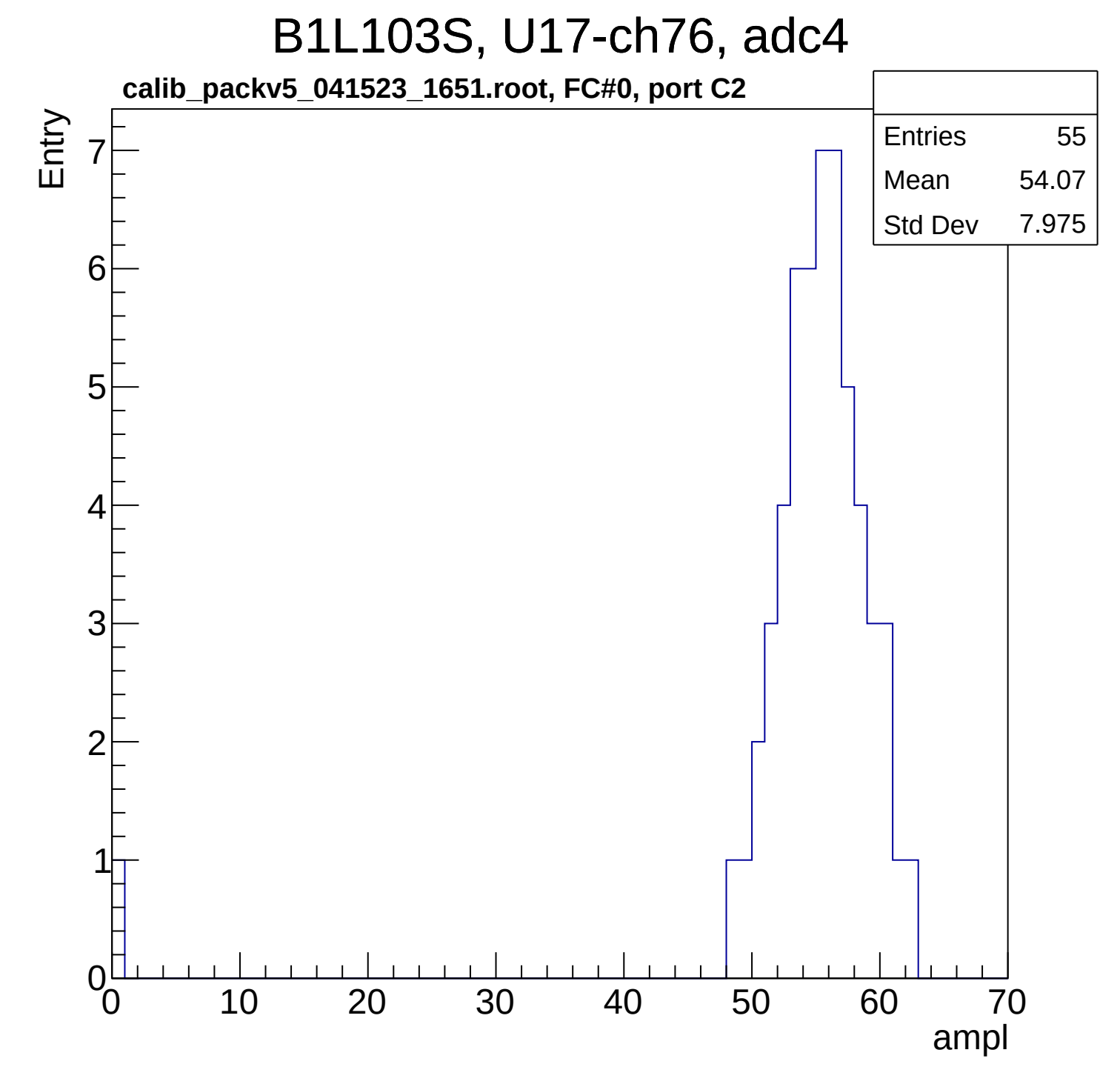

B1L103S, U17-ch75, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

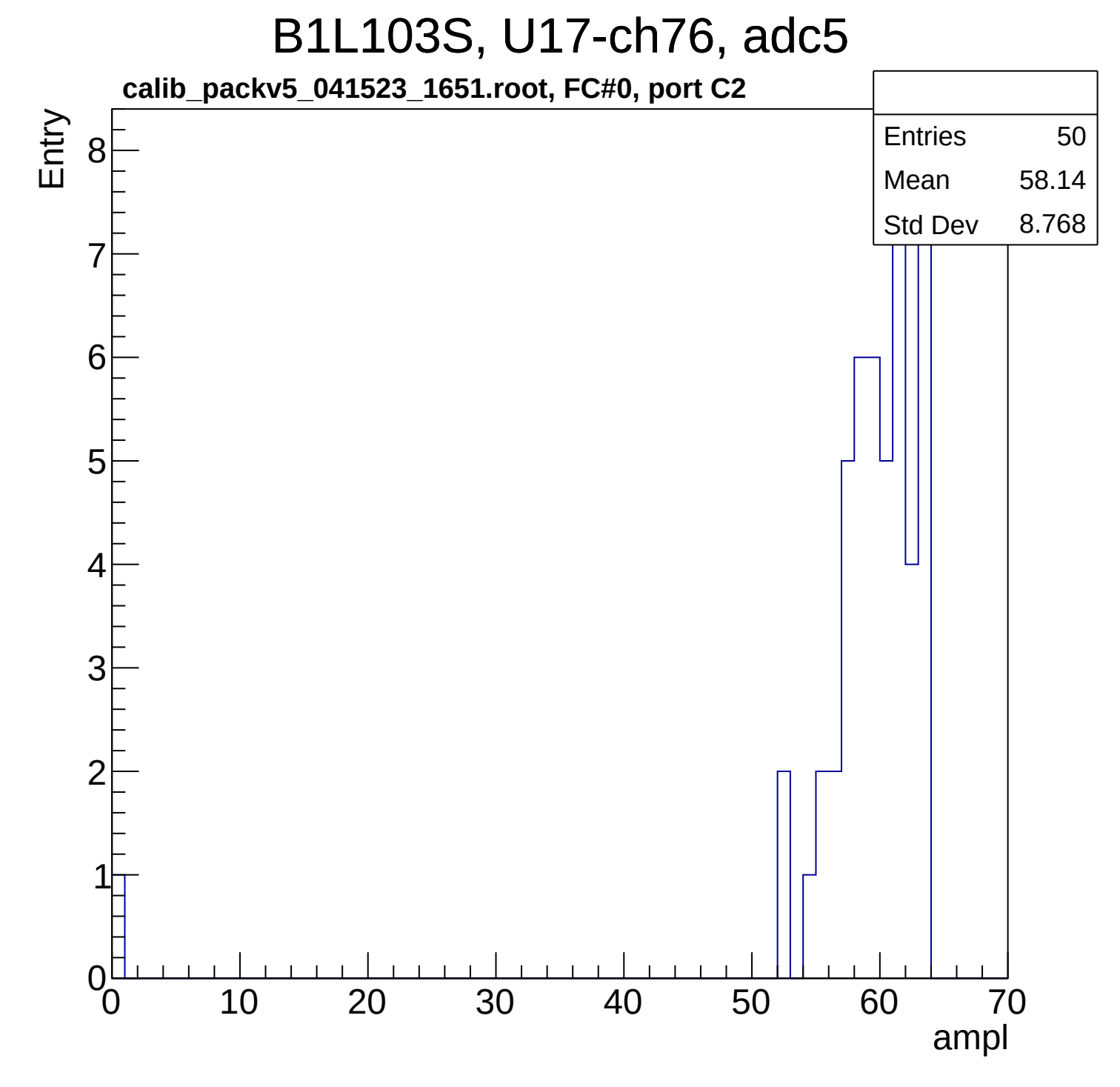

B1L103S, U17-ch76, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 91
Mean 19.32
Std Dev 13.2
Entry
0
5
10
15
20
25
0
10
20
30
40
50
60
70
ampl

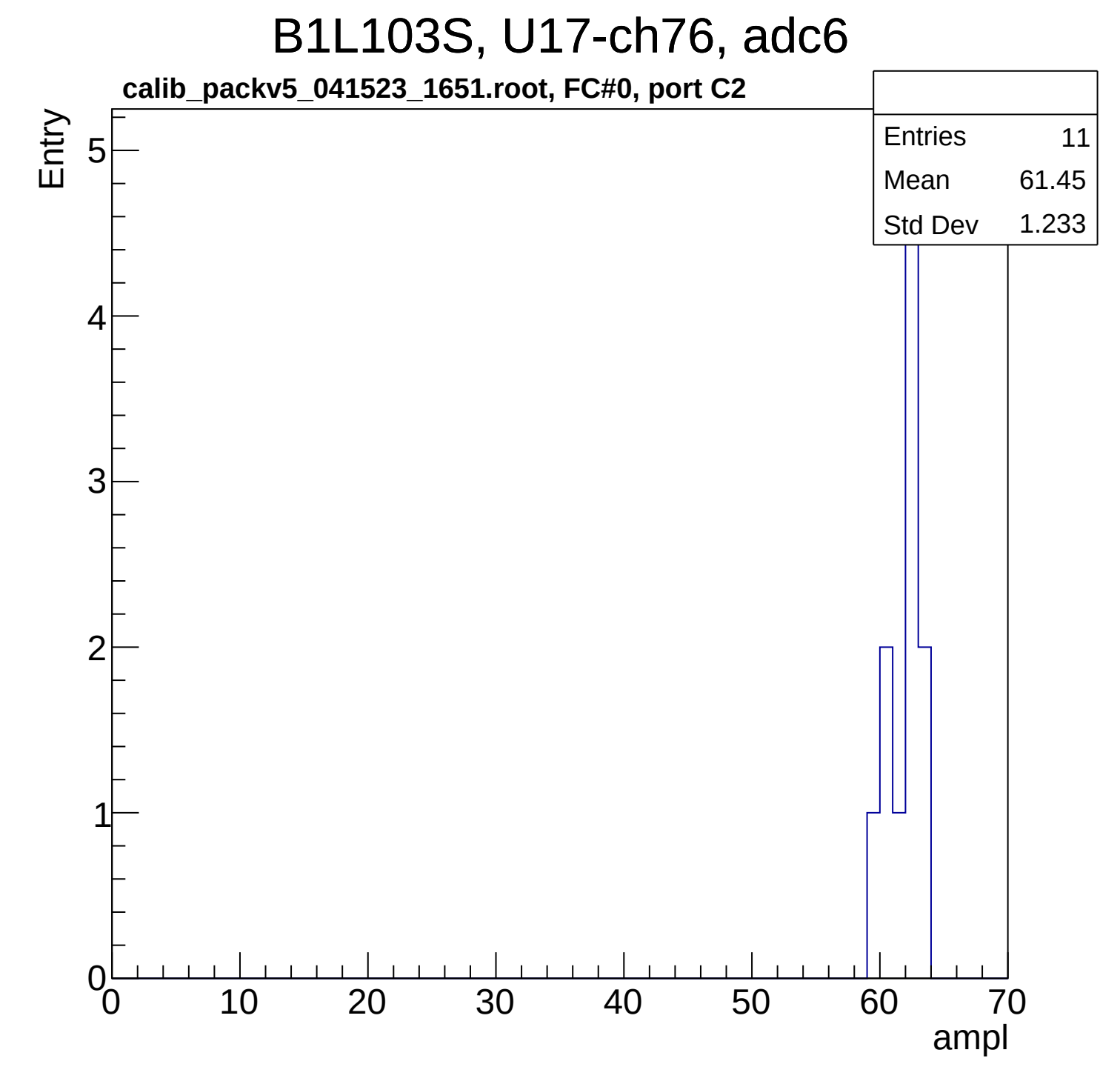

B1L103S, U17-ch76, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 35.29
Std Dev 3.895
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

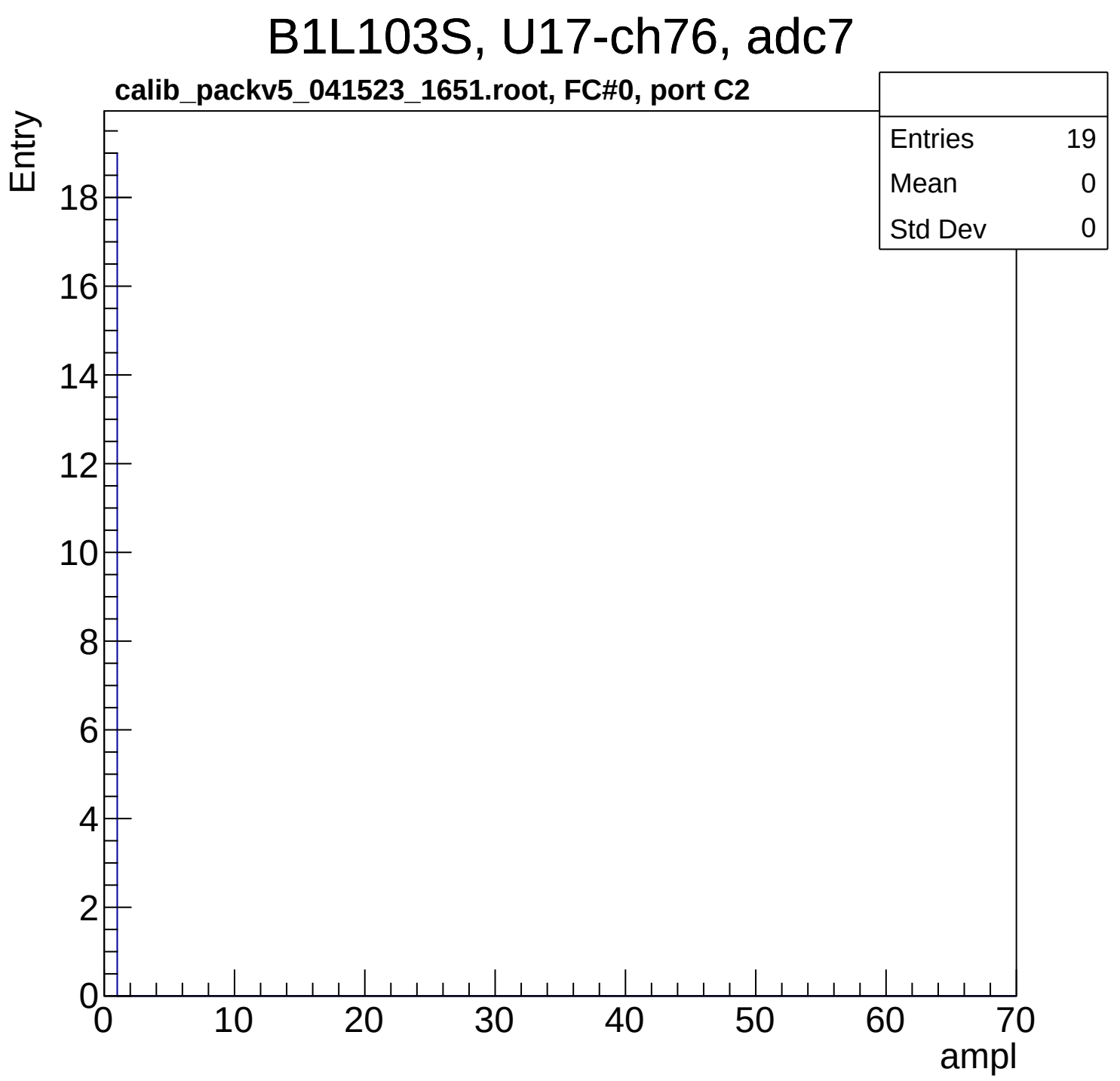

B1L103S, U17-ch76, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 39.08
Std Dev 10.81
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

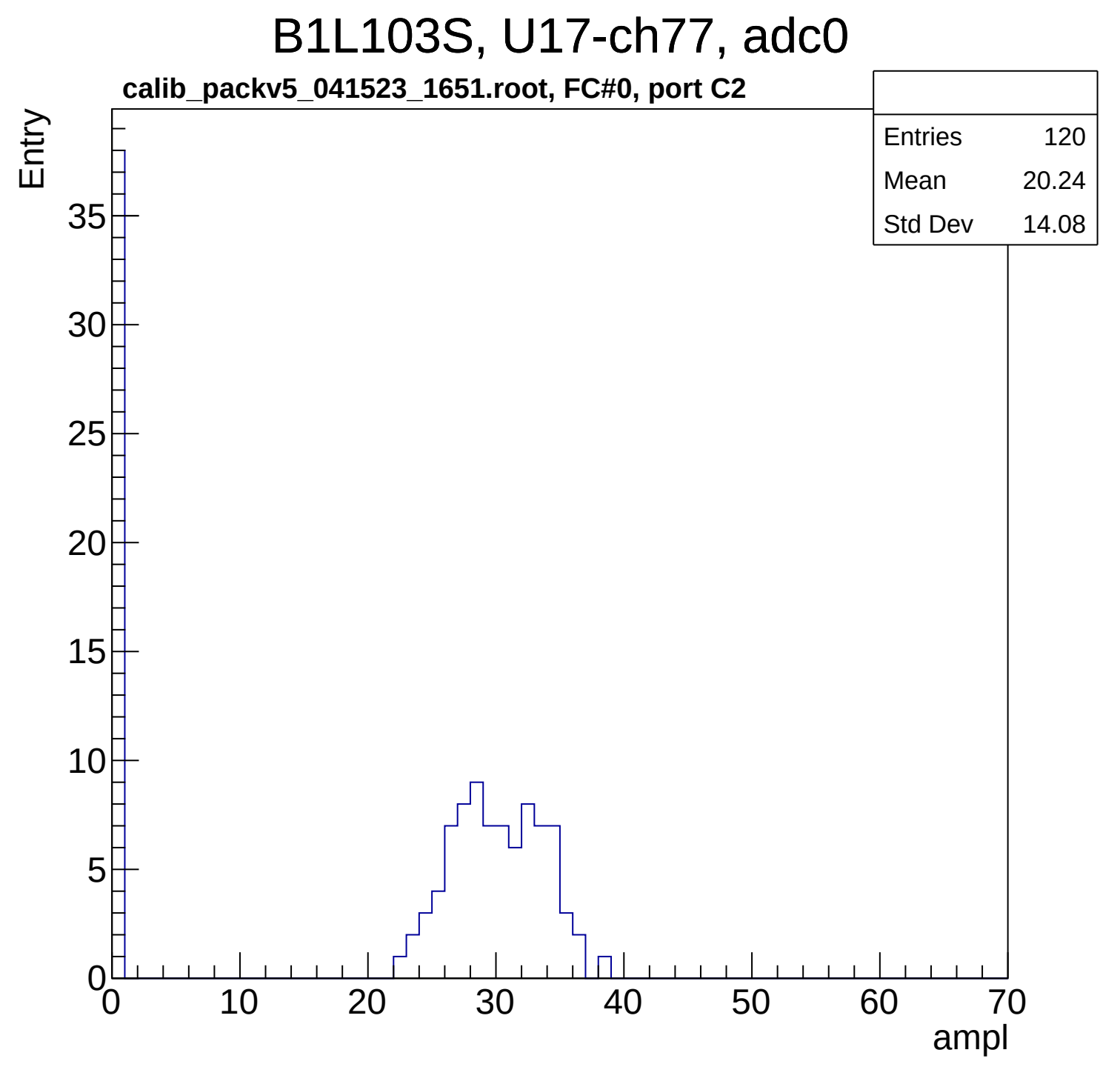

B1L103S, U17-ch76, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 99
Mean 40.7
Std Dev 16.9
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

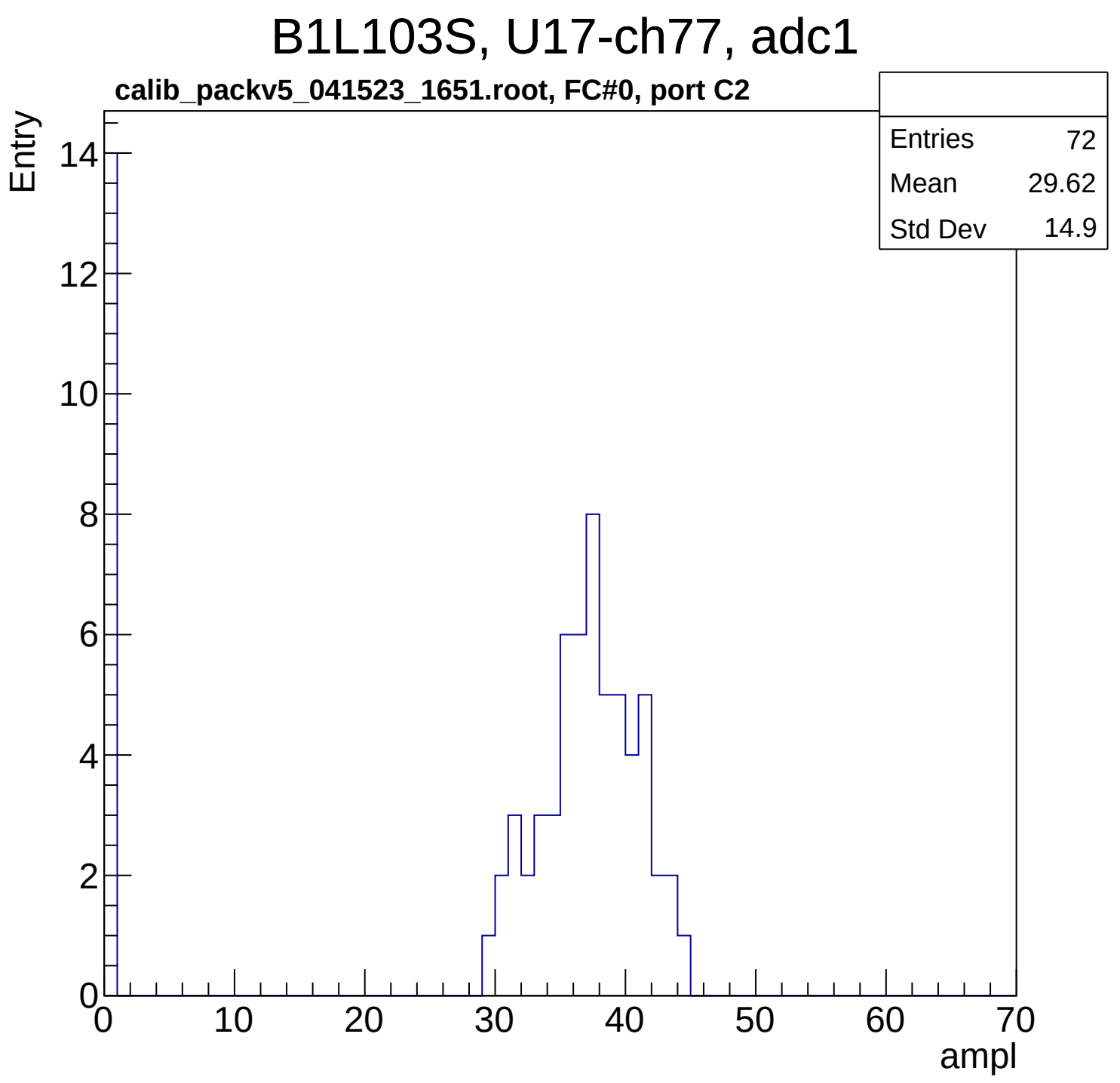

B1L103S, U17-ch76, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 54.07
Std Dev 7.975
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

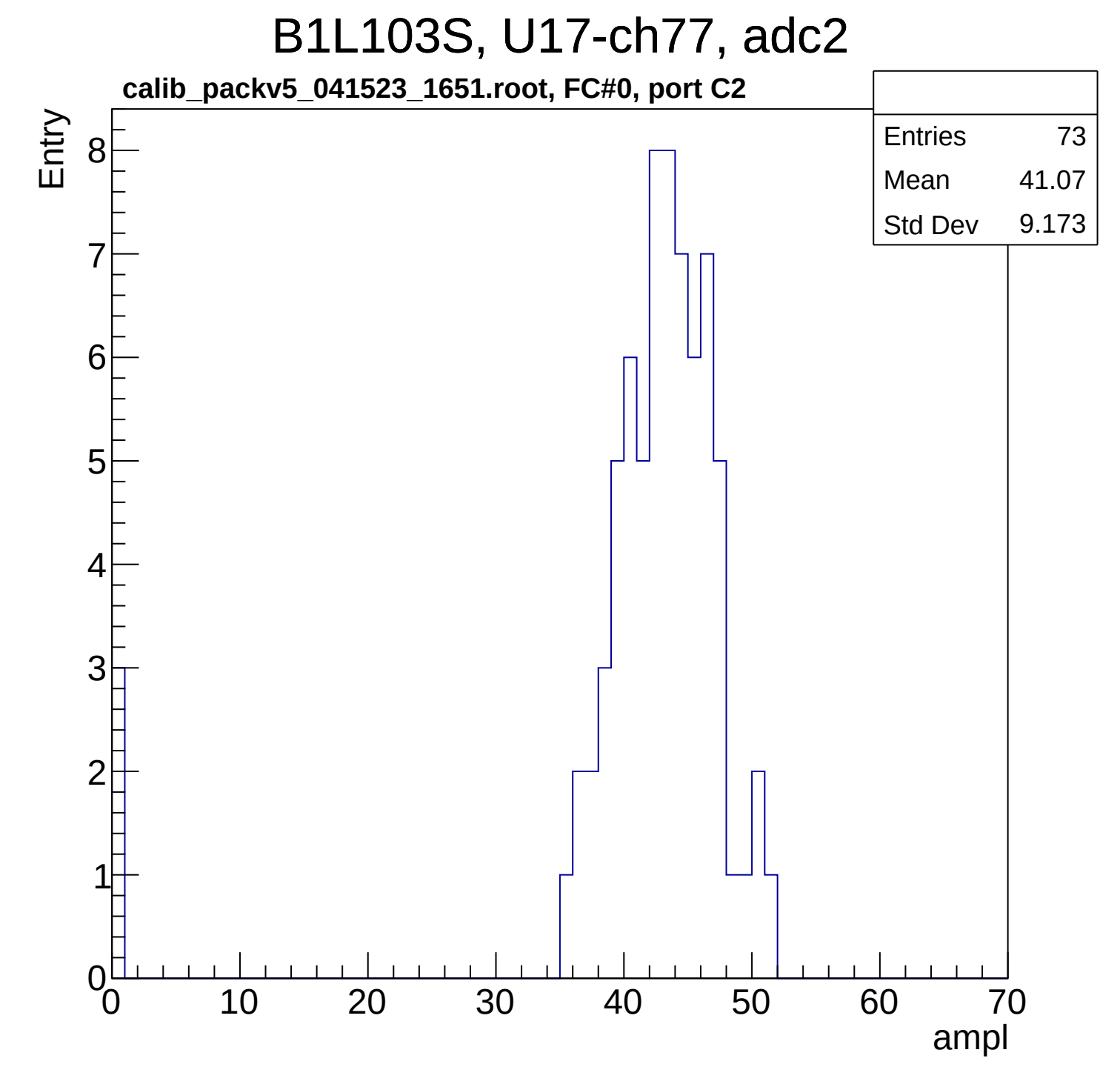

B1L103S, U17-ch76, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 58.14
Std Dev 8.768
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U17-ch76, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 61.45
Std Dev 1.233
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U17-ch76, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch77, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 120
Mean 20.24
Std Dev 14.08
Entry
0
5
10
15
20
25
30
35
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch77, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 29.62
Std Dev 14.9
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch77, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 41.07
Std Dev 9.173
Entry
ampl
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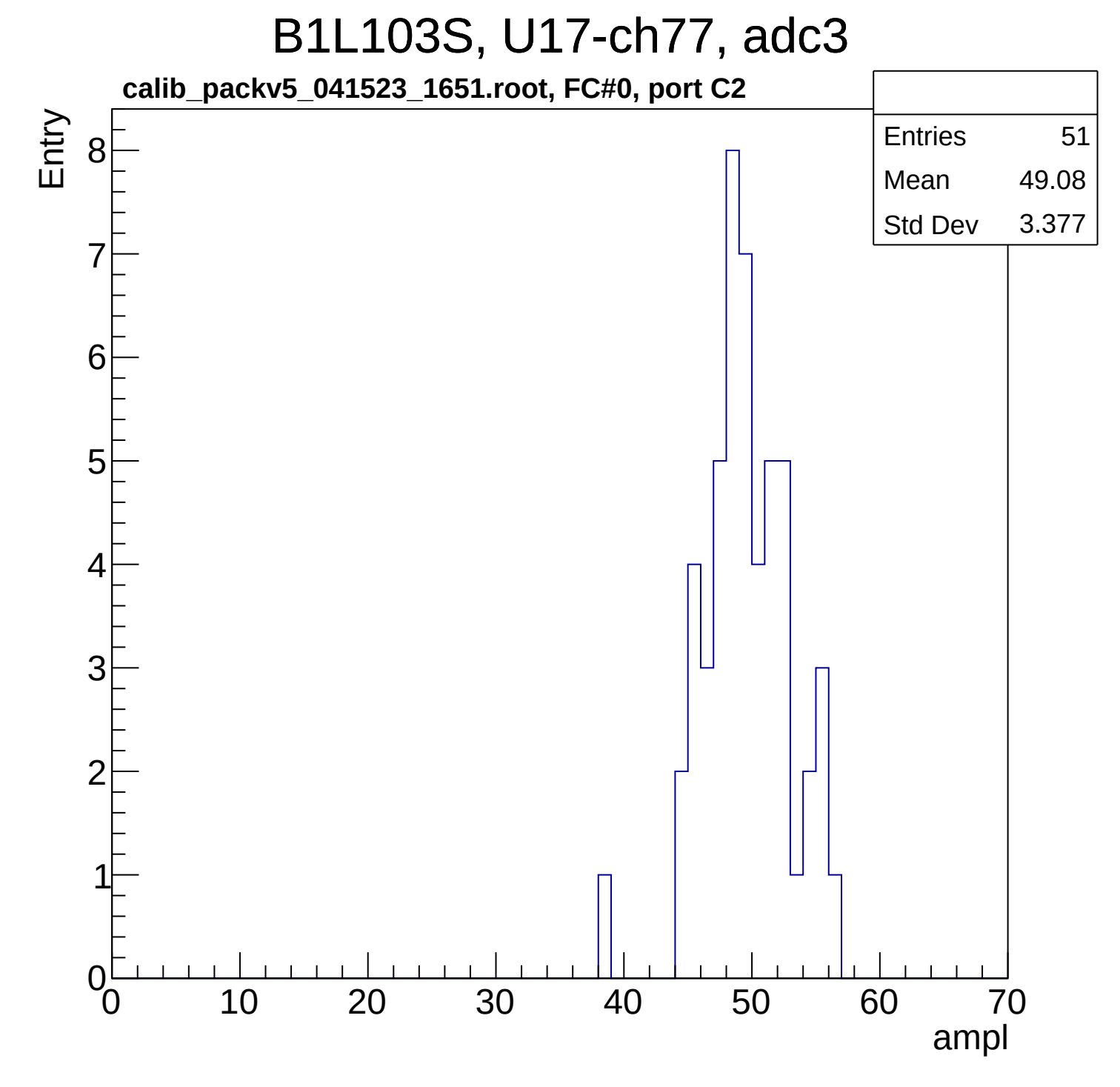
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U17-ch77, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 49.08
Std Dev 3.377
Entry
ampl
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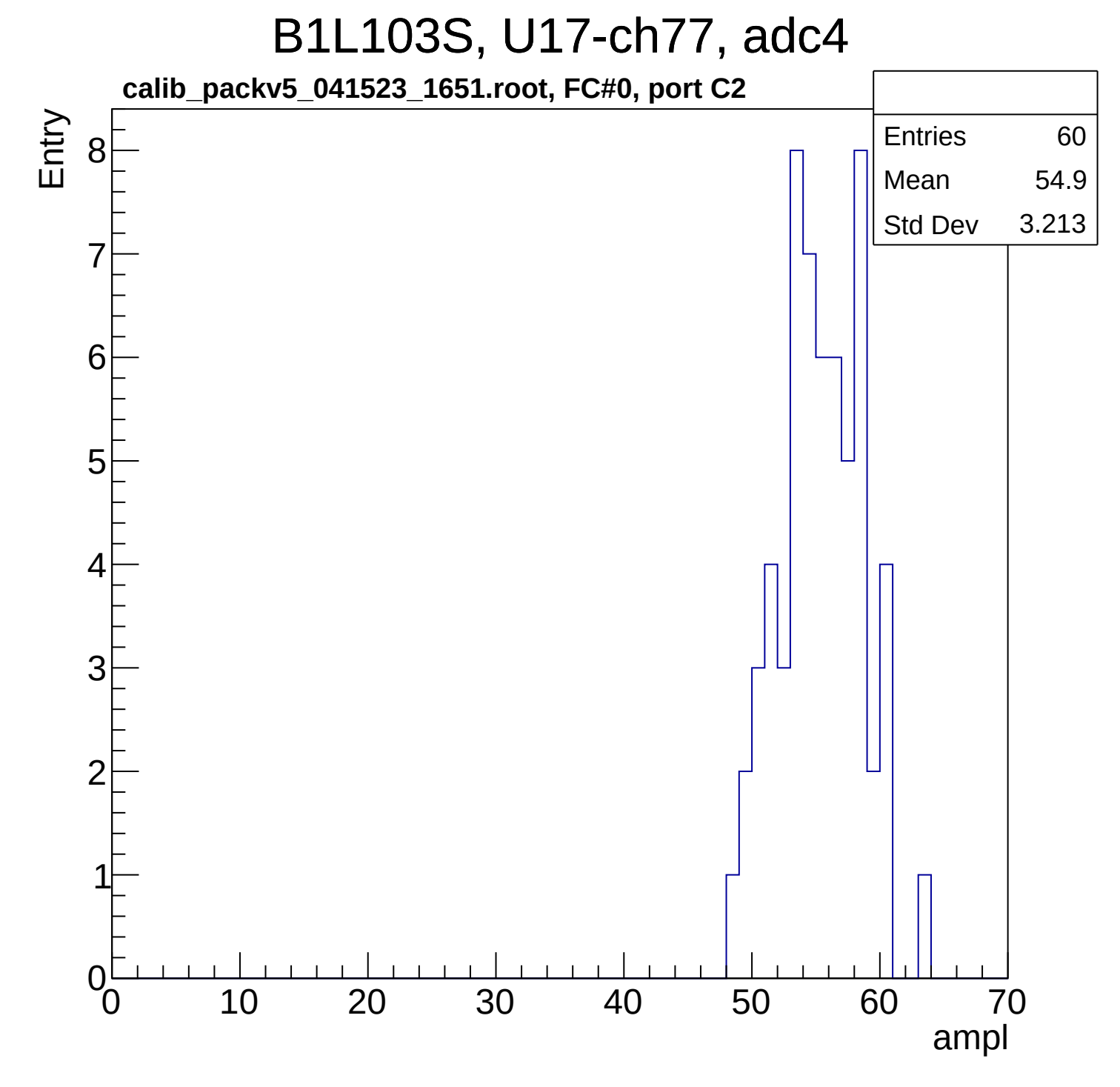
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U17-ch77, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 54.9
Std Dev 3.213
Entry
ampl
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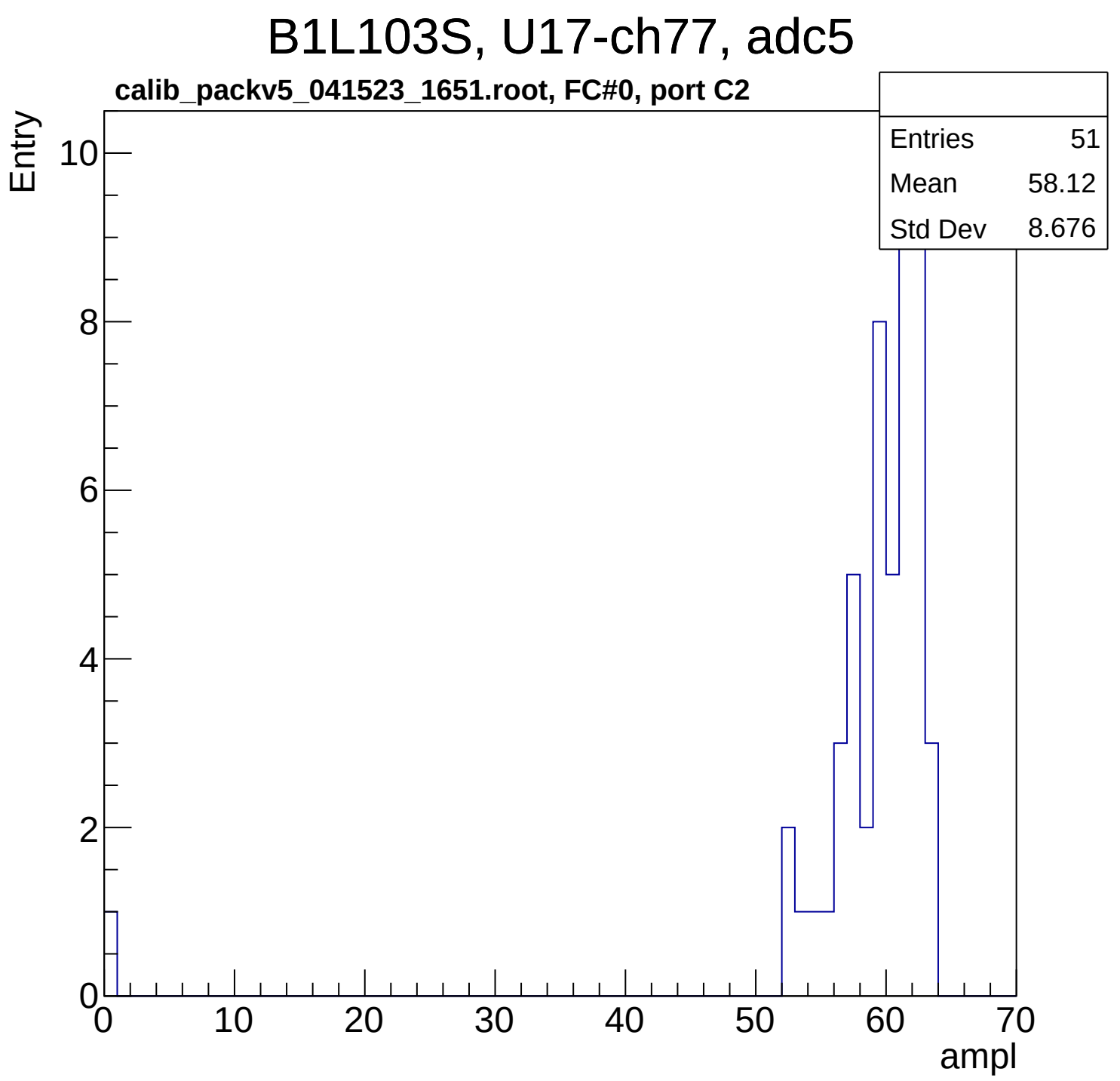
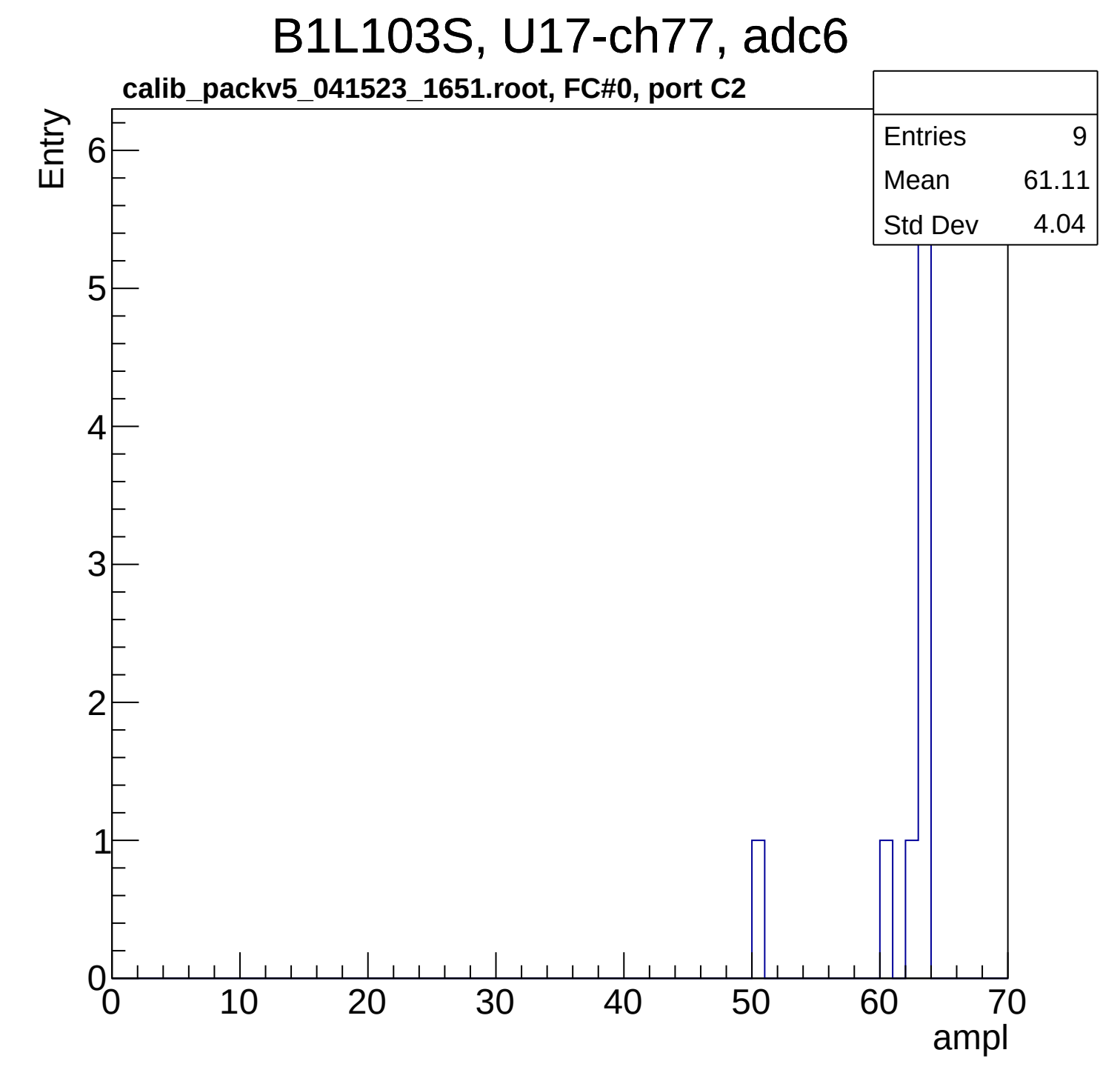
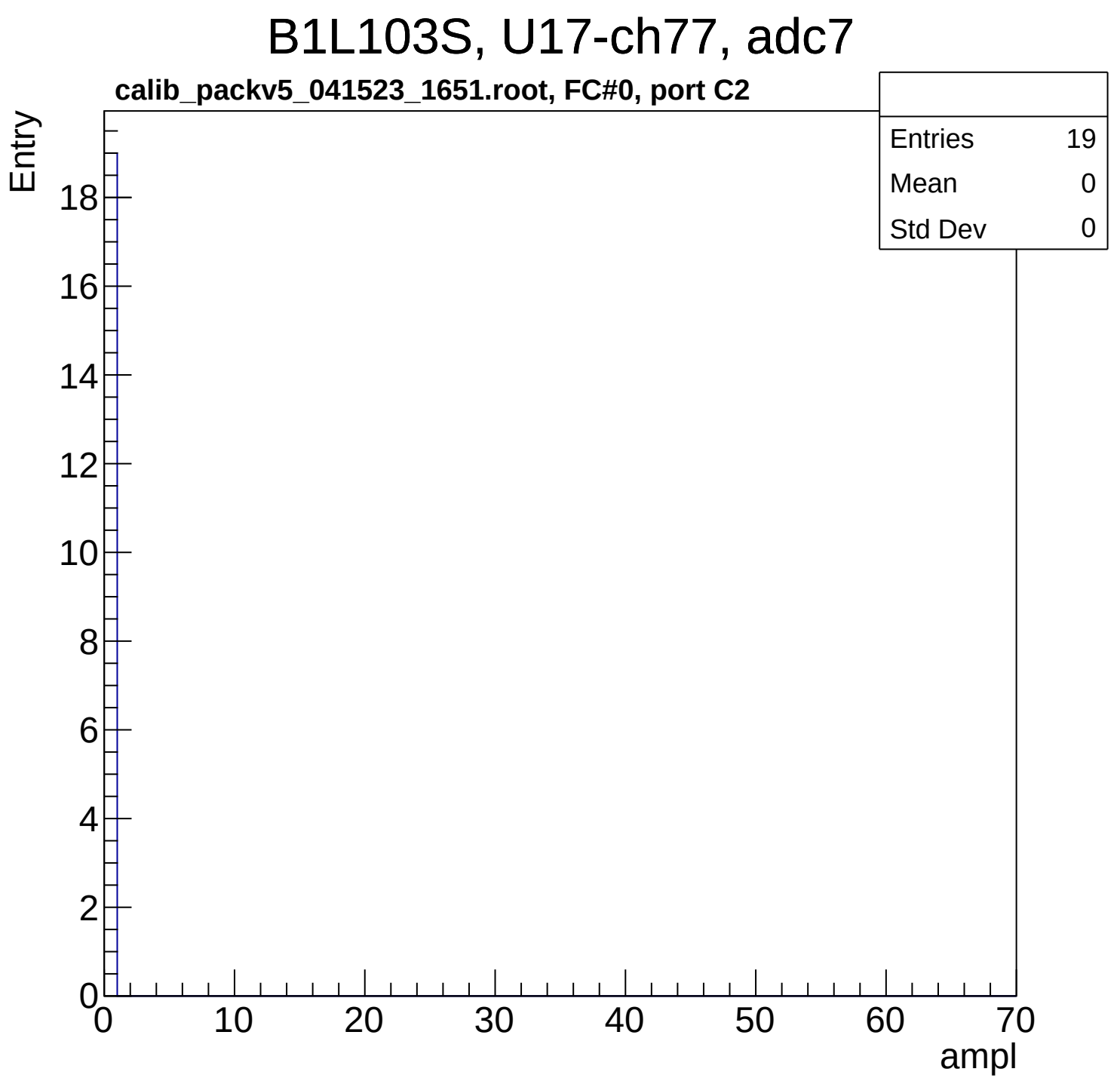
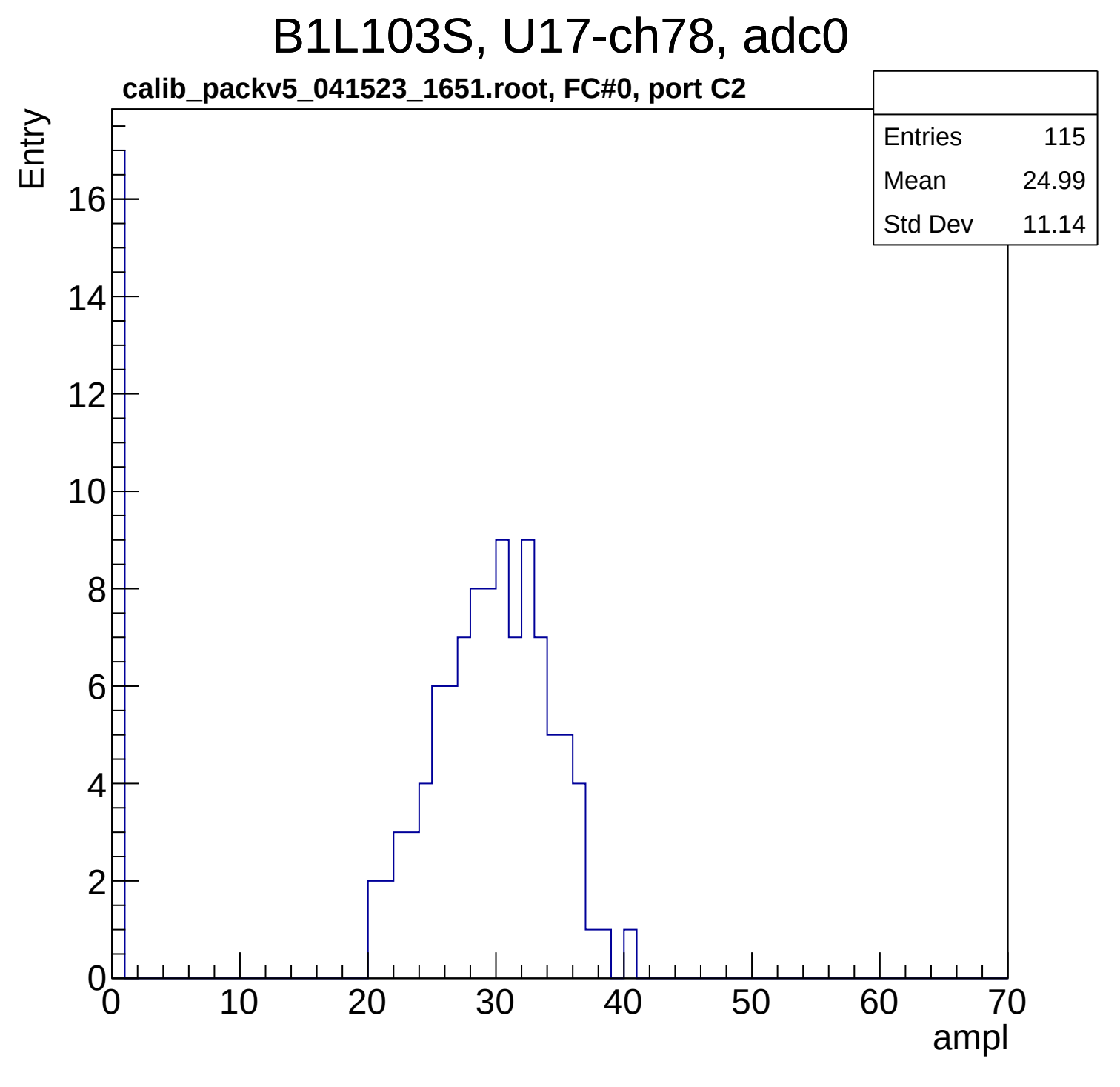
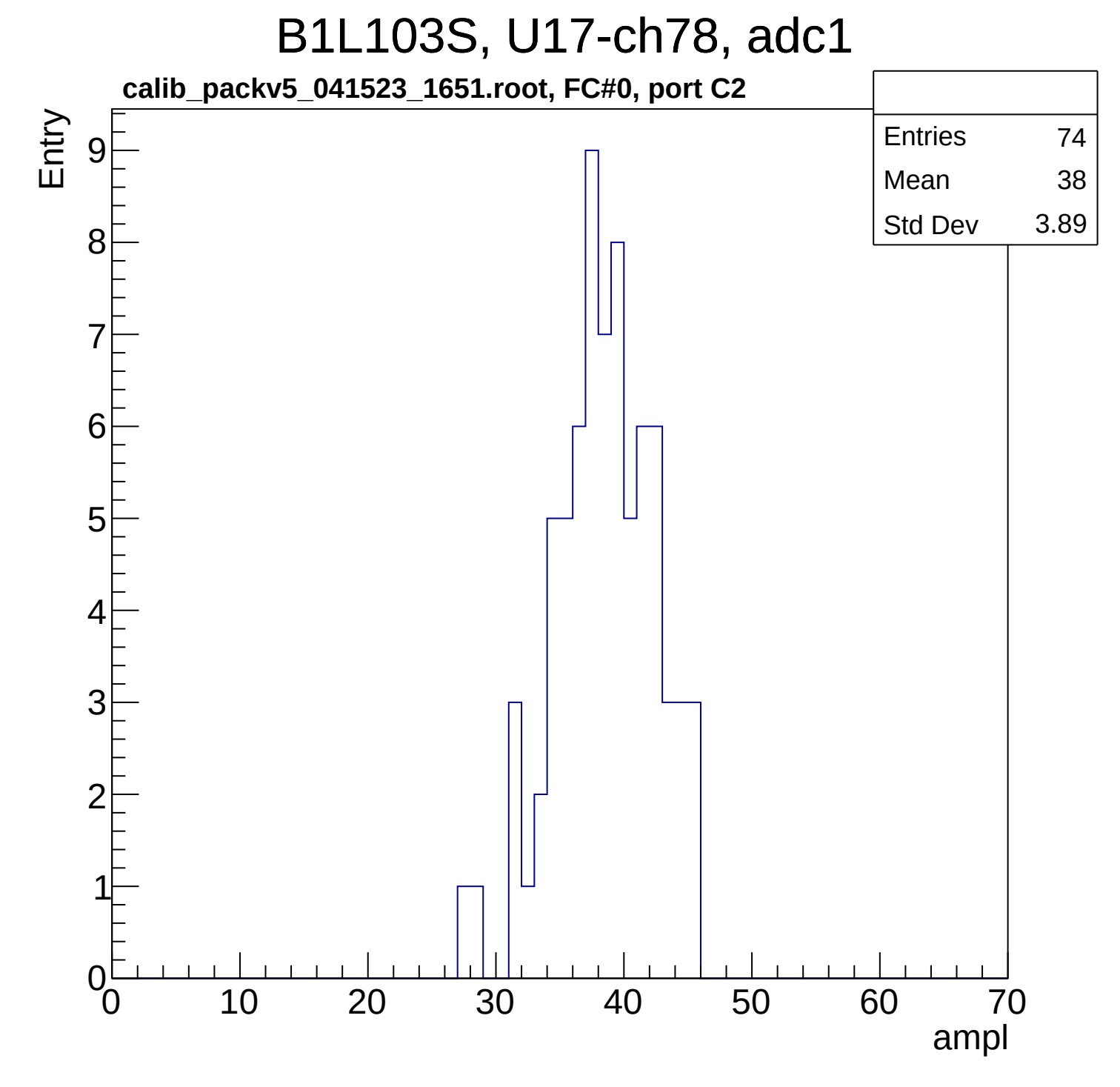
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U17-ch77, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 58.12
Std Dev 8.676
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U17-ch77, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 9
Mean 61.11
Std Dev 4.04
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U17-ch77, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch78, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 115
Mean 24.99
Std Dev 11.14
Entry
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch78, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 38
Std Dev 3.89
Entry
ampl
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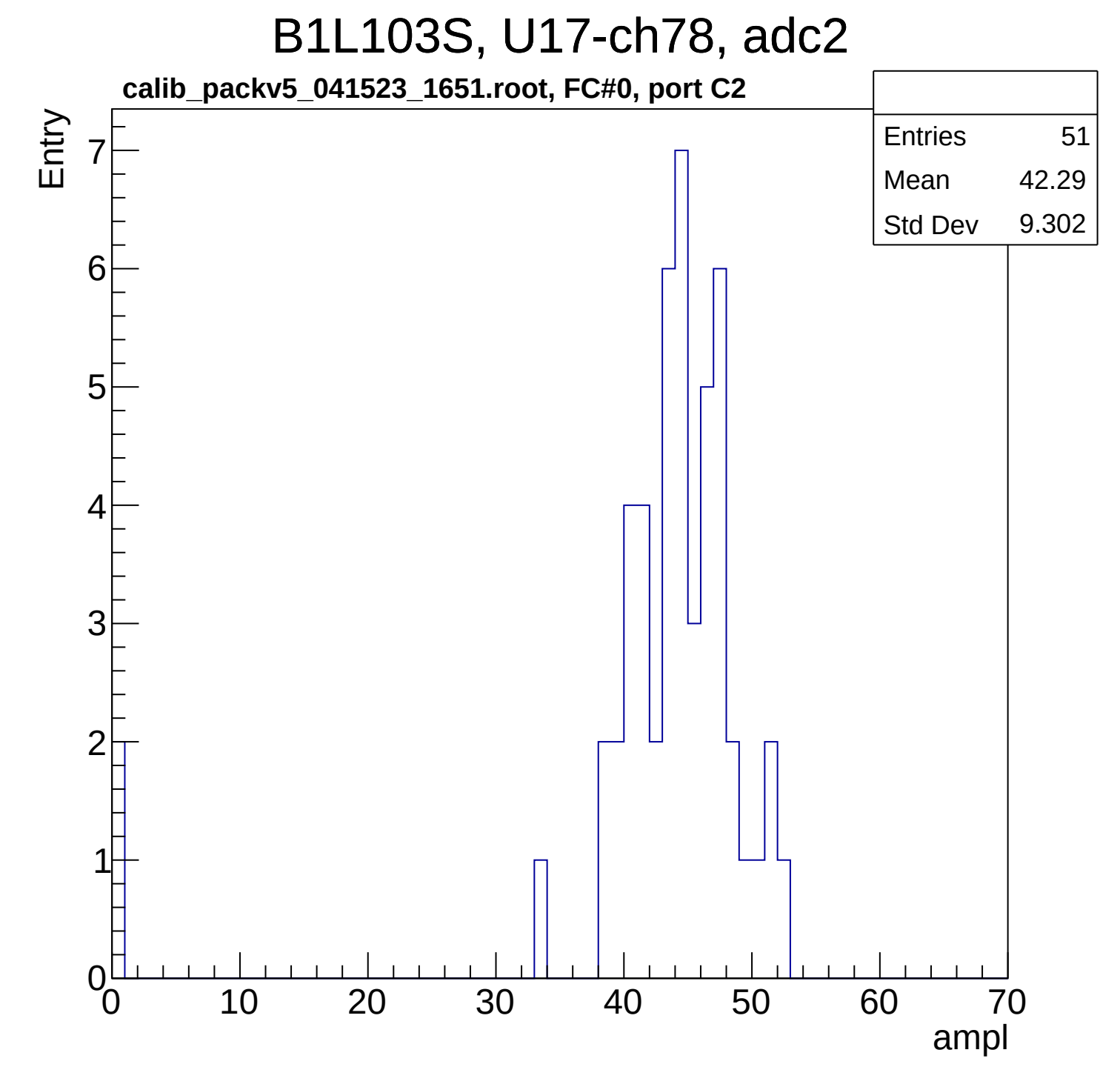
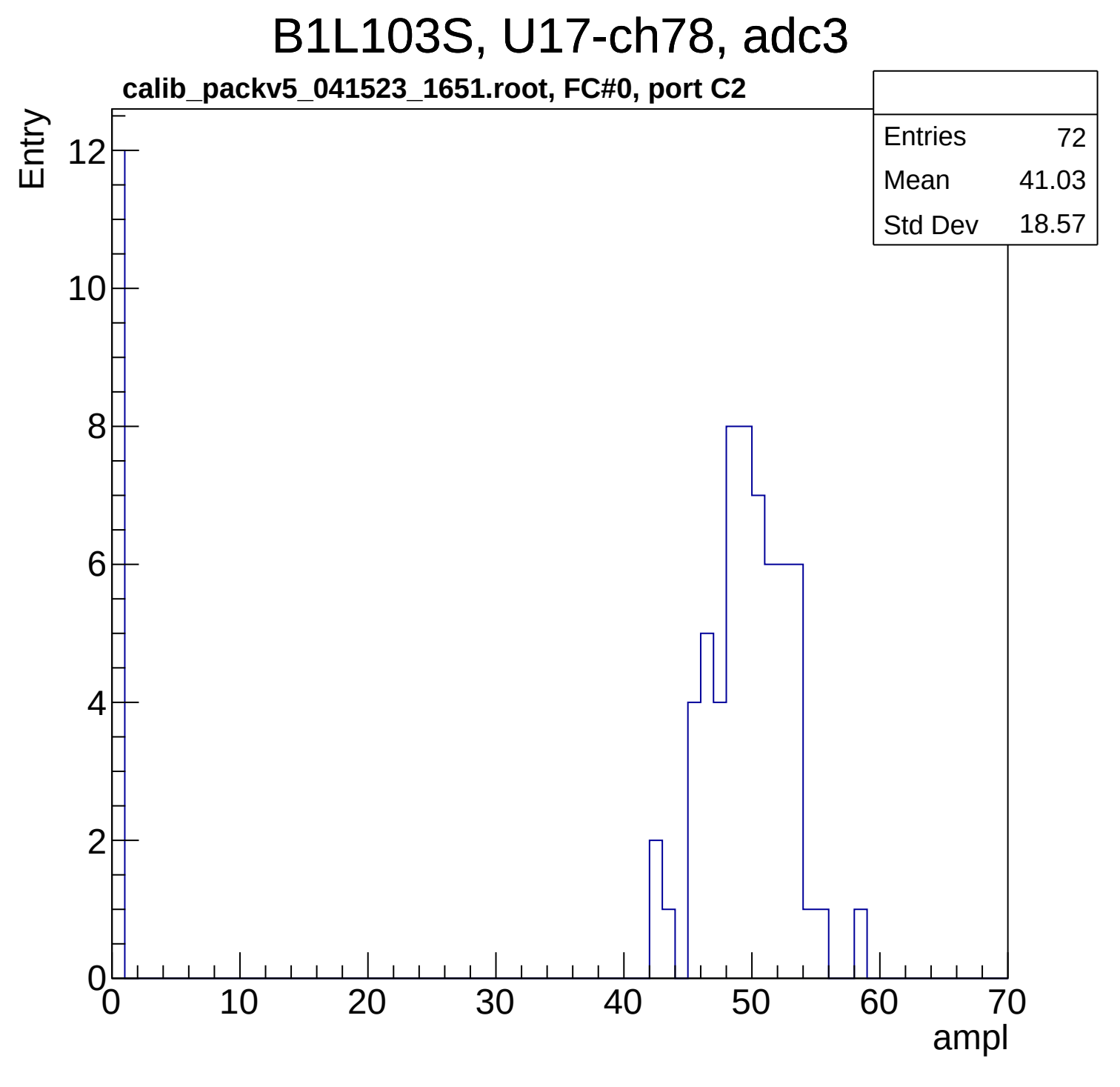
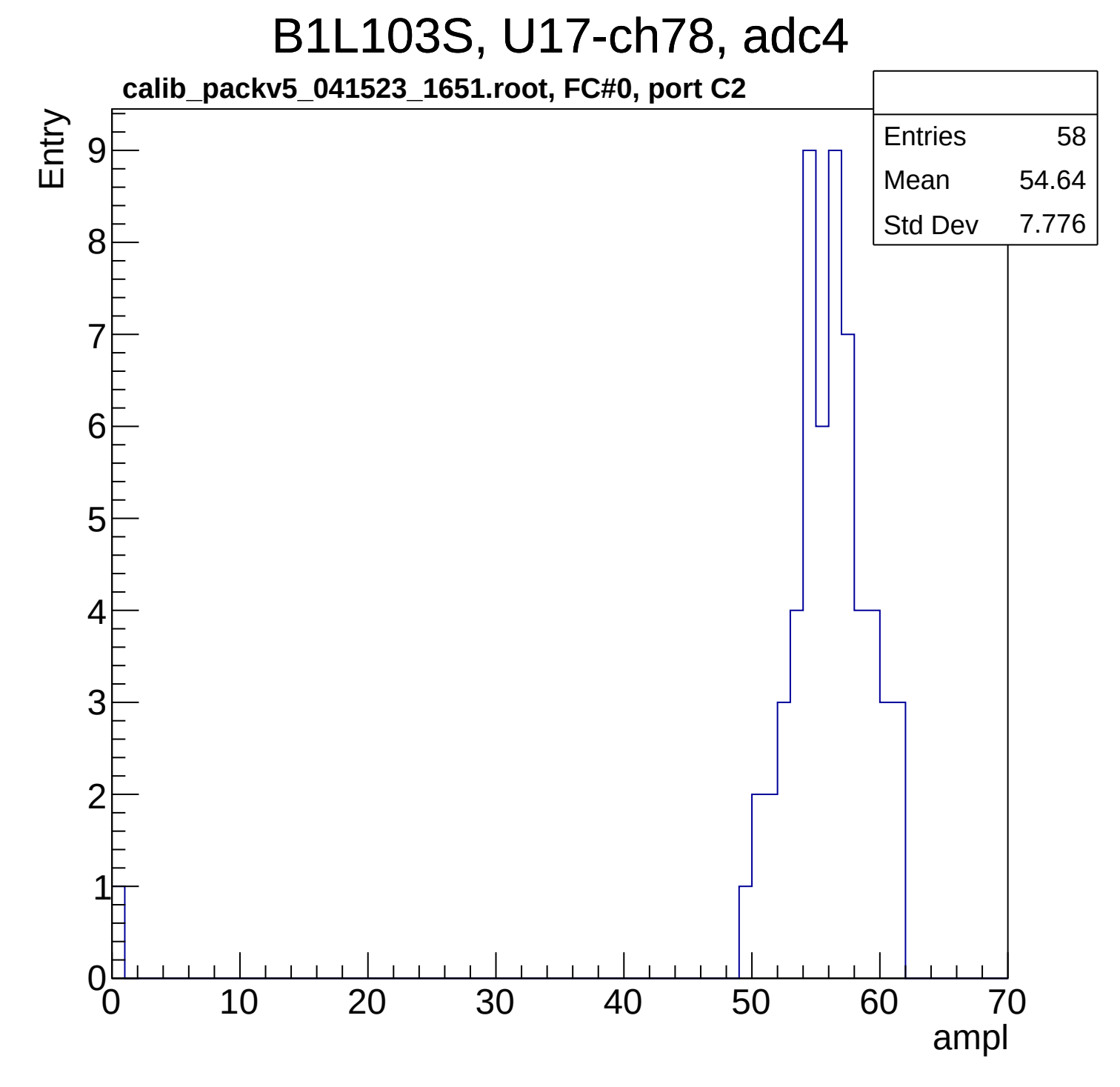
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U17-ch78, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 42.29
Std Dev 9.302
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U17-ch78, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 41.03
Std Dev 18.57
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70


B1L103S, U17-ch78, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 54.64
Std Dev 7.776
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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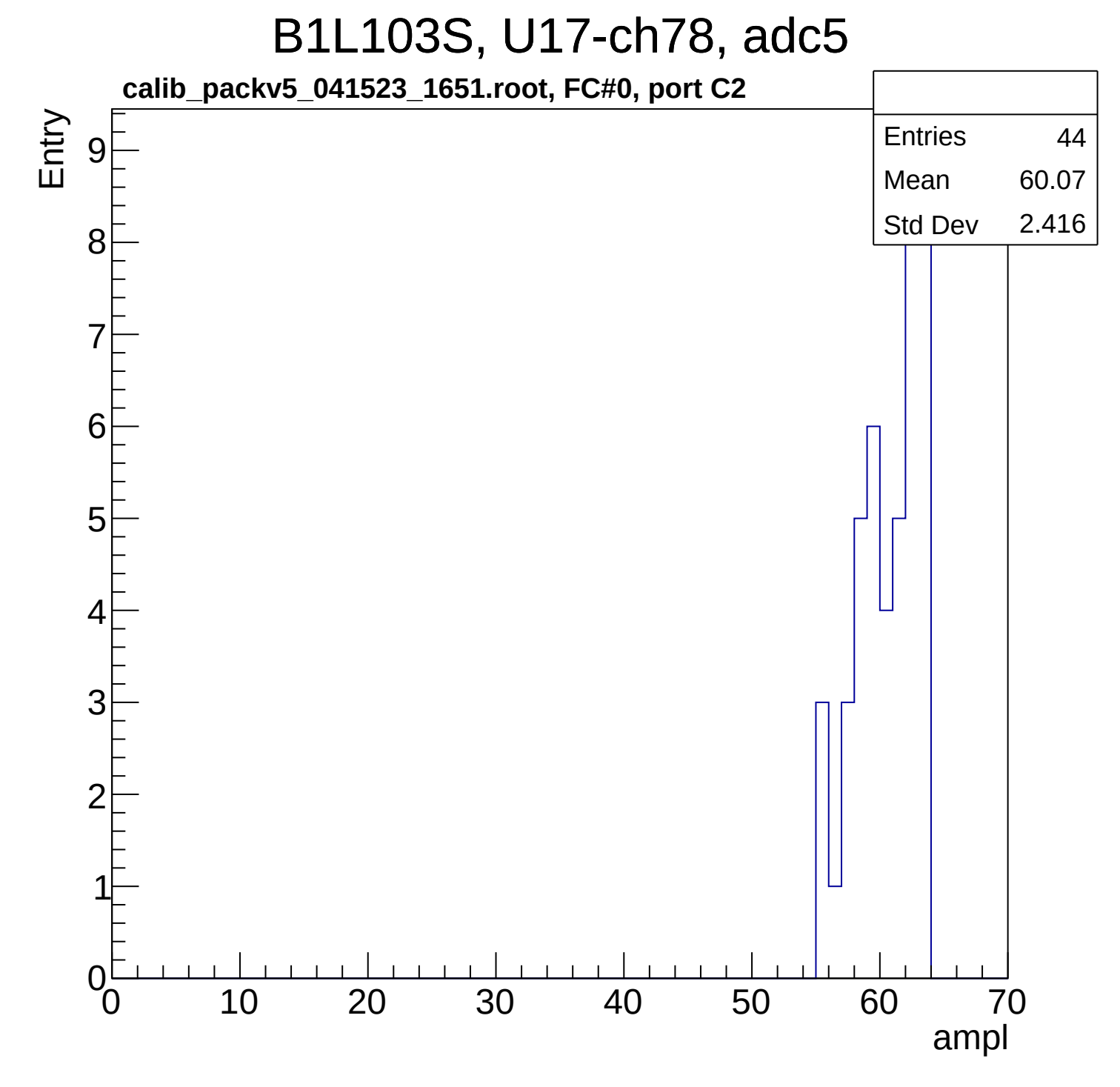
B1L103S, U17-ch78, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 60.07
Std Dev 2.416
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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60
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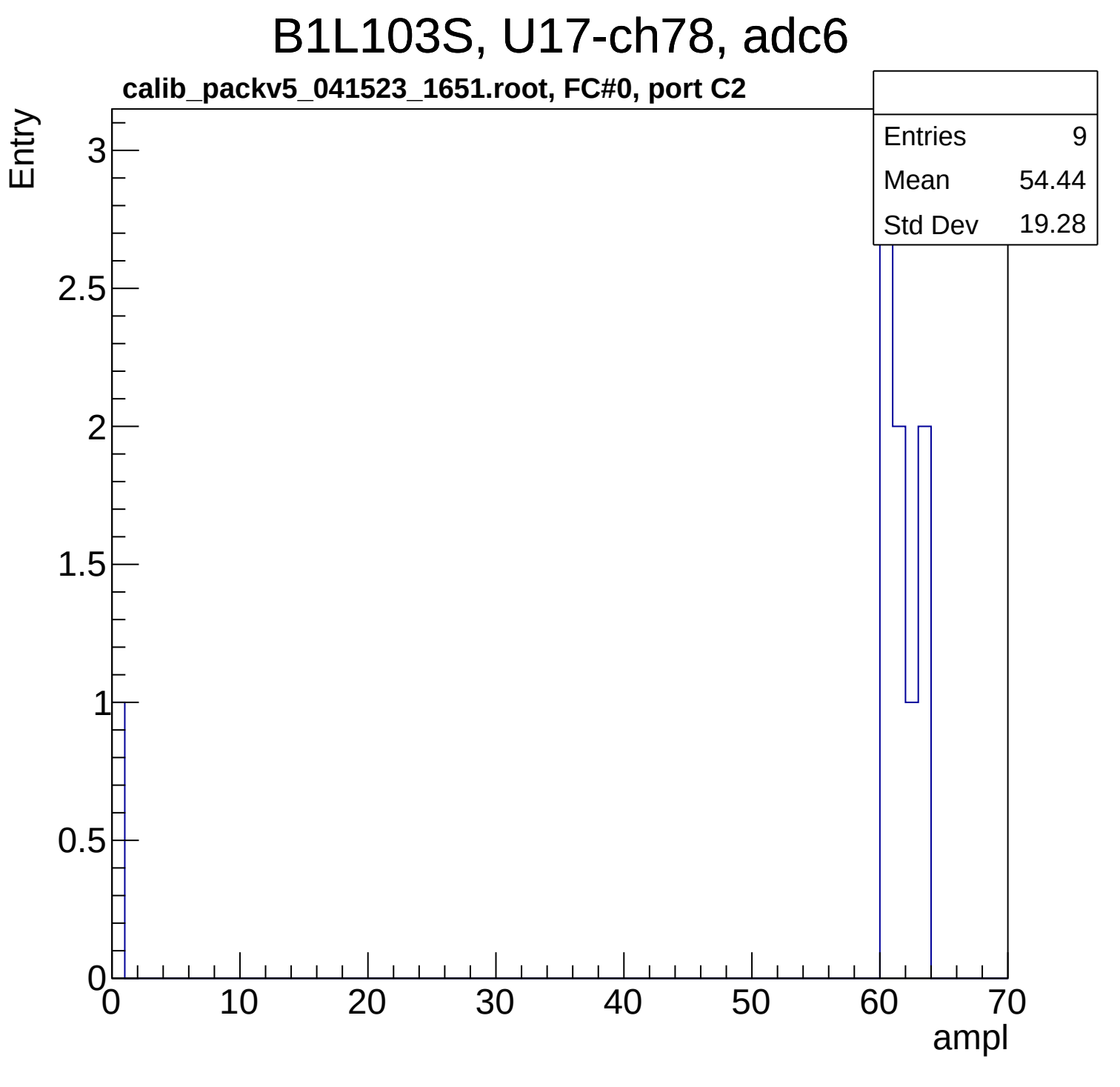
B1L103S, U17-ch78, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 9
Mean 54.44
Std Dev 19.28
Entry
ampl
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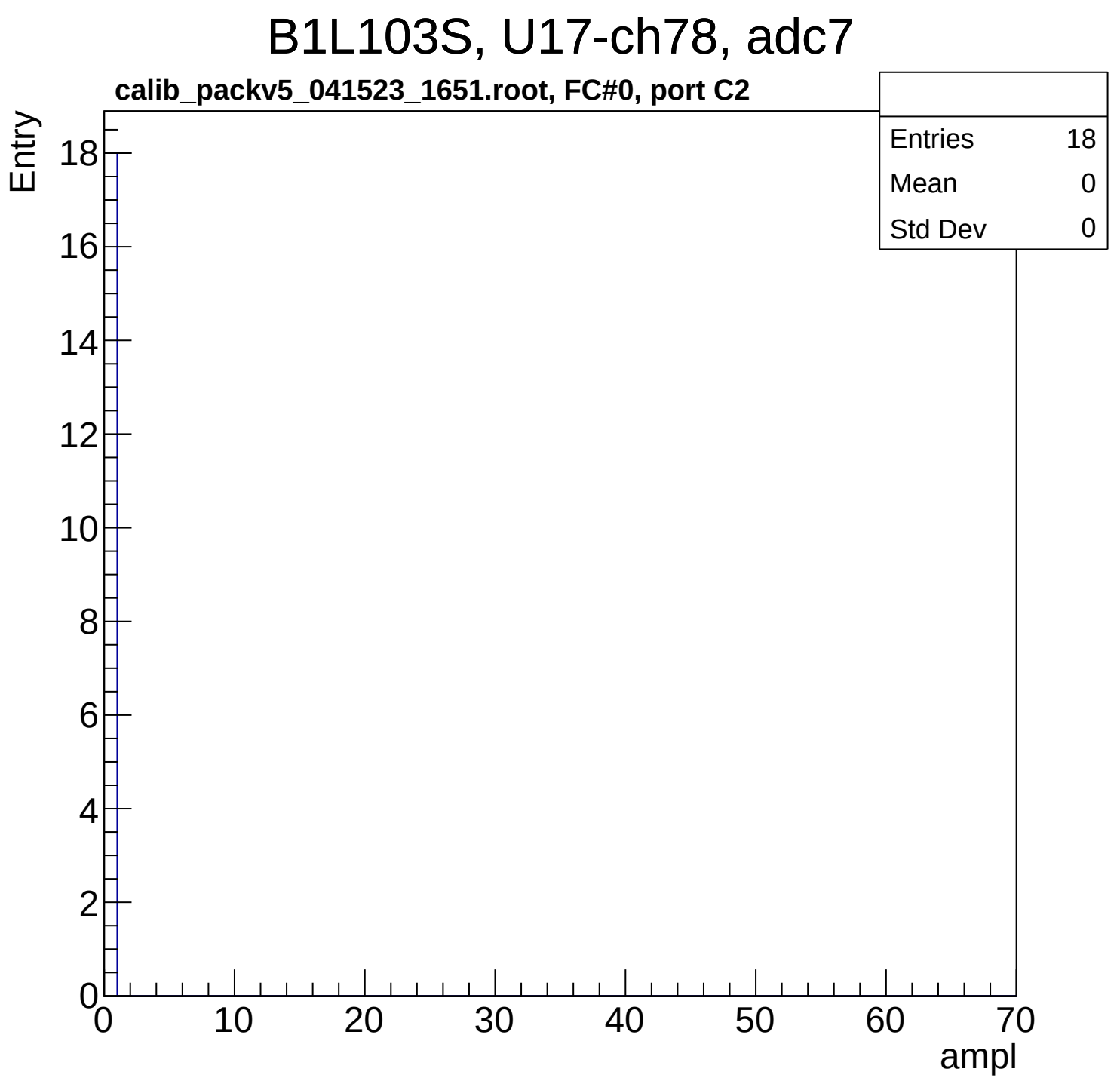
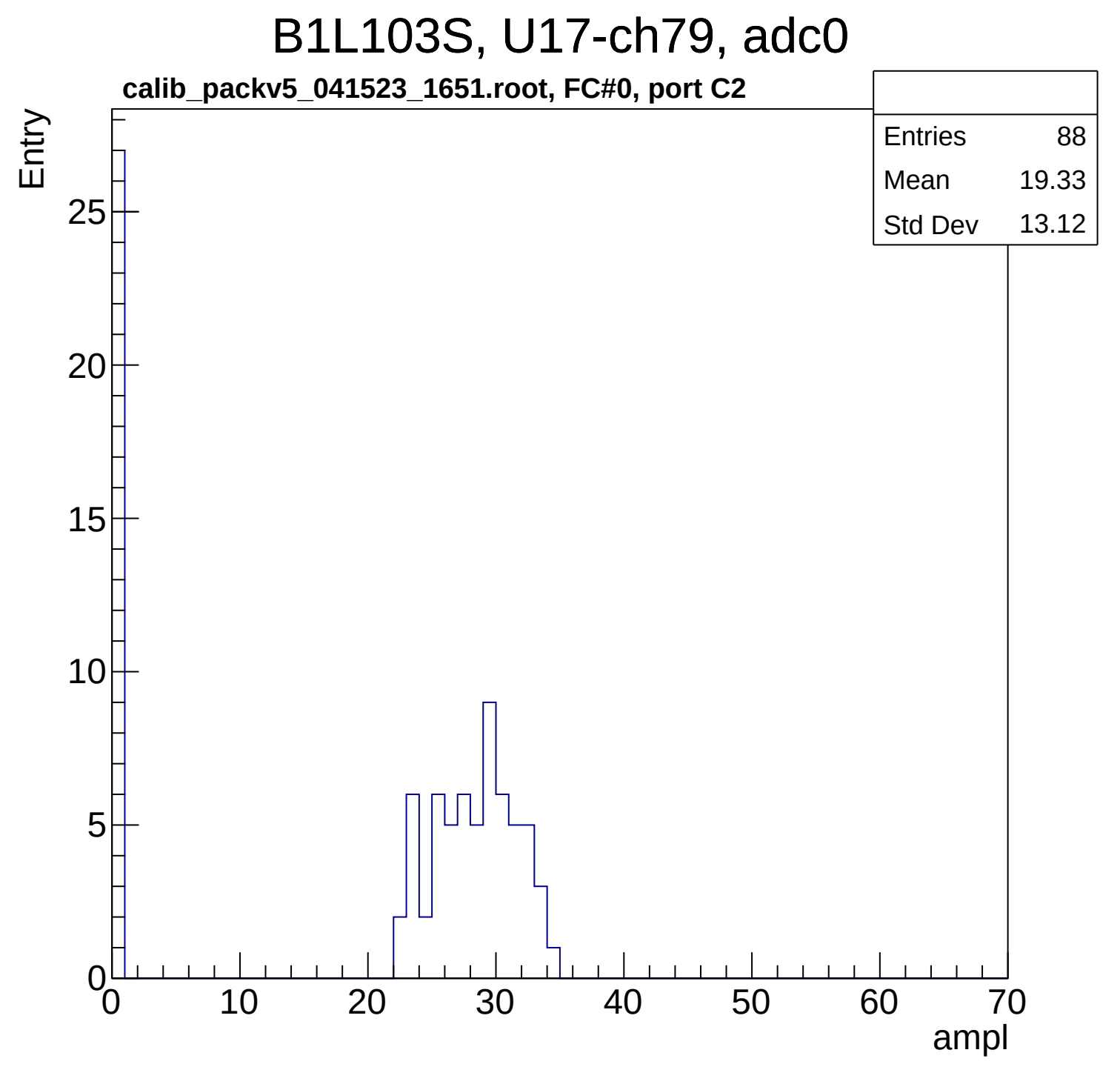
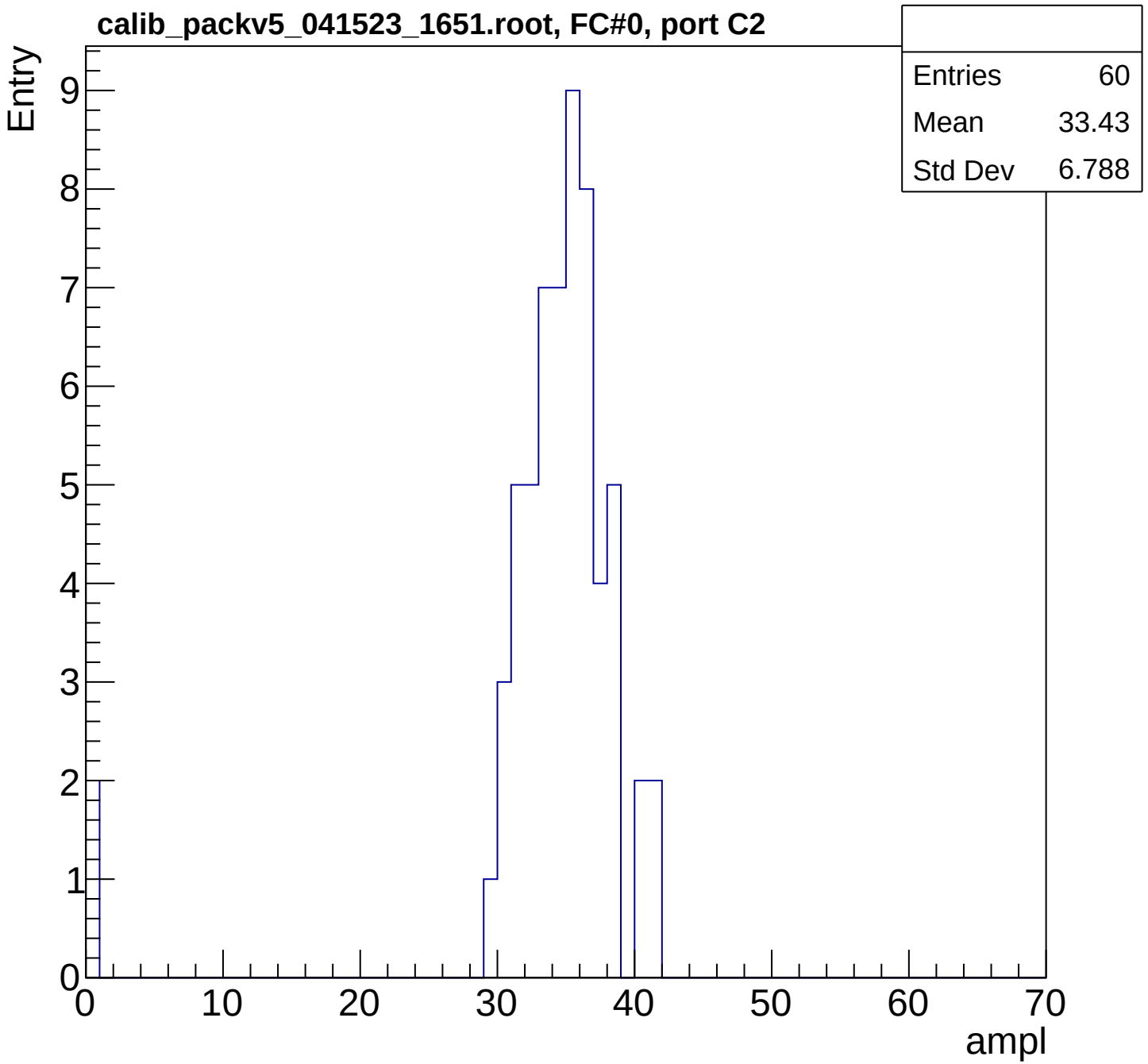
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U17-ch78, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch79, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 88
Mean 19.33
Std Dev 13.12
Entry
0
5
10
15
20
25
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch79, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 33.43
Std Dev 6.788
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
50
60
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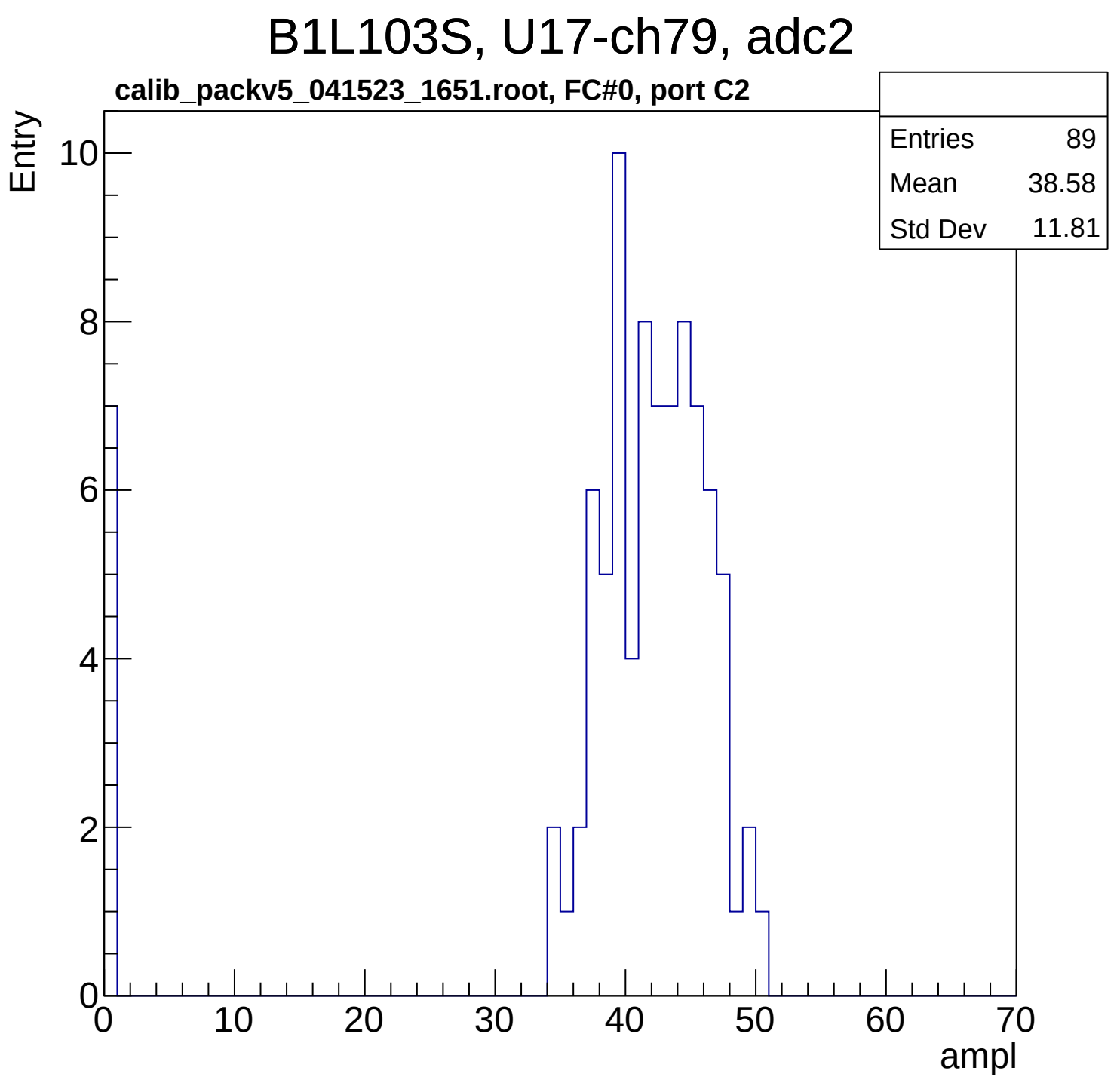
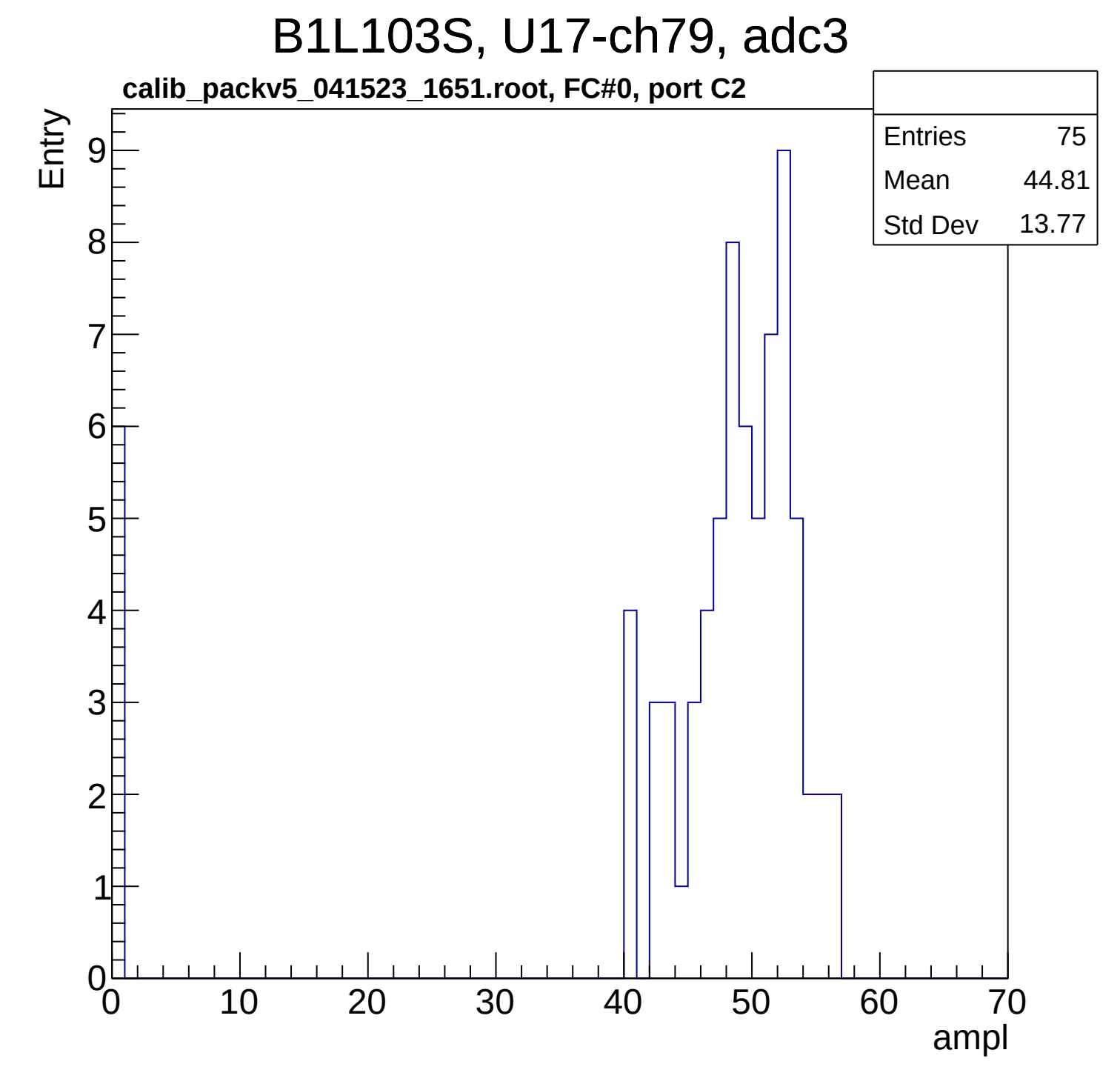

B1L103S, U17-ch79, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 89
Mean 38.58
Std Dev 11.81
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U17-ch79, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 44.81
Std Dev 13.77
Entry
ampl
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1
2
3
4
5
6
7
8
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0
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60
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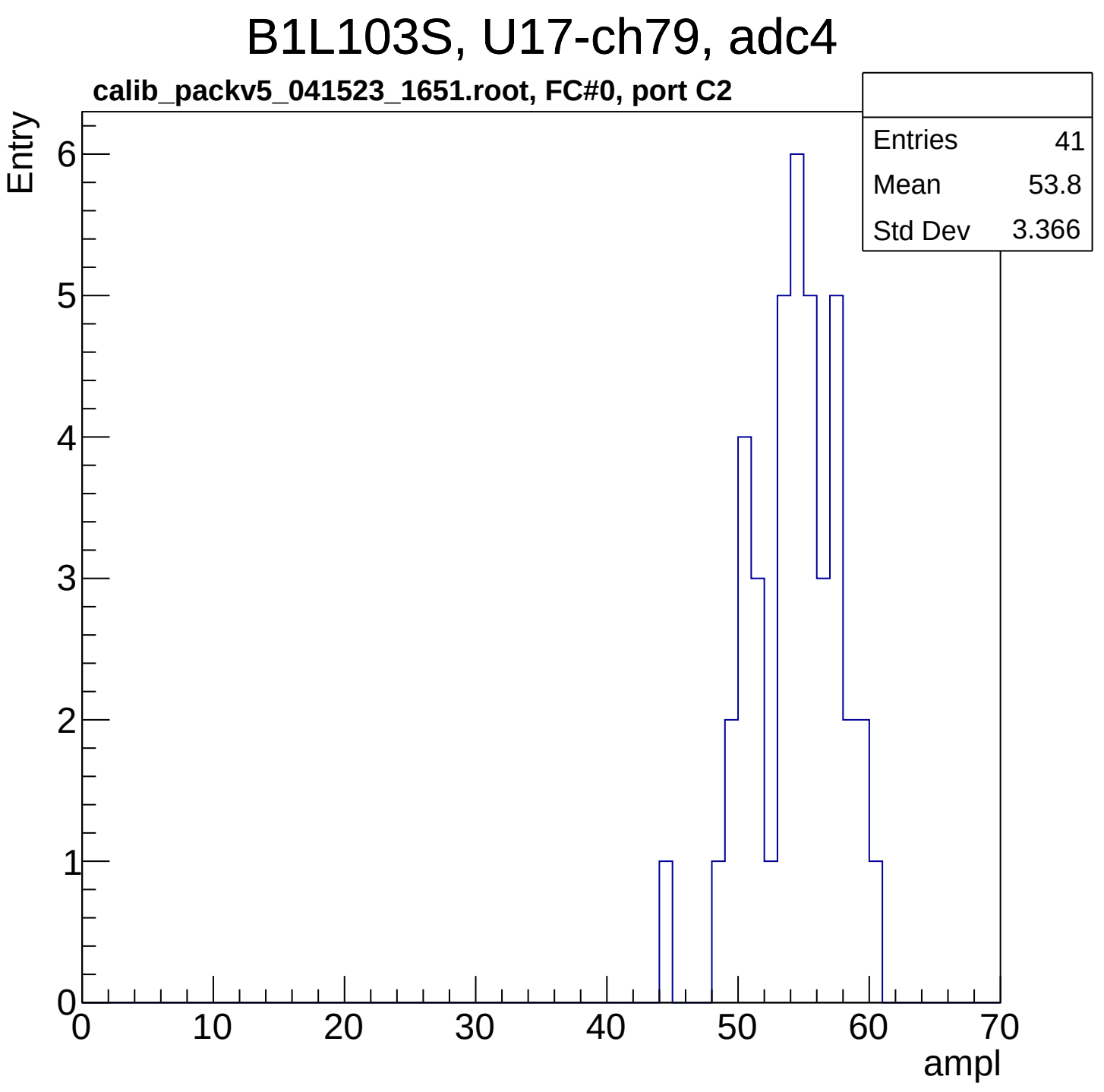
B1L103S, U17-ch79, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 41
Mean 53.8
Std Dev 3.366
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
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60
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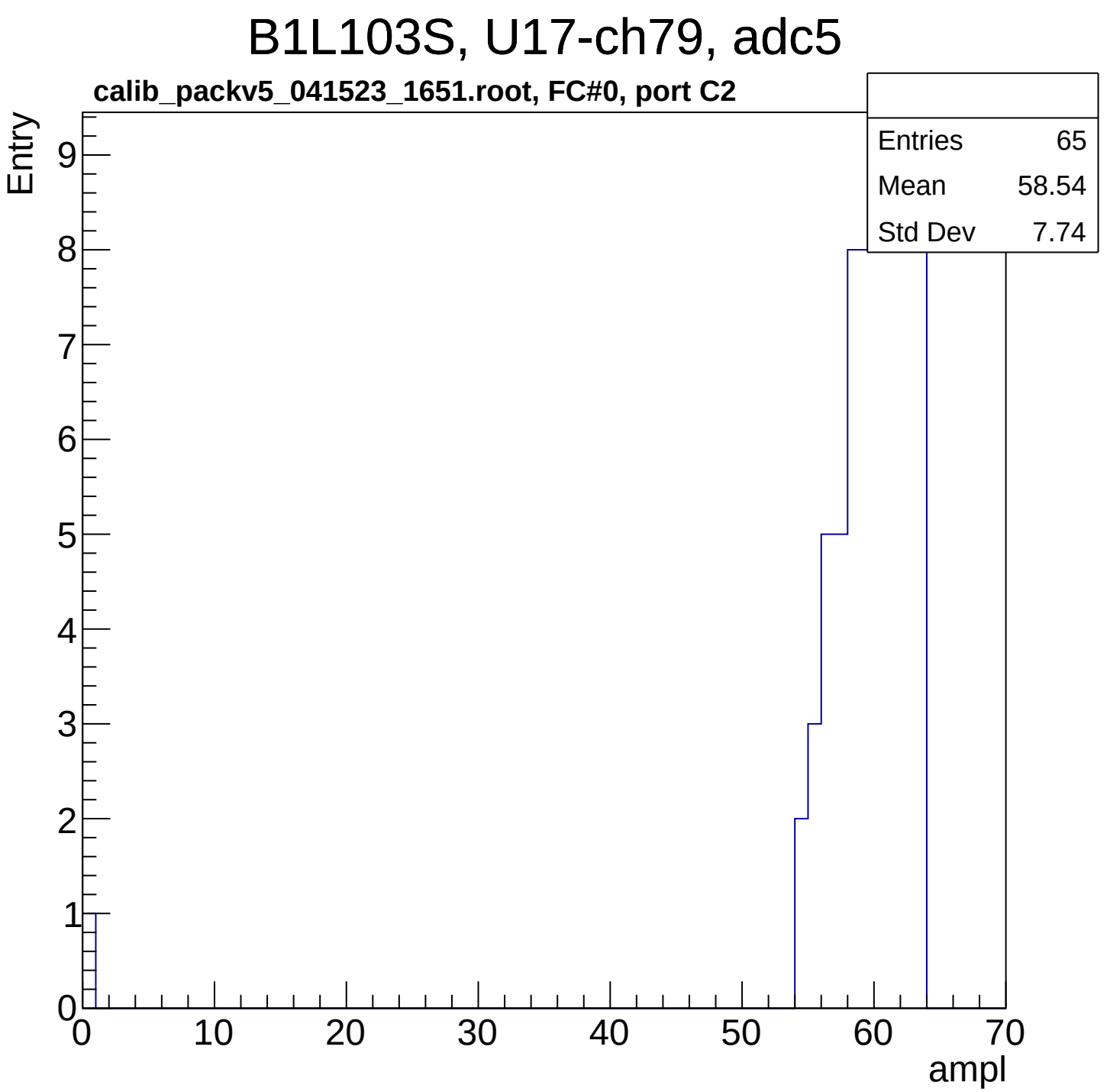
B1L103S, U17-ch79, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 58.54
Std Dev 7.74
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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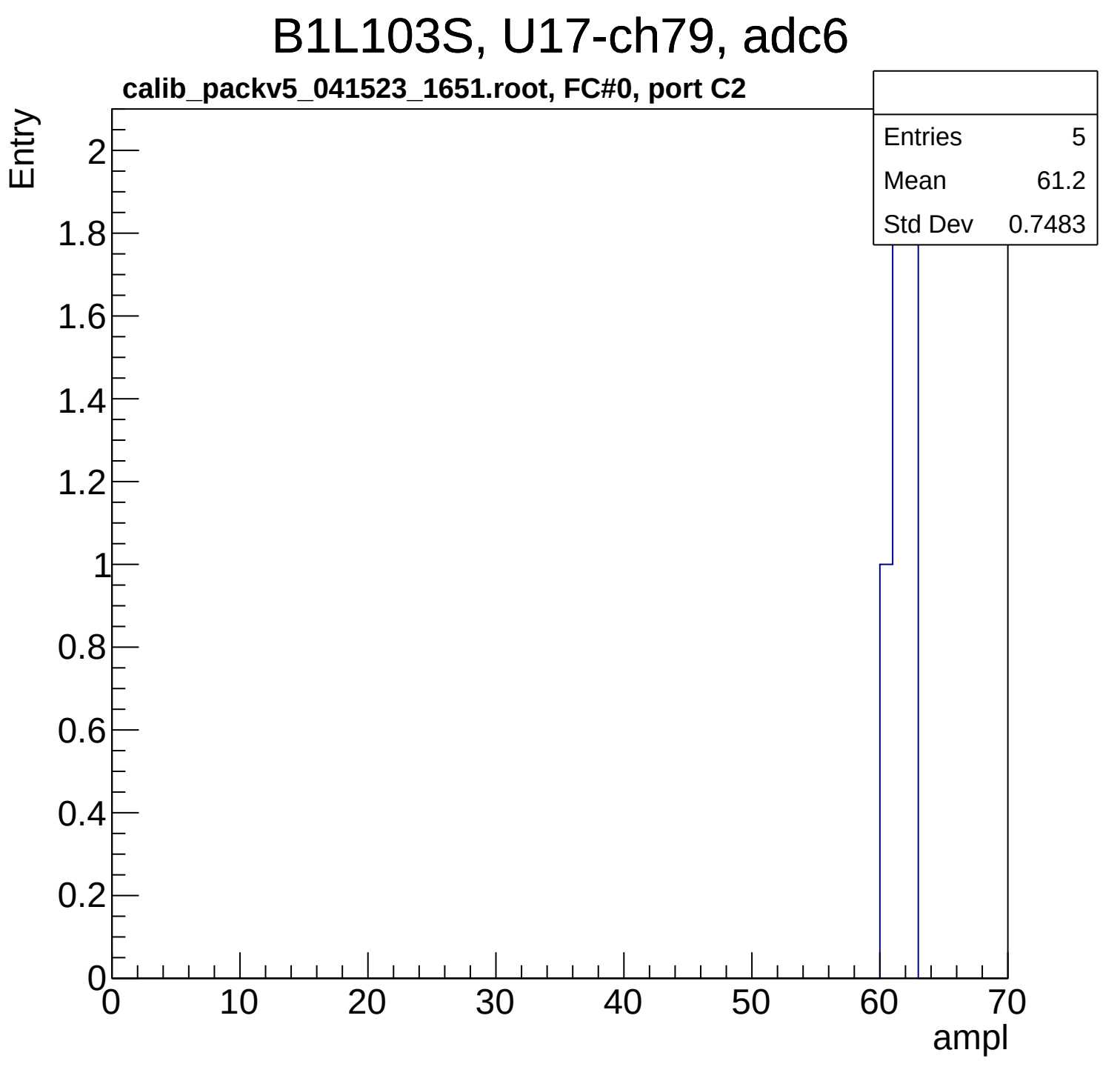
B1L103S, U17-ch79, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 5
Mean 61.2
Std Dev 0.7483
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
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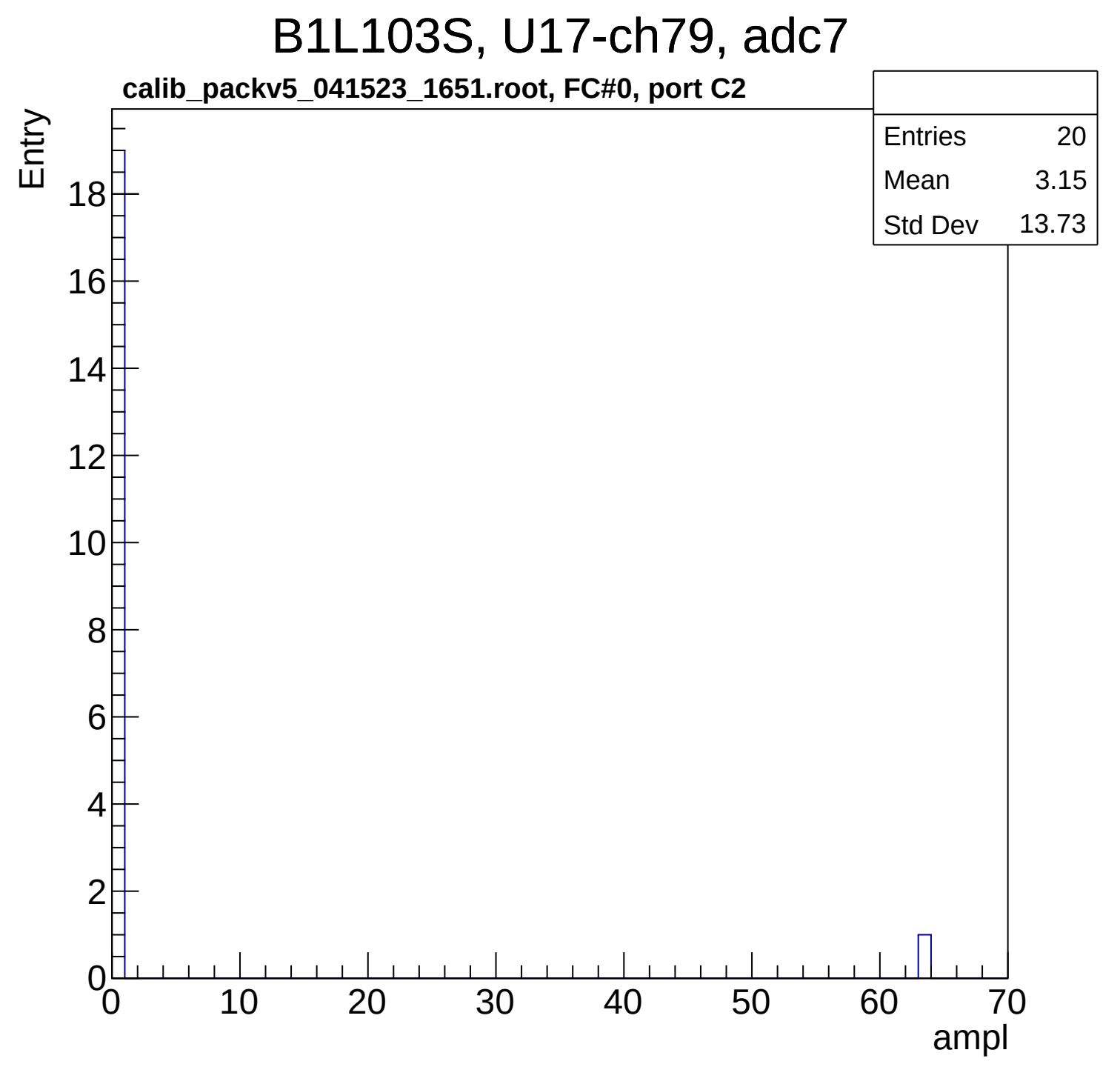
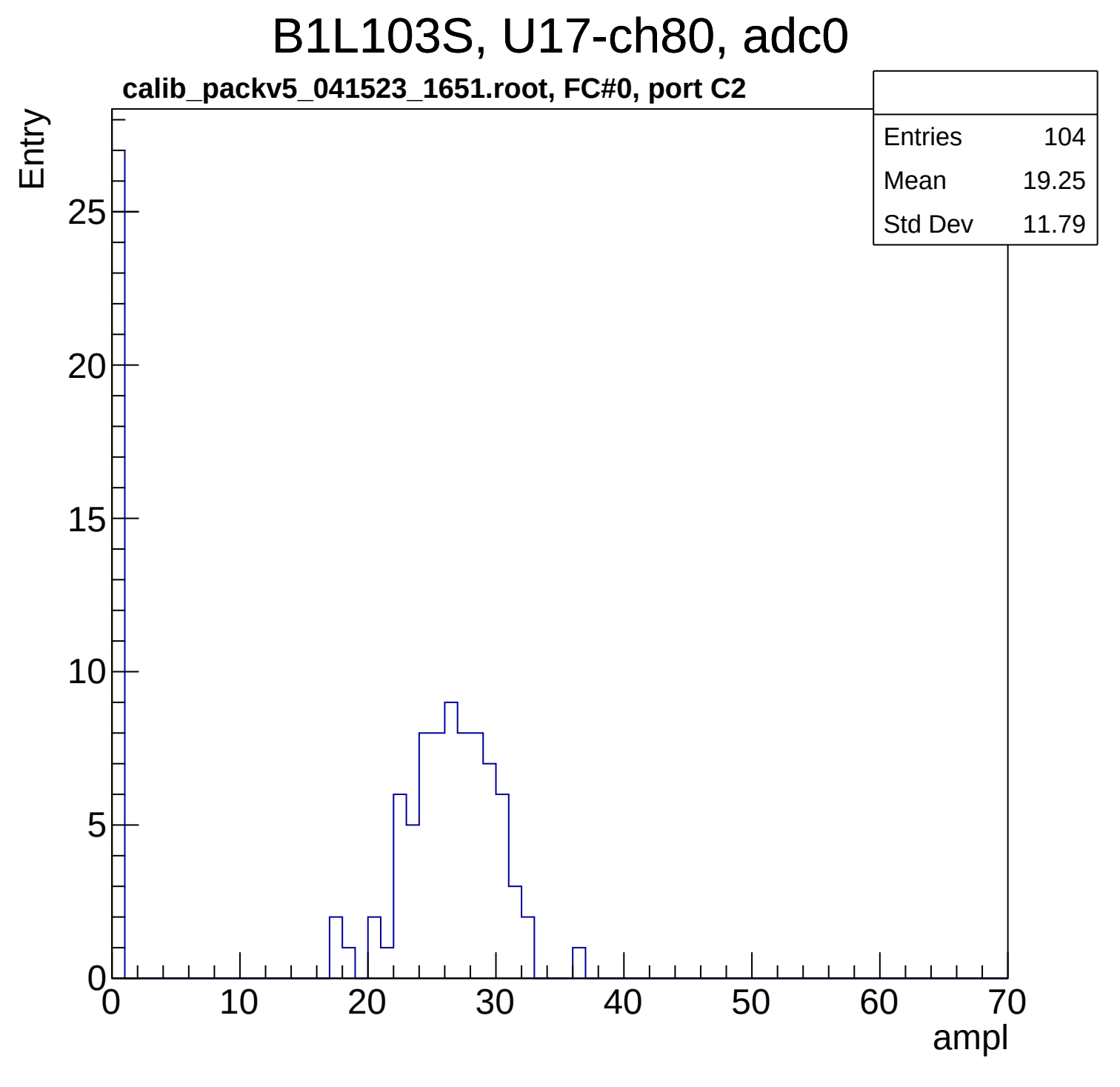
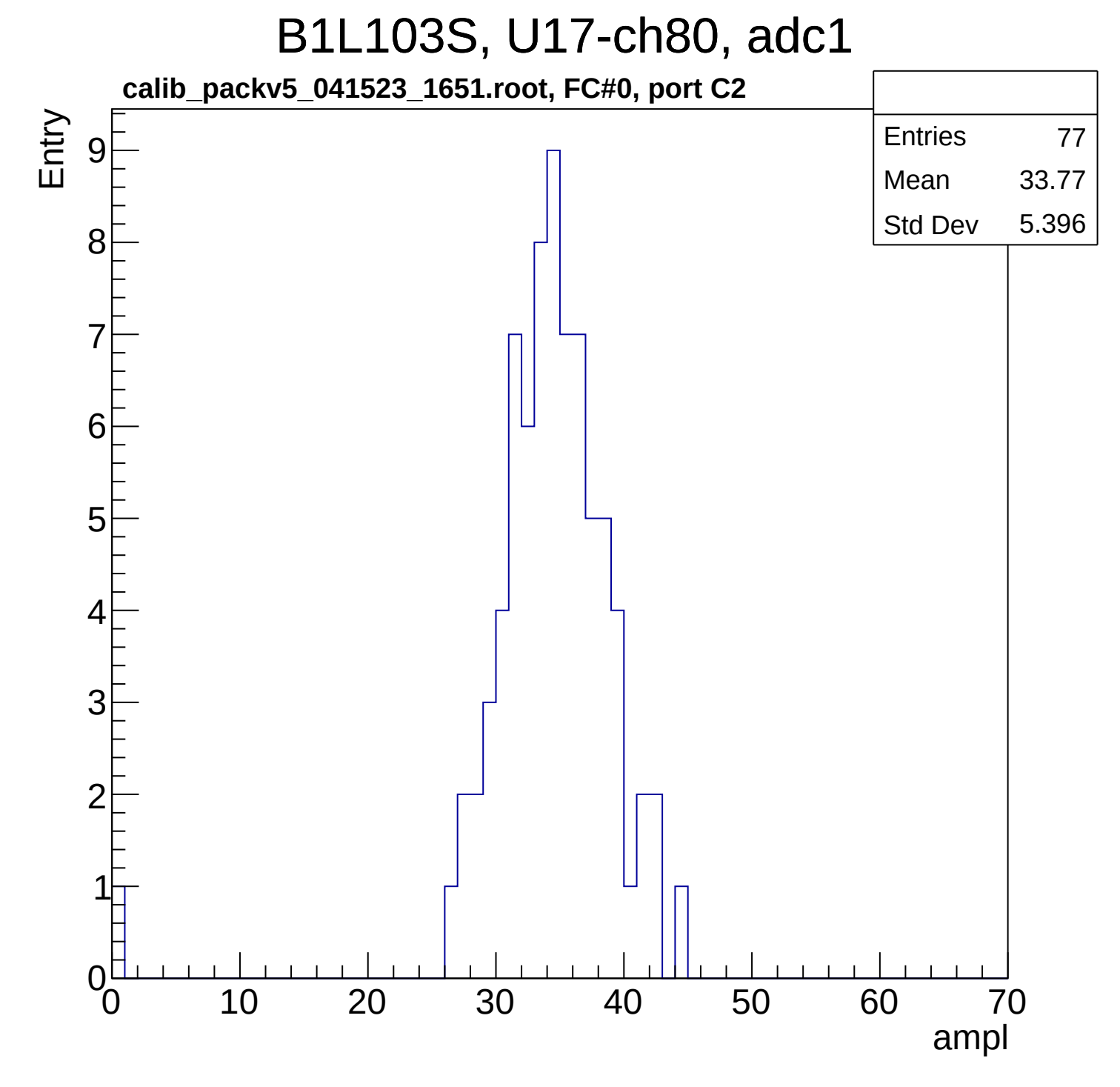

B1L103S, U17-ch79, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch80, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 104
Mean 19.25
Std Dev 11.79
Entry
0
5
10
15
20
25
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch80, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 33.77
Std Dev 5.396
Entry
ampl
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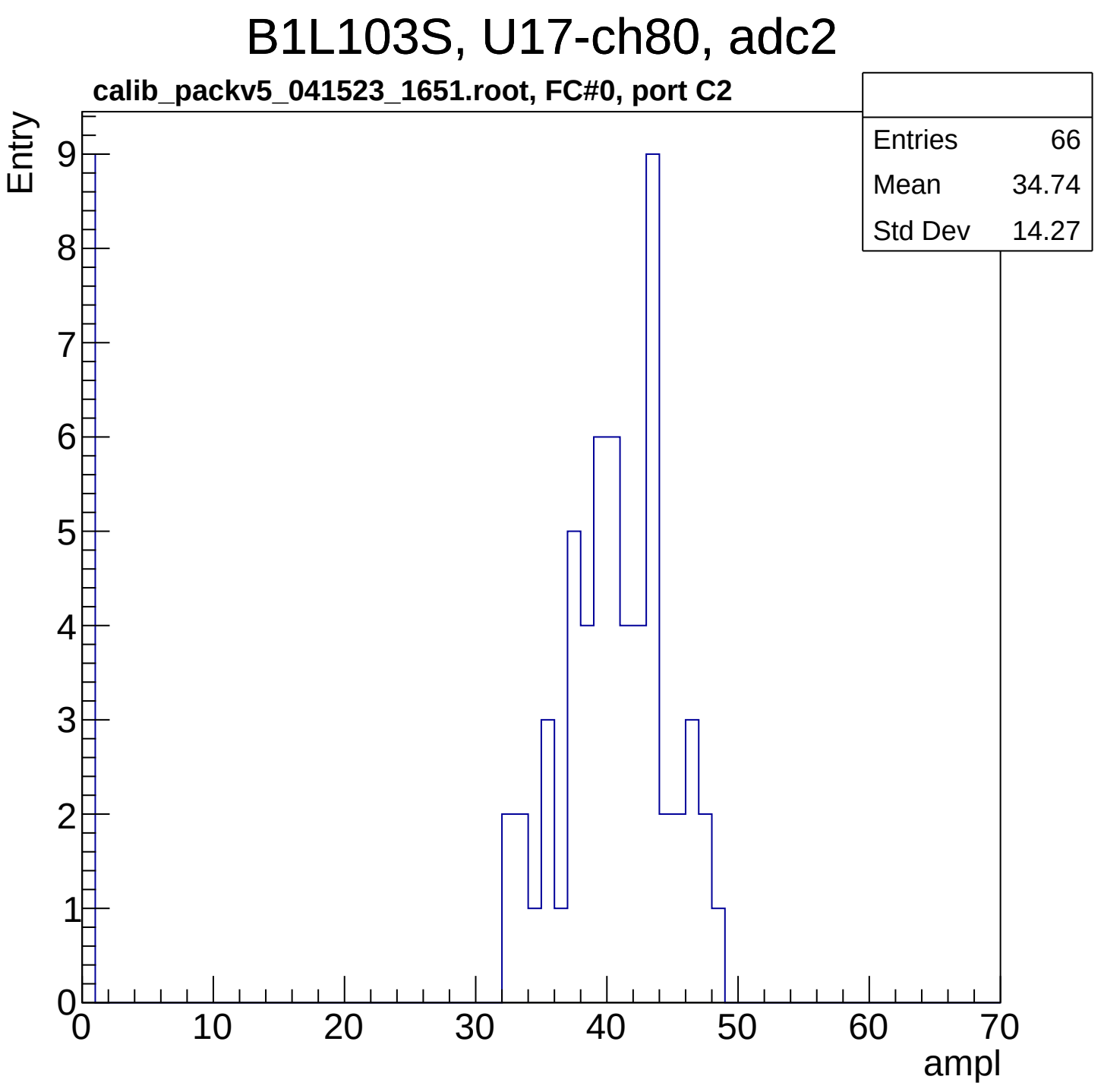
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U17-ch80, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 34.74
Std Dev 14.27
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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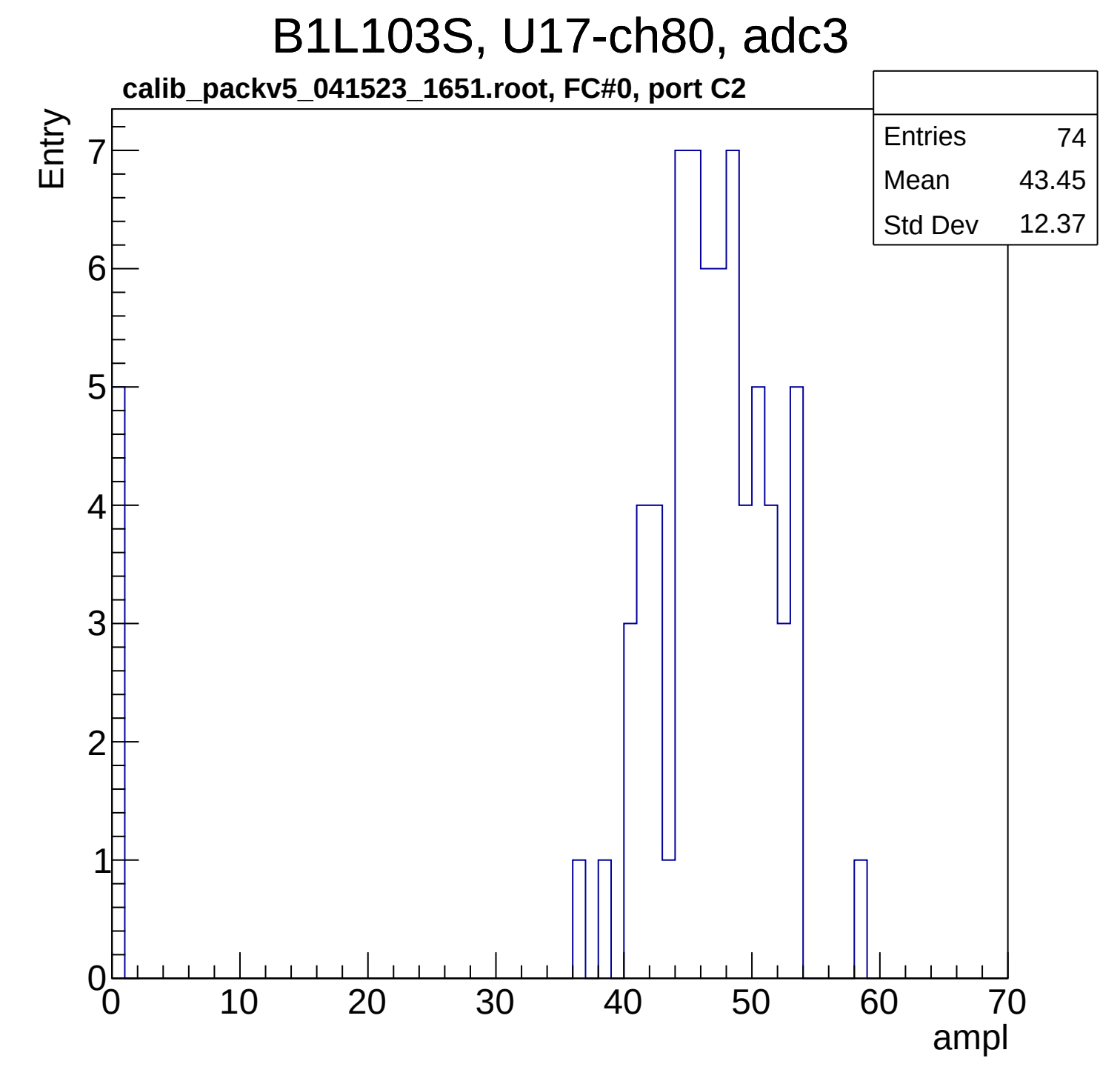
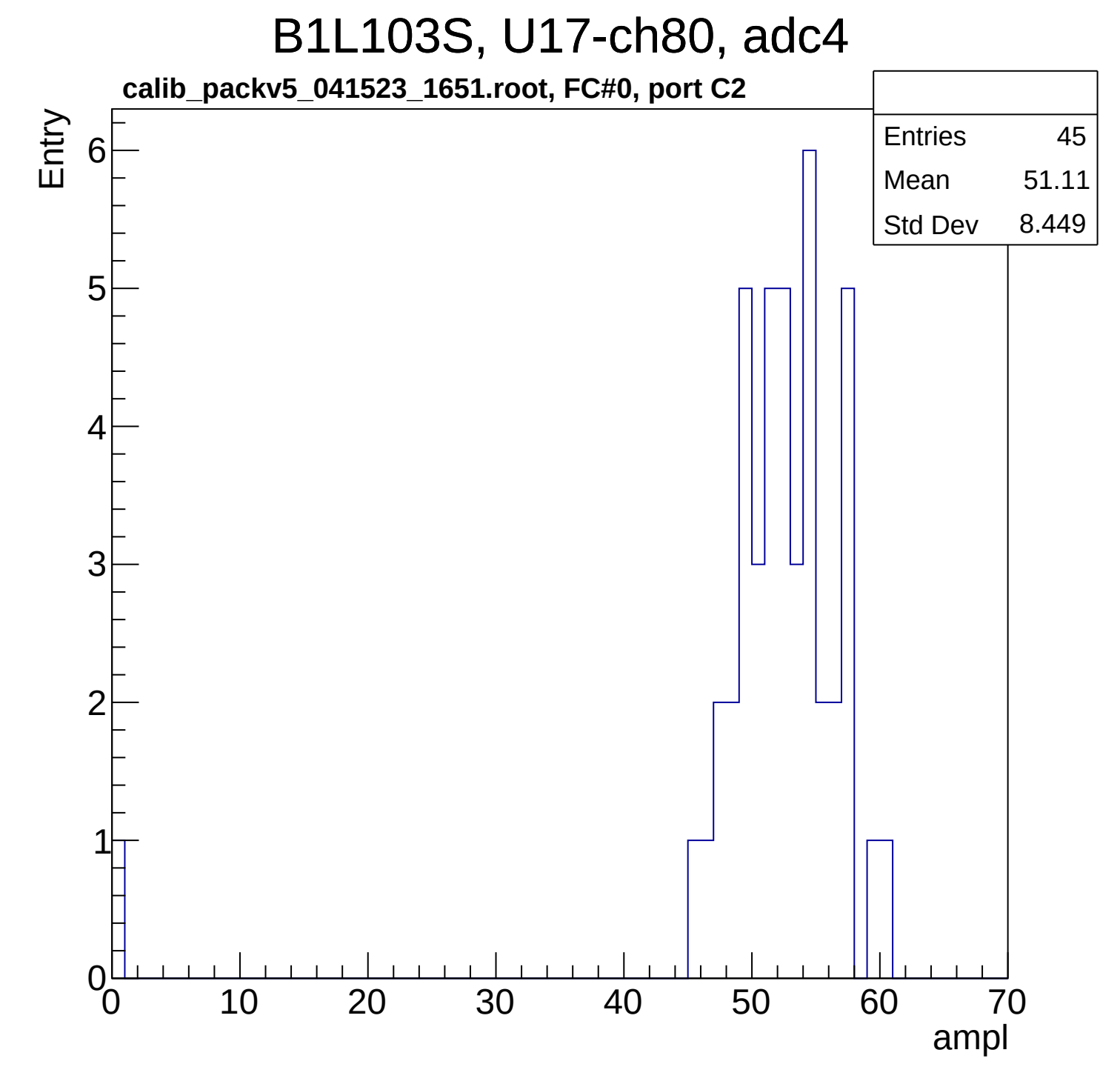
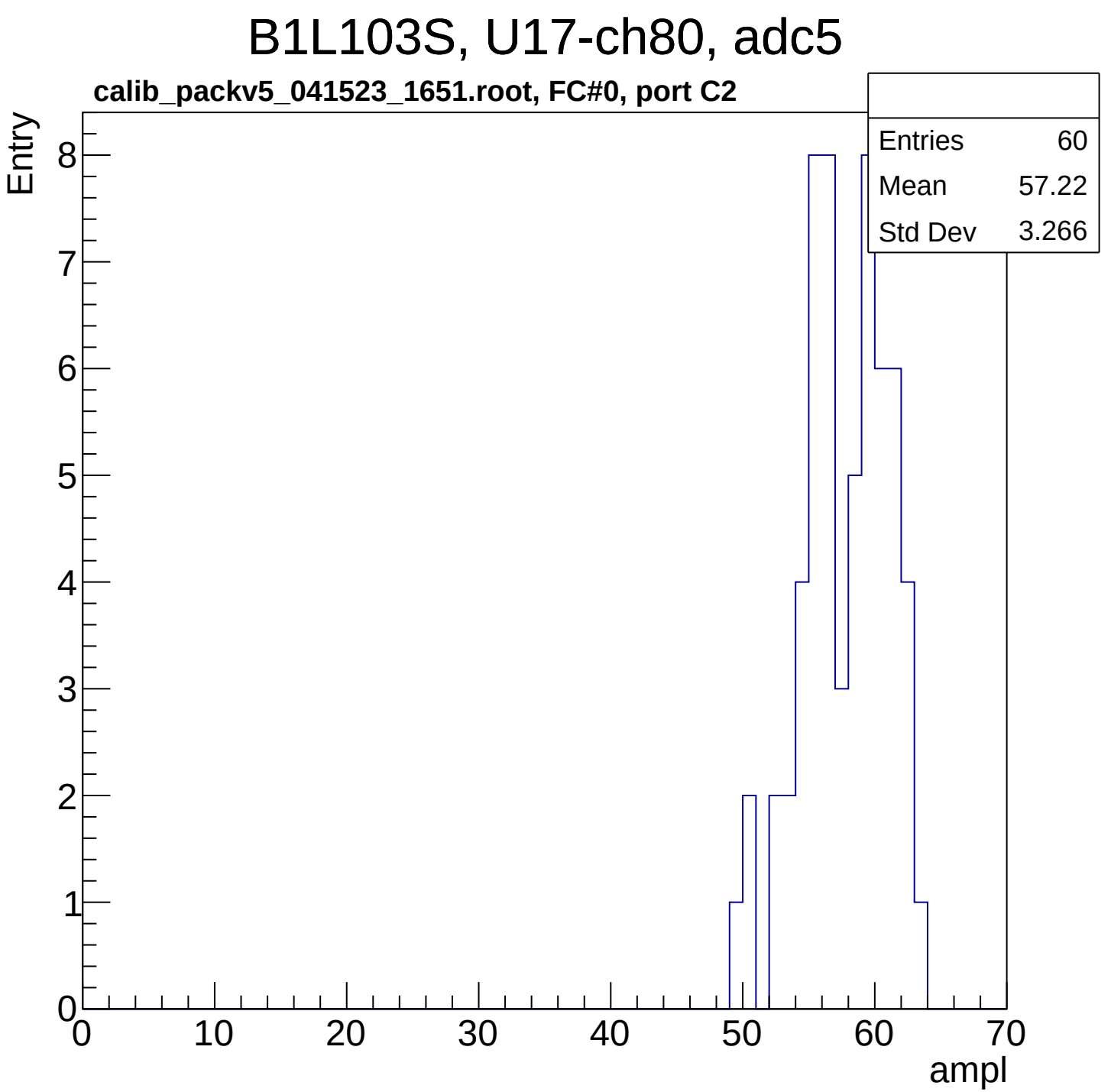

B1L103S, U17-ch80, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 43.45
Std Dev 12.37
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U17-ch80, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 51.11
Std Dev 8.449
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U17-ch80, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 57.22
Std Dev 3.266
Entry
ampl
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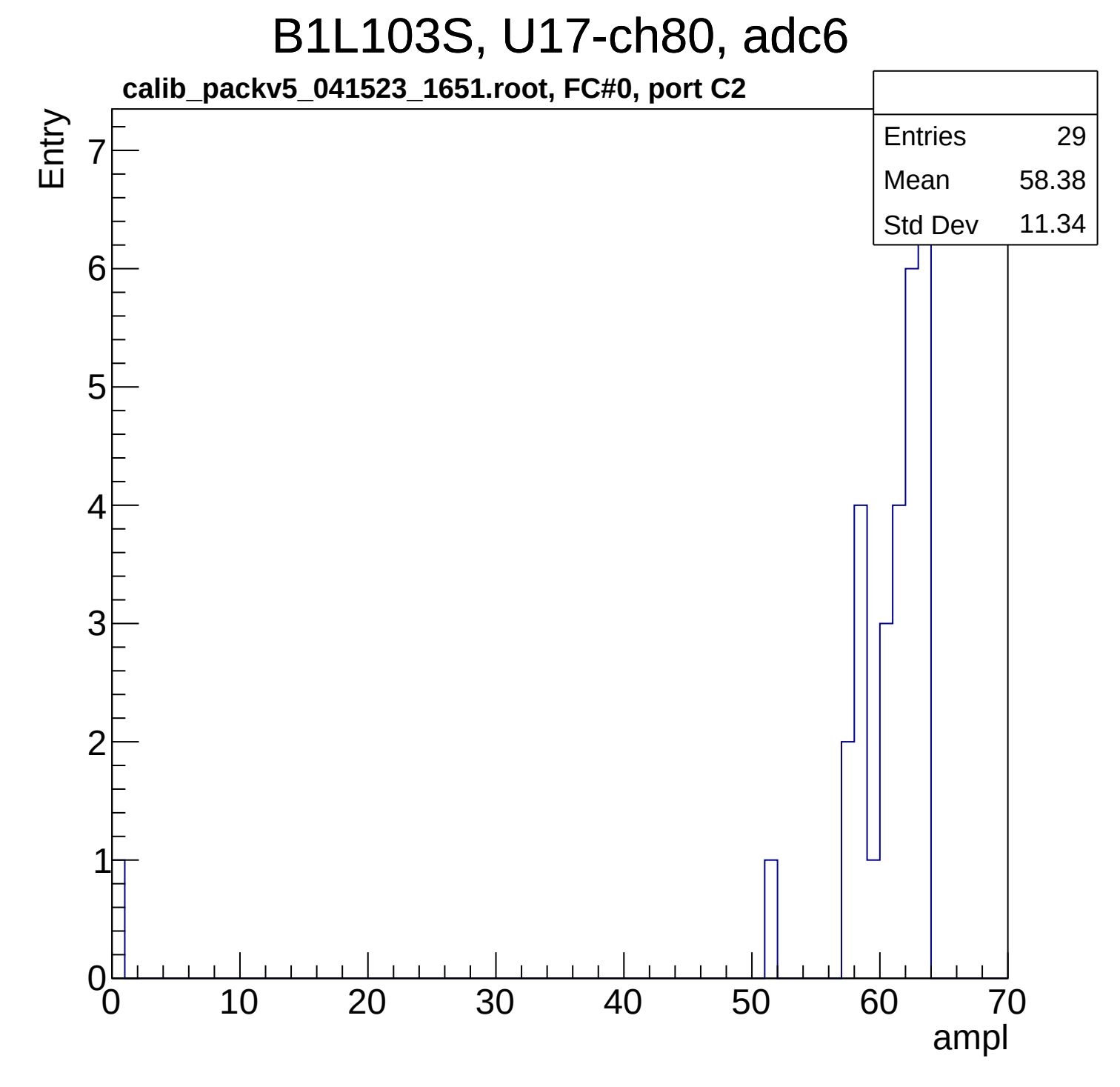
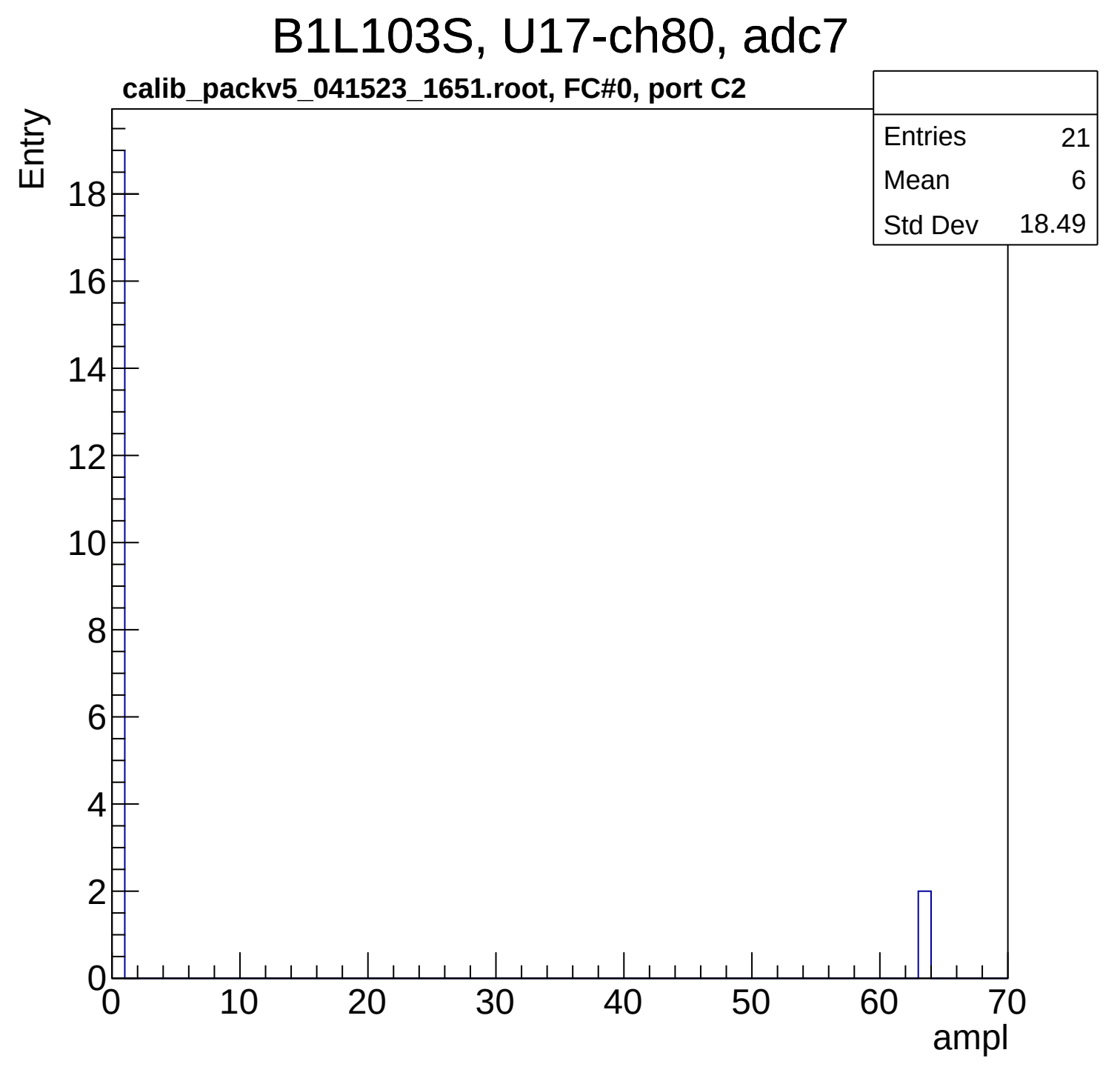
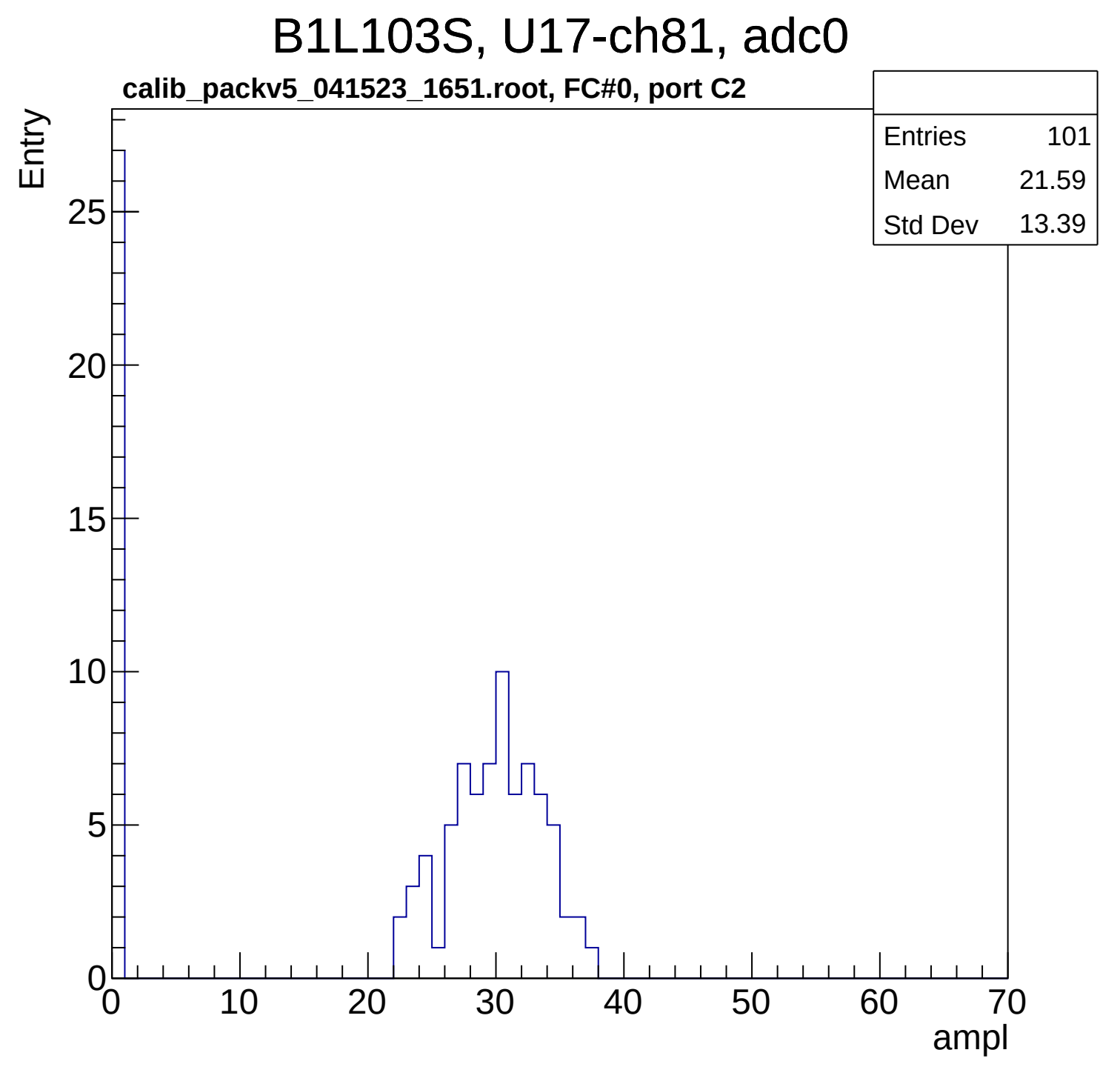
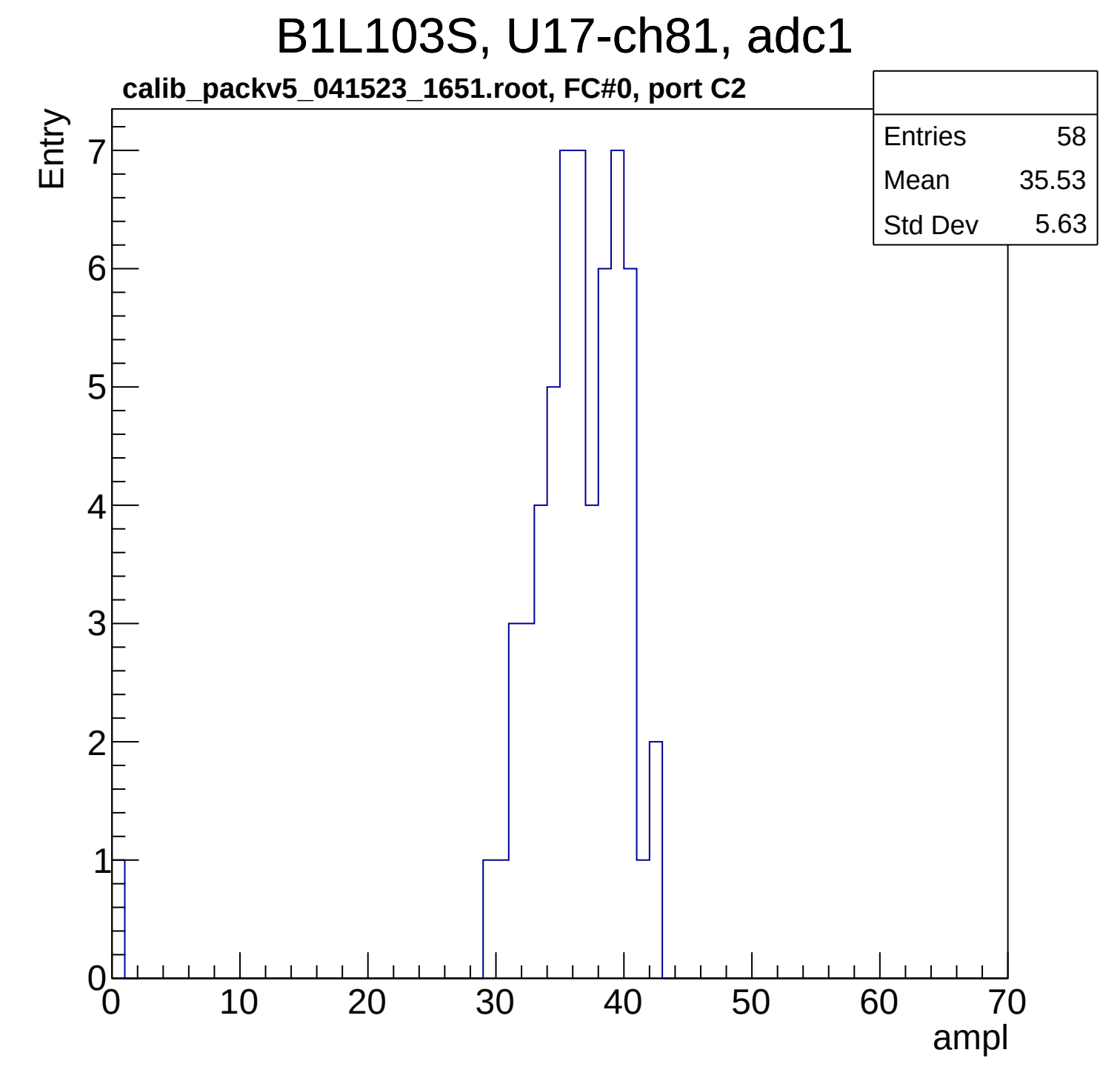
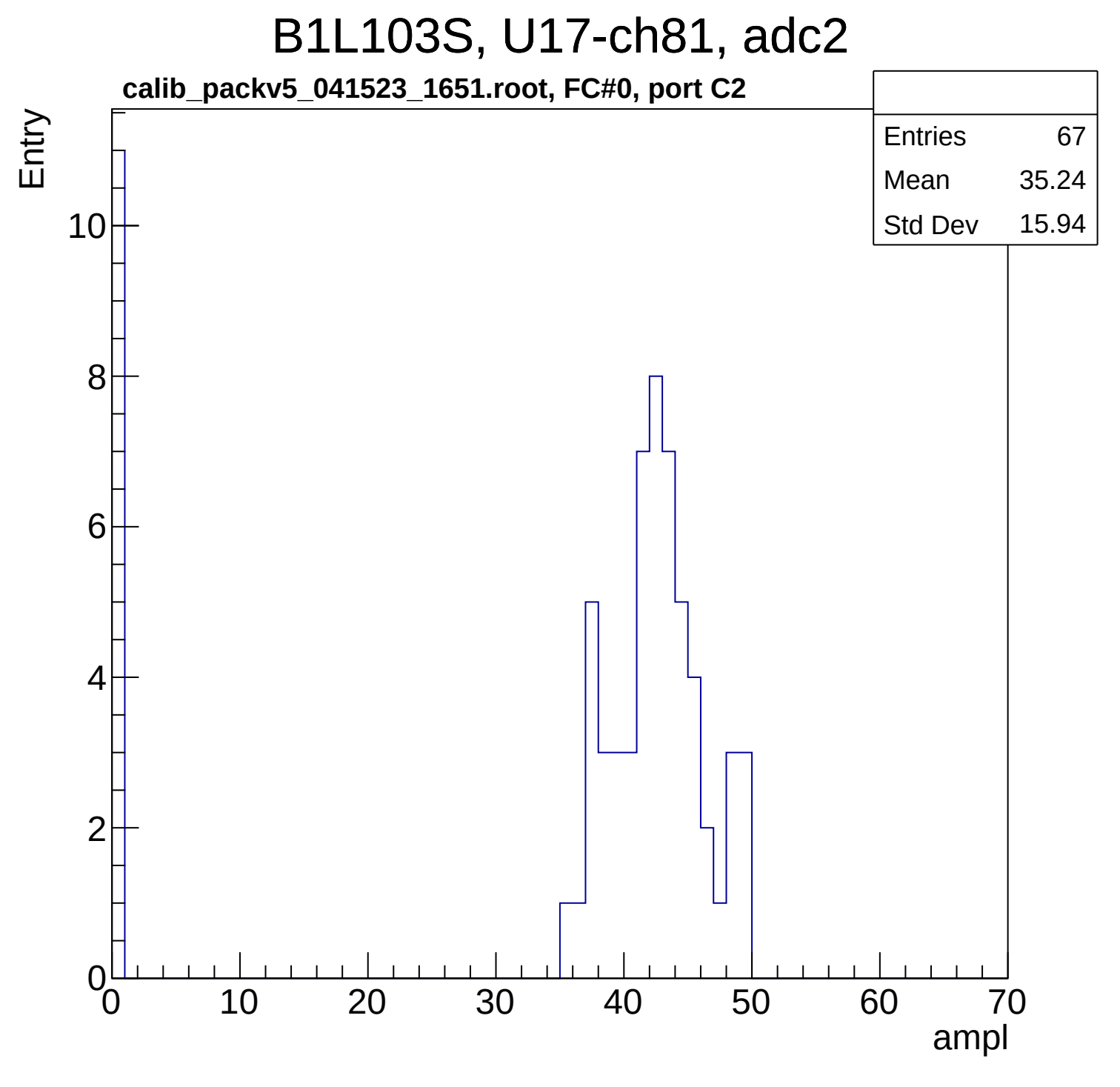
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

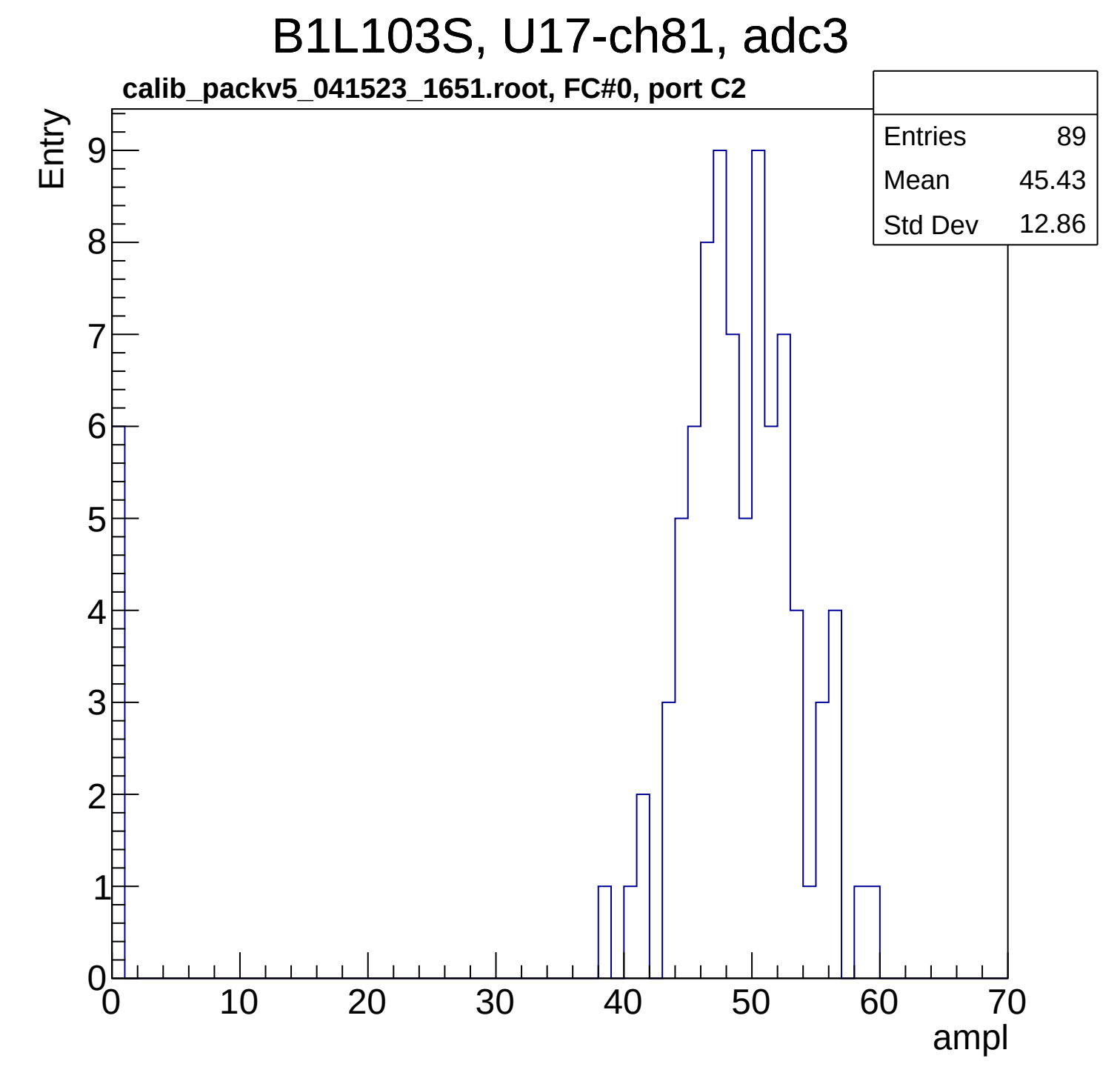

B1L103S, U17-ch80, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 29
Mean 58.38
Std Dev 11.34
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U17-ch80, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 6
Std Dev 18.49
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch81, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 101
Mean 21.59
Std Dev 13.39
Entry
0
5
10
15
20
25
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch81, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 35.53
Std Dev 5.63
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U17-ch81, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 35.24
Std Dev 15.94
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch81, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 89
Mean 45.43
Std Dev 12.86
Entry
ampl
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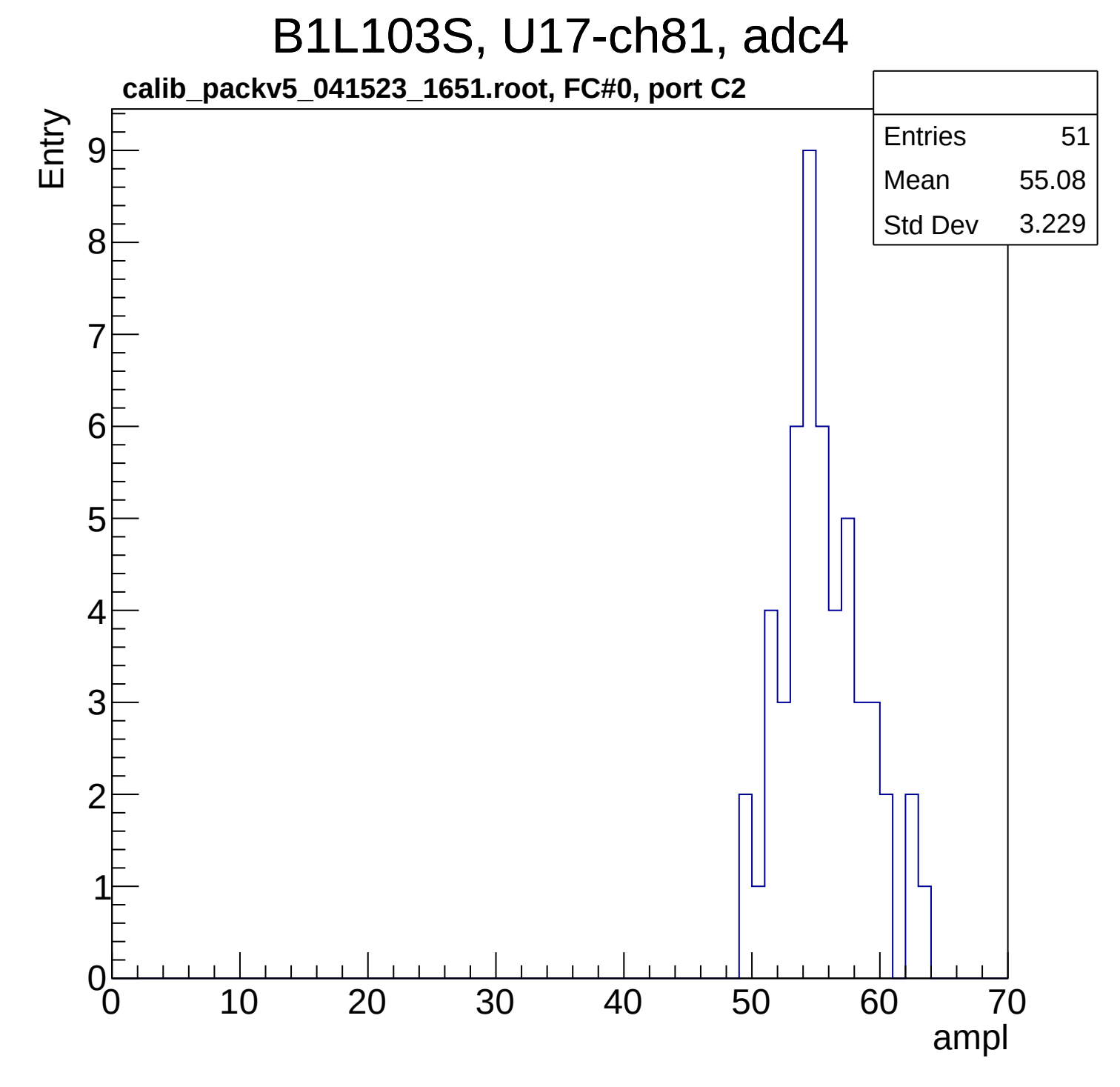
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9


B1L103S, U17-ch81, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 55.08
Std Dev 3.229
Entry
ampl
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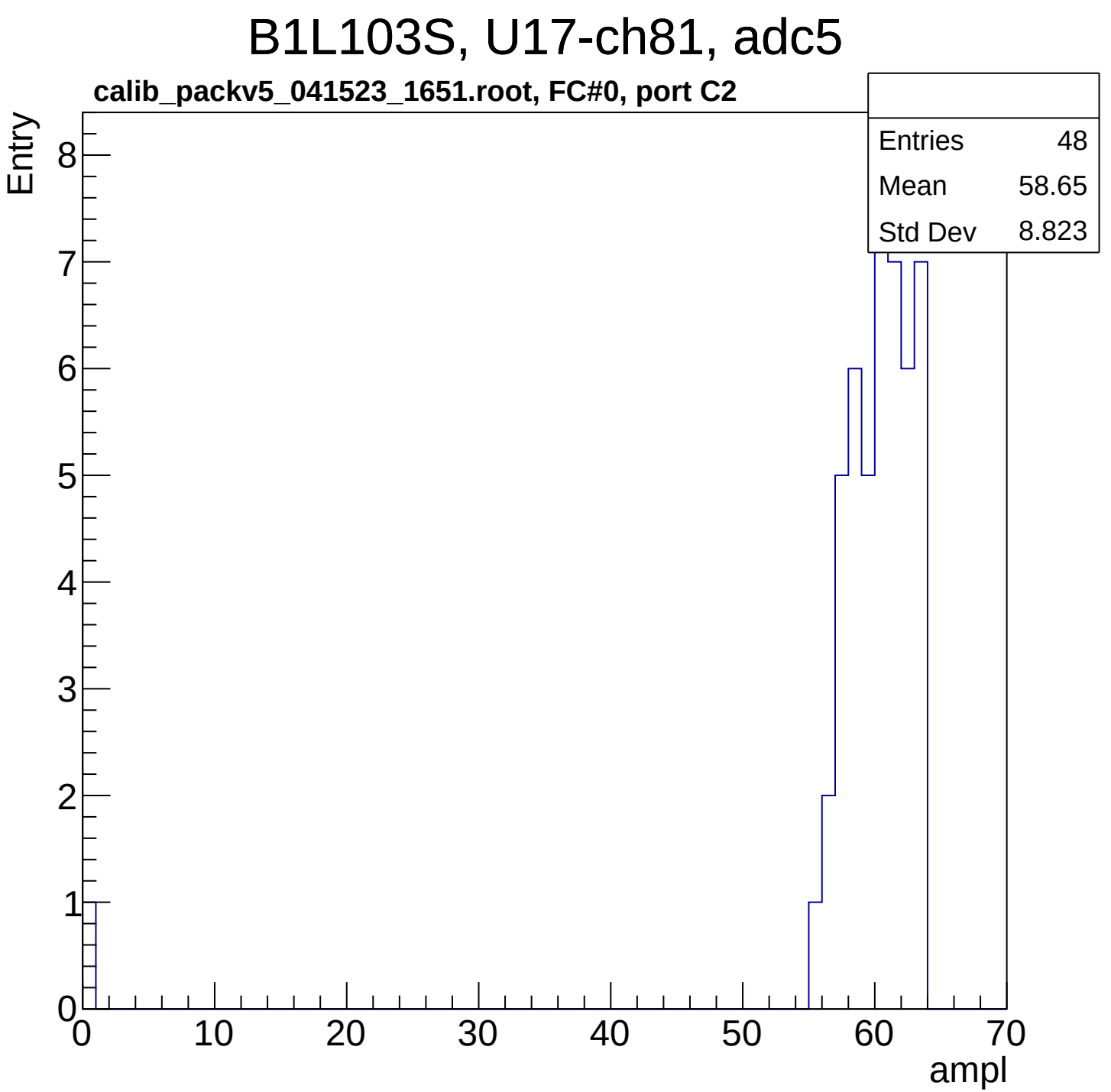
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U17-ch81, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 58.65
Std Dev 8.823
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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40
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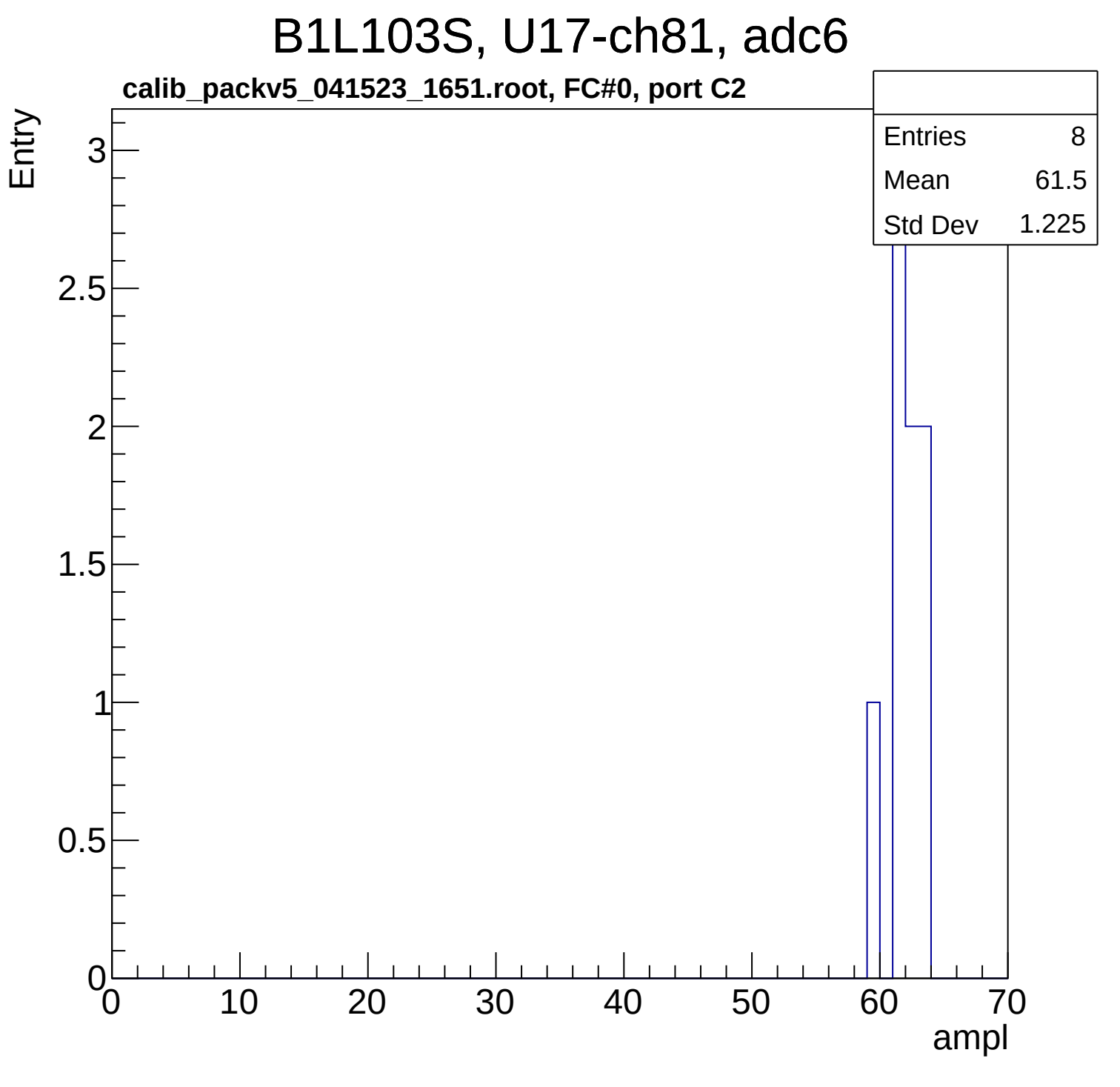
60
70


B1L103S, U17-ch81, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 61.5
Std Dev 1.225
Entry
ampl
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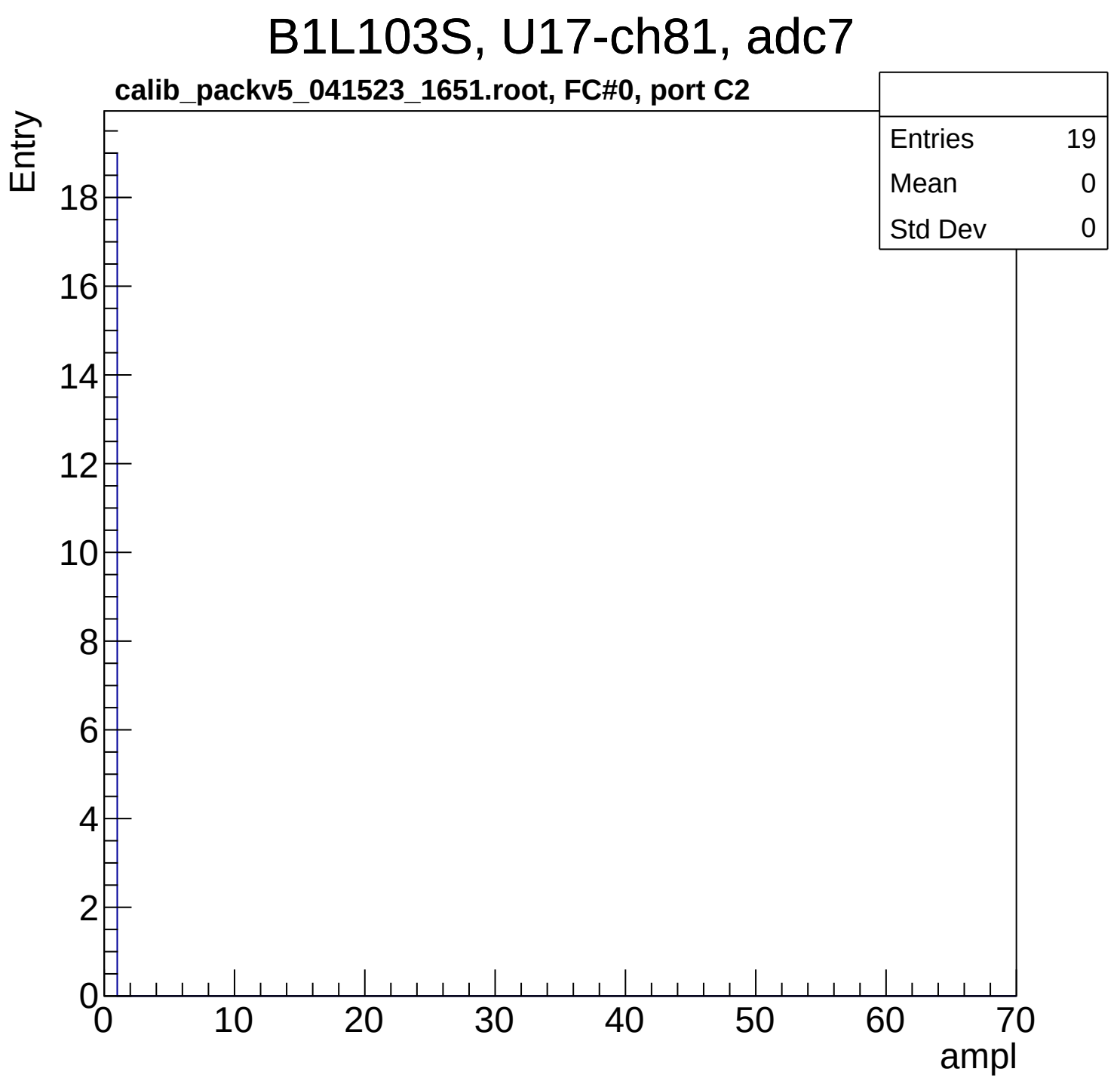
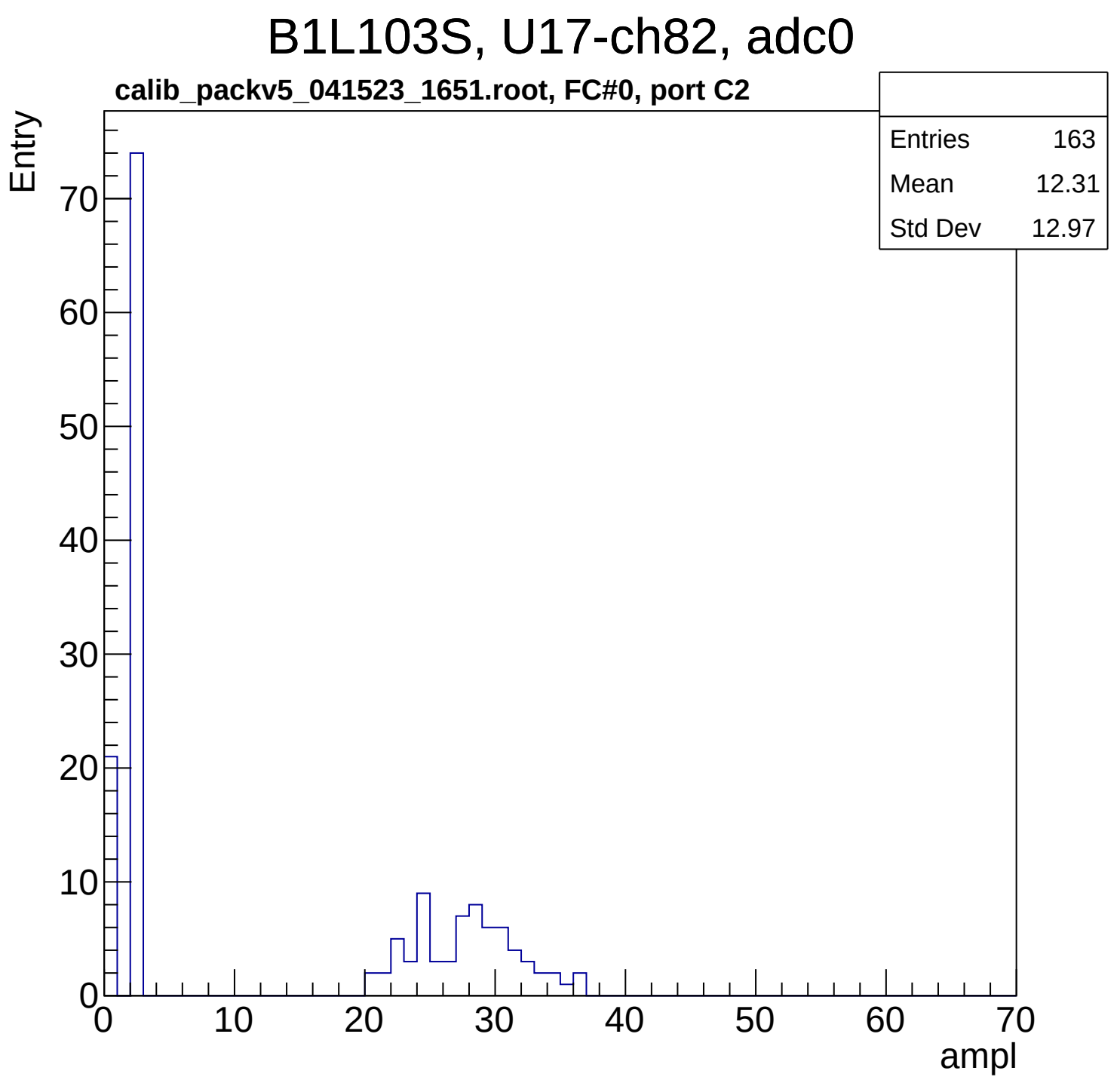
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U17-ch81, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch82, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 163
Mean 12.31
Std Dev 12.97
Entry
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10
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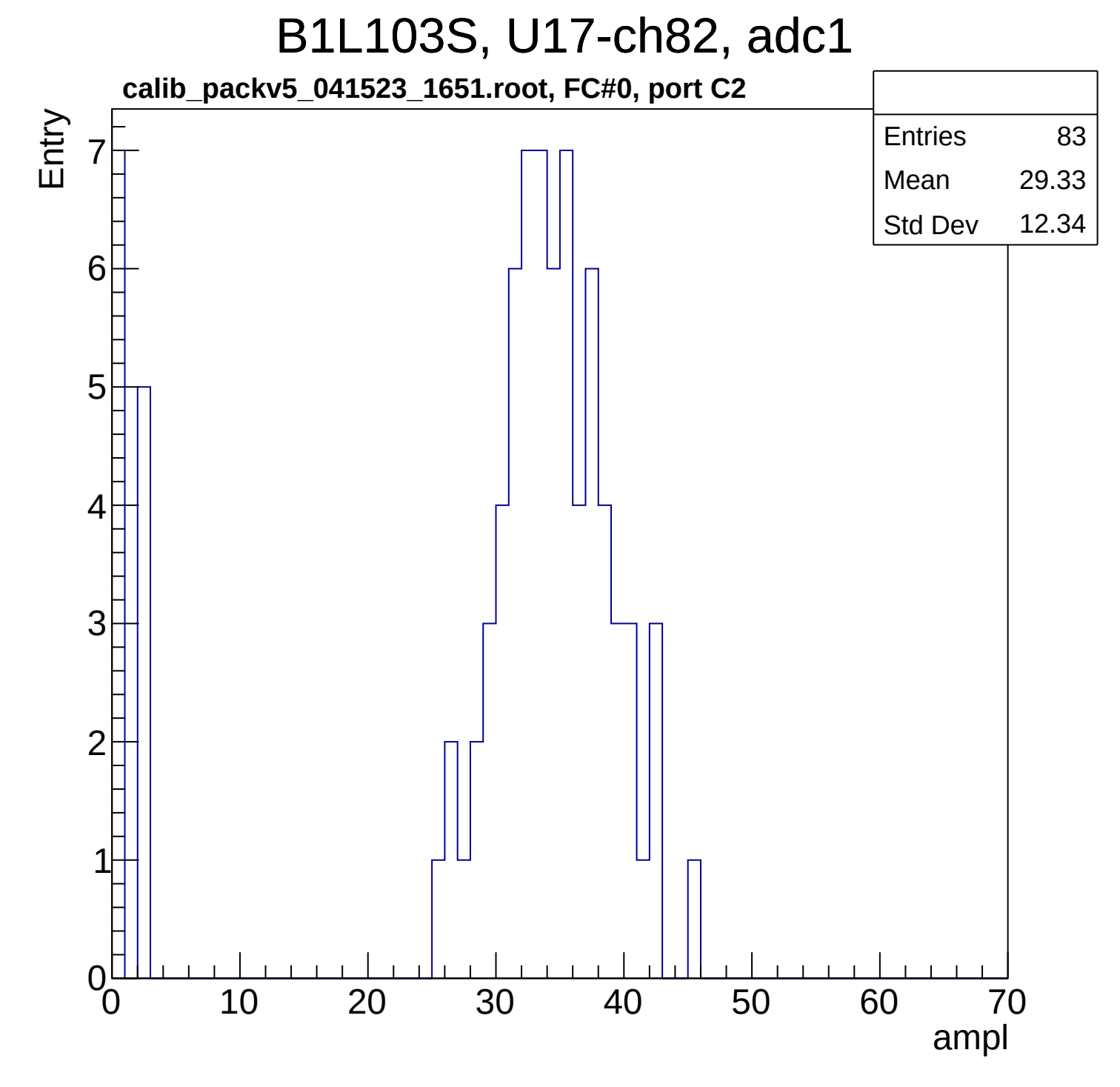
40
50
60
70
ampl


B1L103S, U17-ch82, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 29.33
Std Dev 12.34
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
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40
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60
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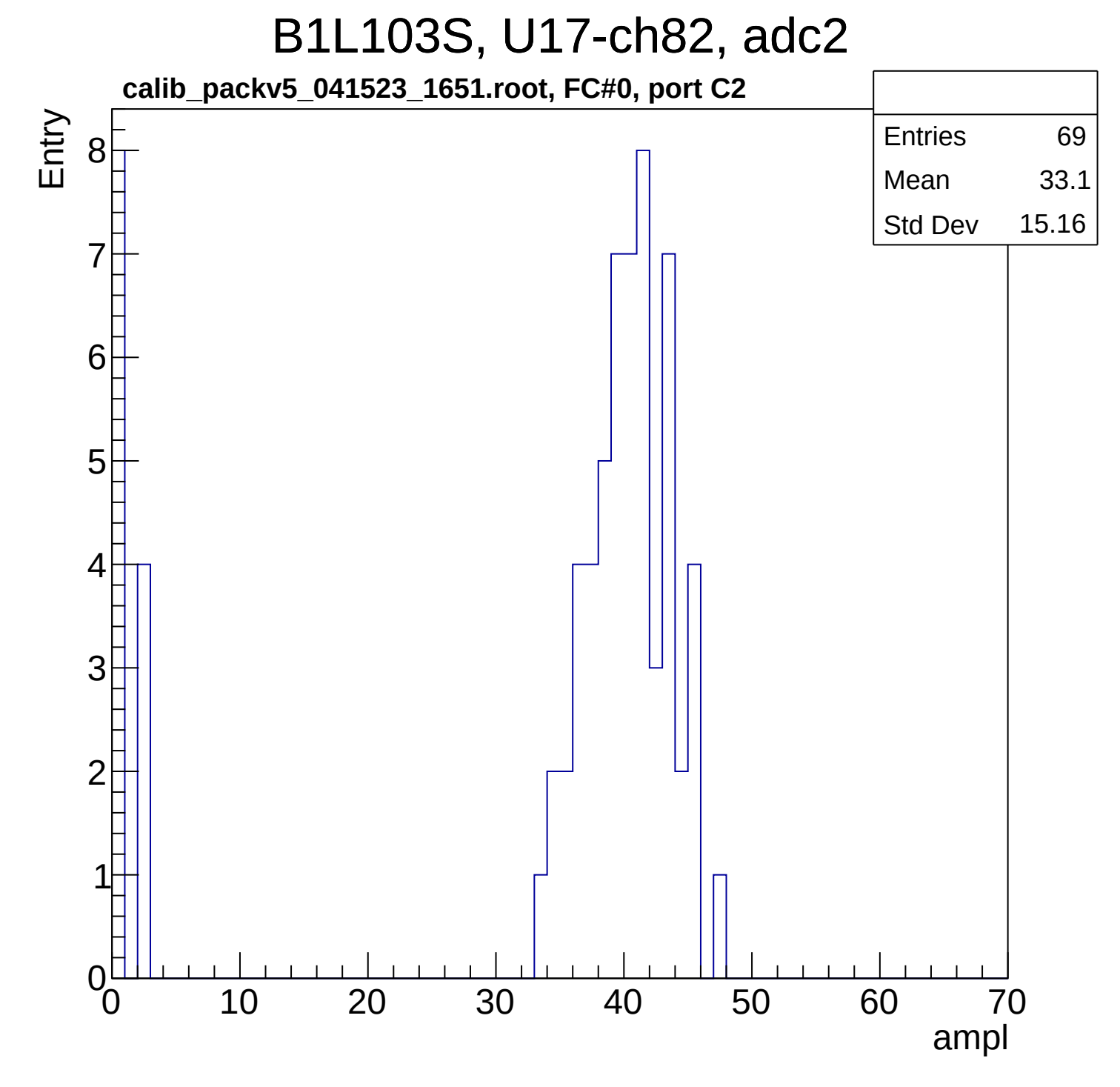
B1L103S, U17-ch82, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 33.1
Std Dev 15.16
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
30
40
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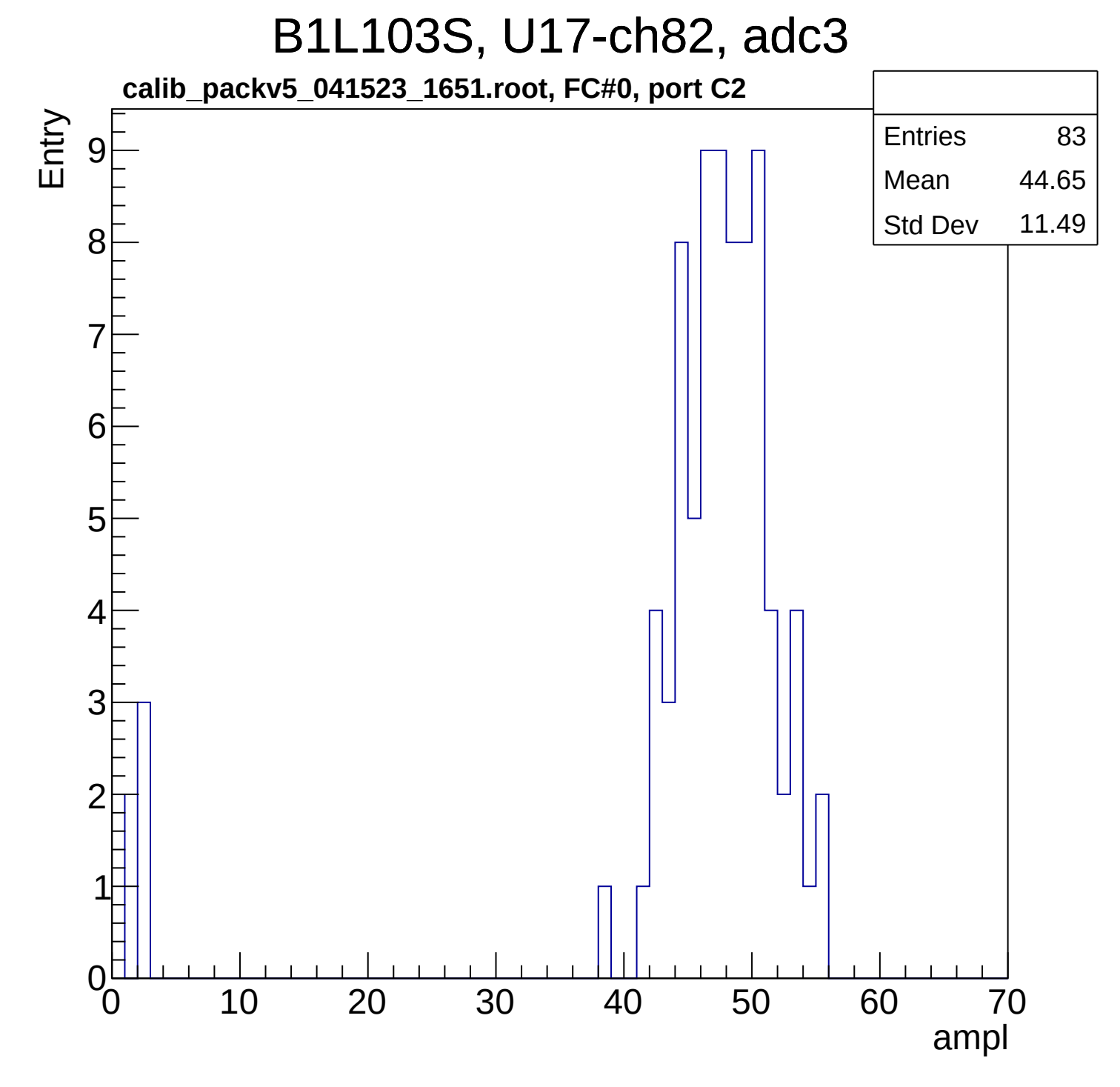
60
70


B1L103S, U17-ch82, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 44.65
Std Dev 11.49
Entry
ampl
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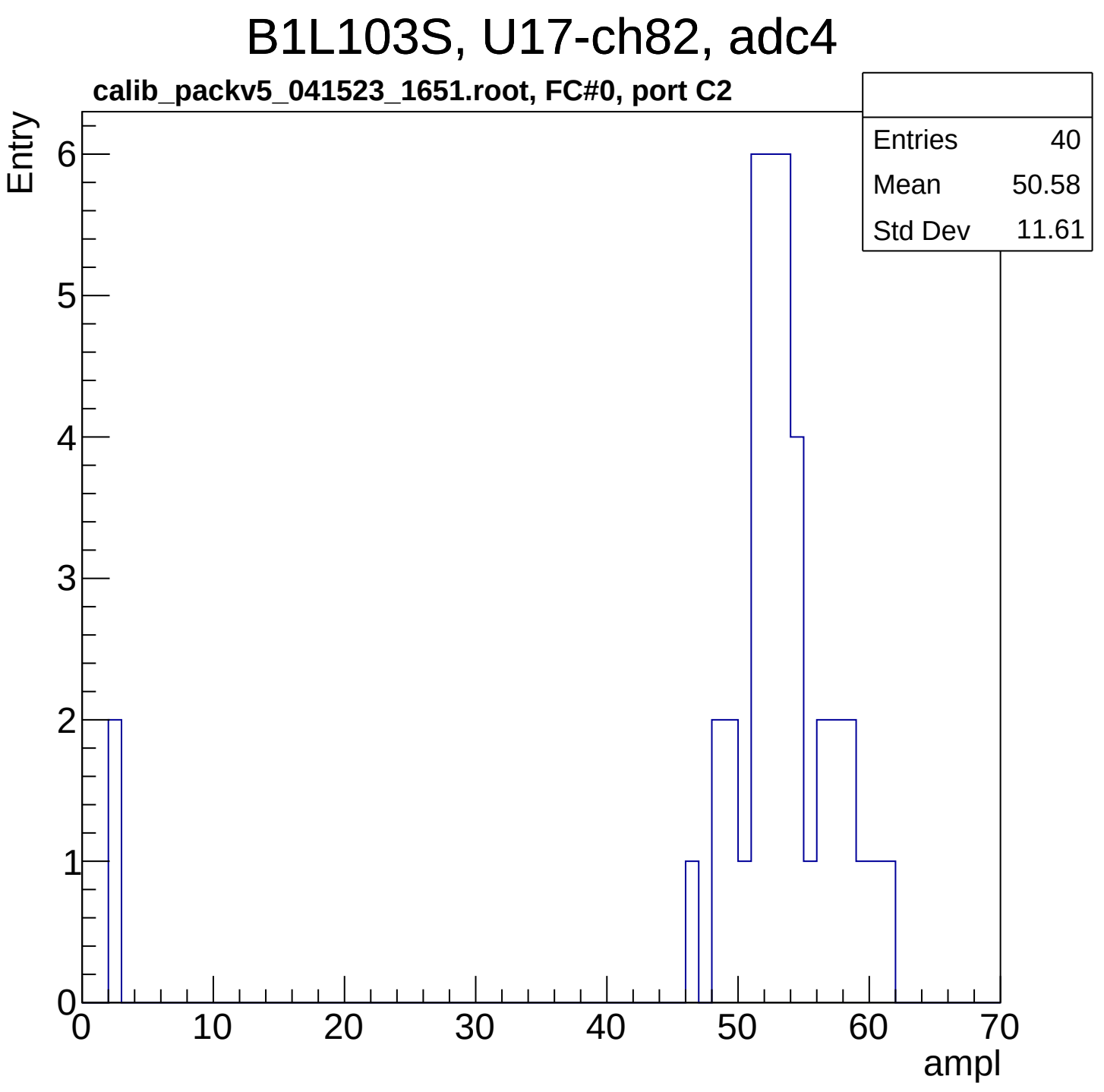
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9


B1L103S, U17-ch82, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 40
Mean 50.58
Std Dev 11.61
Entry
ampl
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0
10
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30
40
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60
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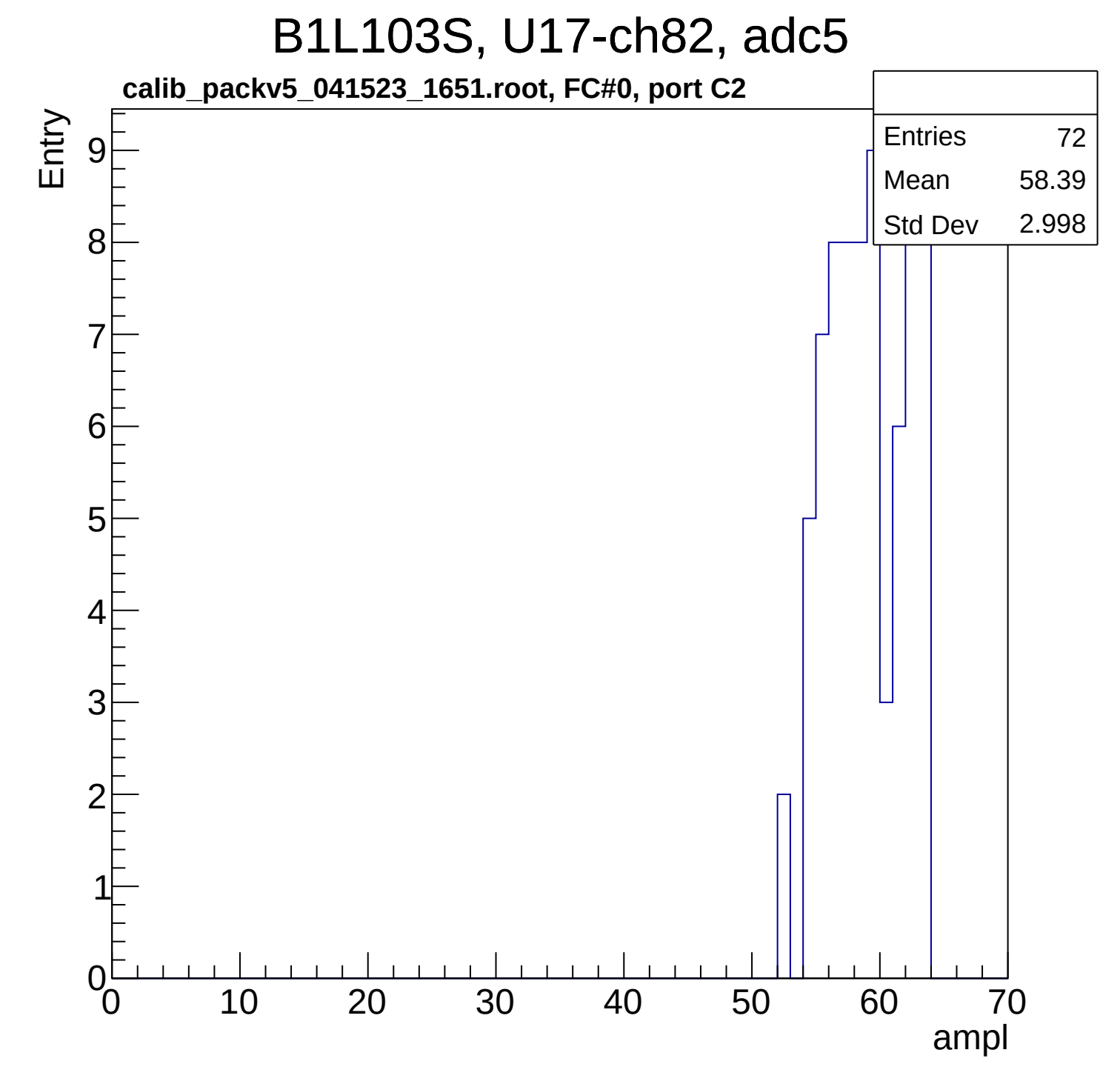
B1L103S, U17-ch82, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 58.39
Std Dev 2.998
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
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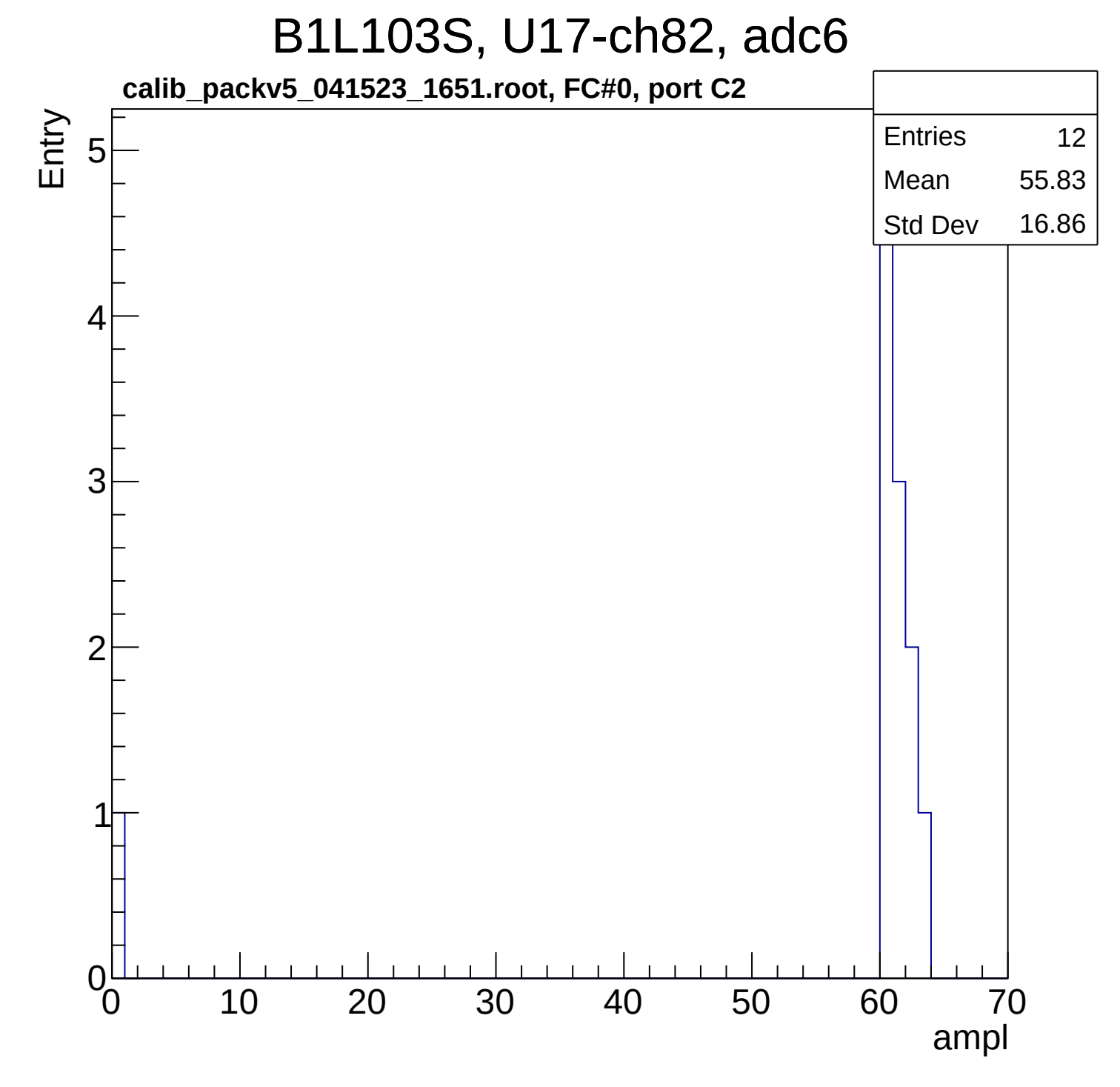
B1L103S, U17-ch82, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 55.83
Std Dev 16.86
Entry
ampl
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1
2
3
4
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0
10
20
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40
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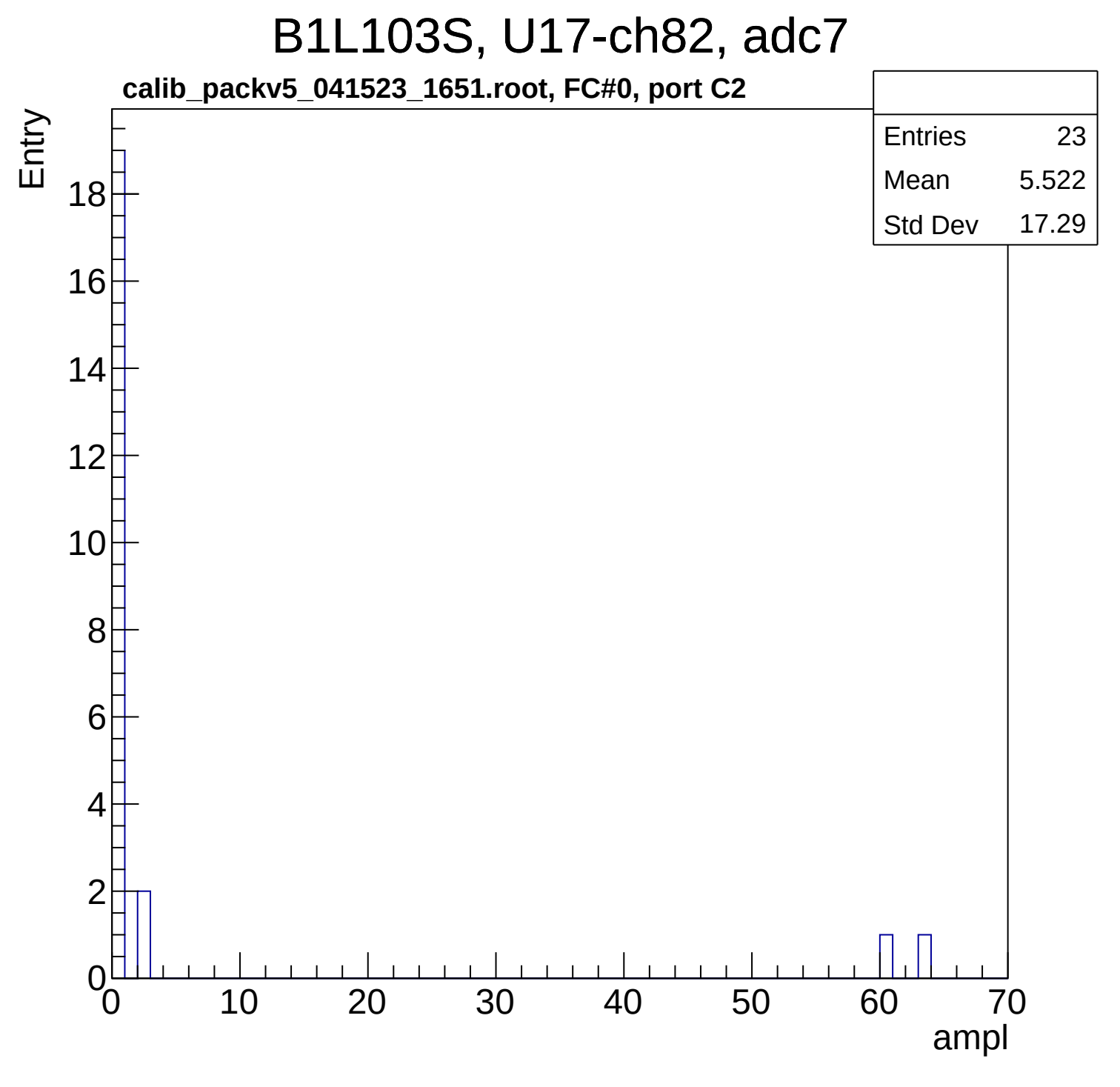
B1L103S, U17-ch82, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 23
Mean 5.522
Std Dev 17.29
Entry
ampl
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4
6
8
10
12
14
16
18
0
10
20
30
40
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60
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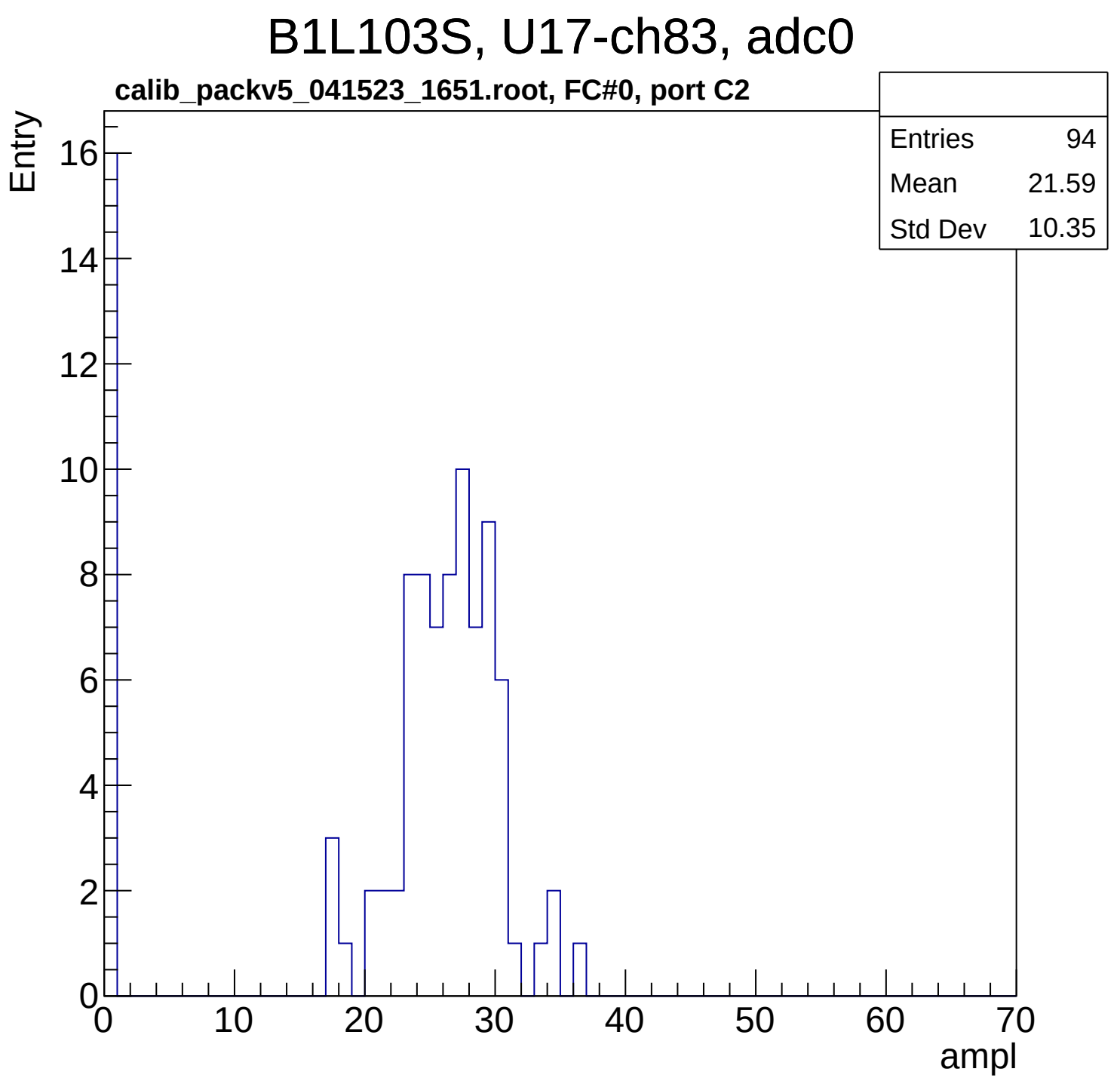
B1L103S, U17-ch83, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 94
Mean 21.59
Std Dev 10.35
Entry
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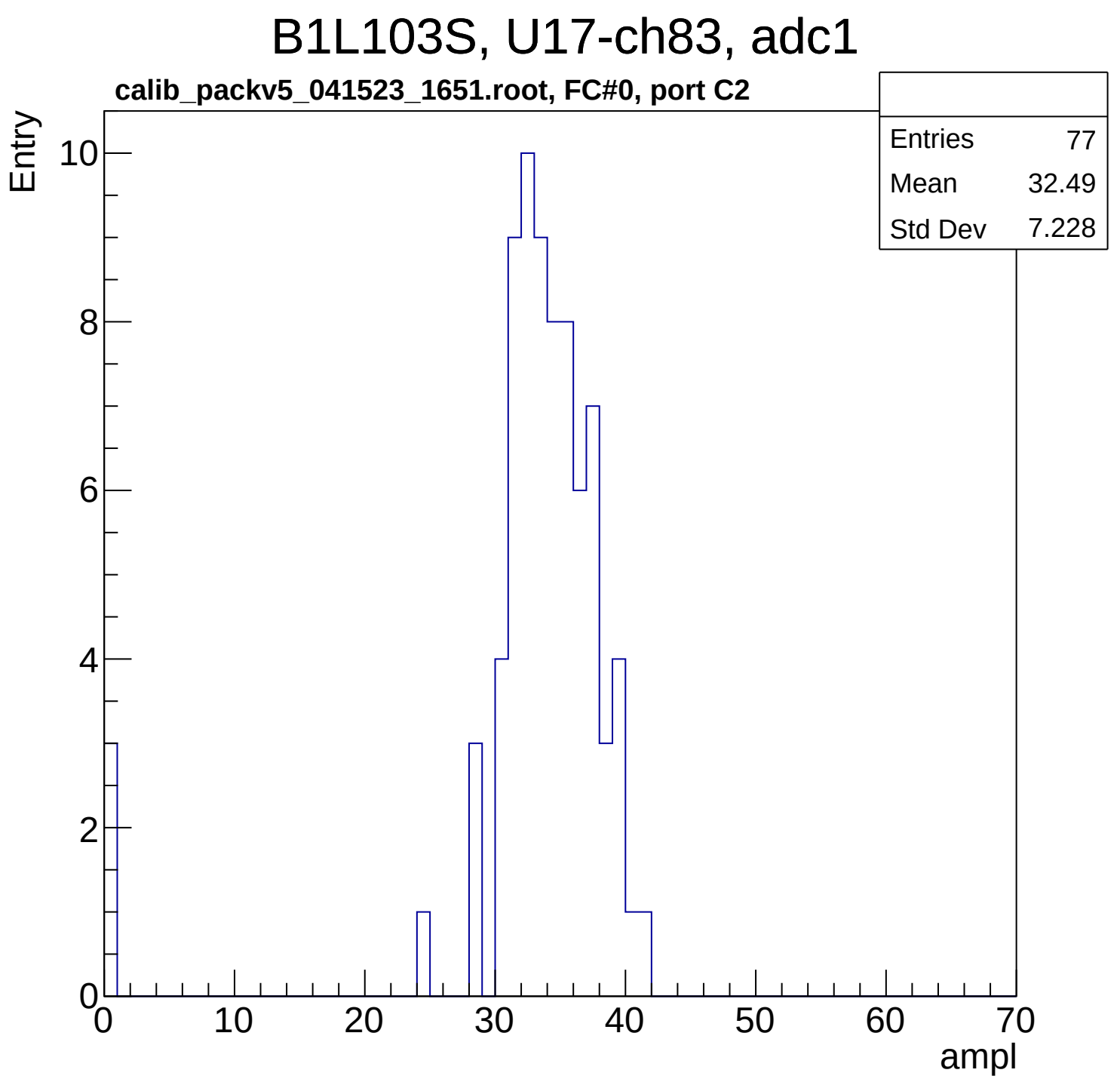
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch83, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 32.49
Std Dev 7.228
Entry
ampl
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4
6
8
10
0
10
20
30
40
50
60
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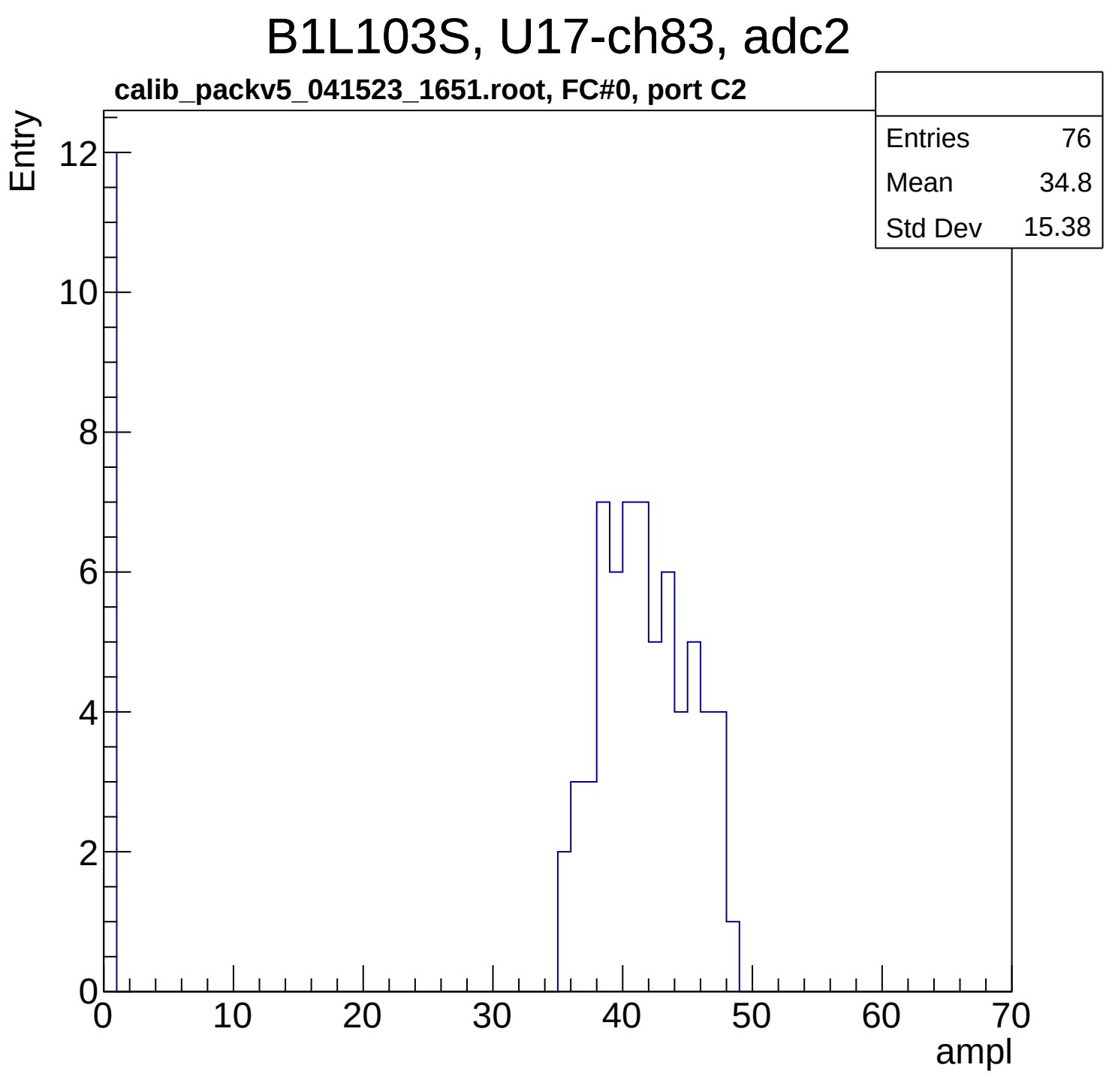
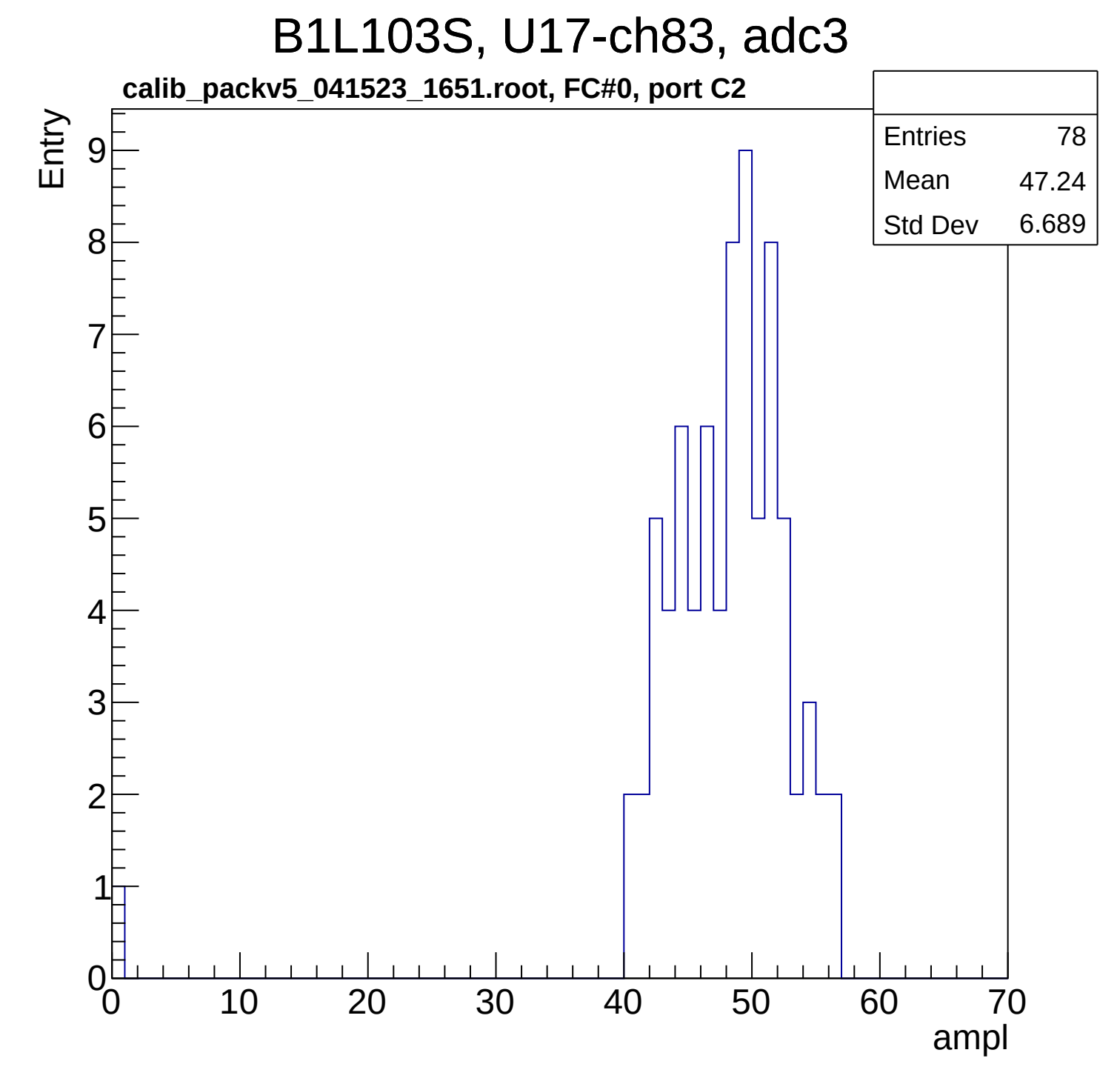

B1L103S, U17-ch83, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 34.8
Std Dev 15.38
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch83, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 47.24
Std Dev 6.689
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
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20
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40
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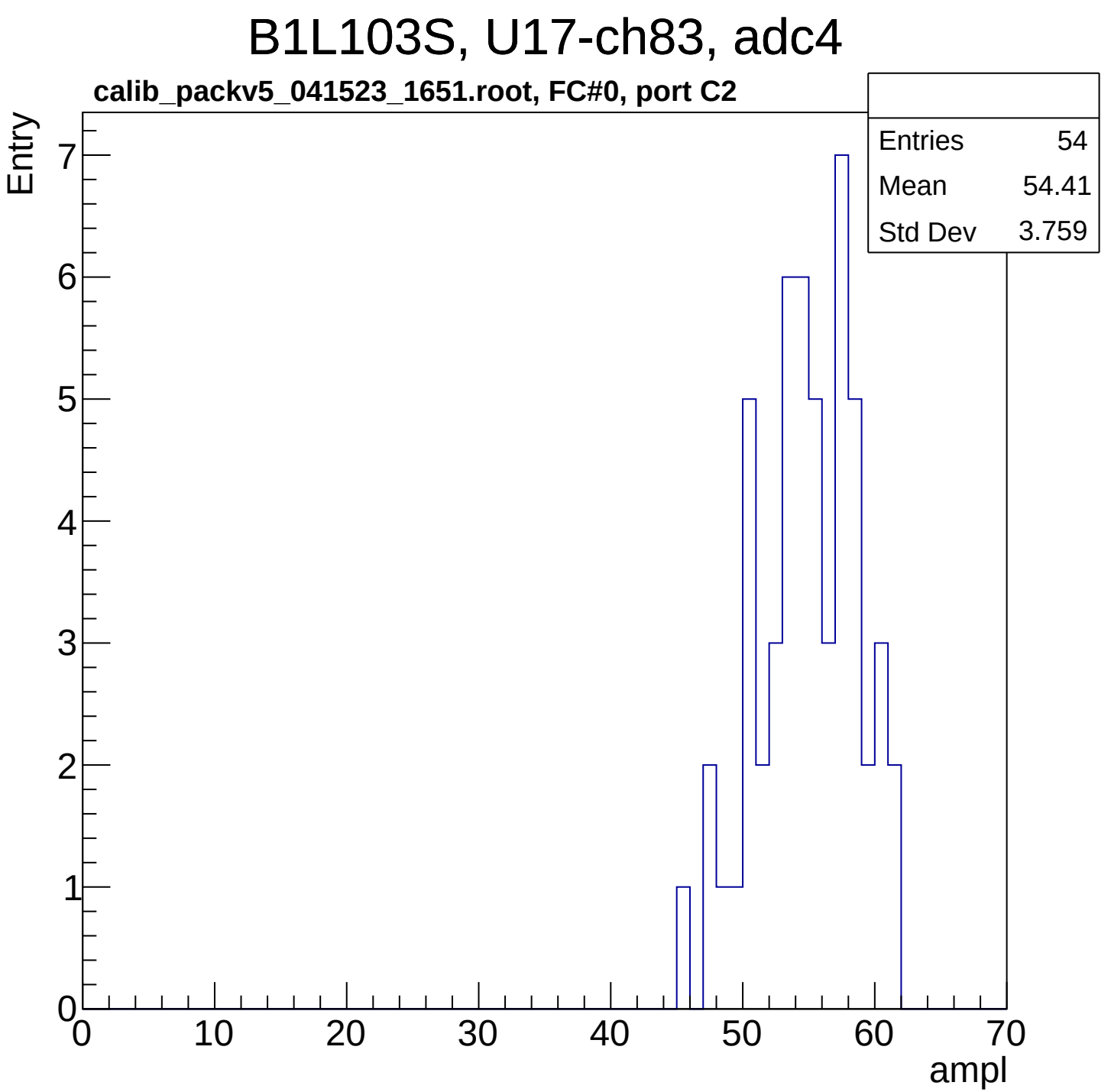
60
70


B1L103S, U17-ch83, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 54.41
Std Dev 3.759
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
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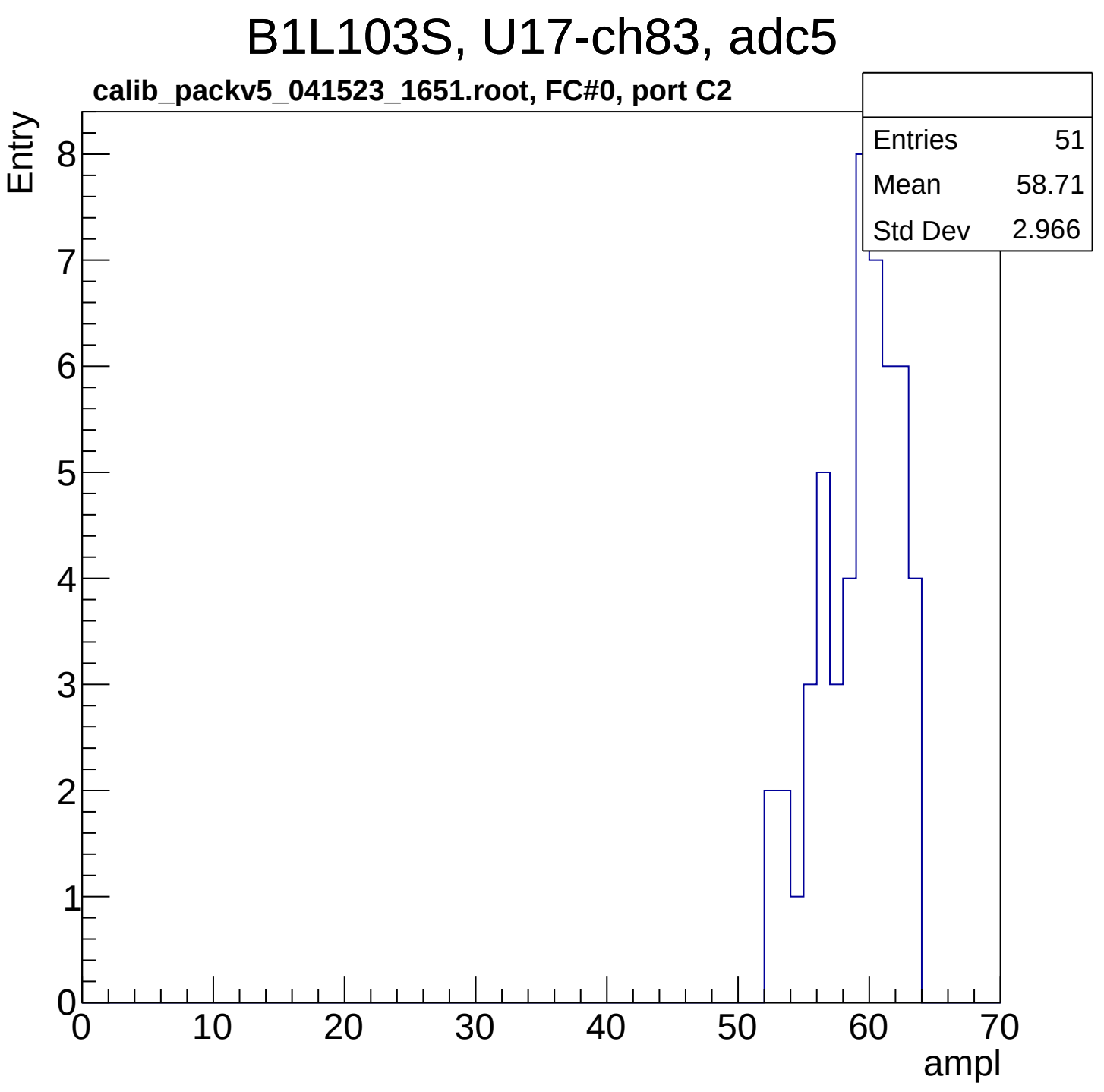
40
50
60
70


B1L103S, U17-ch83, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 58.71
Std Dev 2.966
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
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60
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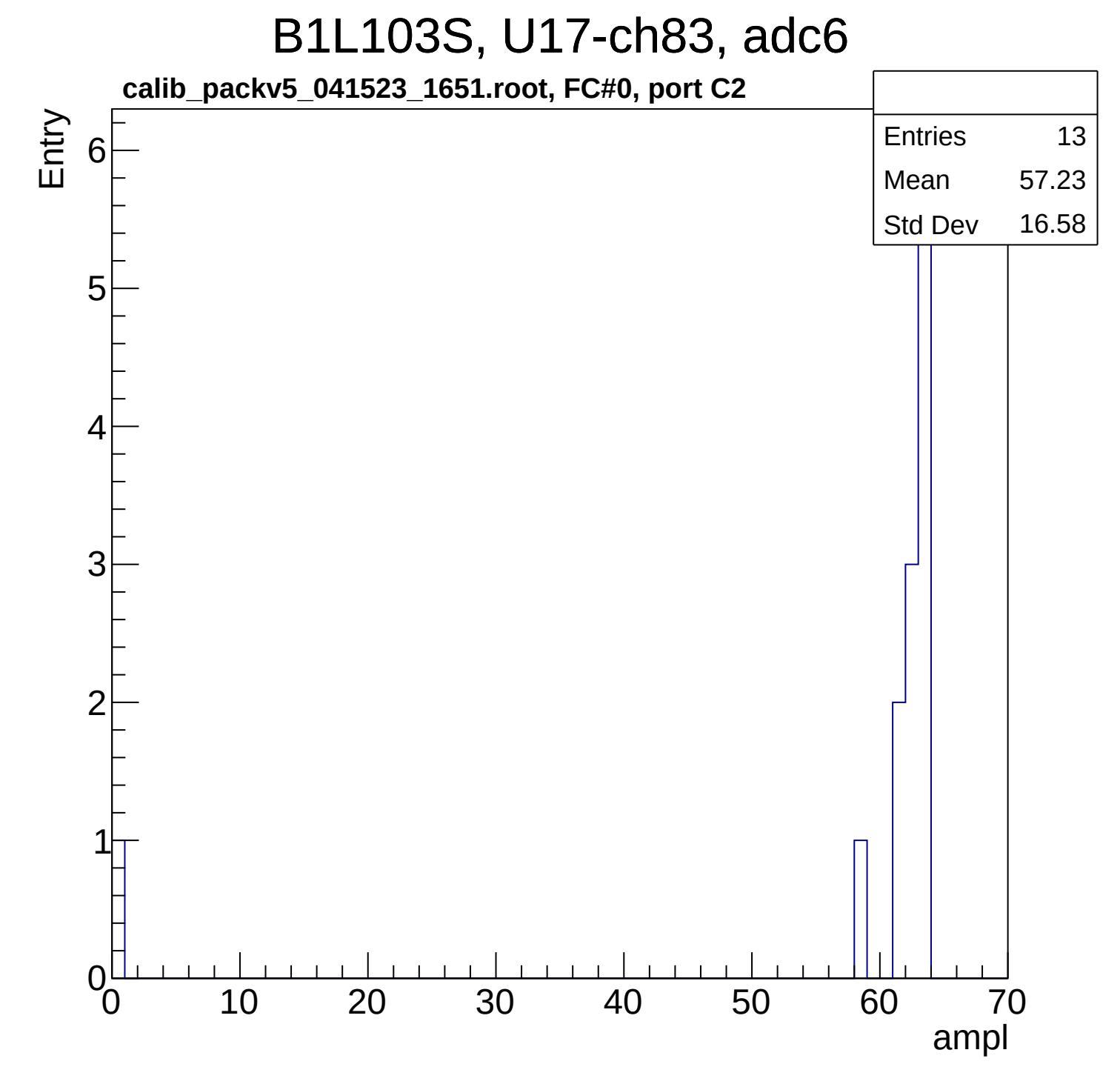
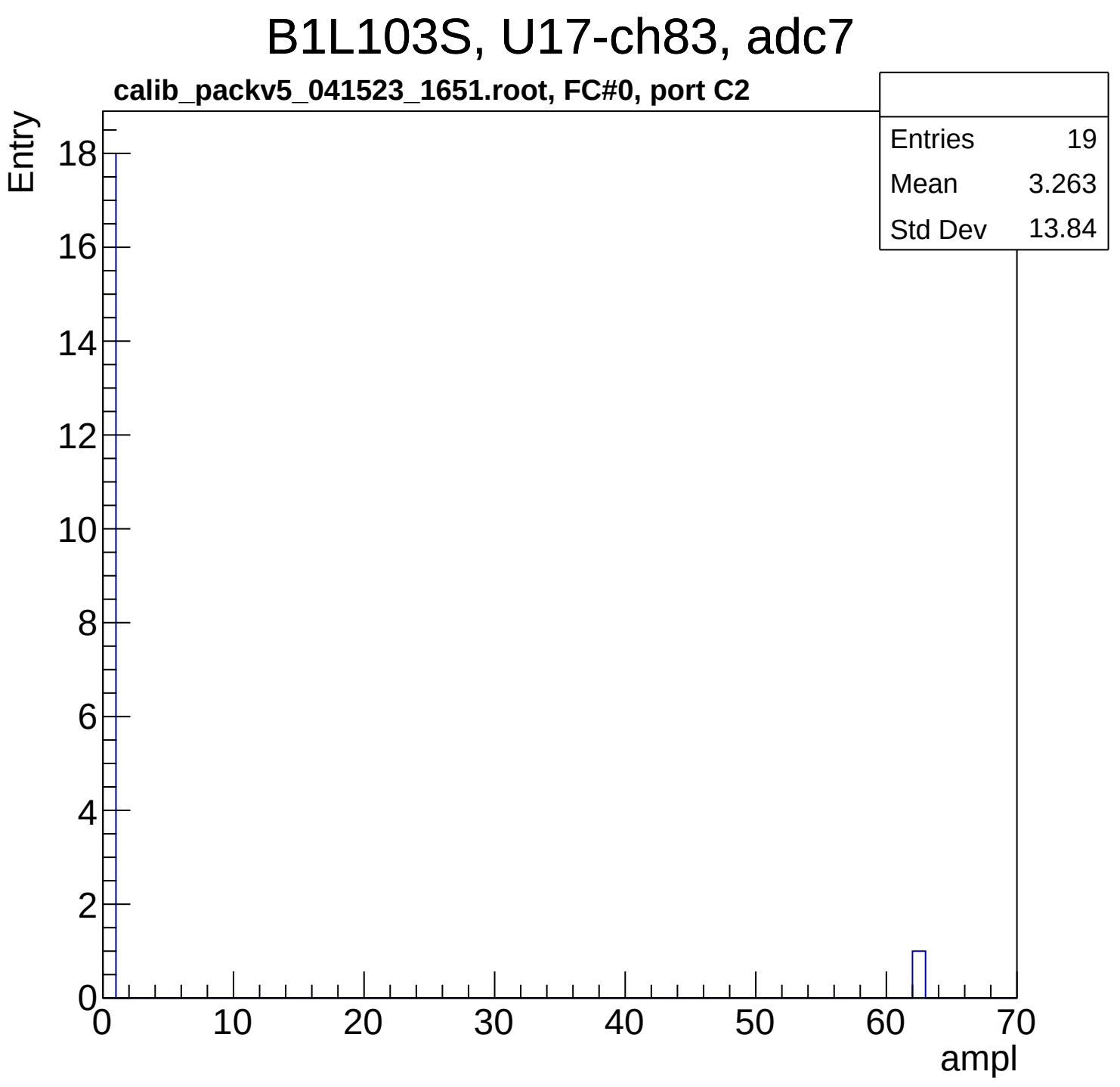
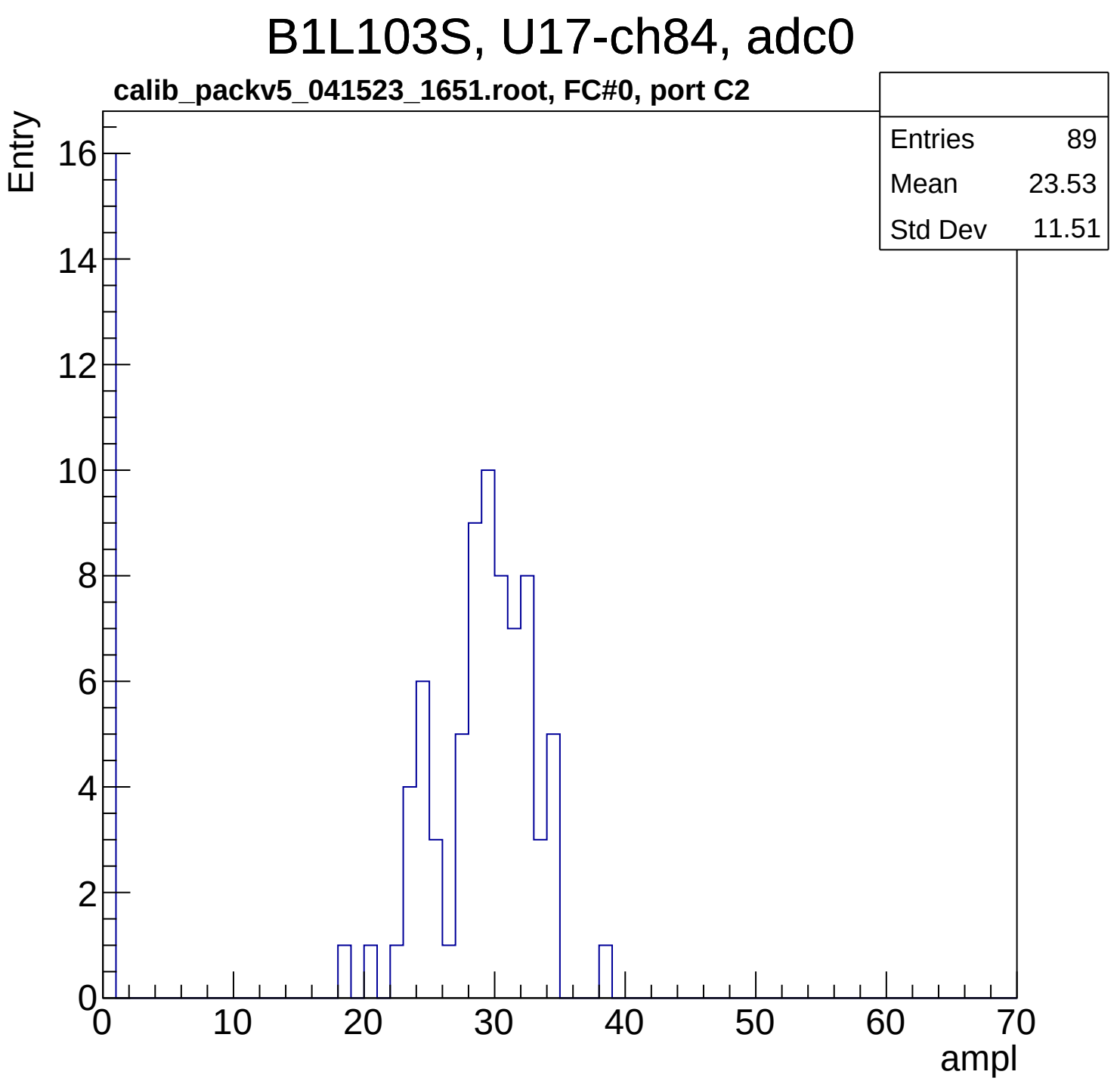
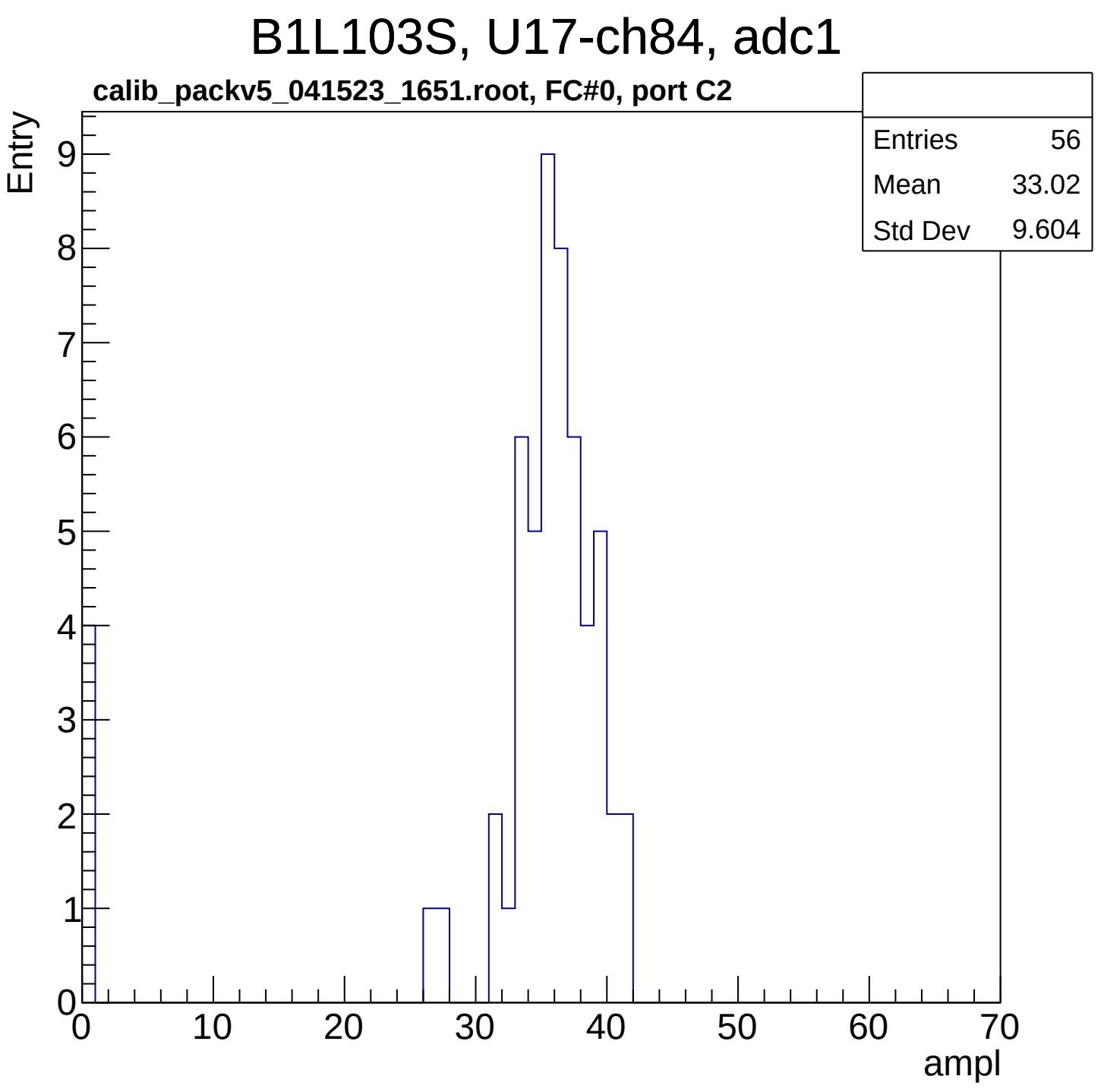

B1L103S, U17-ch83, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 13
Mean 57.23
Std Dev 16.58
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U17-ch83, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 3.263
Std Dev 13.84
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch84, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 89
Mean 23.53
Std Dev 11.51
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70


B1L103S, U17-ch84, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 33.02
Std Dev 9.604
Entry
ampl
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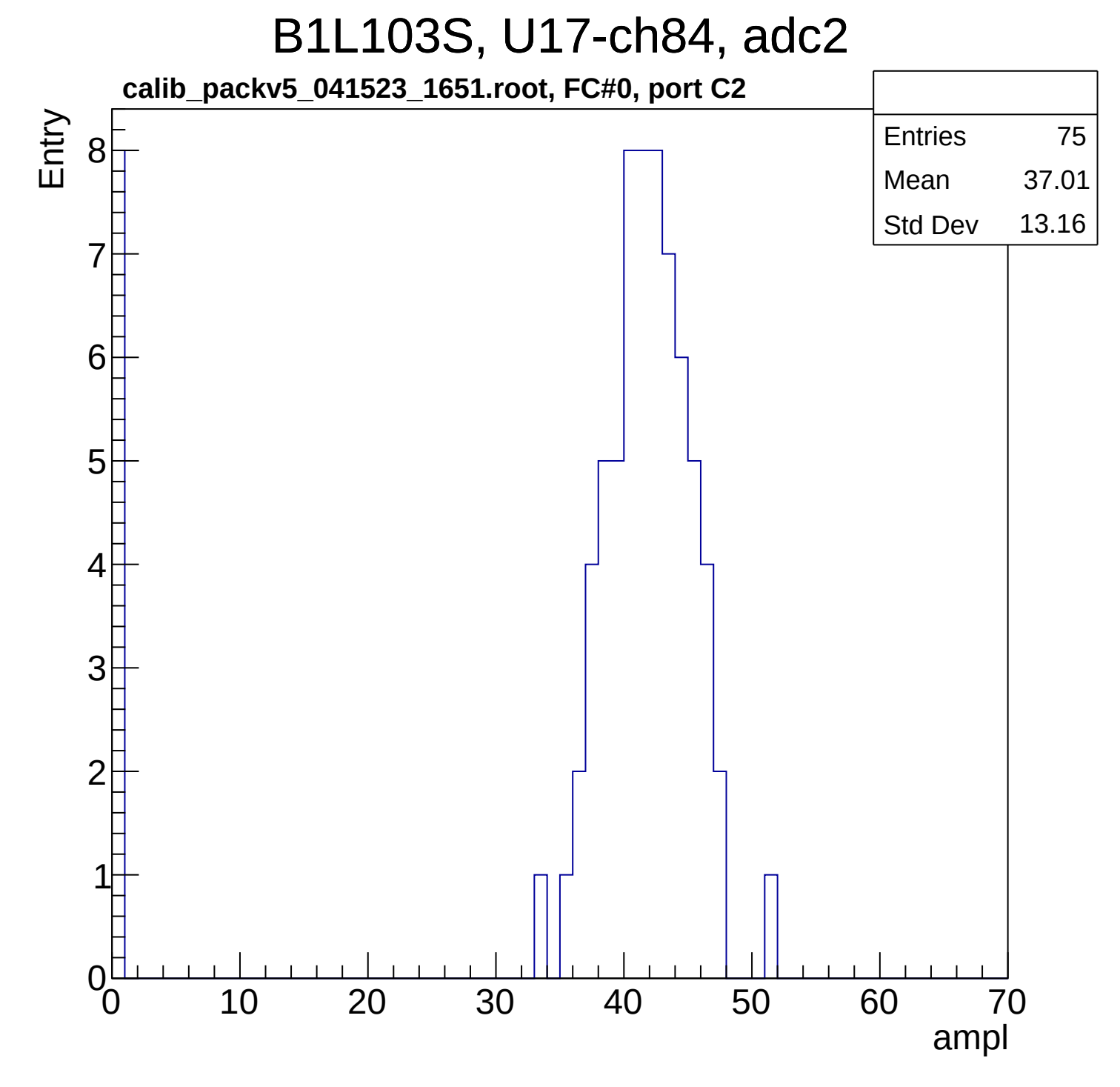
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U17-ch84, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 37.01
Std Dev 13.16
Entry
ampl
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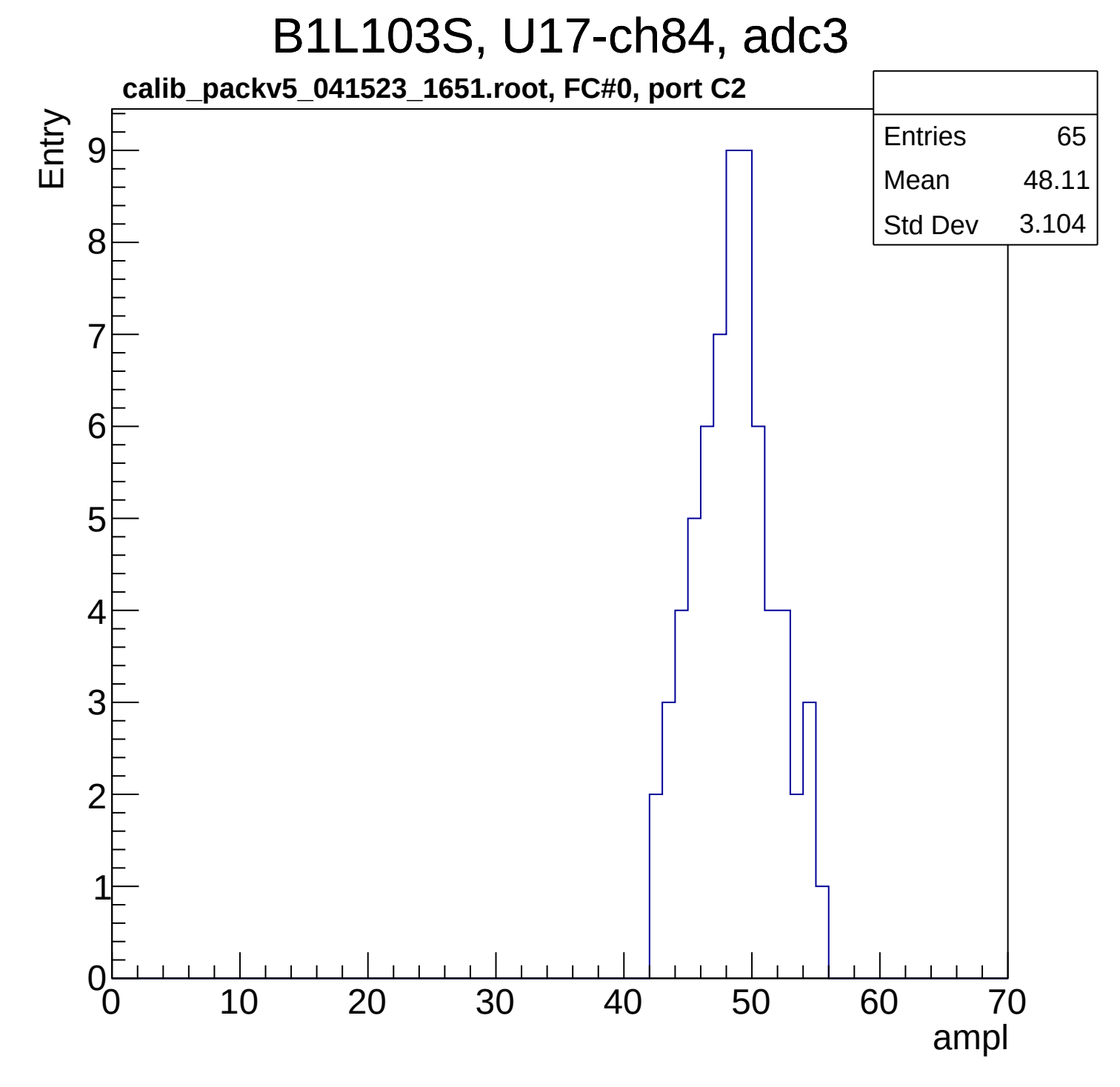
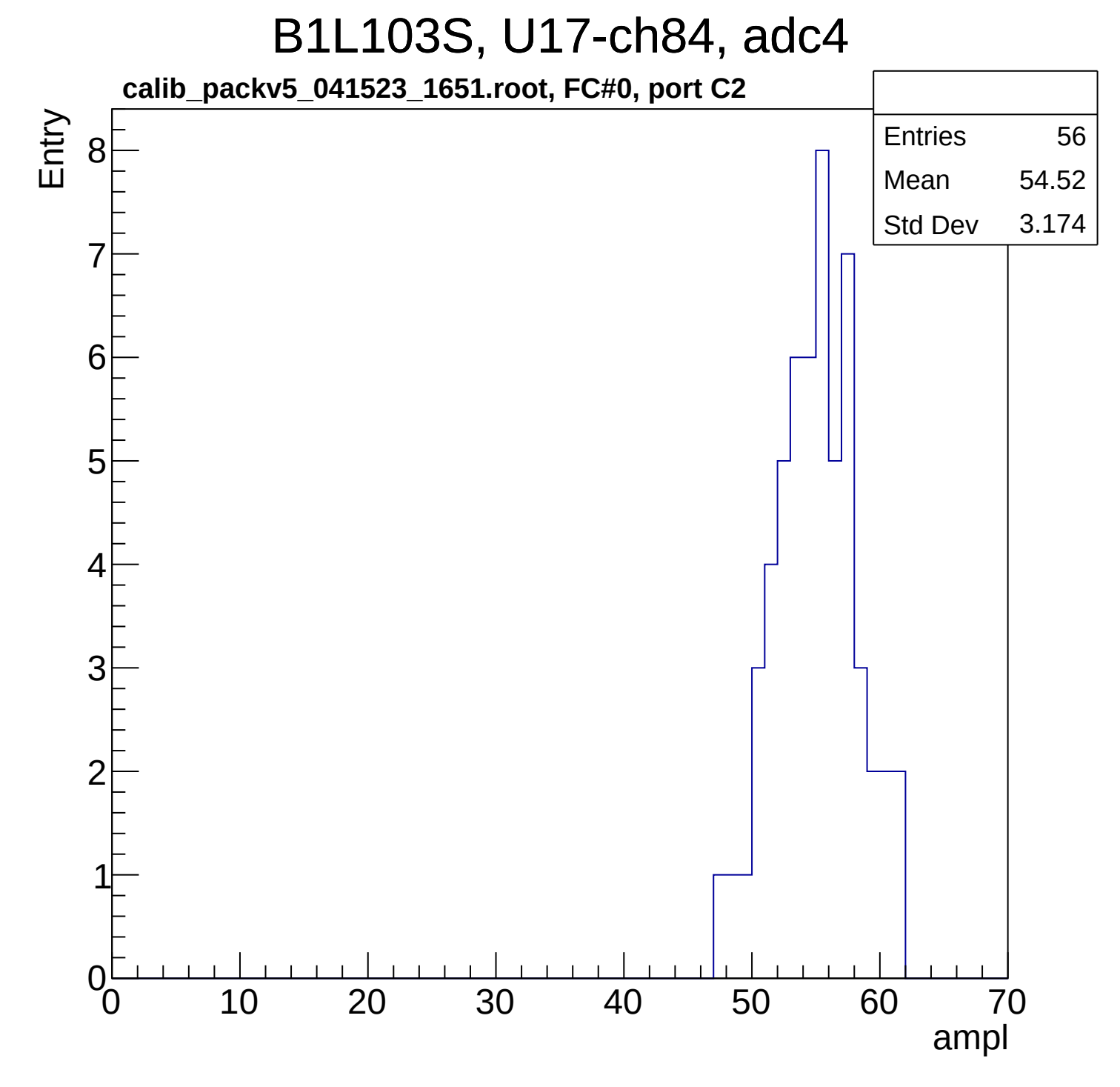
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U17-ch84, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 48.11
Std Dev 3.104
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U17-ch84, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 54.52
Std Dev 3.174
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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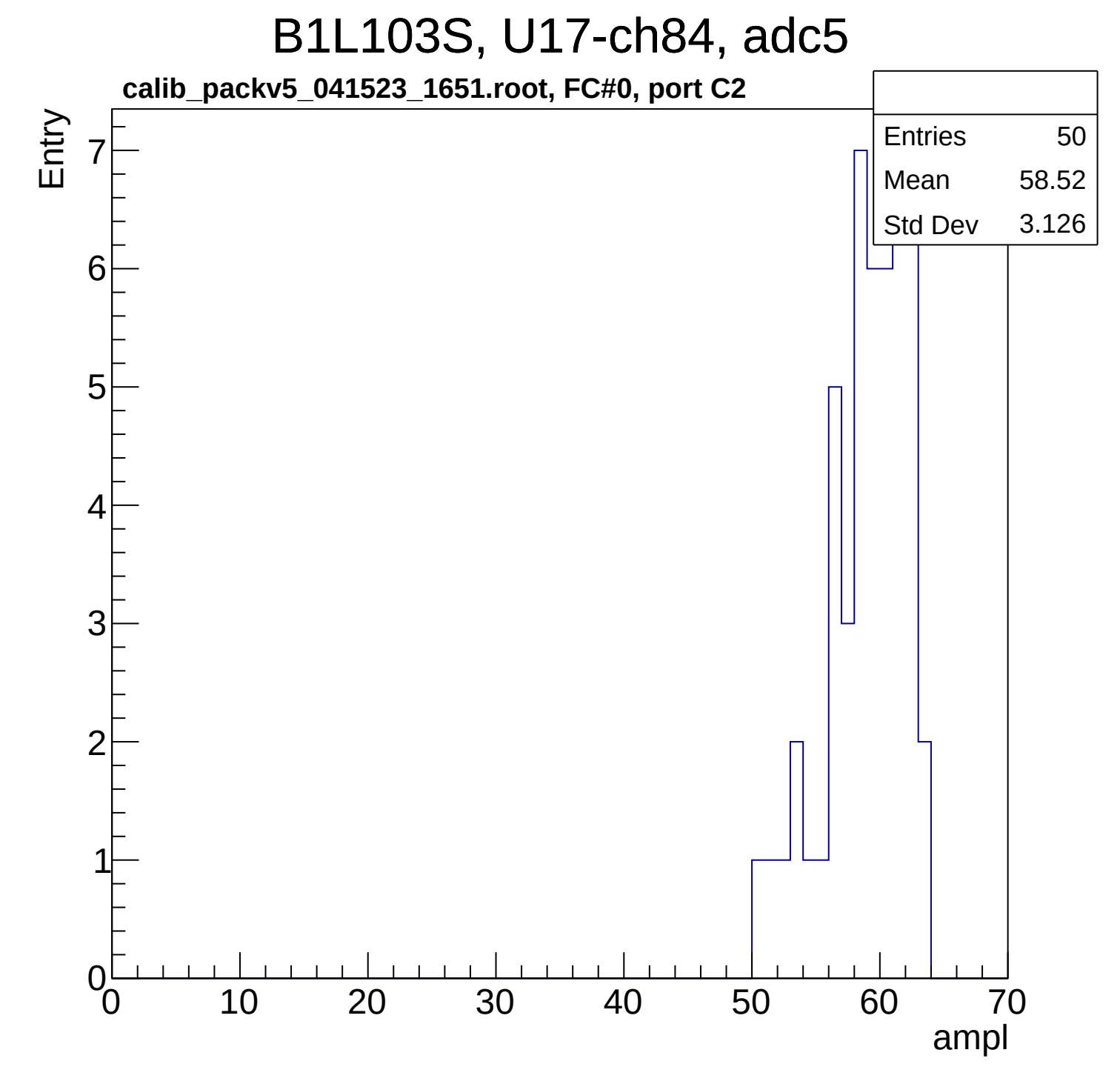
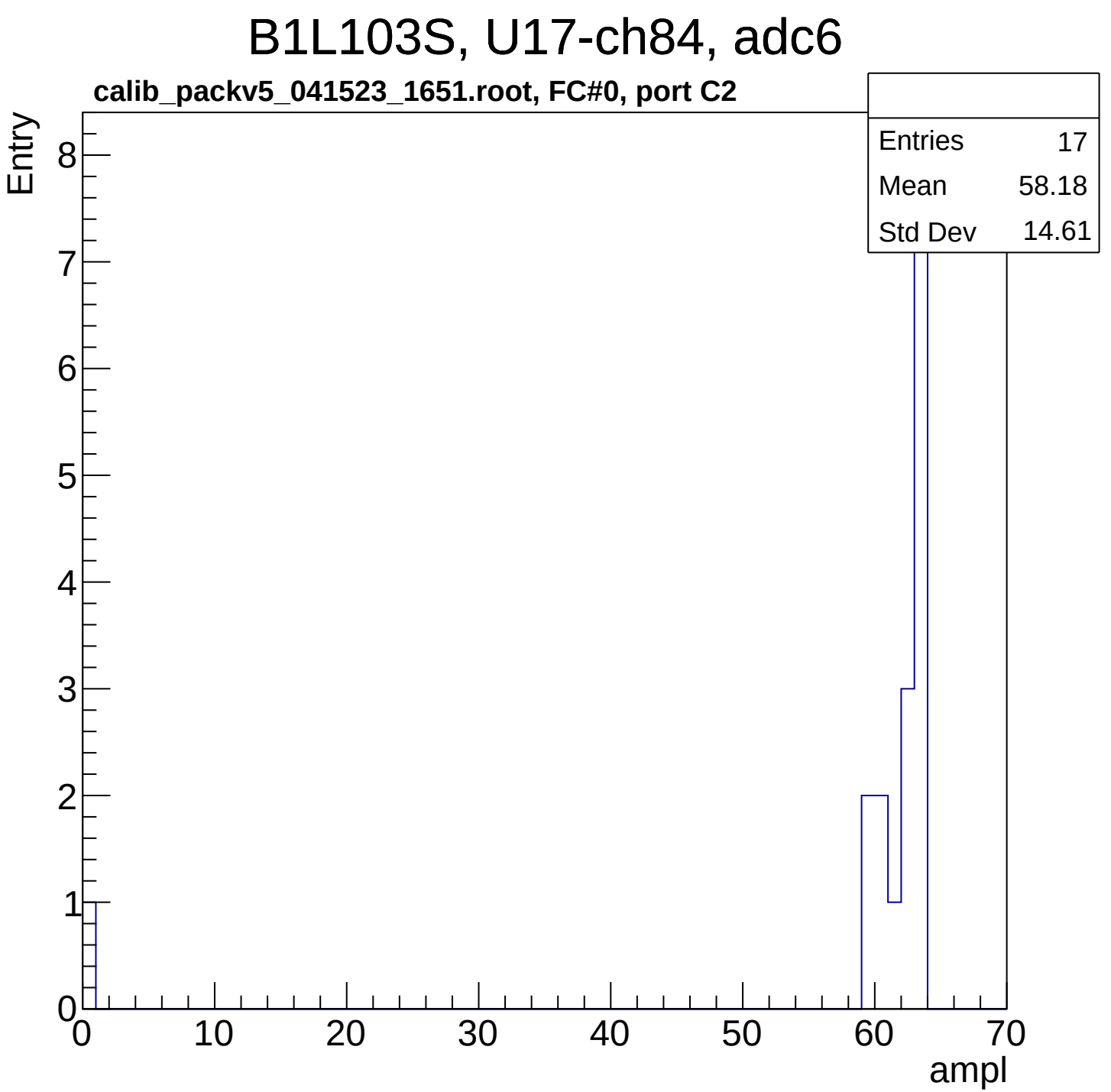

B1L103S, U17-ch84, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 58.52
Std Dev 3.126
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U17-ch84, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 17
Mean 58.18
Std Dev 14.61
Entry
ampl
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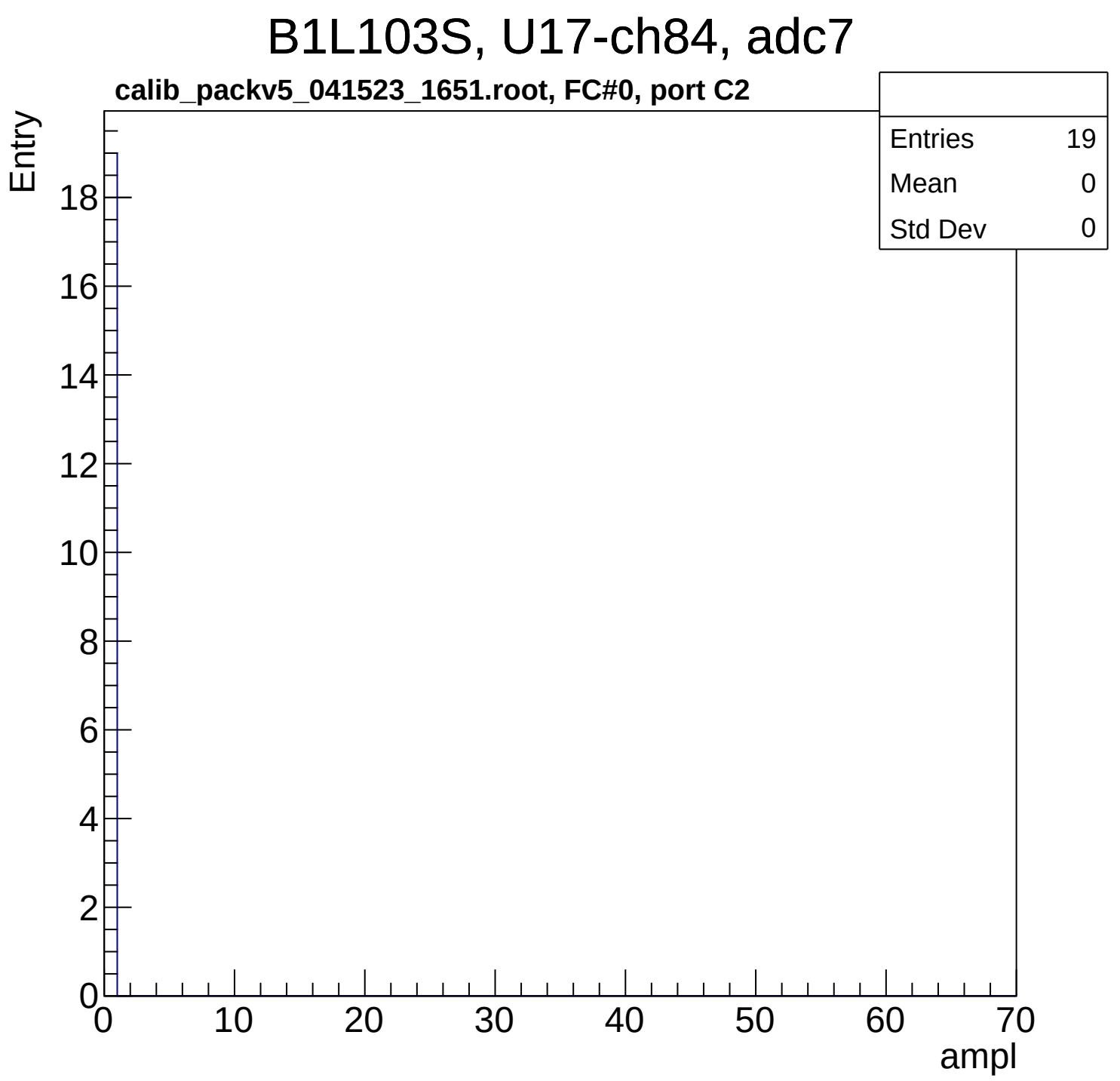
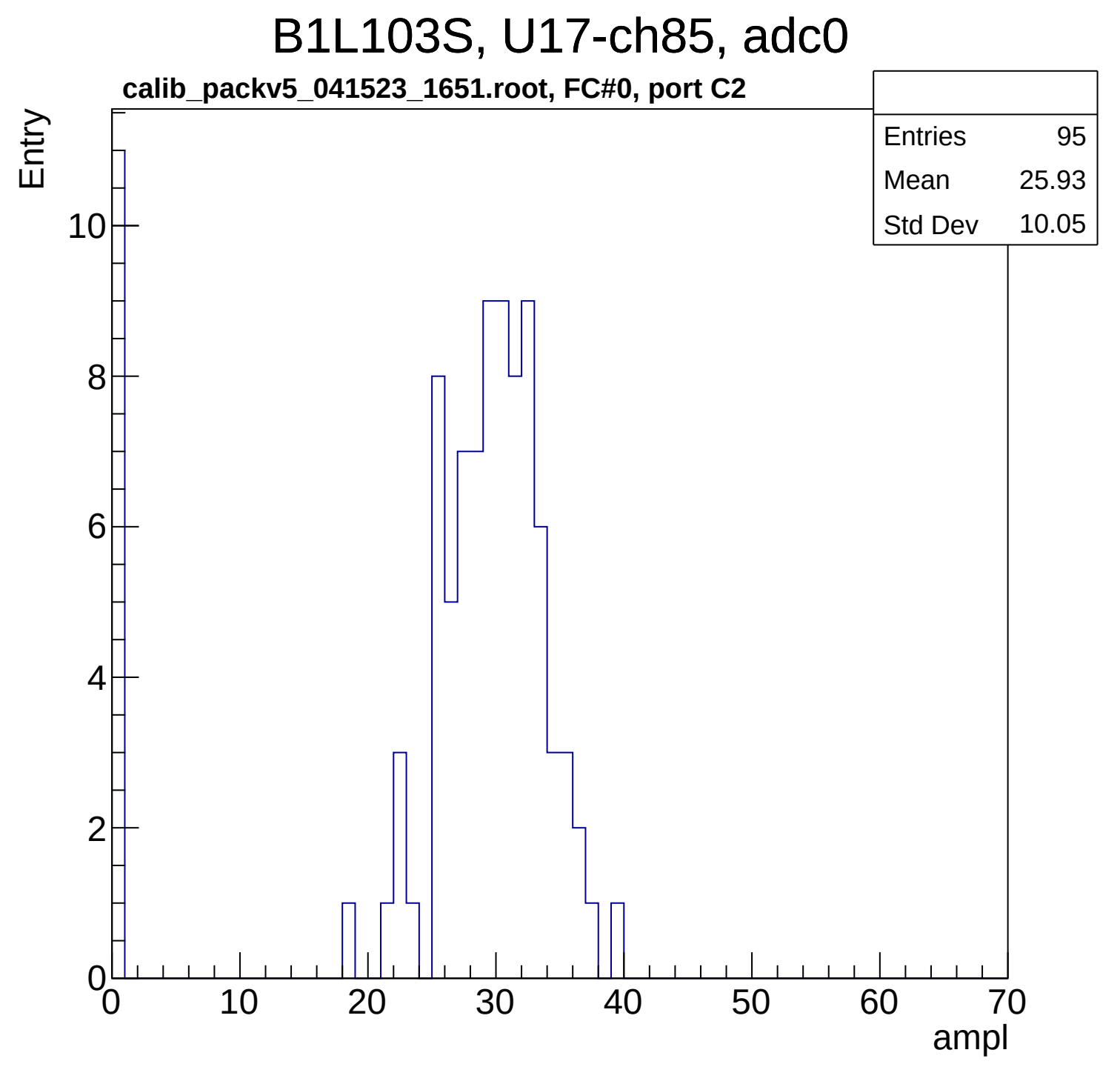
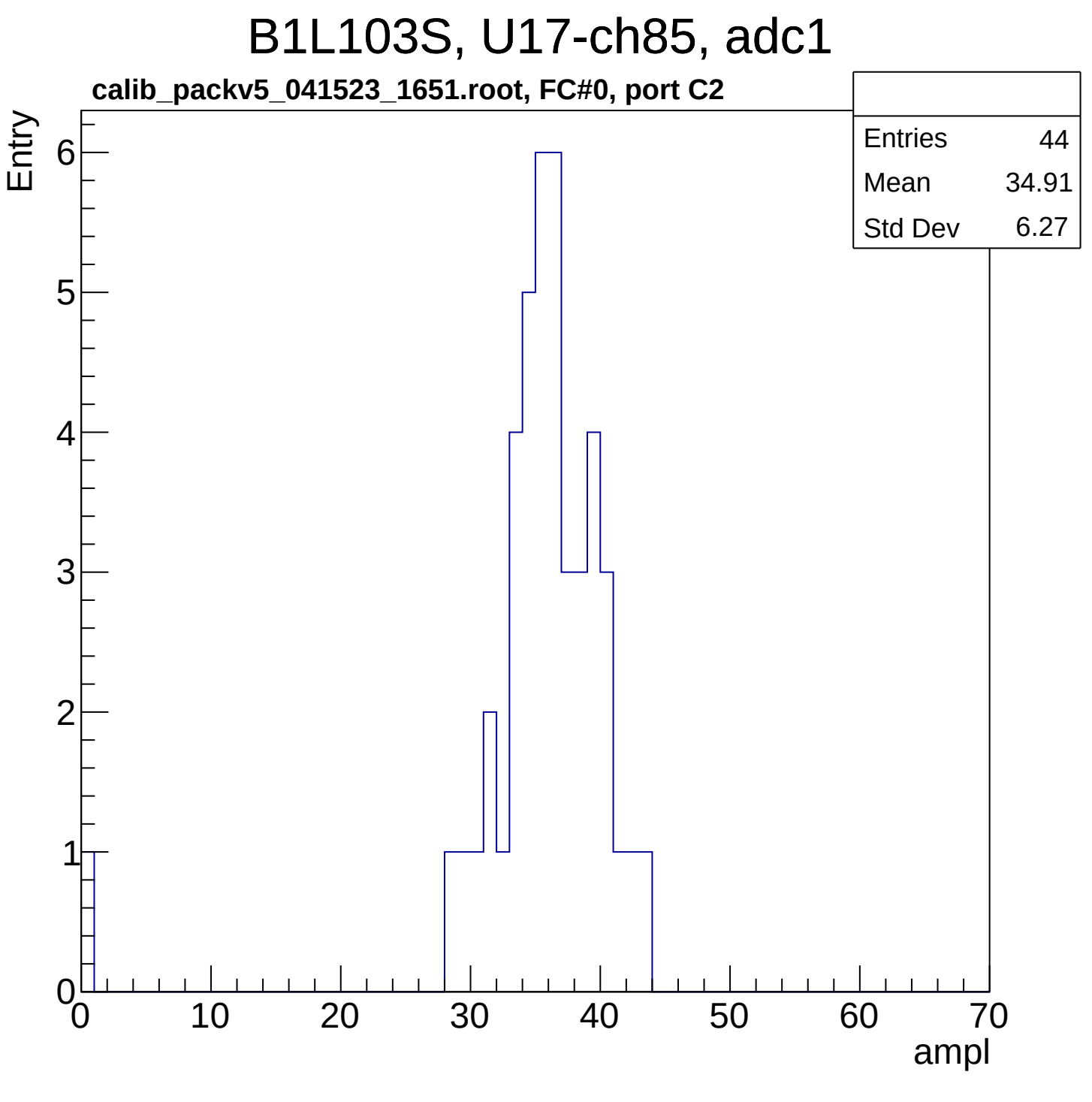
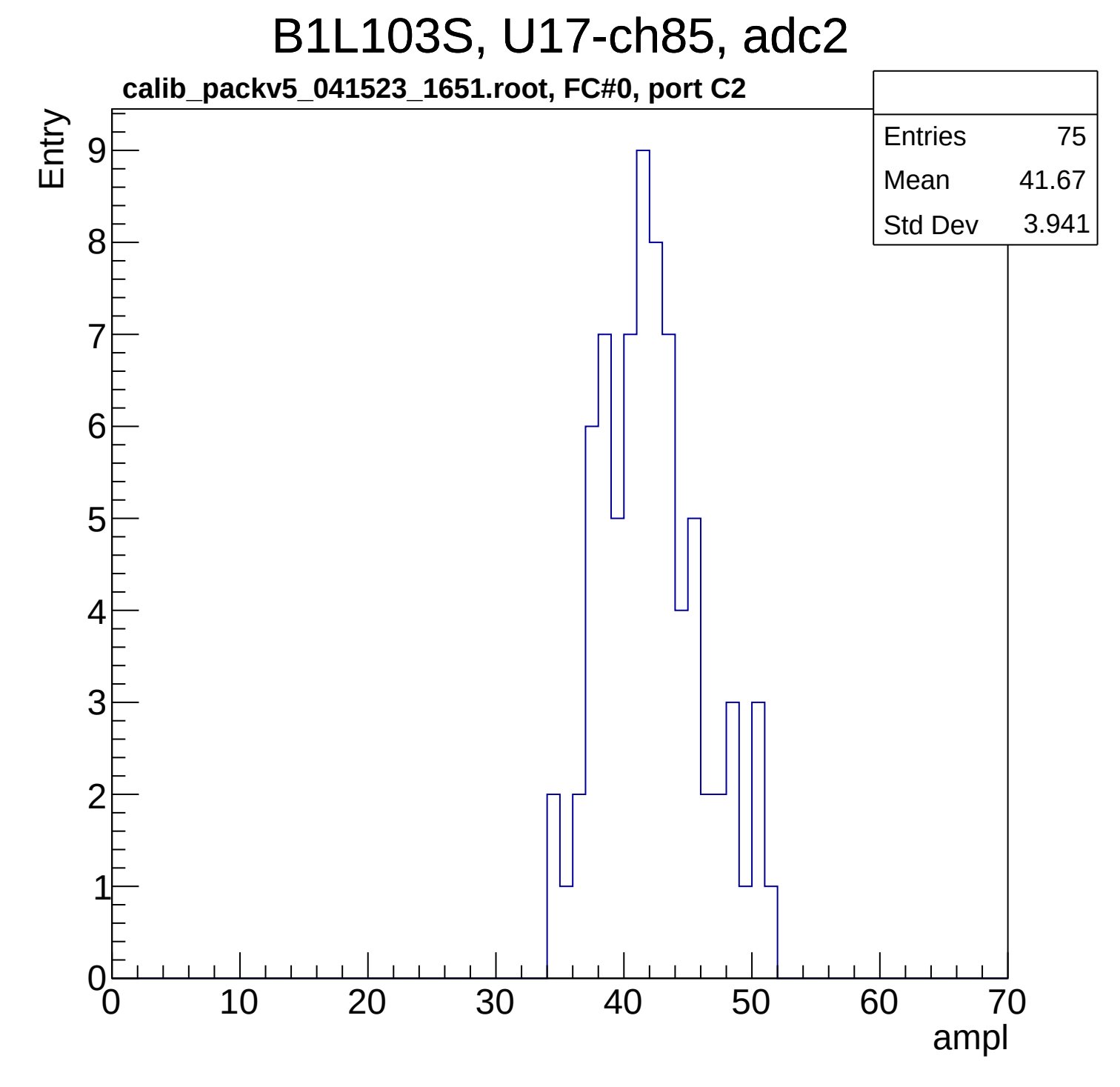
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U17-ch84, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch85, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 95
Mean 25.93
Std Dev 10.05
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch85, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 34.91
Std Dev 6.27
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch85, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 41.67
Std Dev 3.941
Entry
ampl
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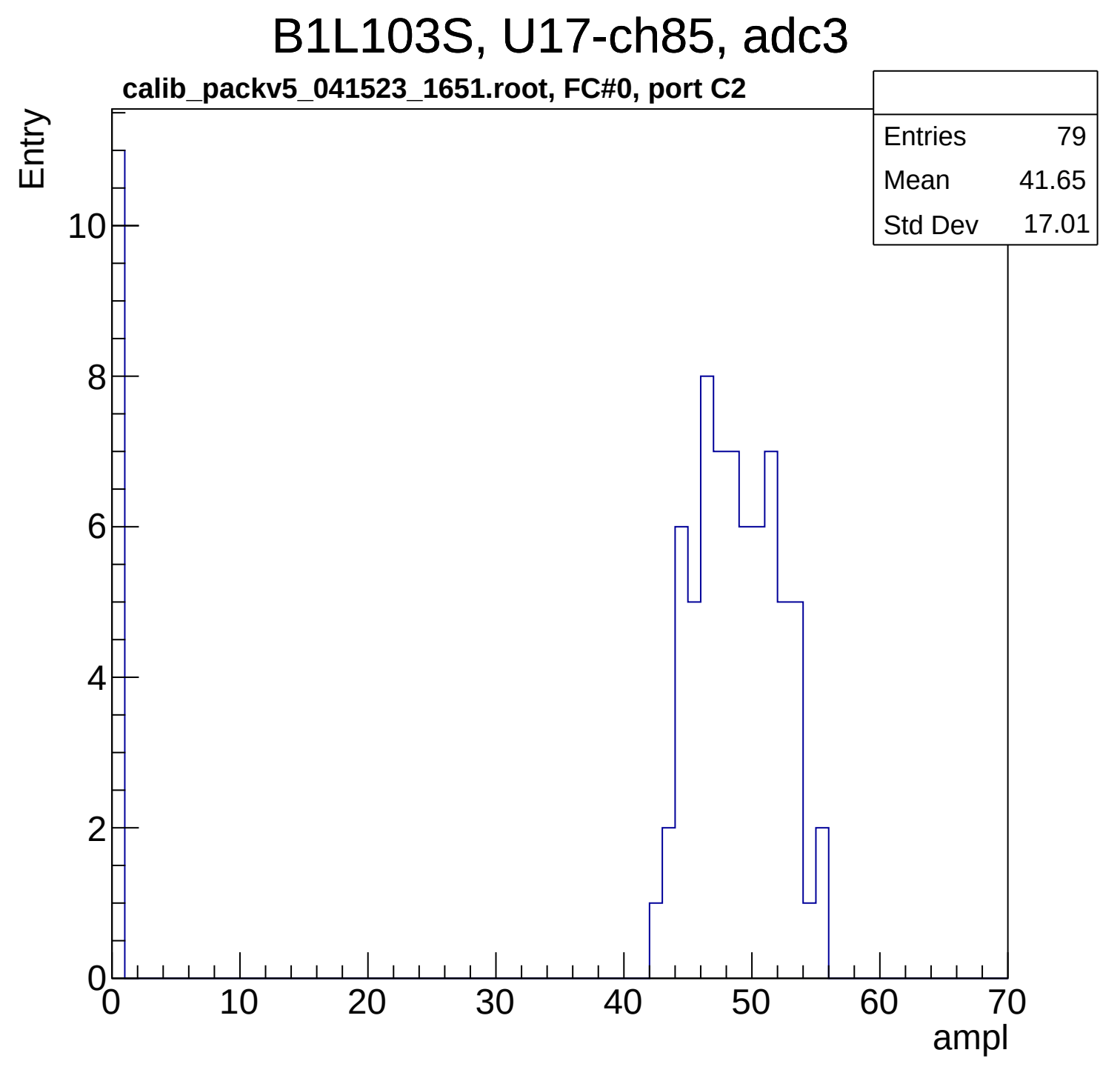
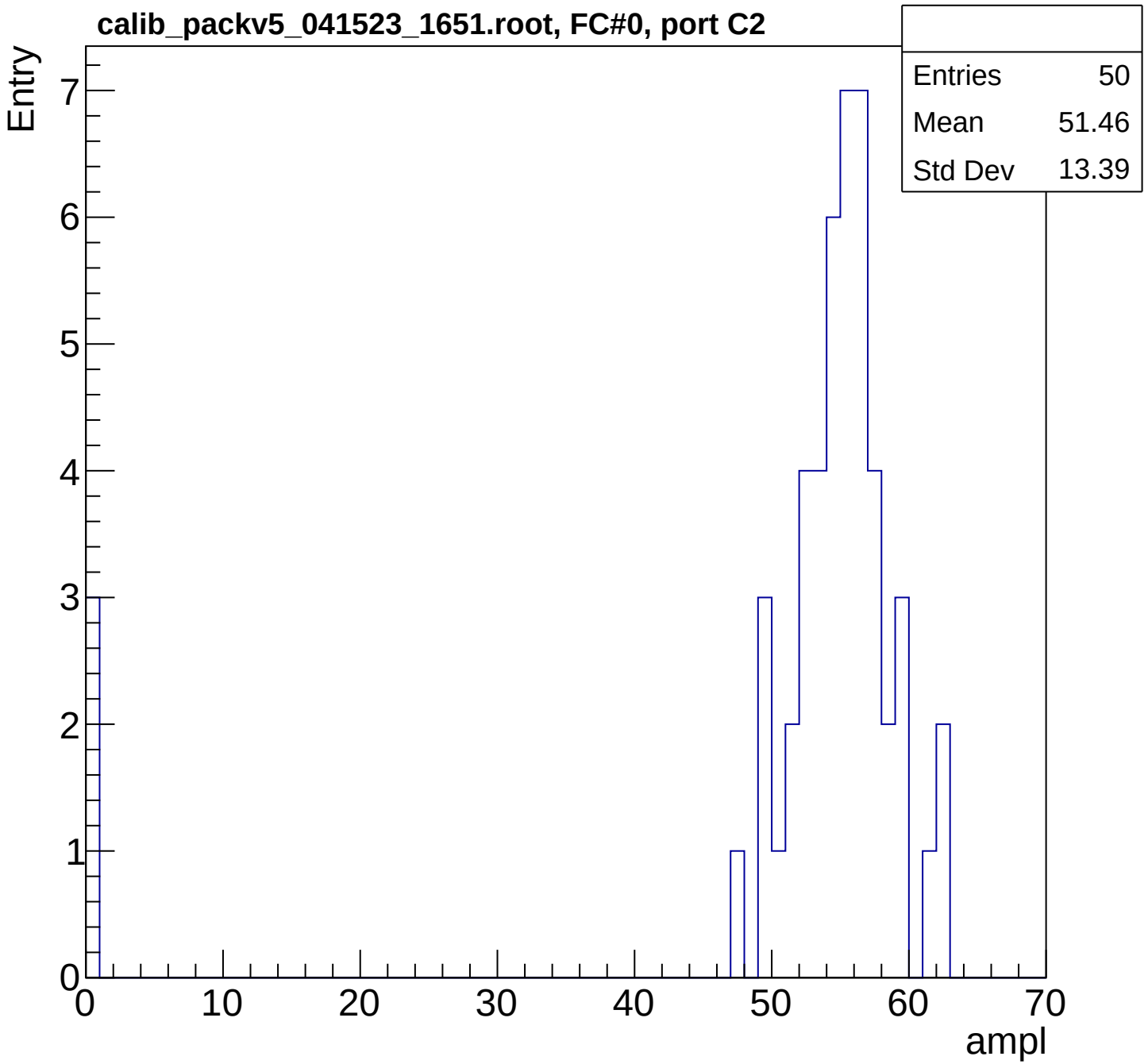
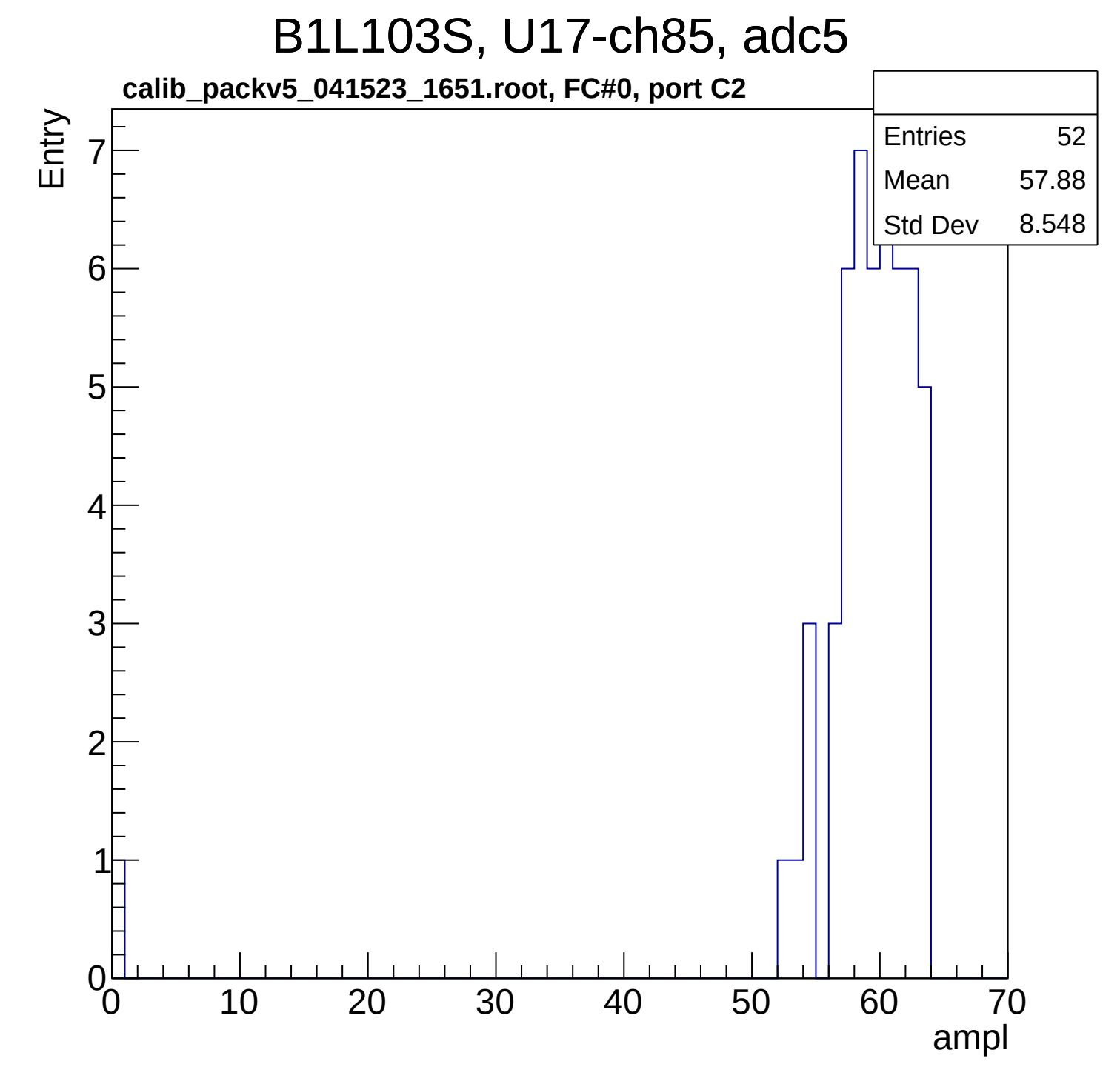
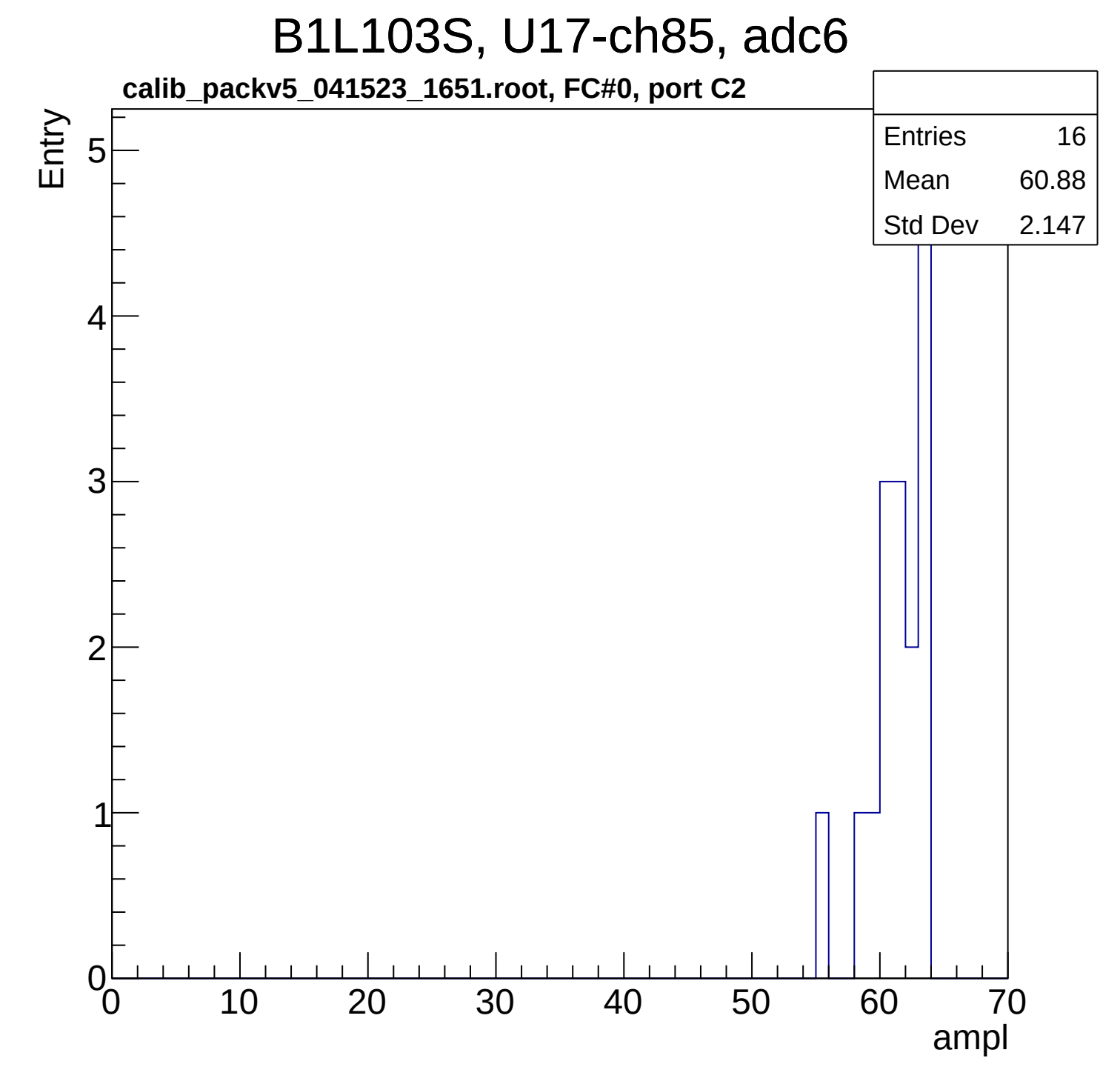
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U17-ch85, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 41.65
Std Dev 17.01
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch85, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 51.46
Std Dev 13.39
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U17-ch85, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 57.88
Std Dev 8.548
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U17-ch85, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 16
Mean 60.88
Std Dev 2.147
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
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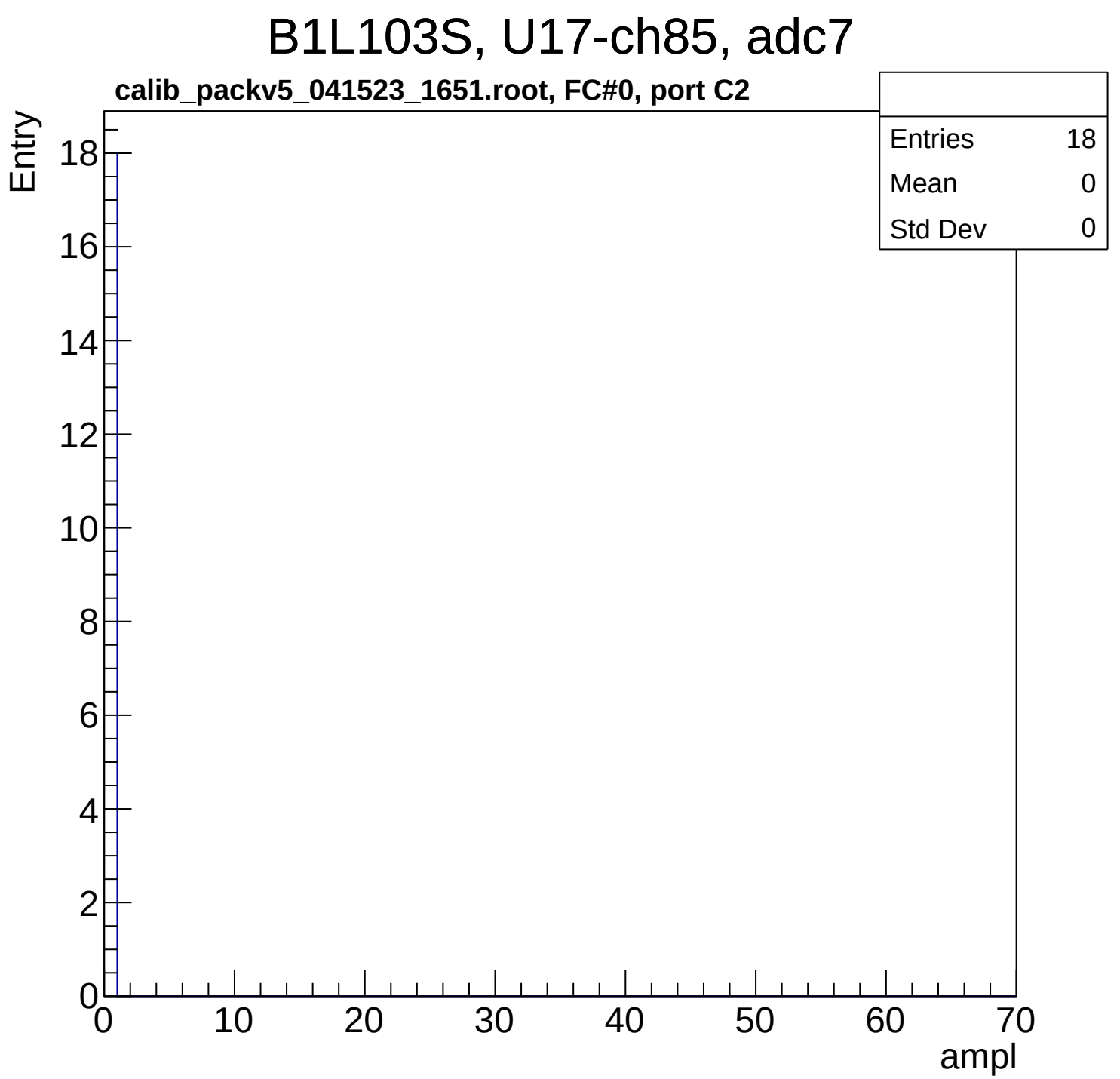
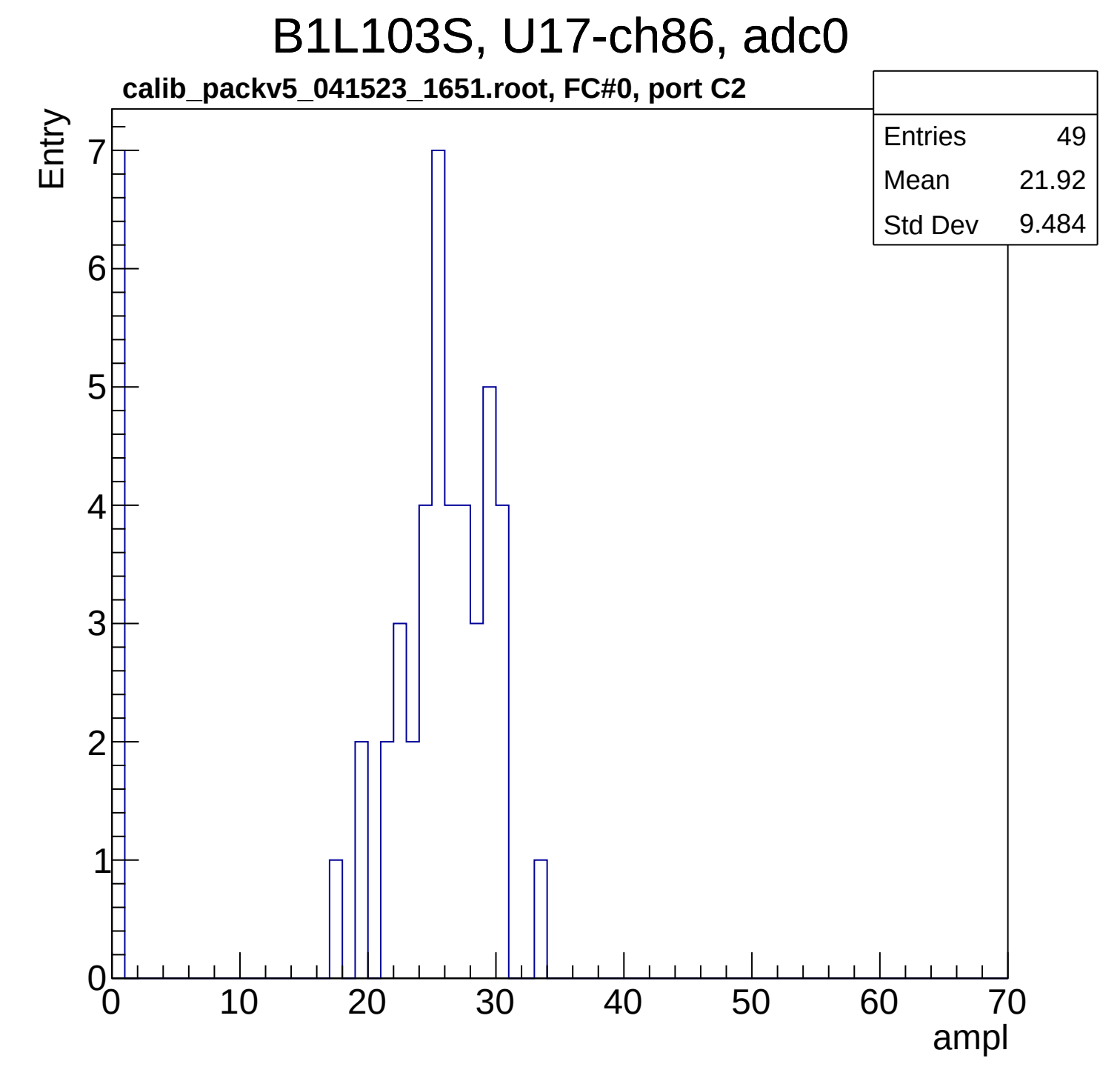
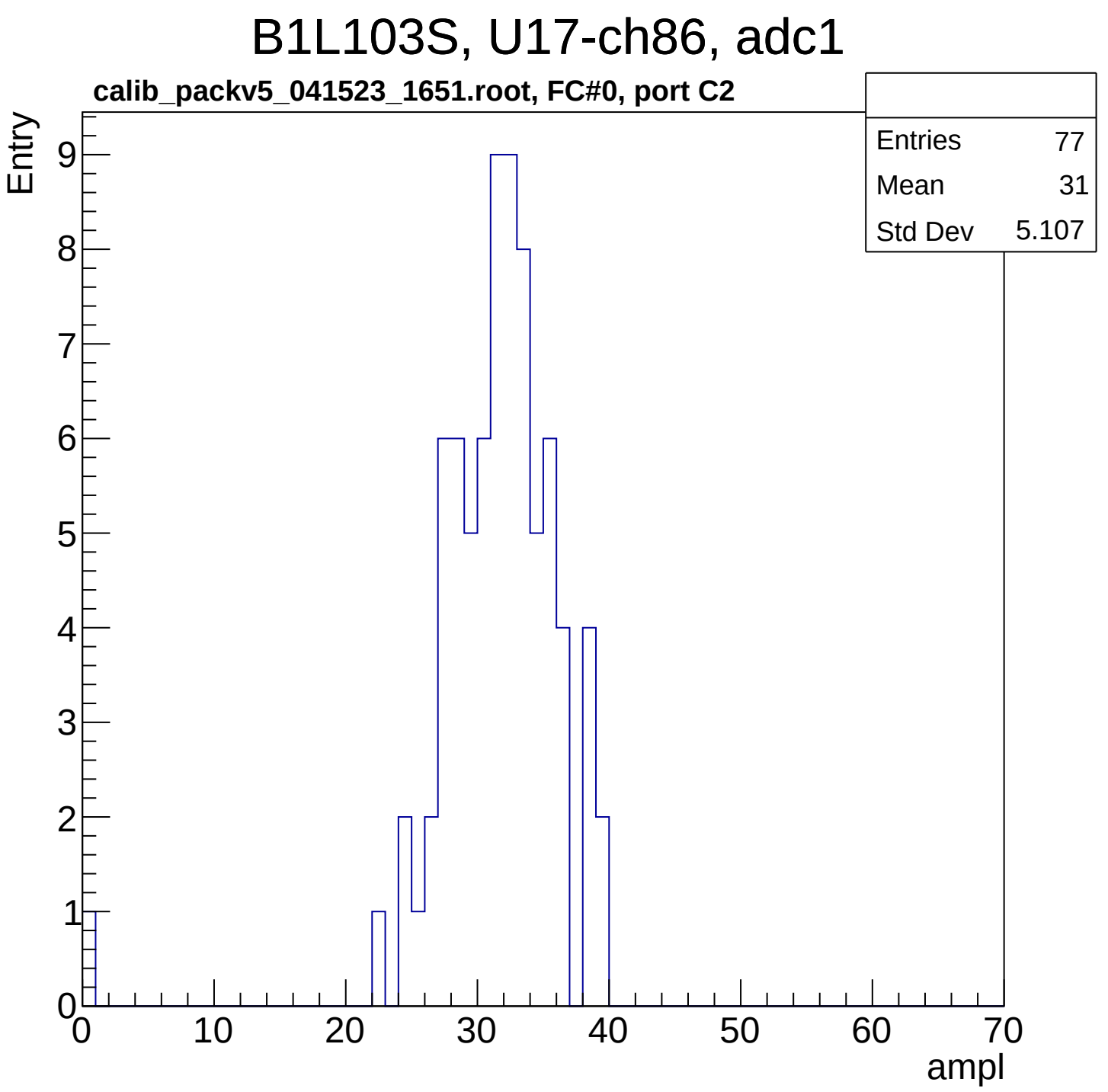

B1L103S, U17-ch85, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch86, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 21.92
Std Dev 9.484
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U17-ch86, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 31
Std Dev 5.107
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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60
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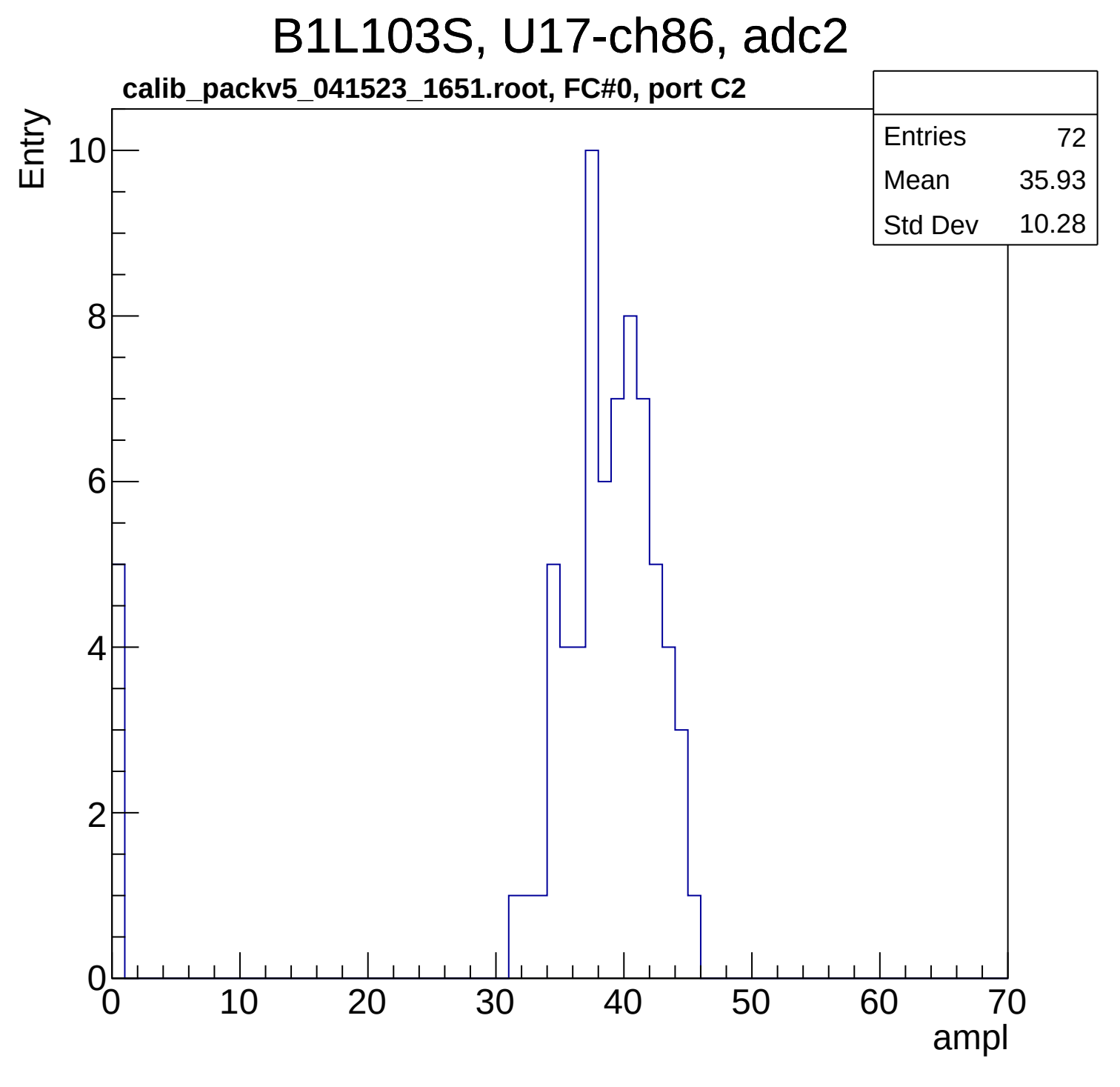
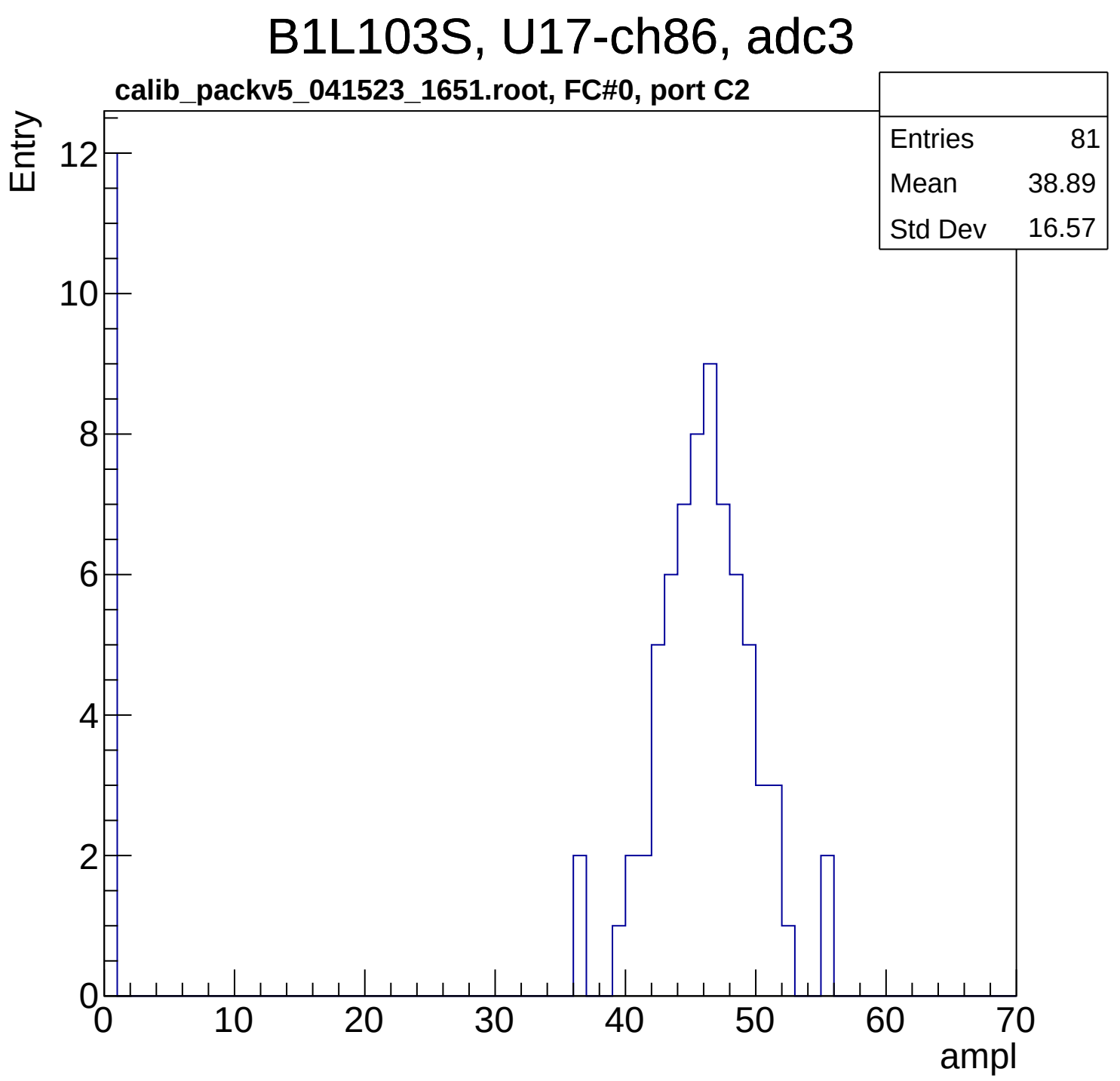
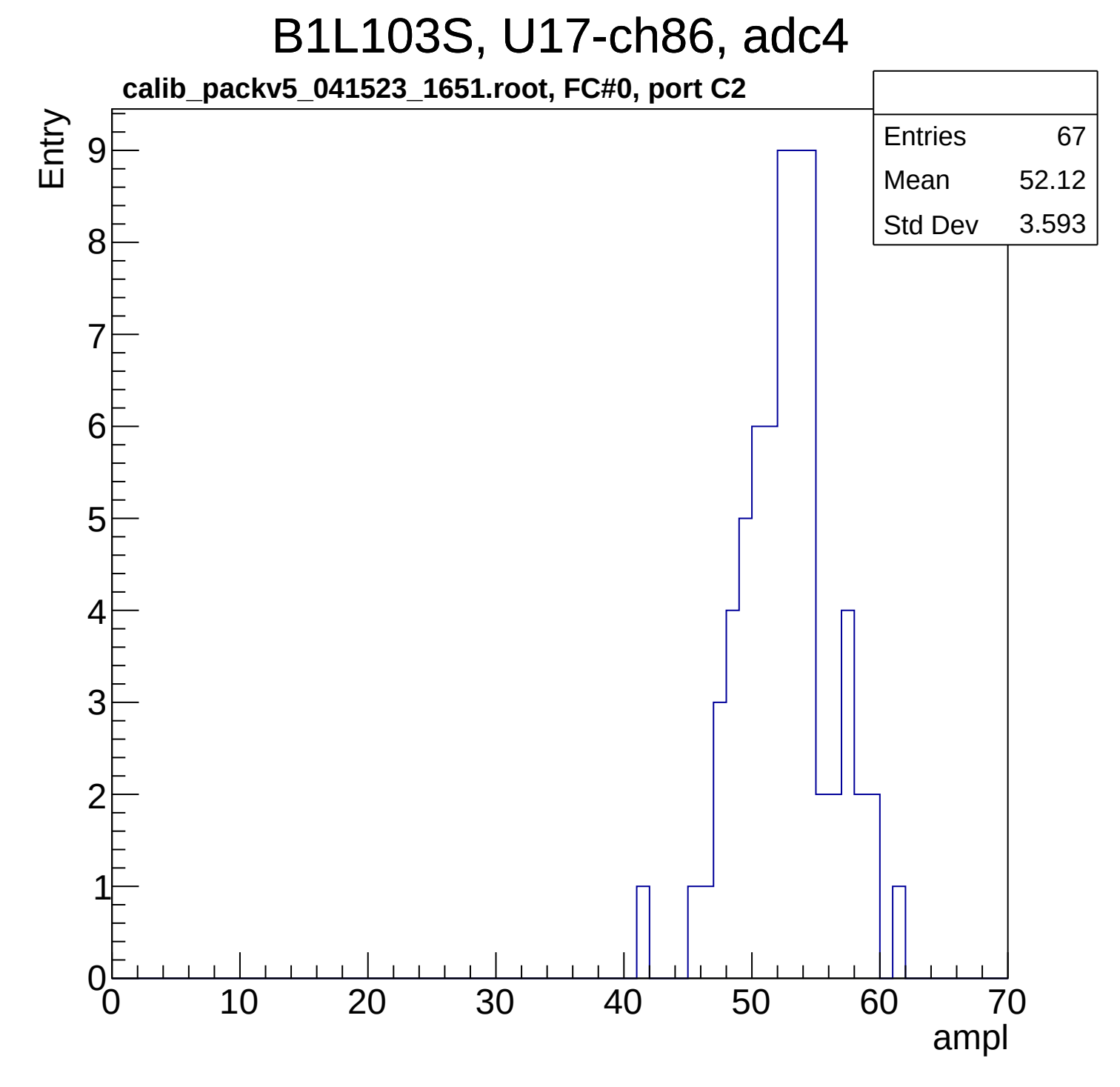

B1L103S, U17-ch86, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 35.93
Std Dev 10.28
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U17-ch86, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 38.89
Std Dev 16.57
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch86, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 52.12
Std Dev 3.593
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
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40
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60
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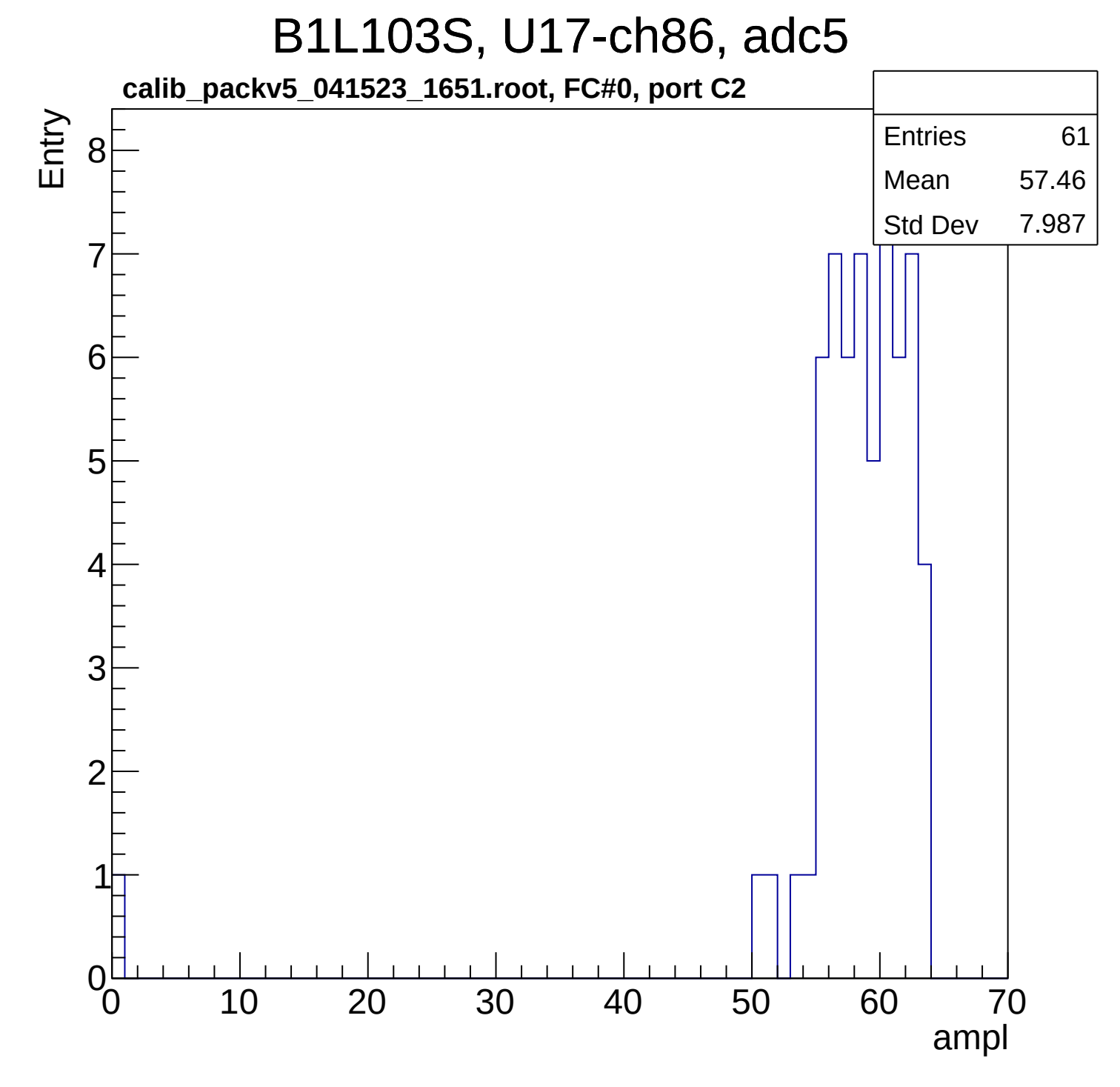
B1L103S, U17-ch86, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 57.46
Std Dev 7.987
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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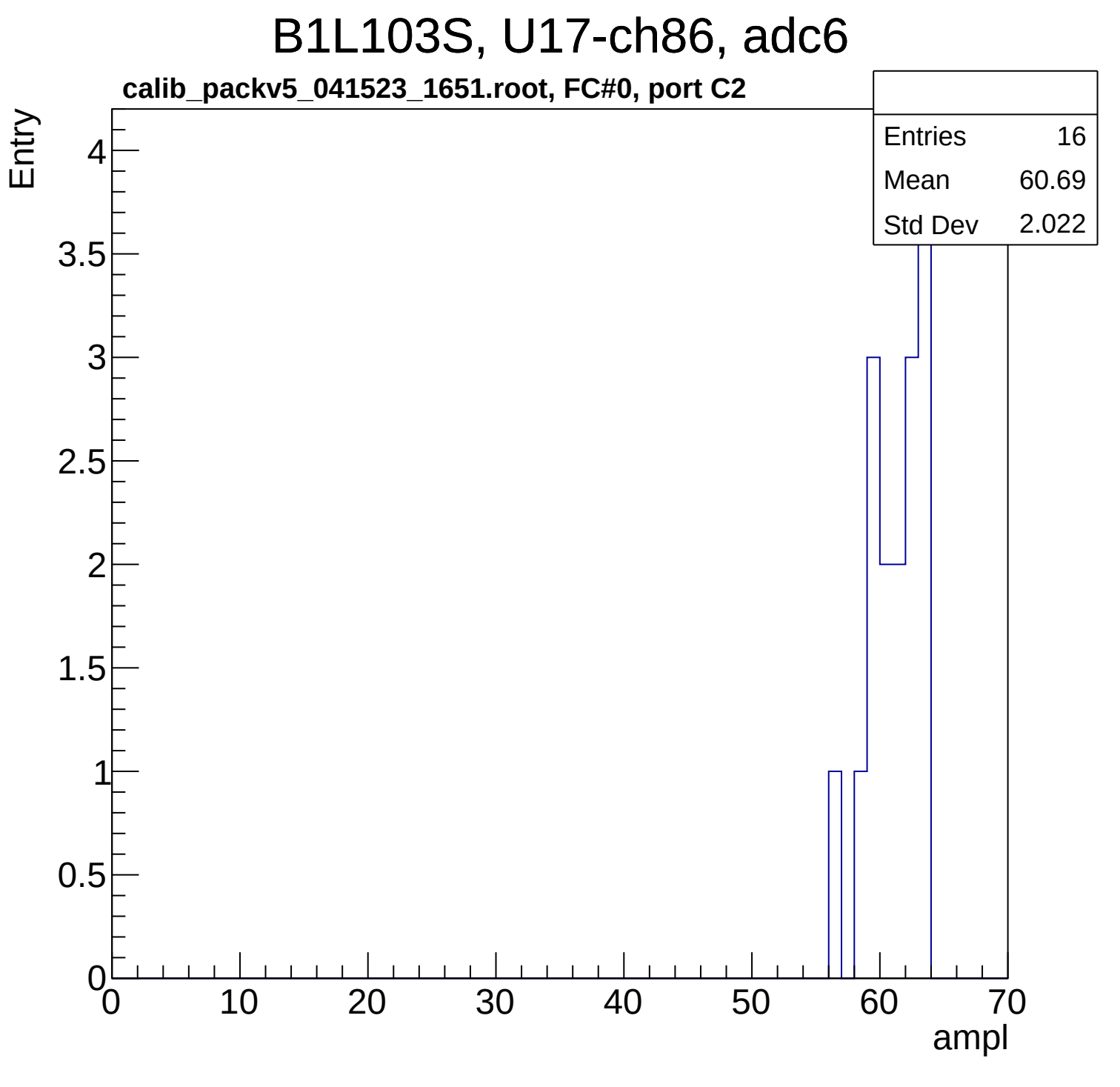
40
50
60
70


B1L103S, U17-ch86, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 16
Mean 60.69
Std Dev 2.022
Entry
ampl
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0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
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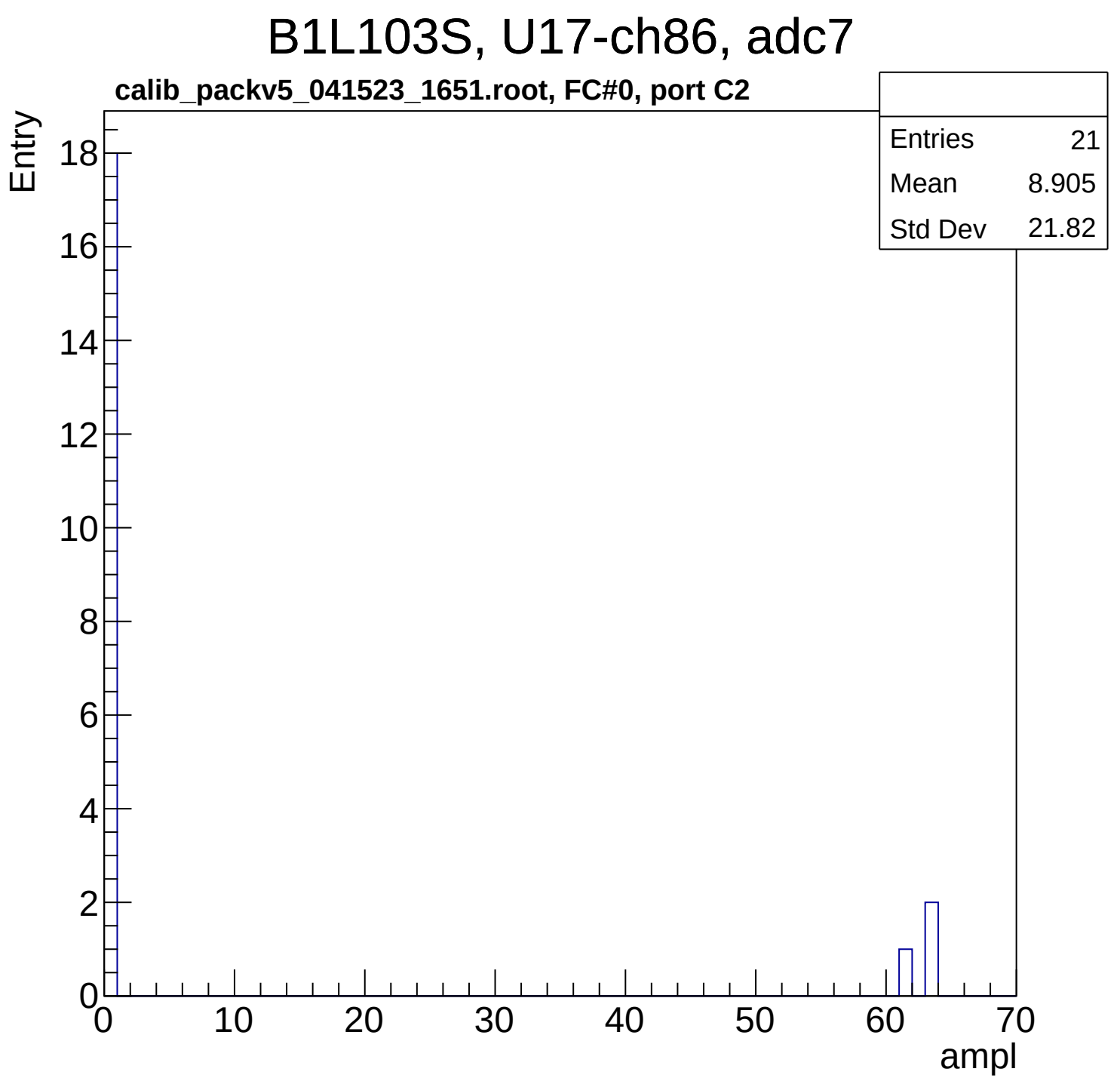
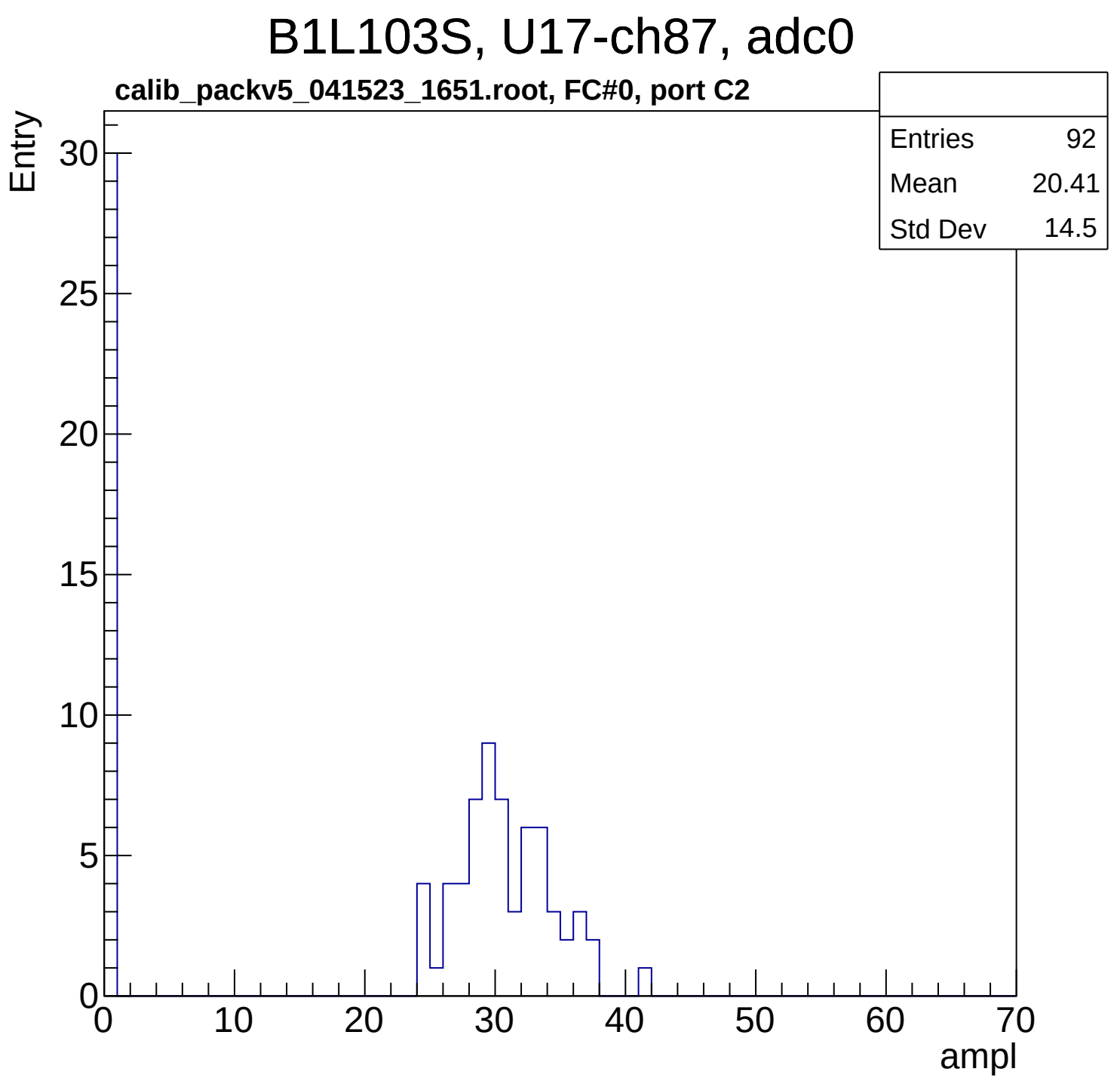
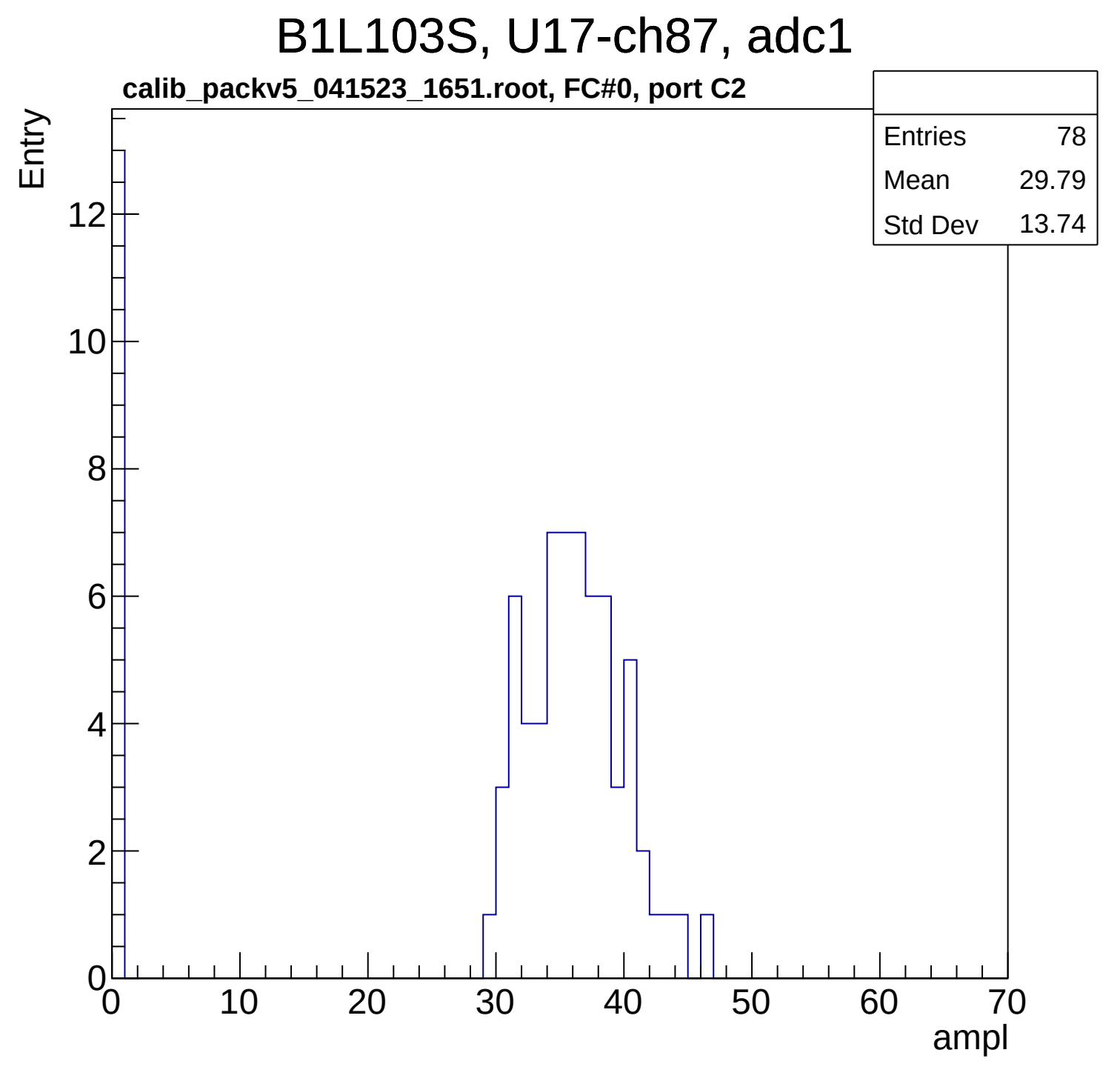
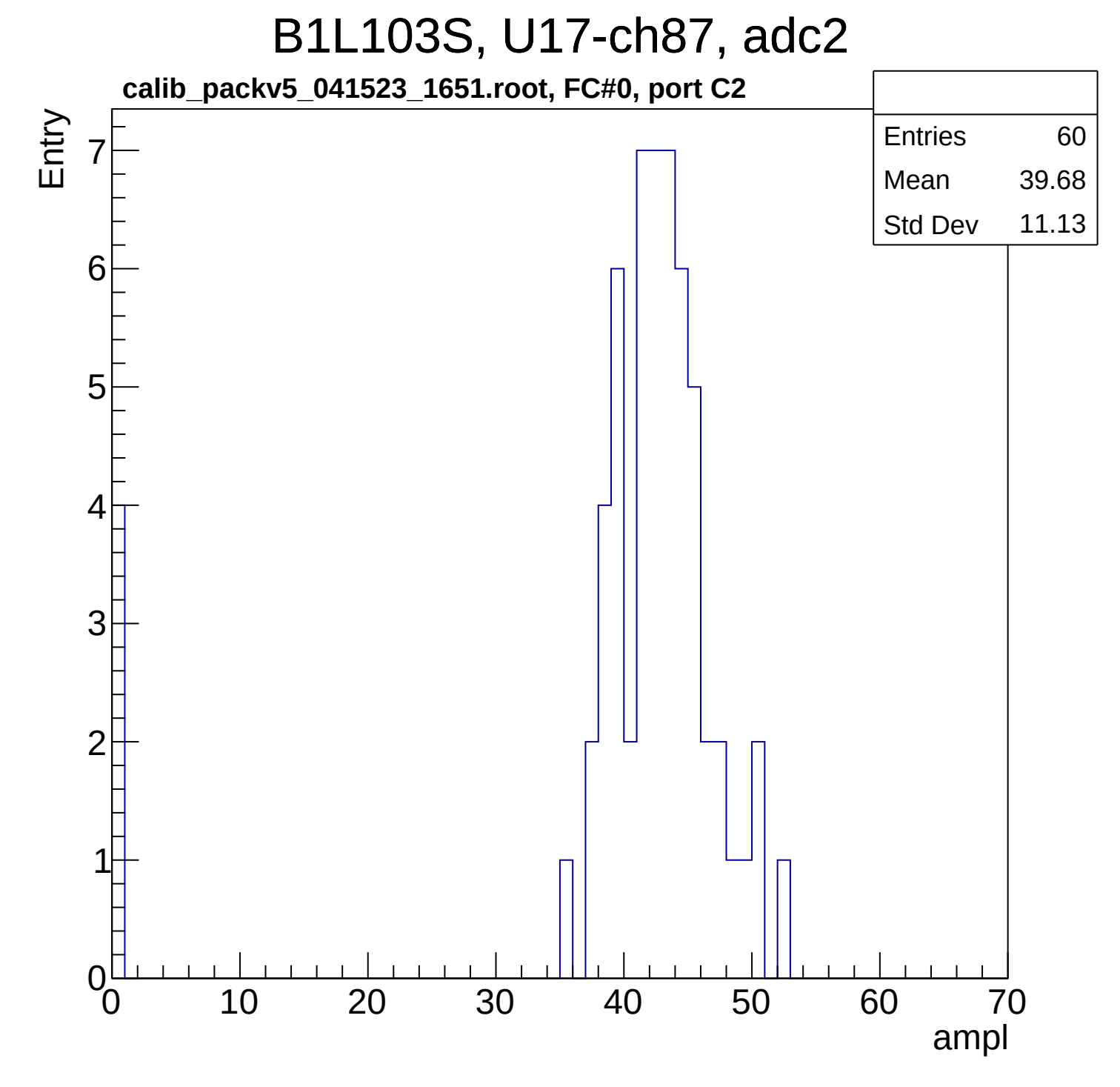
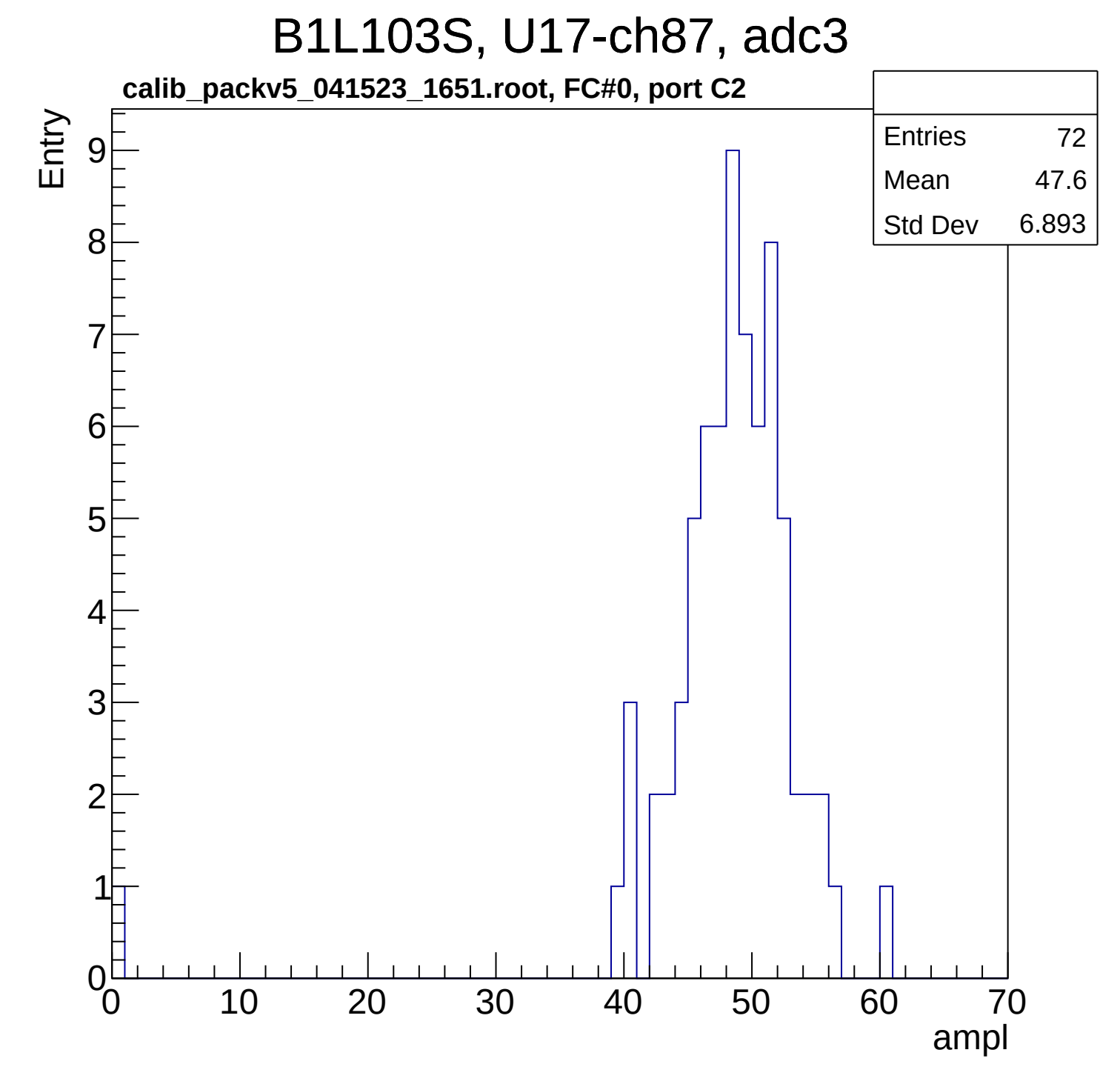
40
50
60
70


B1L103S, U17-ch86, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 8.905
Std Dev 21.82
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch87, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 92
Mean 20.41
Std Dev 14.5
Entry
0
5
10
15
20
25
30
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch87, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 29.79
Std Dev 13.74
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch87, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 39.68
Std Dev 11.13
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U17-ch87, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 47.6
Std Dev 6.893
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
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40
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60
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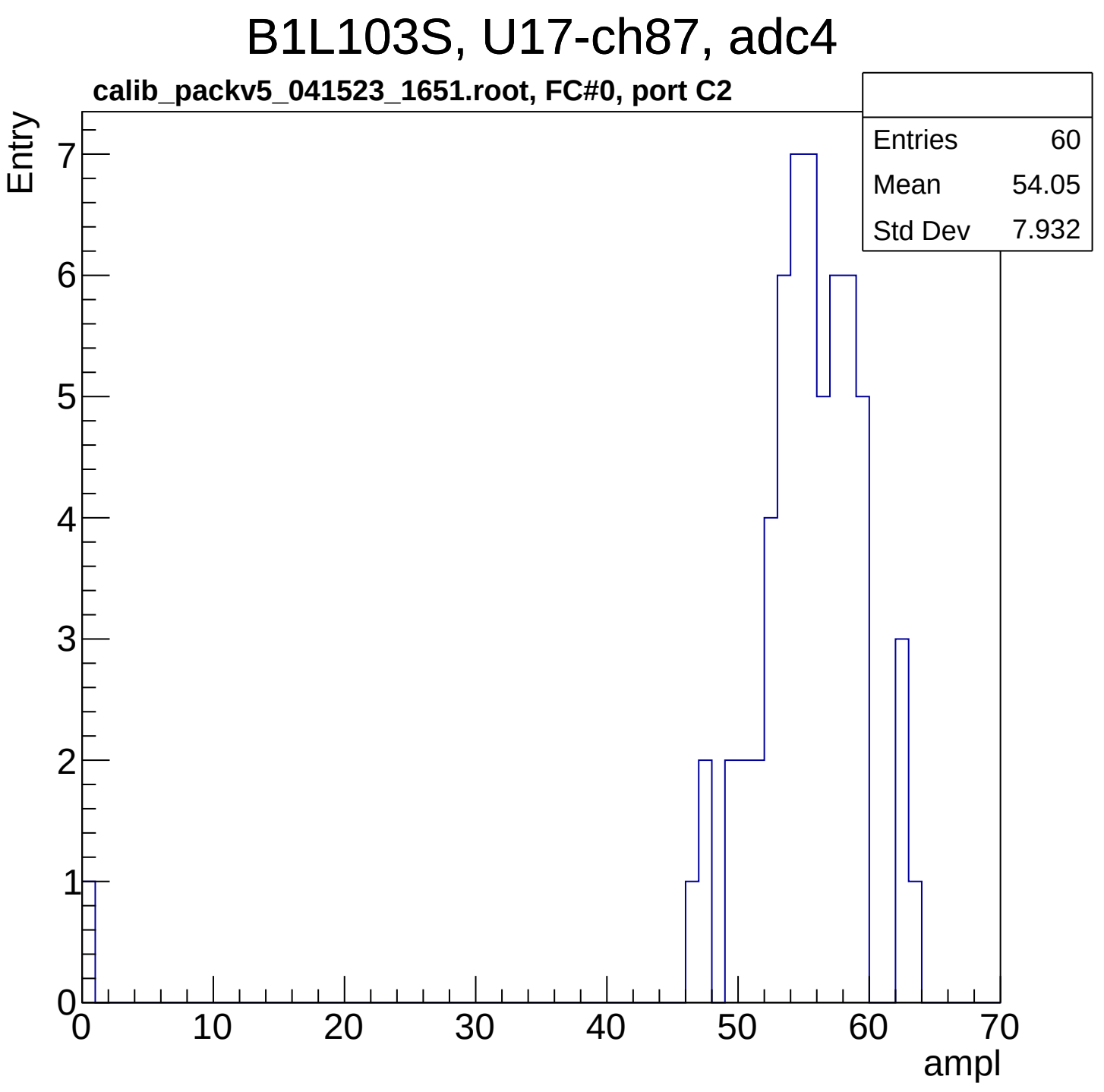
B1L103S, U17-ch87, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 54.05
Std Dev 7.932
Entry
ampl
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1
2
3
4
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6
7
0
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20
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40
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60
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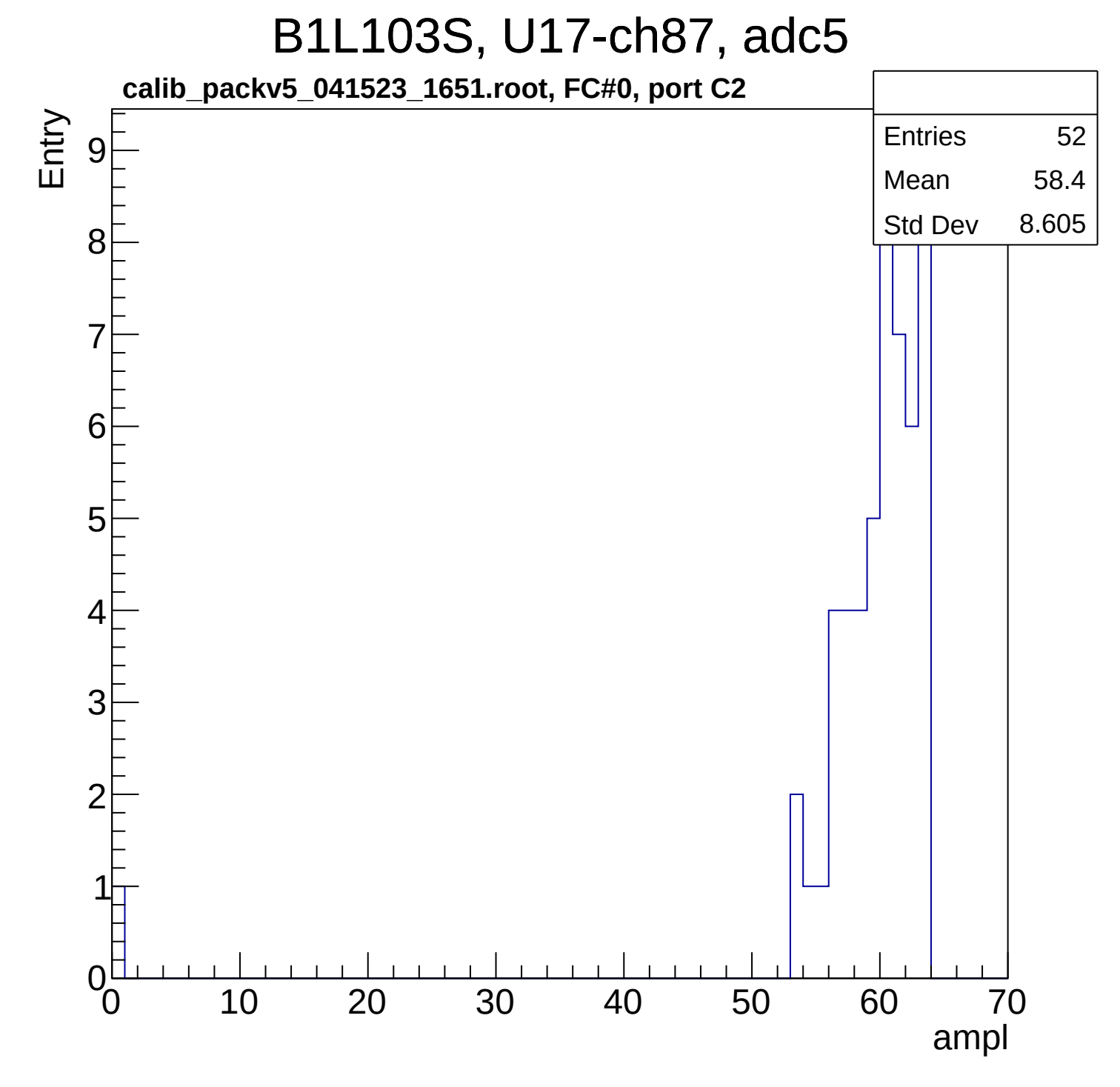
B1L103S, U17-ch87, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 58.4
Std Dev 8.605
Entry
ampl
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2
3
4
5
6
7
8
9
0
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40
50
60
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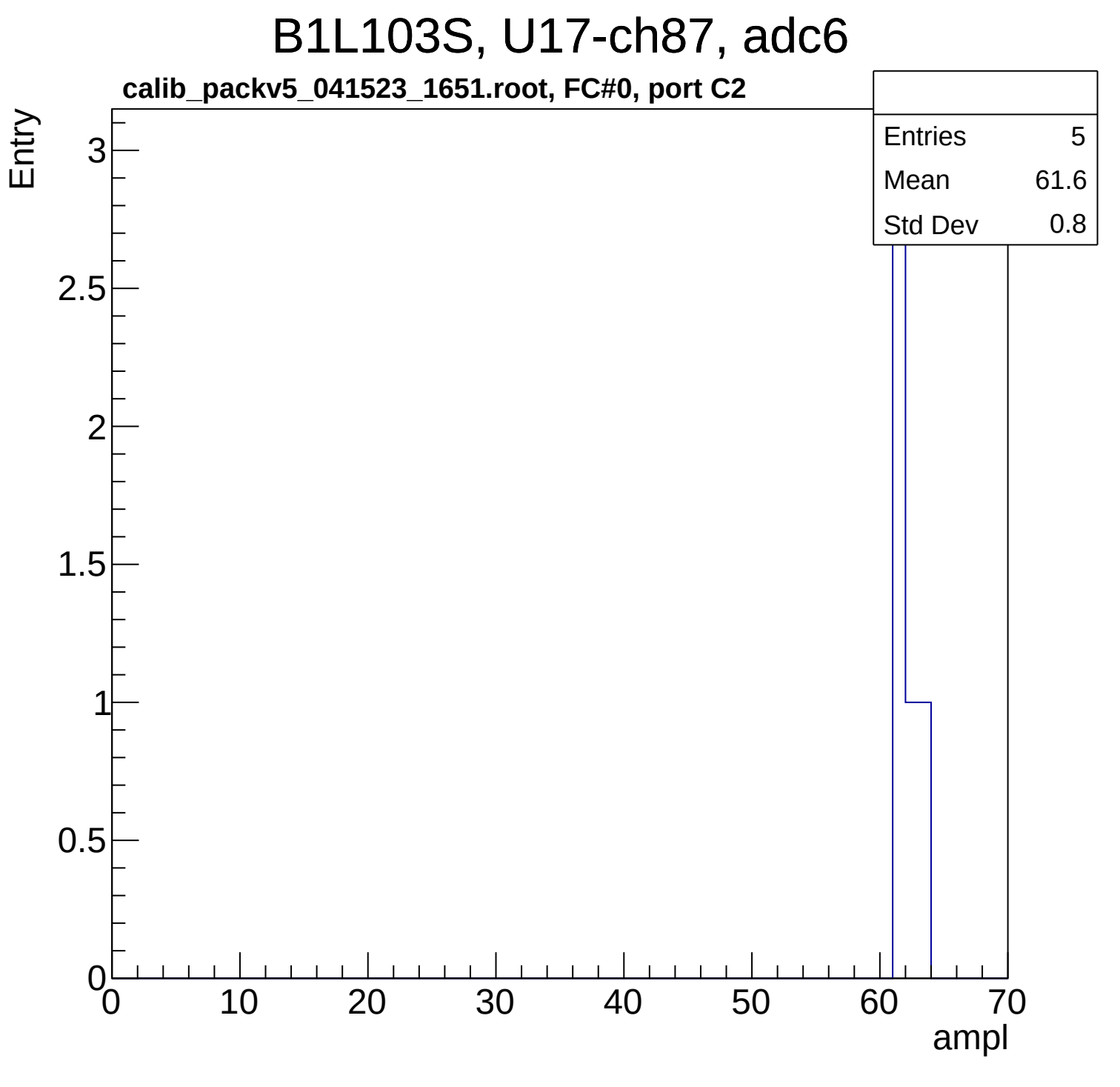
B1L103S, U17-ch87, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 5
Mean 61.6
Std Dev 0.8
Entry
ampl
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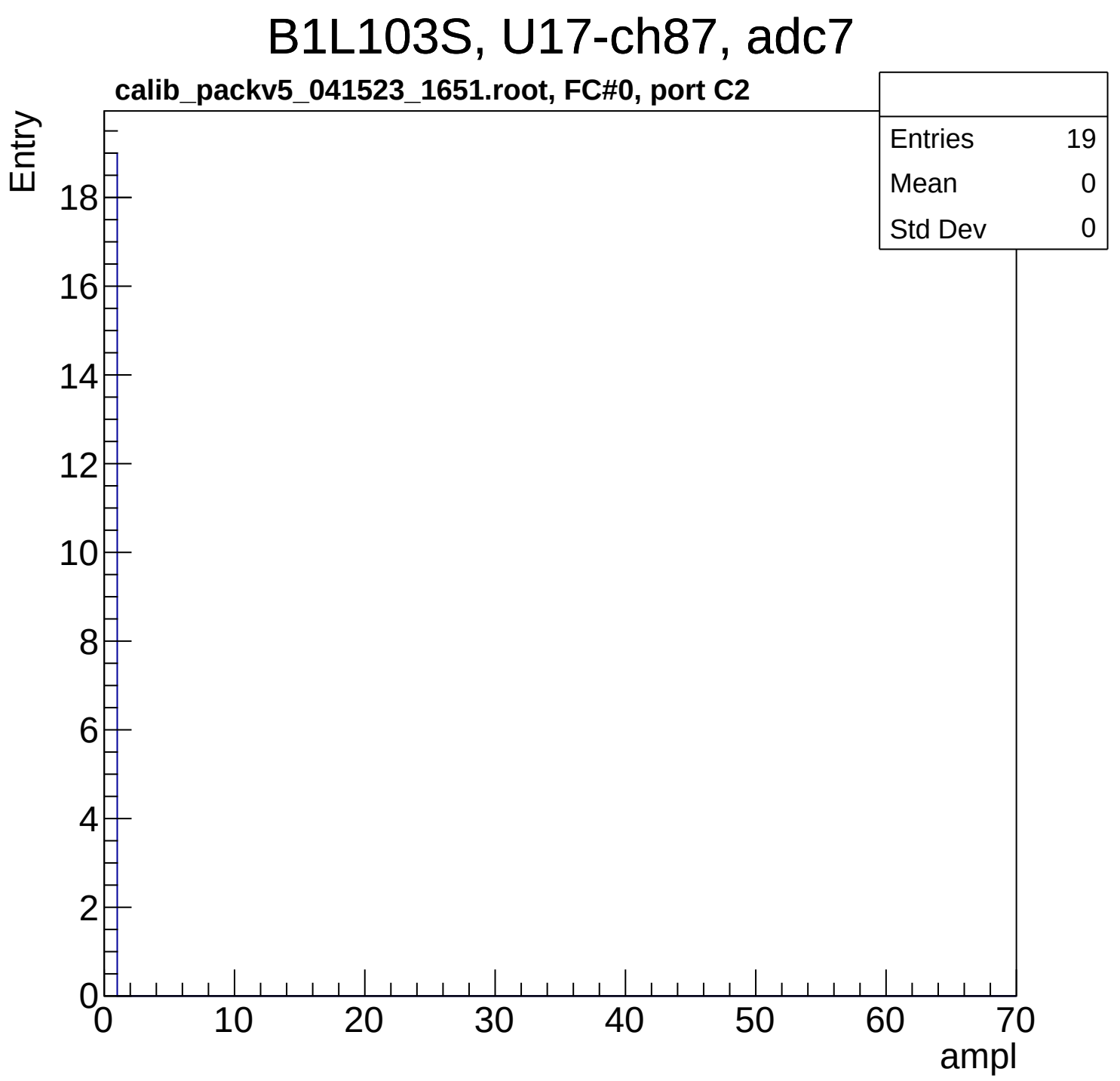
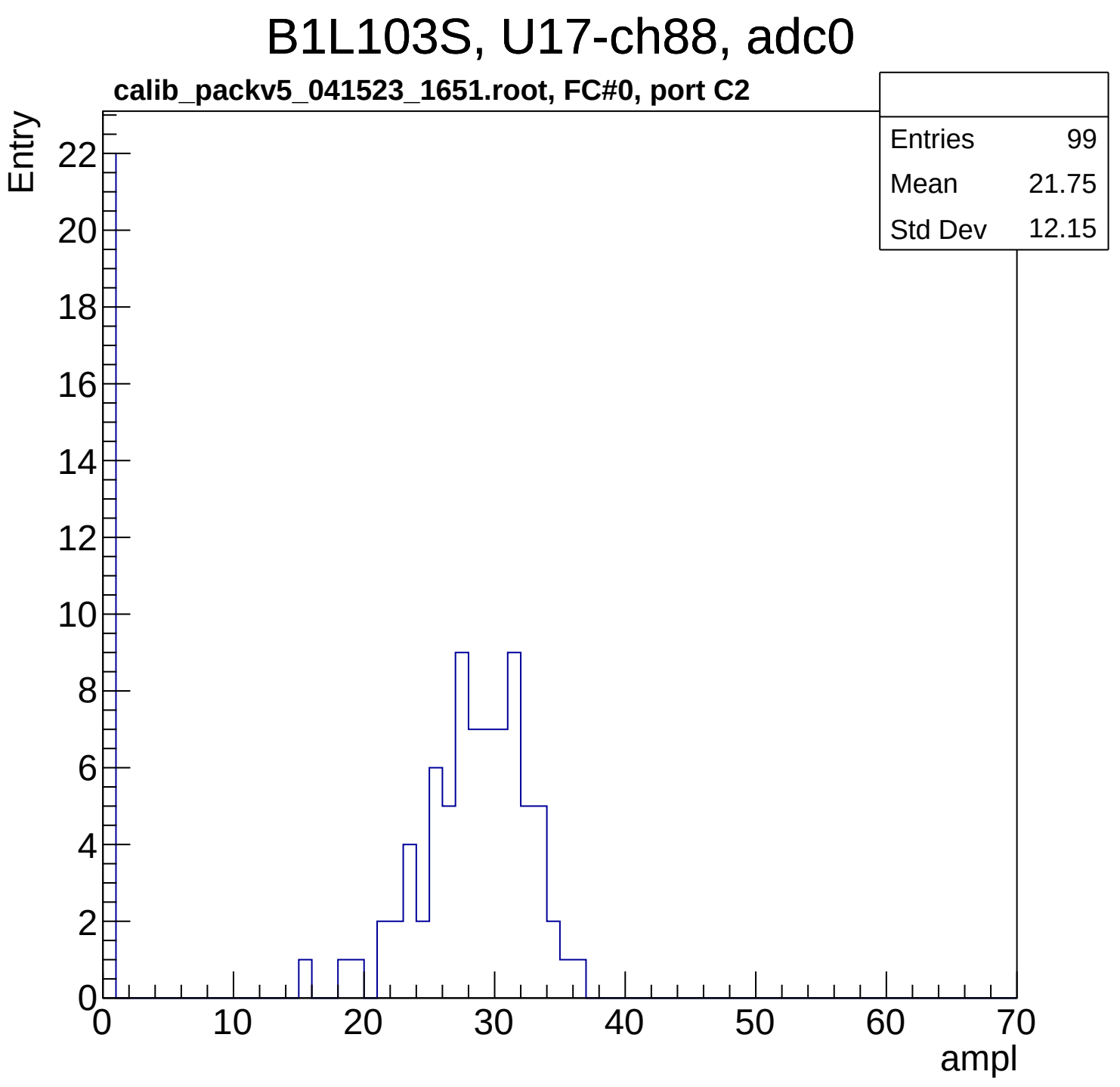
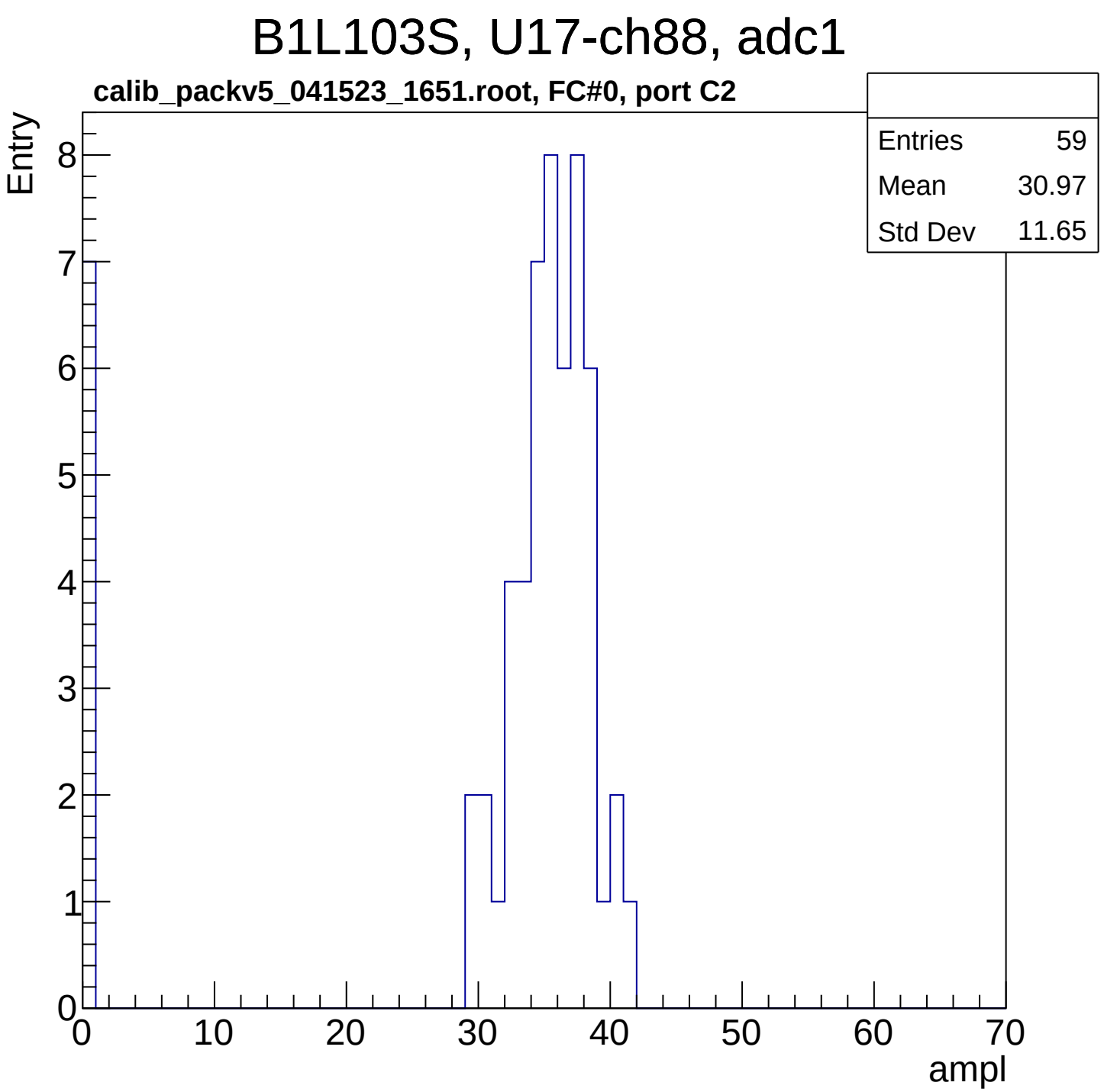
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U17-ch87, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch88, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 99
Mean 21.75
Std Dev 12.15
Entry
0
2
4
6
8
10
12
14
16
18
20
22
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch88, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 30.97
Std Dev 11.65
Entry
ampl
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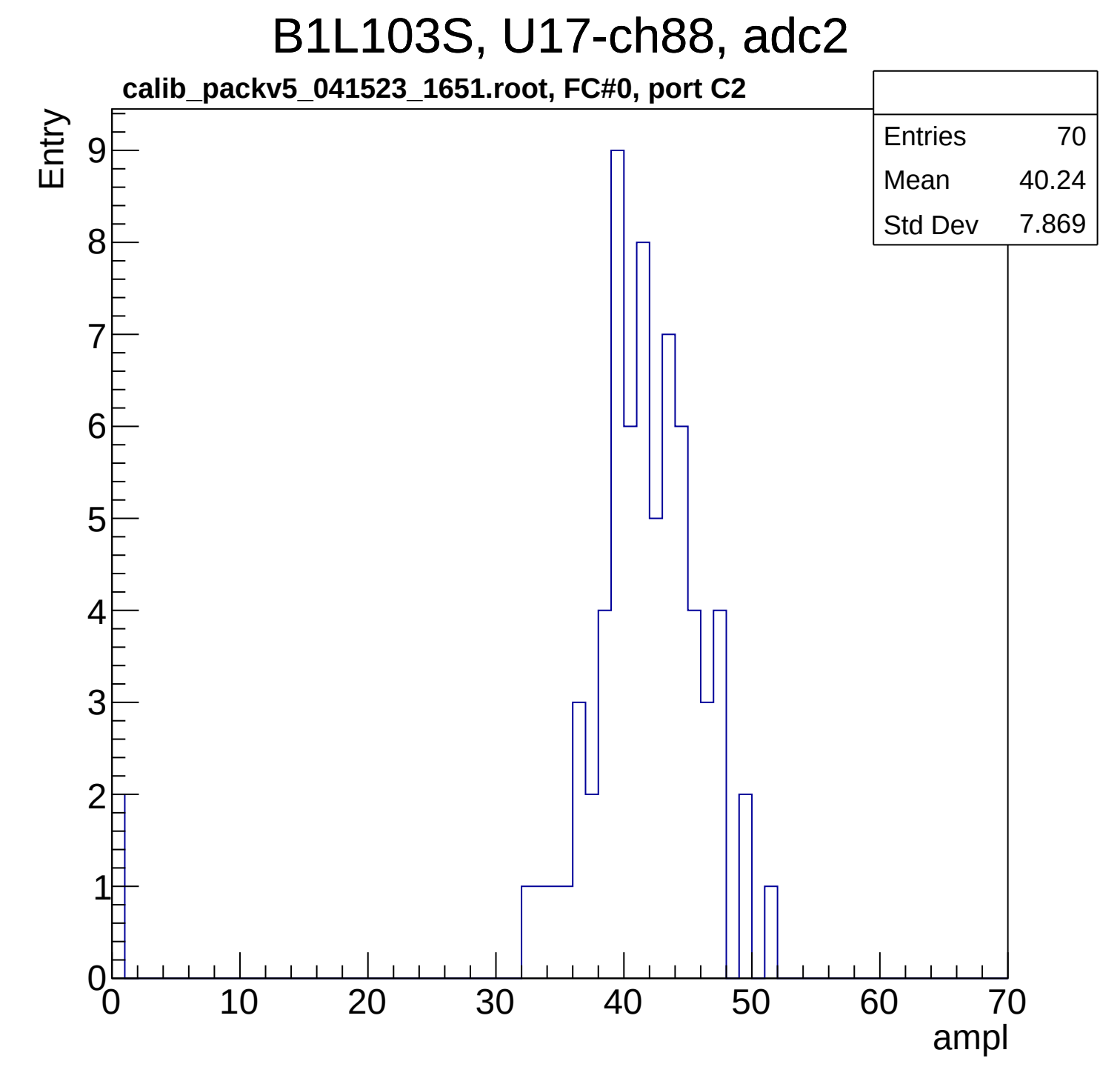
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U17-ch88, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 40.24
Std Dev 7.869
Entry
ampl
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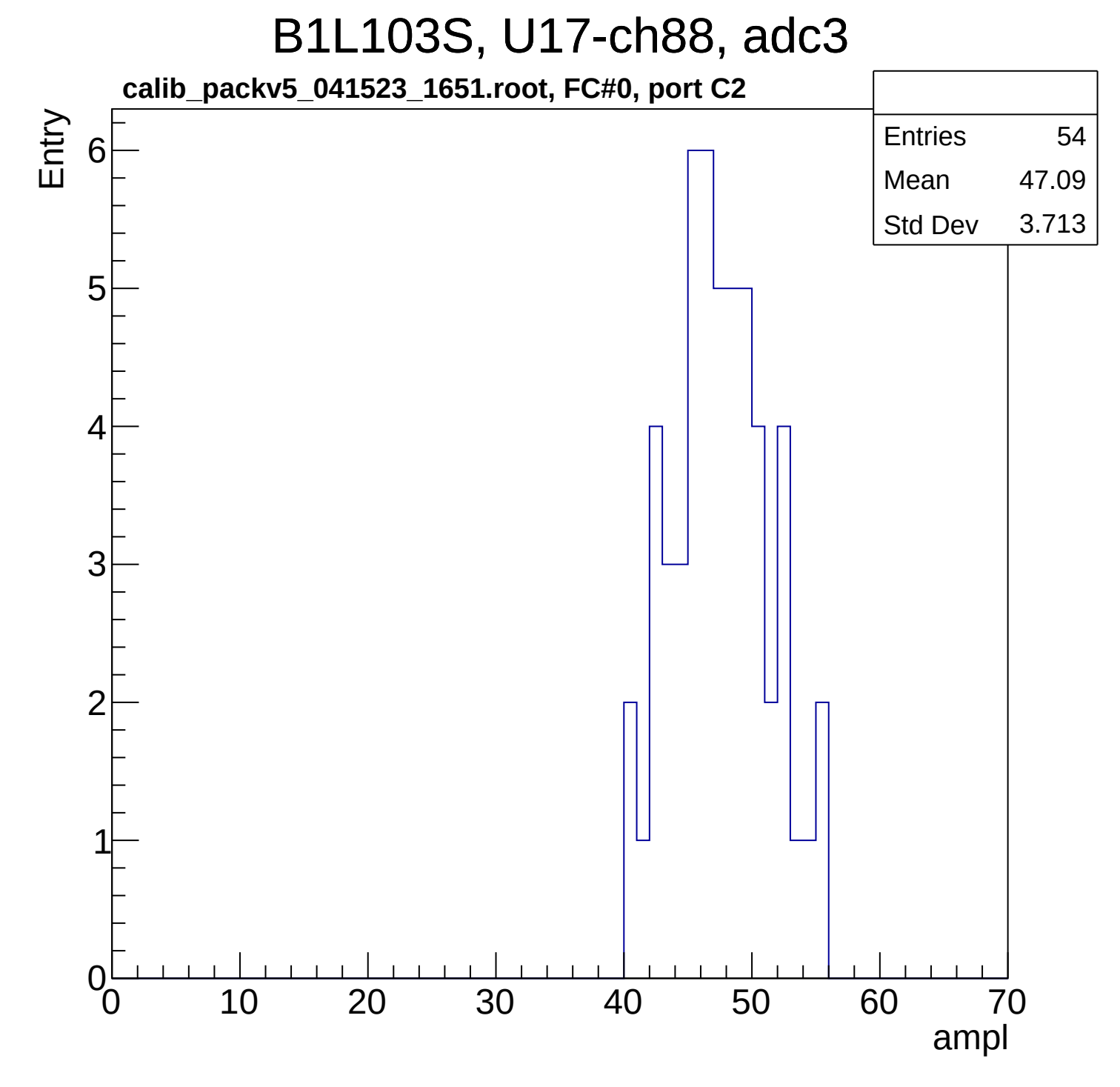
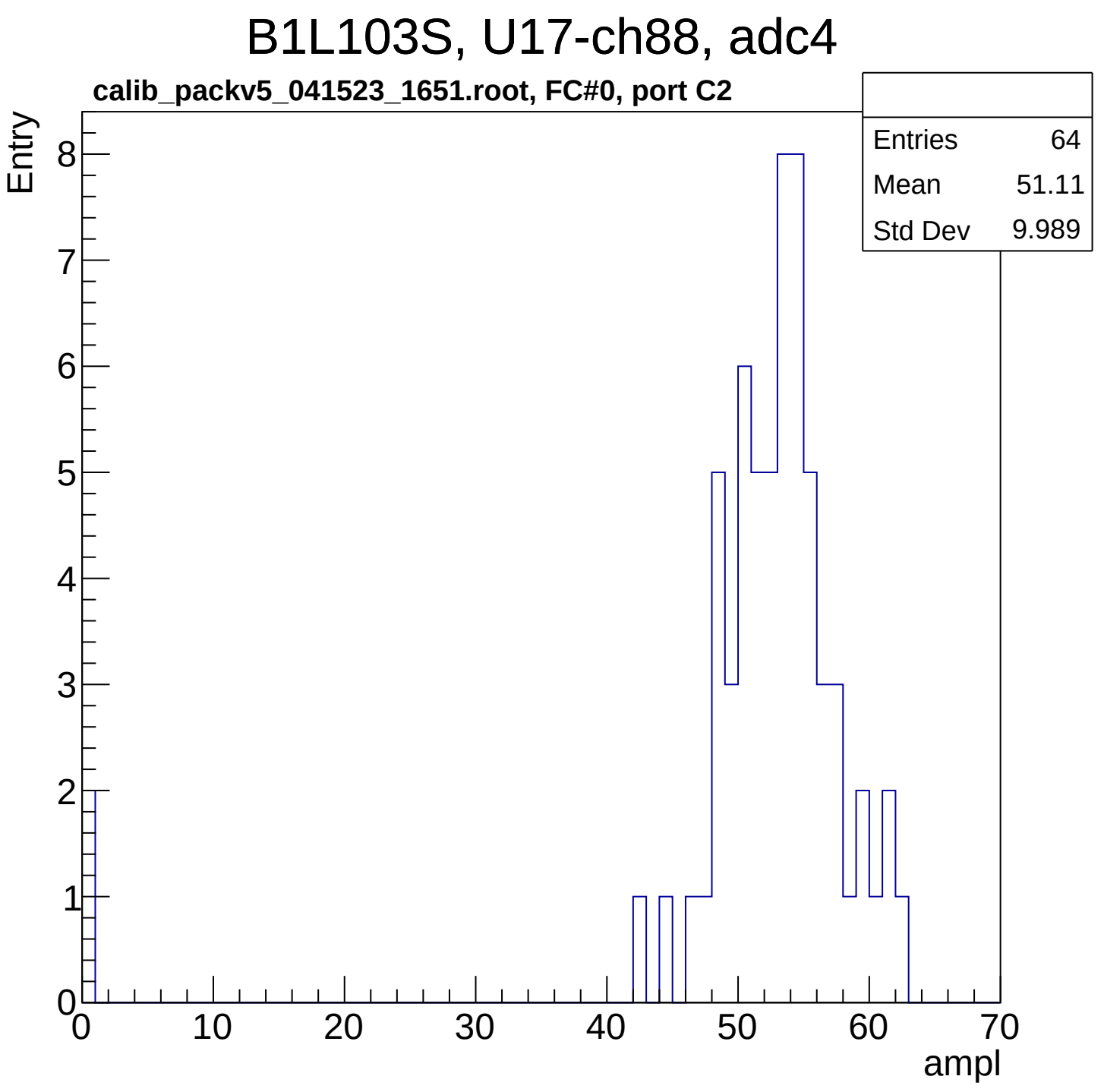
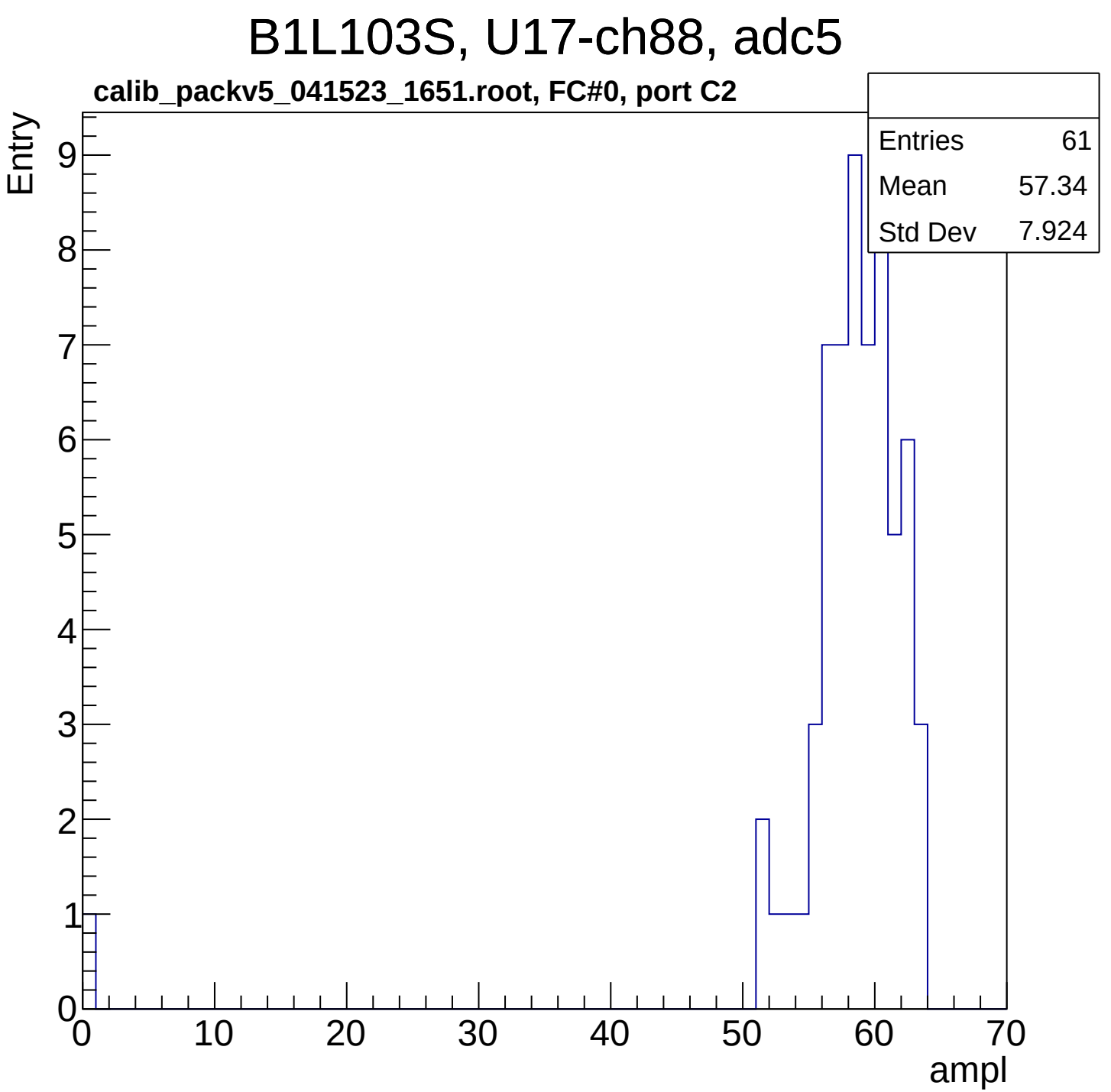
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U17-ch88, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 47.09
Std Dev 3.713
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U17-ch88, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 51.11
Std Dev 9.989
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U17-ch88, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 57.34
Std Dev 7.924
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
30
40
50
60
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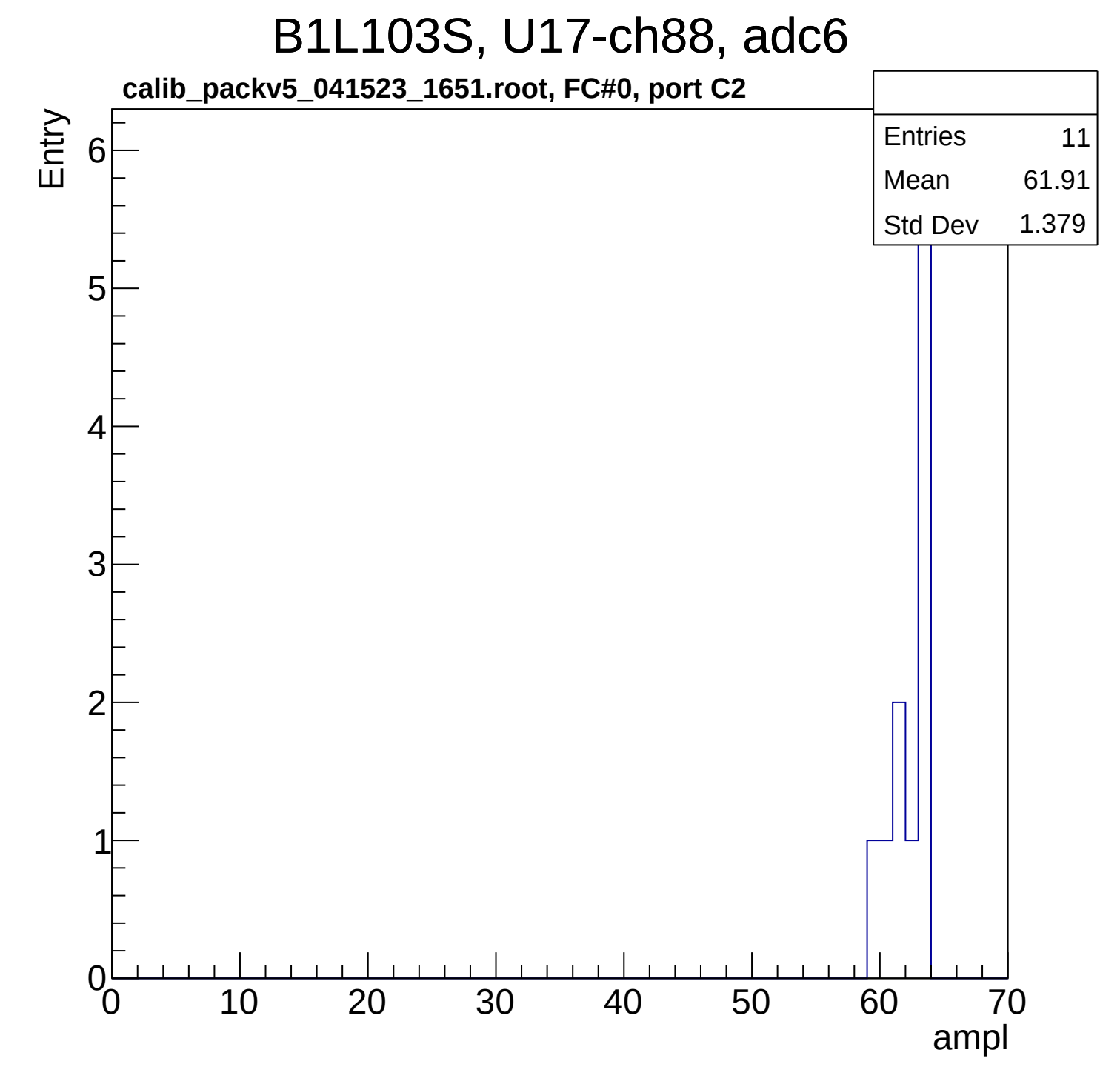
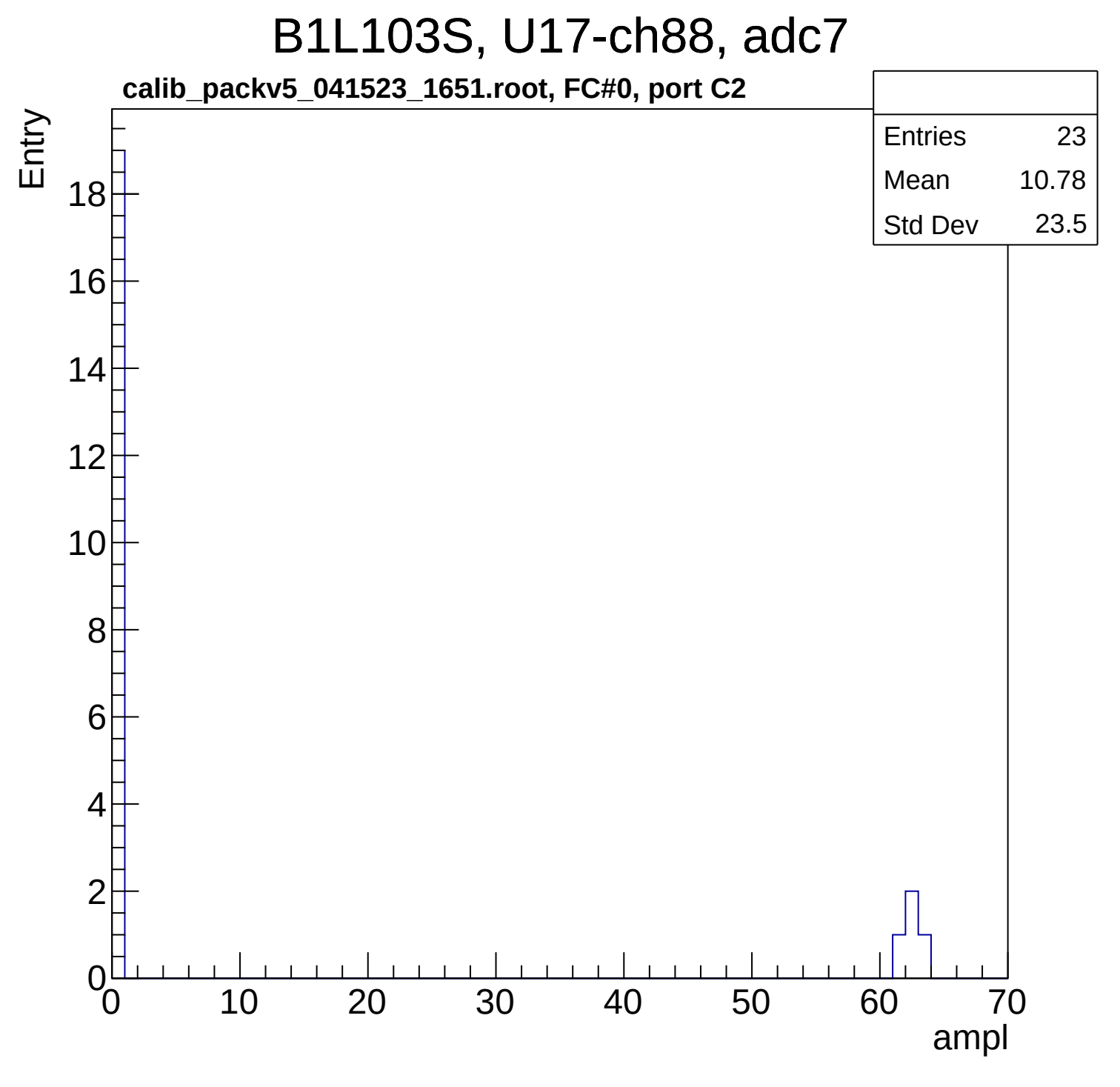
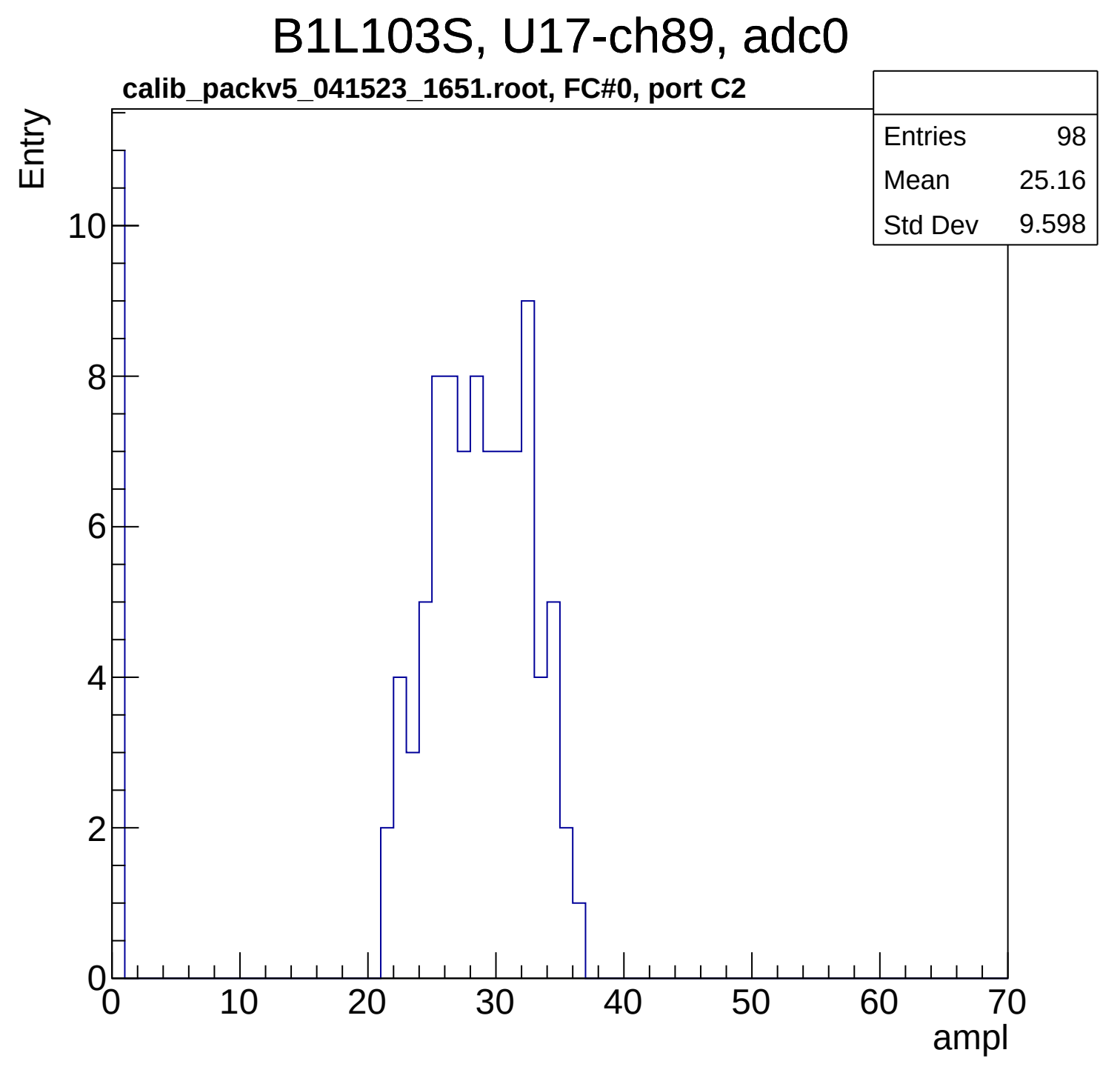
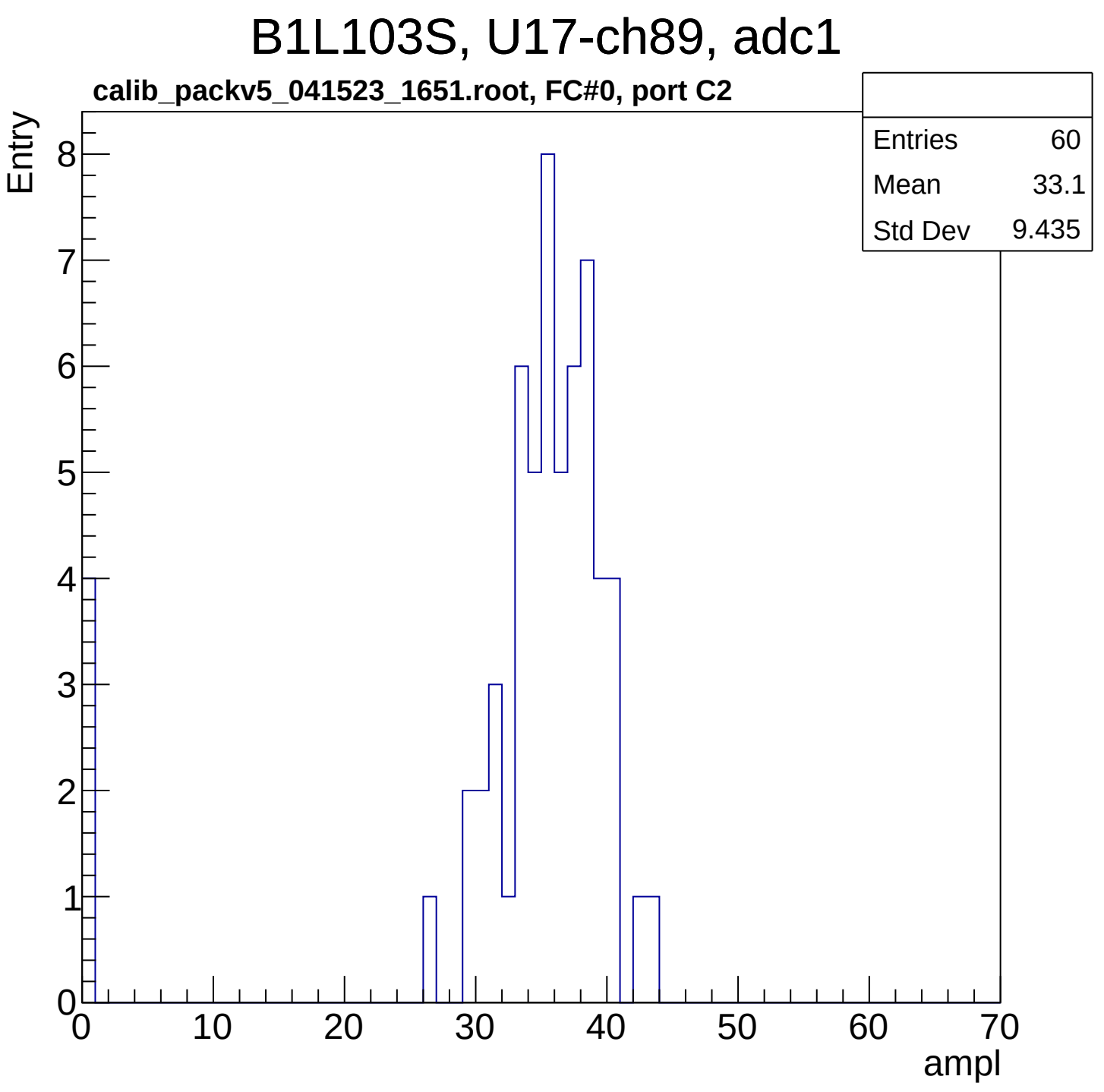

B1L103S, U17-ch88, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 61.91
Std Dev 1.379
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U17-ch88, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 23
Mean 10.78
Std Dev 23.5
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch89, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 98
Mean 25.16
Std Dev 9.598
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch89, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 33.1
Std Dev 9.435
Entry
ampl
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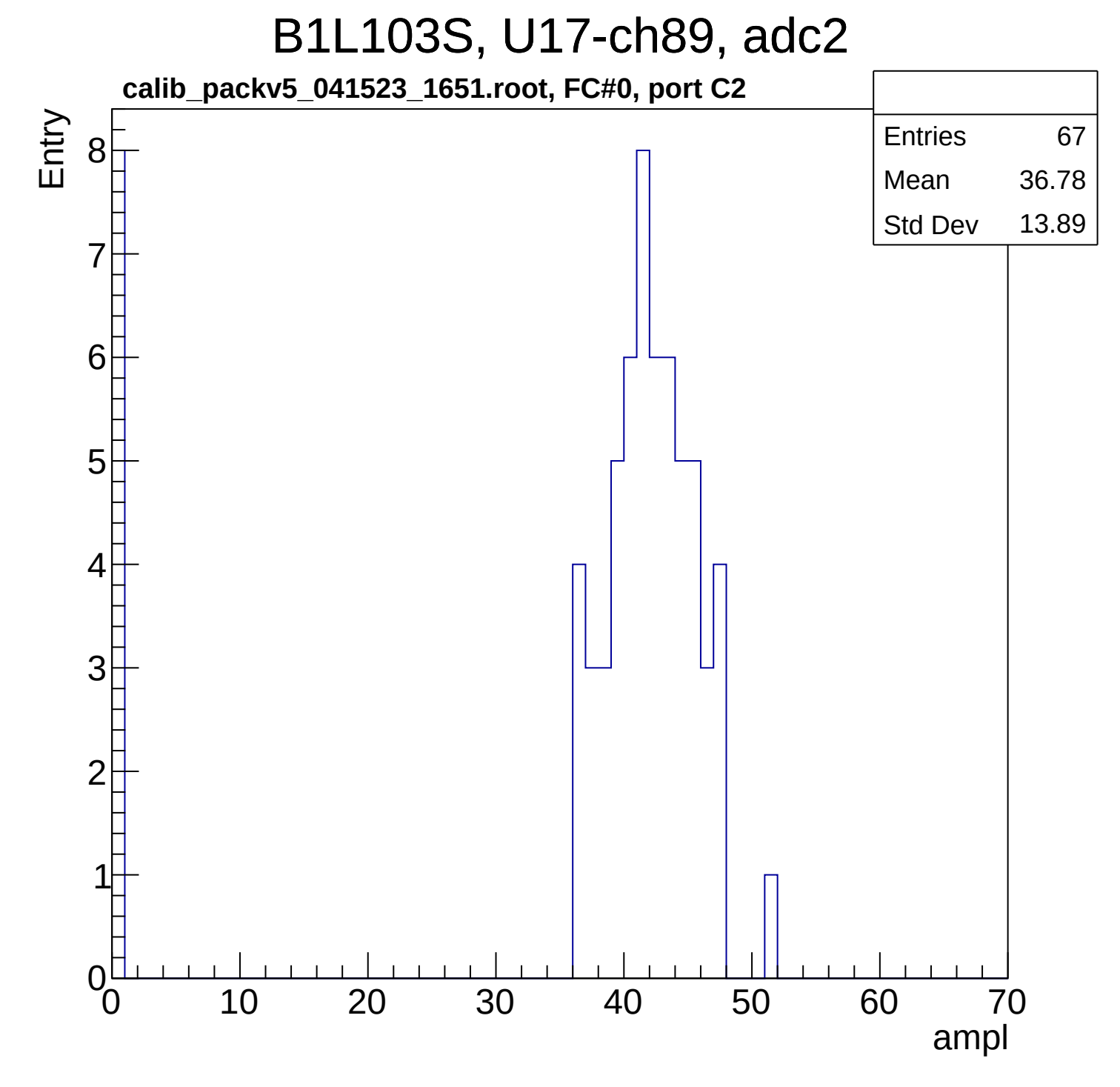
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U17-ch89, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 36.78
Std Dev 13.89
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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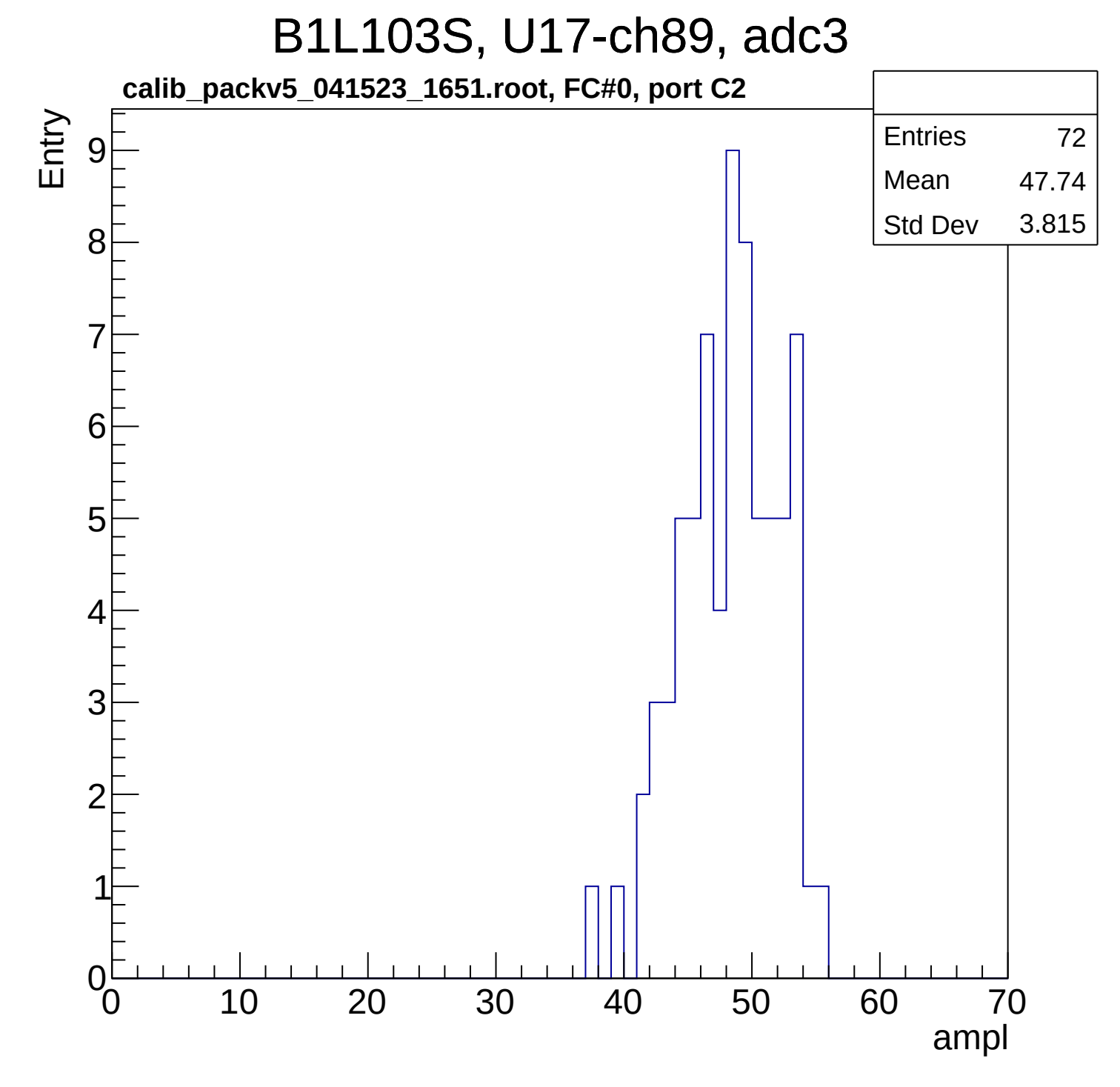
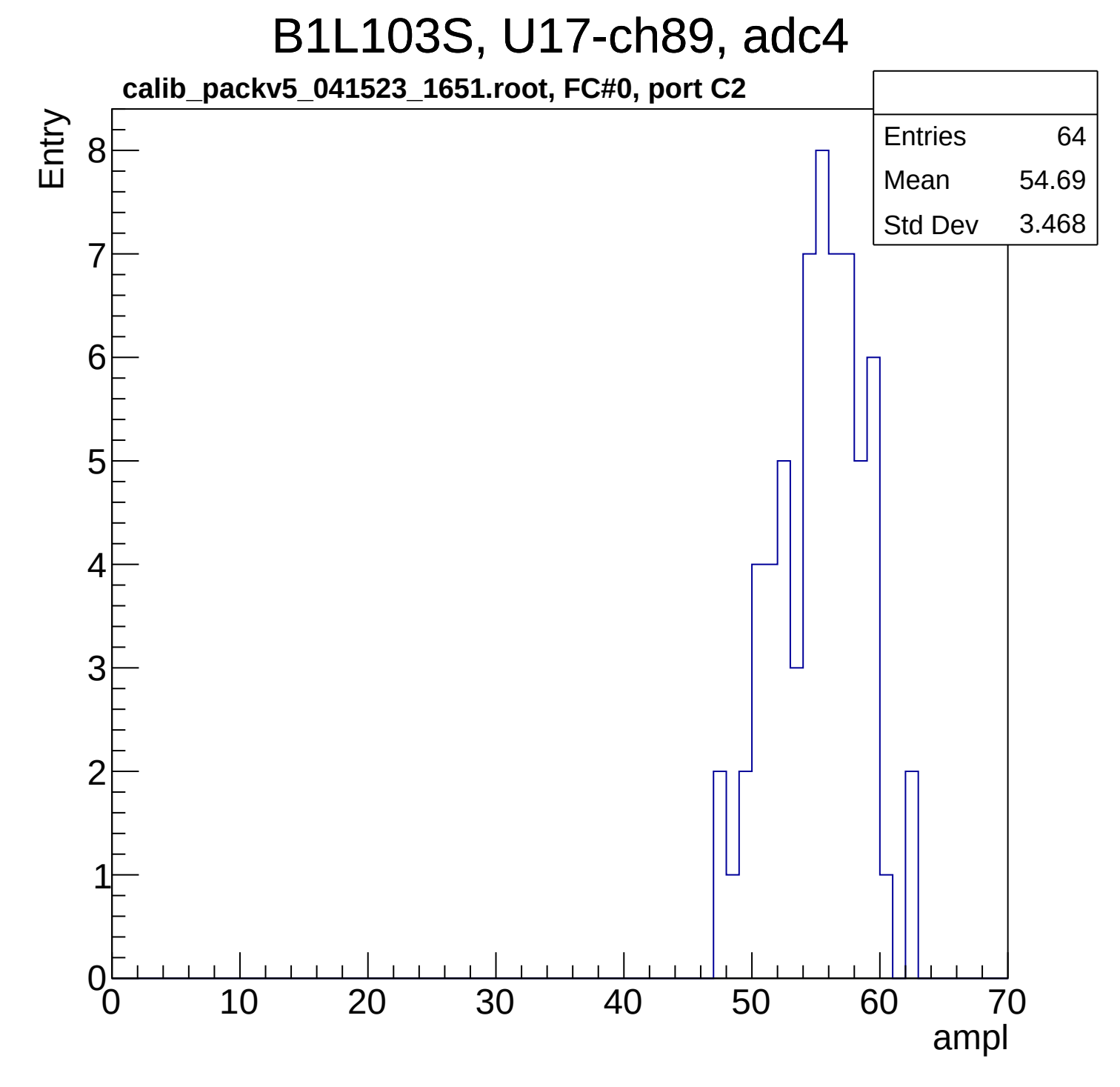

B1L103S, U17-ch89, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 47.74
Std Dev 3.815
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U17-ch89, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 54.69
Std Dev 3.468
Entry
ampl
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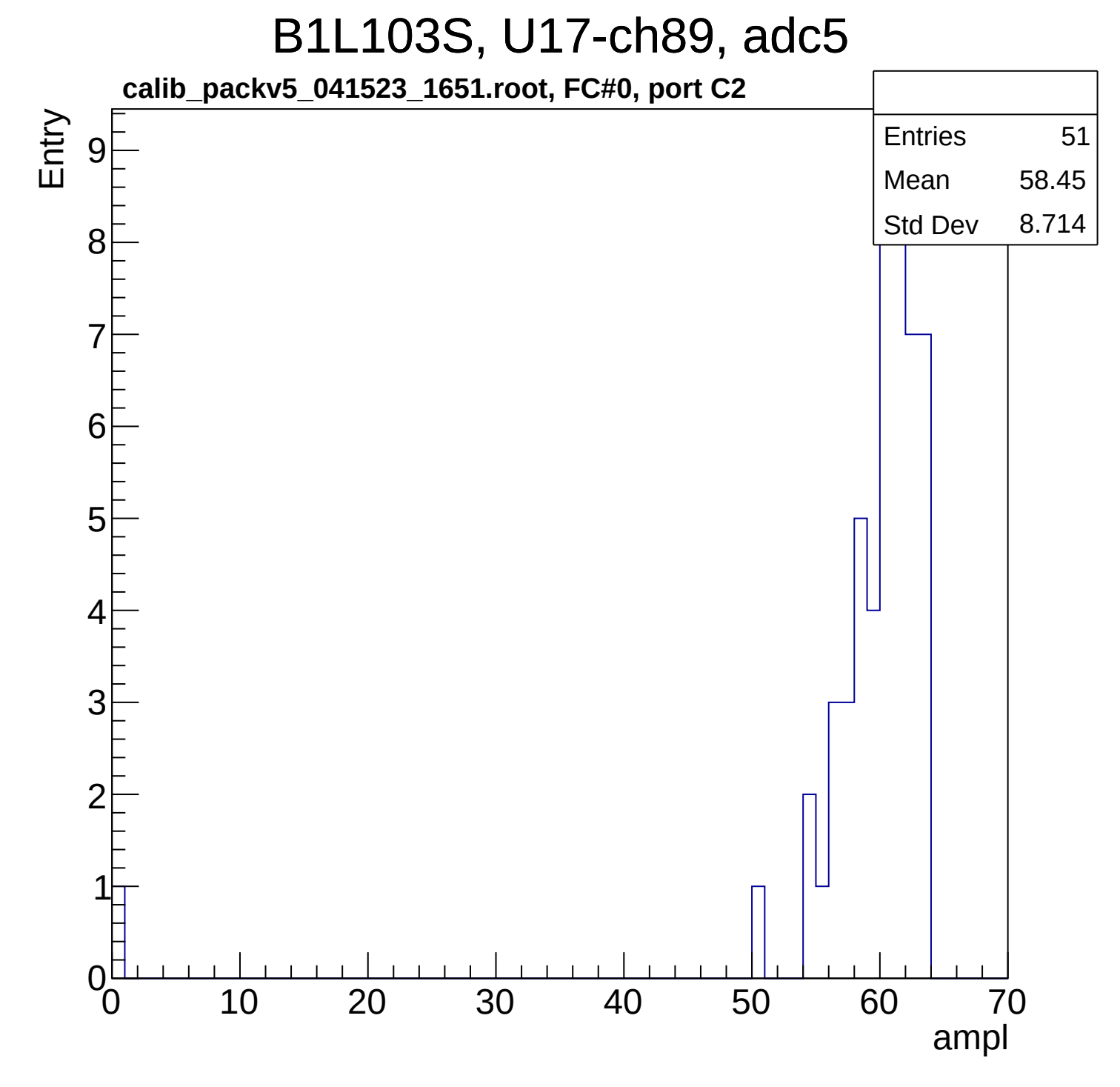
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U17-ch89, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 58.45
Std Dev 8.714
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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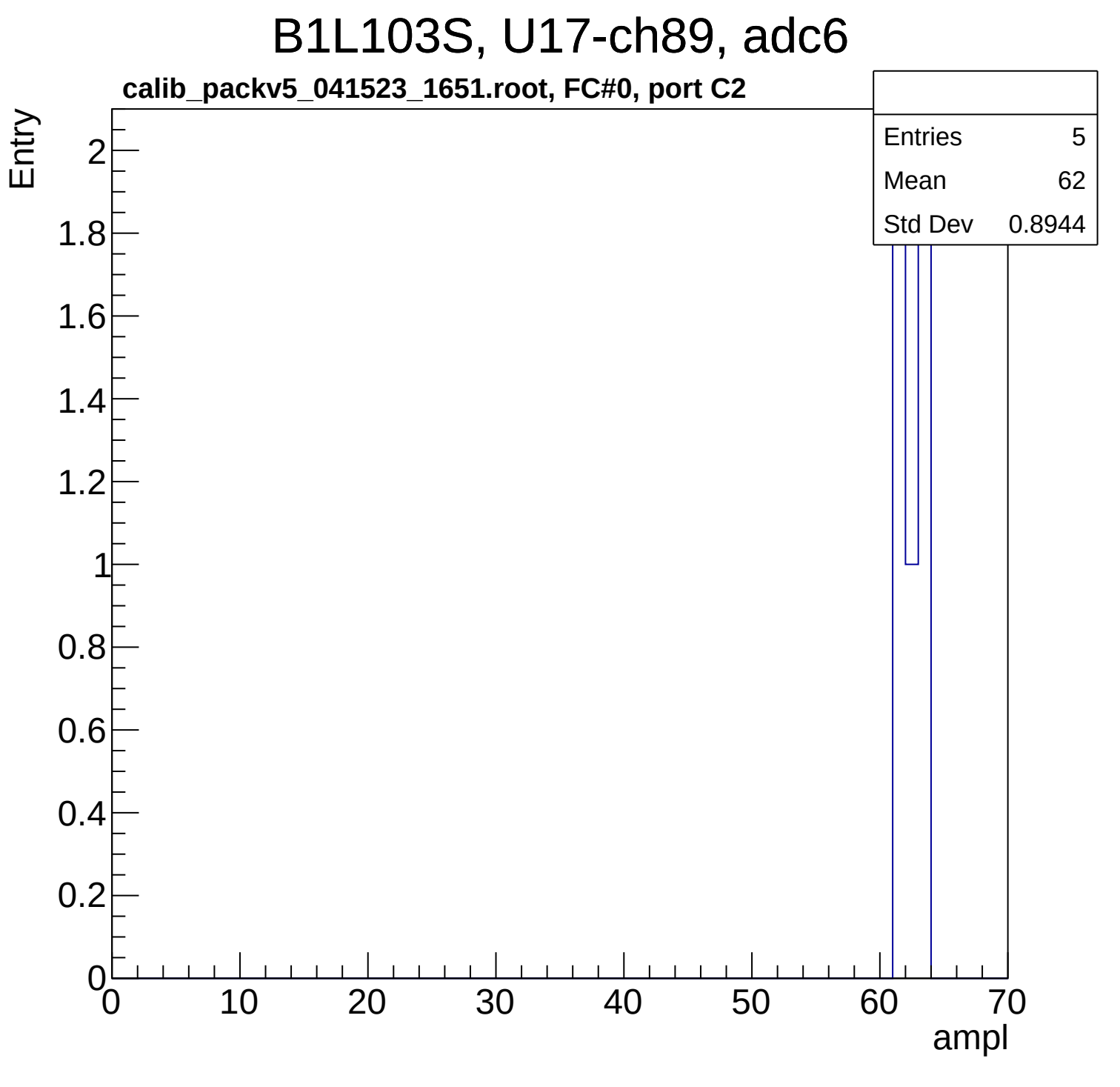
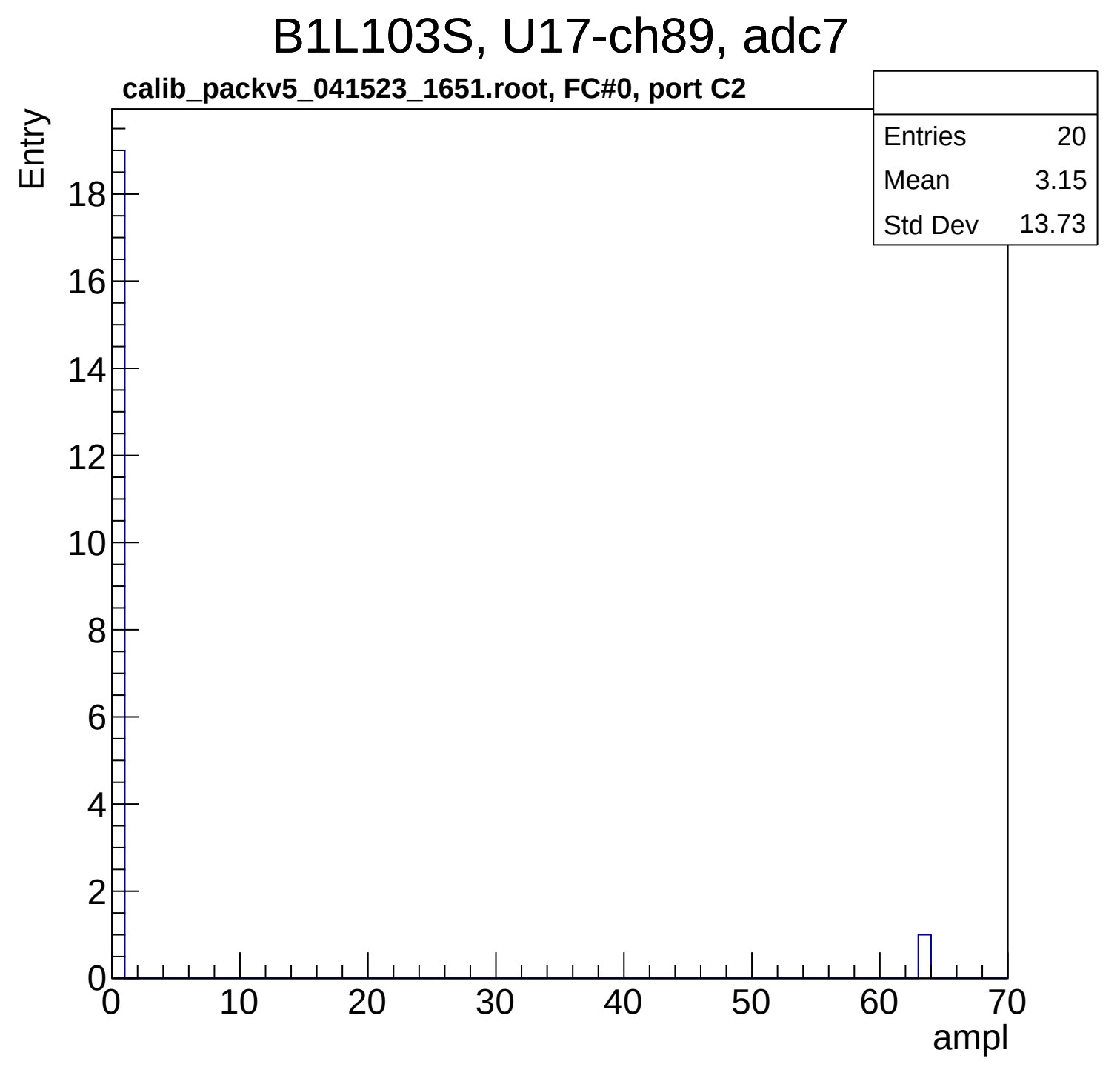
40
50
60
70


B1L103S, U17-ch89, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 5
Mean 62
Std Dev 0.8944
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U17-ch89, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
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6
8
10
12
14
16
18
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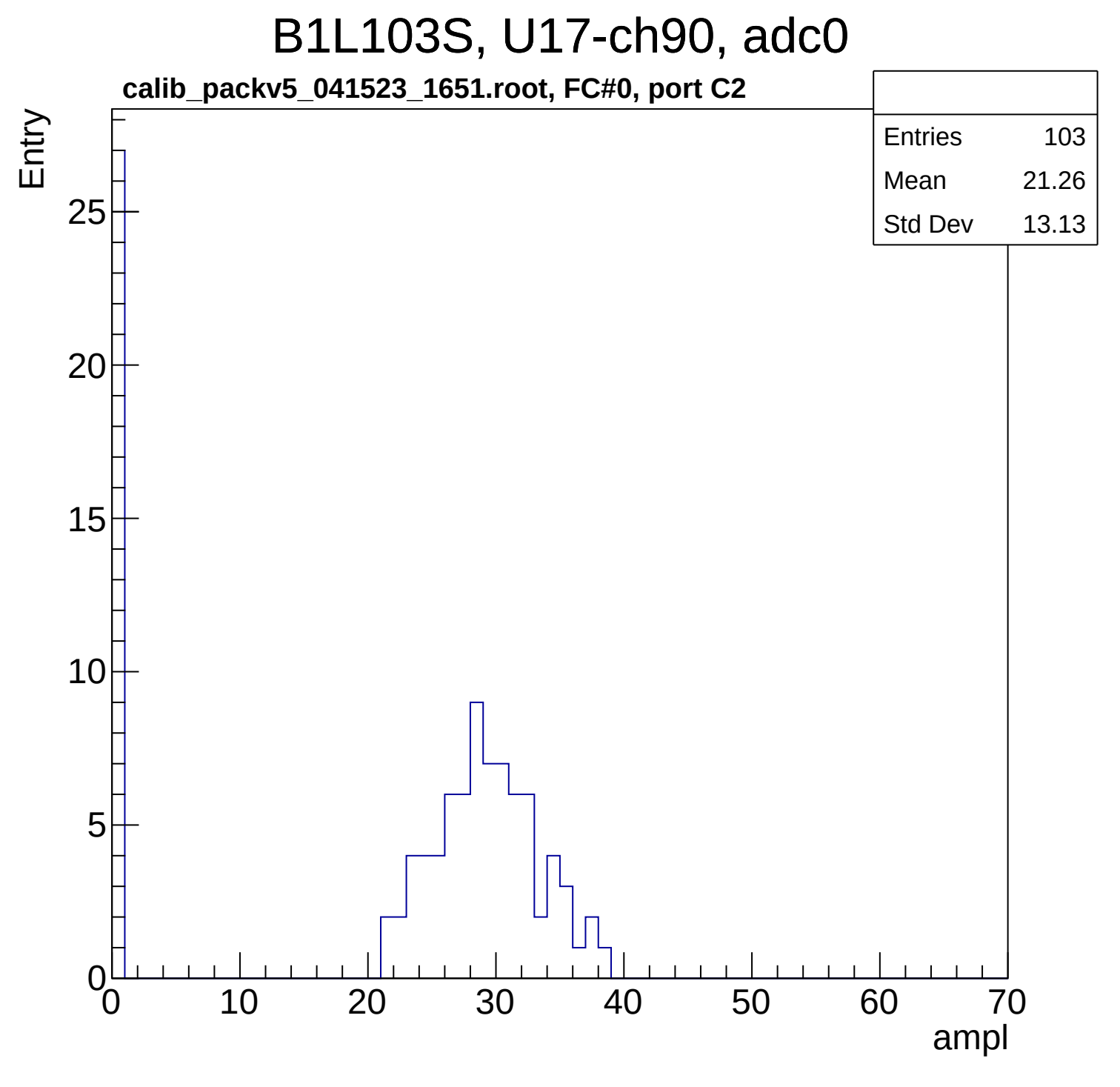
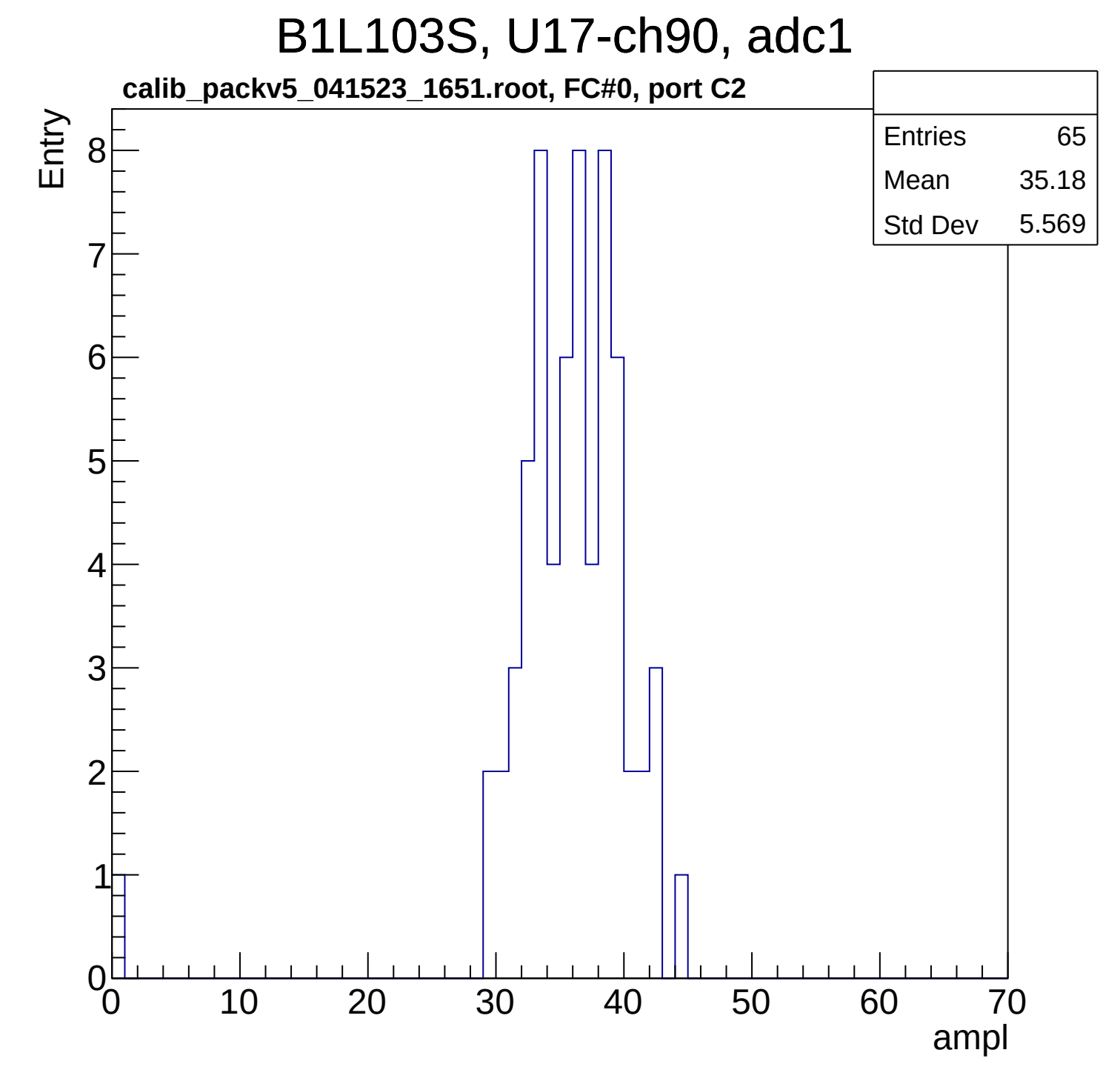
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch90, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 103
Mean 21.26
Std Dev 13.13
Entry
0
5
10
15
20
25
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch90, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 35.18
Std Dev 5.569
Entry
ampl
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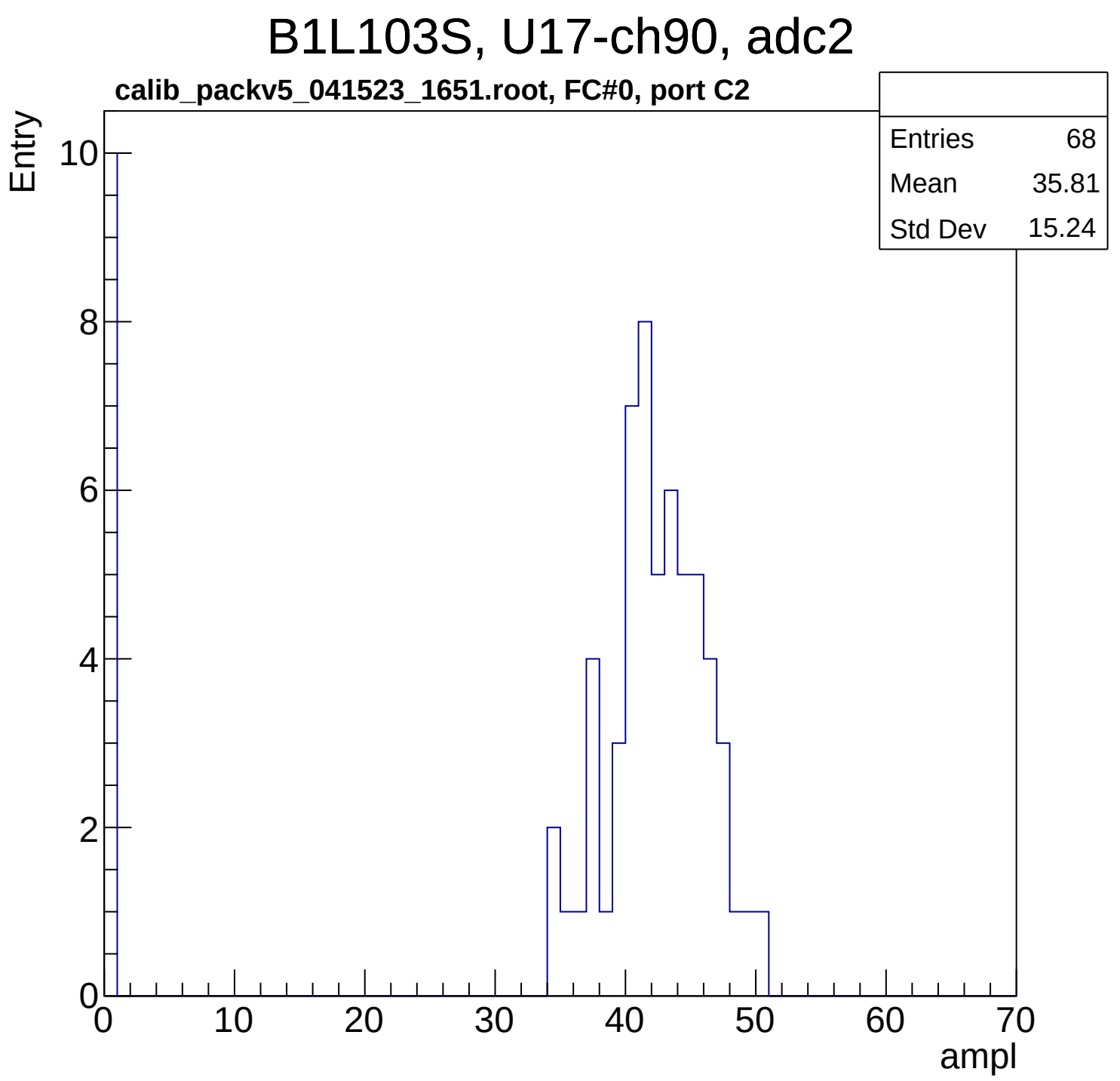
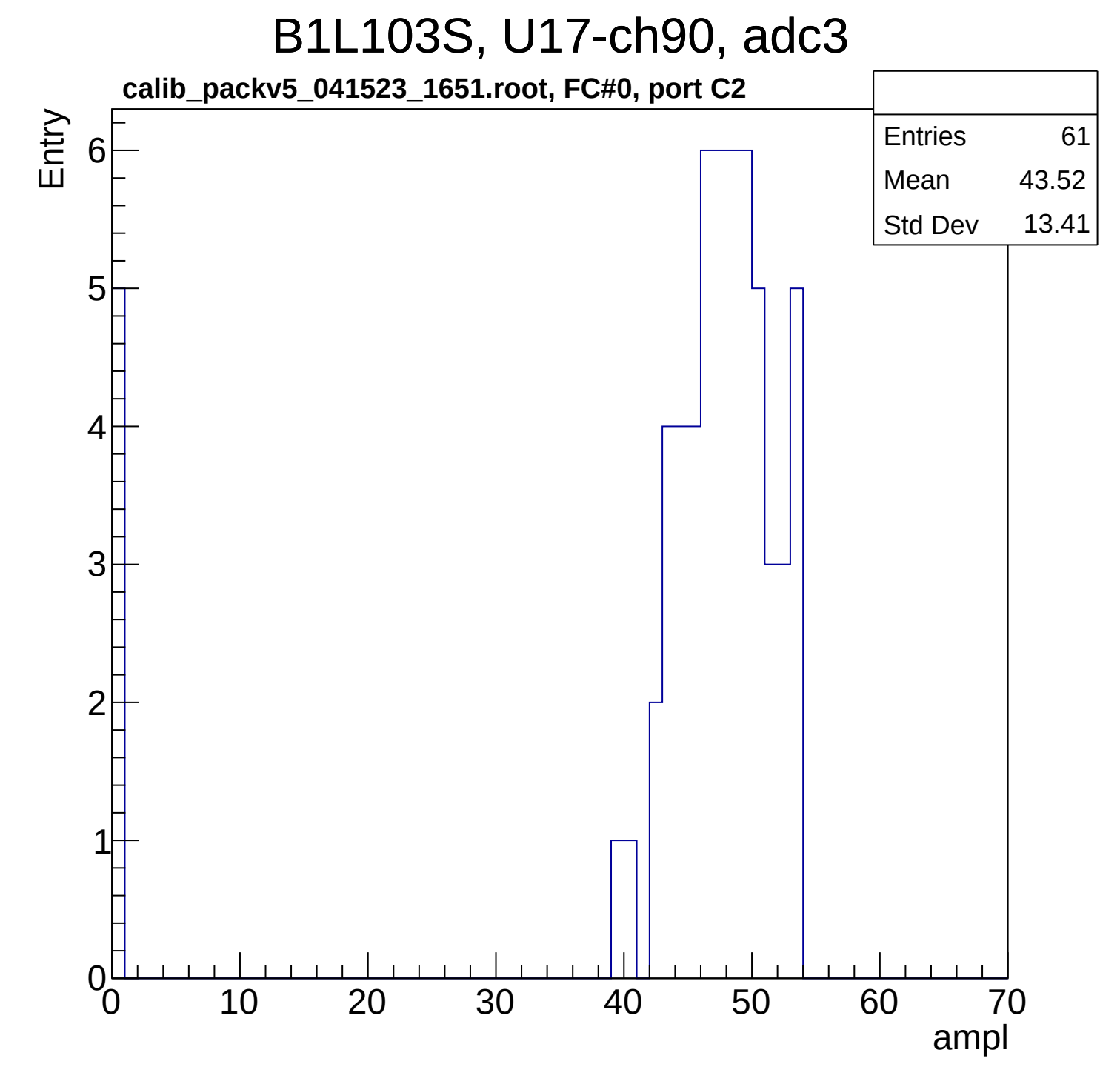
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U17-ch90, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 35.81
Std Dev 15.24
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch90, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 43.52
Std Dev 13.41
Entry
0
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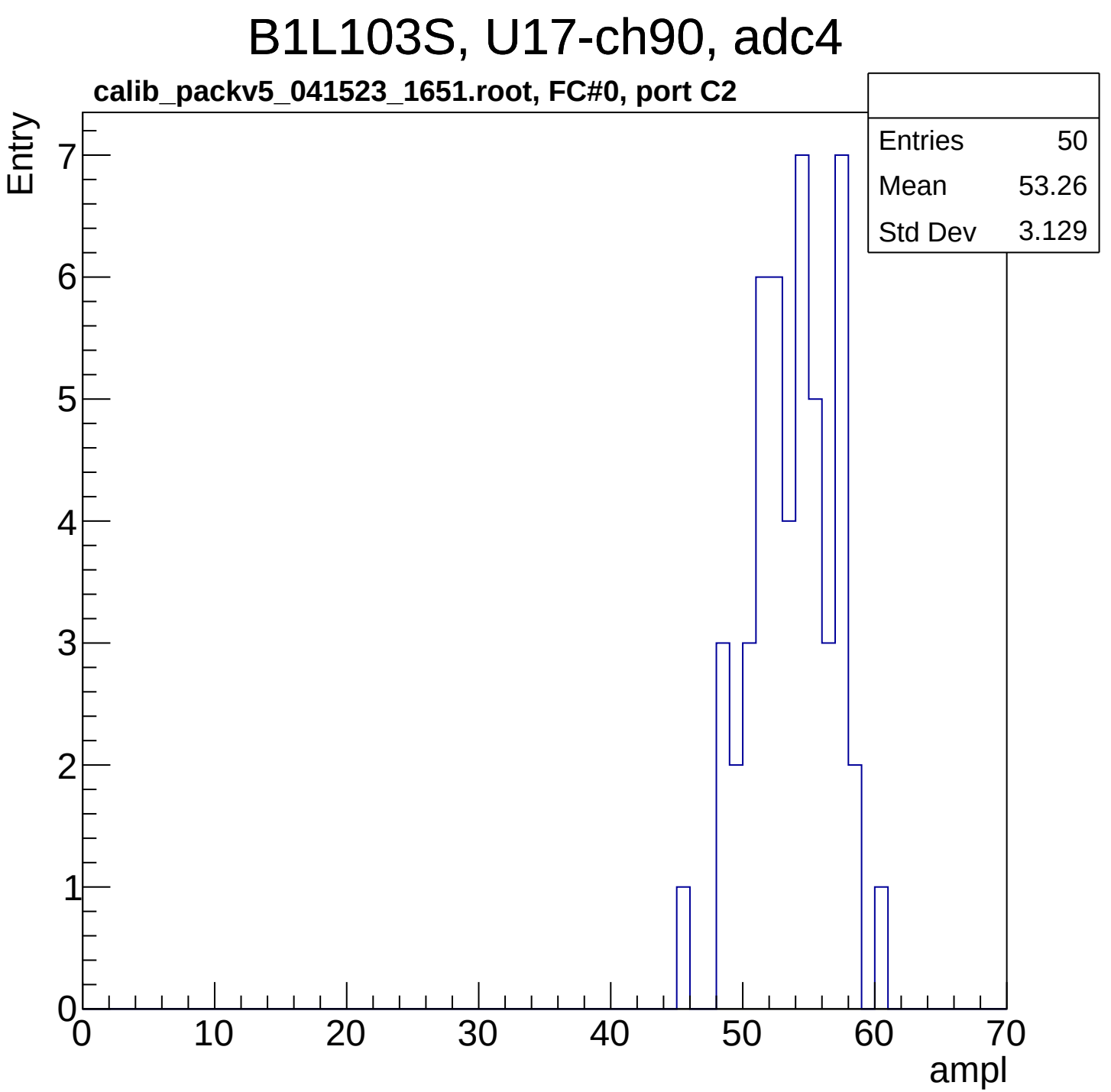
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch90, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 53.26
Std Dev 3.129
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
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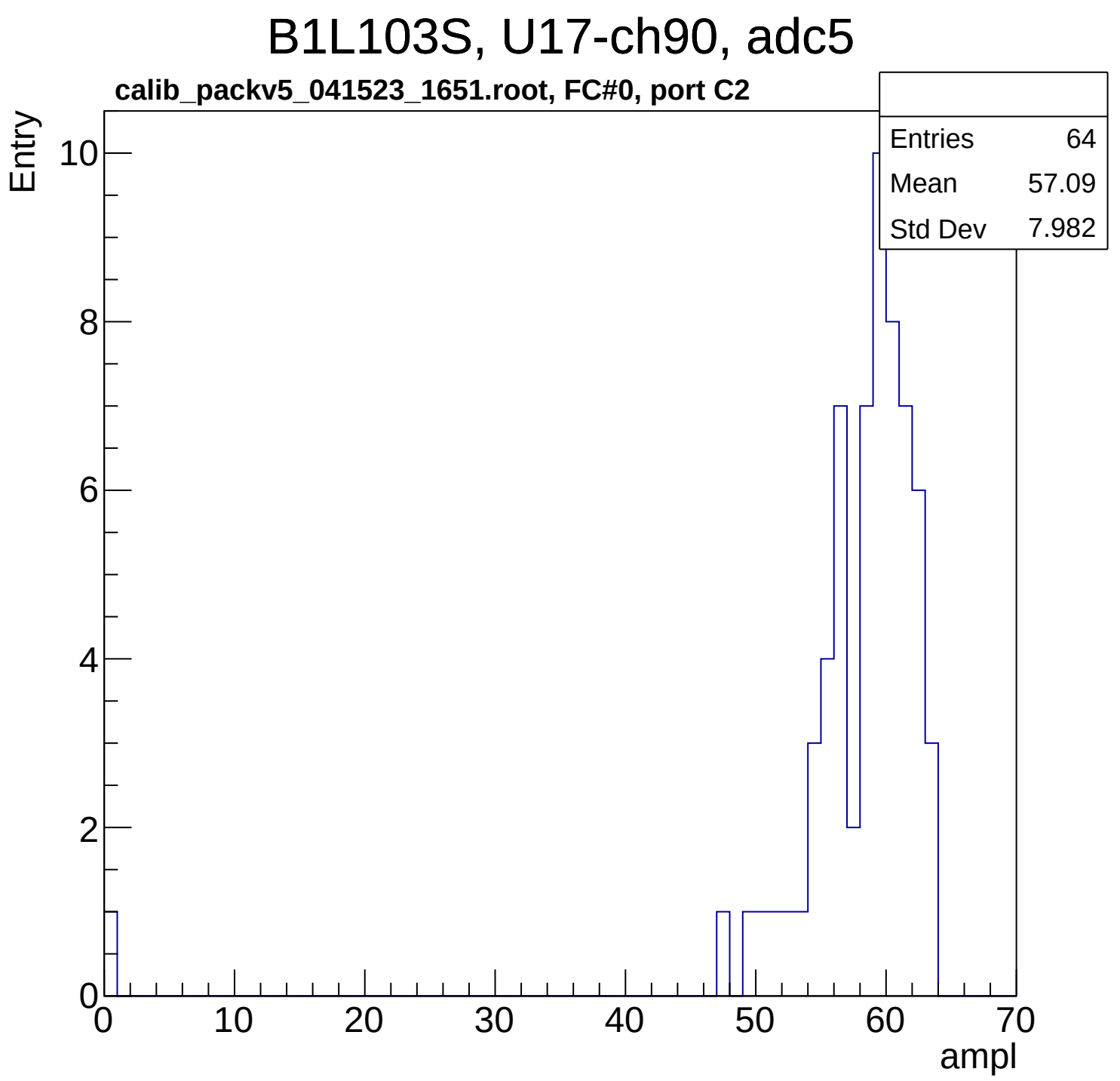
40
50
60
70


B1L103S, U17-ch90, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 57.09
Std Dev 7.982
Entry
ampl
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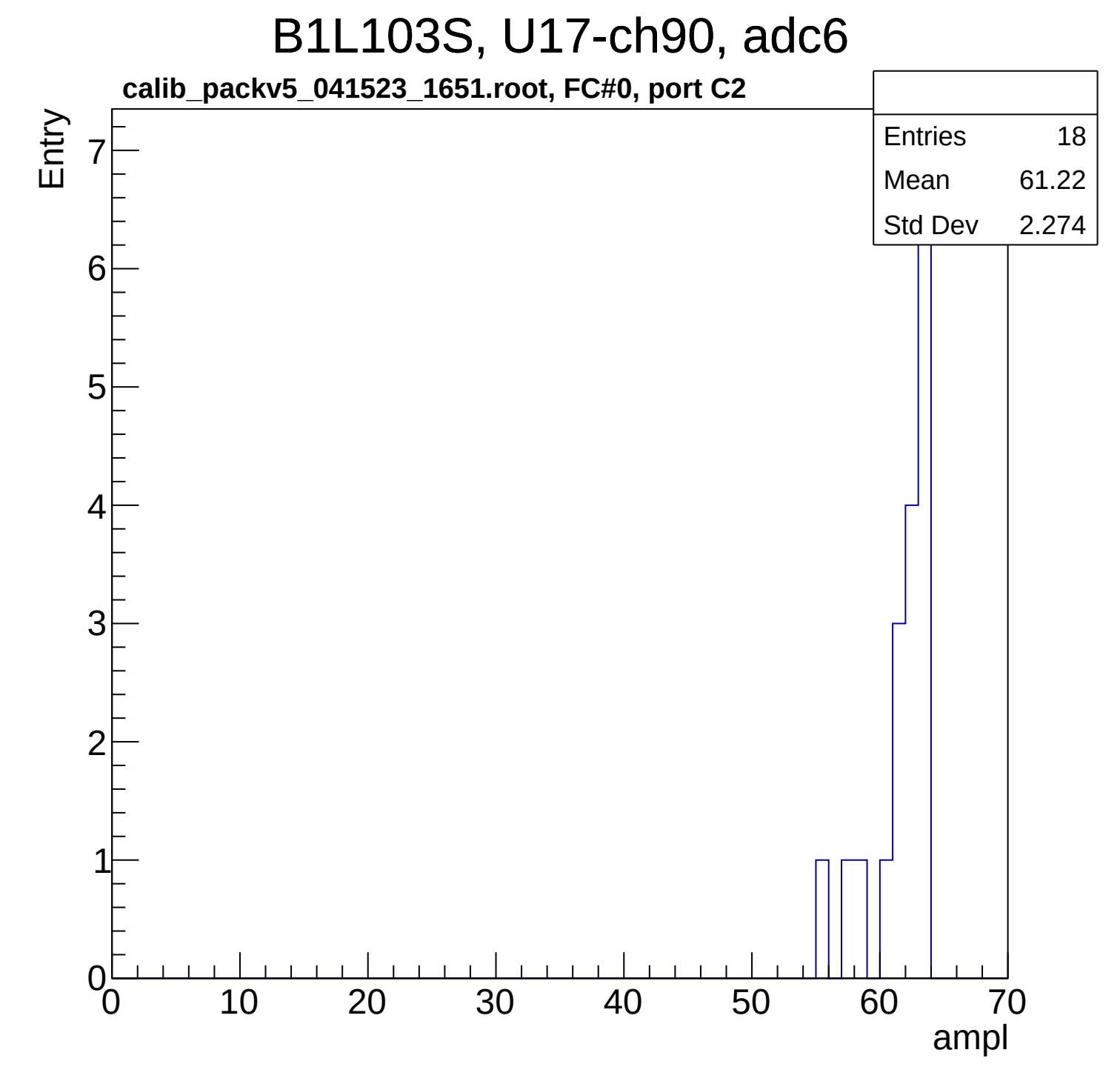
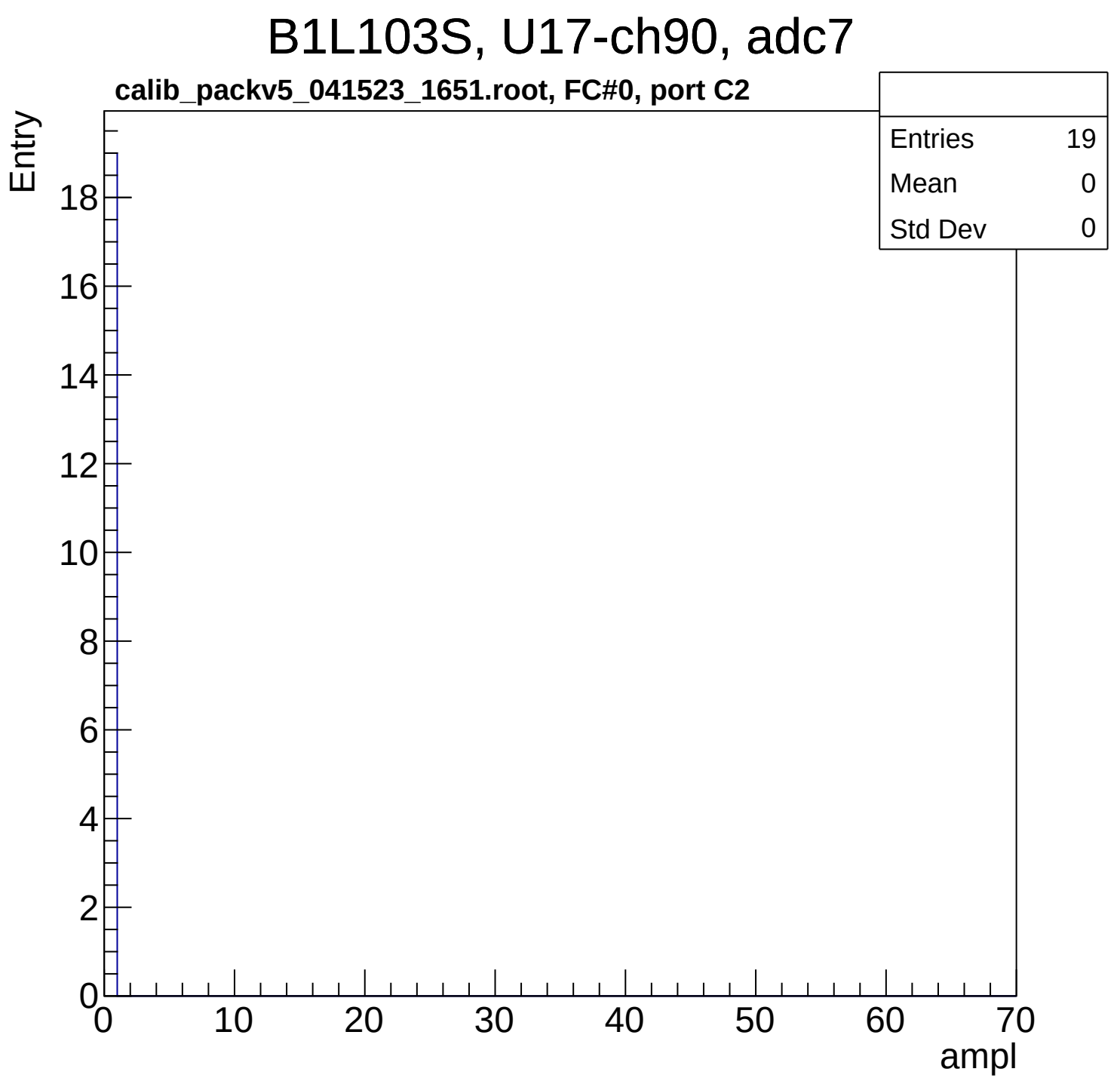
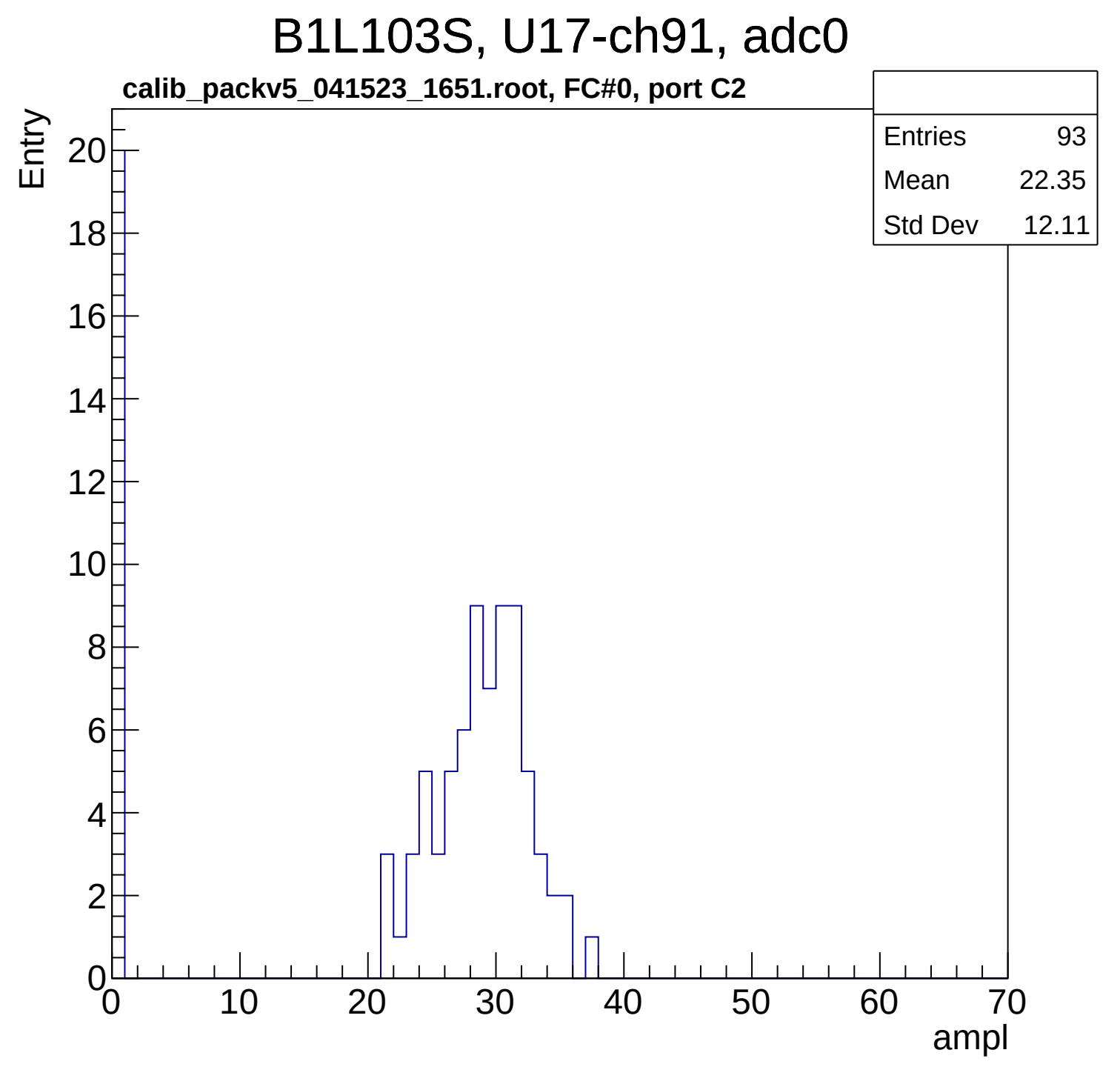
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U17-ch90, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 61.22
Std Dev 2.274
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U17-ch90, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch91, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 93
Mean 22.35
Std Dev 12.11
Entry
ampl
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6
8
10
12
14
16
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0
10
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40
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60
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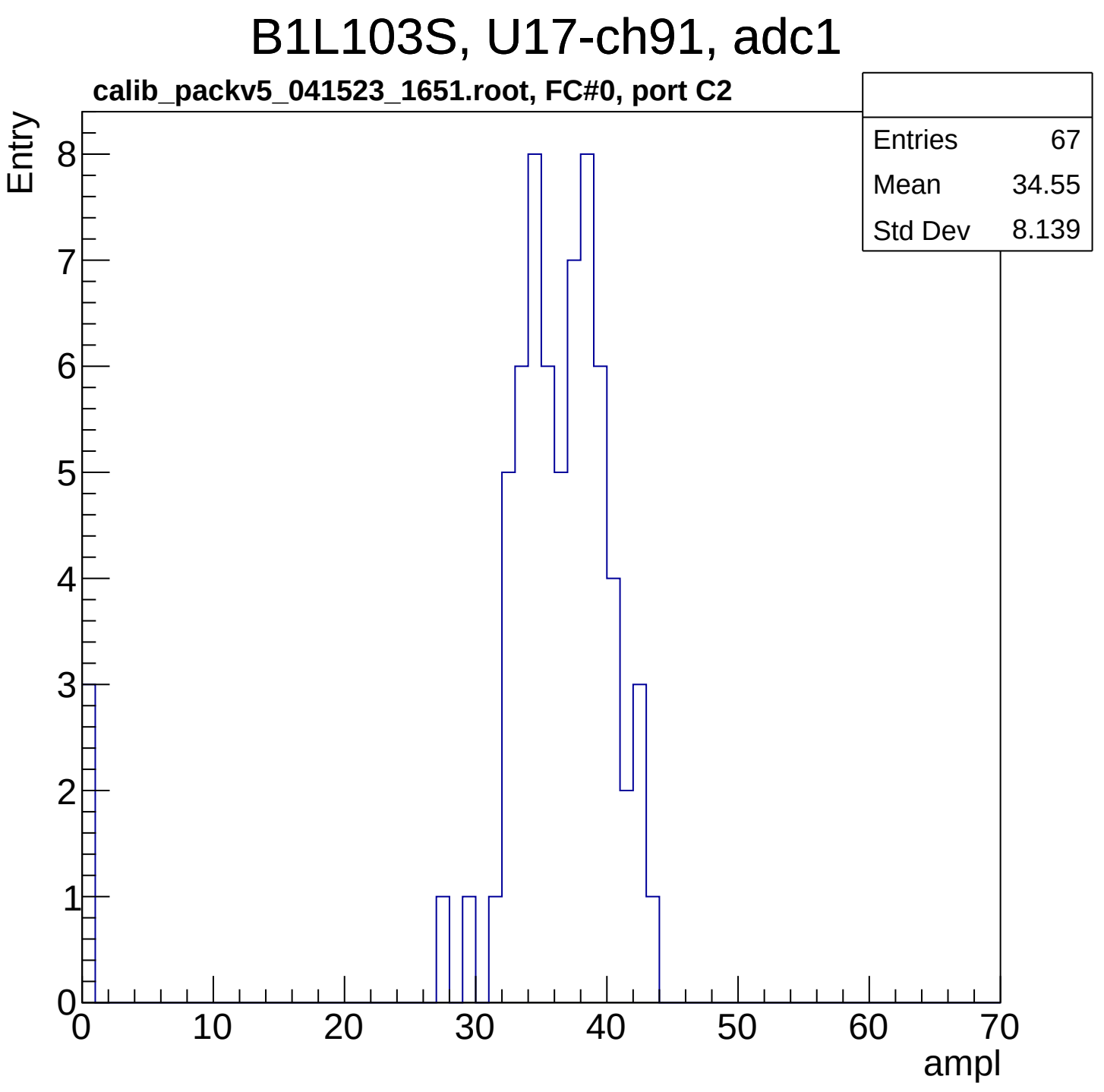
B1L103S, U17-ch91, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 34.55
Std Dev 8.139
Entry
ampl
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4
5
6
7
8
0
10
20
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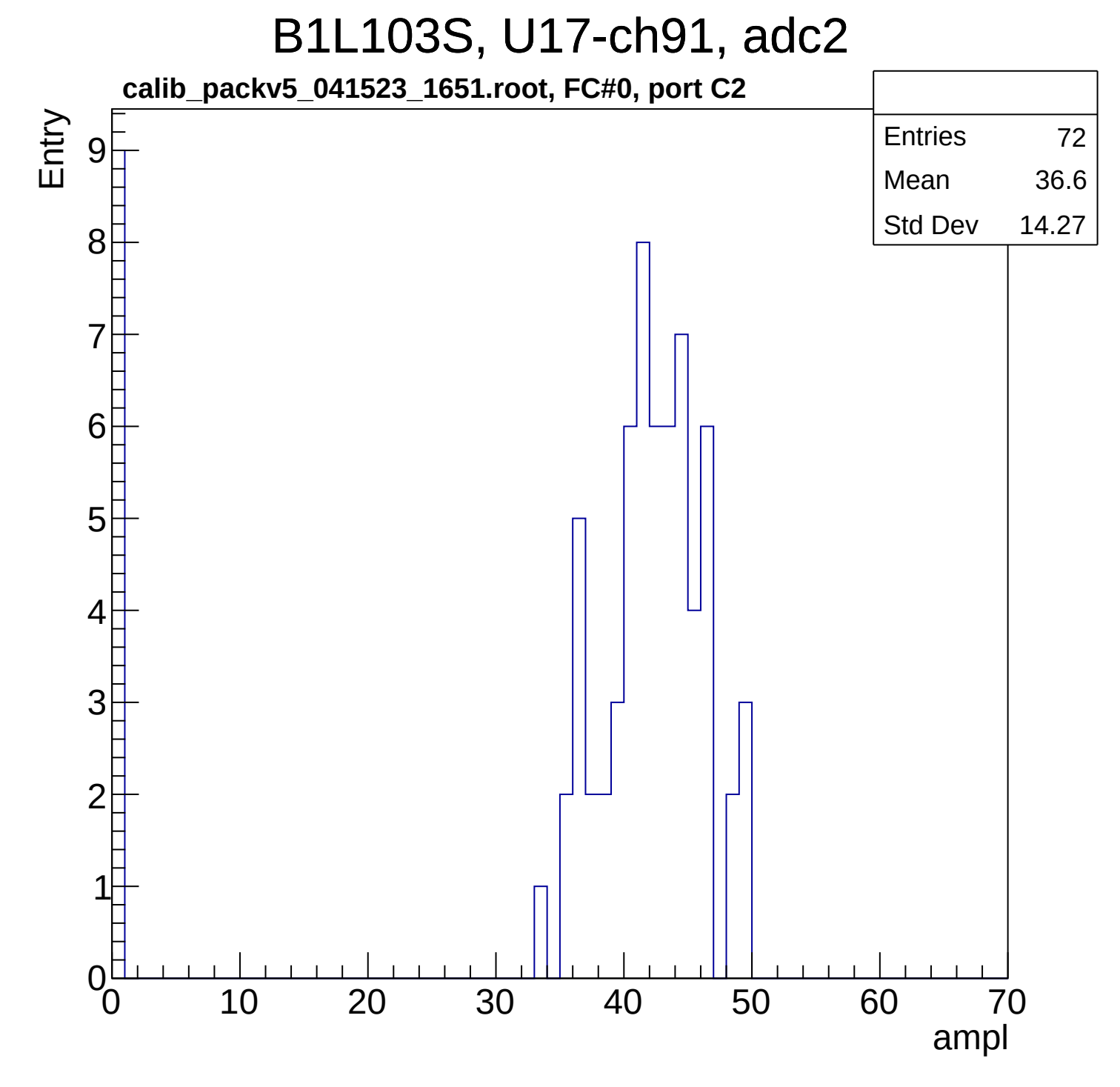
40
50
60
70


B1L103S, U17-ch91, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 36.6
Std Dev 14.27
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
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60
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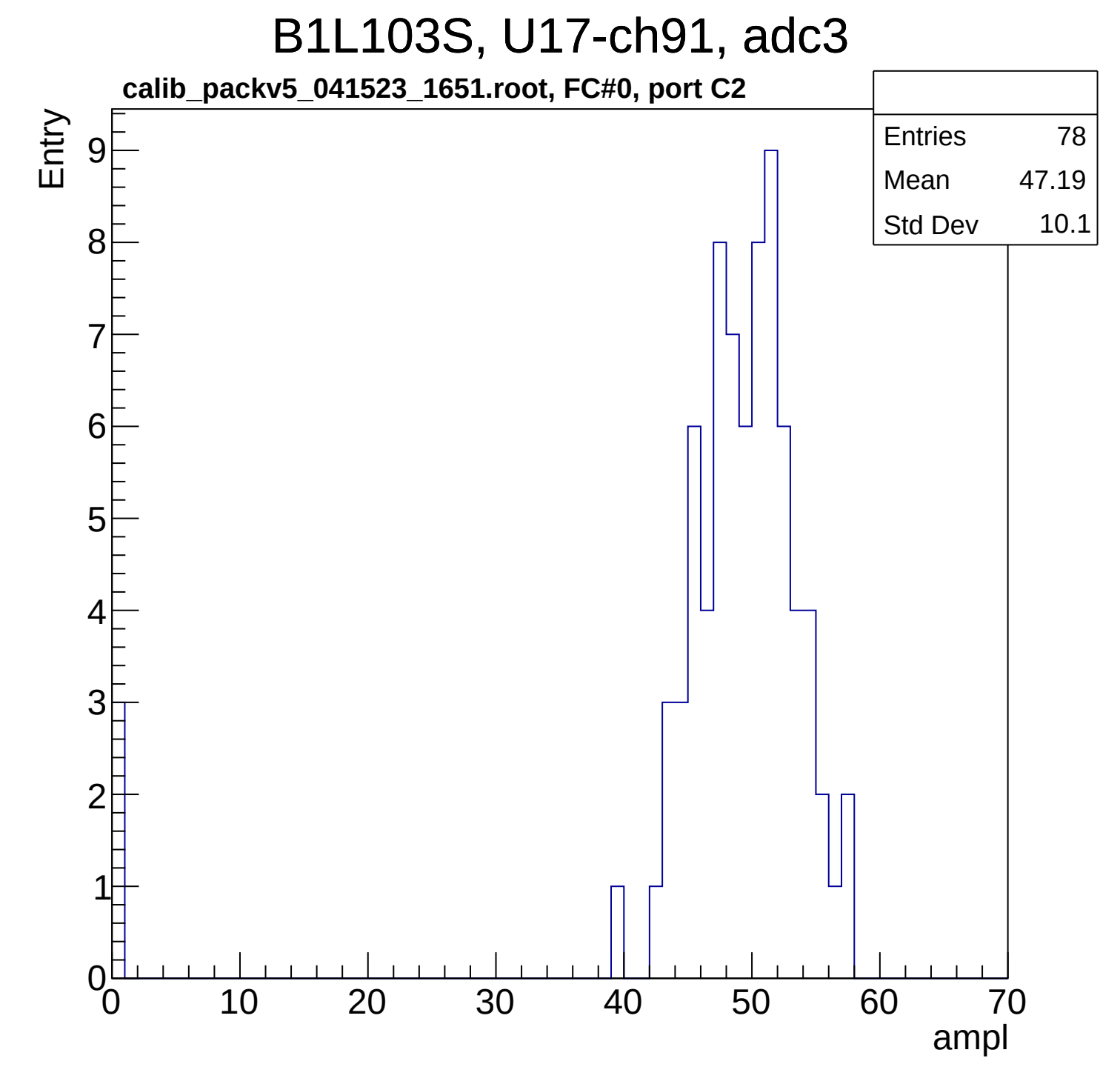
B1L103S, U17-ch91, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 47.19
Std Dev 10.1
Entry
ampl
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10
20
30
40
50
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1
2
3
4
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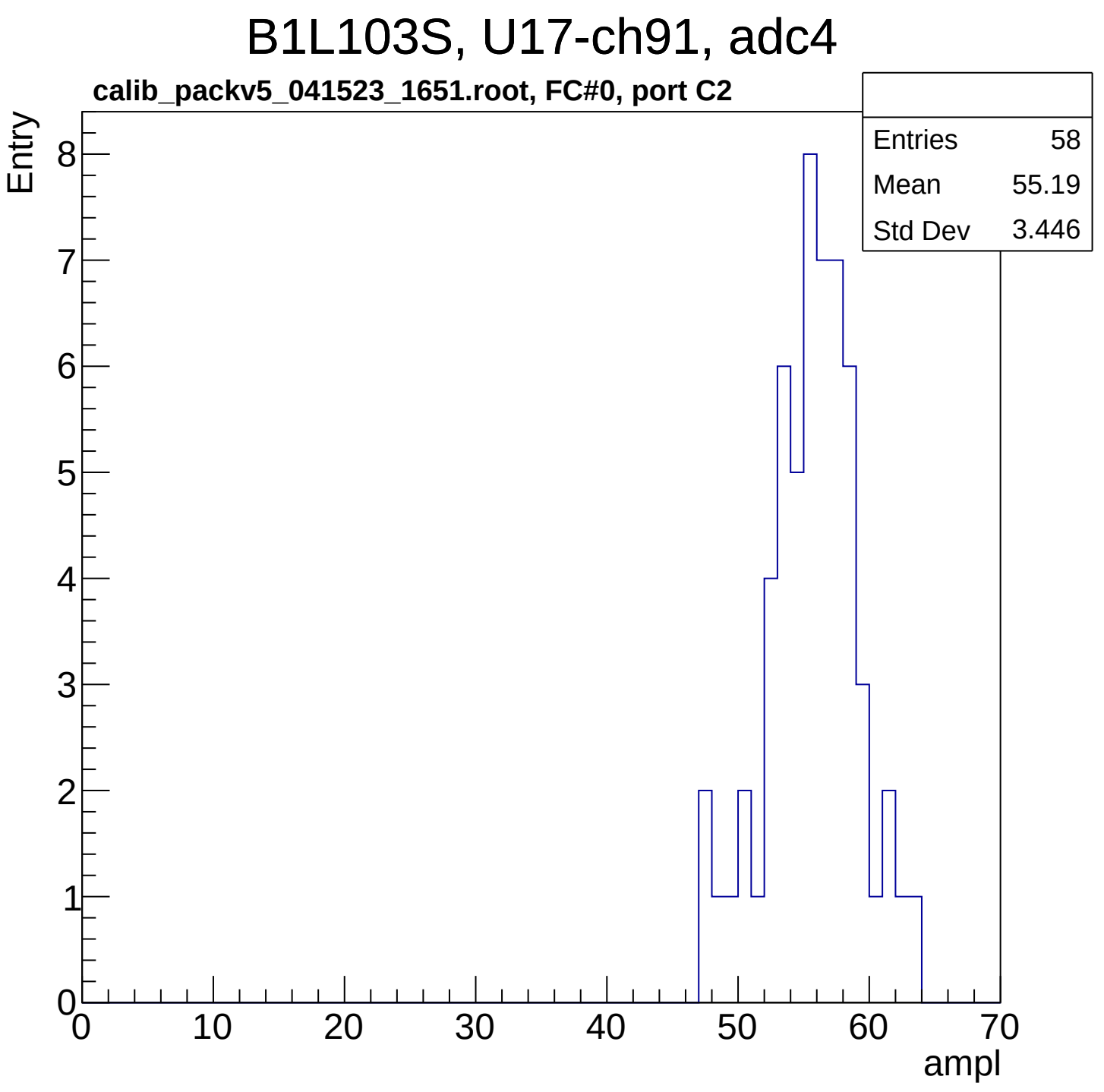
6
7
8
9


B1L103S, U17-ch91, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 55.19
Std Dev 3.446
Entry
ampl
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1
2
3
4
5
6
7
8
0
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40
50
60
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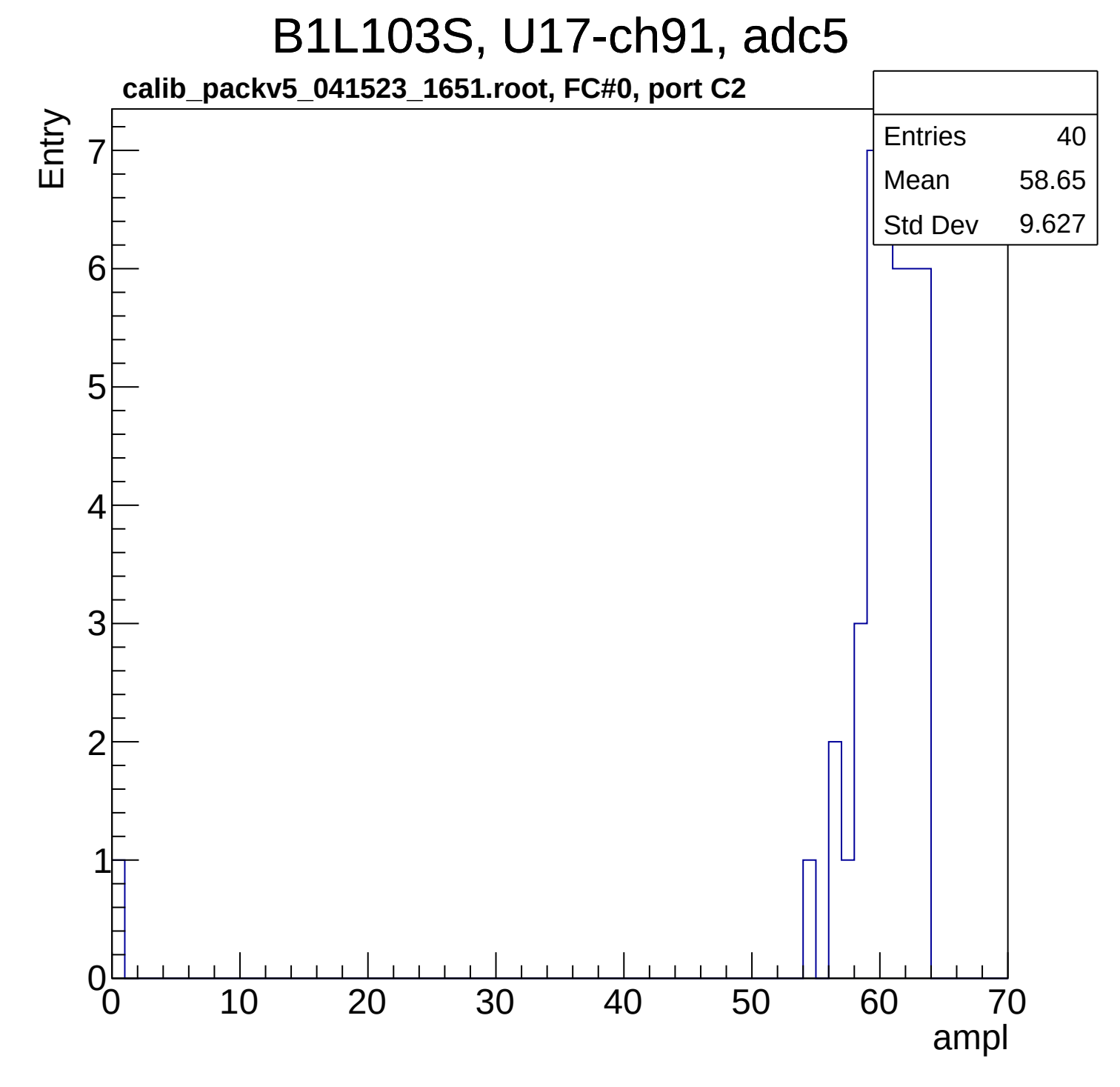
B1L103S, U17-ch91, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 40
Mean 58.65
Std Dev 9.627
Entry
ampl
0
1
2
3
4
5
6
7
0
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20
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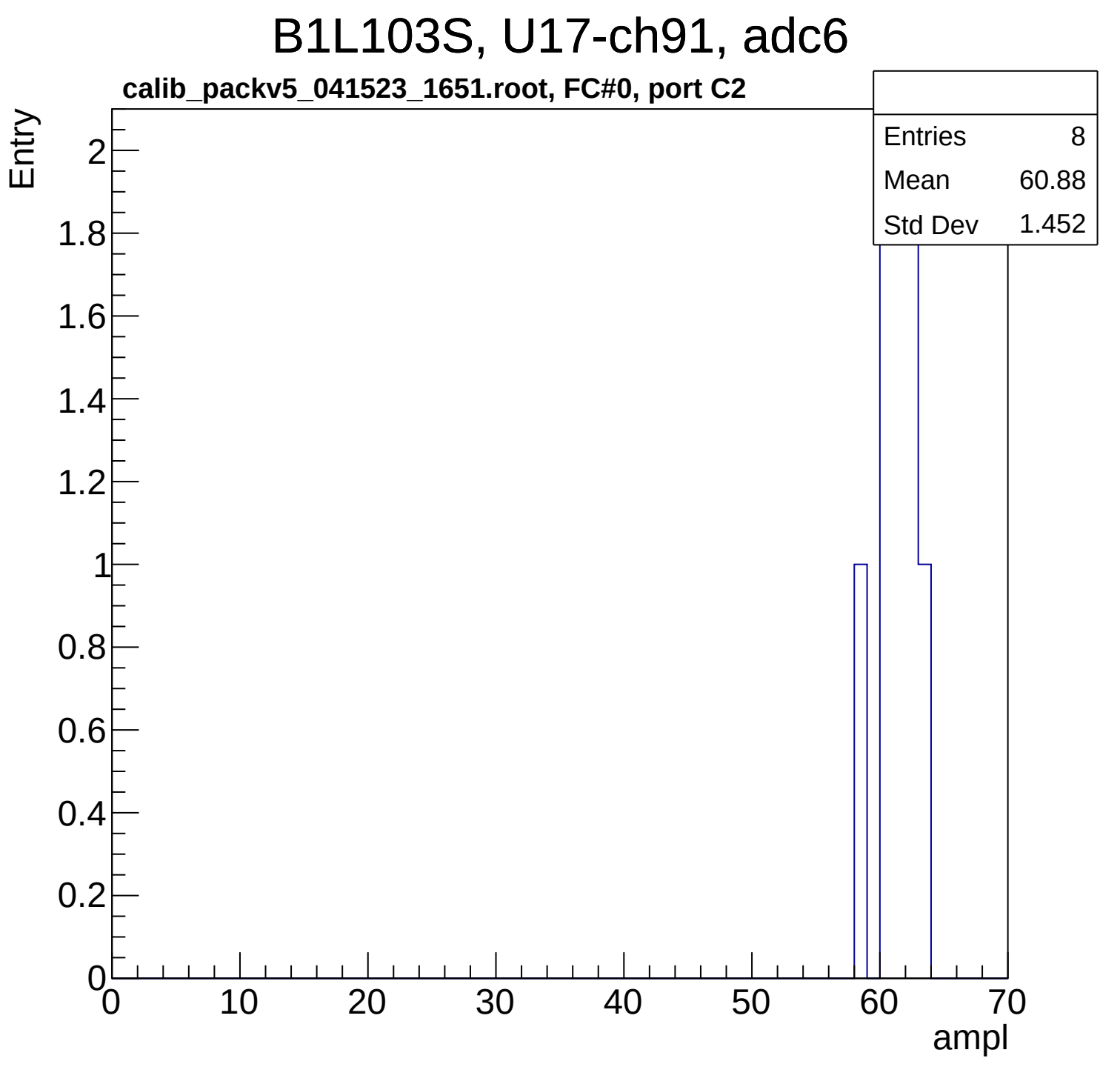
40
50
60
70


B1L103S, U17-ch91, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 60.88
Std Dev 1.452
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
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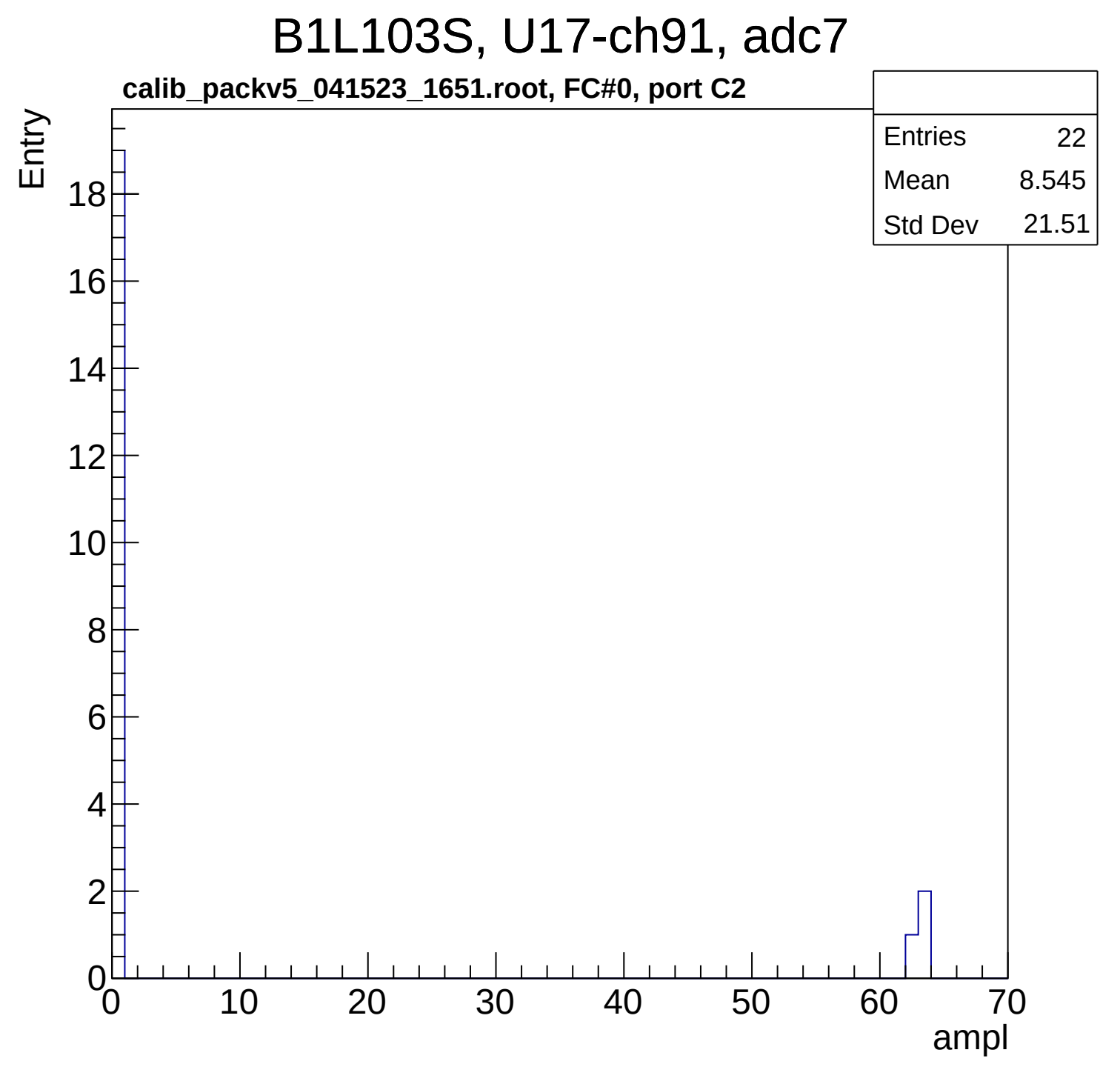
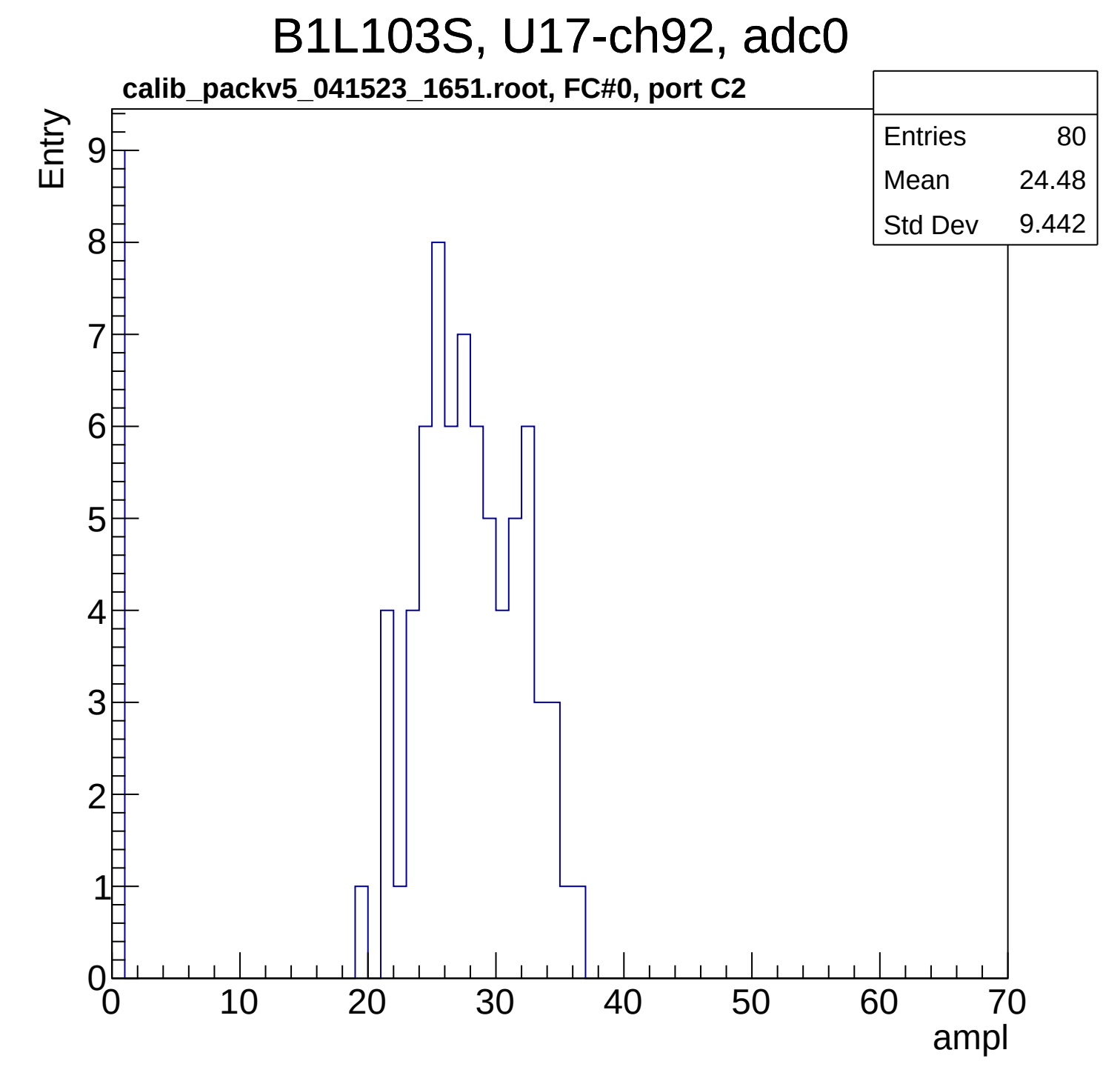

B1L103S, U17-ch91, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 8.545
Std Dev 21.51
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch92, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 24.48
Std Dev 9.442
Entry
ampl
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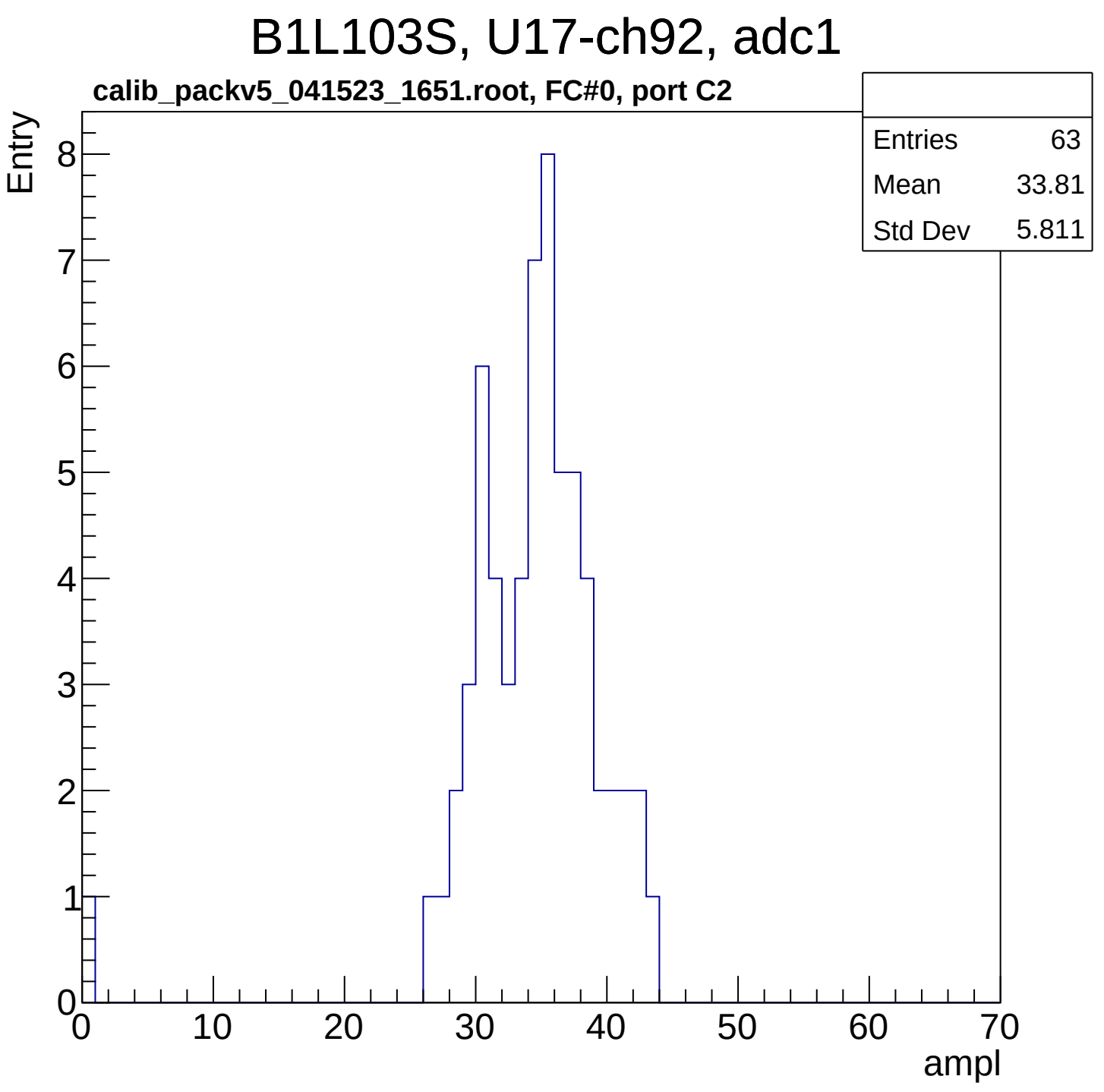
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U17-ch92, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 33.81
Std Dev 5.811
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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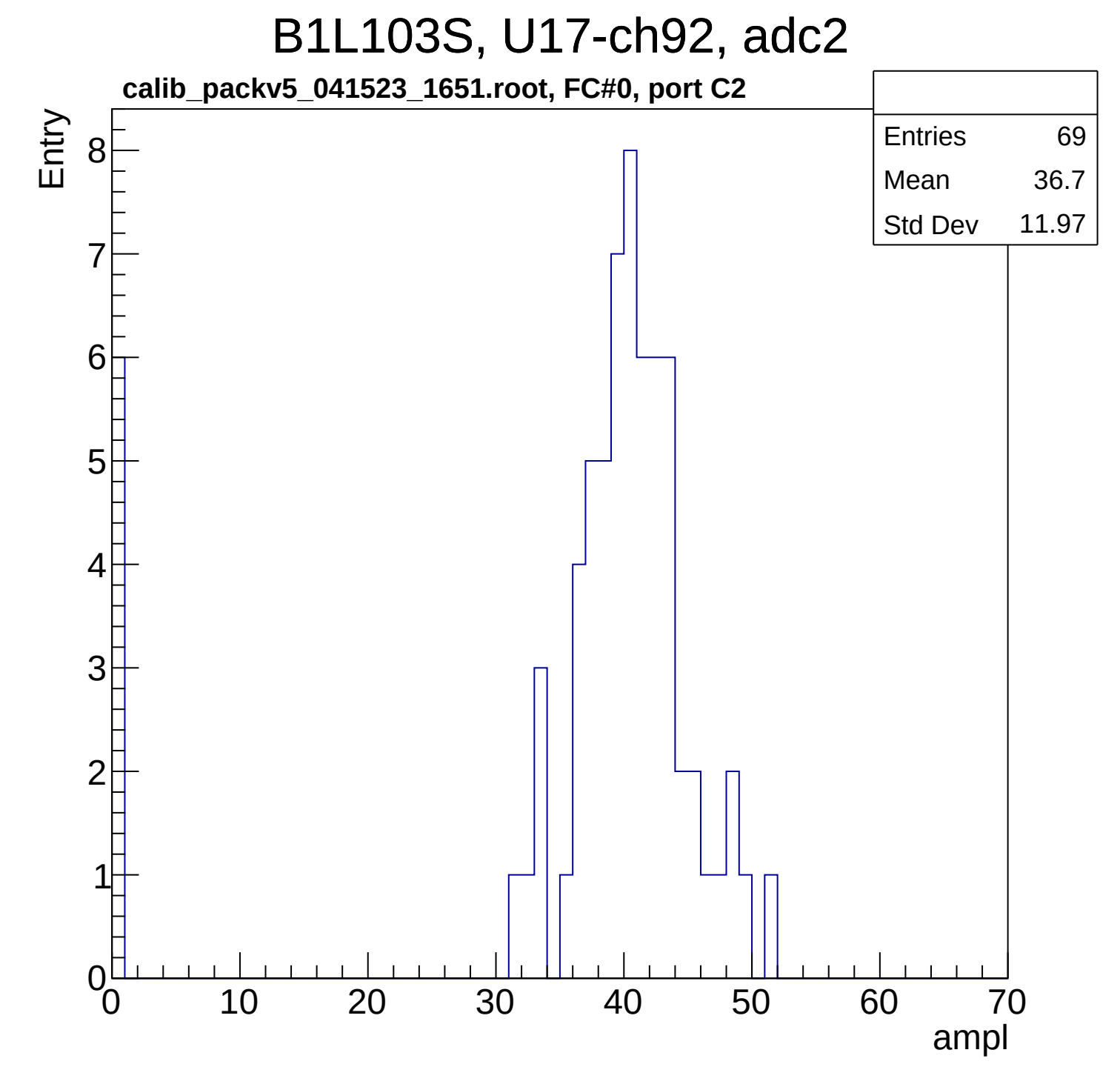
B1L103S, U17-ch92, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 36.7
Std Dev 11.97
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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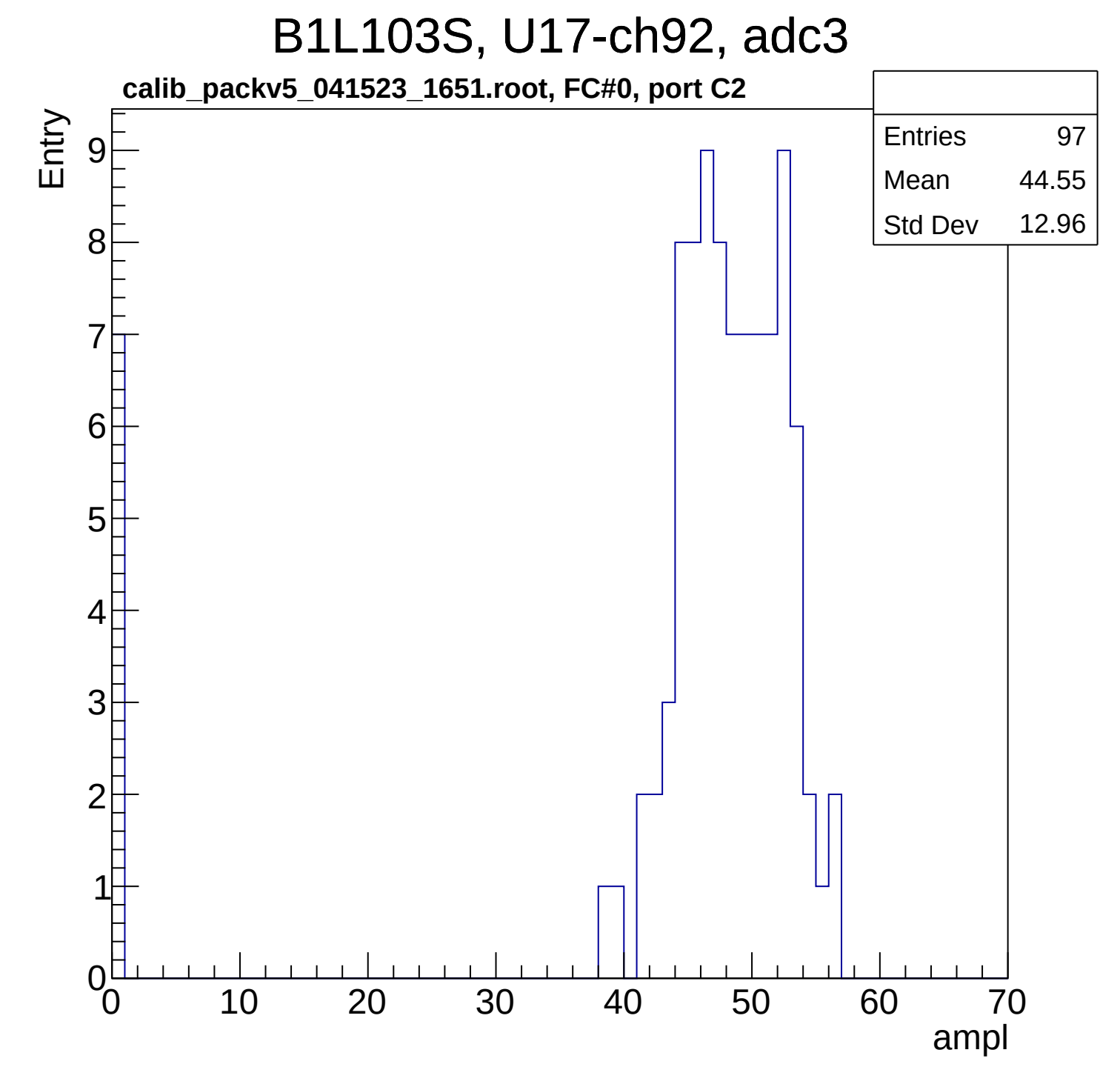
B1L103S, U17-ch92, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 97
Mean 44.55
Std Dev 12.96
Entry
ampl
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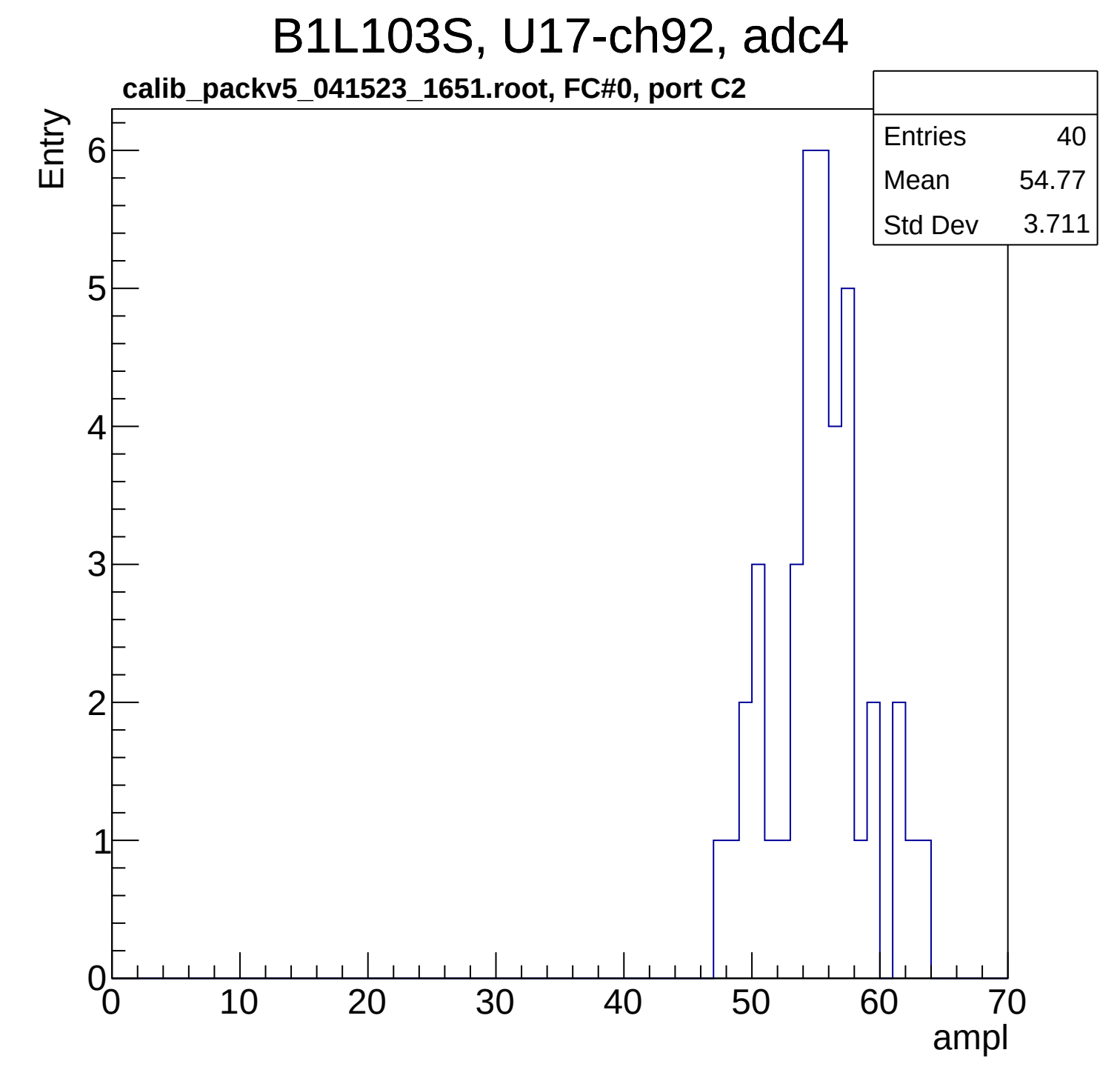
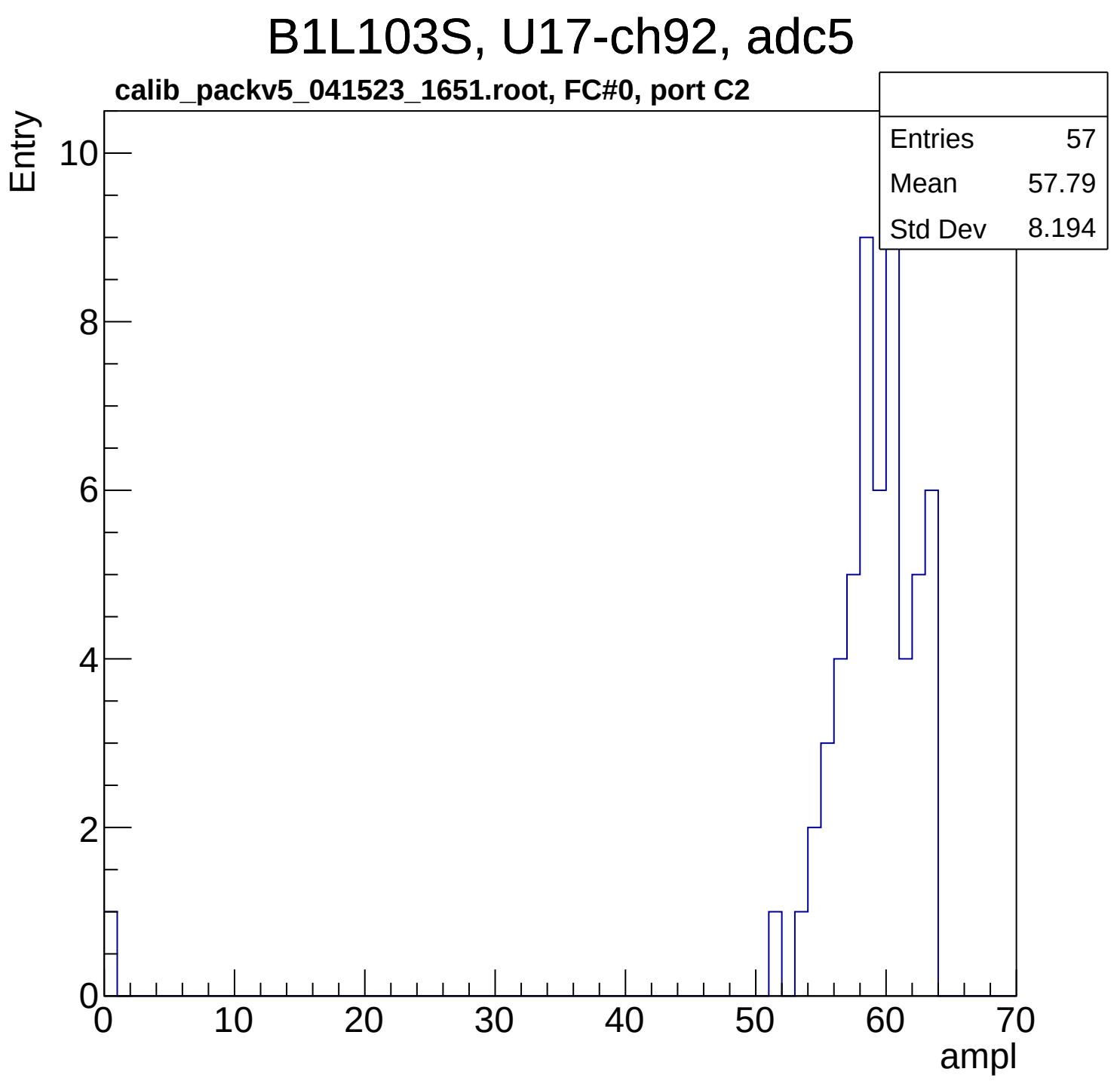
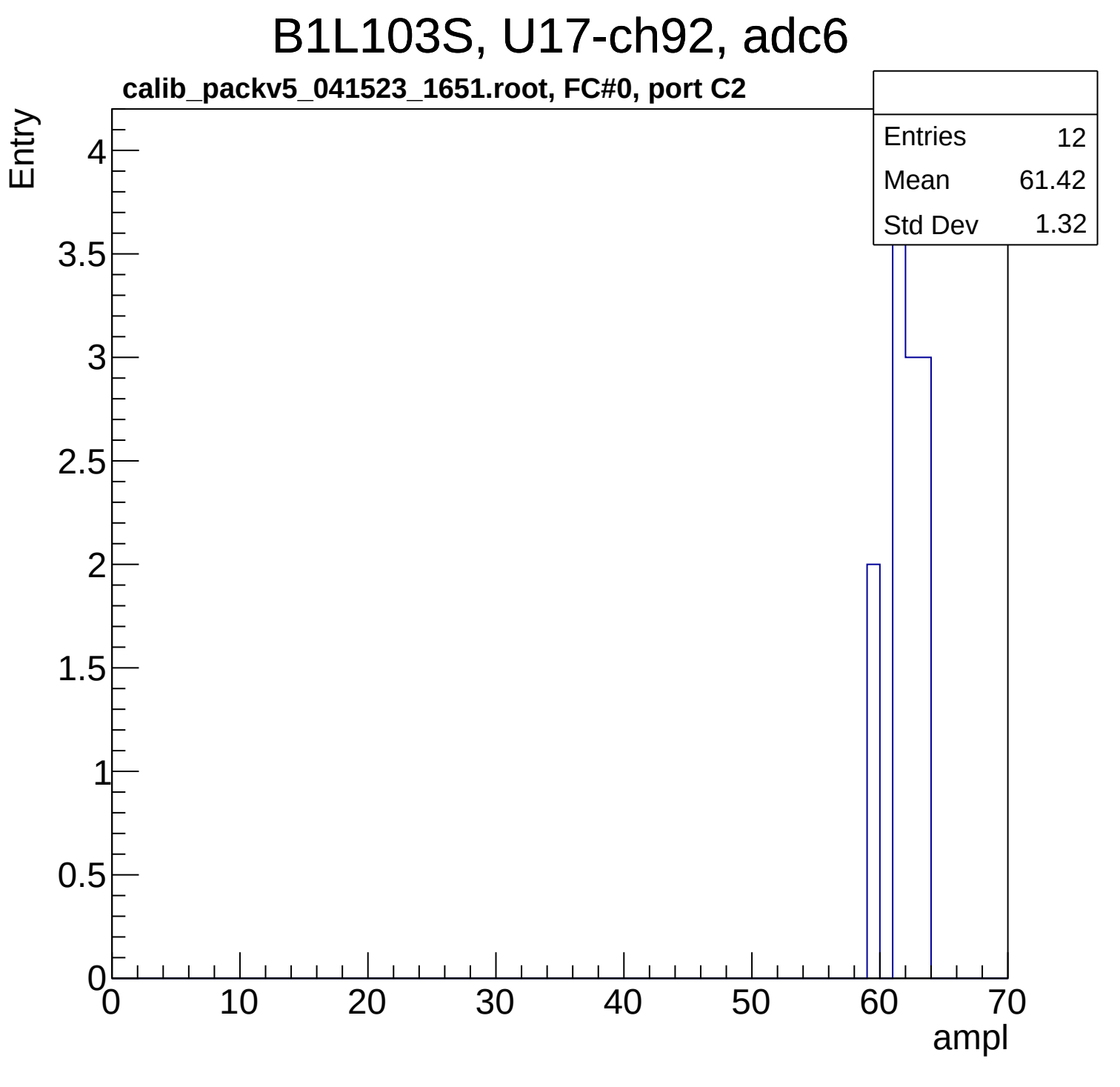
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9


B1L103S, U17-ch92, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 40
Mean 54.77
Std Dev 3.711
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U17-ch92, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 57.79
Std Dev 8.194
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch92, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 61.42
Std Dev 1.32
Entry
ampl
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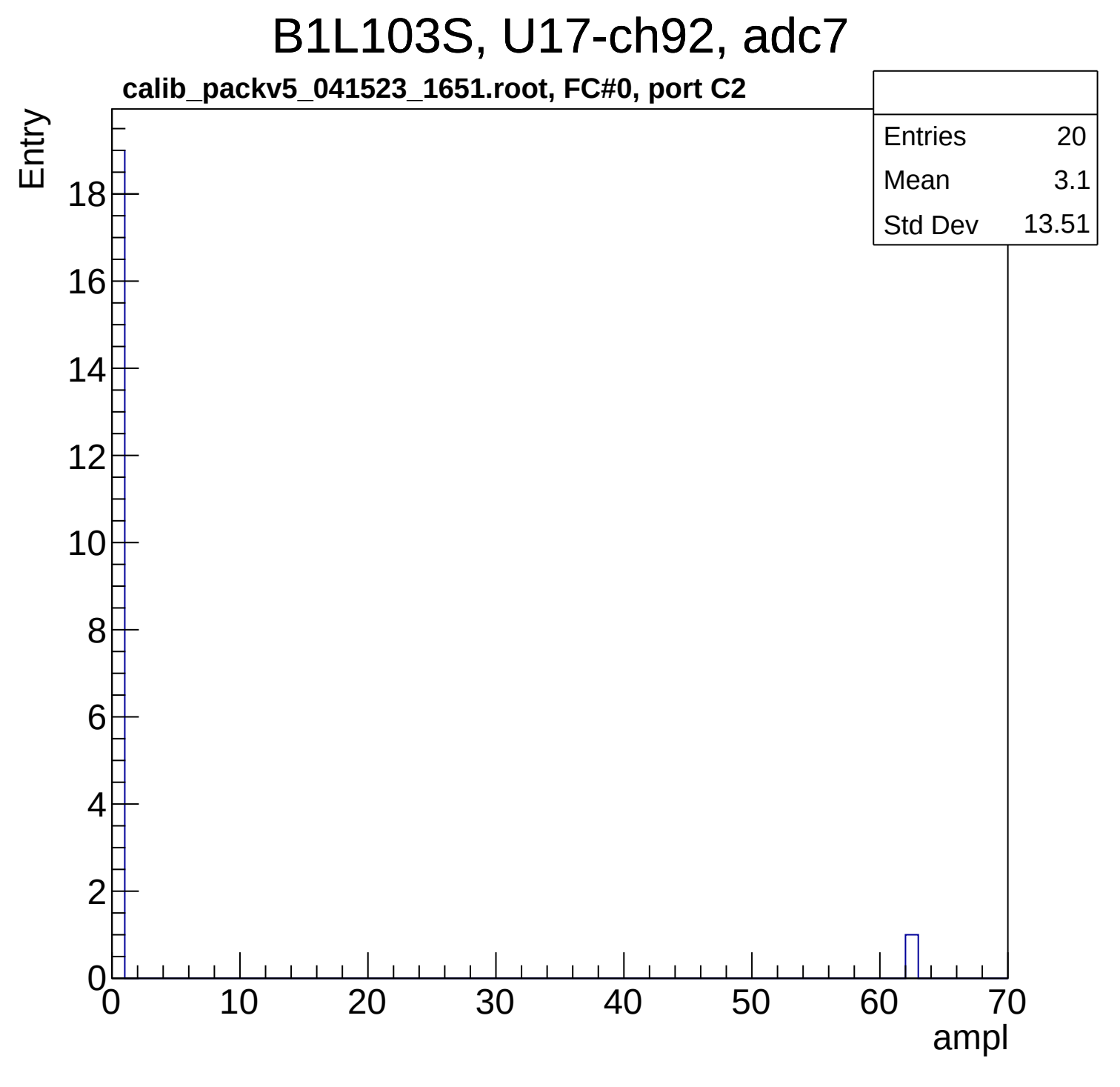
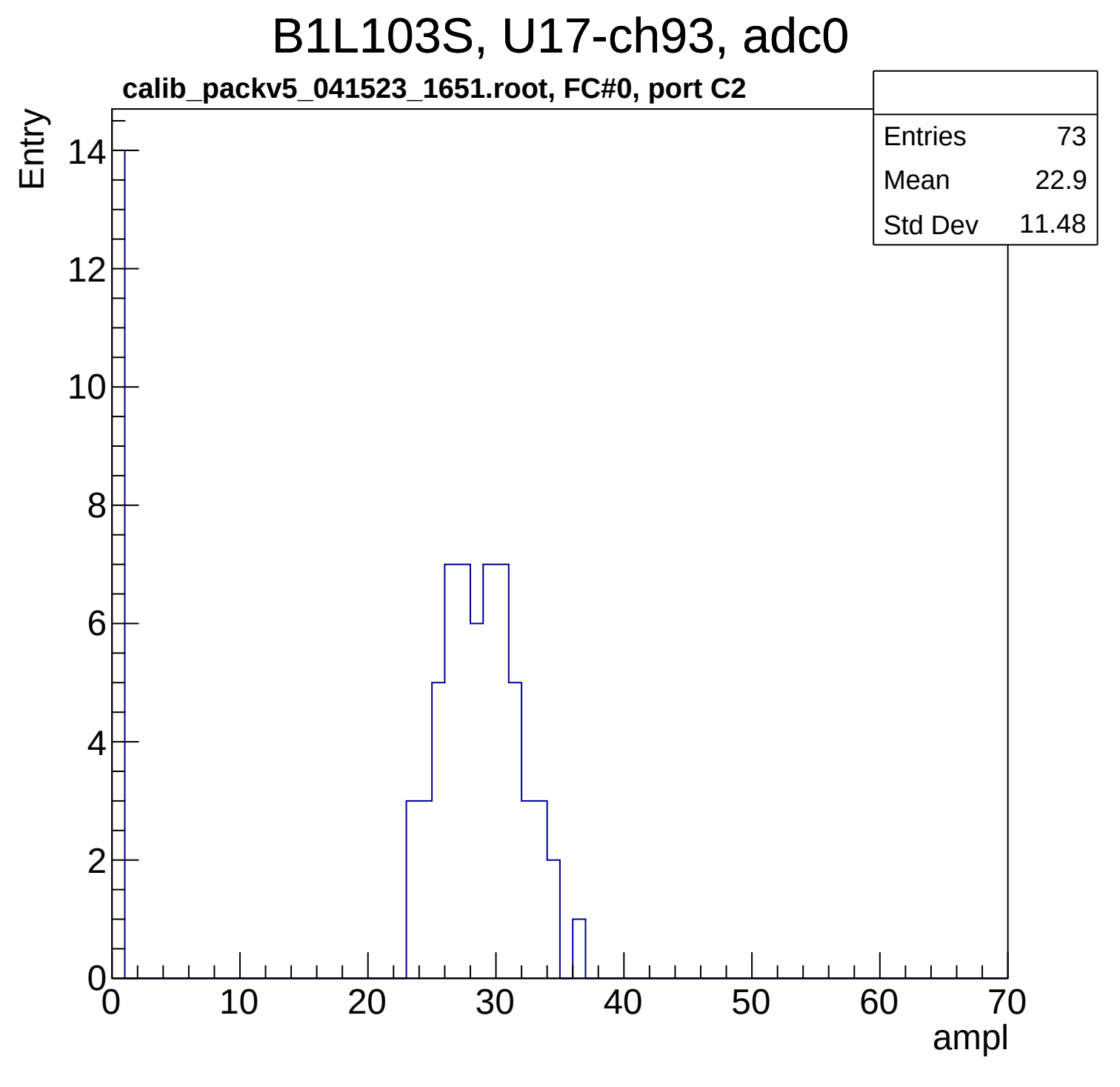
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U17-ch92, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.1
Std Dev 13.51
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch93, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 22.9
Std Dev 11.48
Entry
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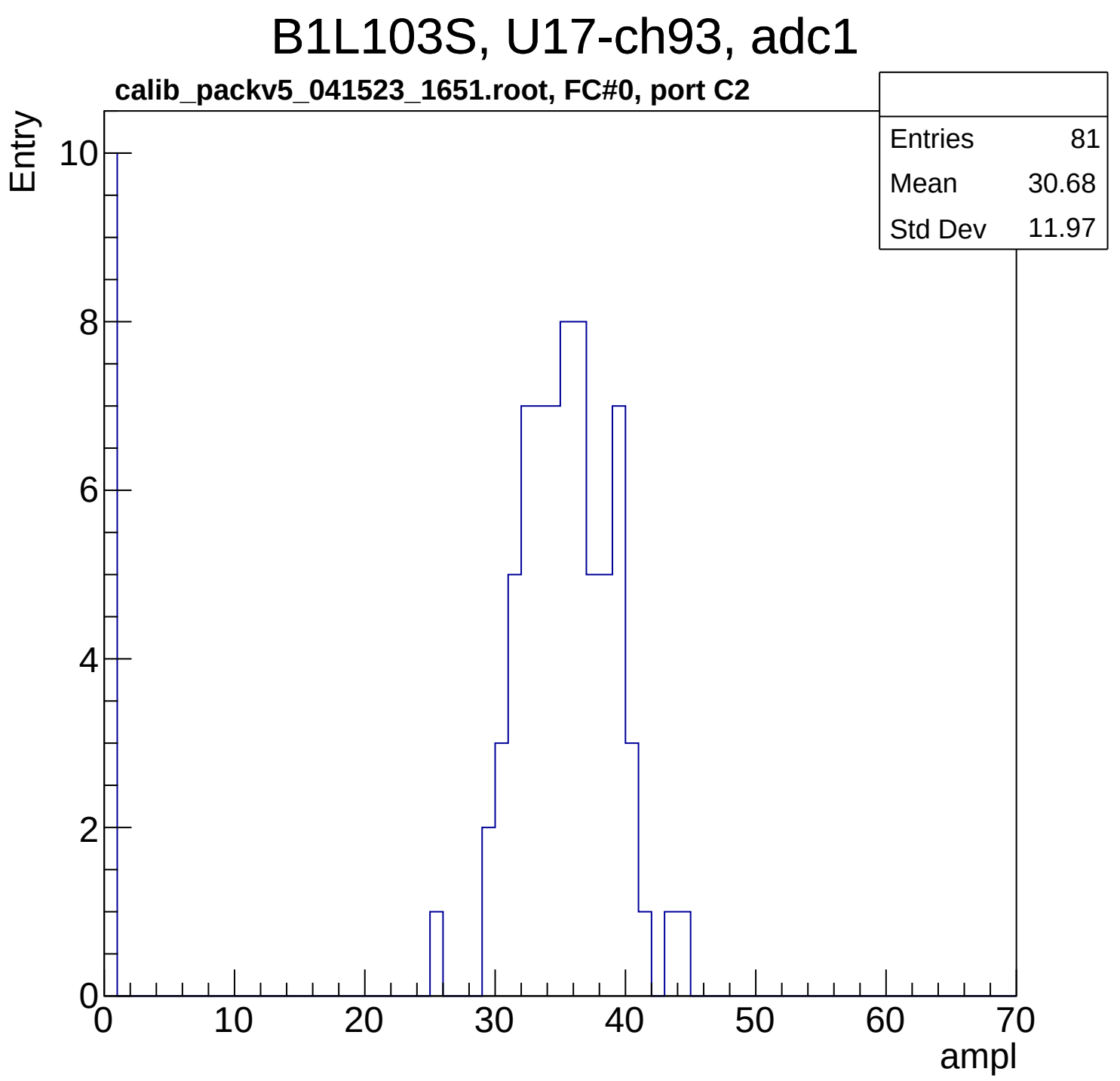
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch93, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 30.68
Std Dev 11.97
Entry
ampl
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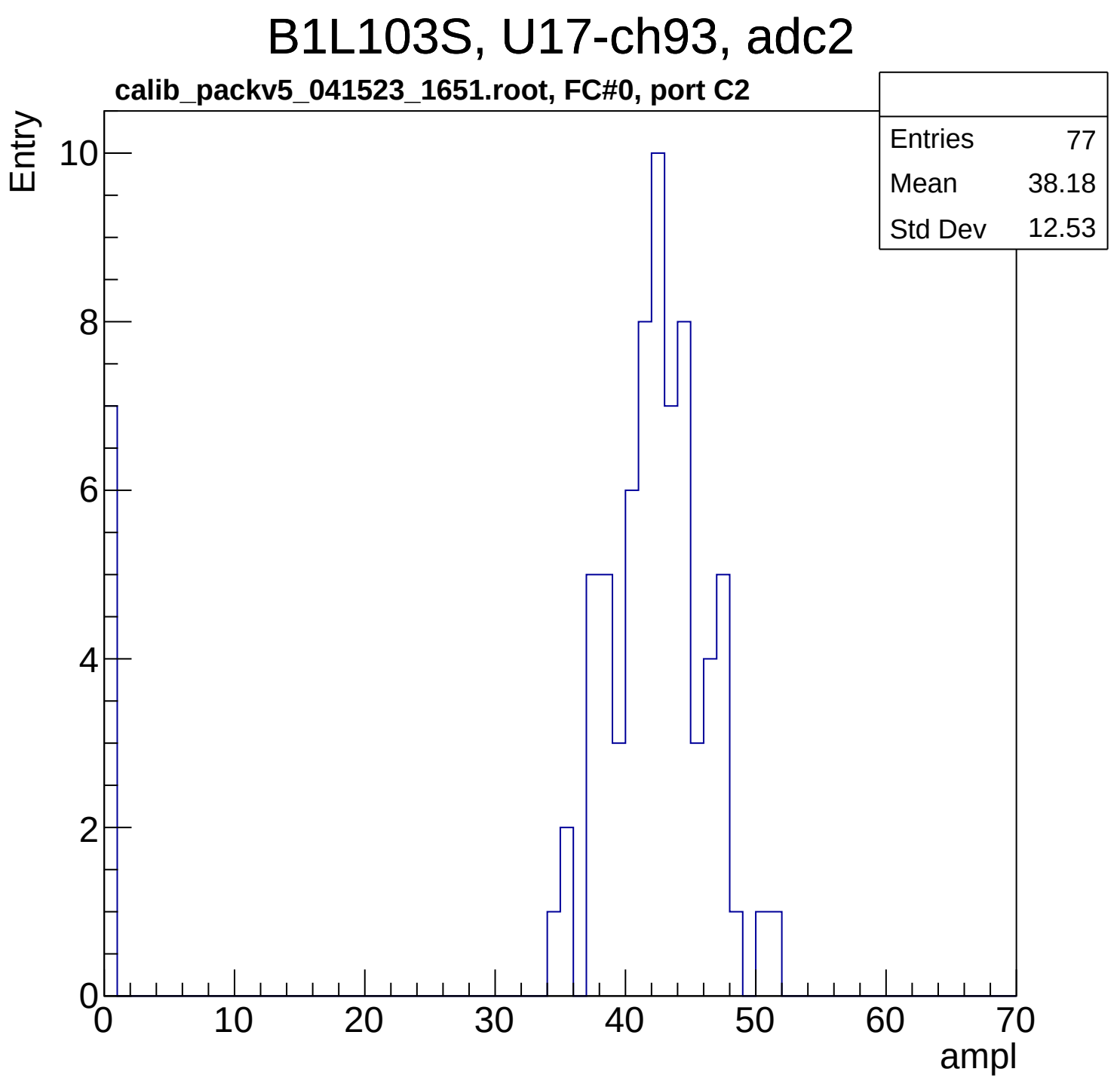
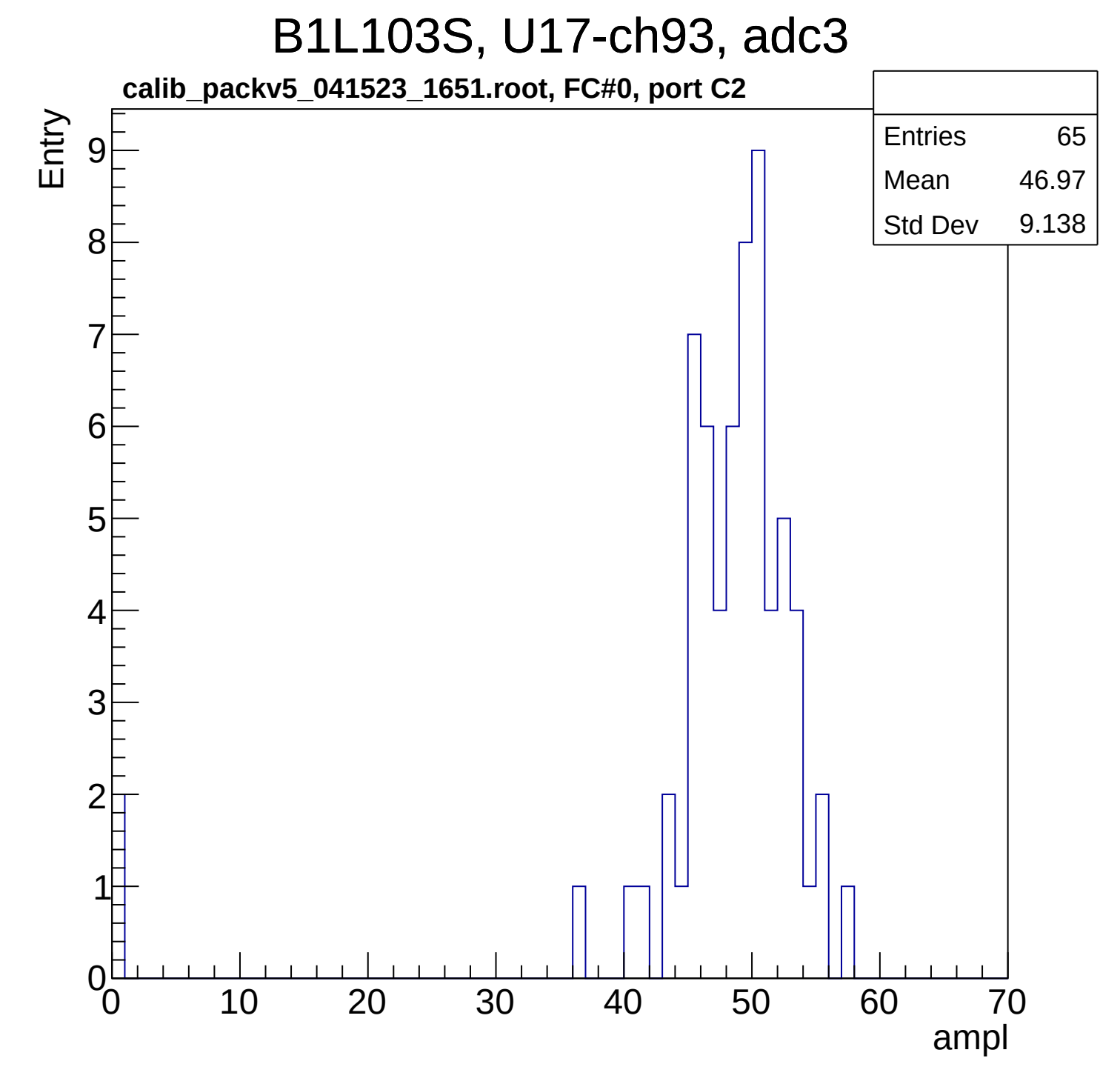
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U17-ch93, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 38.18
Std Dev 12.53
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch93, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 46.97
Std Dev 9.138
Entry
ampl
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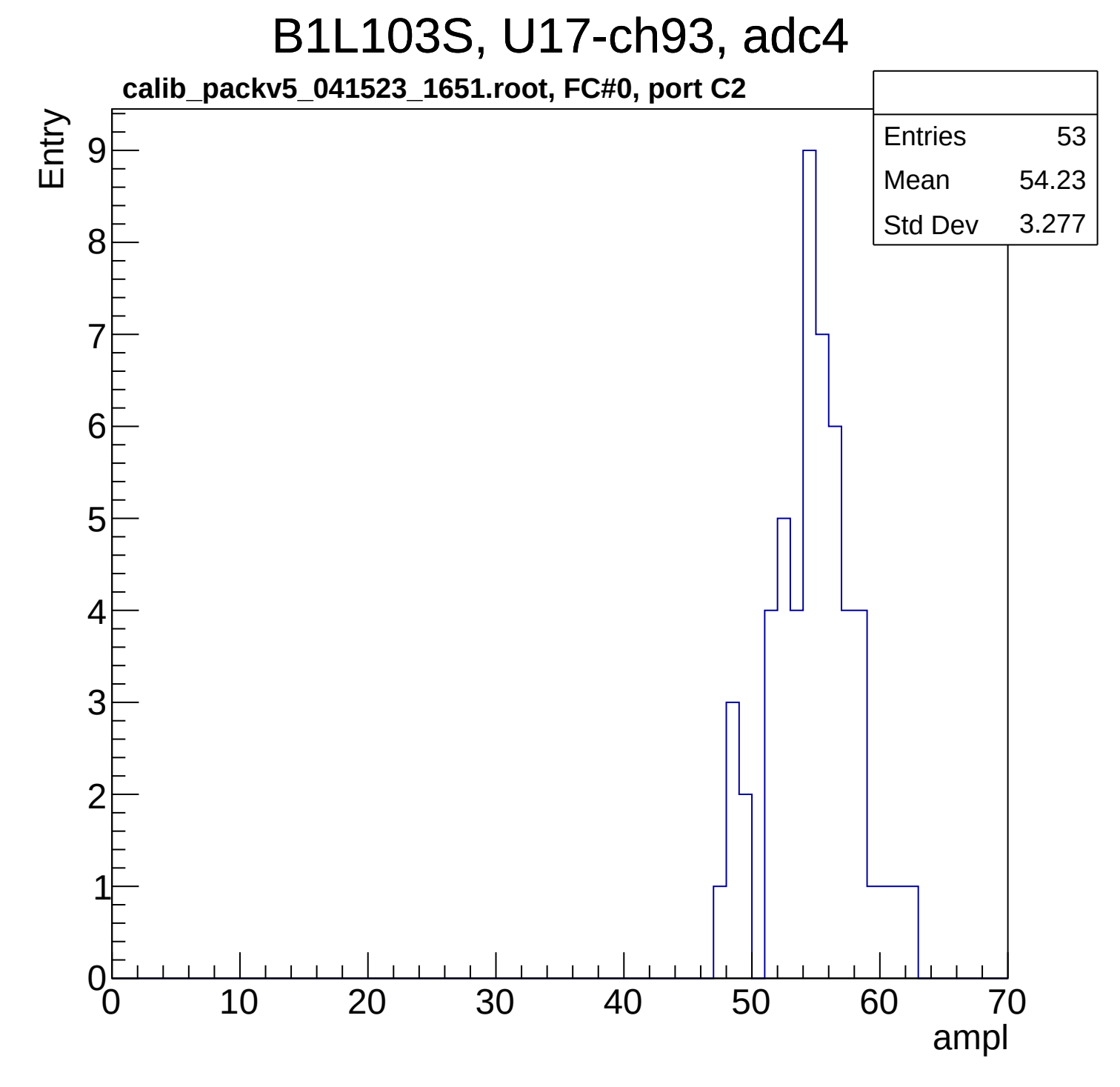
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U17-ch93, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 54.23
Std Dev 3.277
Entry
ampl
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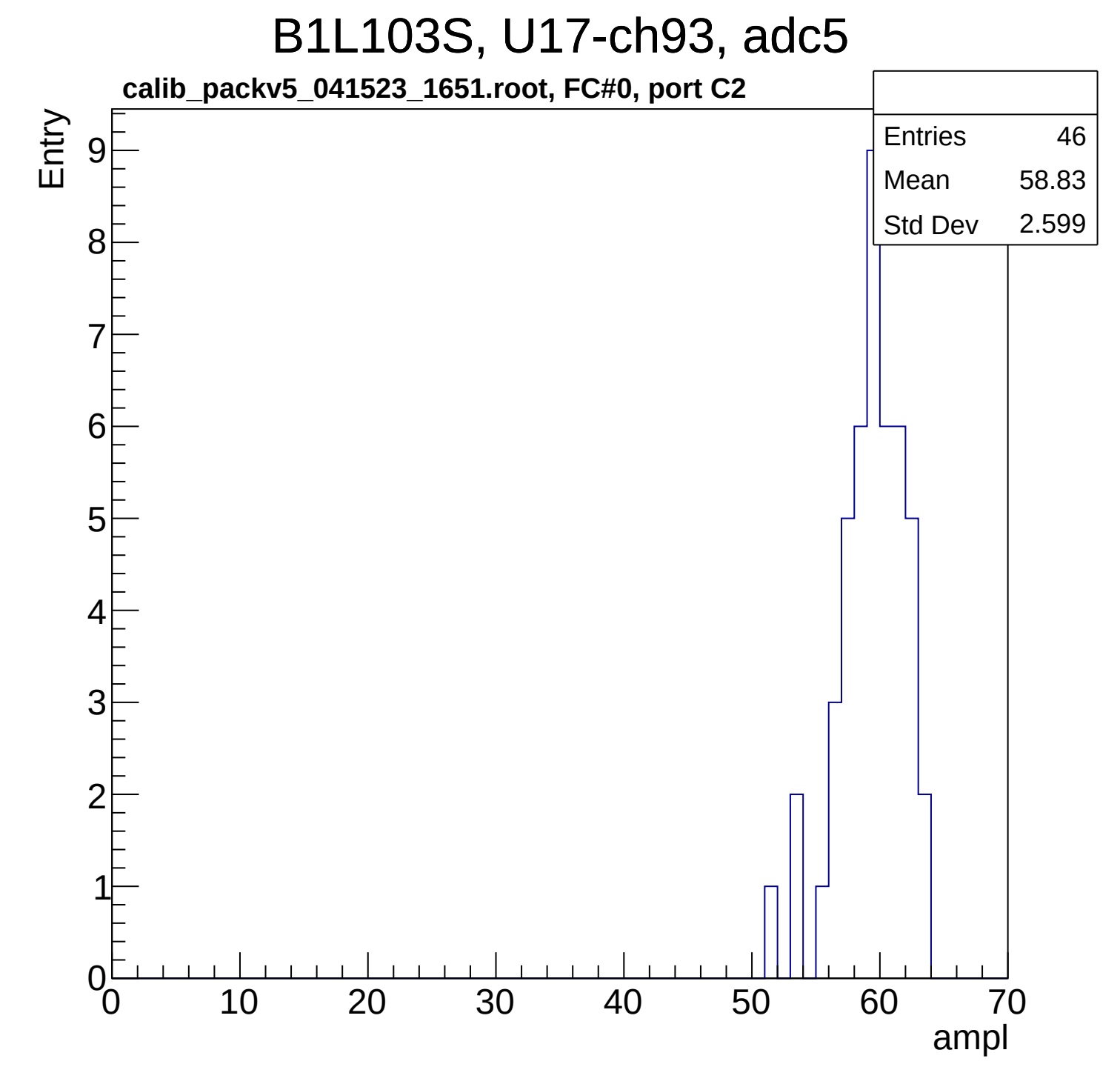
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U17-ch93, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 58.83
Std Dev 2.599
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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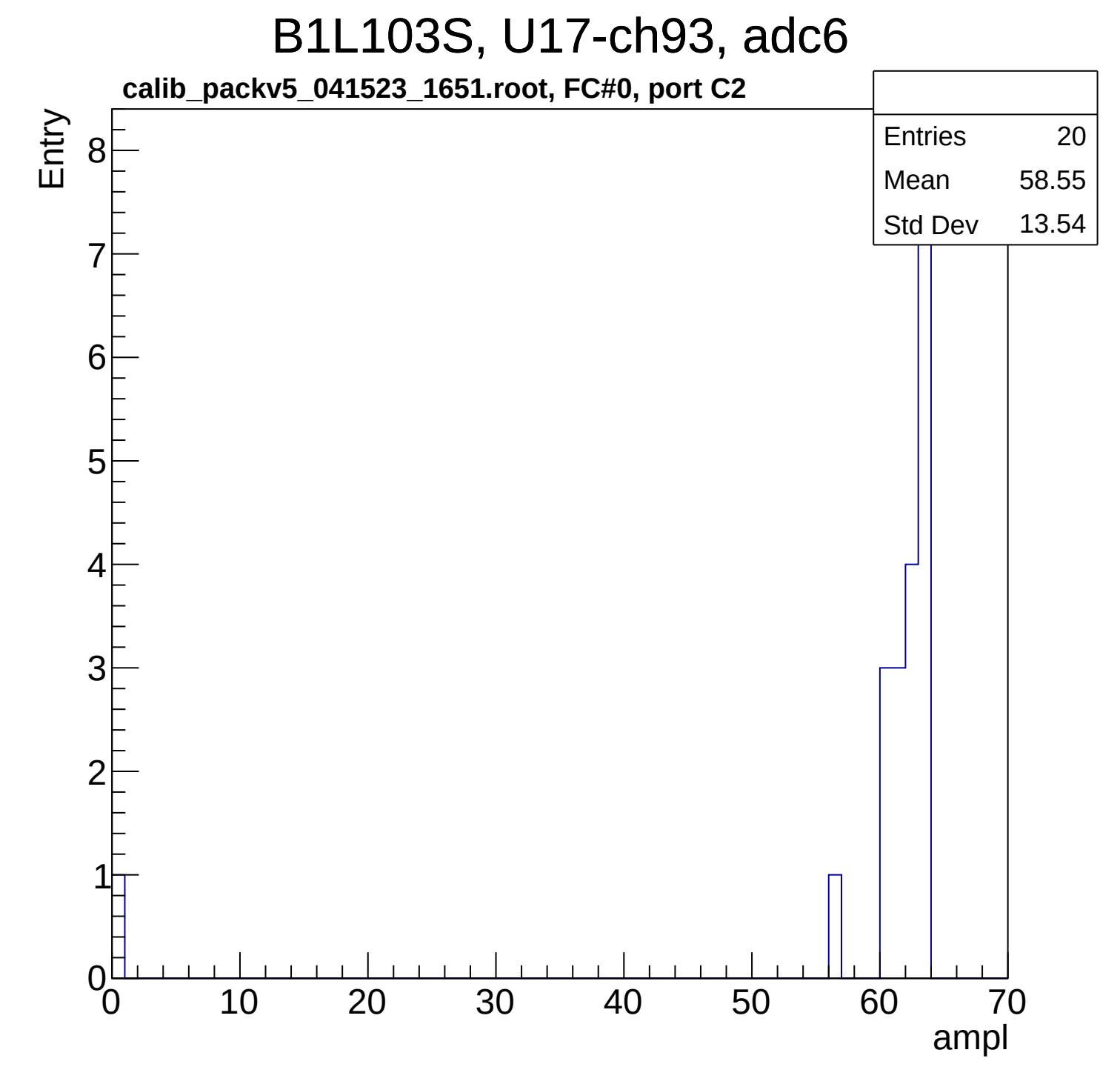
40
50
60
70


B1L103S, U17-ch93, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 58.55
Std Dev 13.54
Entry
ampl
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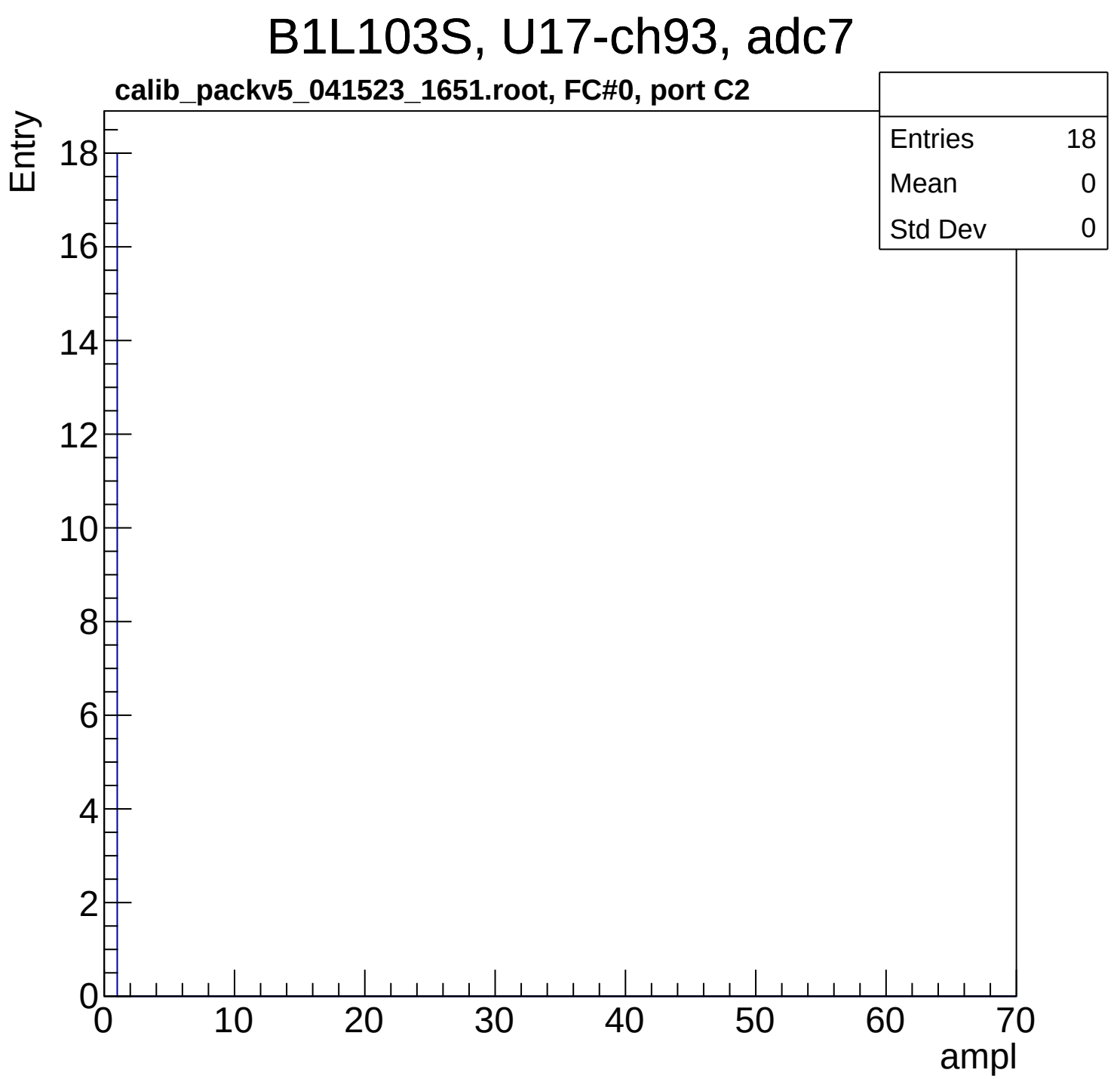
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U17-ch93, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
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2
4
6
8
10
12
14
16
18
0
10
20
30
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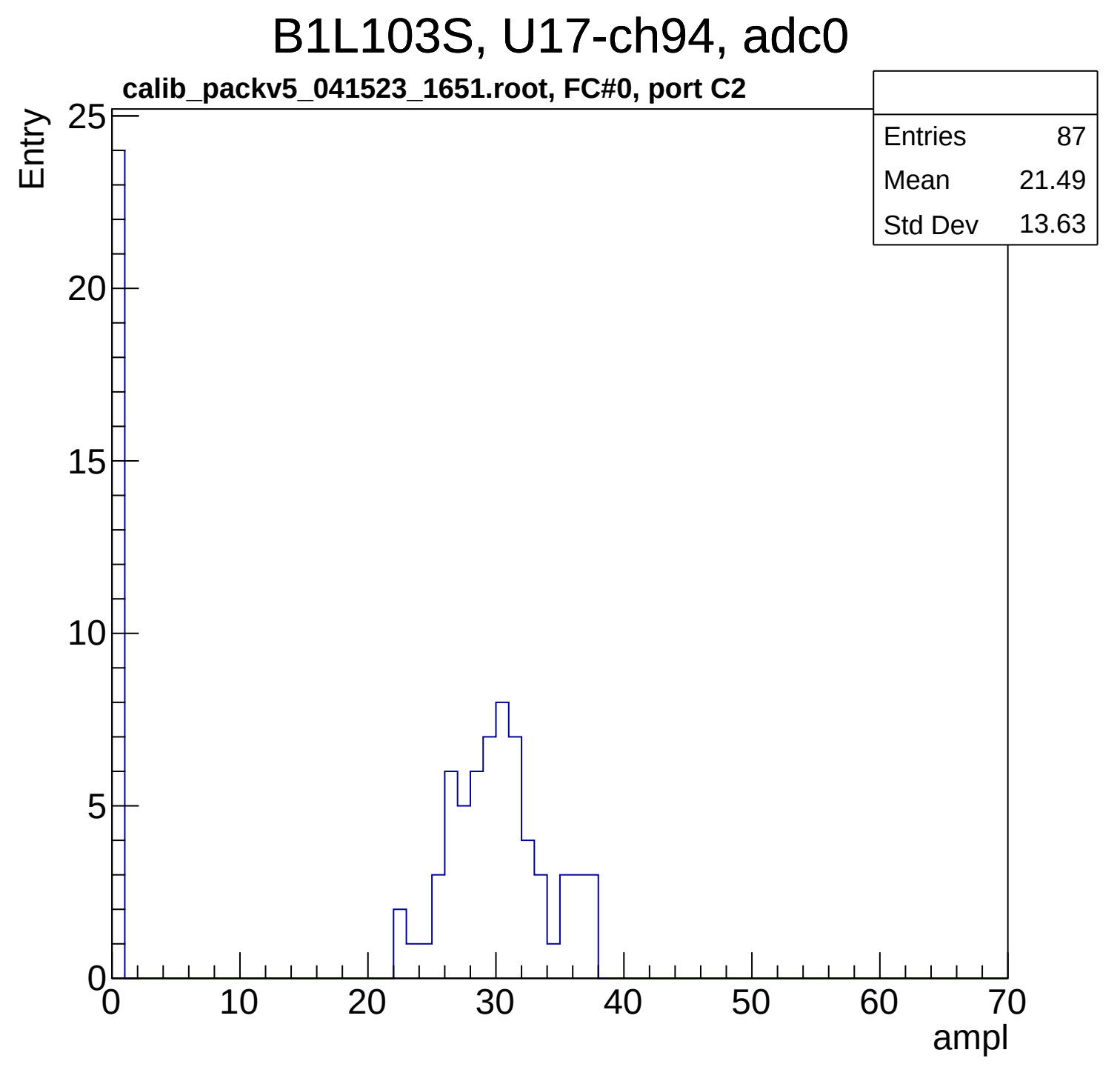
50
60
70
ampl


B1L103S, U17-ch94, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 87
Mean 21.49
Std Dev 13.63
Entry
ampl
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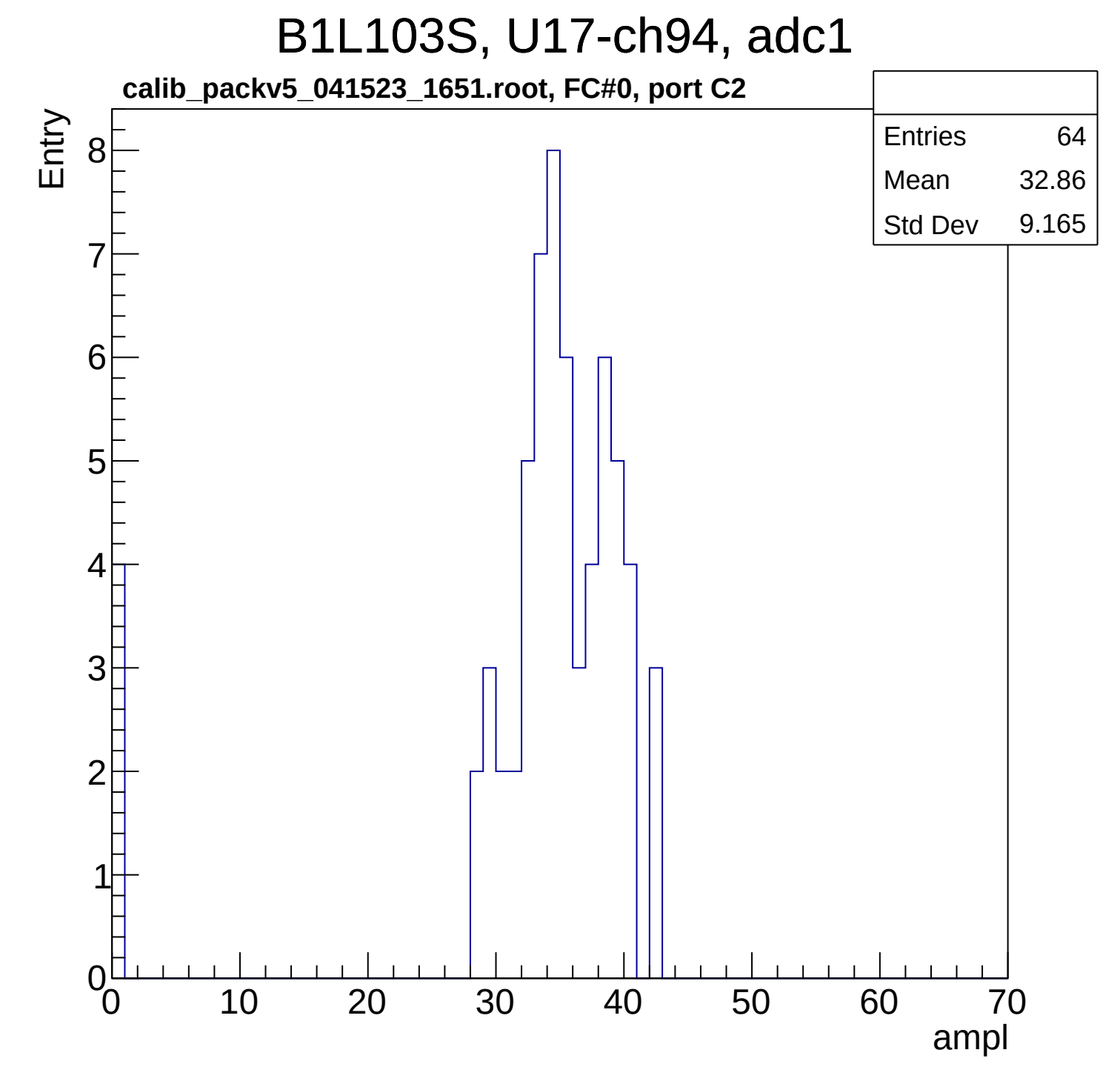
5
10
15
20
25
0
10
20
30
40
50
60
70


B1L103S, U17-ch94, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 32.86
Std Dev 9.165
Entry
ampl
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2
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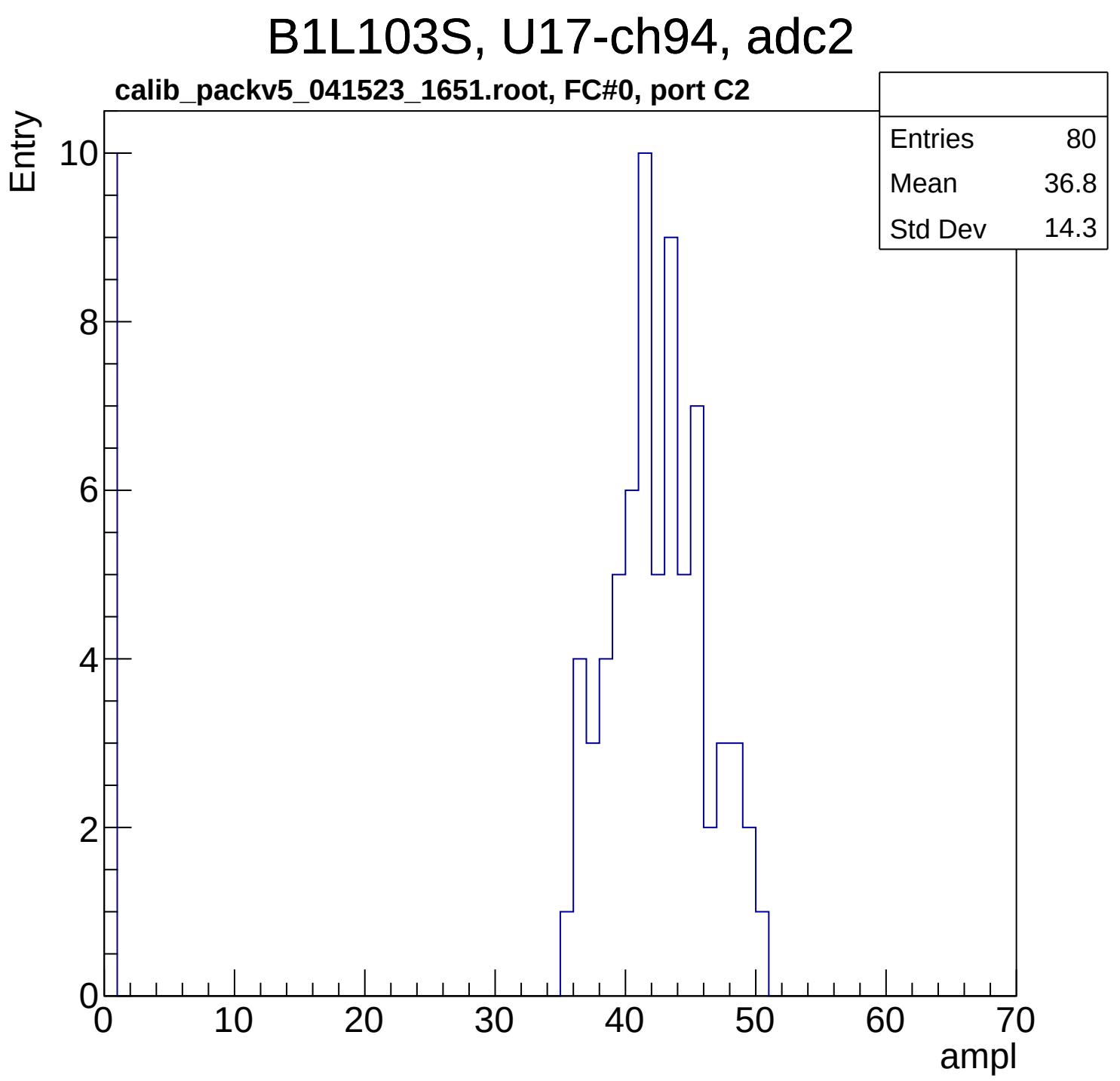
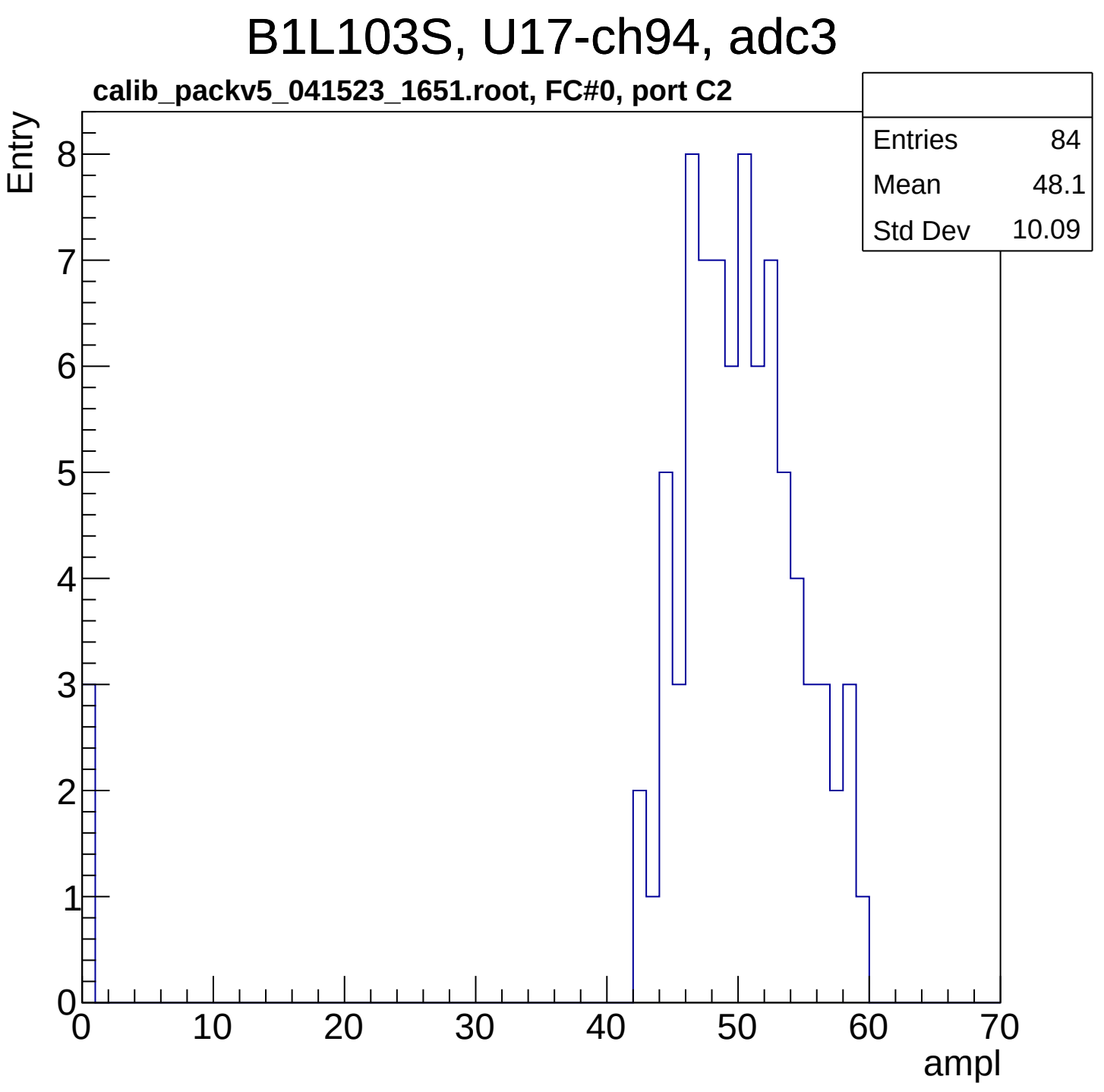
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U17-ch94, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 36.8
Std Dev 14.3
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U17-ch94, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 48.1
Std Dev 10.09
Entry
ampl
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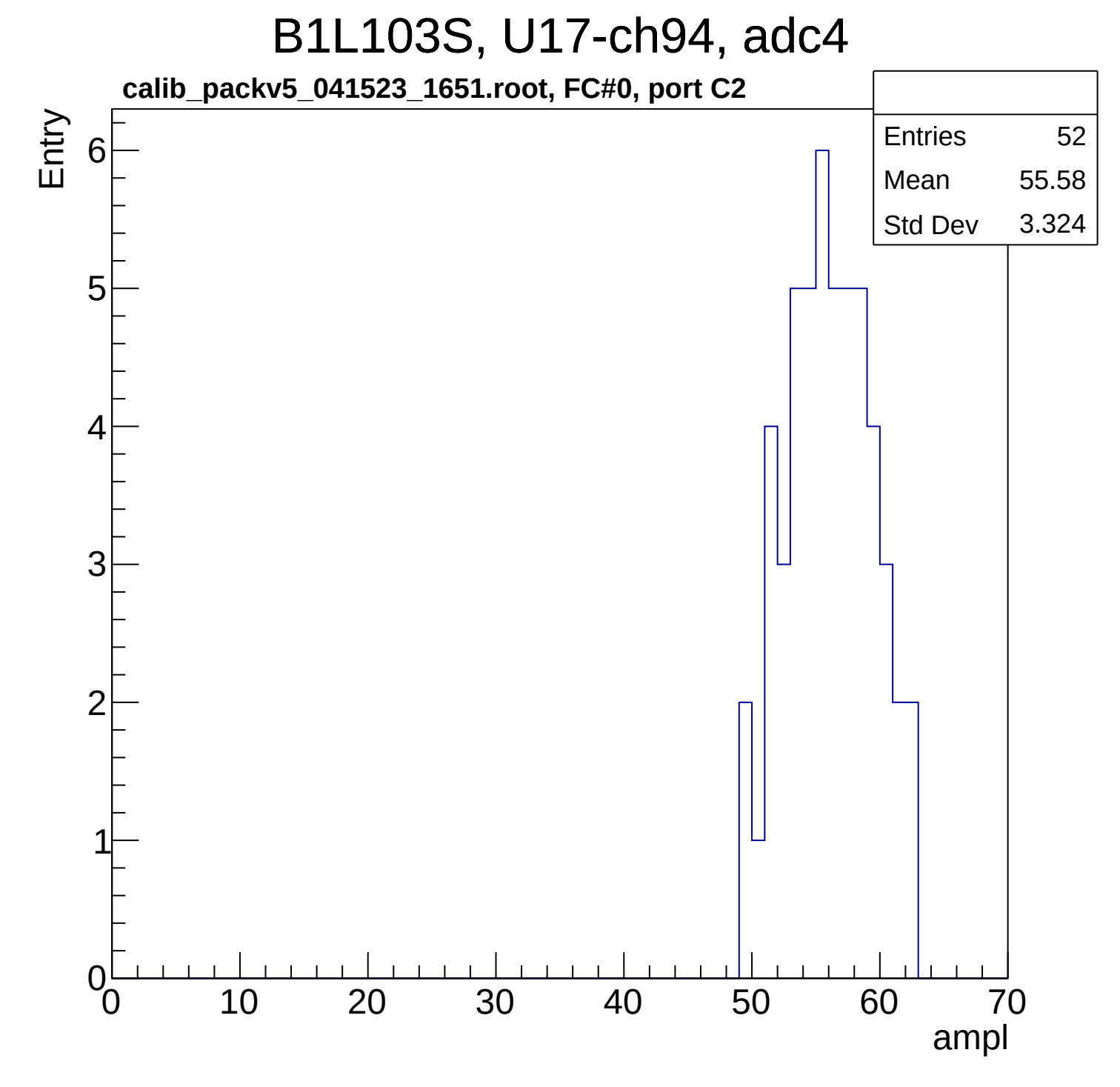
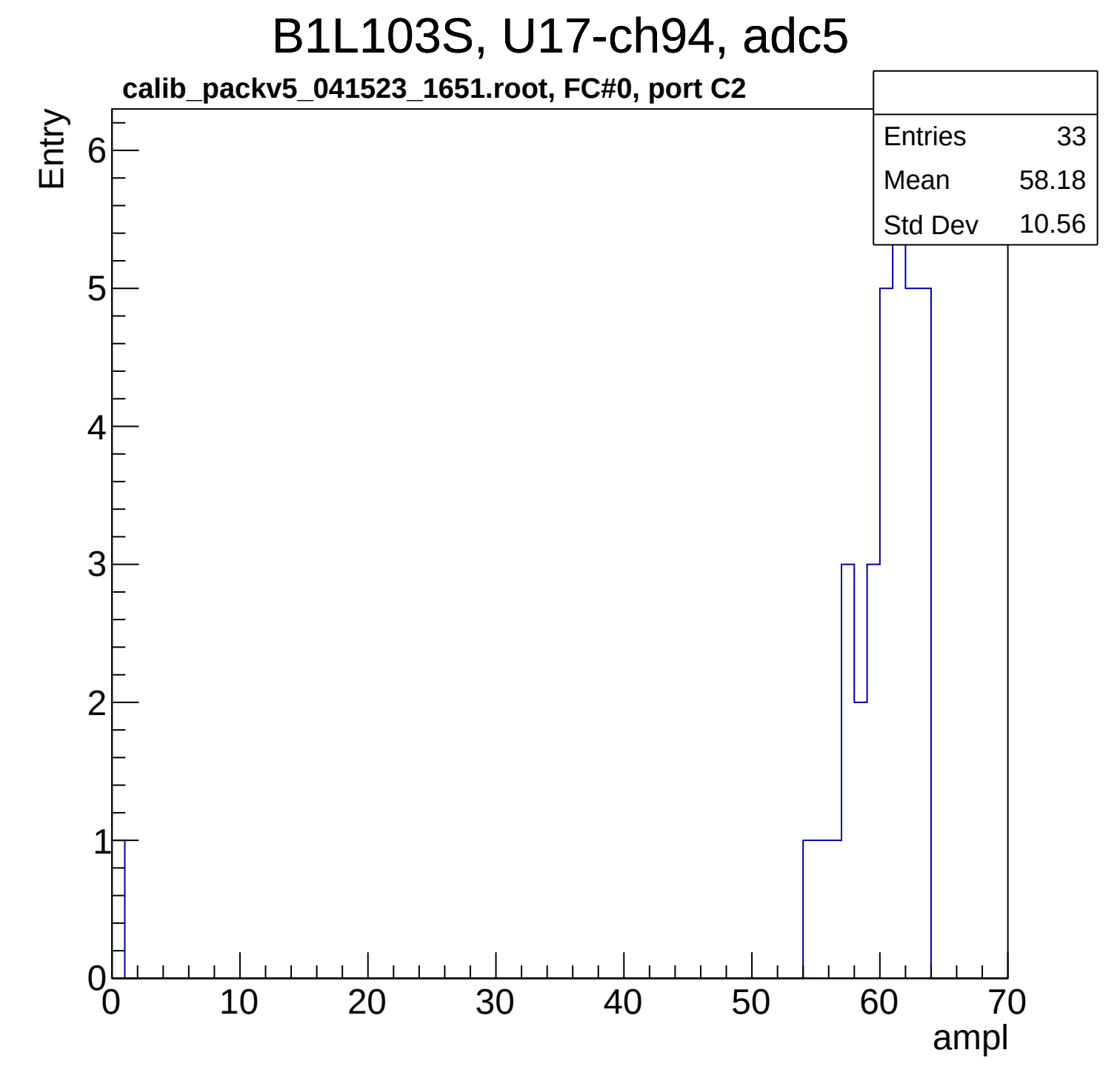
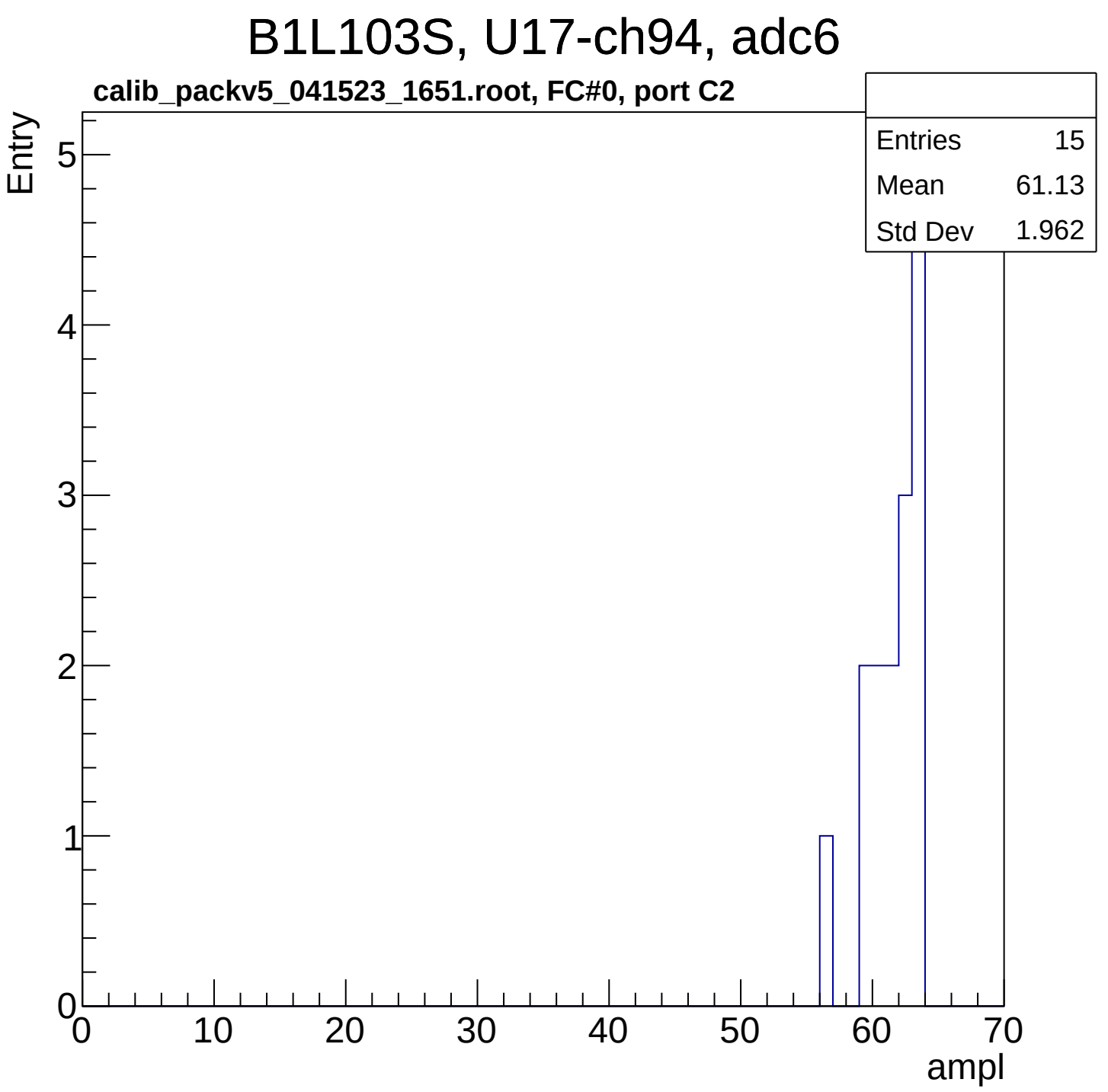
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U17-ch94, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 55.58
Std Dev 3.324
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U17-ch94, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 33
Mean 58.18
Std Dev 10.56
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U17-ch94, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 15
Mean 61.13
Std Dev 1.962
Entry
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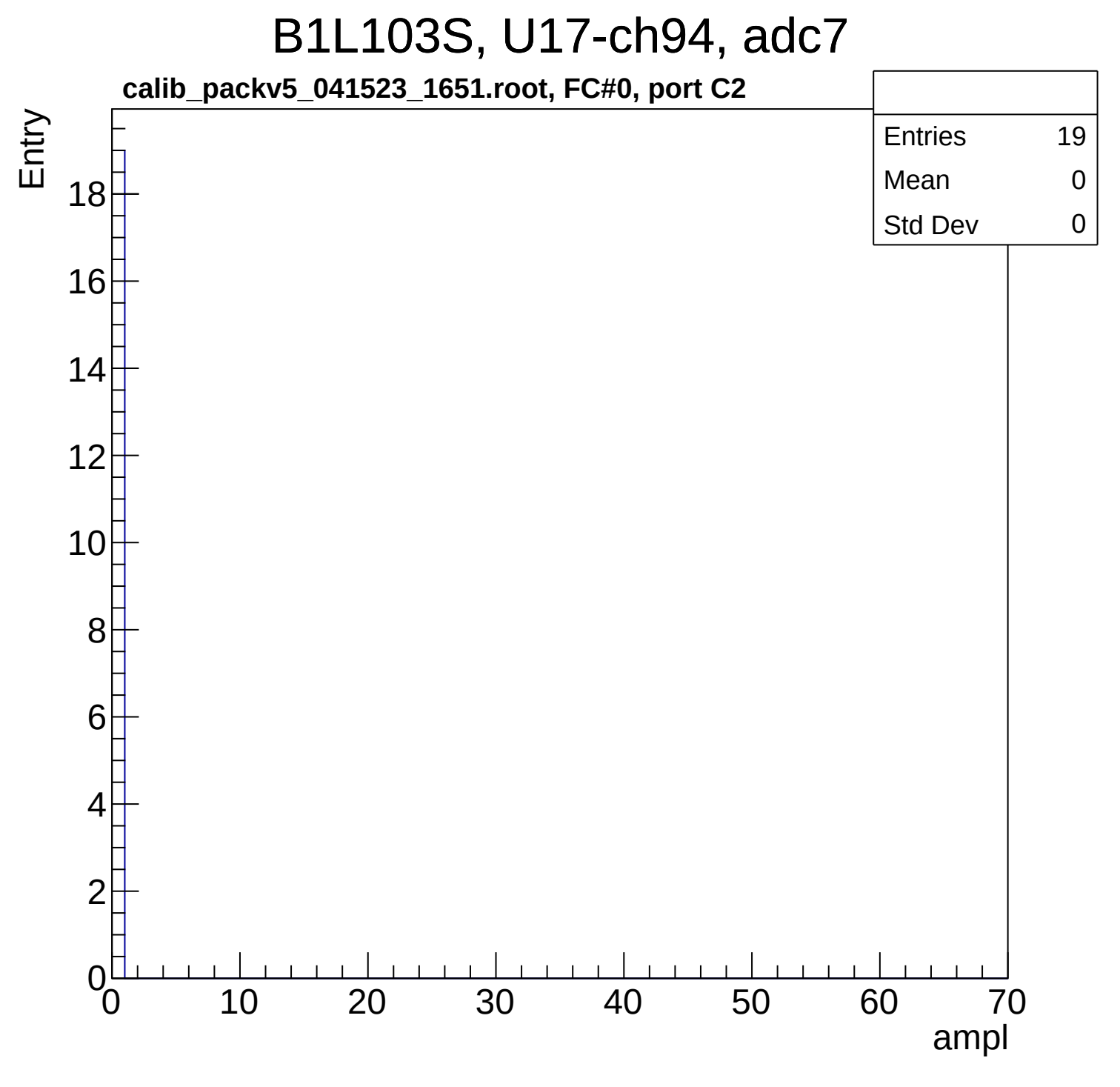
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch94, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
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10
20
30
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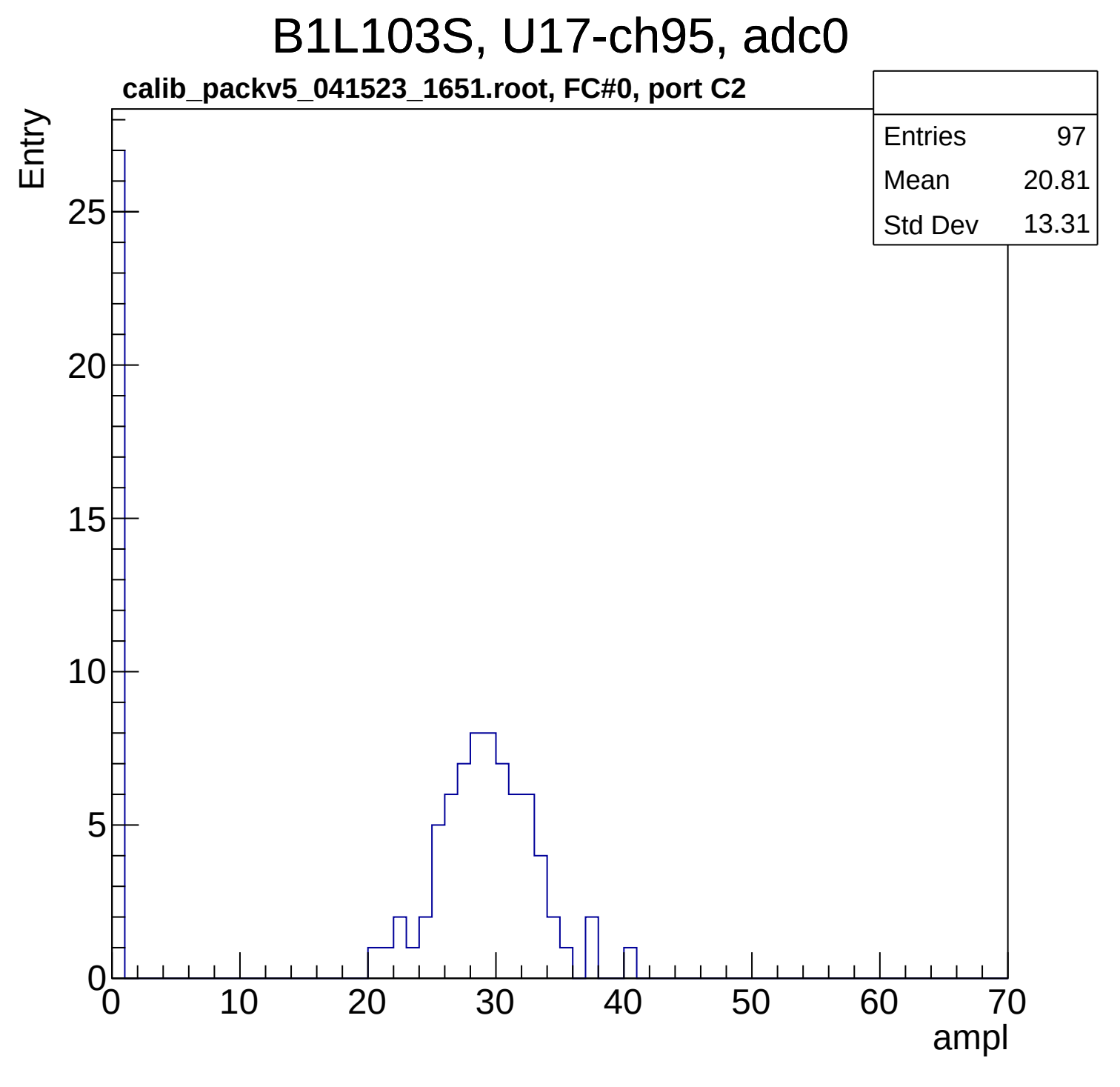
50
60
70
ampl


B1L103S, U17-ch95, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 97
Mean 20.81
Std Dev 13.31
Entry
0
5
10
15
20
25
0
10
20
30
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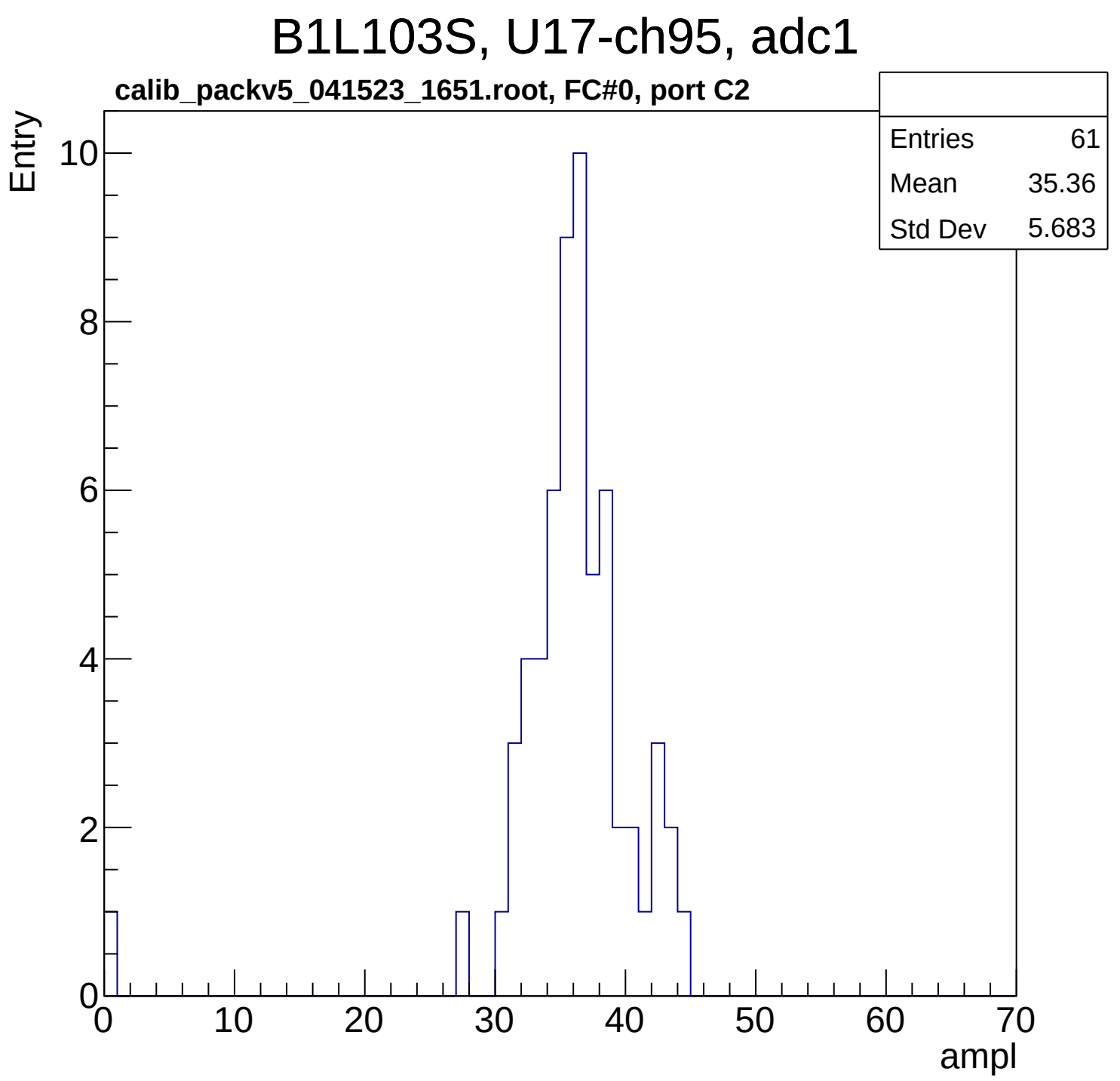
50
60
70
ampl


B1L103S, U17-ch95, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 35.36
Std Dev 5.683
Entry
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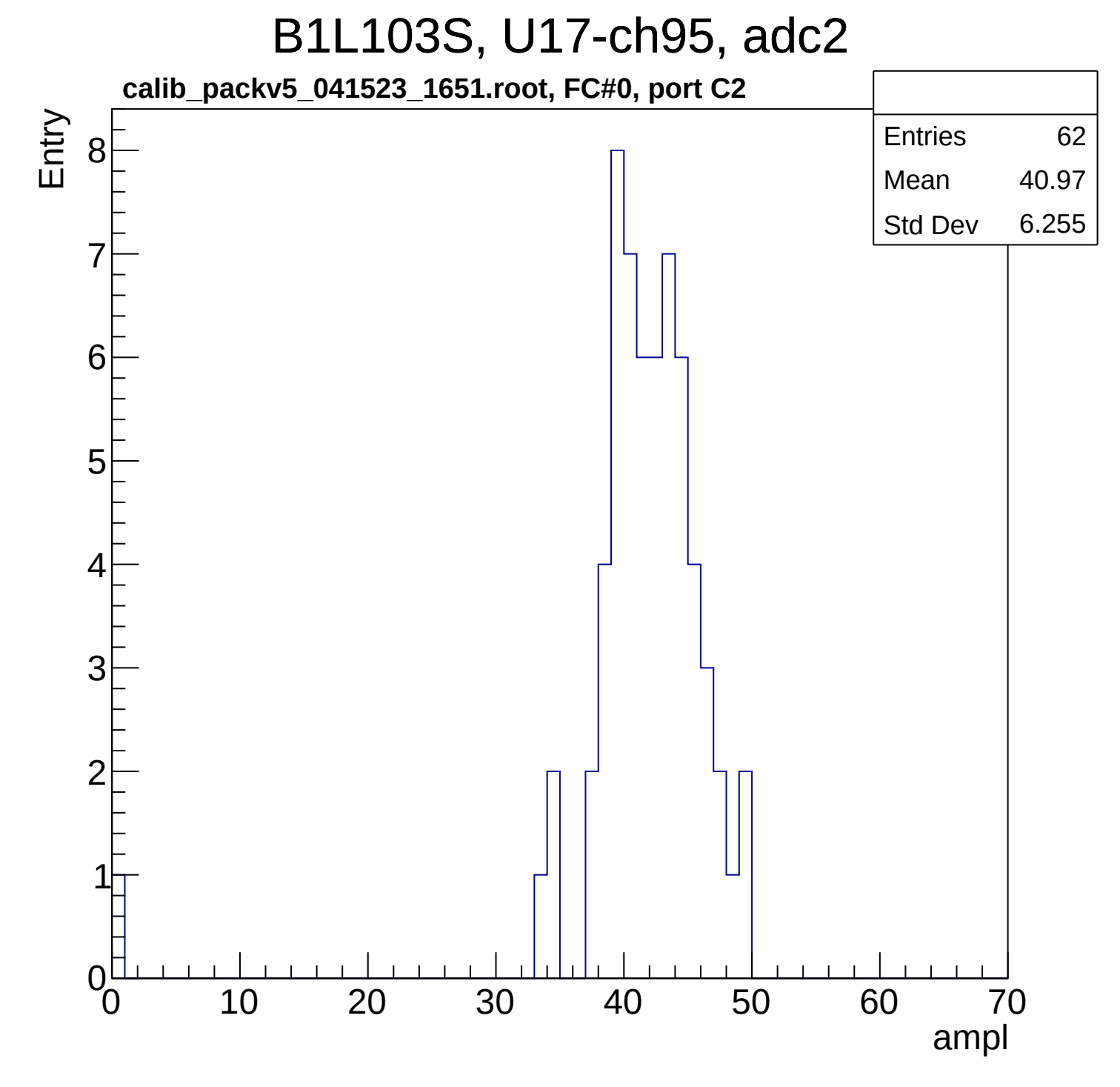
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch95, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 40.97
Std Dev 6.255
Entry
ampl
0
1
2
3
4
5
6
7
8
0
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40
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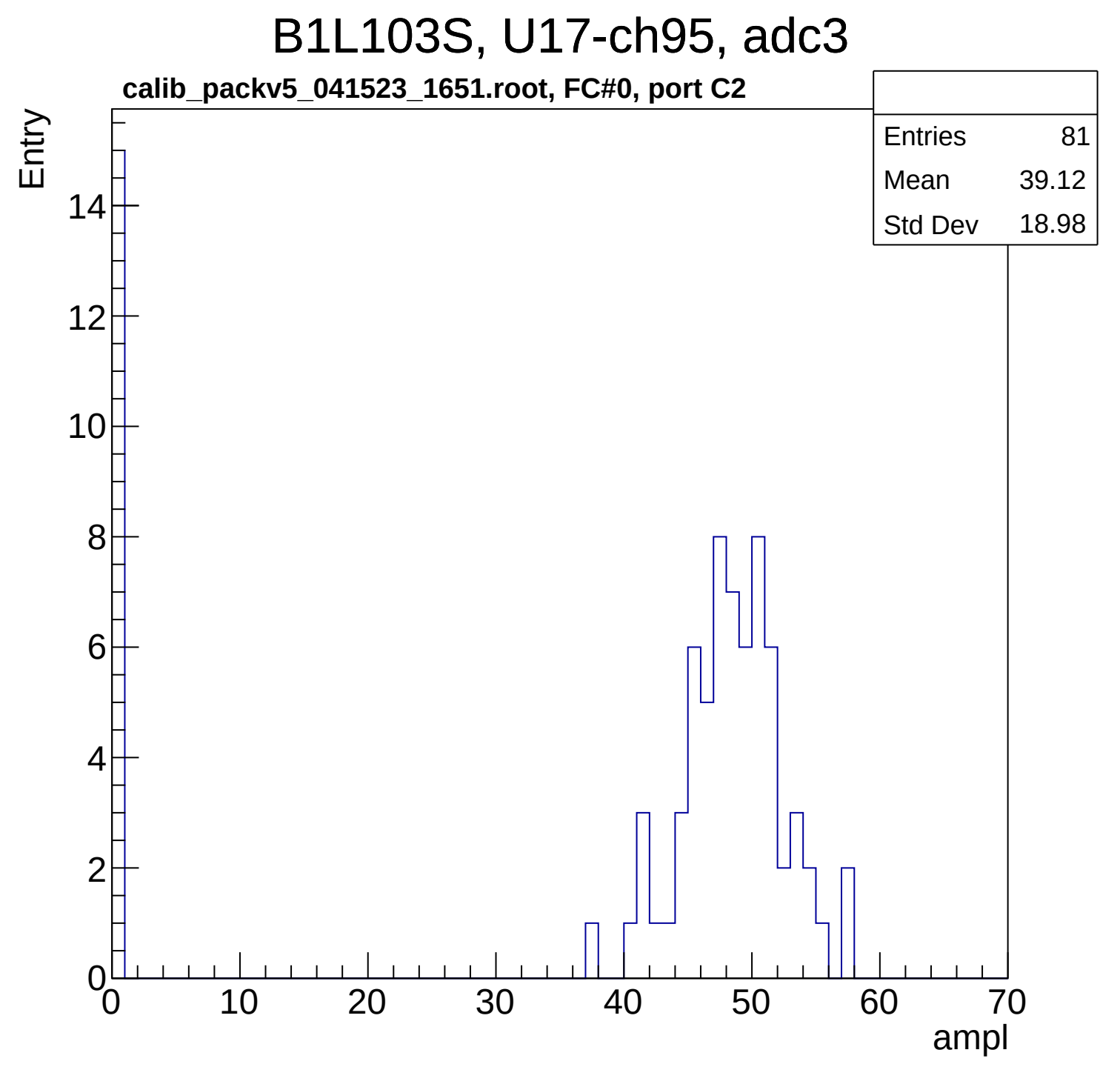
60
70


B1L103S, U17-ch95, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 39.12
Std Dev 18.98
Entry
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2
4
6
8
10
12
14
0
10
20
30
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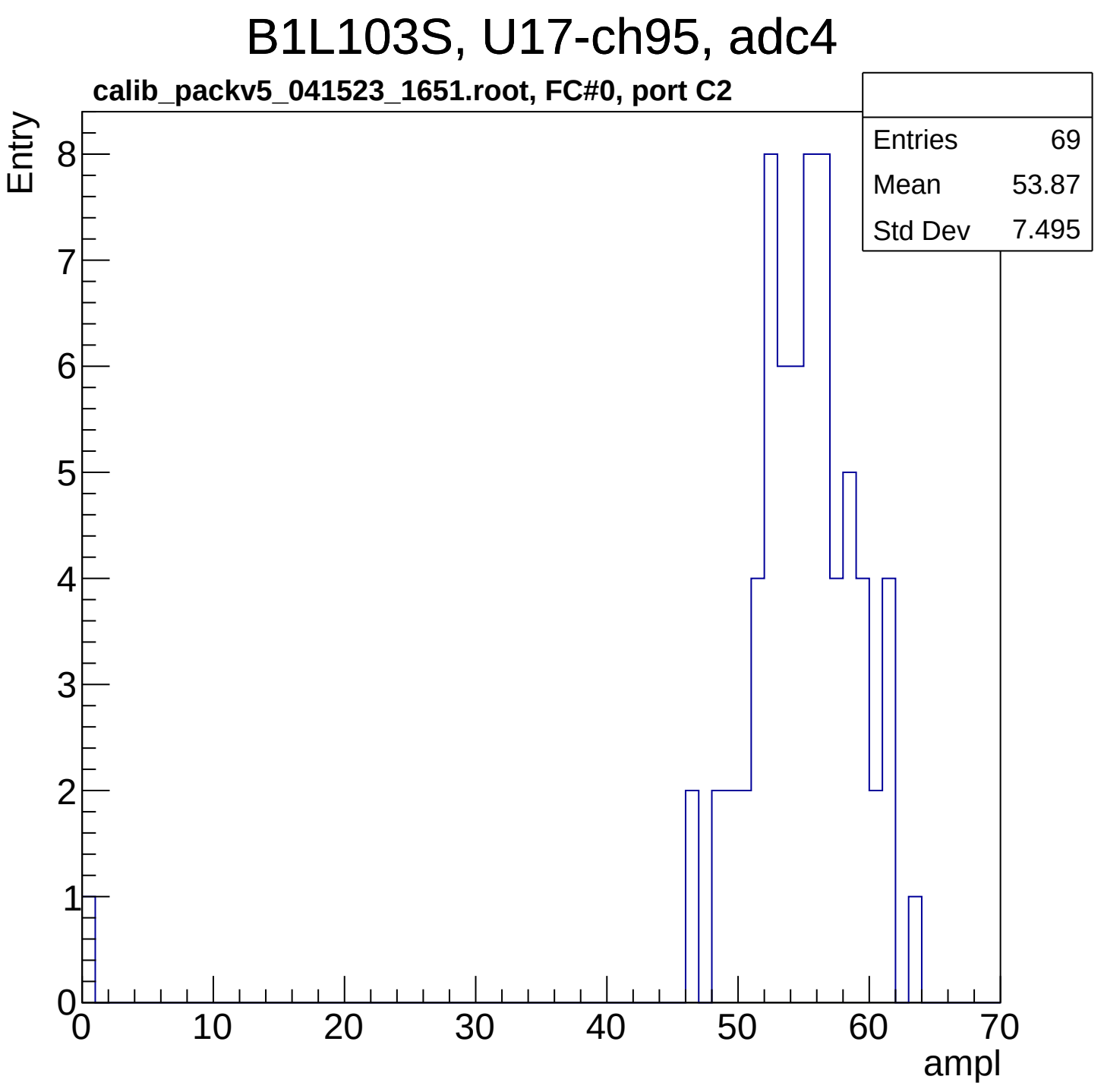
50
60
70
ampl


B1L103S, U17-ch95, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 53.87
Std Dev 7.495
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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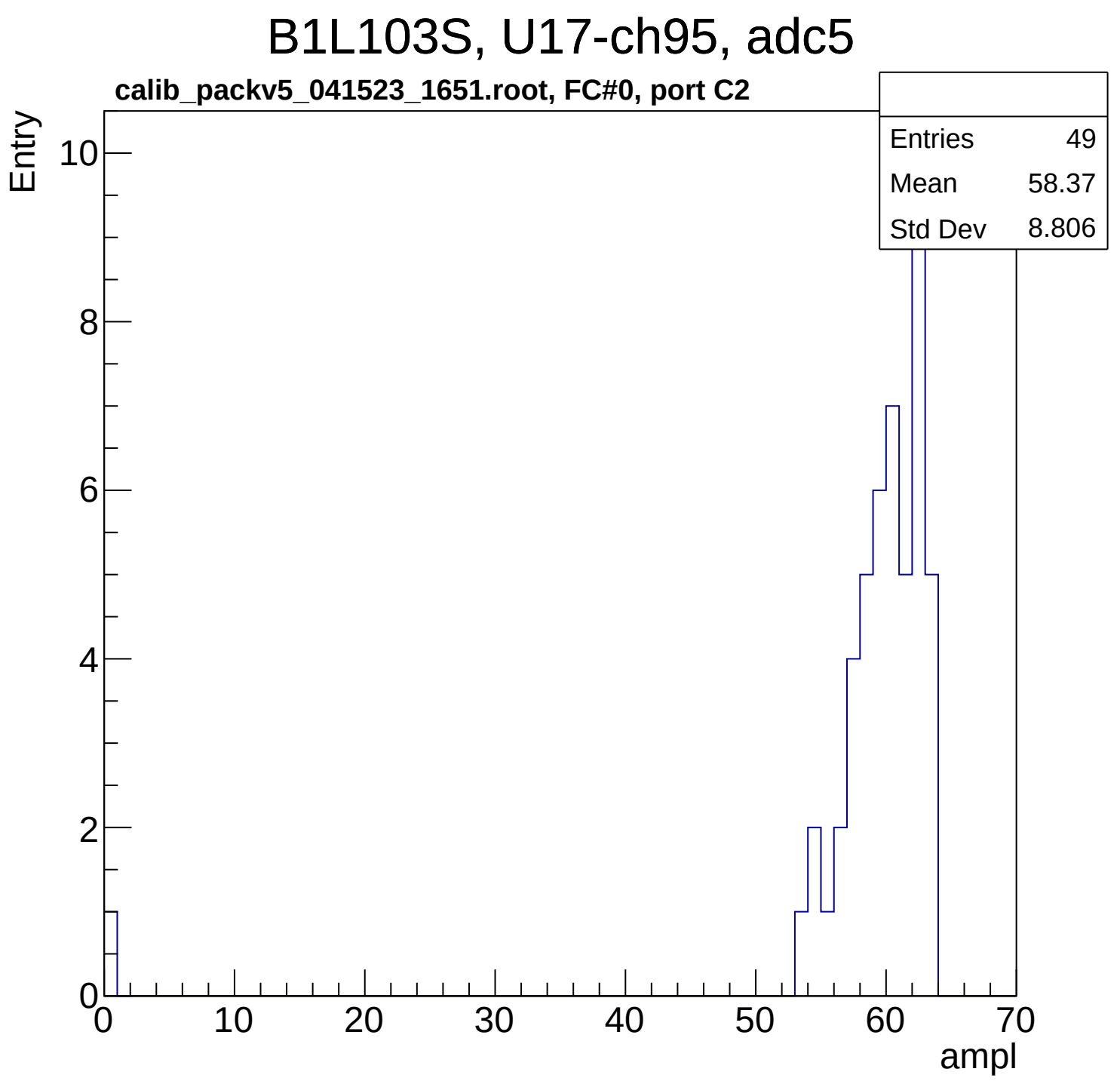
40
50
60
70


B1L103S, U17-ch95, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 58.37
Std Dev 8.806
Entry
ampl
0
2
4
6
8
10
0
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20
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40
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60
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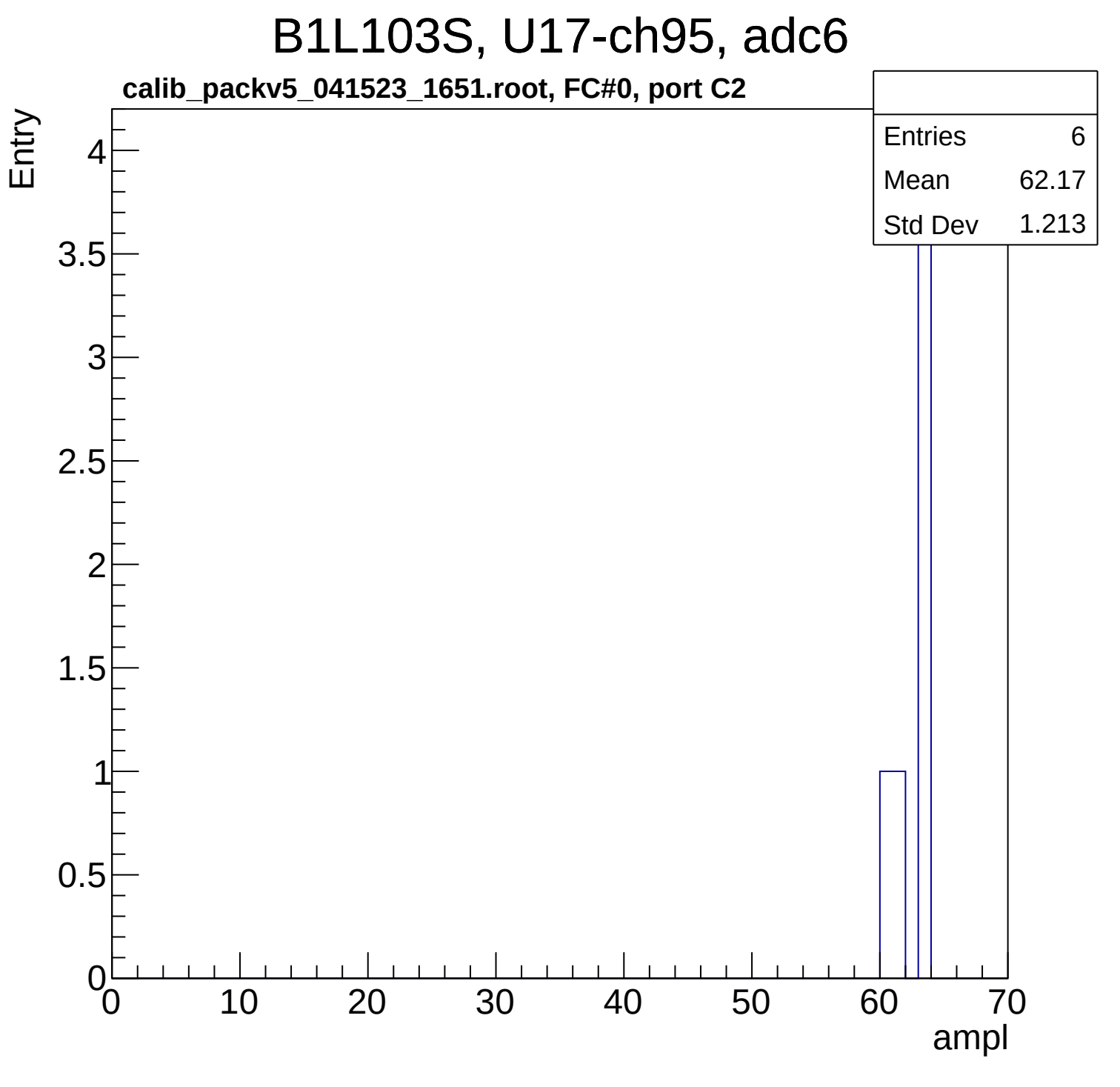
B1L103S, U17-ch95, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 62.17
Std Dev 1.213
Entry
ampl
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1.5
2
2.5
3
3.5
4
0
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20
30
40
50
60
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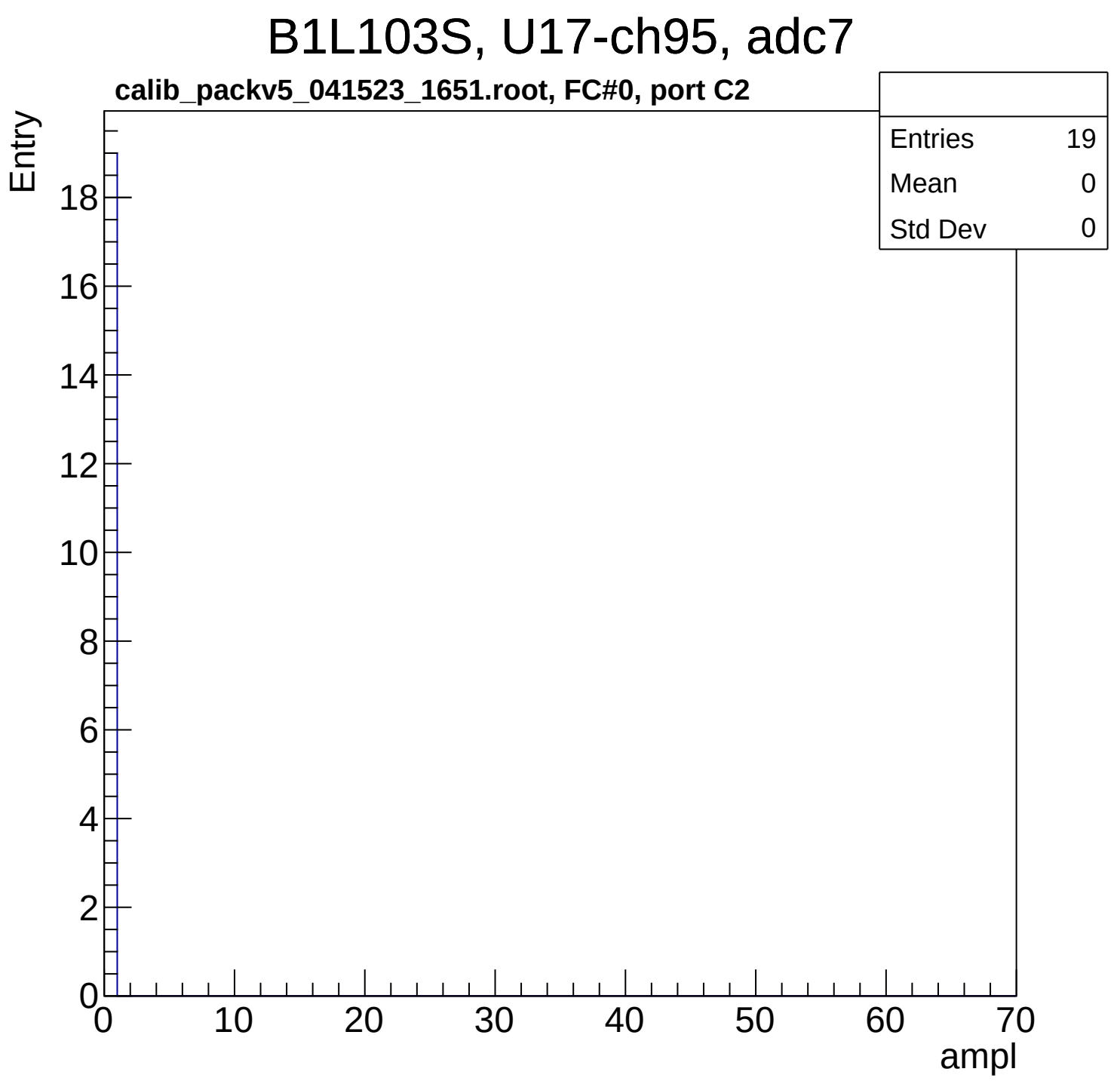
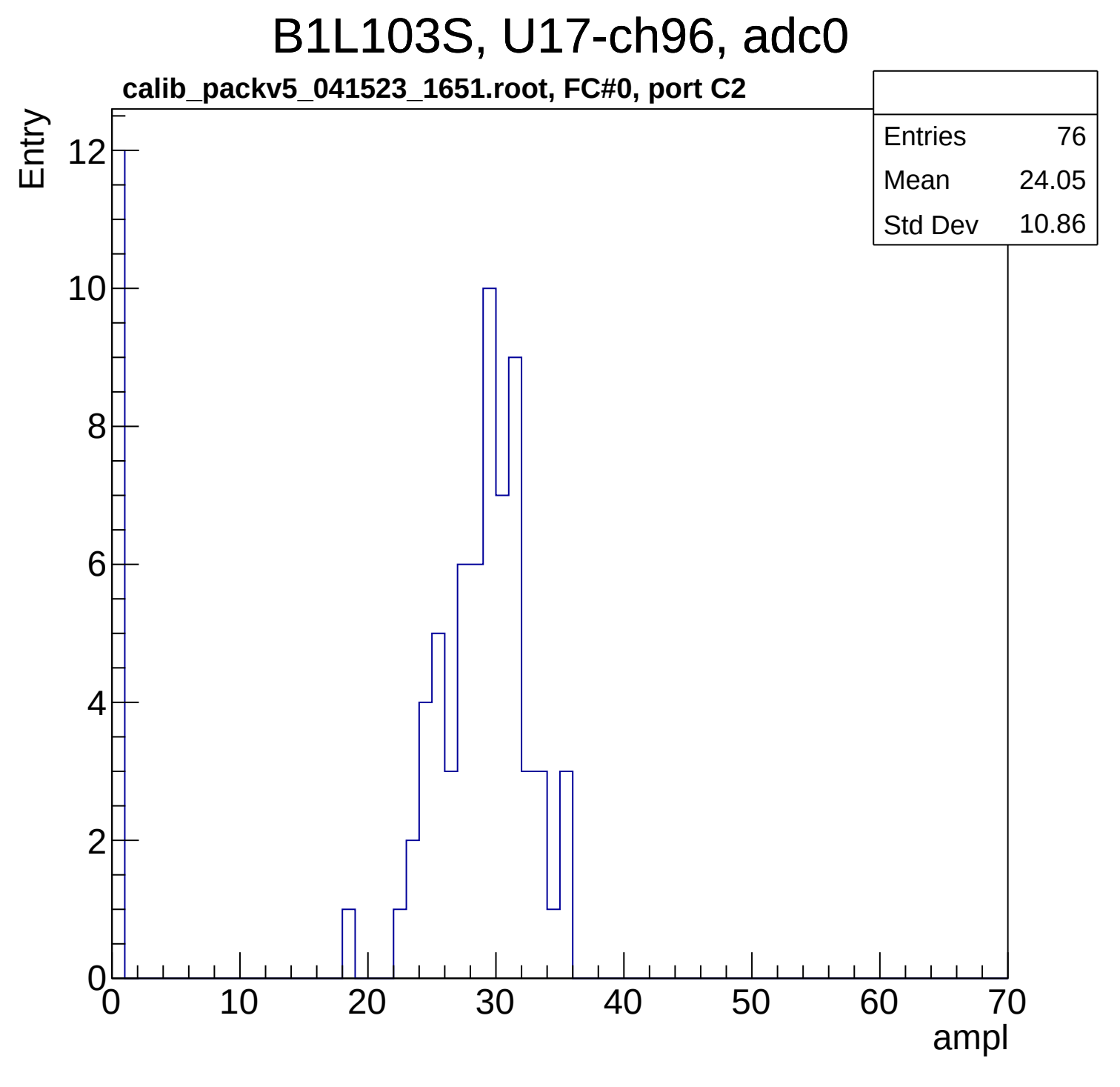

B1L103S, U17-ch95, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch96, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 24.05
Std Dev 10.86
Entry
ampl
0
2
4
6
8
10
12
0
10
20
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40
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60
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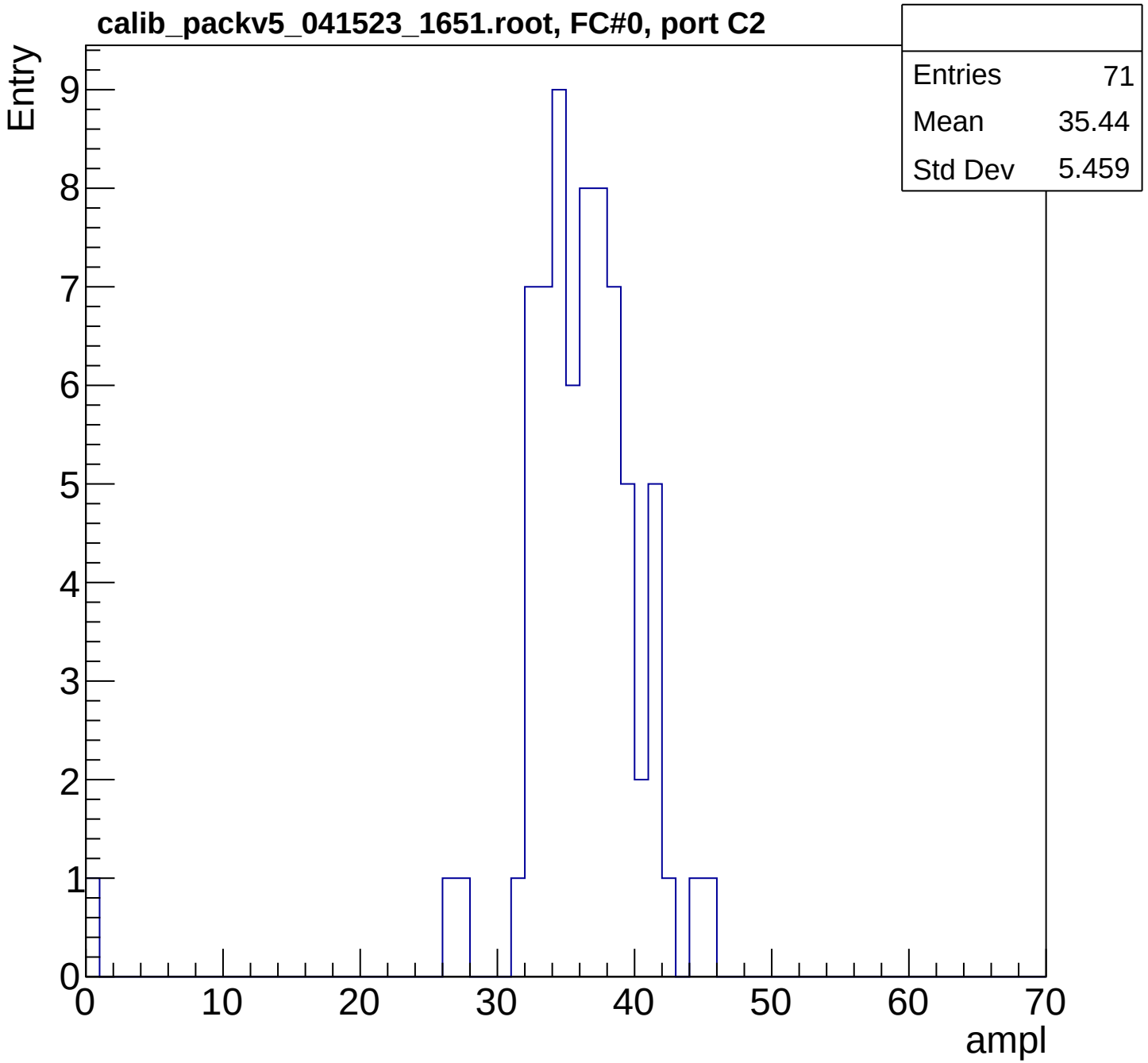
B1L103S, U17-ch96, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 35.44
Std Dev 5.459
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
50
60
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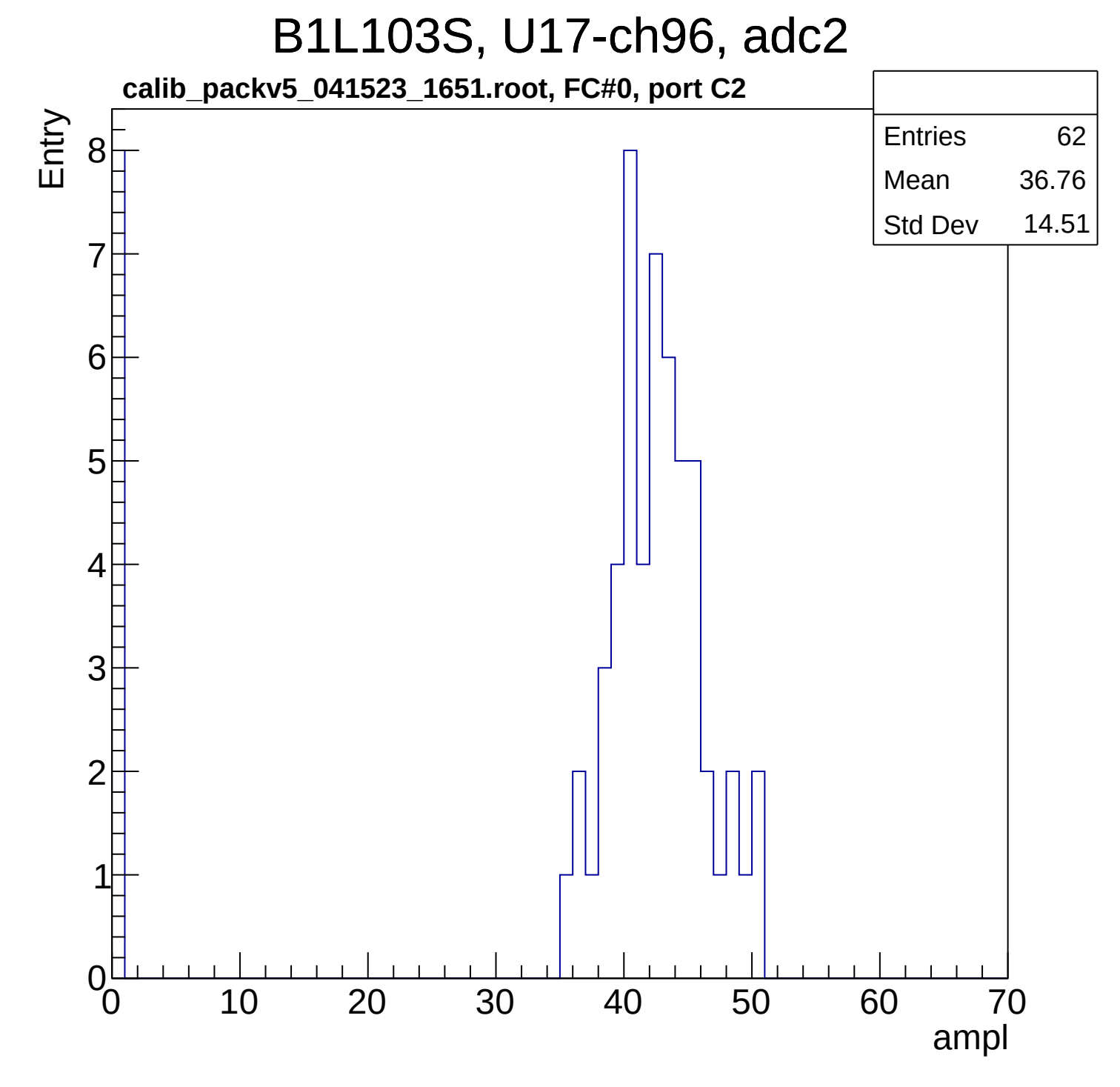
B1L103S, U17-ch96, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 36.76
Std Dev 14.51
Entry
ampl
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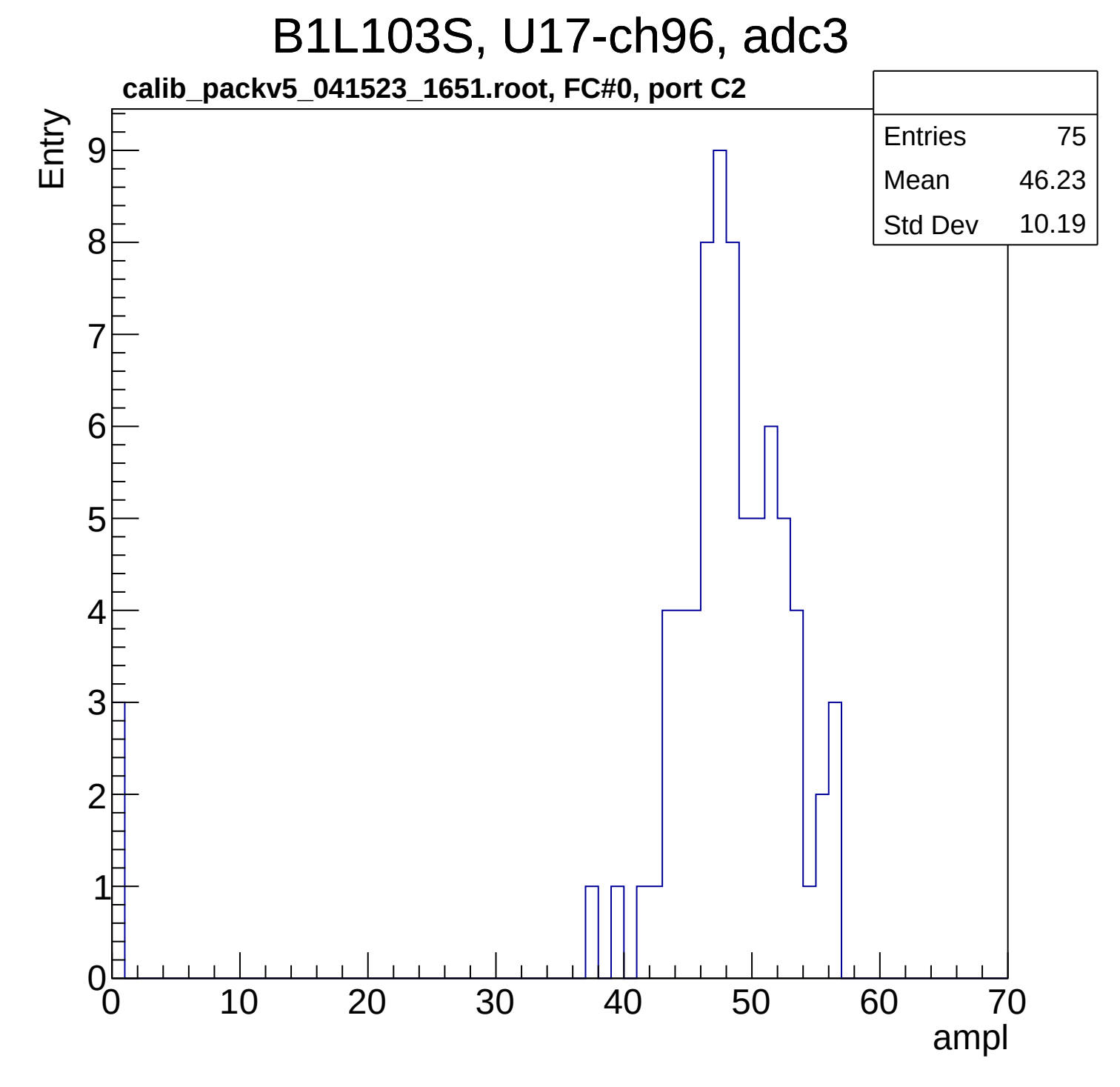
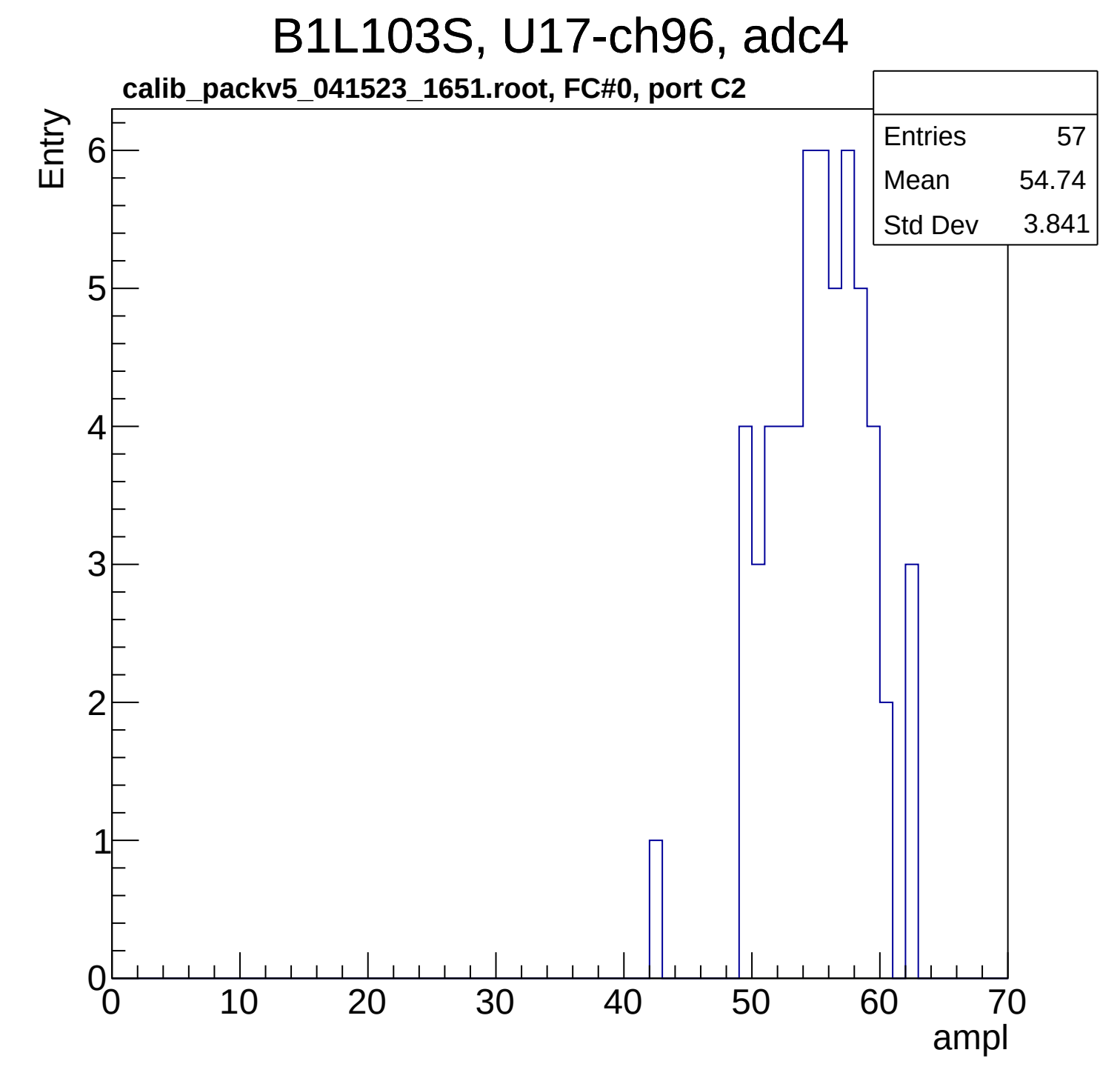
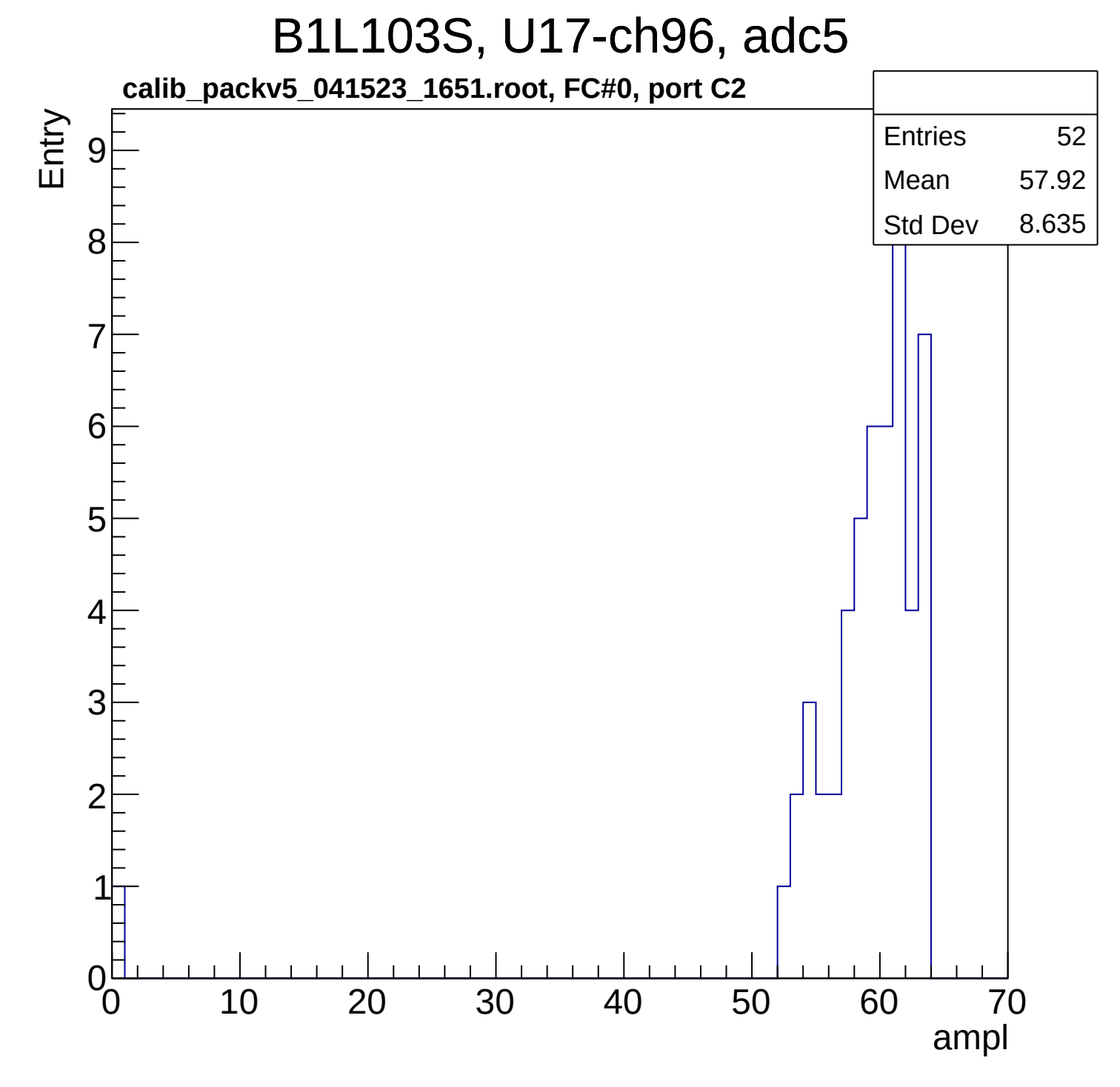
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U17-ch96, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 46.23
Std Dev 10.19
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U17-ch96, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 54.74
Std Dev 3.841
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U17-ch96, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 57.92
Std Dev 8.635
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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60
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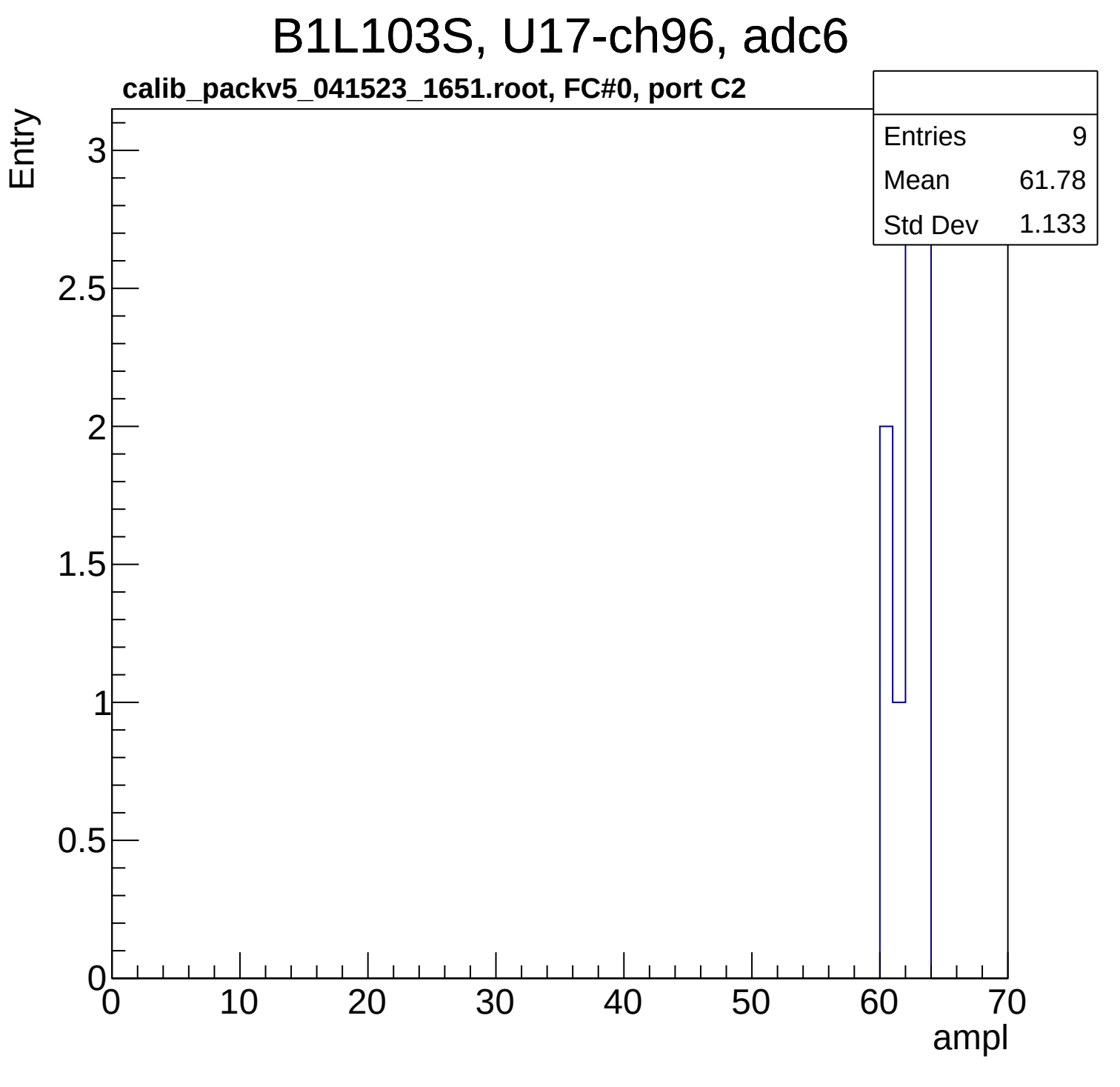
B1L103S, U17-ch96, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 9
Mean 61.78
Std Dev 1.133
Entry
ampl
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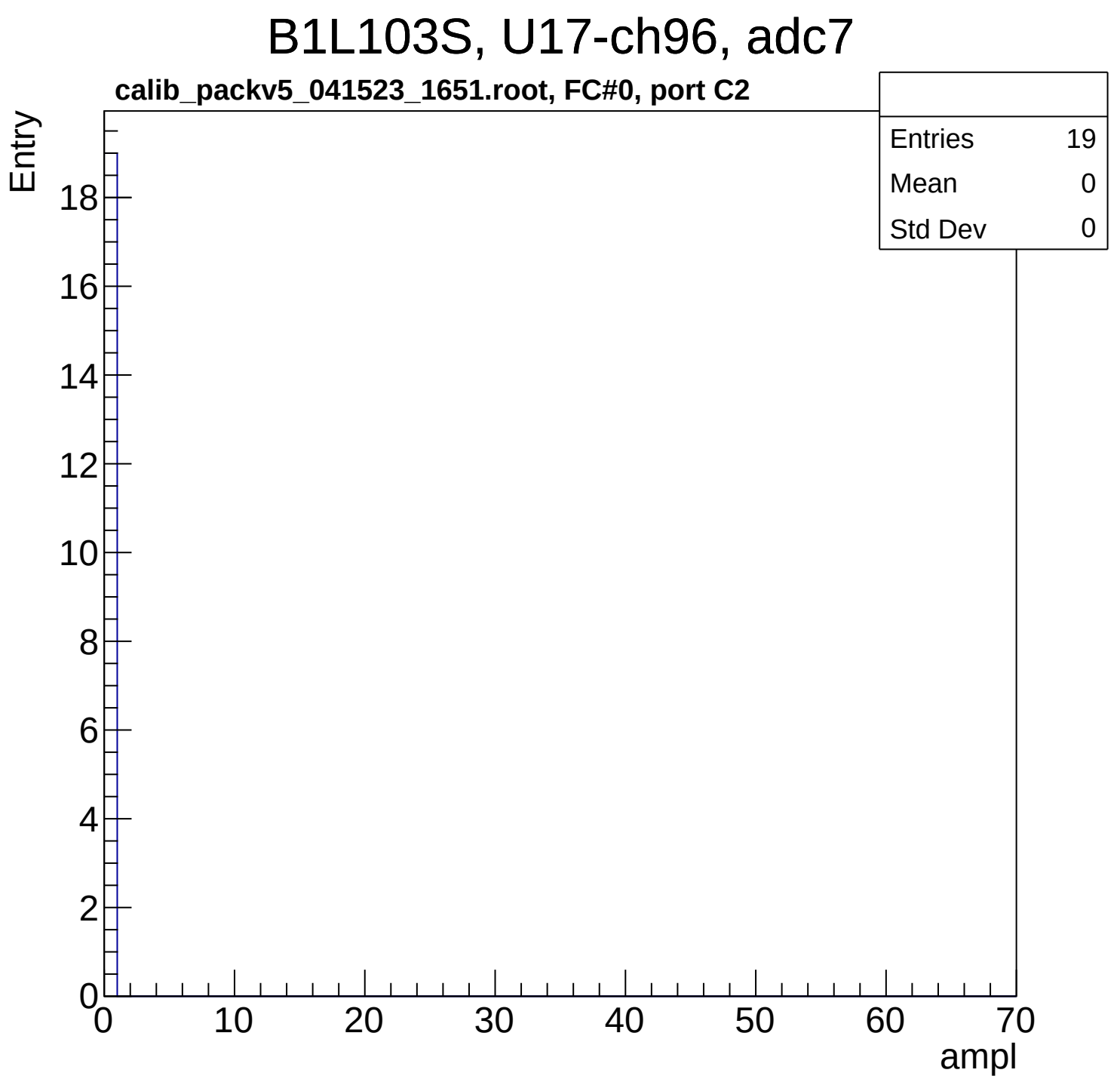
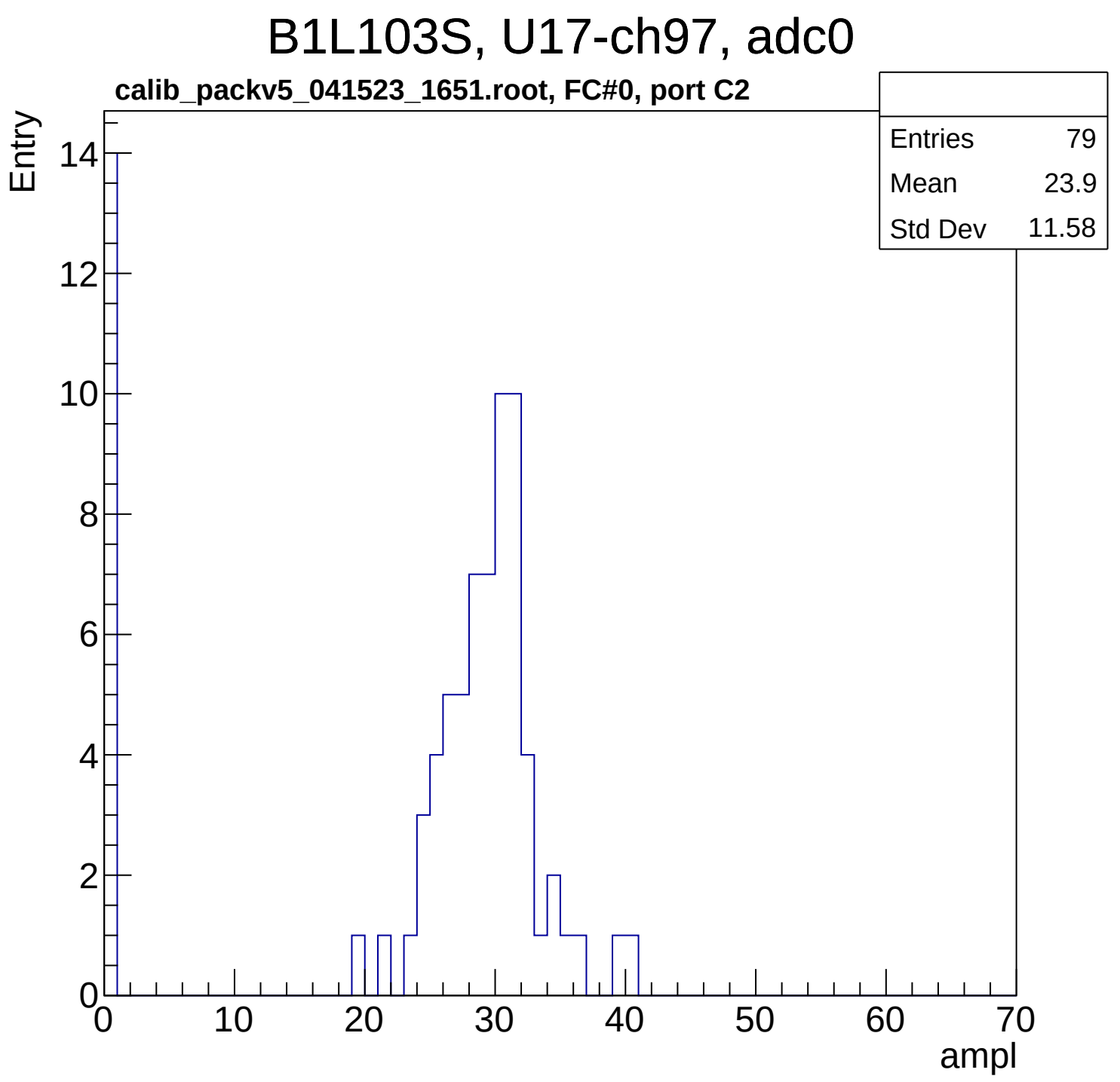
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U17-ch96, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch97, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 23.9
Std Dev 11.58
Entry
ampl
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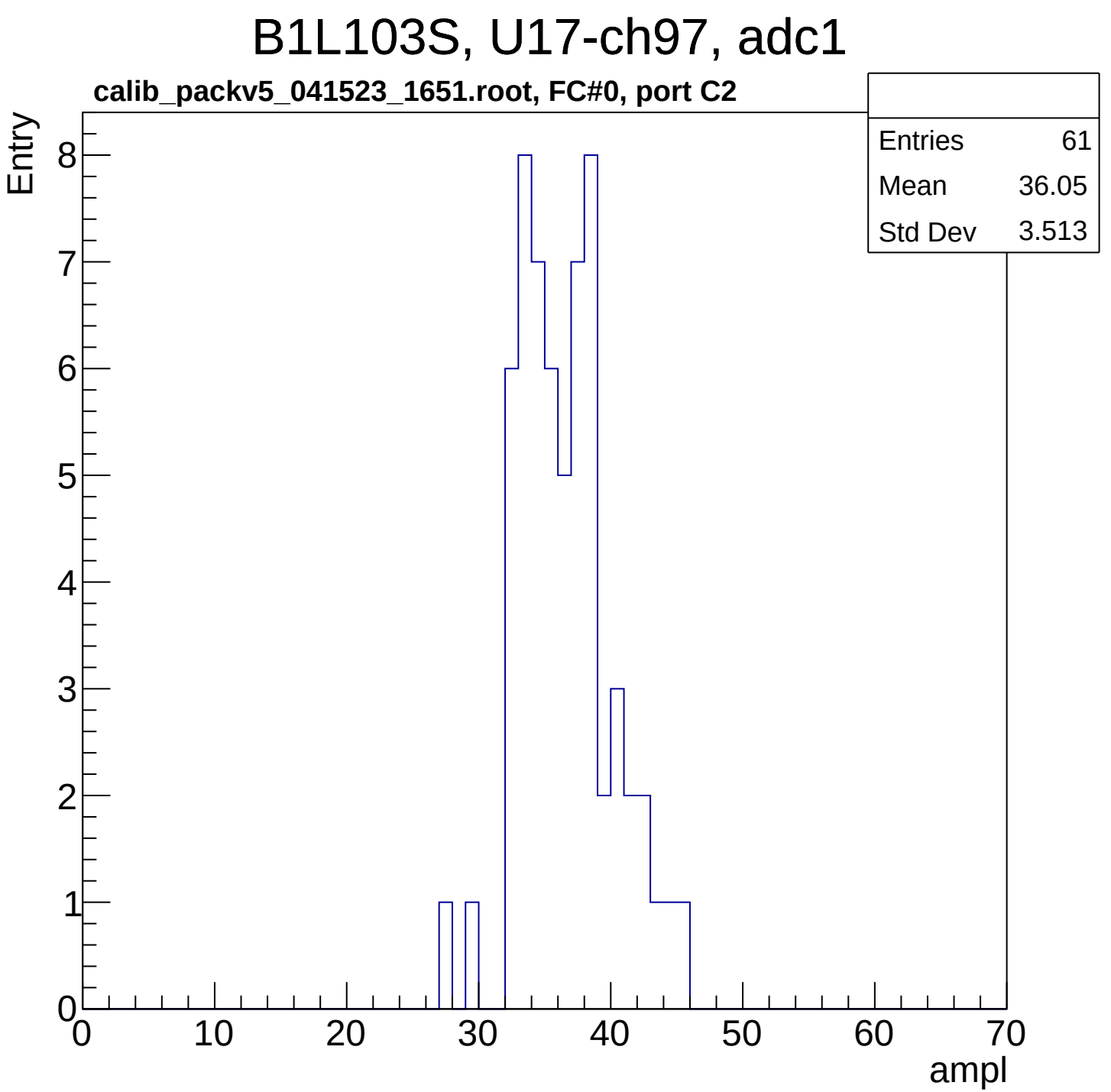
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L103S, U17-ch97, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 36.05
Std Dev 3.513
Entry
ampl
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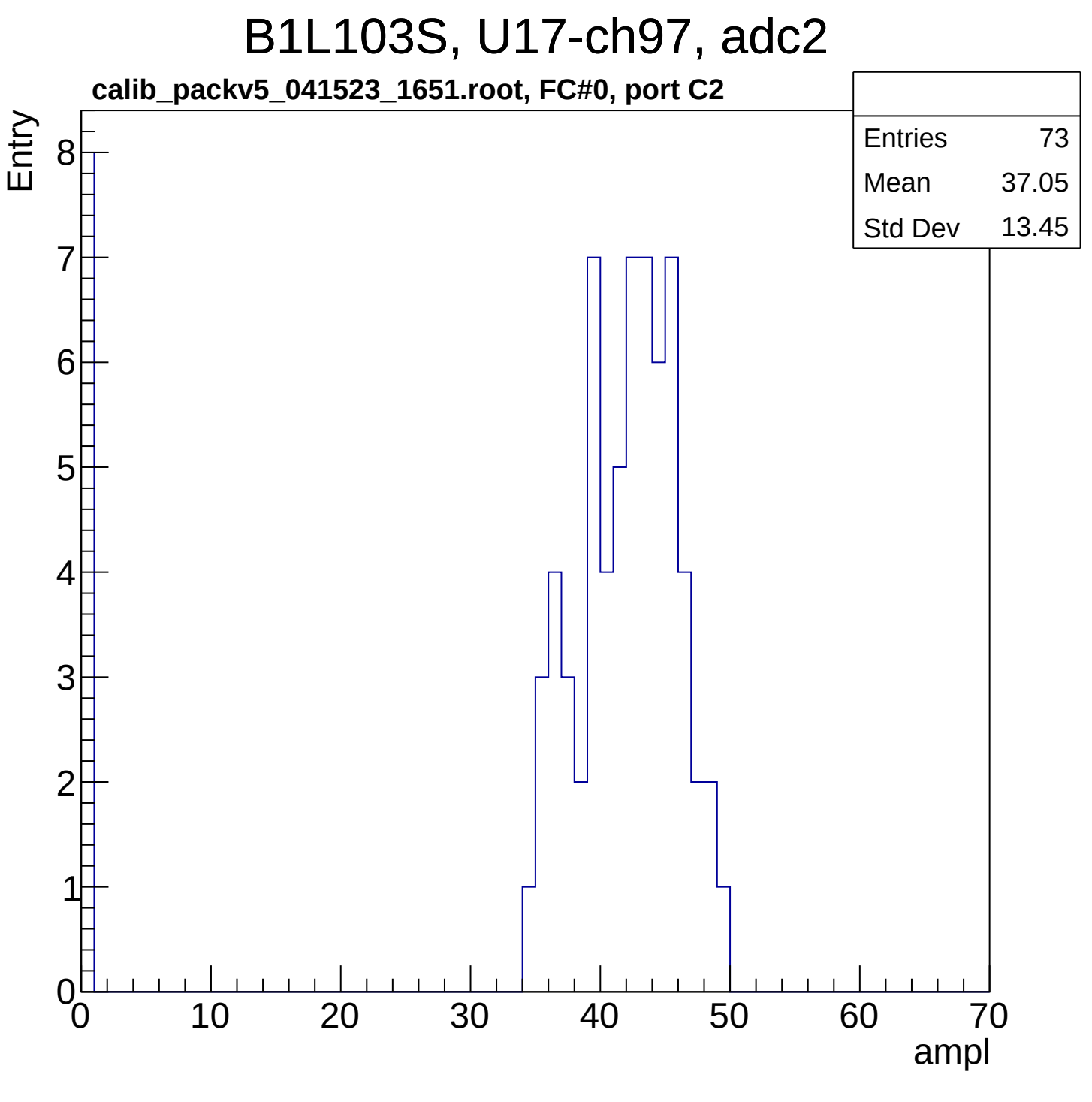
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U17-ch97, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 37.05
Std Dev 13.45
Entry
ampl
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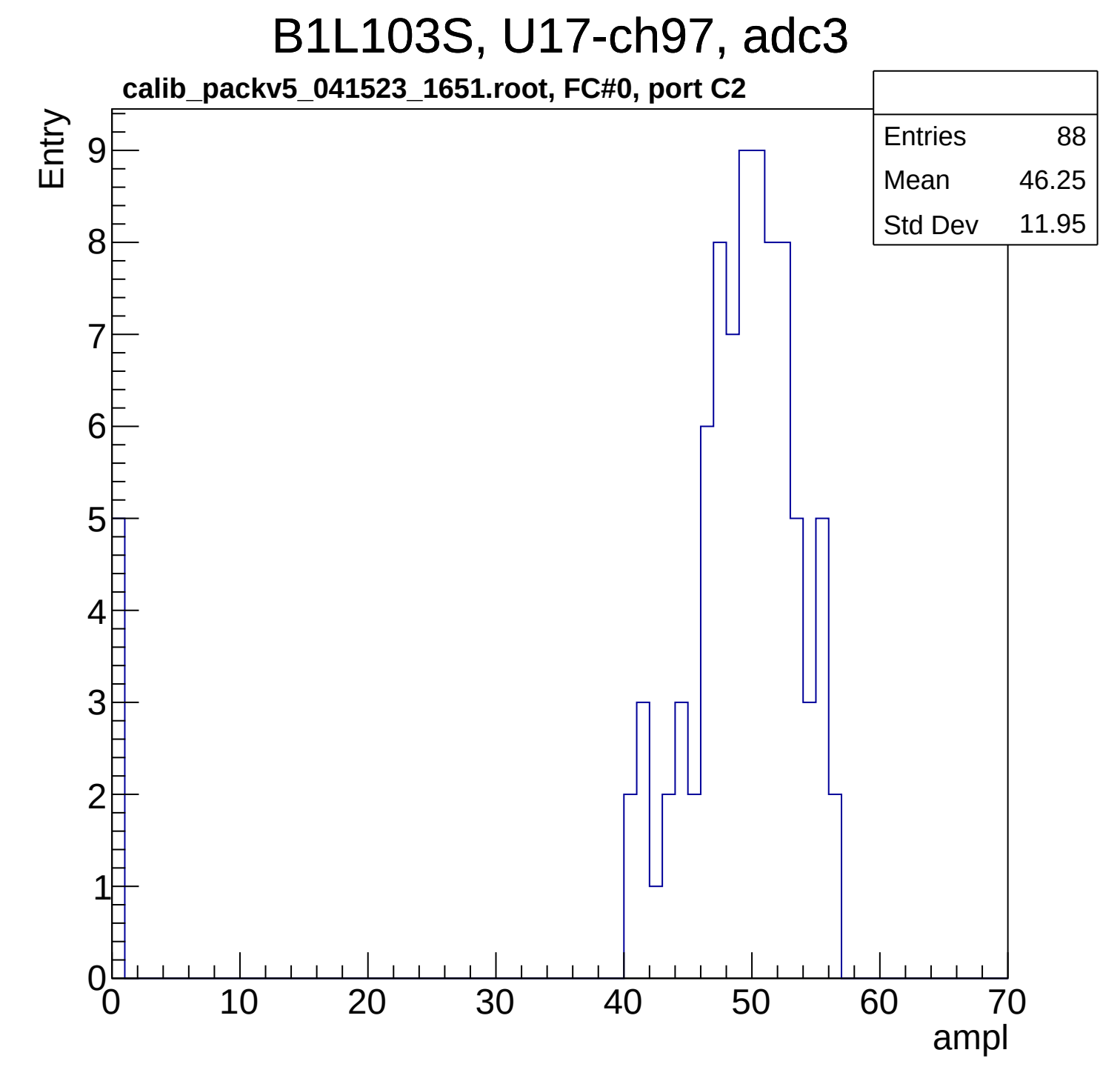
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U17-ch97, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 88
Mean 46.25
Std Dev 11.95
Entry
ampl
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3
4
5
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7
8
9
0
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40
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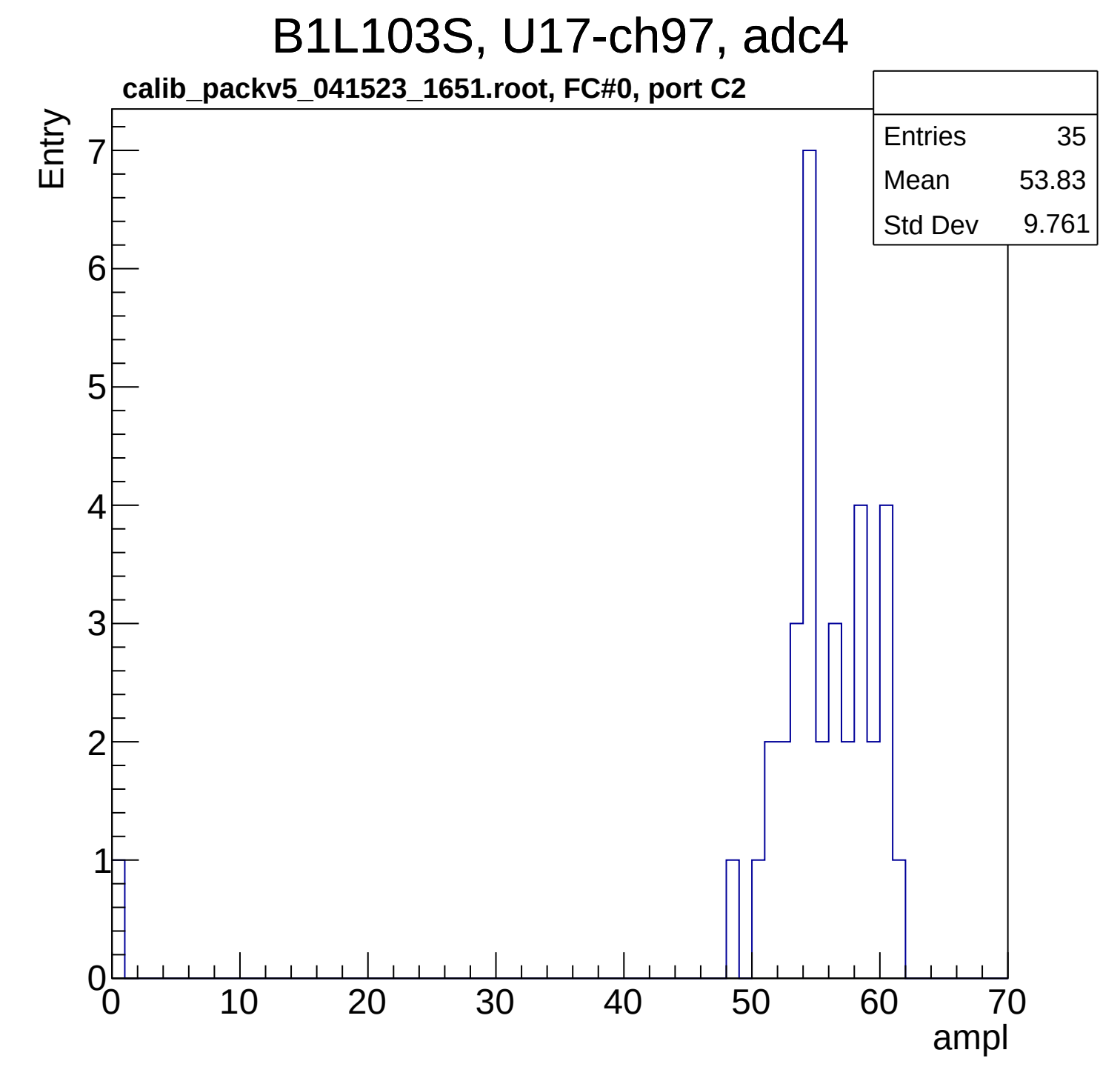
60
70


B1L103S, U17-ch97, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 35
Mean 53.83
Std Dev 9.761
Entry
ampl
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4
5
6
7
0
10
20
30
40
50
60
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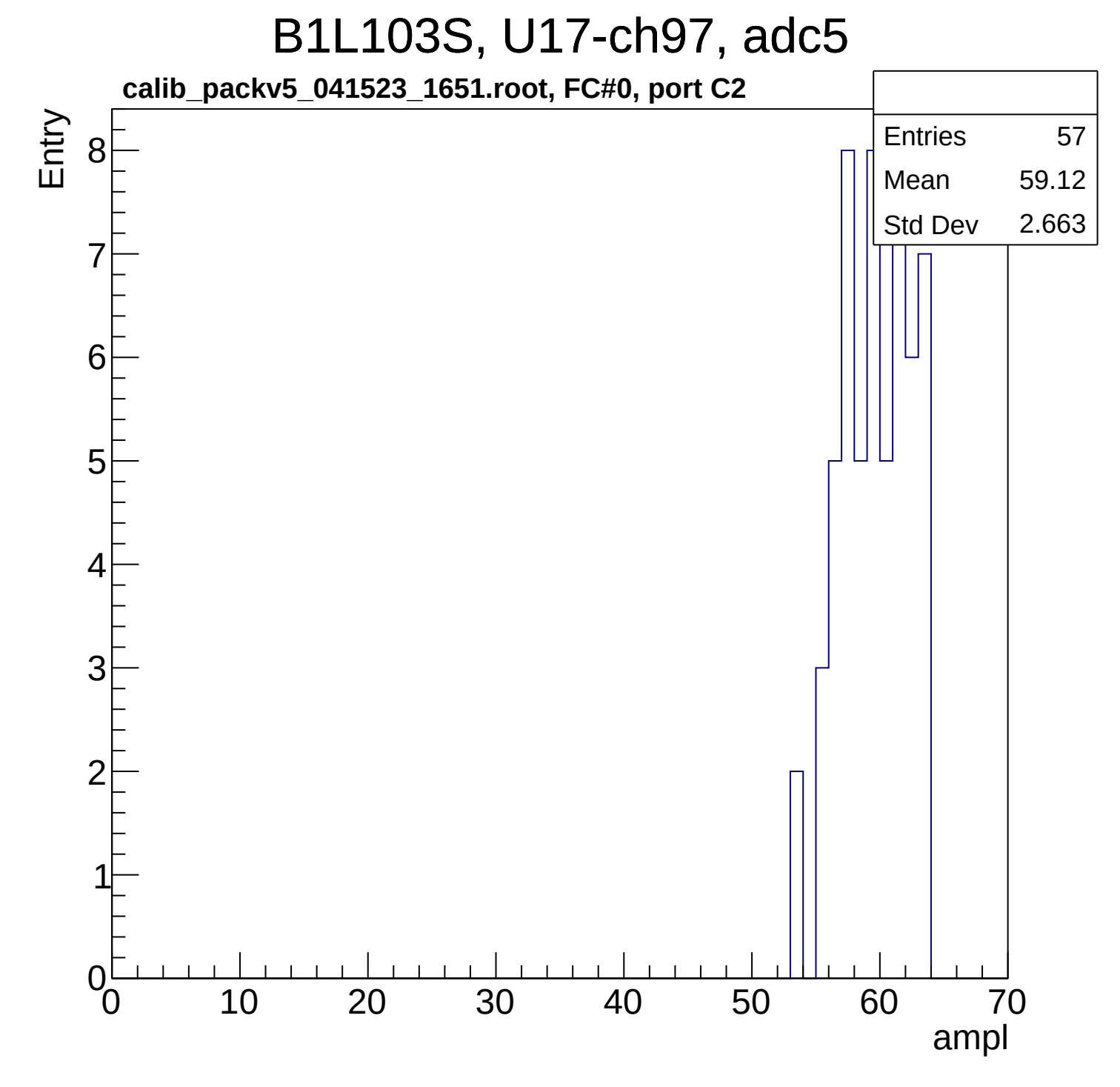
B1L103S, U17-ch97, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 59.12
Std Dev 2.663
Entry
ampl
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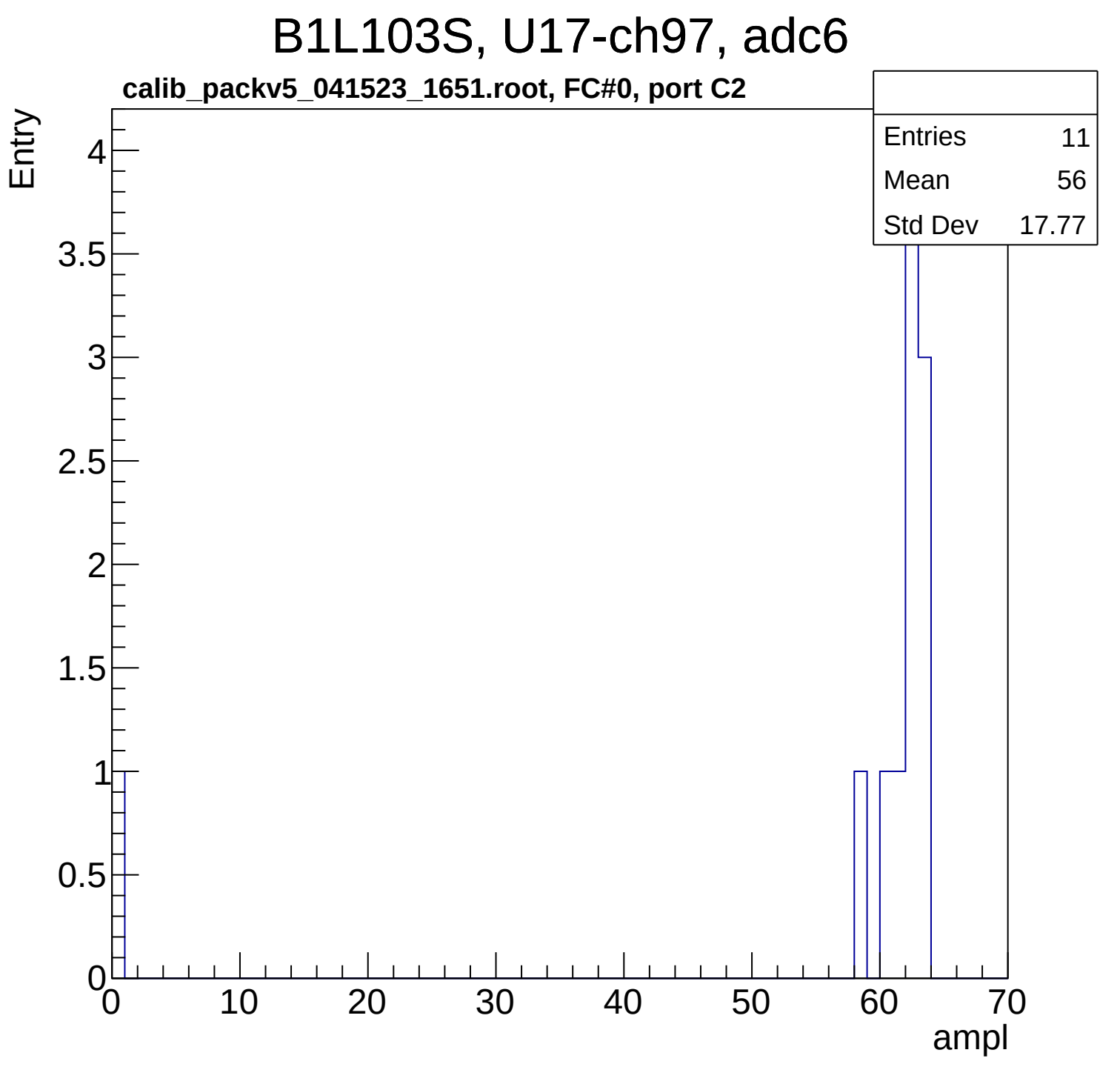
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U17-ch97, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 56
Std Dev 17.77
Entry
ampl
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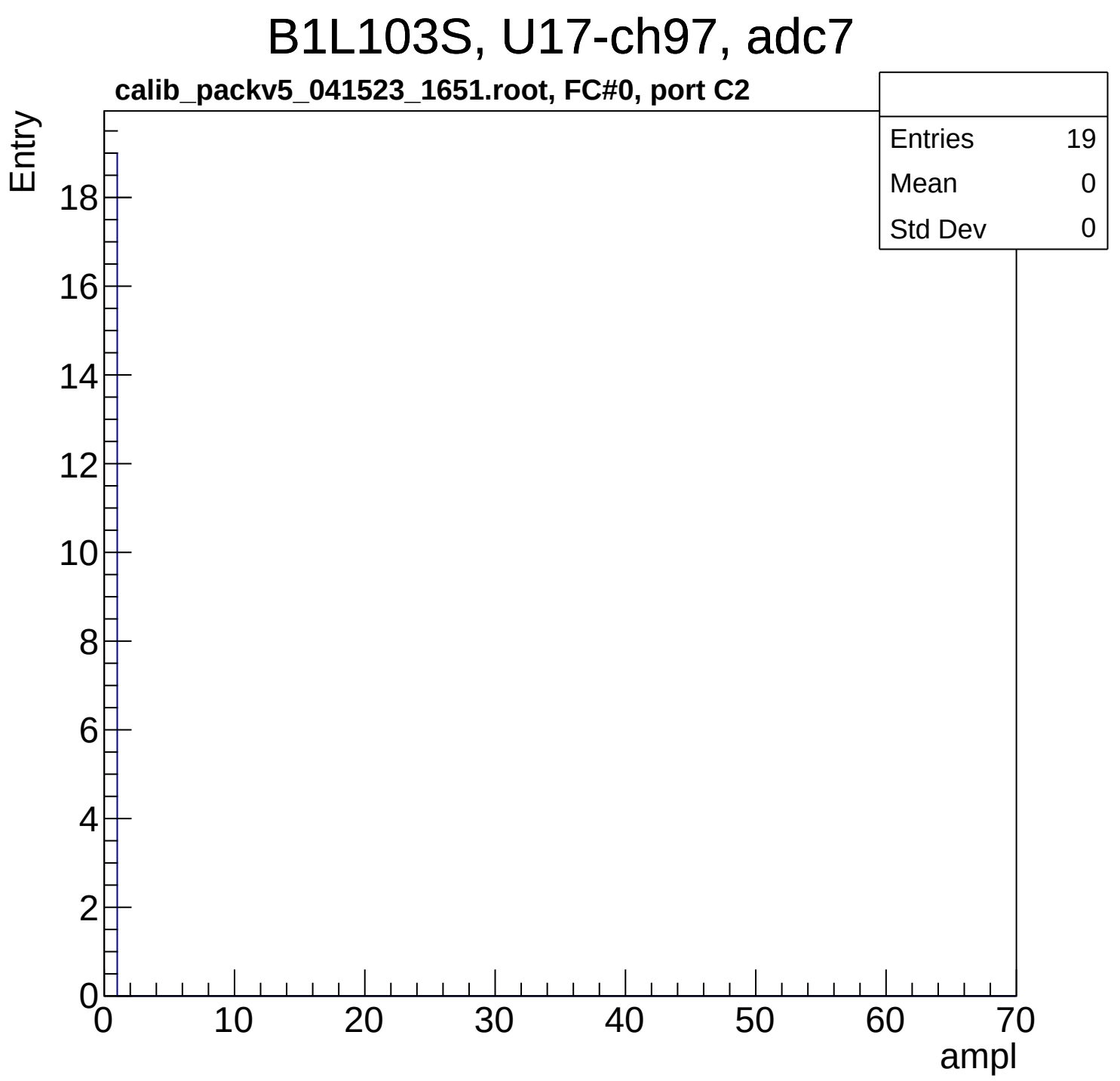
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U17-ch97, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
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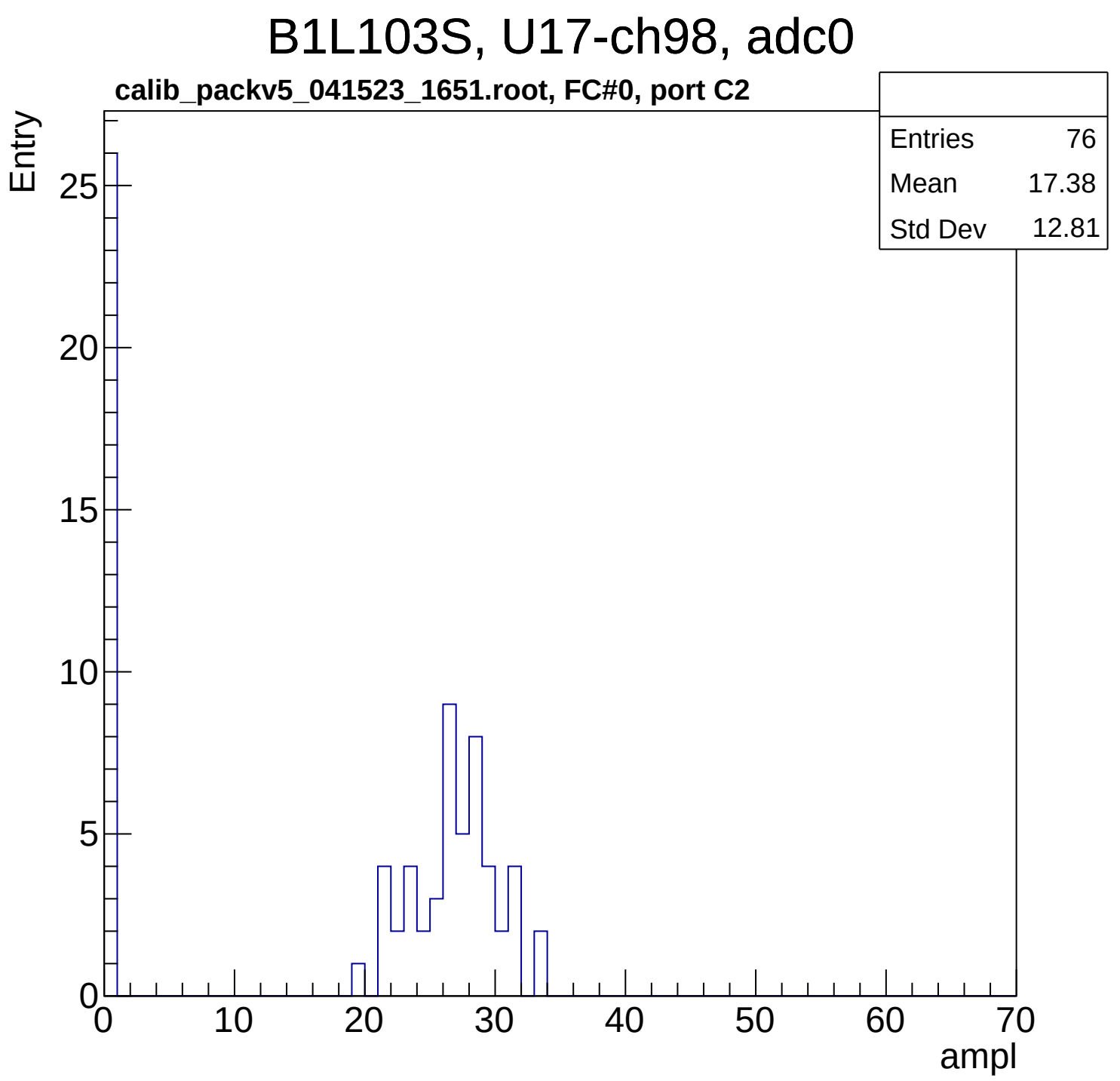
50
60
70
ampl


B1L103S, U17-ch98, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 17.38
Std Dev 12.81
Entry
0
5
10
15
20
25
0
10
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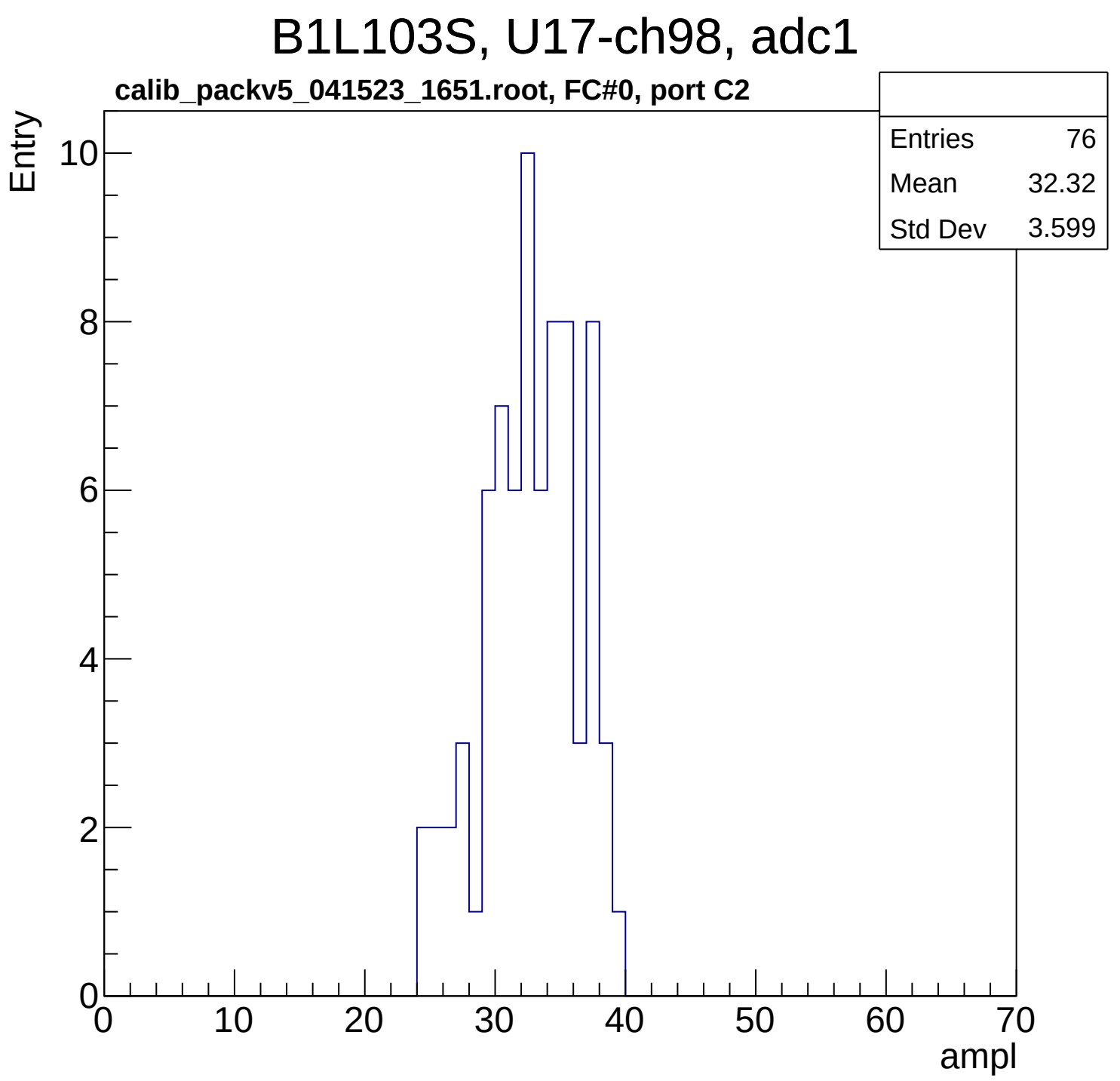
30
40
50
60
70
ampl


B1L103S, U17-ch98, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 32.32
Std Dev 3.599
Entry
ampl
0
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4
6
8
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0
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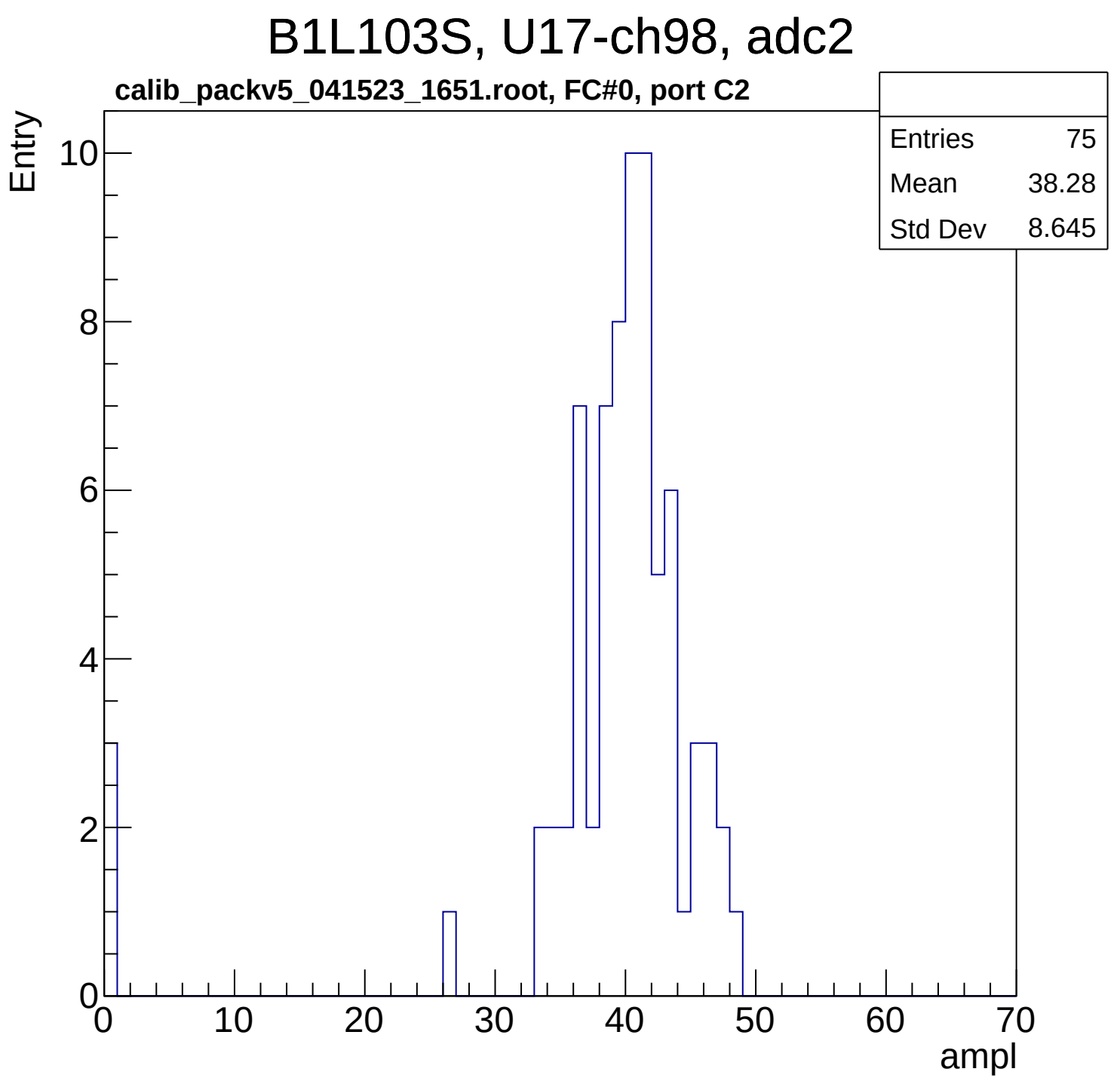
20
30
40
50
60
70


B1L103S, U17-ch98, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 38.28
Std Dev 8.645
Entry
ampl
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4
6
8
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0
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20
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60
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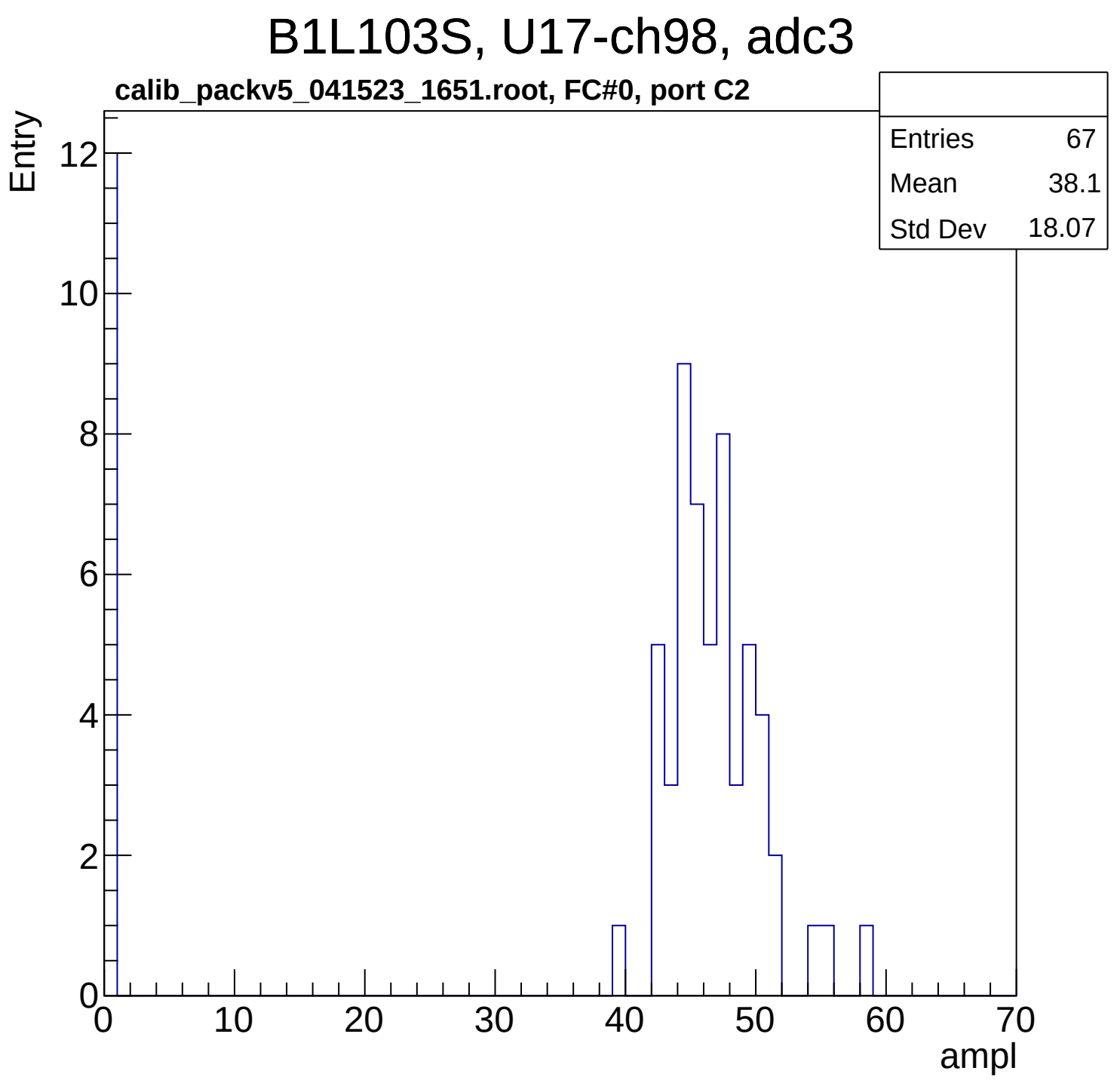
B1L103S, U17-ch98, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 38.1
Std Dev 18.07
Entry
0
2
4
6
8
10
12
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10
20
30
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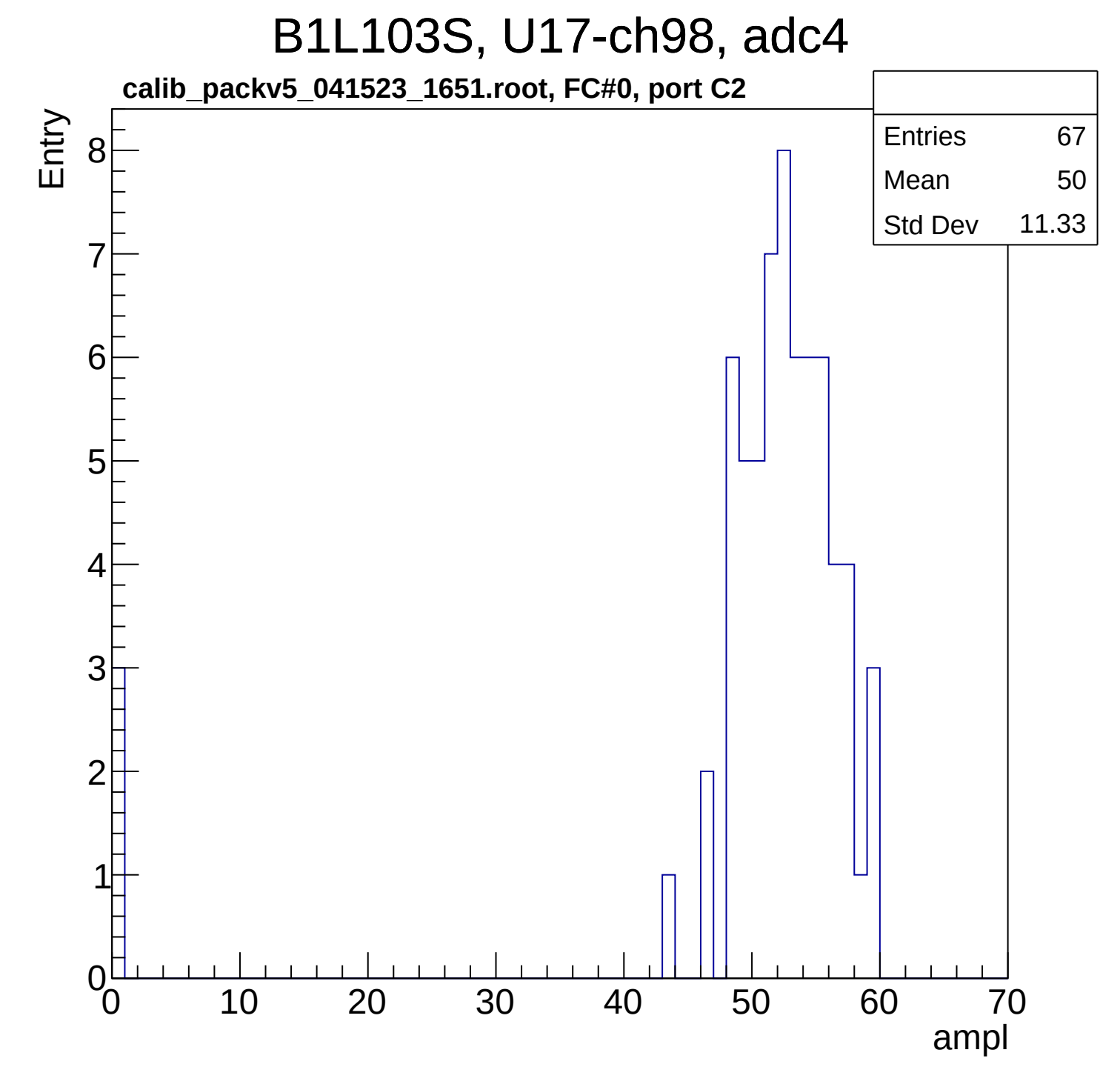
50
60
70
ampl


B1L103S, U17-ch98, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 50
Std Dev 11.33
Entry
ampl
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1
2
3
4
5
6
7
8
0
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60
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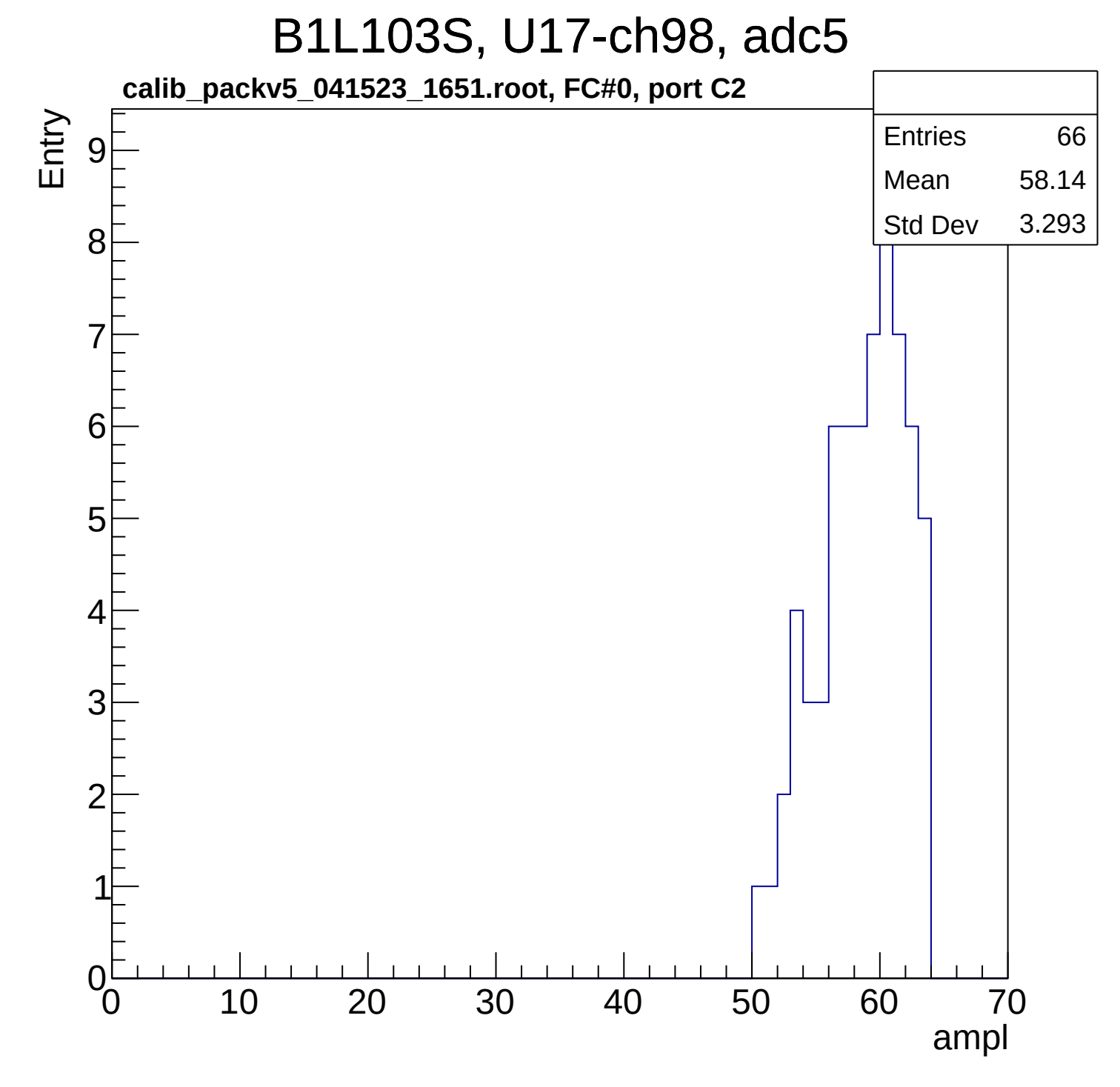
B1L103S, U17-ch98, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 58.14
Std Dev 3.293
Entry
ampl
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2
3
4
5
6
7
8
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0
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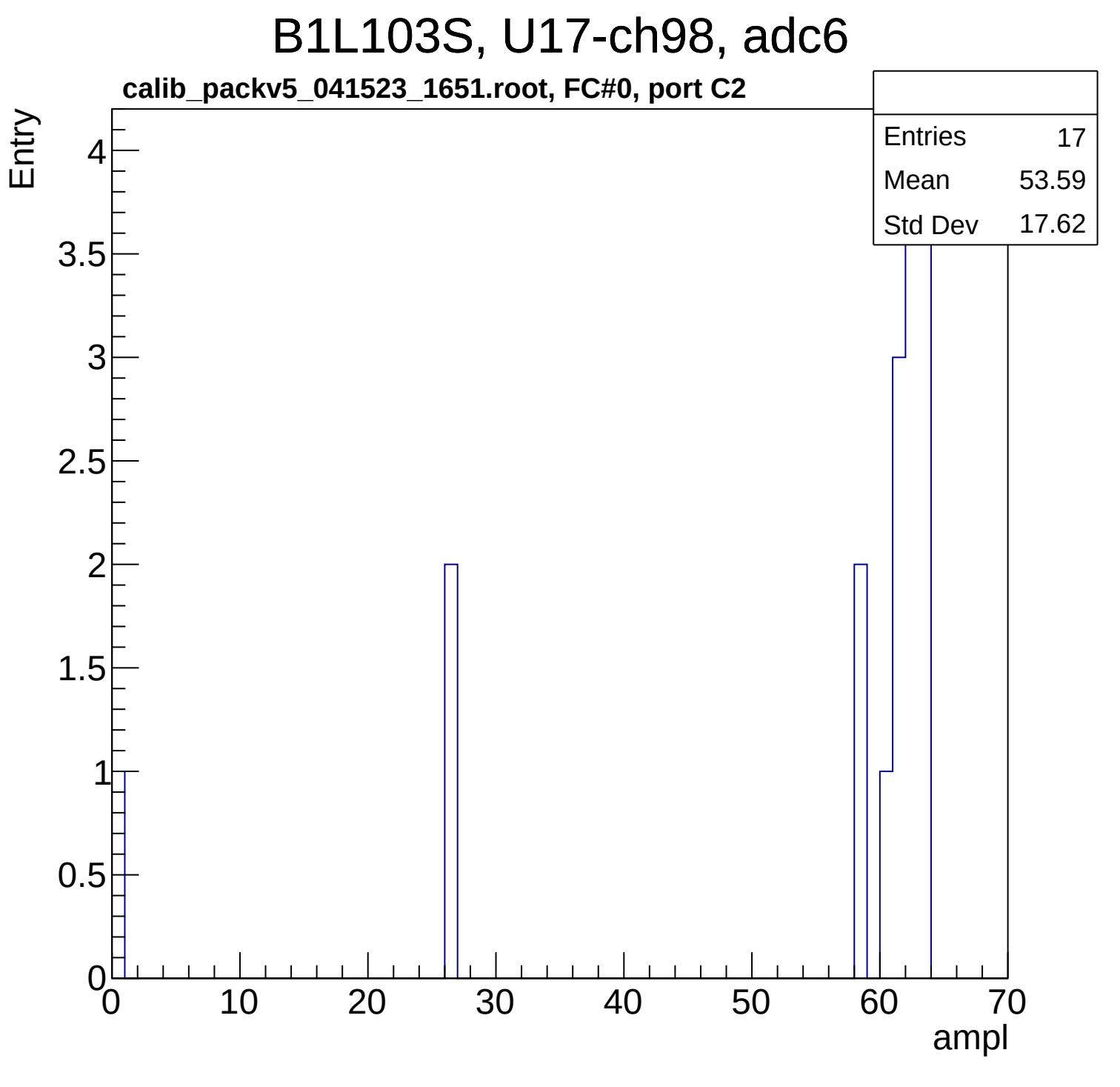
60
70


B1L103S, U17-ch98, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 17
Mean 53.59
Std Dev 17.62
Entry
ampl
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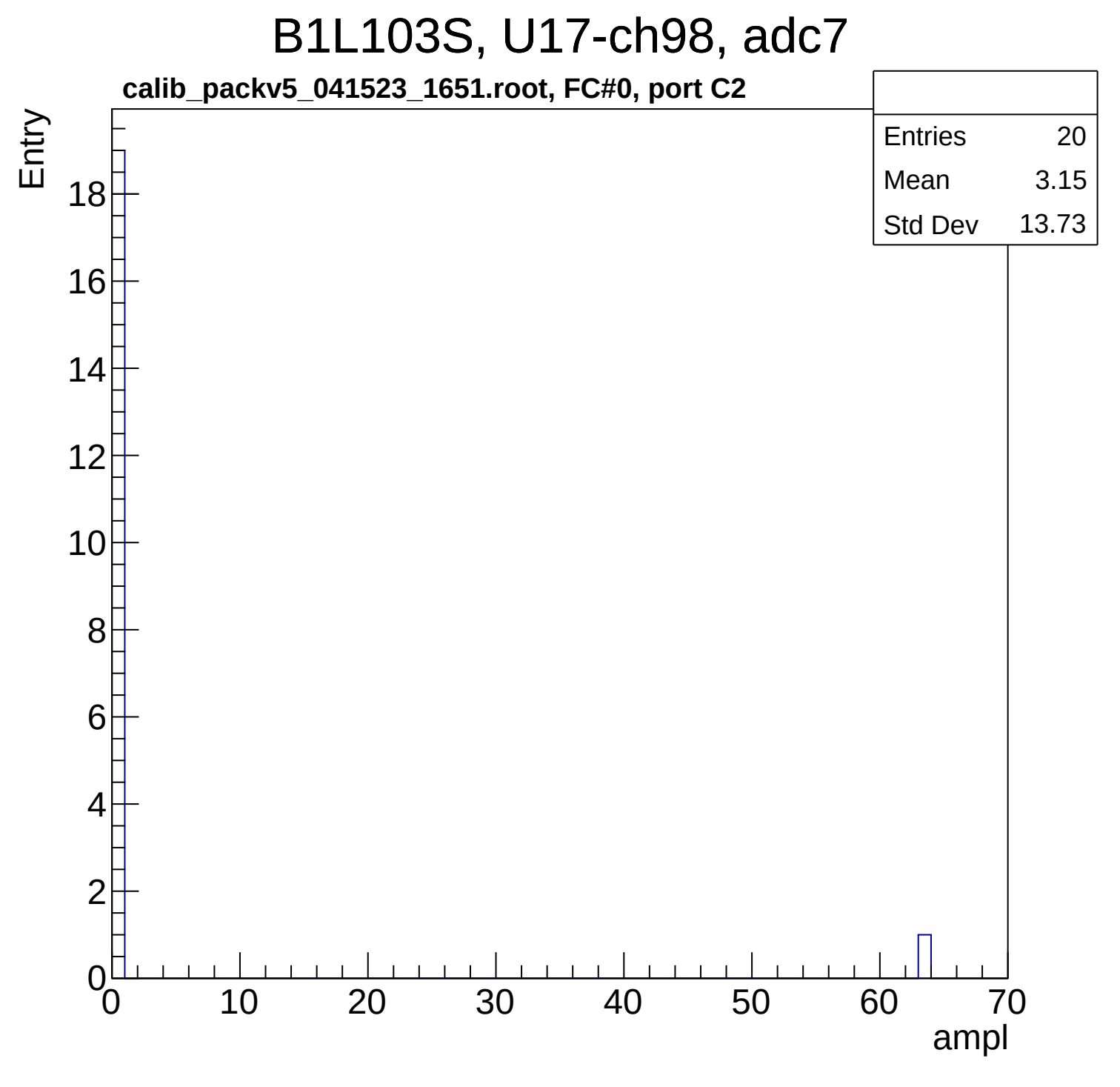
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U17-ch98, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
0
2
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6
8
10
12
14
16
18
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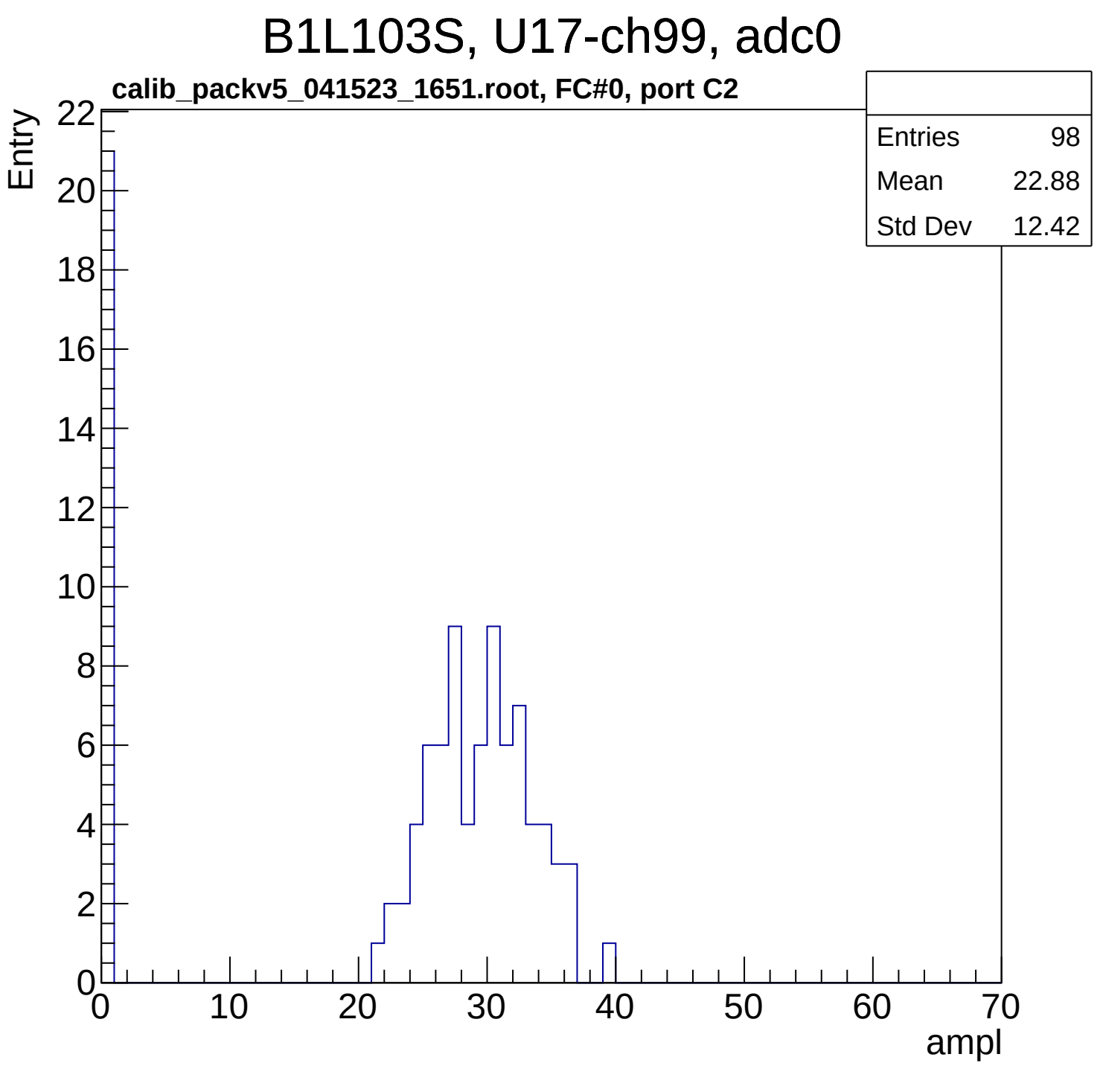
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch99, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 98
Mean 22.88
Std Dev 12.42
Entry
ampl
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8
10
12
14
16
18
20
22
0
10
20
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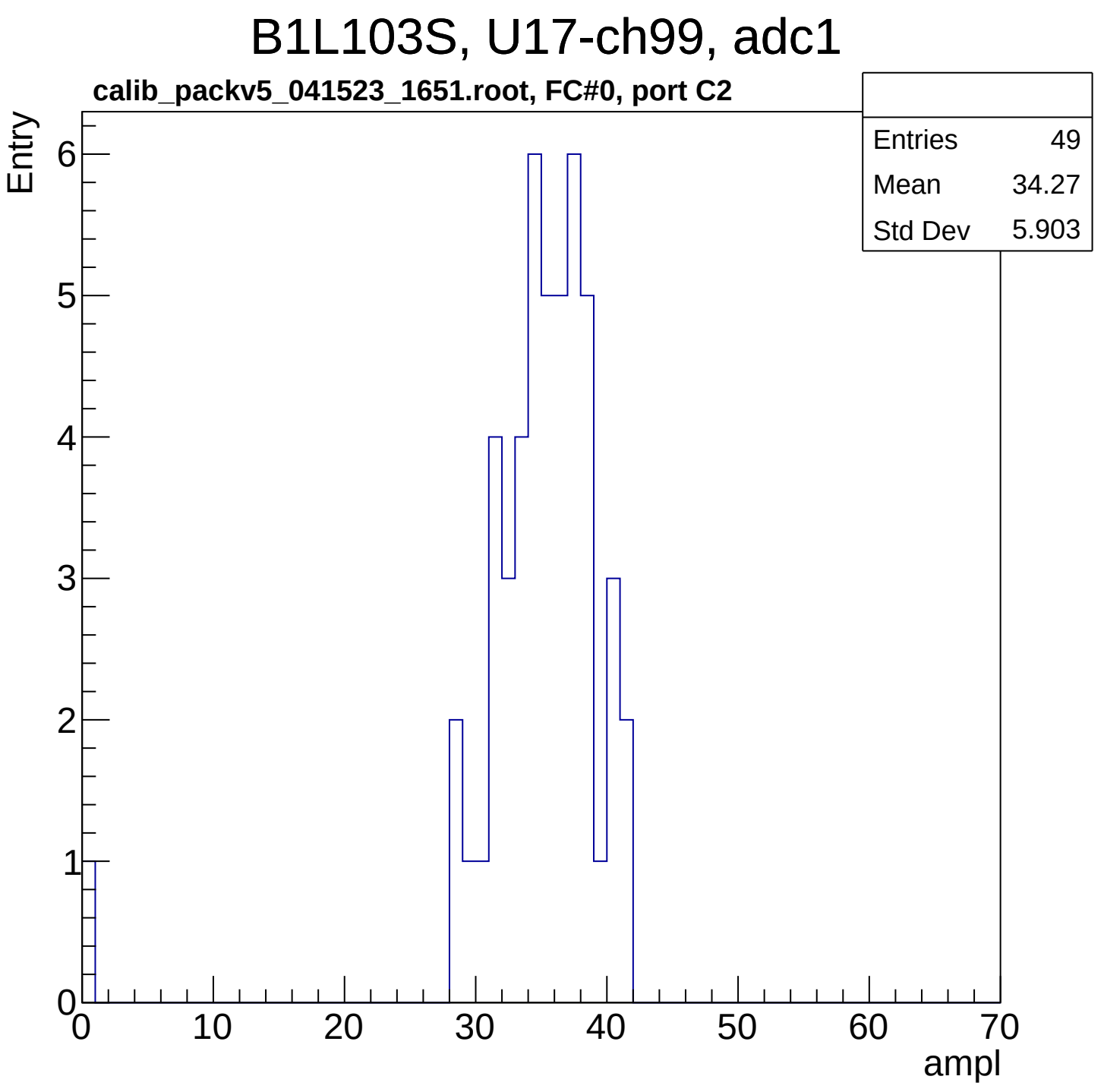
40
50
60
70


B1L103S, U17-ch99, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 34.27
Std Dev 5.903
Entry
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3
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5
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10
20
30
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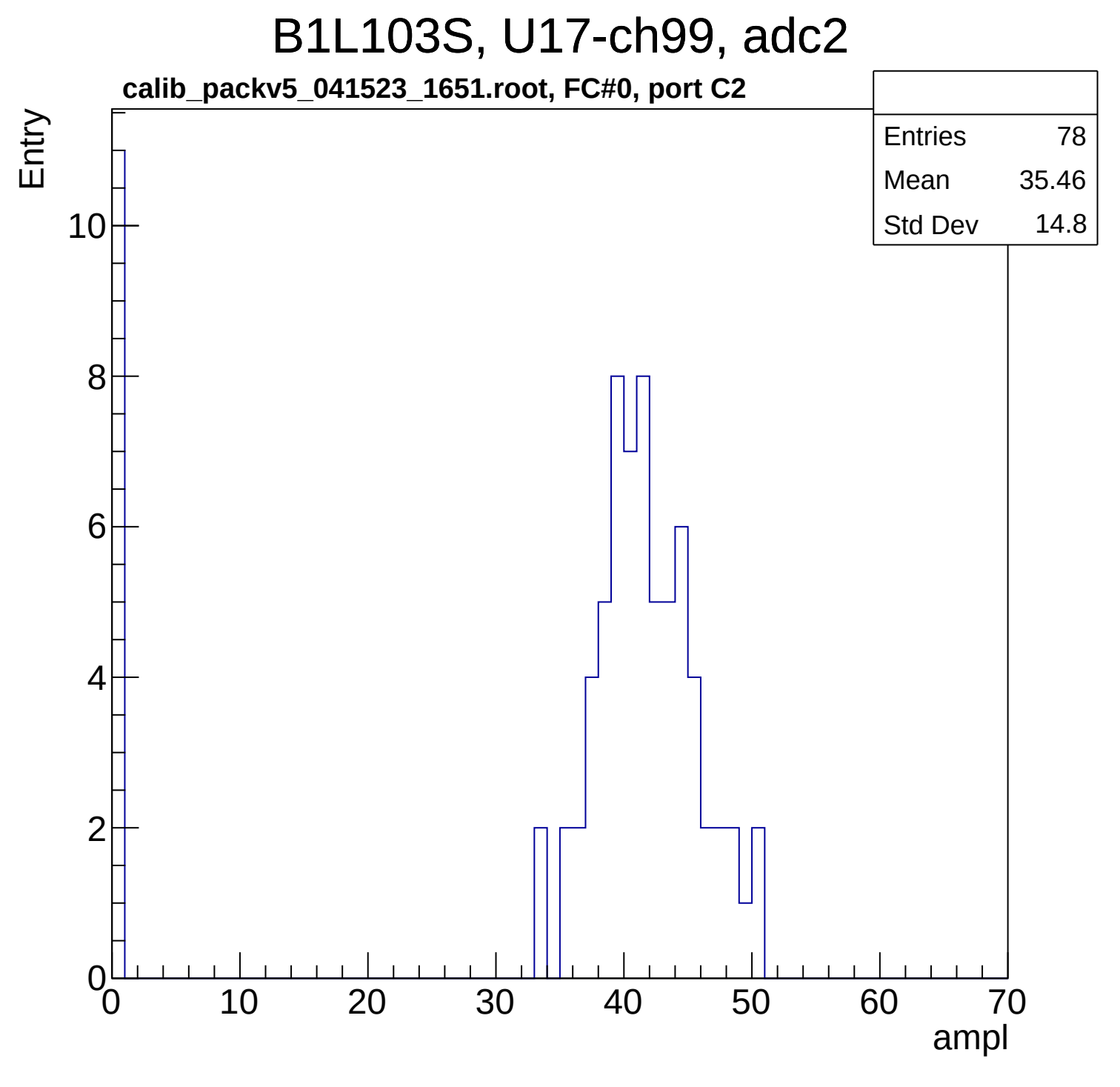
50
60
70
ampl


B1L103S, U17-ch99, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 35.46
Std Dev 14.8
Entry
0
2
4
6
8
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10
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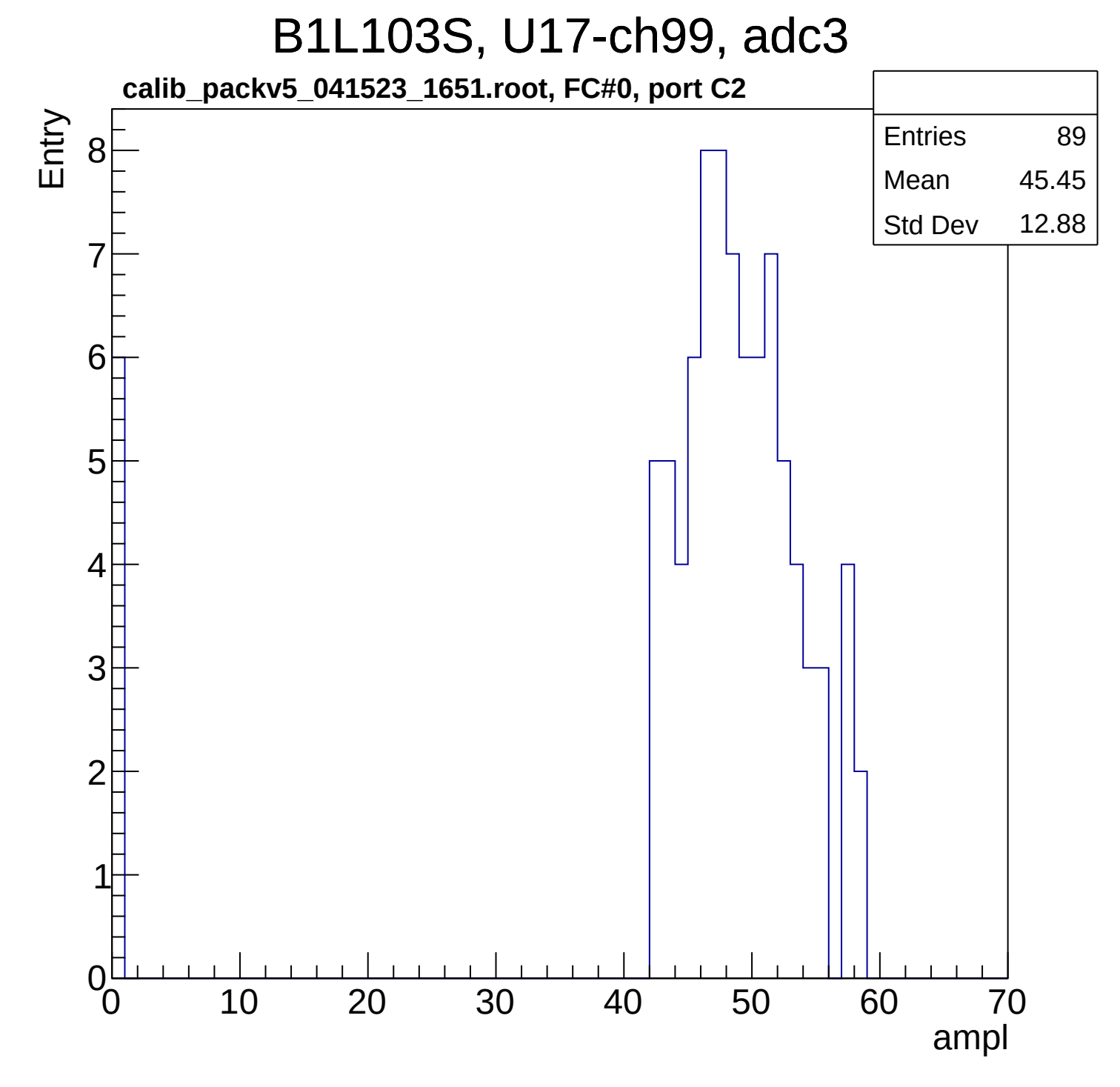
60
70
ampl


B1L103S, U17-ch99, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 89
Mean 45.45
Std Dev 12.88
Entry
ampl
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2
3
4
5
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7
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0
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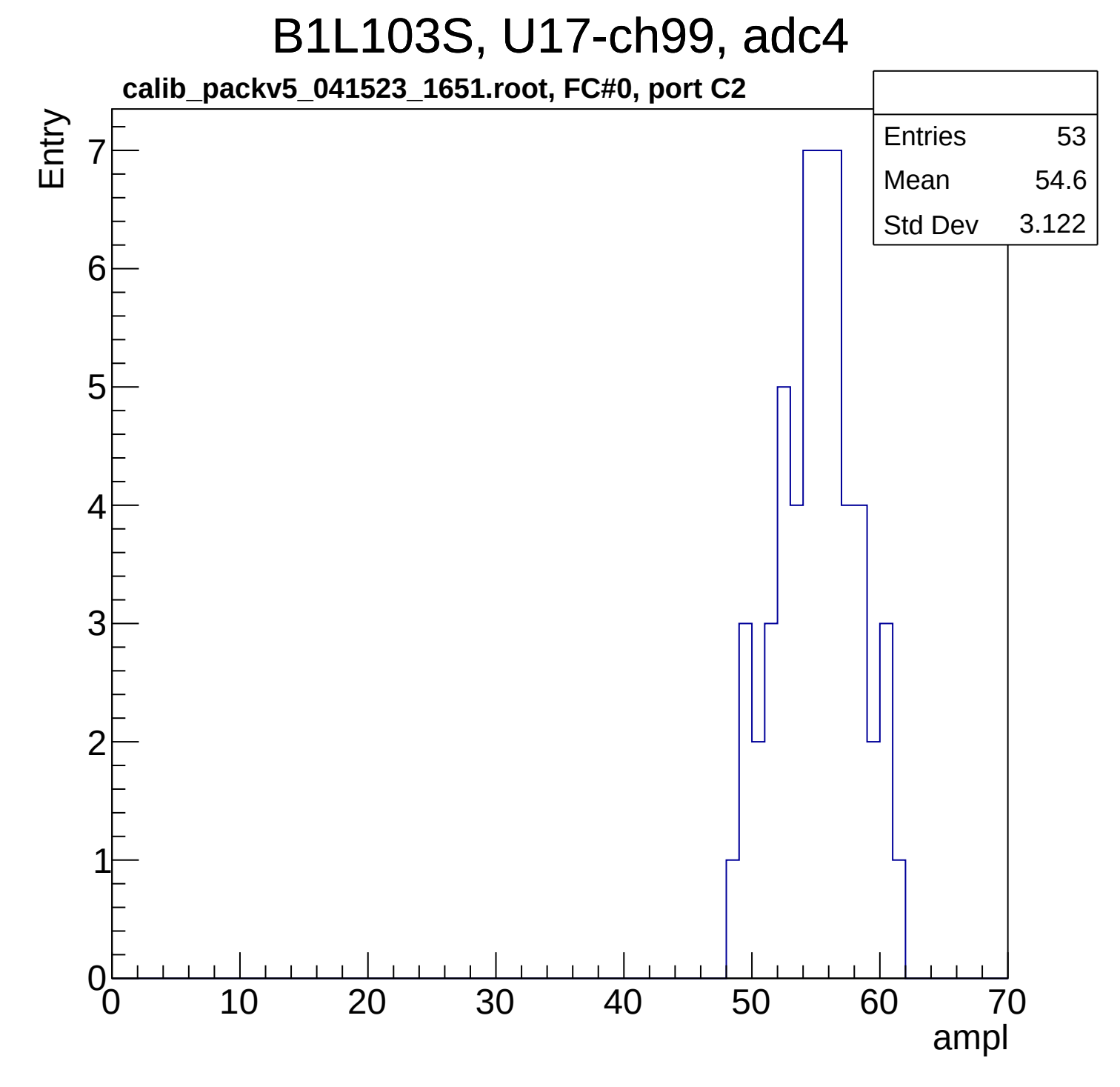
B1L103S, U17-ch99, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 54.6
Std Dev 3.122
Entry
ampl
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1
2
3
4
5
6
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0
10
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40
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60
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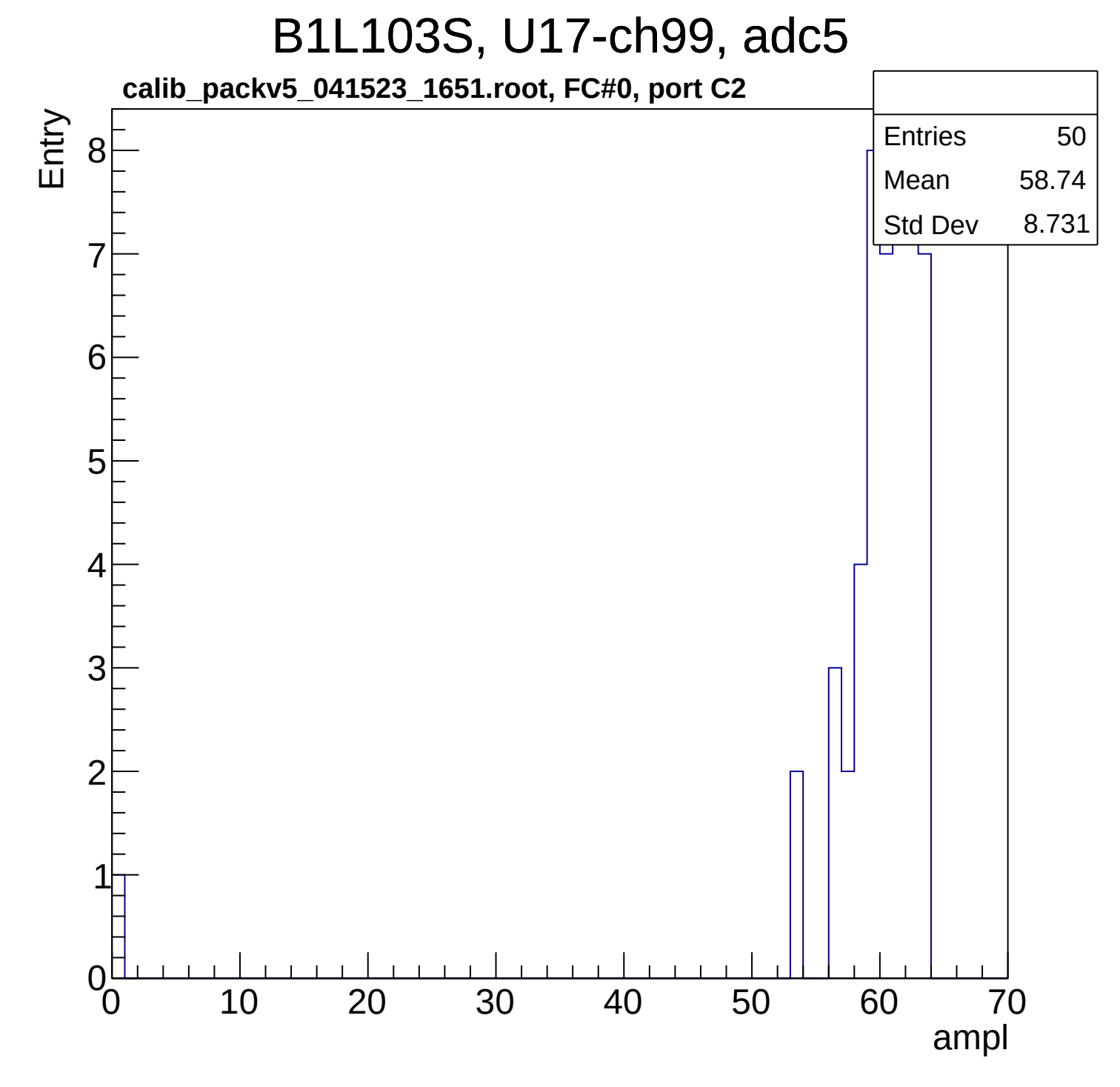
B1L103S, U17-ch99, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 58.74
Std Dev 8.731
Entry
ampl
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2
3
4
5
6
7
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0
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40
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60
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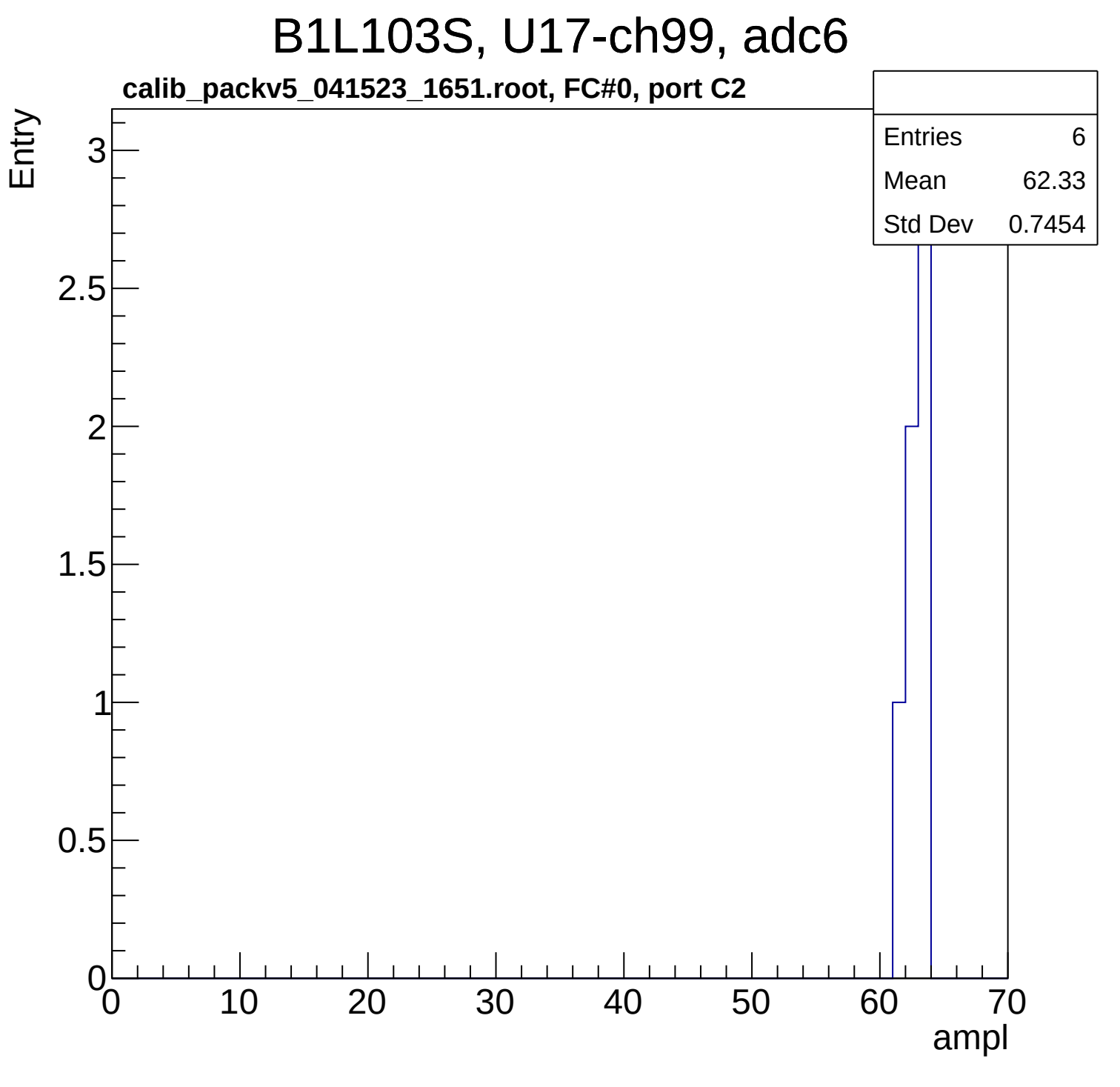
B1L103S, U17-ch99, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 62.33
Std Dev 0.7454
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
10
20
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40
50
60
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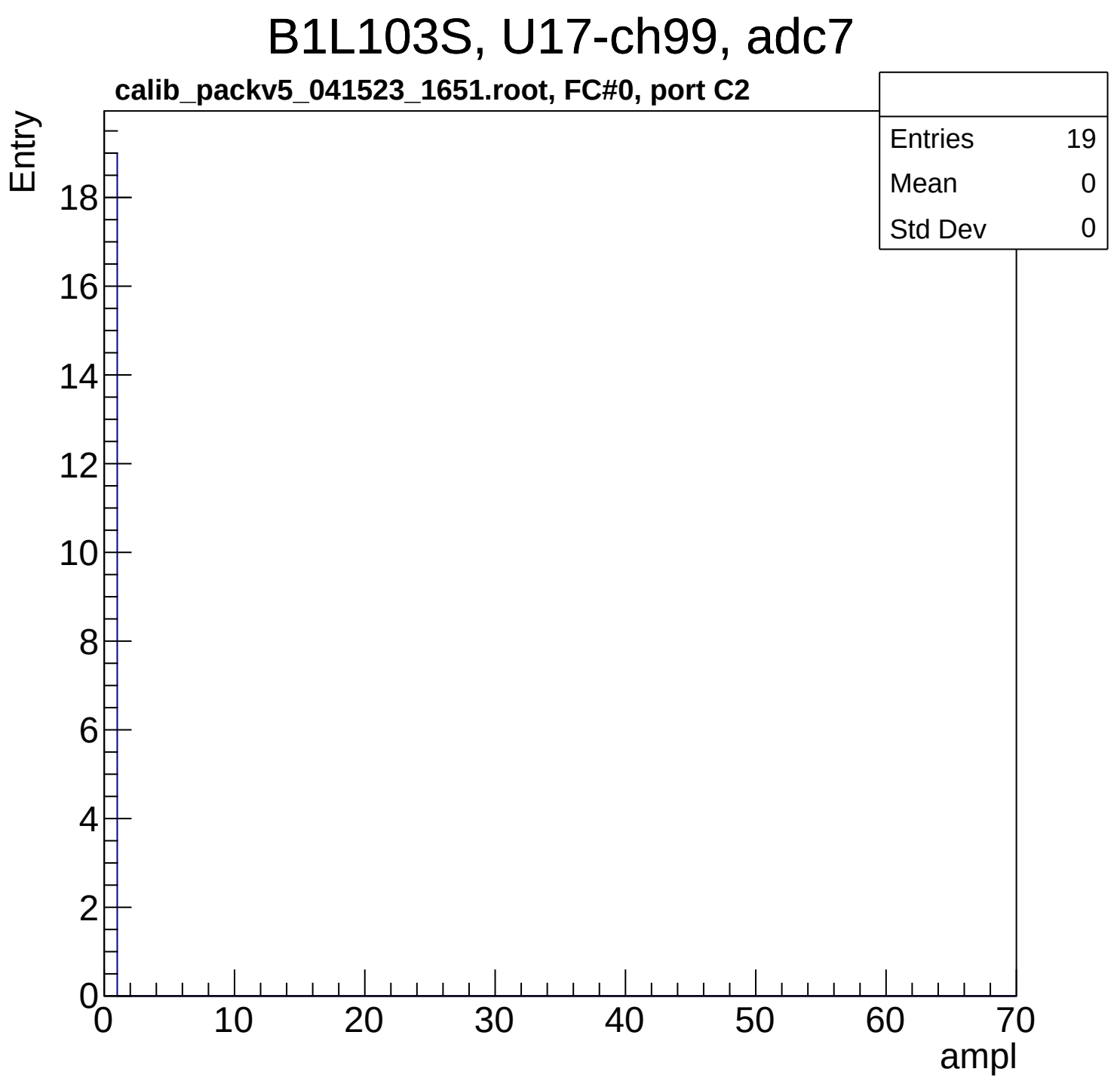
B1L103S, U17-ch99, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
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30
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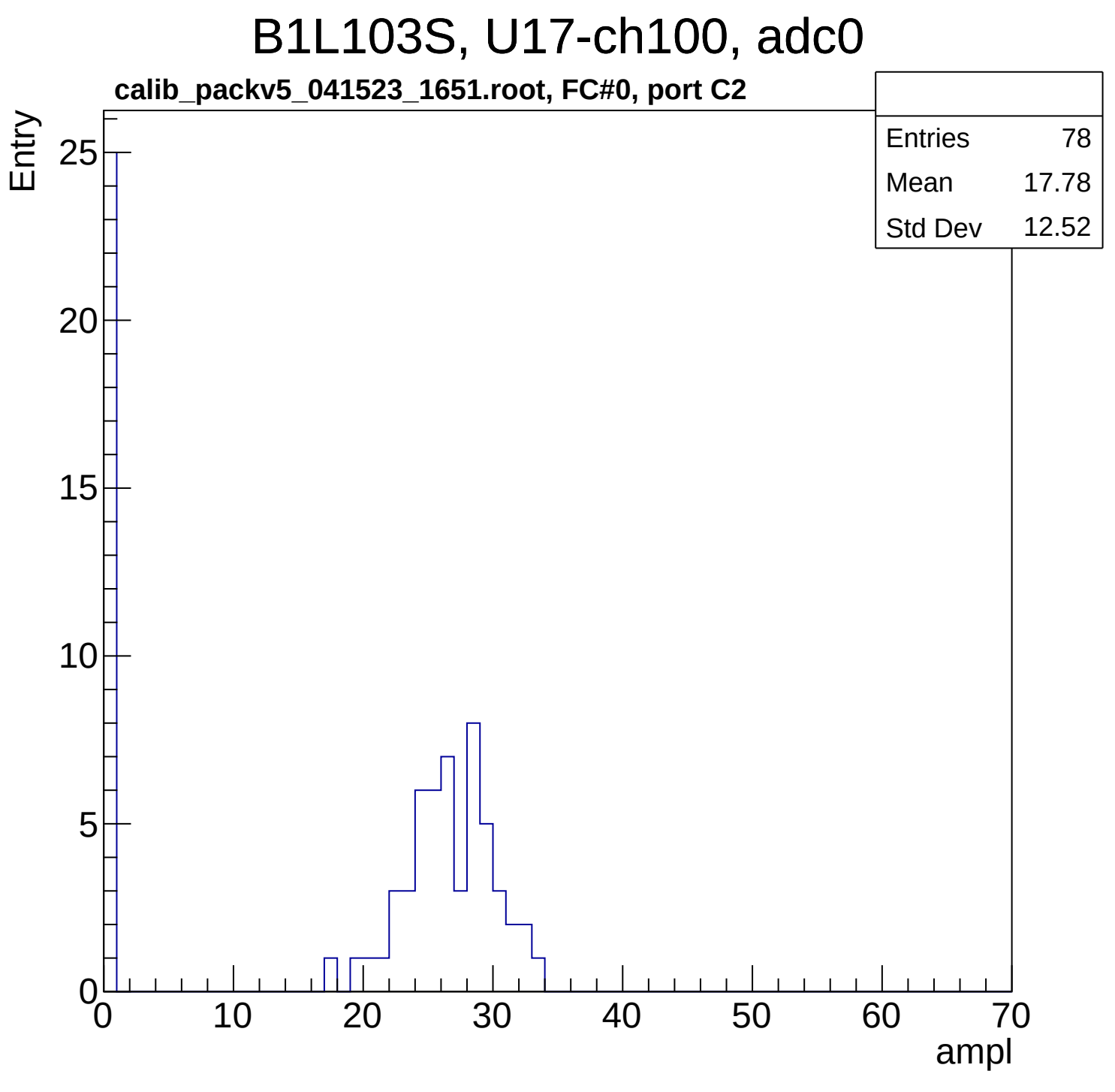
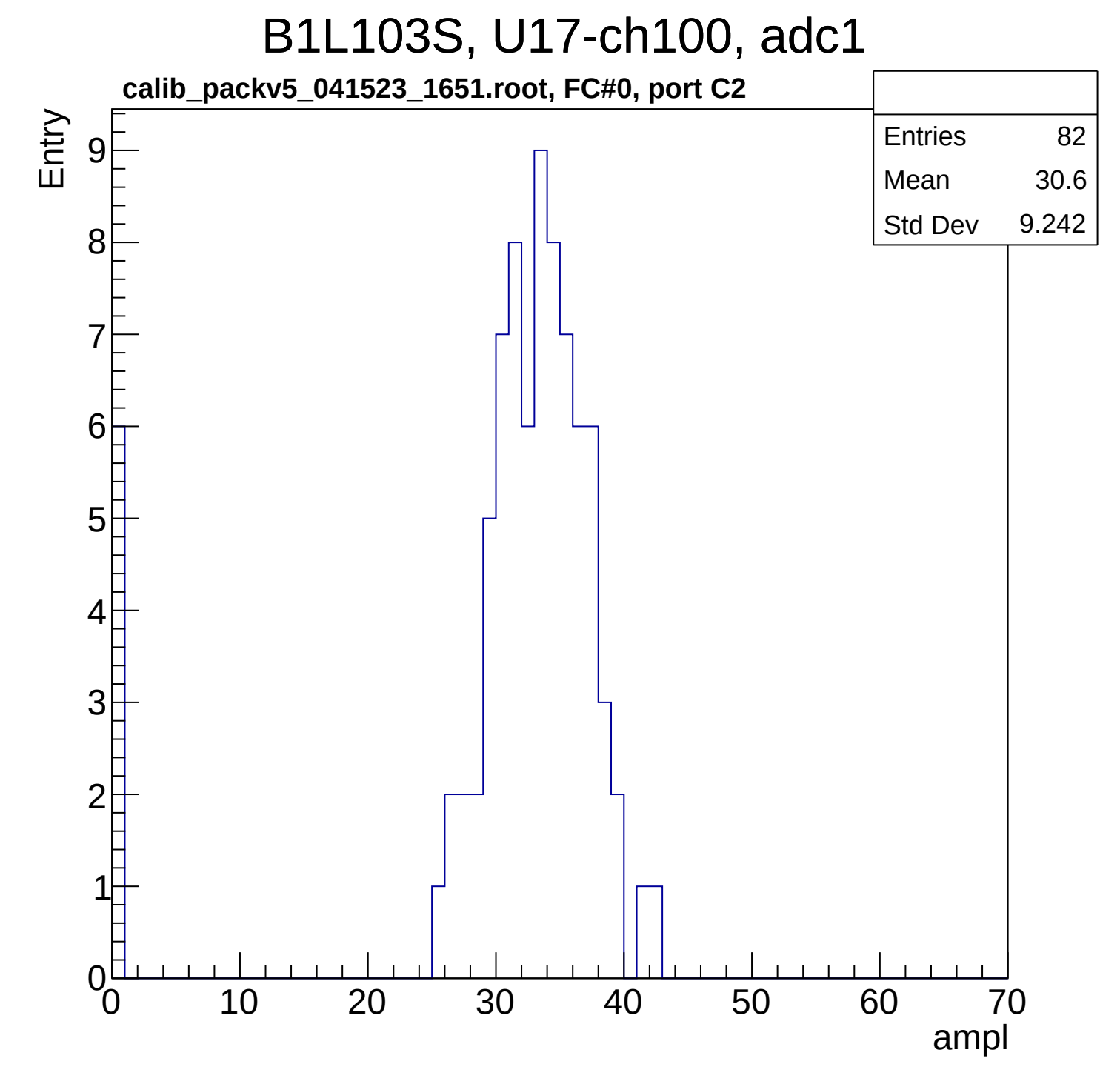
50
60
70
ampl


B1L103S, U17-ch100, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 17.78
Std Dev 12.52
Entry
0
5
10
15
20
25
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch100, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 30.6
Std Dev 9.242
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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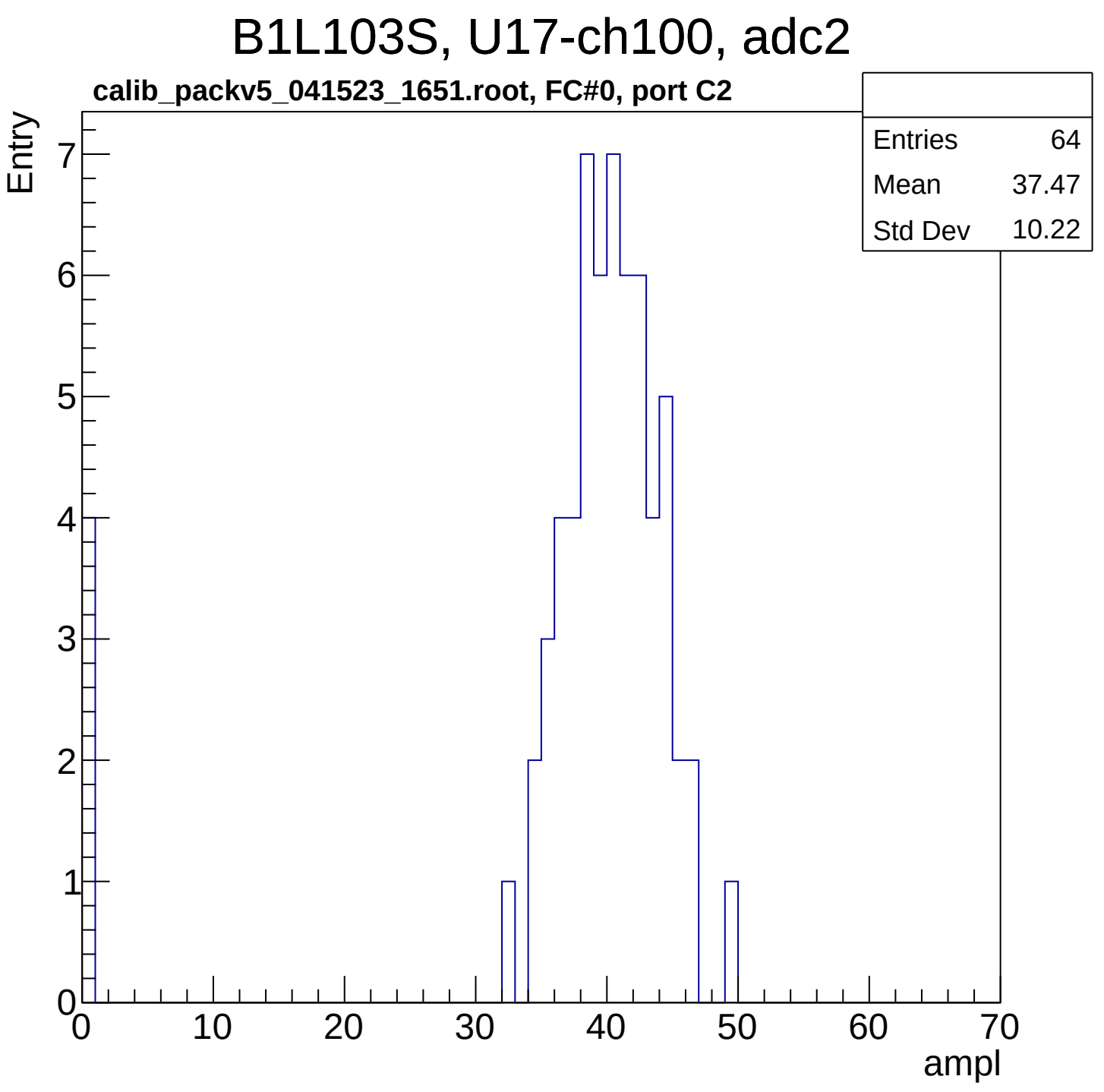
40
50
60
70


B1L103S, U17-ch100, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 37.47
Std Dev 10.22
Entry
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2
3
4
5
6
7
0
10
20
30
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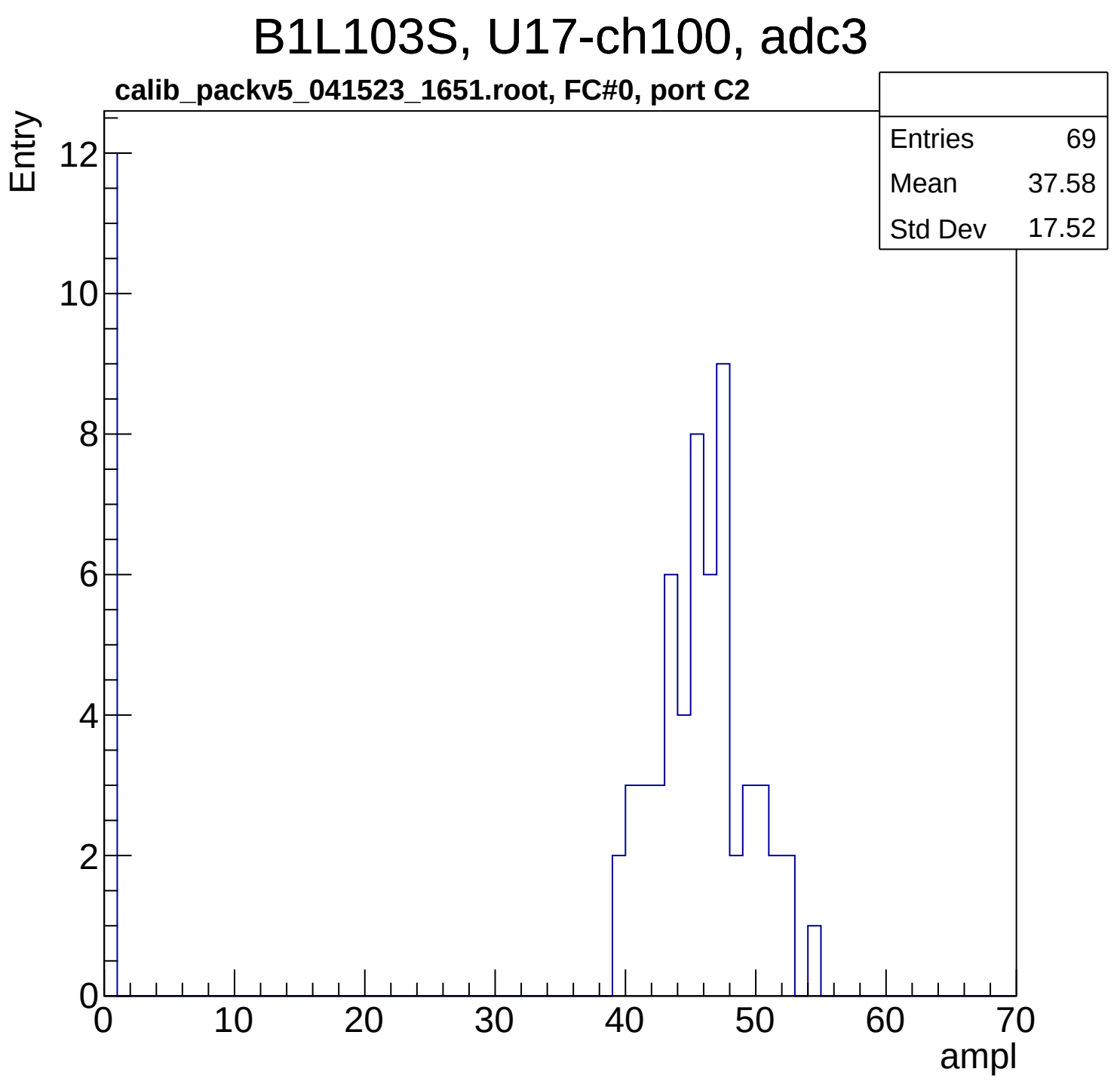
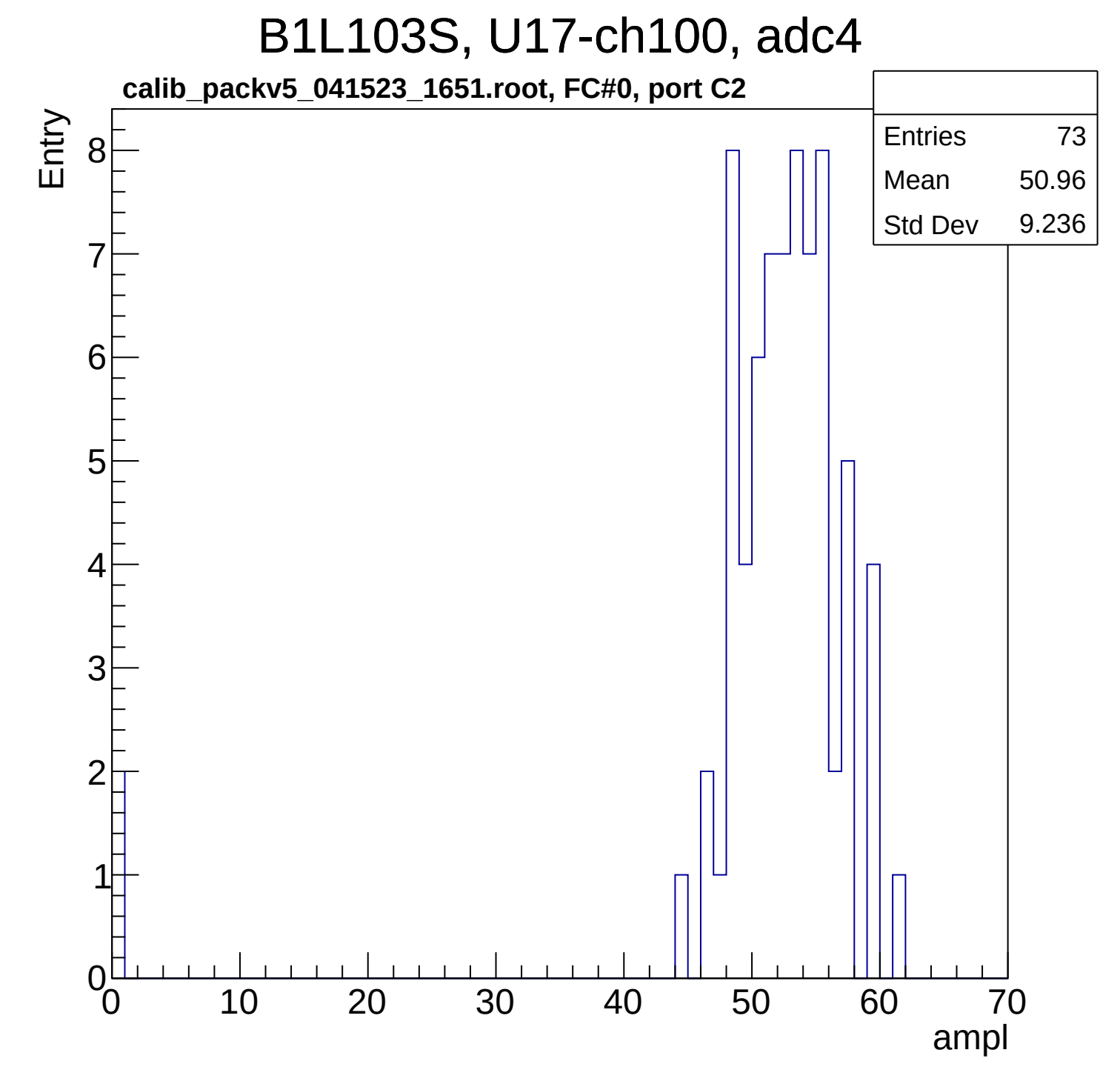
50
60
70
ampl


B1L103S, U17-ch100, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 37.58
Std Dev 17.52
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch100, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 50.96
Std Dev 9.236
Entry
ampl
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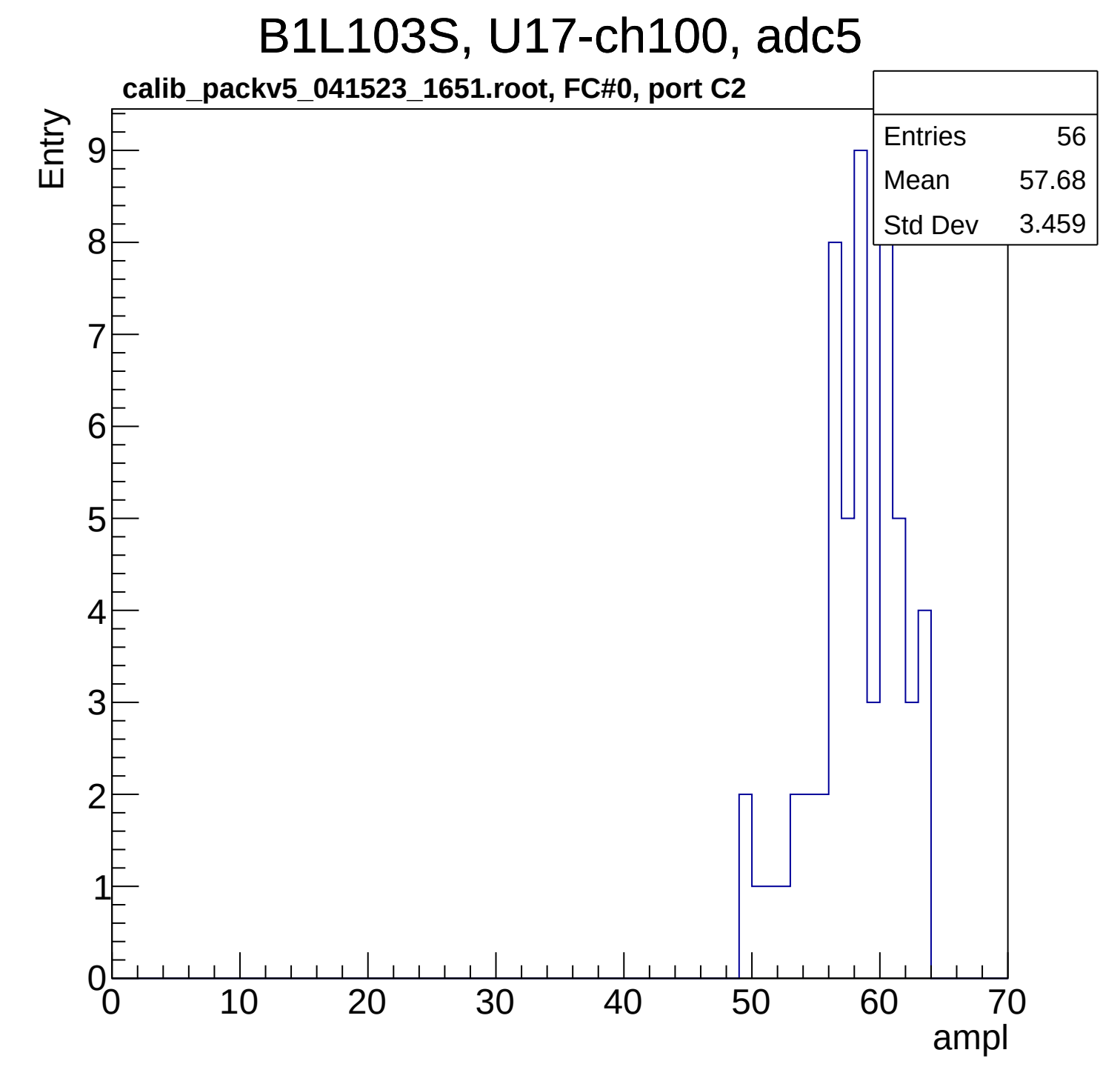
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U17-ch100, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 57.68
Std Dev 3.459
Entry
ampl
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3
4
5
6
7
8
9
0
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60
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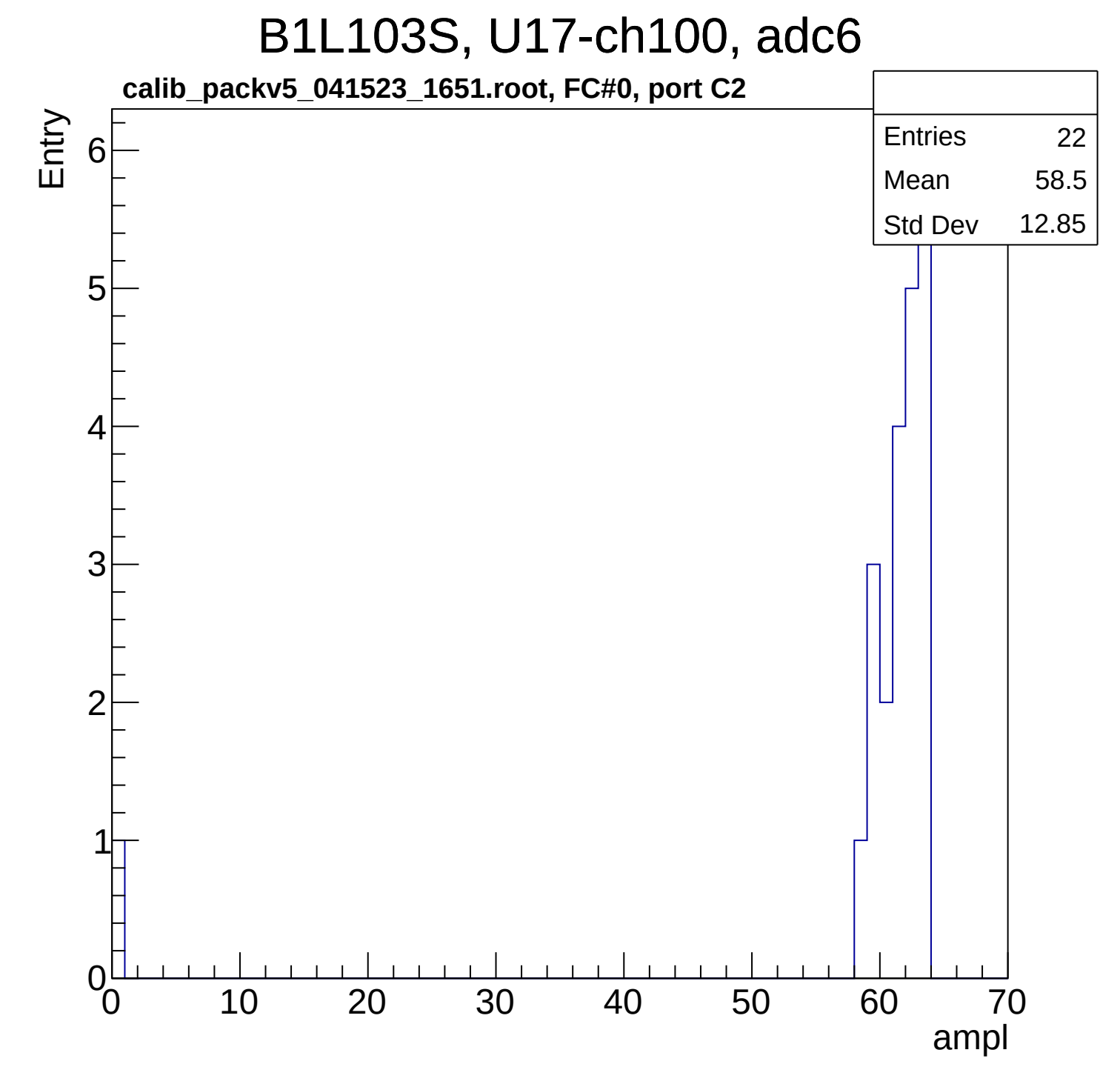
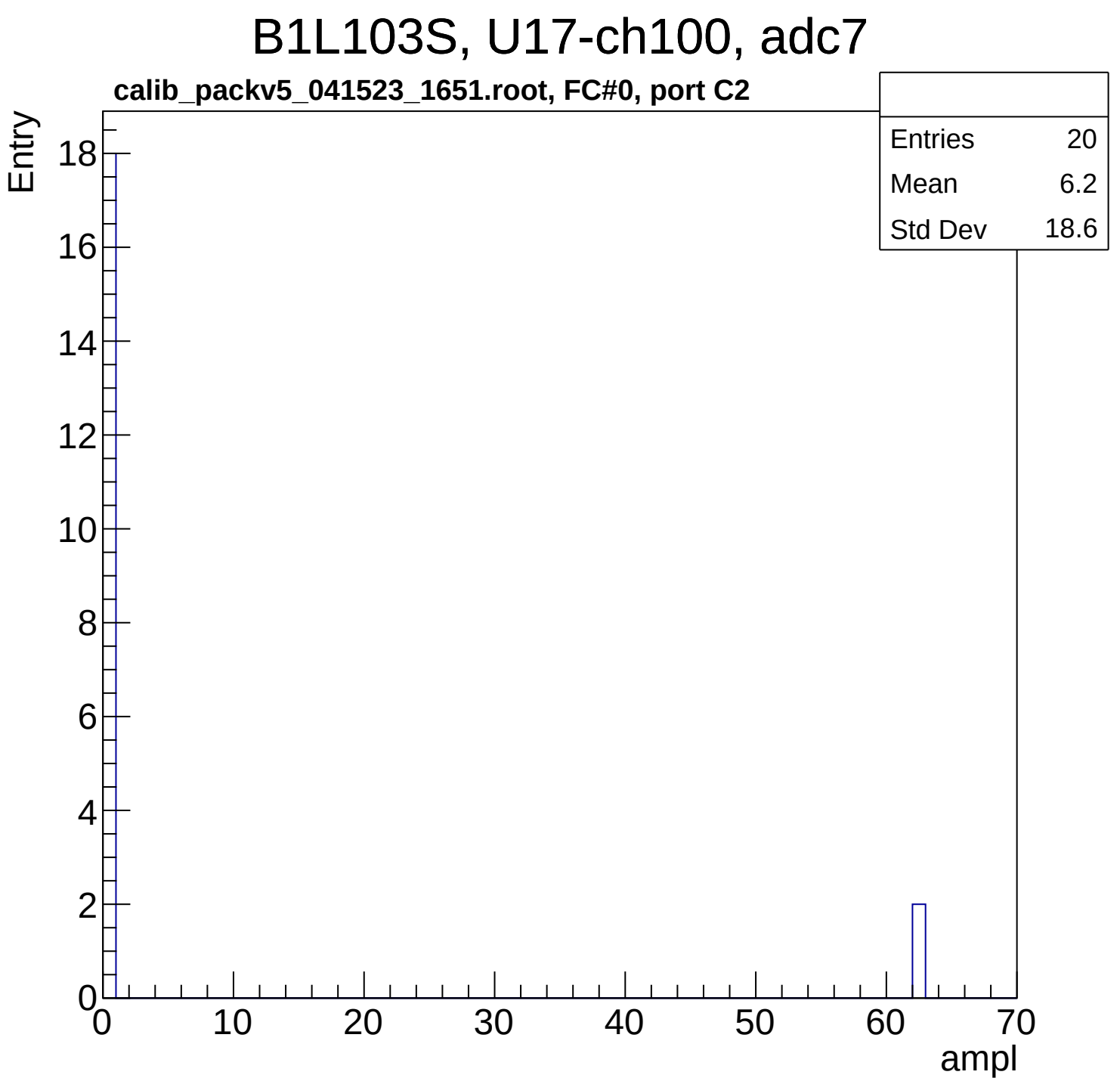
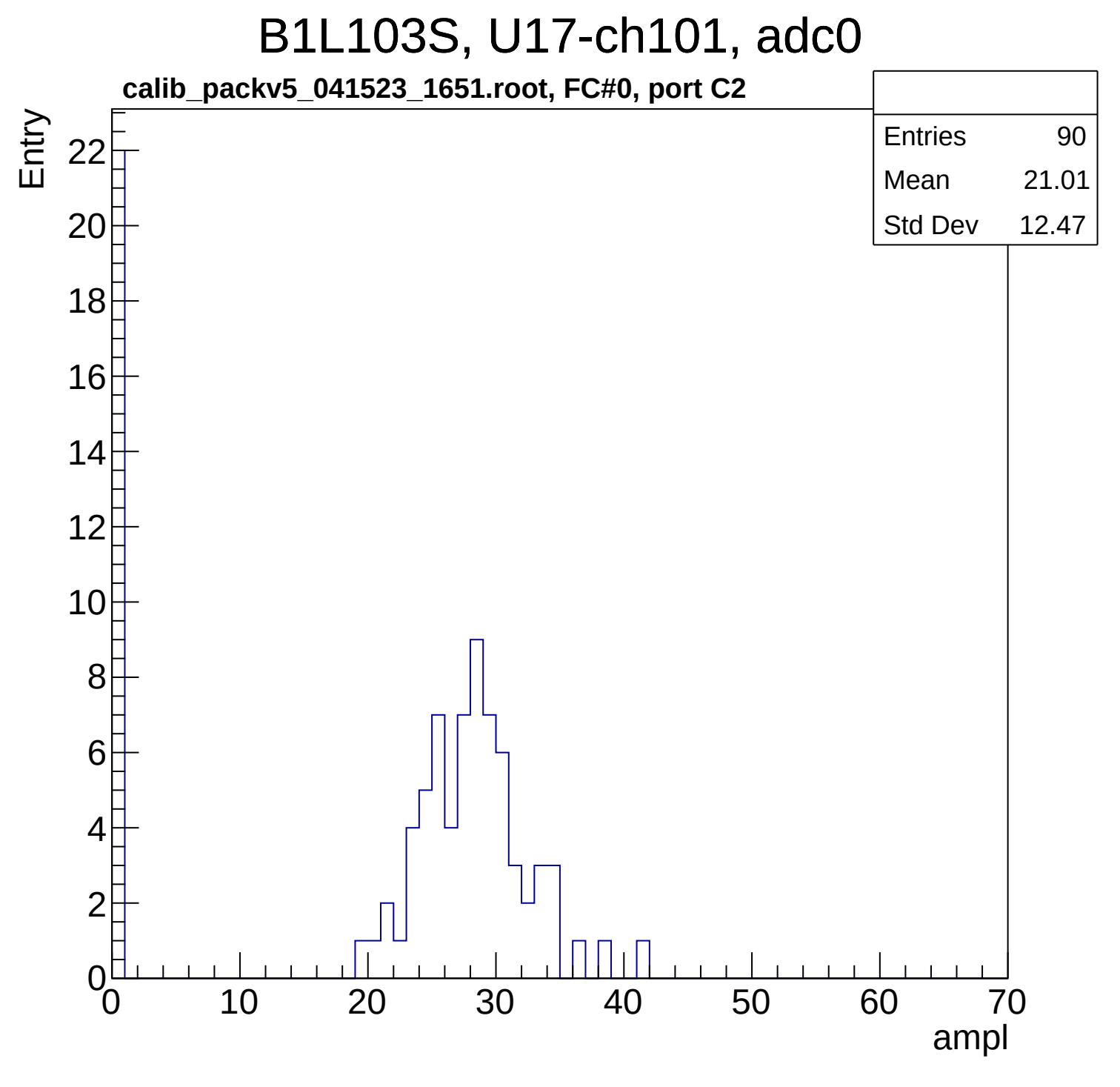

B1L103S, U17-ch100, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 58.5
Std Dev 12.85
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch100, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 6.2
Std Dev 18.6
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch101, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 90
Mean 21.01
Std Dev 12.47
Entry
ampl
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6
8
10
12
14
16
18
20
22
0
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40
50
60
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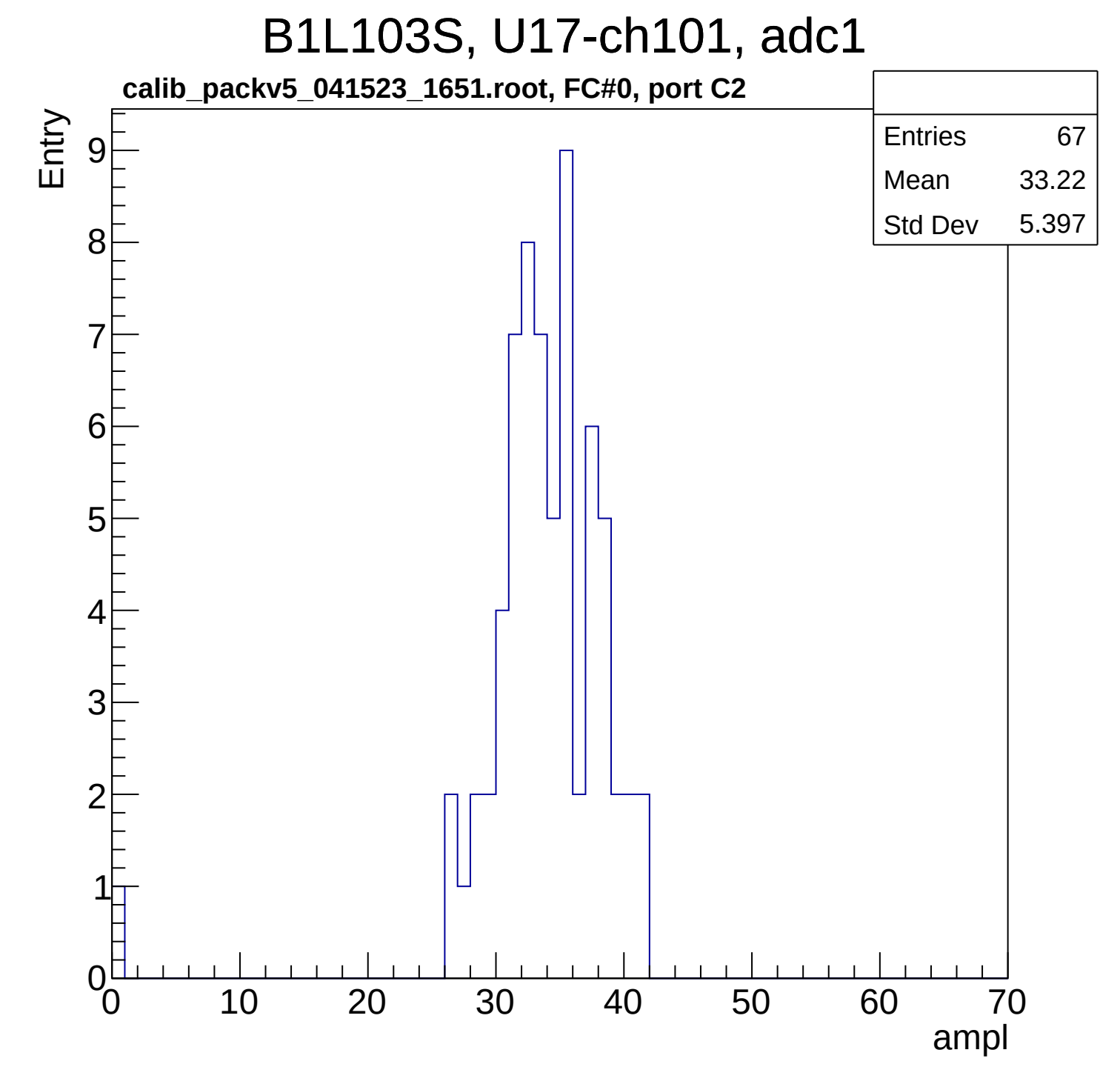
B1L103S, U17-ch101, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 33.22
Std Dev 5.397
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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40
50
60
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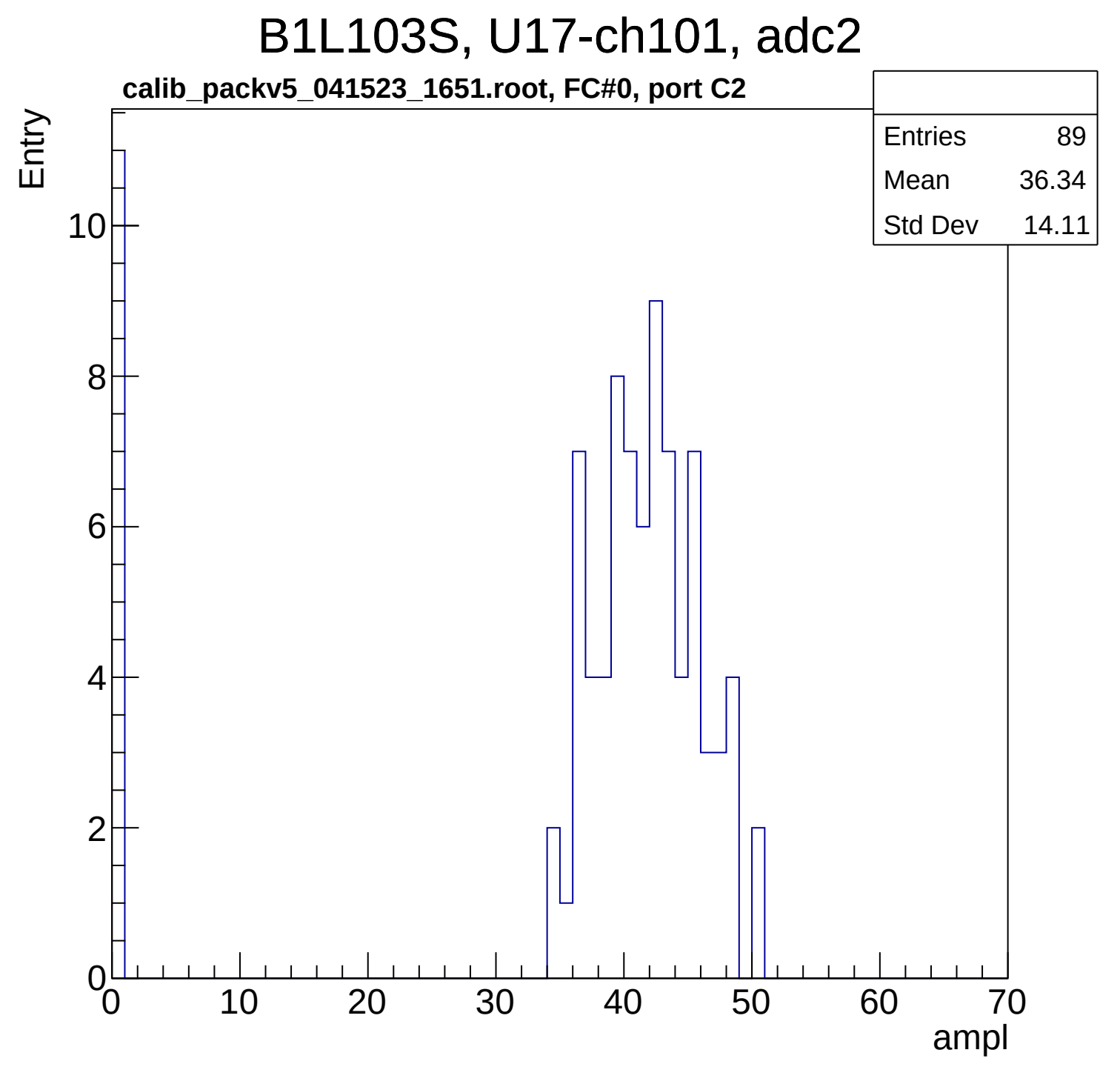
B1L103S, U17-ch101, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 89
Mean 36.34
Std Dev 14.11
Entry
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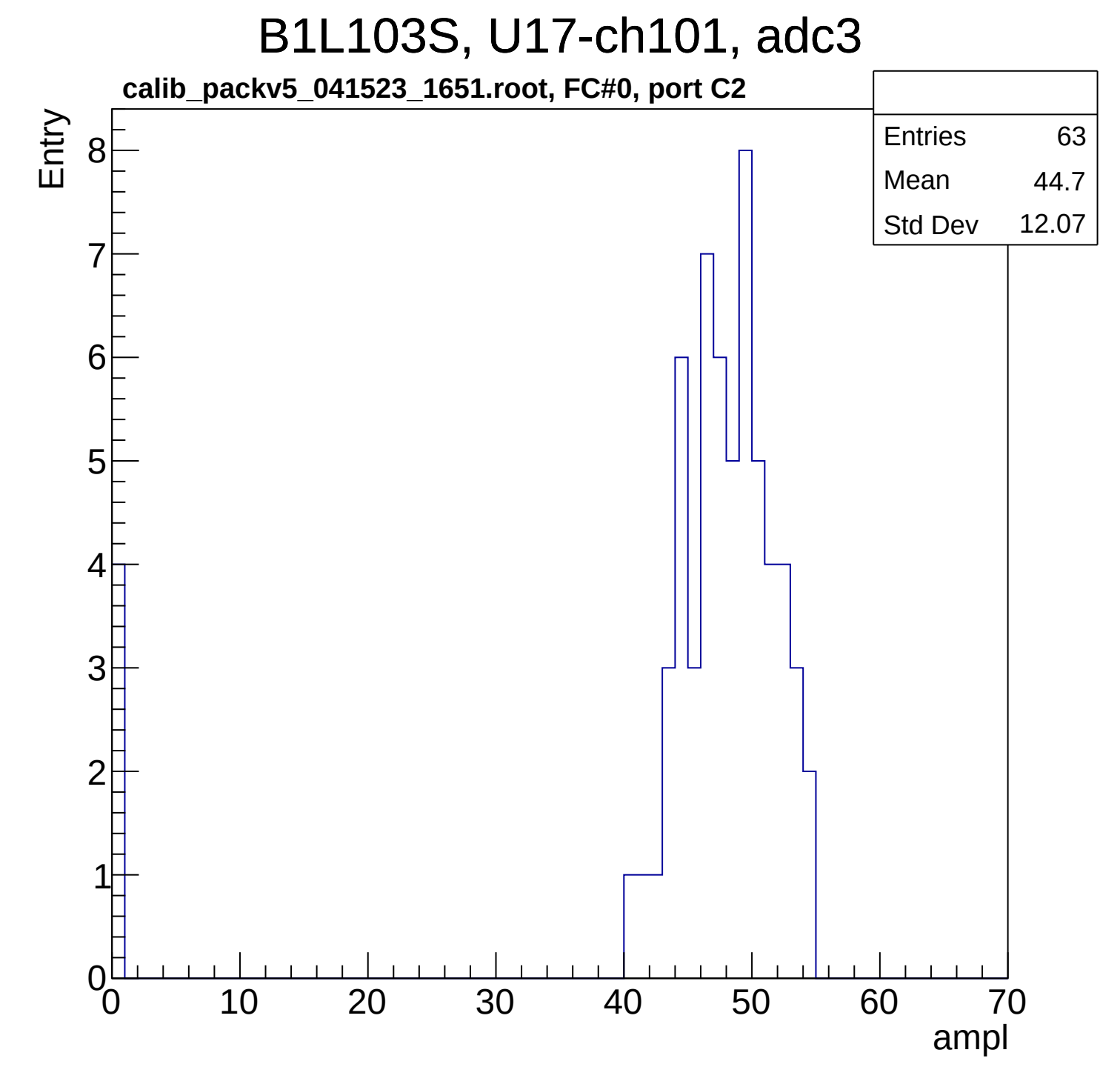
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch101, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 44.7
Std Dev 12.07
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
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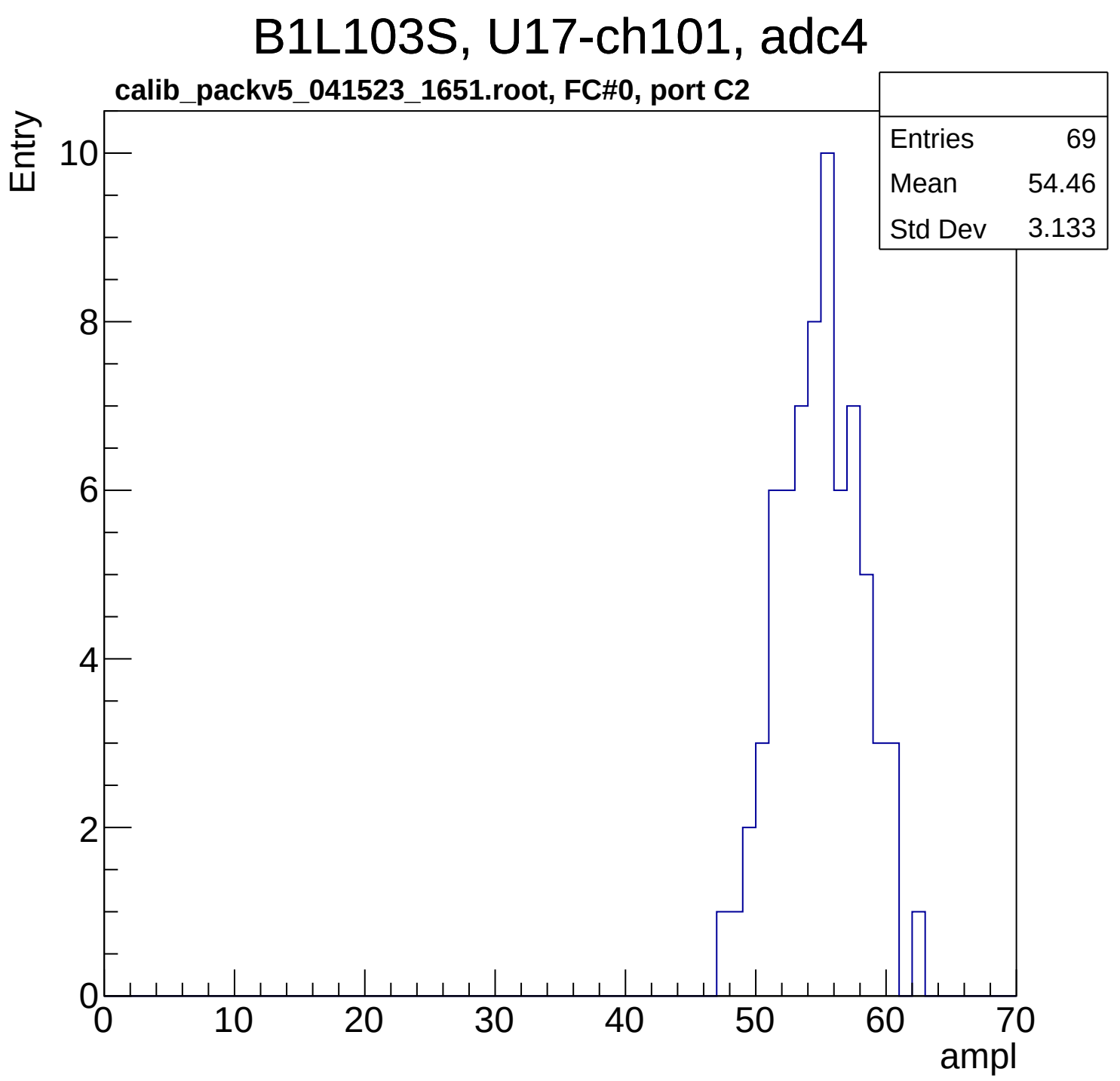
40
50
60
70


B1L103S, U17-ch101, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 54.46
Std Dev 3.133
Entry
ampl
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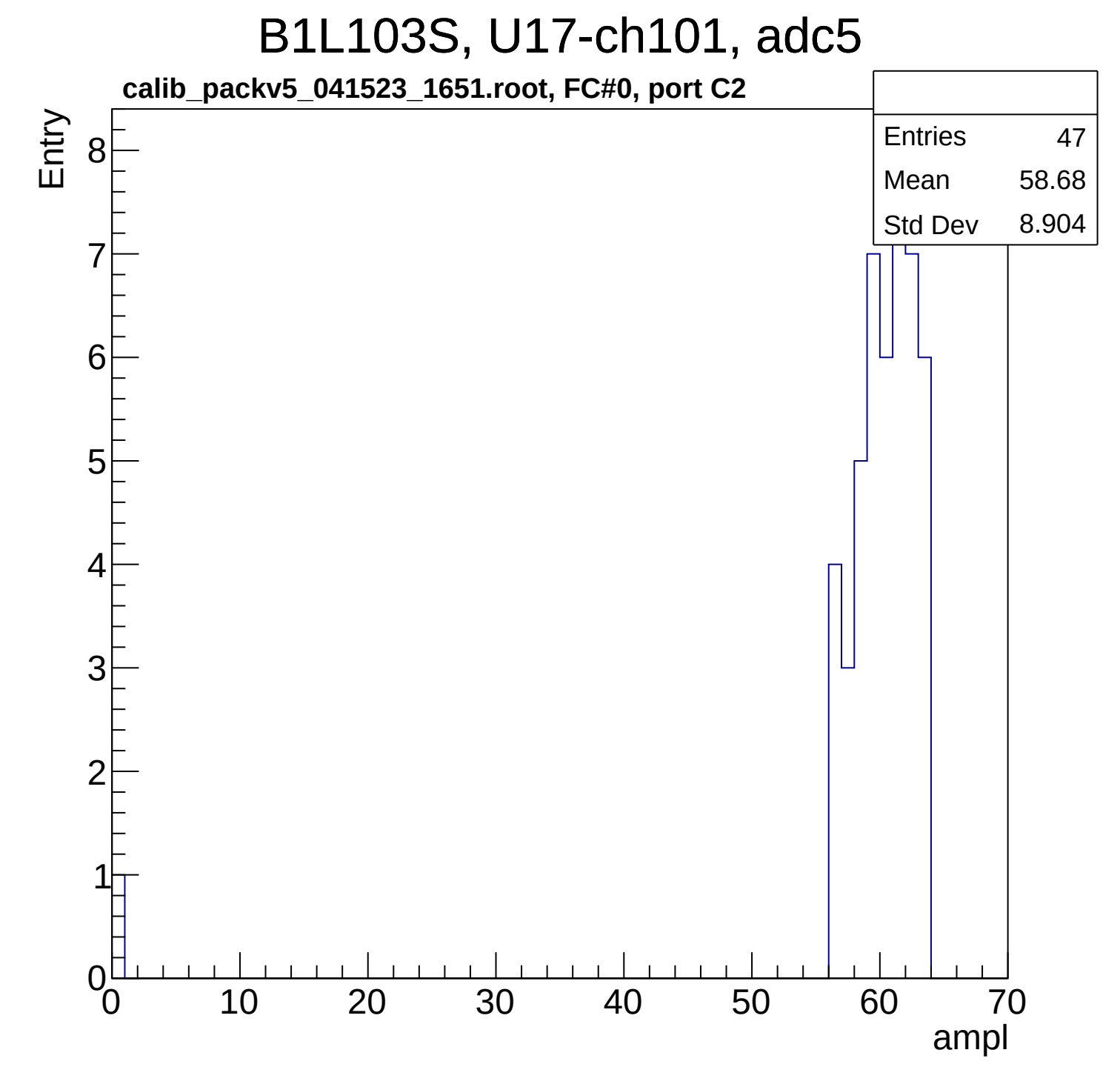
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U17-ch101, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 58.68
Std Dev 8.904
Entry
ampl
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2
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4
5
6
7
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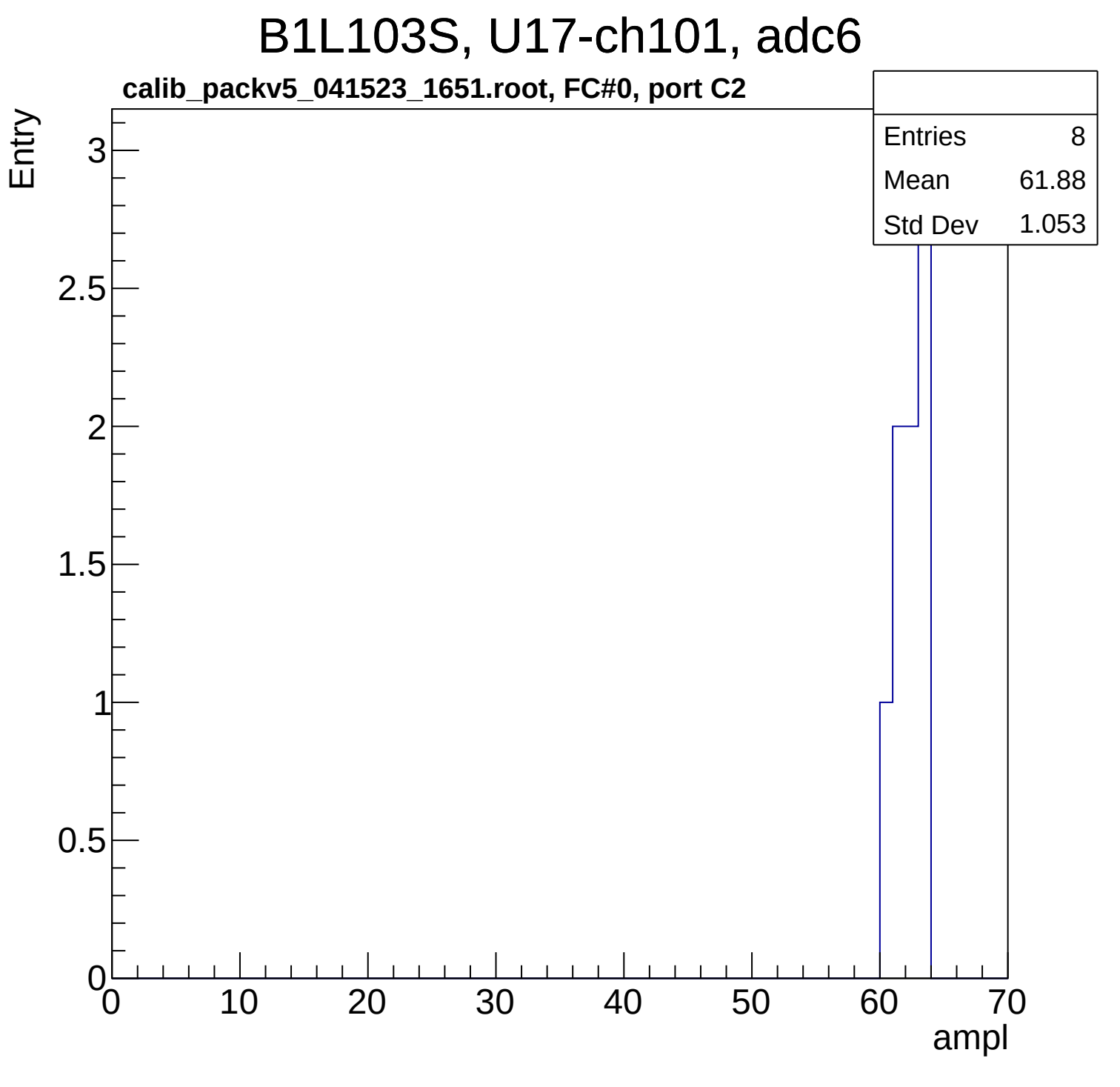
0
10
20
30
40
50
60
70


B1L103S, U17-ch101, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 61.88
Std Dev 1.053
Entry
ampl
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0.5
1
1.5
2
2.5
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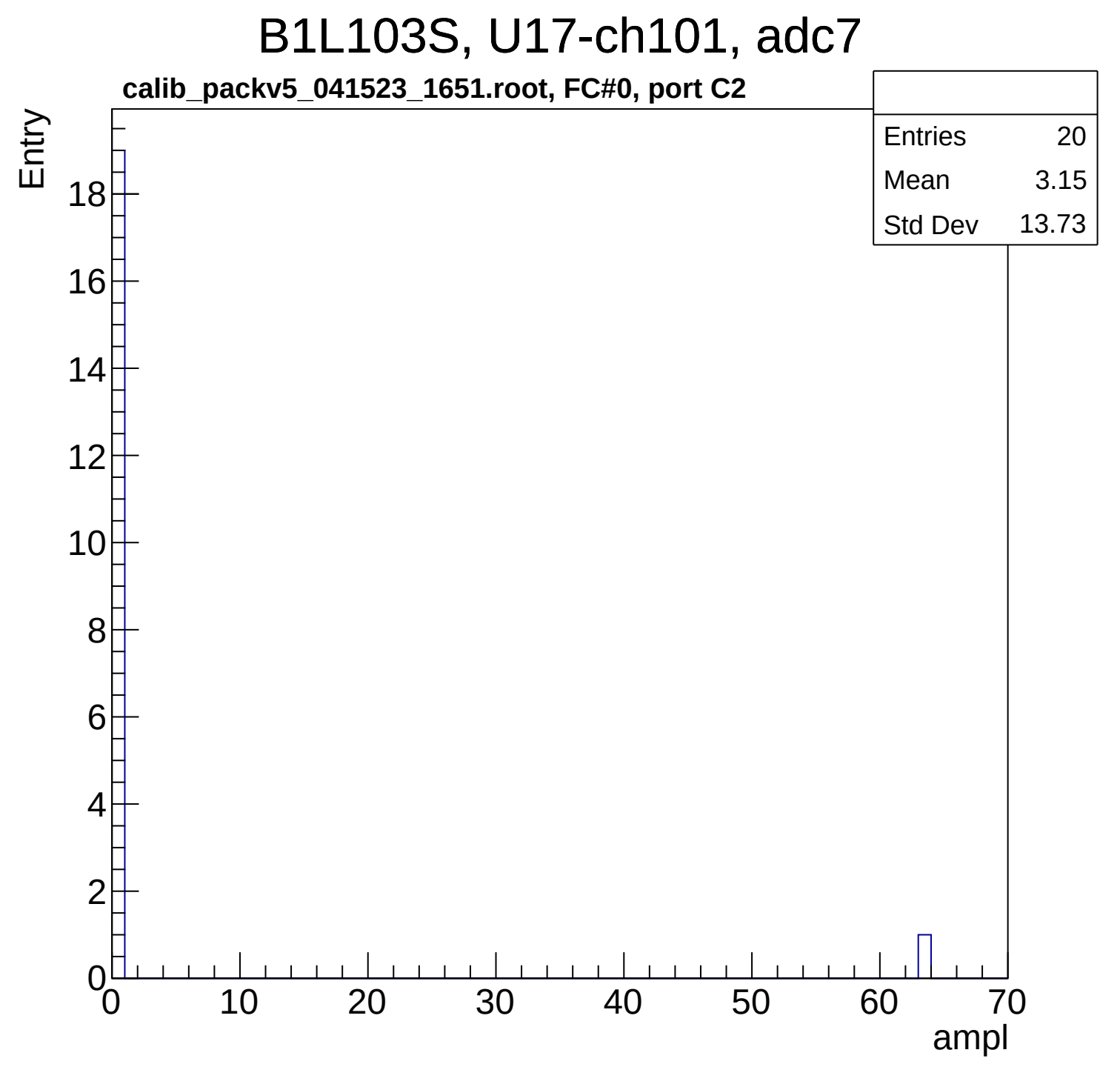
0
10
20
30
40
50
60
70


B1L103S, U17-ch101, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
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6
8
10
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14
16
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10
20
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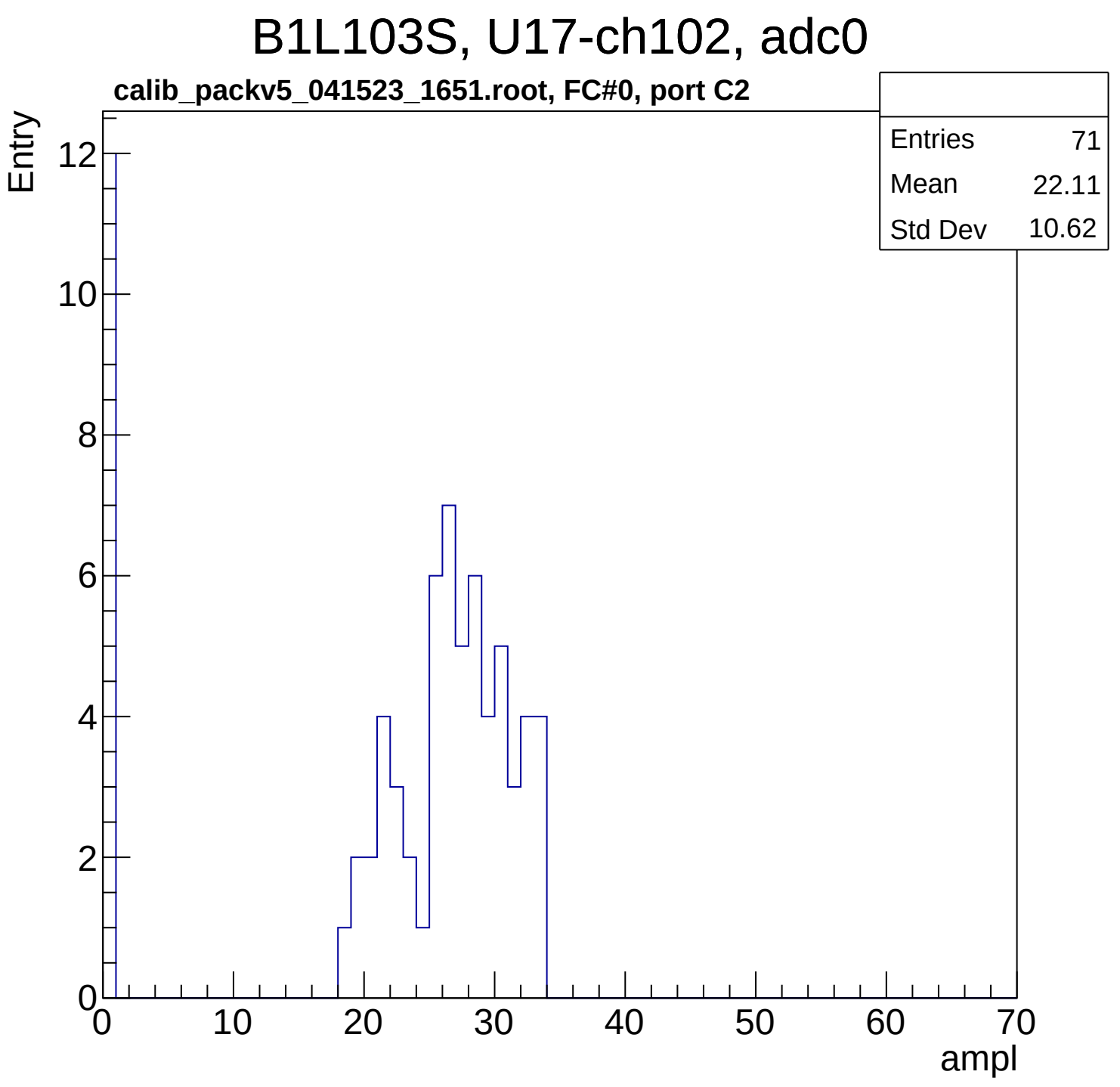
50
60
70
ampl


B1L103S, U17-ch102, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 22.11
Std Dev 10.62
Entry
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6
8
10
12
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10
20
30
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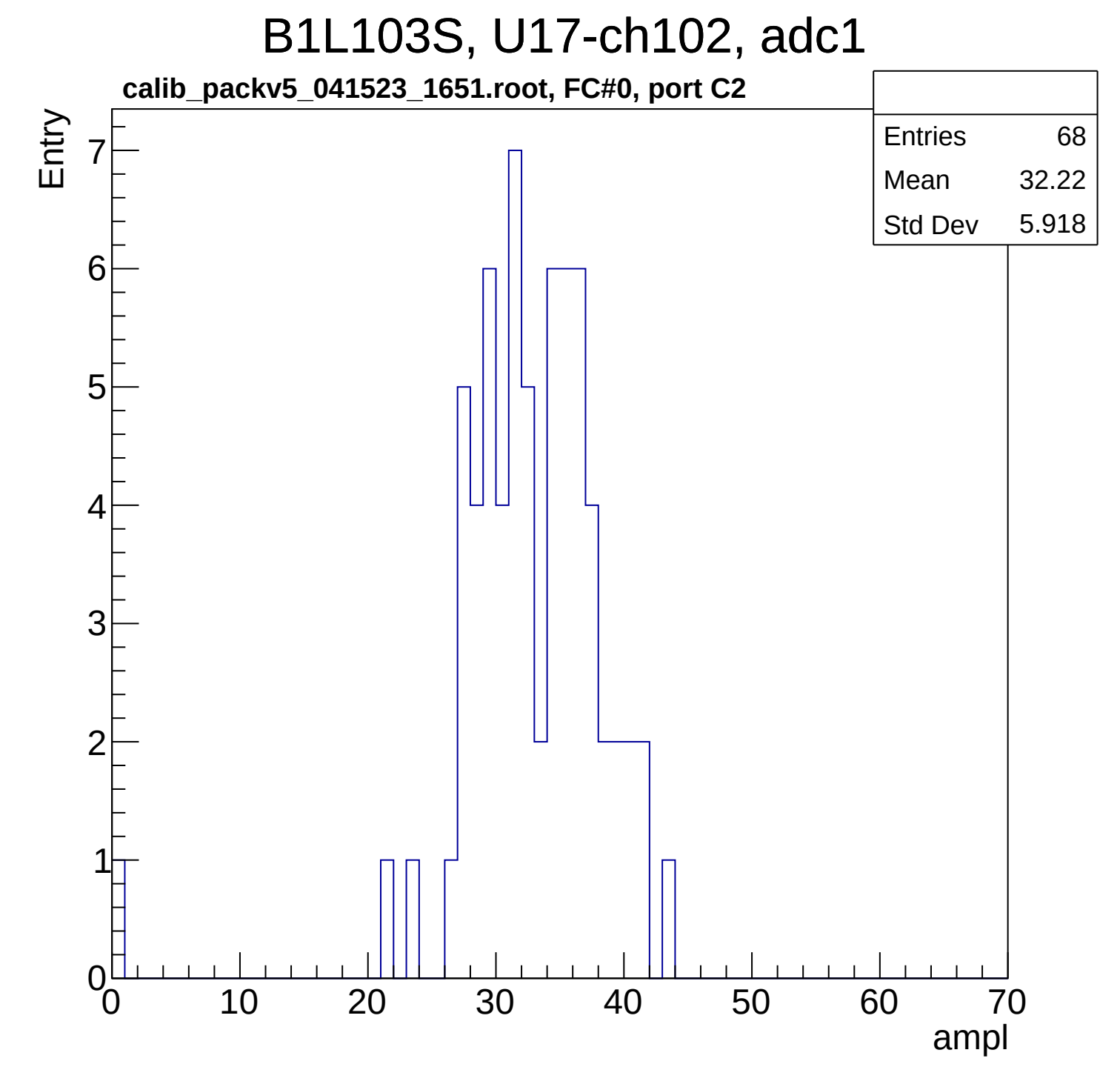
50
60
70
ampl


B1L103S, U17-ch102, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 32.22
Std Dev 5.918
Entry
ampl
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1
2
3
4
5
6
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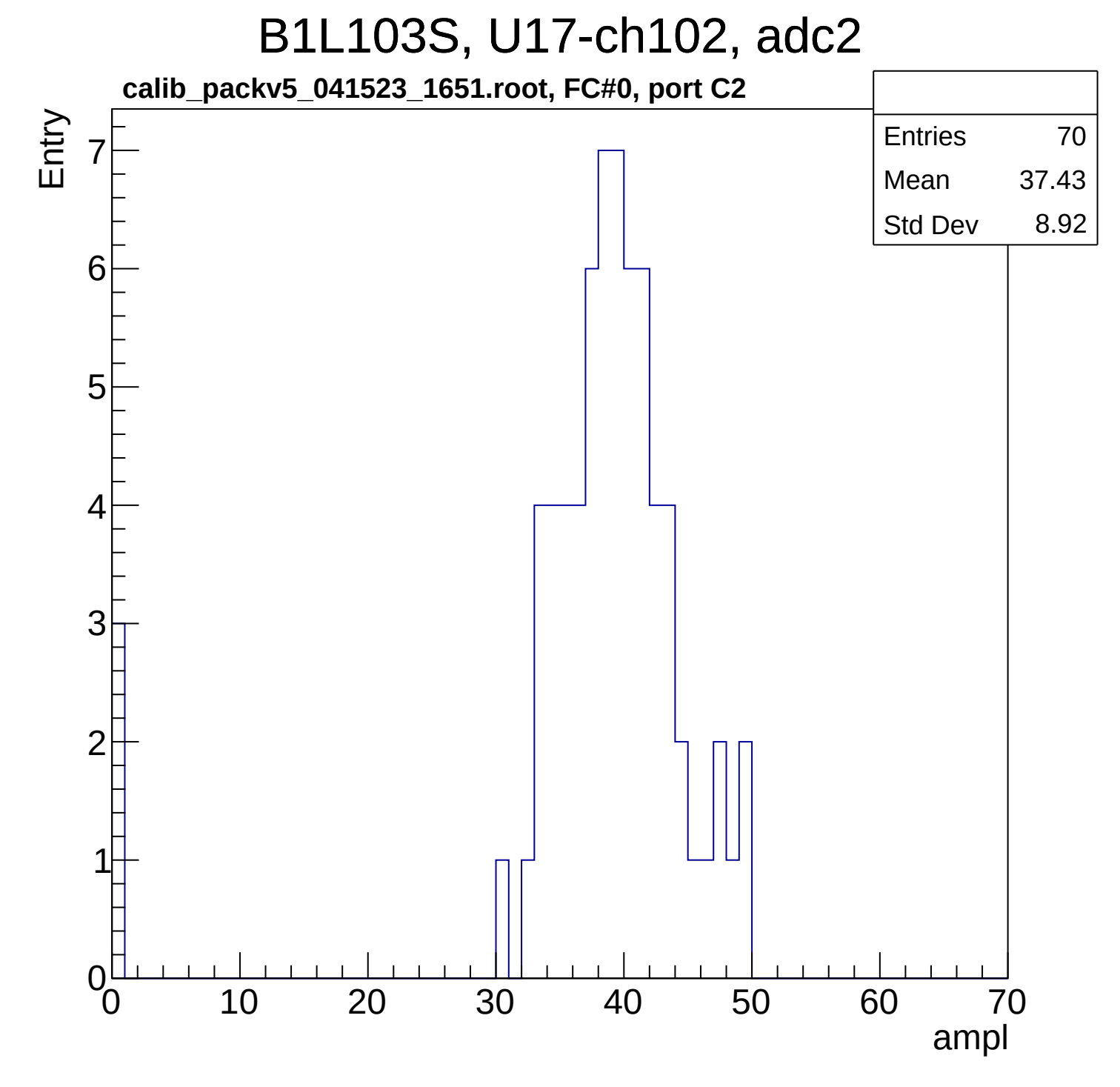
0
10
20
30
40
50
60
70


B1L103S, U17-ch102, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 37.43
Std Dev 8.92
Entry
ampl
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1
2
3
4
5
6
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0
10
20
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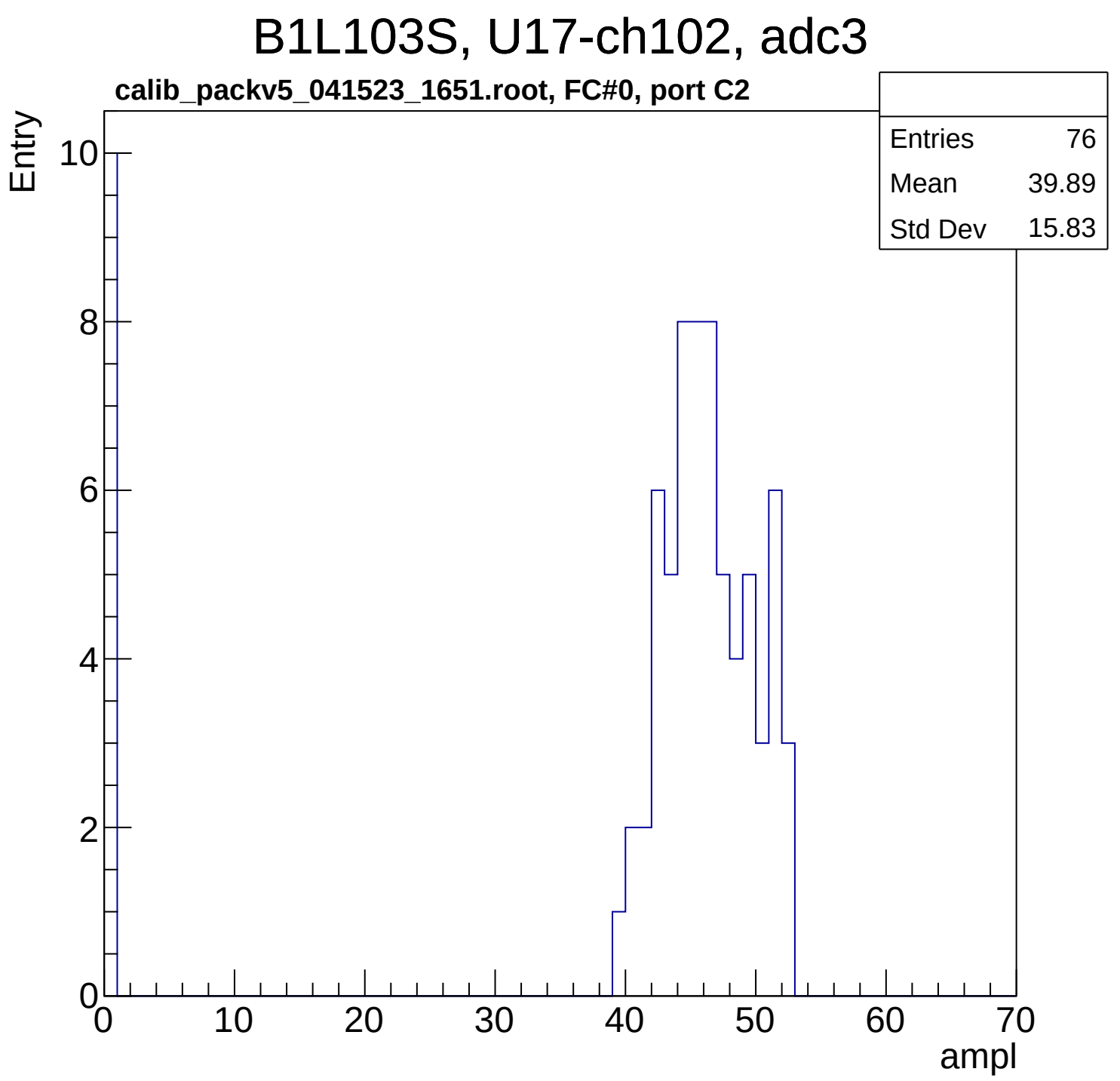
40
50
60
70


B1L103S, U17-ch102, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 39.89
Std Dev 15.83
Entry
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2
4
6
8
10
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10
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30
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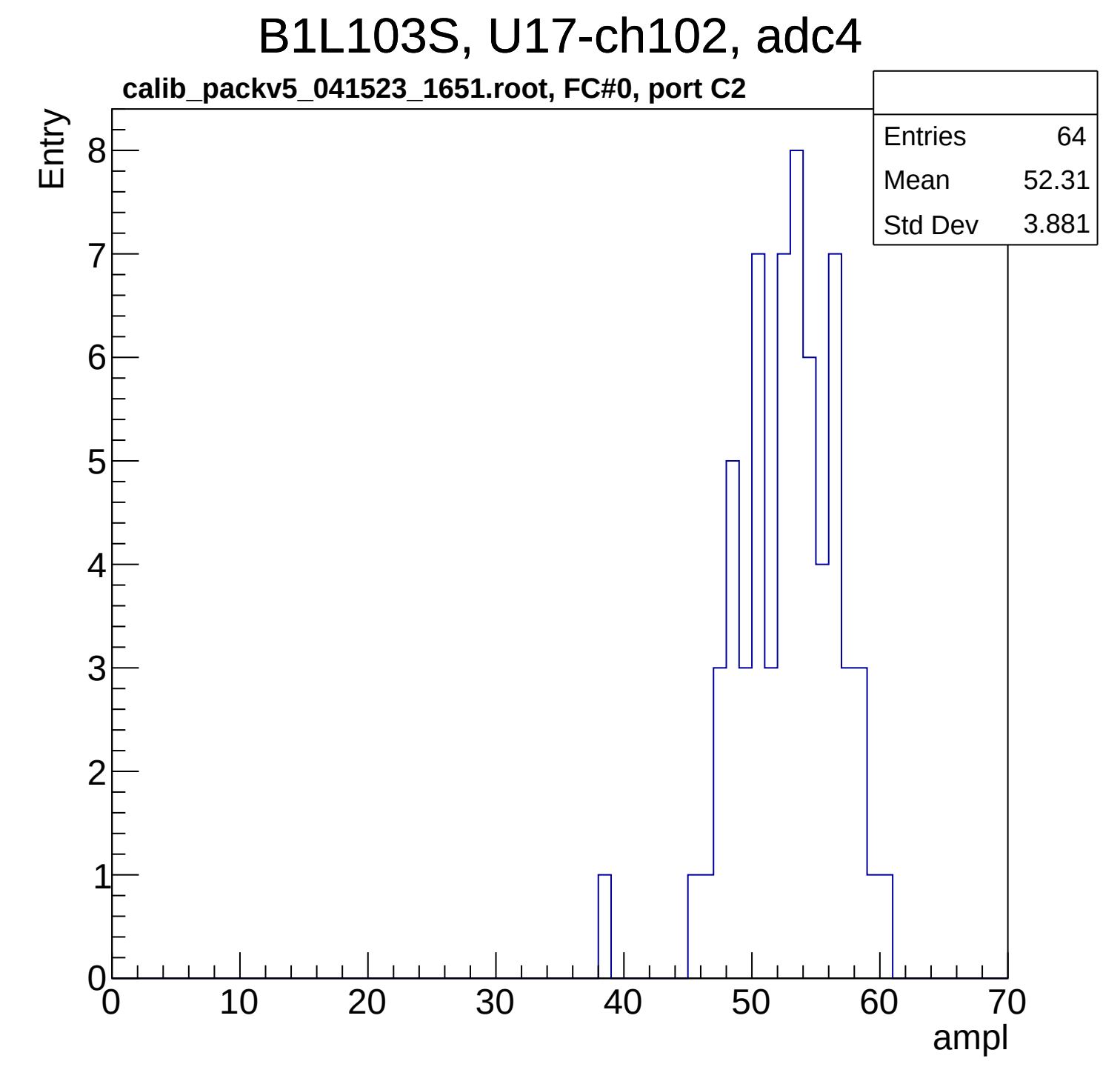
50
60
70
ampl


B1L103S, U17-ch102, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 52.31
Std Dev 3.881
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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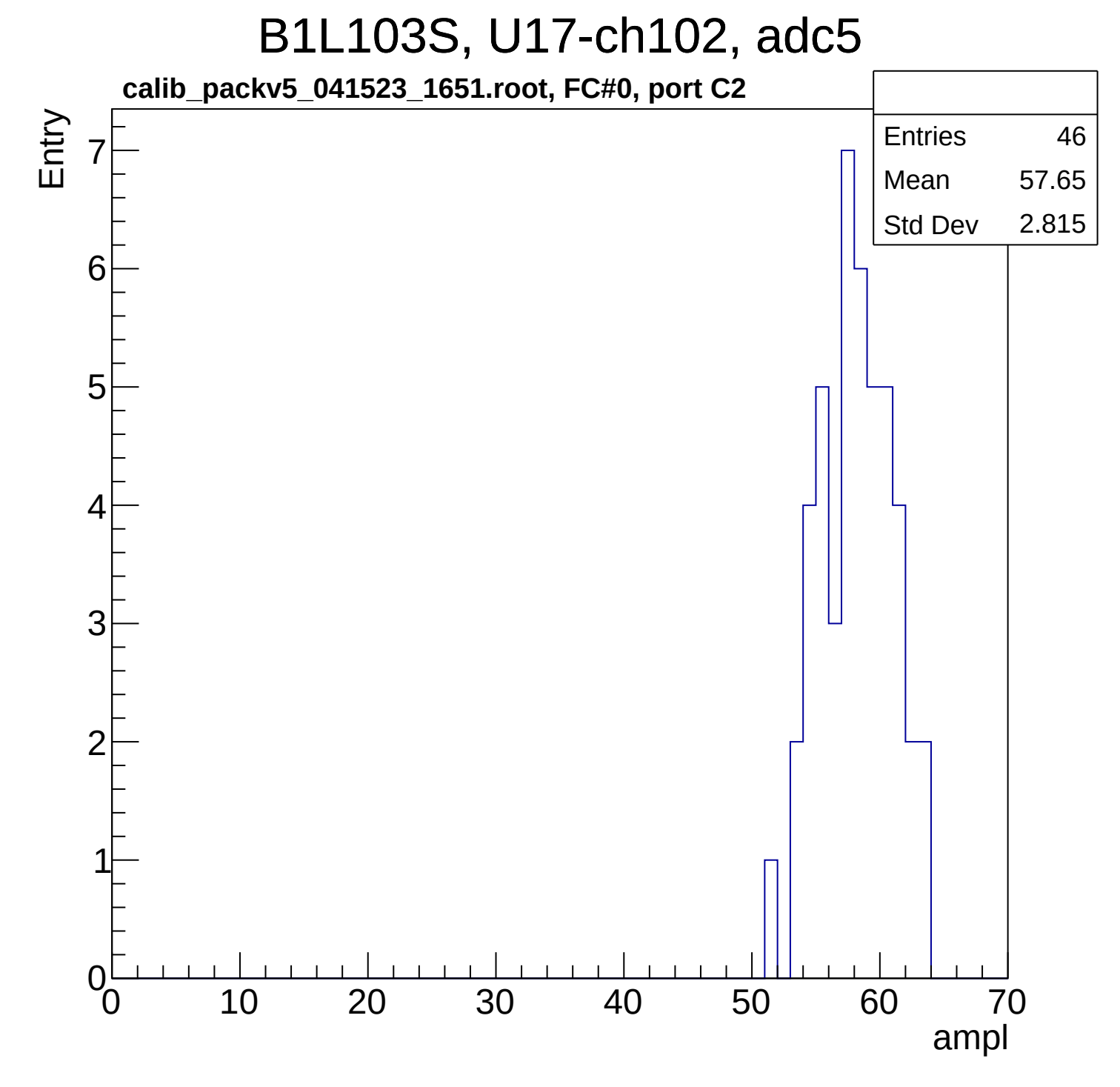
40
50
60
70


B1L103S, U17-ch102, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 57.65
Std Dev 2.815
Entry
ampl
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1
2
3
4
5
6
7
0
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60
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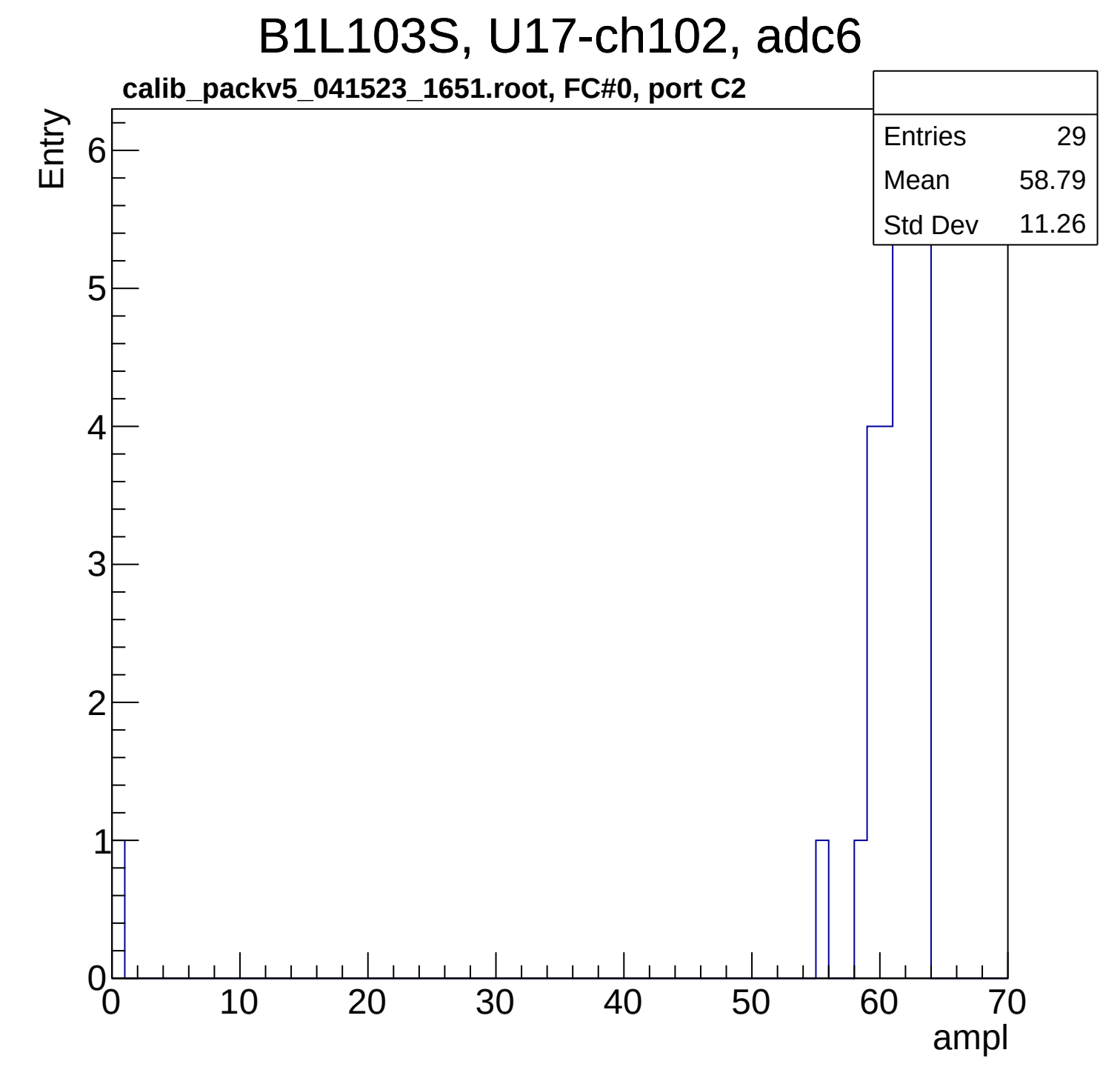
B1L103S, U17-ch102, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 29
Mean 58.79
Std Dev 11.26
Entry
ampl
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3
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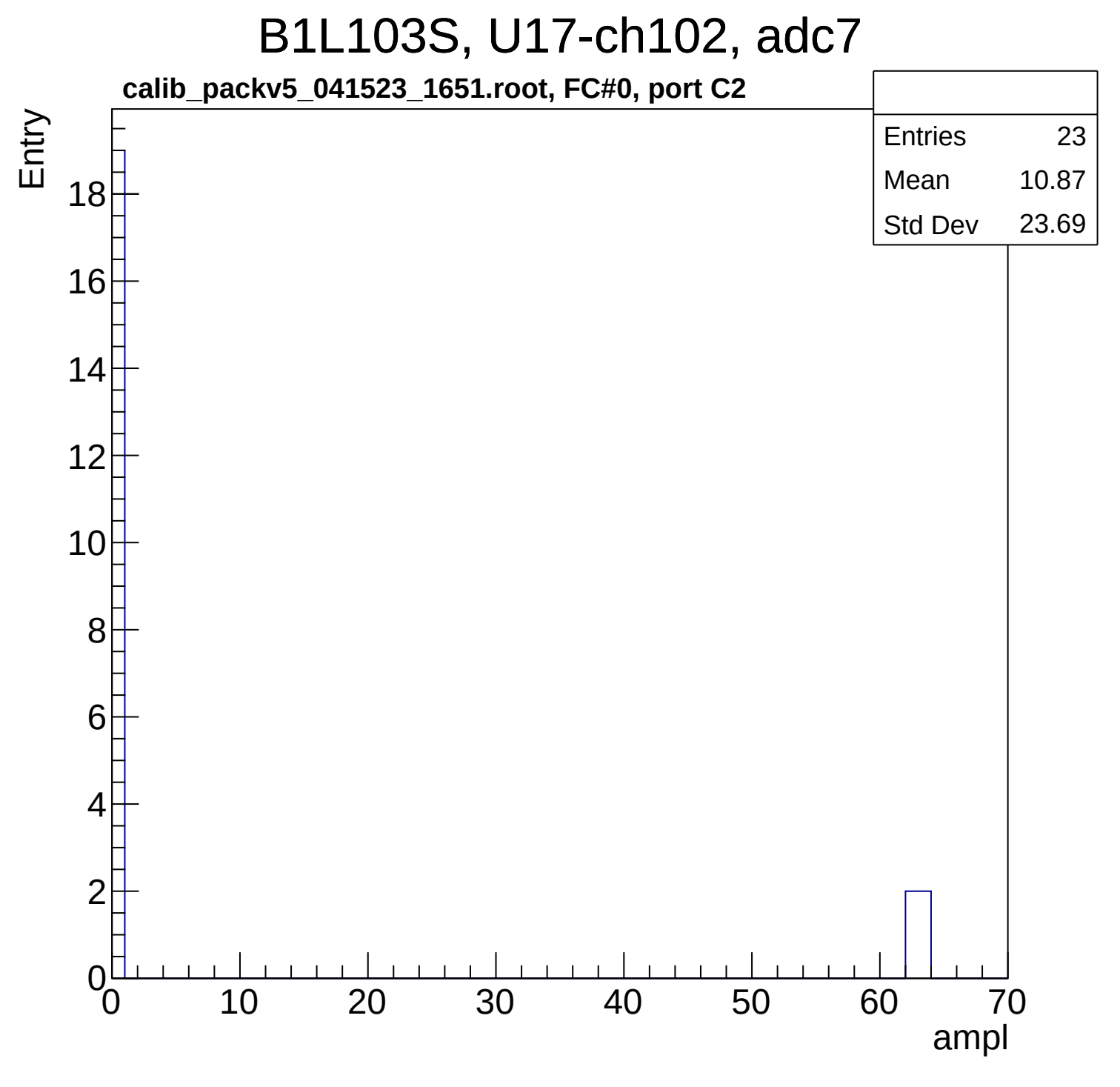
B1L103S, U17-ch102, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 23
Mean 10.87
Std Dev 23.69
Entry
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6
8
10
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14
16
18
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10
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30
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50
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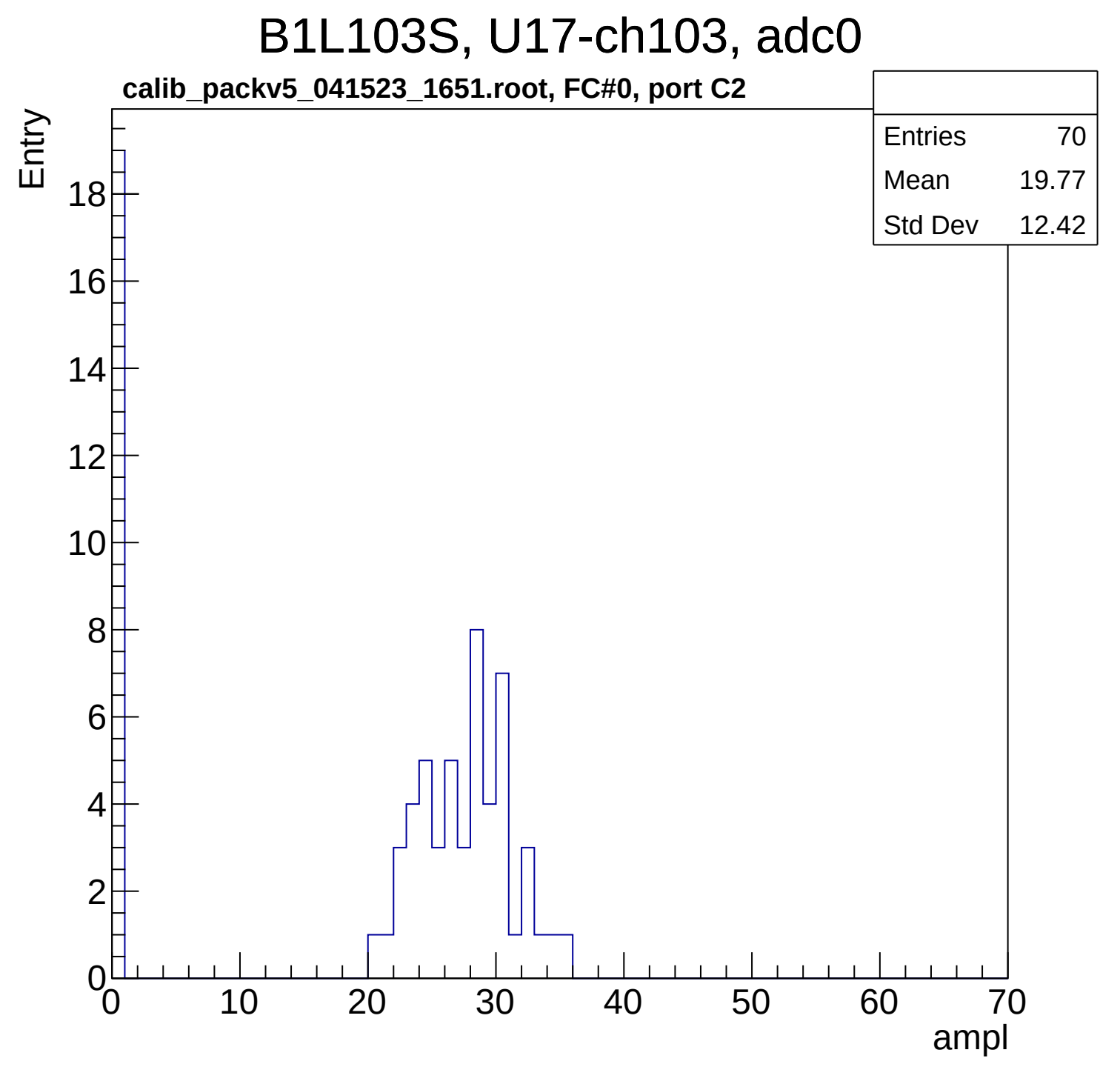
70
ampl


B1L103S, U17-ch103, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 19.77
Std Dev 12.42
Entry
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6
8
10
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14
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50
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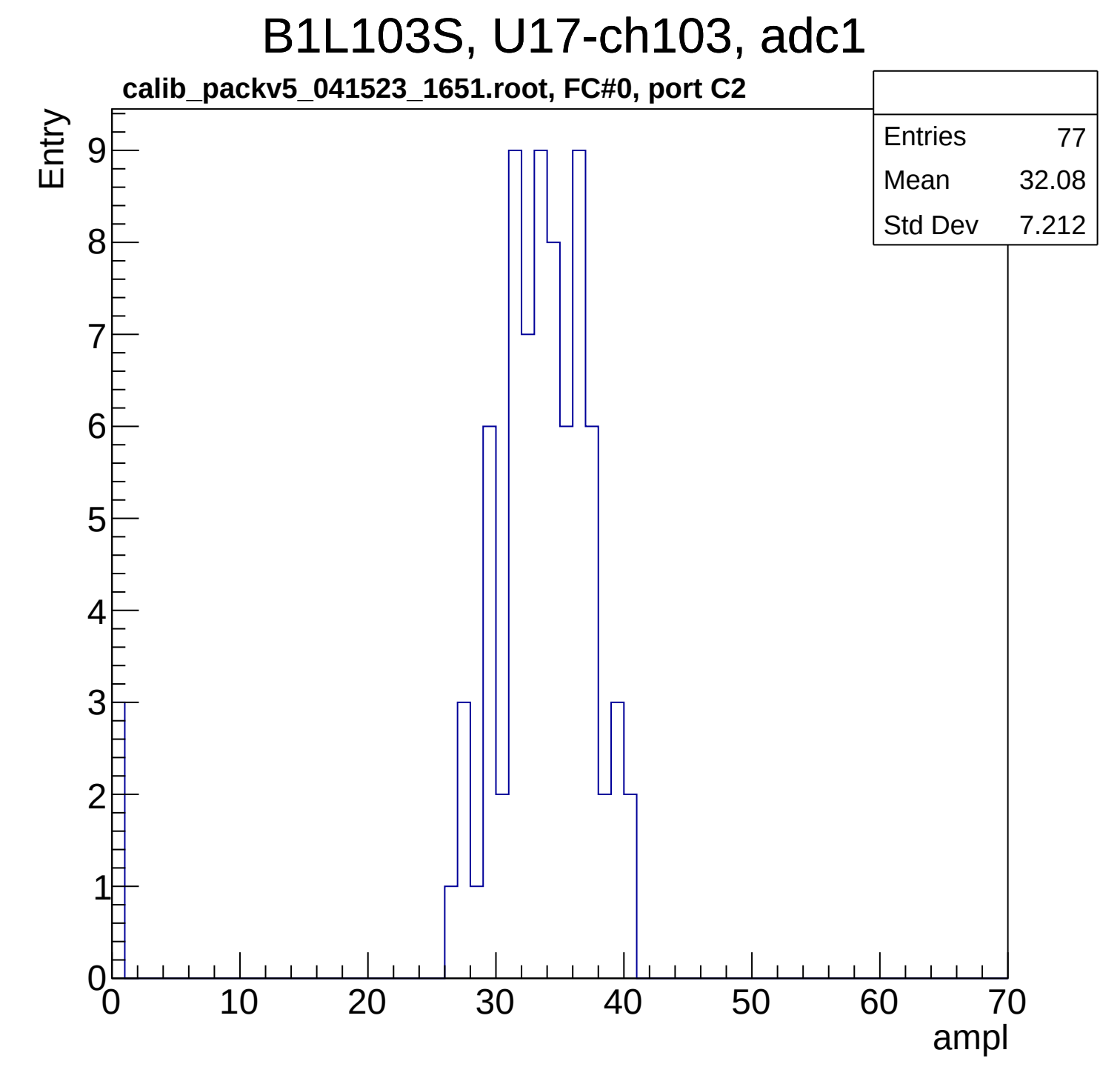
70
ampl


B1L103S, U17-ch103, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 32.08
Std Dev 7.212
Entry
ampl
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4
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6
7
8
9
0
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60
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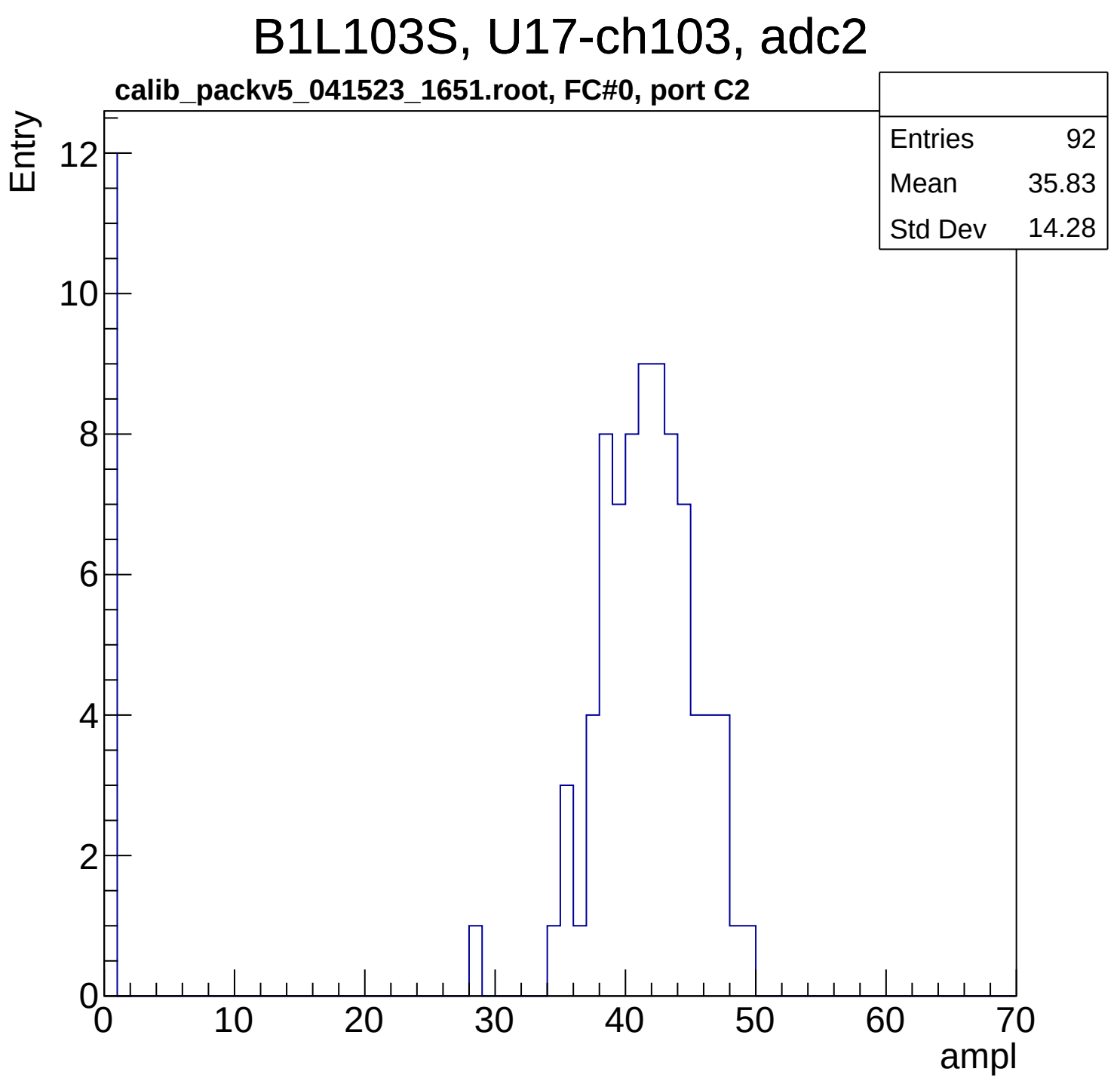
B1L103S, U17-ch103, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 92
Mean 35.83
Std Dev 14.28
Entry
0
2
4
6
8
10
12
0
10
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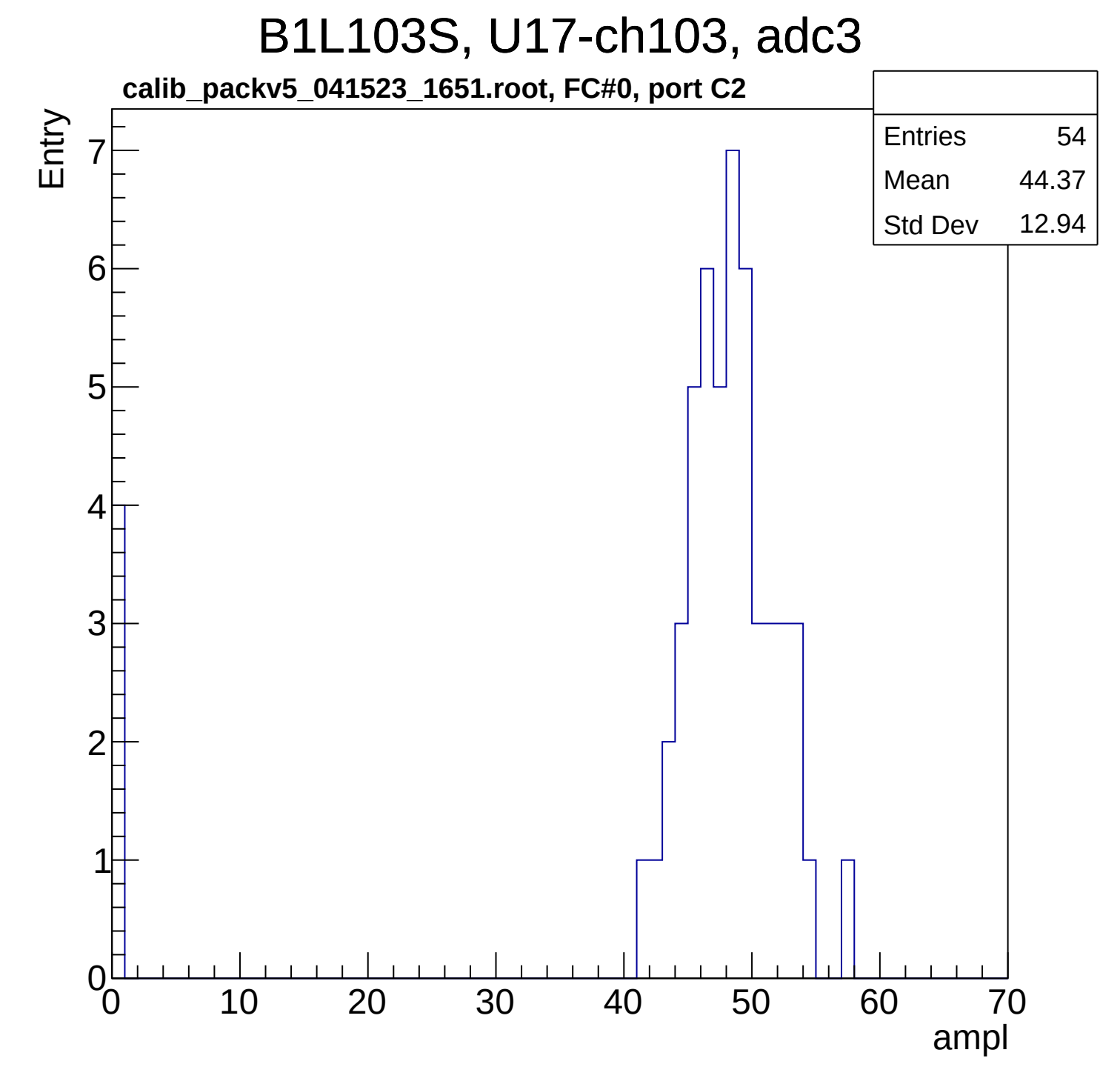
50
60
70
ampl


B1L103S, U17-ch103, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 44.37
Std Dev 12.94
Entry
ampl
0
1
2
3
4
5
6
7
0
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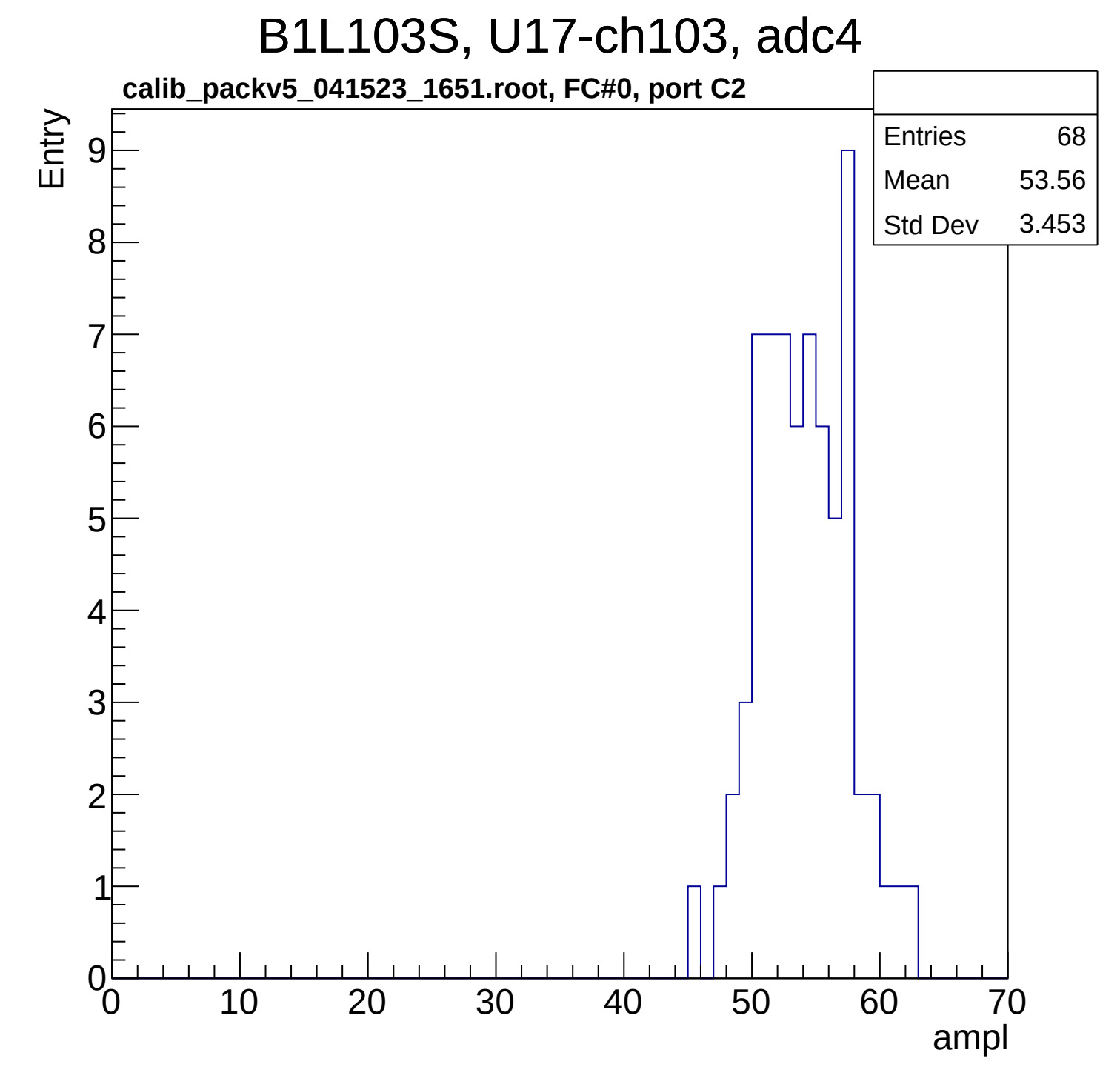
B1L103S, U17-ch103, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 53.56
Std Dev 3.453
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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40
50
60
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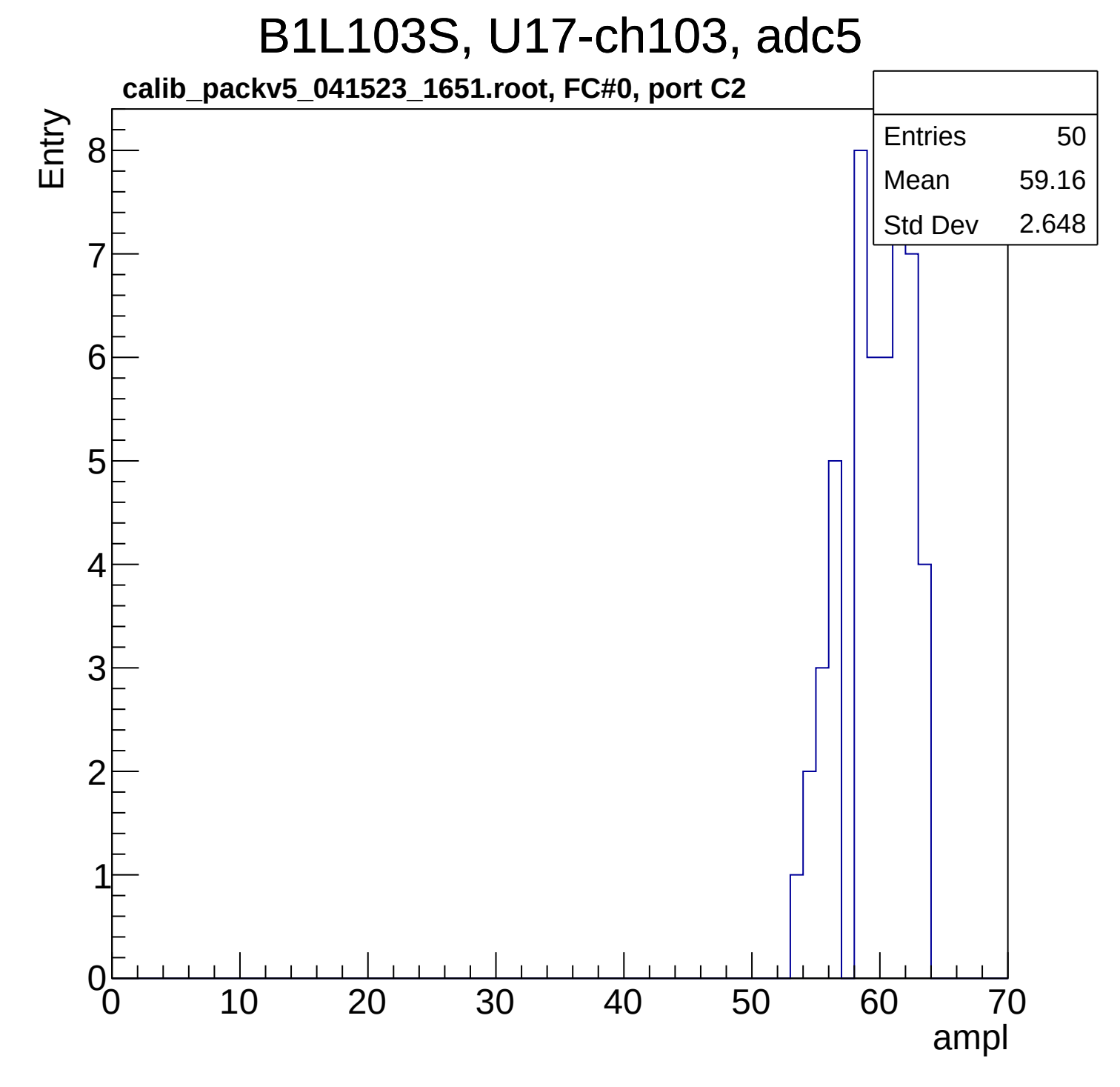
B1L103S, U17-ch103, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 59.16
Std Dev 2.648
Entry
ampl
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1
2
3
4
5
6
7
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0
10
20
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40
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60
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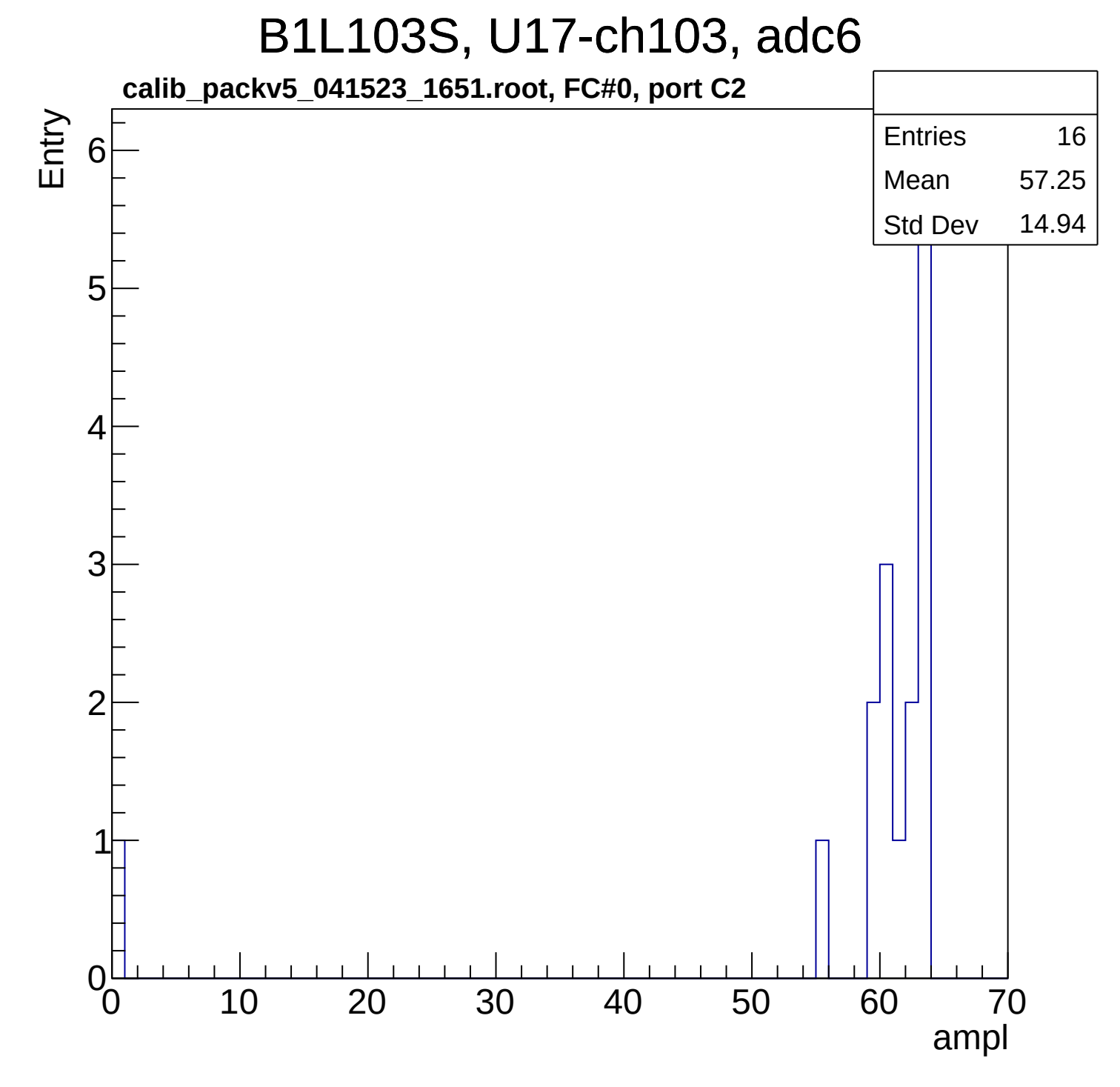
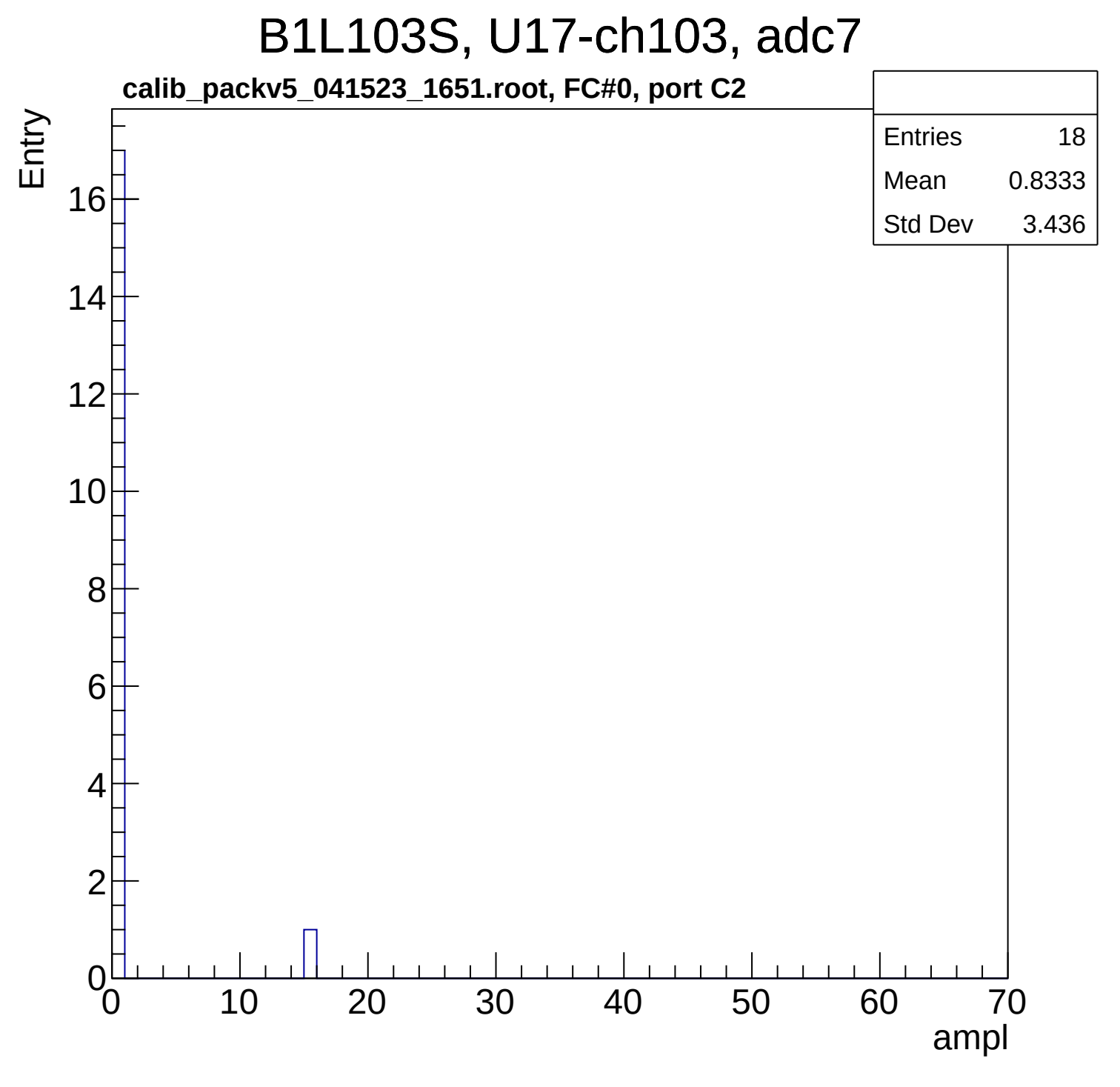

B1L103S, U17-ch103, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 16
Mean 57.25
Std Dev 14.94
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U17-ch103, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0.8333
Std Dev 3.436
Entry
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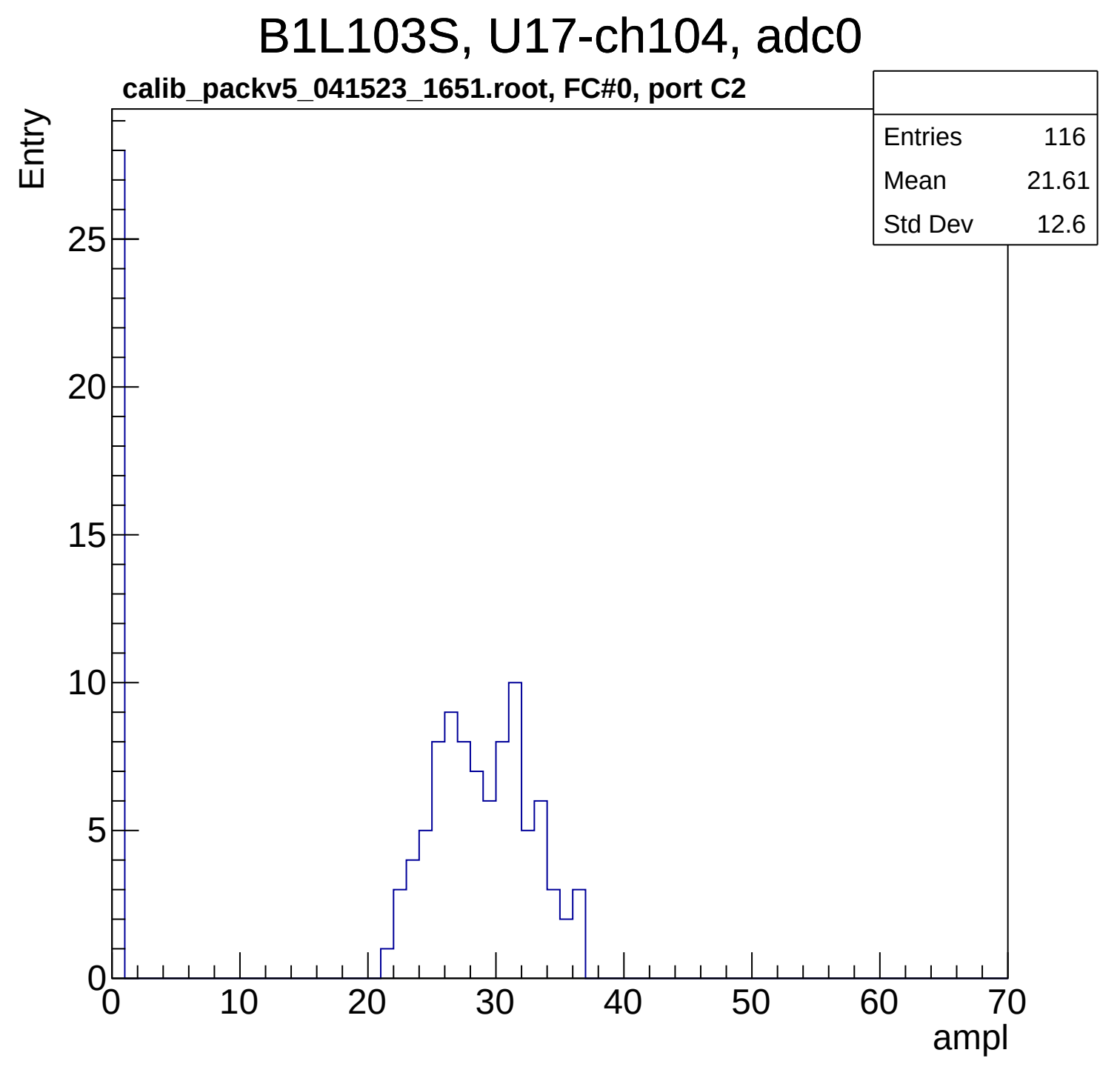
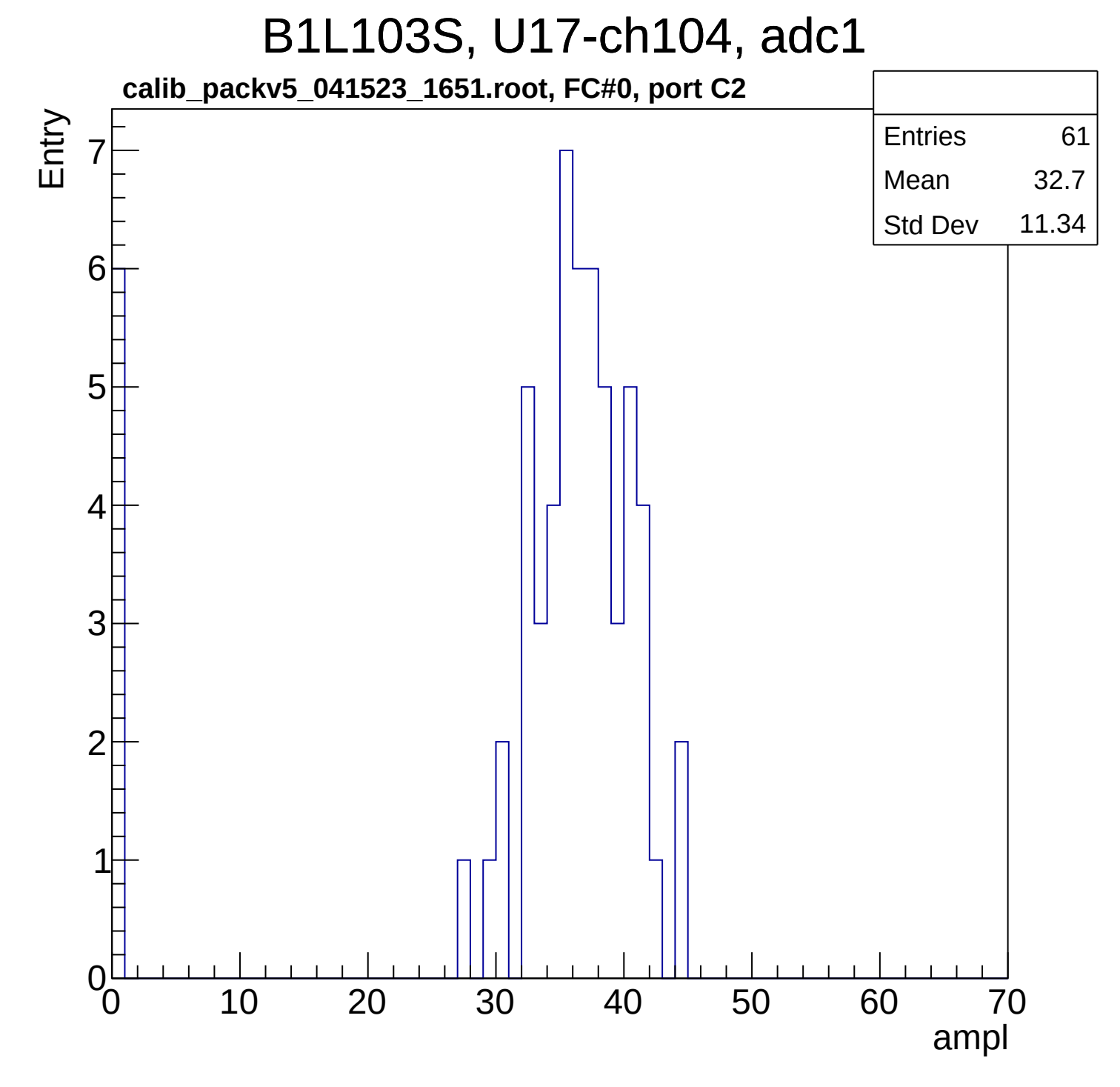
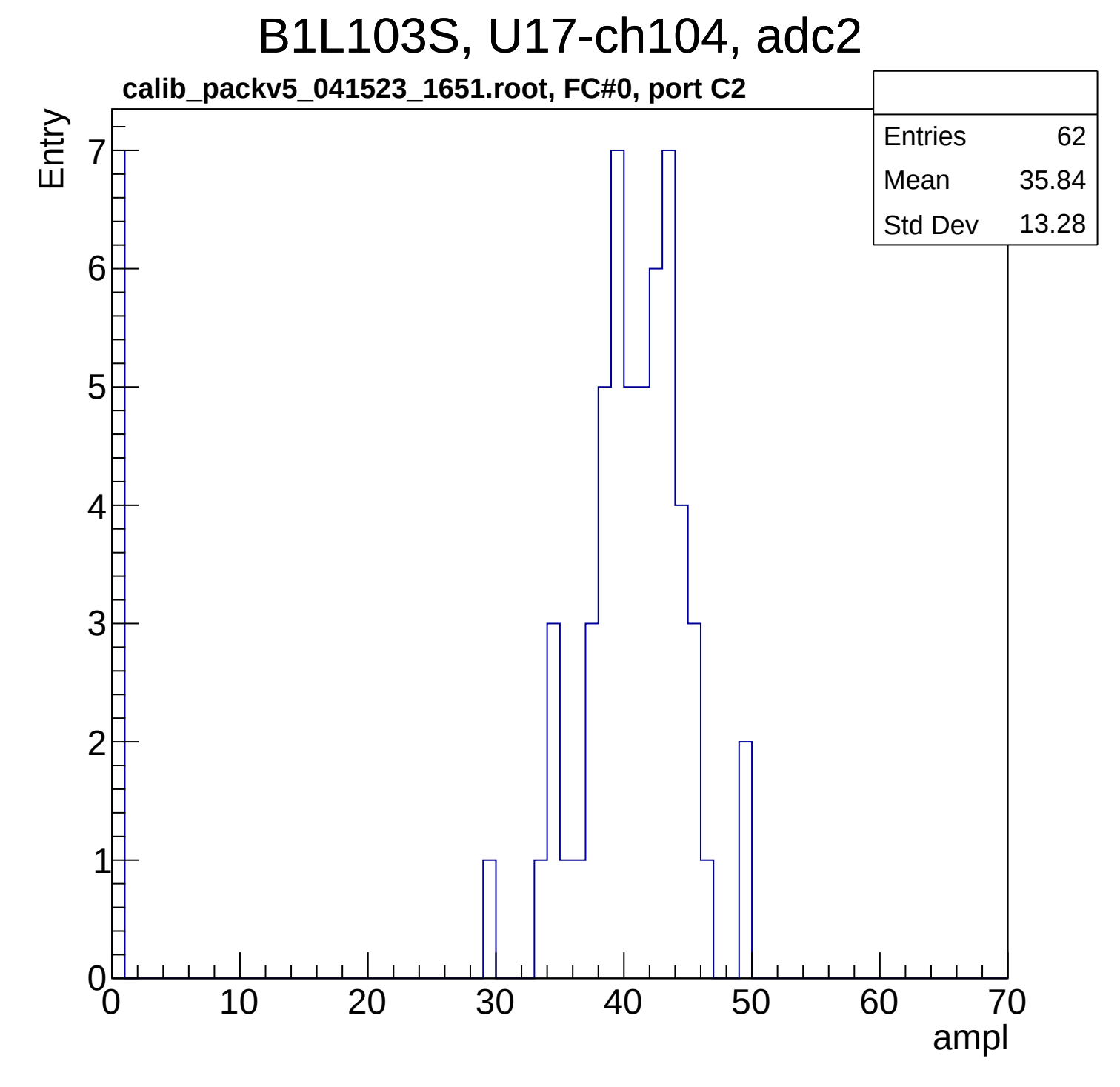
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch104, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 116
Mean 21.61
Std Dev 12.6
Entry
0
5
10
15
20
25
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch104, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 32.7
Std Dev 11.34
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U17-ch104, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 35.84
Std Dev 13.28
Entry
ampl
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2
3
4
5
6
7
0
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20
30
40
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60
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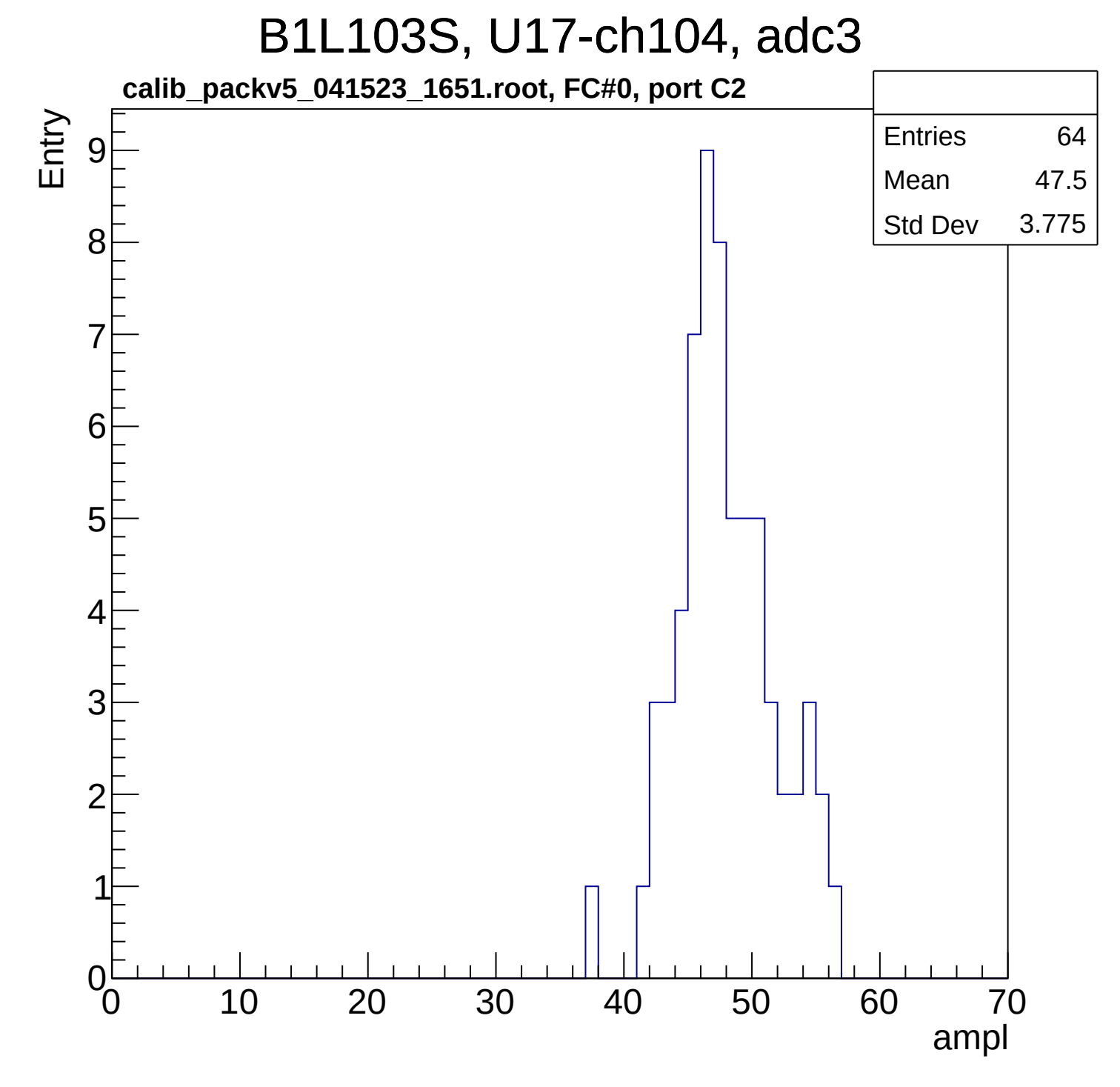
B1L103S, U17-ch104, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 47.5
Std Dev 3.775
Entry
ampl
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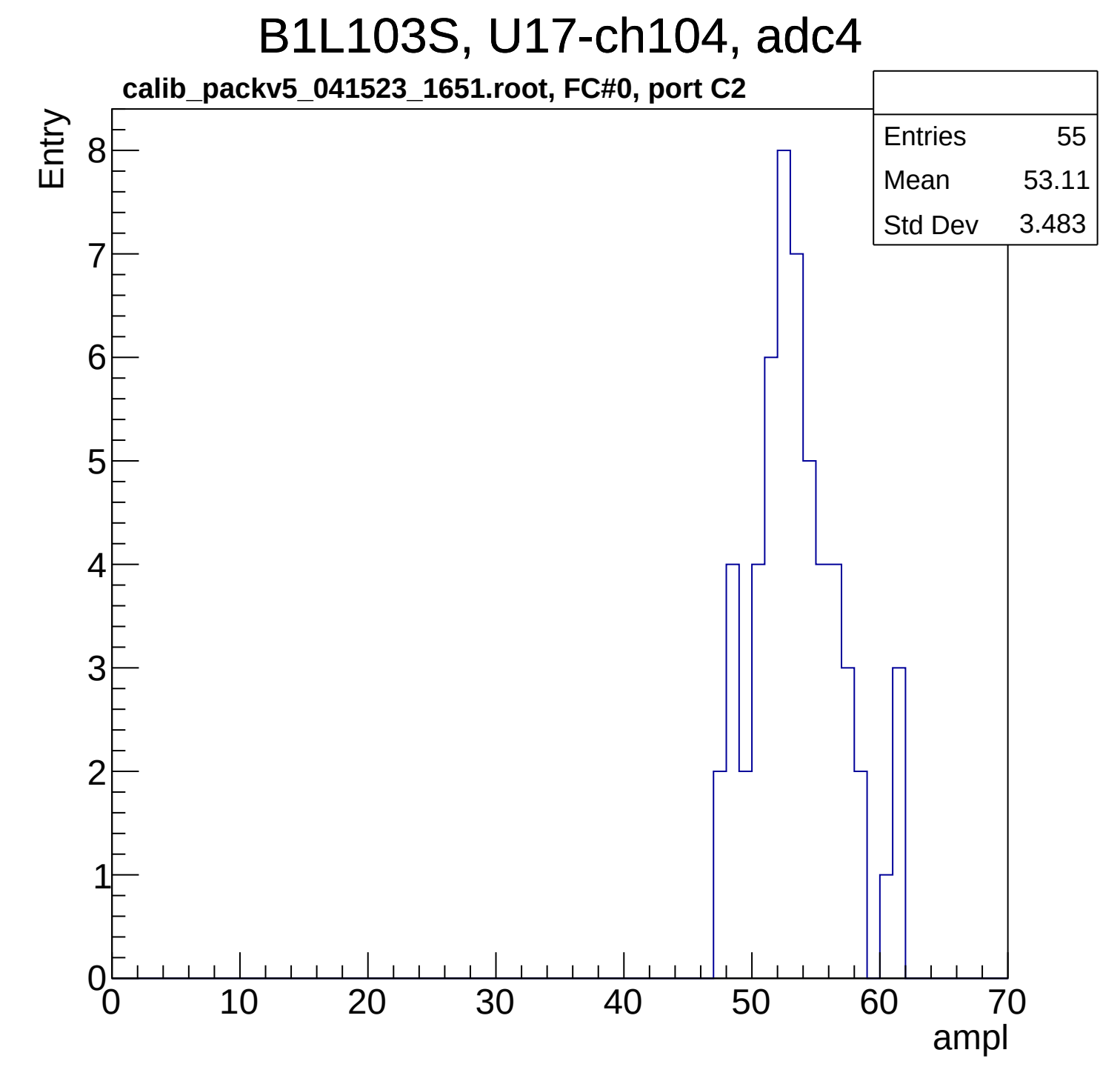
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U17-ch104, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 53.11
Std Dev 3.483
Entry
ampl
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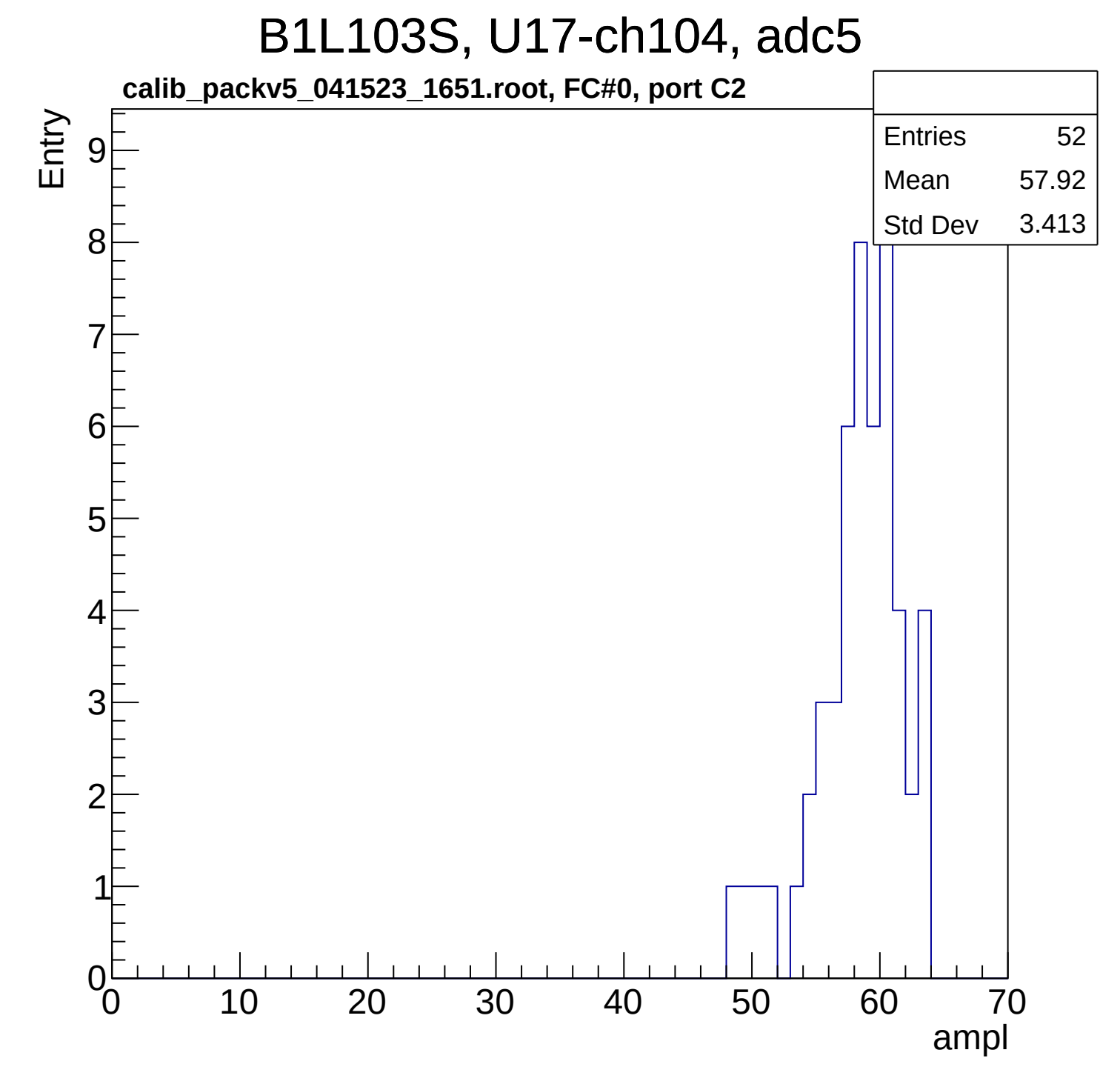
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U17-ch104, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 57.92
Std Dev 3.413
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
50
60
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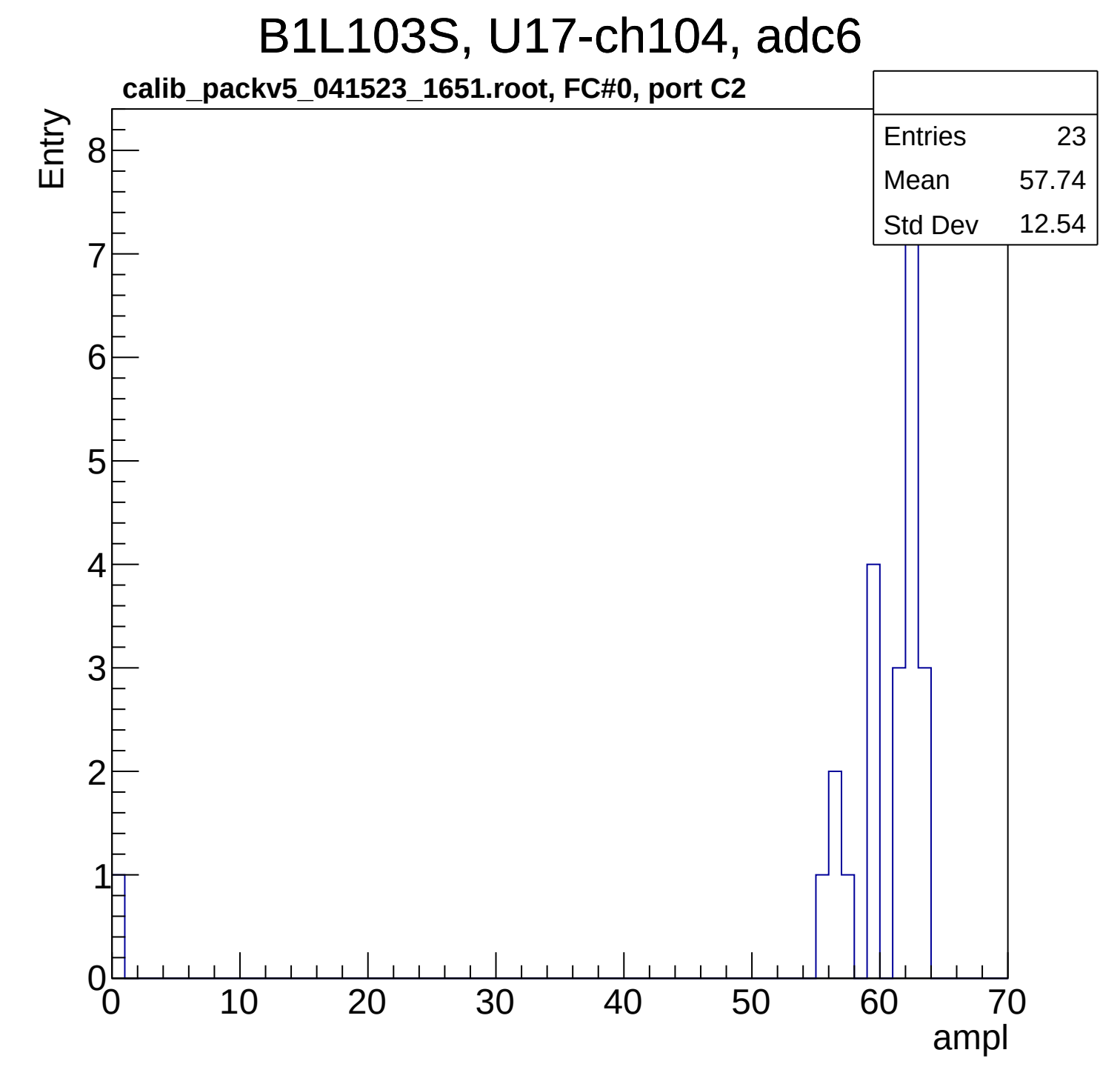
B1L103S, U17-ch104, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 23
Mean 57.74
Std Dev 12.54
Entry
ampl
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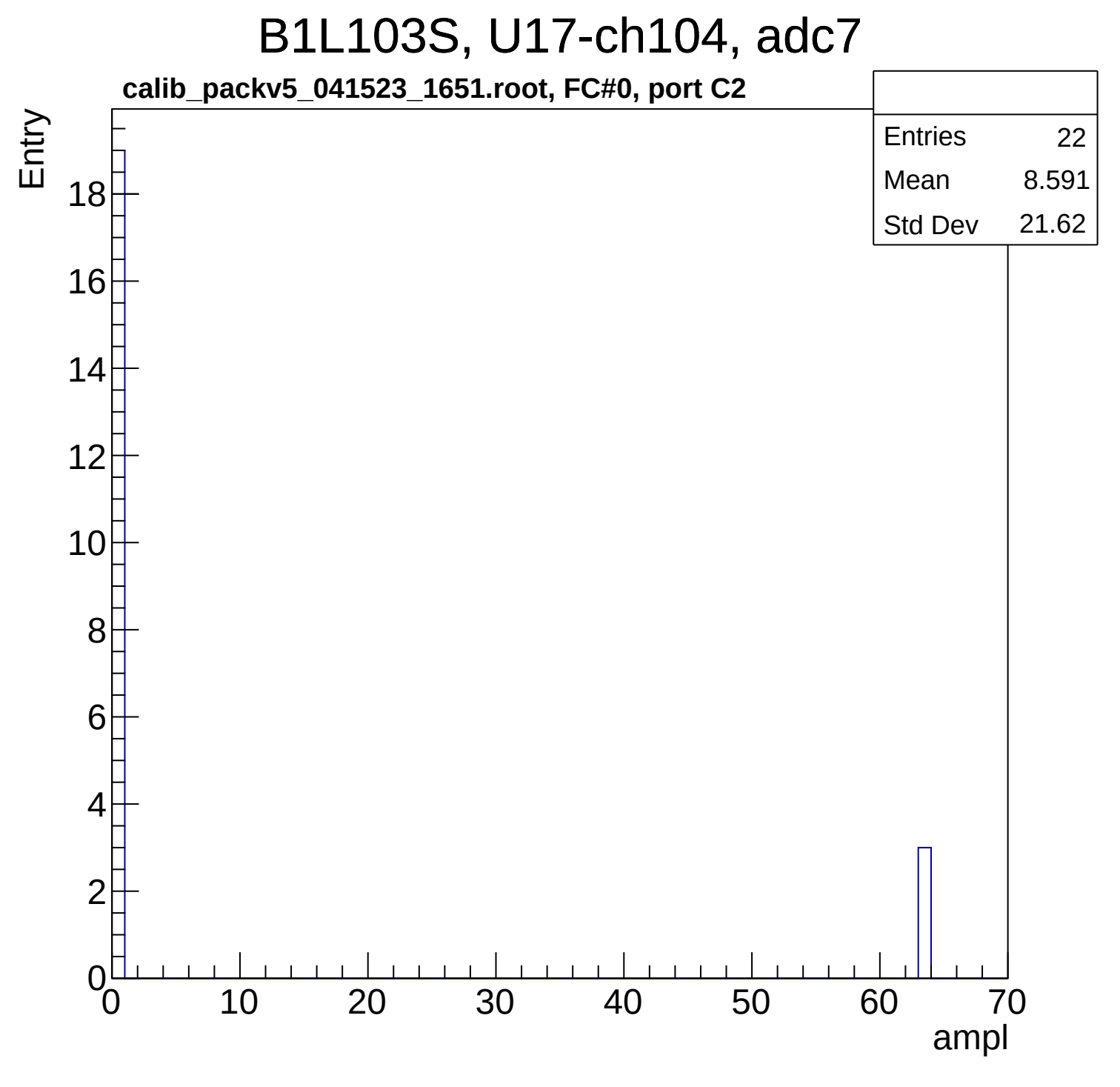
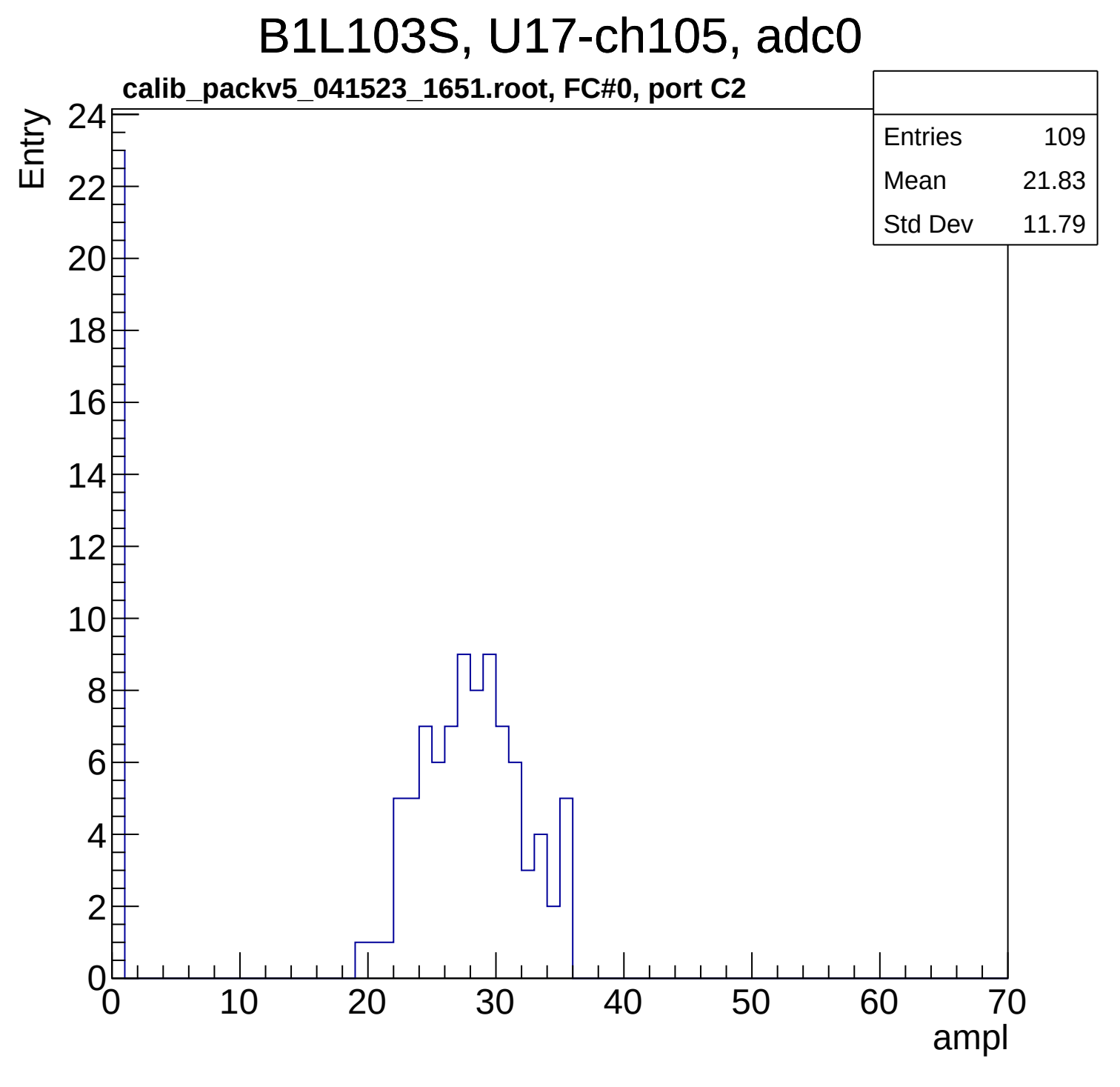
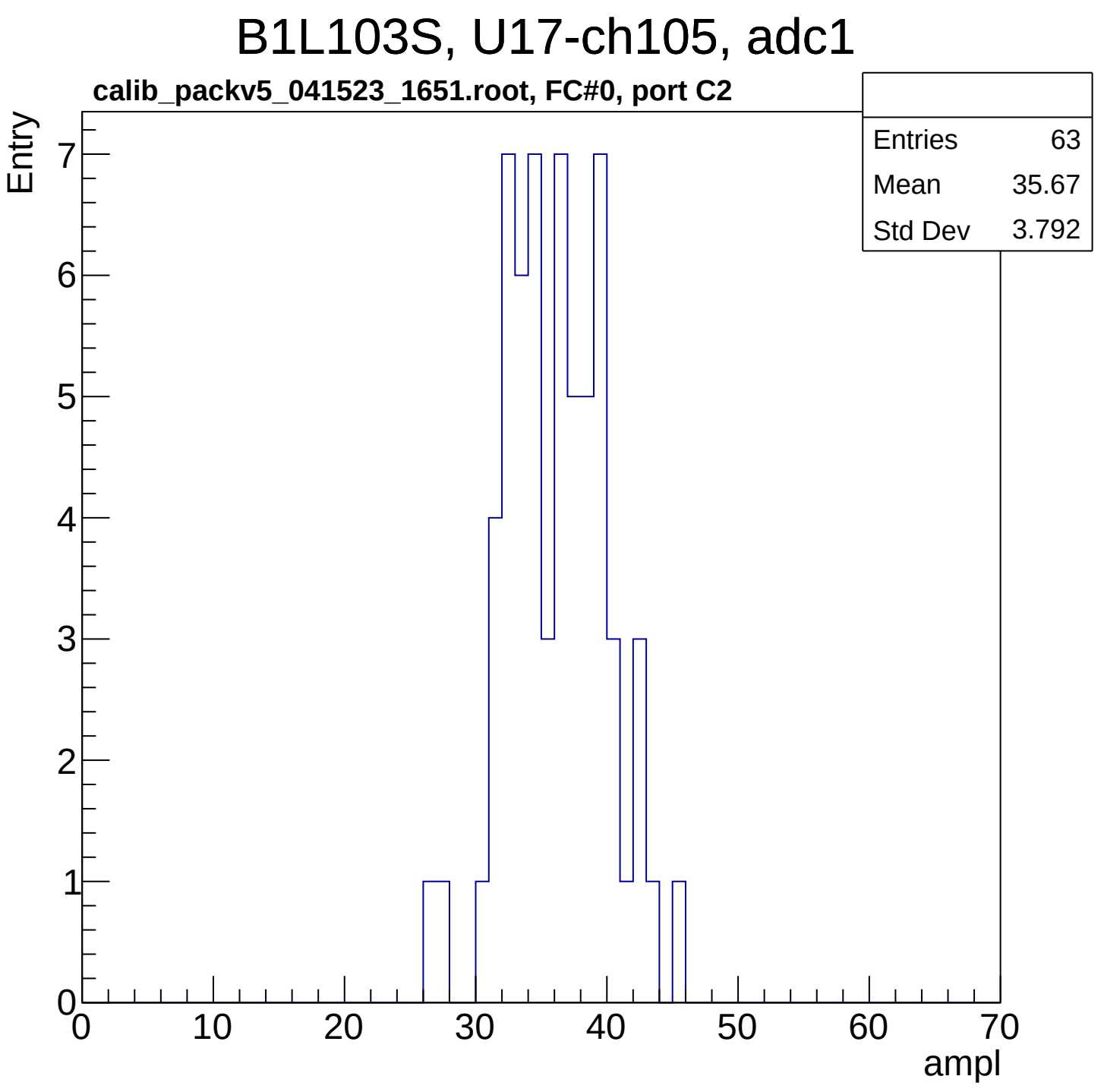
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U17-ch104, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 8.591
Std Dev 21.62
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch105, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 109
Mean 21.83
Std Dev 11.79
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
22
24
0
10
20
30
40
50
60
70


B1L103S, U17-ch105, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 35.67
Std Dev 3.792
Entry
ampl
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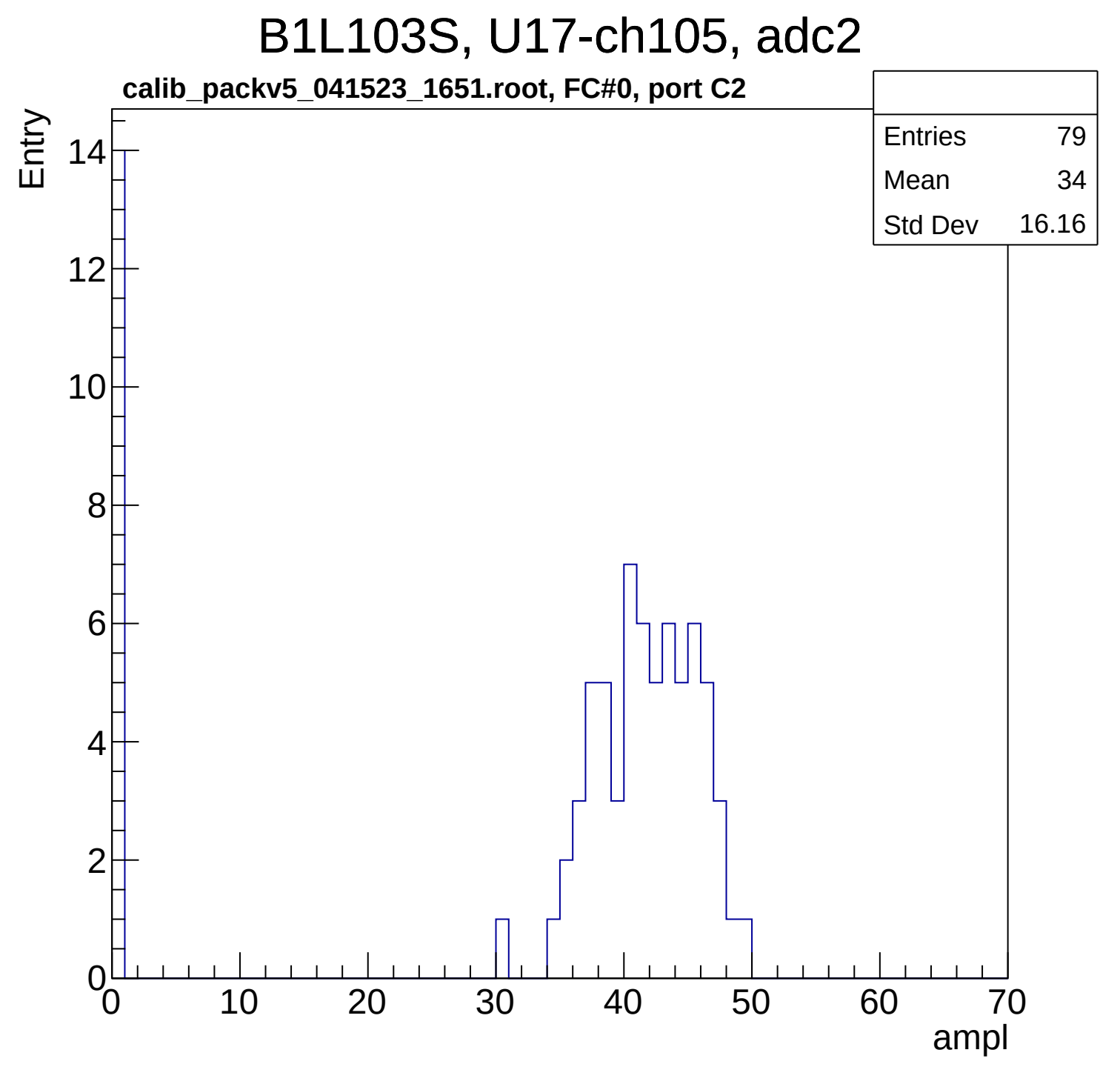
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U17-ch105, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 34
Std Dev 16.16
Entry
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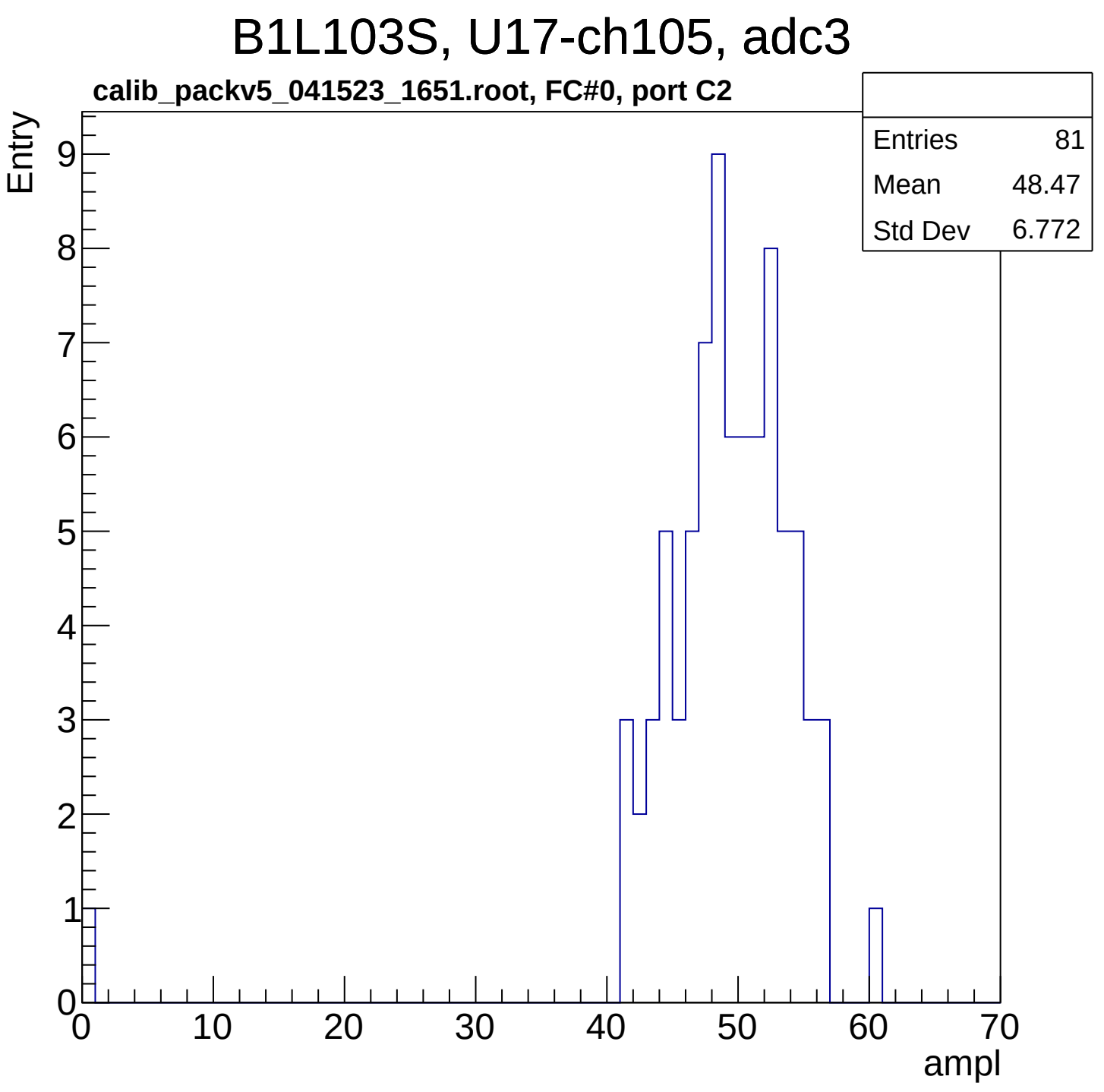
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch105, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 48.47
Std Dev 6.772
Entry
ampl
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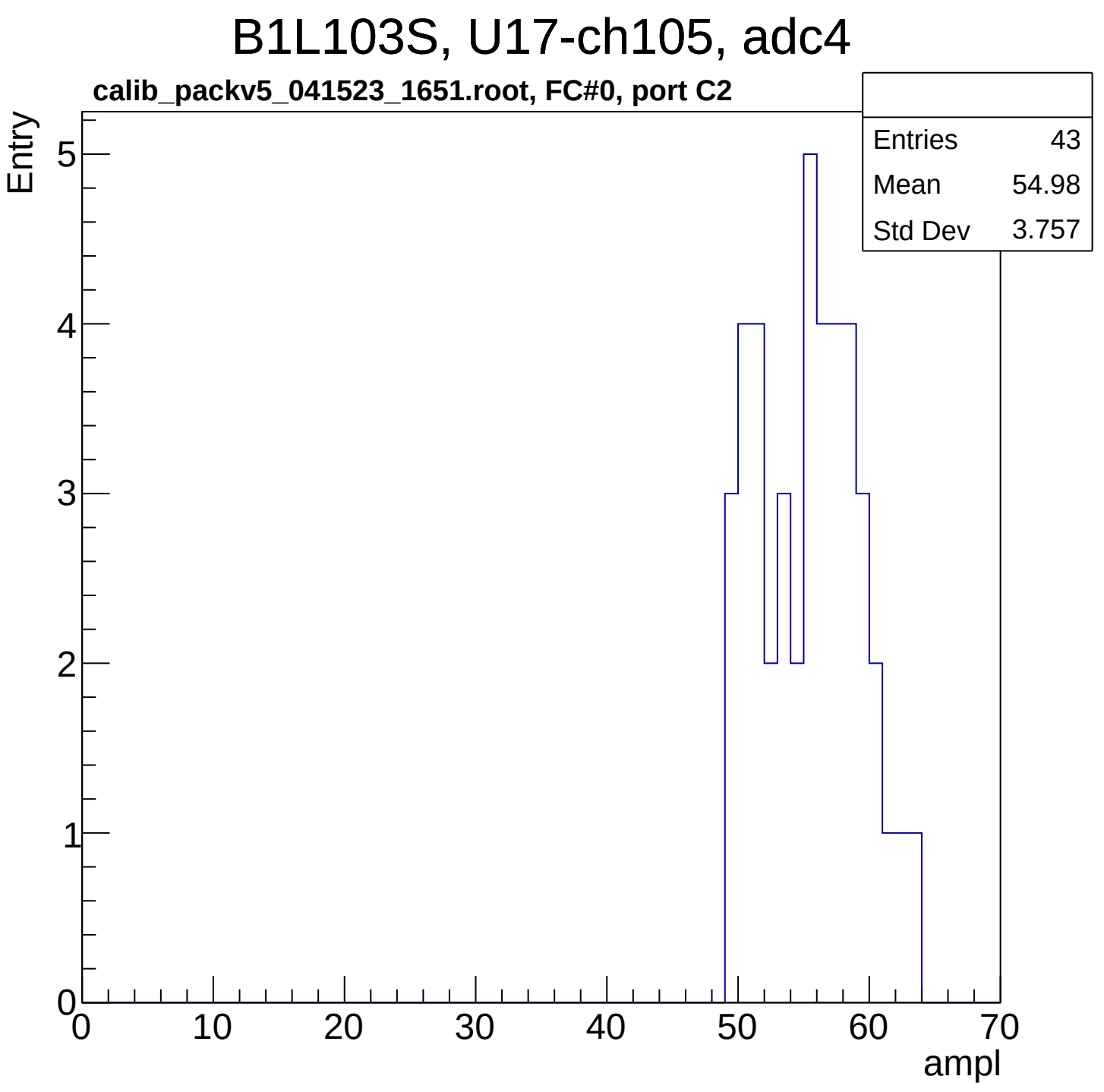
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U17-ch105, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 43
Mean 54.98
Std Dev 3.757
Entry
ampl
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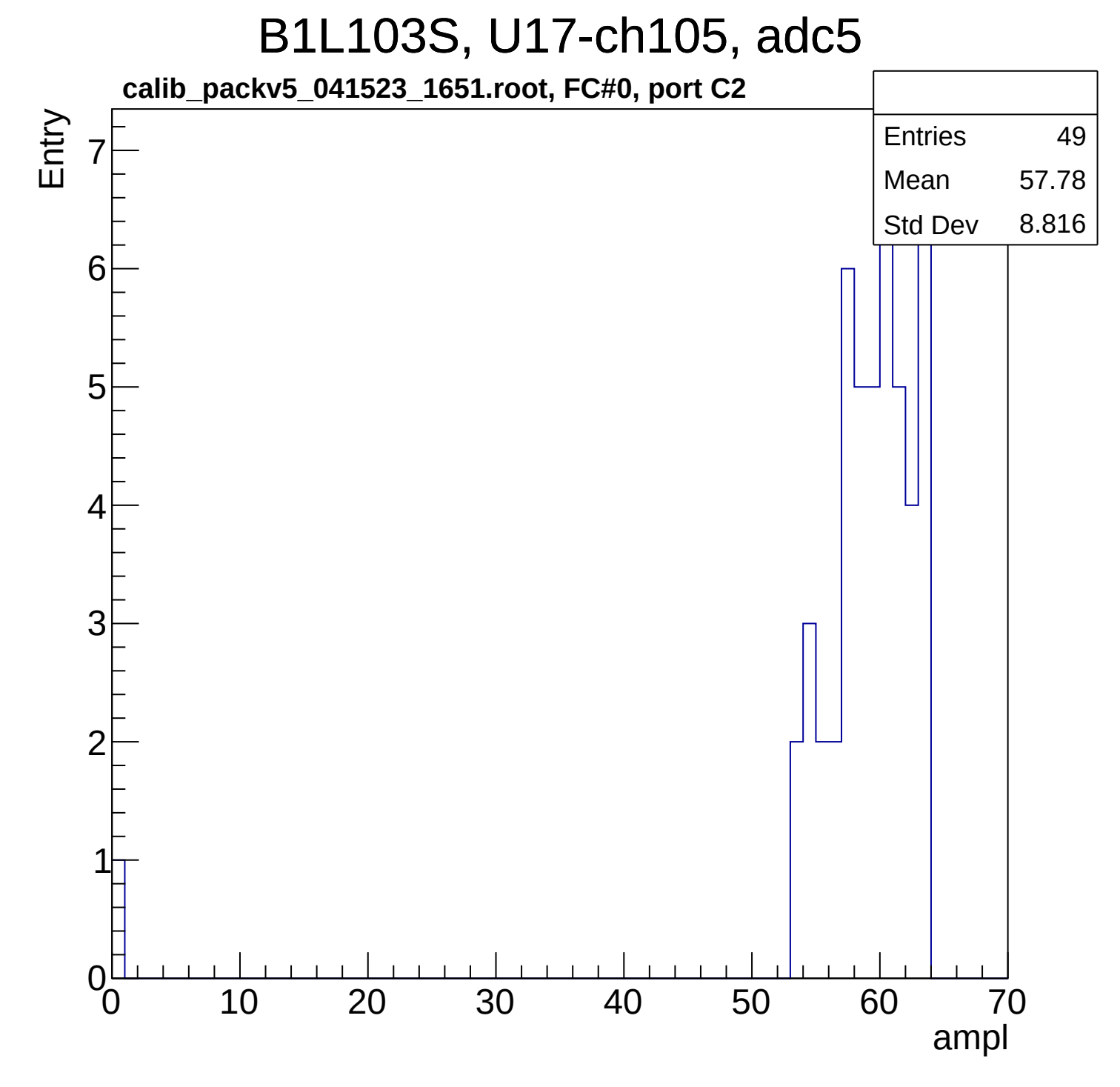
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U17-ch105, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 57.78
Std Dev 8.816
Entry
ampl
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1
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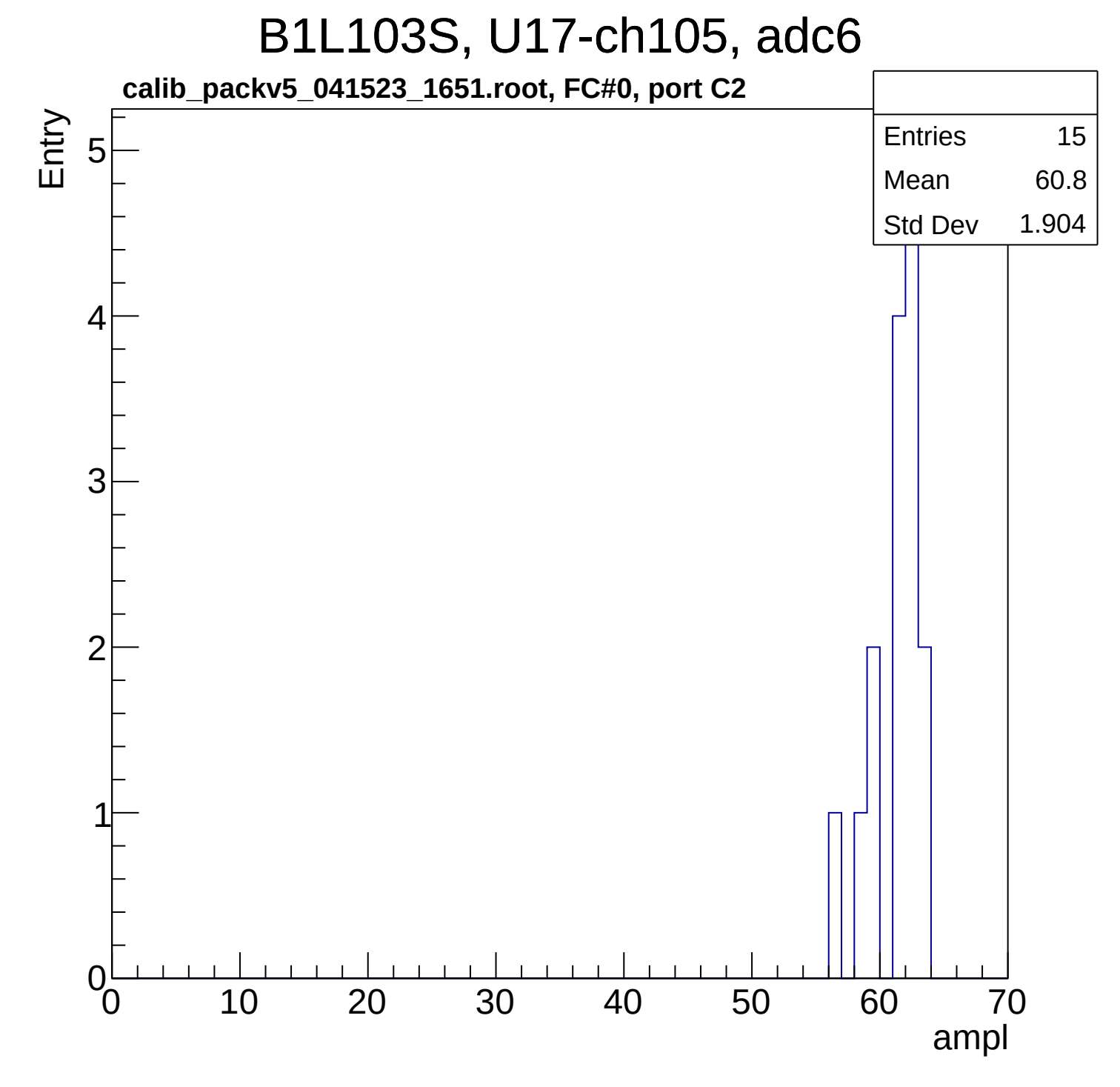
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U17-ch105, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 15
Mean 60.8
Std Dev 1.904
Entry
ampl
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1
2
3
4
5
0
10
20
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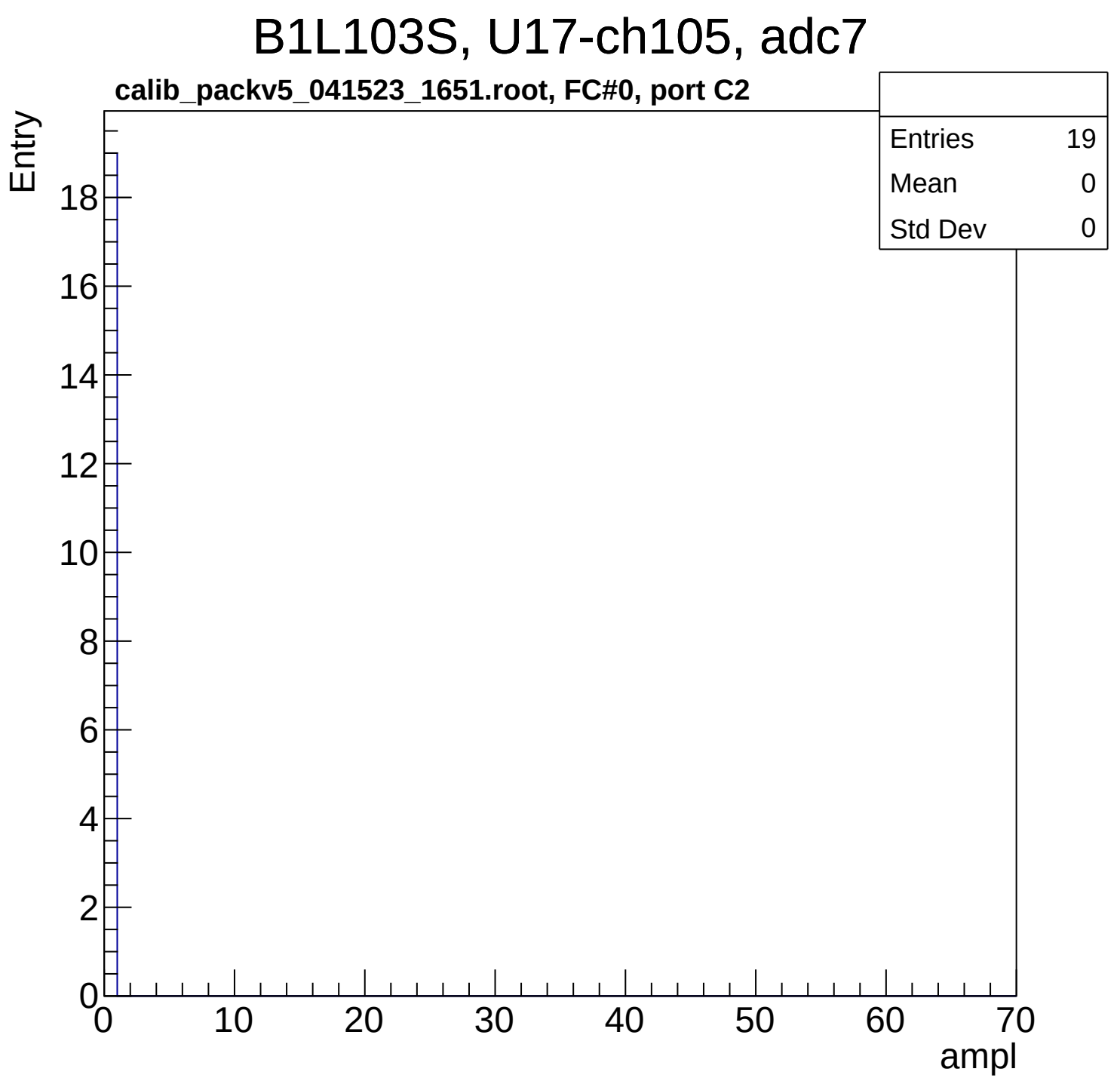
40
50
60
70


B1L103S, U17-ch105, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
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4
6
8
10
12
14
16
18
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10
20
30
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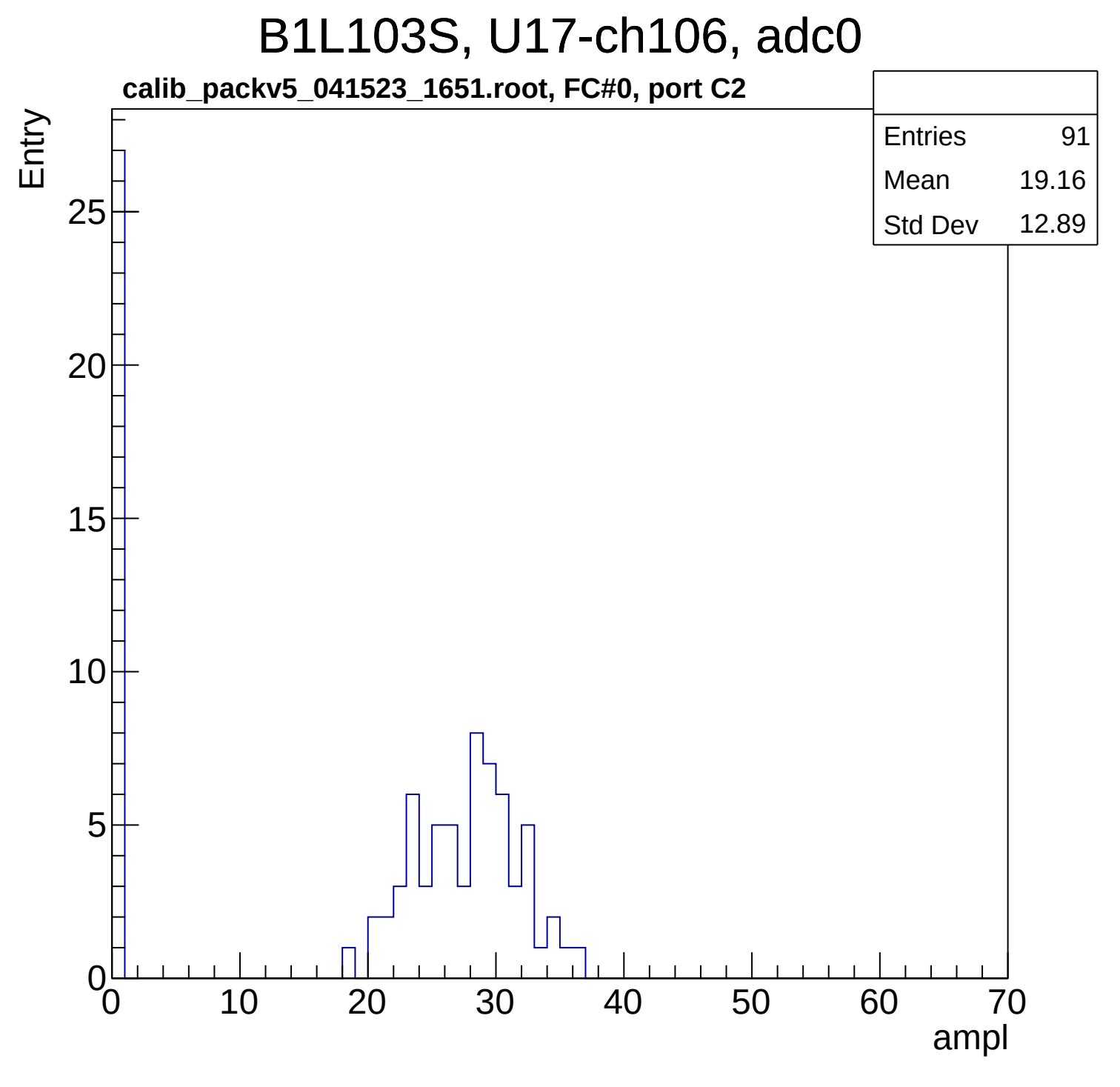
50
60
70
ampl


B1L103S, U17-ch106, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 91
Mean 19.16
Std Dev 12.89
Entry
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5
10
15
20
25
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10
20
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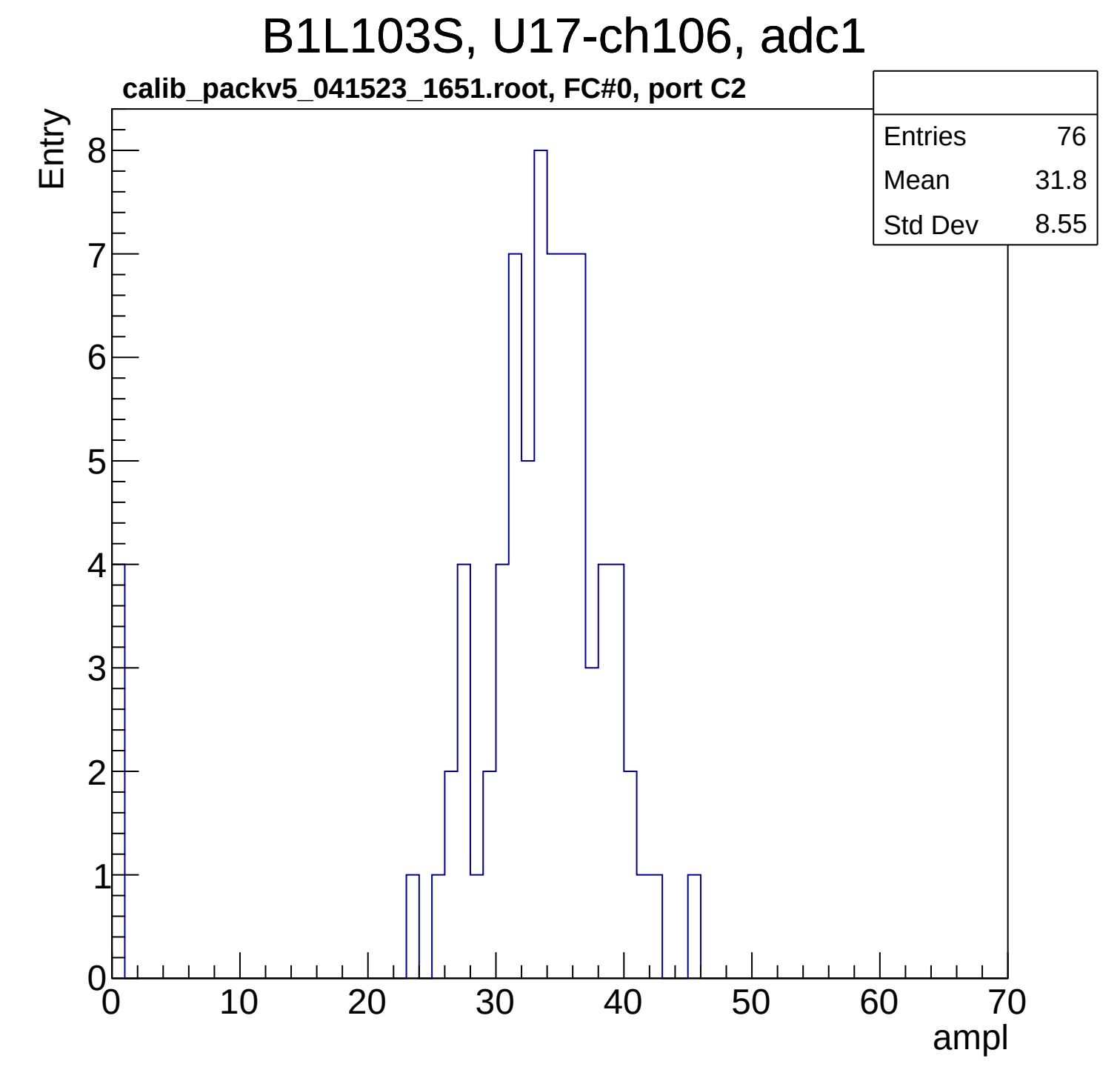
50
60
70
ampl


B1L103S, U17-ch106, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 31.8
Std Dev 8.55
Entry
ampl
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3
4
5
6
7
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0
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20
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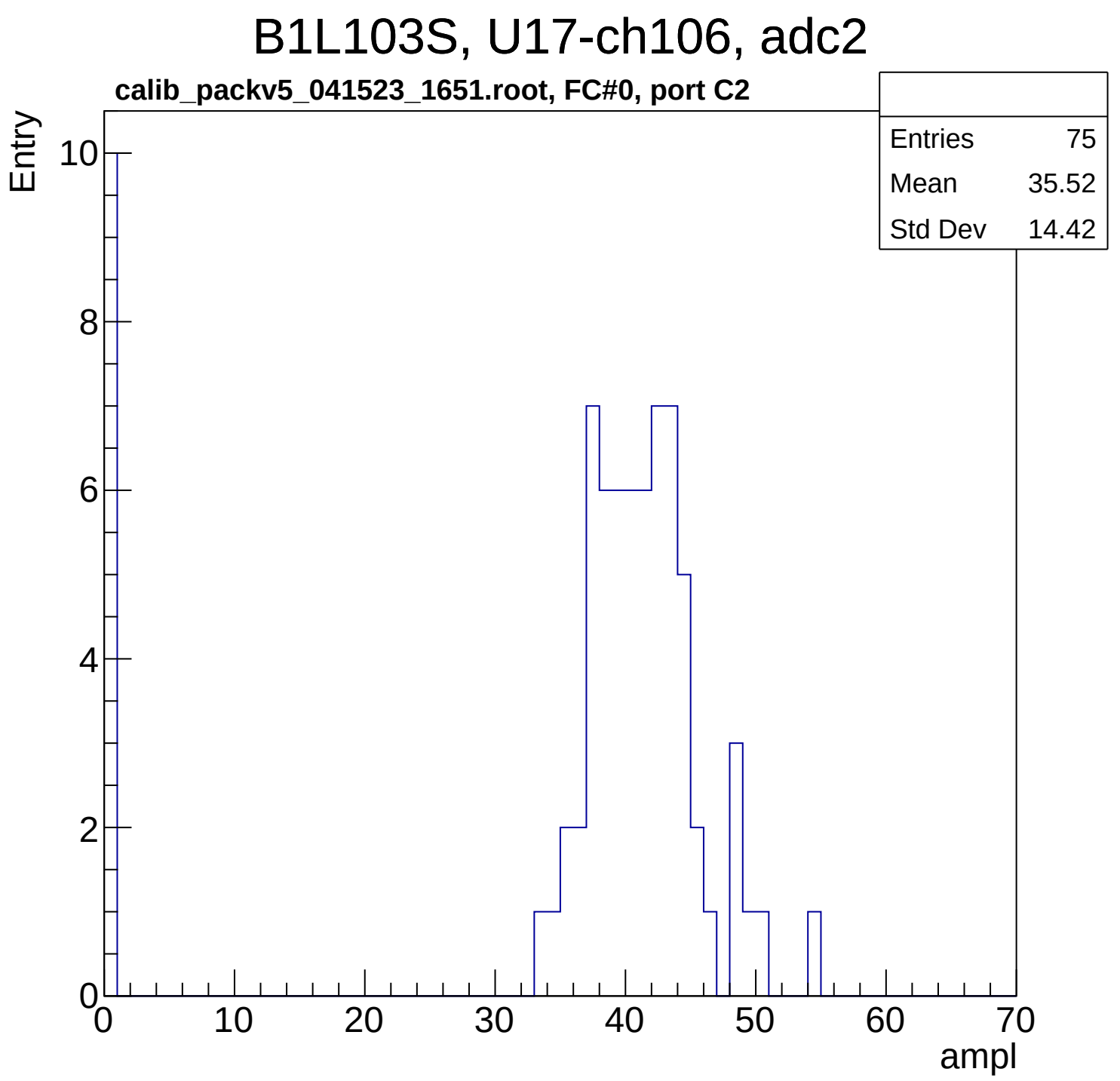
40
50
60
70


B1L103S, U17-ch106, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 35.52
Std Dev 14.42
Entry
ampl
0
2
4
6
8
10
0
10
20
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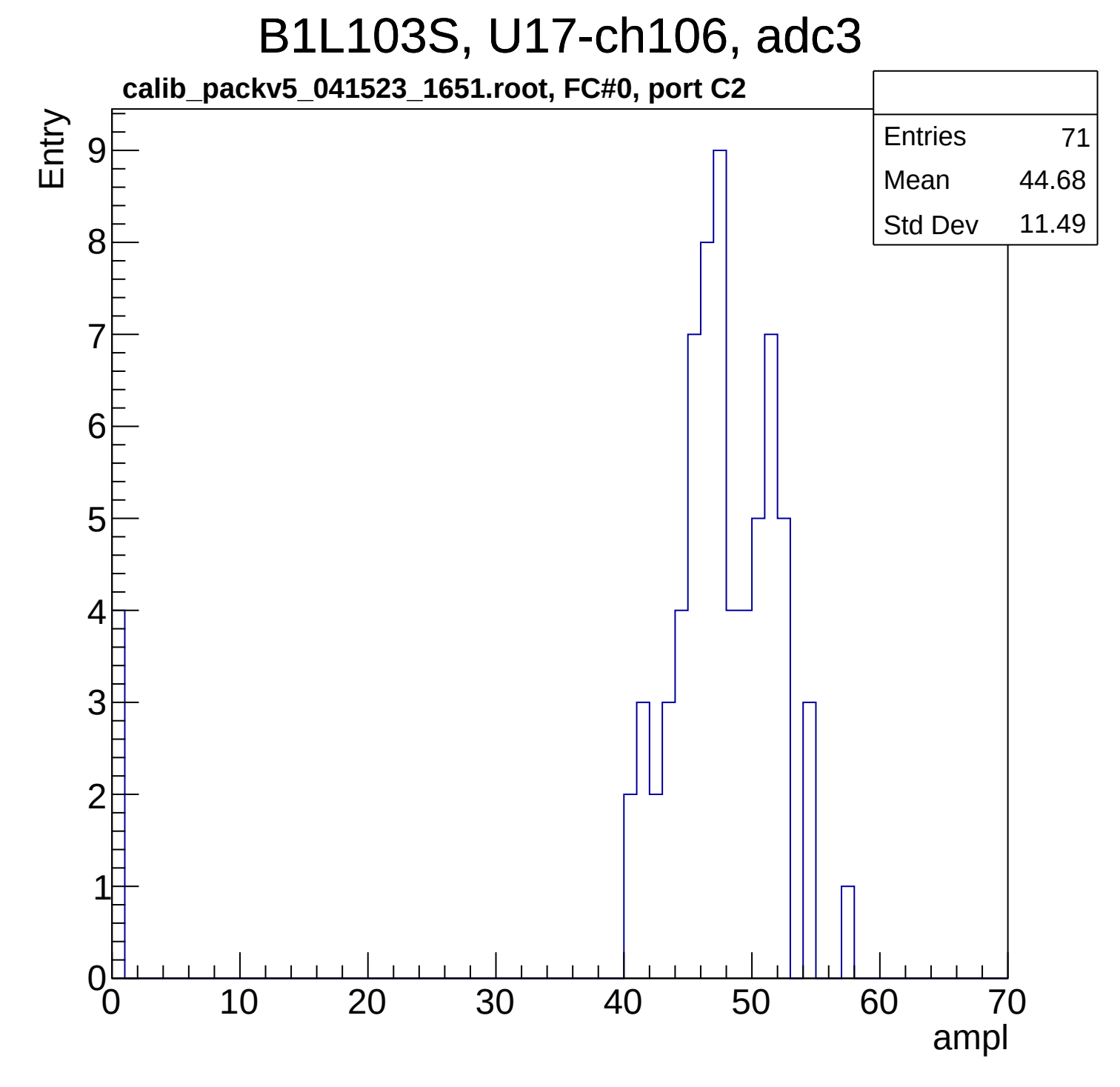
40
50
60
70


B1L103S, U17-ch106, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 44.68
Std Dev 11.49
Entry
ampl
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4
5
6
7
8
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0
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60
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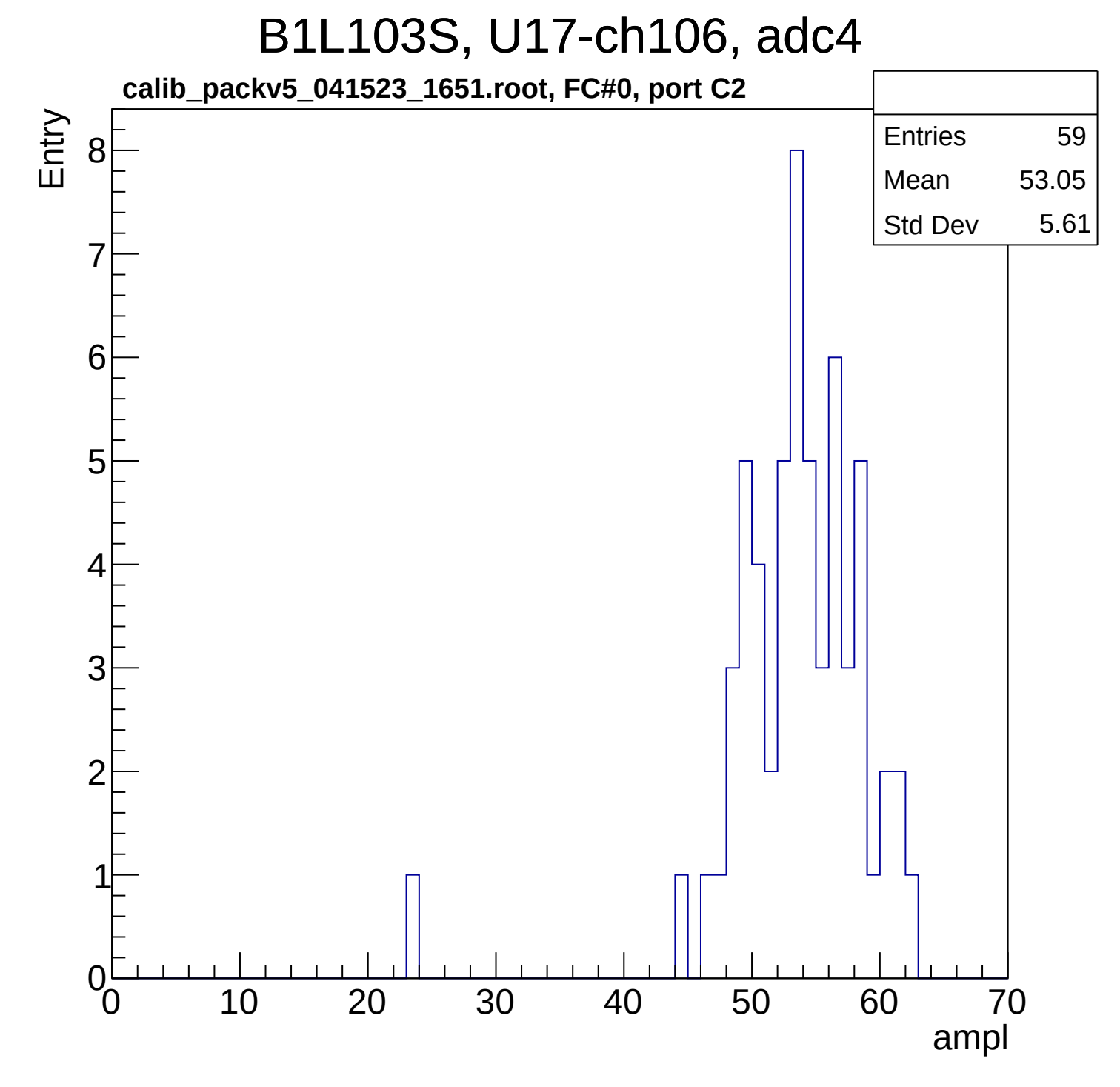
B1L103S, U17-ch106, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 53.05
Std Dev 5.61
Entry
ampl
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1
2
3
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5
6
7
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0
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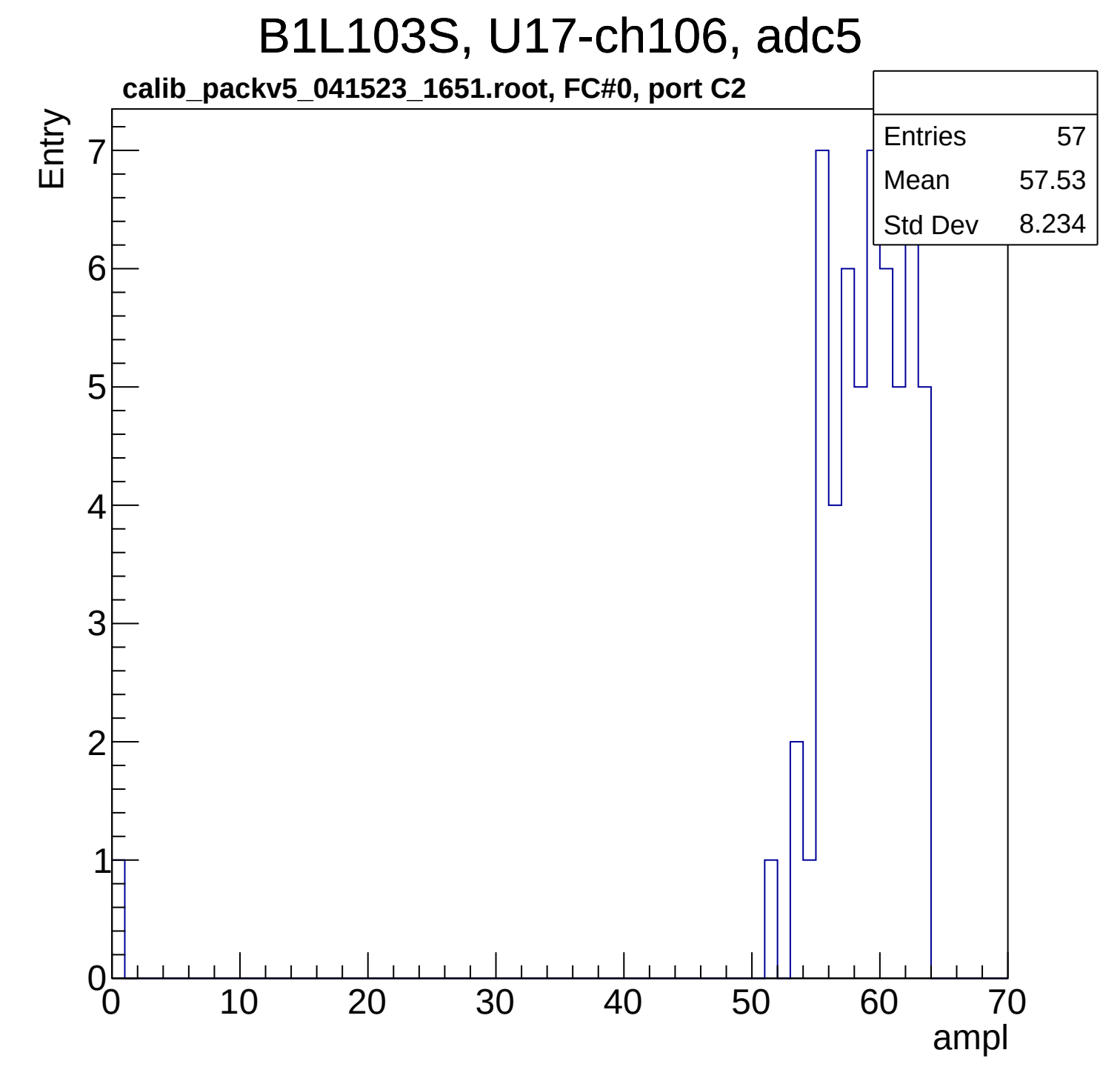
40
50
60
70


B1L103S, U17-ch106, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 57.53
Std Dev 8.234
Entry
ampl
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2
3
4
5
6
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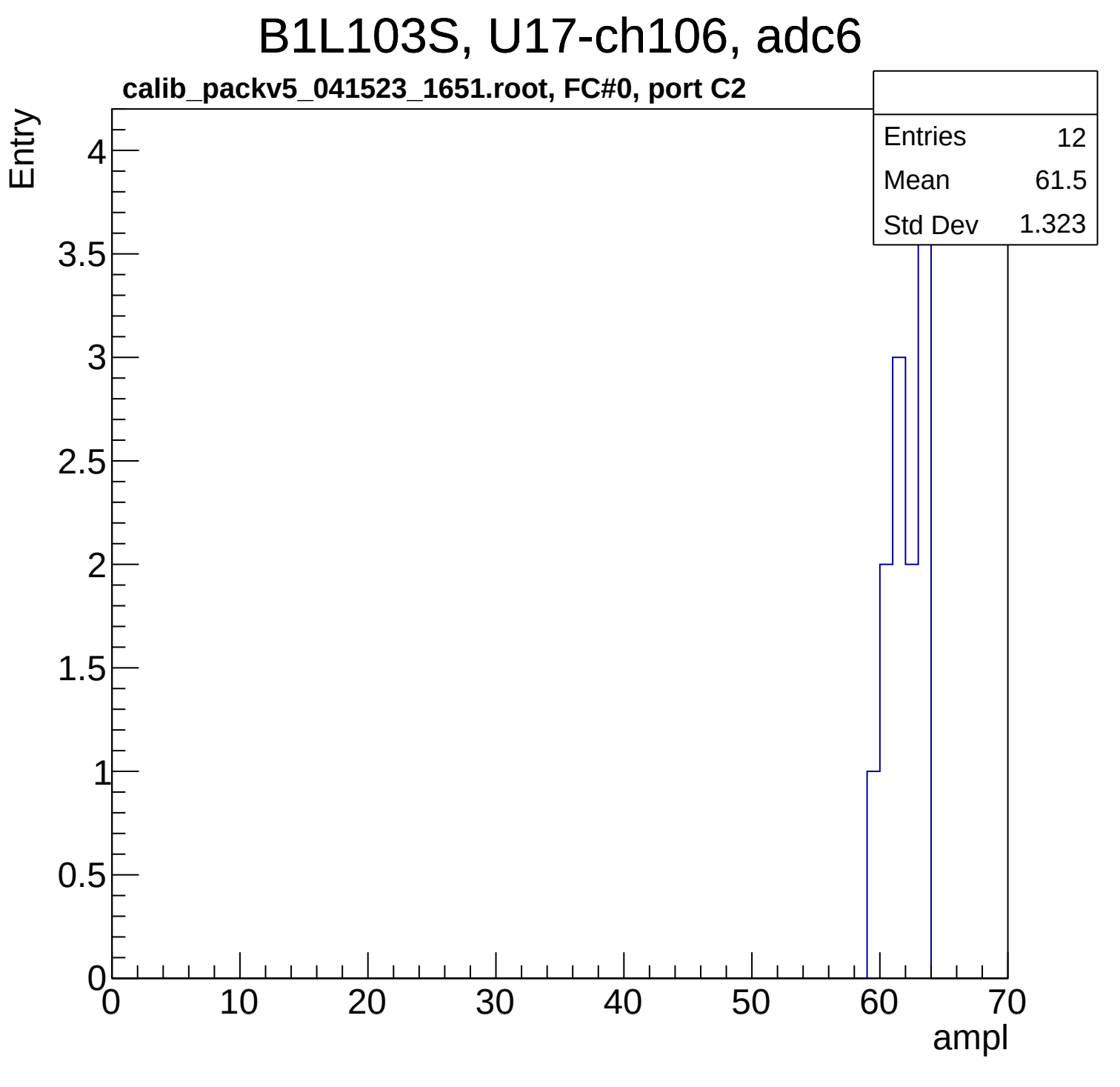
0
10
20
30
40
50
60
70


B1L103S, U17-ch106, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 61.5
Std Dev 1.323
Entry
ampl
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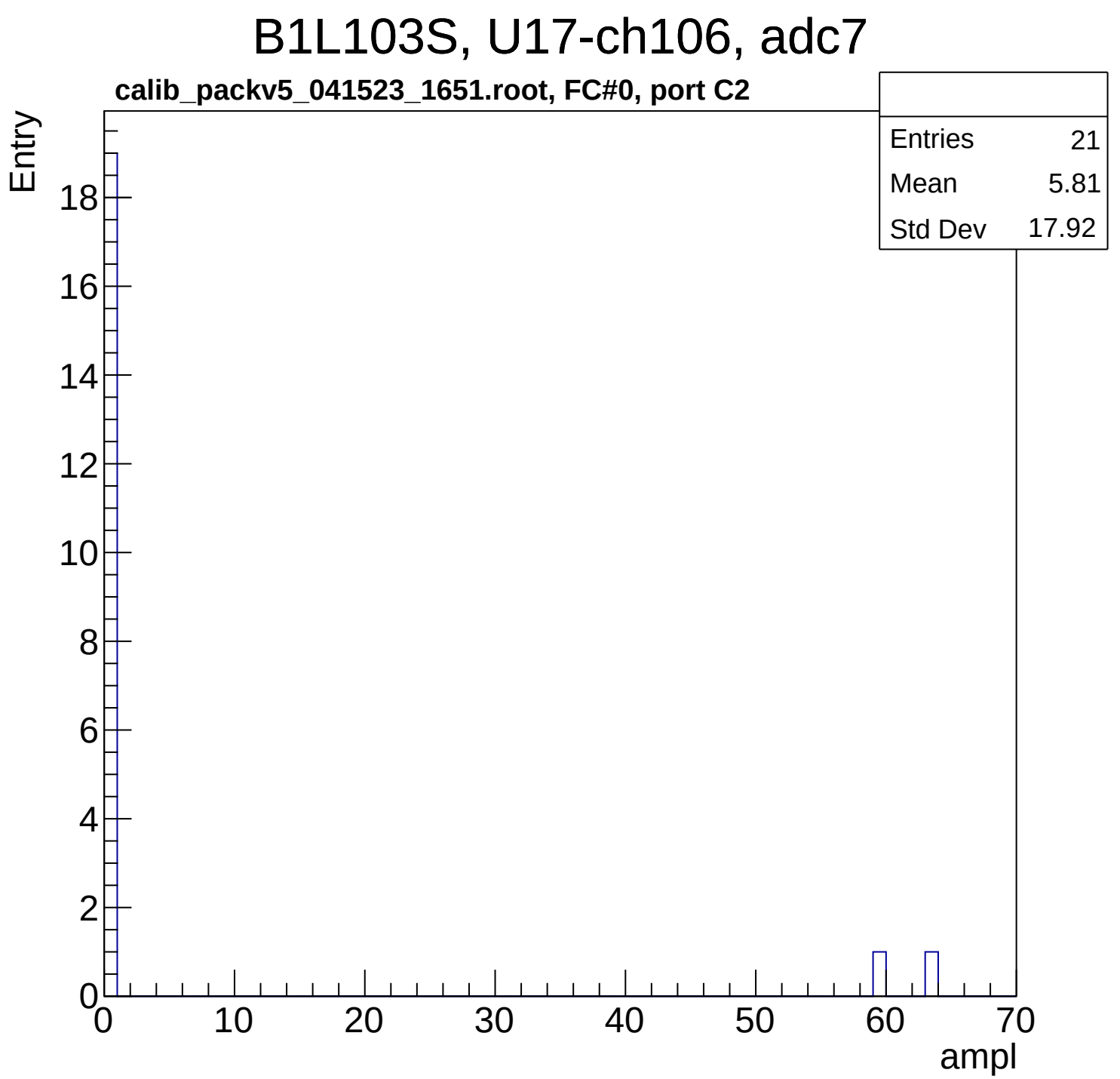
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U17-ch106, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 5.81
Std Dev 17.92
Entry
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8
10
12
14
16
18
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10
20
30
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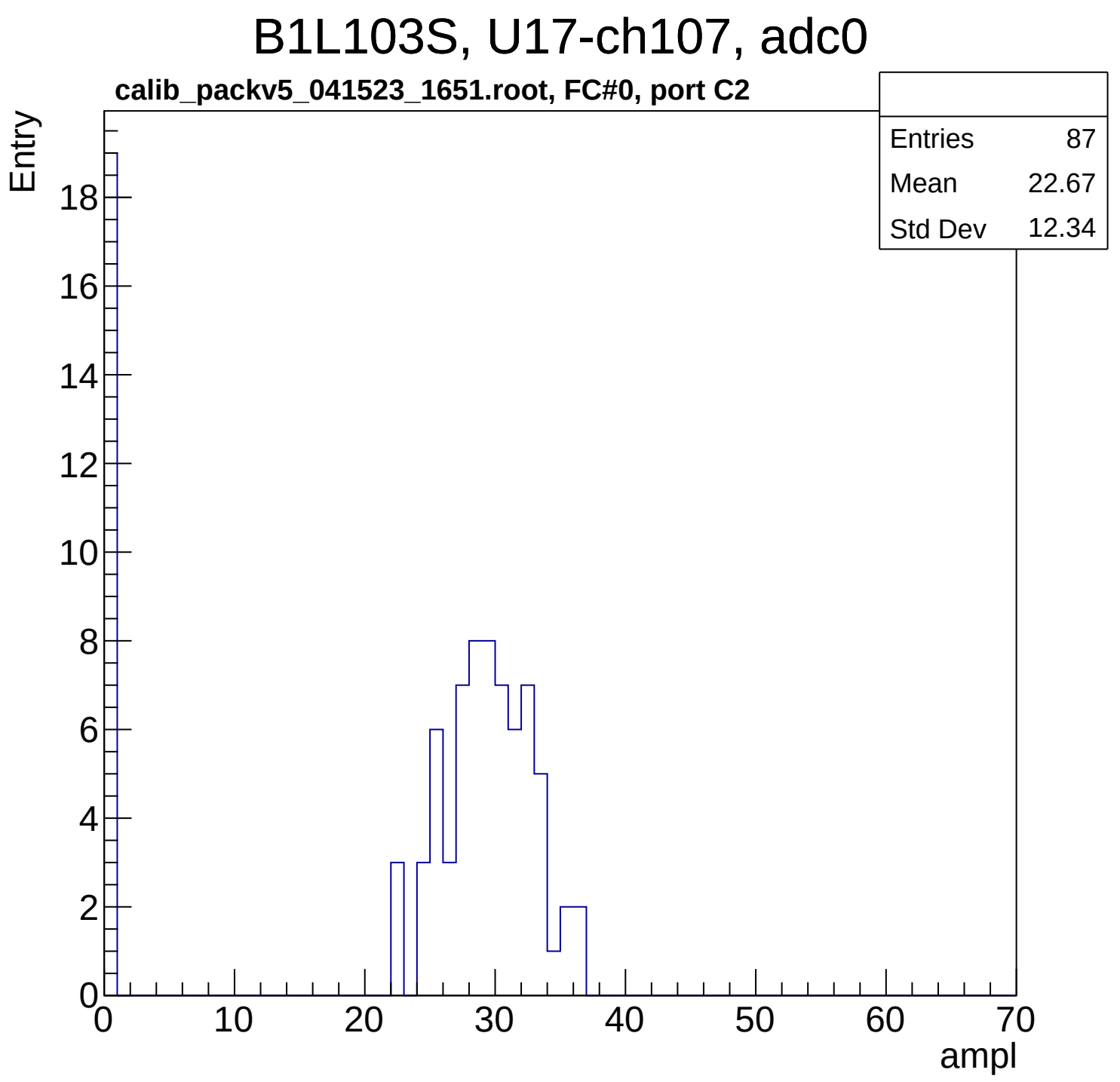
50
60
70
ampl


B1L103S, U17-ch107, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 87
Mean 22.67
Std Dev 12.34
Entry
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6
8
10
12
14
16
18
0
10
20
30
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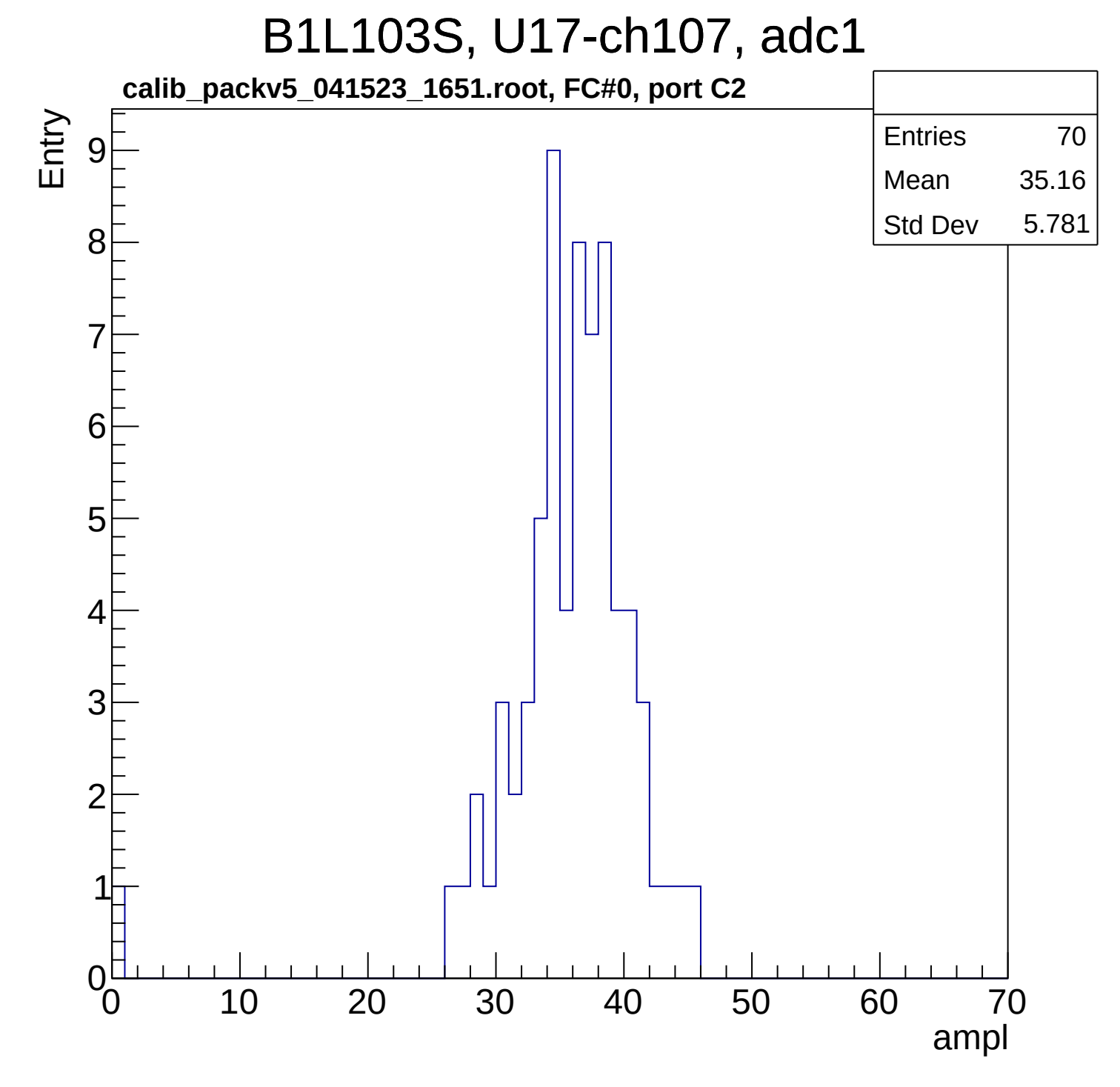
50
60
70
ampl


B1L103S, U17-ch107, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 35.16
Std Dev 5.781
Entry
ampl
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2
3
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5
6
7
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9
0
10
20
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40
50
60
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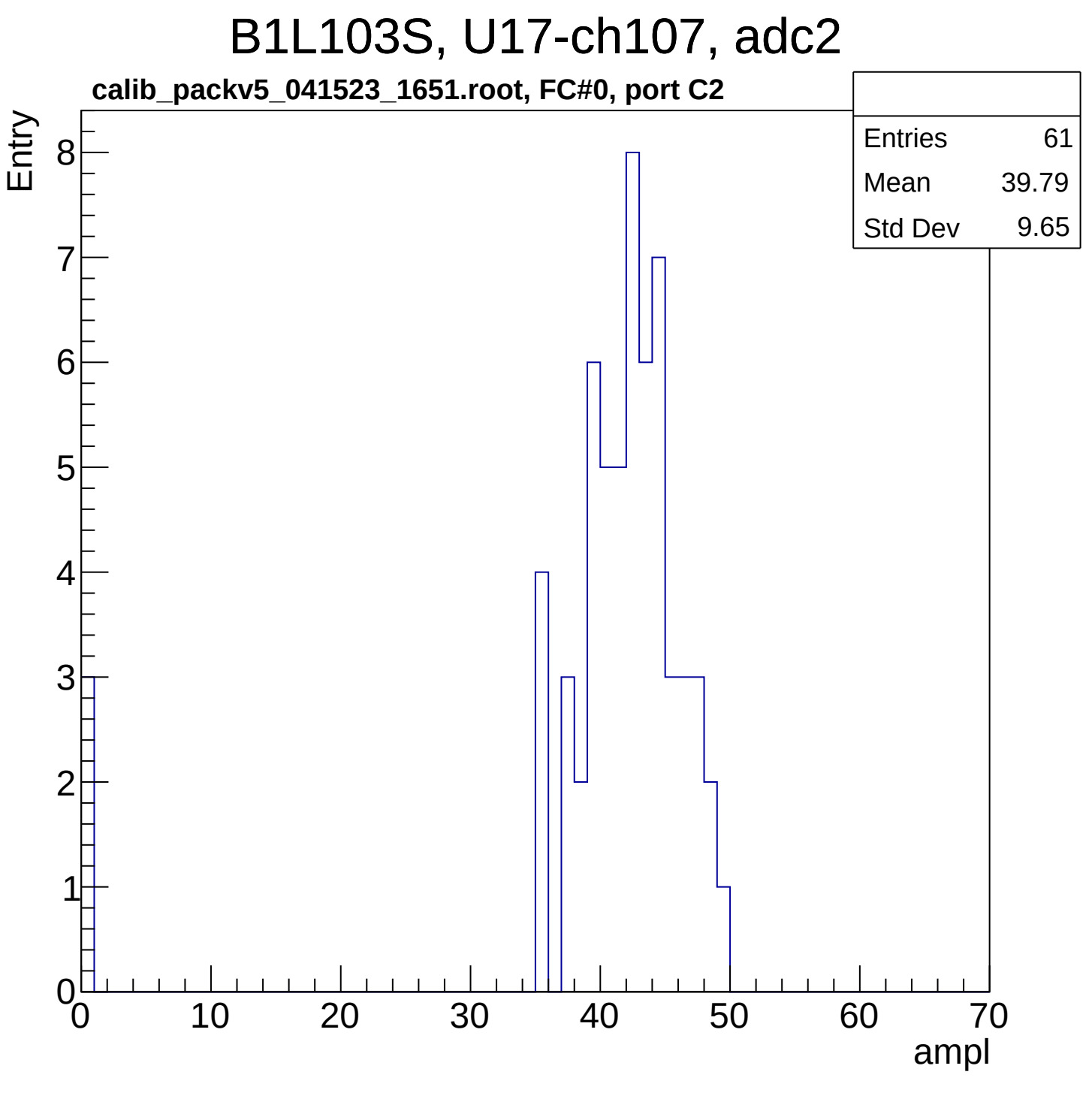
B1L103S, U17-ch107, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 39.79
Std Dev 9.65
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
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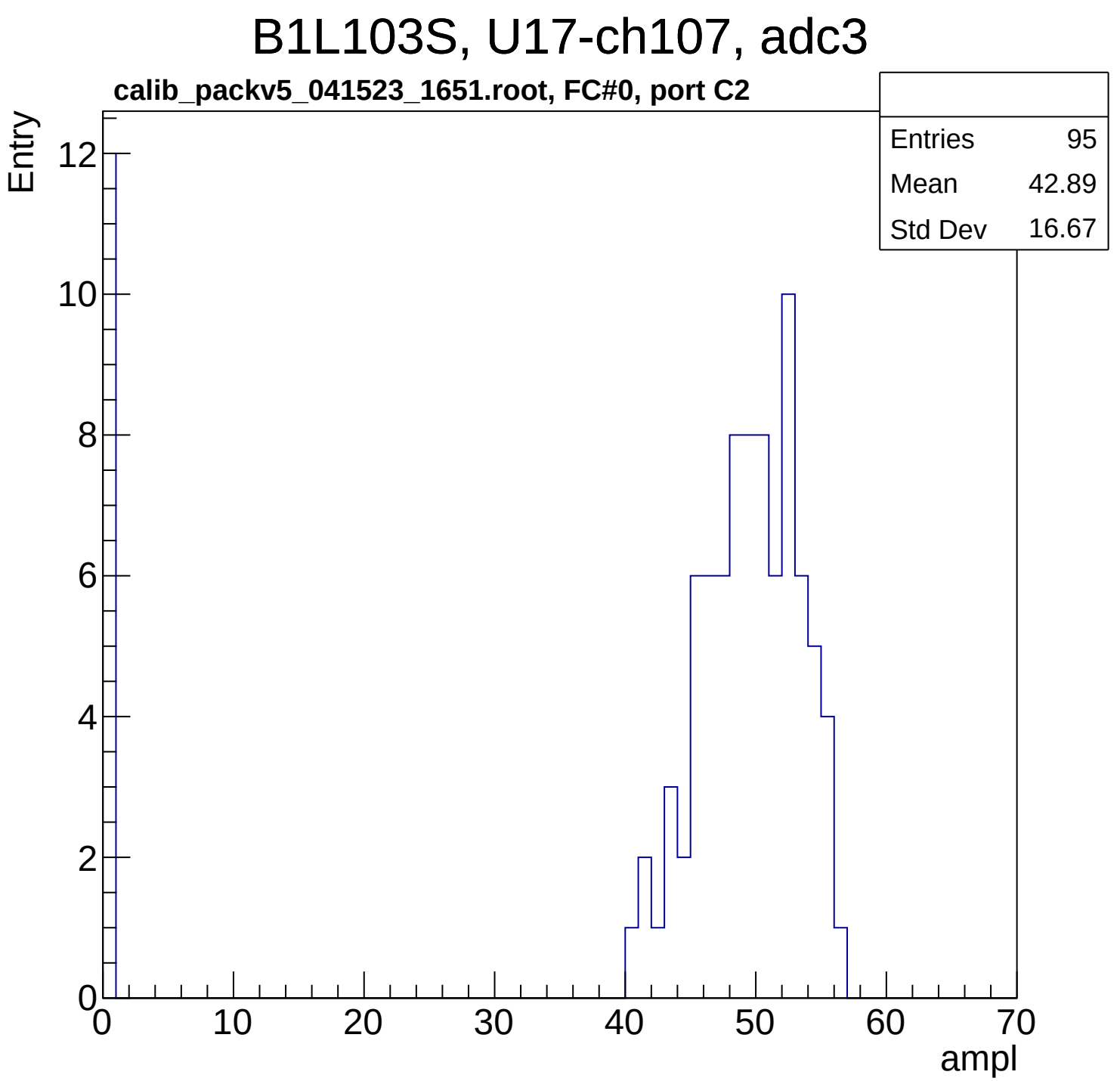
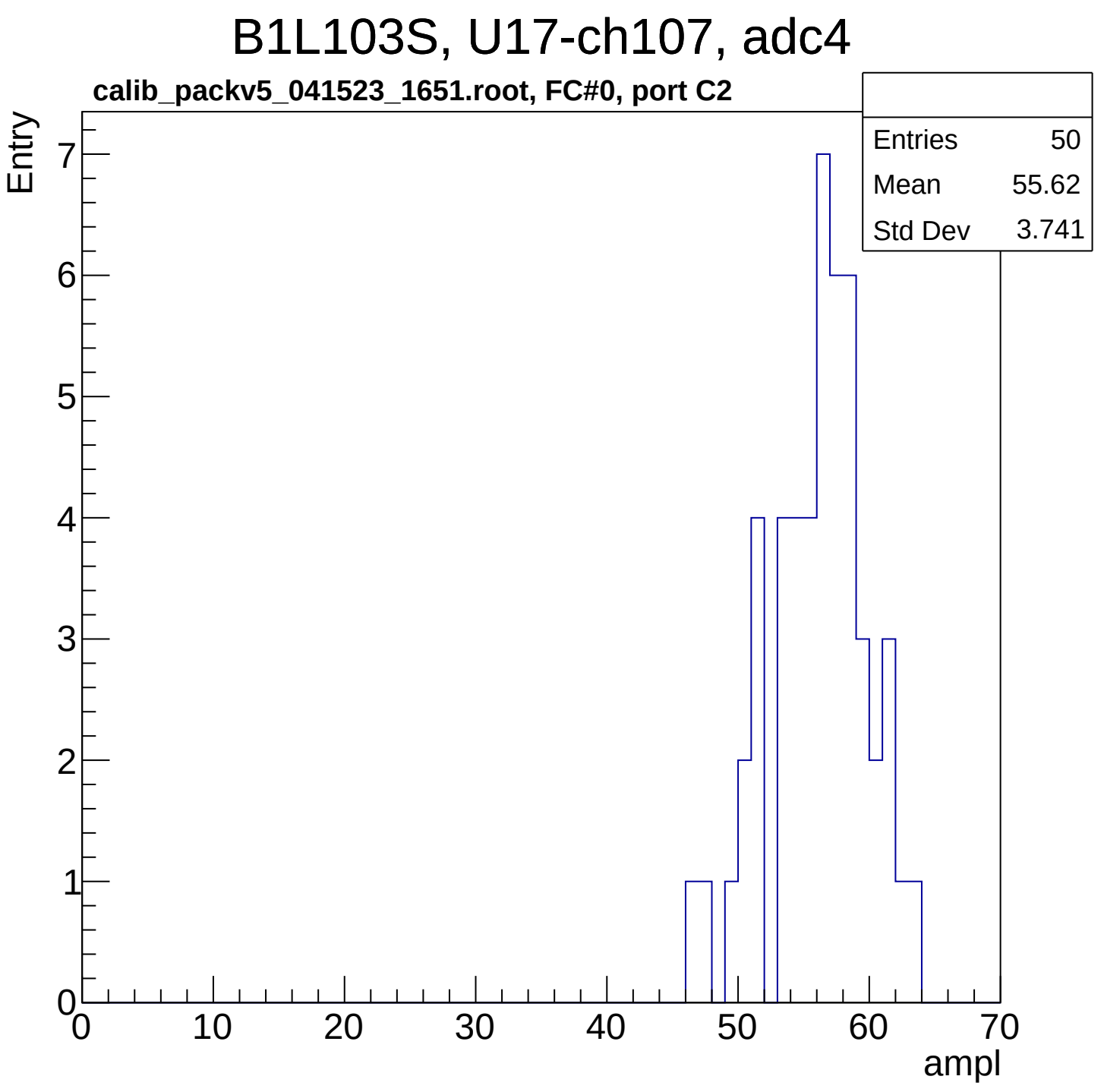
40
50
60
70


B1L103S, U17-ch107, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 95
Mean 42.89
Std Dev 16.67
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch107, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 55.62
Std Dev 3.741
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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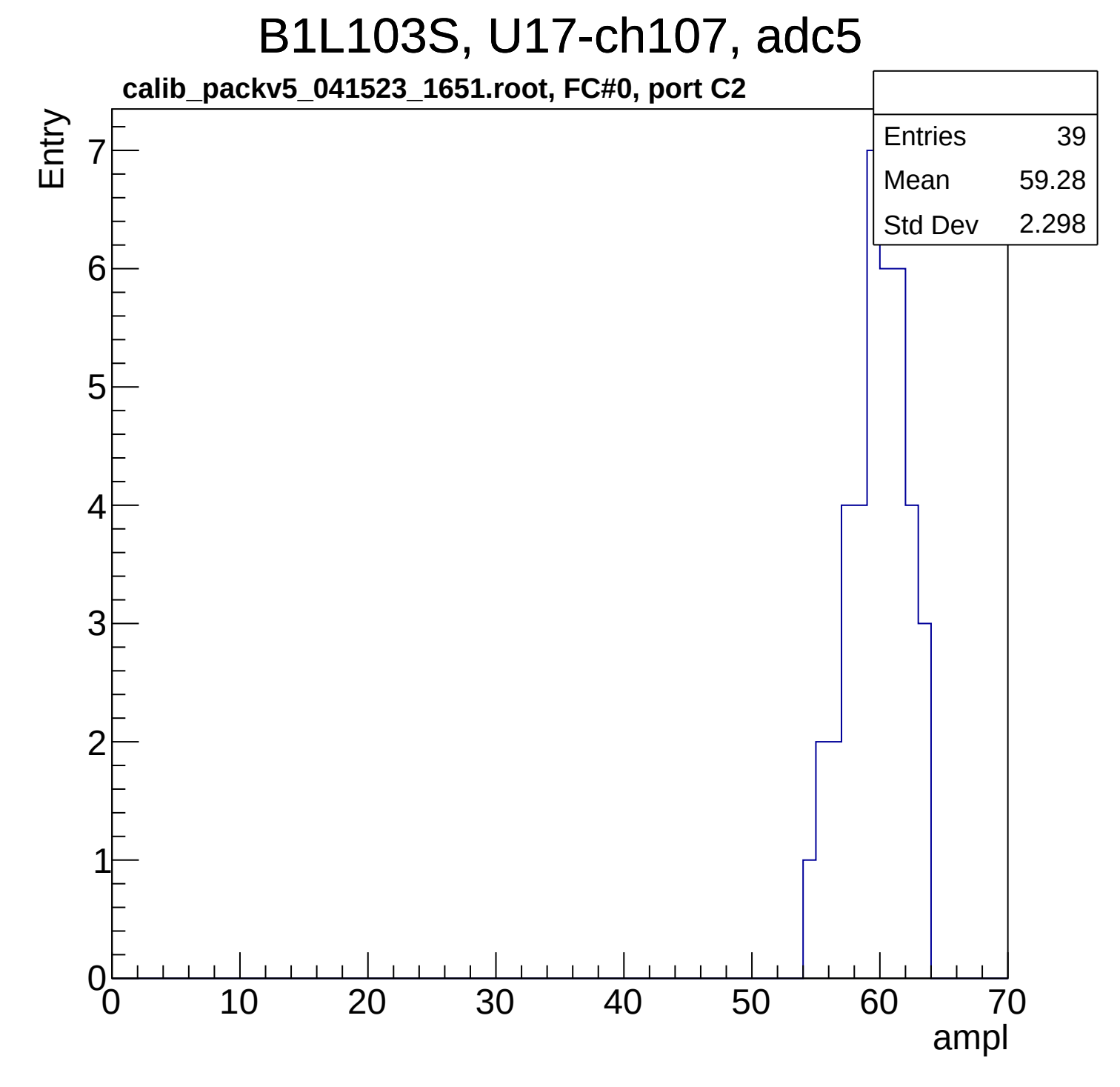
B1L103S, U17-ch107, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 39
Mean 59.28
Std Dev 2.298
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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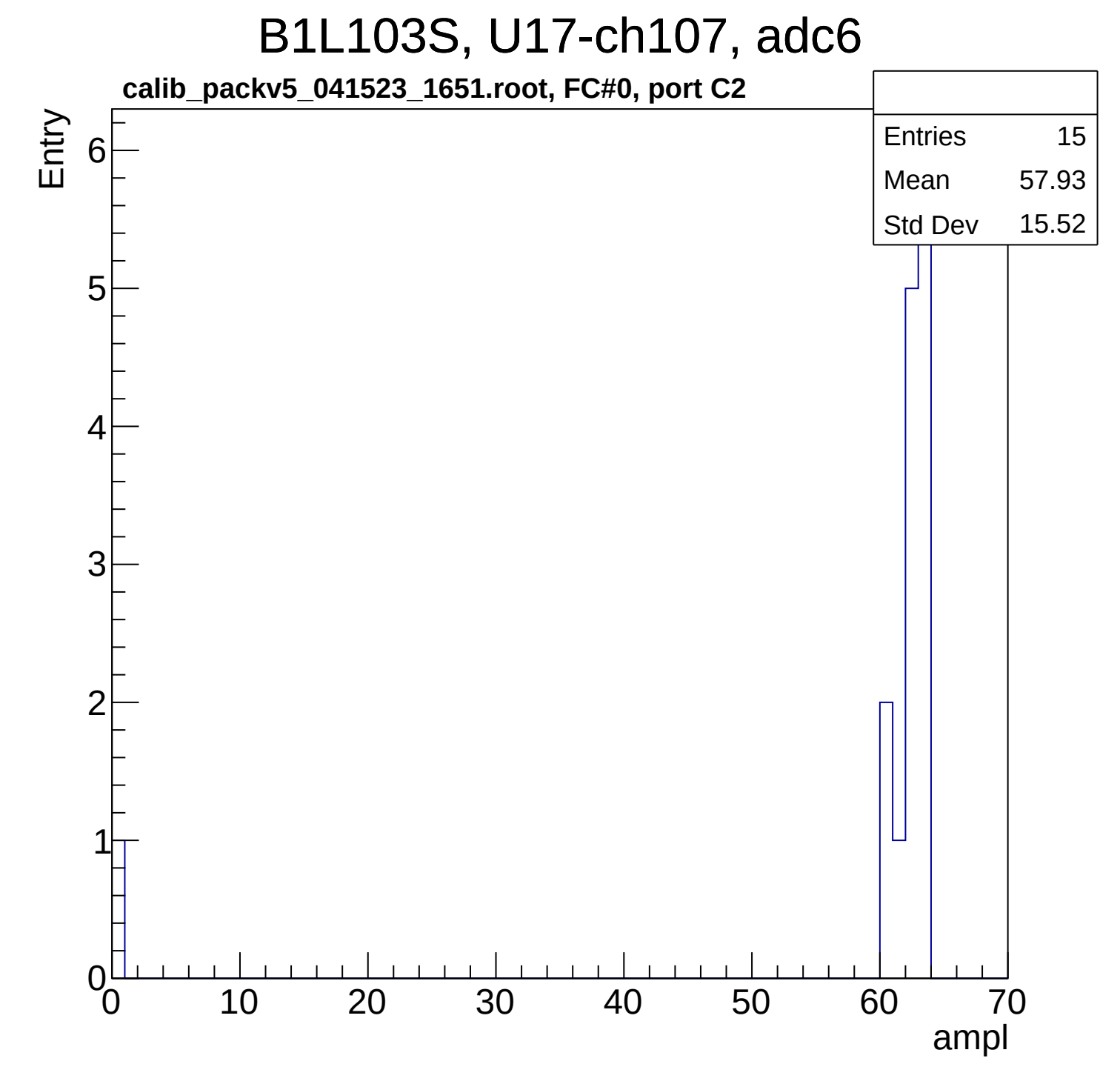
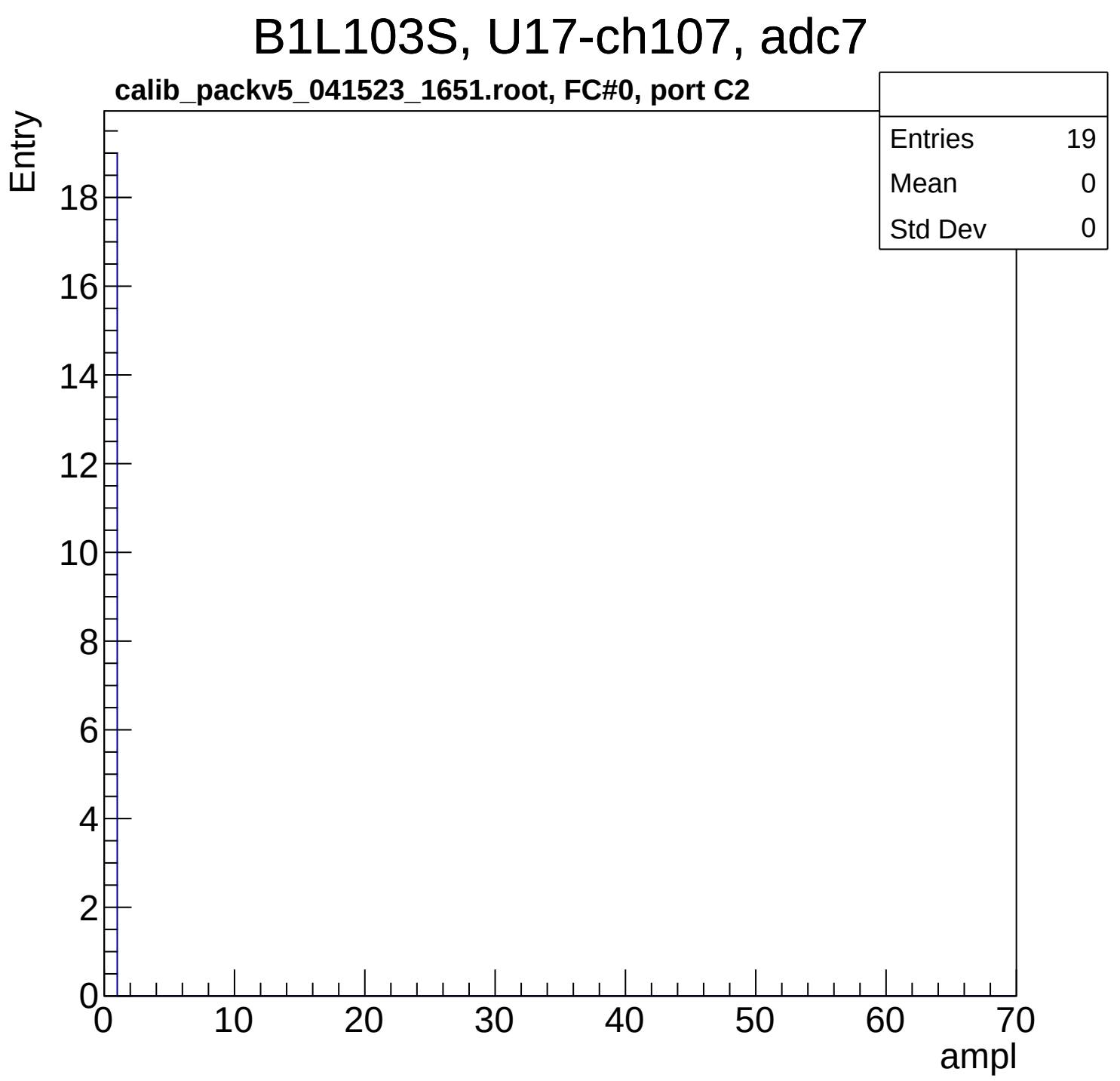
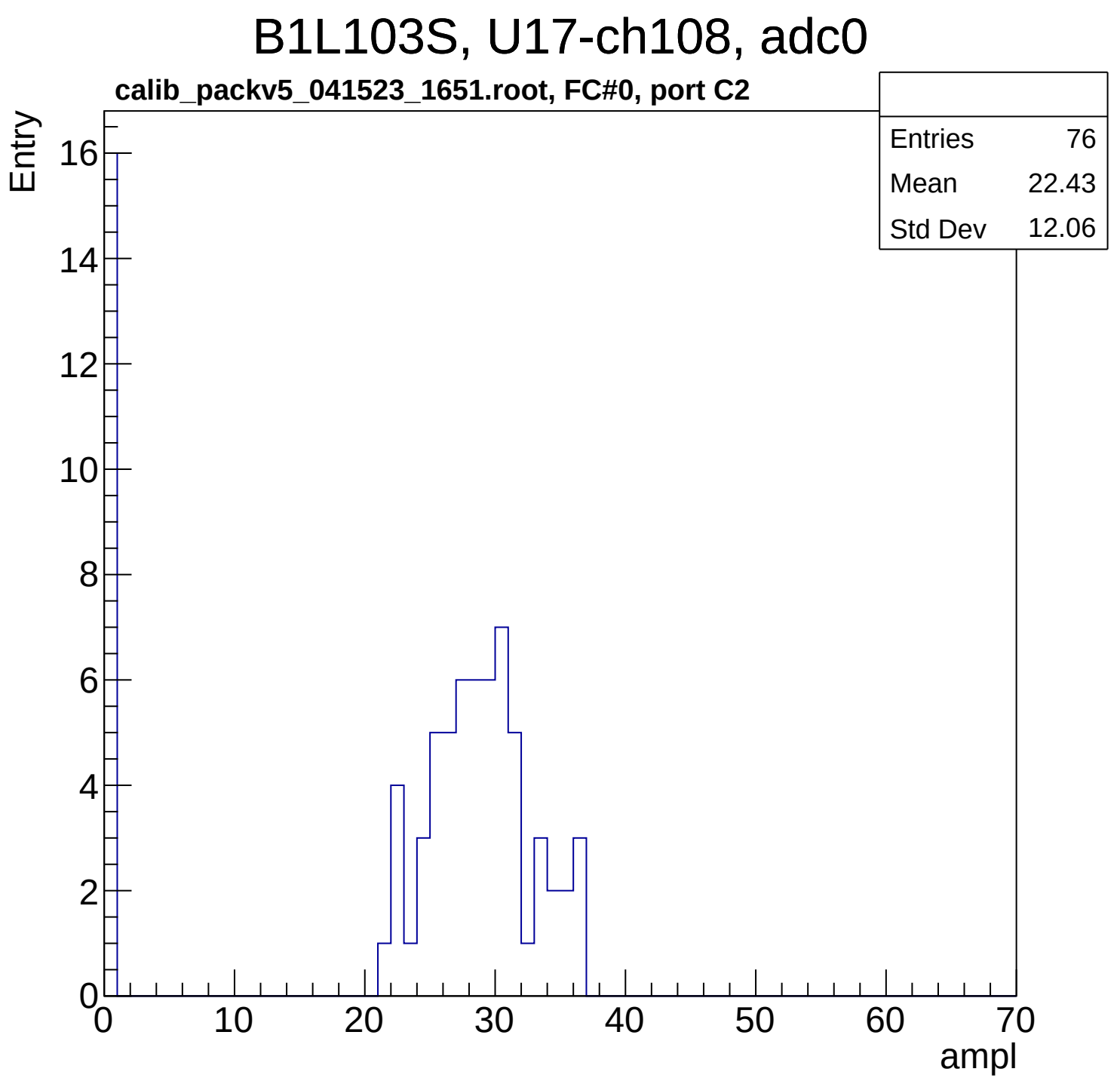

B1L103S, U17-ch107, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 15
Mean 57.93
Std Dev 15.52
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U17-ch107, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch108, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 22.43
Std Dev 12.06
Entry
ampl
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2
4
6
8
10
12
14
16
0
10
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40
50
60
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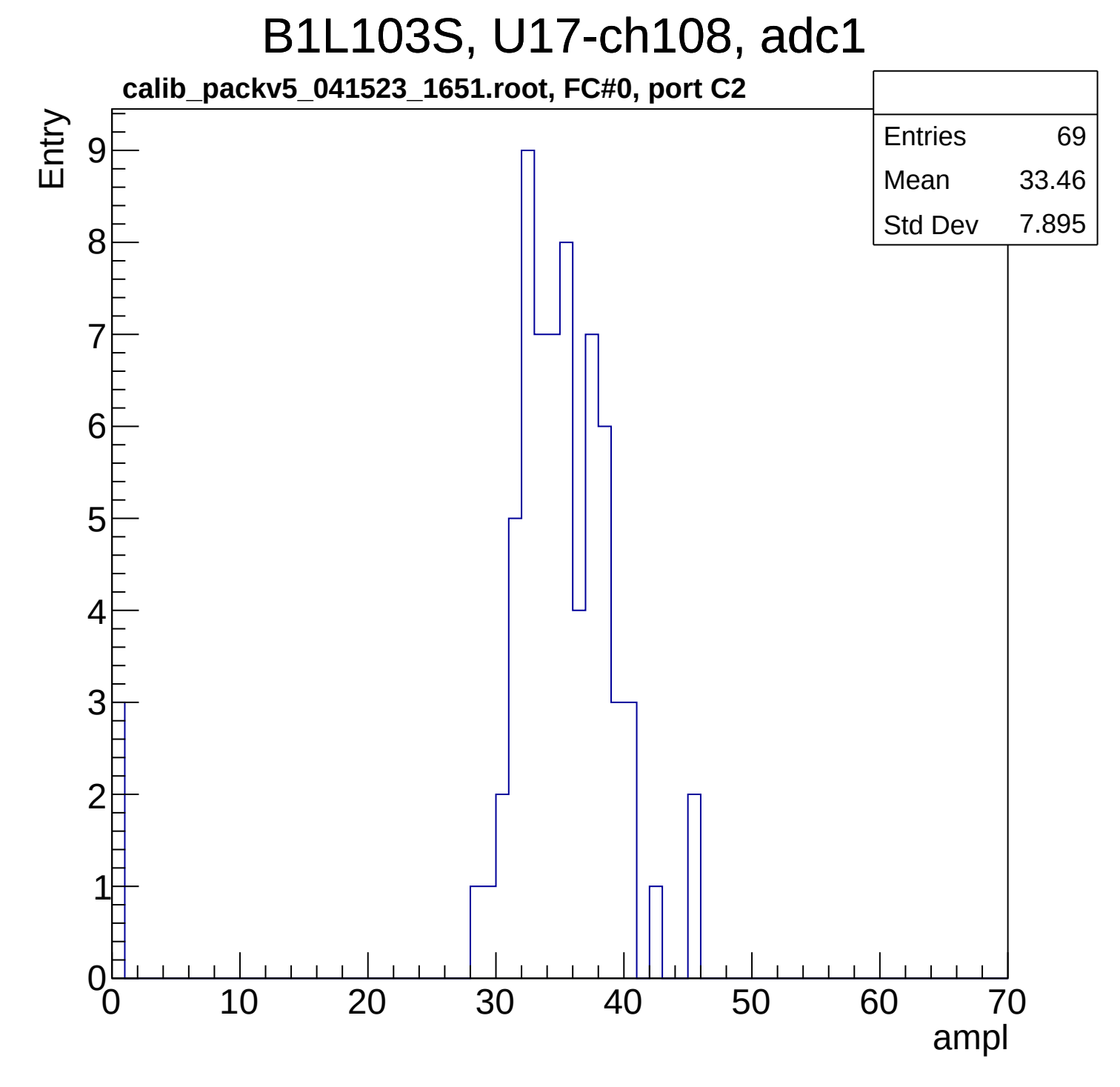
B1L103S, U17-ch108, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 33.46
Std Dev 7.895
Entry
ampl
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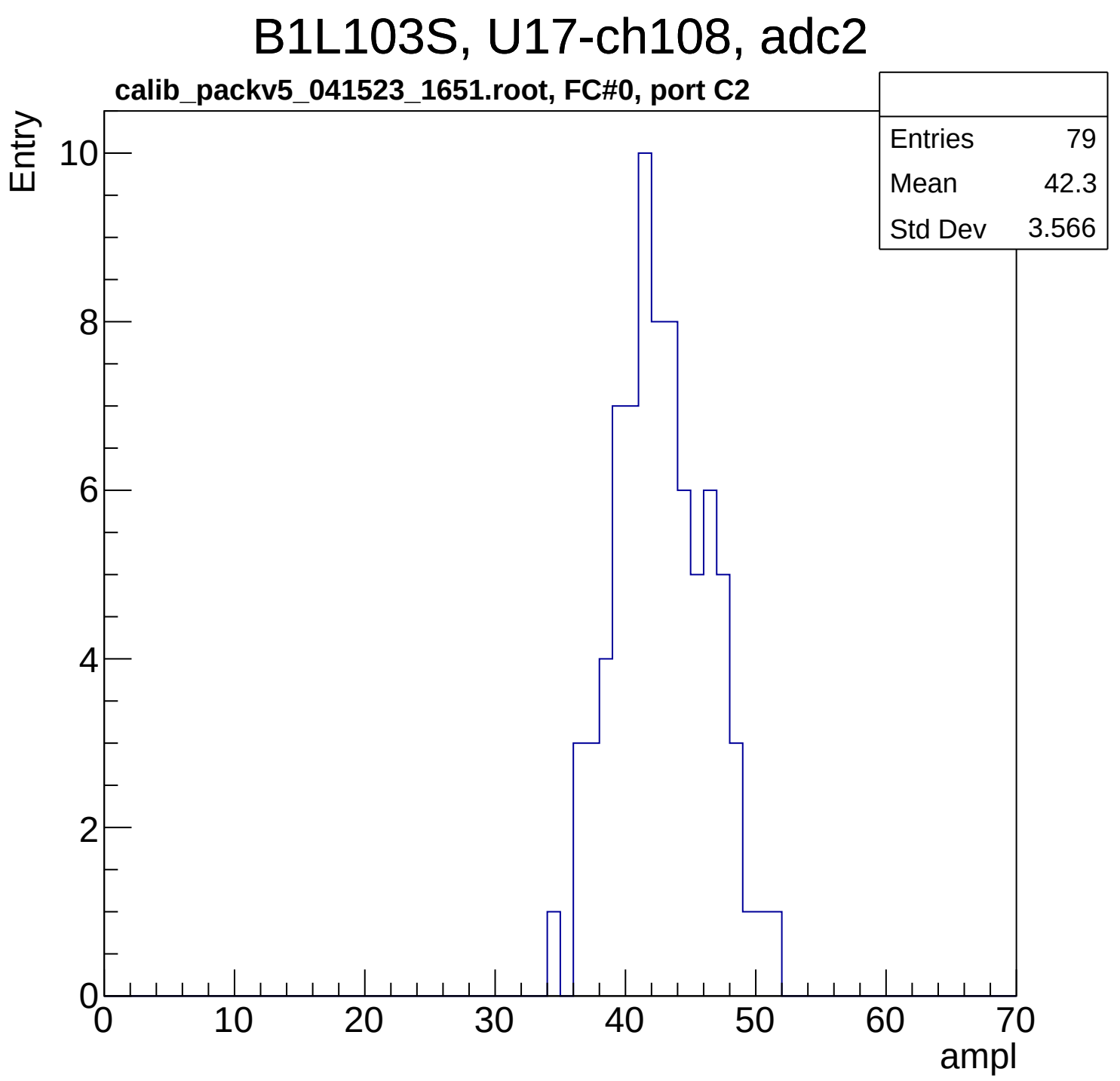
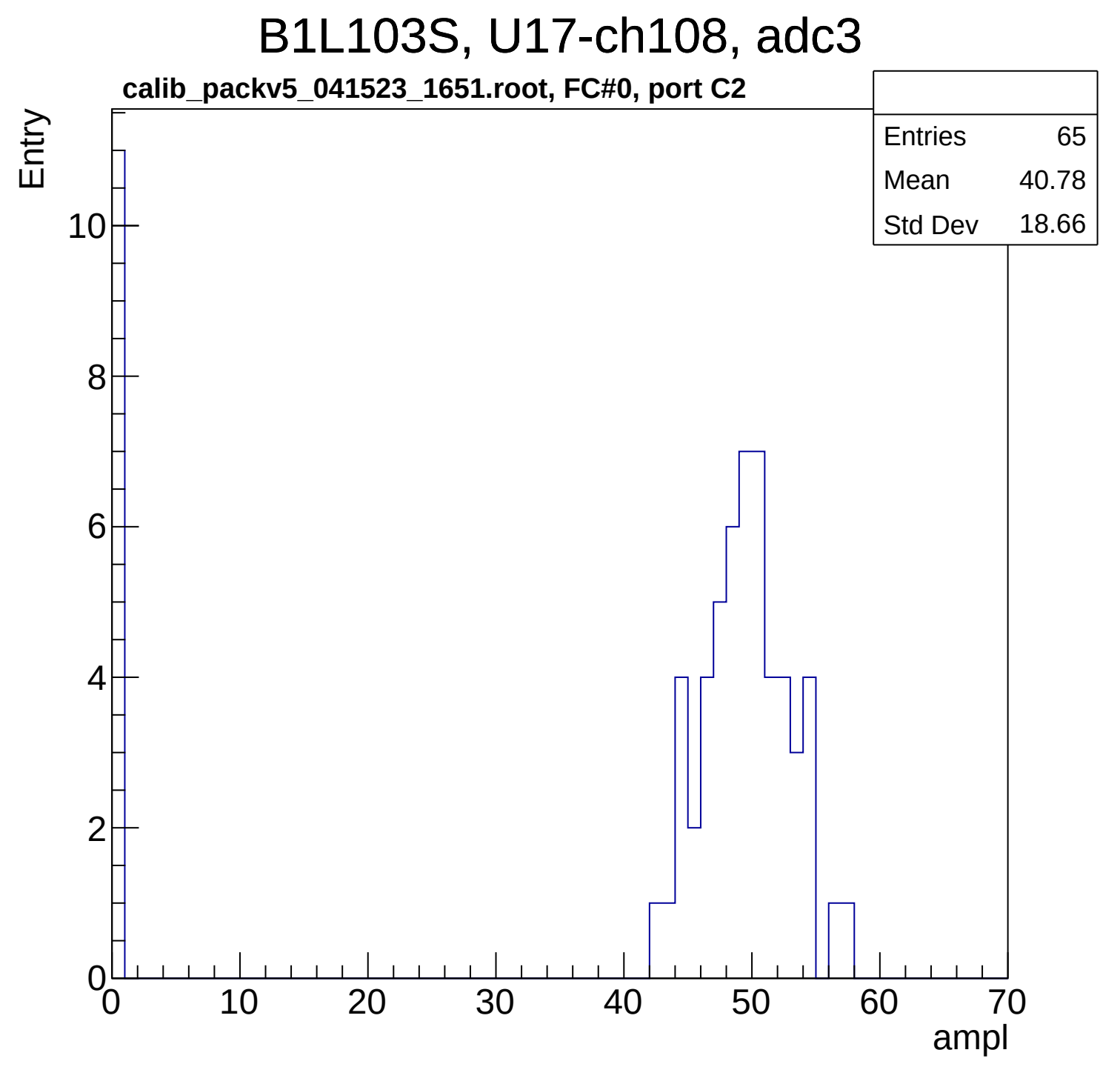
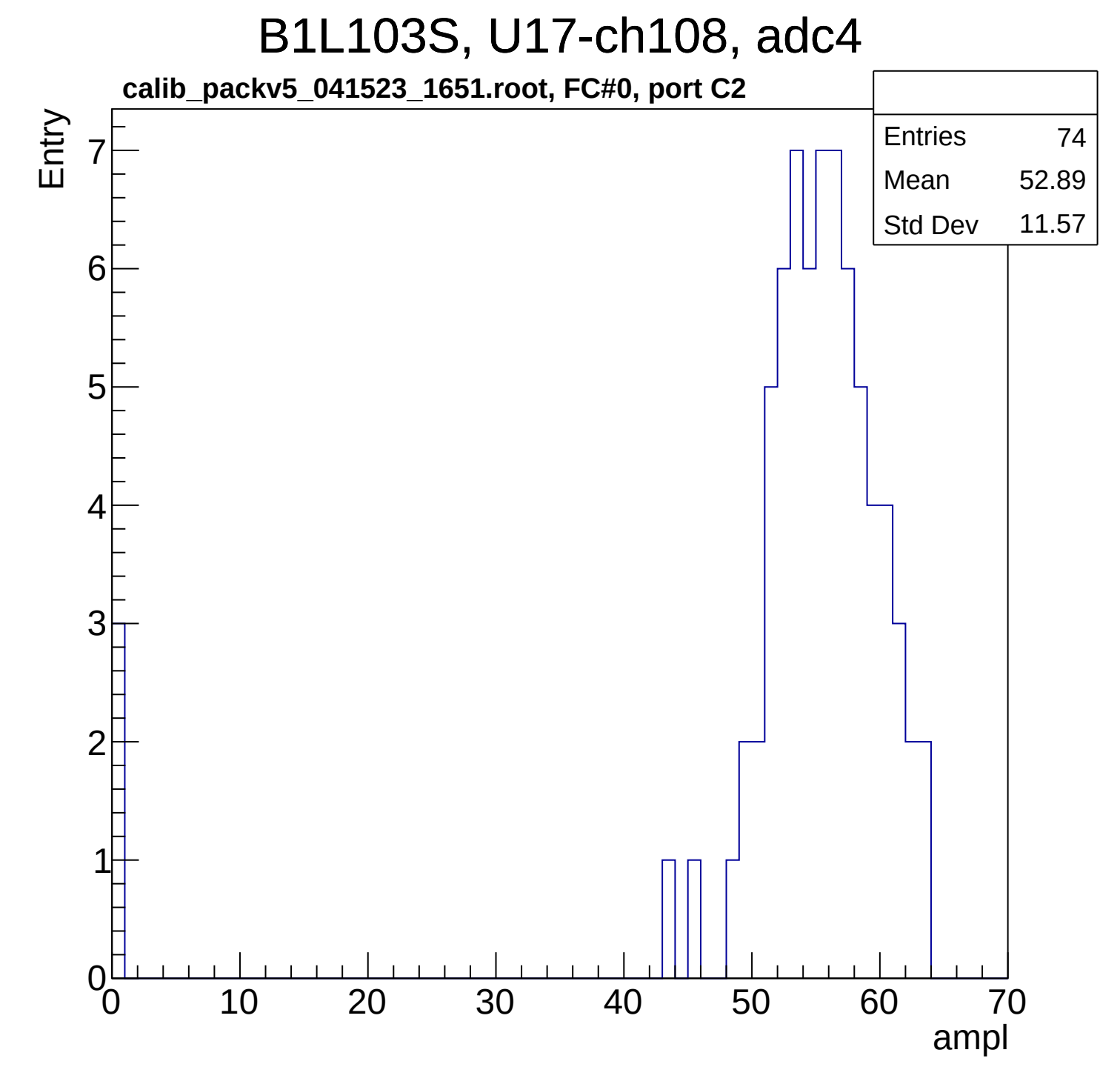
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U17-ch108, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 42.3
Std Dev 3.566
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U17-ch108, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 40.78
Std Dev 18.66
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U17-ch108, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 52.89
Std Dev 11.57
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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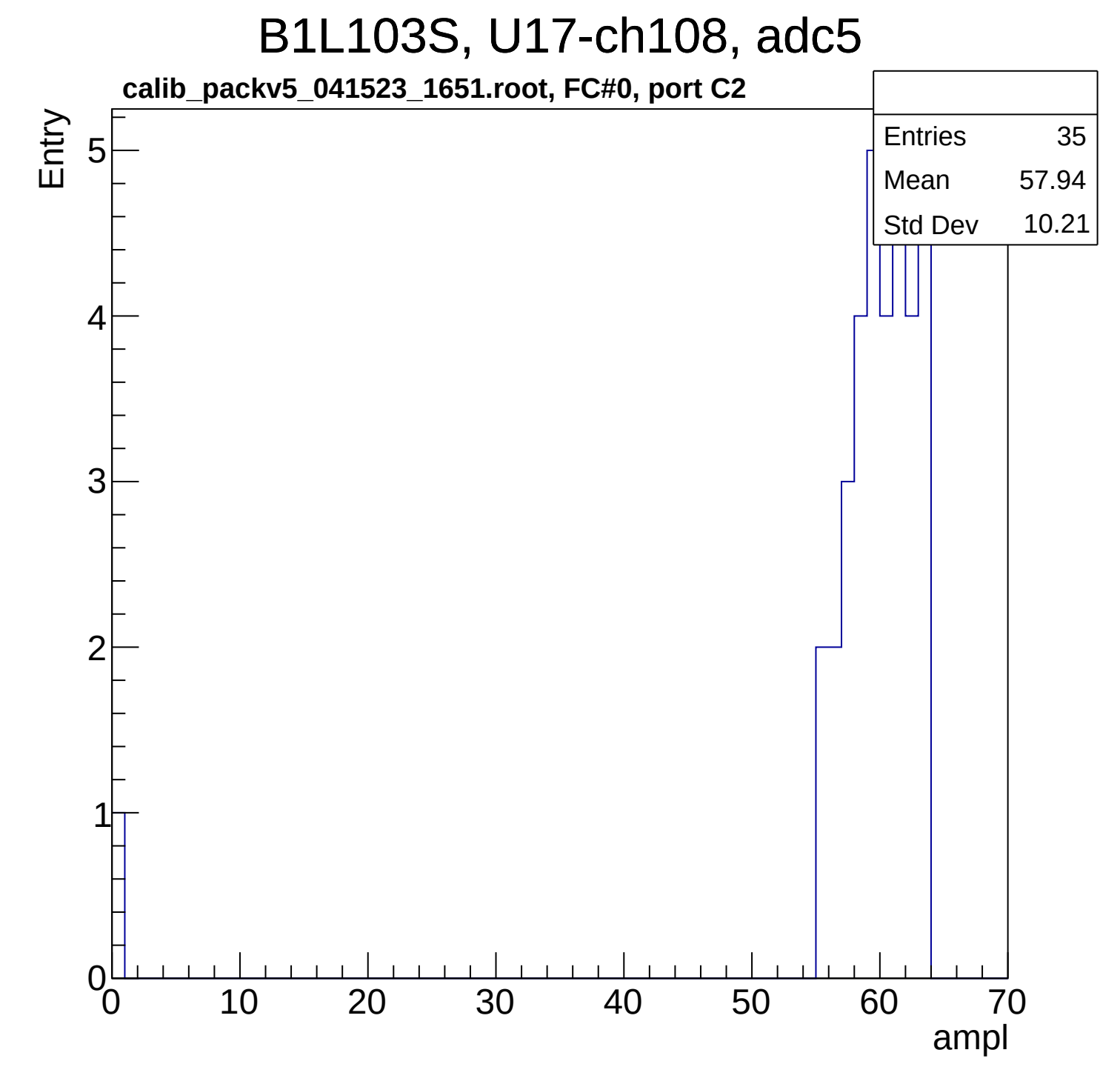
B1L103S, U17-ch108, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 35
Mean 57.94
Std Dev 10.21
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
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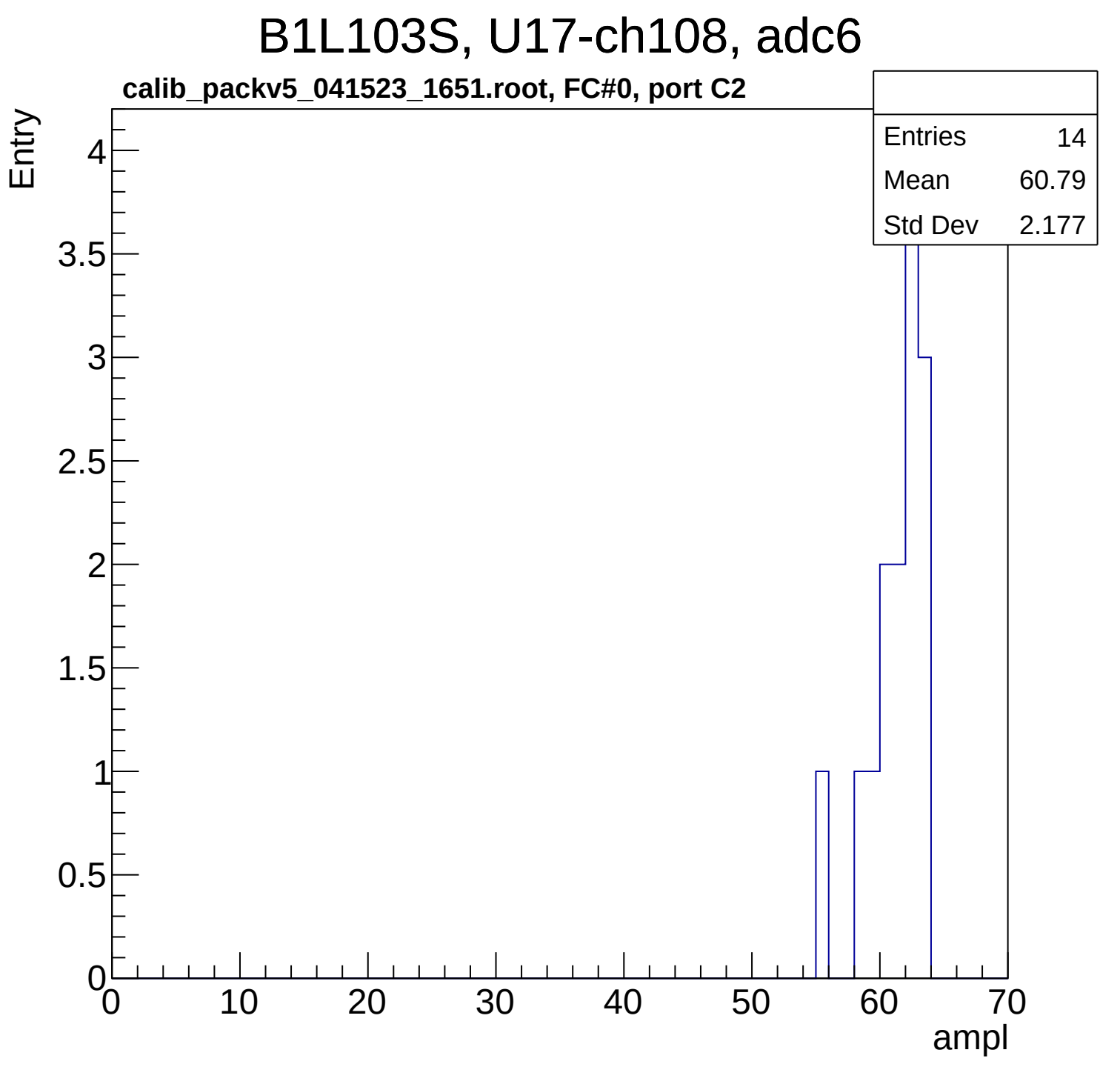
B1L103S, U17-ch108, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 14
Mean 60.79
Std Dev 2.177
Entry
ampl
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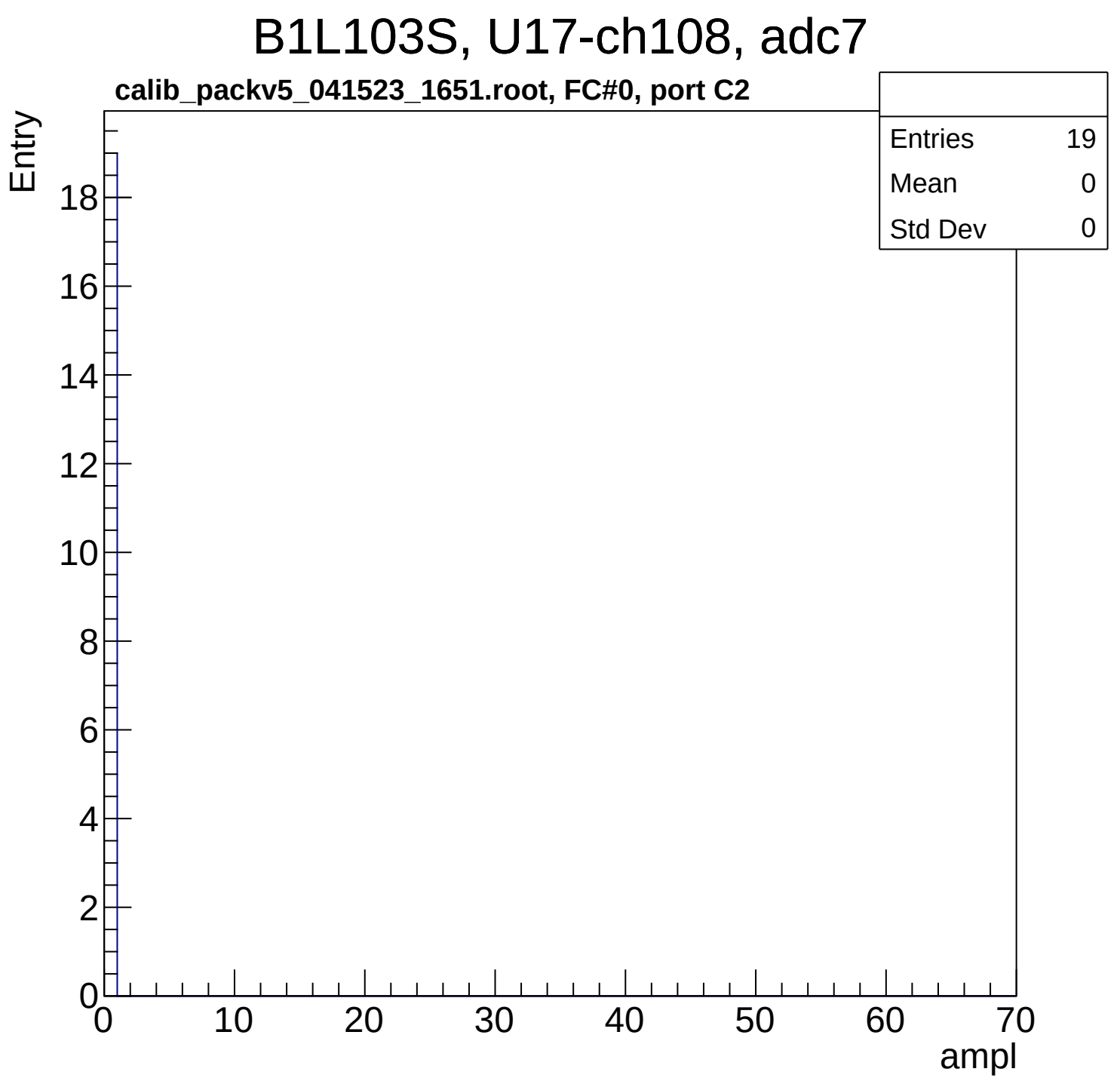
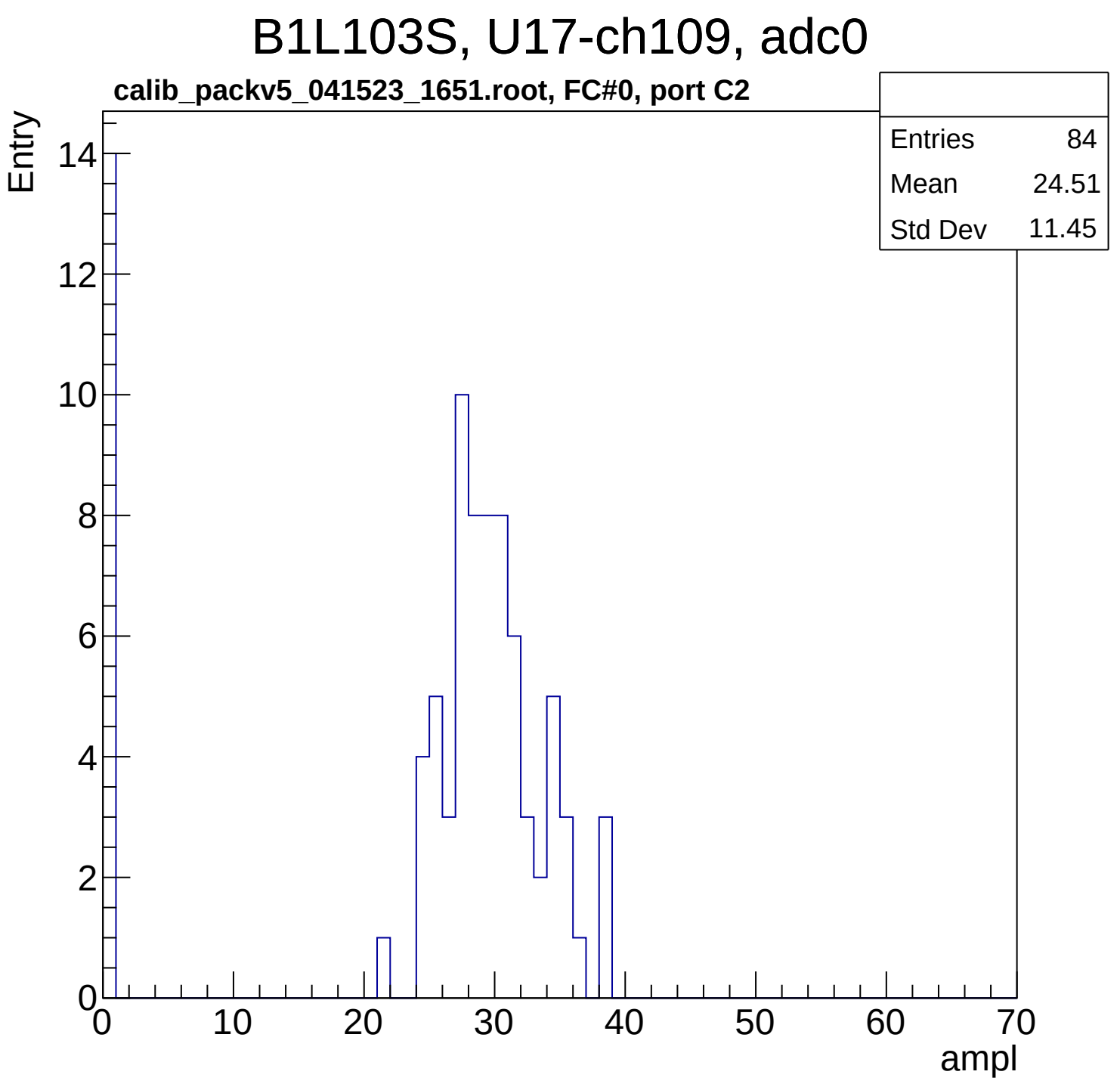
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U17-ch108, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch109, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 24.51
Std Dev 11.45
Entry
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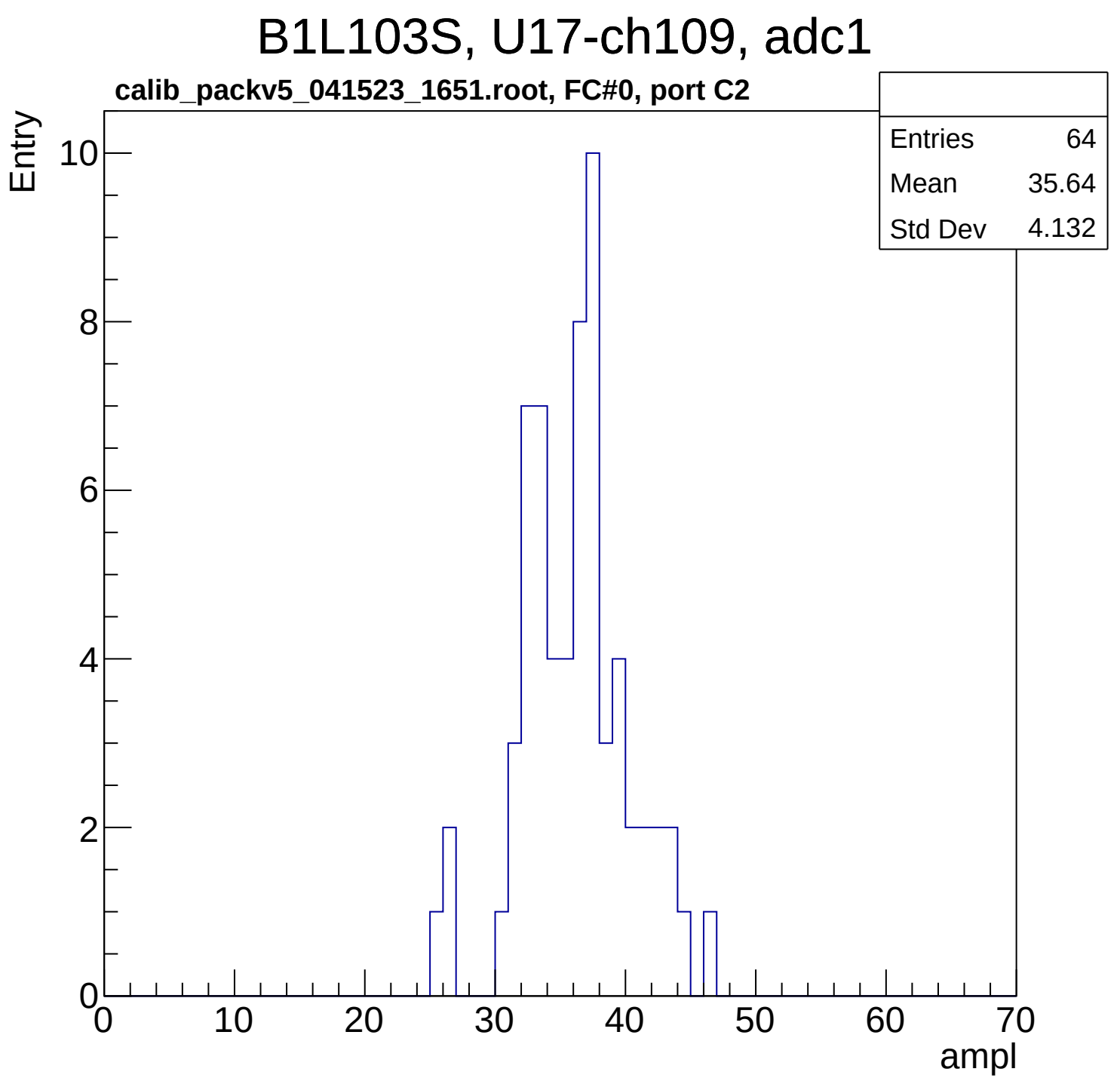
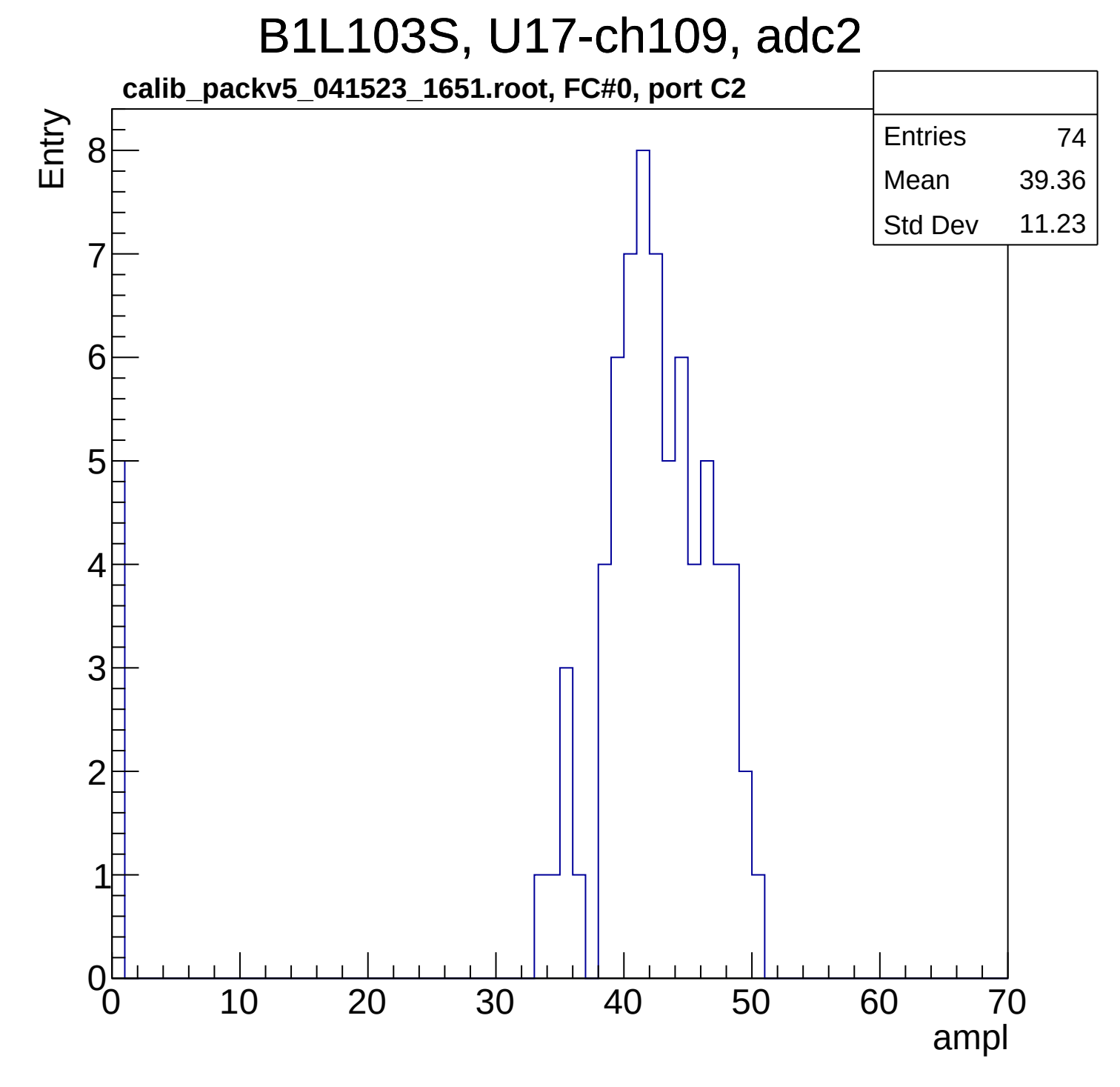
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch109, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 35.64
Std Dev 4.132
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch109, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 39.36
Std Dev 11.23
Entry
ampl
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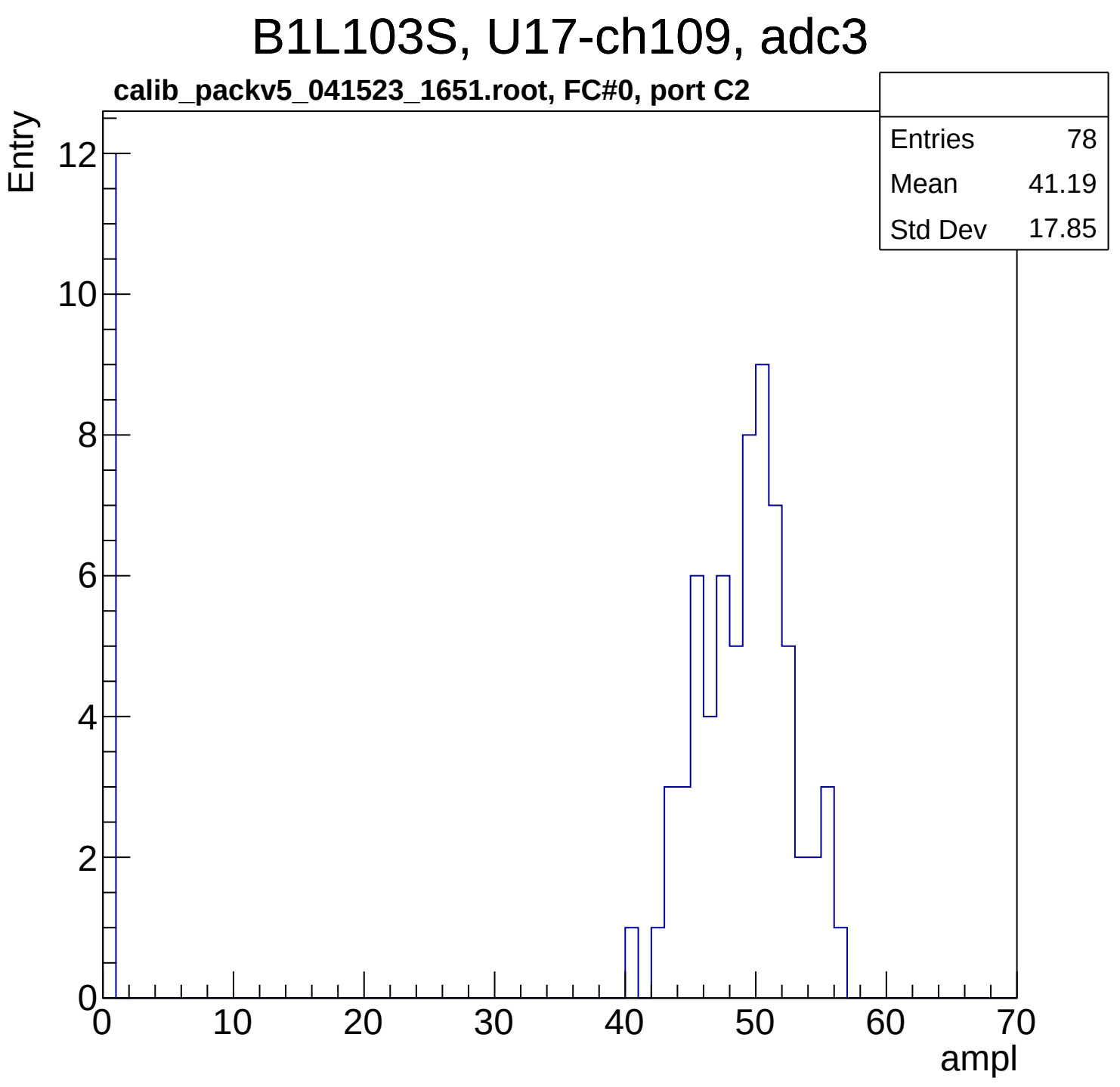
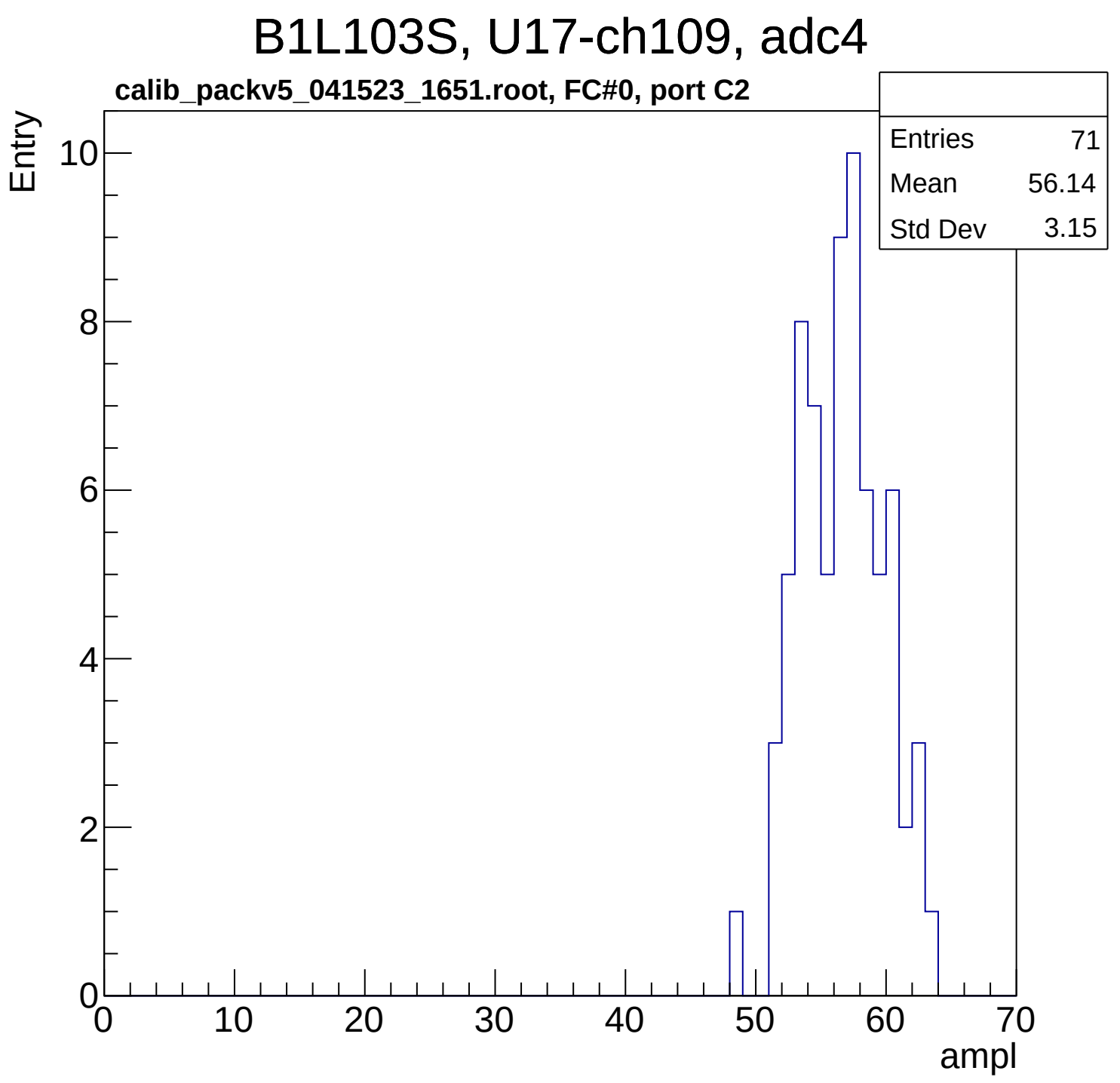
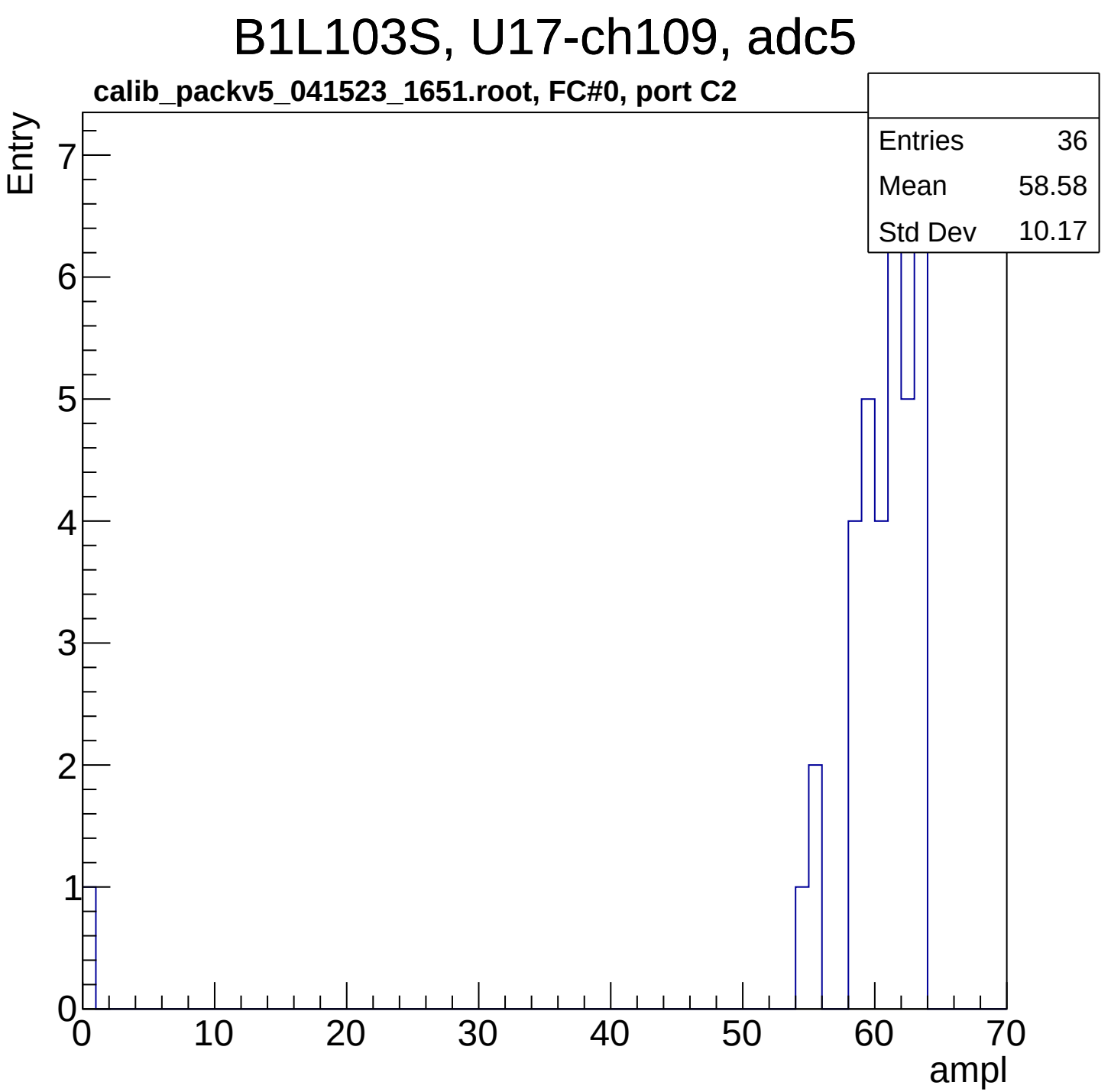
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U17-ch109, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 41.19
Std Dev 17.85
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch109, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 56.14
Std Dev 3.15
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U17-ch109, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 36
Mean 58.58
Std Dev 10.17
Entry
ampl
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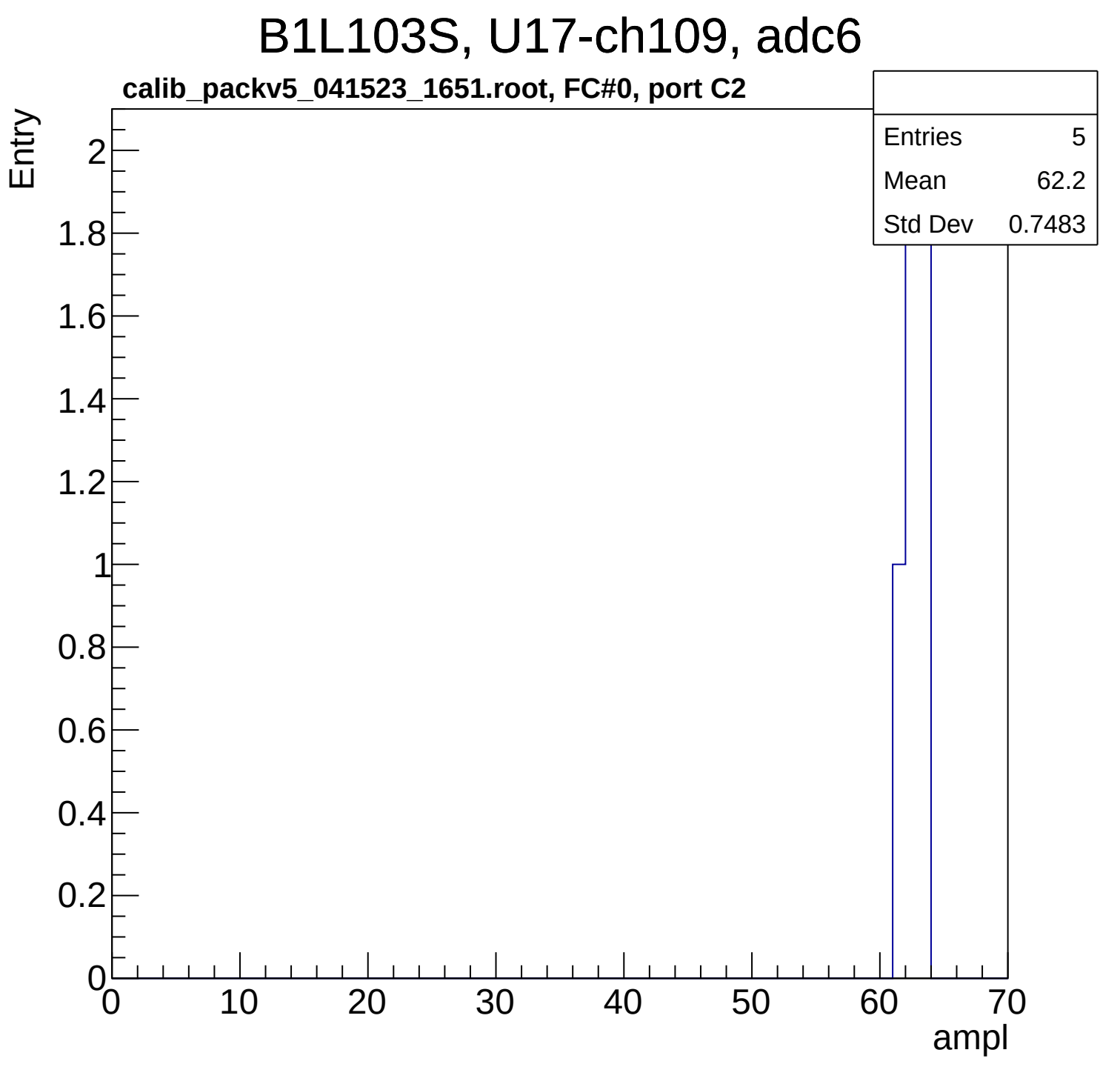
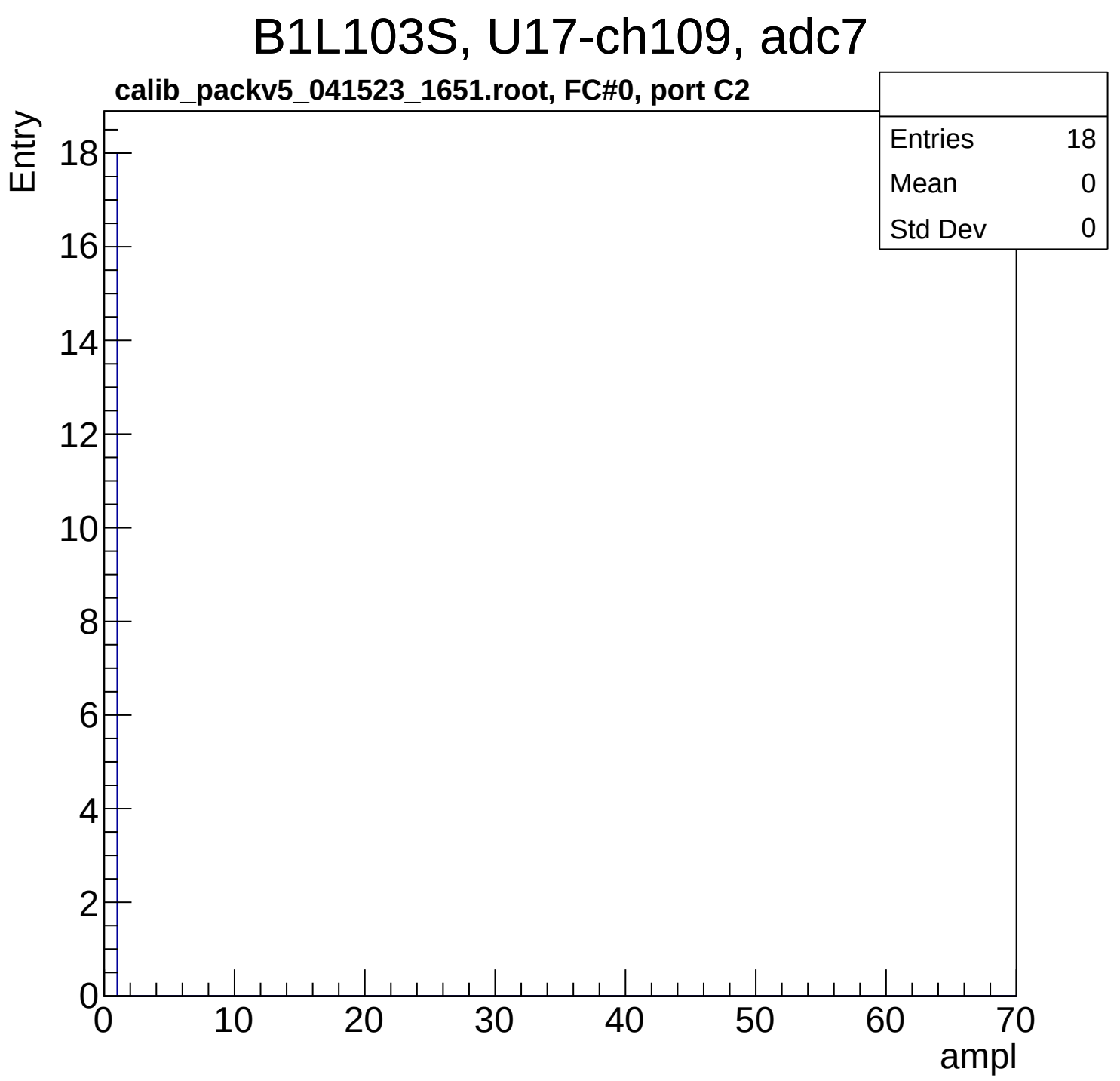
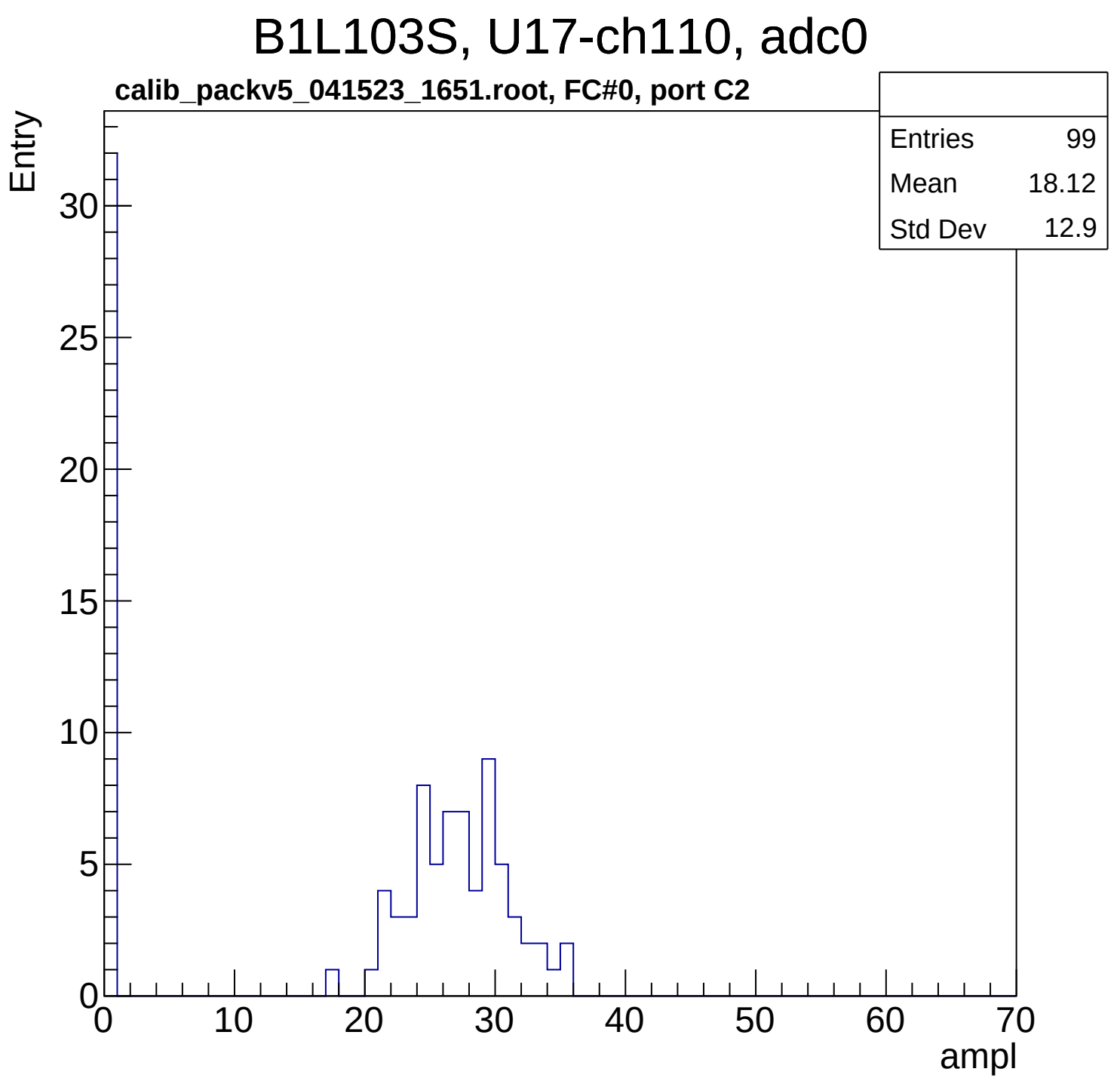
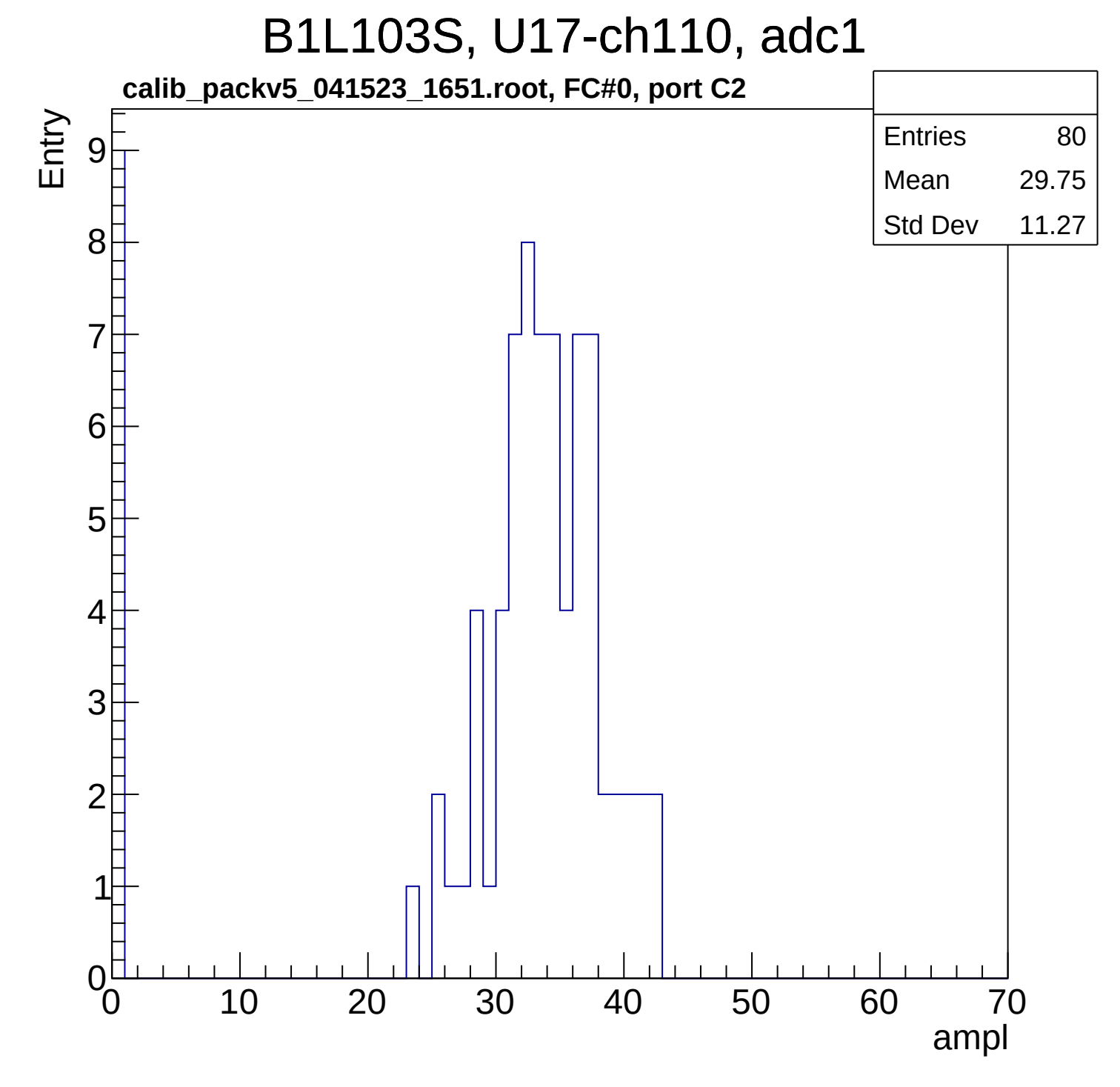
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U17-ch109, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 5
Mean 62.2
Std Dev 0.7483
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U17-ch109, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch110, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 99
Mean 18.12
Std Dev 12.9
Entry
0
5
10
15
20
25
30
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch110, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 29.75
Std Dev 11.27
Entry
ampl
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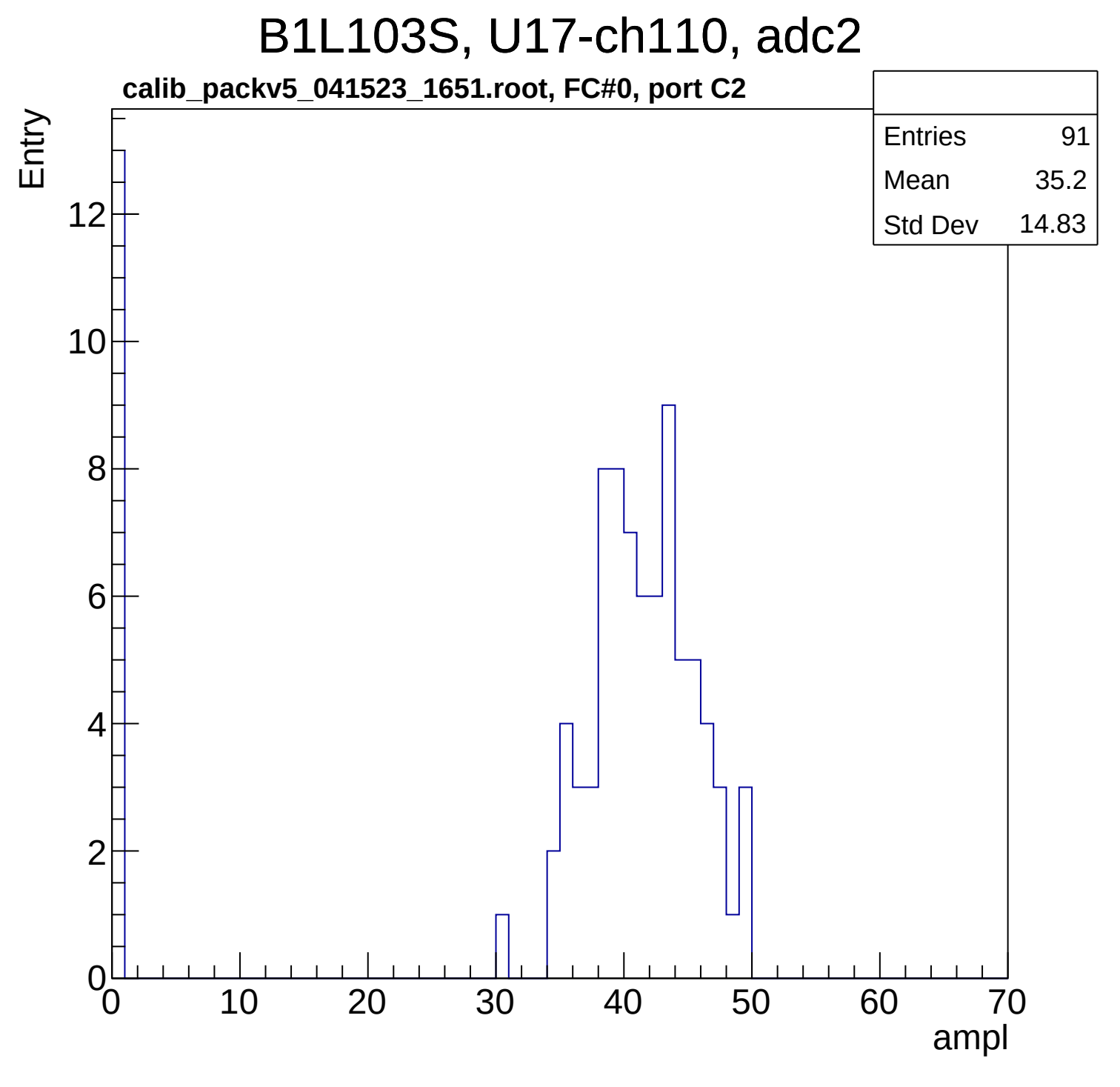
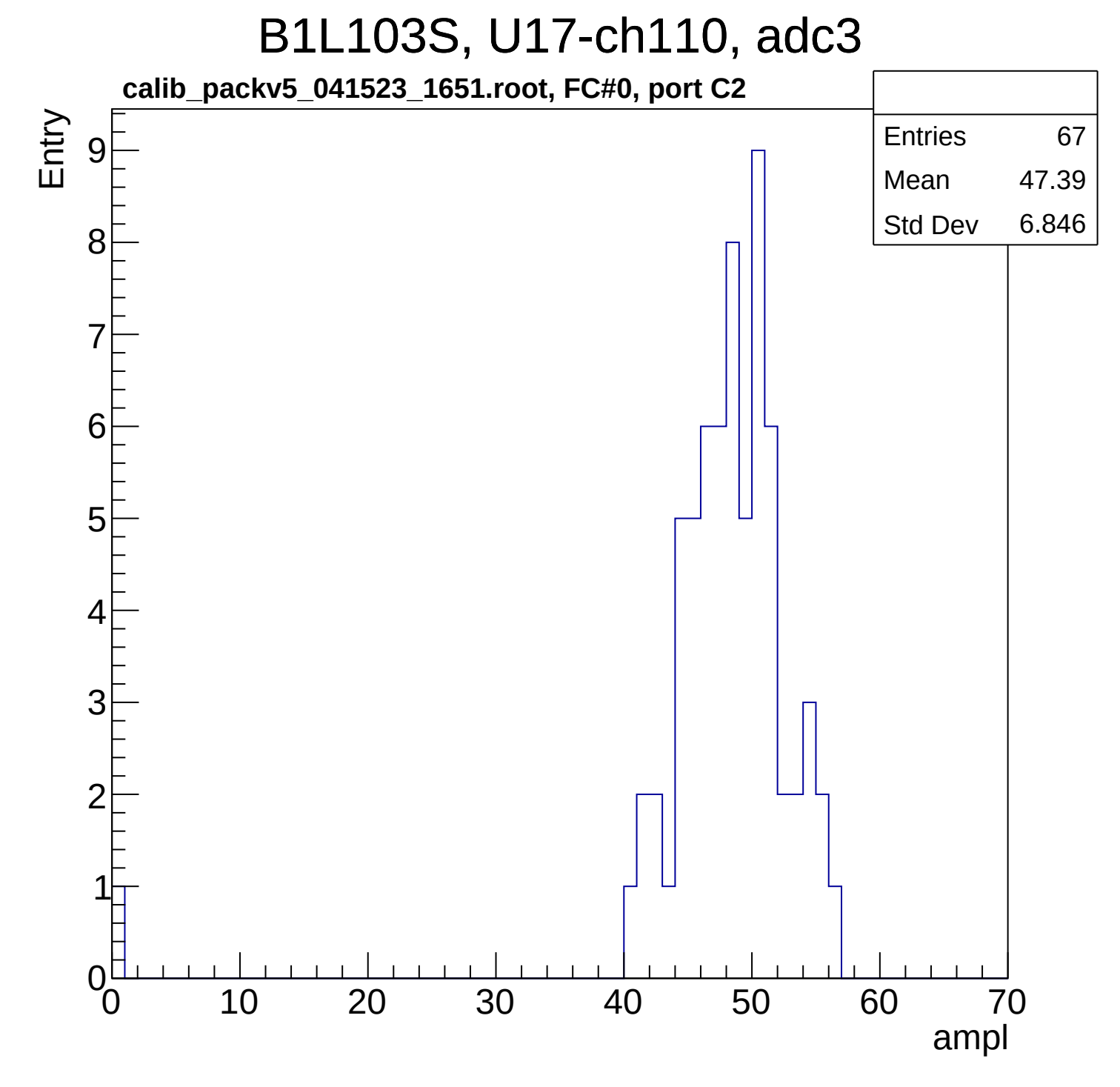
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U17-ch110, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 91
Mean 35.2
Std Dev 14.83
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70


B1L103S, U17-ch110, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 47.39
Std Dev 6.846
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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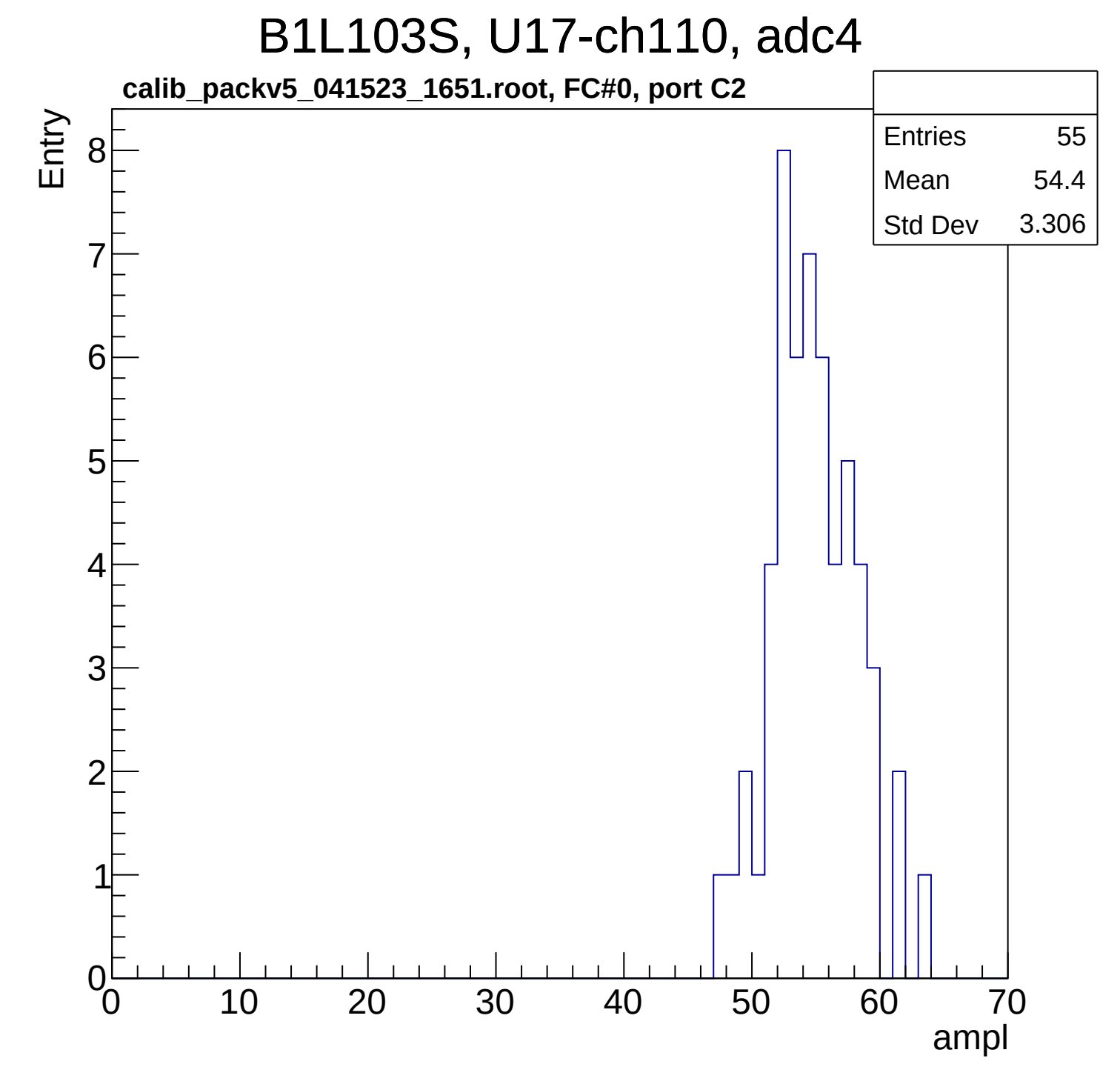
60
70


B1L103S, U17-ch110, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 54.4
Std Dev 3.306
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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50
60
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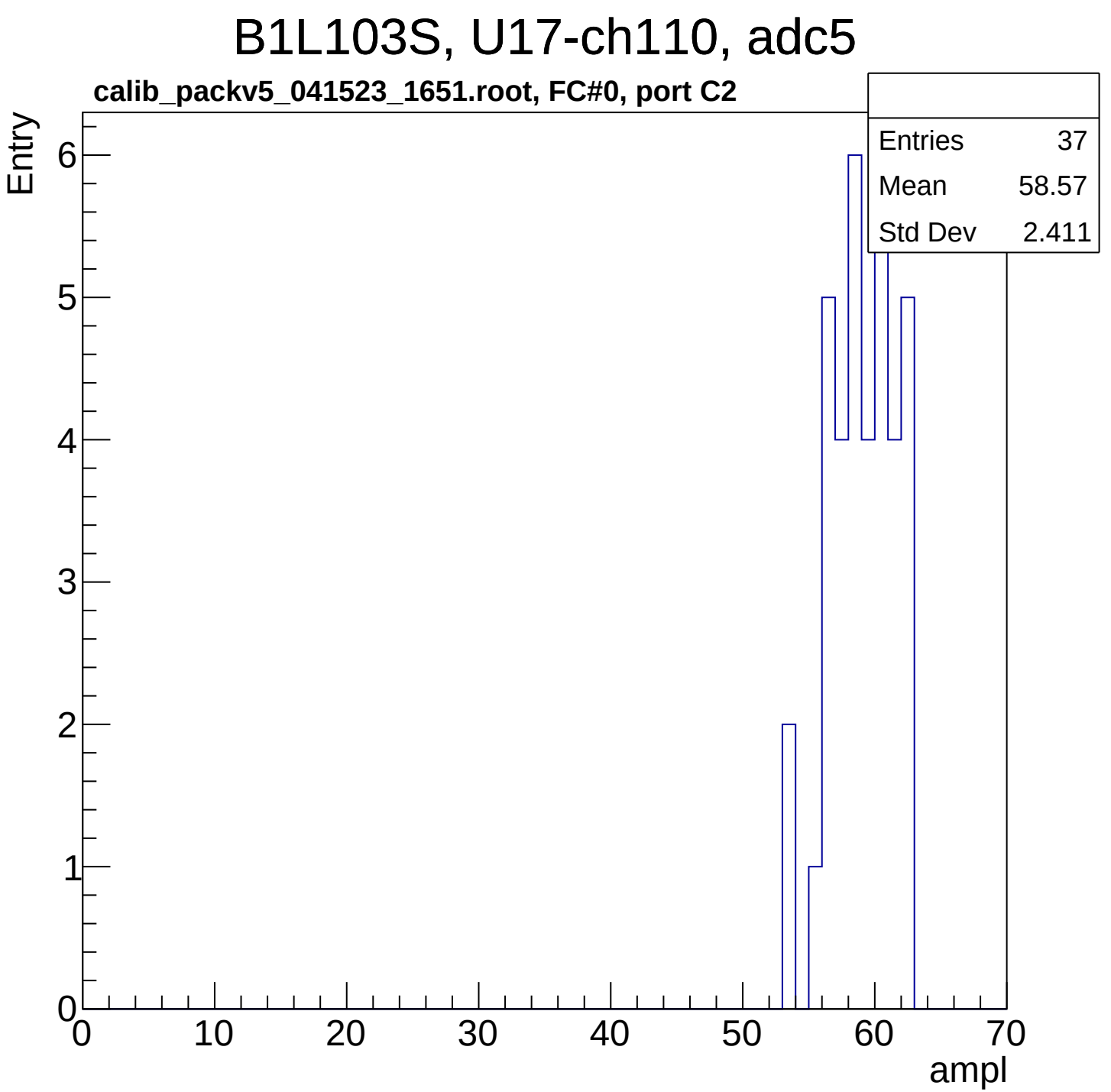
B1L103S, U17-ch110, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 37
Mean 58.57
Std Dev 2.411
Entry
ampl
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1
2
3
4
5
6
0
10
20
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50
60
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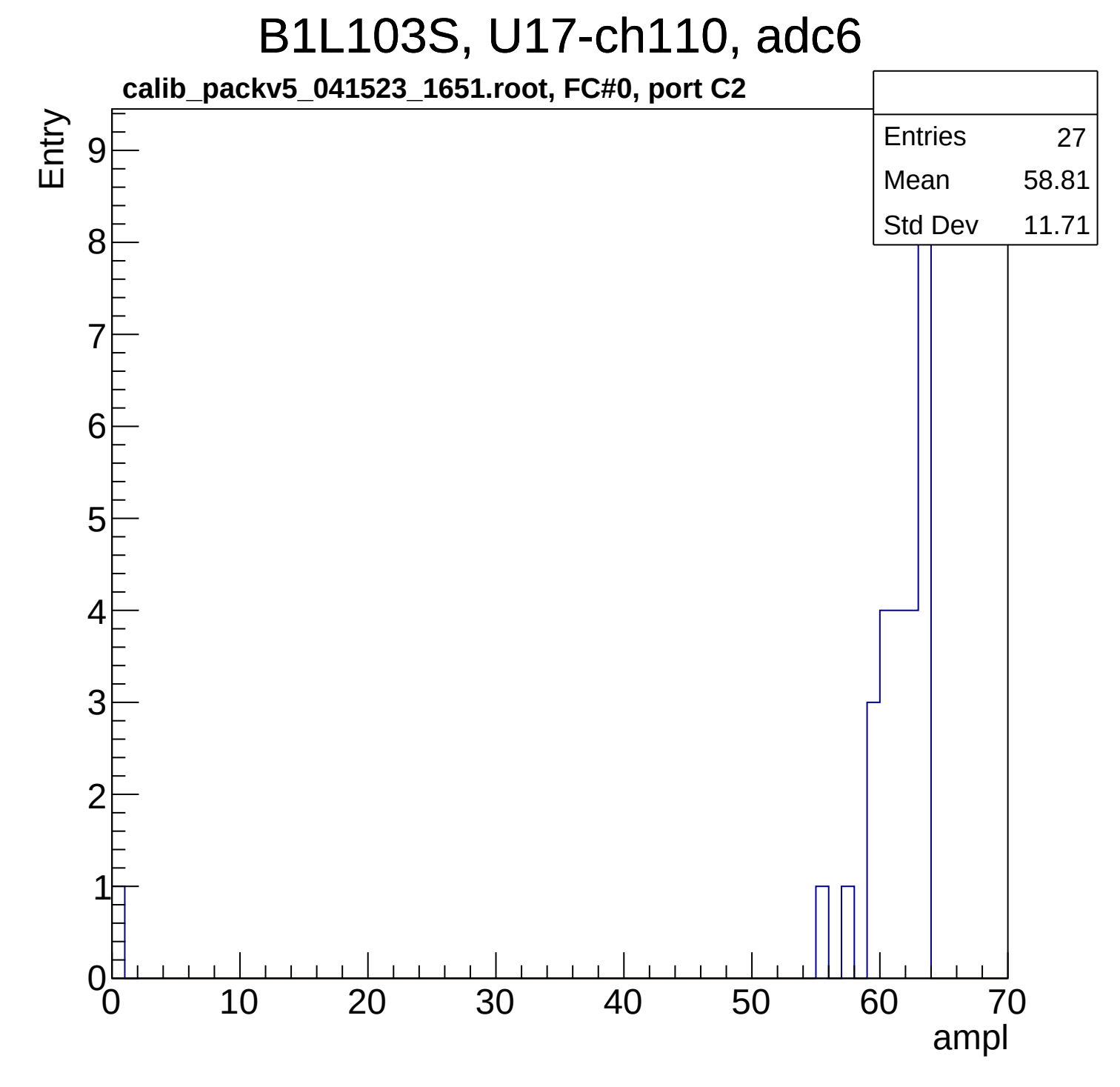
B1L103S, U17-ch110, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 27
Mean 58.81
Std Dev 11.71
Entry
ampl
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2
3
4
5
6
7
8
9
0
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40
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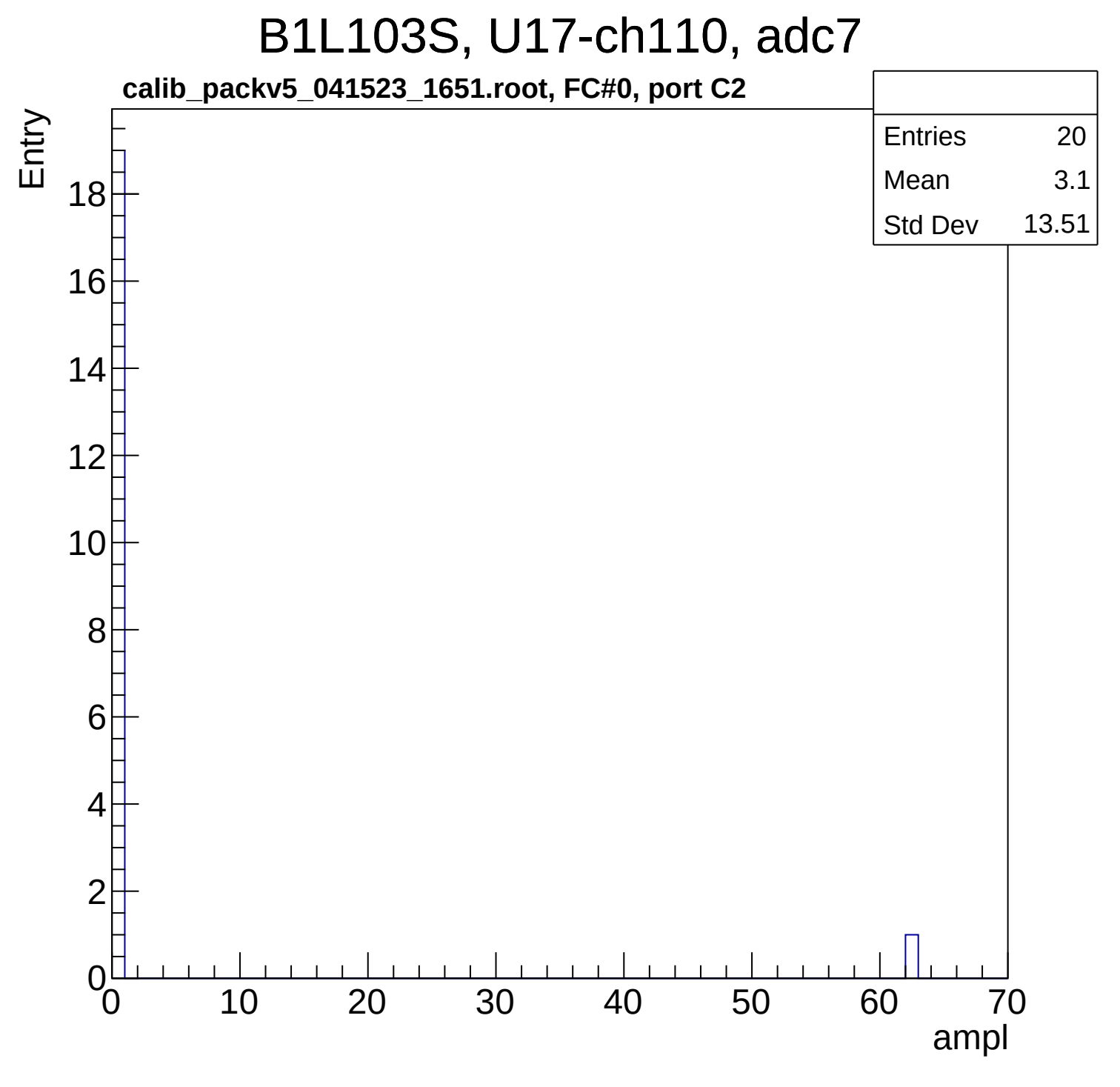
60
70


B1L103S, U17-ch110, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.1
Std Dev 13.51
Entry
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6
8
10
12
14
16
18
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10
20
30
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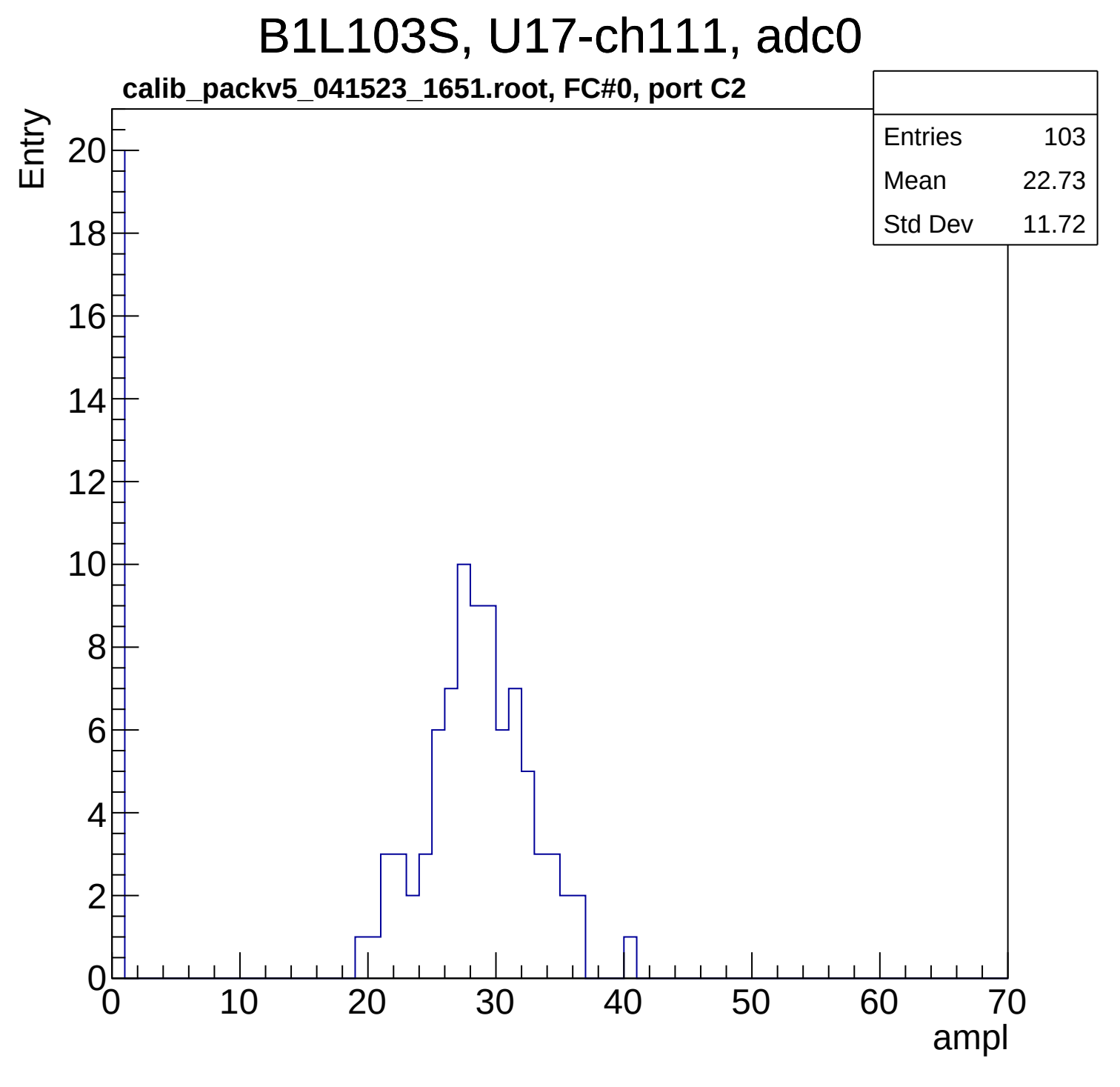
50
60
70
ampl


B1L103S, U17-ch111, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 103
Mean 22.73
Std Dev 11.72
Entry
ampl
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6
8
10
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14
16
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60
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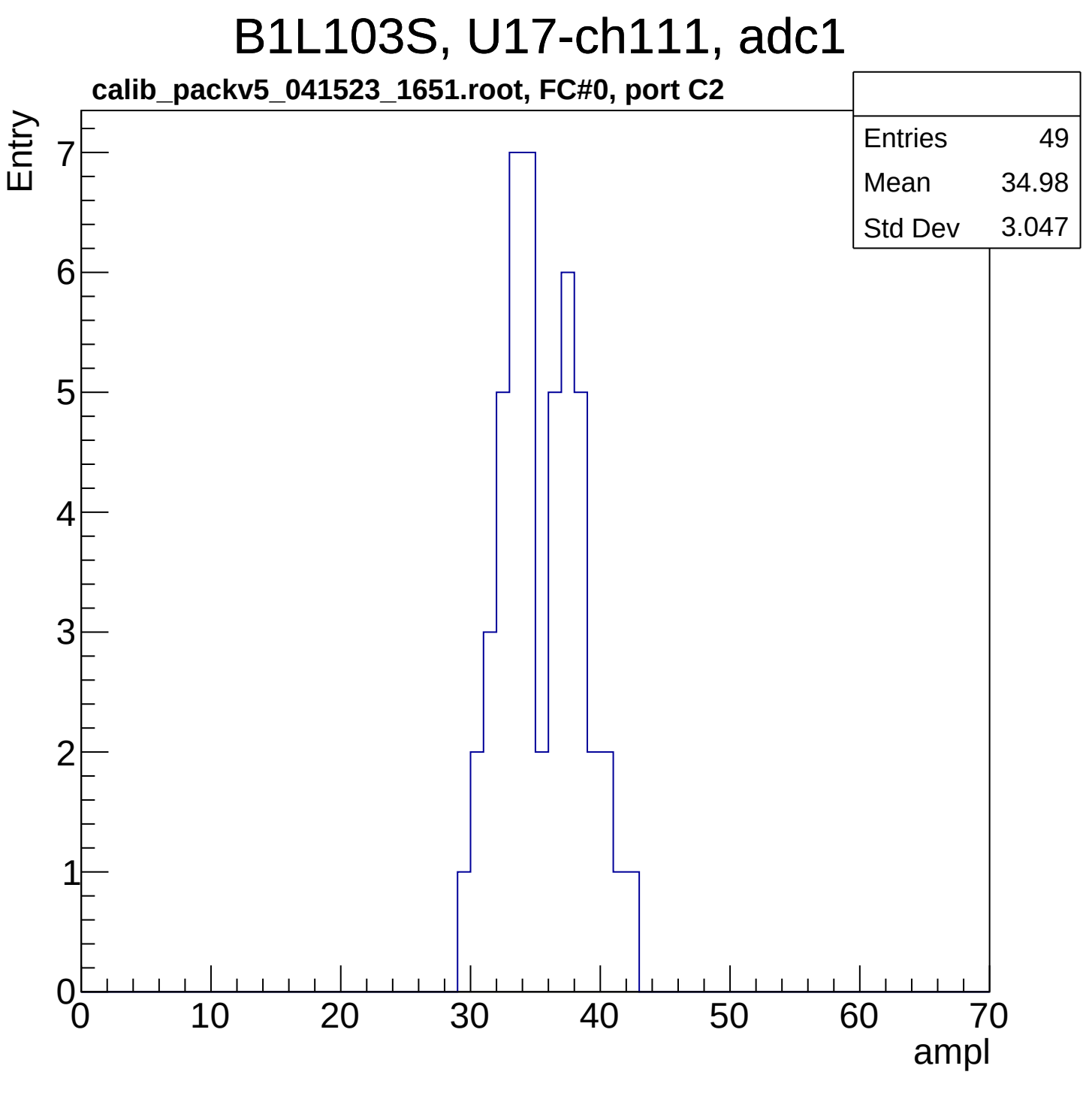
B1L103S, U17-ch111, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 34.98
Std Dev 3.047
Entry
ampl
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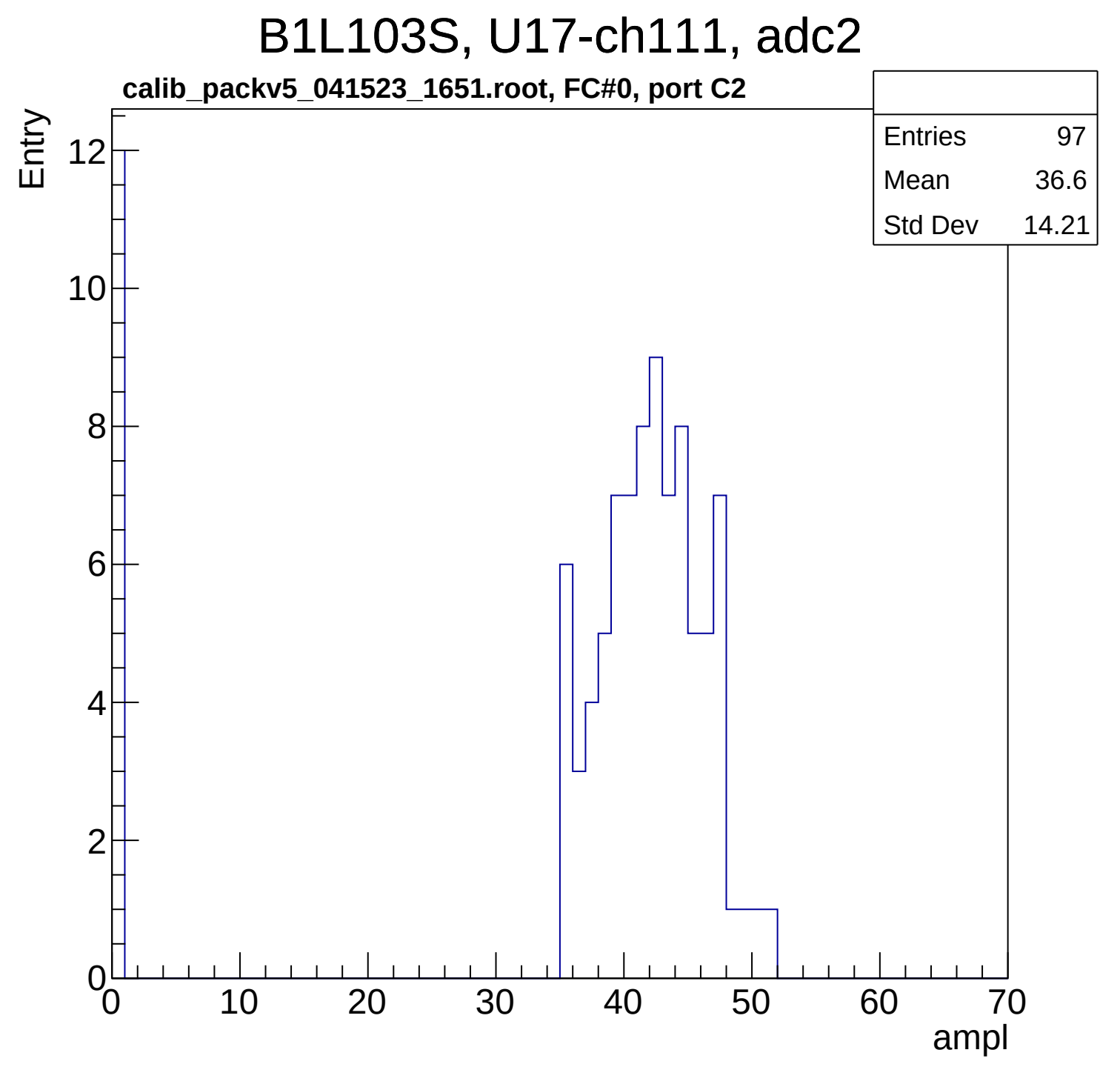
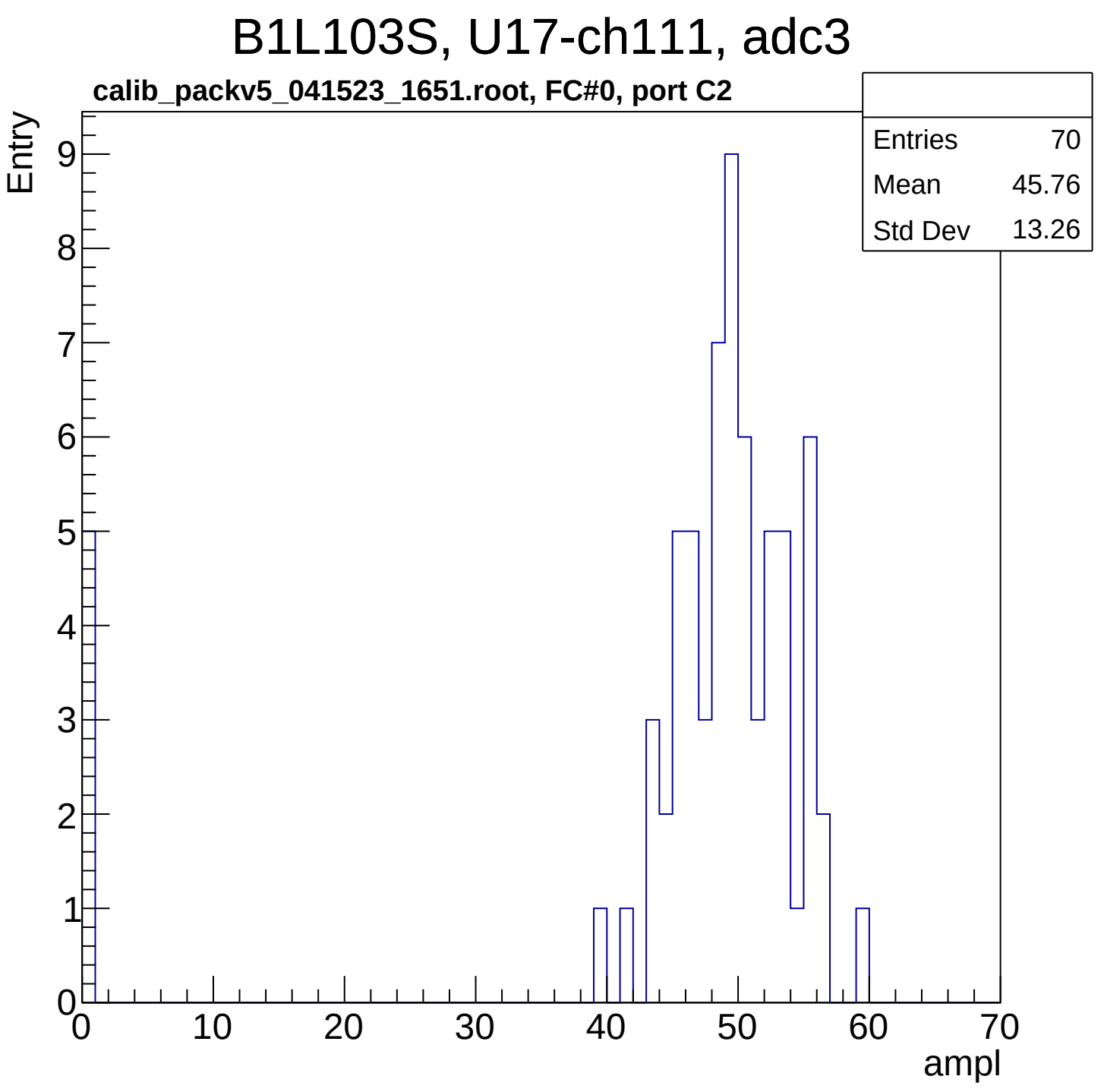

B1L103S, U17-ch111, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 97
Mean 36.6
Std Dev 14.21
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch111, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 45.76
Std Dev 13.26
Entry
ampl
0
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2
3
4
5
6
7
8
9
0
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20
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40
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60
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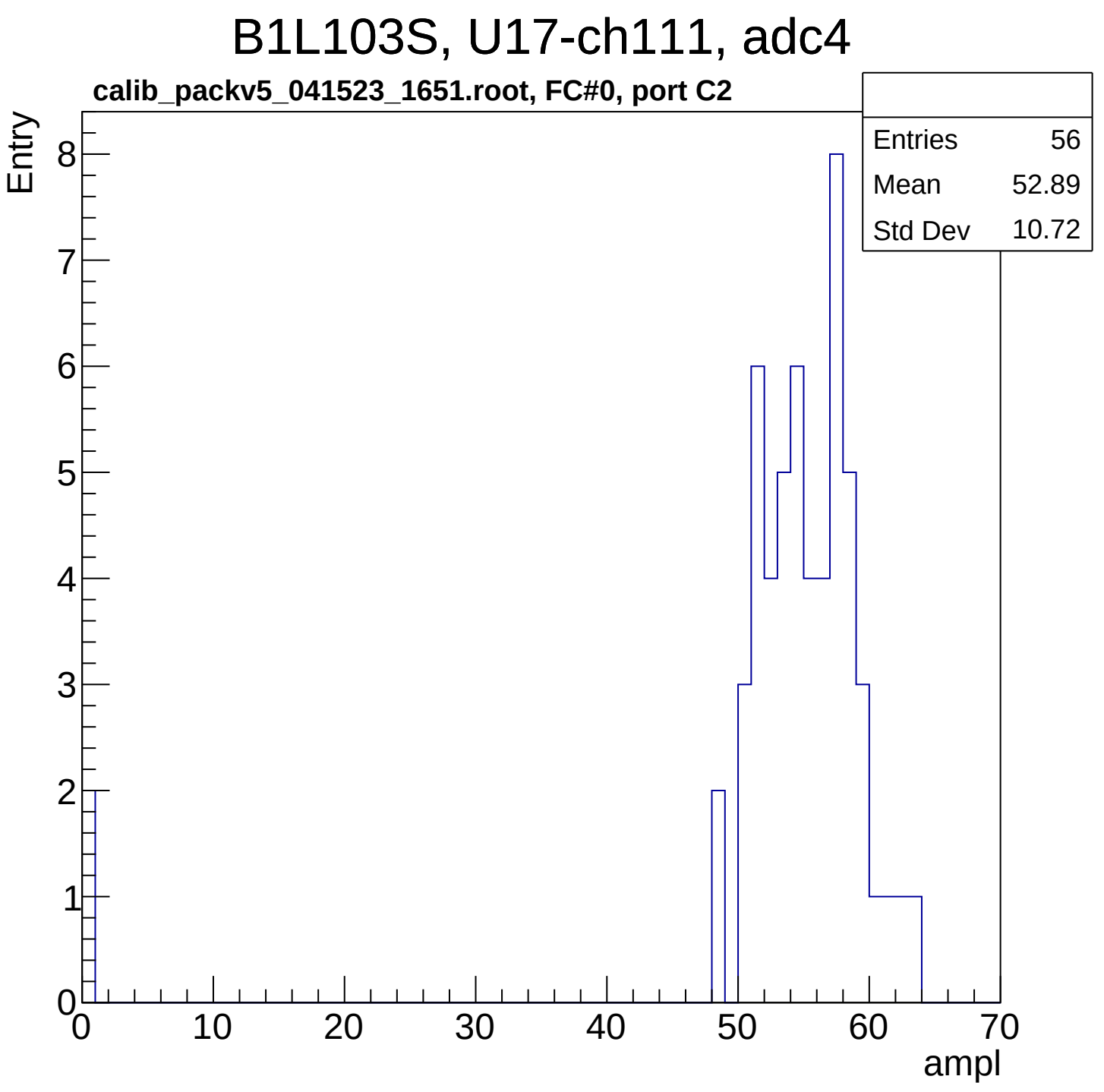
B1L103S, U17-ch111, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 52.89
Std Dev 10.72
Entry
ampl
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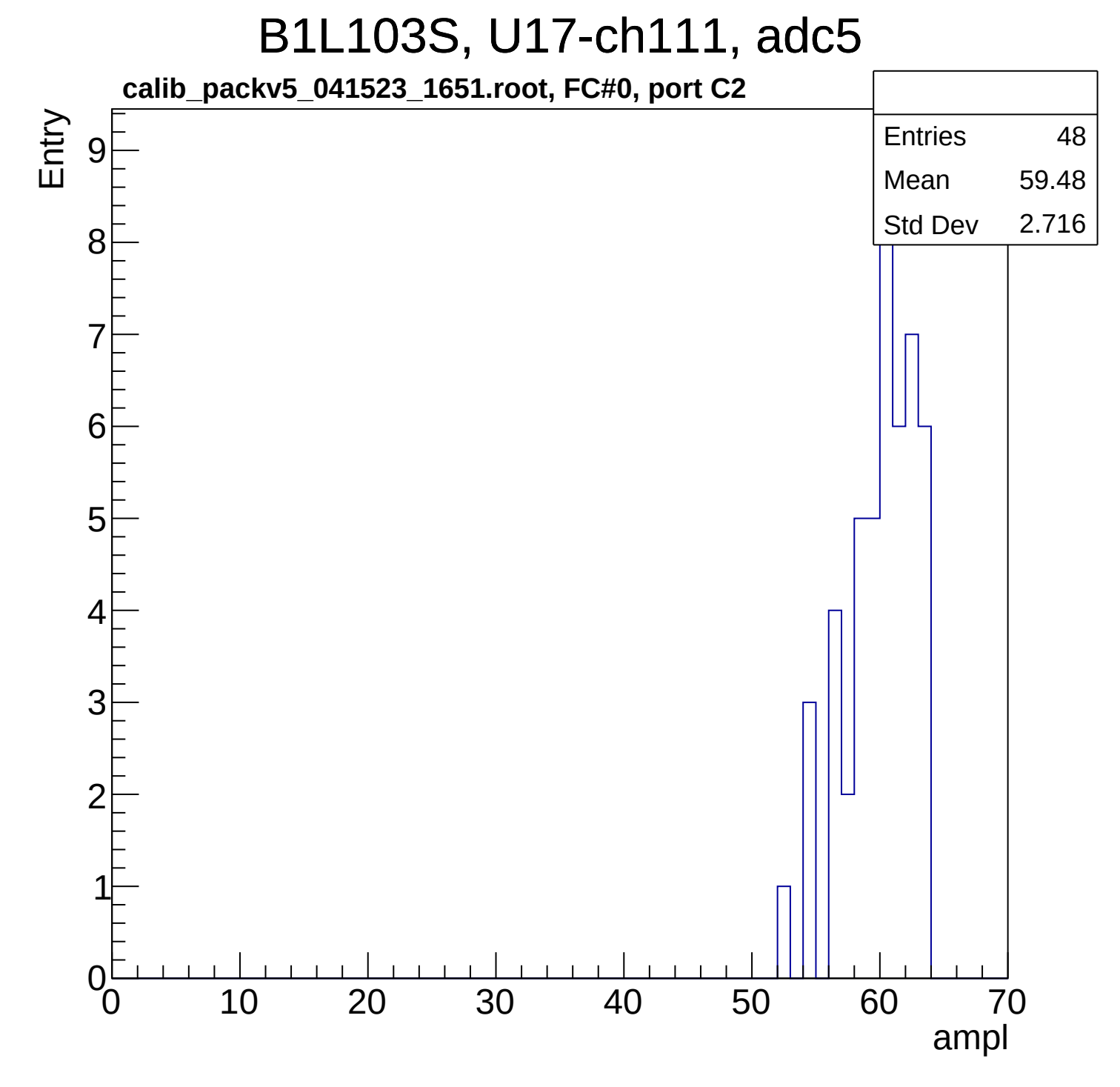
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U17-ch111, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 59.48
Std Dev 2.716
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
30
40
50
60
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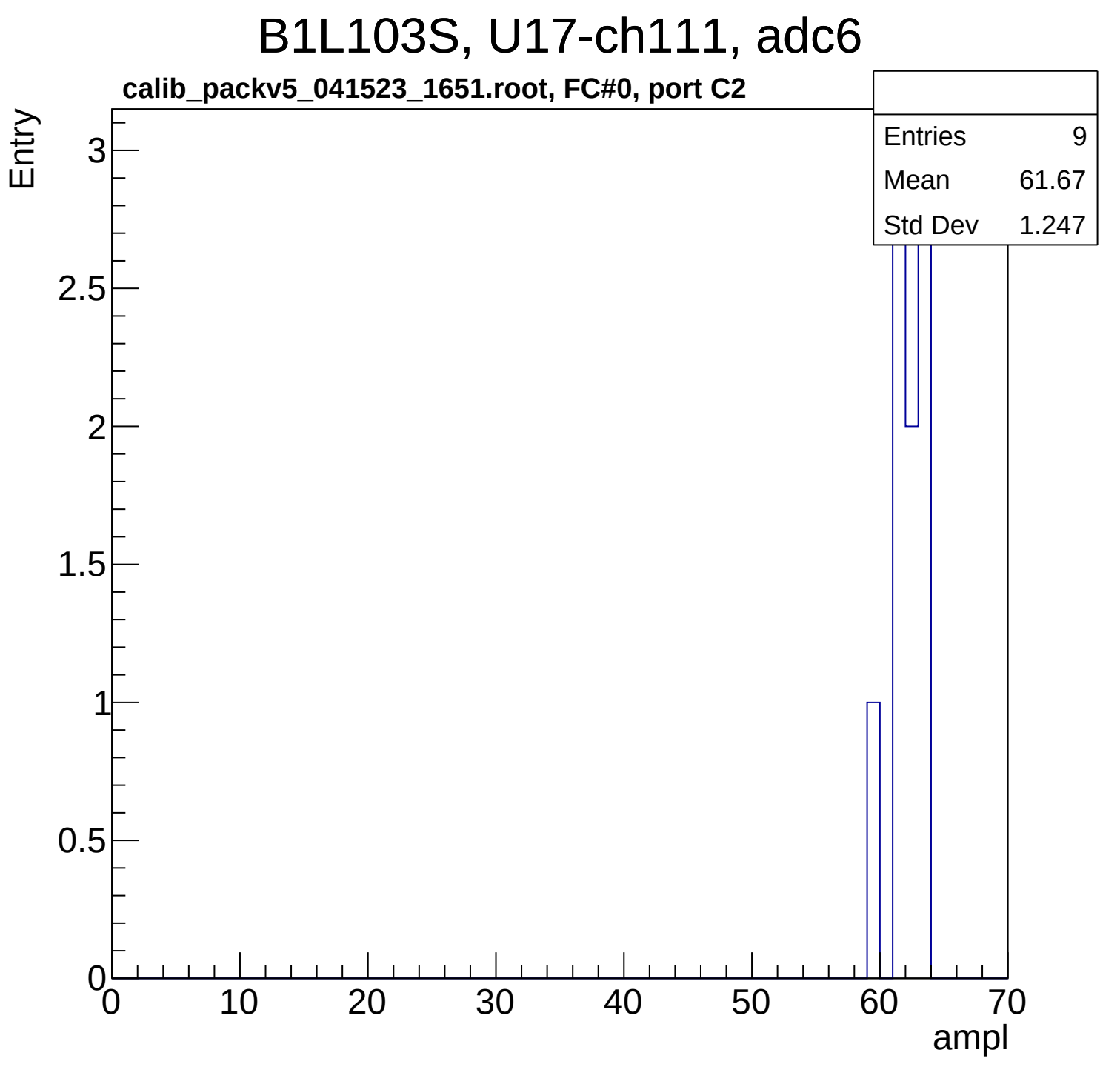
B1L103S, U17-ch111, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 9
Mean 61.67
Std Dev 1.247
Entry
ampl
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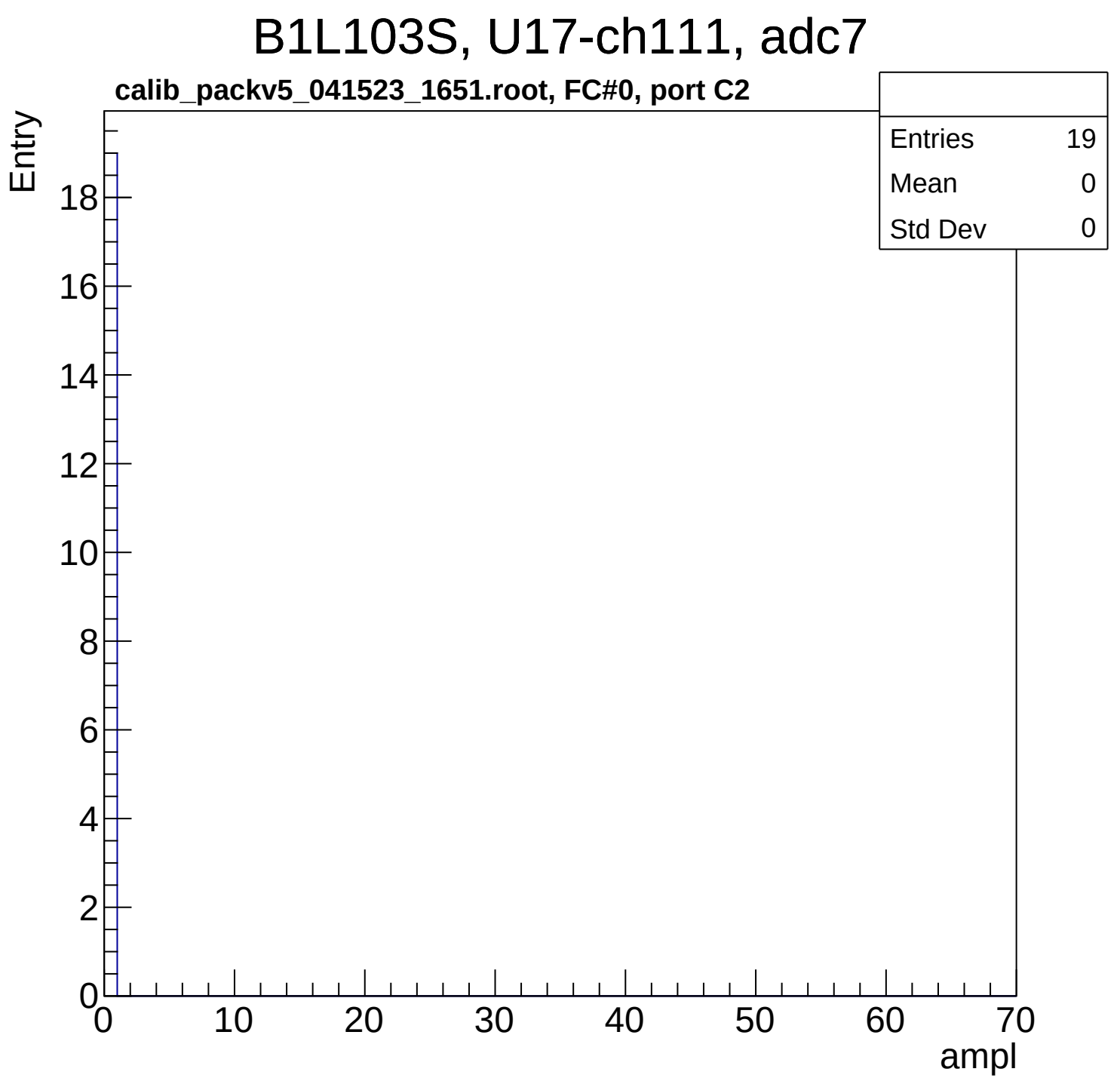
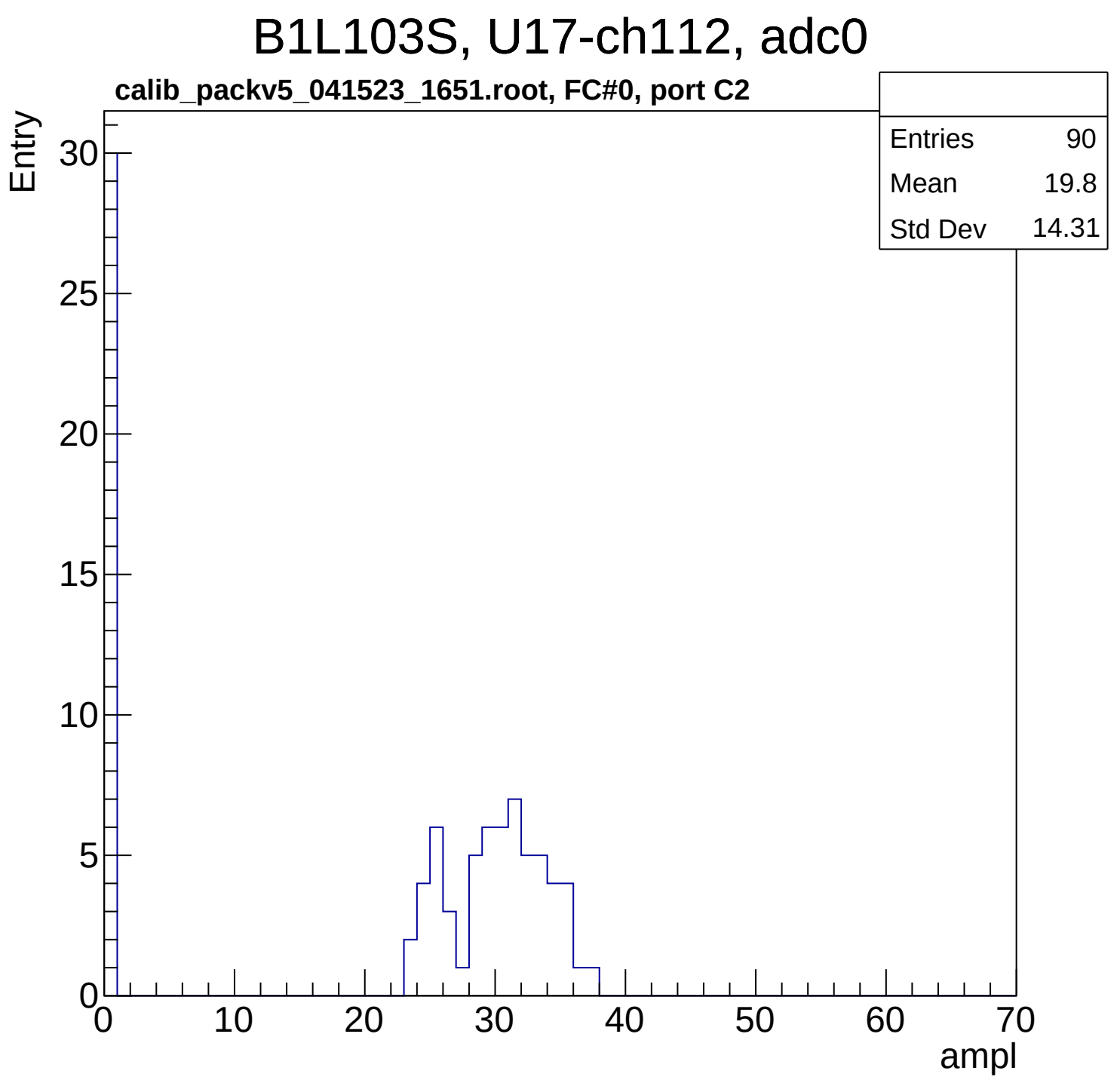
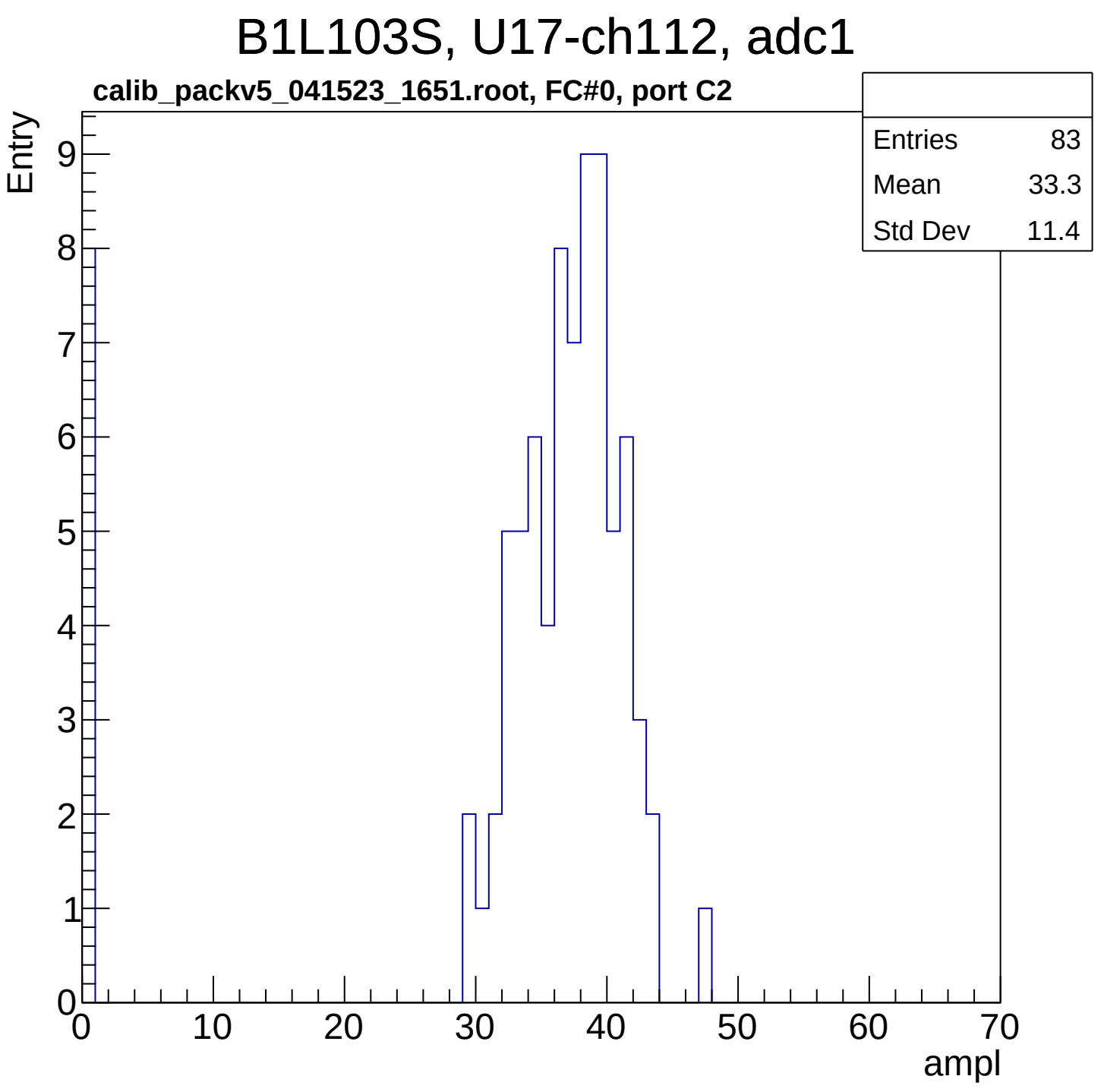
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U17-ch111, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch112, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 90
Mean 19.8
Std Dev 14.31
Entry
ampl
0
5
10
15
20
25
30
0
10
20
30
40
50
60
70


B1L103S, U17-ch112, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 33.3
Std Dev 11.4
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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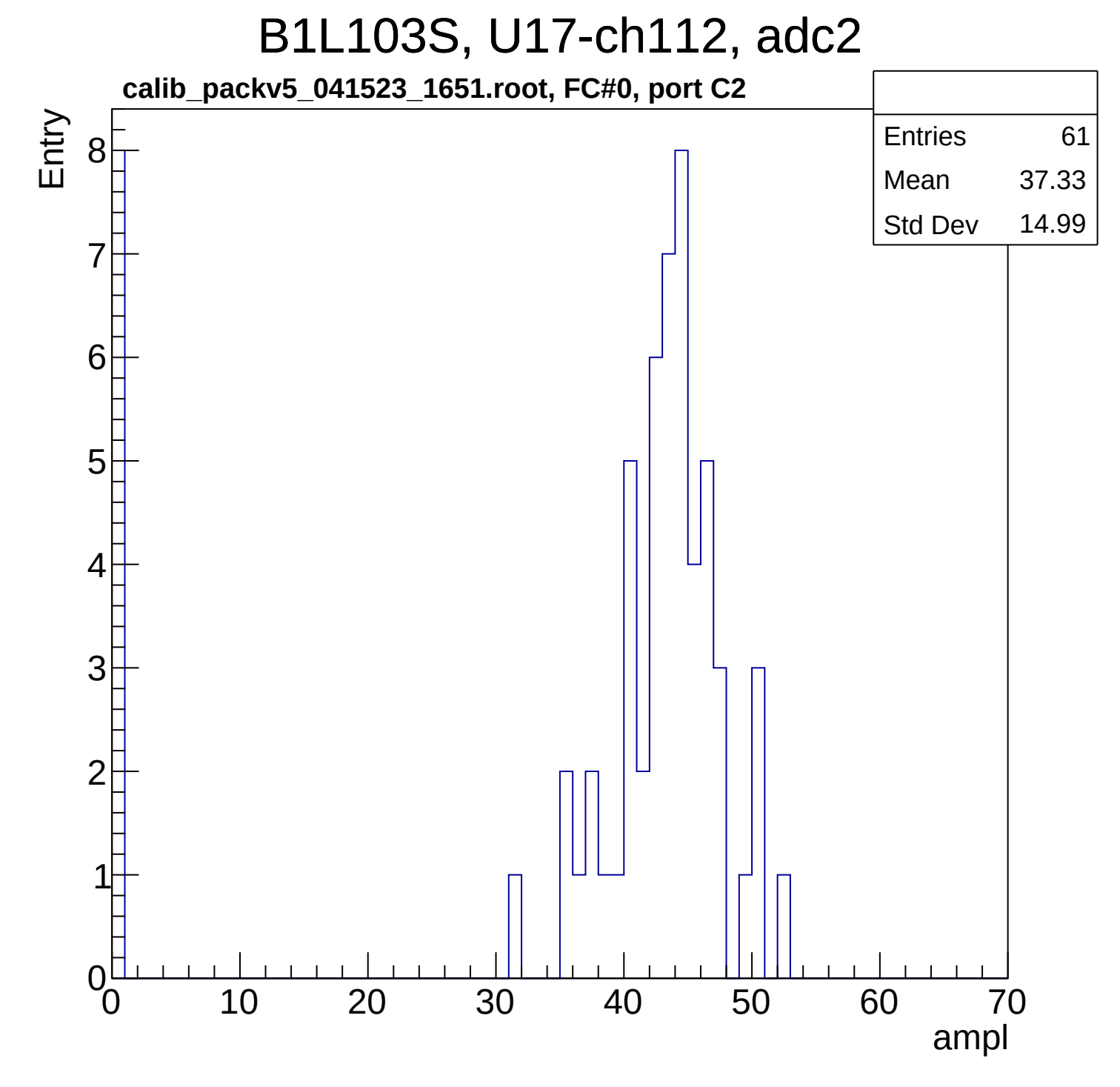
B1L103S, U17-ch112, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 37.33
Std Dev 14.99
Entry
ampl
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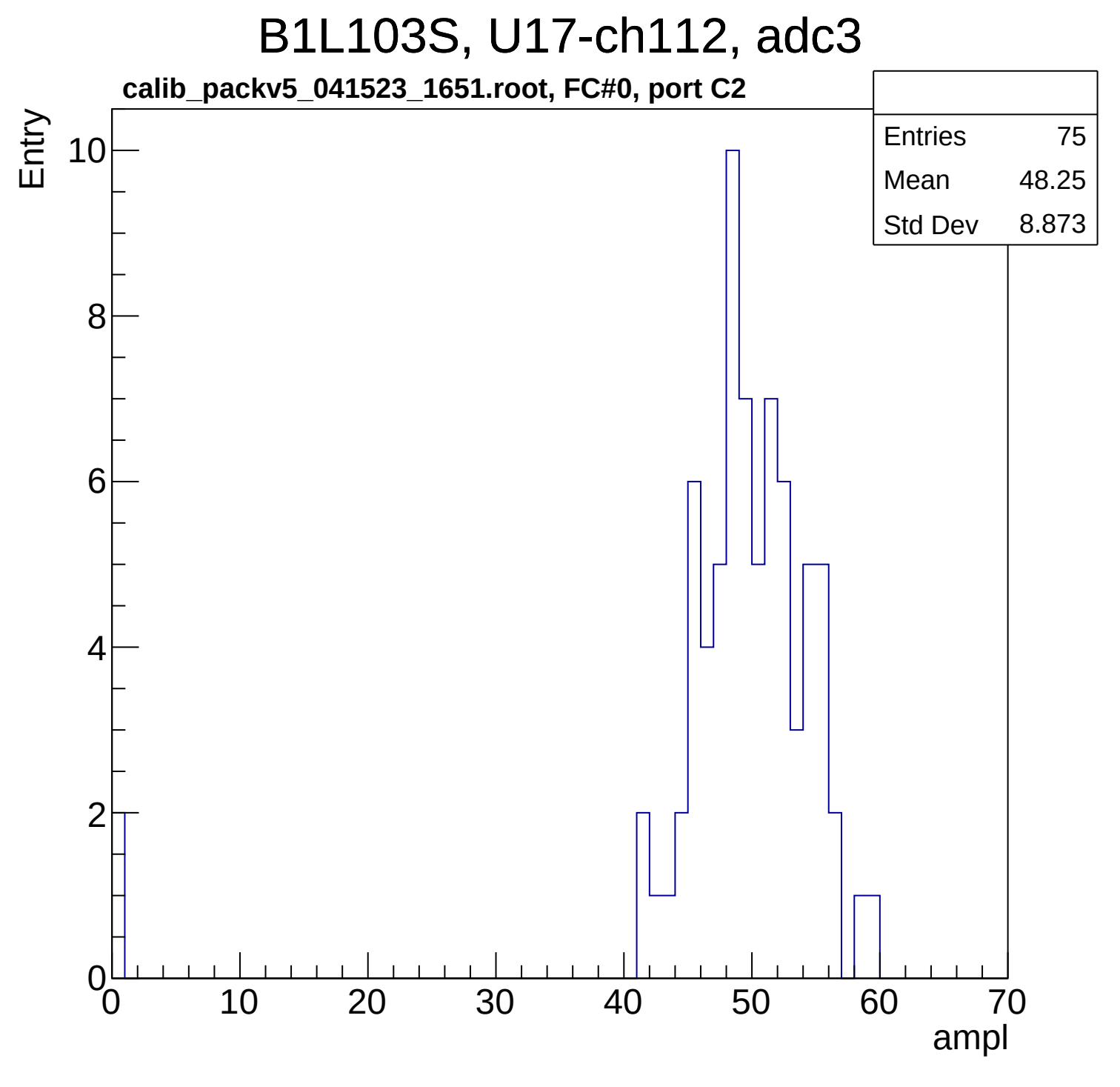
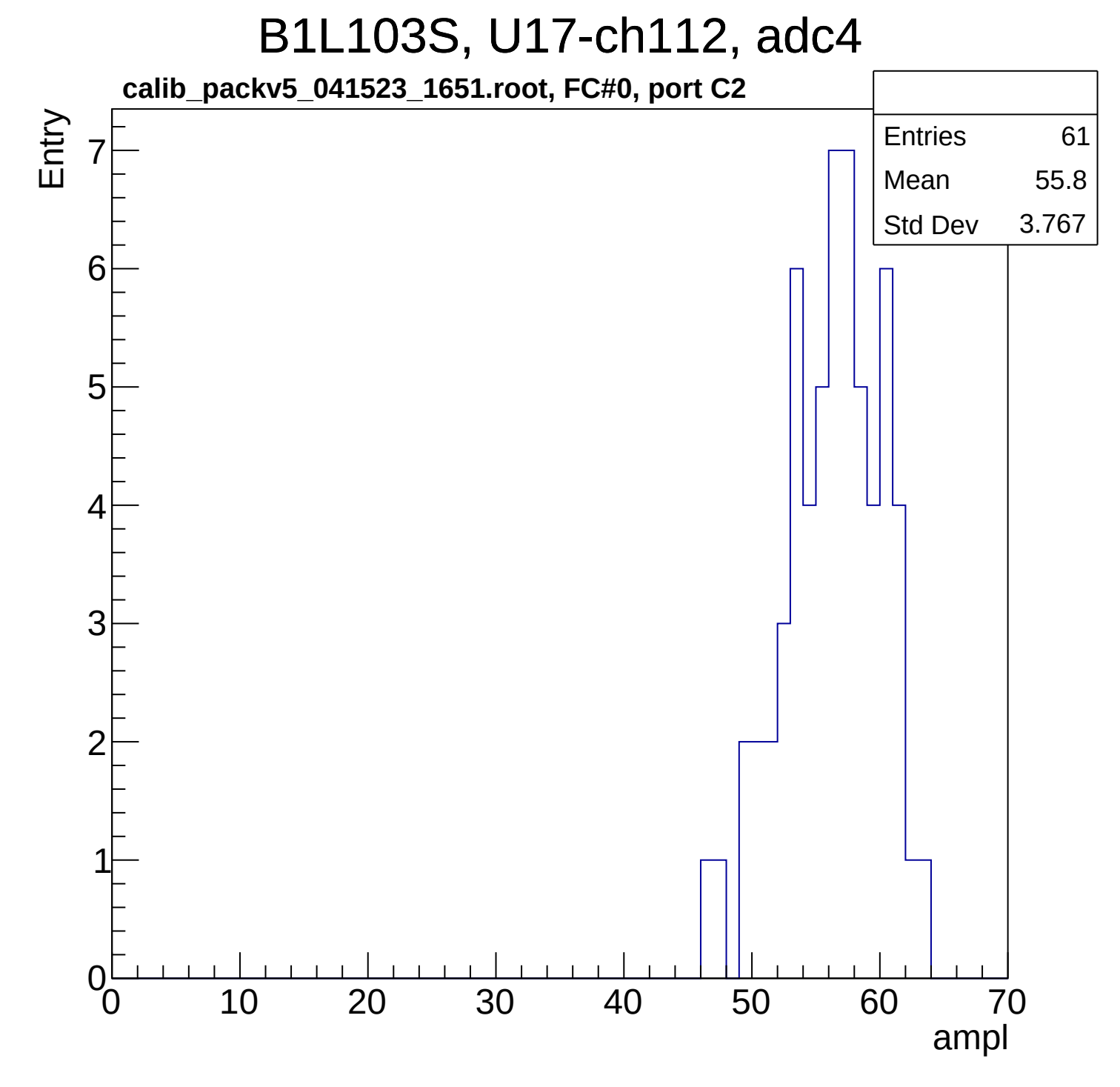
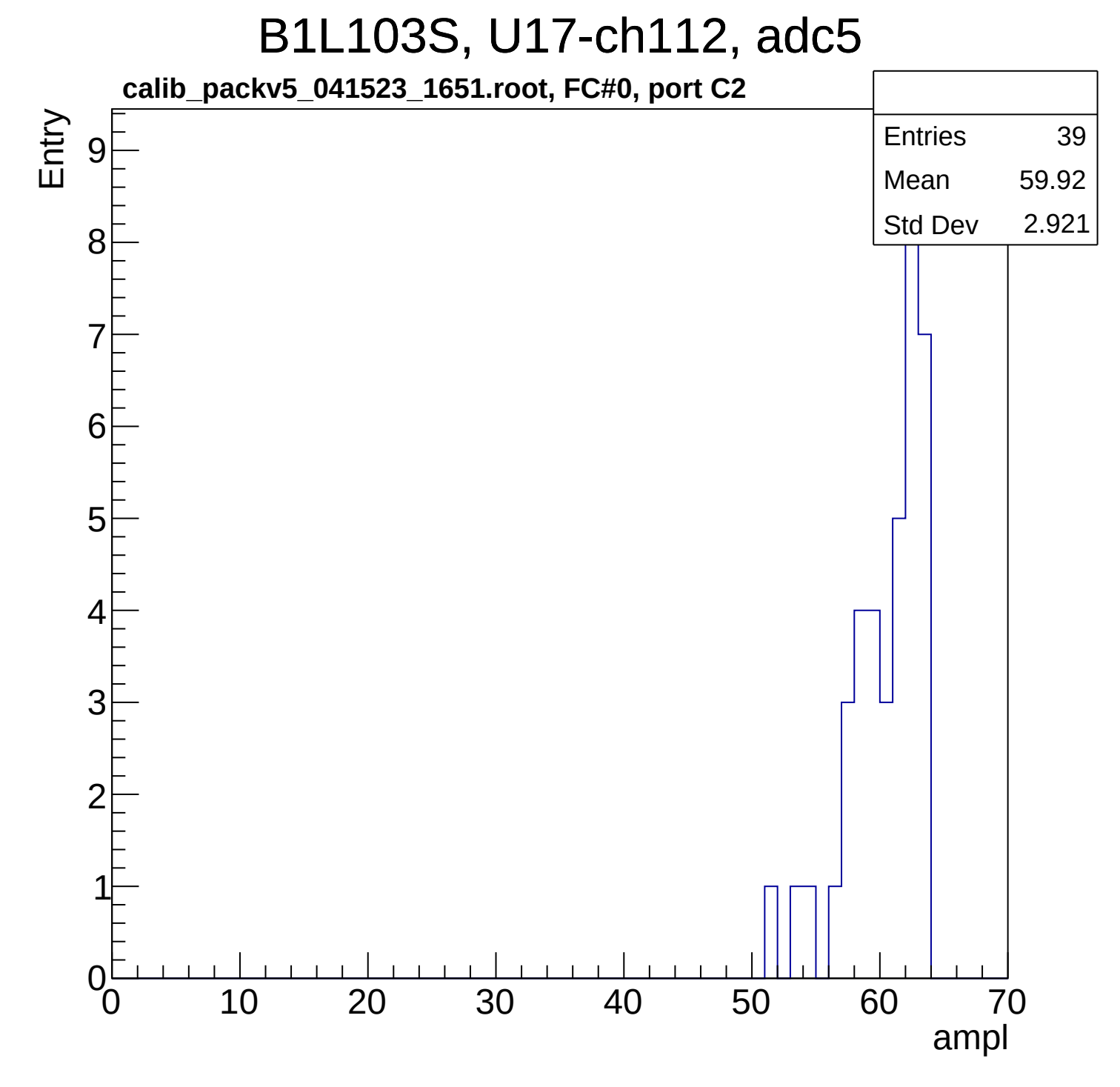
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U17-ch112, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 48.25
Std Dev 8.873
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U17-ch112, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 55.8
Std Dev 3.767
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U17-ch112, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 39
Mean 59.92
Std Dev 2.921
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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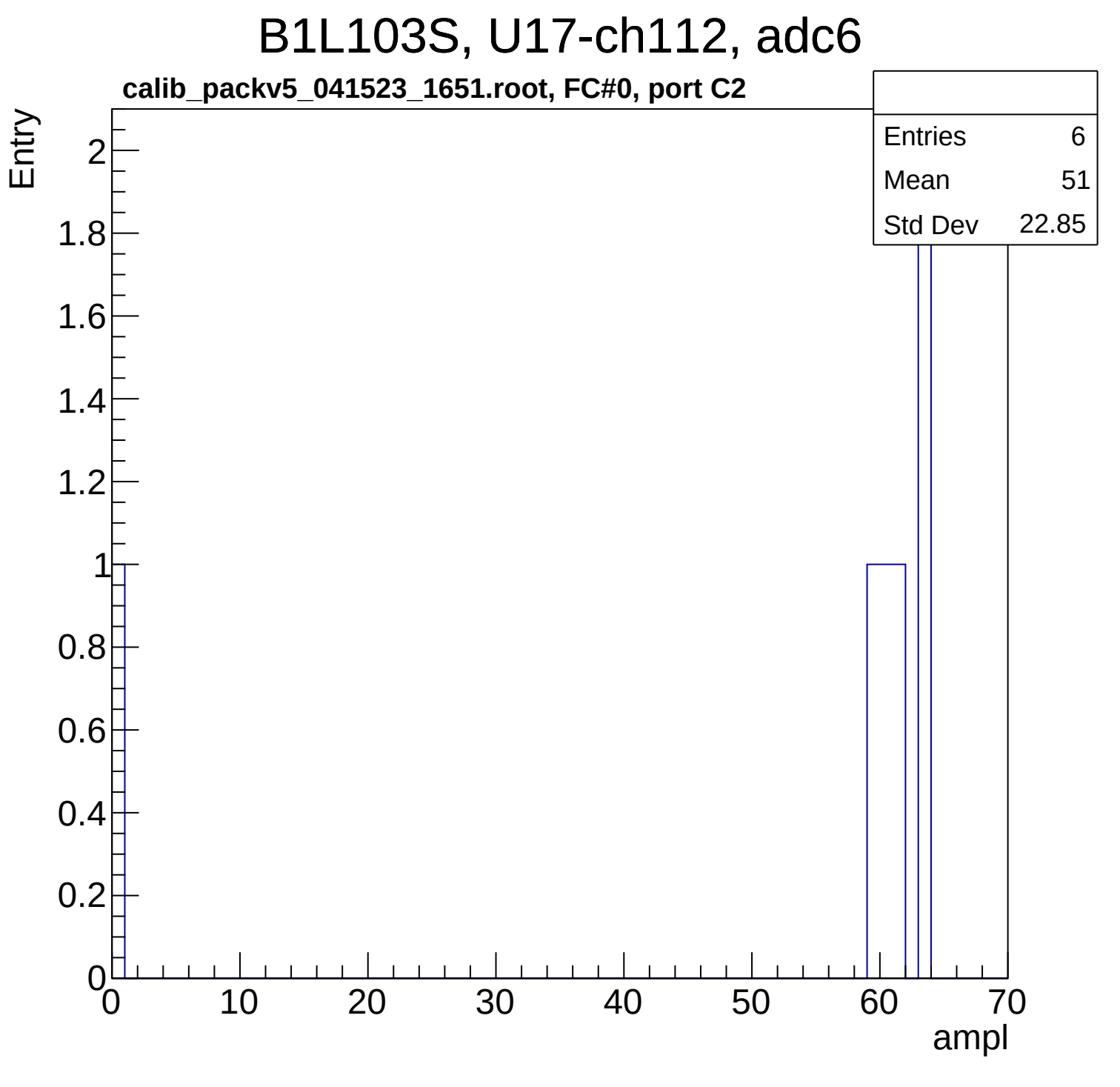
B1L103S, U17-ch112, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 51
Std Dev 22.85
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
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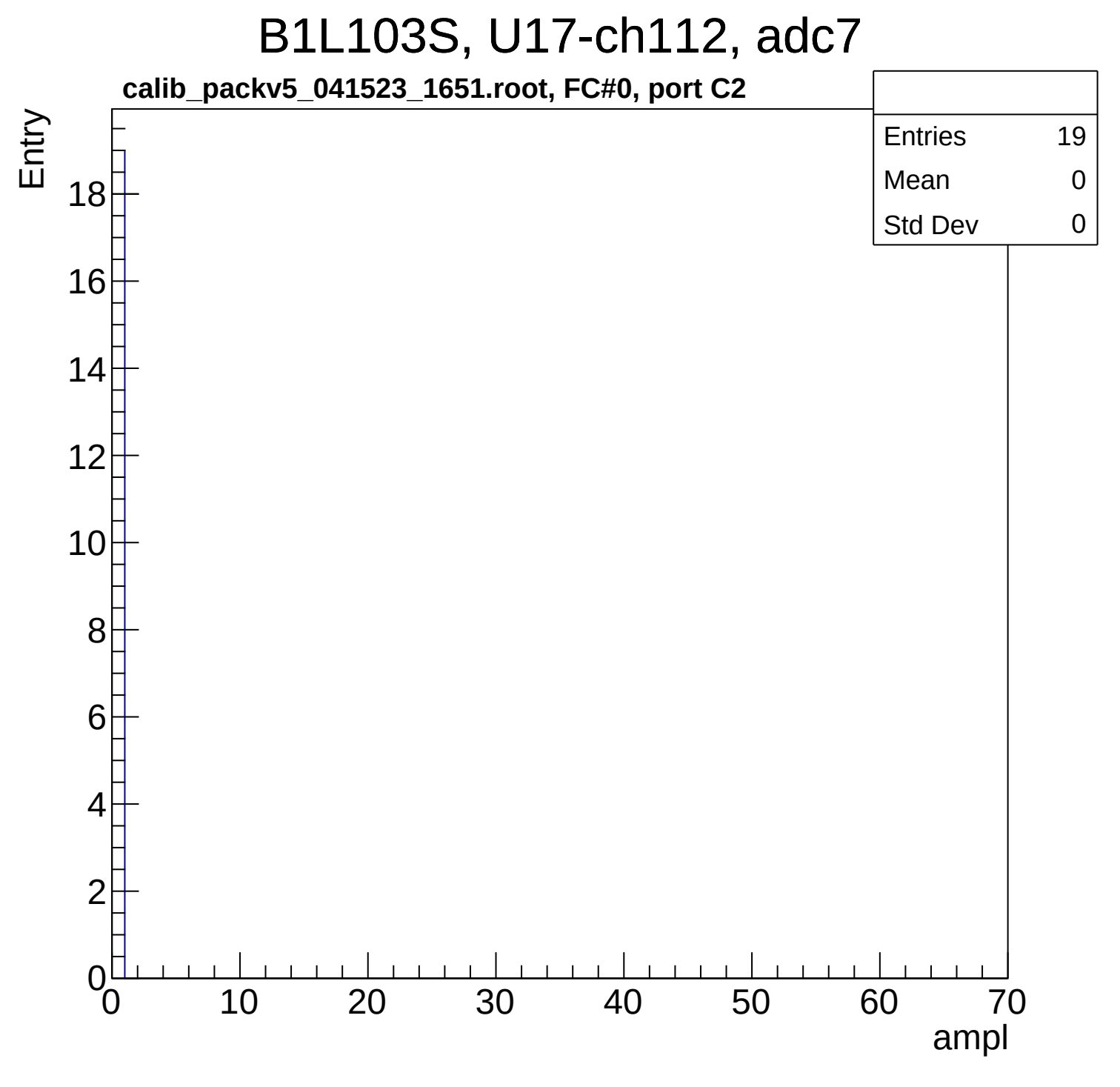
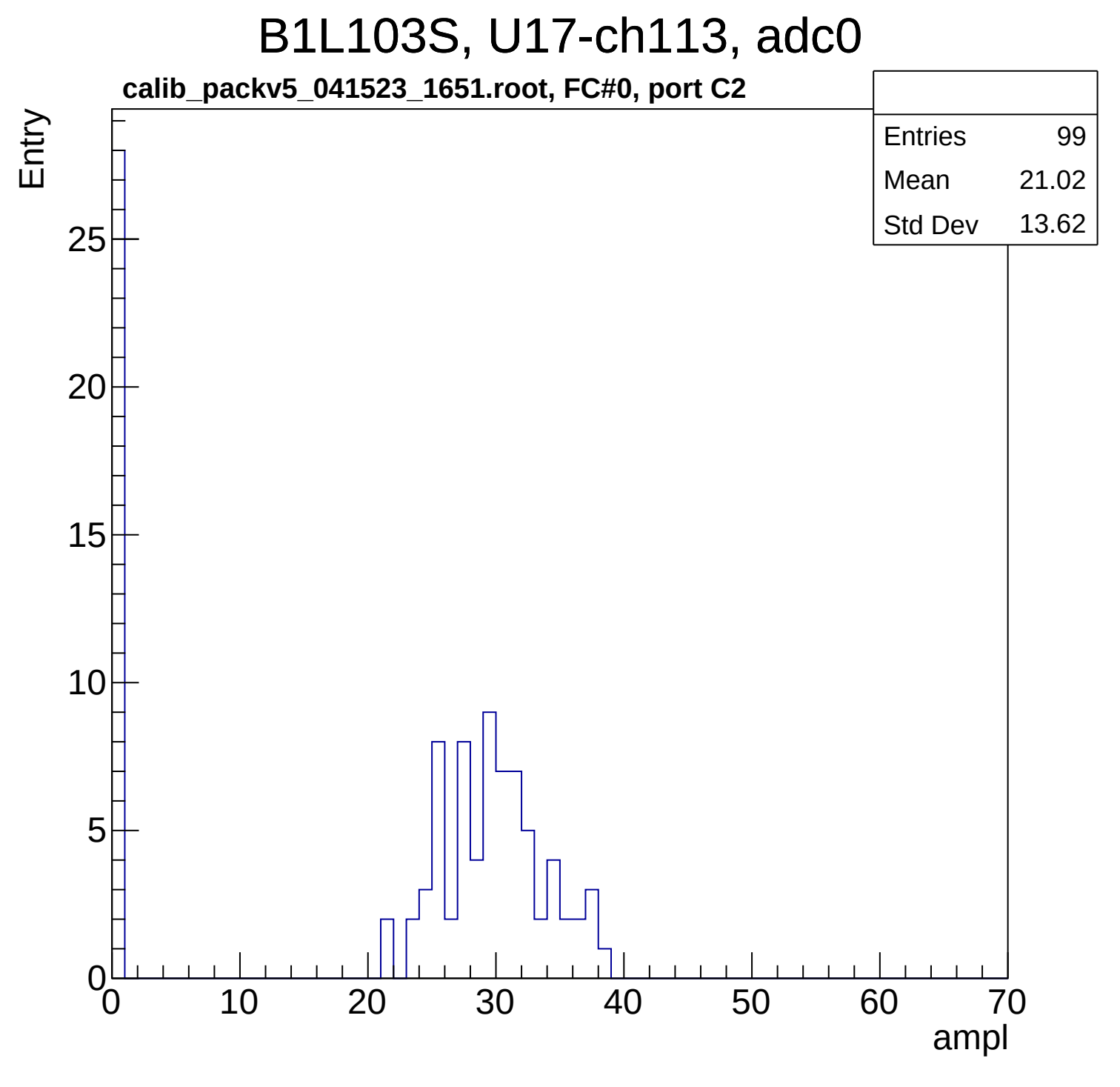
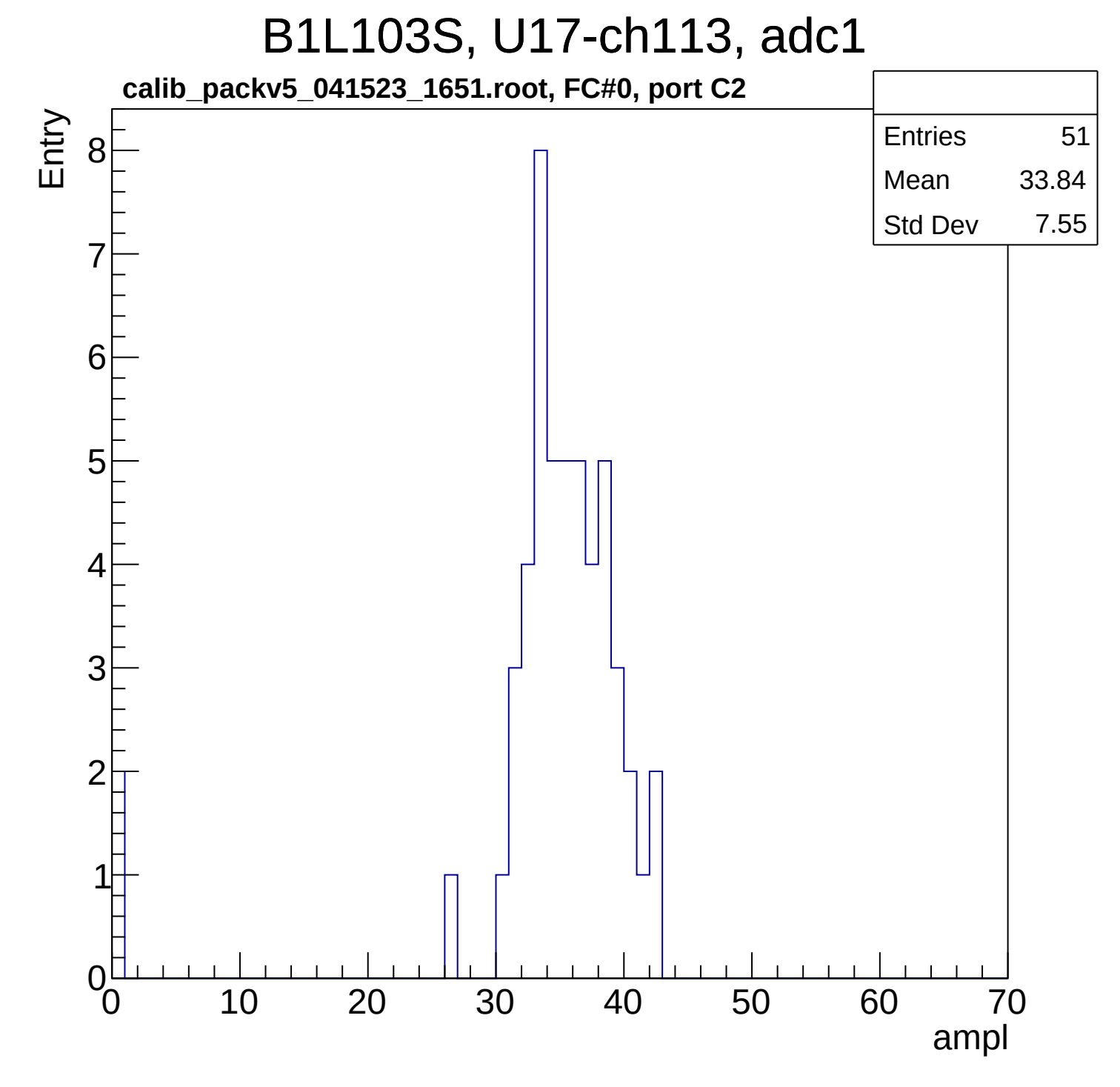

B1L103S, U17-ch112, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch113, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 99
Mean 21.02
Std Dev 13.62
Entry
0
5
10
15
20
25
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch113, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 33.84
Std Dev 7.55
Entry
ampl
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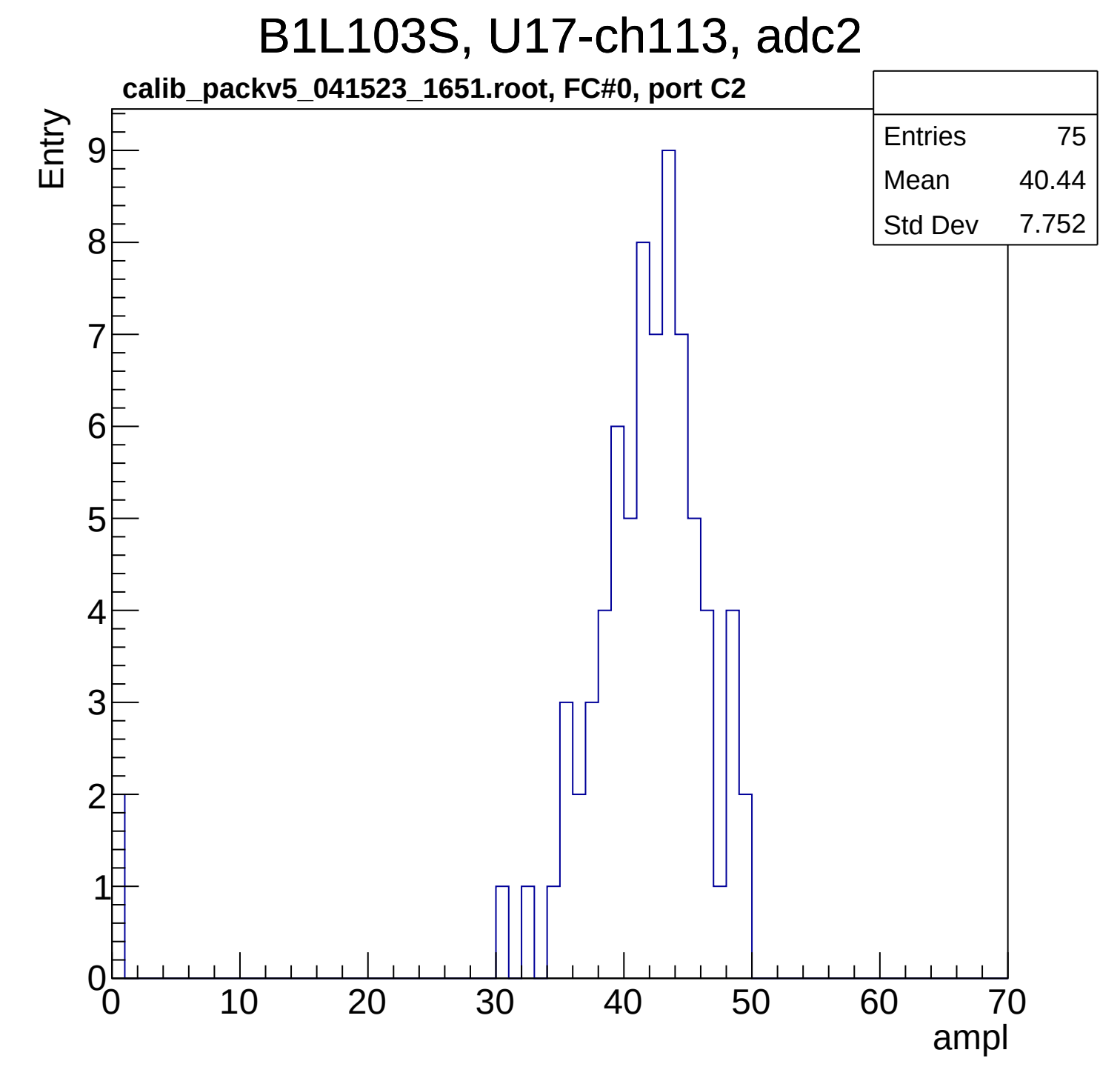
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U17-ch113, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 40.44
Std Dev 7.752
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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50
60
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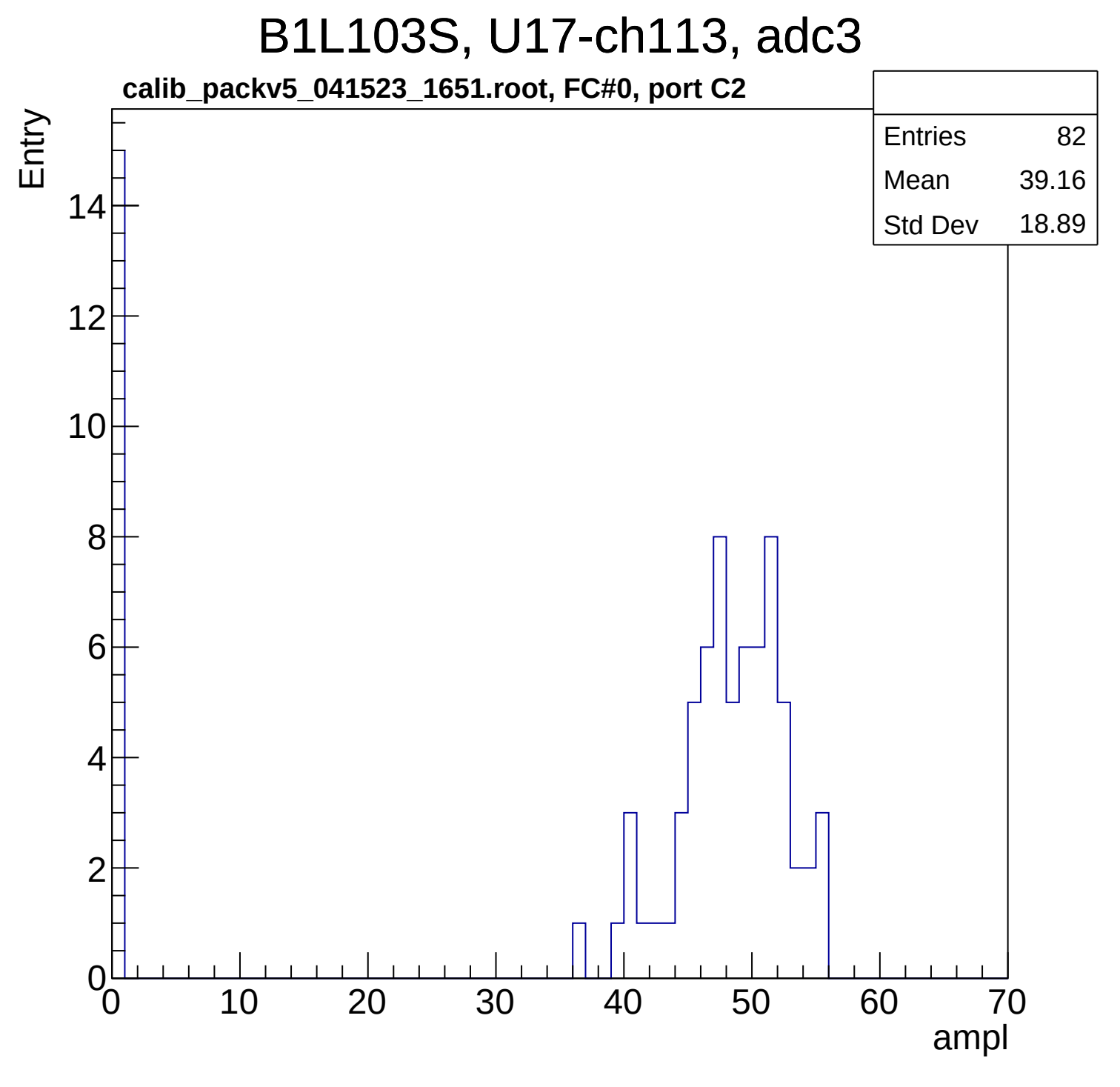
B1L103S, U17-ch113, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 39.16
Std Dev 18.89
Entry
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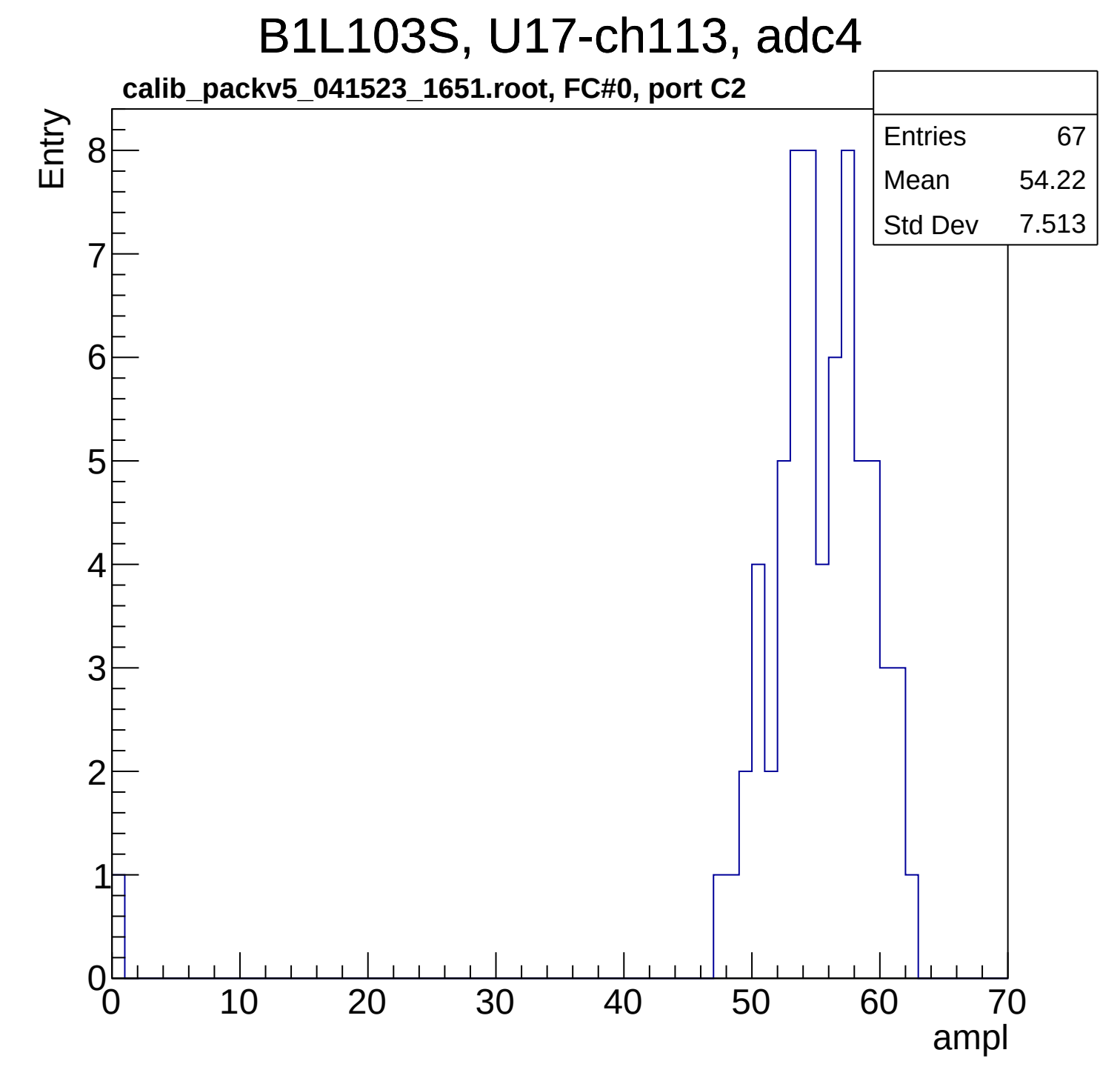
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch113, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 54.22
Std Dev 7.513
Entry
ampl
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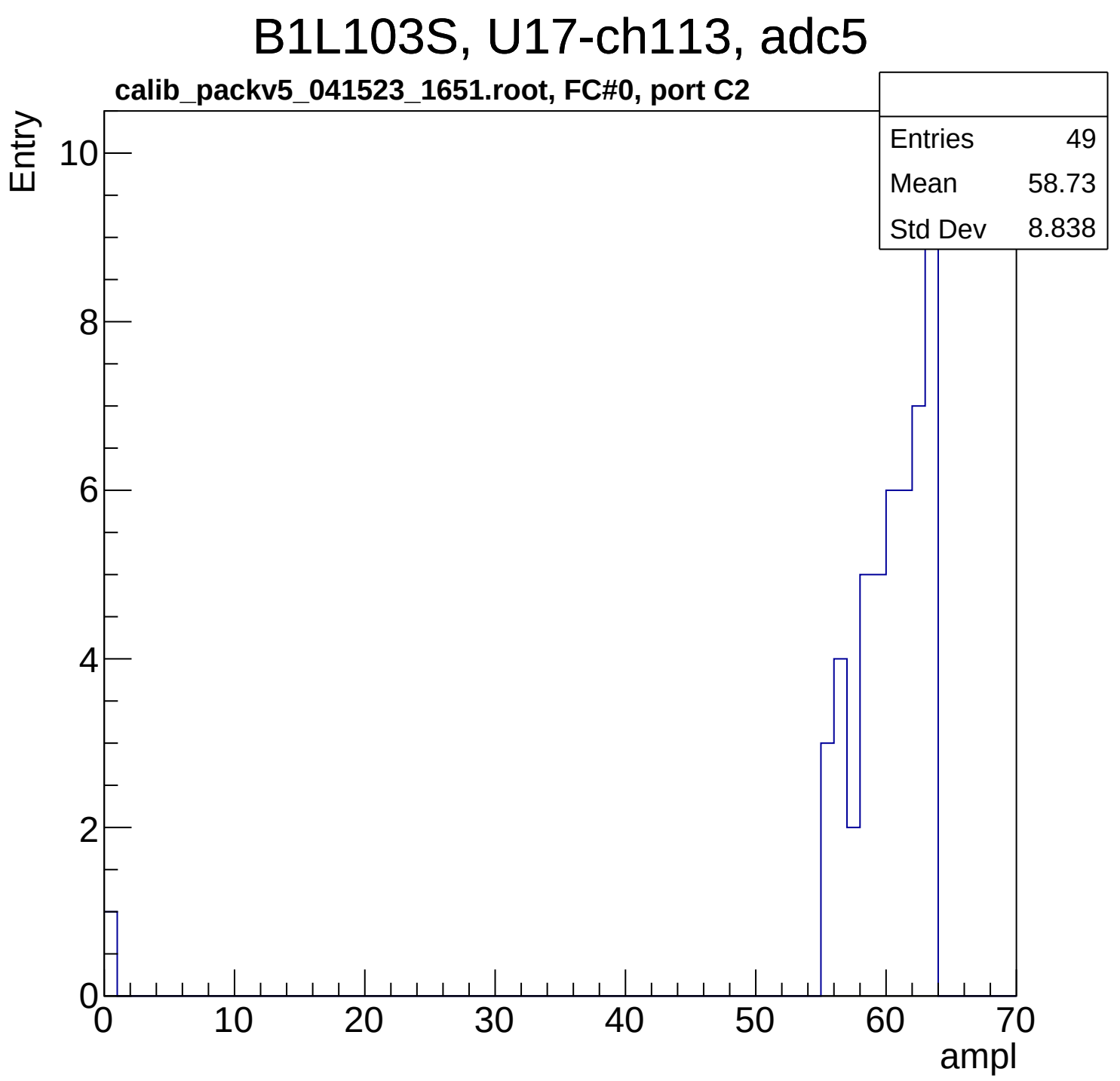
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U17-ch113, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 58.73
Std Dev 8.838
Entry
ampl
0
2
4
6
8
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0
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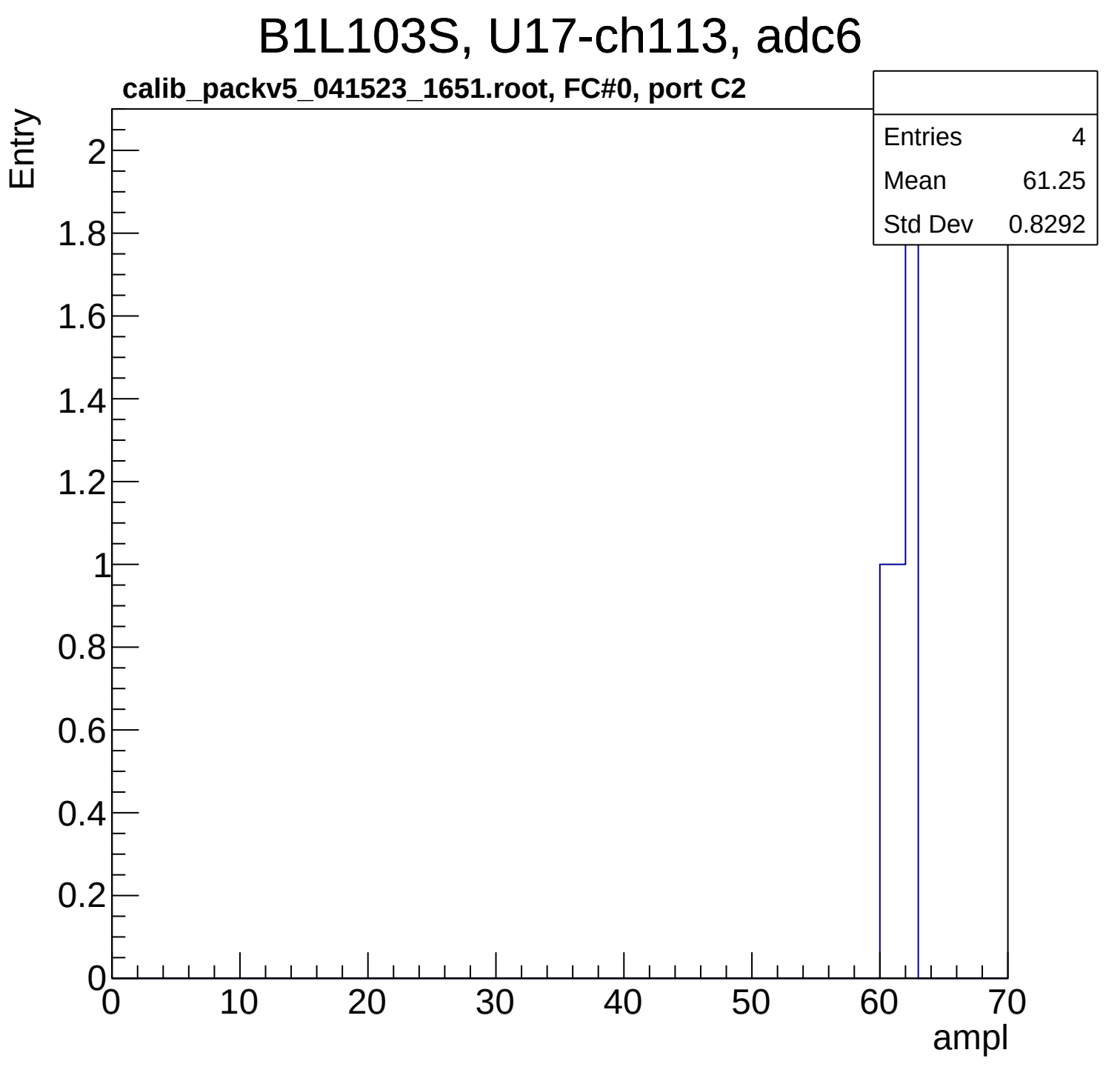
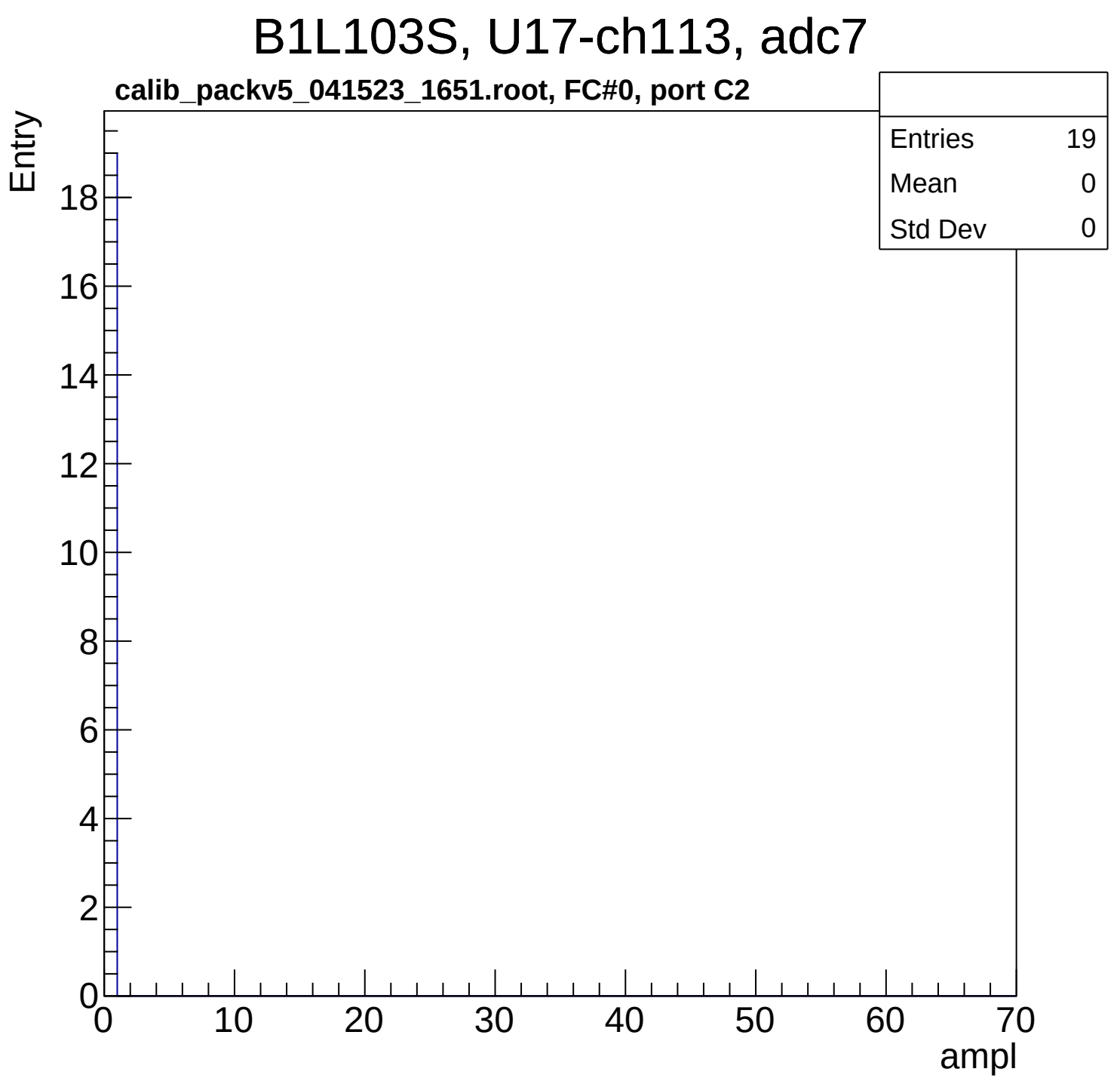
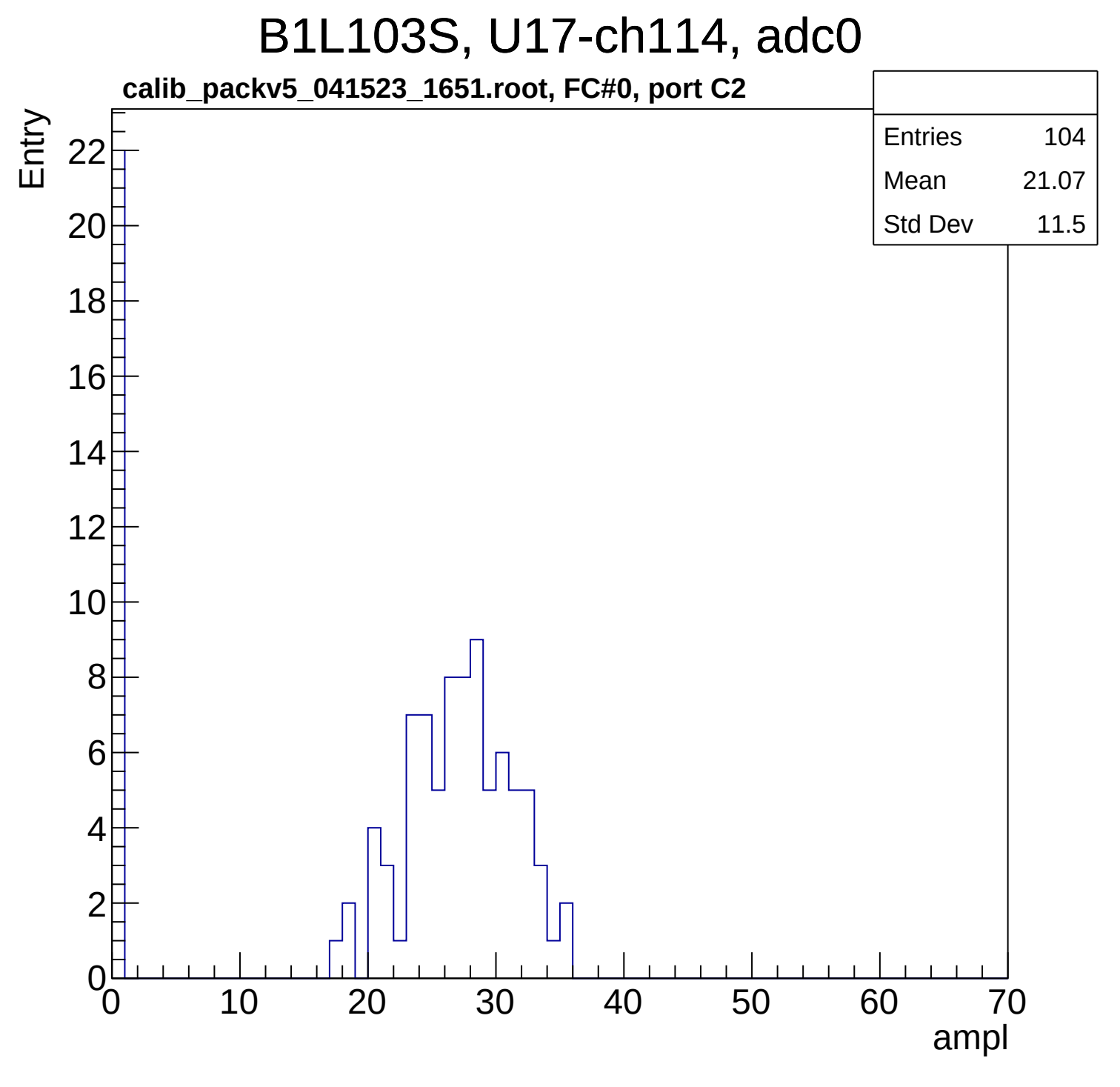
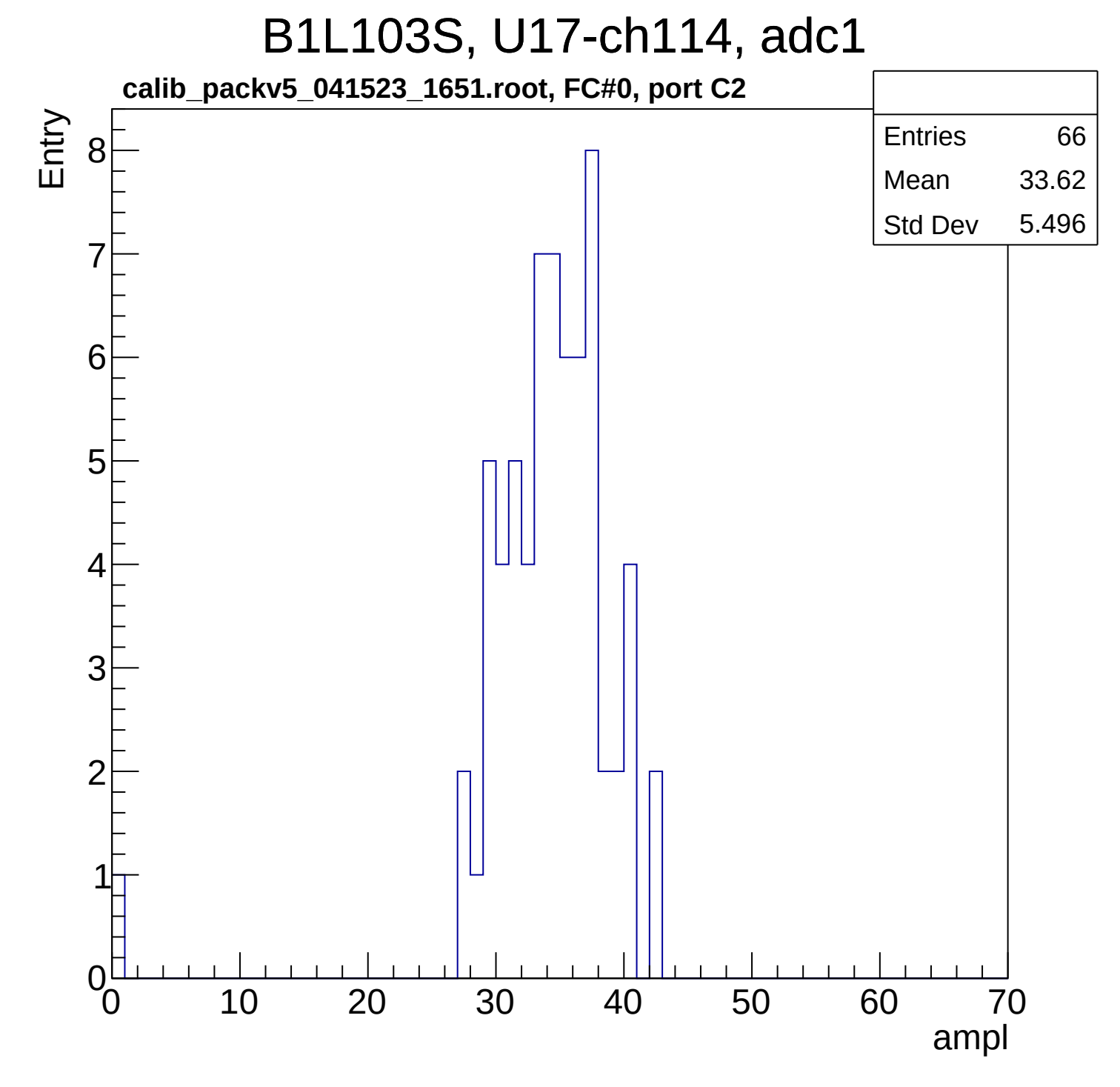
20
30
40
50
60
70


B1L103S, U17-ch113, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 4
Mean 61.25
Std Dev 0.8292
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U17-ch113, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch114, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 104
Mean 21.07
Std Dev 11.5
Entry
0
2
4
6
8
10
12
14
16
18
20
22
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch114, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 33.62
Std Dev 5.496
Entry
ampl
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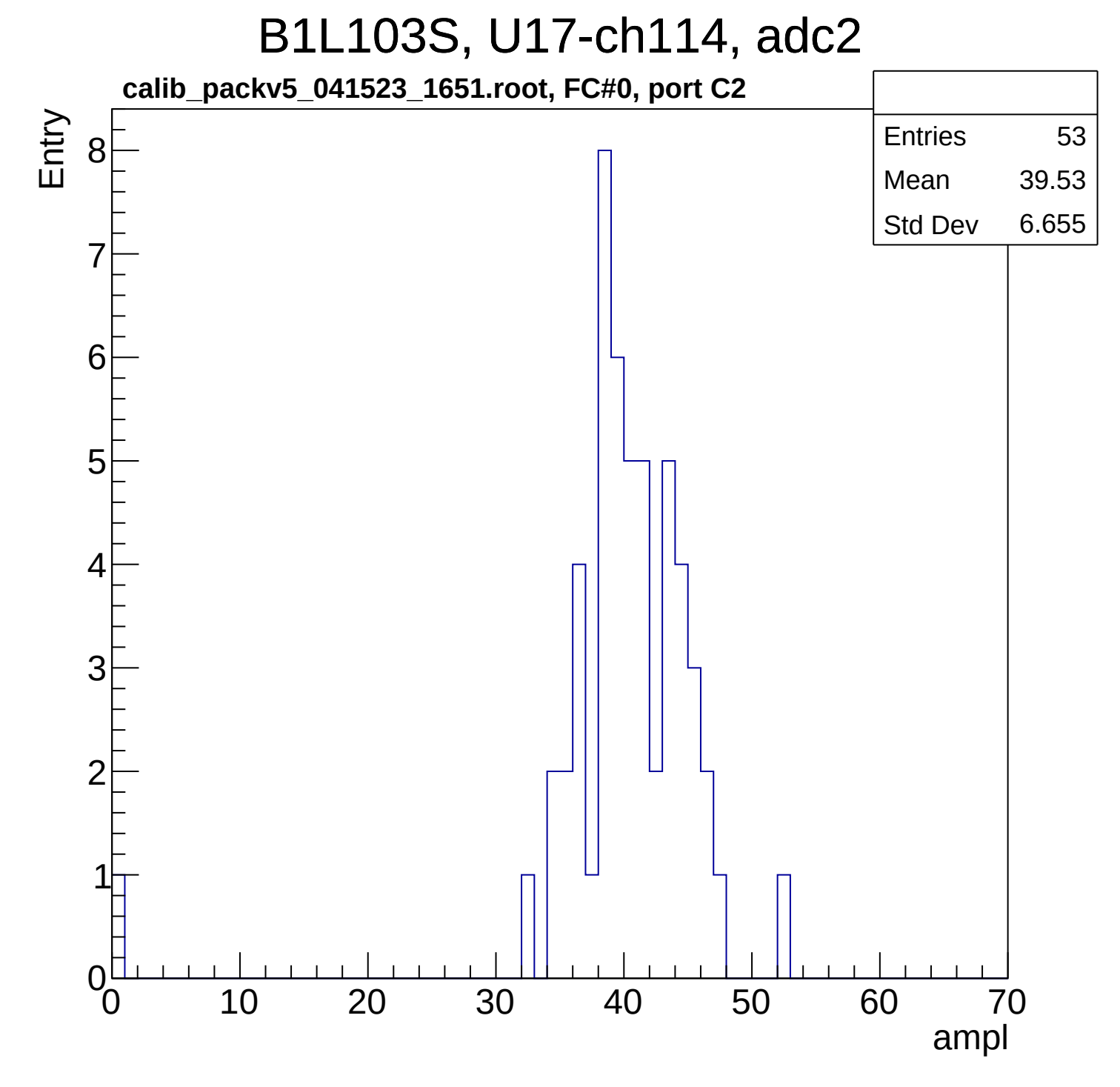
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U17-ch114, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 39.53
Std Dev 6.655
Entry
ampl
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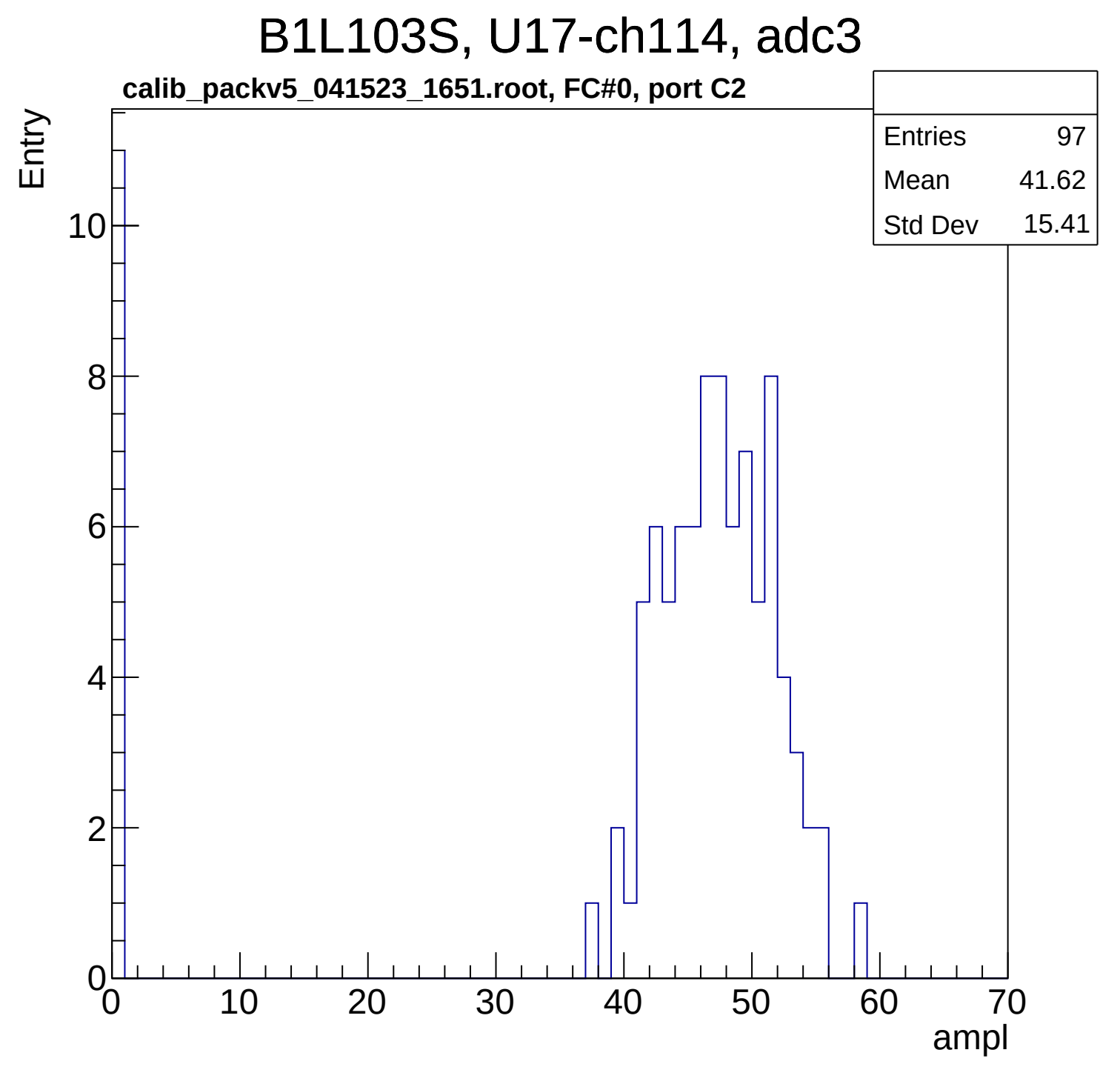
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U17-ch114, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 97
Mean 41.62
Std Dev 15.41
Entry
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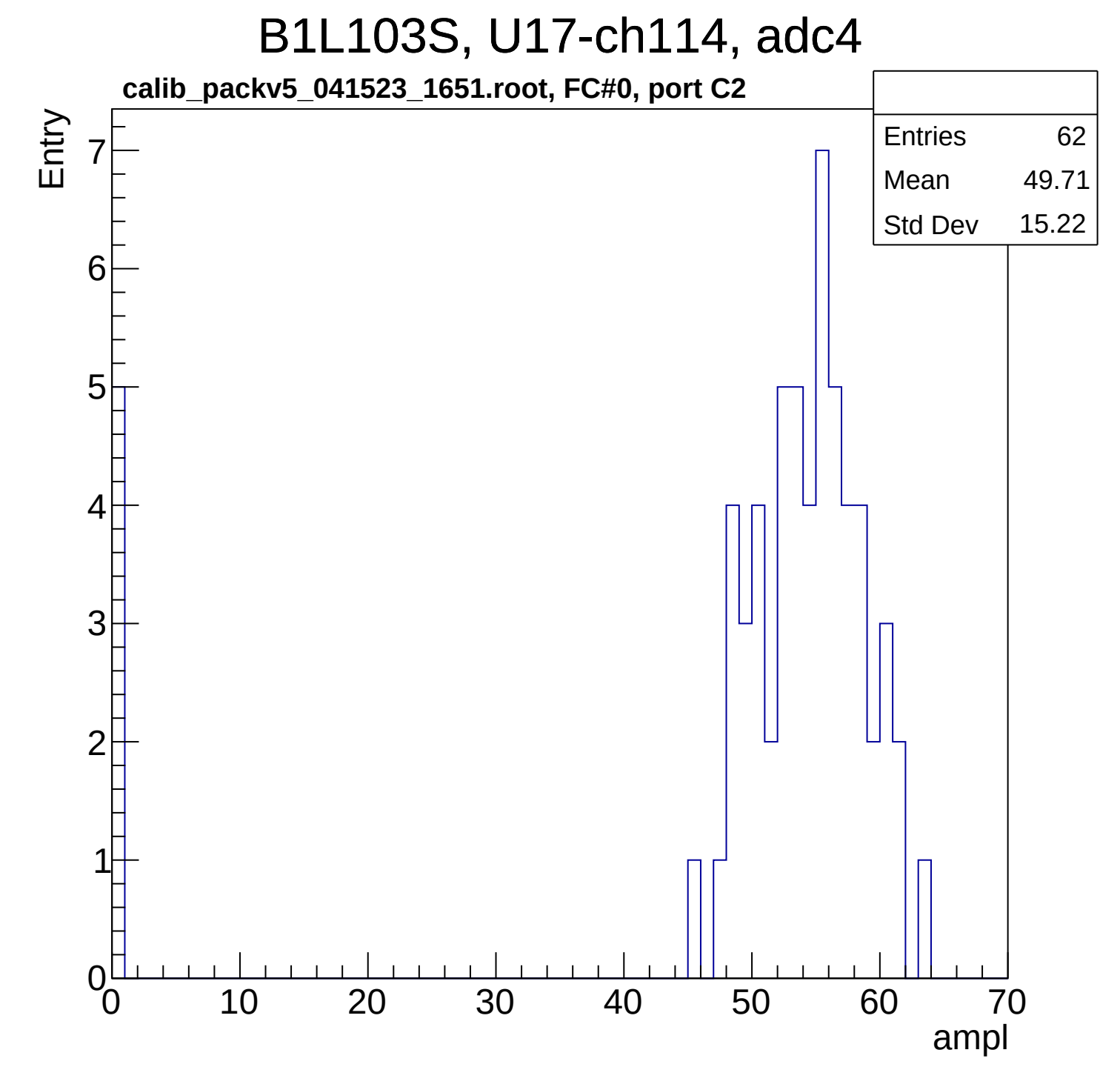
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch114, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 49.71
Std Dev 15.22
Entry
ampl
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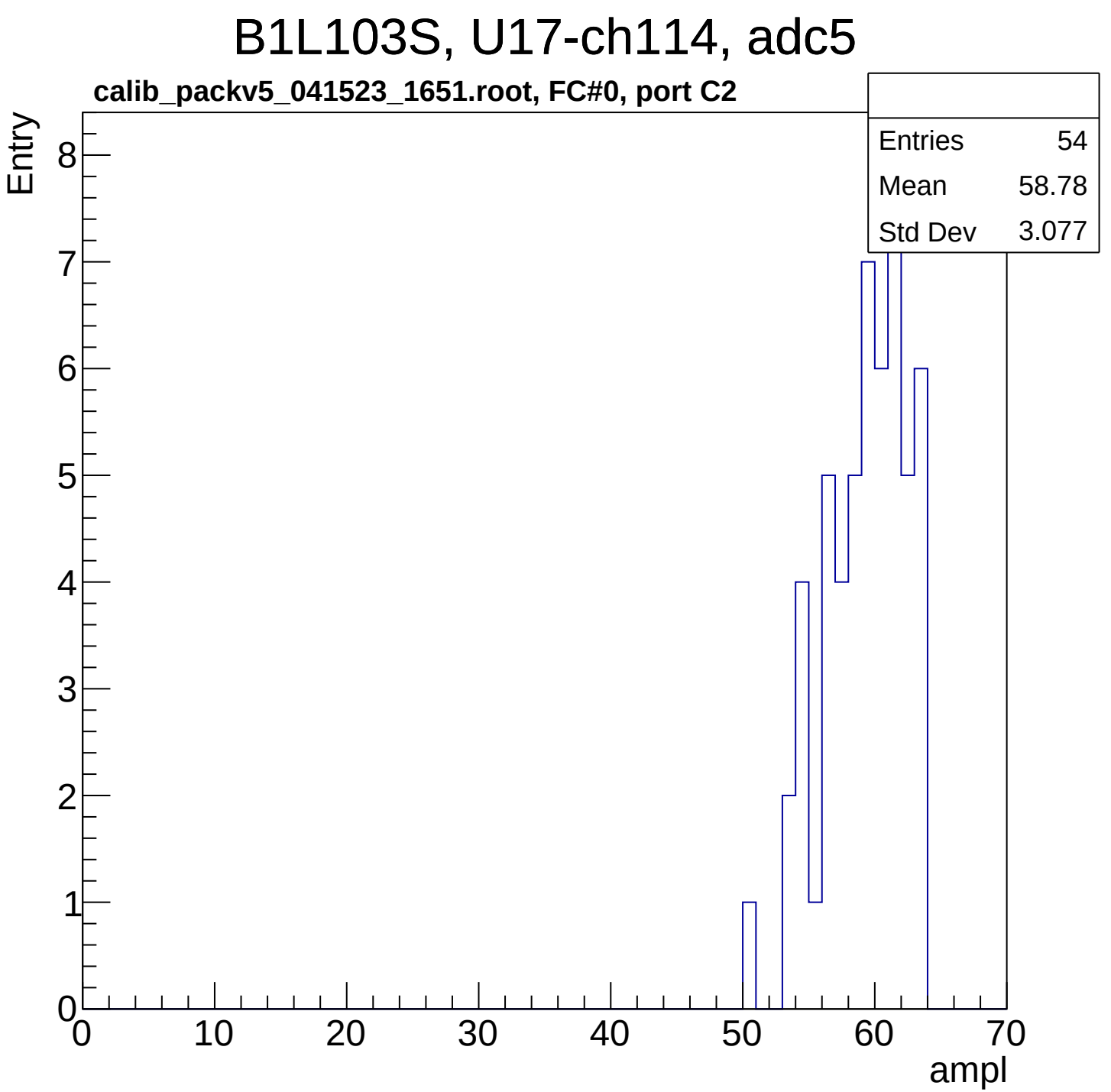
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U17-ch114, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 58.78
Std Dev 3.077
Entry
ampl
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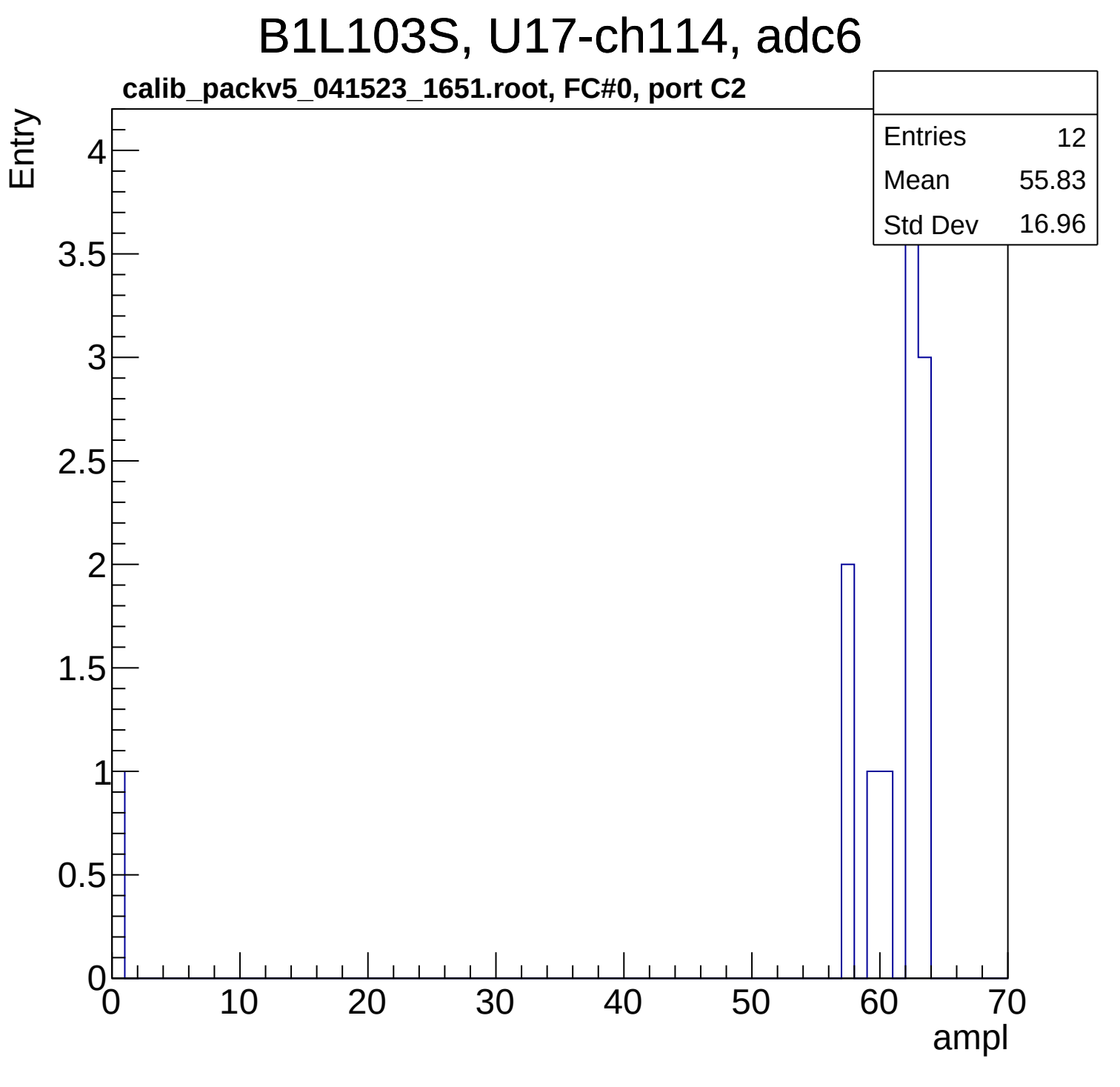
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U17-ch114, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 55.83
Std Dev 16.96
Entry
ampl
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0.5
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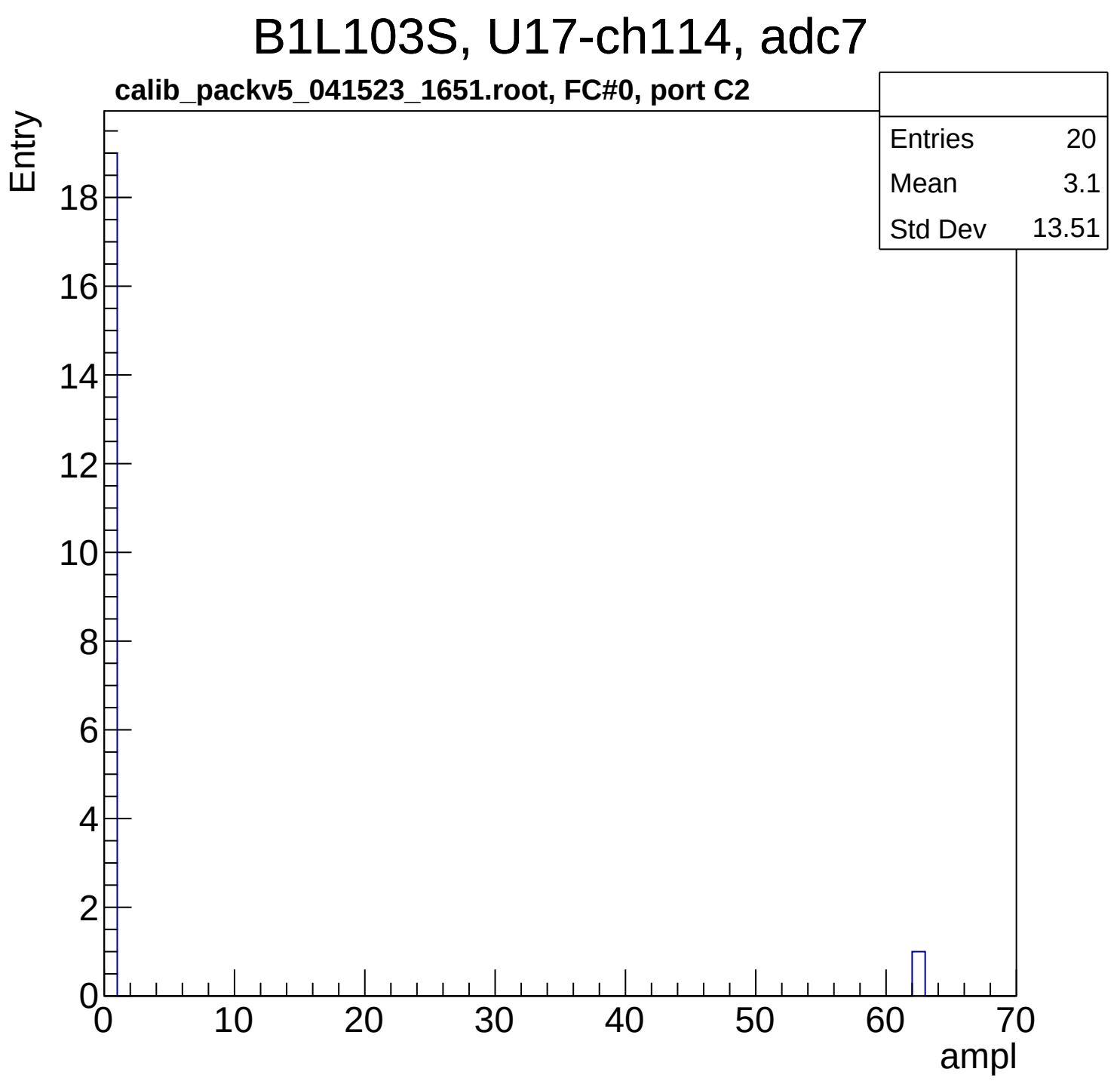
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U17-ch114, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.1
Std Dev 13.51
Entry
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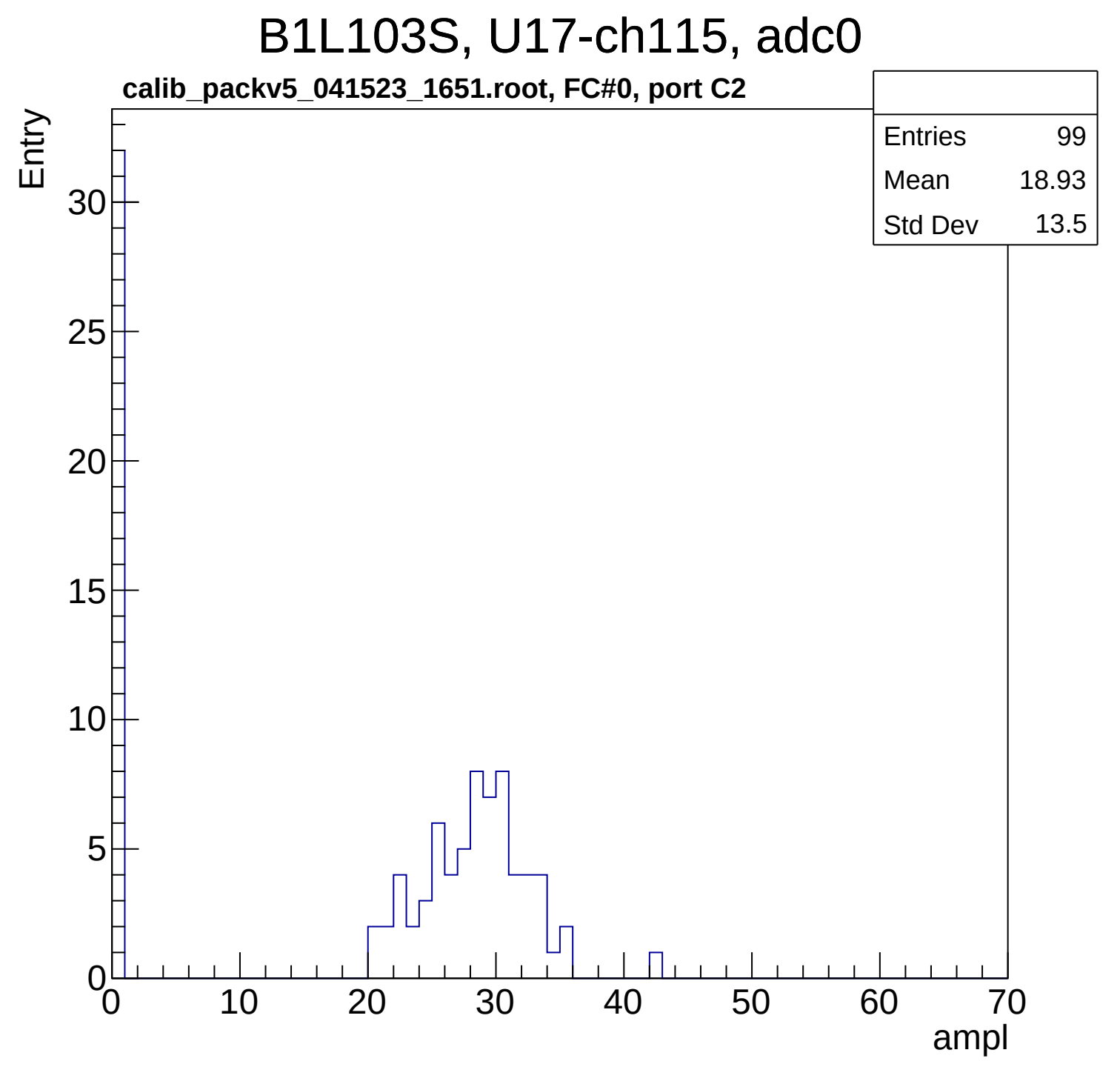
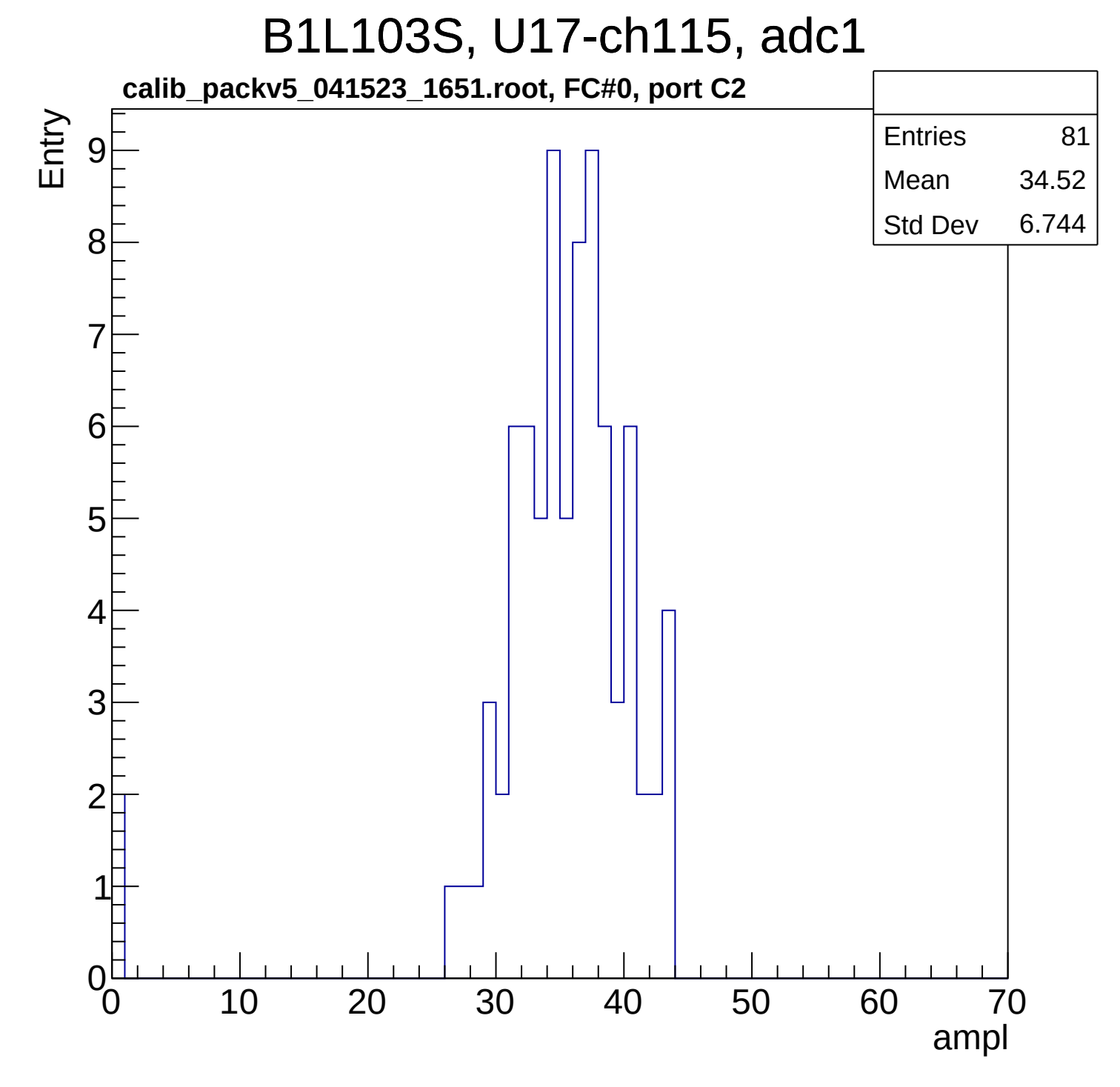
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch115, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 99
Mean 18.93
Std Dev 13.5
Entry
0
5
10
15
20
25
30
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch115, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 34.52
Std Dev 6.744
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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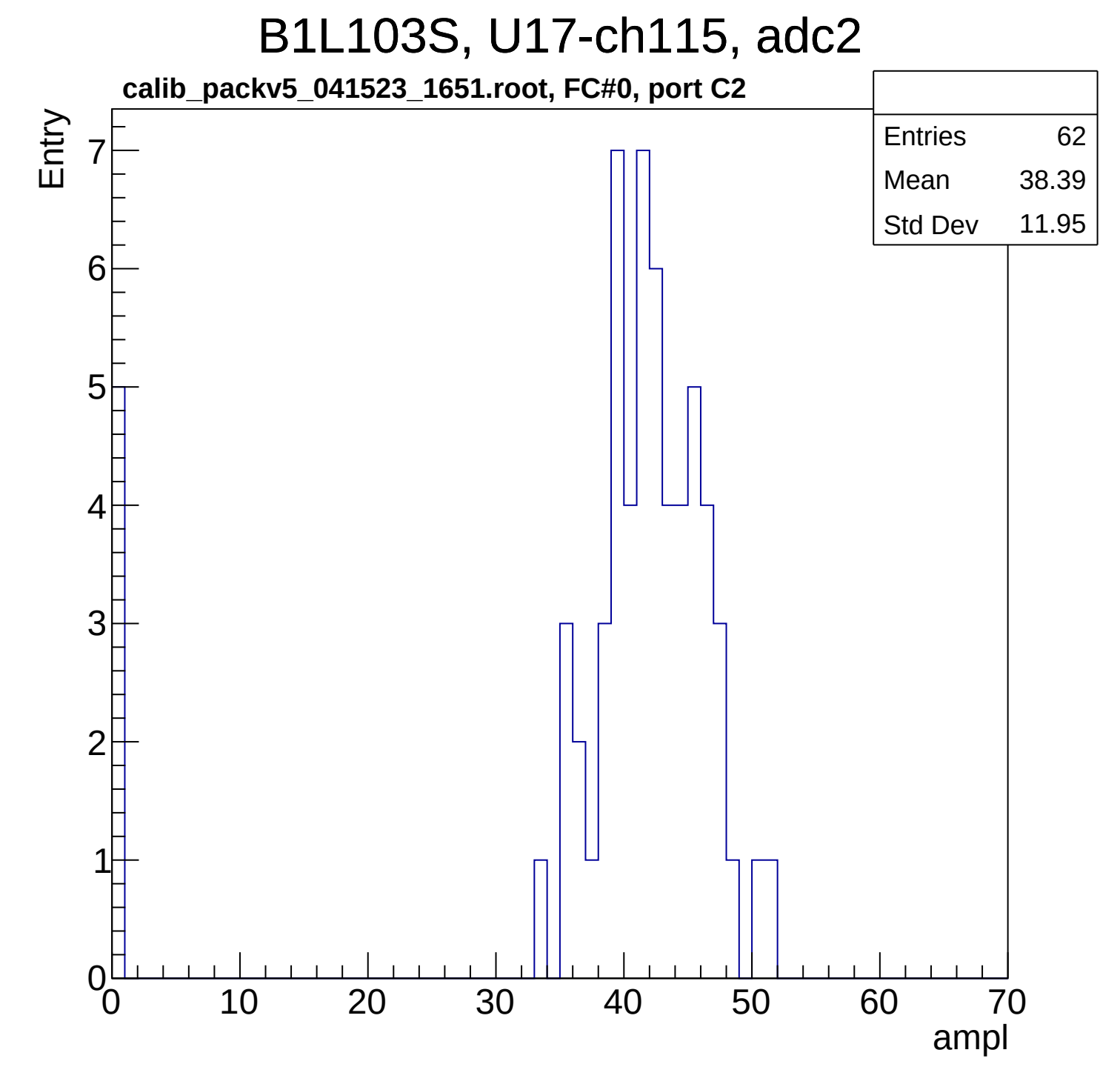
40
50
60
70


B1L103S, U17-ch115, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 38.39
Std Dev 11.95
Entry
ampl
0
1
2
3
4
5
6
7
0
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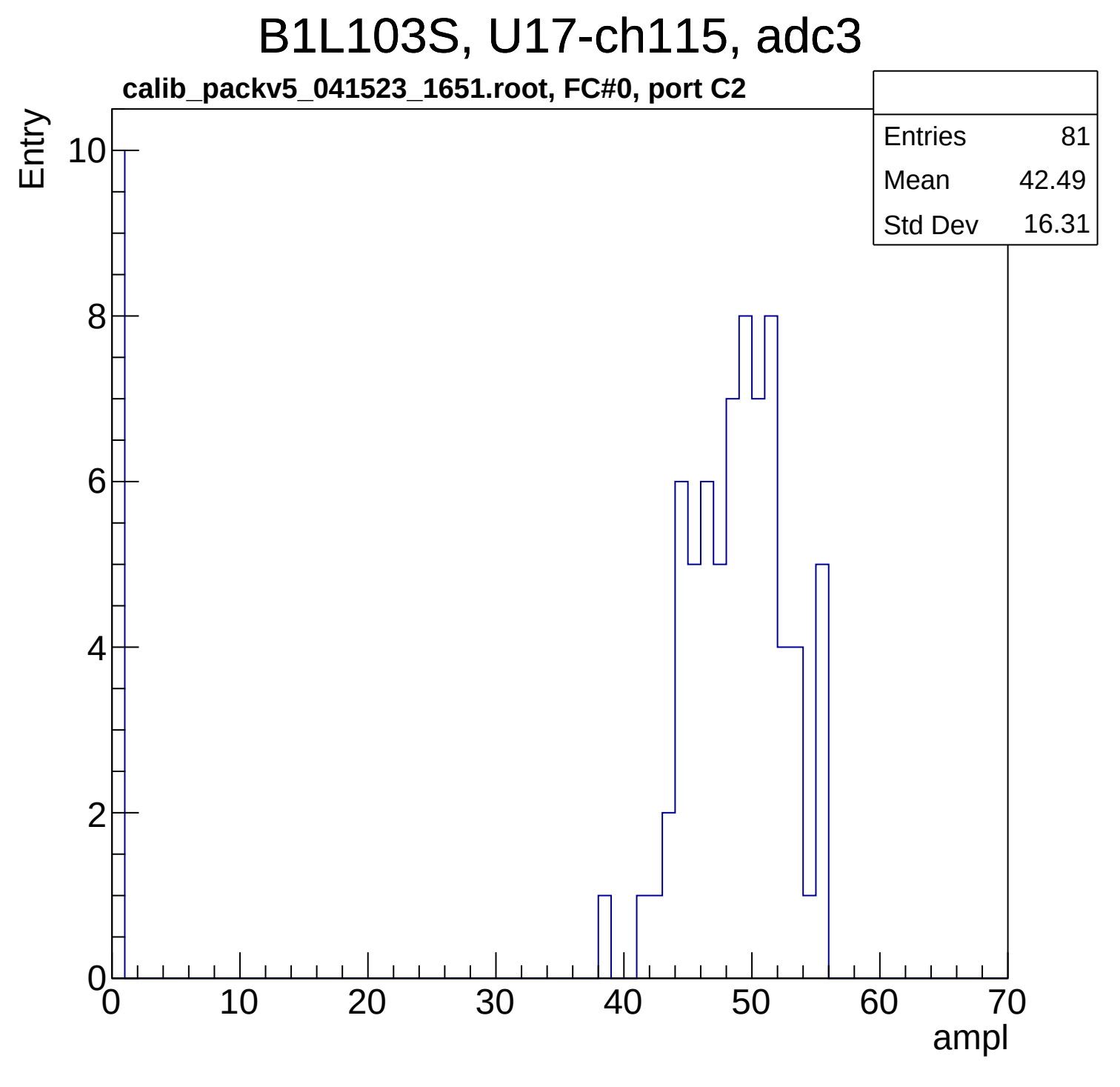
60
70


B1L103S, U17-ch115, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 42.49
Std Dev 16.31
Entry
ampl
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4
6
8
10
0
10
20
30
40
50
60
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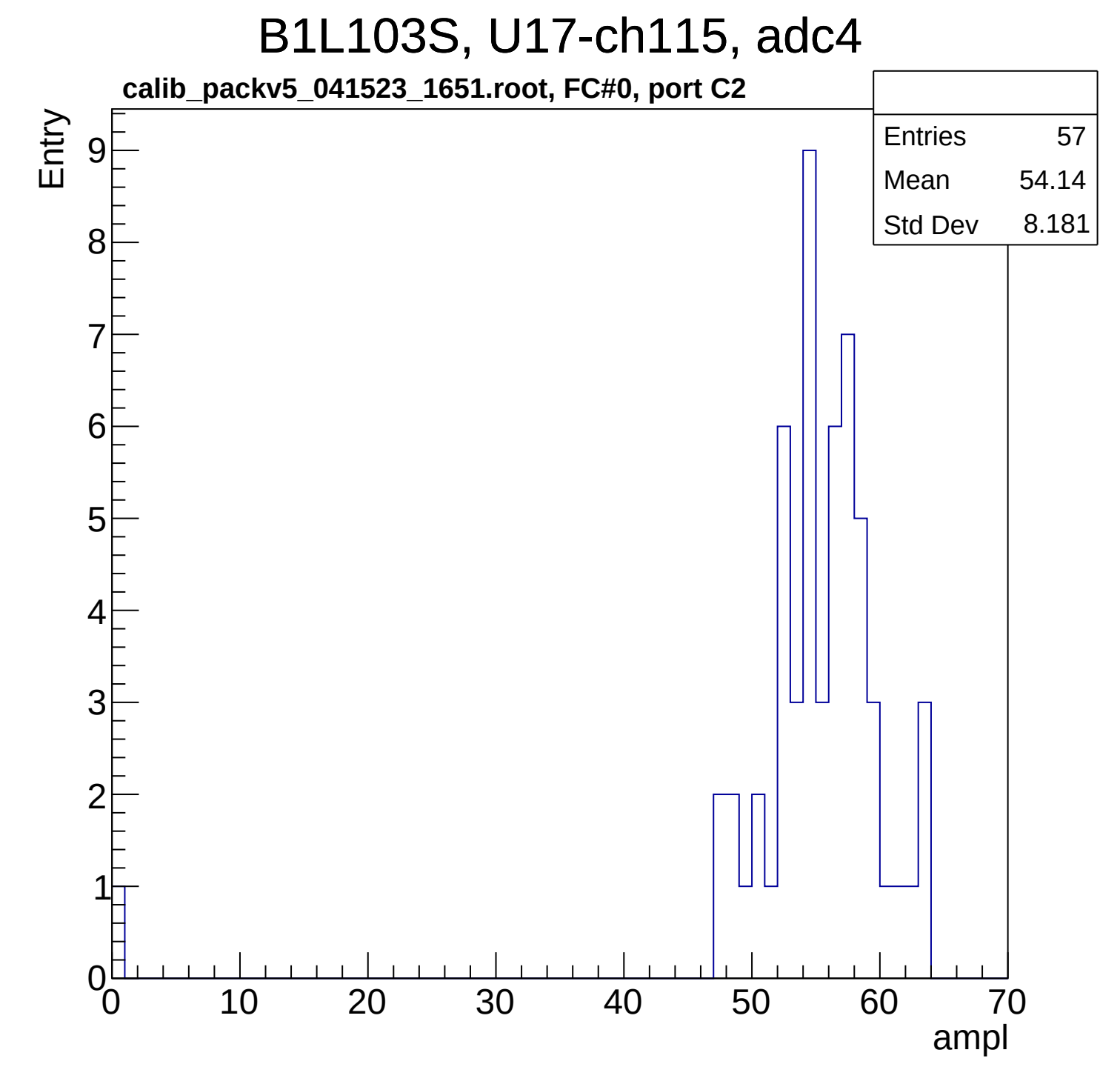
B1L103S, U17-ch115, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 54.14
Std Dev 8.181
Entry
ampl
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2
3
4
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6
7
8
9
0
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60
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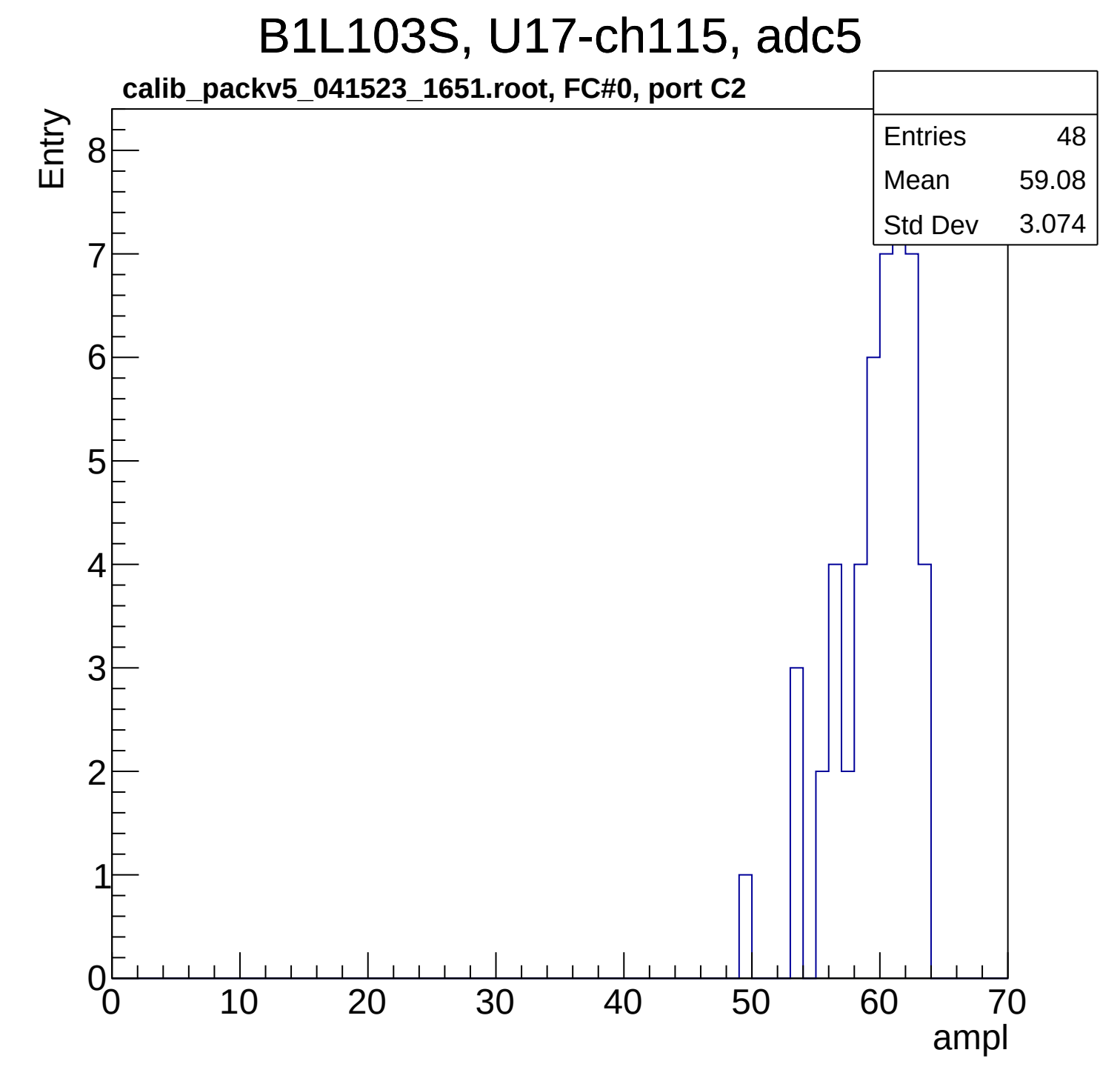
B1L103S, U17-ch115, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 59.08
Std Dev 3.074
Entry
ampl
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3
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5
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7
8
0
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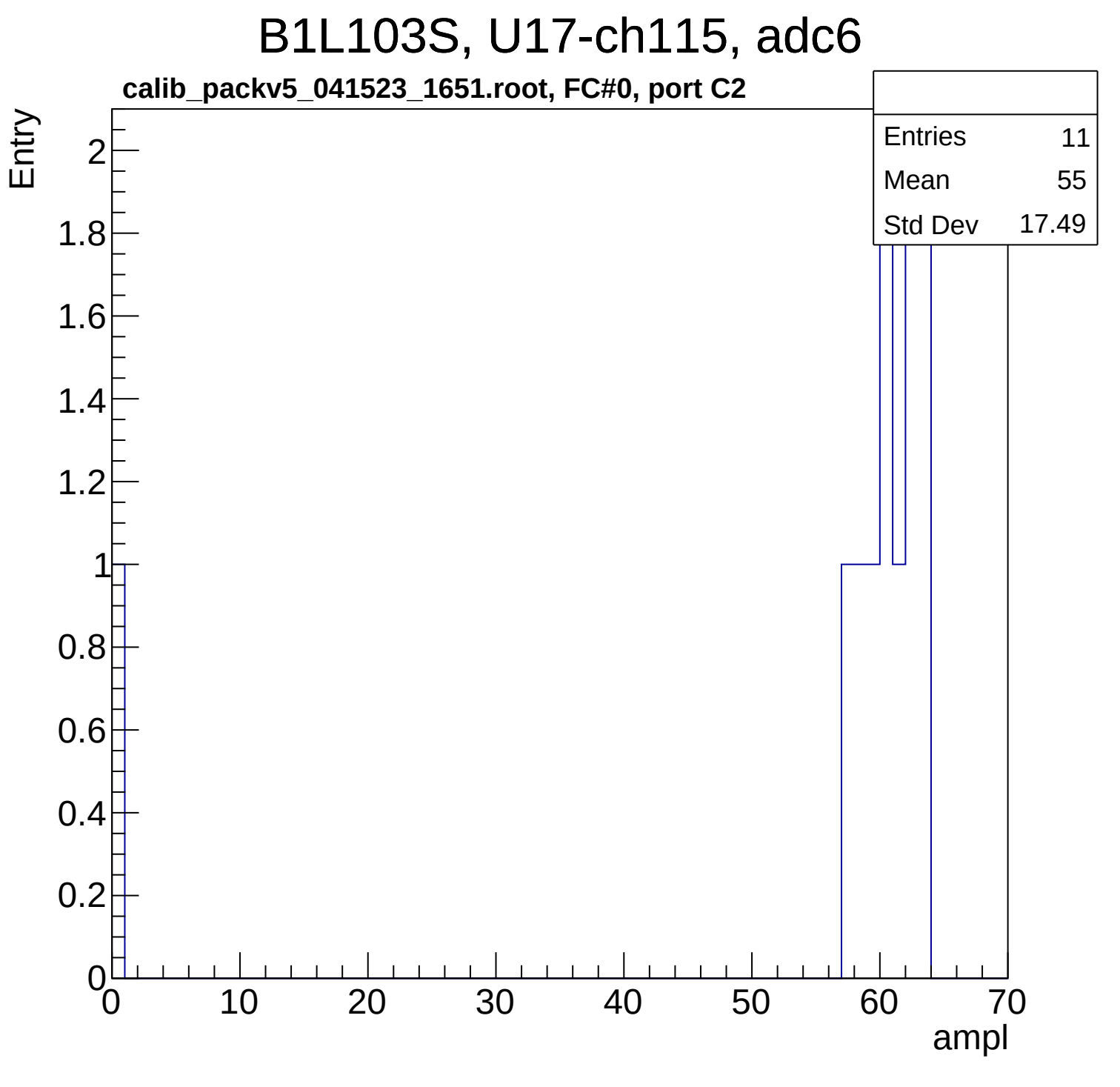
B1L103S, U17-ch115, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 55
Std Dev 17.49
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
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60
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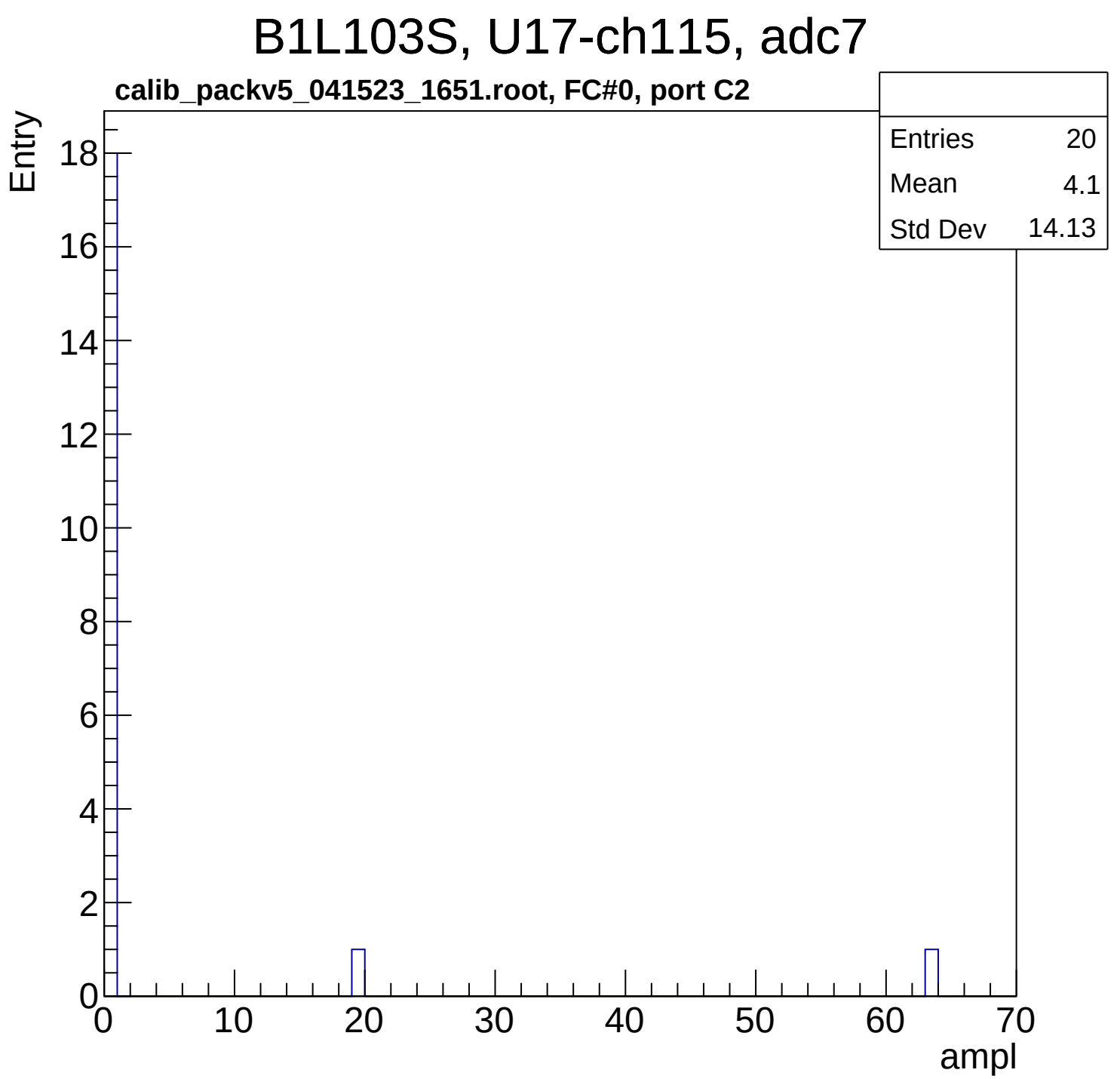
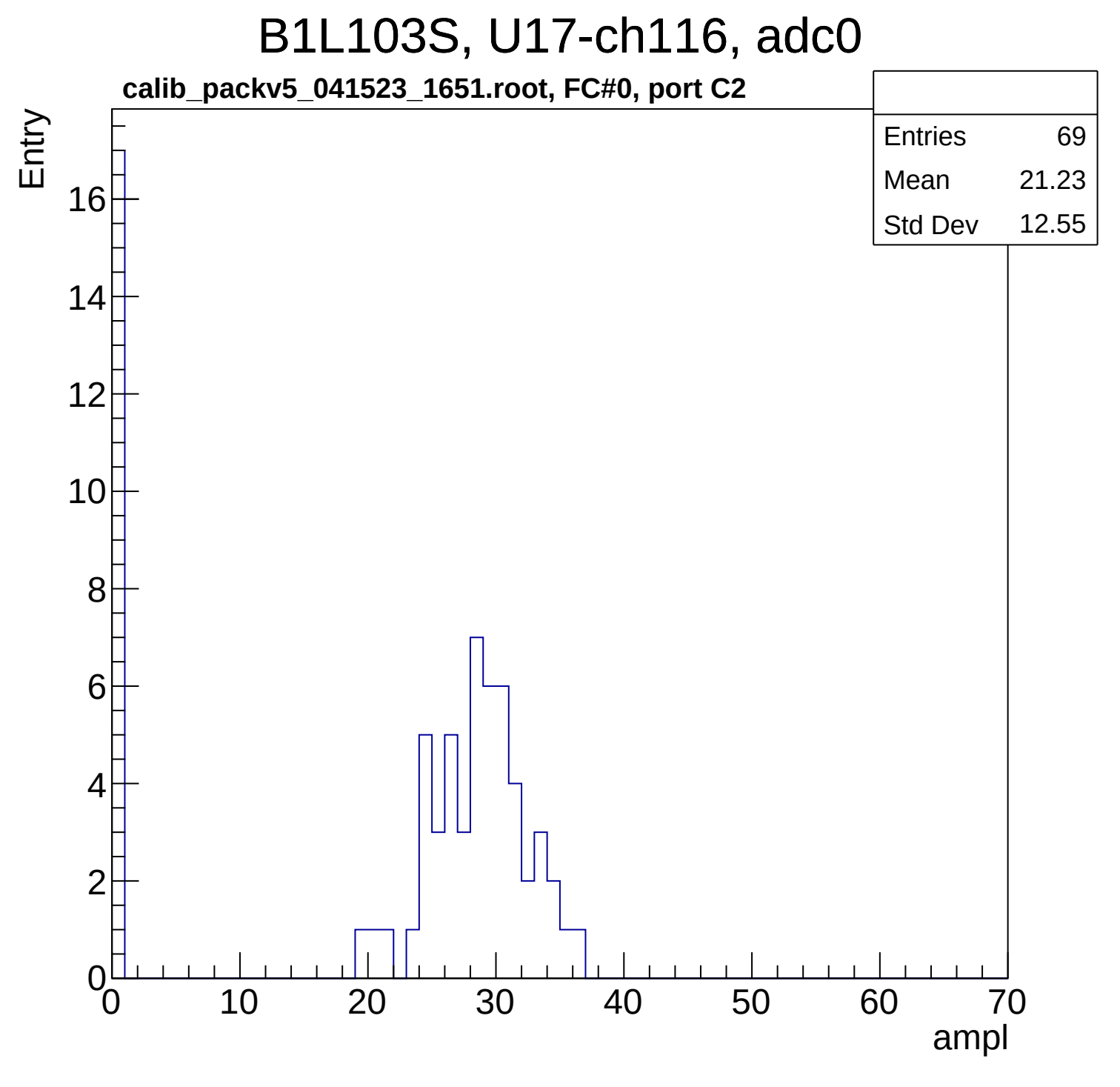
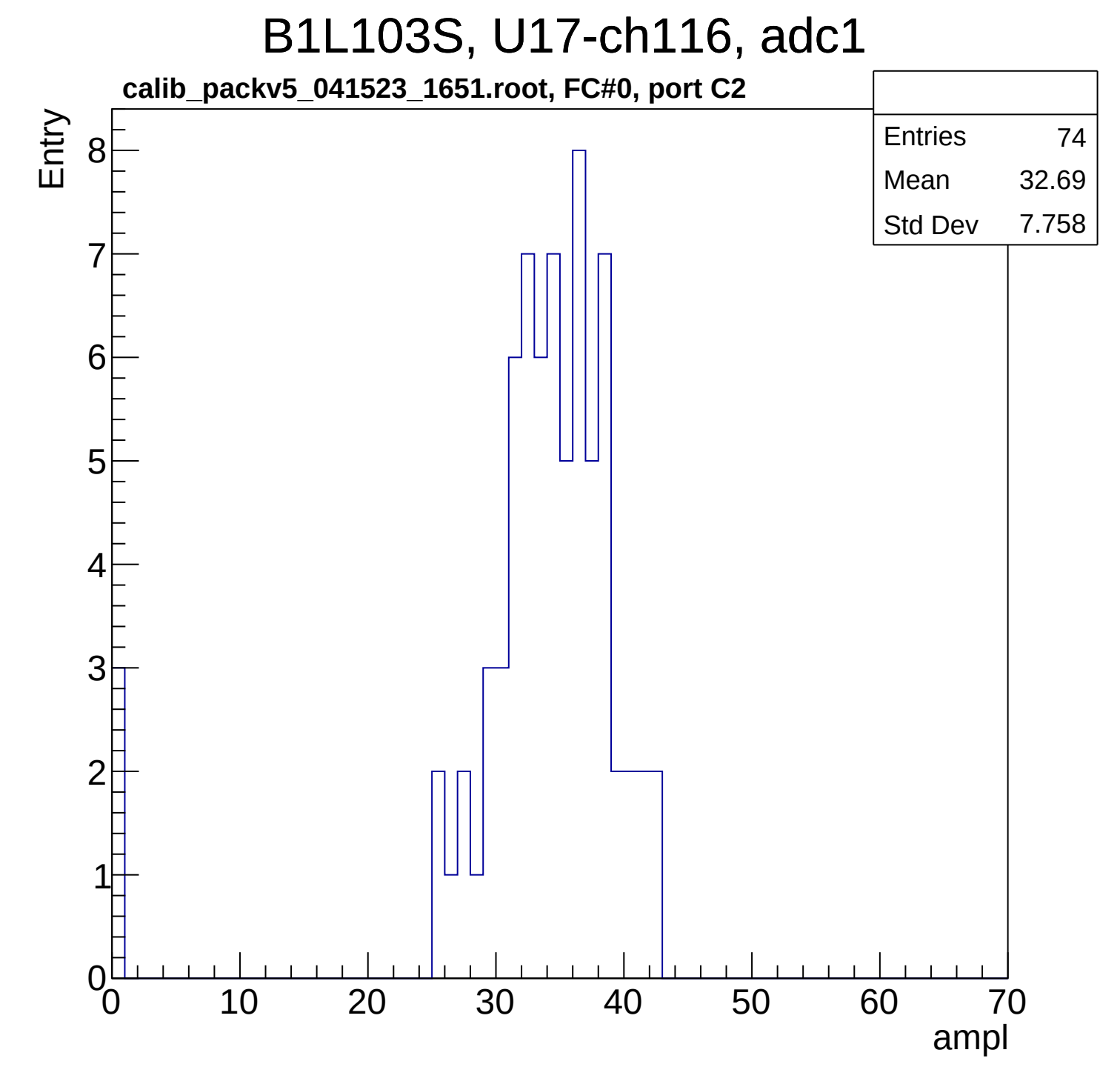

B1L103S, U17-ch115, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 4.1
Std Dev 14.13
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch116, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 21.23
Std Dev 12.55
Entry
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch116, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 32.69
Std Dev 7.758
Entry
ampl
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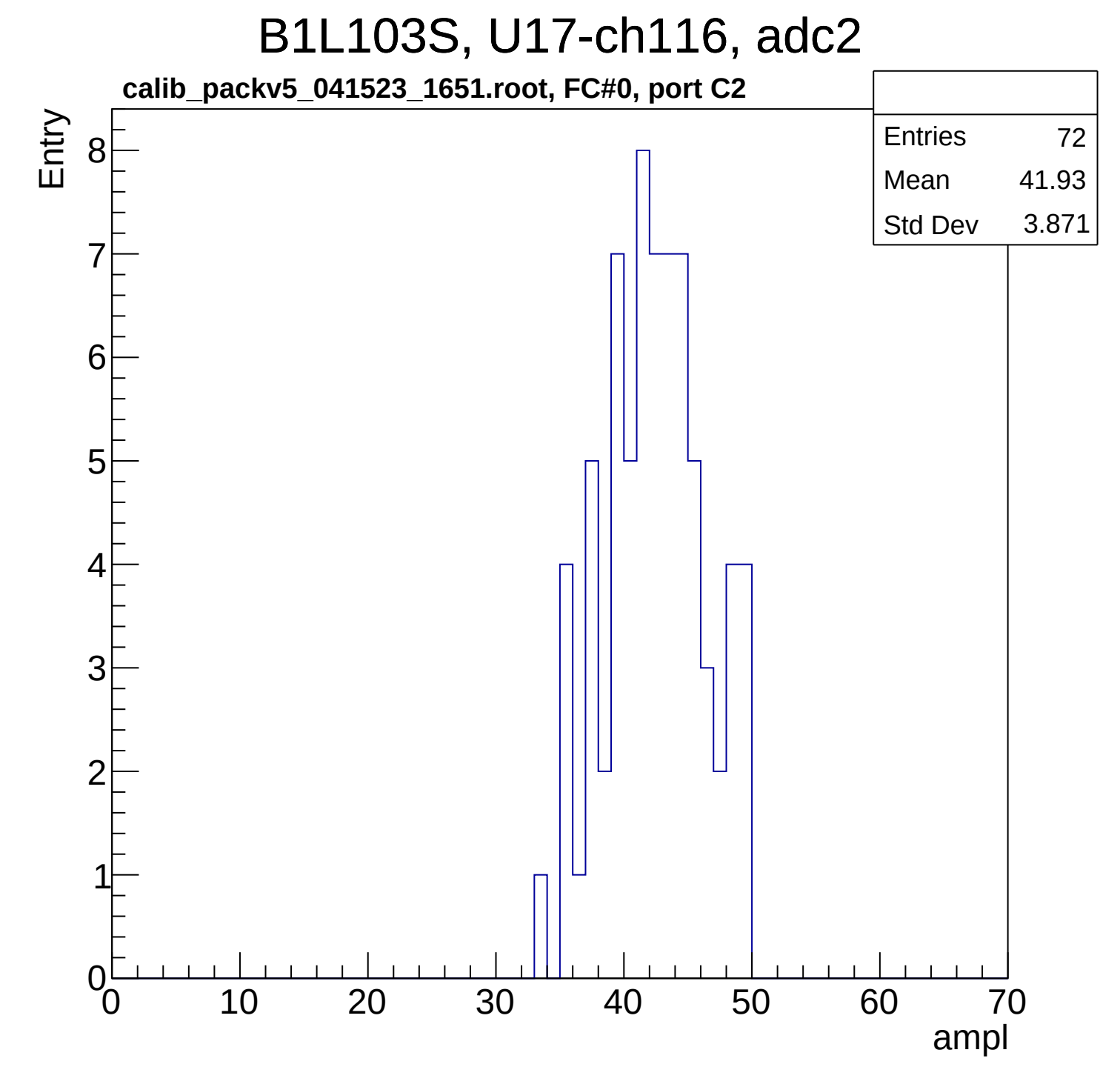
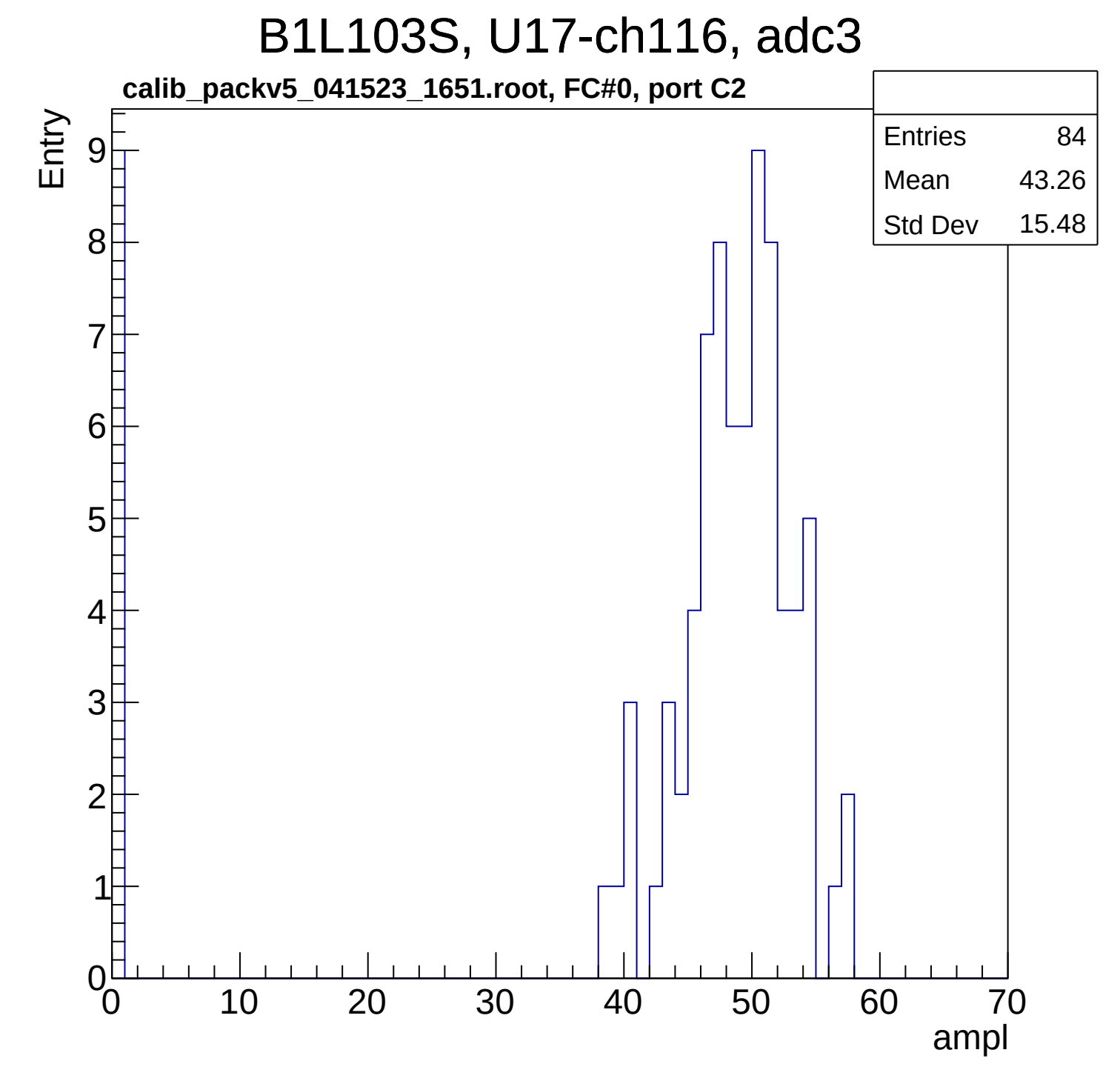
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U17-ch116, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 41.93
Std Dev 3.871
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U17-ch116, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 43.26
Std Dev 15.48
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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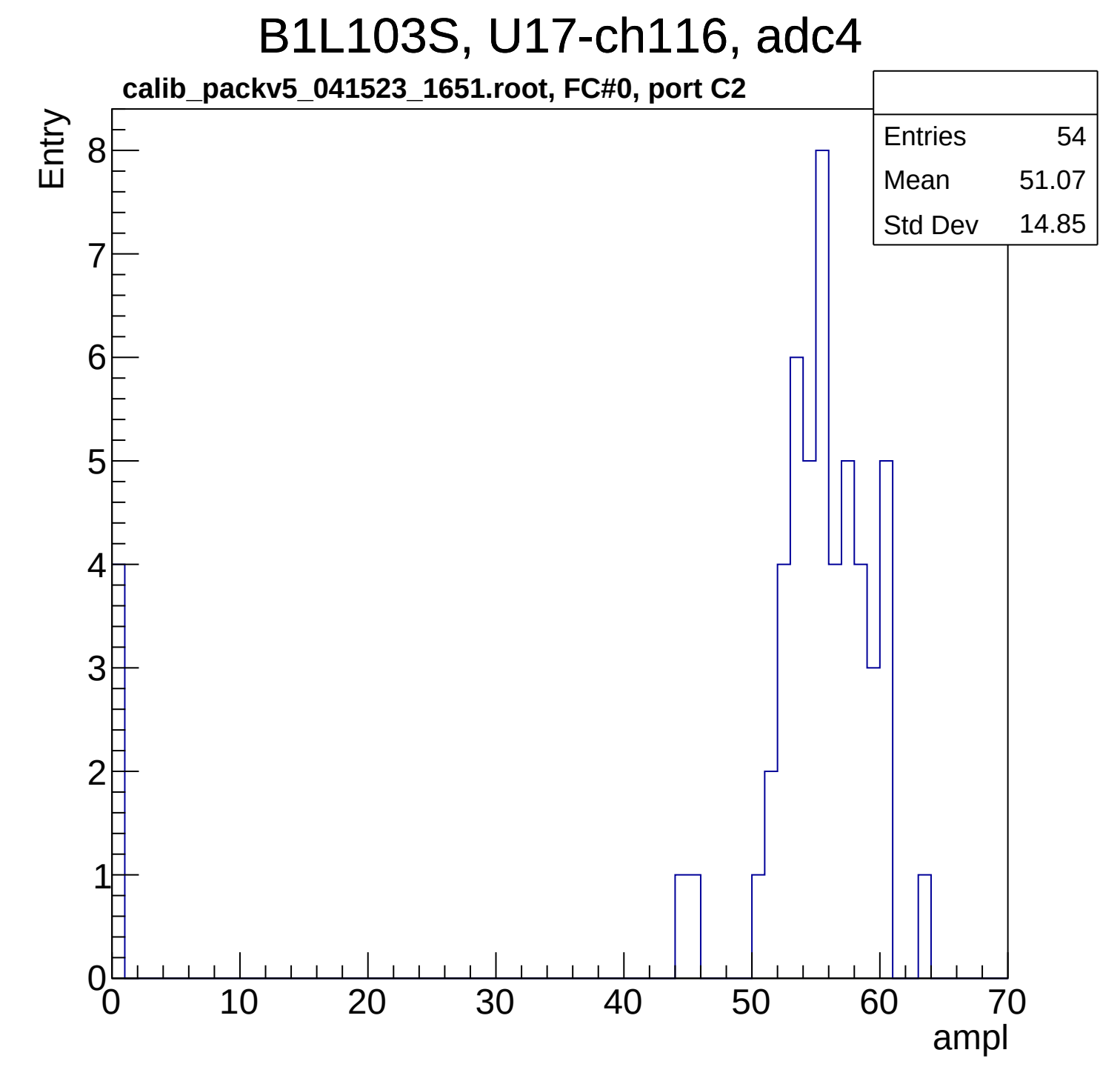
B1L103S, U17-ch116, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 51.07
Std Dev 14.85
Entry
ampl
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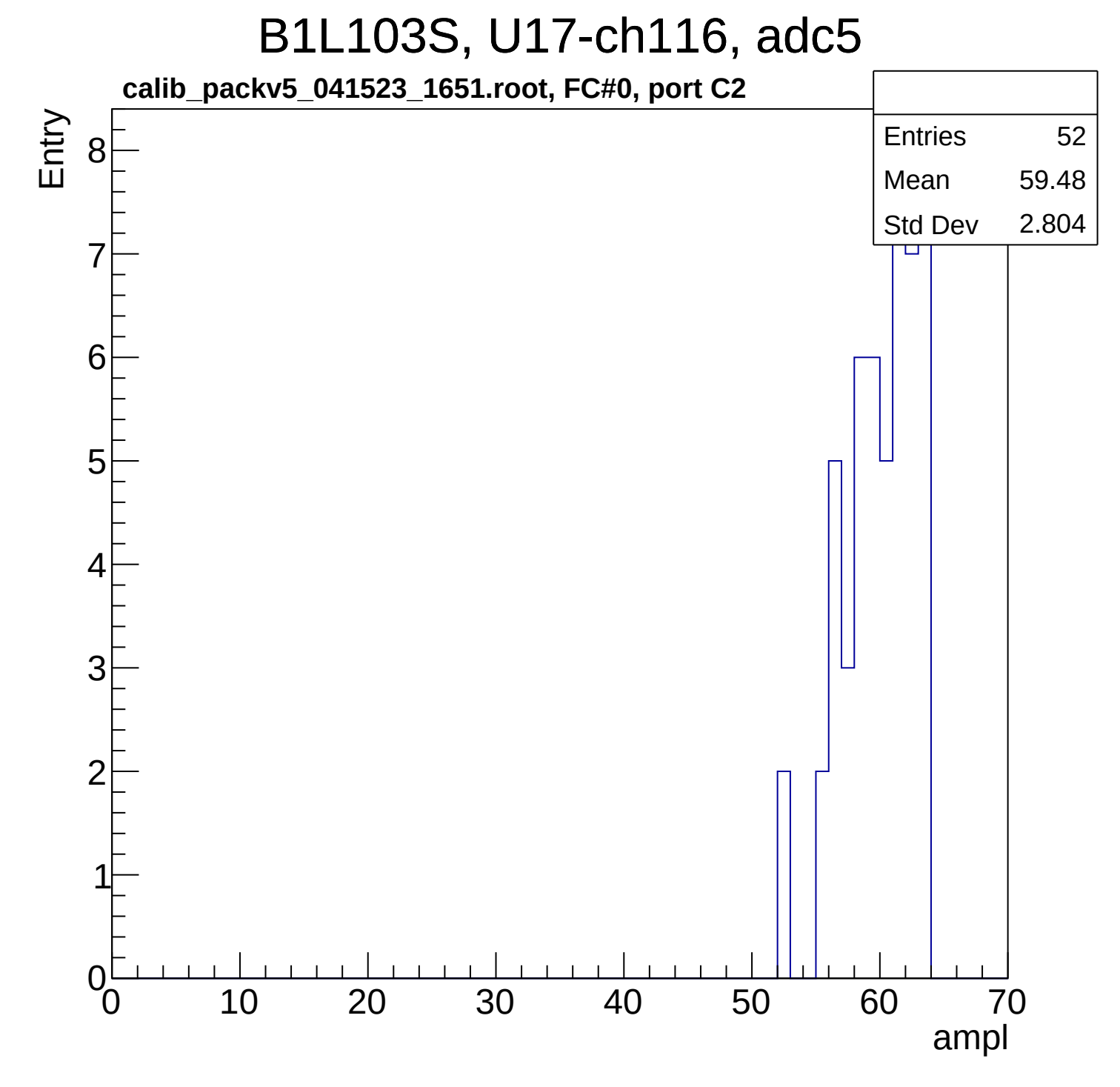
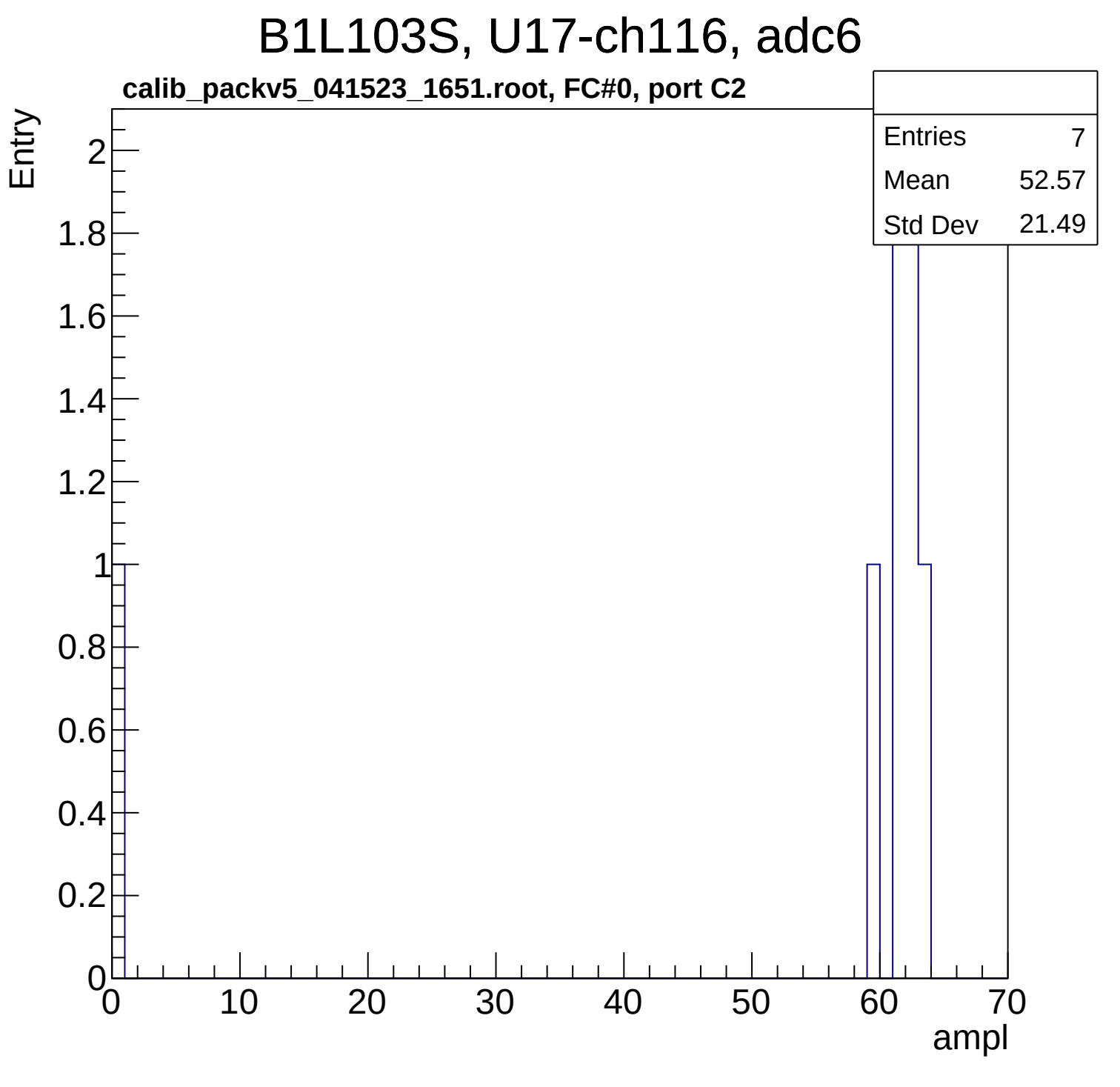
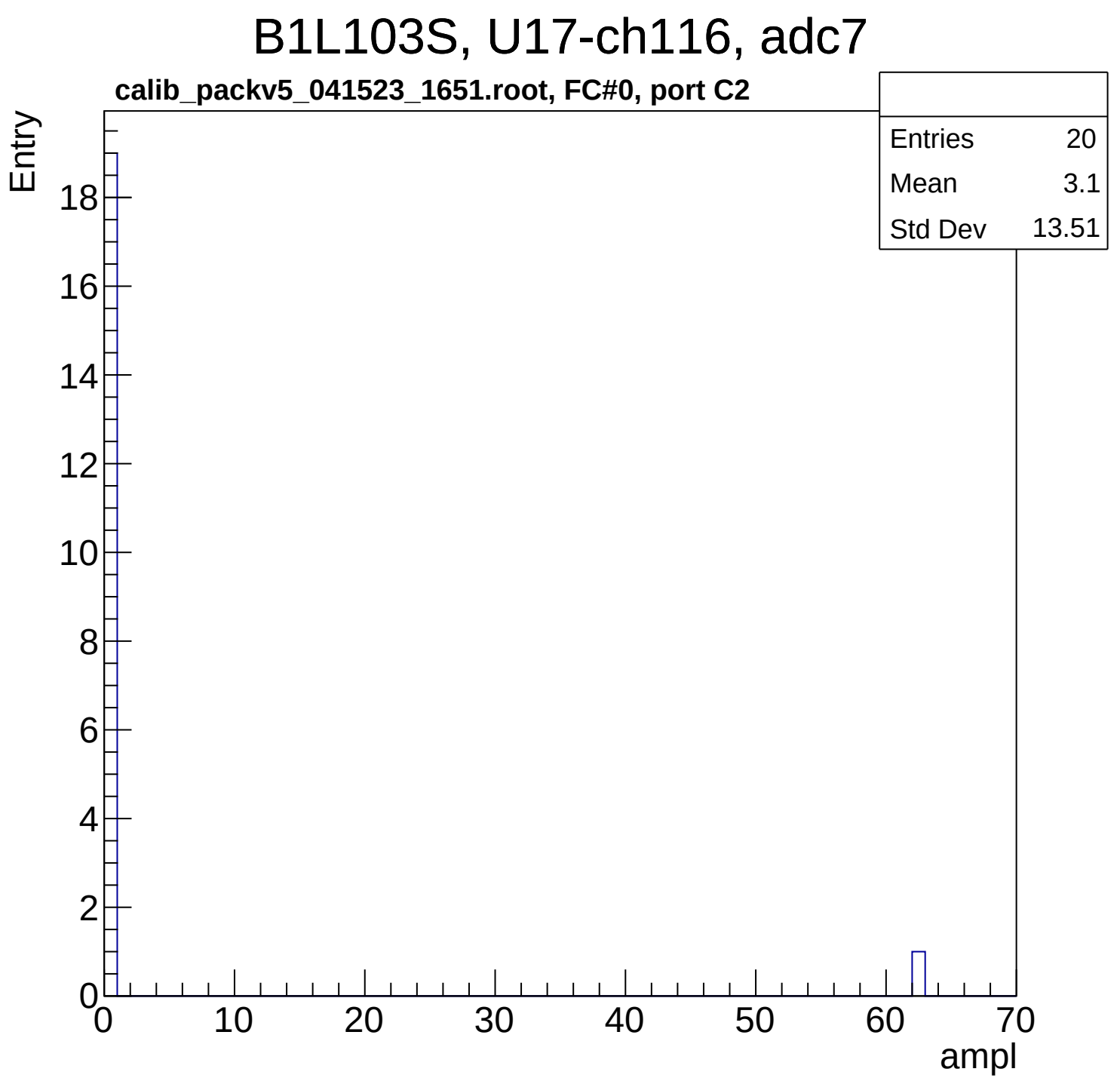
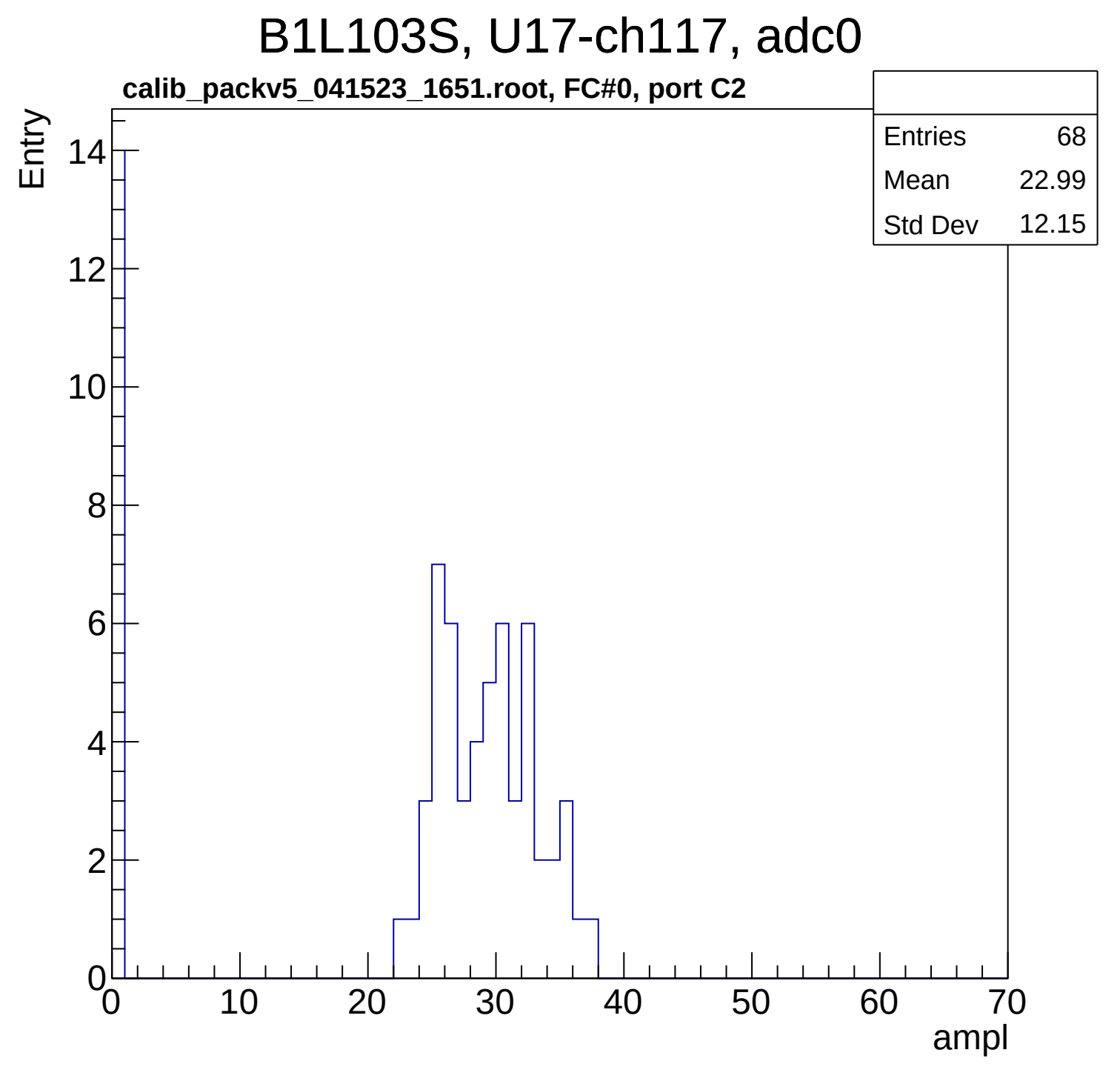
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U17-ch116, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 59.48
Std Dev 2.804
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U17-ch116, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 52.57
Std Dev 21.49
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U17-ch116, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.1
Std Dev 13.51
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch117, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 22.99
Std Dev 12.15
Entry
ampl
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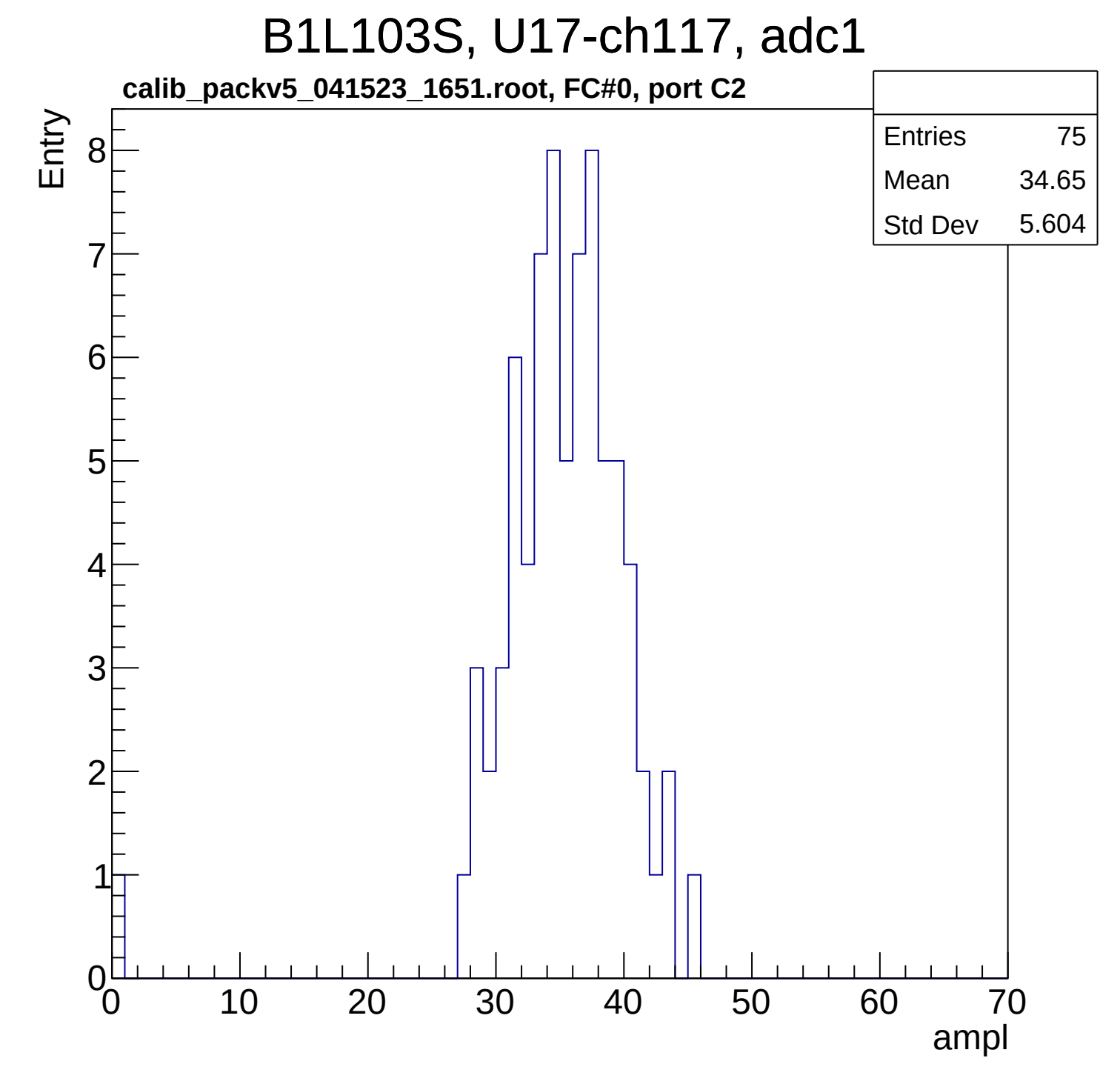
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L103S, U17-ch117, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 34.65
Std Dev 5.604
Entry
ampl
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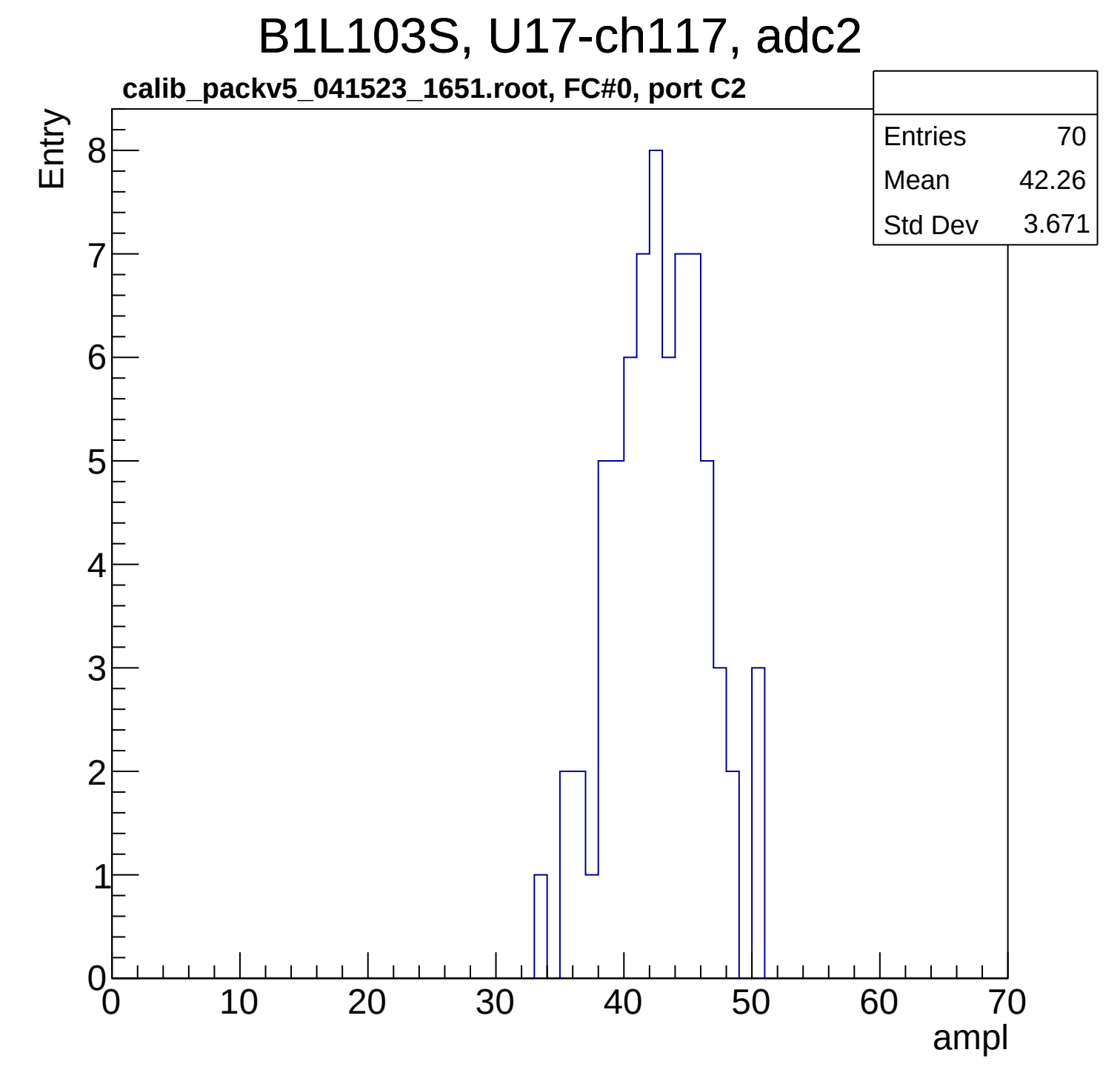
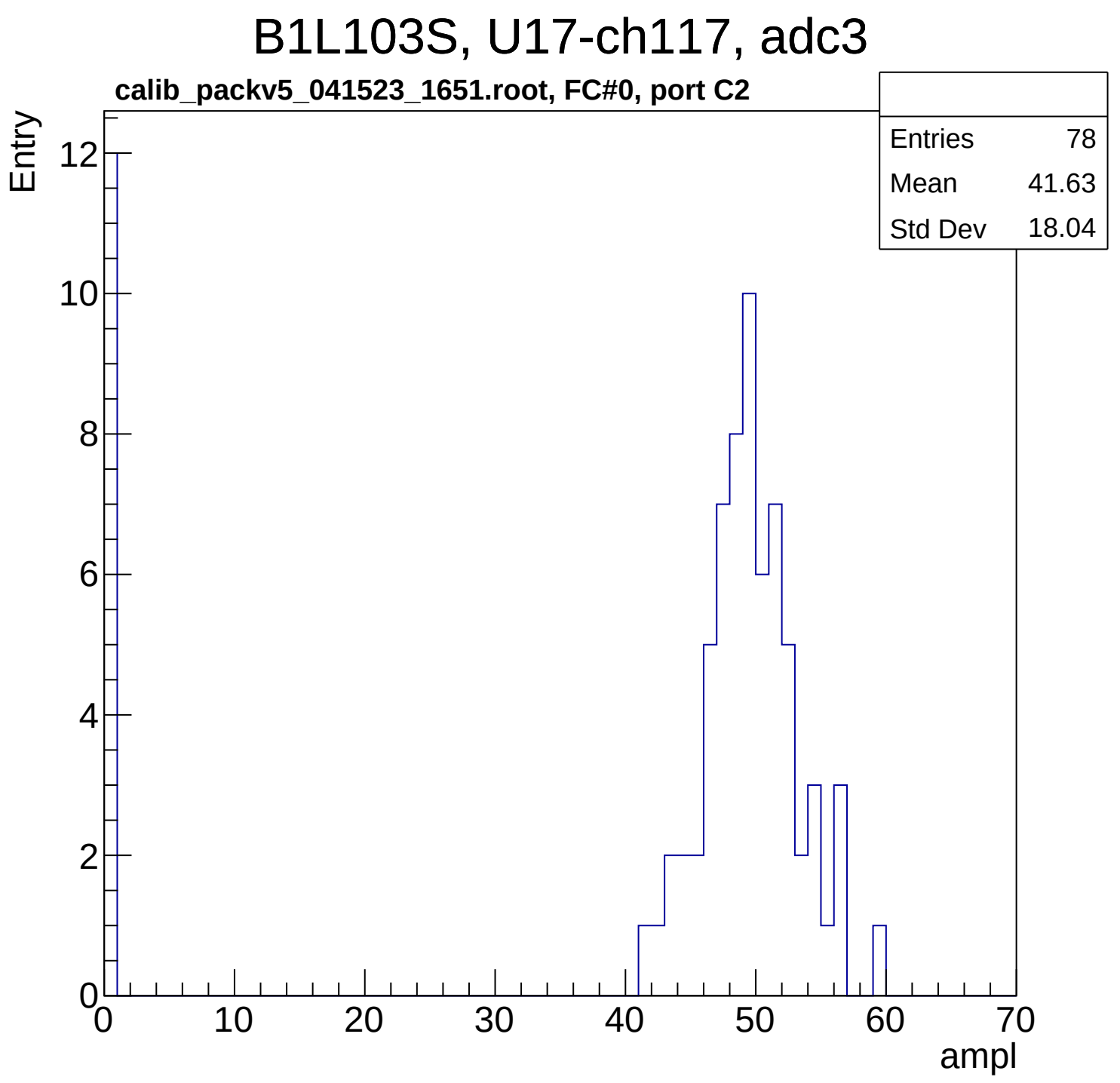
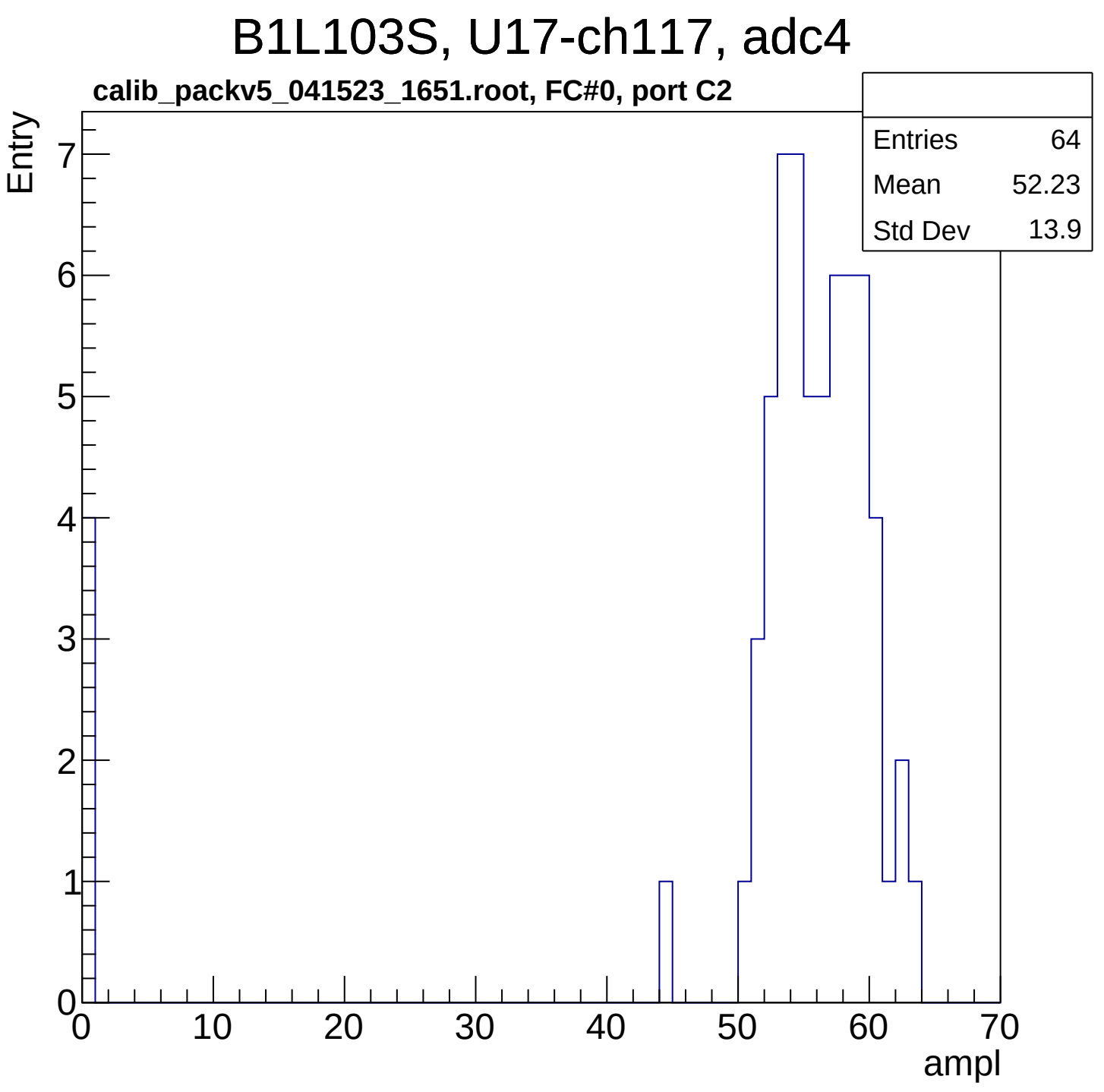
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U17-ch117, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 42.26
Std Dev 3.671
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U17-ch117, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 41.63
Std Dev 18.04
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch117, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 52.23
Std Dev 13.9
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
30
40
50
60
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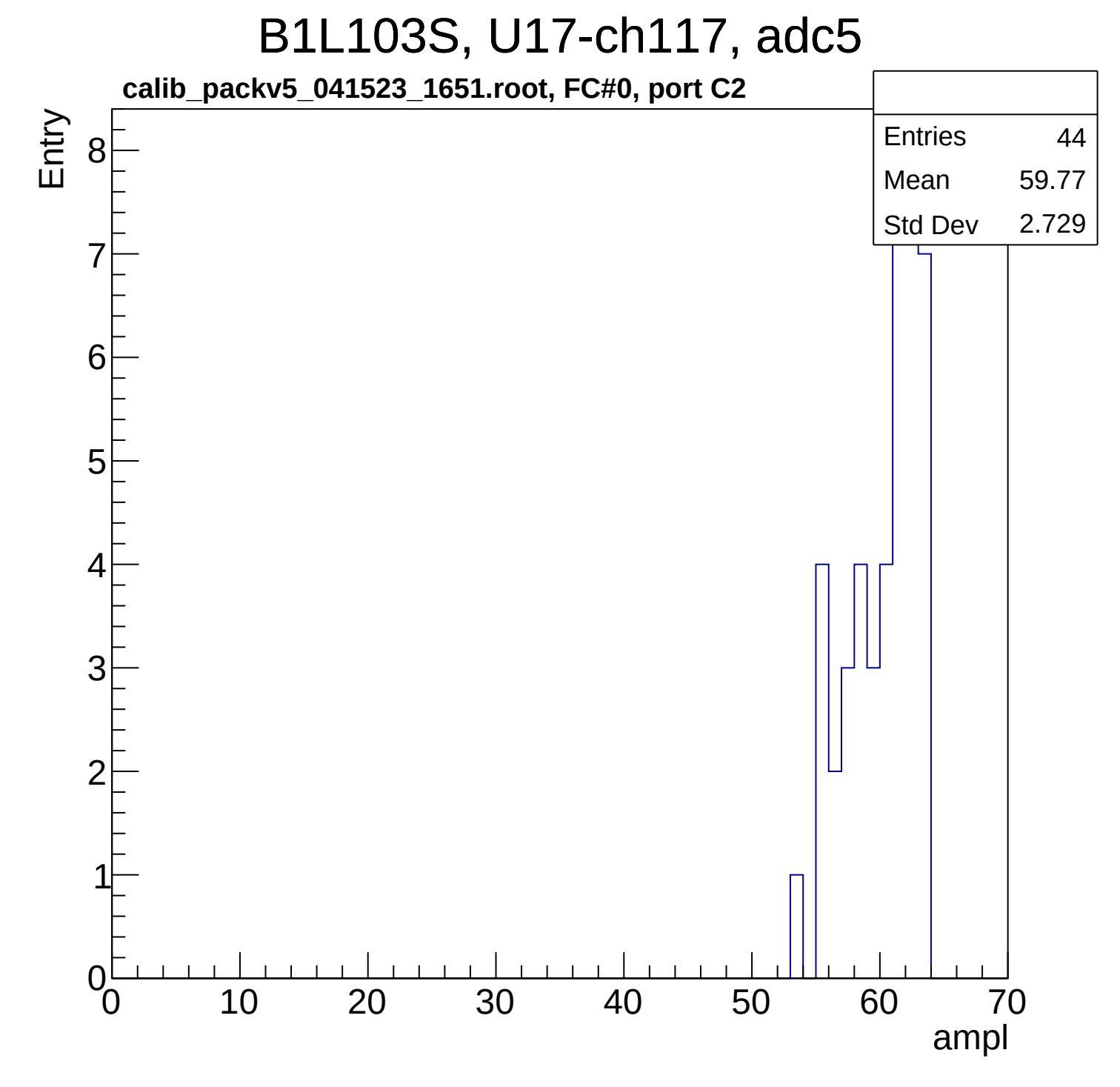
B1L103S, U17-ch117, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 59.77
Std Dev 2.729
Entry
ampl
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2
3
4
5
6
7
8
0
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20
30
40
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60
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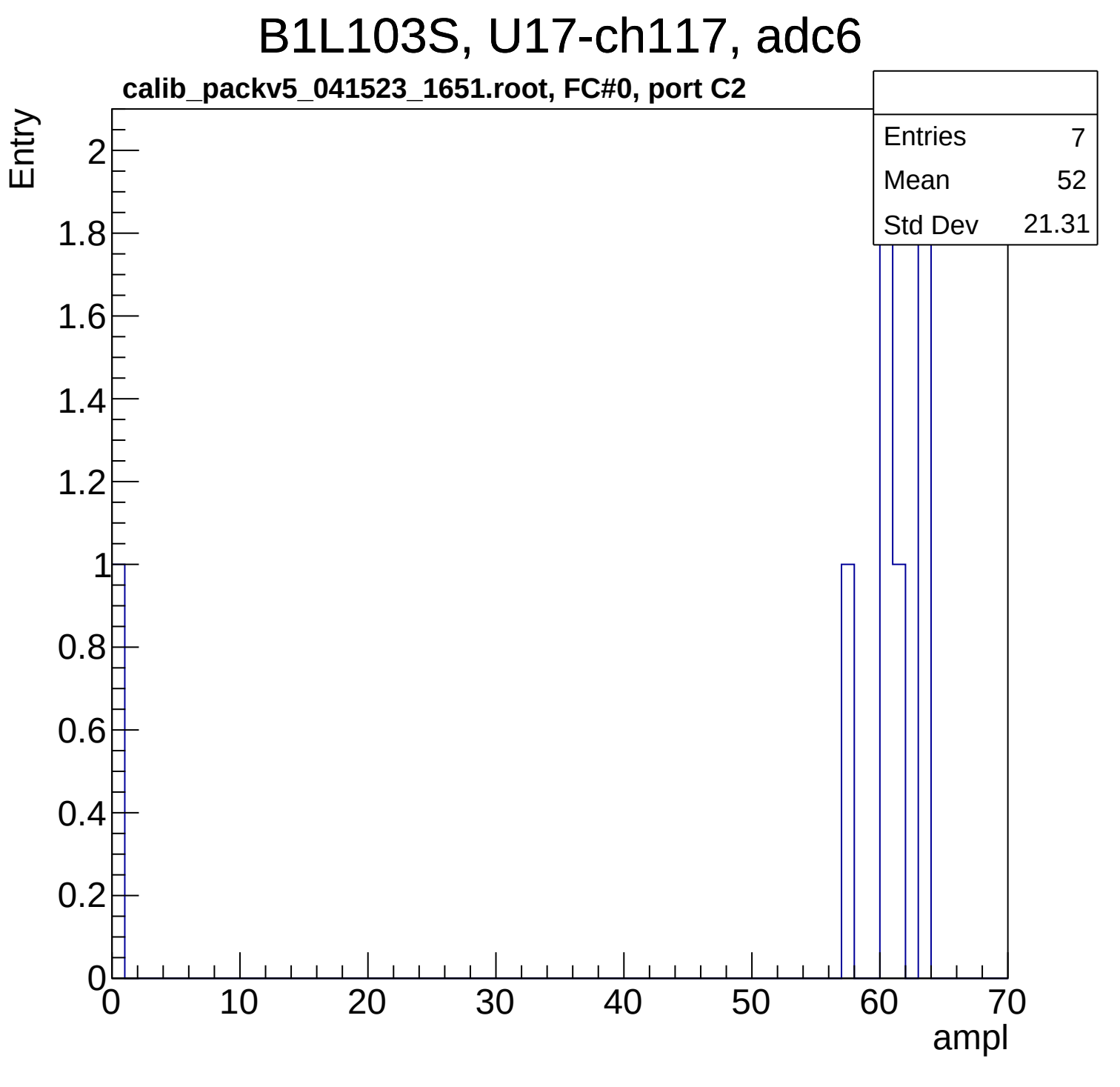
B1L103S, U17-ch117, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 52
Std Dev 21.31
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
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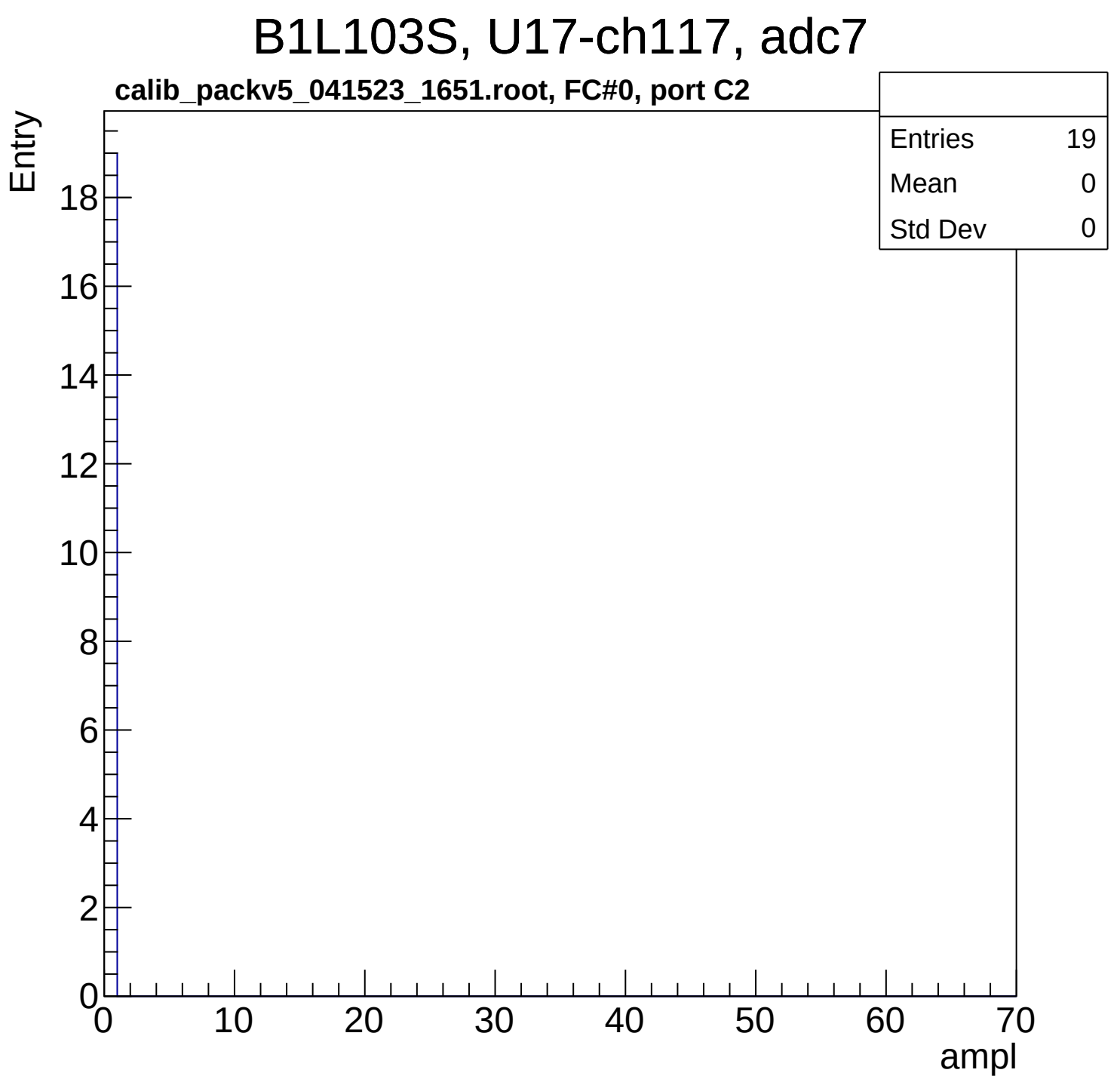
B1L103S, U17-ch117, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
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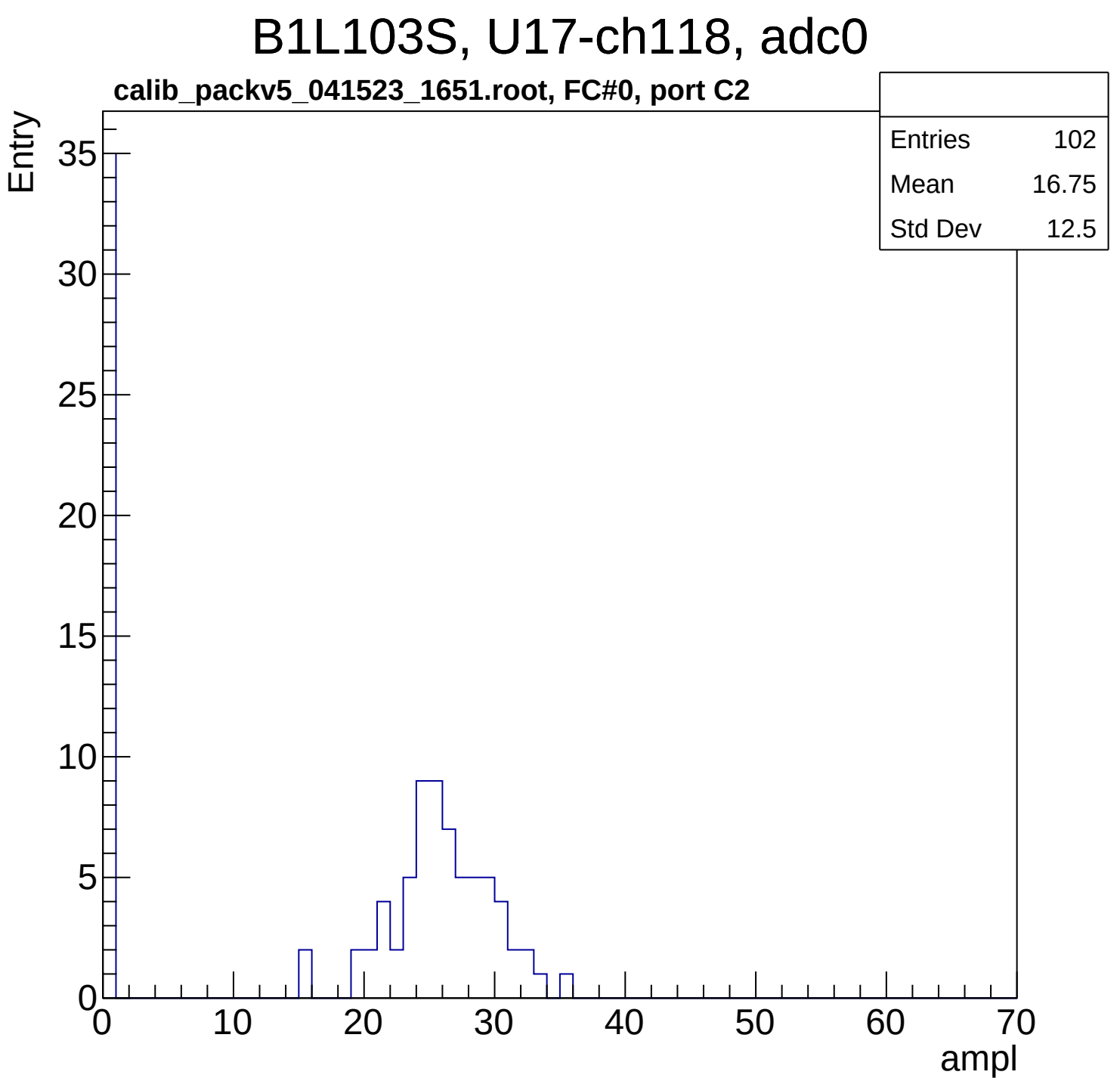
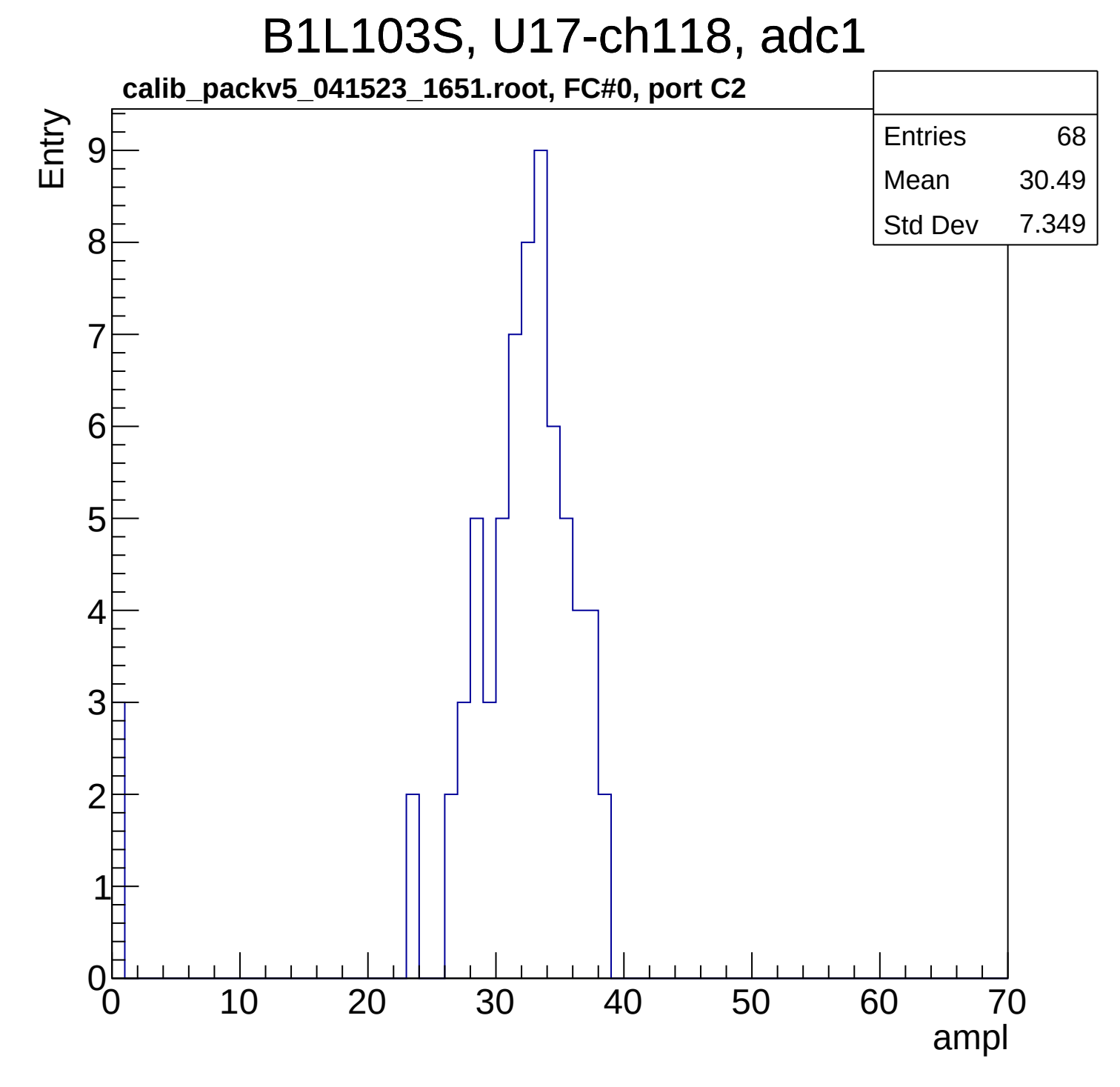
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch118, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 102
Mean 16.75
Std Dev 12.5
Entry
ampl
0
5
10
15
20
25
30
35
0
10
20
30
40
50
60
70


B1L103S, U17-ch118, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 30.49
Std Dev 7.349
Entry
ampl
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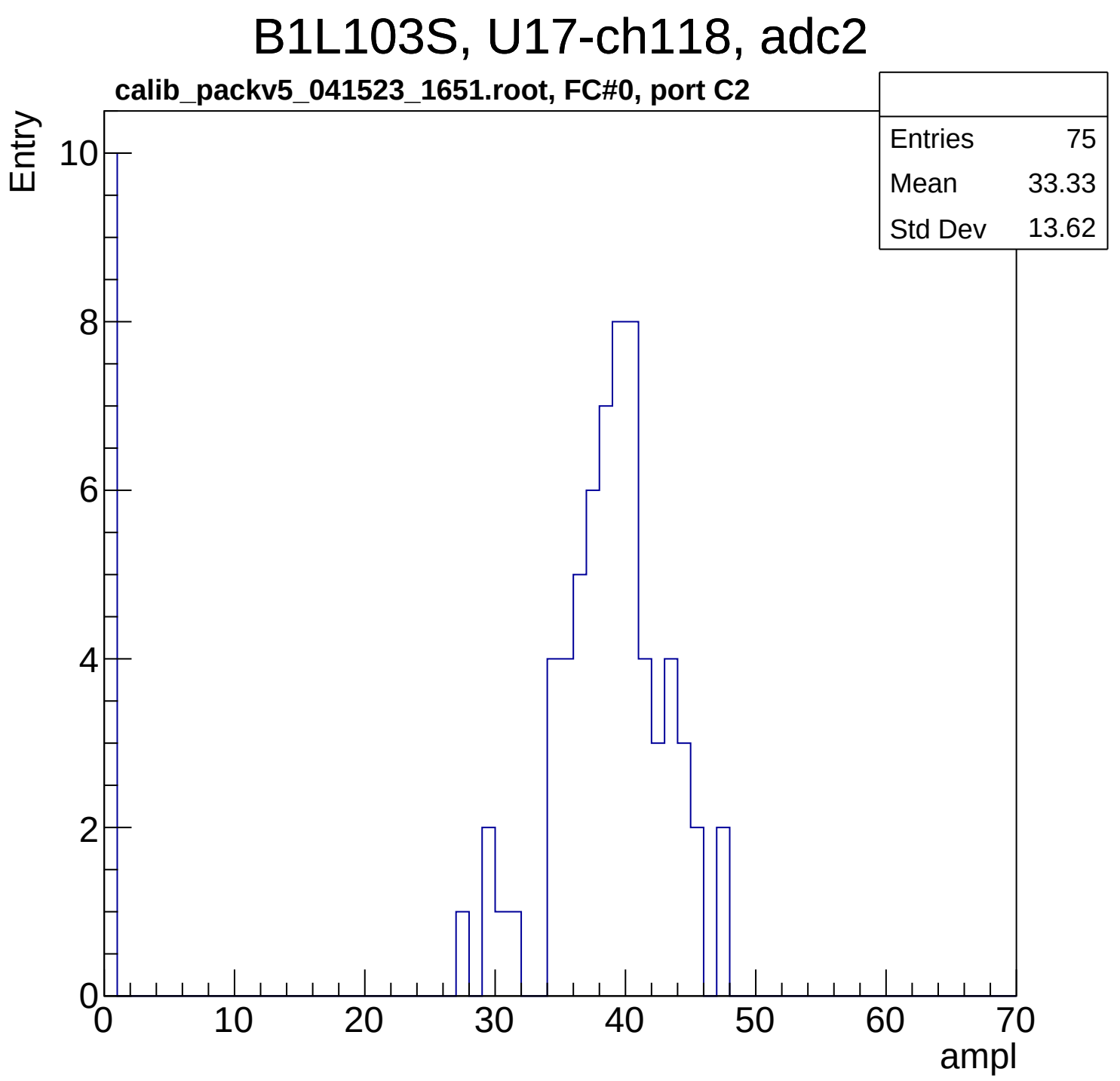
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U17-ch118, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 33.33
Std Dev 13.62
Entry
ampl
0
2
4
6
8
10
0
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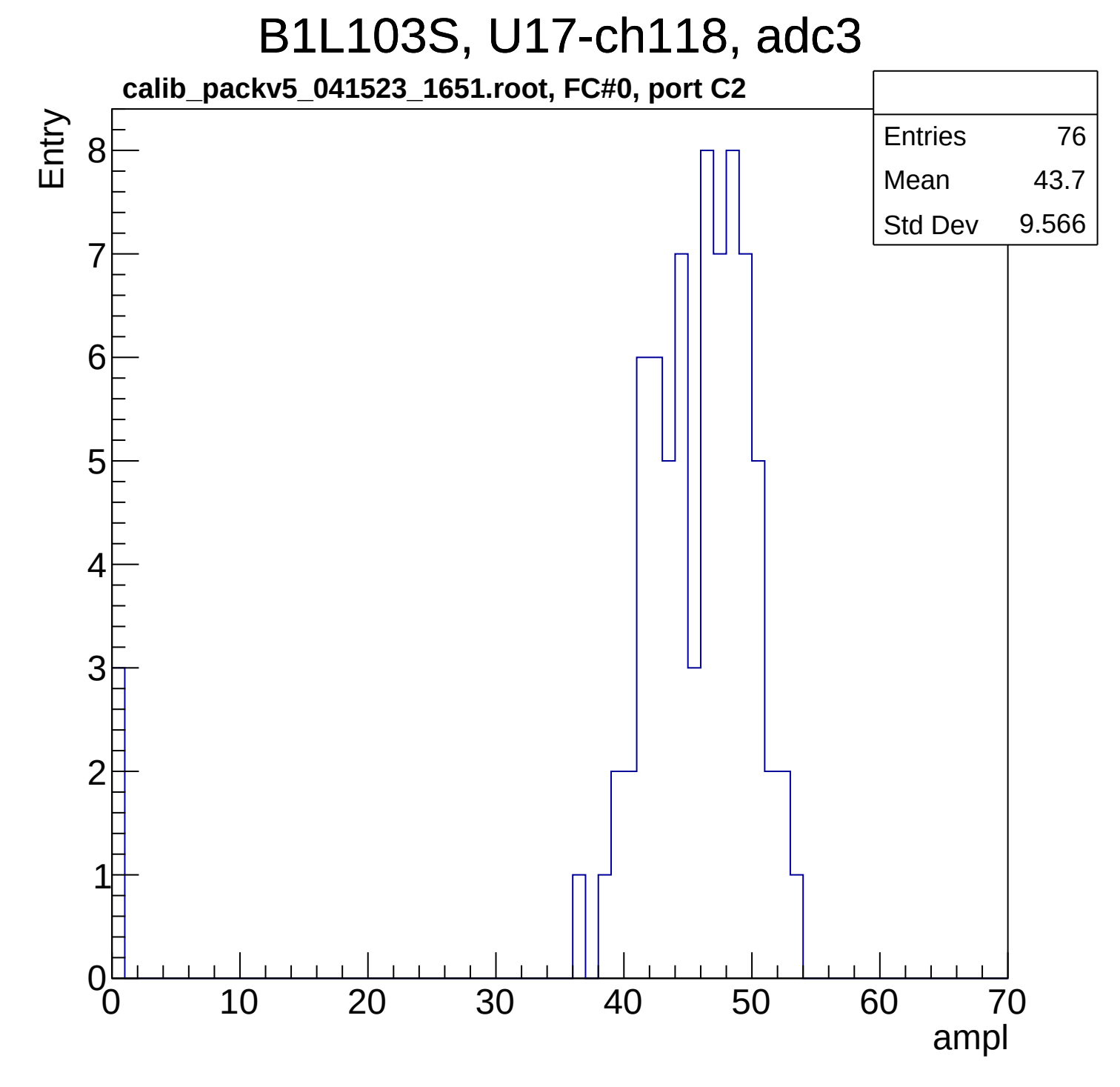
20
30
40
50
60
70


B1L103S, U17-ch118, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 43.7
Std Dev 9.566
Entry
ampl
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1
2
3
4
5
6
7
8
0
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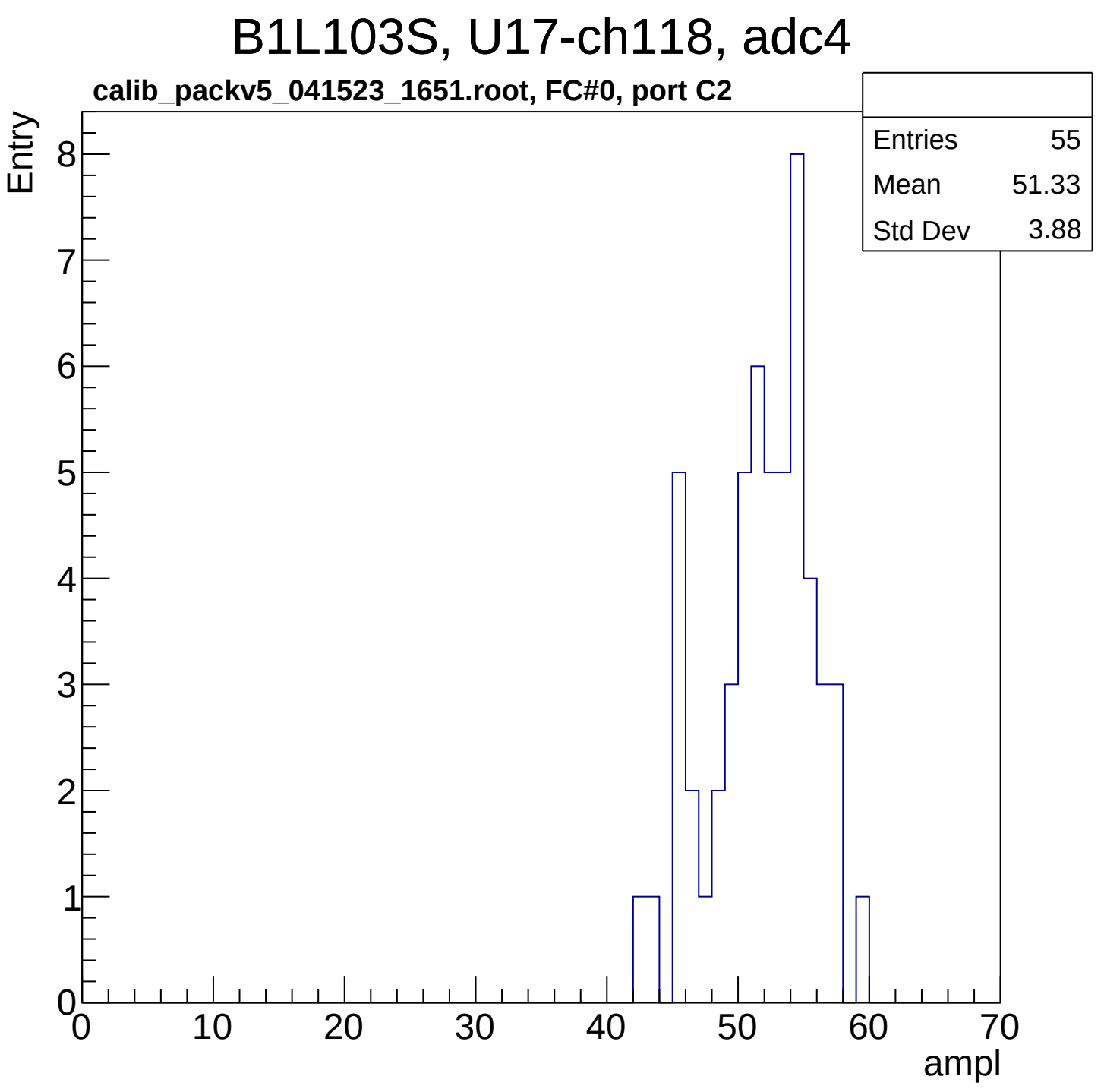
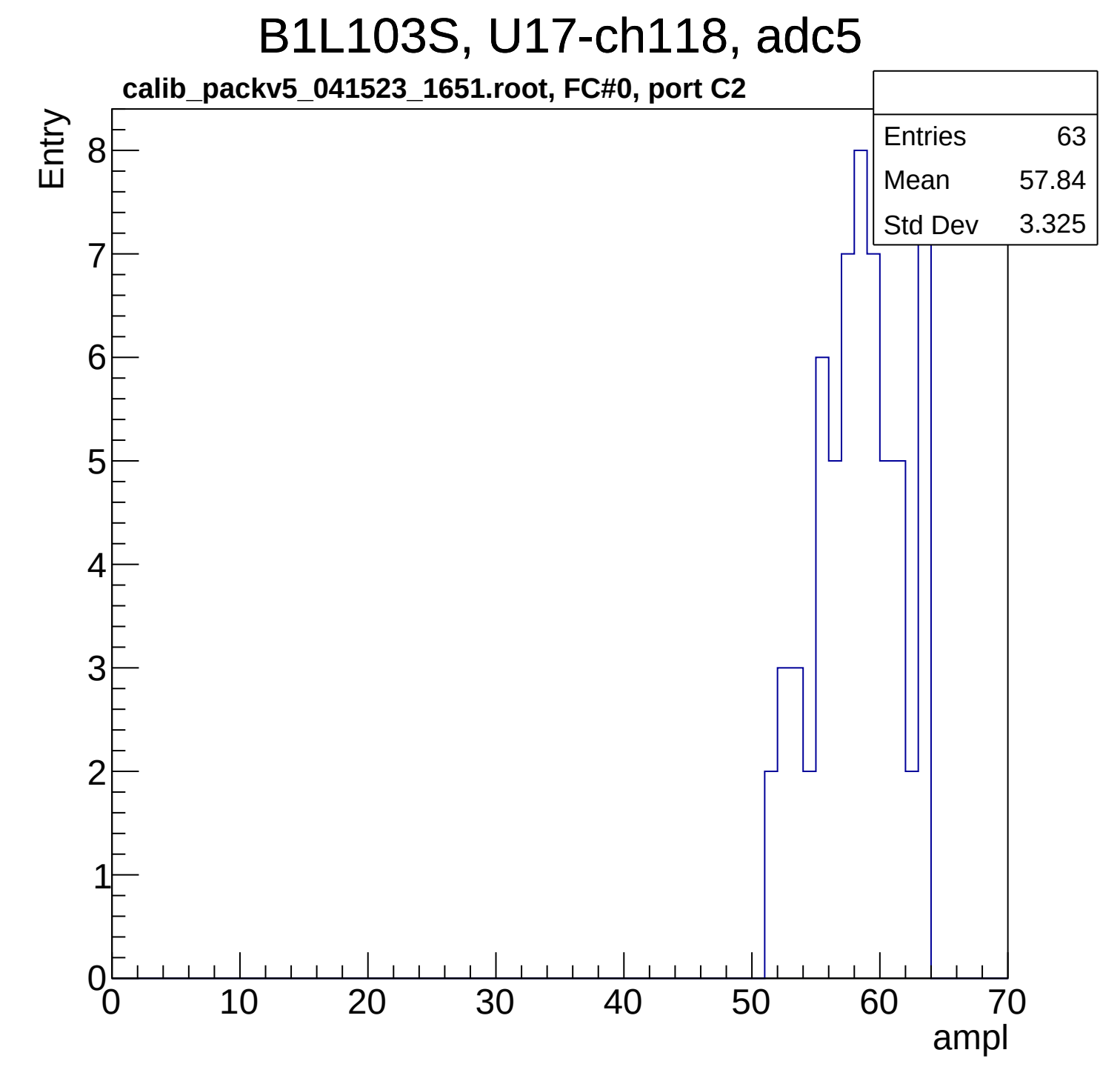
20
30
40
50
60
70


B1L103S, U17-ch118, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 51.33
Std Dev 3.88
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U17-ch118, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 57.84
Std Dev 3.325
Entry
ampl
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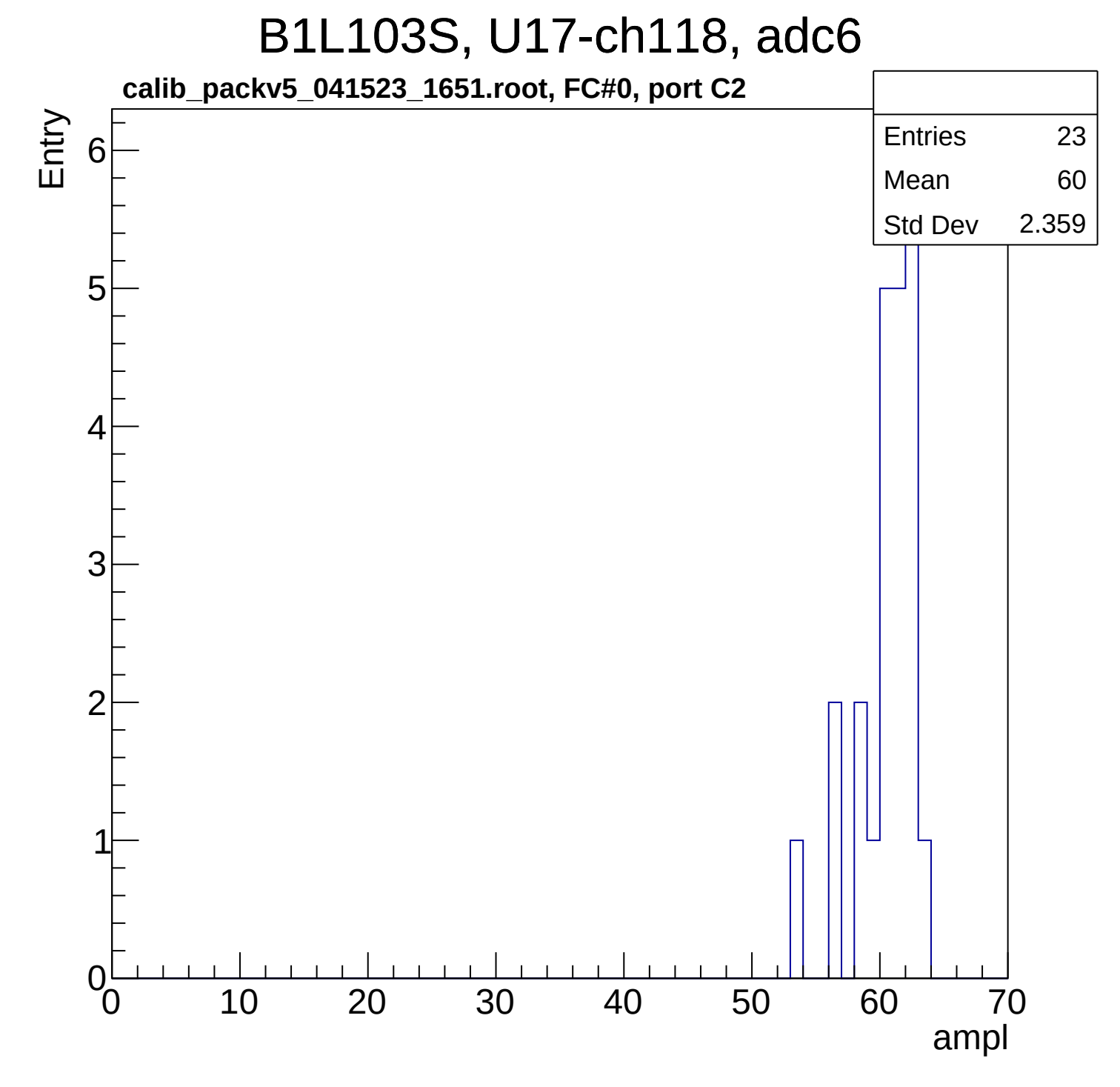
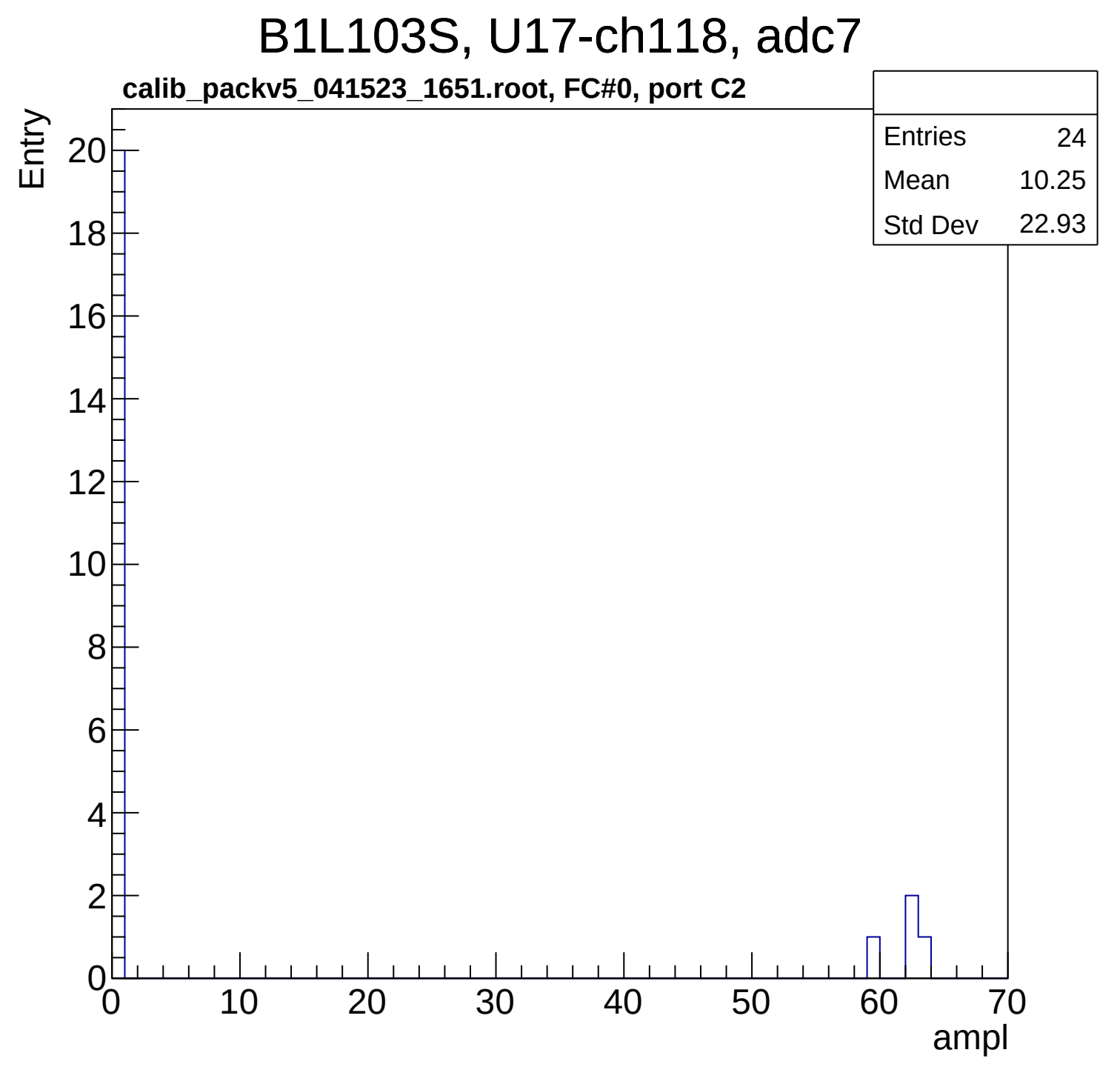
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U17-ch118, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 23
Mean 60
Std Dev 2.359
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U17-ch118, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 24
Mean 10.25
Std Dev 22.93
Entry
ampl
0
2
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6
8
10
12
14
16
18
20
0
10
20
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40
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60
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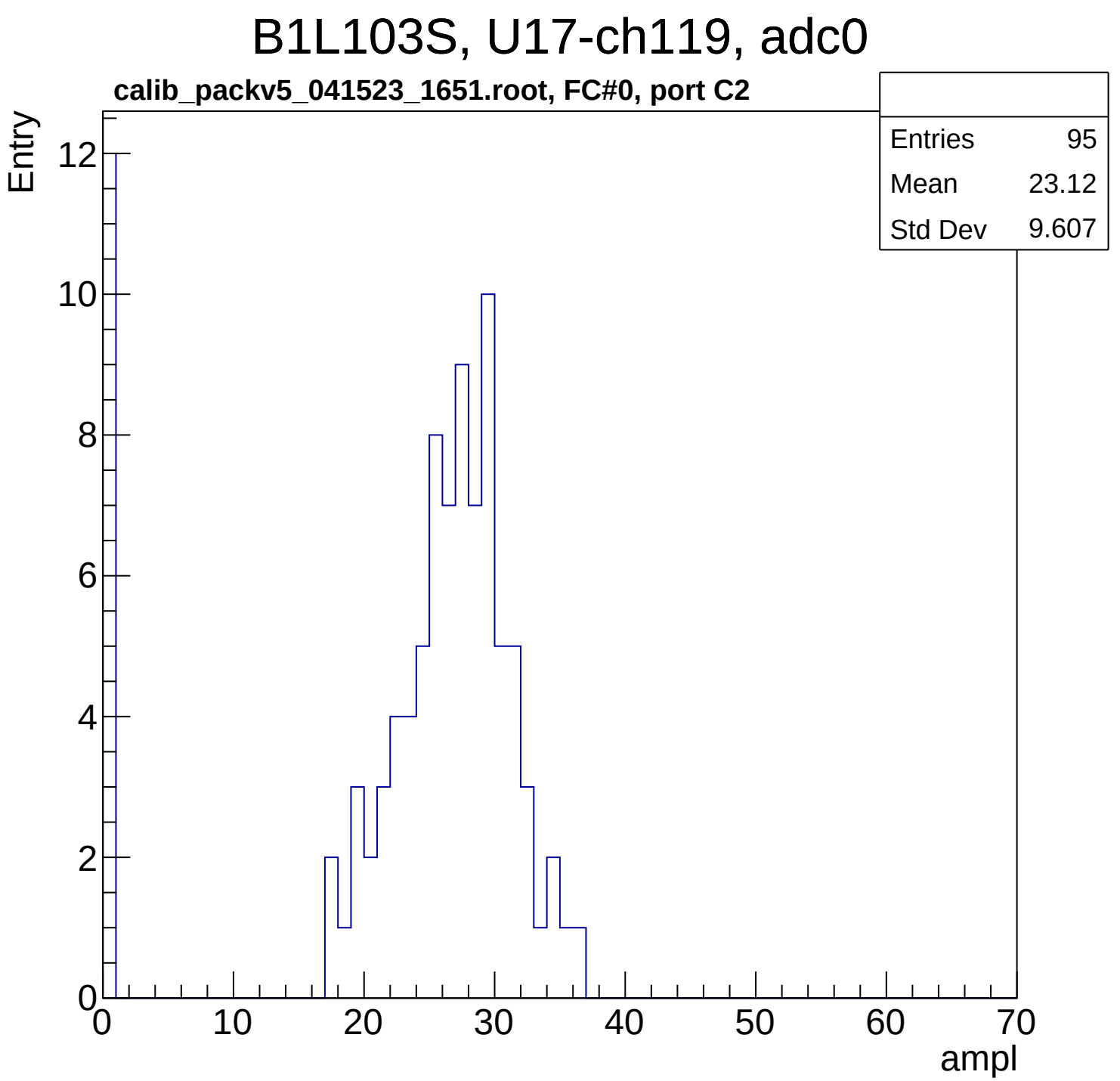
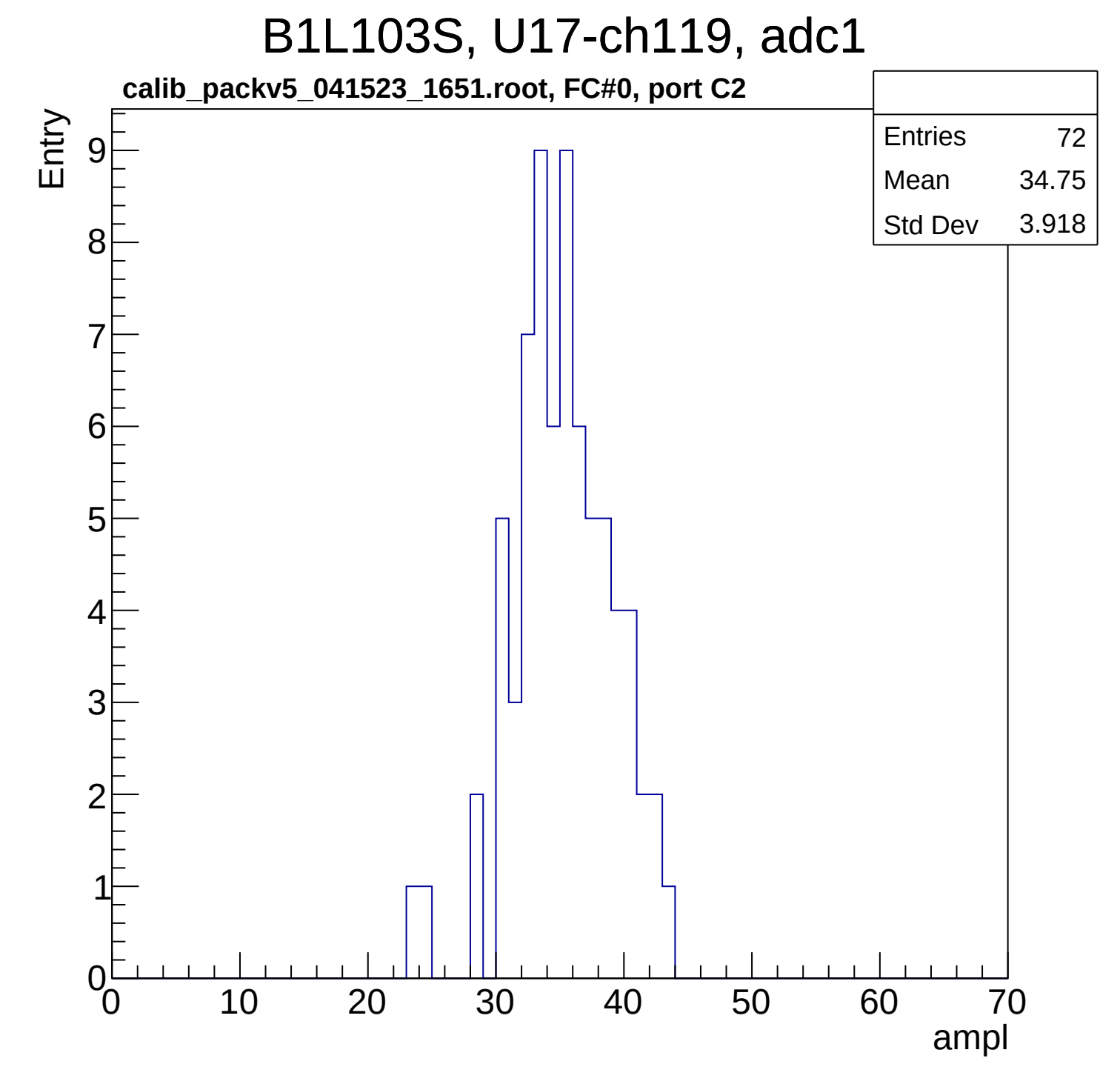
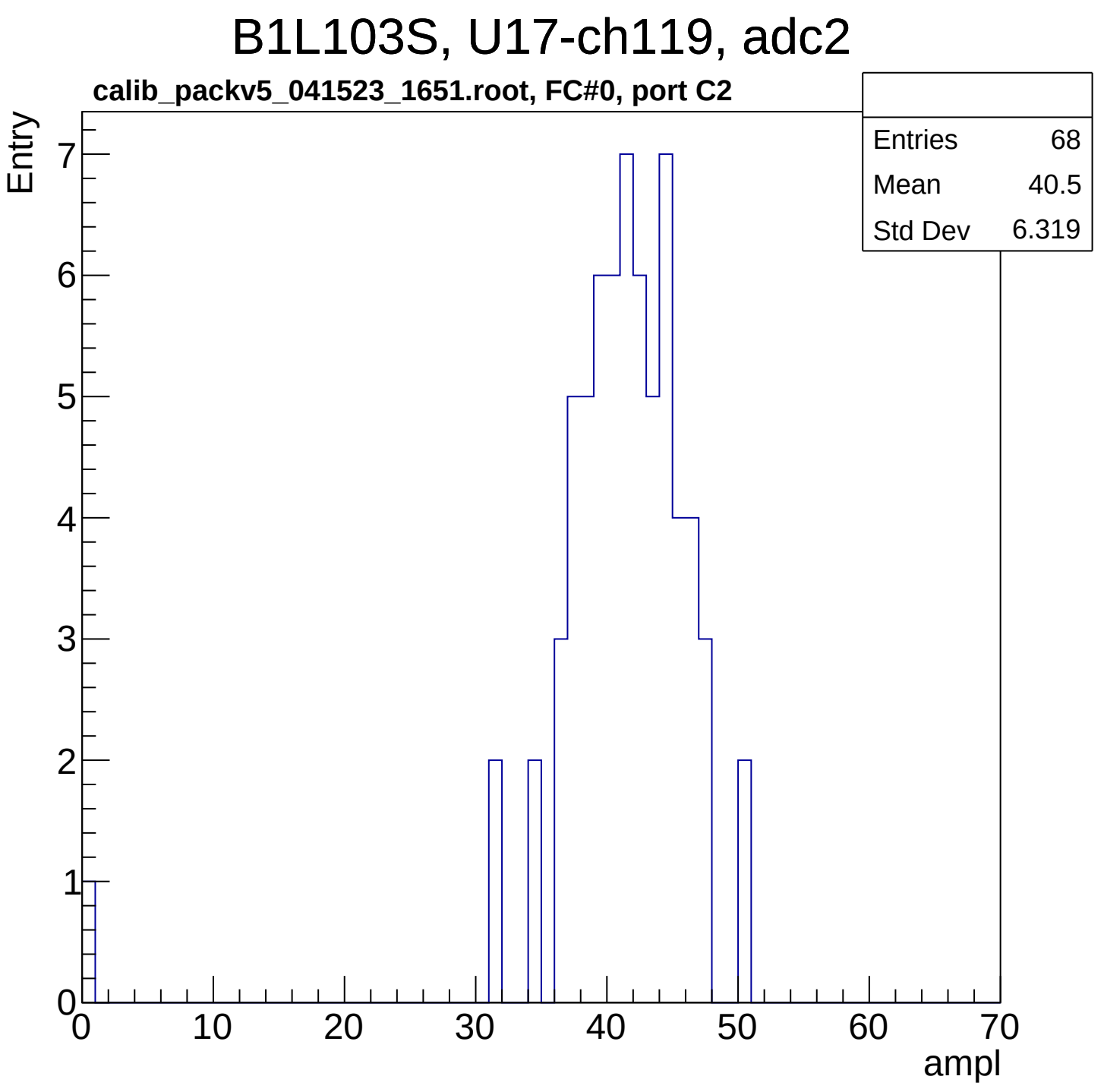

B1L103S, U17-ch119, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 95
Mean 23.12
Std Dev 9.607
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch119, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 34.75
Std Dev 3.918
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U17-ch119, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 40.5
Std Dev 6.319
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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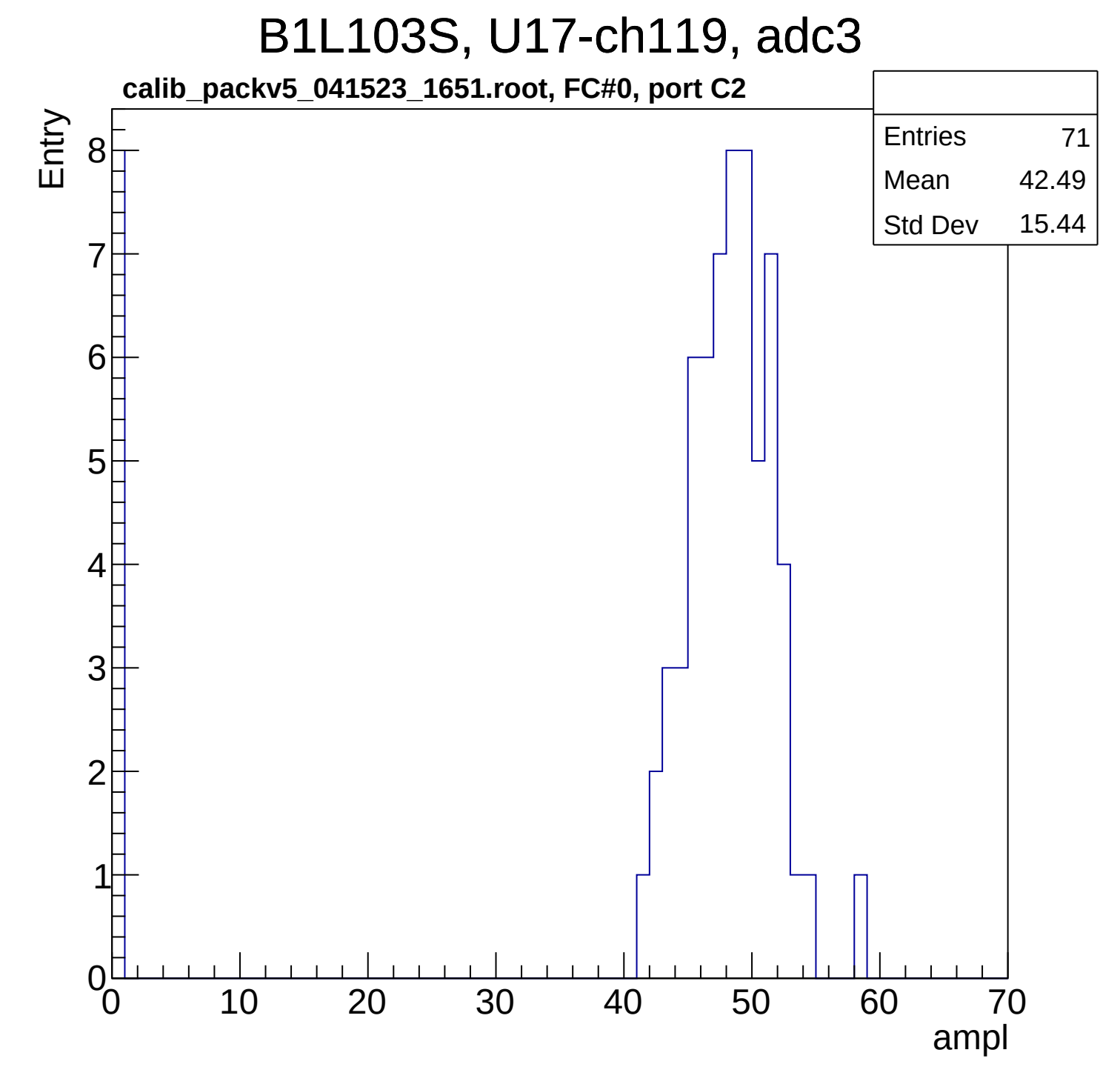
B1L103S, U17-ch119, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 42.49
Std Dev 15.44
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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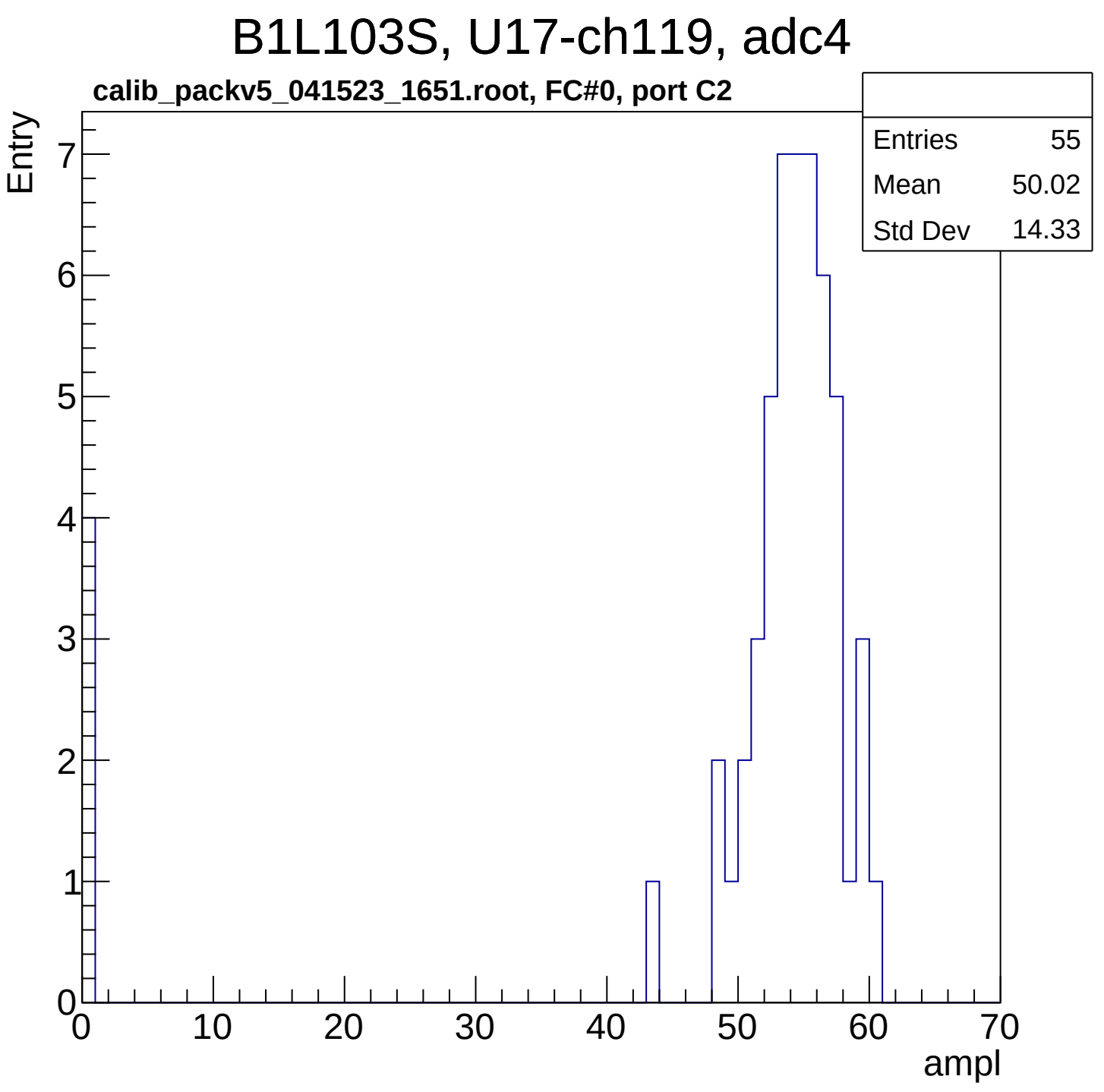
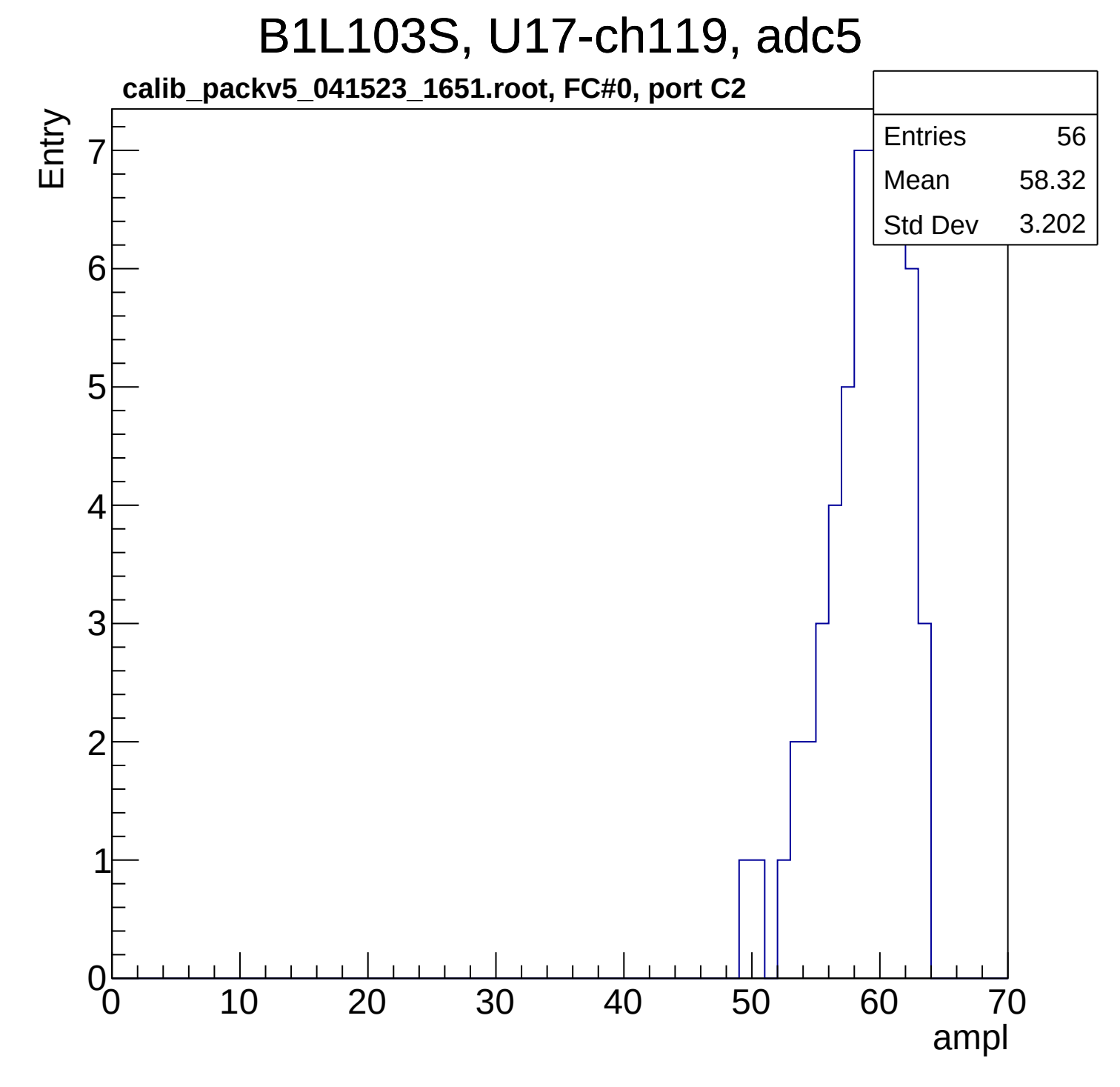
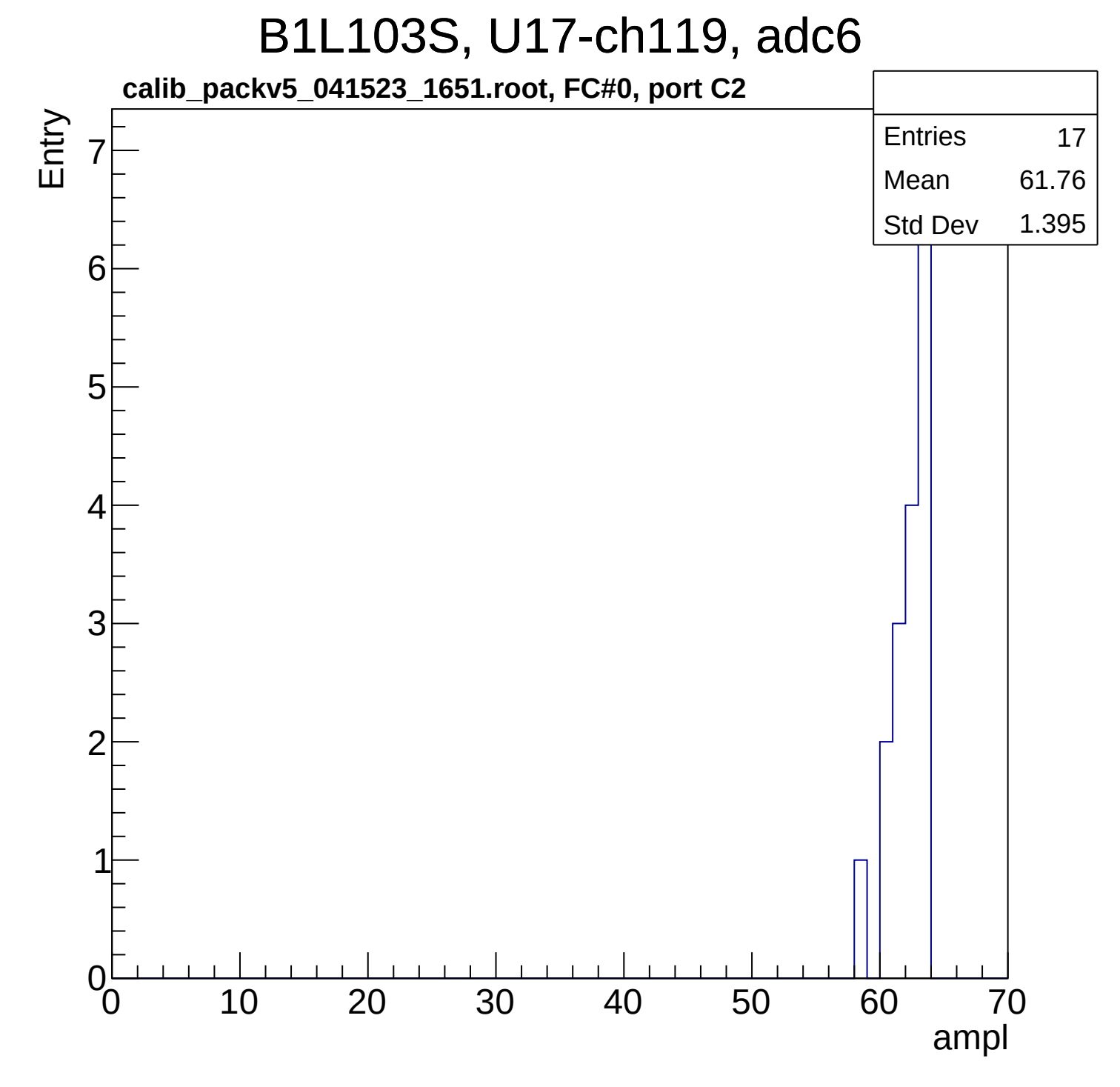
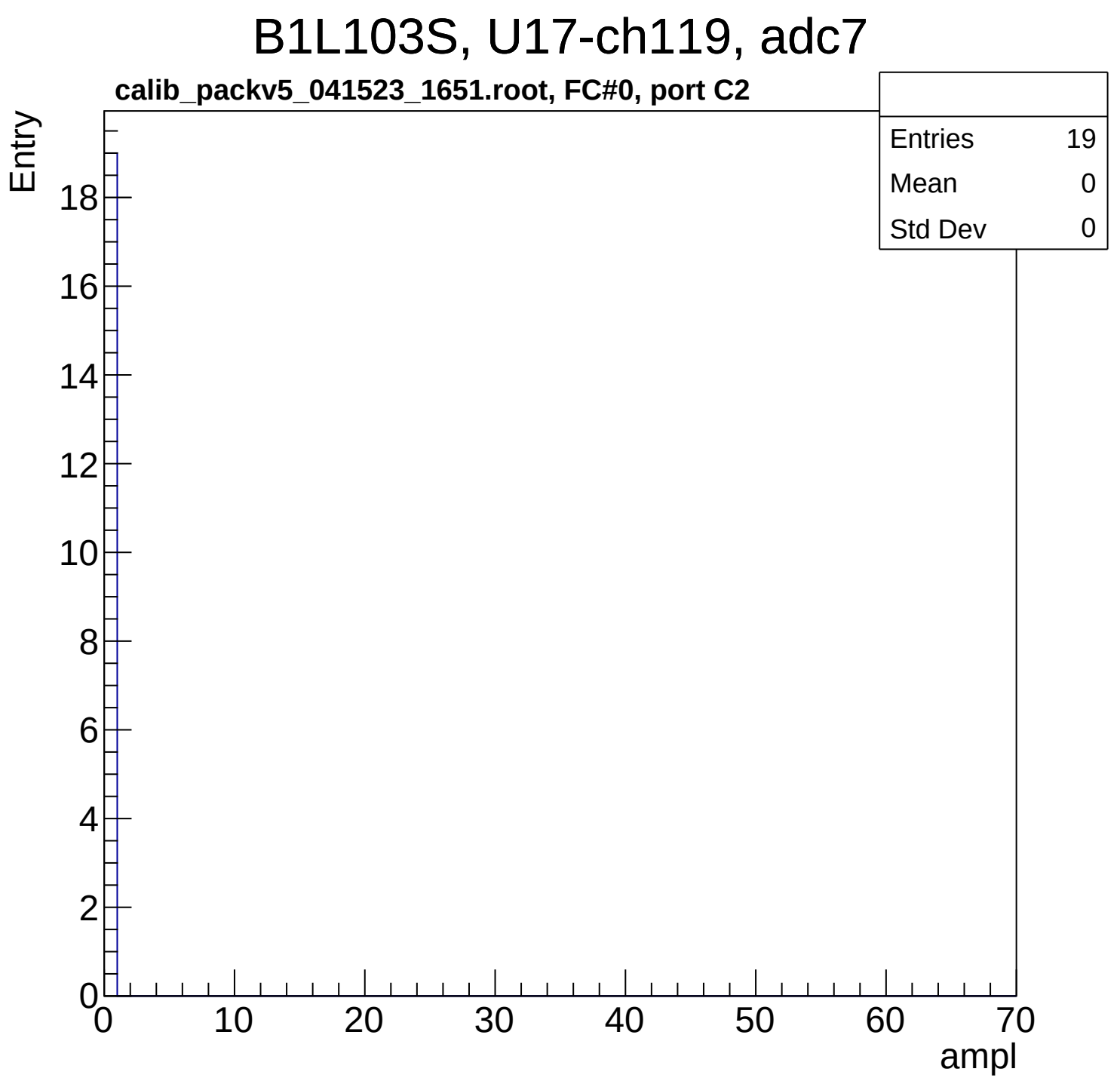
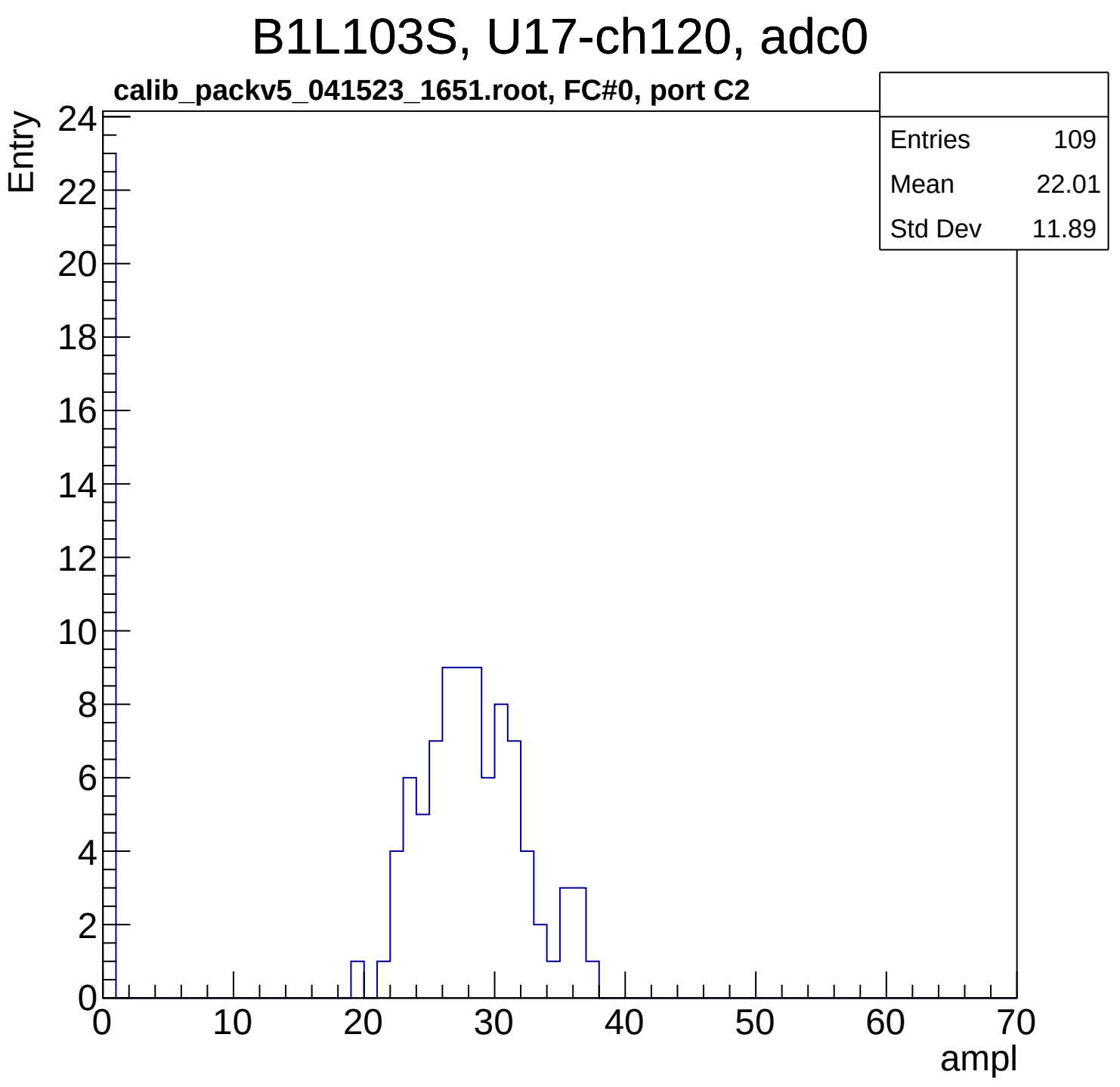
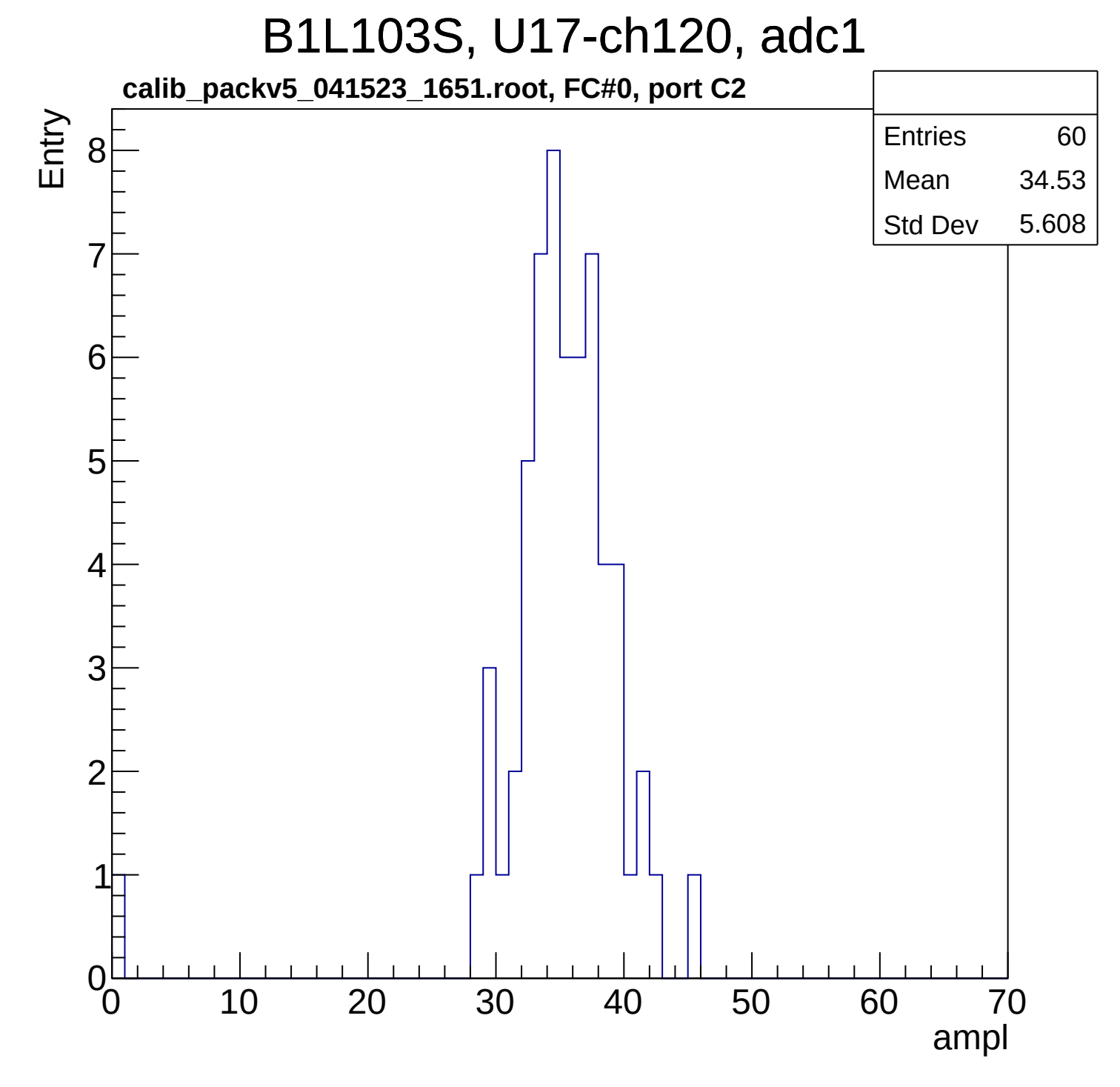

B1L103S, U17-ch119, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 50.02
Std Dev 14.33
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

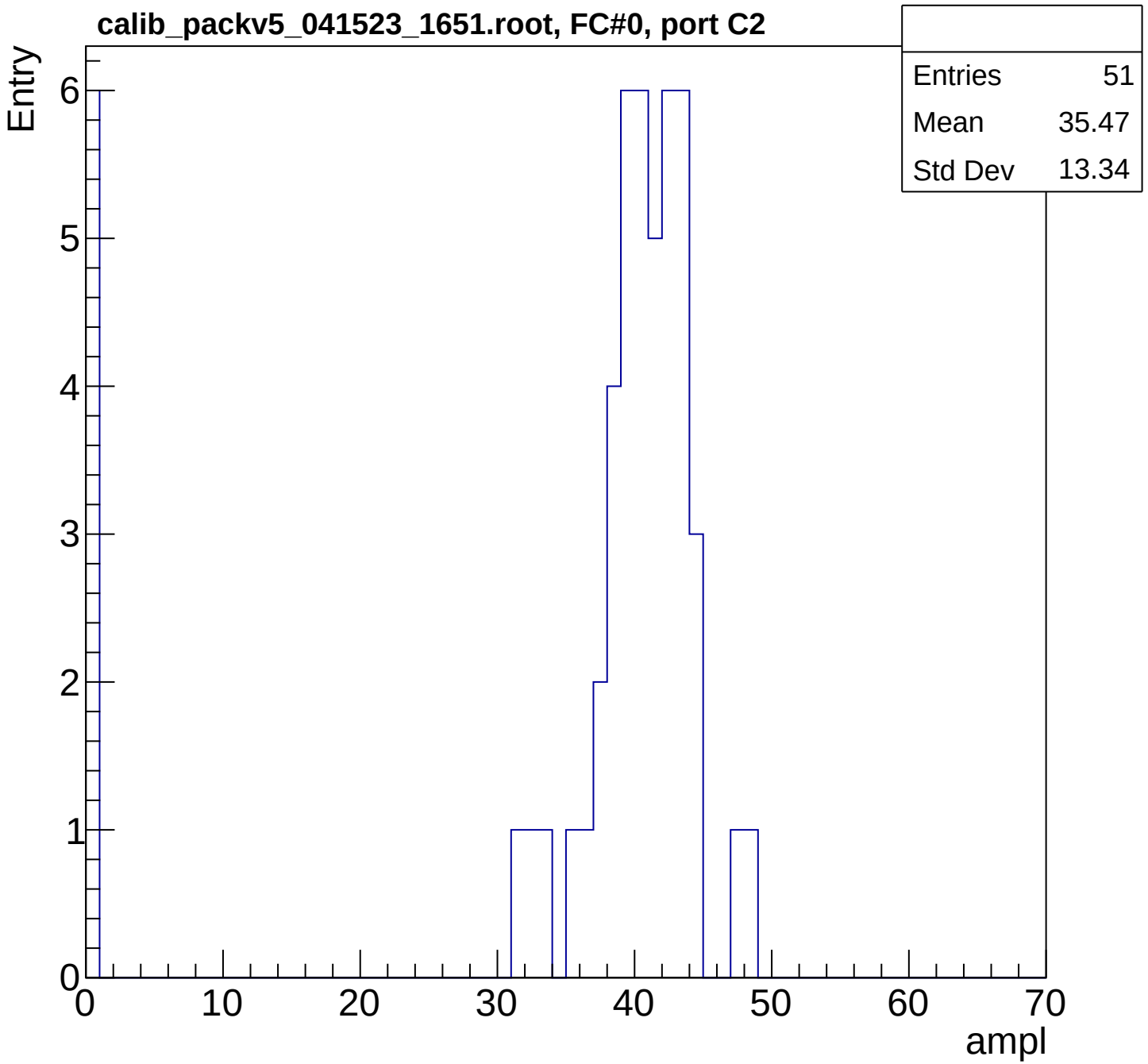

B1L103S, U17-ch119, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 58.32
Std Dev 3.202
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

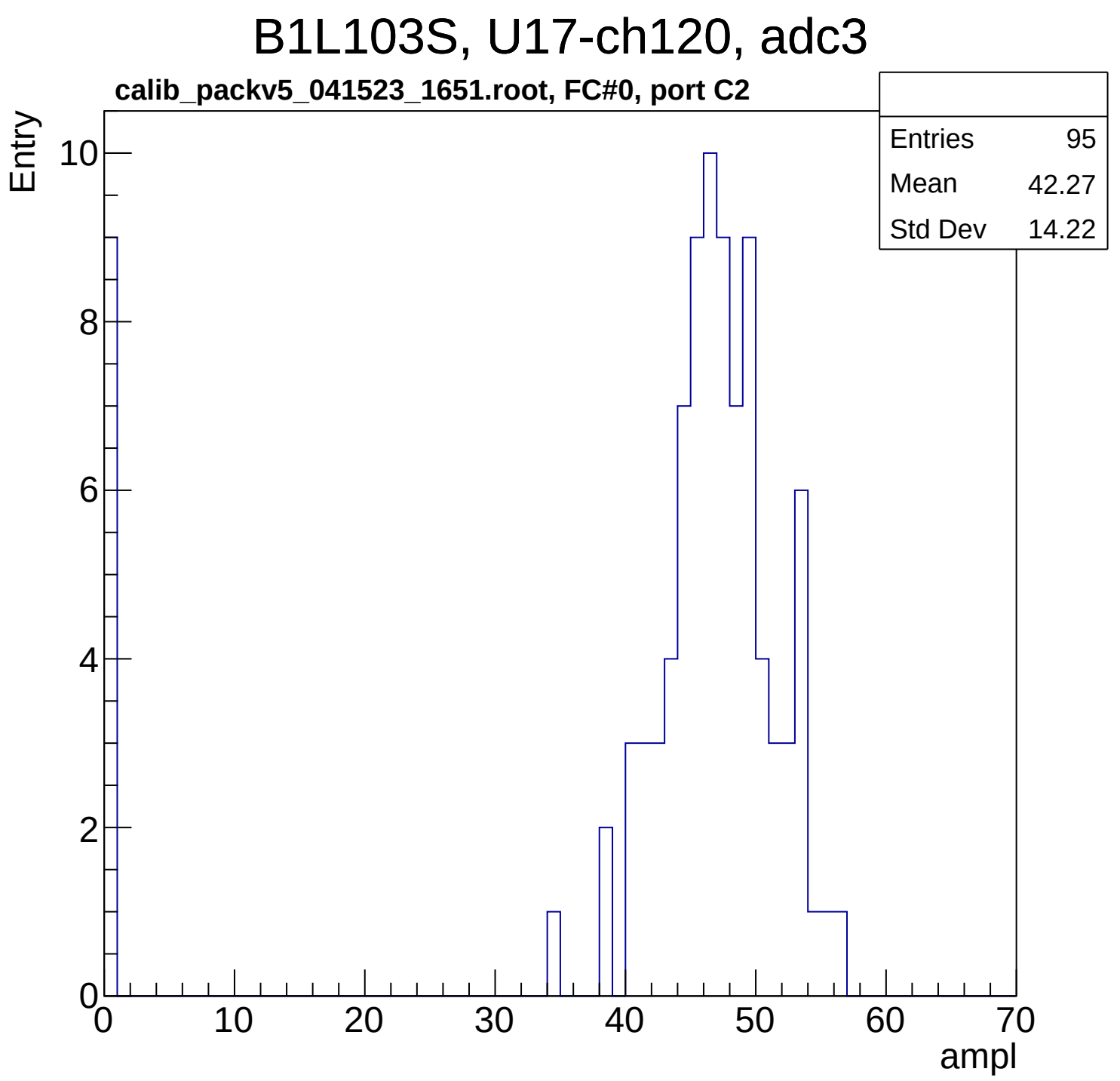

B1L103S, U17-ch119, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 17
Mean 61.76
Std Dev 1.395
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

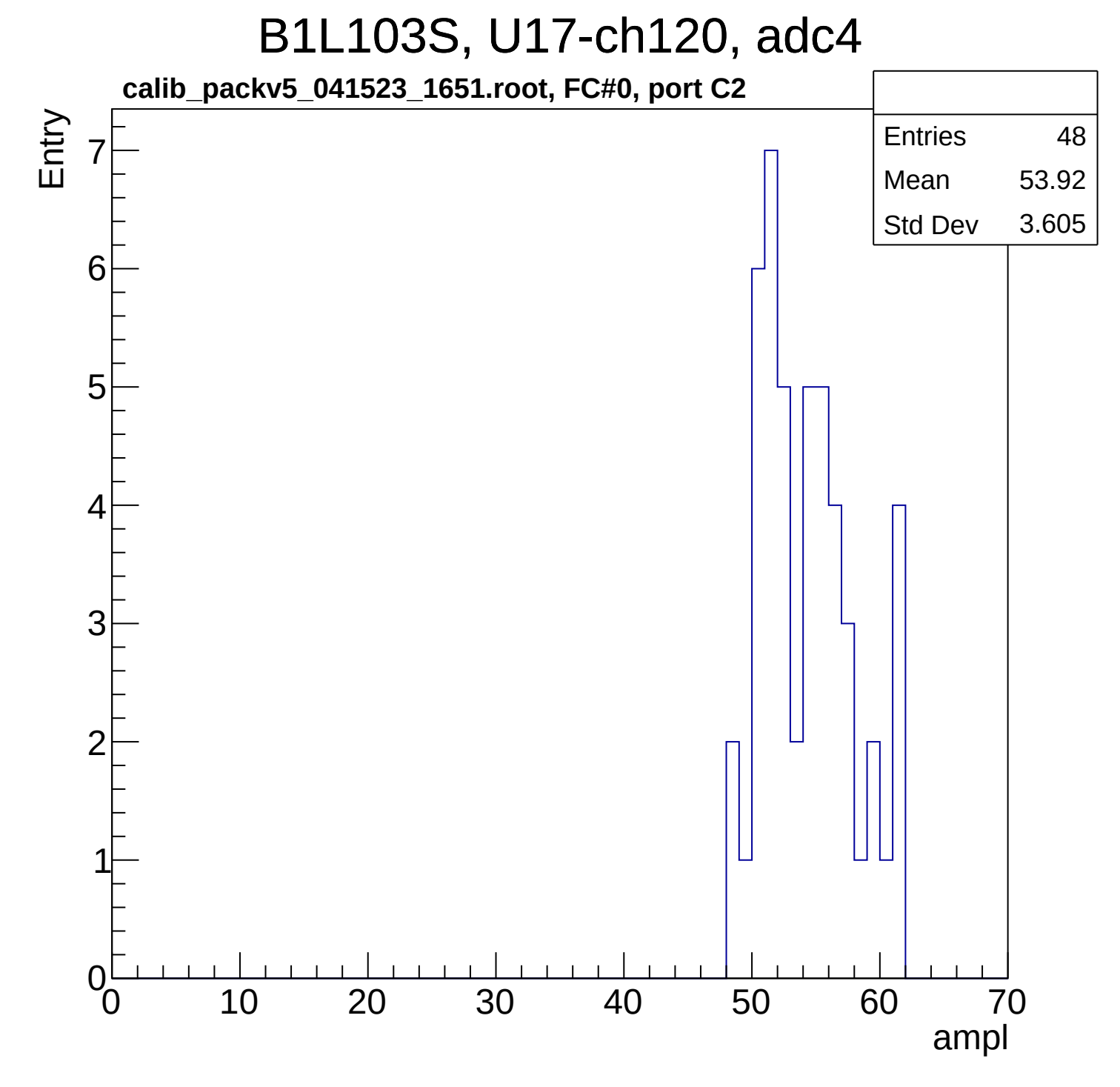

B1L103S, U17-ch119, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

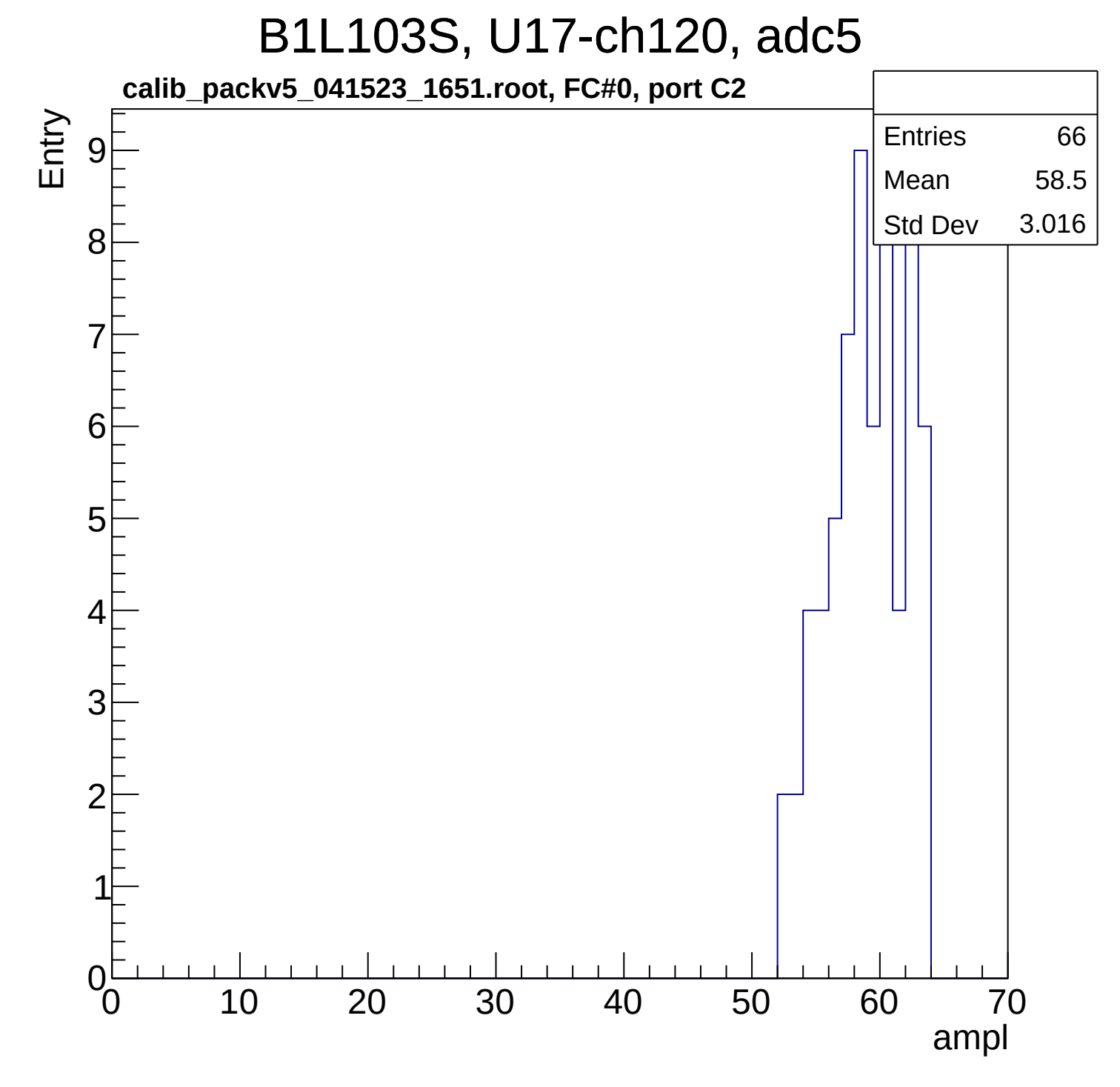

B1L103S, U17-ch120, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 109
Mean 22.01
Std Dev 11.89
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
22
24
0
10
20
30
40
50
60
70

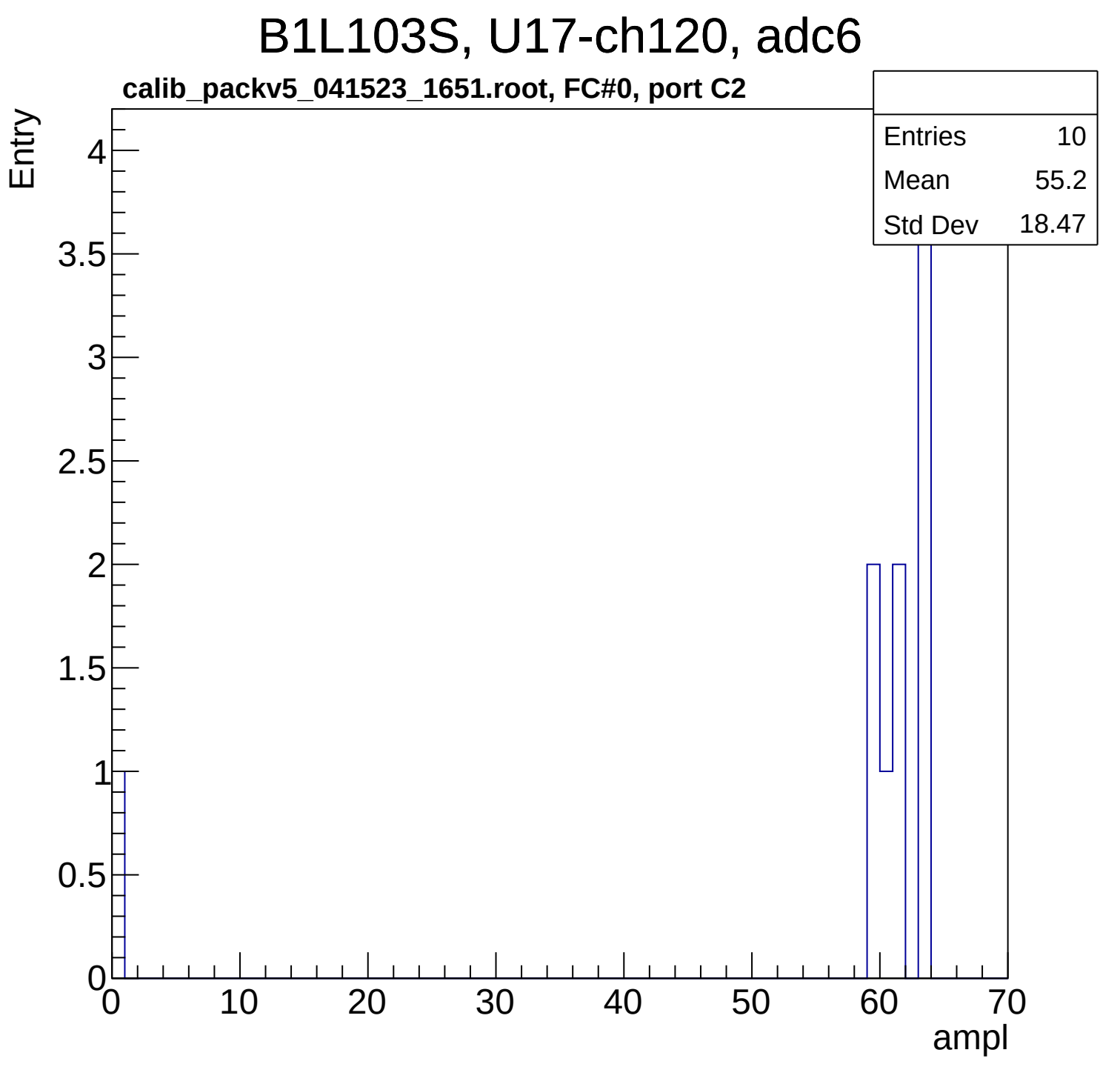

B1L103S, U17-ch120, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 34.53
Std Dev 5.608
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

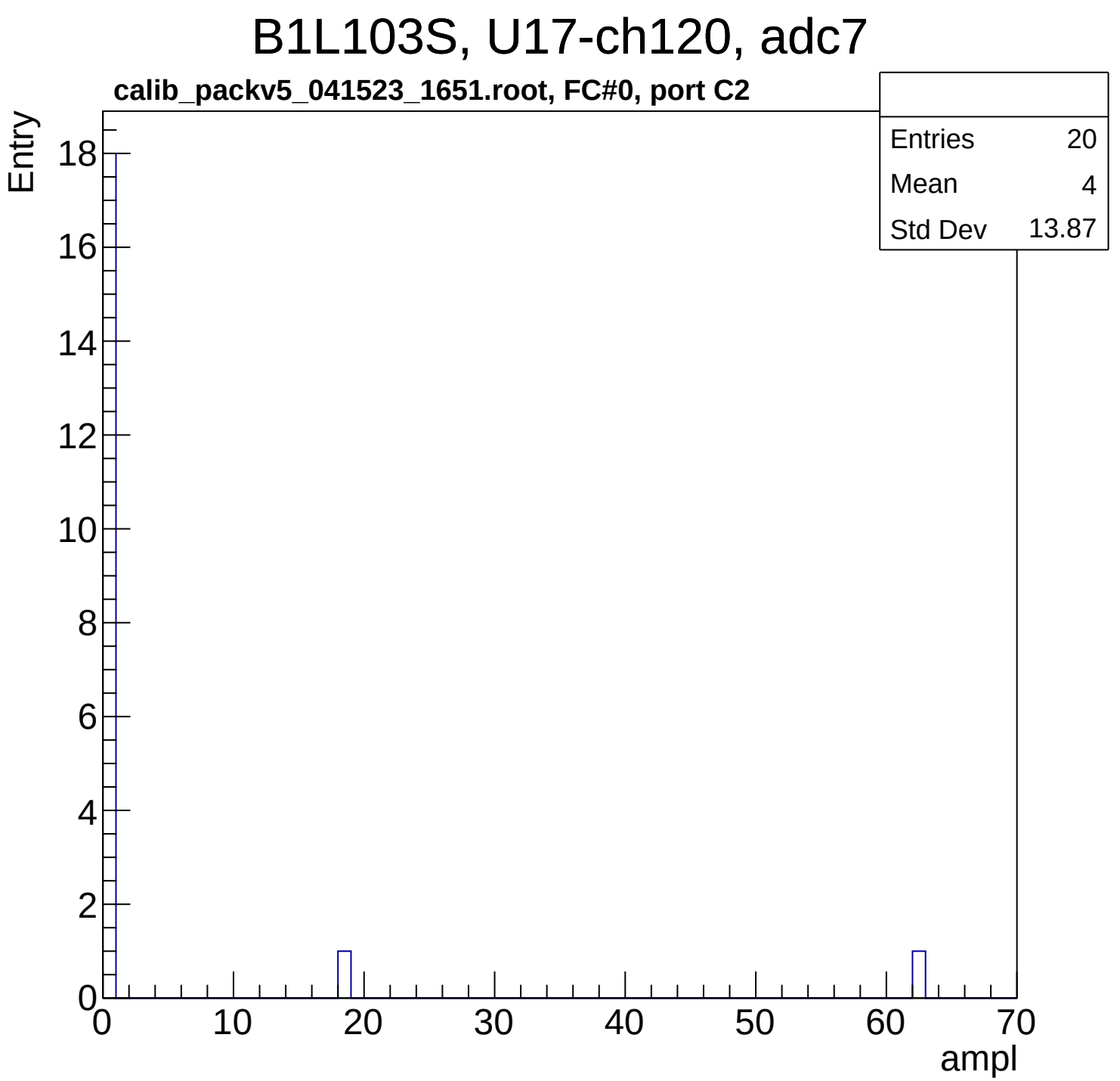

B1L103S, U17-ch120, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 35.47
Std Dev 13.34
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

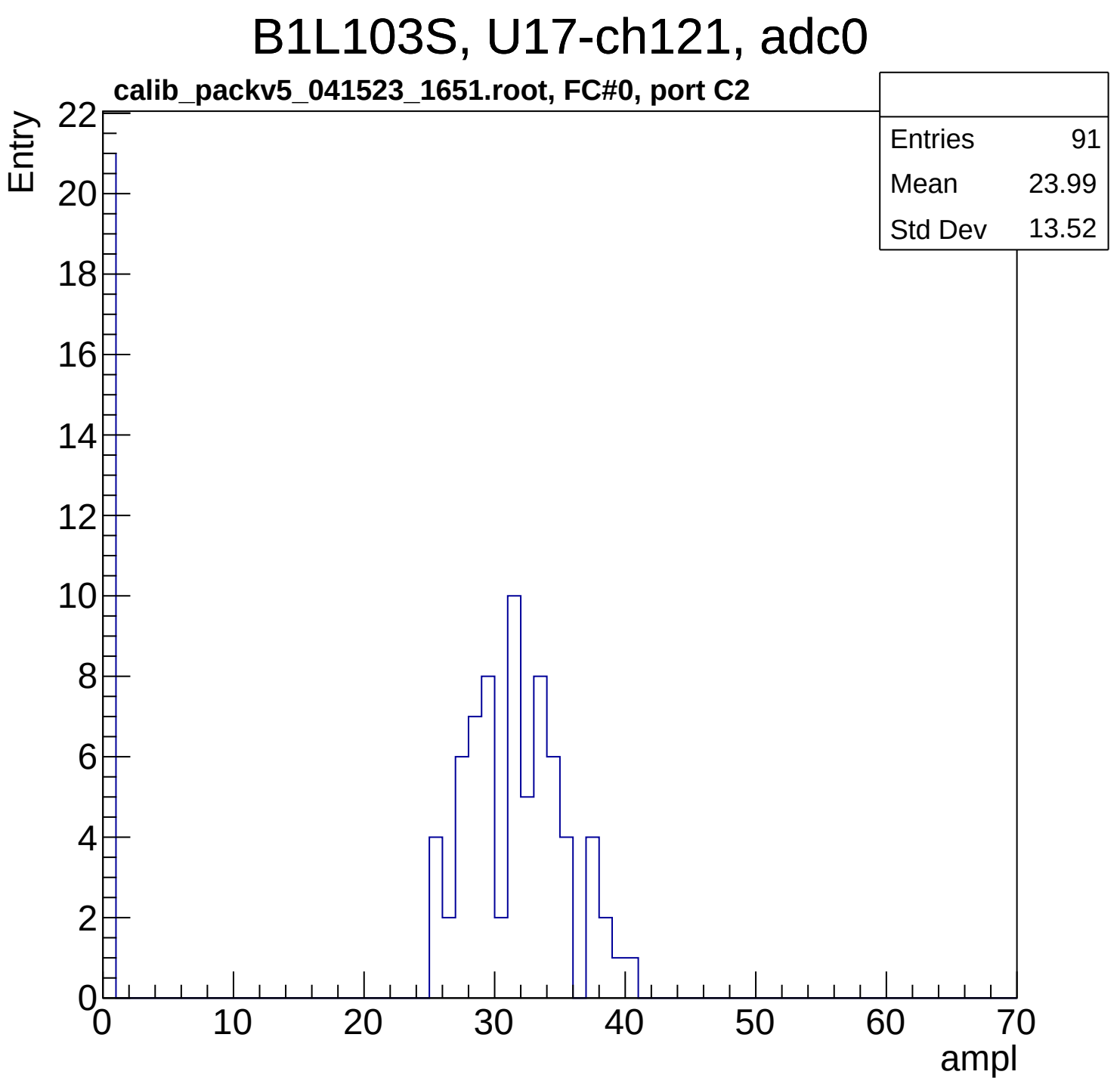

B1L103S, U17-ch120, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 95
Mean 42.27
Std Dev 14.22
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

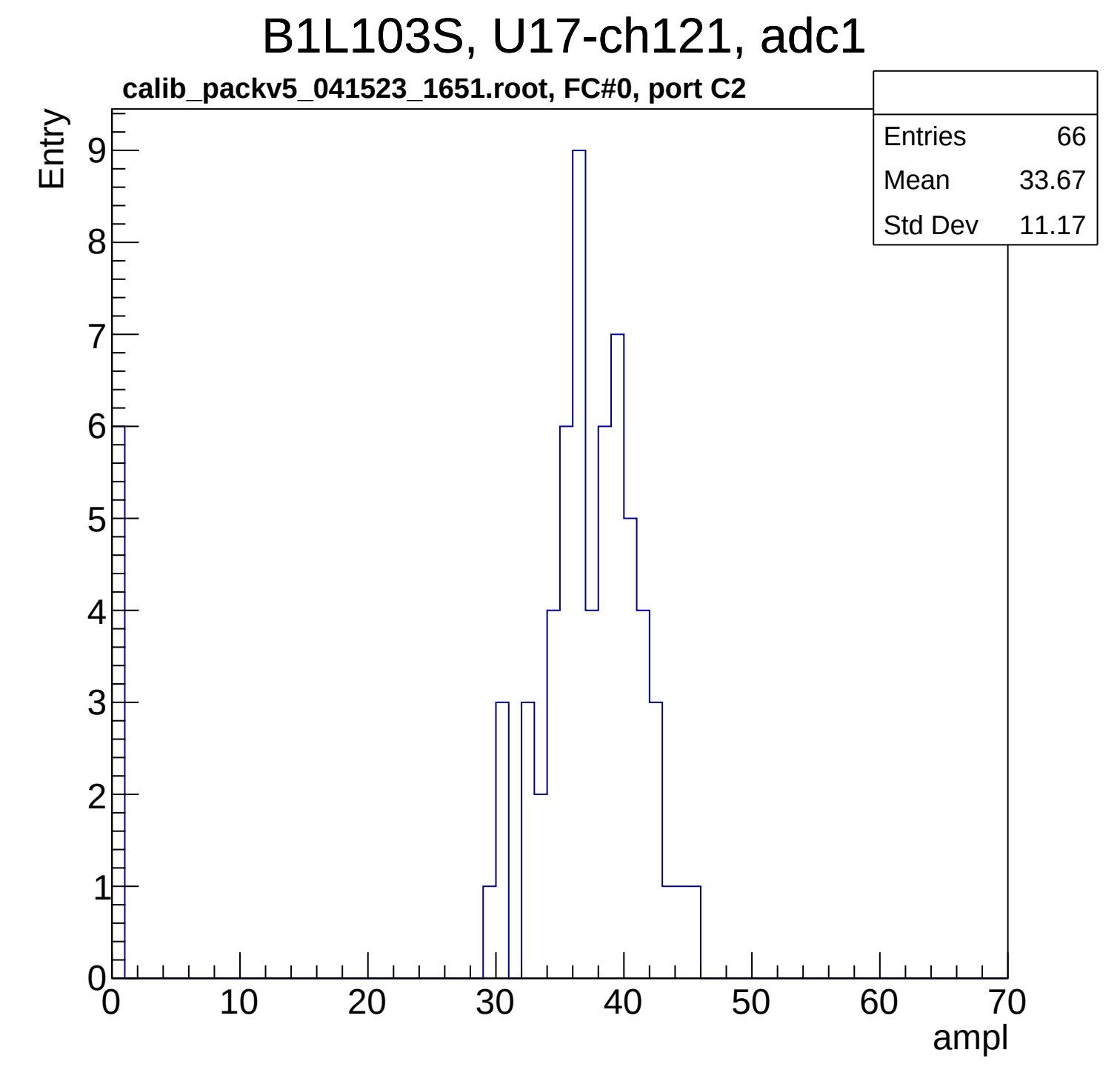

B1L103S, U17-ch120, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 53.92
Std Dev 3.605
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U17-ch120, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 58.5
Std Dev 3.016
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U17-ch120, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 55.2
Std Dev 18.47
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U17-ch120, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 4
Std Dev 13.87
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch121, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 91
Mean 23.99
Std Dev 13.52
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
22
0
10
20
30
40
50
60
70


B1L103S, U17-ch121, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 33.67
Std Dev 11.17
Entry
ampl
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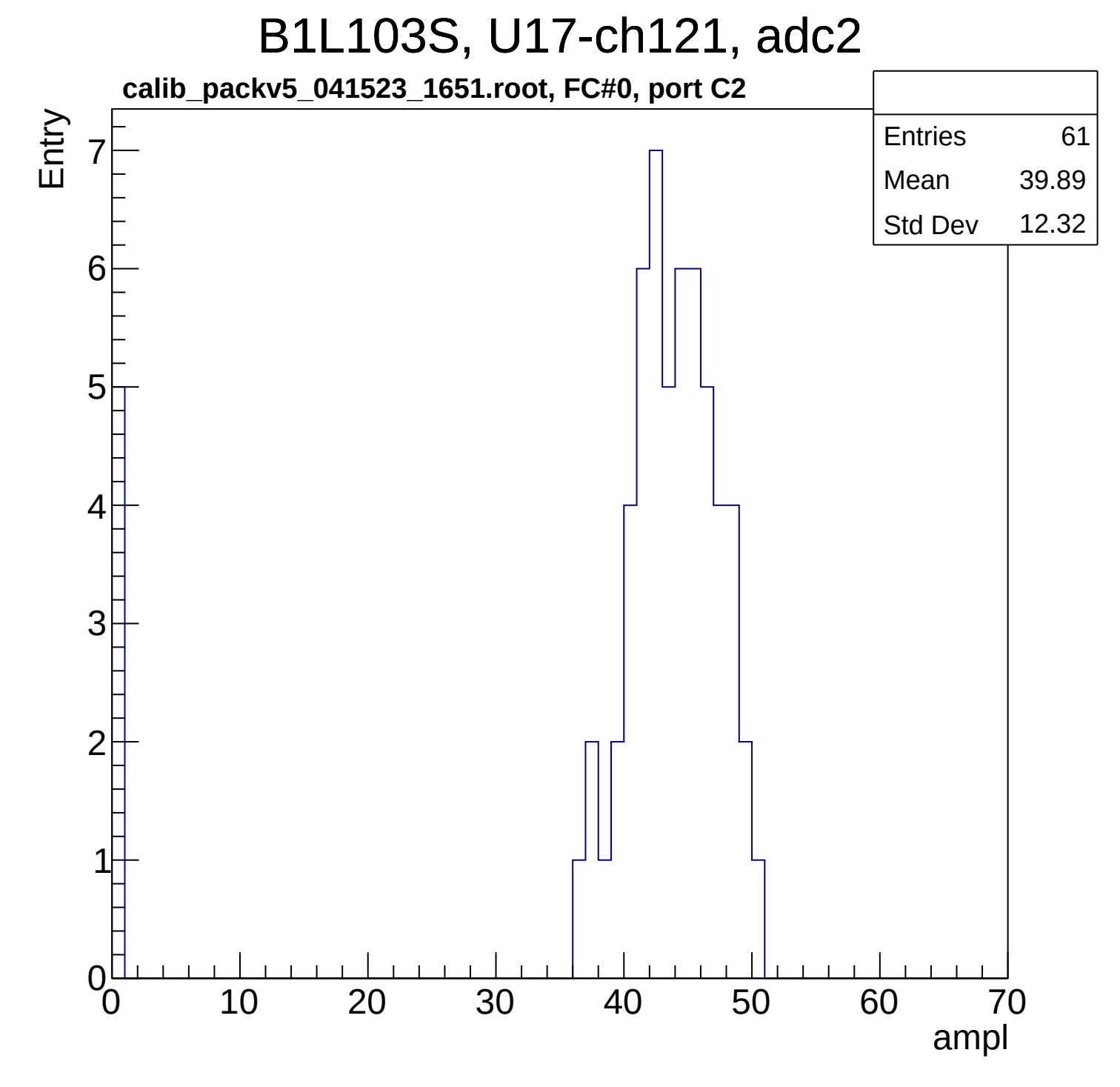
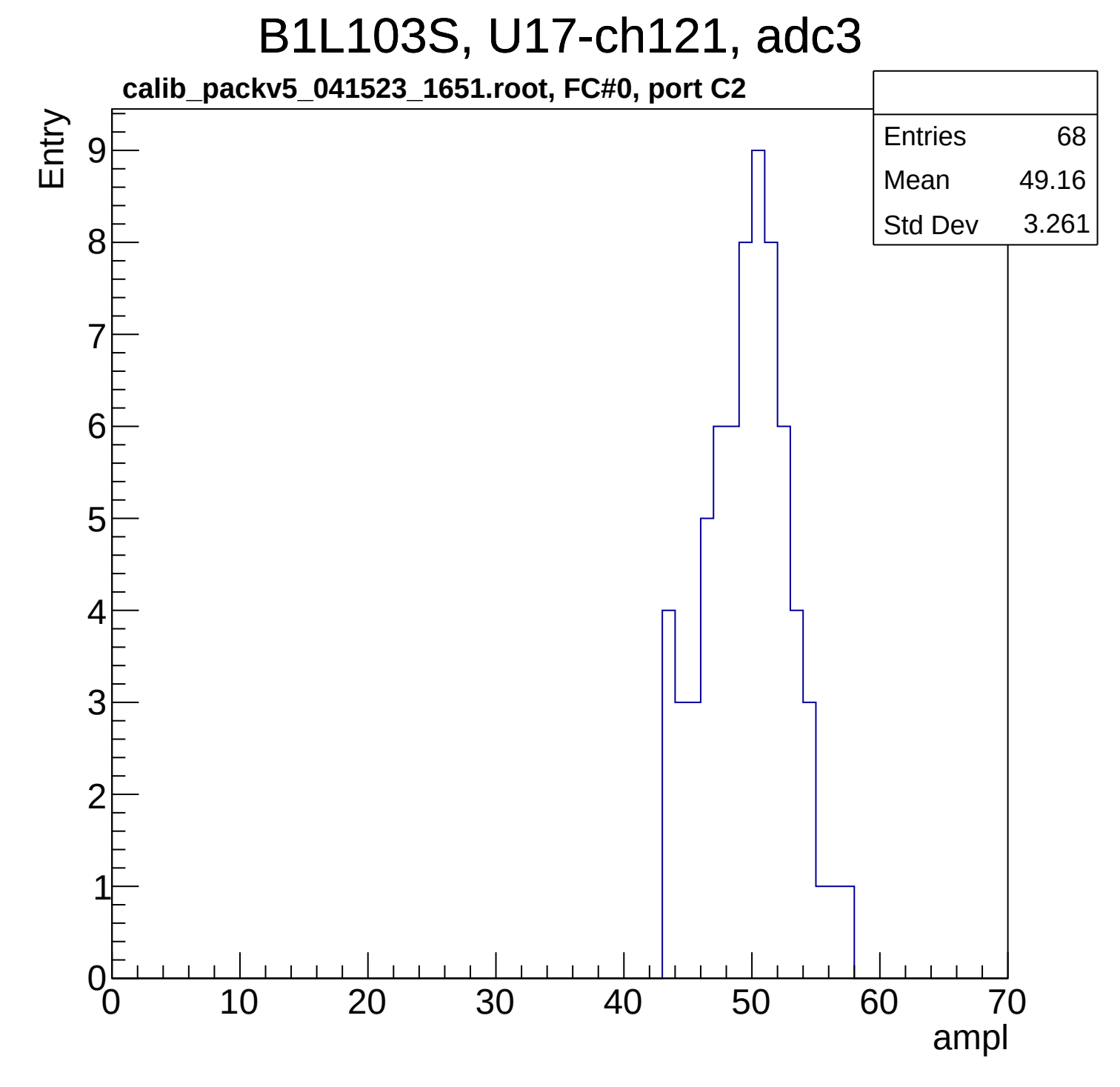
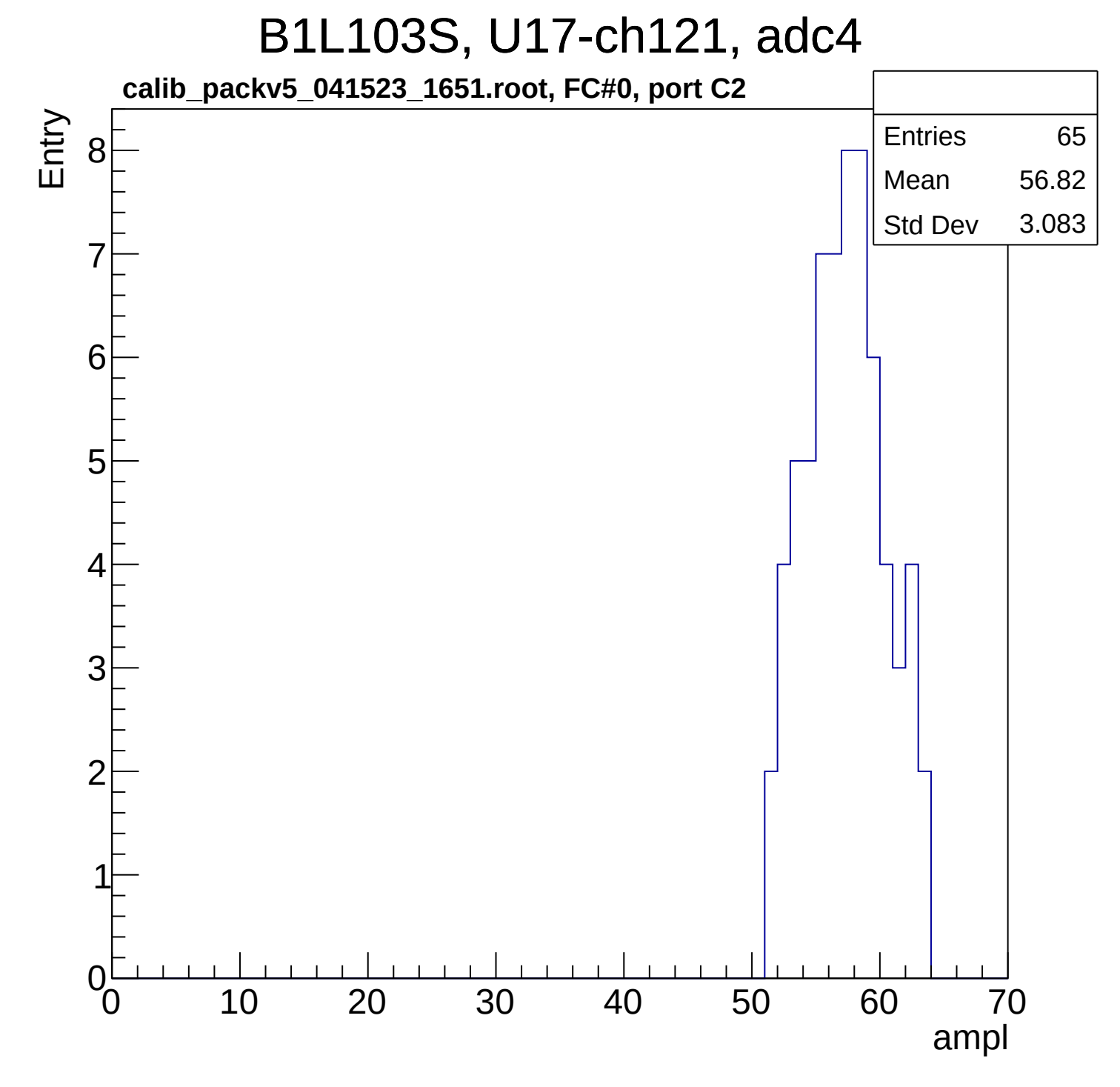
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9


B1L103S, U17-ch121, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 39.89
Std Dev 12.32
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U17-ch121, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 49.16
Std Dev 3.261
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U17-ch121, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 56.82
Std Dev 3.083
Entry
ampl
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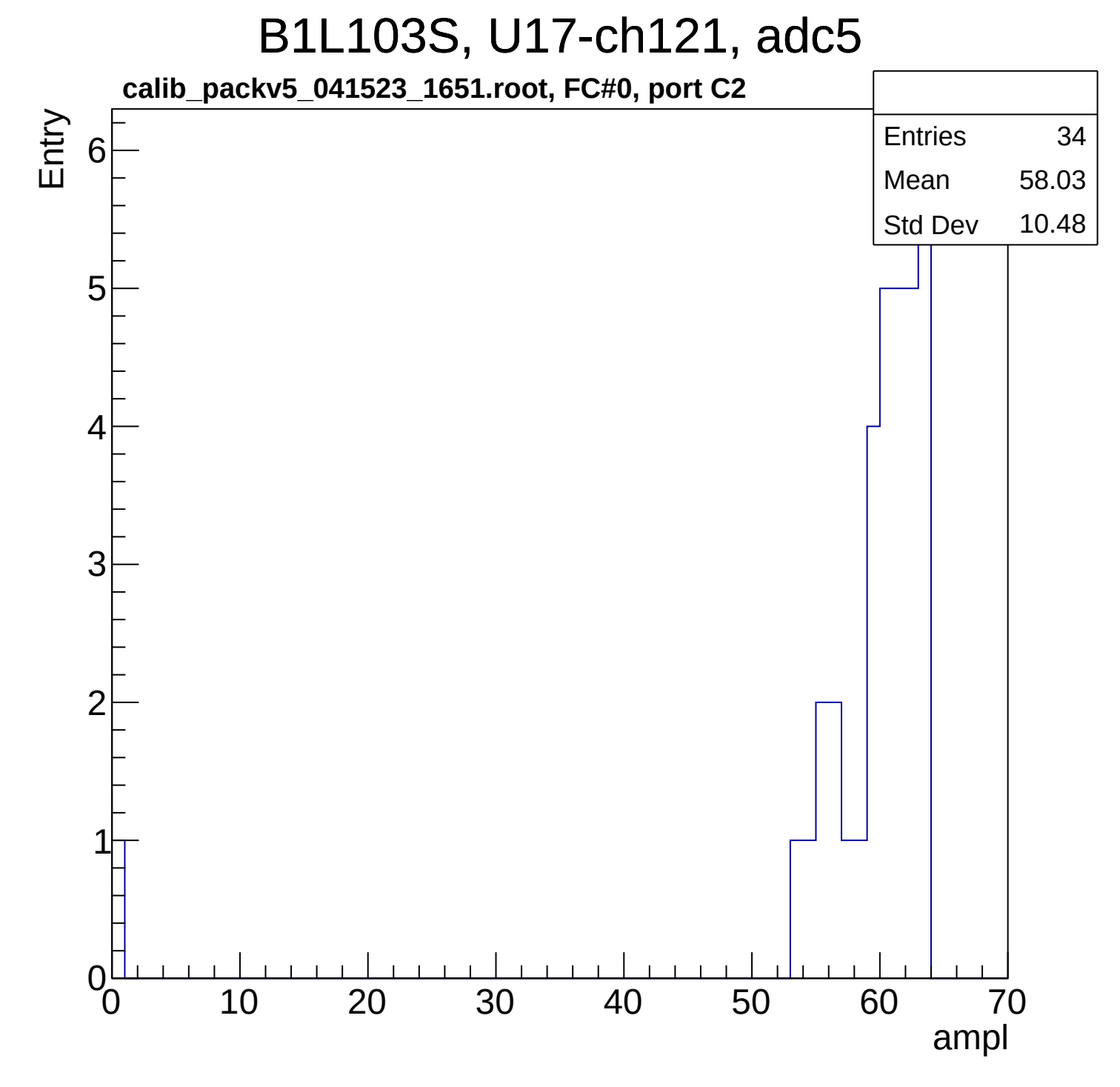
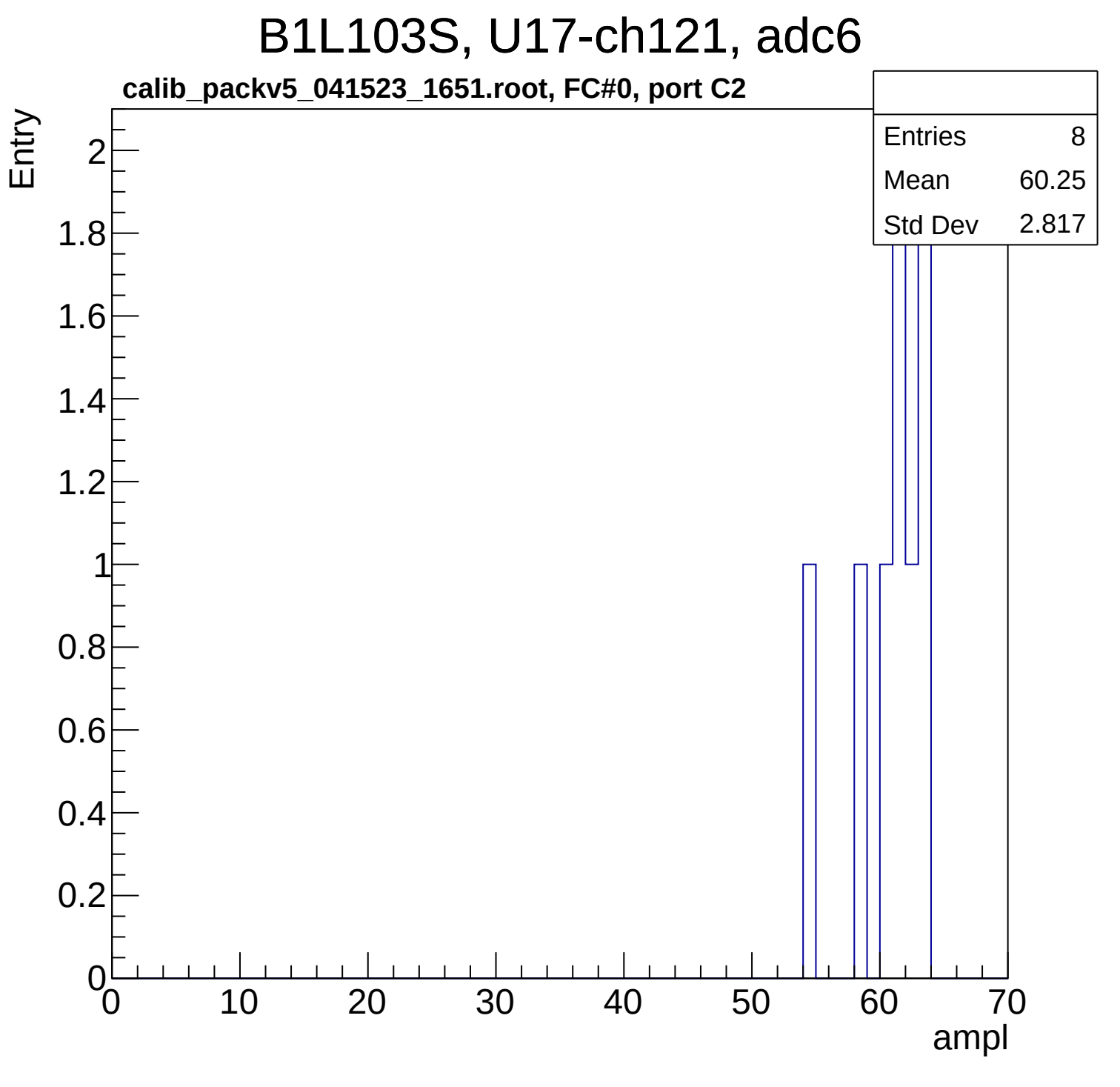
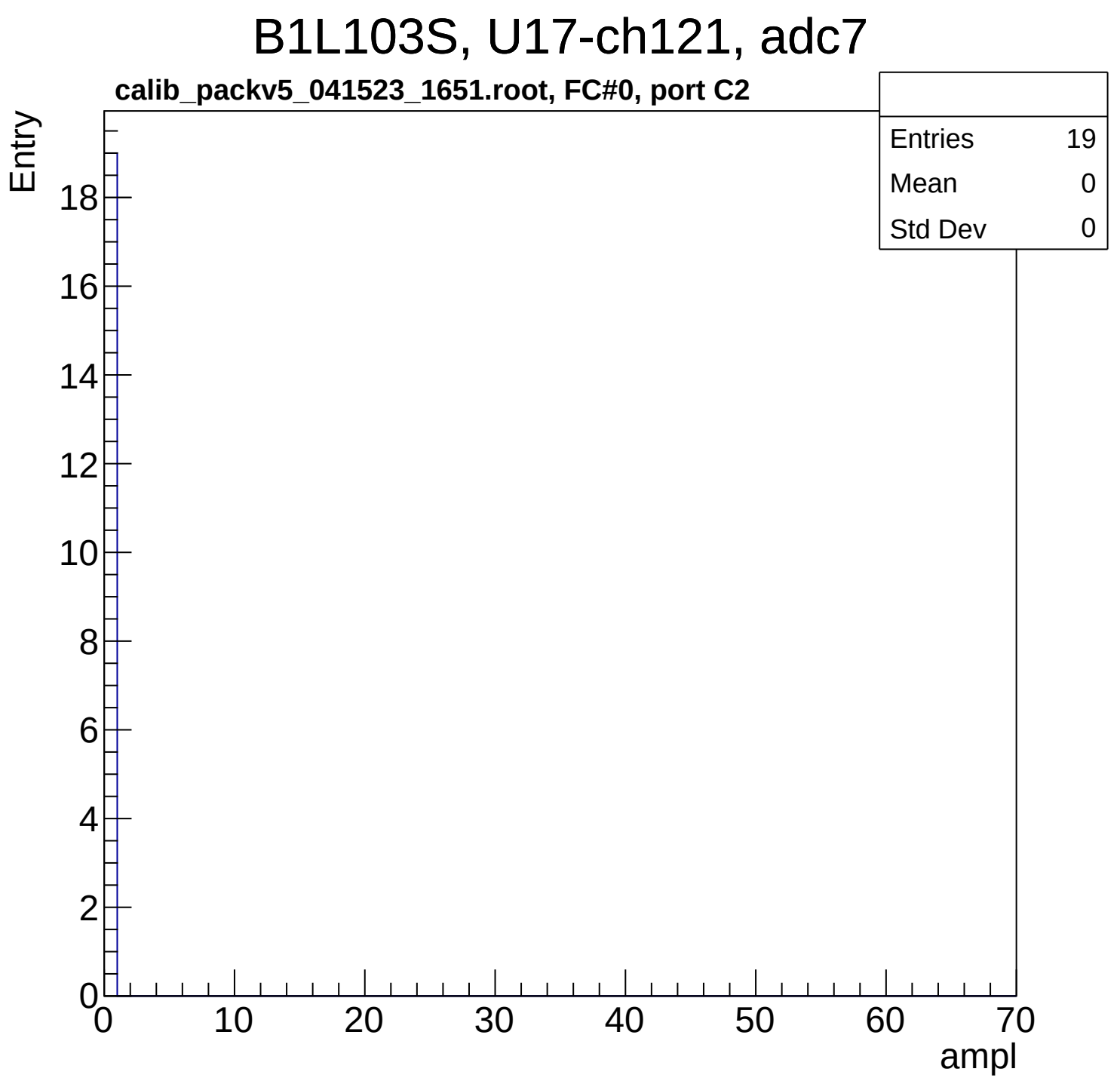
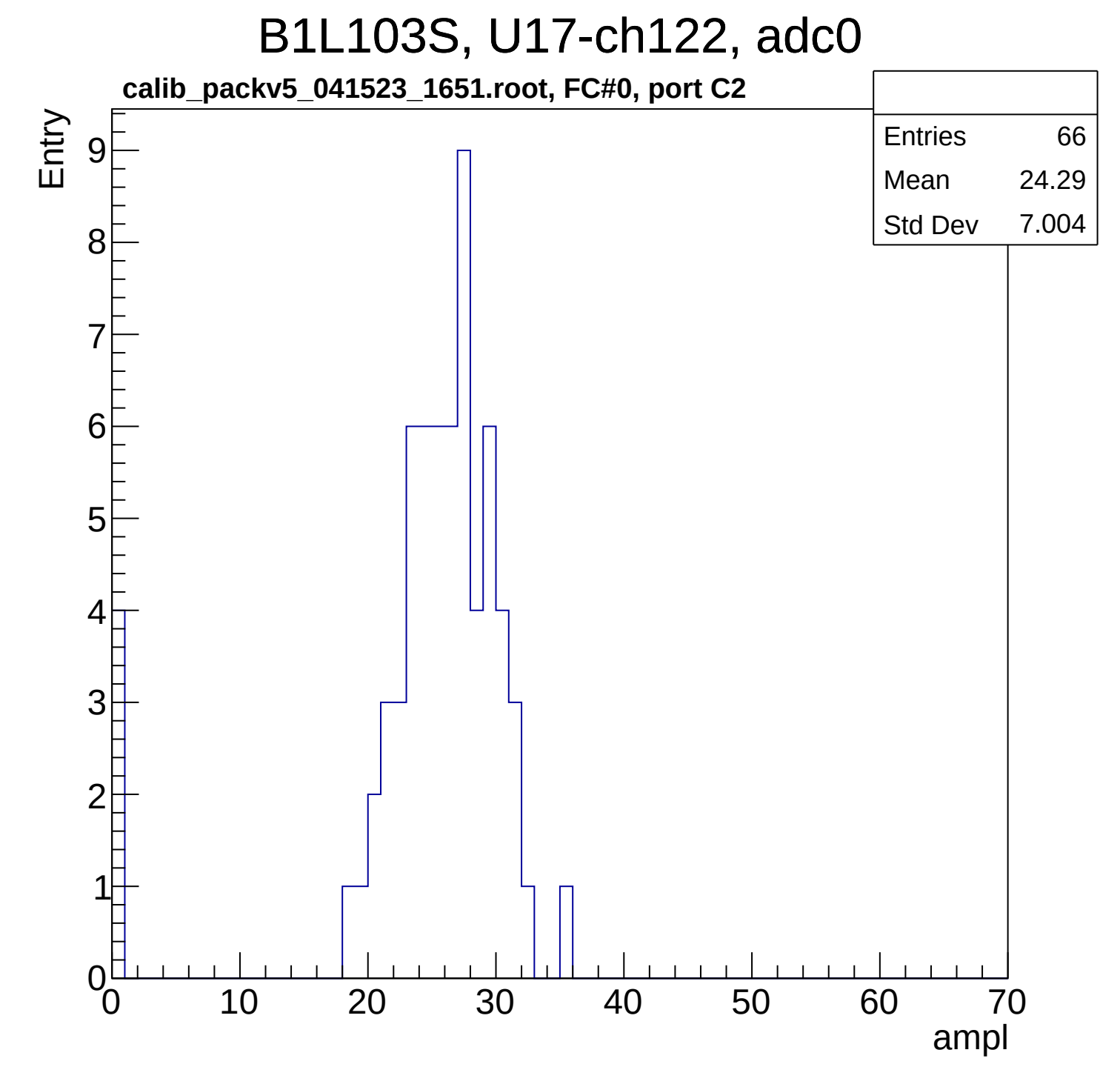
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U17-ch121, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 34
Mean 58.03
Std Dev 10.48
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U17-ch121, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 60.25
Std Dev 2.817
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U17-ch121, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch122, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 24.29
Std Dev 7.004
Entry
ampl
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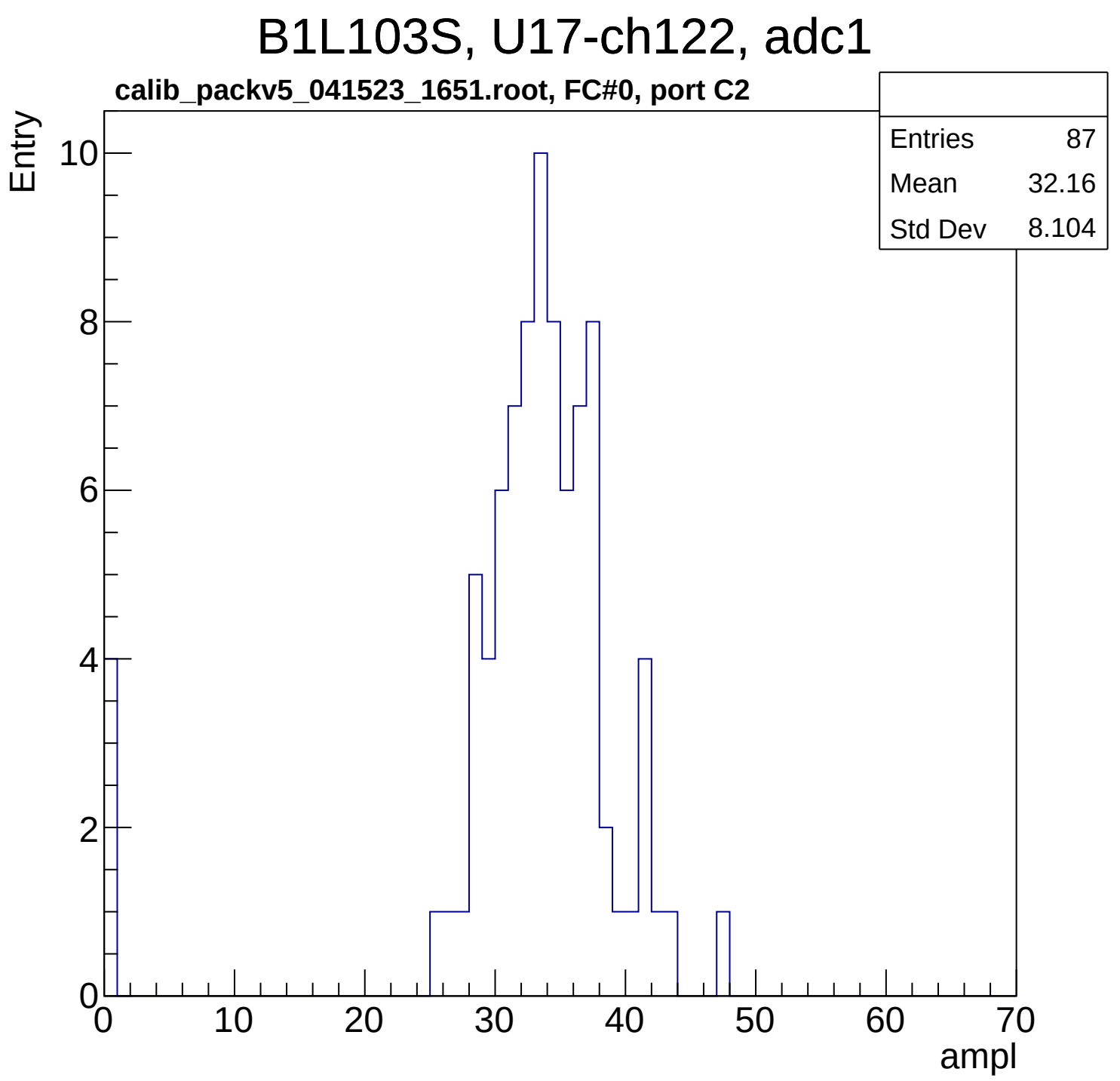
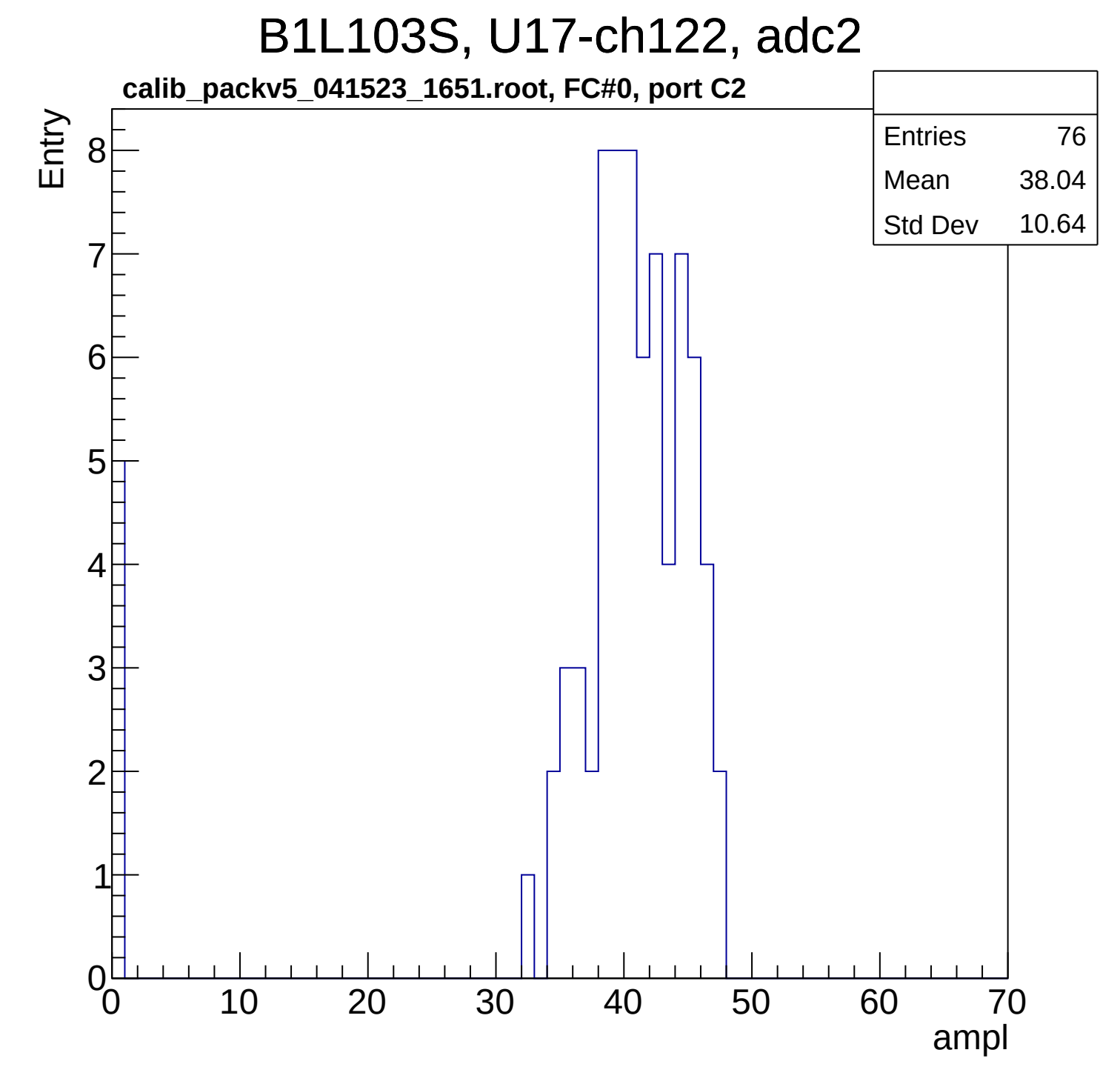
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U17-ch122, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 87
Mean 32.16
Std Dev 8.104
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U17-ch122, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 38.04
Std Dev 10.64
Entry
ampl
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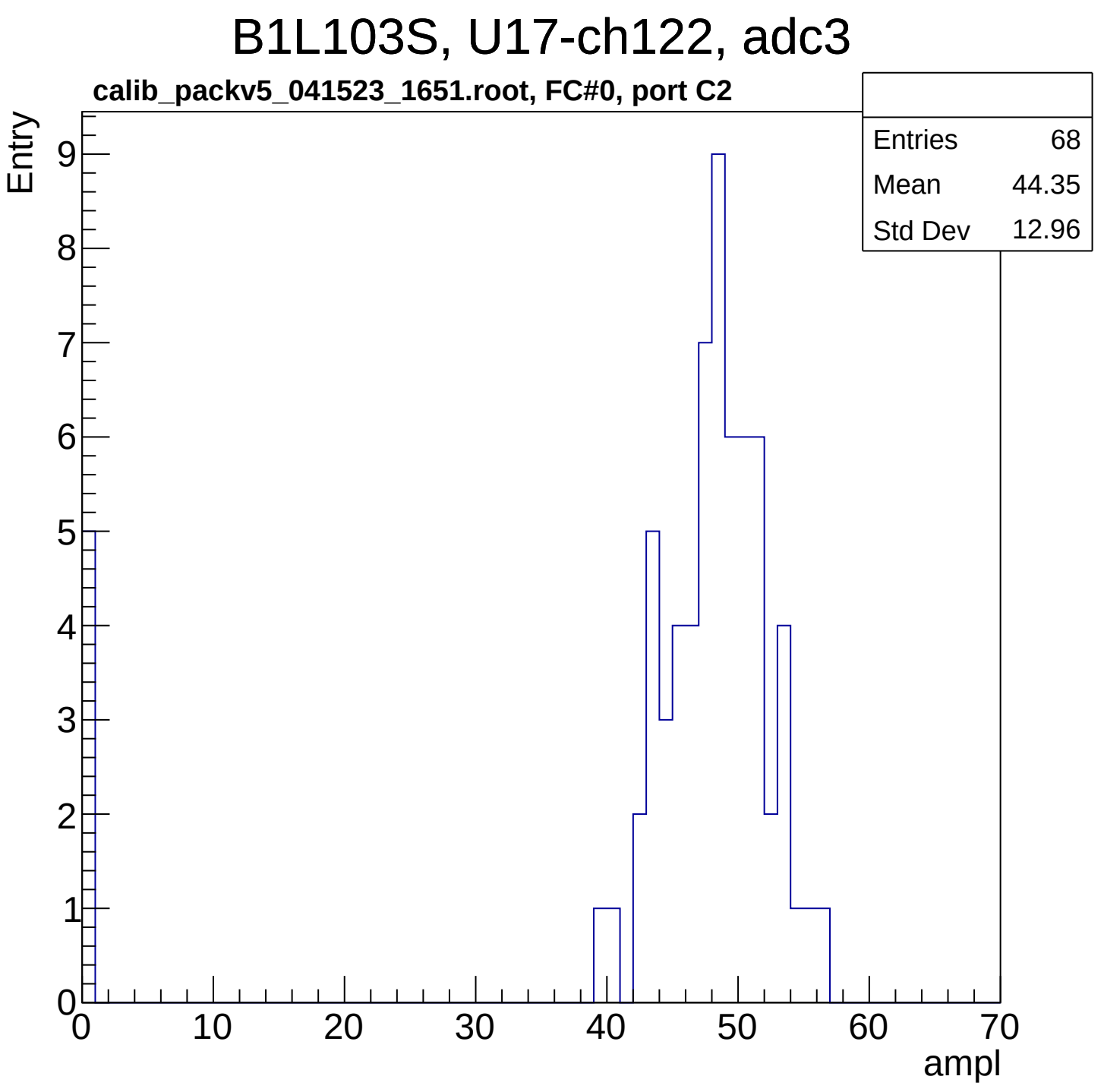
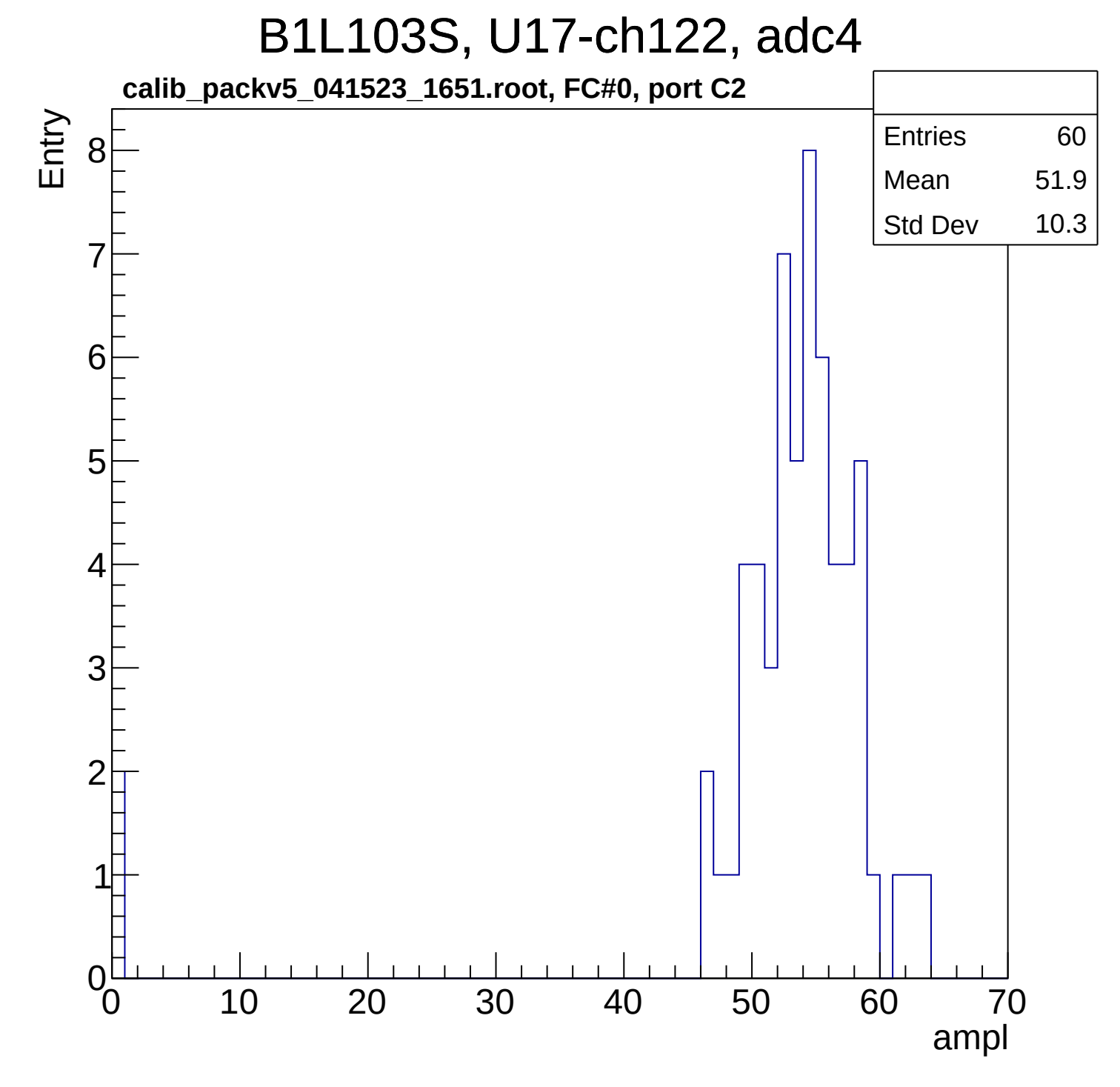
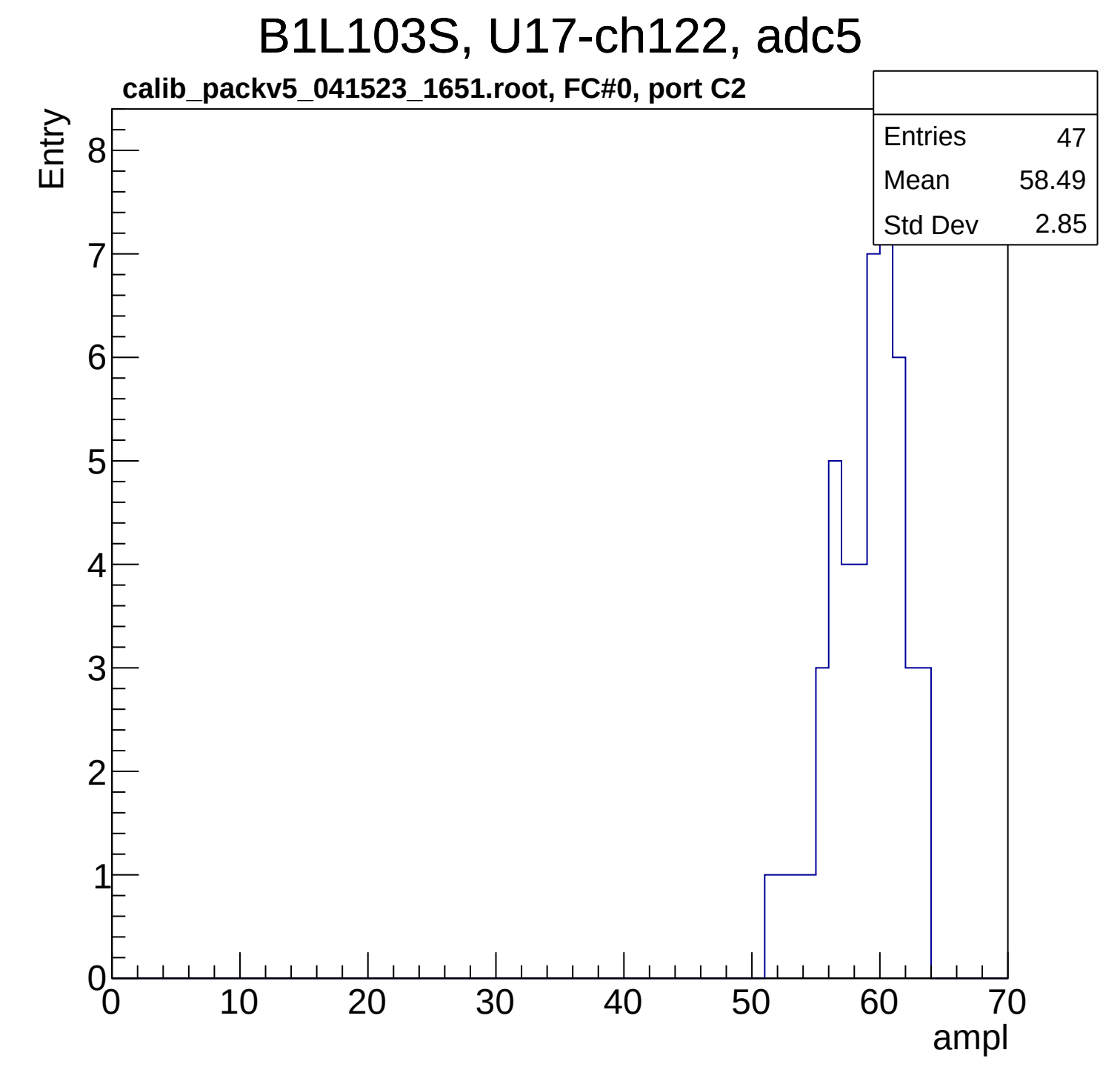
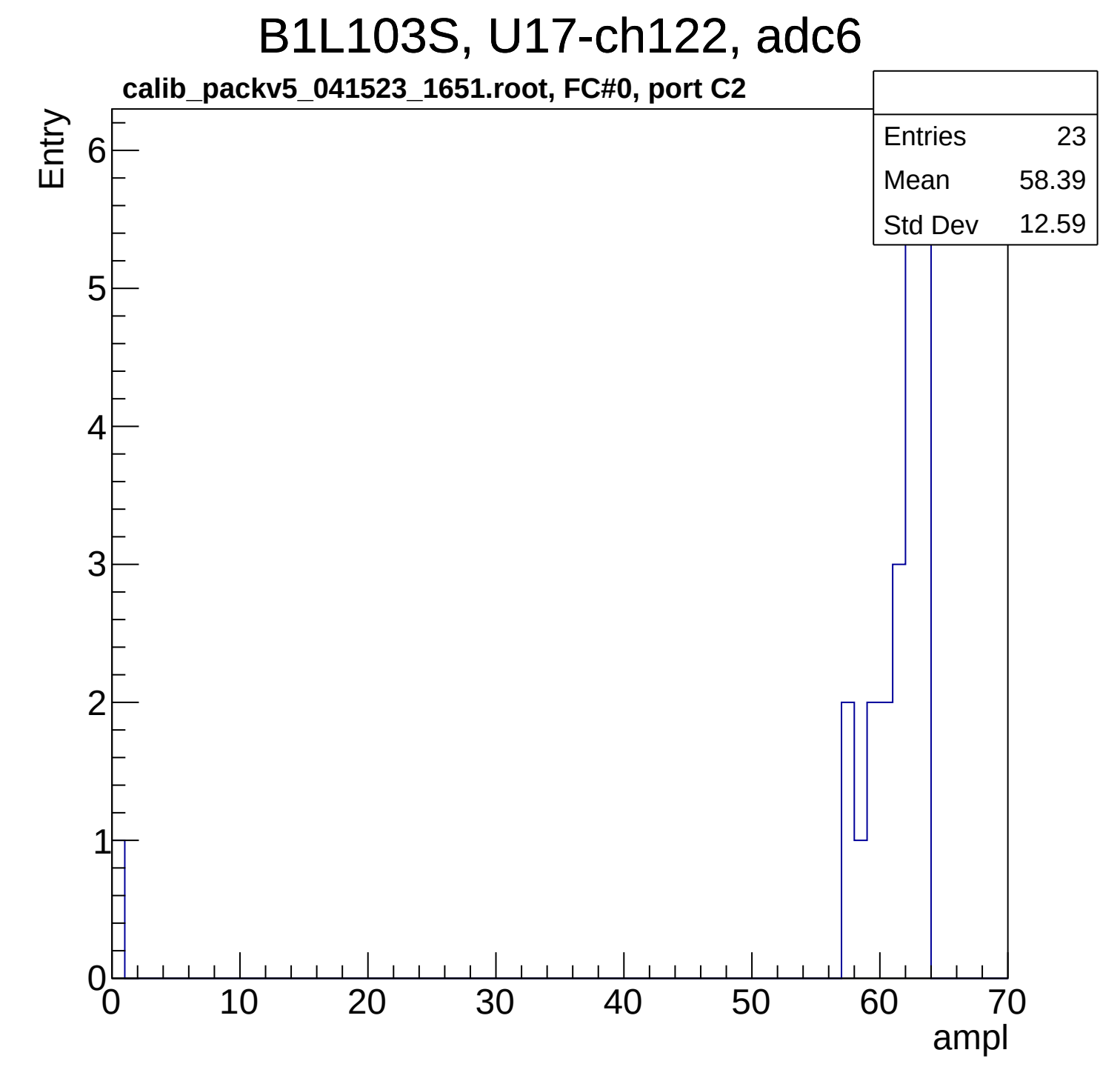
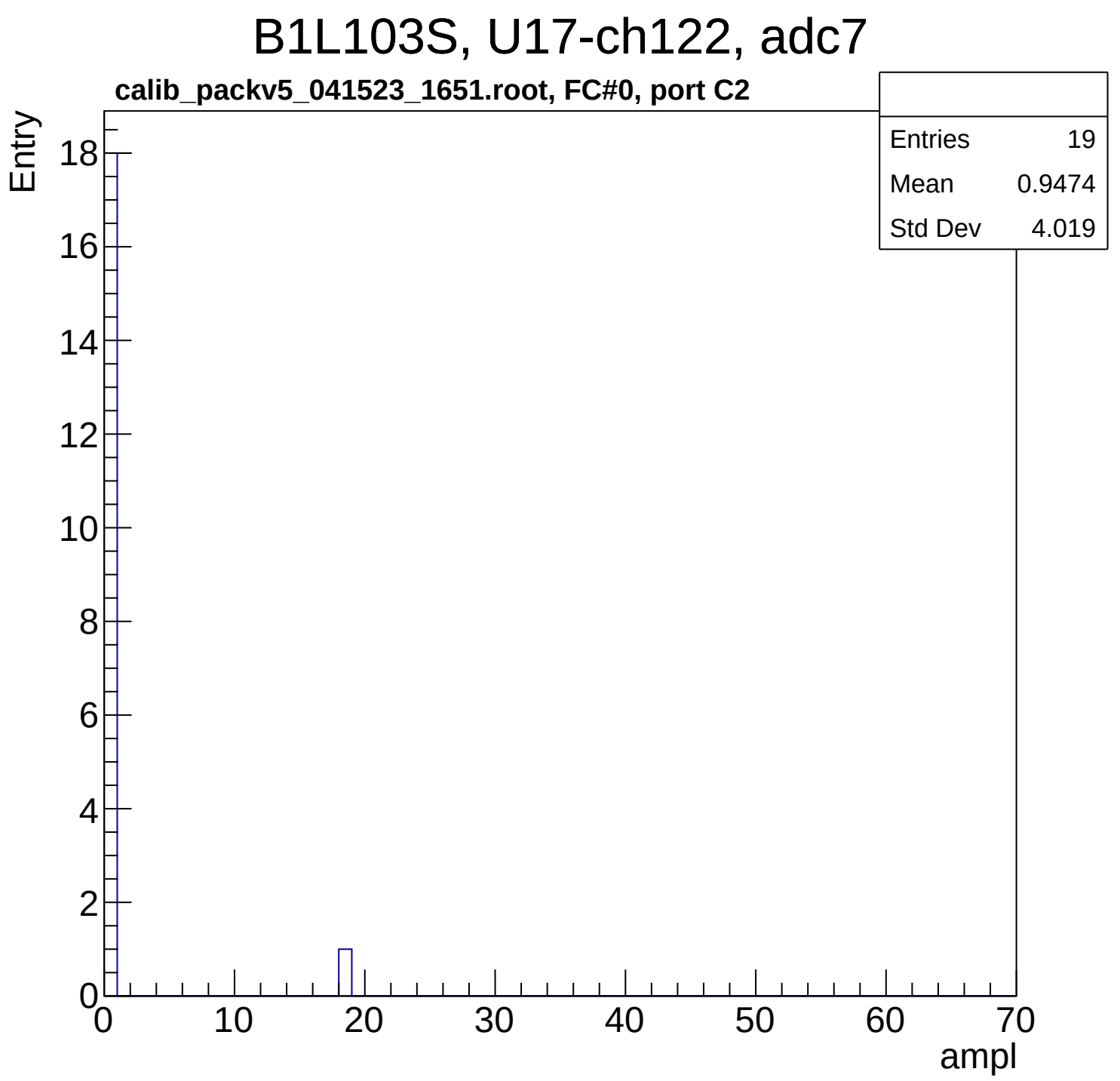
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

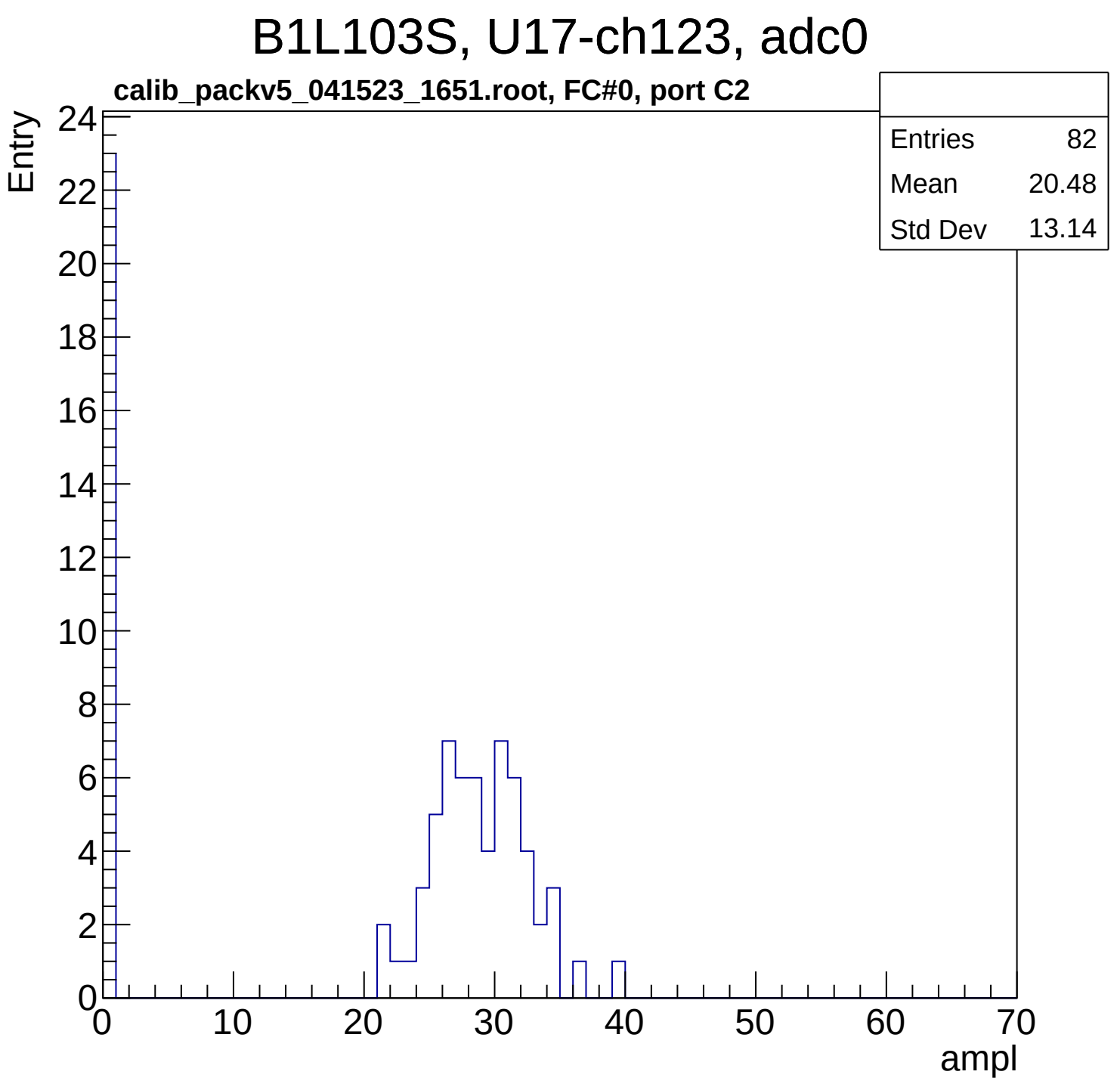

B1L103S, U17-ch122, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 44.35
Std Dev 12.96
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

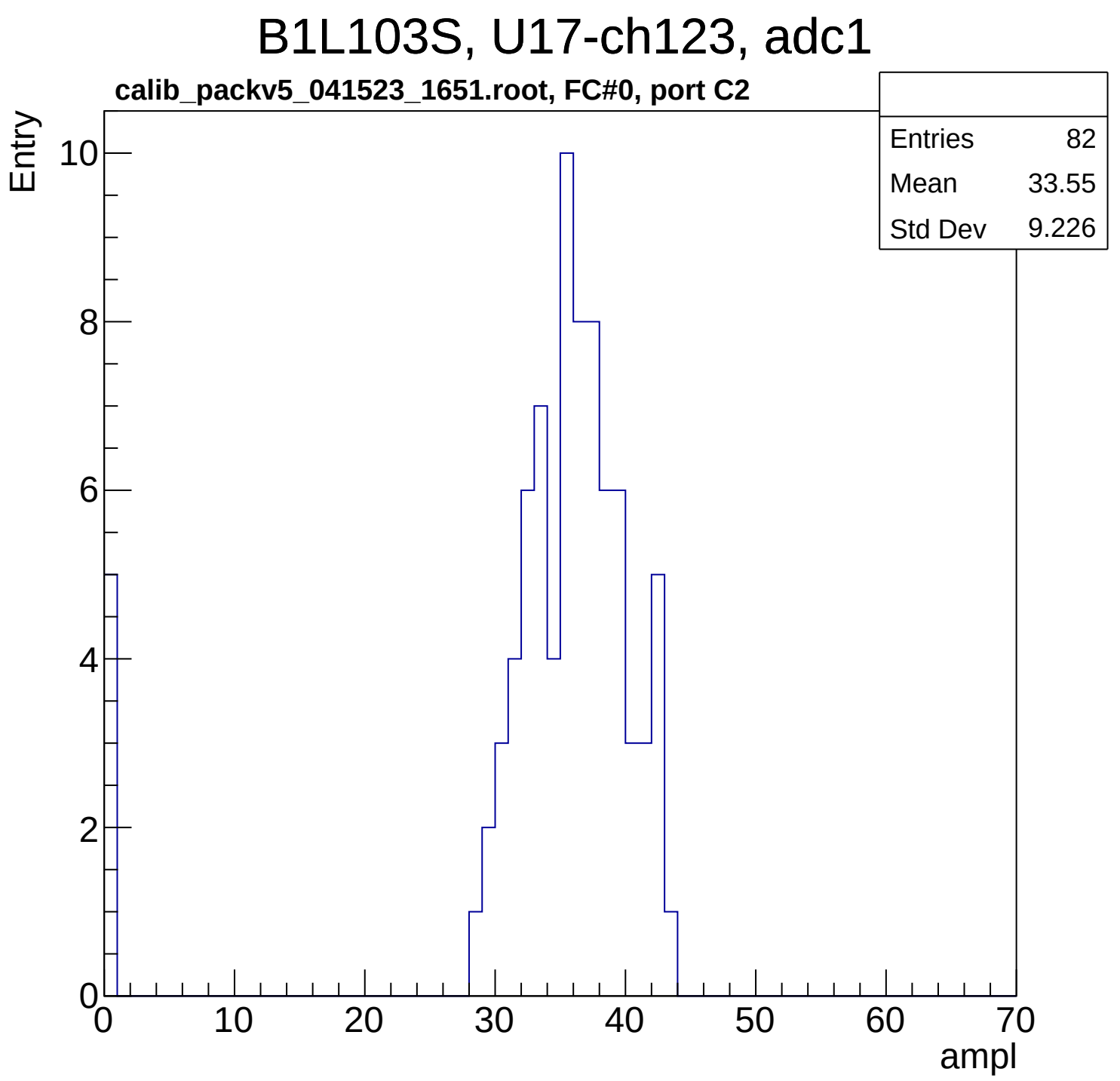

B1L103S, U17-ch122, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 51.9
Std Dev 10.3
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U17-ch122, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 58.49
Std Dev 2.85
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U17-ch122, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 23
Mean 58.39
Std Dev 12.59
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch122, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0.9474
Std Dev 4.019
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch123, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 20.48
Std Dev 13.14
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
22
24
0
10
20
30
40
50
60
70


B1L103S, U17-ch123, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 33.55
Std Dev 9.226
Entry
ampl
0
2
4
6
8
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0
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20
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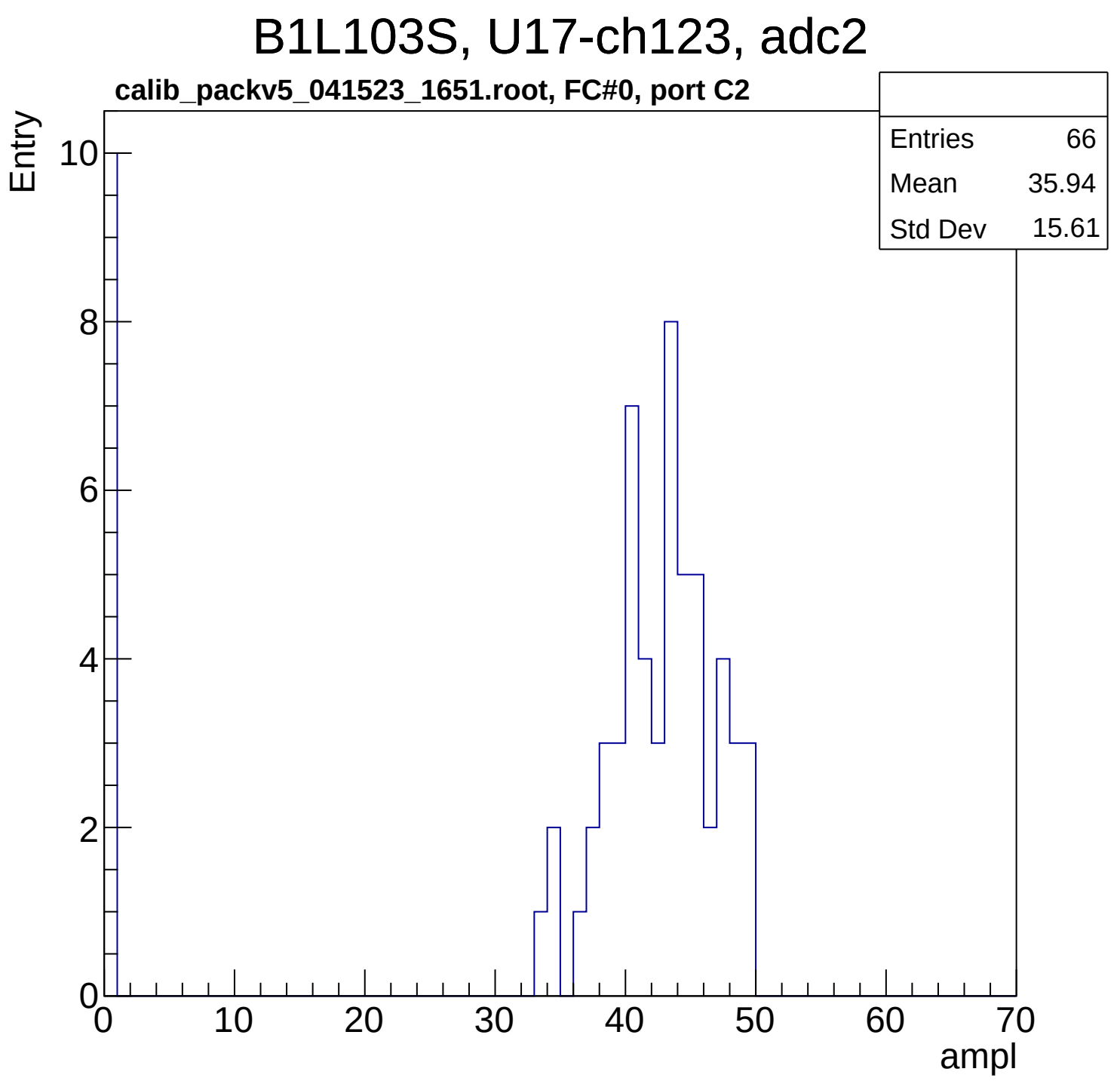
40
50
60
70


B1L103S, U17-ch123, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 35.94
Std Dev 15.61
Entry
ampl
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6
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0
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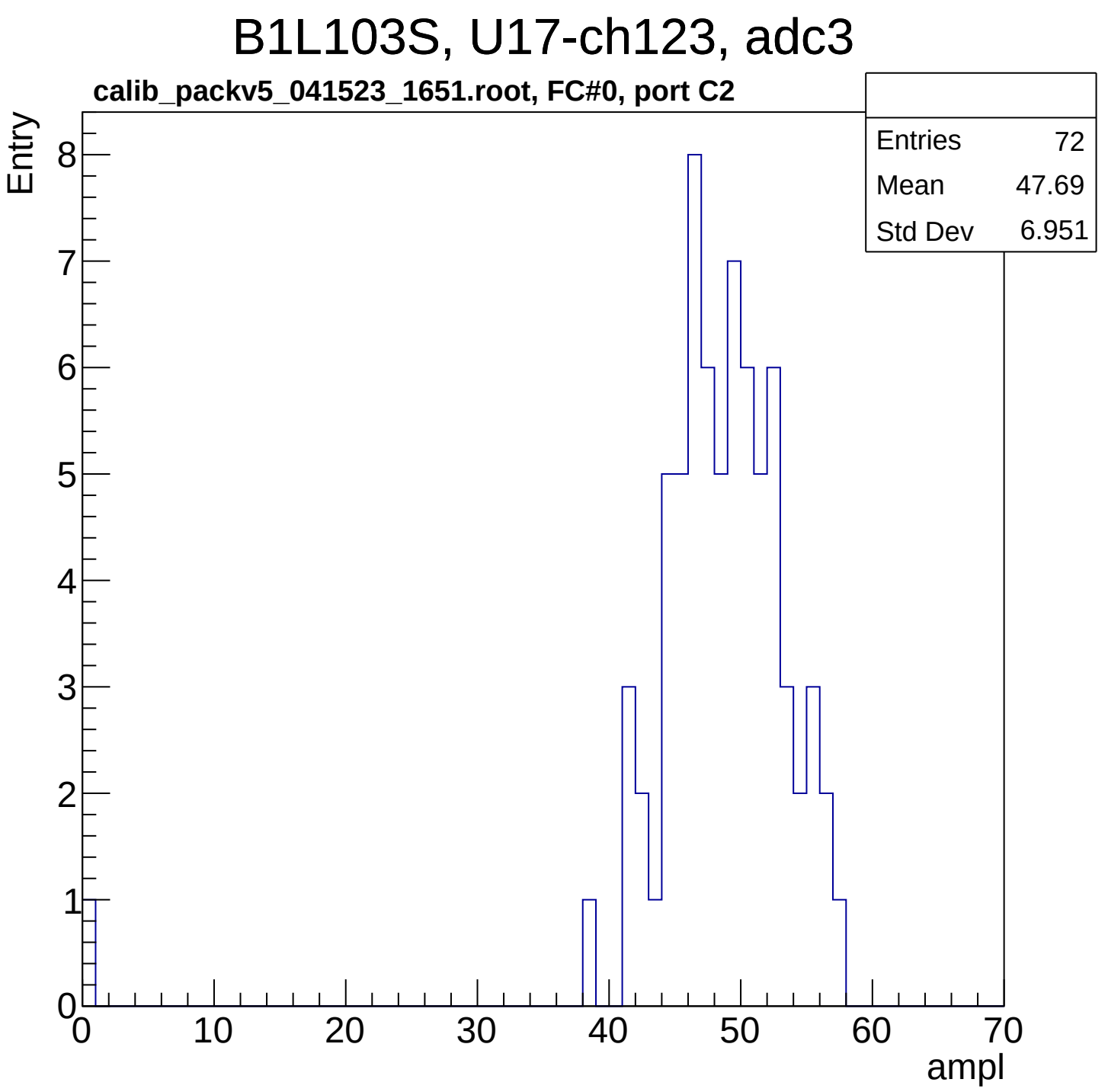
20
30
40
50
60
70


B1L103S, U17-ch123, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 47.69
Std Dev 6.951
Entry
ampl
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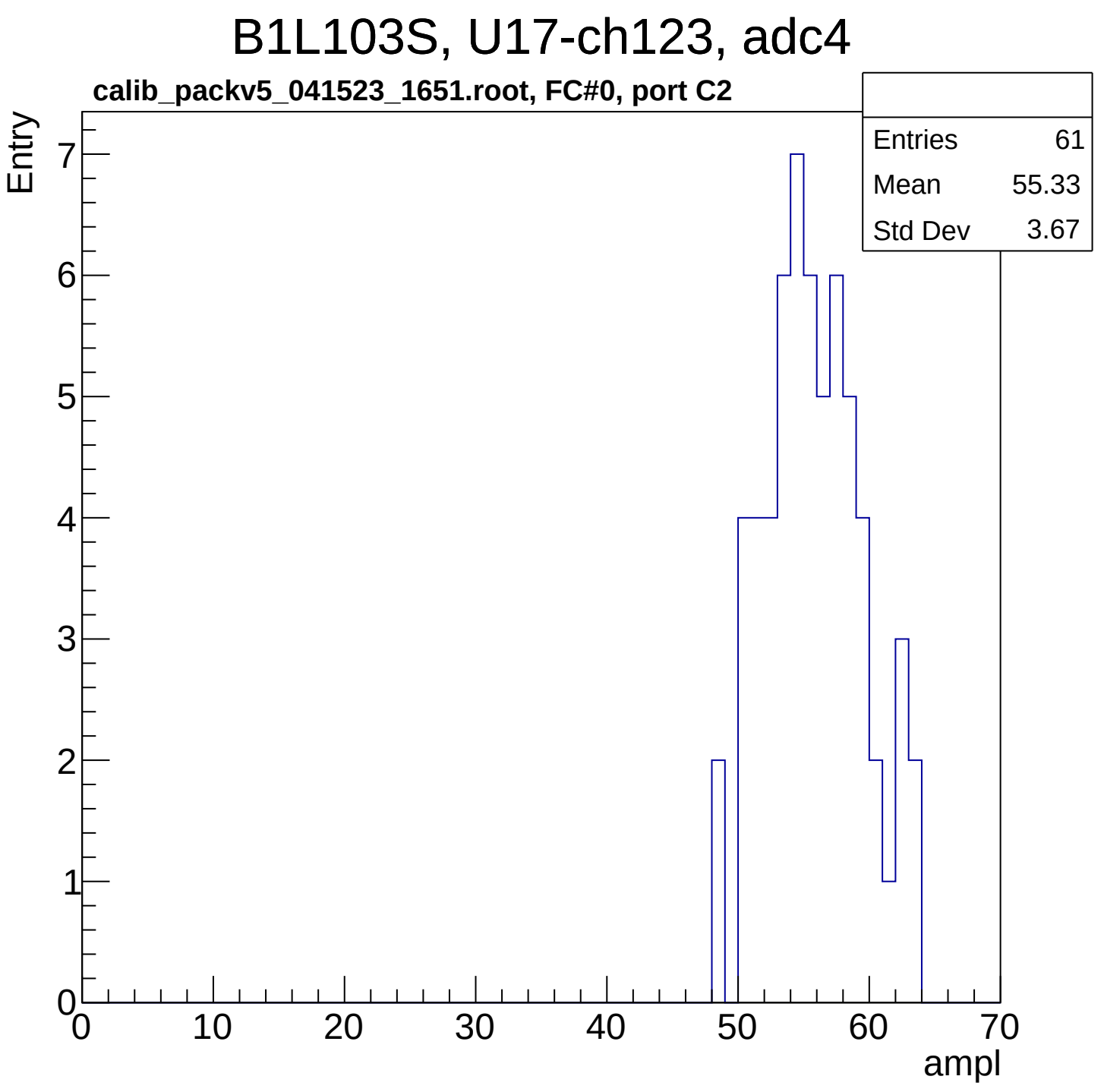
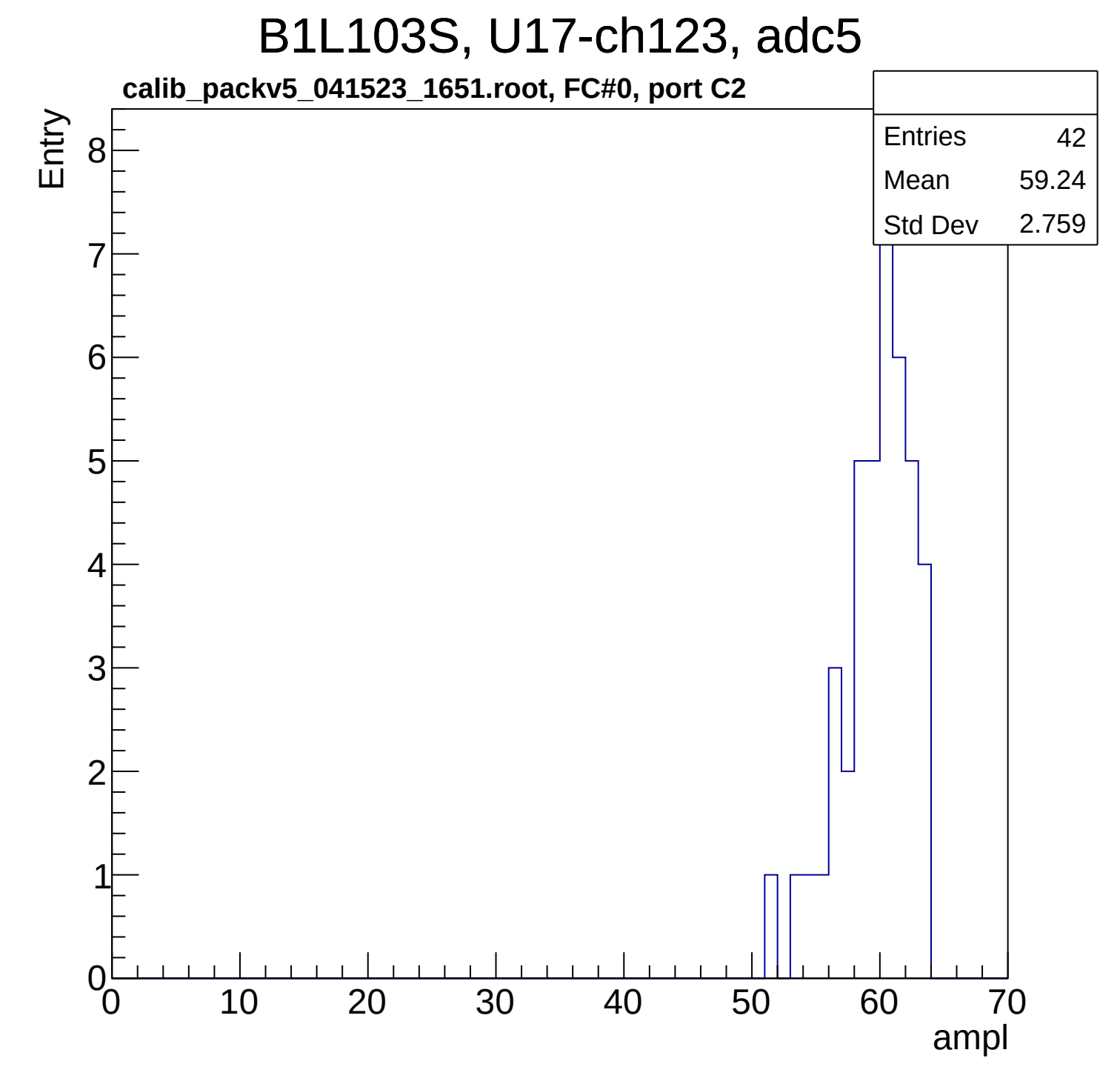
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U17-ch123, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 55.33
Std Dev 3.67
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U17-ch123, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 42
Mean 59.24
Std Dev 2.759
Entry
ampl
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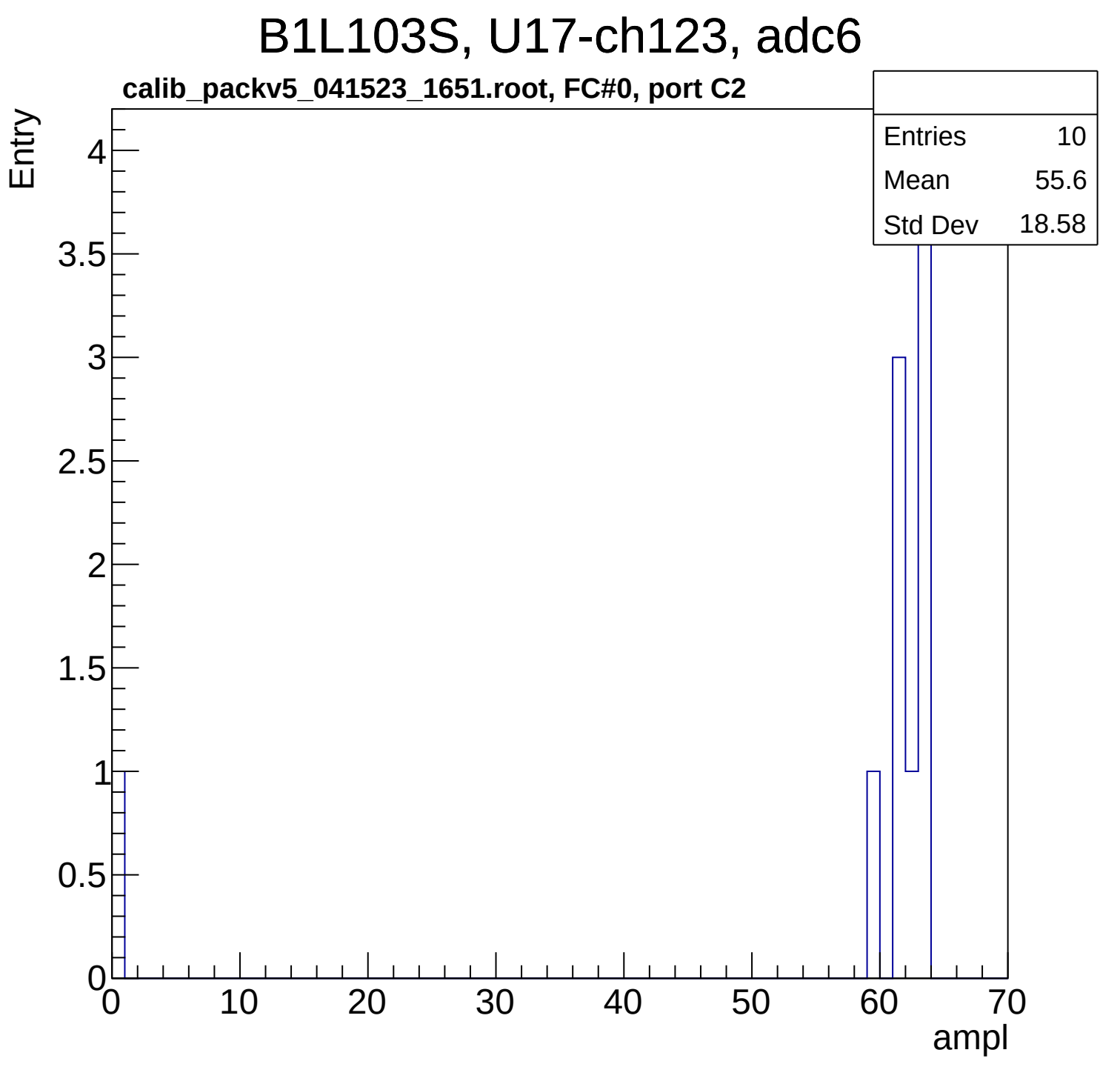
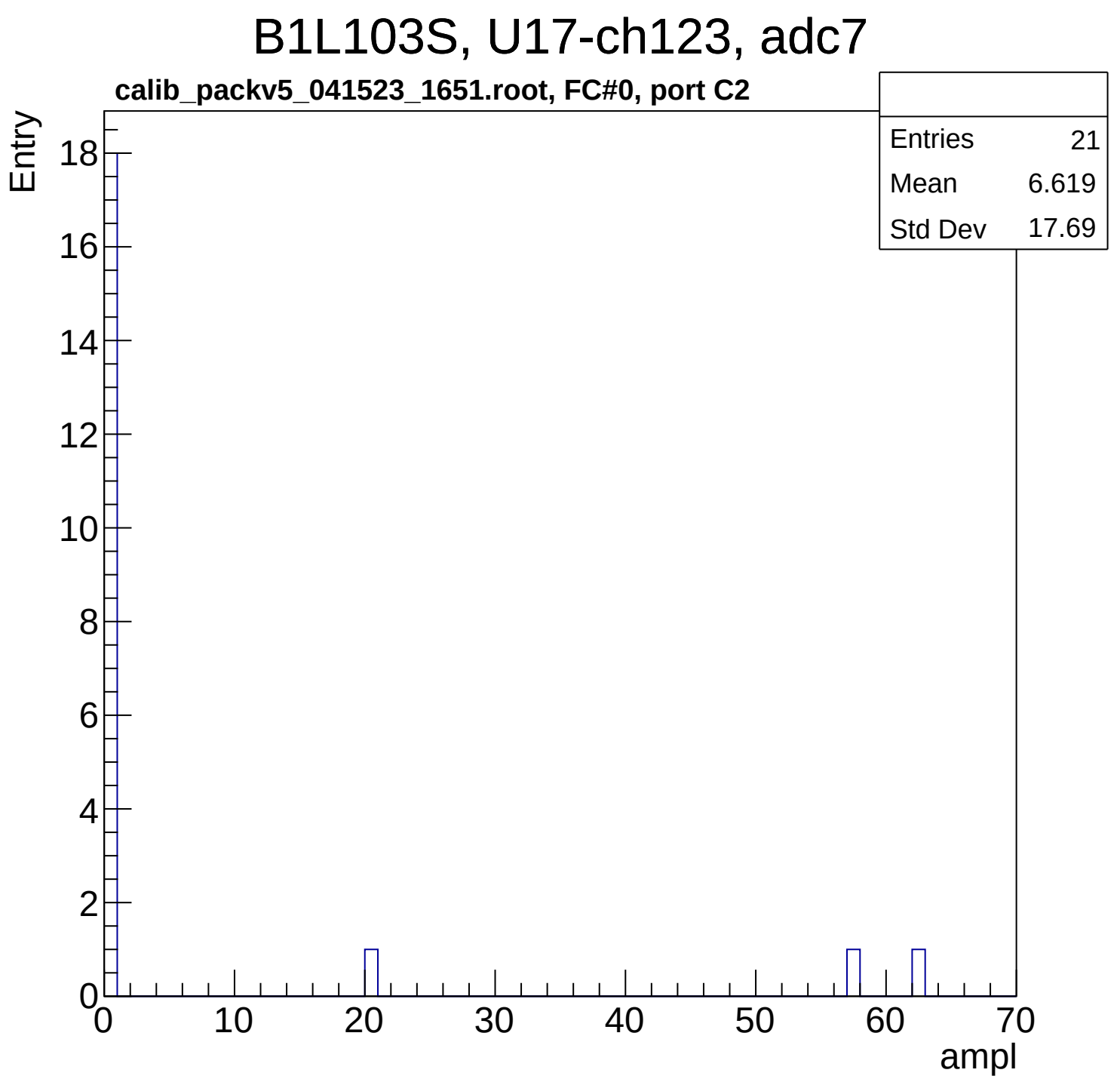
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U17-ch123, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 55.6
Std Dev 18.58
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U17-ch123, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 6.619
Std Dev 17.69
Entry
0
2
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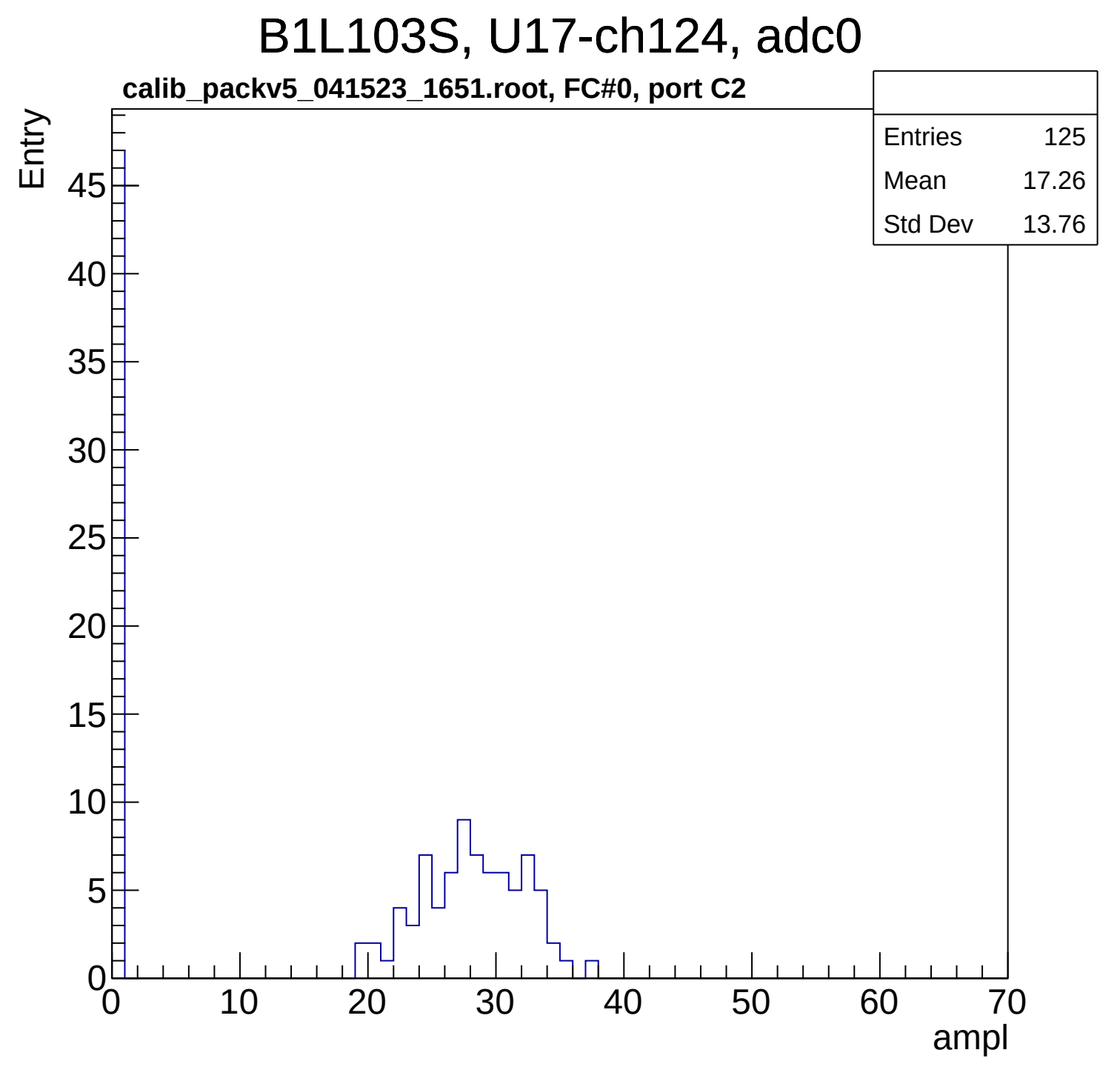
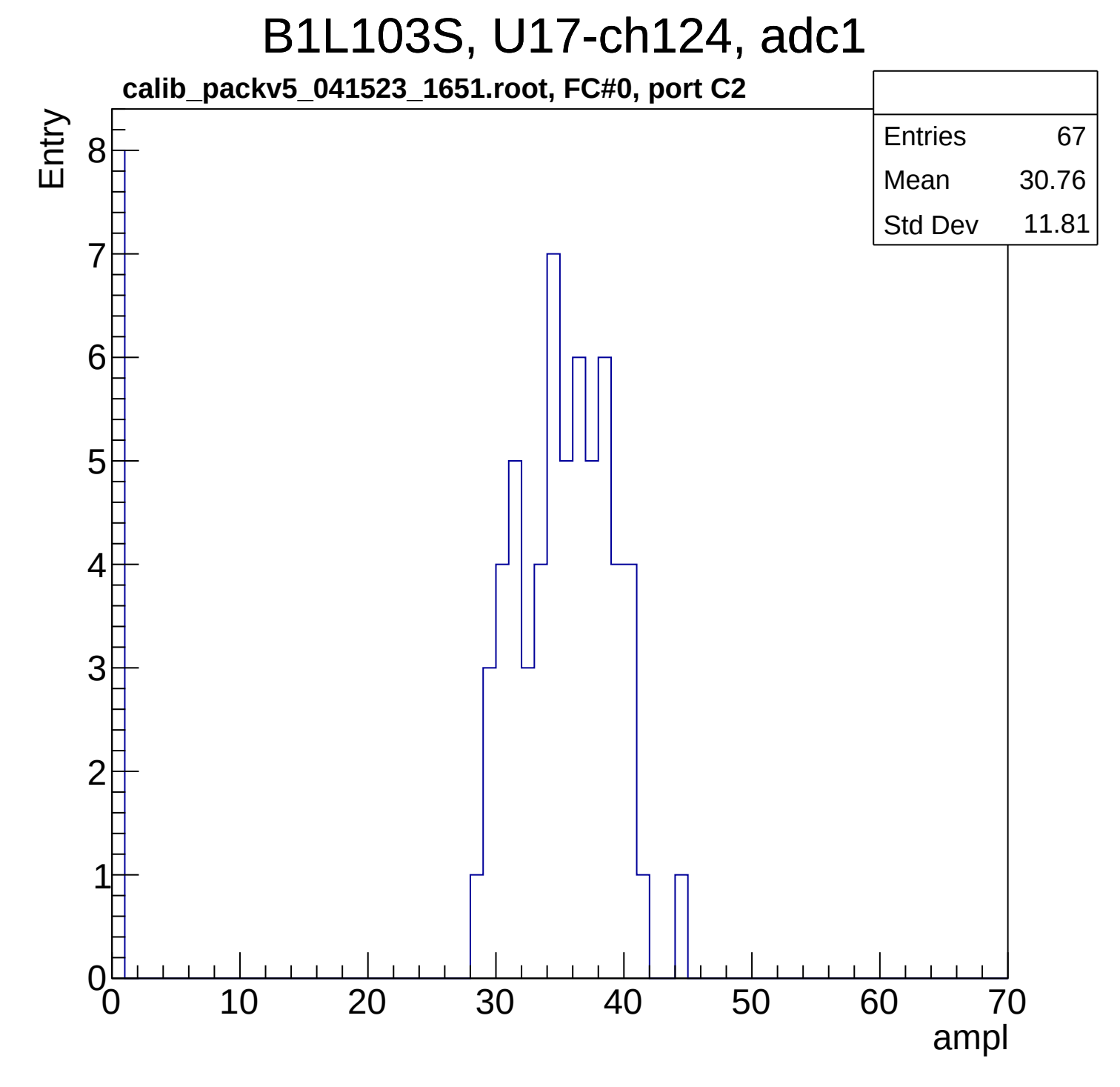
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch124, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 125
Mean 17.26
Std Dev 13.76
Entry
0
5
10
15
20
25
30
35
40
45
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch124, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 30.76
Std Dev 11.81
Entry
ampl
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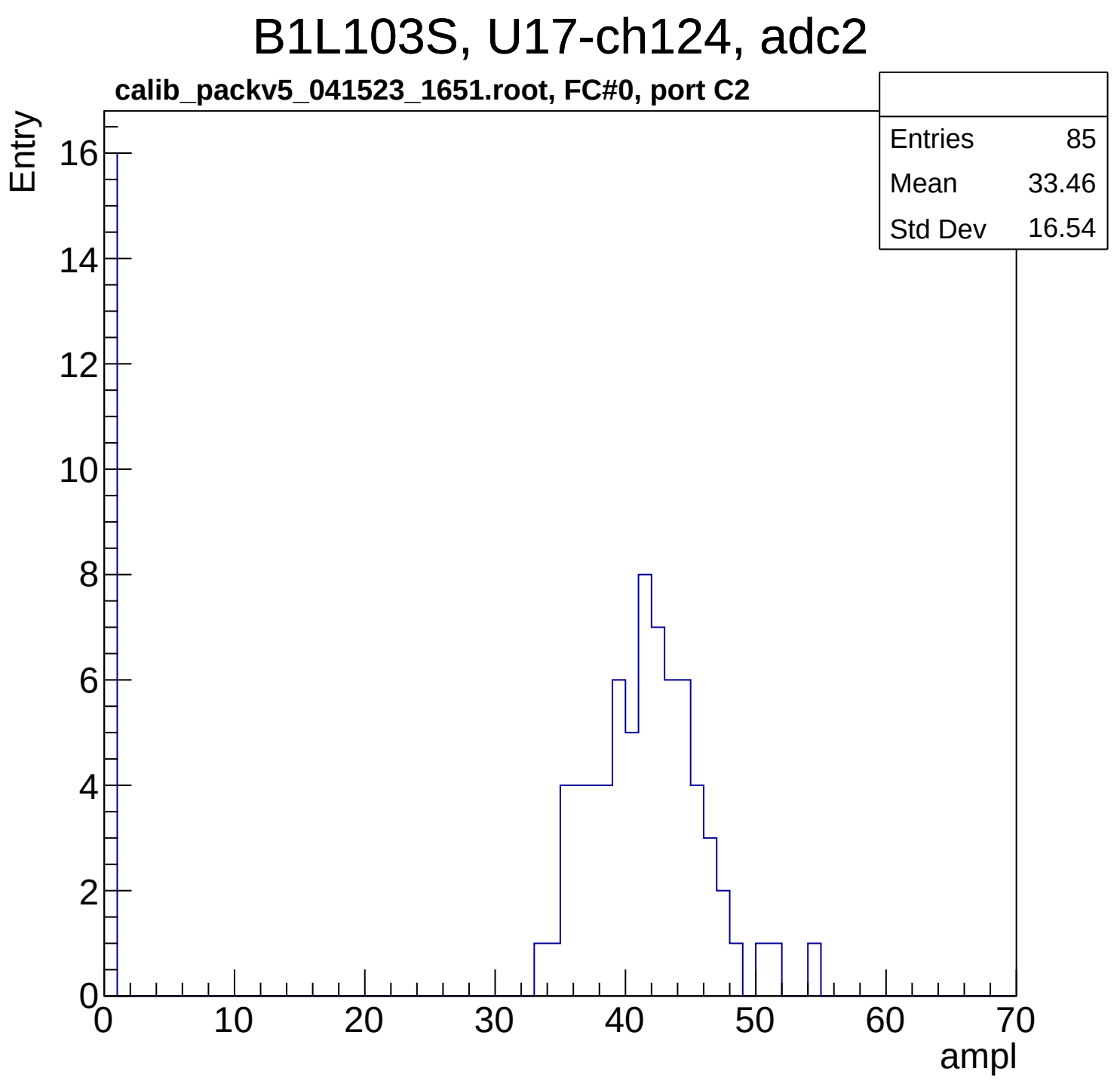
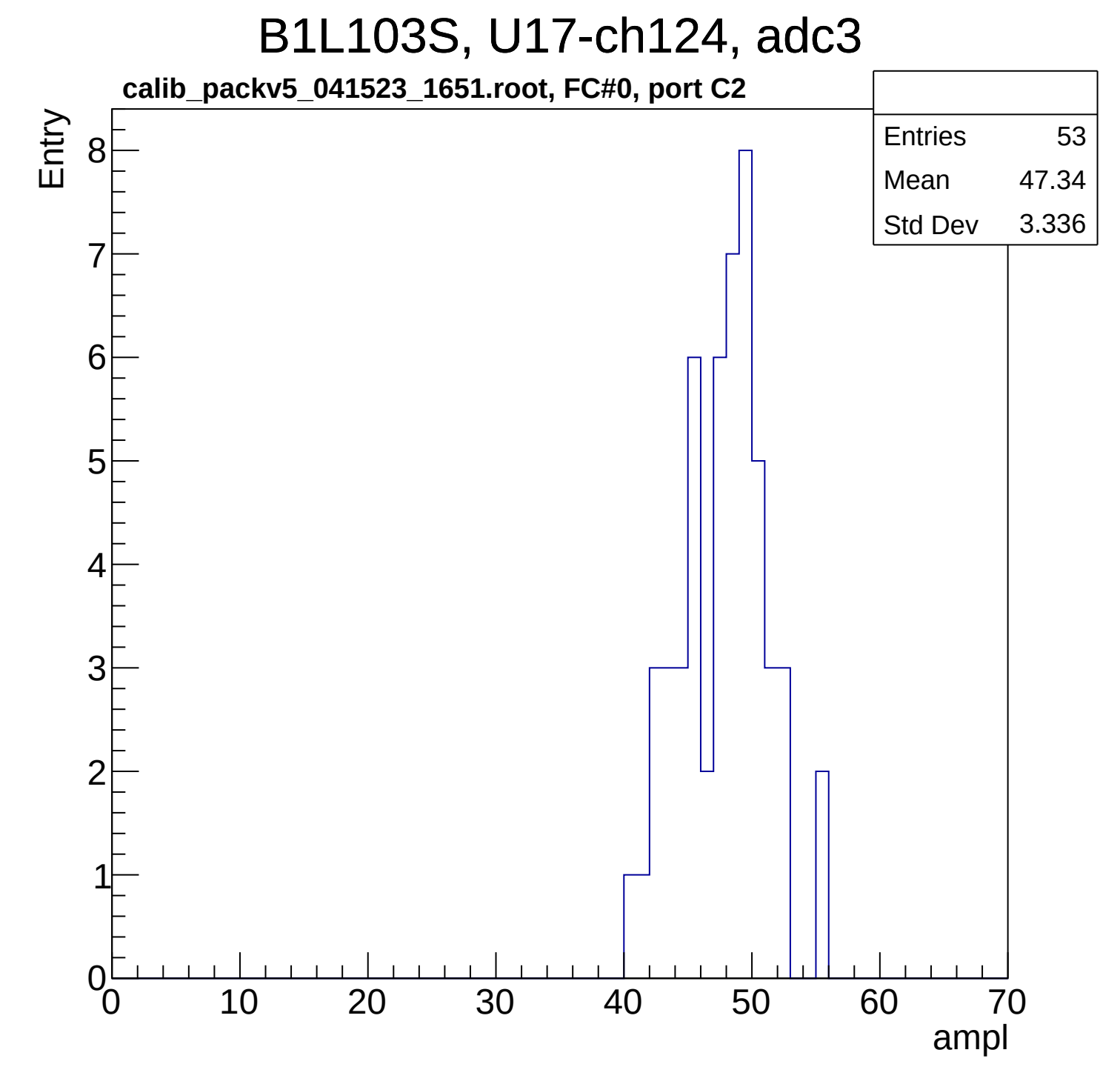
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U17-ch124, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 33.46
Std Dev 16.54
Entry
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch124, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 47.34
Std Dev 3.336
Entry
ampl
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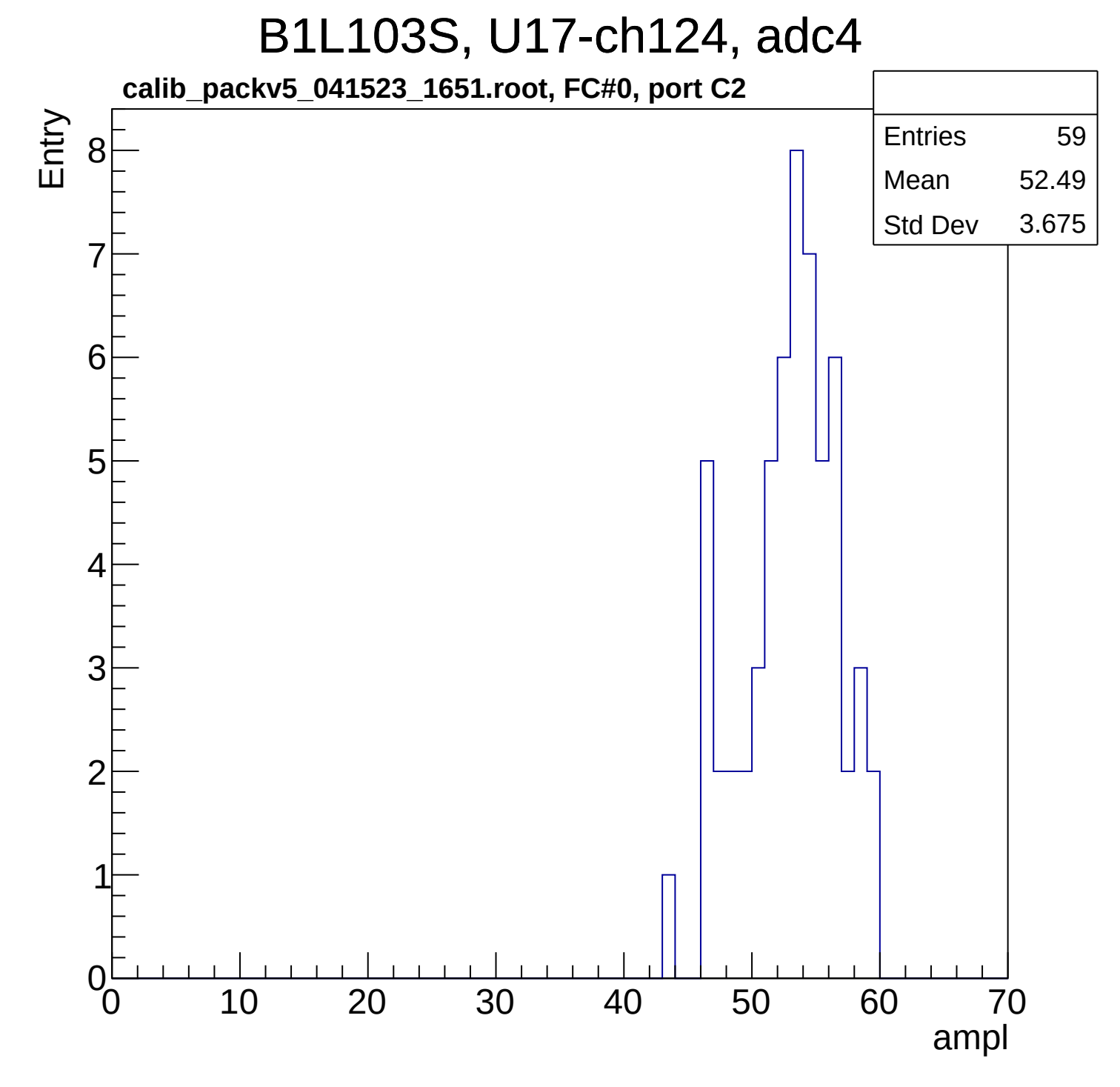
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U17-ch124, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 52.49
Std Dev 3.675
Entry
ampl
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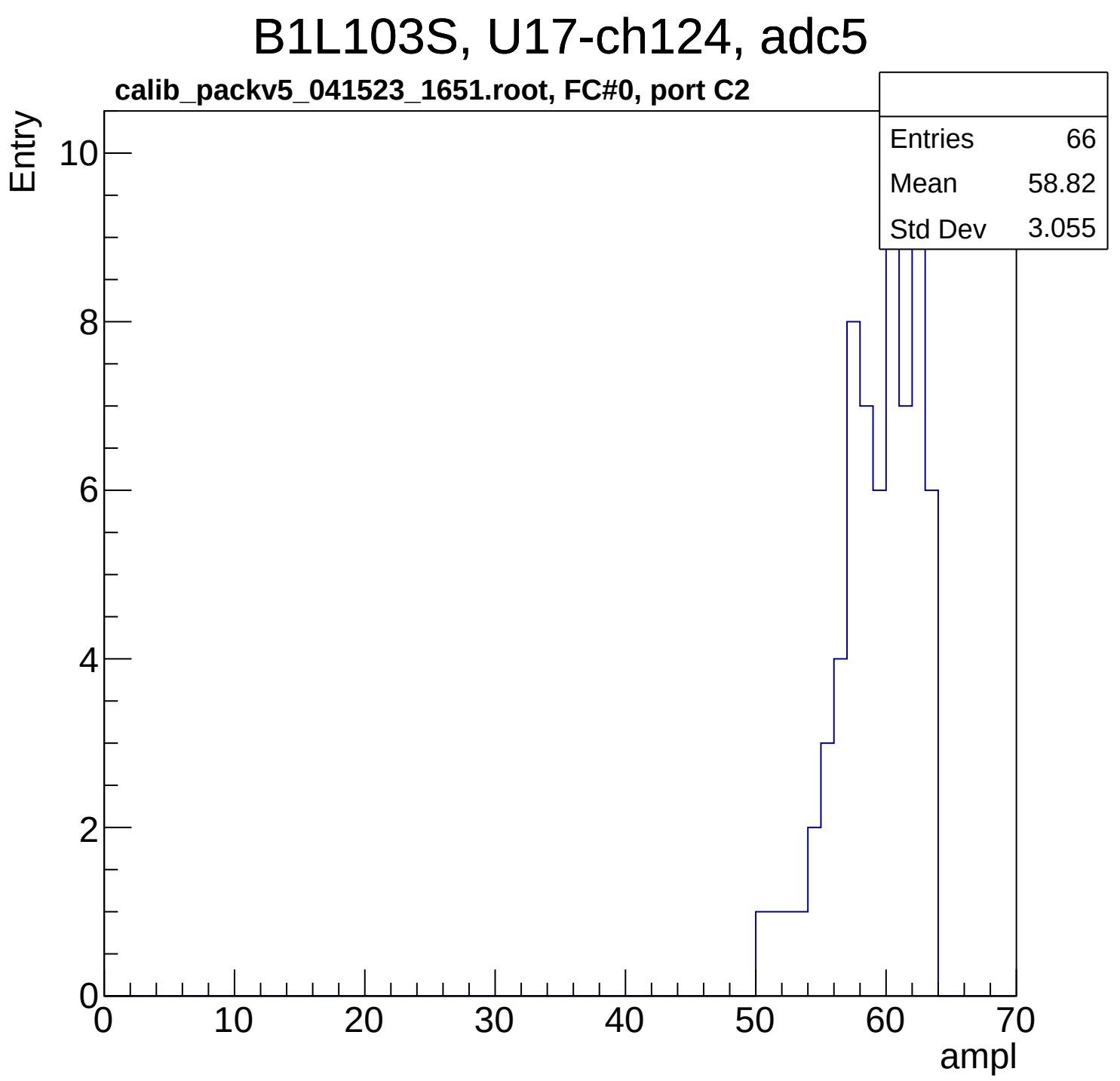
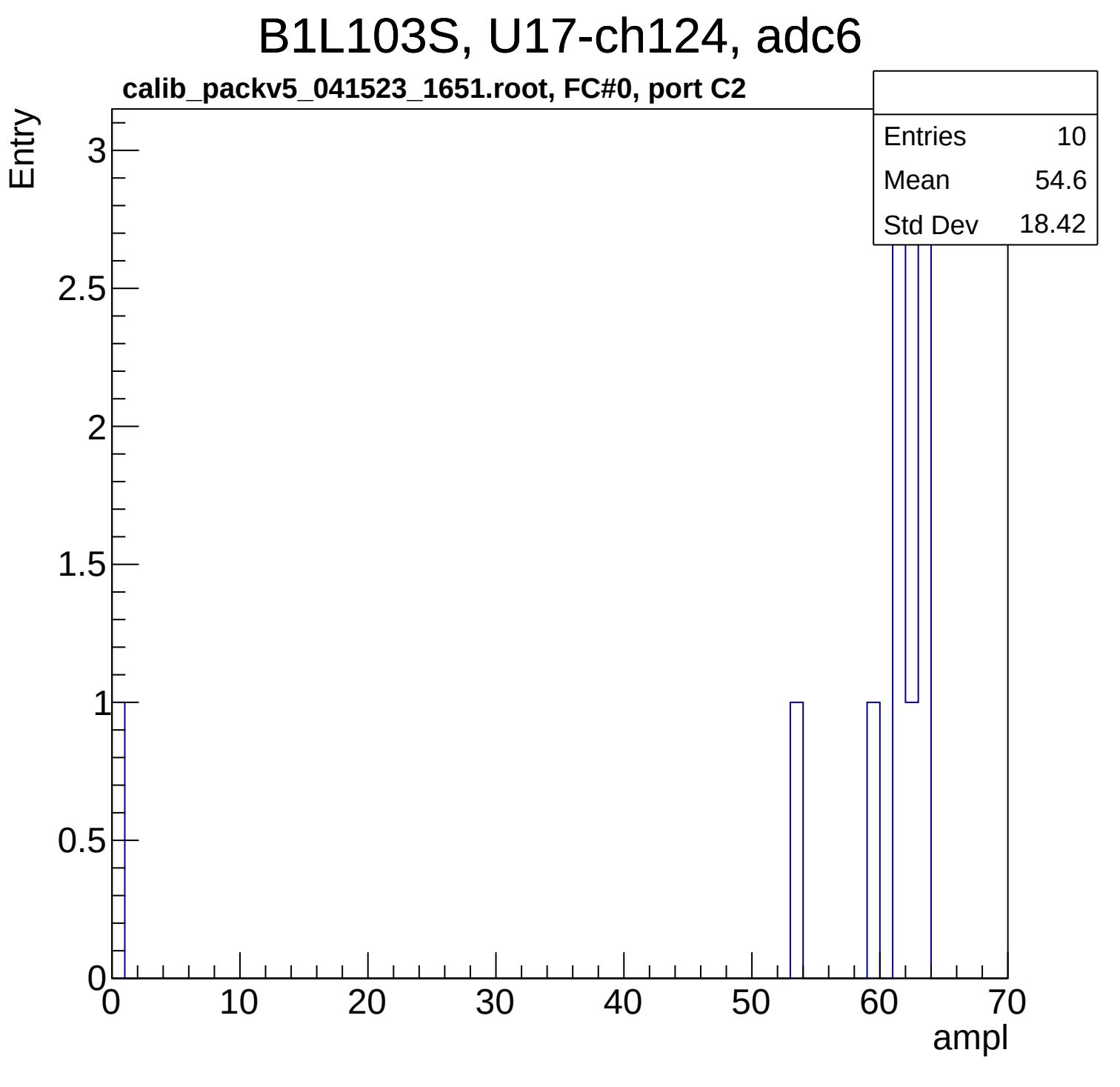
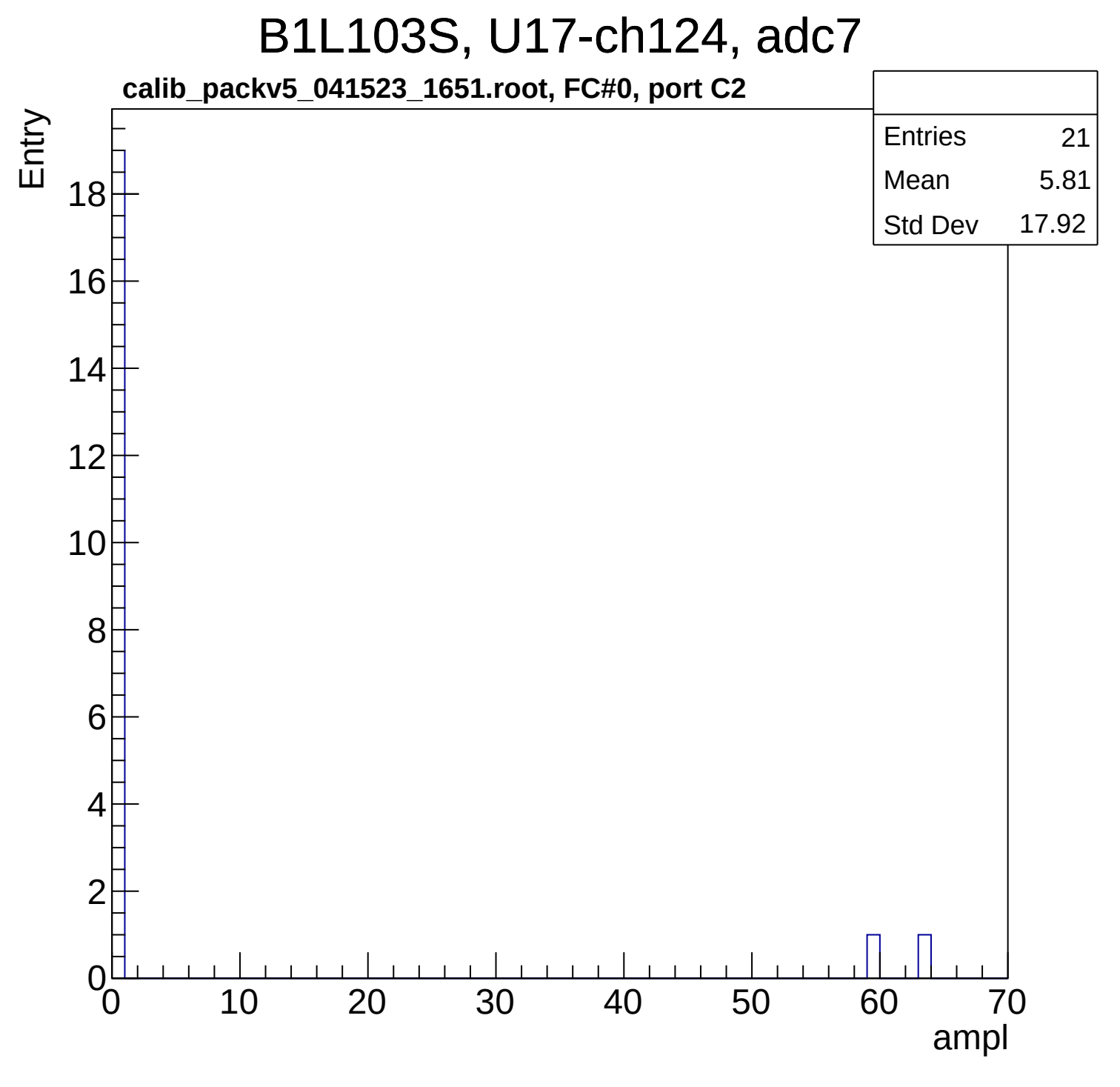
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U17-ch124, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 58.82
Std Dev 3.055
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U17-ch124, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 54.6
Std Dev 18.42
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U17-ch124, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 5.81
Std Dev 17.92
Entry
0
2
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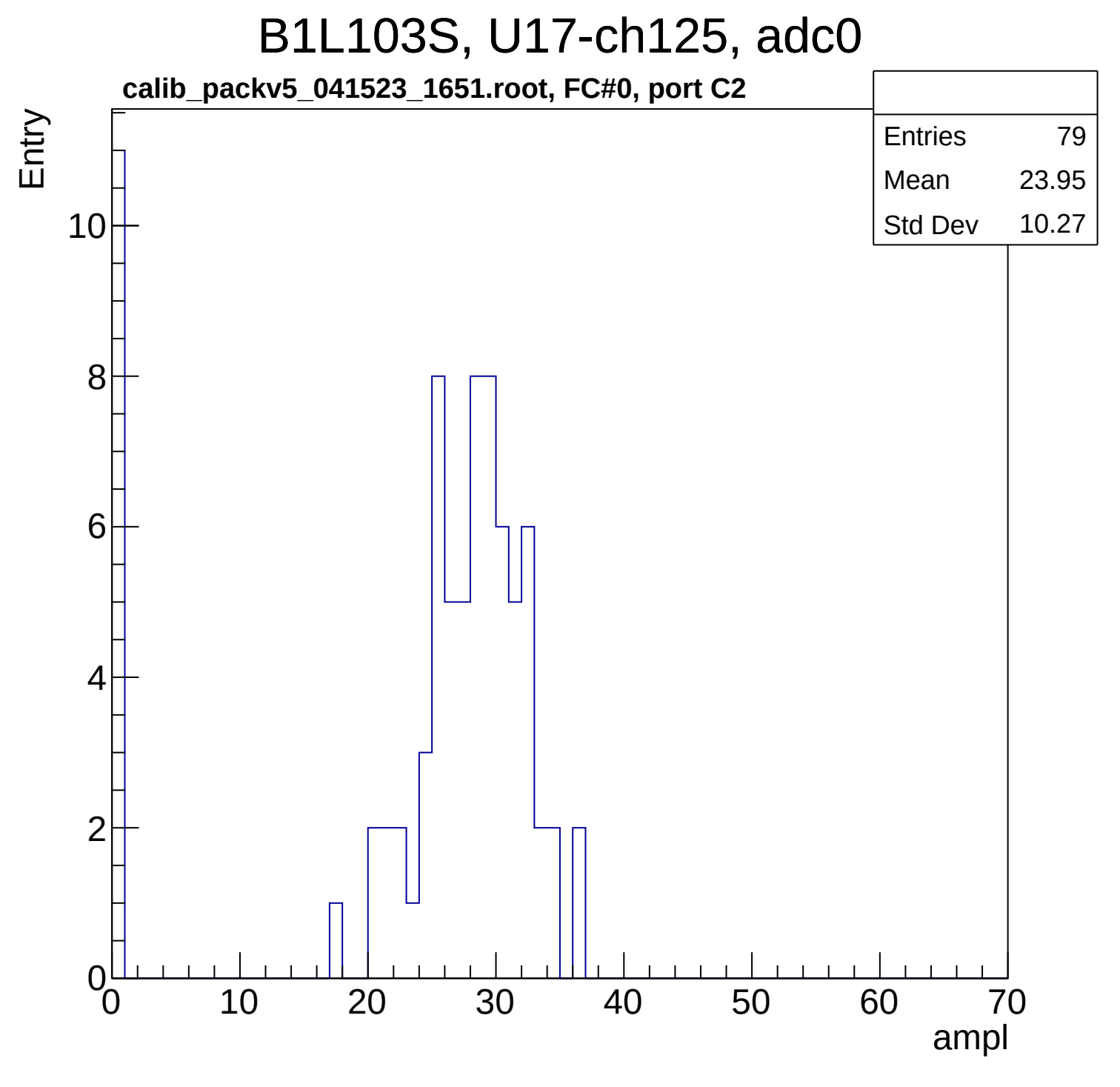
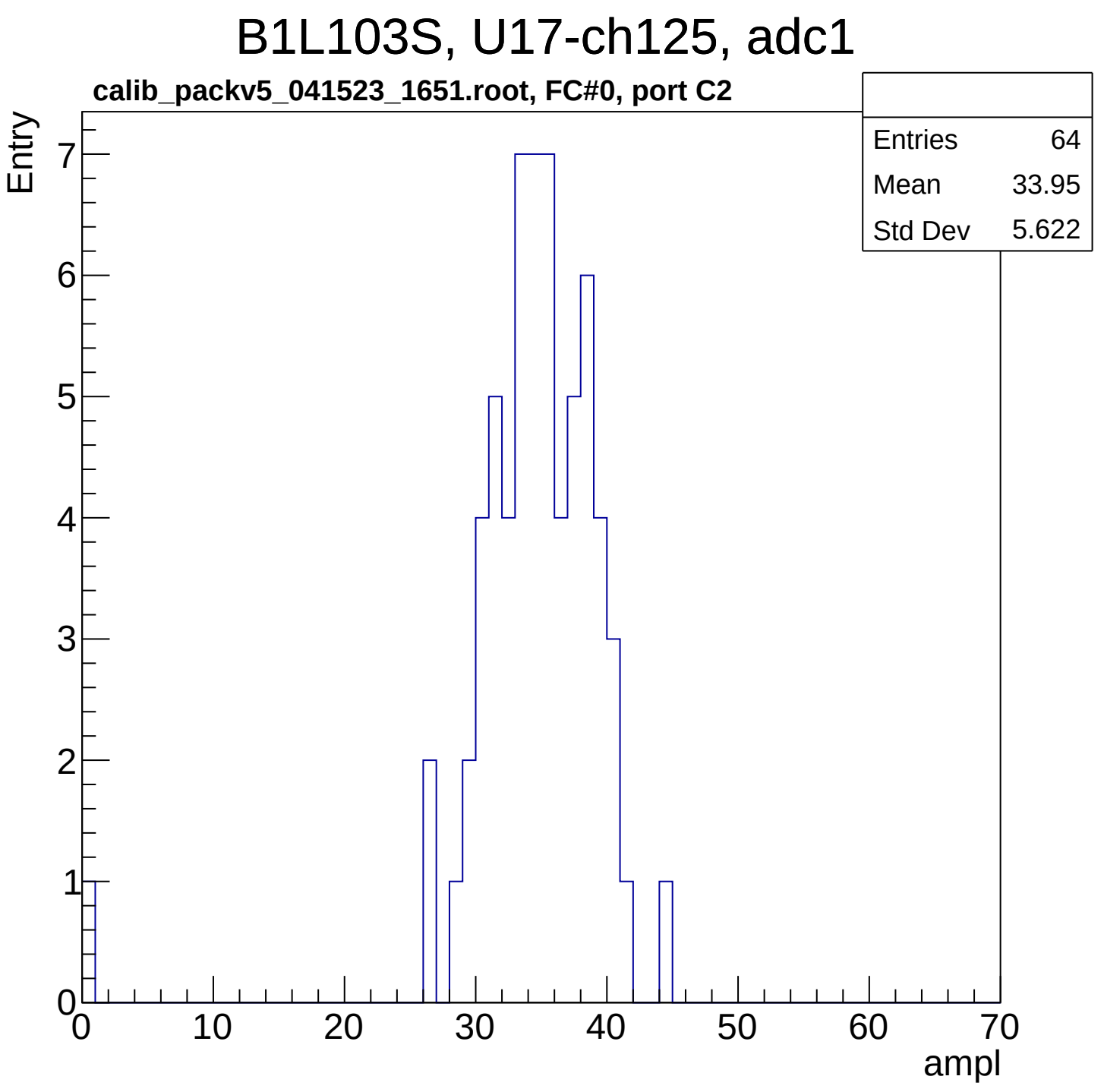
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch125, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 23.95
Std Dev 10.27
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch125, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 33.95
Std Dev 5.622
Entry
ampl
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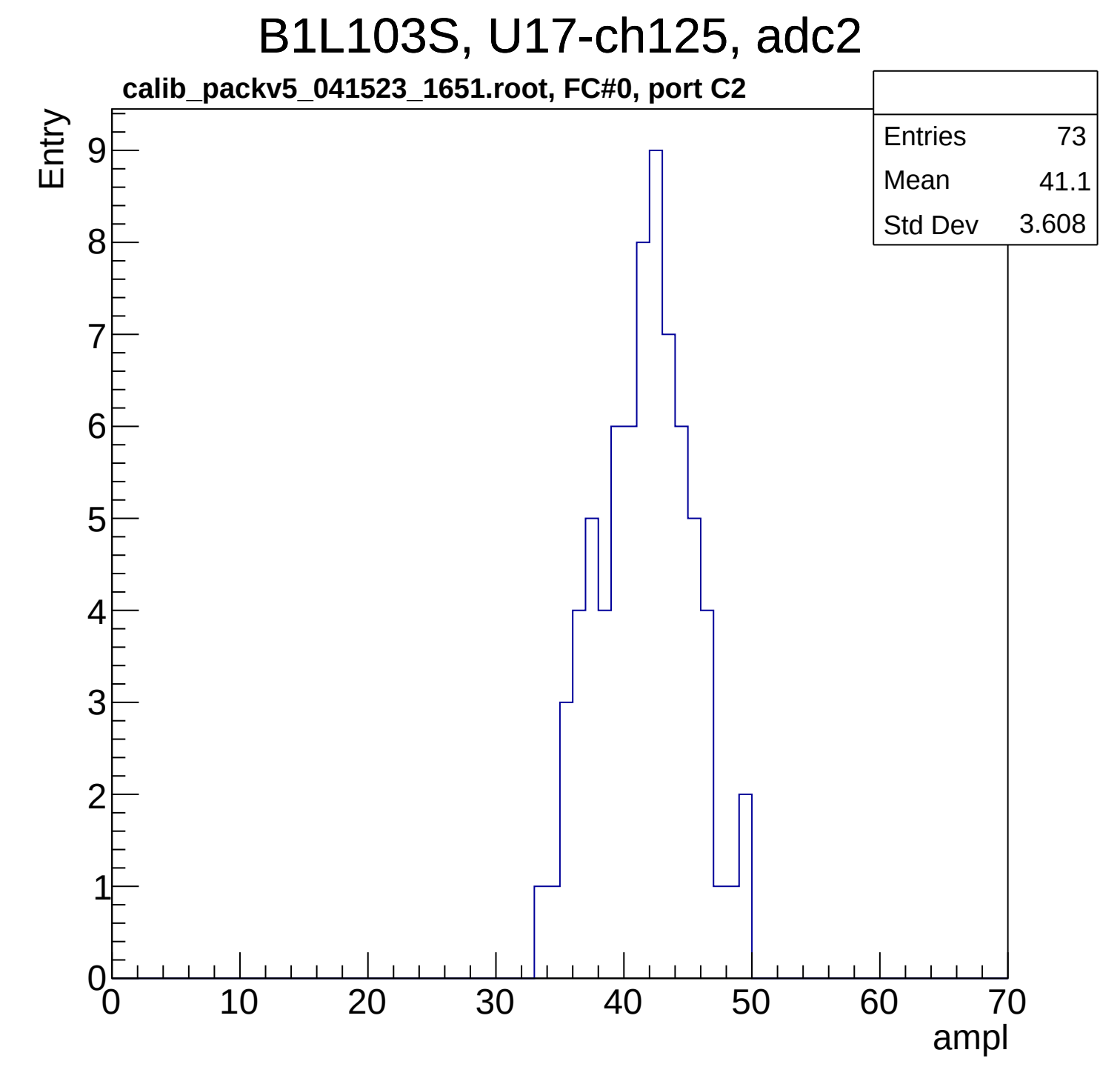
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U17-ch125, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 41.1
Std Dev 3.608
Entry
ampl
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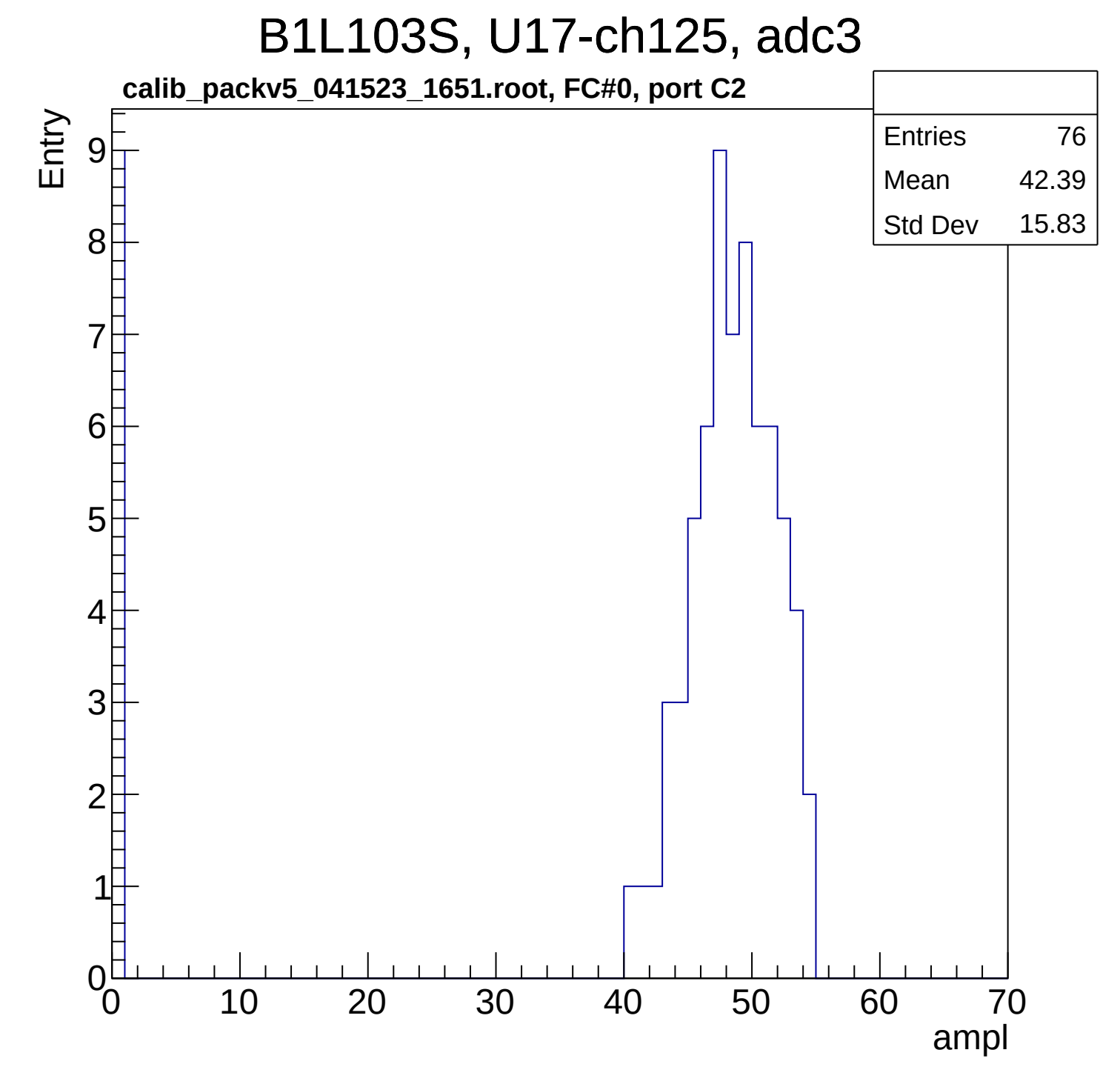
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U17-ch125, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 42.39
Std Dev 15.83
Entry
ampl
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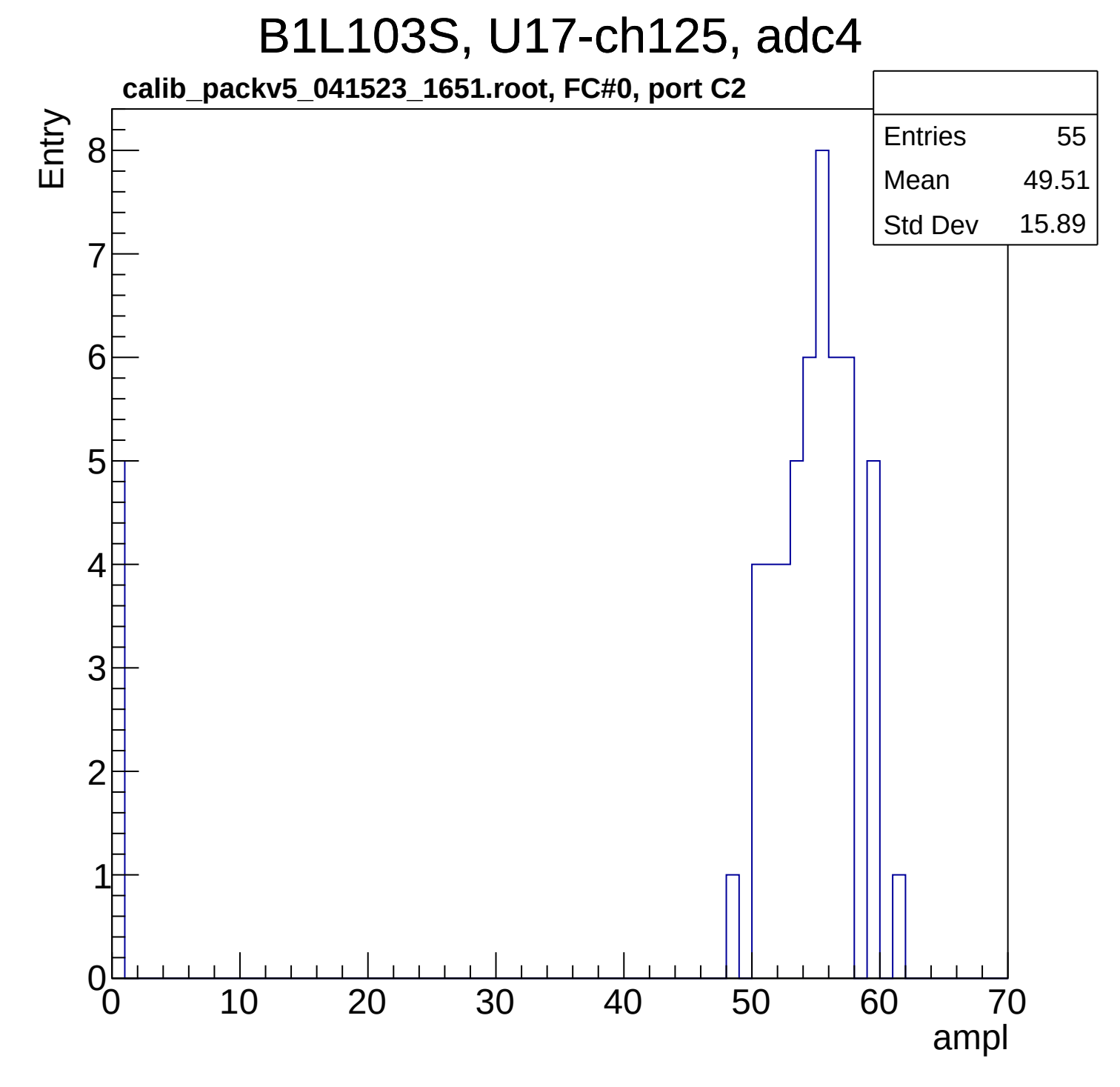
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U17-ch125, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 49.51
Std Dev 15.89
Entry
ampl
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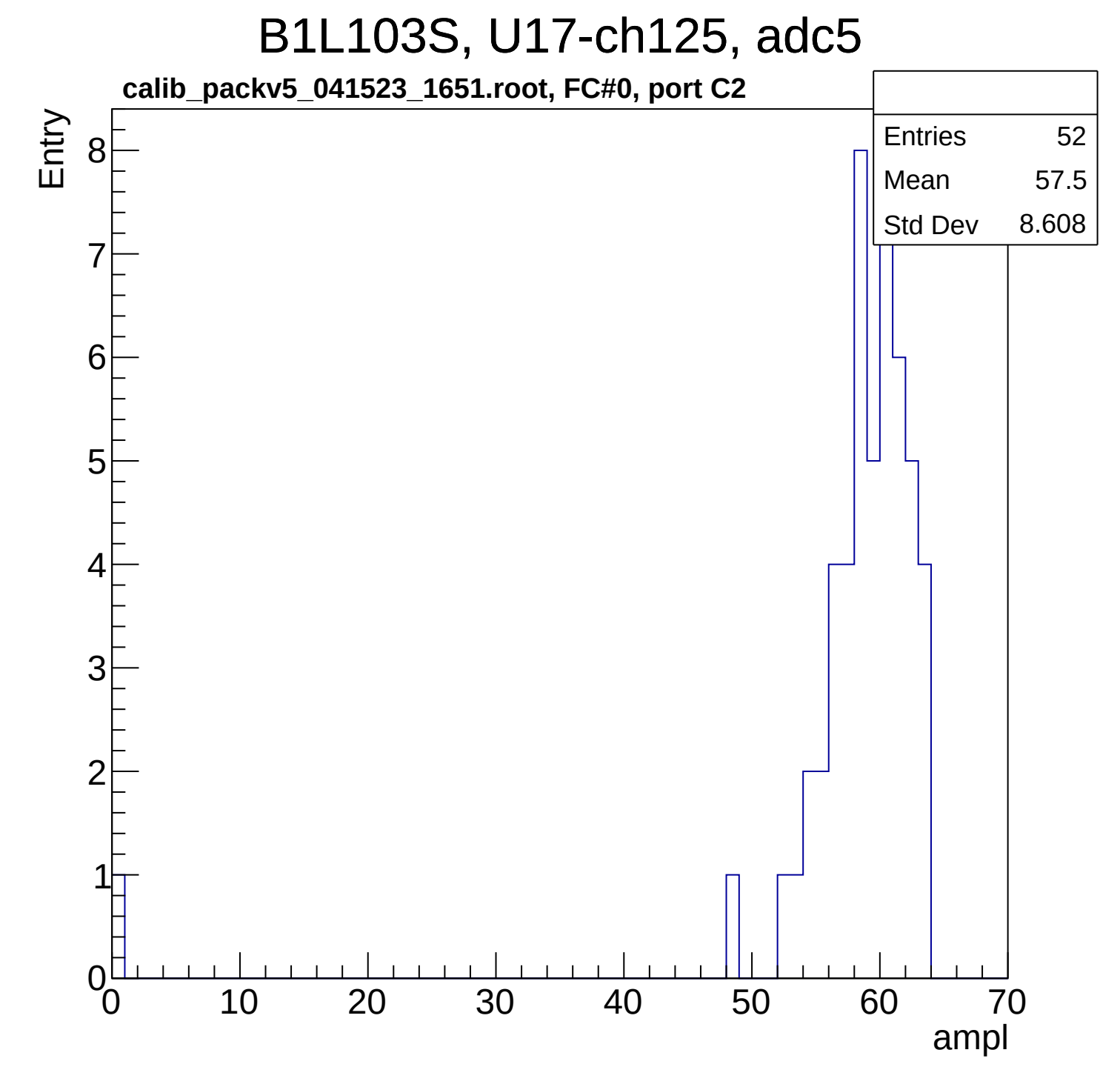
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U17-ch125, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 57.5
Std Dev 8.608
Entry
ampl
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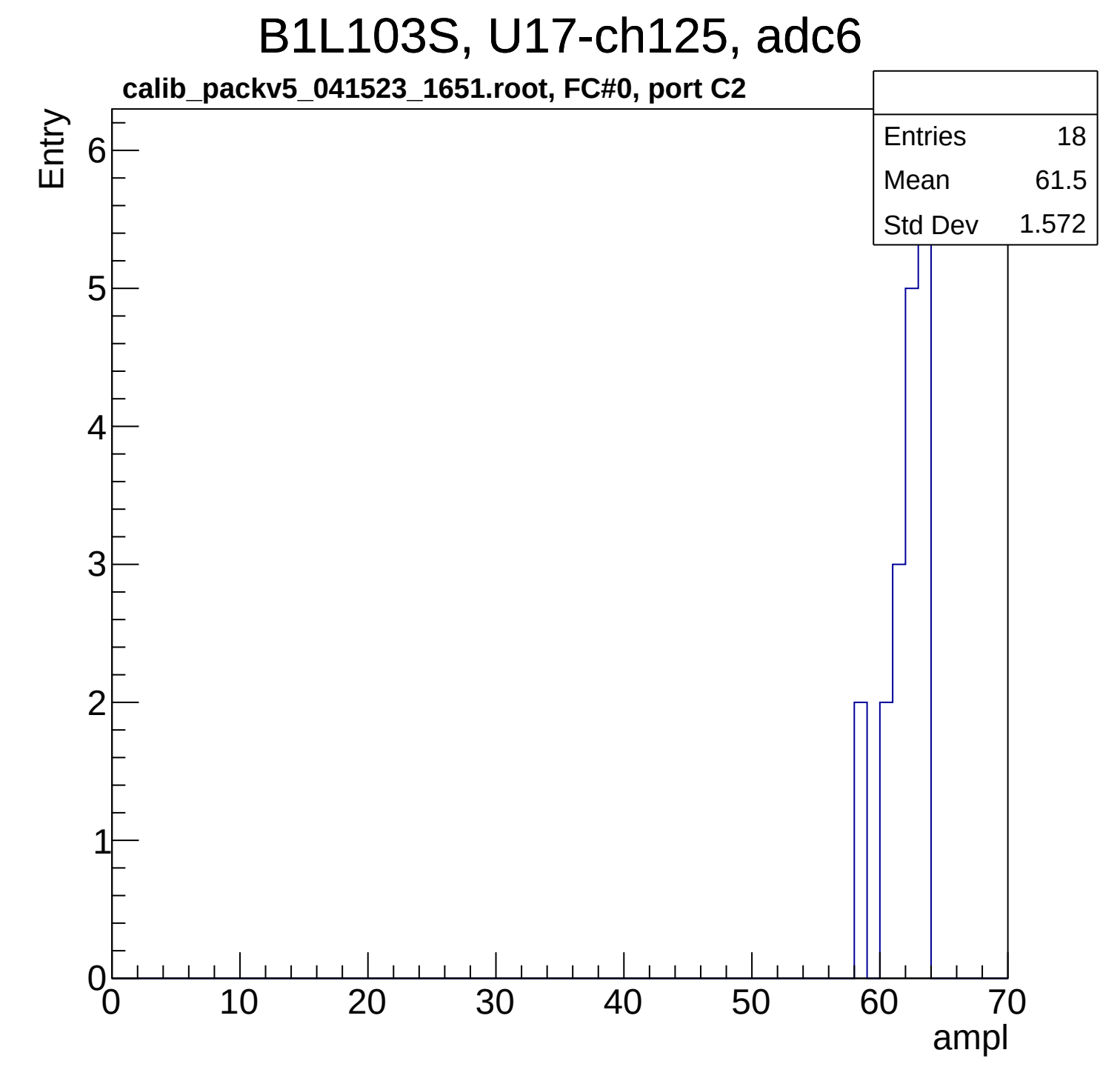
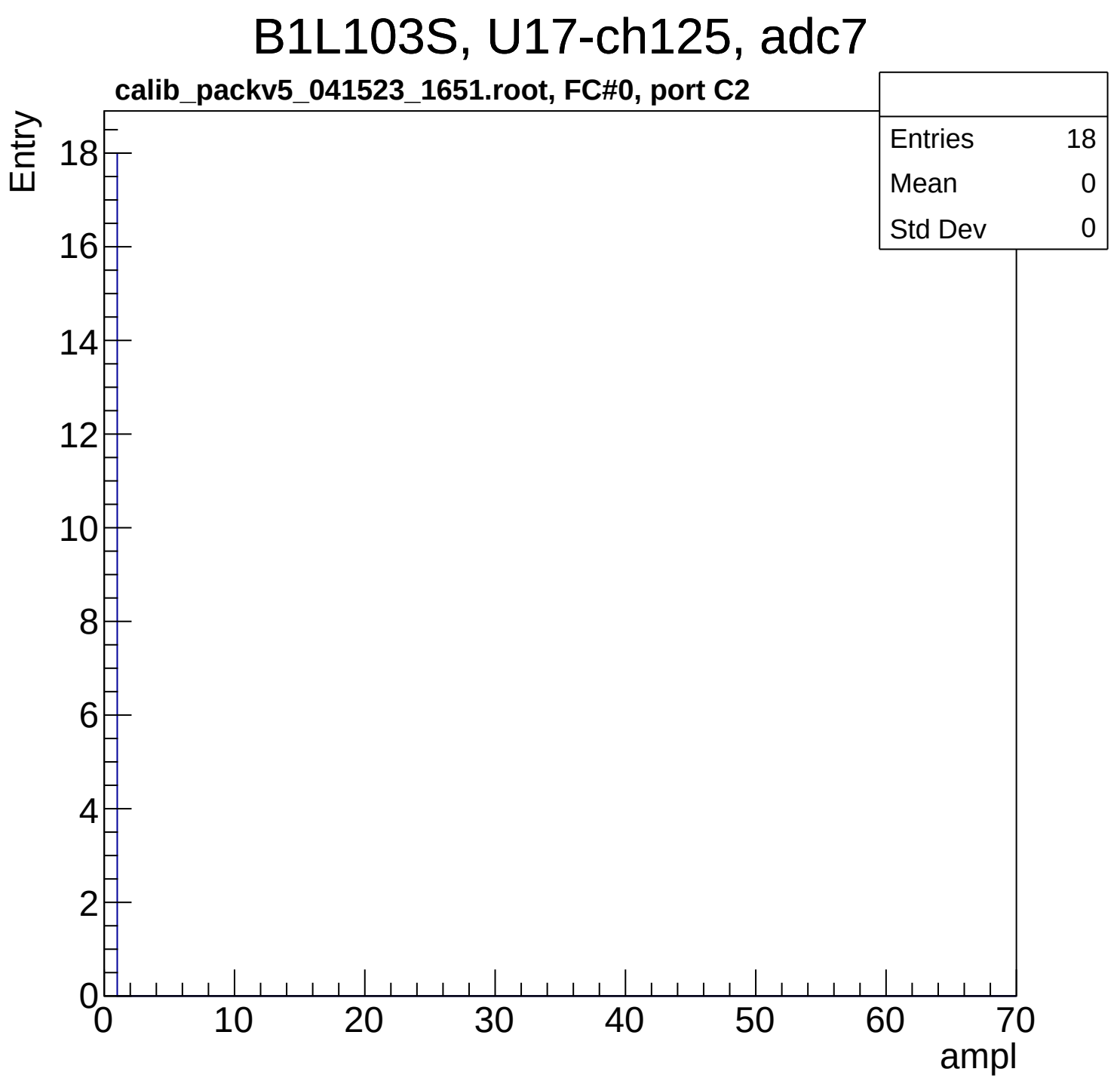
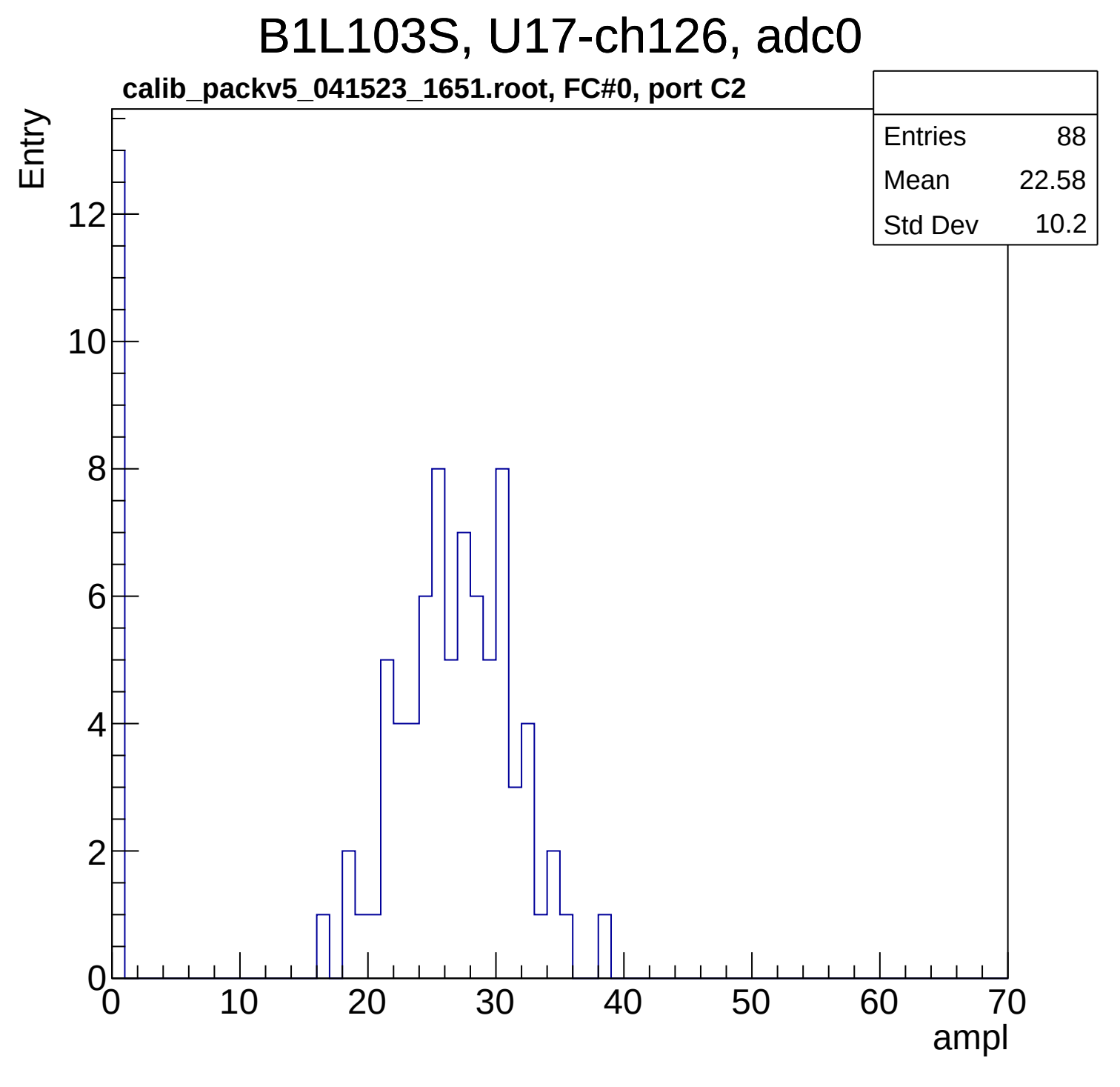
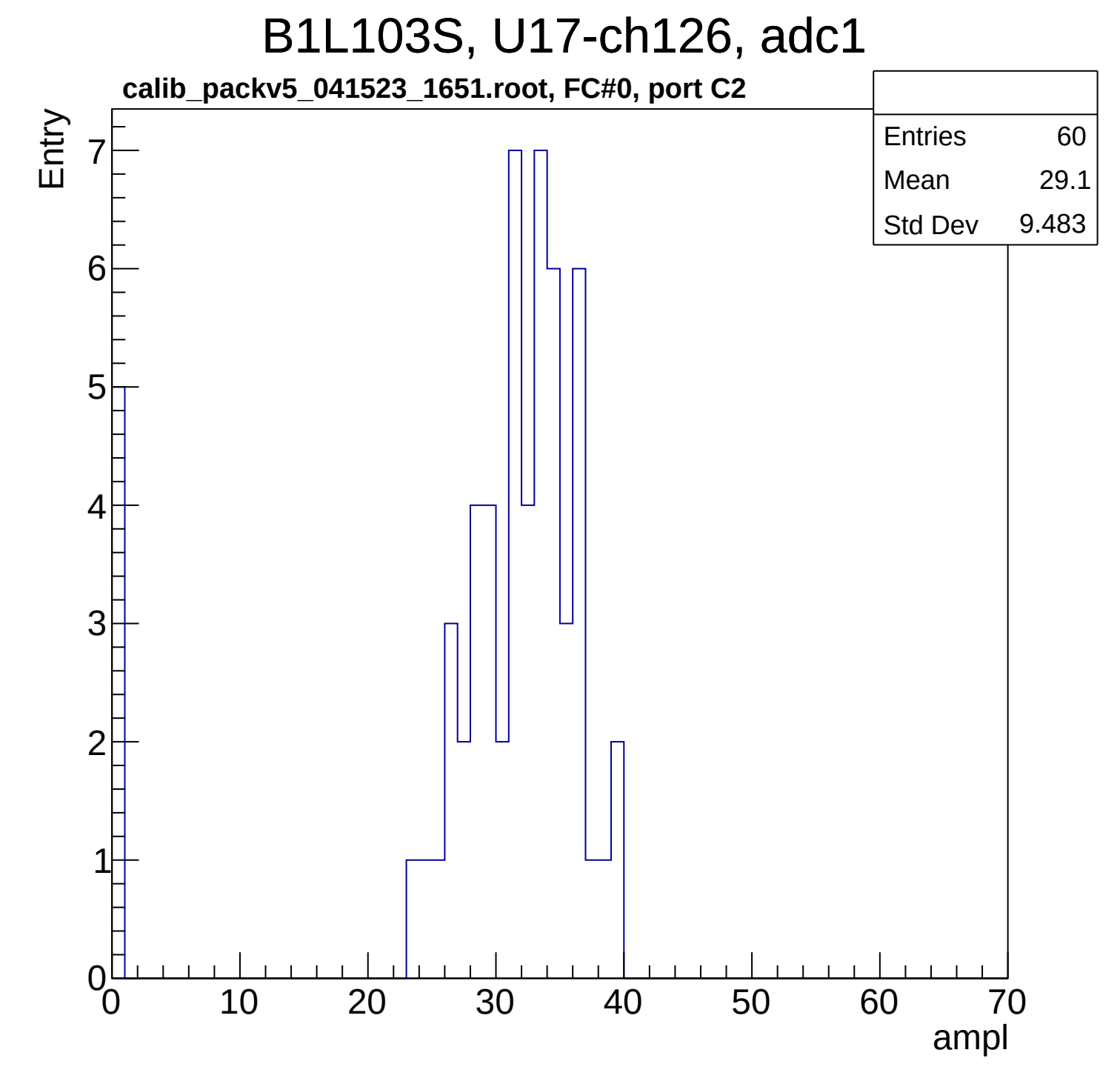
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U17-ch125, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 61.5
Std Dev 1.572
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch125, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch126, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 88
Mean 22.58
Std Dev 10.2
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch126, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 29.1
Std Dev 9.483
Entry
ampl
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1
2
3
4
5
6
7
0
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20
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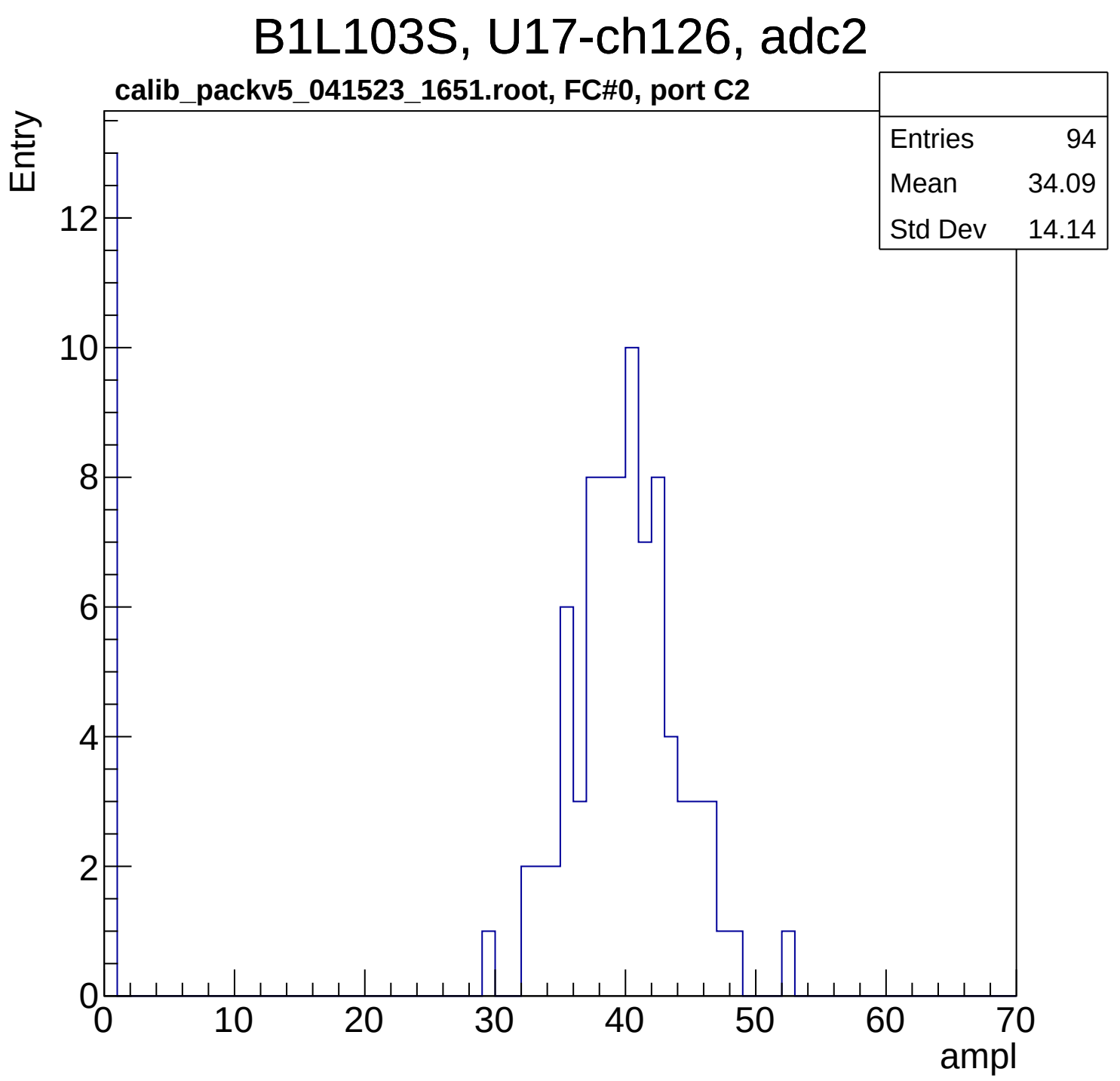
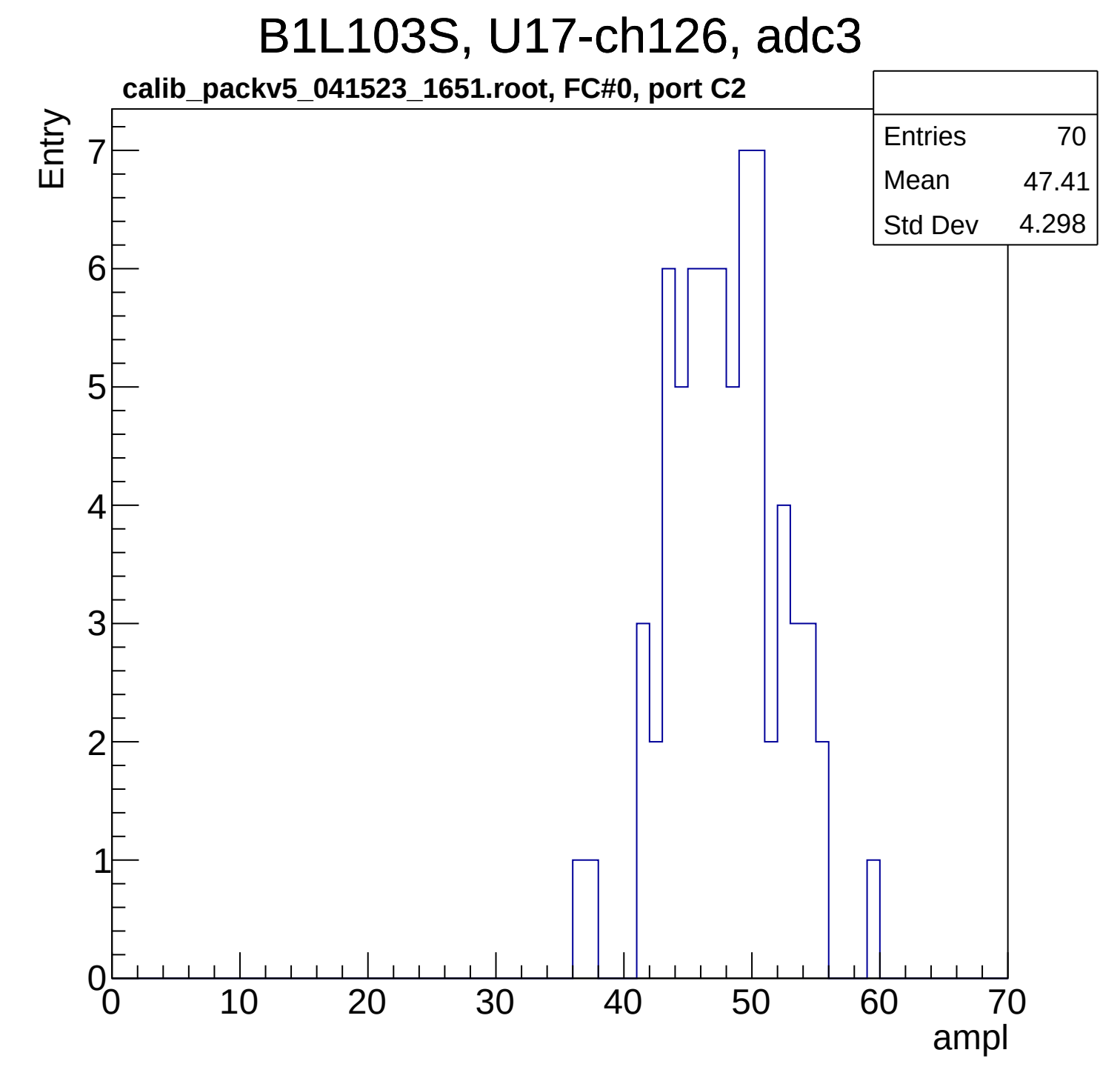
40
50
60
70


B1L103S, U17-ch126, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 94
Mean 34.09
Std Dev 14.14
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch126, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 47.41
Std Dev 4.298
Entry
ampl
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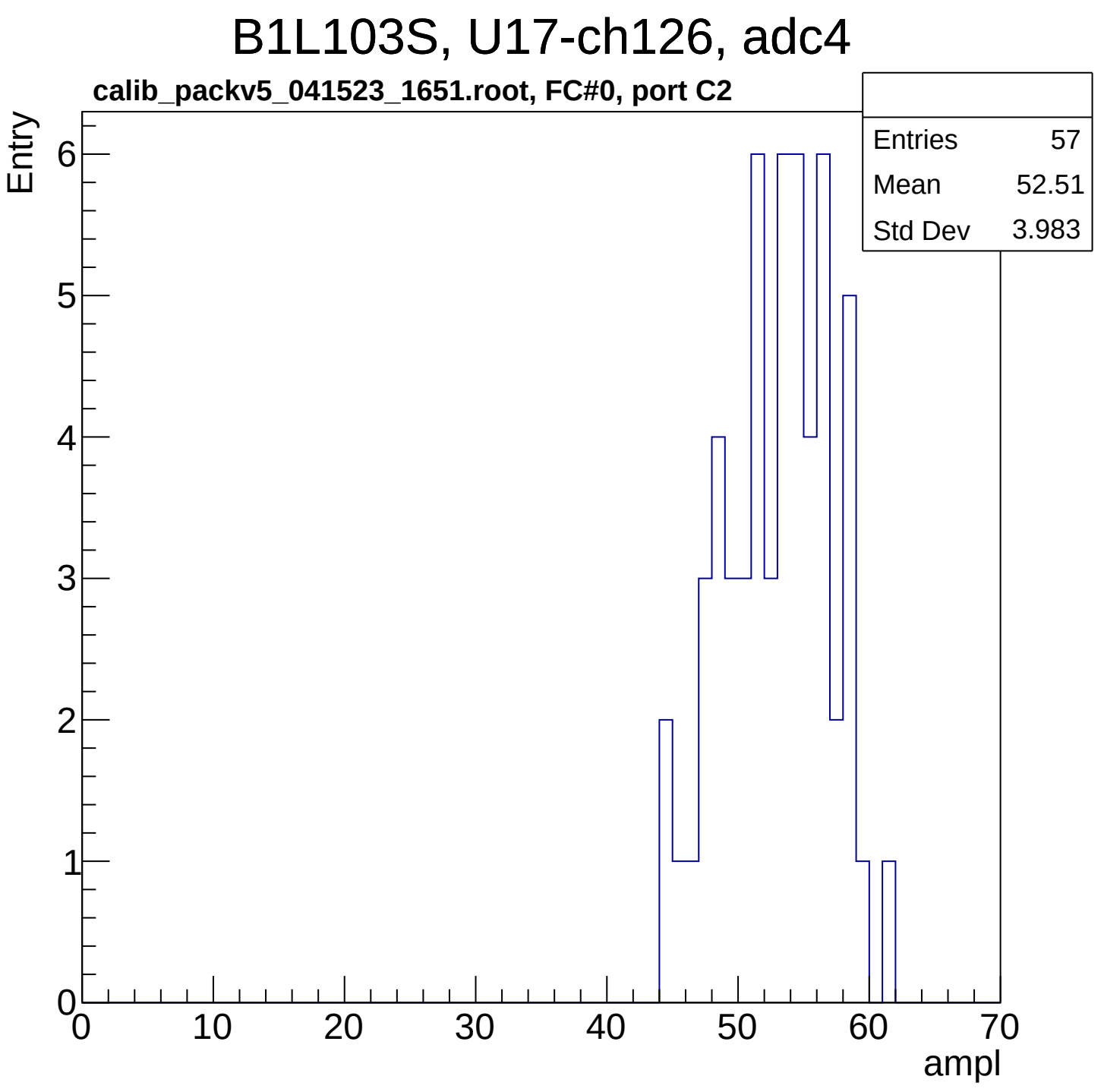
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U17-ch126, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 52.51
Std Dev 3.983
Entry
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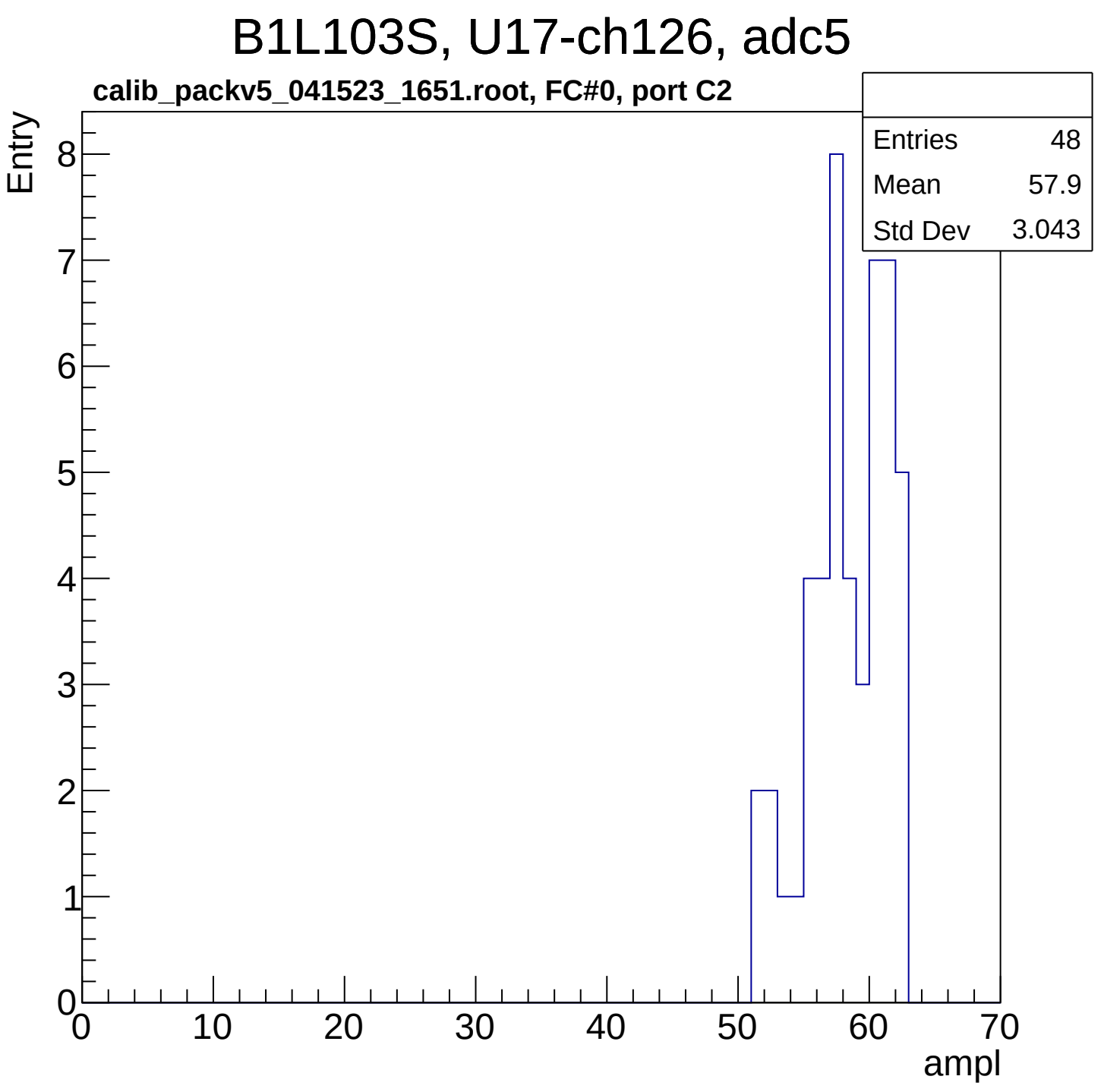
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U17-ch126, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 57.9
Std Dev 3.043
Entry
ampl
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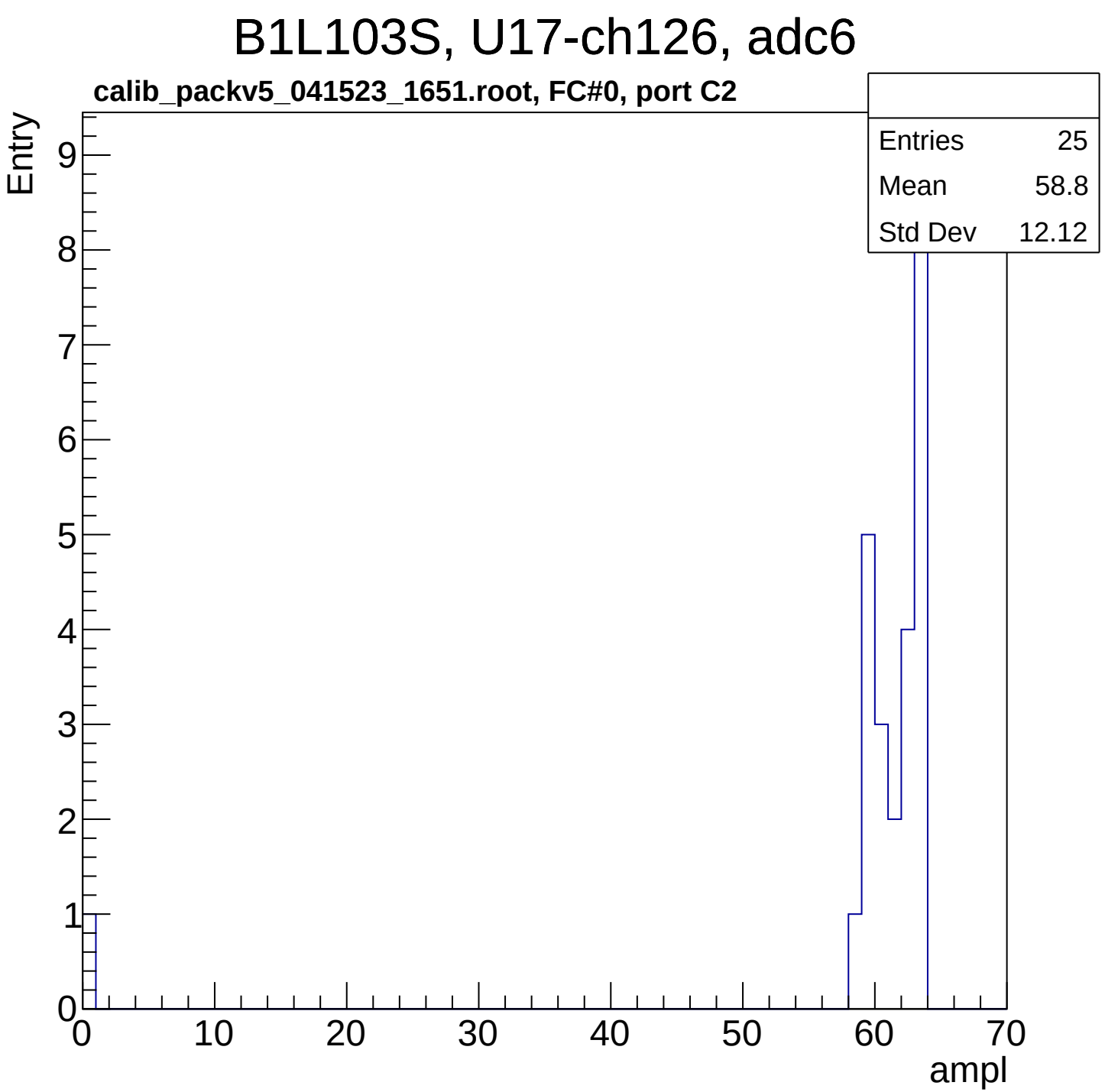
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U17-ch126, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 25
Mean 58.8
Std Dev 12.12
Entry
ampl
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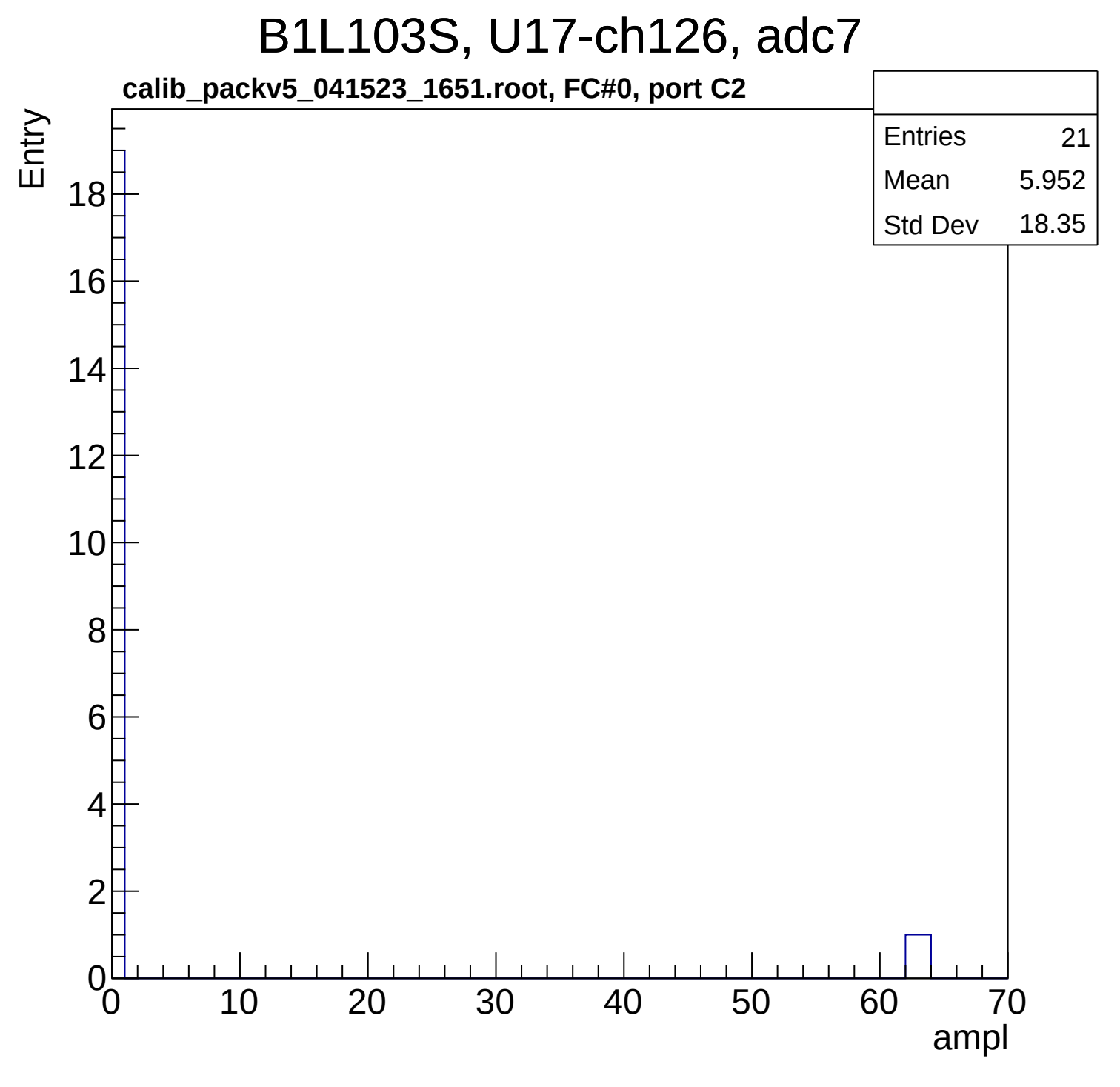
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U17-ch126, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 5.952
Std Dev 18.35
Entry
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6
8
10
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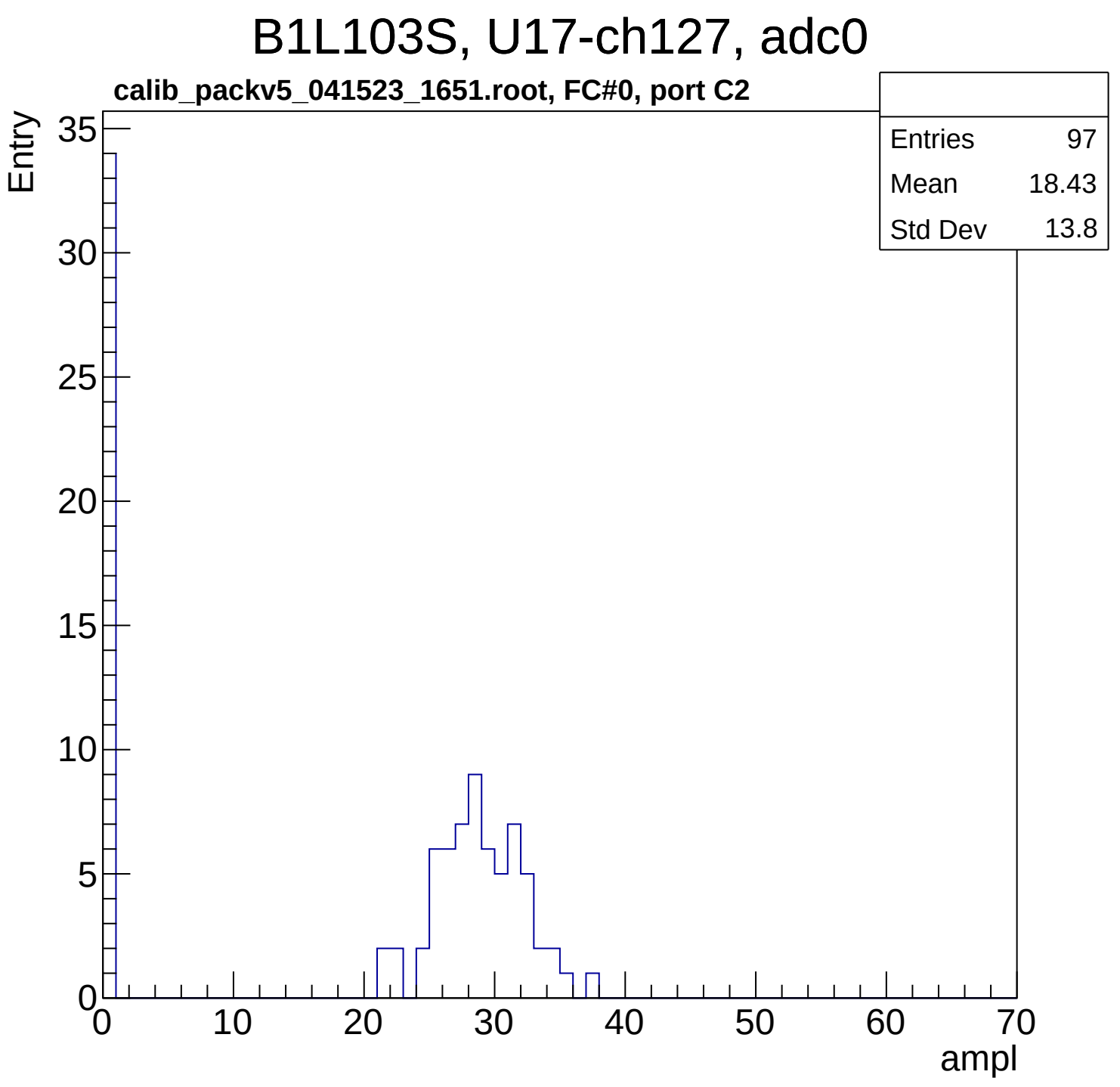
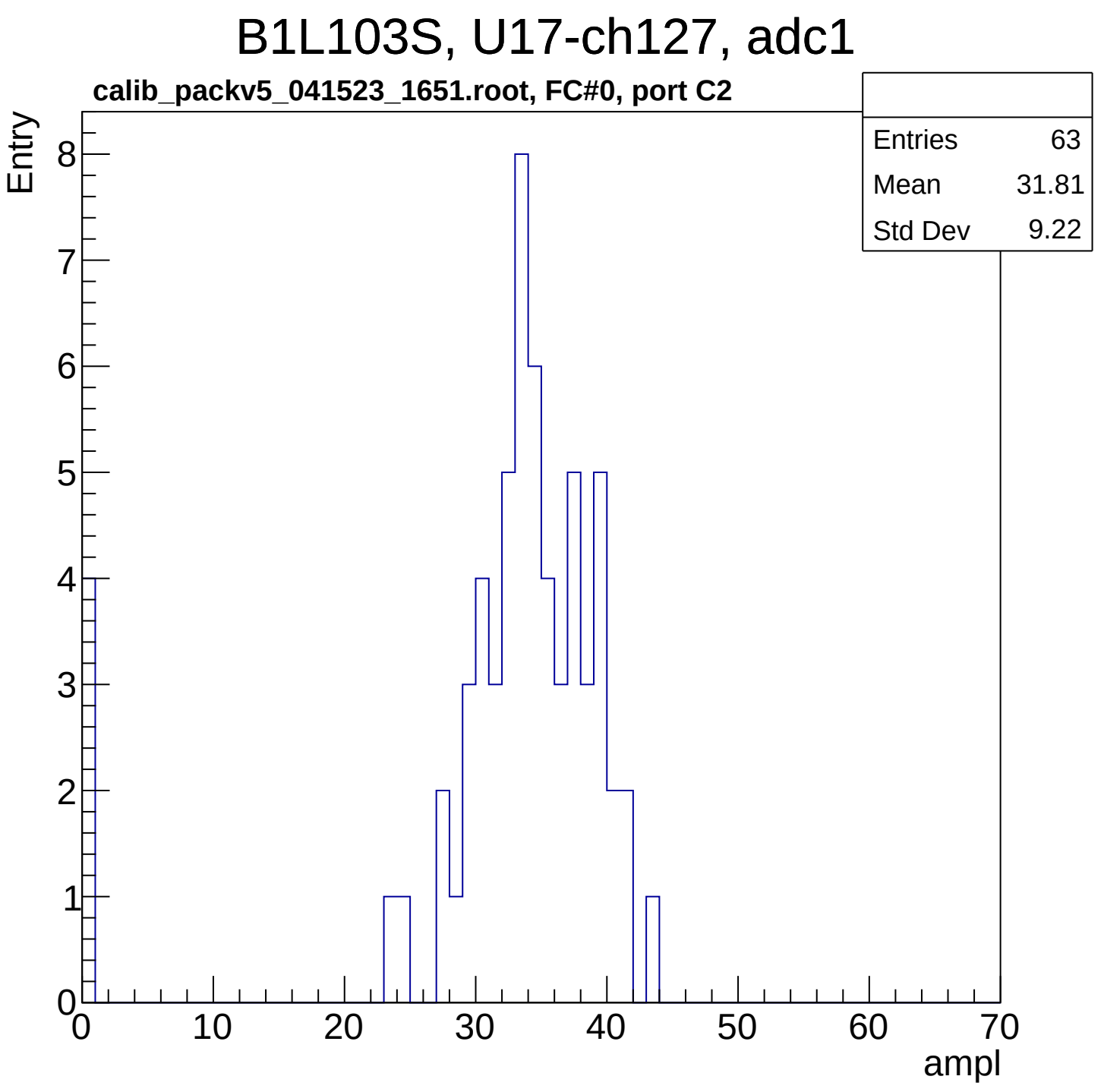
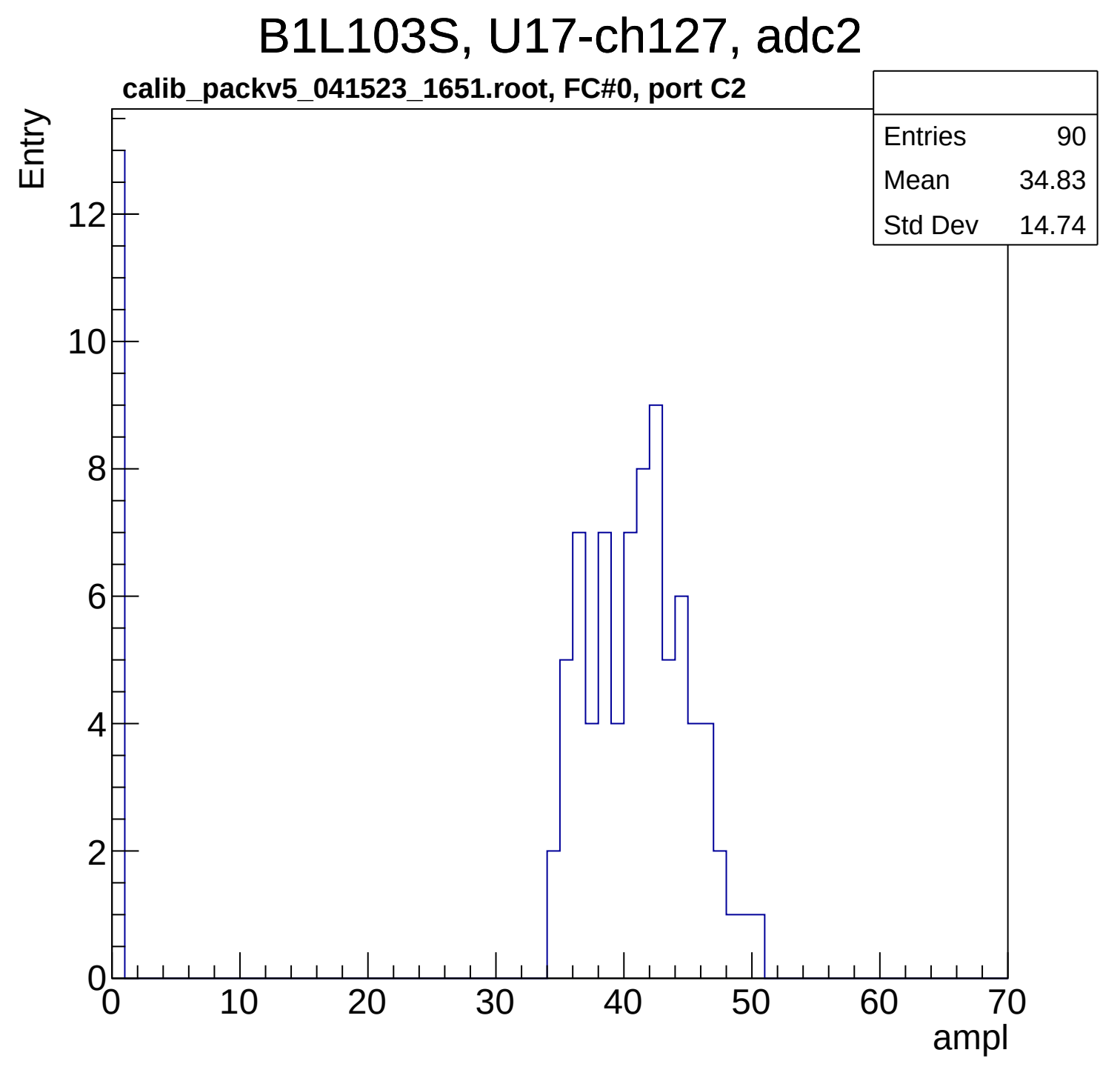
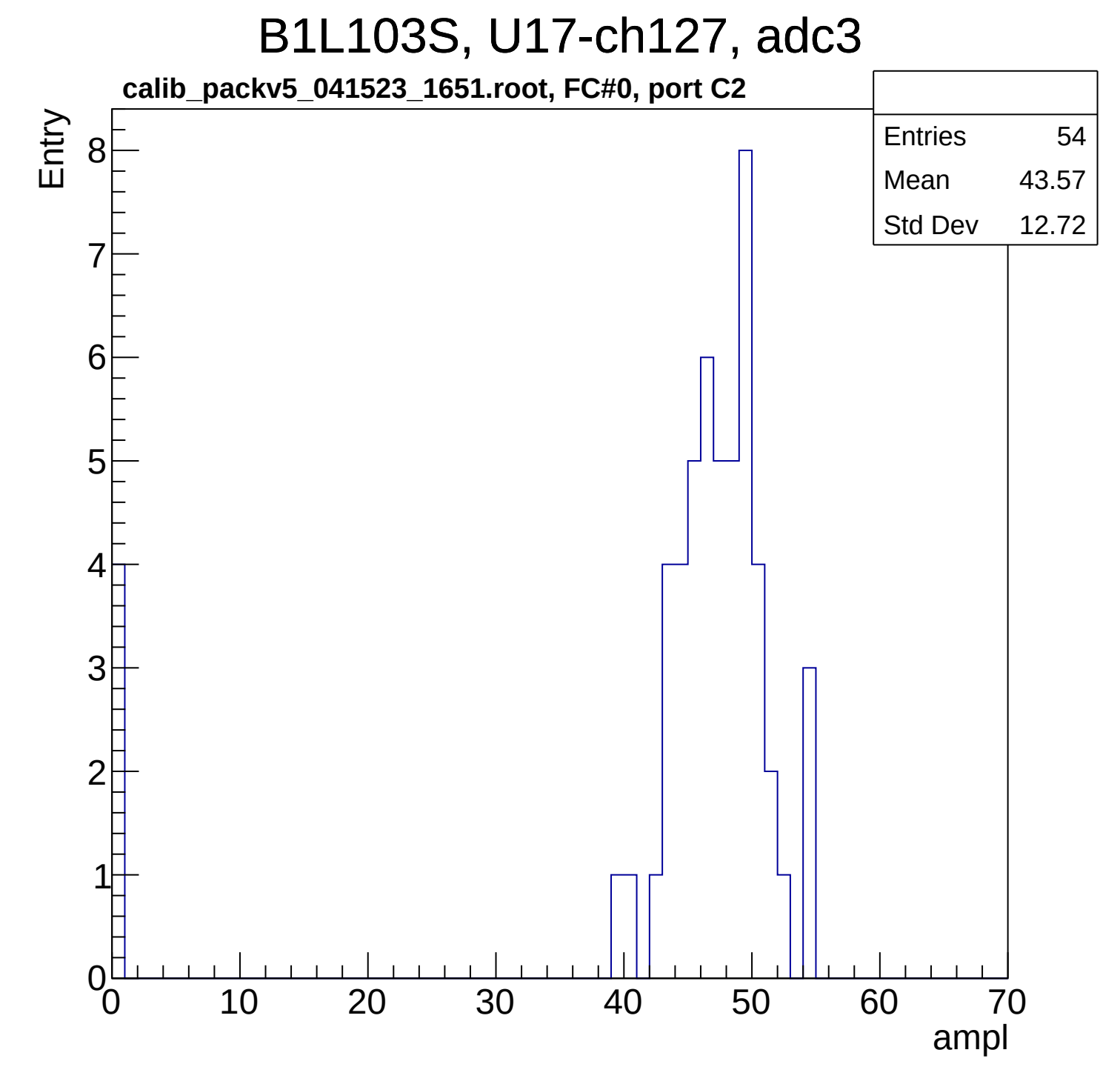
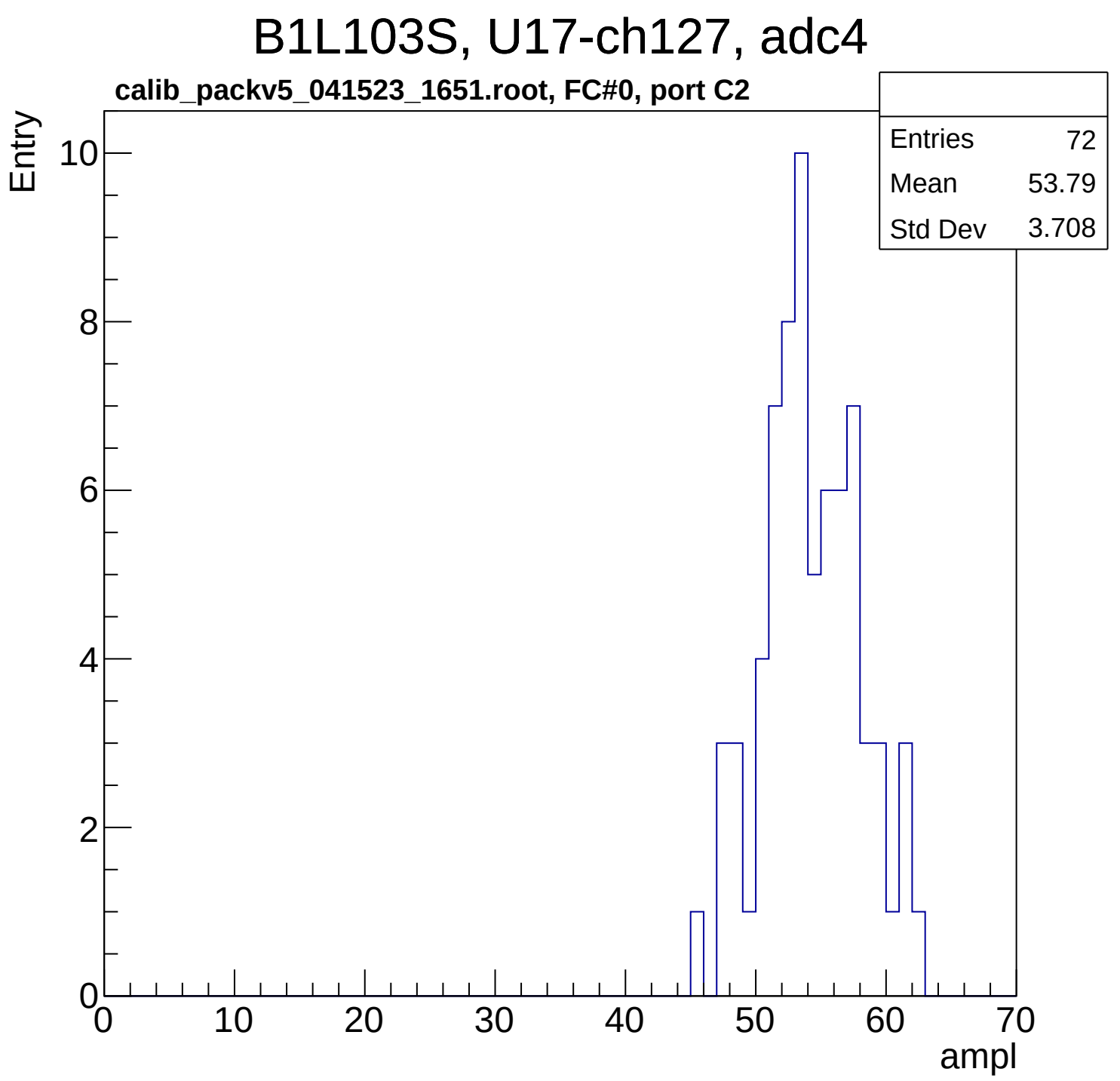
14
16
18
0
10
20
30
40
50
60
70
ampl

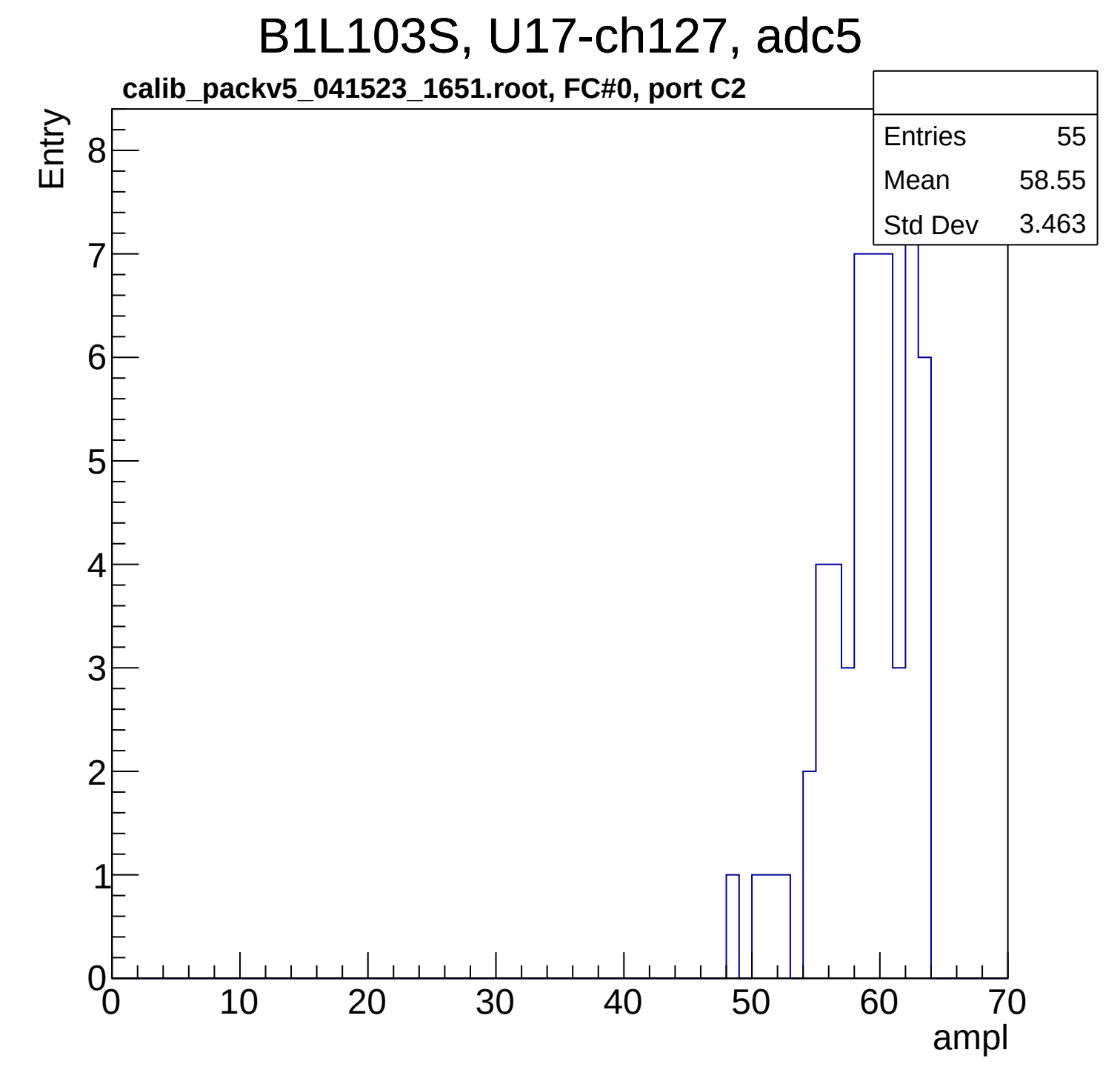

B1L103S, U17-ch127, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 97
Mean 18.43
Std Dev 13.8
Entry
0
5
10
15
20
25
30
35
0
10
20
30
40
50
60
70
ampl

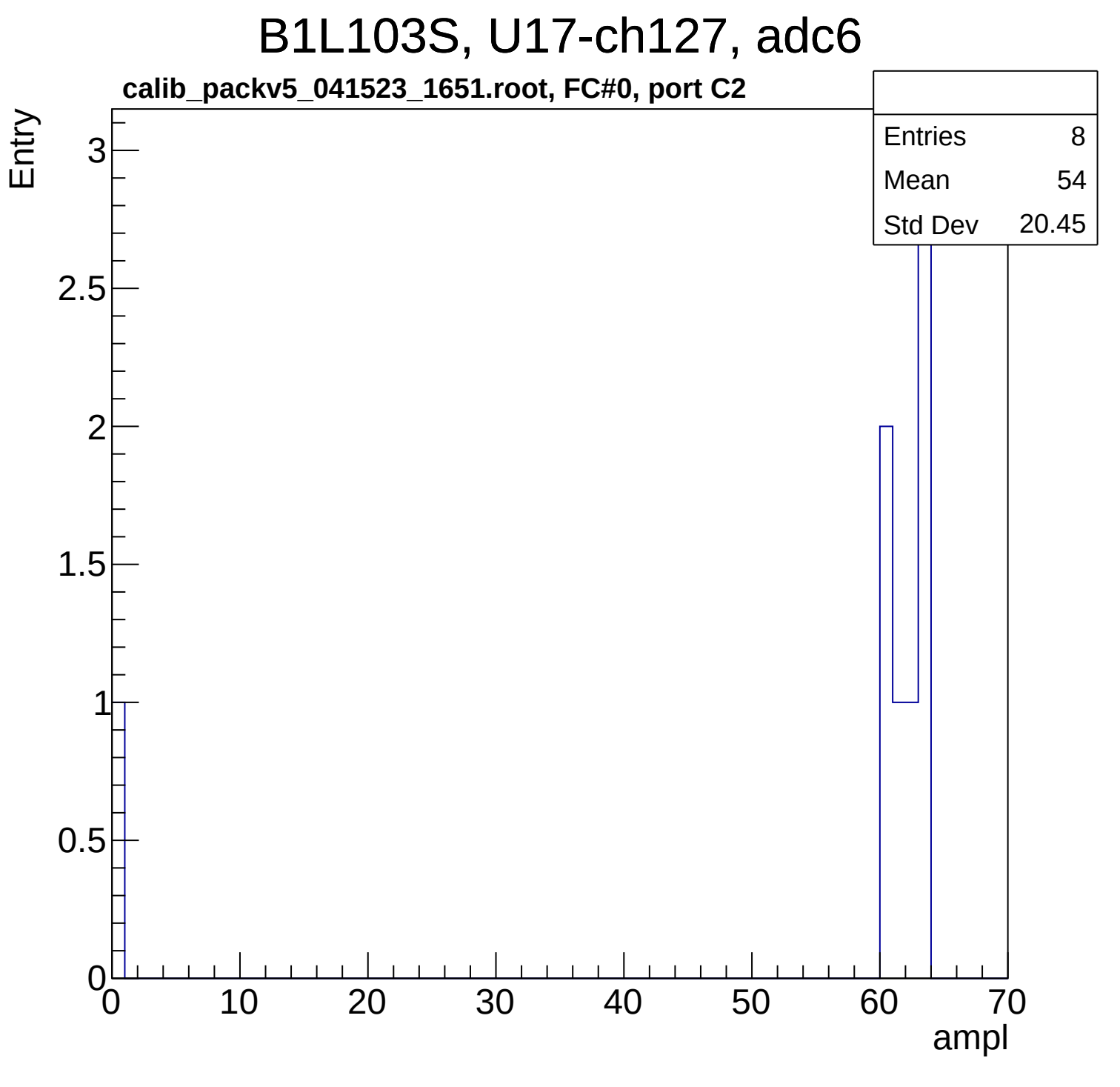

B1L103S, U17-ch127, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 31.81
Std Dev 9.22
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

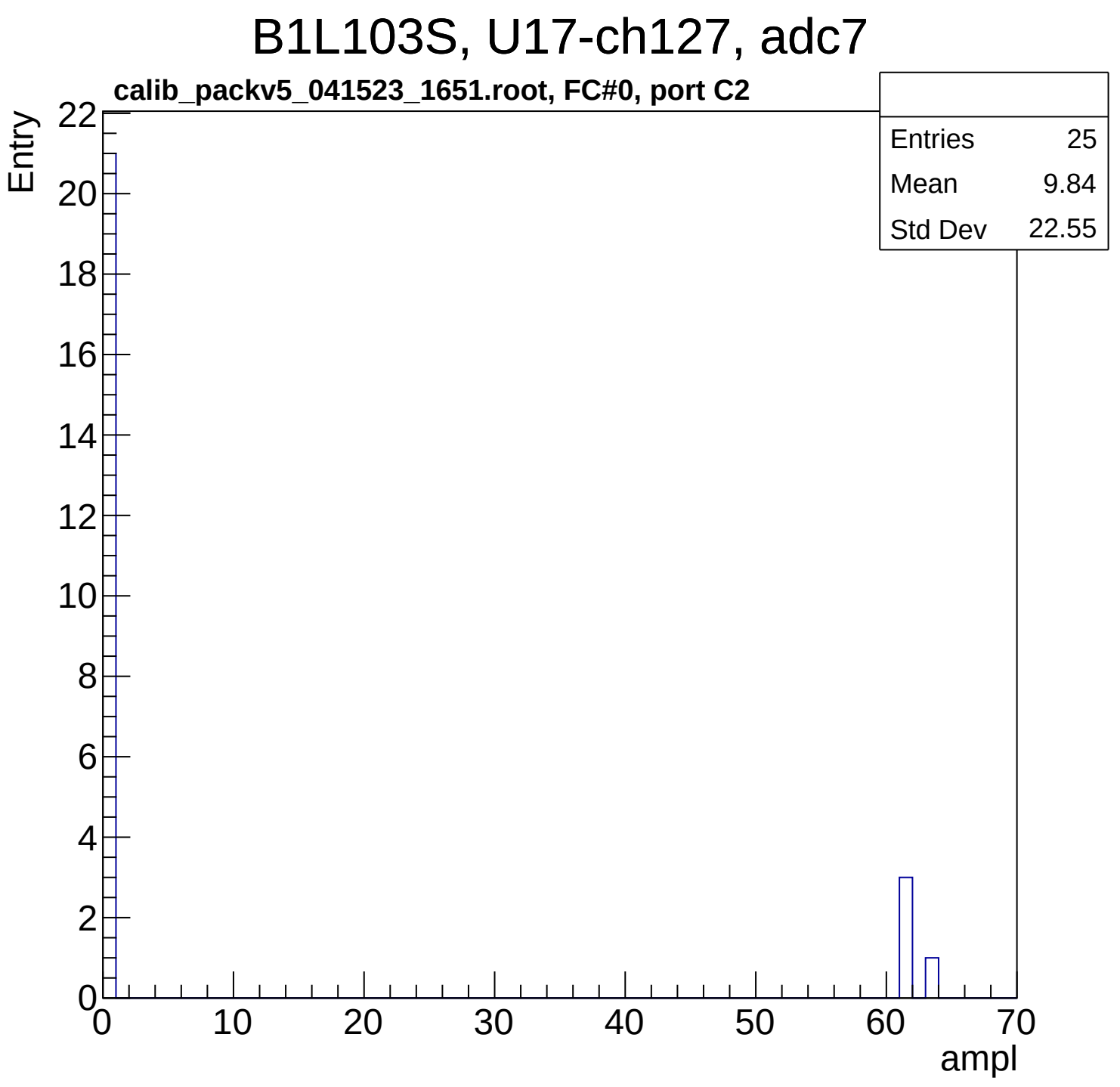

B1L103S, U17-ch127, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 90
Mean 34.83
Std Dev 14.74
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl

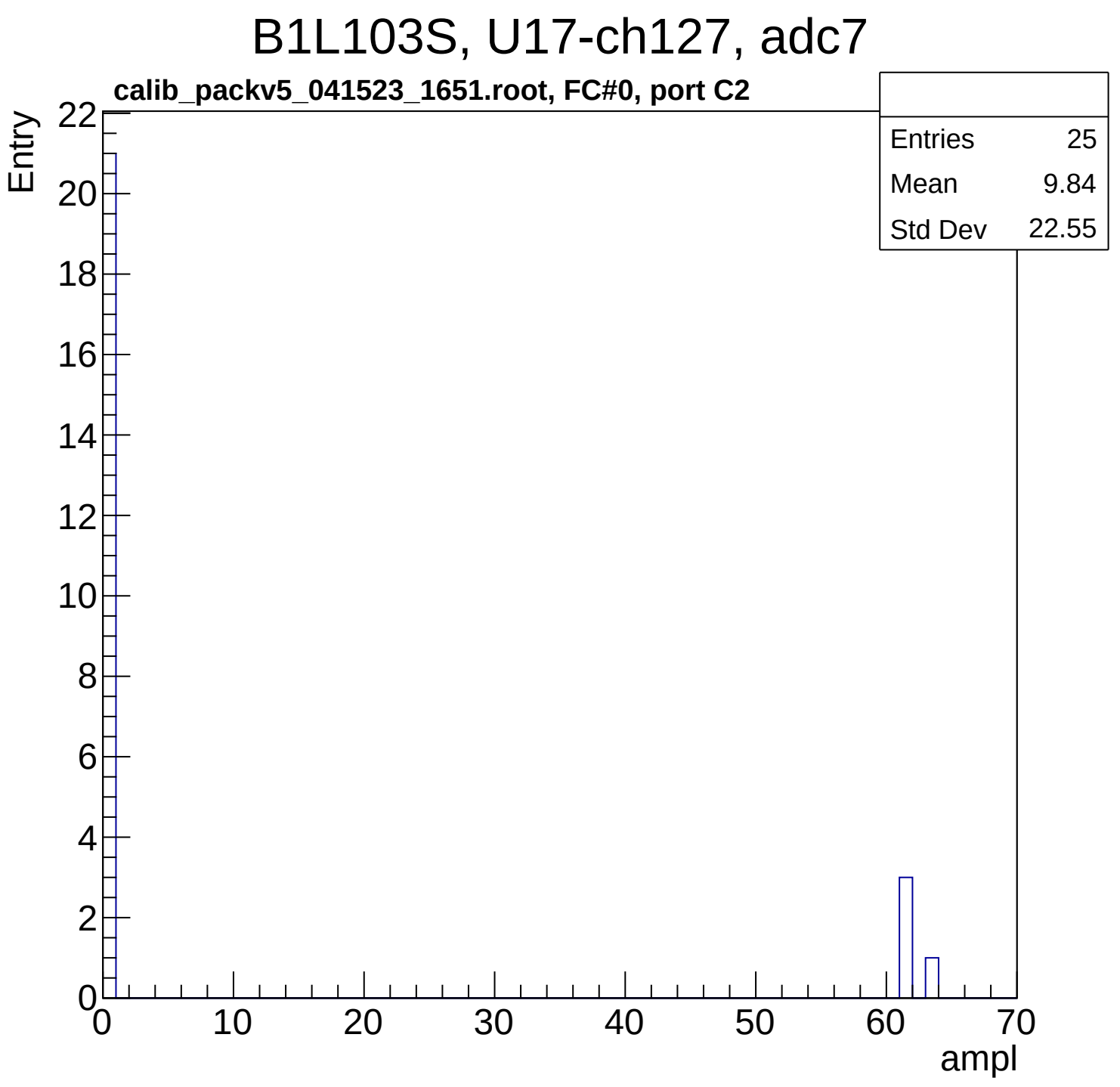

B1L103S, U17-ch127, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 43.57
Std Dev 12.72
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U17-ch127, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 53.79
Std Dev 3.708
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U17-ch127, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 58.55
Std Dev 3.463
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U17-ch127, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 54
Std Dev 20.45
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U17-ch127, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 25
Mean 9.84
Std Dev 22.55
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
22
0
10
20
30
40
50
60
70


B1L103S, U17-ch127, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 25
Mean 9.84
Std Dev 22.55
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
22
0
10
20
30
40
50
60
70