



# B0L001S, U9-ch0

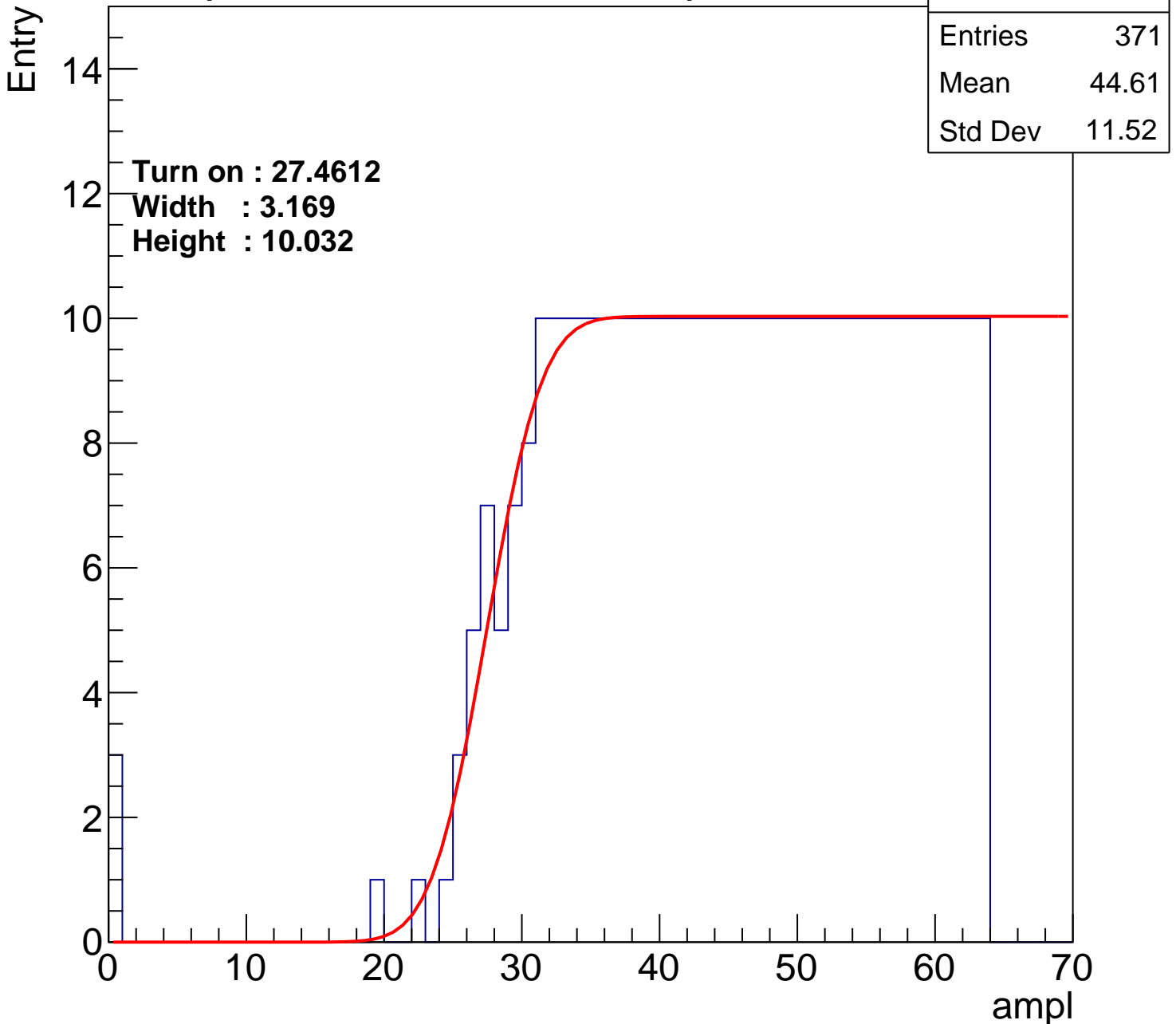
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	371
Mean	44.61
Std Dev	11.52

Turn on : 27.4612

Width : 3.169

Height : 10.032



# B0L001S, U9-ch1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	353
Mean	45.61
Std Dev	10.81

Turn on : 29.9076

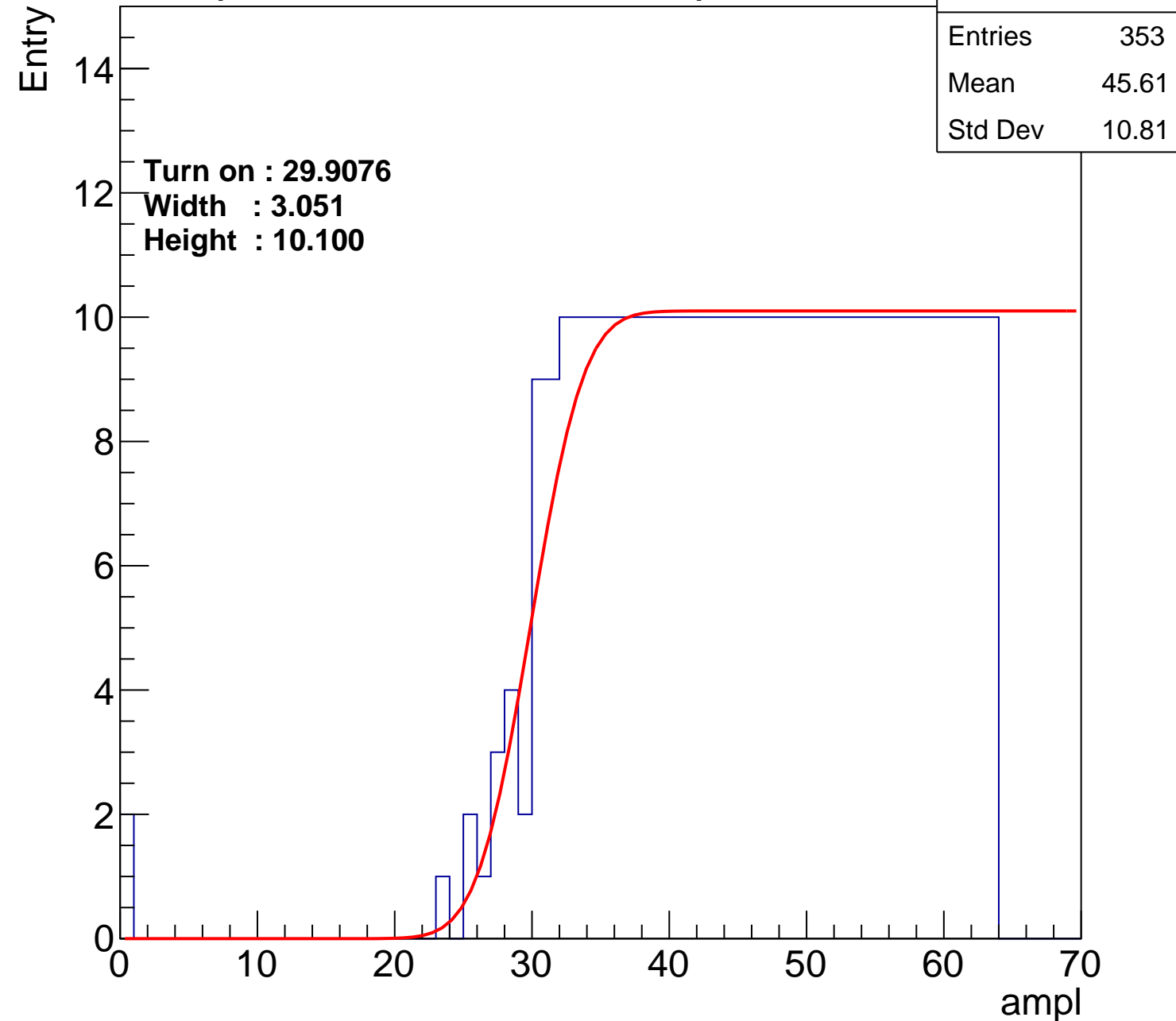
Width : 3.051

Height : 10.100

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U9-ch2

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	352
Mean	45.75
Std Dev	10.52

Turn on : 29.4044

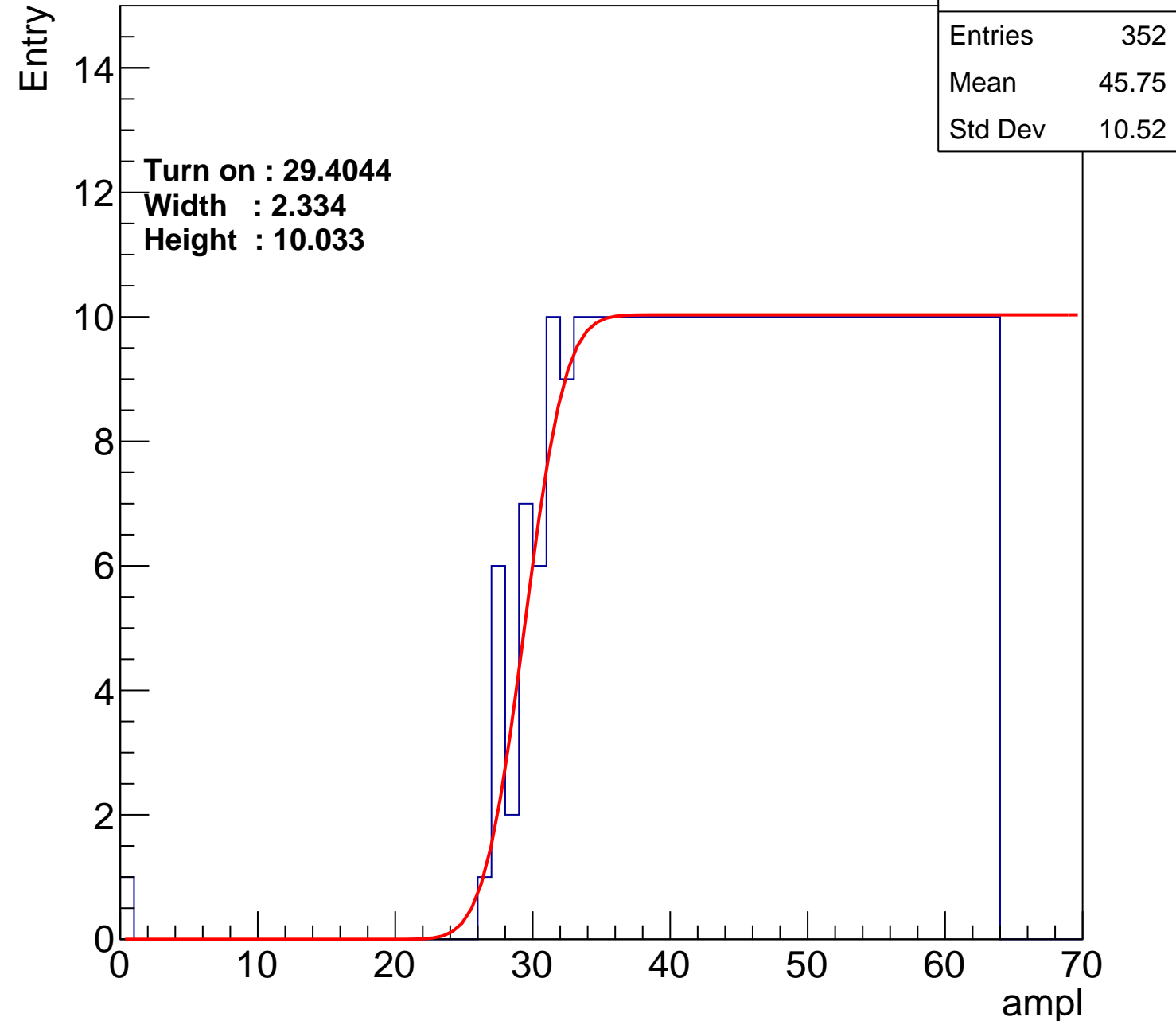
Width : 2.334

Height : 10.033

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U9-ch3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	377
Mean	44.25
Std Dev	11.84

Turn on : 26.7420

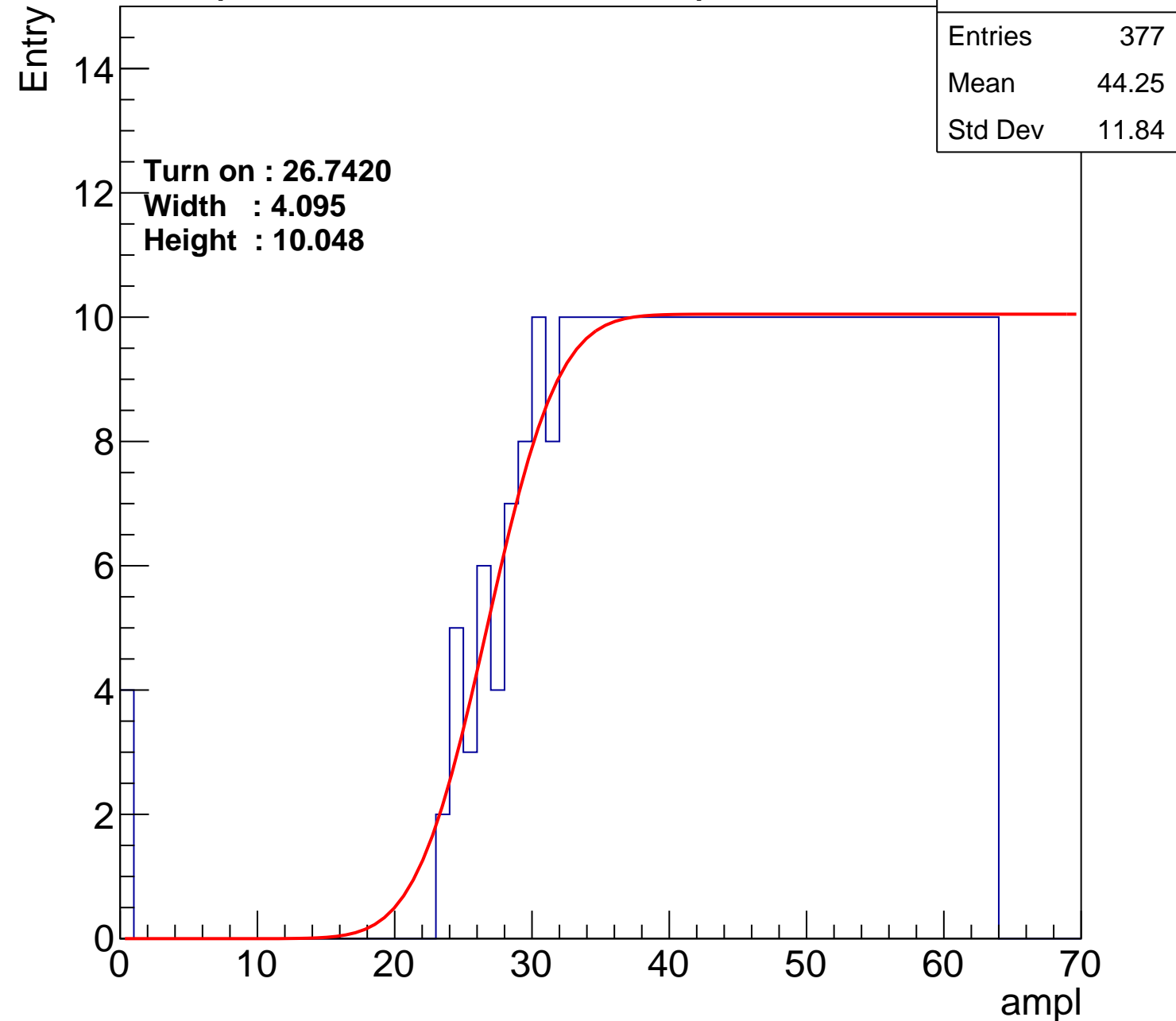
Width : 4.095

Height : 10.048

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U9-ch4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	380
Mean	44.26
Std Dev	11.52

Turn on : 26.4764

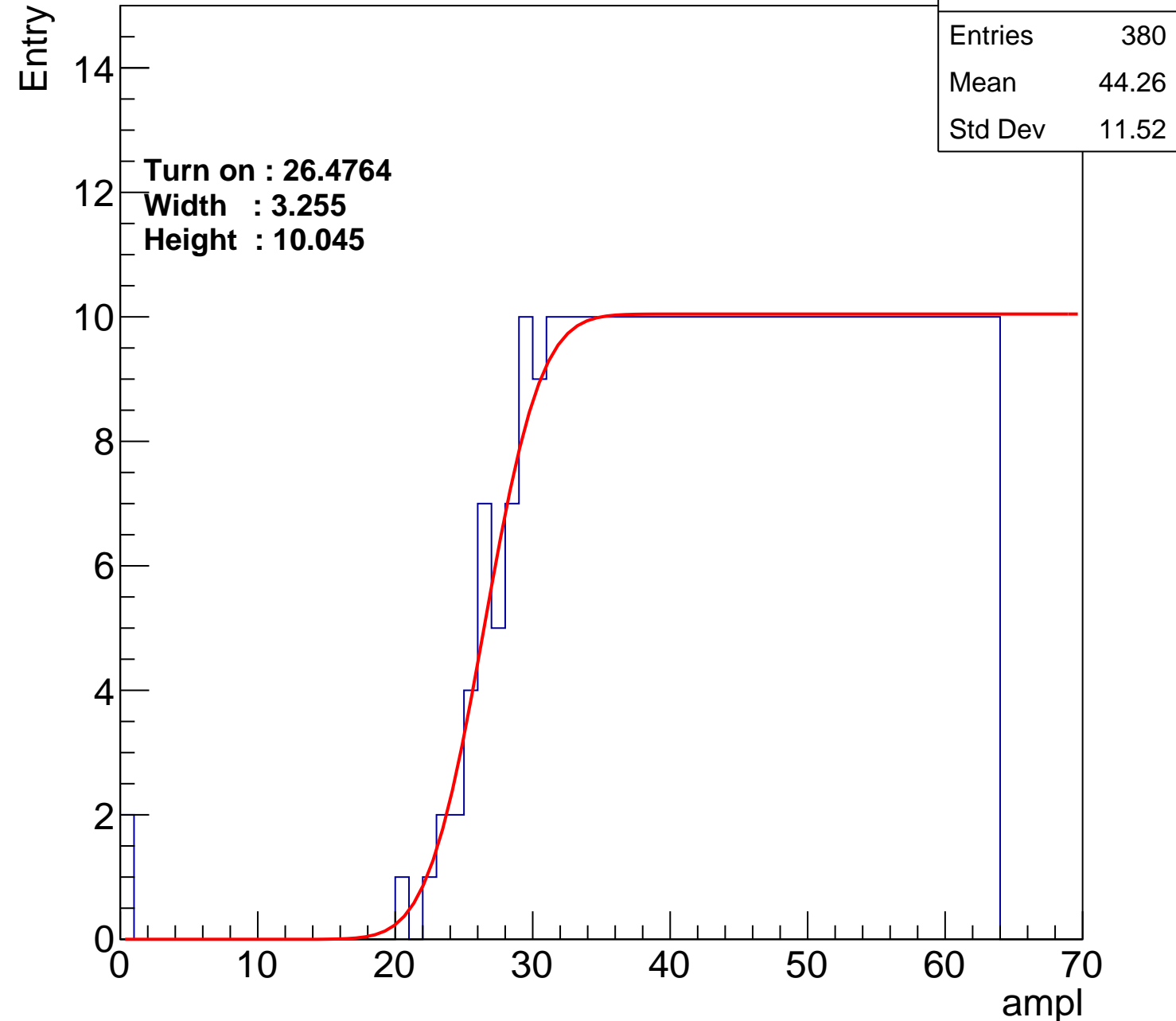
Width : 3.255

Height : 10.045

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U9-ch5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	367
Mean	44.91
Std Dev	11.17

Turn on : 27.7146

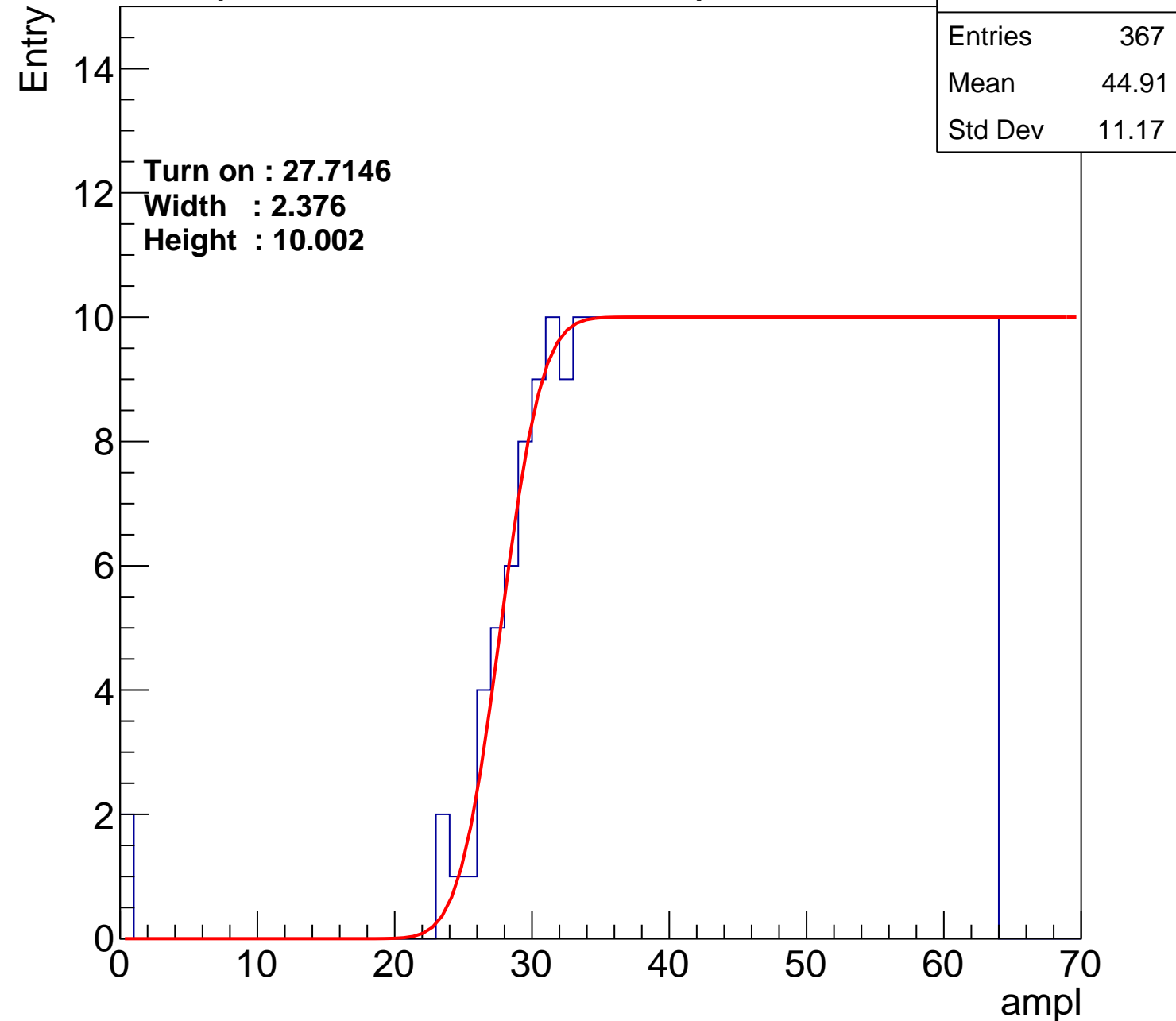
Width : 2.376

Height : 10.002

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U9-ch6

calib\_packv5\_042523\_0143.root, FC#9, port A1

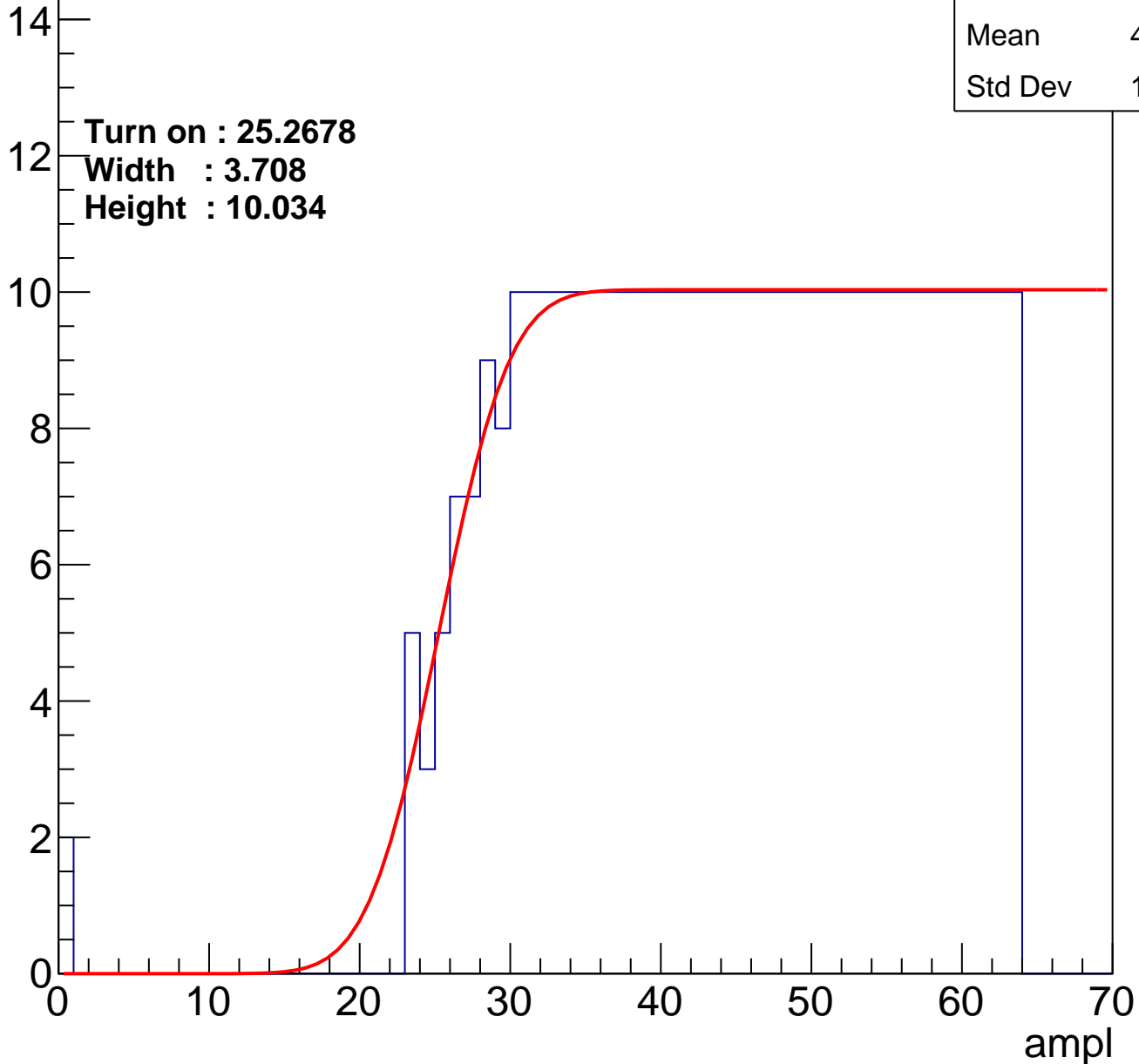
Entries	386
Mean	43.98
Std Dev	11.64

Turn on : 25.2678

Width : 3.708

Height : 10.034

Entry





# B0L001S, U9-ch7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	342
Mean	46.06
Std Dev	10.8

Turn on : 30.4179

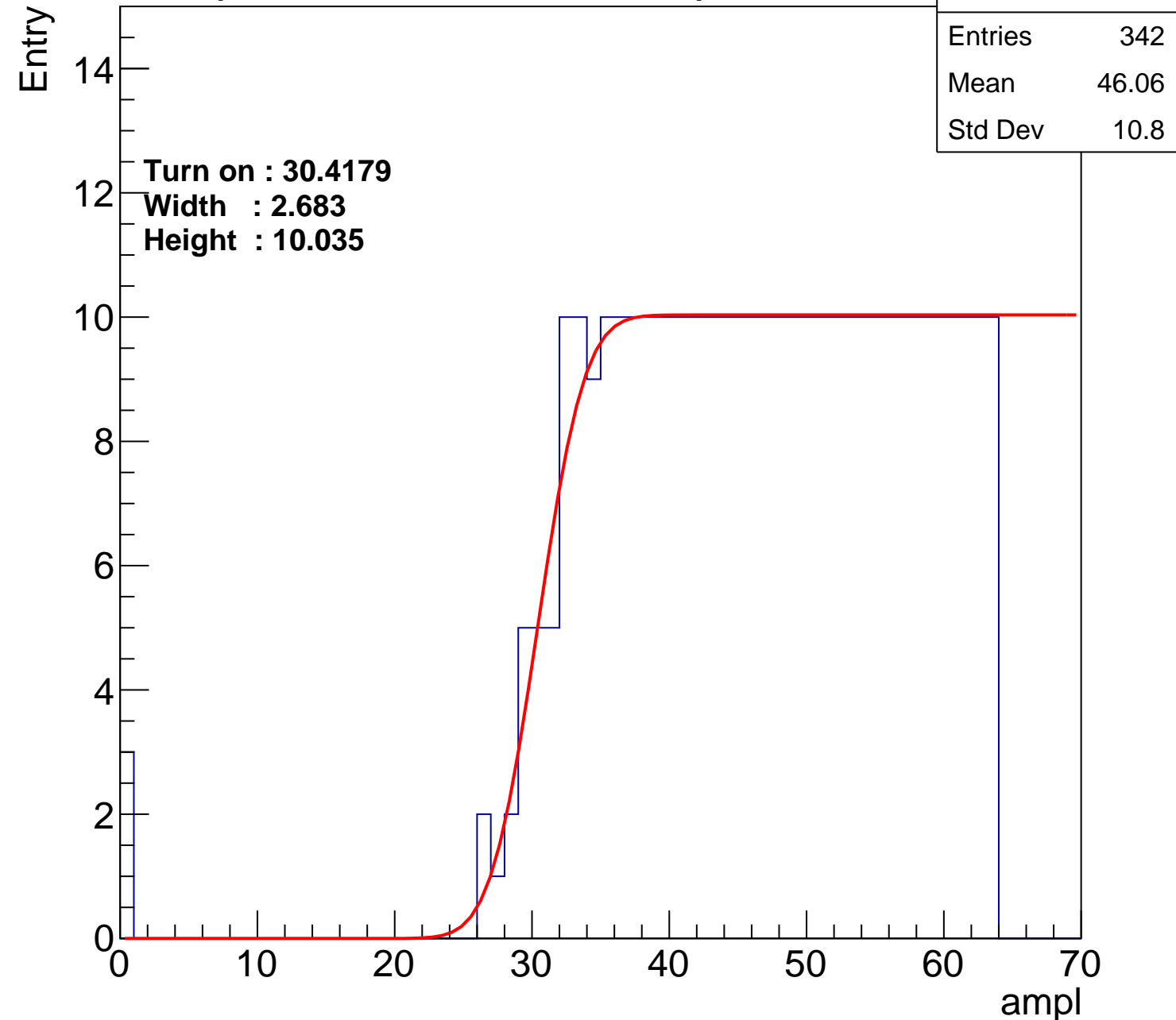
Width : 2.683

Height : 10.035

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U9-ch8

calib\_packv5\_042523\_0143.root, FC#9, port A1

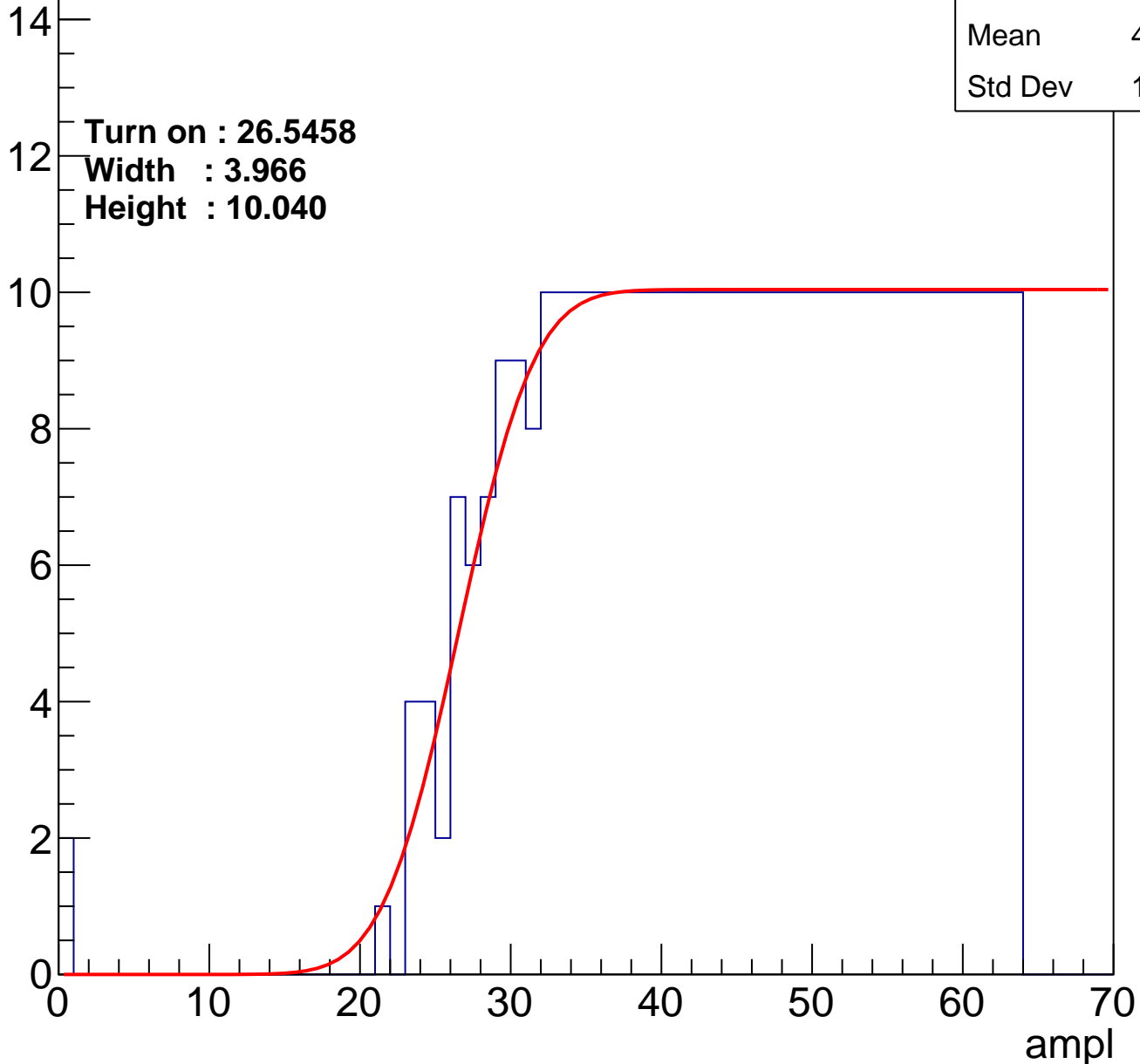
Entries	379
Mean	44.27
Std Dev	11.55

**Turn on : 26.5458**

**Width : 3.966**

**Height : 10.040**

Entry



# B0L001S, U9-ch9

calib\_packv5\_042523\_0143.root, FC#9, port A1

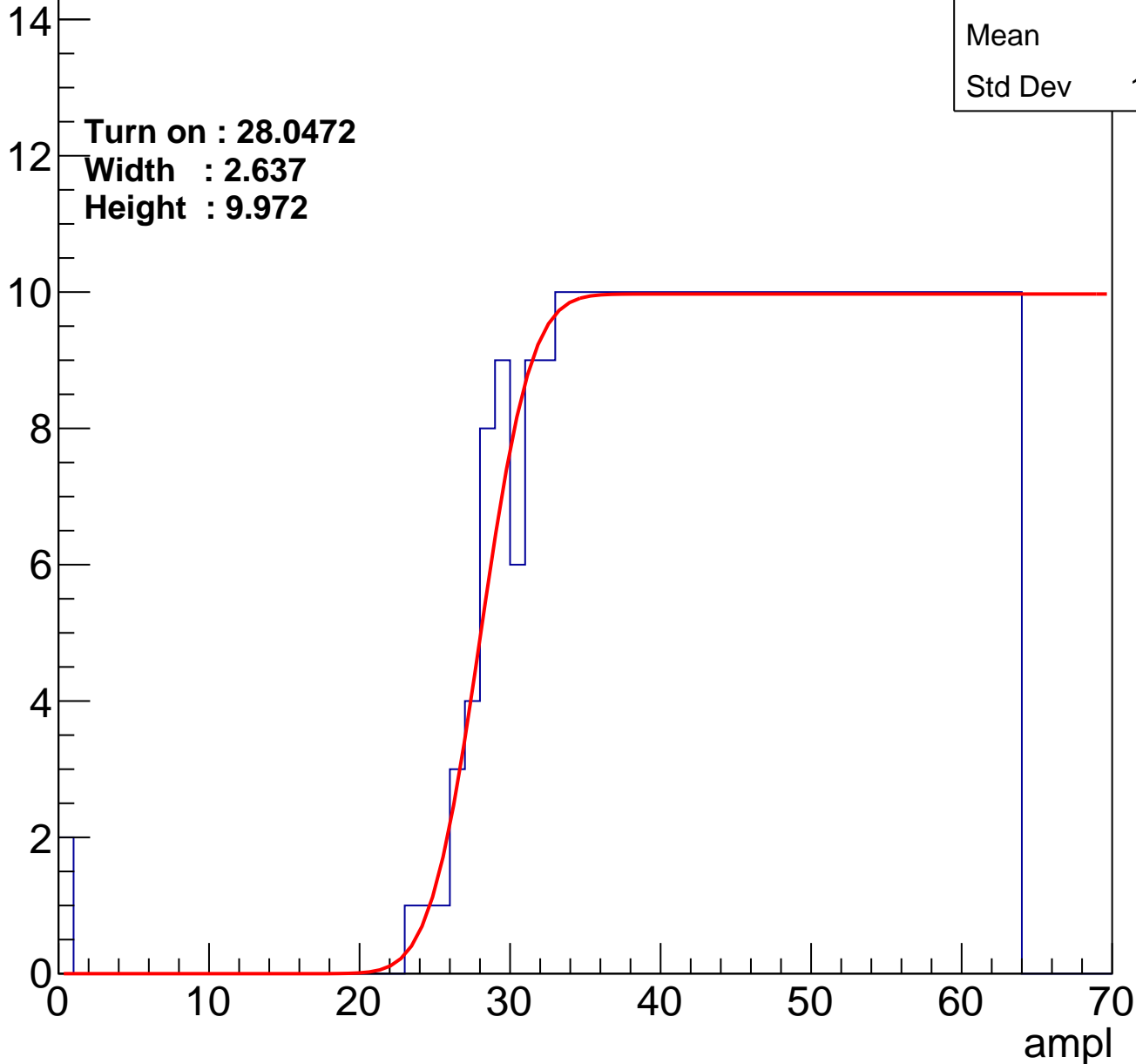
Entries	363
Mean	45.1
Std Dev	11.08

**Turn on : 28.0472**

**Width : 2.637**

**Height : 9.972**

Entry



# B0L001S, U9-ch10

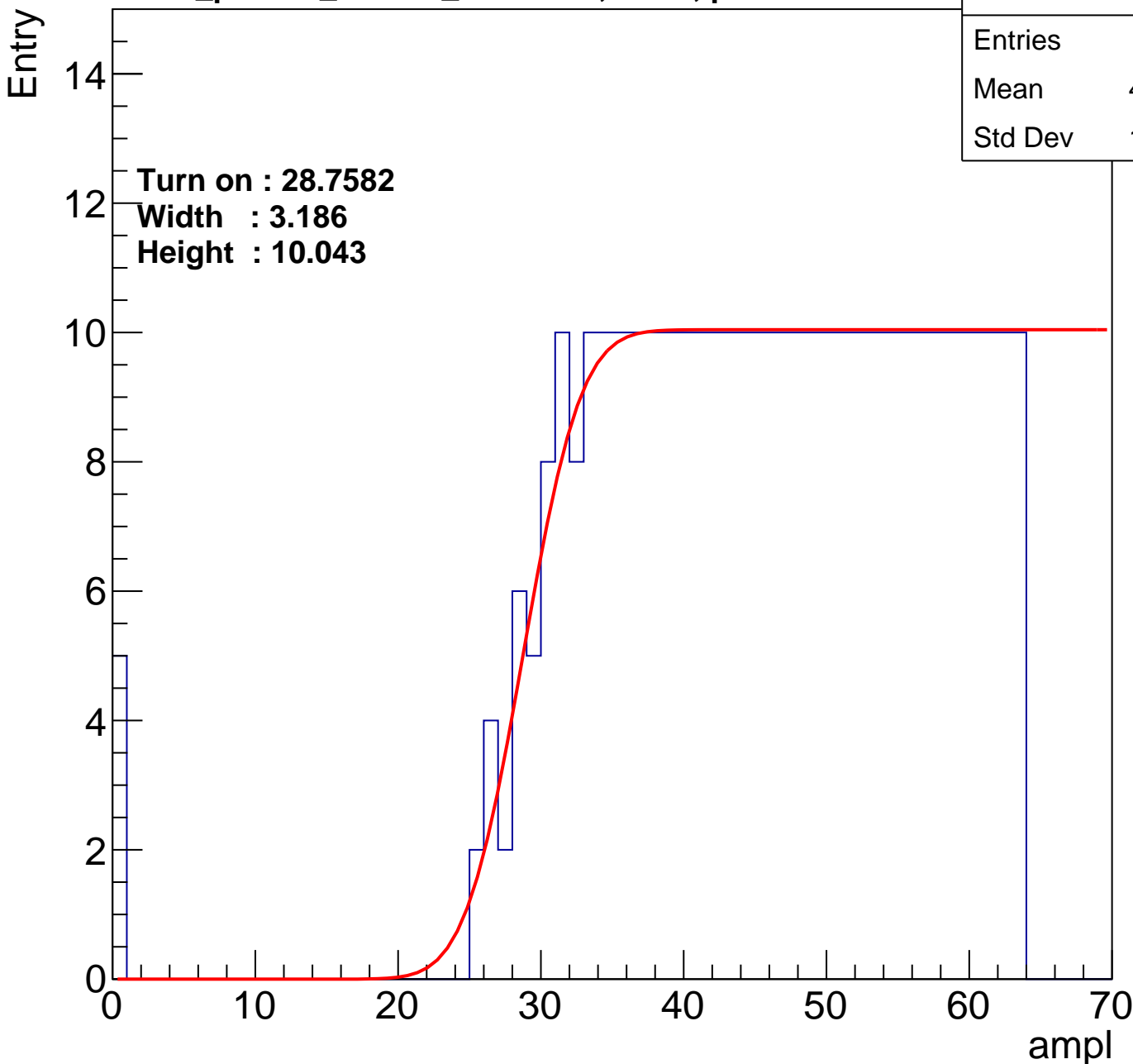
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	360
Mean	45.02
Std Dev	11.63

Turn on : 28.7582

Width : 3.186

Height : 10.043



# B0L001S, U9-ch11

calib\_packv5\_042523\_0143.root, FC#9, port A1

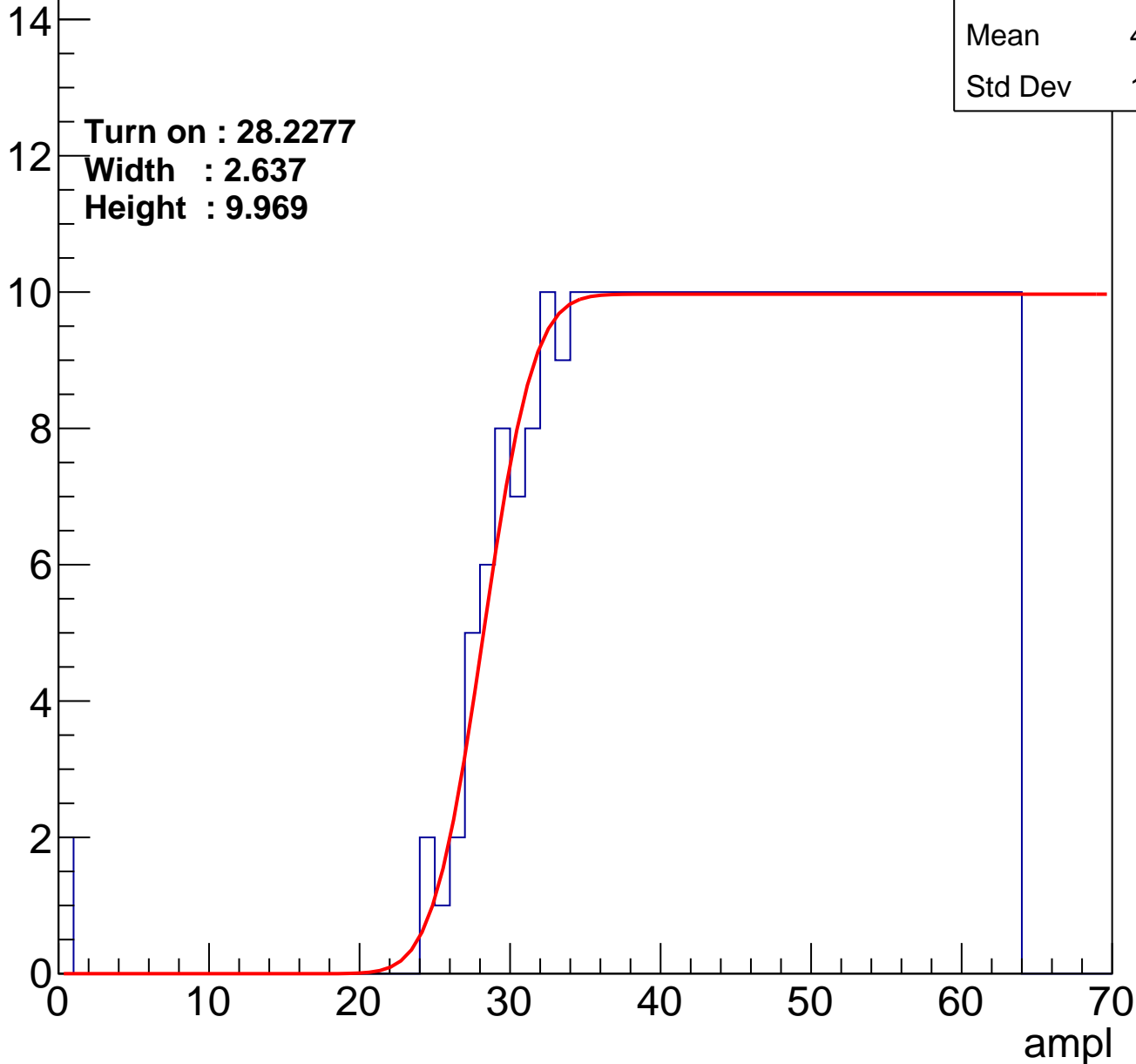
Entries	360
Mean	45.24
Std Dev	11.02

**Turn on : 28.2277**

**Width : 2.637**

**Height : 9.969**

Entry



# B0L001S, U9-ch12

calib\_packv5\_042523\_0143.root, FC#9, port A1

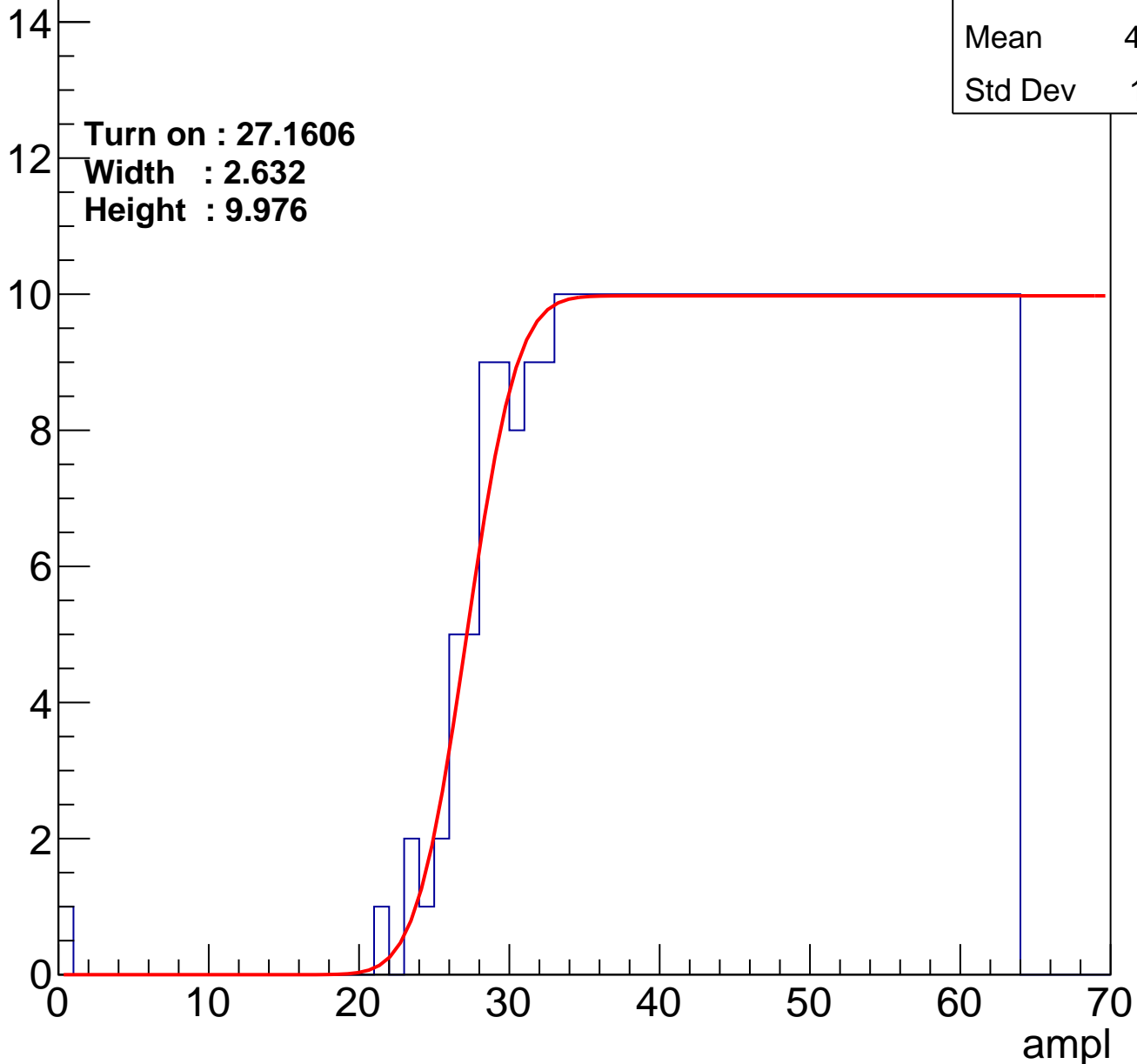
Entries	371
Mean	44.76
Std Dev	11.11

**Turn on : 27.1606**

**Width : 2.632**

**Height : 9.976**

Entry



# B0L001S, U9-ch13

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	359
Mean	45.3
Std Dev	10.89

Turn on : 28.5761

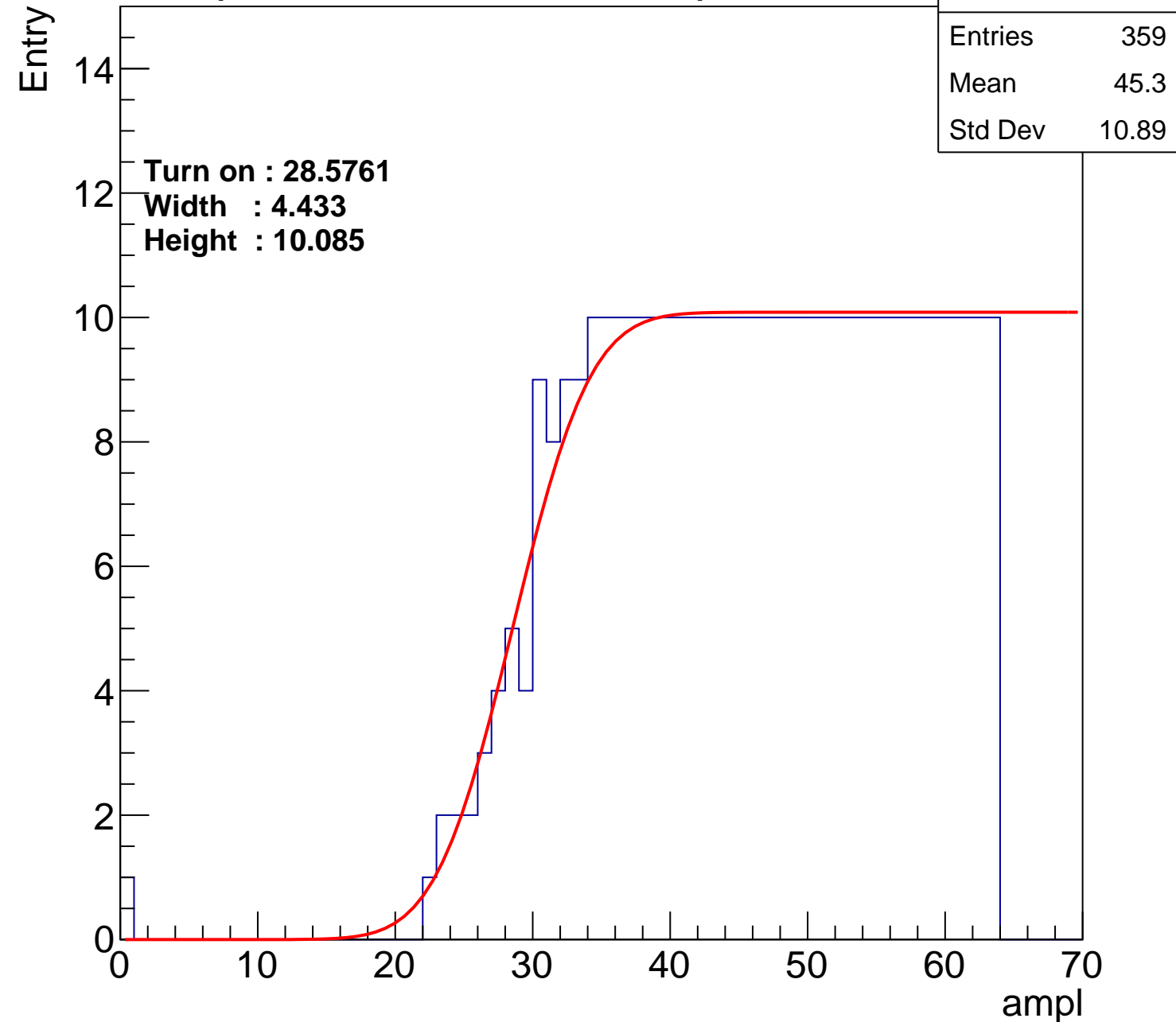
Width : 4.433

Height : 10.085

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U9-ch14

calib\_packv5\_042523\_0143.root, FC#9, port A1

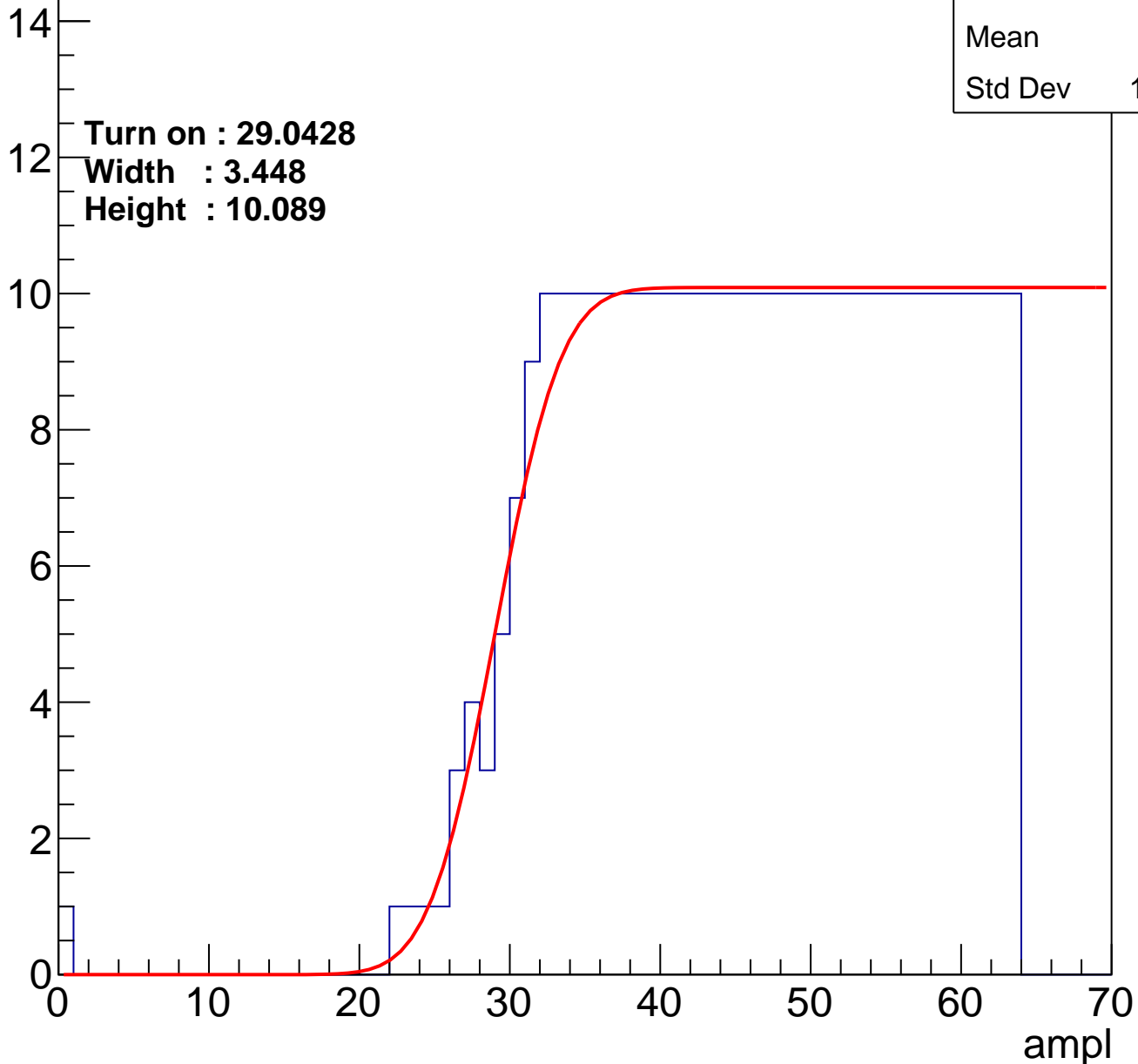
Entries	356
Mean	45.5
Std Dev	10.72

Turn on : 29.0428

Width : 3.448

Height : 10.089

Entry





# B0L001S, U9-ch15

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	362
Mean	45.19
Std Dev	11

**Turn on : 27.6358**

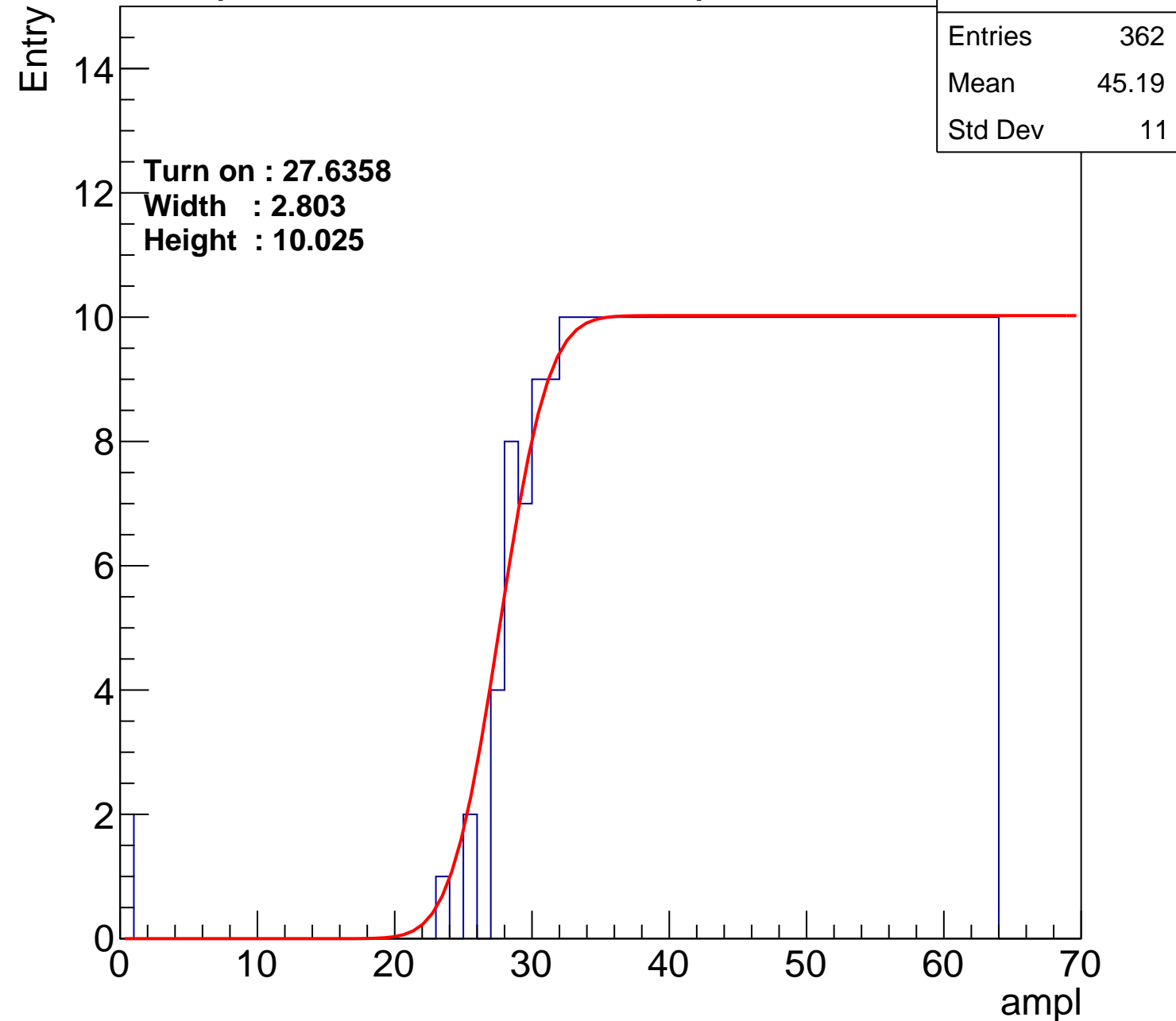
**Width : 2.803**

**Height : 10.025**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U9-ch16

calib\_packv5\_042523\_0143.root, FC#9, port A1

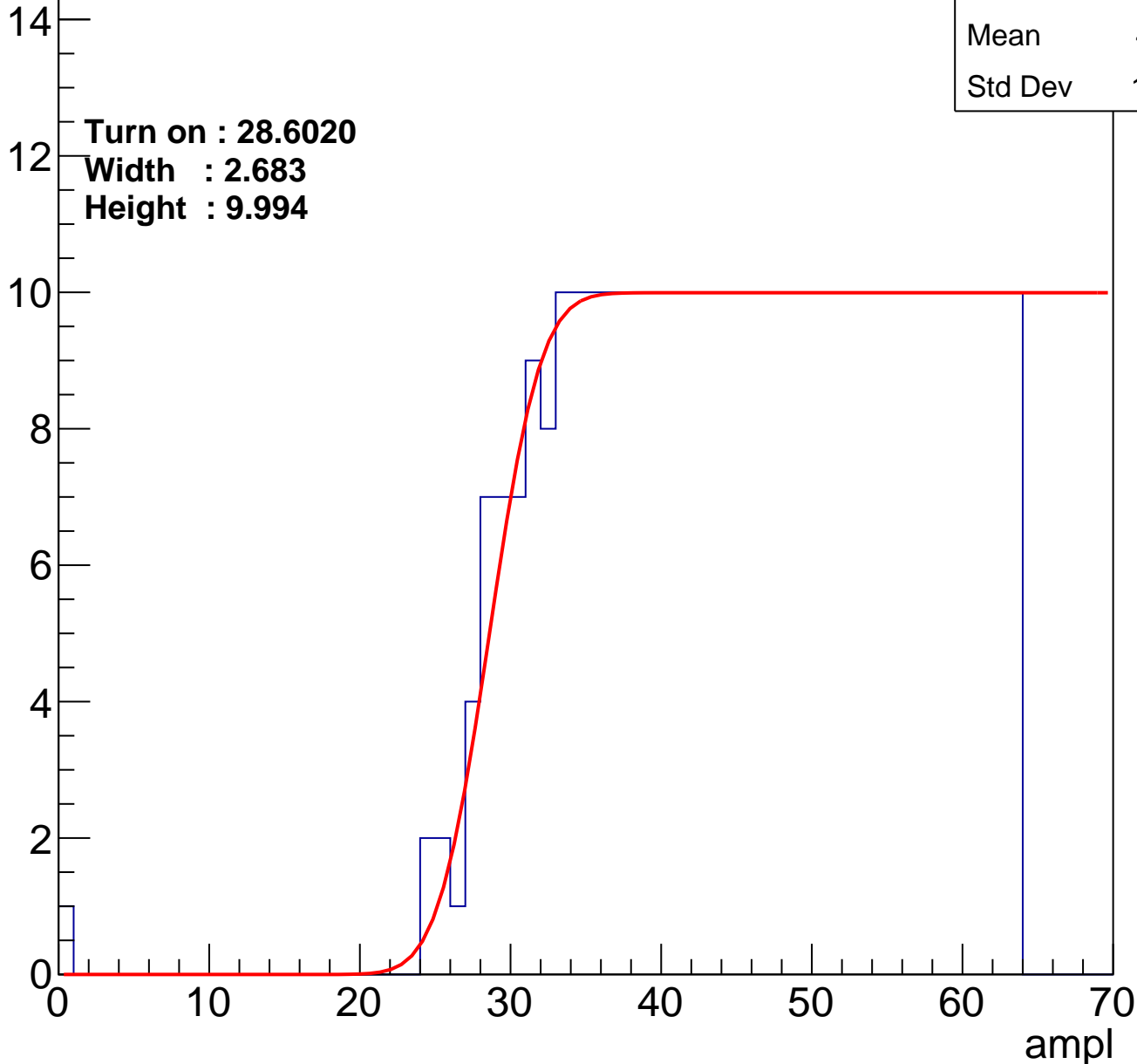
Entries	358
Mean	45.41
Std Dev	10.75

**Turn on : 28.6020**

**Width : 2.683**

**Height : 9.994**

Entry



# B0L001S, U9-ch17

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

14

12

10

8

6

4

2

0

Turn on : 29.0114

Width : 2.778

Height : 9.993

Entries

356

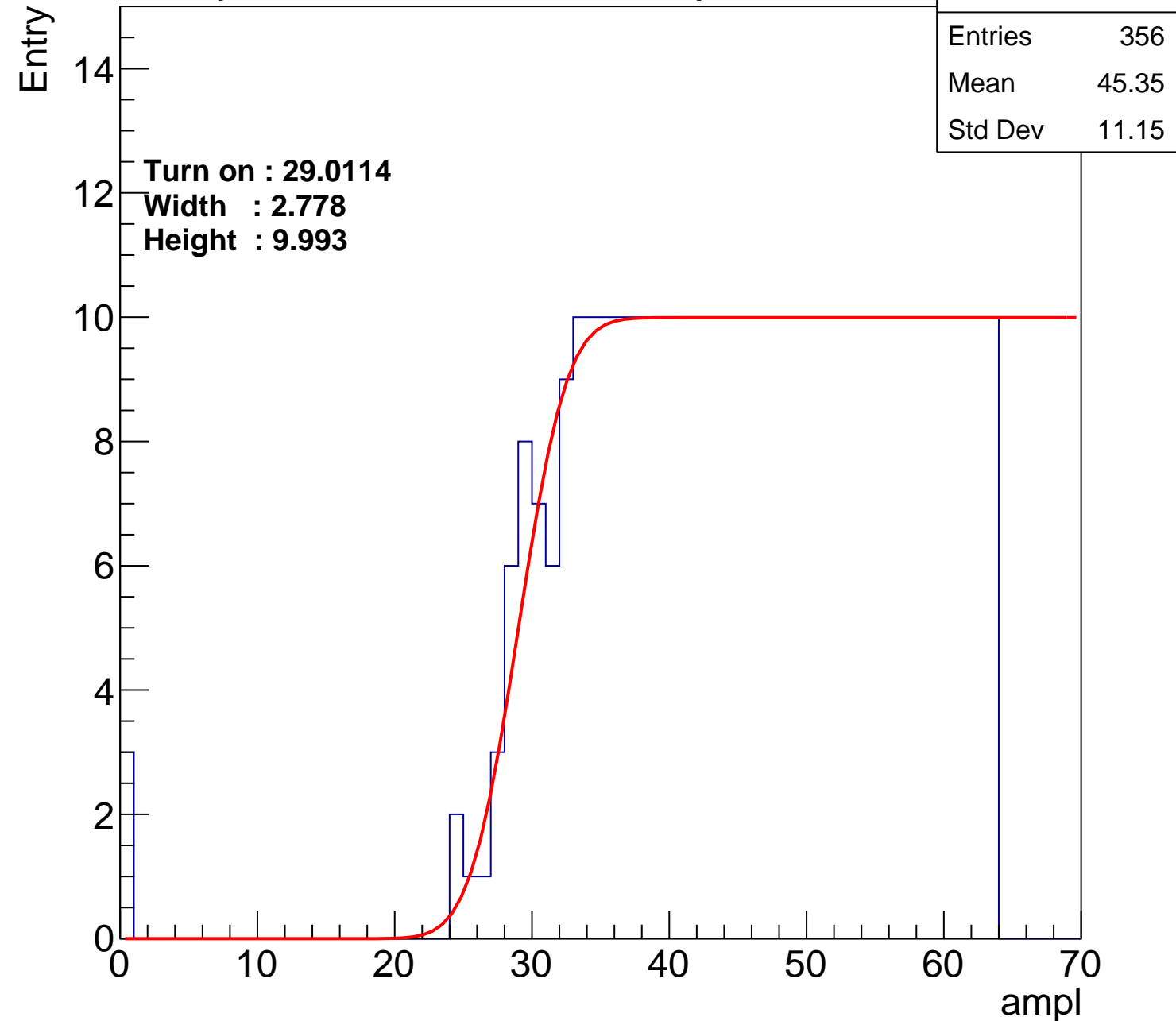
Mean

45.35

Std Dev

11.15

ampl



# B0L001S, U9-ch18

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	353
Mean	45.58
Std Dev	10.84

Turn on : 28.9858

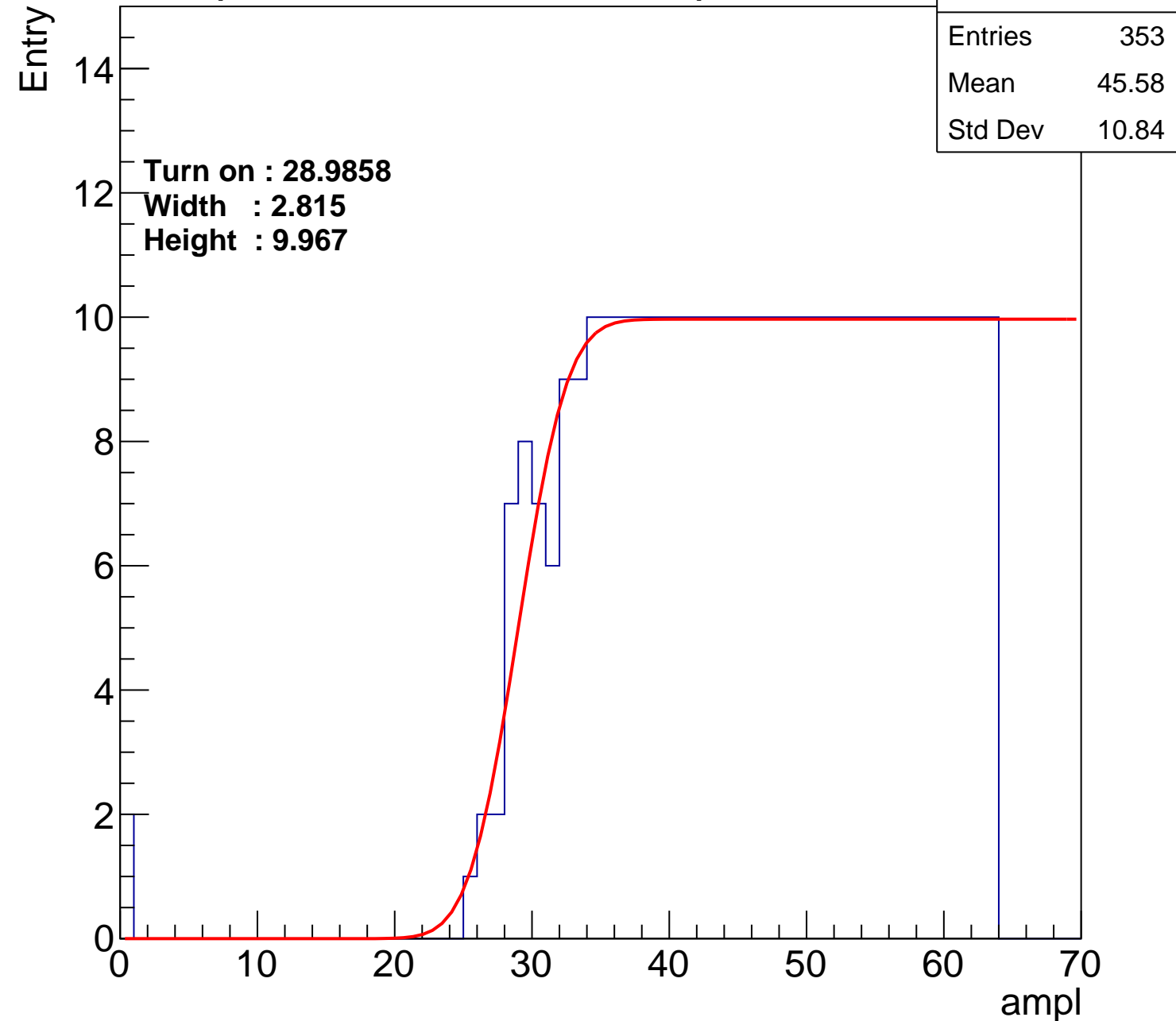
Width : 2.815

Height : 9.967

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U9-ch19

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

14

12

10

8

6

4

2

0

Turn on : 28.4819

Width : 3.117

Height : 9.952

Entries

357

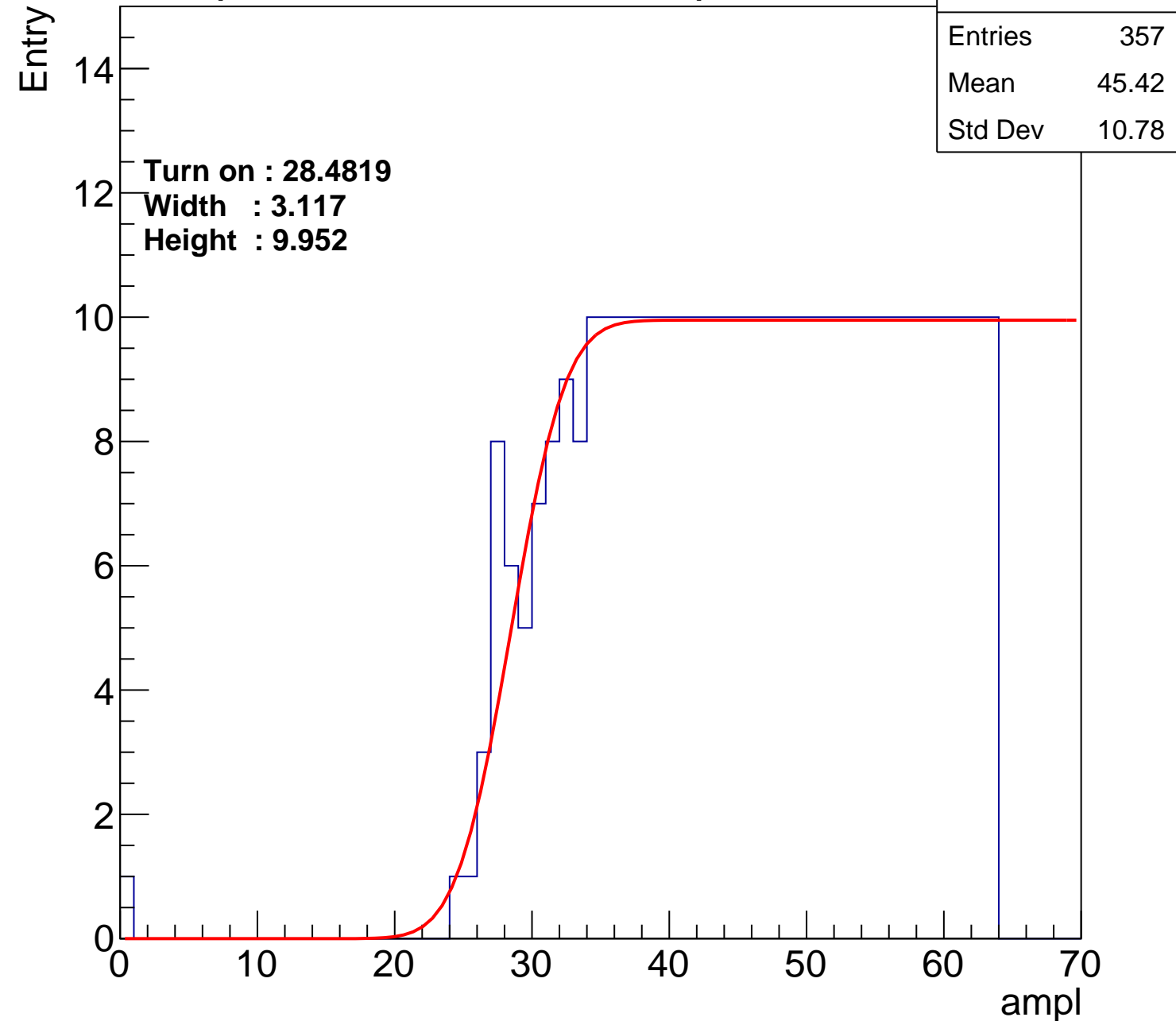
Mean

45.42

Std Dev

10.78

ampl



# B0L001S, U9-ch20

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	358
Mean	45.29
Std Dev	11.14

Turn on : 28.9956

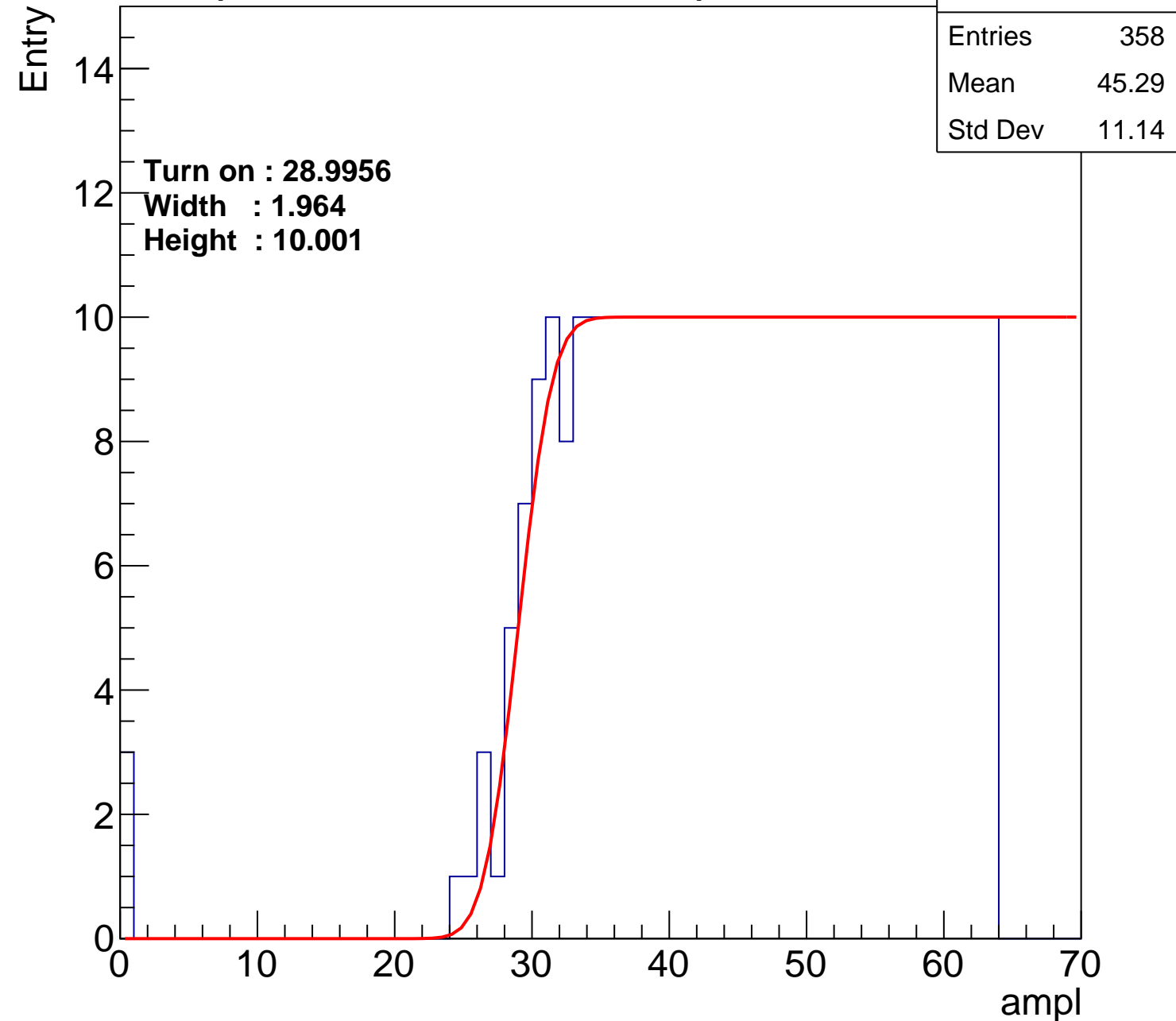
Width : 1.964

Height : 10.001

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U9-ch21

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	376
Mean	44.44
Std Dev	11.43

**Turn on : 26.3879**

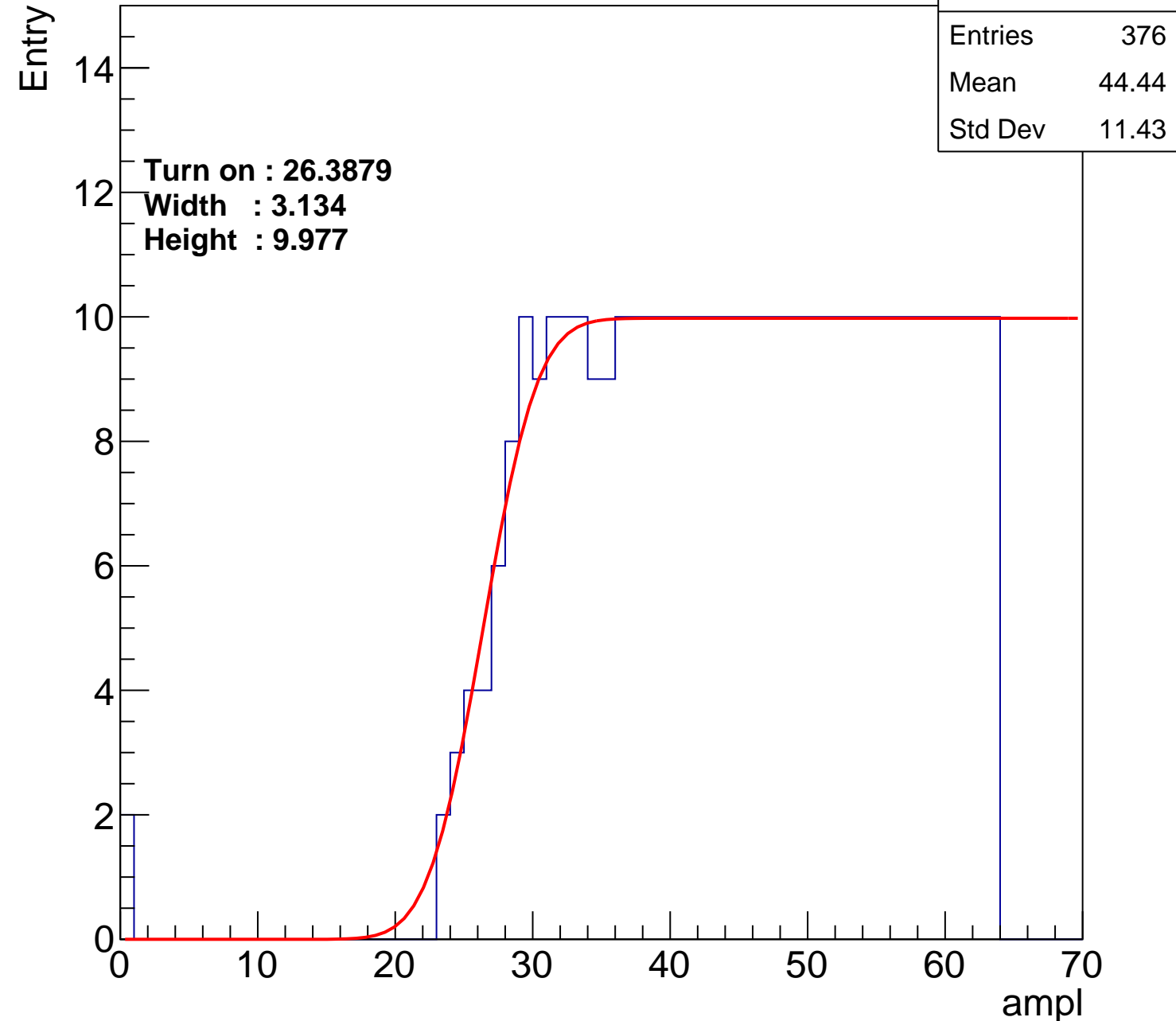
**Width : 3.134**

**Height : 9.977**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U9-ch22

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	362
Mean	44.99
Std Dev	11.39

**Turn on : 28.2770**

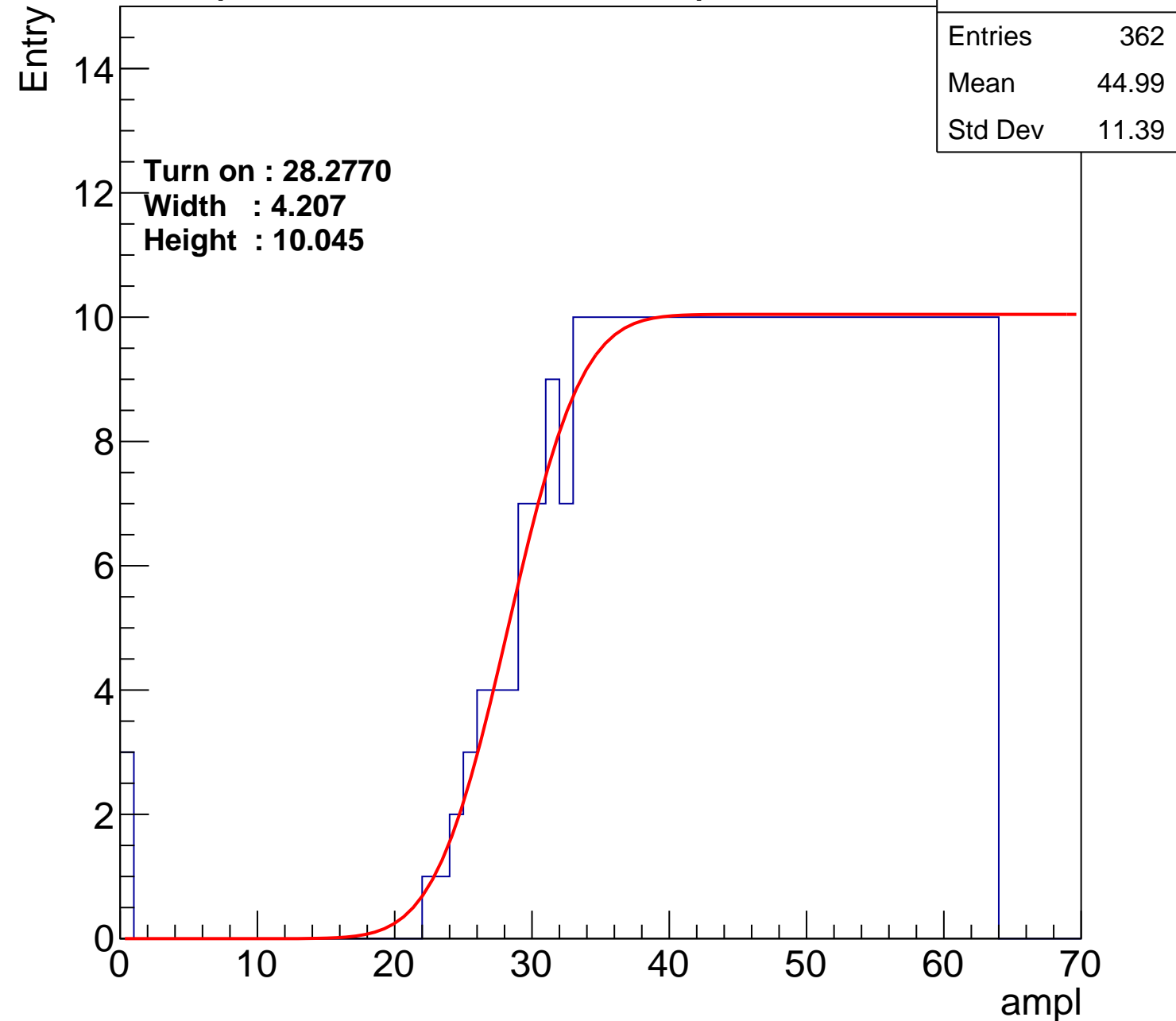
**Width : 4.207**

**Height : 10.045**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B0L001S, U9-ch23

calib\_packv5\_042523\_0143.root, FC#9, port A1

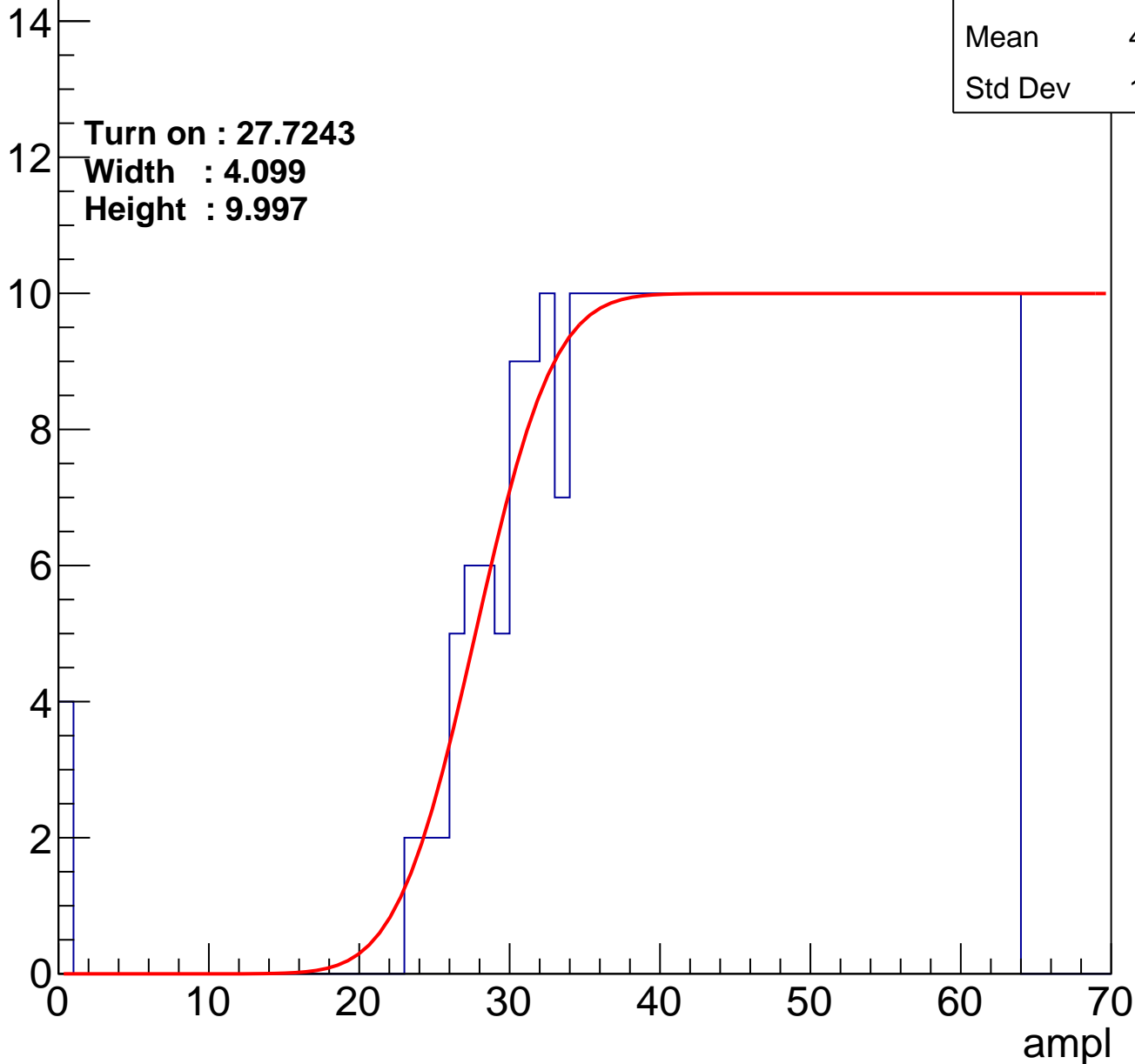
Entry

Entries	367
Mean	44.68
Std Dev	11.69

Turn on : 27.7243

Width : 4.099

Height : 9.997



# B0L001S, U9-ch24

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	348
Mean	45.77
Std Dev	10.92

Turn on : 30.1575

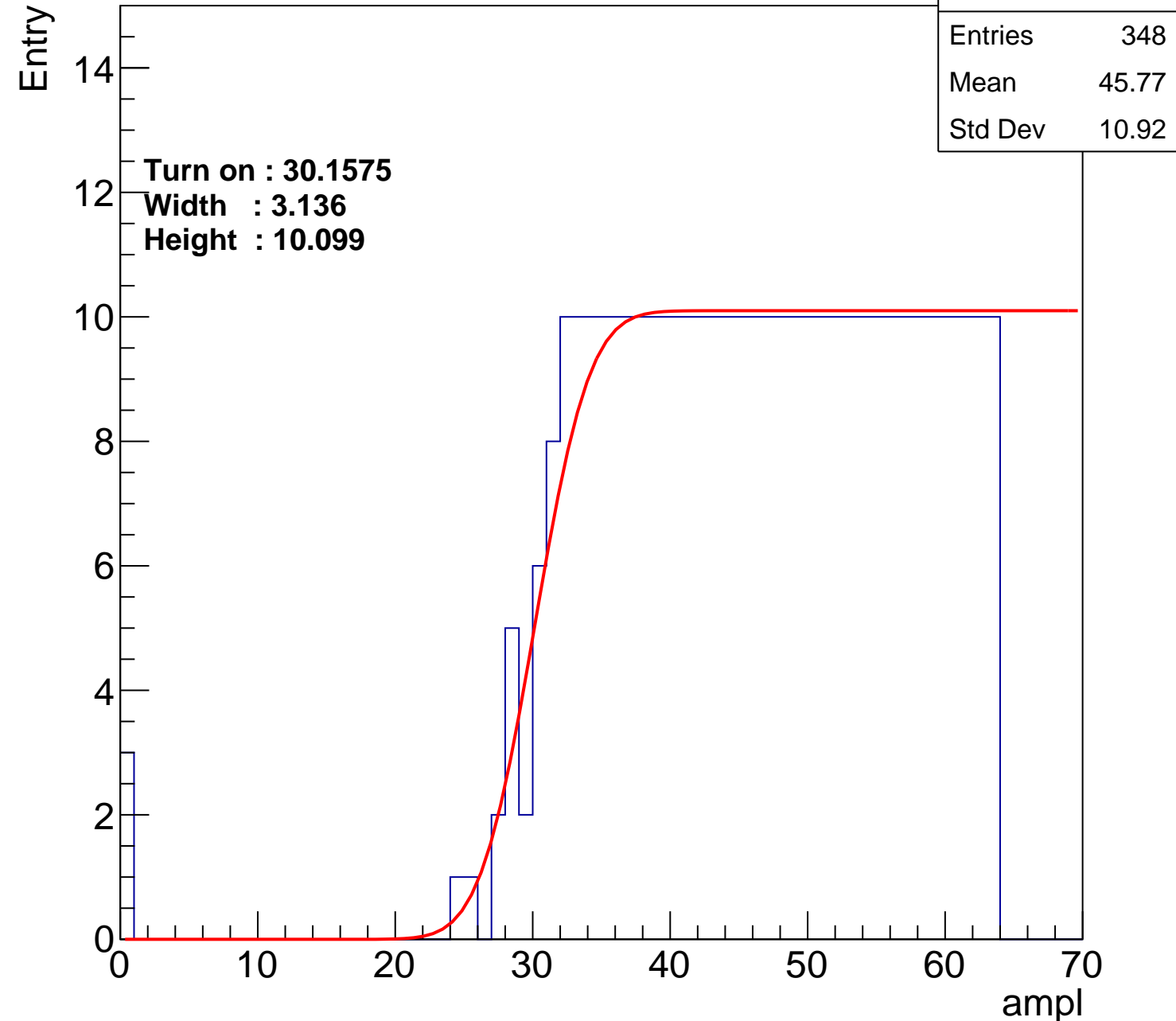
Width : 3.136

Height : 10.099

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U9-ch25

**calib\_packv5\_042523\_0143.root, FC#9, port A1**

Entries	358
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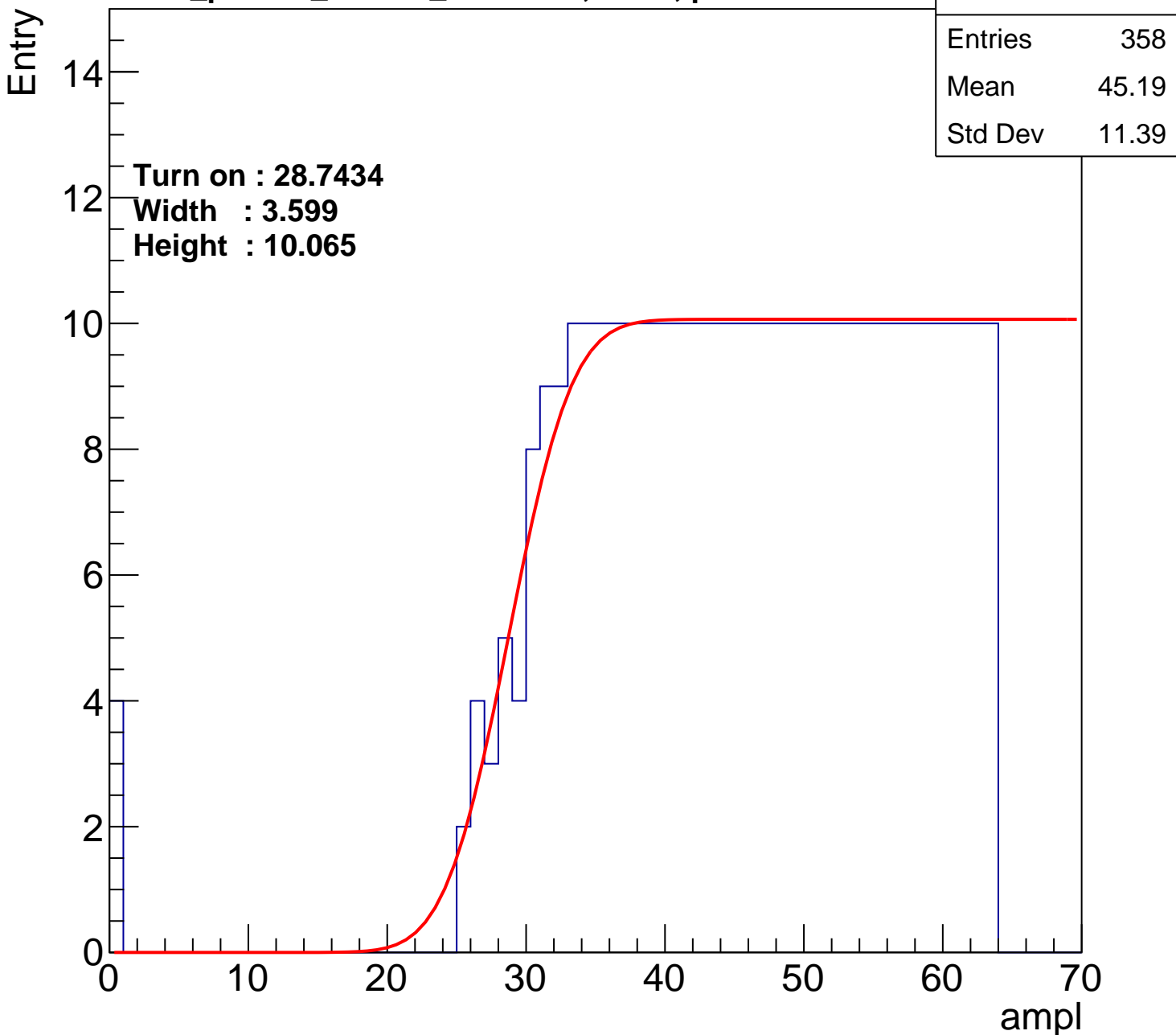
Mean	45.19
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Std Dev	11.39
---------	-------

**Turn on : 28.7434**

**Width : 3.599**

**Height : 10.065**



# B0L001S, U9-ch26

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	356
Mean	45.42
Std Dev	10.94

Turn on : 28.7918

Width : 3.757

Height : 10.072

Entry

14

12

10

8

6

4

2

0

0

10

20

30

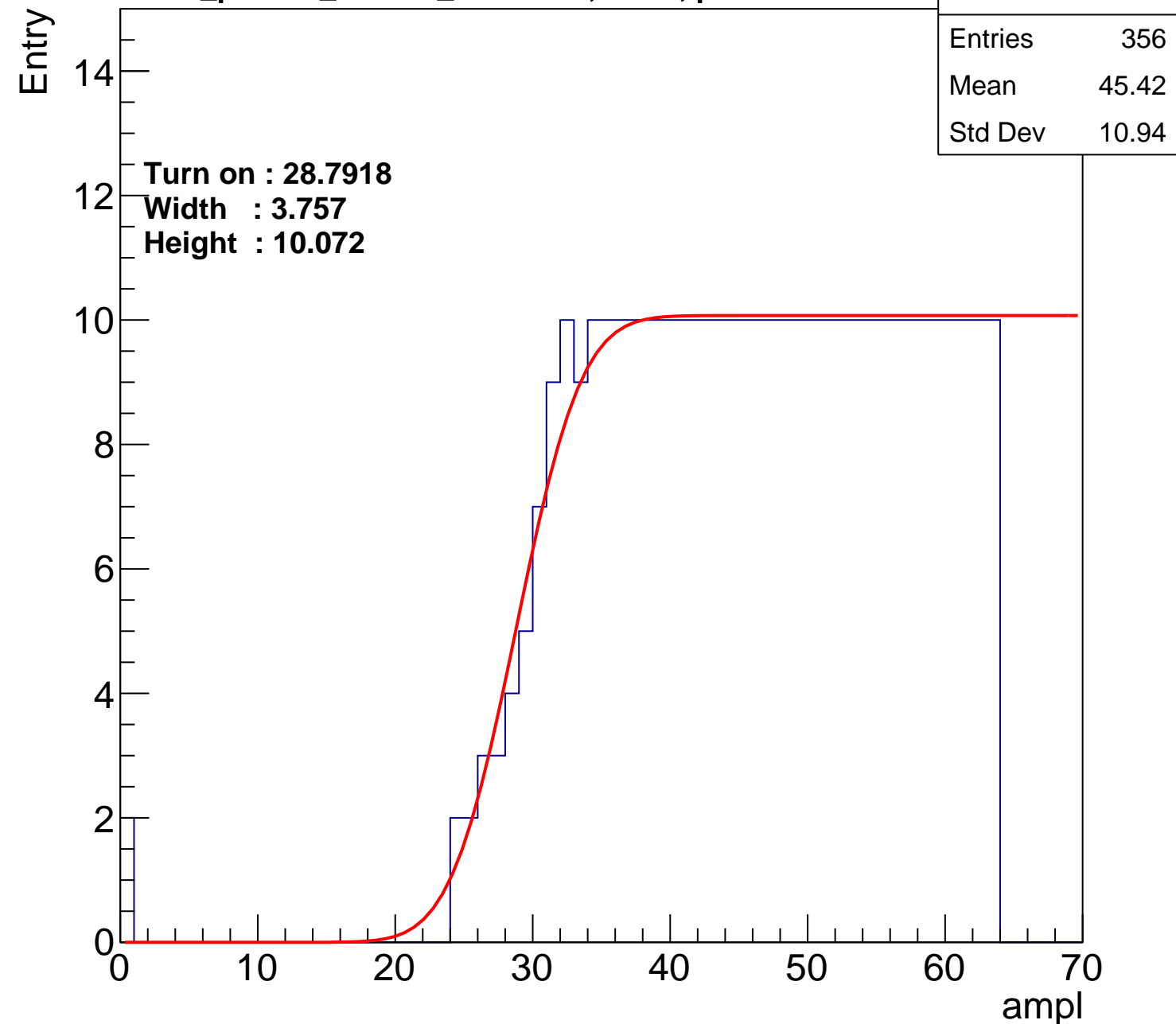
40

50

60

70

ampl



# B0L001S, U9-ch27

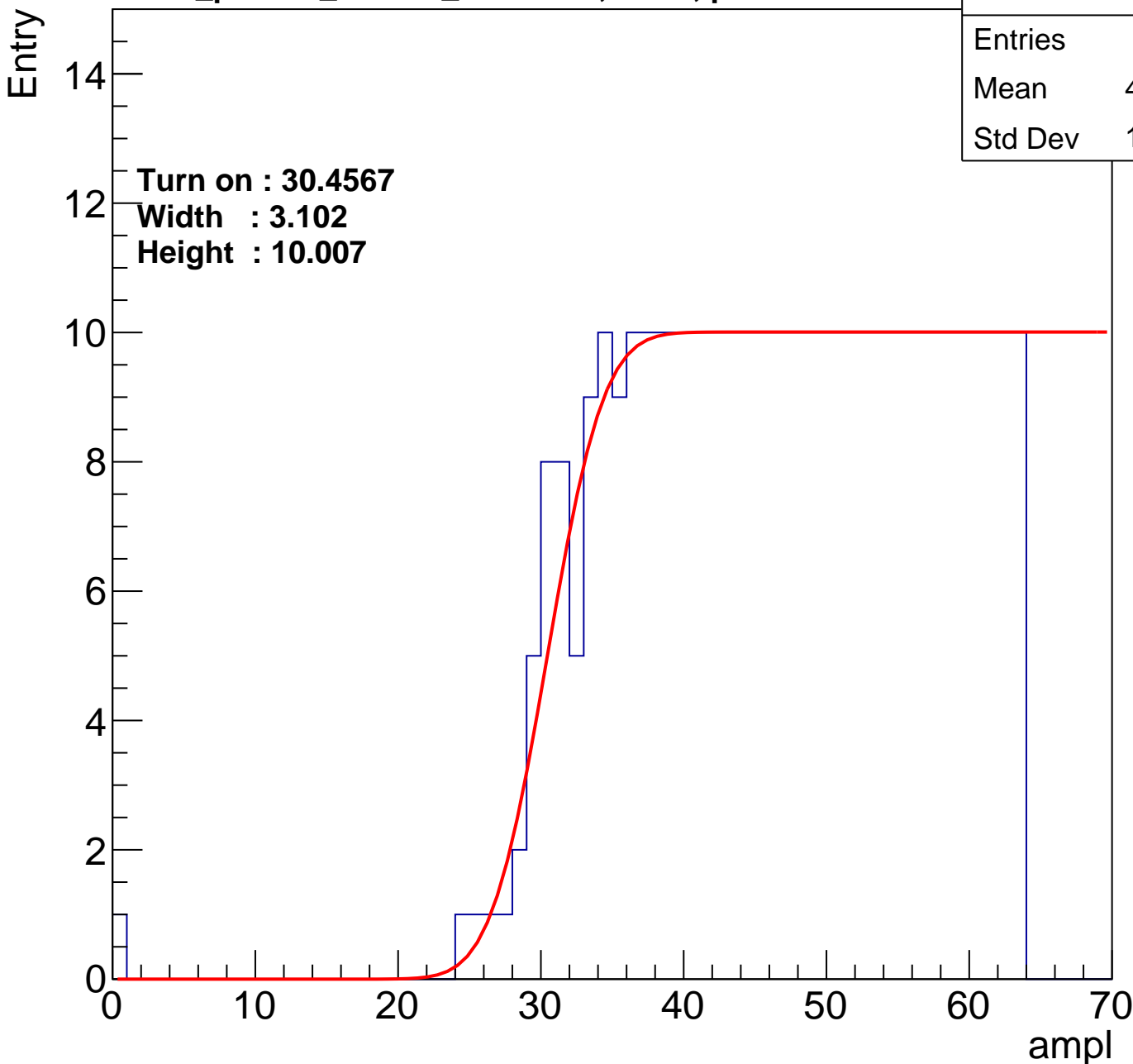
**calib\_packv5\_042523\_0143.root, FC#9, port A1**

Entries	341
Mean	46.23
Std Dev	10.34

**Turn on : 30.4567**

**Width : 3.102**

**Height : 10.007**



# B0L001S, U9-ch28

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	364
Mean	44.82
Std Dev	11.73

**Turn on : 28.1669**

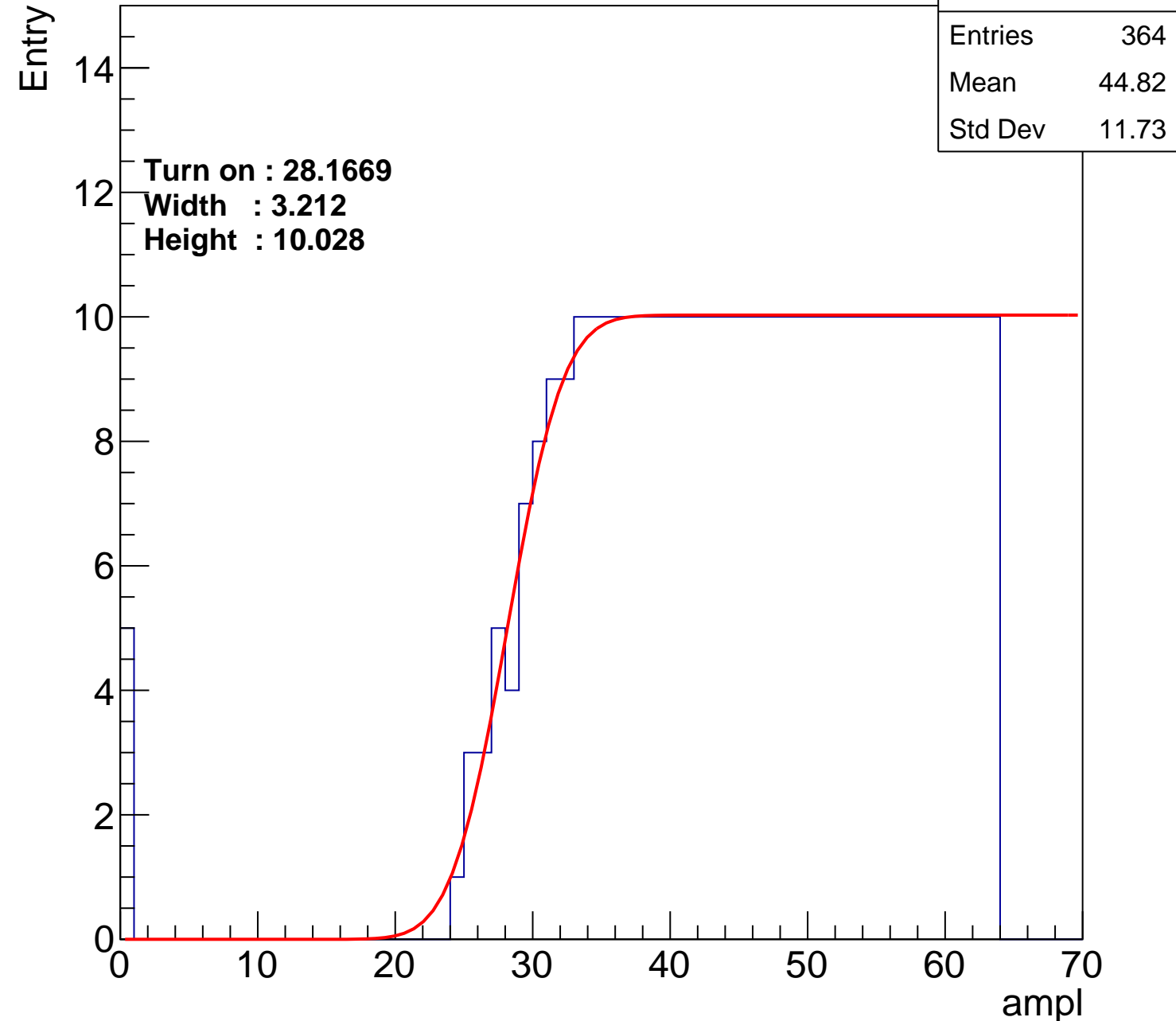
**Width : 3.212**

**Height : 10.028**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U9-ch29

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	358
Mean	45.41
Std Dev	10.74

Turn on : 27.7612

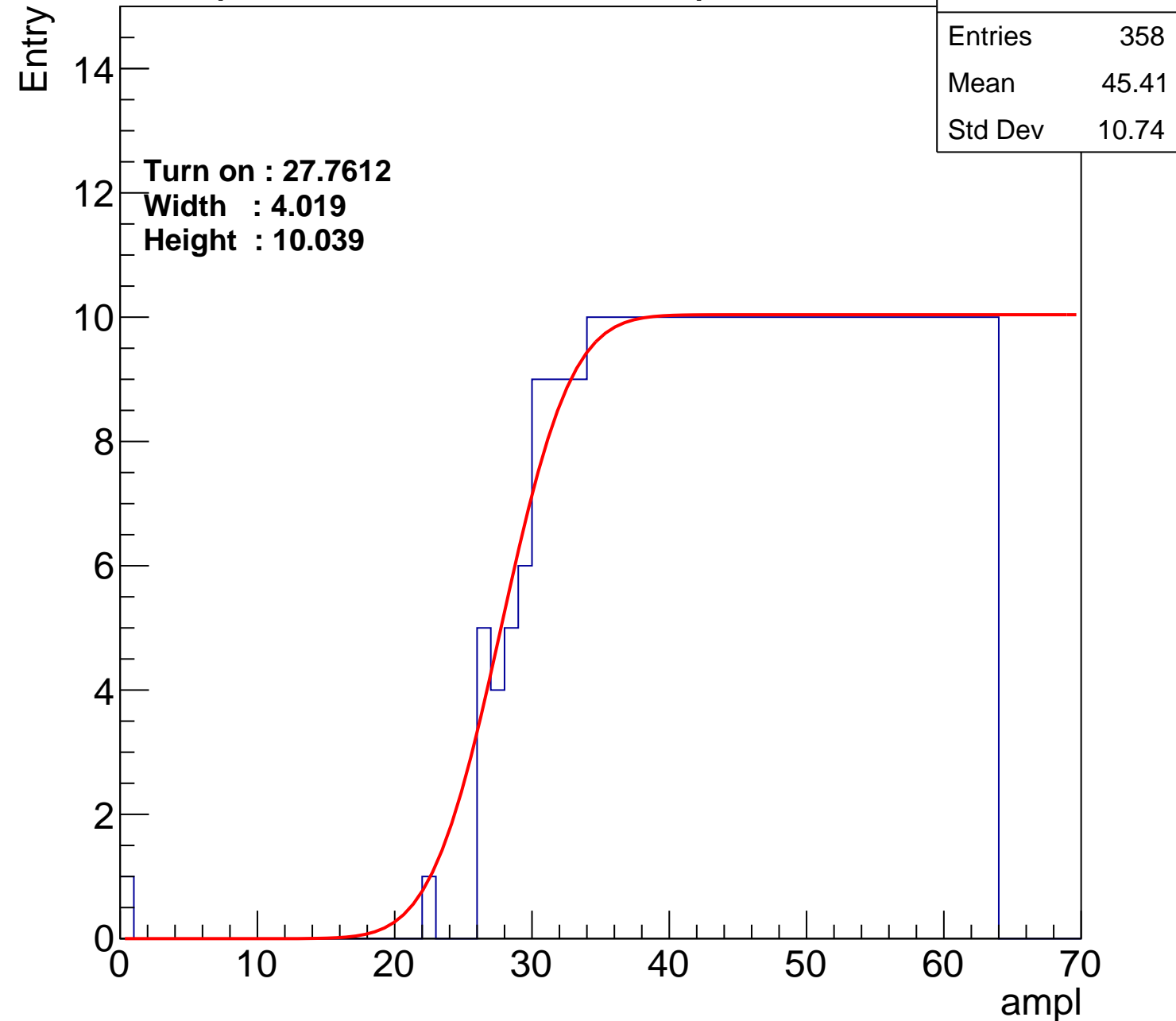
Width : 4.019

Height : 10.039

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U9-ch30

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	375
Mean	44.37
Std Dev	11.76

Turn on : 27.6074

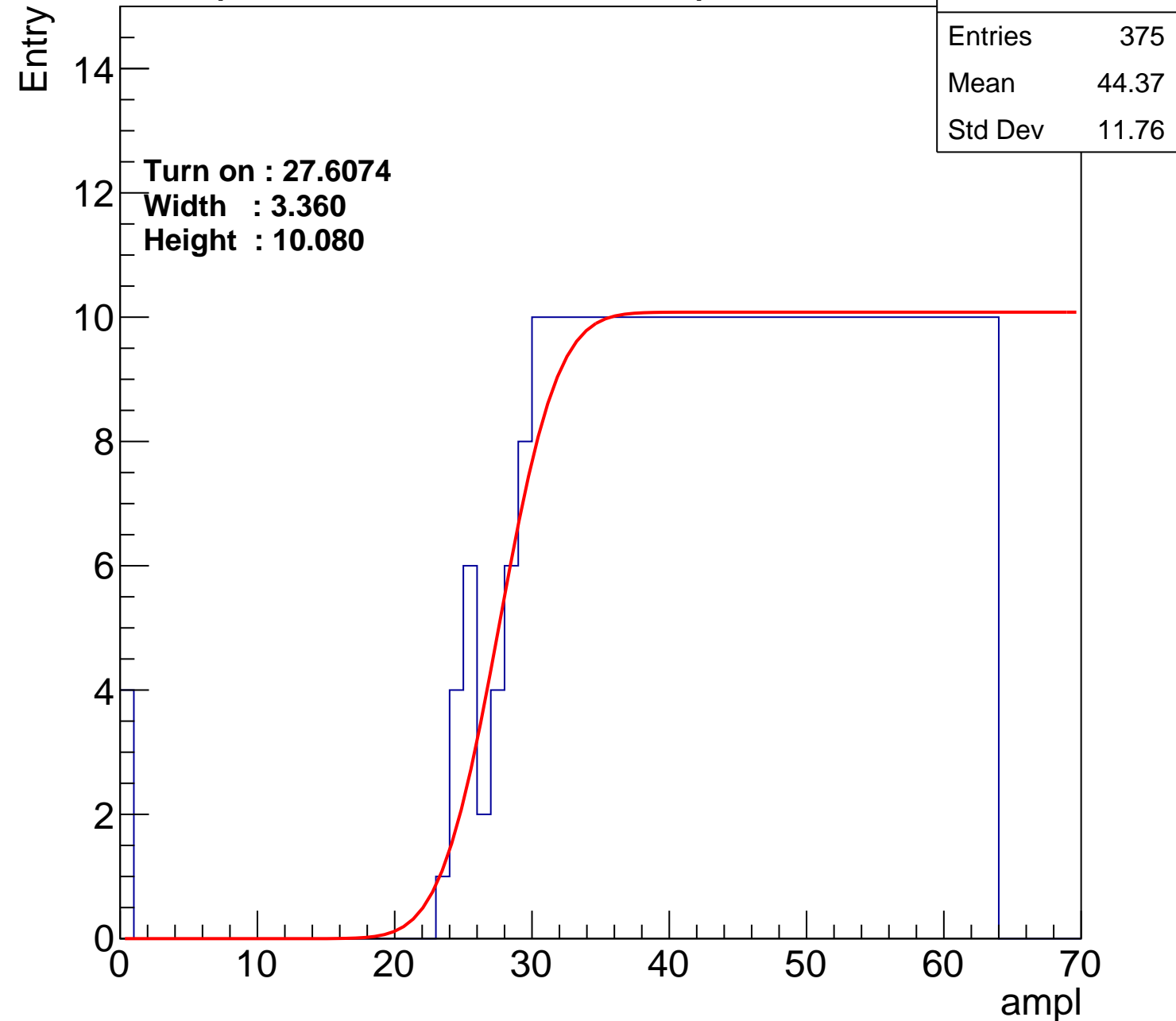
Width : 3.360

Height : 10.080

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B0L001S, U9-ch31

**calib\_packv5\_042523\_0143.root, FC#9, port A1**

Entries	369
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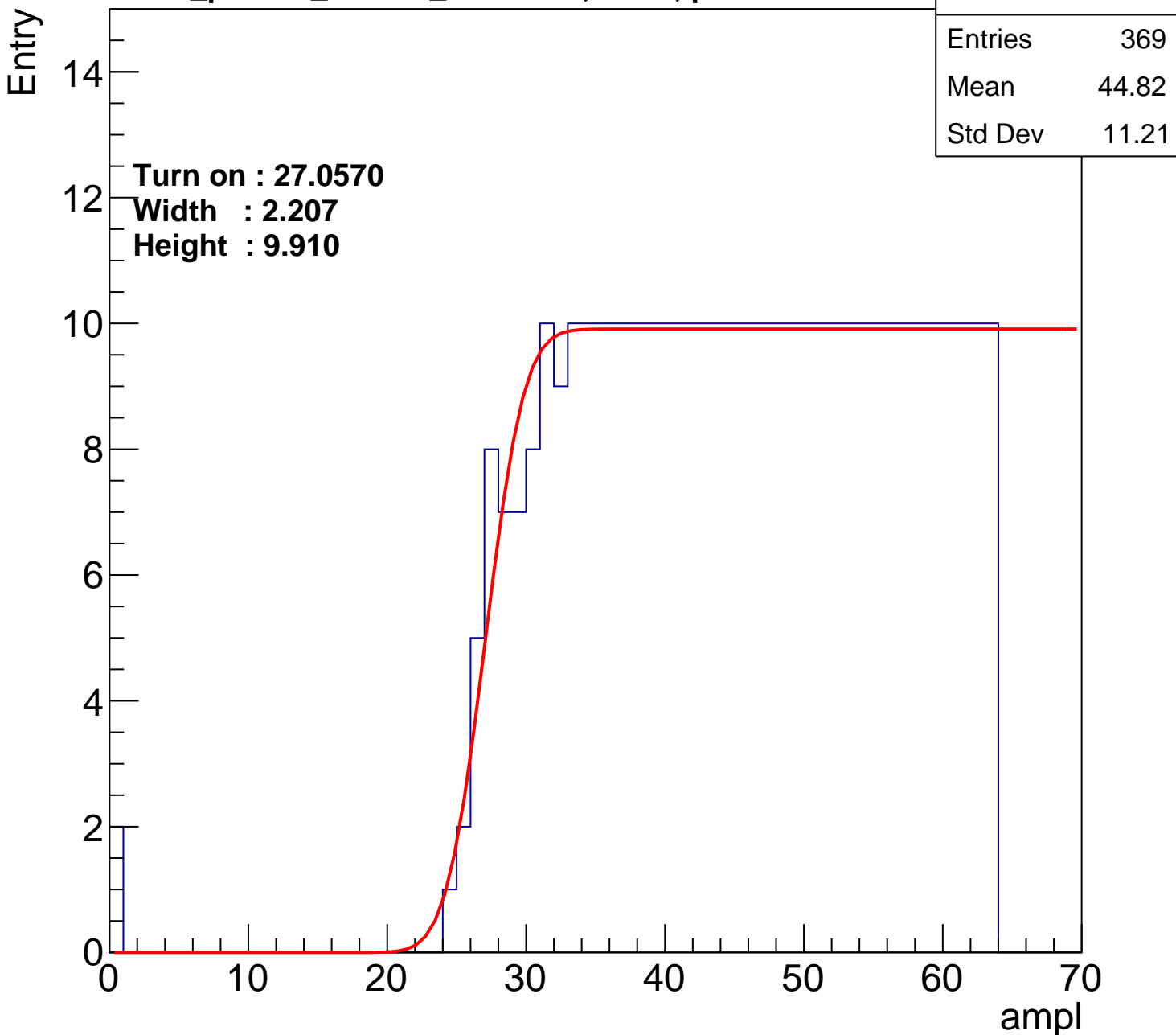
Mean	44.82
------	-------

Std Dev	11.21
---------	-------

**Turn on : 27.0570**

**Width : 2.207**

**Height : 9.910**



# B0L001S, U9-ch32

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	343
Mean	46.07
Std Dev	10.6

**Turn on : 29.7945**

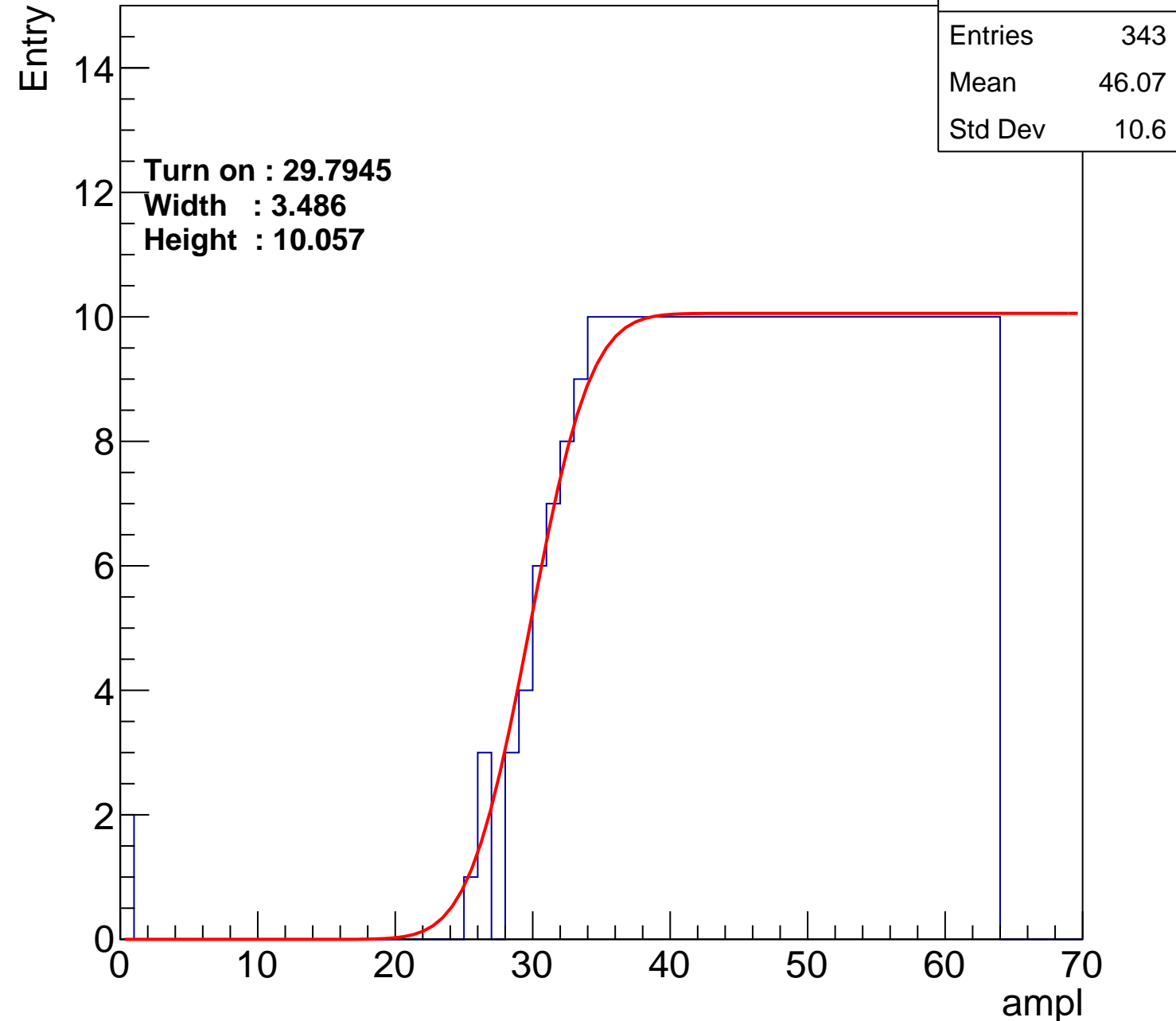
**Width : 3.486**

**Height : 10.057**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U9-ch33

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	384
Mean	43.91
Std Dev	12.01

**Turn on : 26.0571**

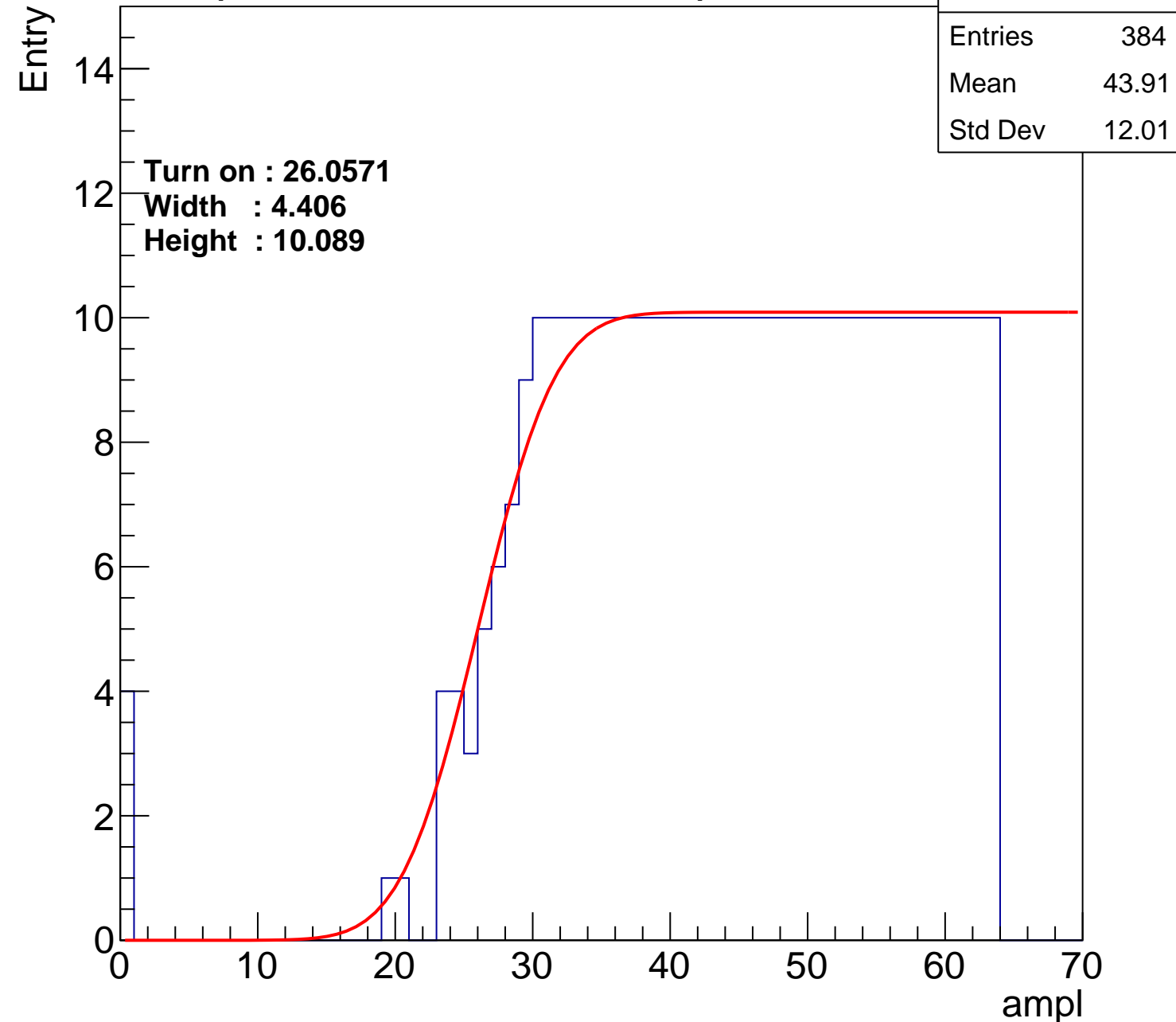
**Width : 4.406**

**Height : 10.089**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U9-ch34

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	366
Mean	44.96
Std Dev	11.14

Turn on : 27.9741

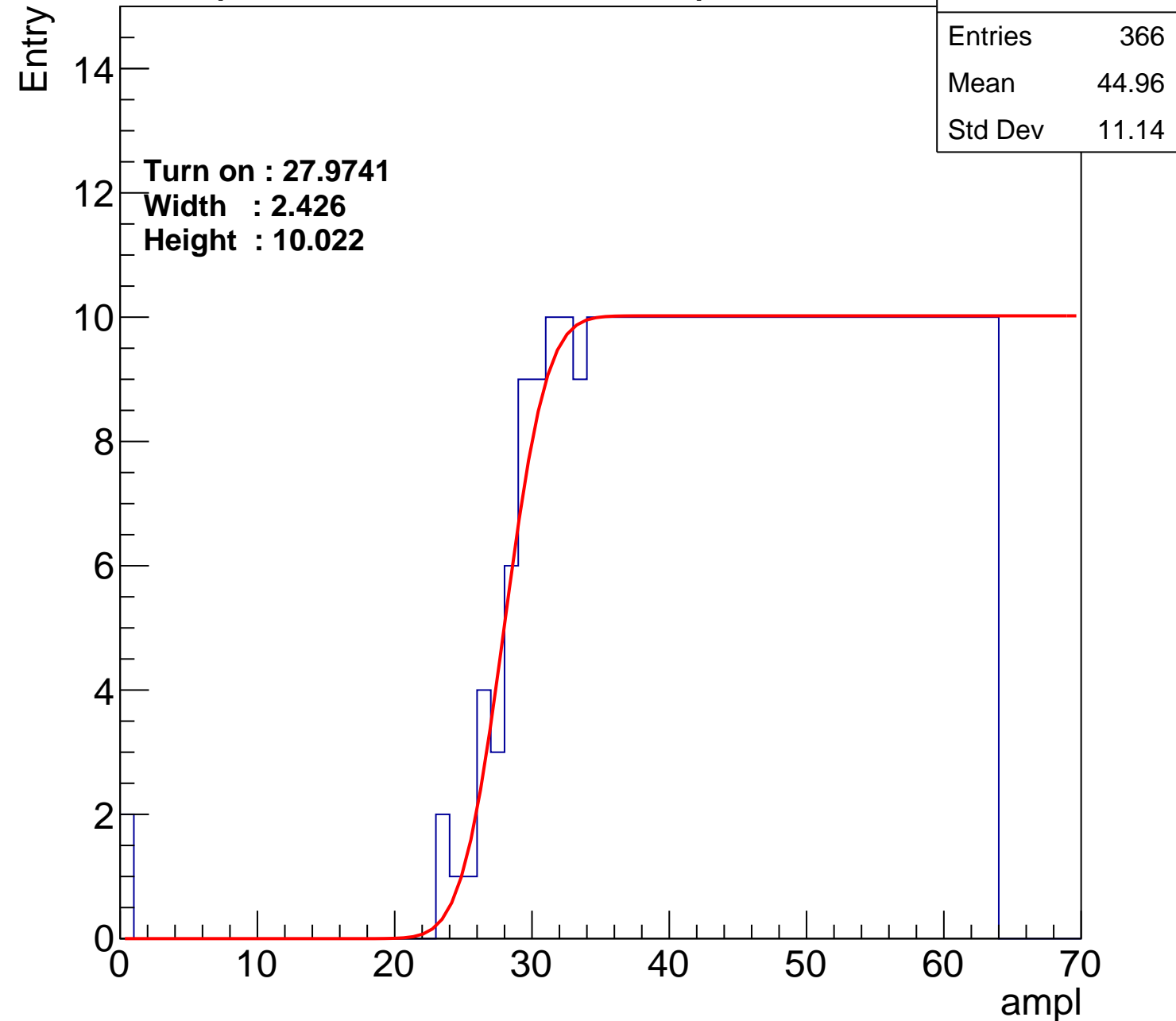
Width : 2.426

Height : 10.022

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U9-ch35

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	362
Mean	44.98
Std Dev	11.5

**Turn on : 28.4023**

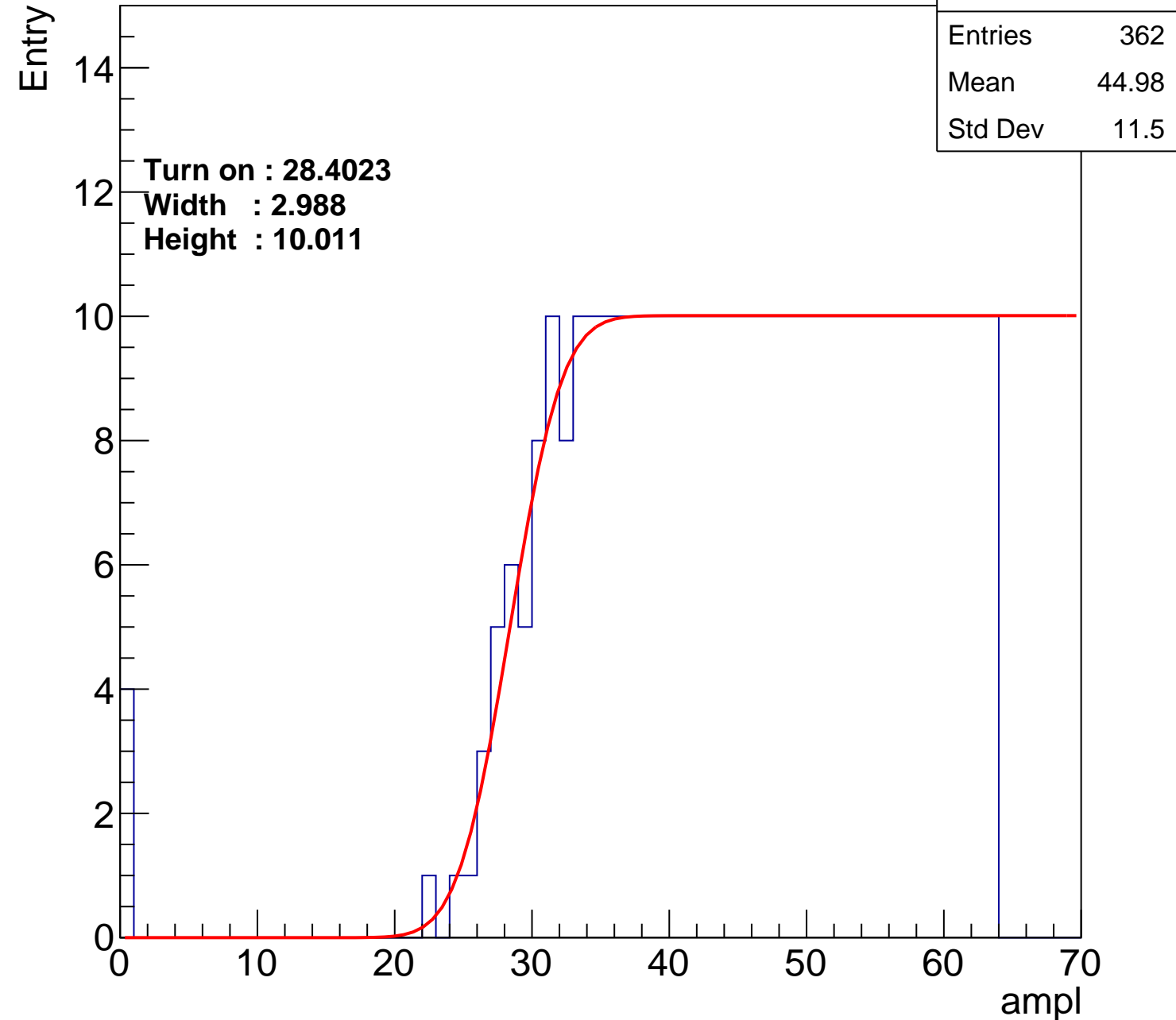
**Width : 2.988**

**Height : 10.011**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U9-ch36

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	348
Mean	45.76
Std Dev	10.83

**Turn on : 29.5422**

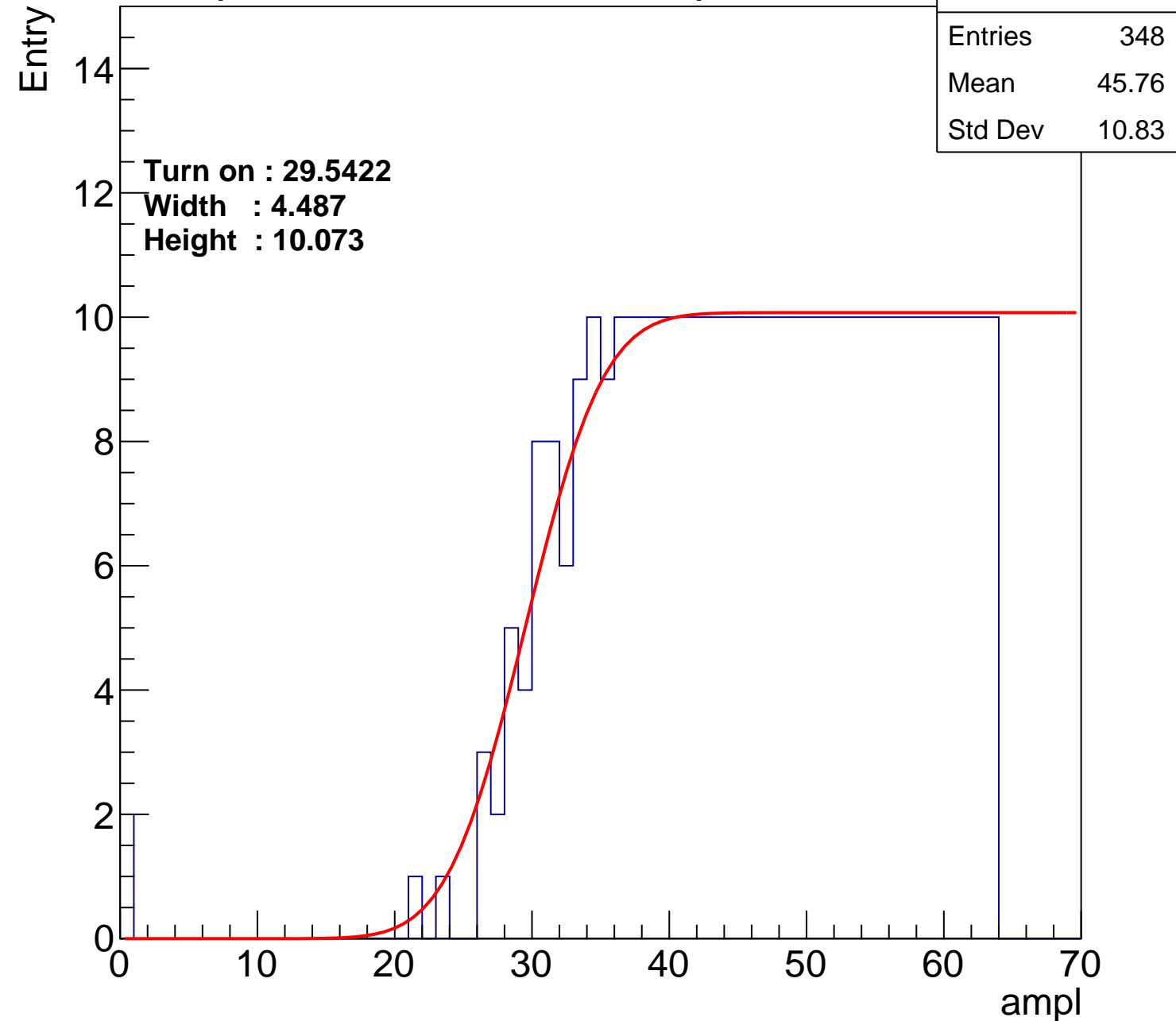
**Width : 4.487**

**Height : 10.073**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U9-ch37

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	360
Mean	45.17
Std Dev	11.23

**Turn on : 28.2994**

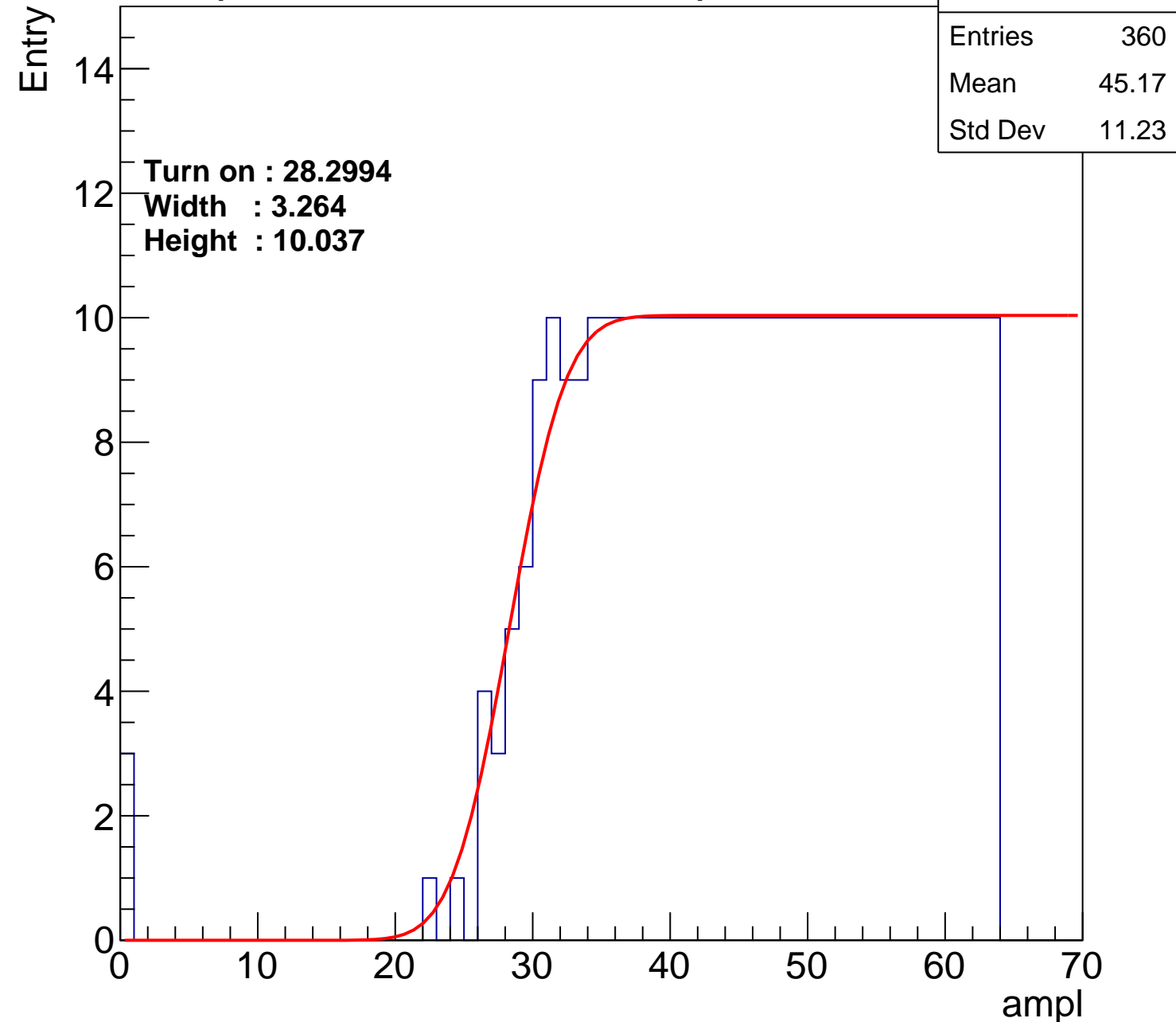
**Width : 3.264**

**Height : 10.037**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U9-ch38

calib\_packv5\_042523\_0143.root, FC#9, port A1

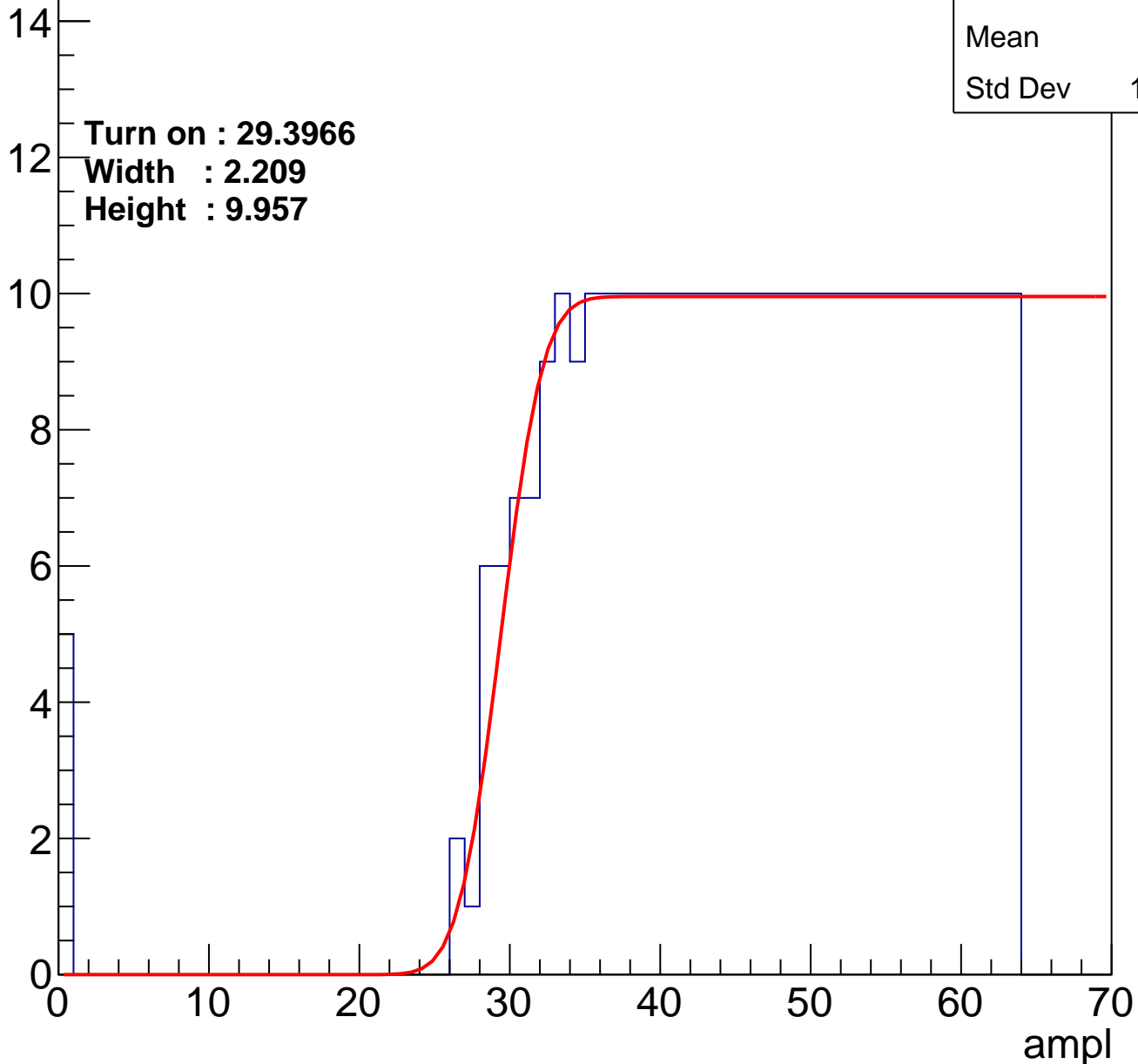
Entries	352
Mean	45.4
Std Dev	11.47

Turn on : 29.3966

Width : 2.209

Height : 9.957

Entry





# B0L001S, U9-ch39

calib\_packv5\_042523\_0143.root, FC#9, port A1

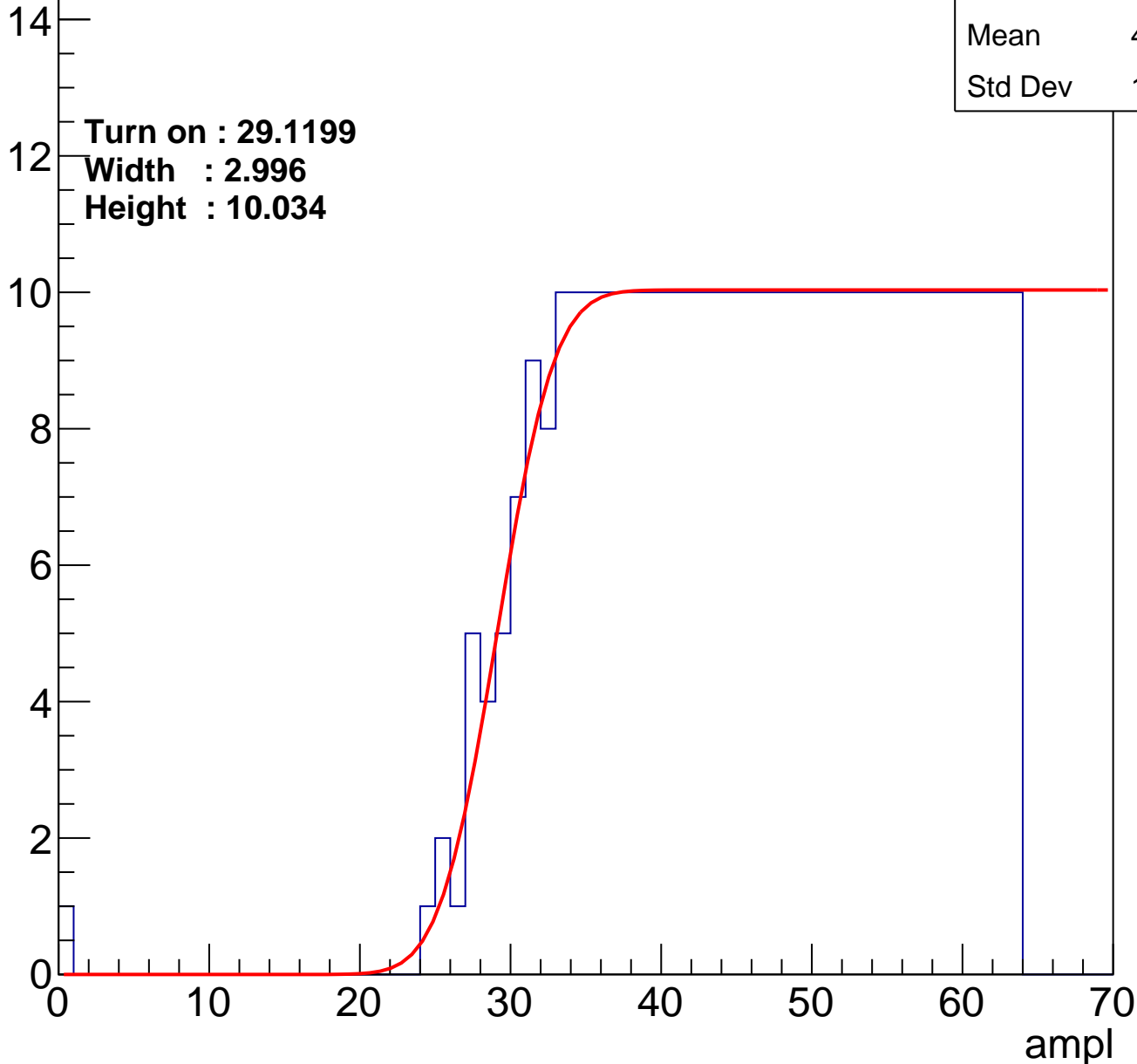
Entries	353
Mean	45.66
Std Dev	10.62

**Turn on : 29.1199**

**Width : 2.996**

**Height : 10.034**

Entry



# B0L001S, U9-ch40

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	372
Mean	44.66
Std Dev	11.3

**Turn on : 26.9174**

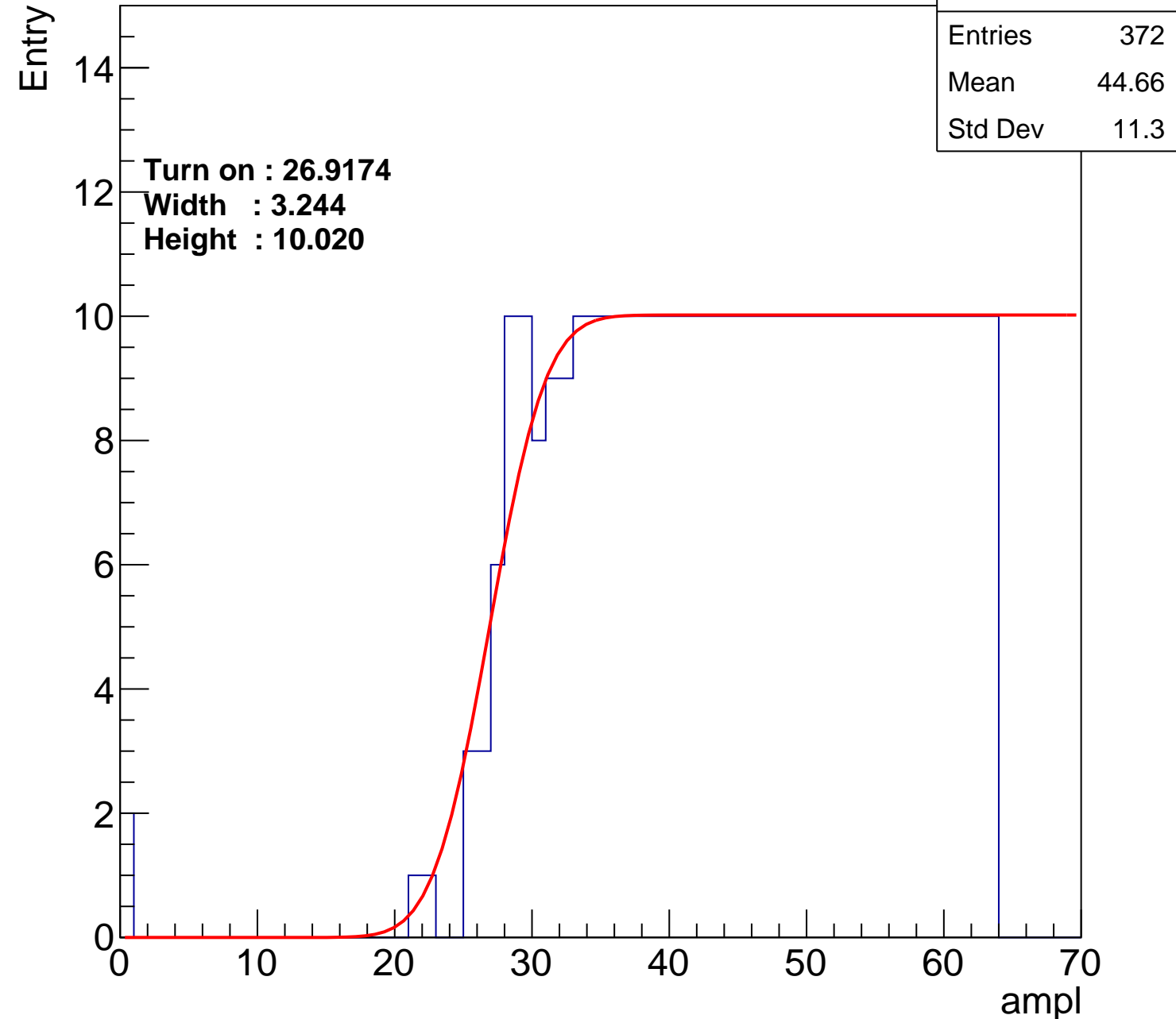
**Width : 3.244**

**Height : 10.020**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U9-ch41

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	356
Mean	45.26
Std Dev	11.4

Turn on : 29.0547

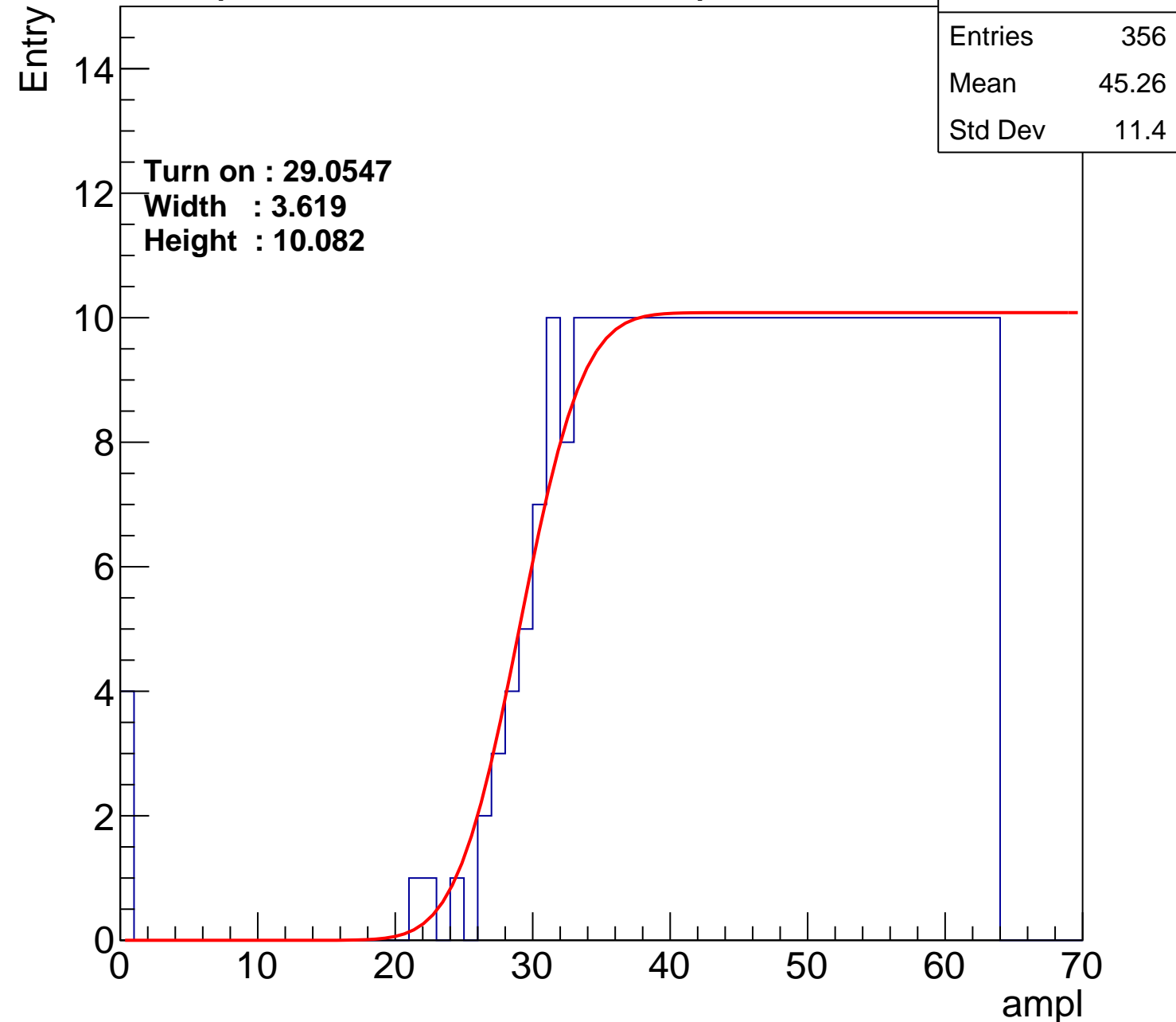
Width : 3.619

Height : 10.082

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U9-ch42

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	352
Mean	45.52
Std Dev	11.2

**Turn on : 29.0217**

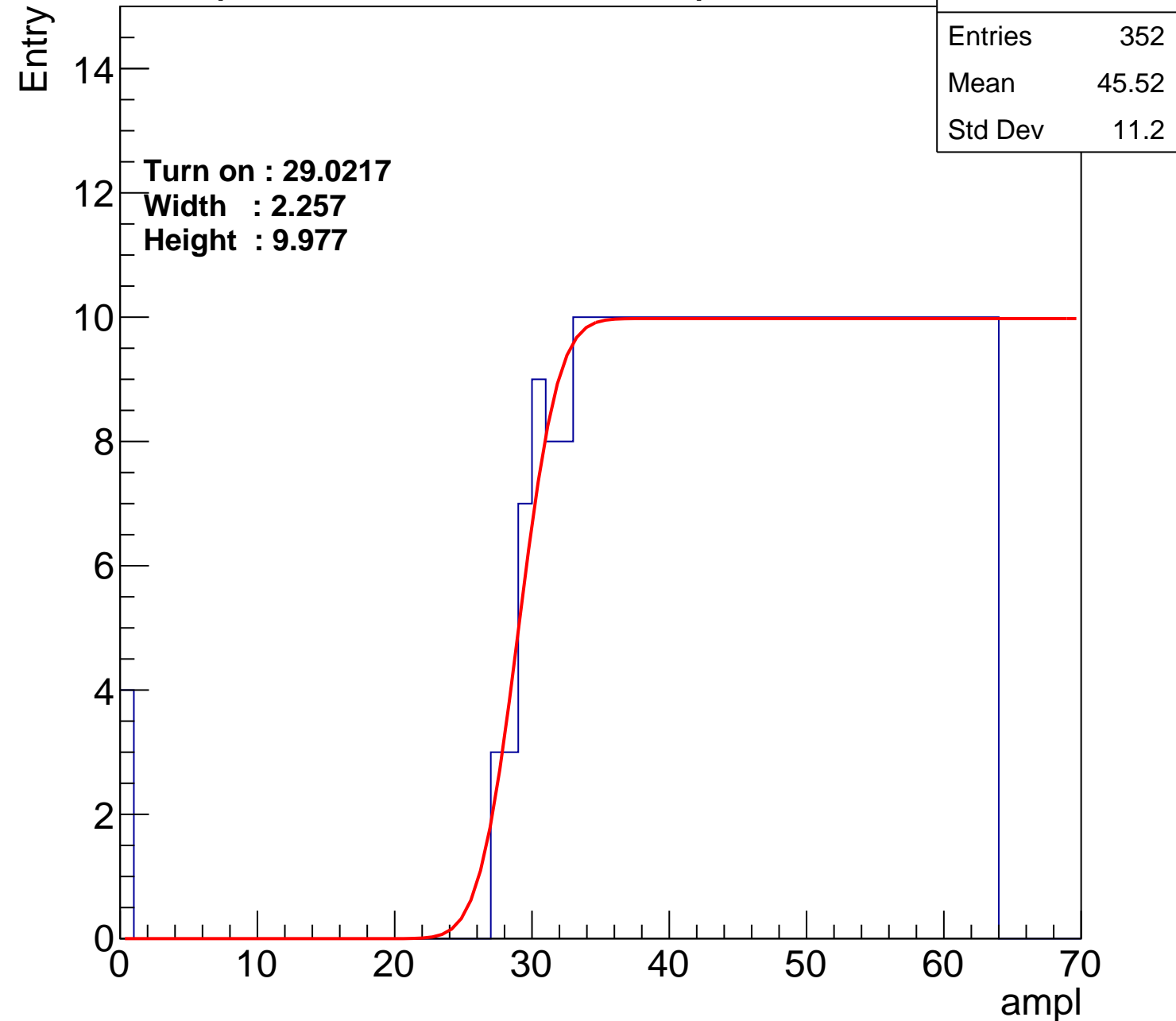
**Width : 2.257**

**Height : 9.977**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U9-ch43

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	363
Mean	45.18
Std Dev	10.86

Turn on : 28.4025

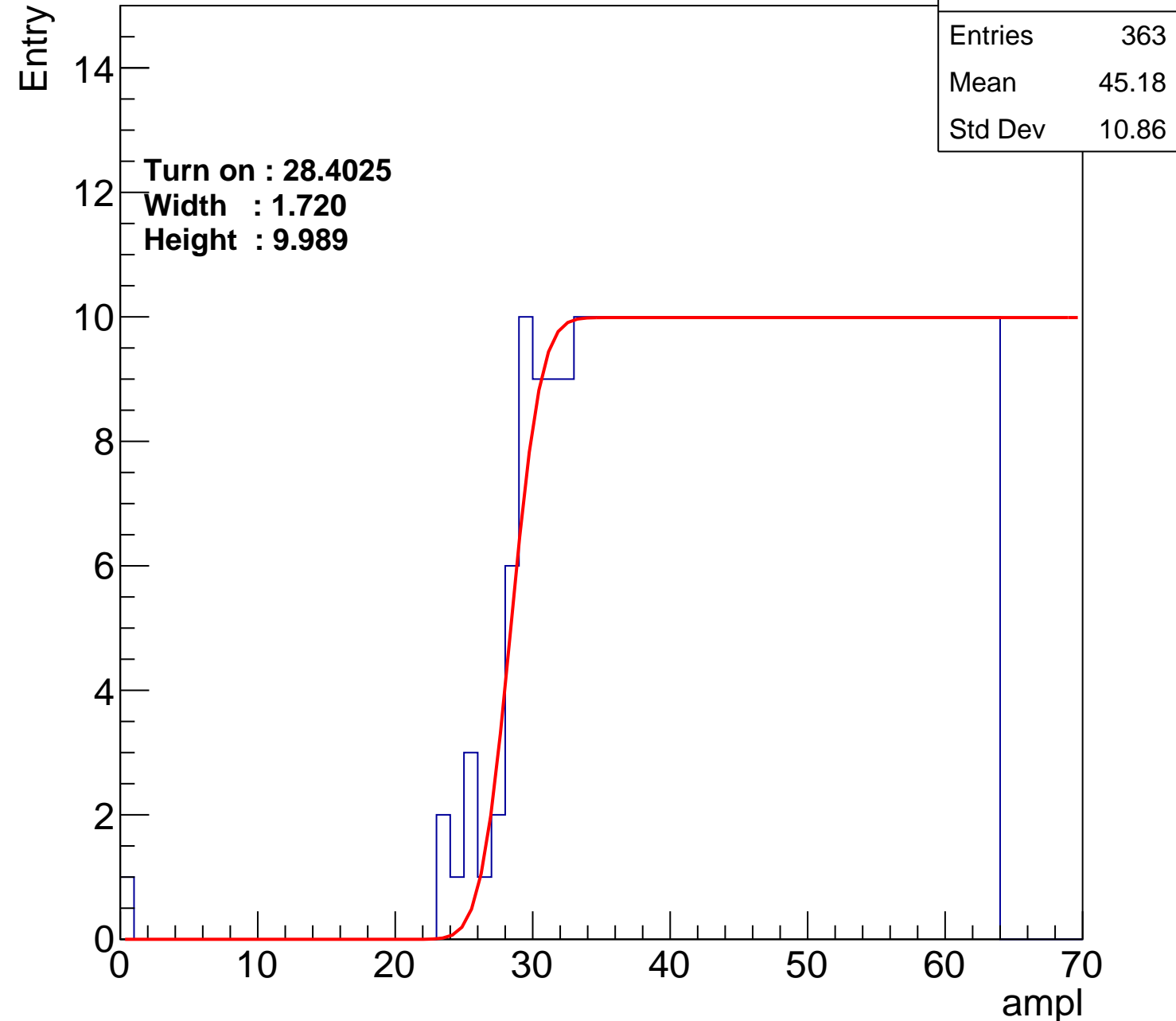
Width : 1.720

Height : 9.989

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U9-ch44

**calib\_packv5\_042523\_0143.root, FC#9, port A1**

Entries	375
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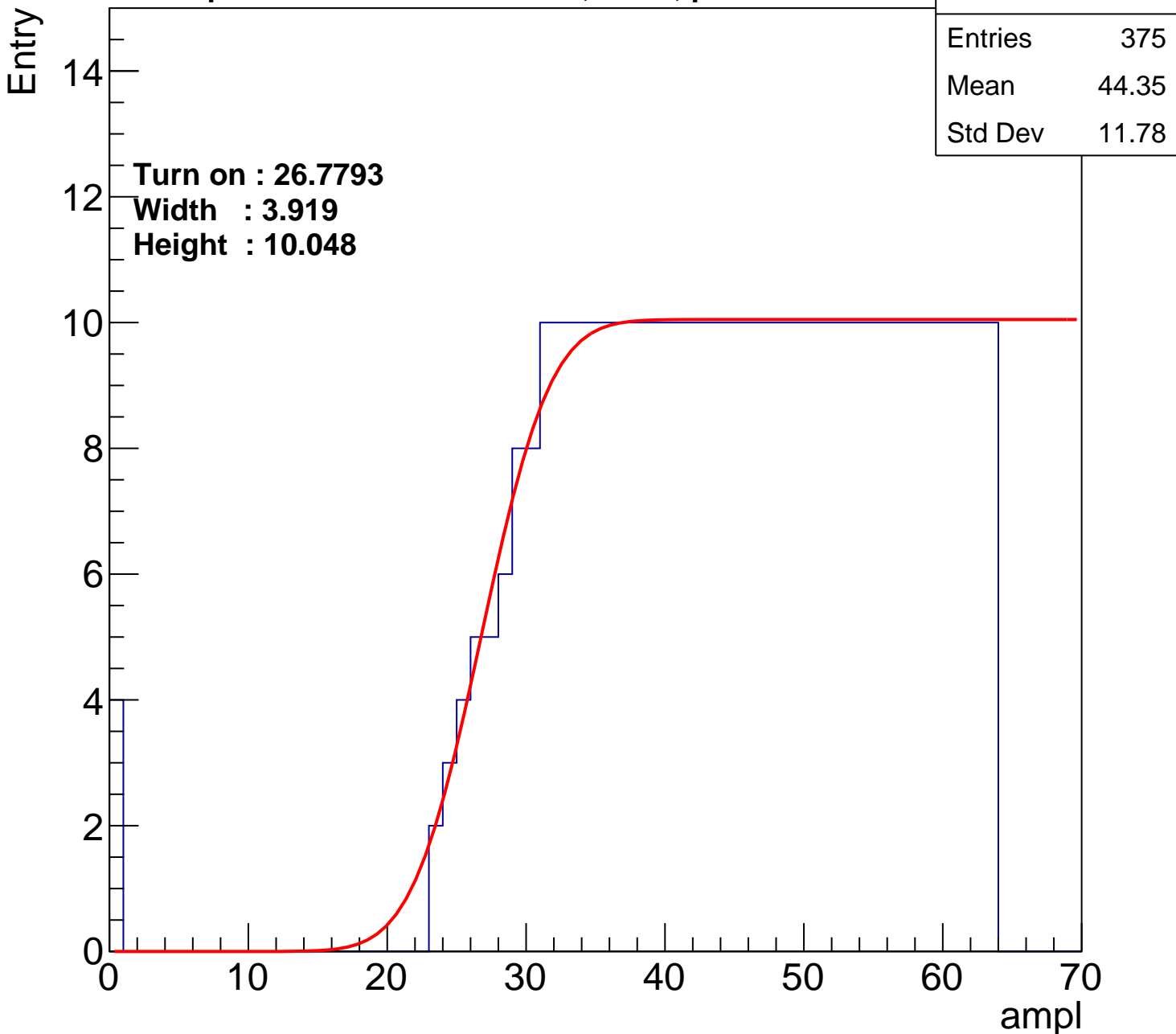
Mean	44.35
------	-------

Std Dev	11.78
---------	-------

**Turn on : 26.7793**

**Width : 3.919**

**Height : 10.048**



# B0L001S, U9-ch45

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	373
Mean	44.67
Std Dev	11.15

Turn on : 26.7724

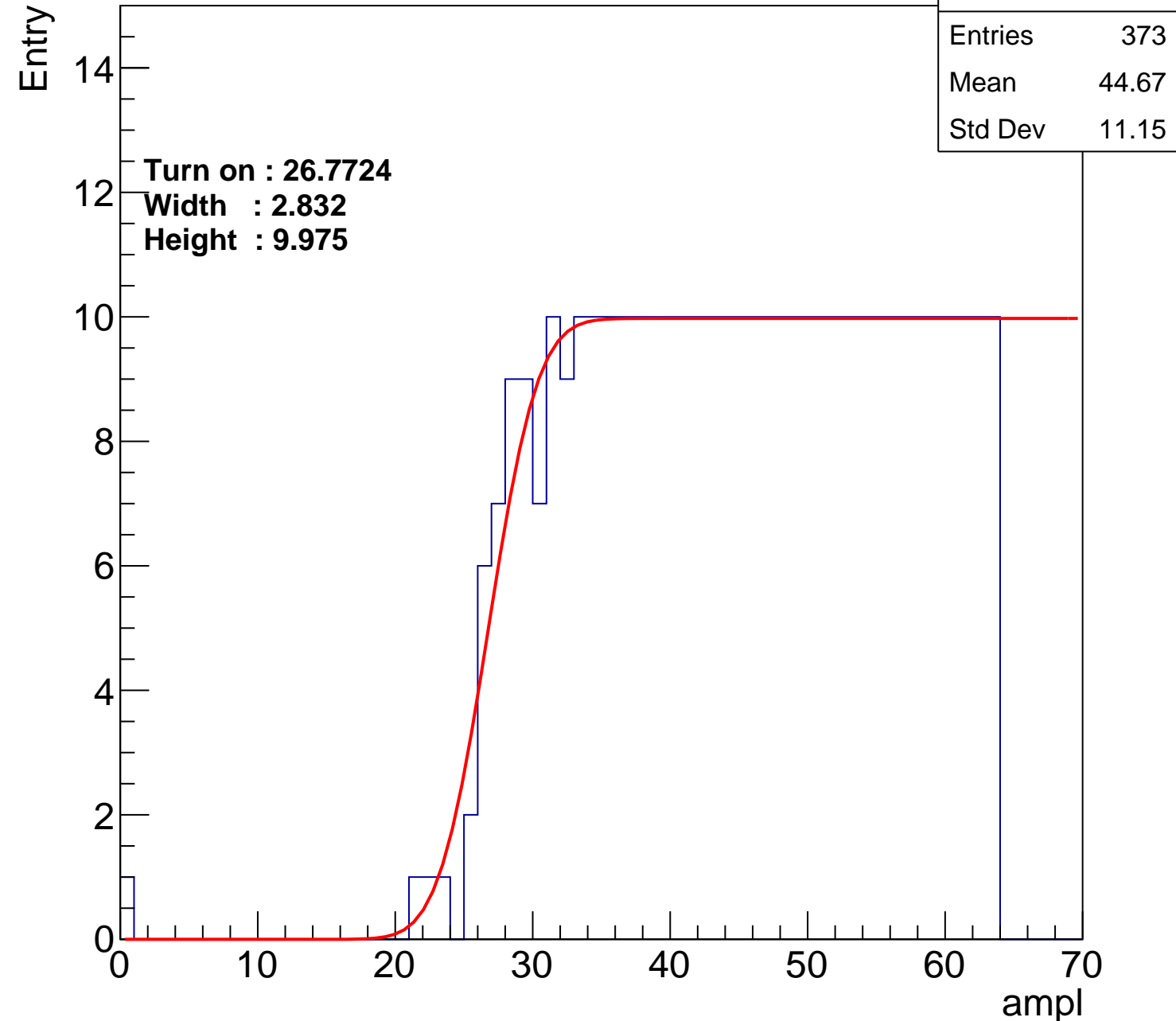
Width : 2.832

Height : 9.975

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U9-ch46

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	365
Mean	44.81
Std Dev	11.7

**Turn on : 28.0659**

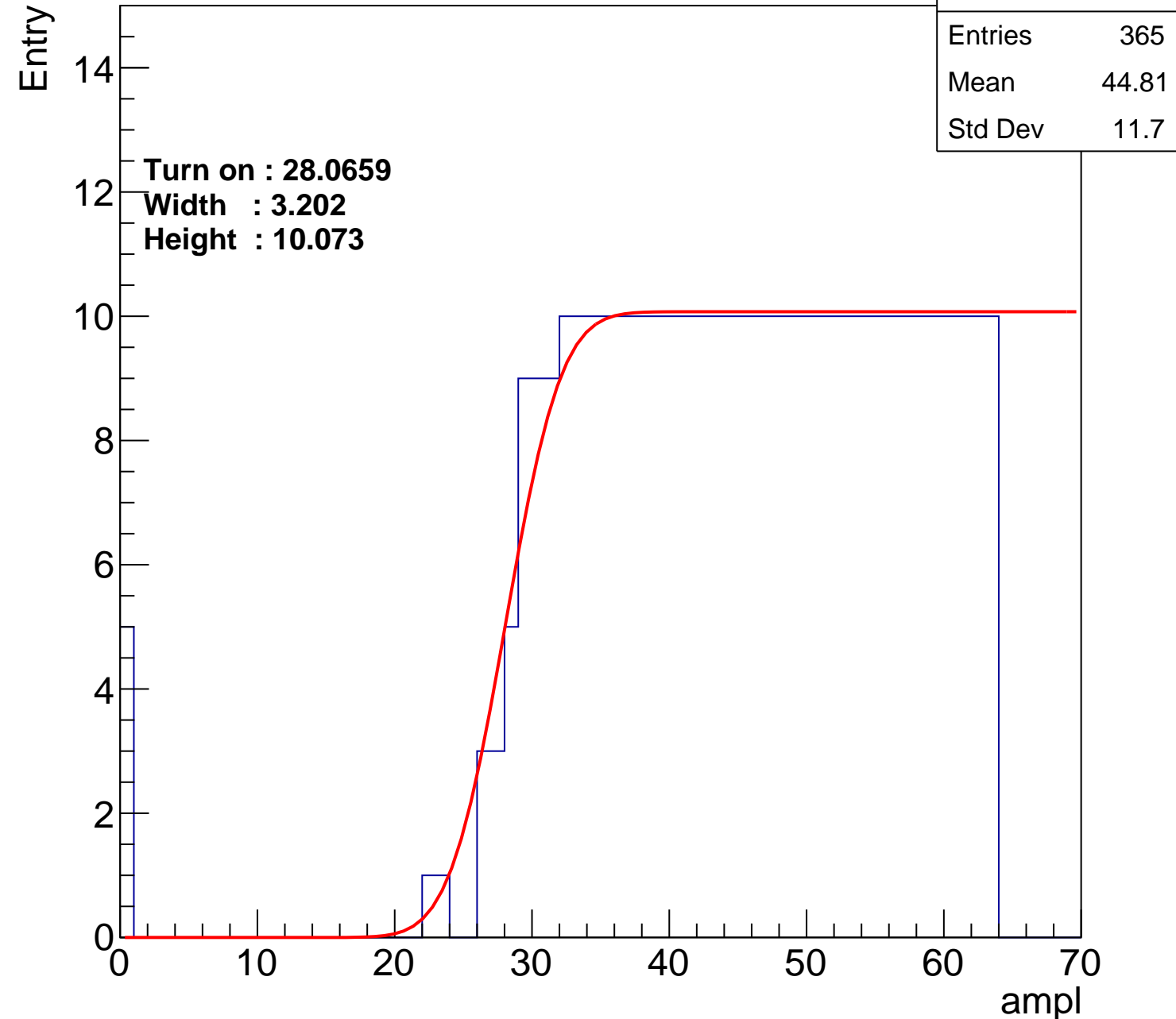
**Width : 3.202**

**Height : 10.073**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B0L001S, U9-ch47

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	367
Mean	44.92
Std Dev	11.07

Turn on : 27.5158

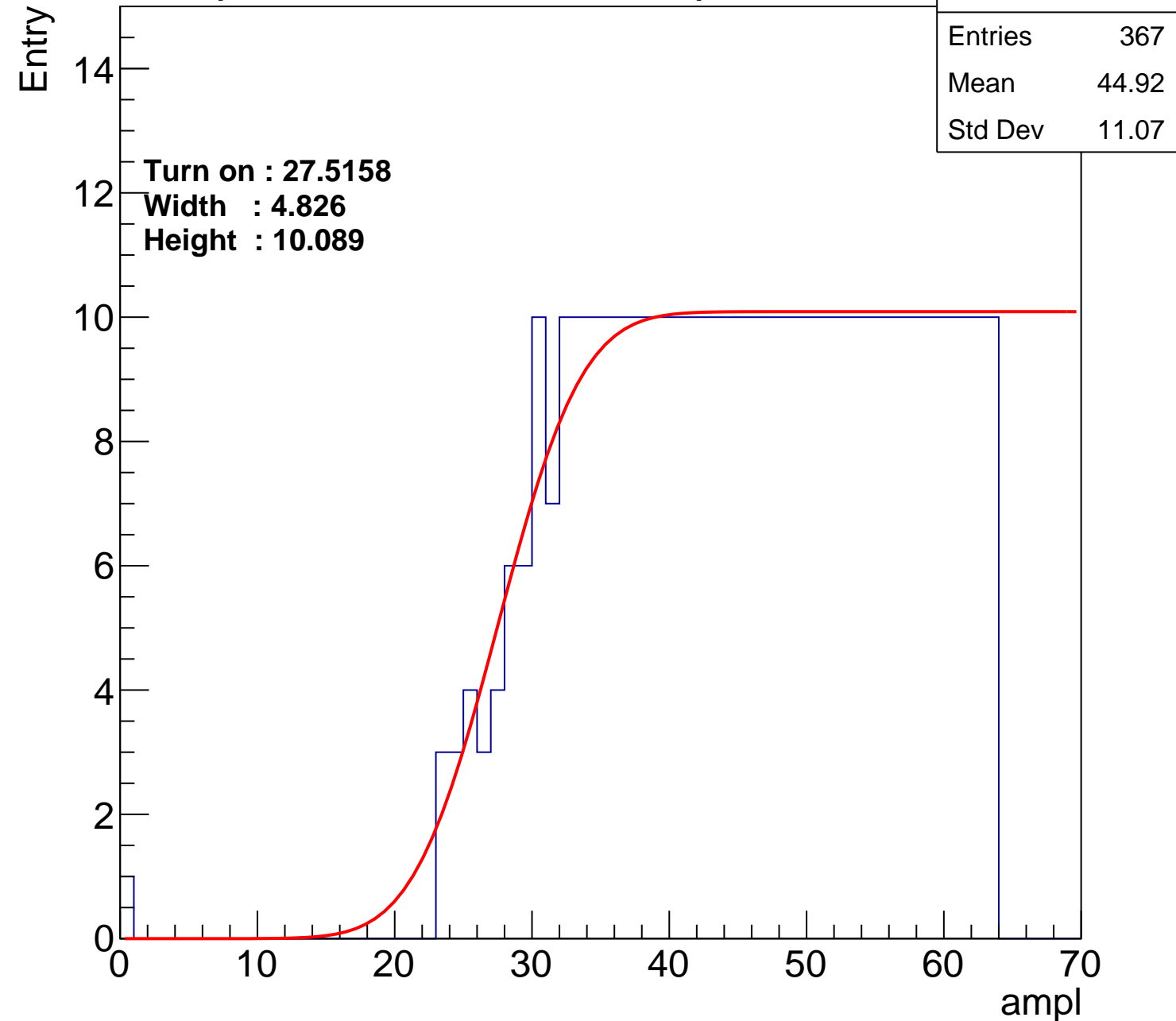
Width : 4.826

Height : 10.089

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U9-ch48

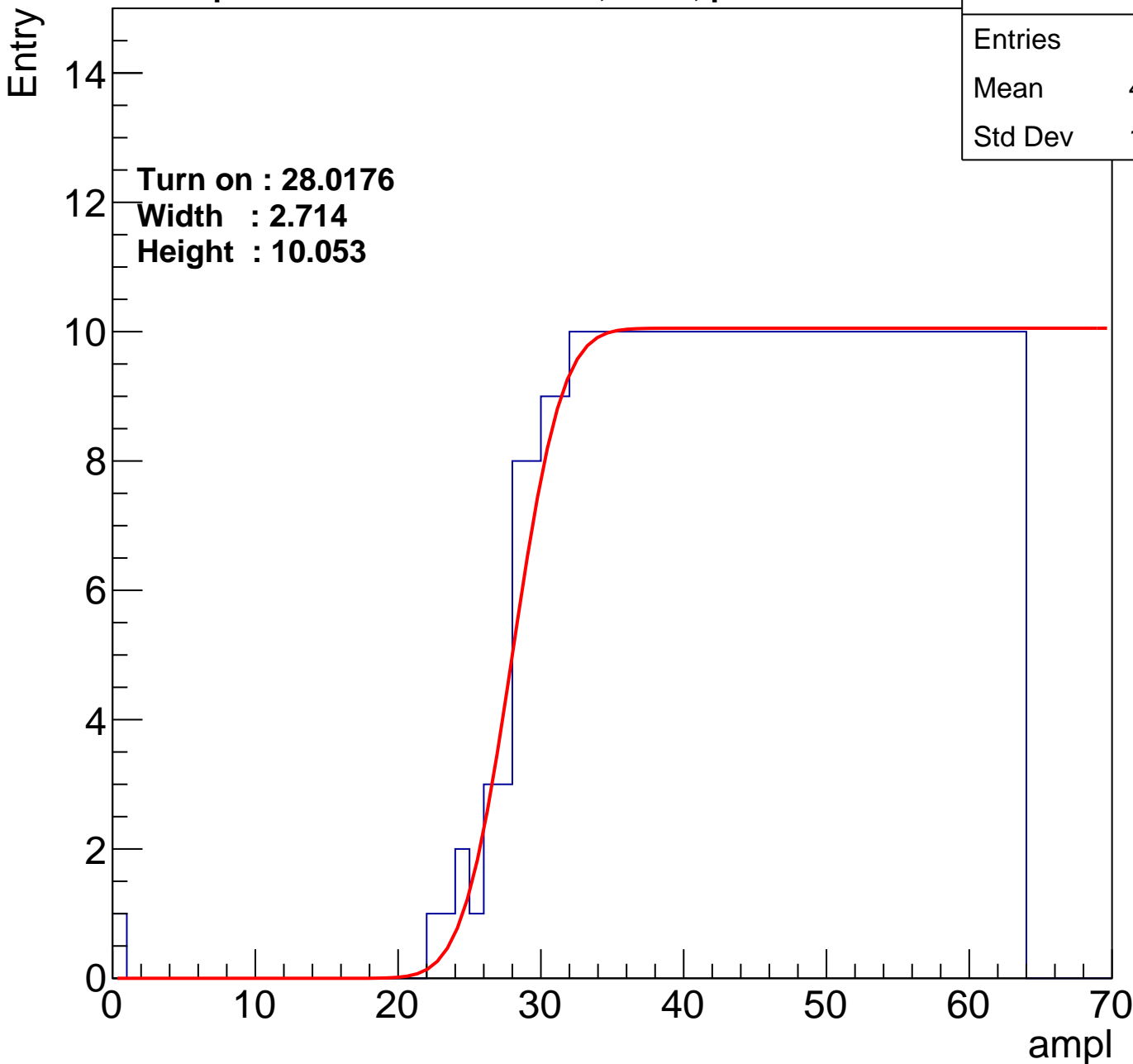
**calib\_packv5\_042523\_0143.root, FC#9, port A1**

Entries	366
Mean	45.03
Std Dev	10.94

**Turn on : 28.0176**

**Width : 2.714**

**Height : 10.053**



# B0L001S, U9-ch49

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	352
Mean	45.57
Std Dev	11.02

**Turn on : 29.0053**

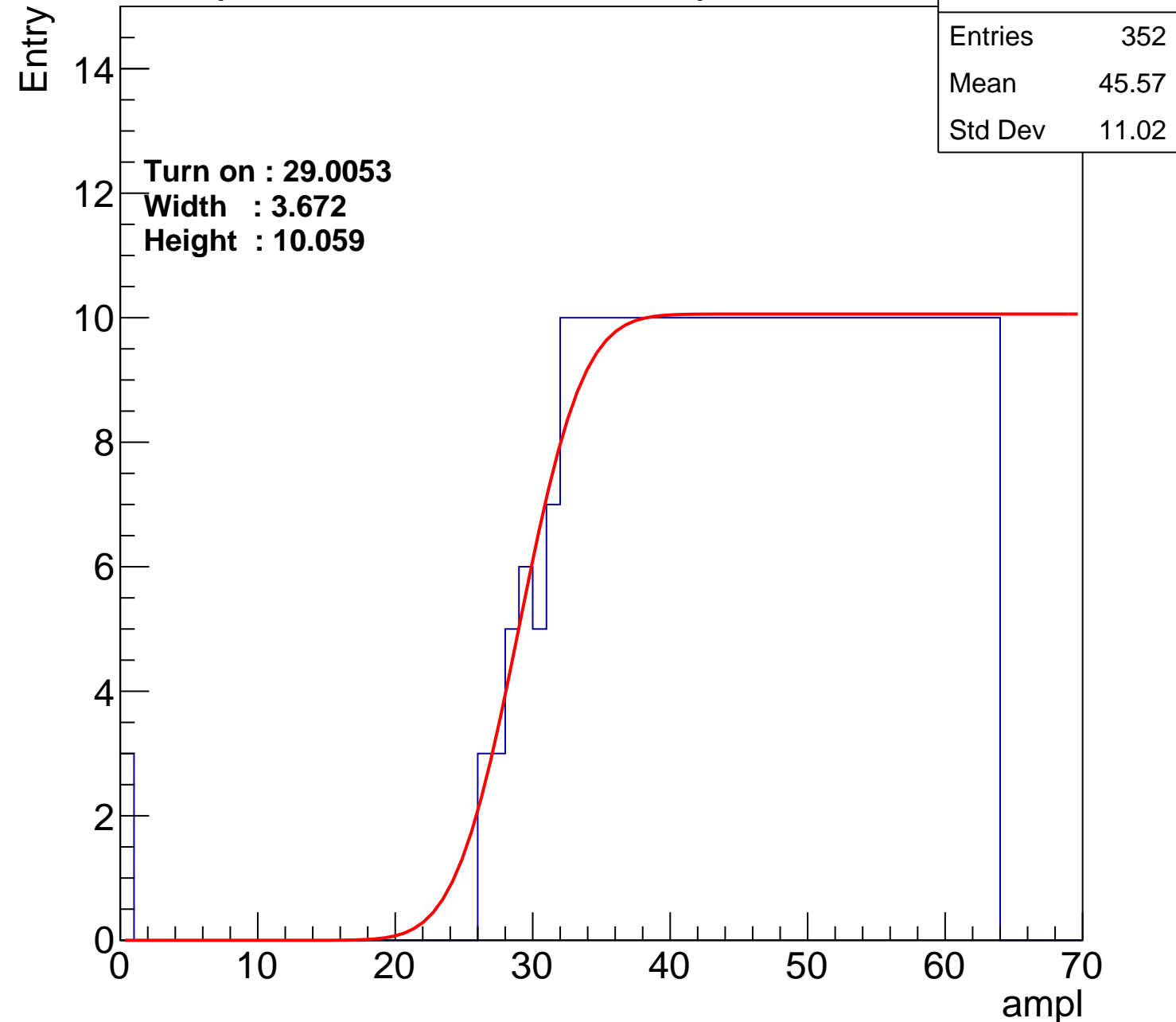
**Width : 3.672**

**Height : 10.059**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U9-ch50

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	379
Mean	44.25
Std Dev	11.66

Turn on : 26.6106

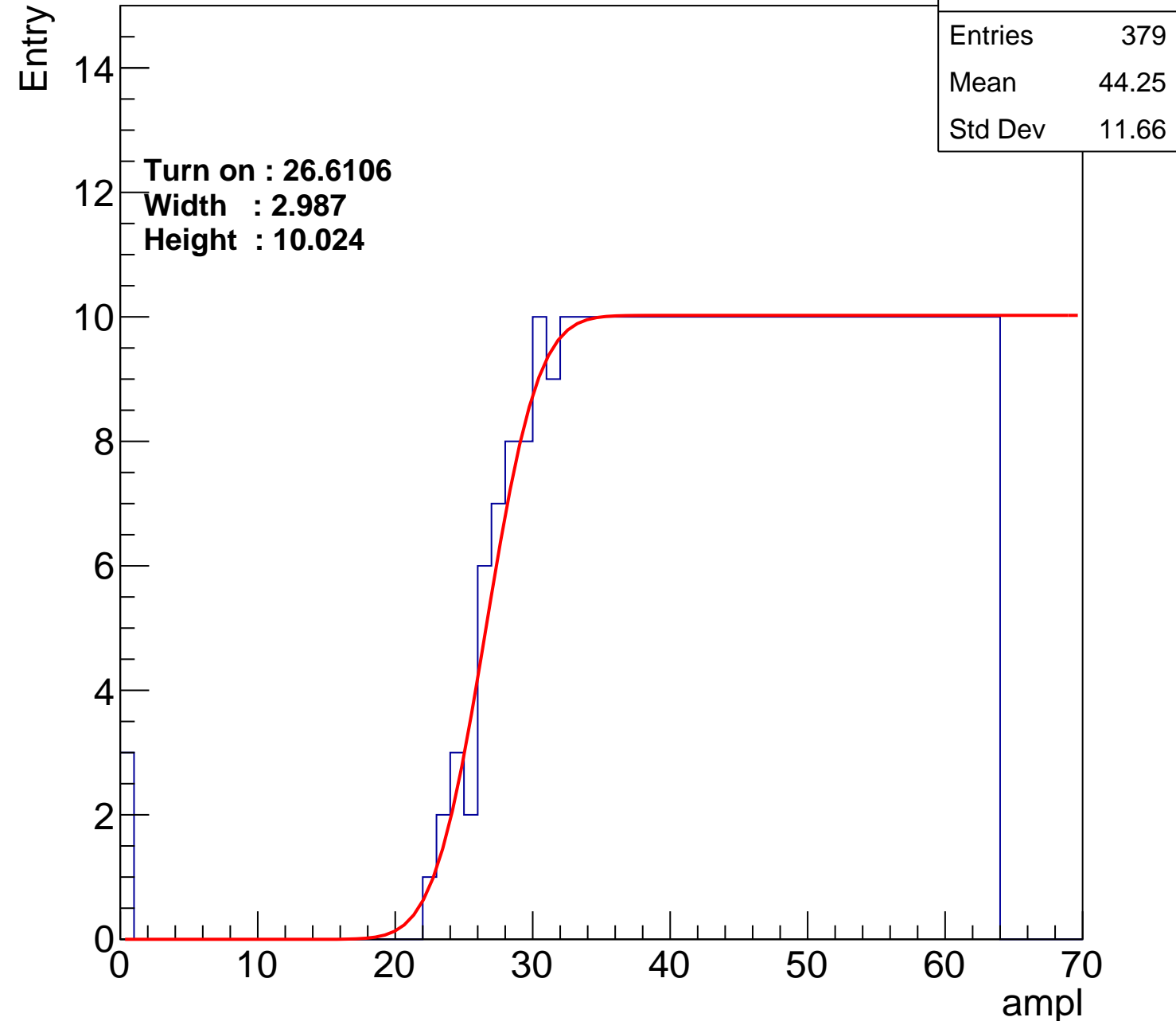
Width : 2.987

Height : 10.024

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U9-ch51

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	352
Mean	45.62
Std Dev	10.84

**Turn on : 28.8974**

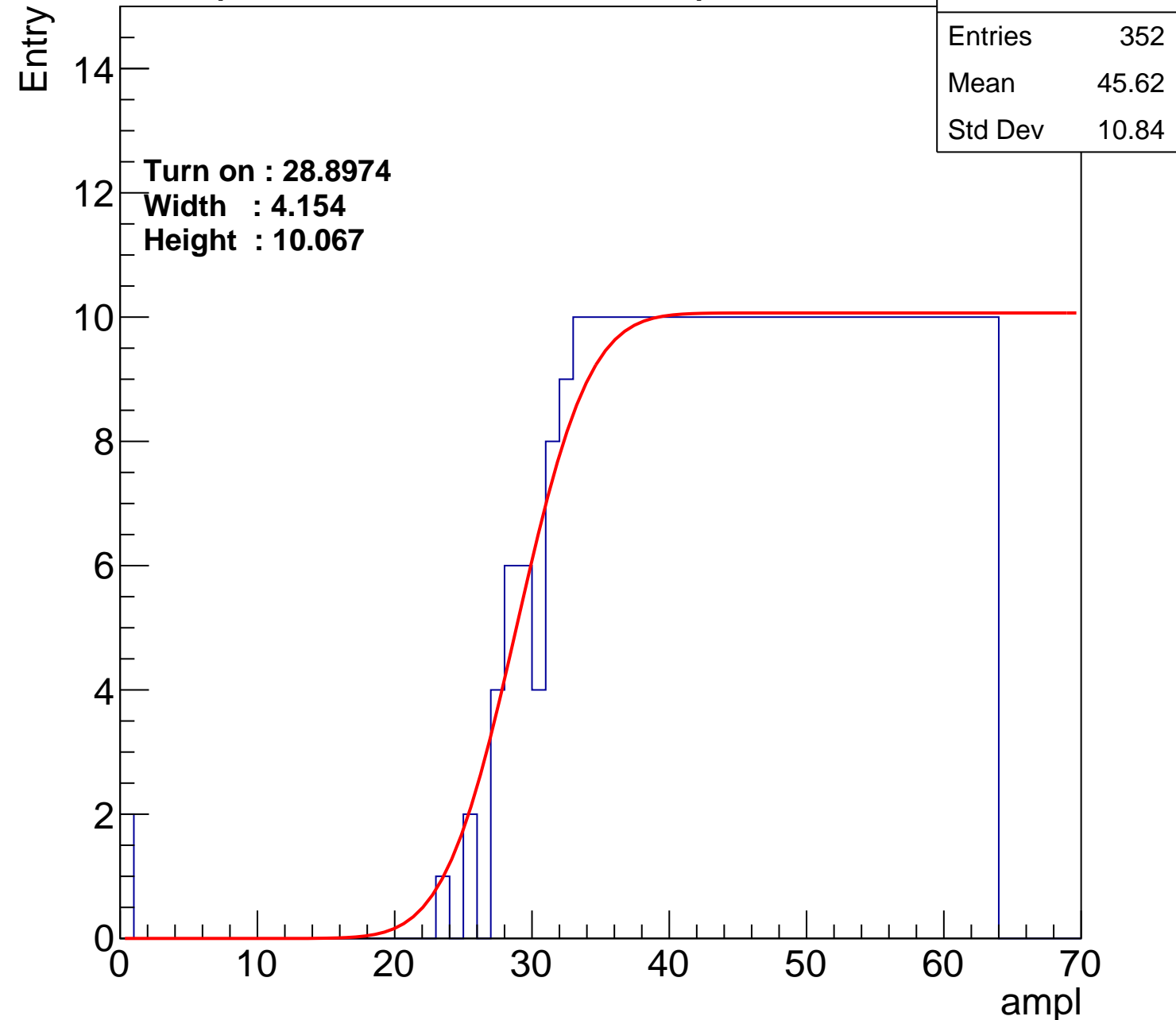
**Width : 4.154**

**Height : 10.067**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U9-ch52

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	354
Mean	45.42
Std Dev	11.15

**Turn on : 28.9199**

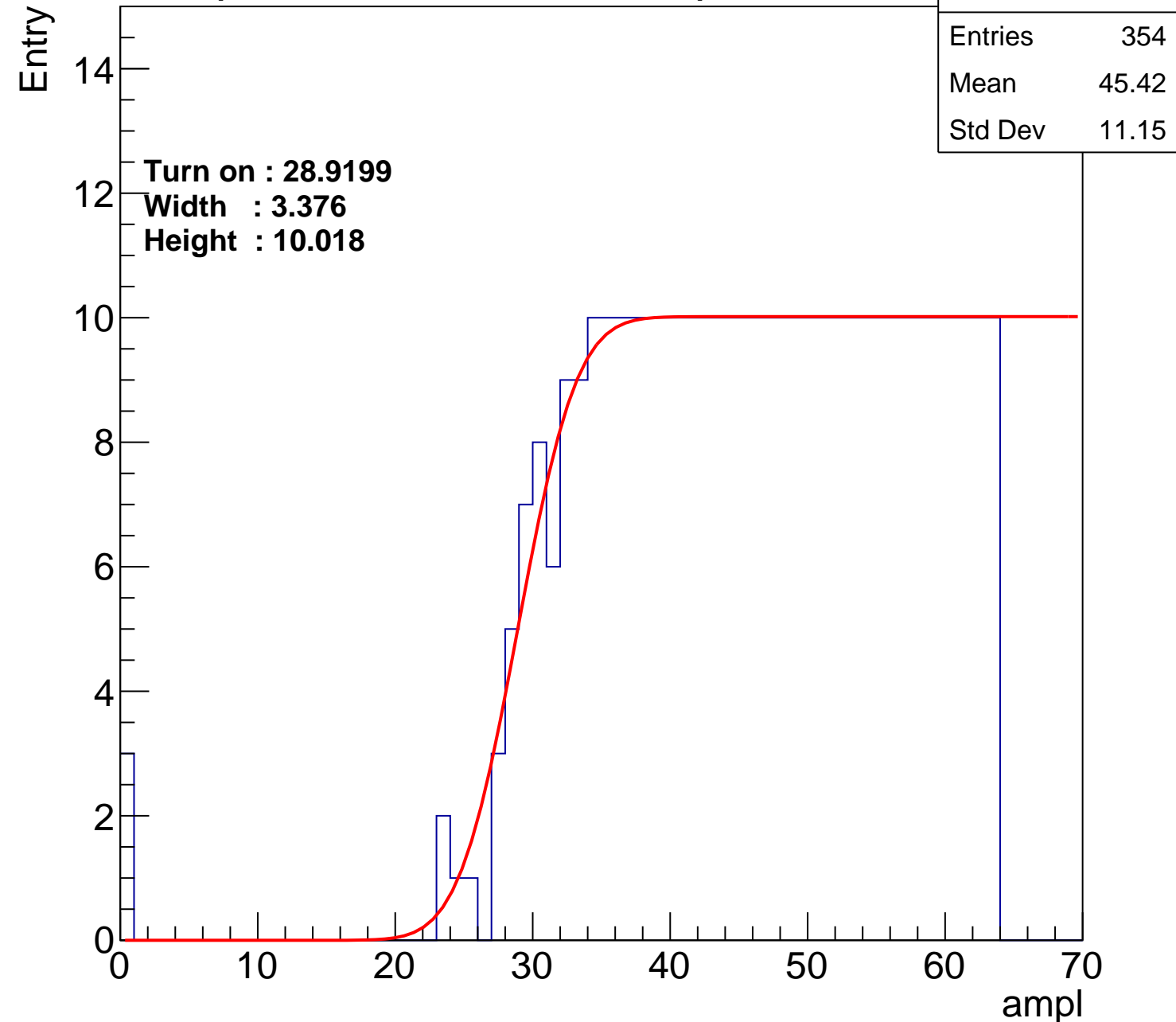
**Width : 3.376**

**Height : 10.018**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U9-ch53

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	346
Mean	45.92
Std Dev	10.68

Turn on : 29.4383

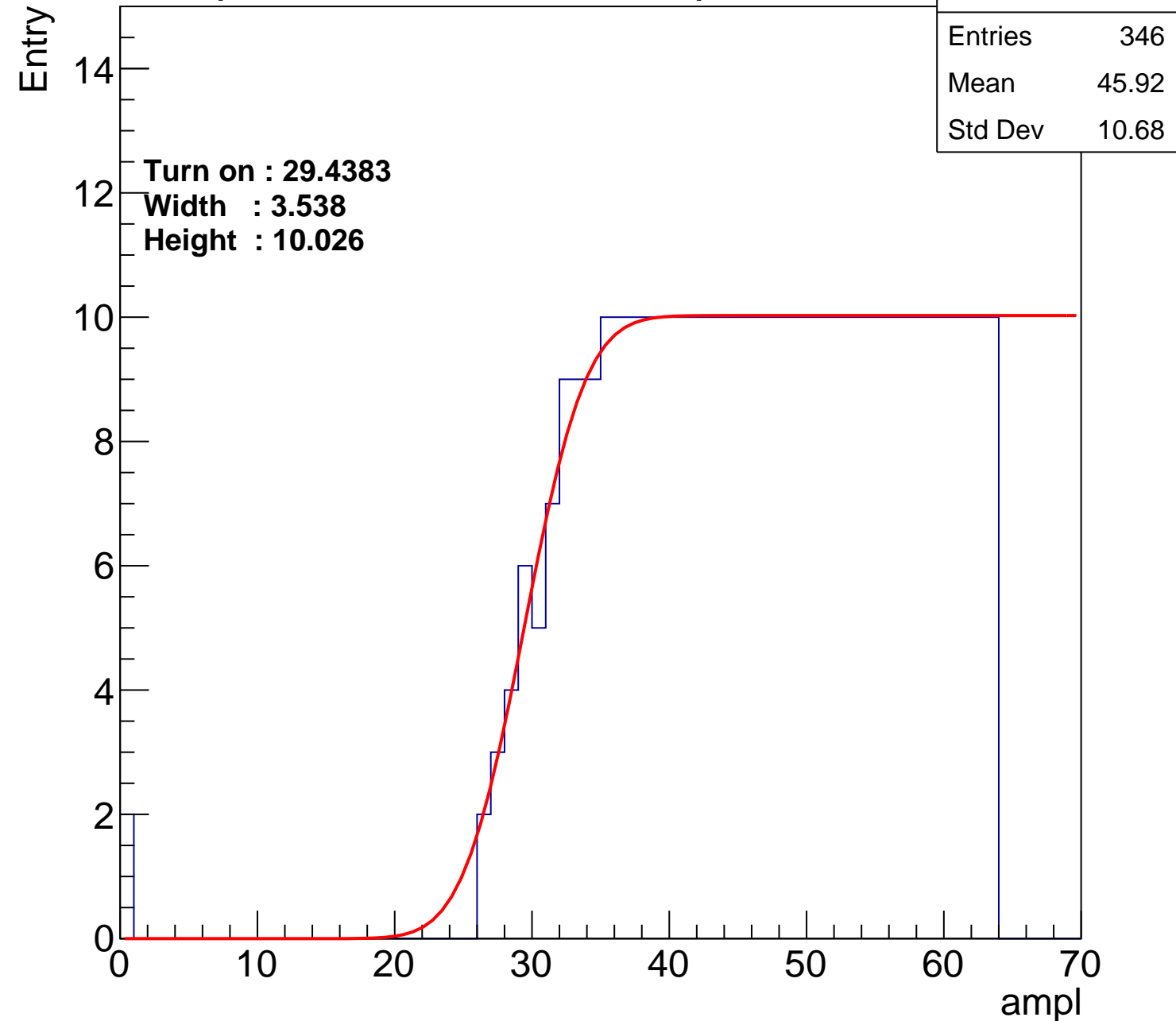
Width : 3.538

Height : 10.026

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U9-ch54

calib\_packv5\_042523\_0143.root, FC#9, port A1

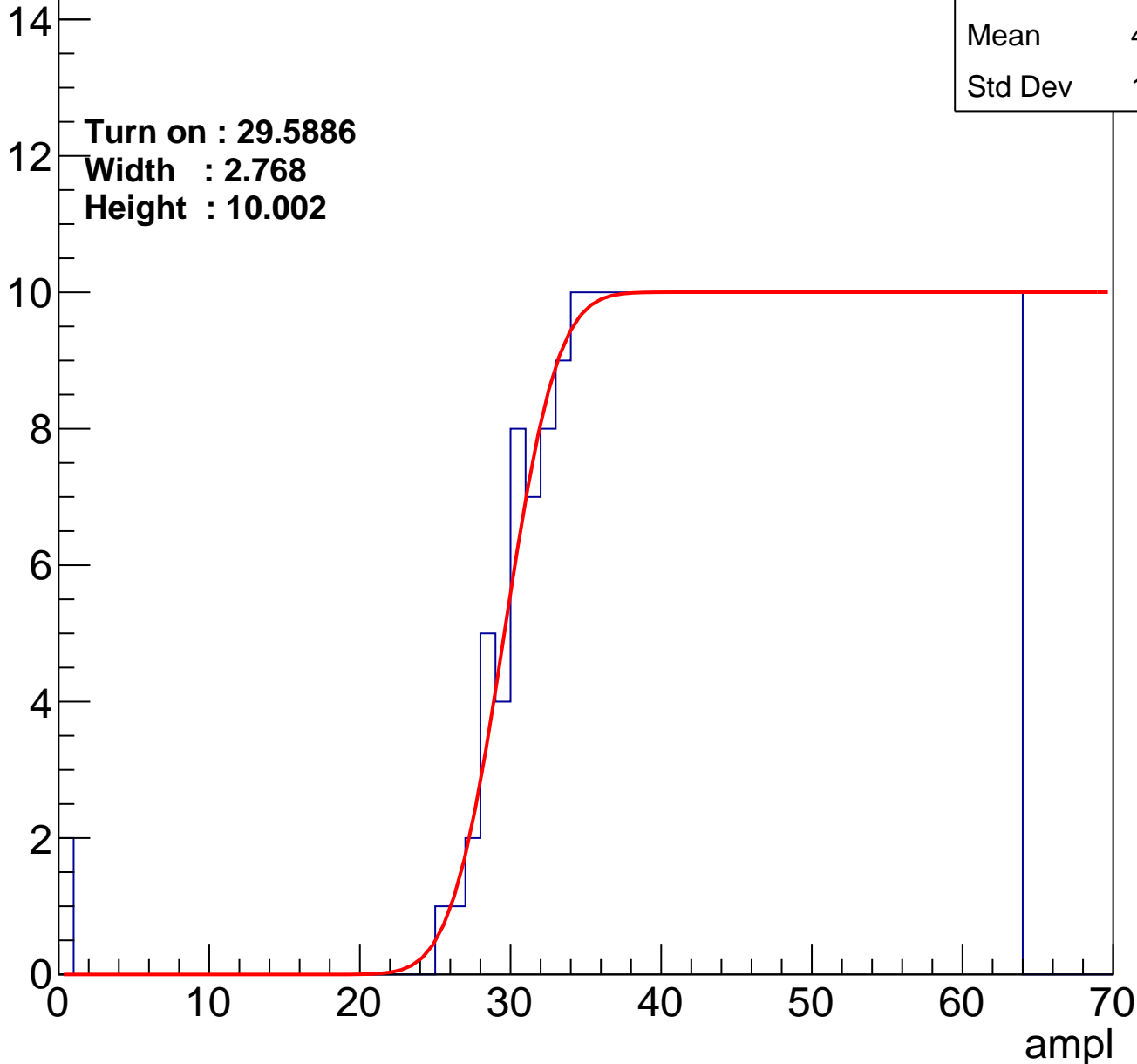
Entries	347
Mean	45.88
Std Dev	10.69

Turn on : 29.5886

Width : 2.768

Height : 10.002

Entry





# B0L001S, U9-ch55

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	373
Mean	44.65
Std Dev	11.19

Turn on : 28.1990

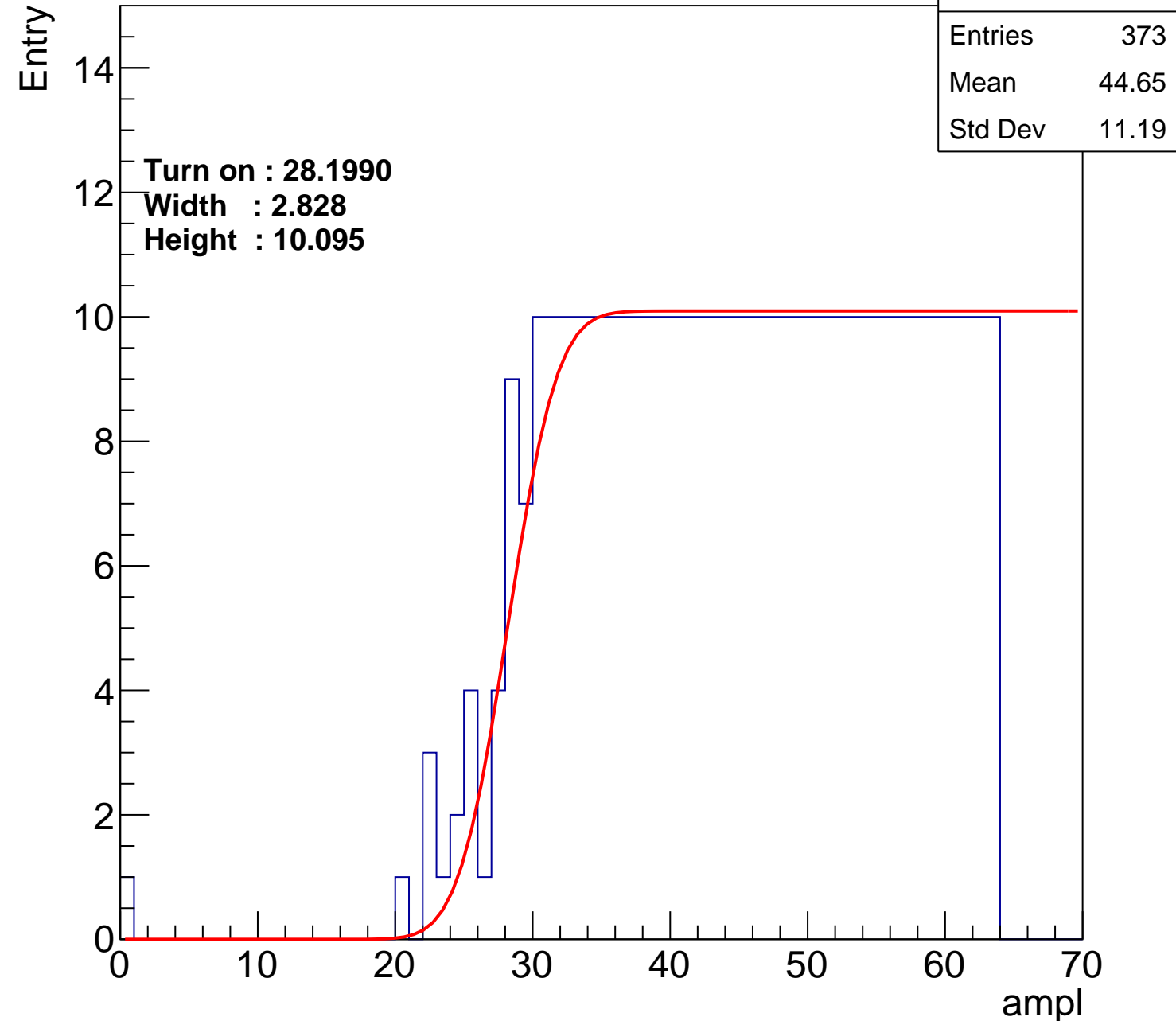
Width : 2.828

Height : 10.095

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U9-ch56

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	369
Mean	44.85
Std Dev	11.17

**Turn on : 27.2859**

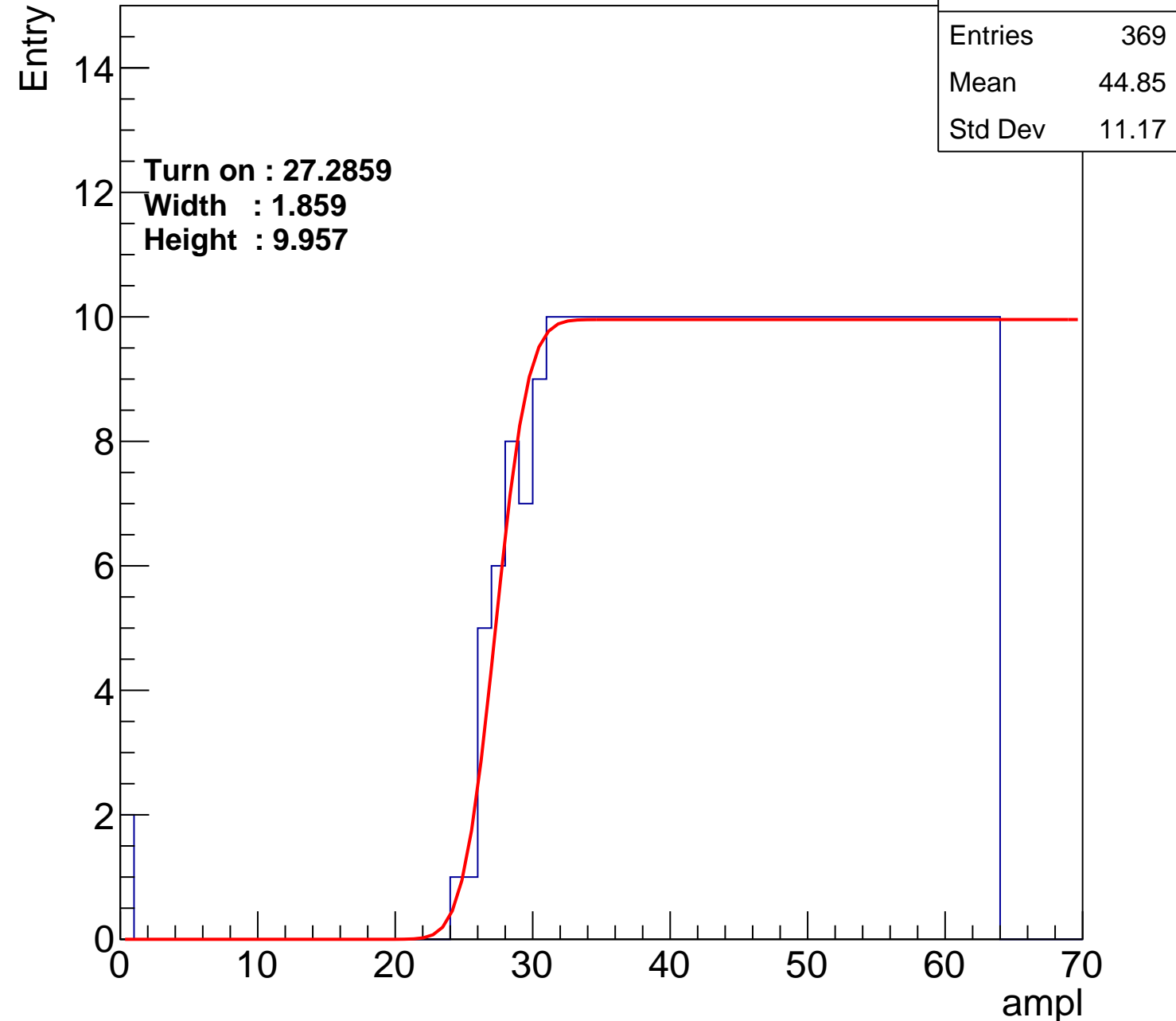
**Width : 1.859**

**Height : 9.957**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U9-ch57

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	341
Mean	46.06
Std Dev	10.85

Turn on : 30.6738

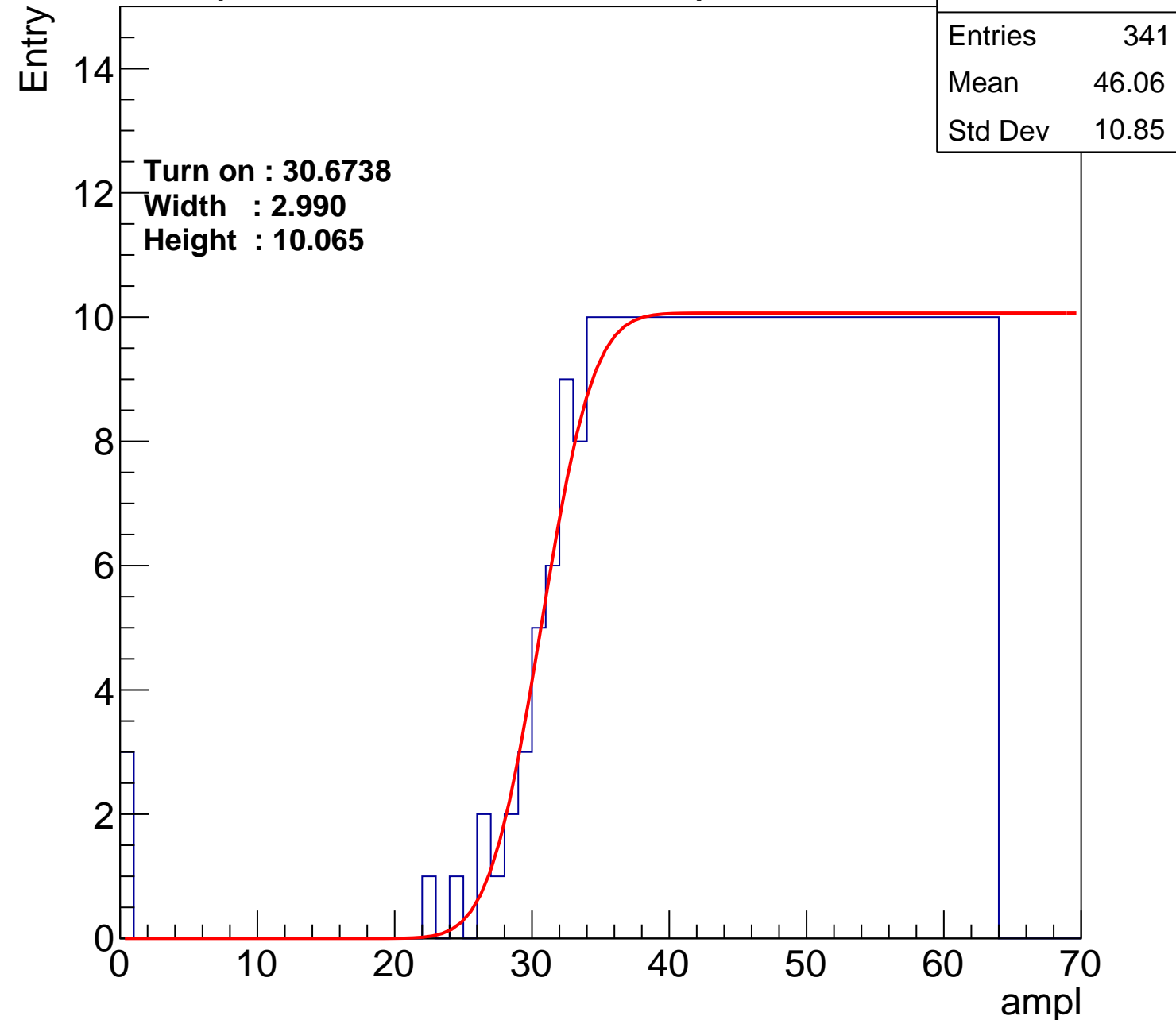
Width : 2.990

Height : 10.065

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U9-ch58

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	362
Mean	45.21
Std Dev	10.86

Turn on : 28.2214

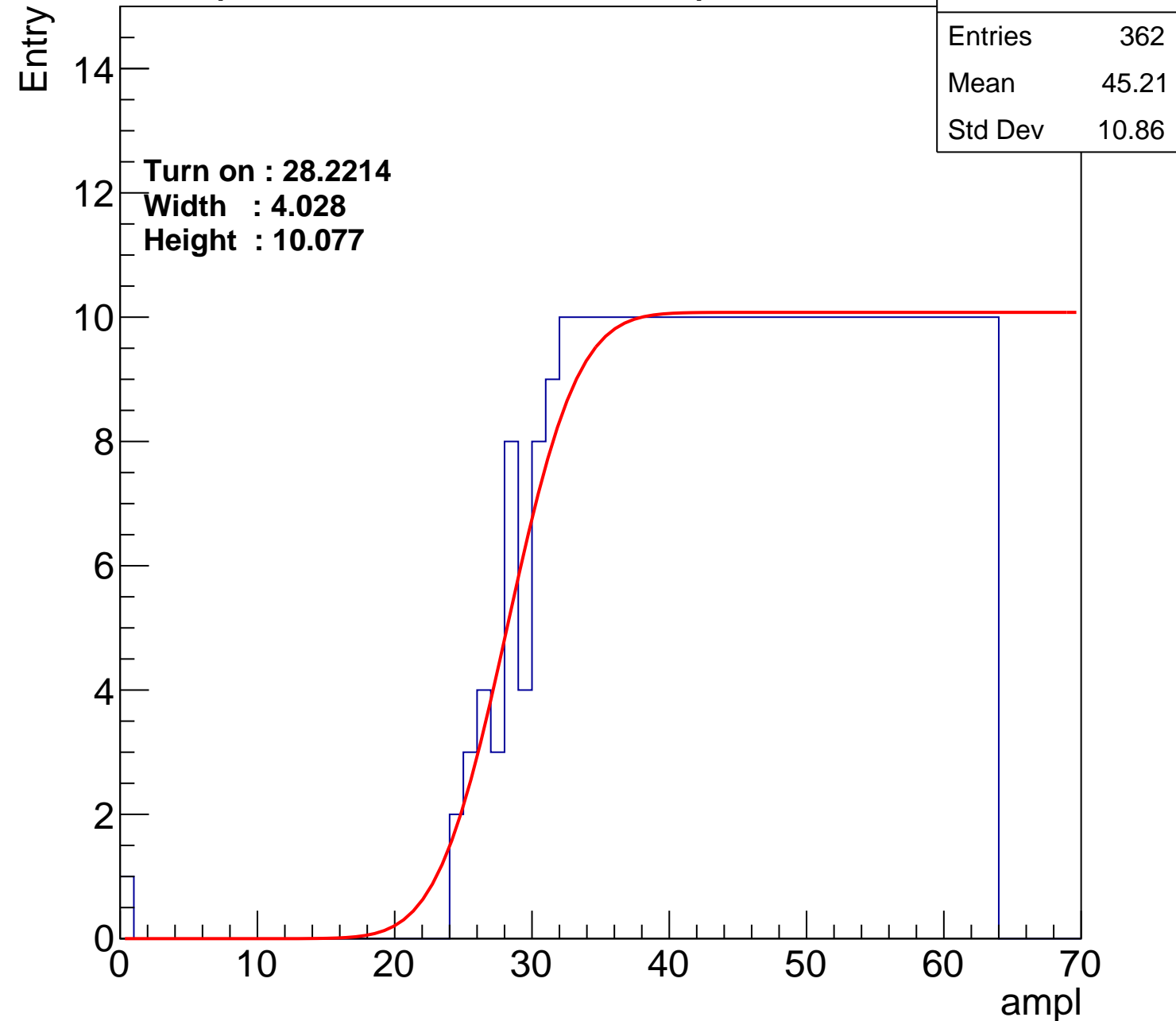
Width : 4.028

Height : 10.077

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U9-ch59

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	356
Mean	45.54
Std Dev	10.65

Turn on : 29.2022

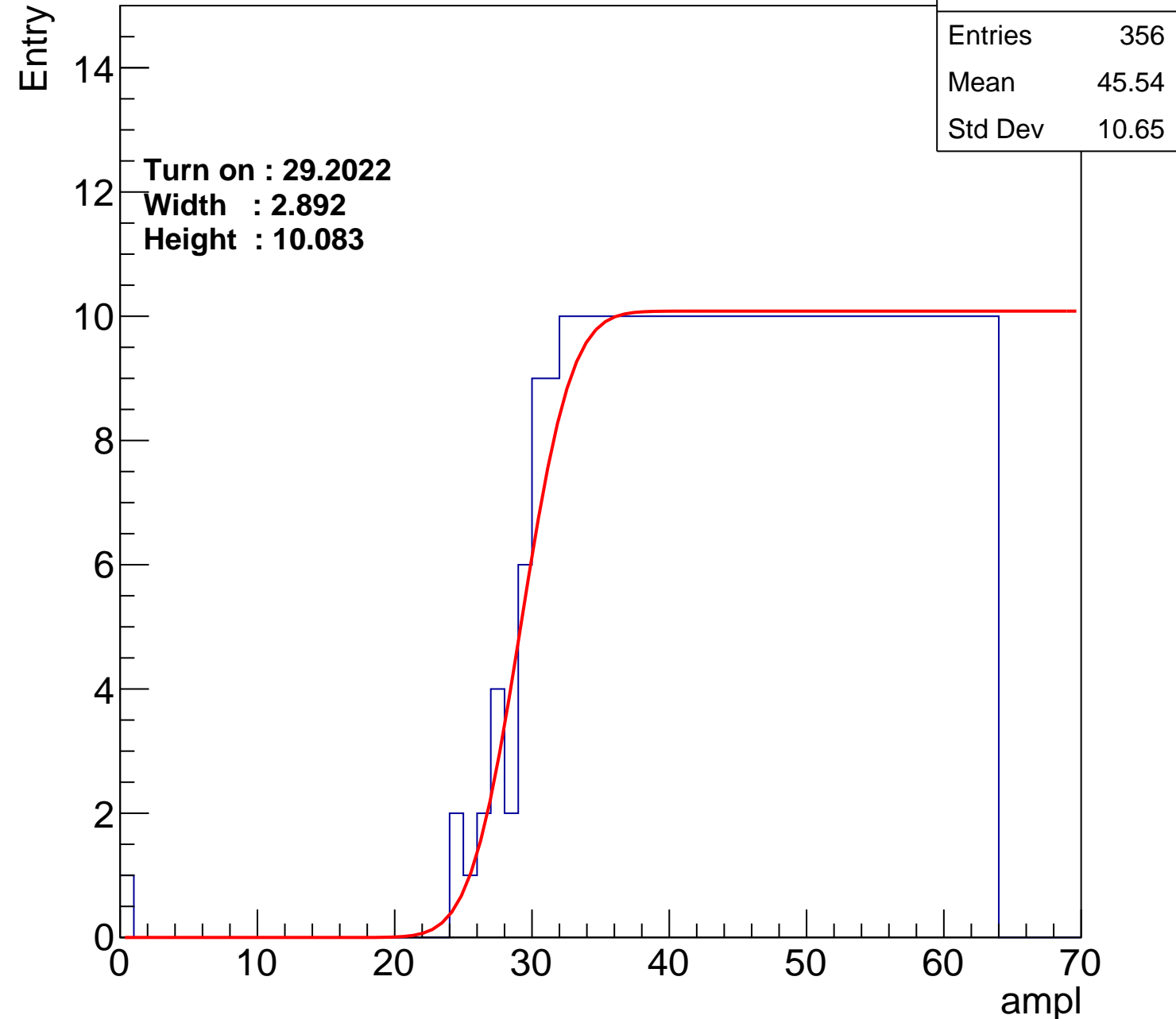
Width : 2.892

Height : 10.083

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U9-ch60

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	345
Mean	45.95
Std Dev	10.68

Turn on : 30.4335

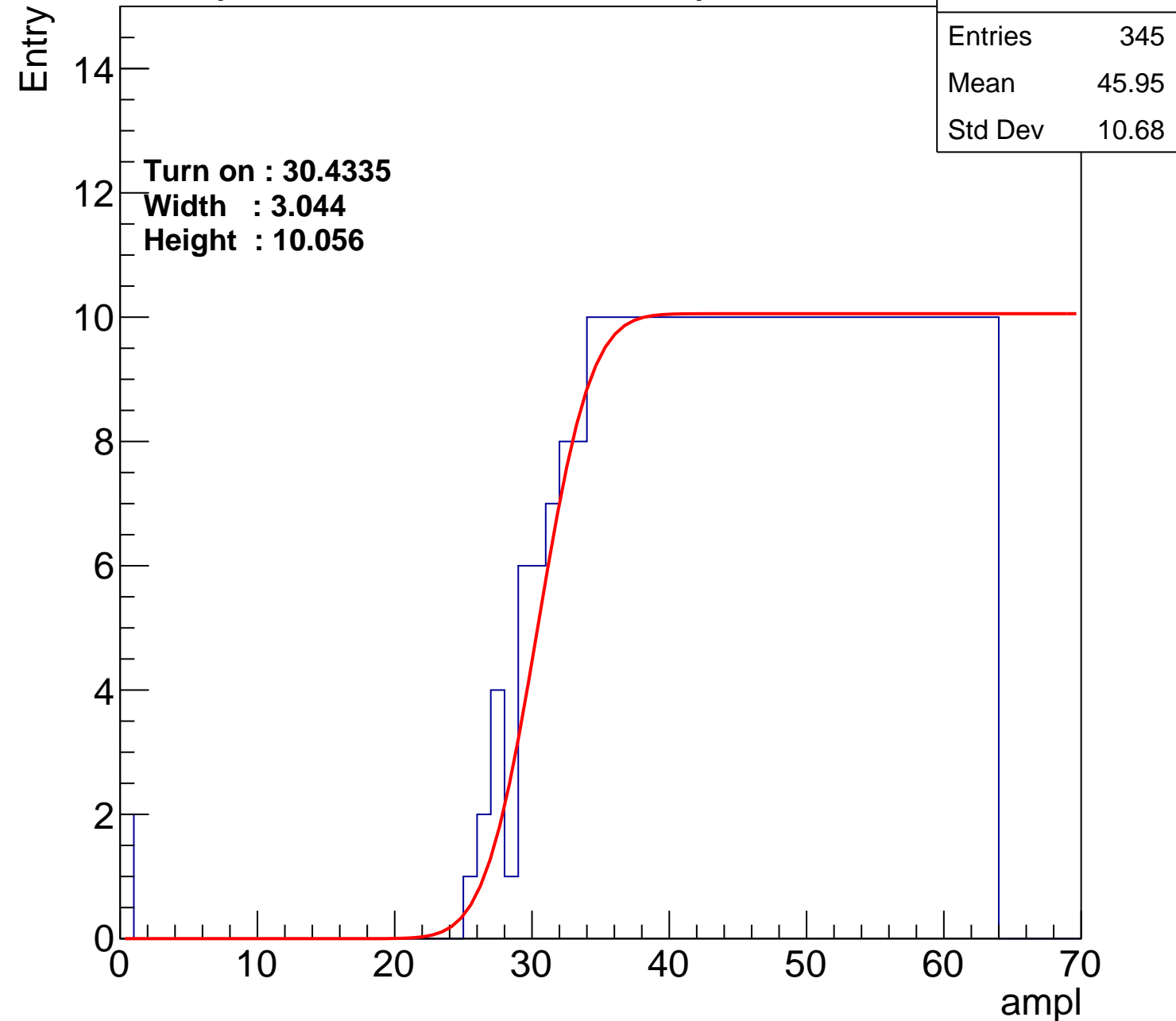
Width : 3.044

Height : 10.056

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



B0L001S, U9-ch61

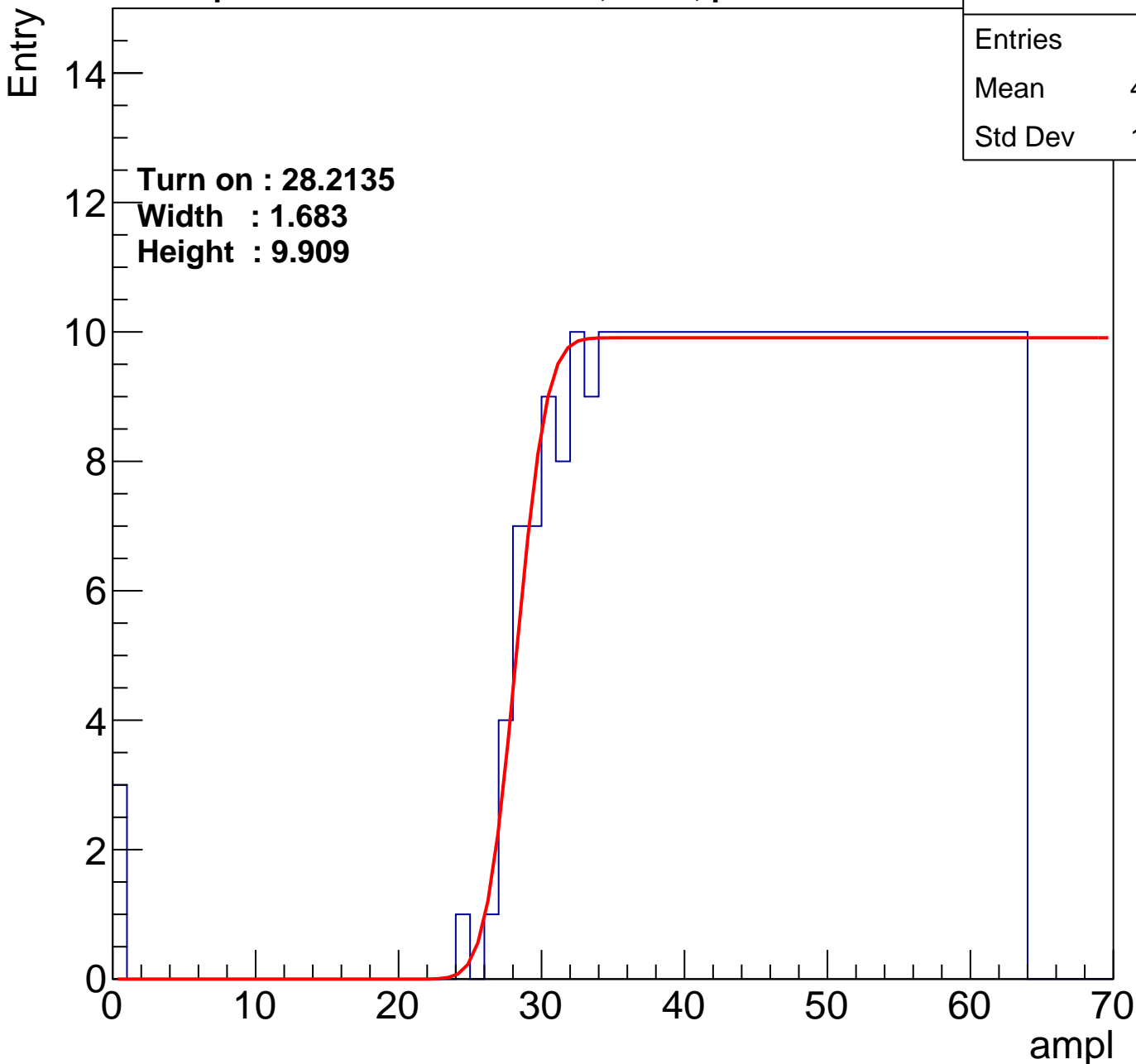
**calib\_packv5\_042523\_0143.root, FC#9, port A1**

**Turn on : 28.2135**

**Width : 1.683**

**Height : 9.909**

Entries	359
Mean	45.24
Std Dev	11.16



# B0L001S, U9-ch62

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	364
Mean	44.87
Std Dev	11.56

Turn on : 27.6348

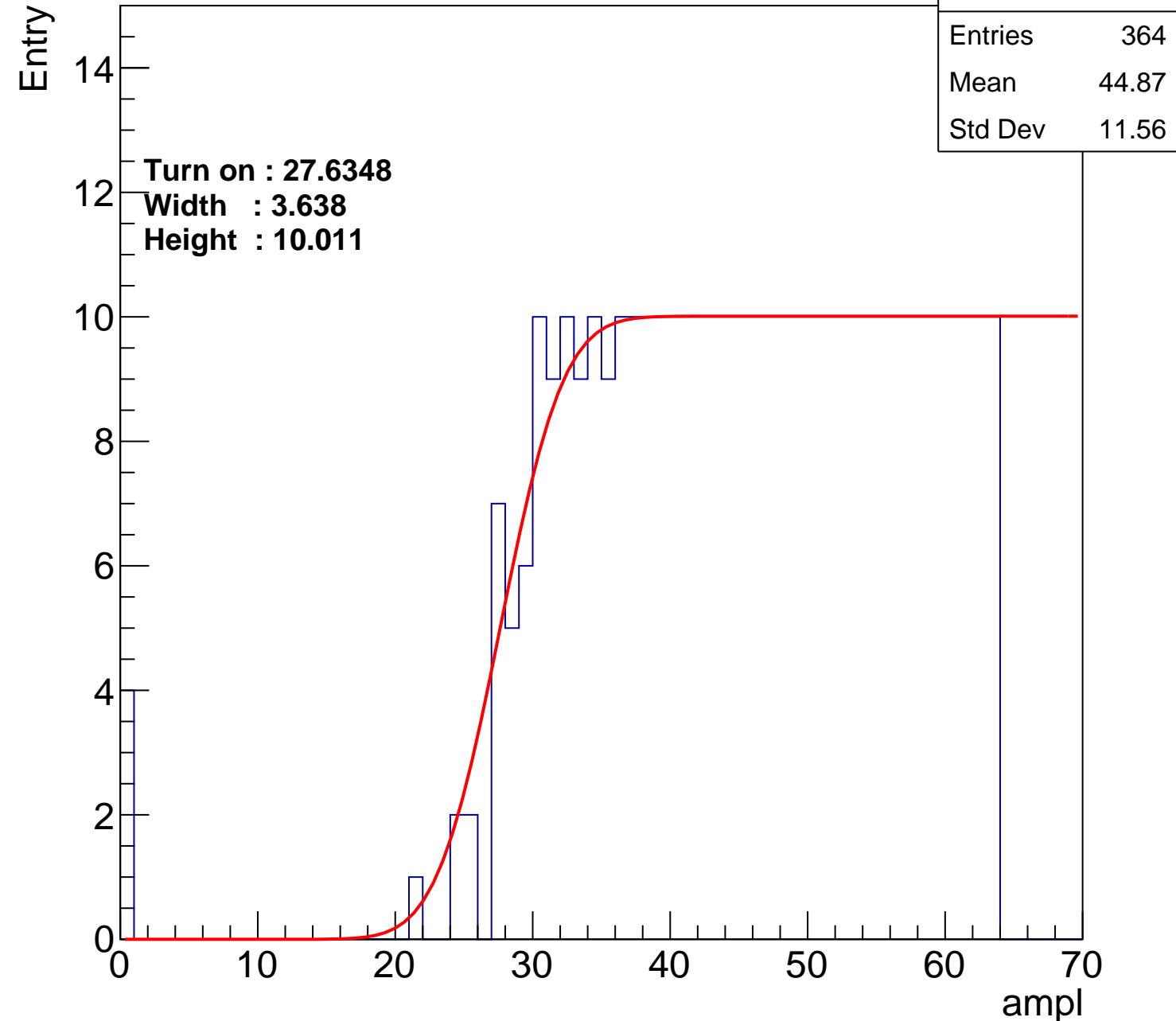
Width : 3.638

Height : 10.011

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B0L001S, U9-ch63

calib\_packv5\_042523\_0143.root, FC#9, port A1

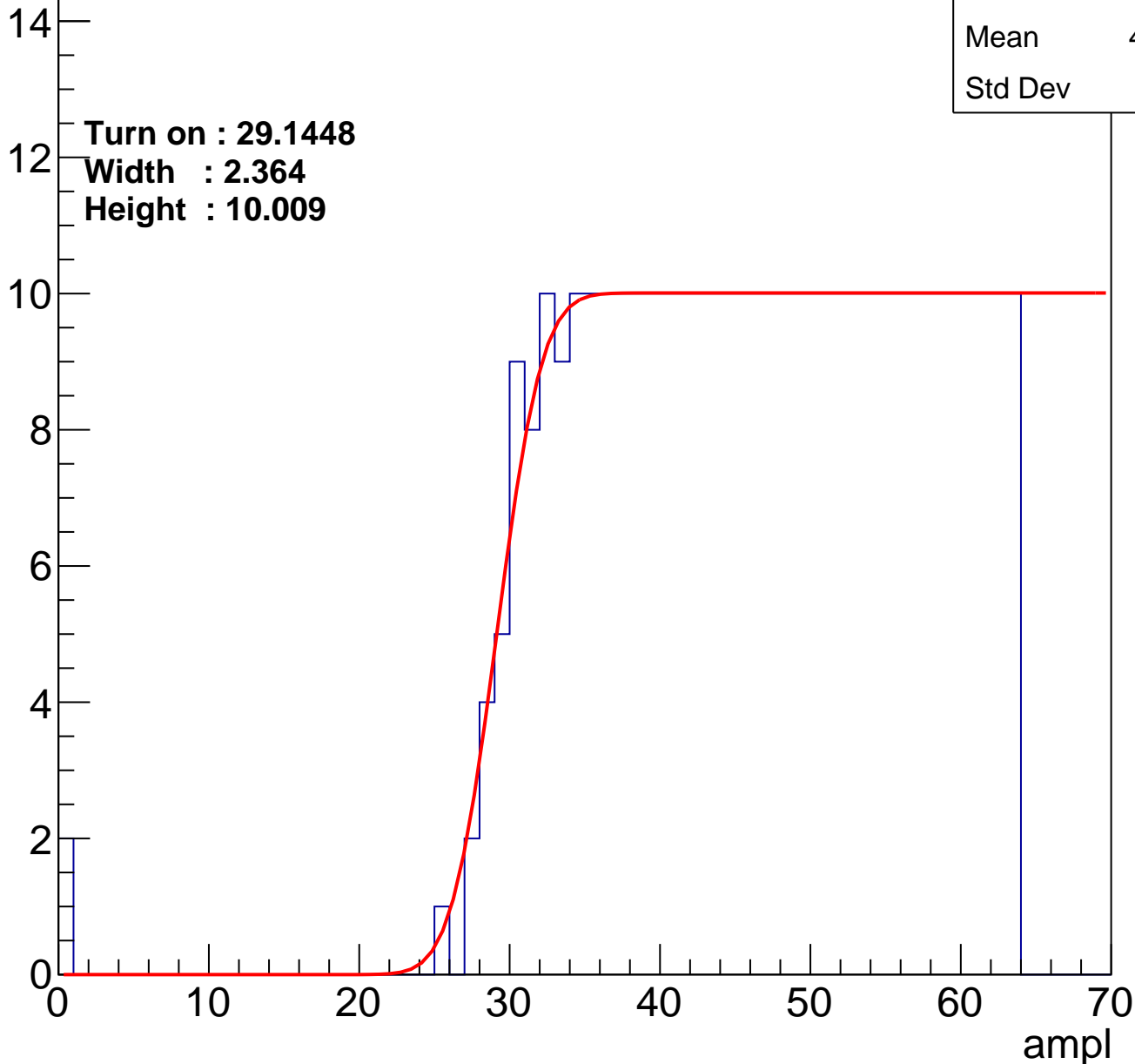
Entry

Entries	350
Mean	45.77
Std Dev	10.7

Turn on : 29.1448

Width : 2.364

Height : 10.009



# B0L001S, U9-ch64

calib\_packv5\_042523\_0143.root, FC#9, port A1

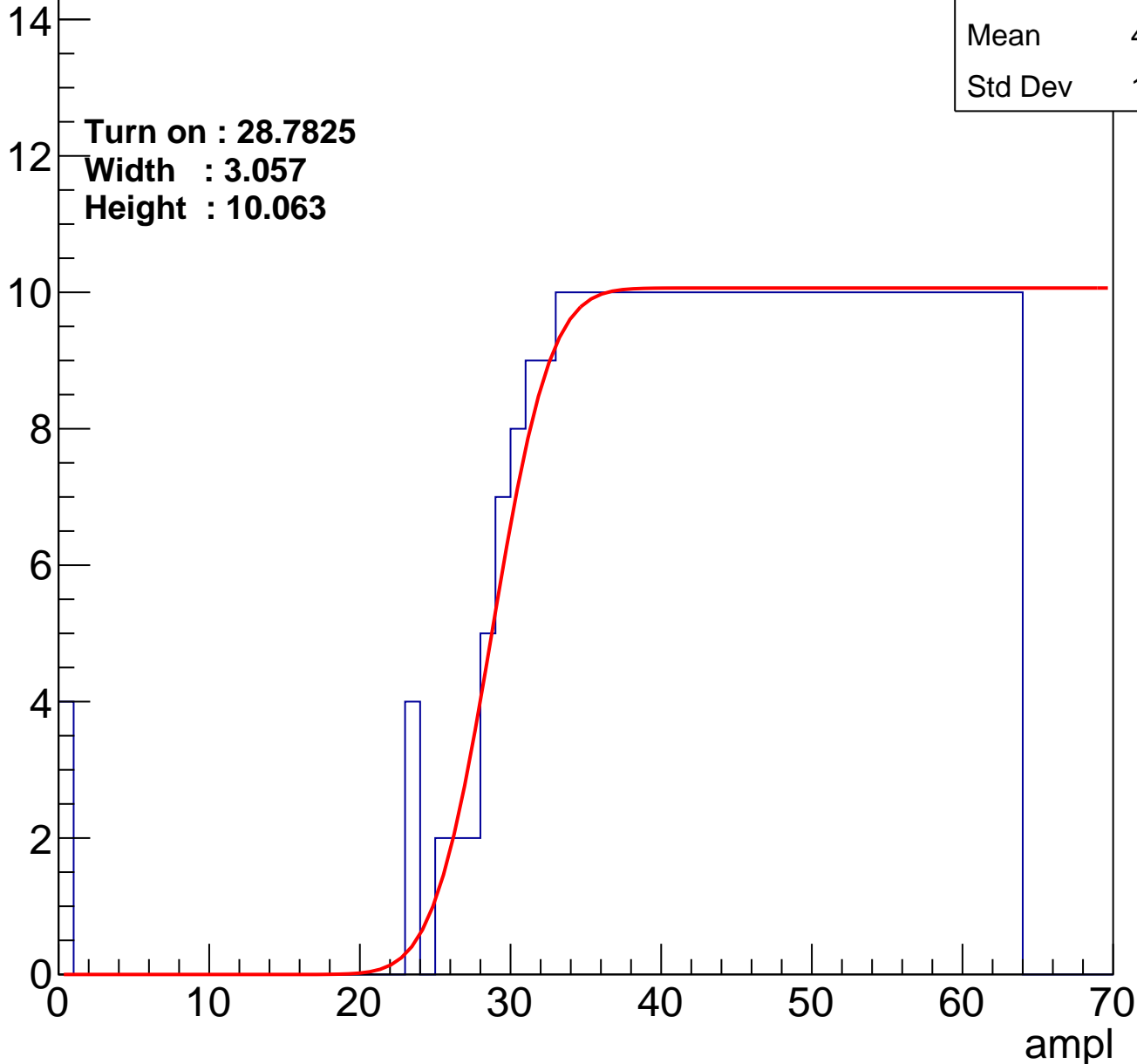
Entry

Entries	362
Mean	44.97
Std Dev	11.53

Turn on : 28.7825

Width : 3.057

Height : 10.063



# B0L001S, U9-ch65

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	353
Mean	45.47
Std Dev	11.12

**Turn on : 29.8550**

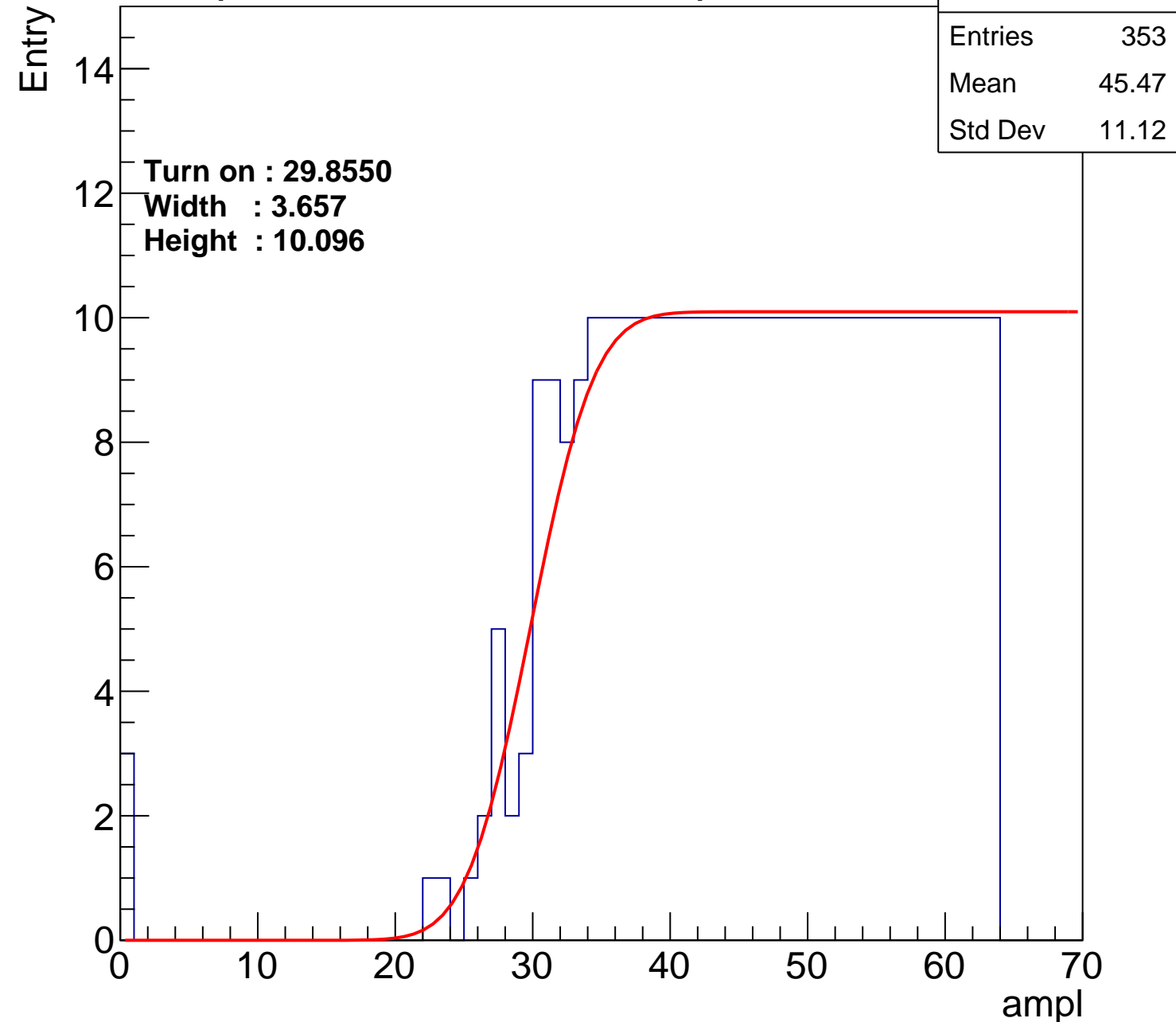
**Width : 3.657**

**Height : 10.096**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U9-ch66

calib\_packv5\_042523\_0143.root, FC#9, port A1

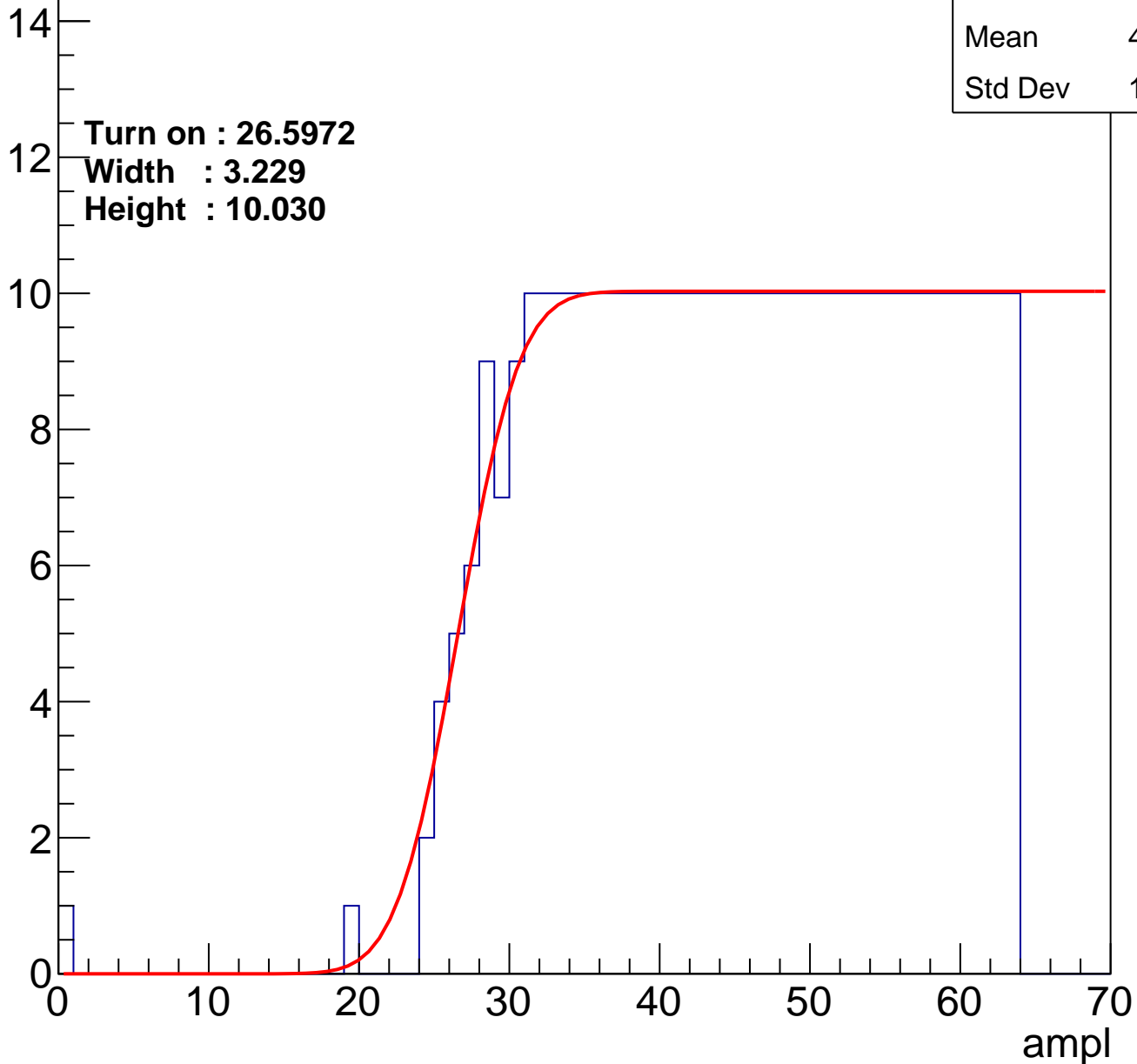
Entries	374
Mean	44.64
Std Dev	11.16

Turn on : 26.5972

Width : 3.229

Height : 10.030

Entry



# B0L001S, U9-ch67

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	357
Mean	45.3
Std Dev	11.18

Turn on : 29.0542

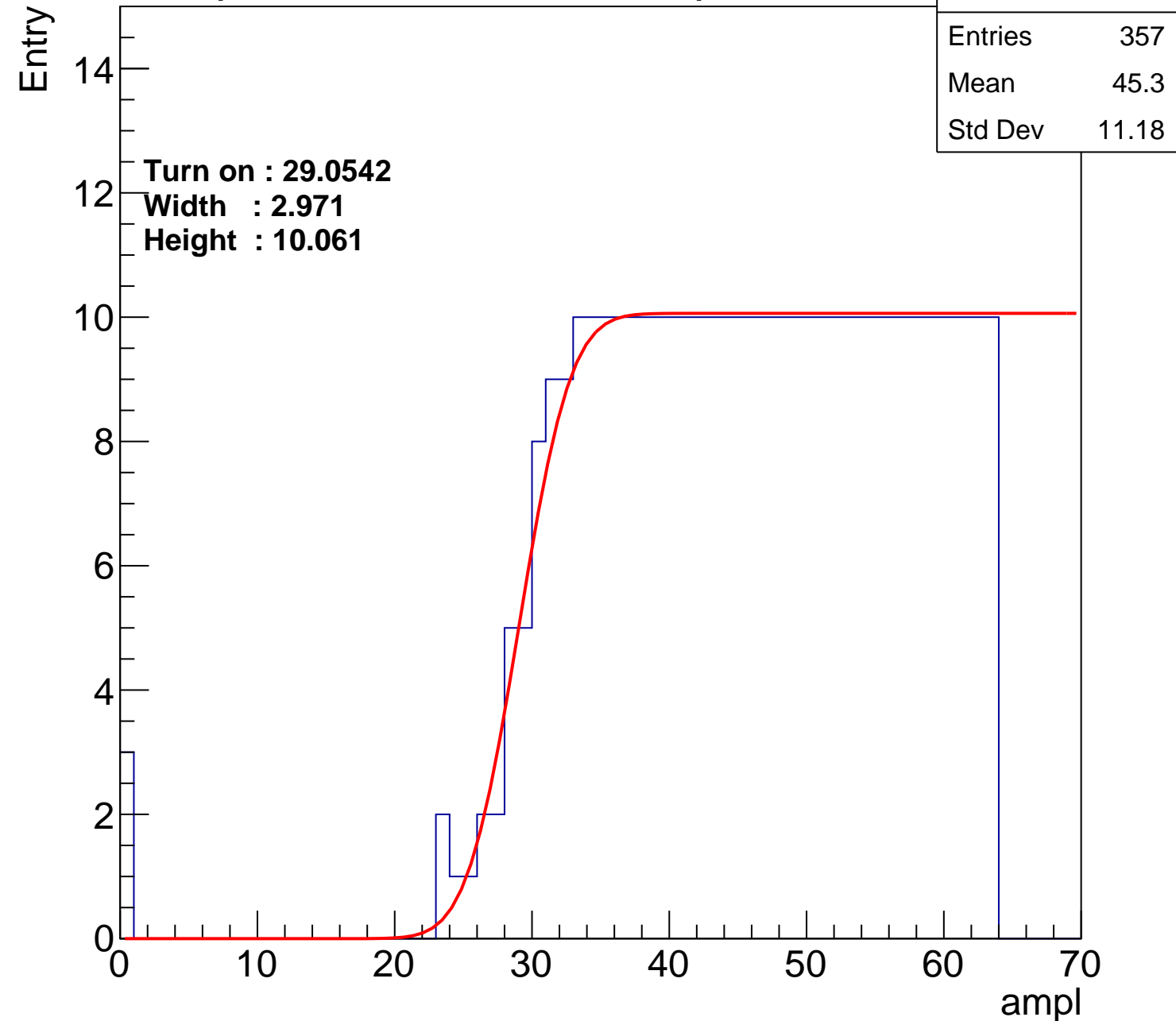
Width : 2.971

Height : 10.061

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U9-ch68

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	368
Mean	44.68
Std Dev	11.65

Turn on : 28.2873

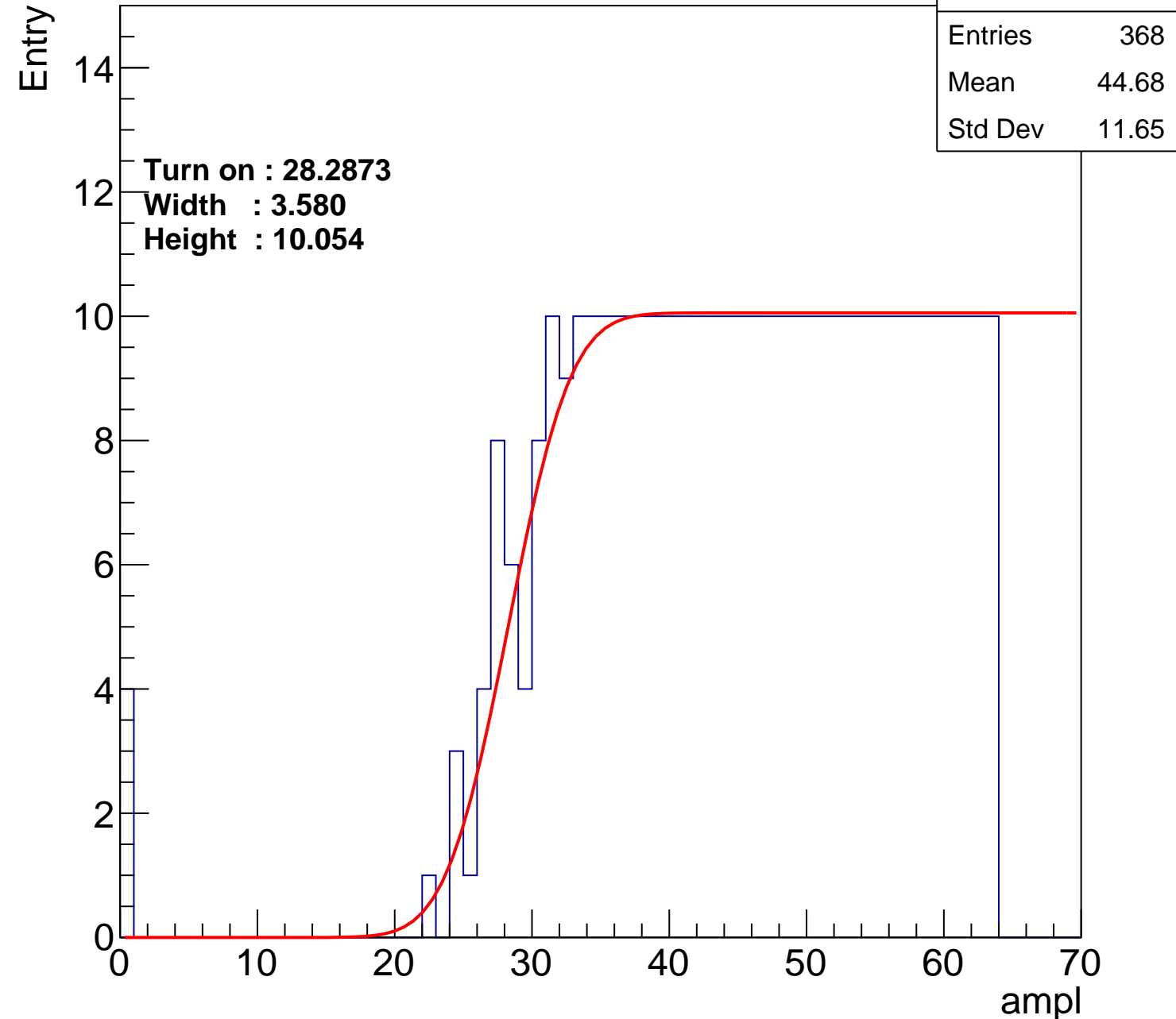
Width : 3.580

Height : 10.054

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U9-ch69

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	359
Mean	45.18
Std Dev	11.25

Turn on : 28.7475

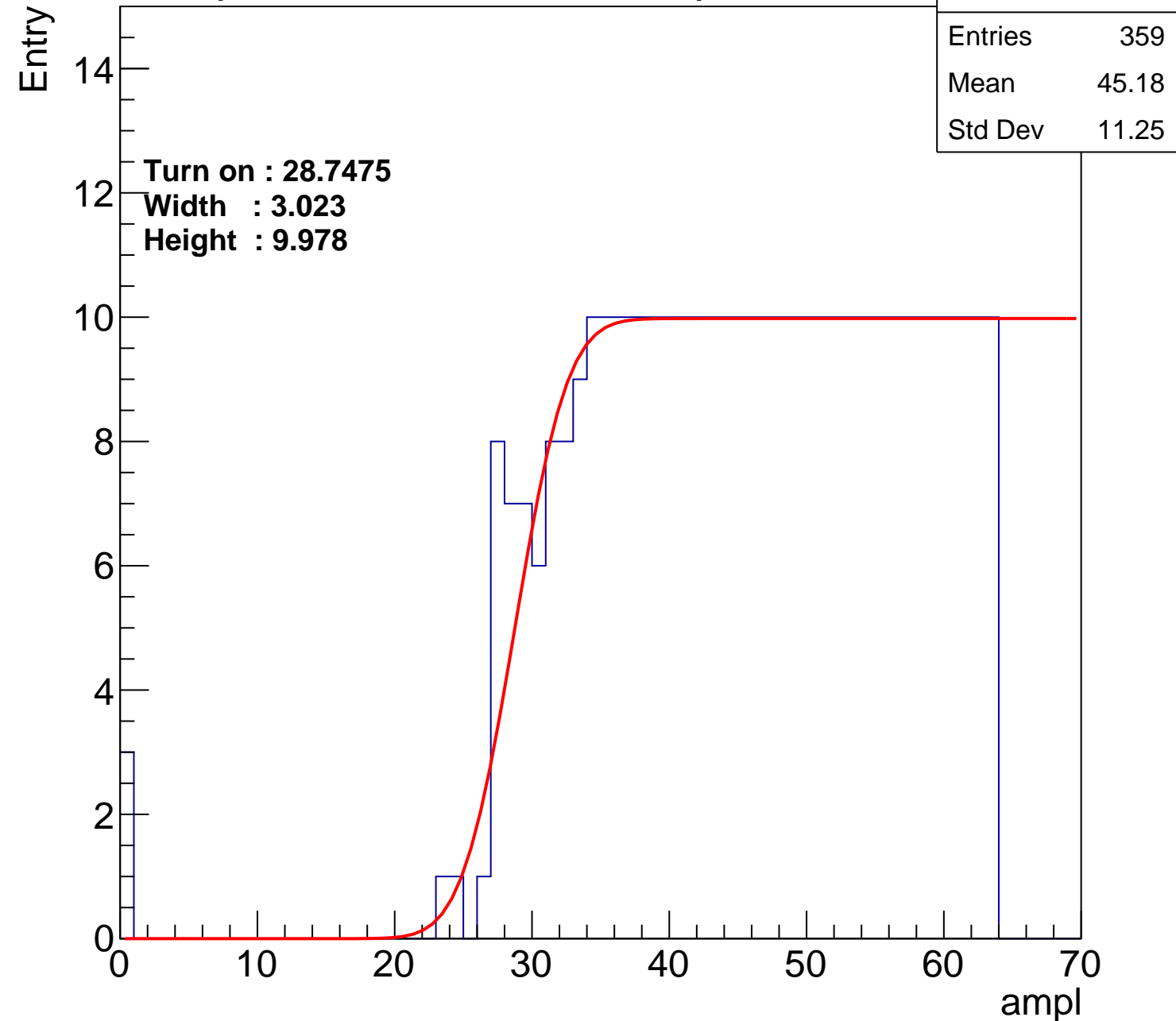
Width : 3.023

Height : 9.978

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U9-ch70

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	342
Mean	46.01
Std Dev	10.88

**Turn on : 30.6850**

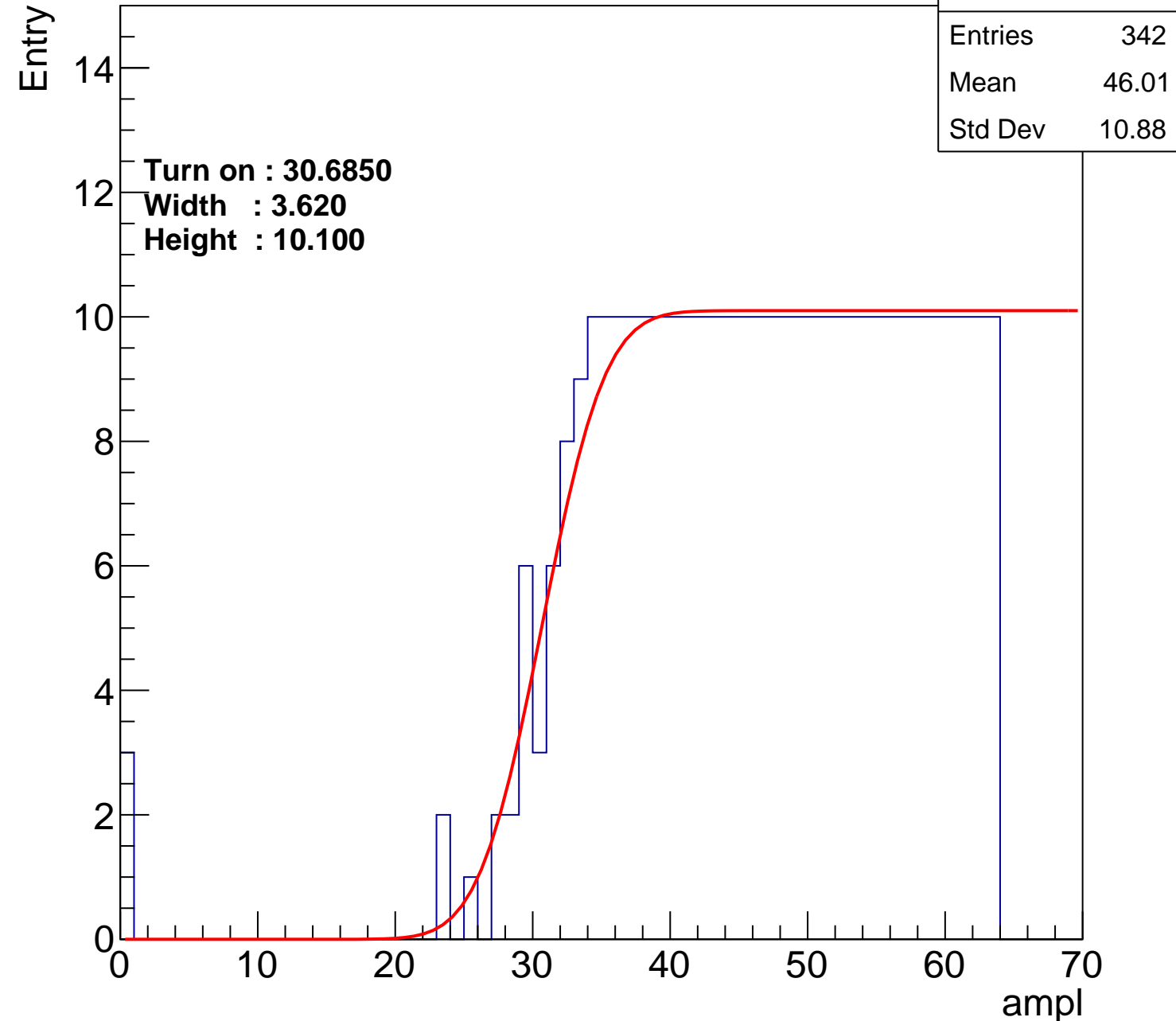
**Width : 3.620**

**Height : 10.100**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B0L001S, U9-ch71

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	375
Mean	44.34
Std Dev	11.82

**Turn on : 27.2047**

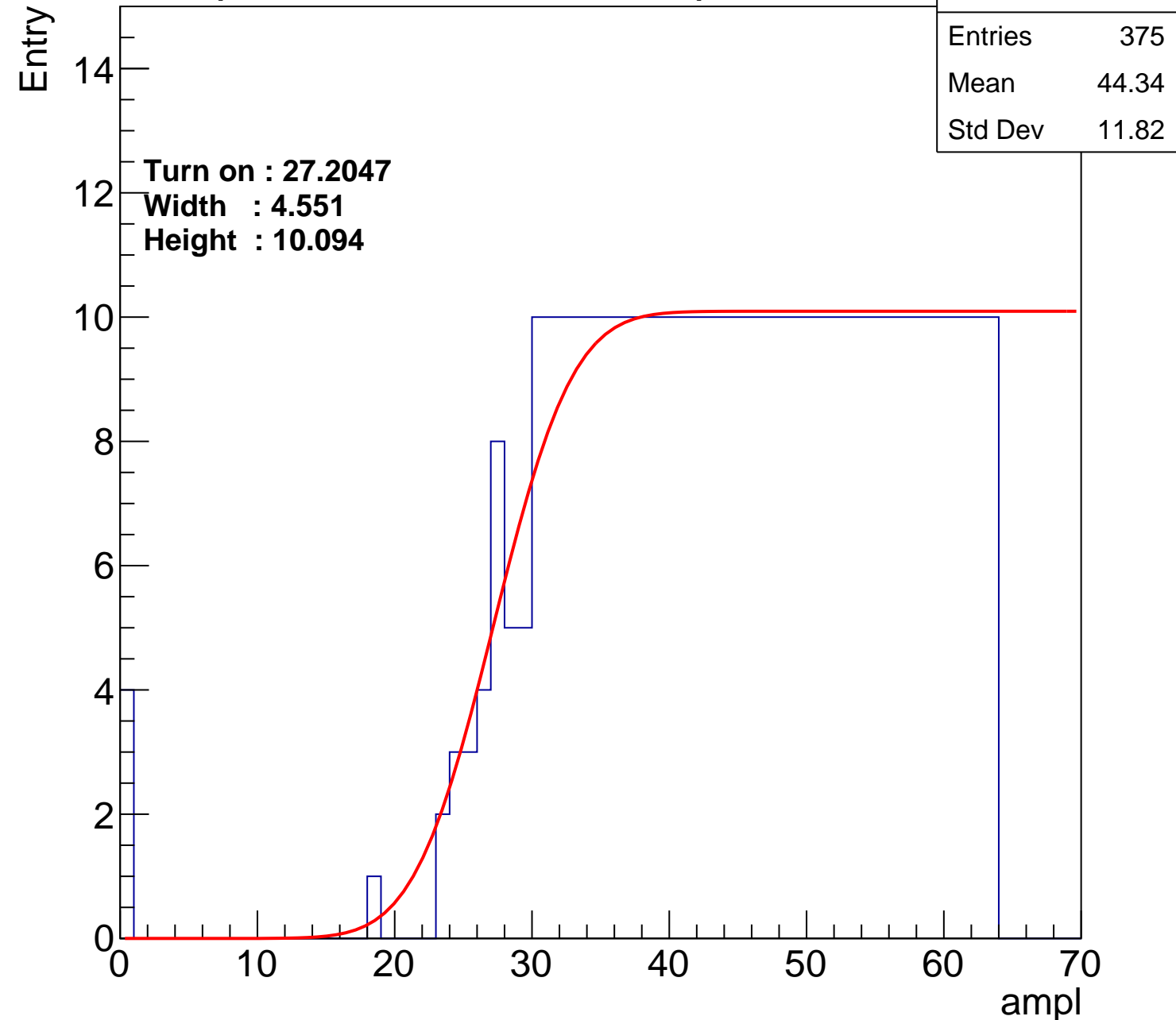
**Width : 4.551**

**Height : 10.094**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U9-ch72

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	356
Mean	45.44
Std Dev	10.91

**Turn on : 28.9287**

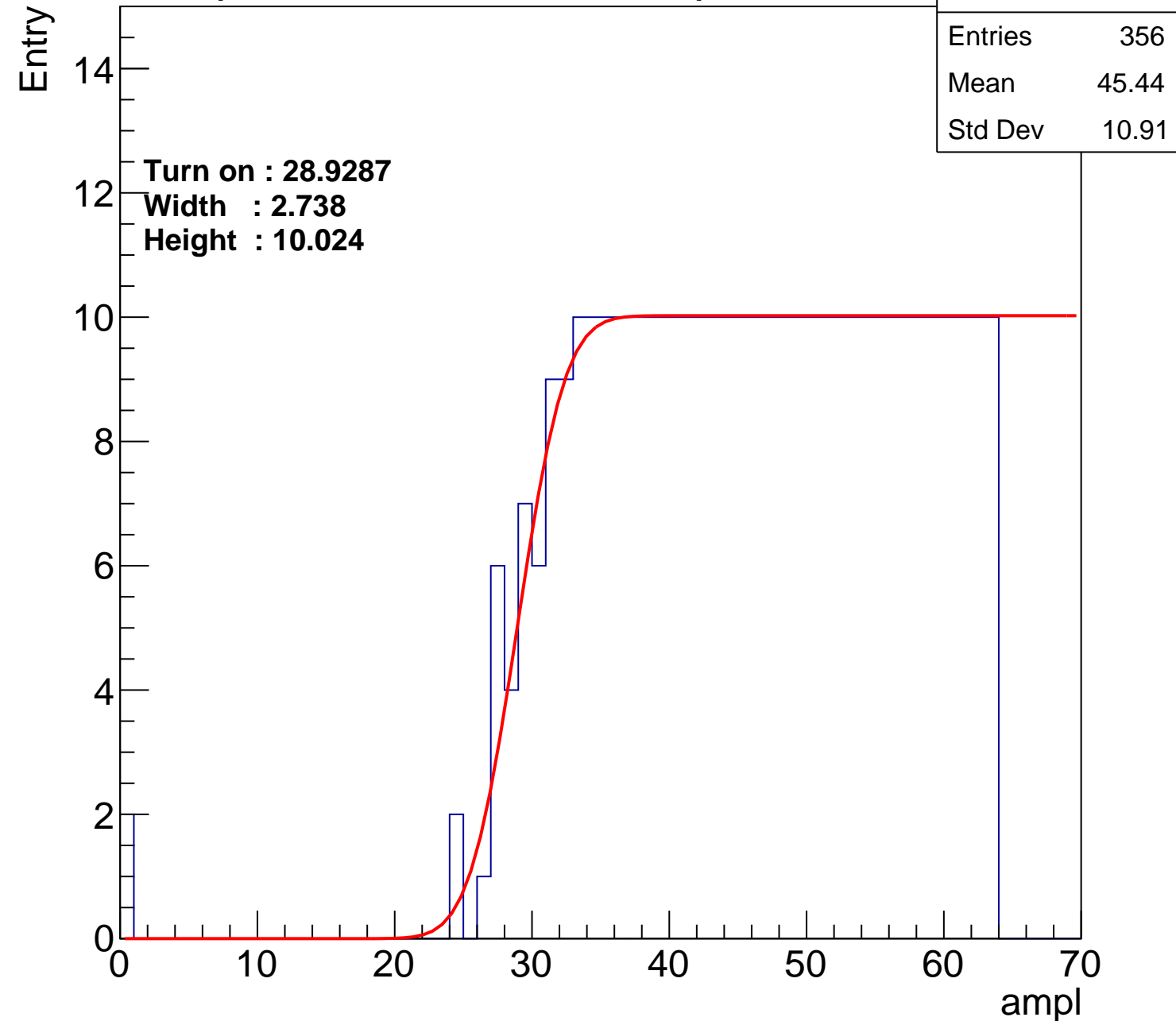
**Width : 2.738**

**Height : 10.024**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U9-ch73

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	364
Mean	45.04
Std Dev	11.13

Turn on : 28.0255

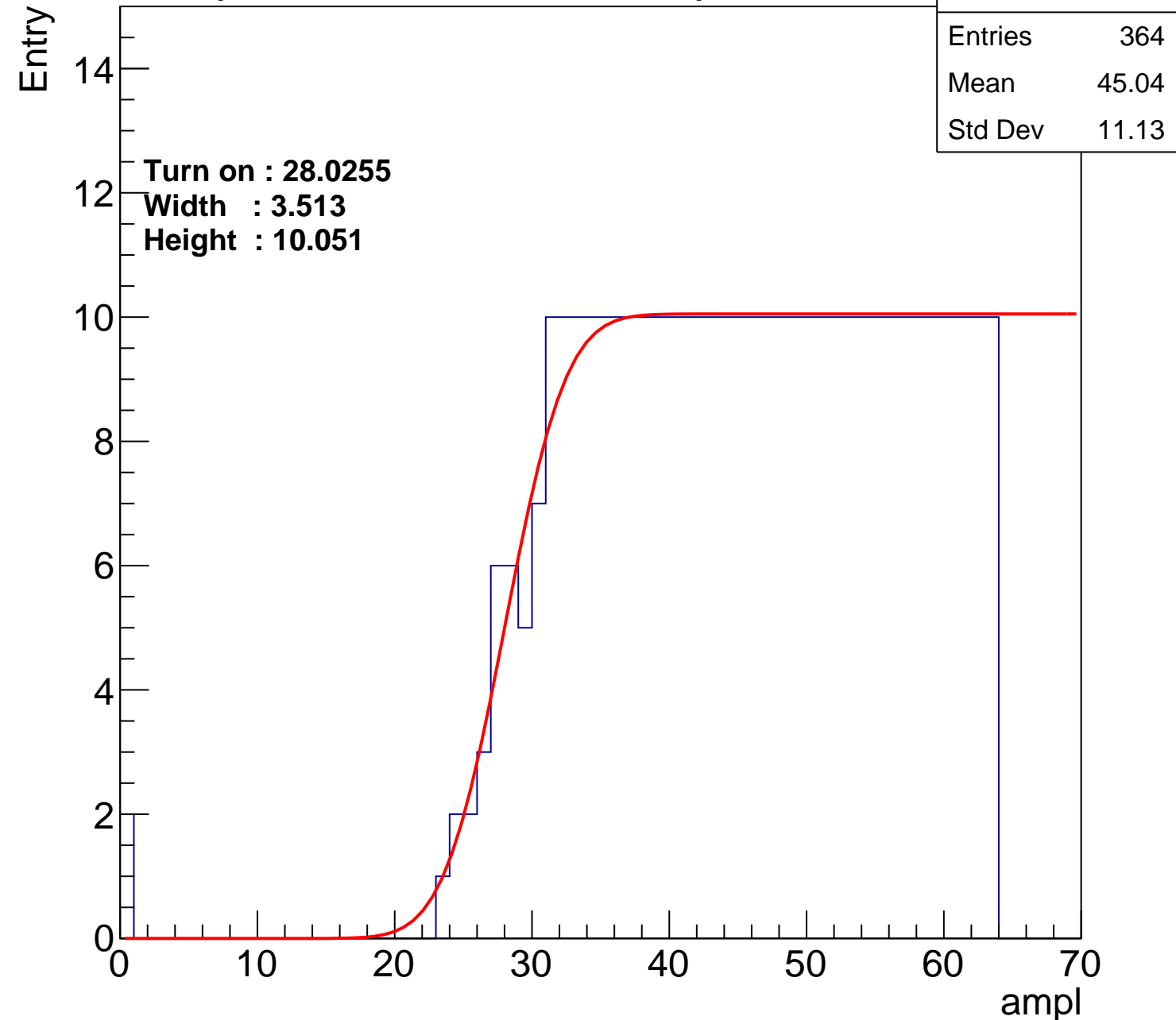
Width : 3.513

Height : 10.051

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



**B0L001S, U9-ch74**

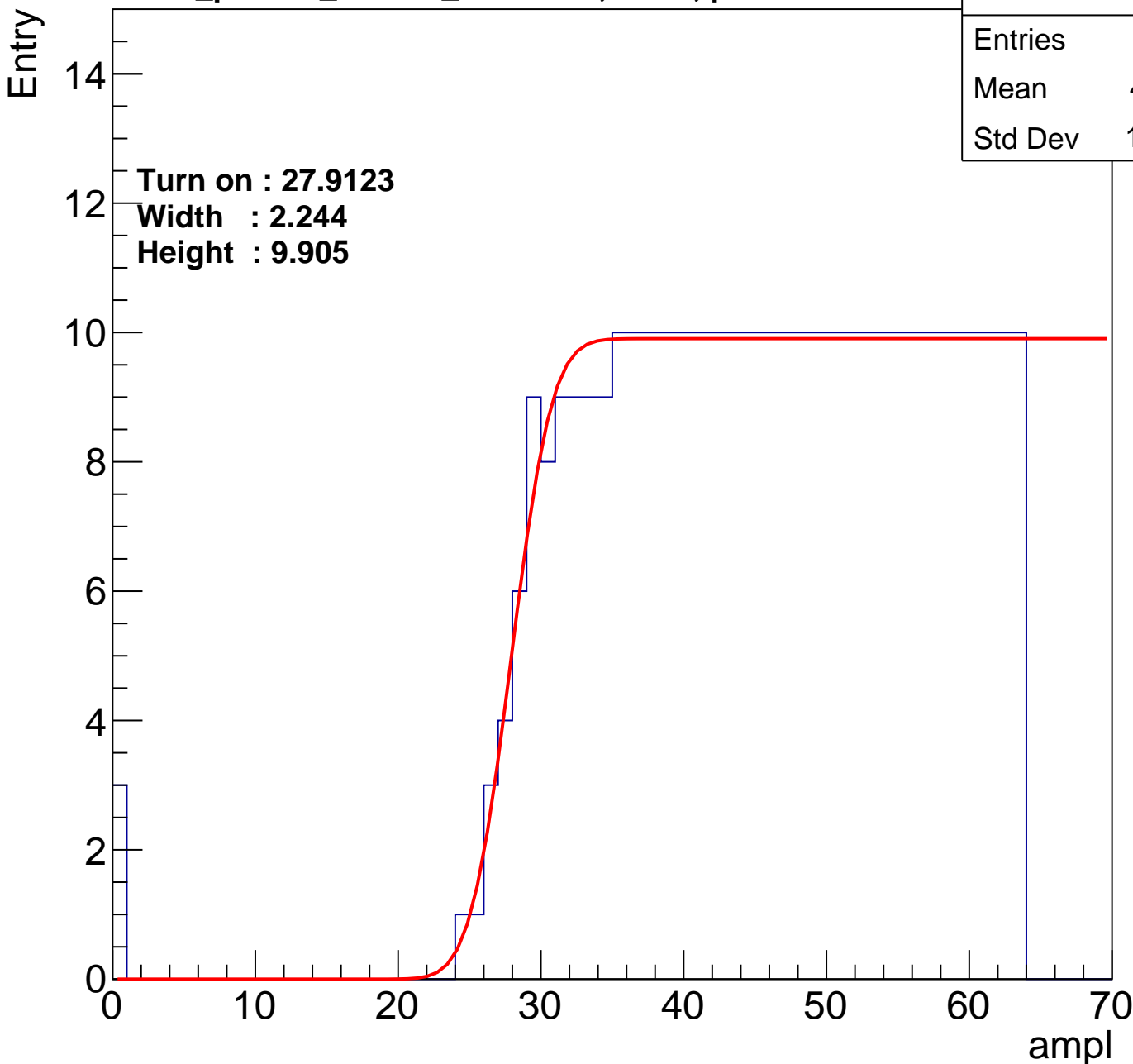
**calib\_packv5\_042523\_0143.root, FC#9, port A1**

Entries	361
Mean	45.11
Std Dev	11.26

**Turn on : 27.9123**

**Width : 2.244**

**Height : 9.905**



# B0L001S, U9-ch75

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	362
Mean	44.92
Std Dev	11.68

**Turn on : 28.6109**

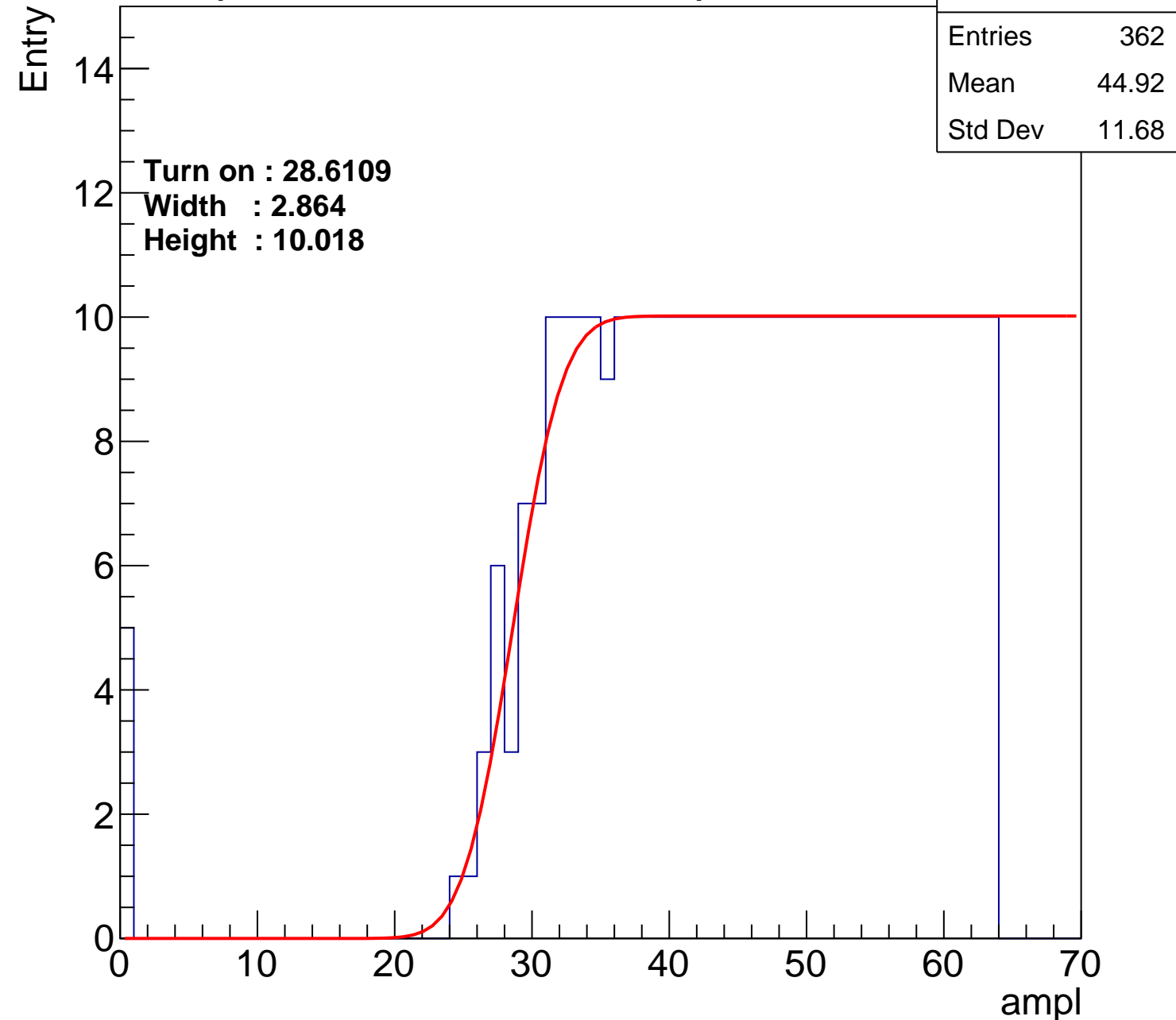
**Width : 2.864**

**Height : 10.018**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U9-ch76

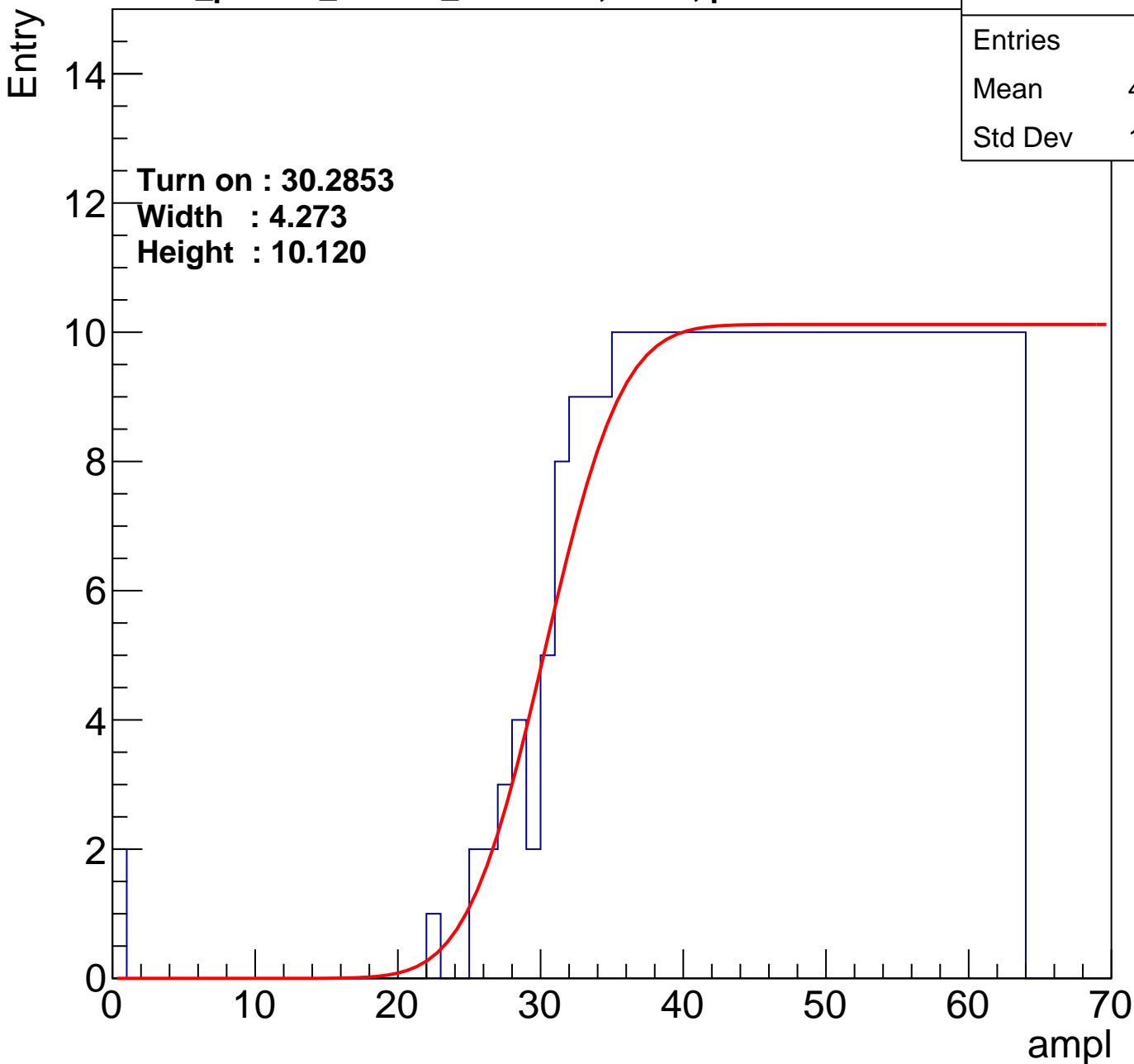
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	346
Mean	45.88
Std Dev	10.75

Turn on : 30.2853

Width : 4.273

Height : 10.120



# B0L001S, U9-ch77

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	355
Mean	45.23
Std Dev	11.58

Turn on : 29.3134

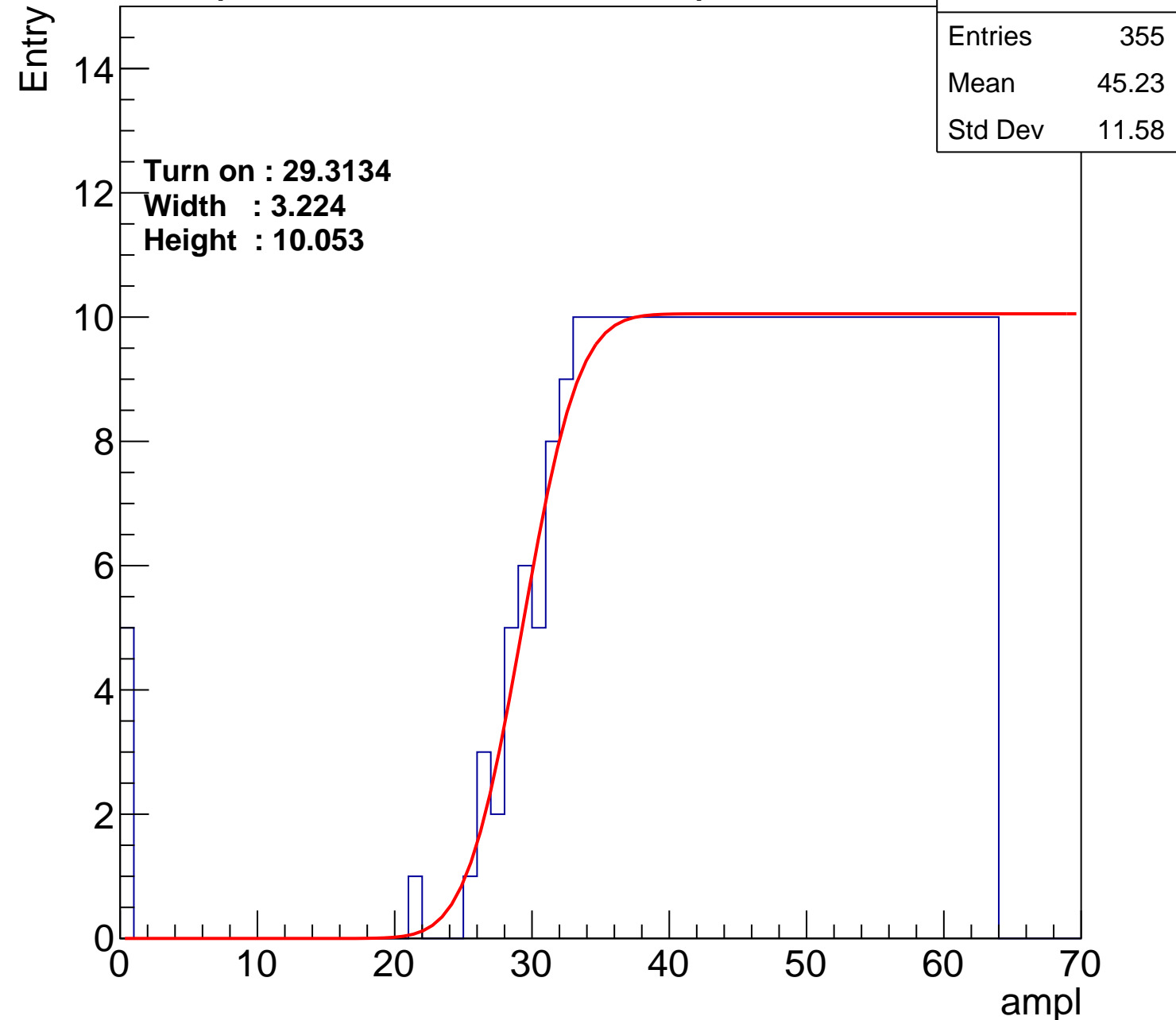
Width : 3.224

Height : 10.053

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U9-ch78

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	355
Mean	45.4
Std Dev	11.13

Turn on : 29.2074

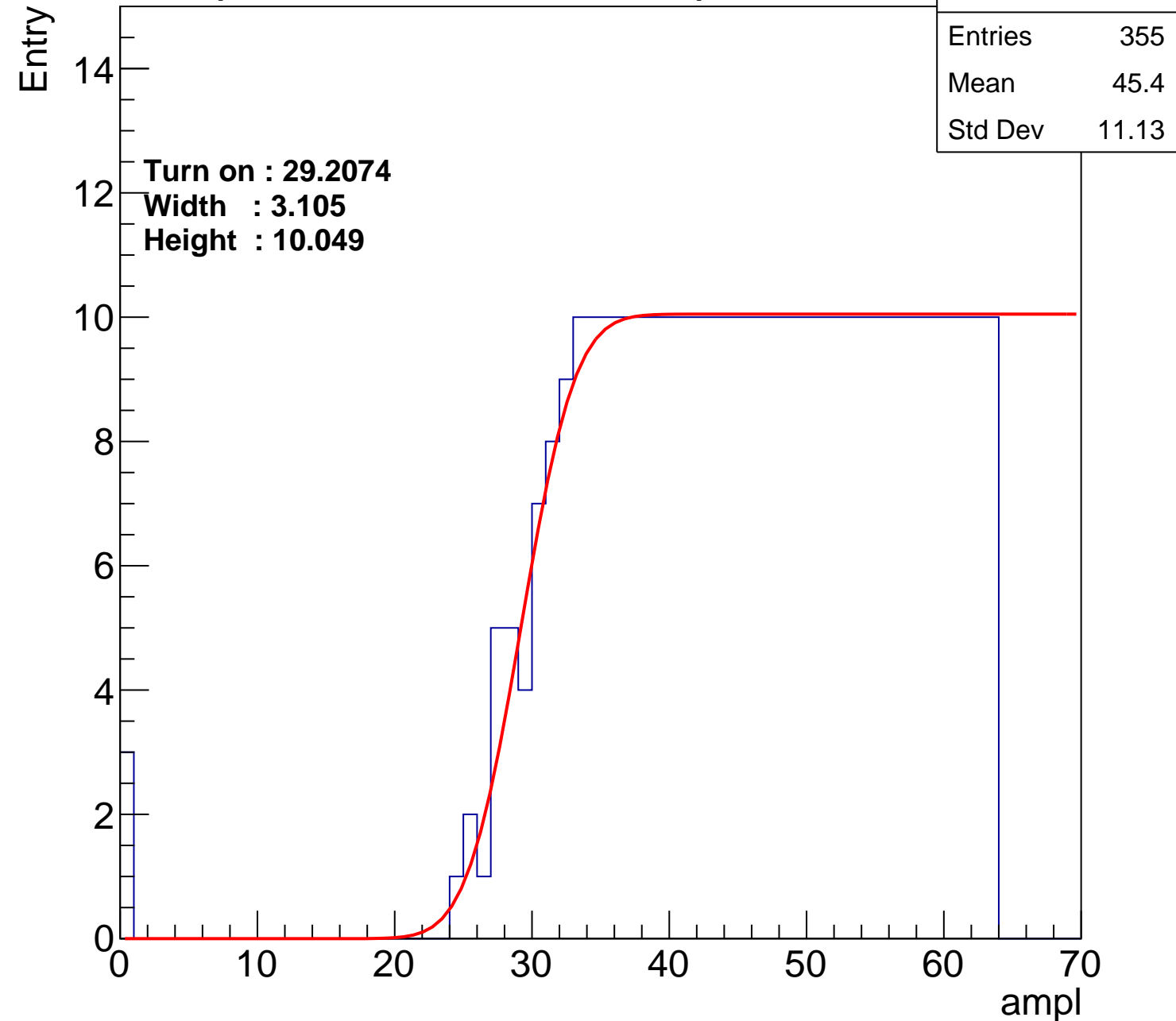
Width : 3.105

Height : 10.049

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B0L001S, U9-ch79

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	360
Mean	45.35
Std Dev	10.74

Turn on : 28.3246

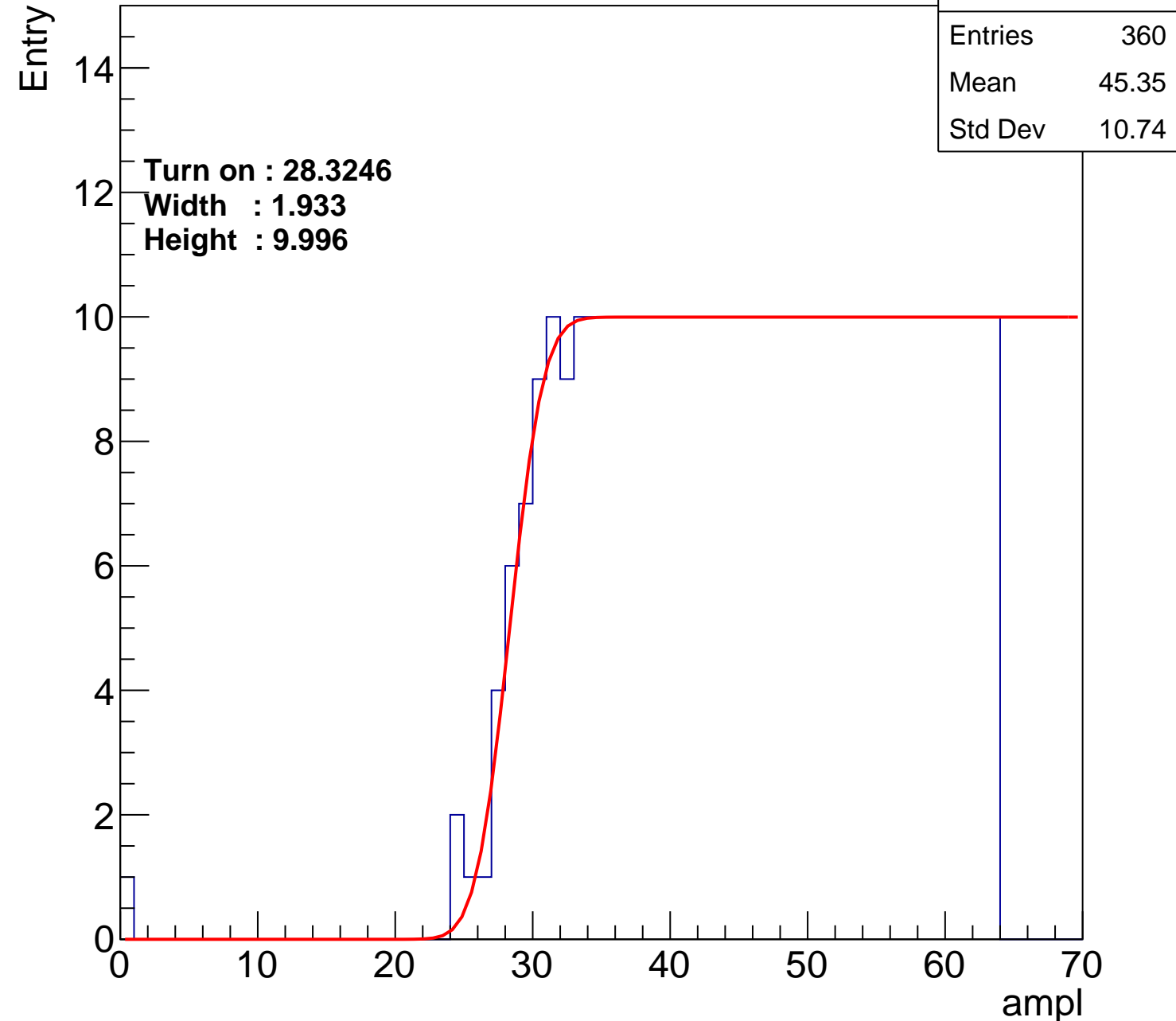
Width : 1.933

Height : 9.996

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U9-ch80

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	384
Mean	43.96
Std Dev	11.92

Turn on : 26.1742

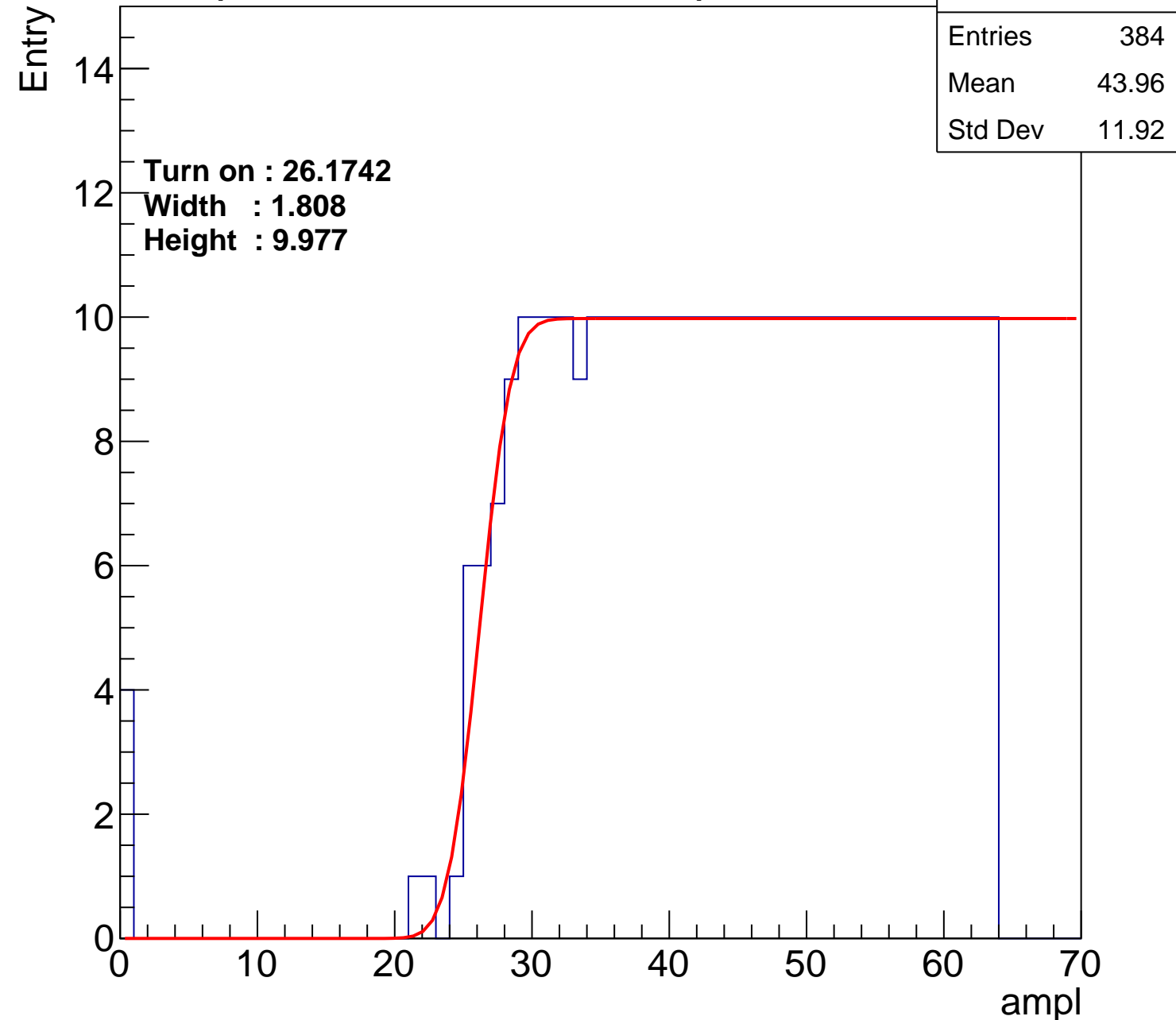
Width : 1.808

Height : 9.977

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U9-ch81

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	360
Mean	45.37
Std Dev	10.71

**Turn on : 28.1505**

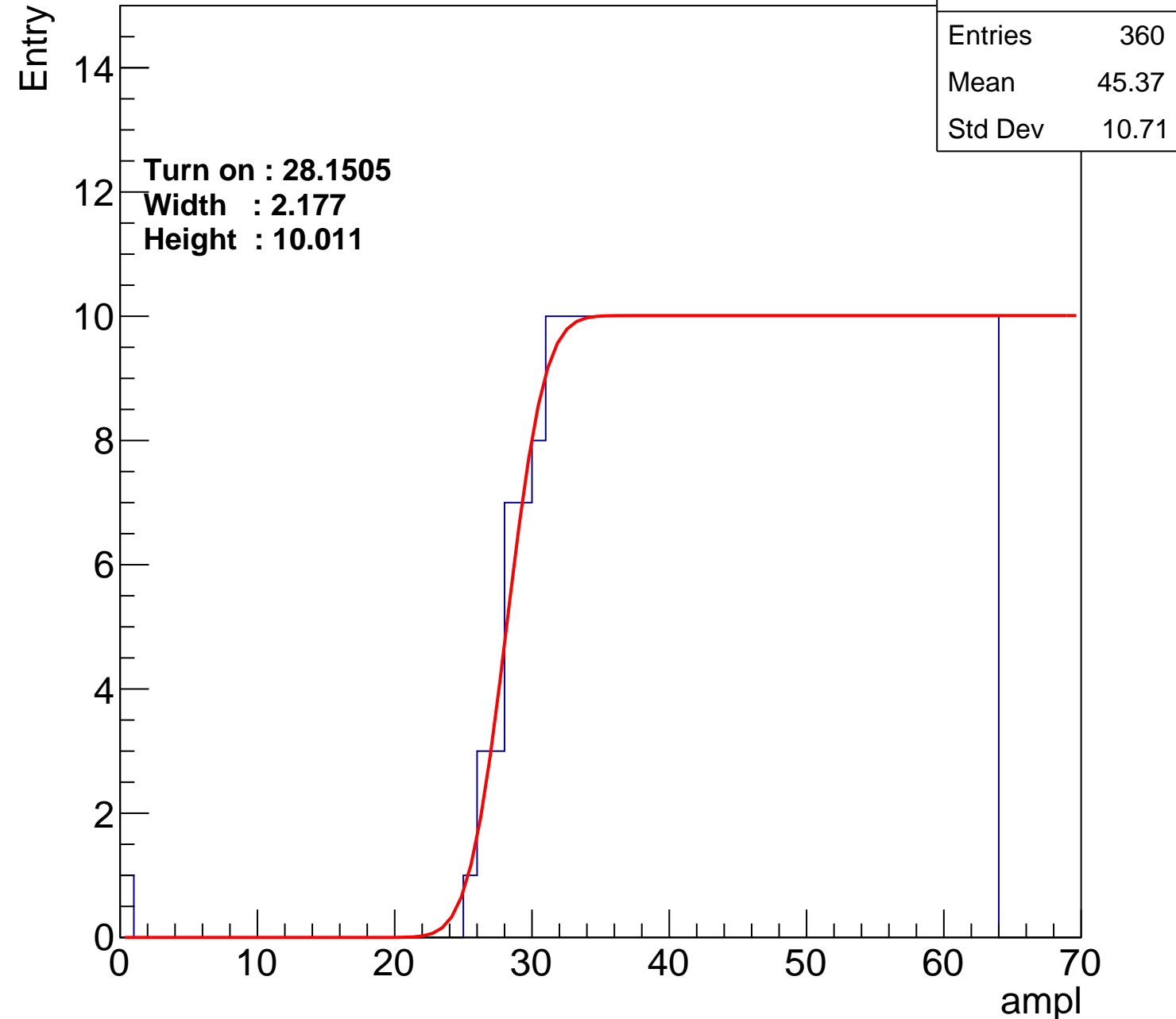
**Width : 2.177**

**Height : 10.011**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U9-ch82

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	353
Mean	45.61
Std Dev	10.69

Turn on : 29.2715

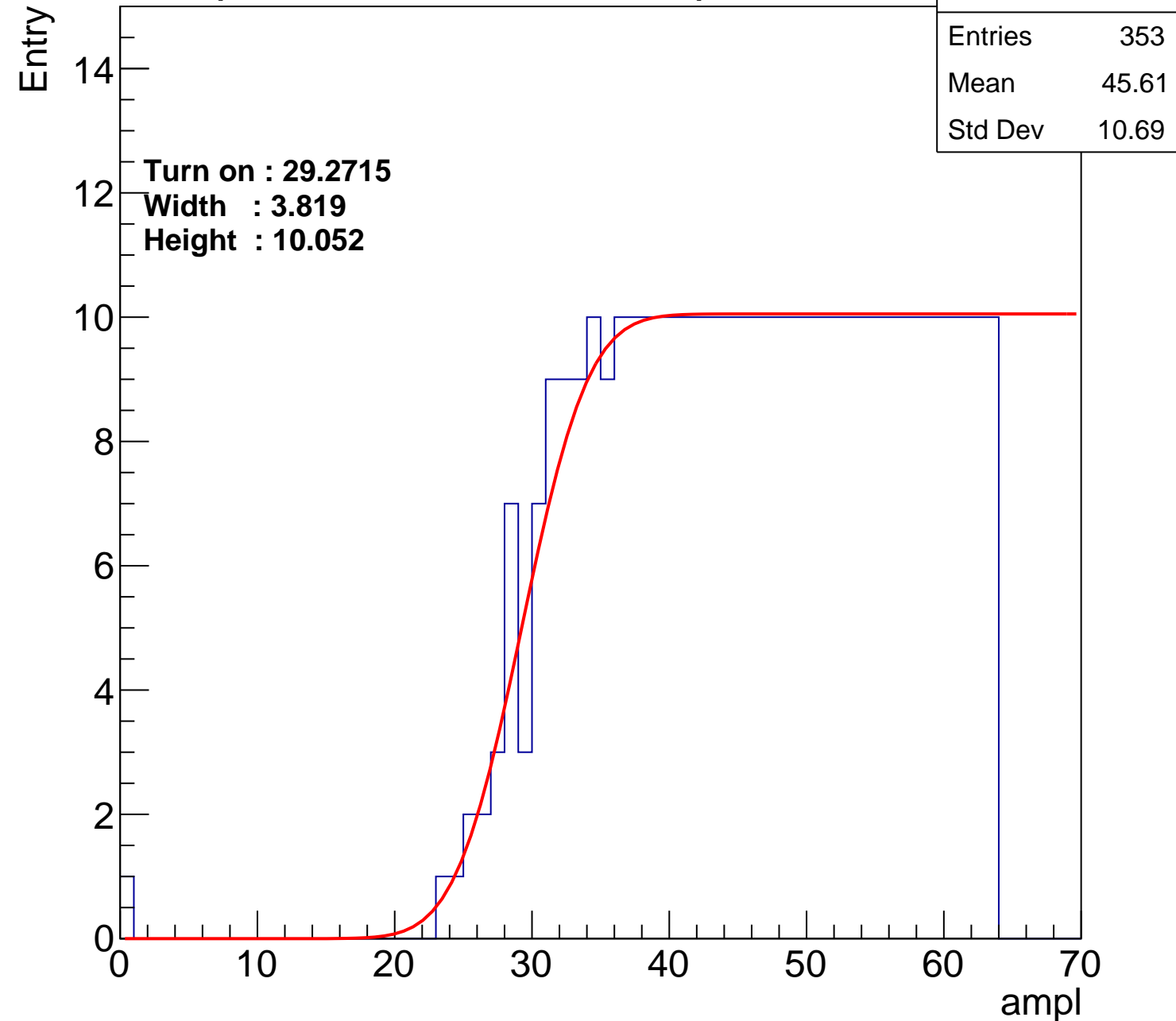
Width : 3.819

Height : 10.052

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U9-ch83

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	380
Mean	44.11
Std Dev	11.9

Turn on : 26.5011

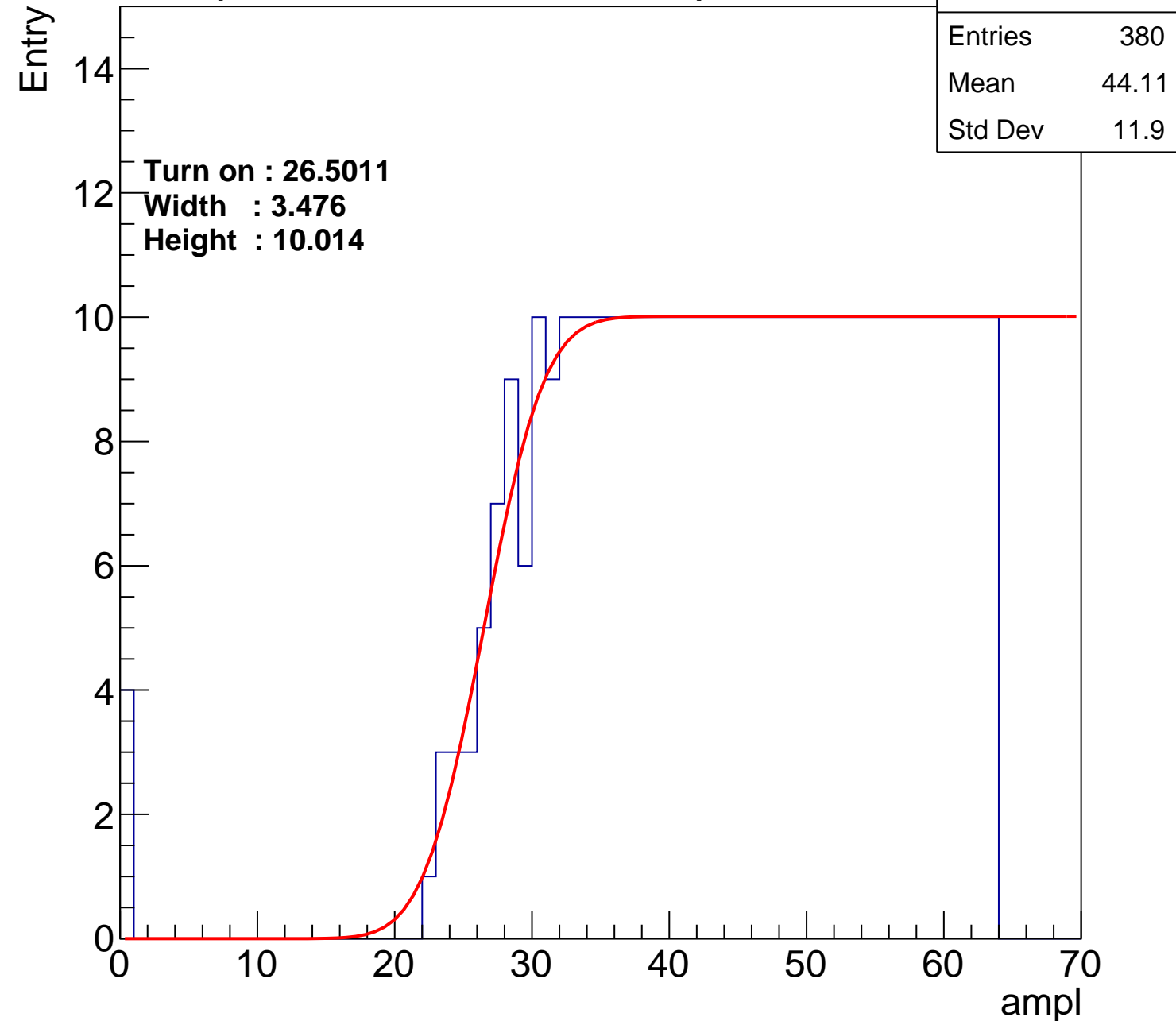
Width : 3.476

Height : 10.014

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U9-ch84

calib\_packv5\_042523\_0143.root, FC#9, port A1

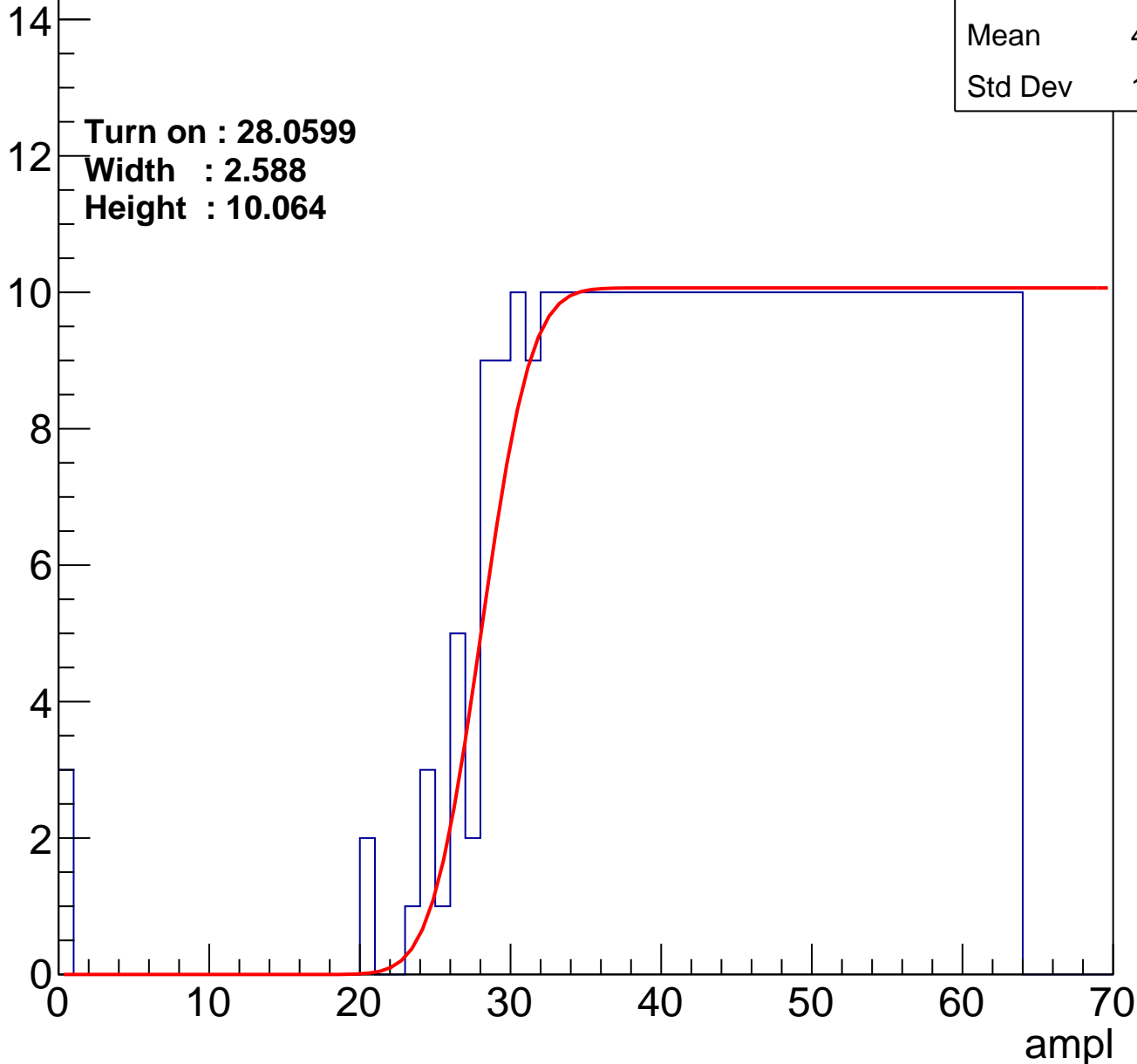
Entry

Entries	374
Mean	44.48
Std Dev	11.57

Turn on : 28.0599

Width : 2.588

Height : 10.064



# B0L001S, U9-ch85

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	363
Mean	44.88
Std Dev	11.61

**Turn on : 27.5710**

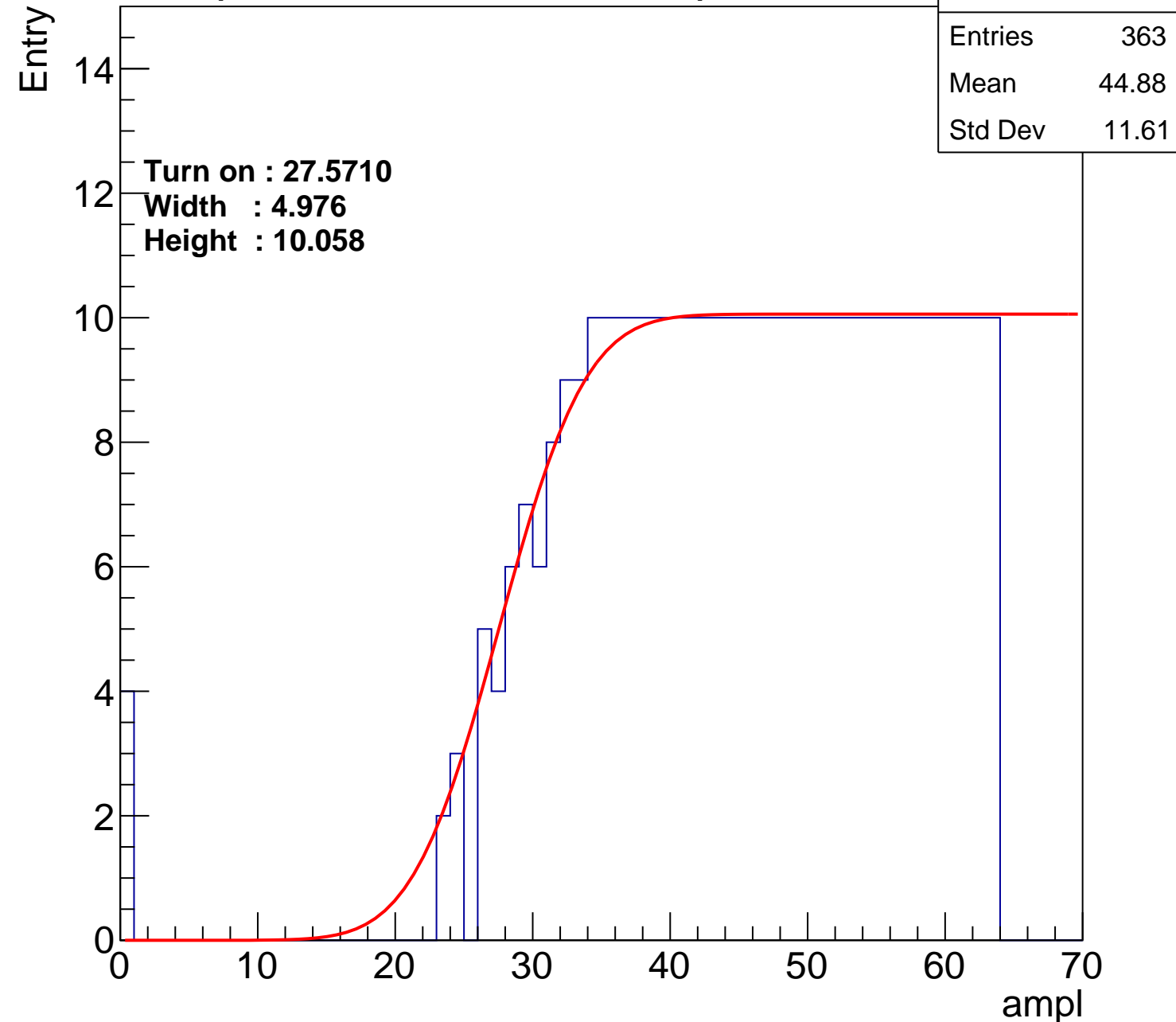
**Width : 4.976**

**Height : 10.058**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U9-ch86

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	375
Mean	44.39
Std Dev	11.65

Turn on : 26.8315

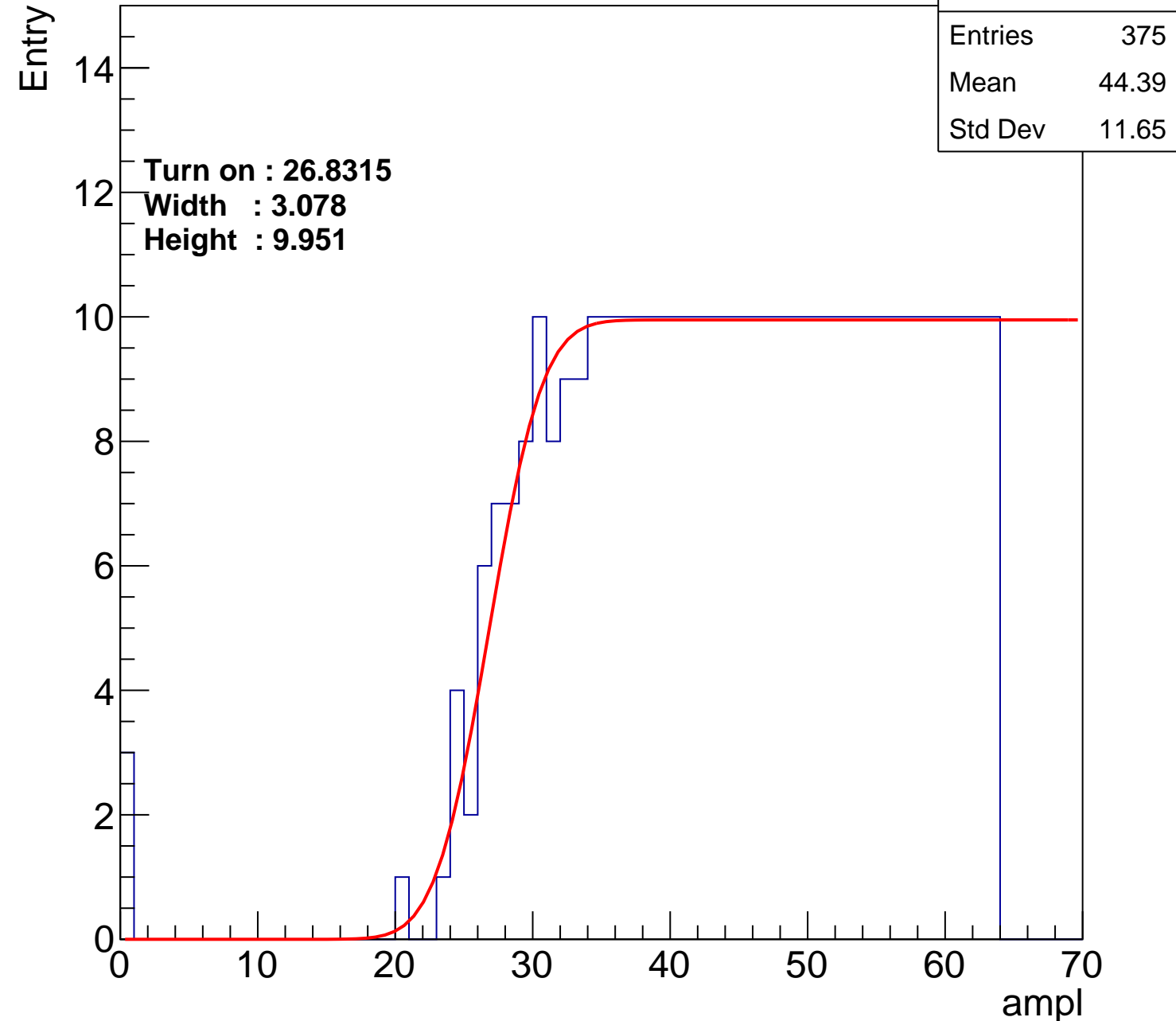
Width : 3.078

Height : 9.951

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B0L001S, U9-ch87

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	348
Mean	45.75
Std Dev	10.96

Turn on : 30.2861

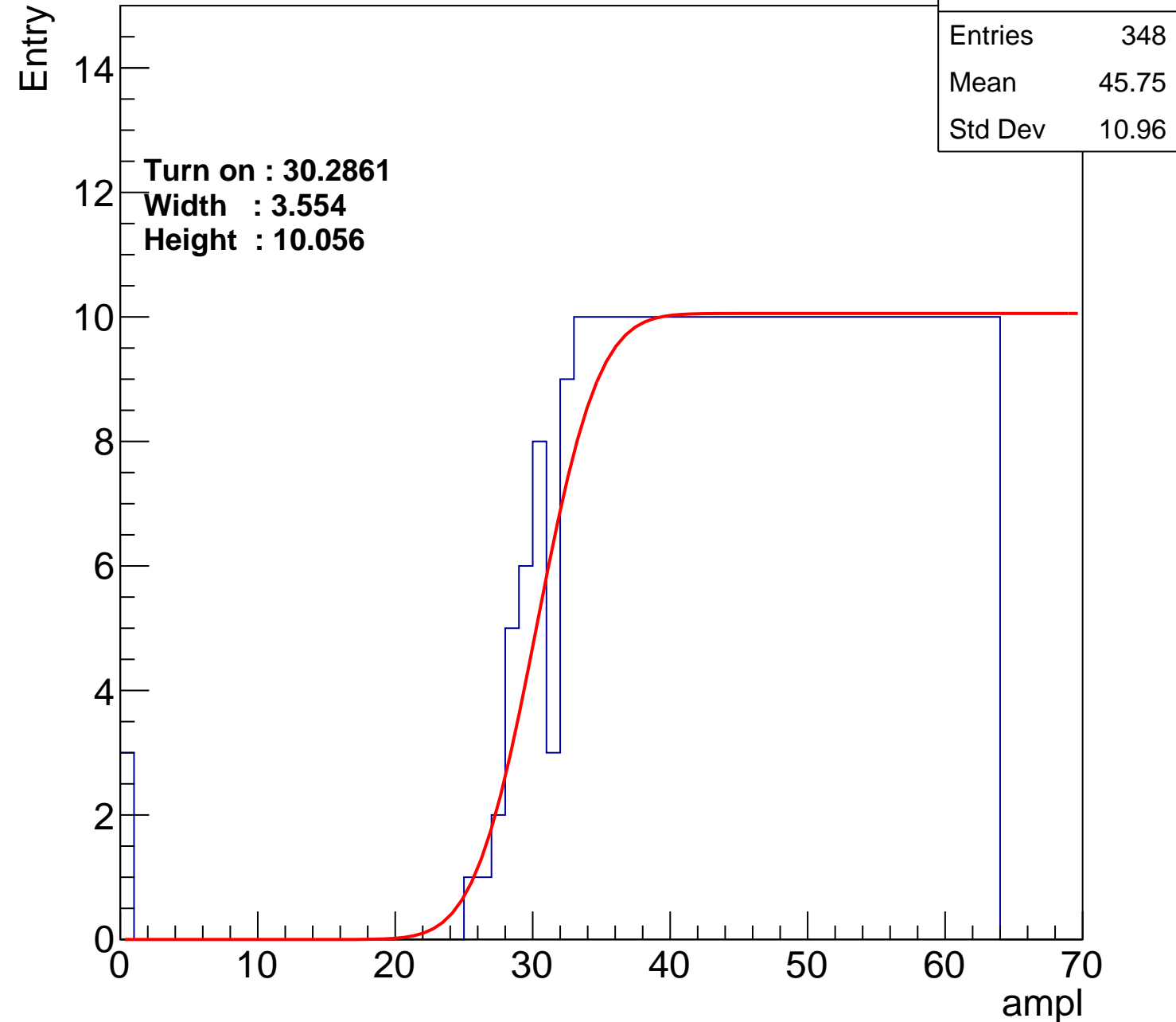
Width : 3.554

Height : 10.056

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U9-ch88

calib\_packv5\_042523\_0143.root, FC#9, port A1

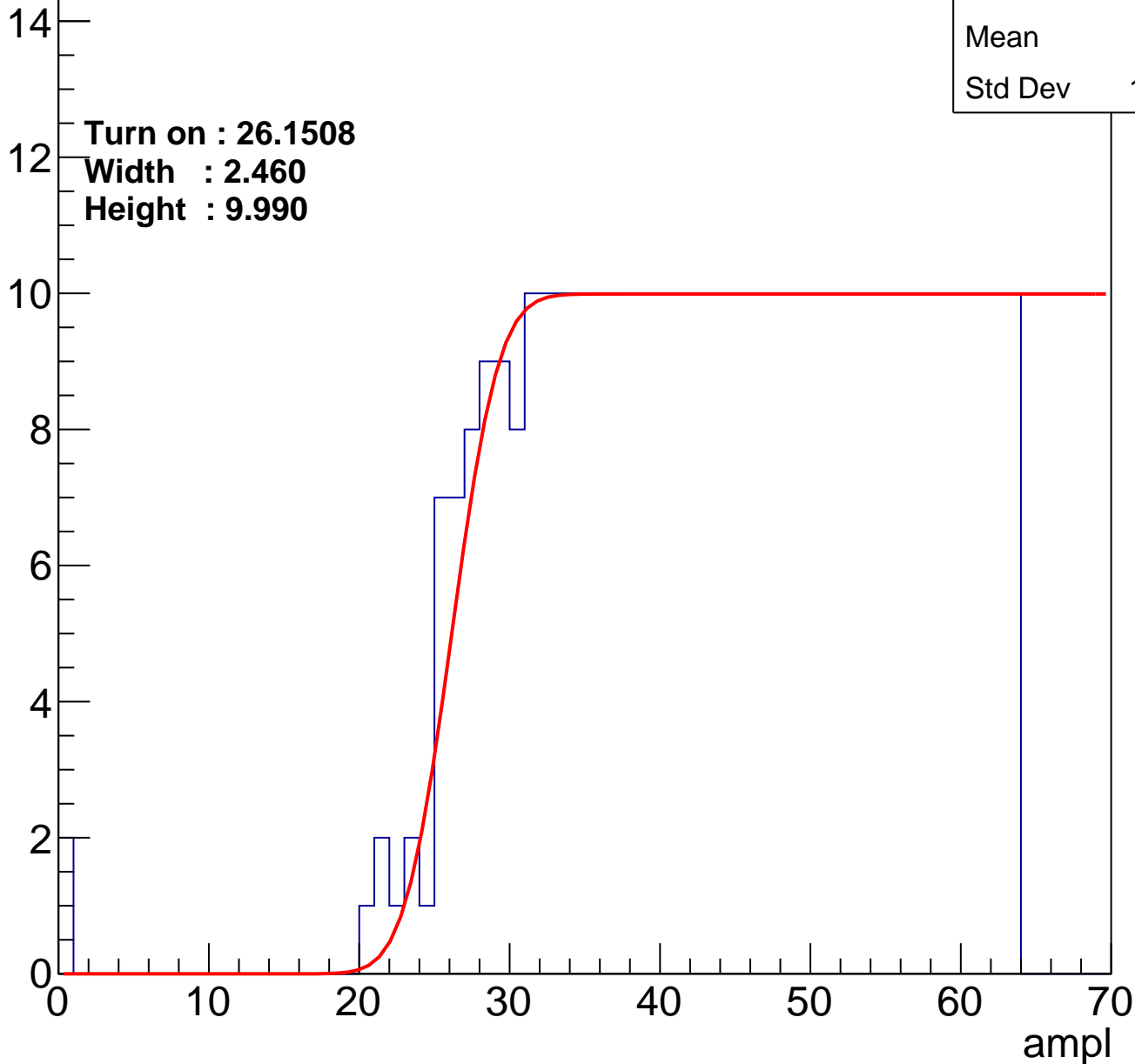
Entry

Entries	387
Mean	43.9
Std Dev	11.72

Turn on : 26.1508

Width : 2.460

Height : 9.990



# B0L001S, U9-ch89

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	371
Mean	44.61
Std Dev	11.51

Turn on : 26.9671

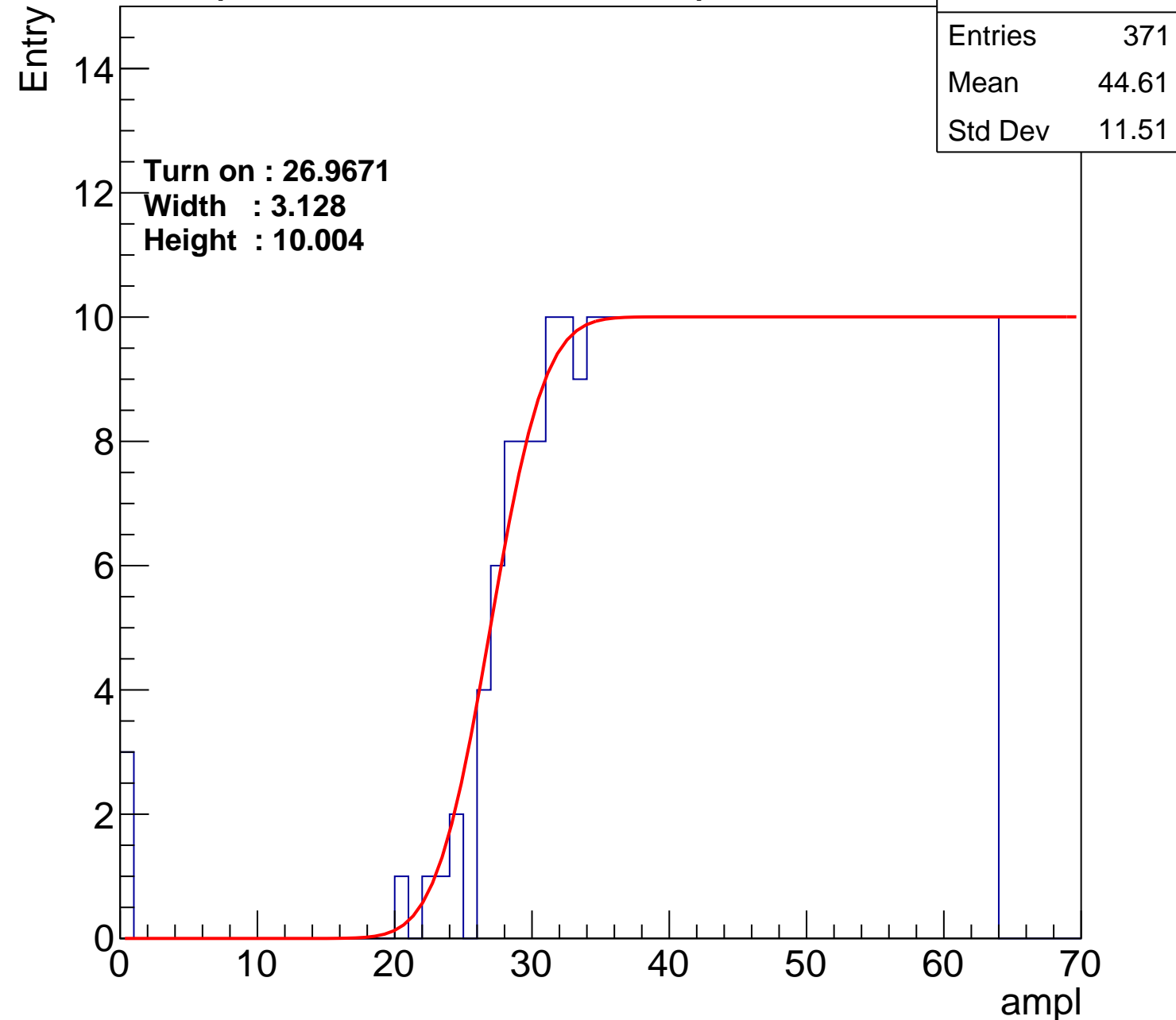
Width : 3.128

Height : 10.004

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U9-ch90

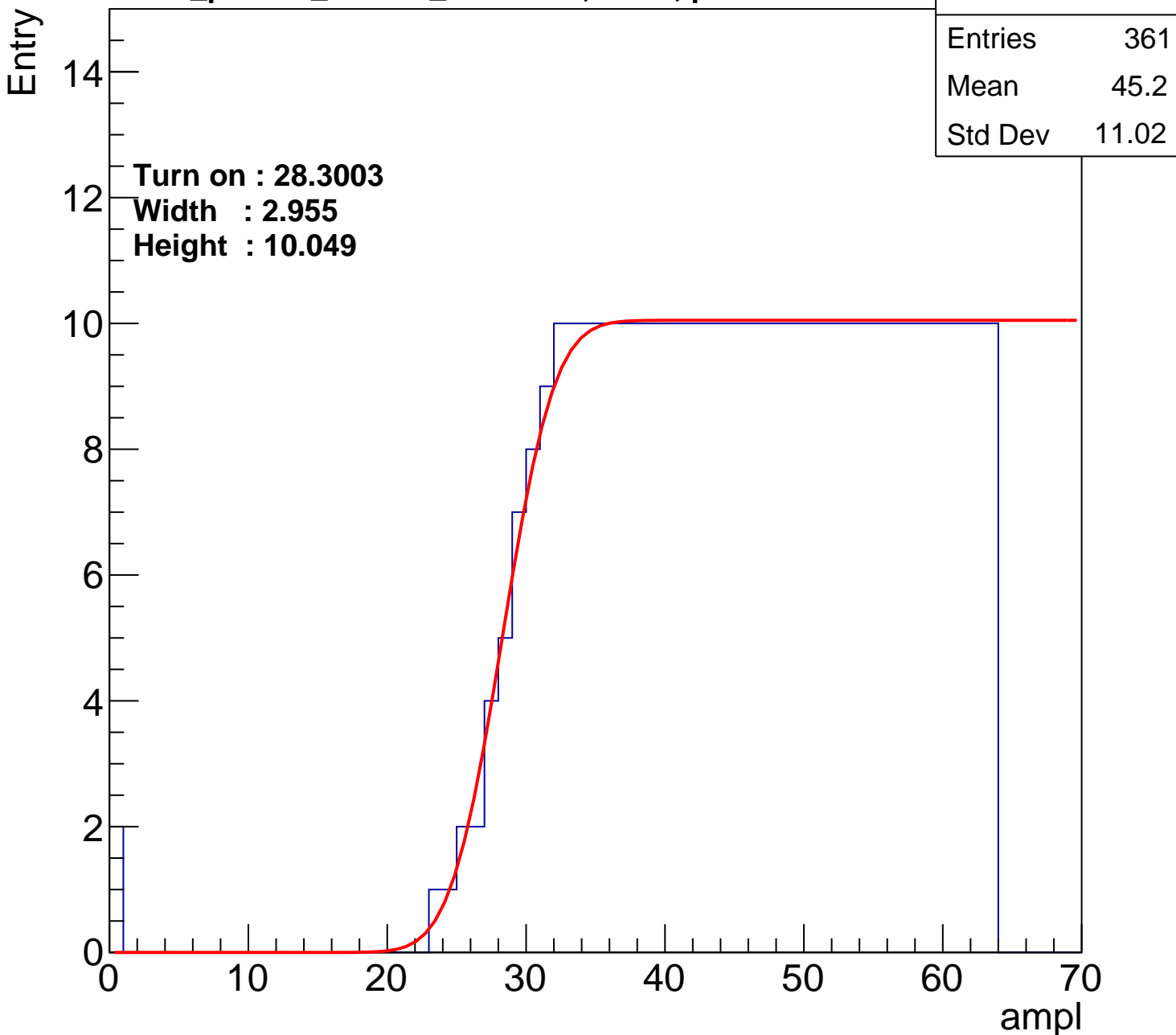
**calib\_packv5\_042523\_0143.root, FC#9, port A1**

**Turn on : 28.3003**

**Width : 2.955**

**Height : 10.049**

Entries	361
Mean	45.2
Std Dev	11.02



# B0L001S, U9-ch91

calib\_packv5\_042523\_0143.root, FC#9, port A1

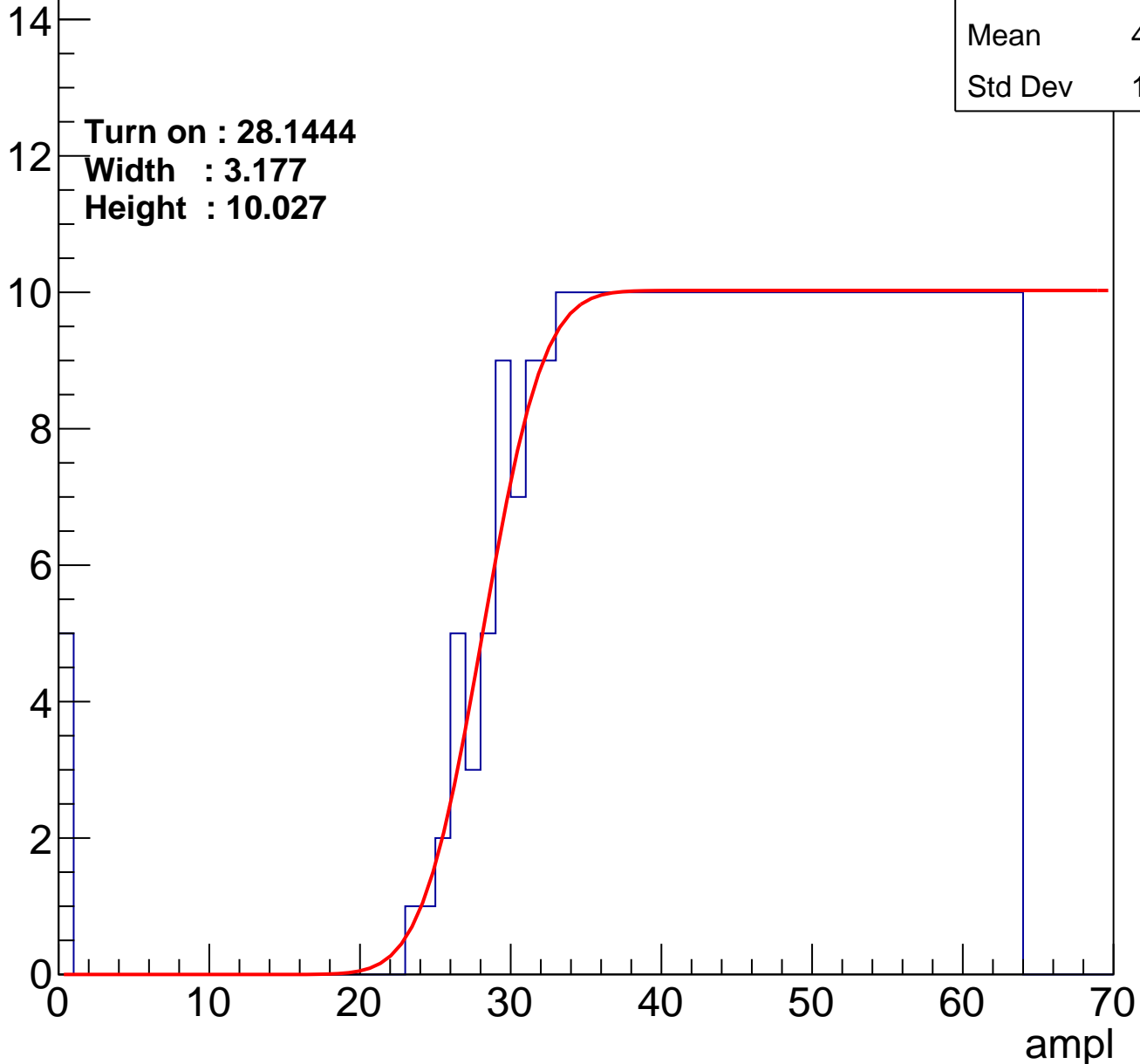
Entries	366
Mean	44.72
Std Dev	11.78

Turn on : 28.1444

Width : 3.177

Height : 10.027

Entry



# B0L001S, U9-ch92

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	352
Mean	45.43
Std Dev	11.35

Turn on : 29.5887

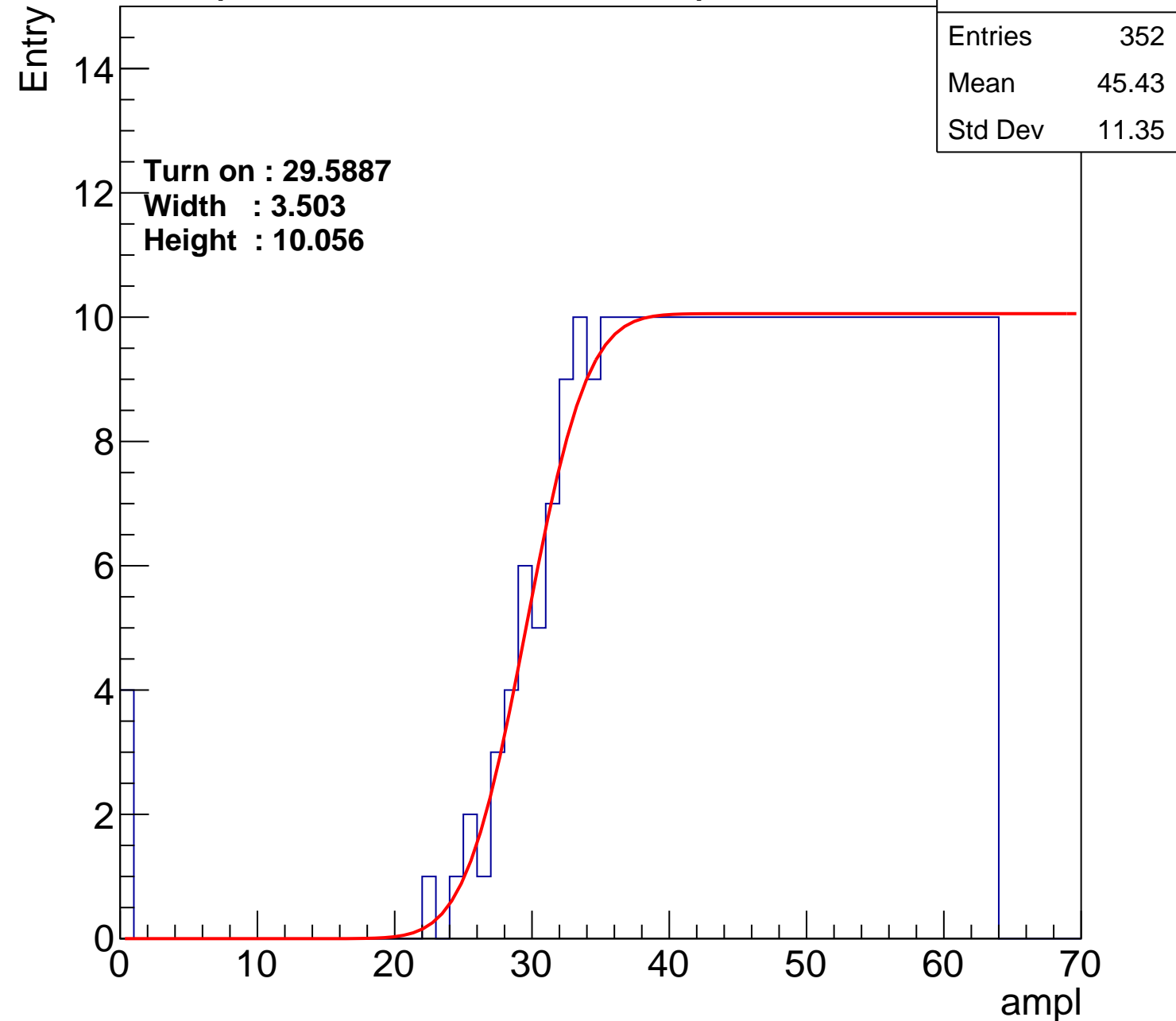
Width : 3.503

Height : 10.056

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U9-ch93

calib\_packv5\_042523\_0143.root, FC#9, port A1

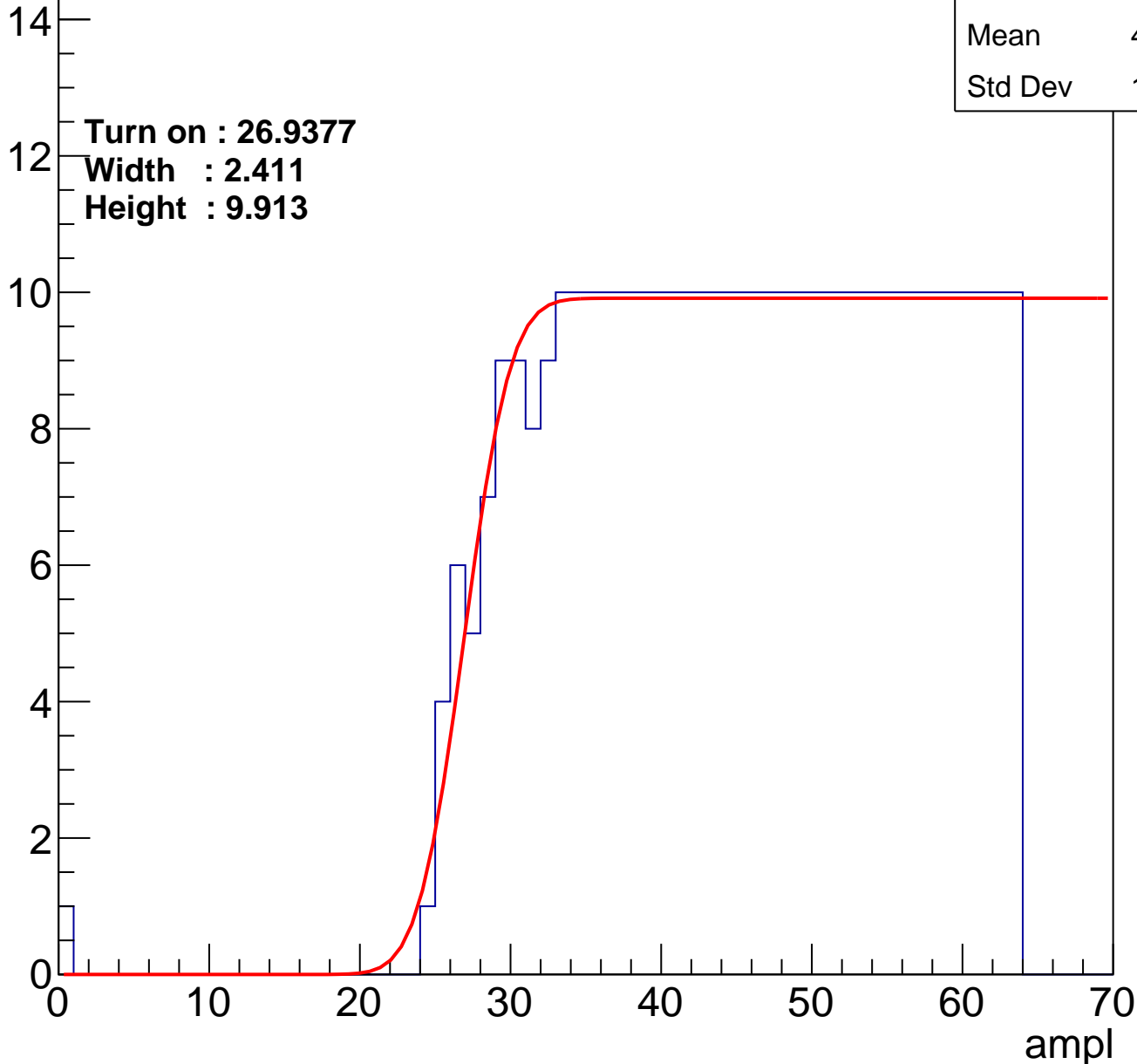
Entry

Entries	369
Mean	44.87
Std Dev	11.03

Turn on : 26.9377

Width : 2.411

Height : 9.913



# B0L001S, U9-ch94

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	366
Mean	44.9
Std Dev	11.25

Turn on : 28.1666

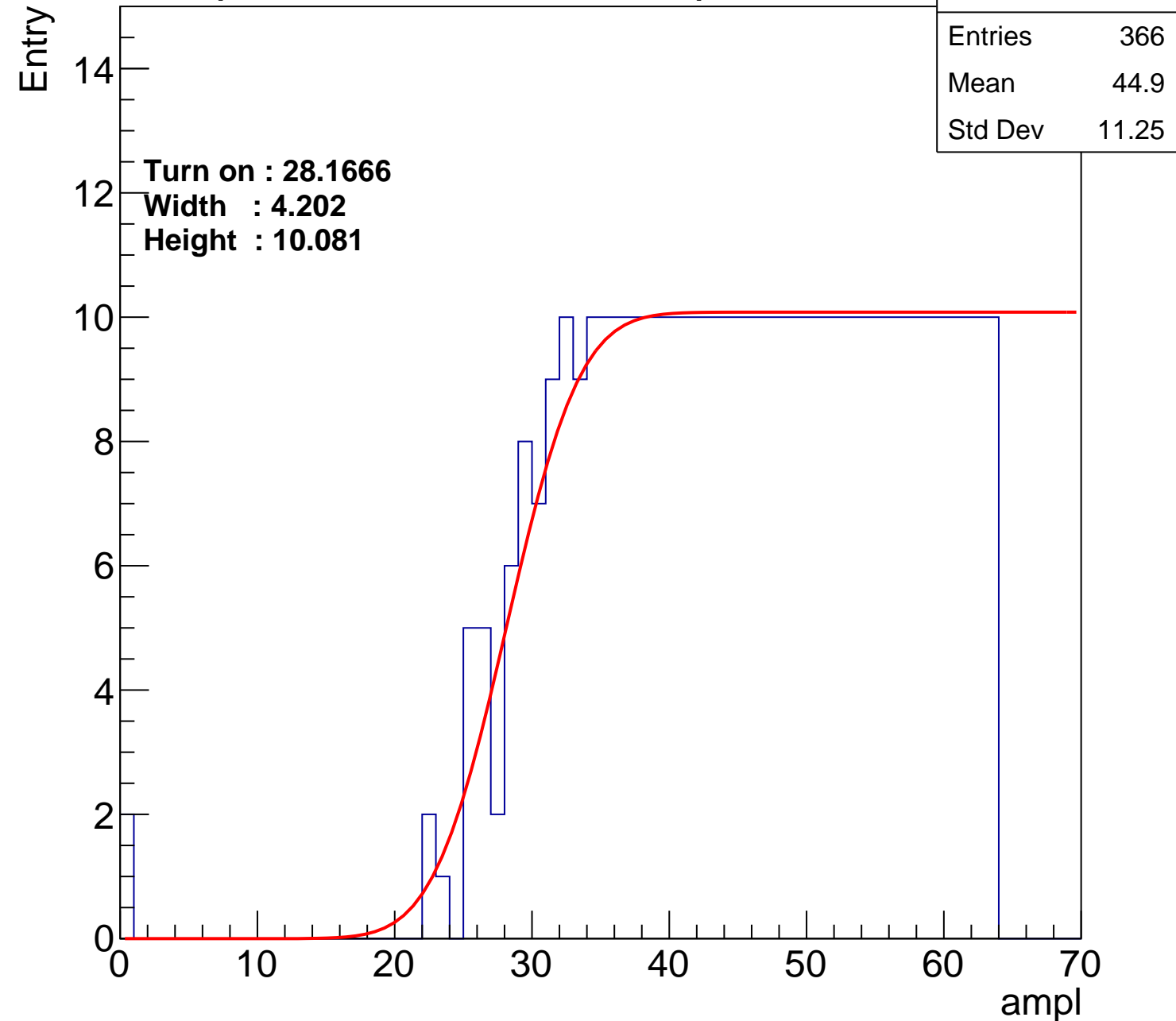
Width : 4.202

Height : 10.081

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B0L001S, U9-ch95

calib\_packv5\_042523\_0143.root, FC#9, port A1

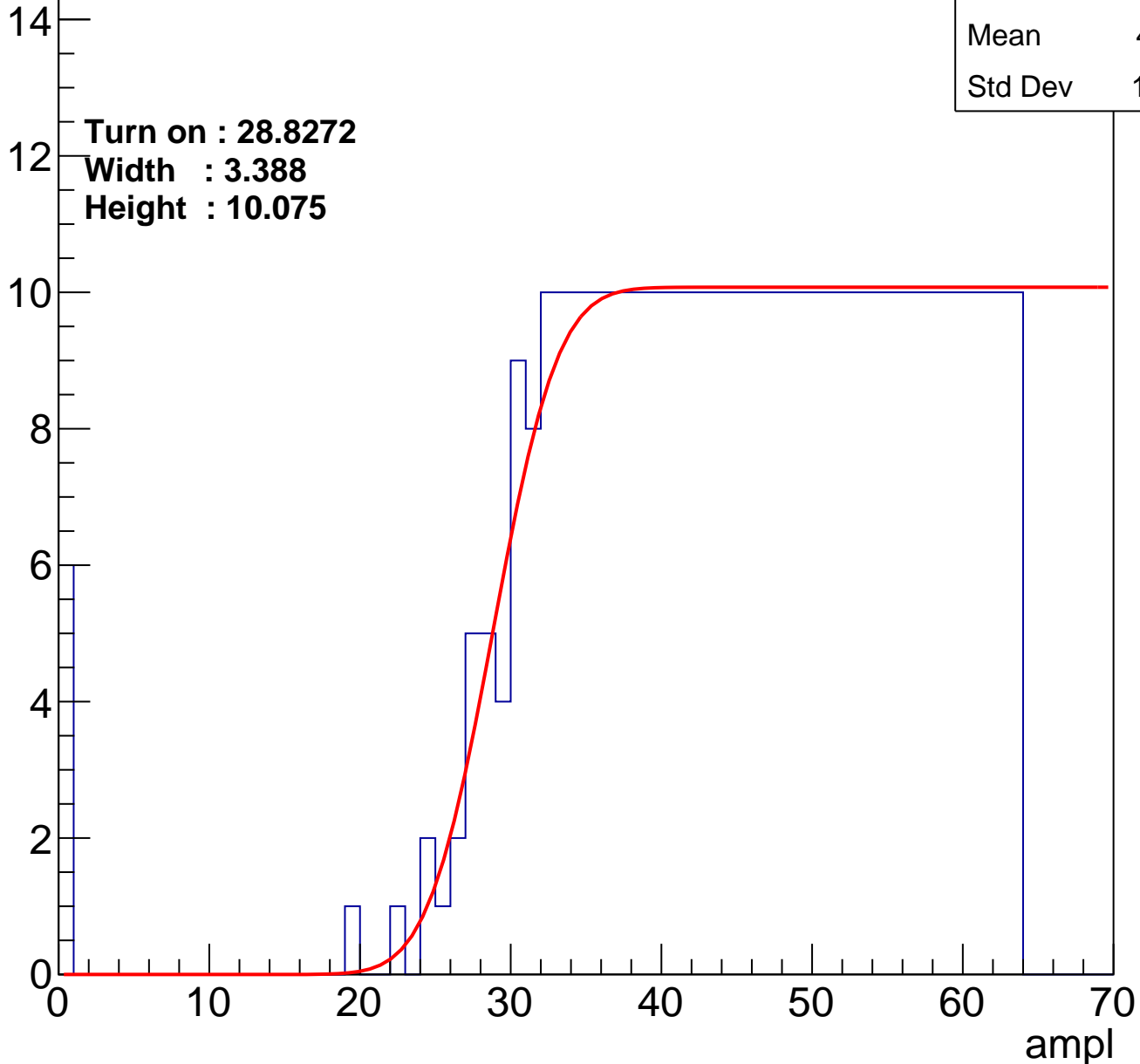
Entries	364
Mean	44.71
Std Dev	11.99

Turn on : 28.8272

Width : 3.388

Height : 10.075

Entry



# B0L001S, U9-ch96

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	373
Mean	44.58
Std Dev	11.37

Turn on : 26.8844

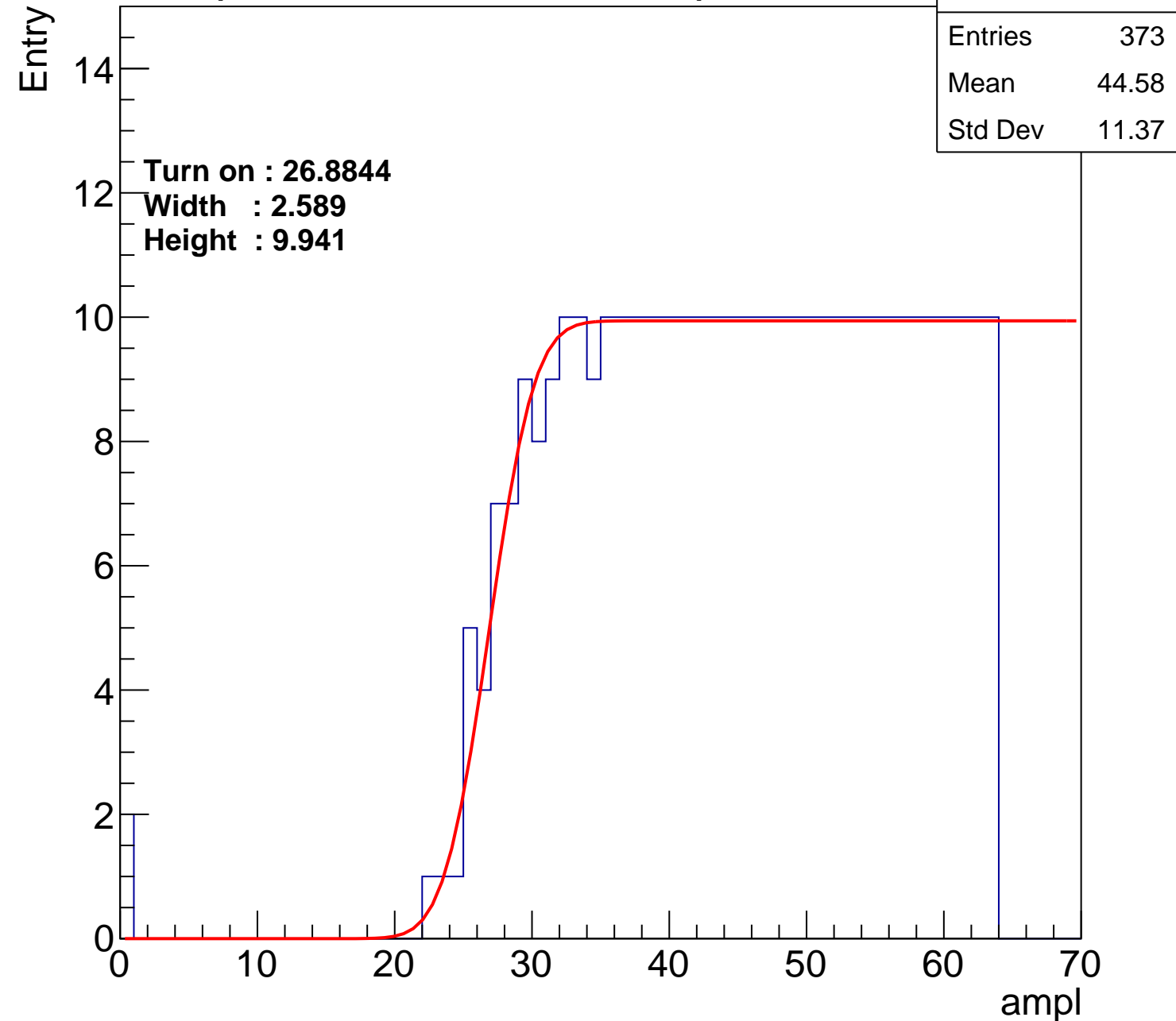
Width : 2.589

Height : 9.941

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U9-ch97

calib\_packv5\_042523\_0143.root, FC#9, port A1

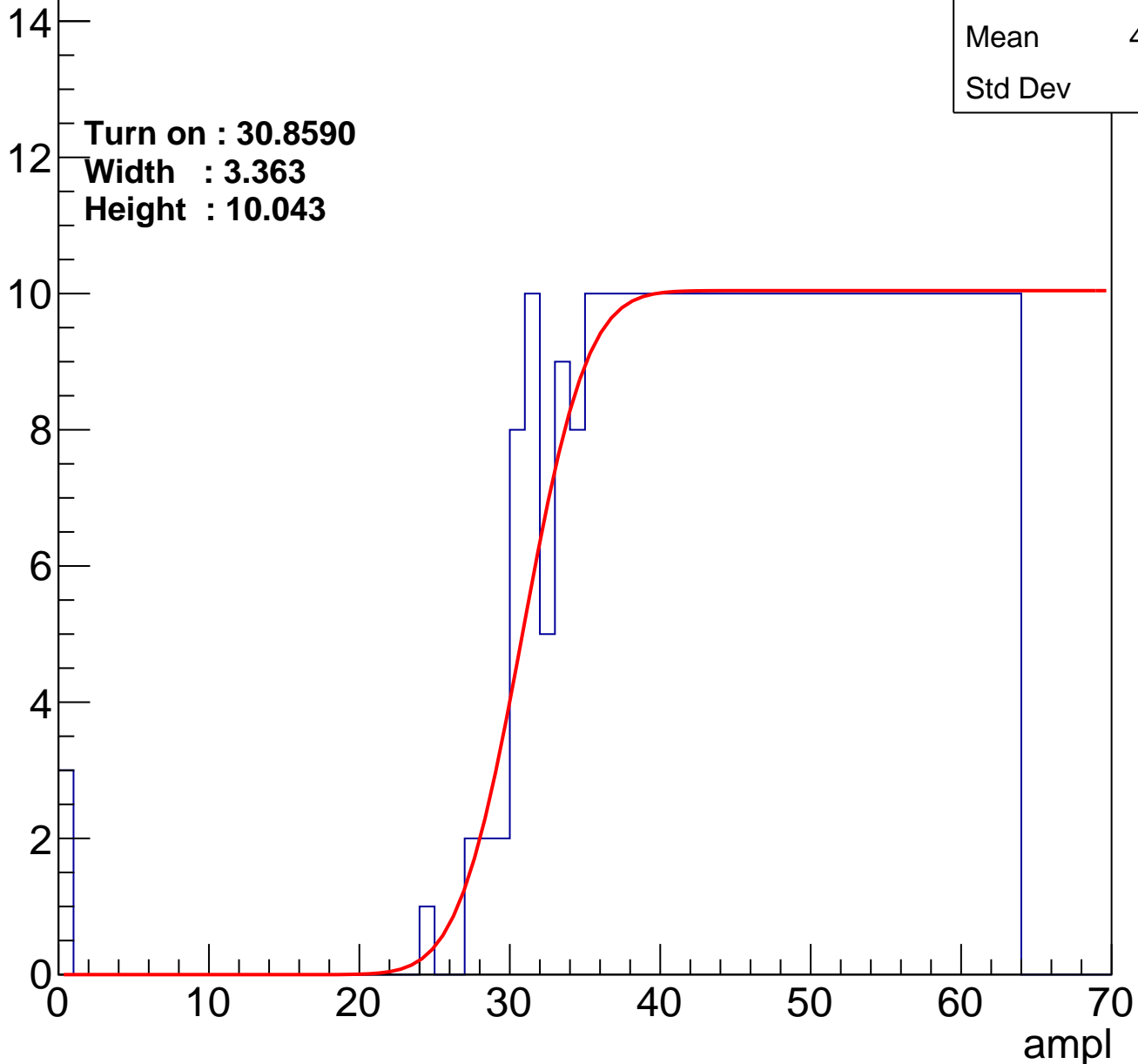
Entry

Entries	340
Mean	46.12
Std Dev	10.8

Turn on : 30.8590

Width : 3.363

Height : 10.043



# B0L001S, U9-ch98

calib\_packv5\_042523\_0143.root, FC#9, port A1

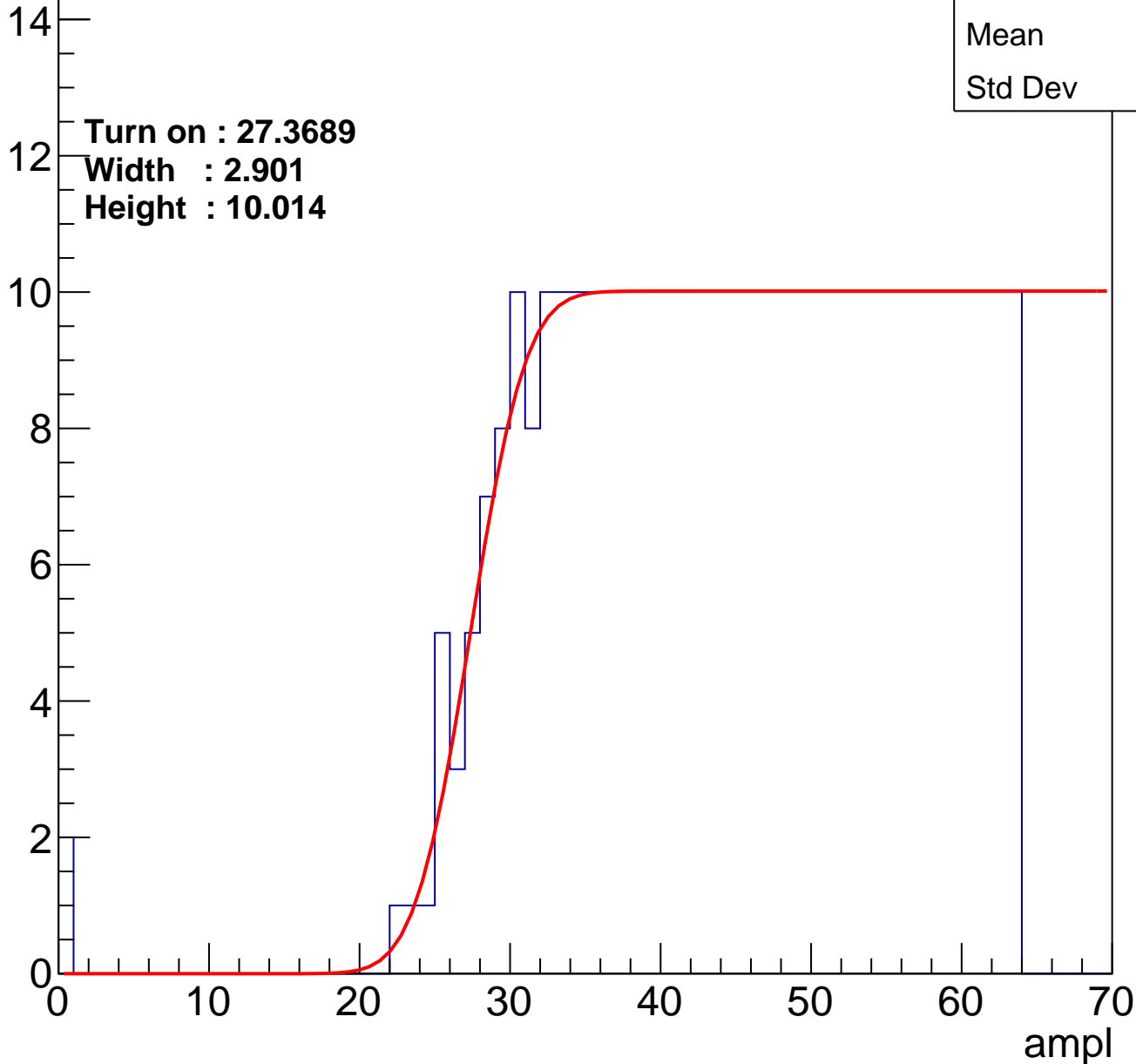
Entry

Entries	371
Mean	44.7
Std Dev	11.3

Turn on : 27.3689

Width : 2.901

Height : 10.014



# B0L001S, U9-ch99

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	368
Mean	44.43
Std Dev	12.26

Turn on : 28.4434

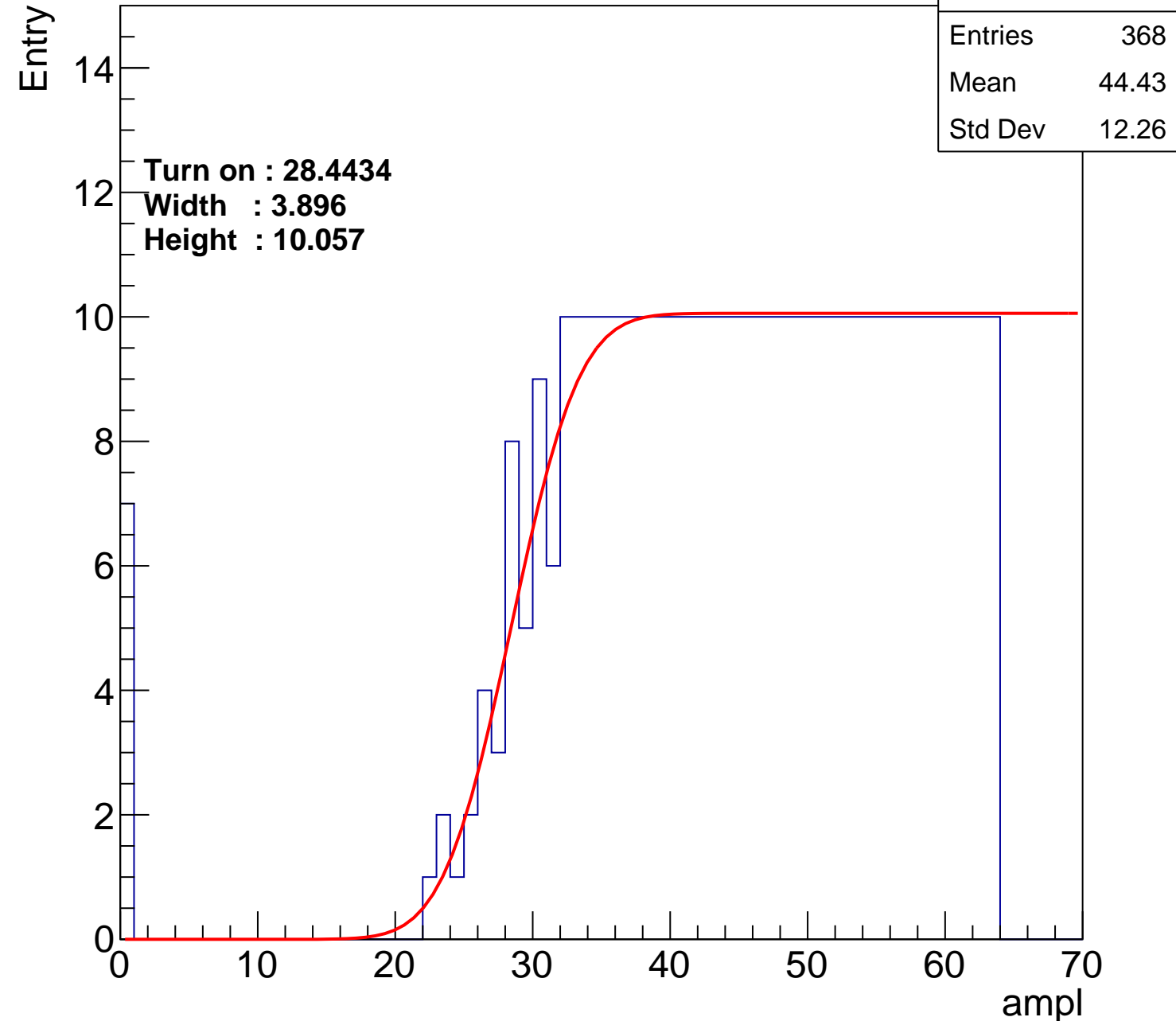
Width : 3.896

Height : 10.057

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U9-ch100

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	383
Mean	43.89
Std Dev	12.16

Turn on : 25.8206

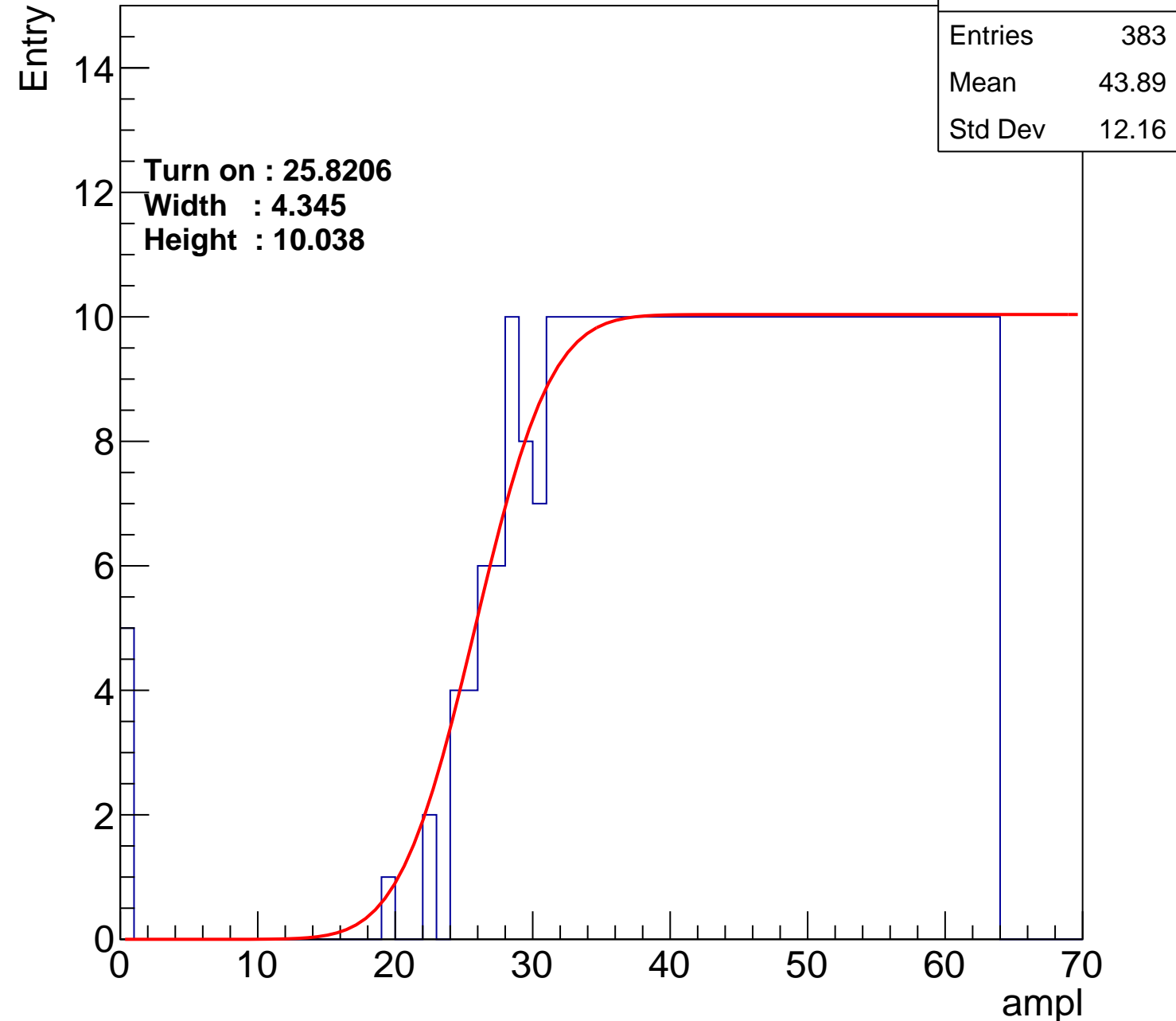
Width : 4.345

Height : 10.038

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U9-ch101

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	357
Mean	45.41
Std Dev	10.9

**Turn on : 29.1585**

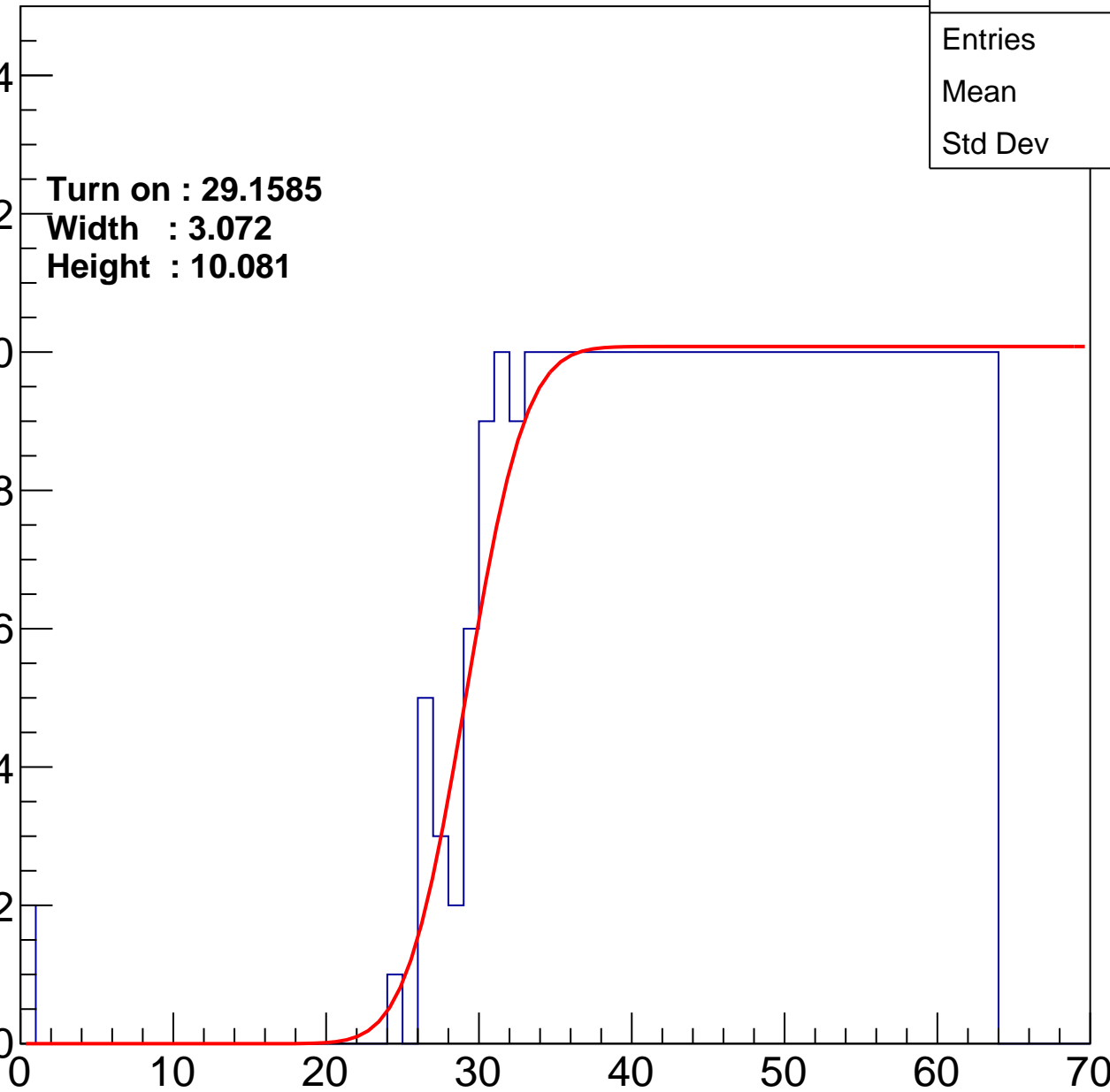
**Width : 3.072**

**Height : 10.081**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U9-ch102

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	374
Mean	44.47
Std Dev	11.57

Turn on : 26.9966

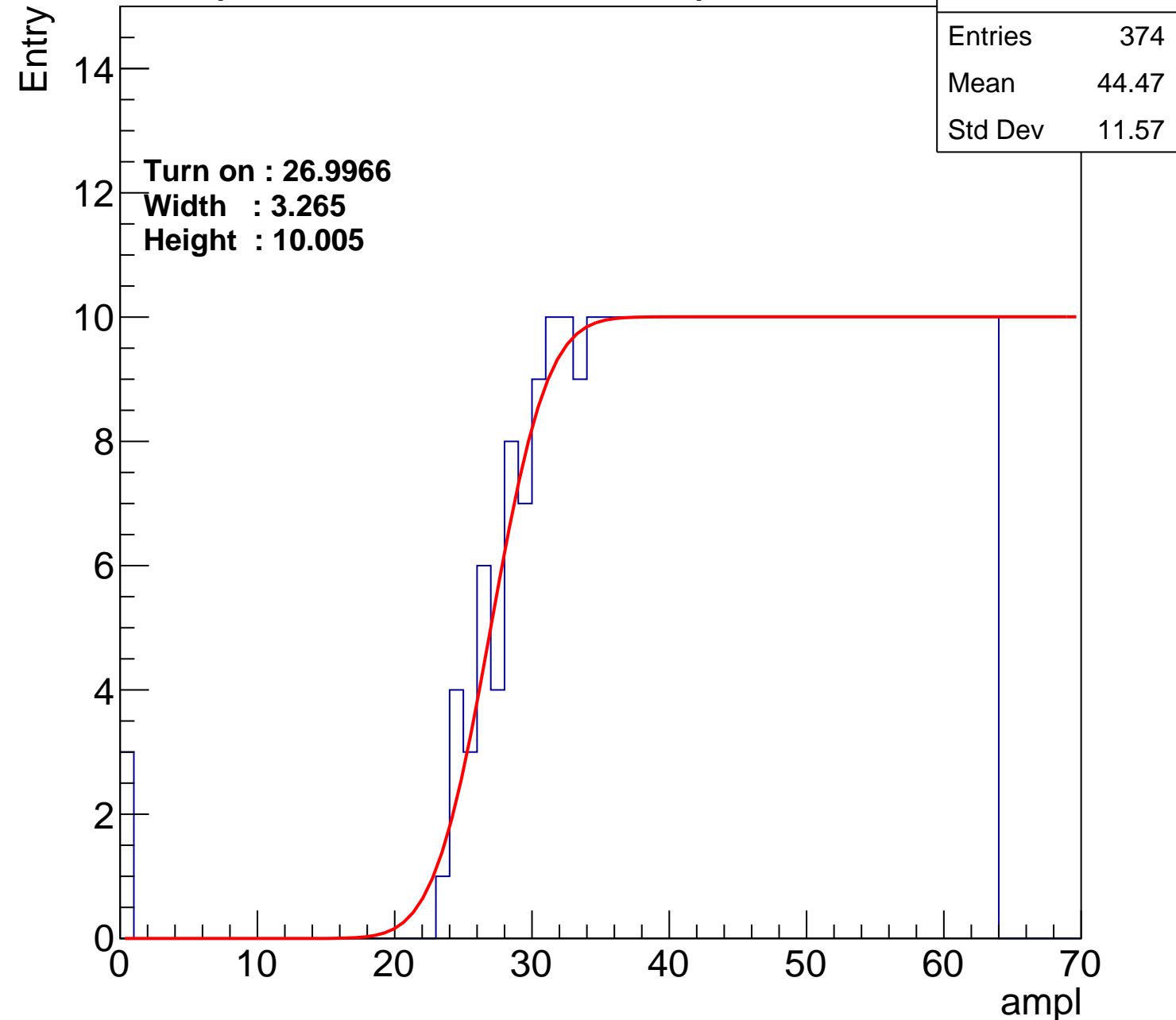
Width : 3.265

Height : 10.005

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B0L001S, U9-ch103

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	355
Mean	45.32
Std Dev	11.35

Turn on : 29.2720

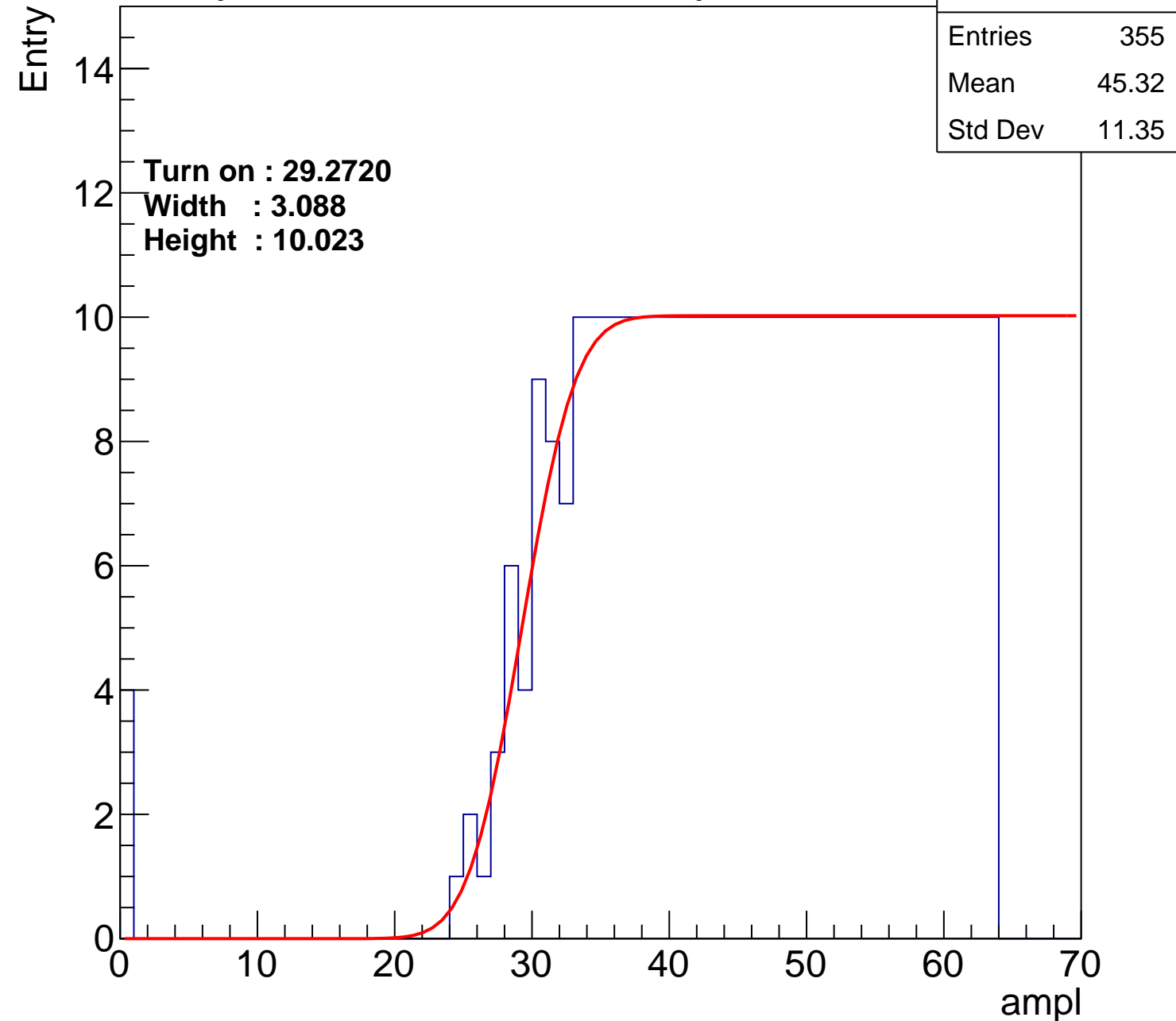
Width : 3.088

Height : 10.023

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U9-ch104

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	377
Mean	44.26
Std Dev	11.83

Turn on : 27.0352

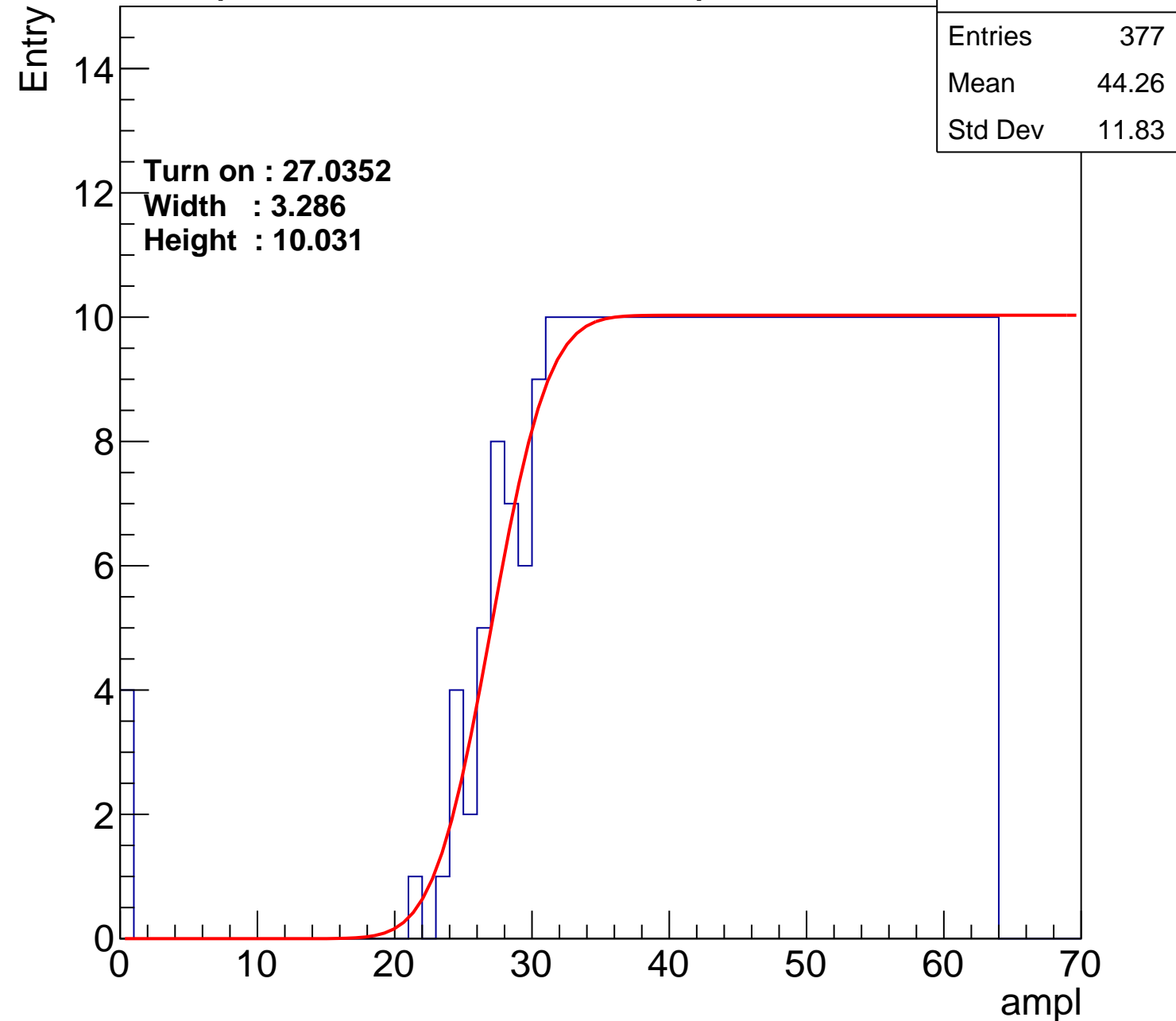
Width : 3.286

Height : 10.031

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U9-ch105

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	364
Mean	44.66
Std Dev	12.13

Turn on : 28.1841

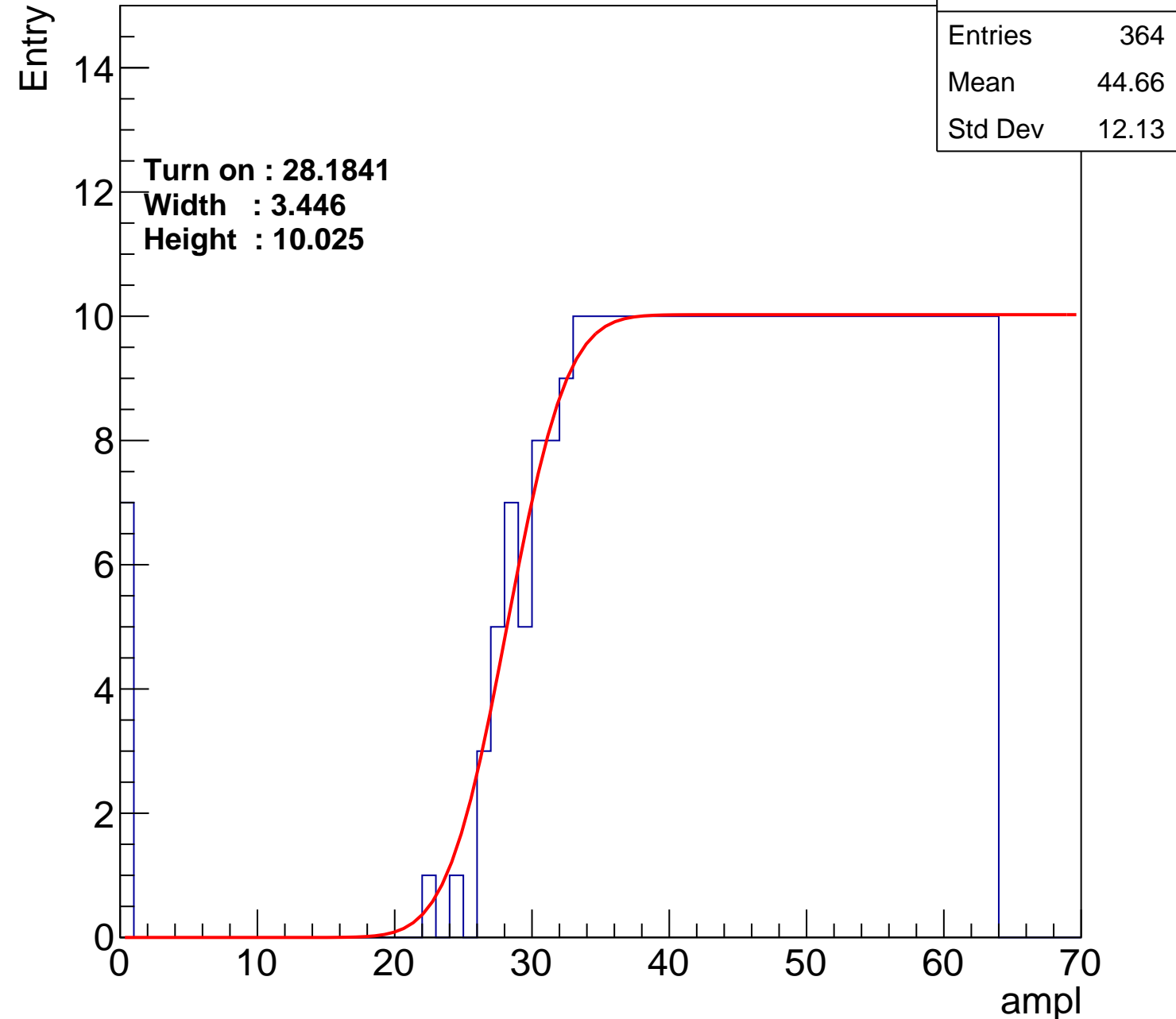
Width : 3.446

Height : 10.025

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U9-ch106

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	361
Mean	44.97
Std Dev	11.66

**Turn on : 28.8193**

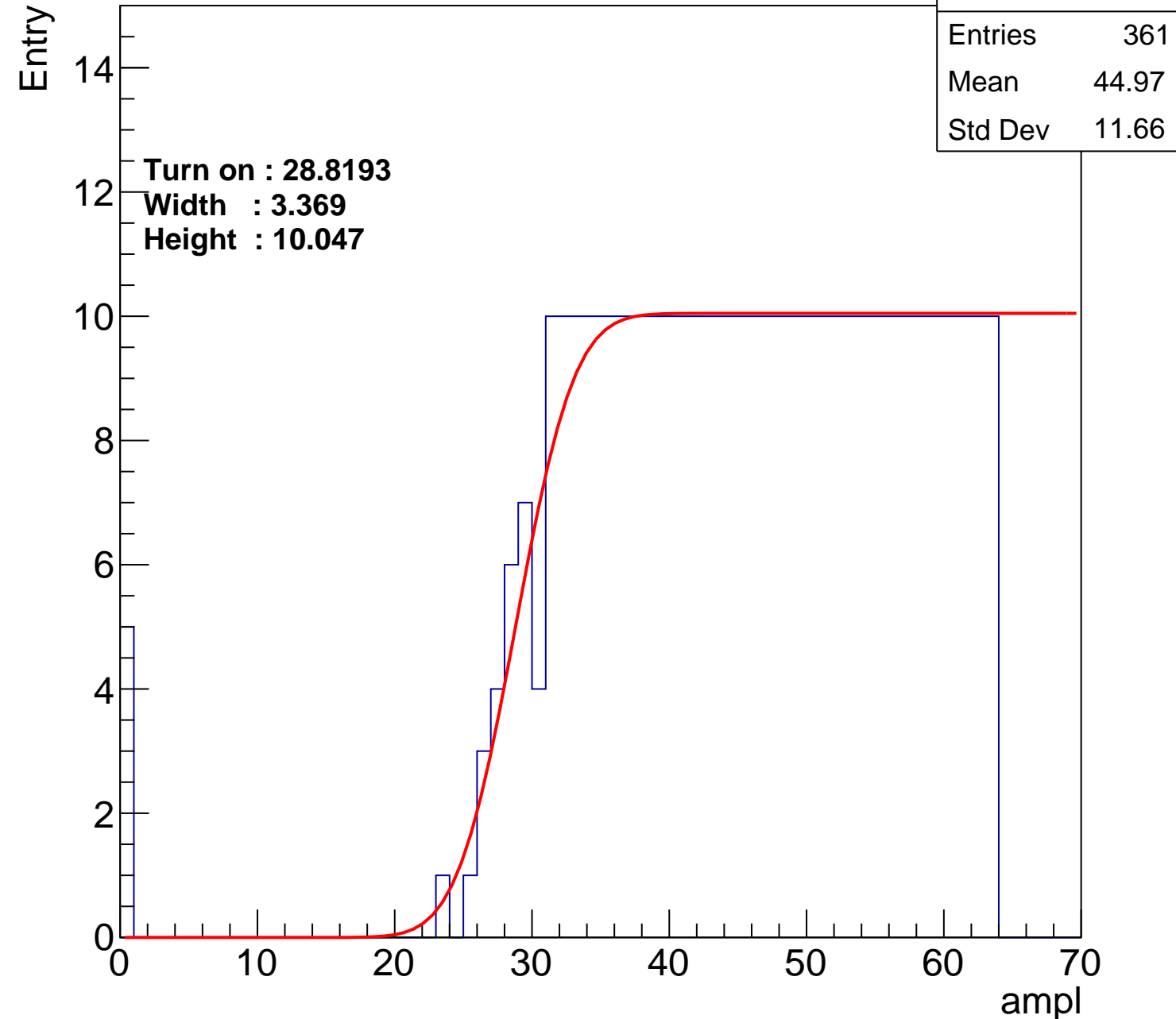
**Width : 3.369**

**Height : 10.047**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U9-ch107

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	379
Mean	44.13
Std Dev	11.92

Turn on : 26.5541

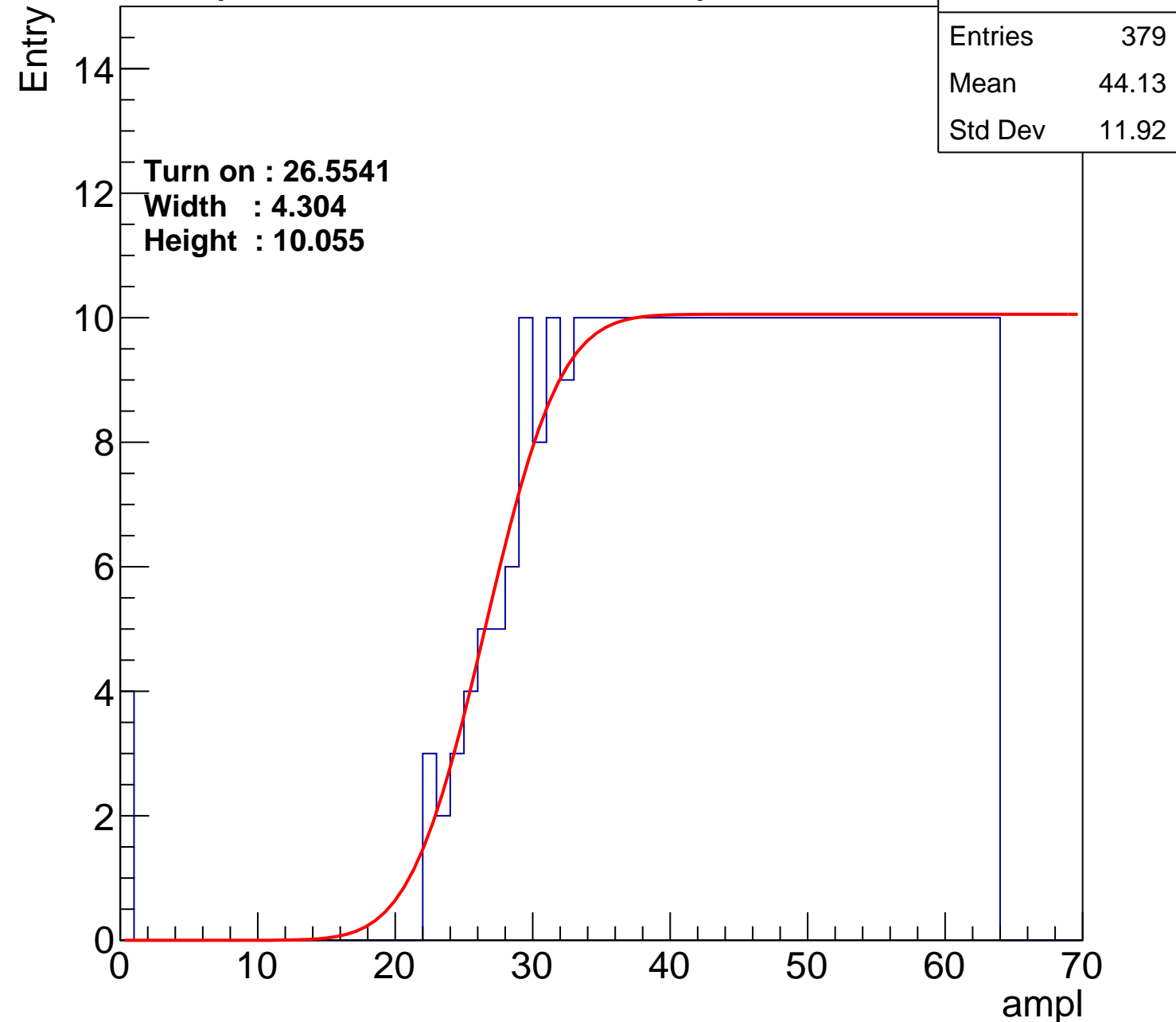
Width : 4.304

Height : 10.055

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U9-ch108

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	364
Mean	44.98
Std Dev	11.22

Turn on : 28.1251

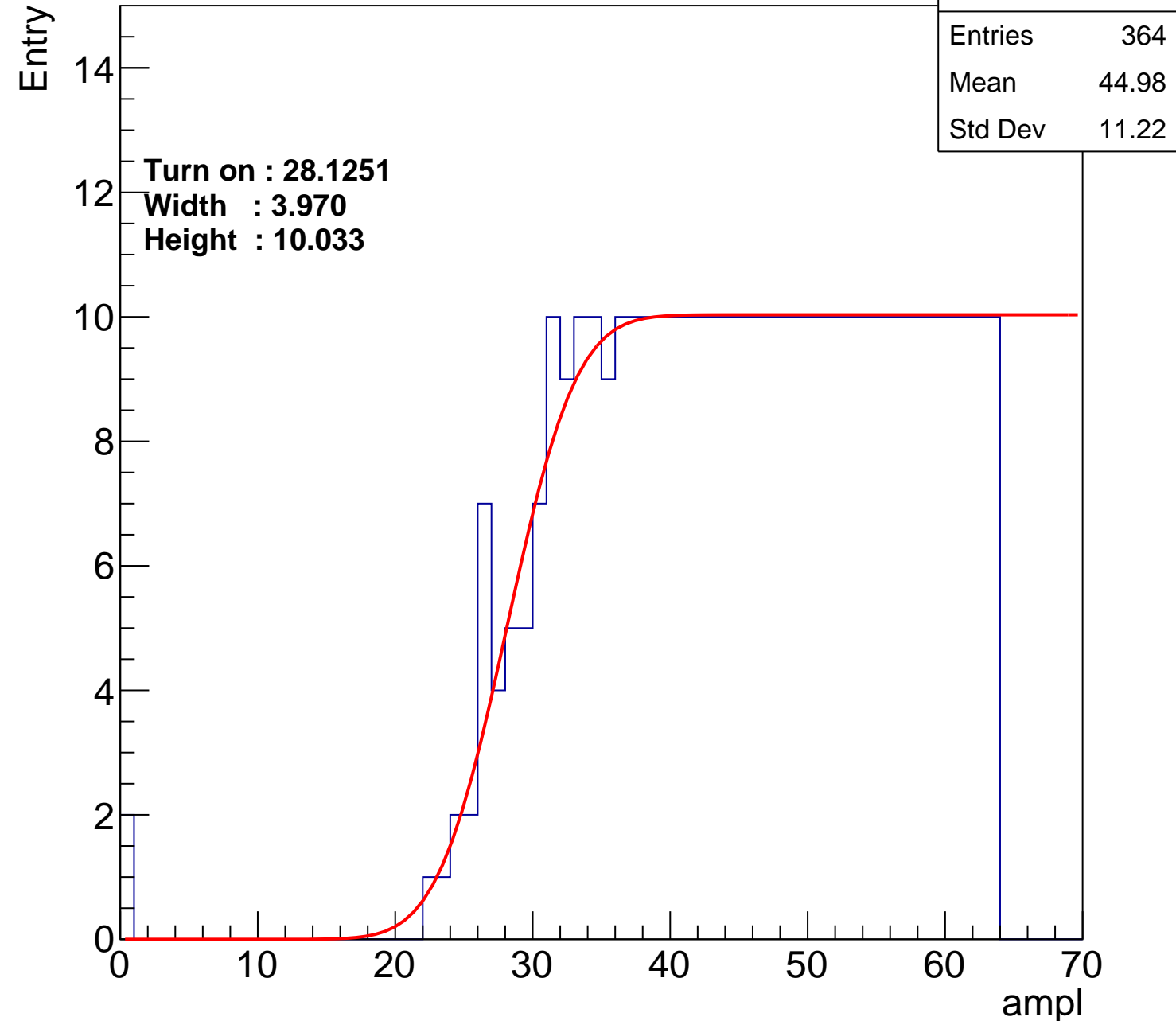
Width : 3.970

Height : 10.033

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U9-ch109

calib\_packv5\_042523\_0143.root, FC#9, port A1

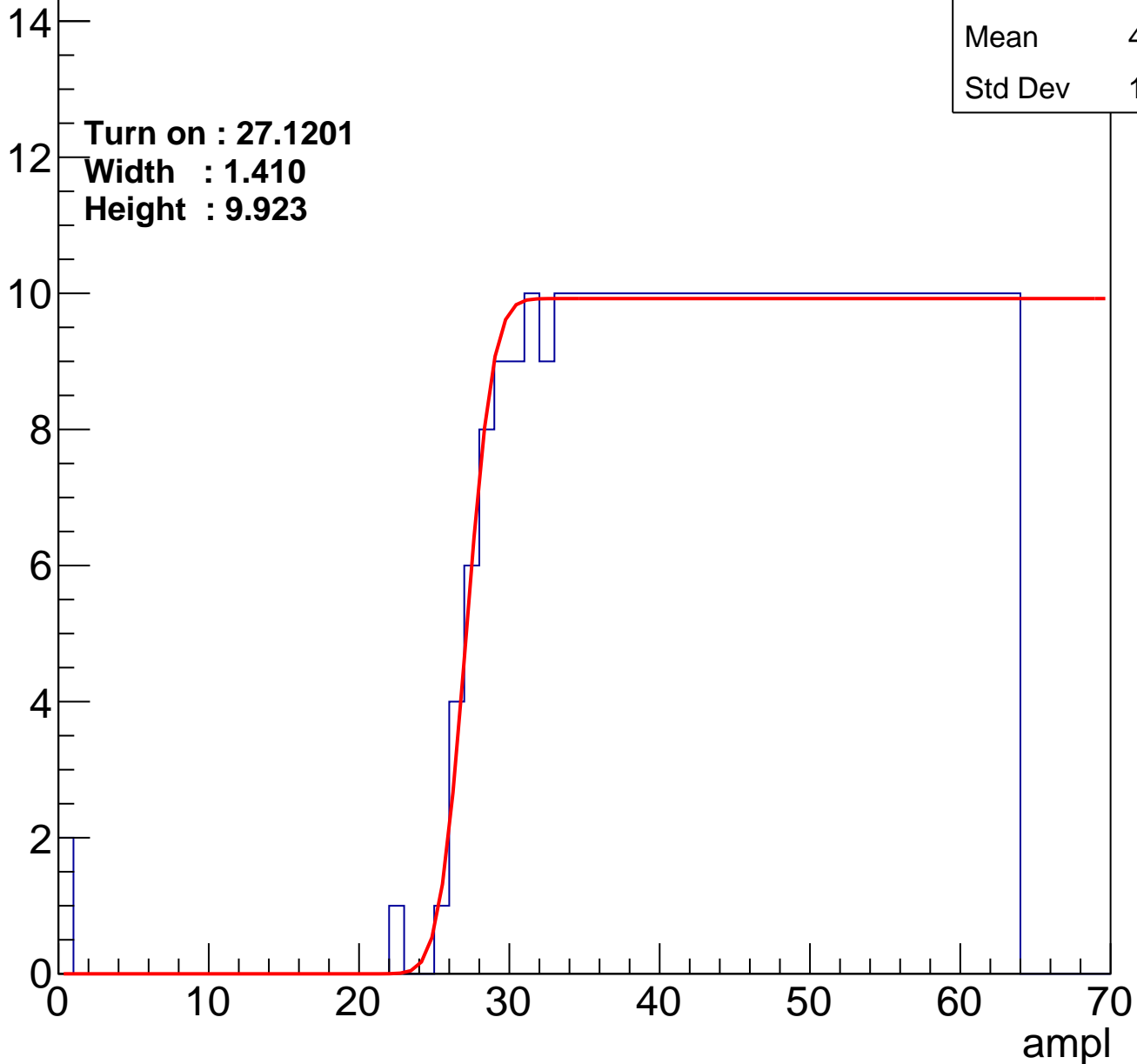
Entries	369
Mean	44.84
Std Dev	11.17

Turn on : 27.1201

Width : 1.410

Height : 9.923

Entry



# B0L001S, U9-ch110

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	360
Mean	45.26
Std Dev	10.99

**Turn on : 28.6015**

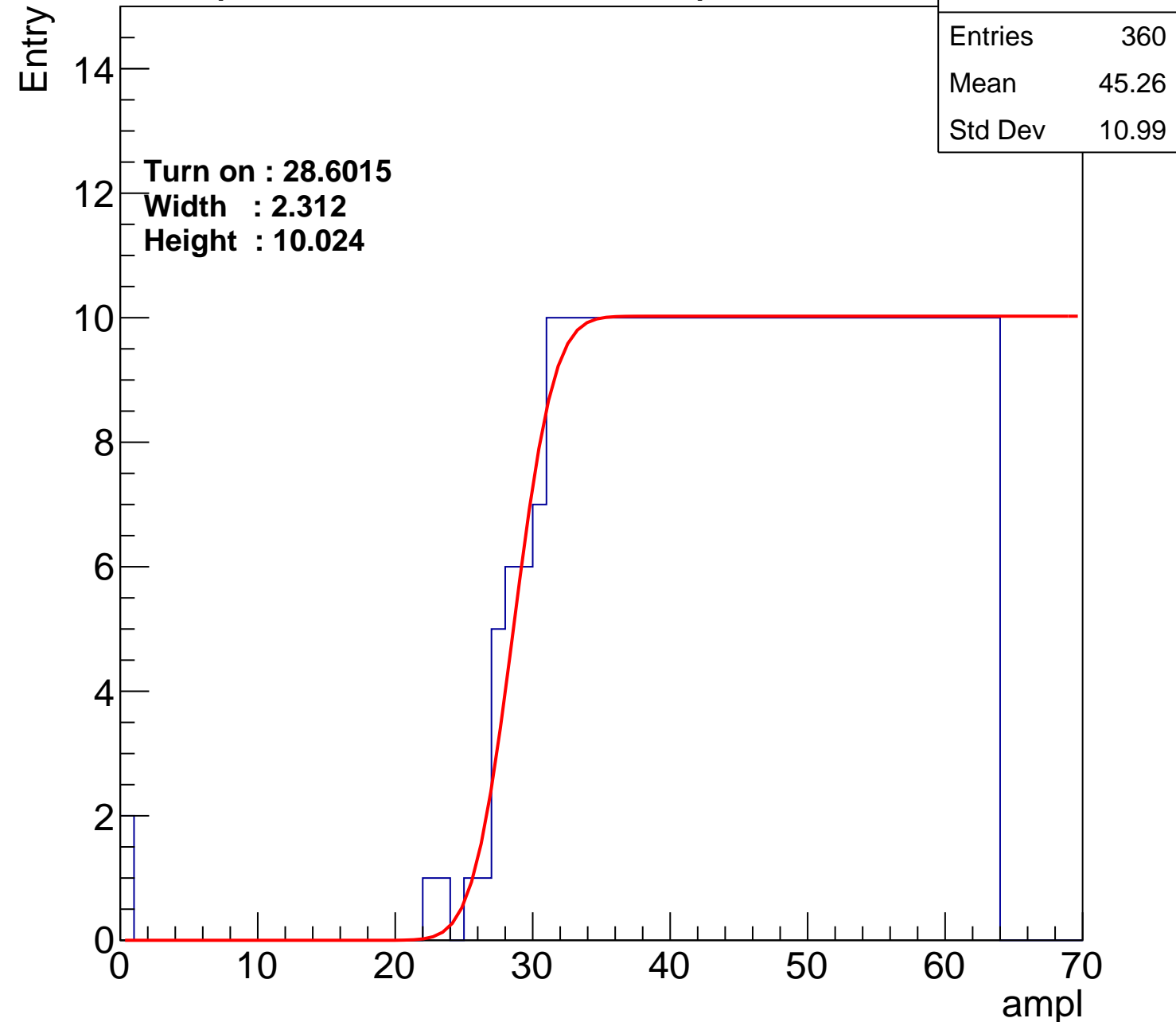
**Width : 2.312**

**Height : 10.024**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B0L001S, U9-ch111

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	357
Mean	45.17
Std Dev	11.47

Turn on : 28.9366

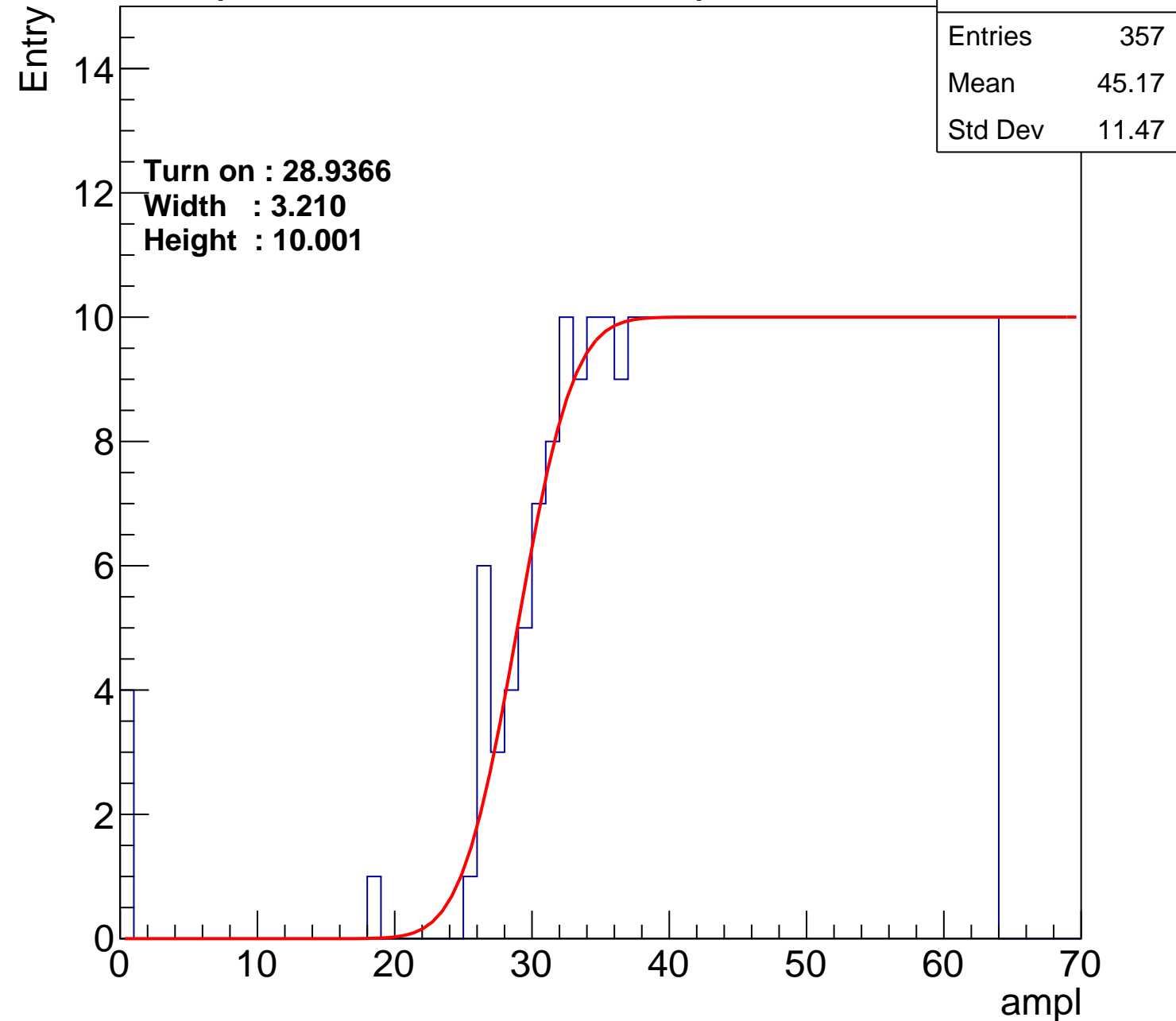
Width : 3.210

Height : 10.001

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U9-ch112

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	353
Mean	45.54
Std Dev	11.01

**Turn on : 28.7363**

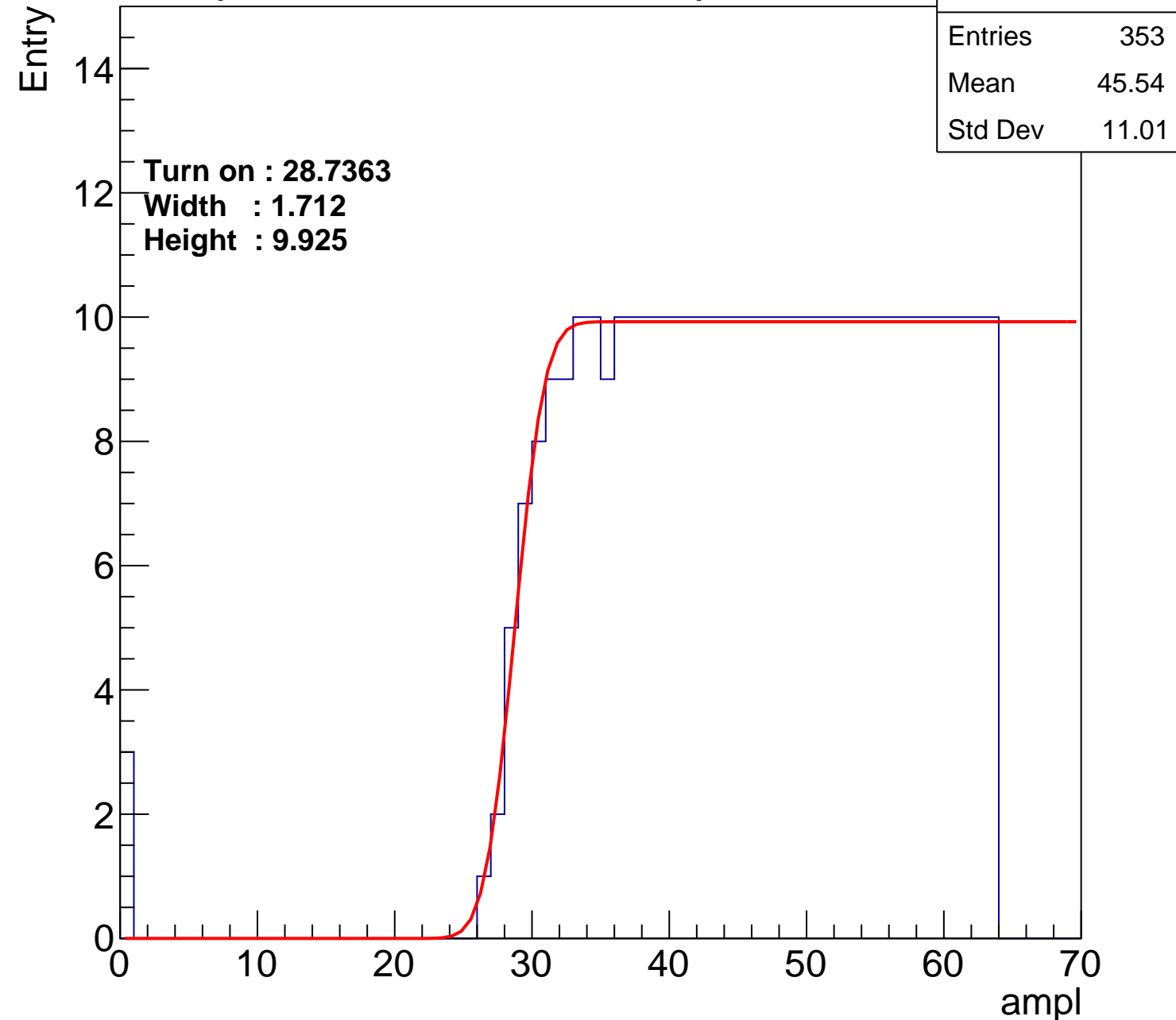
**Width : 1.712**

**Height : 9.925**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U9-ch113

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	365
Mean	44.71
Std Dev	11.93

**Turn on : 28.3745**

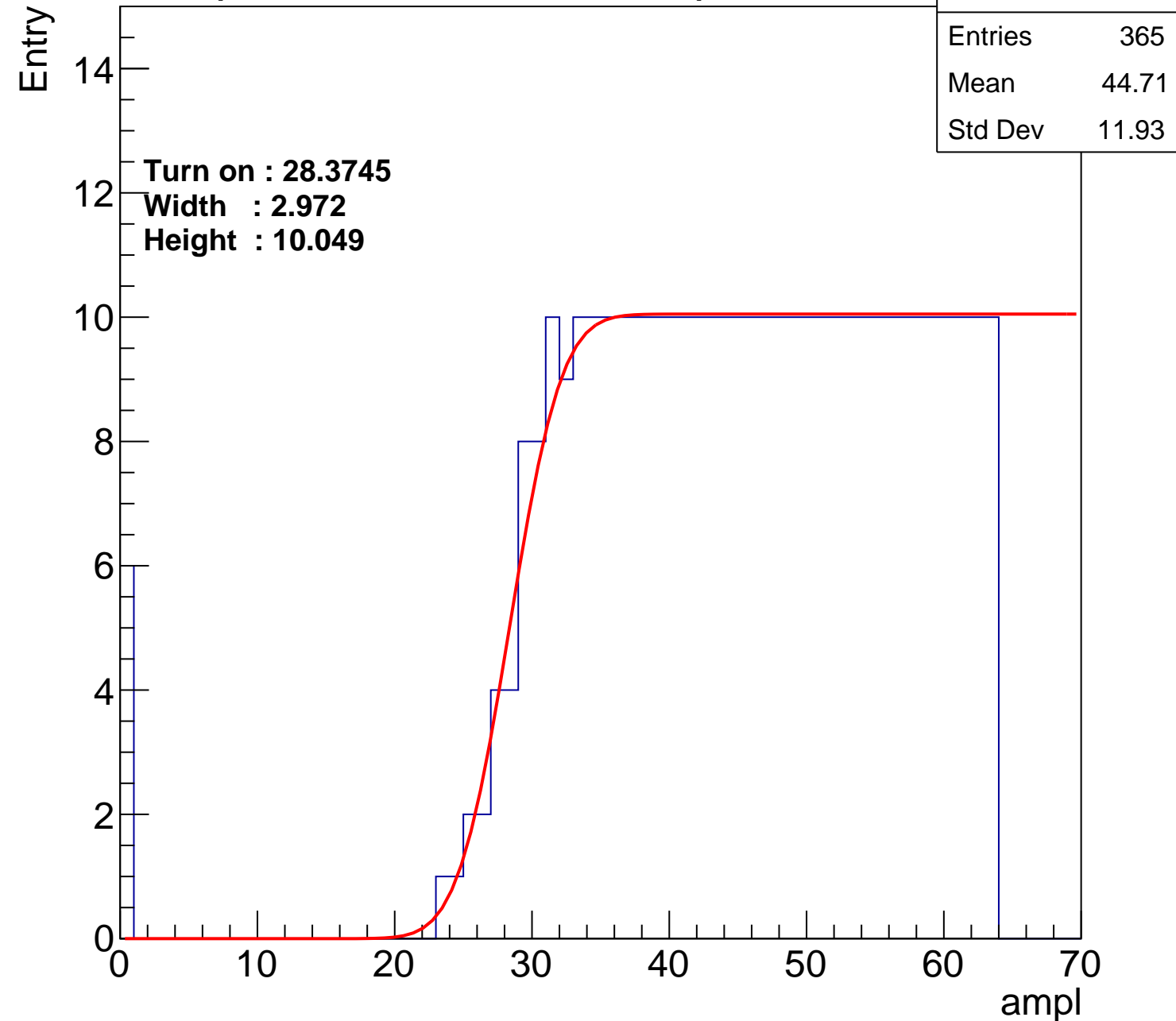
**Width : 2.972**

**Height : 10.049**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U9-ch114

calib\_packv5\_042523\_0143.root, FC#9, port A1

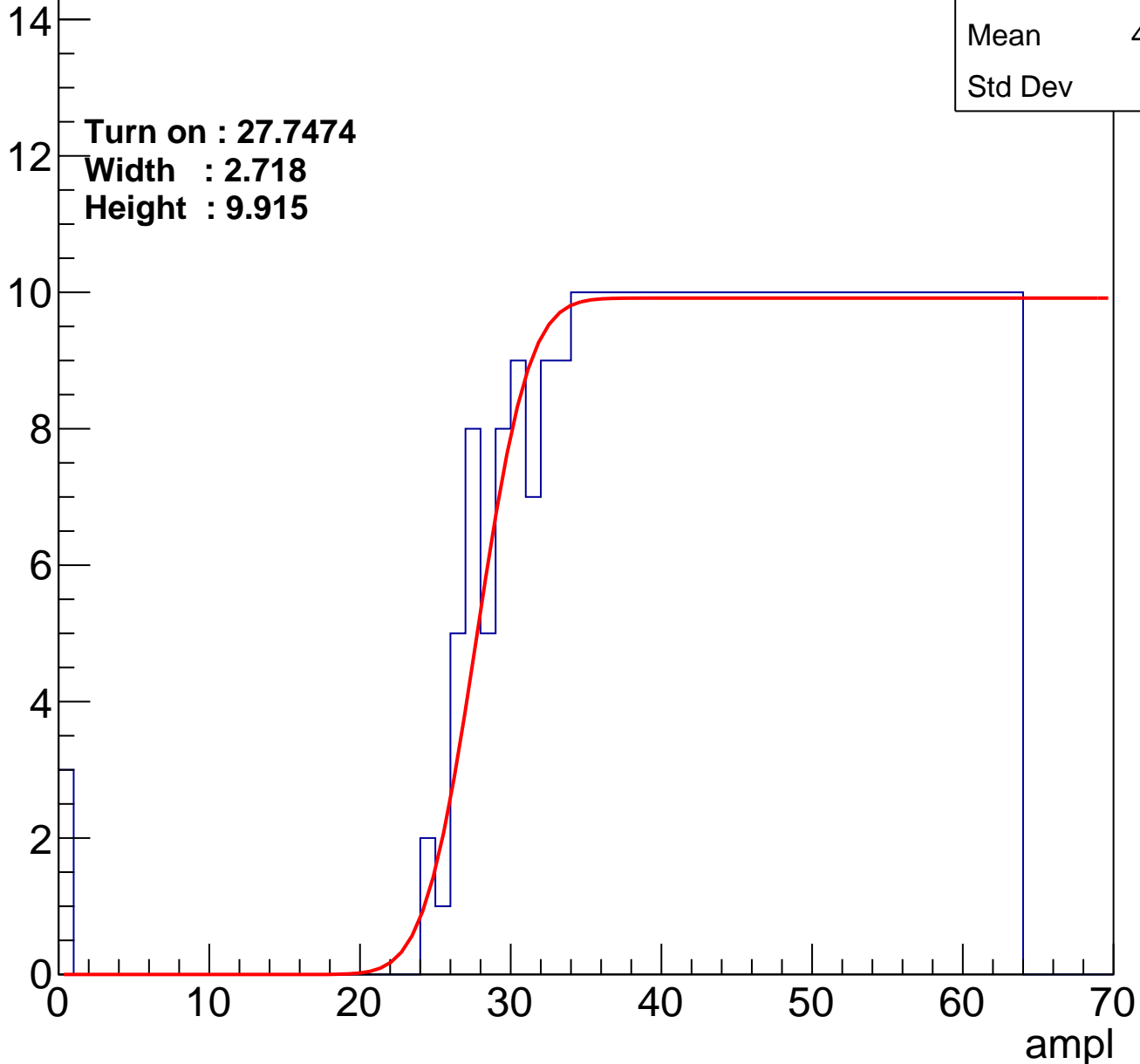
Entries	366
Mean	44.84
Std Dev	11.4

Turn on : 27.7474

Width : 2.718

Height : 9.915

Entry



# B0L001S, U9-ch115

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	359
Mean	44.96
Std Dev	11.76

**Turn on : 28.9627**

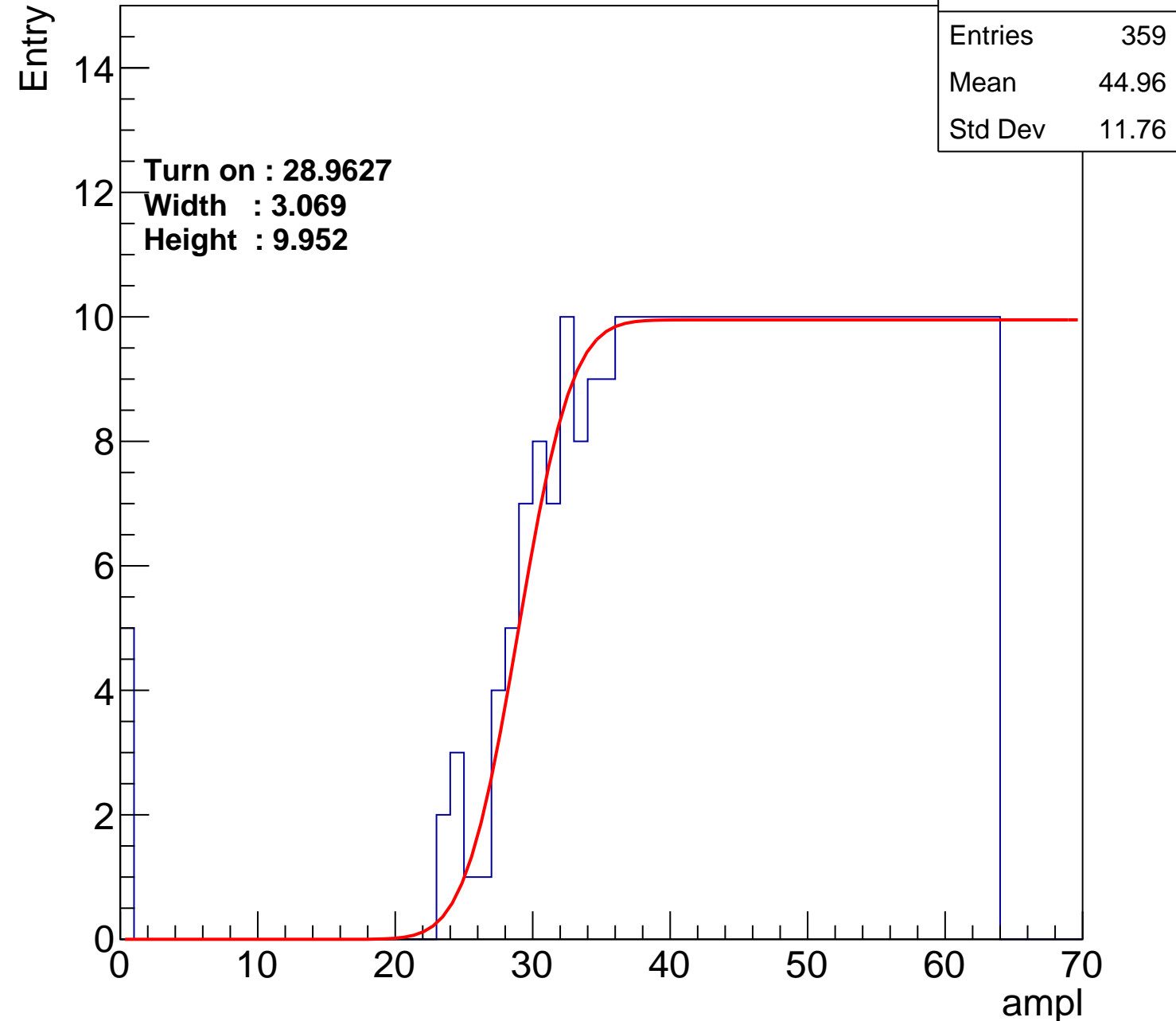
**Width : 3.069**

**Height : 9.952**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U9-ch116

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	357
Mean	45.22
Std Dev	11.4

Turn on : 29.0206

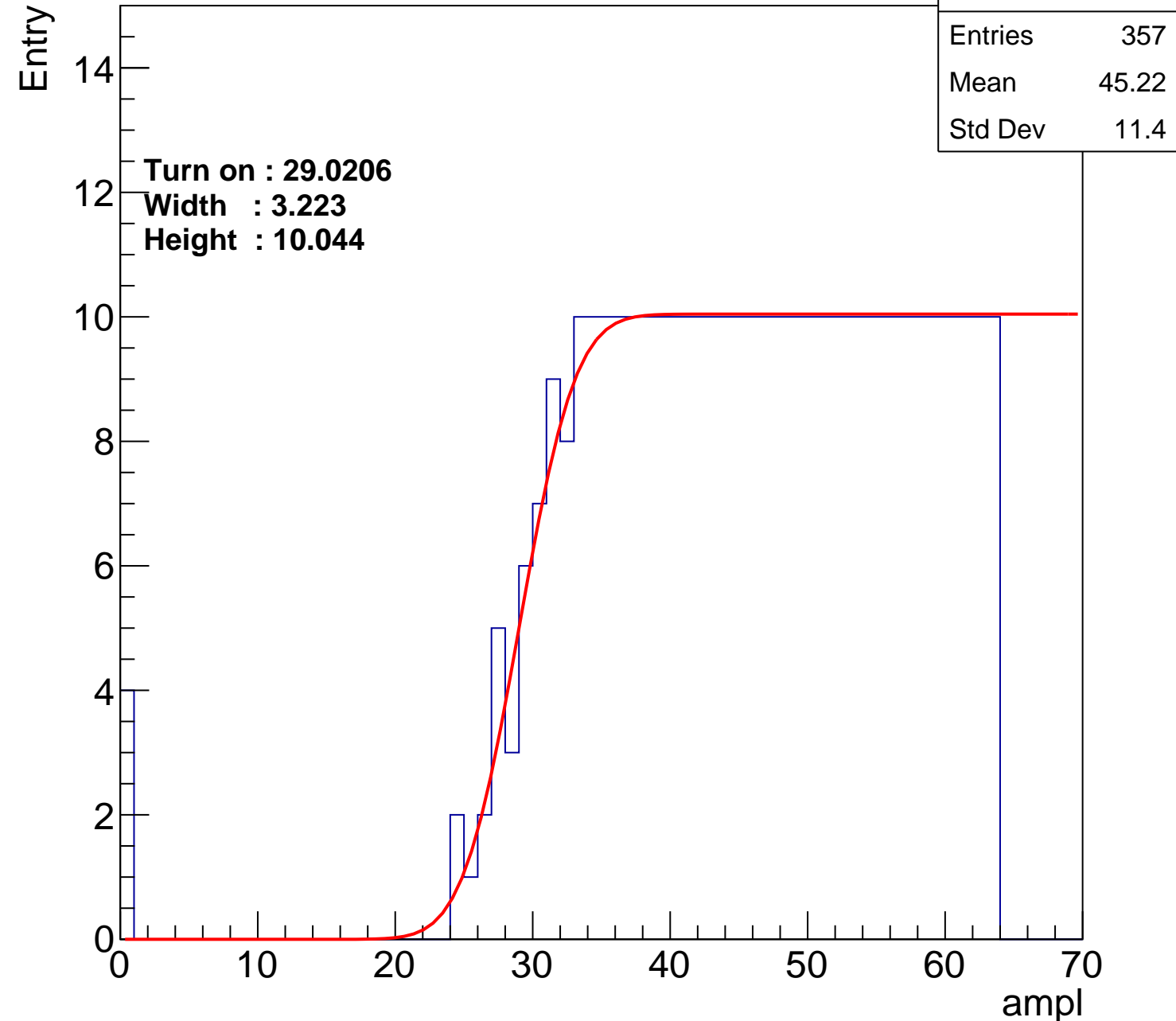
Width : 3.223

Height : 10.044

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U9-ch117

calib\_packv5\_042523\_0143.root, FC#9, port A1

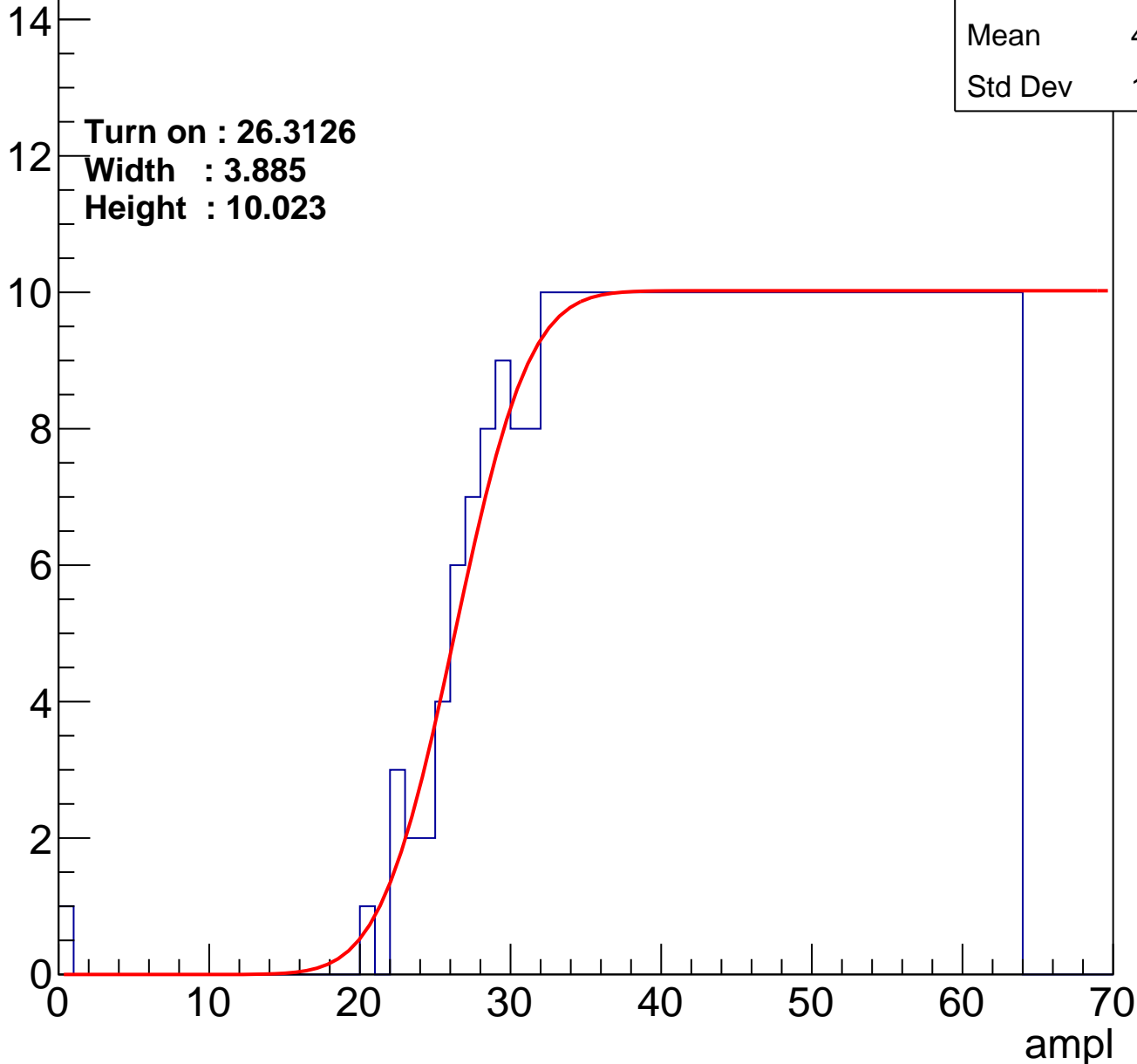
Entries	379
Mean	44.32
Std Dev	11.39

Turn on : 26.3126

Width : 3.885

Height : 10.023

Entry



# B0L001S, U9-ch118

calib\_packv5\_042523\_0143.root, FC#9, port A1

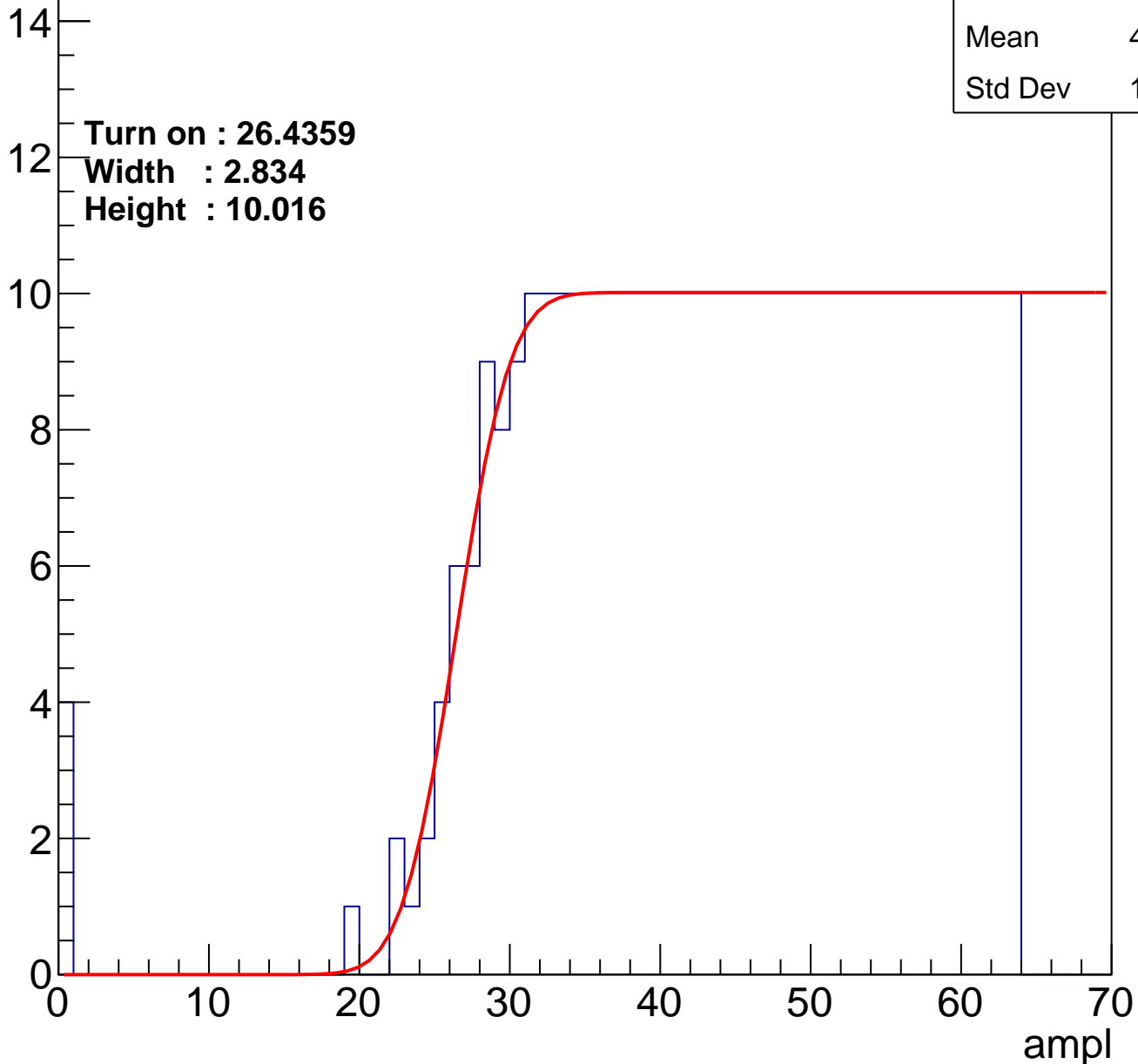
Entries	382
Mean	44.02
Std Dev	11.94

Turn on : 26.4359

Width : 2.834

Height : 10.016

Entry





# B0L001S, U9-ch119

calib\_packv5\_042523\_0143.root, FC#9, port A1

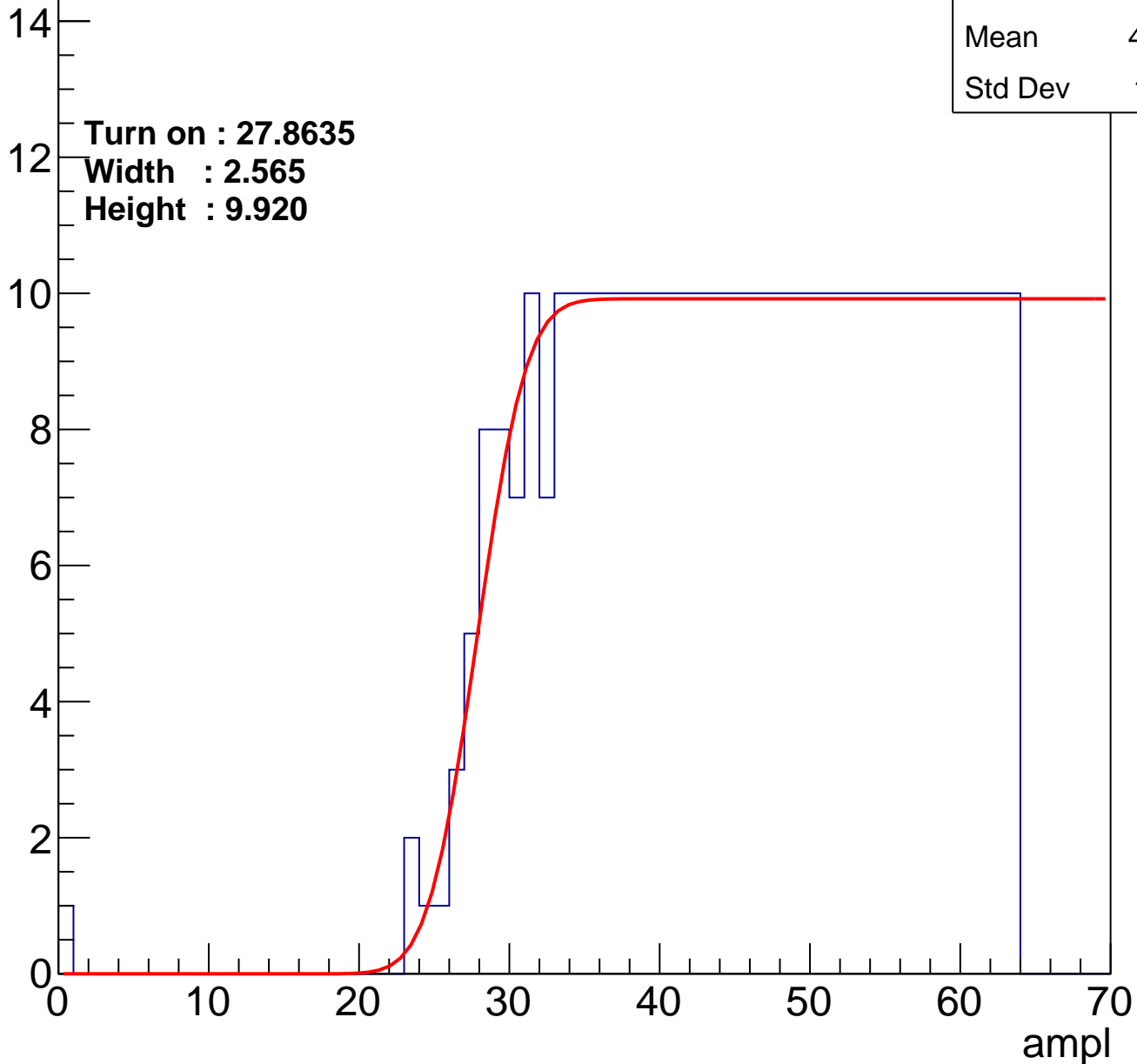
Entries	363
Mean	45.15
Std Dev	10.91

Turn on : 27.8635

Width : 2.565

Height : 9.920

Entry



# B0L001S, U9-ch120

calib\_packv5\_042523\_0143.root, FC#9, port A1

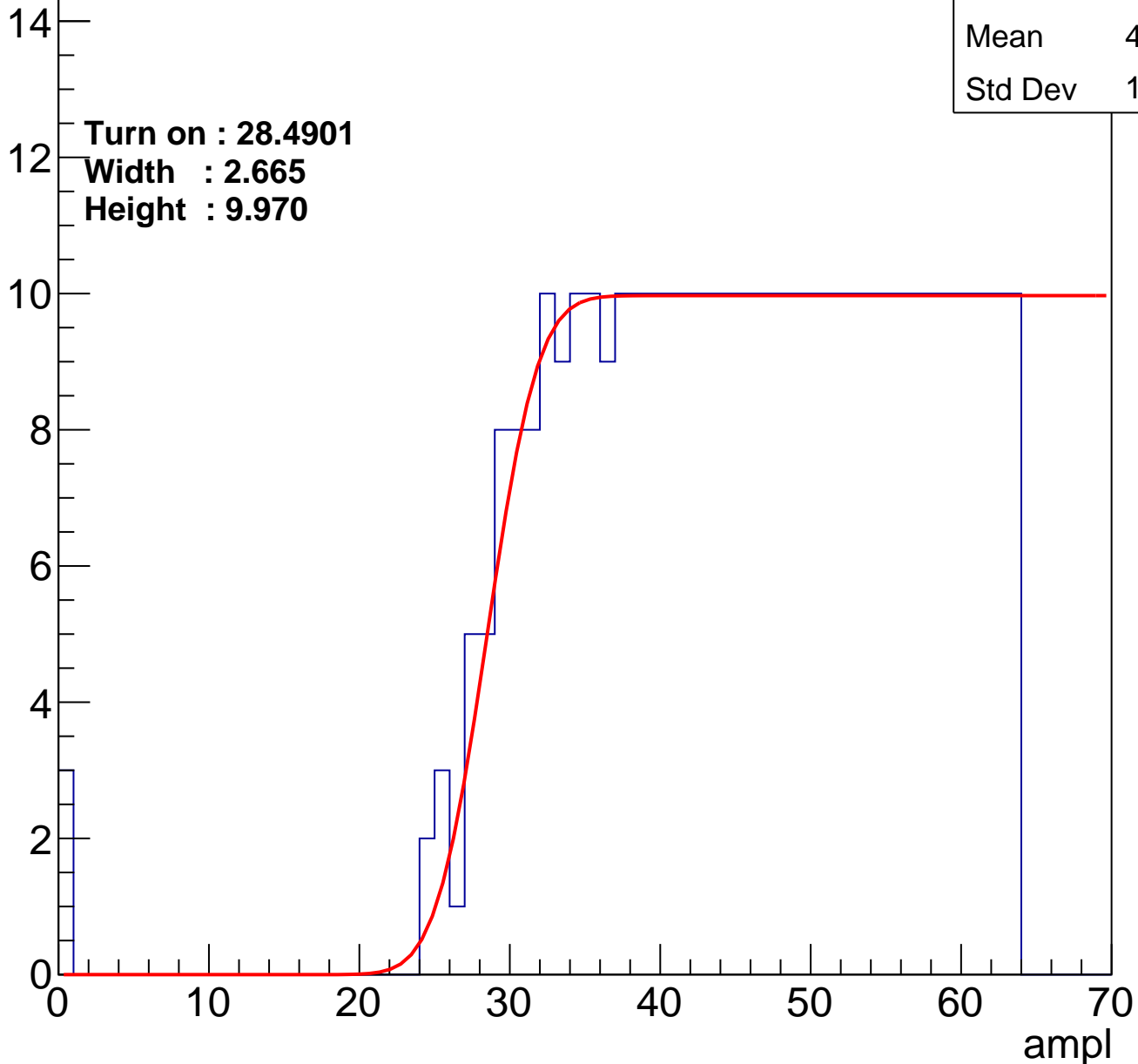
Entries	361
Mean	45.08
Std Dev	11.29

Turn on : 28.4901

Width : 2.665

Height : 9.970

Entry



# B0L001S, U9-ch121

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	345
Mean	45.73
Std Dev	11.24

Turn on : 30.6646

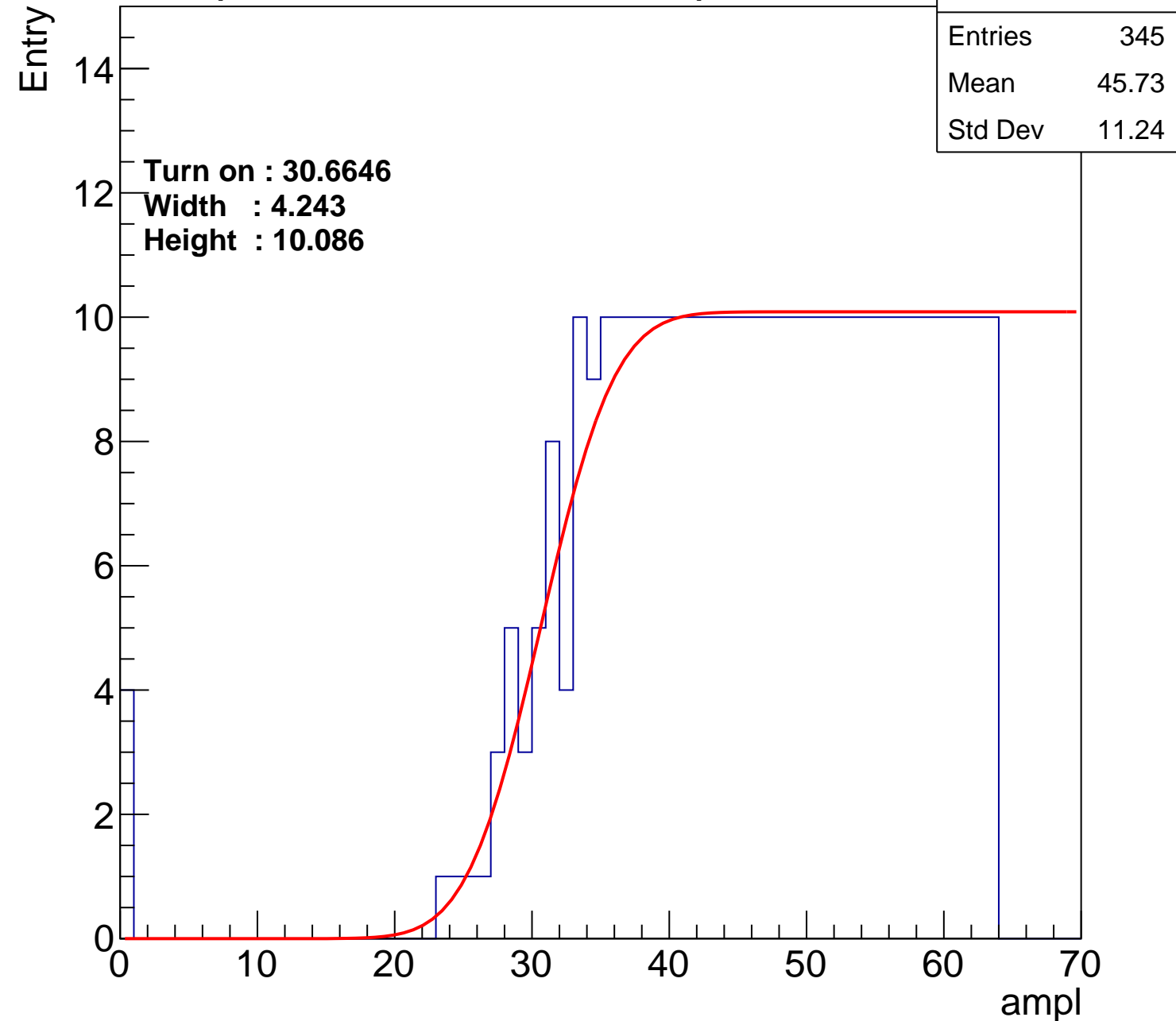
Width : 4.243

Height : 10.086

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U9-ch122

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	371
Mean	44.49
Std Dev	11.86

Turn on : 27.6586

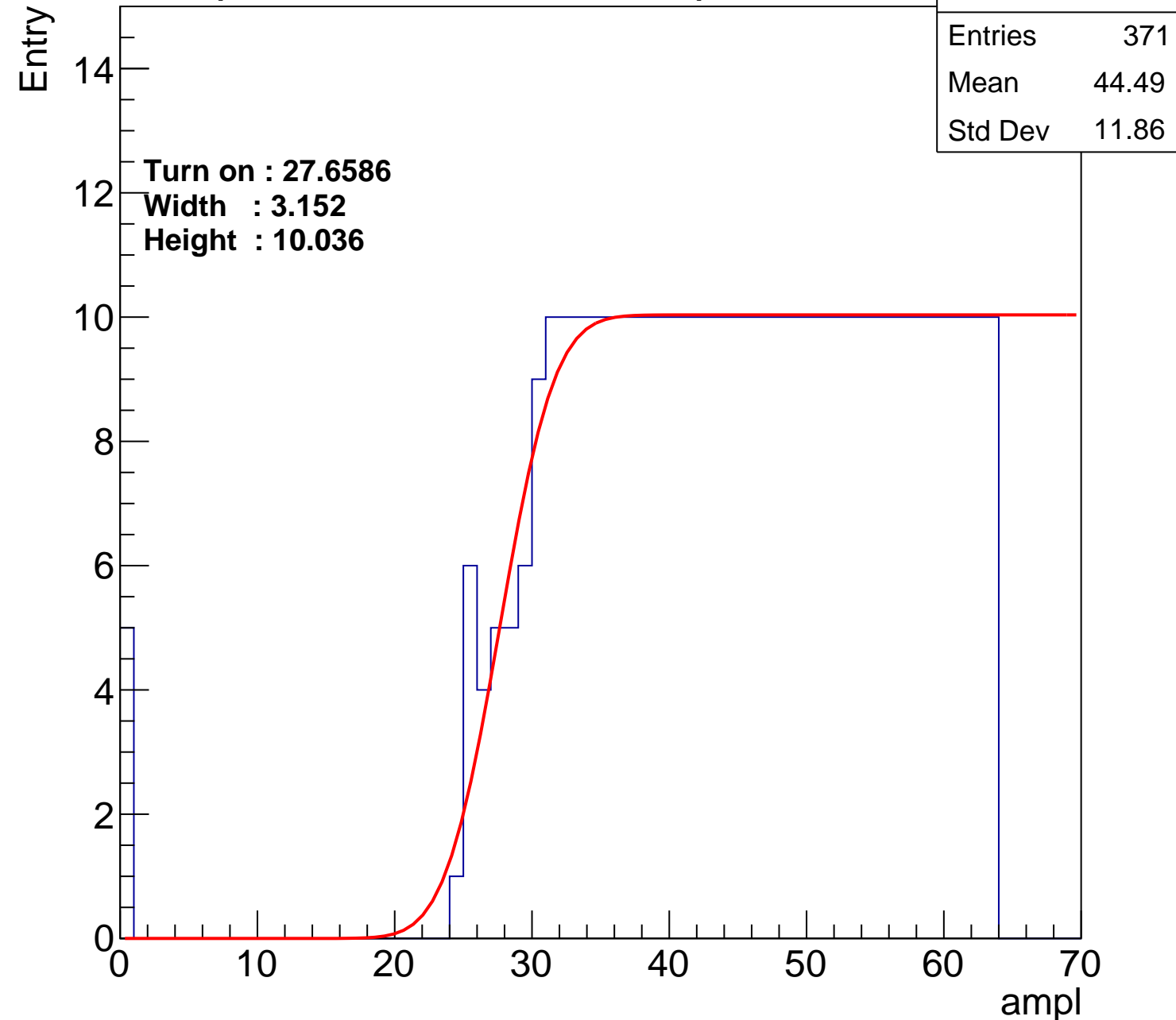
Width : 3.152

Height : 10.036

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U9-ch123

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	348
Mean	45.68
Std Dev	11.06

**Turn on : 29.7517**

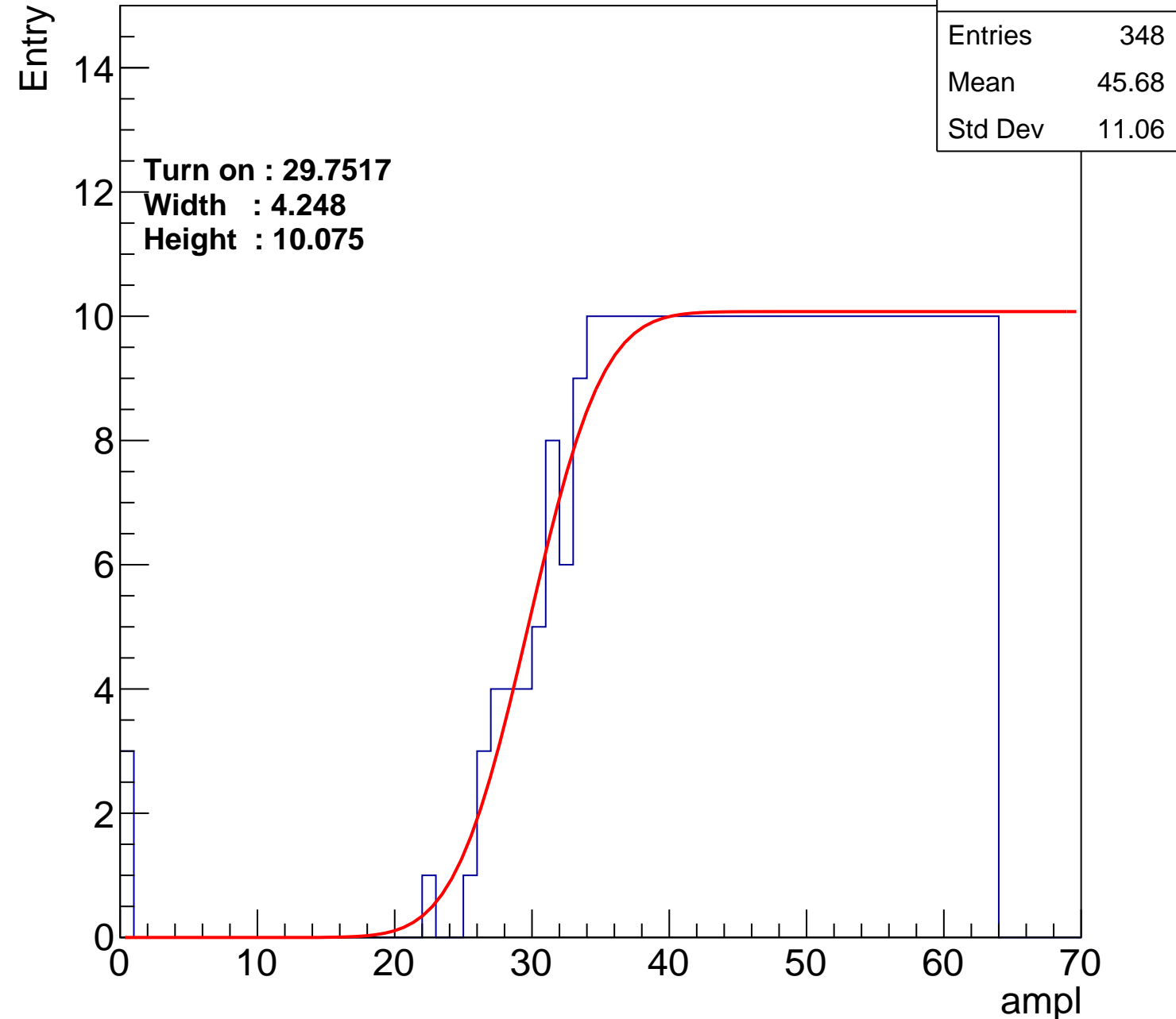
**Width : 4.248**

**Height : 10.075**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U9-ch124

calib\_packv5\_042523\_0143.root, FC#9, port A1

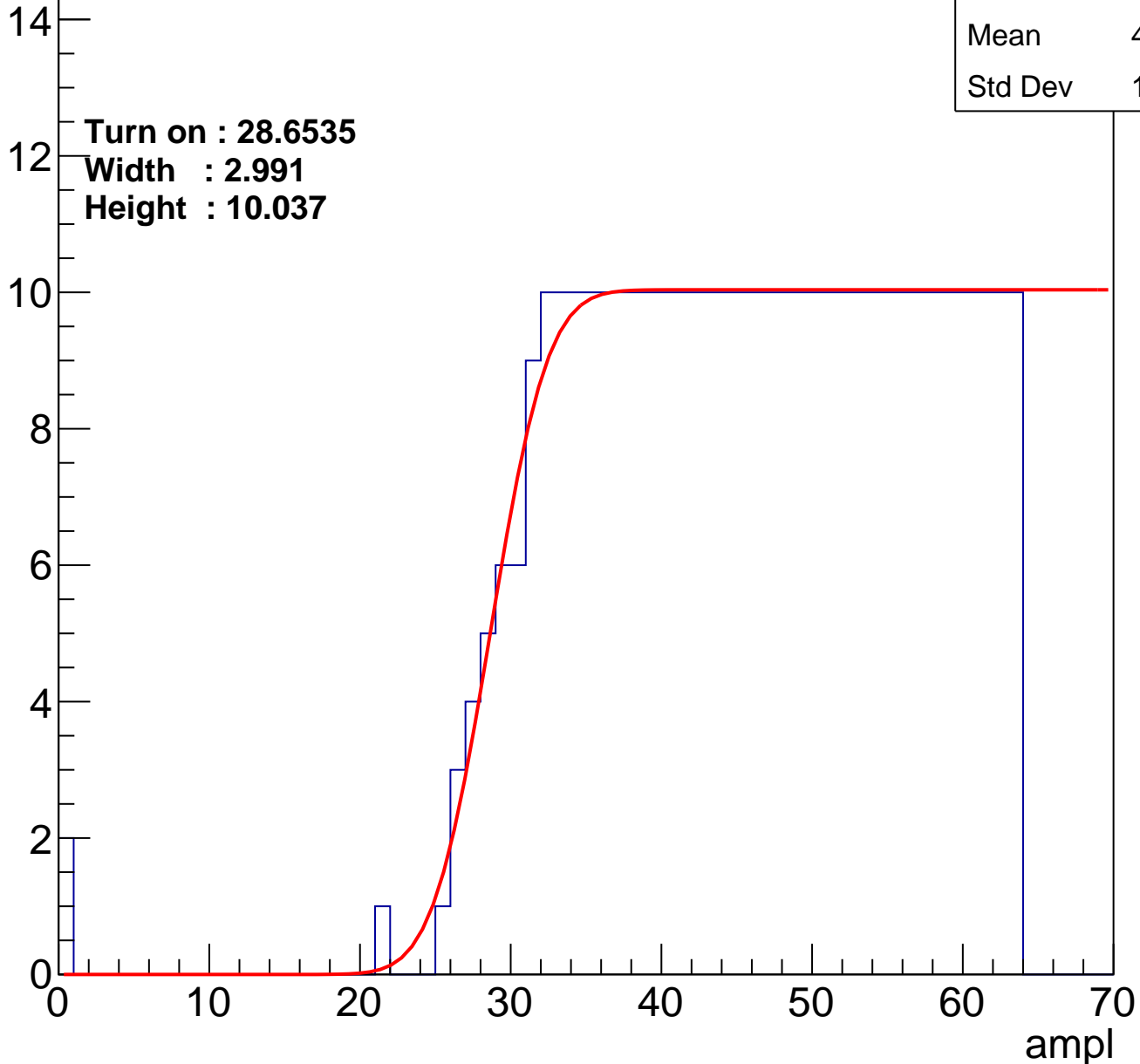
Entries	357
Mean	45.39
Std Dev	10.94

**Turn on : 28.6535**

**Width : 2.991**

**Height : 10.037**

Entry



# B0L001S, U9-ch125

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	344
Mean	46.01
Std Dev	10.65

**Turn on : 29.9844**

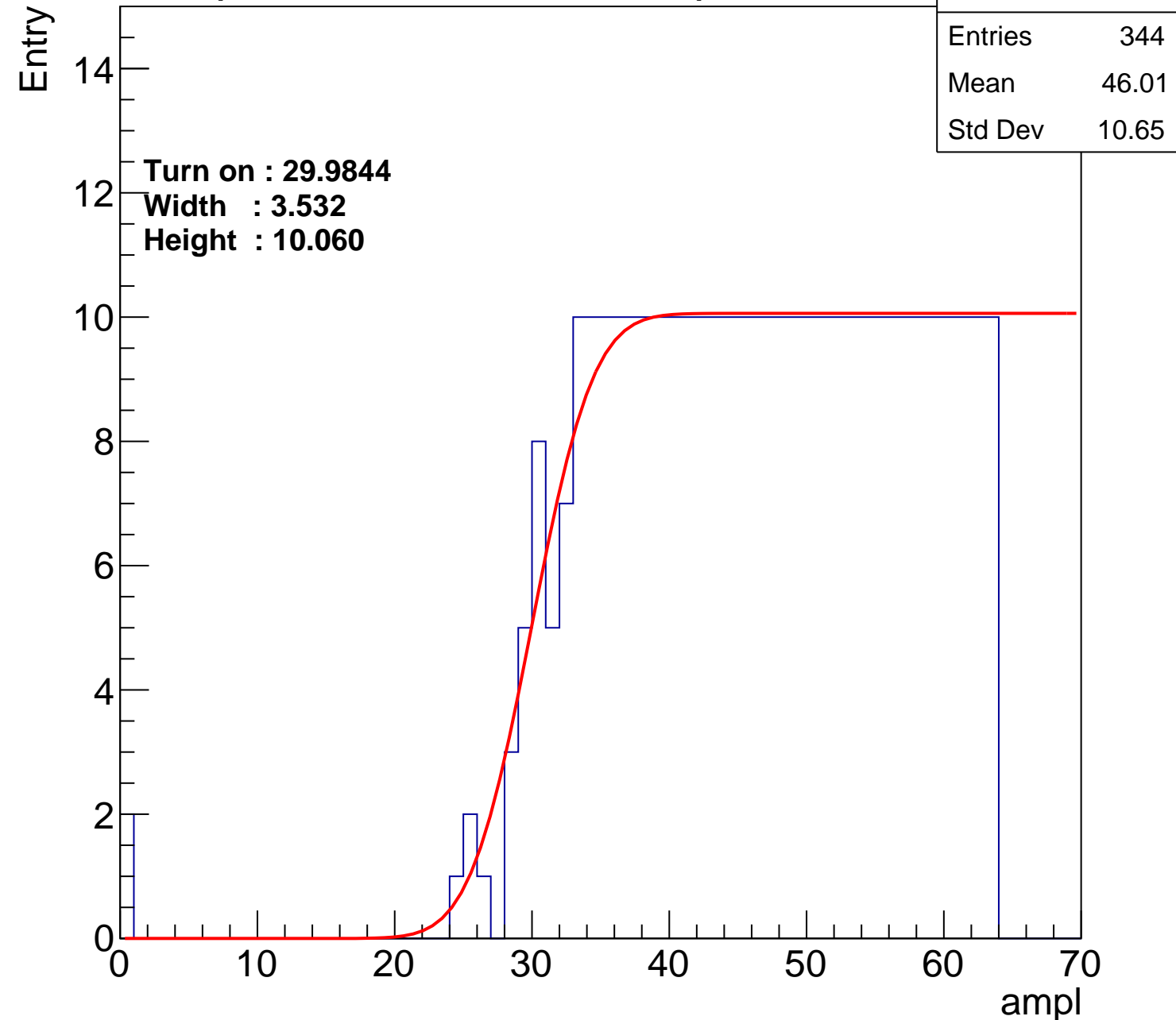
**Width : 3.532**

**Height : 10.060**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U9-ch126

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	350
Mean	45.59
Std Dev	11.1

Turn on : 29.8666

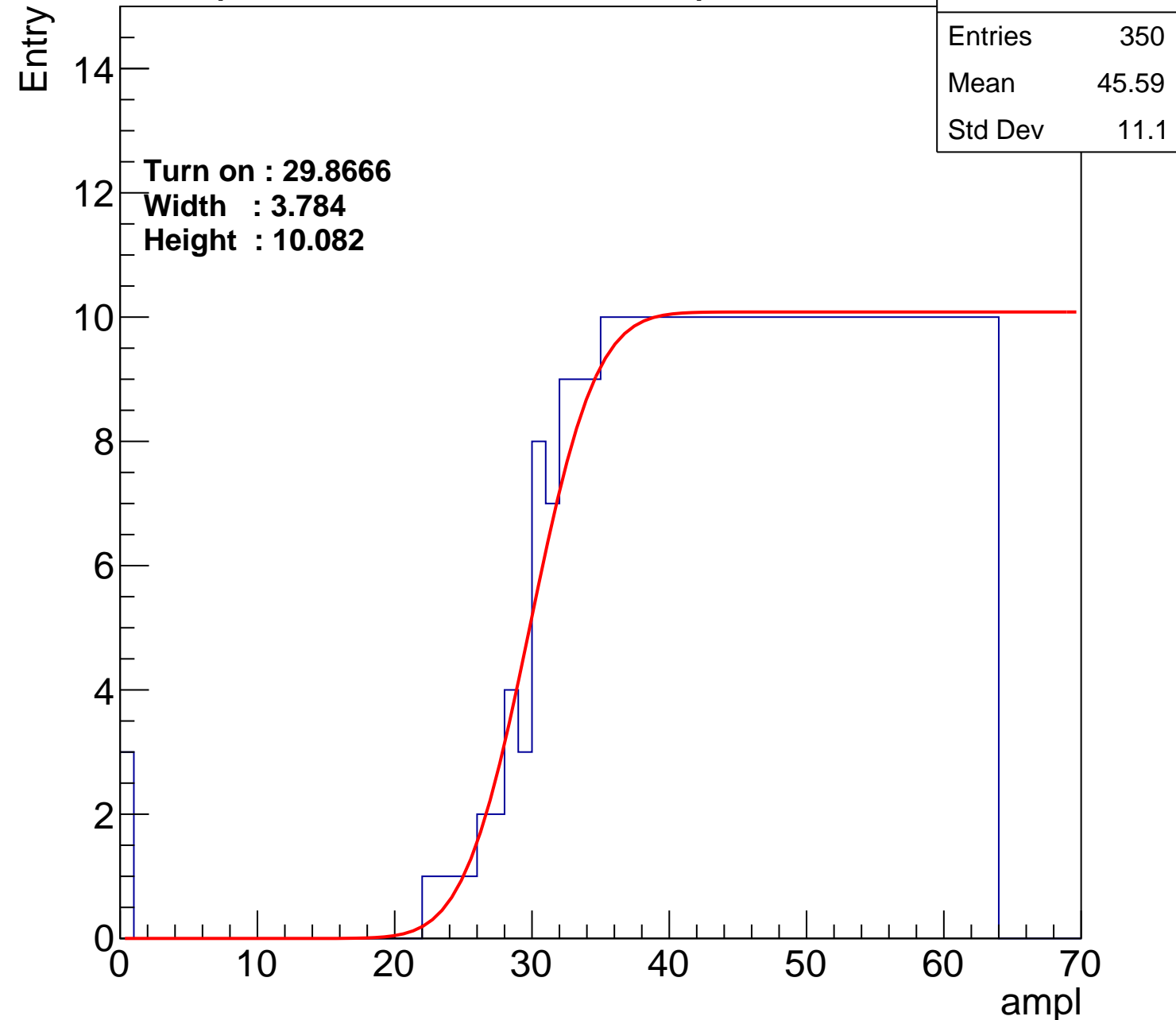
Width : 3.784

Height : 10.082

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B0L001S, U9-ch127

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	383
Mean	44.12
Std Dev	11.59

Turn on : 26.2418

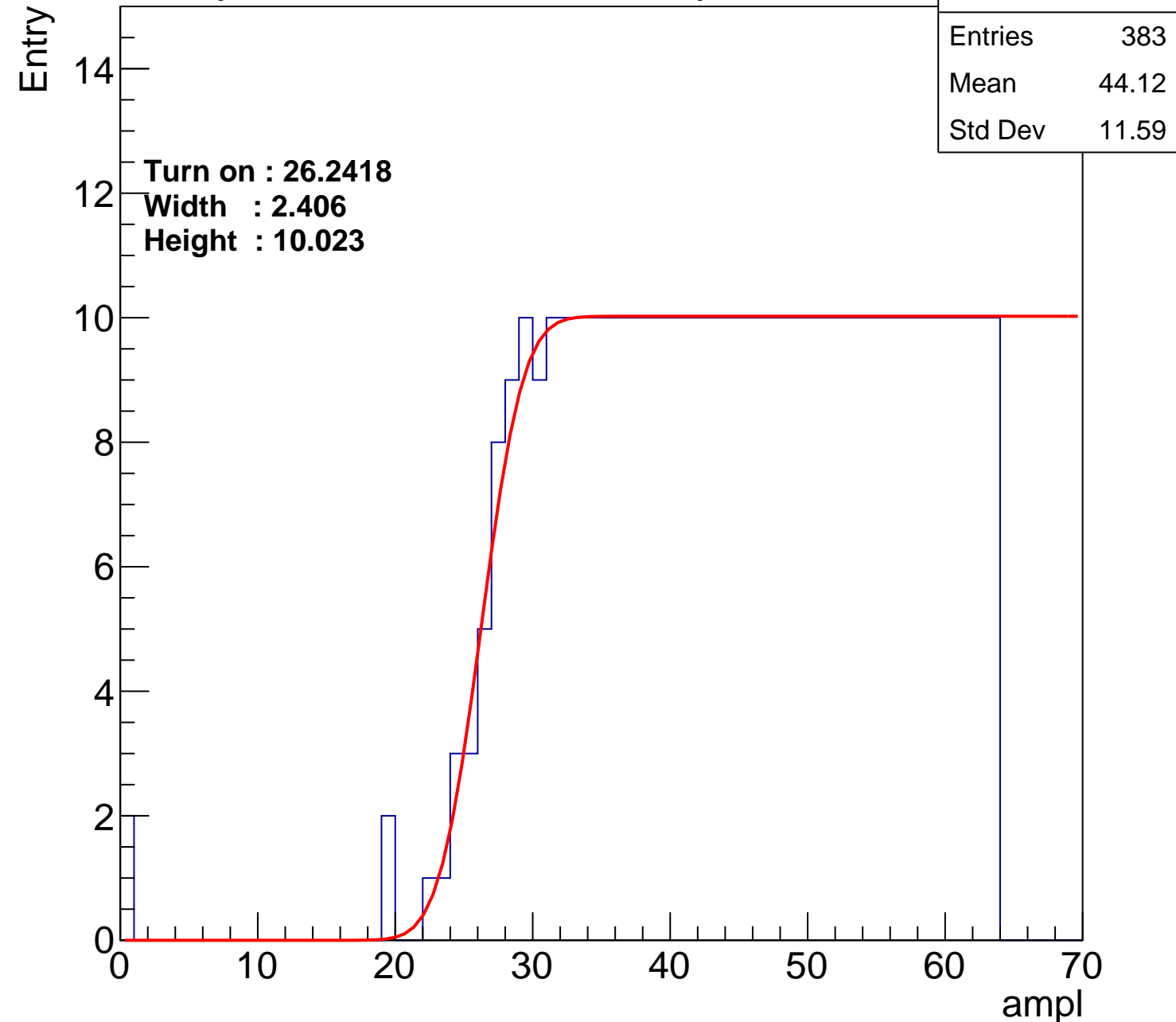
Width : 2.406

Height : 10.023

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U9-ch127

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	383
Mean	44.12
Std Dev	11.59

Turn on : 26.2418

Width : 2.406

Height : 10.023

Entry

