



# B1L104S, U3-ch0

calib\_packv5\_033123\_0516.root, FC#4, port A1

Entries	240
Mean	30.32
Std Dev	28.2

Turn on : 51.2219

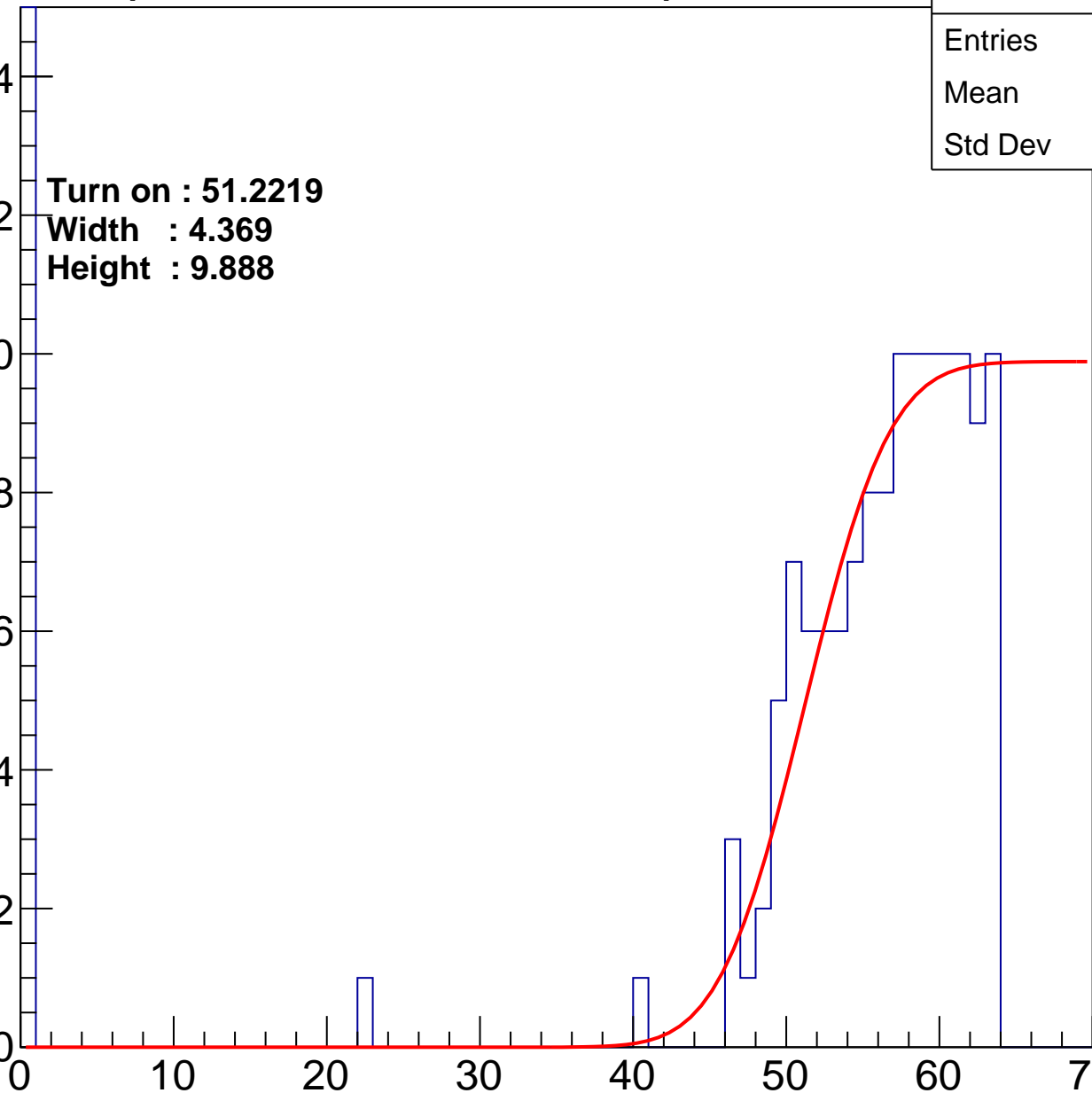
Width : 4.369

Height : 9.888

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L104S, U3-ch1

calib\_packv5\_033123\_0516.root, FC#4, port A1

Entries	198
Mean	31.77
Std Dev	28.84

**Turn on : 53.0999**

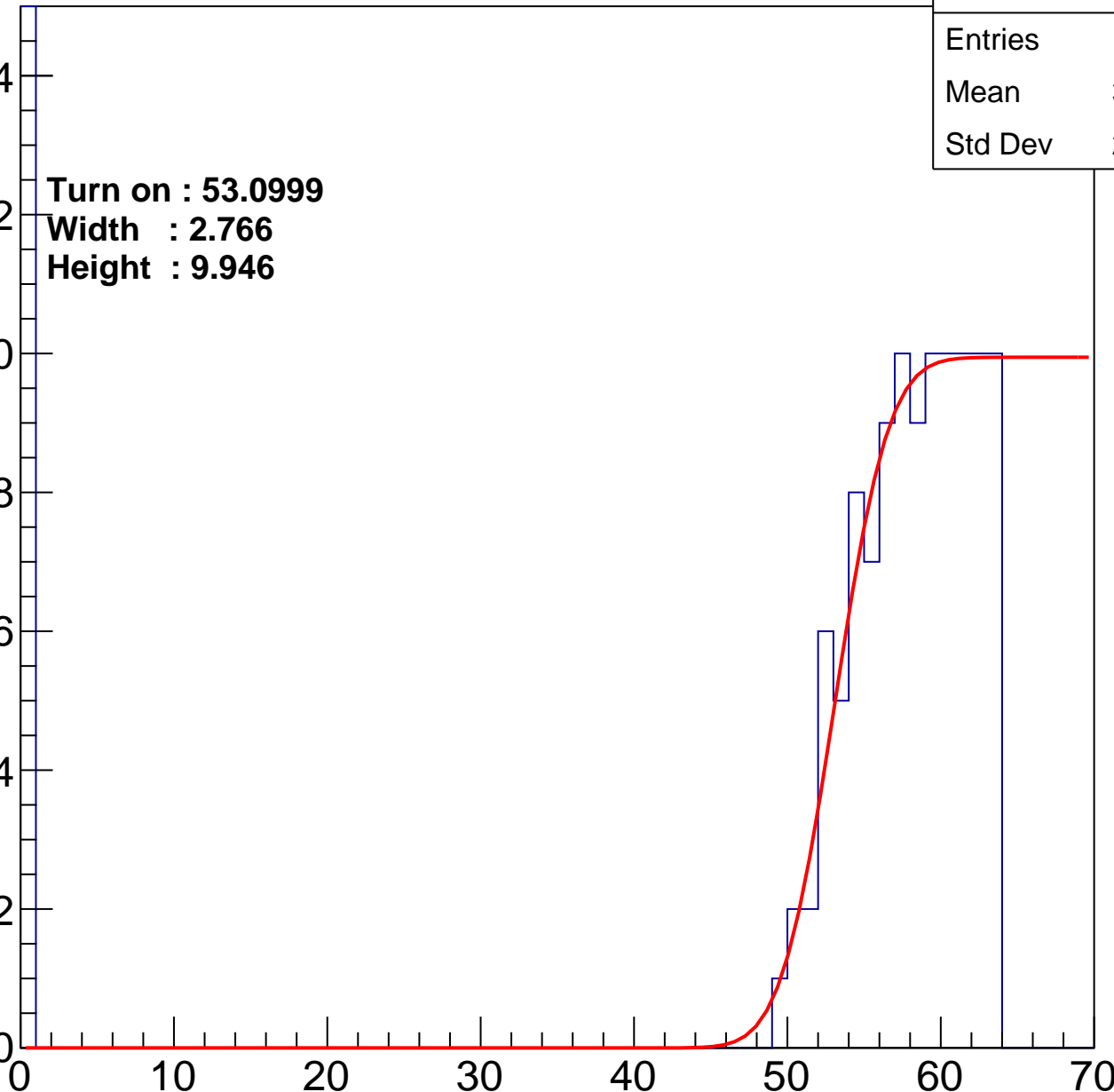
**Width : 2.766**

**Height : 9.946**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L104S, U3-ch2

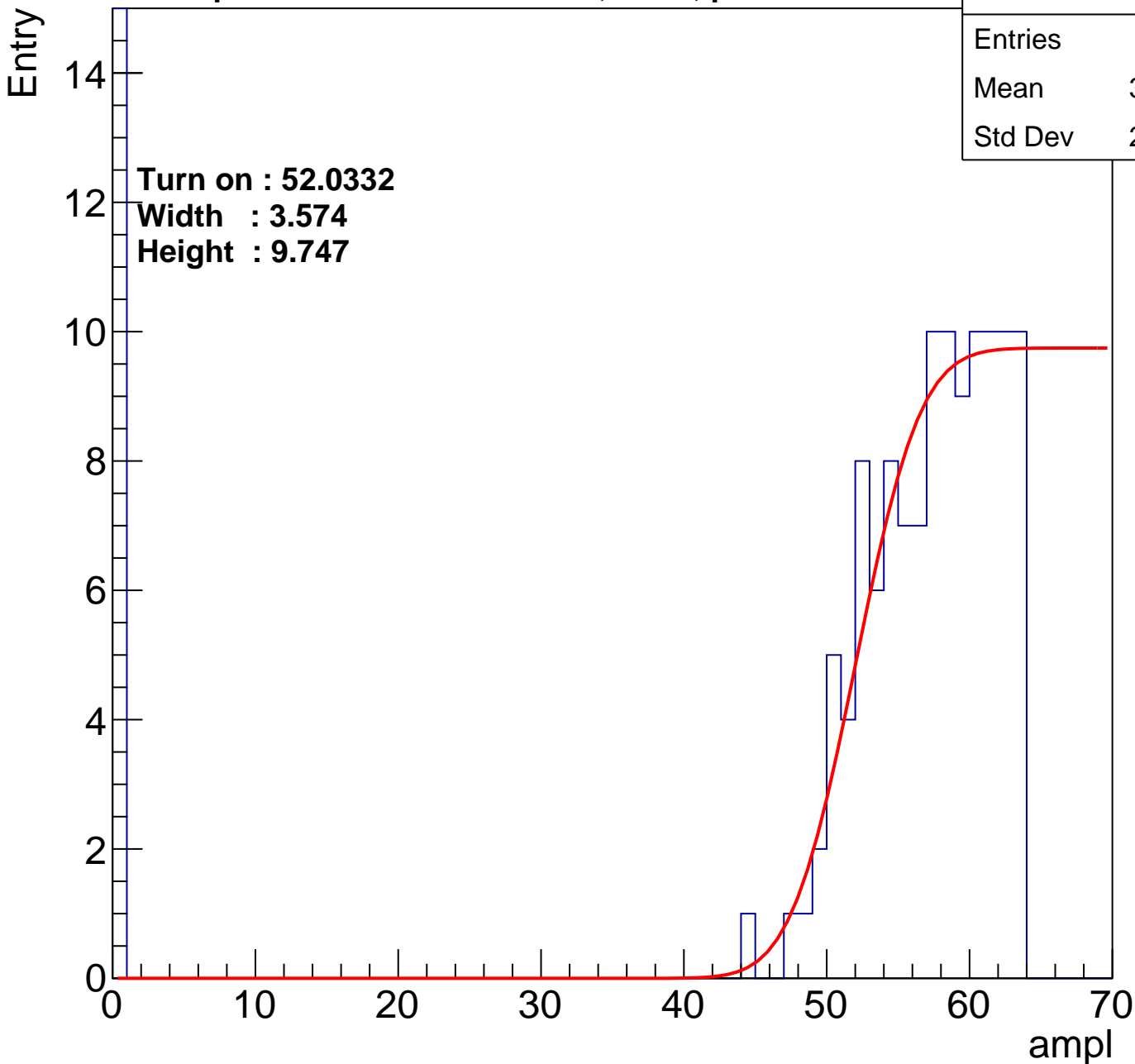
calib\_packv5\_033123\_0516.root, FC#4, port A1

Entries	219
Mean	30.94
Std Dev	28.53

Turn on : 52.0332

Width : 3.574

Height : 9.747



# B1L104S, U3-ch3

calib\_packv5\_033123\_0516.root, FC#4, port A1

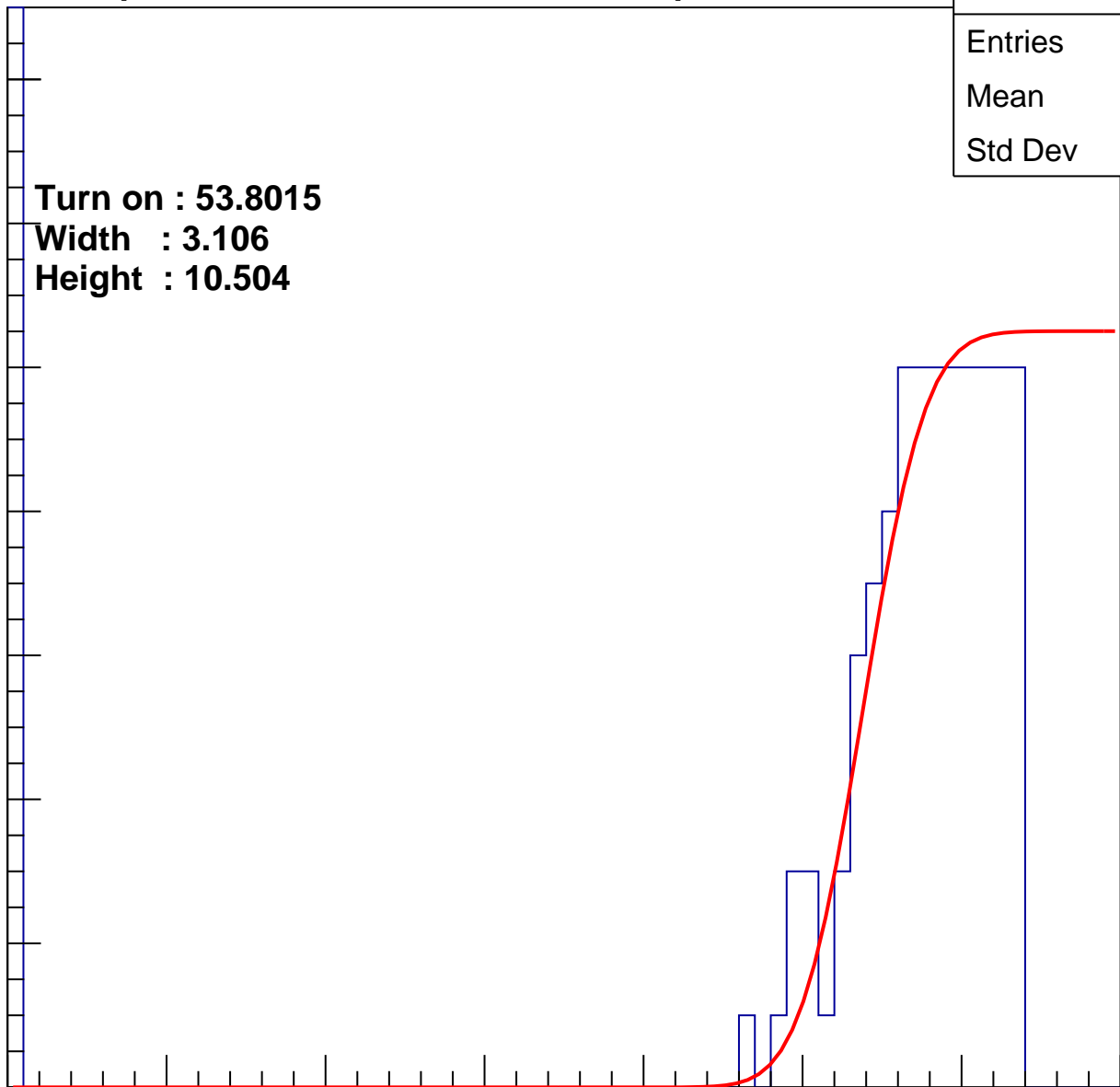
Entry

14  
12  
10  
8  
6  
4  
2  
0

Turn on : 53.8015  
Width : 3.106  
Height : 10.504

Entries	213
Mean	30.49
Std Dev	28.82

ampl



# B1L104S, U3-ch4

calib\_packv5\_033123\_0516.root, FC#4, port A1

Entries	208
Mean	32.31
Std Dev	28.41

**Turn on : 53.9017**

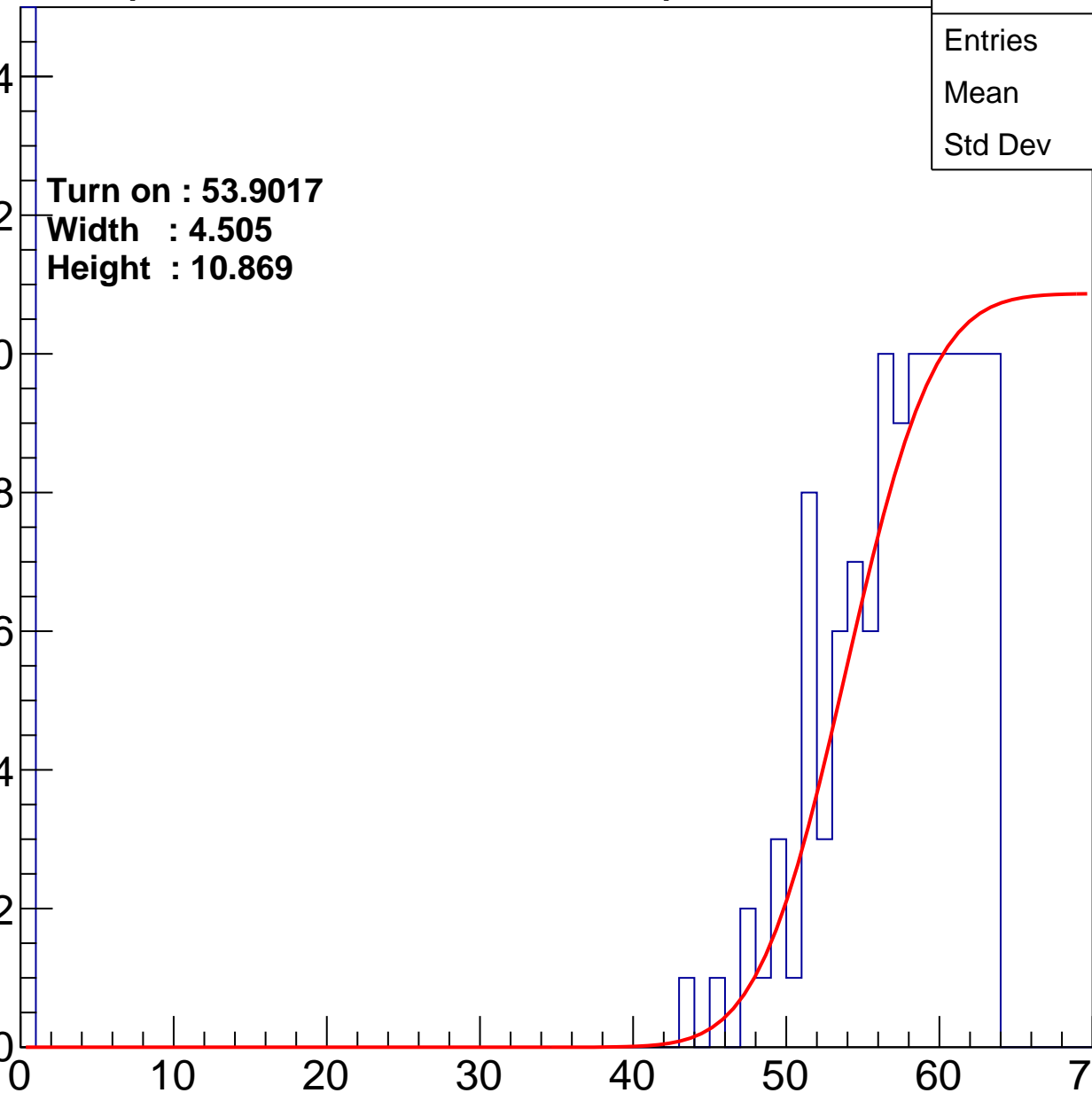
**Width : 4.505**

**Height : 10.869**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L104S, U3-ch5

calib\_packv5\_033123\_0516.root, FC#4, port A1

Entries	194
Mean	33.71
Std Dev	28.39

Turn on : 52.9331

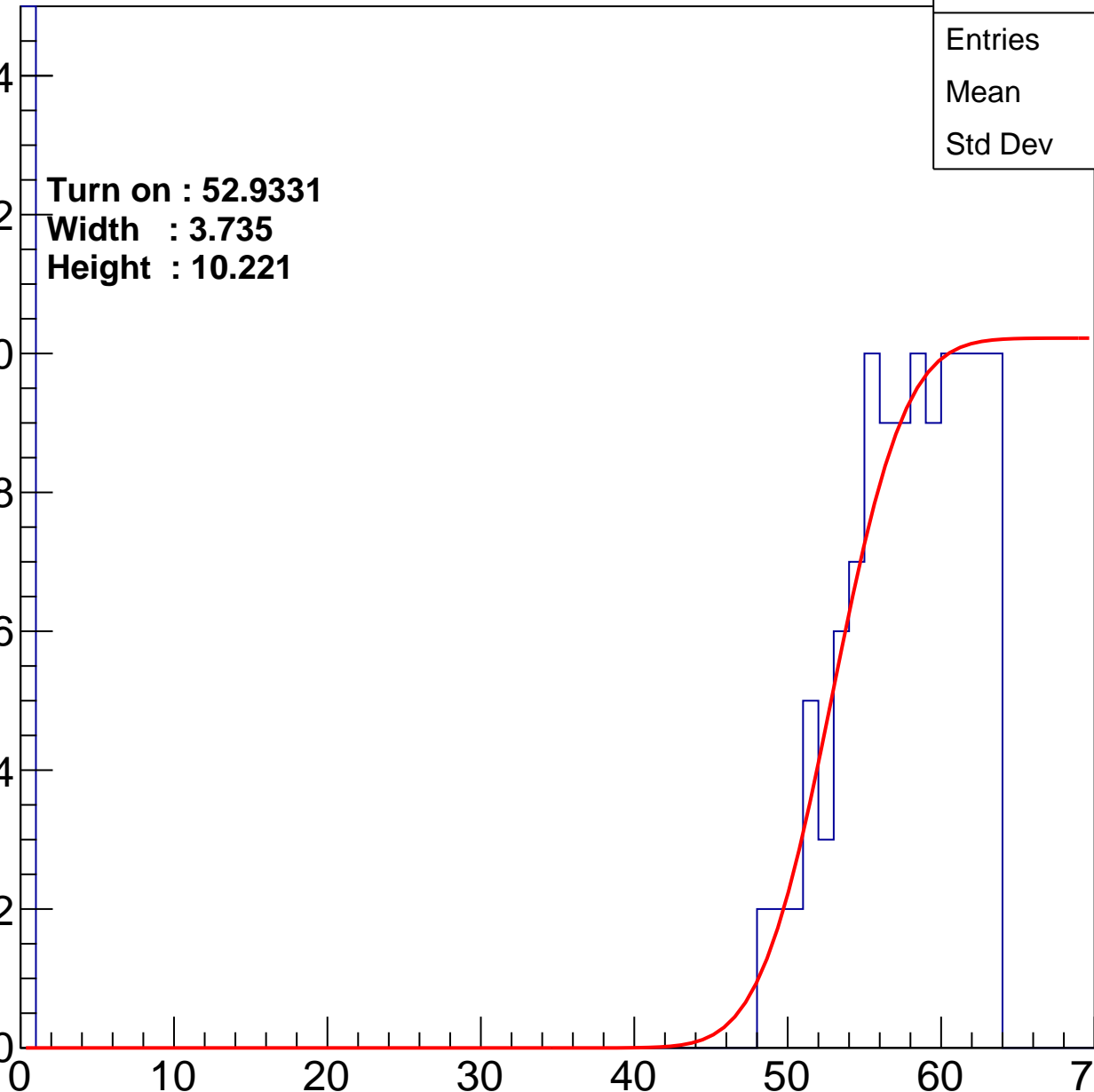
Width : 3.735

Height : 10.221

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L104S, U3-ch6

calib\_packv5\_033123\_0516.root, FC#4, port A1

Entries	207
Mean	36.2
Std Dev	27.25

**Turn on : 50.3785**

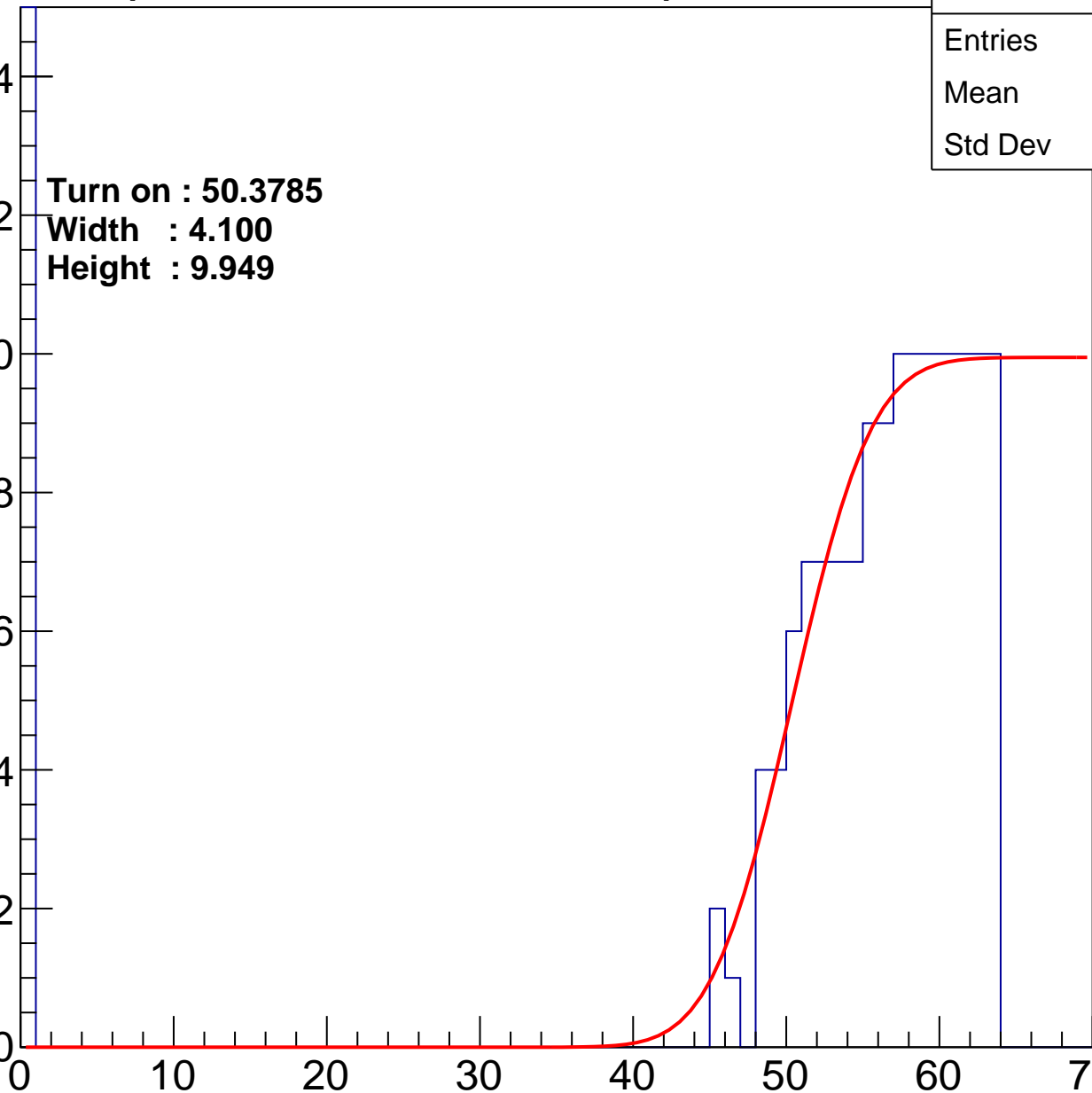
**Width : 4.100**

**Height : 9.949**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L104S, U3-ch7

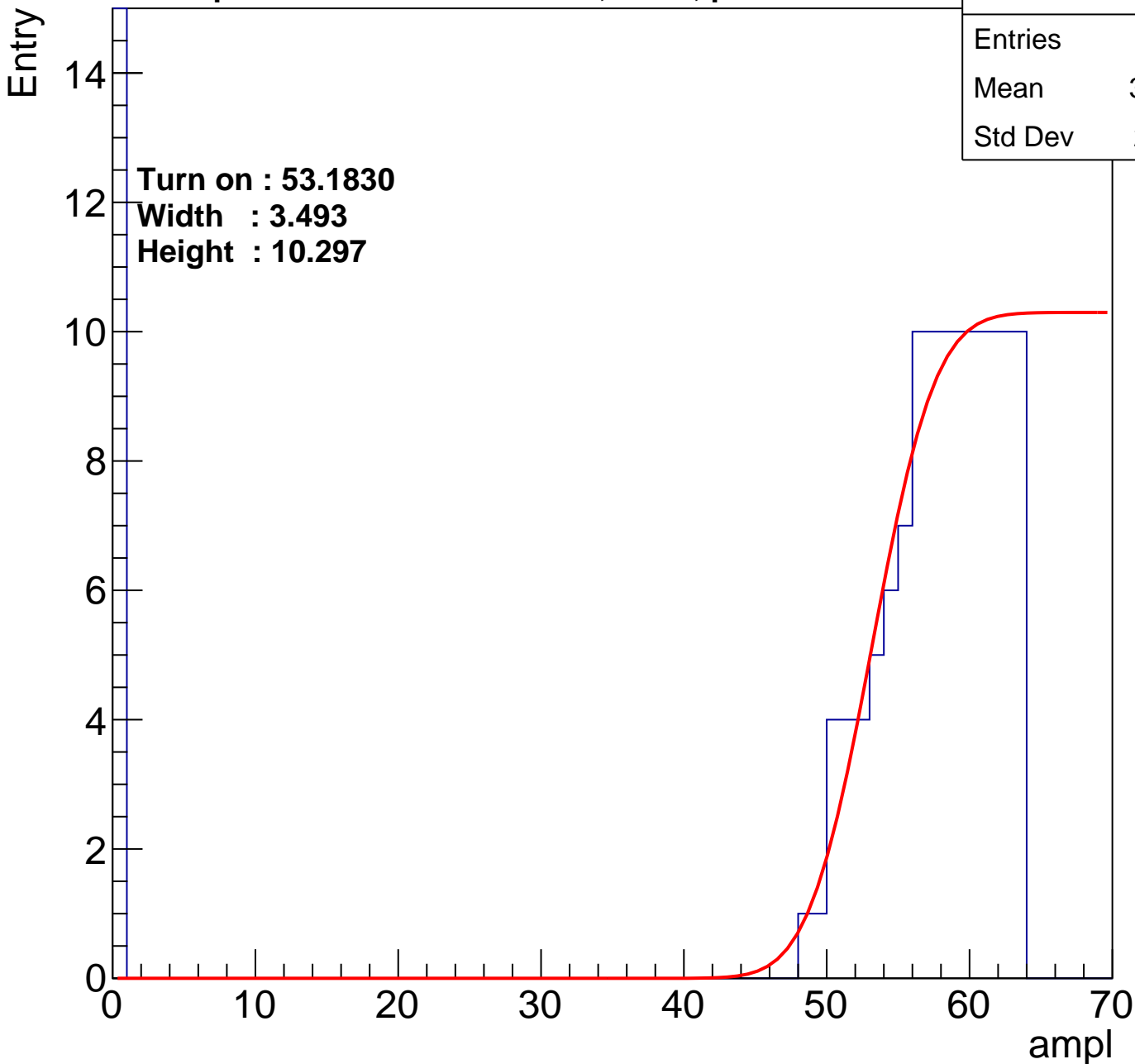
calib\_packv5\_033123\_0516.root, FC#4, port A1

Entries	186
Mean	34.64
Std Dev	28.31

Turn on : 53.1830

Width : 3.493

Height : 10.297



# B1L104S, U3-ch8

calib\_packv5\_033123\_0516.root, FC#4, port A1

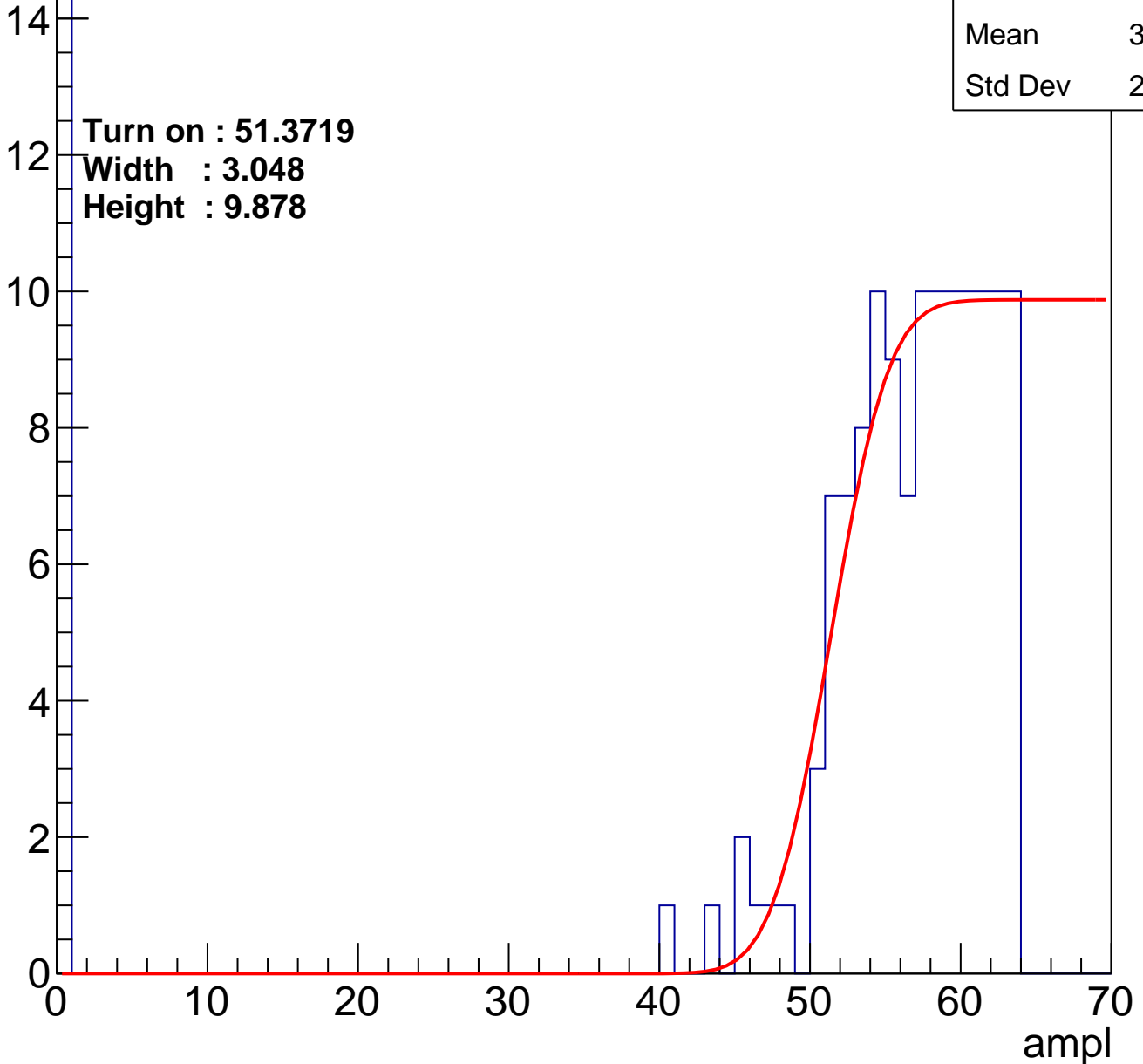
Entry

Entries	215
Mean	33.66
Std Dev	27.98

Turn on : 51.3719

Width : 3.048

Height : 9.878



# B1L104S, U3-ch9

calib\_packv5\_033123\_0516.root, FC#4, port A1

Entries	242
Mean	27.64
Std Dev	28.71

**Turn on : 52.6512**

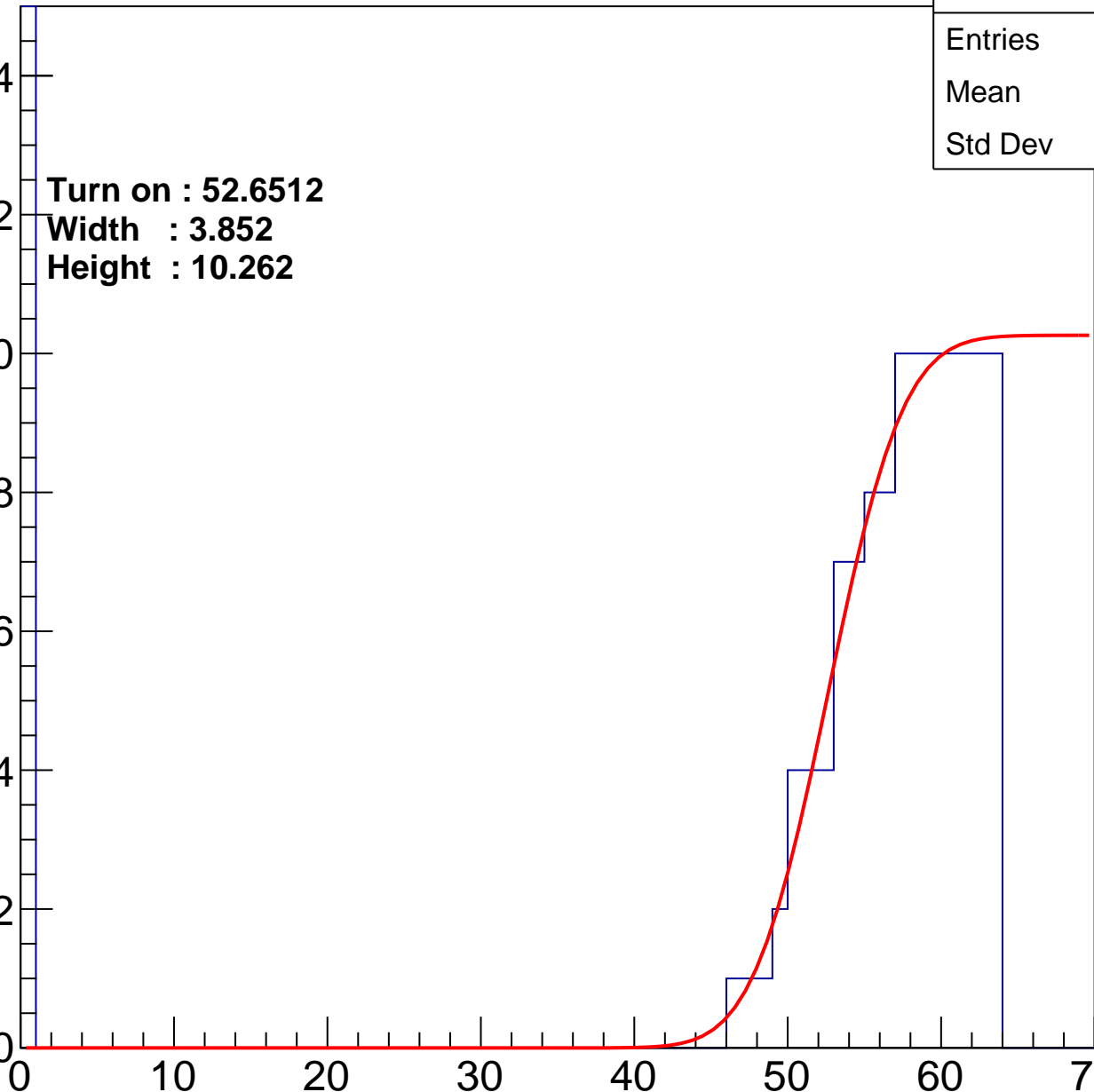
**Width : 3.852**

**Height : 10.262**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L104S, U3-ch10

calib\_packv5\_033123\_0516.root, FC#4, port A1

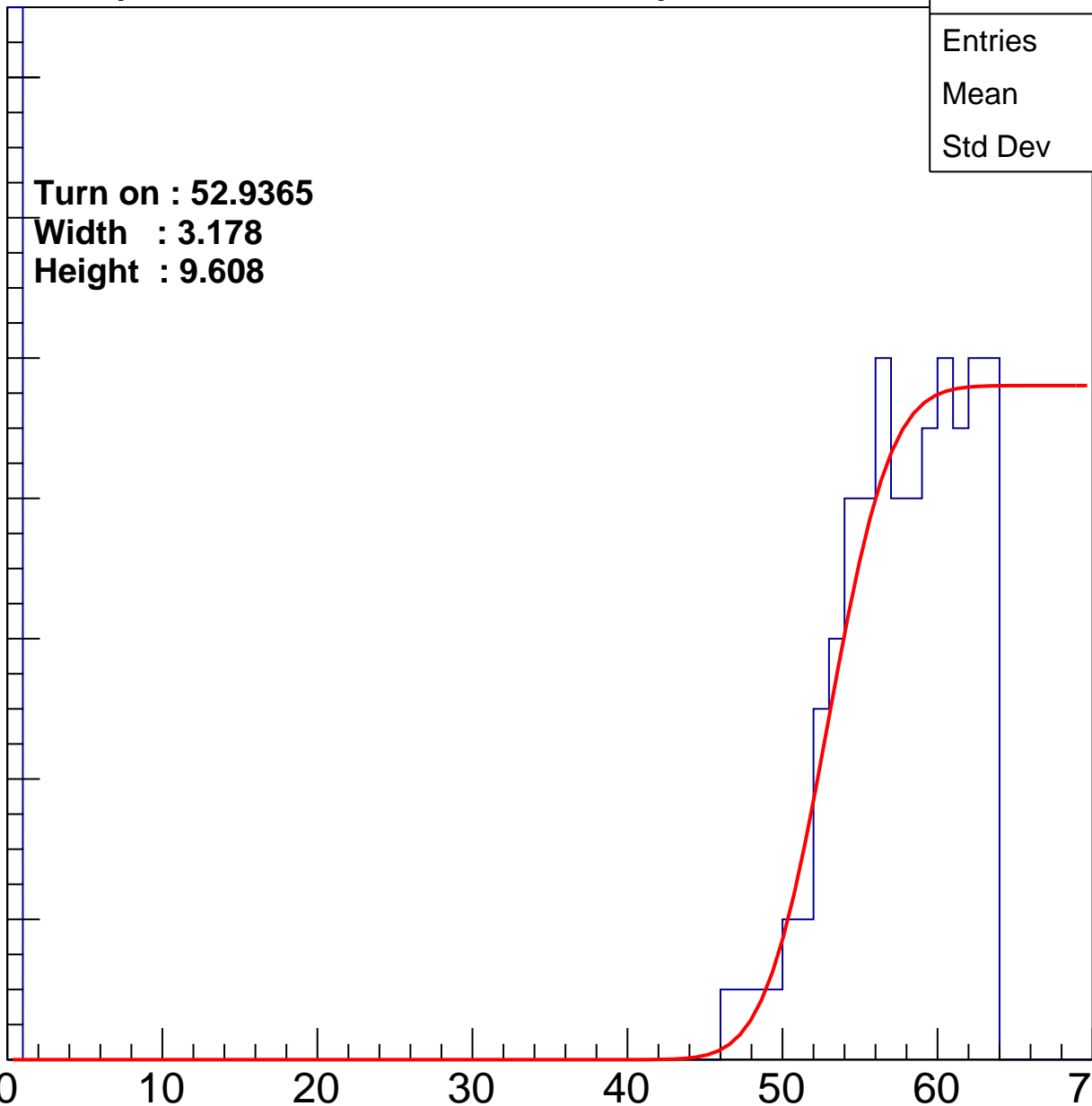
Entry

14  
12  
10  
8  
6  
4  
2  
0

Turn on : 52.9365  
Width : 3.178  
Height : 9.608

Entries	189
Mean	33.08
Std Dev	28.5

ampl



# B1L104S, U3-ch11

calib\_packv5\_033123\_0516.root, FC#4, port A1

Entries	191
Mean	32.33
Std Dev	28.78

**Turn on : 53.4253**

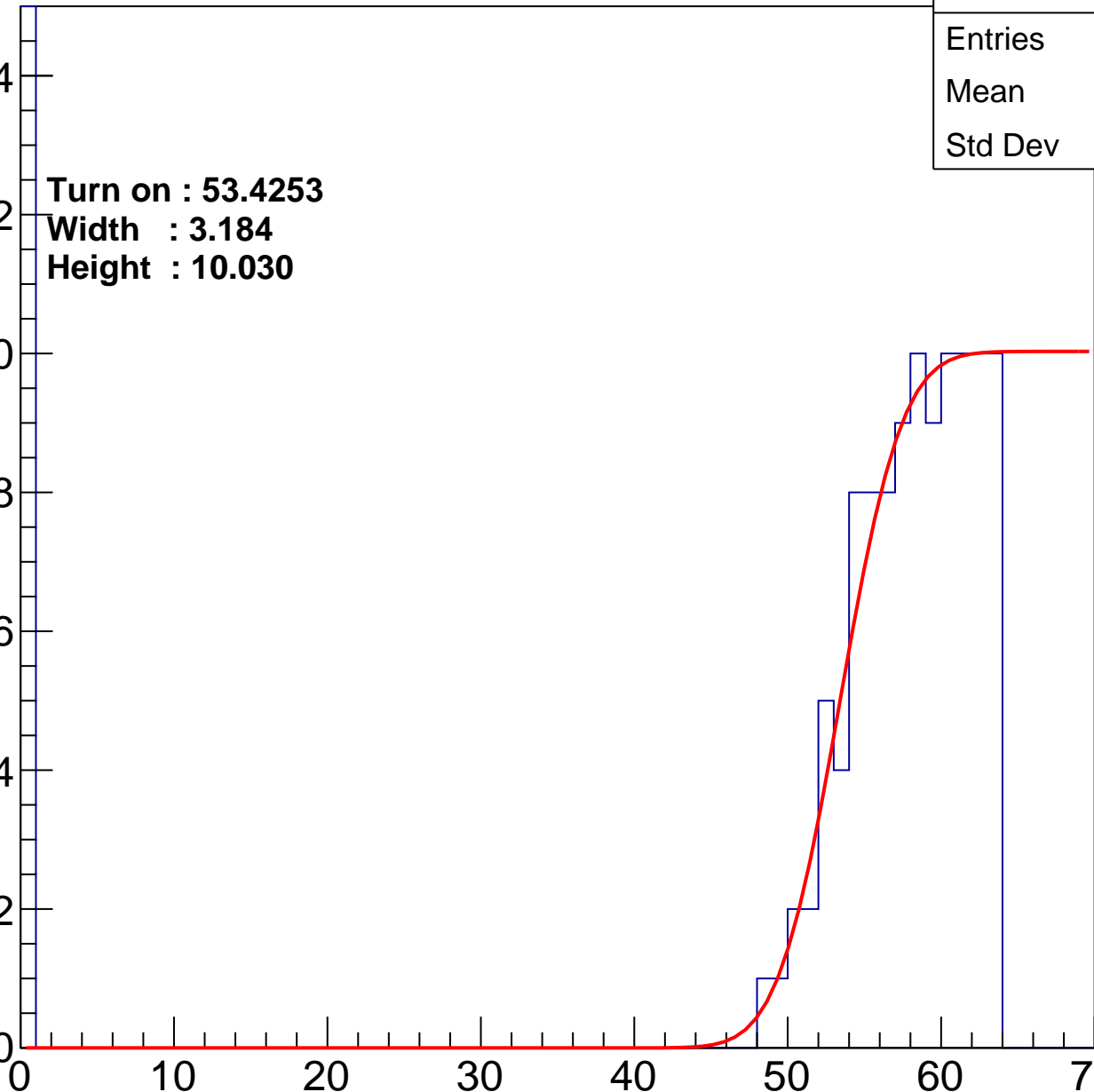
**Width : 3.184**

**Height : 10.030**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L104S, U3-ch12

calib\_packv5\_033123\_0516.root, FC#4, port A1

Entries	238
Mean	31.93
Std Dev	28.1

Turn on : 50.6390

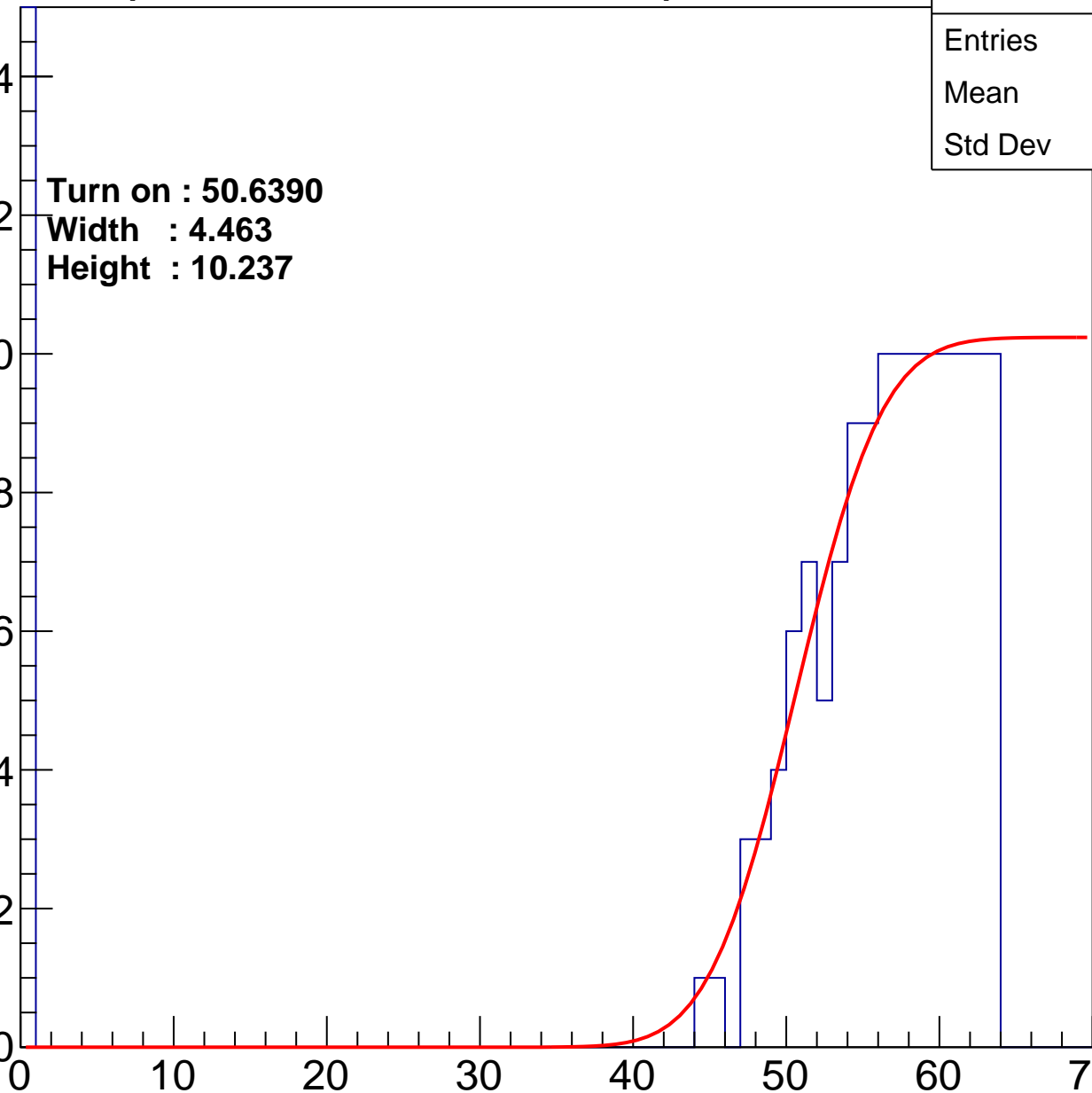
Width : 4.463

Height : 10.237

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L104S, U3-ch13

calib\_packv5\_033123\_0516.root, FC#4, port A1

Entries	175
Mean	33.75
Std Dev	28.7

Turn on : 54.5758

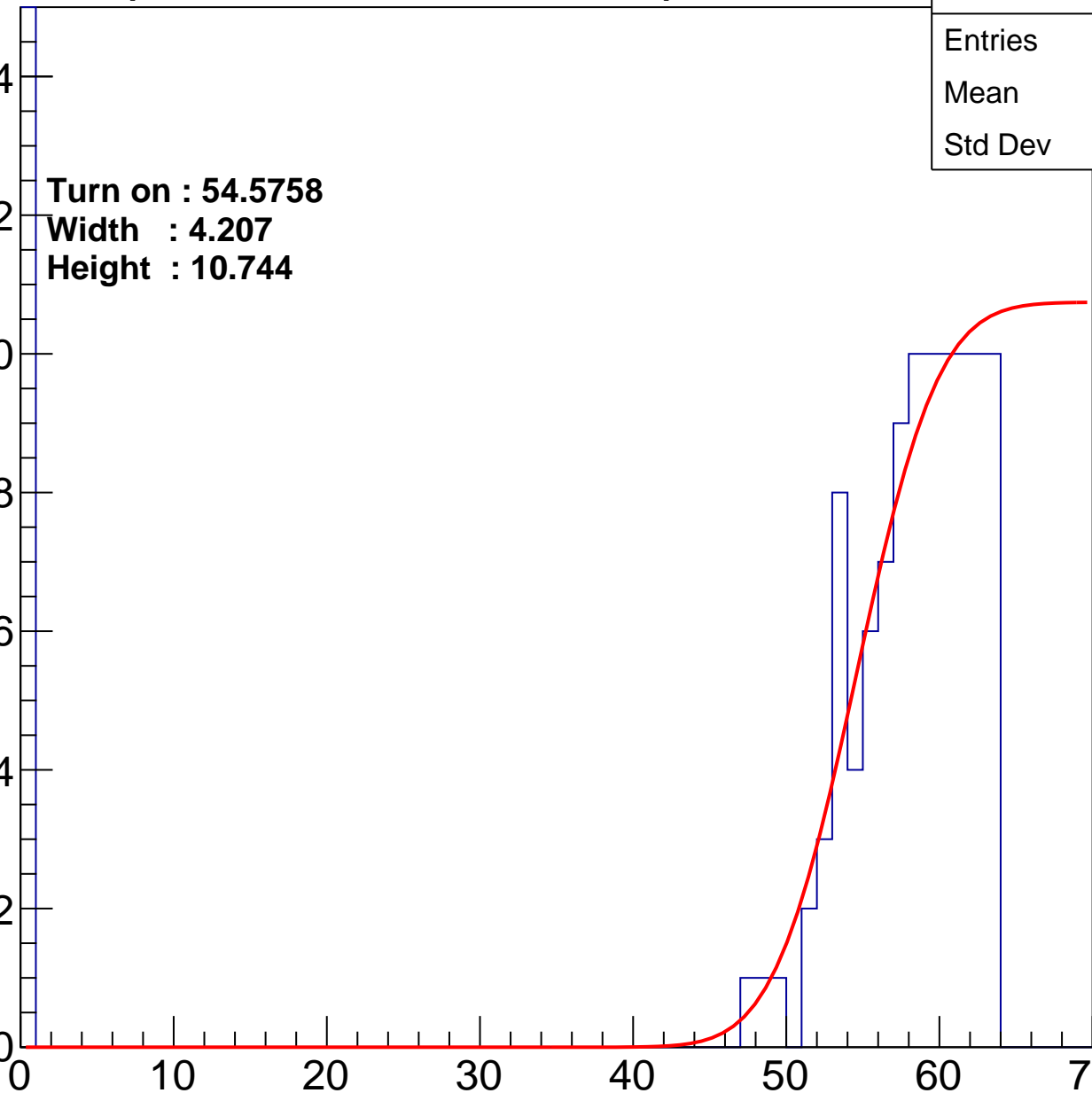
Width : 4.207

Height : 10.744

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L104S, U3-ch14

calib\_packv5\_033123\_0516.root, FC#4, port A1

Entries	224
Mean	29.64
Std Dev	28.74

Turn on : 52.1904

Width : 2.215

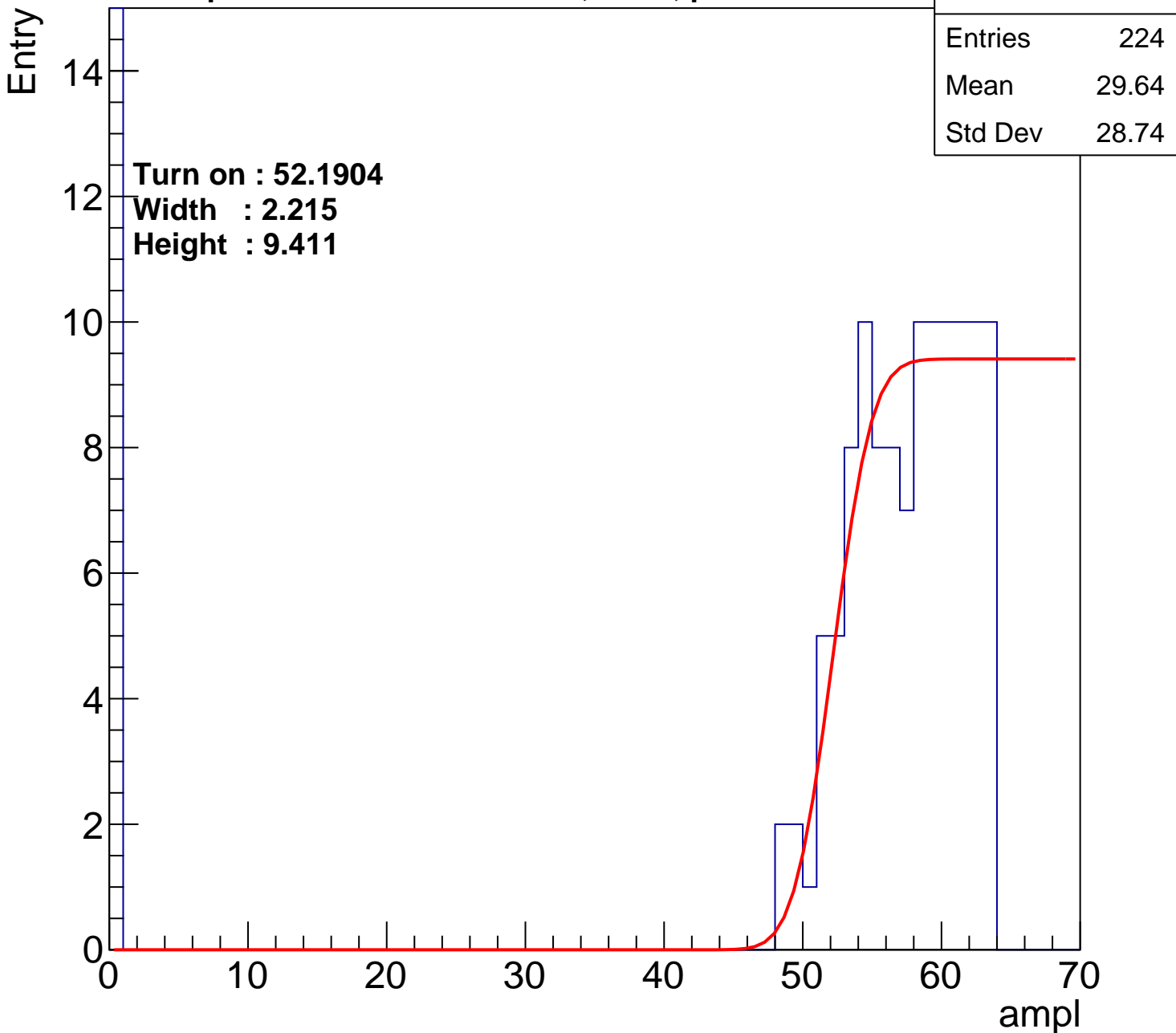
Height : 9.411

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70





# B1L104S, U3-ch15

calib\_packv5\_033123\_0516.root, FC#4, port A1

Entries	204
Mean	27.44
Std Dev	29.2

Turn on : 54.5806

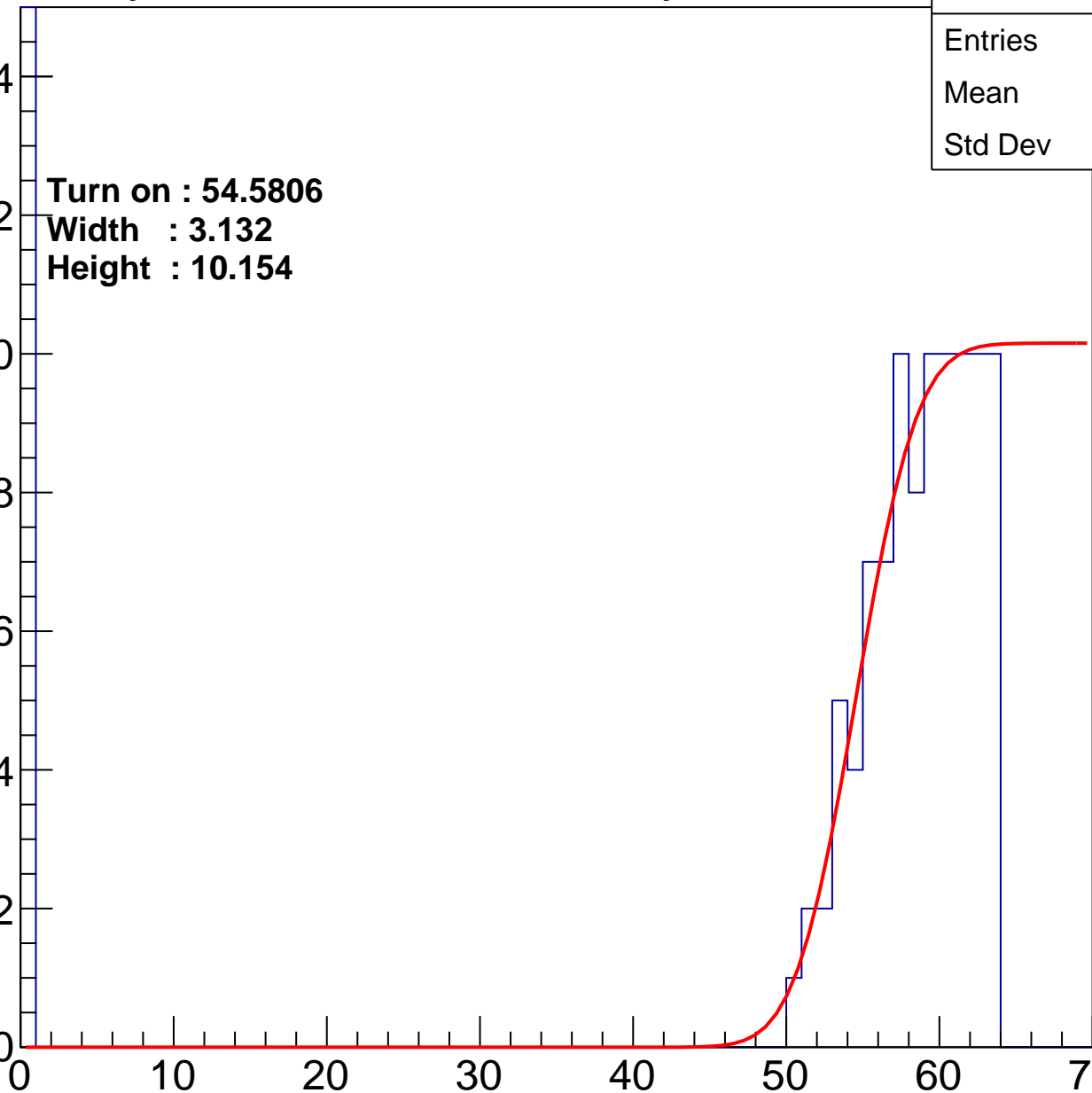
Width : 3.132

Height : 10.154

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L104S, U3-ch16

calib\_packv5\_033123\_0516.root, FC#4, port A1

Entries	207
Mean	35.73
Std Dev	27.21

Turn on : 50.4784

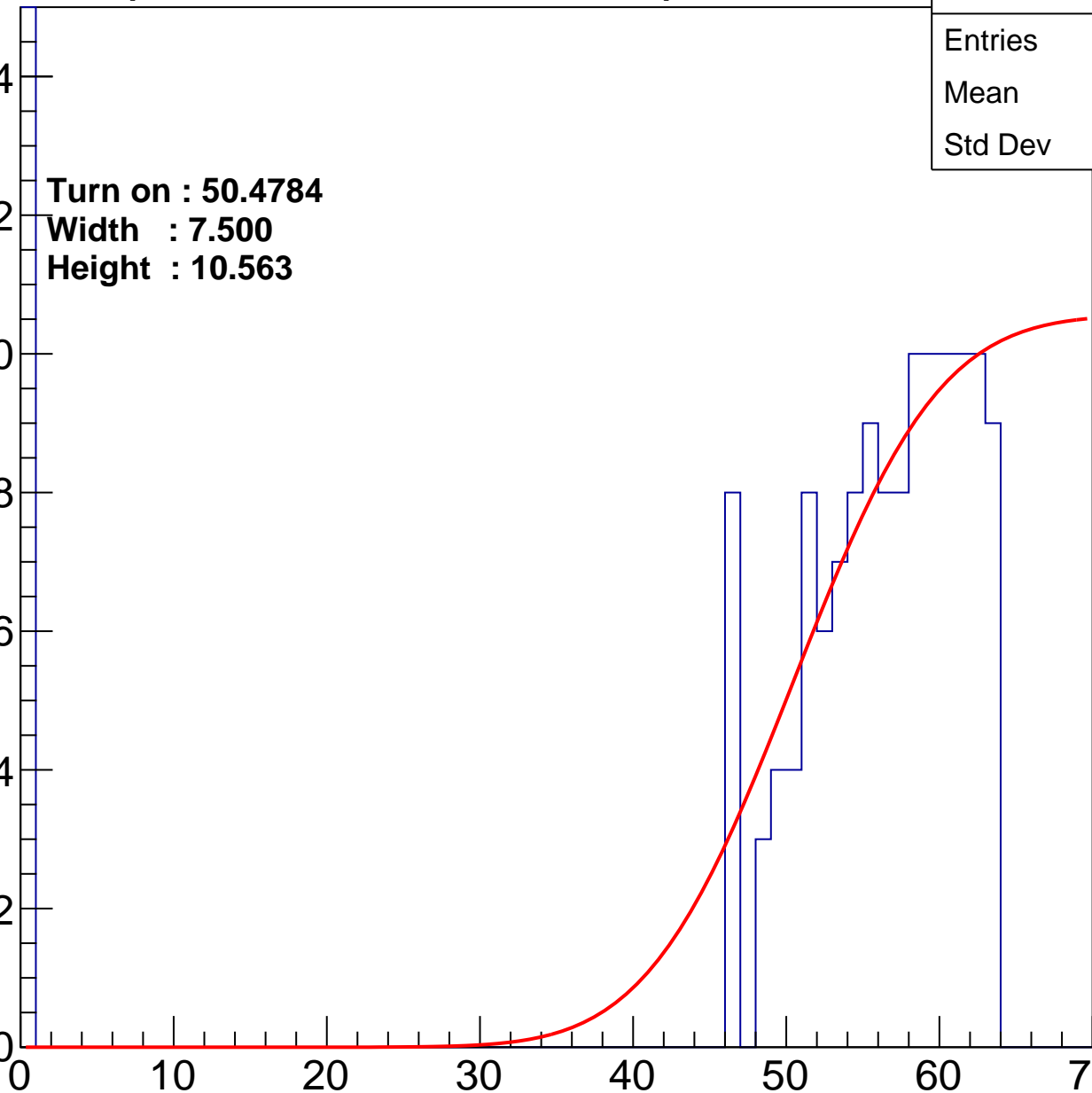
Width : 7.500

Height : 10.563

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L104S, U3-ch17

calib\_packv5\_033123\_0516.root, FC#4, port A1

Entries	201
Mean	30.17
Std Dev	28.98

Turn on : 54.4275

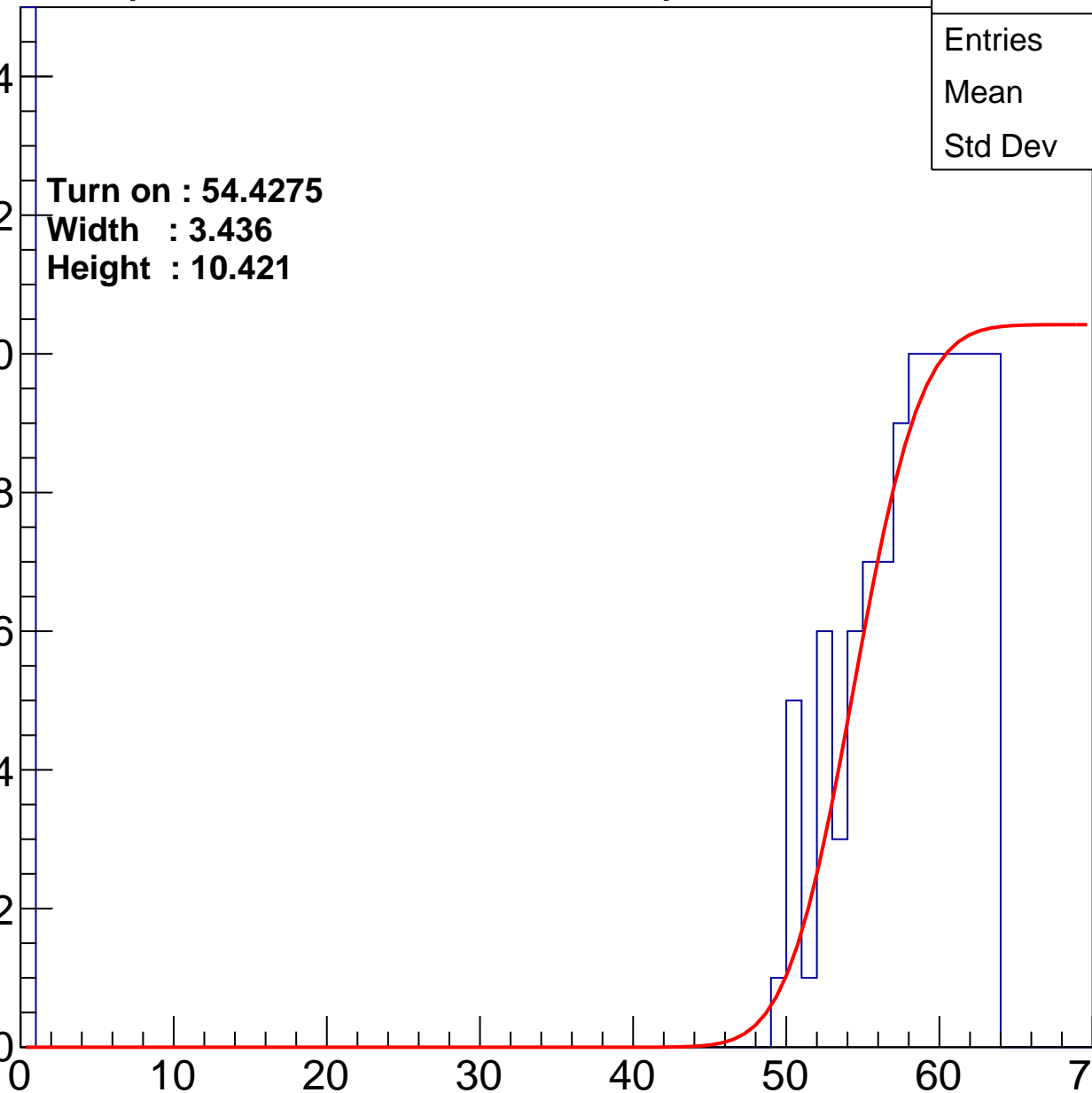
Width : 3.436

Height : 10.421

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L104S, U3-ch18

calib\_packv5\_033123\_0516.root, FC#4, port A1

Entries	200
Mean	34.47
Std Dev	28.04

**Turn on : 52.1242**

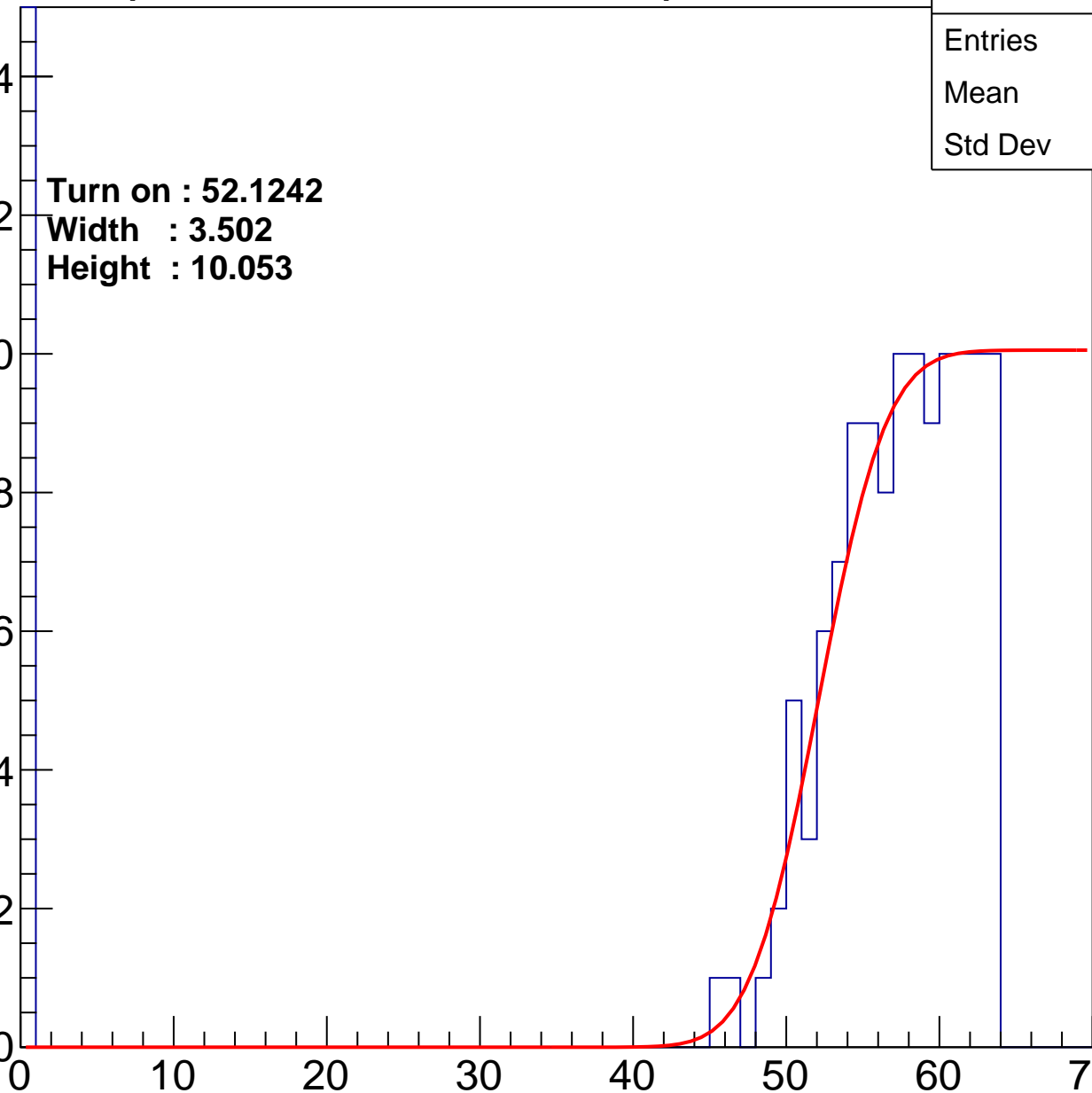
**Width : 3.502**

**Height : 10.053**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L104S, U3-ch19

calib\_packv5\_033123\_0516.root, FC#4, port A1

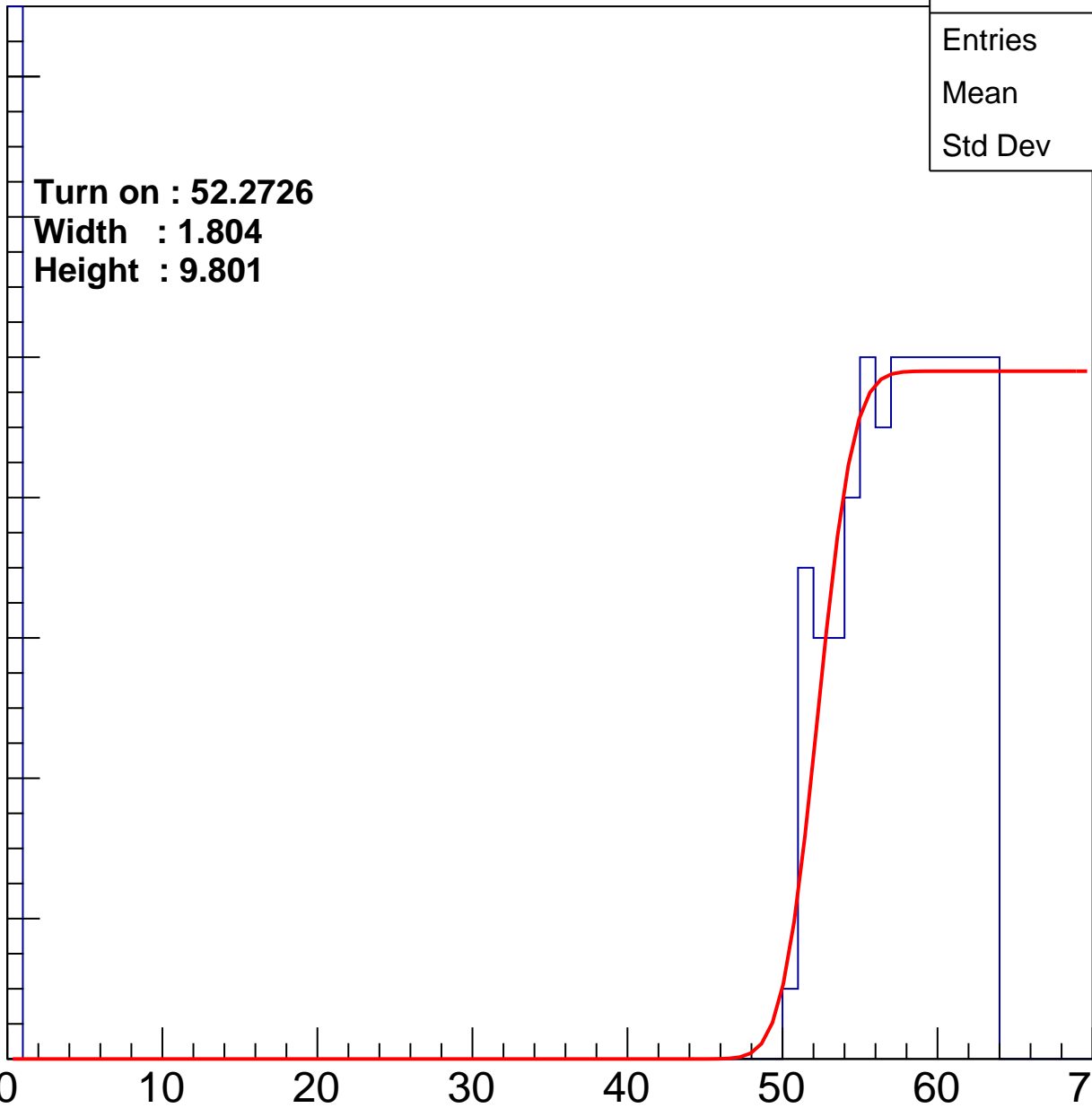
Entry

14  
12  
10  
8  
6  
4  
2  
0

Turn on : 52.2726  
Width : 1.804  
Height : 9.801

Entries	190
Mean	35.38
Std Dev	28.1

ampl



# B1L104S, U3-ch20

calib\_packv5\_033123\_0516.root, FC#4, port A1

Entries	205
Mean	31.1
Std Dev	28.77

Turn on : 52.9261

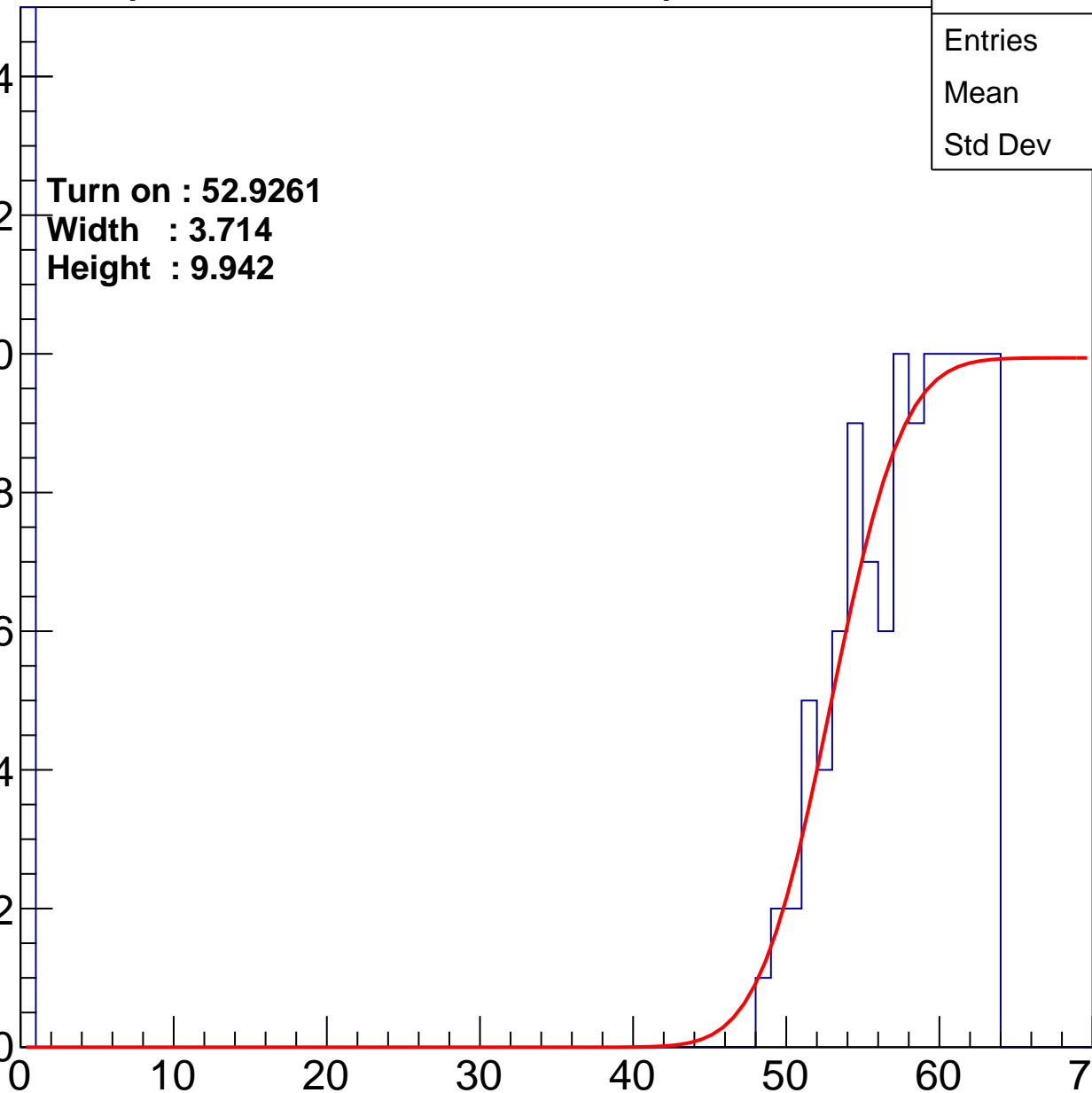
Width : 3.714

Height : 9.942

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L104S, U3-ch21

calib\_packv5\_033123\_0516.root, FC#4, port A1

Entries	195
Mean	27.28
Std Dev	29.25

Turn on : 55.1929

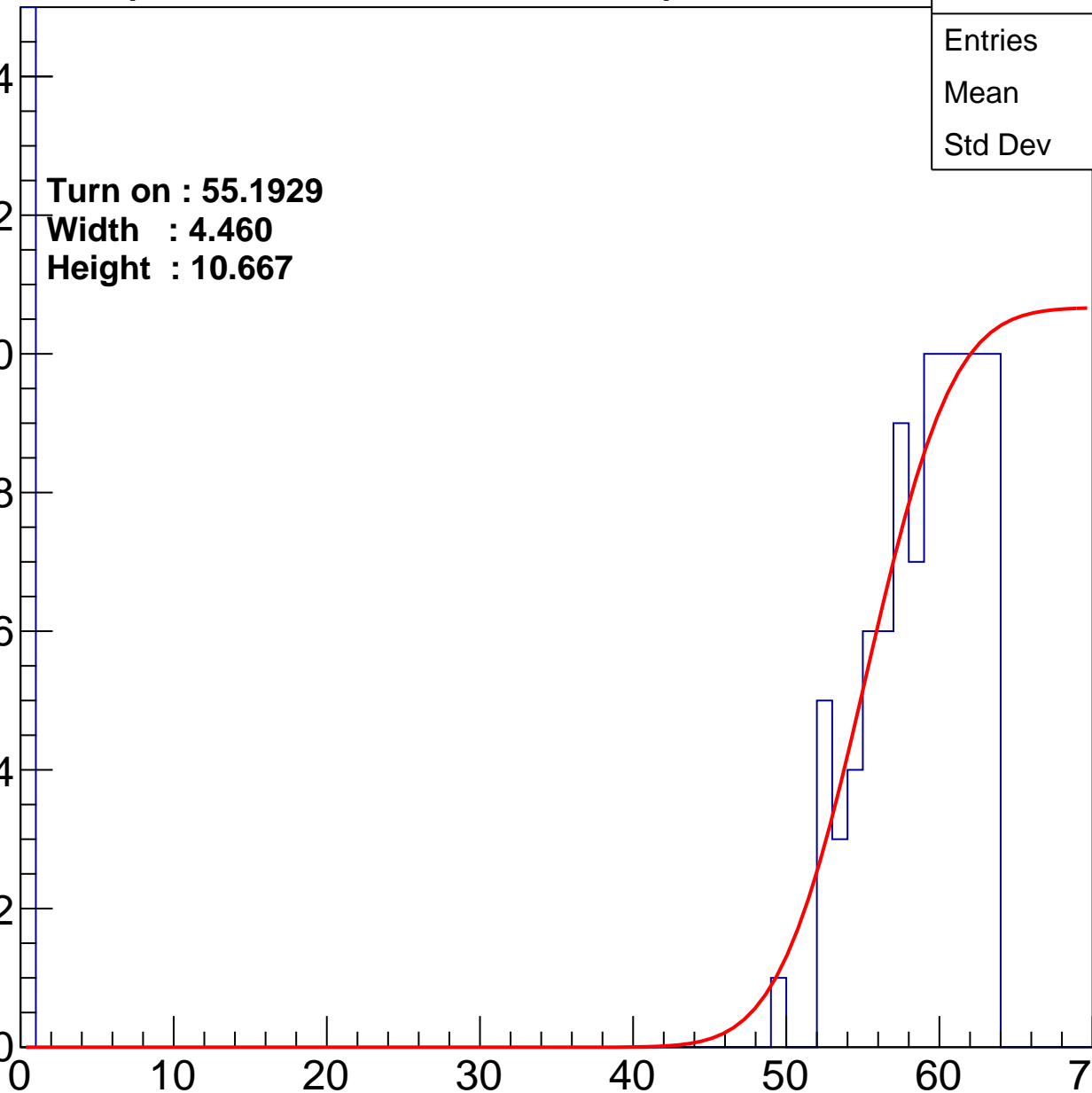
Width : 4.460

Height : 10.667

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L104S, U3-ch22

calib\_packv5\_033123\_0516.root, FC#4, port A1

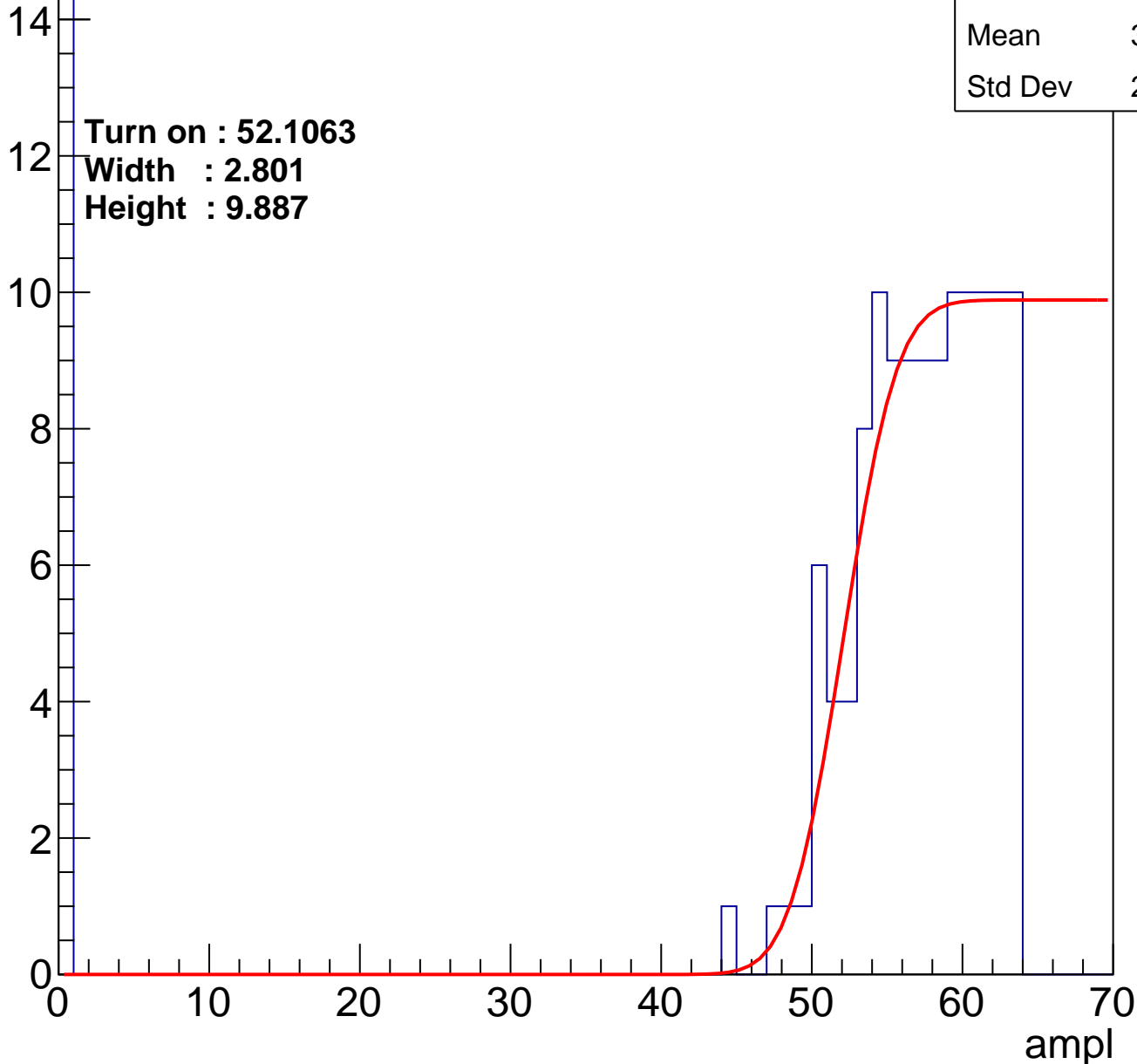
Entry

Entries	213
Mean	32.62
Std Dev	28.35

Turn on : 52.1063

Width : 2.801

Height : 9.887





# B1L104S, U3-ch23

calib\_packv5\_033123\_0516.root, FC#4, port A1

Entries	207
Mean	32.68
Std Dev	28.52

Turn on : 52.1025

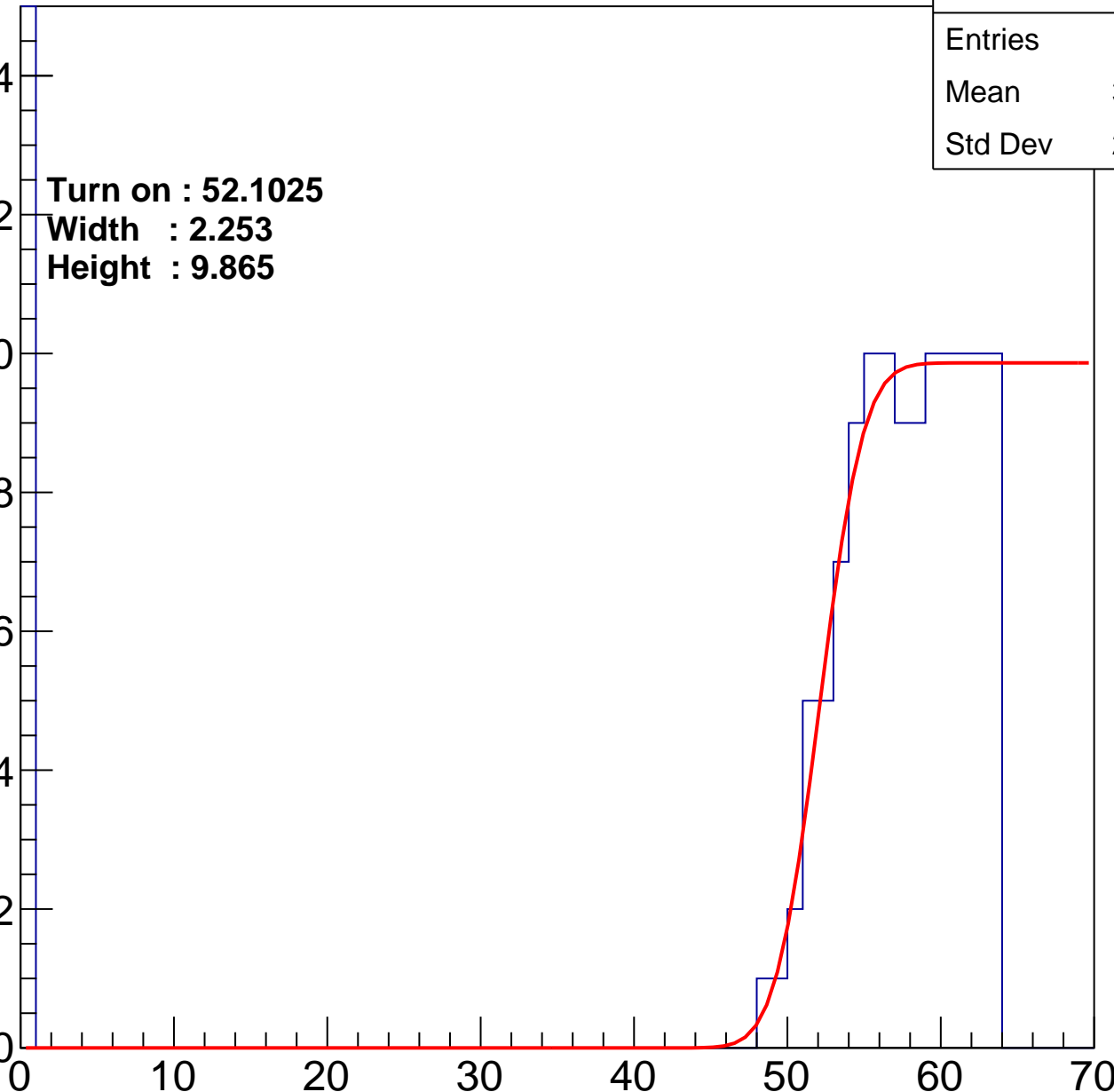
Width : 2.253

Height : 9.865

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L104S, U3-ch24

calib\_packv5\_033123\_0516.root, FC#4, port A1

Entries	199
Mean	31.6
Std Dev	28.84

Turn on : 53.1320

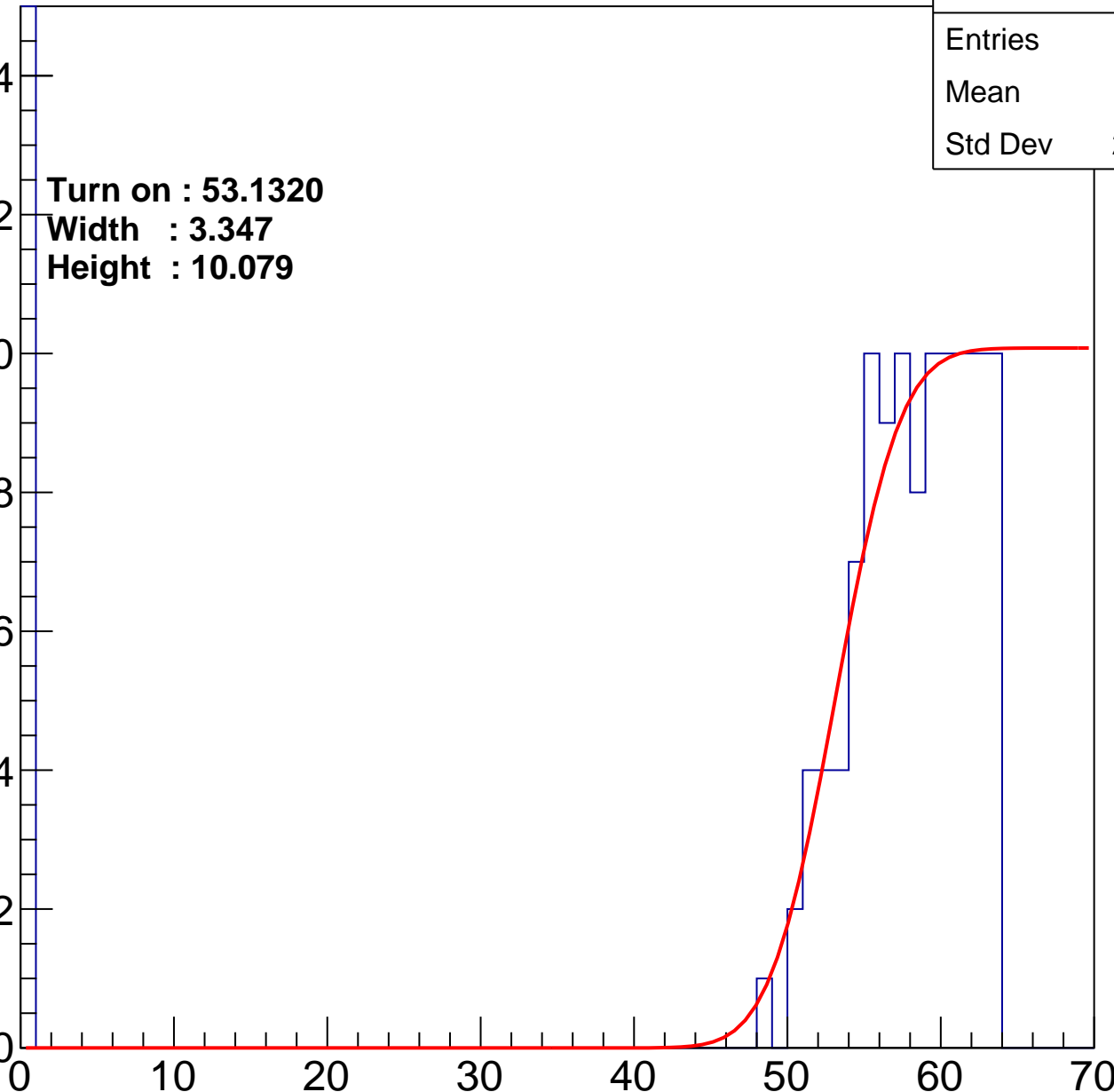
Width : 3.347

Height : 10.079

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L104S, U3-ch25

calib\_packv5\_033123\_0516.root, FC#4, port A1

Entries	218
Mean	31.73
Std Dev	28.56

Turn on : 52.0386

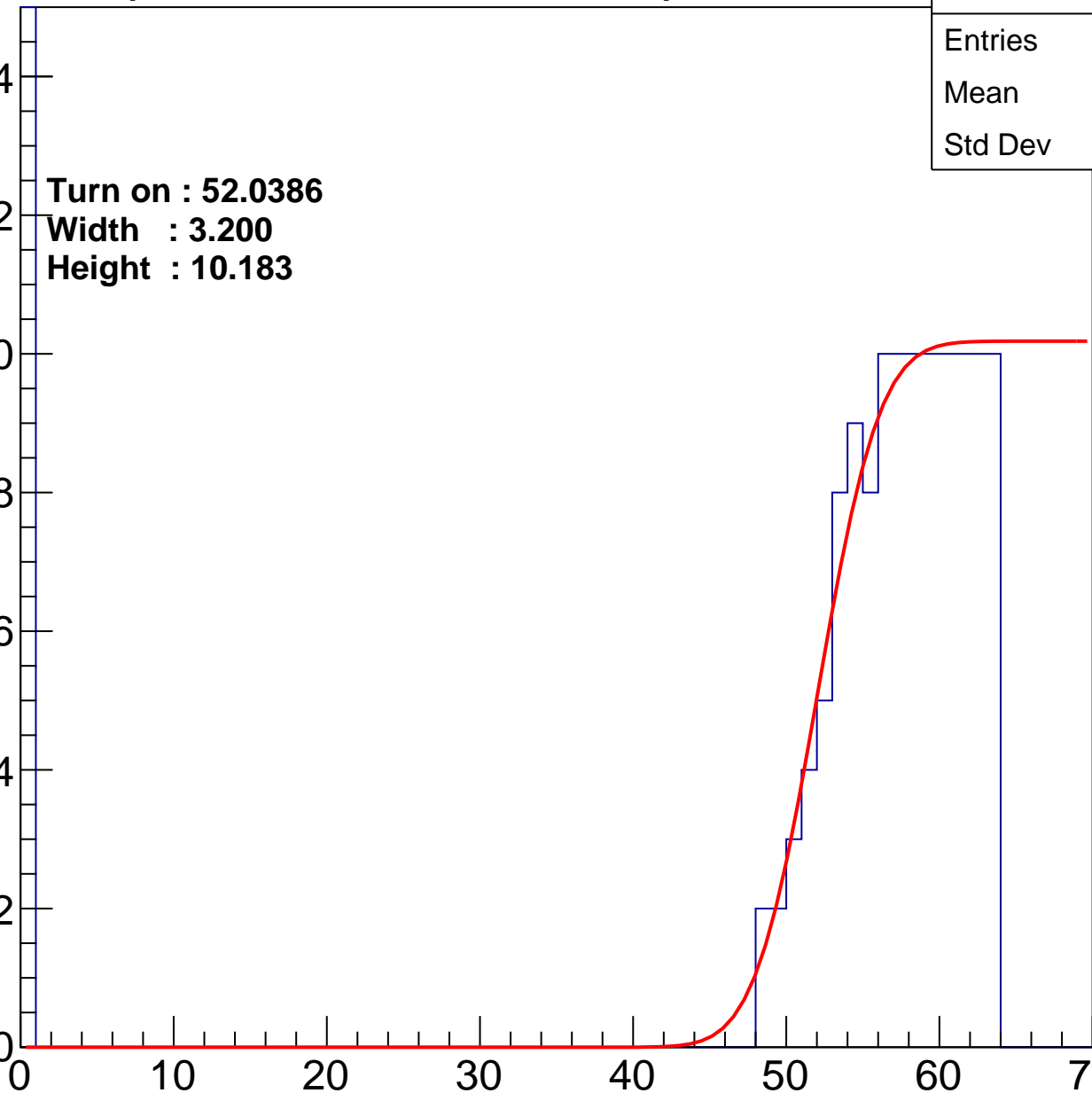
Width : 3.200

Height : 10.183

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L104S, U3-ch26

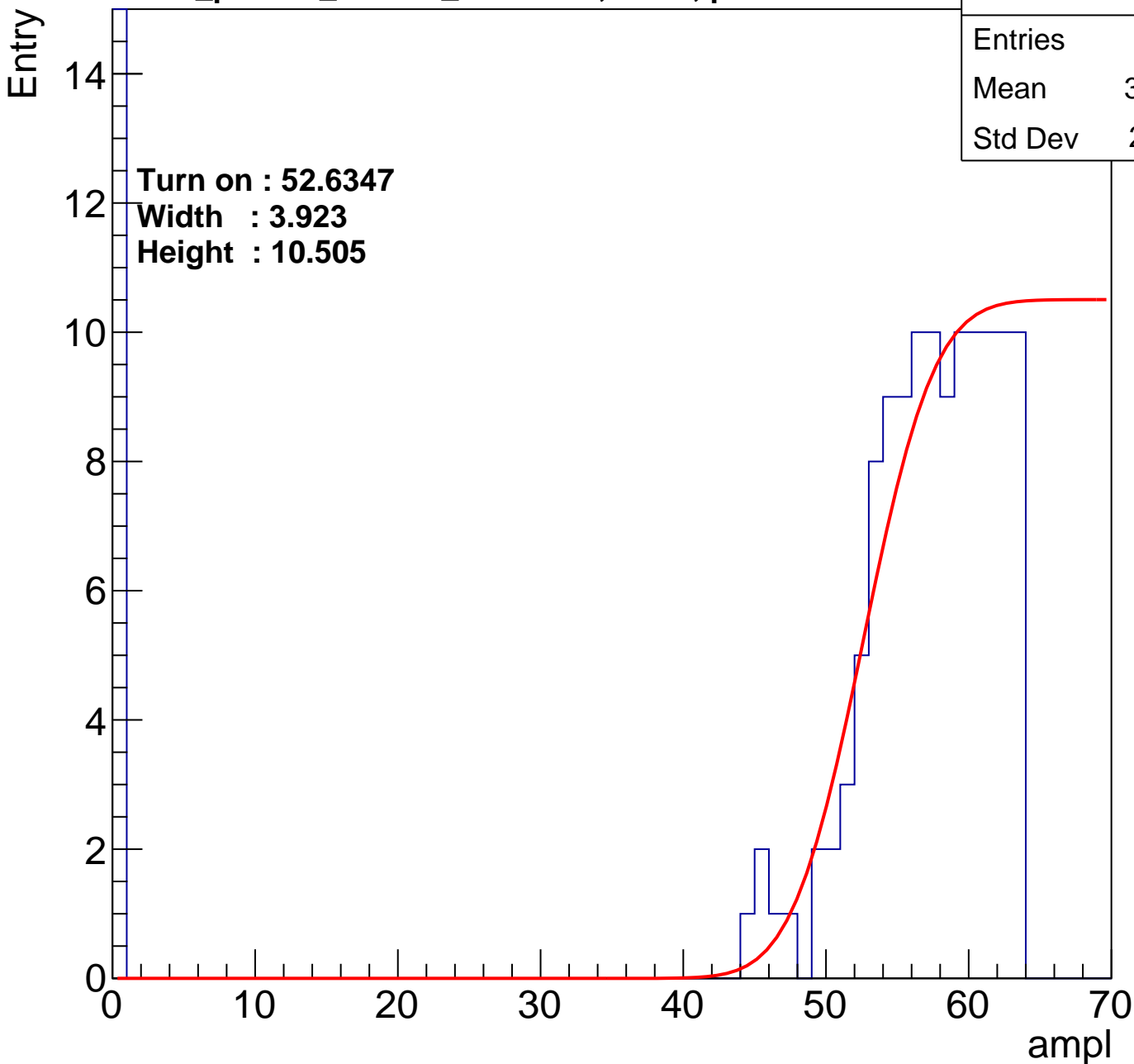
calib\_packv5\_033123\_0516.root, FC#4, port A1

Entries	201
Mean	34.55
Std Dev	28.01

Turn on : 52.6347

Width : 3.923

Height : 10.505



# B1L104S, U3-ch27

calib\_packv5\_033123\_0516.root, FC#4, port A1

Entries	202
Mean	36.66
Std Dev	27.22

Turn on : 50.3814

Width : 4.524

Height : 10.134

Entry

14

12

10

8

6

4

2

0

0

10

20

30

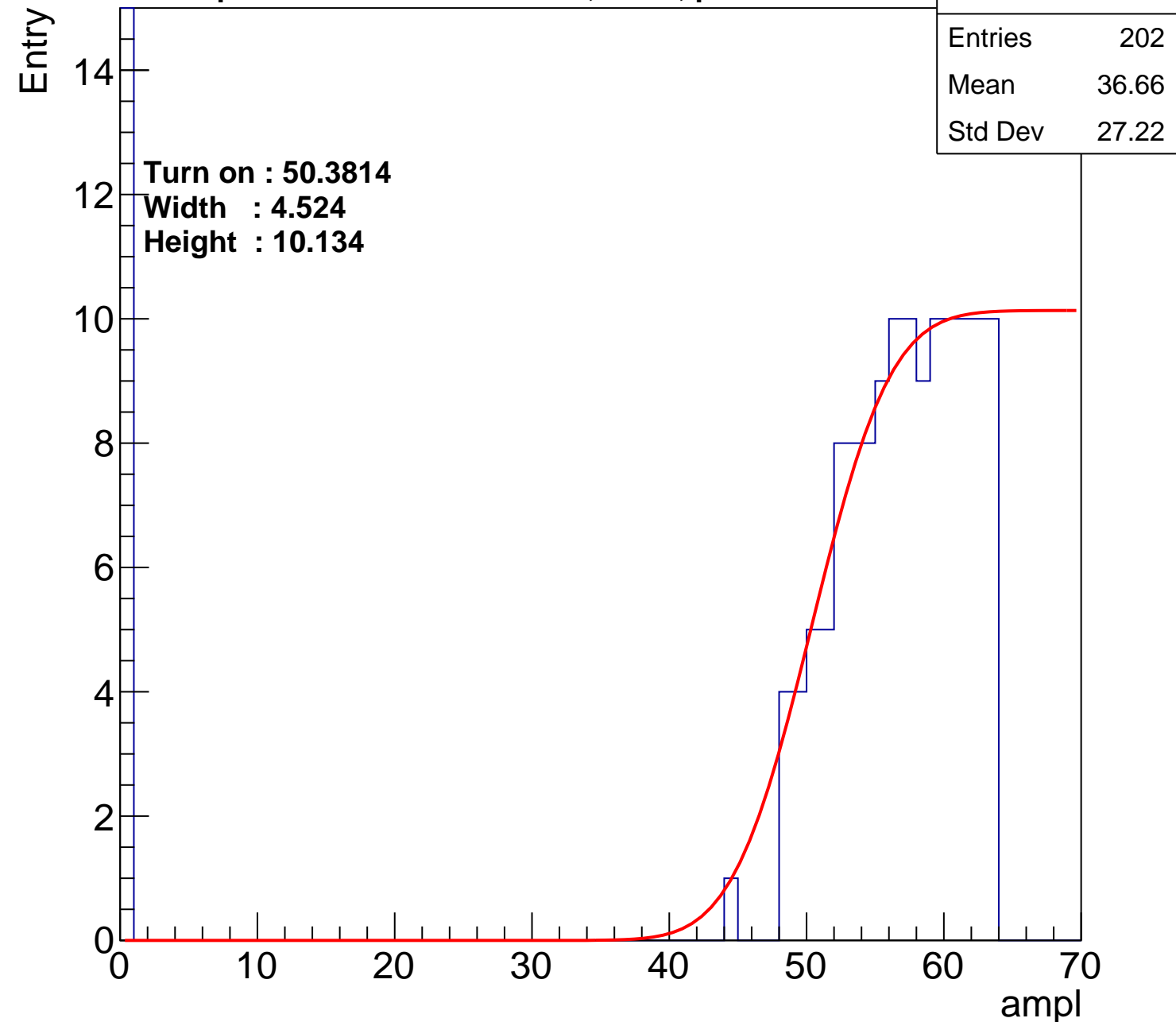
40

50

60

ampl

70



# B1L104S, U3-ch28

calib\_packv5\_033123\_0516.root, FC#4, port A1

Entries	206
Mean	27.9
Std Dev	29.12

**Turn on : 54.6372**

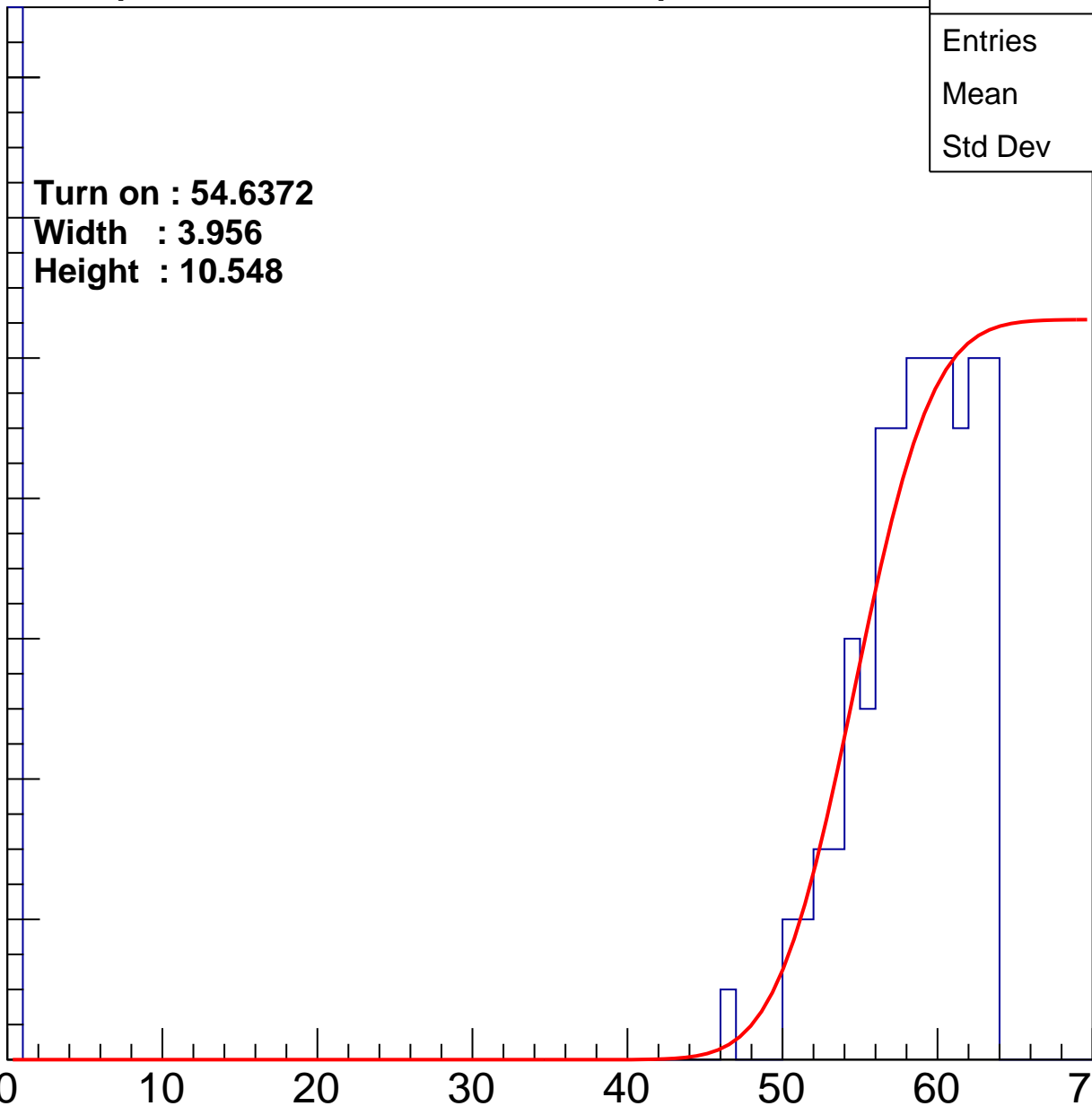
**Width : 3.956**

**Height : 10.548**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L104S, U3-ch29

calib\_packv5\_033123\_0516.root, FC#4, port A1

Entries	196
Mean	29.56
Std Dev	29.09

Turn on : 55.5859

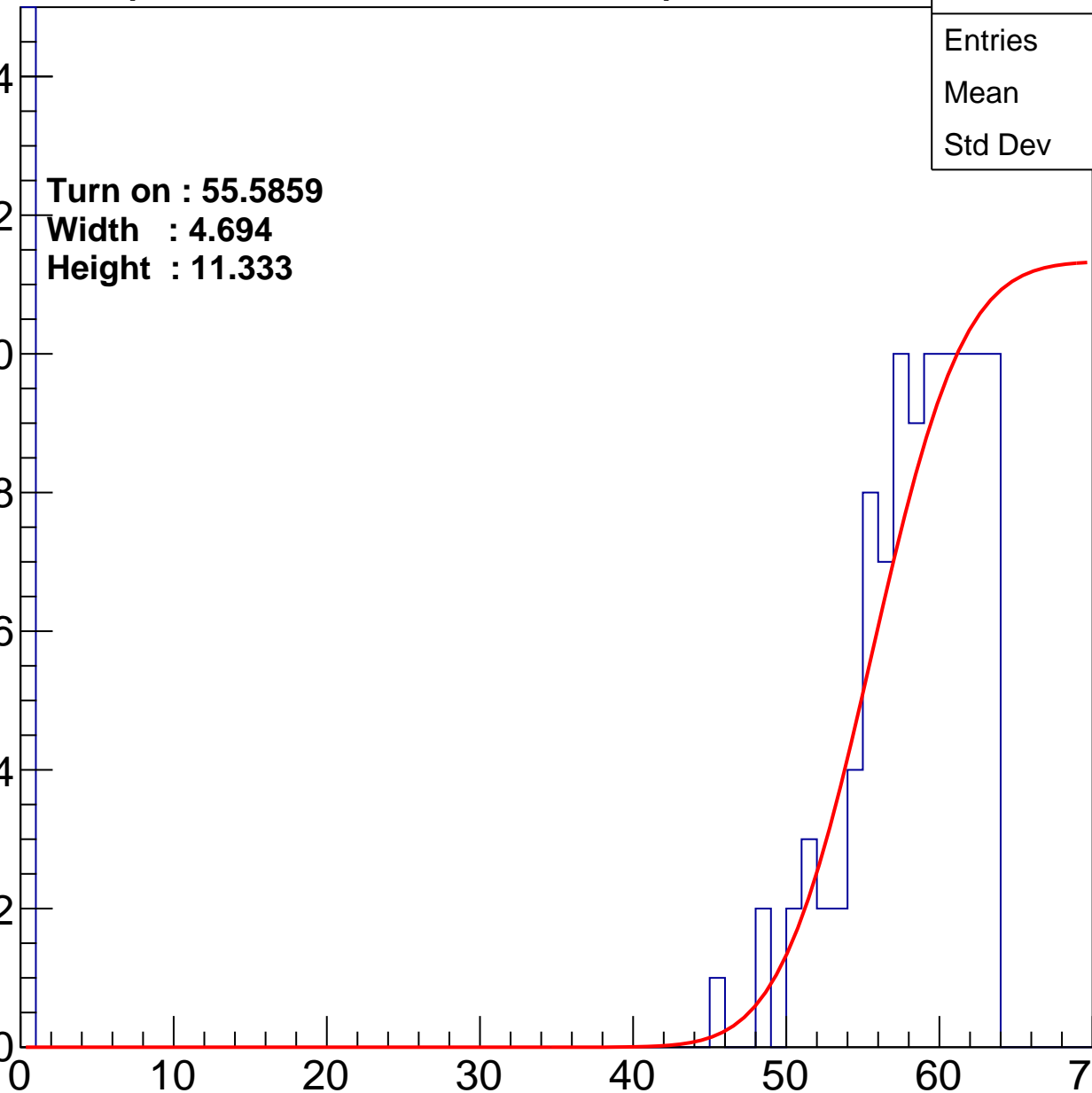
Width : 4.694

Height : 11.333

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L104S, U3-ch30

calib\_packv5\_033123\_0516.root, FC#4, port A1

Entries	210
Mean	27.66
Std Dev	29.1

Turn on : 54.0306

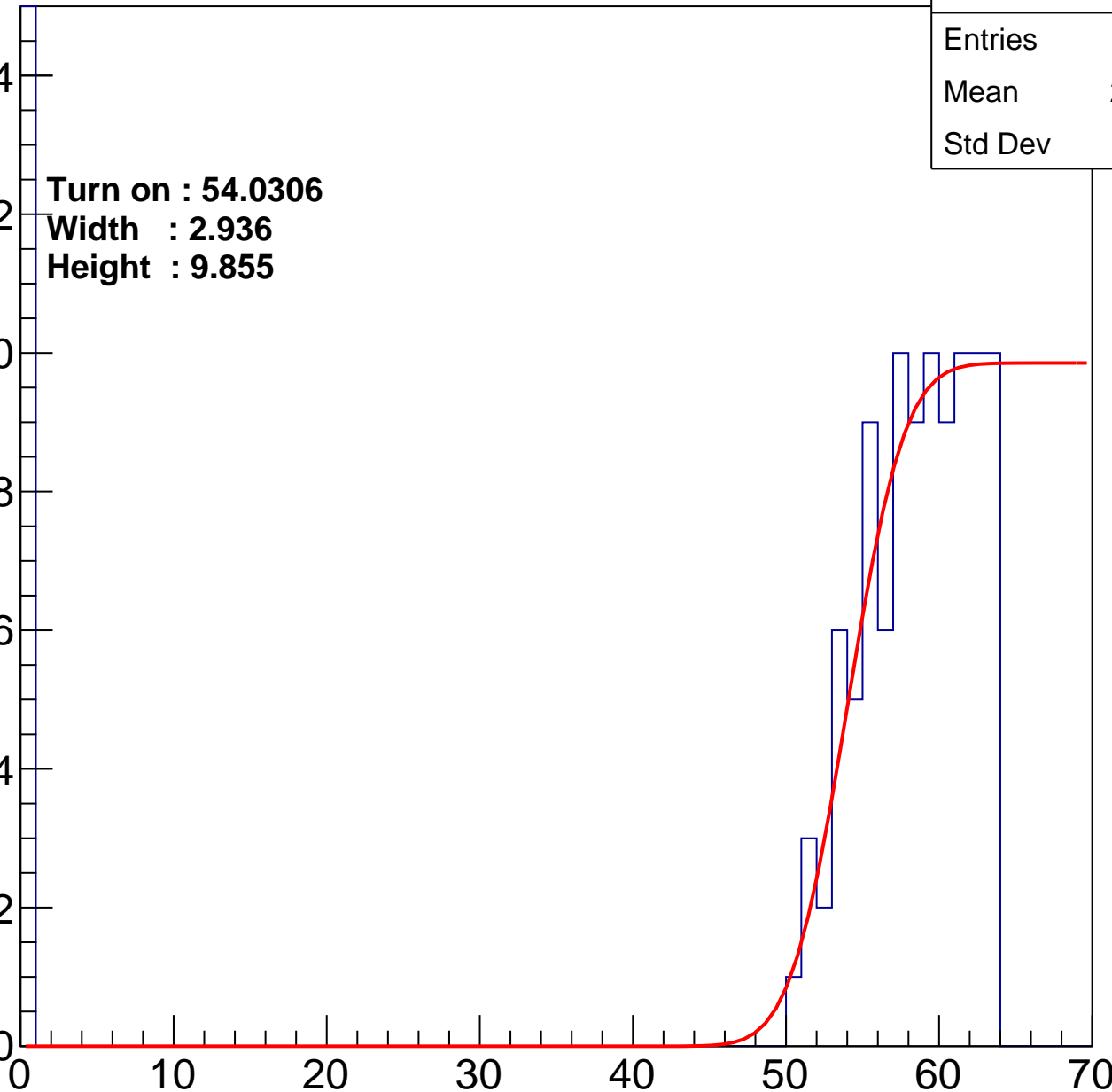
Width : 2.936

Height : 9.855

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L104S, U3-ch31

calib\_packv5\_033123\_0516.root, FC#4, port A1

Entries	188
Mean	32.3
Std Dev	28.85

**Turn on : 53.7543**

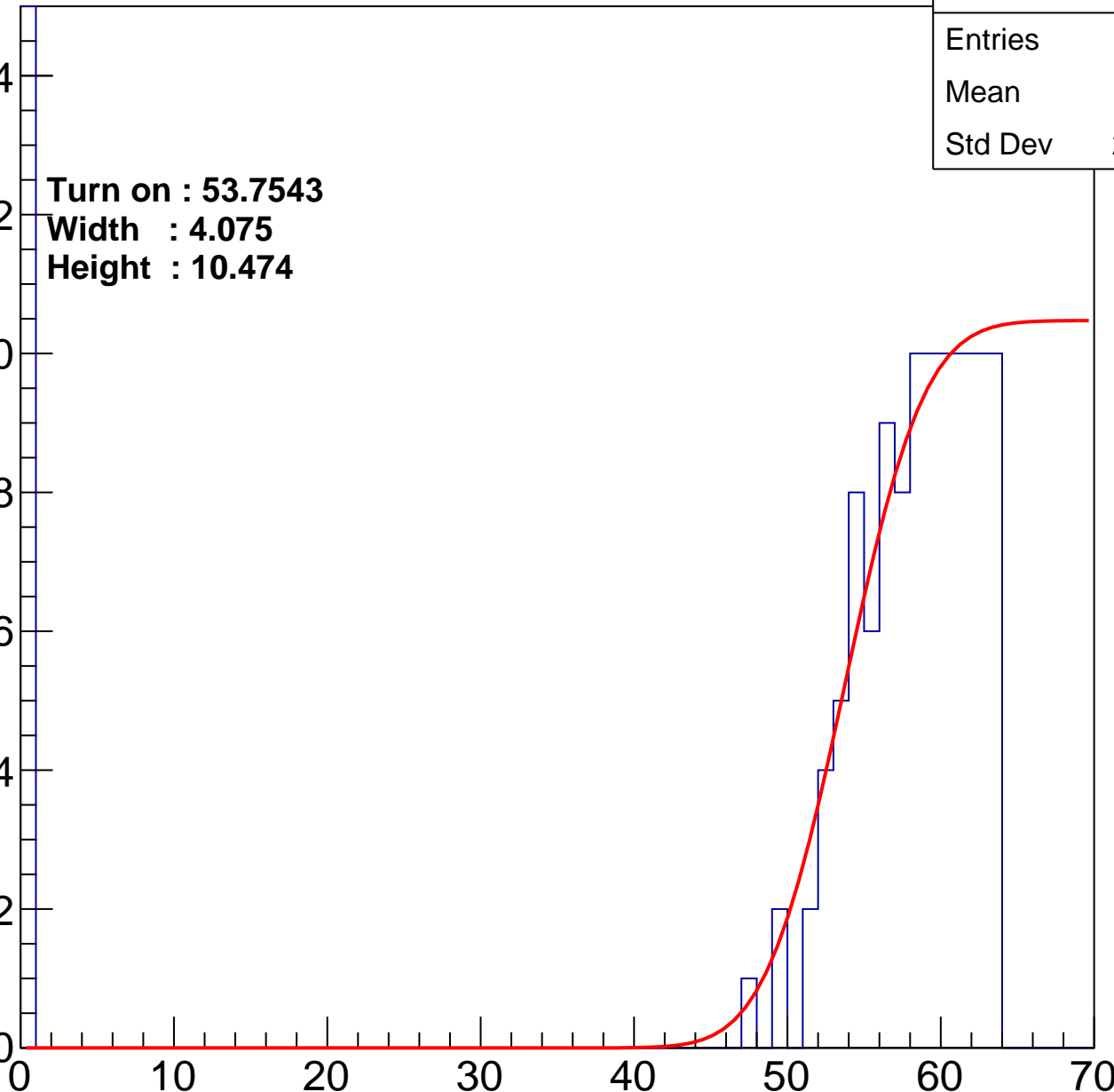
**Width : 4.075**

**Height : 10.474**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L104S, U3-ch32

calib\_packv5\_033123\_0516.root, FC#4, port A1

Entries	239
Mean	28.7
Std Dev	28.72

Turn on : 52.3366

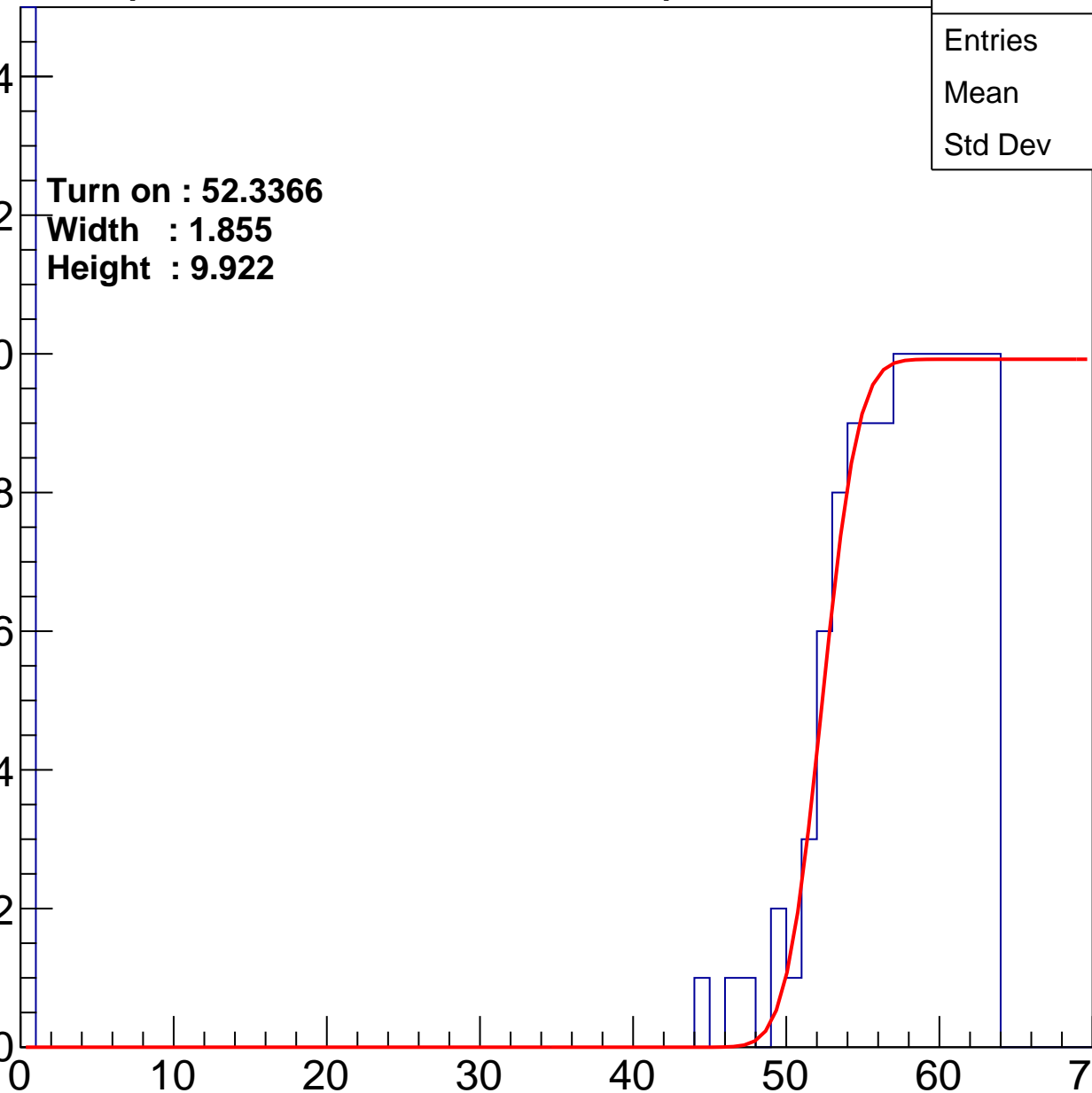
Width : 1.855

Height : 9.922

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L104S, U3-ch33

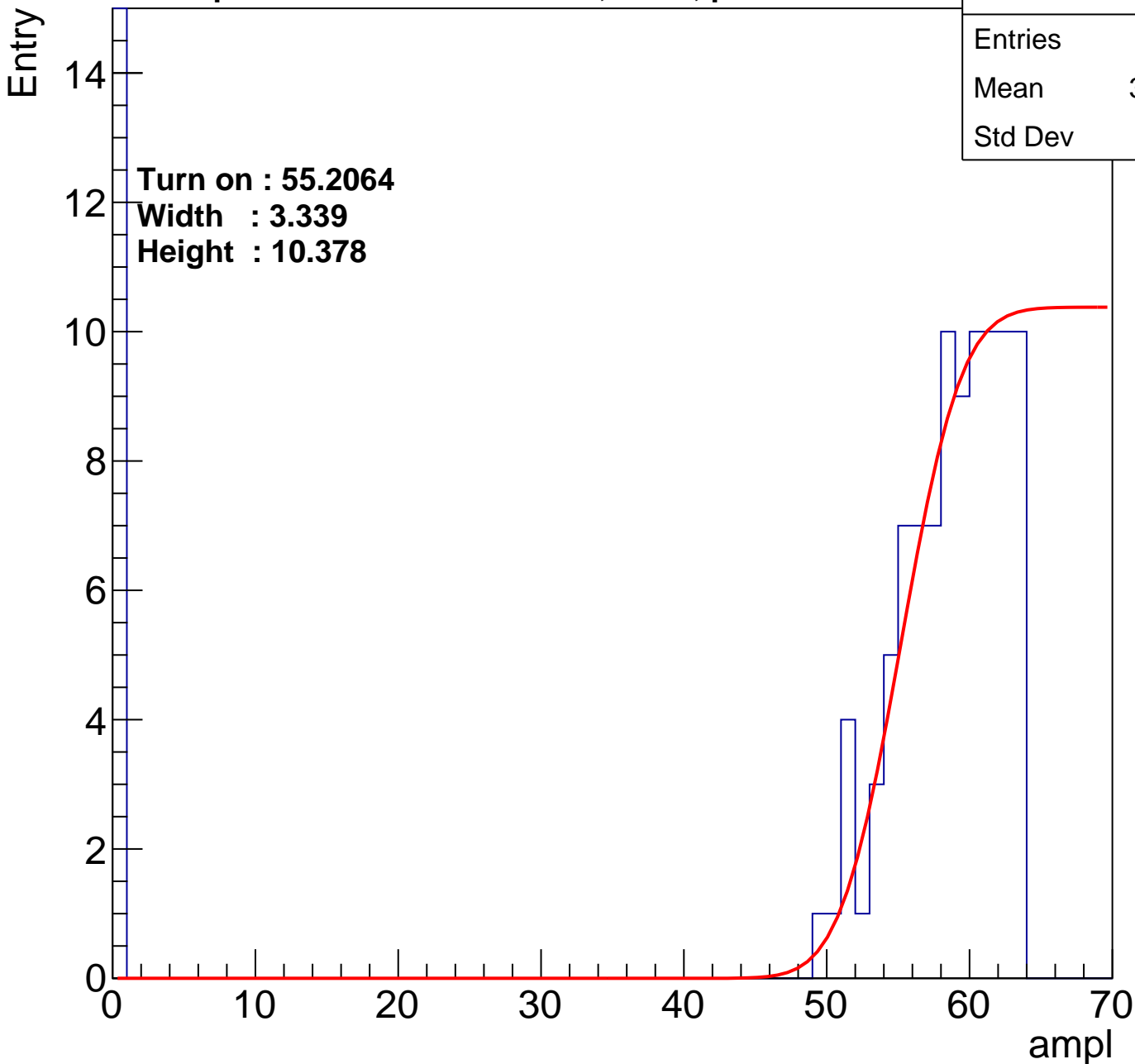
calib\_packv5\_033123\_0516.root, FC#4, port A1

Entries	184
Mean	30.06
Std Dev	29.2

Turn on : 55.2064

Width : 3.339

Height : 10.378



# B1L104S, U3-ch34

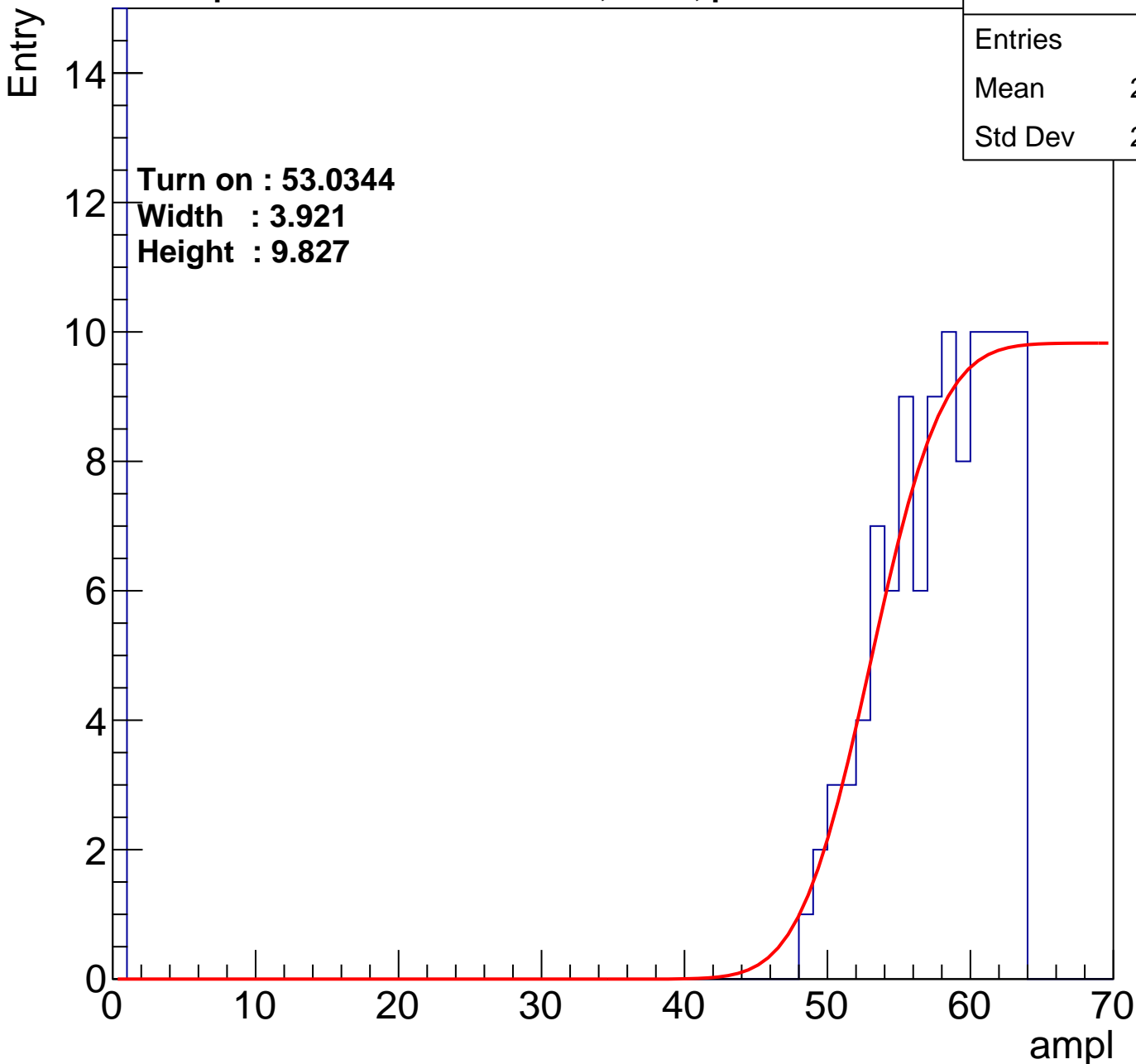
calib\_packv5\_033123\_0516.root, FC#4, port A1

Entries	223
Mean	27.84
Std Dev	28.85

Turn on : 53.0344

Width : 3.921

Height : 9.827



# B1L104S, U3-ch35

calib\_packv5\_033123\_0516.root, FC#4, port A1

Entries	183
Mean	34.96
Std Dev	28.31

**Turn on : 53.2248**

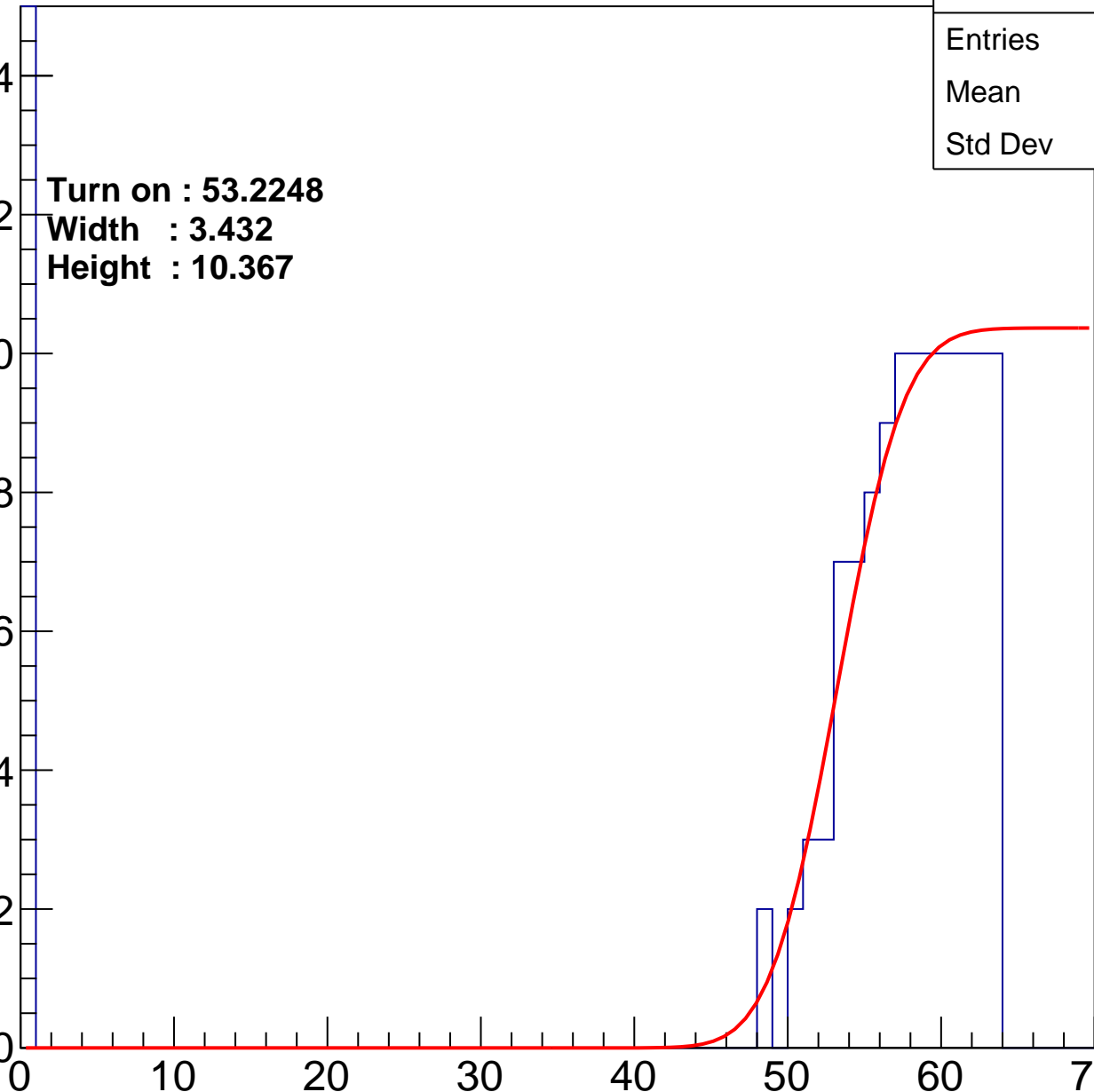
**Width : 3.432**

**Height : 10.367**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L104S, U3-ch36

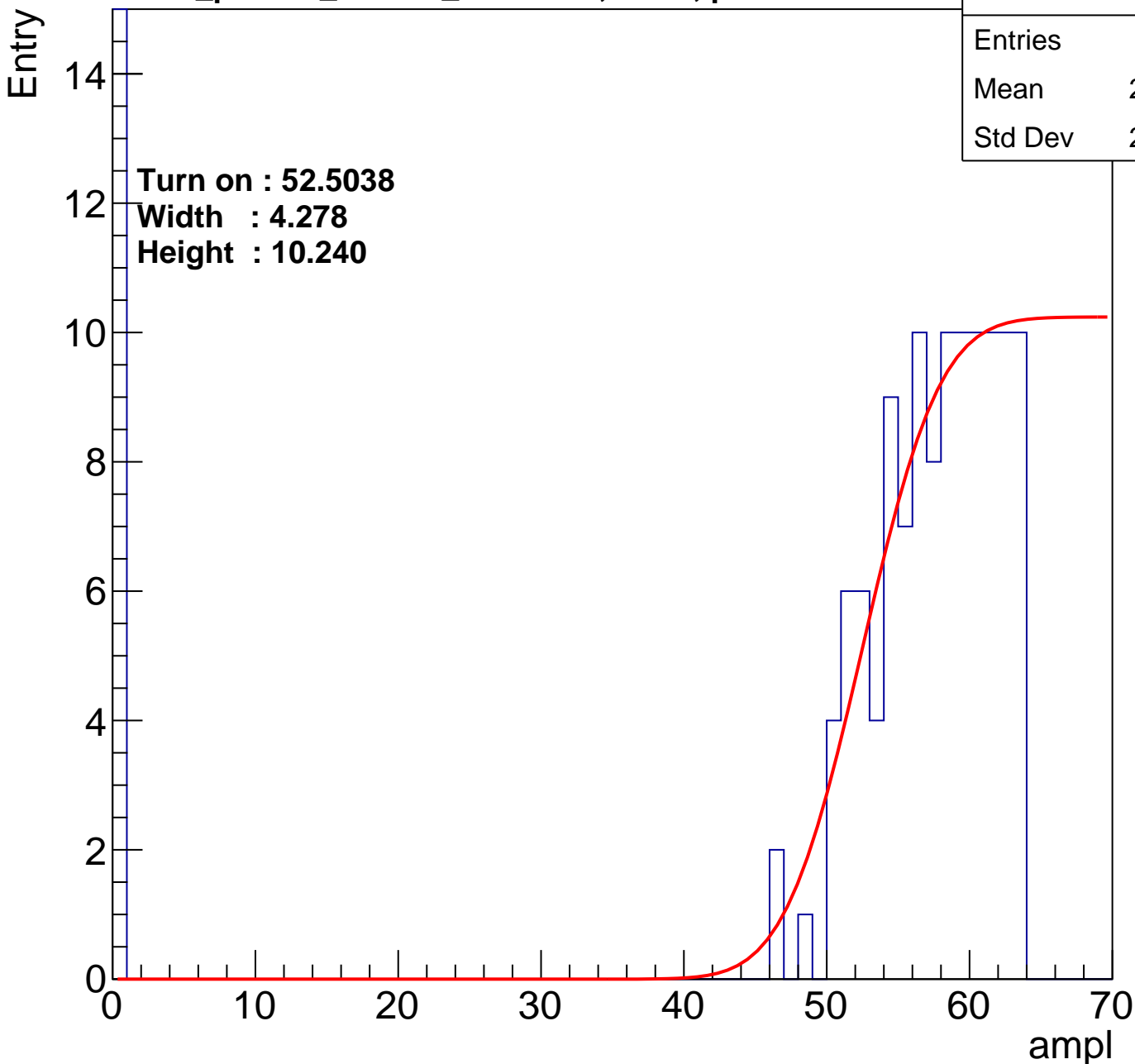
calib\_packv5\_033123\_0516.root, FC#4, port A1

Entries	235
Mean	28.46
Std Dev	28.72

Turn on : 52.5038

Width : 4.278

Height : 10.240



# B1L104S, U3-ch37

calib\_packv5\_033123\_0516.root, FC#4, port A1

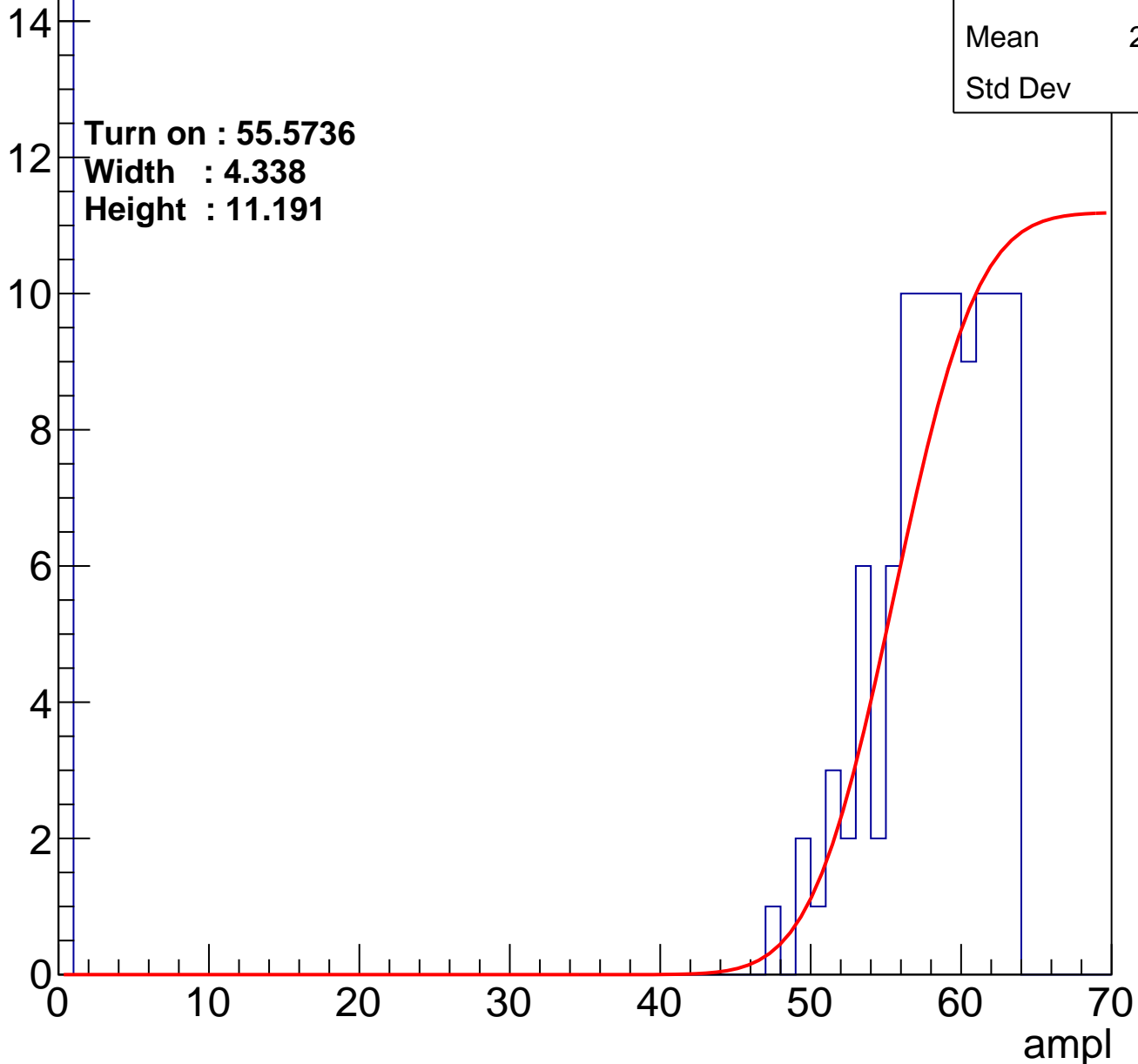
Entry

Entries	219
Mean	26.98
Std Dev	29

Turn on : 55.5736

Width : 4.338

Height : 11.191



# B1L104S, U3-ch38

calib\_packv5\_033123\_0516.root, FC#4, port A1

Entries	184
Mean	27.43
Std Dev	29.36

Turn on : 56.1796

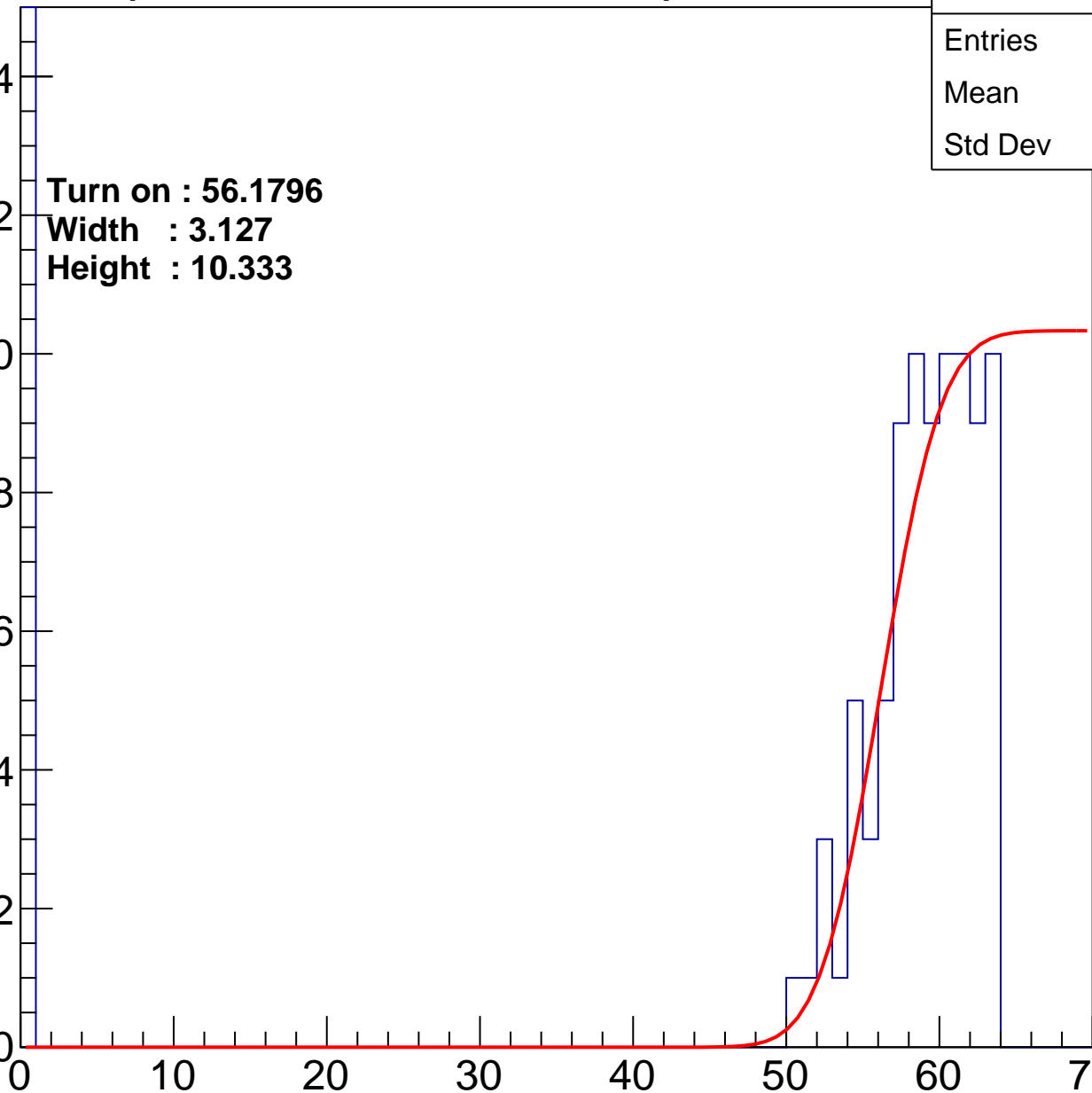
Width : 3.127

Height : 10.333

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L104S, U3-ch39

calib\_packv5\_033123\_0516.root, FC#4, port A1

Entries	172
Mean	39.01
Std Dev	26.94

**Turn on : 52.2778**

**Width : 2.318**

**Height : 9.894**

Entry

14

12

10

8

6

4

2

0

0

10

20

30

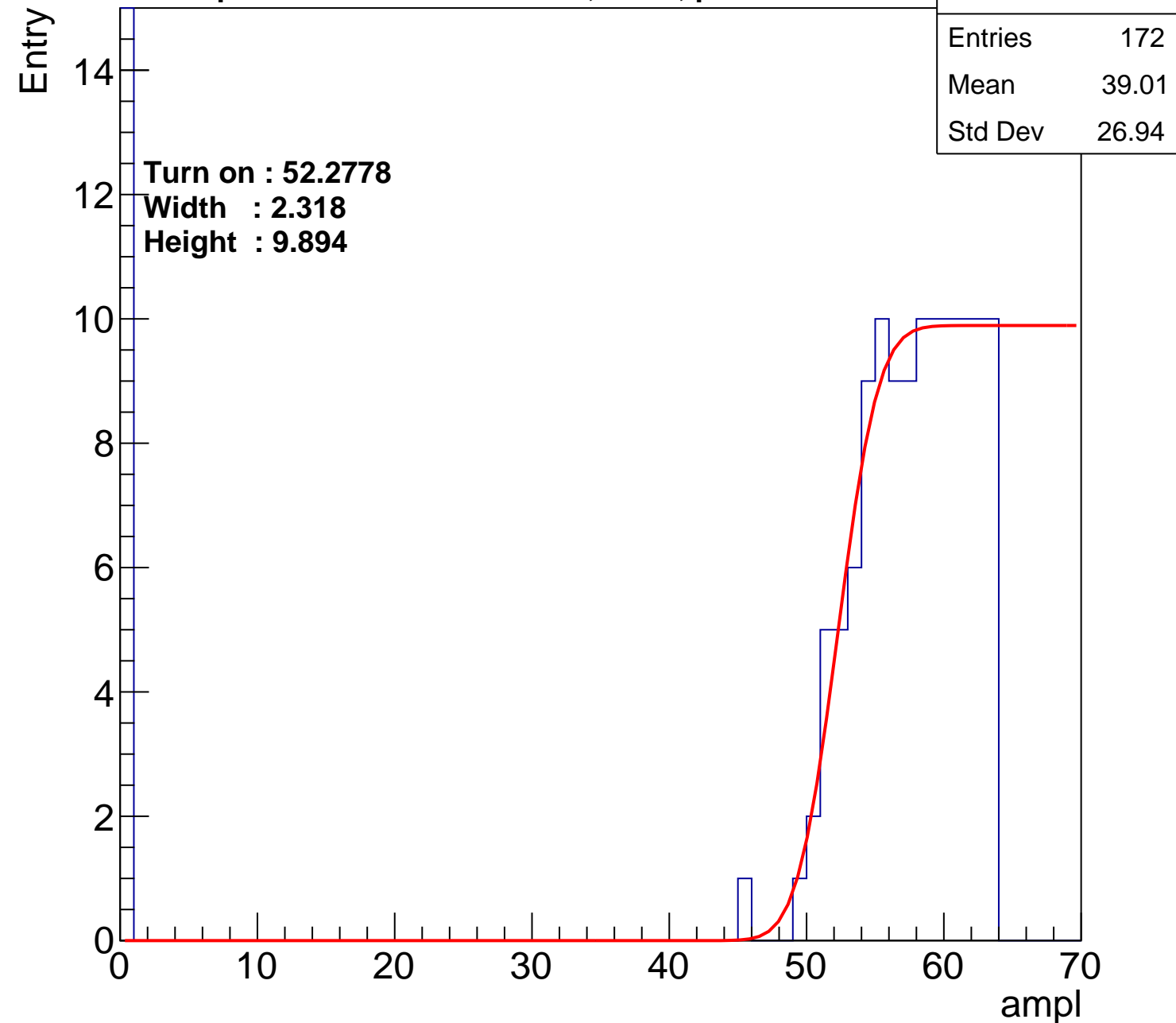
40

50

60

70

ampl



# B1L104S, U3-ch40

calib\_packv5\_033123\_0516.root, FC#4, port A1

Entries	195
Mean	35.08
Std Dev	27.93

**Turn on : 52.0743**

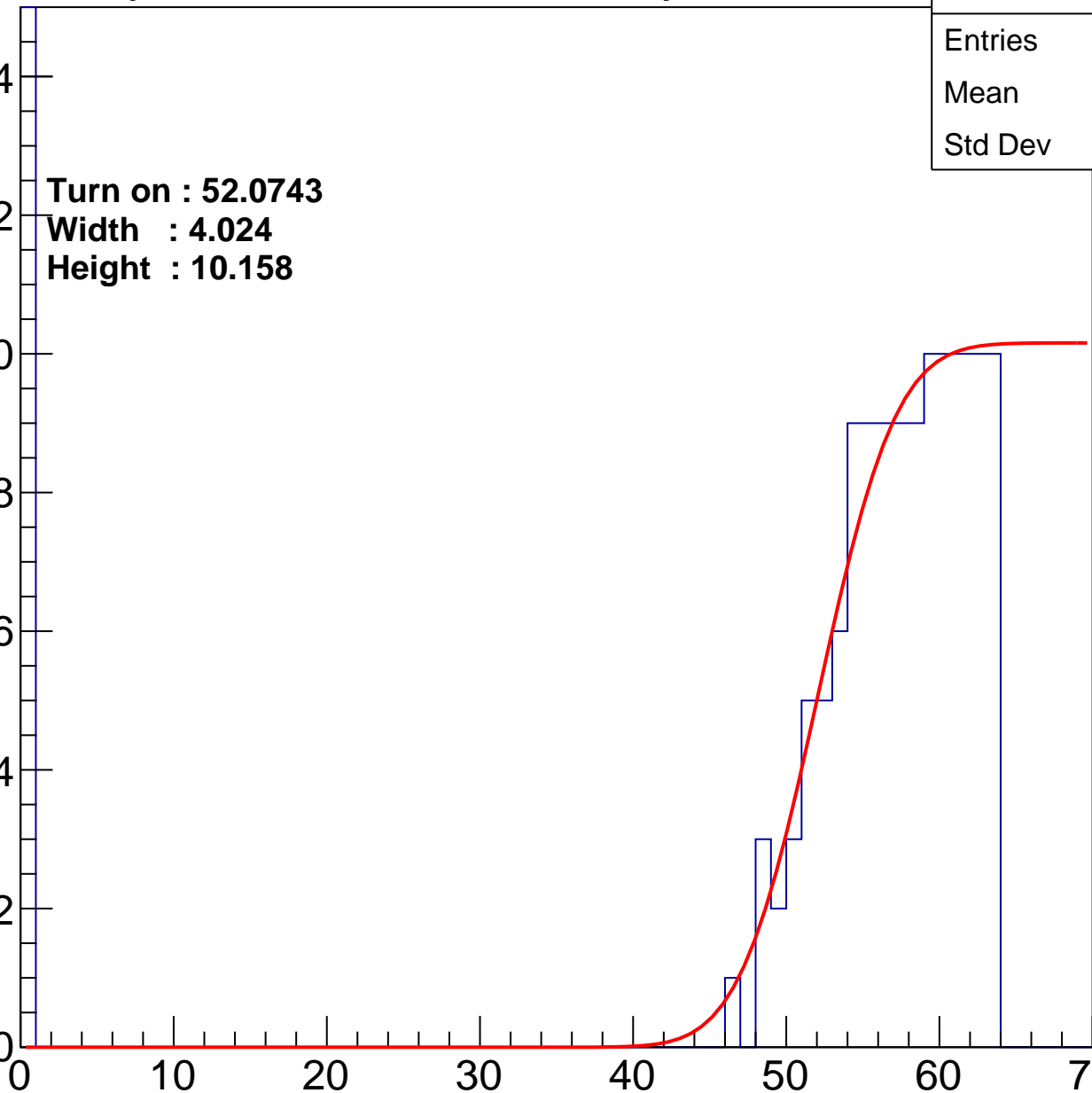
**Width : 4.024**

**Height : 10.158**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L104S, U3-ch41

calib\_packv5\_033123\_0516.root, FC#4, port A1

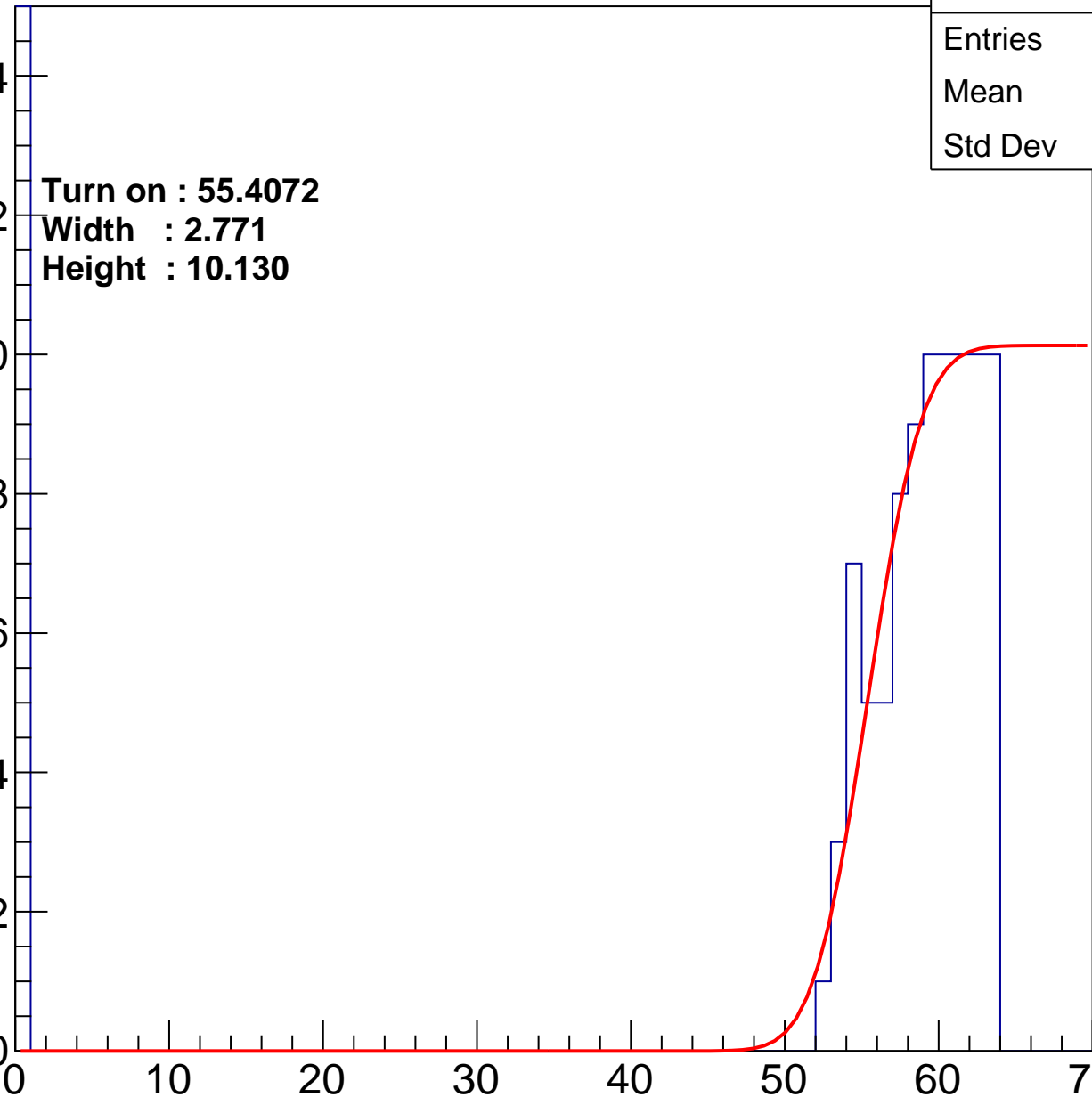
Entry

14  
12  
10  
8  
6  
4  
2  
0

Turn on : 55.4072  
Width : 2.771  
Height : 10.130

Entries	191
Mean	27.08
Std Dev	29.37

ampl



# B1L104S, U3-ch42

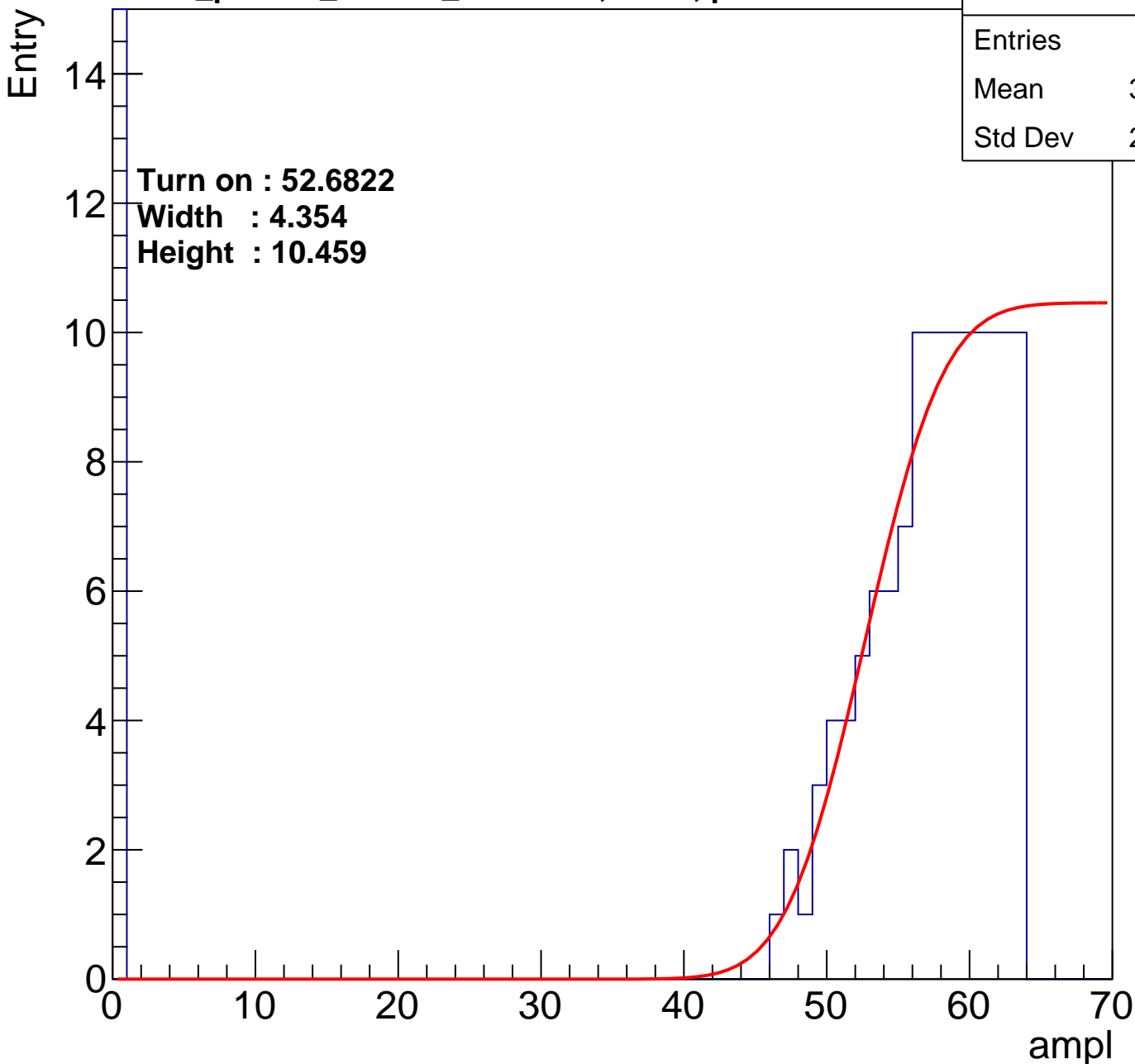
calib\_packv5\_033123\_0516.root, FC#4, port A1

Entries	223
Mean	30.43
Std Dev	28.62

Turn on : 52.6822

Width : 4.354

Height : 10.459



# B1L104S, U3-ch43

calib\_packv5\_033123\_0516.root, FC#4, port A1

Entries	215
Mean	31.87
Std Dev	28.52

Turn on : 52.6096

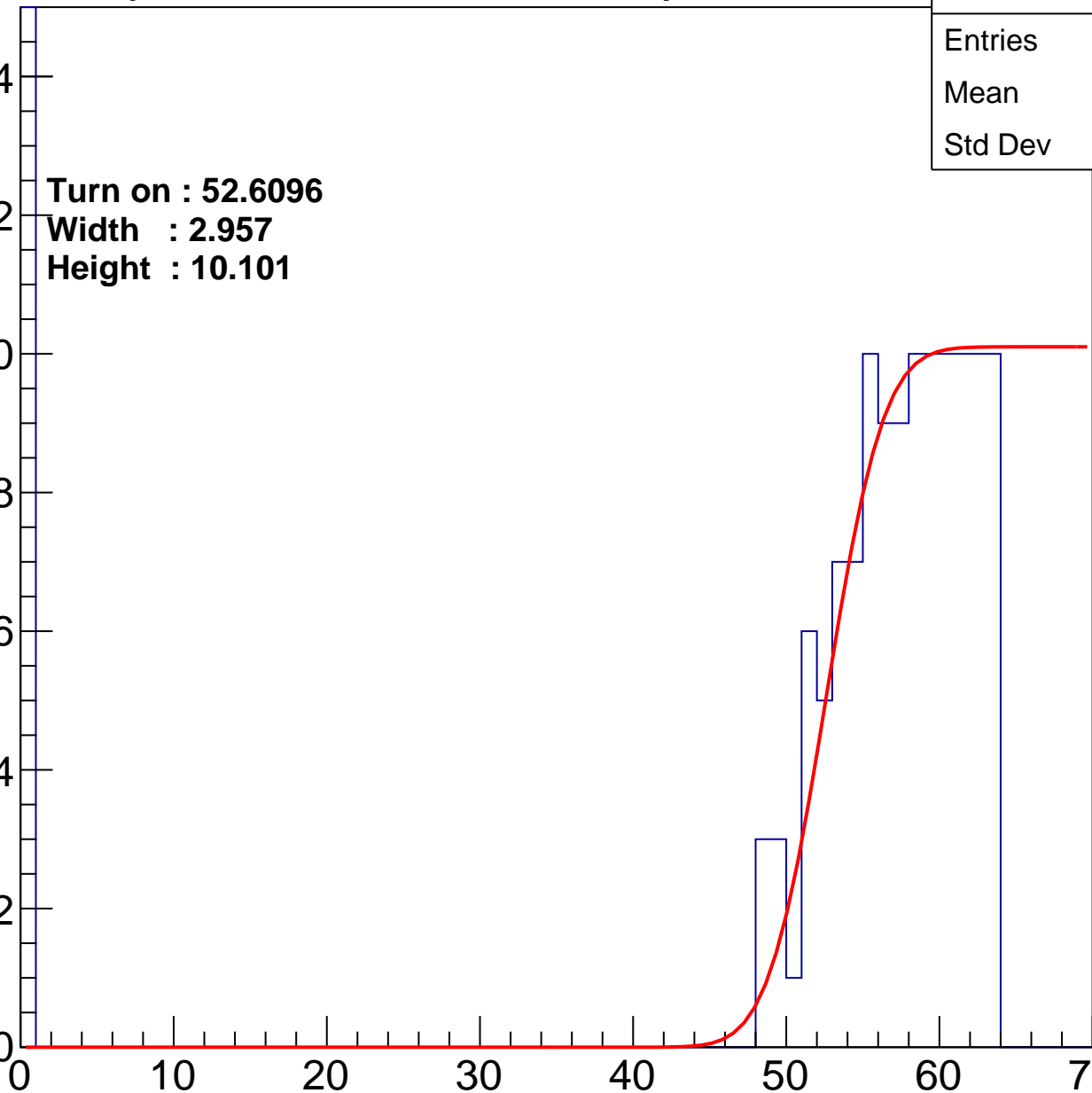
Width : 2.957

Height : 10.101

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L104S, U3-ch44

calib\_packv5\_033123\_0516.root, FC#4, port A1

Entries	208
Mean	32.31
Std Dev	28.41

**Turn on : 53.2473**

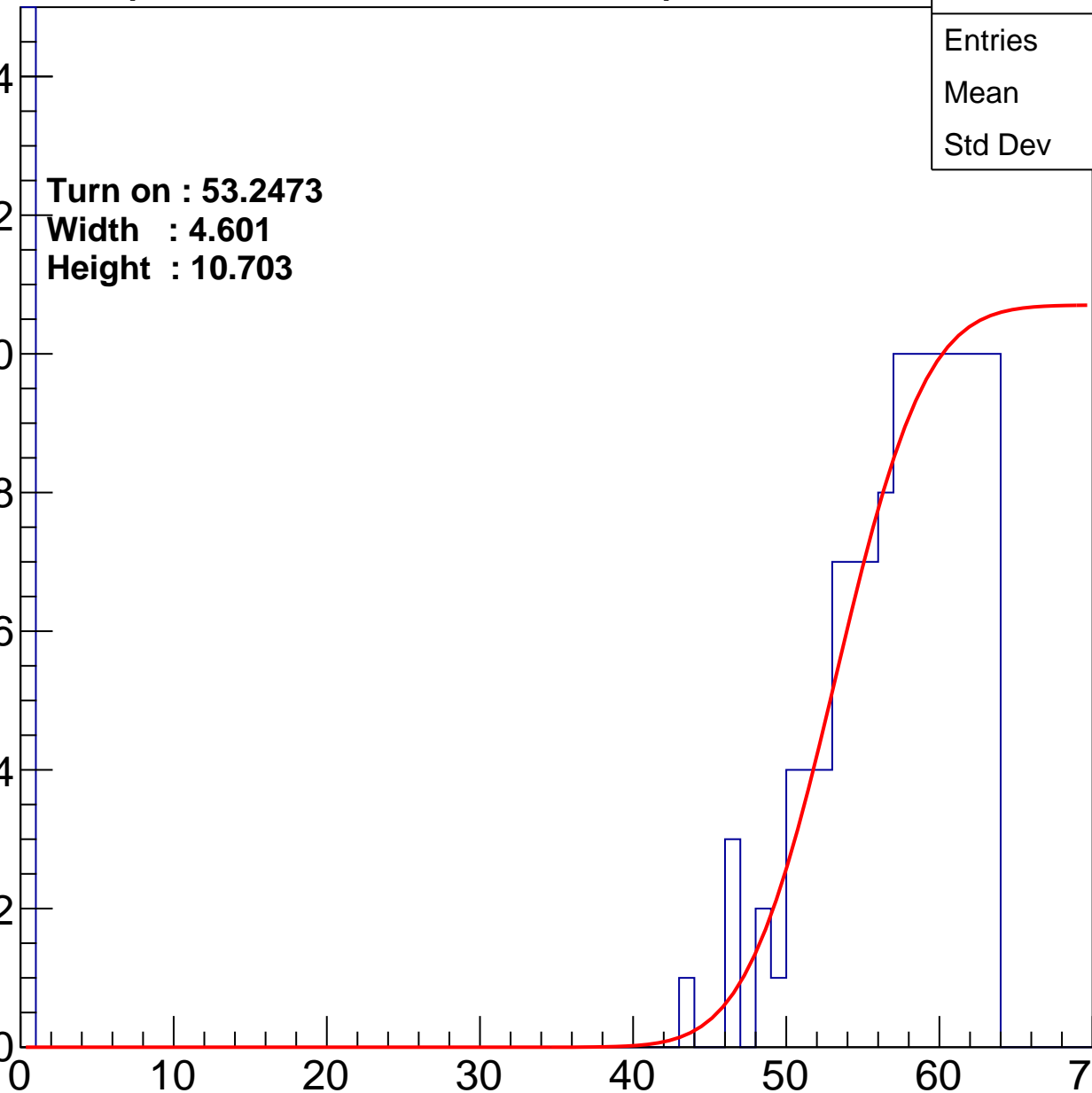
**Width : 4.601**

**Height : 10.703**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L104S, U3-ch45

calib\_packv5\_033123\_0516.root, FC#4, port A1

Entries	211
Mean	32
Std Dev	28.56

Turn on : 52.0152

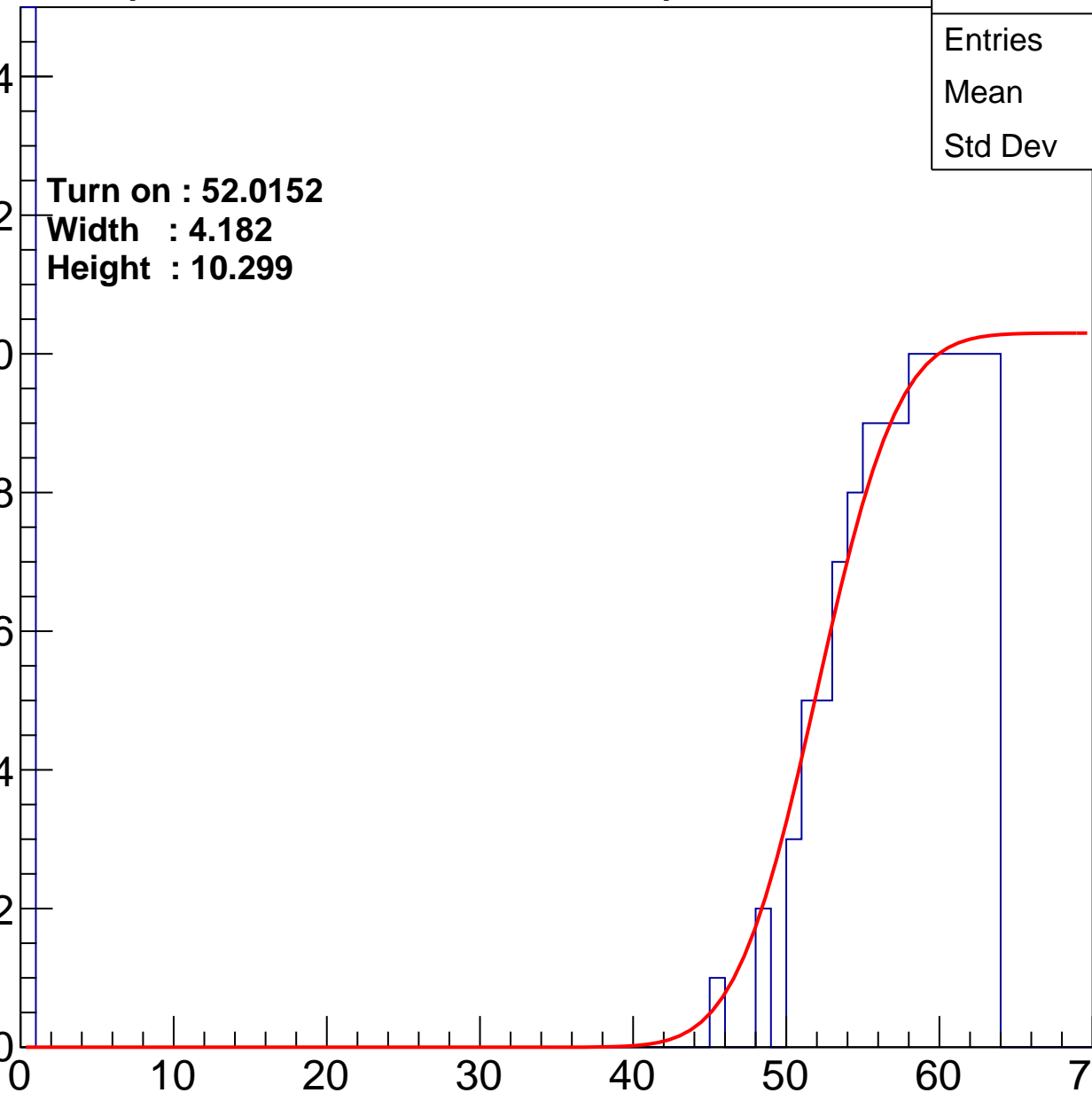
Width : 4.182

Height : 10.299

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L104S, U3-ch46

calib\_packv5\_033123\_0516.root, FC#4, port A1

Entries	236
Mean	31.11
Std Dev	28.29

**Turn on : 51.5873**

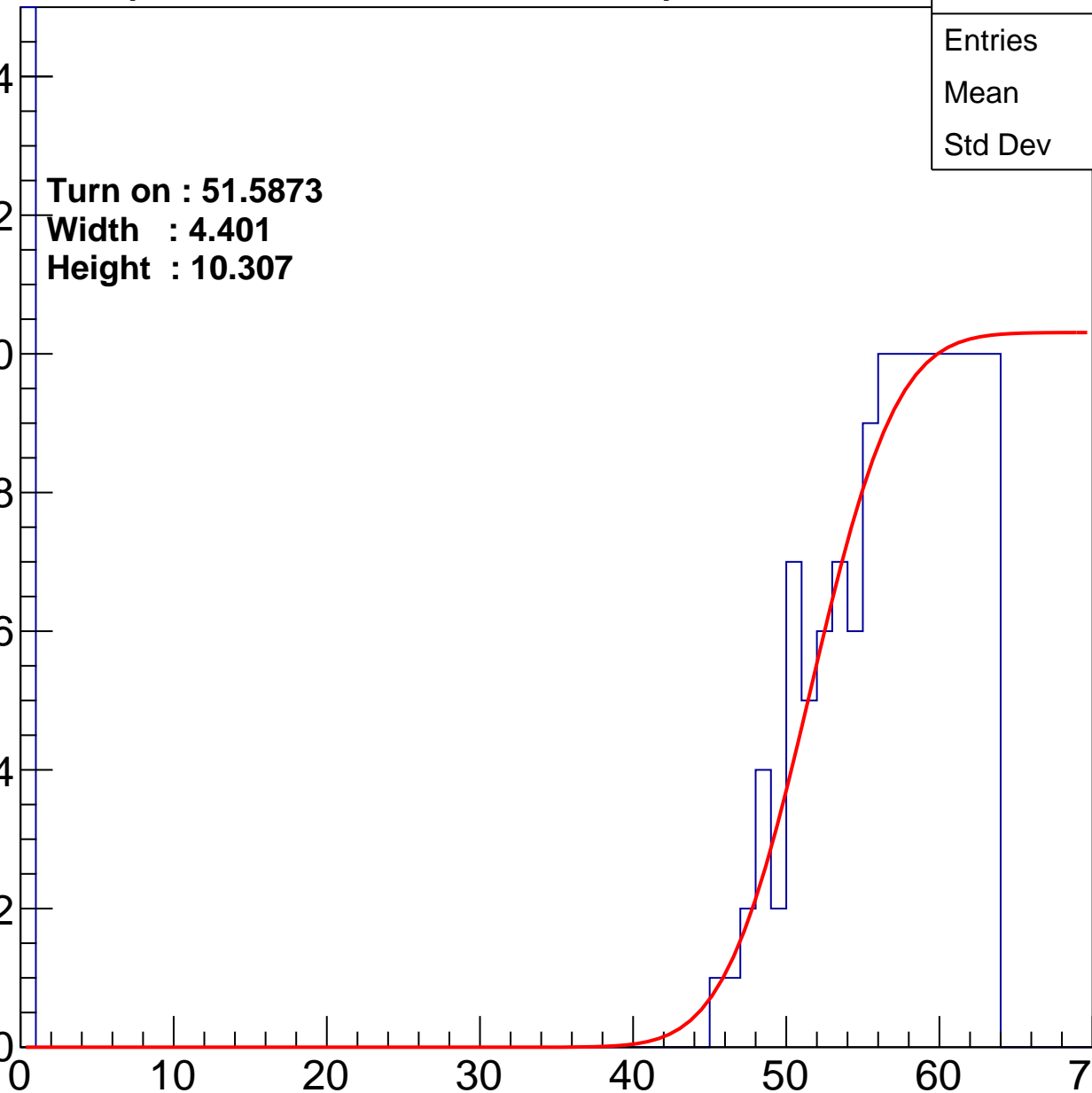
**Width : 4.401**

**Height : 10.307**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L104S, U3-ch47

calib\_packv5\_033123\_0516.root, FC#4, port A1

Entries	229
Mean	29.39
Std Dev	28.67

Turn on : 52.8881

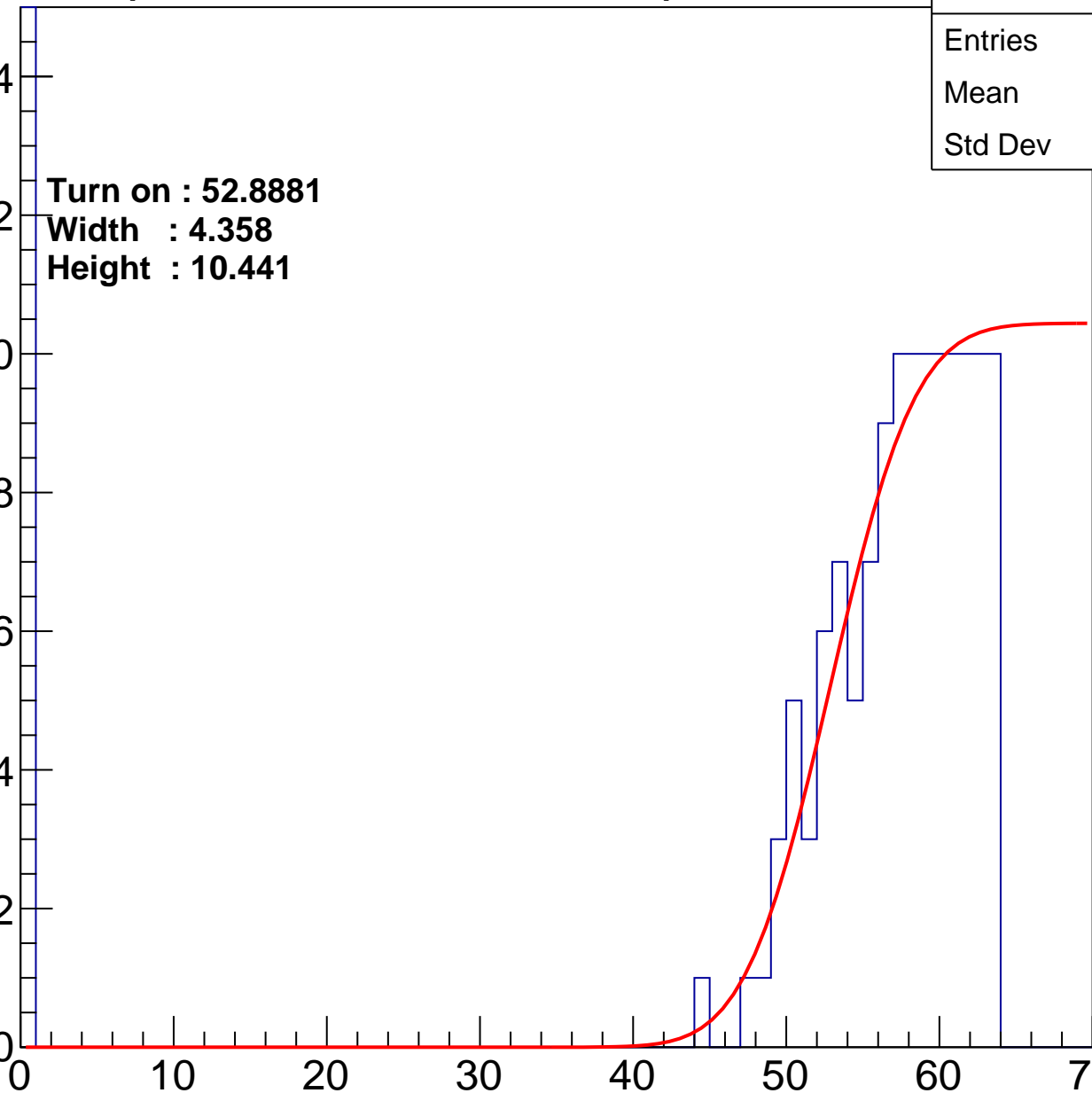
Width : 4.358

Height : 10.441

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L104S, U3-ch48

calib\_packv5\_033123\_0516.root, FC#4, port A1

Entries	227
Mean	28.28
Std Dev	28.8

**Turn on : 53.2175**

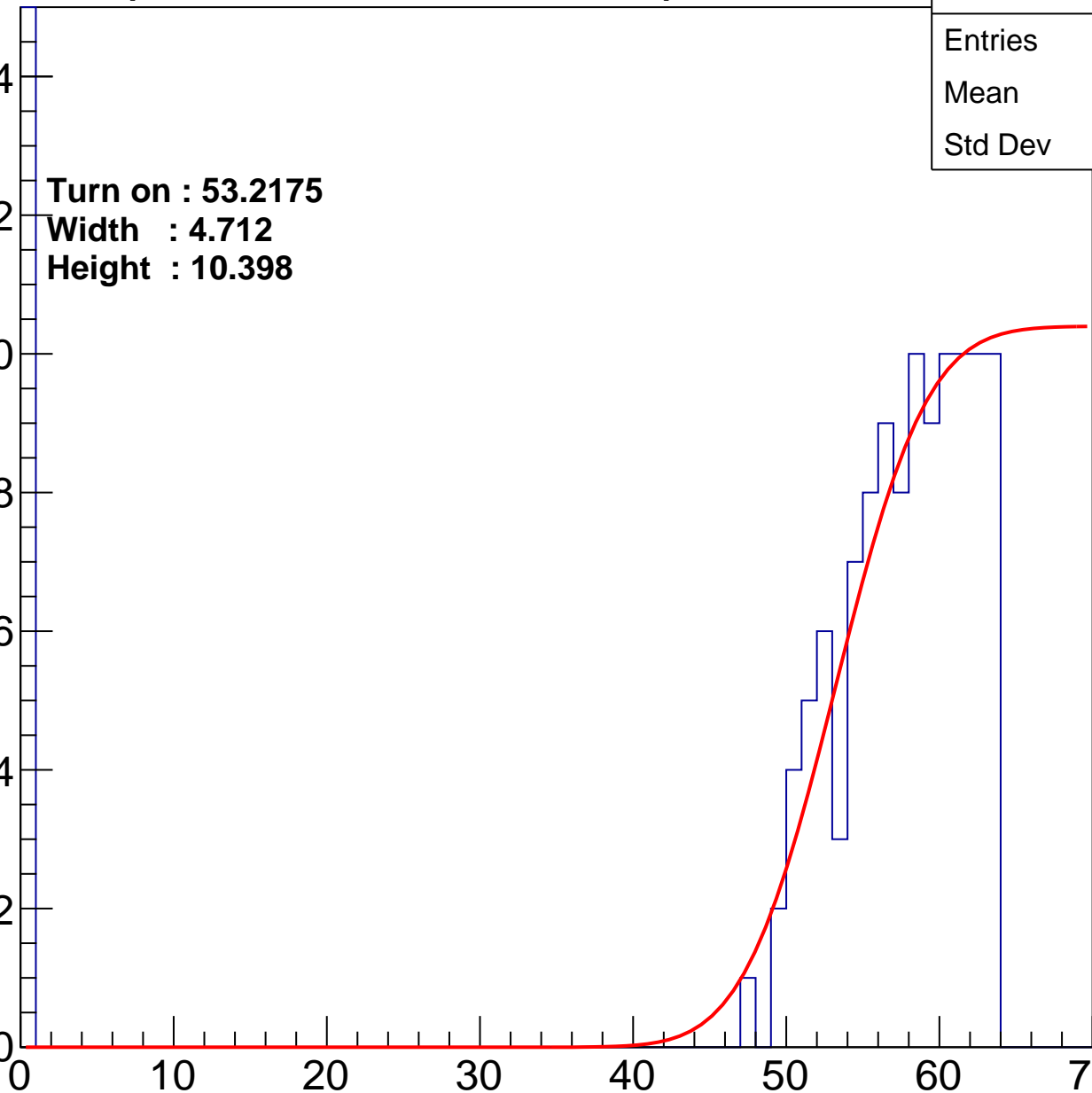
**Width : 4.712**

**Height : 10.398**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L104S, U3-ch49

calib\_packv5\_033123\_0516.root, FC#4, port A1

Entries	190
Mean	33.28
Std Dev	28.53

Turn on : 52.6526

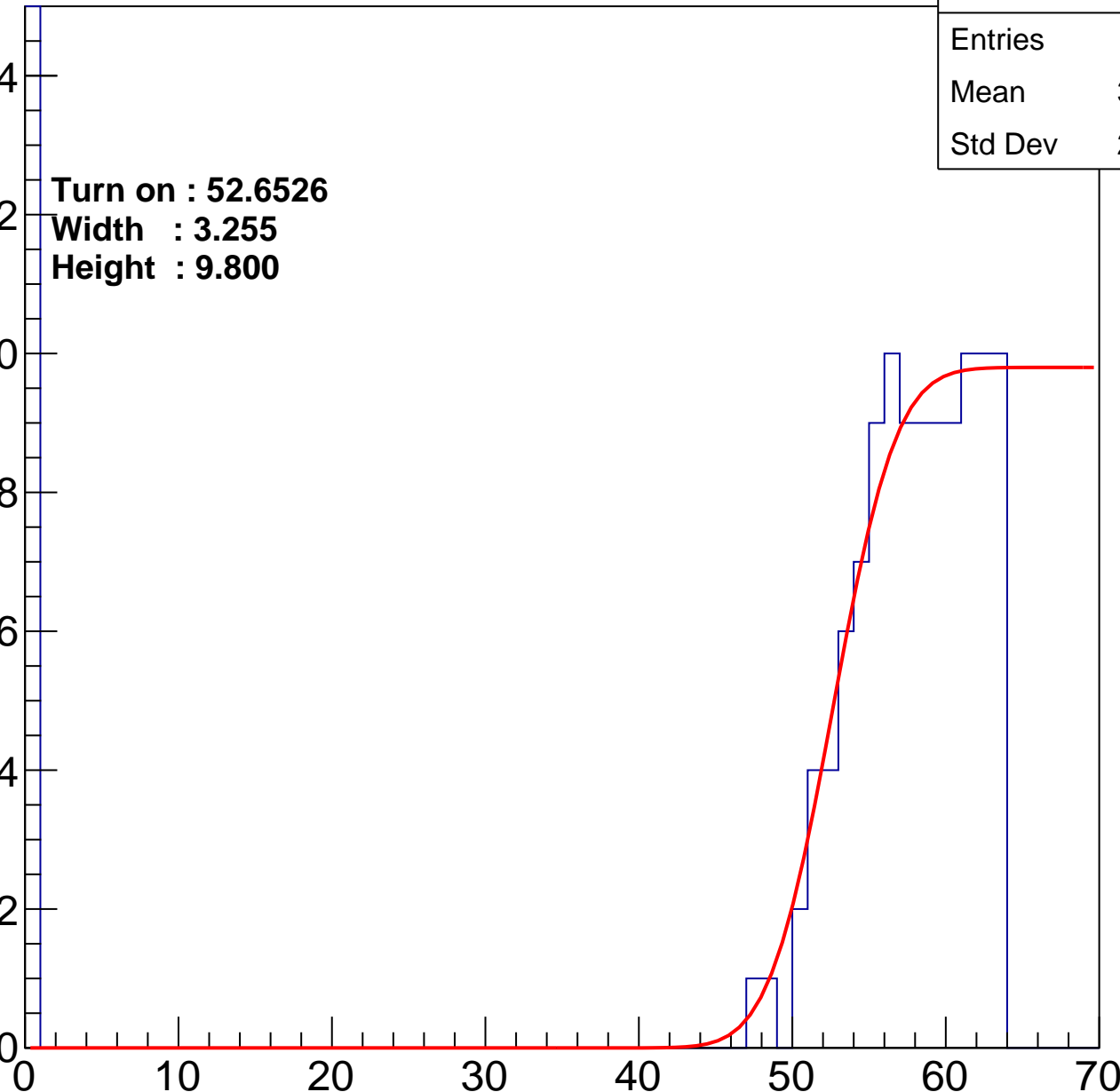
Width : 3.255

Height : 9.800

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L104S, U3-ch50

calib\_packv5\_033123\_0516.root, FC#4, port A1

Entries	217
Mean	29.58
Std Dev	28.79

**Turn on : 54.7846**

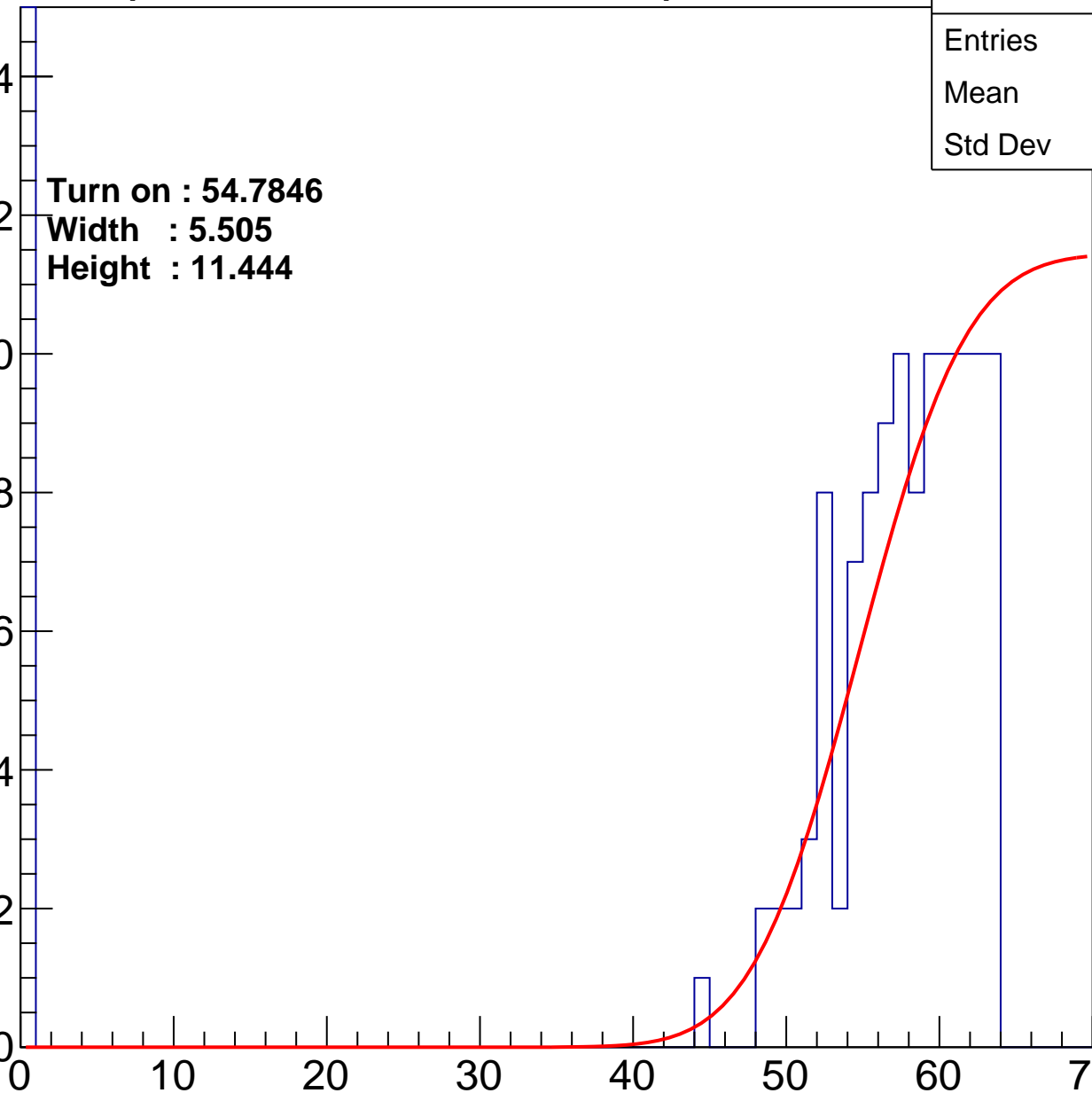
**Width : 5.505**

**Height : 11.444**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L104S, U3-ch51

calib\_packv5\_033123\_0516.root, FC#4, port A1

Entries	205
Mean	28.01
Std Dev	29.1

**Turn on : 55.0693**

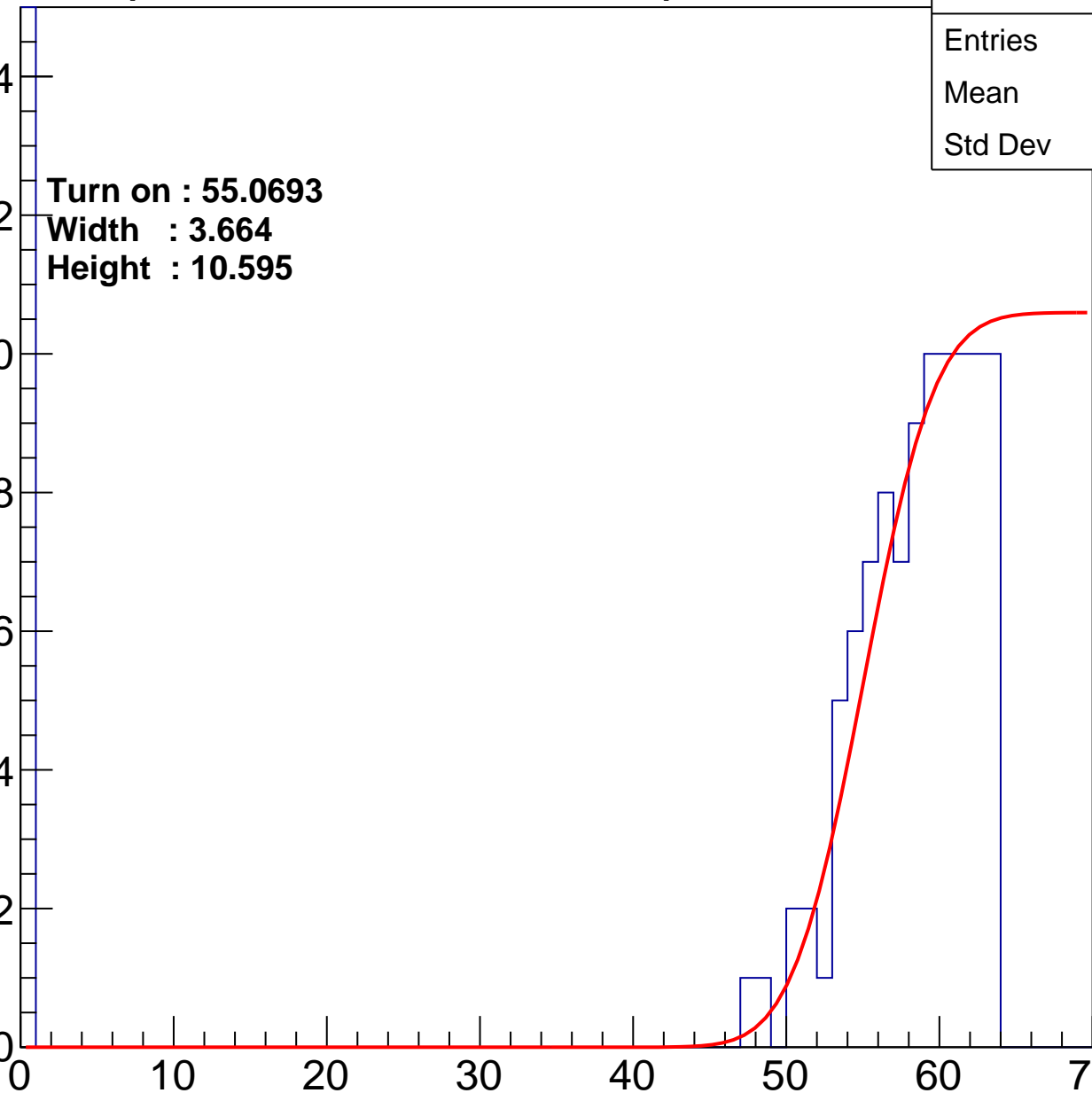
**Width : 3.664**

**Height : 10.595**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L104S, U3-ch52

calib\_packv5\_033123\_0516.root, FC#4, port A1

Entries	192
Mean	31.27
Std Dev	28.91

Turn on : 54.8101

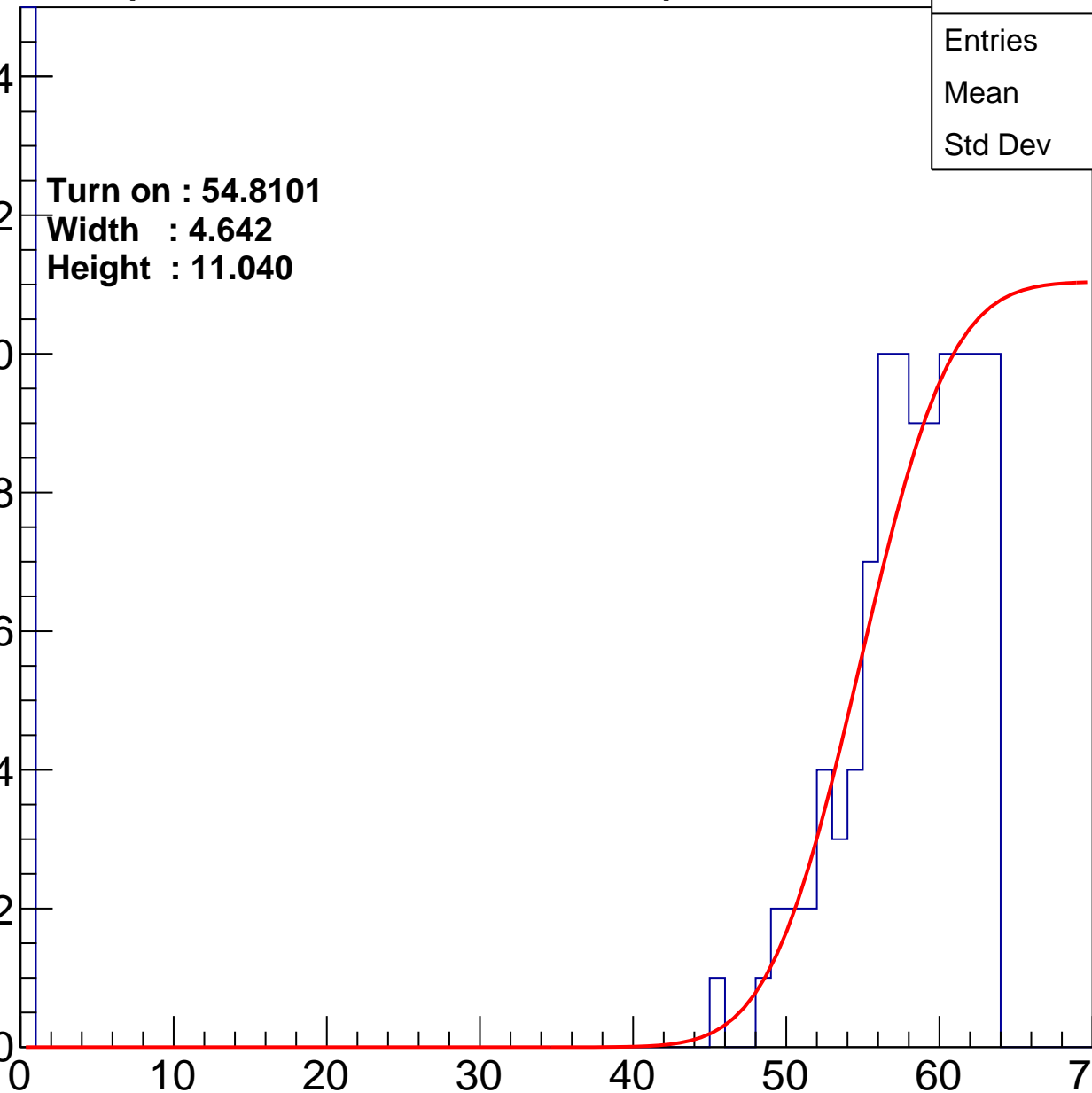
Width : 4.642

Height : 11.040

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L104S, U3-ch53

calib\_packv5\_033123\_0516.root, FC#4, port A1

Entries	194
Mean	30.71
Std Dev	28.98

Turn on : 54.3054

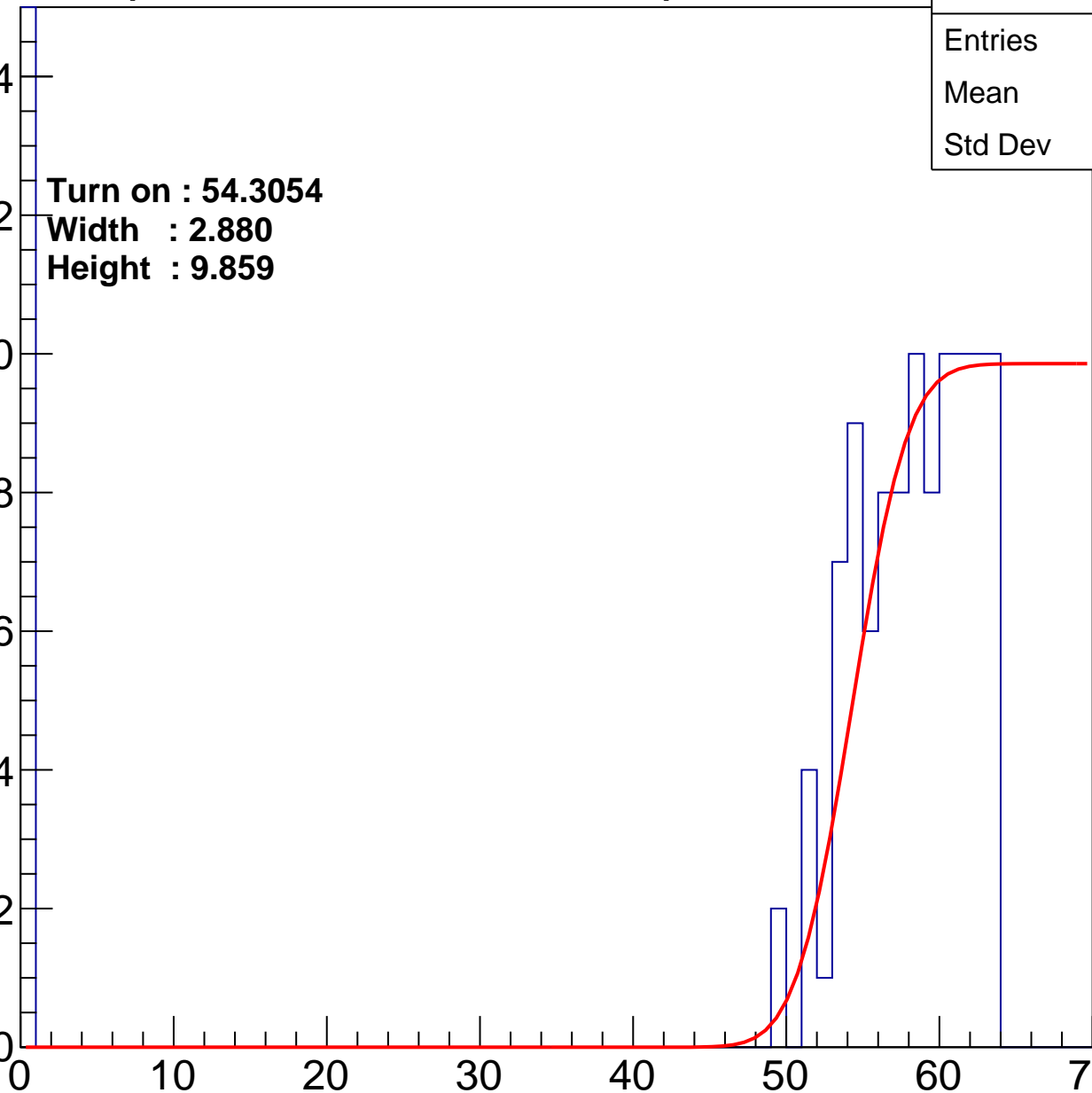
Width : 2.880

Height : 9.859

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L104S, U3-ch54

calib\_packv5\_033123\_0516.root, FC#4, port A1

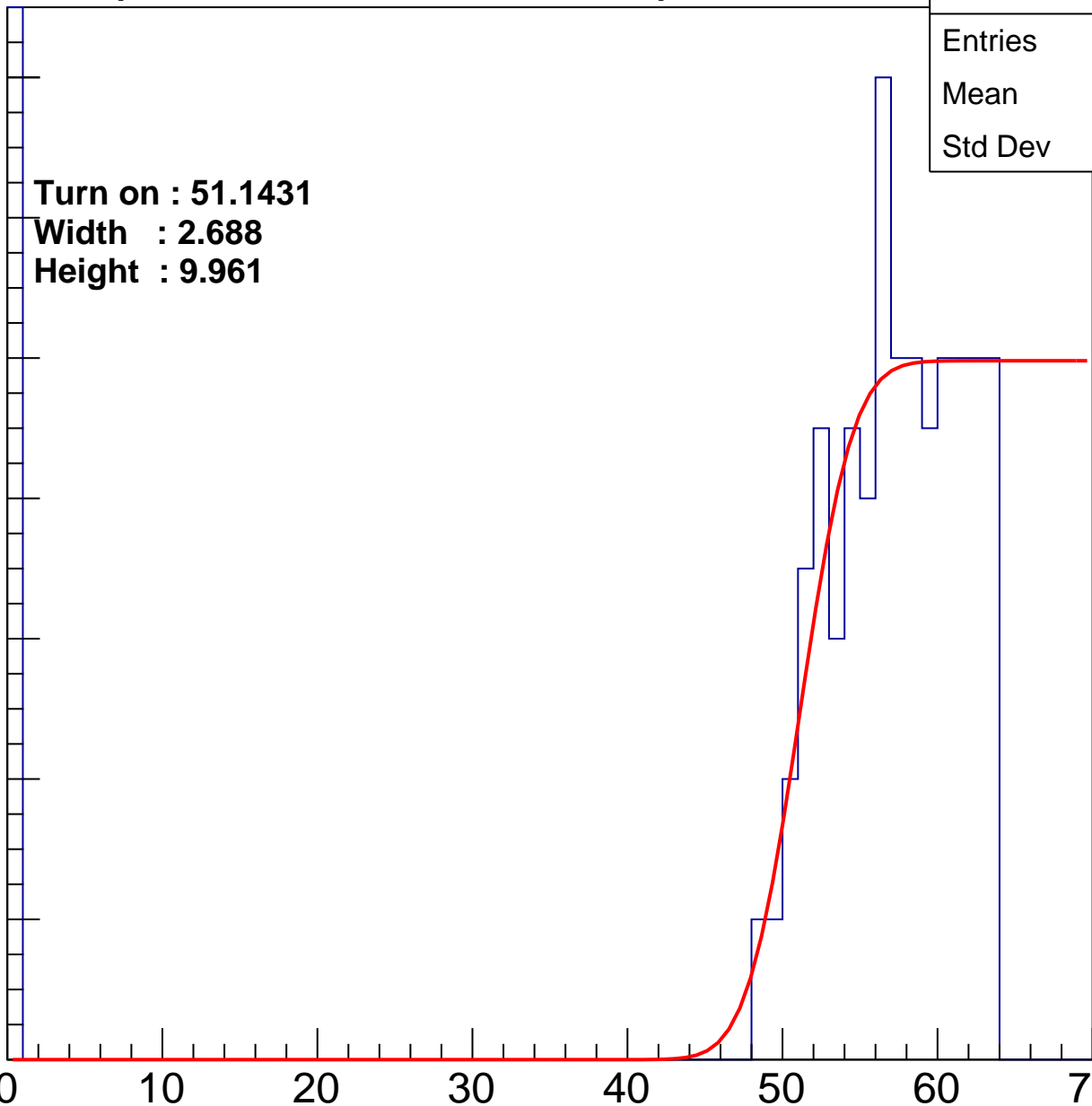
Entry

14  
12  
10  
8  
6  
4  
2  
0

Turn on : 51.1431  
Width : 2.688  
Height : 9.961

Entries	239
Mean	30.91
Std Dev	28.46

ampl





# B1L104S, U3-ch55

calib\_packv5\_033123\_0516.root, FC#4, port A1

Entries	208
Mean	33.74
Std Dev	28.21

**Turn on : 51.8423**

**Width : 2.593**

**Height : 9.938**

Entry

14

12

10

8

6

4

2

0

0

10

20

30

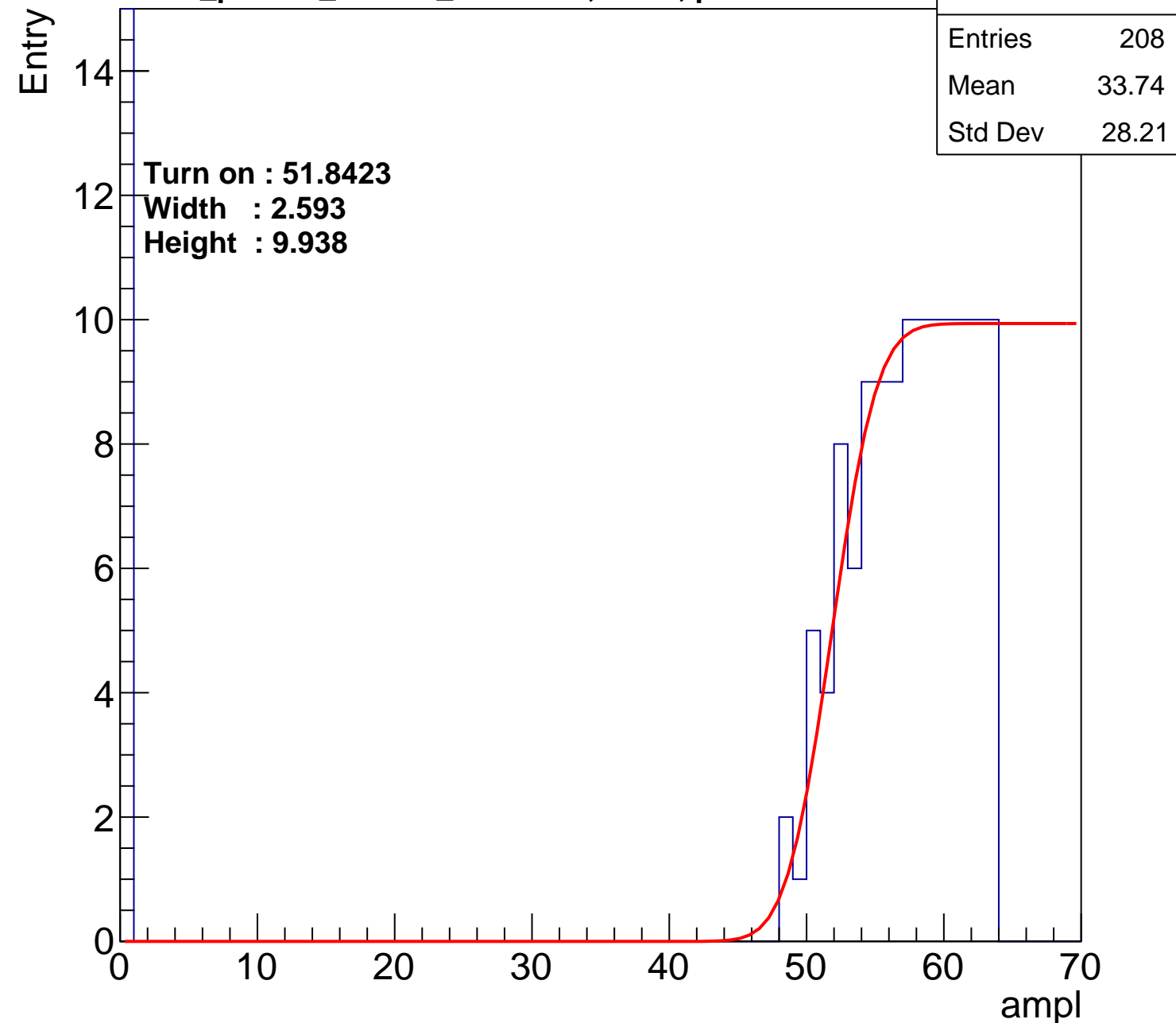
40

50

60

70

ampl



# B1L104S, U3-ch56

calib\_packv5\_033123\_0516.root, FC#4, port A1

Entries	228
Mean	31.54
Std Dev	28.33

Turn on : 52.0792

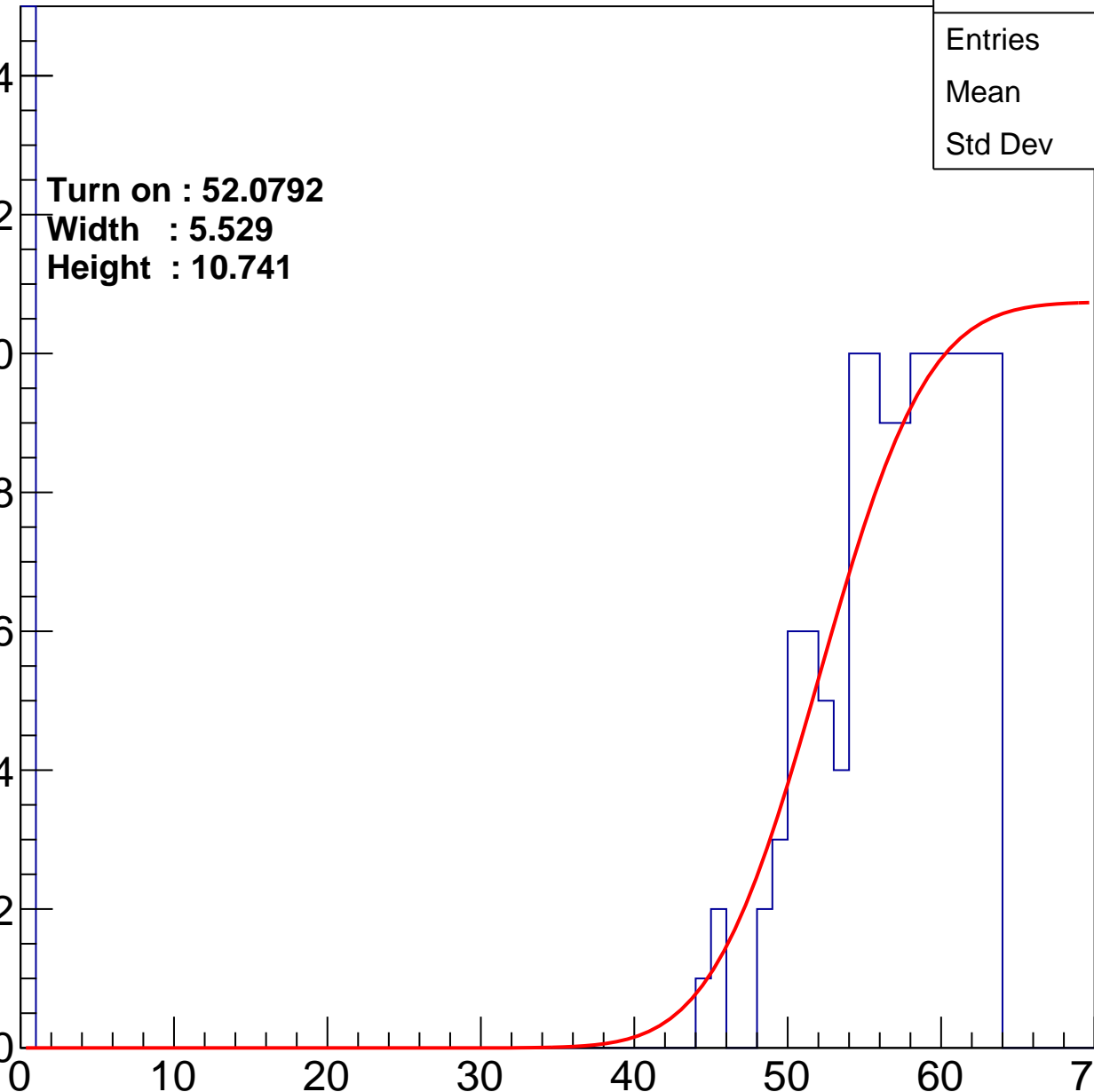
Width : 5.529

Height : 10.741

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L104S, U3-ch57

calib\_packv5\_033123\_0516.root, FC#4, port A1

Entries	238
Mean	30.95
Std Dev	28.39

Turn on : 51.7545

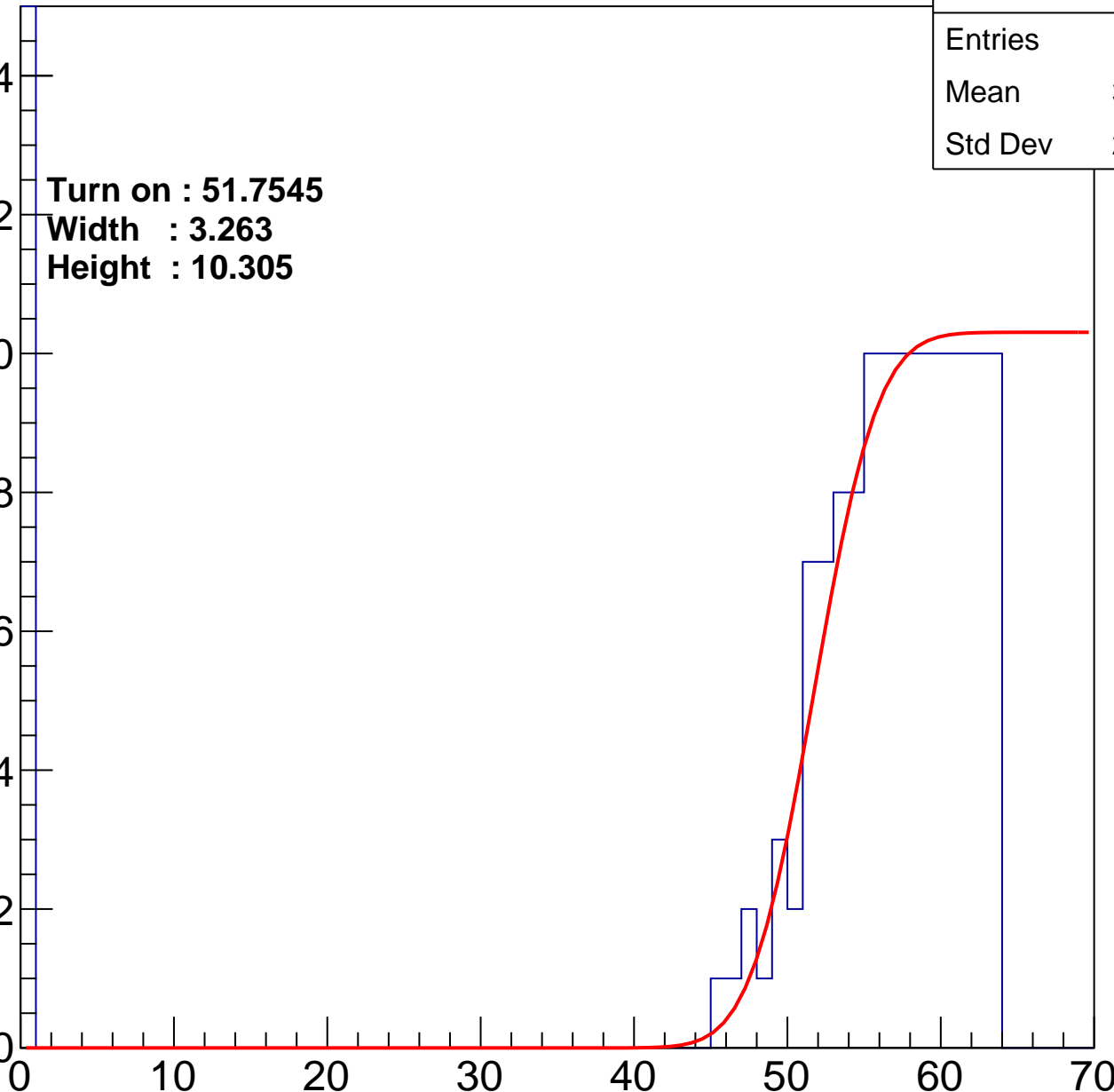
Width : 3.263

Height : 10.305

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L104S, U3-ch58

calib\_packv5\_033123\_0516.root, FC#4, port A1

Entries	222
Mean	31.47
Std Dev	28.41

Turn on : 52.3694

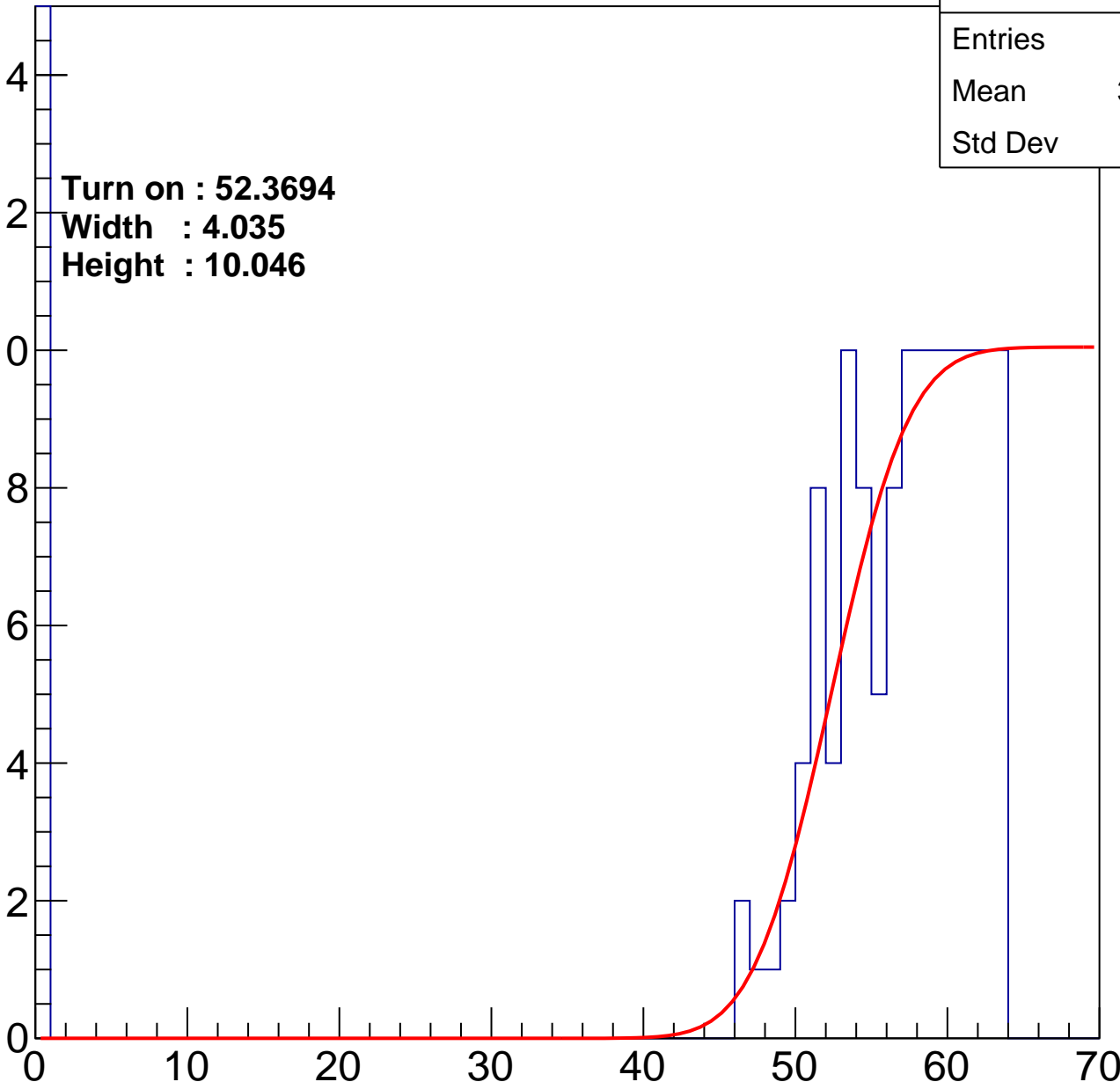
Width : 4.035

Height : 10.046

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L104S, U3-ch59

calib\_packv5\_033123\_0516.root, FC#4, port A1

Entries	210
Mean	31.81
Std Dev	28.53

Turn on : 52.7945

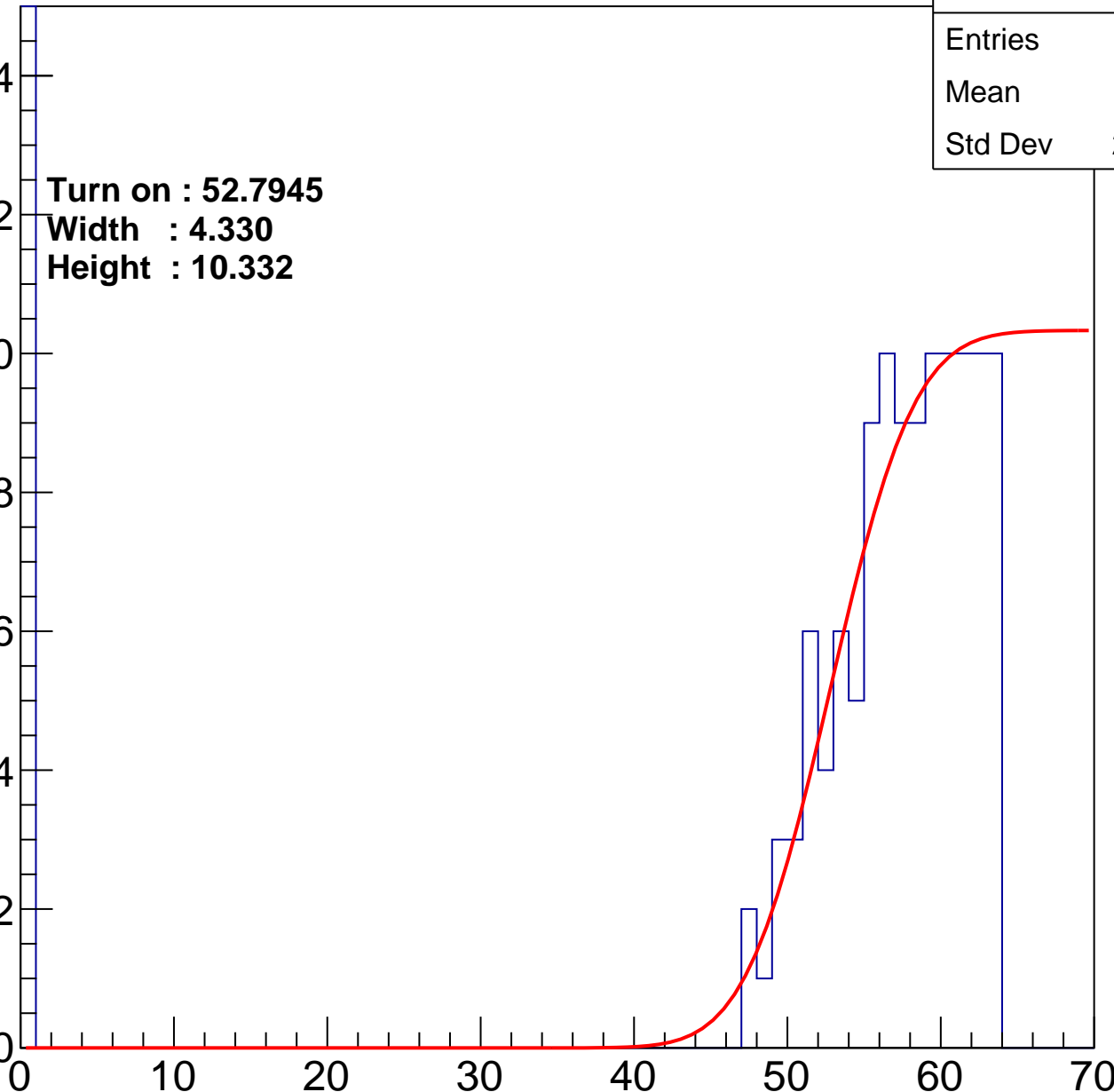
Width : 4.330

Height : 10.332

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L104S, U3-ch60

calib\_packv5\_033123\_0516.root, FC#4, port A1

Entries	220
Mean	32.24
Std Dev	28.3

Turn on : 52.6791

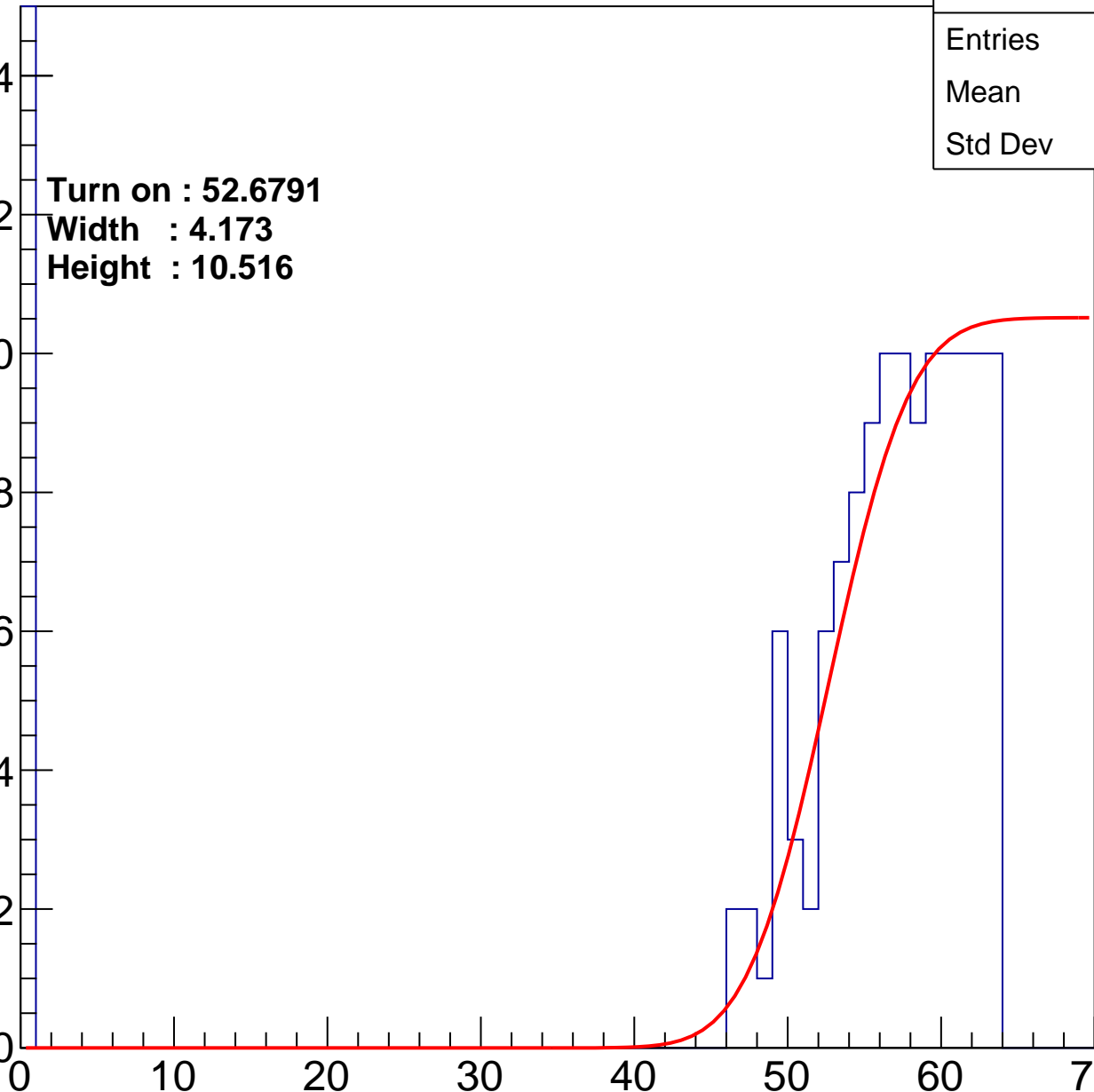
Width : 4.173

Height : 10.516

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L104S, U3-ch61

calib\_packv5\_033123\_0516.root, FC#4, port A1

Entries	235
Mean	29.61
Std Dev	28.65

**Turn on : 52.3829**

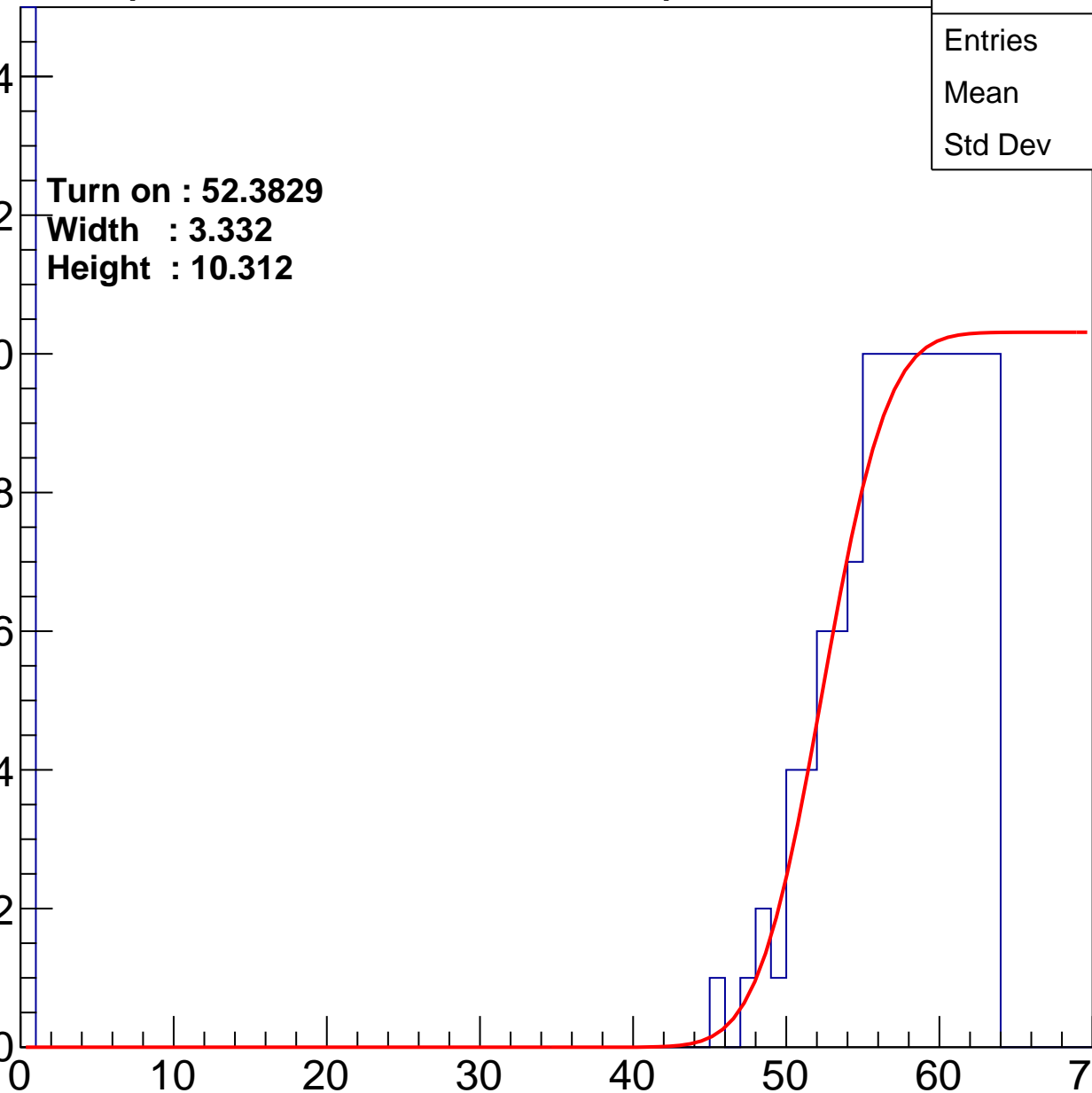
**Width : 3.332**

**Height : 10.312**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L104S, U3-ch62

calib\_packv5\_033123\_0516.root, FC#4, port A1

Entries	213
Mean	31.63
Std Dev	28.55

**Turn on : 53.1157**

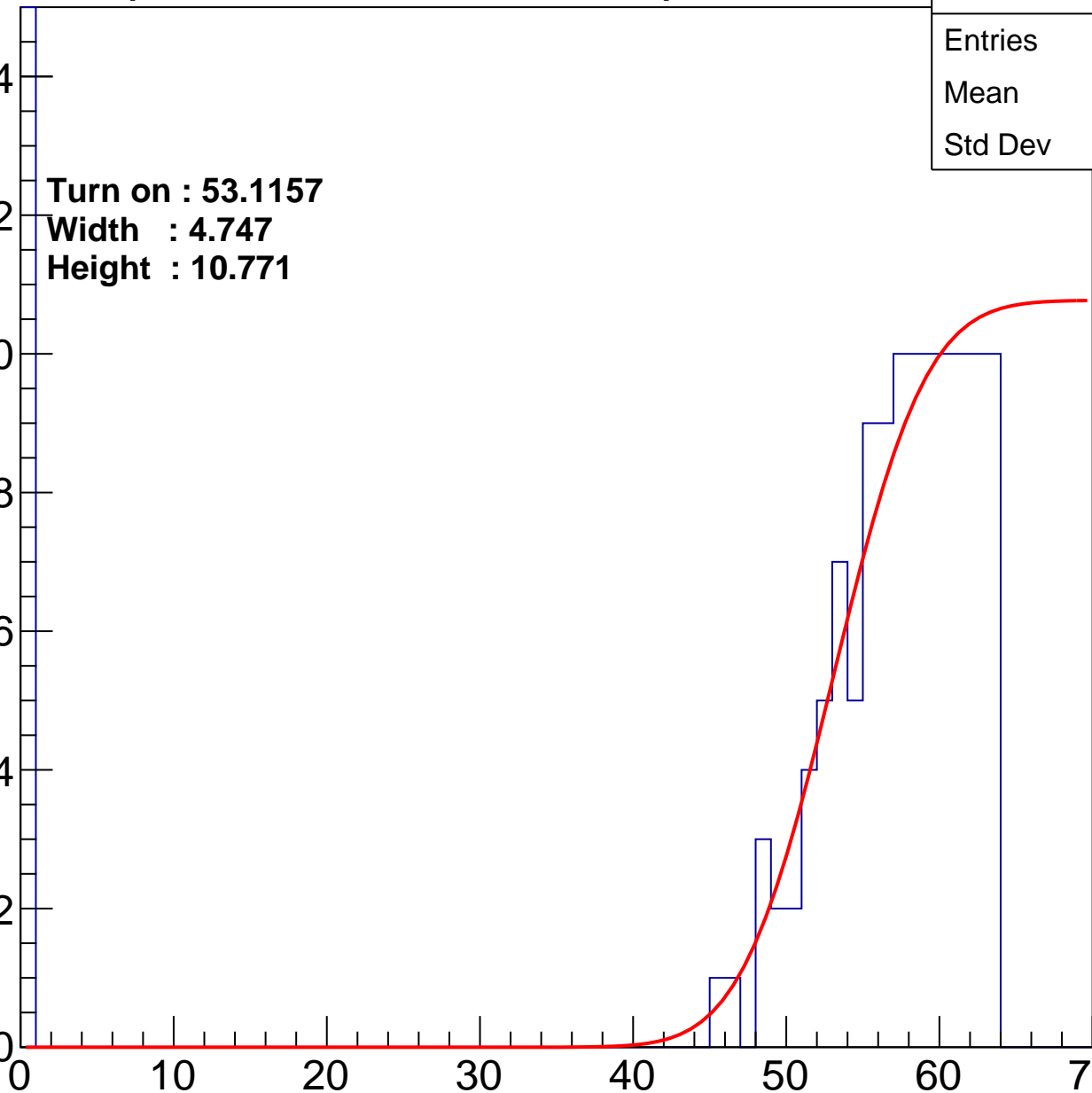
**Width : 4.747**

**Height : 10.771**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L104S, U3-ch63

calib\_packv5\_033123\_0516.root, FC#4, port A1

Entries	209
Mean	35.51
Std Dev	27.61

Turn on : 50.4859

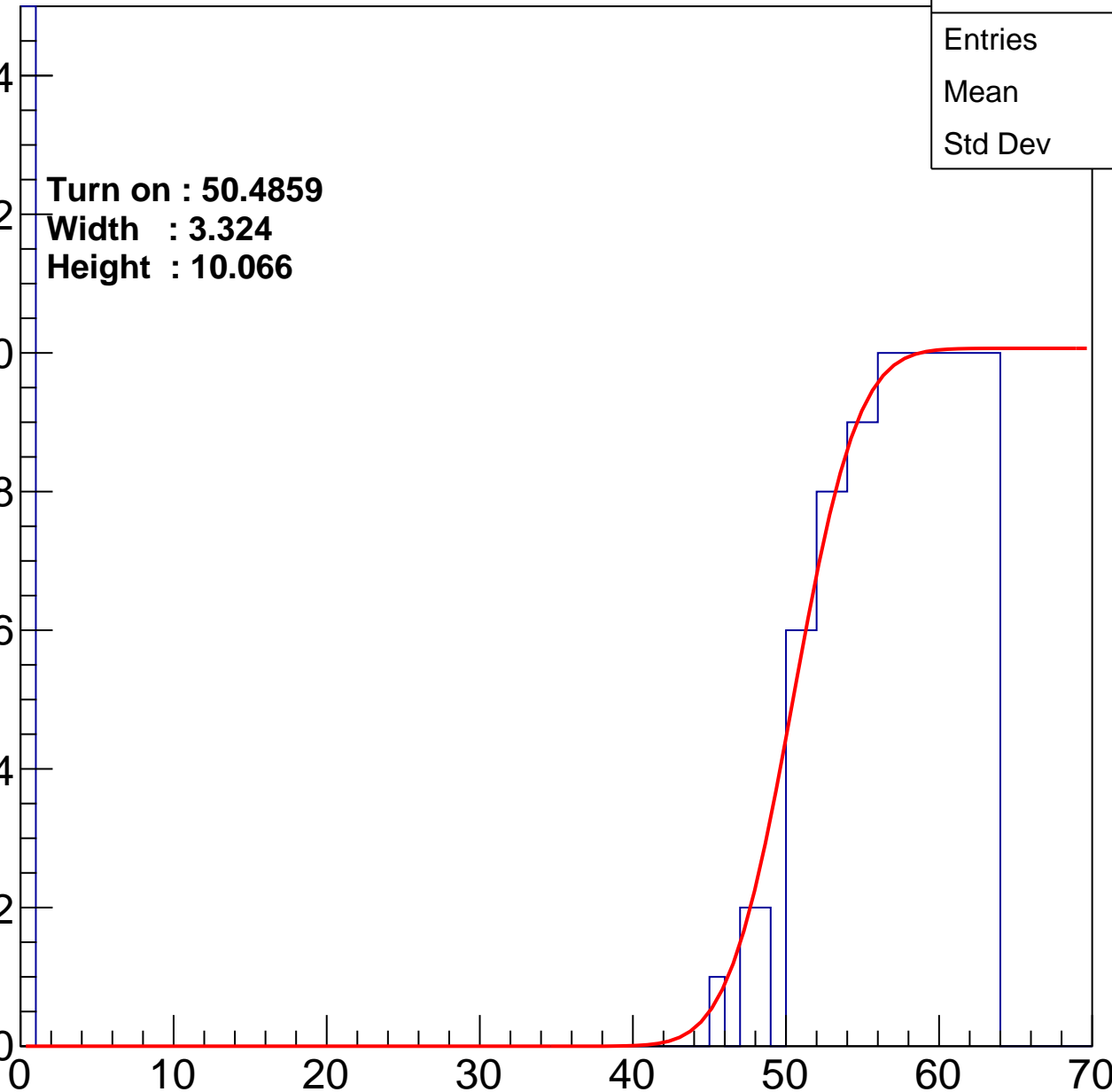
Width : 3.324

Height : 10.066

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L104S, U3-ch64

calib\_packv5\_033123\_0516.root, FC#4, port A1

Entries	220
Mean	30.35
Std Dev	28.64

Turn on : 52.9600

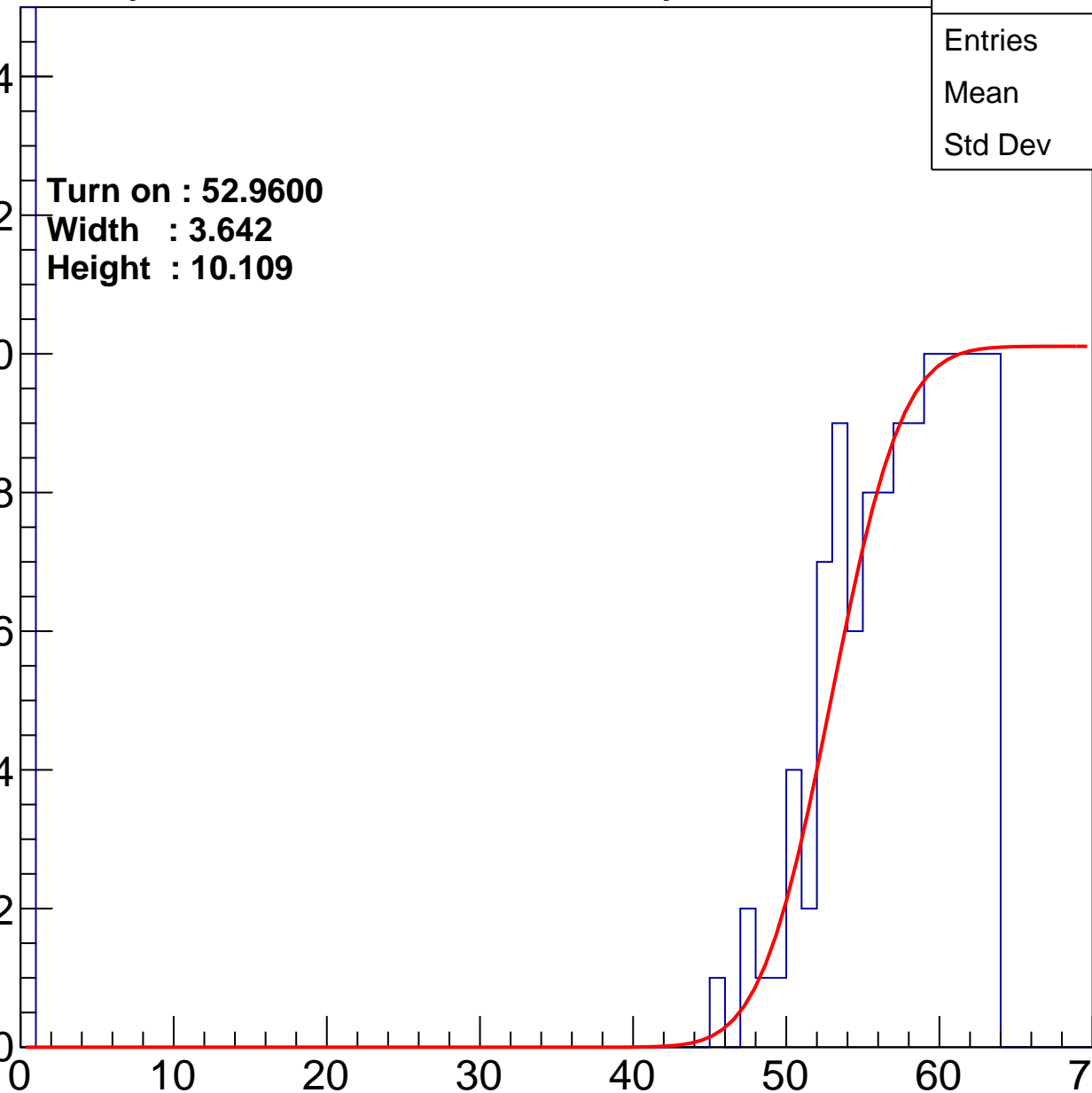
Width : 3.642

Height : 10.109

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L104S, U3-ch65

calib\_packv5\_033123\_0516.root, FC#4, port A1

Entries	189
Mean	27.93
Std Dev	29.37

Turn on : 55.1875

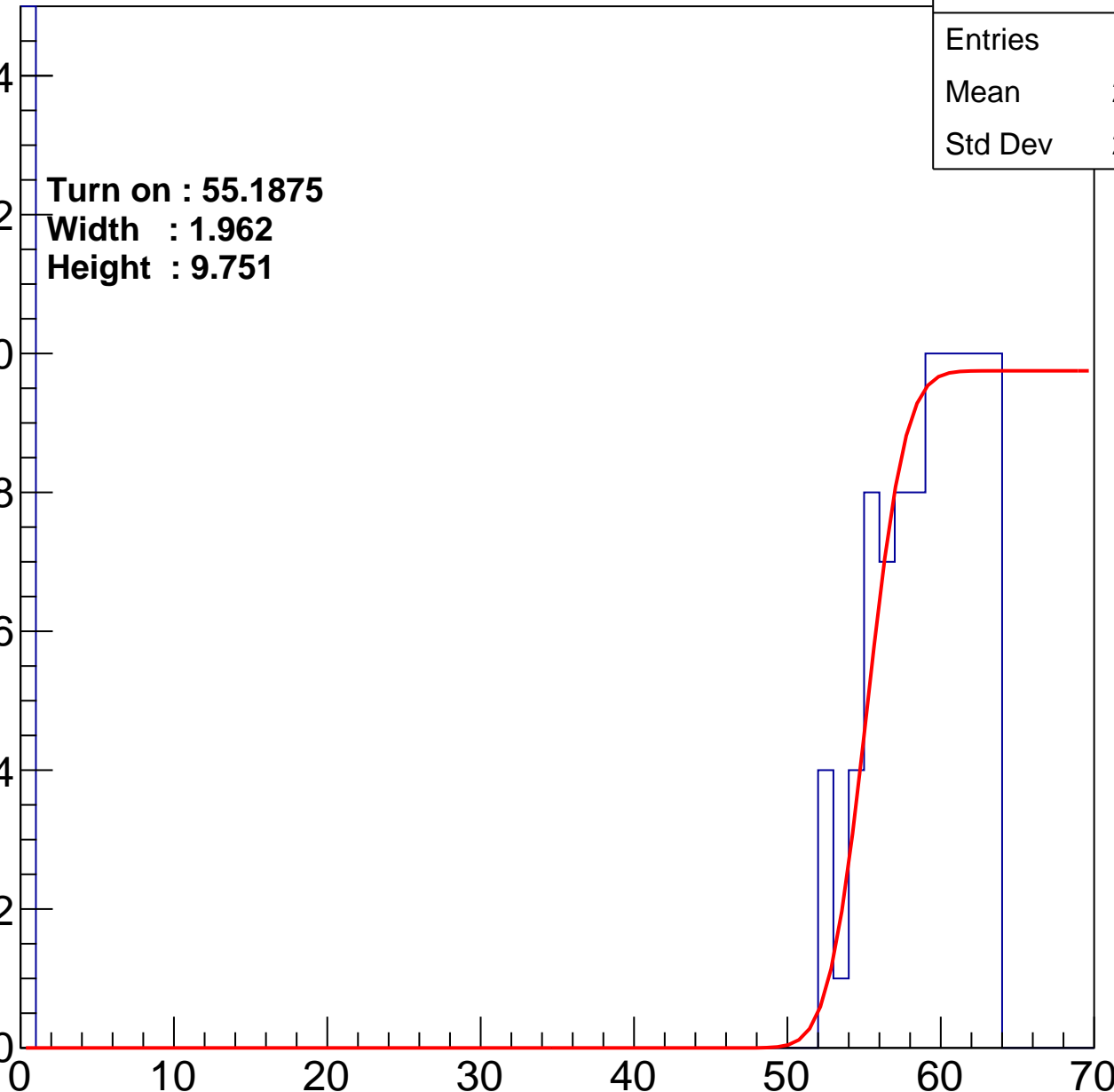
Width : 1.962

Height : 9.751

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L104S, U3-ch66

calib\_packv5\_033123\_0516.root, FC#4, port A1

Entries	202
Mean	29.17
Std Dev	29.02

Turn on : 55.0288

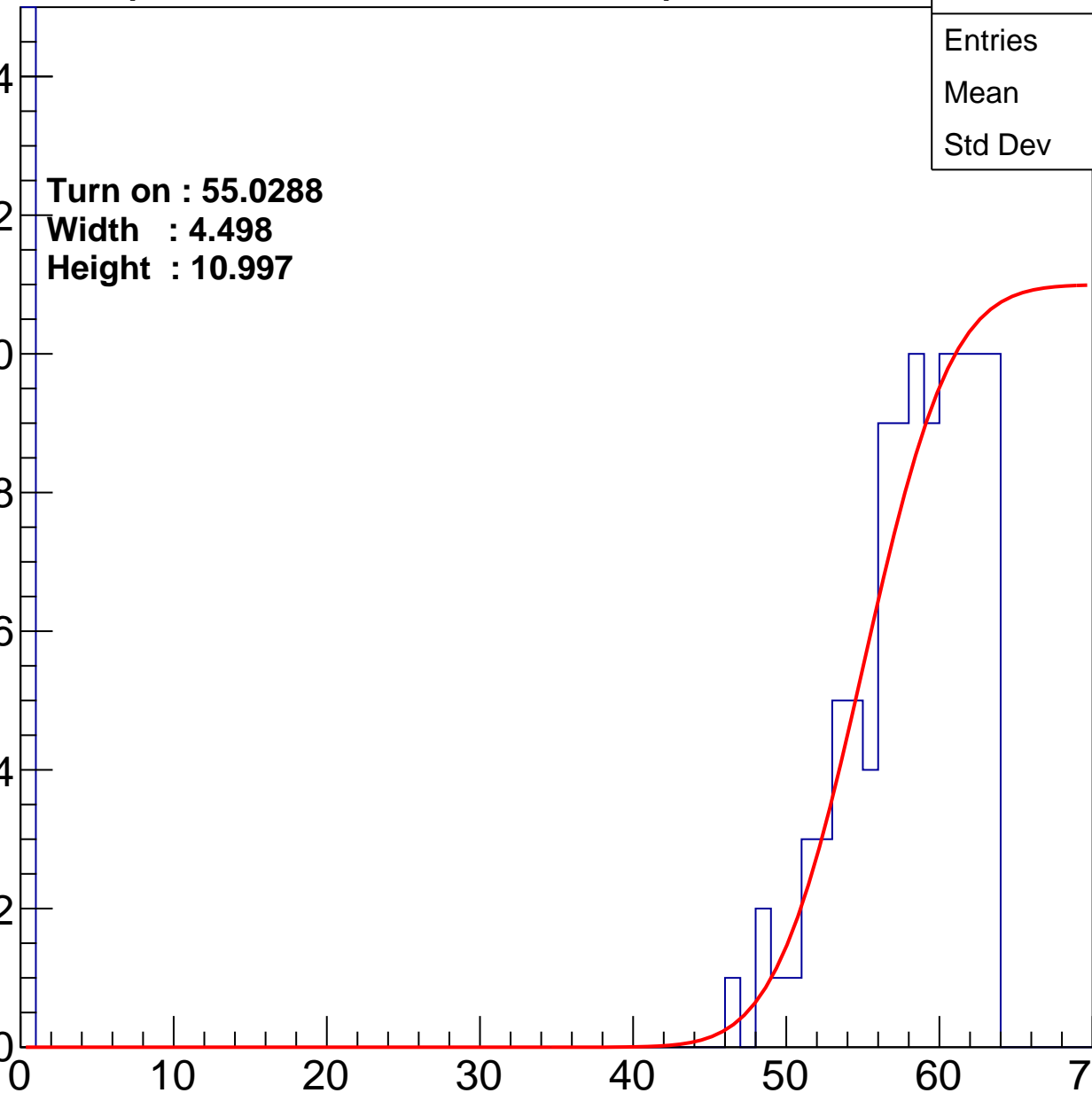
Width : 4.498

Height : 10.997

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L104S, U3-ch67

calib\_packv5\_033123\_0516.root, FC#4, port A1

Entries	168
Mean	31.65
Std Dev	29.22

**Turn on : 55.2194**

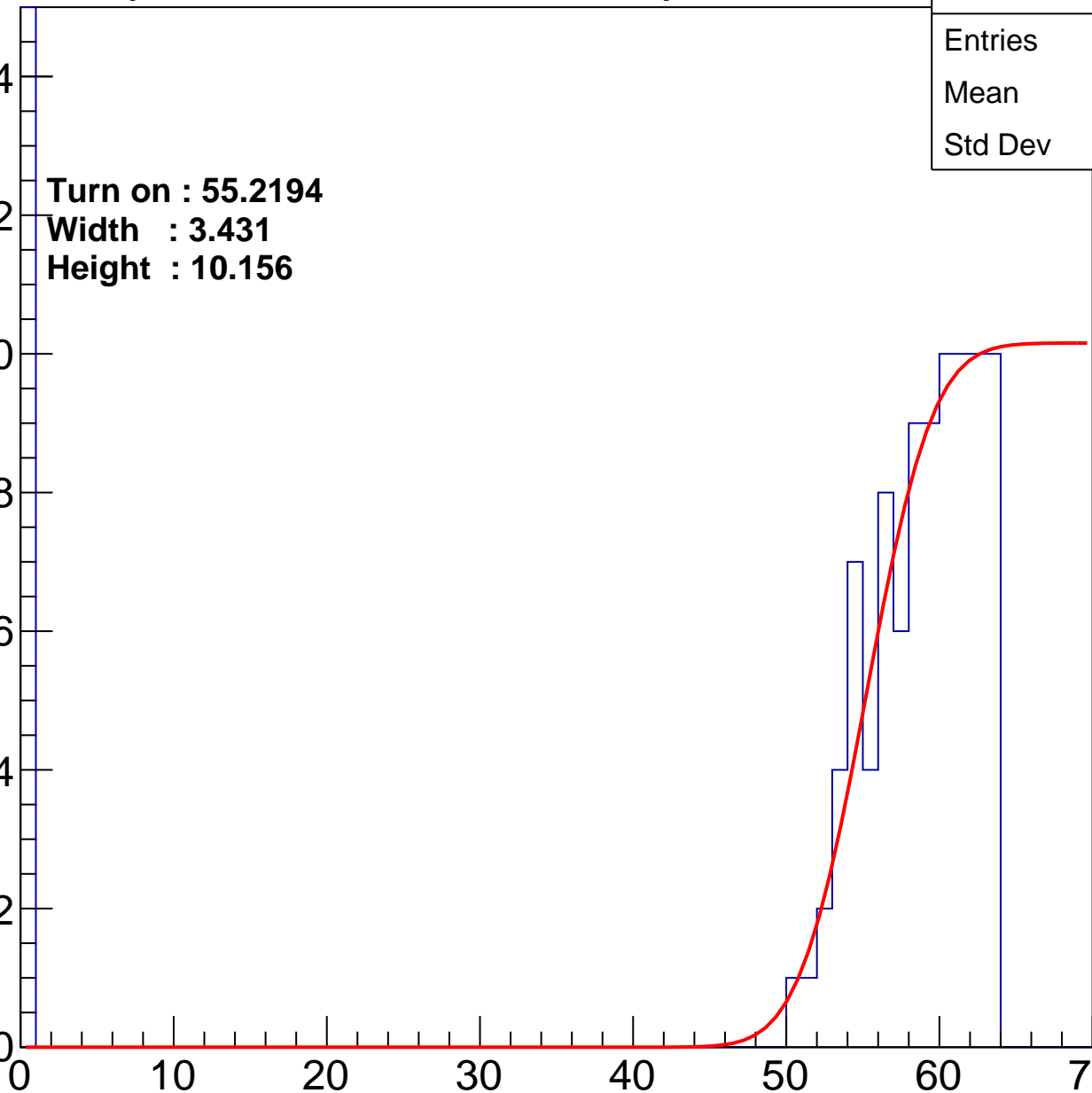
**Width : 3.431**

**Height : 10.156**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L104S, U3-ch68

calib\_packv5\_033123\_0516.root, FC#4, port A1

Entries	222
Mean	31.22
Std Dev	28.45

Turn on : 52.6152

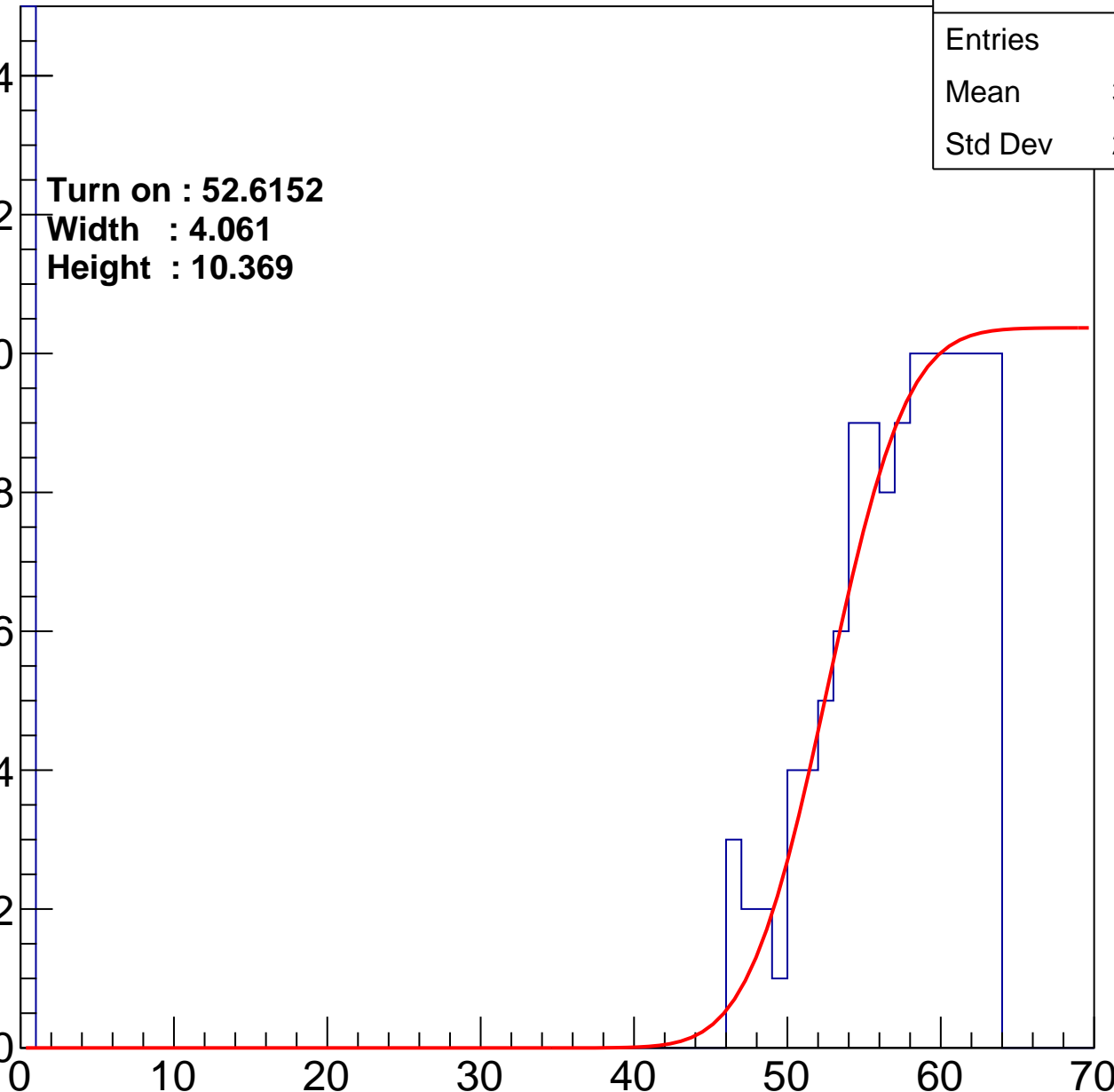
Width : 4.061

Height : 10.369

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L104S, U3-ch69

calib\_packv5\_033123\_0516.root, FC#4, port A1

Entries	183
Mean	29.49
Std Dev	29.14

Turn on : 55.2992

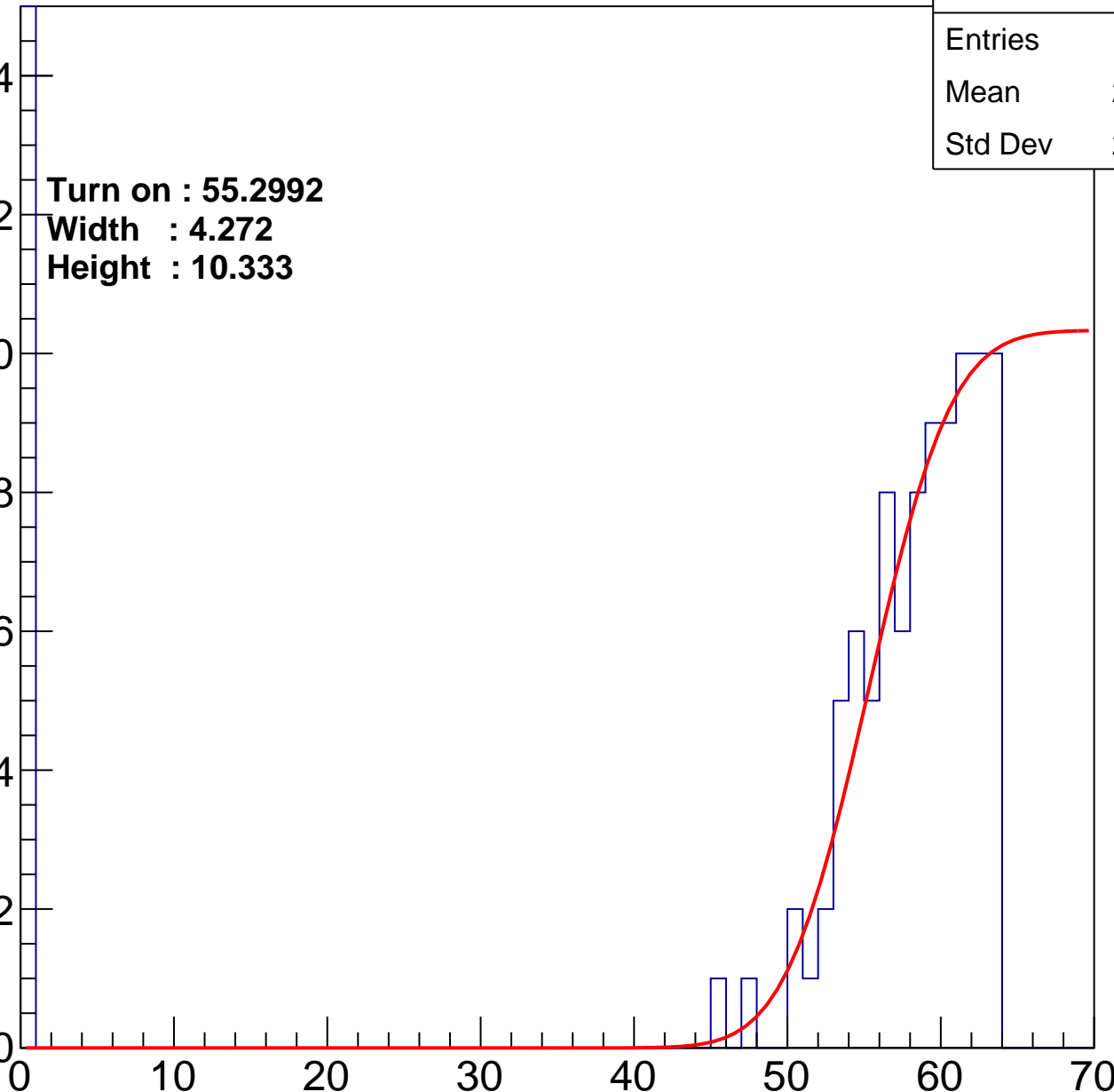
Width : 4.272

Height : 10.333

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L104S, U3-ch70

calib\_packv5\_033123\_0516.root, FC#4, port A1

Entries	185
Mean	36.08
Std Dev	27.71

Turn on : 55.6654

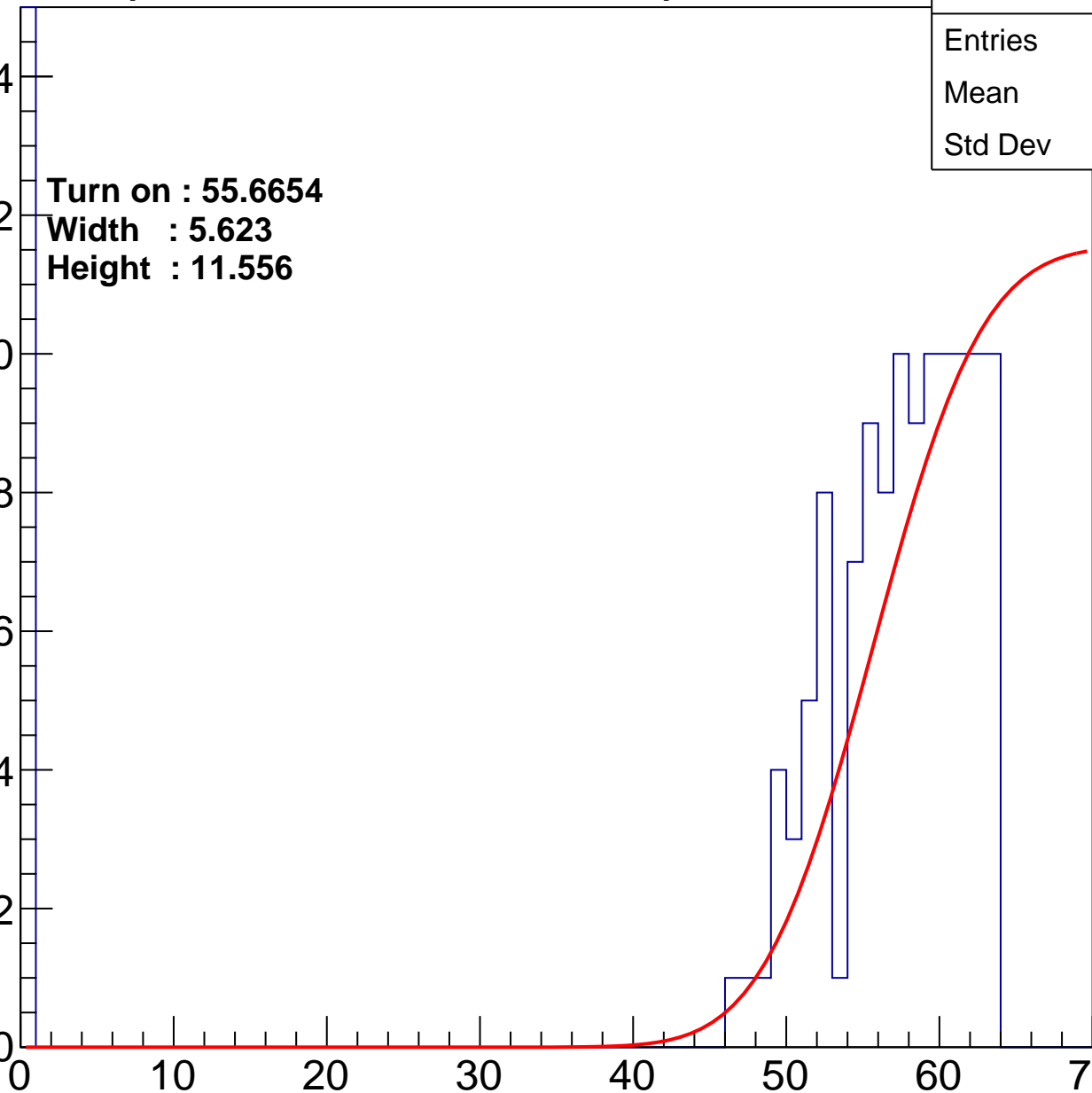
Width : 5.623

Height : 11.556

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L104S, U3-ch71

calib\_packv5\_033123\_0516.root, FC#4, port A1

Entries	212
Mean	28.32
Std Dev	28.98

**Turn on : 54.7949**

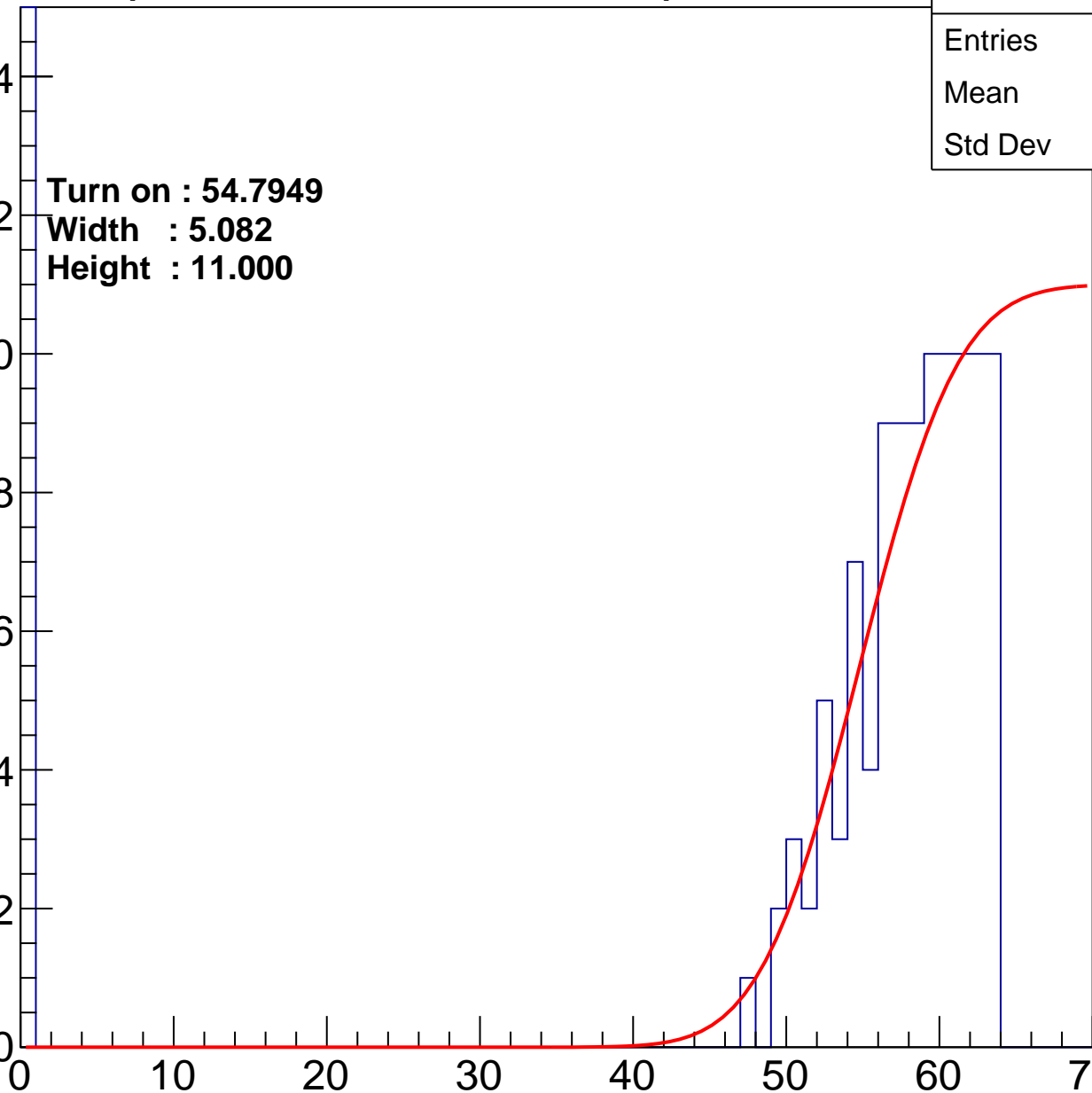
**Width : 5.082**

**Height : 11.000**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L104S, U3-ch72

calib\_packv5\_033123\_0516.root, FC#4, port A1

Entries	242
Mean	27.92
Std Dev	28.75

Turn on : 52.4495

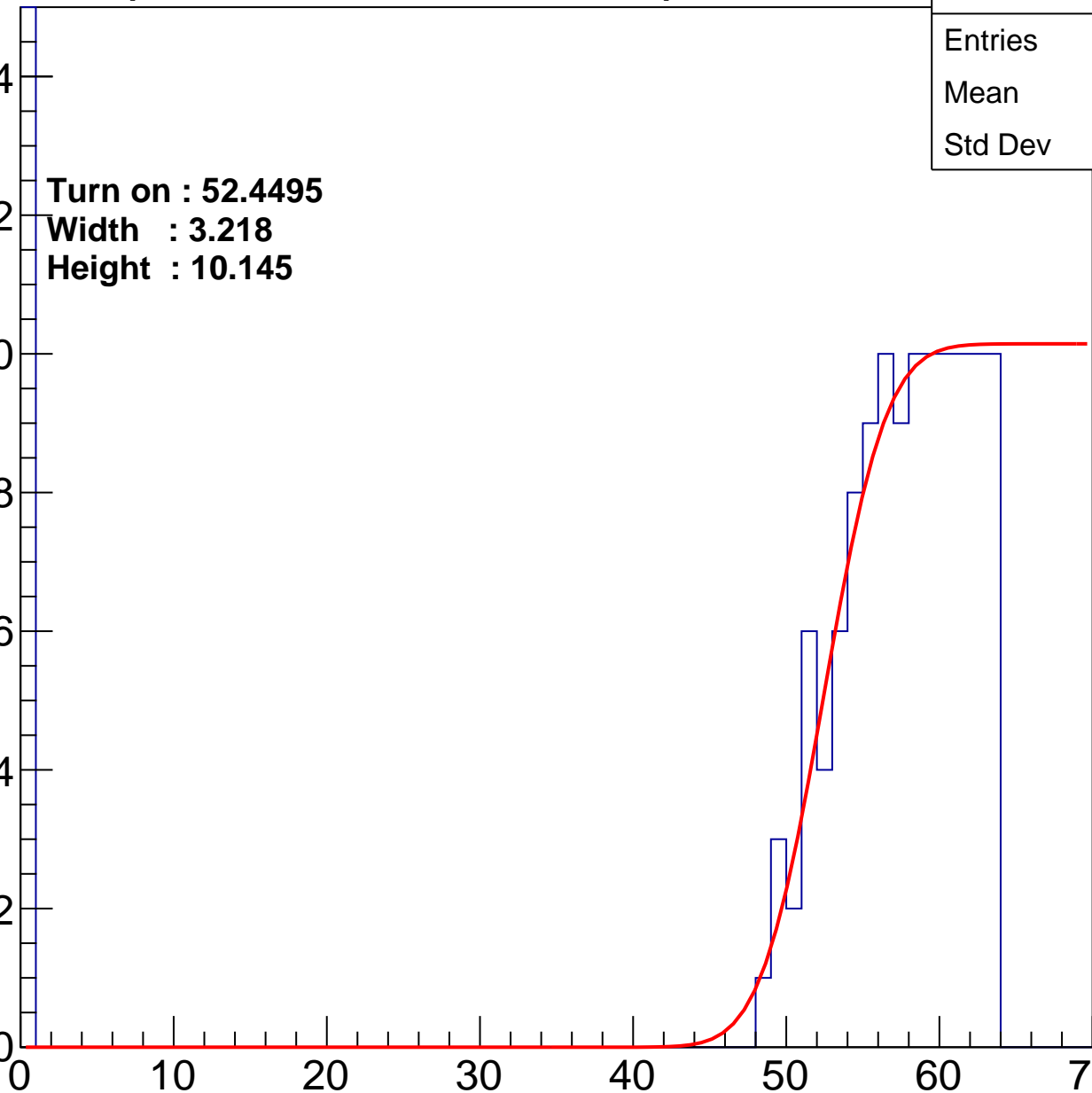
Width : 3.218

Height : 10.145

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L104S, U3-ch73

calib\_packv5\_033123\_0516.root, FC#4, port A1

Entries	227
Mean	33.16
Std Dev	28.06

Turn on : 51.0674

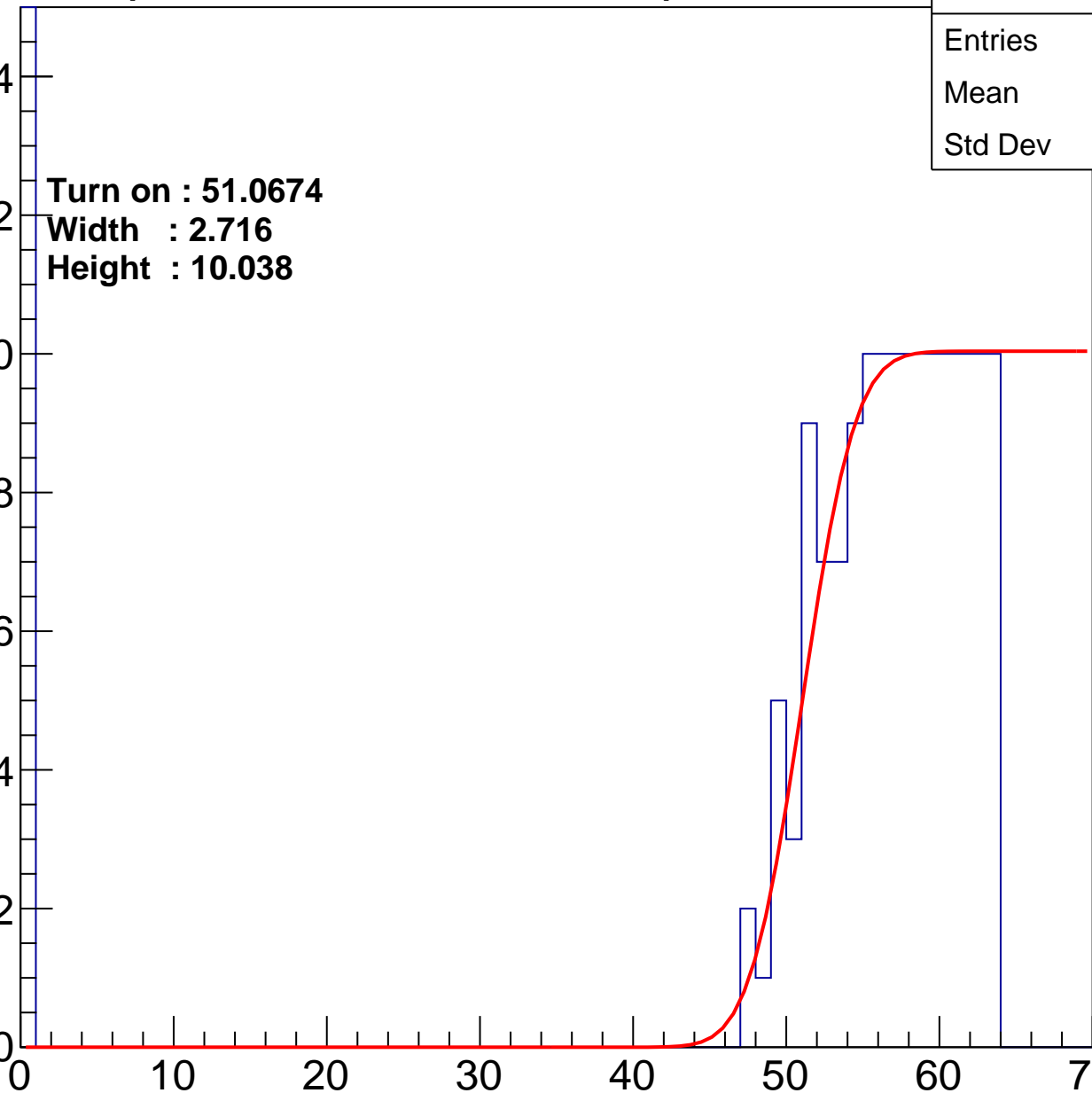
Width : 2.716

Height : 10.038

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L104S, U3-ch74

calib\_packv5\_033123\_0516.root, FC#4, port A1

Entries	204
Mean	33.07
Std Dev	28.4

**Turn on : 53.4382**

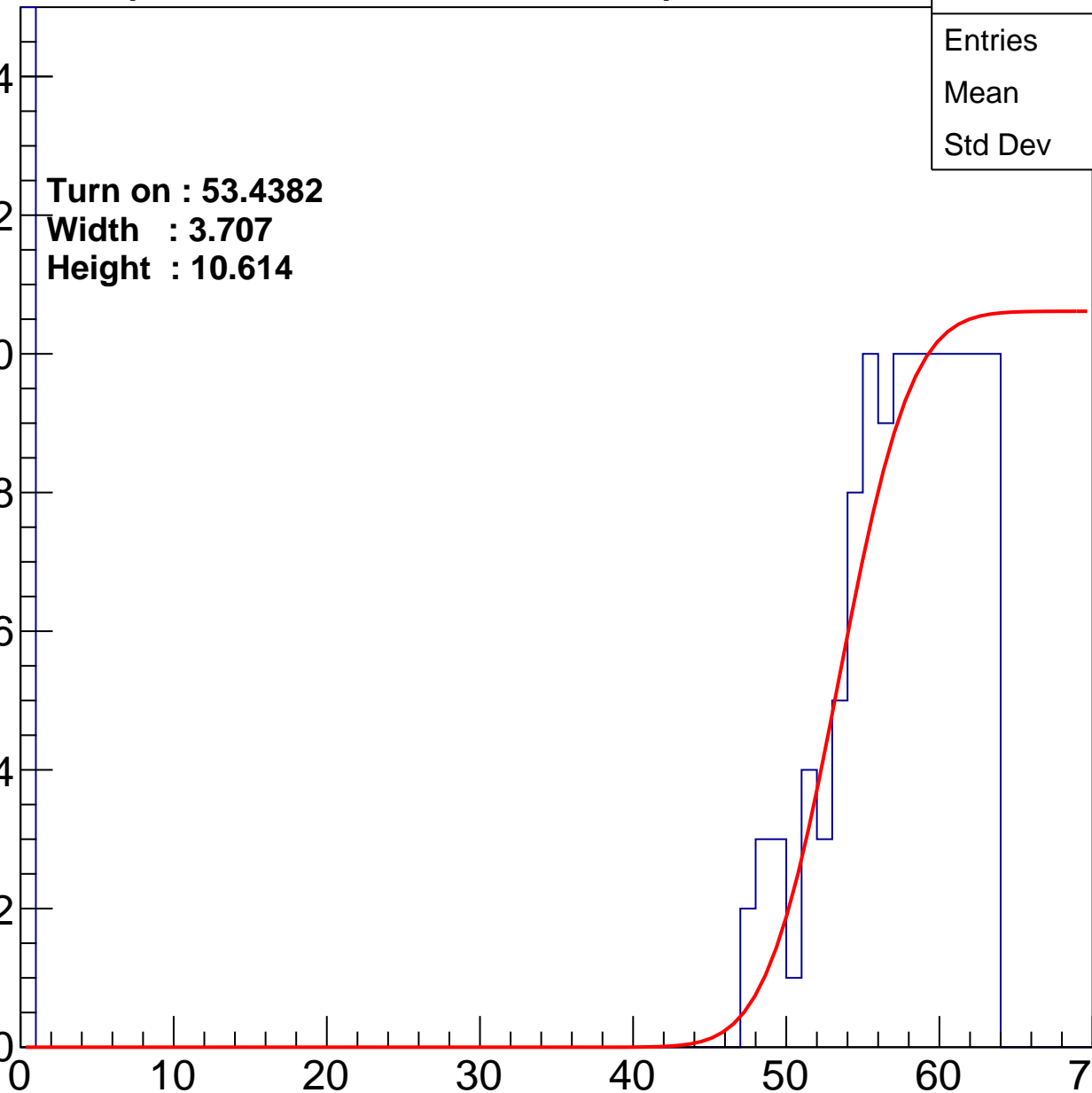
**Width : 3.707**

**Height : 10.614**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L104S, U3-ch75

calib\_packv5\_033123\_0516.root, FC#4, port A1

Entries	231
Mean	28.36
Std Dev	28.86

Turn on : 52.8384

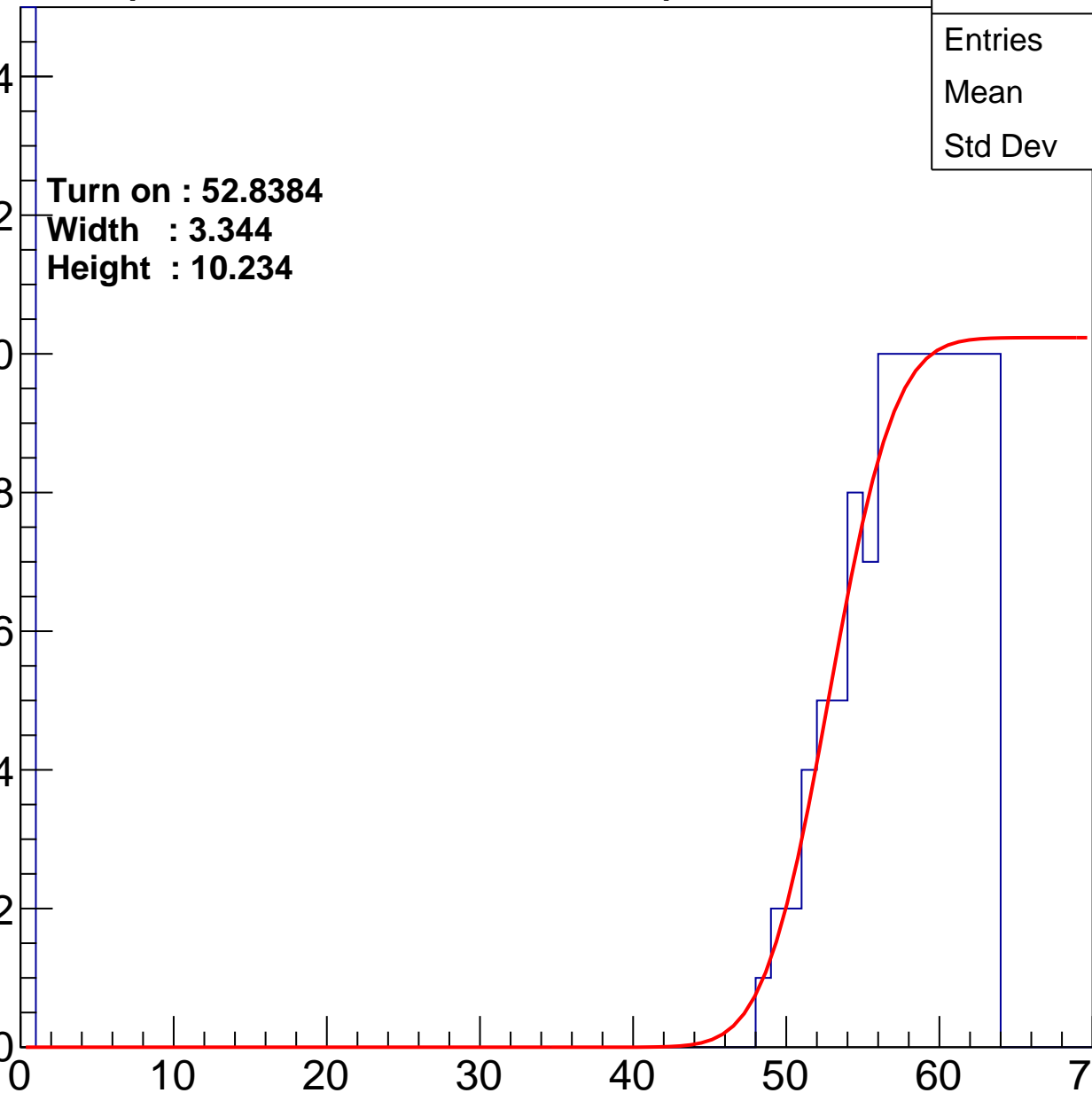
Width : 3.344

Height : 10.234

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L104S, U3-ch76

calib\_packv5\_033123\_0516.root, FC#4, port A1

Entries	234
Mean	26.71
Std Dev	28.94

Turn on : 53.0345

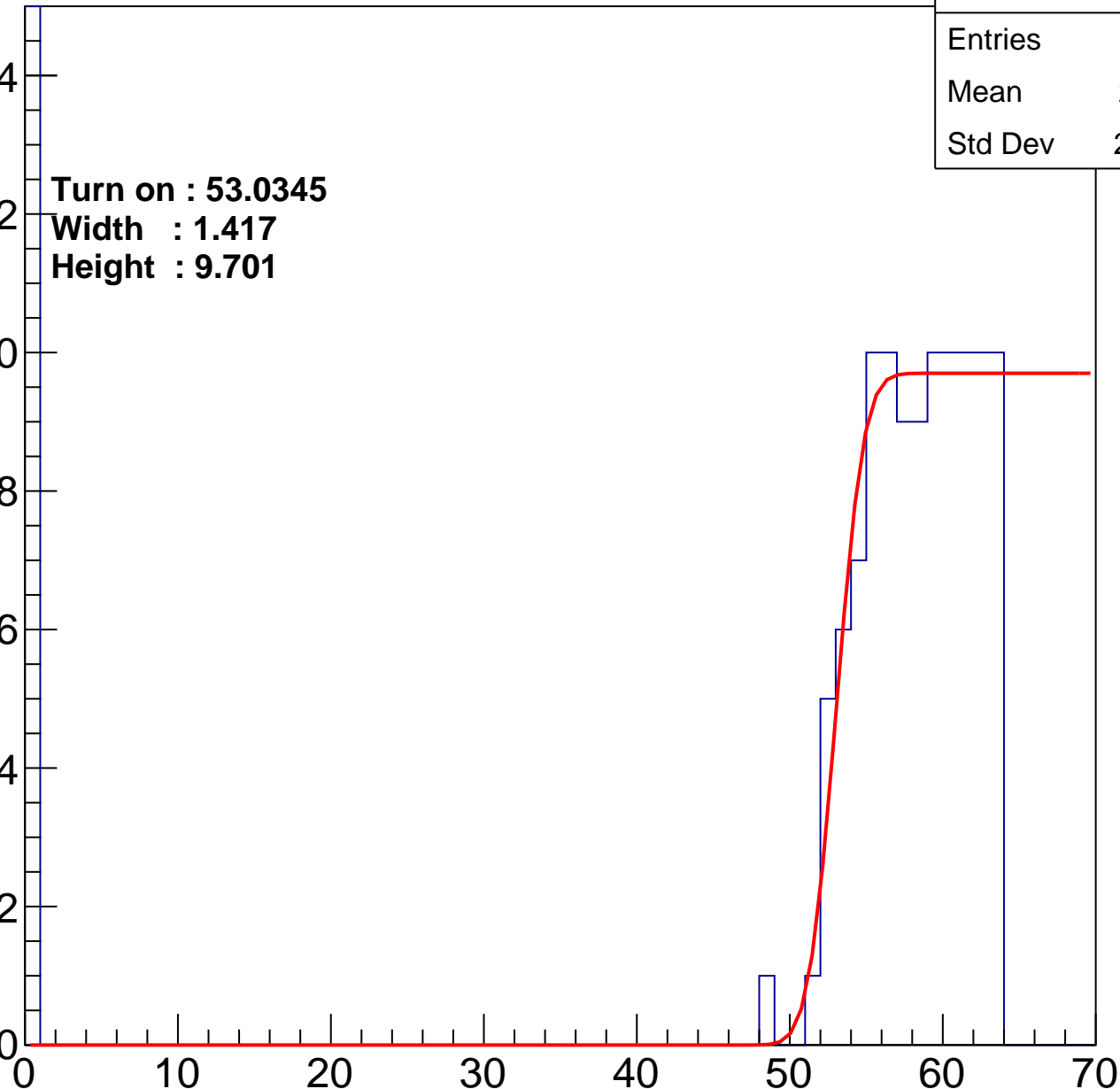
Width : 1.417

Height : 9.701

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L104S, U3-ch77

calib\_packv5\_033123\_0516.root, FC#4, port A1

Entries	207
Mean	28.89
Std Dev	29.13

Turn on : 53.8209

Width : 2.506

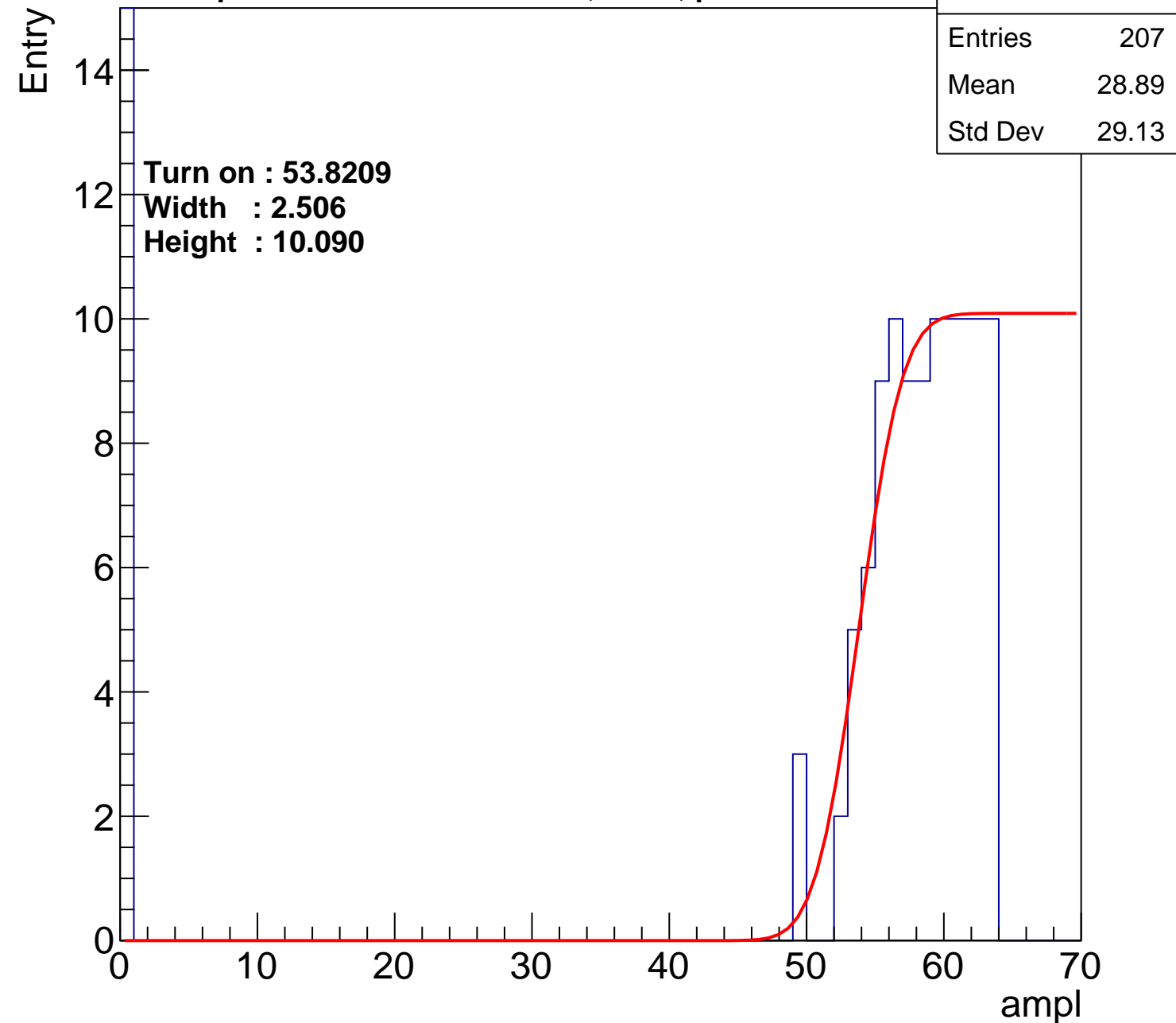
Height : 10.090

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L104S, U3-ch78

calib\_packv5\_033123\_0516.root, FC#4, port A1

Entries	245
Mean	30.21
Std Dev	28.37

**Turn on : 51.5429**

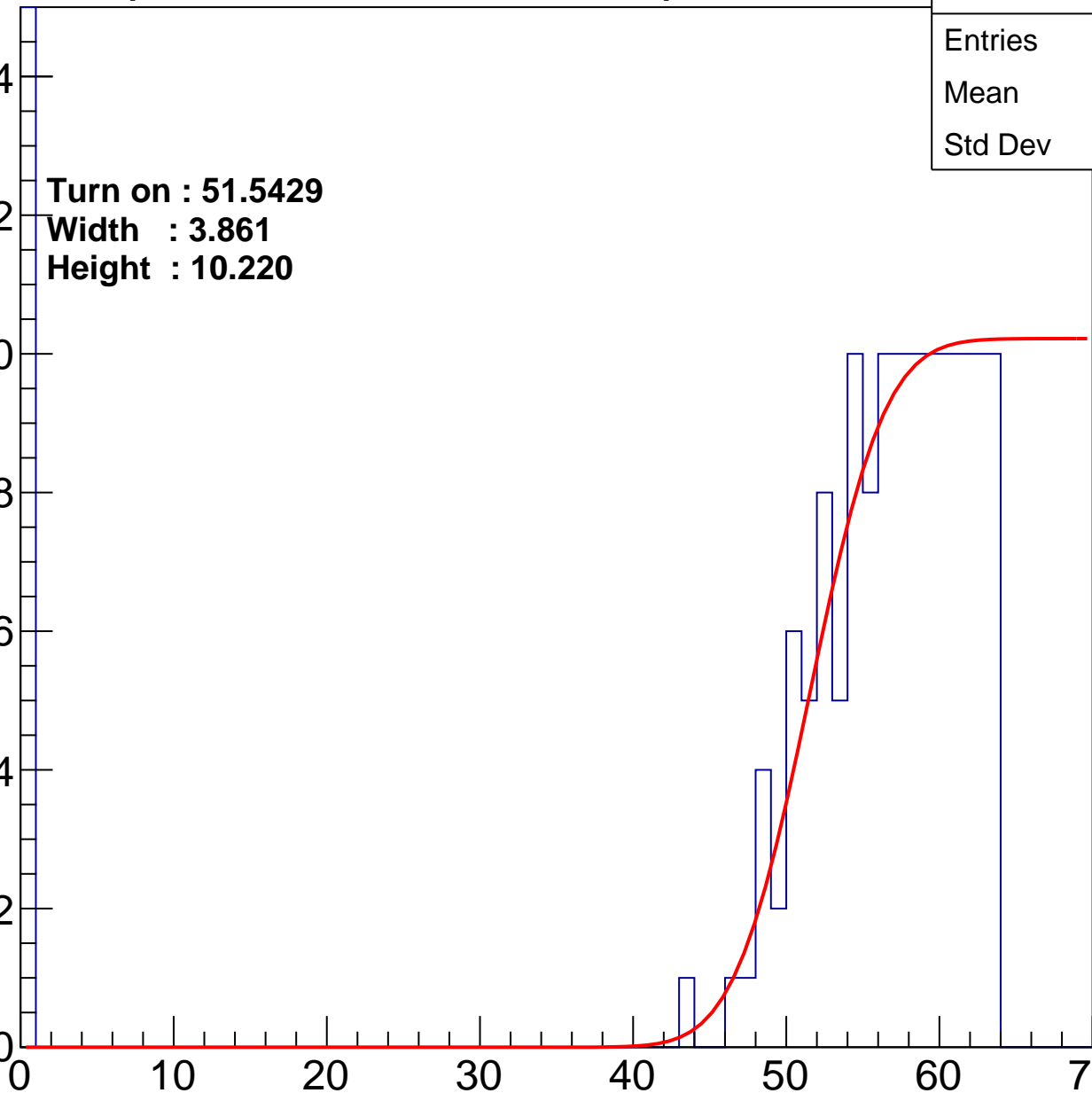
**Width : 3.861**

**Height : 10.220**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L104S, U3-ch79

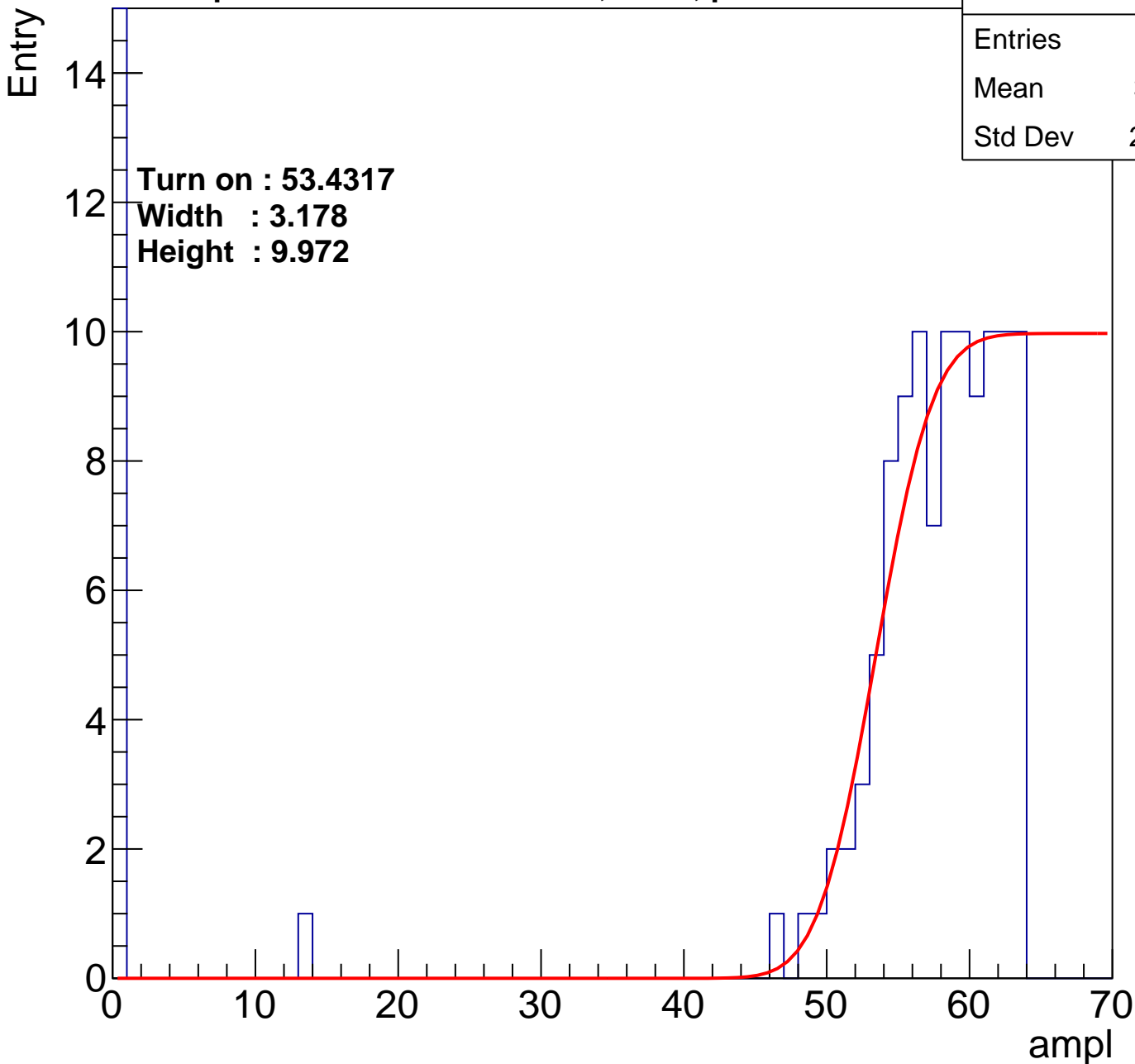
calib\_packv5\_033123\_0516.root, FC#4, port A1

Entries	205
Mean	30.41
Std Dev	28.84

Turn on : 53.4317

Width : 3.178

Height : 9.972



# B1L104S, U3-ch80

calib\_packv5\_033123\_0516.root, FC#4, port A1

Entries	230
Mean	27.71
Std Dev	28.83

Turn on : 52.8169

Width : 3.410

Height : 9.992

Entry

14

12

10

8

6

4

2

0

0

10

20

30

40

50

60

70

ampl

0

2

4

6

8

10

12

14

# B1L104S, U3-ch81

calib\_packv5\_033123\_0516.root, FC#4, port A1

Entries	175
Mean	32.25
Std Dev	29.03

Turn on : 54.8061

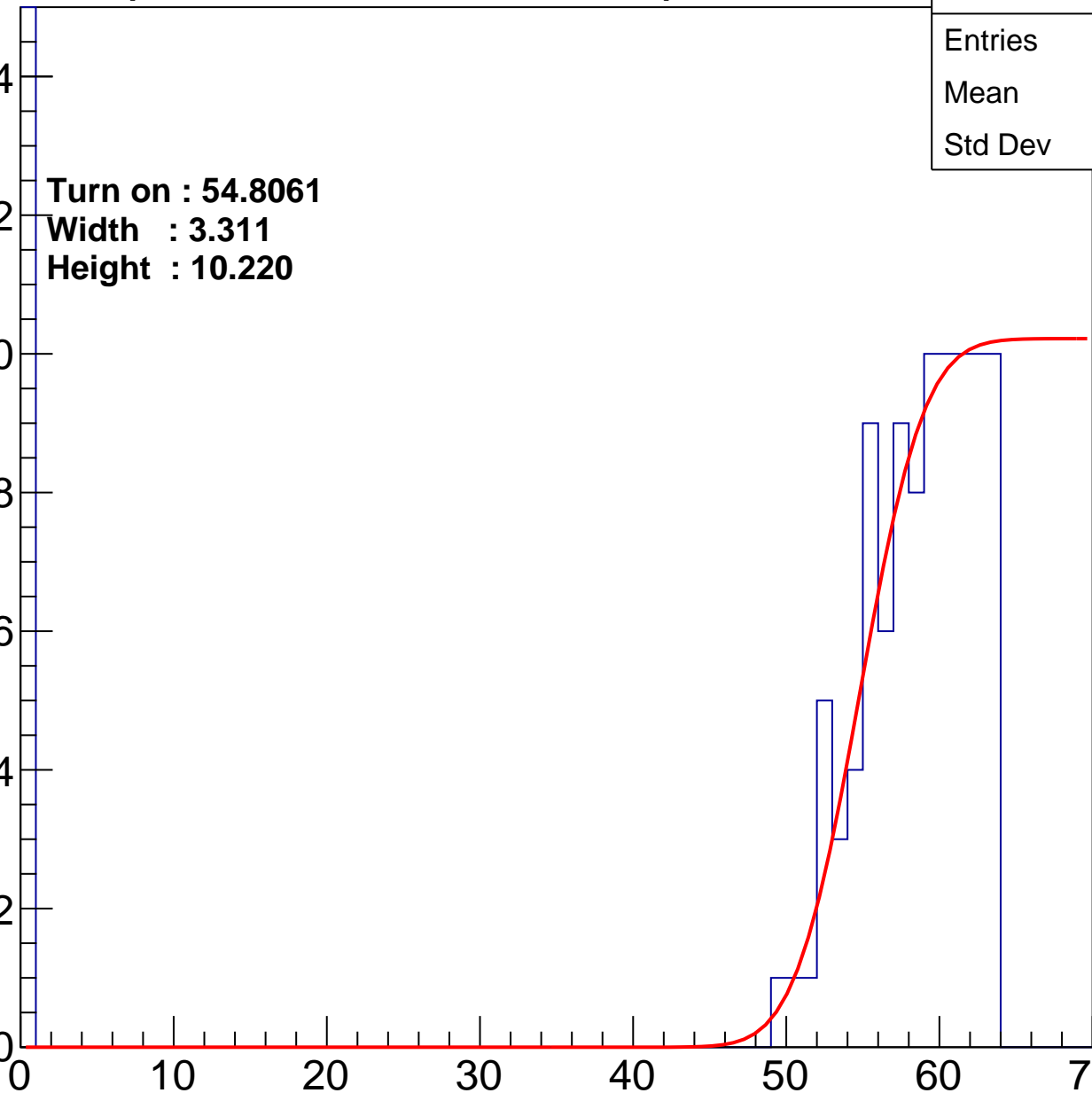
Width : 3.311

Height : 10.220

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L104S, U3-ch82

calib\_packv5\_033123\_0516.root, FC#4, port A1

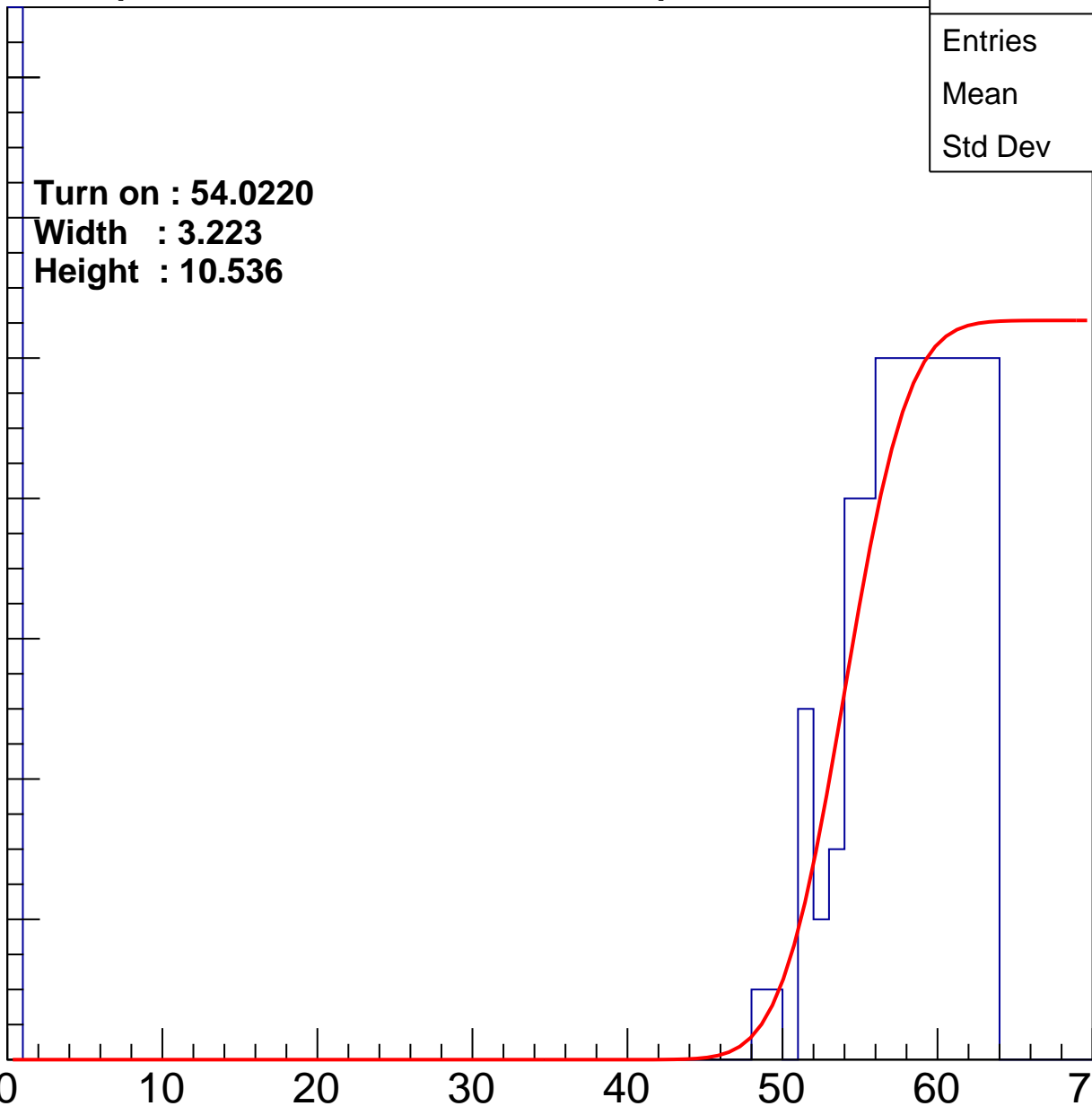
Entry

14  
12  
10  
8  
6  
4  
2  
0

Turn on : 54.0220  
Width : 3.223  
Height : 10.536

Entries	193
Mean	32.37
Std Dev	28.84

ampl



# B1L104S, U3-ch83

calib\_packv5\_033123\_0516.root, FC#4, port A1

Entries	236
Mean	30.3
Std Dev	28.48

Turn on : 51.7941

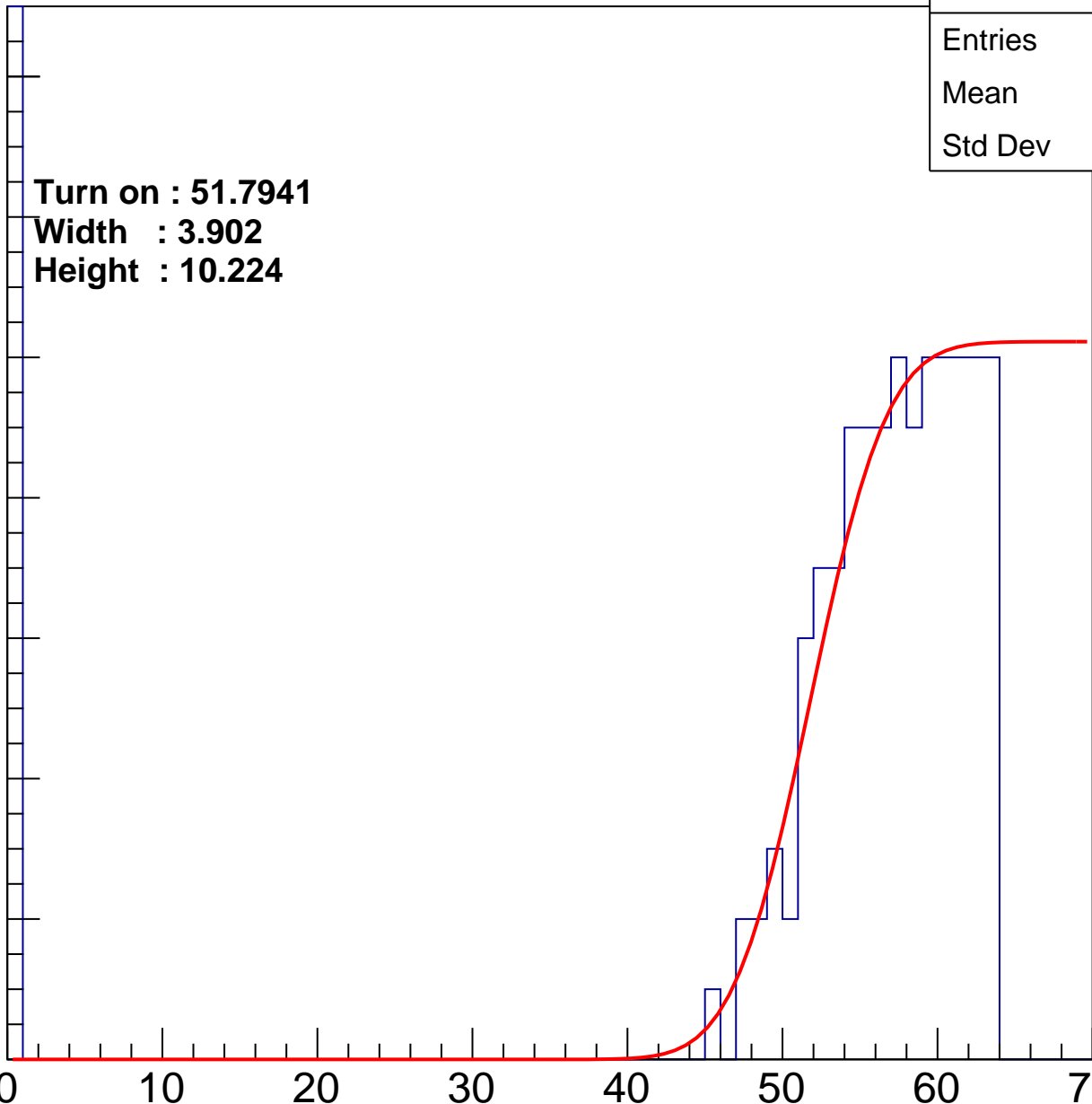
Width : 3.902

Height : 10.224

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L104S, U3-ch84

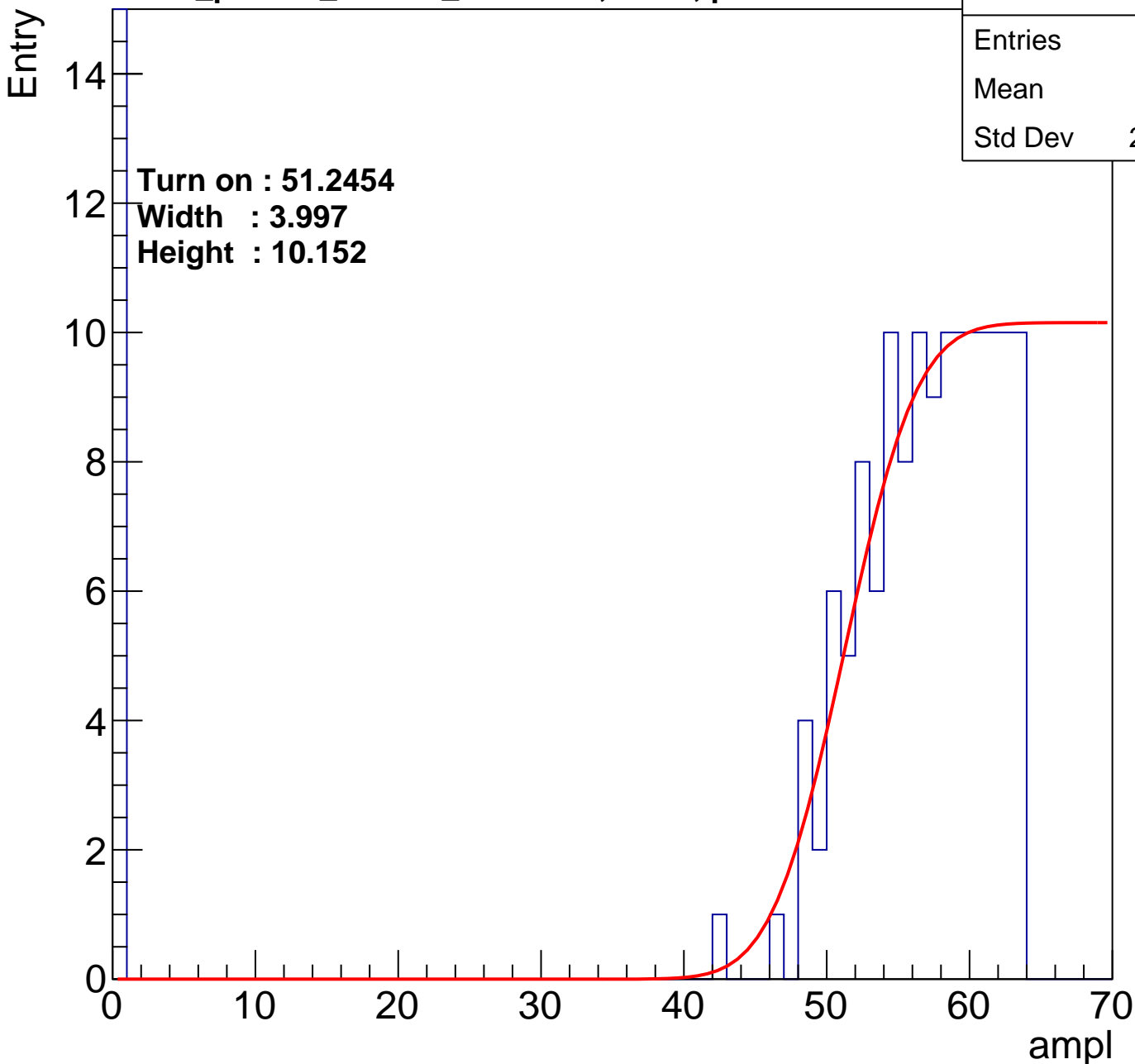
calib\_packv5\_033123\_0516.root, FC#4, port A1

Entries	250
Mean	29.4
Std Dev	28.43

Turn on : 51.2454

Width : 3.997

Height : 10.152



# B1L104S, U3-ch85

calib\_packv5\_033123\_0516.root, FC#4, port A1

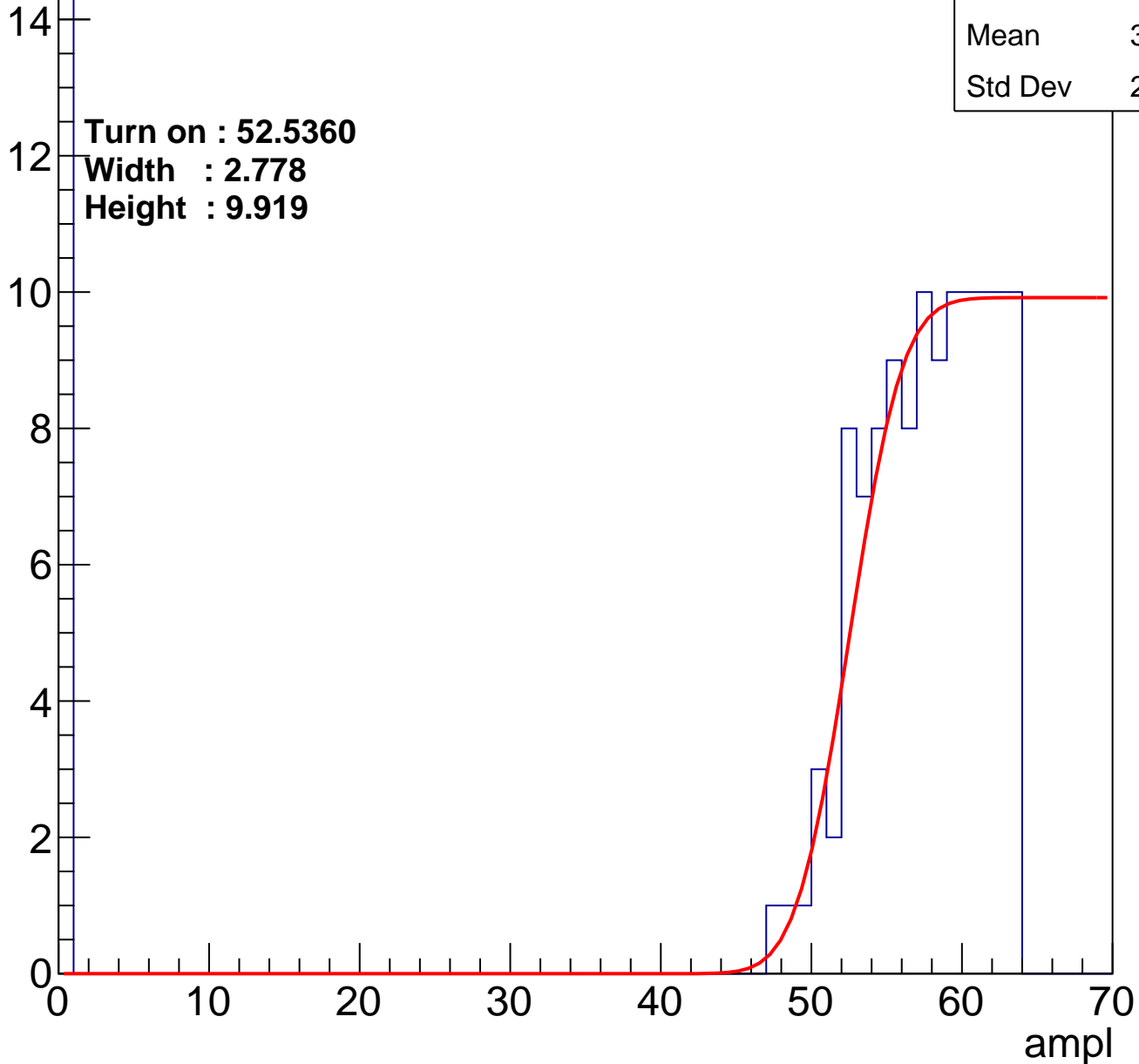
Entries	222
Mean	30.18
Std Dev	28.73

Turn on : 52.5360

Width : 2.778

Height : 9.919

Entry



# B1L104S, U3-ch86

calib\_packv5\_033123\_0516.root, FC#4, port A1

Entries	197
Mean	32.22
Std Dev	28.79

**Turn on : 53.1839**

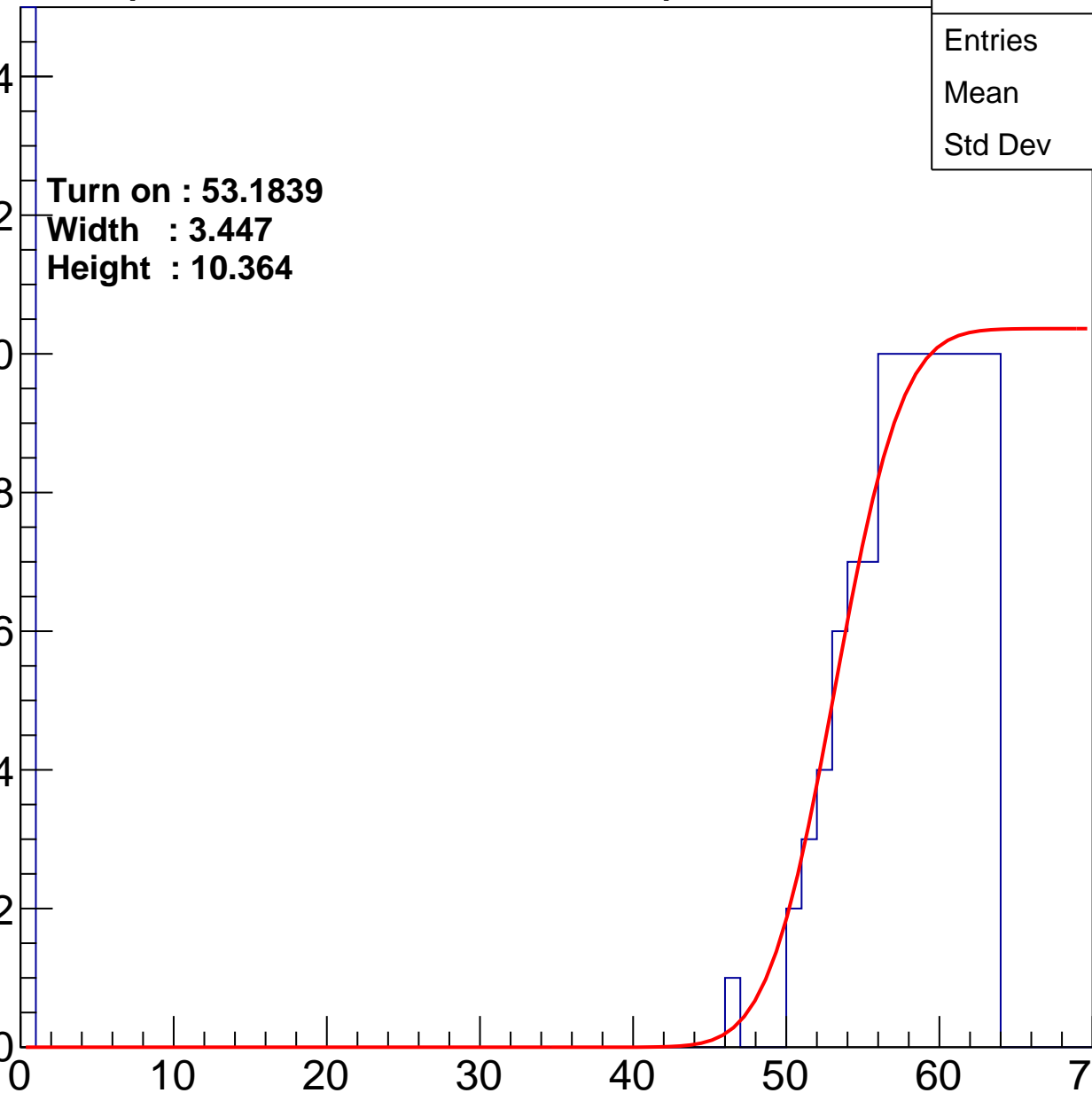
**Width : 3.447**

**Height : 10.364**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L104S, U3-ch87

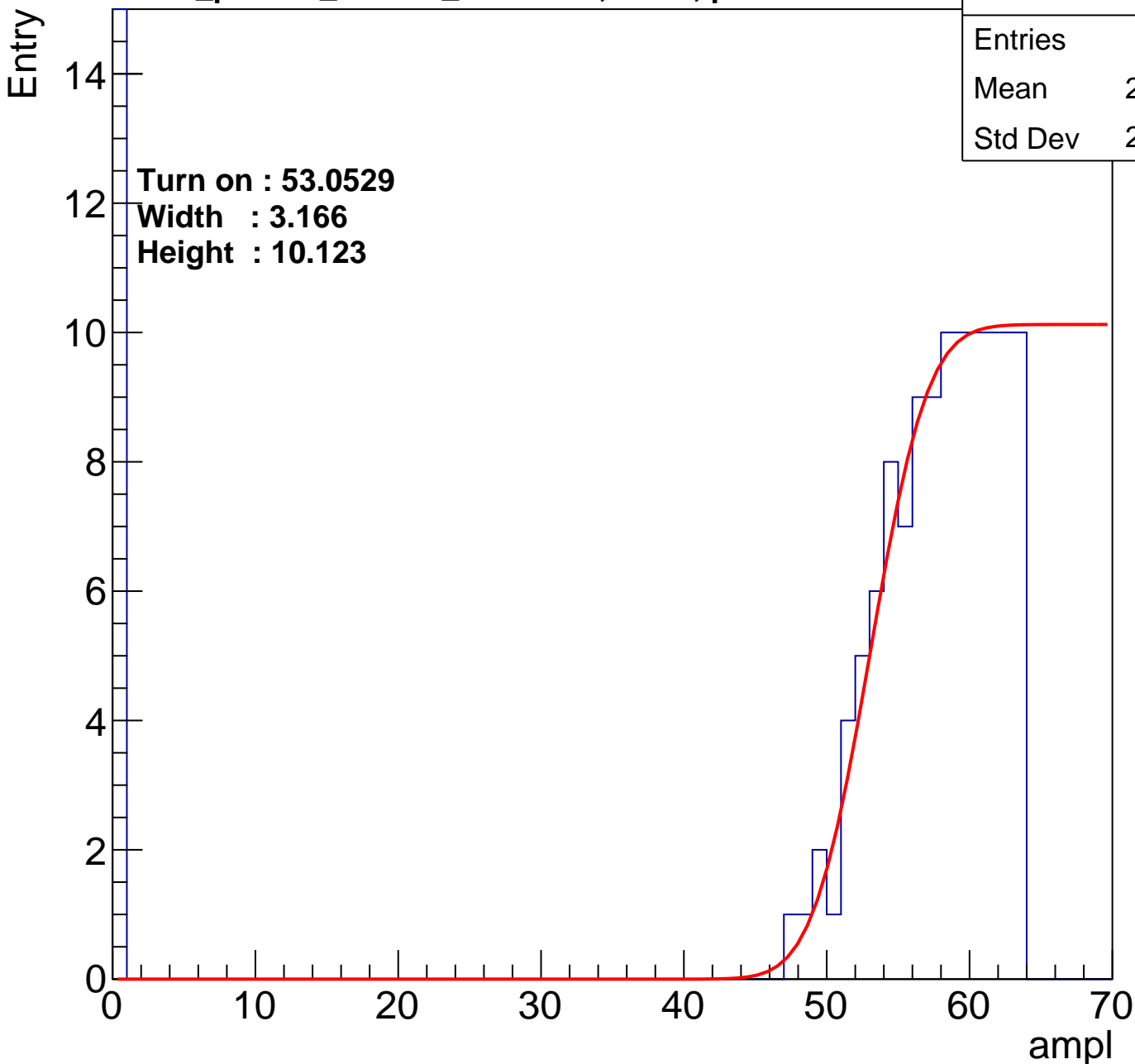
calib\_packv5\_033123\_0516.root, FC#4, port A1

Entries	221
Mean	29.36
Std Dev	28.84

Turn on : 53.0529

Width : 3.166

Height : 10.123



# B1L104S, U3-ch88

calib\_packv5\_033123\_0516.root, FC#4, port A1

Entries	221
Mean	29.16
Std Dev	28.88

Turn on : 52.4734

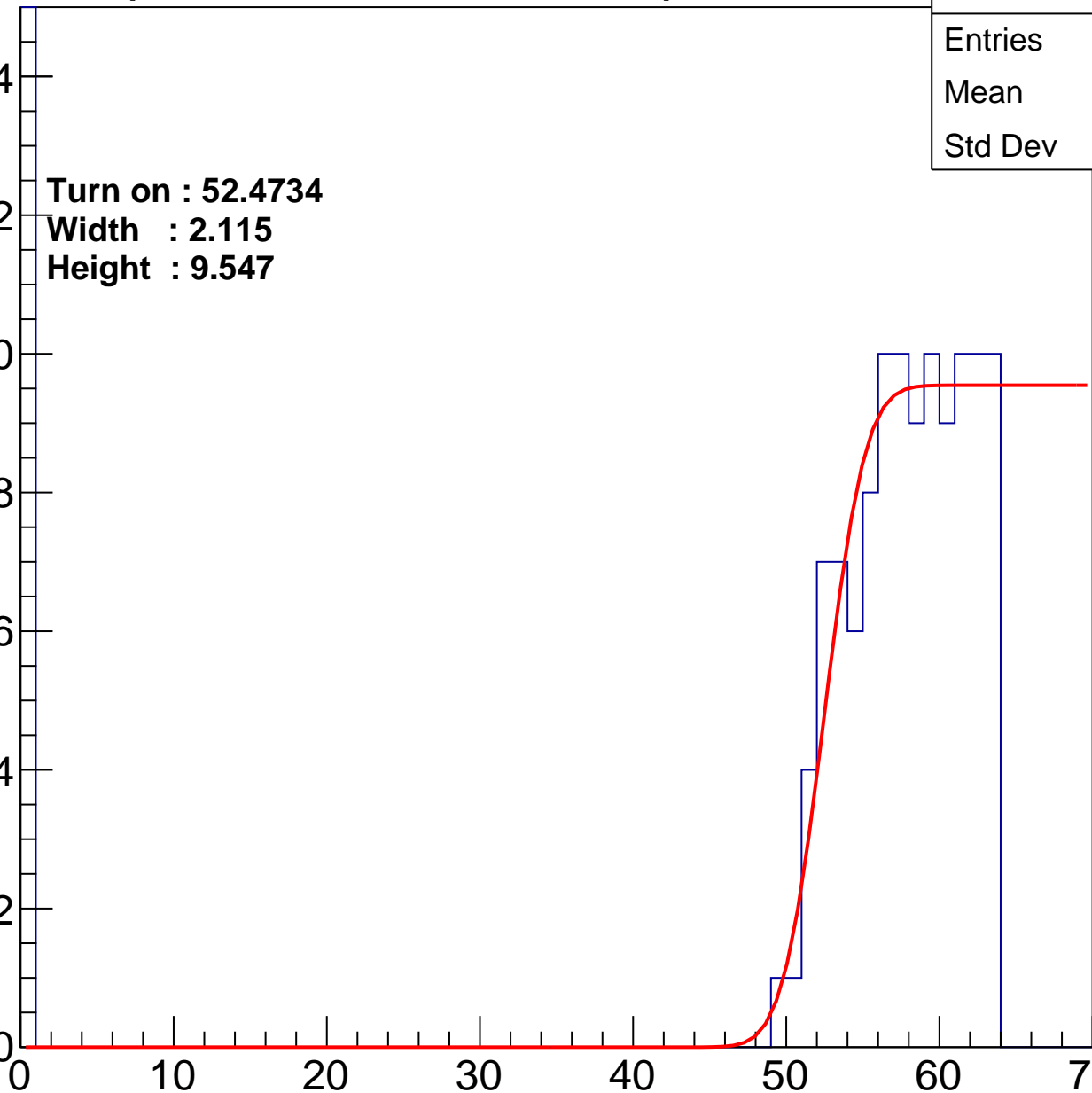
Width : 2.115

Height : 9.547

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L104S, U3-ch89

calib\_packv5\_033123\_0516.root, FC#4, port A1

Entries	181
Mean	32.58
Std Dev	28.81

Turn on : 54.1122

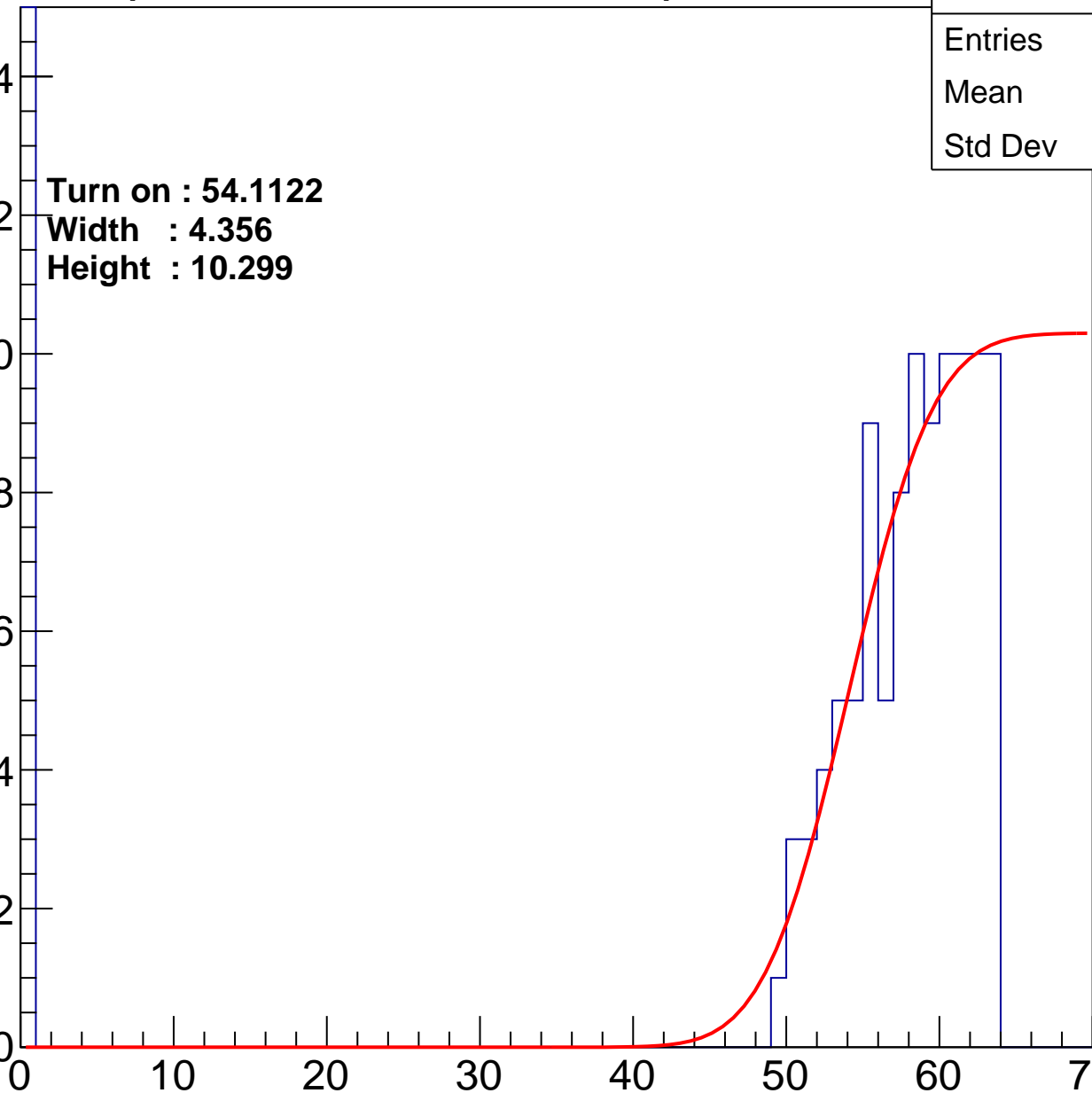
Width : 4.356

Height : 10.299

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L104S, U3-ch90

calib\_packv5\_033123\_0516.root, FC#4, port A1

Entries	256
Mean	27.39
Std Dev	28.44

Turn on : 52.7061

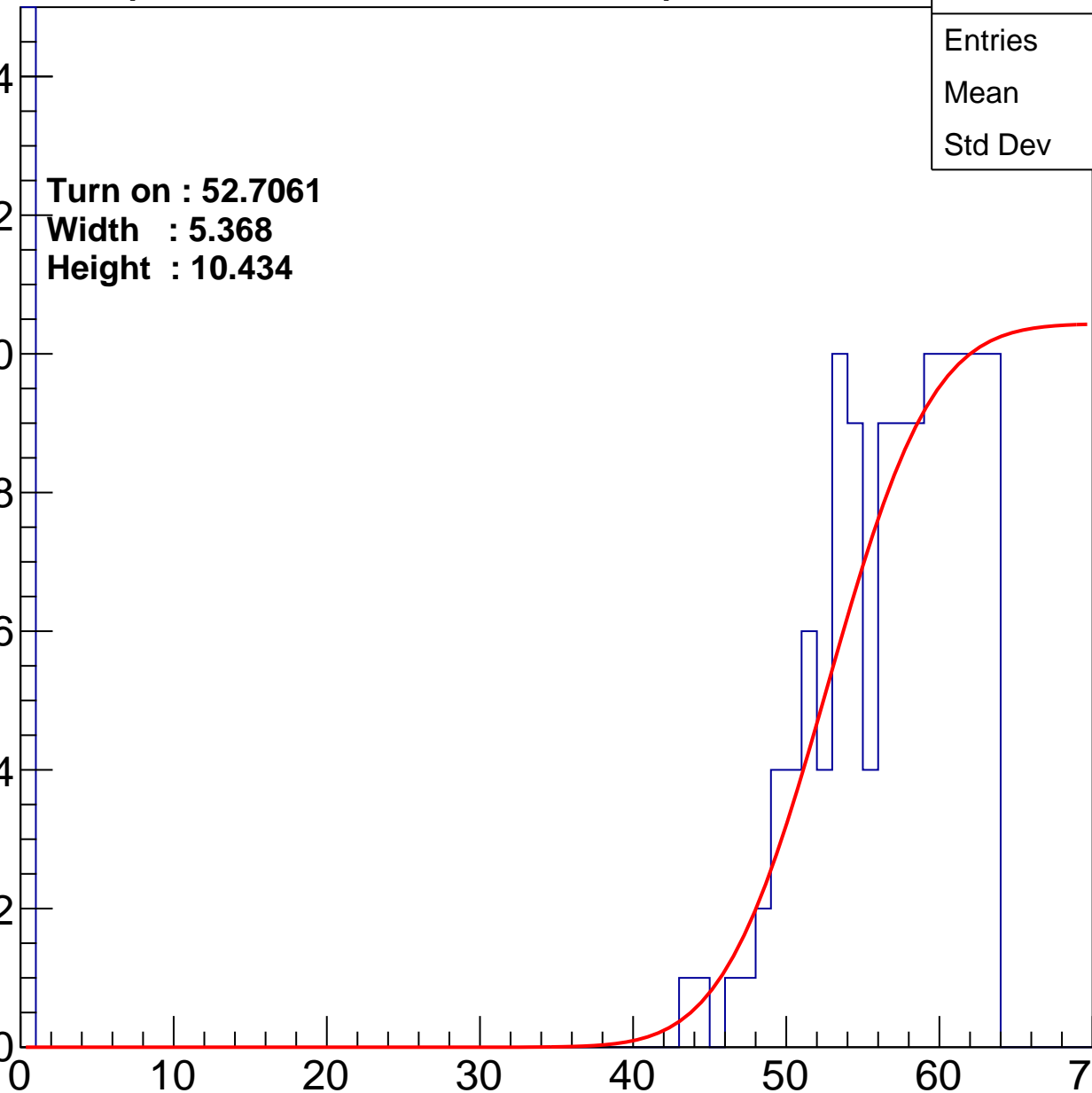
Width : 5.368

Height : 10.434

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L104S, U3-ch91

calib\_packv5\_033123\_0516.root, FC#4, port A1

Entries	206
Mean	26.57
Std Dev	29.1

**Turn on : 54.9596**

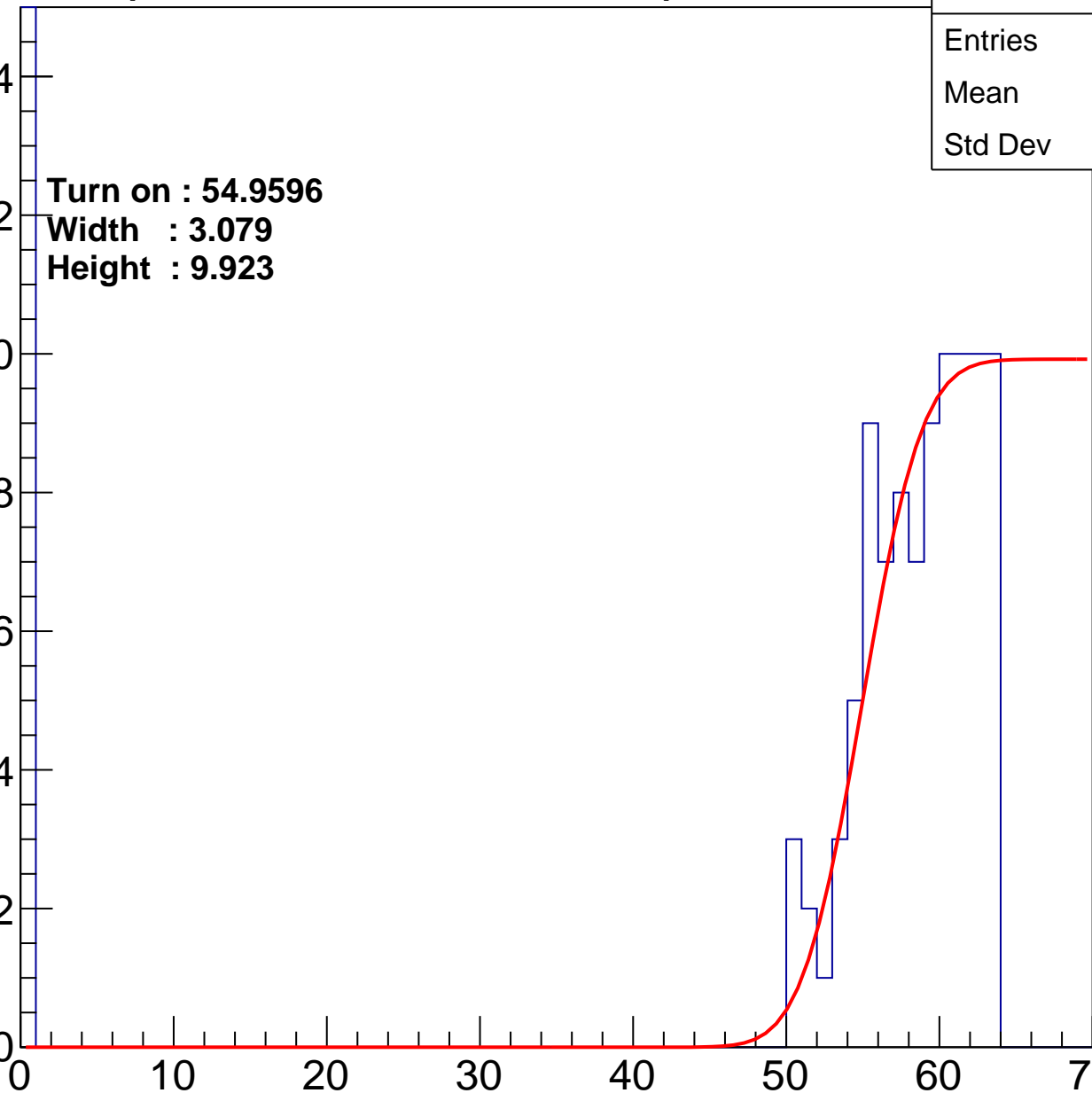
**Width : 3.079**

**Height : 9.923**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L104S, U3-ch92

calib\_packv5\_033123\_0516.root, FC#4, port A1

Entries	227
Mean	29.13
Std Dev	28.87

**Turn on : 52.6601**

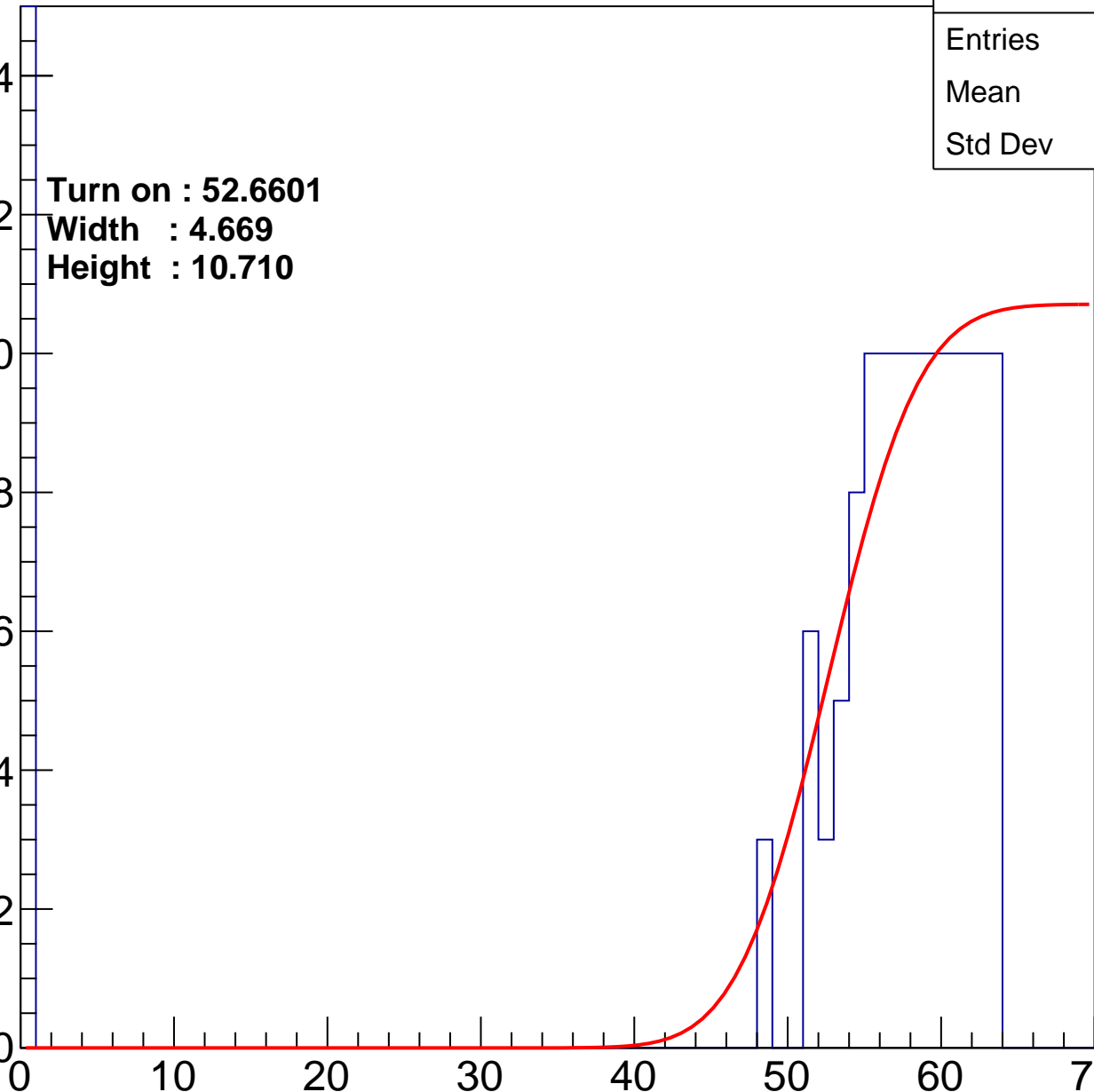
**Width : 4.669**

**Height : 10.710**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L104S, U3-ch93

calib\_packv5\_033123\_0516.root, FC#4, port A1

Entries	186
Mean	33.52
Std Dev	28.63

**Turn on : 54.6020**

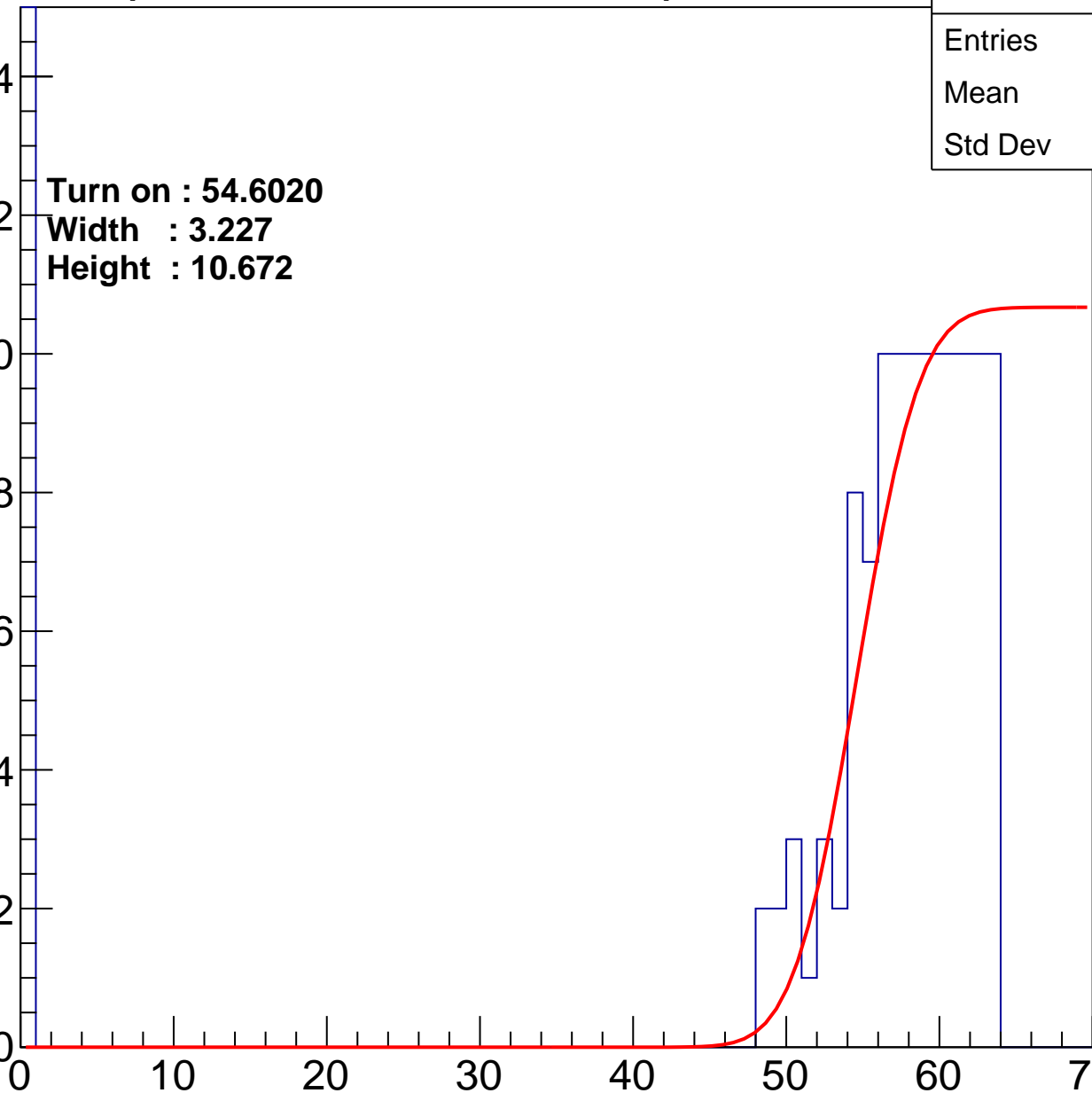
**Width : 3.227**

**Height : 10.672**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L104S, U3-ch94

calib\_packv5\_033123\_0516.root, FC#4, port A1

Entries	207
Mean	26.8
Std Dev	29.18

Turn on : 54.6384

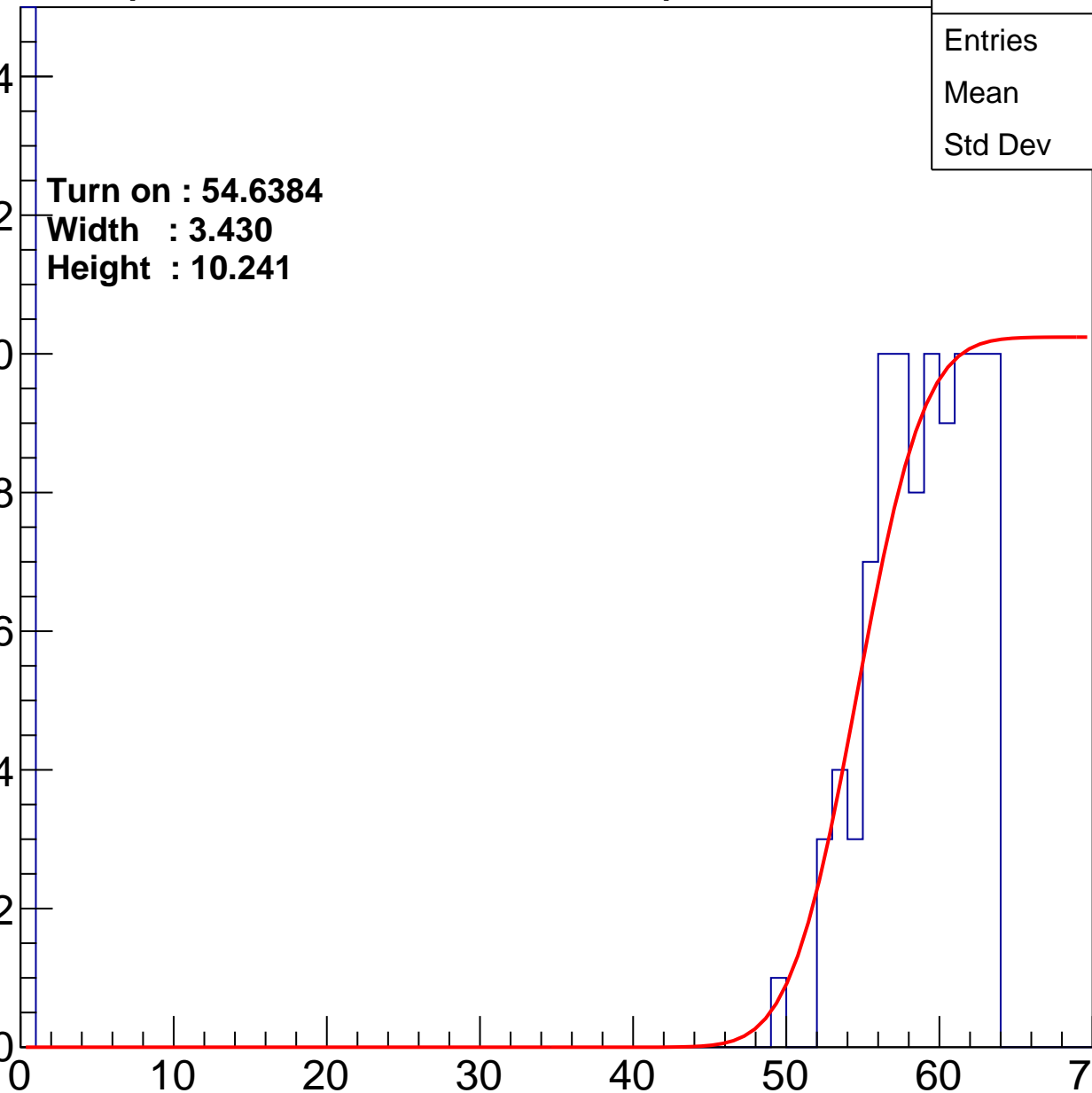
Width : 3.430

Height : 10.241

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L104S, U3-ch95

calib\_packv5\_033123\_0516.root, FC#4, port A1

Entries	213
Mean	28.97
Std Dev	28.95

**Turn on : 52.7786**

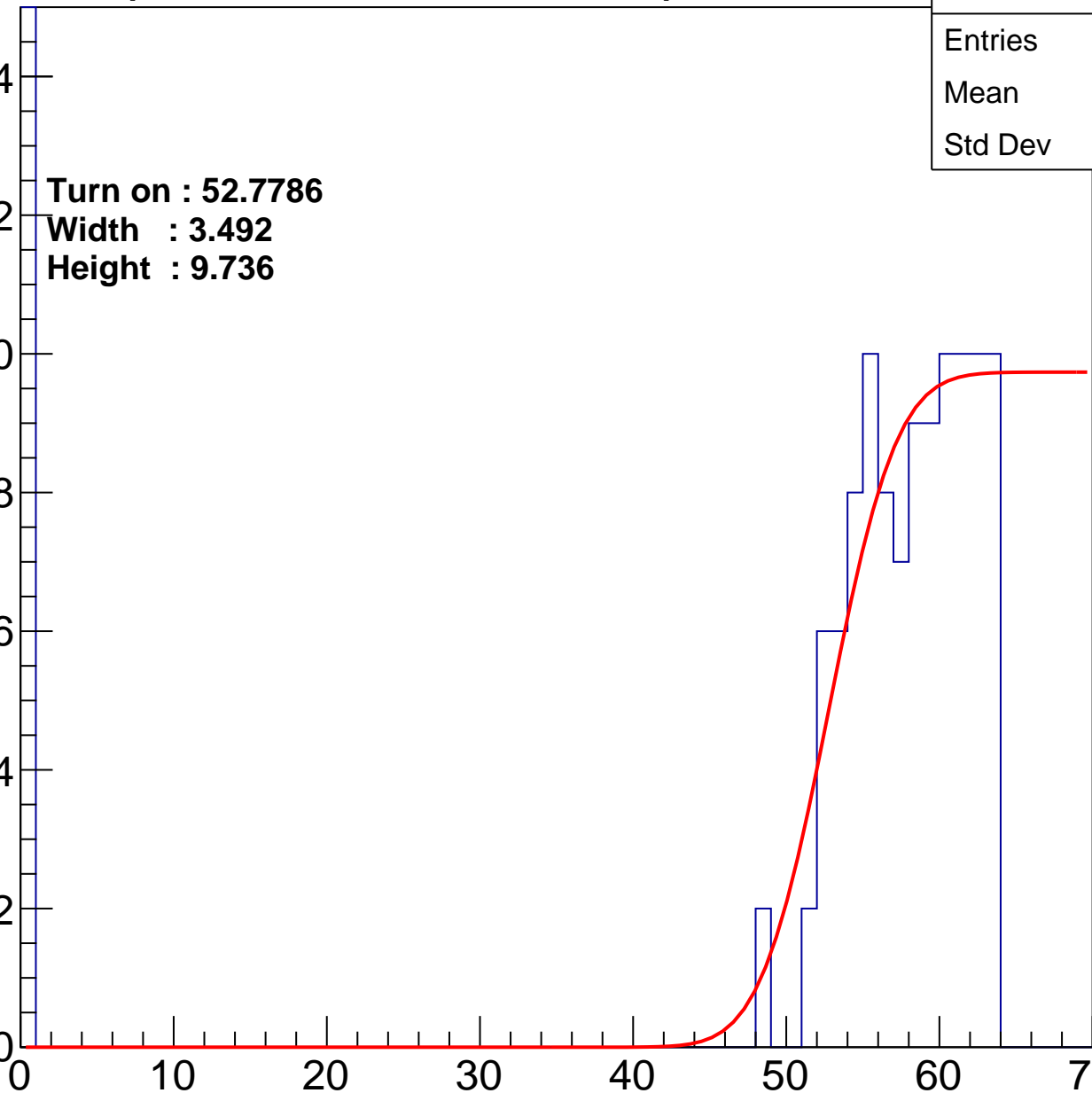
**Width : 3.492**

**Height : 9.736**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L104S, U3-ch96

calib\_packv5\_033123\_0516.root, FC#4, port A1

Entries	237
Mean	31.66
Std Dev	28.2

Turn on : 51.0261

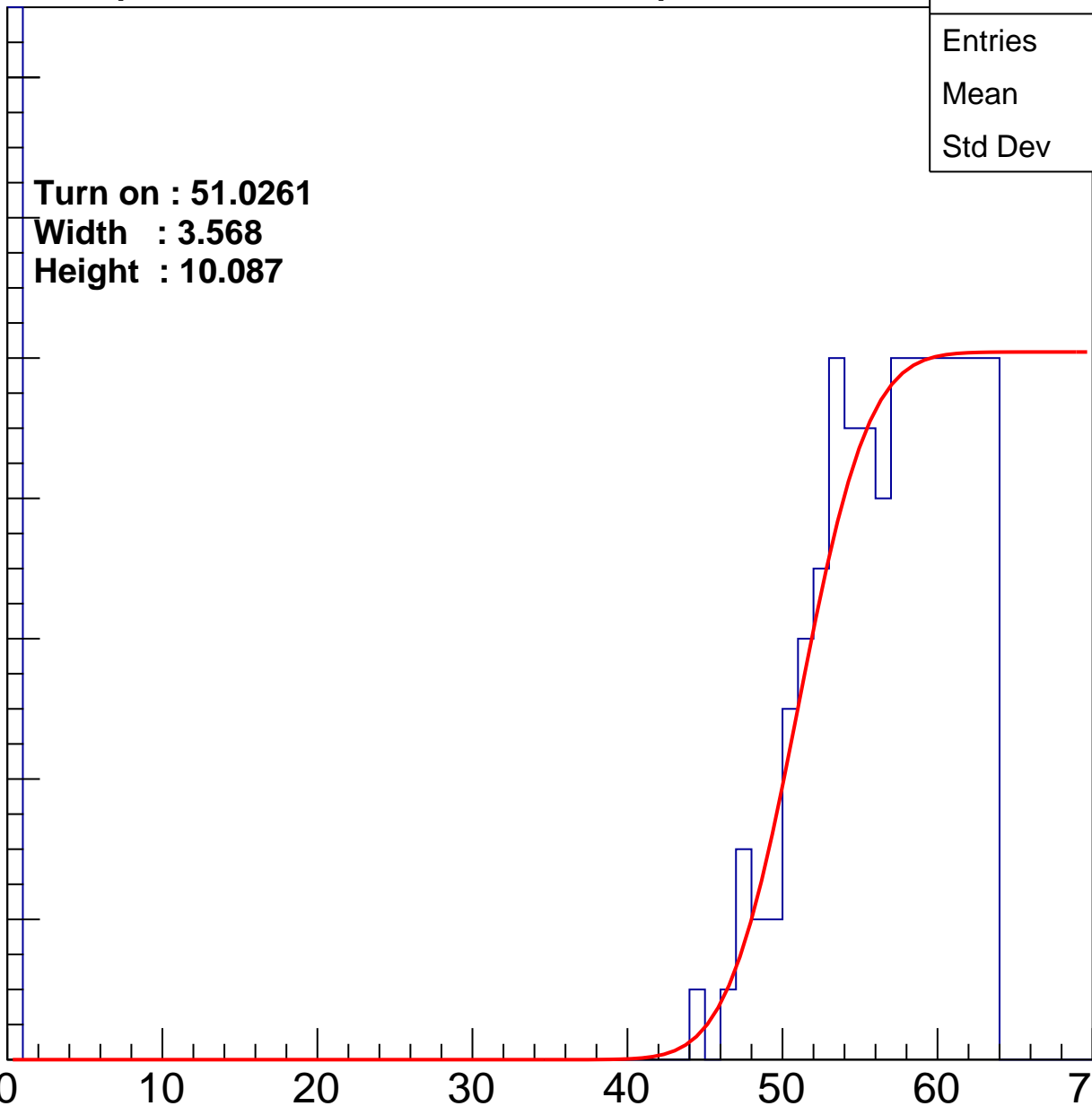
Width : 3.568

Height : 10.087

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L104S, U3-ch97

calib\_packv5\_033123\_0516.root, FC#4, port A1

Entries	222
Mean	27.07
Std Dev	28.95

**Turn on : 54.0977**

**Width : 4.131**

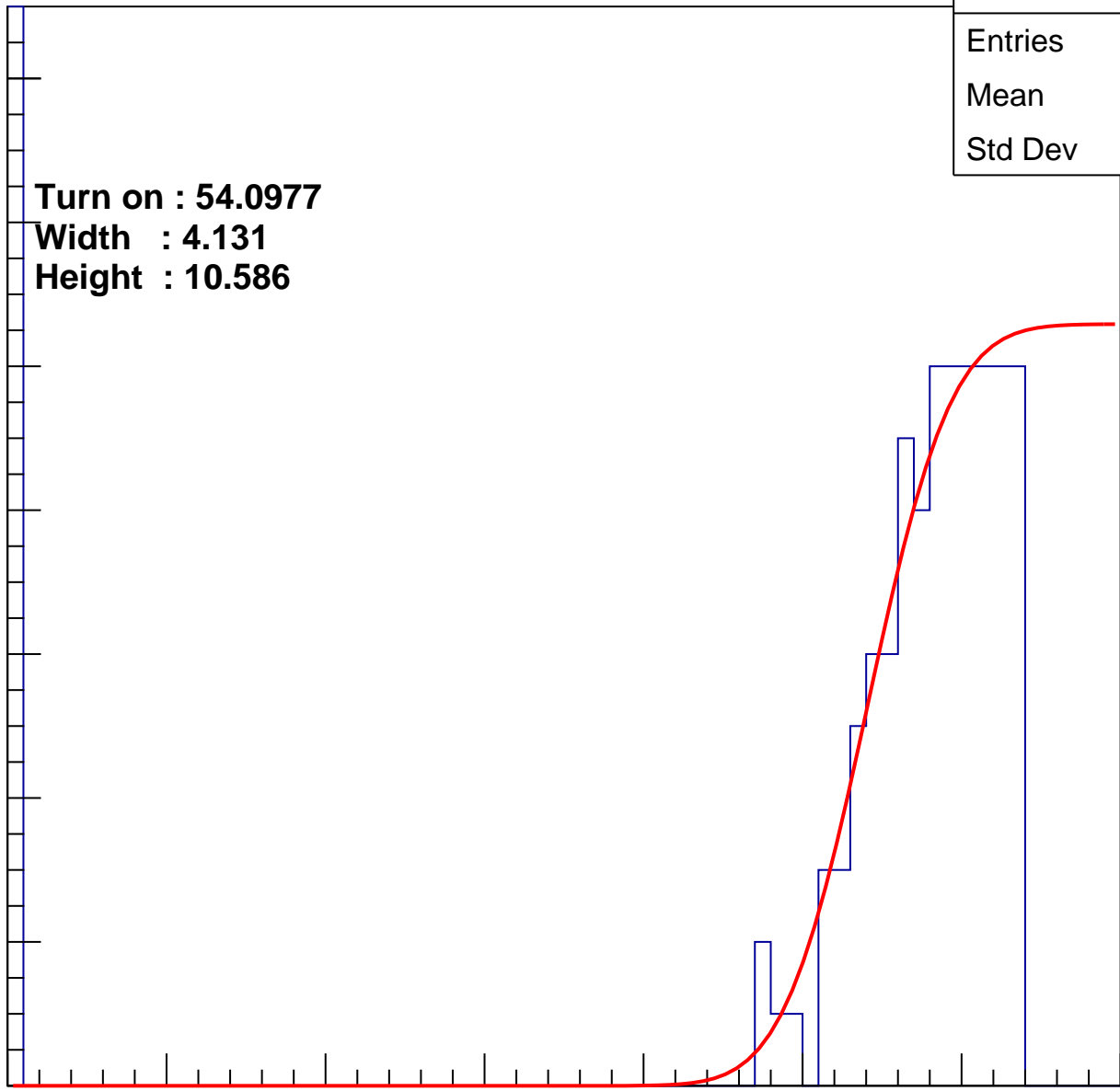
**Height : 10.586**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L104S, U3-ch98

calib\_packv5\_033123\_0516.root, FC#4, port A1

Entries	211
Mean	30.93
Std Dev	28.7

**Turn on : 53.4232**

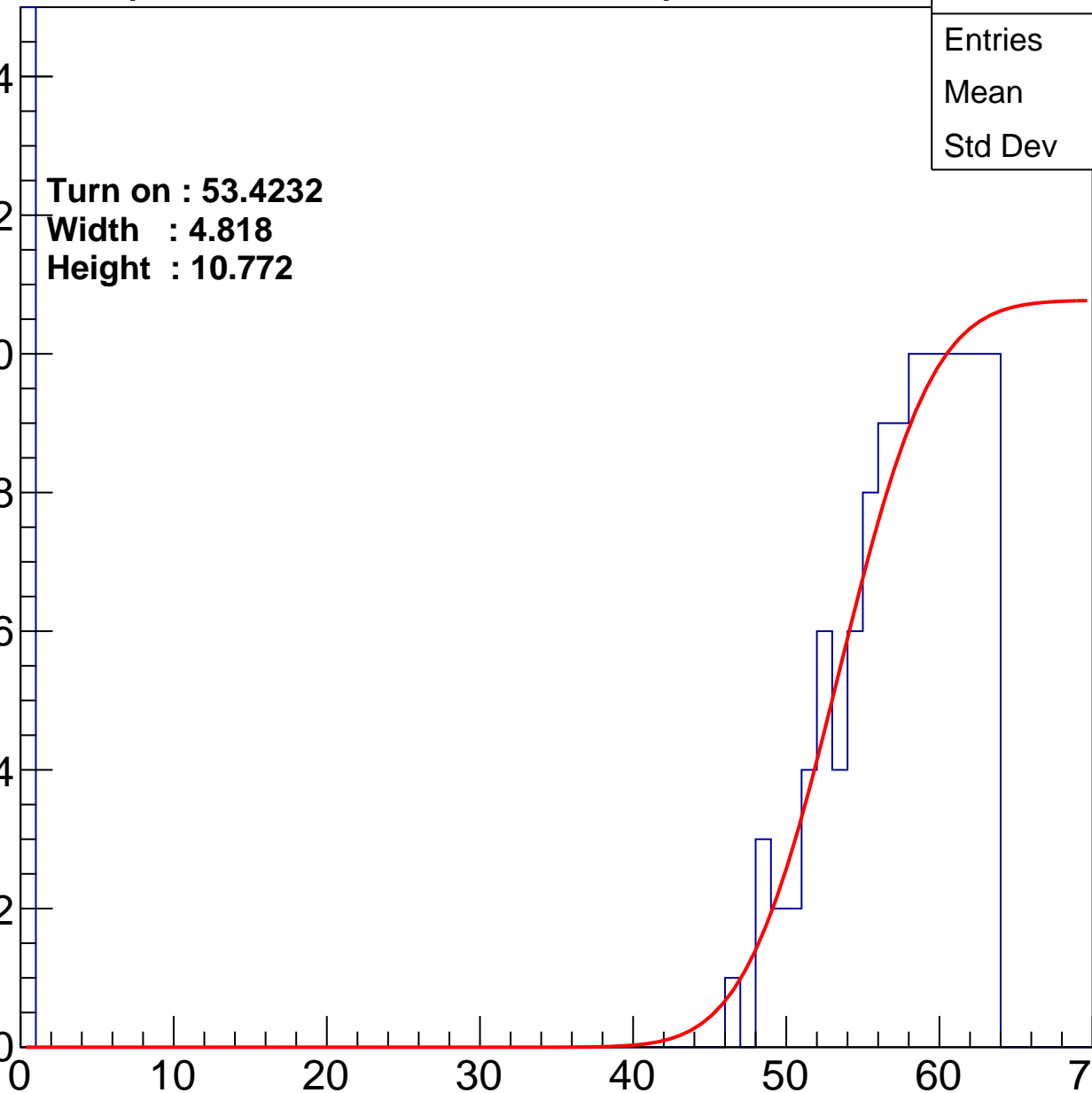
**Width : 4.818**

**Height : 10.772**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L104S, U3-ch99

calib\_packv5\_033123\_0516.root, FC#4, port A1

Entries	177
Mean	29.15
Std Dev	29.41

**Turn on : 56.0646**

**Width : 1.629**

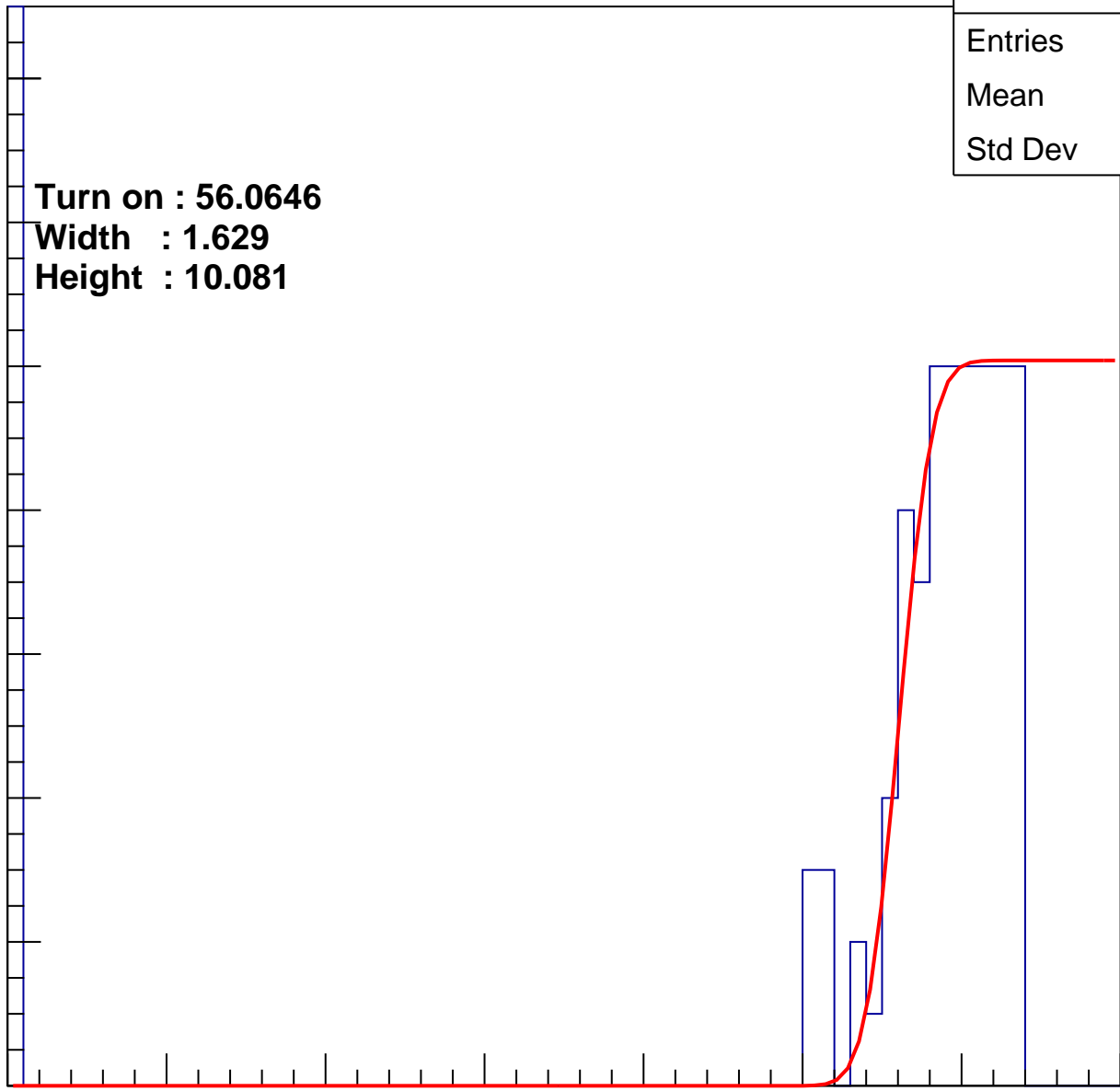
**Height : 10.081**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L104S, U3-ch100

calib\_packv5\_033123\_0516.root, FC#4, port A1

Entries	239
Mean	28.57
Std Dev	28.62

**Turn on : 52.2555**

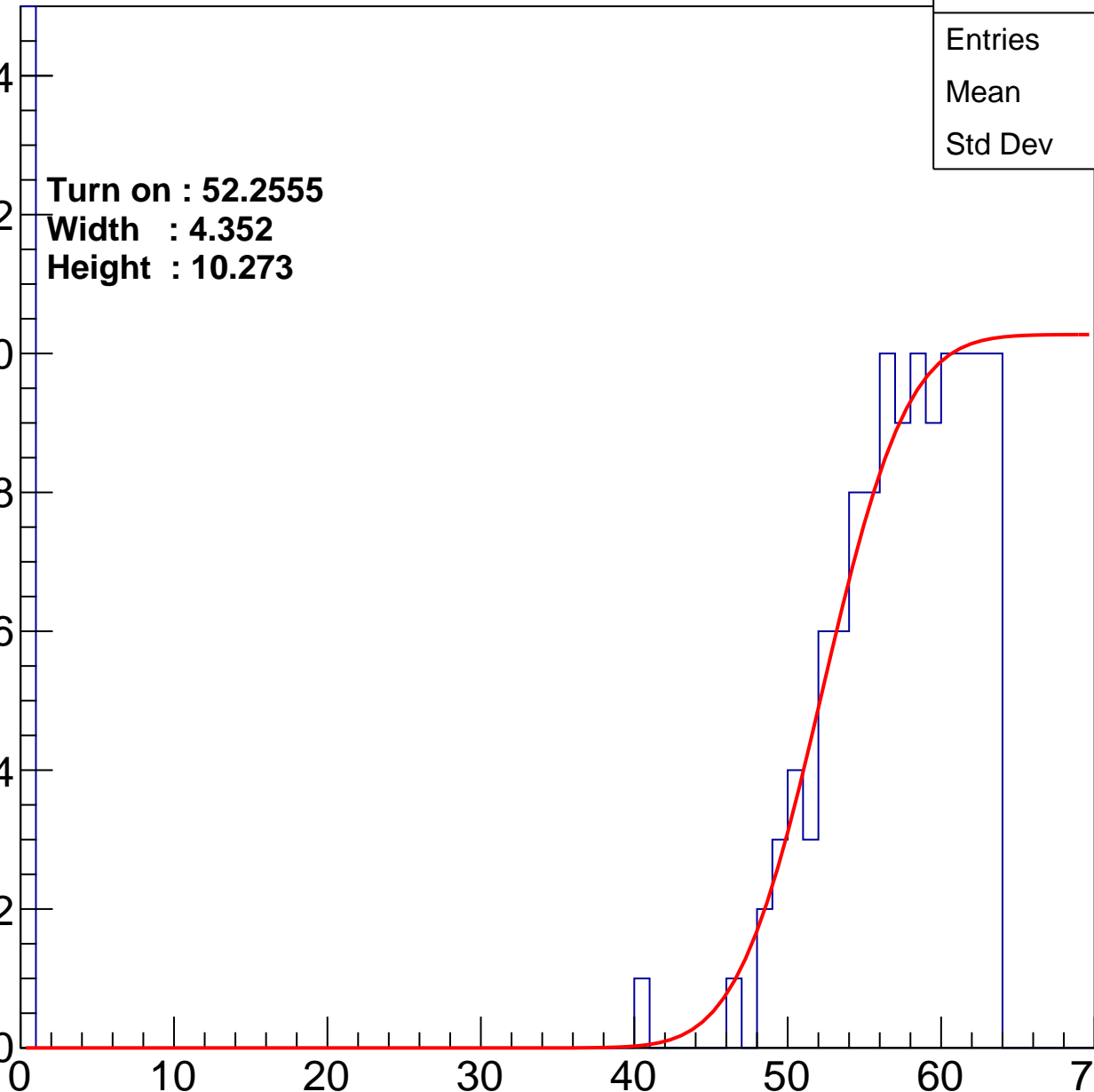
**Width : 4.352**

**Height : 10.273**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L104S, U3-ch101

calib\_packv5\_033123\_0516.root, FC#4, port A1

Entries	216
Mean	28.05
Std Dev	28.97

**Turn on : 53.8269**

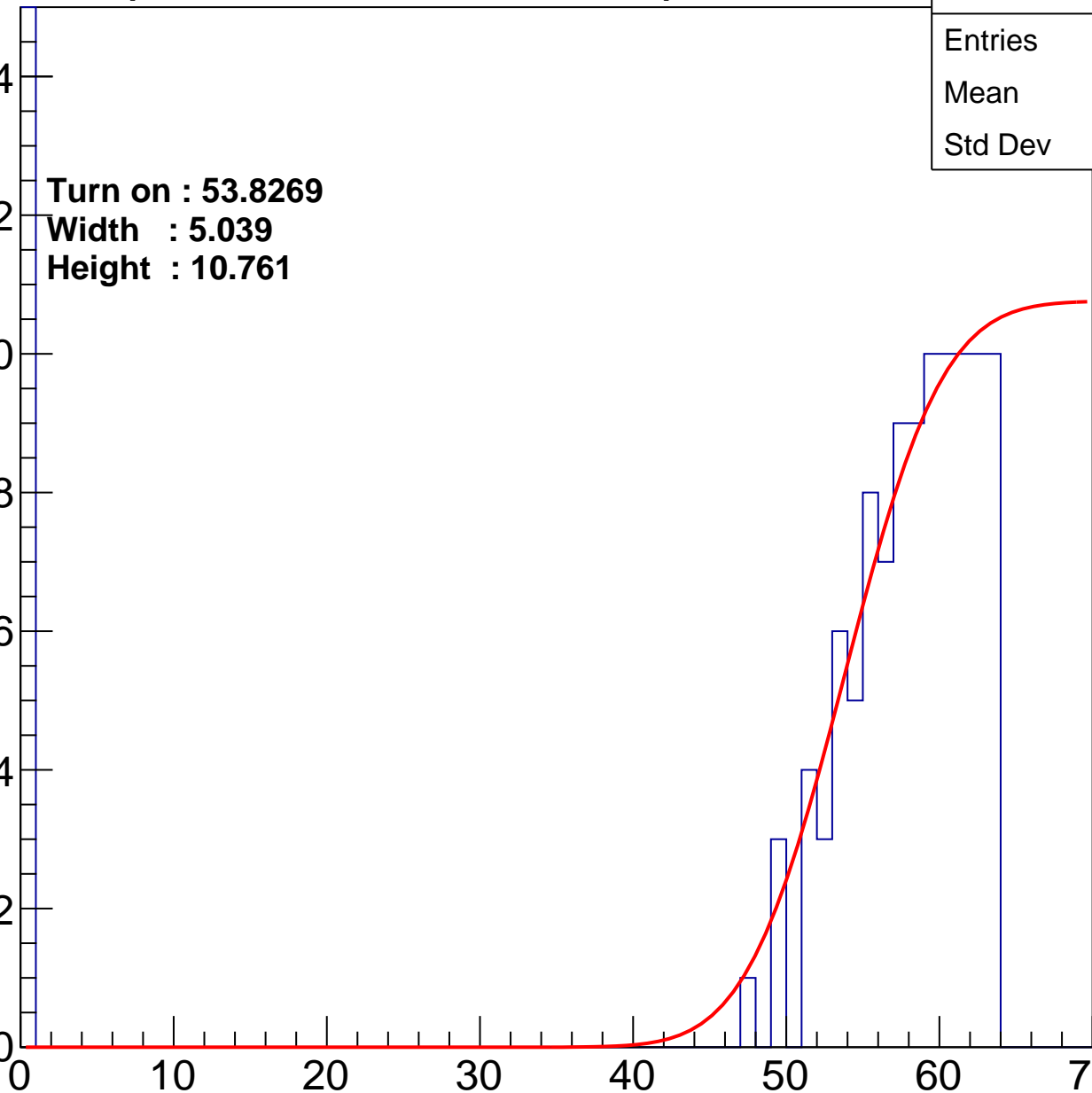
**Width : 5.039**

**Height : 10.761**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L104S, U3-ch102

calib\_packv5\_033123\_0516.root, FC#4, port A1

Entries	235
Mean	31.86
Std Dev	28.13

Turn on : 51.7644

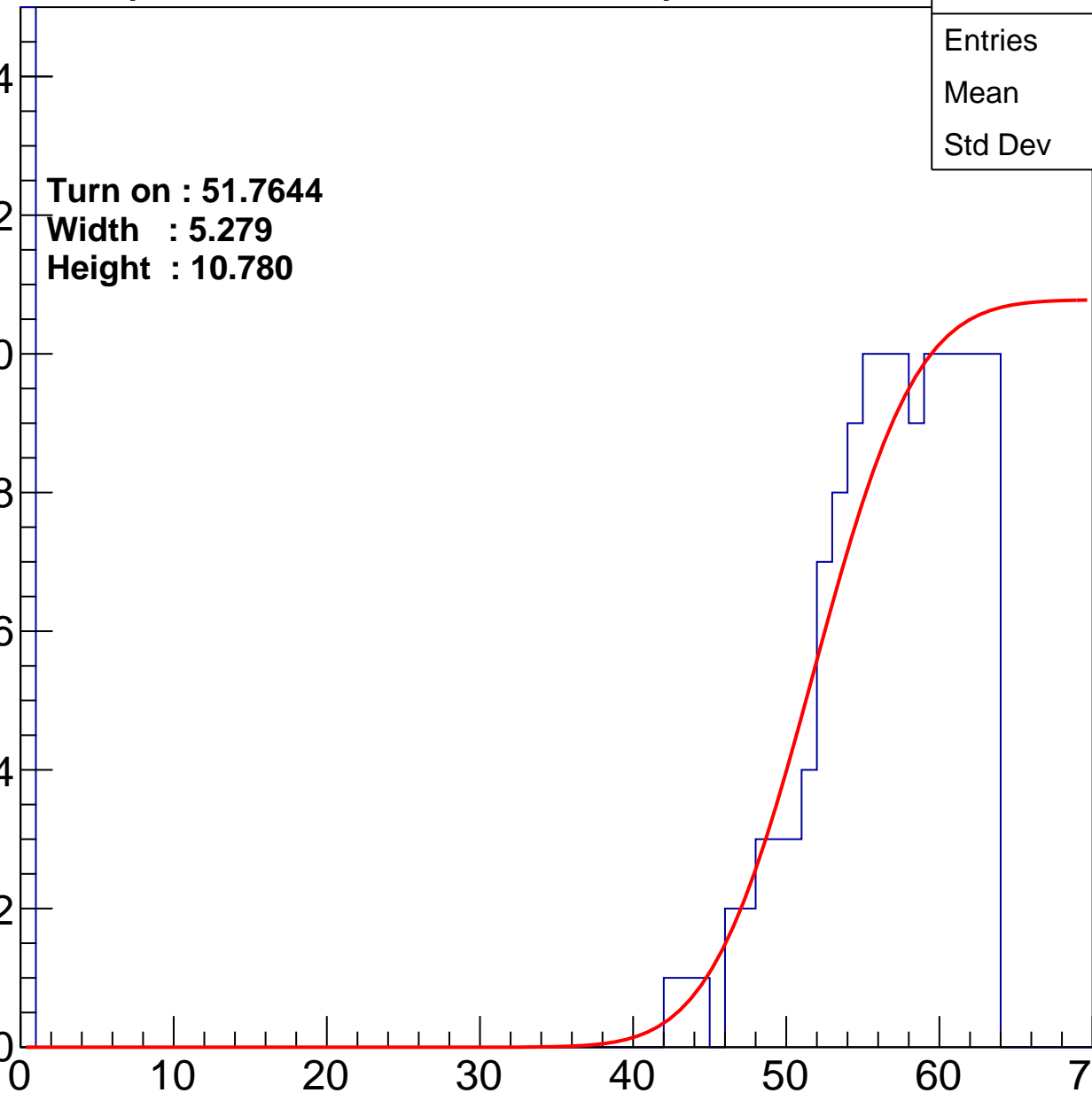
Width : 5.279

Height : 10.780

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L104S, U3-ch103

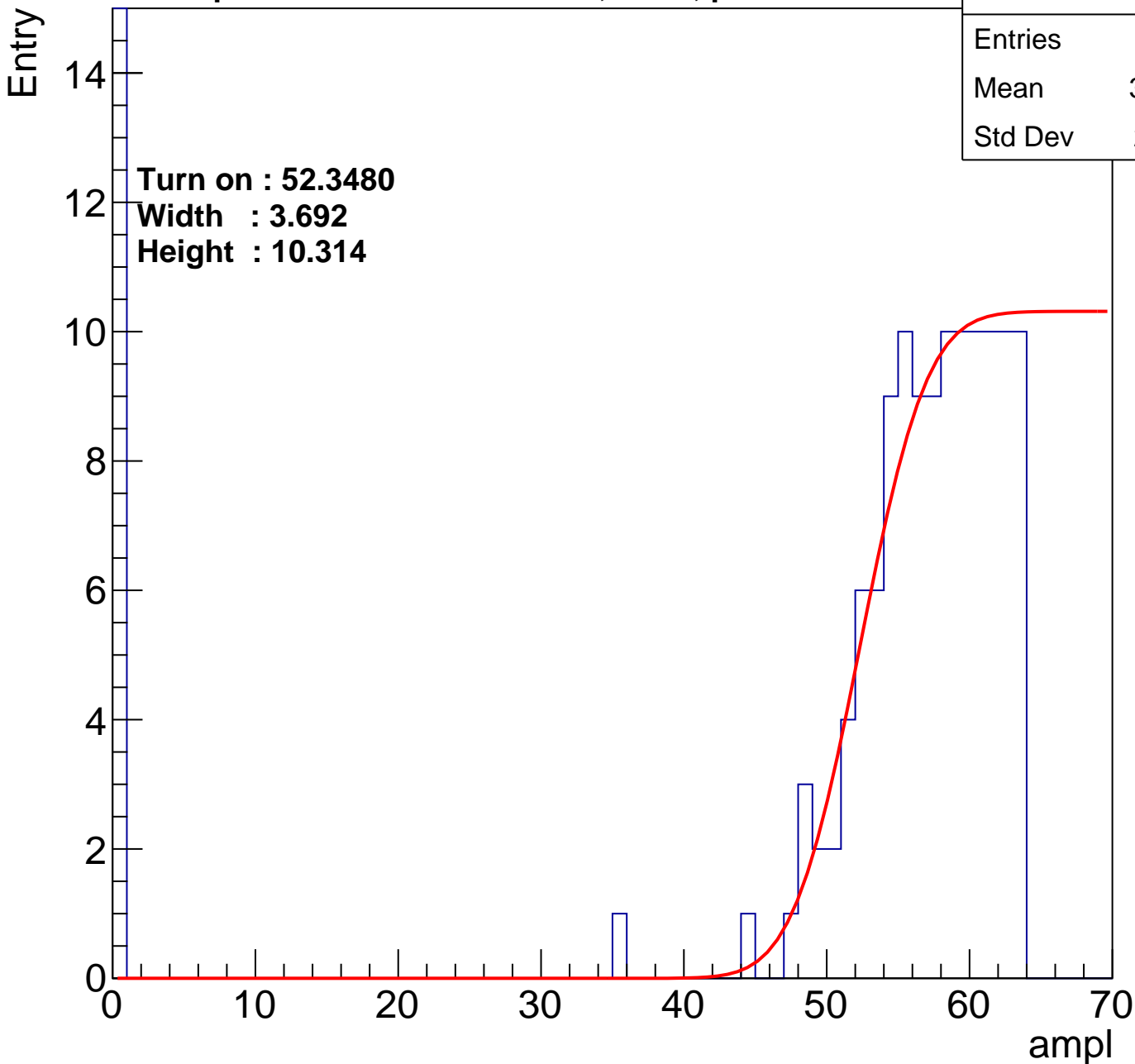
calib\_packv5\_033123\_0516.root, FC#4, port A1

Entries	220
Mean	31.75
Std Dev	28.41

Turn on : 52.3480

Width : 3.692

Height : 10.314



# B1L104S, U3-ch104

calib\_packv5\_033123\_0516.root, FC#4, port A1

Entries	203
Mean	31.69
Std Dev	28.7

**Turn on : 53.3889**

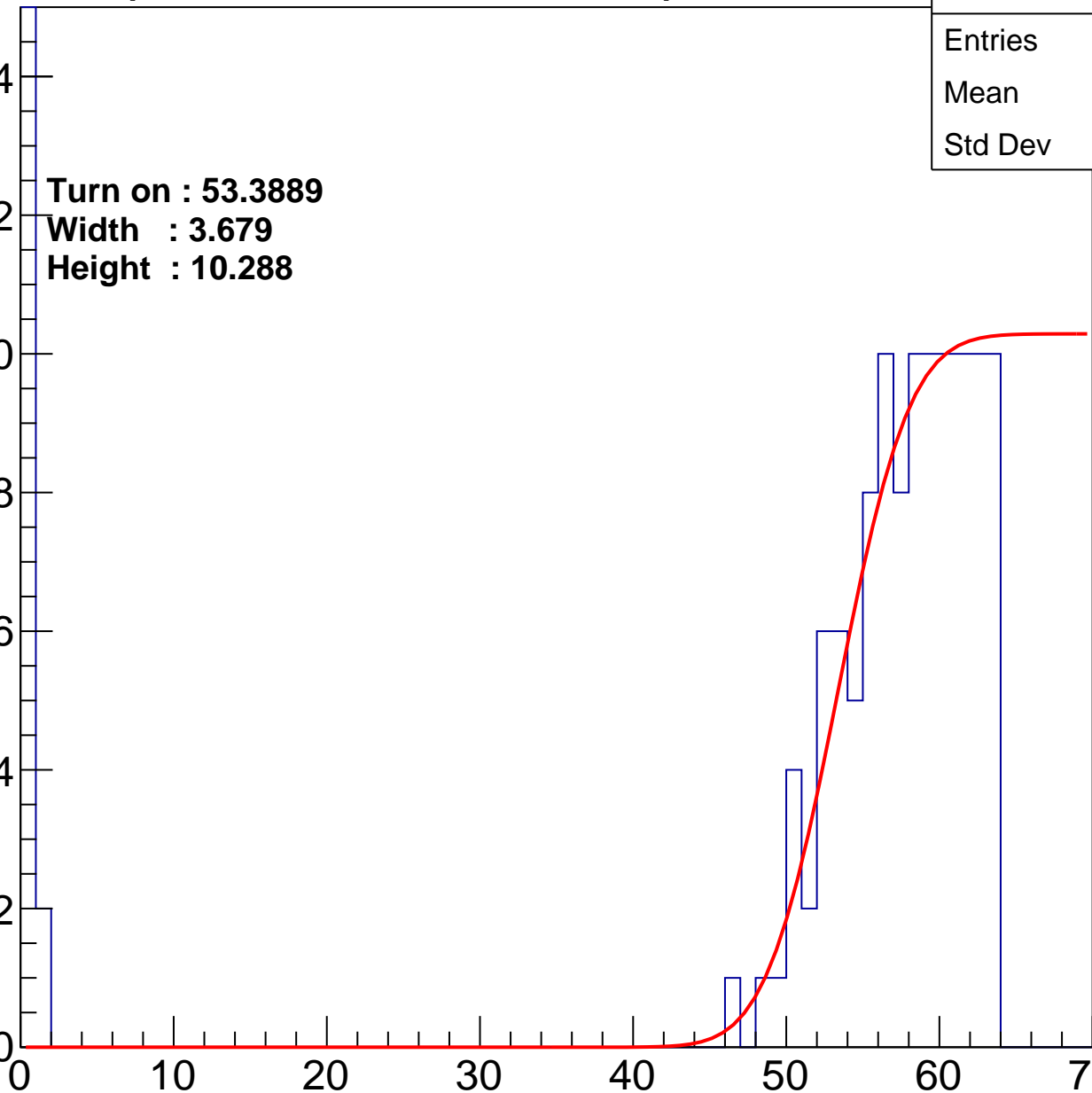
**Width : 3.679**

**Height : 10.288**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L104S, U3-ch105

calib\_packv5\_033123\_0516.root, FC#4, port A1

Entries	167
Mean	35.96
Std Dev	28.16

**Turn on : 53.7509**

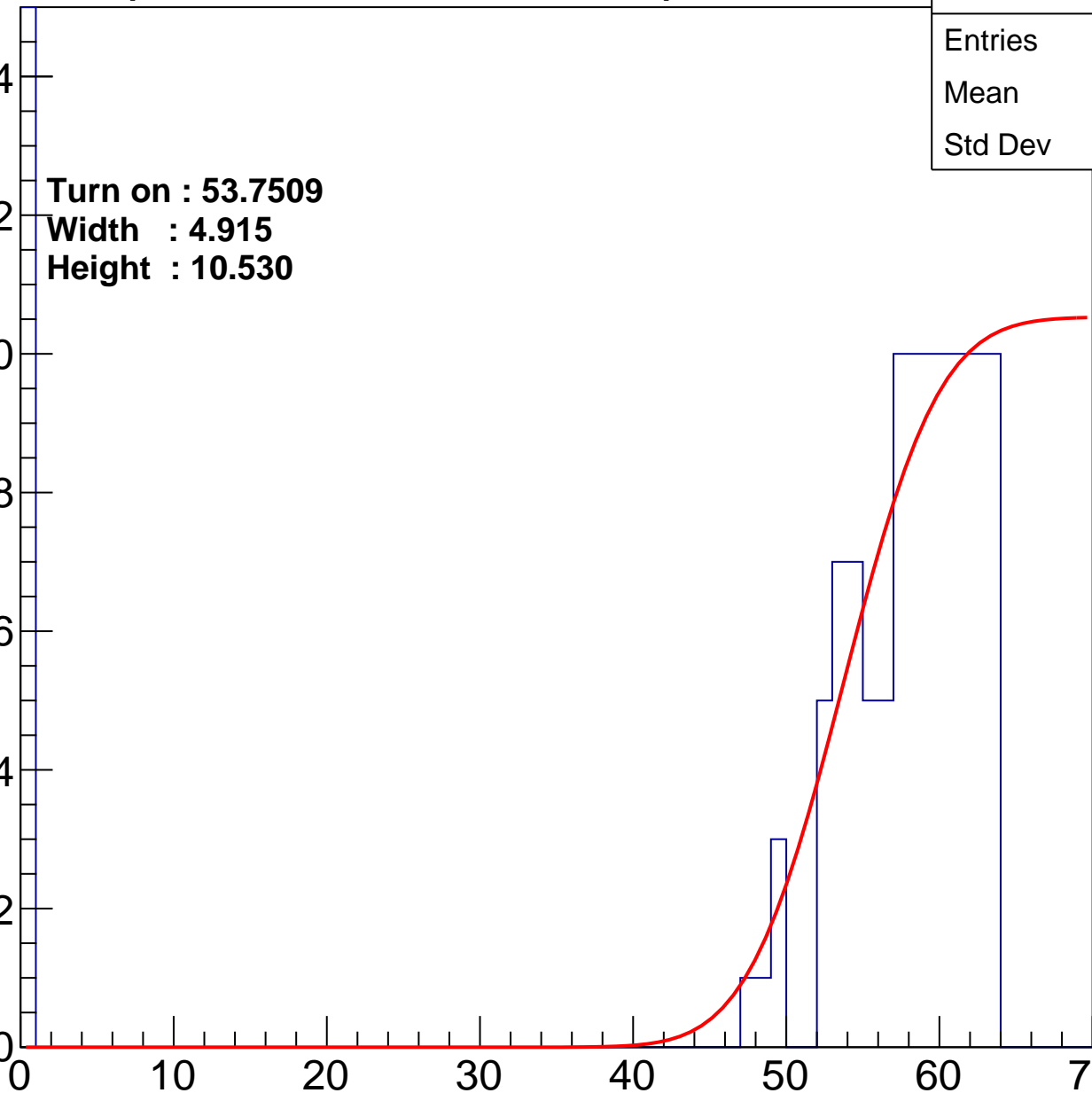
**Width : 4.915**

**Height : 10.530**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L104S, U3-ch106

calib\_packv5\_033123\_0516.root, FC#4, port A1

Entries	209
Mean	29.01
Std Dev	28.99

**Turn on : 53.4780**

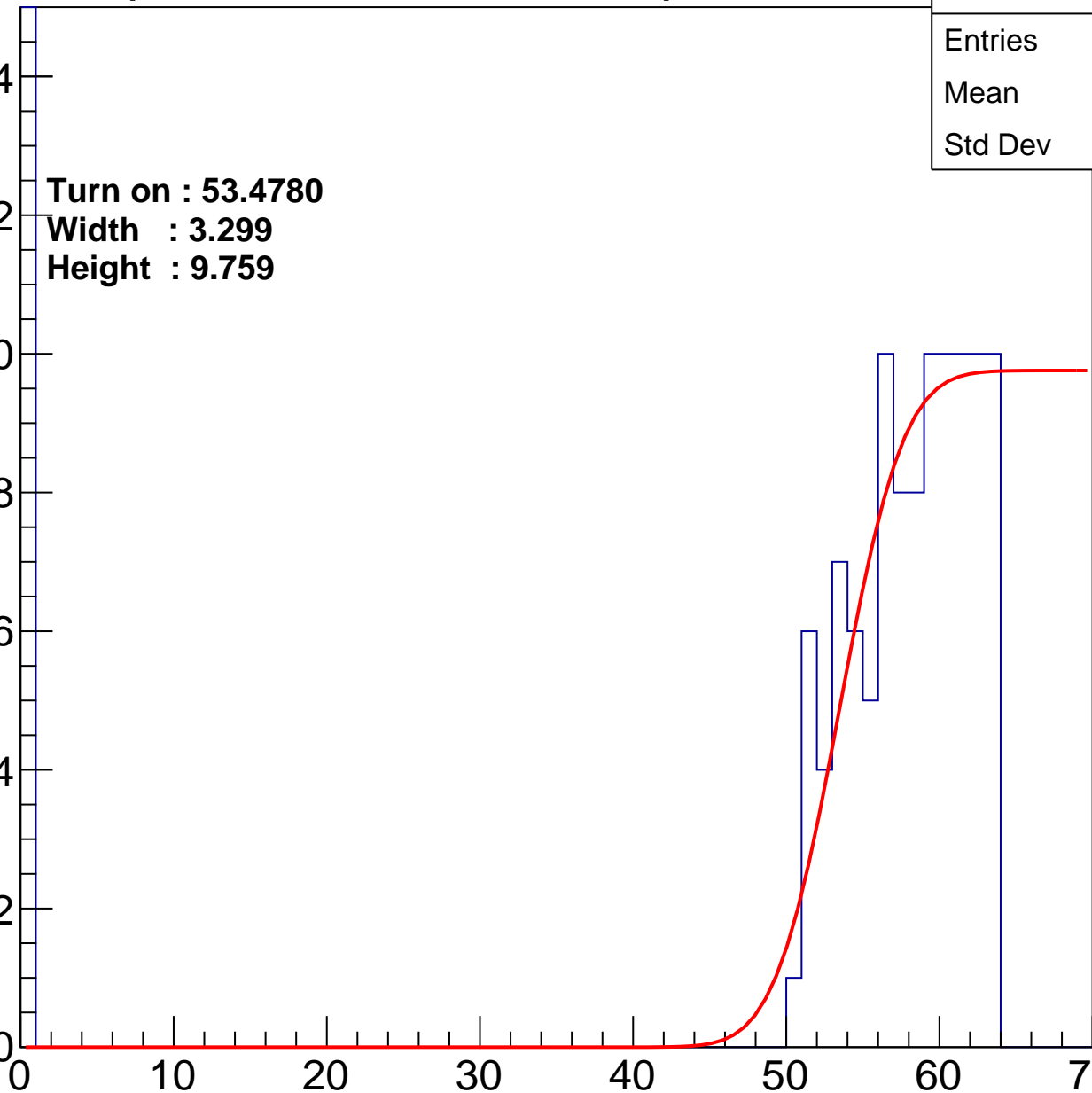
**Width : 3.299**

**Height : 9.759**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L104S, U3-ch107

calib\_packv5\_033123\_0516.root, FC#4, port A1

Entries	206
Mean	34.94
Std Dev	27.77

Turn on : 52.0822

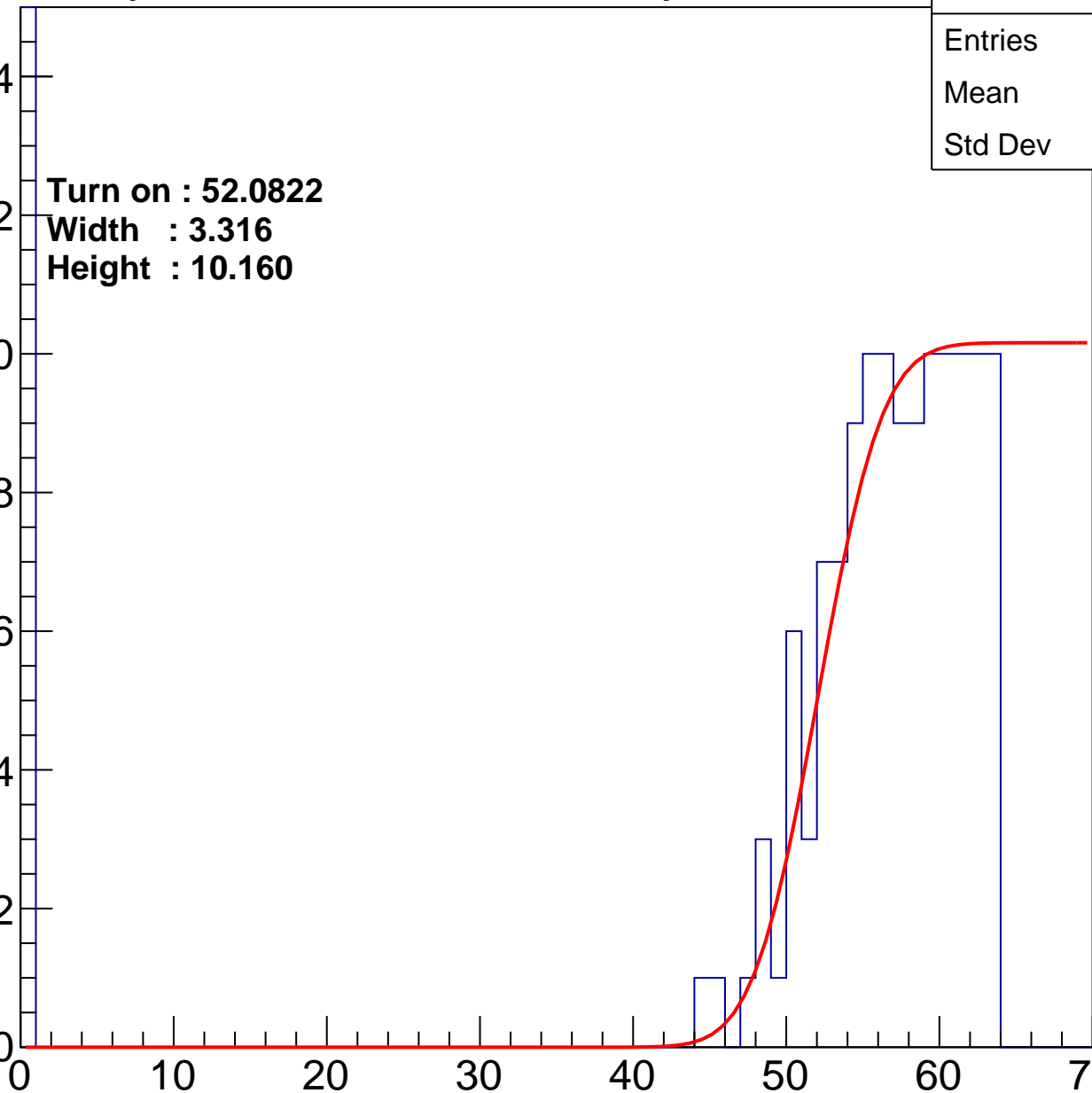
Width : 3.316

Height : 10.160

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L104S, U3-ch108

calib\_packv5\_033123\_0516.root, FC#4, port A1

Entries	219
Mean	28.72
Std Dev	28.75

**Turn on : 53.6838**

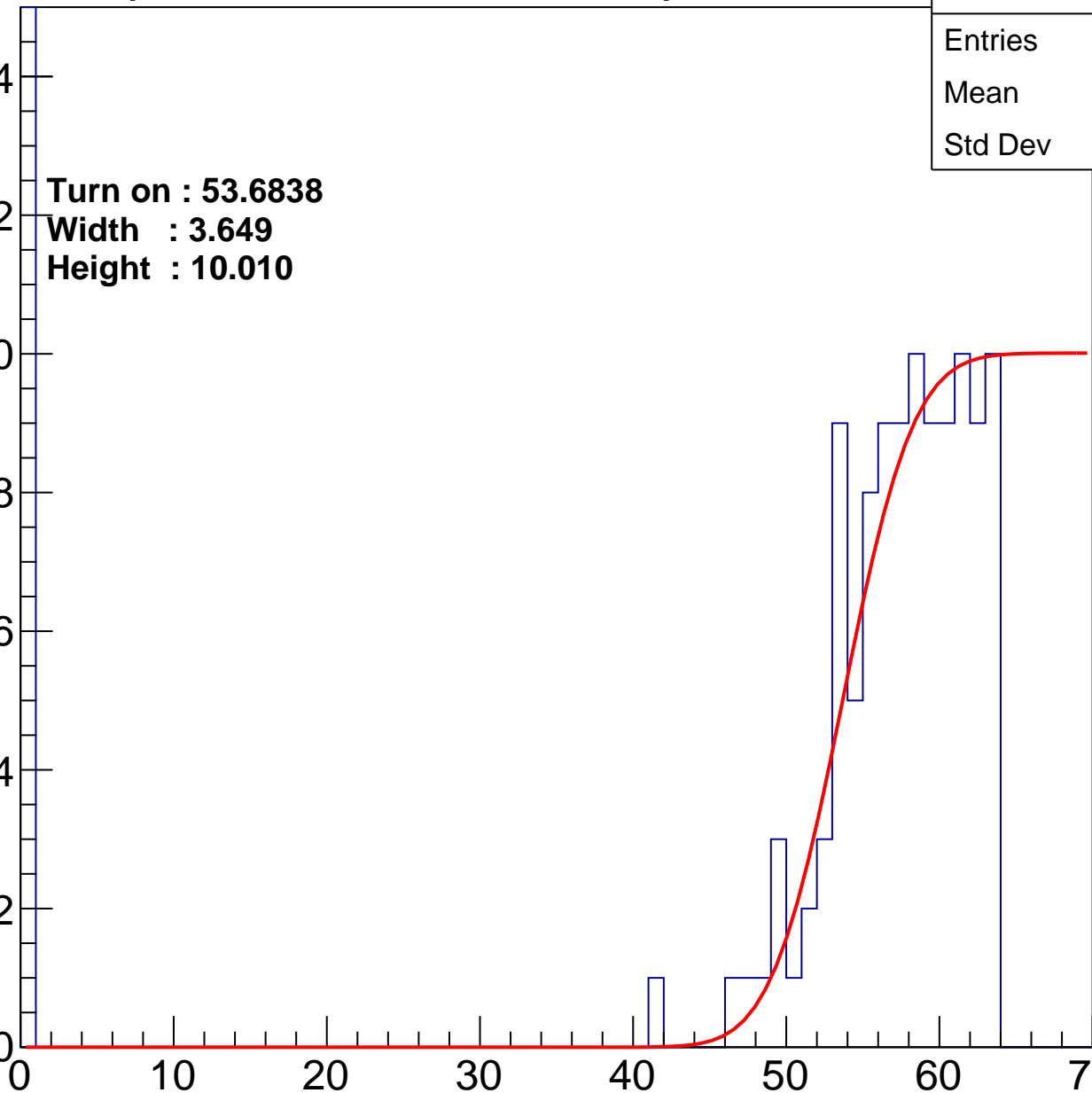
**Width : 3.649**

**Height : 10.010**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L104S, U3-ch109

calib\_packv5\_033123\_0516.root, FC#4, port A1

Entries	208
Mean	31.23
Std Dev	28.77

**Turn on : 53.5227**

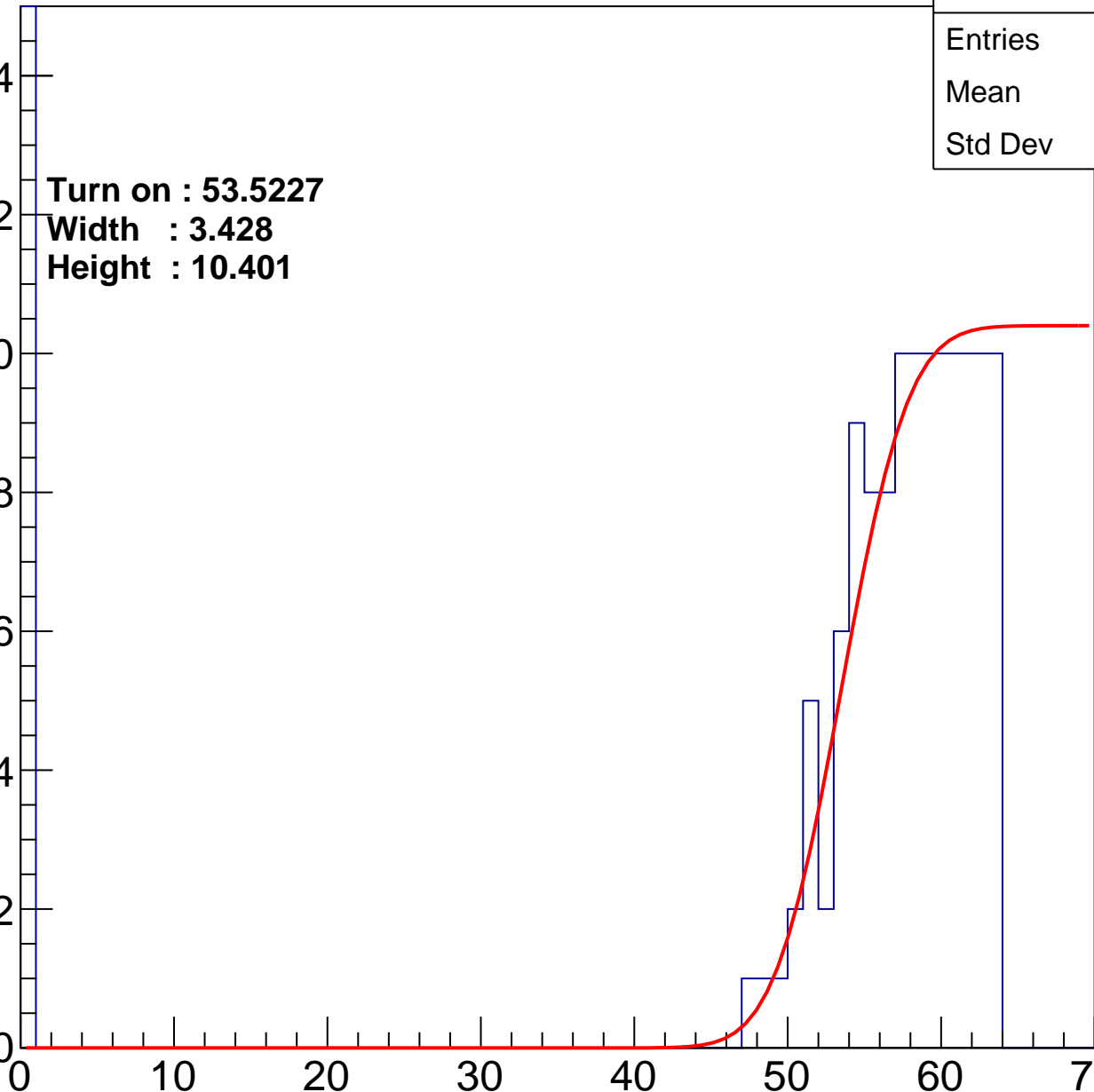
**Width : 3.428**

**Height : 10.401**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L104S, U3-ch110

calib\_packv5\_033123\_0516.root, FC#4, port A1

Entries	223
Mean	33.68
Std Dev	27.92

**Turn on : 50.9713**

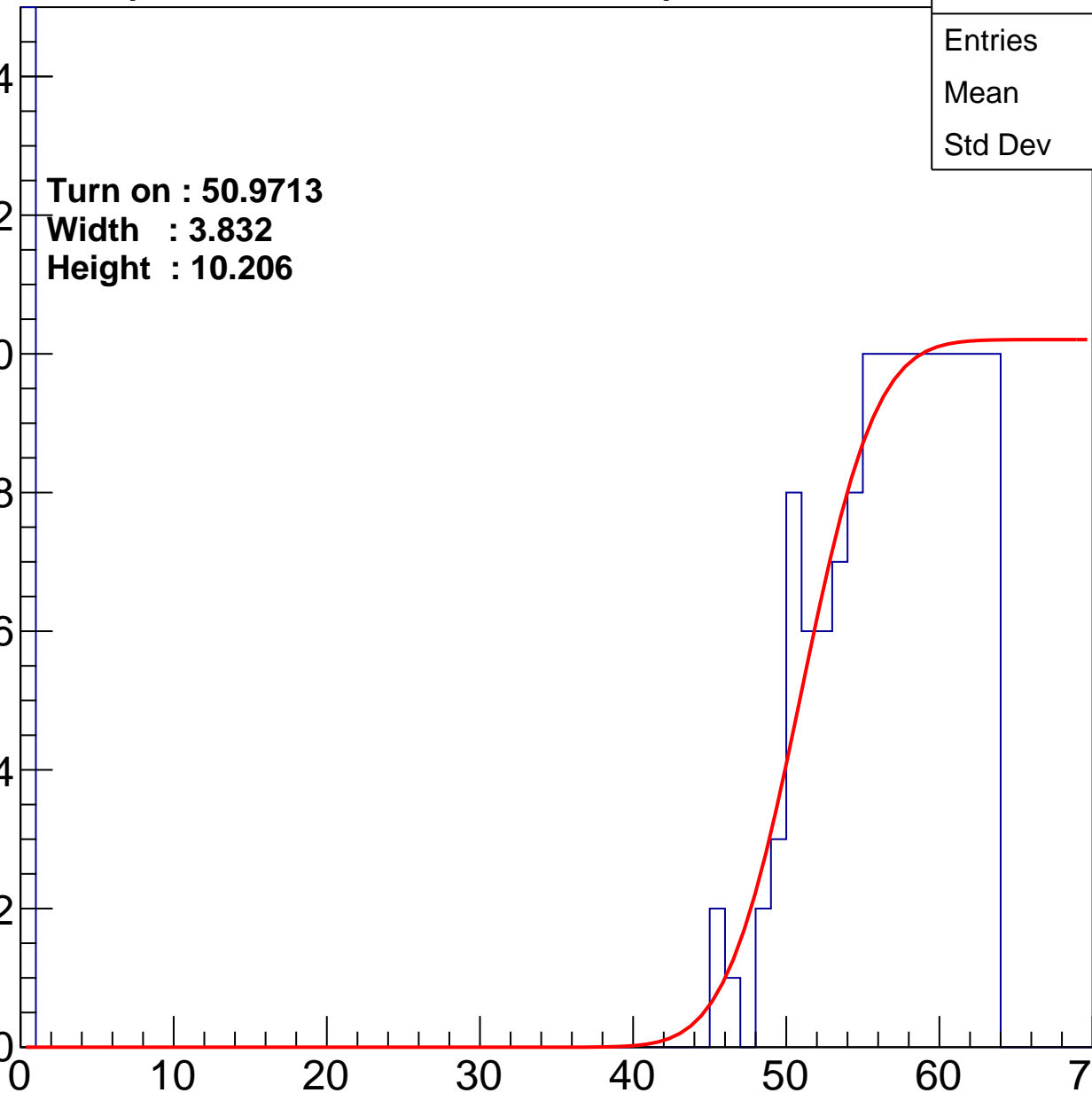
**Width : 3.832**

**Height : 10.206**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L104S, U3-ch111

calib\_packv5\_033123\_0516.root, FC#4, port A1

Entries	204
Mean	32.23
Std Dev	28.53

Turn on : 54.1331

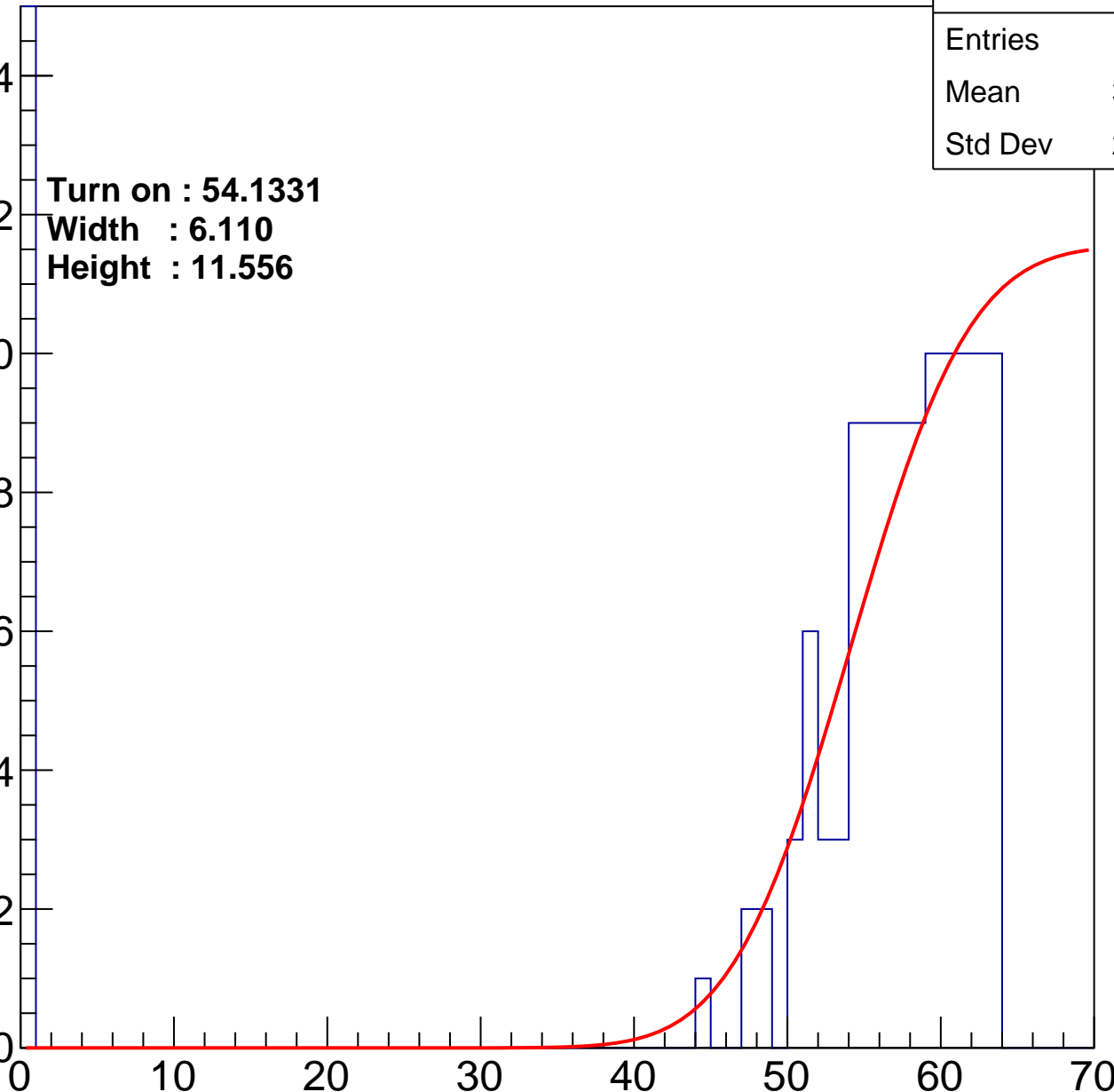
Width : 6.110

Height : 11.556

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L104S, U3-ch112

calib\_packv5\_033123\_0516.root, FC#4, port A1

Entries	240
Mean	29.08
Std Dev	28.53

**Turn on : 51.5880**

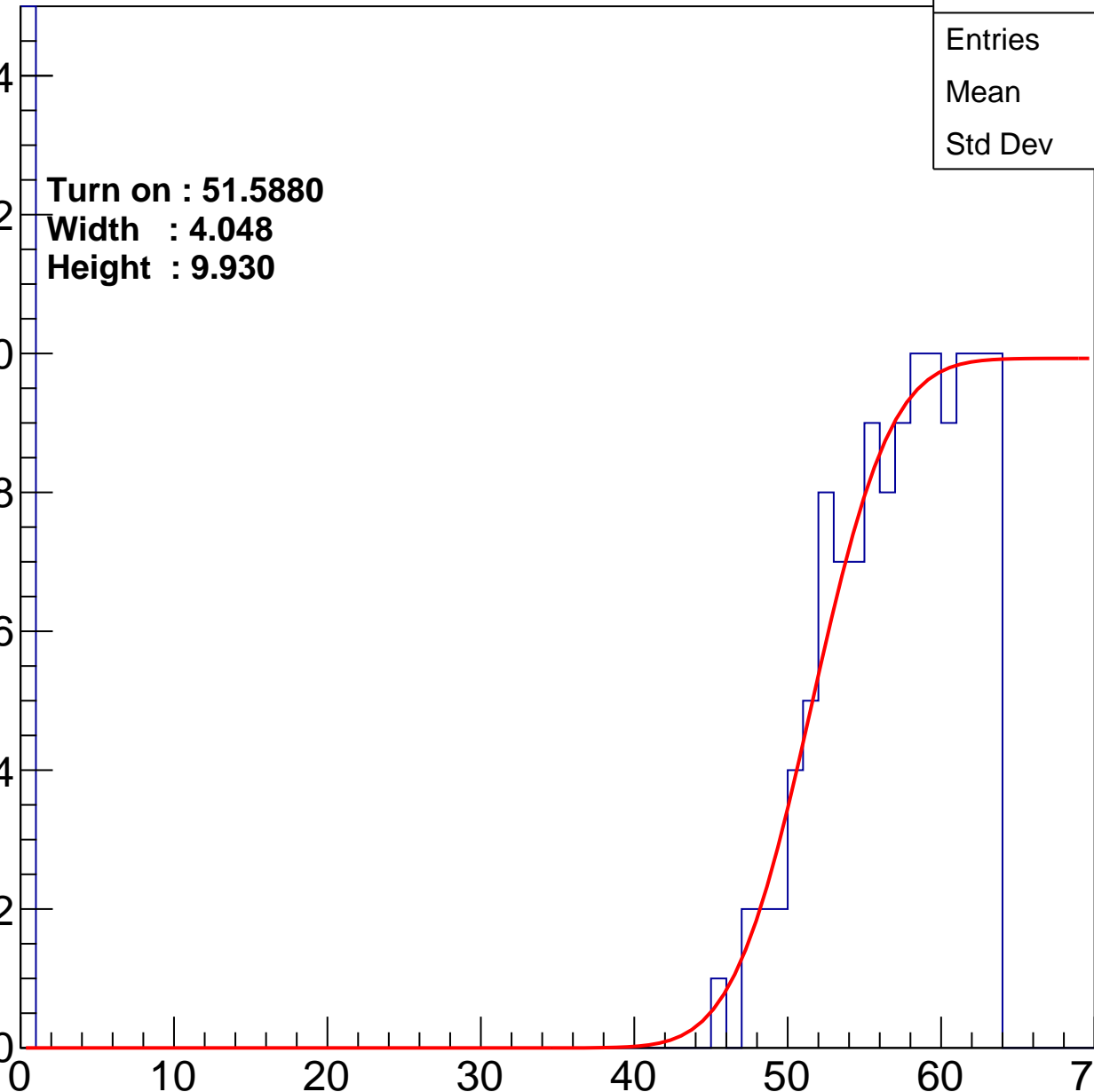
**Width : 4.048**

**Height : 9.930**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L104S, U3-ch113

calib\_packv5\_033123\_0516.root, FC#4, port A1

Entries	196
Mean	33.62
Std Dev	28.38

**Turn on : 53.1243**

**Width : 4.924**

**Height : 10.753**

Entry

14

12

10

8

6

4

2

0

0

10

20

30

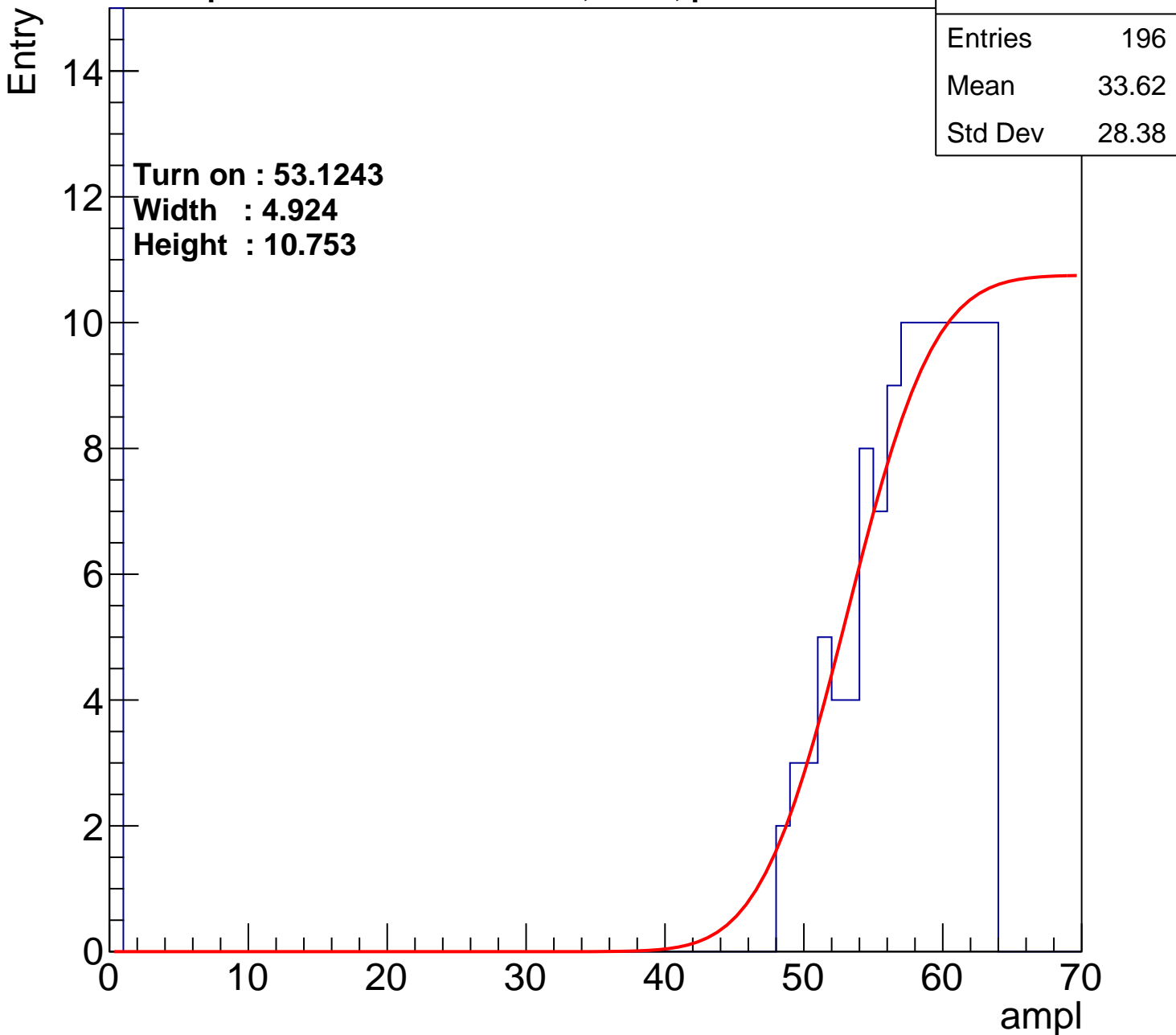
40

50

60

70

ampl



# B1L104S, U3-ch114

calib\_packv5\_033123\_0516.root, FC#4, port A1

Entries	224
Mean	33.53
Std Dev	27.96

Turn on : 51.2190

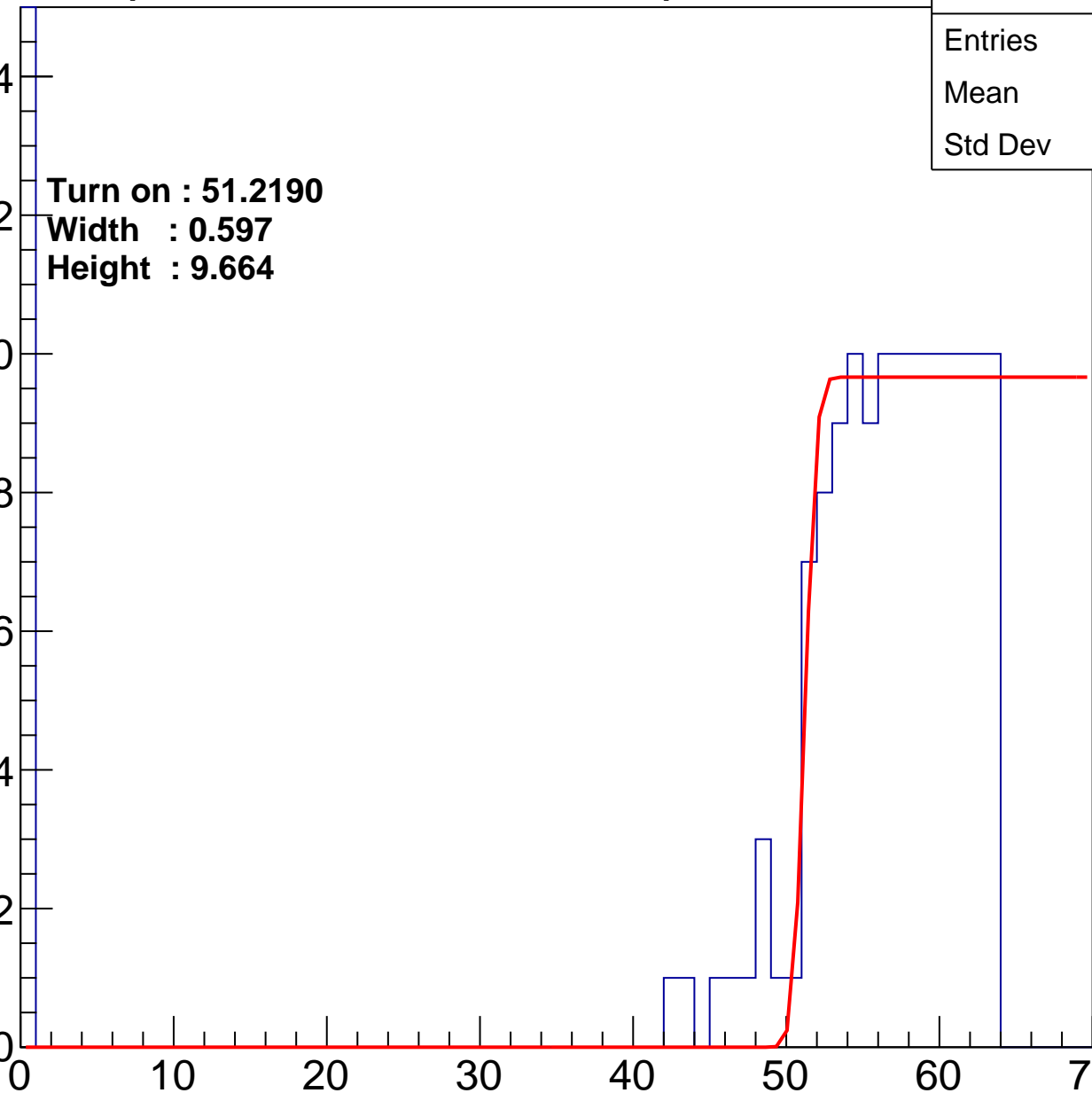
Width : 0.597

Height : 9.664

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L104S, U3-ch115

calib\_packv5\_033123\_0516.root, FC#4, port A1

Entries	167
Mean	33.16
Std Dev	28.98

Turn on : 55.4928

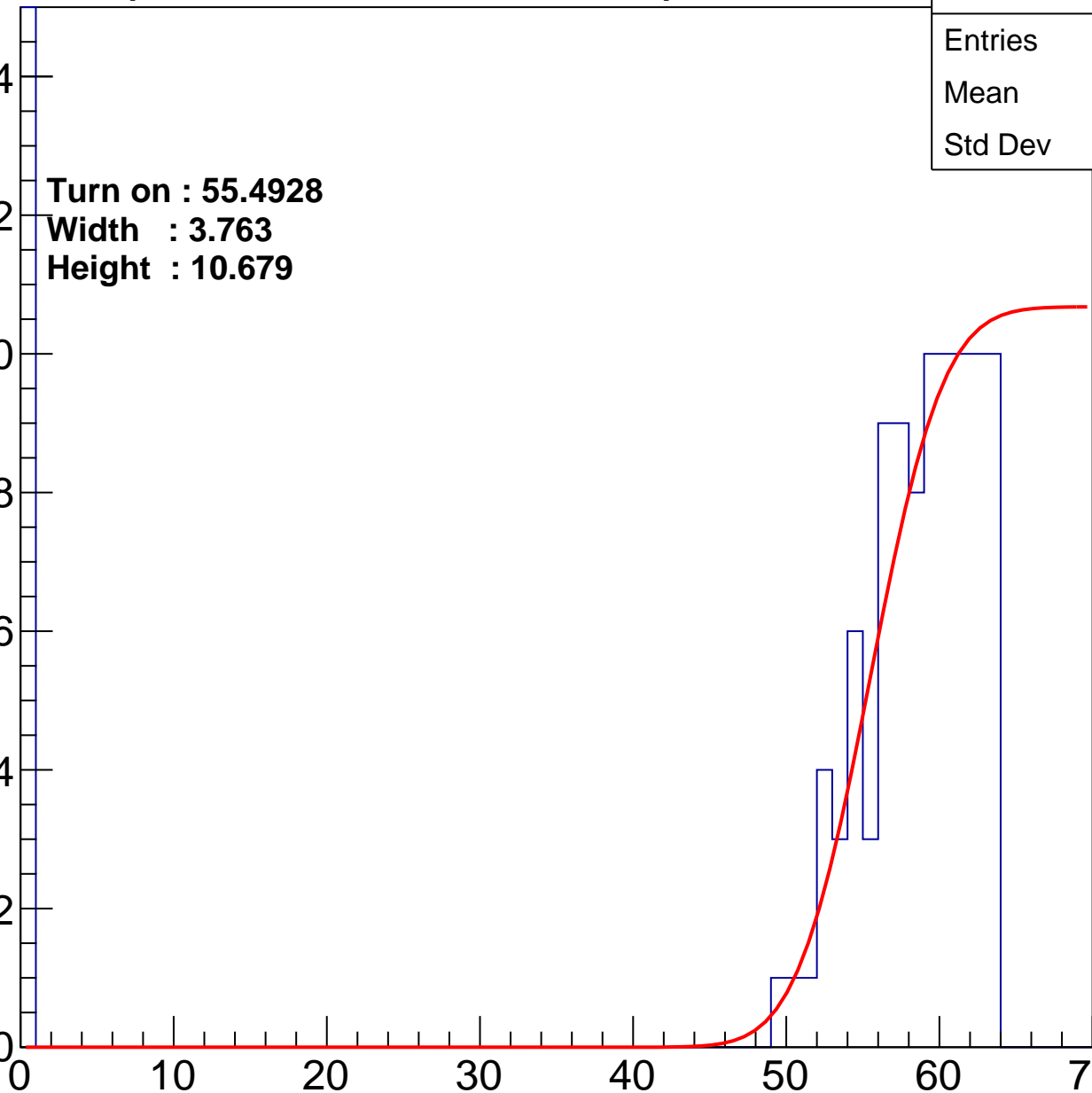
Width : 3.763

Height : 10.679

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L104S, U3-ch116

calib\_packv5\_033123\_0516.root, FC#4, port A1

Entries	200
Mean	32.58
Std Dev	28.48

**Turn on : 53.0457**

**Width : 5.486**

**Height : 10.760**

Entry

14

12

10

8

6

4

2

0

0

10

20

30

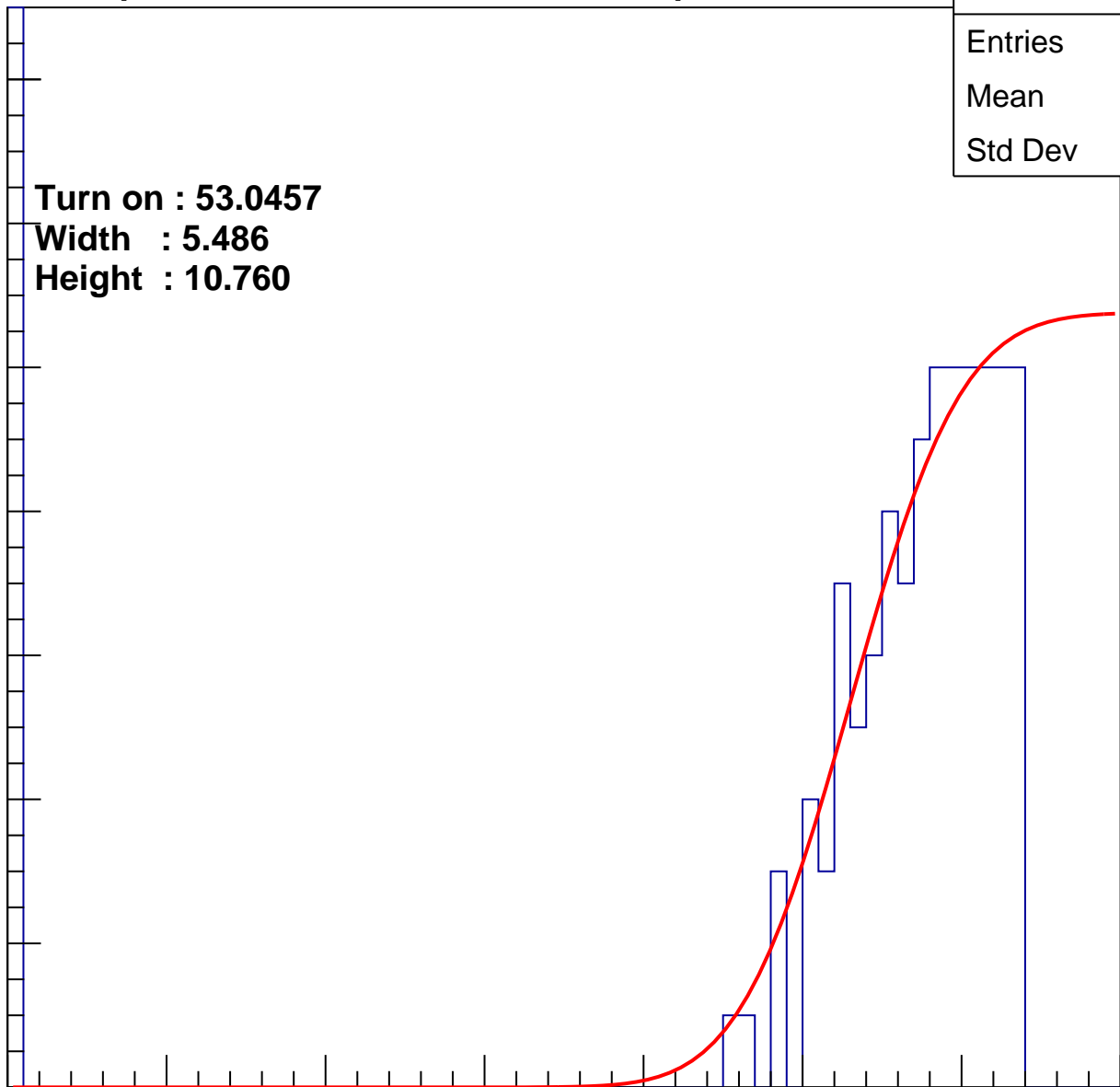
40

50

60

70

ampl



# B1L104S, U3-ch117

calib\_packv5\_033123\_0516.root, FC#4, port A1

Entries	192
Mean	35.64
Std Dev	27.8

Turn on : 52.7139

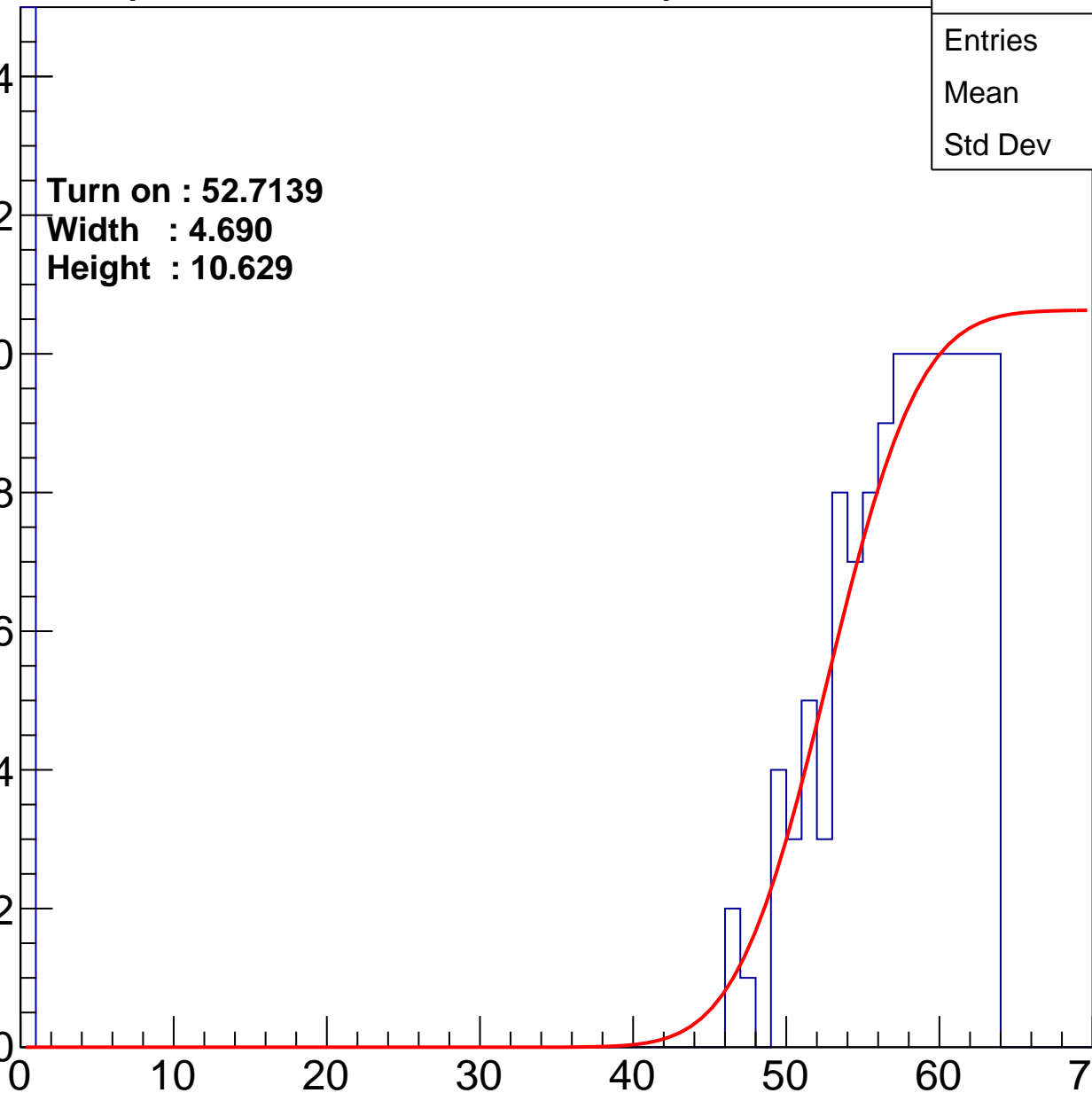
Width : 4.690

Height : 10.629

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L104S, U3-ch118

calib\_packv5\_033123\_0516.root, FC#4, port A1

Entries	216
Mean	34.28
Std Dev	27.83

**Turn on : 51.2879**

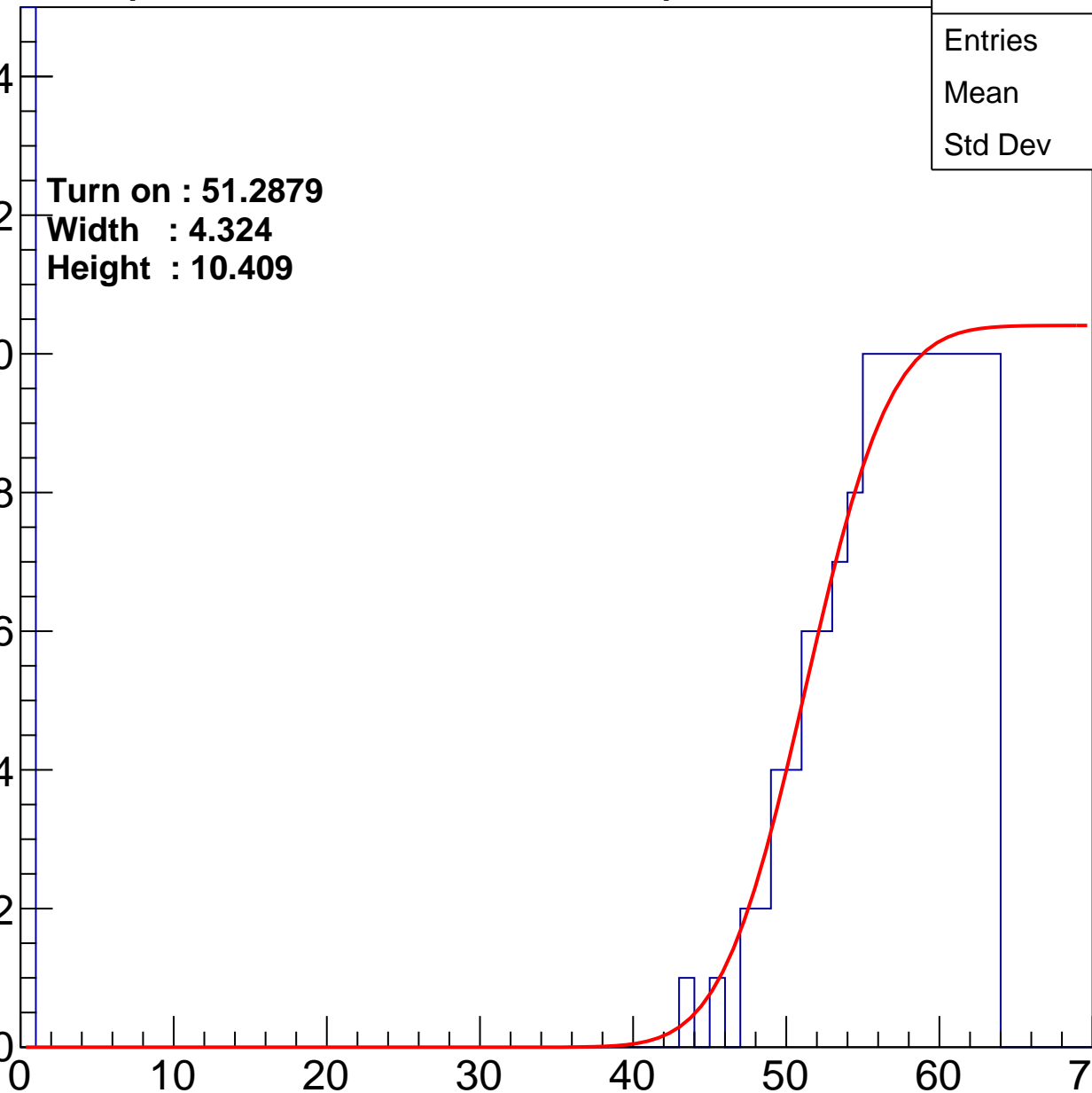
**Width : 4.324**

**Height : 10.409**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L104S, U3-ch119

calib\_packv5\_033123\_0516.root, FC#4, port A1

Entries	218
Mean	32.63
Std Dev	28.33

Turn on : 52.5346

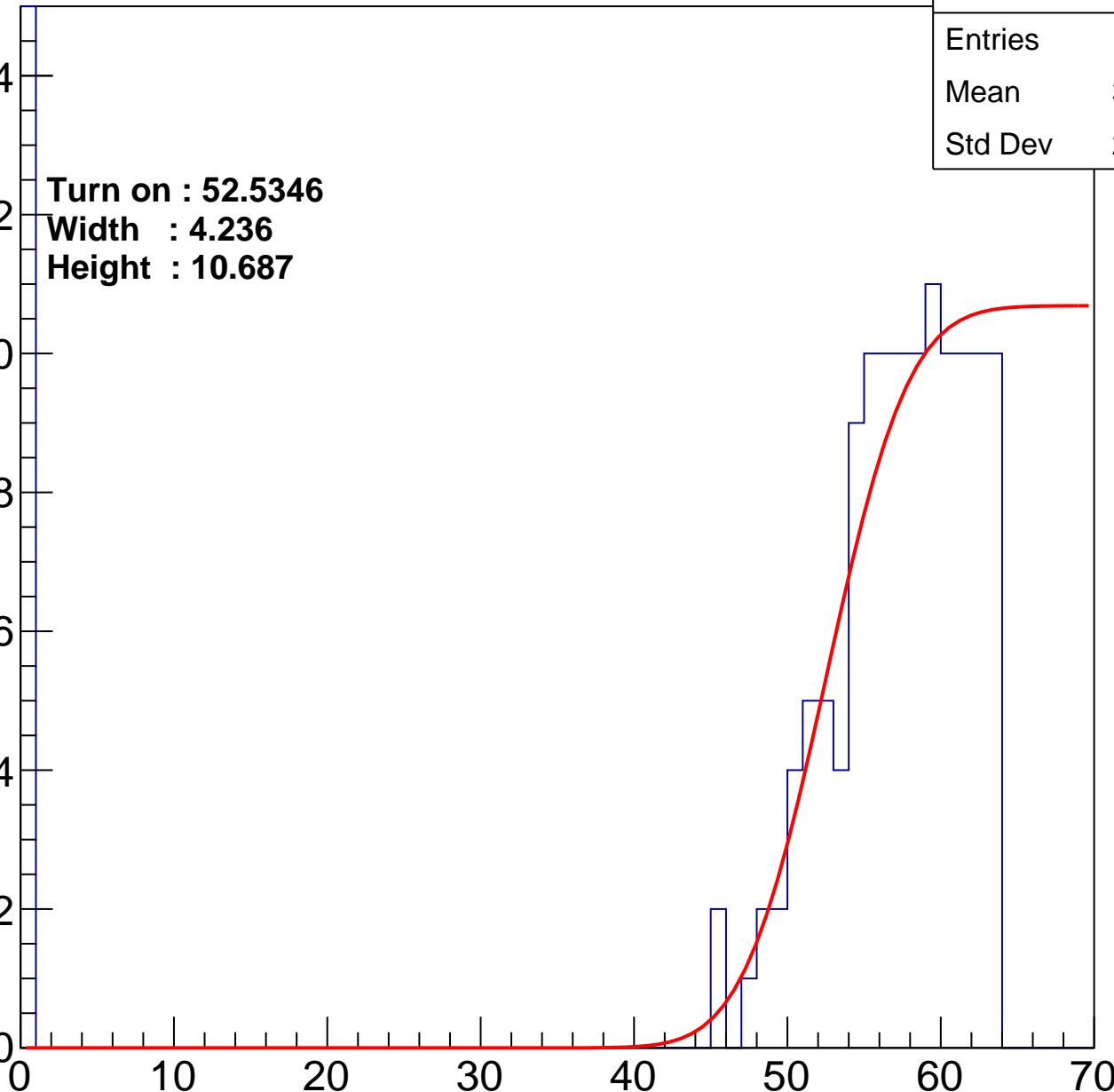
Width : 4.236

Height : 10.687

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L104S, U3-ch120

calib\_packv5\_033123\_0516.root, FC#4, port A1

Entries	227
Mean	31.44
Std Dev	27.95

Turn on : 52.4588

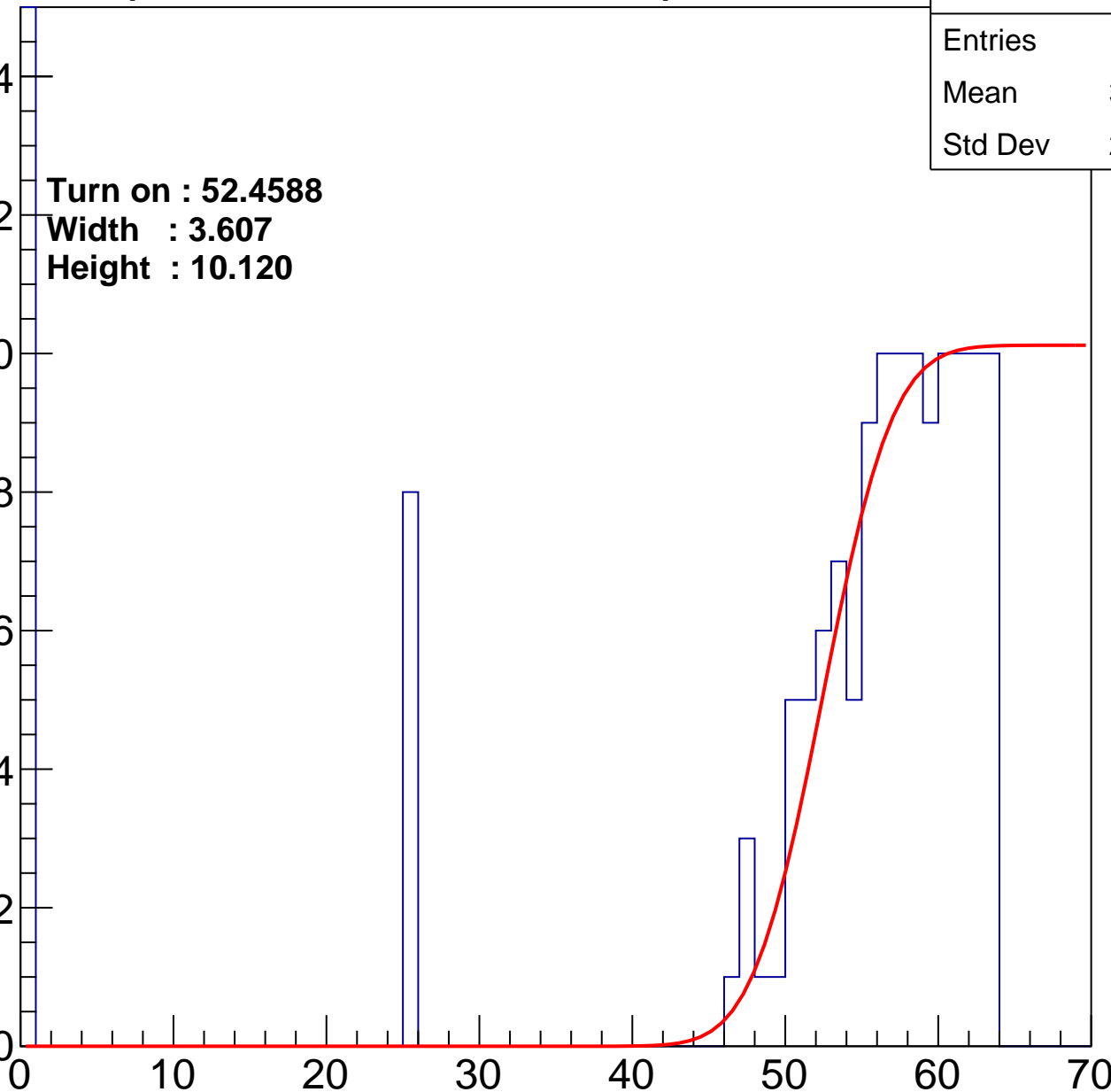
Width : 3.607

Height : 10.120

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L104S, U3-ch121

calib\_packv5\_033123\_0516.root, FC#4, port A1

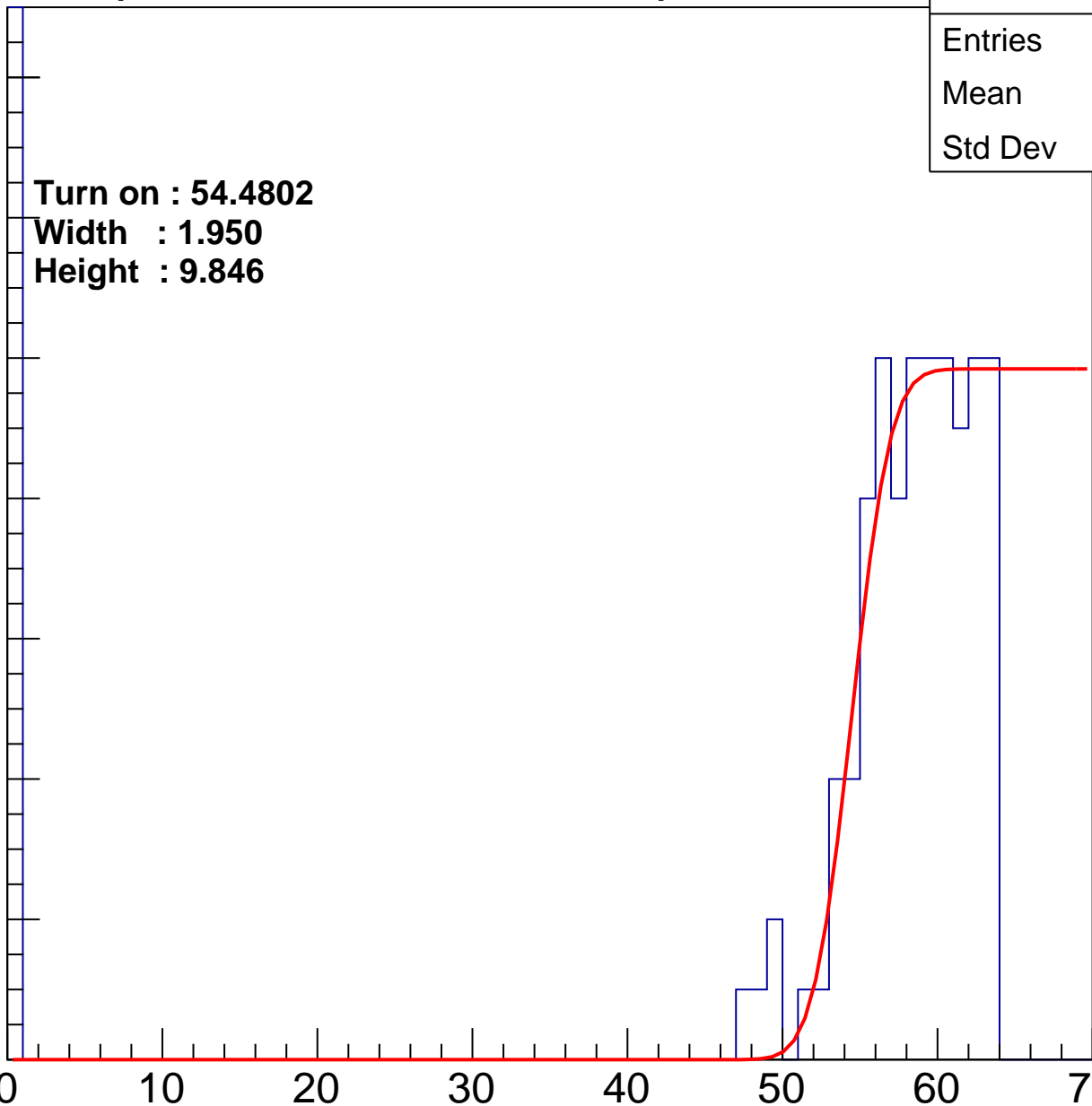
Entry

14  
12  
10  
8  
6  
4  
2  
0

Turn on : 54.4802  
Width : 1.950  
Height : 9.846

Entries	191
Mean	30.1
Std Dev	29.13

ampl



# B1L104S, U3-ch122

calib\_packv5\_033123\_0516.root, FC#4, port A1

Entries	214
Mean	31.81
Std Dev	28.36

**Turn on : 52.4642**

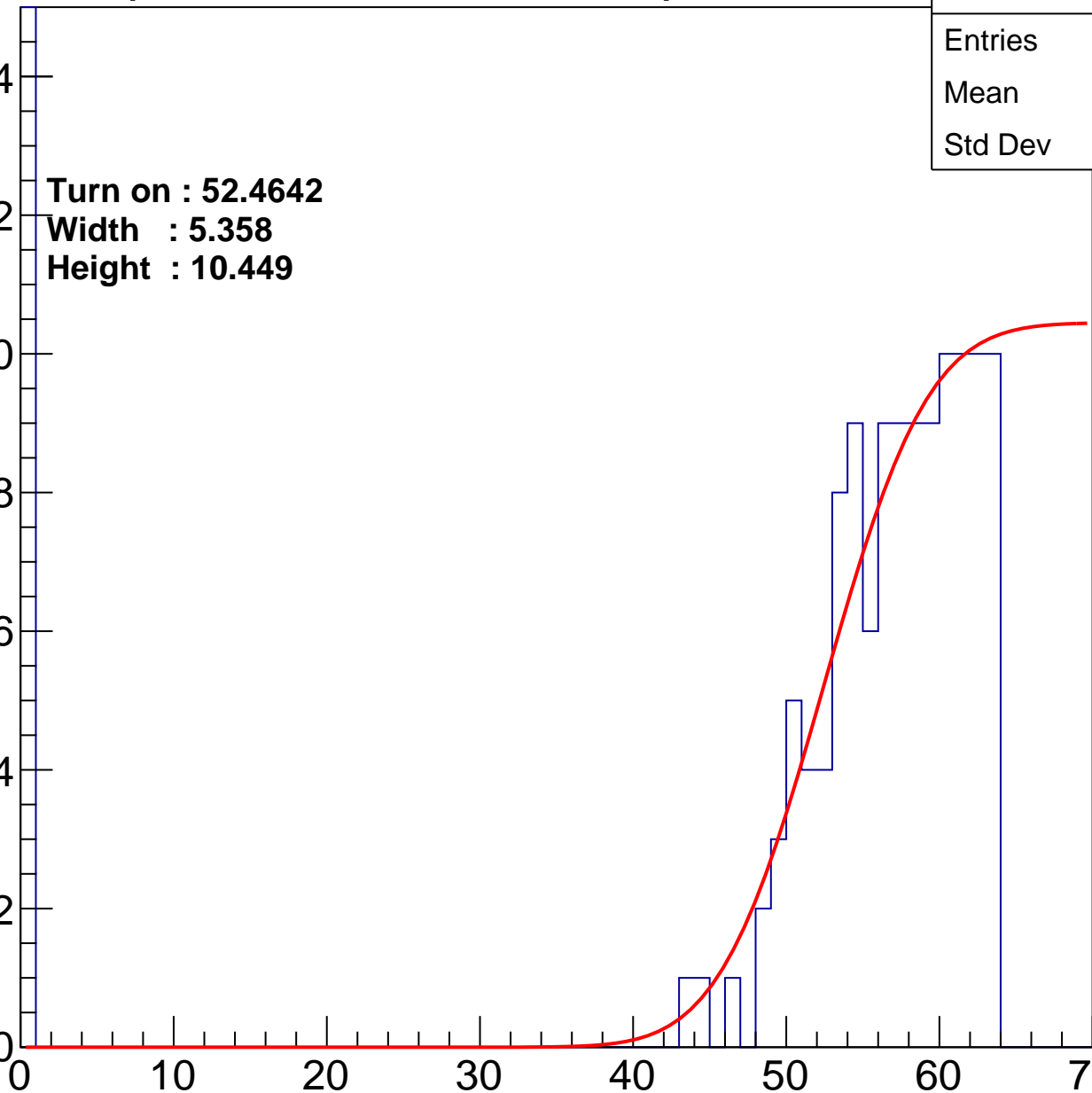
**Width : 5.358**

**Height : 10.449**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L104S, U3-ch123

calib\_packv5\_033123\_0516.root, FC#4, port A1

Entries	212
Mean	32.29
Std Dev	28.45

**Turn on : 52.5732**

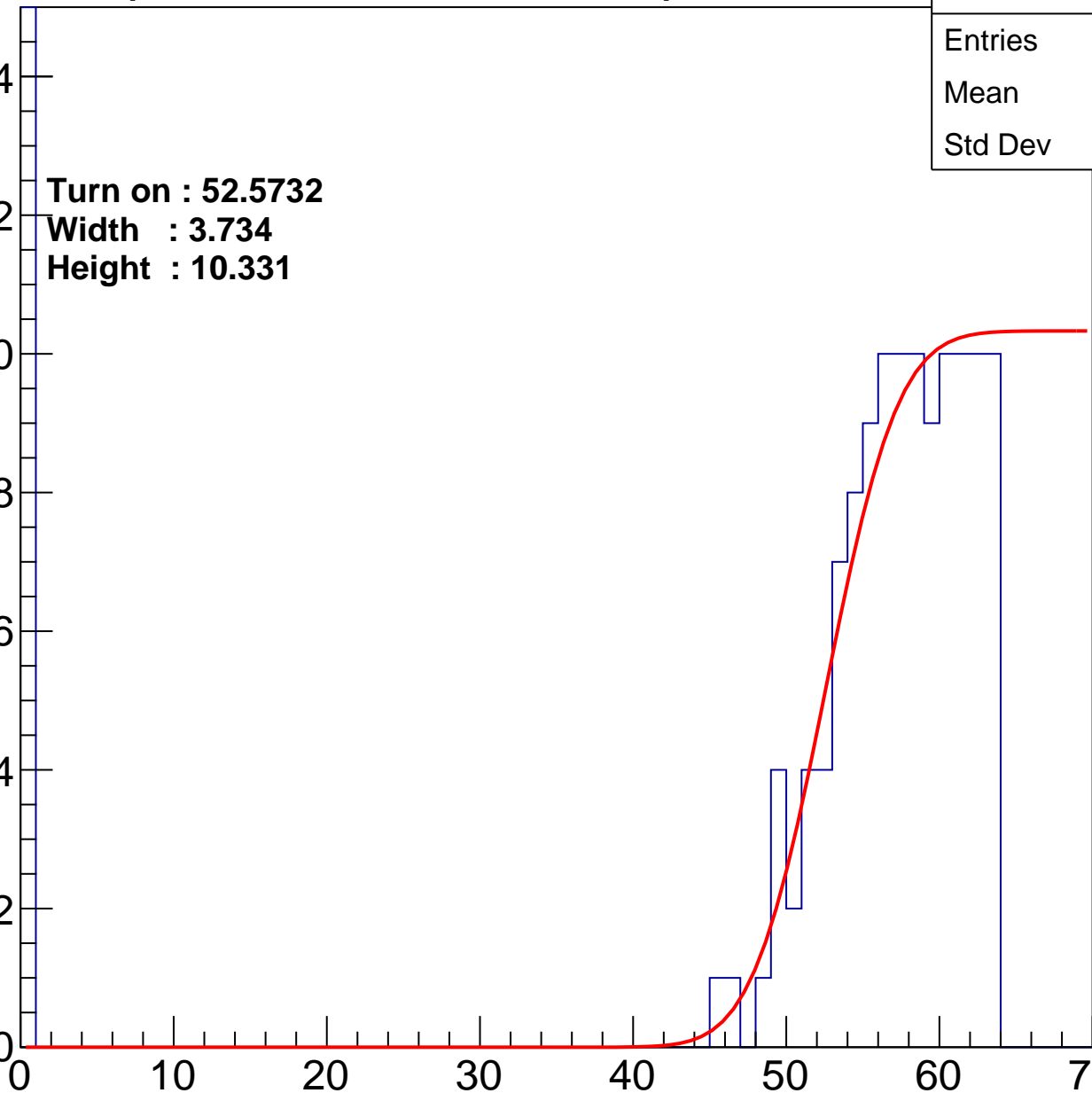
**Width : 3.734**

**Height : 10.331**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L104S, U3-ch124

calib\_packv5\_033123\_0516.root, FC#4, port A1

Entries	205
Mean	33.87
Std Dev	28.13

**Turn on : 51.7262**

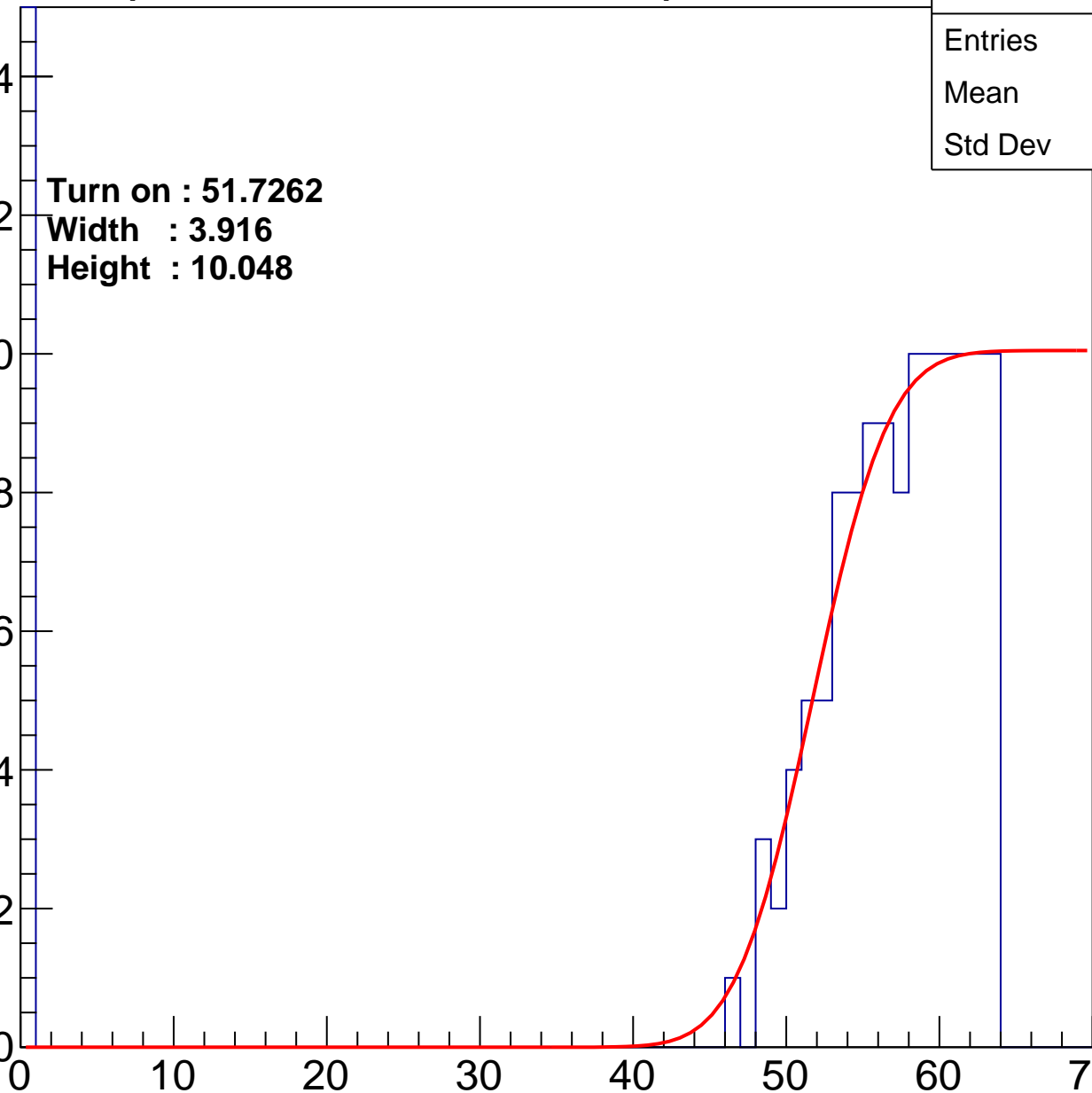
**Width : 3.916**

**Height : 10.048**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L104S, U3-ch125

calib\_packv5\_033123\_0516.root, FC#4, port A1

Entries	187
Mean	33.91
Std Dev	28.51

**Turn on : 52.7528**

**Width : 2.749**

**Height : 9.822**

Entry

14

12

10

8

6

4

2

0

0

10

20

30

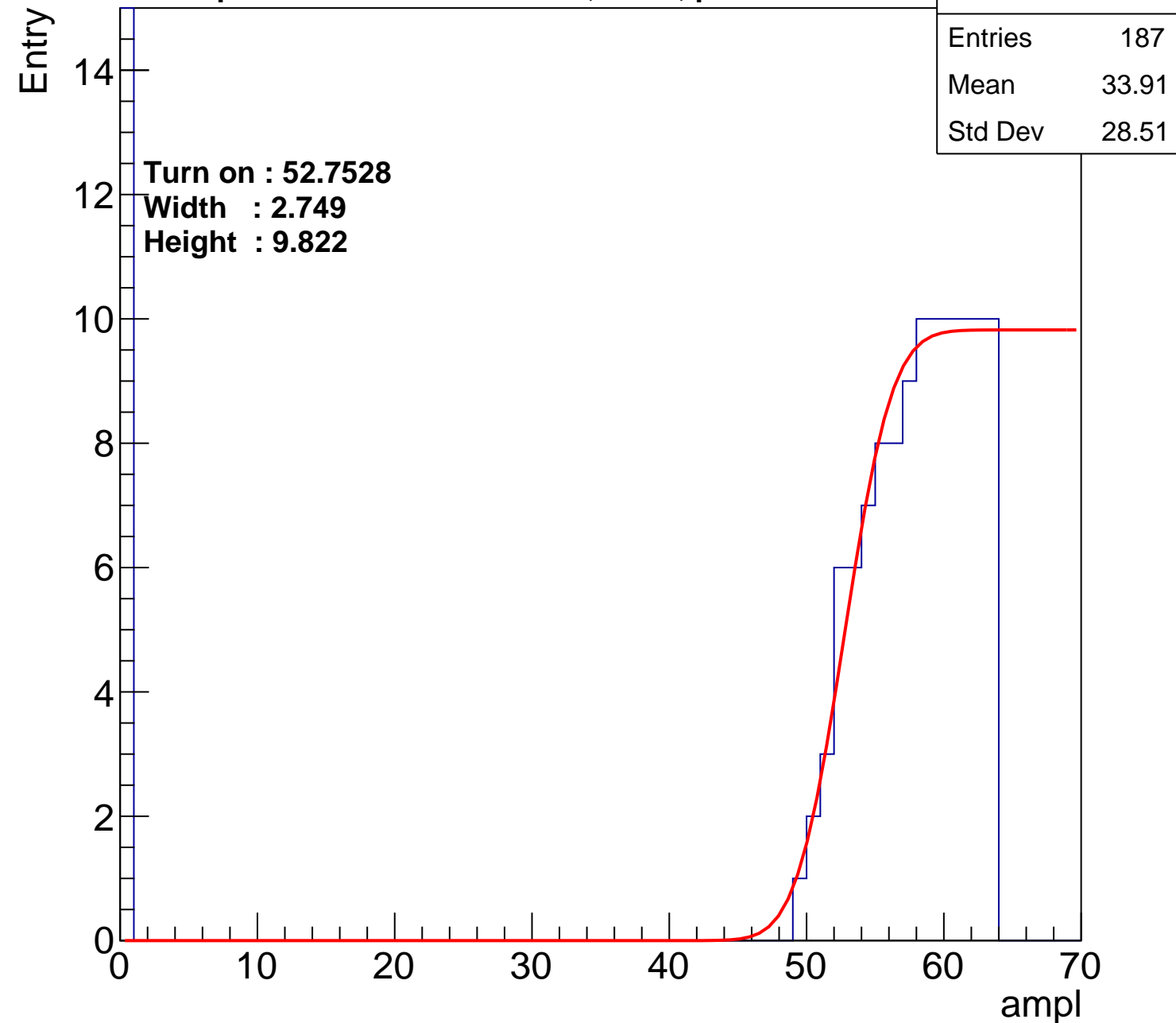
40

50

60

70

ampl



# B1L104S, U3-ch126

calib\_packv5\_033123\_0516.root, FC#4, port A1

Entries	192
Mean	29.78
Std Dev	28.99

**Turn on : 53.8304**

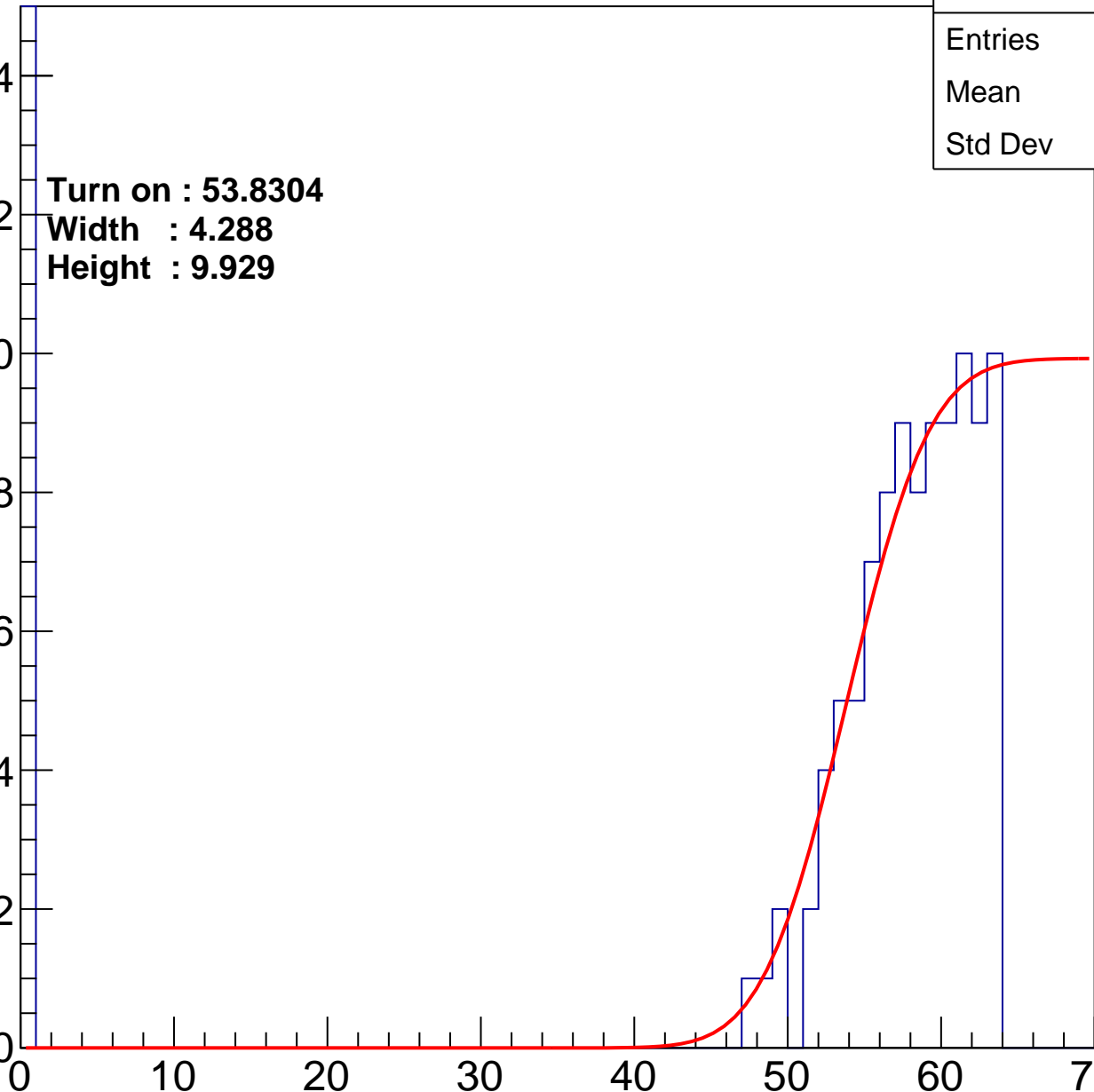
**Width : 4.288**

**Height : 9.929**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L104S, U3-ch127

calib\_packv5\_033123\_0516.root, FC#4, port A1

Entries	225
Mean	29.68
Std Dev	28.46

Turn on : 52.7045

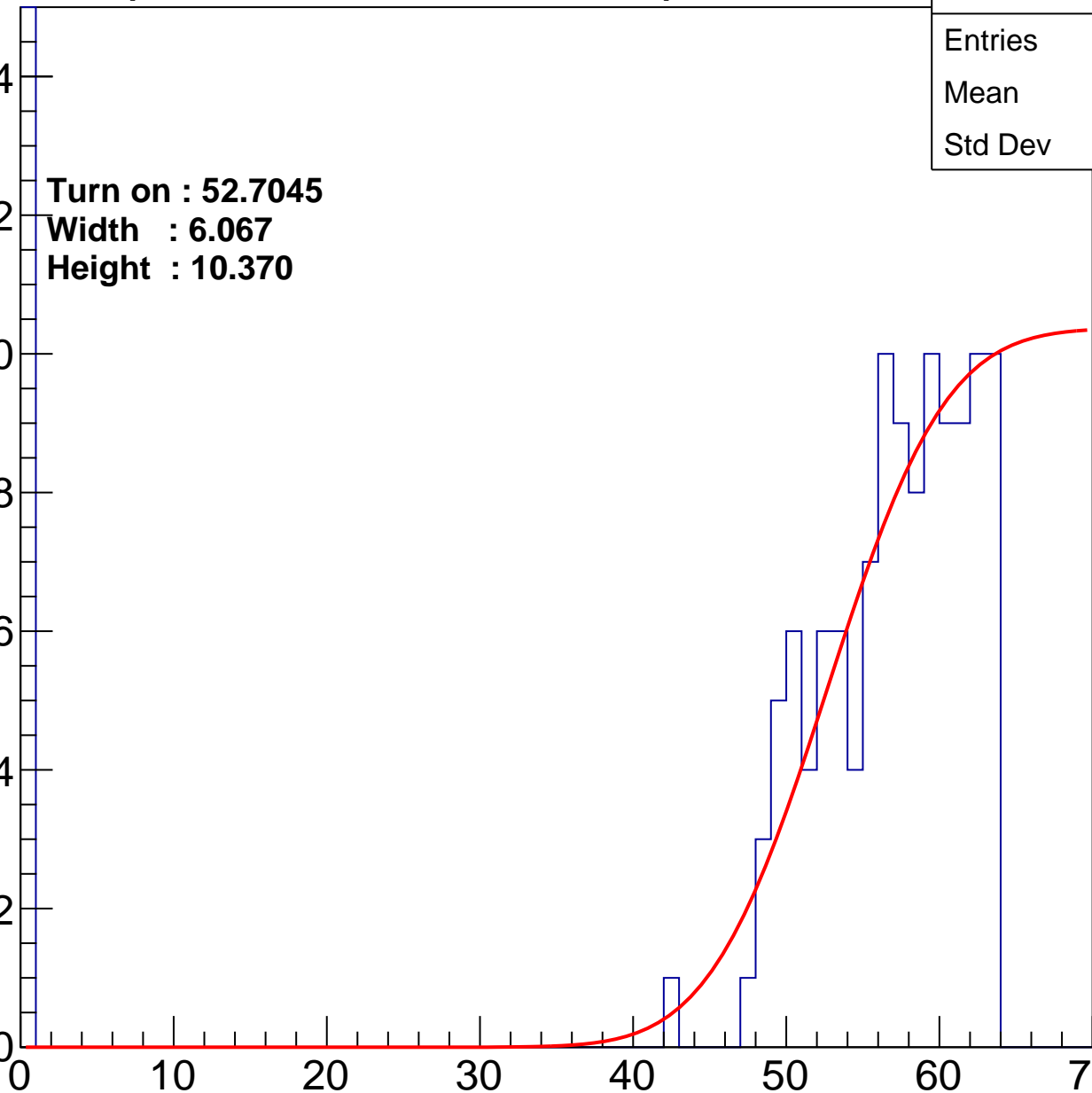
Width : 6.067

Height : 10.370

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L104S, U3-ch127

calib\_packv5\_033123\_0516.root, FC#4, port A1

Entries	225
Mean	29.68
Std Dev	28.46

**Turn on : 52.7045**

**Width : 6.067**

**Height : 10.370**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl

