

B1L103S, U25-ch0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	458
Mean	37.5
Std Dev	18.59

Turn on : 25.0534

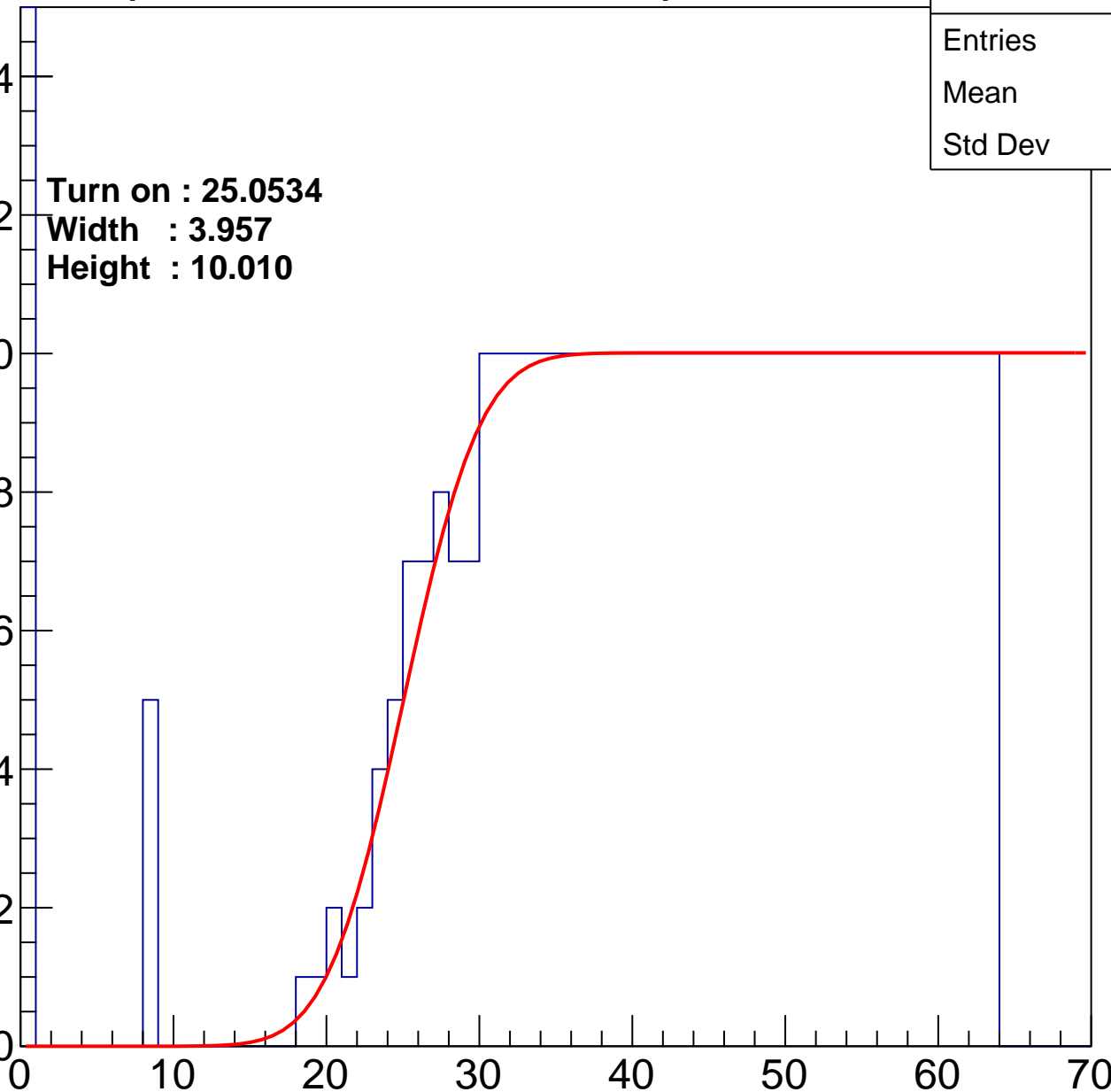
Width : 3.957

Height : 10.010

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U25-ch1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	385
Mean	41.46
Std Dev	16.83

Turn on : 29.5926

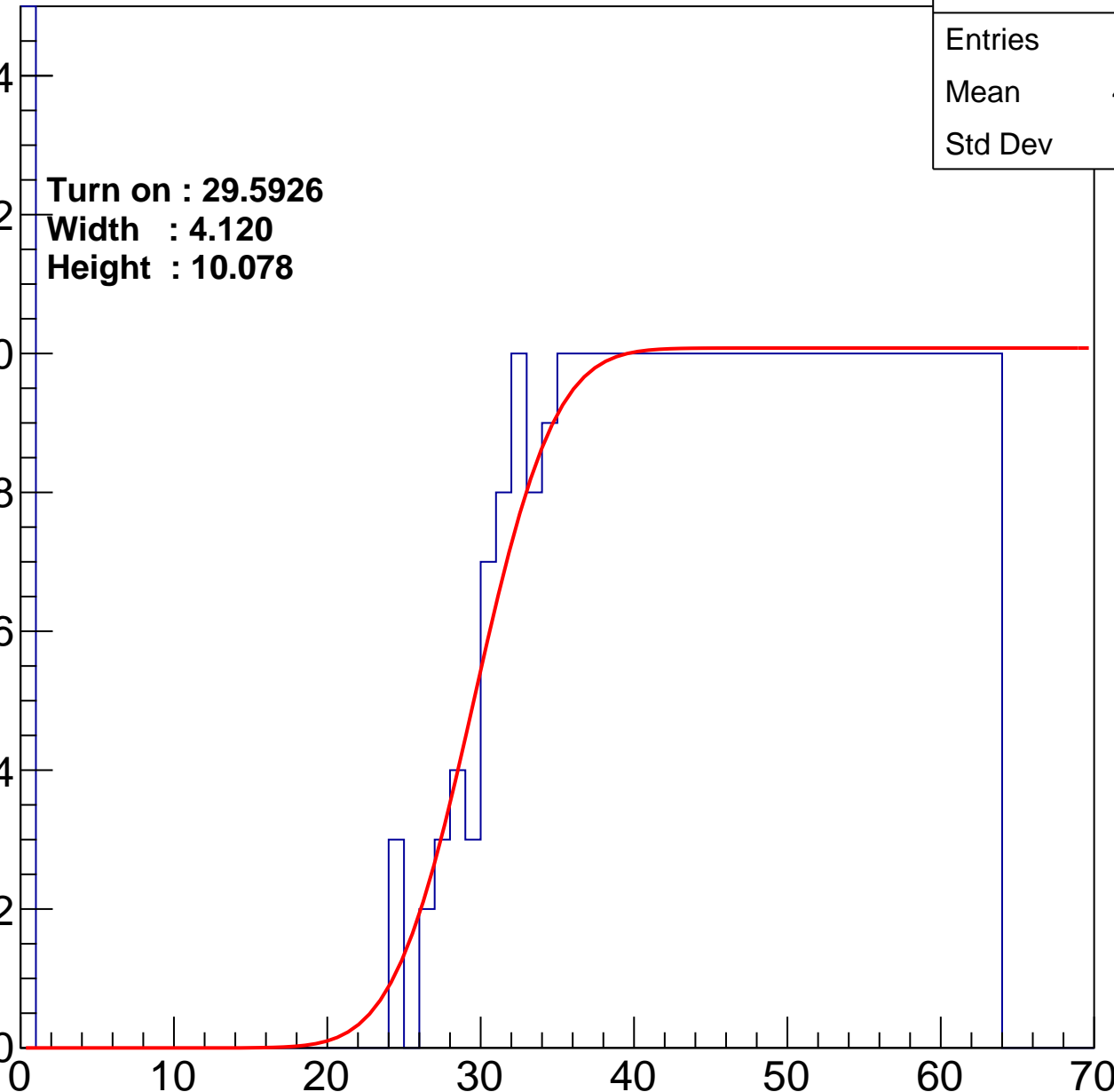
Width : 4.120

Height : 10.078

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U25-ch2

calib_packv5_041523_1651.root, FC#0, port C2

Entries	413
Mean	40.66
Std Dev	16.38

Turn on : 26.7762

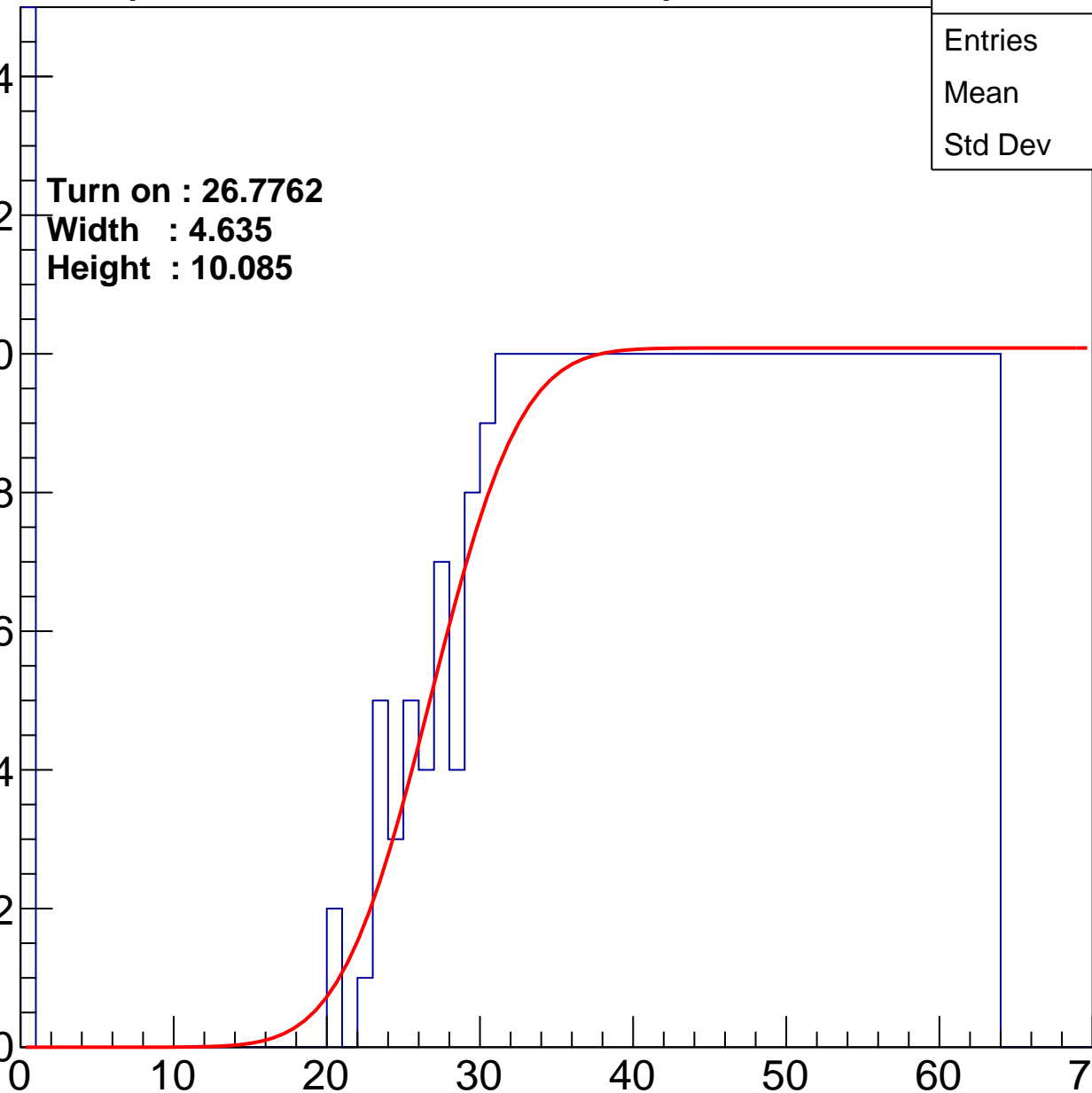
Width : 4.635

Height : 10.085

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U25-ch3

calib_packv5_041523_1651.root, FC#0, port C2

Entries	411
Mean	40.11
Std Dev	17.44

Turn on : 27.5888

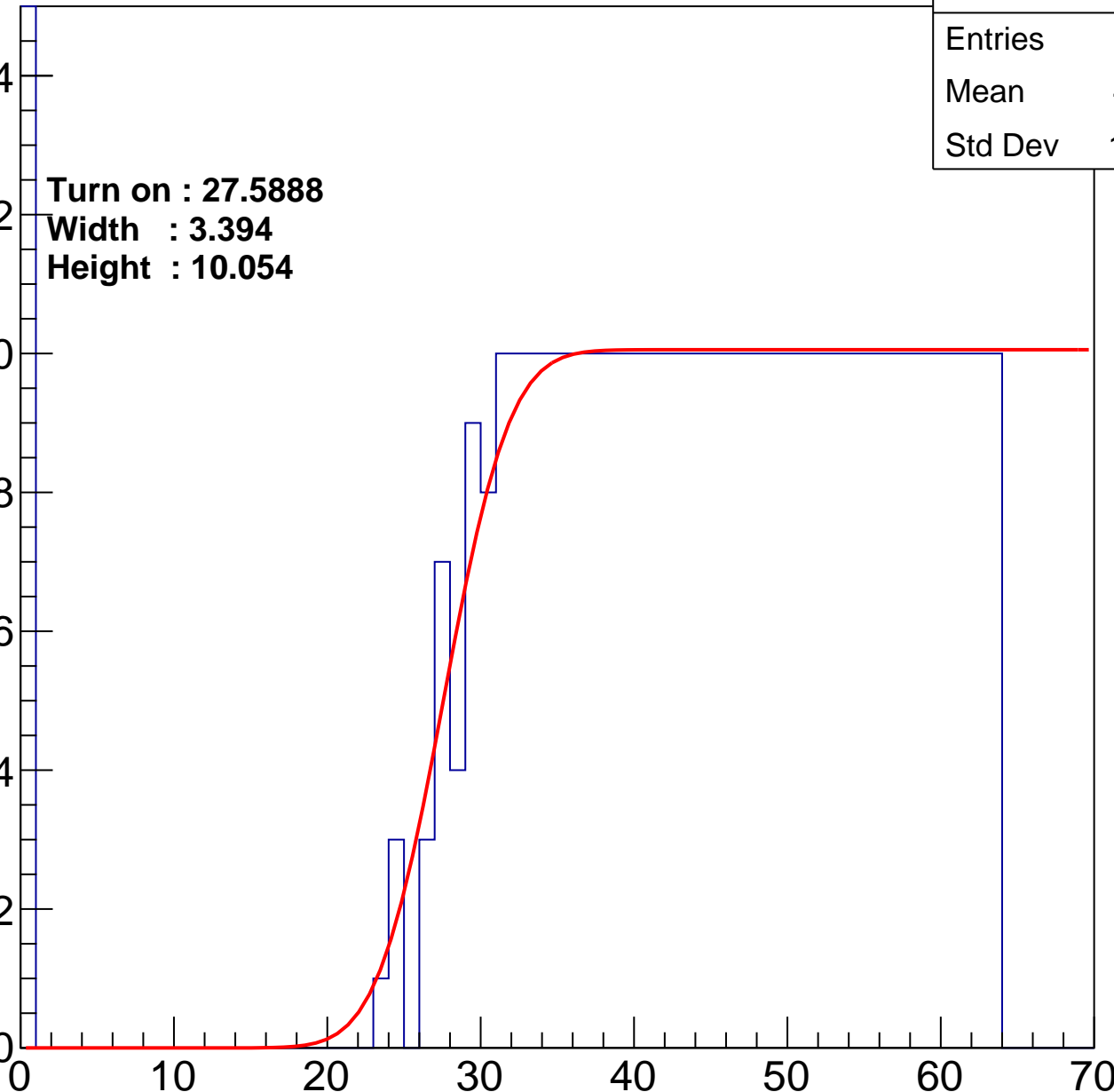
Width : 3.394

Height : 10.054

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U25-ch4

calib_packv5_041523_1651.root, FC#0, port C2

Entries	427
Mean	39.17
Std Dev	17.9

Turn on : 26.4485

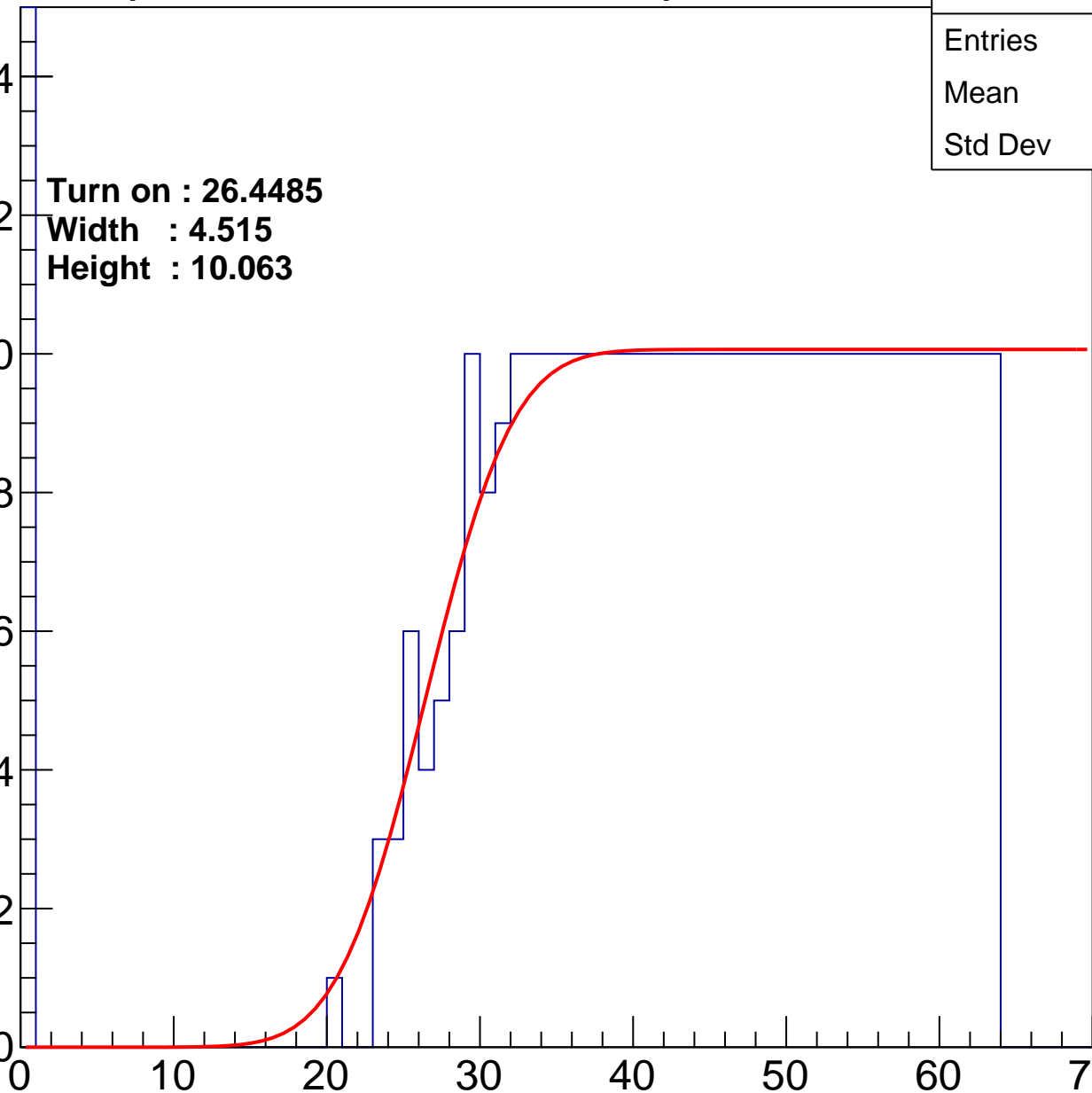
Width : 4.515

Height : 10.063

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U25-ch5

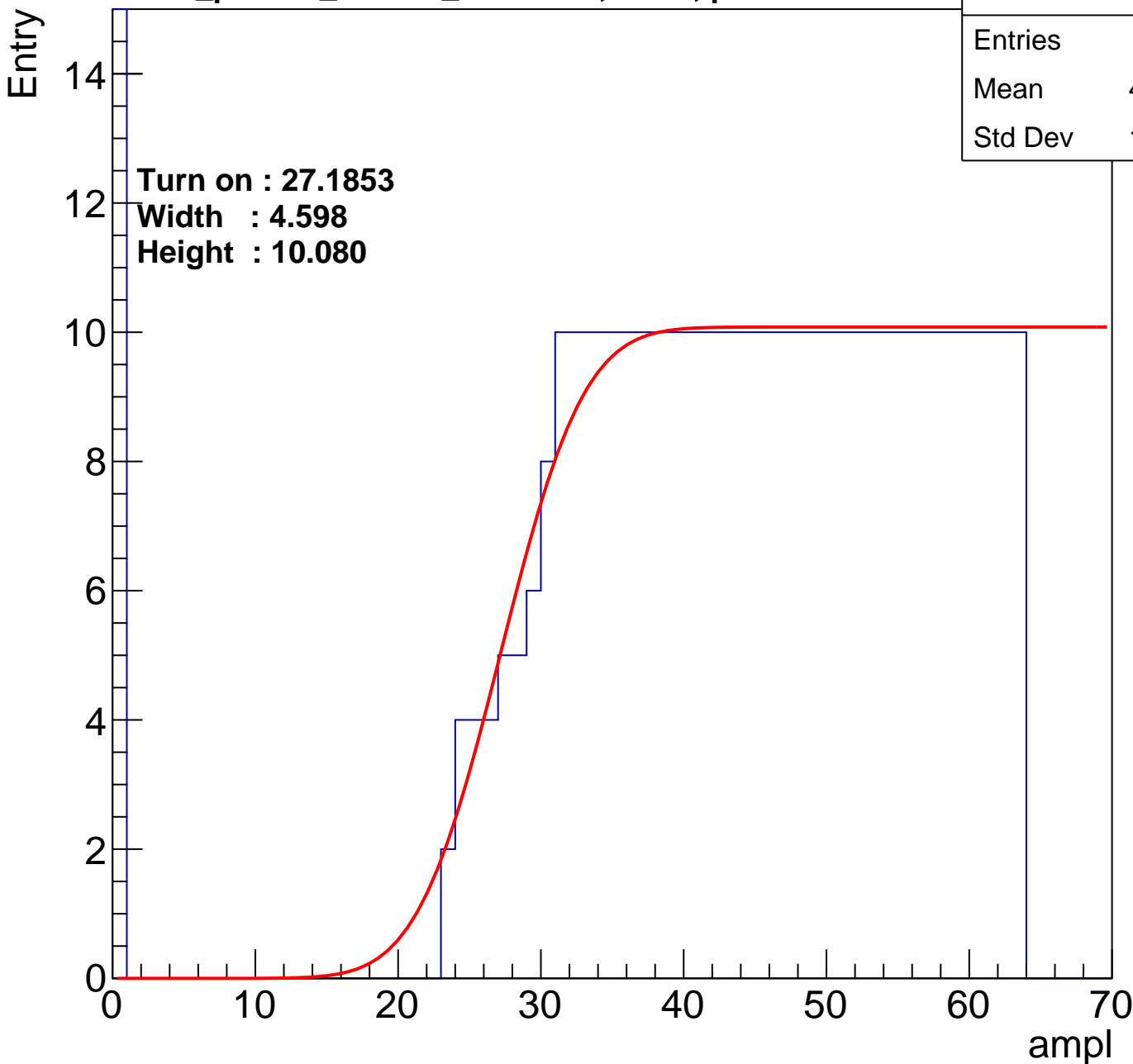
calib_packv5_041523_1651.root, FC#0, port C2

Entries	408
Mean	40.55
Std Dev	16.89

Turn on : 27.1853

Width : 4.598

Height : 10.080



B1L103S, U25-ch6

calib_packv5_041523_1651.root, FC#0, port C2

Entries	424
Mean	40.24
Std Dev	16.46

Turn on : 25.4607

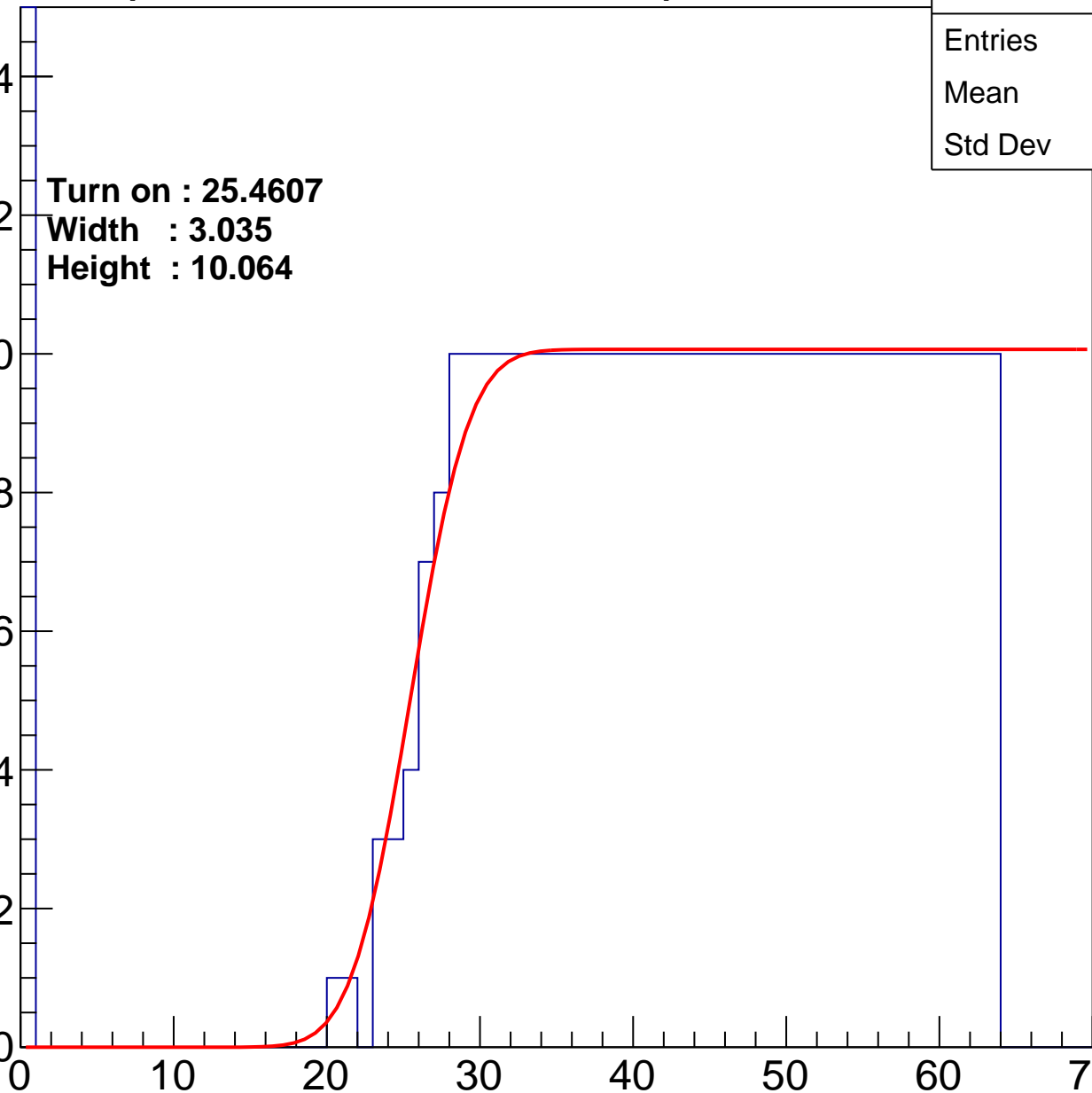
Width : 3.035

Height : 10.064

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U25-ch7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	423
Mean	39.55
Std Dev	17.62

Turn on : 26.4826

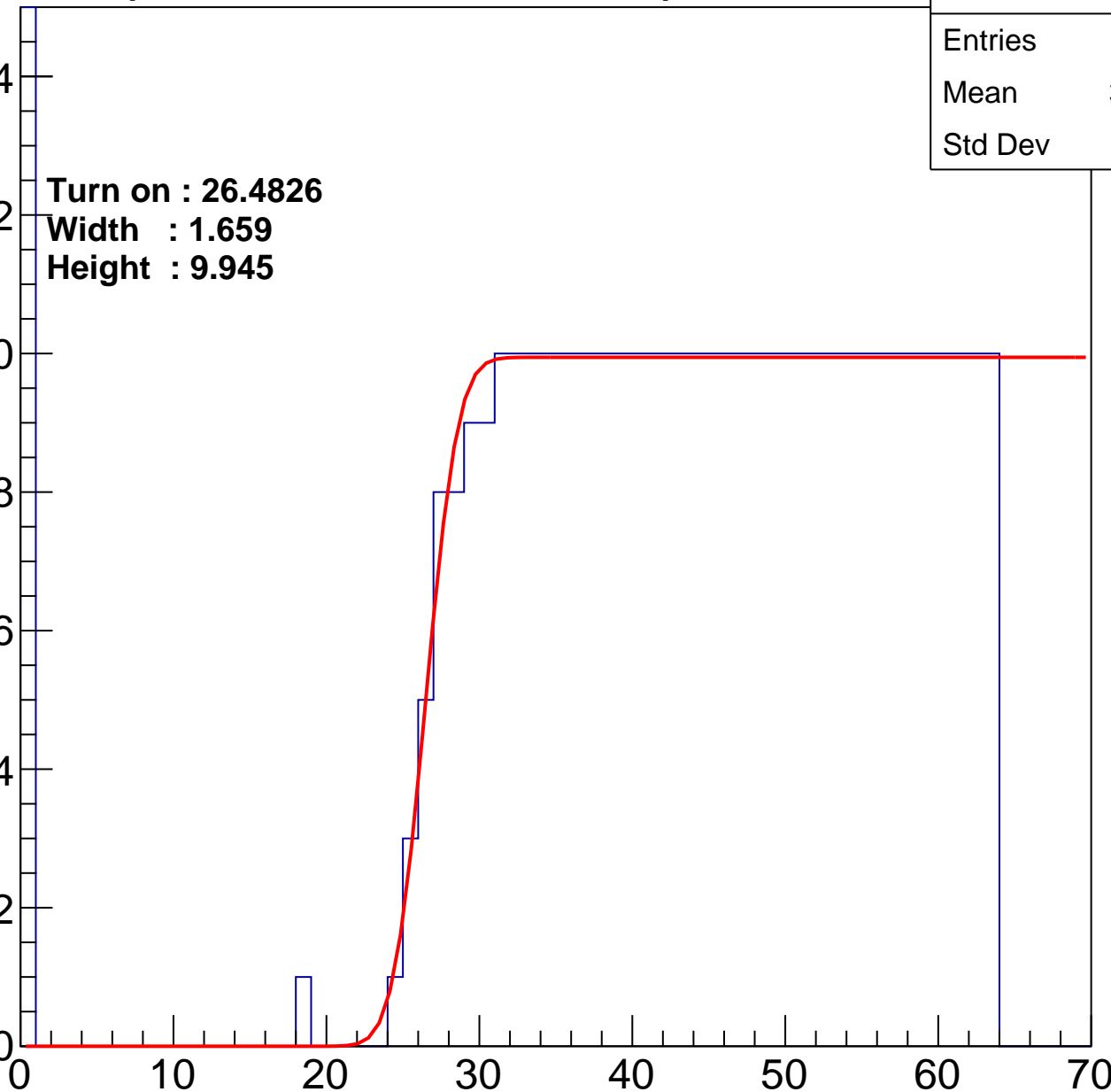
Width : 1.659

Height : 9.945

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U25-ch8

calib_packv5_041523_1651.root, FC#0, port C2

Entries	435
Mean	39.18
Std Dev	17.47

Turn on : 25.5032

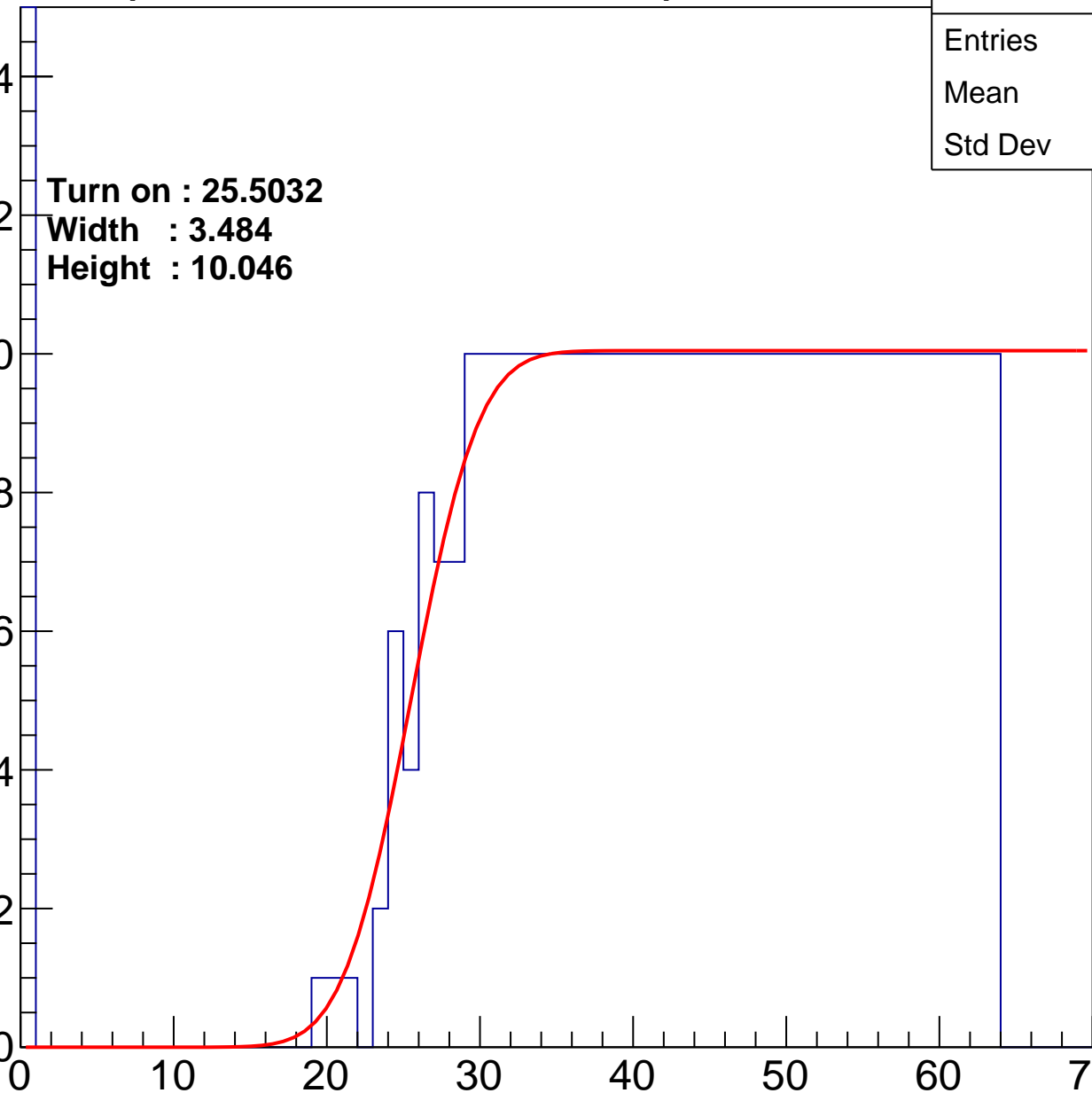
Width : 3.484

Height : 10.046

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U25-ch9

calib_packv5_041523_1651.root, FC#0, port C2

Entries	404
Mean	40.34
Std Dev	17.44

Turn on : 28.4616

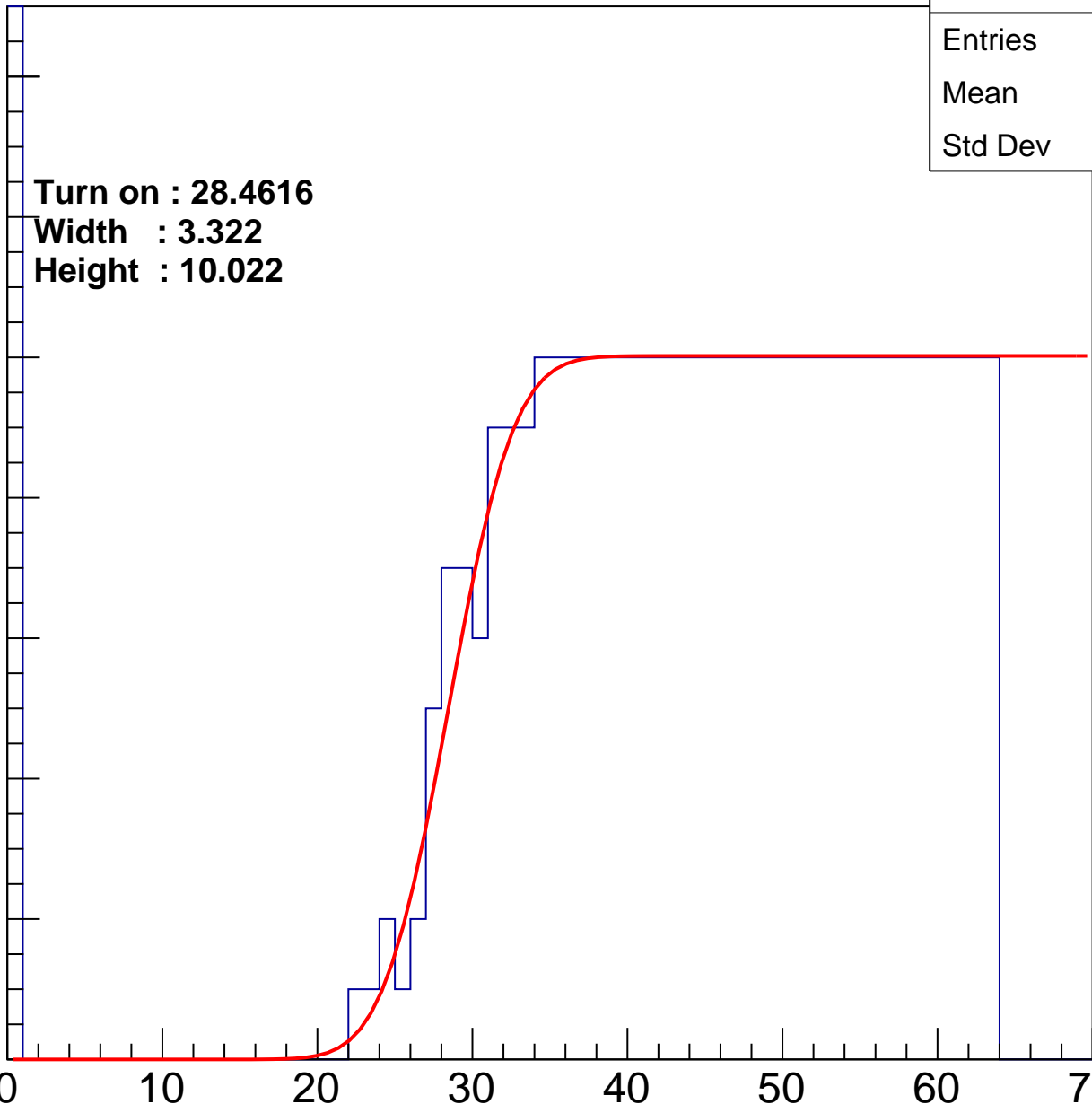
Width : 3.322

Height : 10.022

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U25-ch10

calib_packv5_041523_1651.root, FC#0, port C2

Entries	432
Mean	39.32
Std Dev	17.37

Turn on : 25.9742

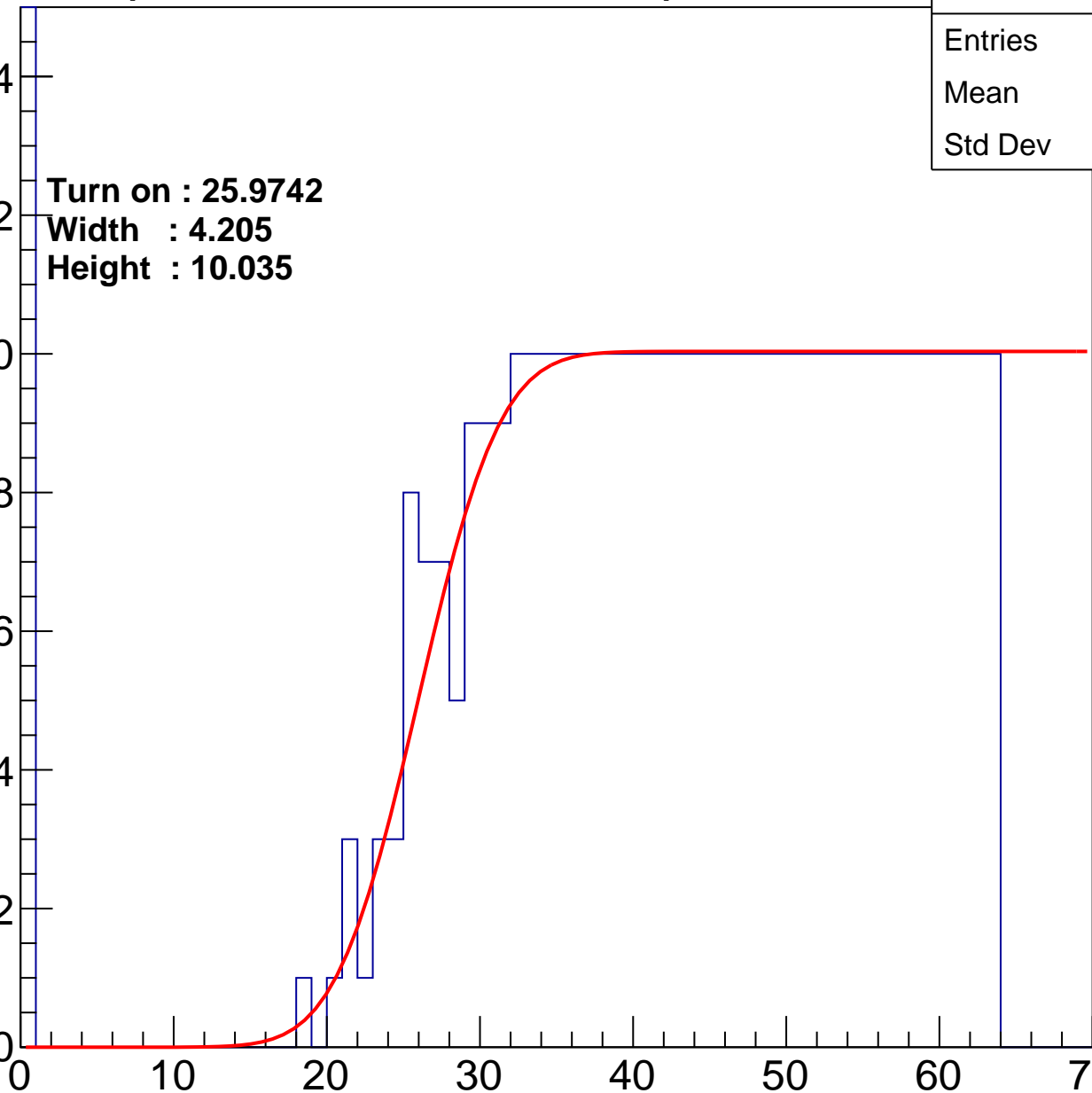
Width : 4.205

Height : 10.035

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U25-ch11

calib_packv5_041523_1651.root, FC#0, port C2

Entries	402
Mean	40.83
Std Dev	16.81

Turn on : 27.7586

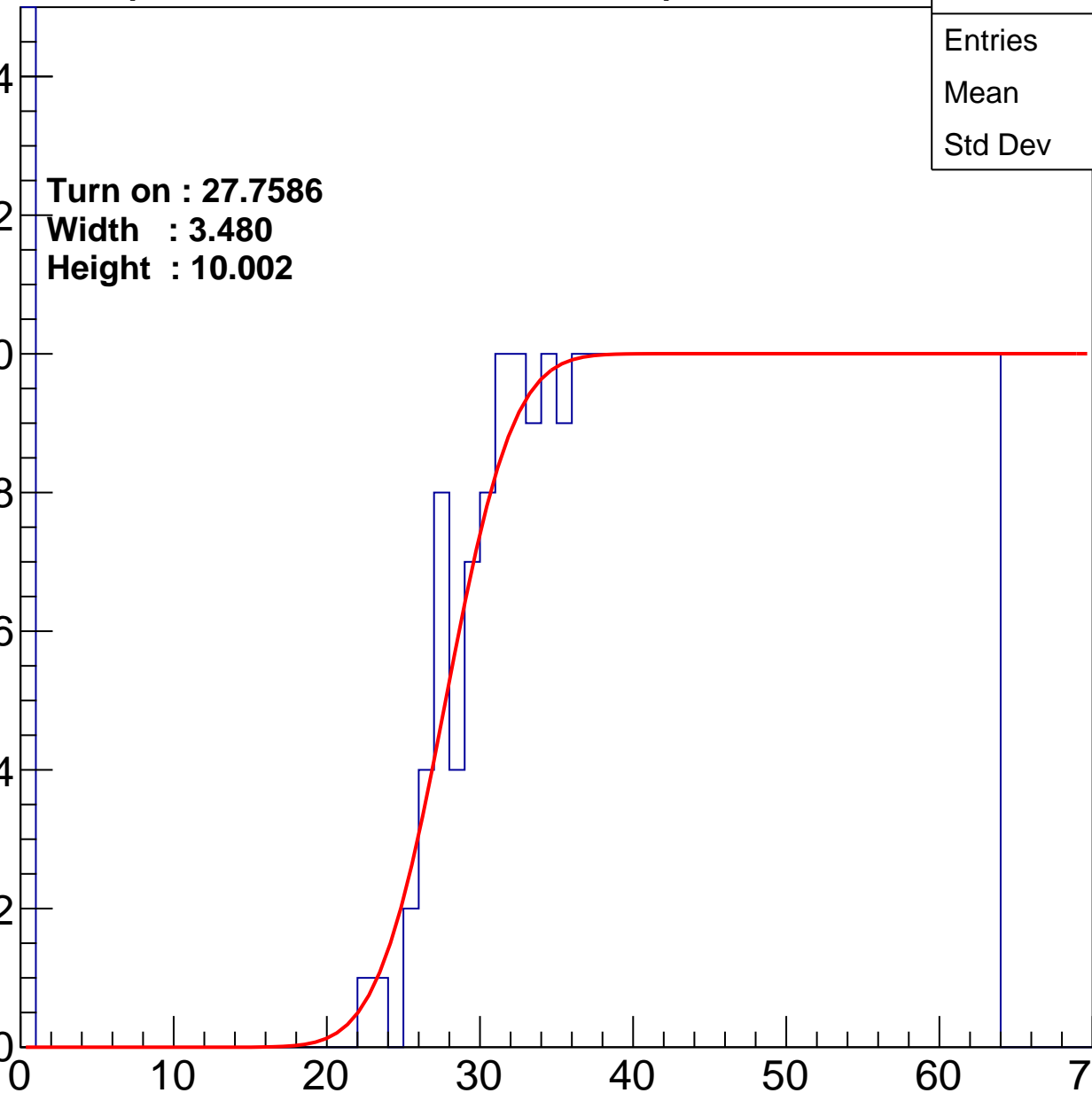
Width : 3.480

Height : 10.002

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U25-ch12

calib_packv5_041523_1651.root, FC#0, port C2

Entries	445
Mean	38.48
Std Dev	17.93

Turn on : 24.9046

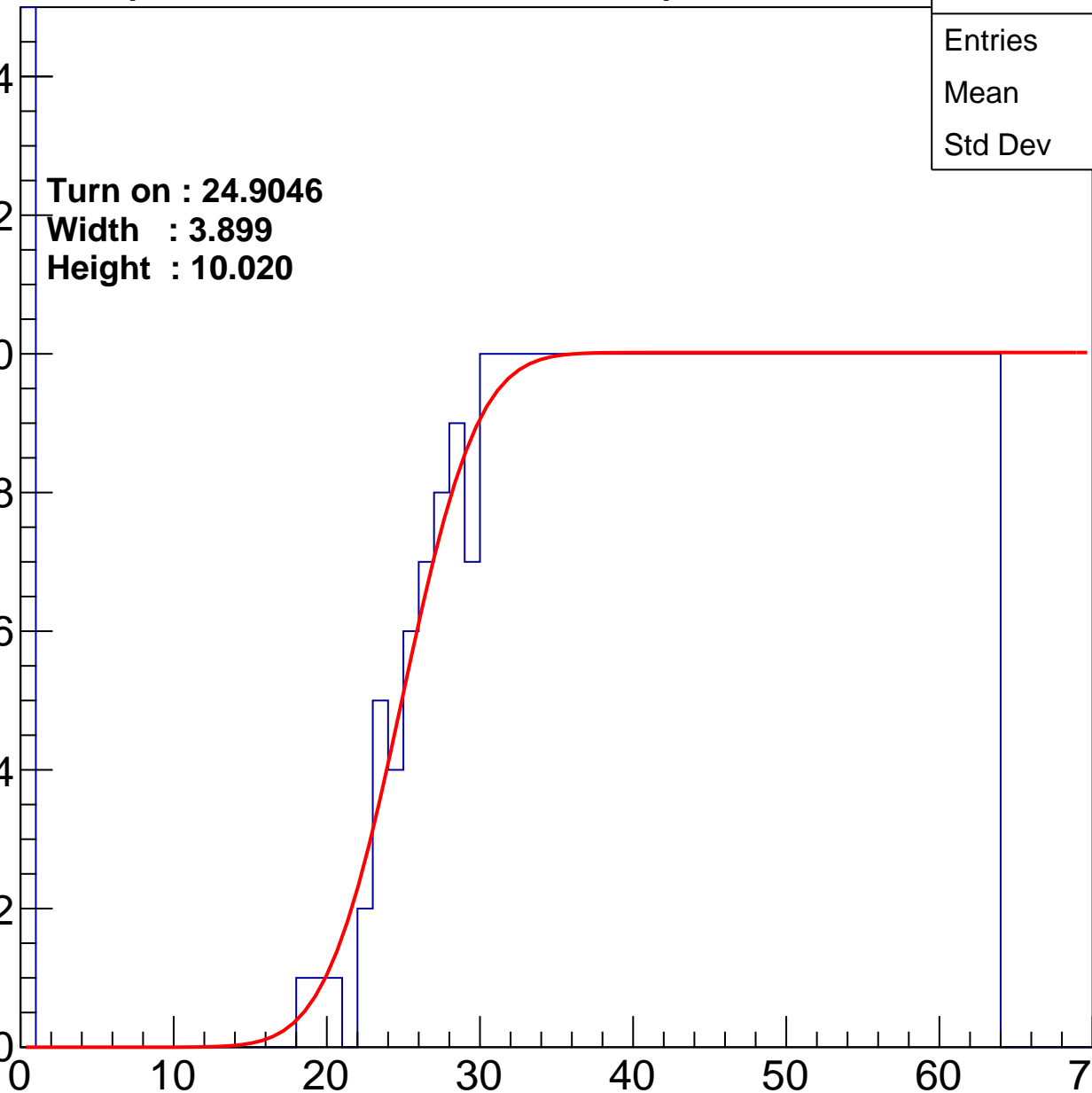
Width : 3.899

Height : 10.020

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U25-ch13

calib_packv5_041523_1651.root, FC#0, port C2

Entries	414
Mean	40.23
Std Dev	17.09

Turn on : 26.7482

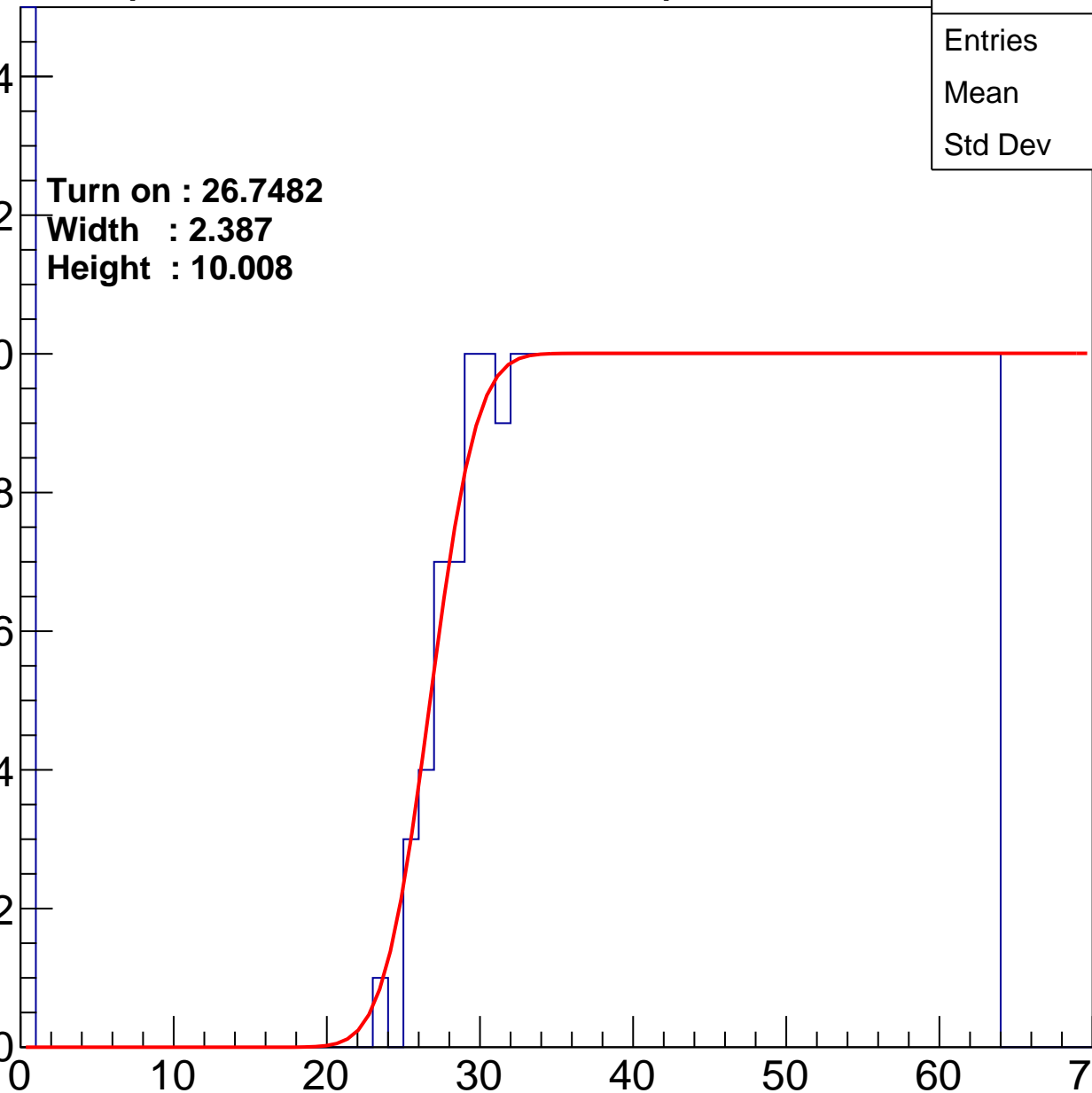
Width : 2.387

Height : 10.008

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U25-ch14

calib_packv5_041523_1651.root, FC#0, port C2

Entries	429
Mean	39.82
Std Dev	16.84

Turn on : 25.4961

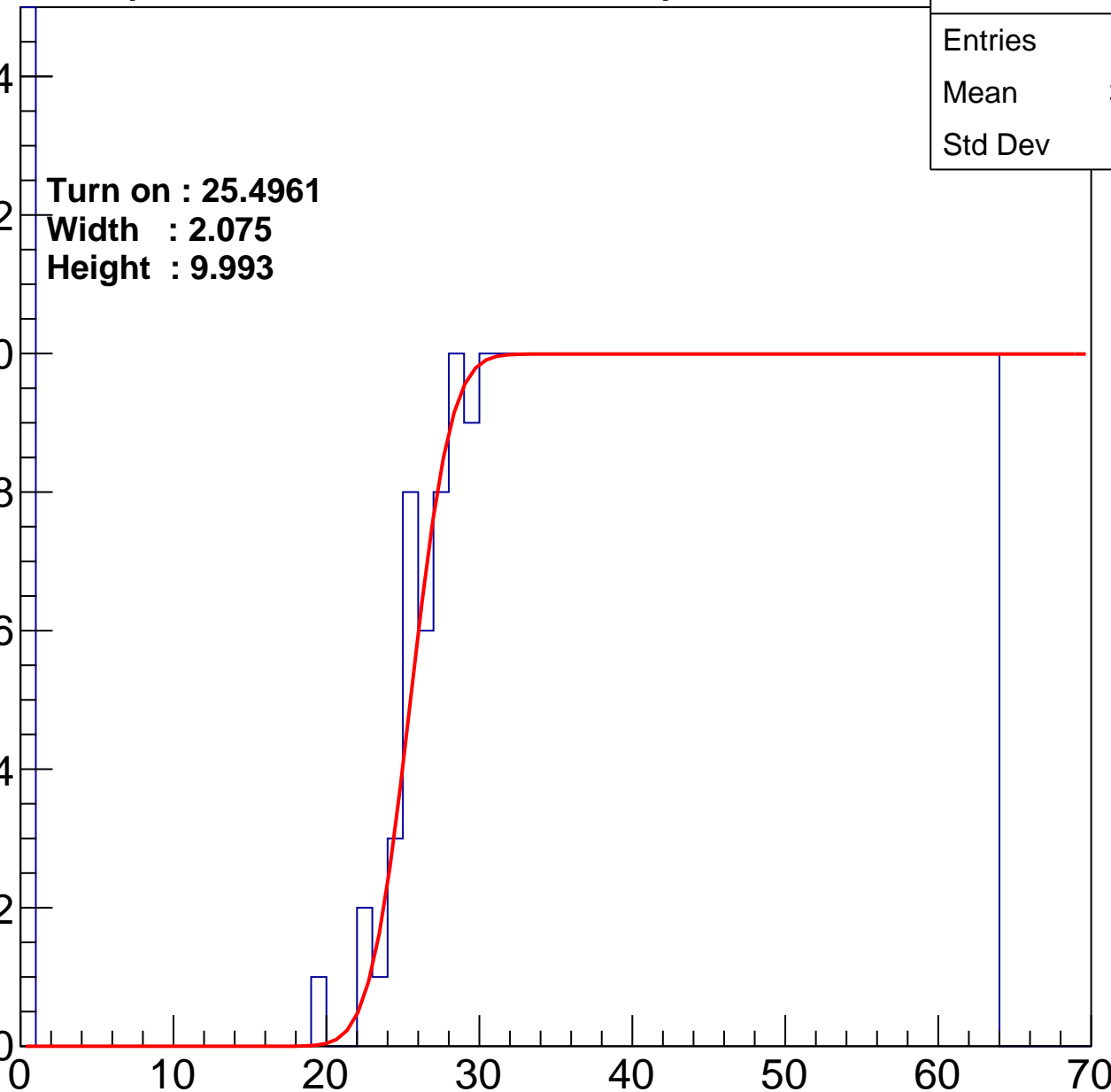
Width : 2.075

Height : 9.993

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U25-ch15

calib_packv5_041523_1651.root, FC#0, port C2

Entries	405
Mean	40.45
Std Dev	17.27

Turn on : 28.0663

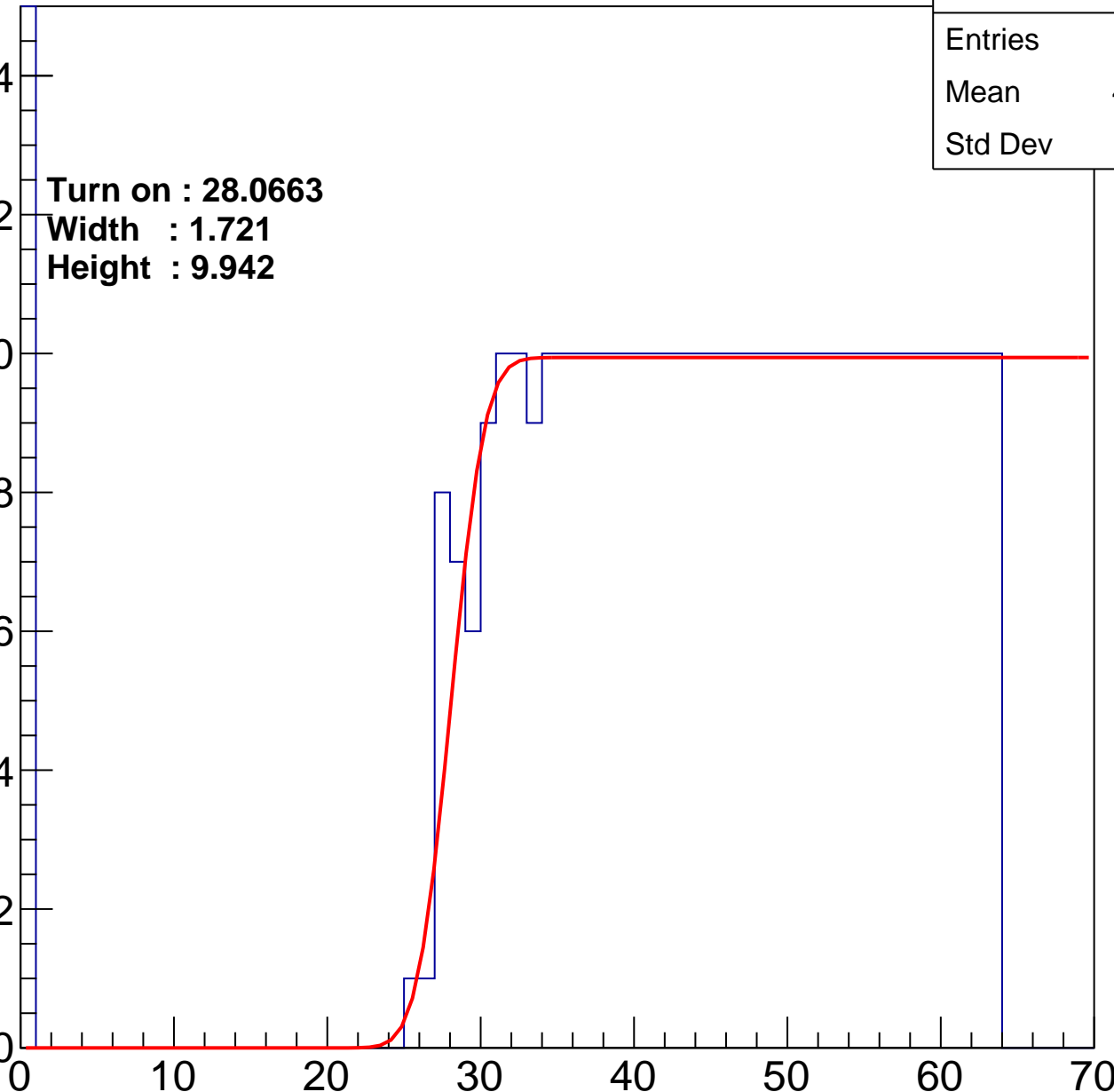
Width : 1.721

Height : 9.942

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U25-ch16

calib_packv5_041523_1651.root, FC#0, port C2

Entries	412
Mean	40.4
Std Dev	16.98

Turn on : 27.7318

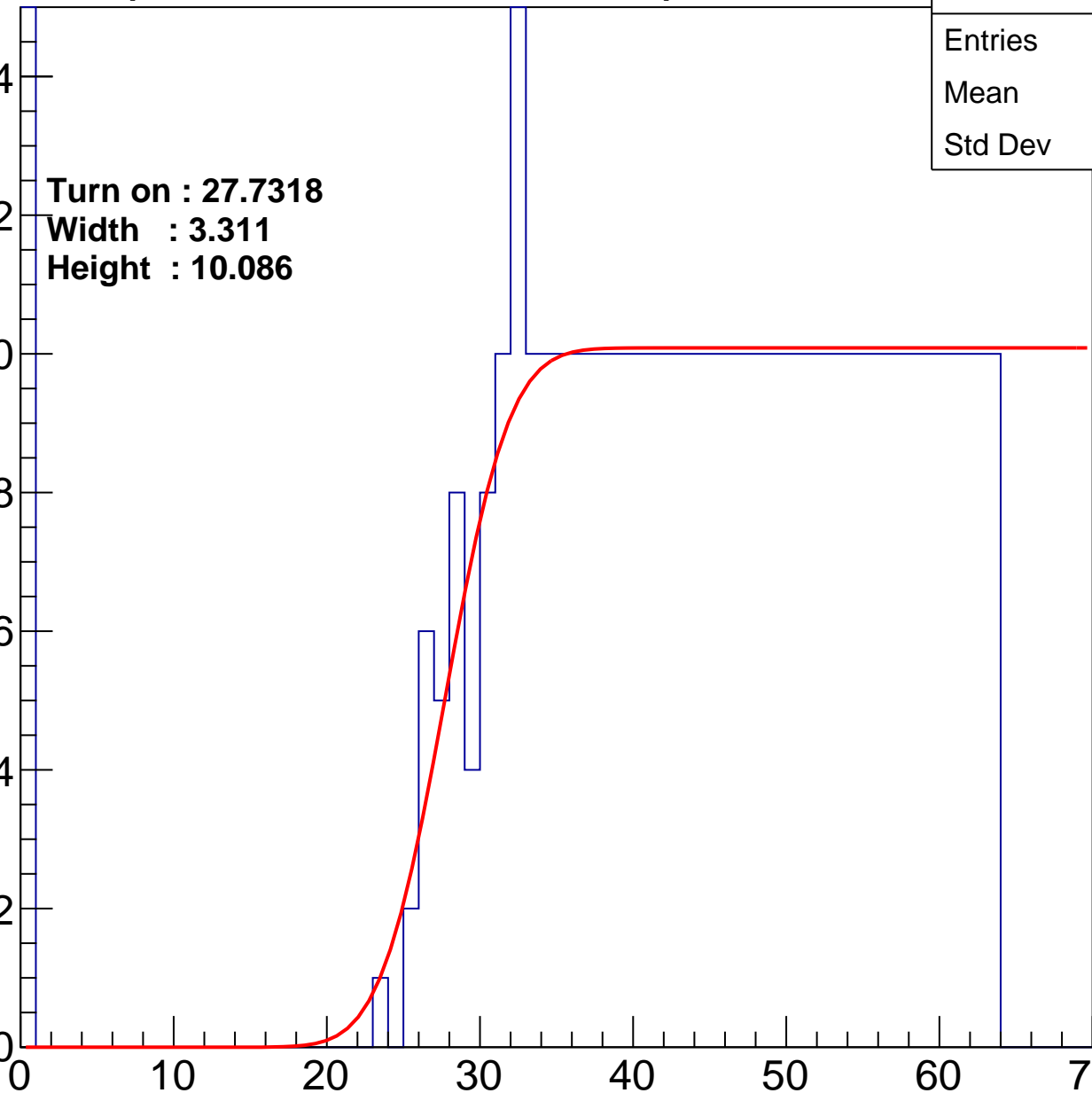
Width : 3.311

Height : 10.086

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U25-ch17

calib_packv5_041523_1651.root, FC#0, port C2

Entries	434
Mean	38.82
Std Dev	18.06

Turn on : 26.2307

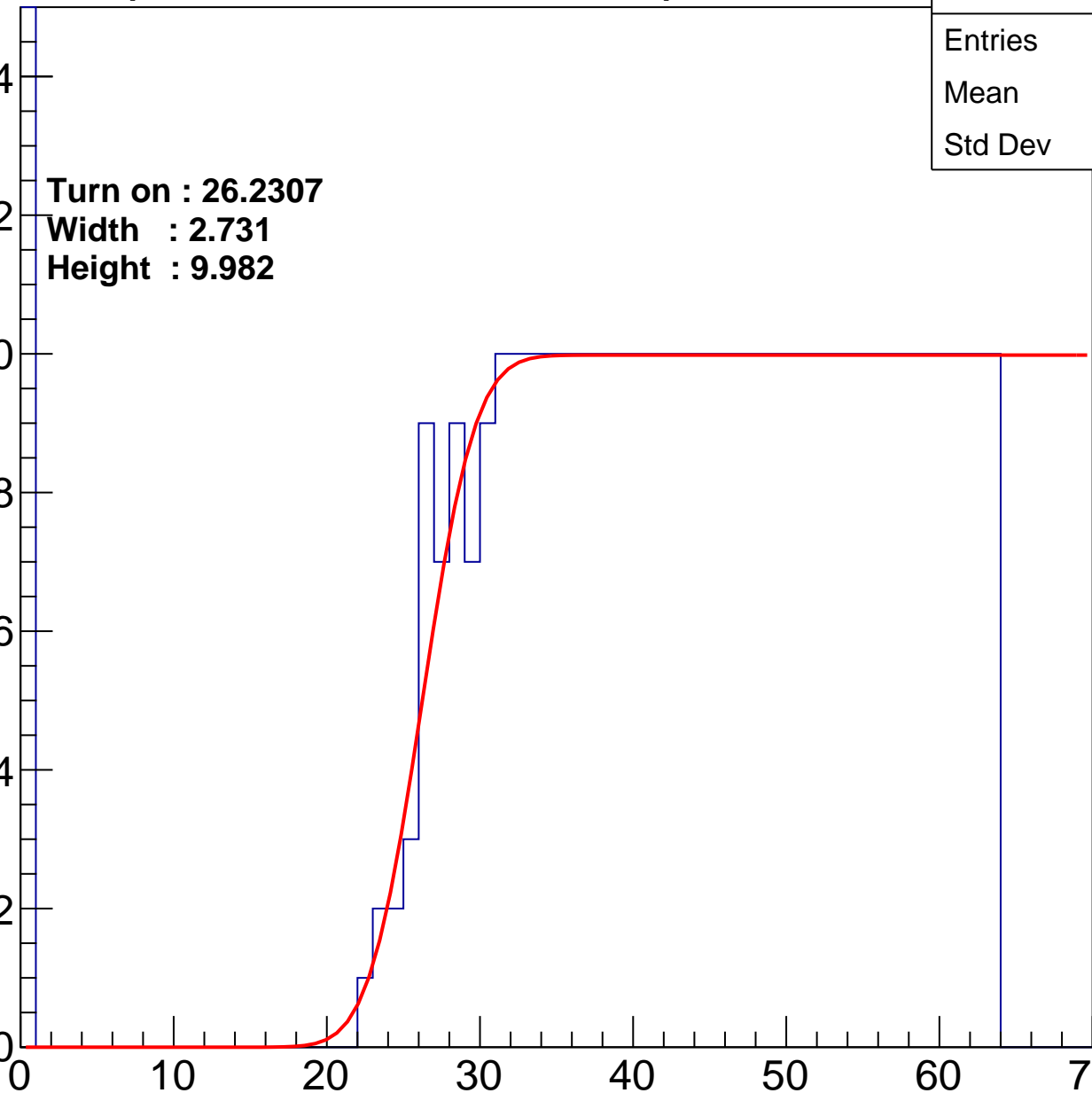
Width : 2.731

Height : 9.982

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U25-ch18

calib_packv5_041523_1651.root, FC#0, port C2

Entries	394
Mean	41.32
Std Dev	16.51

Turn on : 28.0487

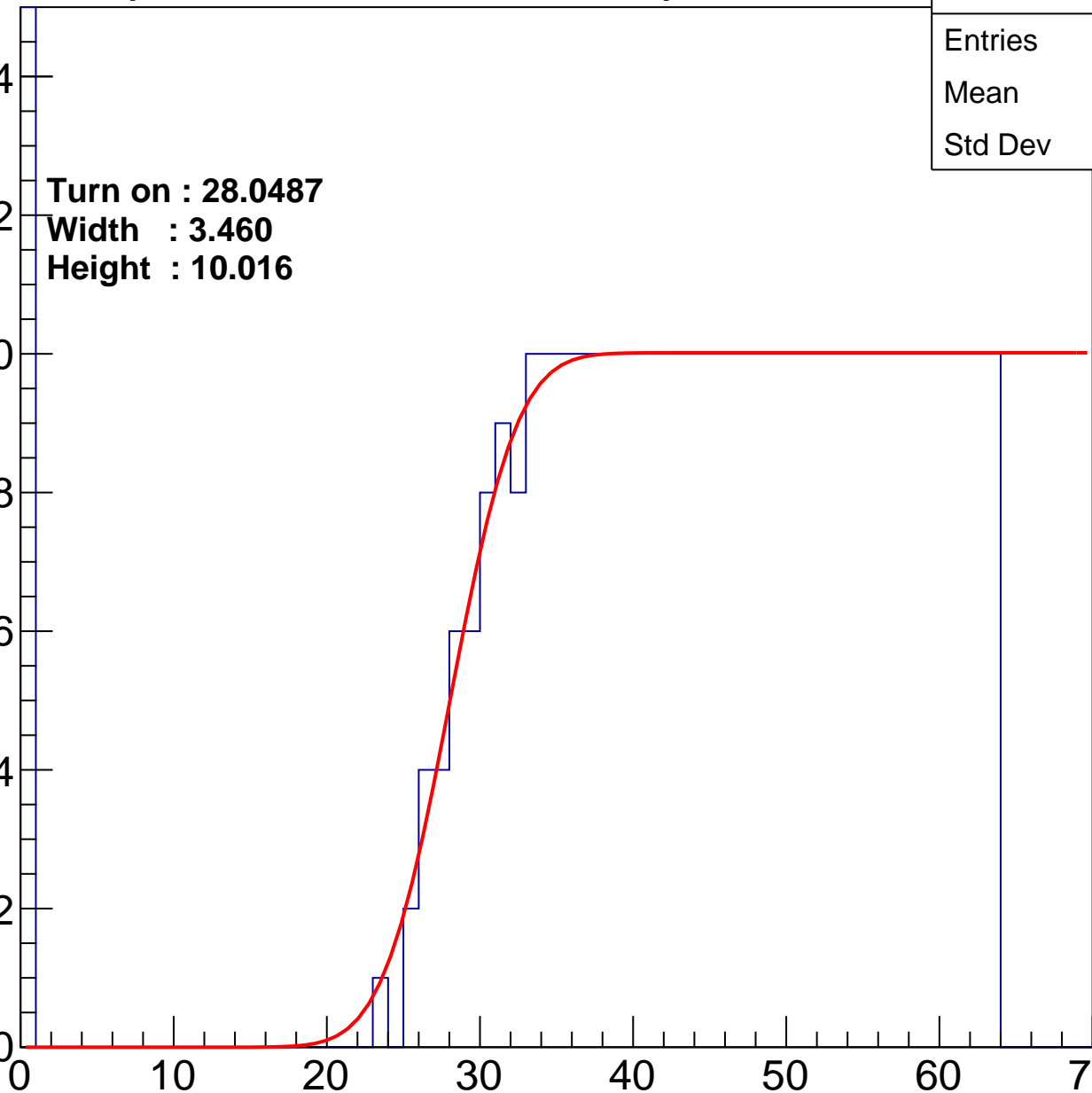
Width : 3.460

Height : 10.016

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U25-ch19

calib_packv5_041523_1651.root, FC#0, port C2

Entries	417
Mean	40
Std Dev	17.27

Turn on : 26.9469

Width : 2.037

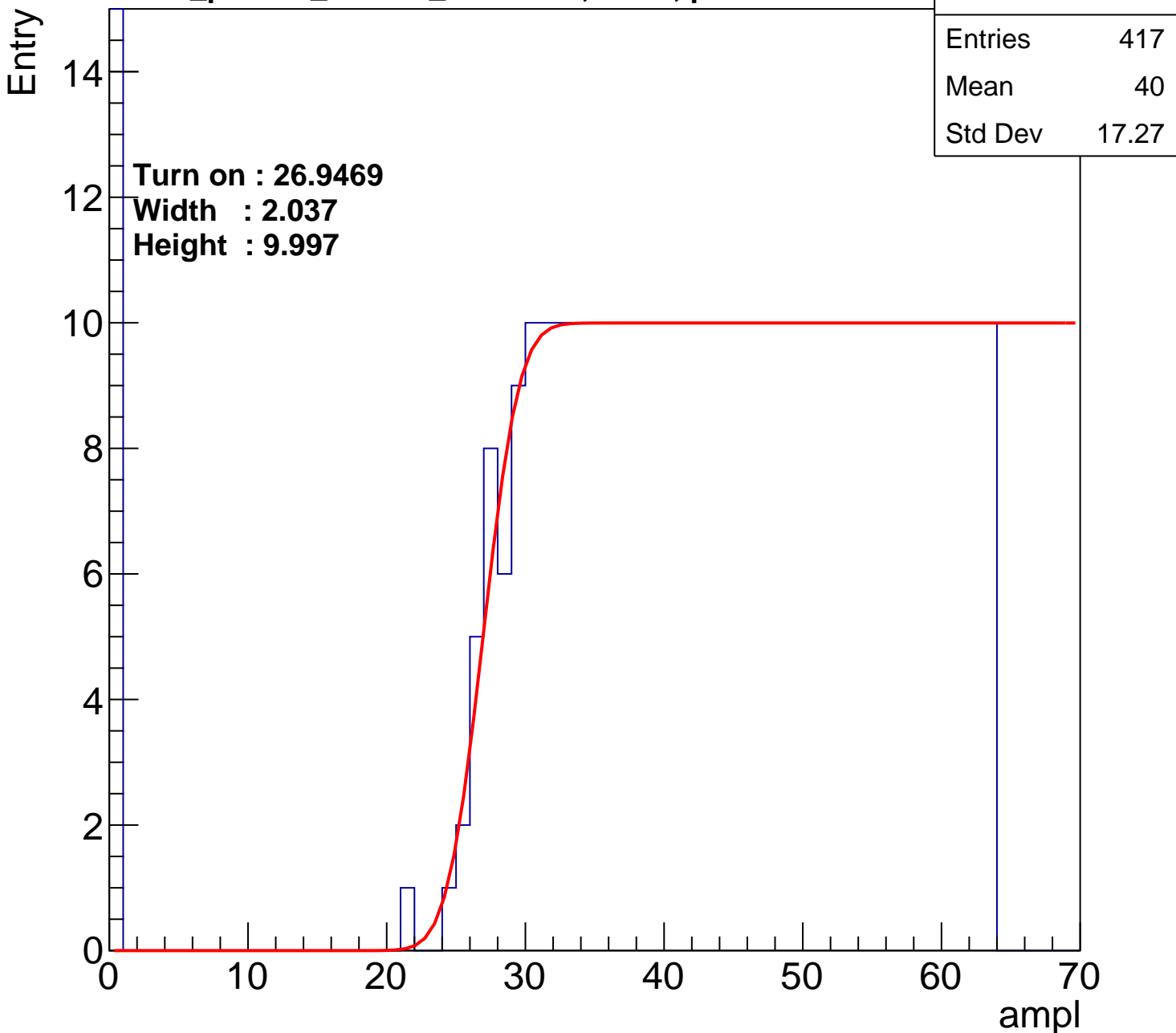
Height : 9.997

Entry

14
12
10
8
6
4
2
0

ampl

0 10 20 30 40 50 60 70



B1L103S, U25-ch20

calib_packv5_041523_1651.root, FC#0, port C2

Entries	430
Mean	39.27
Std Dev	17.61

Turn on : 26.1859

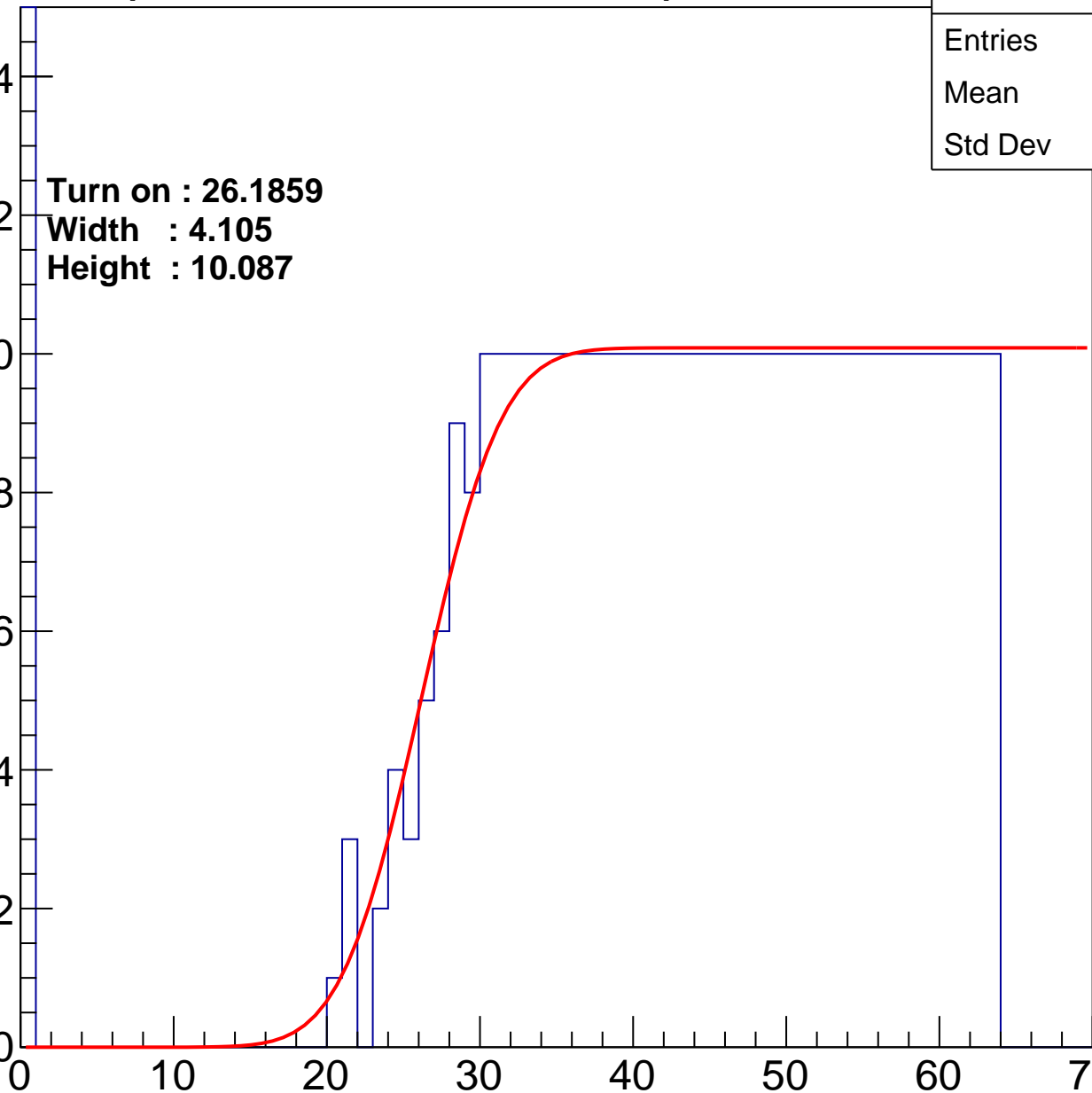
Width : 4.105

Height : 10.087

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U25-ch21

calib_packv5_041523_1651.root, FC#0, port C2

Entries	410
Mean	40.98
Std Dev	16.08

Turn on : 26.3185

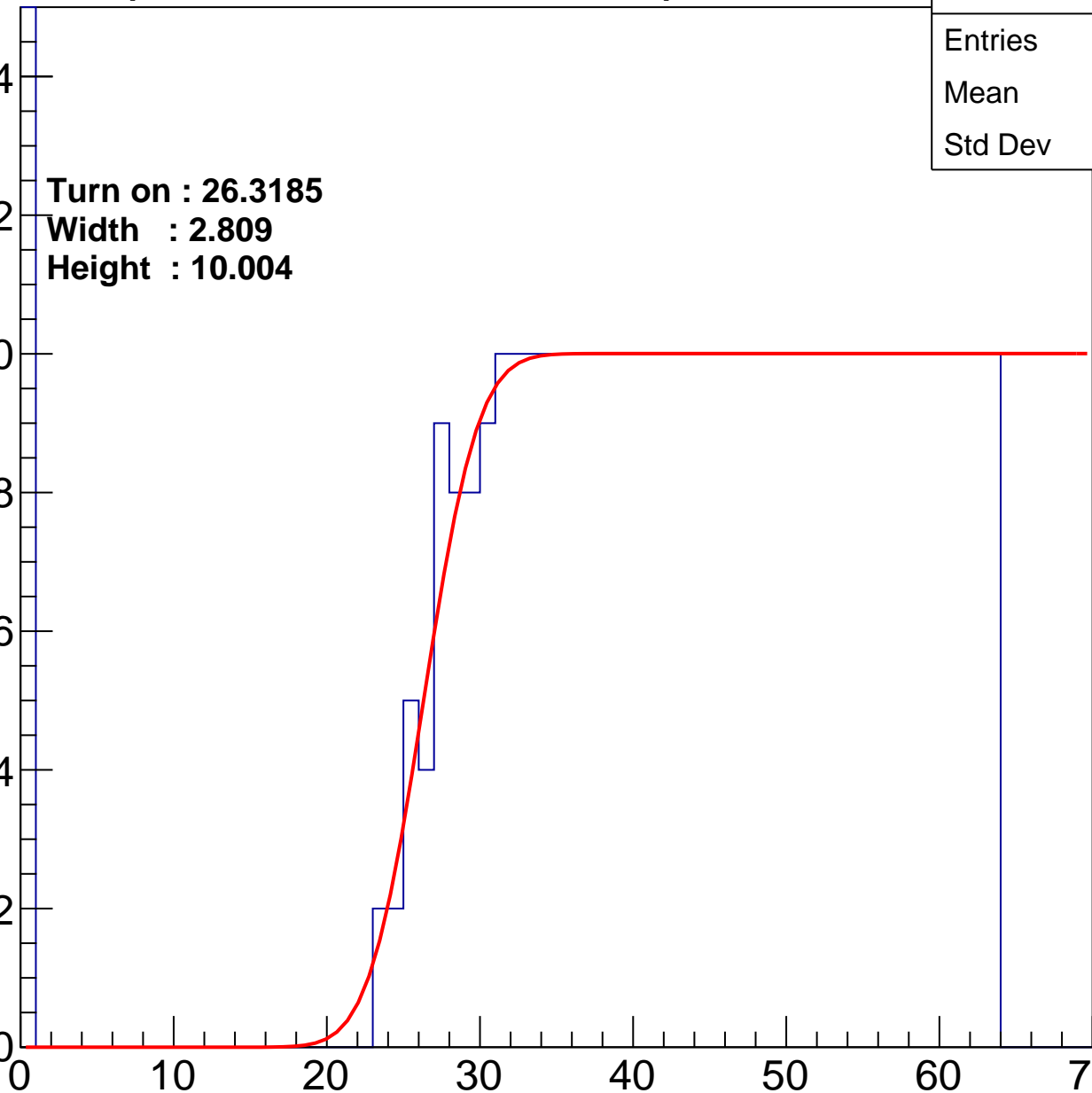
Width : 2.809

Height : 10.004

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U25-ch22

calib_packv5_041523_1651.root, FC#0, port C2

Entries	453
Mean	38.85
Std Dev	17.02

Turn on : 22.3887

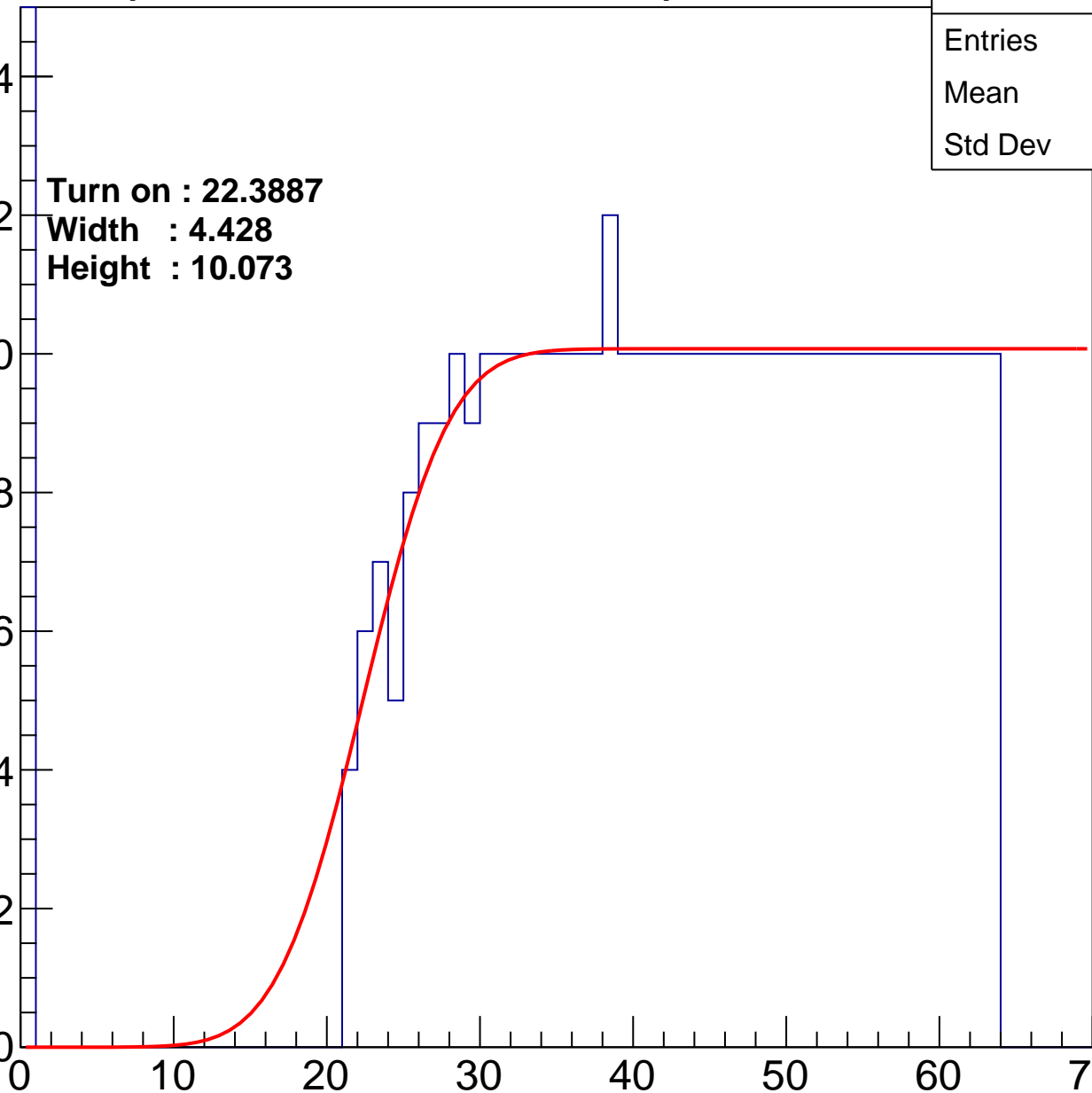
Width : 4.428

Height : 10.073

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U25-ch23

calib_packv5_041523_1651.root, FC#0, port C2

Entries	410
Mean	40.02
Std Dev	17.59

Turn on : 28.0286

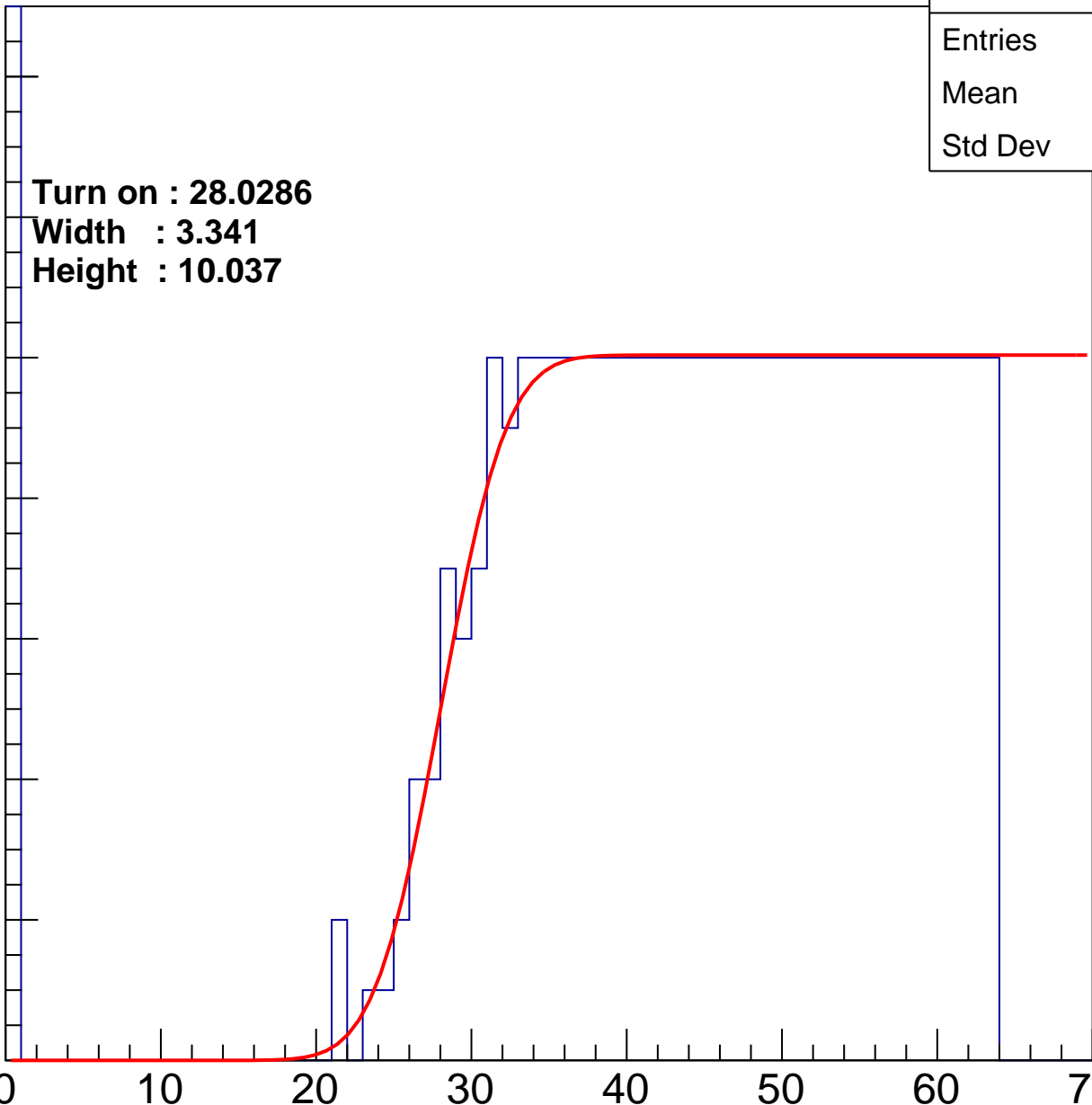
Width : 3.341

Height : 10.037

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U25-ch24

calib_packv5_041523_1651.root, FC#0, port C2

Entries	418
Mean	40.61
Std Dev	16.19

Turn on : 25.6929

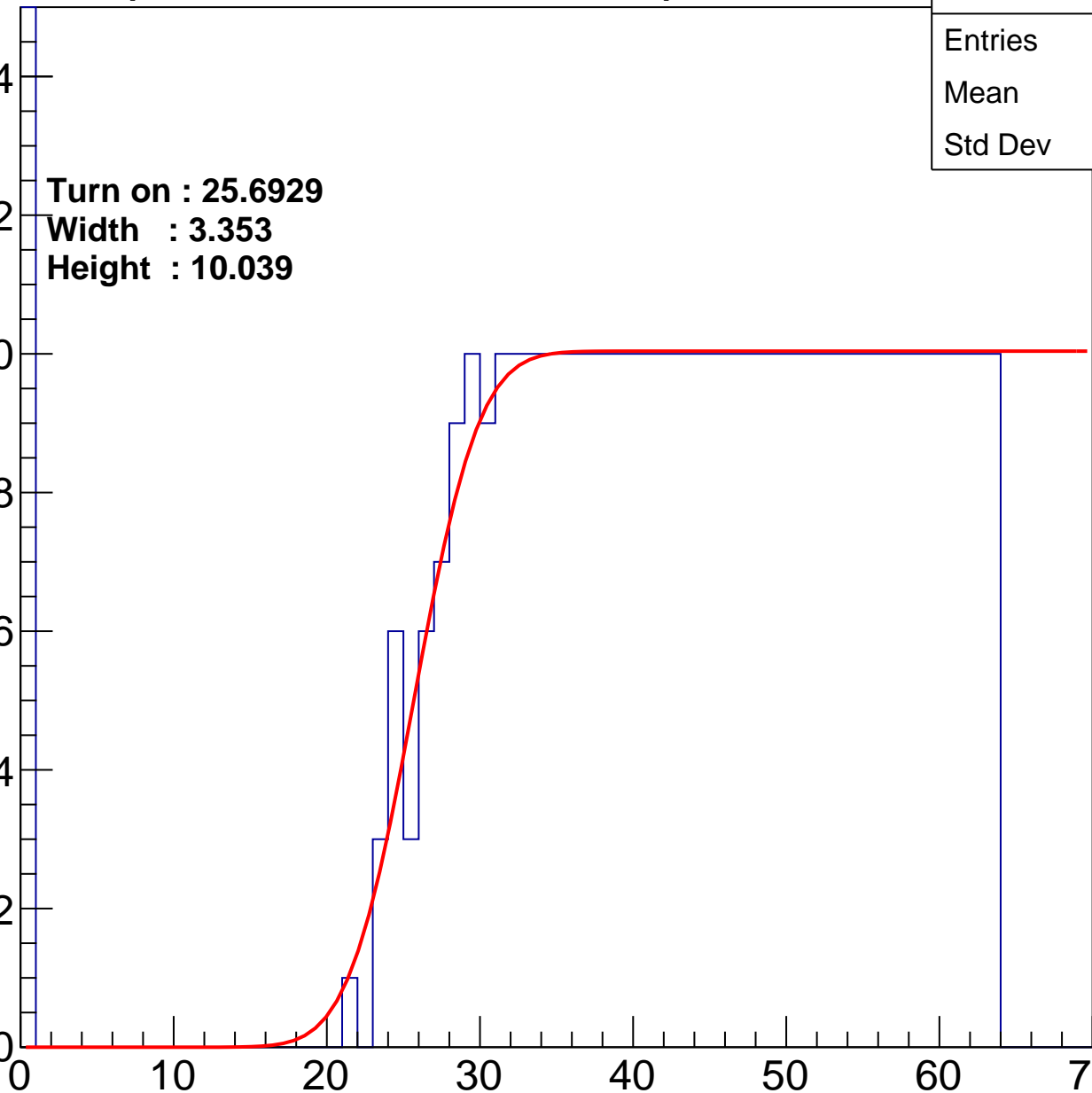
Width : 3.353

Height : 10.039

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U25-ch25

calib_packv5_041523_1651.root, FC#0, port C2

Entries	408
Mean	40.96
Std Dev	16.23

Turn on : 27.0550

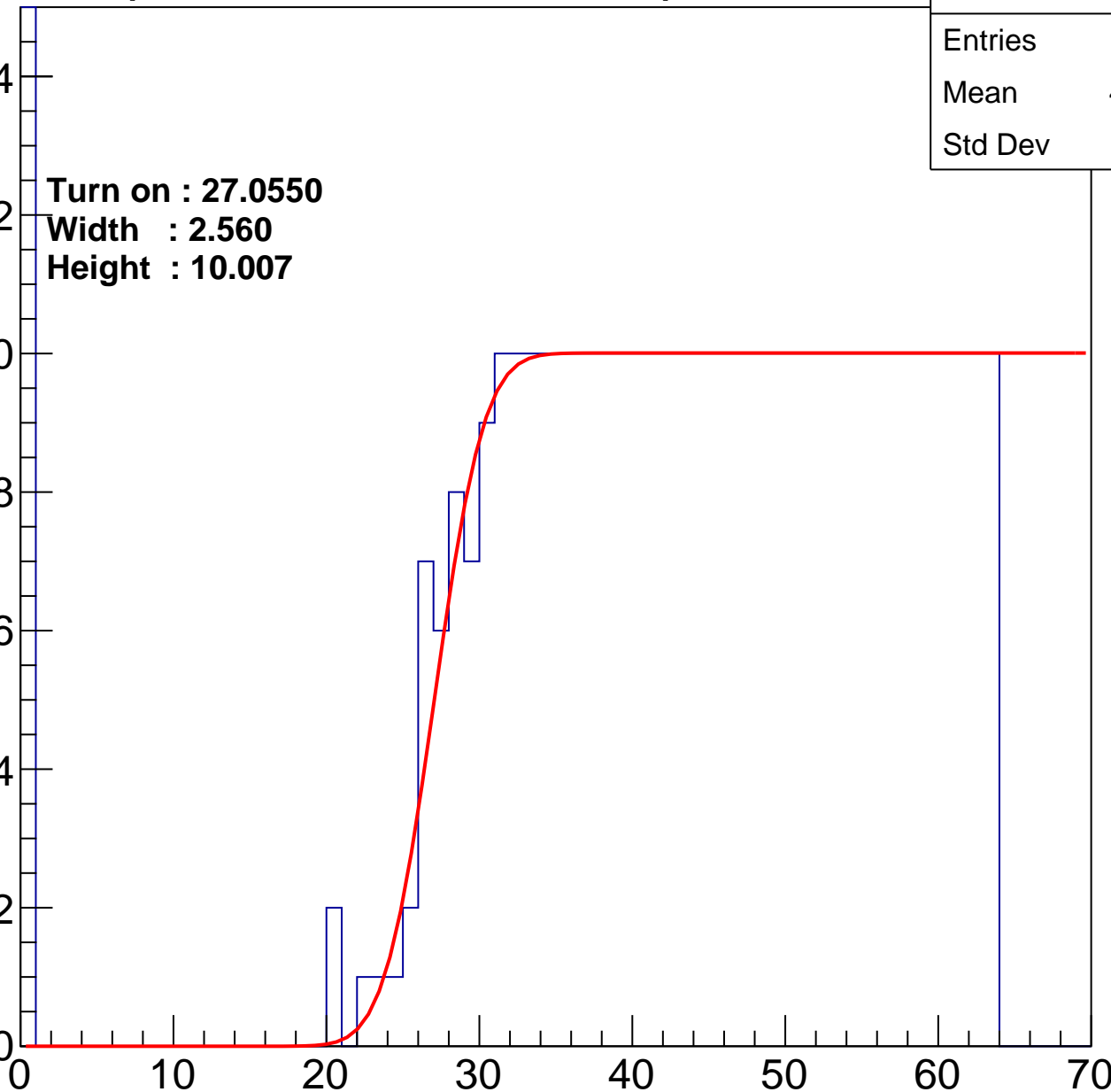
Width : 2.560

Height : 10.007

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U25-ch26

calib_packv5_041523_1651.root, FC#0, port C2

Entries	435
Mean	39.6
Std Dev	16.83

Turn on : 24.7496

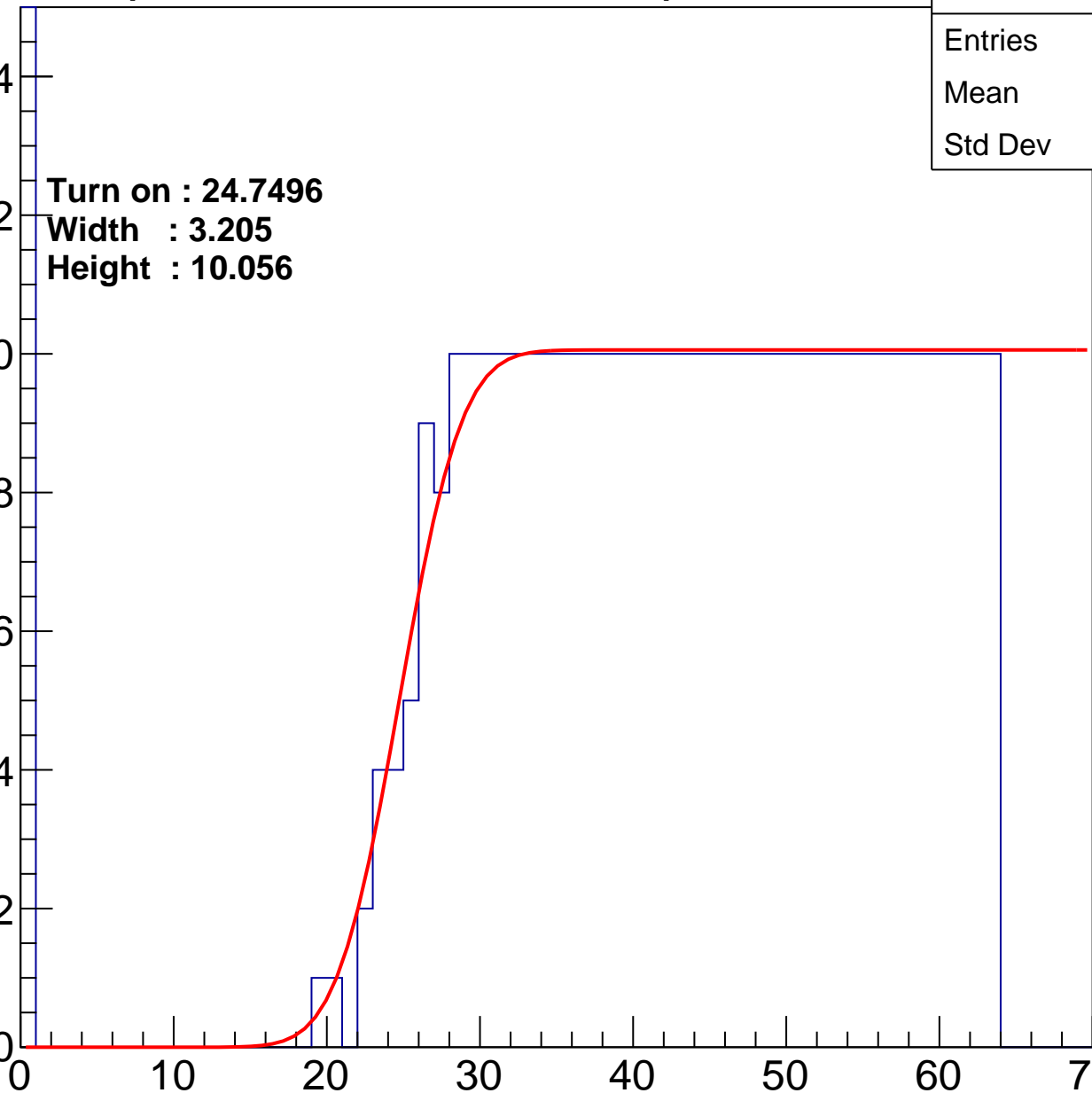
Width : 3.205

Height : 10.056

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U25-ch27

calib_packv5_041523_1651.root, FC#0, port C2

Entries	425
Mean	39.44
Std Dev	17.63

Turn on : 26.9140

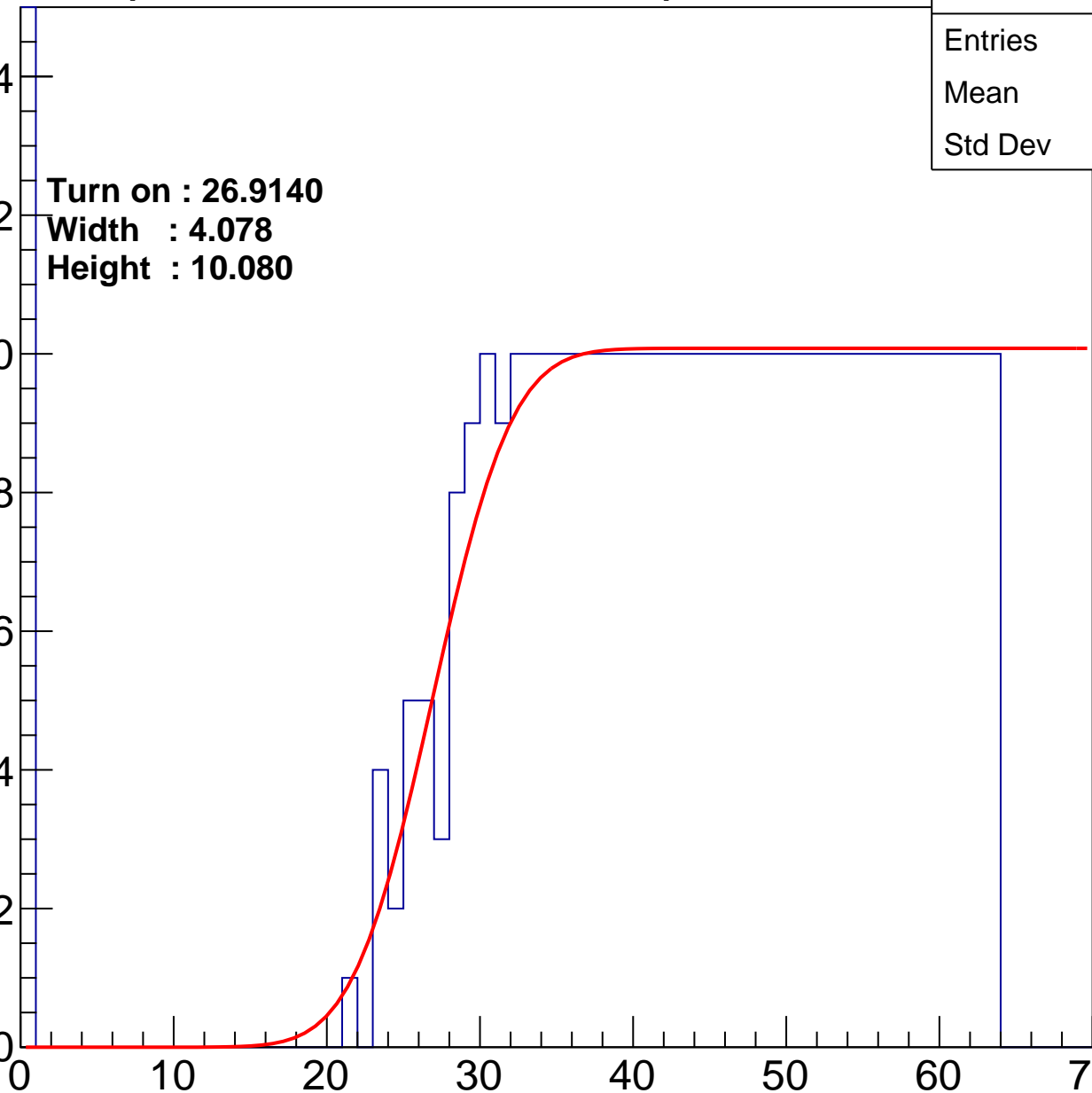
Width : 4.078

Height : 10.080

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U25-ch28

calib_packv5_041523_1651.root, FC#0, port C2

Entries	430
Mean	39.54
Std Dev	17.21

Turn on : 25.7580

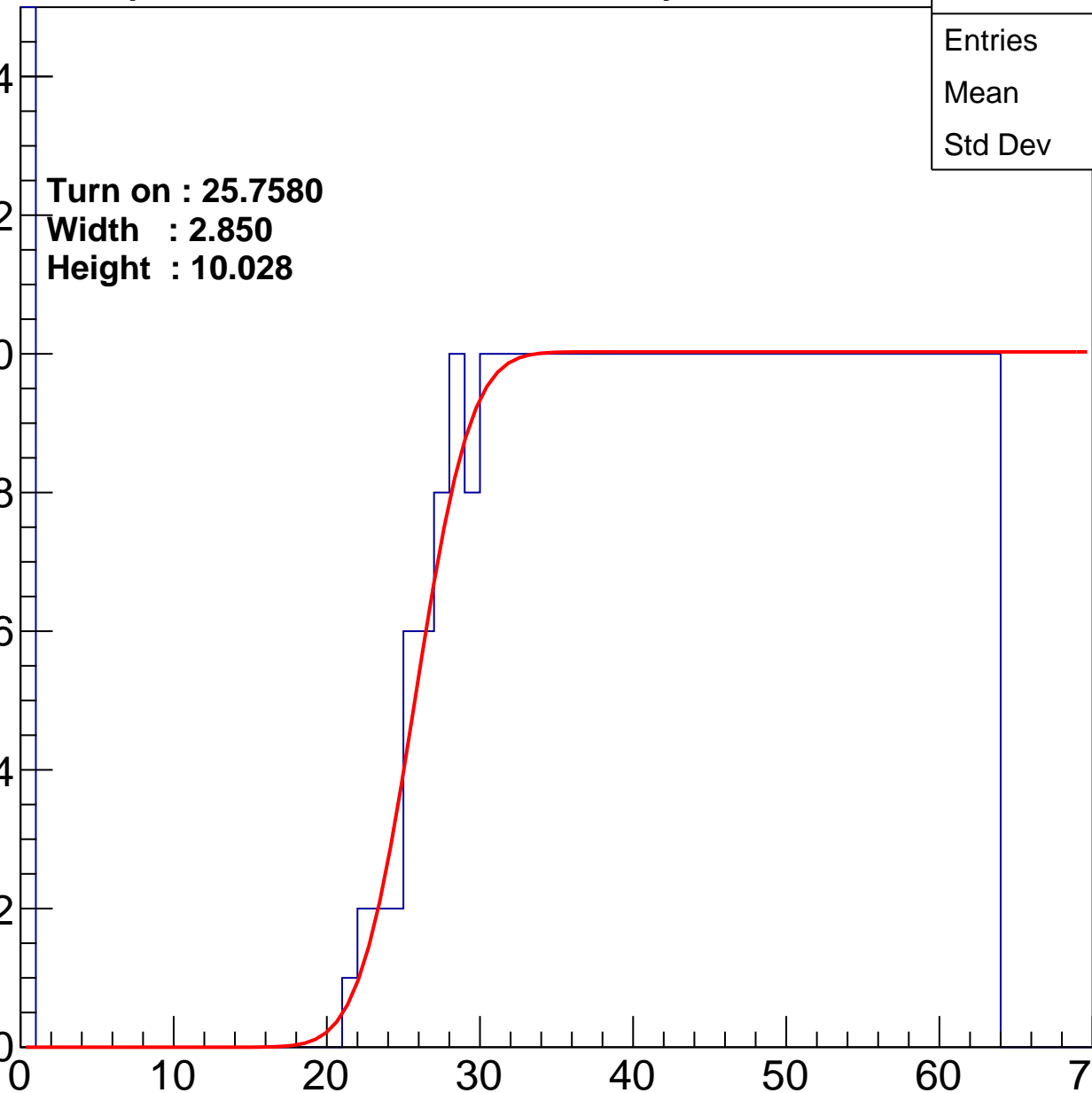
Width : 2.850

Height : 10.028

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U25-ch29

calib_packv5_041523_1651.root, FC#0, port C2

Entries	403
Mean	39.94
Std Dev	18.13

Turn on : 28.6883

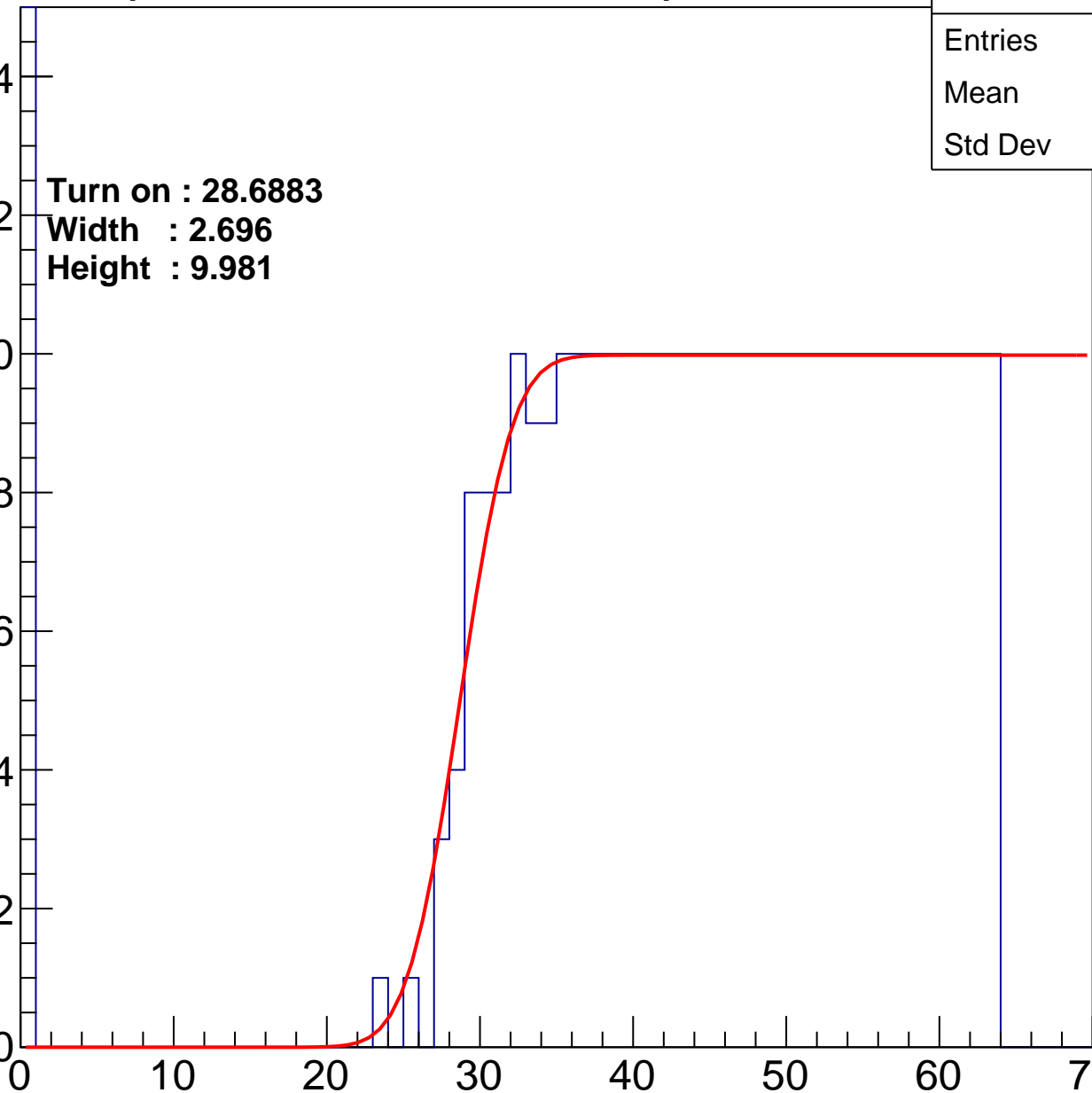
Width : 2.696

Height : 9.981

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U25-ch30

calib_packv5_041523_1651.root, FC#0, port C2

Entries	426
Mean	38.93
Std Dev	18.32

Turn on : 27.0207

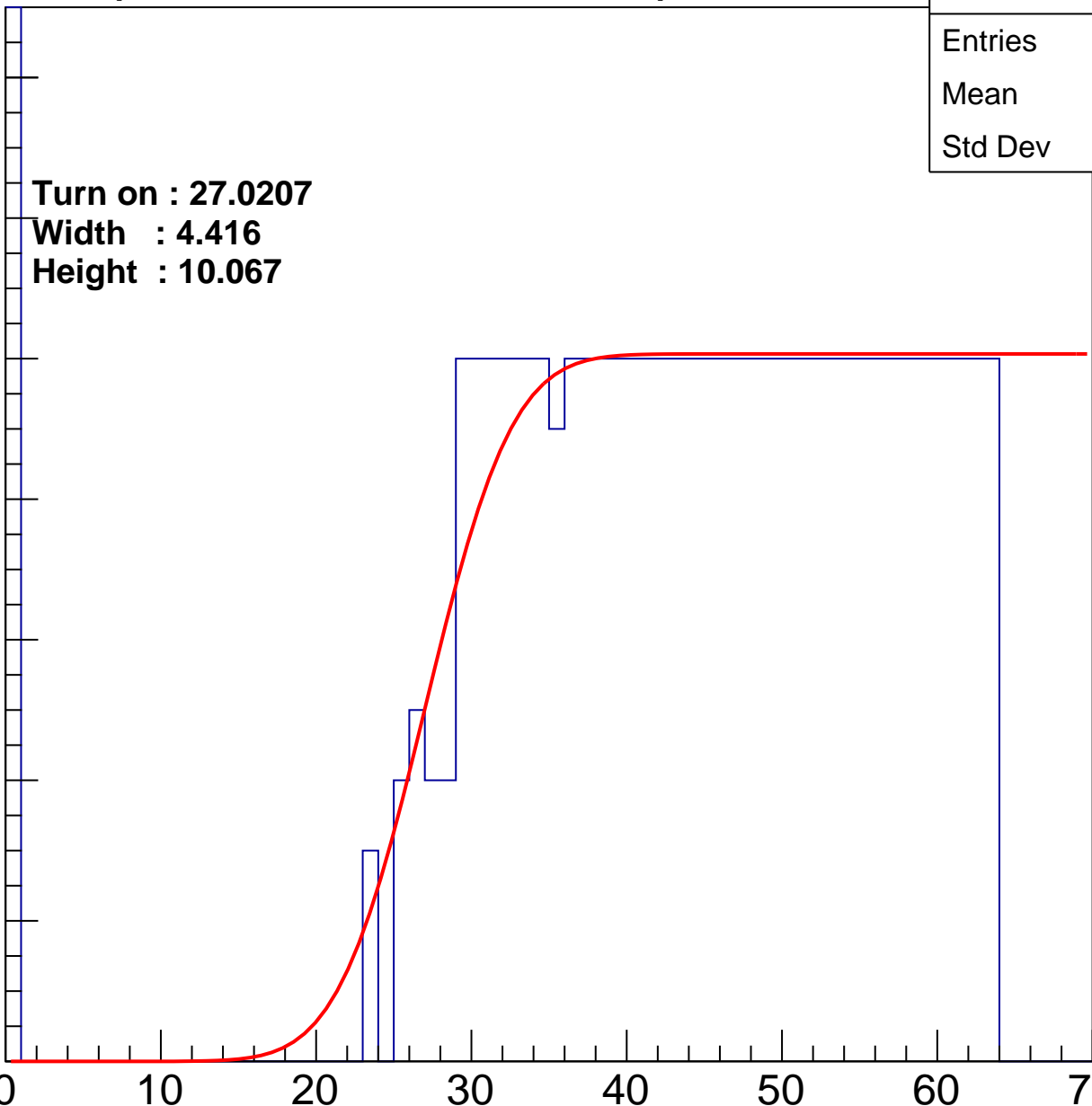
Width : 4.416

Height : 10.067

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U25-ch31

calib_packv5_041523_1651.root, FC#0, port C2

Entries	430
Mean	39.13
Std Dev	17.83

Turn on : 26.2801

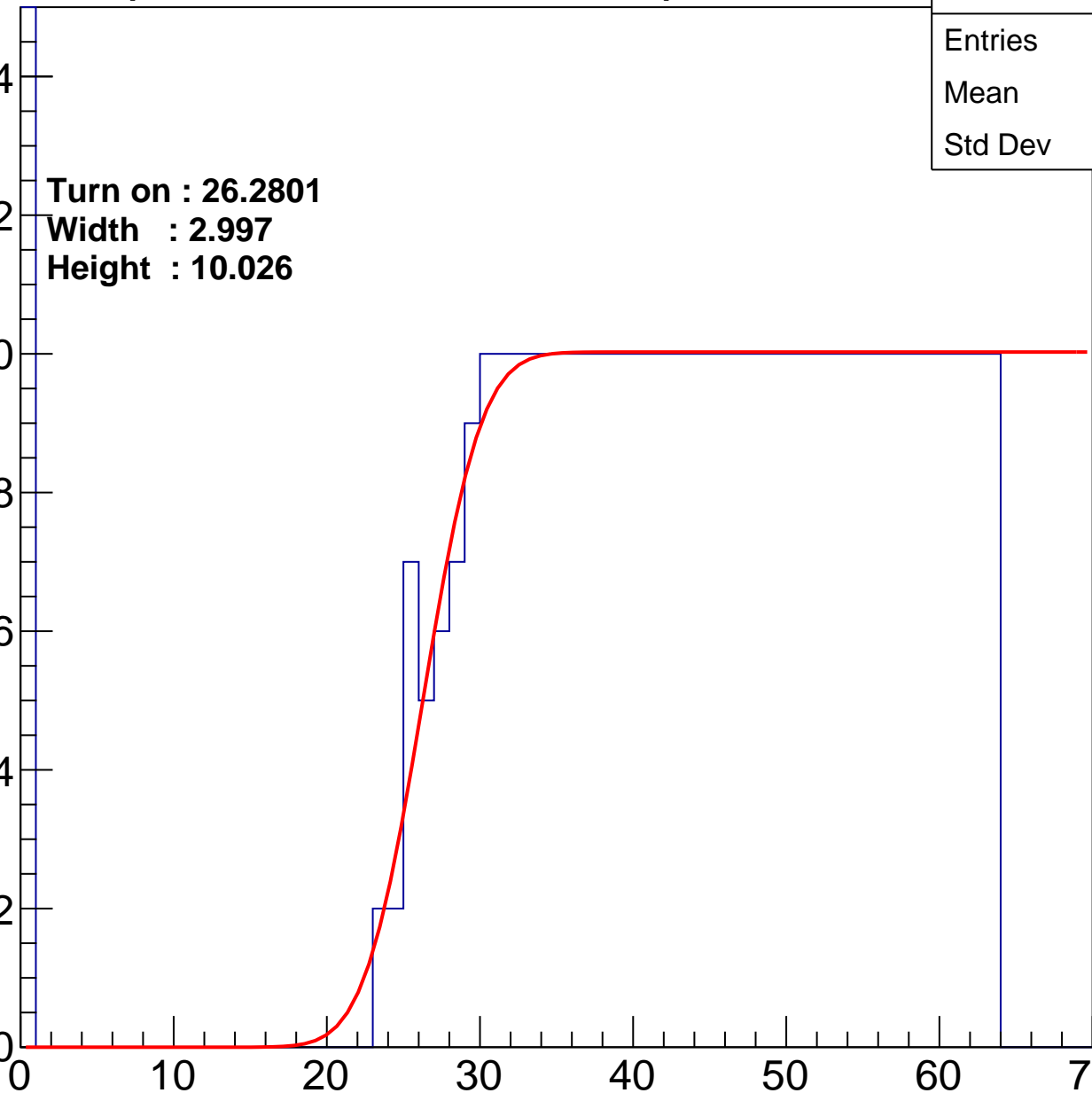
Width : 2.997

Height : 10.026

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U25-ch32

calib_packv5_041523_1651.root, FC#0, port C2

Entries	445
Mean	38.65
Std Dev	17.73

Turn on : 25.2737

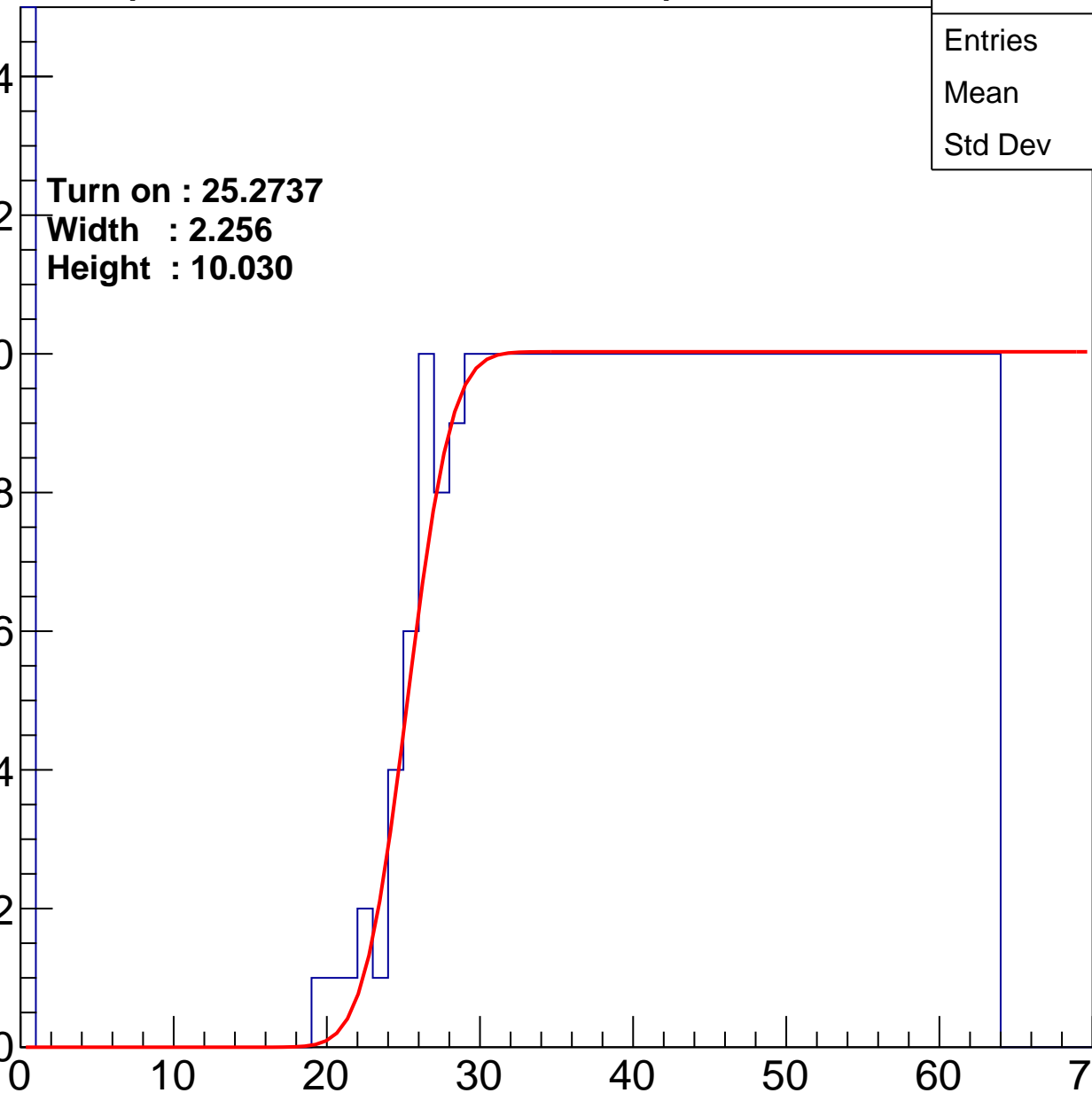
Width : 2.256

Height : 10.030

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U25-ch33

calib_packv5_041523_1651.root, FC#0, port C2

Entries	414
Mean	40.04
Std Dev	17.35

Turn on : 27.3618

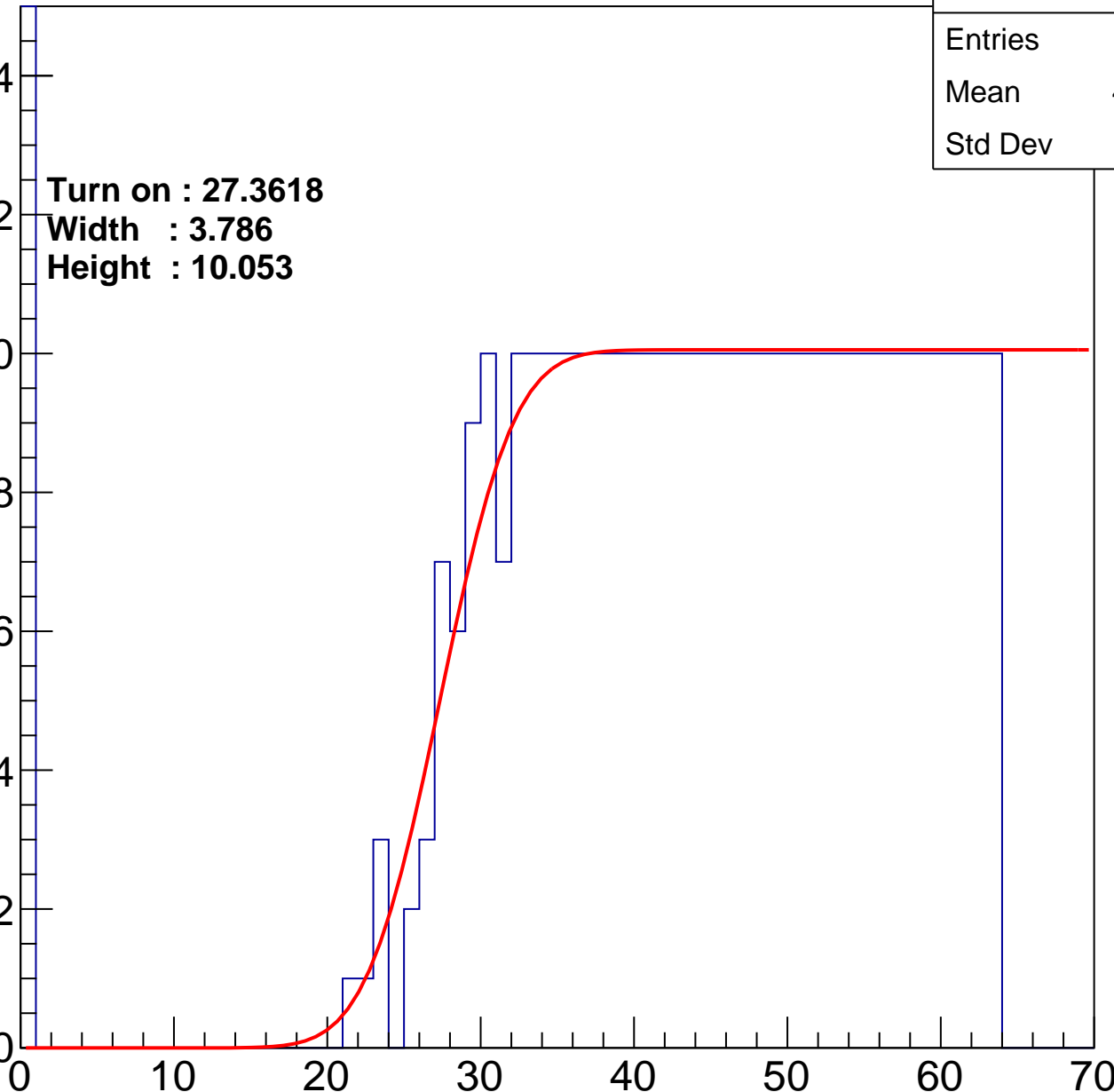
Width : 3.786

Height : 10.053

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U25-ch34

calib_packv5_041523_1651.root, FC#0, port C2

Entries	456
Mean	38.11
Std Dev	17.92

Turn on : 25.1948

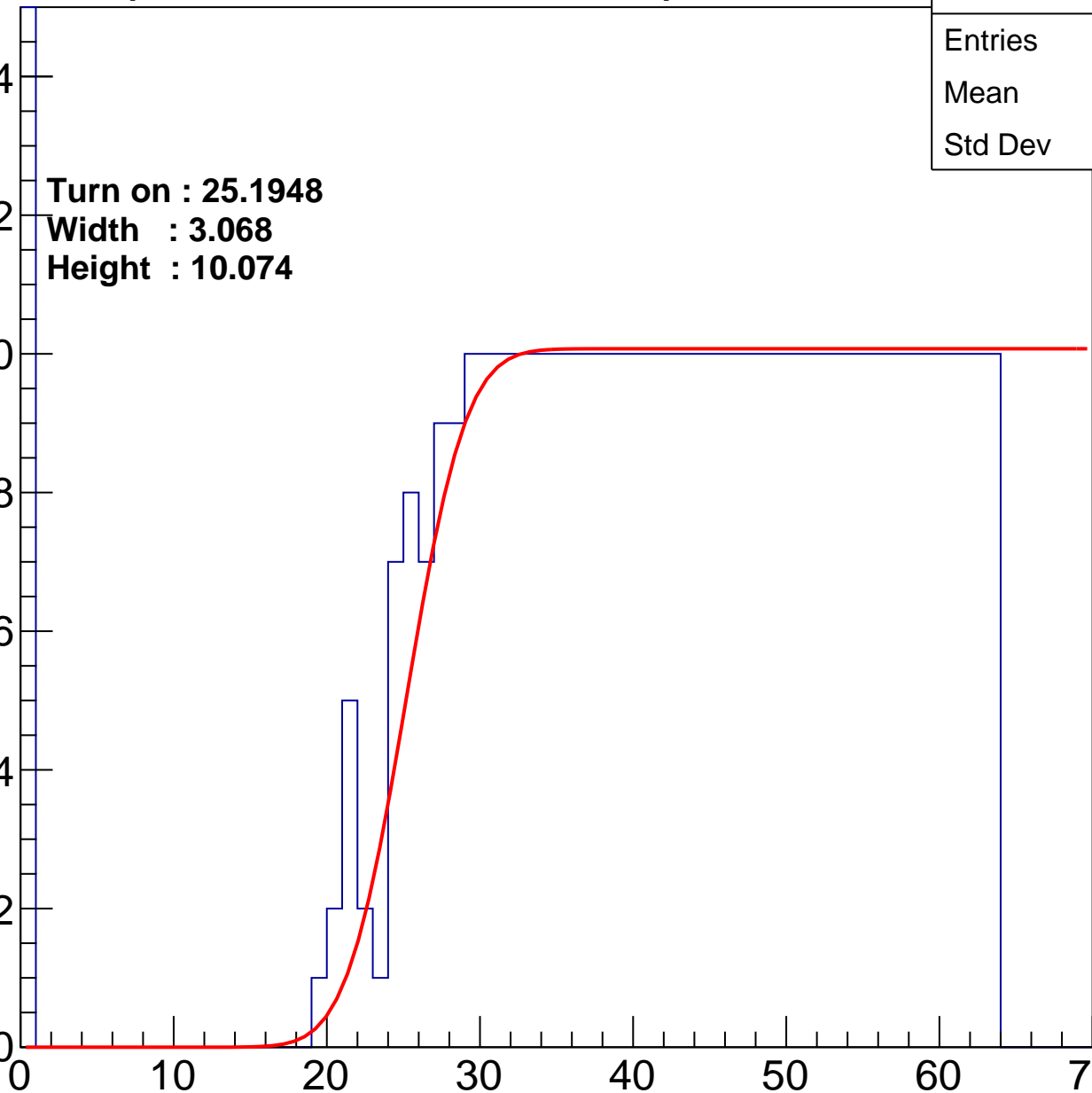
Width : 3.068

Height : 10.074

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U25-ch35

calib_packv5_041523_1651.root, FC#0, port C2

Entries	418
Mean	40.08
Std Dev	17.08

Turn on : 26.6971

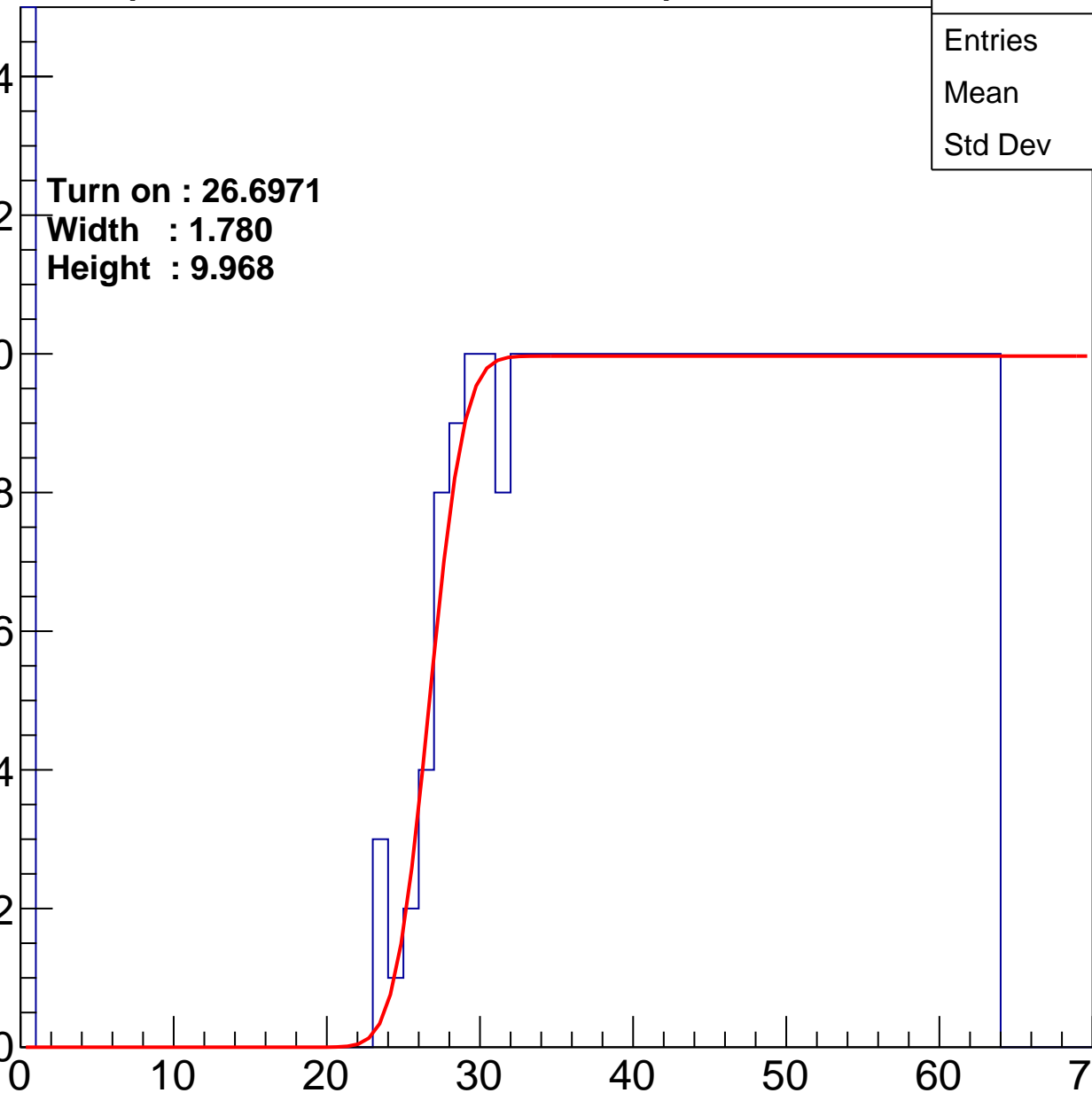
Width : 1.780

Height : 9.968

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U25-ch36

calib_packv5_041523_1651.root, FC#0, port C2

Entries	446
Mean	38.77
Std Dev	17.54

Turn on : 24.2491

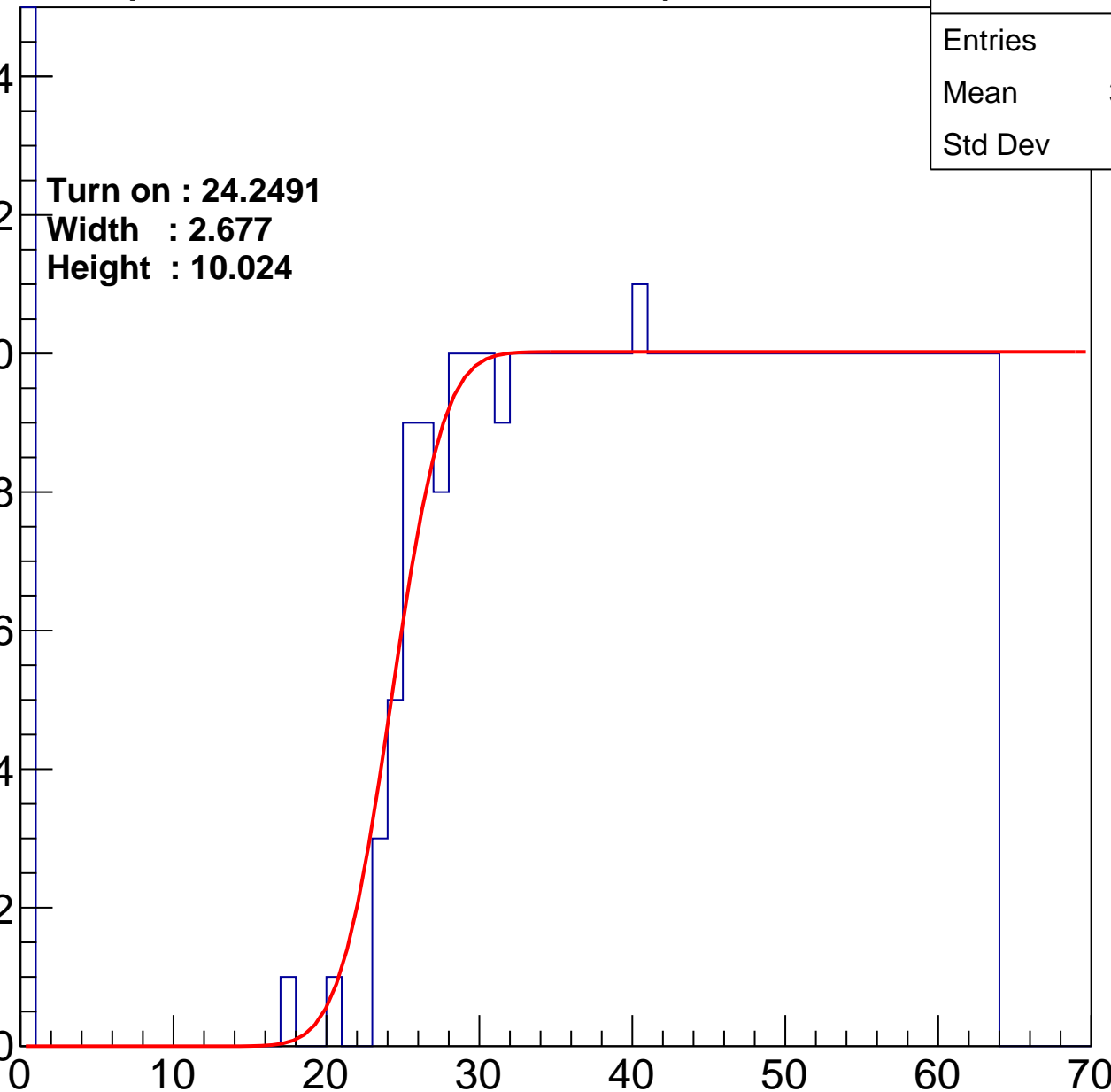
Width : 2.677

Height : 10.024

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U25-ch37

calib_packv5_041523_1651.root, FC#0, port C2

Entries	434
Mean	39.16
Std Dev	17.56

Turn on : 25.8317

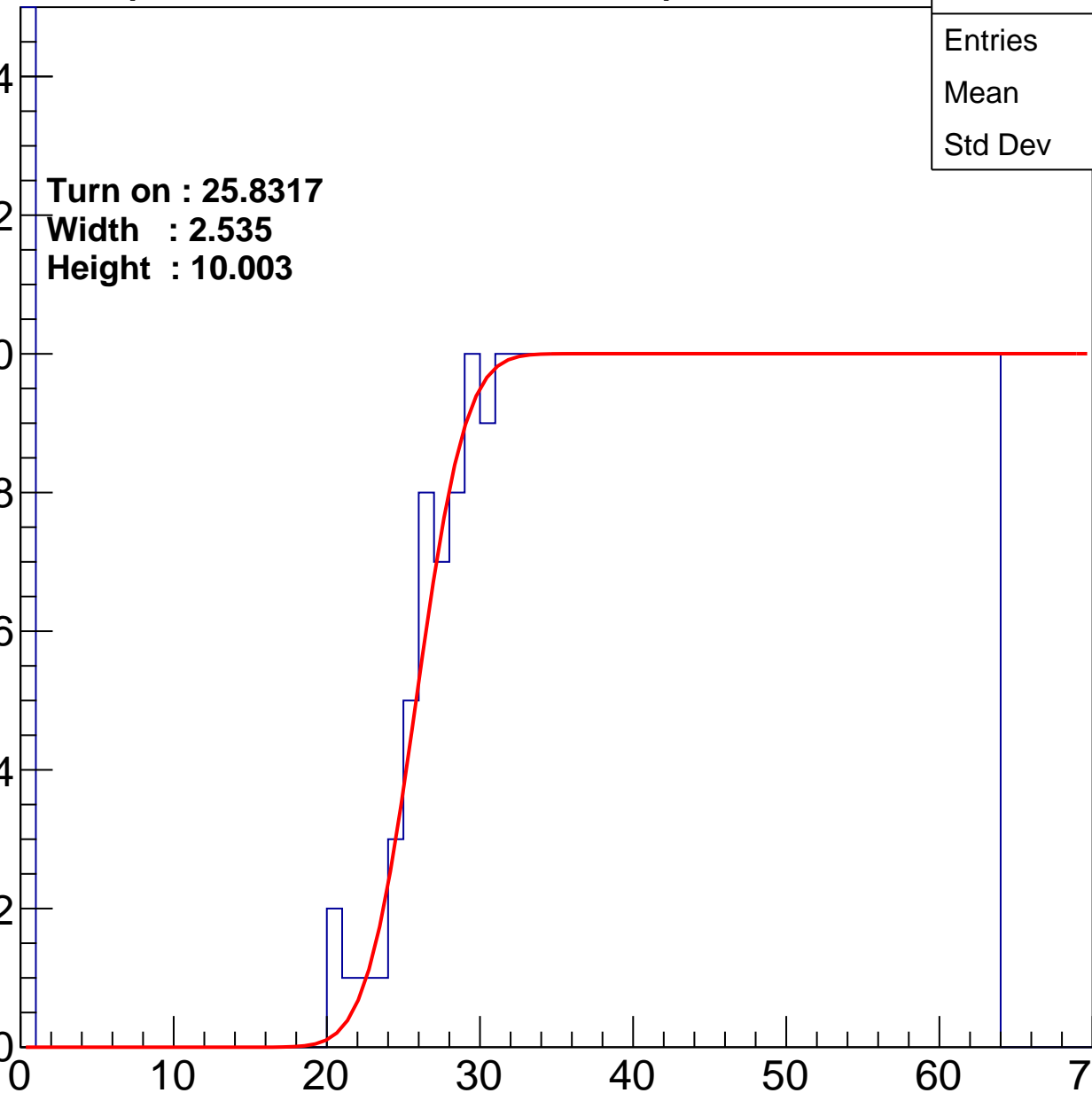
Width : 2.535

Height : 10.003

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U25-ch38

calib_packv5_041523_1651.root, FC#0, port C2

Entries	418
Mean	40.35
Std Dev	16.62

Turn on : 25.8348

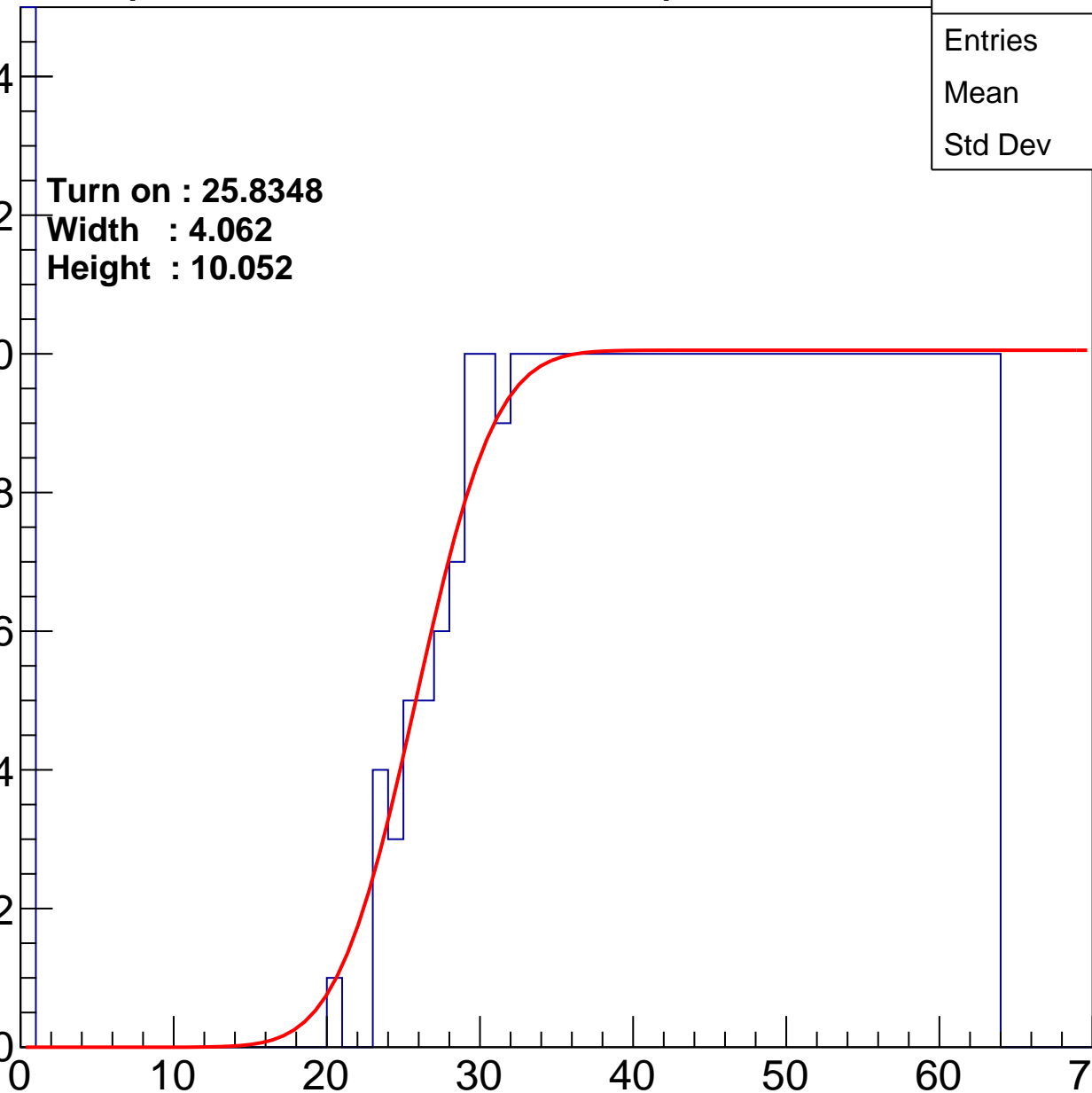
Width : 4.062

Height : 10.052

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U25-ch39

calib_packv5_041523_1651.root, FC#0, port C2

Entries	435
Mean	39.49
Std Dev	17

Turn on : 25.1737

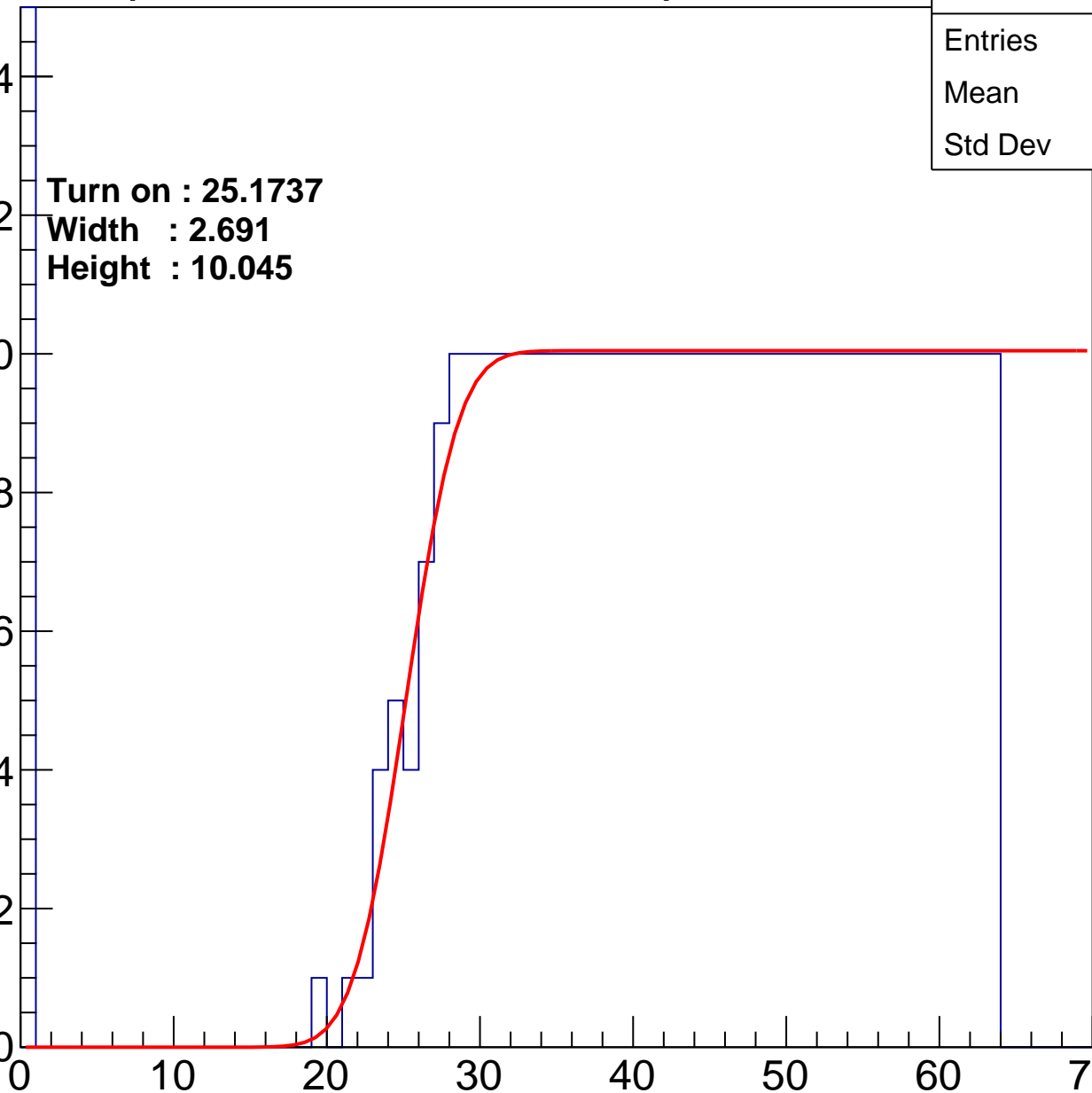
Width : 2.691

Height : 10.045

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U25-ch40

calib_packv5_041523_1651.root, FC#0, port C2

Entries	435
Mean	39.87
Std Dev	16.67

Turn on : 25.0314

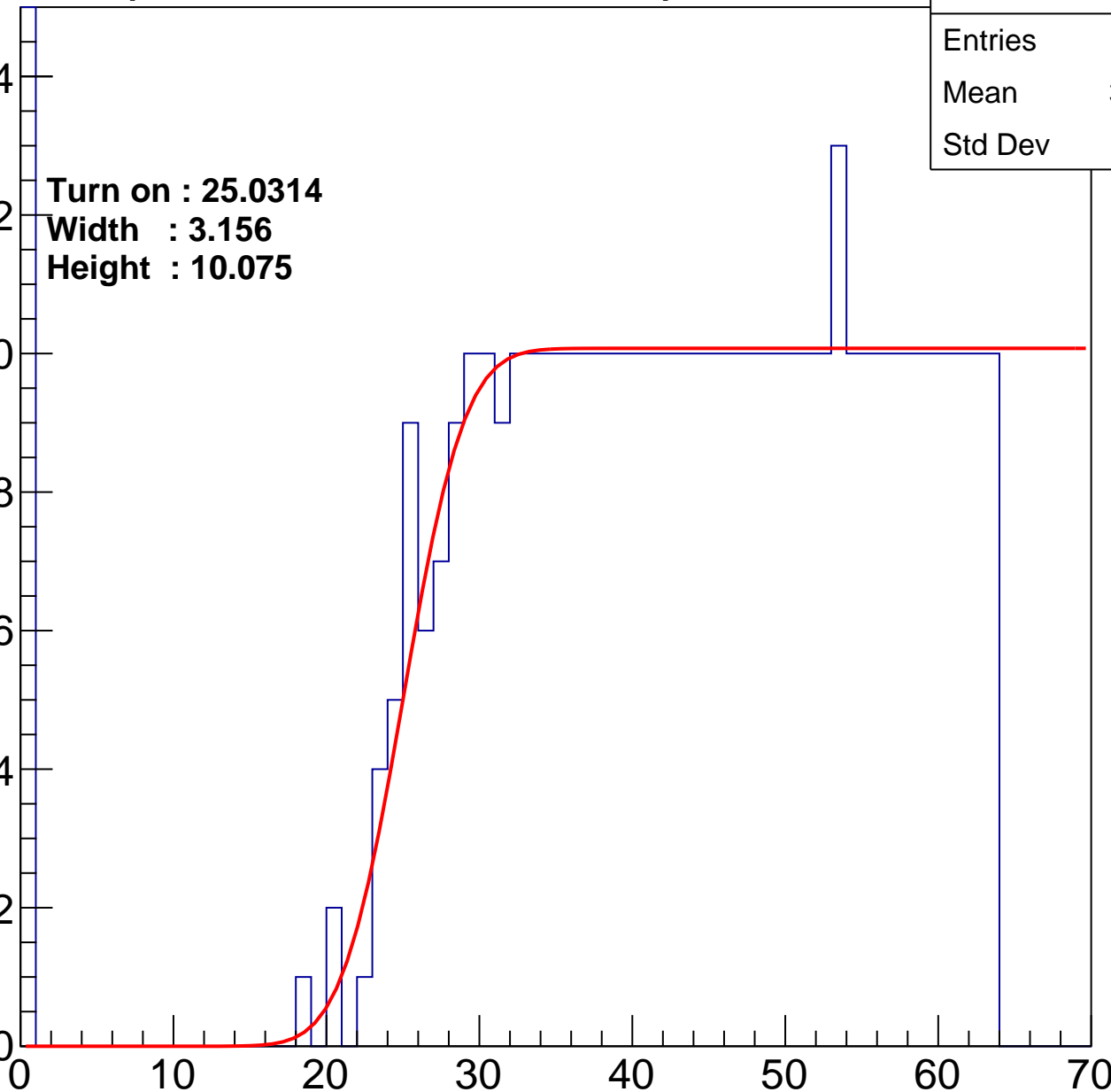
Width : 3.156

Height : 10.075

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U25-ch41

calib_packv5_041523_1651.root, FC#0, port C2

Entries	419
Mean	39.8
Std Dev	17.4

Turn on : 26.5504

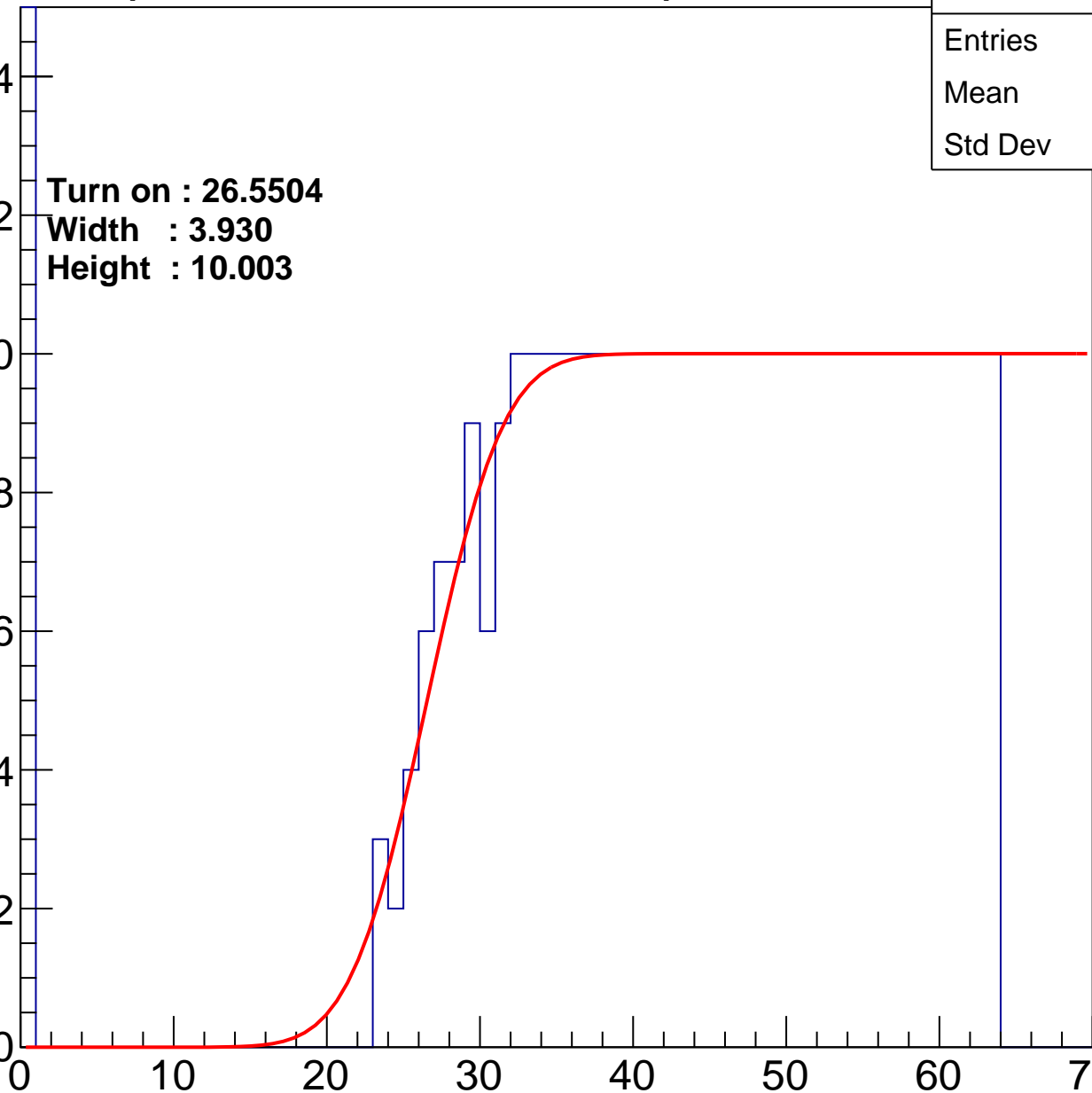
Width : 3.930

Height : 10.003

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U25-ch42

calib_packv5_041523_1651.root, FC#0, port C2

Entries	426
Mean	40.05
Std Dev	16.6

Turn on : 25.5910

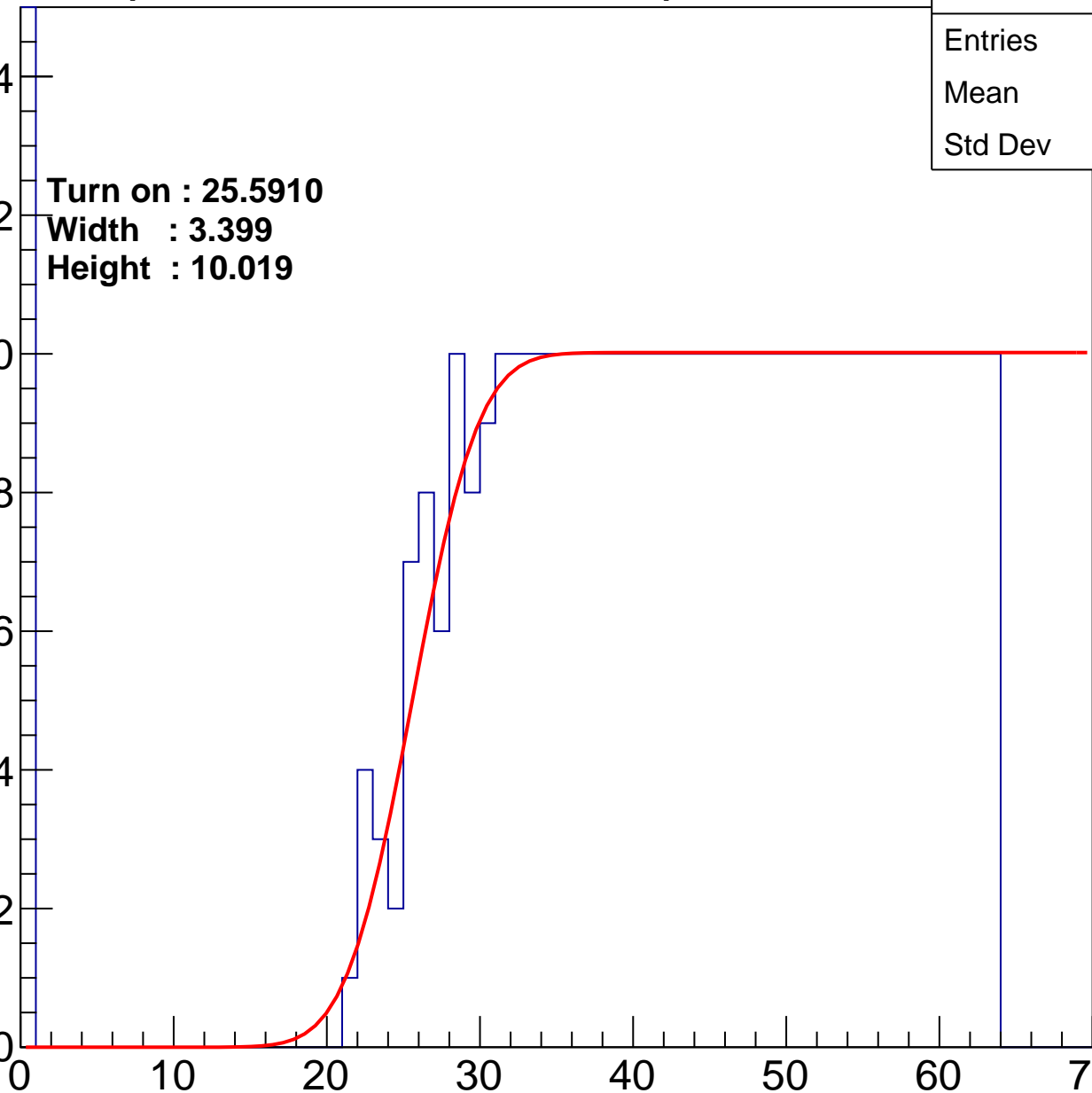
Width : 3.399

Height : 10.019

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U25-ch43

calib_packv5_041523_1651.root, FC#0, port C2

Entries	449
Mean	38.51
Std Dev	17.71

Turn on : 24.5555

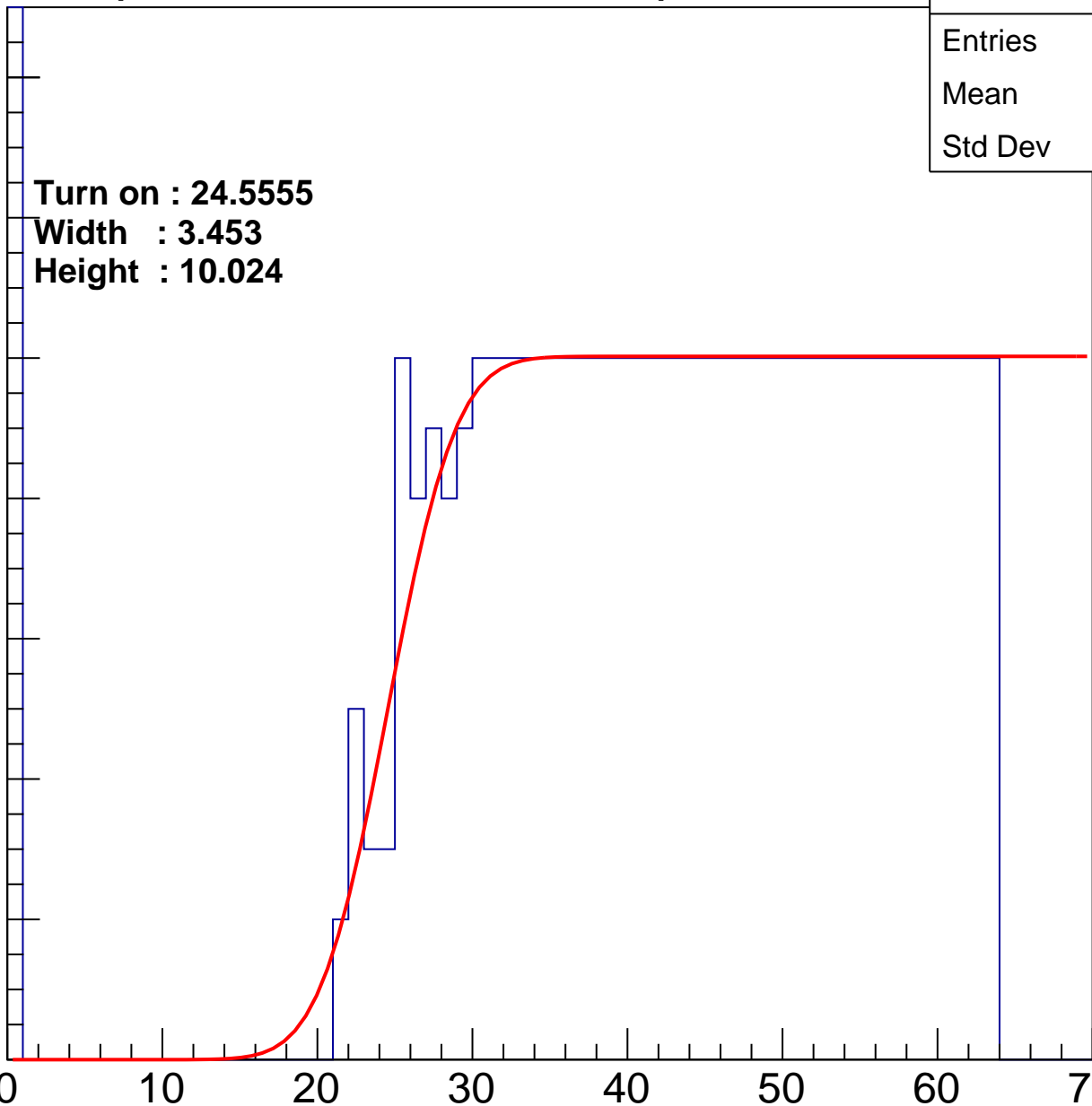
Width : 3.453

Height : 10.024

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U25-ch44

calib_packv5_041523_1651.root, FC#0, port C2

Entries	446
Mean	38.94
Std Dev	17.19

Turn on : 23.9343

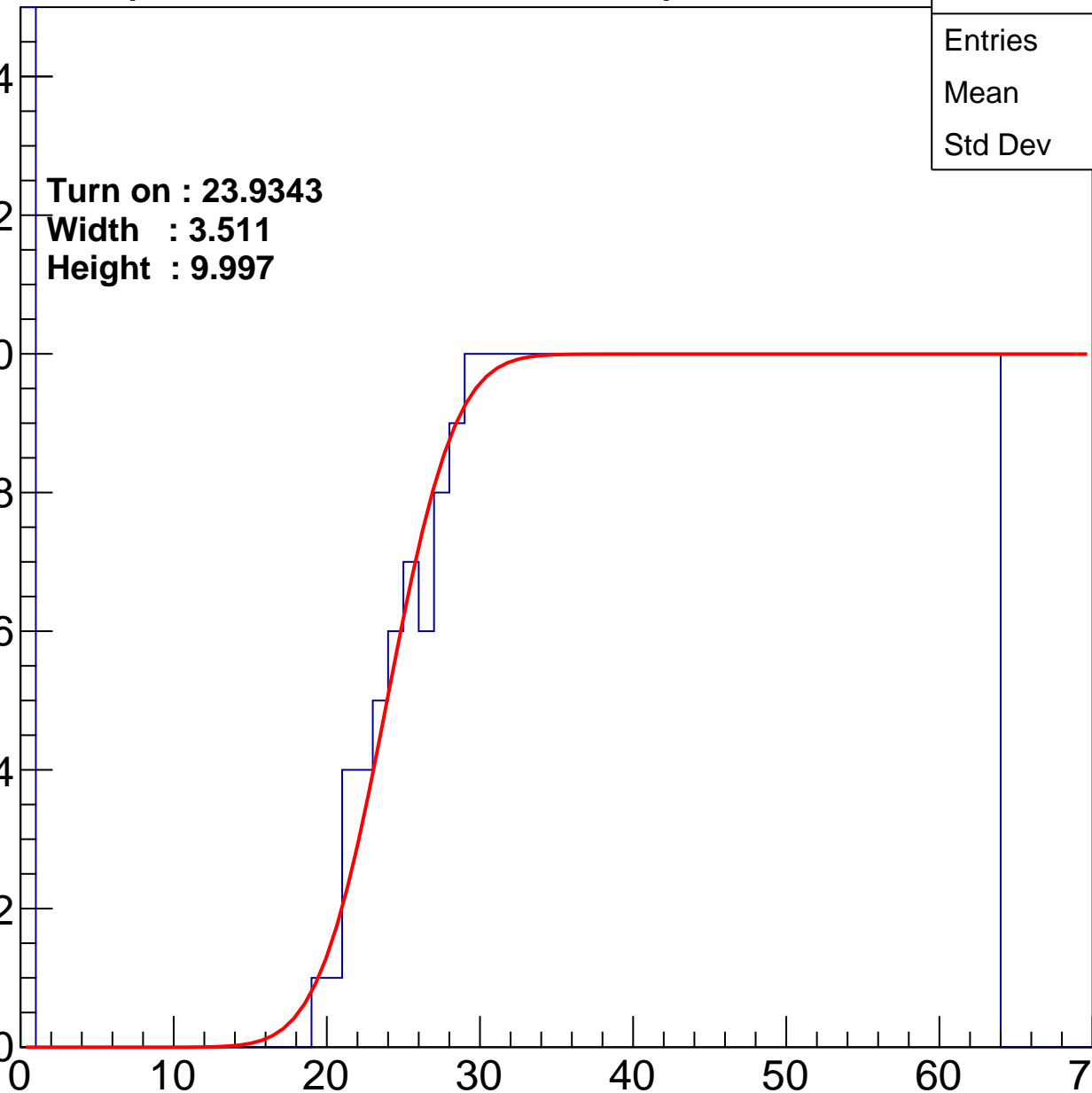
Width : 3.511

Height : 9.997

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U25-ch45

calib_packv5_041523_1651.root, FC#0, port C2

Entries	431
Mean	39.26
Std Dev	17.57

Turn on : 27.0233

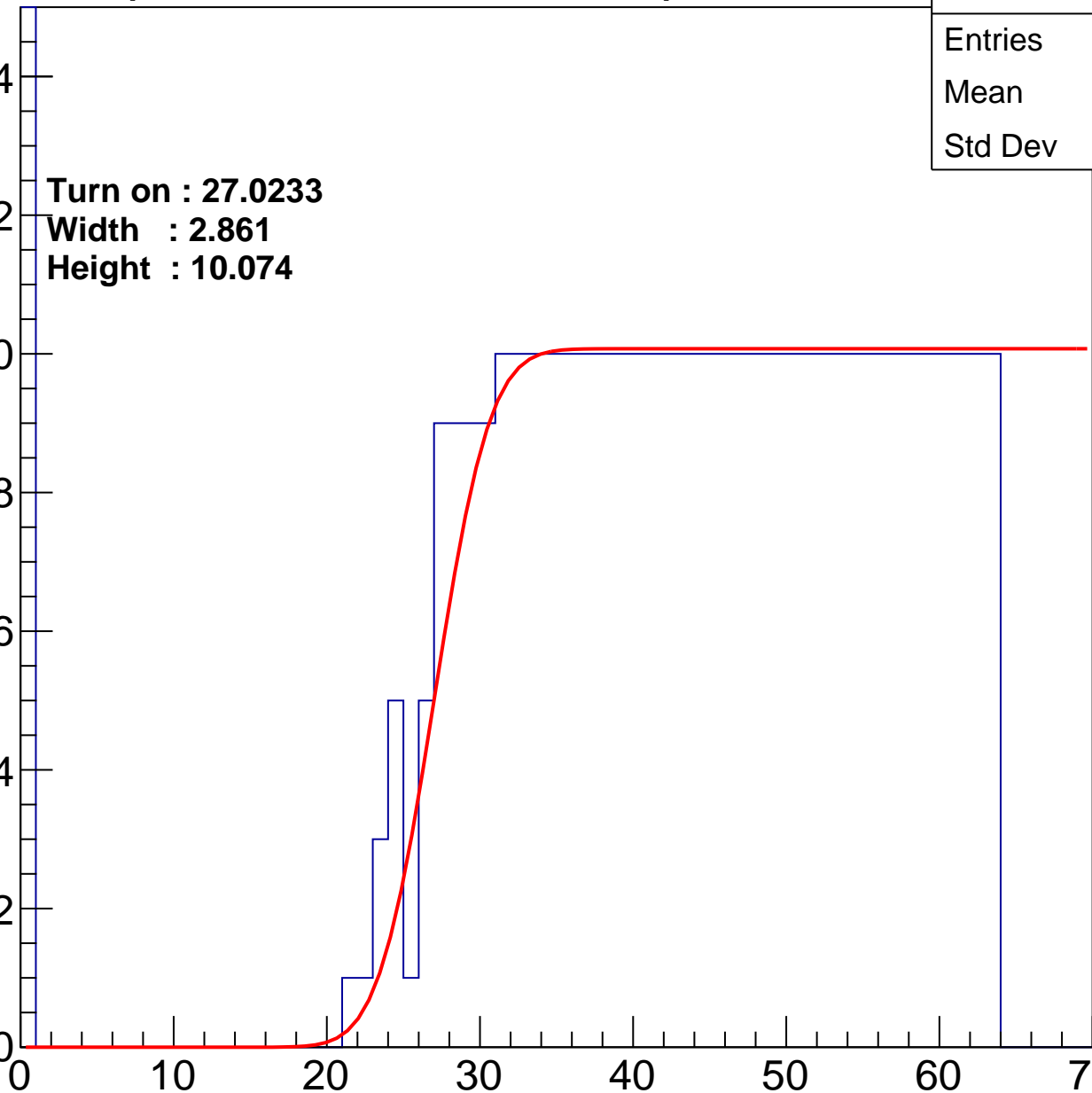
Width : 2.861

Height : 10.074

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U25-ch46

calib_packv5_041523_1651.root, FC#0, port C2

Entries	437
Mean	39.5
Std Dev	16.85

Turn on : 24.7099

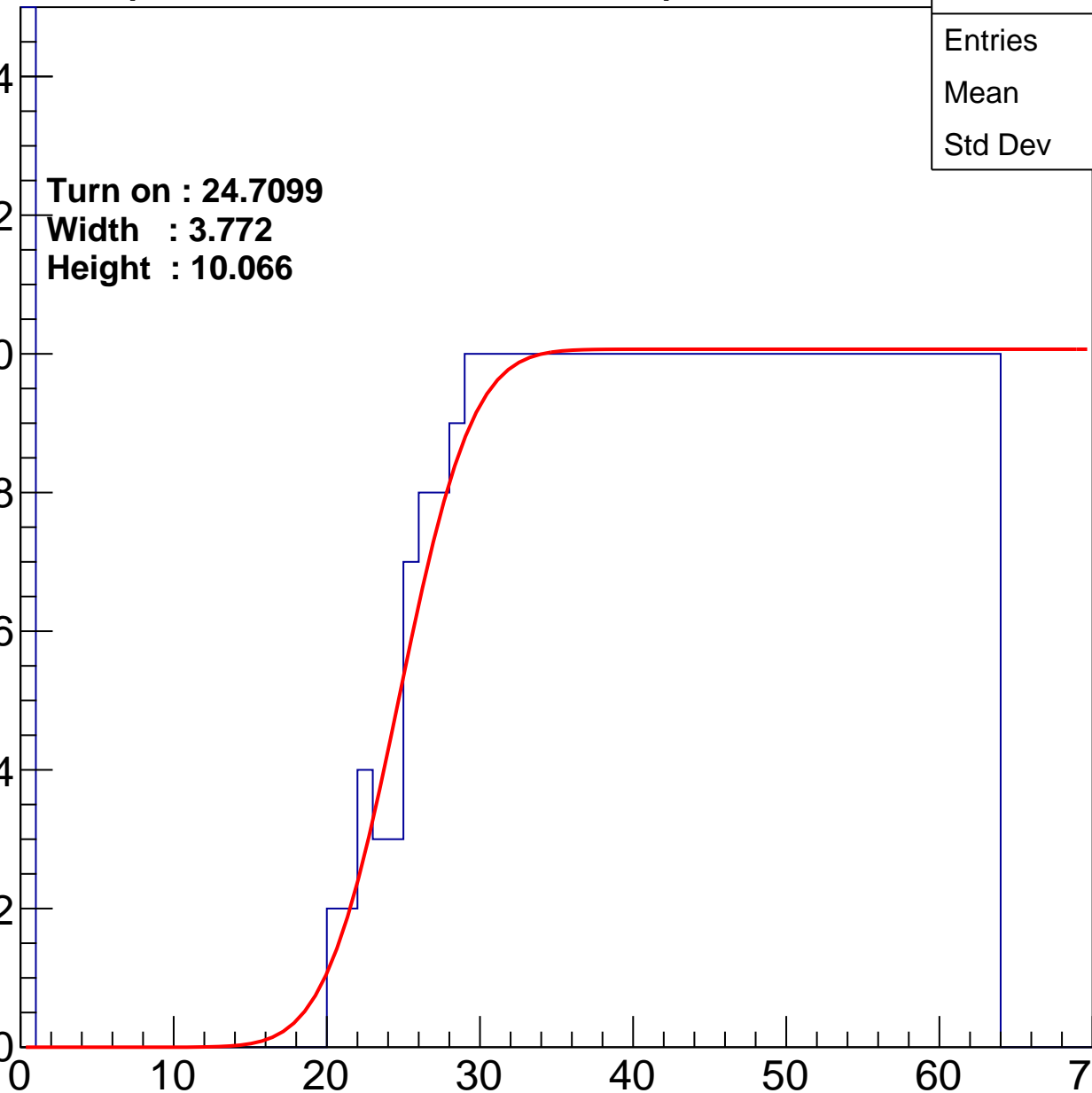
Width : 3.772

Height : 10.066

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U25-ch47

calib_packv5_041523_1651.root, FC#0, port C2

Entries	423
Mean	39.61
Std Dev	17.47

Turn on : 26.5745

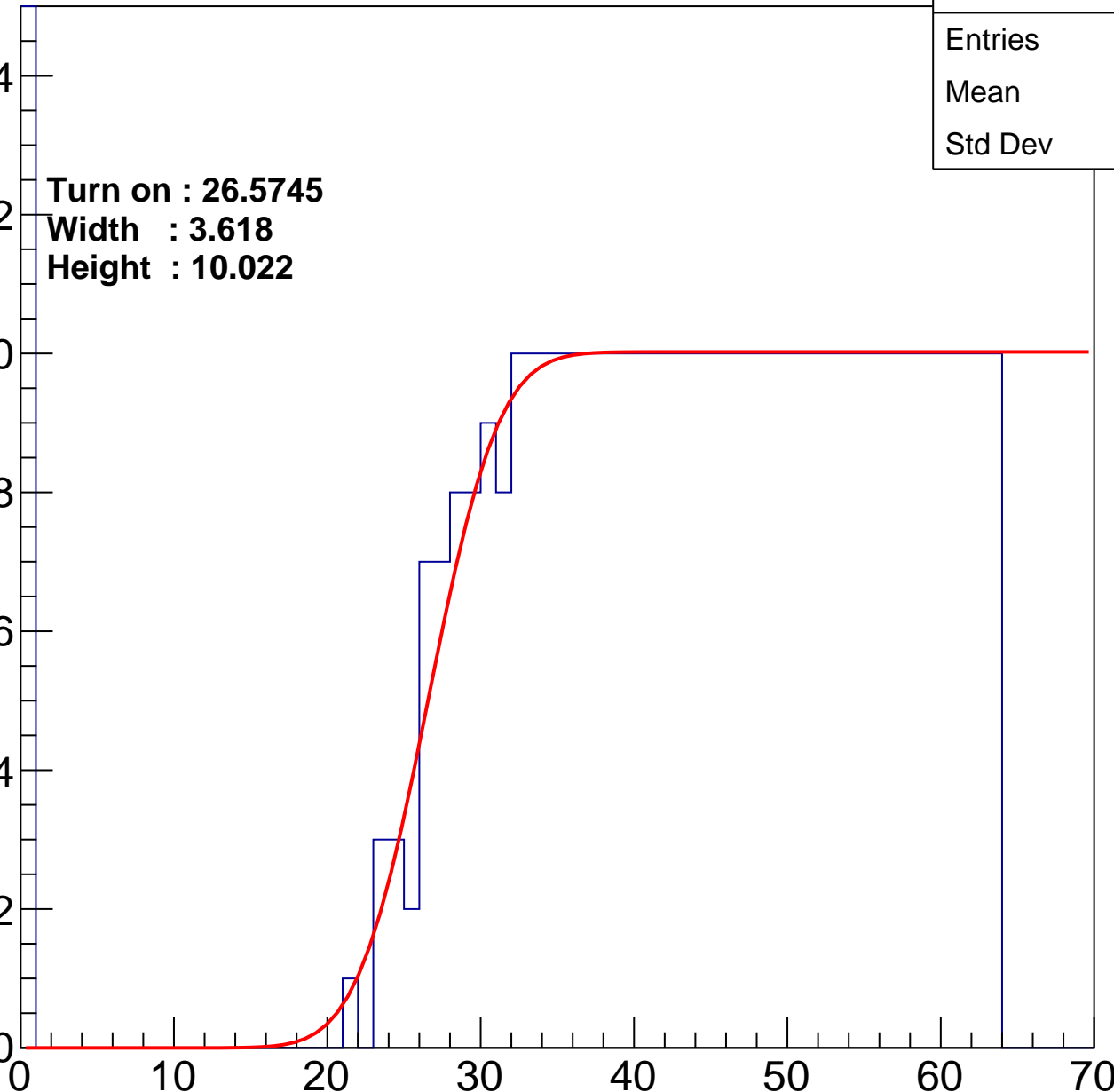
Width : 3.618

Height : 10.022

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U25-ch48

calib_packv5_041523_1651.root, FC#0, port C2

Entries	440
Mean	39.23
Std Dev	17.1

Turn on : 24.2855

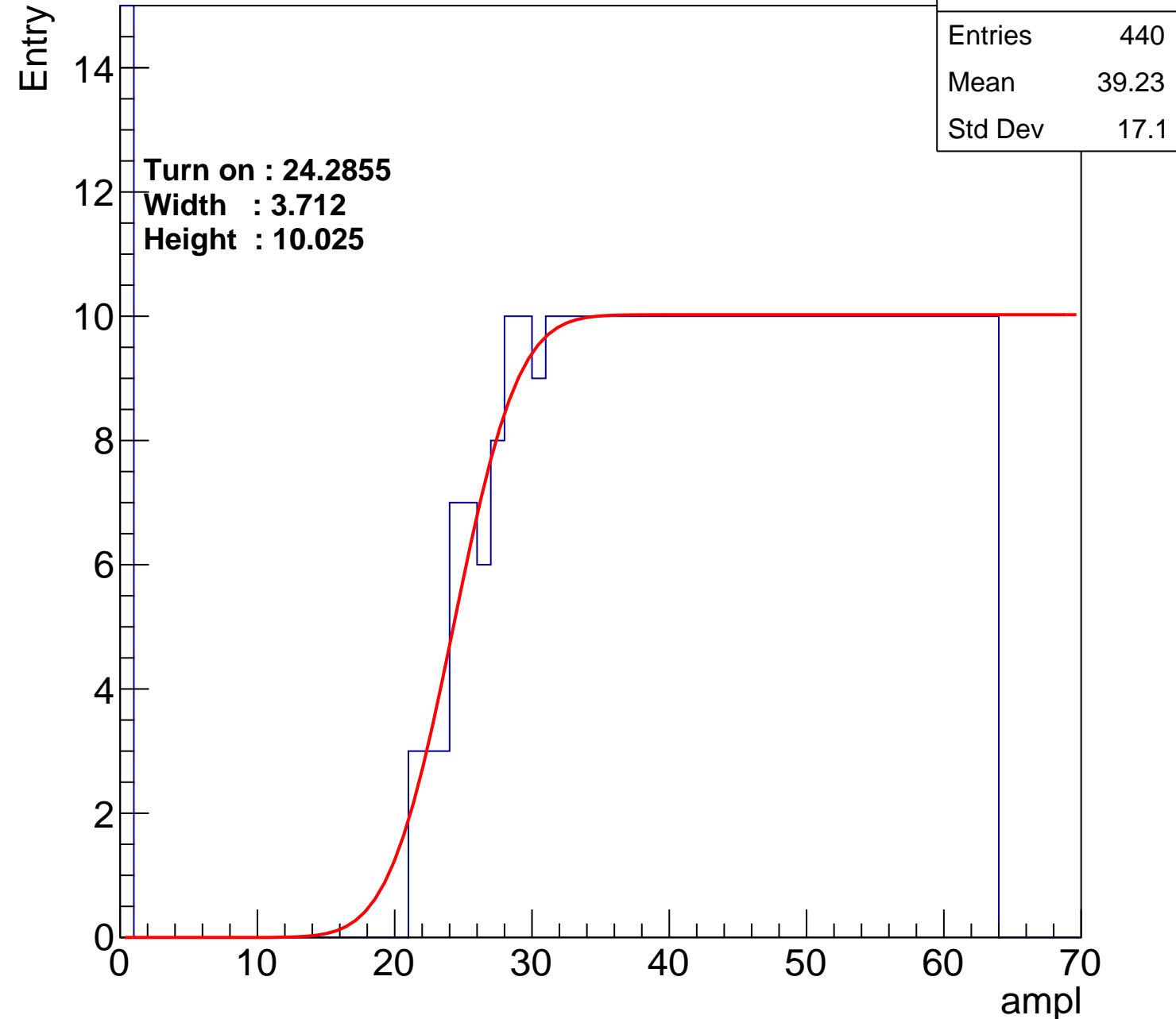
Width : 3.712

Height : 10.025

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U25-ch49

calib_packv5_041523_1651.root, FC#0, port C2

Entries	419
Mean	40.52
Std Dev	16.28

Turn on : 25.6943

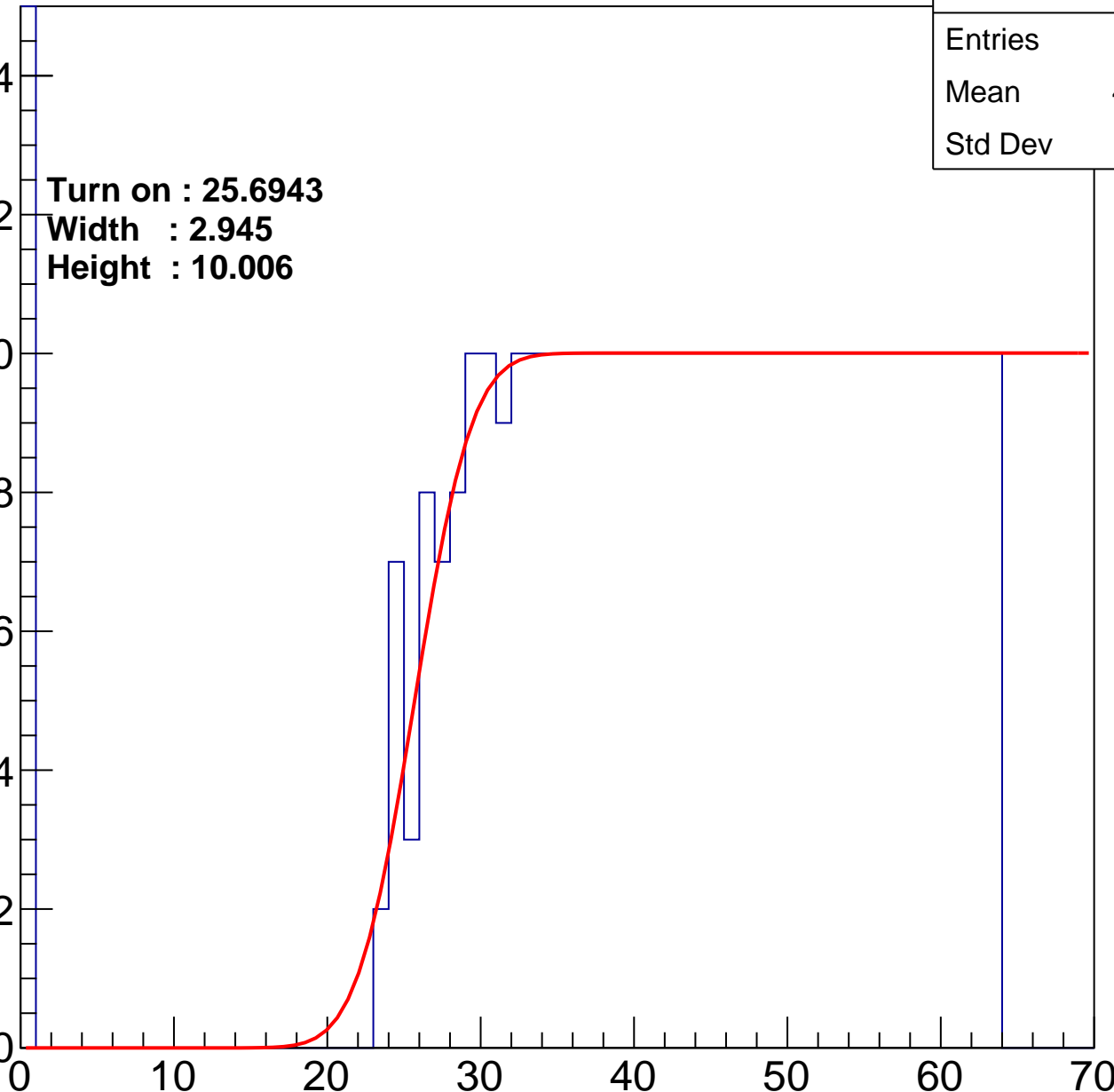
Width : 2.945

Height : 10.006

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U25-ch50

calib_packv5_041523_1651.root, FC#0, port C2

Entries	439
Mean	39.37
Std Dev	16.93

Turn on : 24.5060

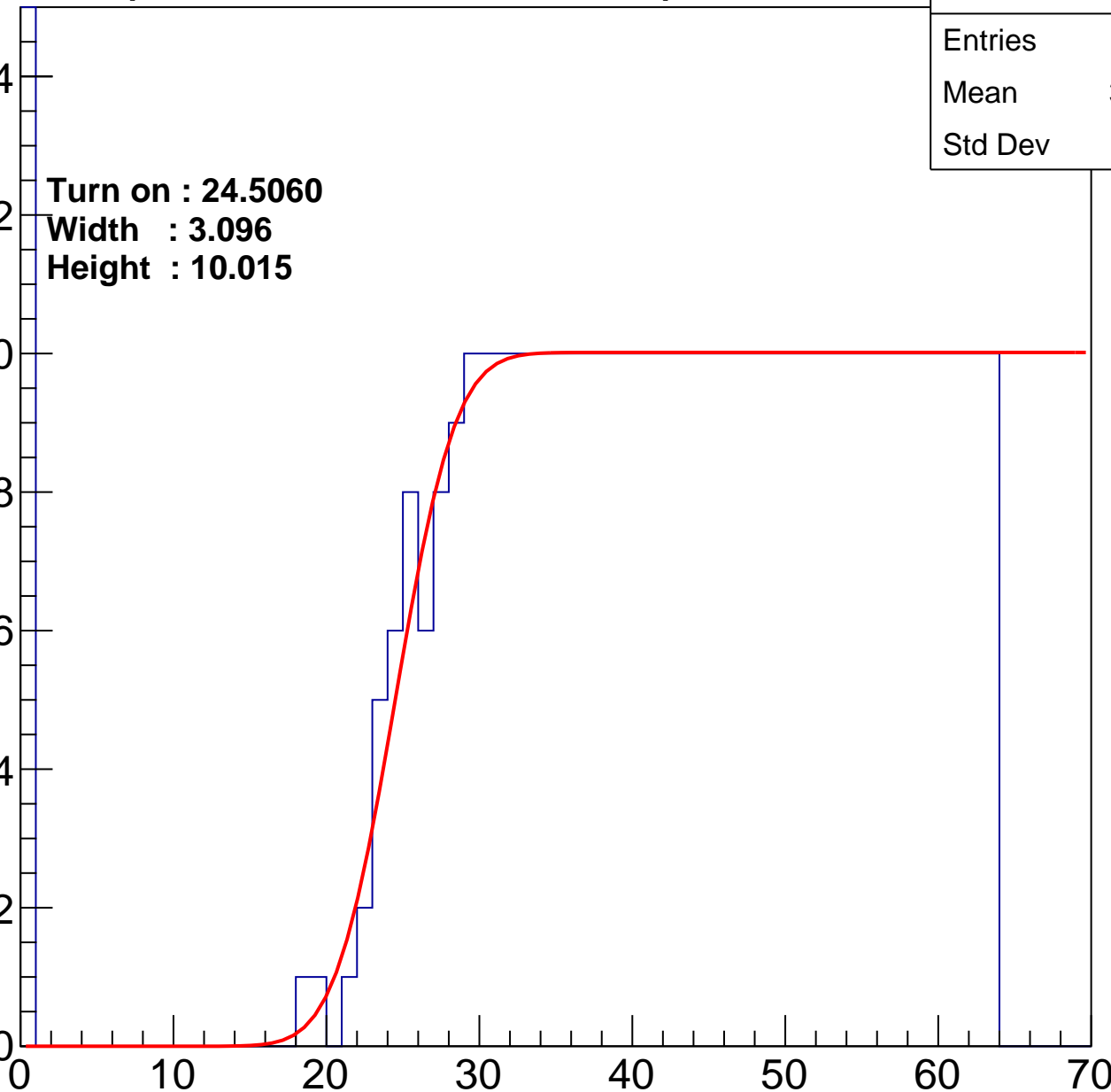
Width : 3.096

Height : 10.015

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U25-ch51

calib_packv5_041523_1651.root, FC#0, port C2

Entries	398
Mean	40.67
Std Dev	17.28

Turn on : 29.5611

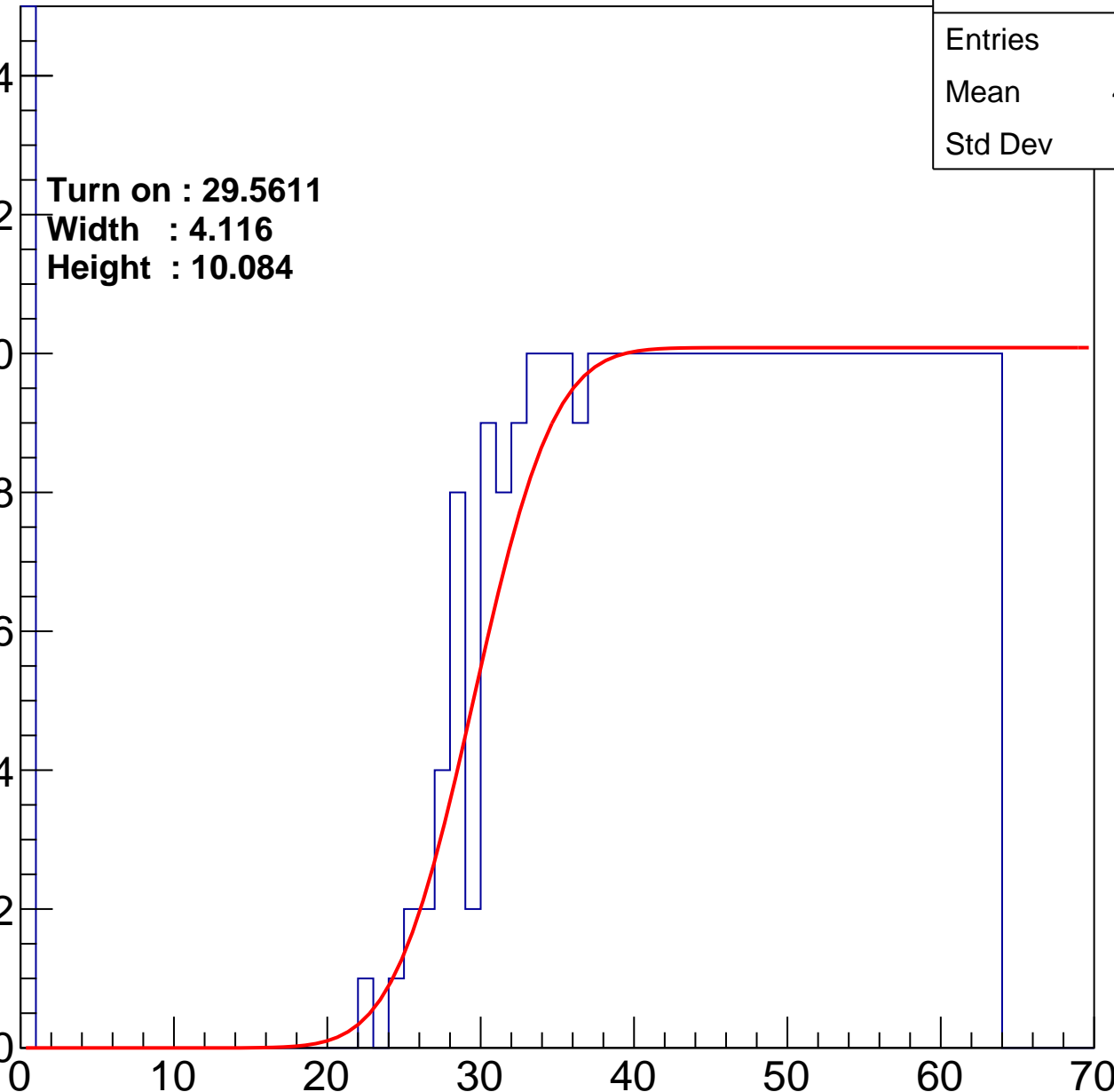
Width : 4.116

Height : 10.084

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U25-ch52

calib_packv5_041523_1651.root, FC#0, port C2

Entries	455
Mean	38.65
Std Dev	17.15

Turn on : 23.0782

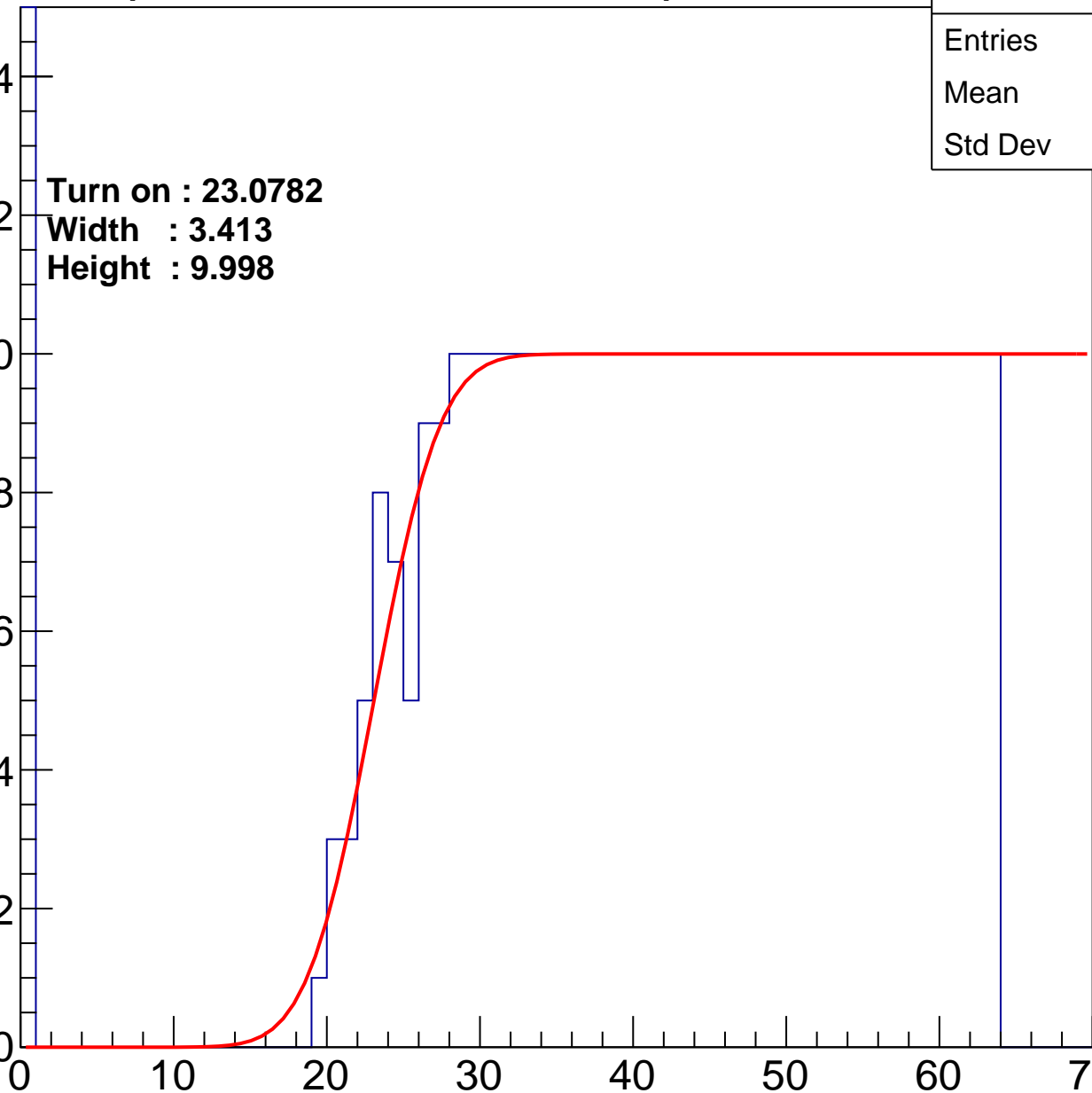
Width : 3.413

Height : 9.998

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U25-ch53

calib_packv5_041523_1651.root, FC#0, port C2

Entries	428
Mean	39.4
Std Dev	17.52

Turn on : 25.9367

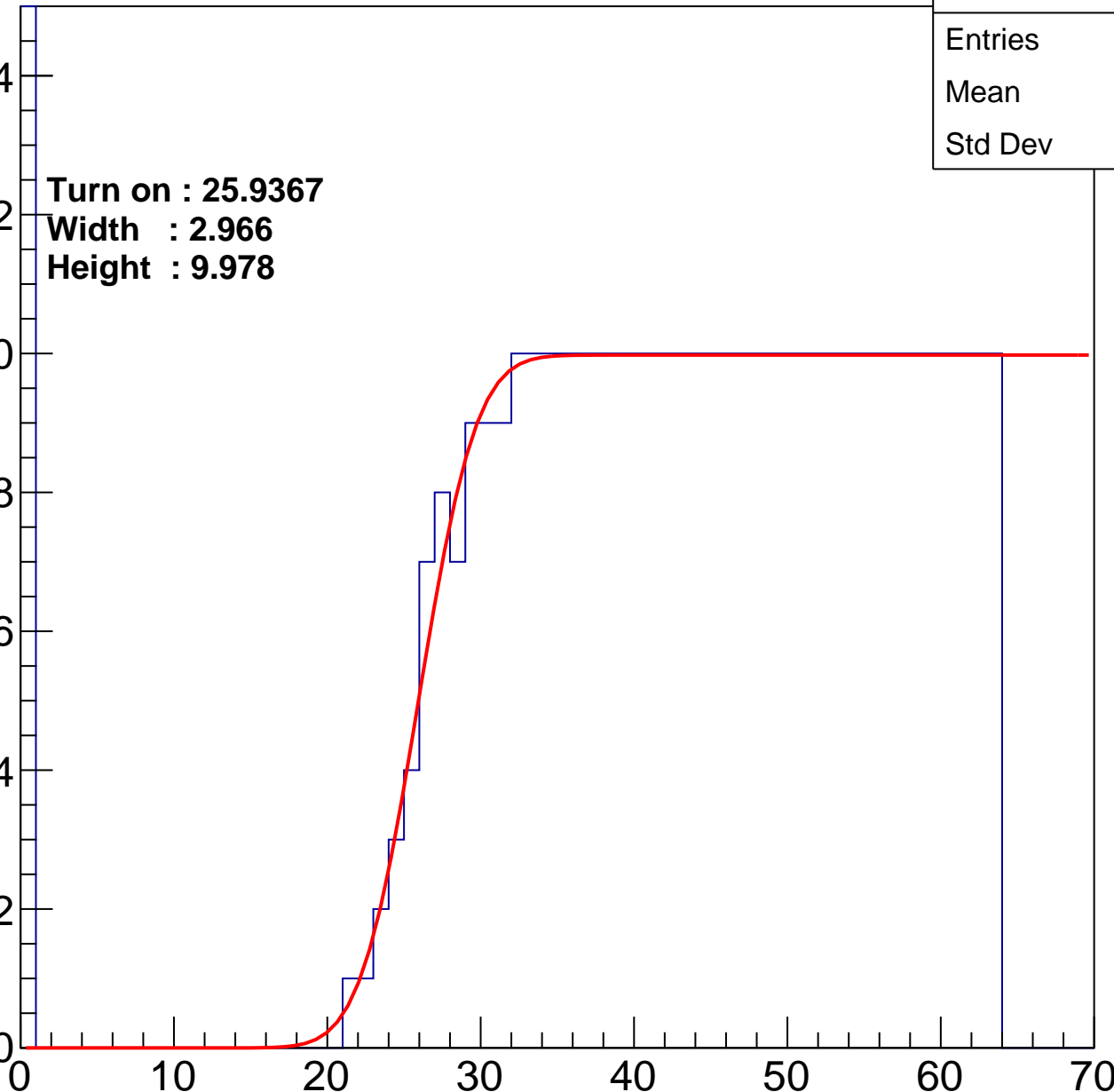
Width : 2.966

Height : 9.978

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U25-ch54

calib_packv5_041523_1651.root, FC#0, port C2

Entries	440
Mean	38.87
Std Dev	17.64

Turn on : 25.2409

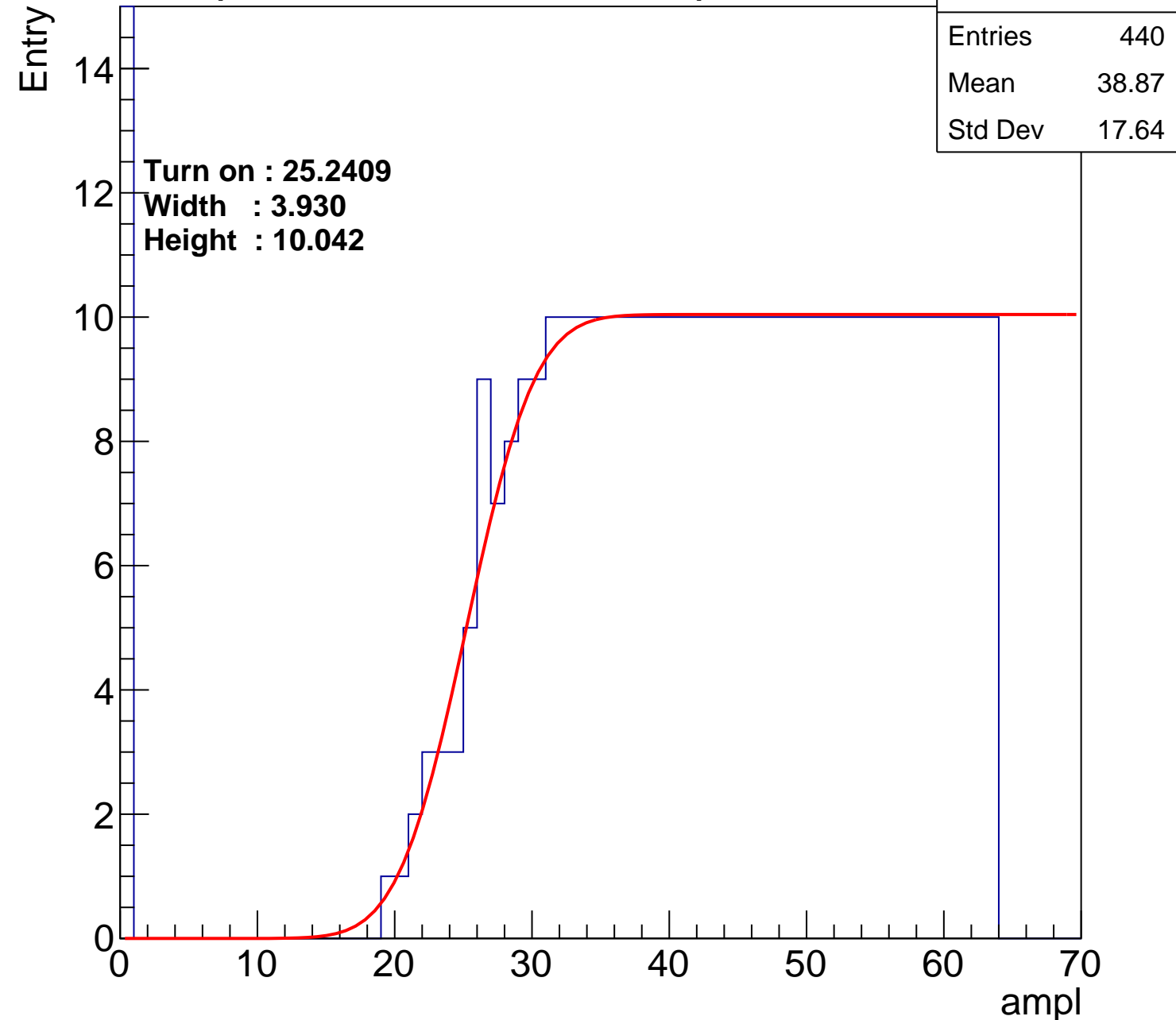
Width : 3.930

Height : 10.042

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U25-ch55

calib_packv5_041523_1651.root, FC#0, port C2

Entries	413
Mean	40.71
Std Dev	16.33

Turn on : 26.6090

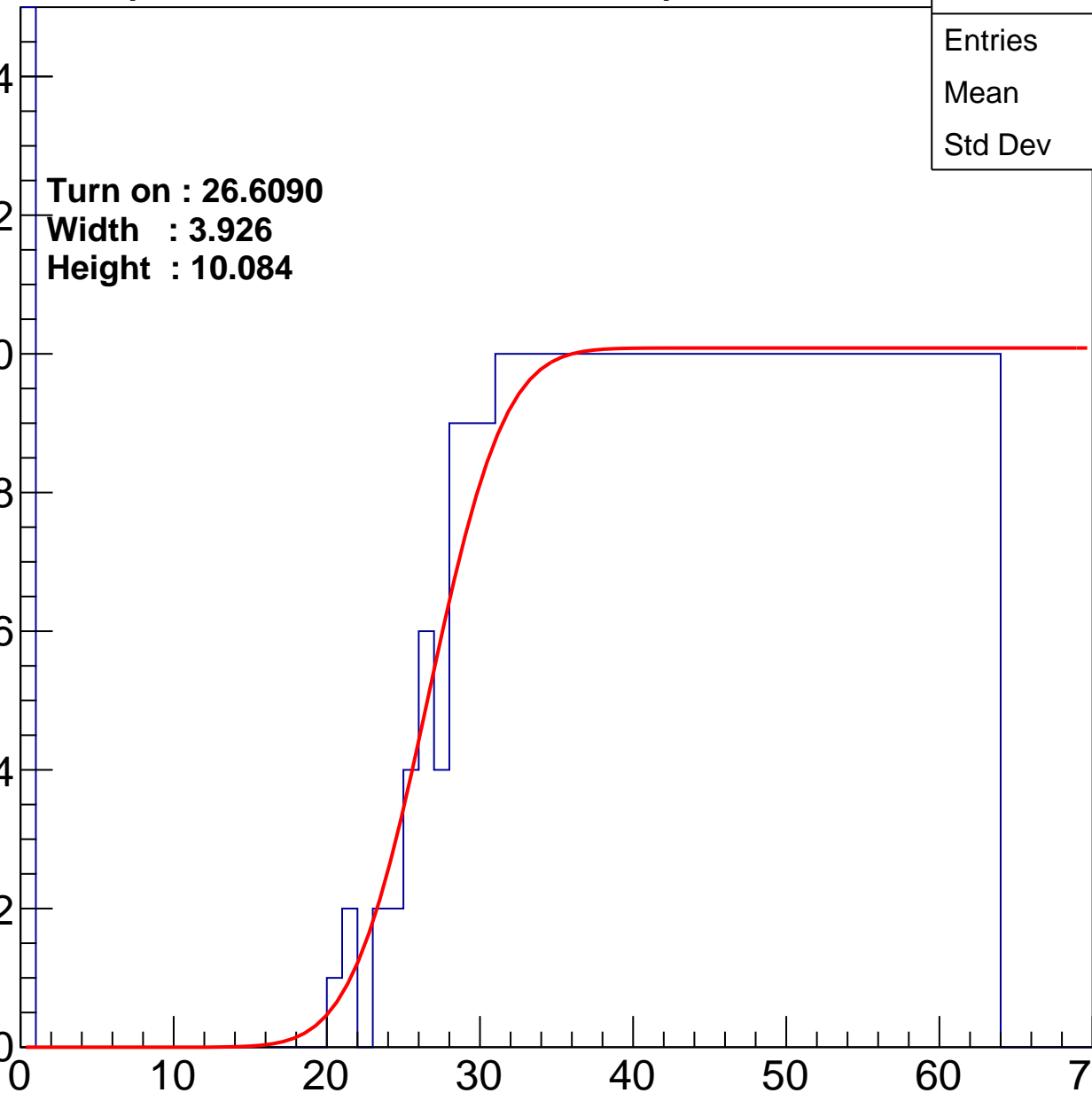
Width : 3.926

Height : 10.084

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U25-ch56

calib_packv5_041523_1651.root, FC#0, port C2

Entries	439
Mean	38.9
Std Dev	17.68

Turn on : 25.6331

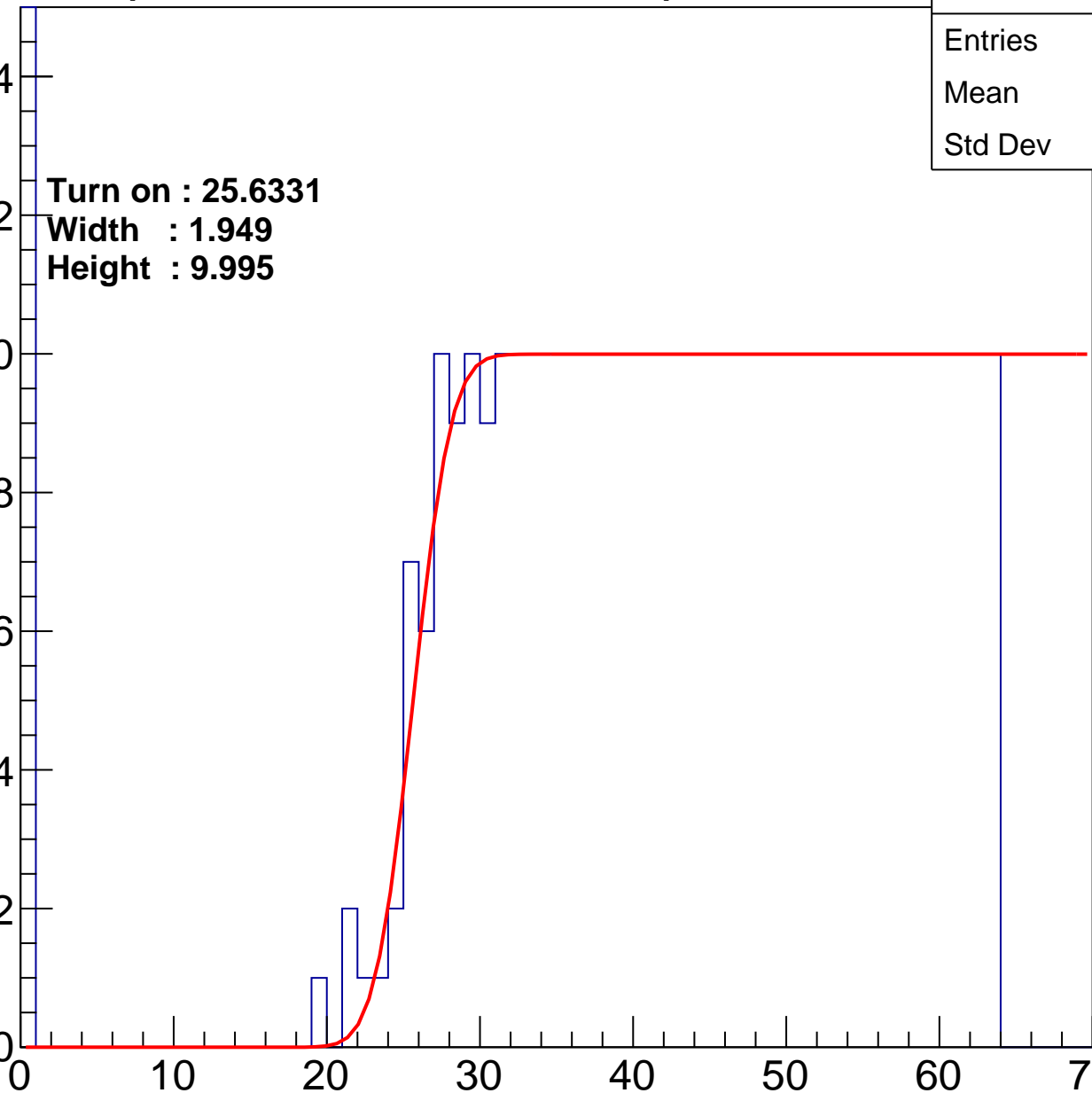
Width : 1.949

Height : 9.995

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U25-ch57

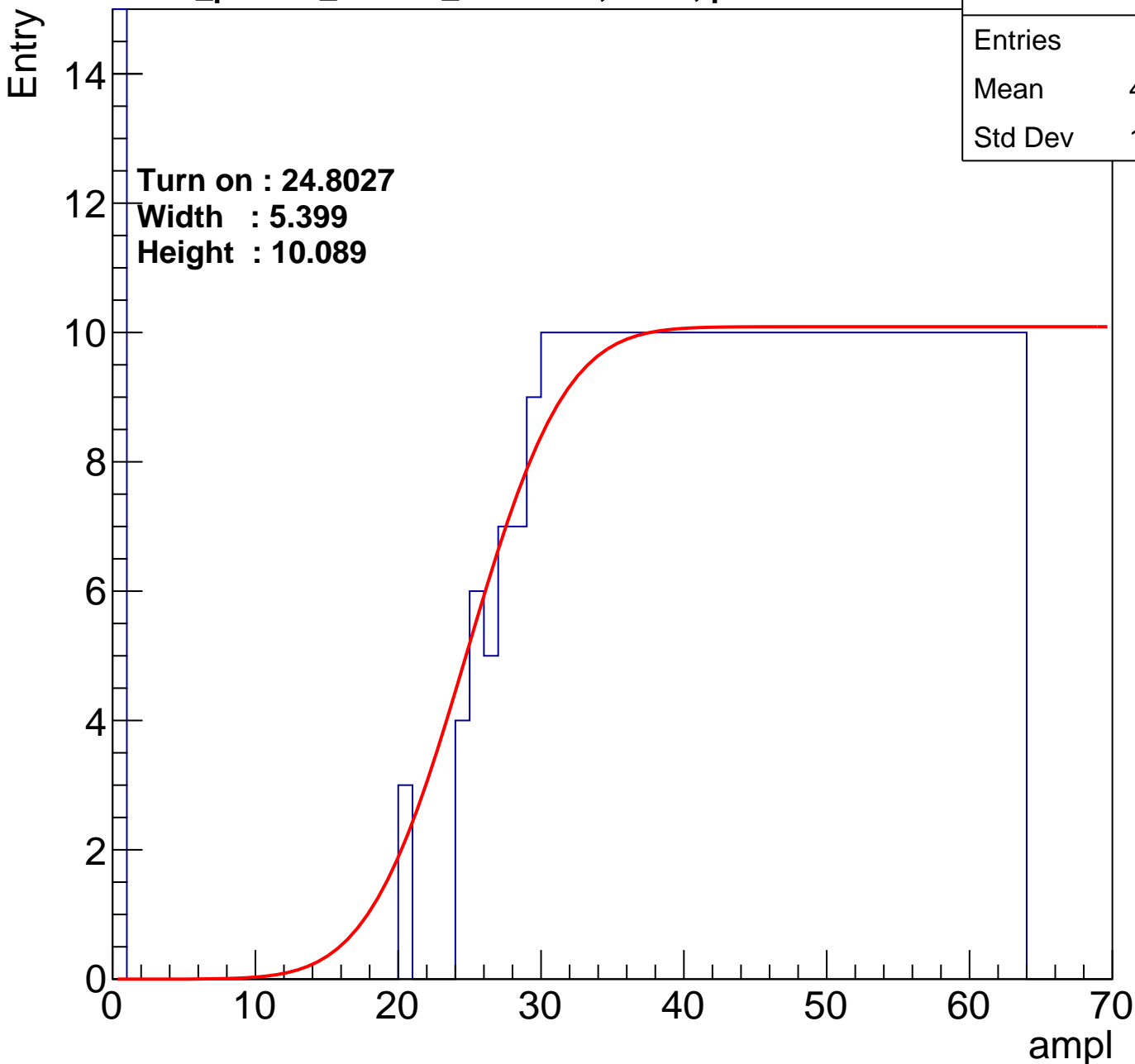
calib_packv5_041523_1651.root, FC#0, port C2

Entries	419
Mean	40.32
Std Dev	16.62

Turn on : 24.8027

Width : 5.399

Height : 10.089



B1L103S, U25-ch58

calib_packv5_041523_1651.root, FC#0, port C2

Entries	482
Mean	36.76
Std Dev	18.51

Turn on : 22.5100

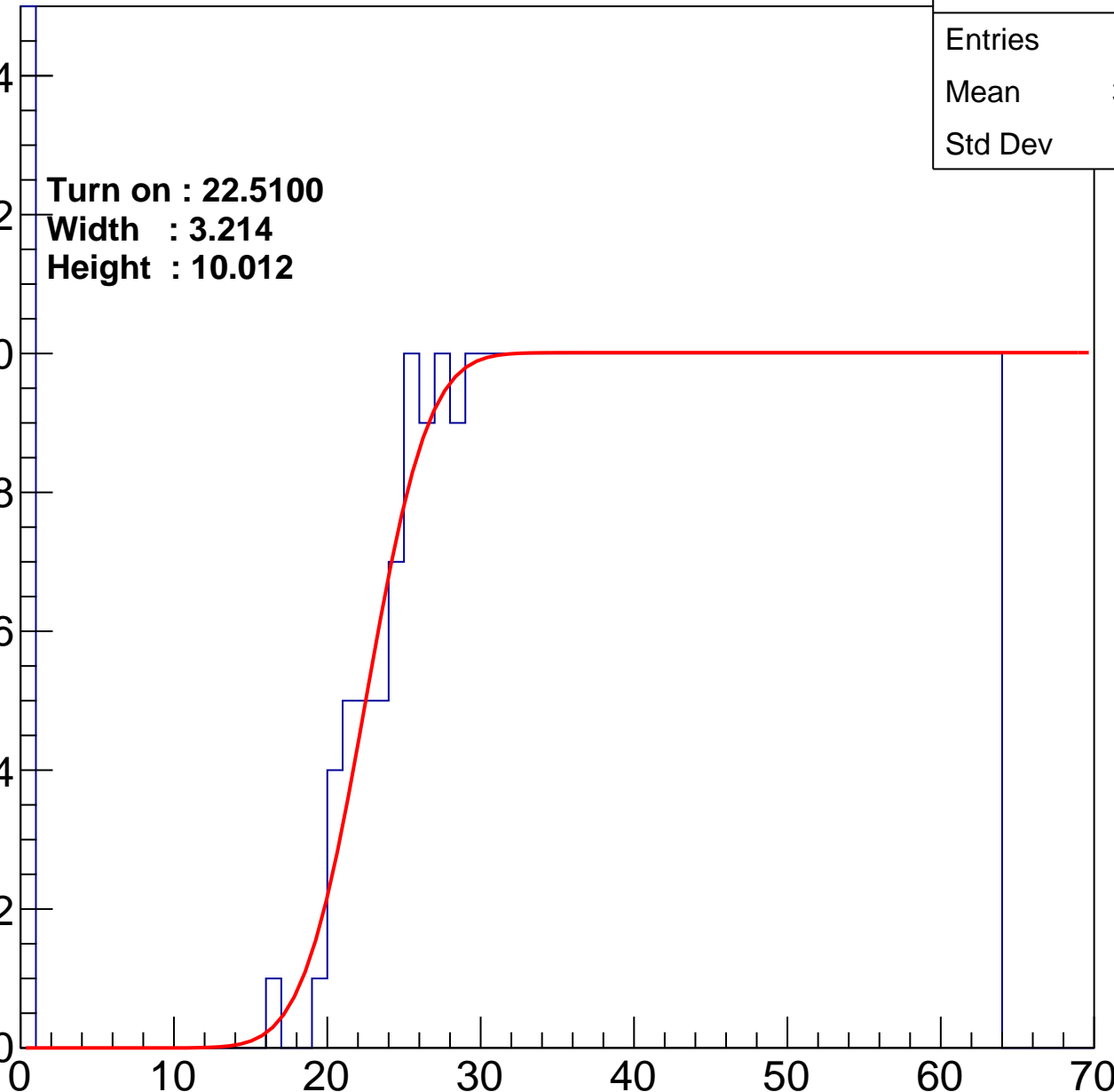
Width : 3.214

Height : 10.012

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U25-ch59

calib_packv5_041523_1651.root, FC#0, port C2

Entries	424
Mean	39.44
Std Dev	17.66

Turn on : 26.7015

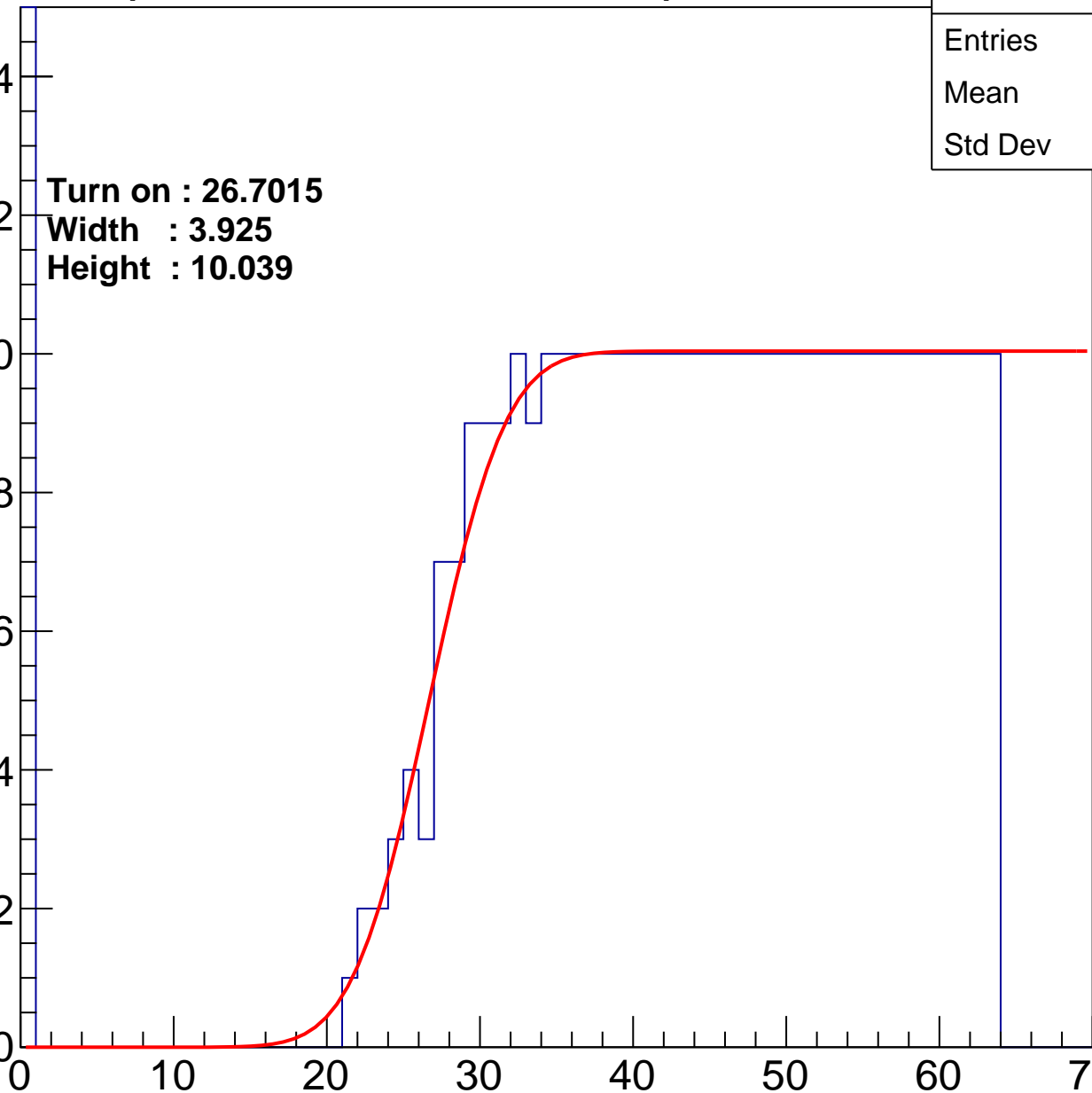
Width : 3.925

Height : 10.039

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U25-ch60

calib_packv5_041523_1651.root, FC#0, port C2

Entries	448
Mean	38.84
Std Dev	17.25

Turn on : 23.6392

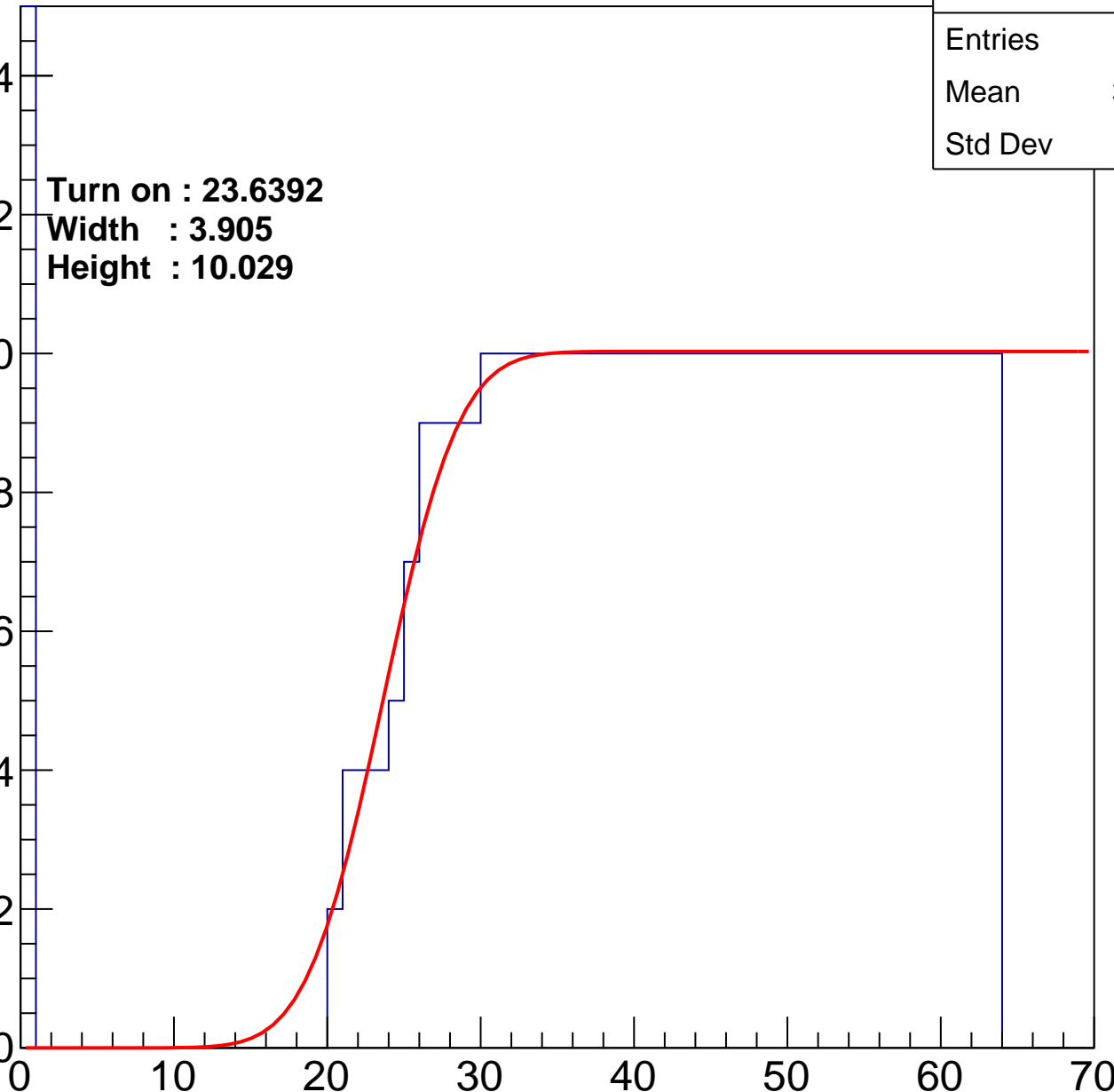
Width : 3.905

Height : 10.029

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U25-ch61

calib_packv5_041523_1651.root, FC#0, port C2

Entries	416
Mean	40.09
Std Dev	17.19

Turn on : 27.2022

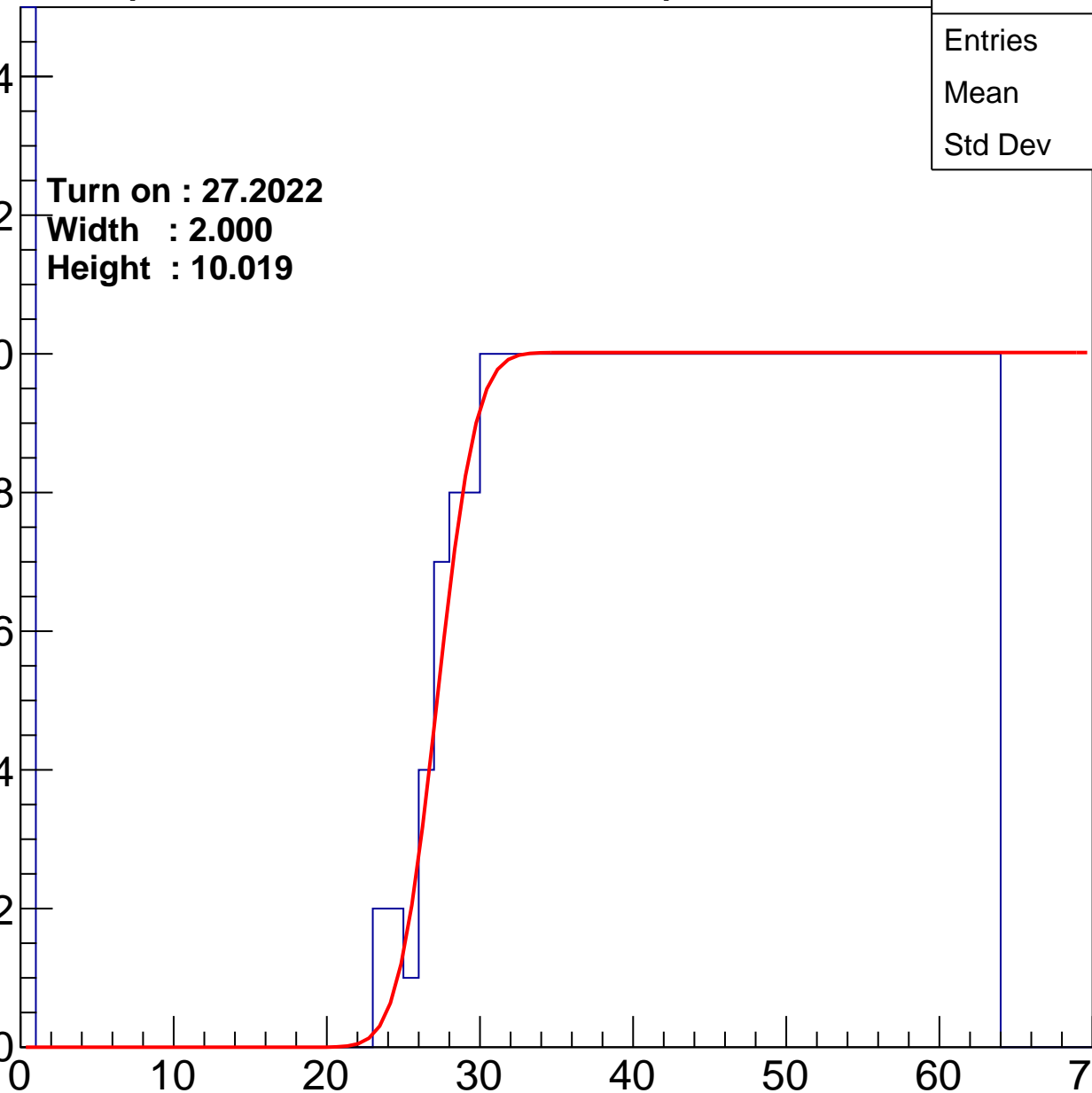
Width : 2.000

Height : 10.019

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U25-ch62

calib_packv5_041523_1651.root, FC#0, port C2

Entries	421
Mean	40.8
Std Dev	15.66

Turn on : 25.3785

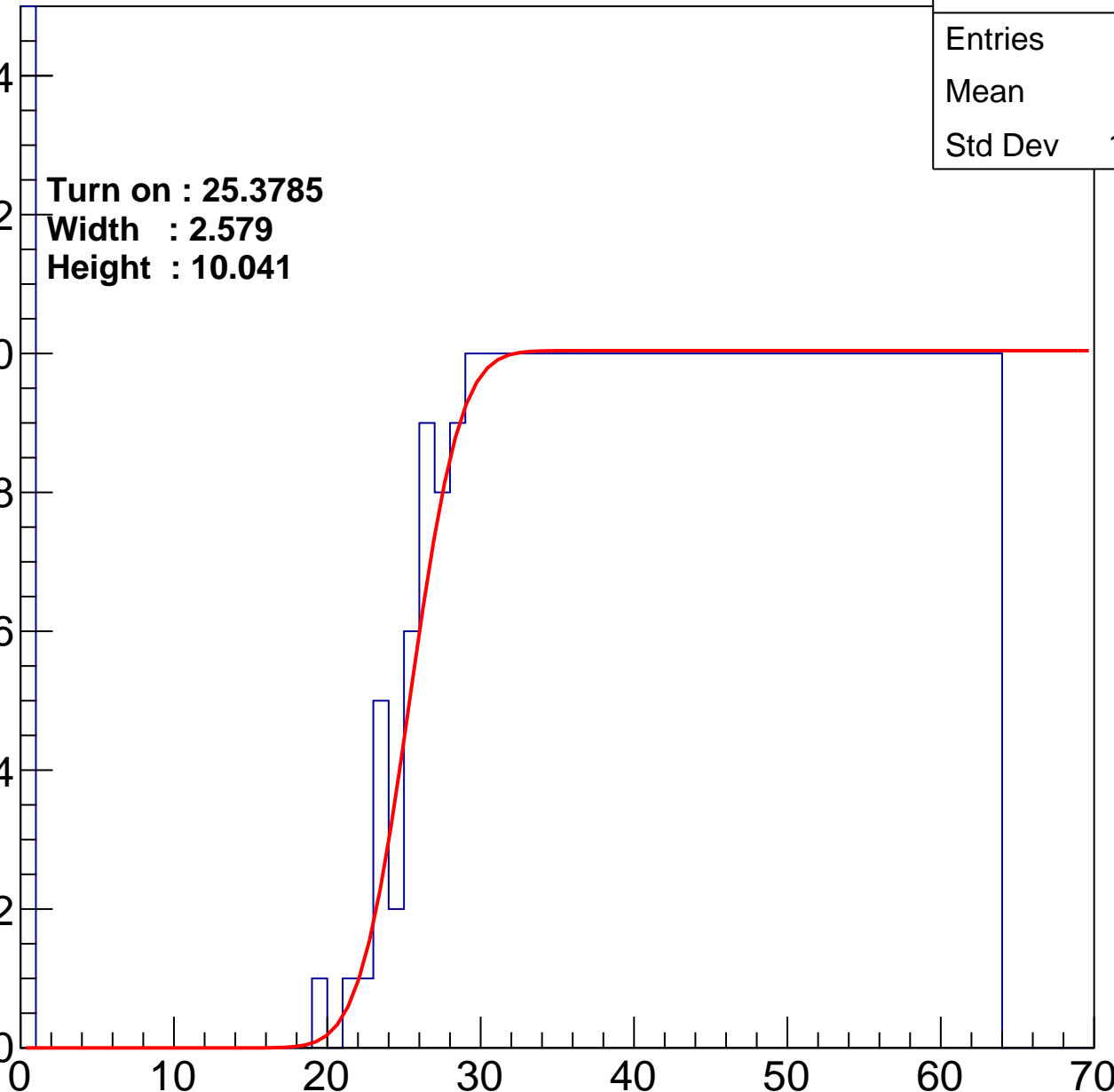
Width : 2.579

Height : 10.041

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U25-ch63

calib_packv5_041523_1651.root, FC#0, port C2

Entries	423
Mean	40.3
Std Dev	16.39

Turn on : 25.3539

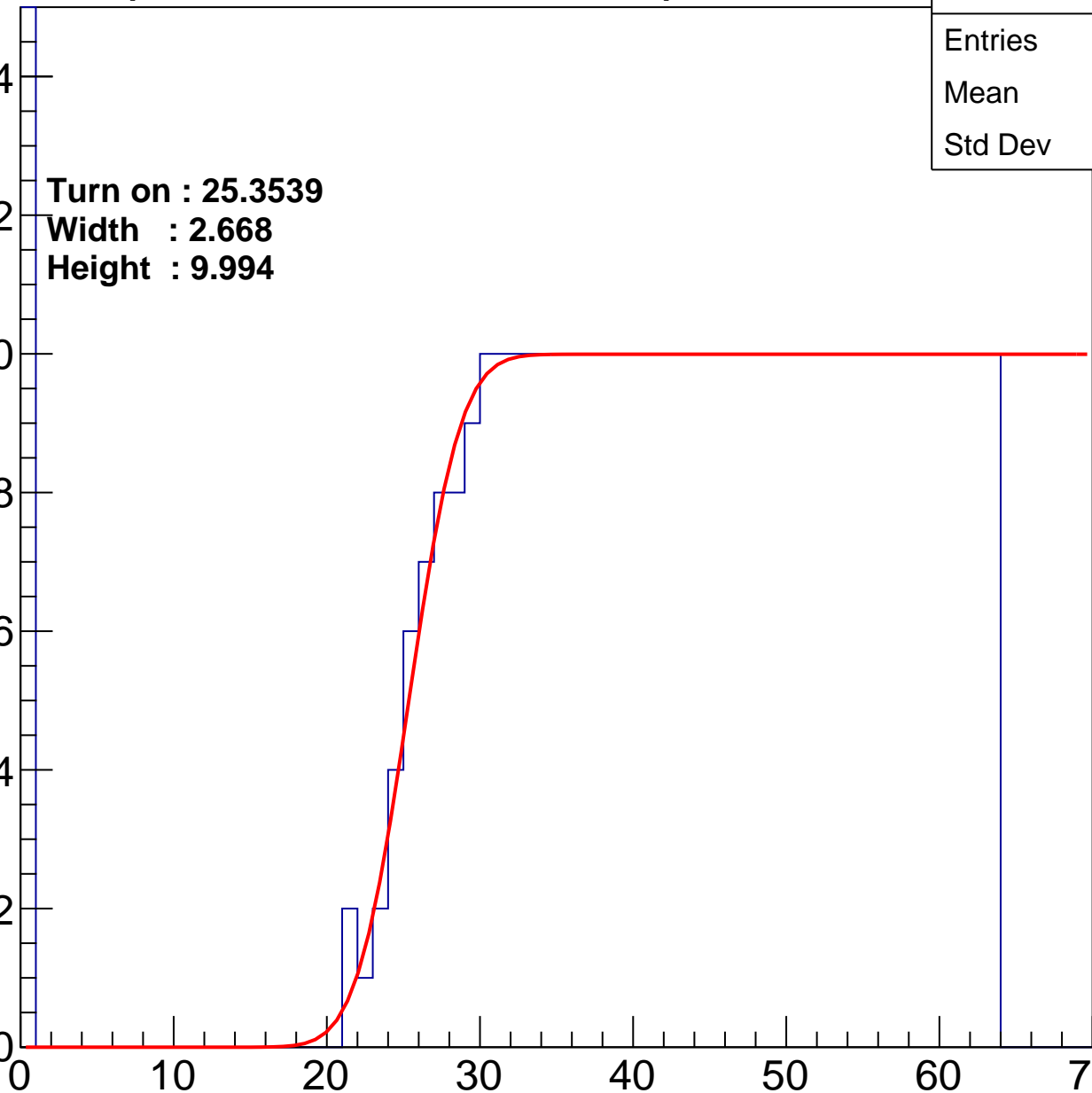
Width : 2.668

Height : 9.994

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U25-ch64

calib_packv5_041523_1651.root, FC#0, port C2

Entries	460
Mean	37.68
Std Dev	18.32

Turn on : 23.6168

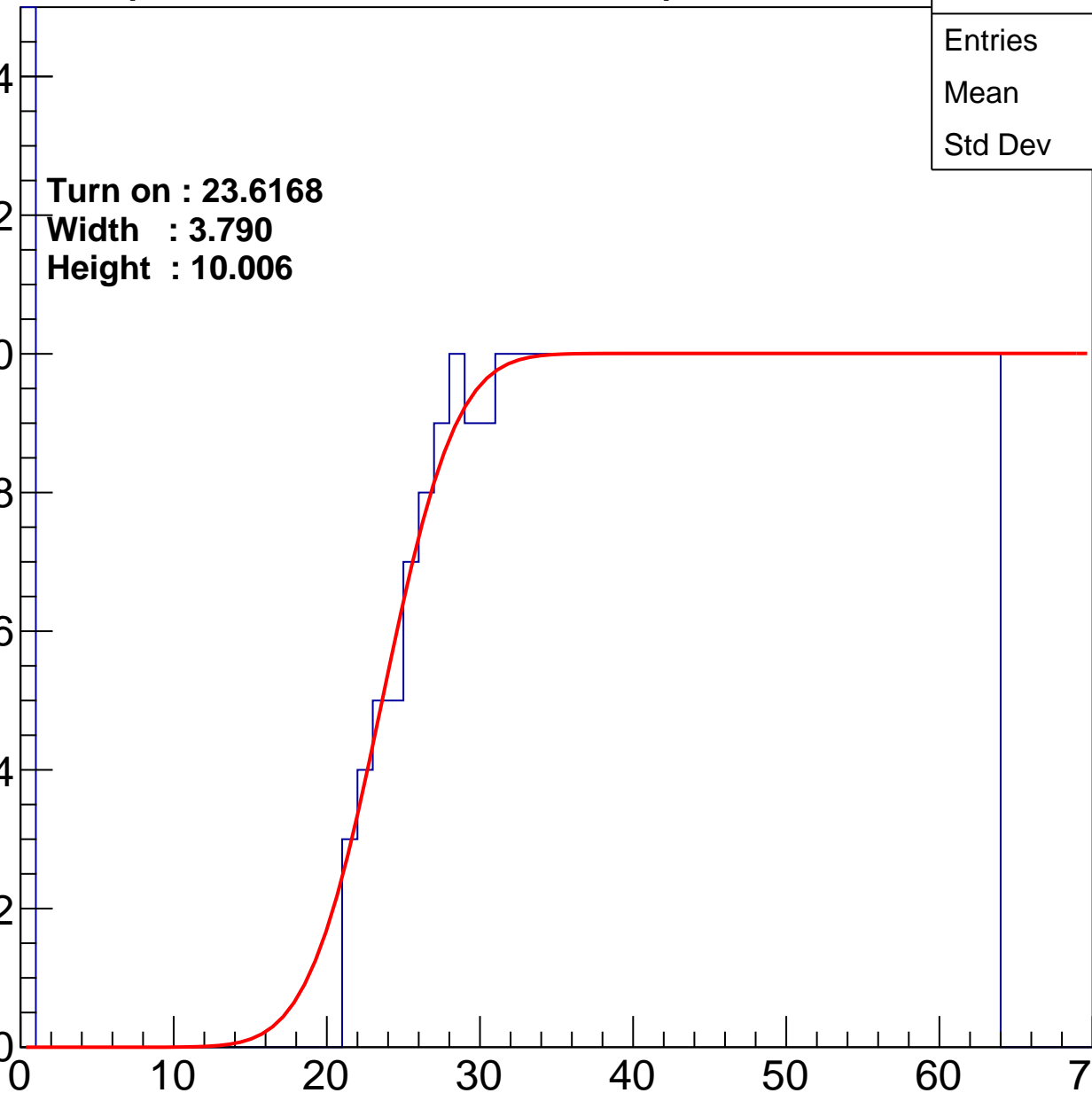
Width : 3.790

Height : 10.006

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U25-ch65

calib_packv5_041523_1651.root, FC#0, port C2

Entries	419
Mean	39.35
Std Dev	18.07

Turn on : 27.6355

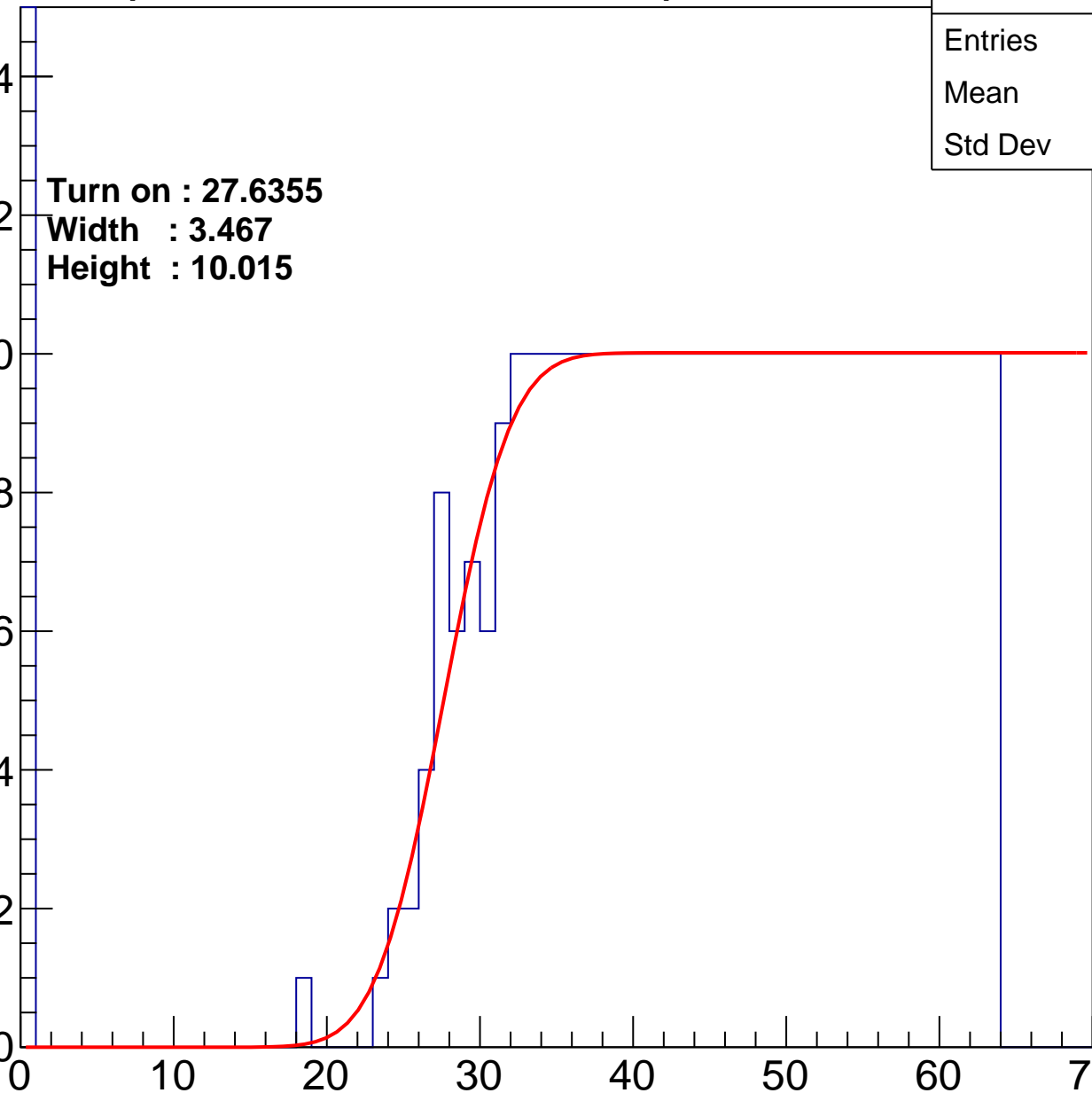
Width : 3.467

Height : 10.015

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U25-ch66

calib_packv5_041523_1651.root, FC#0, port C2

Entries	441
Mean	39.29
Std Dev	16.9

Turn on : 24.0225

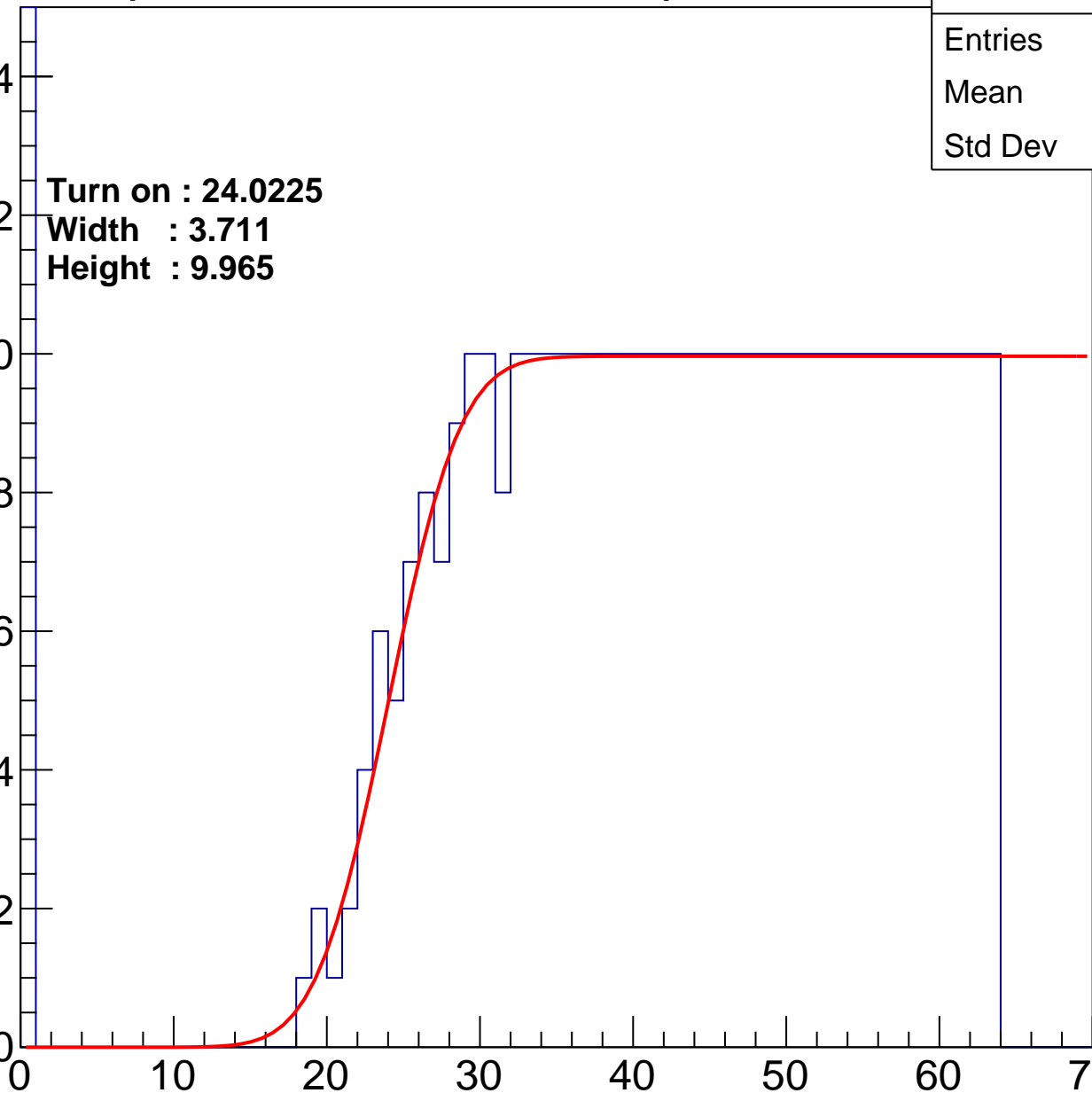
Width : 3.711

Height : 9.965

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U25-ch67

calib_packv5_041523_1651.root, FC#0, port C2

Entries	398
Mean	41.76
Std Dev	15.51

Turn on : 27.5641

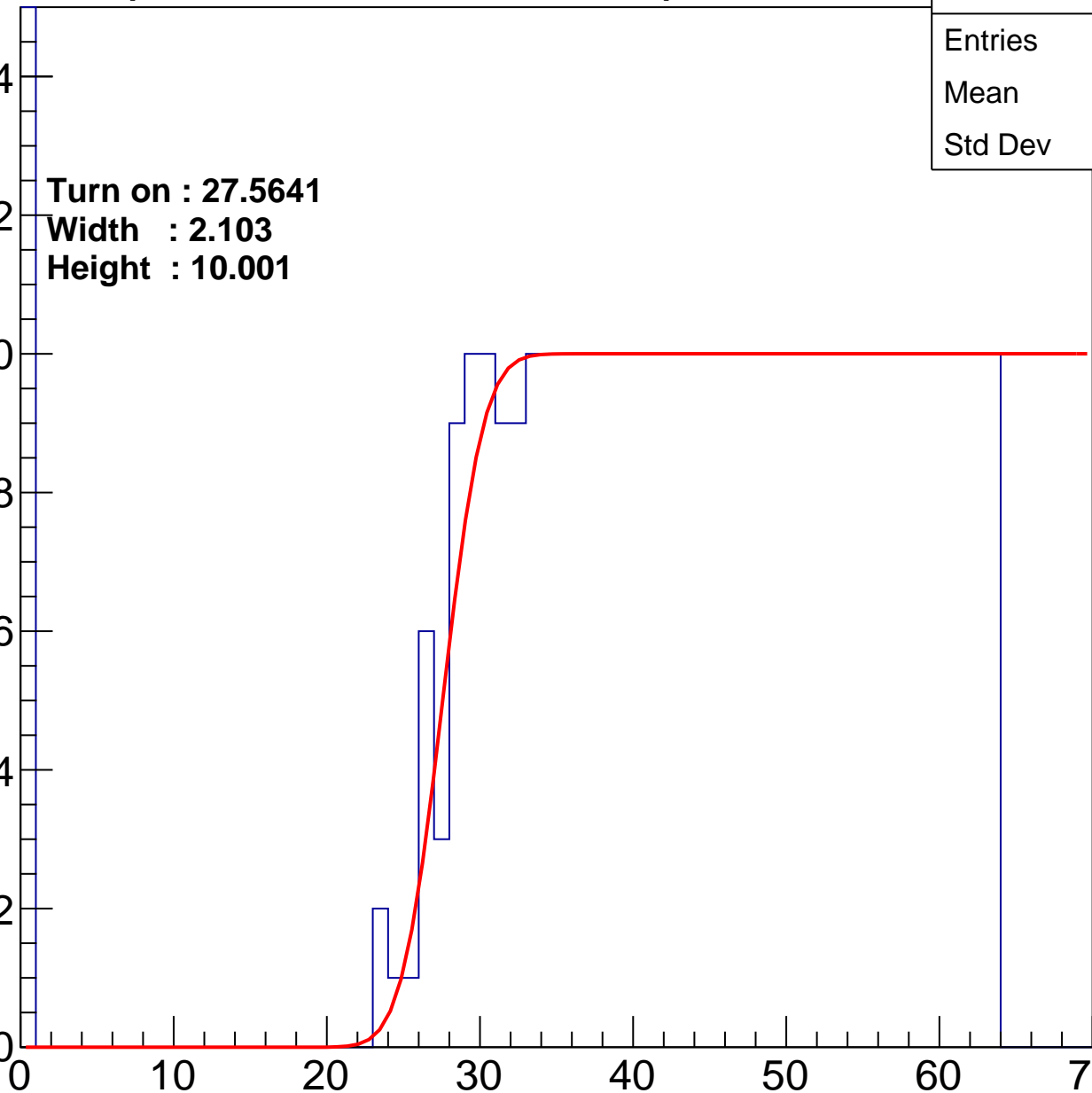
Width : 2.103

Height : 10.001

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U25-ch68

calib_packv5_041523_1651.root, FC#0, port C2

Entries	460
Mean	37.92
Std Dev	17.97

Turn on : 23.5247

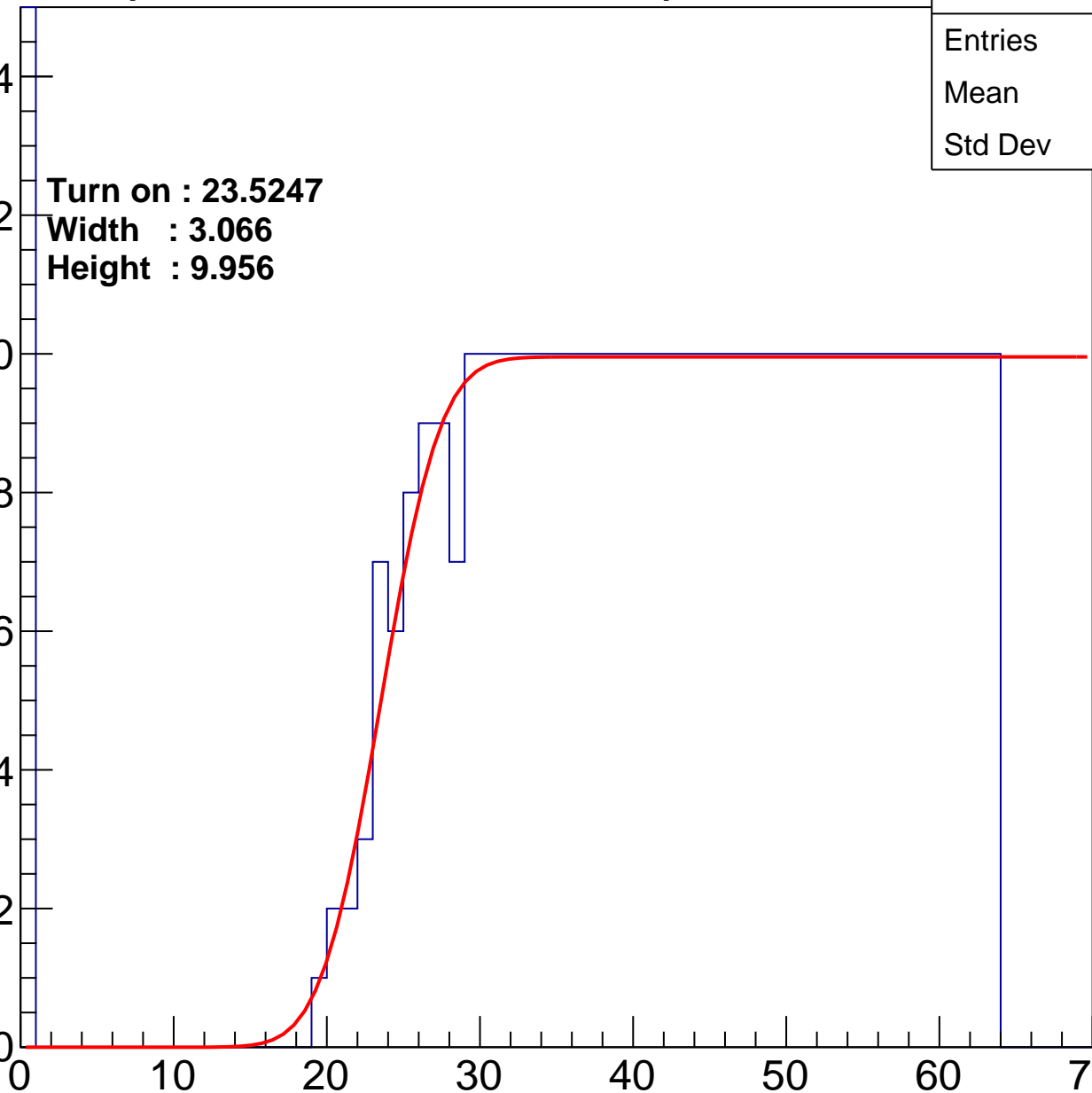
Width : 3.066

Height : 9.956

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U25-ch69

calib_packv5_041523_1651.root, FC#0, port C2

Entries	429
Mean	39.75
Std Dev	16.95

Turn on : 26.0108

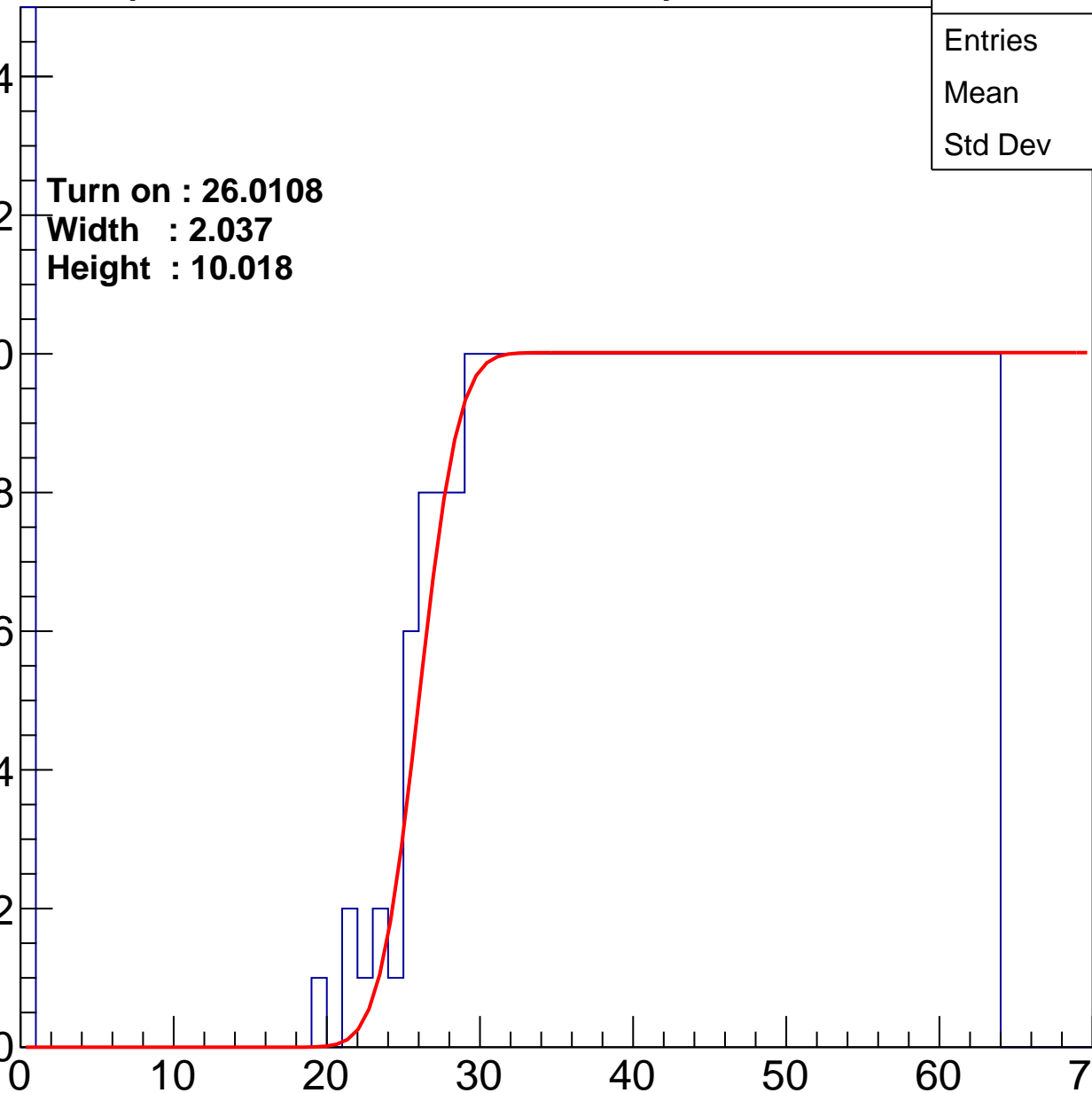
Width : 2.037

Height : 10.018

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U25-ch70

calib_packv5_041523_1651.root, FC#0, port C2

Entries	445
Mean	39.13
Std Dev	16.95

Turn on : 23.8973

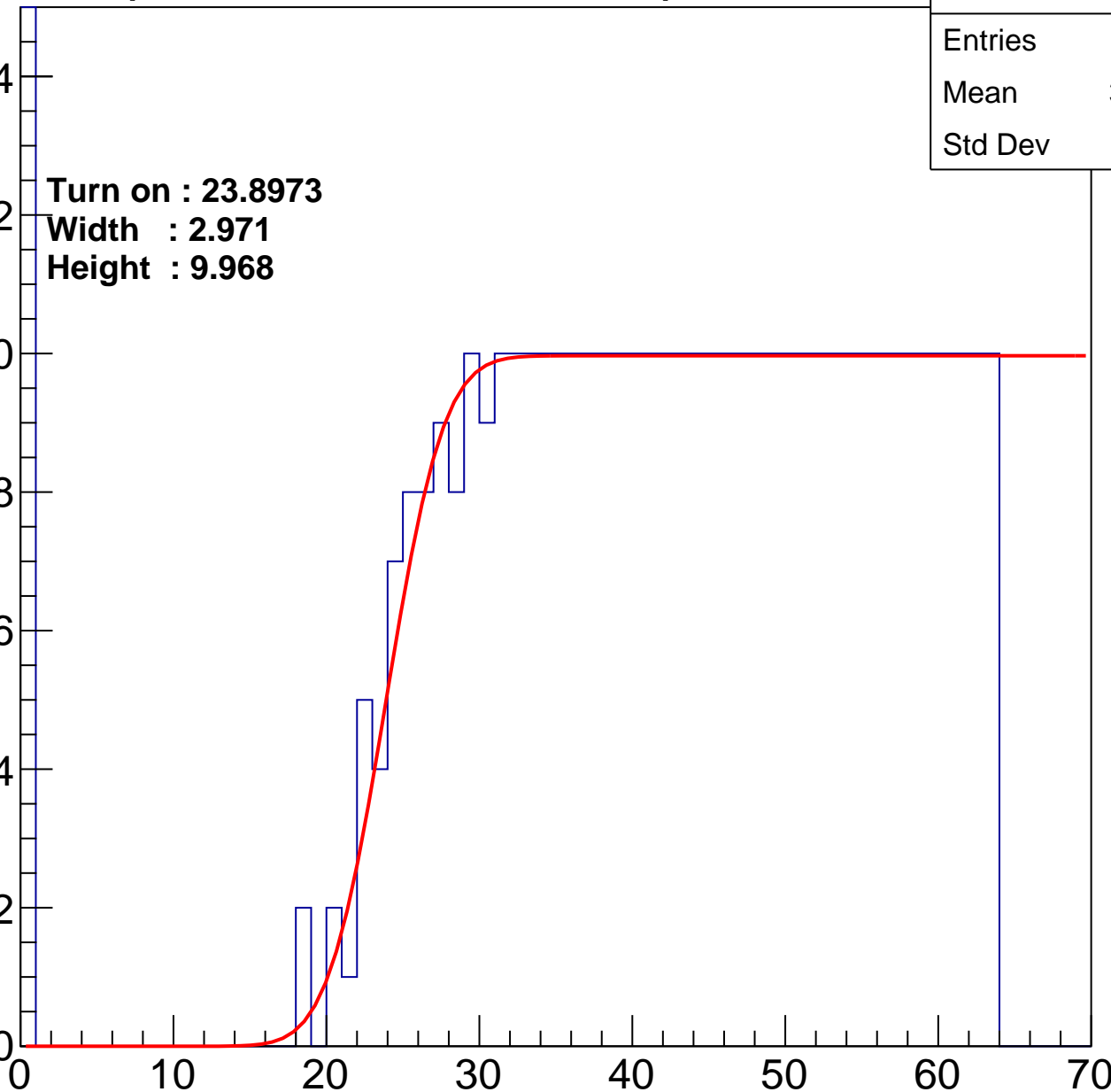
Width : 2.971

Height : 9.968

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U25-ch71

calib_packv5_041523_1651.root, FC#0, port C2

Entries	432
Mean	39.52
Std Dev	17.08

Turn on : 25.7337

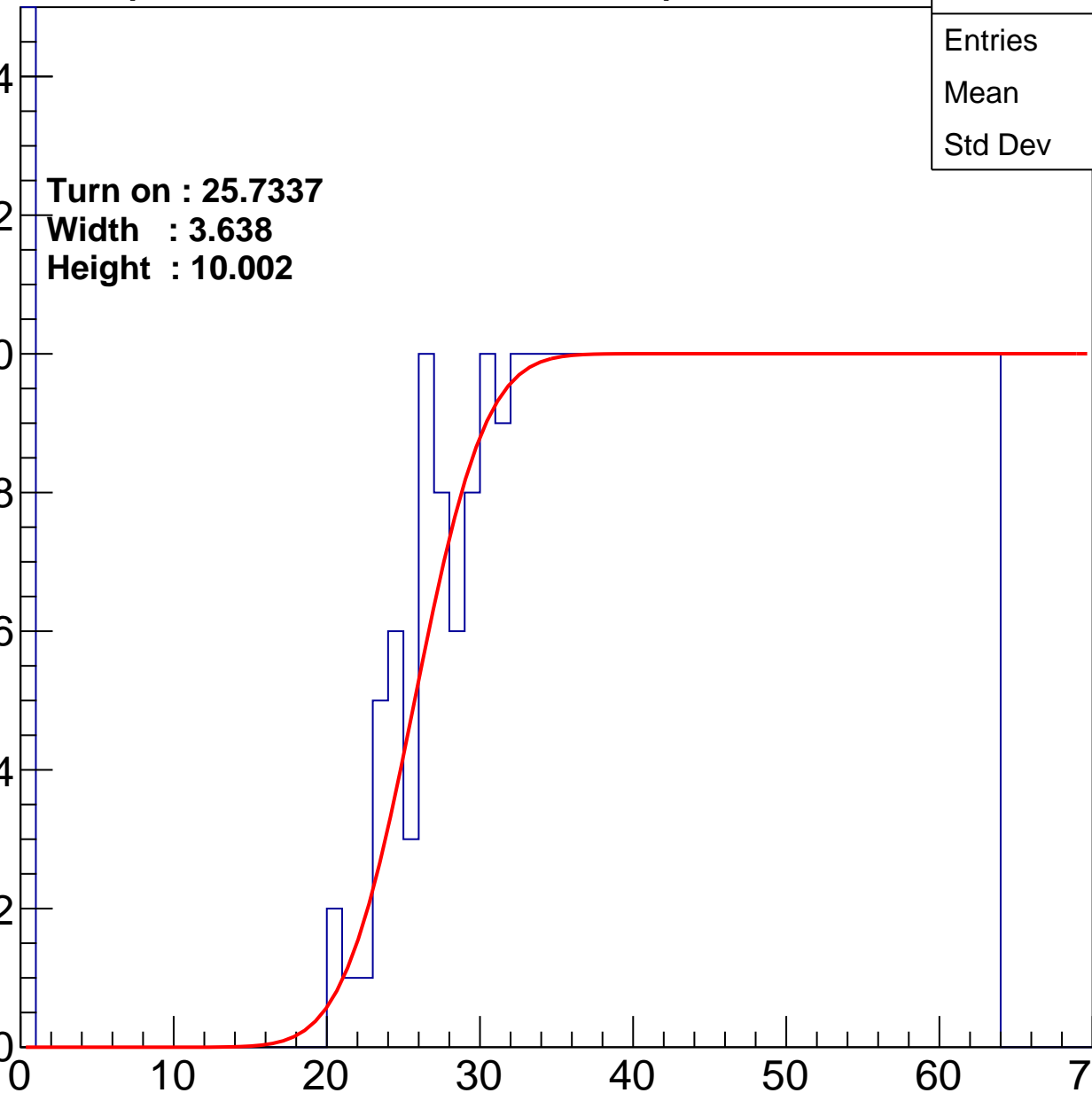
Width : 3.638

Height : 10.002

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U25-ch72

calib_packv5_041523_1651.root, FC#0, port C2

Entries	464
Mean	37.83
Std Dev	17.92

Turn on : 23.7110

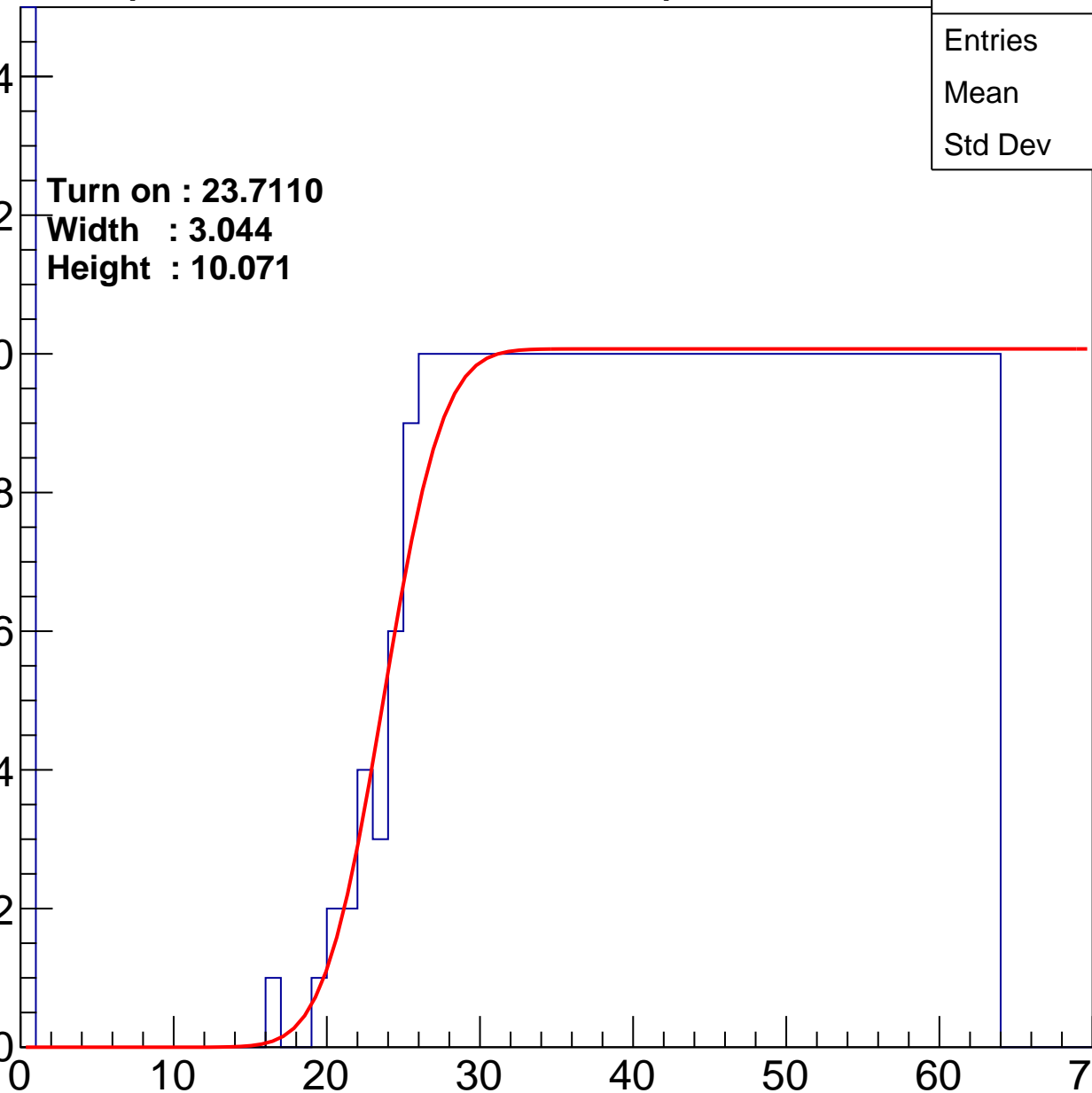
Width : 3.044

Height : 10.071

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U25-ch73

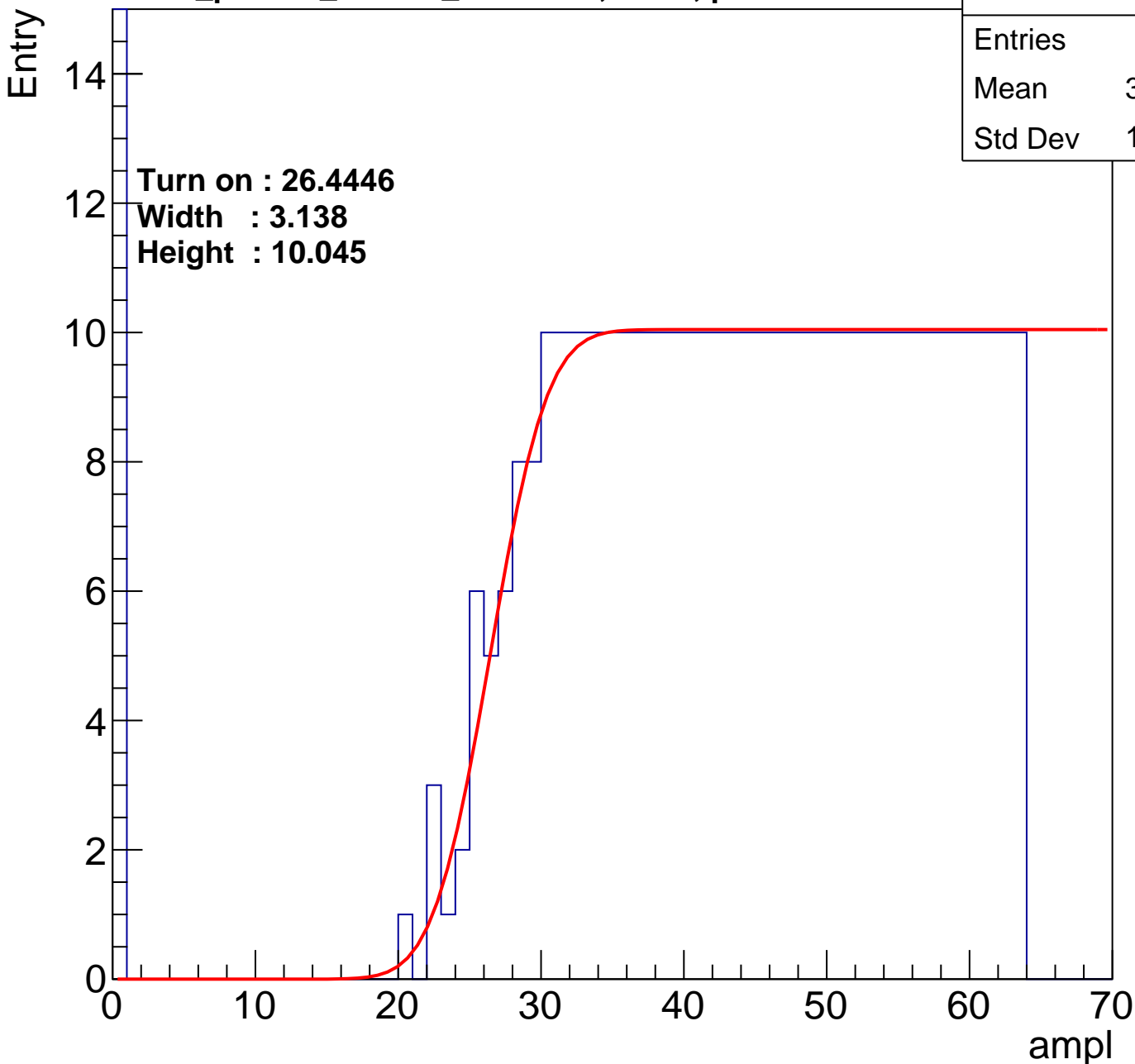
calib_packv5_041523_1651.root, FC#0, port C2

Entries	431
Mean	39.13
Std Dev	17.76

Turn on : 26.4446

Width : 3.138

Height : 10.045



B1L103S, U25-ch74

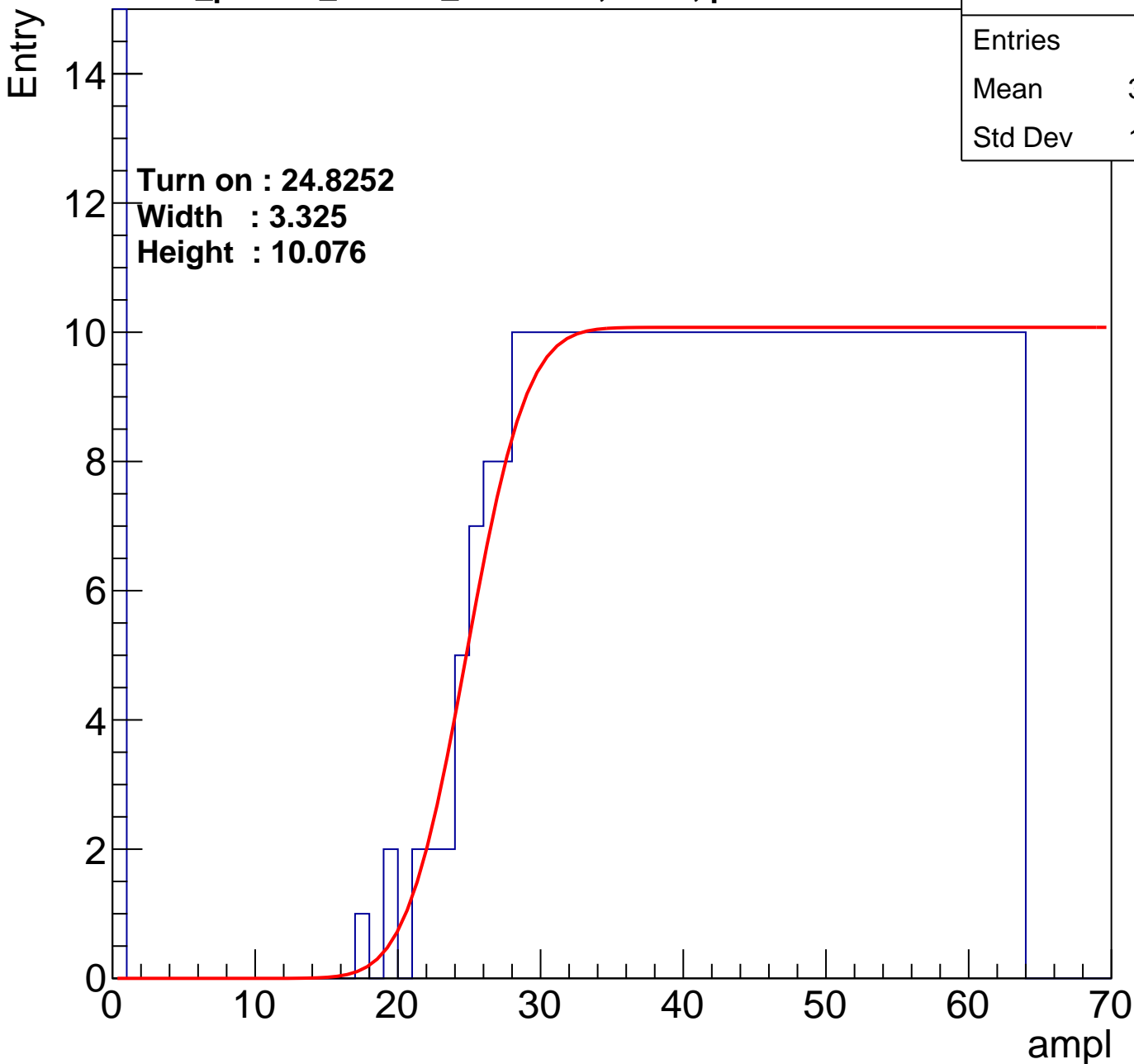
calib_packv5_041523_1651.root, FC#0, port C2

Entries	454
Mean	38.07
Std Dev	18.08

Turn on : 24.8252

Width : 3.325

Height : 10.076



B1L103S, U25-ch75

calib_packv5_041523_1651.root, FC#0, port C2

Entries	428
Mean	39.41
Std Dev	17.51

Turn on : 25.5447

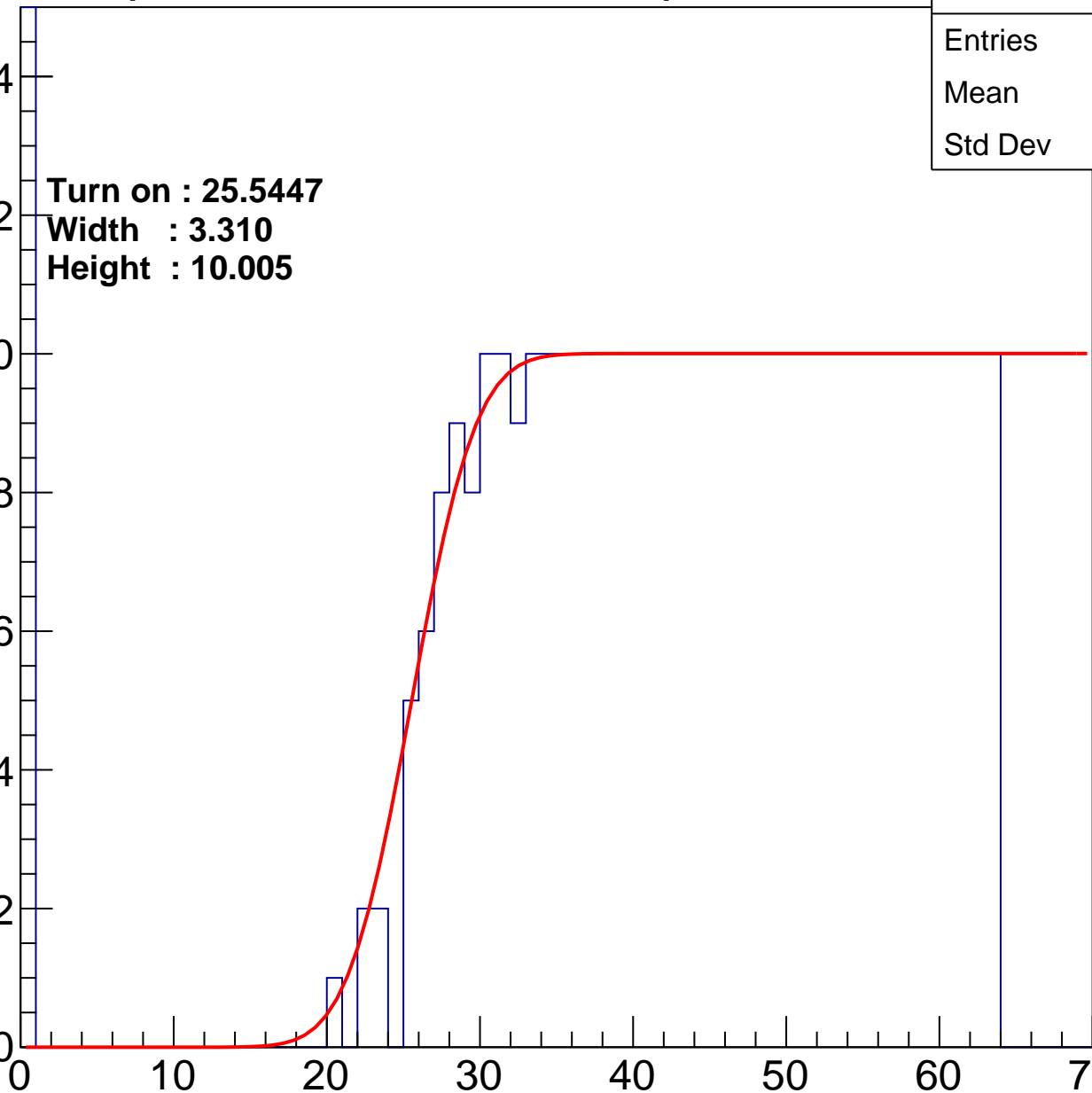
Width : 3.310

Height : 10.005

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U25-ch76

calib_packv5_041523_1651.root, FC#0, port C2

Entries	453
Mean	37.94
Std Dev	18.31

Turn on : 24.8478

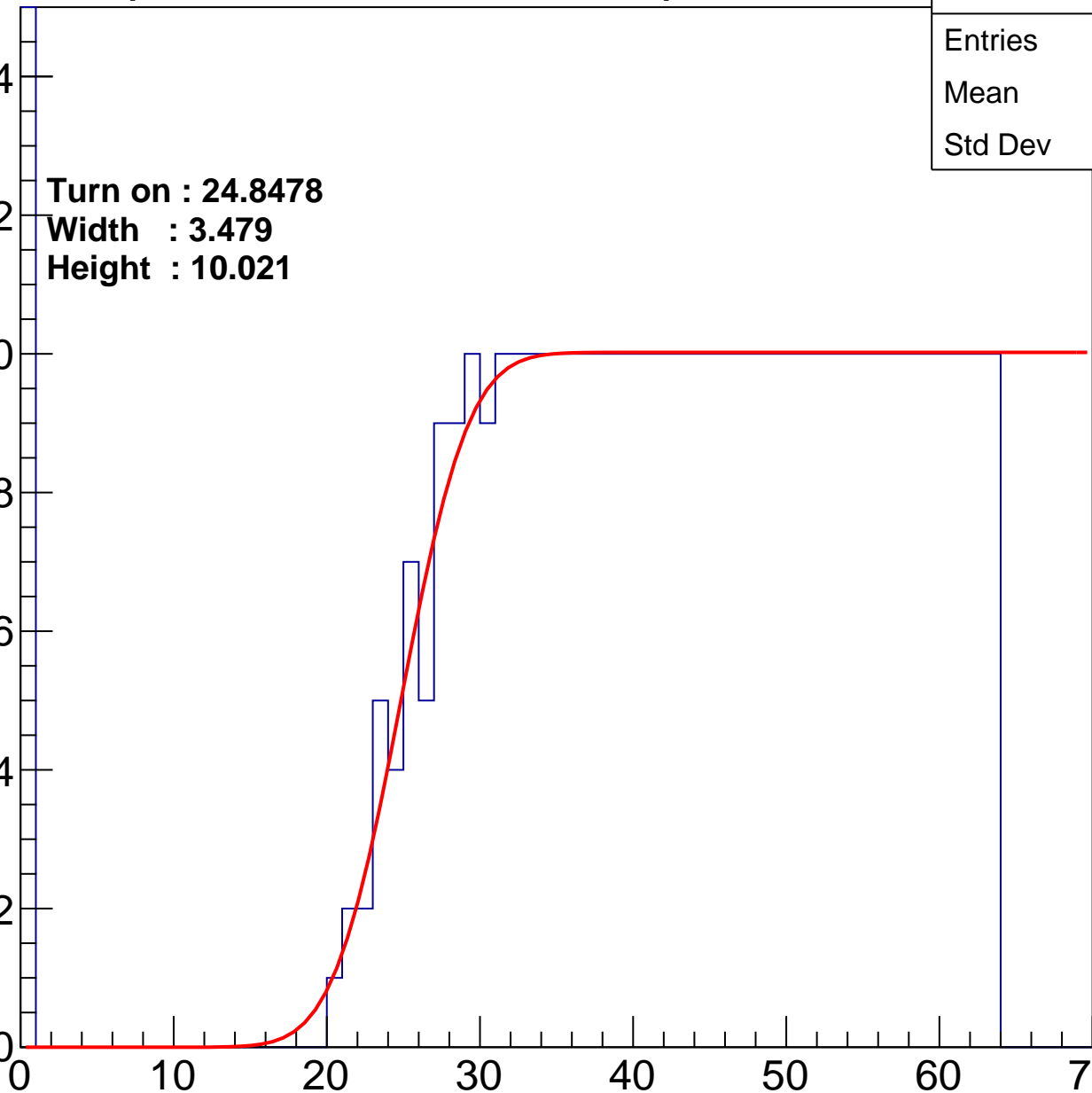
Width : 3.479

Height : 10.021

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U25-ch77

calib_packv5_041523_1651.root, FC#0, port C2

Entries	426
Mean	40.49
Std Dev	15.88

Turn on : 24.7486

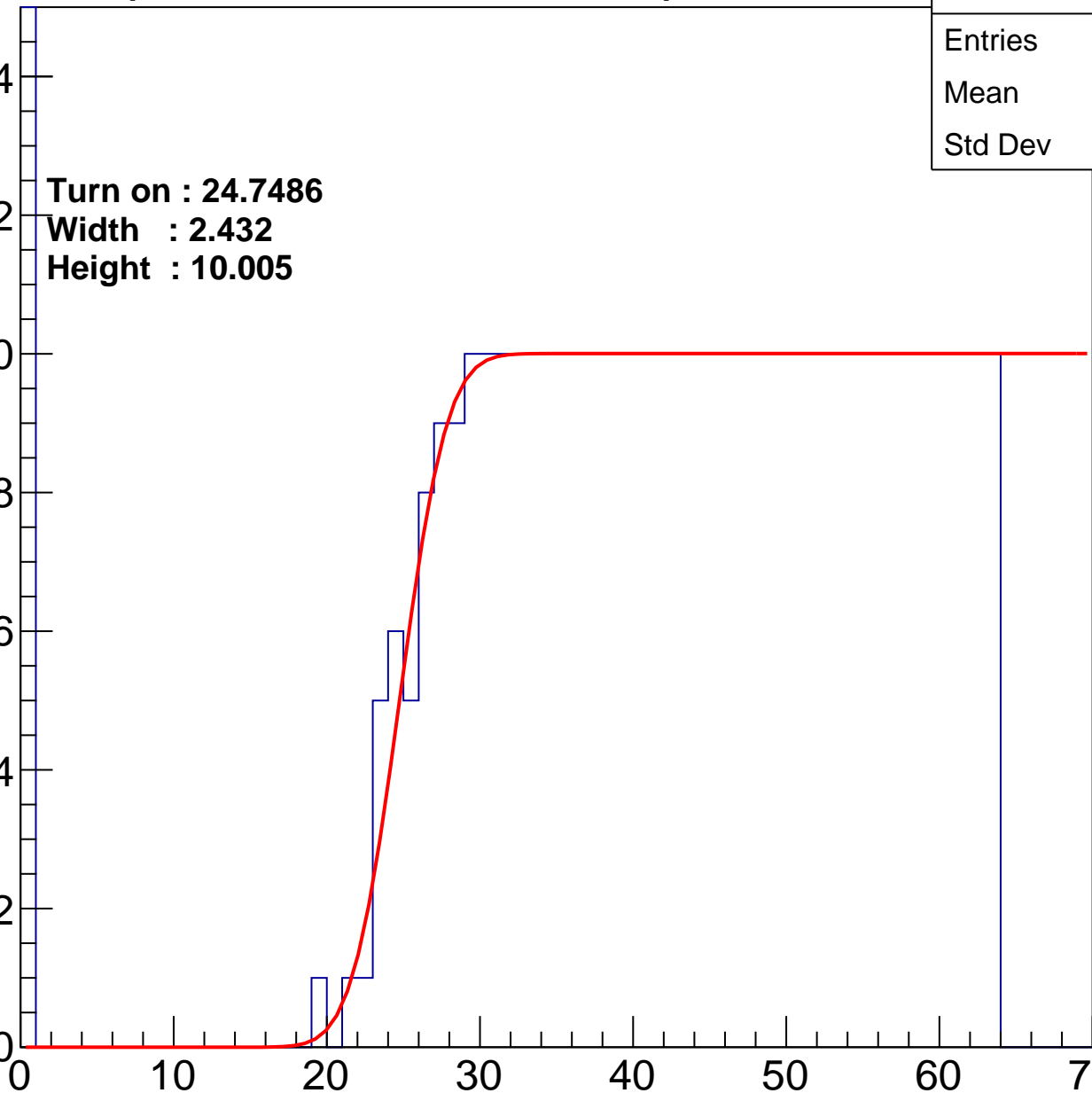
Width : 2.432

Height : 10.005

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U25-ch78

calib_packv5_041523_1651.root, FC#0, port C2

Entries	442
Mean	39.12
Std Dev	17.17

Turn on : 24.5097

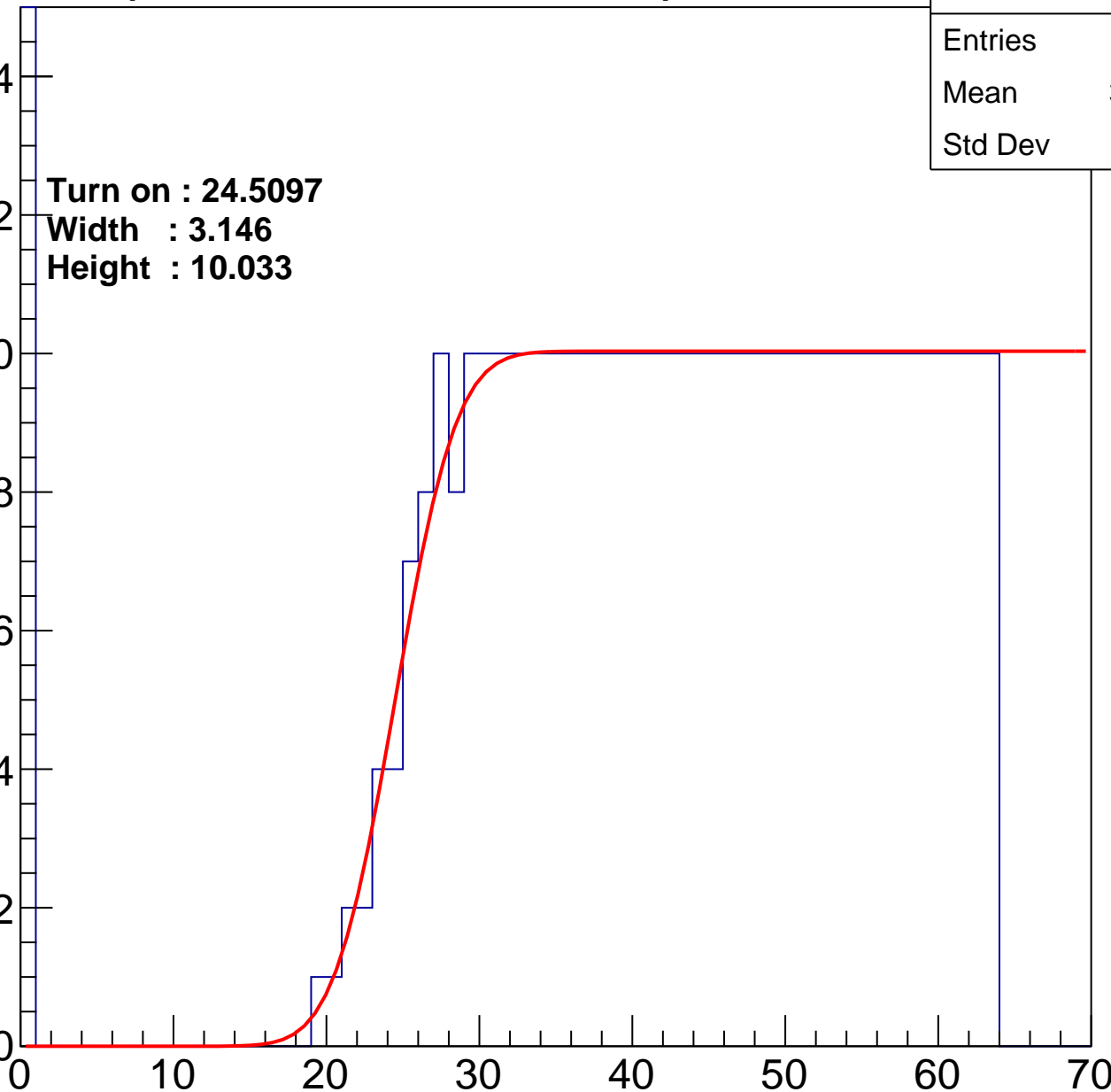
Width : 3.146

Height : 10.033

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U25-ch79

calib_packv5_041523_1651.root, FC#0, port C2

Entries	453
Mean	37.23
Std Dev	19.28

Turn on : 27.0415

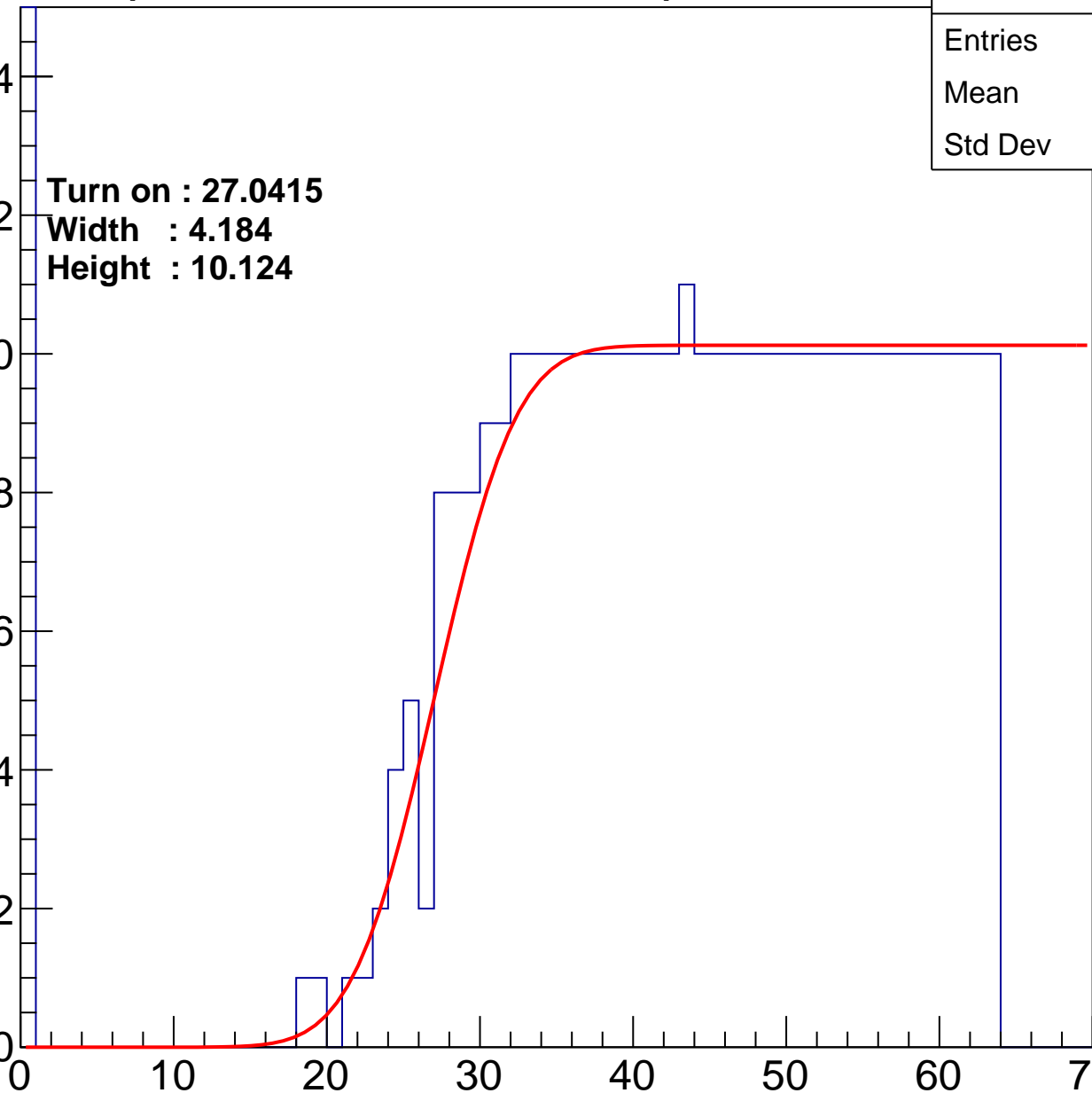
Width : 4.184

Height : 10.124

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U25-ch80

calib_packv5_041523_1651.root, FC#0, port C2

Entries	432
Mean	39.71
Std Dev	16.78

Turn on : 24.5622

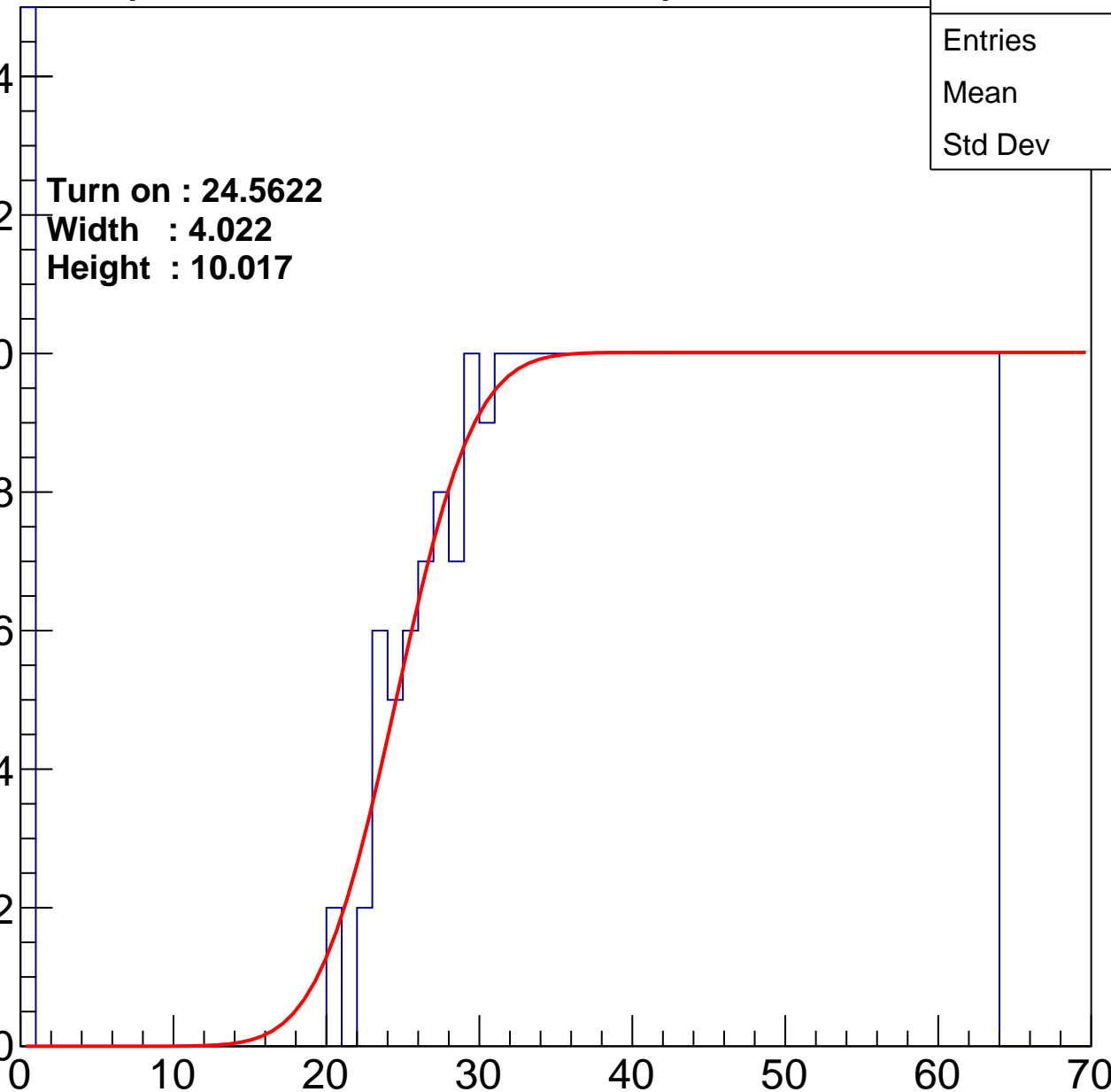
Width : 4.022

Height : 10.017

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U25-ch81

calib_packv5_041523_1651.root, FC#0, port C2

Entries	409
Mean	40.54
Std Dev	16.86

Turn on : 27.9020

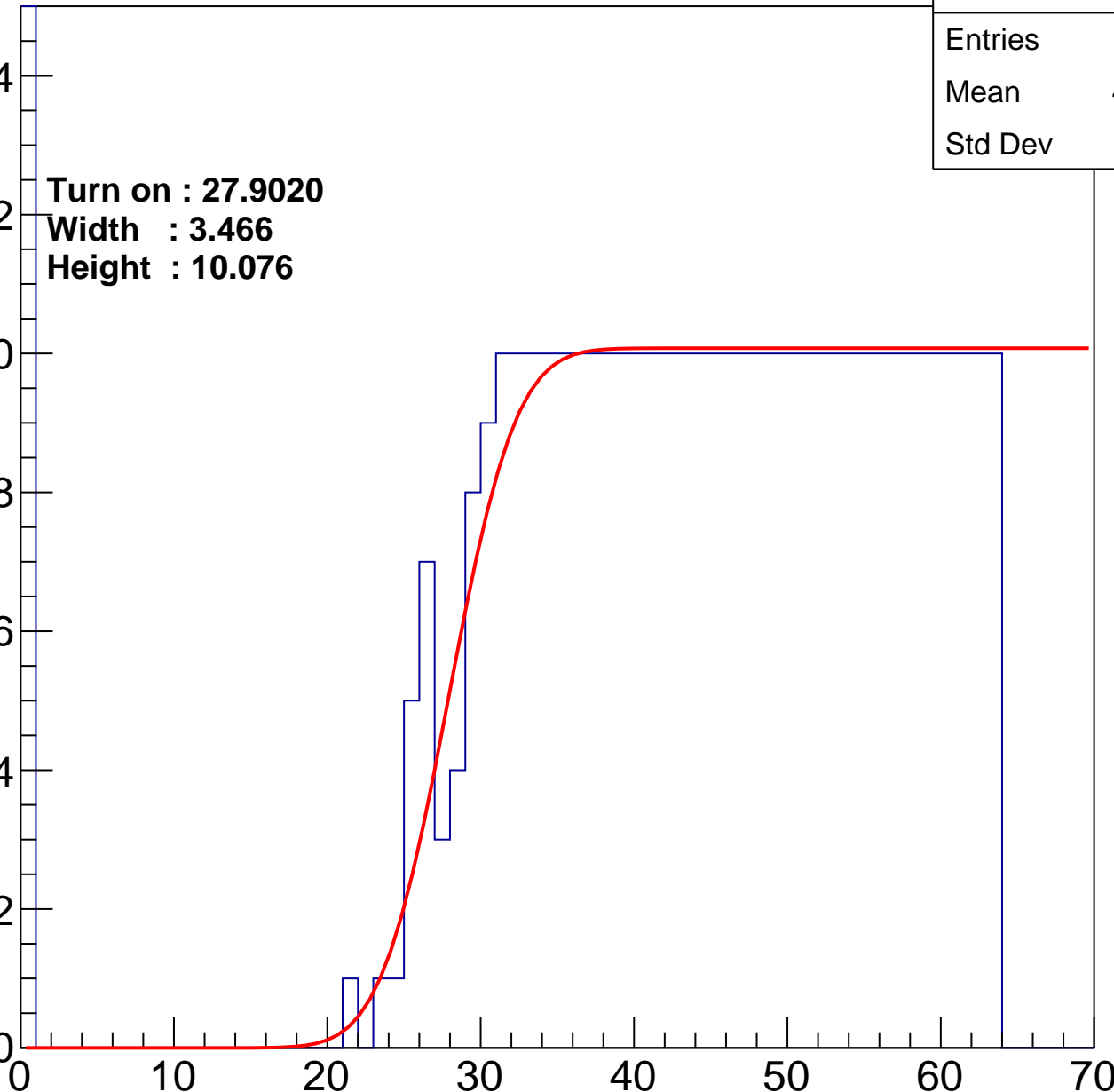
Width : 3.466

Height : 10.076

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U25-ch82

calib_packv5_041523_1651.root, FC#0, port C2

Entries	524
Mean	33.73
Std Dev	20.34

Turn on : 23.4408

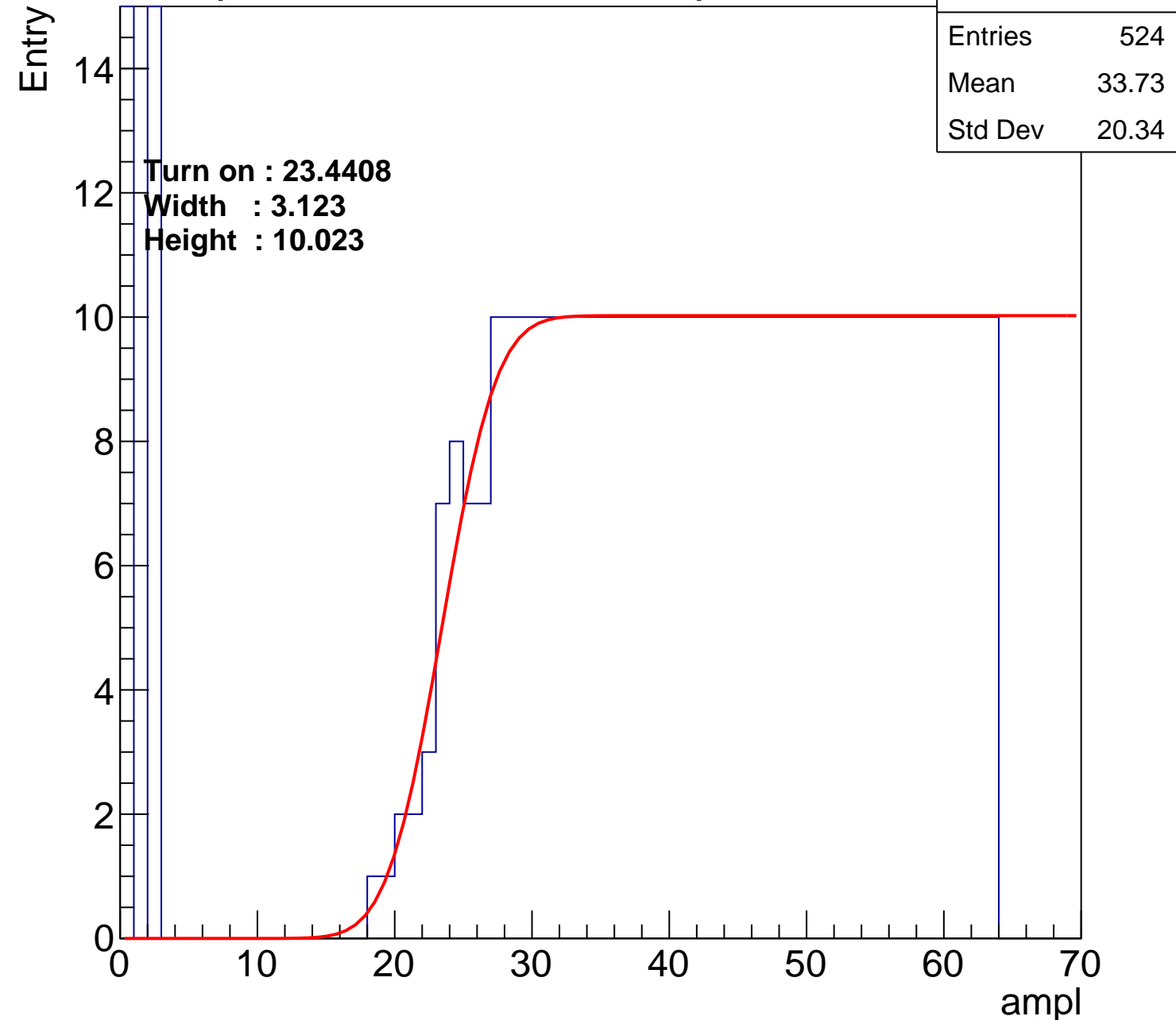
Width : 3.123

Height : 10.023

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U25-ch83

calib_packv5_041523_1651.root, FC#0, port C2

Entries	424
Mean	40.41
Std Dev	16.12

Turn on : 25.2605

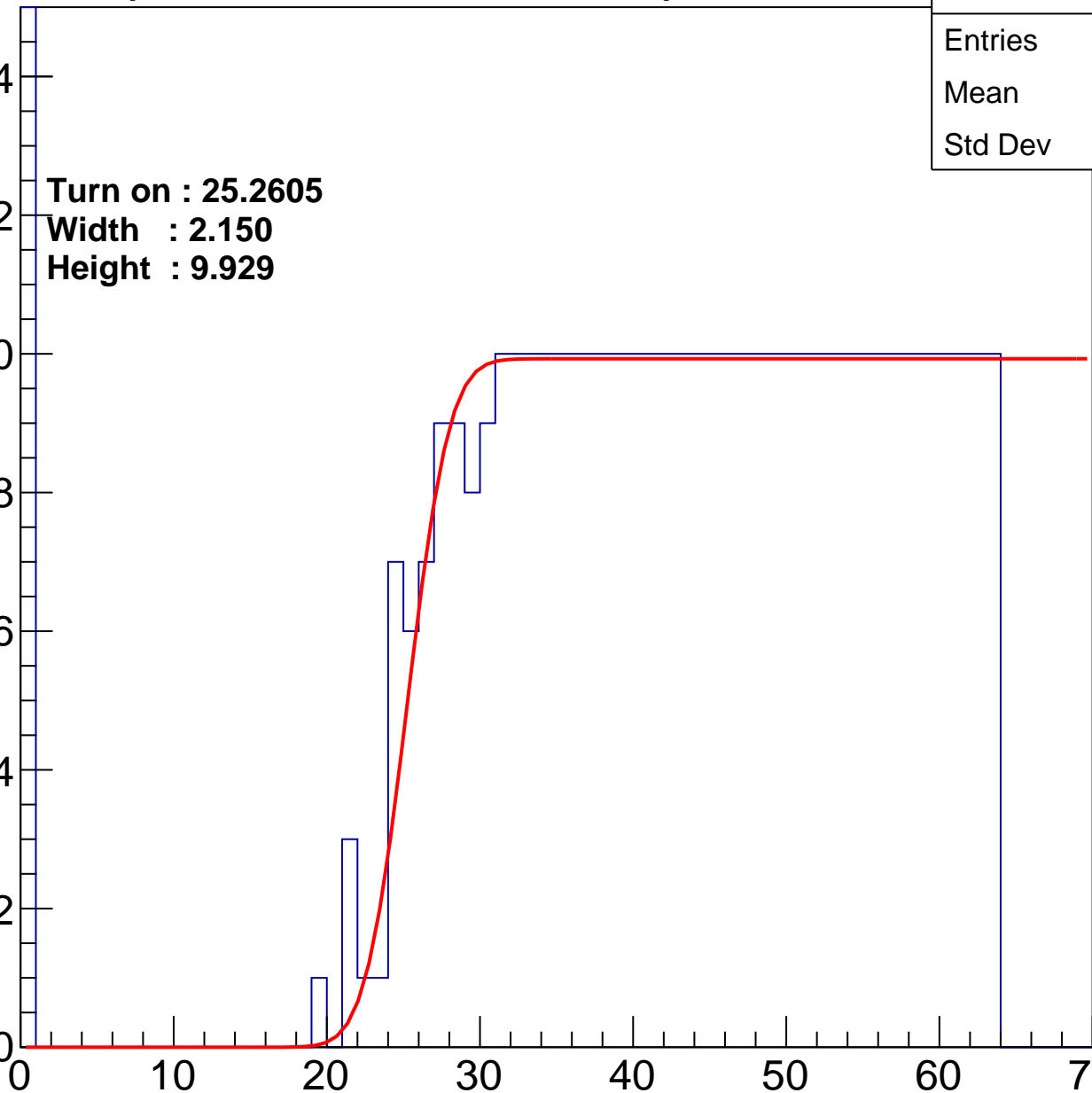
Width : 2.150

Height : 9.929

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U25-ch84

calib_packv5_041523_1651.root, FC#0, port C2

Entries	434
Mean	39.53
Std Dev	16.98

Turn on : 25.4788

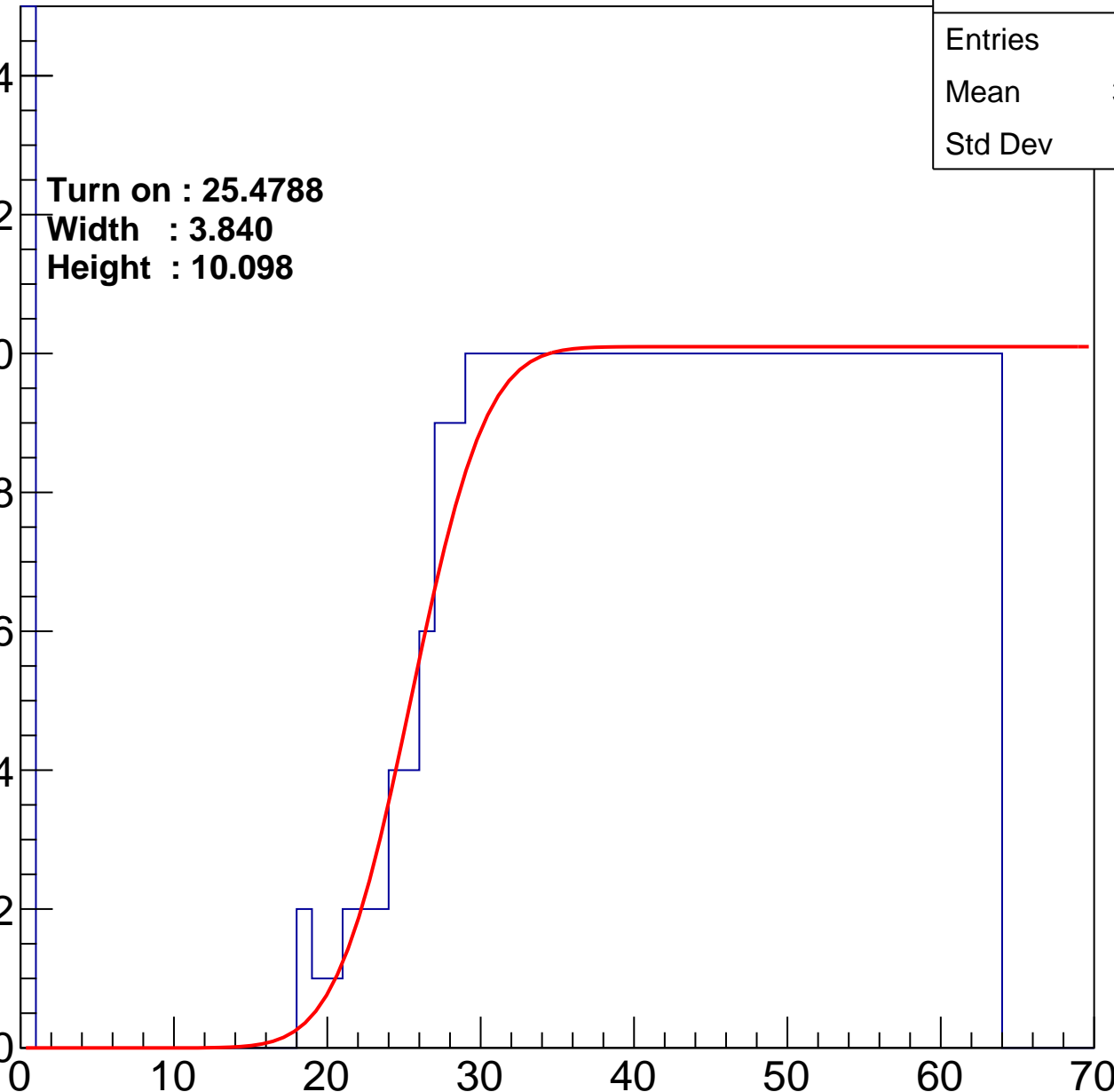
Width : 3.840

Height : 10.098

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U25-ch85

calib_packv5_041523_1651.root, FC#0, port C2

Entries	409
Mean	39.97
Std Dev	17.76

Turn on : 28.4327

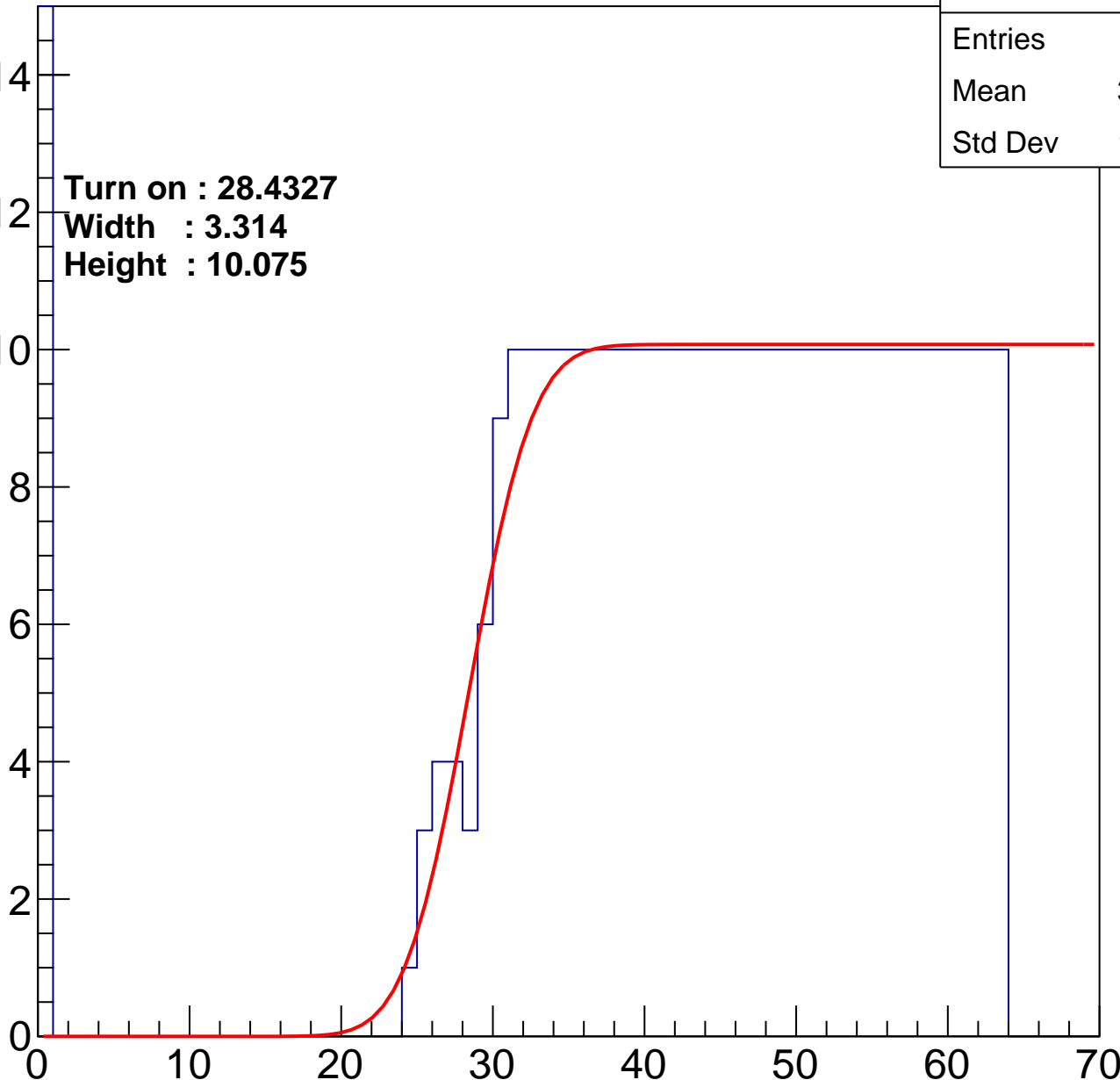
Width : 3.314

Height : 10.075

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U25-ch86

calib_packv5_041523_1651.root, FC#0, port C2

Entries	469
Mean	37.52
Std Dev	18.08

Turn on : 23.1237

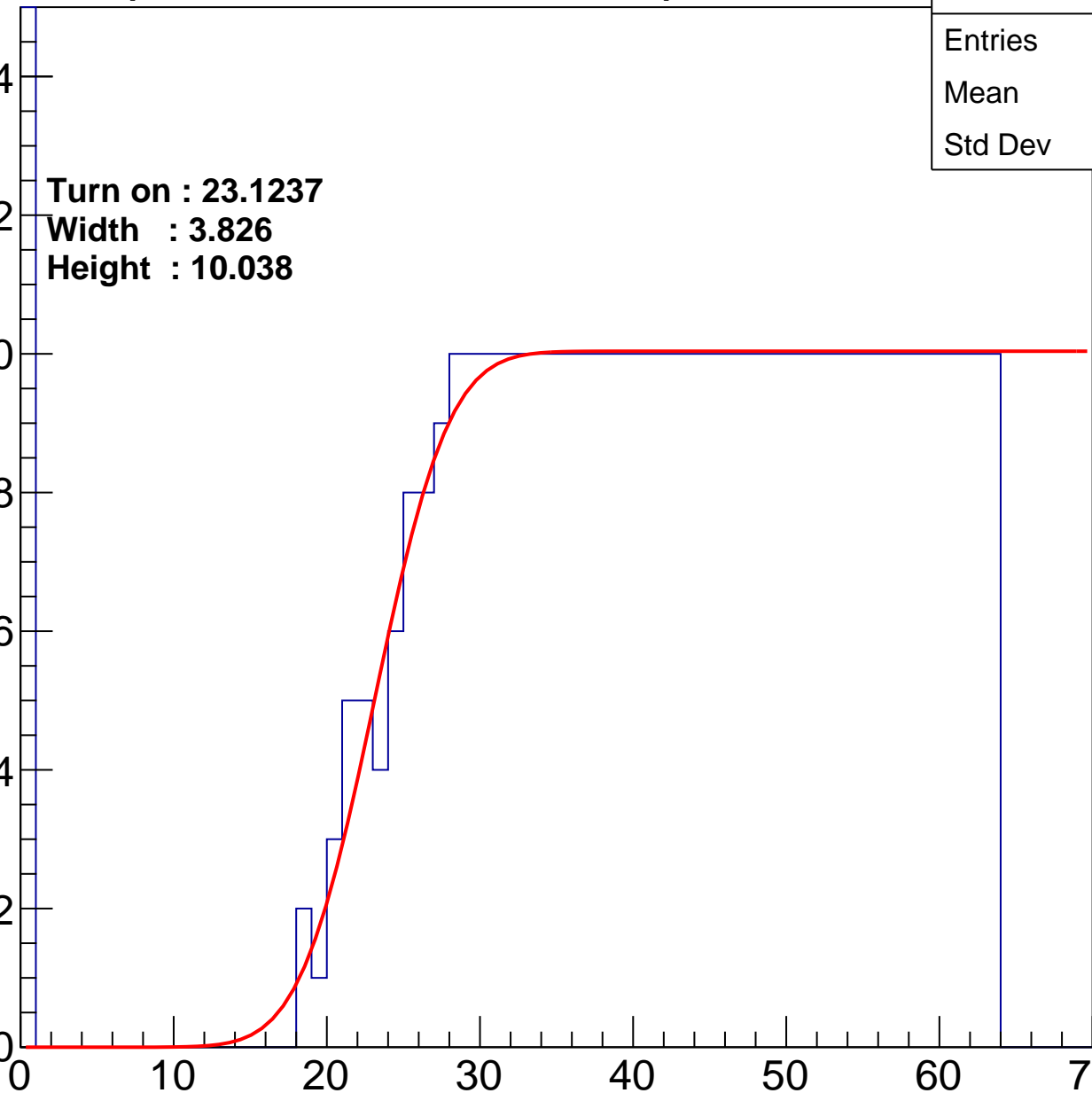
Width : 3.826

Height : 10.038

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U25-ch87

calib_packv5_041523_1651.root, FC#0, port C2

Entries	441
Mean	39.21
Std Dev	17.08

Turn on : 24.7318

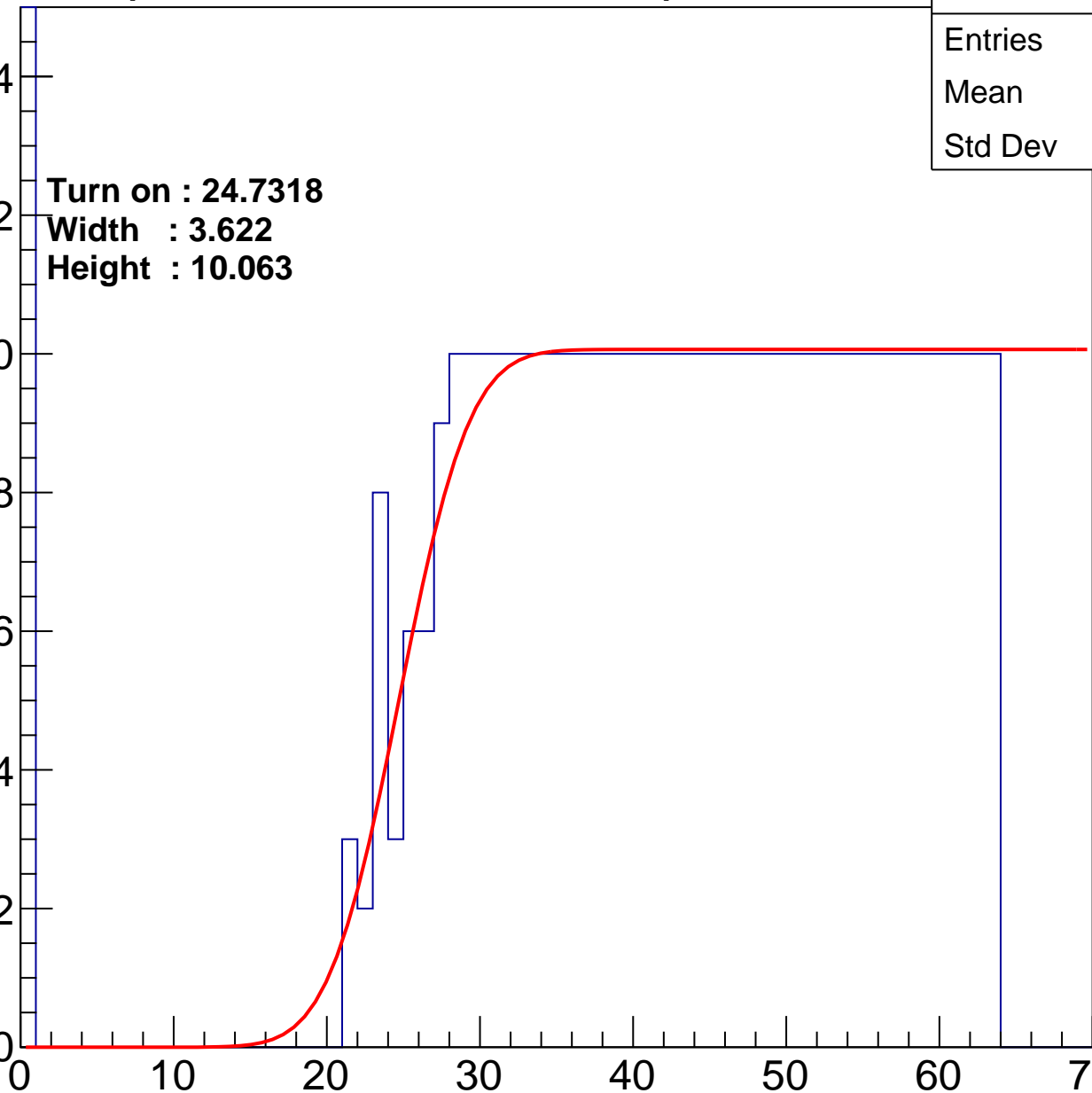
Width : 3.622

Height : 10.063

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U25-ch88

calib_packv5_041523_1651.root, FC#0, port C2

Entries	453
Mean	38.36
Std Dev	17.74

Turn on : 24.1772

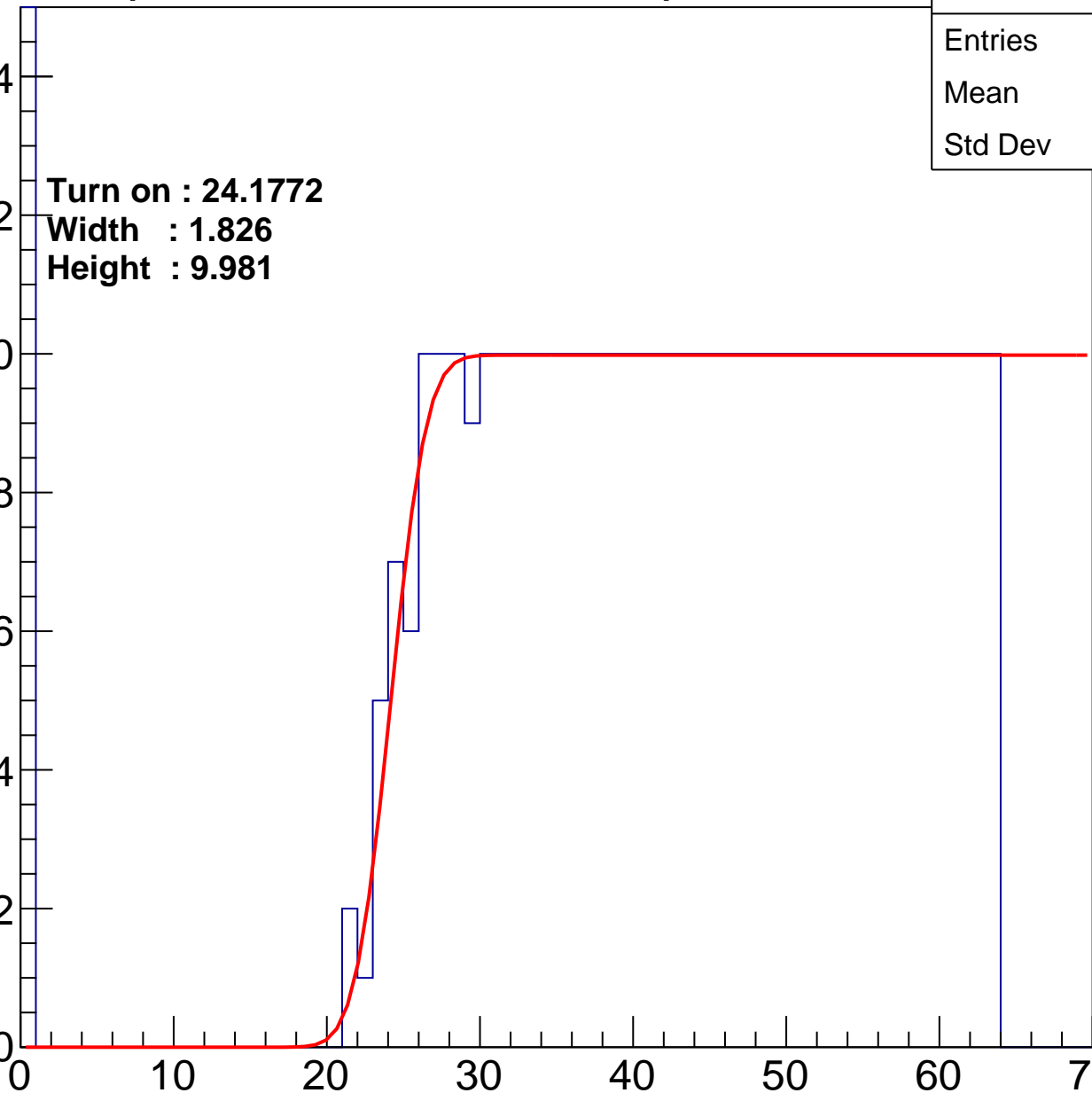
Width : 1.826

Height : 9.981

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U25-ch89

calib_packv5_041523_1651.root, FC#0, port C2

Entries	416
Mean	40.25
Std Dev	16.91

Turn on : 26.2008

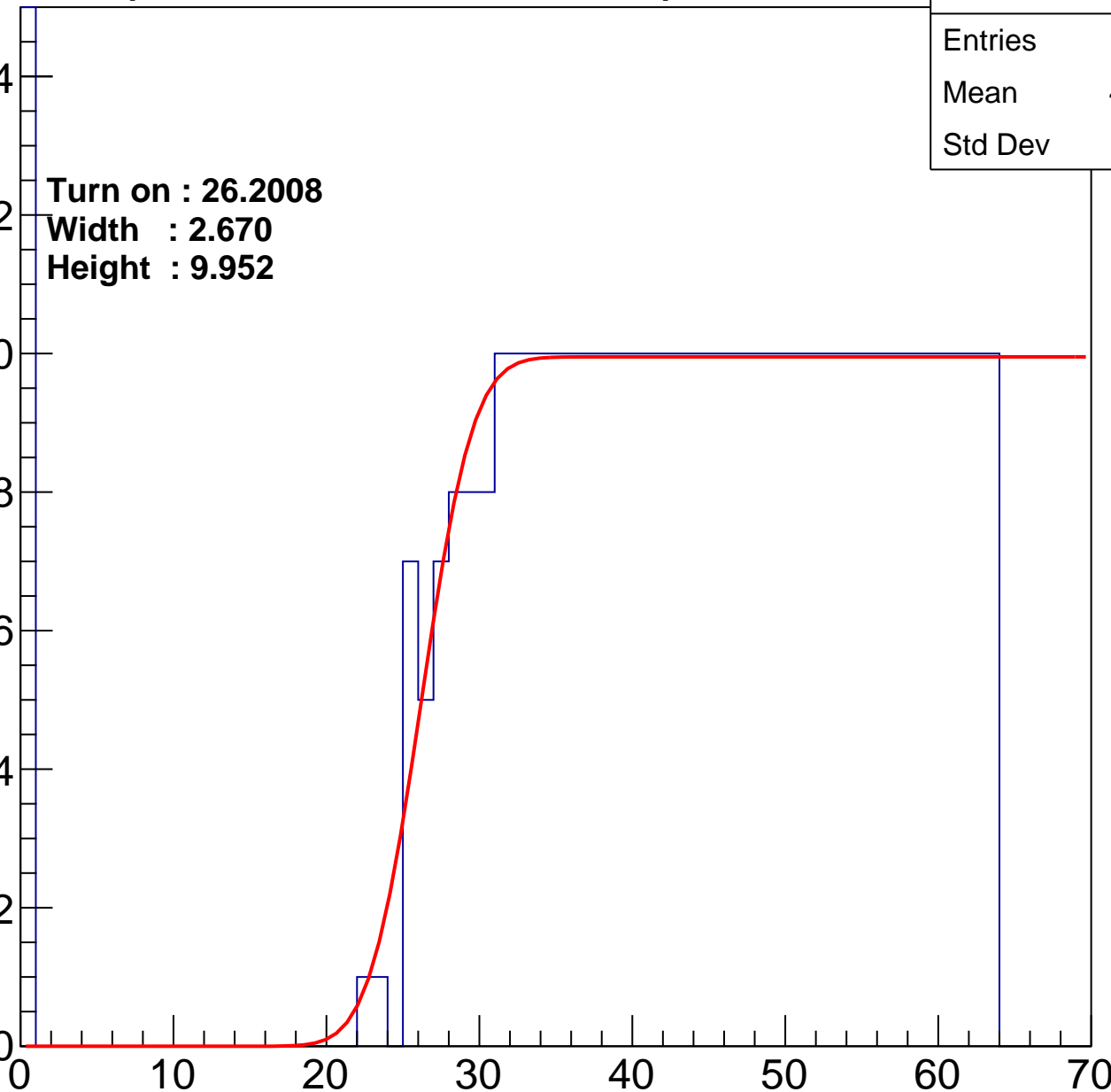
Width : 2.670

Height : 9.952

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U25-ch90

calib_packv5_041523_1651.root, FC#0, port C2

Entries	423
Mean	39.88
Std Dev	17.08

Turn on : 26.2448

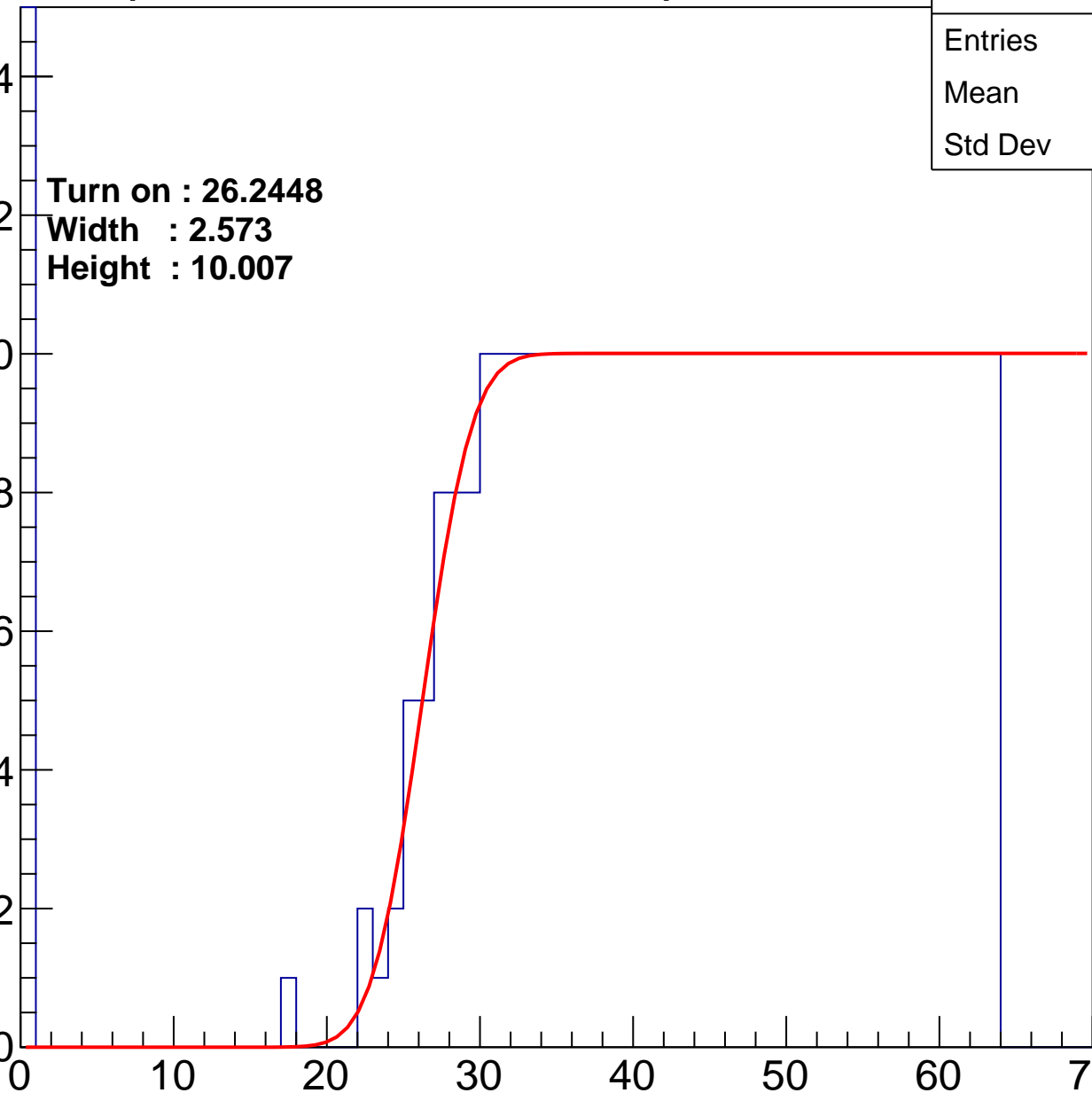
Width : 2.573

Height : 10.007

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U25-ch91

calib_packv5_041523_1651.root, FC#0, port C2

Entries	456
Mean	38.21
Std Dev	17.77

Turn on : 24.0344

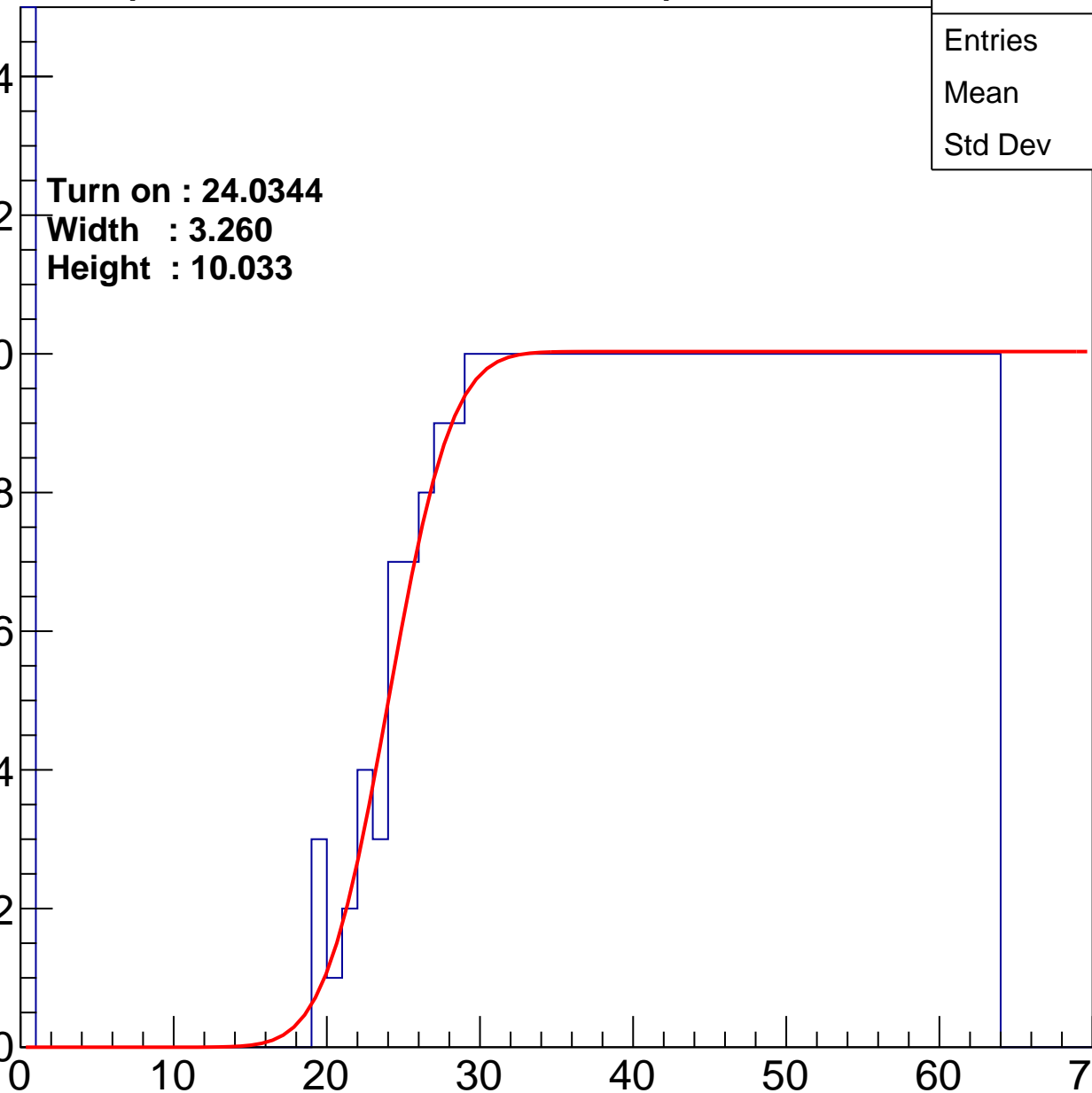
Width : 3.260

Height : 10.033

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U25-ch92

calib_packv5_041523_1651.root, FC#0, port C2

Entries	432
Mean	39.77
Std Dev	16.69

Turn on : 24.1954

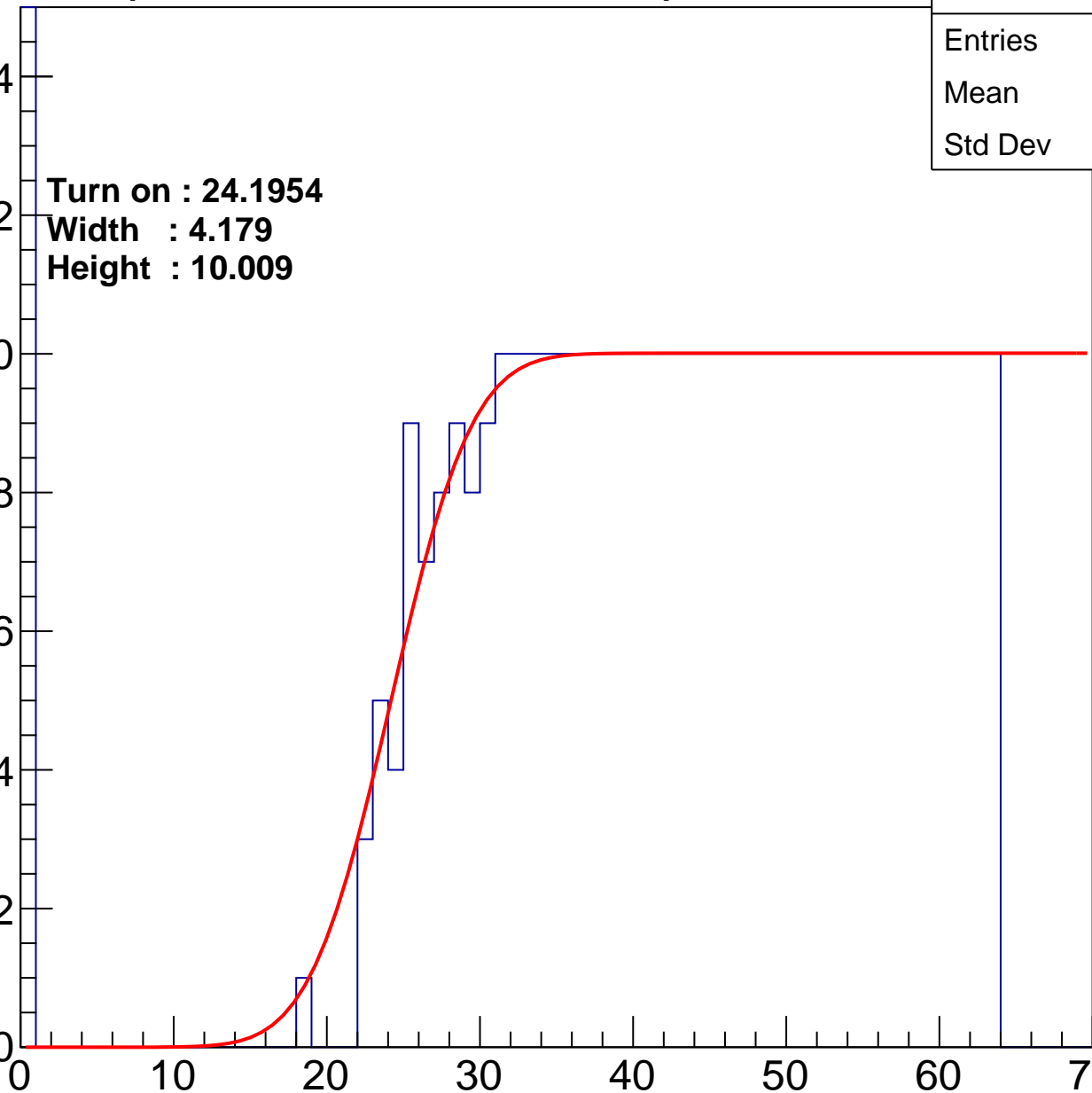
Width : 4.179

Height : 10.009

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U25-ch93

calib_packv5_041523_1651.root, FC#0, port C2

Entries	427
Mean	38.98
Std Dev	18.17

Turn on : 27.2039

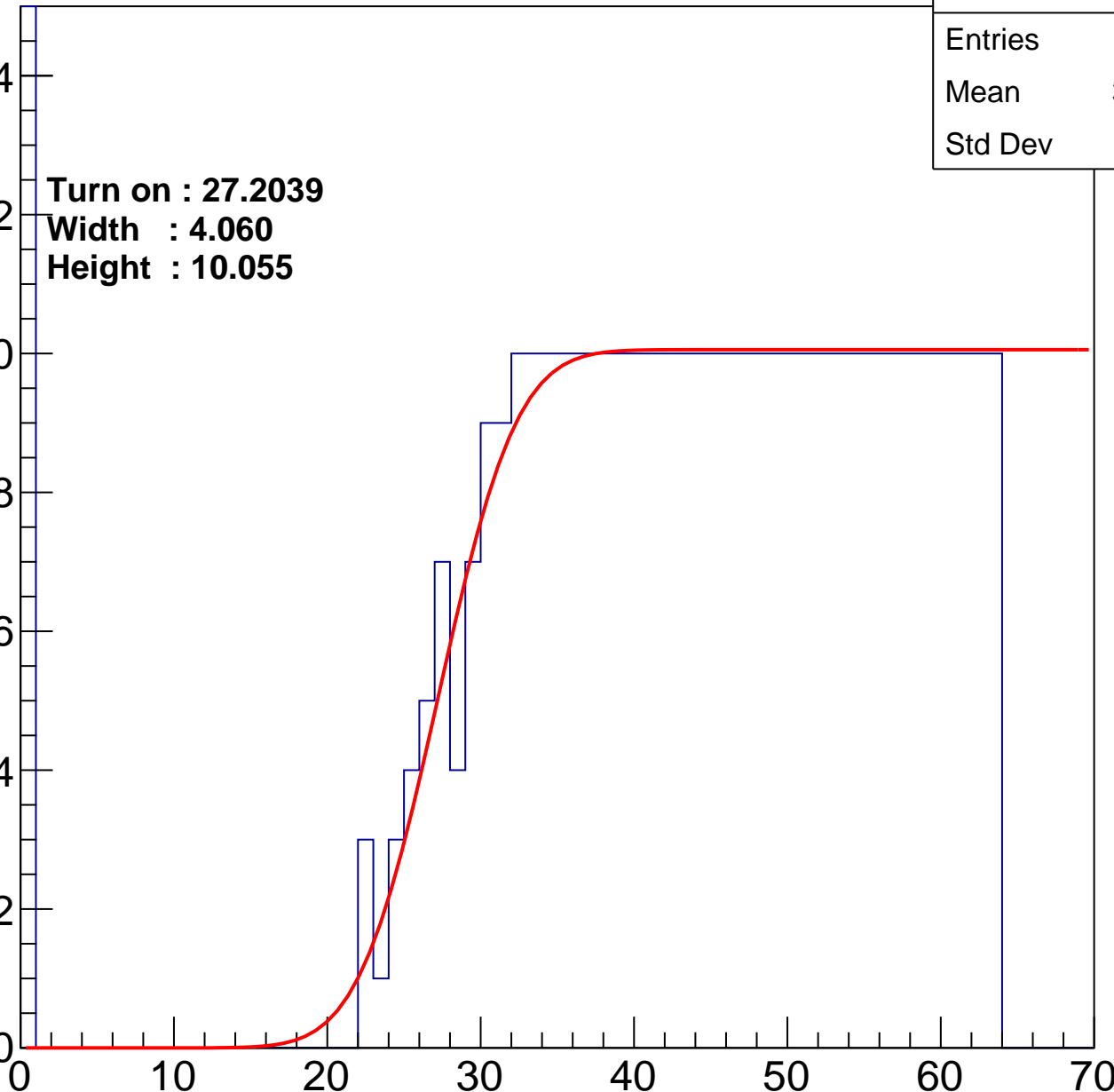
Width : 4.060

Height : 10.055

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U25-ch94

calib_packv5_041523_1651.root, FC#0, port C2

Entries	465
Mean	37.83
Std Dev	17.86

Turn on : 23.1243

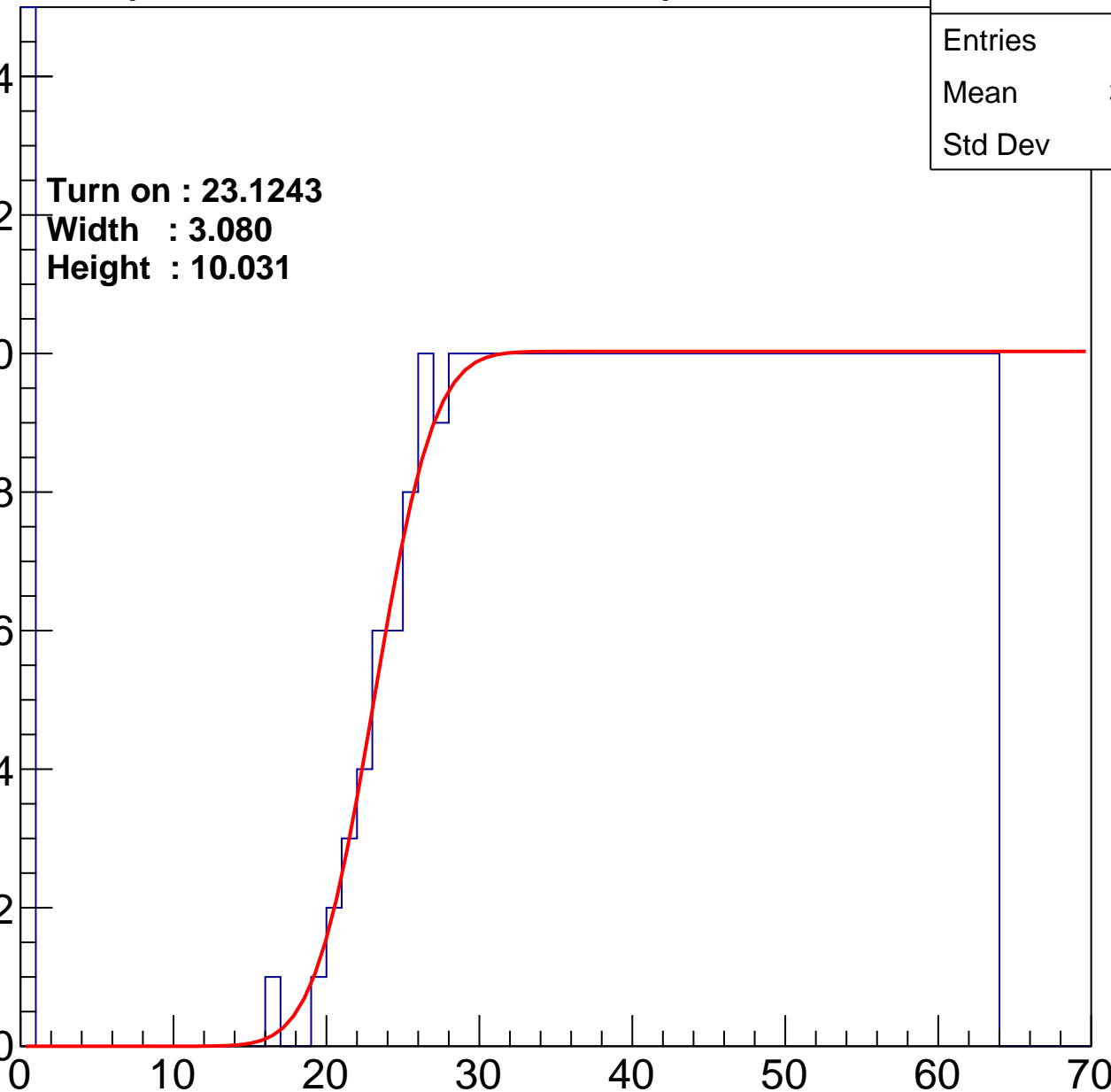
Width : 3.080

Height : 10.031

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U25-ch95

calib_packv5_041523_1651.root, FC#0, port C2

Entries	426
Mean	39.65
Std Dev	17.25

Turn on : 26.1454

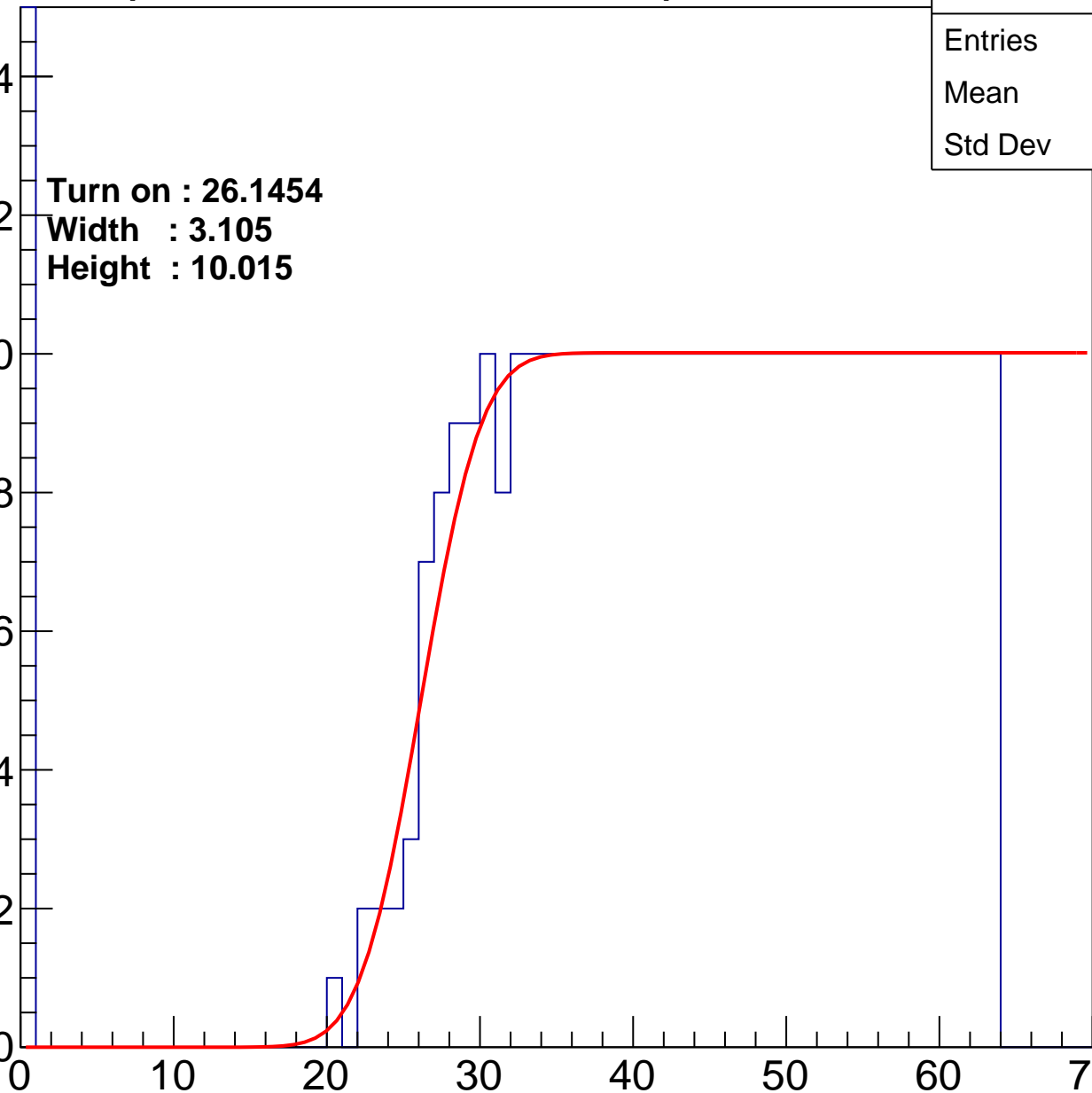
Width : 3.105

Height : 10.015

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U25-ch96

calib_packv5_041523_1651.root, FC#0, port C2

Entries	439
Mean	39.59
Std Dev	16.56

Turn on : 23.8507

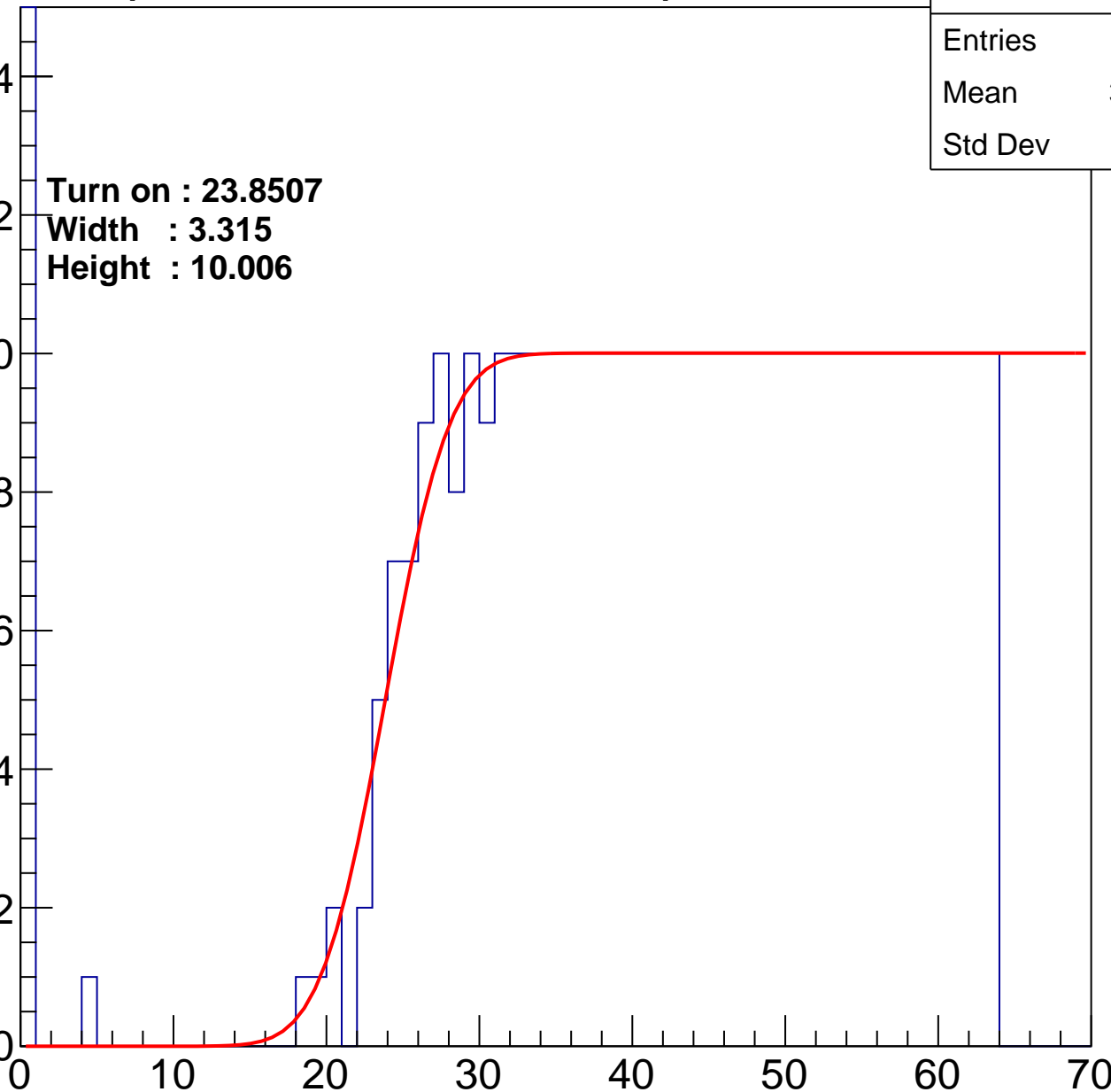
Width : 3.315

Height : 10.006

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U25-ch97

calib_packv5_041523_1651.root, FC#0, port C2

Entries	437
Mean	39.61
Std Dev	16.67

Turn on : 23.9024

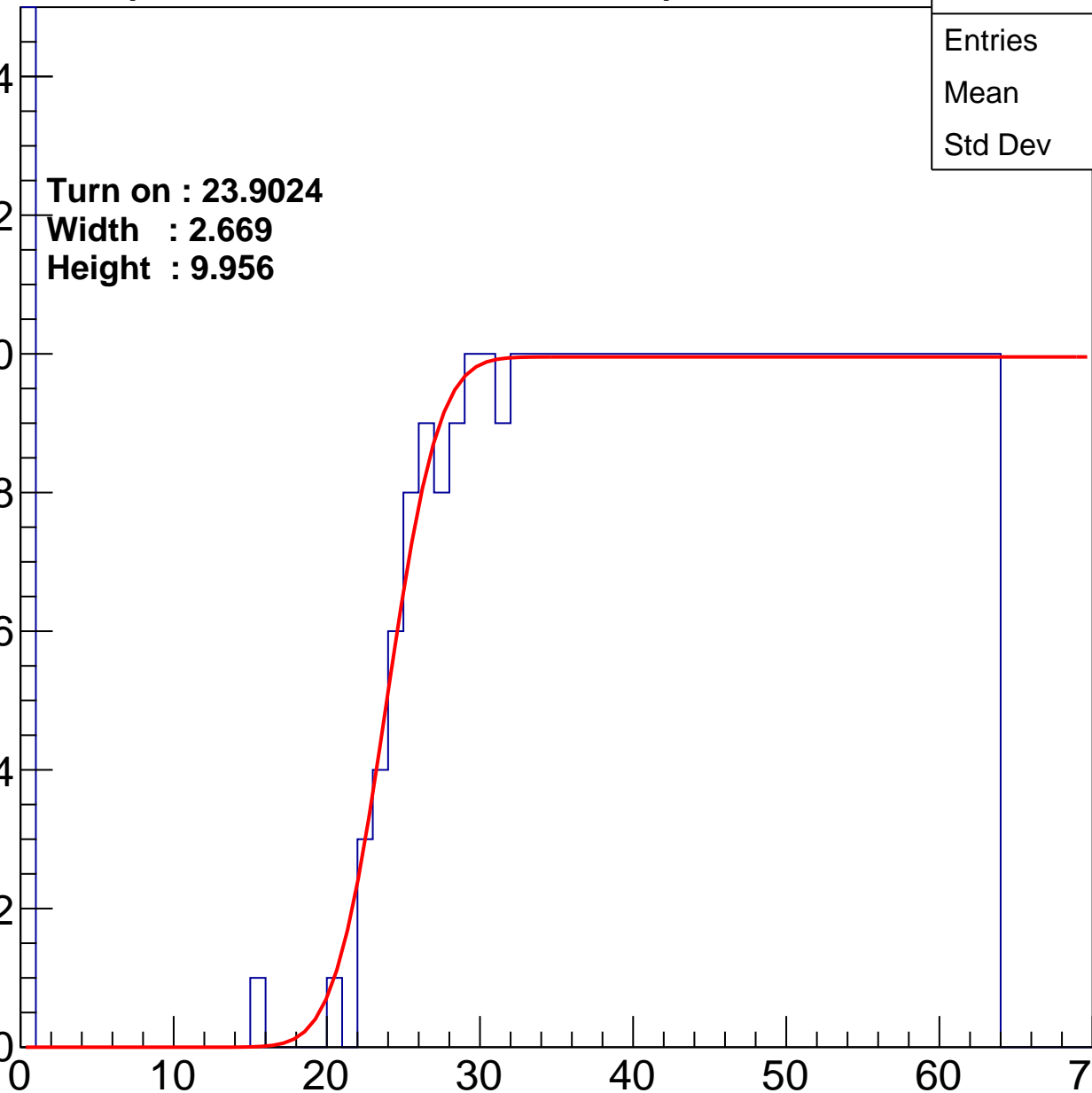
Width : 2.669

Height : 9.956

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U25-ch98

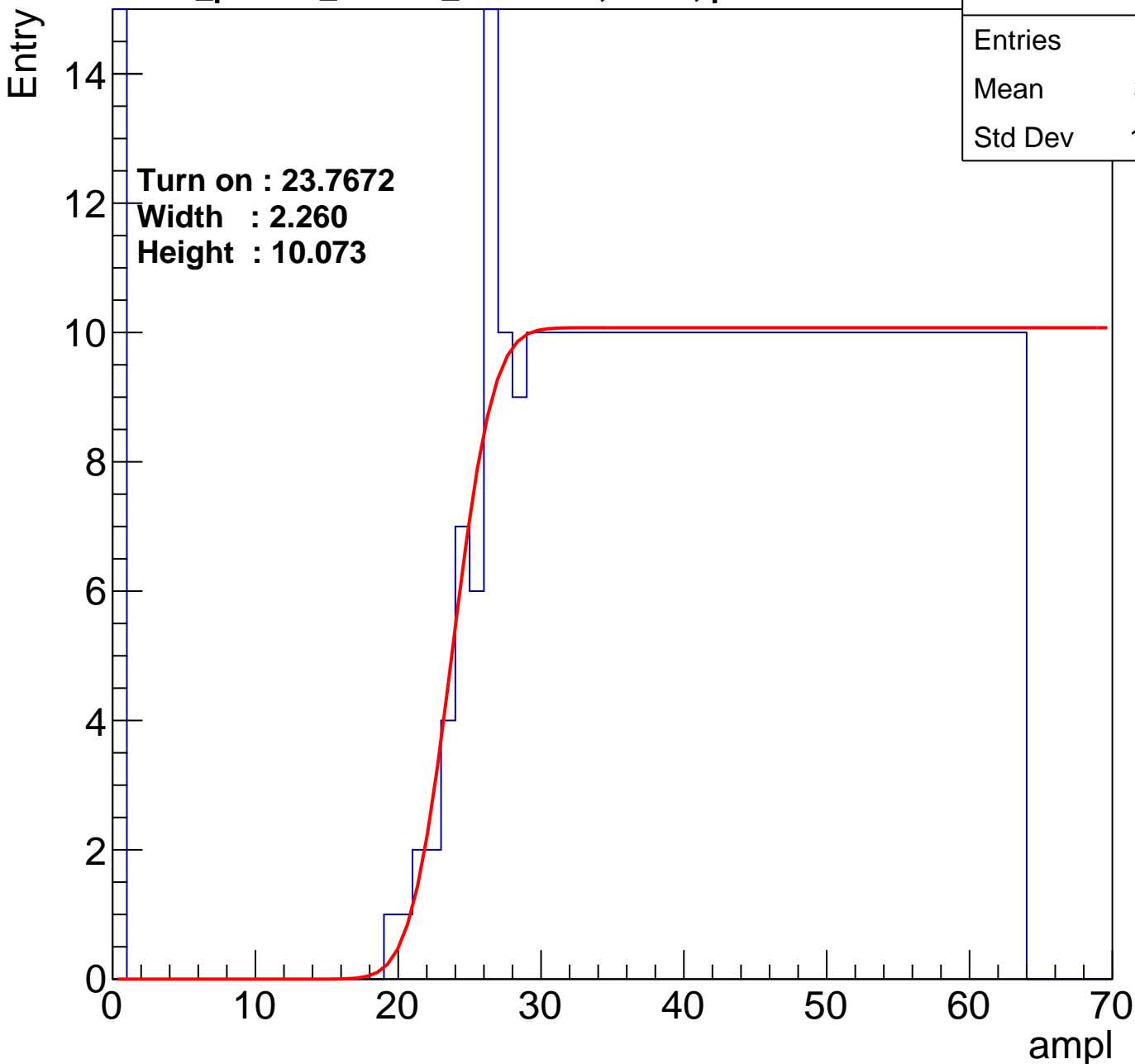
calib_packv5_041523_1651.root, FC#0, port C2

Entries	462
Mean	38.71
Std Dev	16.76

Turn on : 23.7672

Width : 2.260

Height : 10.073



B1L103S, U25-ch99

calib_packv5_041523_1651.root, FC#0, port C2

Entries	412
Mean	40.55
Std Dev	16.65

Turn on : 27.1088

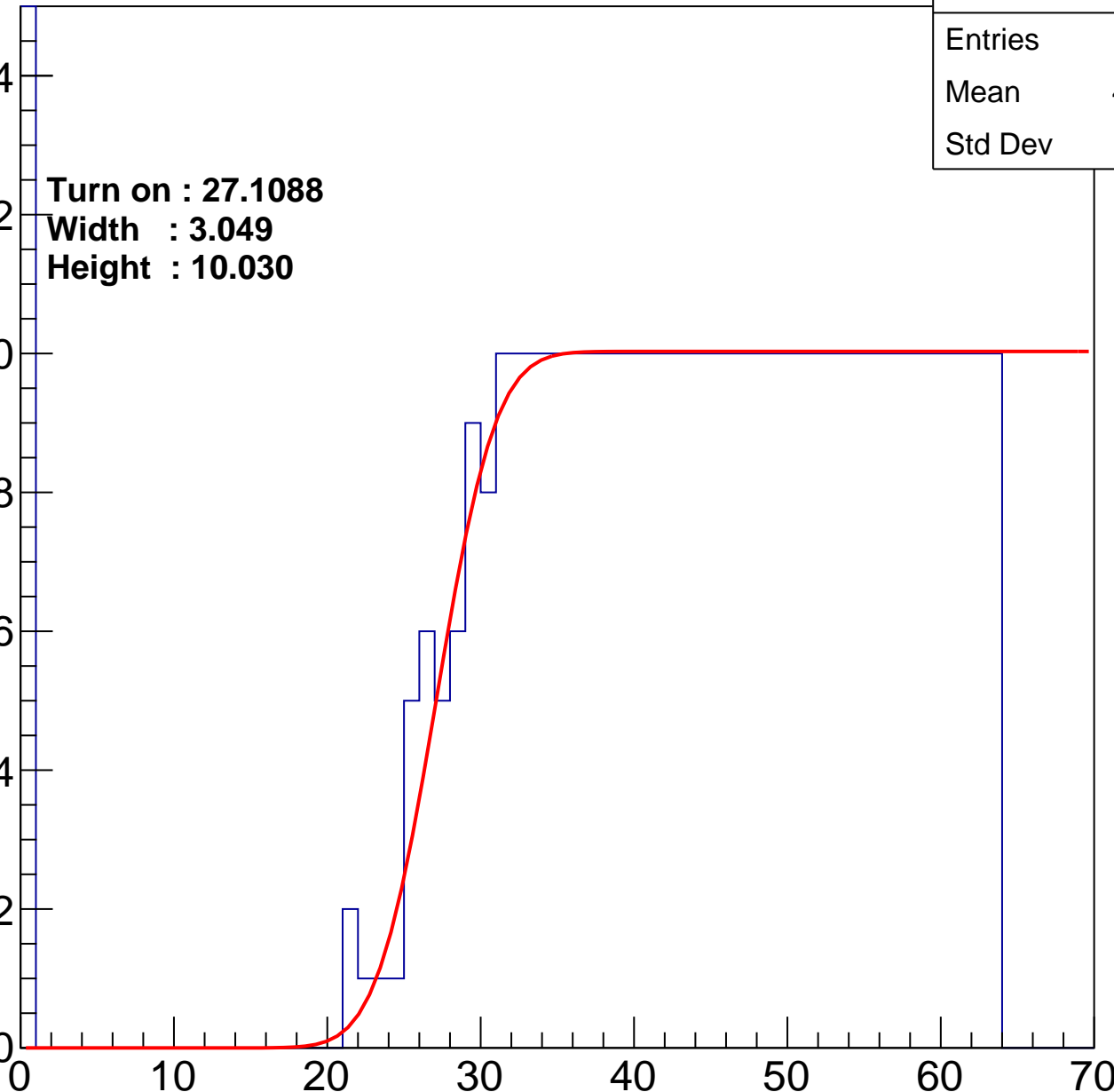
Width : 3.049

Height : 10.030

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U25-ch100

calib_packv5_041523_1651.root, FC#0, port C2

Entries	459
Mean	38.46
Std Dev	17.19

Turn on : 22.7307

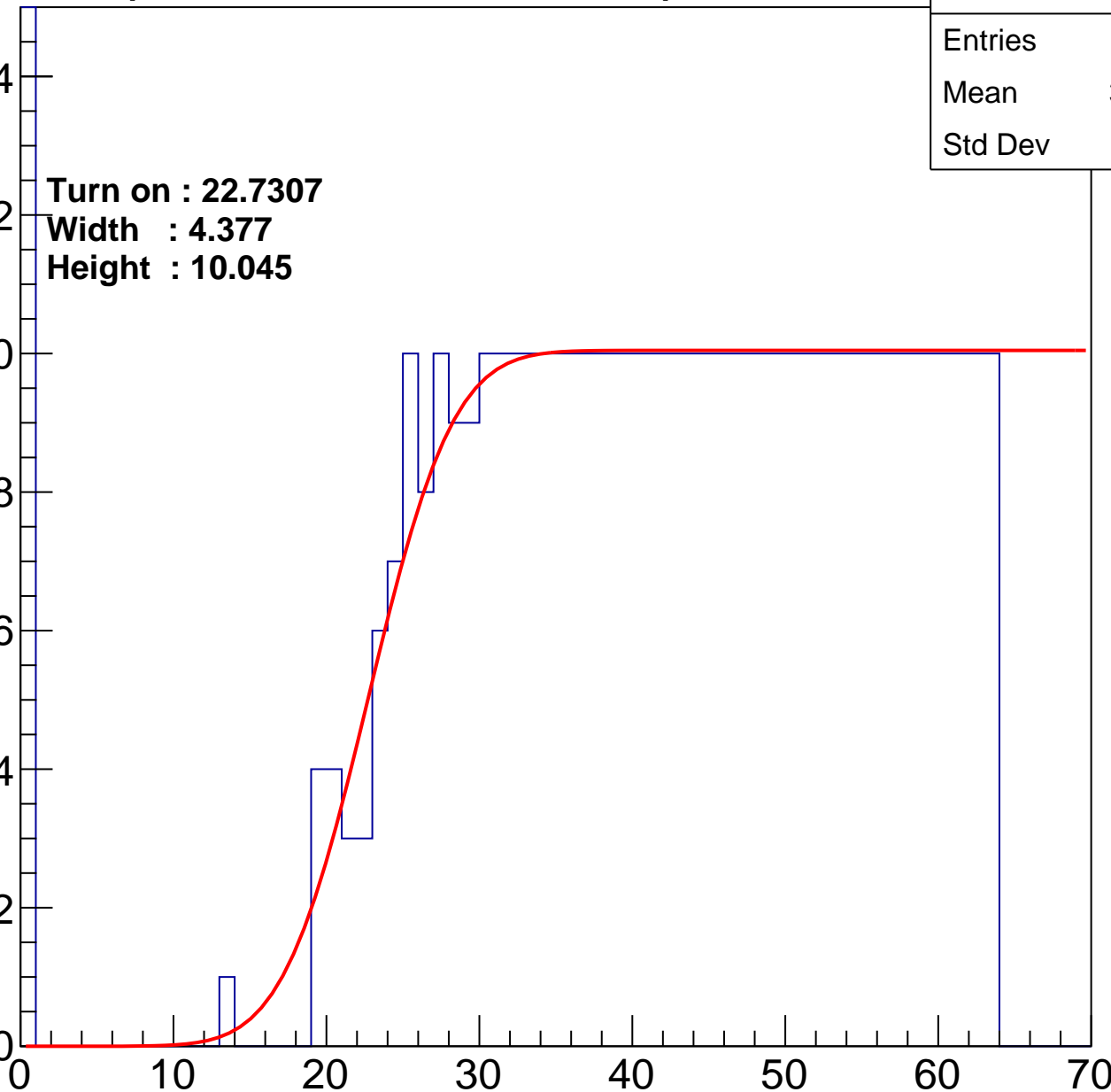
Width : 4.377

Height : 10.045

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U25-ch101

calib_packv5_041523_1651.root, FC#0, port C2

Entries	437
Mean	39.01
Std Dev	17.62

Turn on : 26.2083

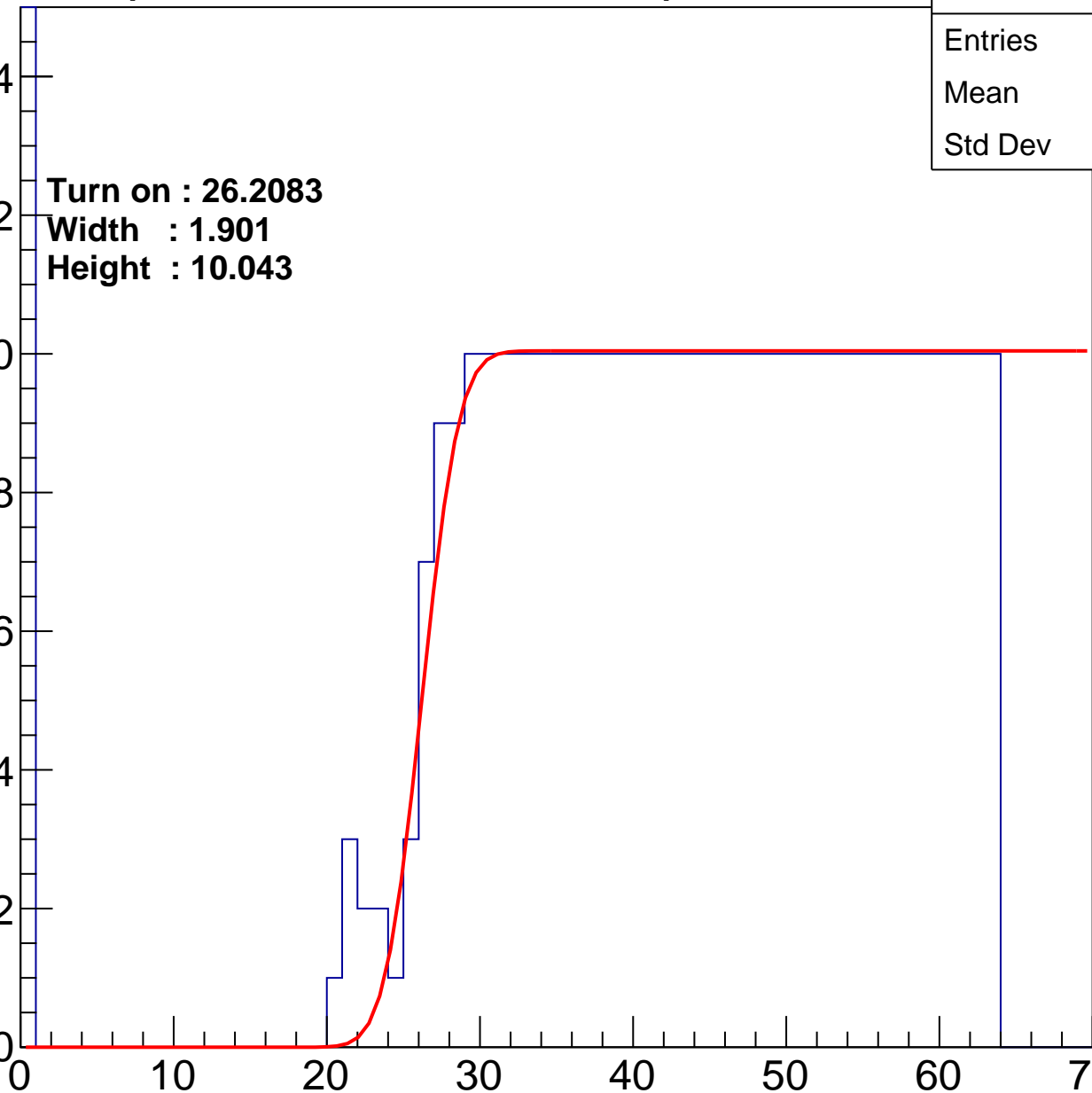
Width : 1.901

Height : 10.043

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U25-ch102

calib_packv5_041523_1651.root, FC#0, port C2

Entries	444
Mean	38.56
Std Dev	17.92

Turn on : 25.7387

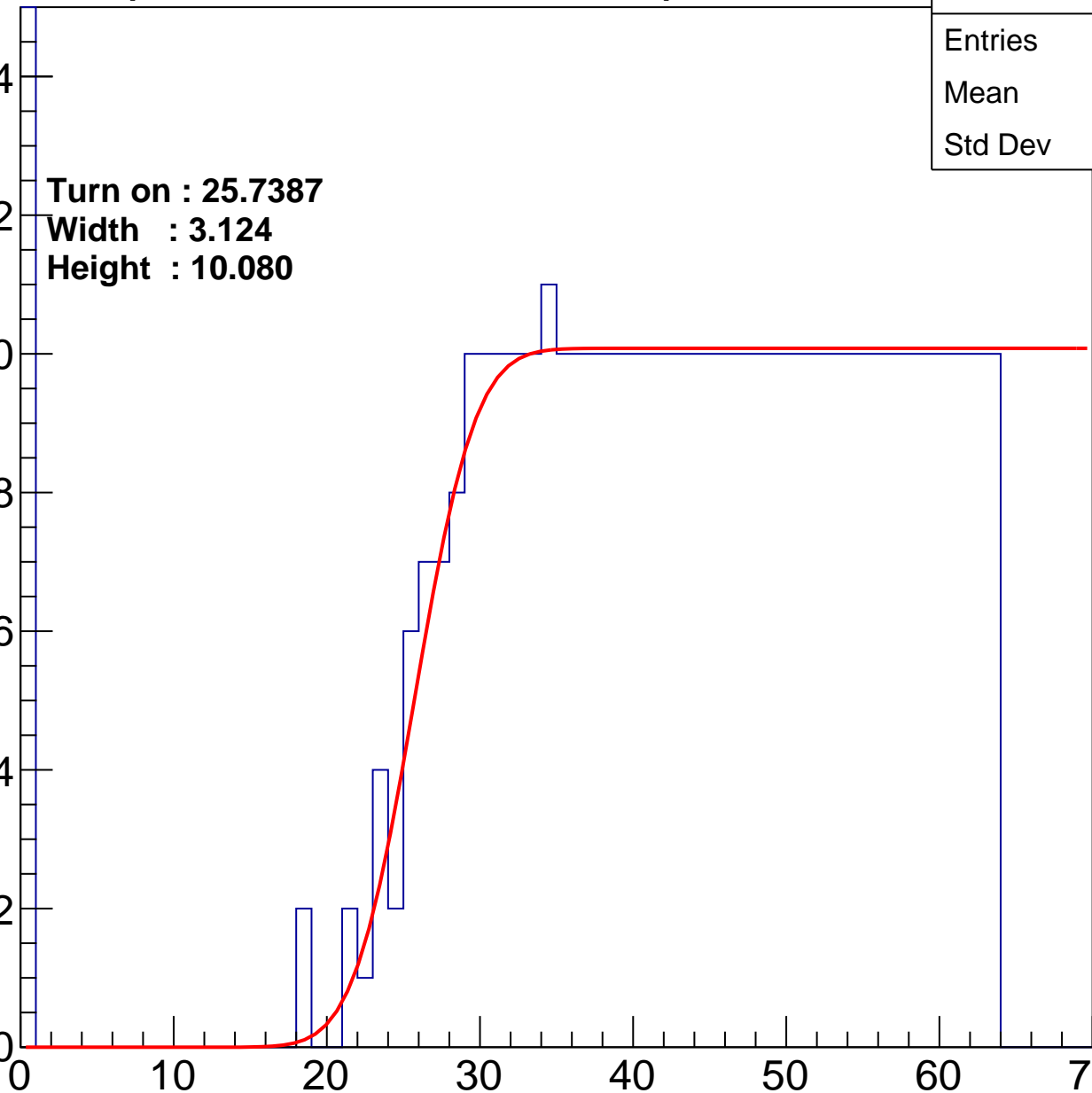
Width : 3.124

Height : 10.080

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U25-ch103

calib_packv5_041523_1651.root, FC#0, port C2

Entries	455
Mean	37.74
Std Dev	18.47

Turn on : 24.9145

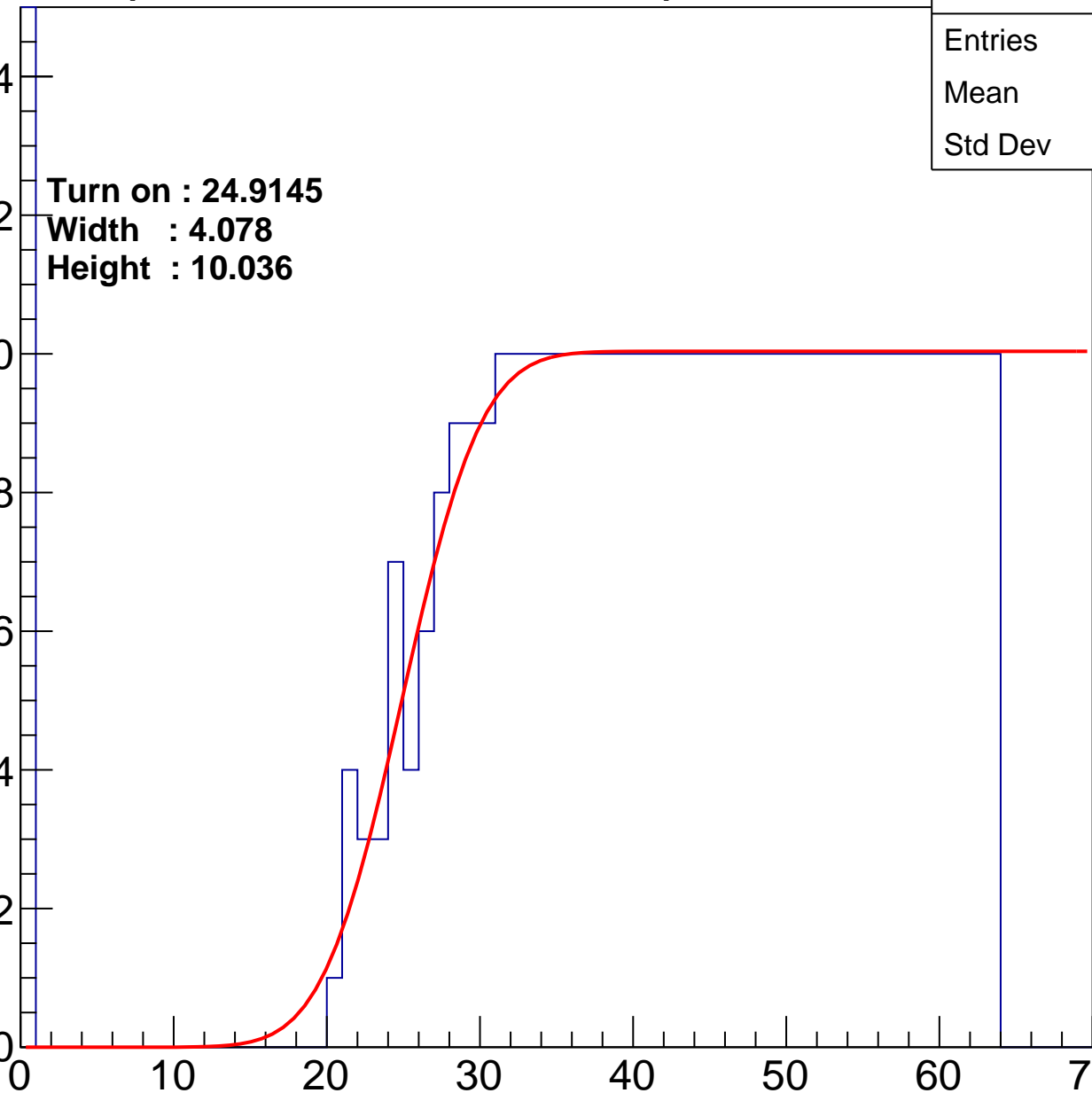
Width : 4.078

Height : 10.036

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U25-ch104

calib_packv5_041523_1651.root, FC#0, port C2

Entries	472
Mean	37.32
Std Dev	18.24

Turn on : 23.1769

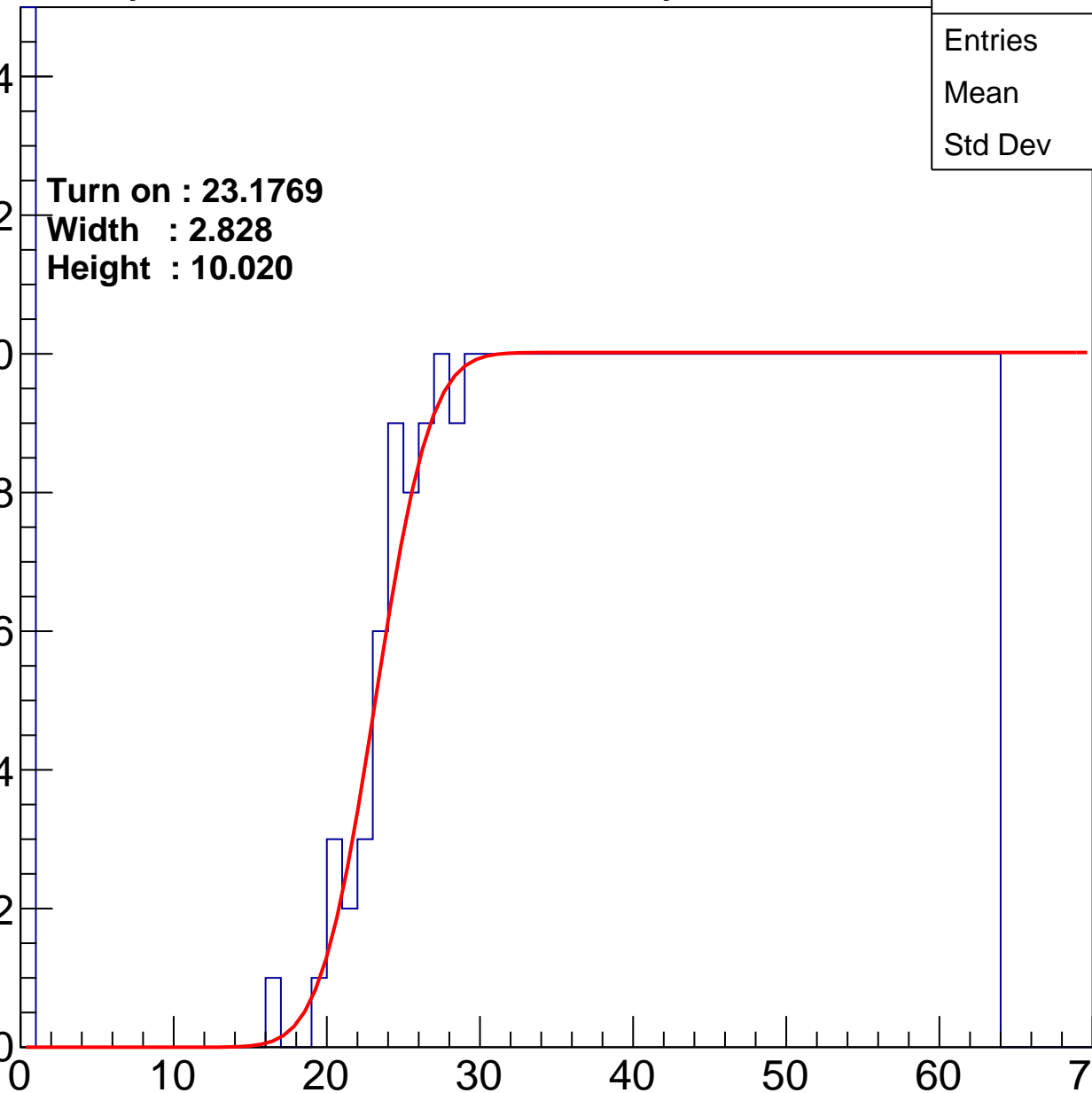
Width : 2.828

Height : 10.020

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U25-ch105

calib_packv5_041523_1651.root, FC#0, port C2

Entries	441
Mean	38.44
Std Dev	18.32

Turn on : 26.1649

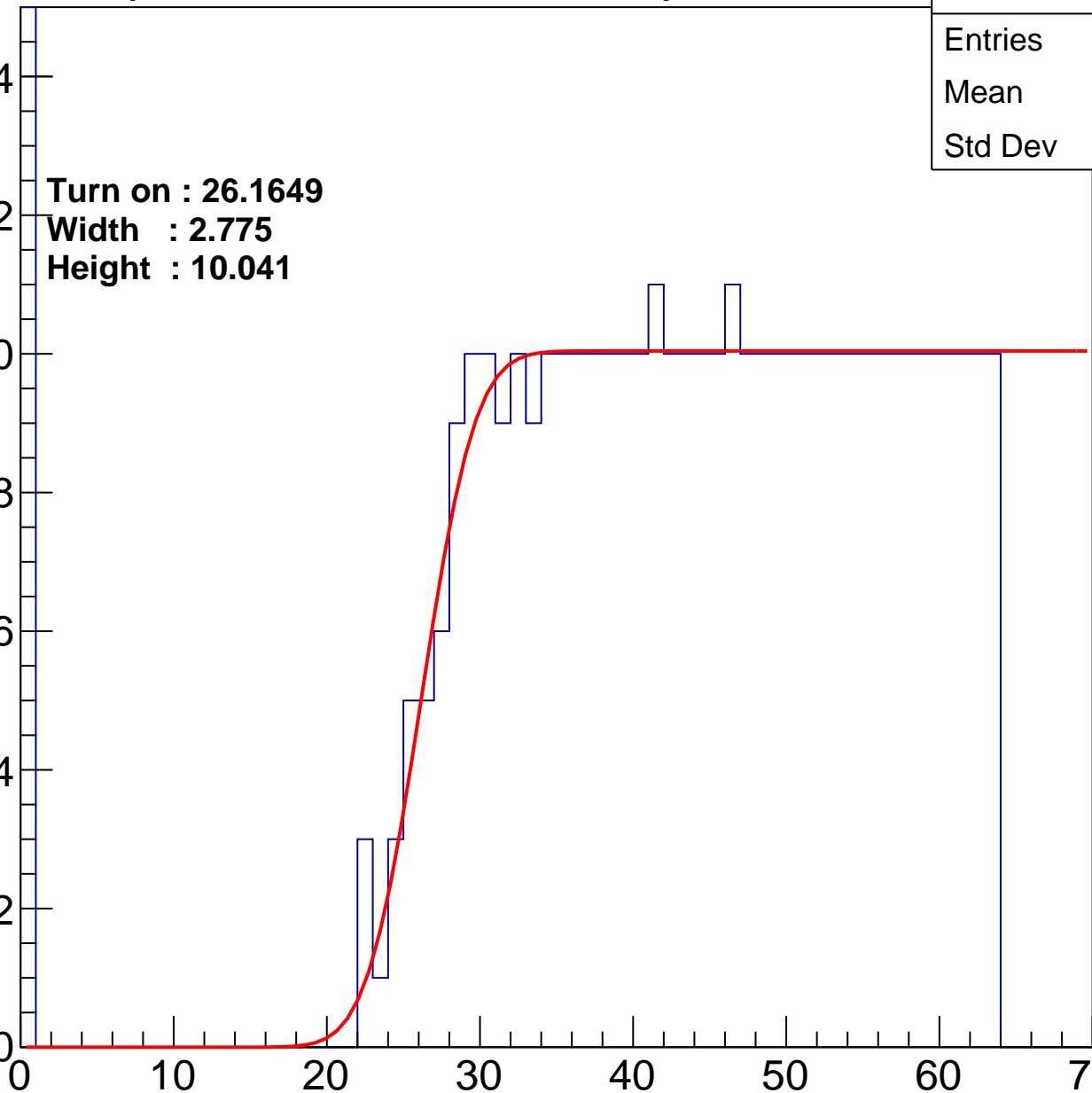
Width : 2.775

Height : 10.041

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U25-ch106

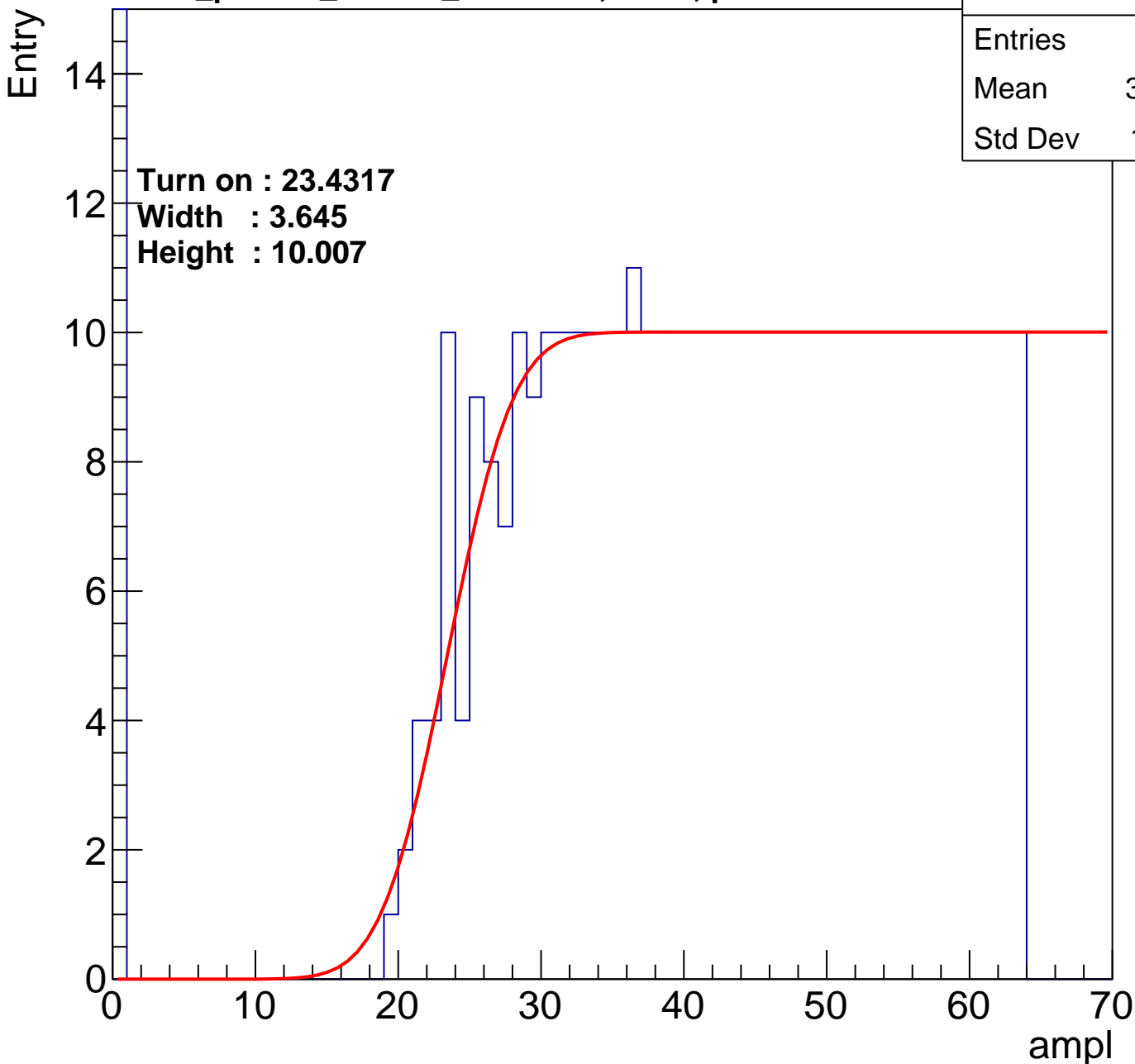
calib_packv5_041523_1651.root, FC#0, port C2

Entries	451
Mean	38.95
Std Dev	16.91

Turn on : 23.4317

Width : 3.645

Height : 10.007



B1L103S, U25-ch107

calib_packv5_041523_1651.root, FC#0, port C2

Entries	437
Mean	38.97
Std Dev	17.65

Turn on : 25.9847

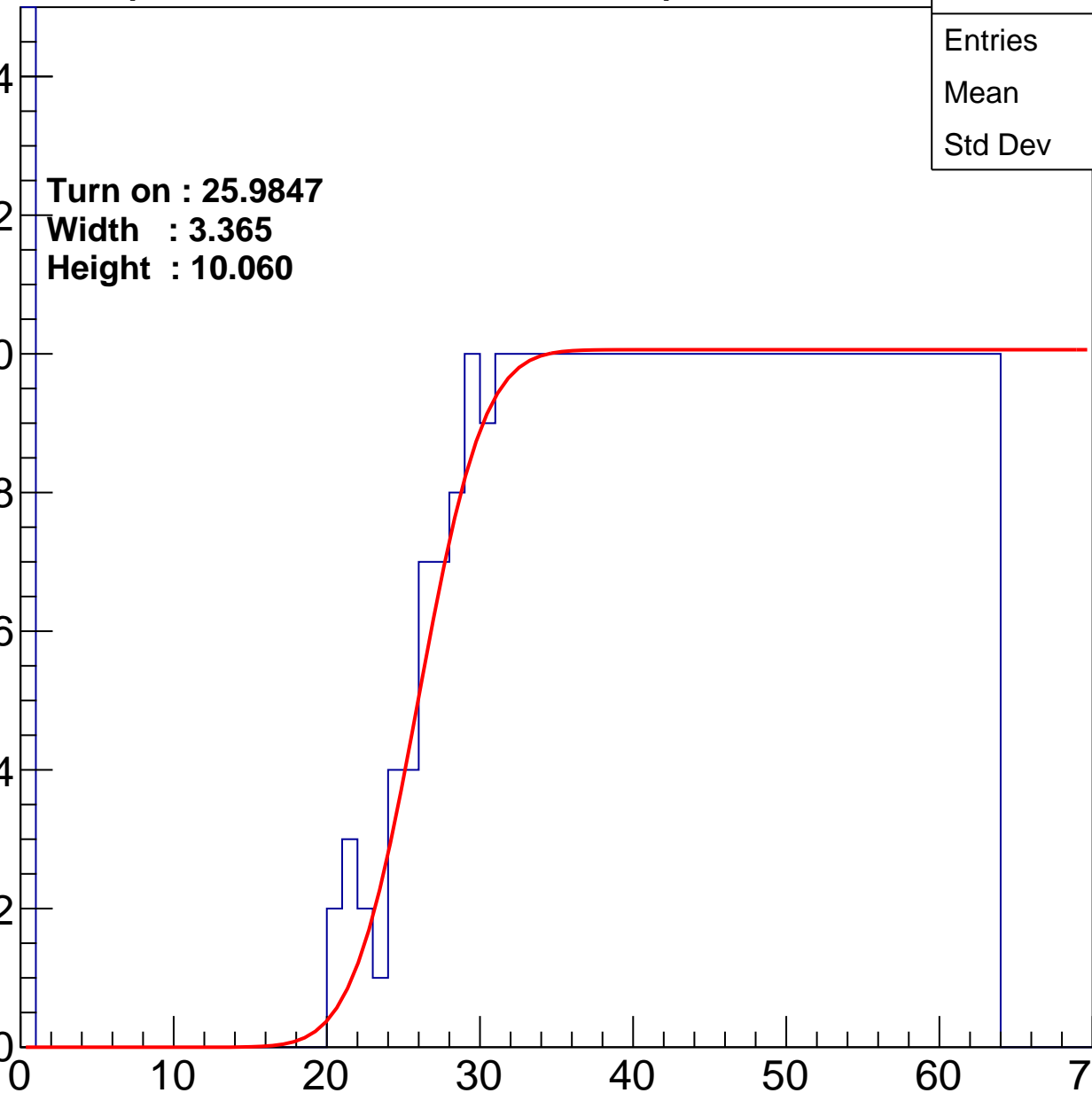
Width : 3.365

Height : 10.060

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U25-ch108

calib_packv5_041523_1651.root, FC#0, port C2

Entries	466
Mean	37.72
Std Dev	17.92

Turn on : 23.5086

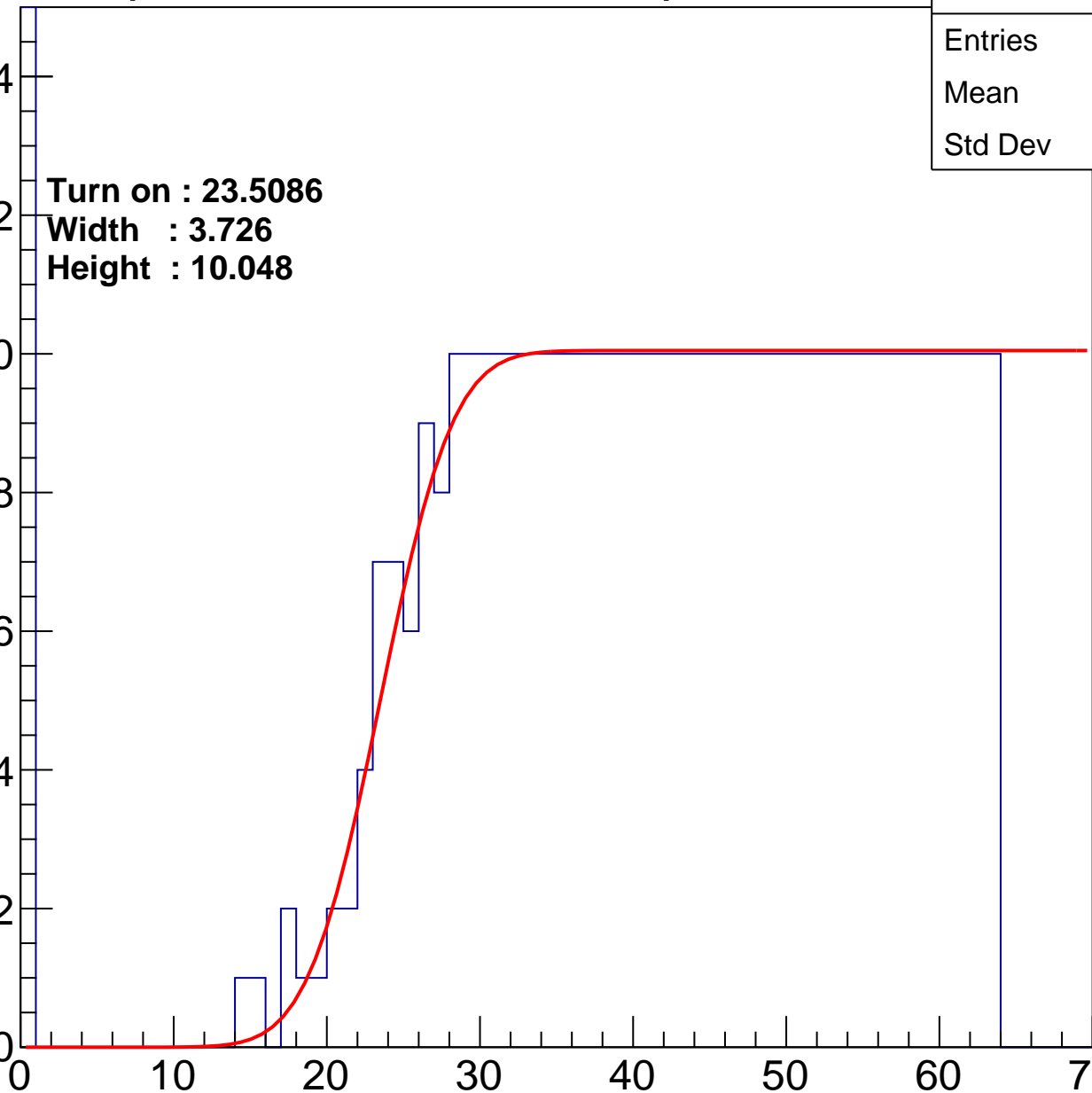
Width : 3.726

Height : 10.048

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U25-ch109

calib_packv5_041523_1651.root, FC#0, port C2

Entries	444
Mean	38.87
Std Dev	17.42

Turn on : 24.4954

Width : 3.388

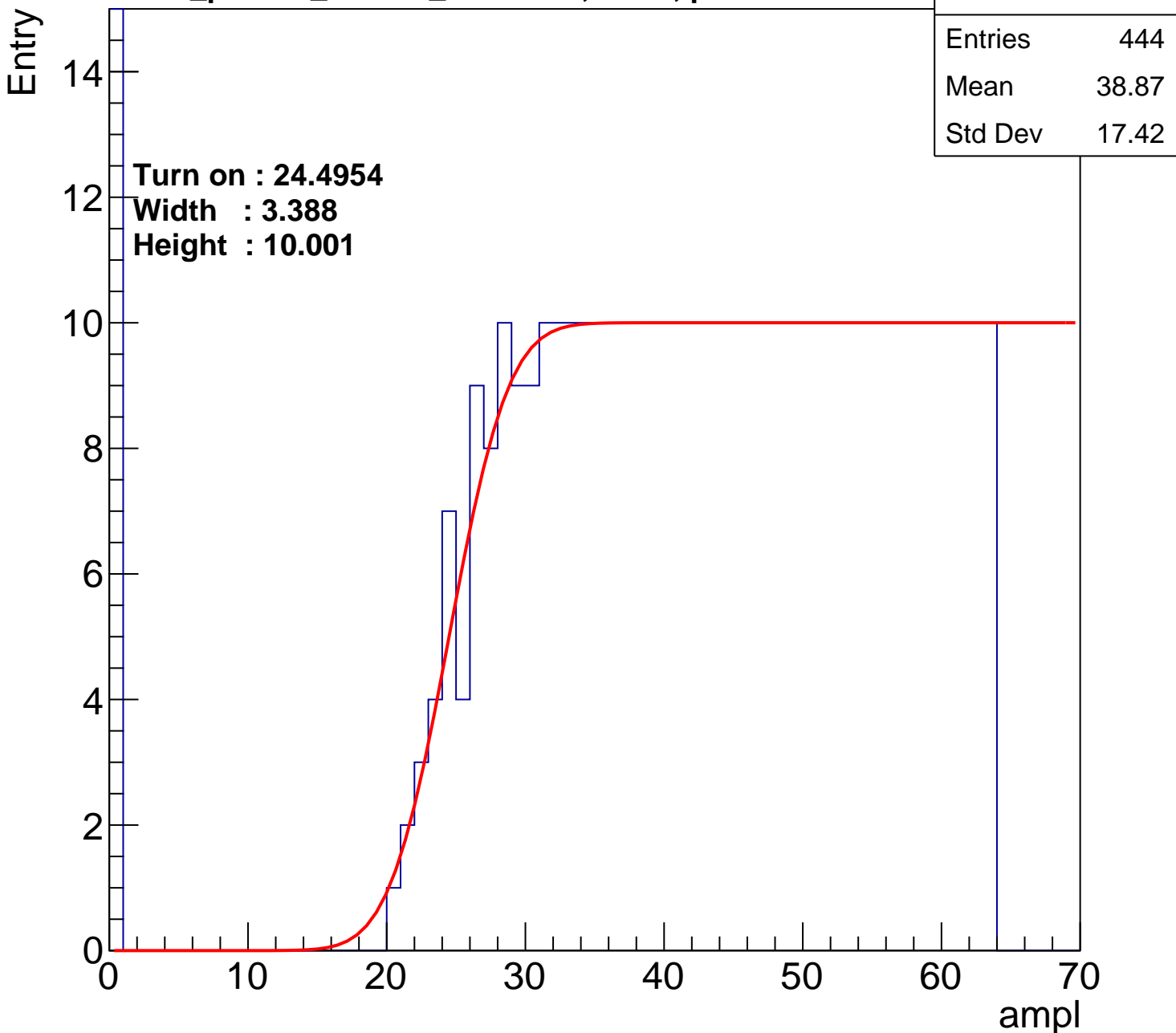
Height : 10.001

Entry

14
12
10
8
6
4
2
0

ampl

0 10 20 30 40 50 60 70



B1L103S, U25-ch110

calib_packv5_041523_1651.root, FC#0, port C2

Entries	474
Mean	37.85
Std Dev	17.35

Turn on : 21.0332

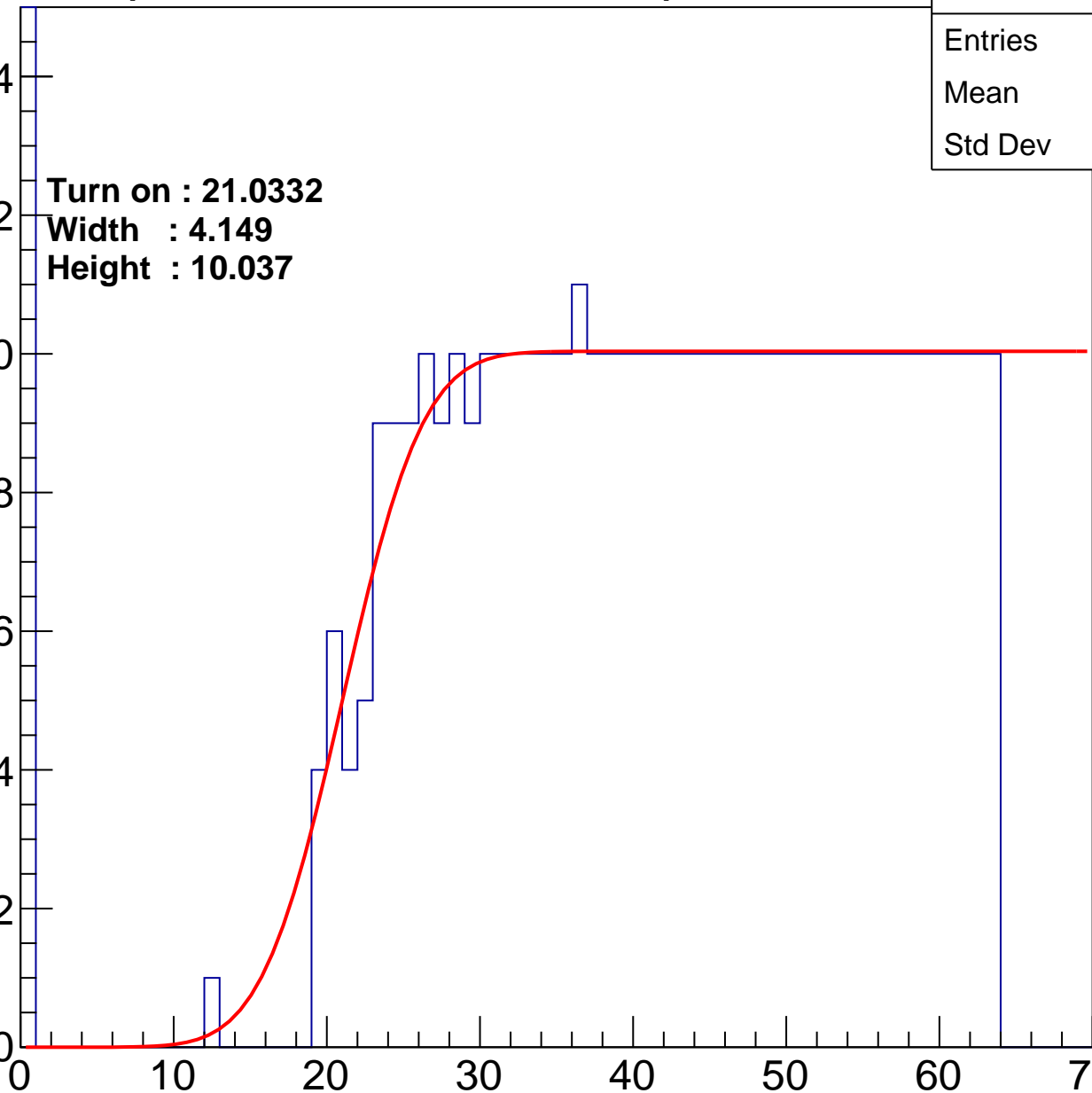
Width : 4.149

Height : 10.037

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U25-ch111

calib_packv5_041523_1651.root, FC#0, port C2

Entries	450
Mean	38.36
Std Dev	17.88

Turn on : 24.9399

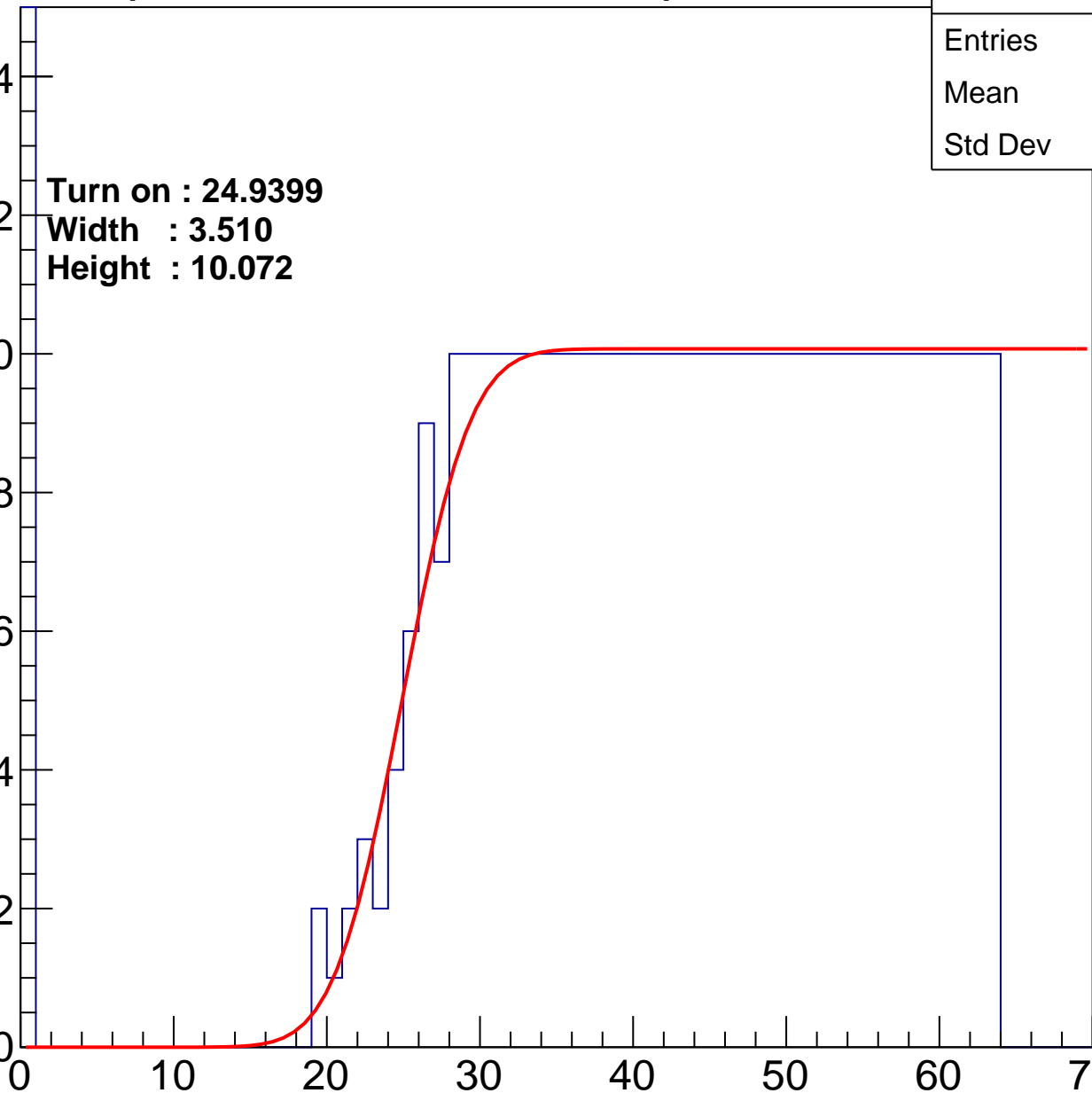
Width : 3.510

Height : 10.072

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U25-ch112

calib_packv5_041523_1651.root, FC#0, port C2

Entries	480
Mean	38.02
Std Dev	17.12

Turn on : 20.7313

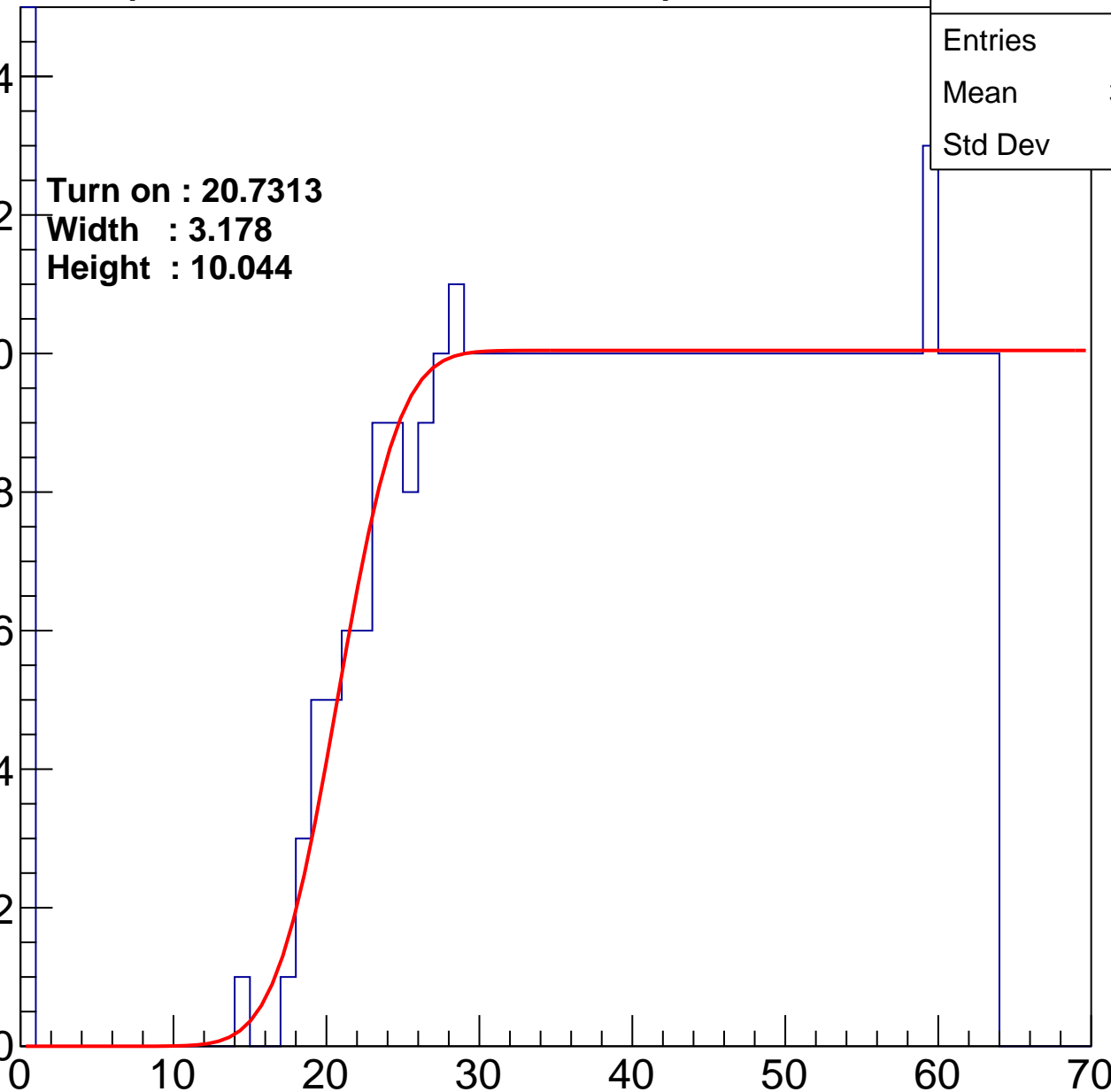
Width : 3.178

Height : 10.044

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U25-ch113

calib_packv5_041523_1651.root, FC#0, port C2

Entries	435
Mean	38.75
Std Dev	18.09

Turn on : 26.2783

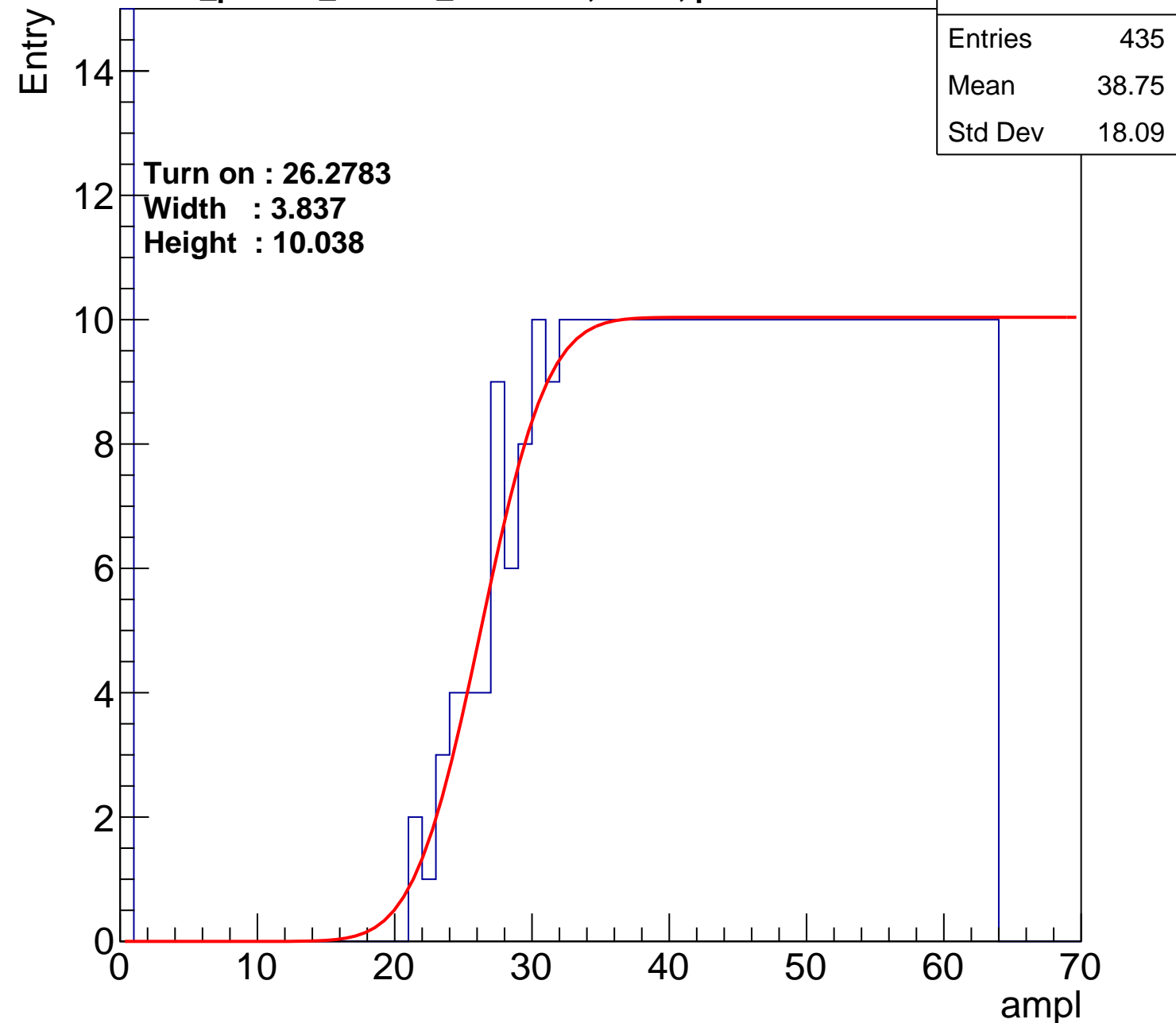
Width : 3.837

Height : 10.038

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U25-ch114

calib_packv5_041523_1651.root, FC#0, port C2

Entries	470
Mean	37.62
Std Dev	17.9

Turn on : 23.2918

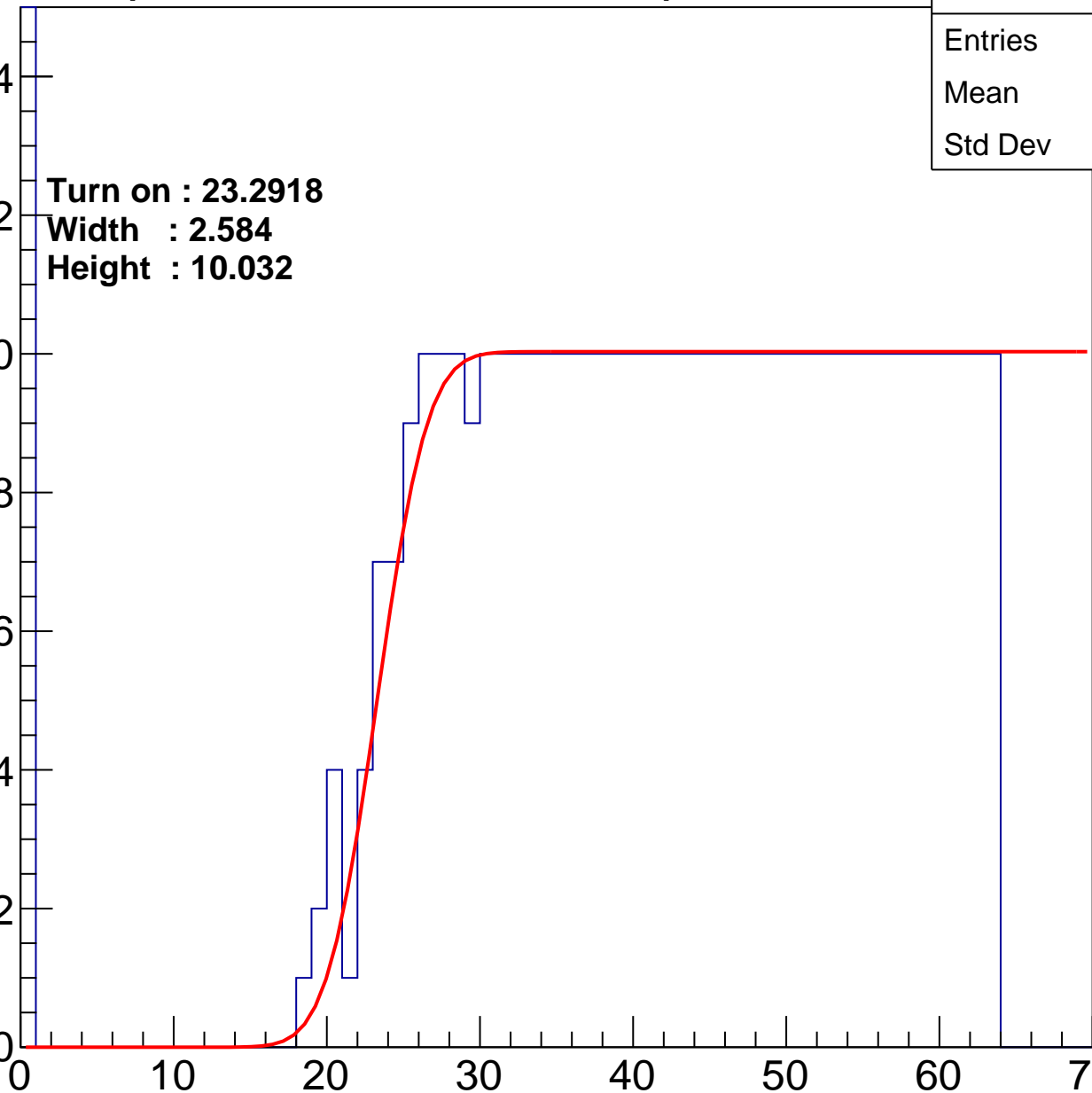
Width : 2.584

Height : 10.032

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U25-ch115

calib_packv5_041523_1651.root, FC#0, port C2

Entries	454
Mean	38.23
Std Dev	17.85

Turn on : 24.6081

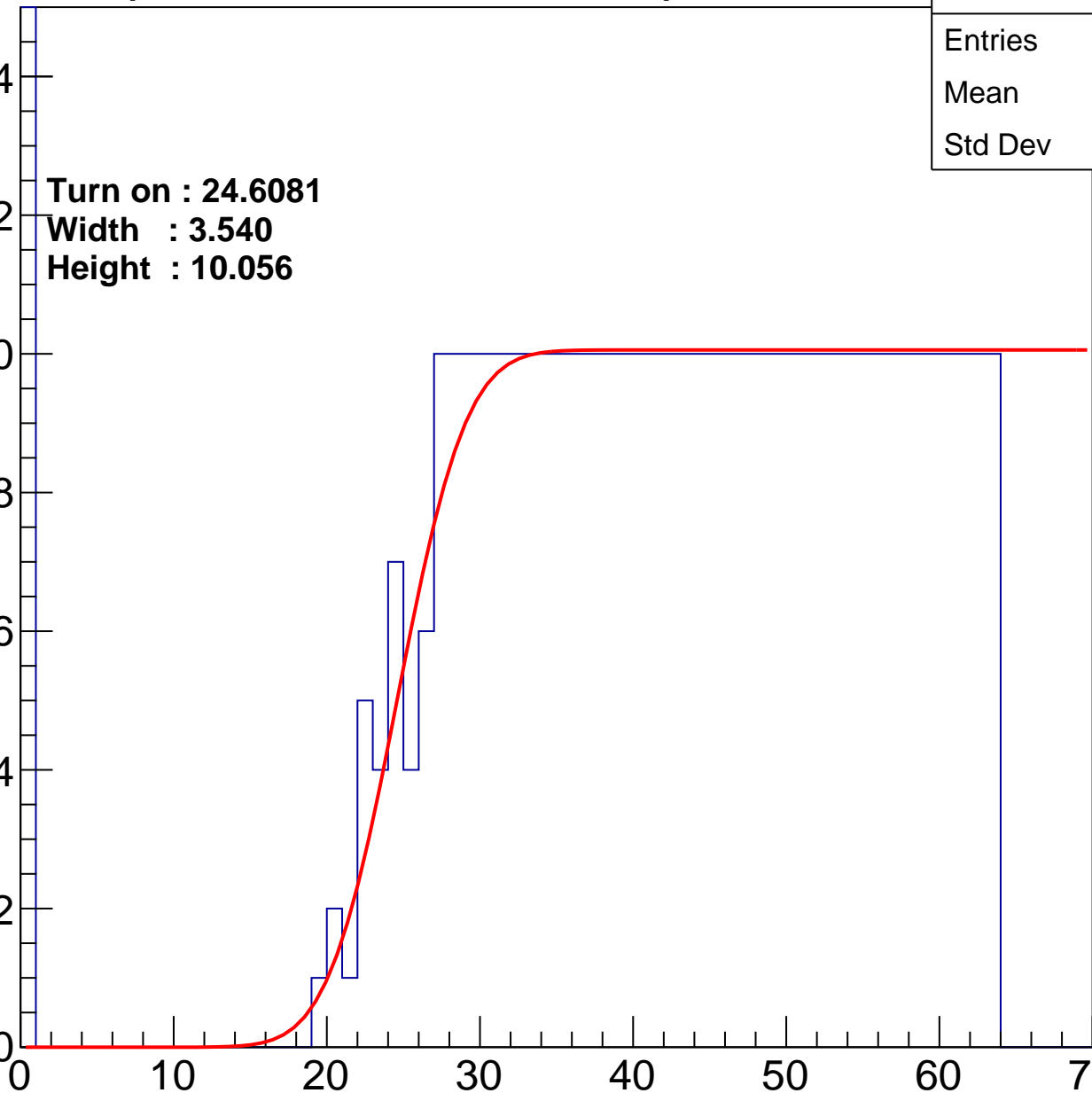
Width : 3.540

Height : 10.056

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U25-ch116

calib_packv5_041523_1651.root, FC#0, port C2

Entries	449
Mean	38.32
Std Dev	17.97

Turn on : 25.1833

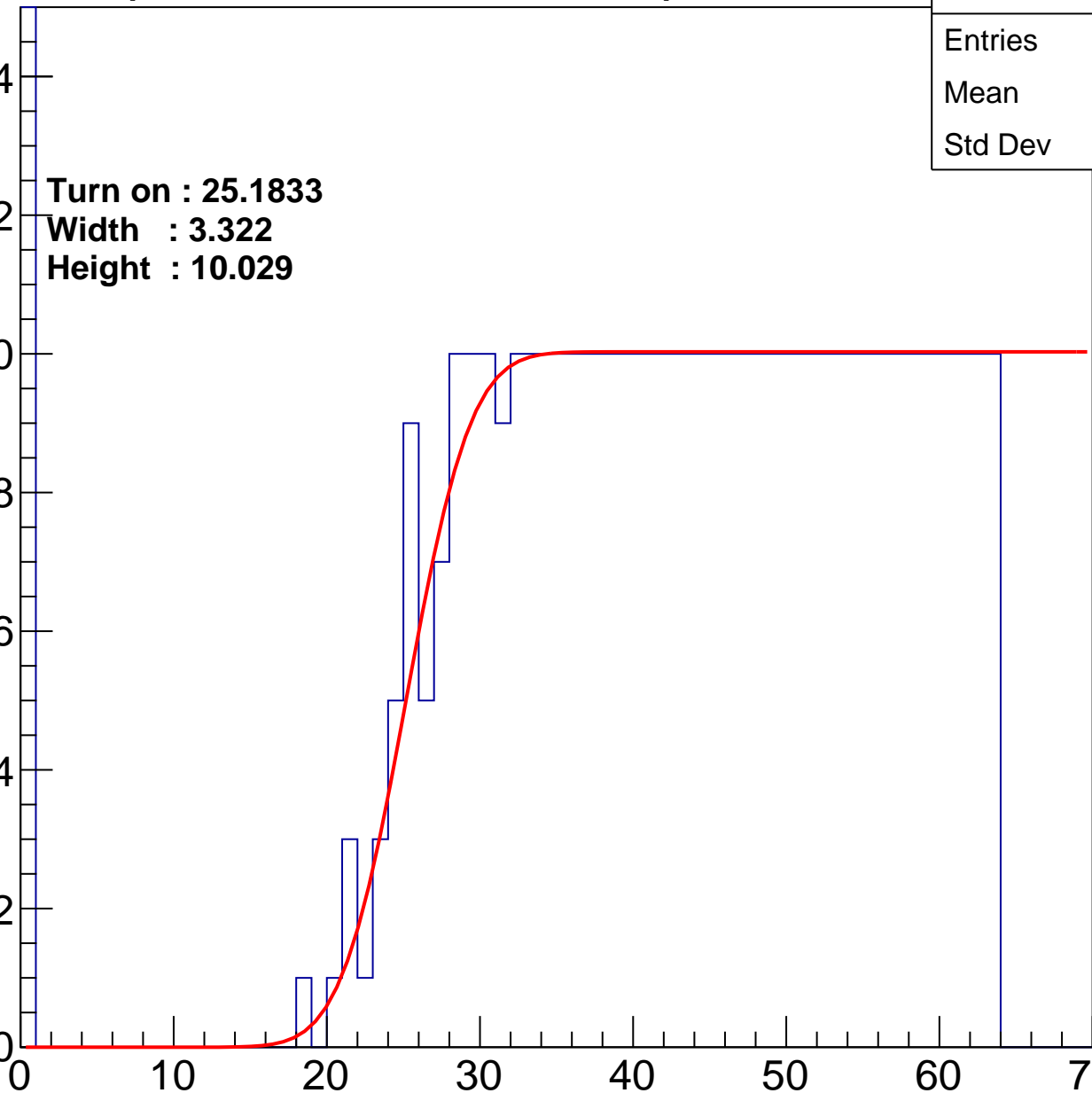
Width : 3.322

Height : 10.029

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U25-ch117

calib_packv5_041523_1651.root, FC#0, port C2

Entries	435
Mean	39.17
Std Dev	17.48

Turn on : 25.3150

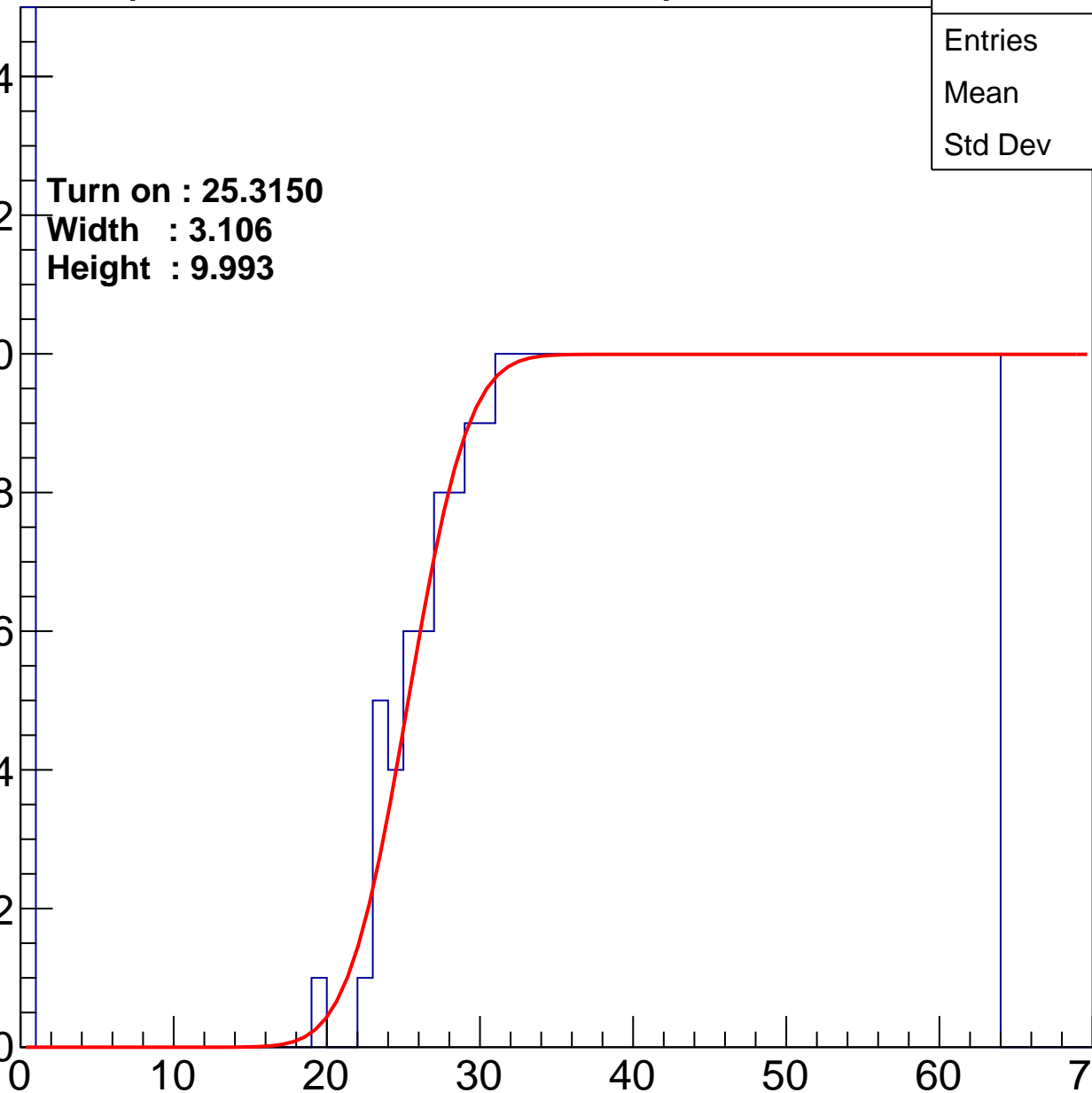
Width : 3.106

Height : 9.993

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U25-ch118

calib_packv5_041523_1651.root, FC#0, port C2

Entries	445
Mean	39.3
Std Dev	16.63

Turn on : 22.7411

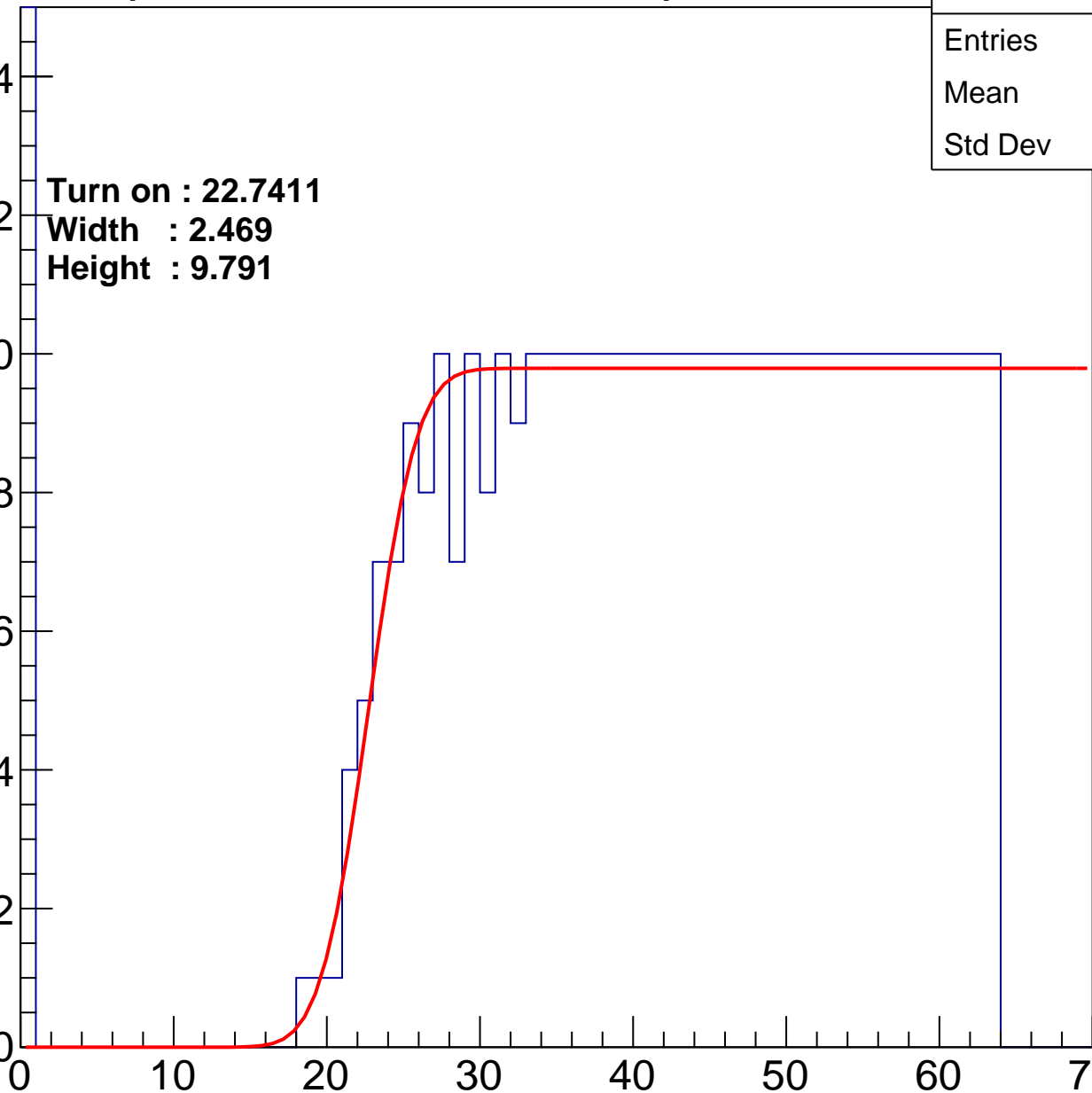
Width : 2.469

Height : 9.791

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U25-ch119

calib_packv5_041523_1651.root, FC#0, port C2

Entries	431
Mean	38.82
Std Dev	18.2

Turn on : 26.7446

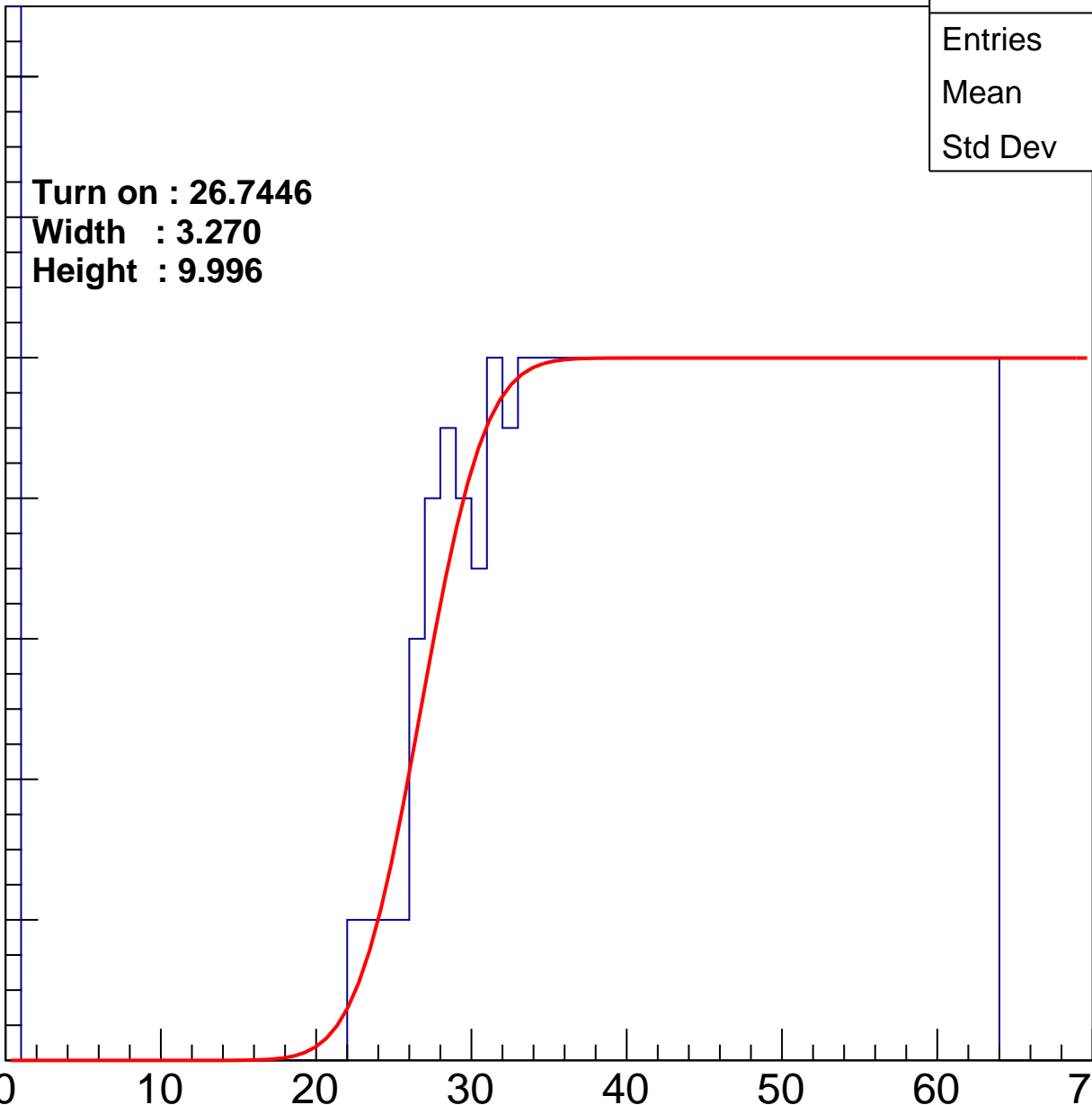
Width : 3.270

Height : 9.996

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U25-ch120

calib_packv5_041523_1651.root, FC#0, port C2

Entries	453
Mean	38.23
Std Dev	17.88

Turn on : 24.3877

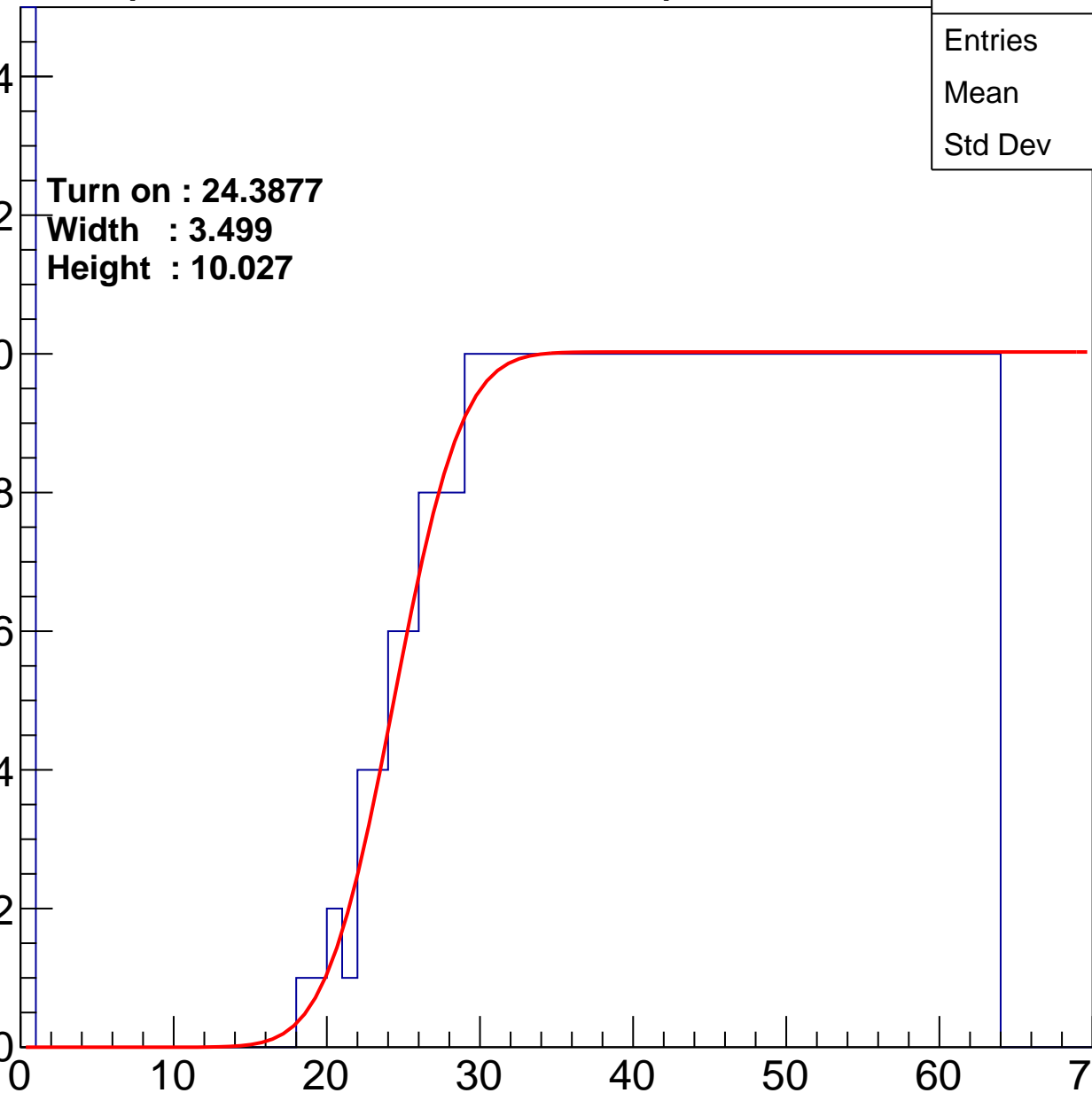
Width : 3.499

Height : 10.027

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U25-ch121

calib_packv5_041523_1651.root, FC#0, port C2

Entries	432
Mean	39.35
Std Dev	17.39

Turn on : 25.6819

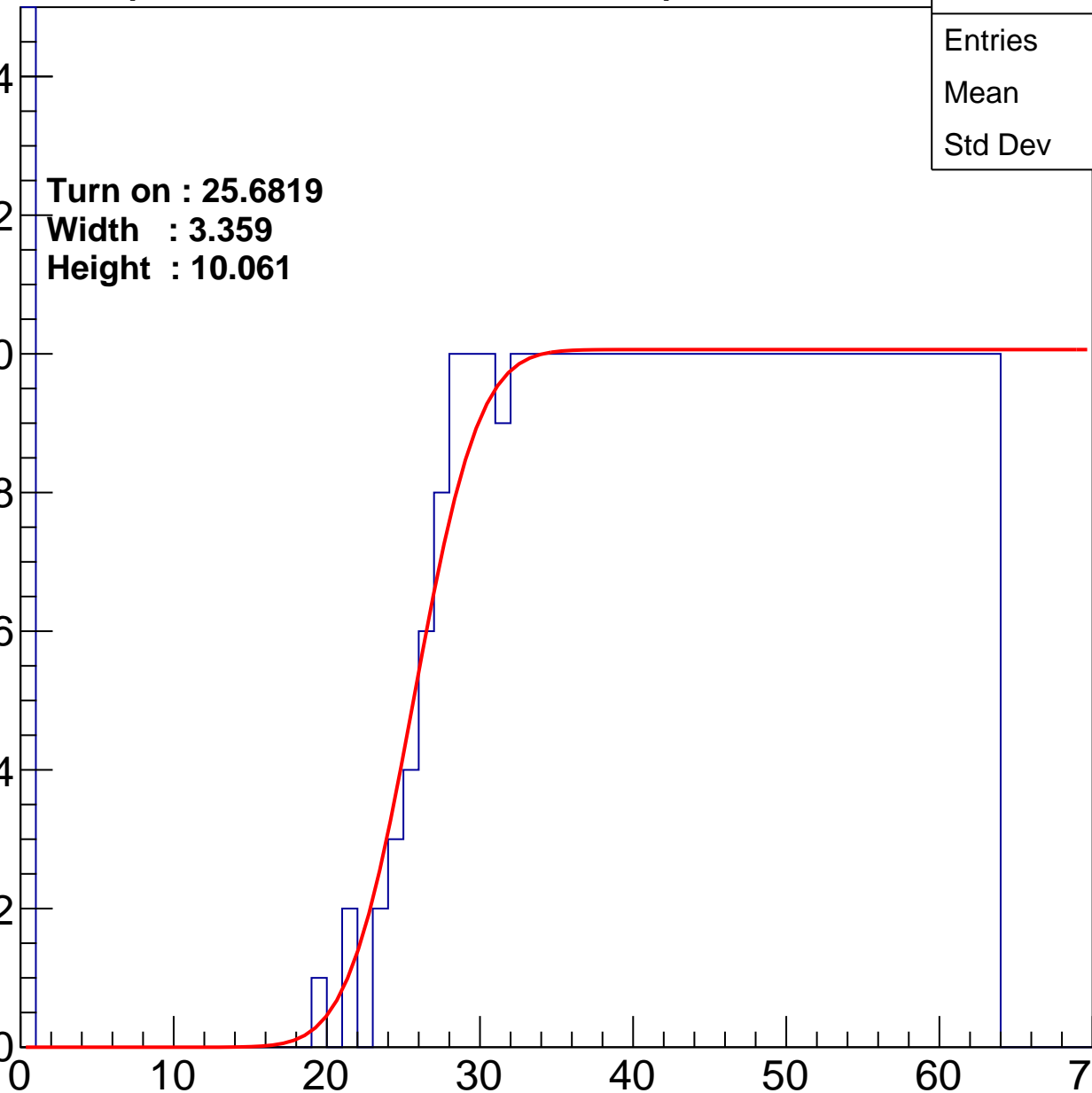
Width : 3.359

Height : 10.061

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U25-ch122

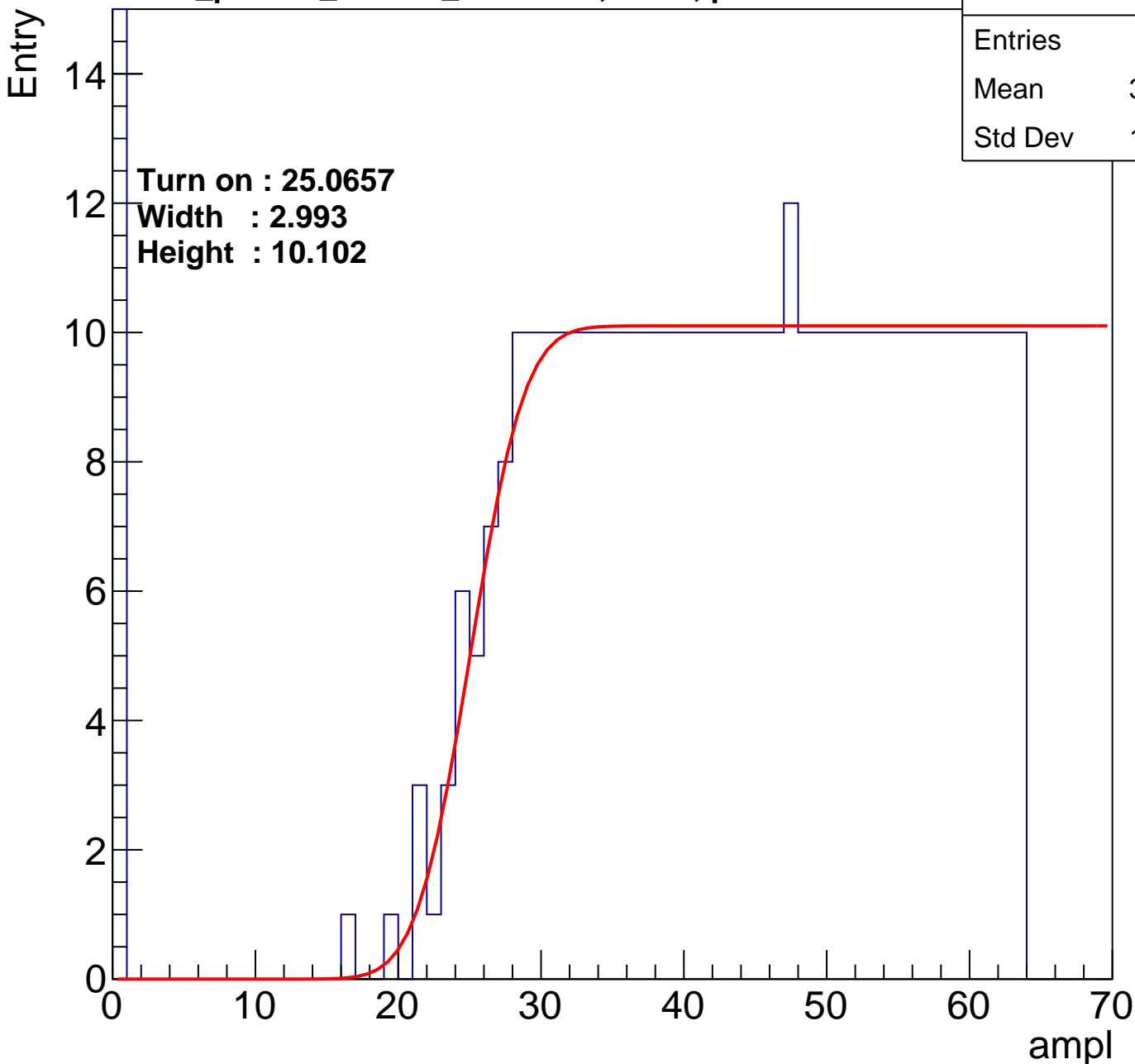
calib_packv5_041523_1651.root, FC#0, port C2

Entries	454
Mean	38.17
Std Dev	18.07

Turn on : 25.0657

Width : 2.993

Height : 10.102



B1L103S, U25-ch123

calib_packv5_041523_1651.root, FC#0, port C2

Entries	406
Mean	40.44
Std Dev	17.2

Turn on : 27.6529

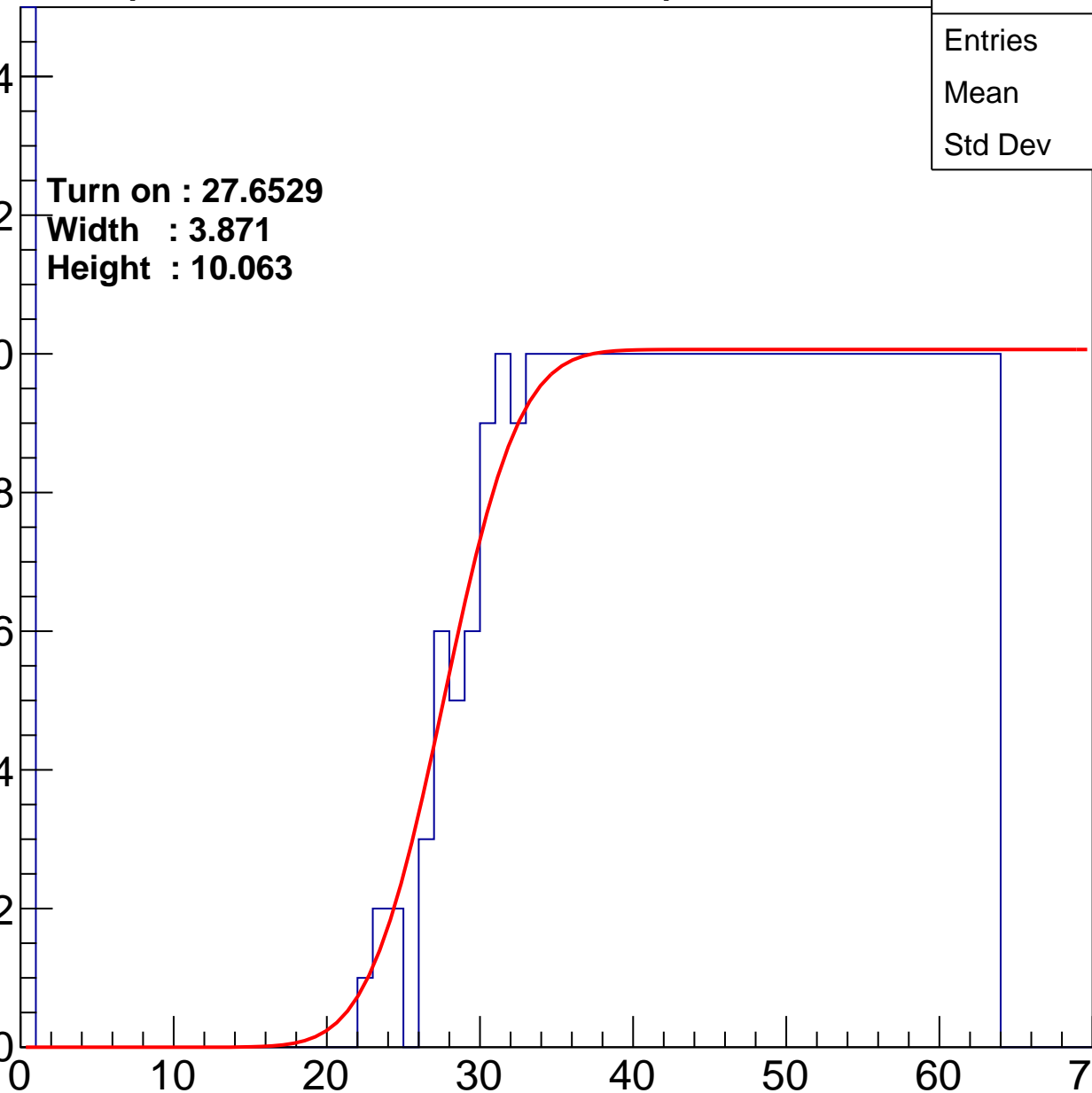
Width : 3.871

Height : 10.063

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U25-ch124

calib_packv5_041523_1651.root, FC#0, port C2

Entries	468
Mean	37.28
Std Dev	18.48

Turn on : 23.8912

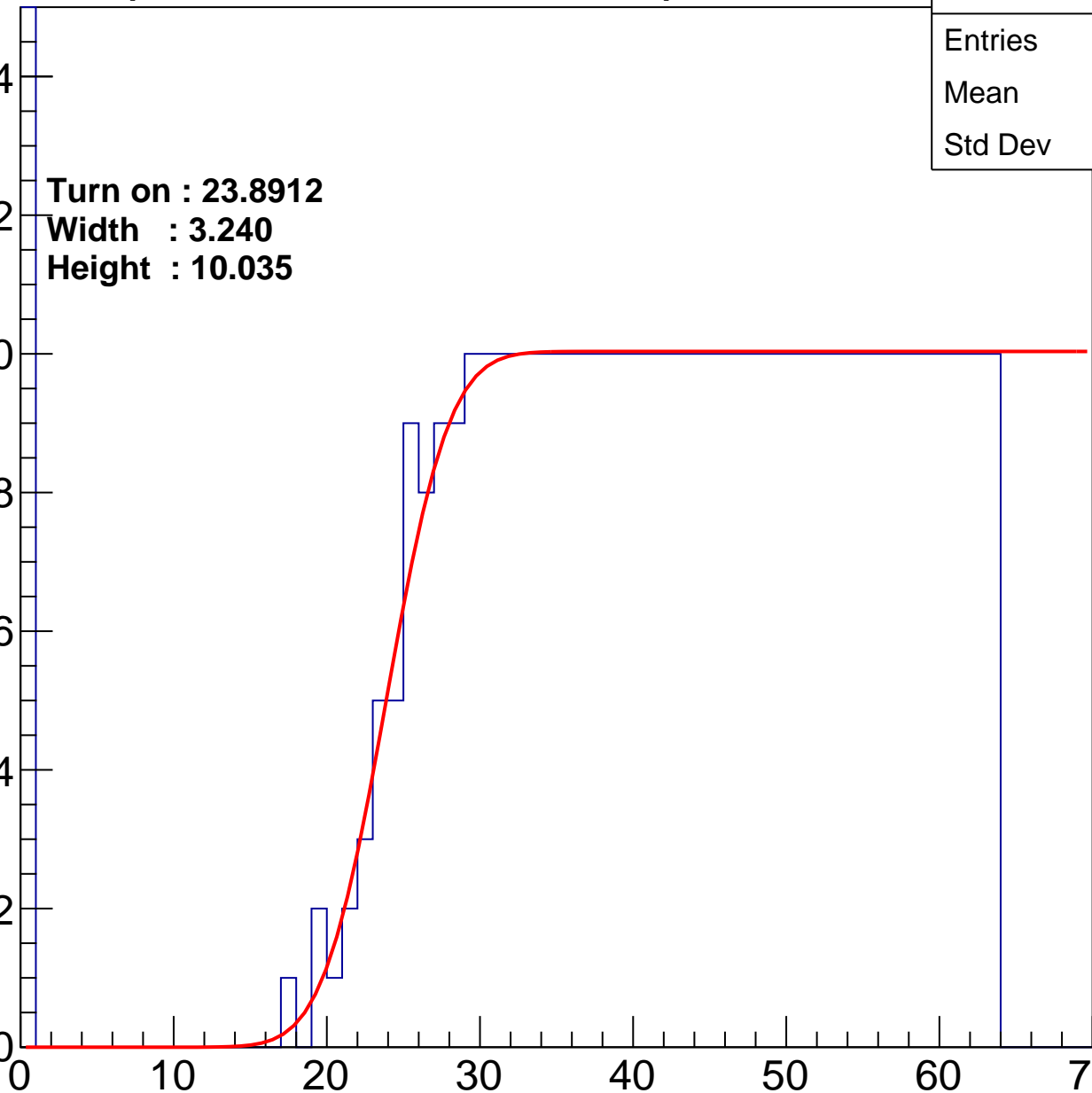
Width : 3.240

Height : 10.035

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U25-ch125

calib_packv5_041523_1651.root, FC#0, port C2

Entries	412
Mean	40.08
Std Dev	17.38

Turn on : 27.8766

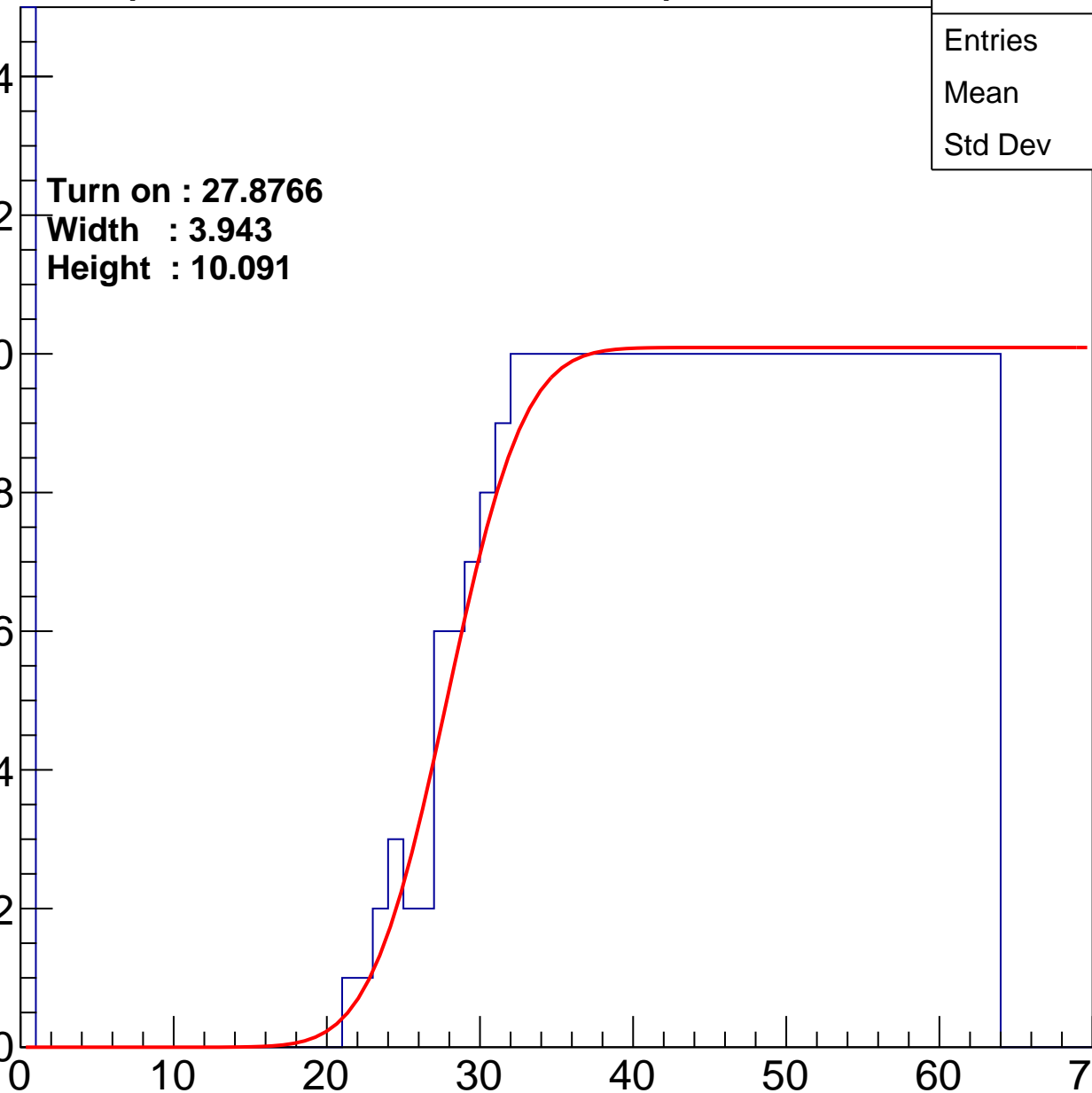
Width : 3.943

Height : 10.091

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U25-ch126

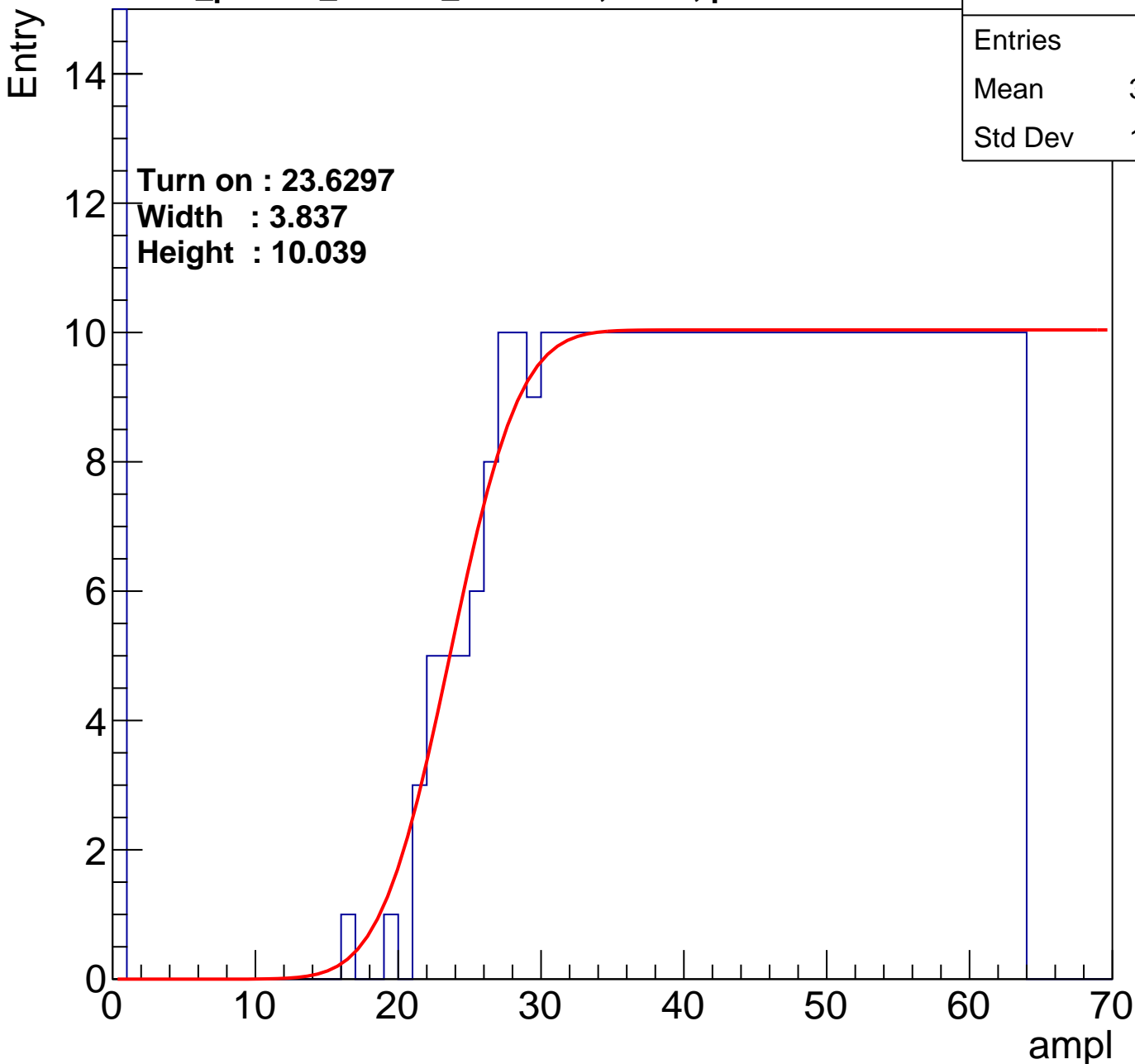
calib_packv5_041523_1651.root, FC#0, port C2

Entries	459
Mean	37.96
Std Dev	17.98

Turn on : 23.6297

Width : 3.837

Height : 10.039



B1L103S, U25-ch127

calib_packv5_041523_1651.root, FC#0, port C2

Entries	479
Mean	36.95
Std Dev	18.35

Turn on : 22.4929

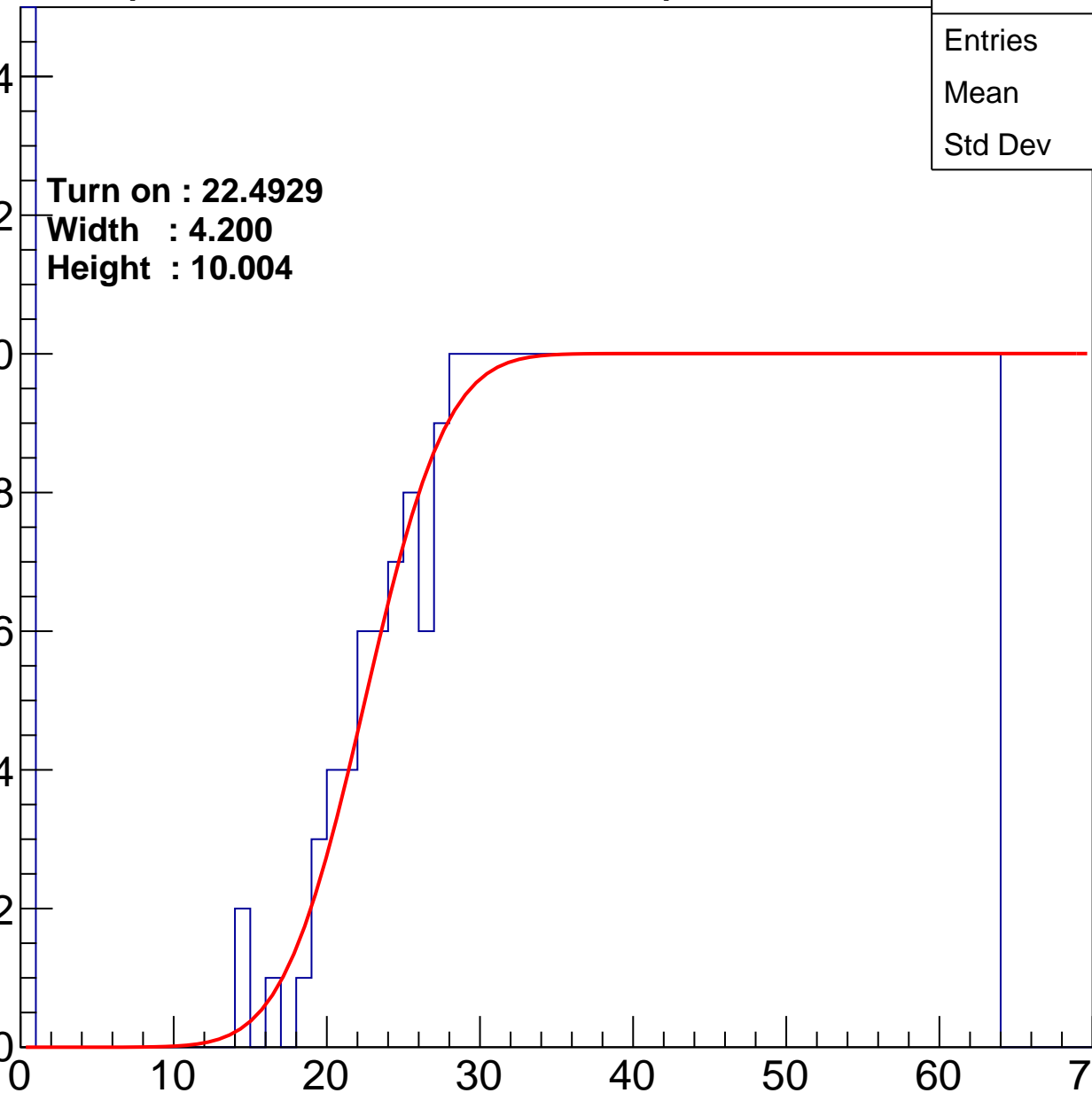
Width : 4.200

Height : 10.004

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U25-ch127

calib_packv5_041523_1651.root, FC#0, port C2

Entries	479
Mean	36.95
Std Dev	18.35

Turn on : 22.4929

Width : 4.200

Height : 10.004

Entry

14
12
10
8
6
4
2
0

ampl

