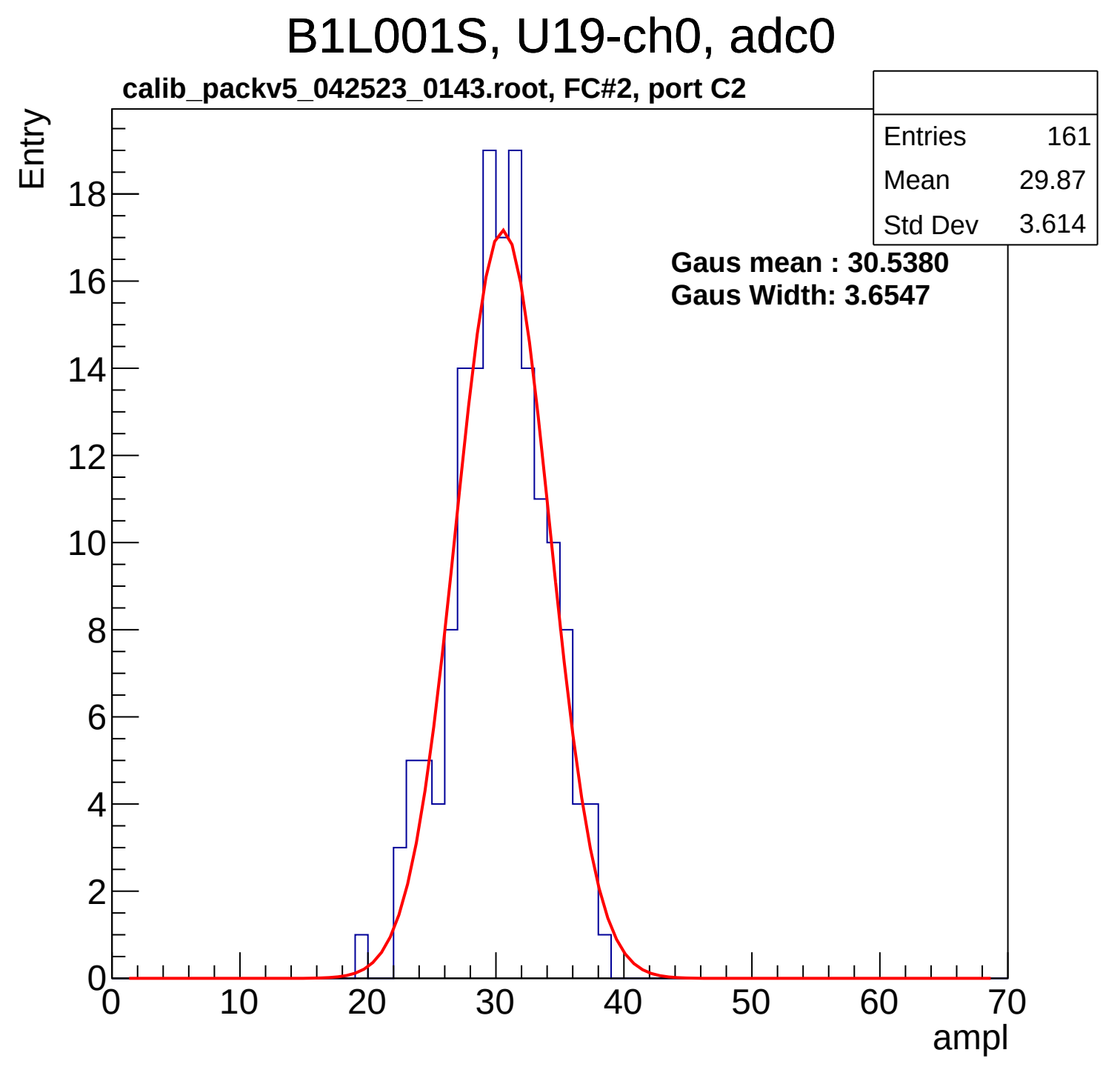
B1L001S, U19-ch0, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 161
Mean 29.87
Std Dev 3.614
Gaus mean : 30.5380
Gaus Width: 3.6547
Entry
ampl
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2
4
6
8
10
12
14
16
18
0
10
20
30
40
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60
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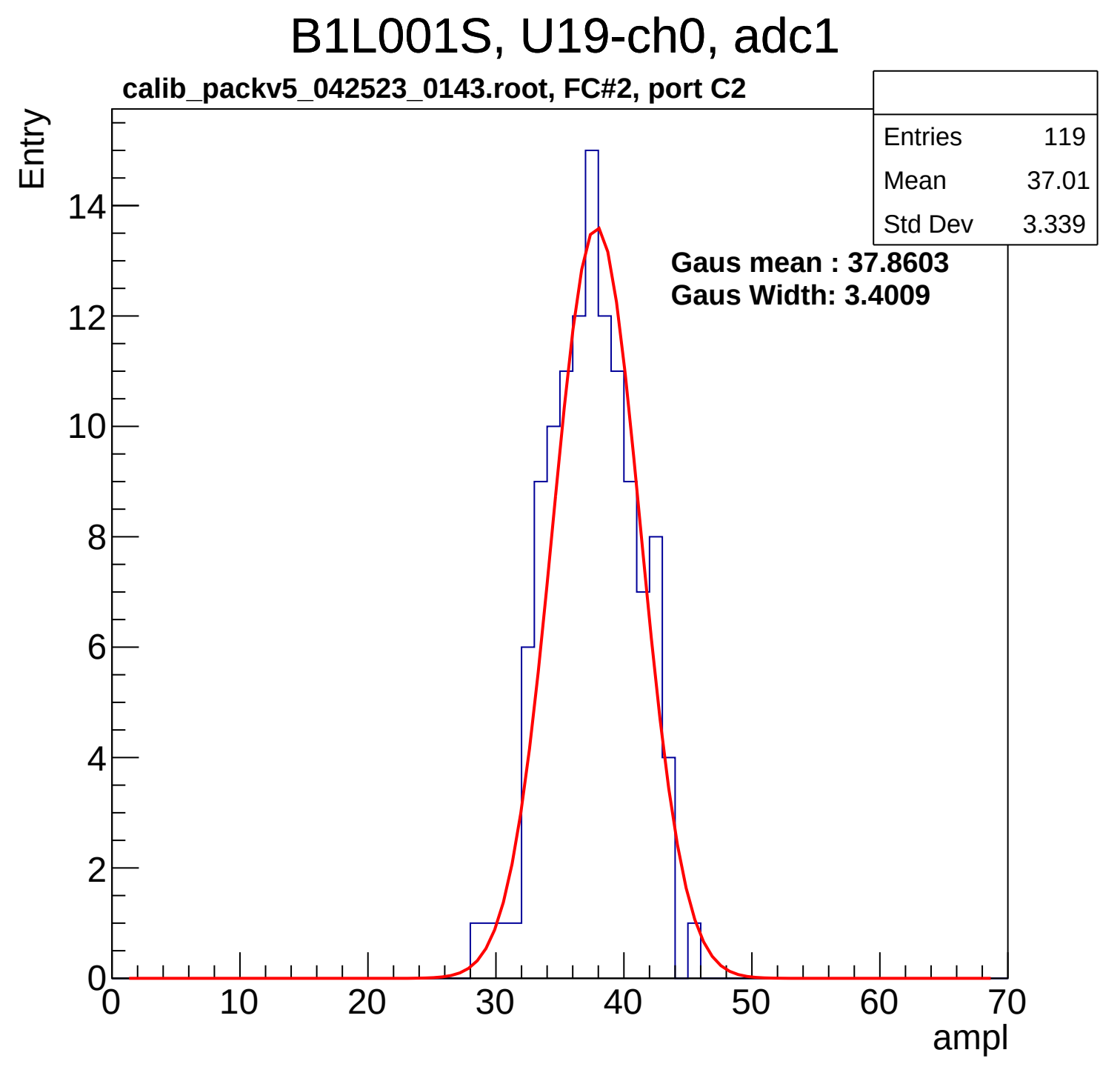
B1L001S, U19-ch0, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 119
Mean 37.01
Std Dev 3.339
Gaus mean : 37.8603
Gaus Width: 3.4009
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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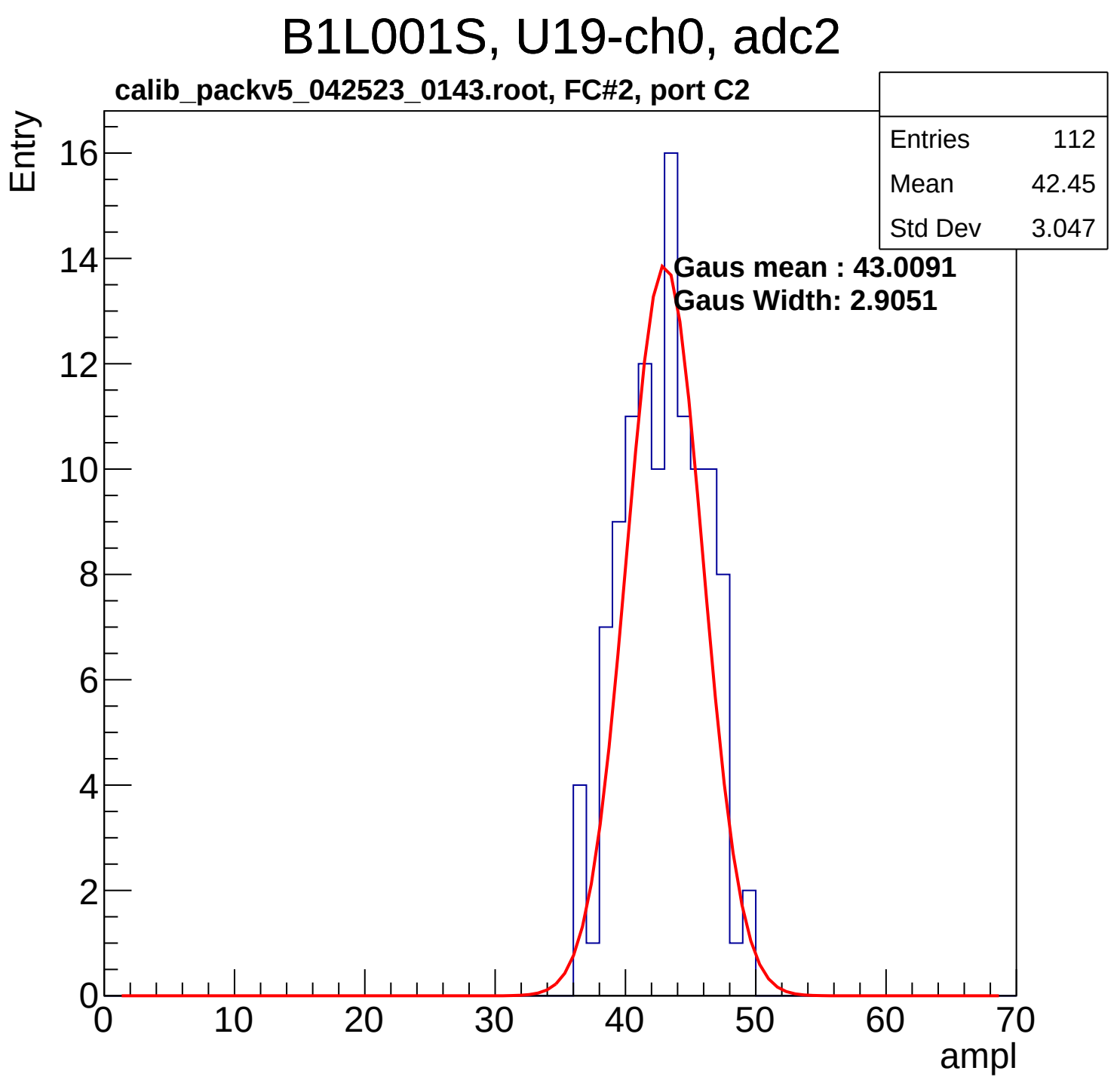
B1L001S, U19-ch0, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 112
Mean 42.45
Std Dev 3.047
Gaus mean : 43.0091
Gaus Width: 2.9051
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
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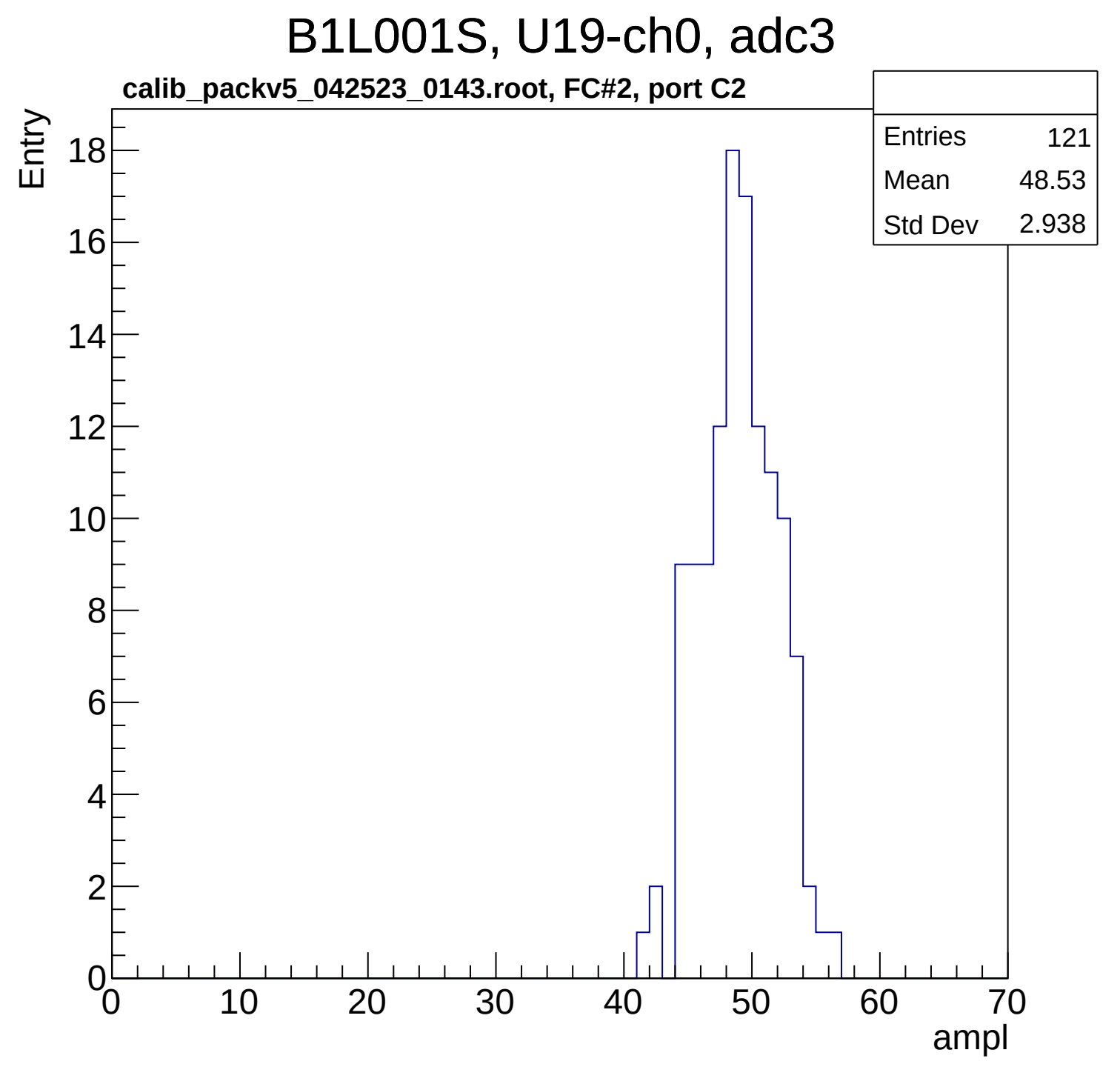
B1L001S, U19-ch0, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 121
Mean 48.53
Std Dev 2.938
Entry
ampl
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2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
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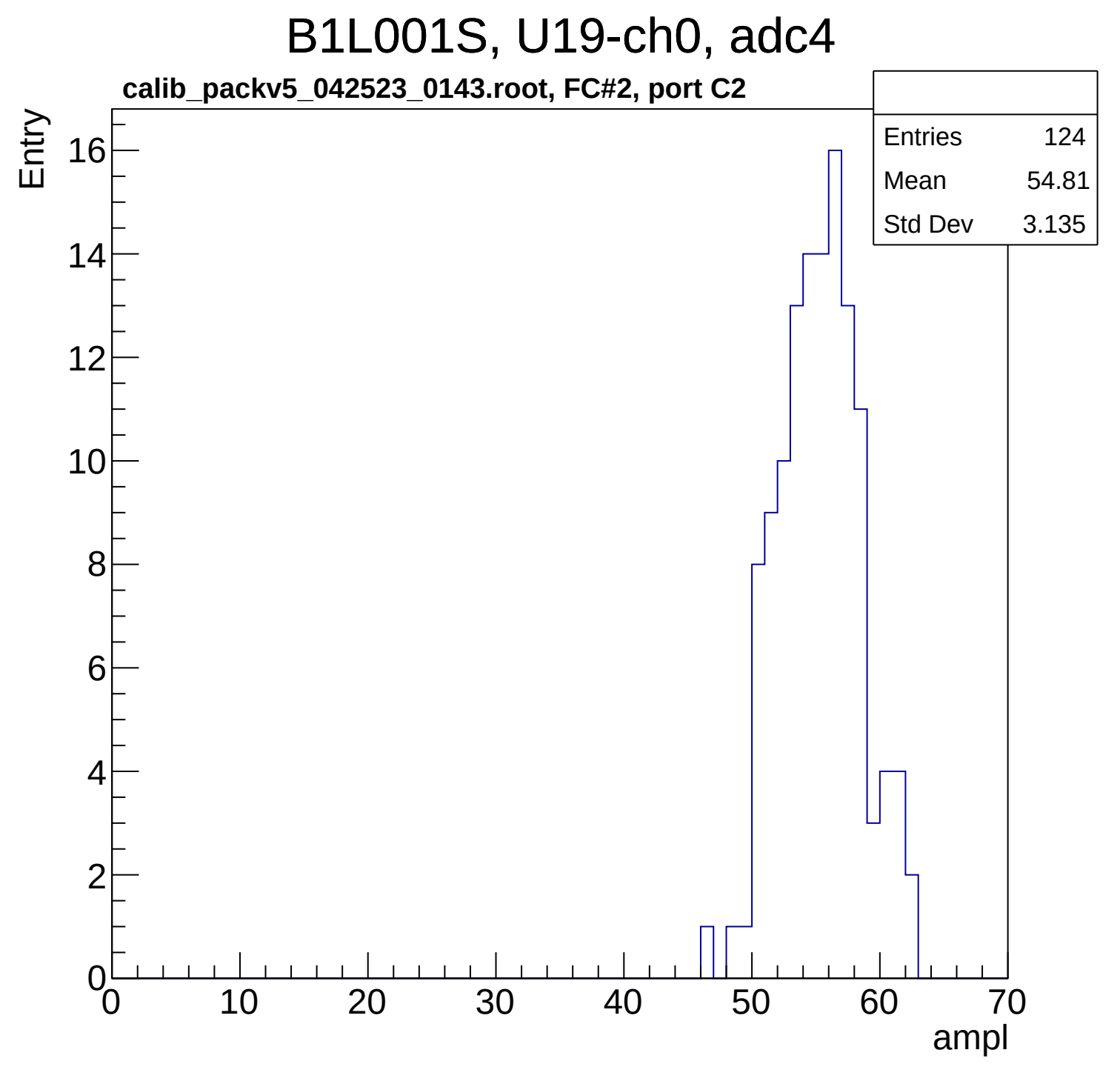
B1L001S, U19-ch0, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 124
Mean 54.81
Std Dev 3.135
Entry
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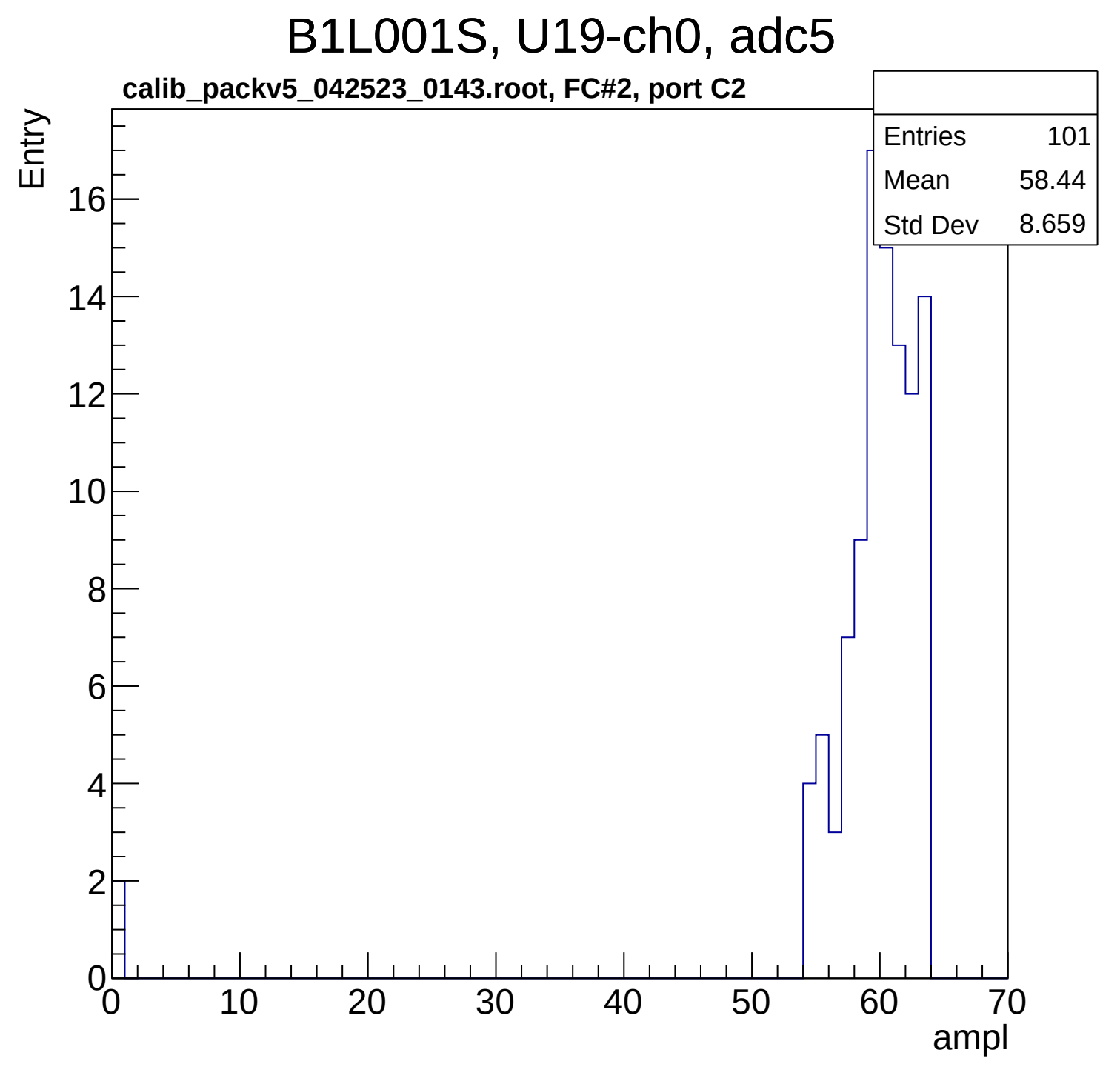
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch0, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 101
Mean 58.44
Std Dev 8.659
Entry
ampl
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2
4
6
8
10
12
14
16
0
10
20
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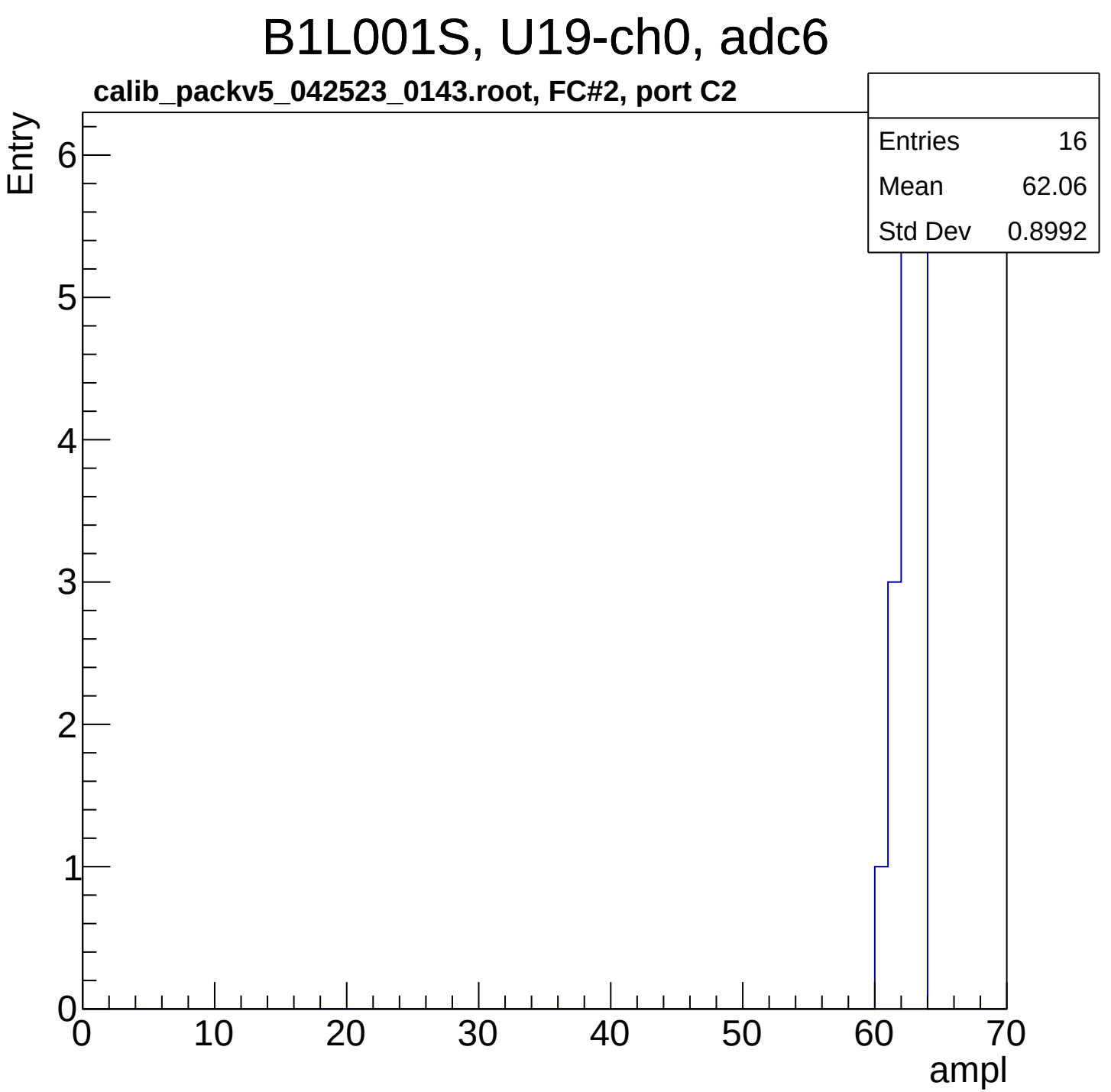
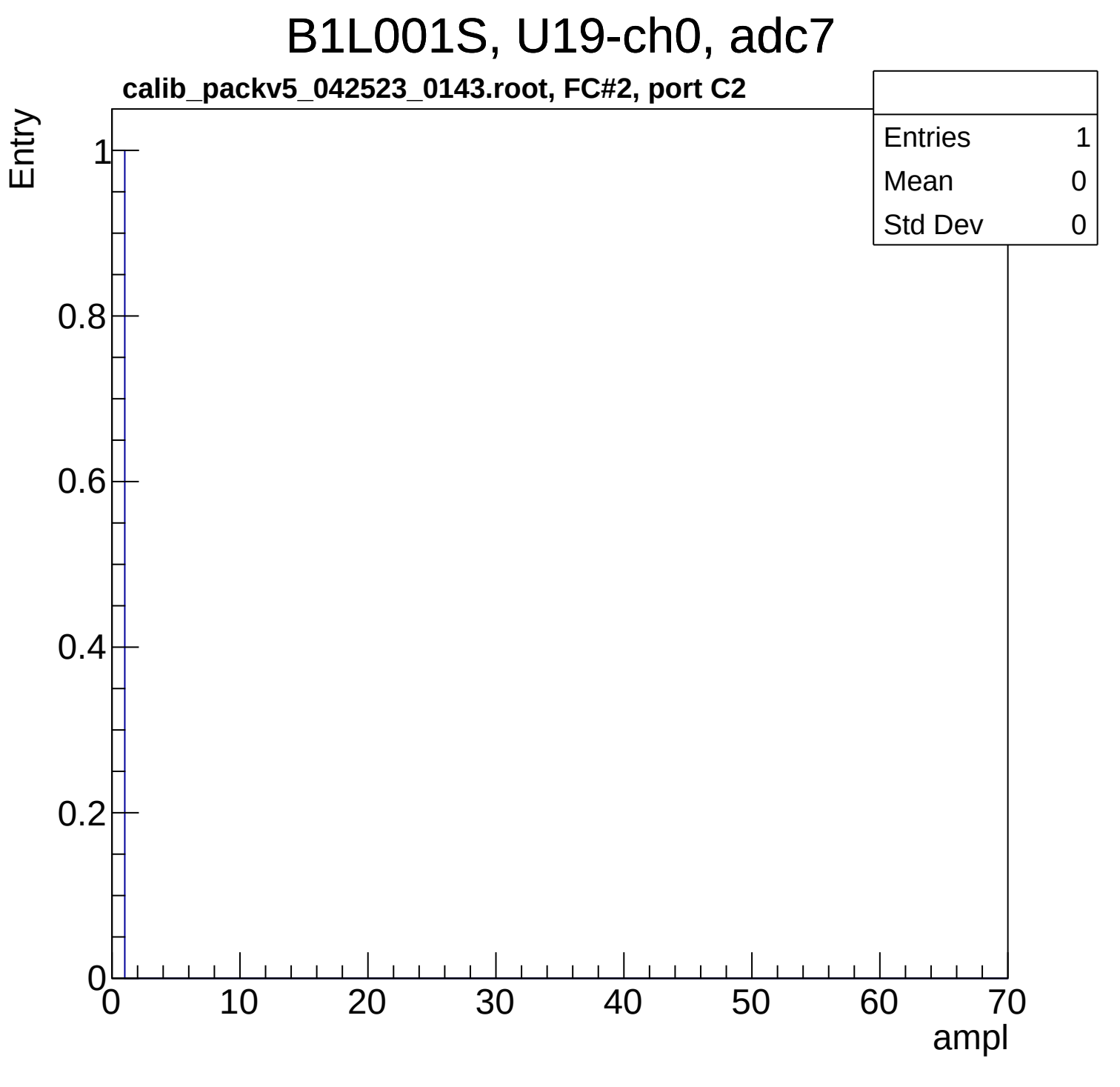
40
50
60
70


B1L001S, U19-ch0, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 16
Mean 62.06
Std Dev 0.8992
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch0, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 0
Std Dev 0
Entry
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0.6
0.4
0.2
0
0
10
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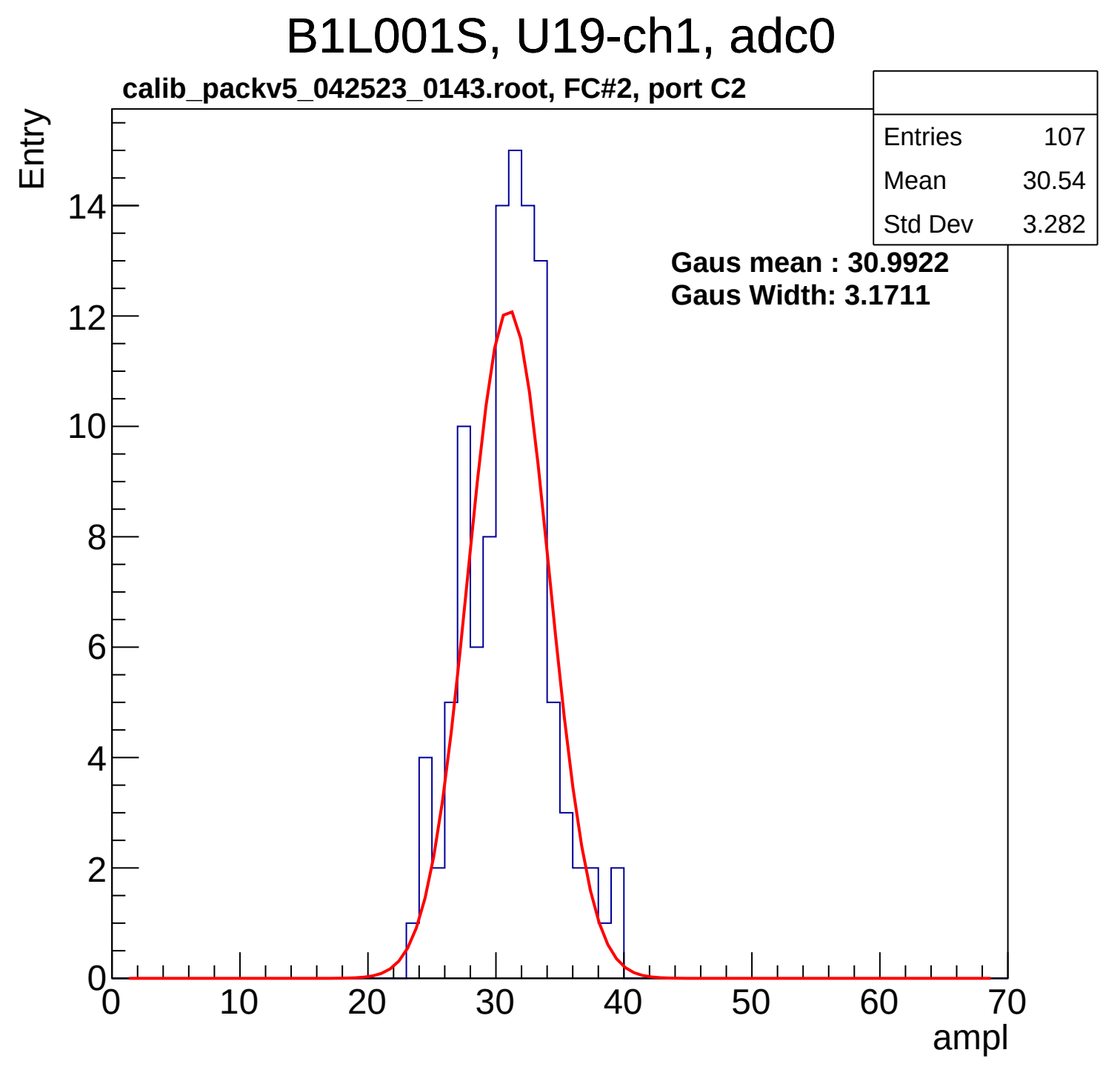
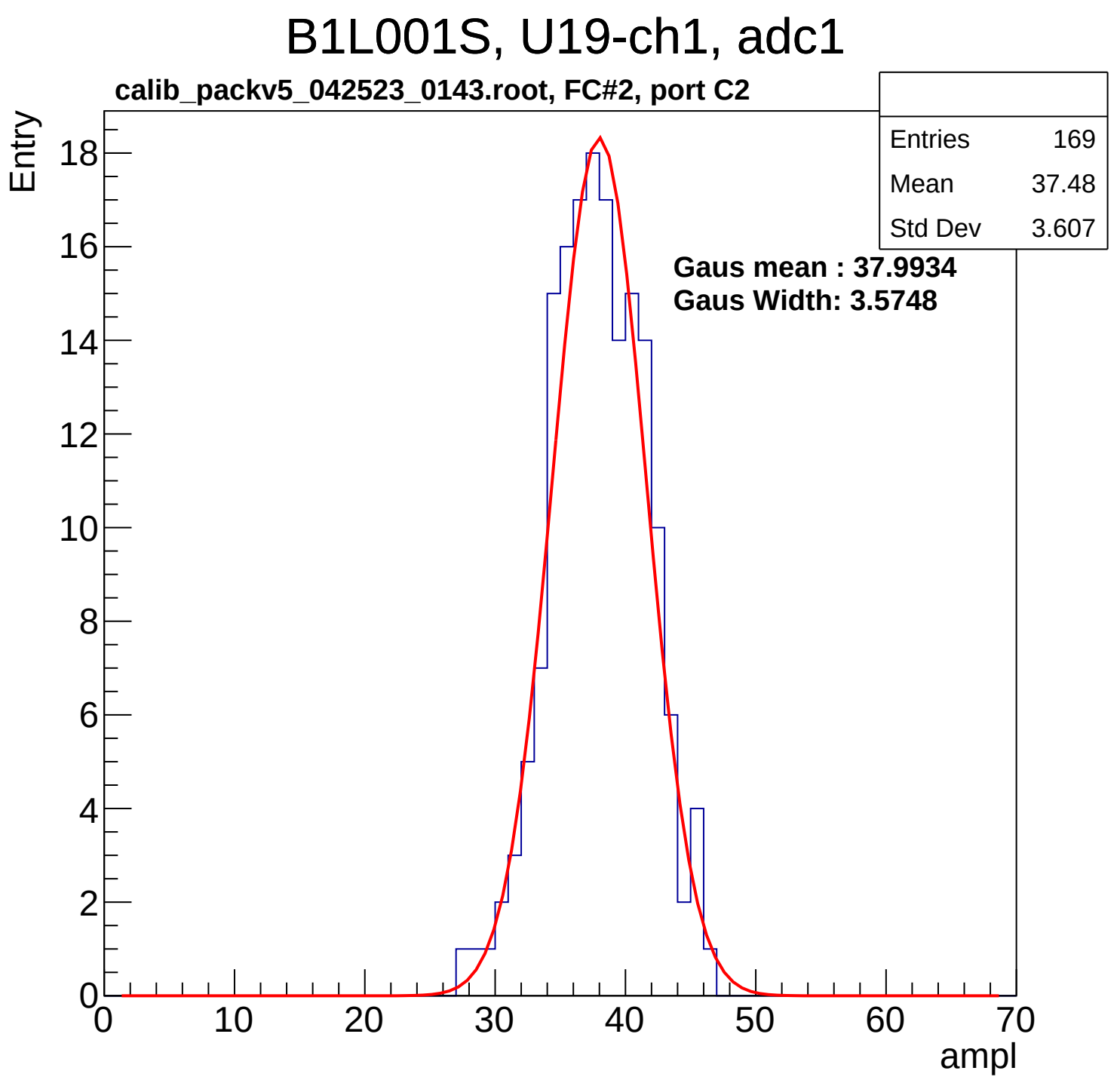
30
40
50
60
70
ampl


B1L001S, U19-ch1, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 107
Mean 30.54
Std Dev 3.282
Gaus mean : 30.9922
Gaus Width: 3.1711
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L001S, U19-ch1, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 169
Mean 37.48
Std Dev 3.607
Gaus mean : 37.9934
Gaus Width: 3.5748
Entry
ampl
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4
6
8
10
12
14
16
18
0
10
20
30
40
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60
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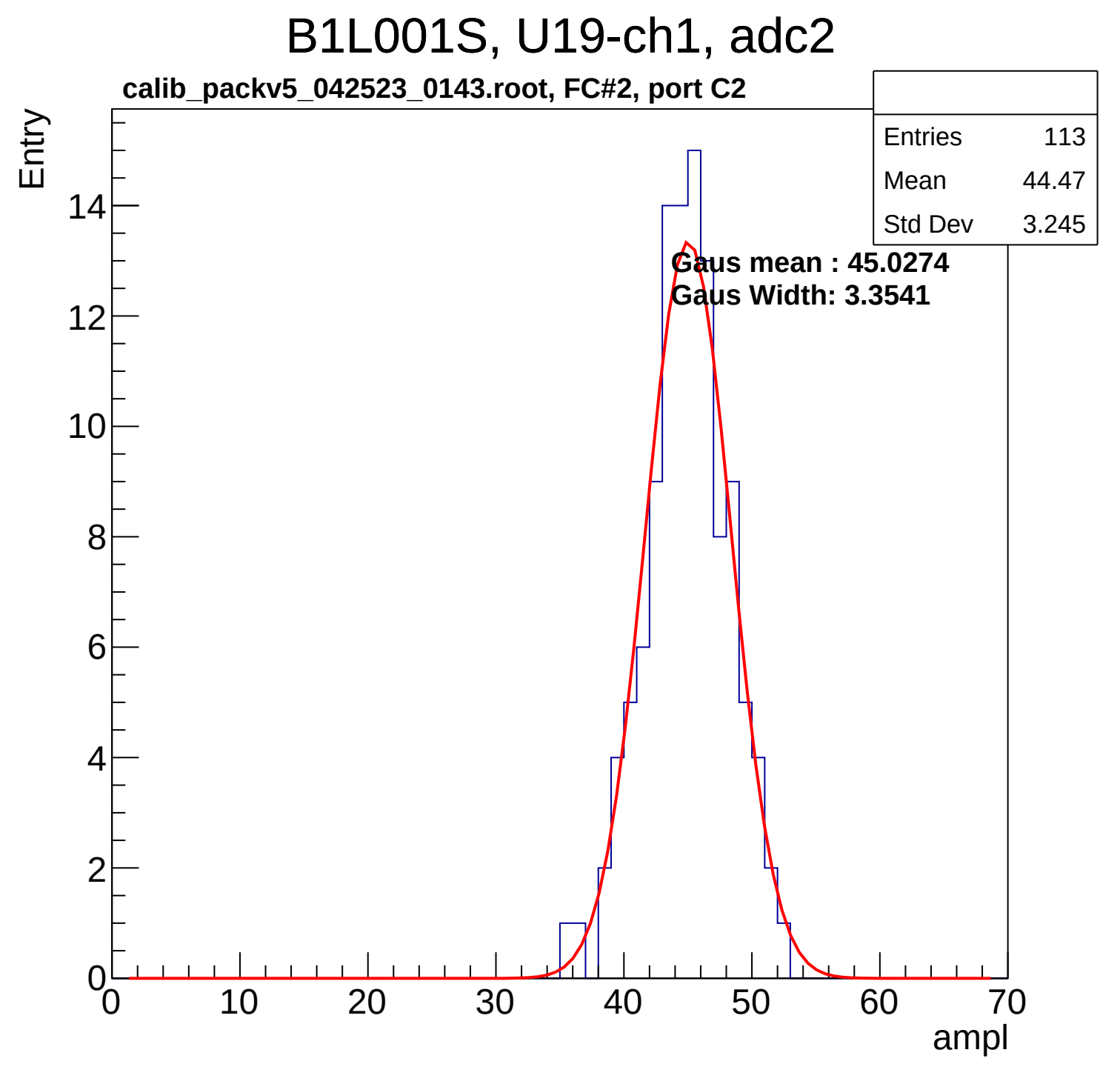
B1L001S, U19-ch1, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 113
Mean 44.47
Std Dev 3.245
Gaus mean : 45.0274
Gaus Width: 3.3541
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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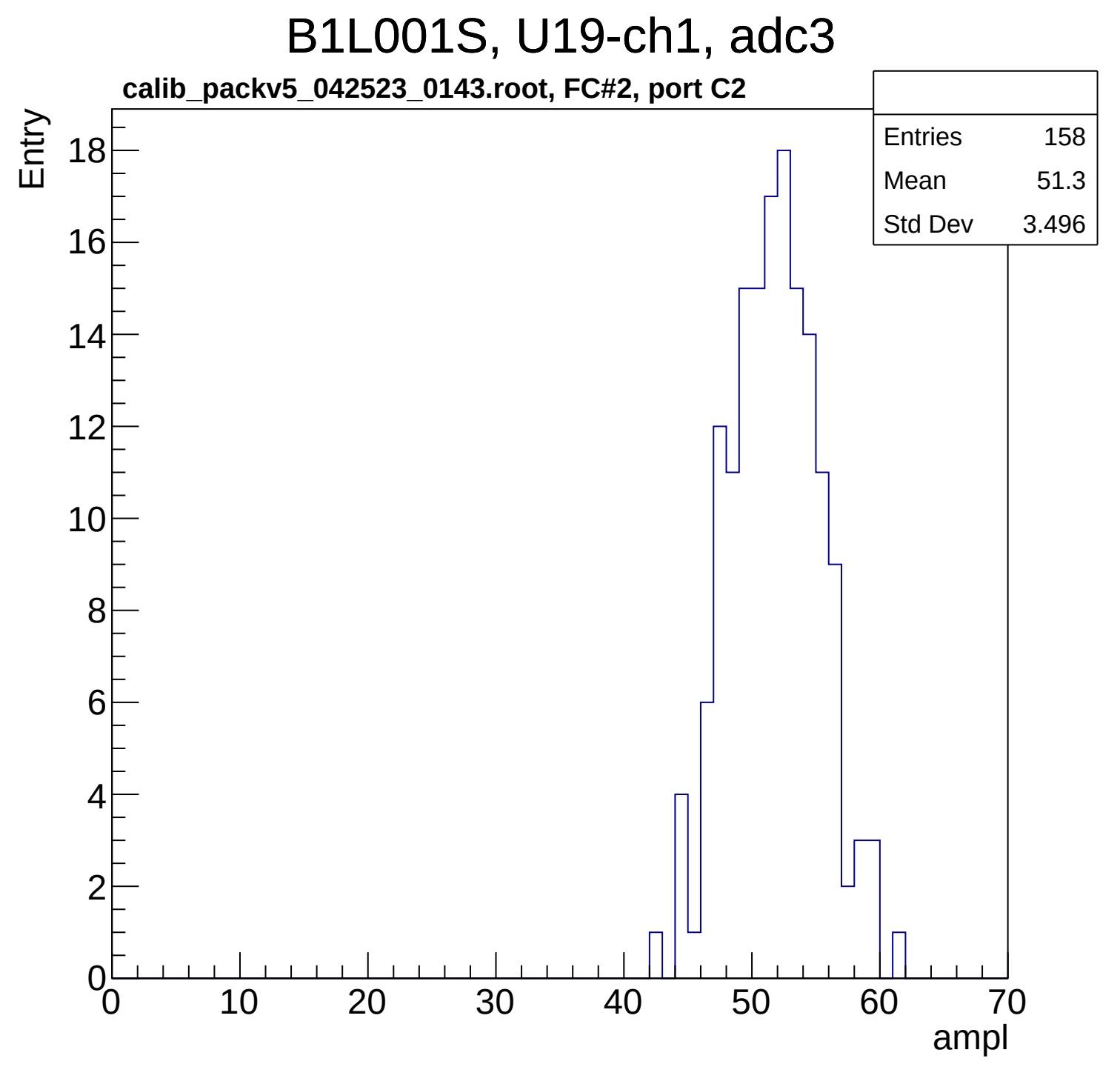
B1L001S, U19-ch1, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 158
Mean 51.3
Std Dev 3.496
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
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60
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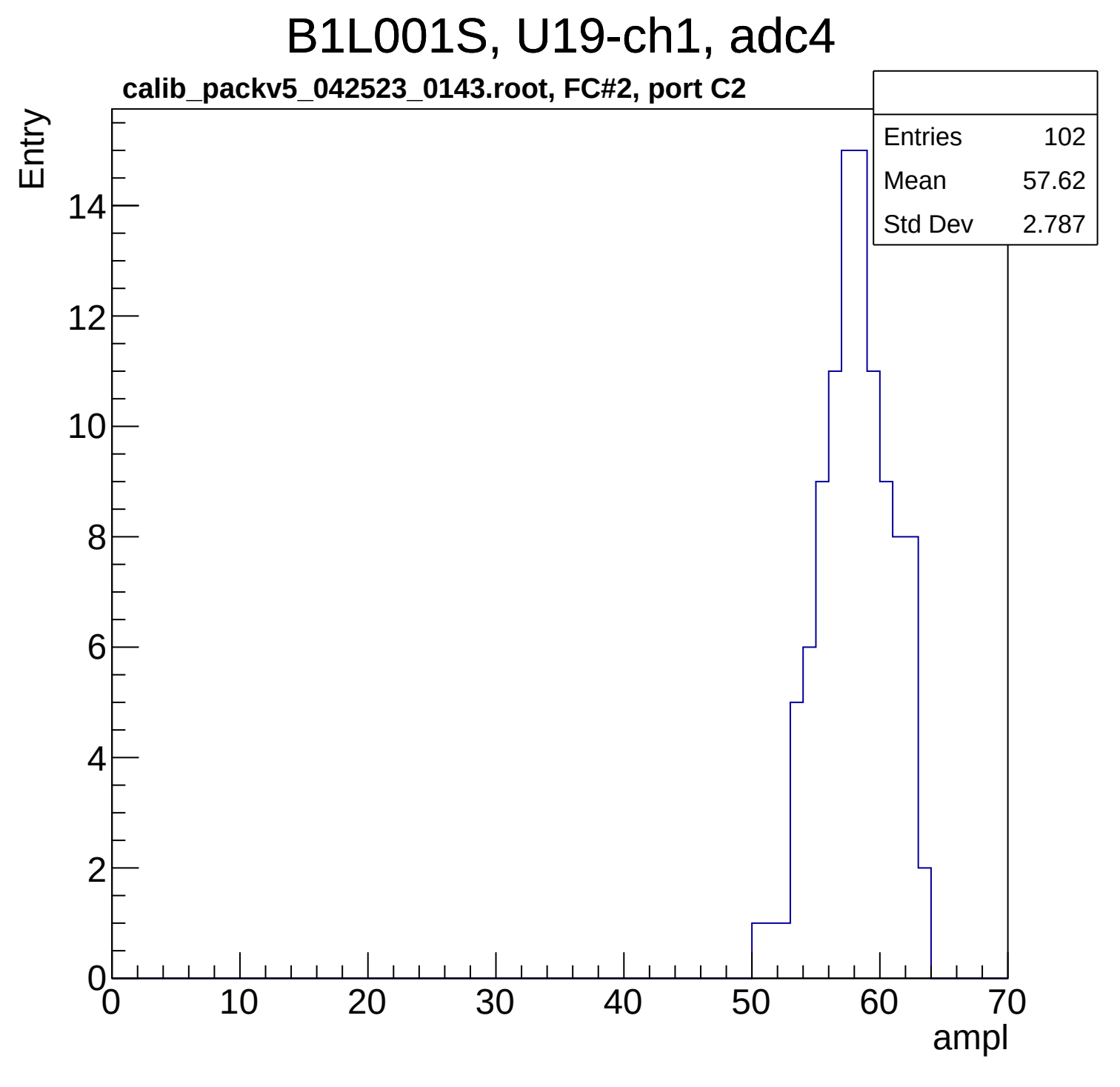
B1L001S, U19-ch1, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 102
Mean 57.62
Std Dev 2.787
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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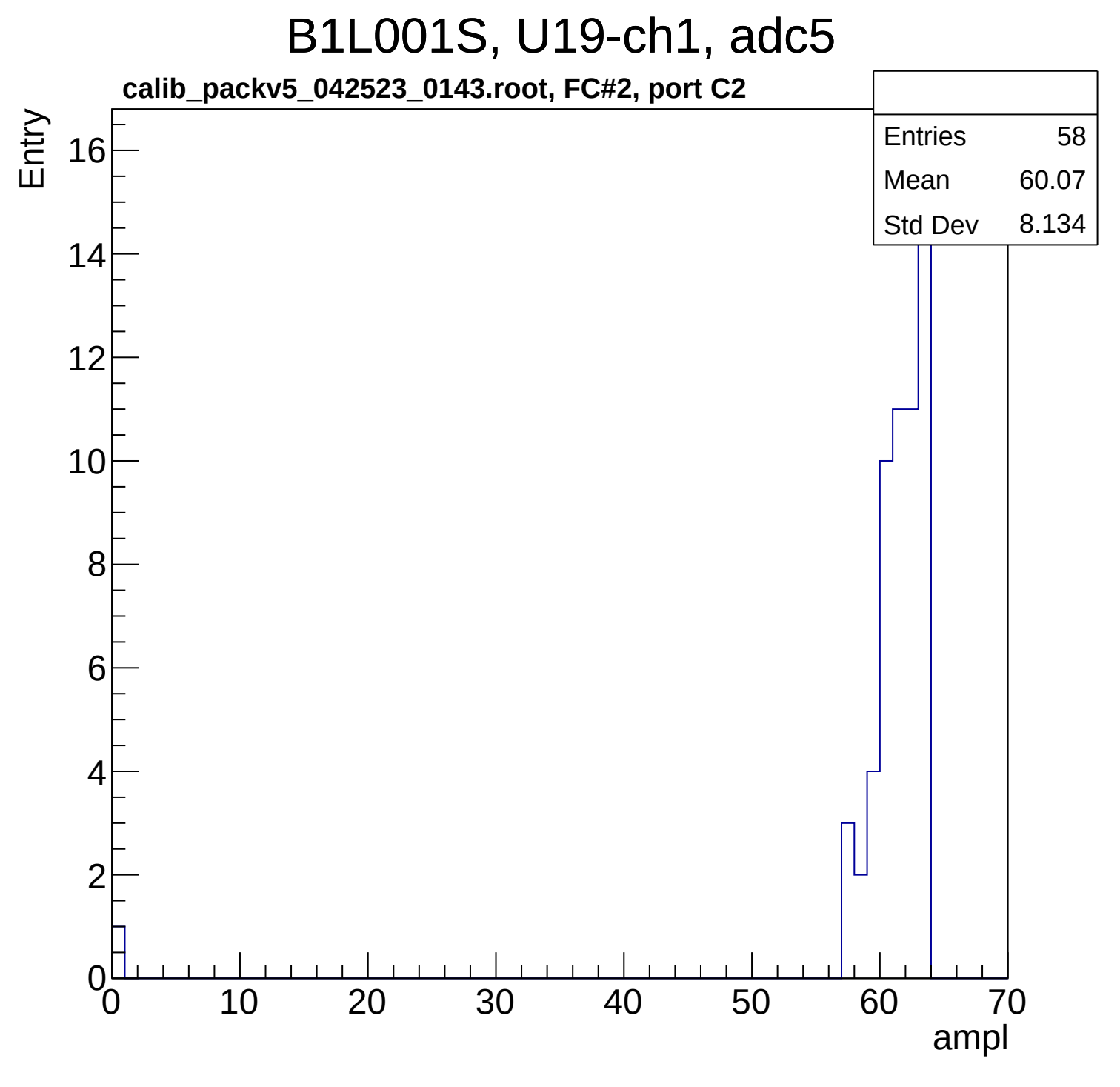
B1L001S, U19-ch1, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 58
Mean 60.07
Std Dev 8.134
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
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40
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60
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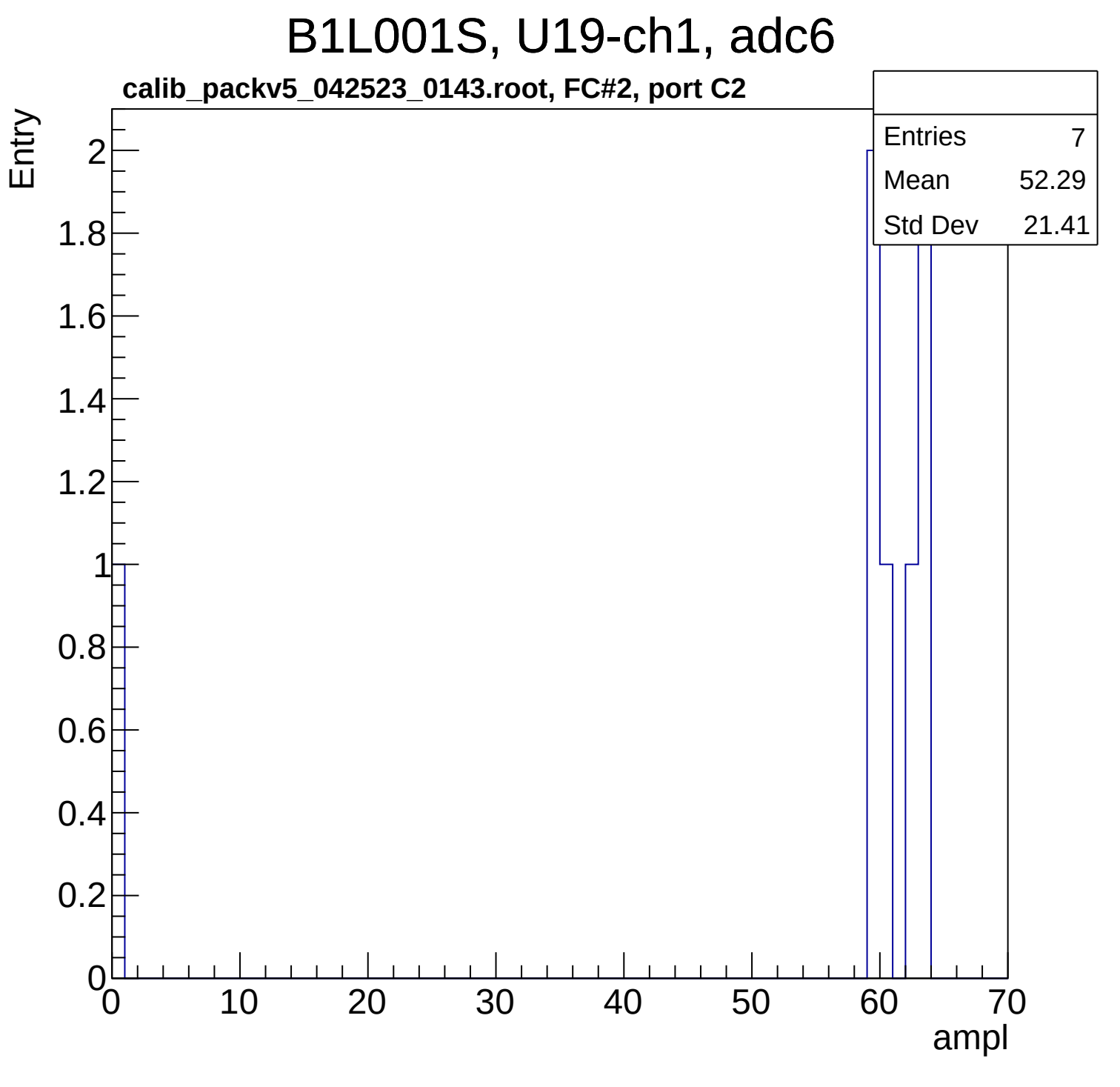
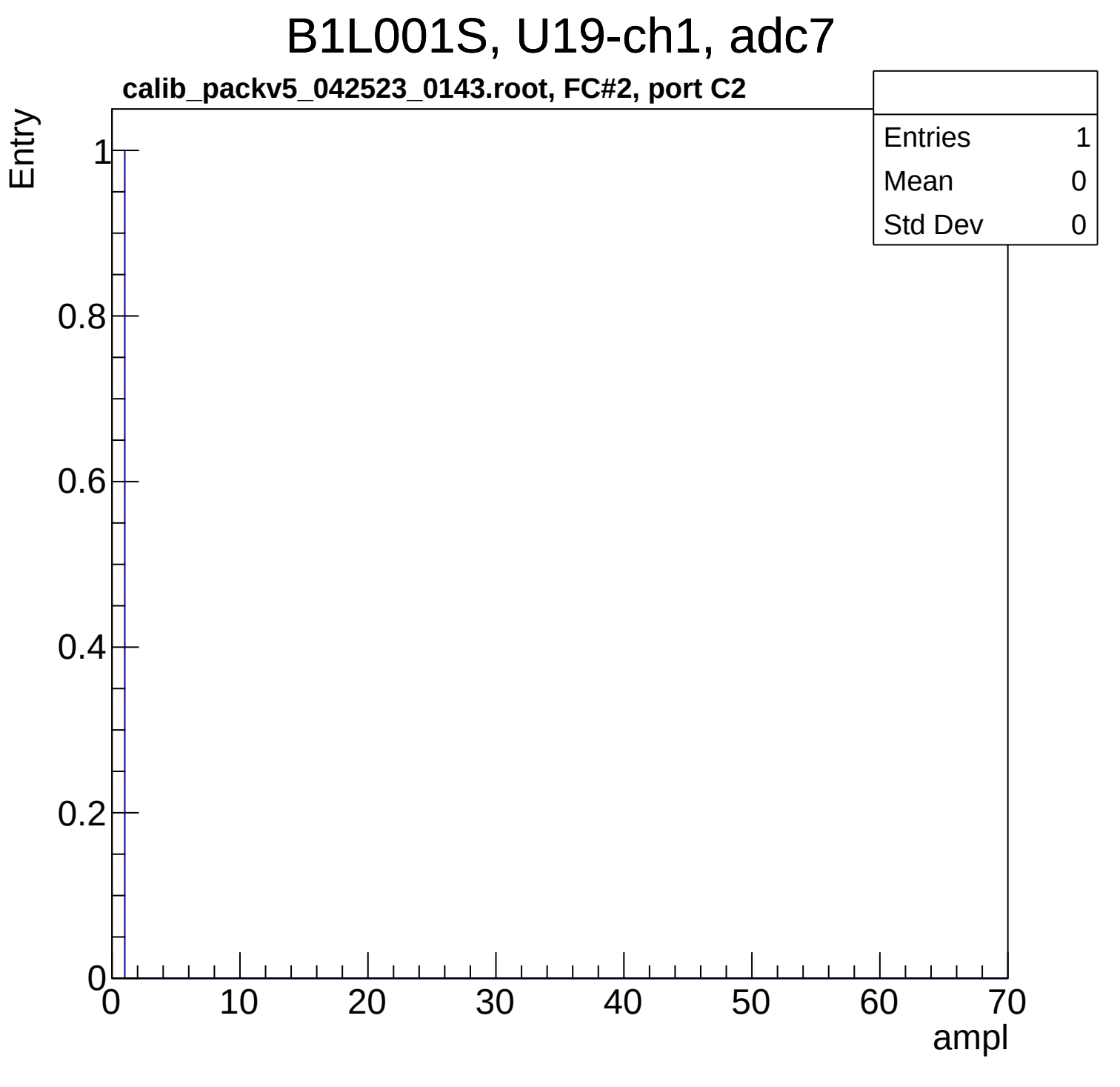
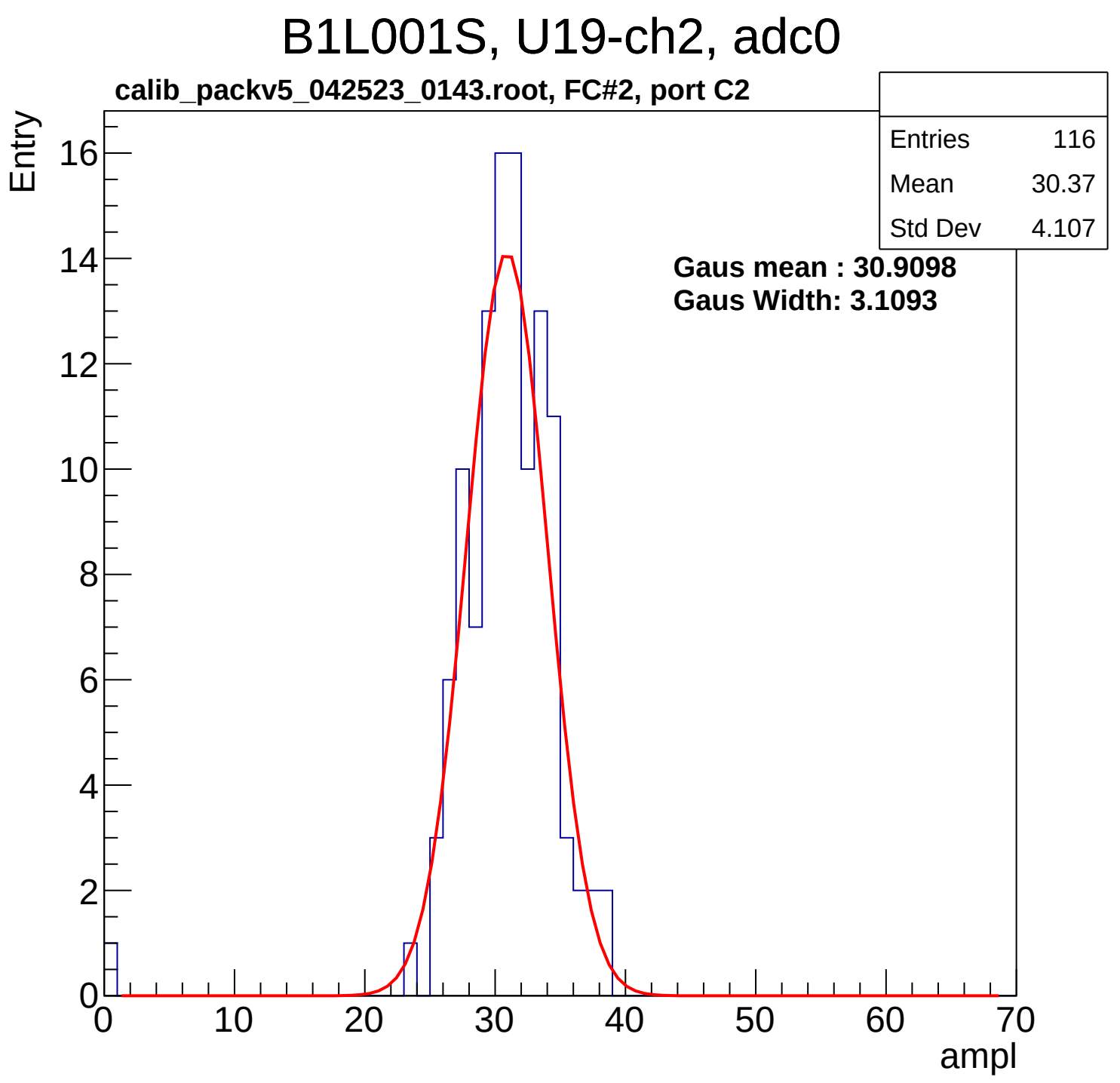
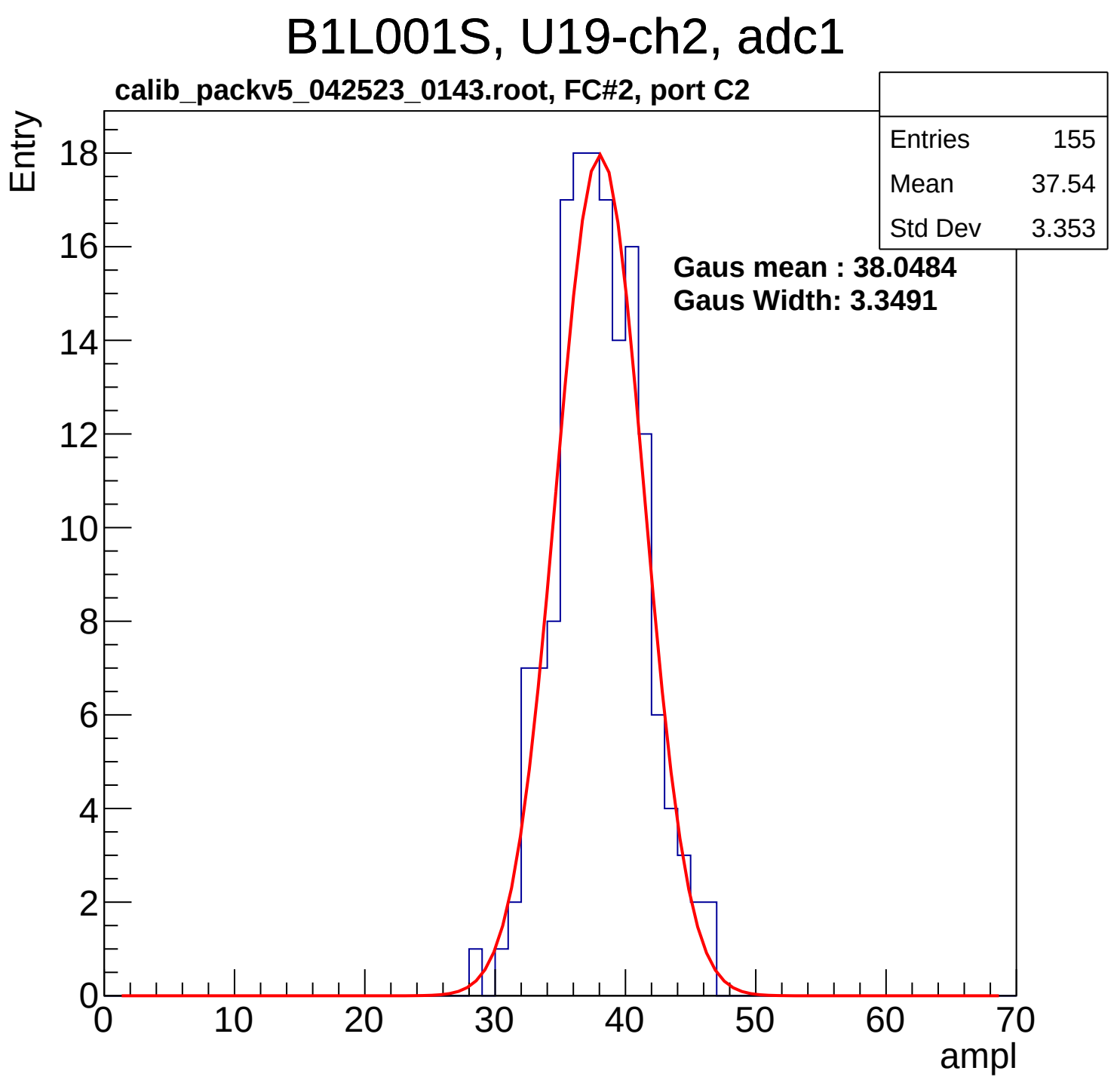
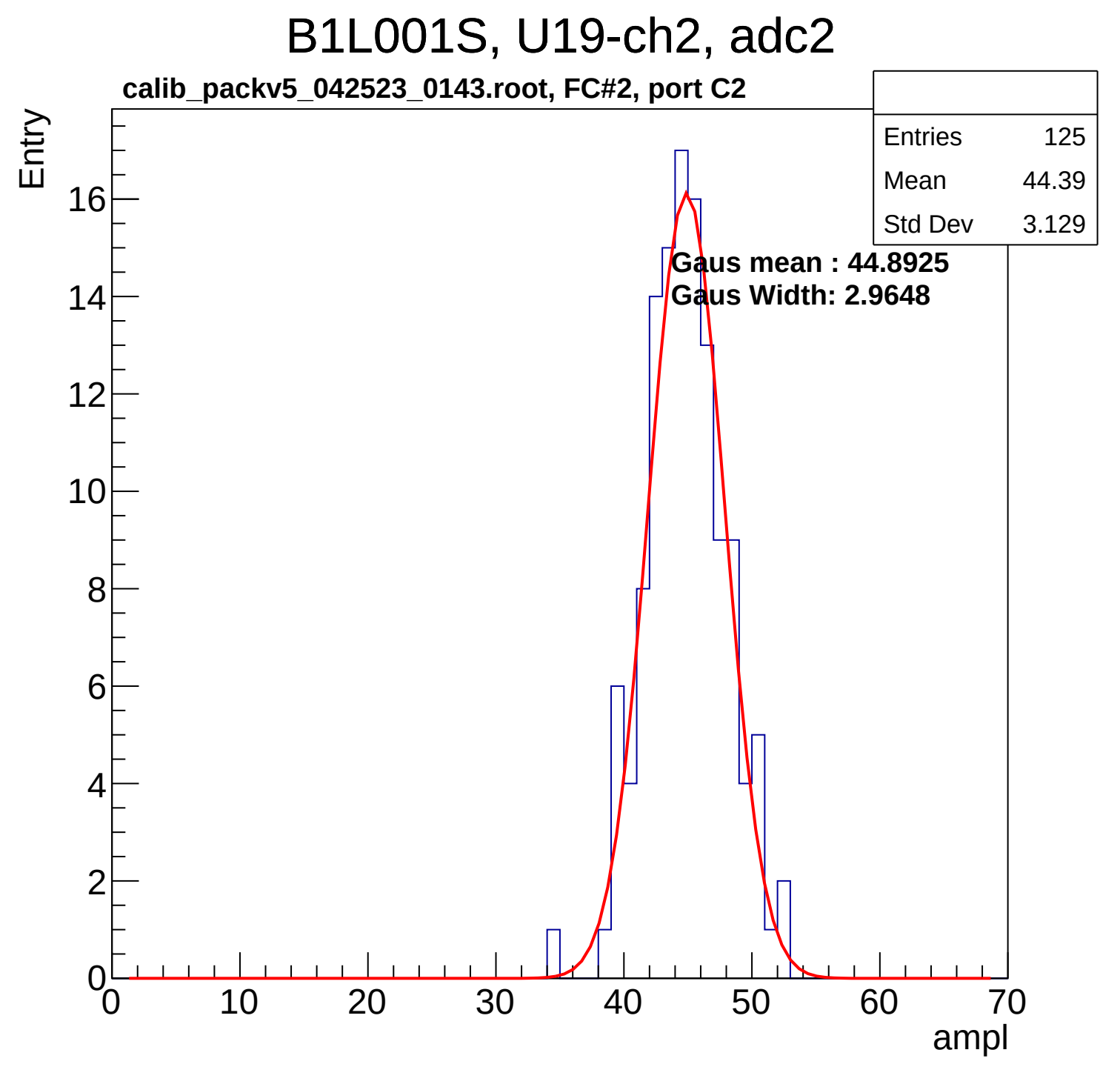

B1L001S, U19-ch1, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 7
Mean 52.29
Std Dev 21.41
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L001S, U19-ch1, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch2, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 116
Mean 30.37
Std Dev 4.107
Gaus mean : 30.9098
Gaus Width: 3.1093
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70


B1L001S, U19-ch2, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 155
Mean 37.54
Std Dev 3.353
Gaus mean : 38.0484
Gaus Width: 3.3491
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70


B1L001S, U19-ch2, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 125
Mean 44.39
Std Dev 3.129
Gaus mean : 44.8925
Gaus Width: 2.9648
Entry
ampl
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2
4
6
8
10
12
14
16
0
10
20
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40
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60
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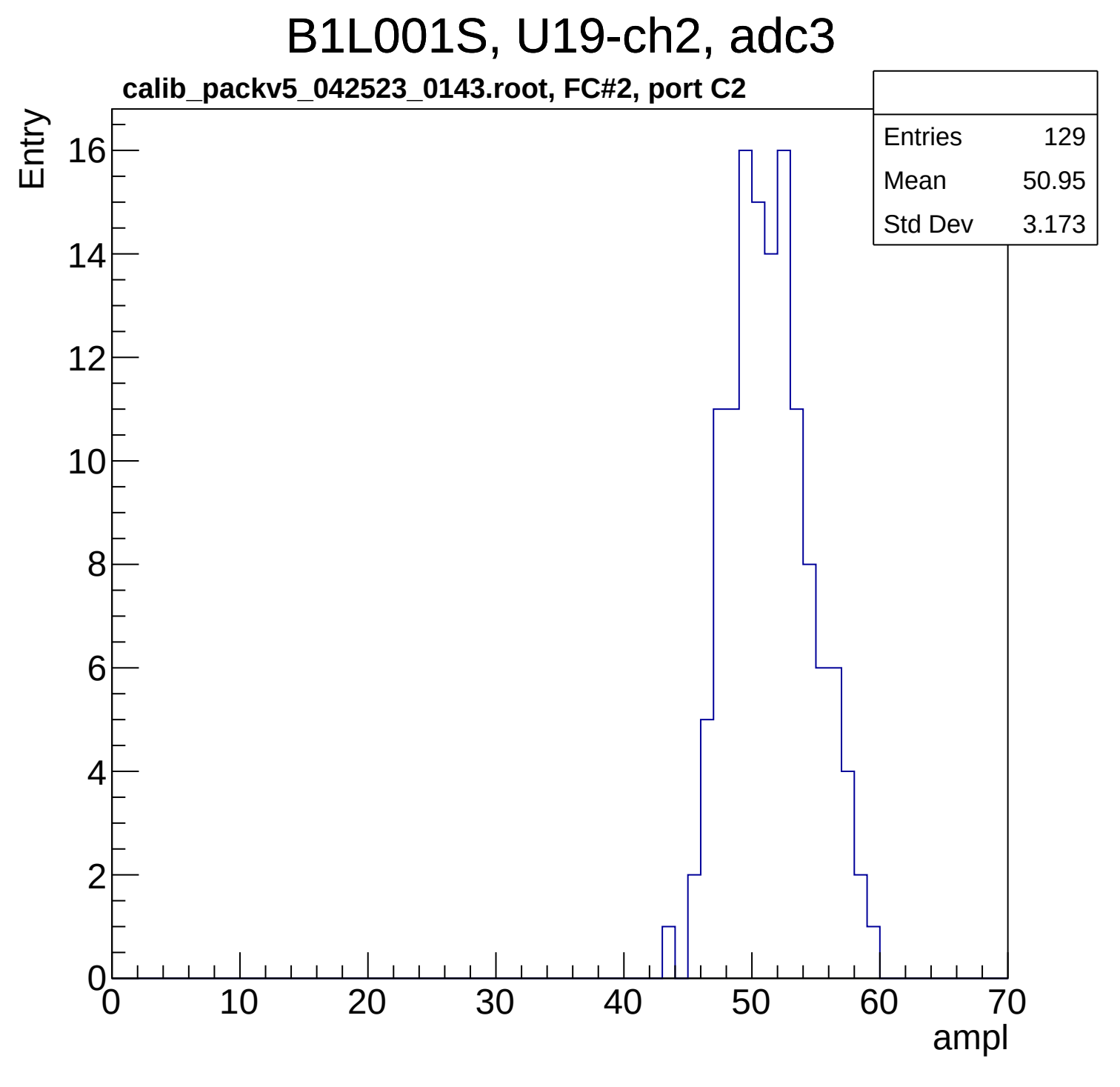
B1L001S, U19-ch2, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 129
Mean 50.95
Std Dev 3.173
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
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40
50
60
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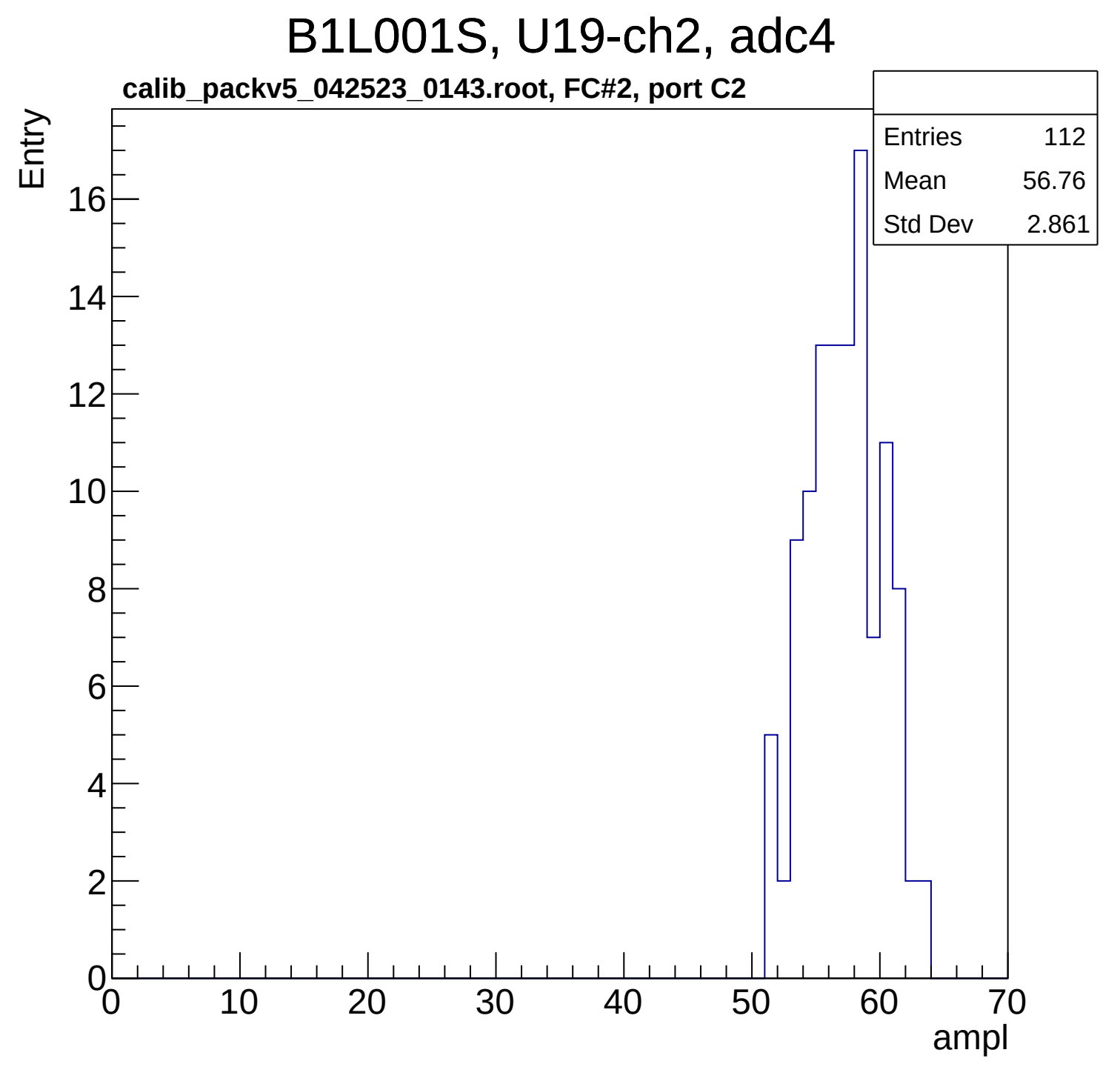
B1L001S, U19-ch2, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 112
Mean 56.76
Std Dev 2.861
Entry
ampl
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2
4
6
8
10
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0
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60
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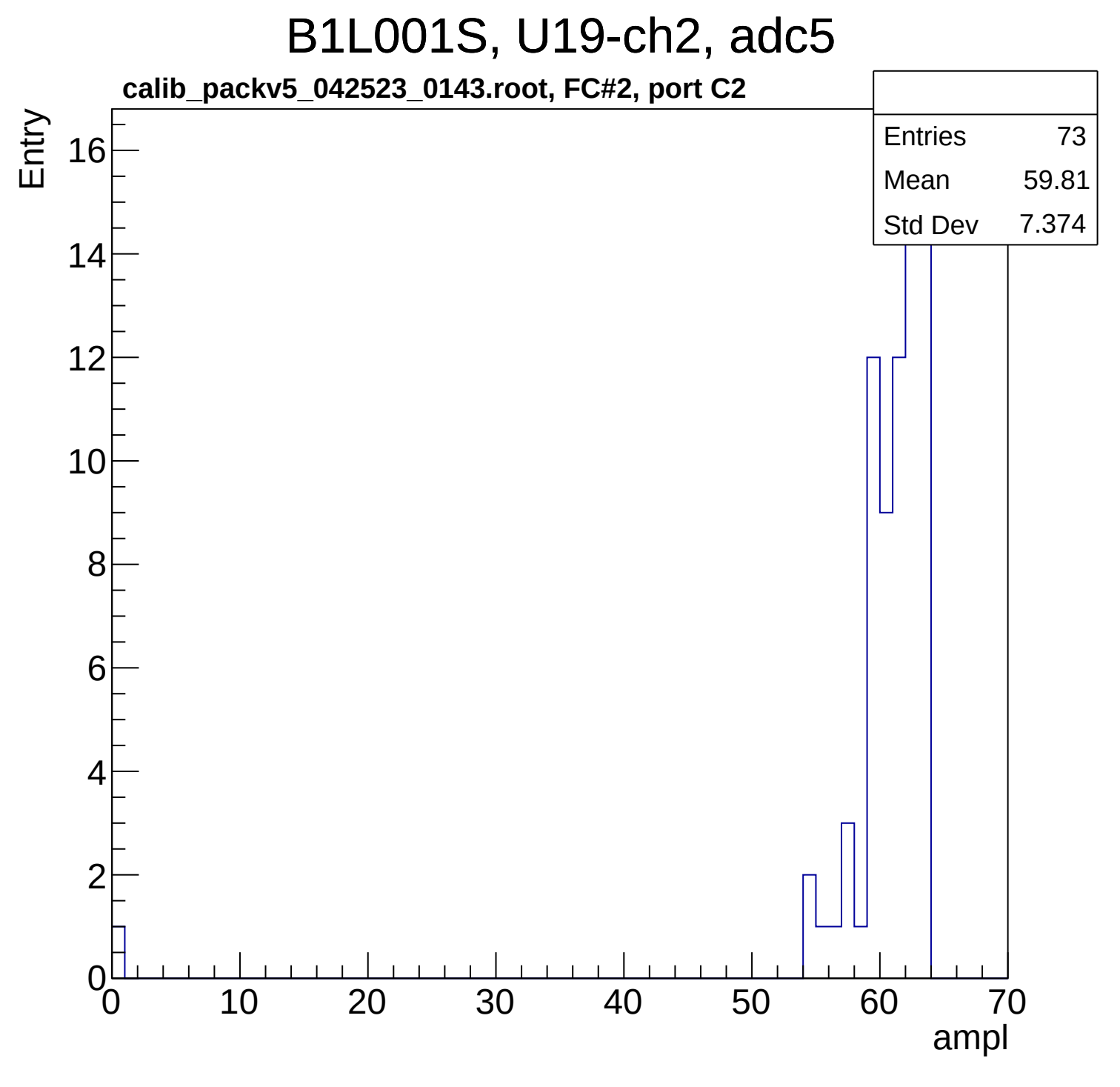
B1L001S, U19-ch2, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 73
Mean 59.81
Std Dev 7.374
Entry
ampl
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2
4
6
8
10
12
14
16
0
10
20
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60
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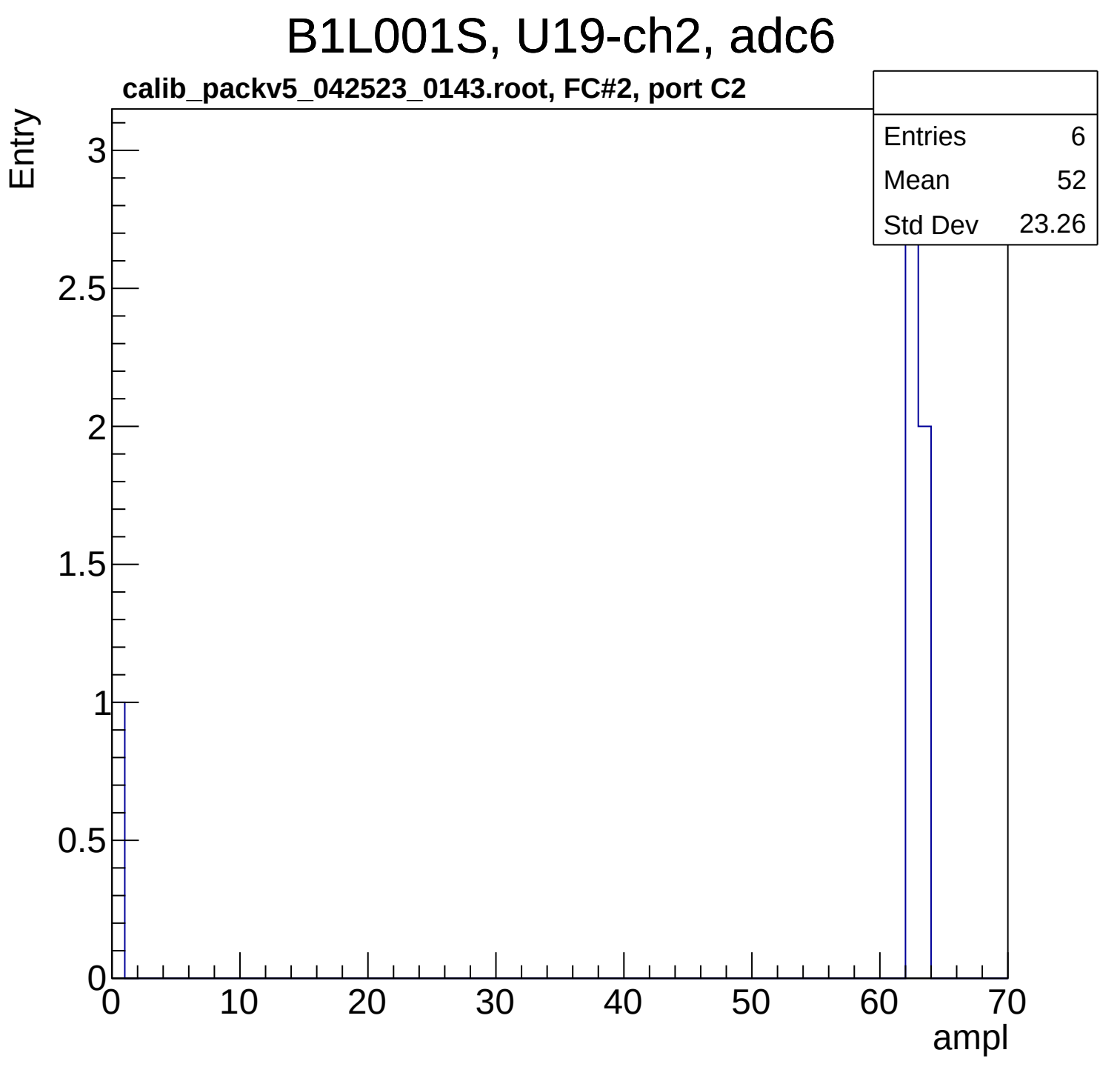
B1L001S, U19-ch2, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 6
Mean 52
Std Dev 23.26
Entry
ampl
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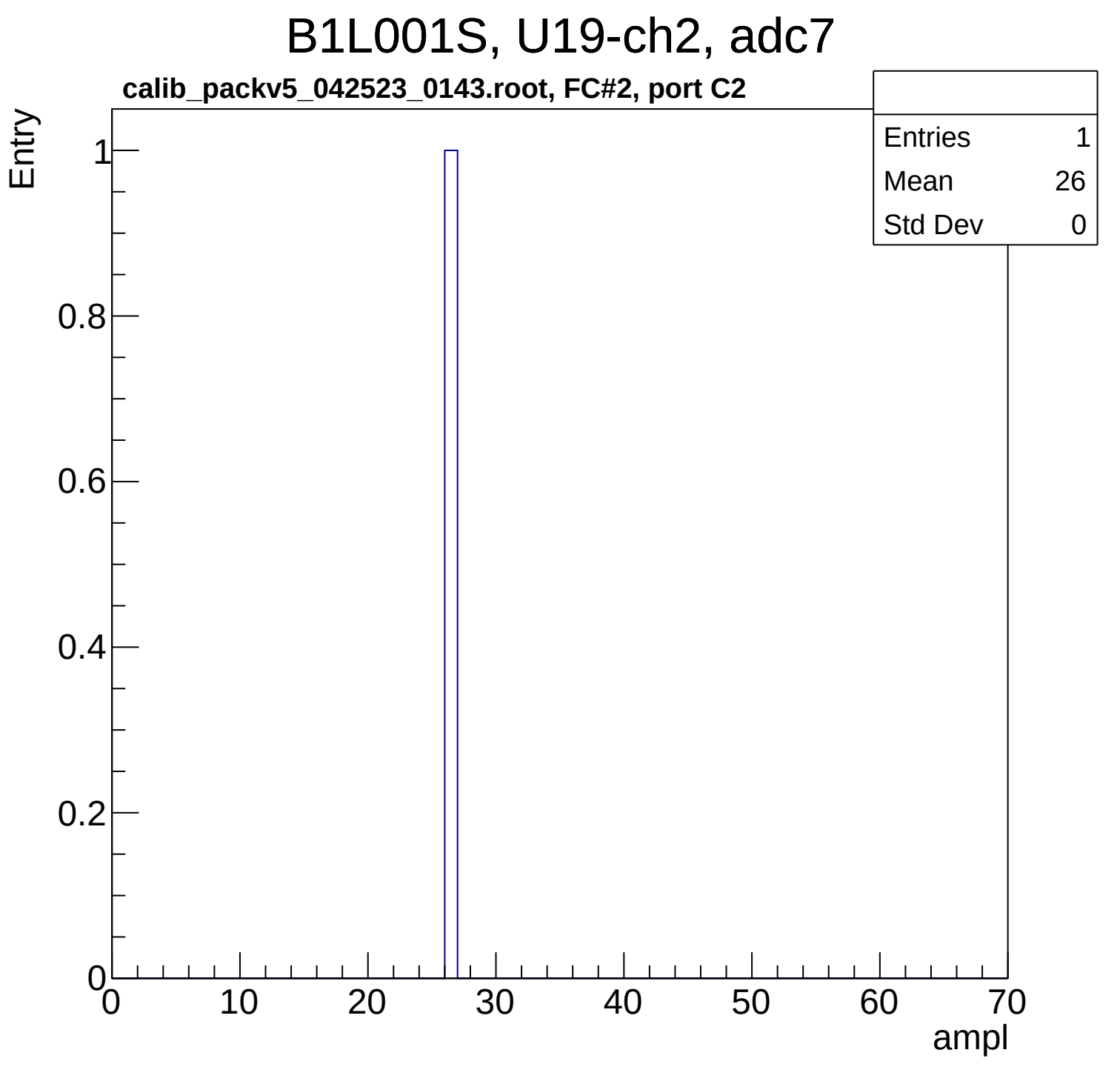
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L001S, U19-ch2, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 26
Std Dev 0
Entry
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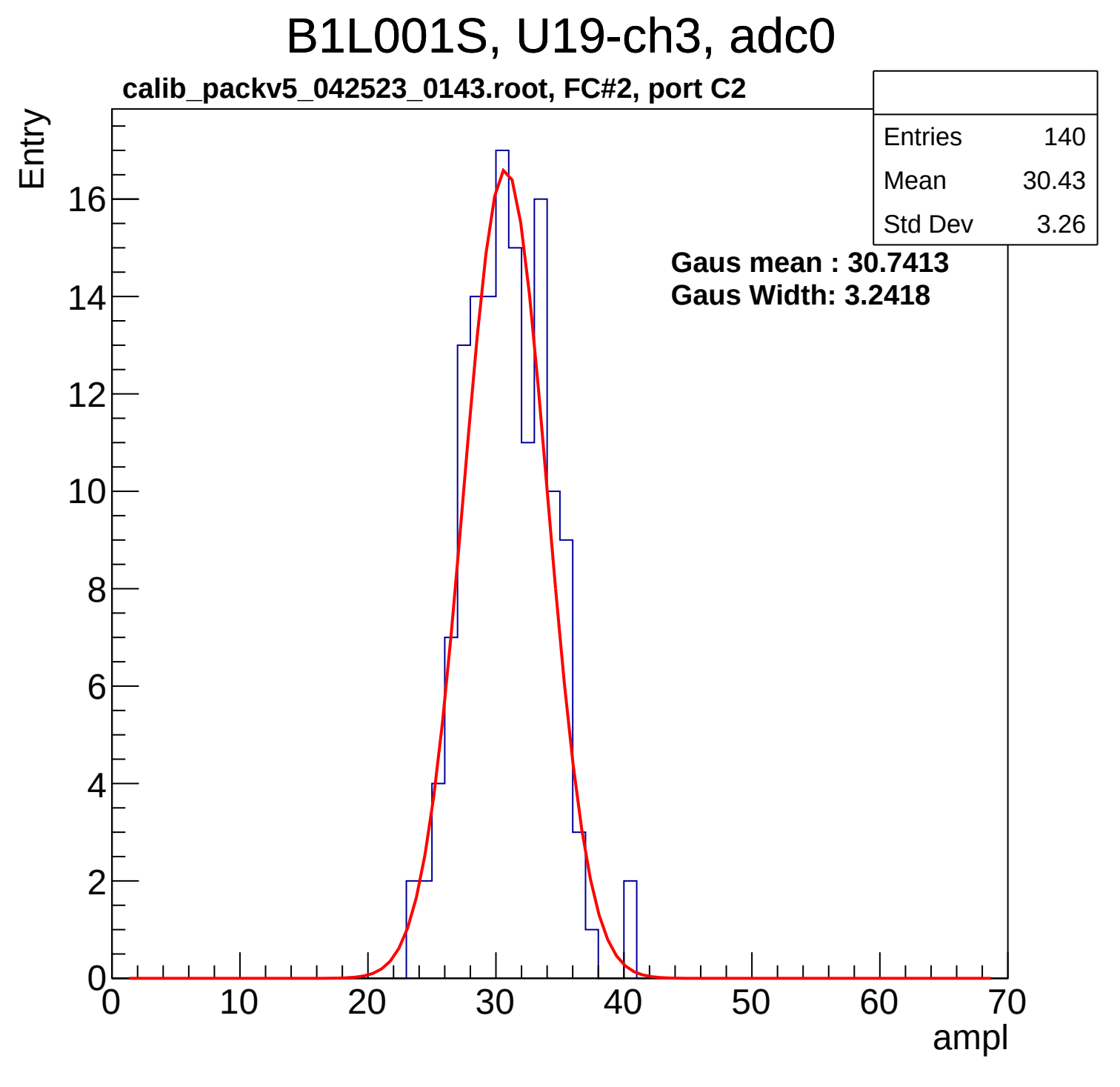
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch3, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 140
Mean 30.43
Std Dev 3.26
Gaus mean : 30.7413
Gaus Width: 3.2418
Entry
ampl
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2
4
6
8
10
12
14
16
0
10
20
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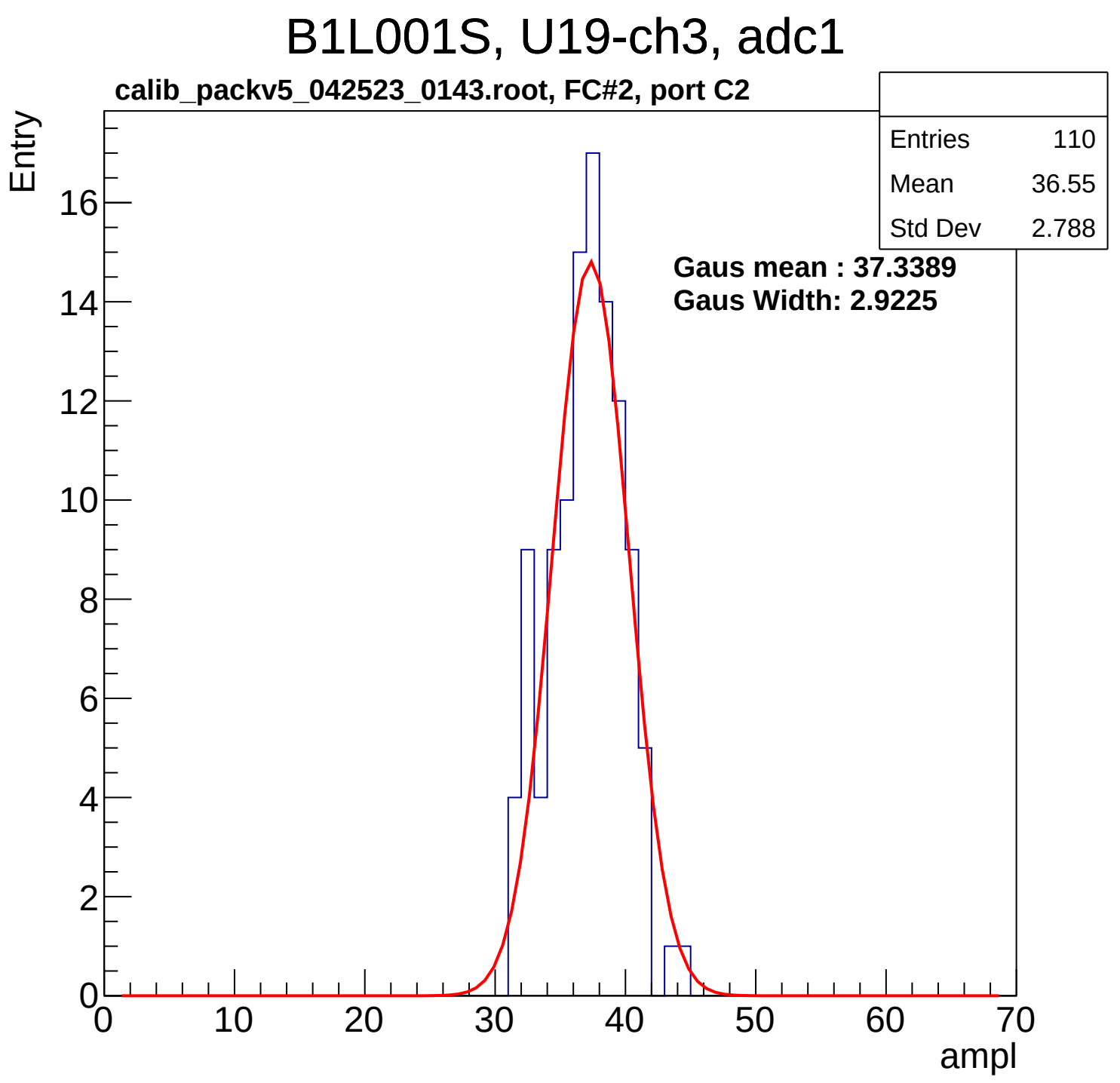
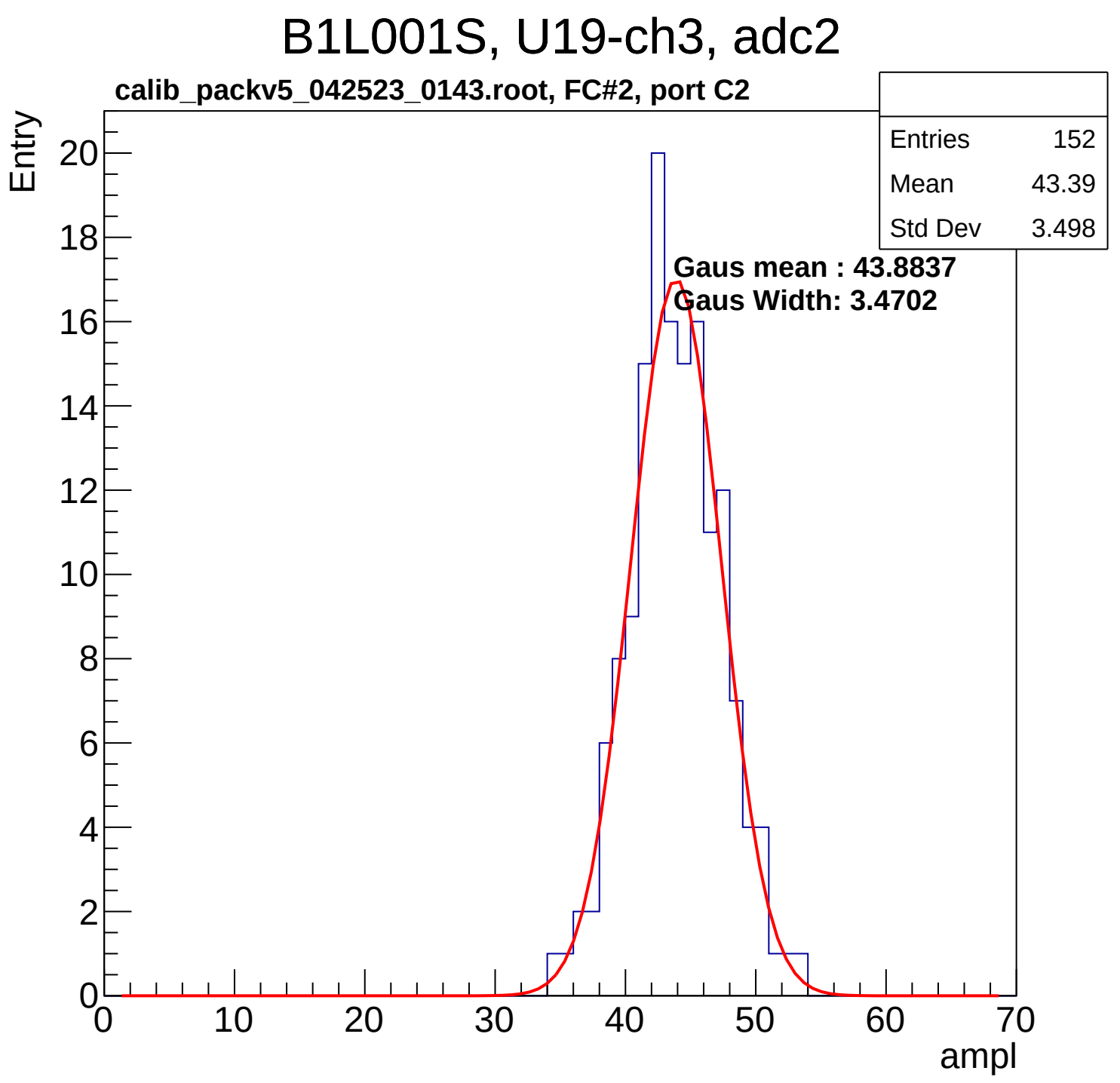
40
50
60
70


B1L001S, U19-ch3, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 110
Mean 36.55
Std Dev 2.788
Gaus mean : 37.3389
Gaus Width: 2.9225
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70


B1L001S, U19-ch3, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 152
Mean 43.39
Std Dev 3.498
Gaus mean : 43.8837
Gaus Width: 3.4702
Entry
ampl
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4
6
8
10
12
14
16
18
20
0
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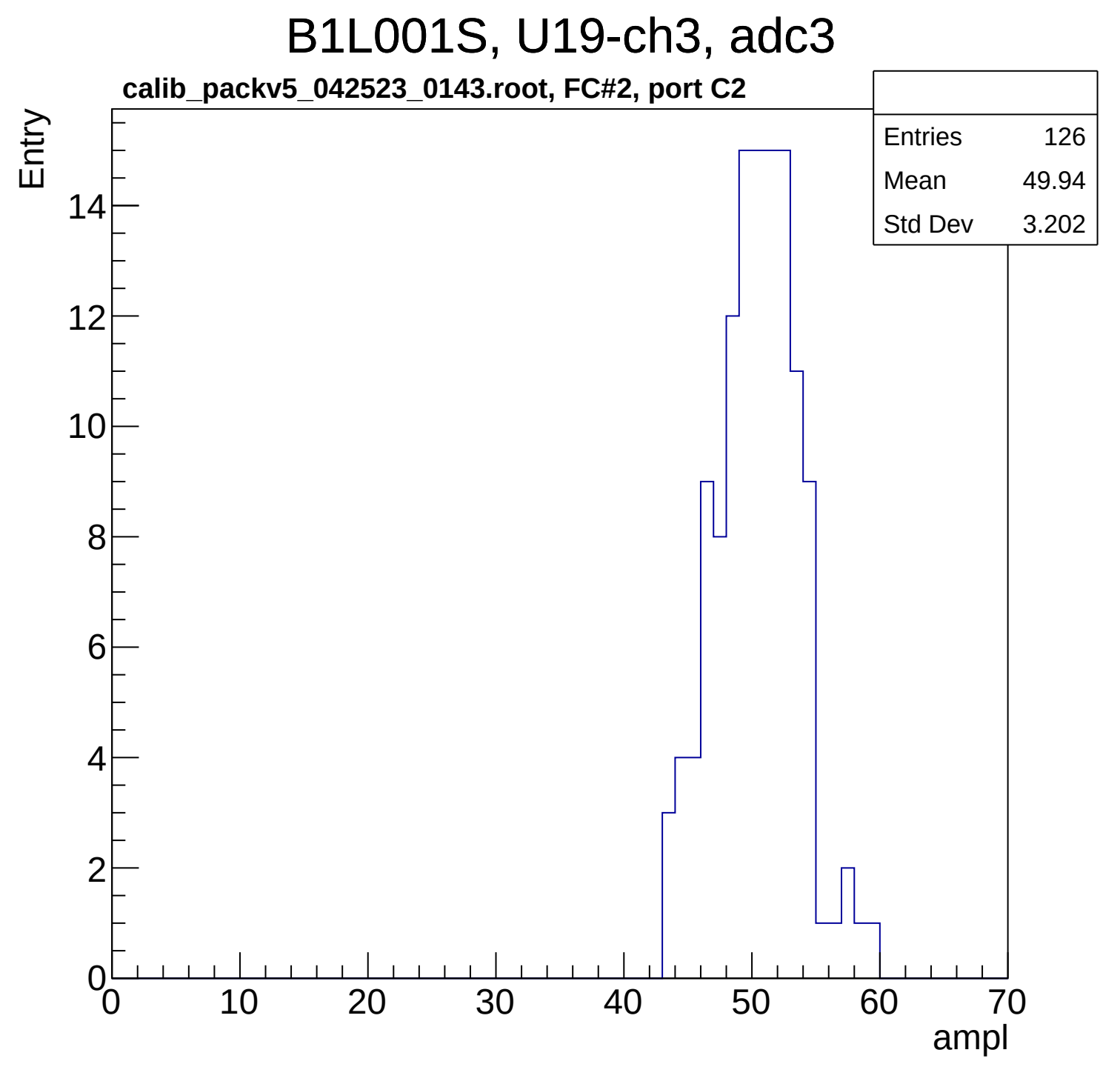
20
30
40
50
60
70


B1L001S, U19-ch3, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 126
Mean 49.94
Std Dev 3.202
Entry
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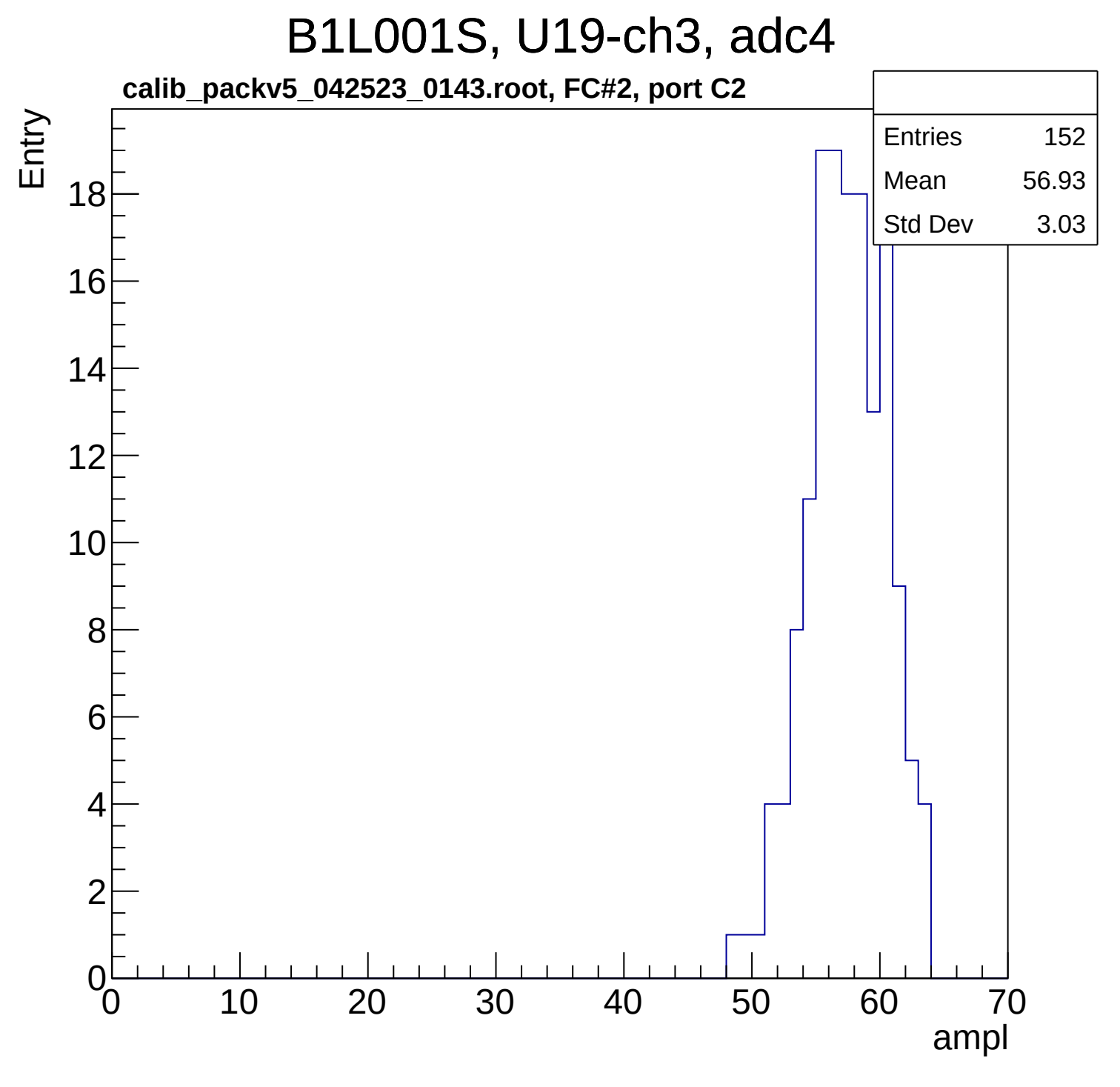
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch3, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 152
Mean 56.93
Std Dev 3.03
Entry
ampl
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4
6
8
10
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18
0
10
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40
50
60
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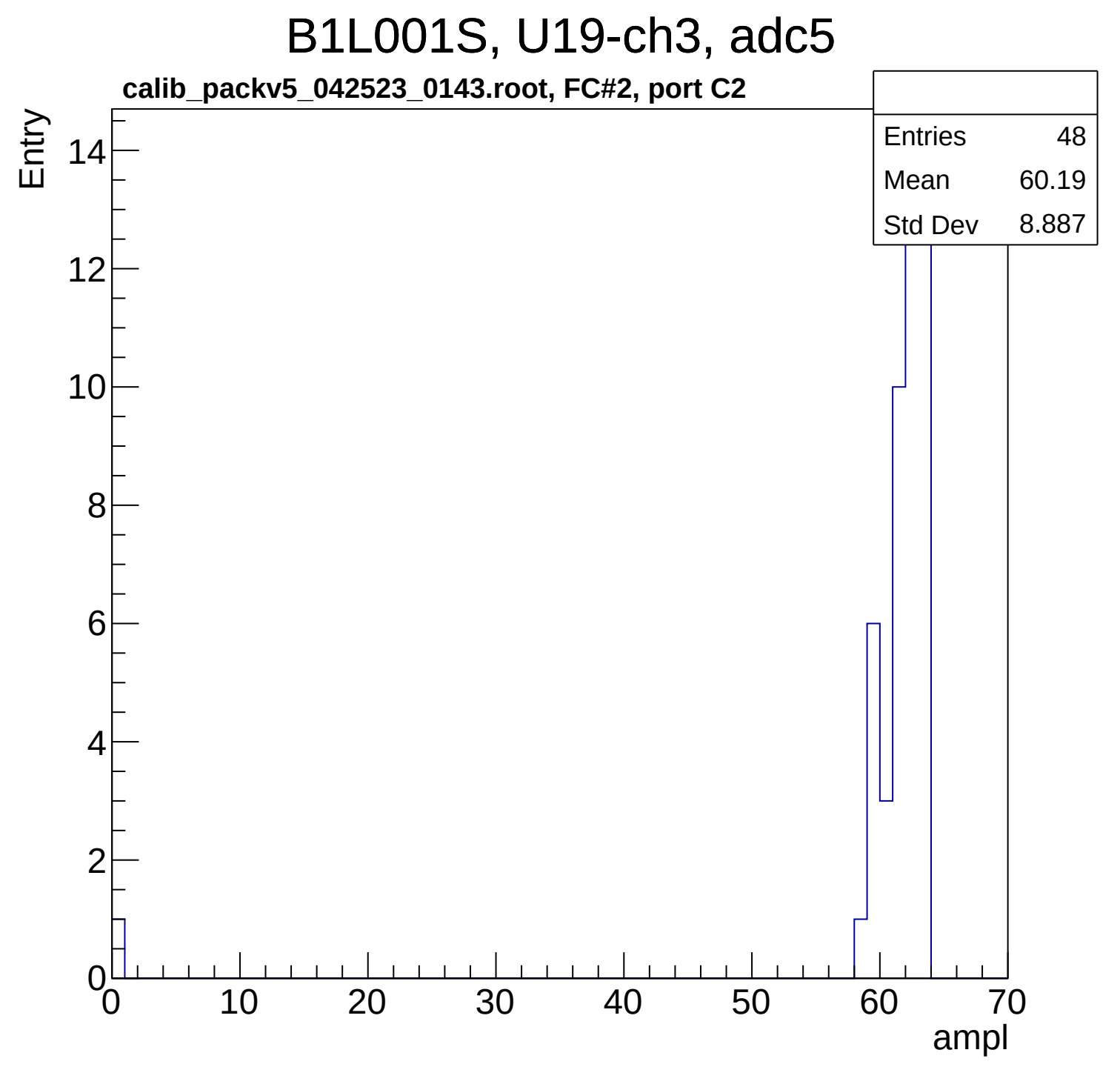
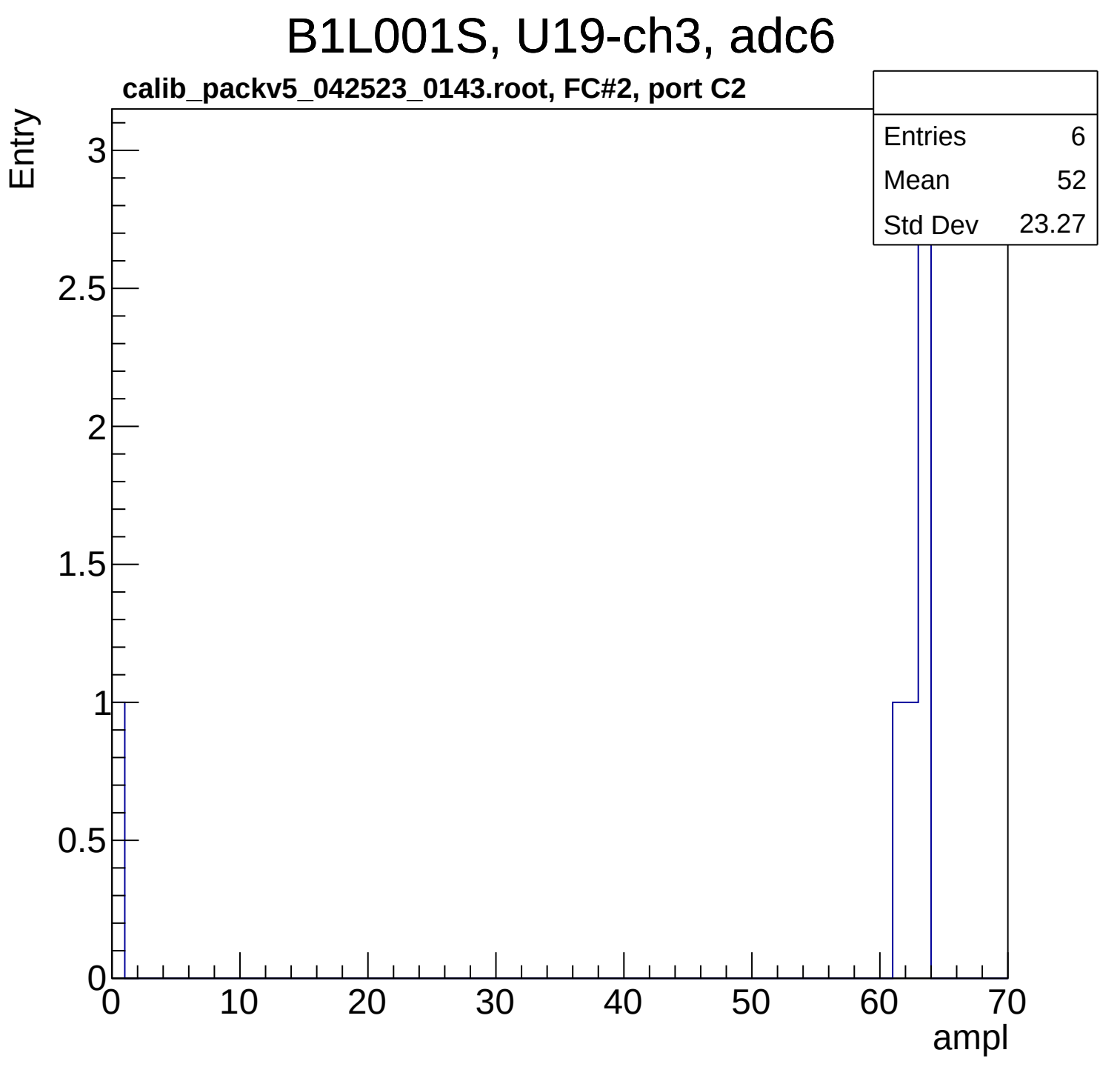

B1L001S, U19-ch3, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 48
Mean 60.19
Std Dev 8.887
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L001S, U19-ch3, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 6
Mean 52
Std Dev 23.27
Entry
ampl
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0.5
1
1.5
2
2.5
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0
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60
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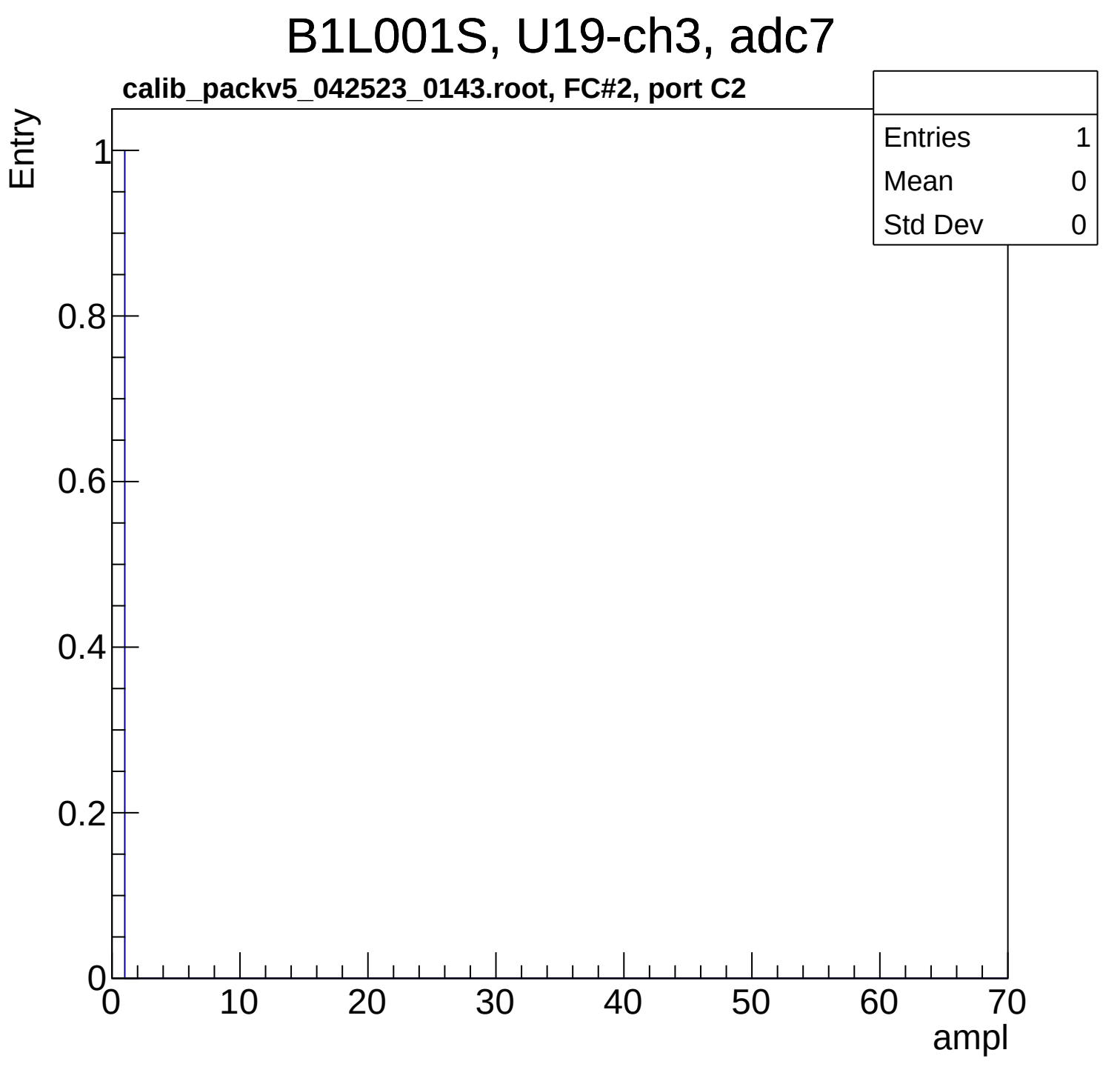
B1L001S, U19-ch3, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
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0
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10
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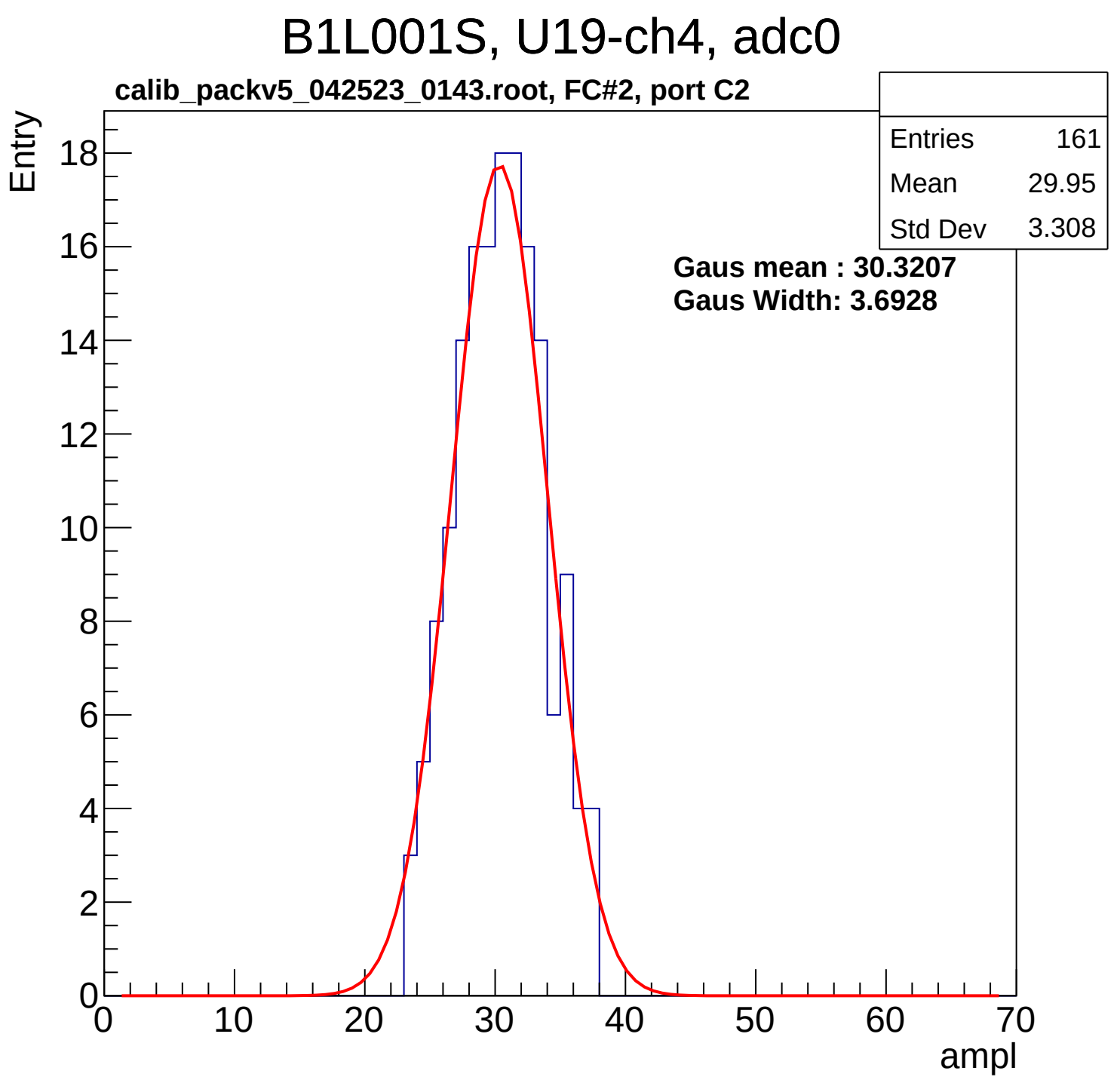
50
60
70
ampl


B1L001S, U19-ch4, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 161
Mean 29.95
Std Dev 3.308
Gaus mean : 30.3207
Gaus Width: 3.6928
Entry
ampl
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4
6
8
10
12
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16
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0
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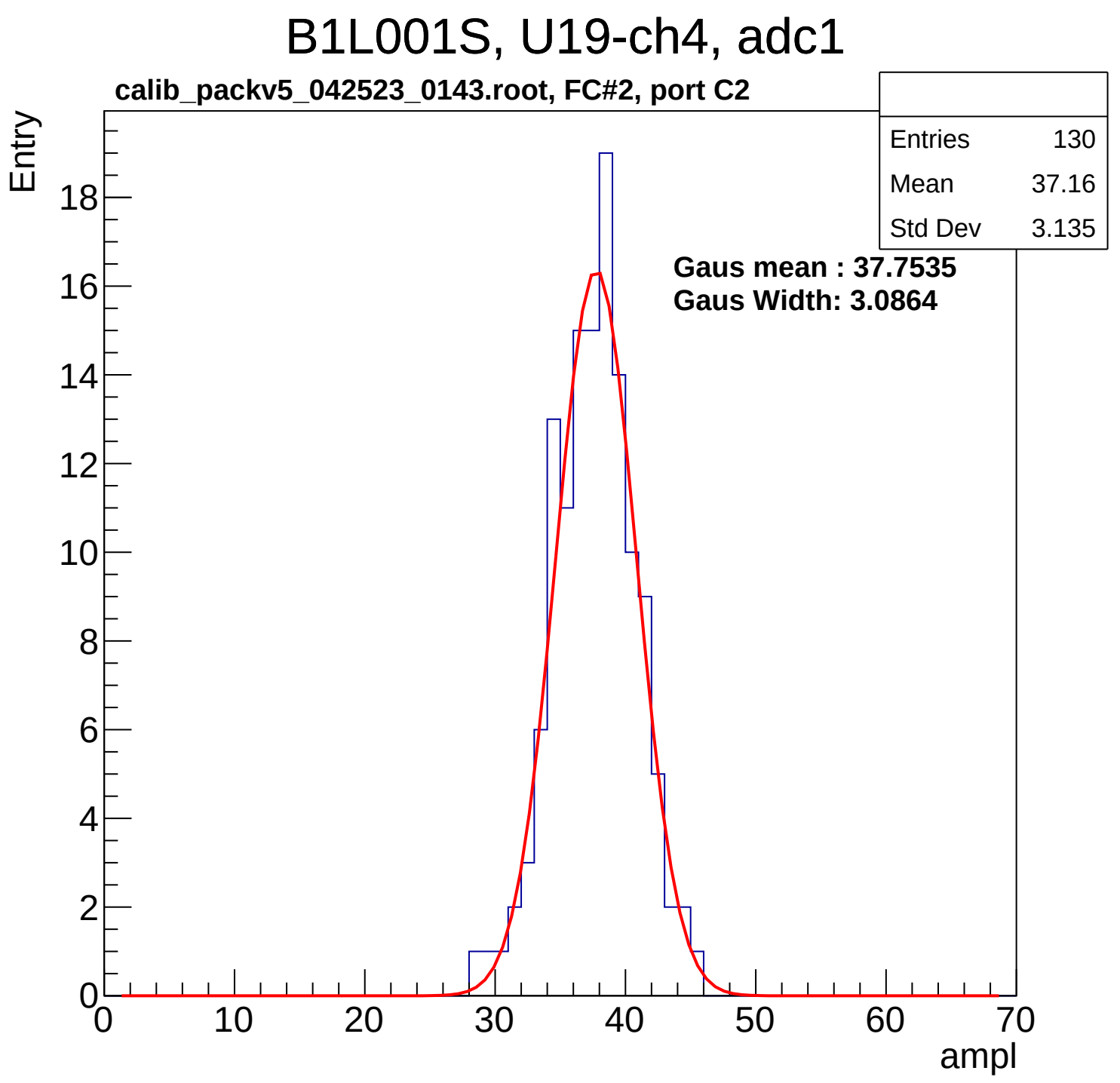
B1L001S, U19-ch4, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 130
Mean 37.16
Std Dev 3.135
Gaus mean : 37.7535
Gaus Width: 3.0864
Entry
ampl
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4
6
8
10
12
14
16
18
0
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40
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60
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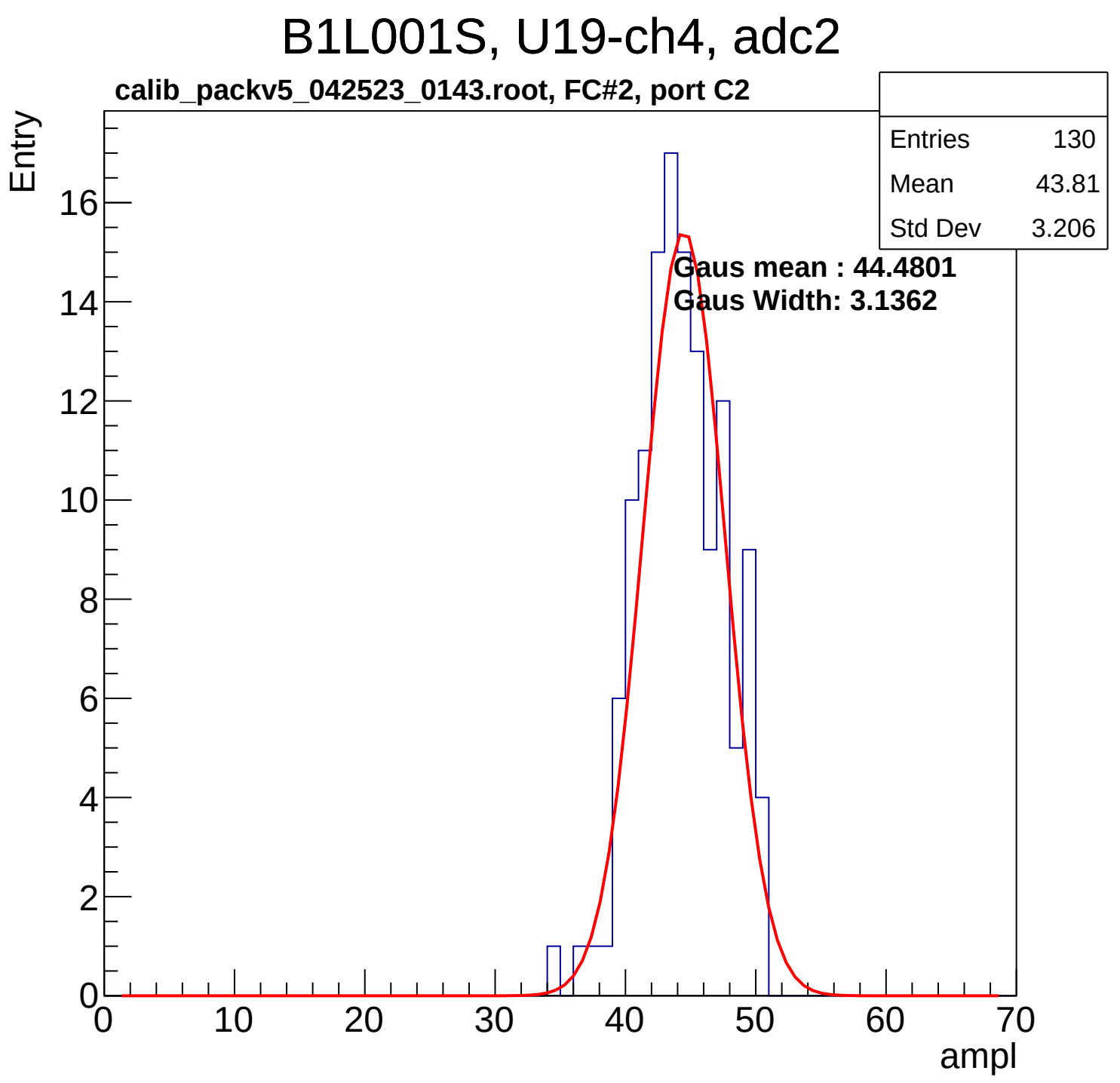
B1L001S, U19-ch4, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 130
Mean 43.81
Std Dev 3.206
Gaus mean : 44.4801
Gaus Width: 3.1362
Entry
ampl
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2
4
6
8
10
12
14
16
0
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40
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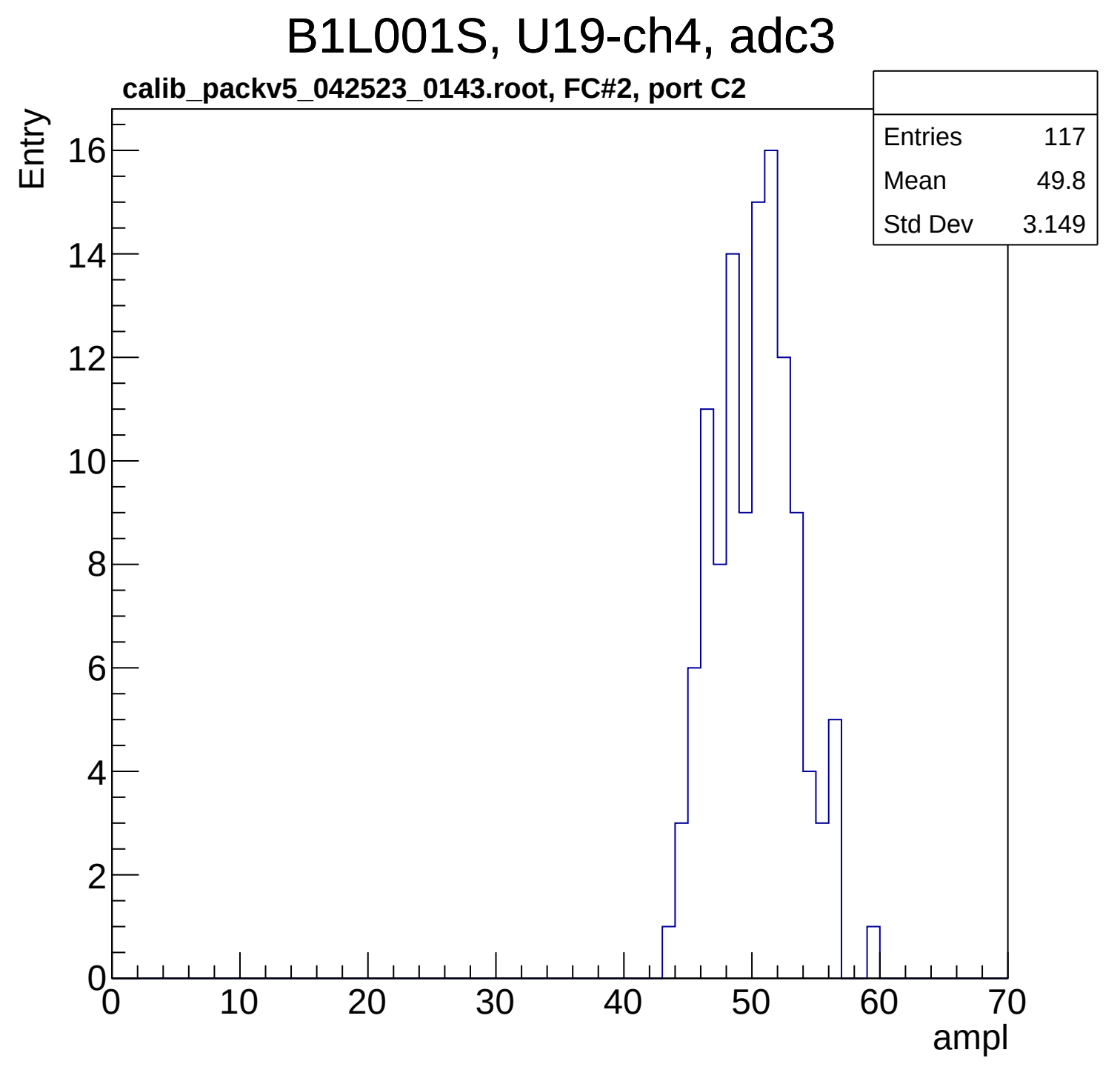
B1L001S, U19-ch4, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 117
Mean 49.8
Std Dev 3.149
Entry
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4
6
8
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14
16
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10
20
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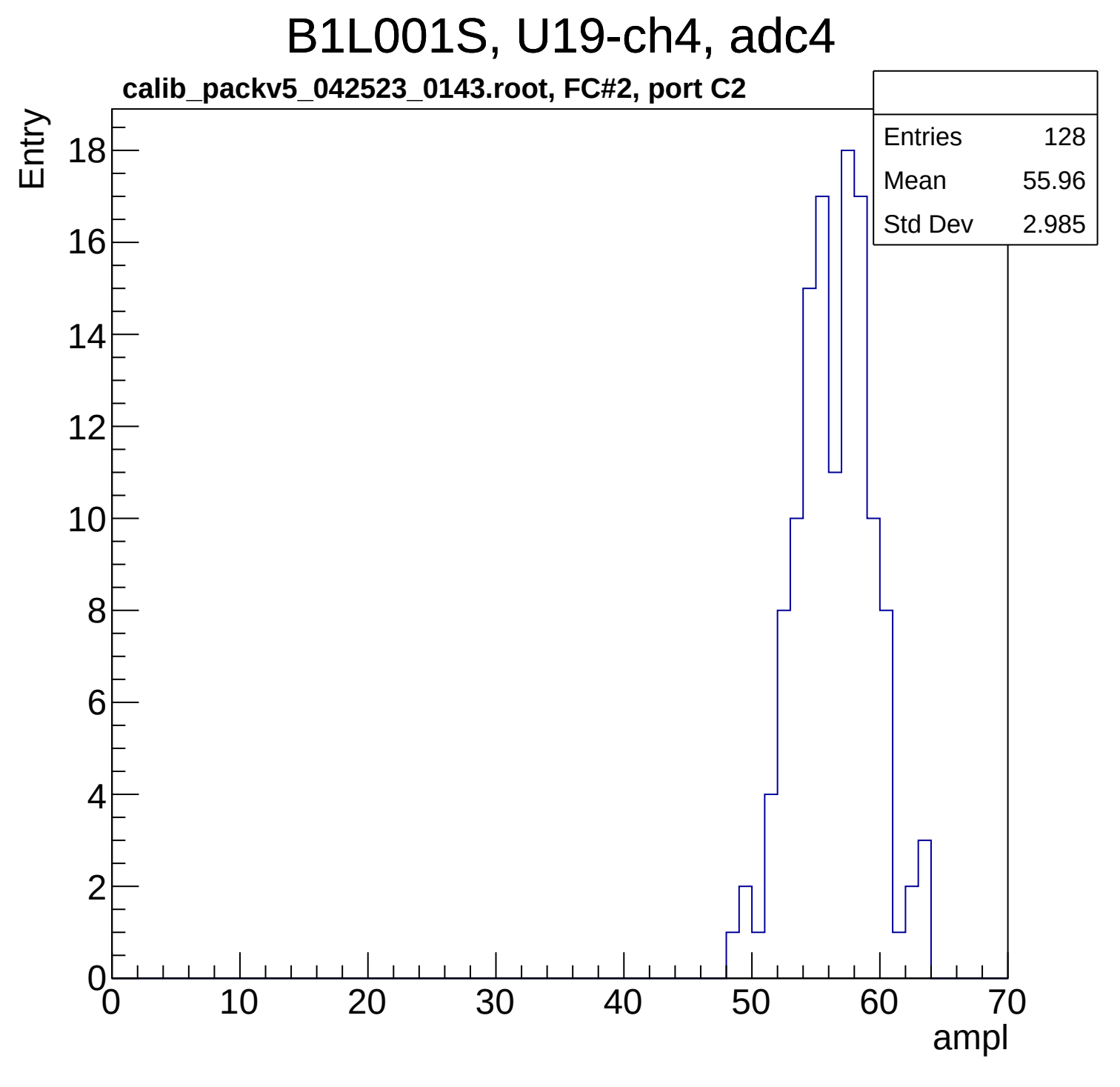
40
50
60
70
ampl


B1L001S, U19-ch4, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 128
Mean 55.96
Std Dev 2.985
Entry
ampl
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4
6
8
10
12
14
16
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0
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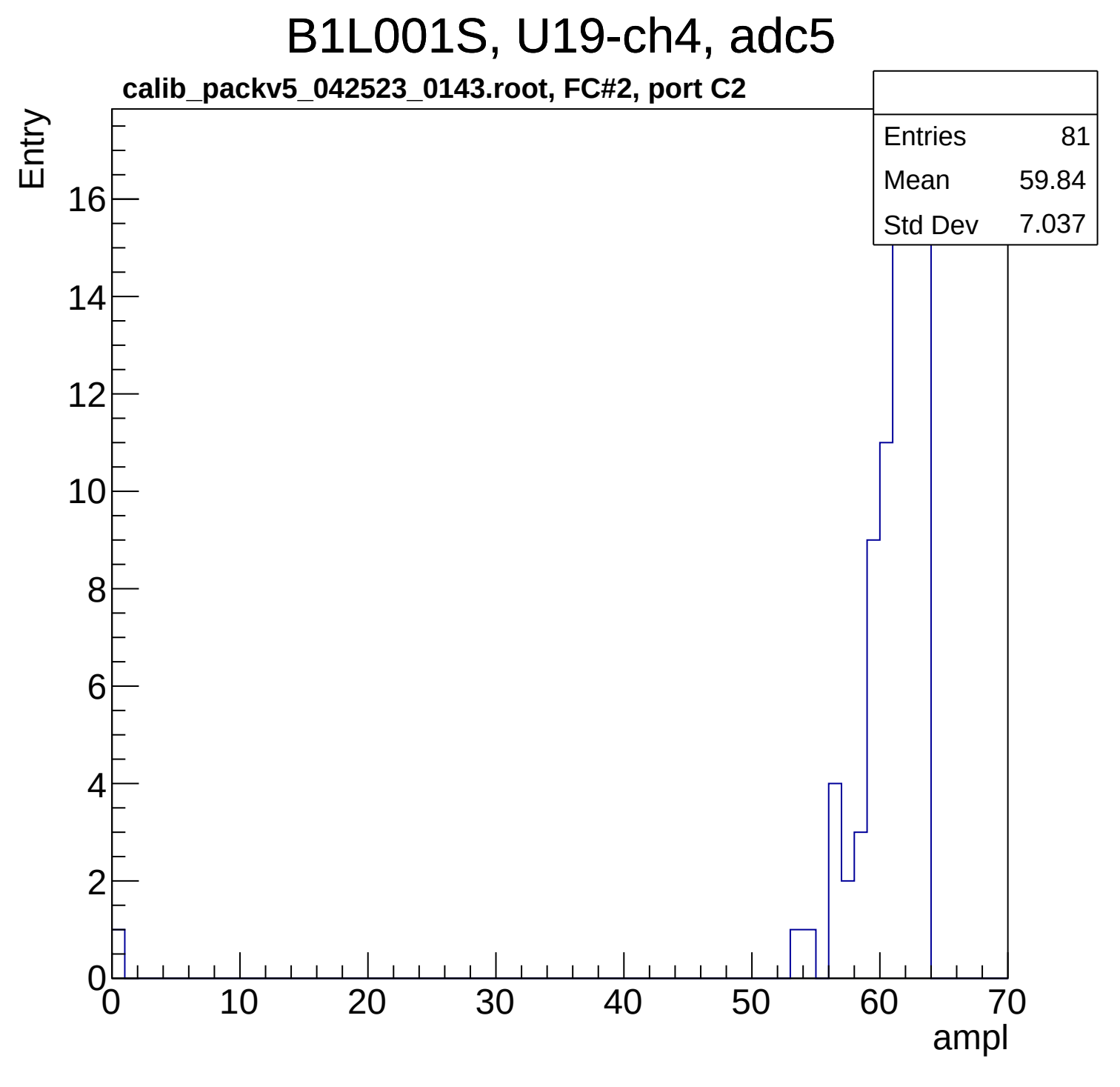
B1L001S, U19-ch4, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 81
Mean 59.84
Std Dev 7.037
Entry
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10
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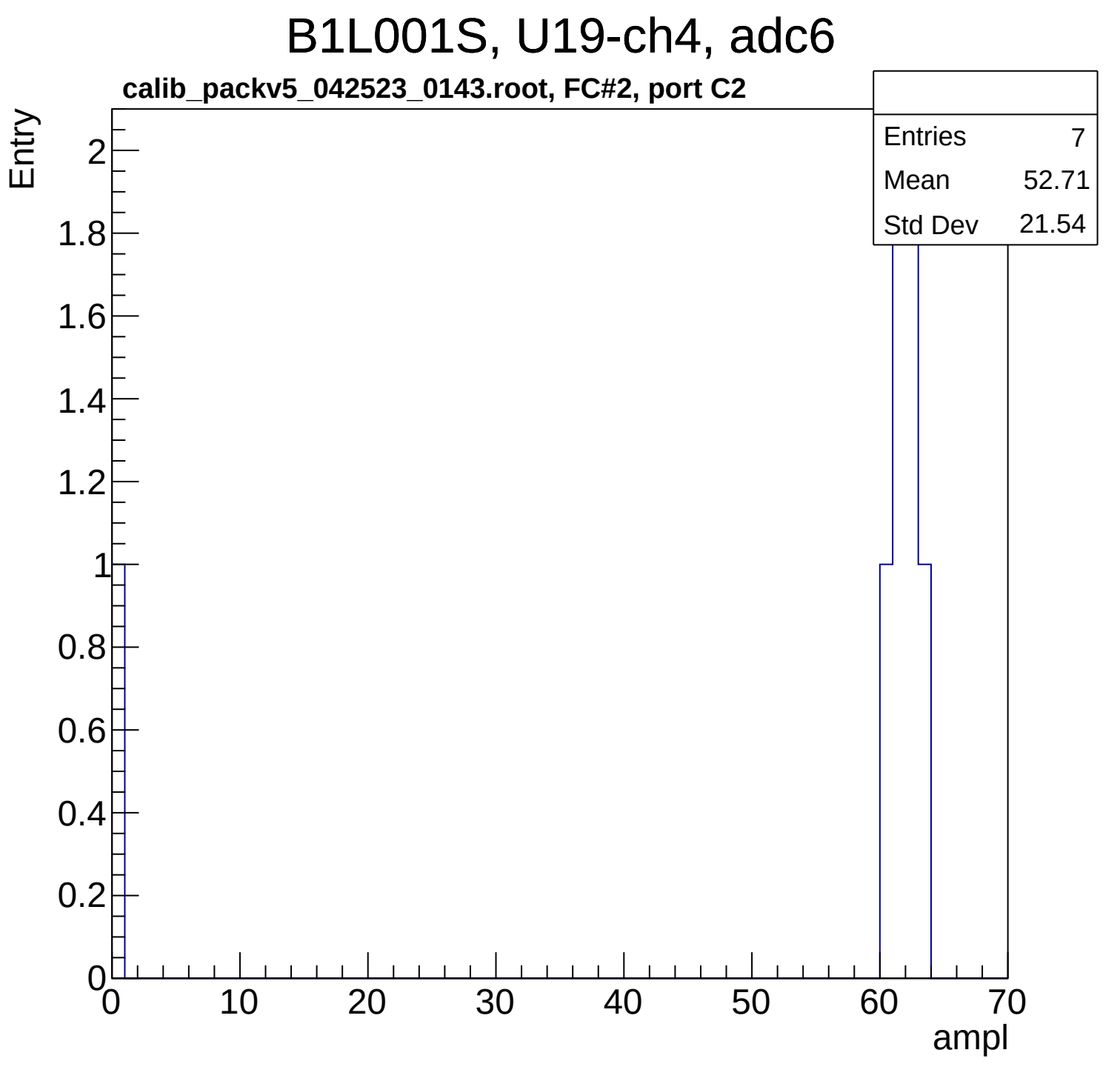
50
60
70
ampl


B1L001S, U19-ch4, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 7
Mean 52.71
Std Dev 21.54
Entry
ampl
0
0.2
0.4
0.6
0.8
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1.2
1.4
1.6
1.8
2
0
10
20
30
40
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60
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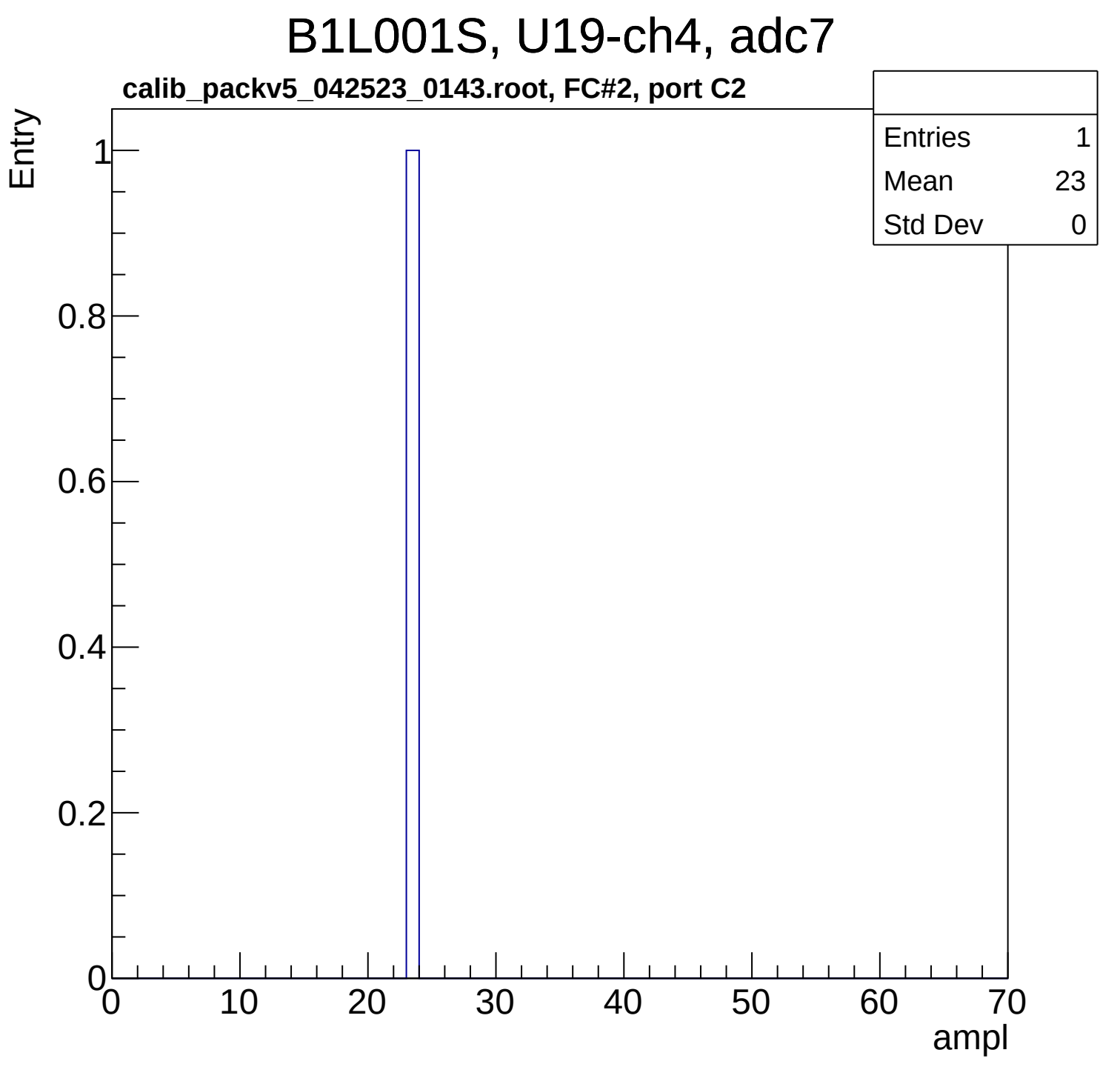
B1L001S, U19-ch4, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 23
Std Dev 0
Entry
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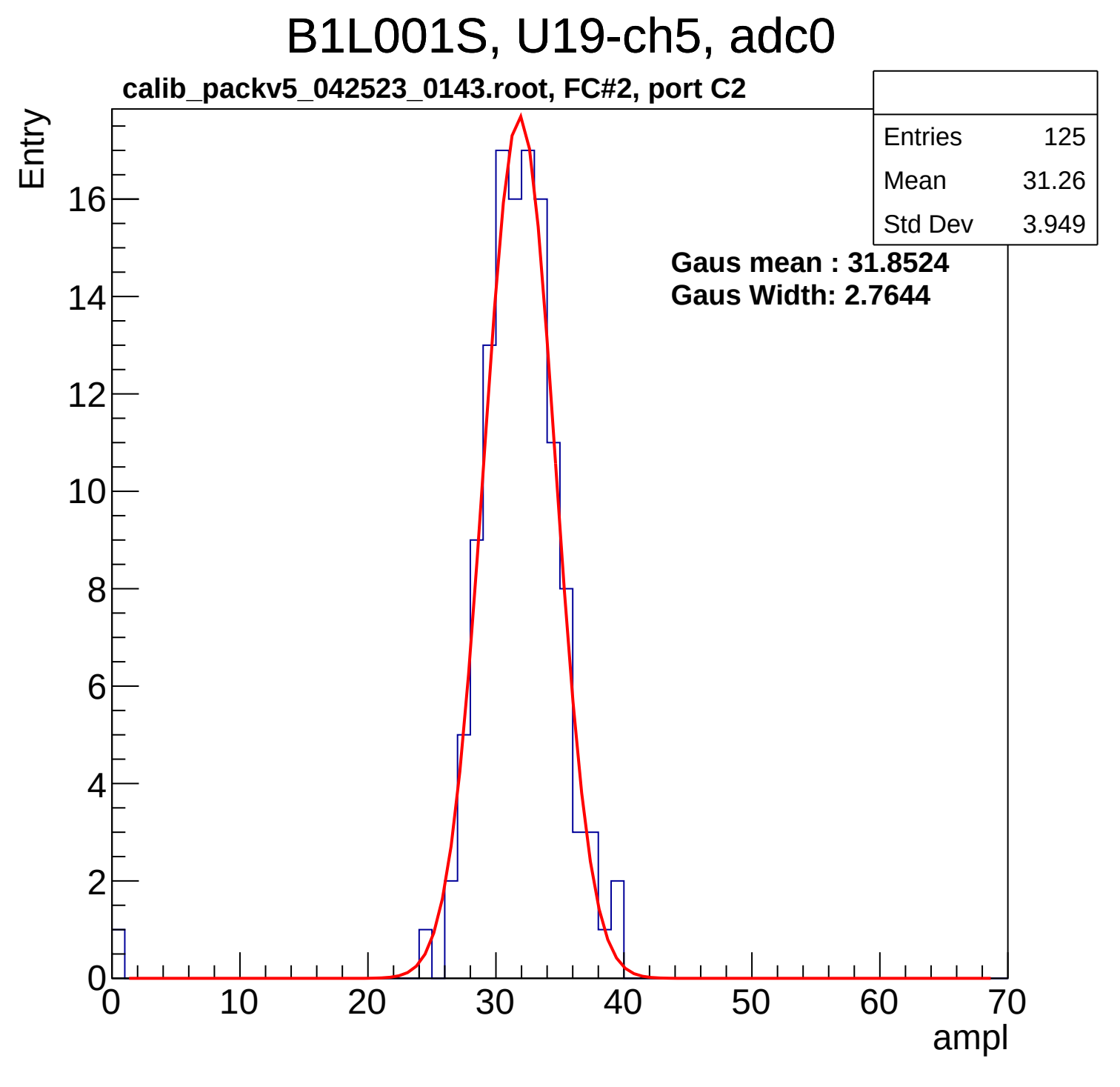
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch5, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 125
Mean 31.26
Std Dev 3.949
Gaus mean : 31.8524
Gaus Width: 2.7644
Entry
ampl
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2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
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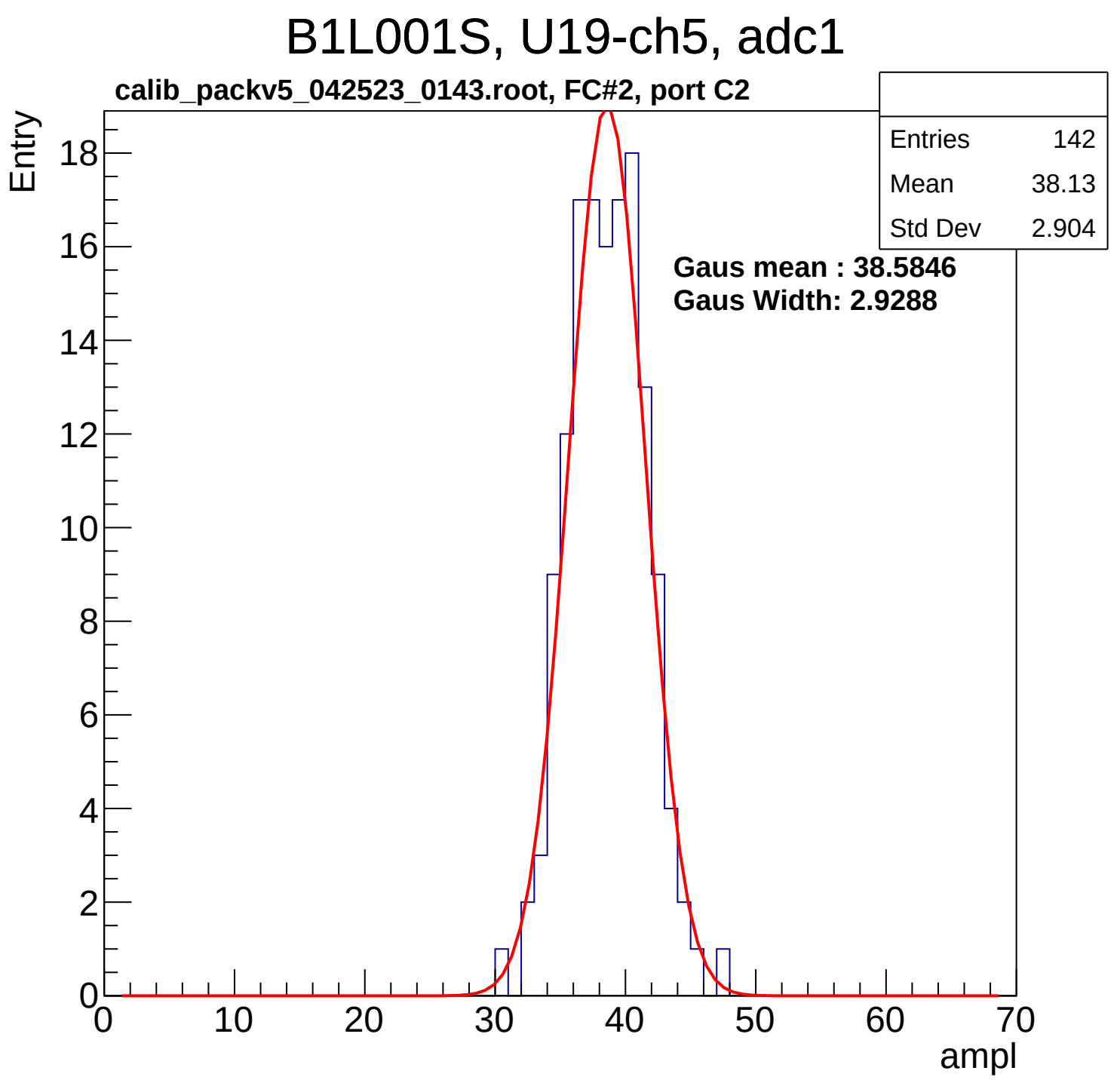
B1L001S, U19-ch5, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 142
Mean 38.13
Std Dev 2.904
Gaus mean : 38.5846
Gaus Width: 2.9288
Entry
ampl
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4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
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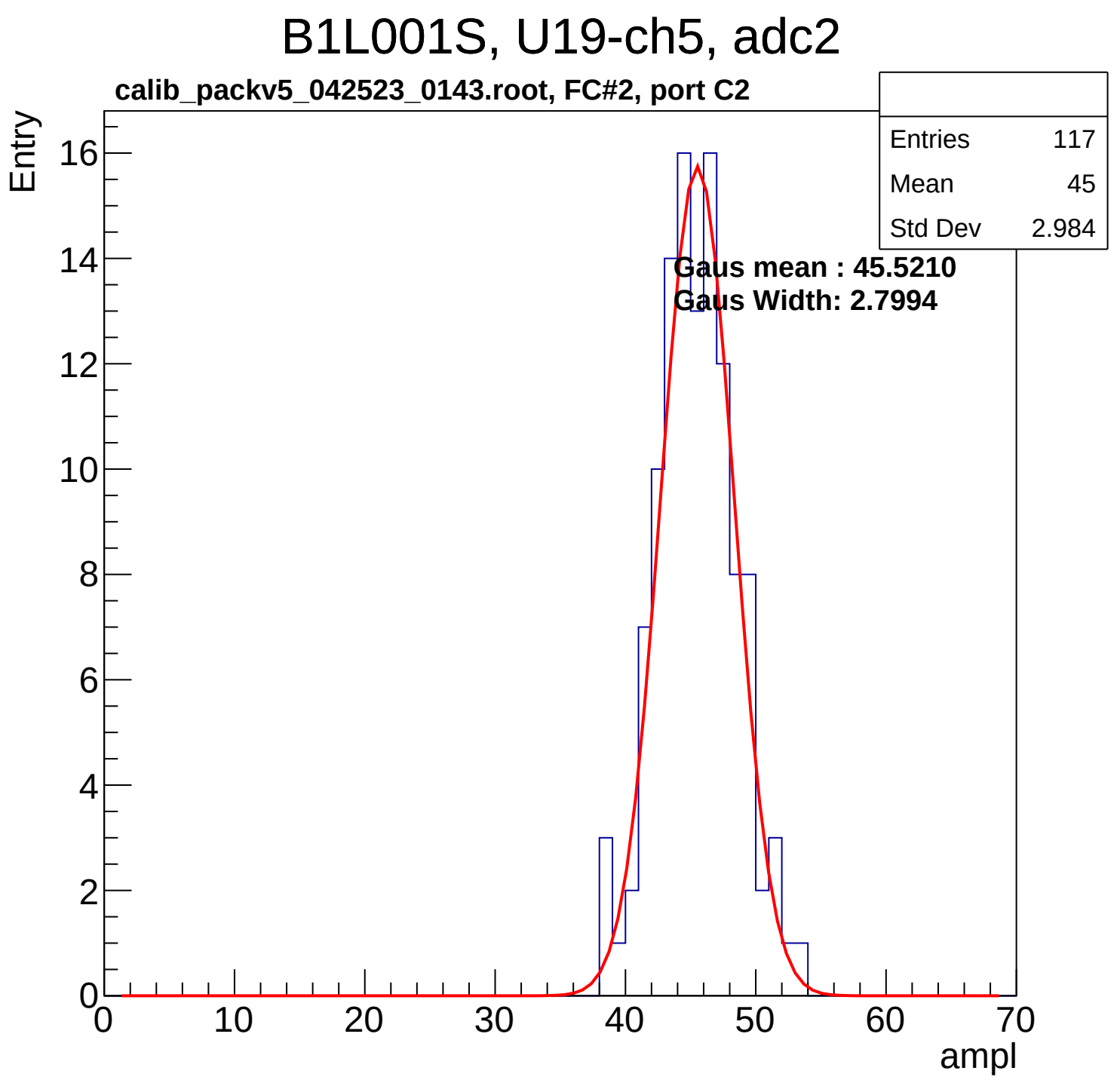
B1L001S, U19-ch5, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 117
Mean 45
Std Dev 2.984
Gaus mean : 45.5210
Gaus Width: 2.7994
Entry
ampl
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4
6
8
10
12
14
16
0
10
20
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40
50
60
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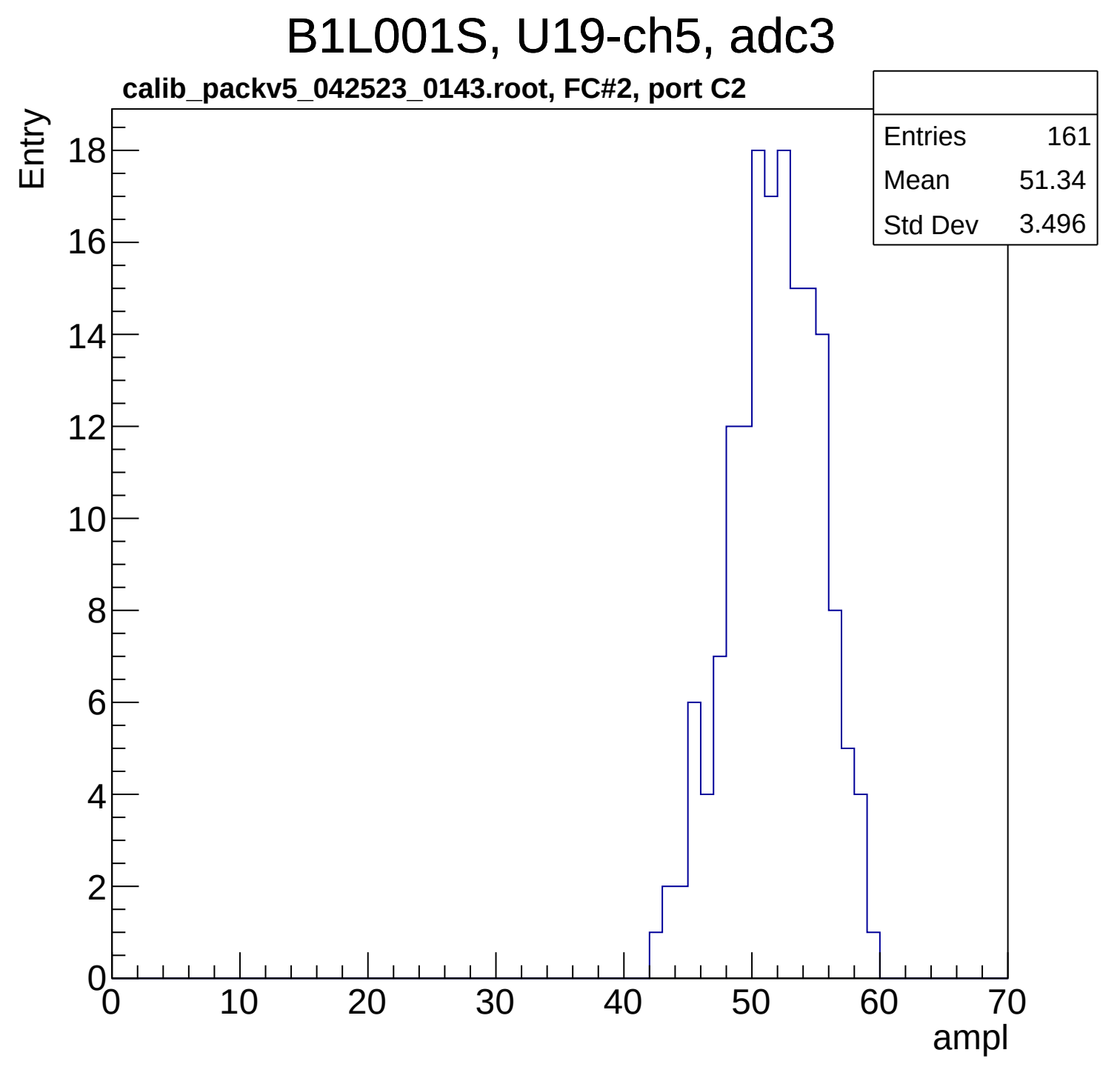
B1L001S, U19-ch5, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 161
Mean 51.34
Std Dev 3.496
Entry
ampl
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4
6
8
10
12
14
16
18
0
10
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60
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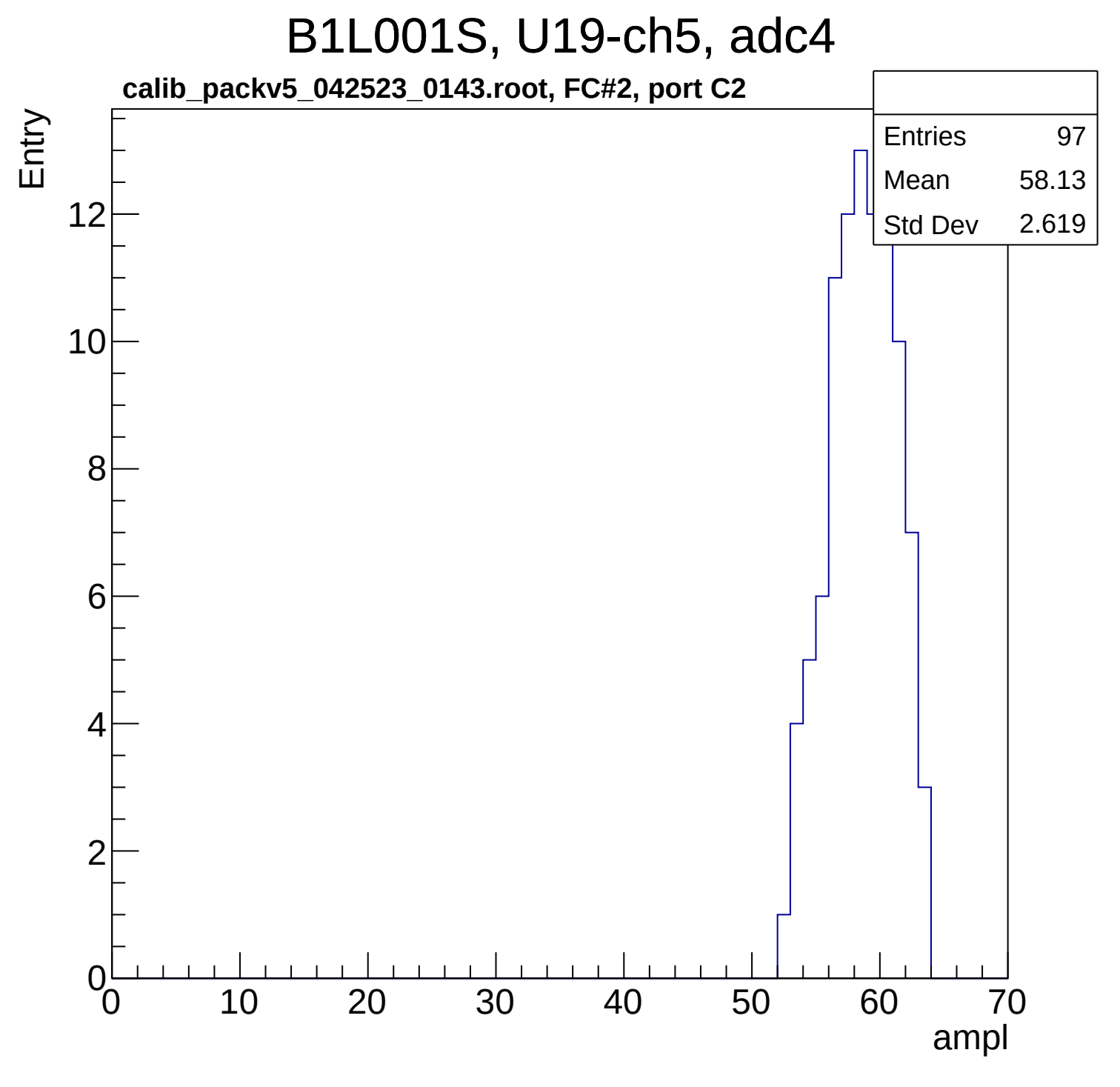
B1L001S, U19-ch5, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 97
Mean 58.13
Std Dev 2.619
Entry
0
2
4
6
8
10
12
0
10
20
30
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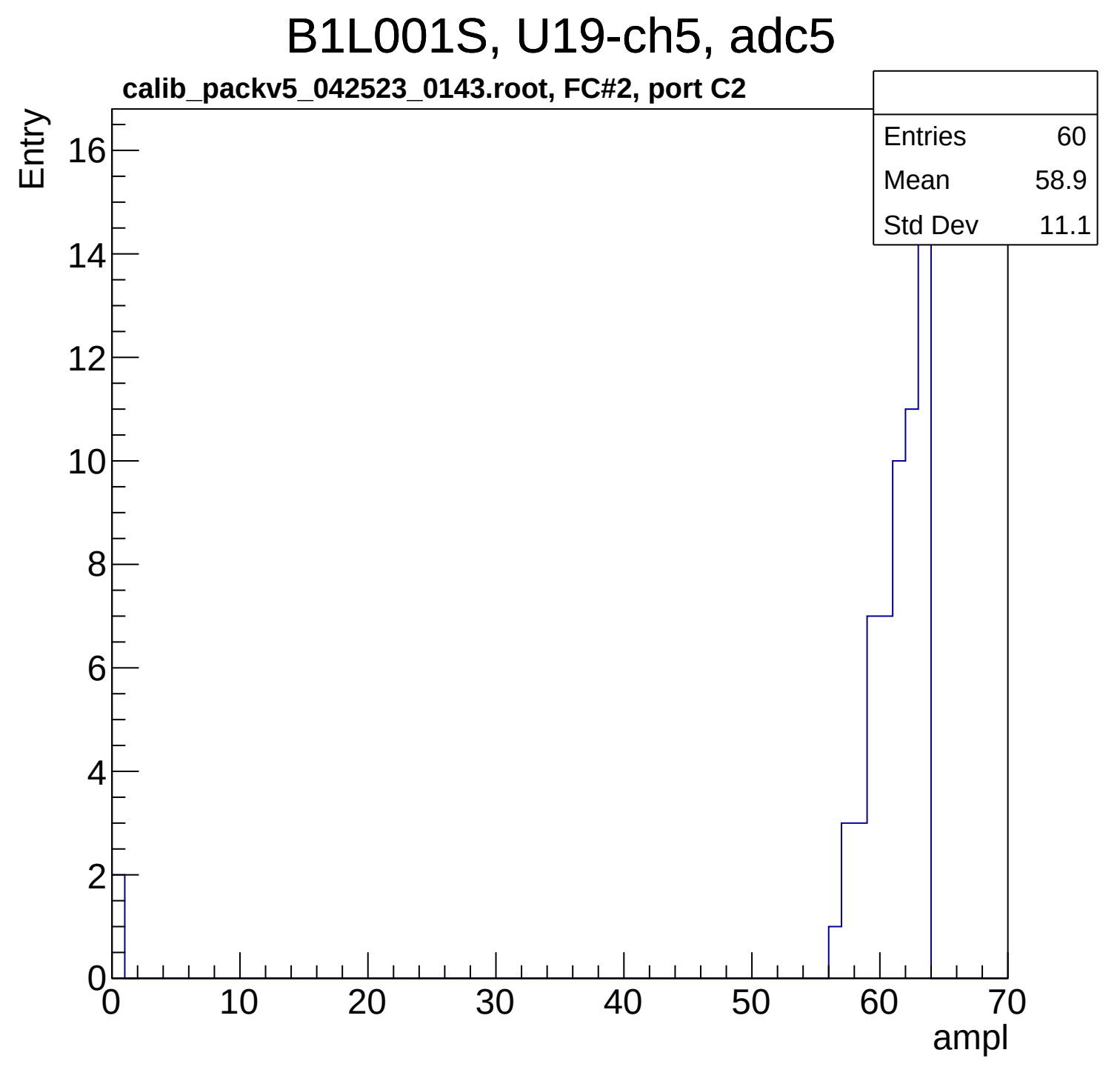
50
60
70
ampl


B1L001S, U19-ch5, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 60
Mean 58.9
Std Dev 11.1
Entry
0
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4
6
8
10
12
14
16
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10
20
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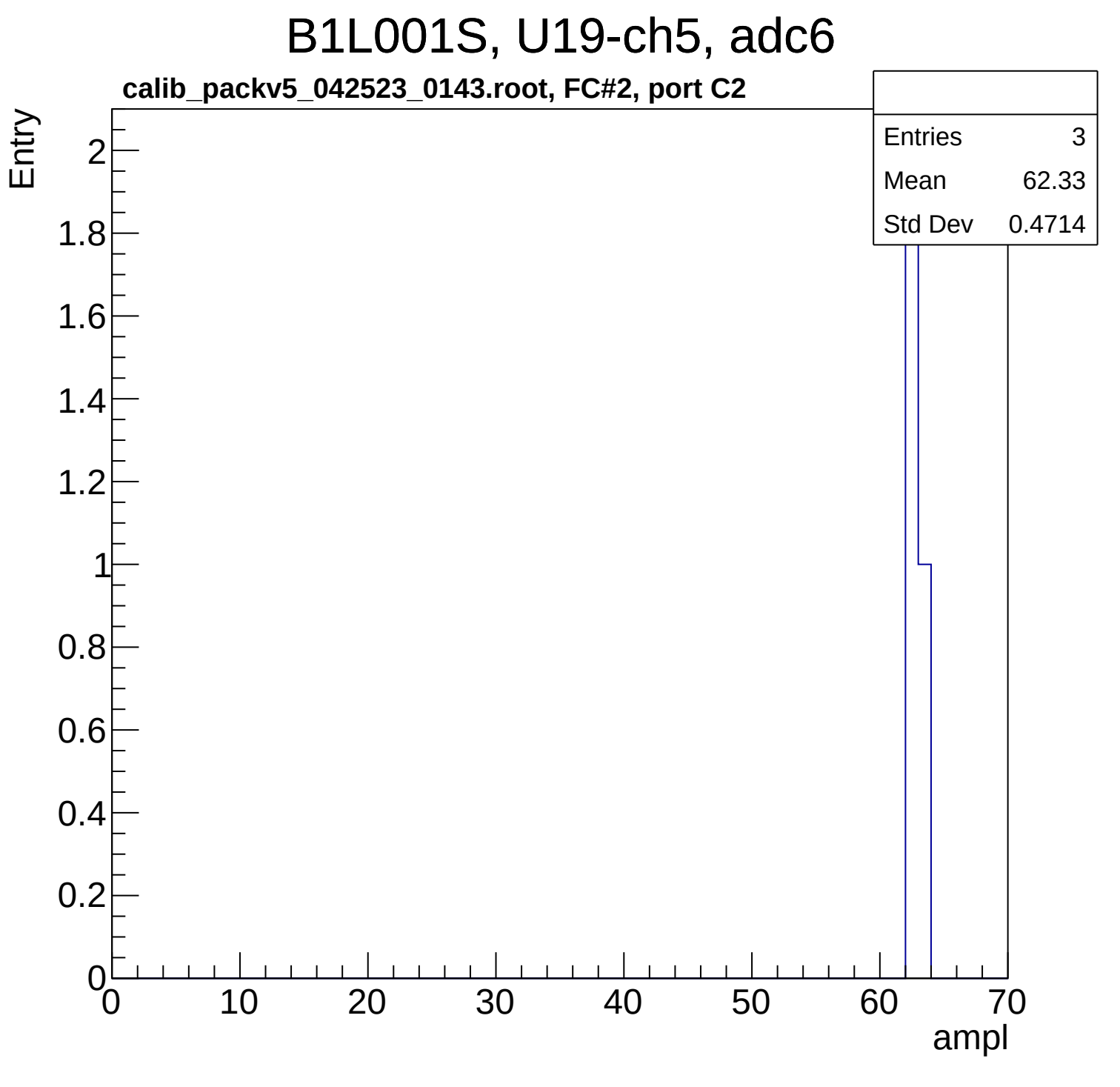
70
ampl


B1L001S, U19-ch5, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 3
Mean 62.33
Std Dev 0.4714
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
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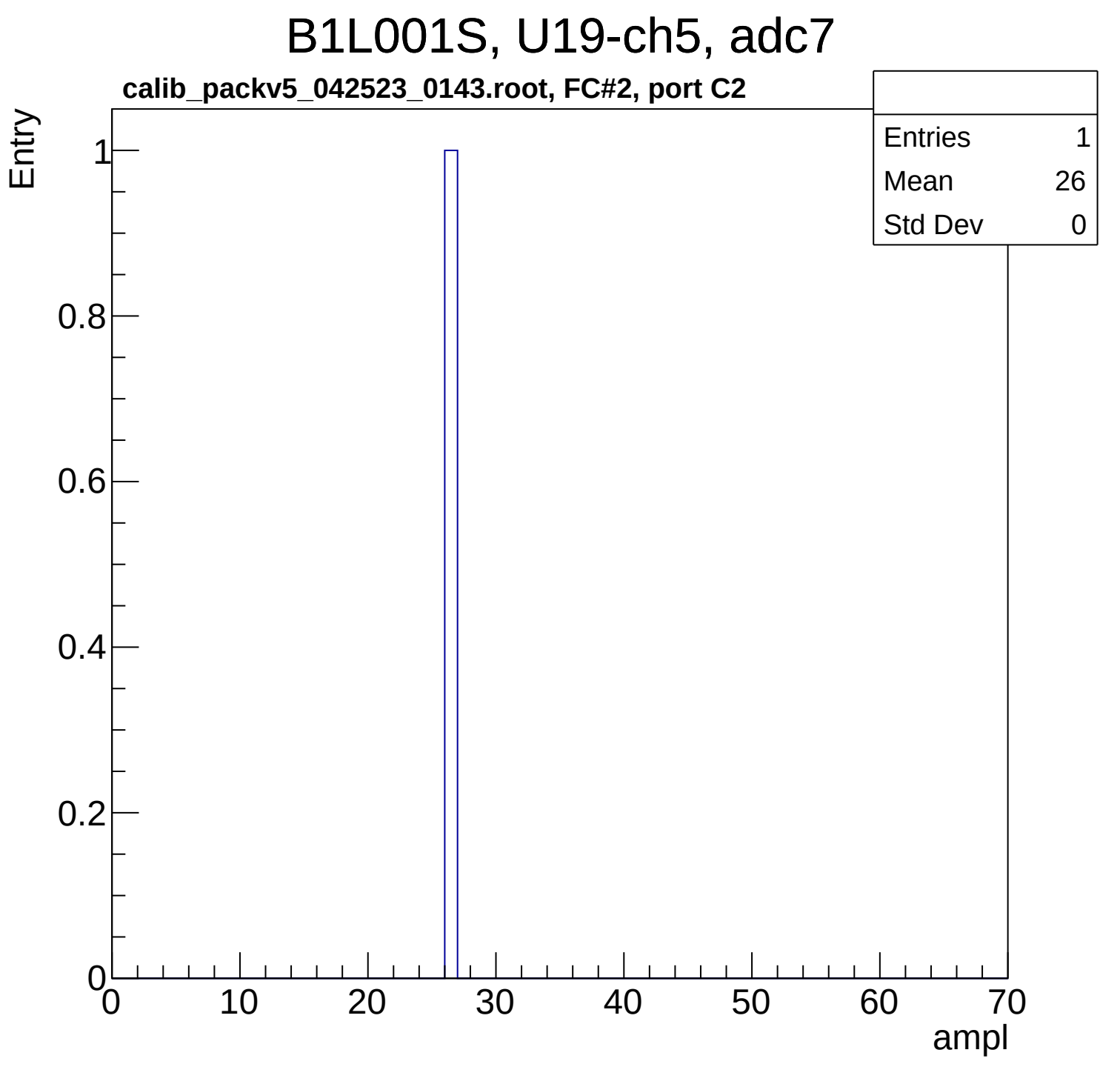
B1L001S, U19-ch5, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 26
Std Dev 0
Entry
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0.6
0.4
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10
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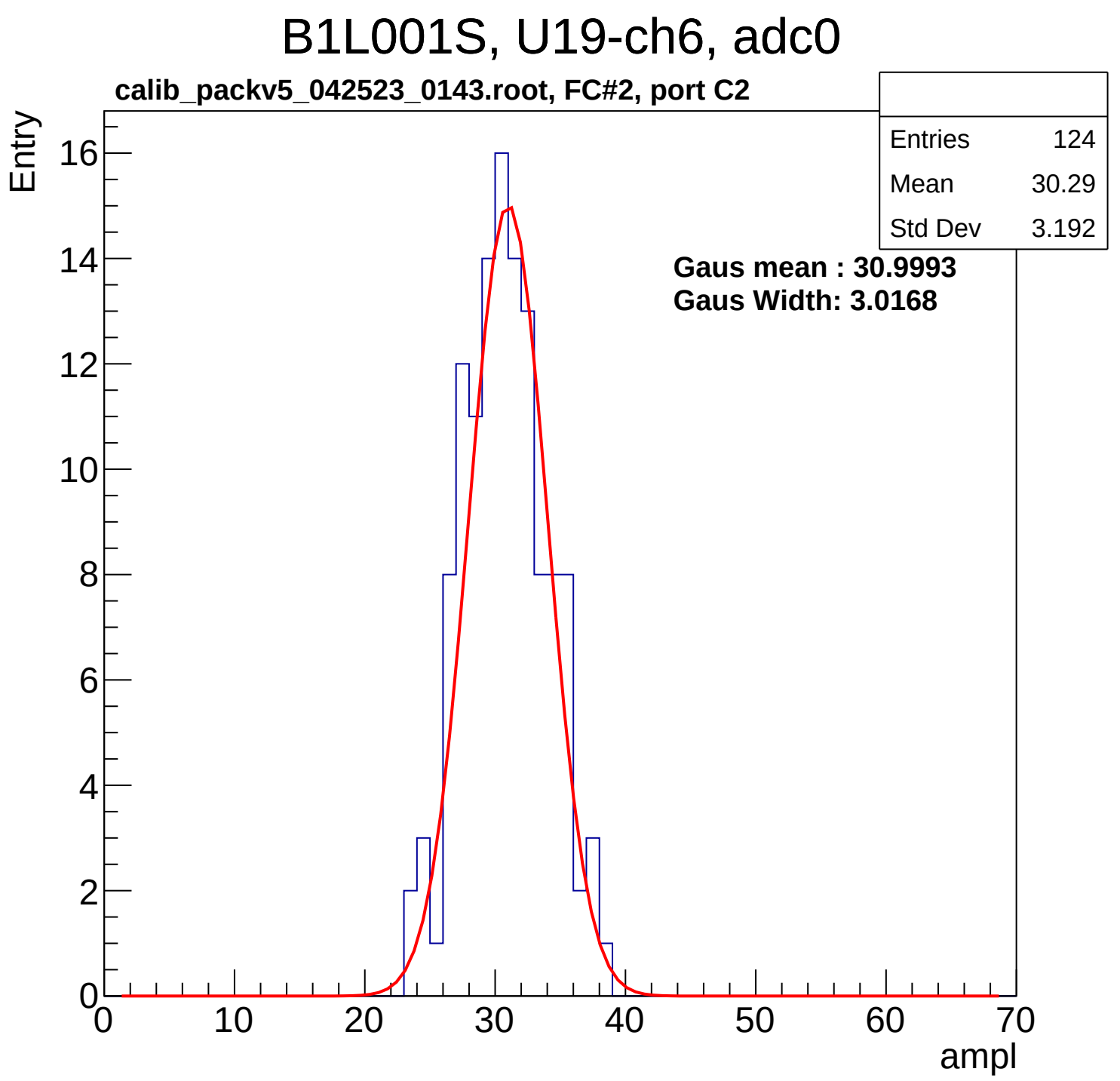
60
70
ampl


B1L001S, U19-ch6, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 124
Mean 30.29
Std Dev 3.192
Gaus mean : 30.9993
Gaus Width: 3.0168
Entry
ampl
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4
6
8
10
12
14
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0
10
20
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60
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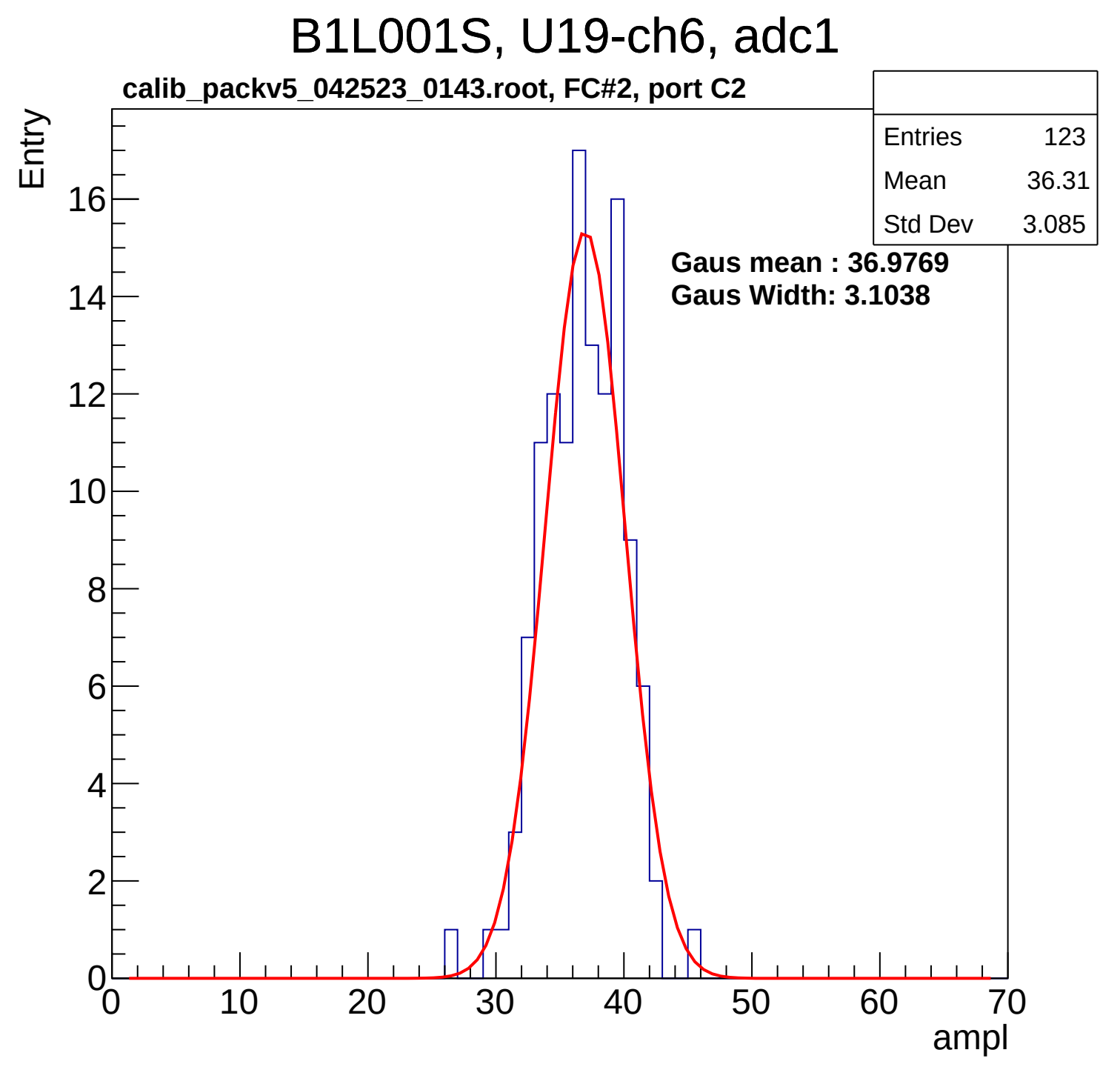
B1L001S, U19-ch6, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 123
Mean 36.31
Std Dev 3.085
Gaus mean : 36.9769
Gaus Width: 3.1038
Entry
ampl
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2
4
6
8
10
12
14
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0
10
20
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50
60
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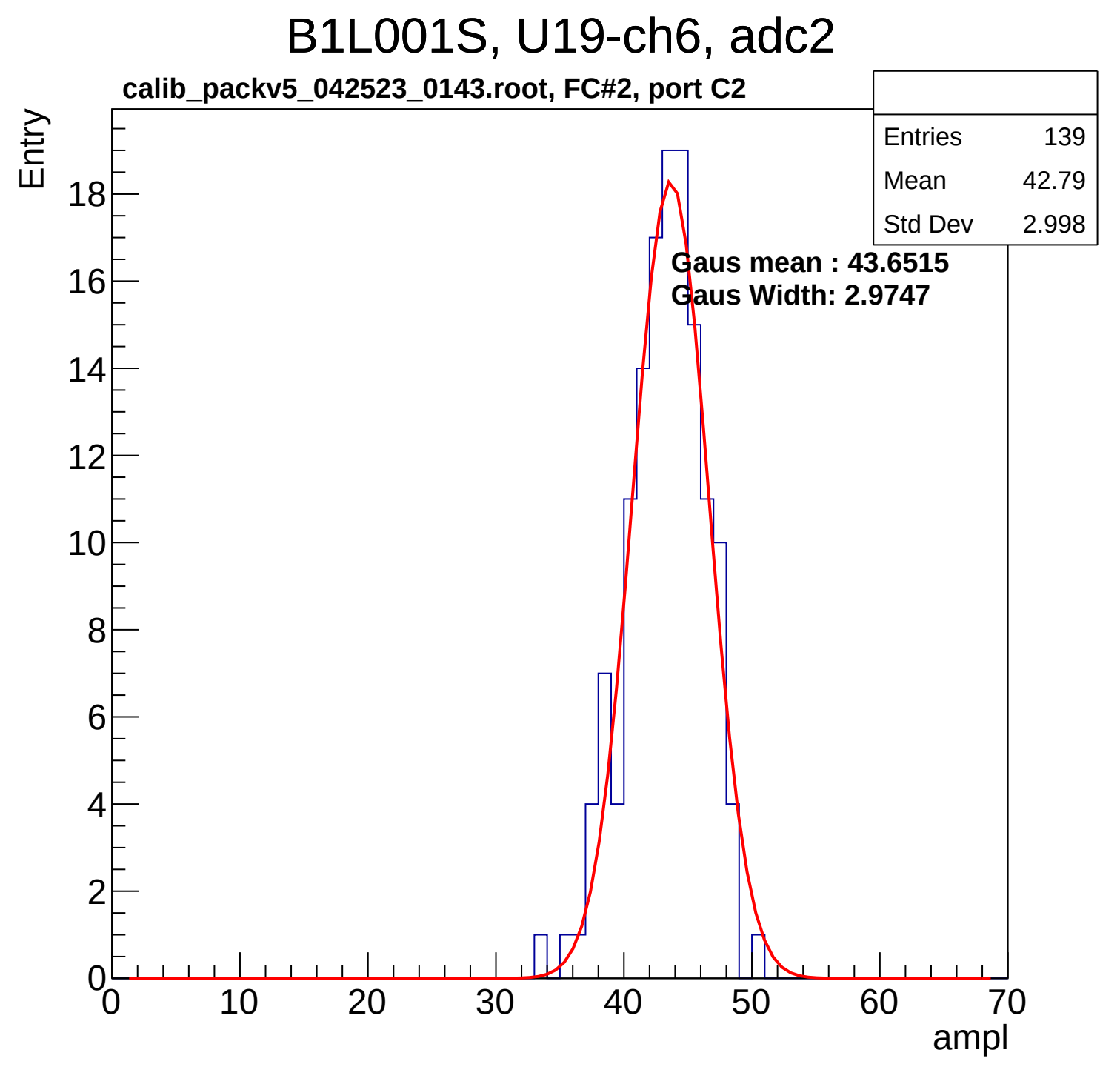
B1L001S, U19-ch6, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 139
Mean 42.79
Std Dev 2.998
Gaus mean : 43.6515
Gaus Width: 2.9747
Entry
ampl
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4
6
8
10
12
14
16
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0
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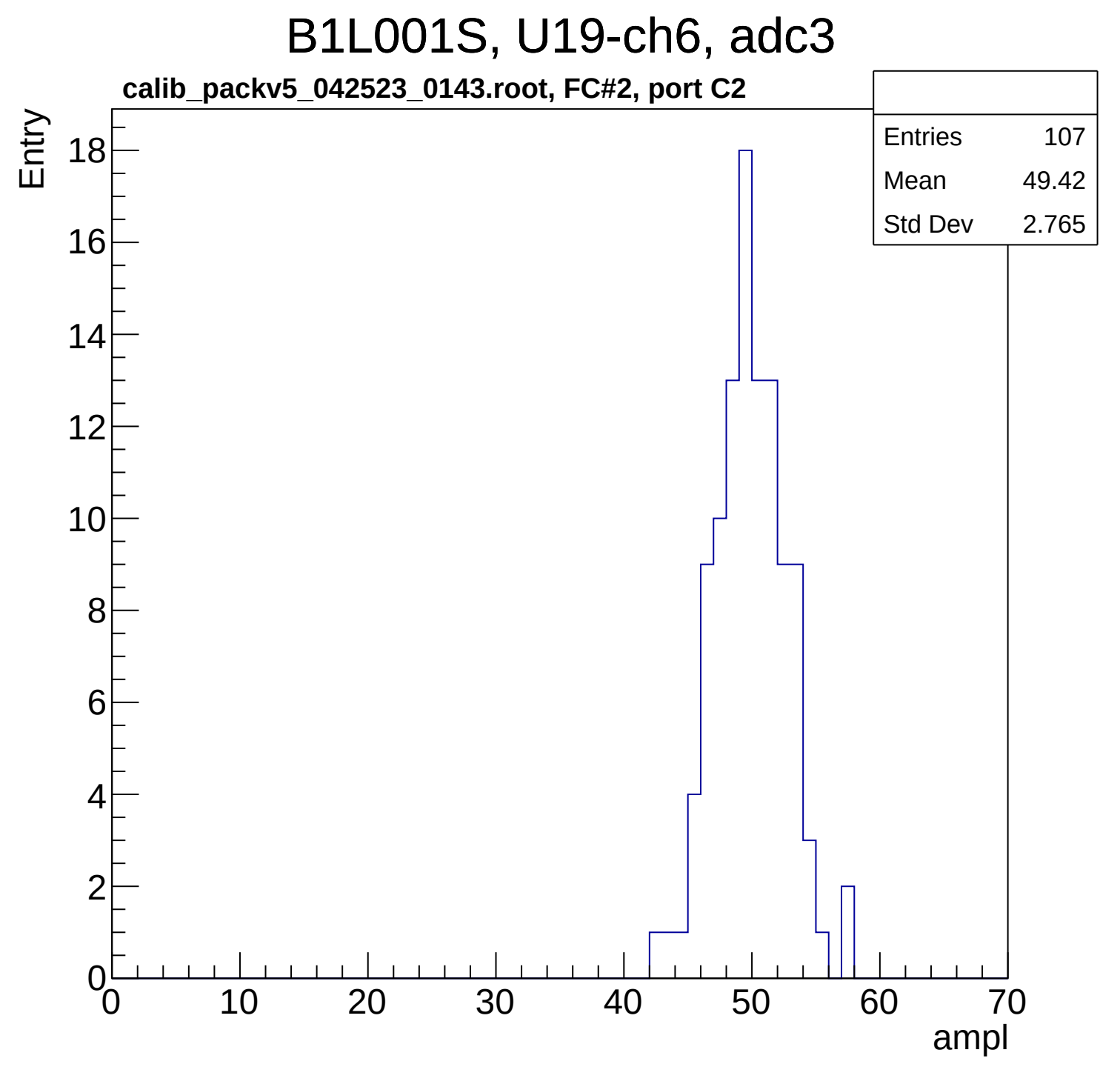
B1L001S, U19-ch6, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 107
Mean 49.42
Std Dev 2.765
Entry
ampl
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10
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14
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0
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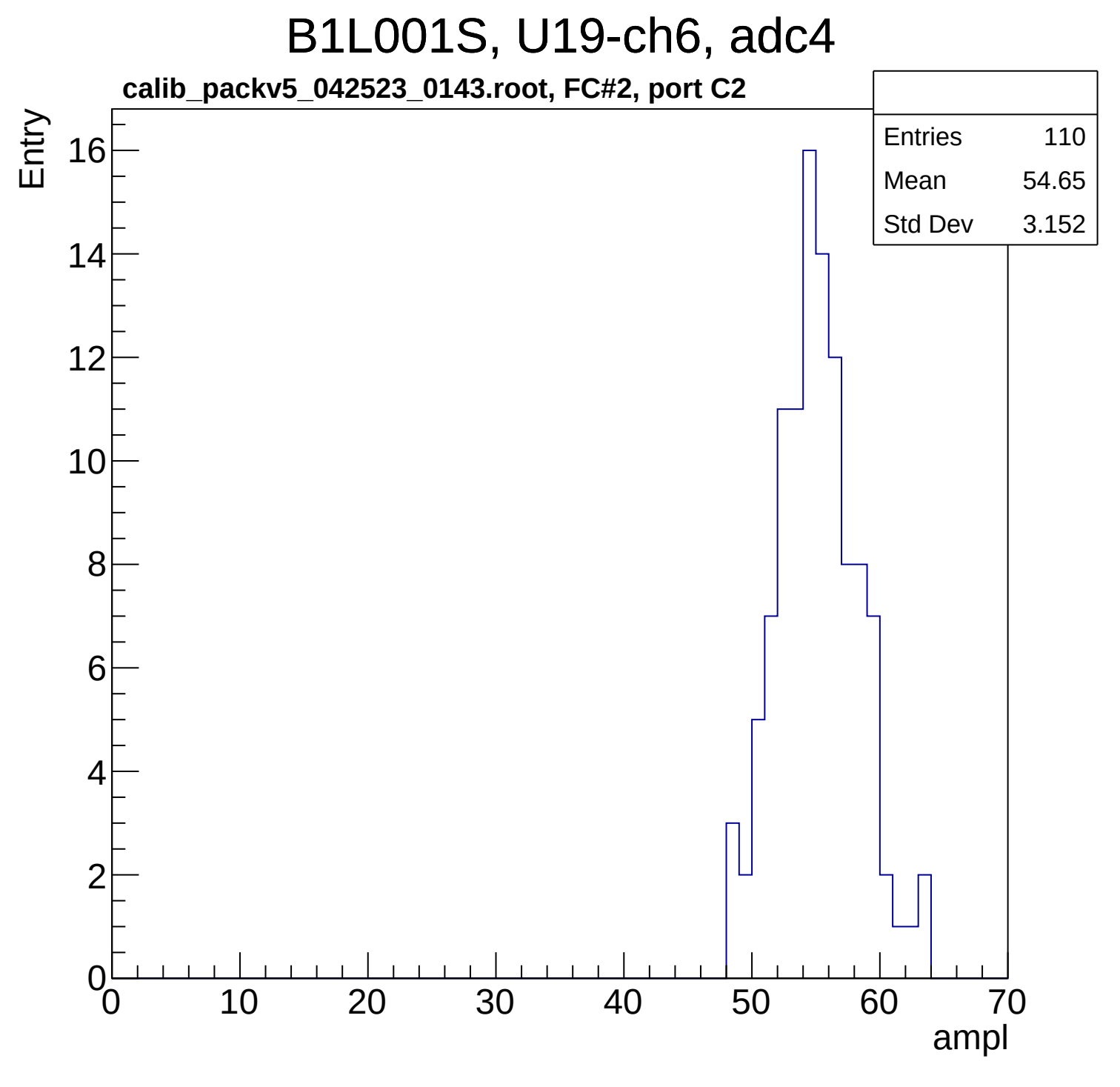
B1L001S, U19-ch6, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 110
Mean 54.65
Std Dev 3.152
Entry
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4
6
8
10
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14
16
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10
20
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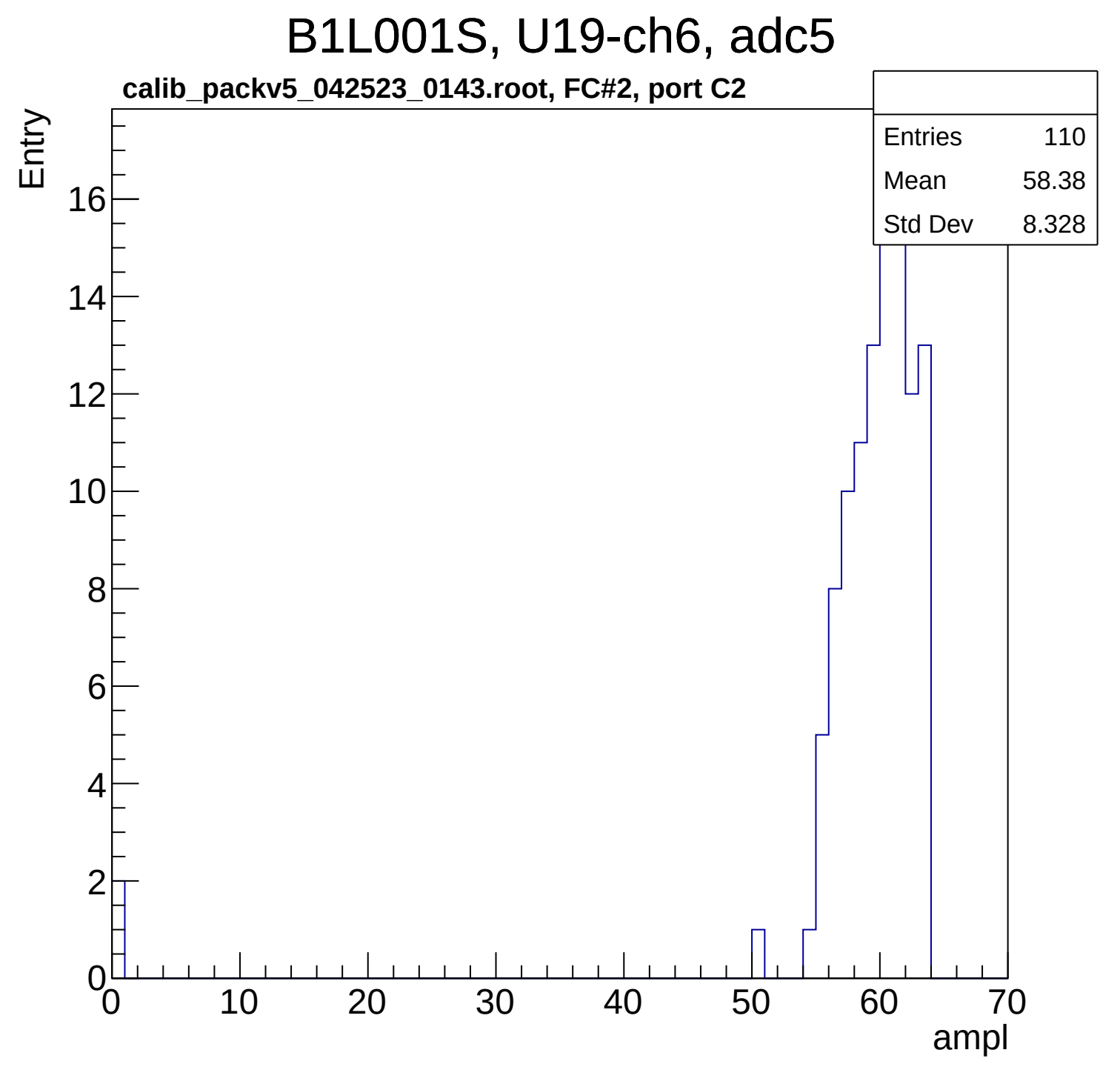
70
ampl


B1L001S, U19-ch6, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 110
Mean 58.38
Std Dev 8.328
Entry
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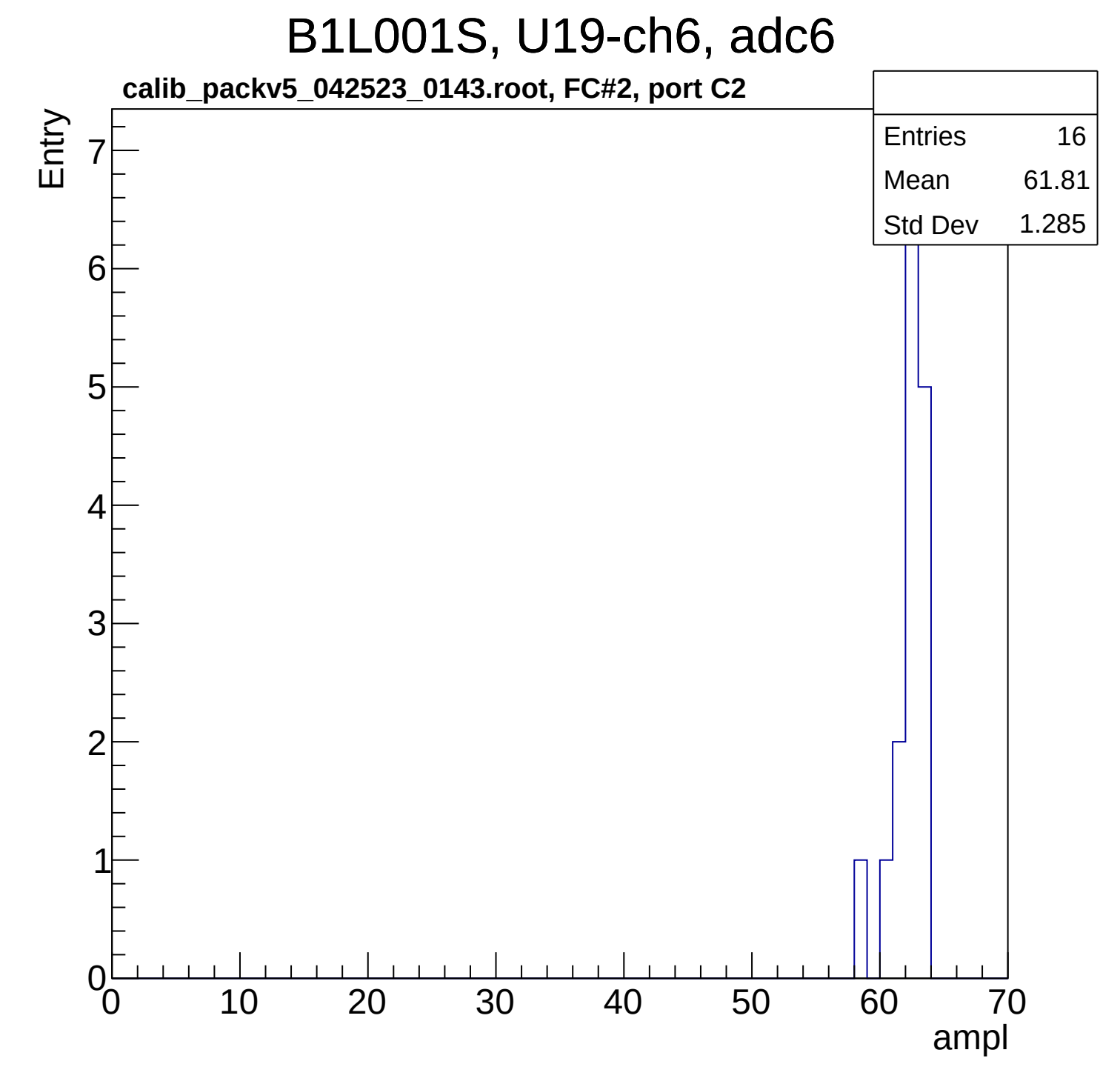
ampl


B1L001S, U19-ch6, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 16
Mean 61.81
Std Dev 1.285
Entry
ampl
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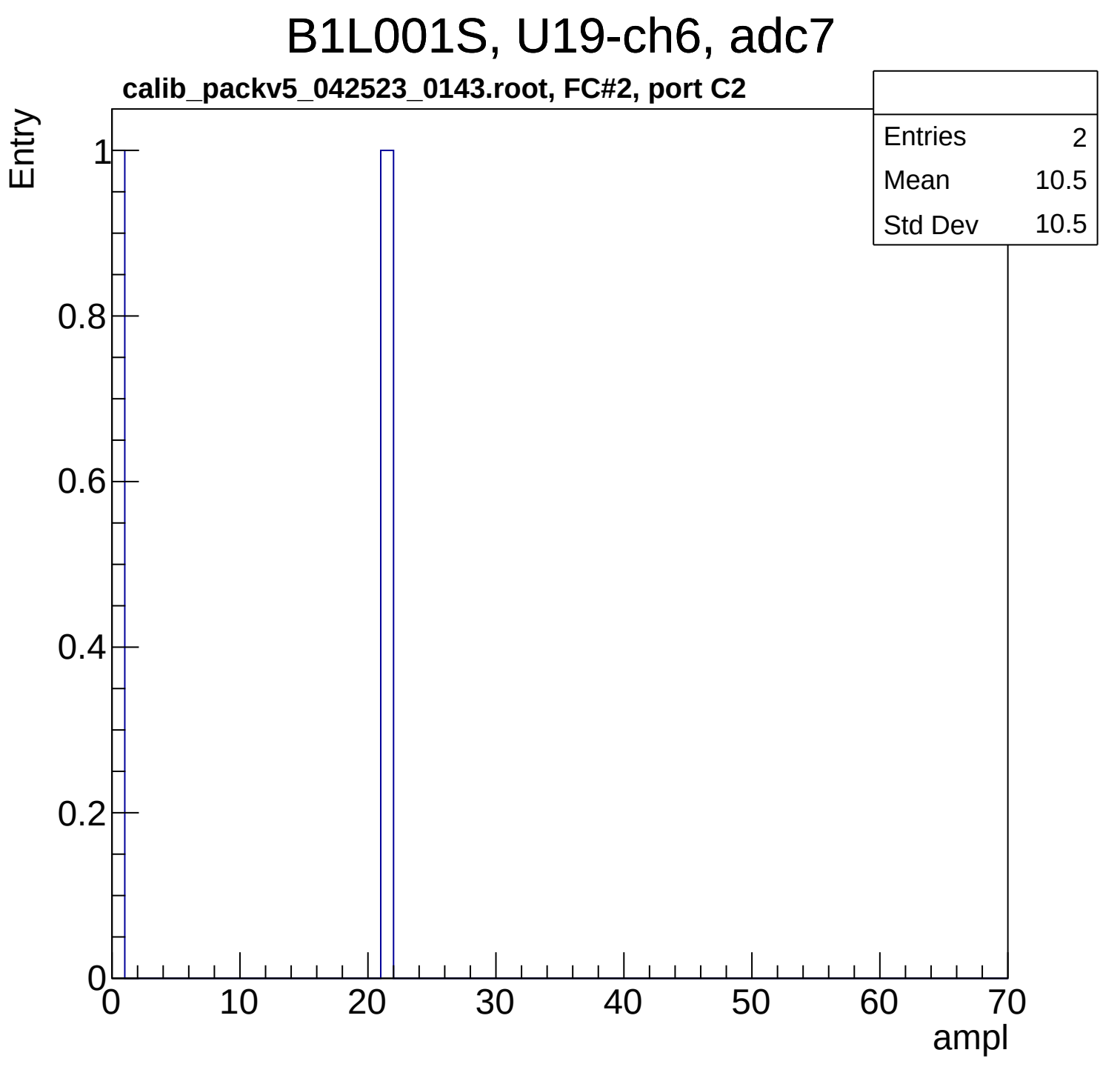
B1L001S, U19-ch6, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 10.5
Std Dev 10.5
Entry
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0.6
0.4
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0
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10
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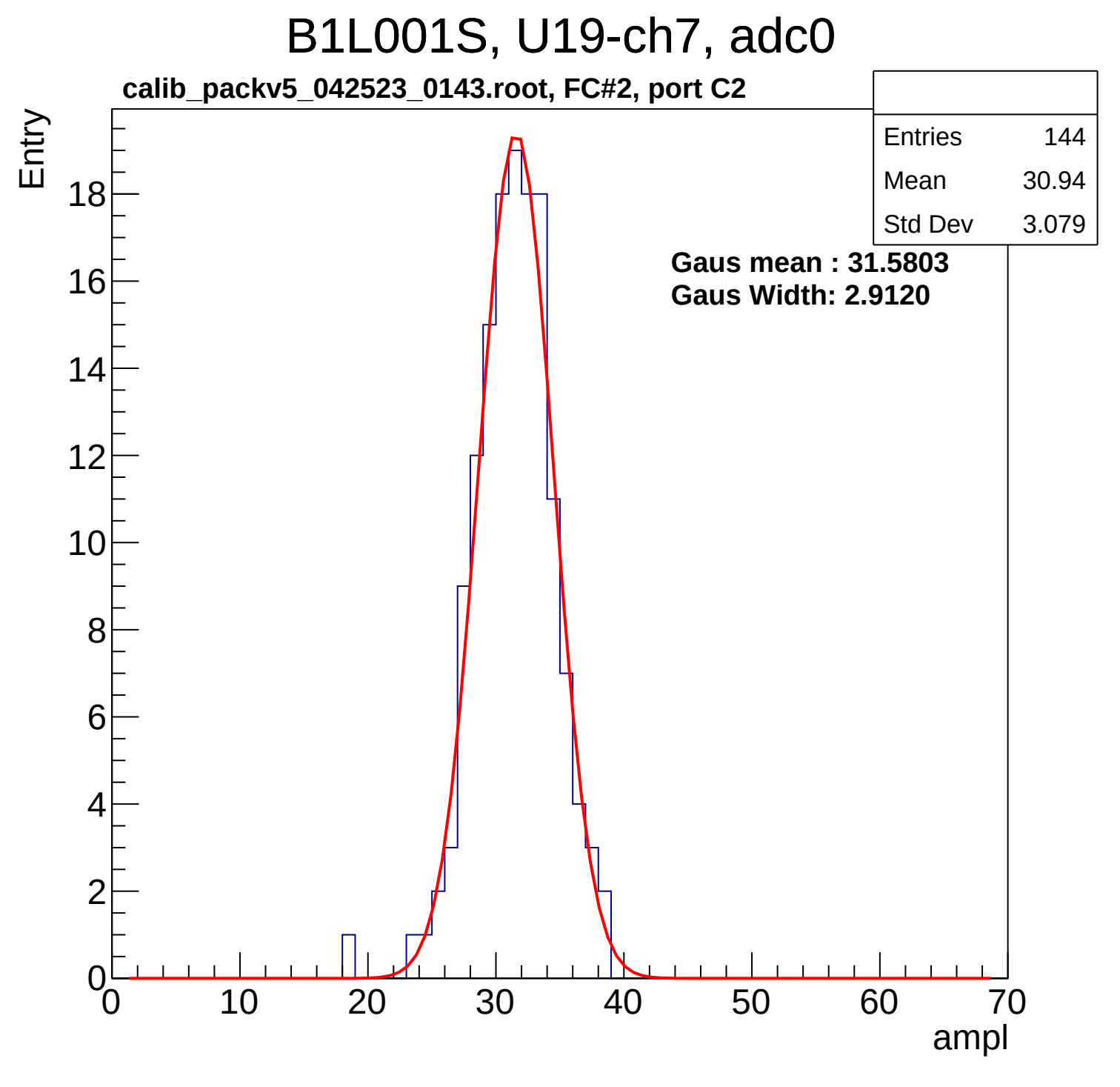
50
60
70
ampl


B1L001S, U19-ch7, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 144
Mean 30.94
Std Dev 3.079
Gaus mean : 31.5803
Gaus Width: 2.9120
Entry
ampl
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4
6
8
10
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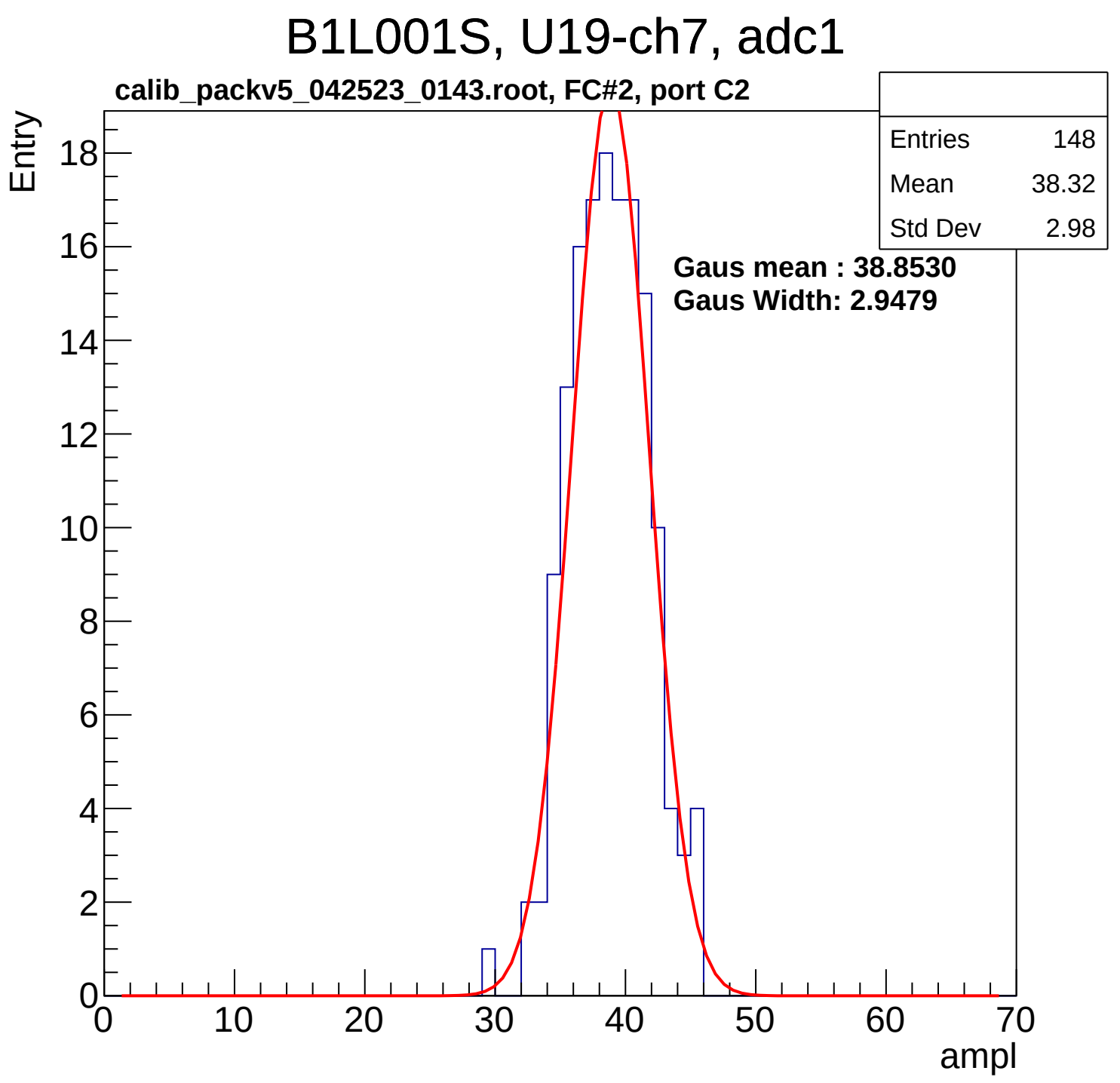
B1L001S, U19-ch7, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 148
Mean 38.32
Std Dev 2.98
Gaus mean : 38.8530
Gaus Width: 2.9479
Entry
ampl
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4
6
8
10
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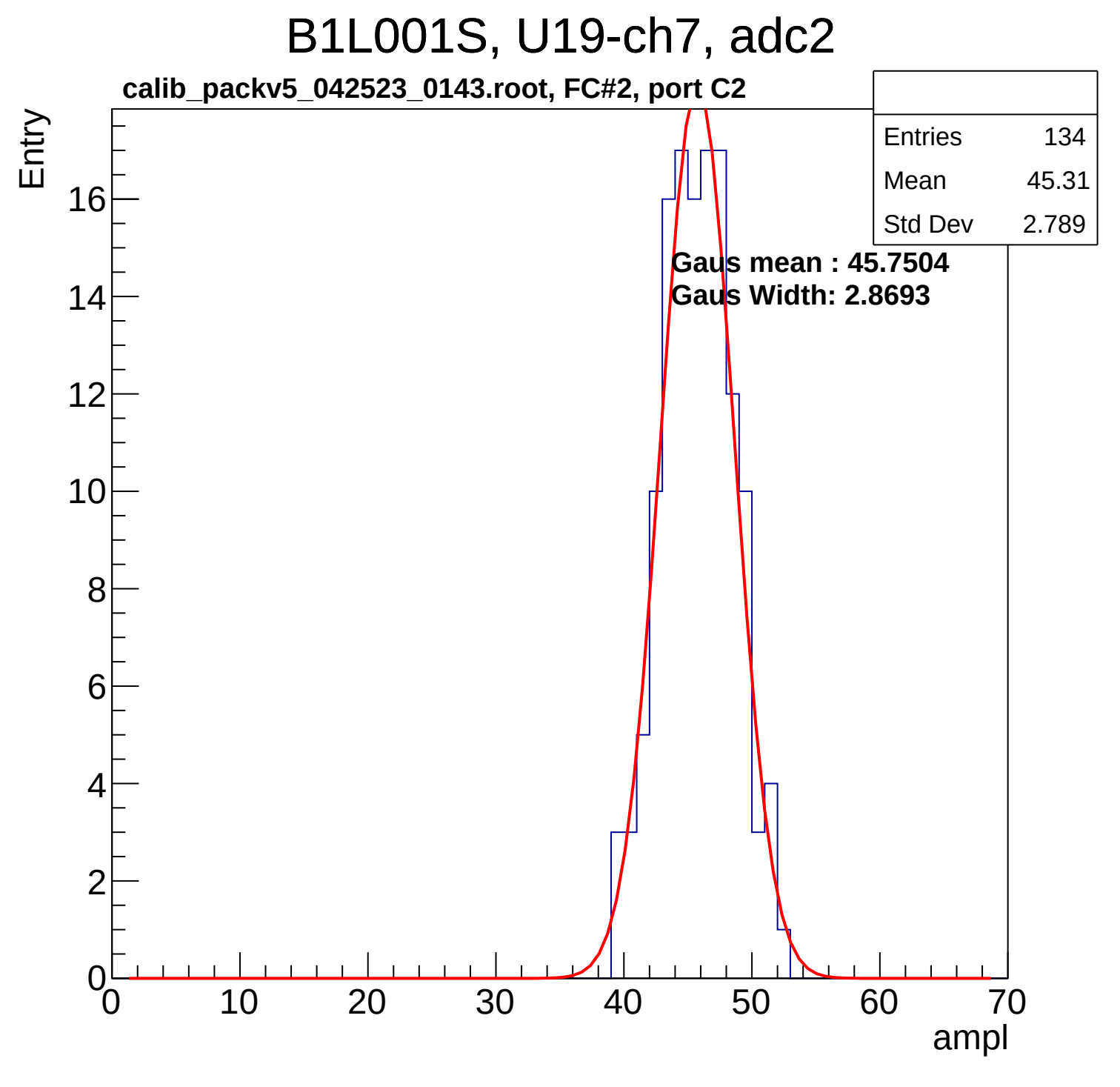
B1L001S, U19-ch7, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 134
Mean 45.31
Std Dev 2.789
Gaus mean : 45.7504
Gaus Width: 2.8693
Entry
ampl
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2
4
6
8
10
12
14
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10
20
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40
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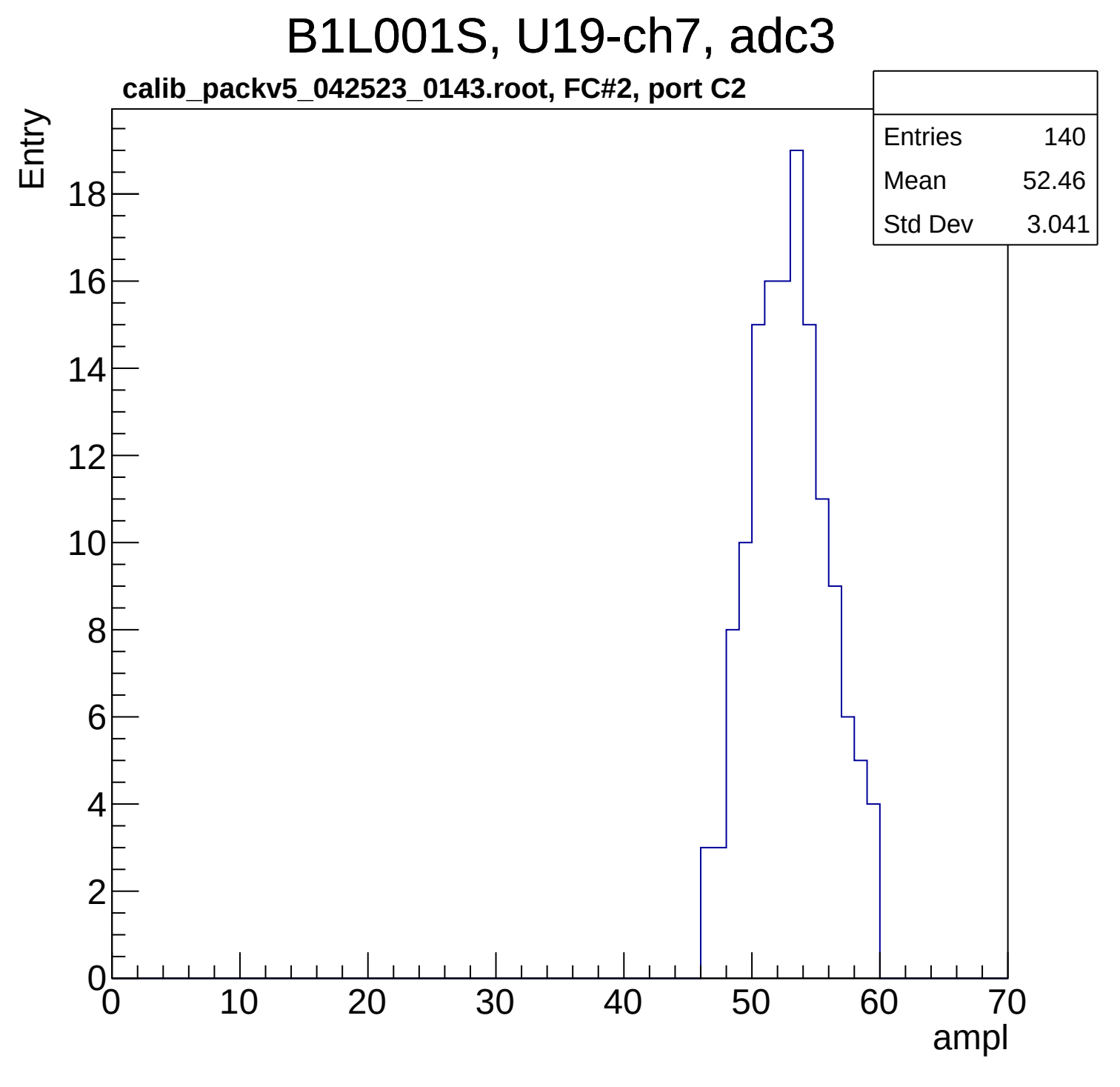
B1L001S, U19-ch7, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 140
Mean 52.46
Std Dev 3.041
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
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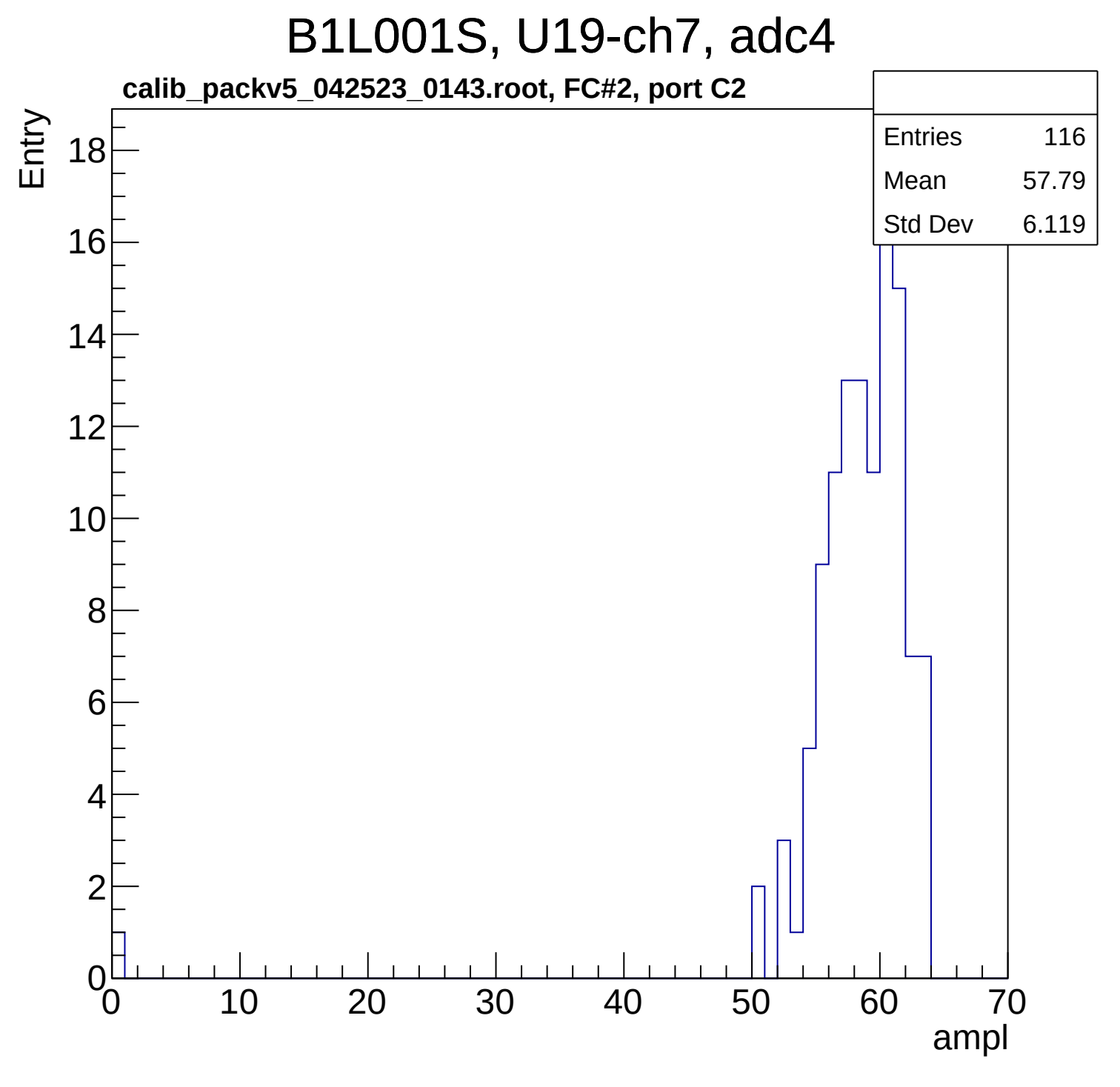
B1L001S, U19-ch7, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 116
Mean 57.79
Std Dev 6.119
Entry
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6
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14
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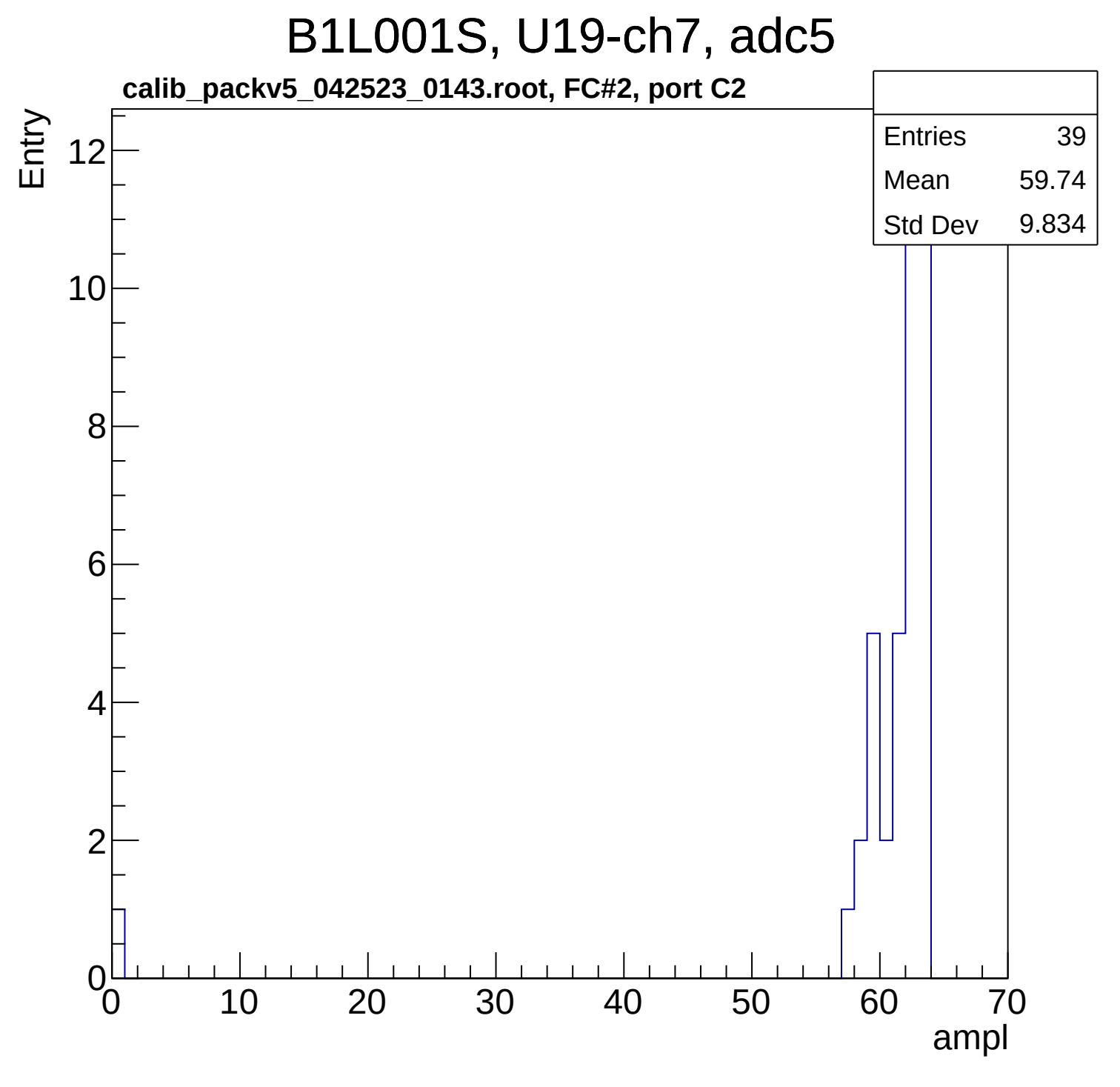
ampl


B1L001S, U19-ch7, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 39
Mean 59.74
Std Dev 9.834
Entry
ampl
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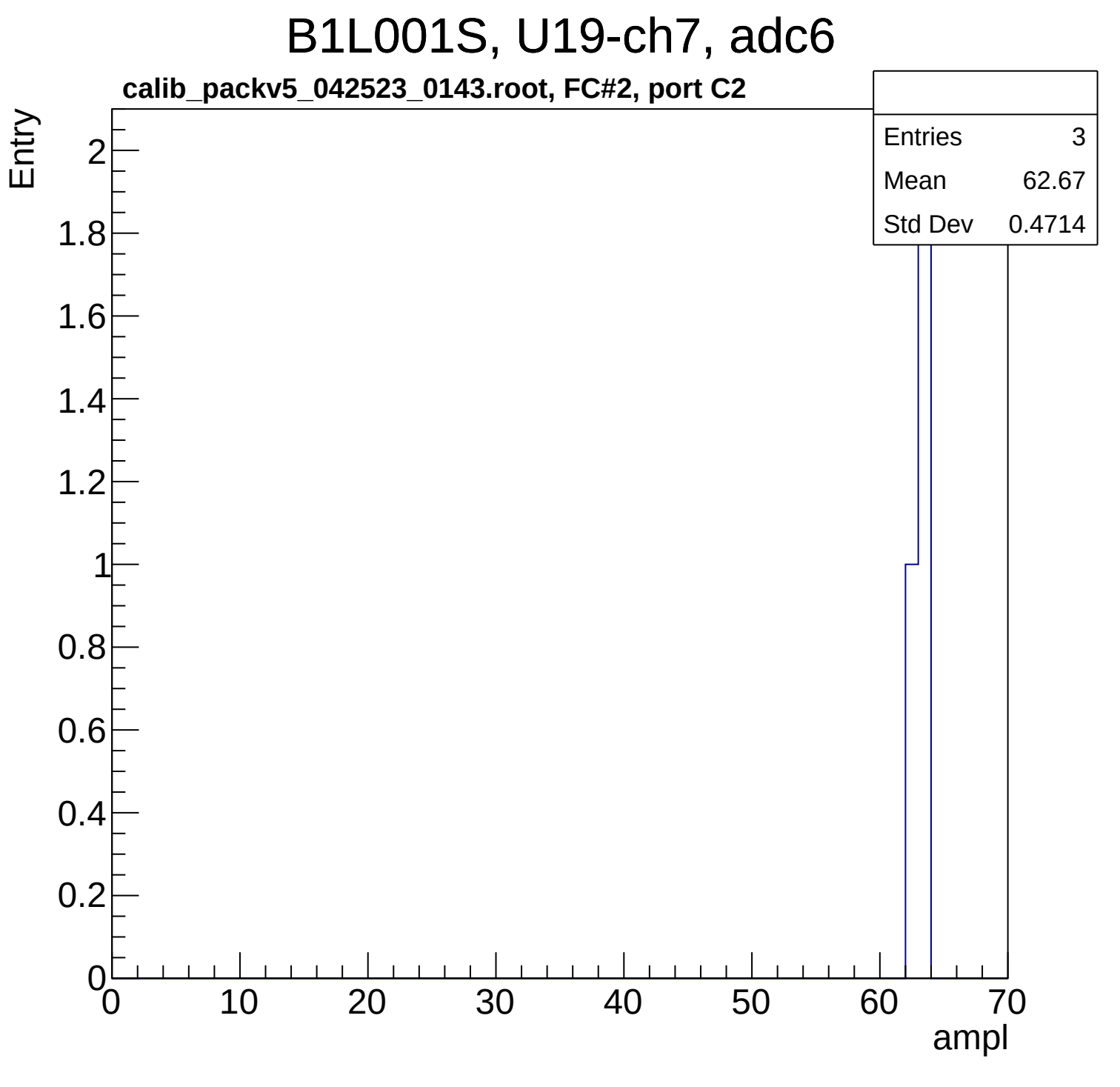
B1L001S, U19-ch7, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 3
Mean 62.67
Std Dev 0.4714
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
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40
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60
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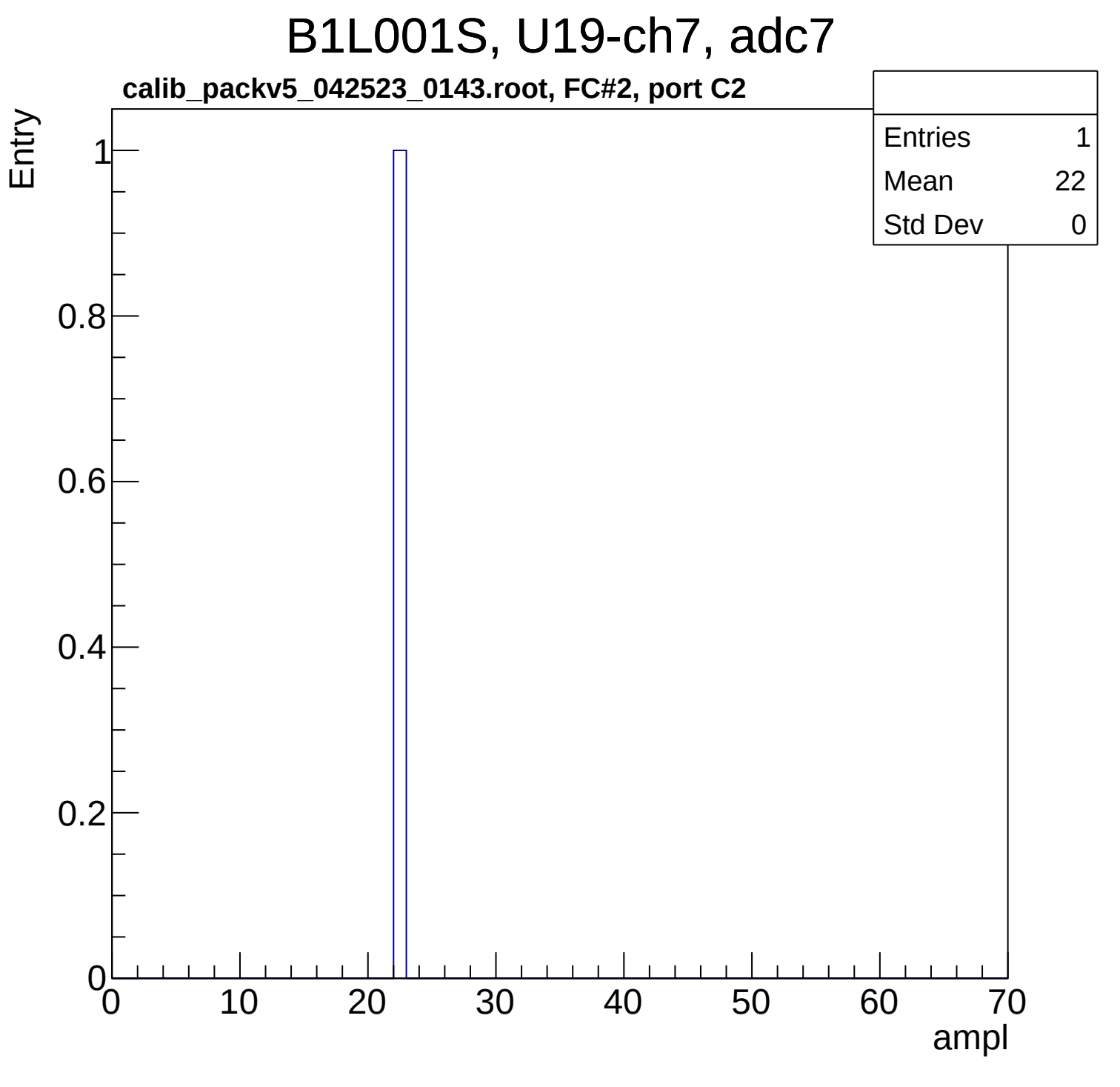
B1L001S, U19-ch7, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 22
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
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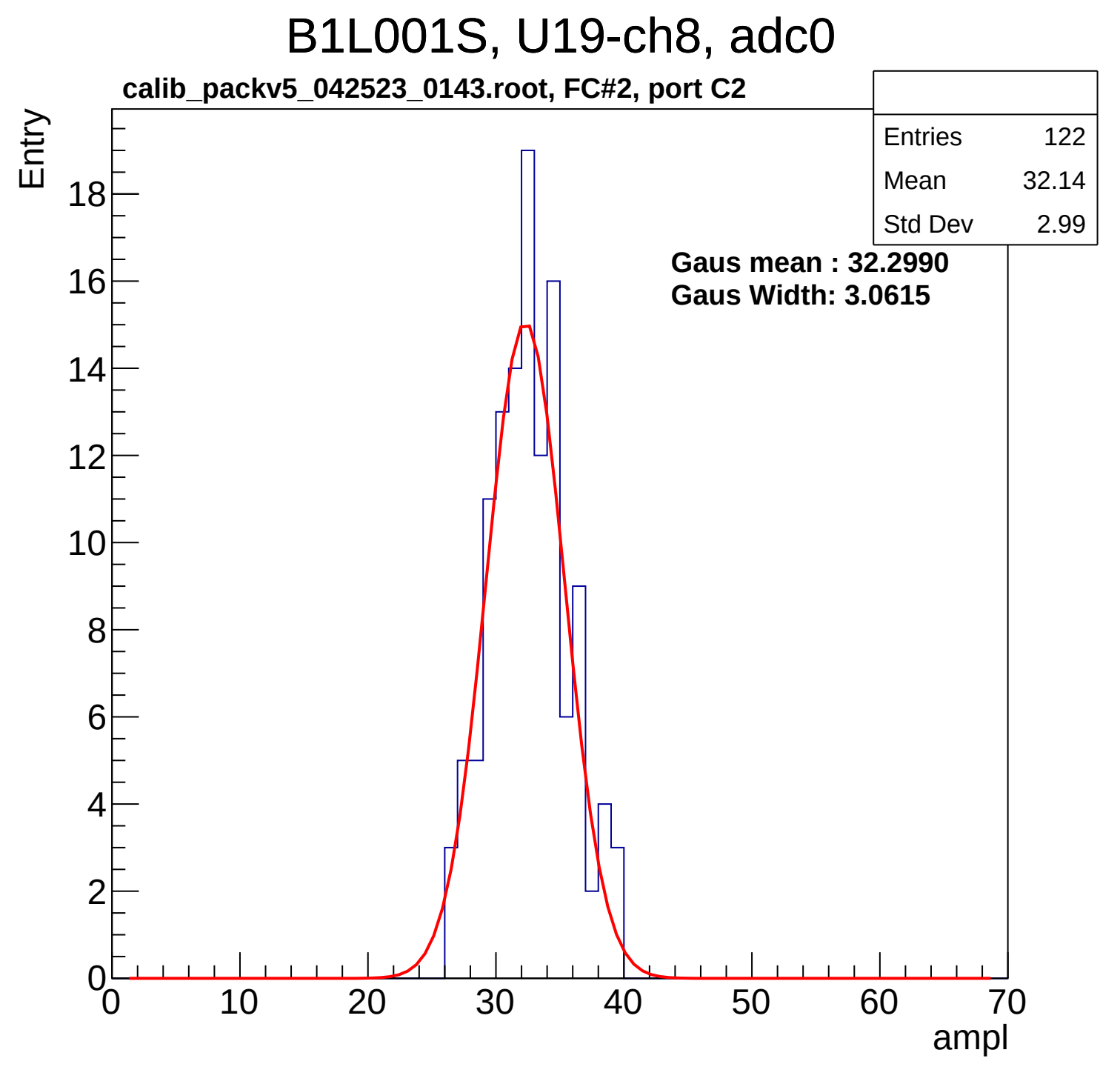
ampl


B1L001S, U19-ch8, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 122
Mean 32.14
Std Dev 2.99
Gaus mean : 32.2990
Gaus Width: 3.0615
Entry
ampl
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6
8
10
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0
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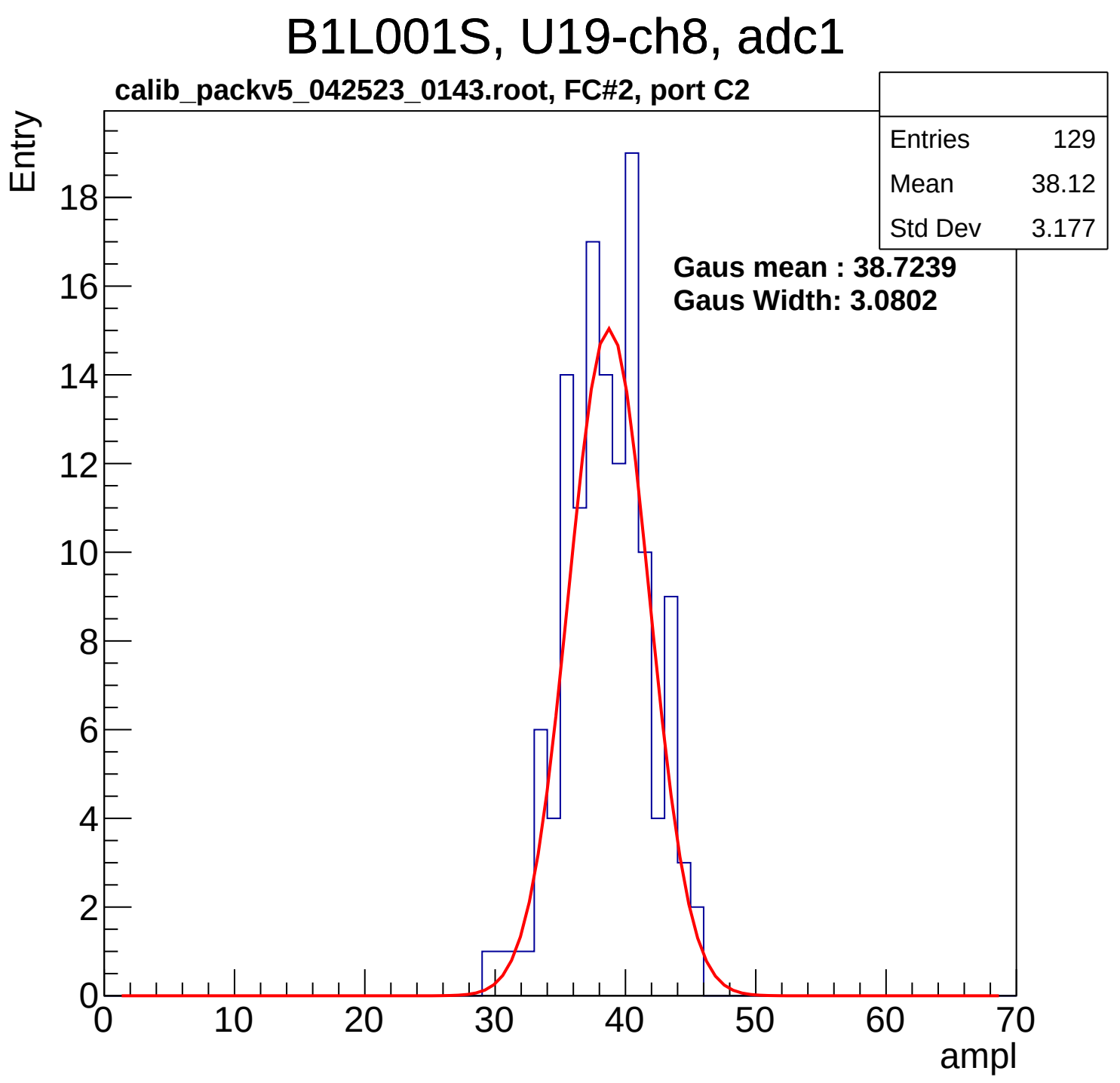
B1L001S, U19-ch8, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 129
Mean 38.12
Std Dev 3.177
Gaus mean : 38.7239
Gaus Width: 3.0802
Entry
ampl
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6
8
10
12
14
16
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0
10
20
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40
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60
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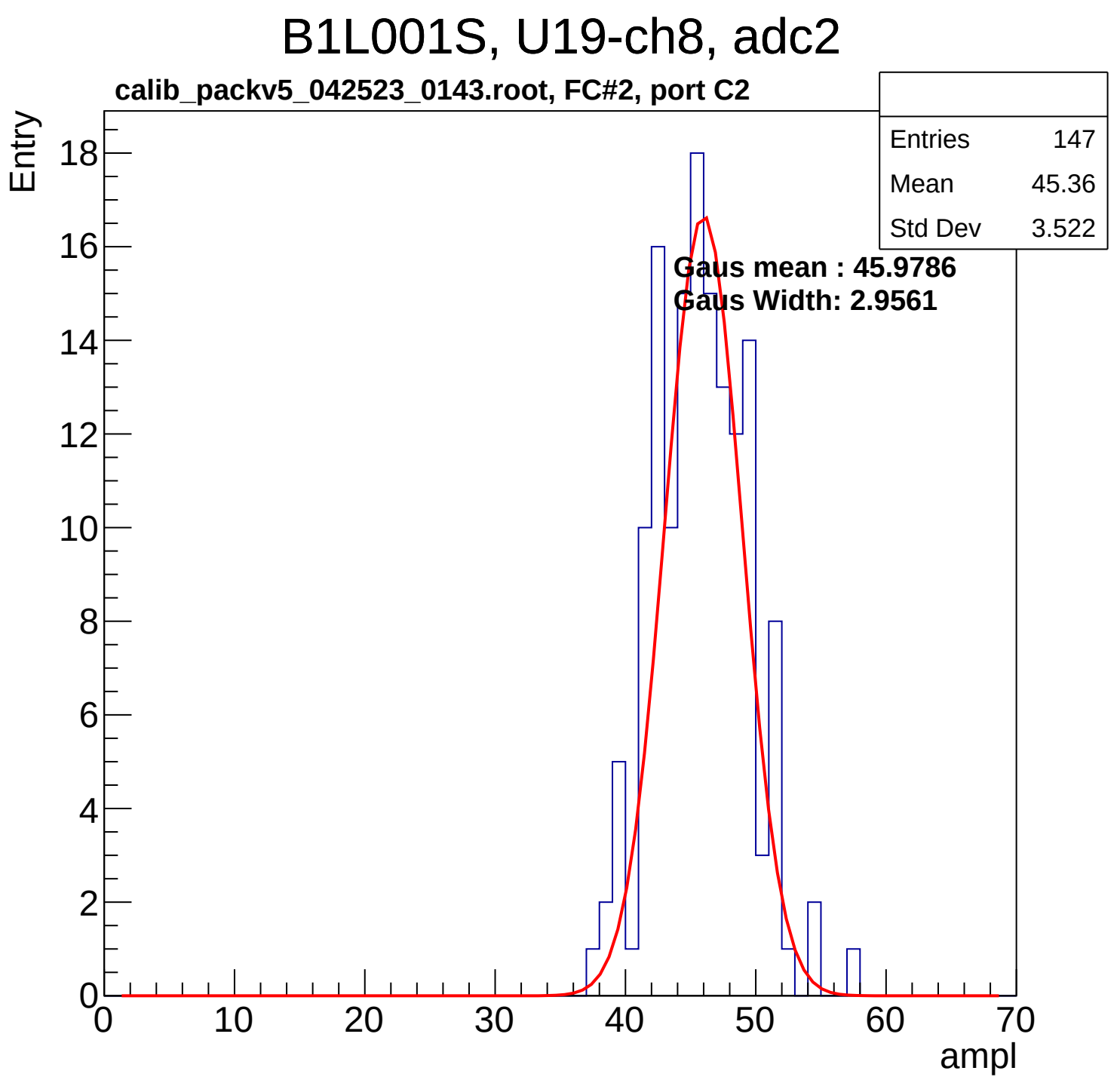
B1L001S, U19-ch8, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 147
Mean 45.36
Std Dev 3.522
Gaus mean : 45.9786
Gaus Width: 2.9561
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
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60
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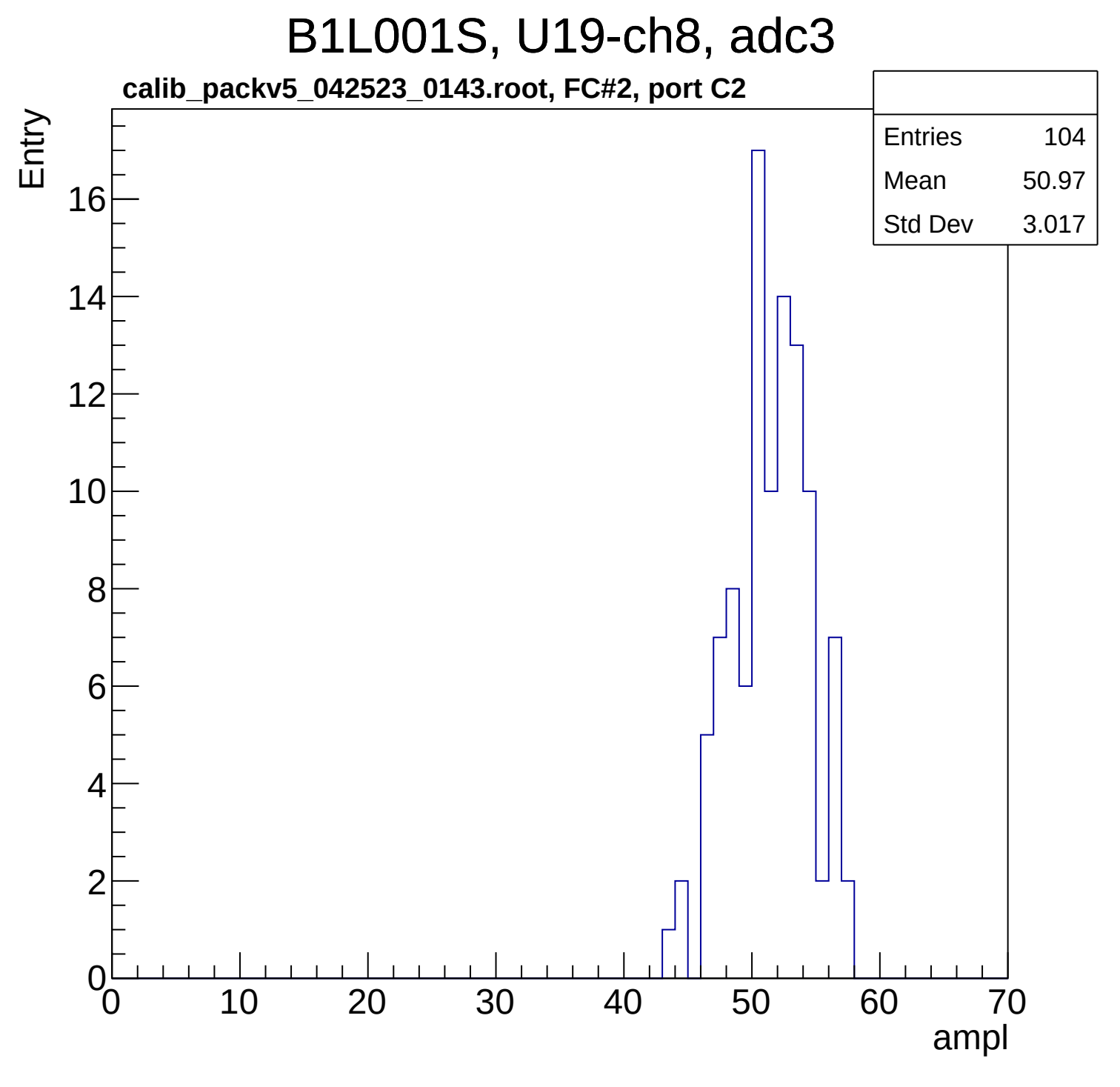
B1L001S, U19-ch8, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 104
Mean 50.97
Std Dev 3.017
Entry
ampl
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2
4
6
8
10
12
14
16
0
10
20
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40
50
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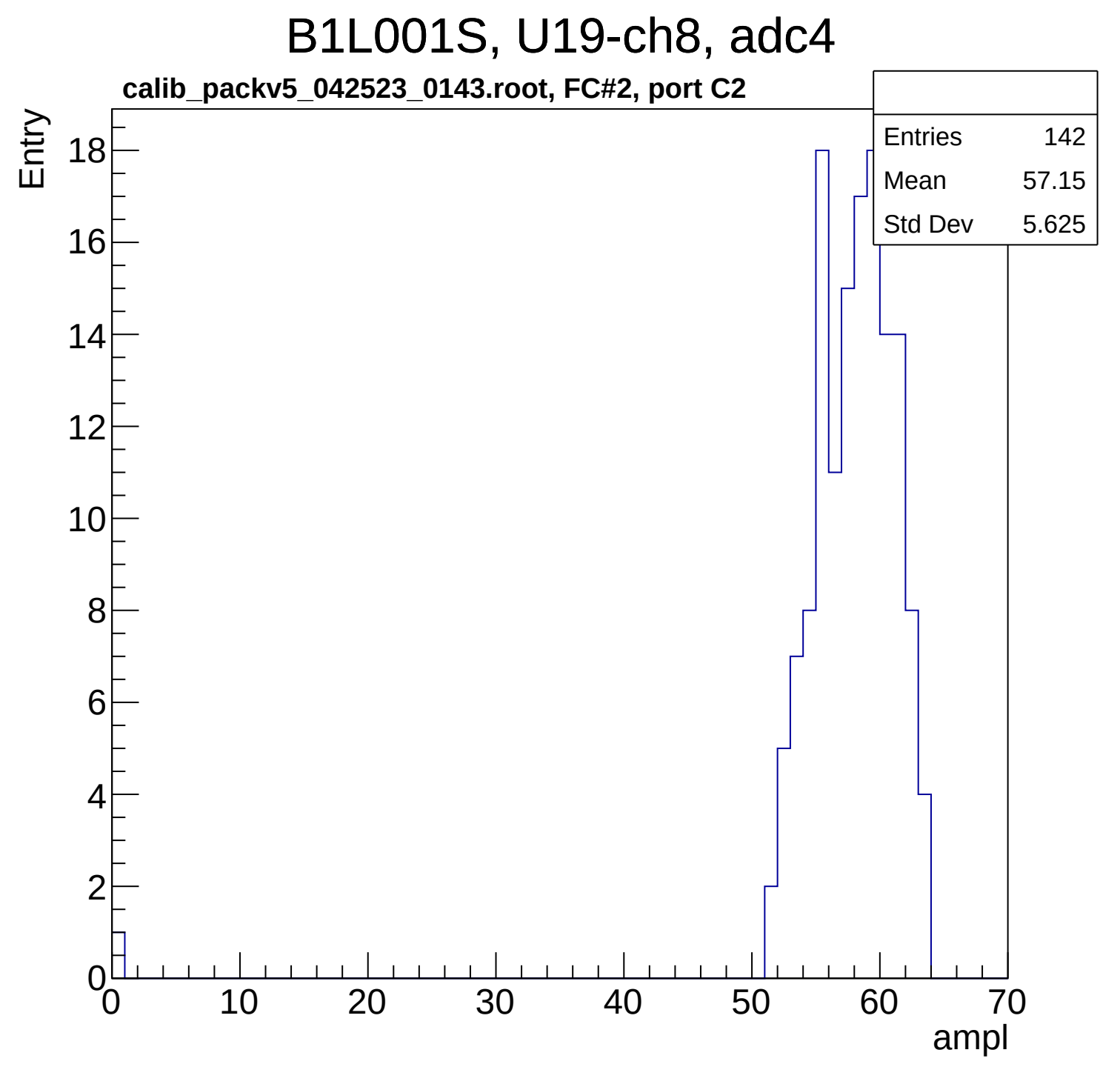
B1L001S, U19-ch8, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 142
Mean 57.15
Std Dev 5.625
Entry
ampl
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4
6
8
10
12
14
16
18
0
10
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40
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60
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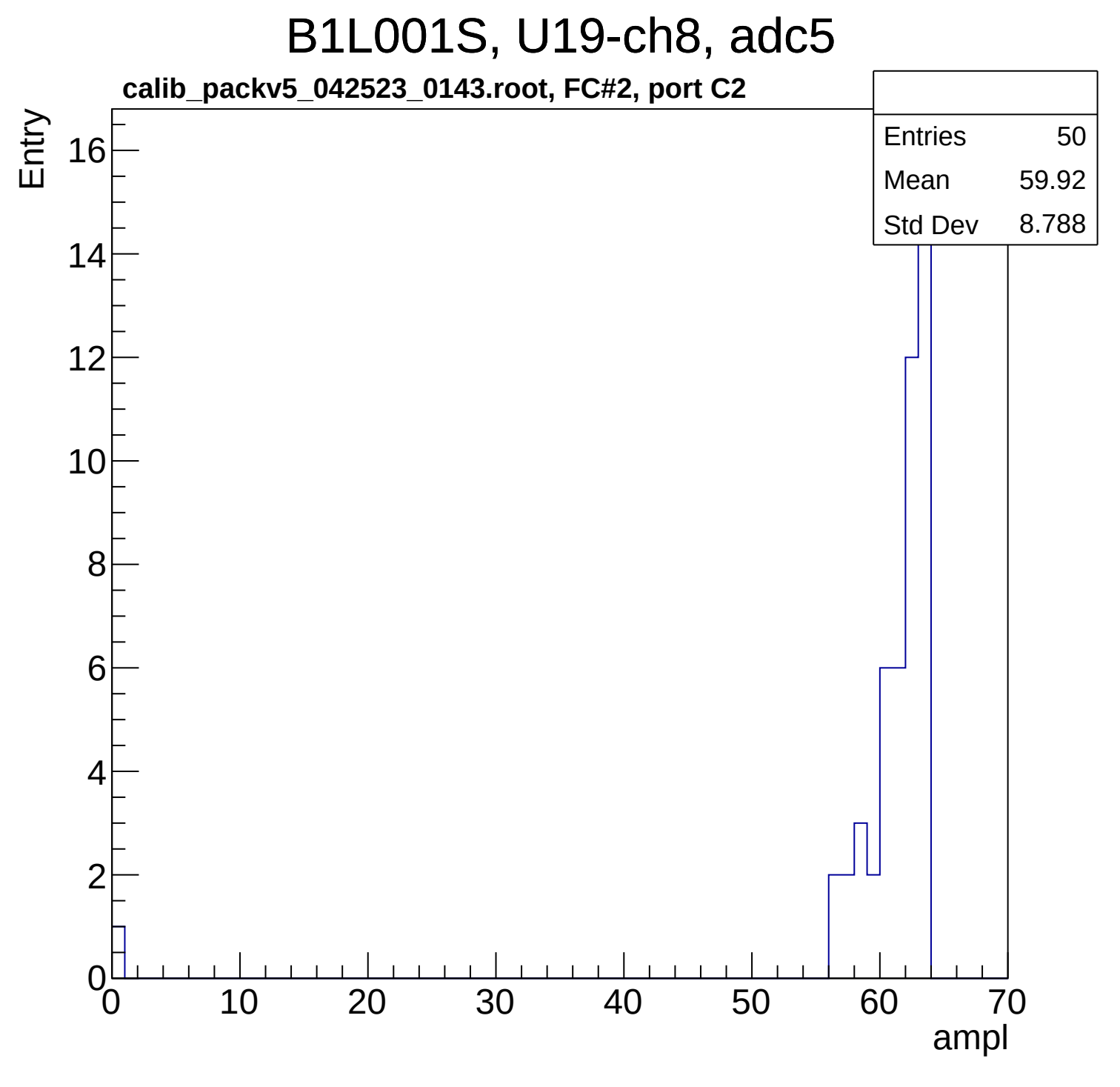
B1L001S, U19-ch8, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 50
Mean 59.92
Std Dev 8.788
Entry
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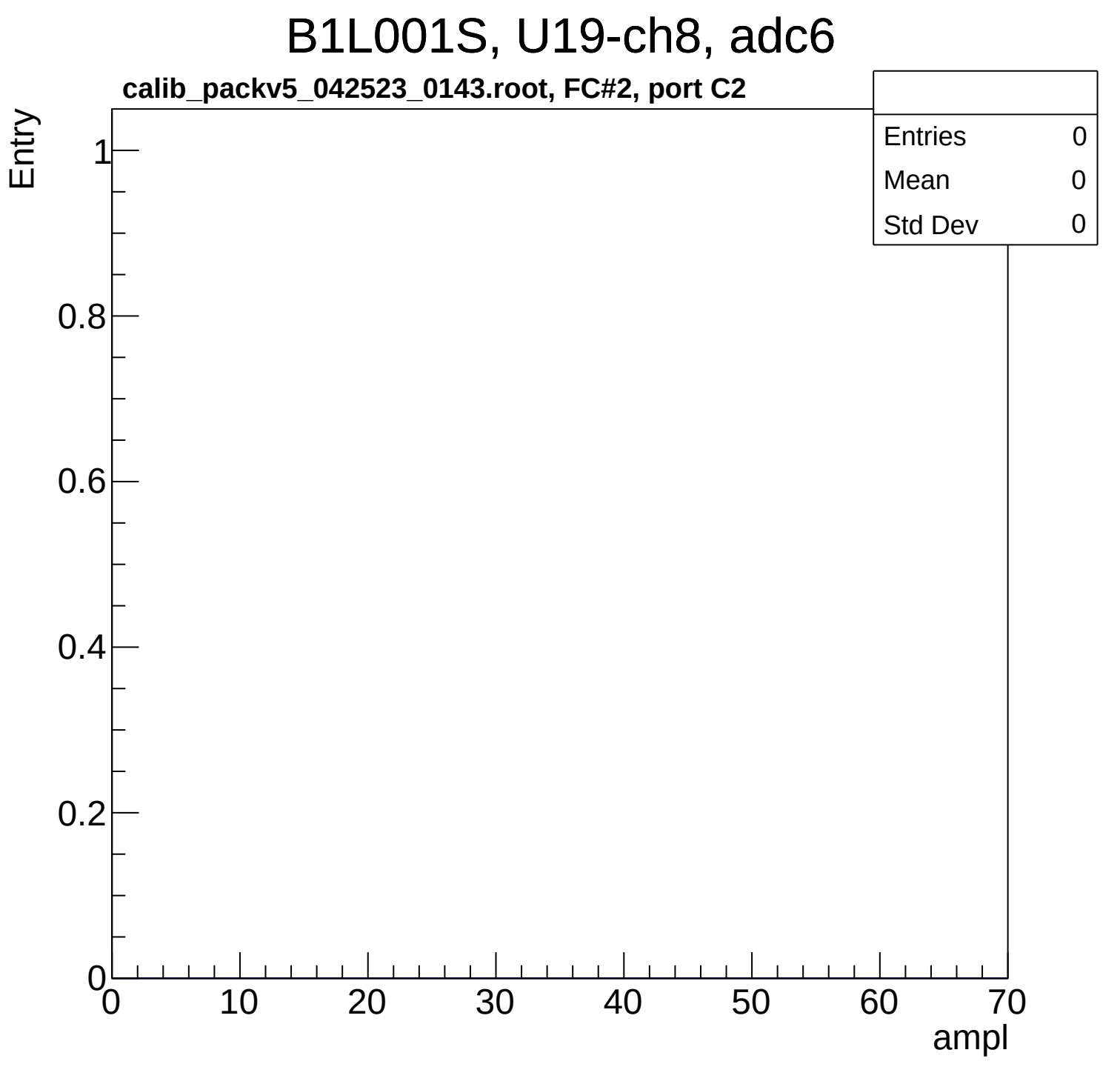
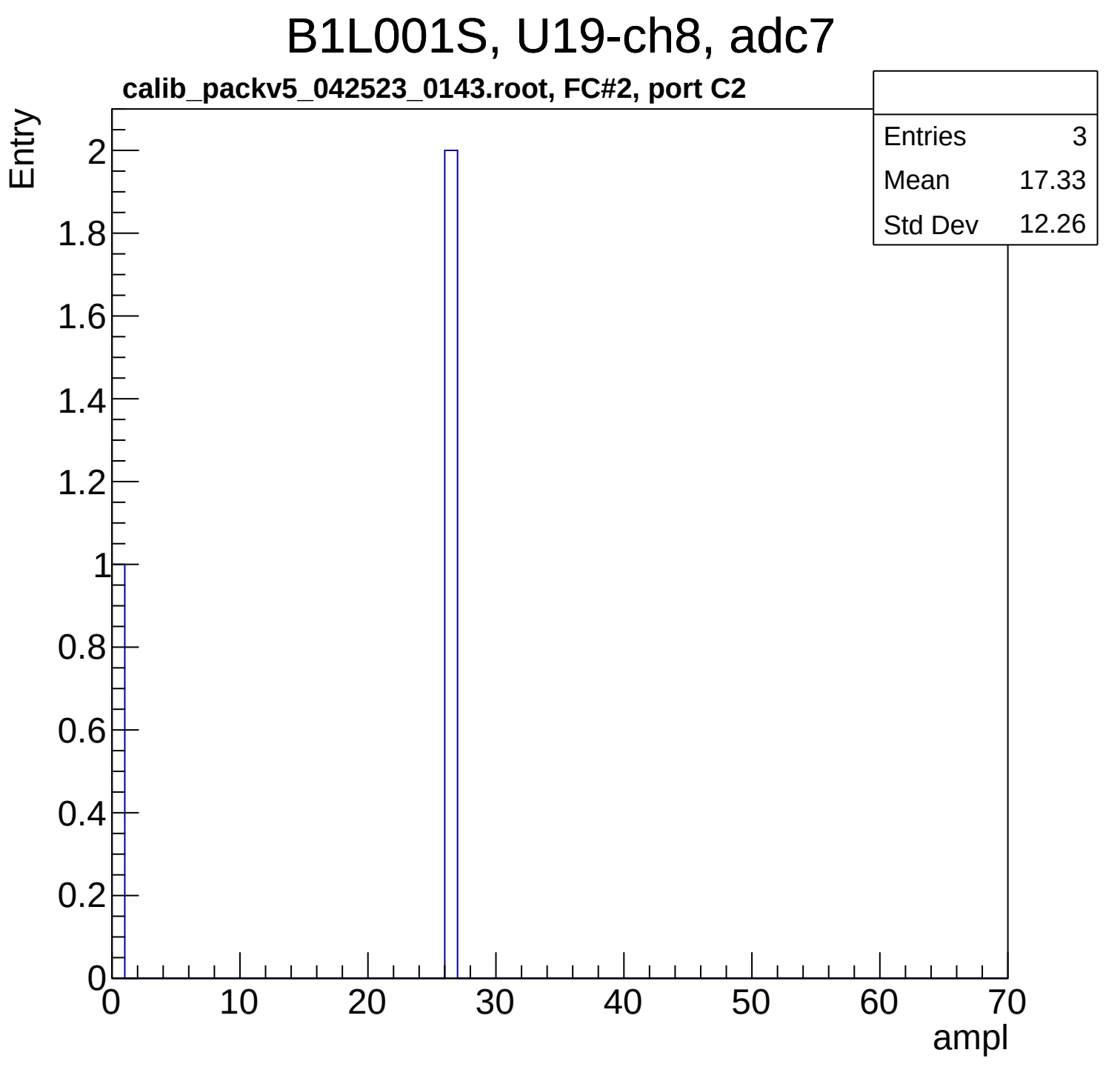
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch8, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch8, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 3
Mean 17.33
Std Dev 12.26
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
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40
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60
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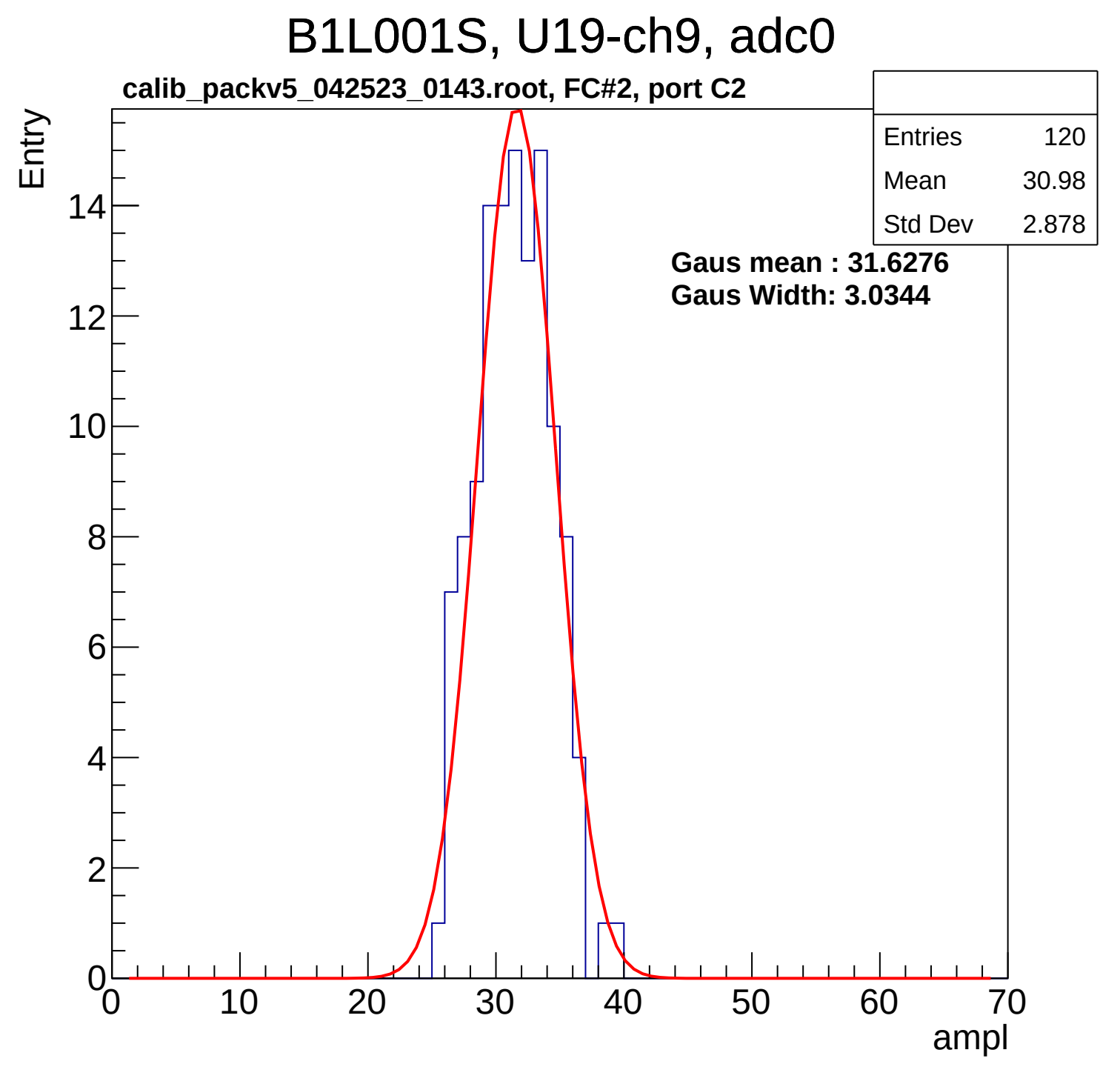
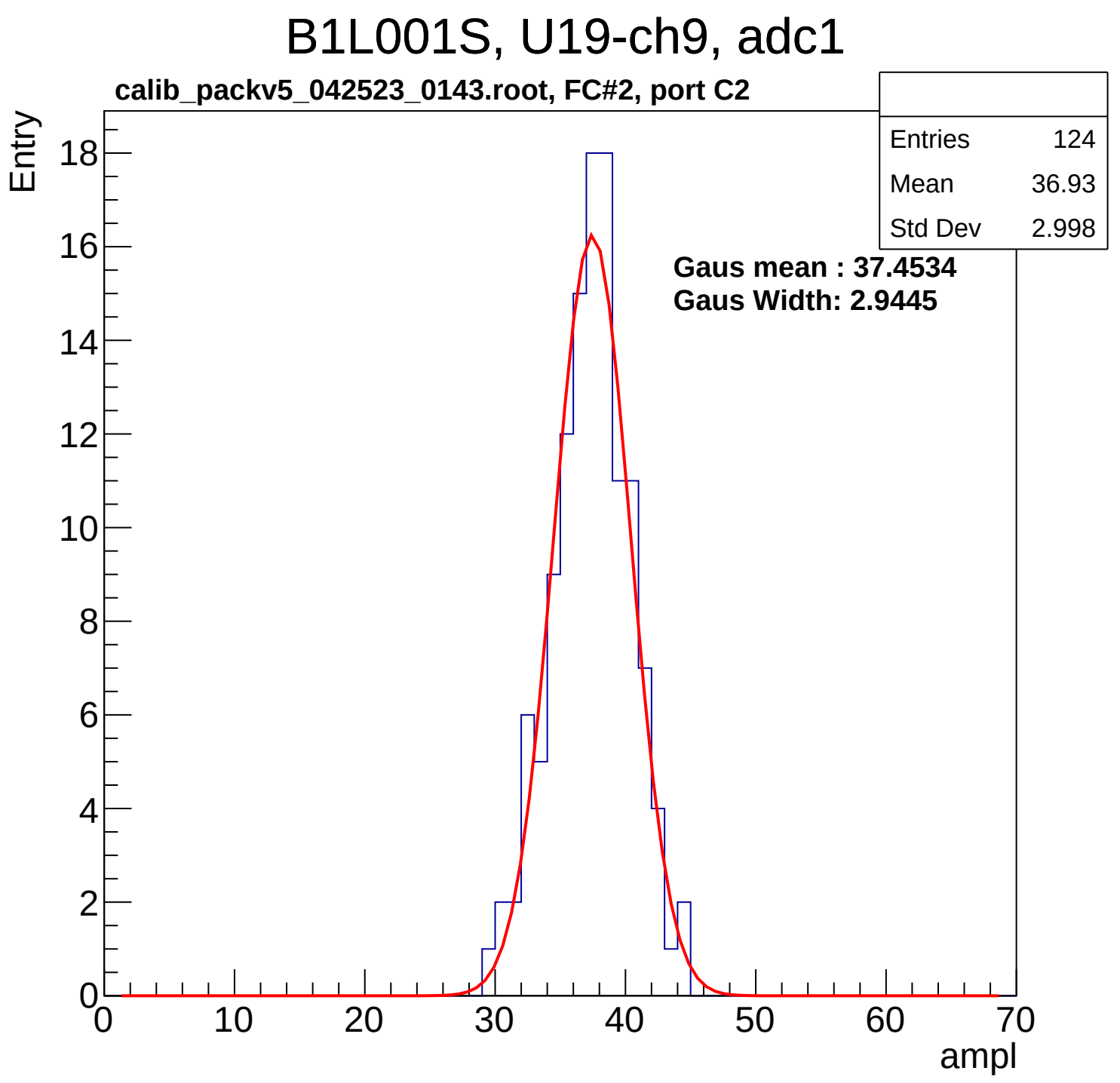

B1L001S, U19-ch9, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 120
Mean 30.98
Std Dev 2.878
Gaus mean : 31.6276
Gaus Width: 3.0344
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L001S, U19-ch9, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 124
Mean 36.93
Std Dev 2.998
Gaus mean : 37.4534
Gaus Width: 2.9445
Entry
ampl
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4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
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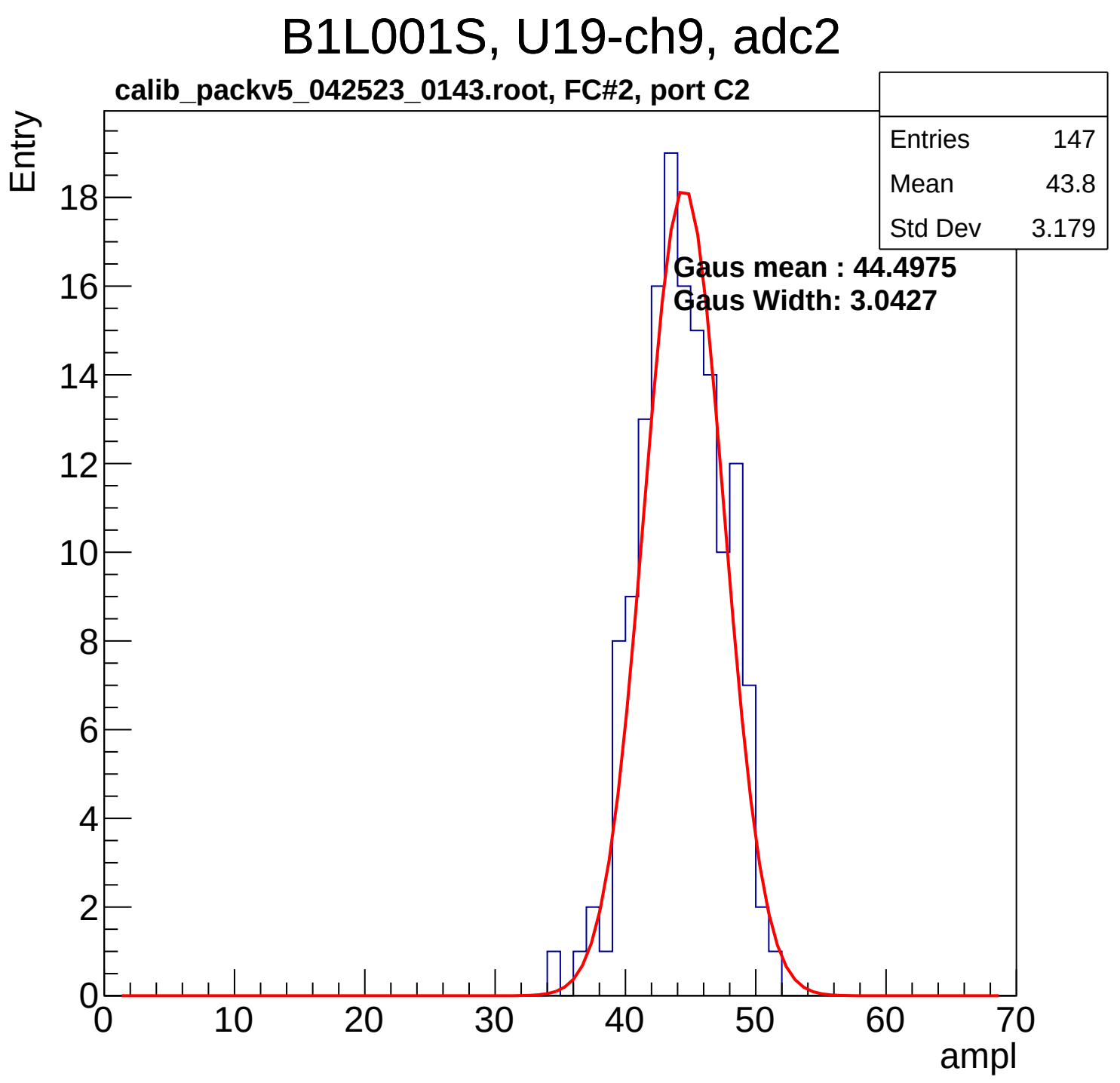
B1L001S, U19-ch9, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 147
Mean 43.8
Std Dev 3.179
Gaus mean : 44.4975
Gaus Width: 3.0427
Entry
ampl
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4
6
8
10
12
14
16
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0
10
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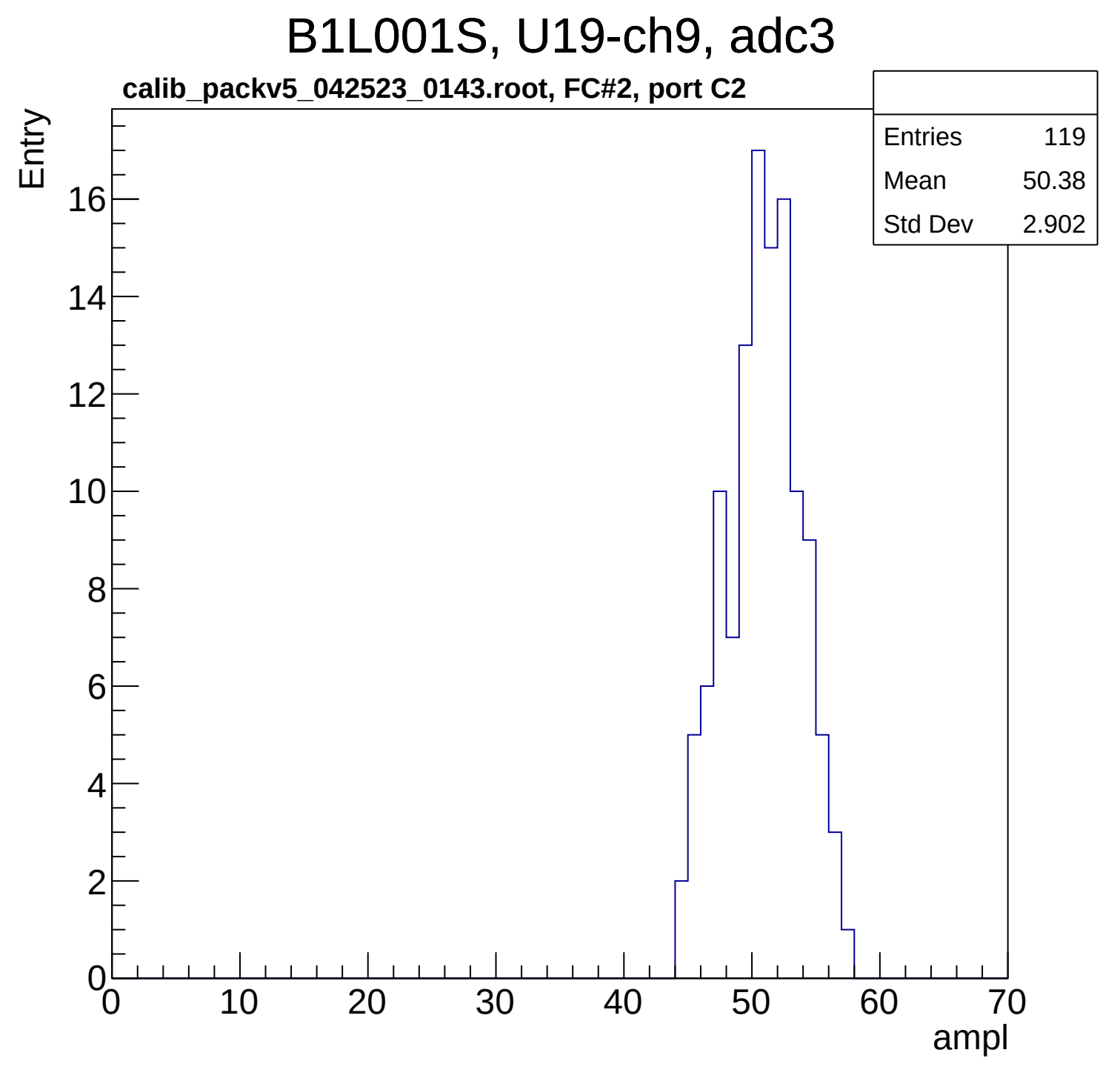
60
70


B1L001S, U19-ch9, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 119
Mean 50.38
Std Dev 2.902
Entry
ampl
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2
4
6
8
10
12
14
16
0
10
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40
50
60
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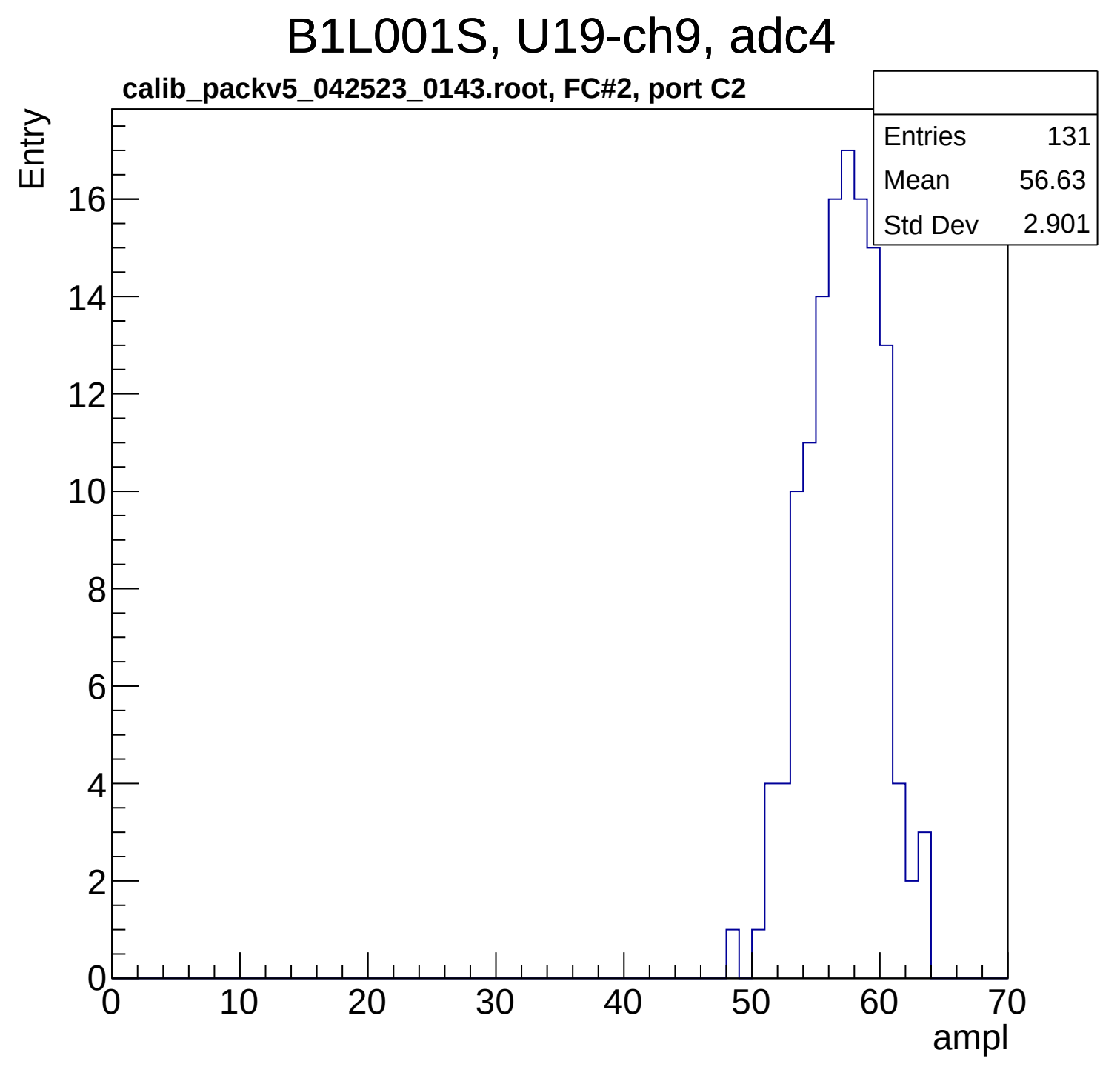
B1L001S, U19-ch9, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 131
Mean 56.63
Std Dev 2.901
Entry
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4
6
8
10
12
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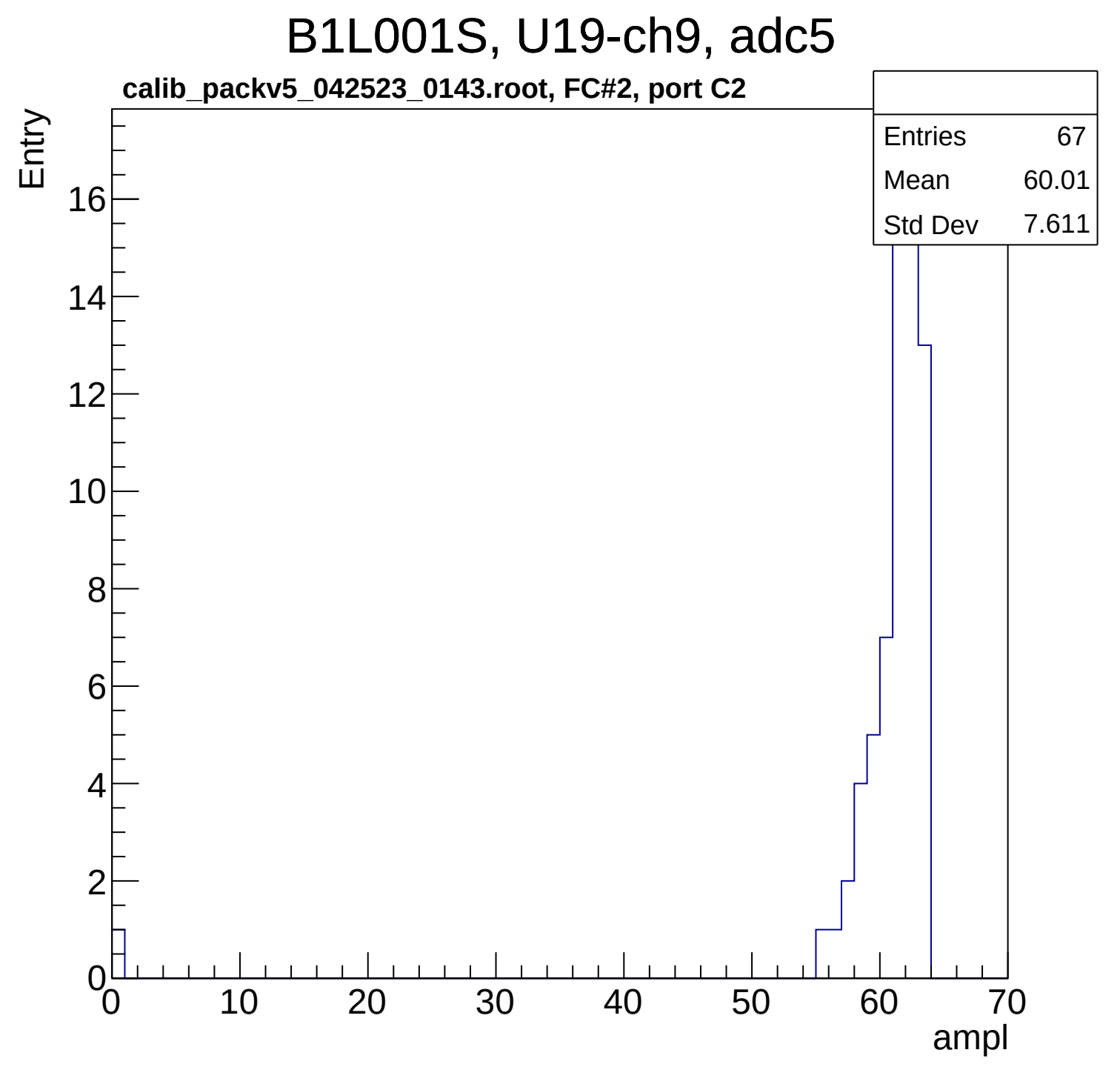
16
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch9, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 67
Mean 60.01
Std Dev 7.611
Entry
ampl
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4
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8
10
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0
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60
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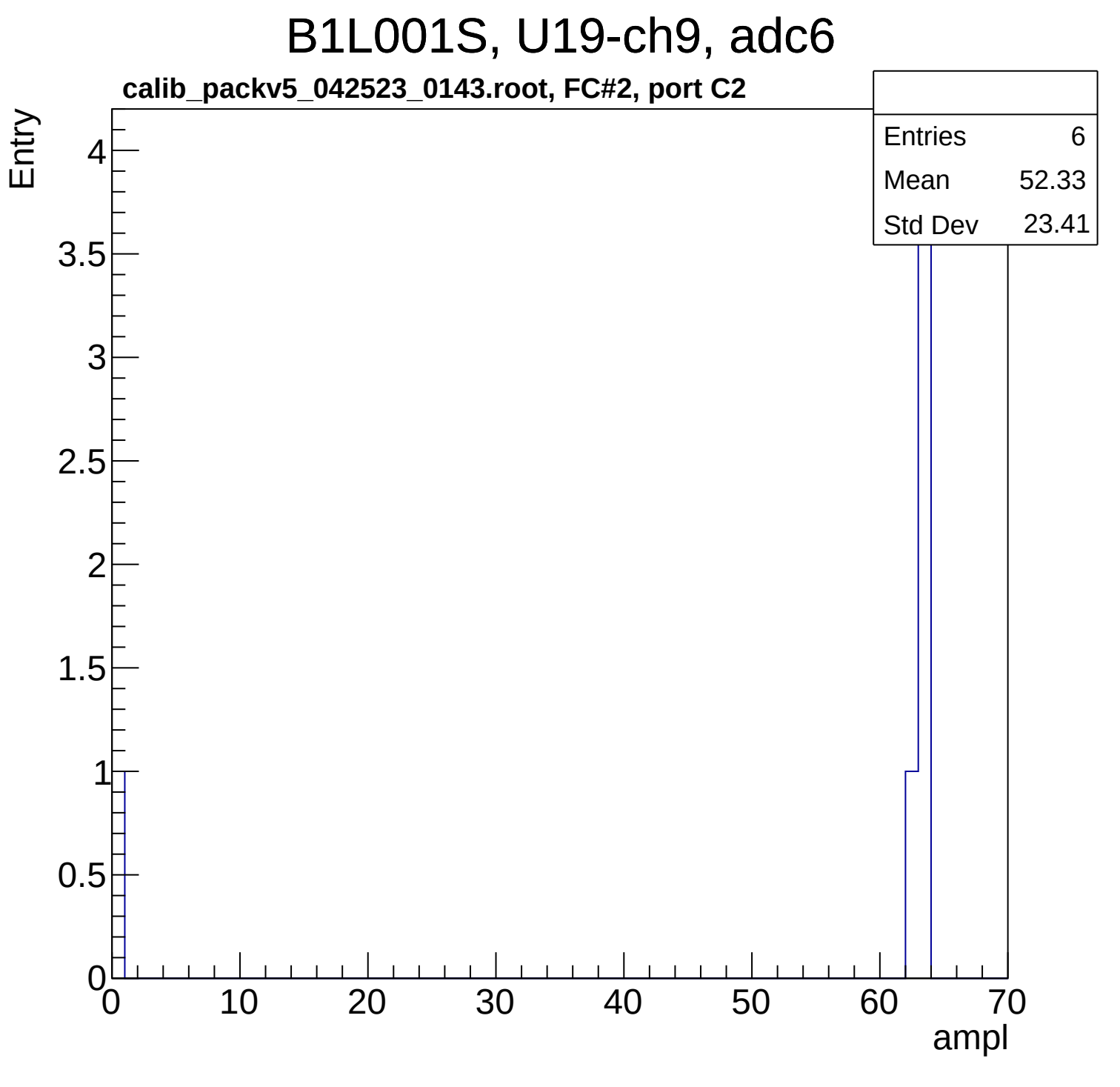
B1L001S, U19-ch9, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 6
Mean 52.33
Std Dev 23.41
Entry
ampl
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0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
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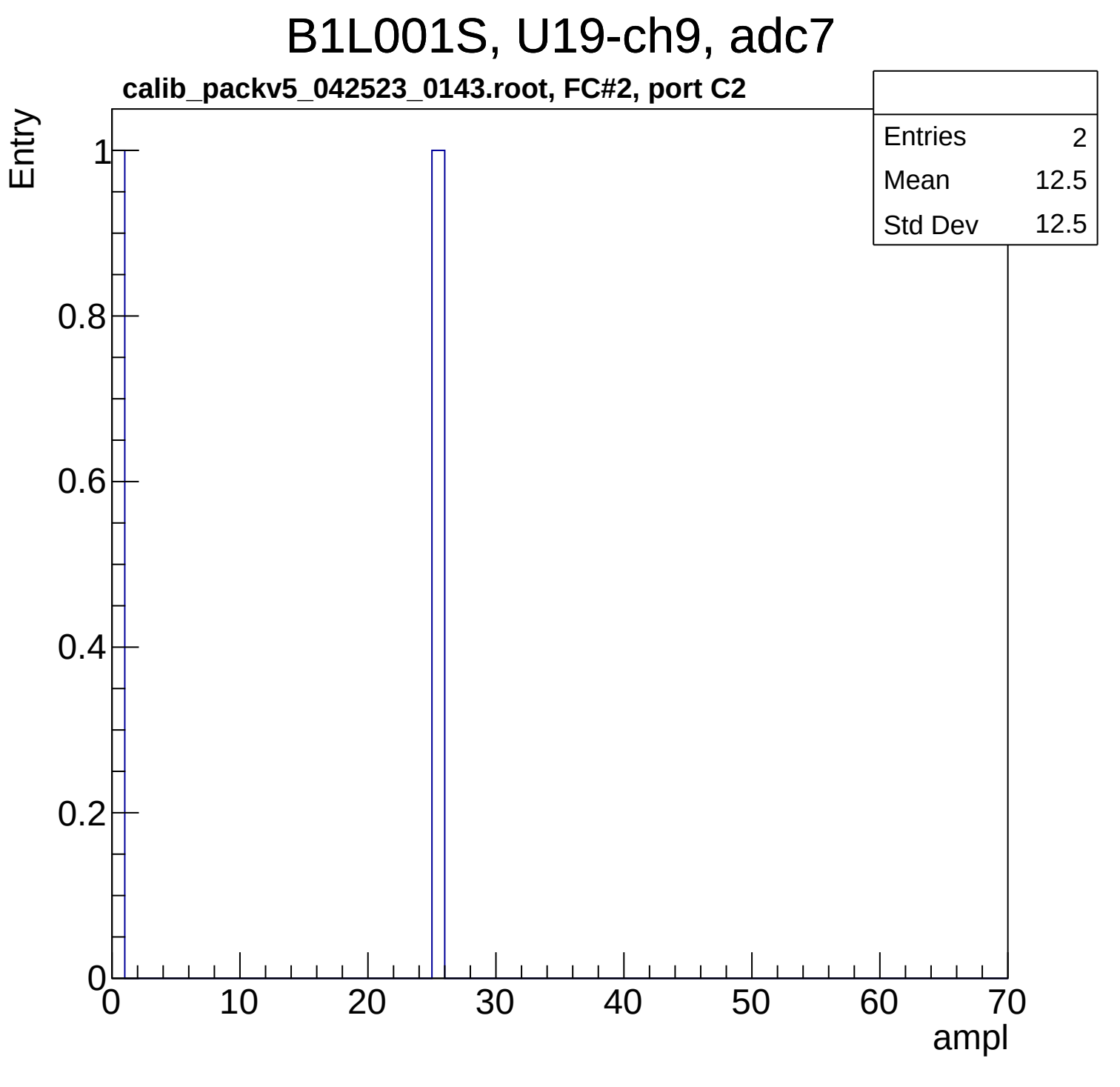
40
50
60
70


B1L001S, U19-ch9, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 12.5
Std Dev 12.5
Entry
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0.6
0.4
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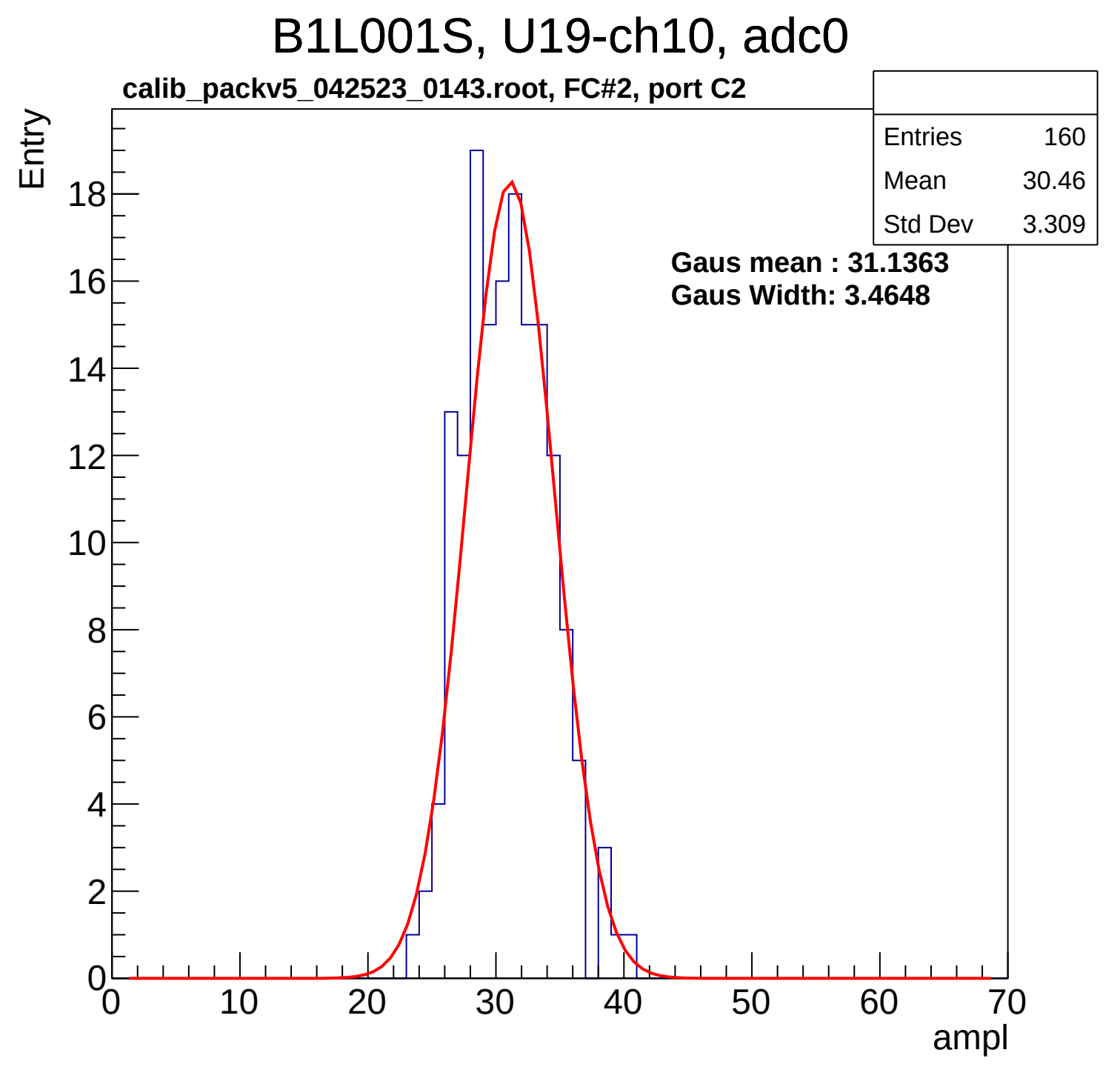
50
60
70
ampl


B1L001S, U19-ch10, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 160
Mean 30.46
Std Dev 3.309
Gaus mean : 31.1363
Gaus Width: 3.4648
Entry
ampl
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4
6
8
10
12
14
16
18
0
10
20
30
40
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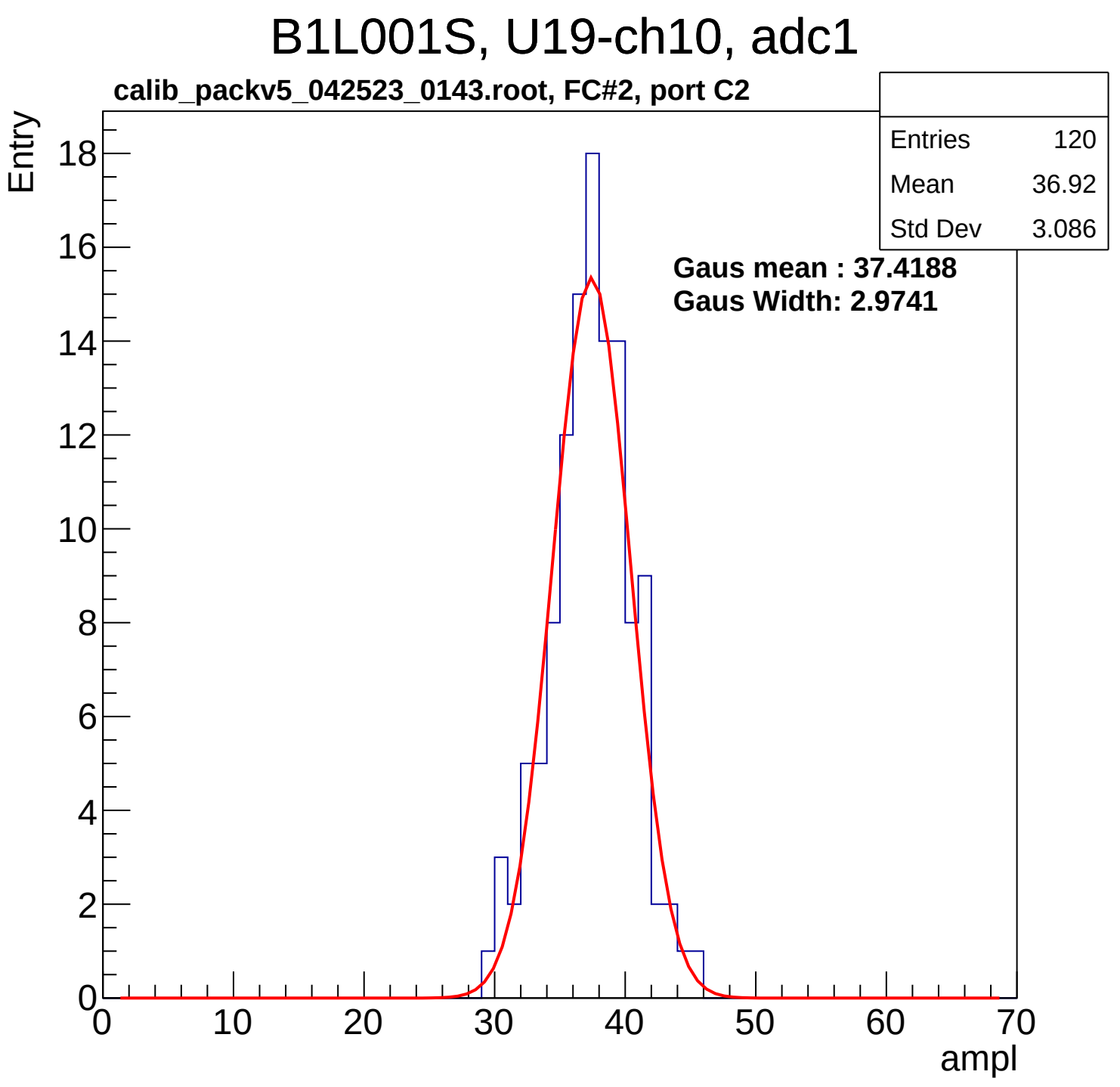
60
70


B1L001S, U19-ch10, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 120
Mean 36.92
Std Dev 3.086
Gaus mean : 37.4188
Gaus Width: 2.9741
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
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60
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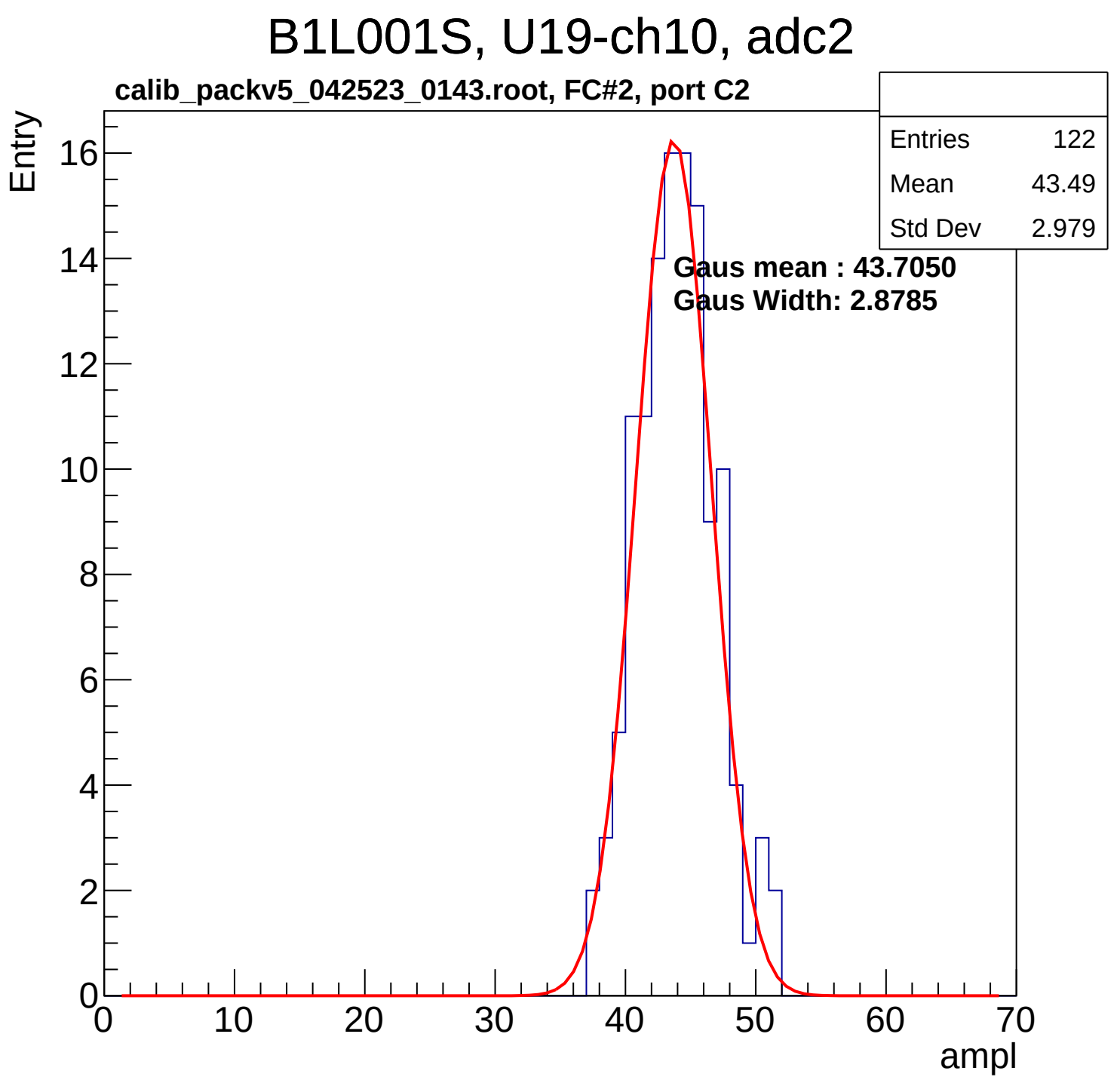
B1L001S, U19-ch10, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 122
Mean 43.49
Std Dev 2.979
Gaus mean : 43.7050
Gaus Width: 2.8785
Entry
ampl
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2
4
6
8
10
12
14
16
0
10
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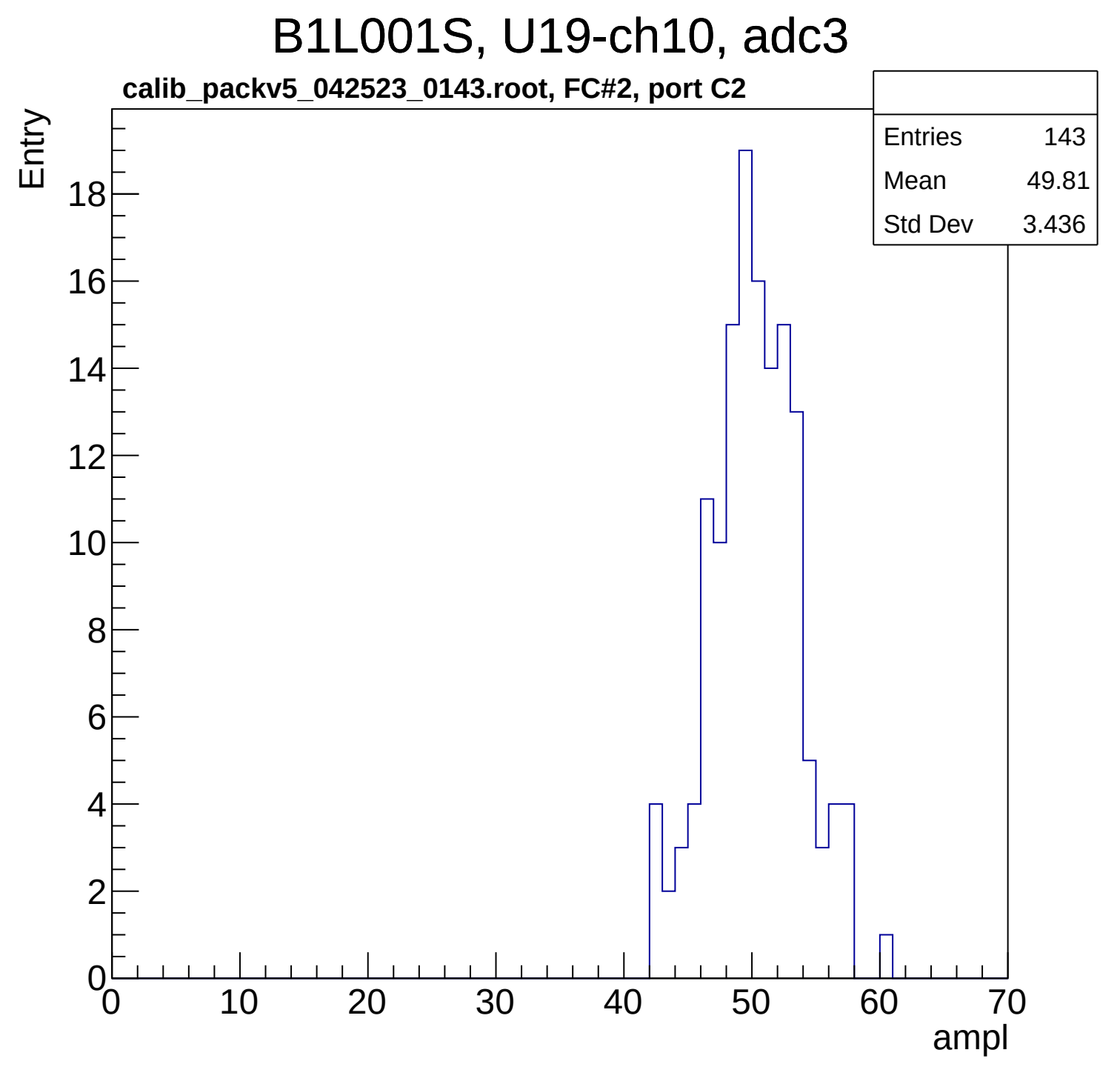
40
50
60
70


B1L001S, U19-ch10, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 143
Mean 49.81
Std Dev 3.436
Entry
ampl
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4
6
8
10
12
14
16
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0
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60
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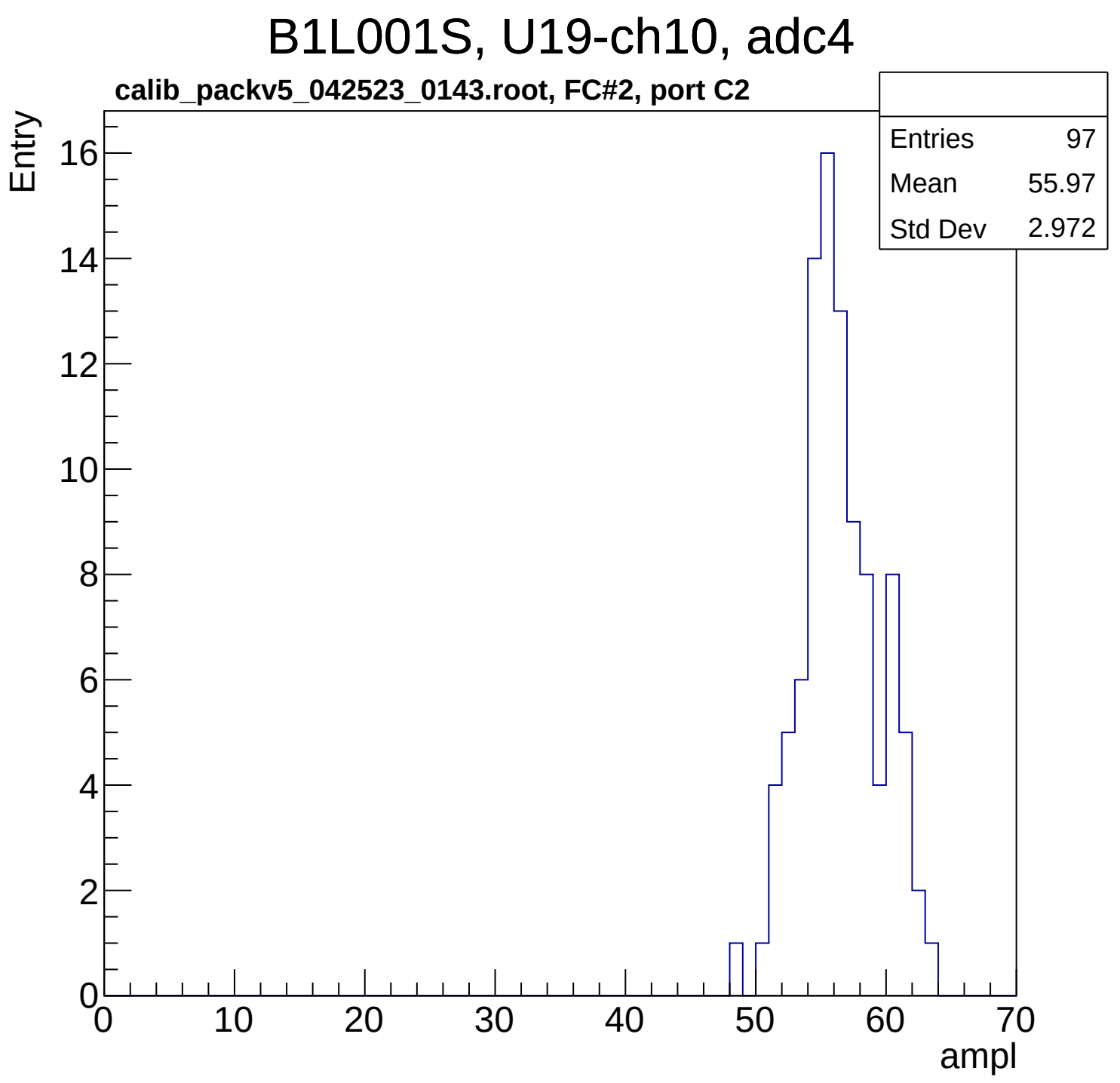
B1L001S, U19-ch10, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 97
Mean 55.97
Std Dev 2.972
Entry
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4
6
8
10
12
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16
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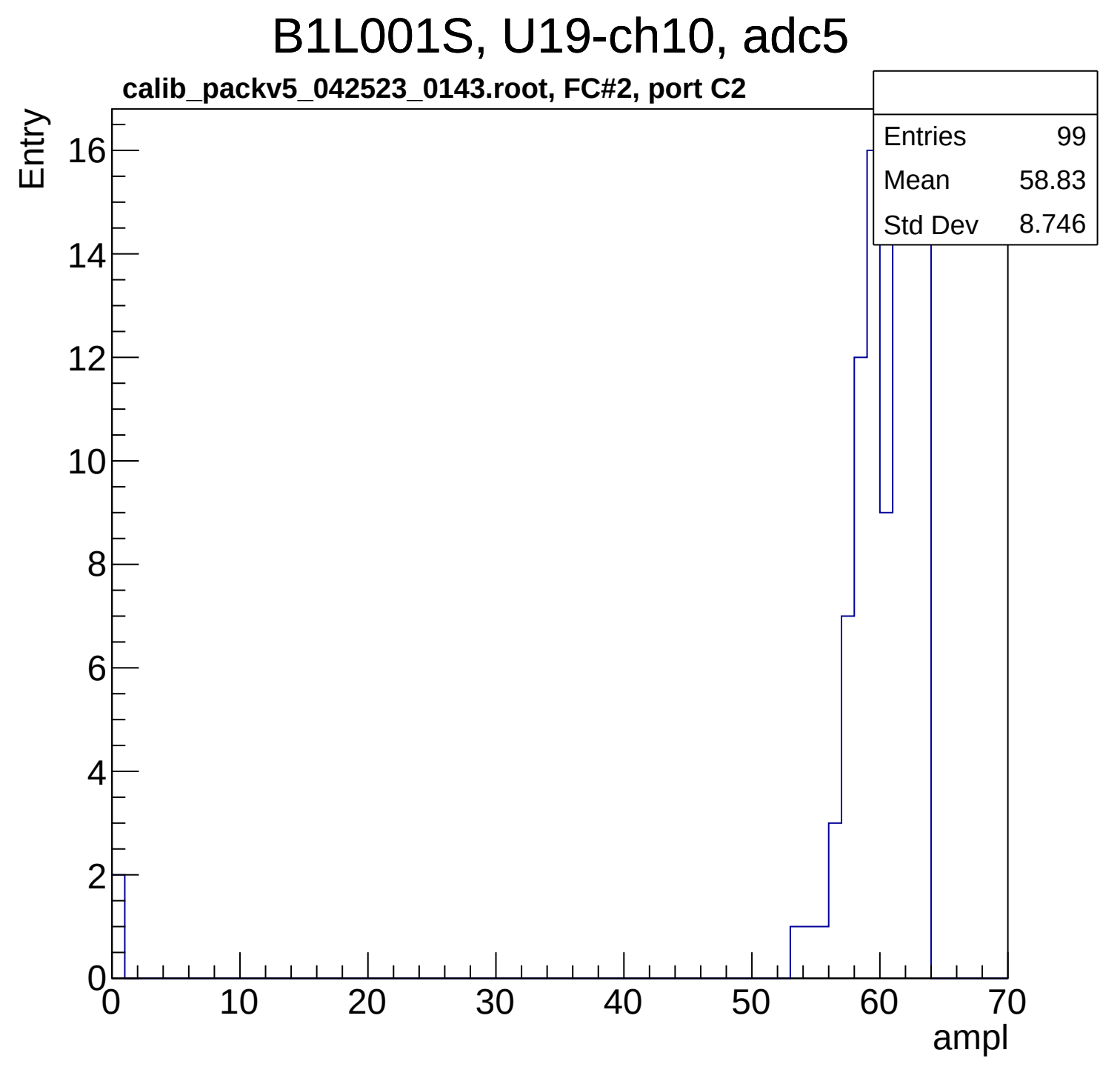
50
60
70
ampl


B1L001S, U19-ch10, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 99
Mean 58.83
Std Dev 8.746
Entry
ampl
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2
4
6
8
10
12
14
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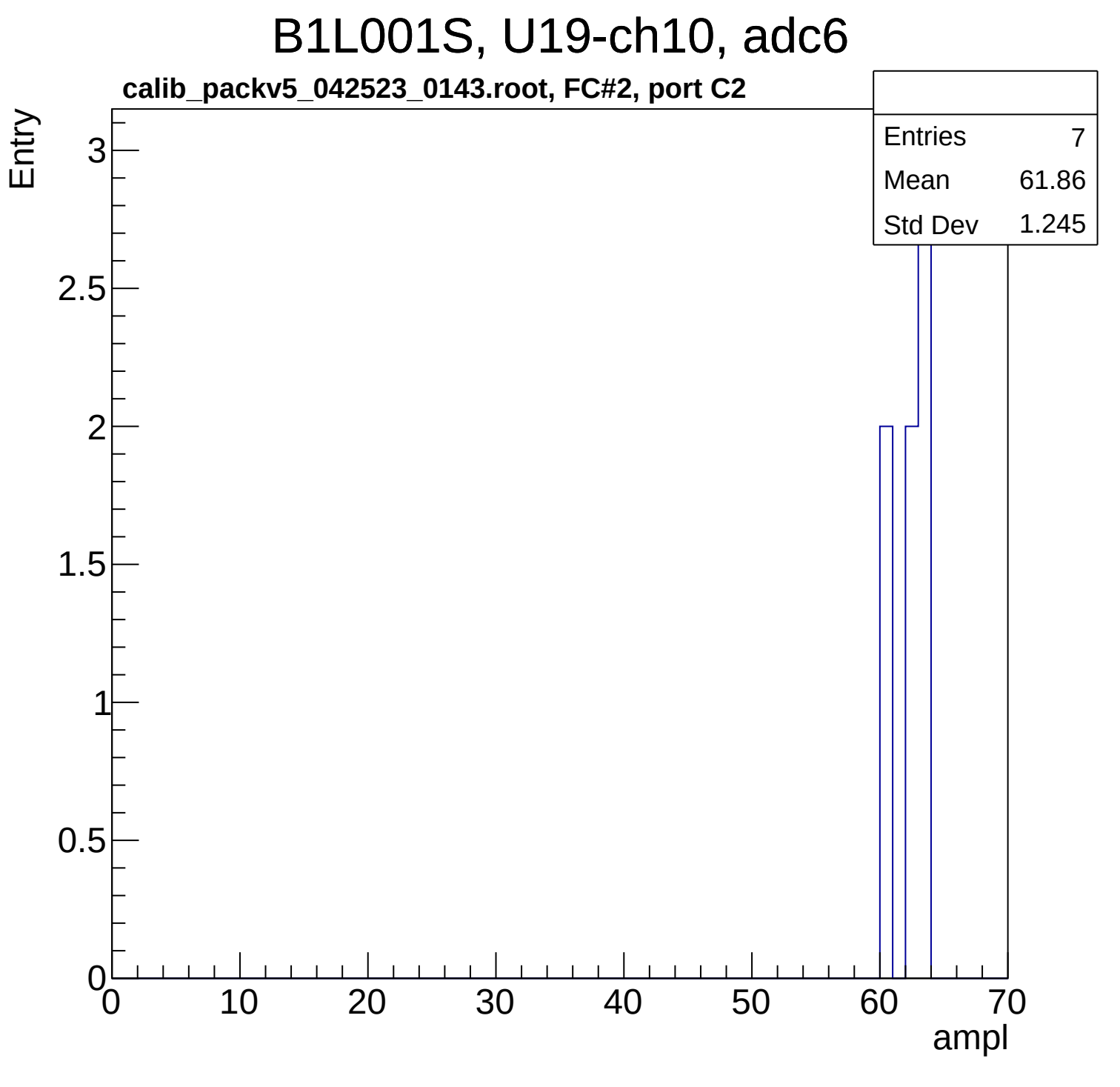
0
10
20
30
40
50
60
70


B1L001S, U19-ch10, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 7
Mean 61.86
Std Dev 1.245
Entry
ampl
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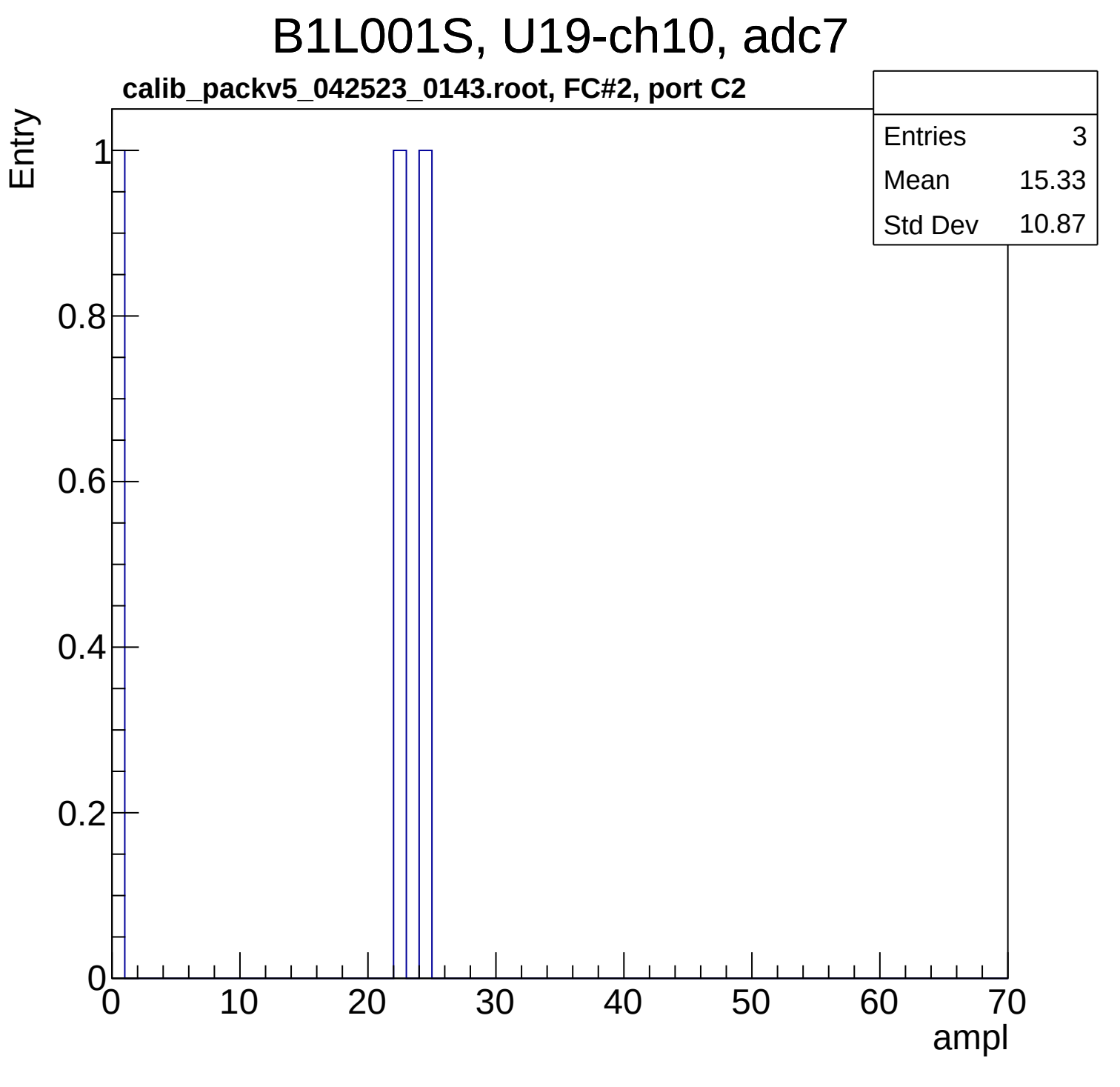
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L001S, U19-ch10, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 3
Mean 15.33
Std Dev 10.87
Entry
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0.4
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20
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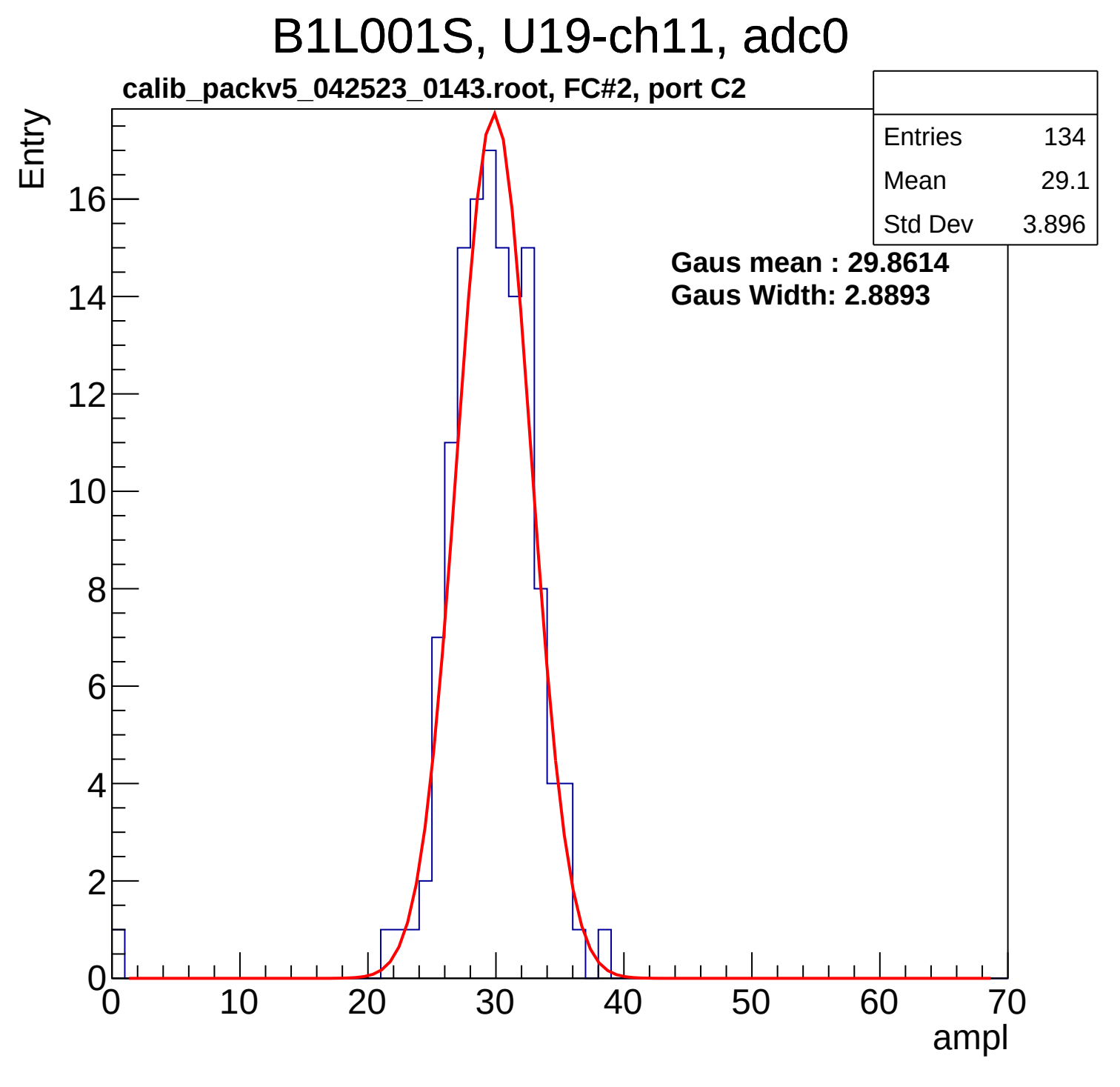
50
60
70
ampl


B1L001S, U19-ch11, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 134
Mean 29.1
Std Dev 3.896
Gaus mean : 29.8614
Gaus Width: 2.8893
Entry
ampl
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2
4
6
8
10
12
14
16
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20
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40
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60
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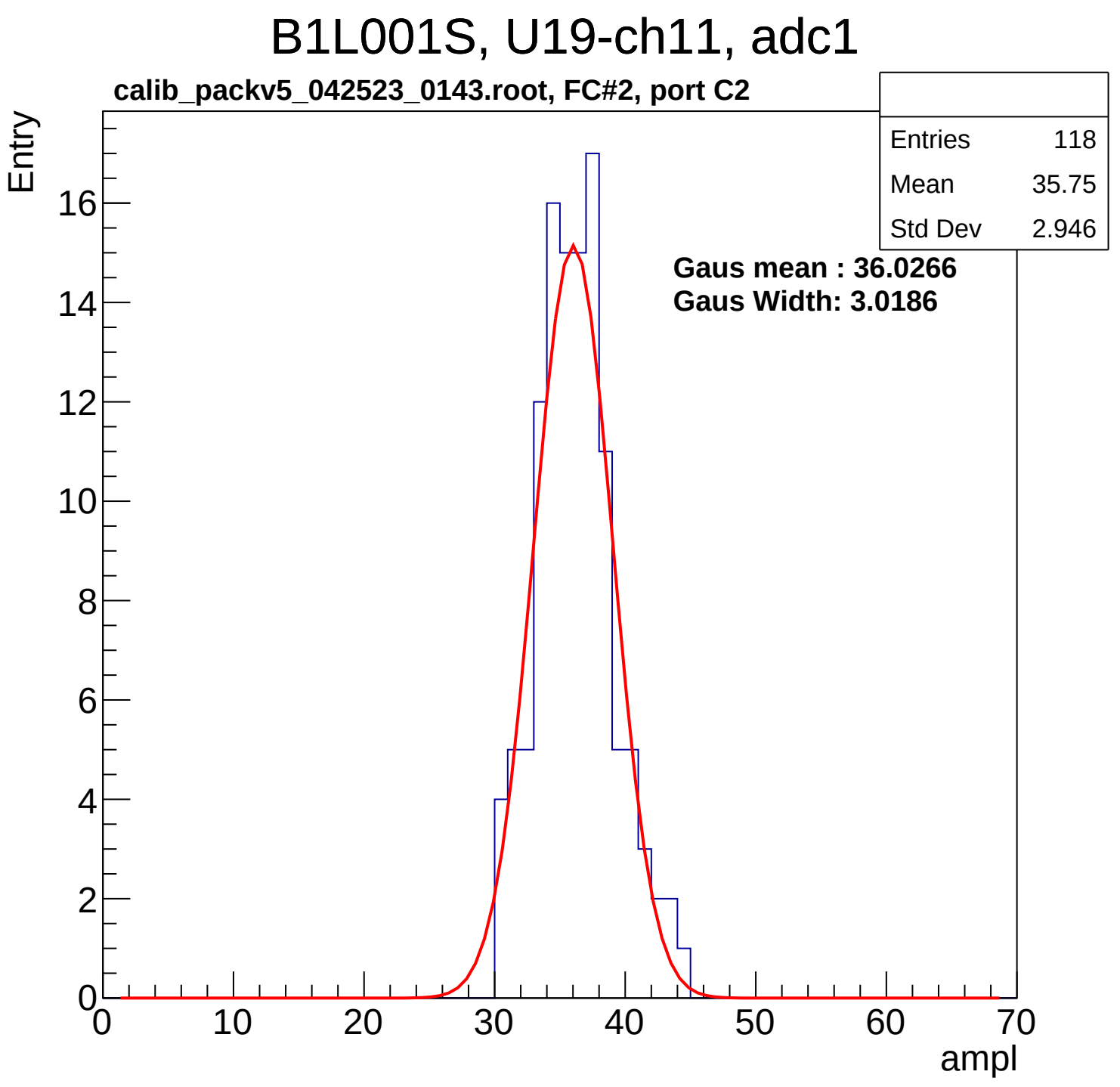
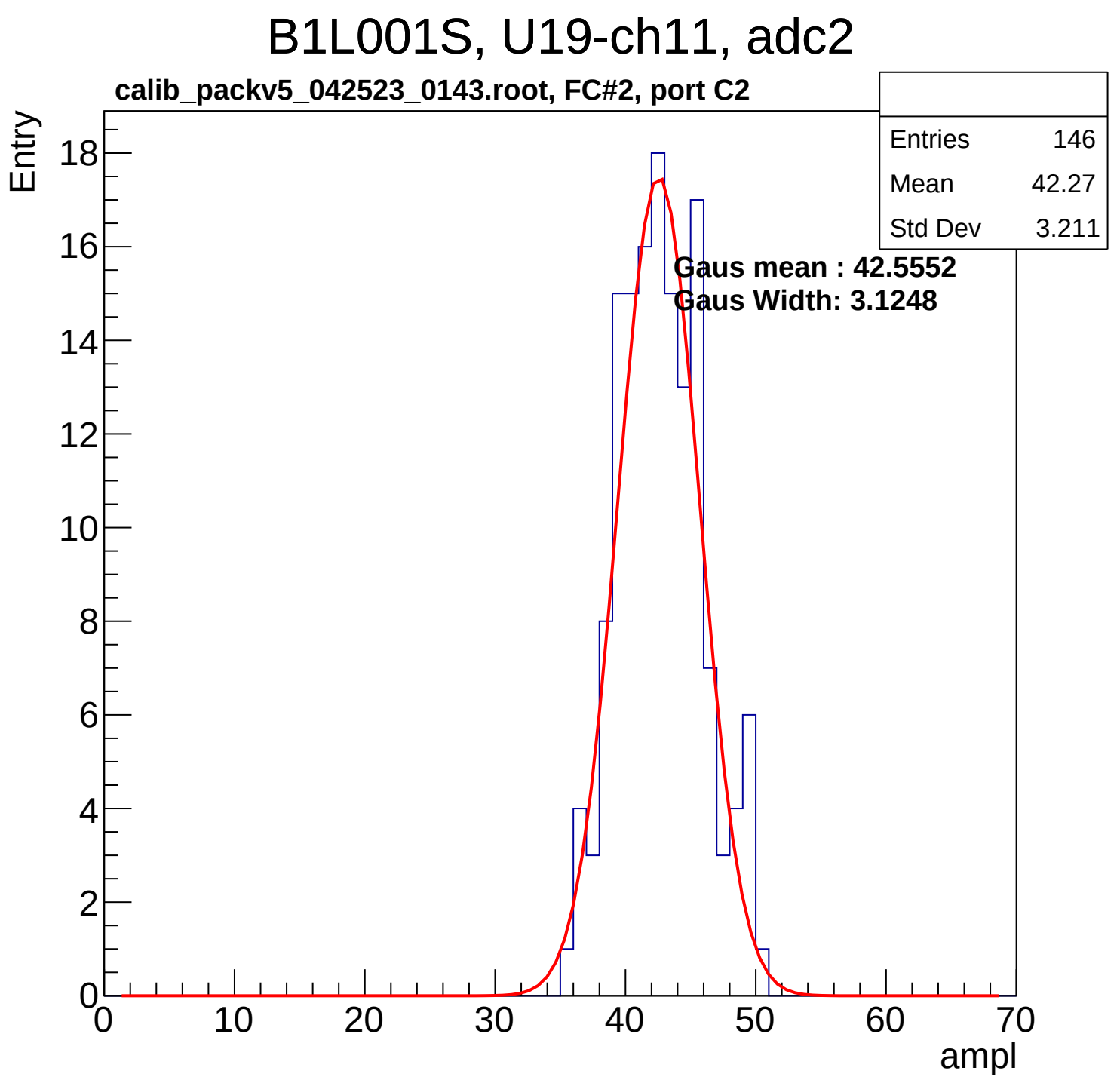

B1L001S, U19-ch11, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 118
Mean 35.75
Std Dev 2.946
Gaus mean : 36.0266
Gaus Width: 3.0186
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70


B1L001S, U19-ch11, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 146
Mean 42.27
Std Dev 3.211
Gaus mean : 42.5552
Gaus Width: 3.1248
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
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40
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60
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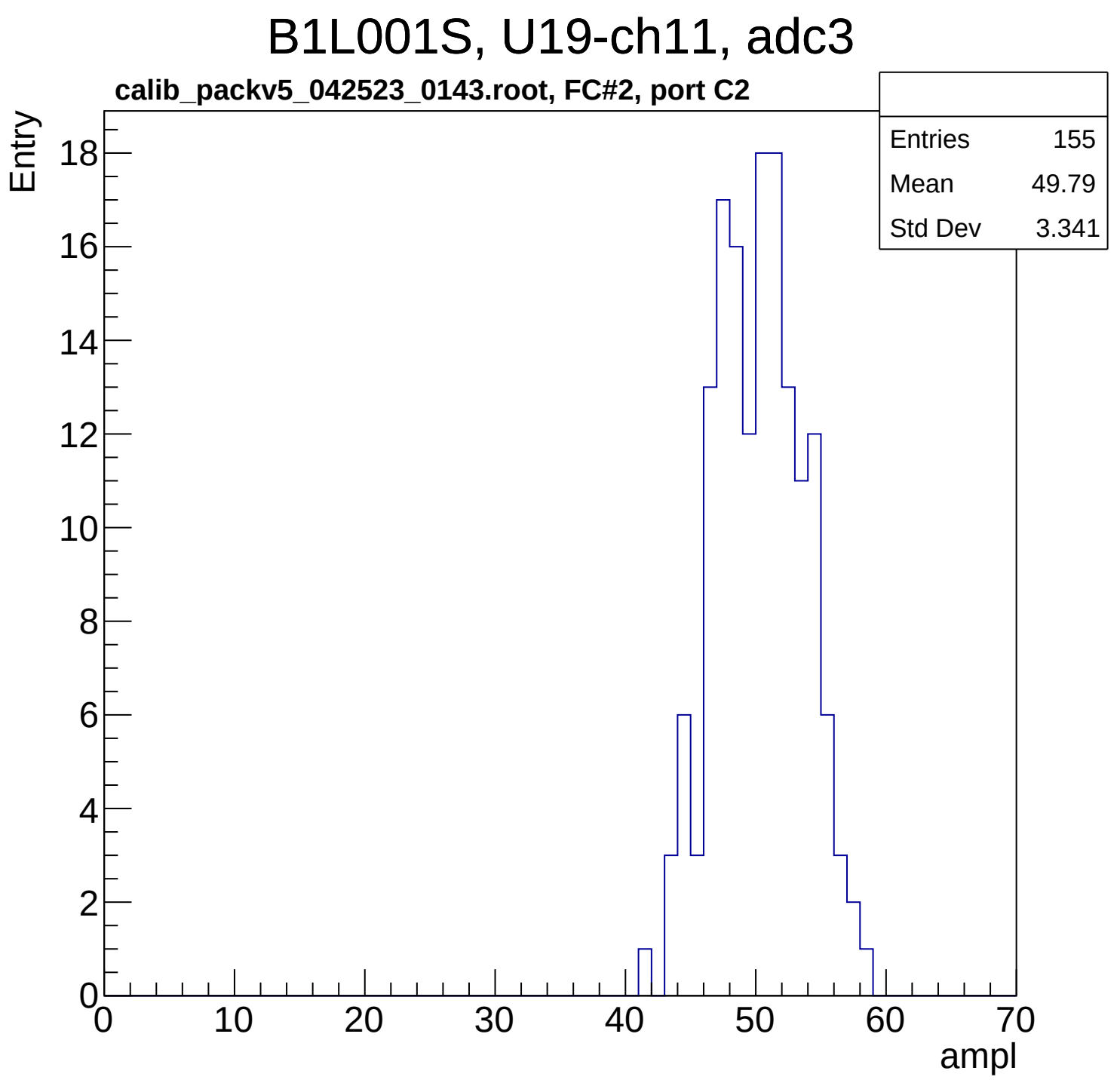
B1L001S, U19-ch11, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 155
Mean 49.79
Std Dev 3.341
Entry
ampl
0
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4
6
8
10
12
14
16
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0
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20
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40
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60
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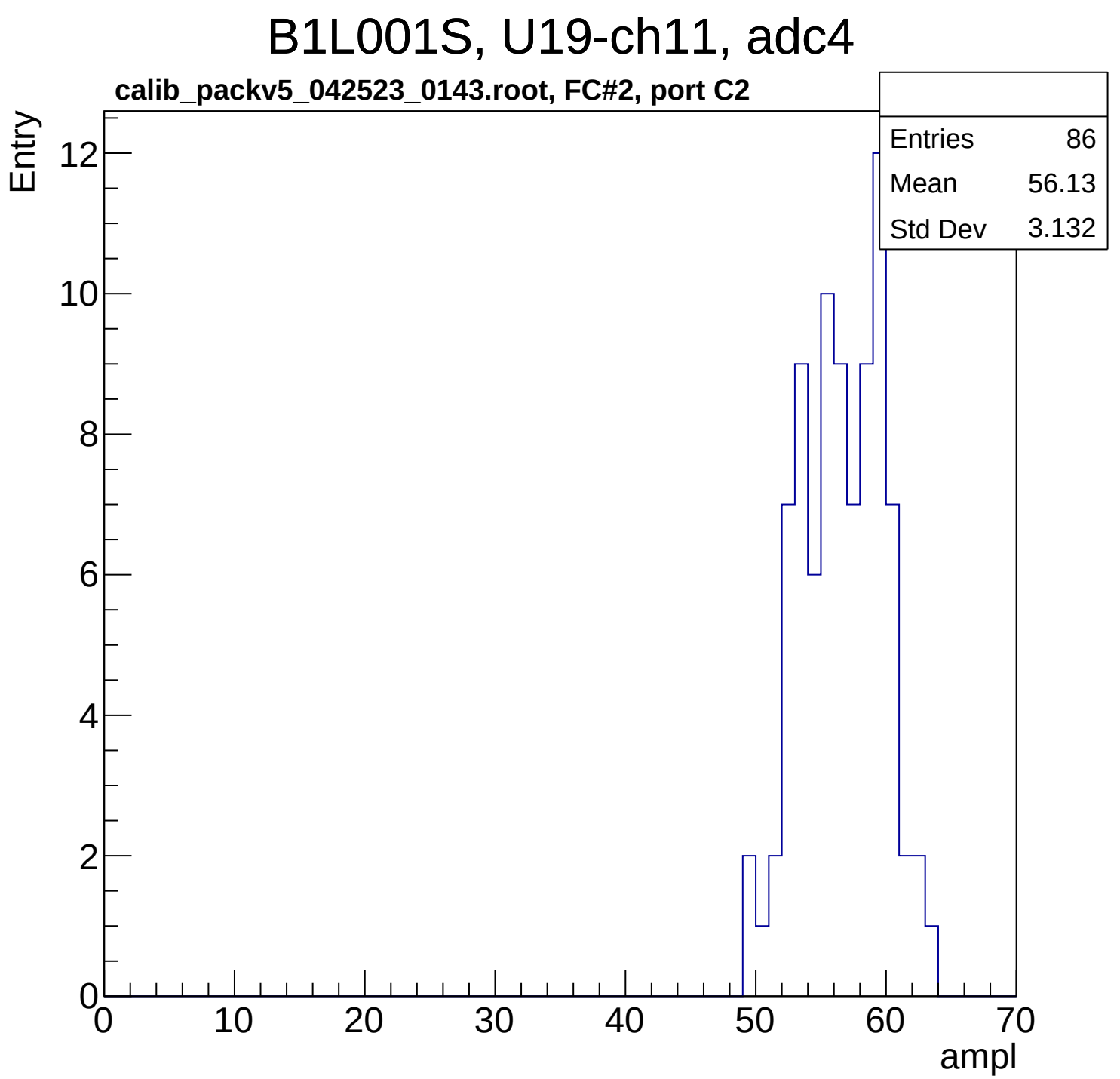
B1L001S, U19-ch11, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 86
Mean 56.13
Std Dev 3.132
Entry
ampl
0
2
4
6
8
10
12
0
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30
40
50
60
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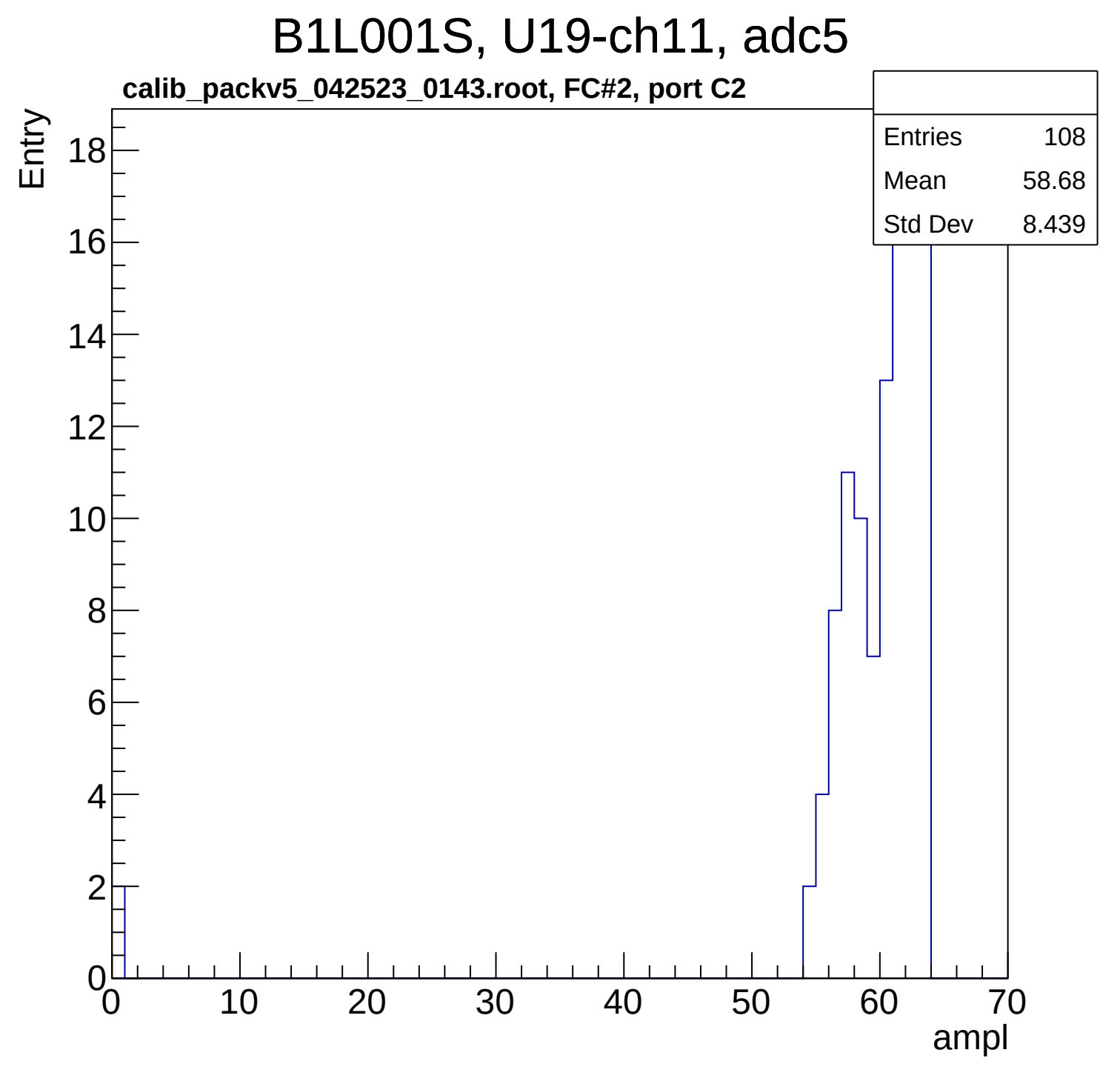
B1L001S, U19-ch11, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 108
Mean 58.68
Std Dev 8.439
Entry
ampl
0
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4
6
8
10
12
14
16
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0
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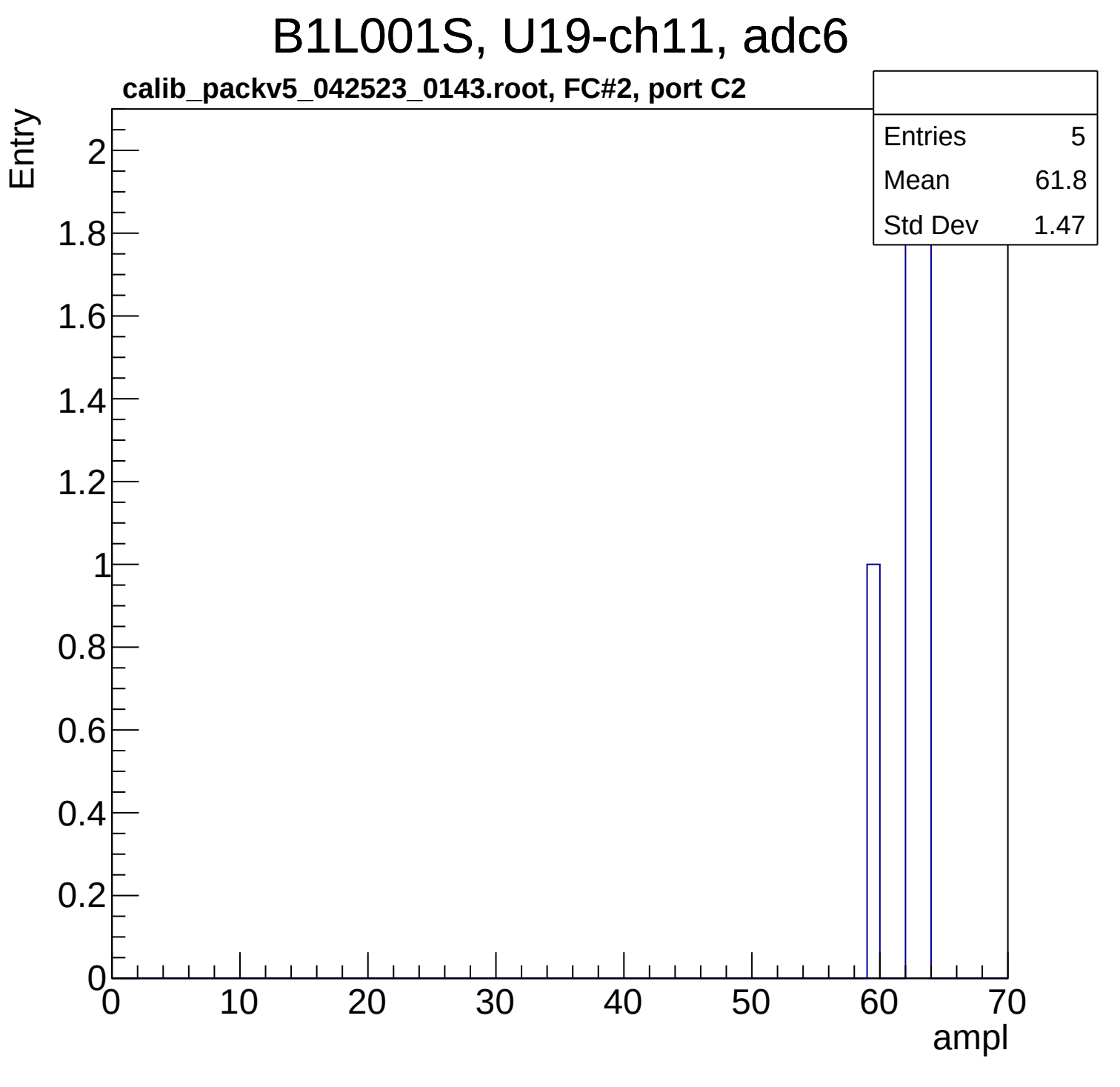
B1L001S, U19-ch11, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 5
Mean 61.8
Std Dev 1.47
Entry
ampl
0
0.2
0.4
0.6
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1
1.2
1.4
1.6
1.8
2
0
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60
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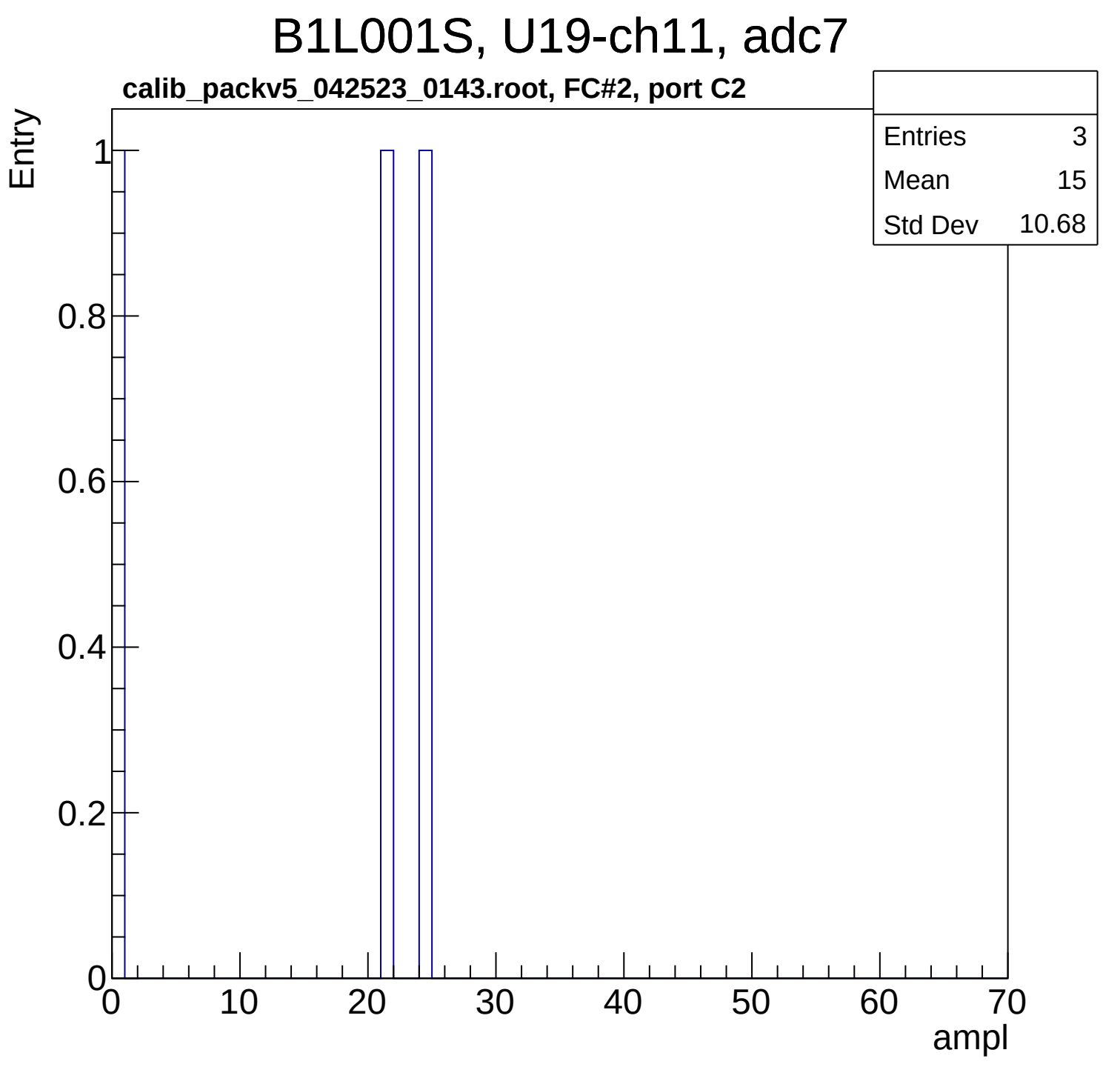
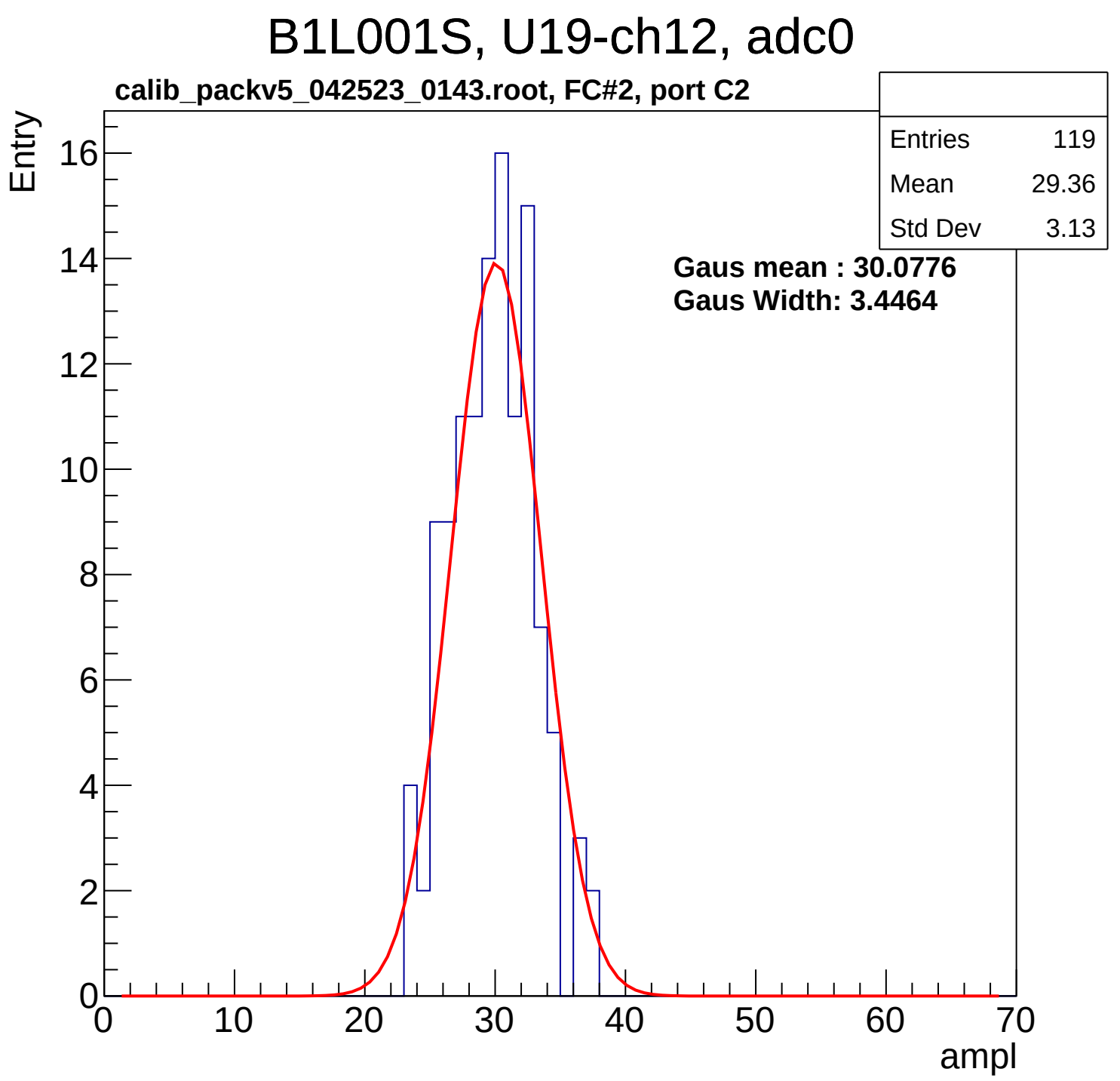

B1L001S, U19-ch11, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 3
Mean 15
Std Dev 10.68
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch12, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 119
Mean 29.36
Std Dev 3.13
Gaus mean : 30.0776
Gaus Width: 3.4464
Entry
ampl
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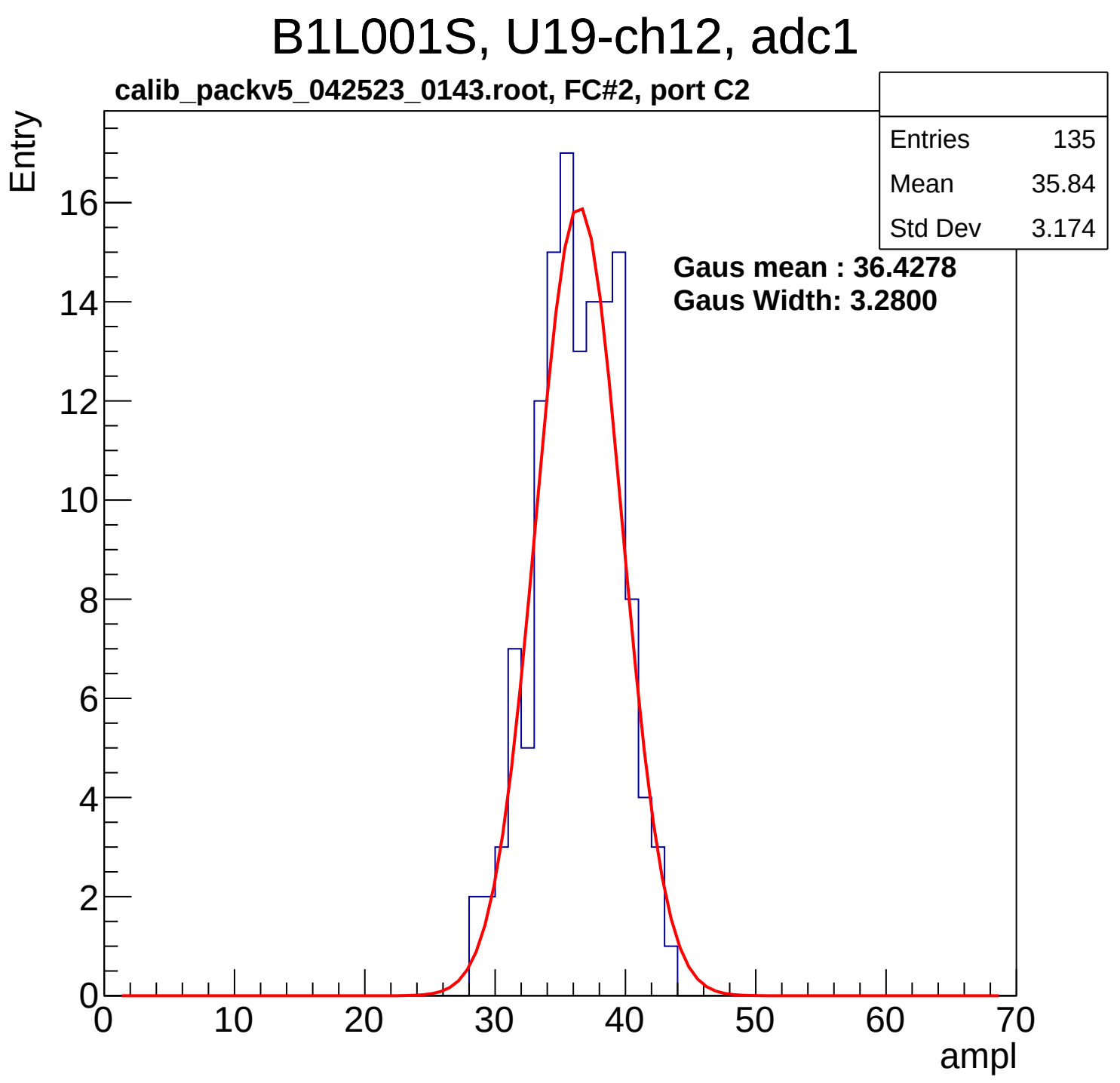
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70


B1L001S, U19-ch12, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 135
Mean 35.84
Std Dev 3.174
Gaus mean : 36.4278
Gaus Width: 3.2800
Entry
ampl
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2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
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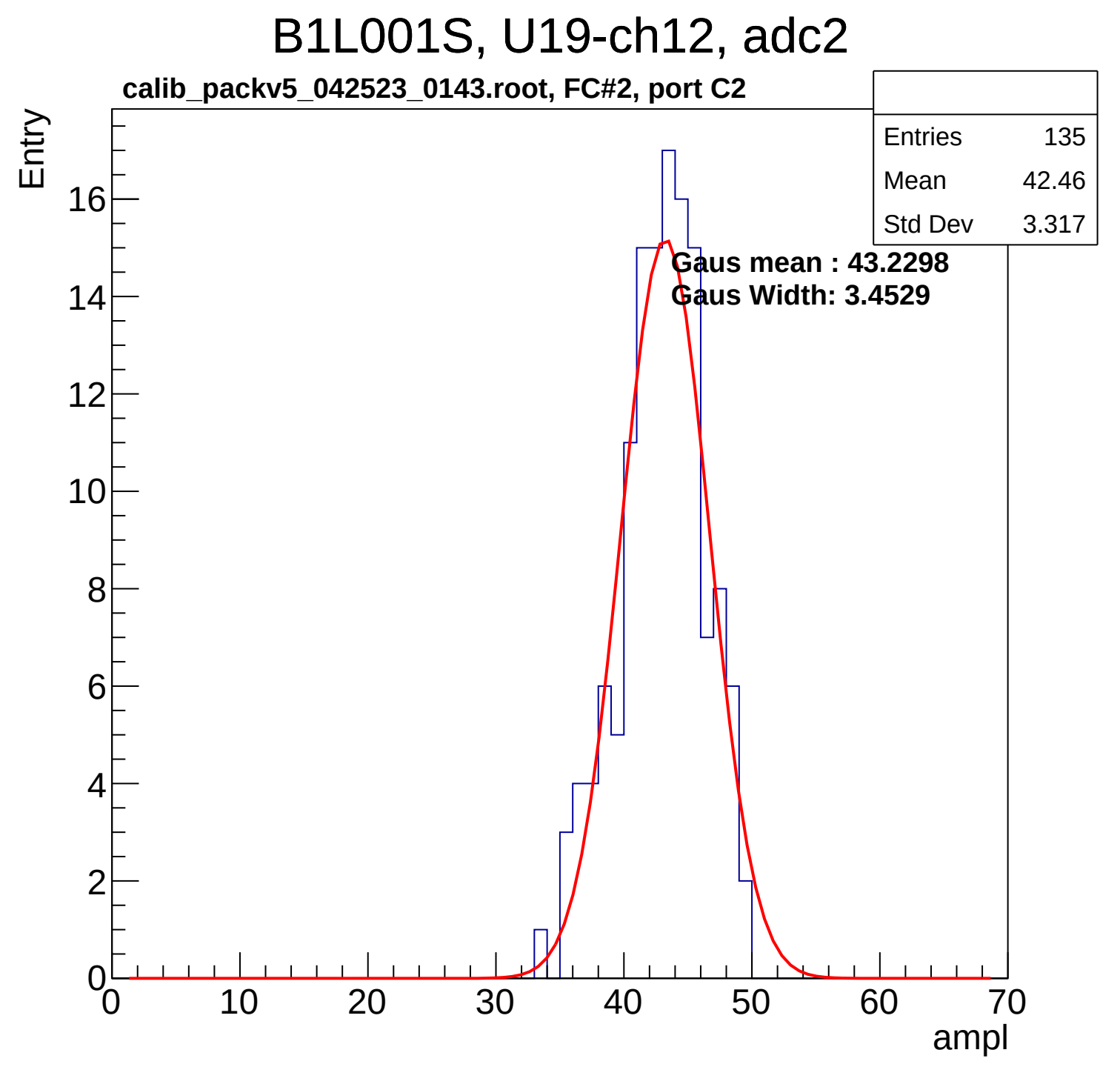
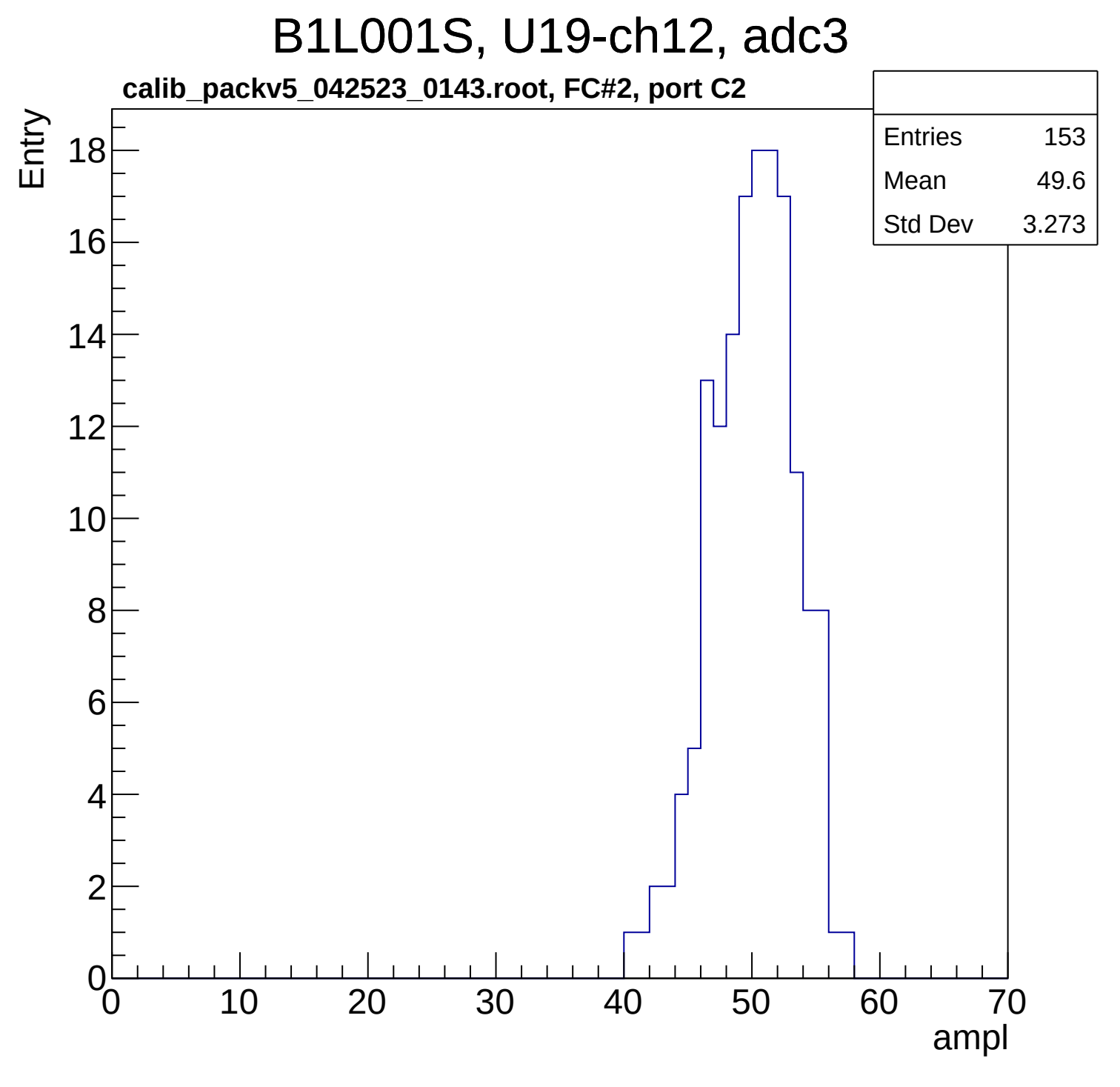
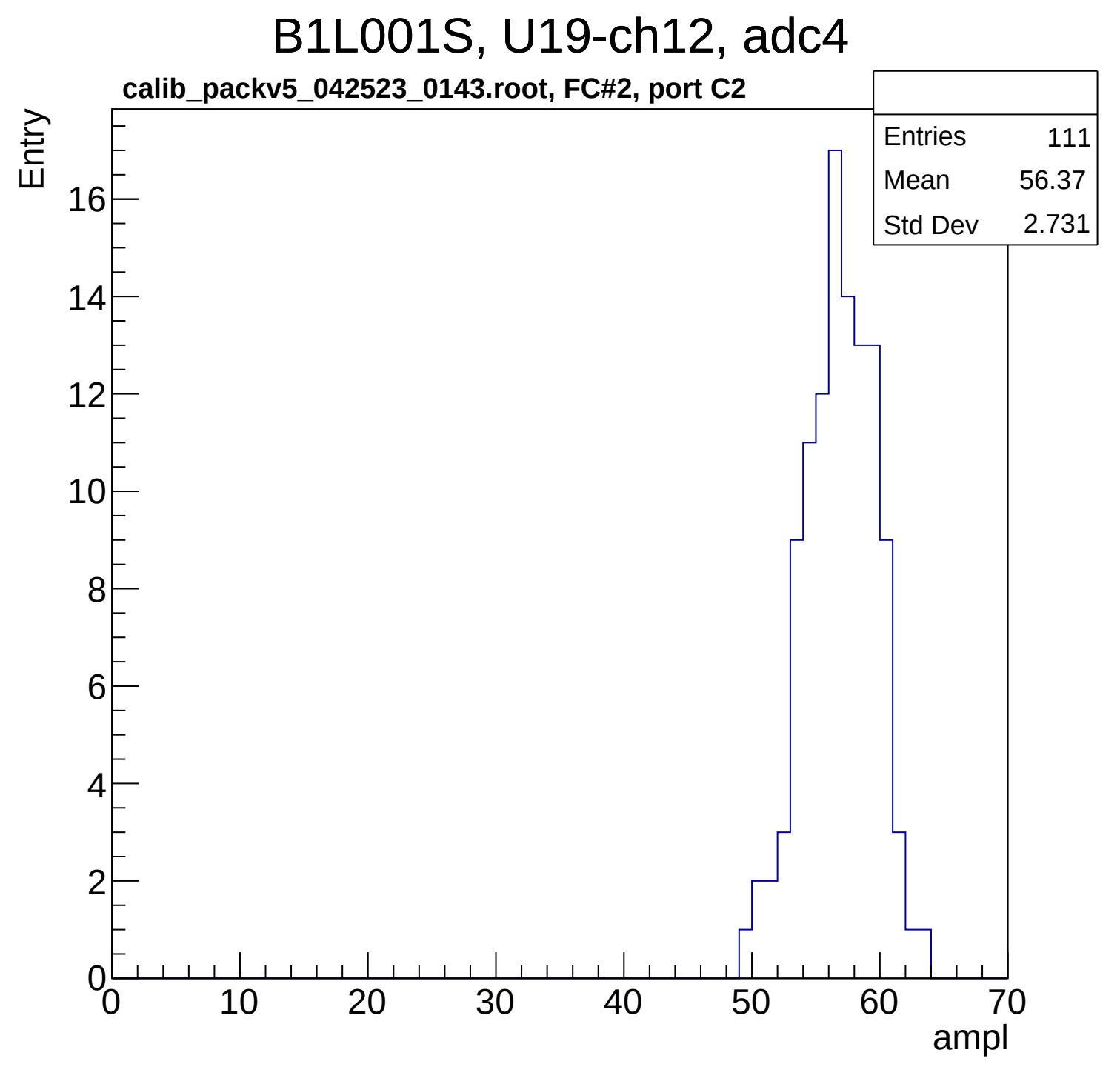

B1L001S, U19-ch12, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 135
Mean 42.46
Std Dev 3.317
Gaus mean : 43.2298
Gaus Width: 3.4529
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70


B1L001S, U19-ch12, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 153
Mean 49.6
Std Dev 3.273
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch12, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 111
Mean 56.37
Std Dev 2.731
Entry
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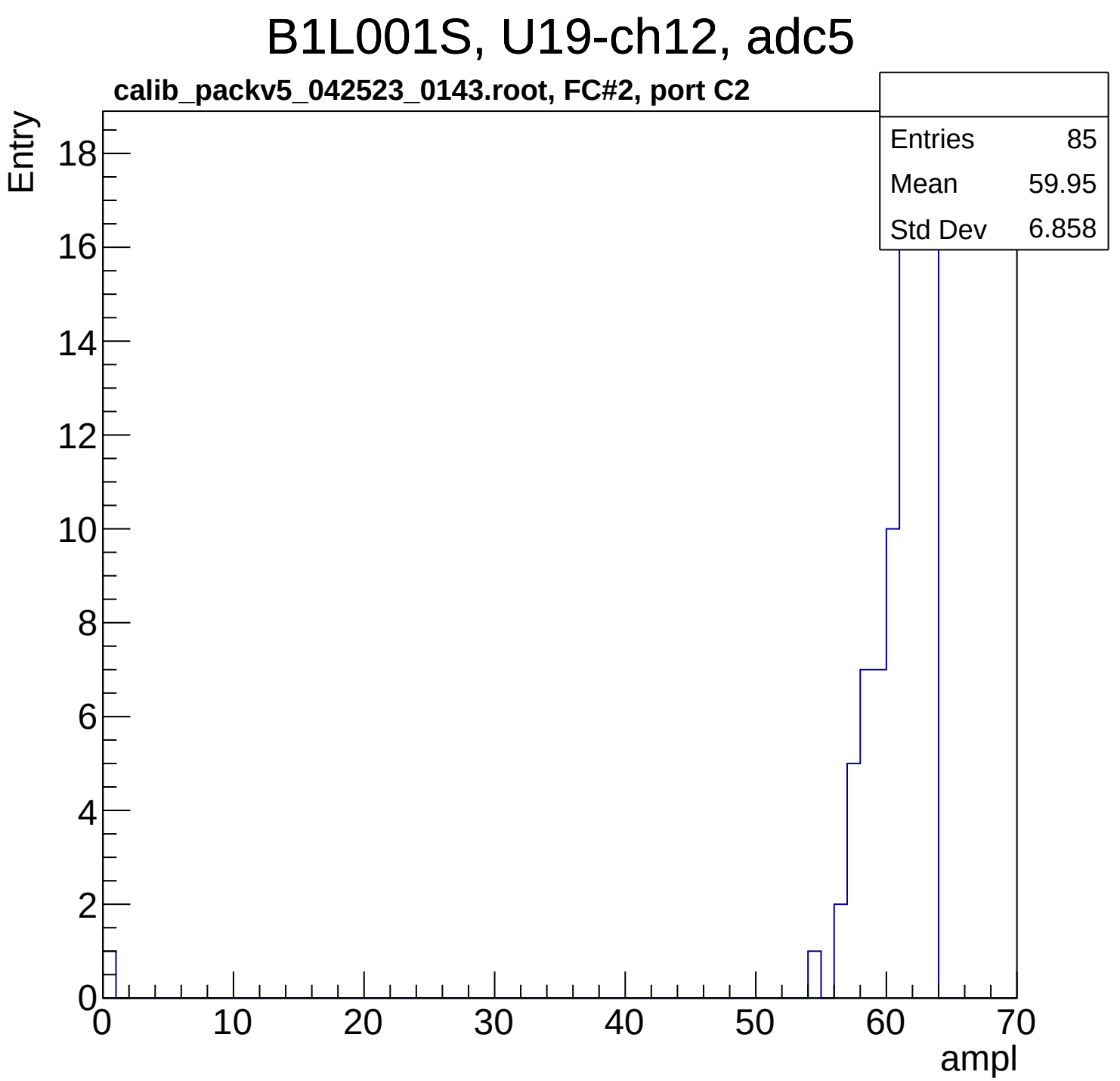
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch12, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 85
Mean 59.95
Std Dev 6.858
Entry
ampl
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4
6
8
10
12
14
16
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0
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60
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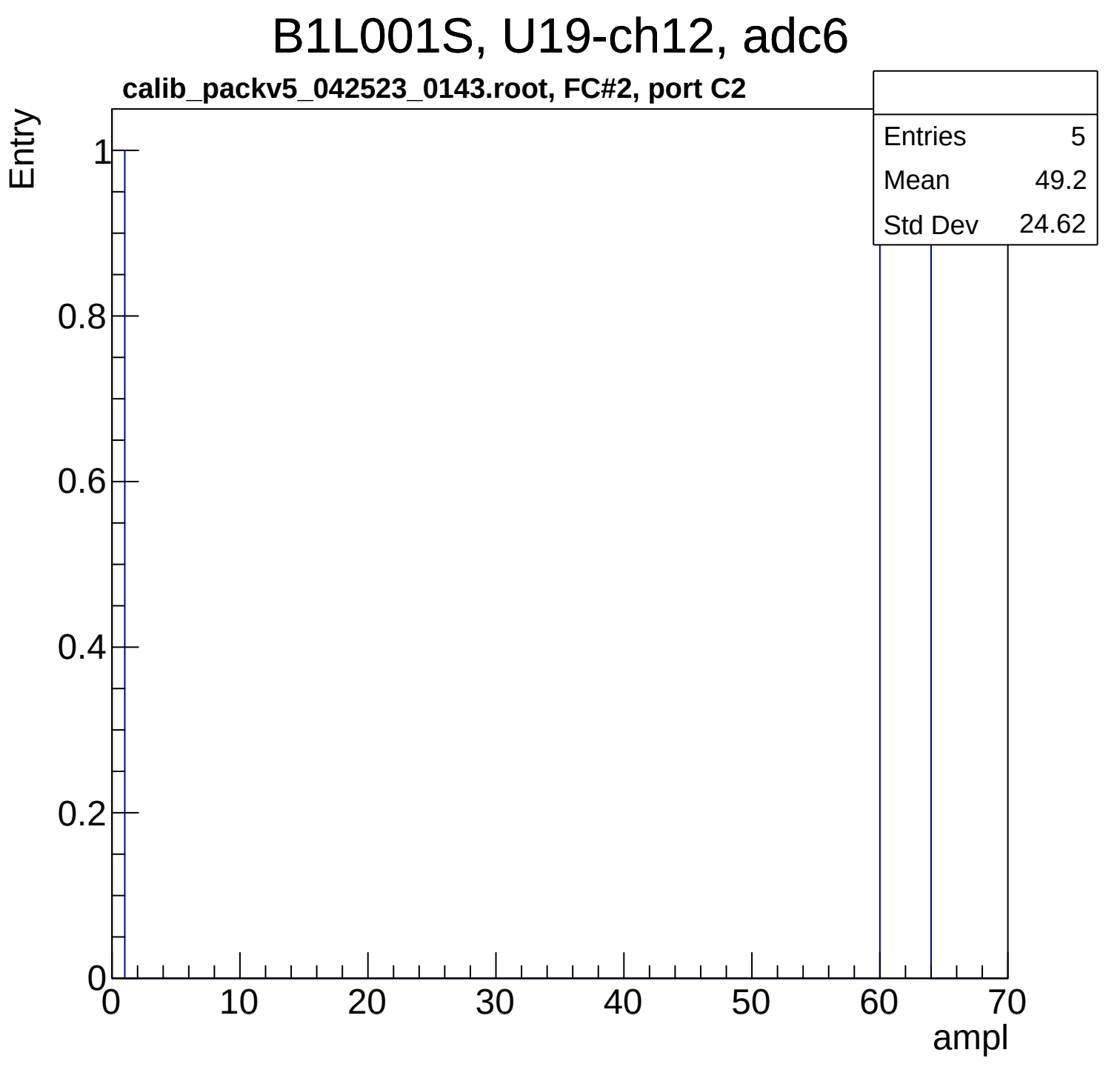
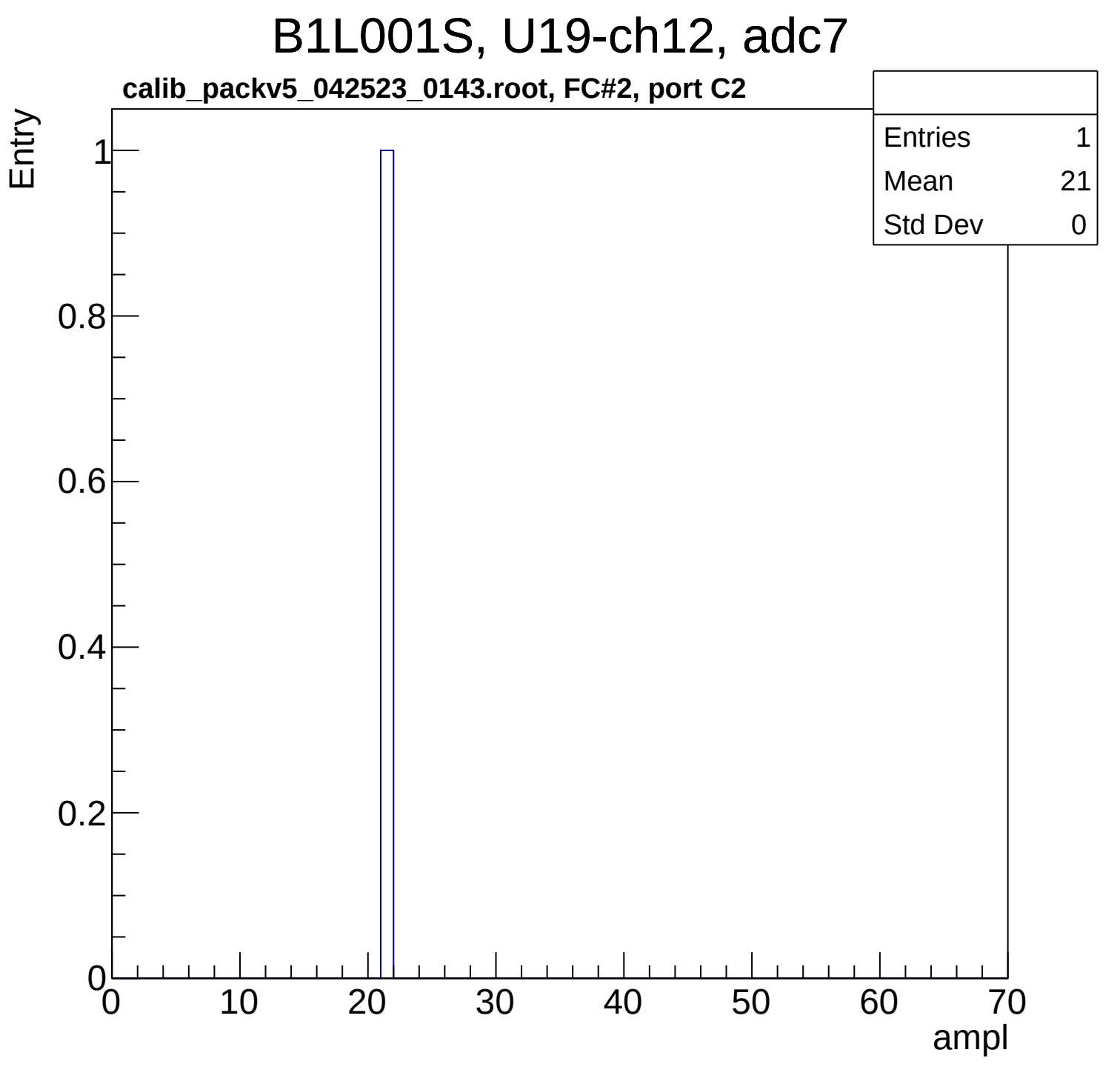
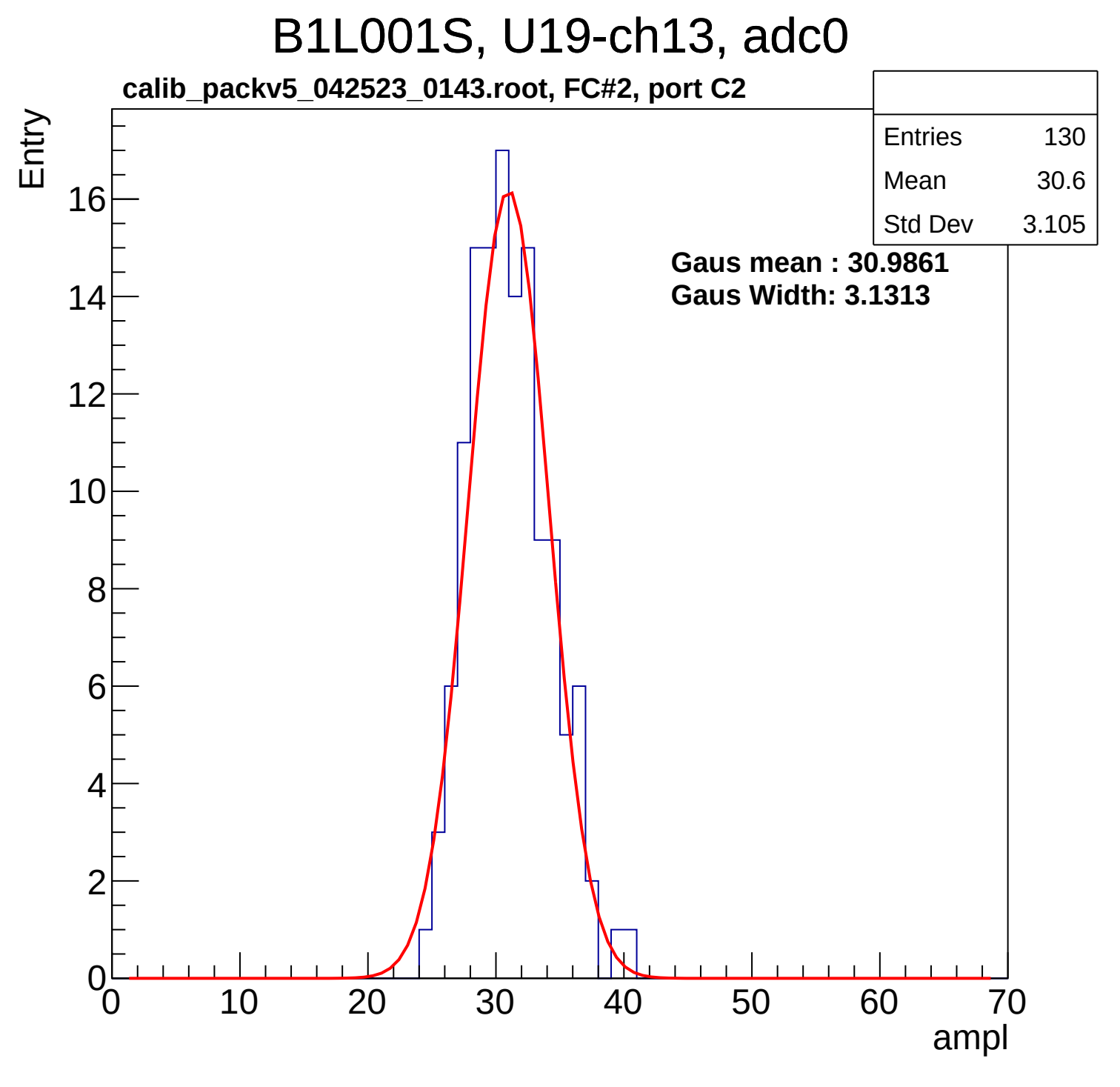
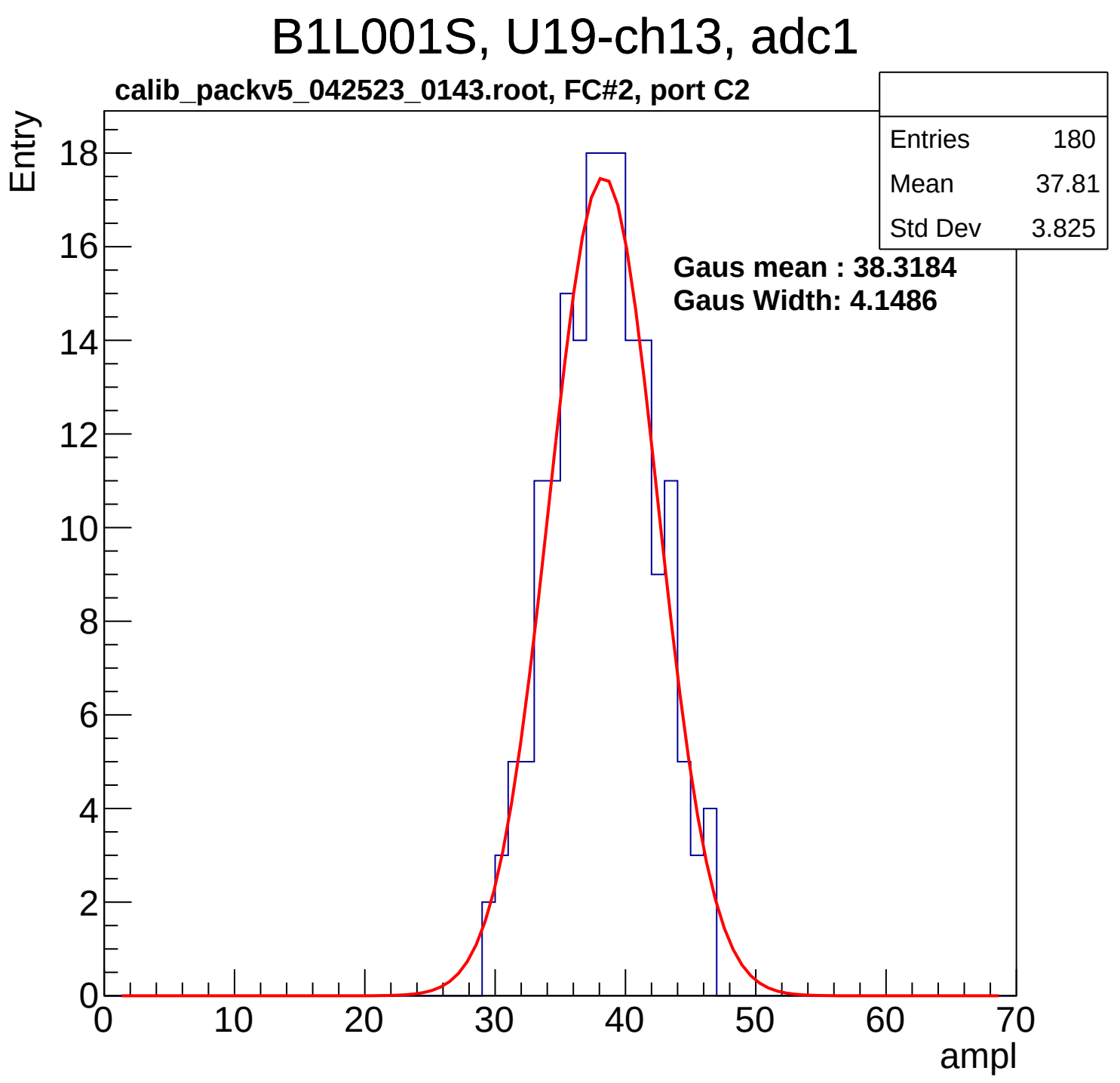

B1L001S, U19-ch12, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 5
Mean 49.2
Std Dev 24.62
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch12, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 21
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch13, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 130
Mean 30.6
Std Dev 3.105
Gaus mean : 30.9861
Gaus Width: 3.1313
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70


B1L001S, U19-ch13, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 180
Mean 37.81
Std Dev 3.825
Gaus mean : 38.3184
Gaus Width: 4.1486
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
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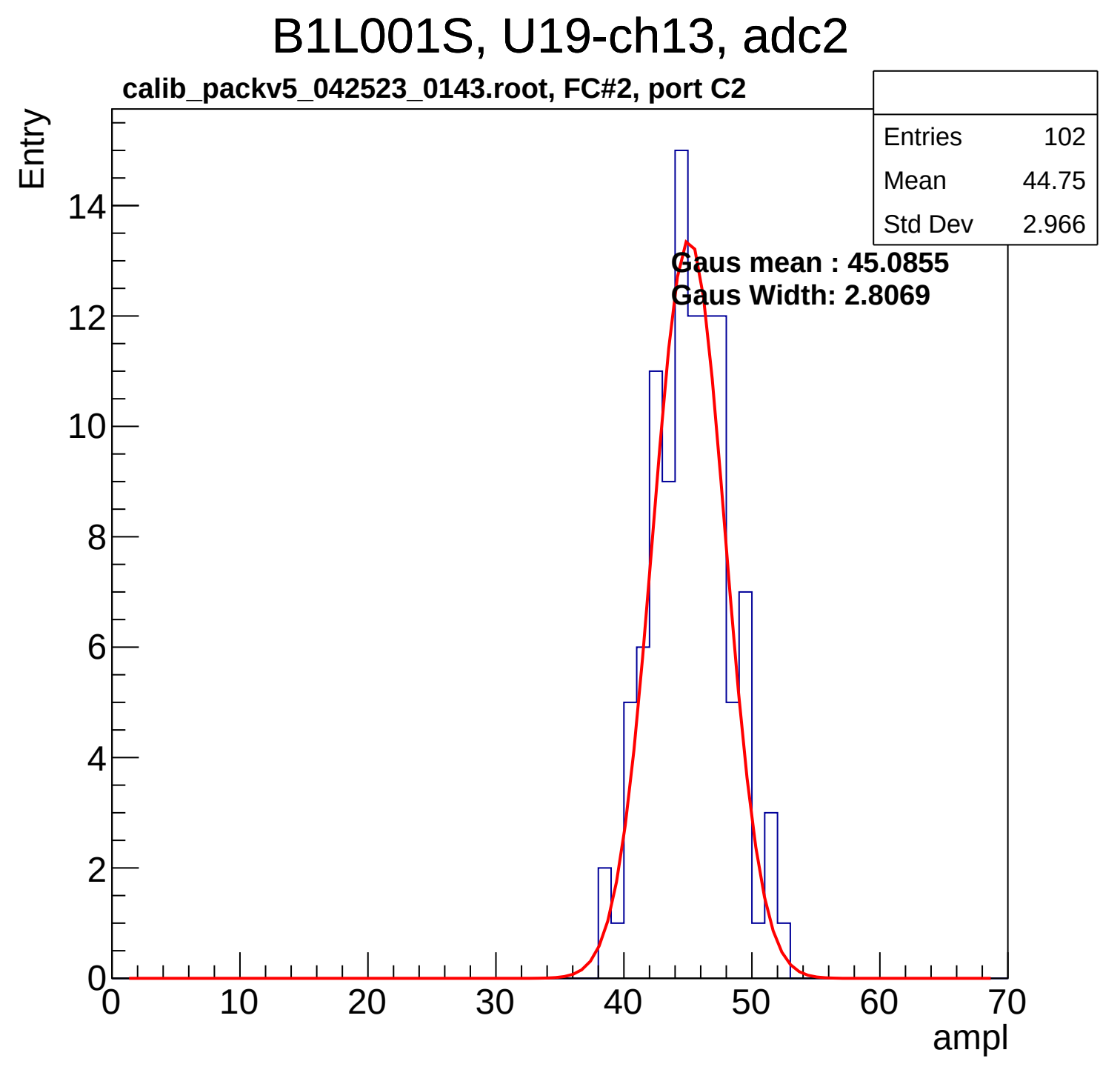
B1L001S, U19-ch13, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 102
Mean 44.75
Std Dev 2.966
Gaus mean : 45.0855
Gaus Width: 2.8069
Entry
ampl
0
2
4
6
8
10
12
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0
10
20
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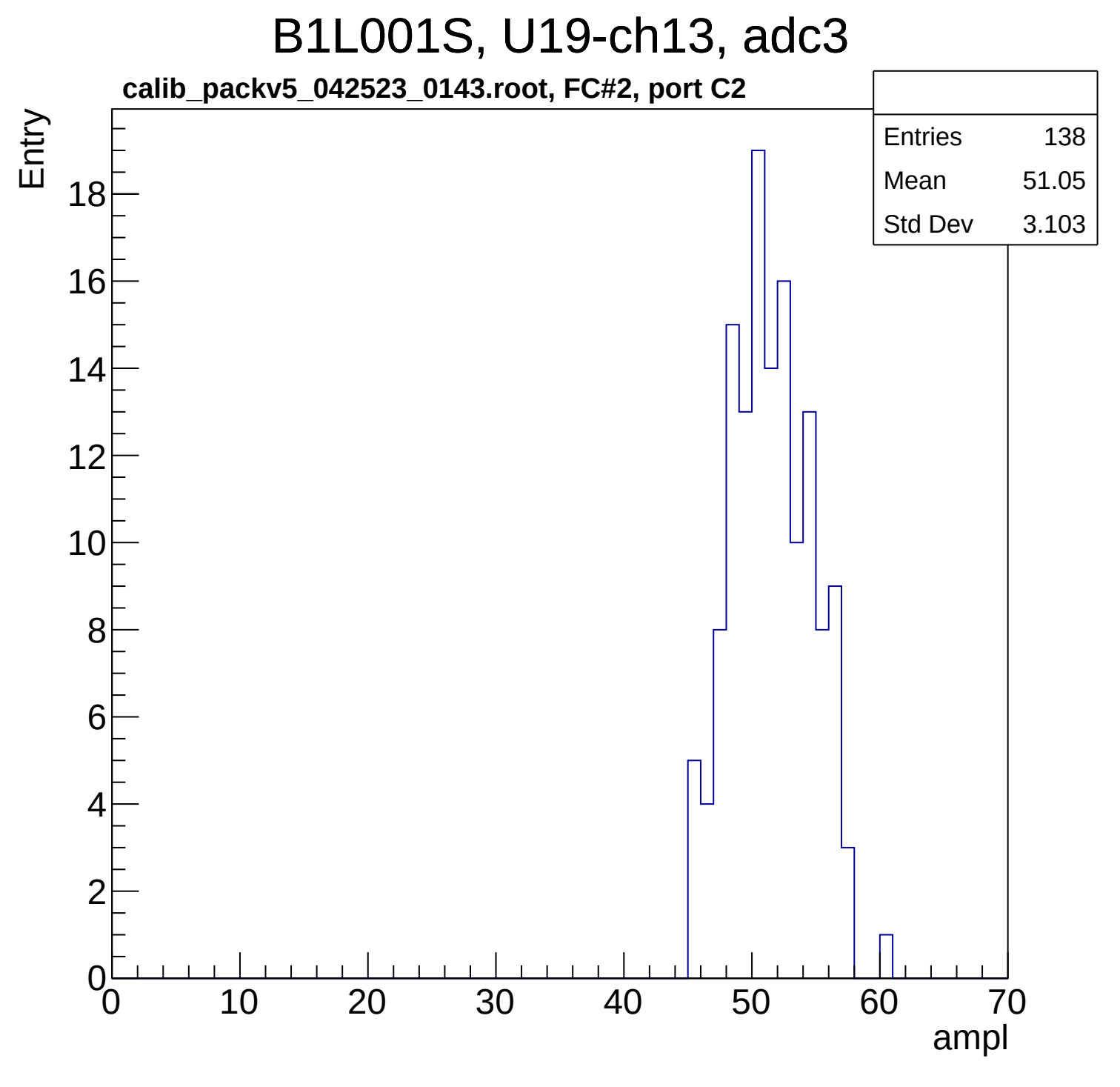
40
50
60
70


B1L001S, U19-ch13, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 138
Mean 51.05
Std Dev 3.103
Entry
ampl
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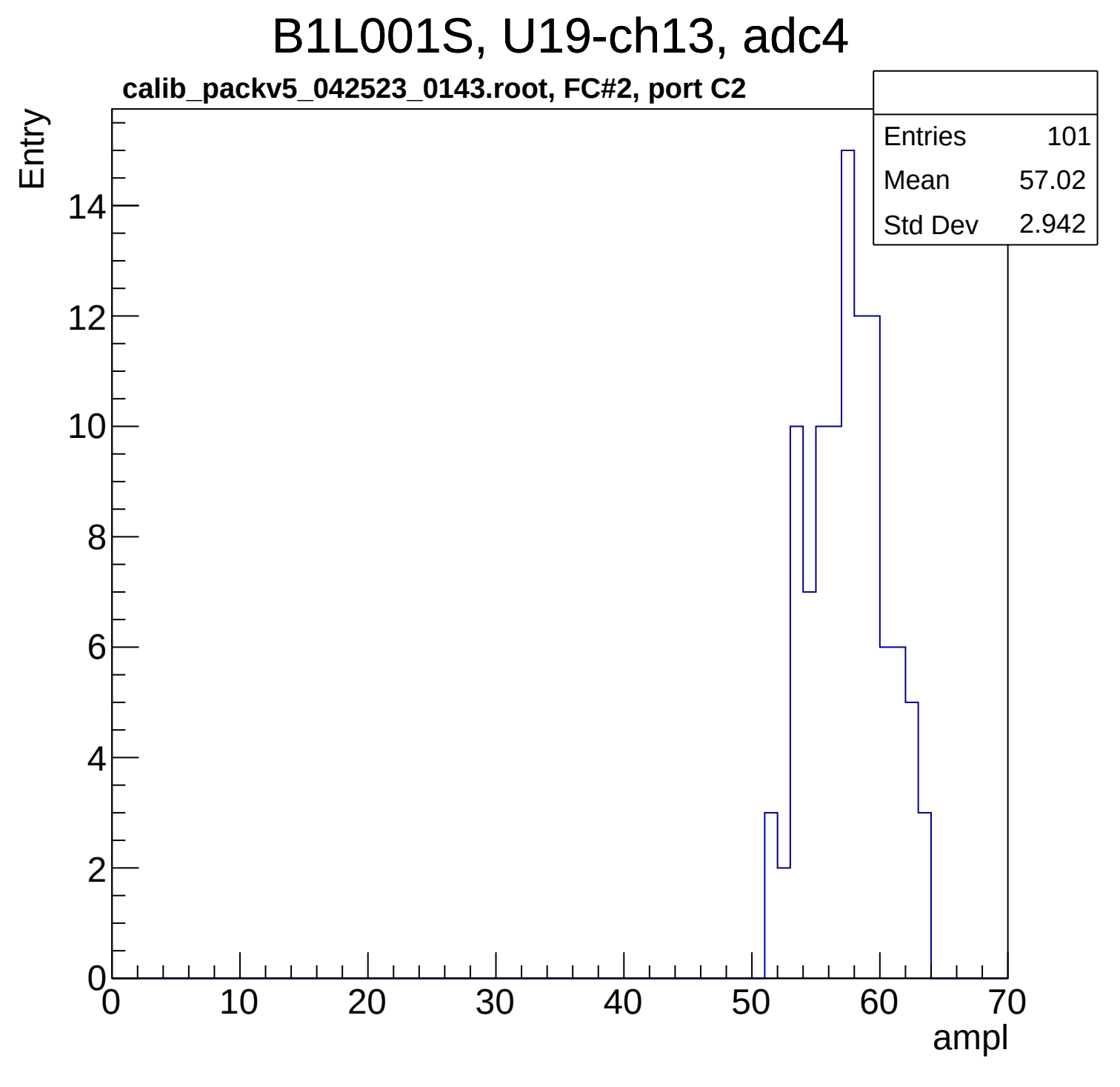
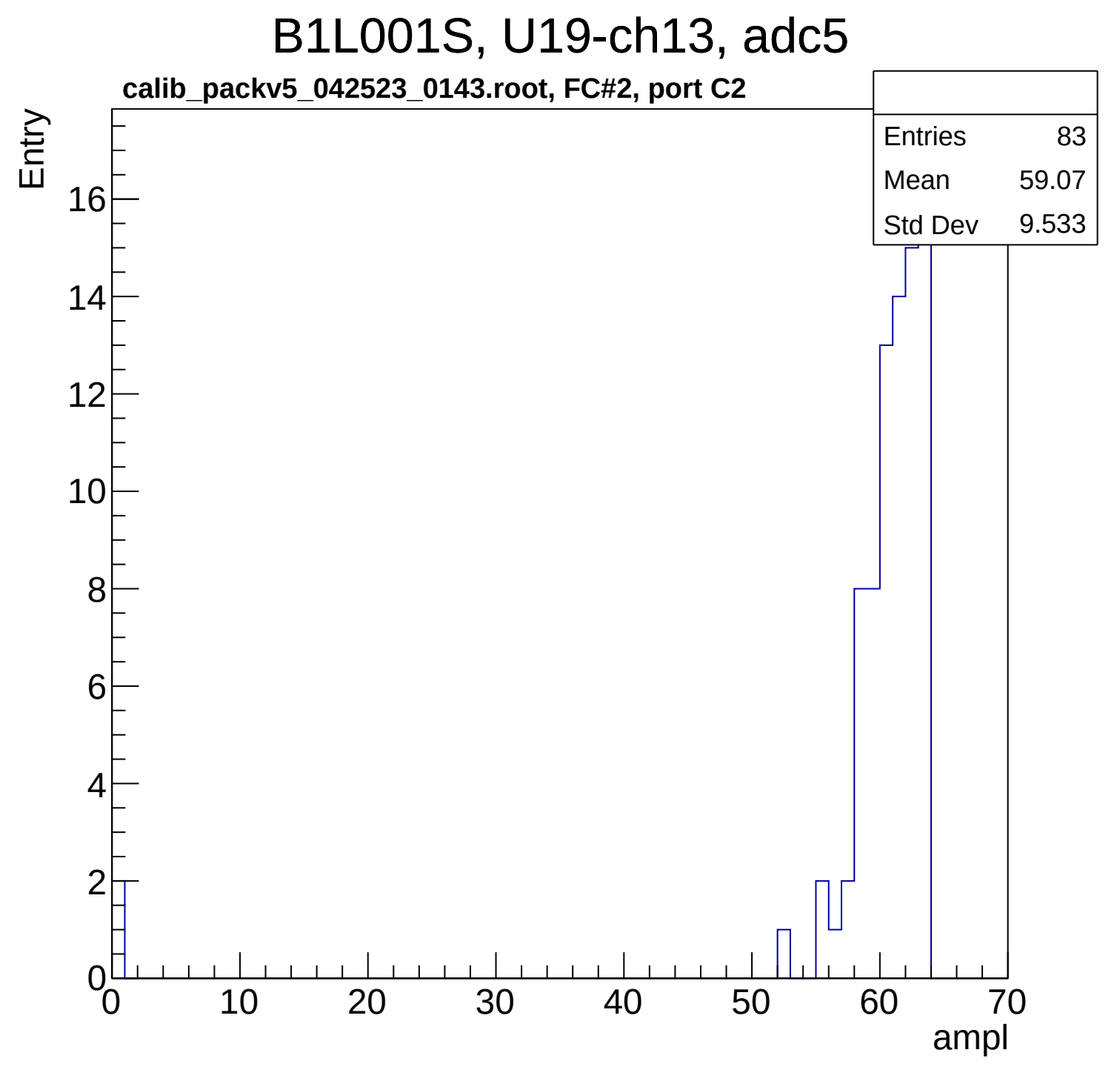
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70


B1L001S, U19-ch13, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 101
Mean 57.02
Std Dev 2.942
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch13, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 83
Mean 59.07
Std Dev 9.533
Entry
ampl
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2
4
6
8
10
12
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0
10
20
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60
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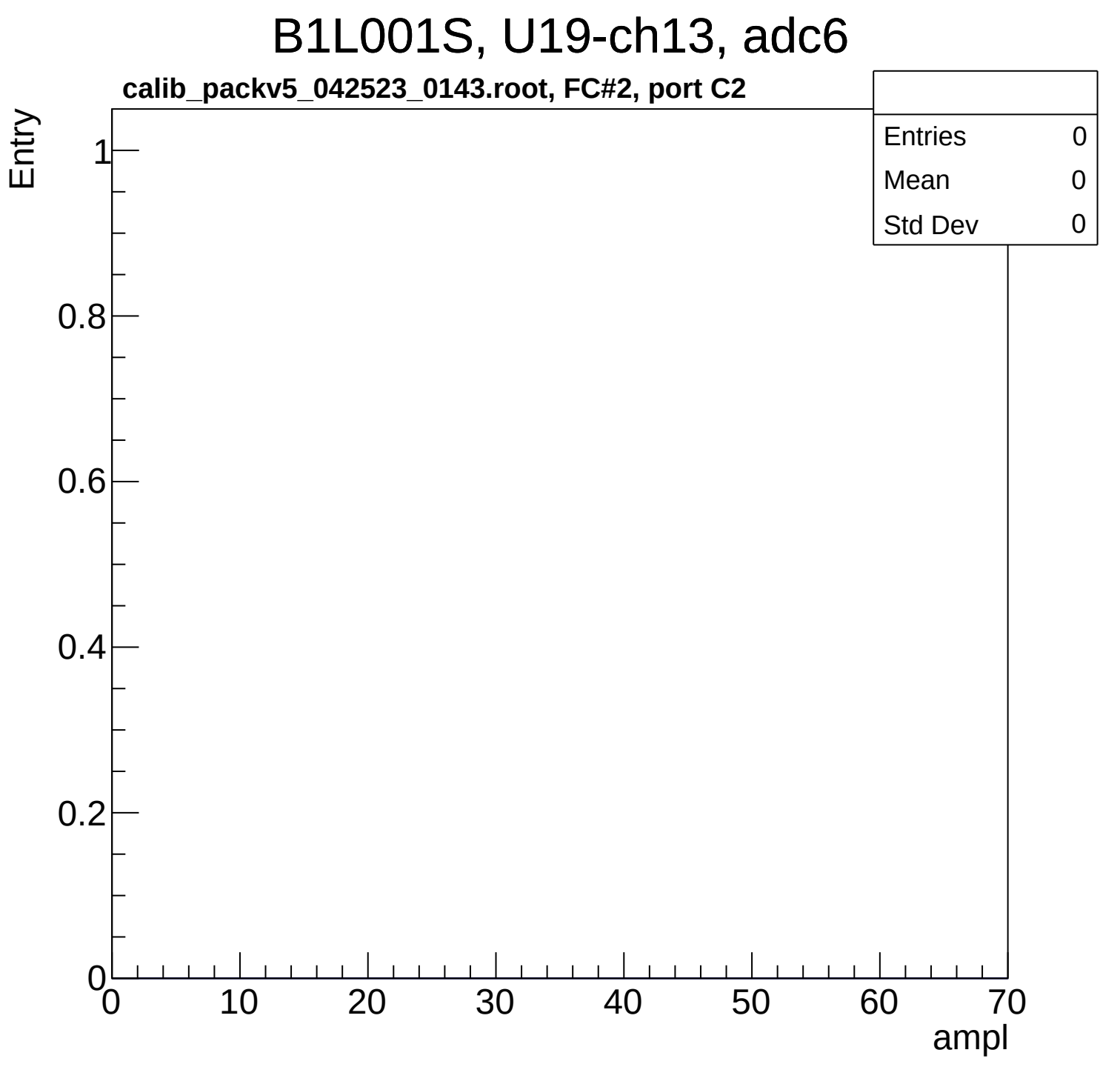
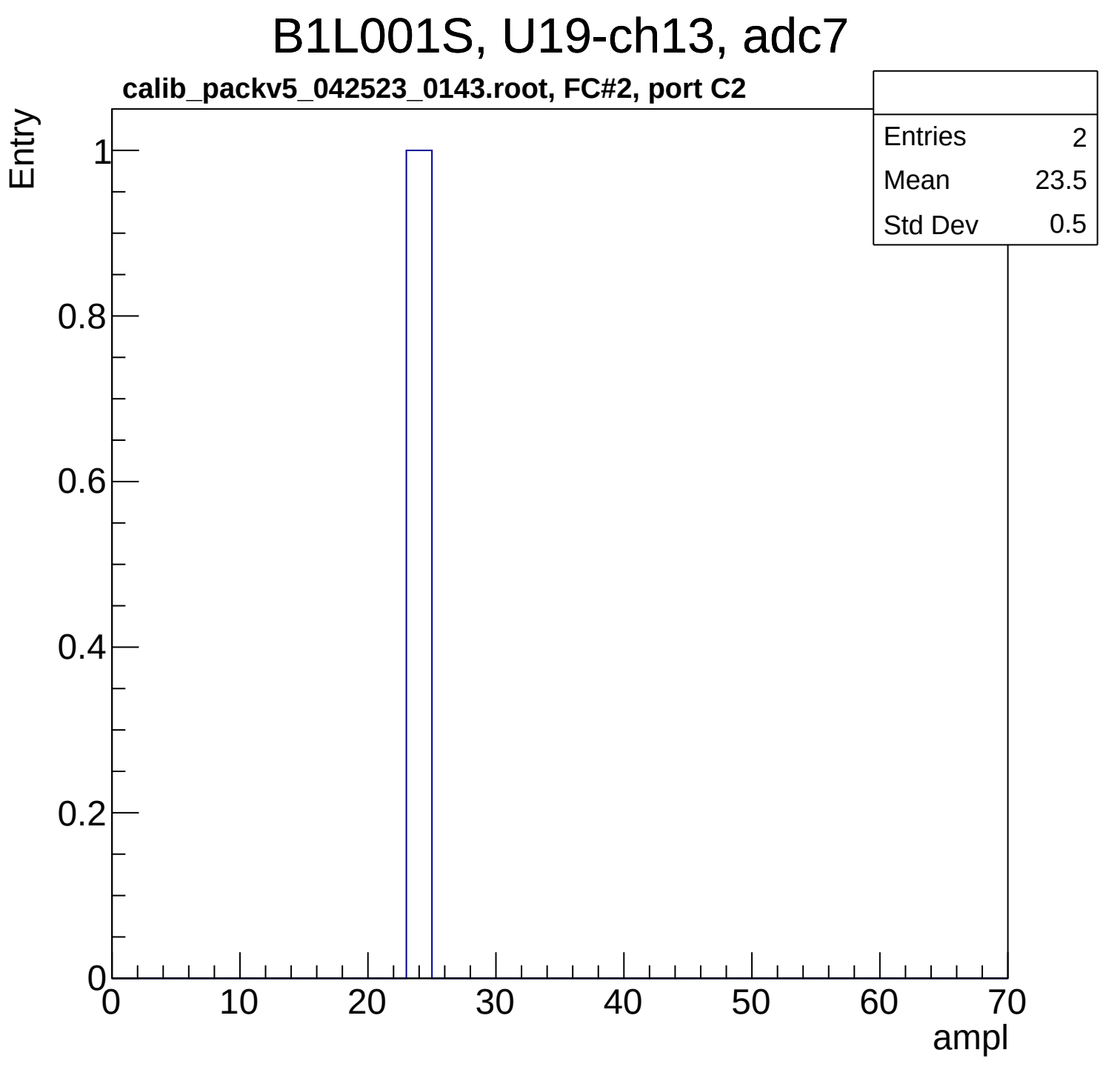

B1L001S, U19-ch13, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch13, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 23.5
Std Dev 0.5
Entry
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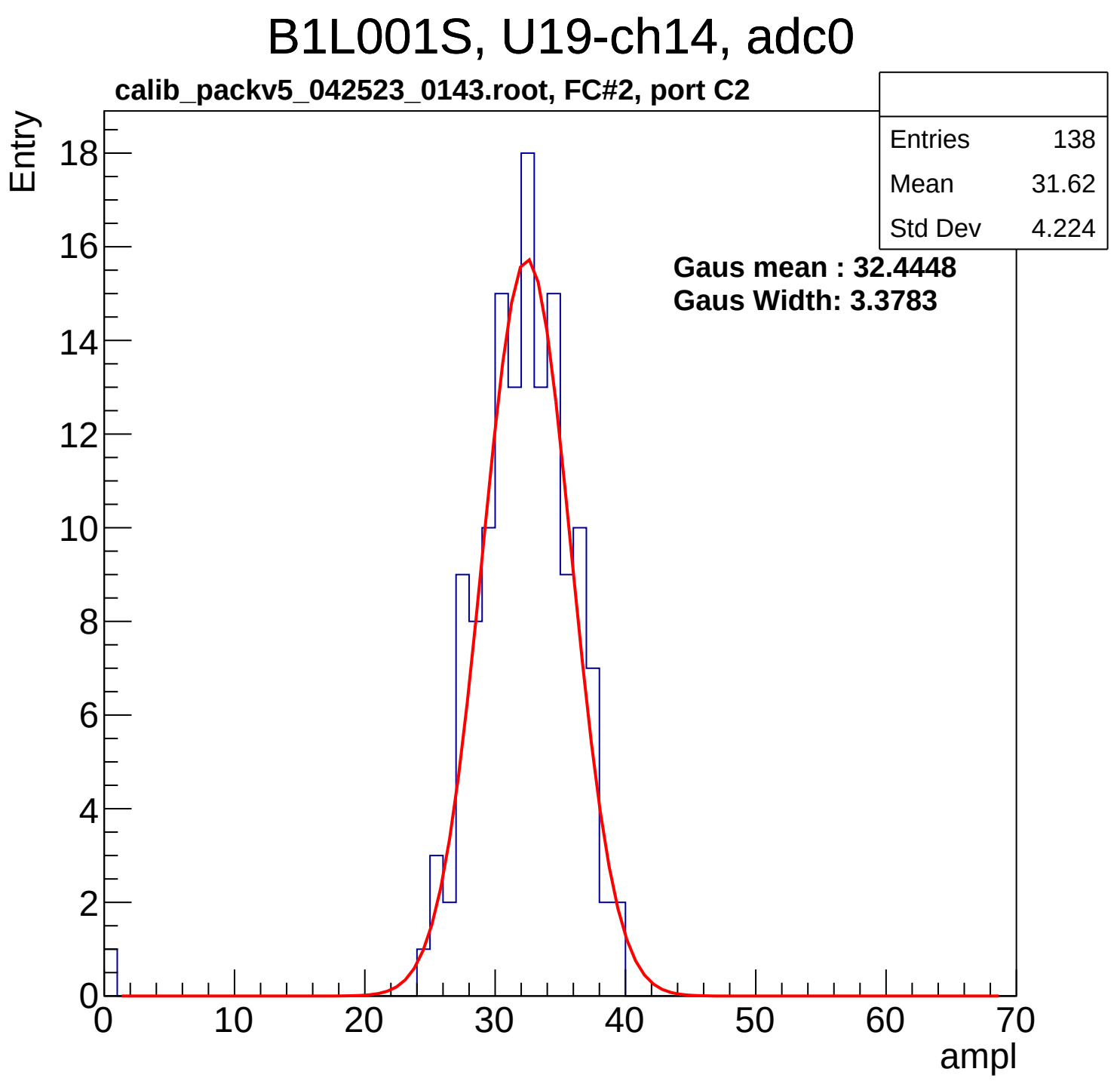
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch14, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 138
Mean 31.62
Std Dev 4.224
Gaus mean : 32.4448
Gaus Width: 3.3783
Entry
ampl
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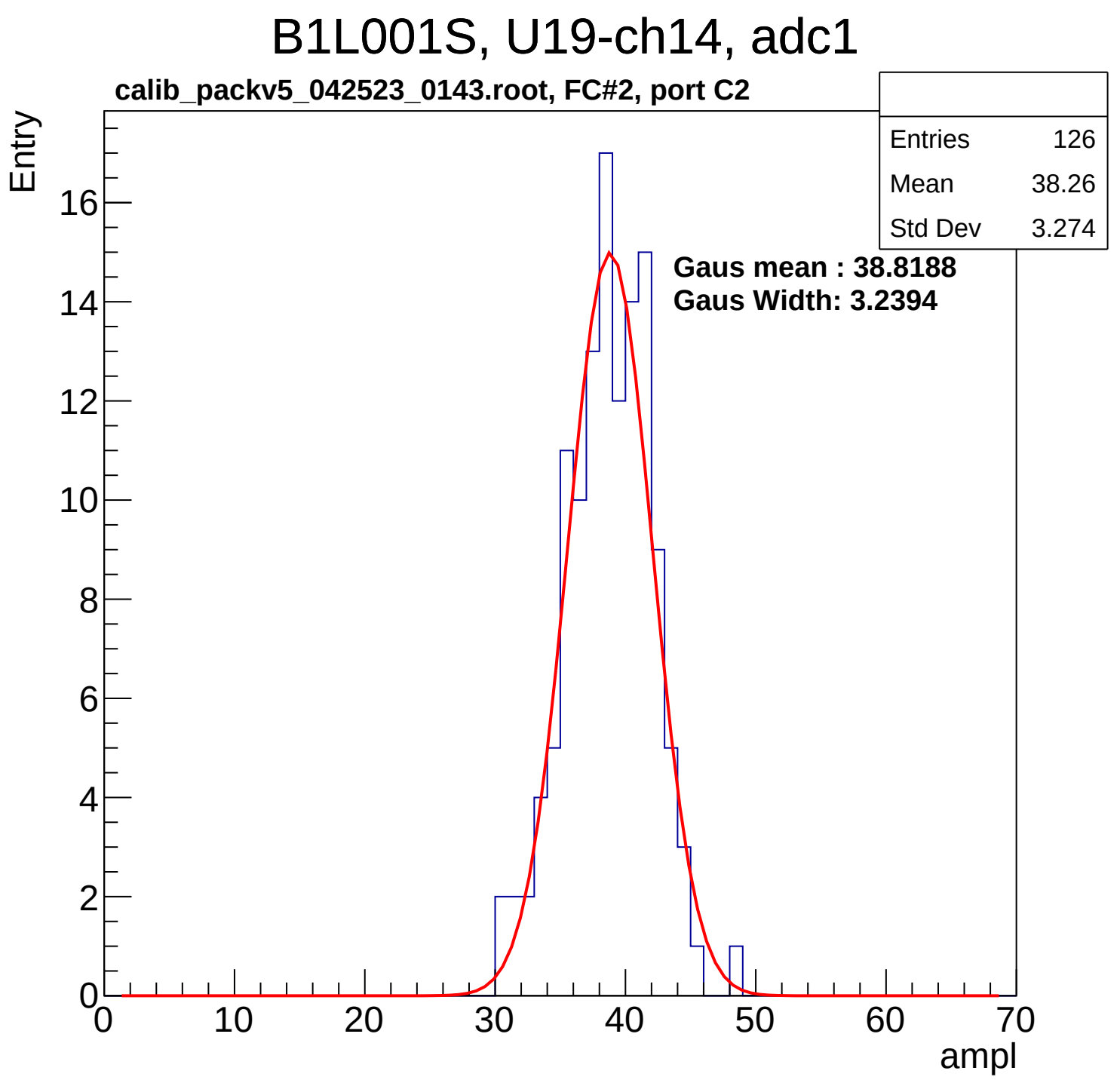
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70


B1L001S, U19-ch14, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 126
Mean 38.26
Std Dev 3.274
Gaus mean : 38.8188
Gaus Width: 3.2394
Entry
ampl
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2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
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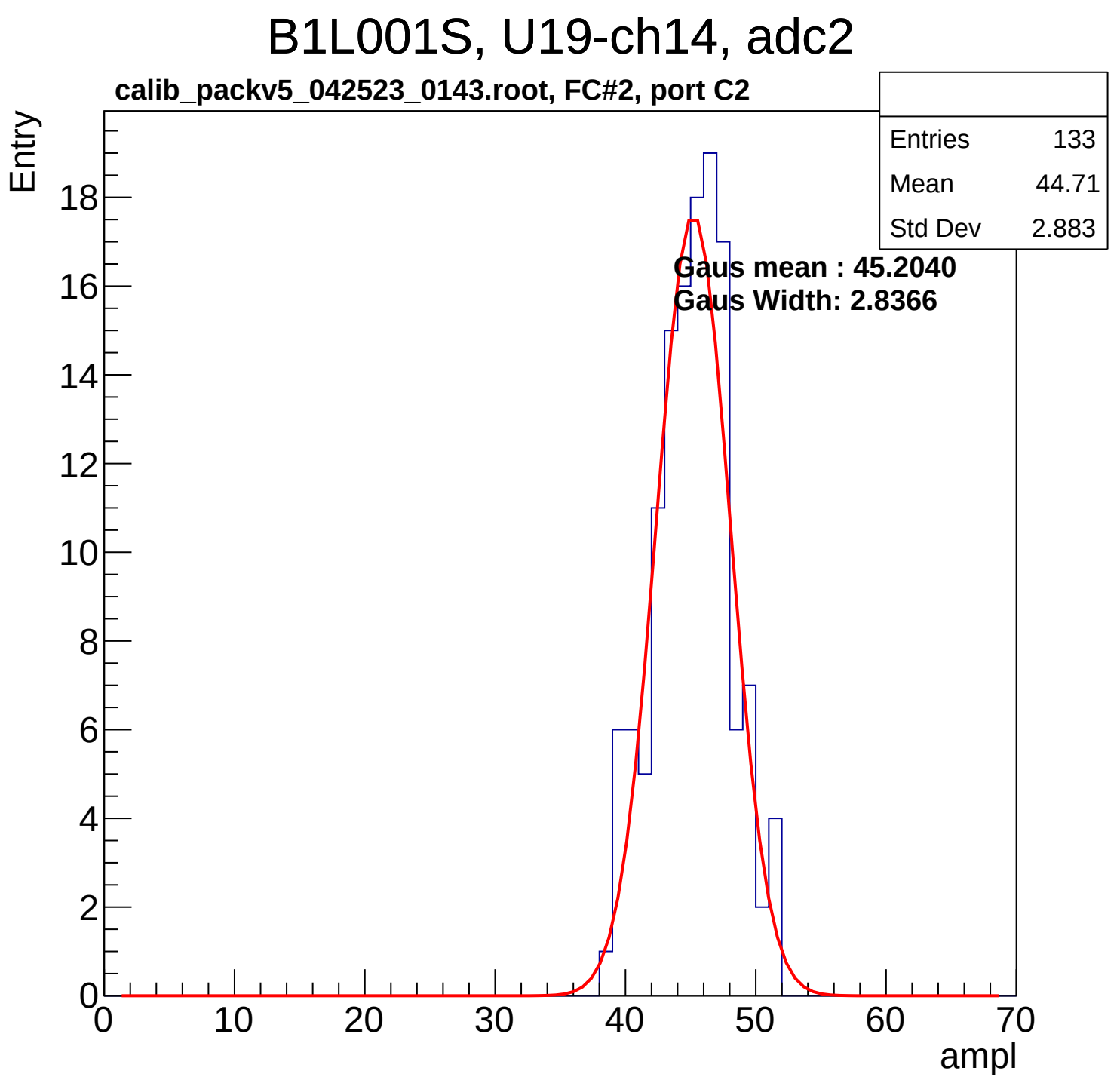
B1L001S, U19-ch14, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 133
Mean 44.71
Std Dev 2.883
Gaus mean : 45.2040
Gaus Width: 2.8366
Entry
ampl
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2
4
6
8
10
12
14
16
18
0
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20
30
40
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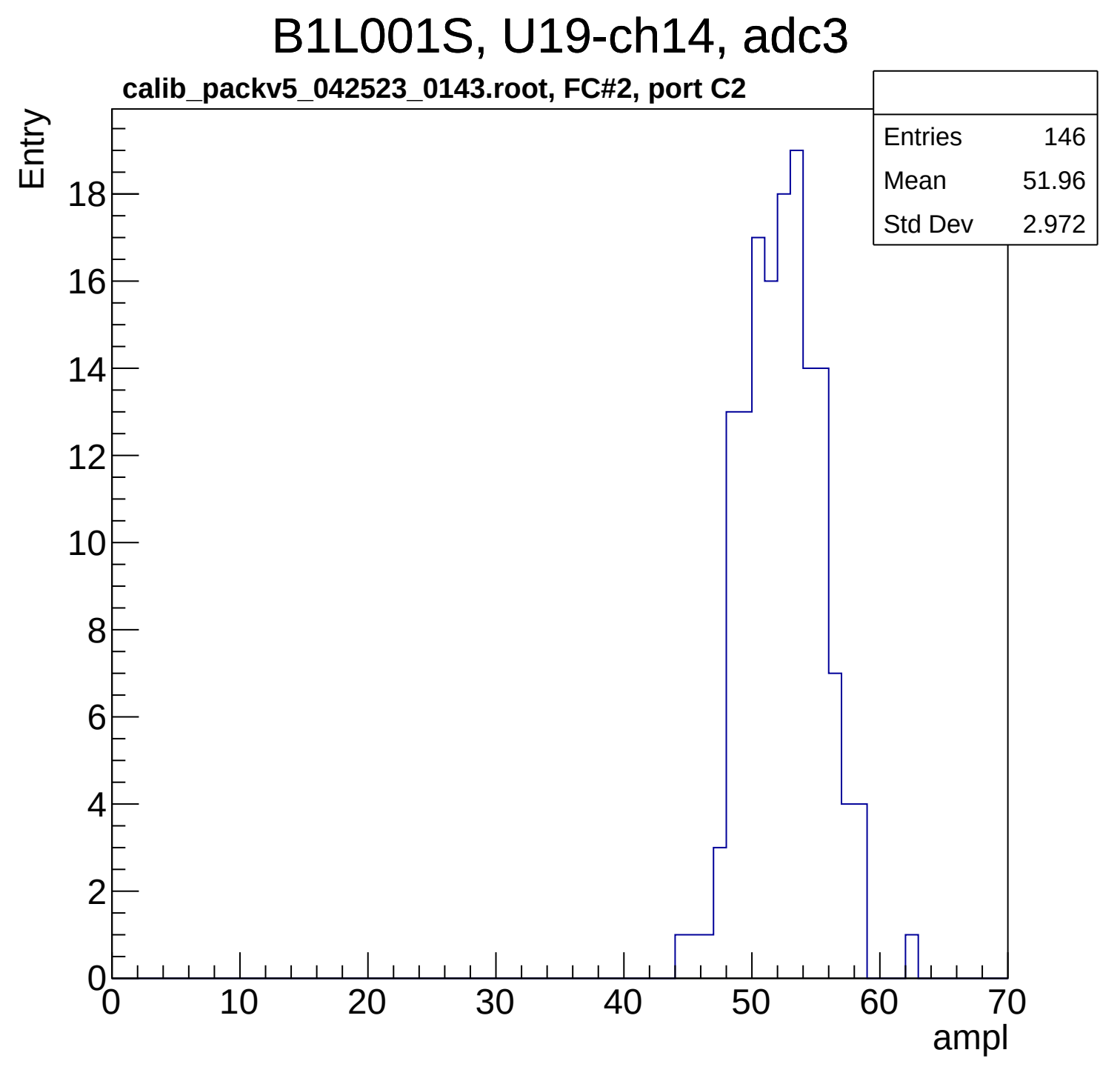
60
70


B1L001S, U19-ch14, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 146
Mean 51.96
Std Dev 2.972
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
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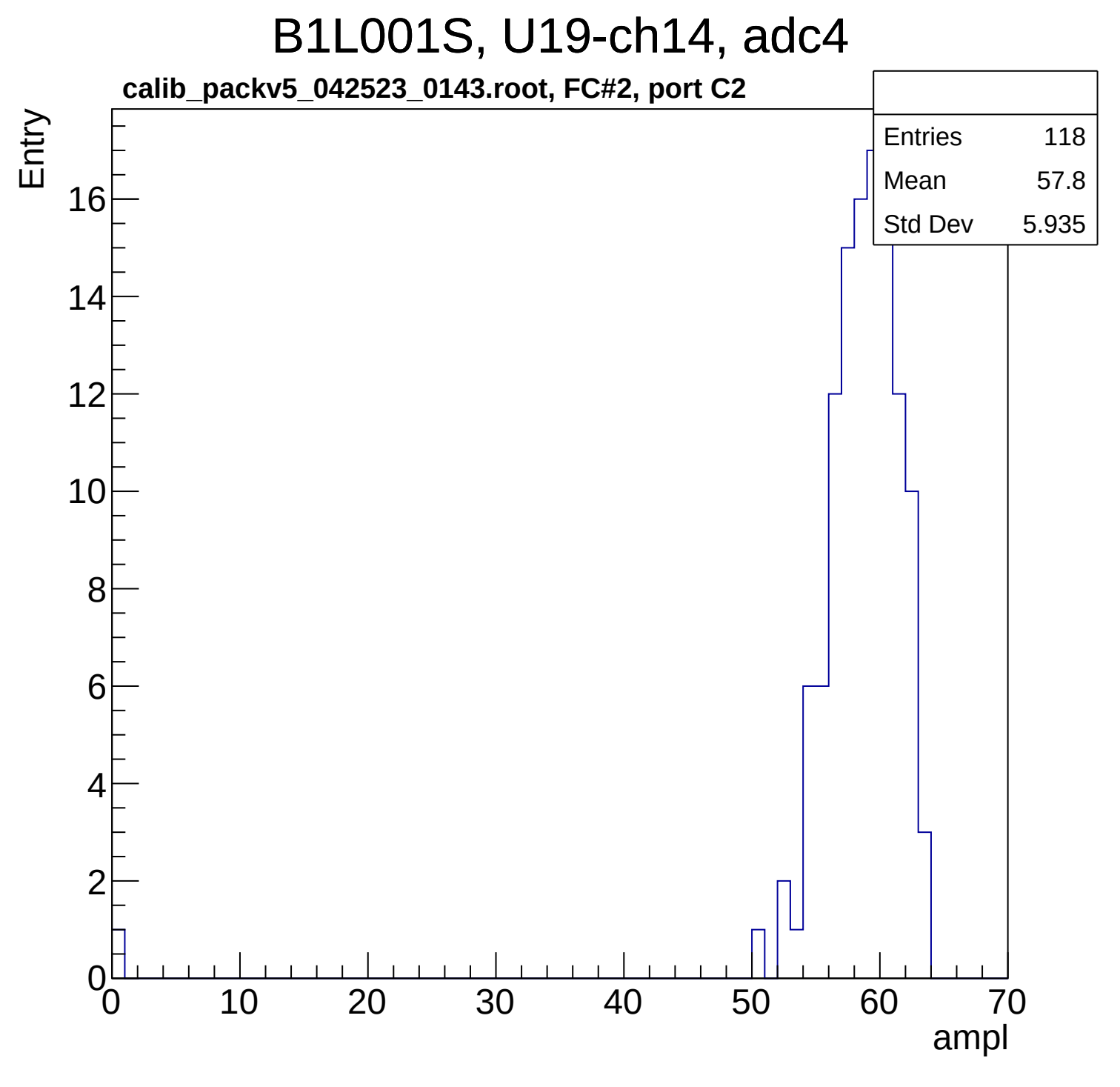
B1L001S, U19-ch14, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 118
Mean 57.8
Std Dev 5.935
Entry
ampl
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2
4
6
8
10
12
14
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0
10
20
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40
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60
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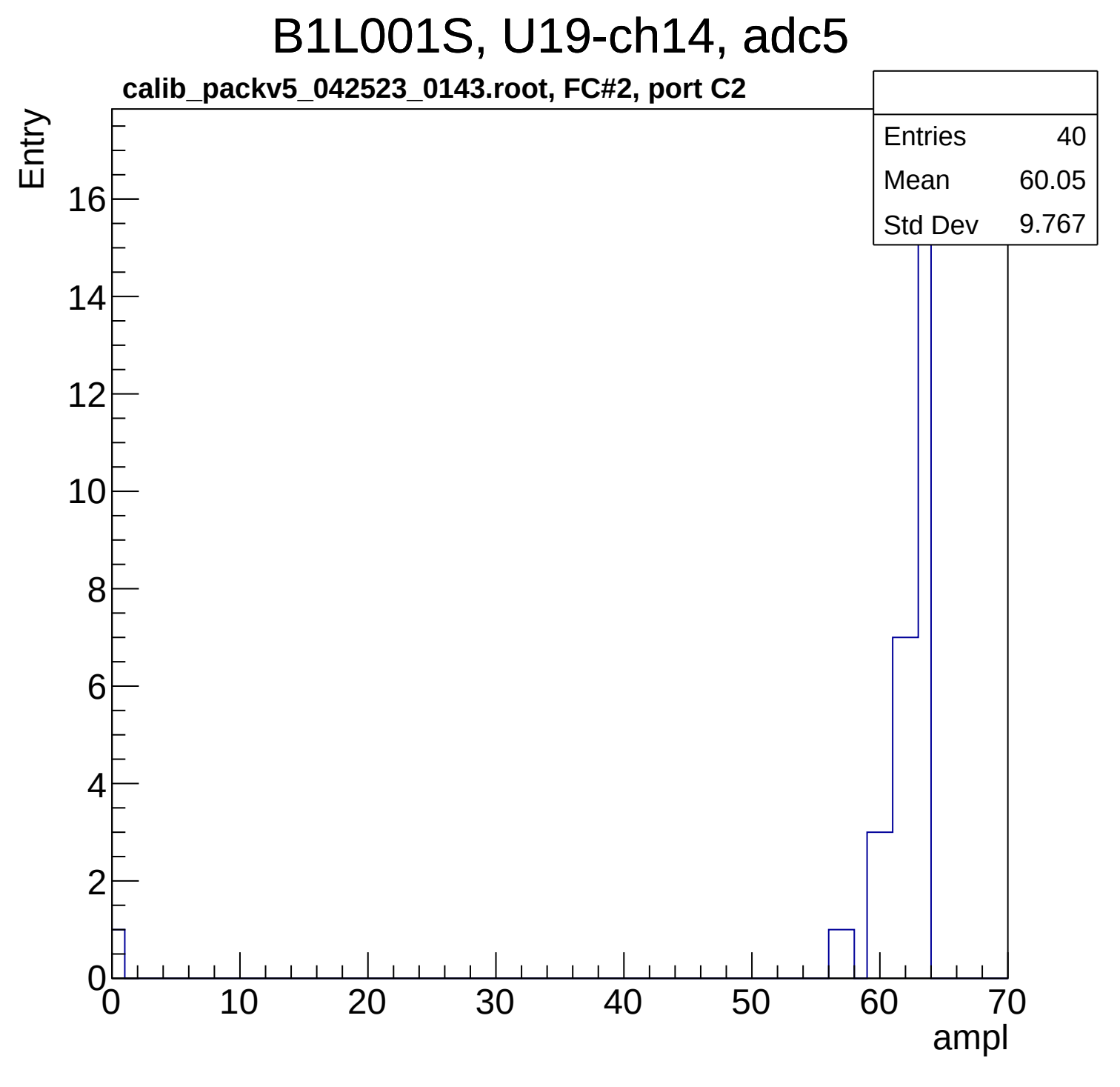
B1L001S, U19-ch14, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 40
Mean 60.05
Std Dev 9.767
Entry
ampl
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2
4
6
8
10
12
14
16
0
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20
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40
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60
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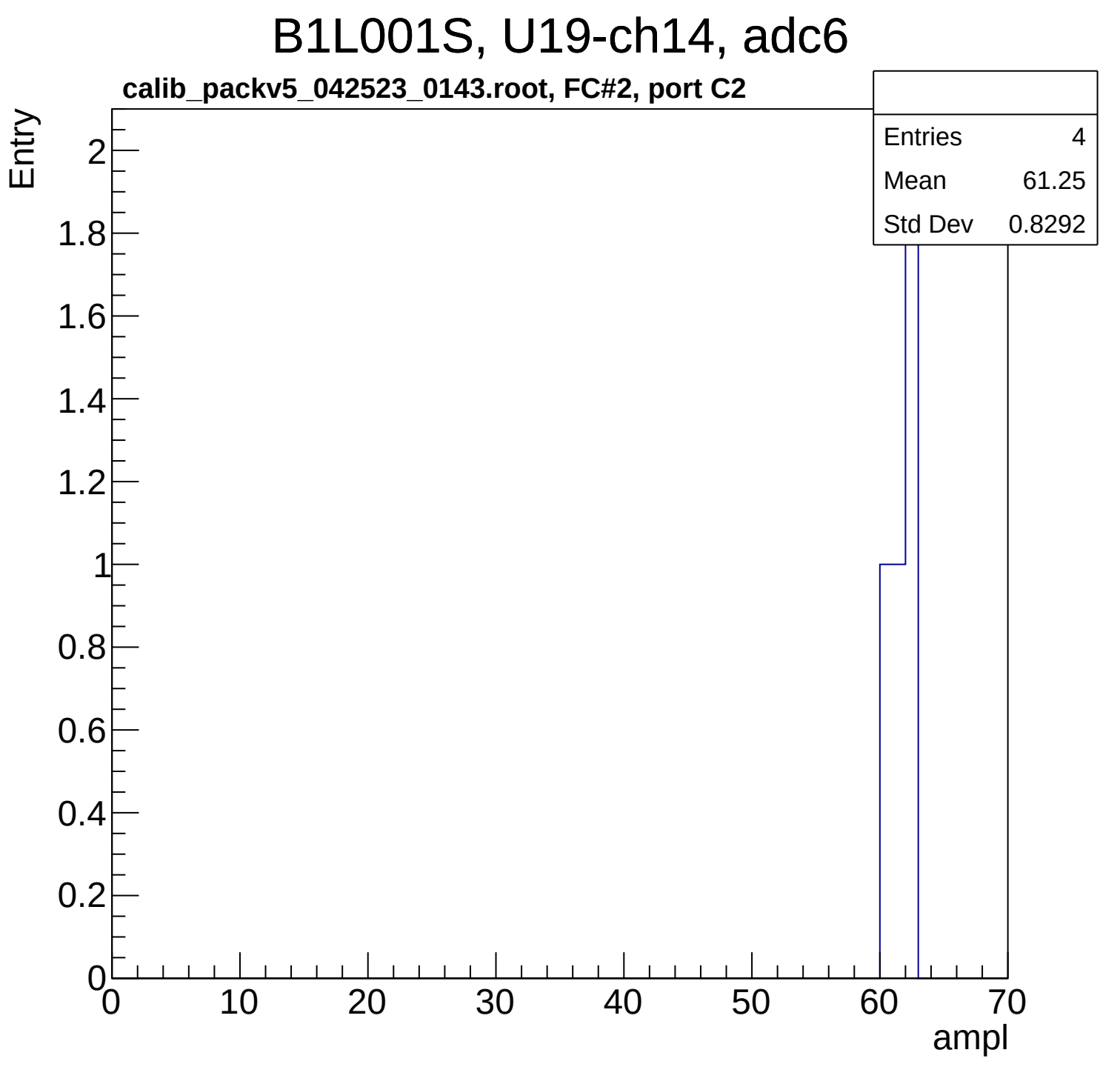
B1L001S, U19-ch14, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 4
Mean 61.25
Std Dev 0.8292
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
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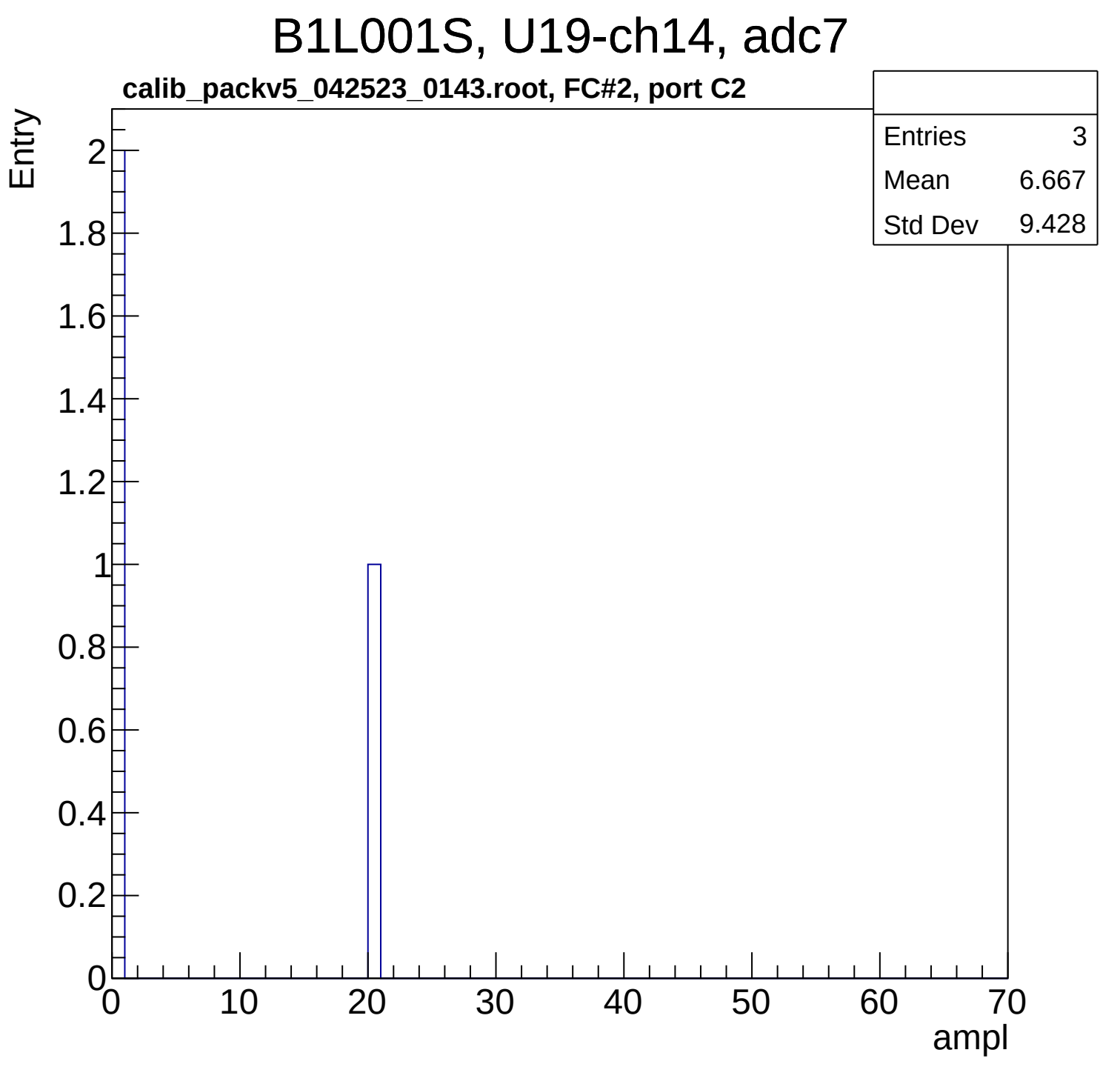
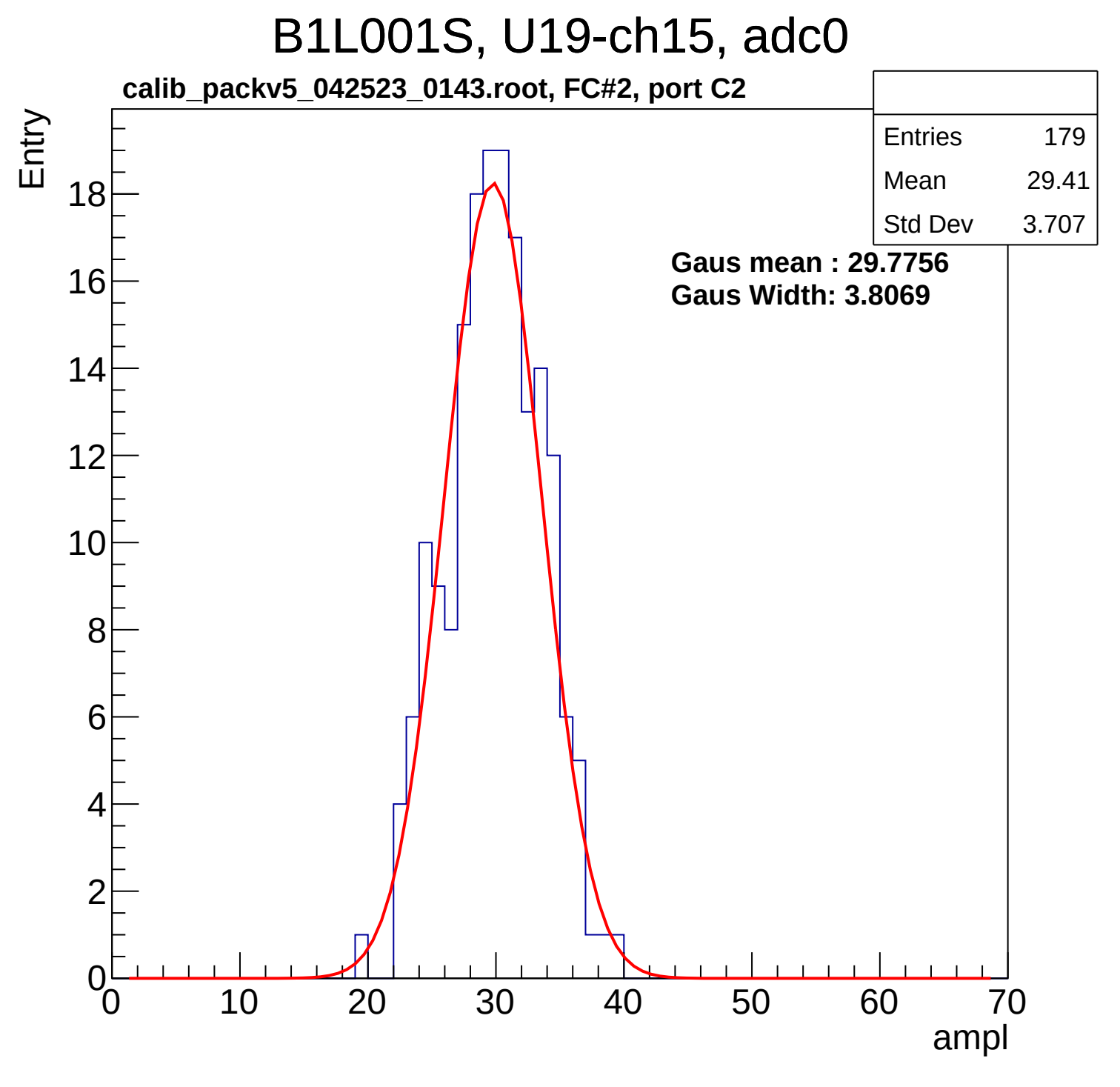
40
50
60
70


B1L001S, U19-ch14, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 3
Mean 6.667
Std Dev 9.428
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L001S, U19-ch15, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 179
Mean 29.41
Std Dev 3.707
Gaus mean : 29.7756
Gaus Width: 3.8069
Entry
ampl
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4
6
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10
12
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0
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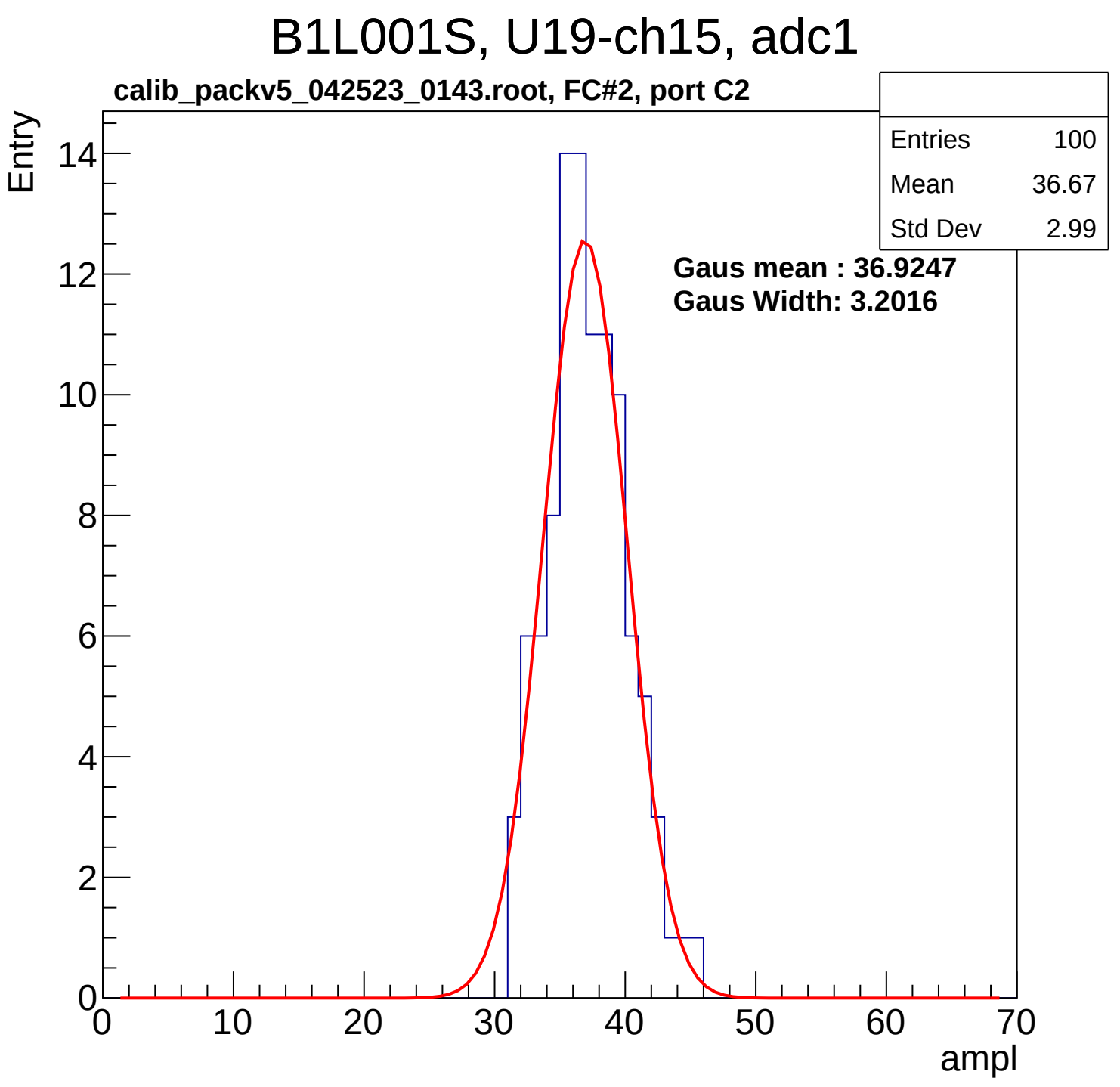
B1L001S, U19-ch15, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 100
Mean 36.67
Std Dev 2.99
Gaus mean : 36.9247
Gaus Width: 3.2016
Entry
ampl
0
2
4
6
8
10
12
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0
10
20
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40
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60
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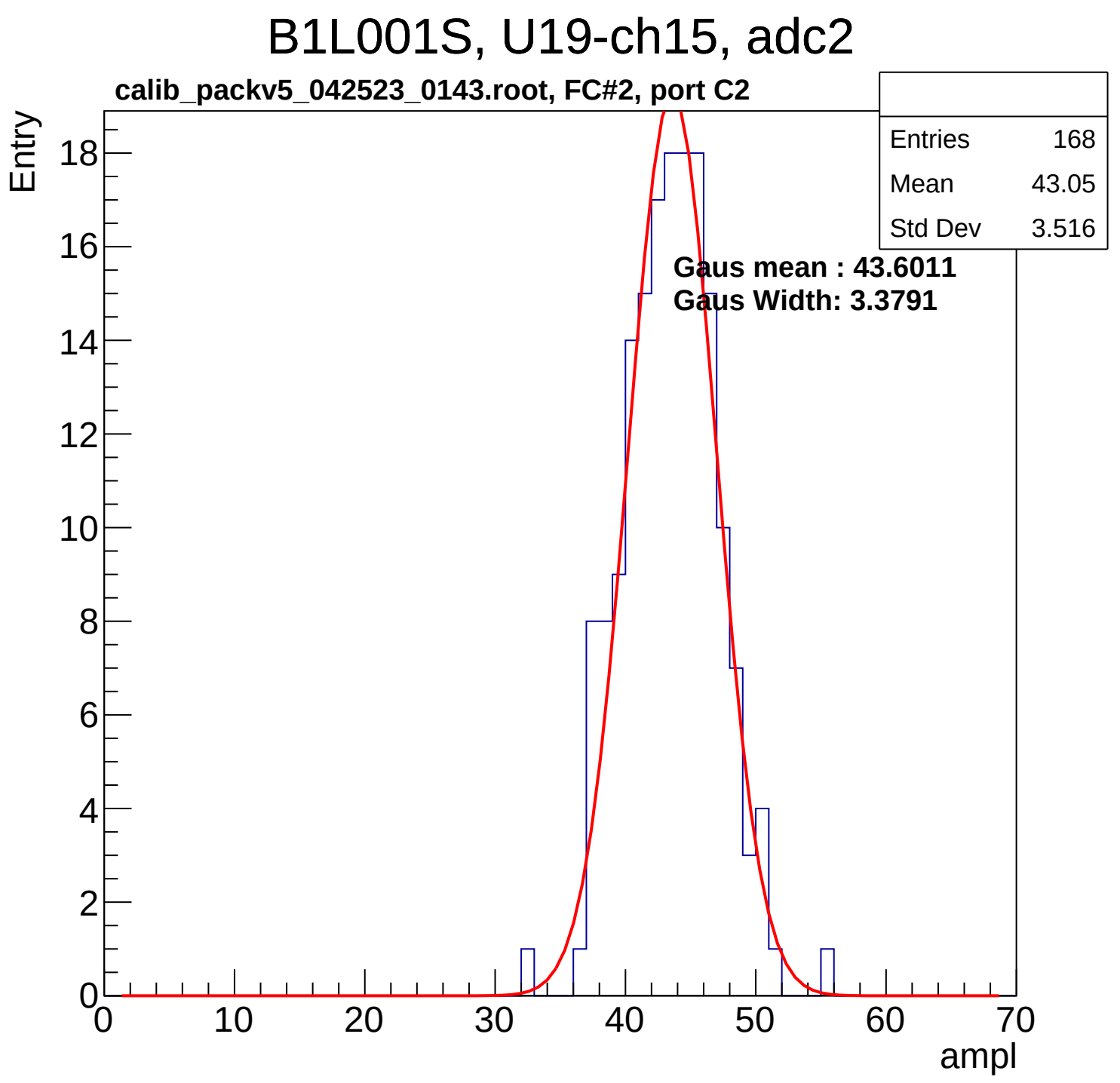
B1L001S, U19-ch15, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 168
Mean 43.05
Std Dev 3.516
Gaus mean : 43.6011
Gaus Width: 3.3791
Entry
ampl
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4
6
8
10
12
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16
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0
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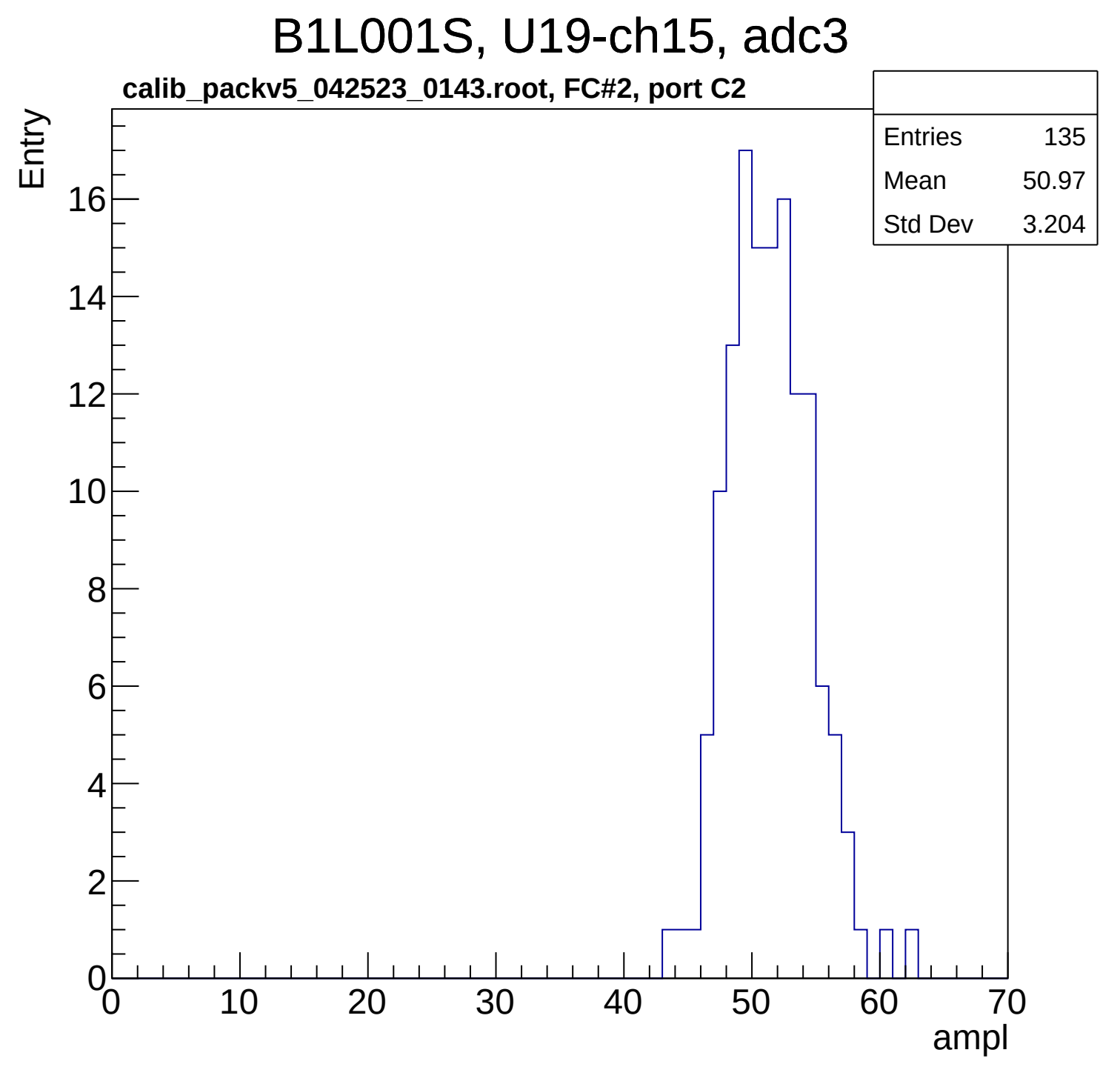
B1L001S, U19-ch15, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 135
Mean 50.97
Std Dev 3.204
Entry
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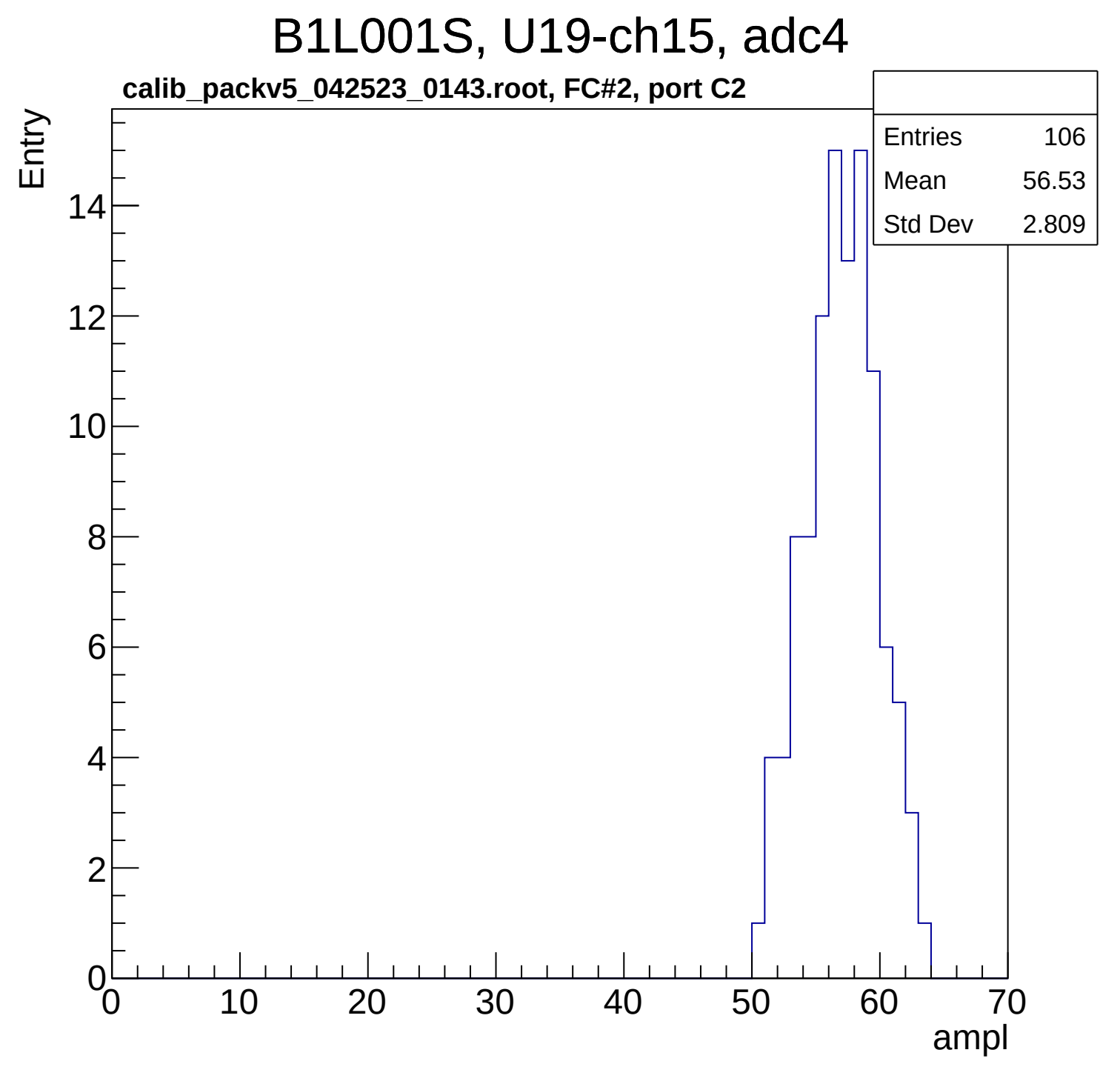
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch15, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 106
Mean 56.53
Std Dev 2.809
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
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60
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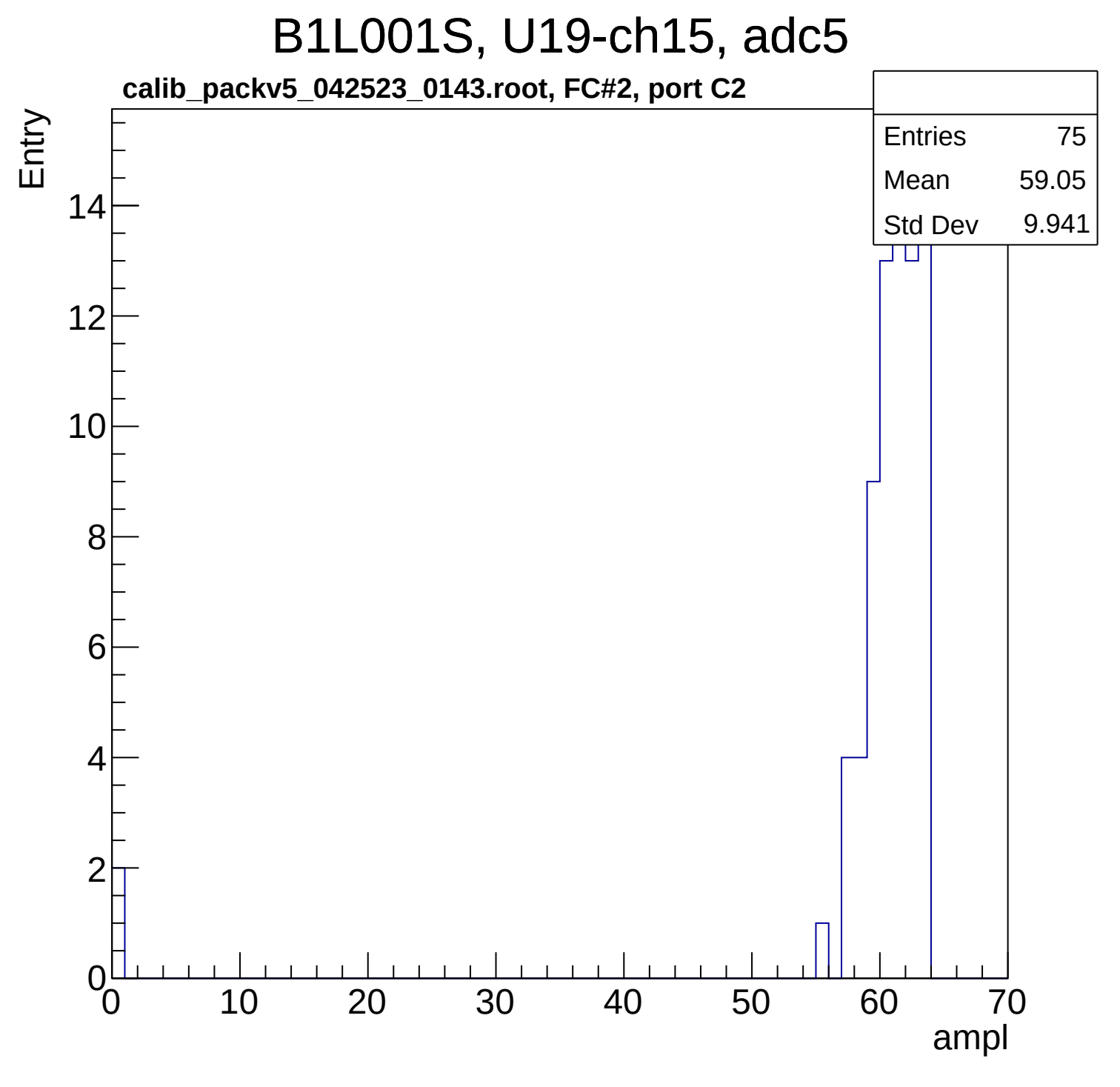
B1L001S, U19-ch15, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 75
Mean 59.05
Std Dev 9.941
Entry
ampl
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12
14
0
10
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60
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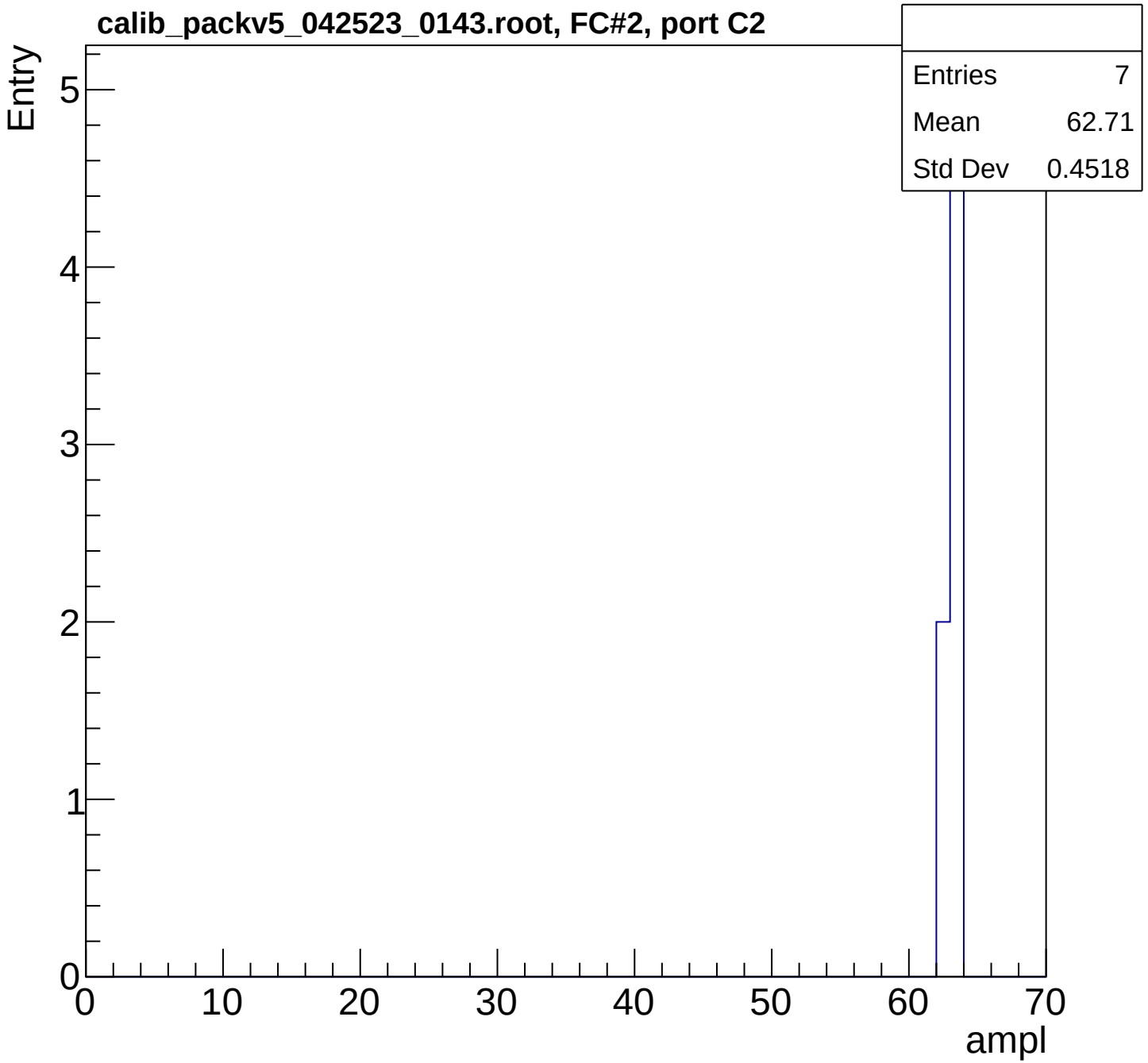
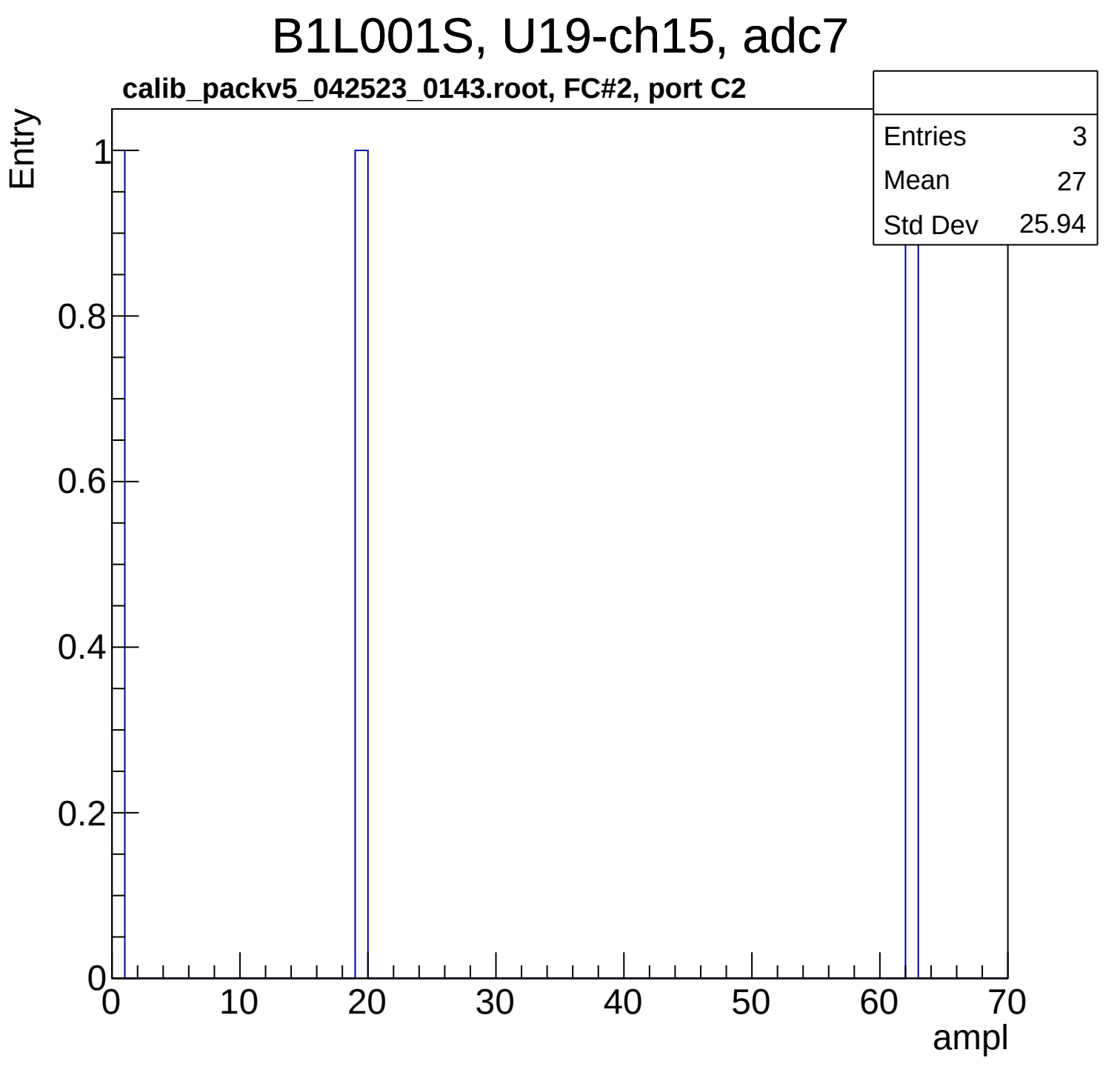

B1L001S, U19-ch15, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 7
Mean 62.71
Std Dev 0.4518
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch15, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 3
Mean 27
Std Dev 25.94
Entry
ampl
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0.4
0.6
0.8
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0
10
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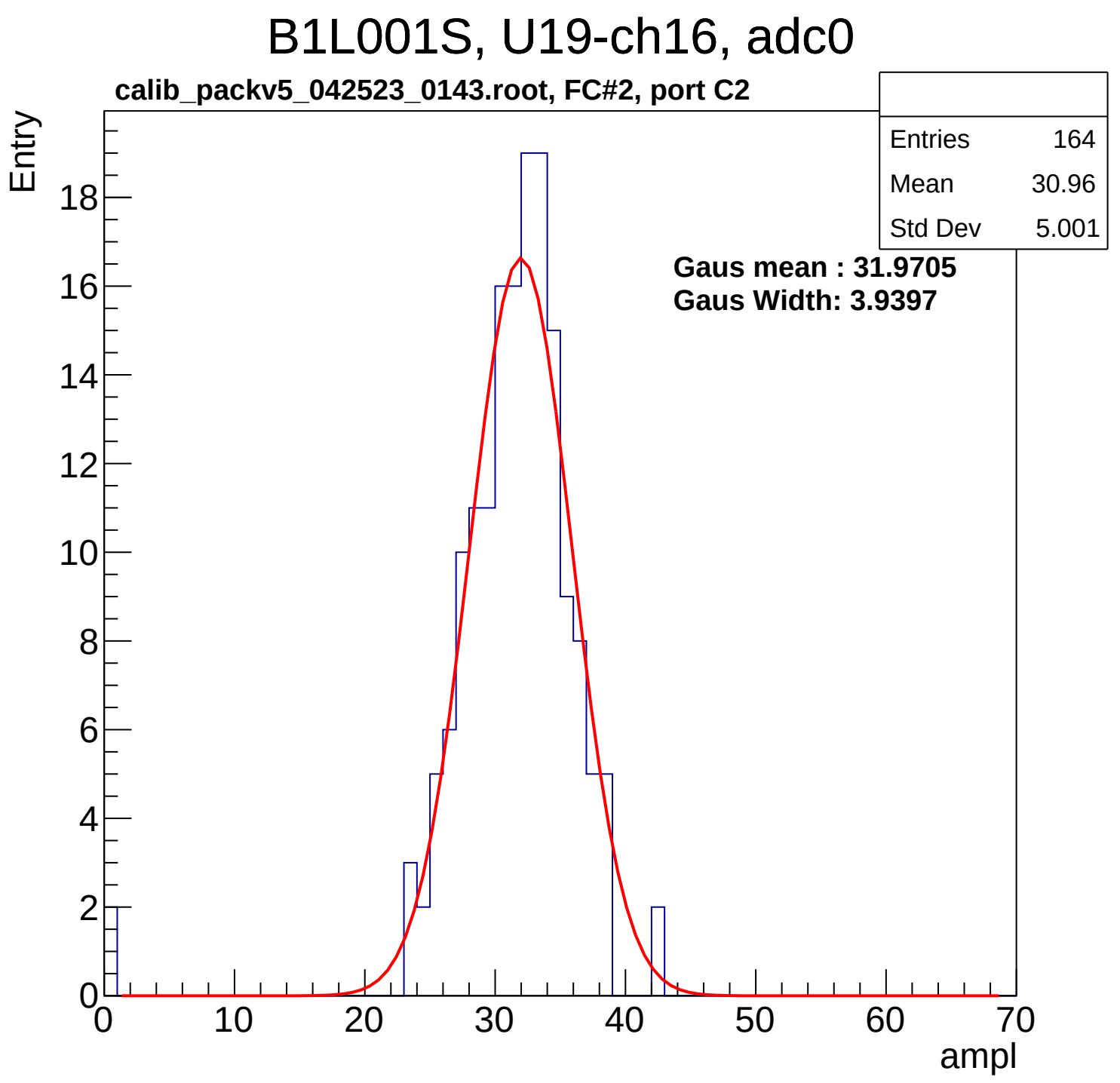
30
40
50
60
70


B1L001S, U19-ch16, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 164
Mean 30.96
Std Dev 5.001
Gaus mean : 31.9705
Gaus Width: 3.9397
Entry
ampl
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2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
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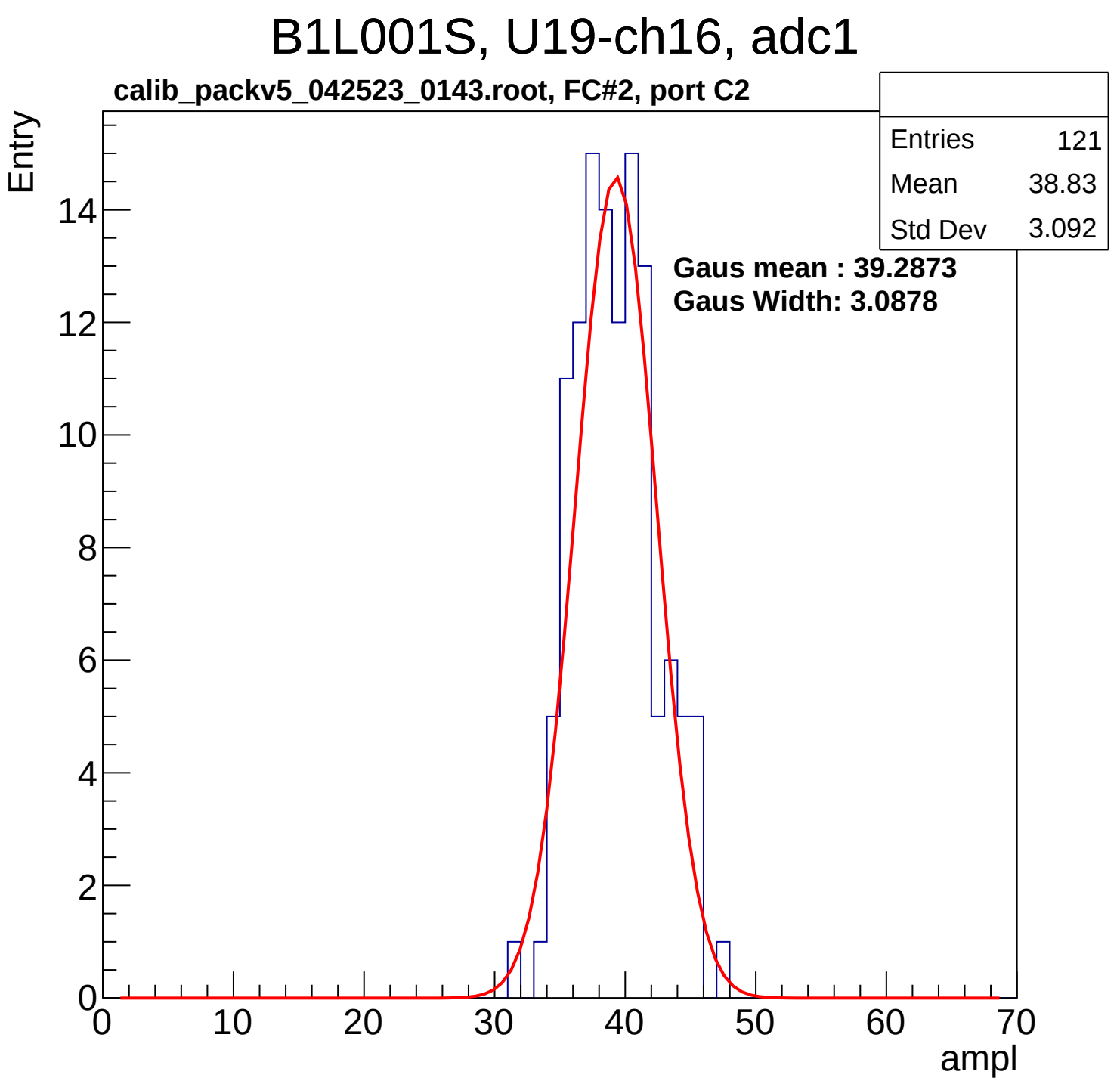
B1L001S, U19-ch16, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 121
Mean 38.83
Std Dev 3.092
Gaus mean : 39.2873
Gaus Width: 3.0878
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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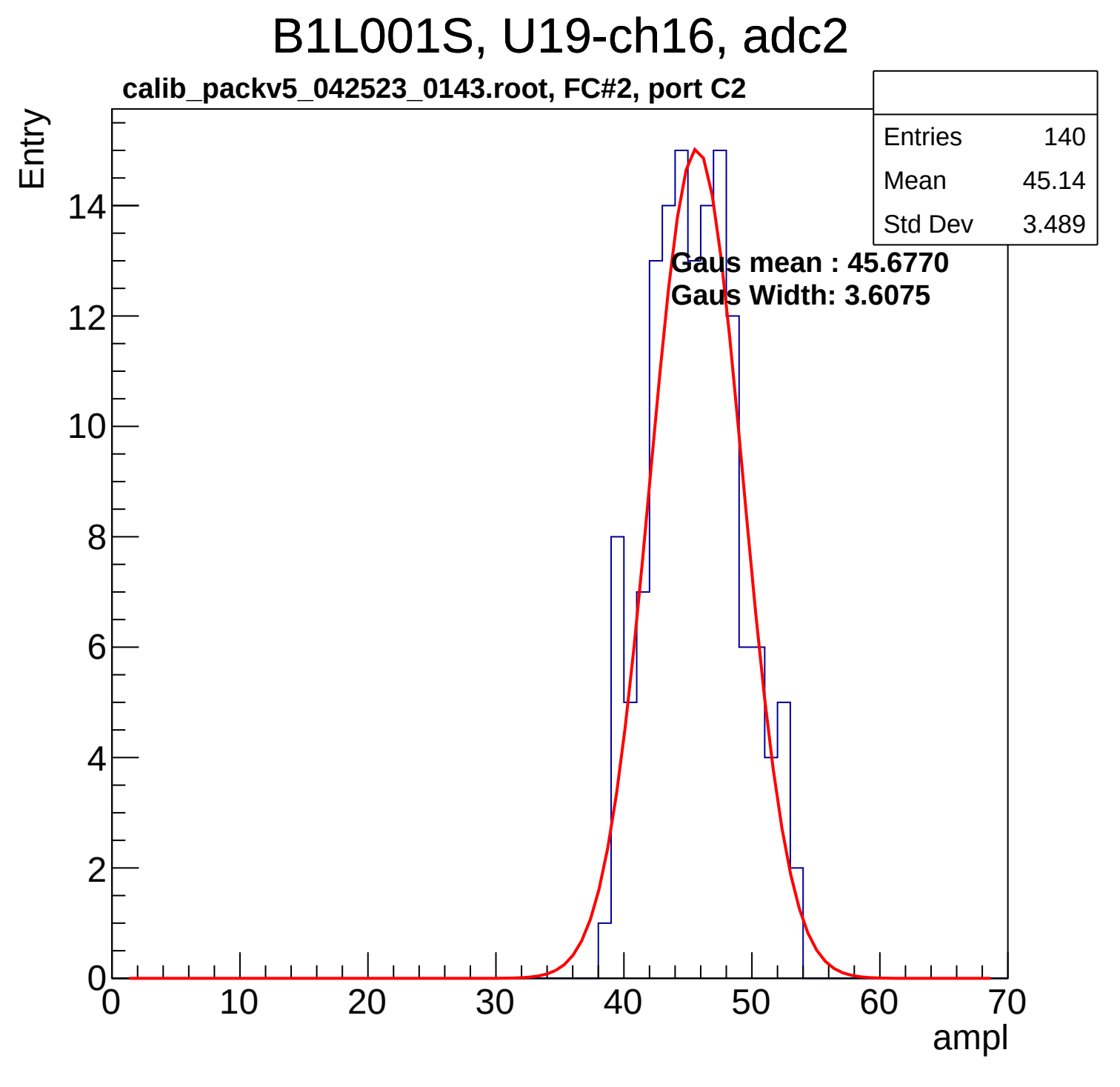
B1L001S, U19-ch16, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 140
Mean 45.14
Std Dev 3.489
Gaus mean : 45.6770
Gaus Width: 3.6075
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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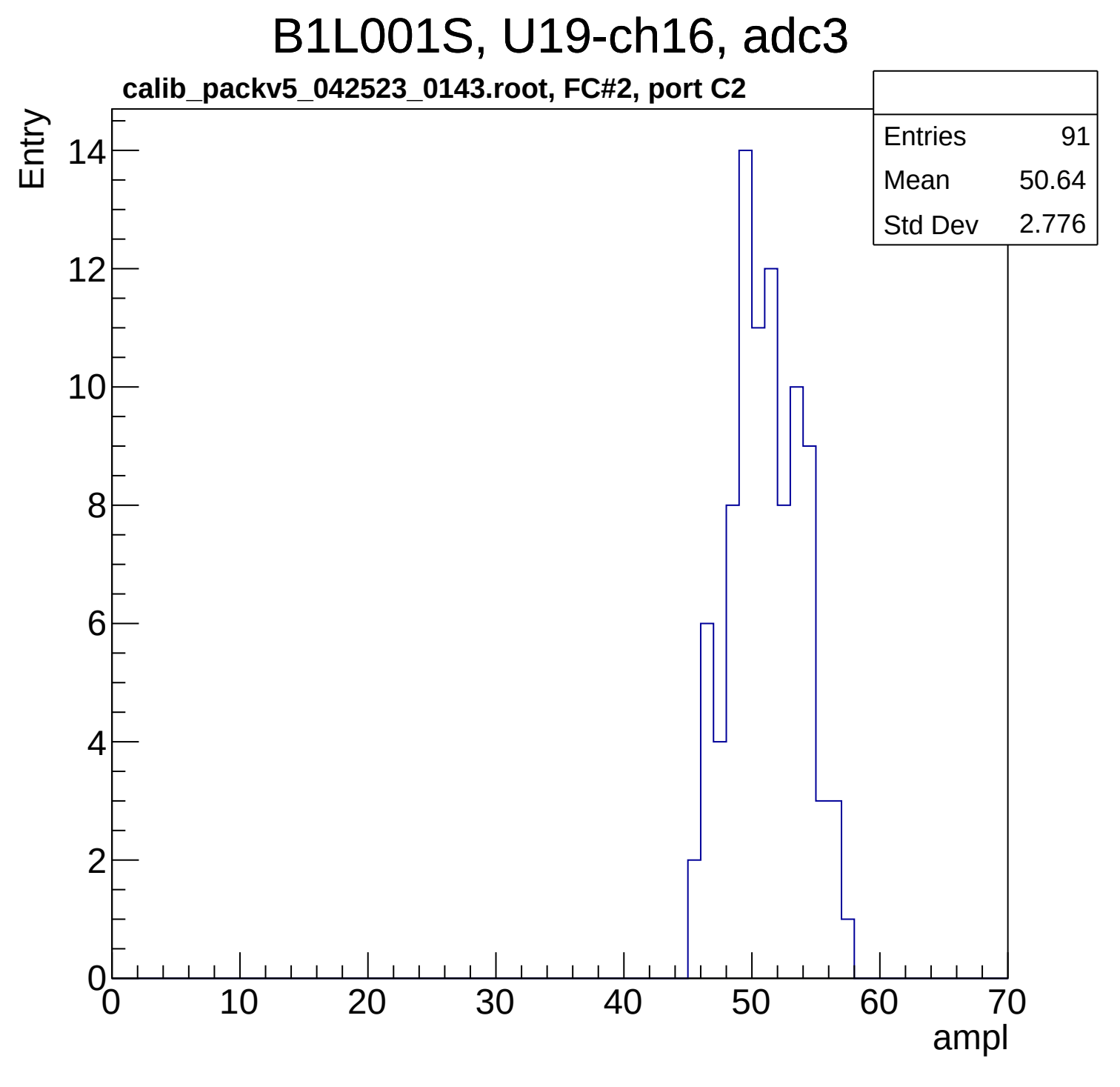
B1L001S, U19-ch16, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 91
Mean 50.64
Std Dev 2.776
Entry
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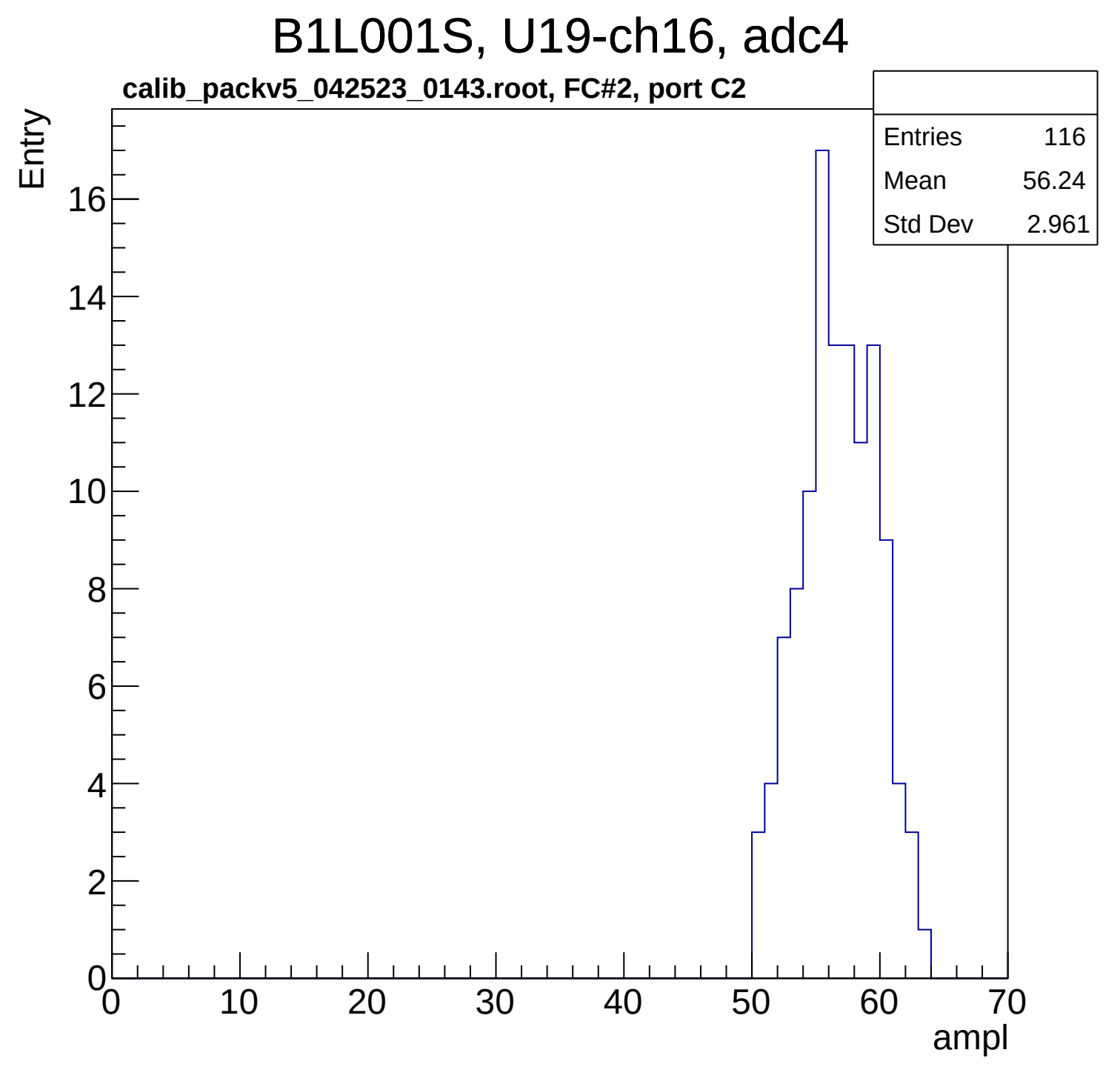
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch16, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 116
Mean 56.24
Std Dev 2.961
Entry
ampl
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4
6
8
10
12
14
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10
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60
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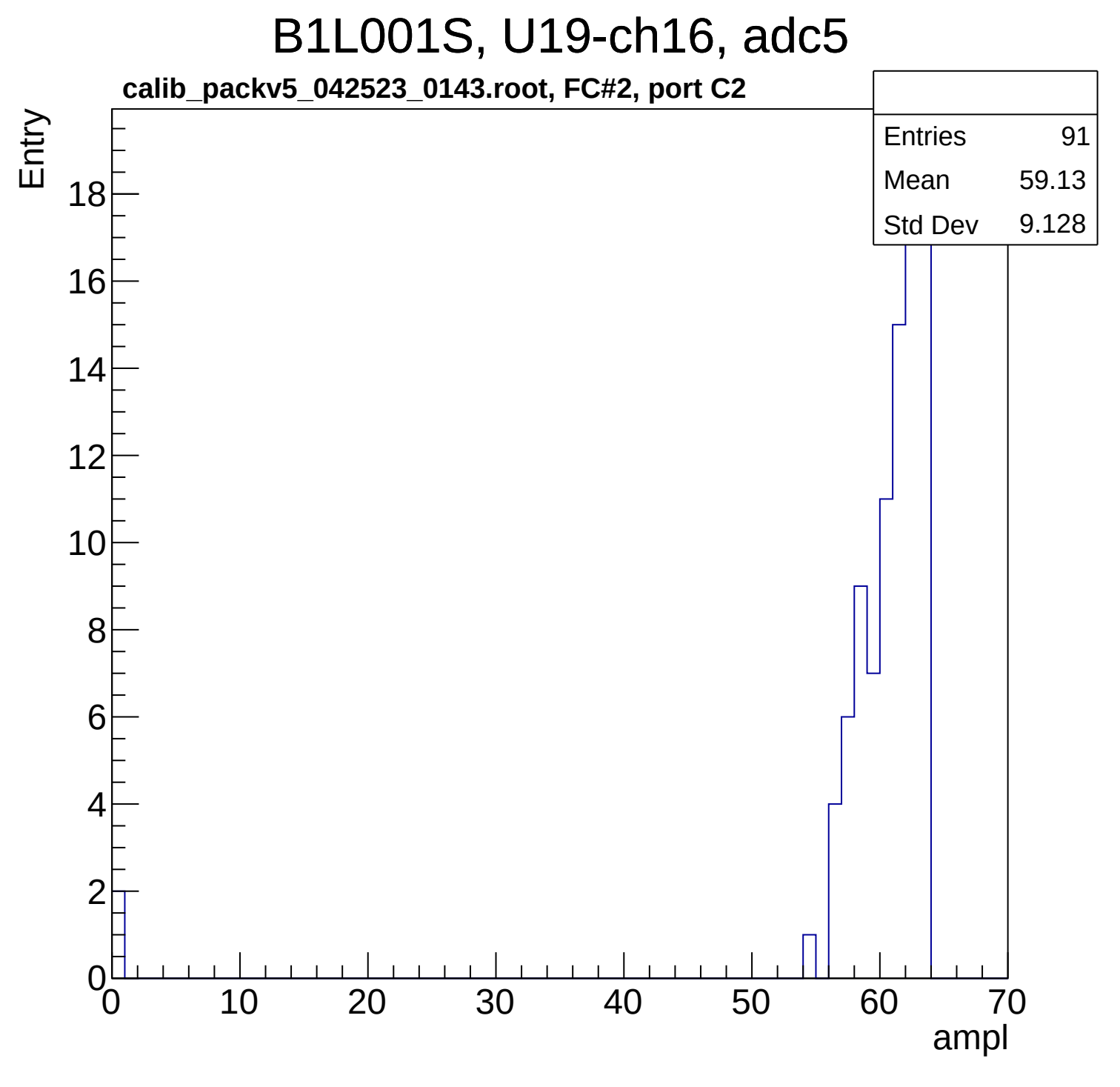
B1L001S, U19-ch16, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 91
Mean 59.13
Std Dev 9.128
Entry
ampl
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4
6
8
10
12
14
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0
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60
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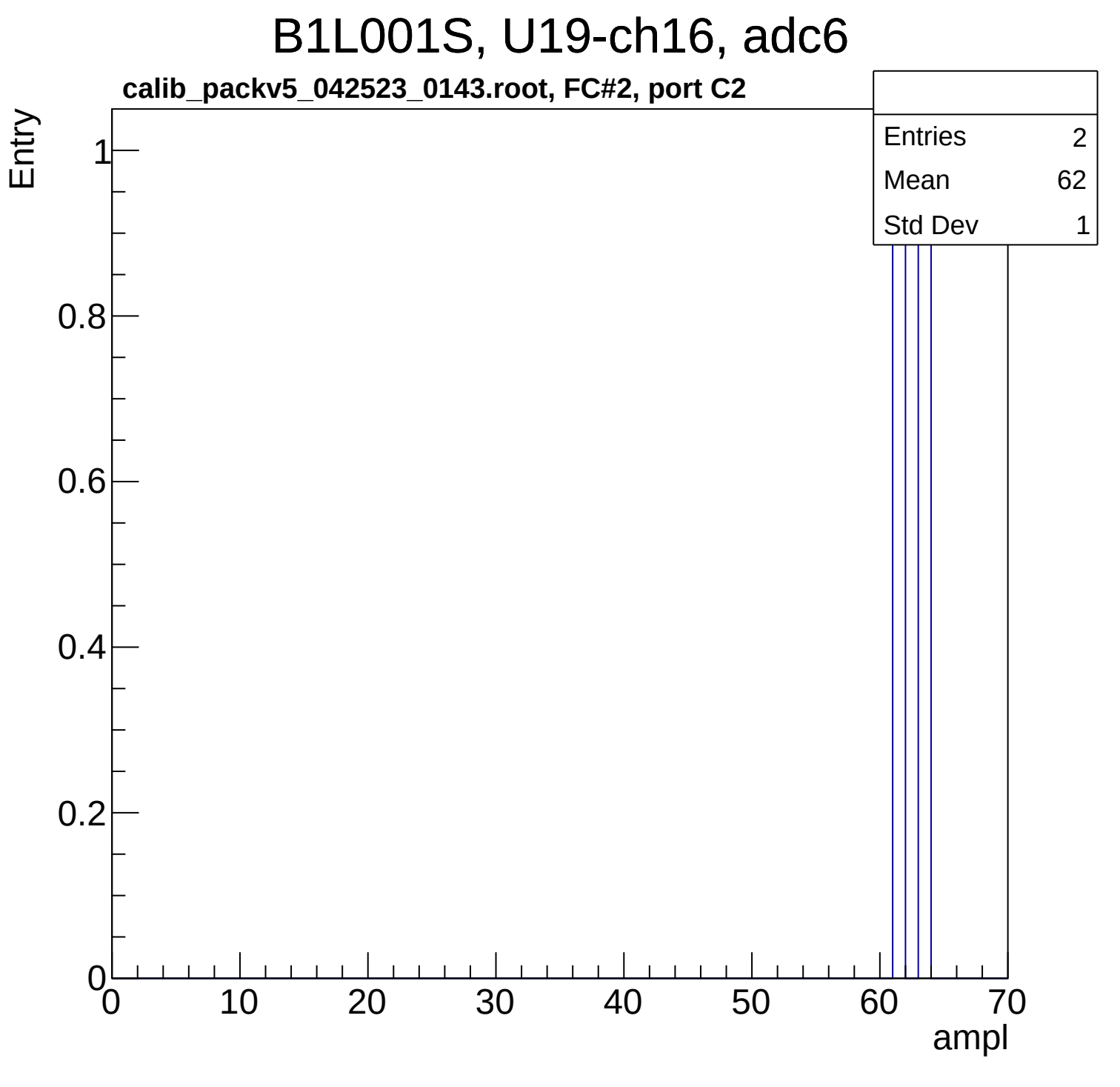
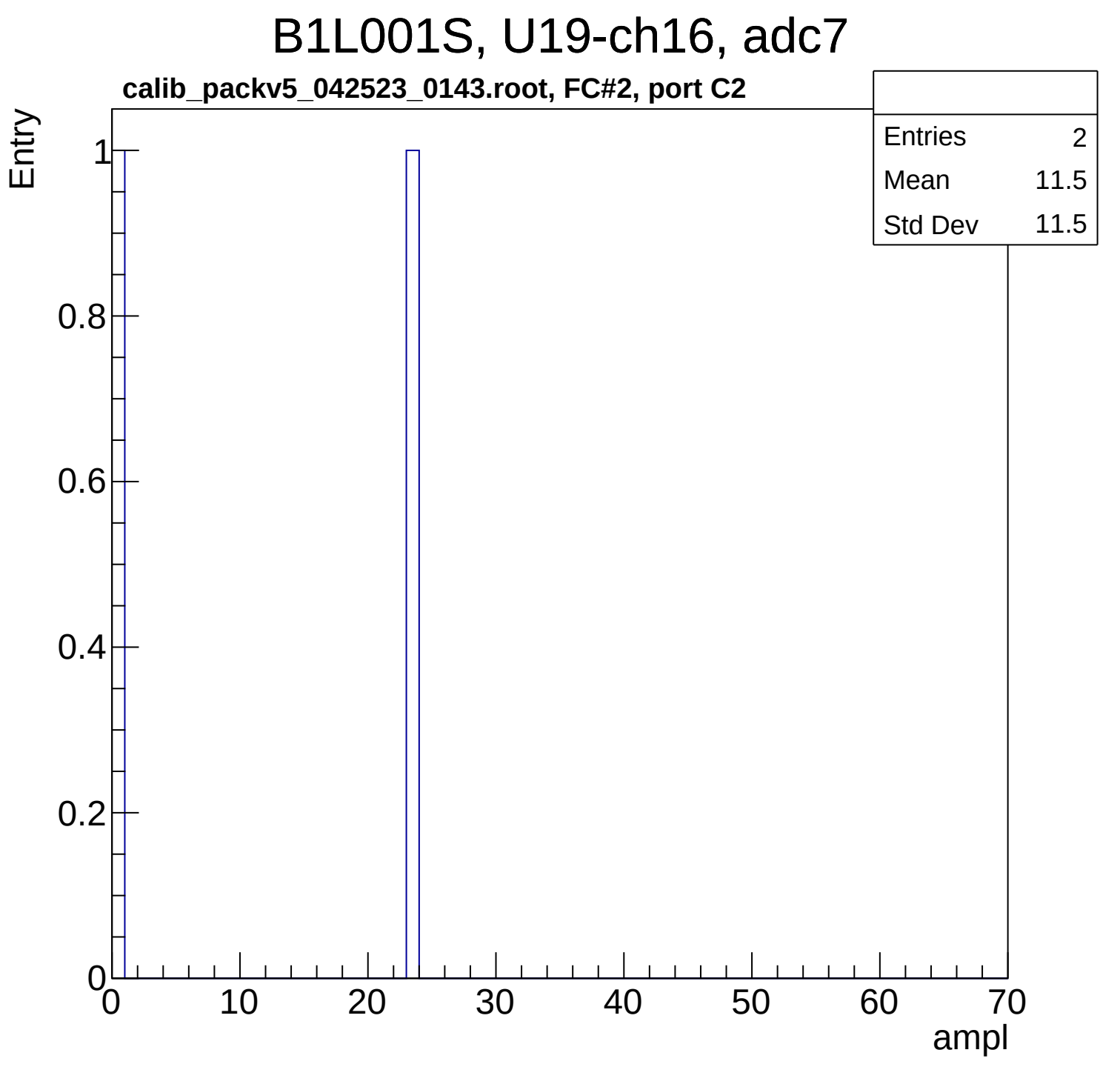

B1L001S, U19-ch16, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 62
Std Dev 1
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch16, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 11.5
Std Dev 11.5
Entry
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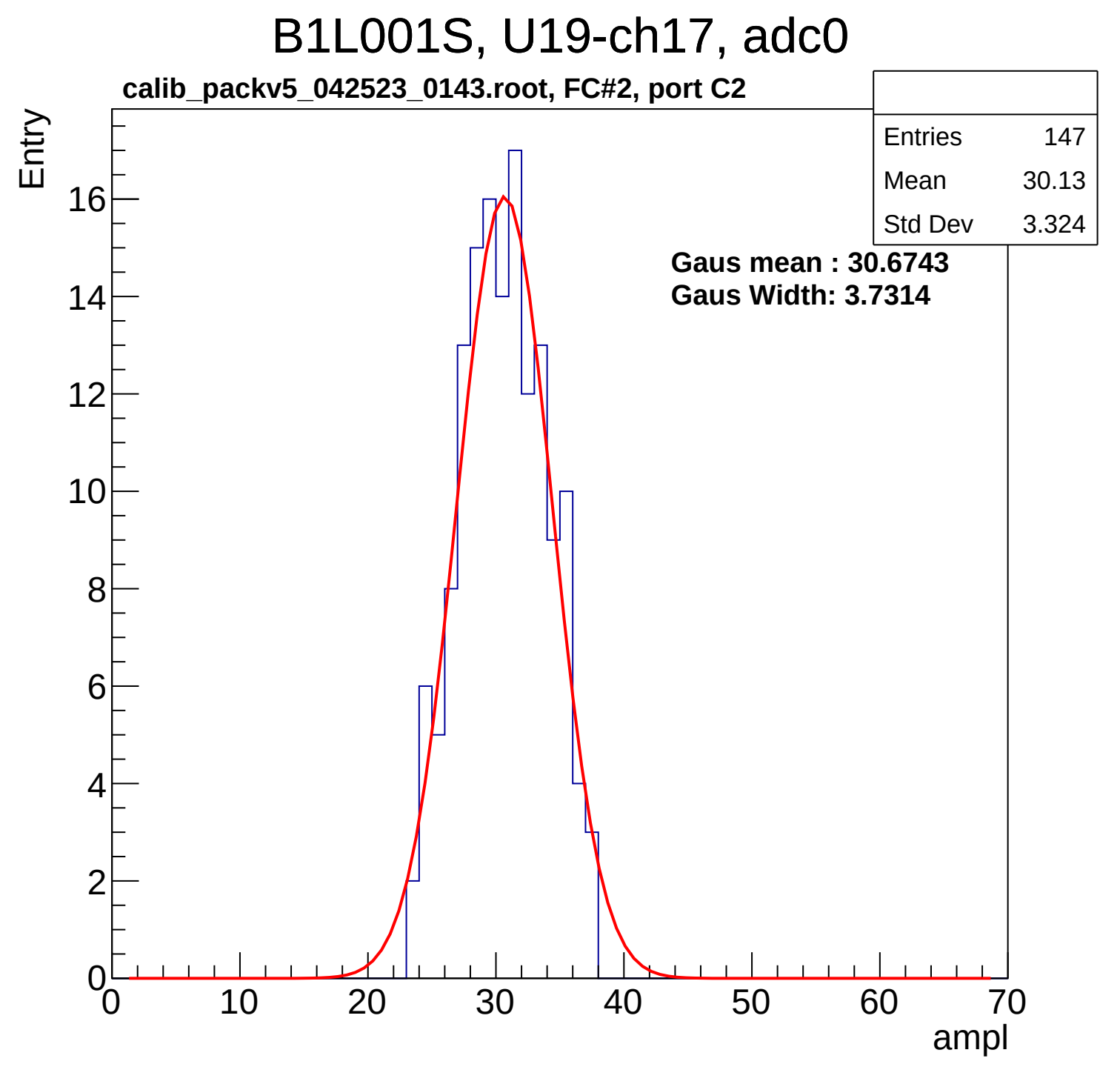
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch17, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 147
Mean 30.13
Std Dev 3.324
Gaus mean : 30.6743
Gaus Width: 3.7314
Entry
ampl
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2
4
6
8
10
12
14
16
0
10
20
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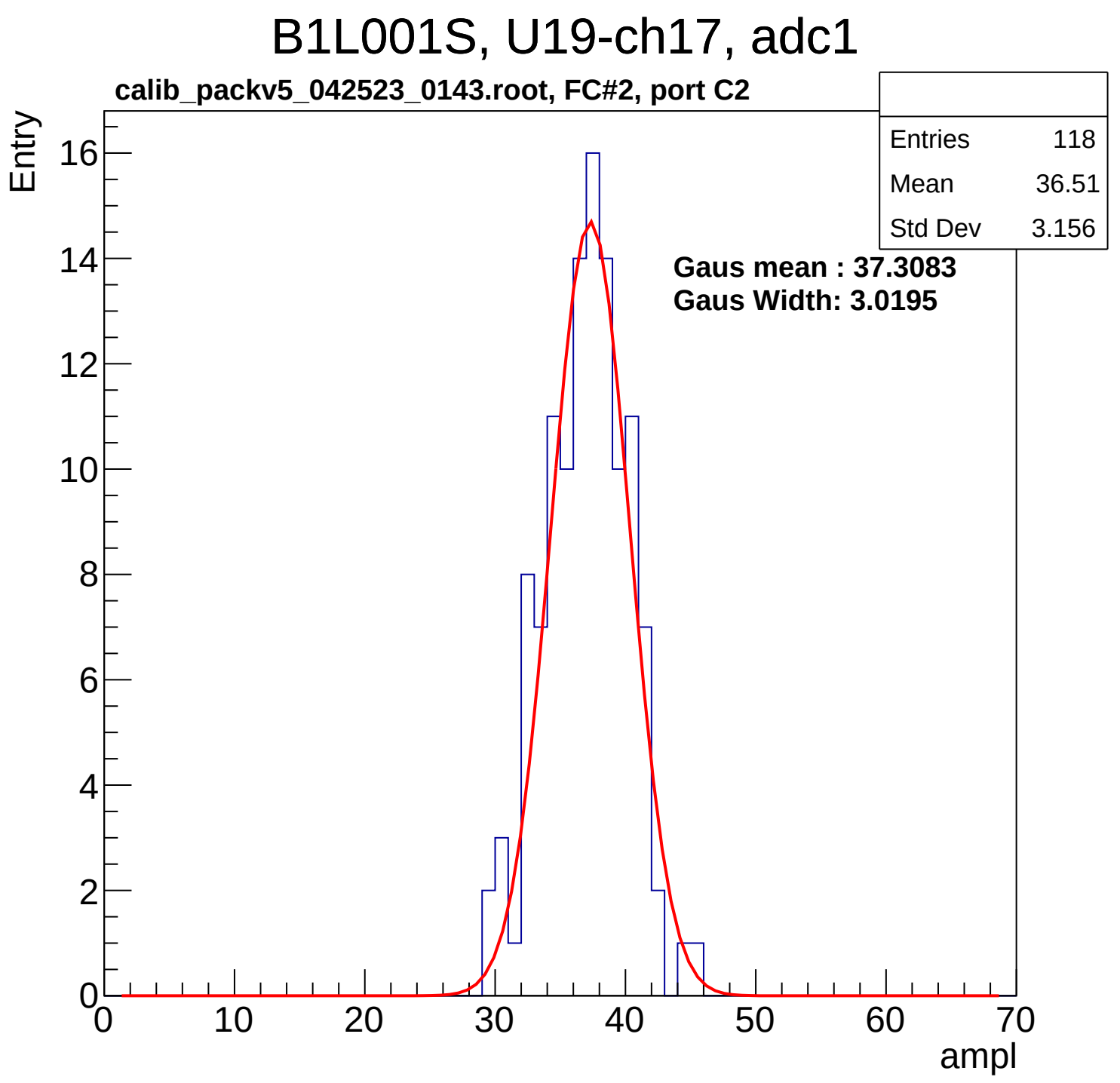
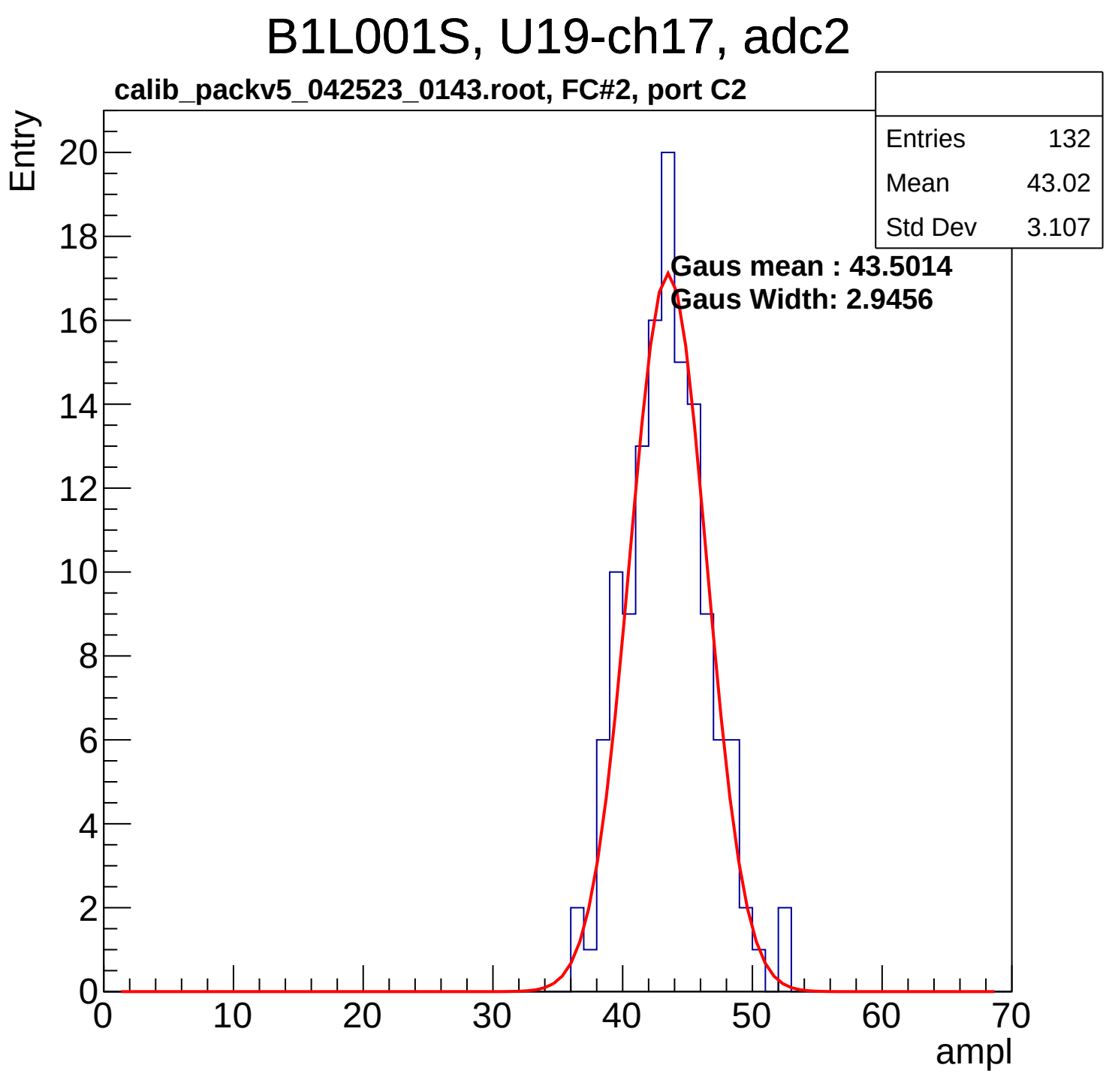
40
50
60
70


B1L001S, U19-ch17, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 118
Mean 36.51
Std Dev 3.156
Gaus mean : 37.3083
Gaus Width: 3.0195
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70


B1L001S, U19-ch17, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 132
Mean 43.02
Std Dev 3.107
Gaus mean : 43.5014
Gaus Width: 2.9456
Entry
ampl
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6
8
10
12
14
16
18
20
0
10
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60
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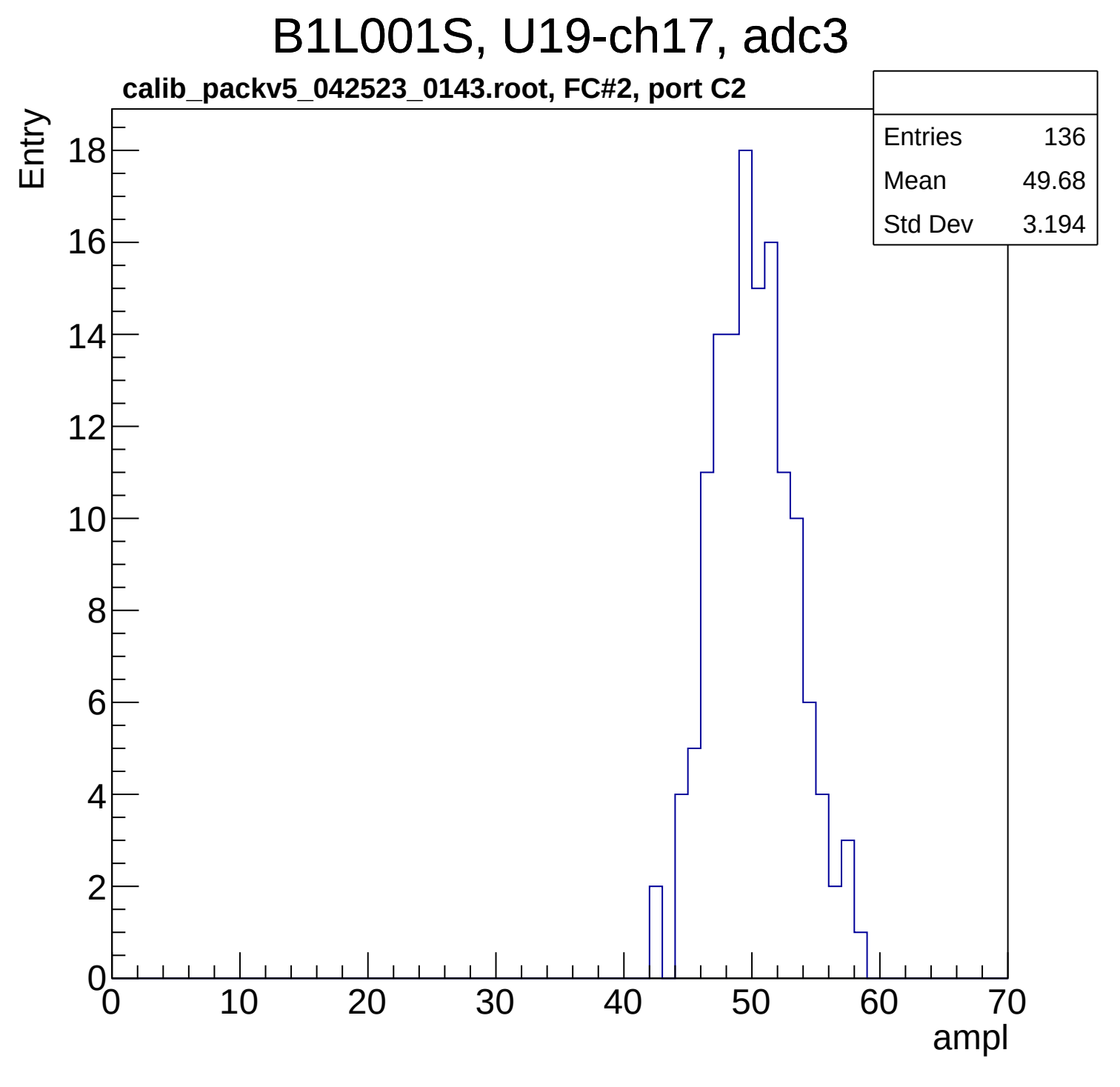
B1L001S, U19-ch17, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 136
Mean 49.68
Std Dev 3.194
Entry
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10
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14
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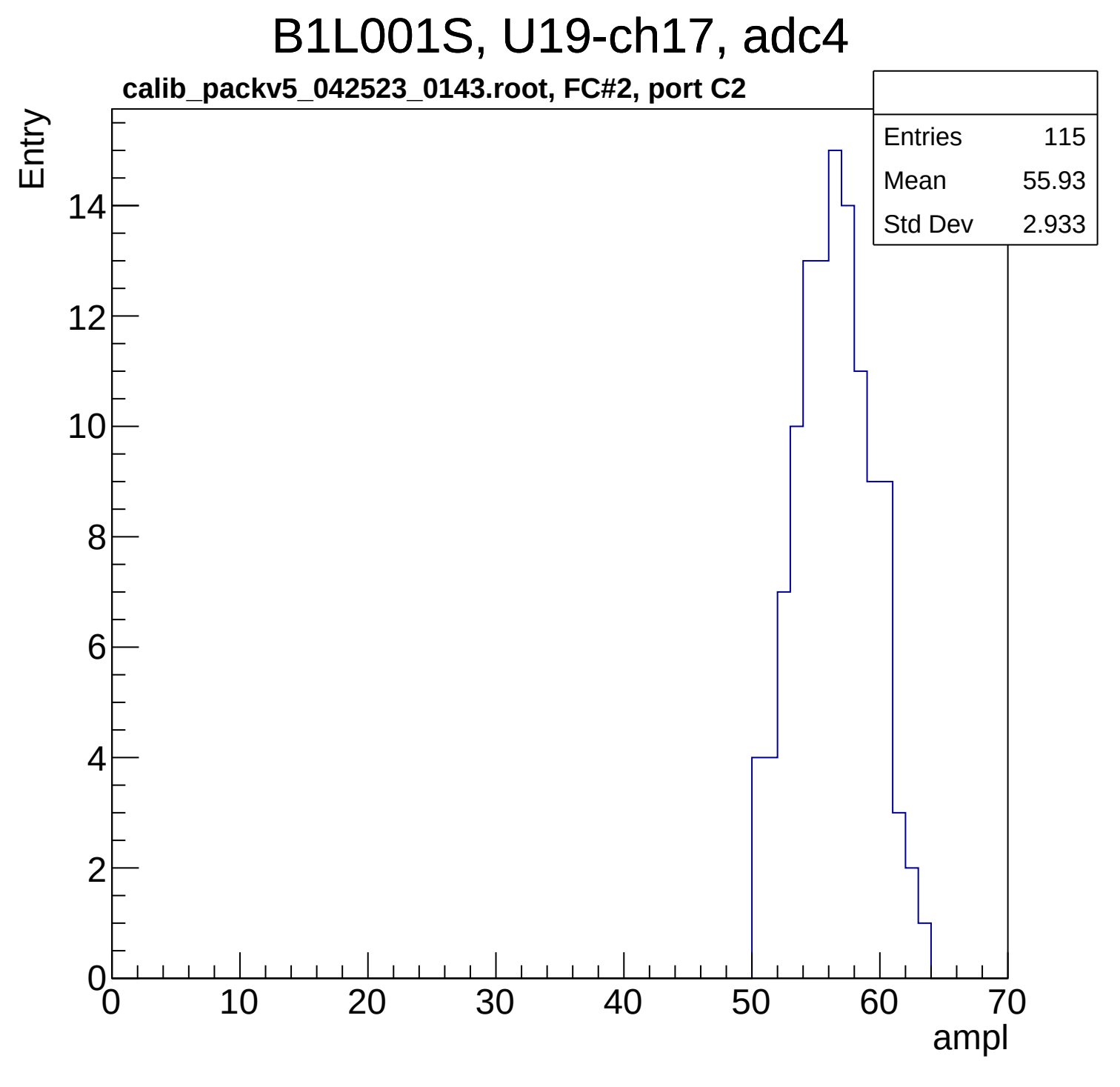
70
ampl


B1L001S, U19-ch17, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 115
Mean 55.93
Std Dev 2.933
Entry
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2
4
6
8
10
12
14
0
10
20
30
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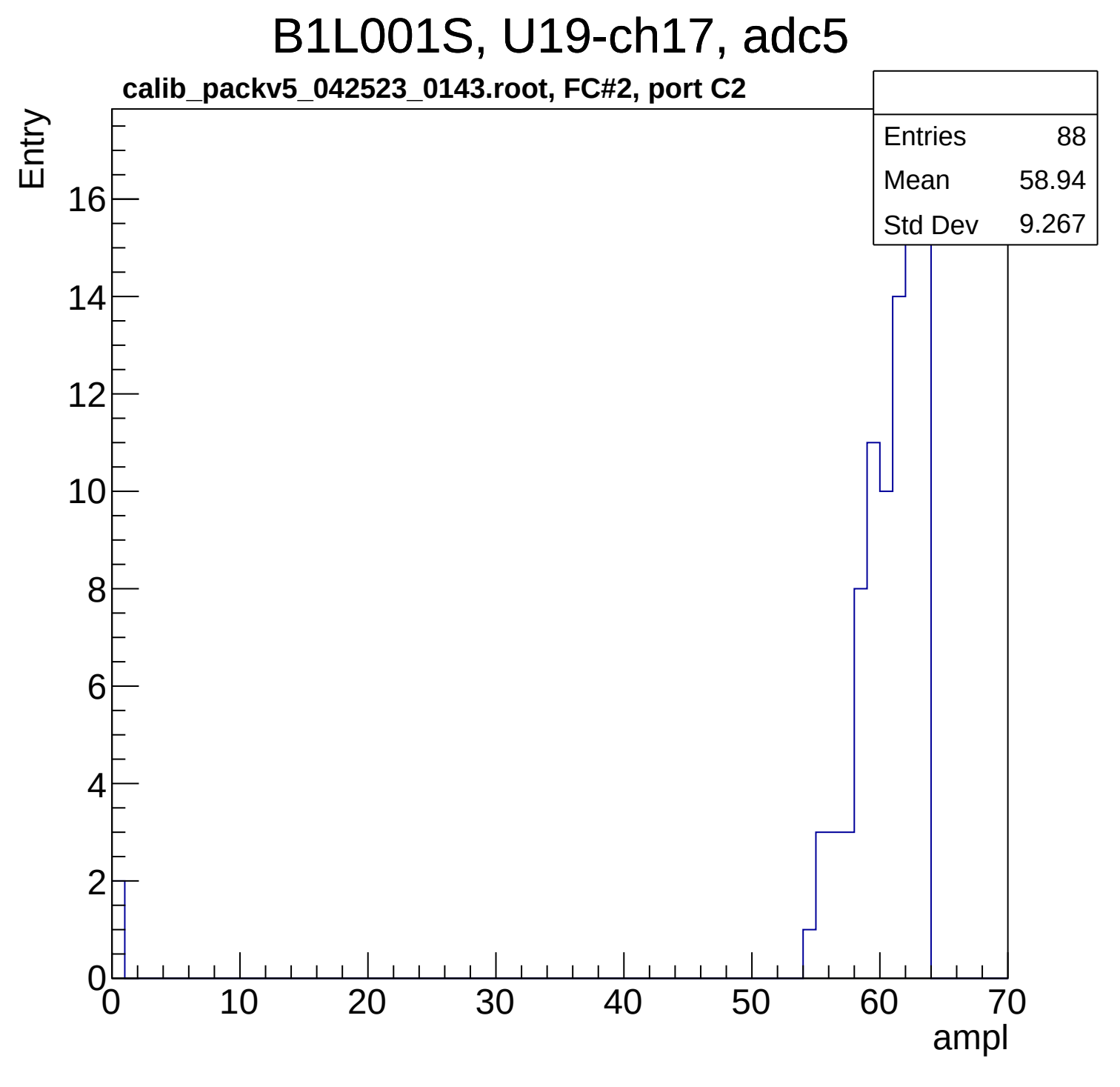
50
60
70
ampl


B1L001S, U19-ch17, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 88
Mean 58.94
Std Dev 9.267
Entry
ampl
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10
12
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60
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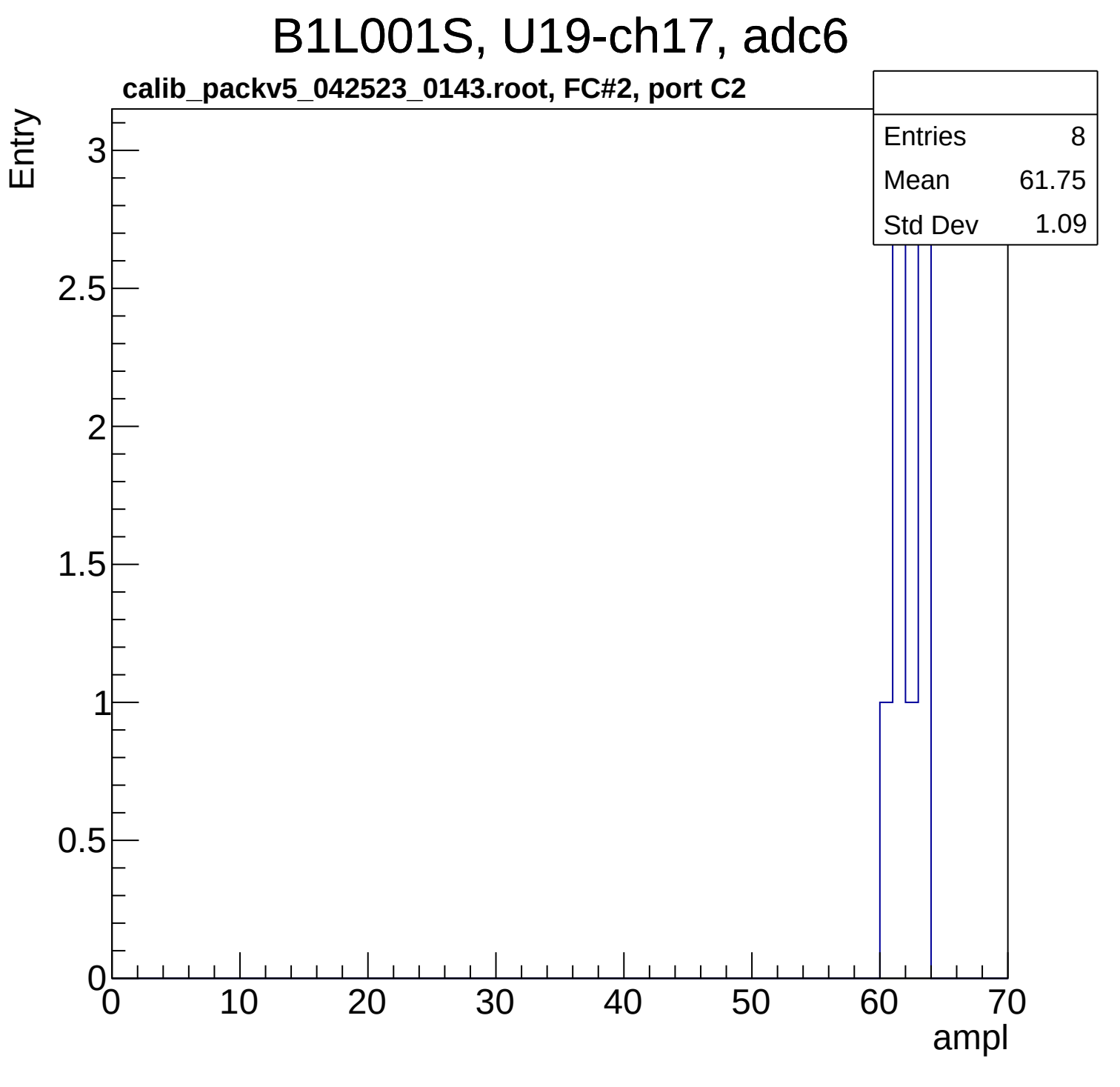
B1L001S, U19-ch17, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 8
Mean 61.75
Std Dev 1.09
Entry
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1
1.5
2
2.5
3
0
10
20
30
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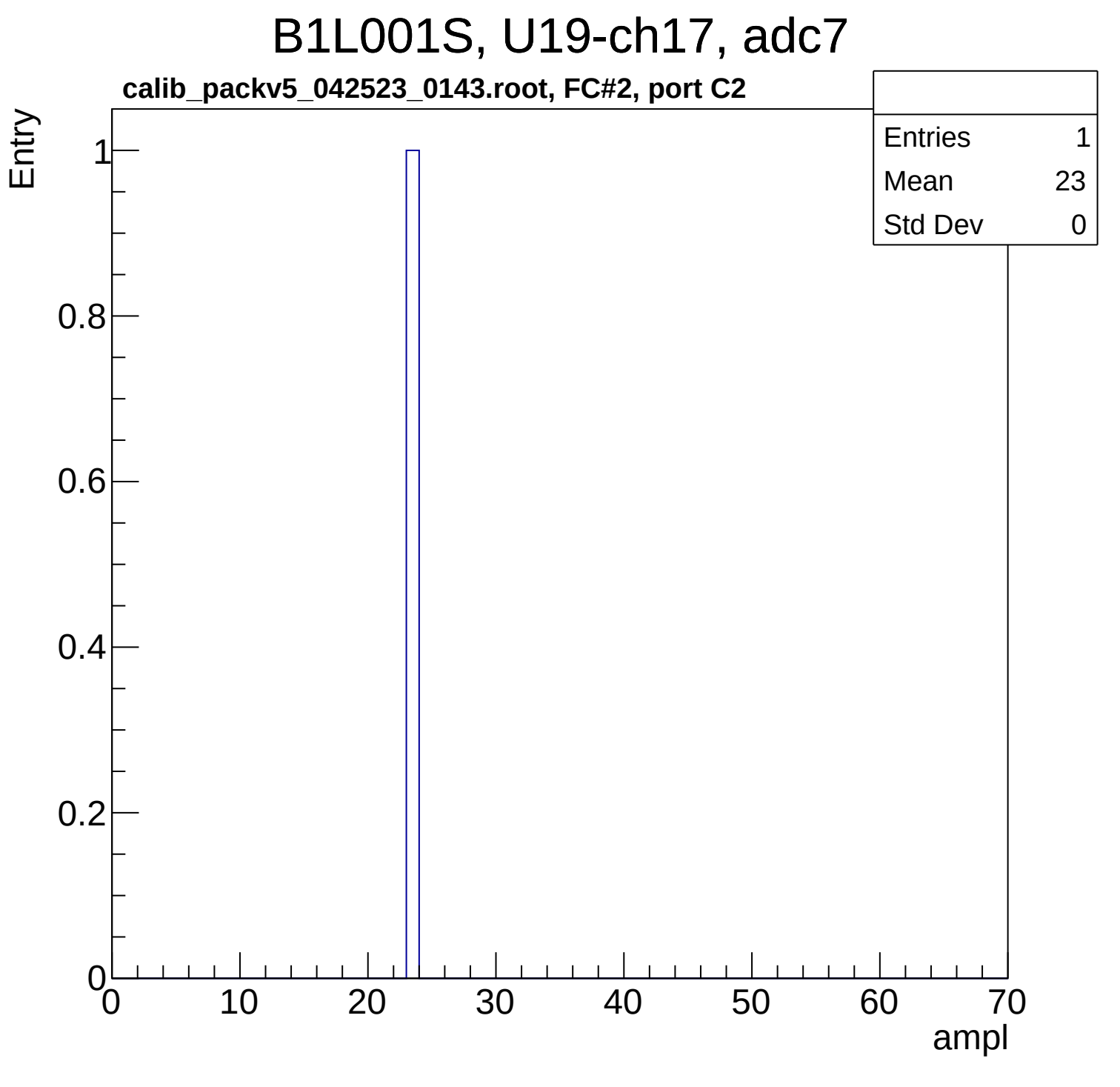
50
60
70
ampl


B1L001S, U19-ch17, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 23
Std Dev 0
Entry
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0.6
0.4
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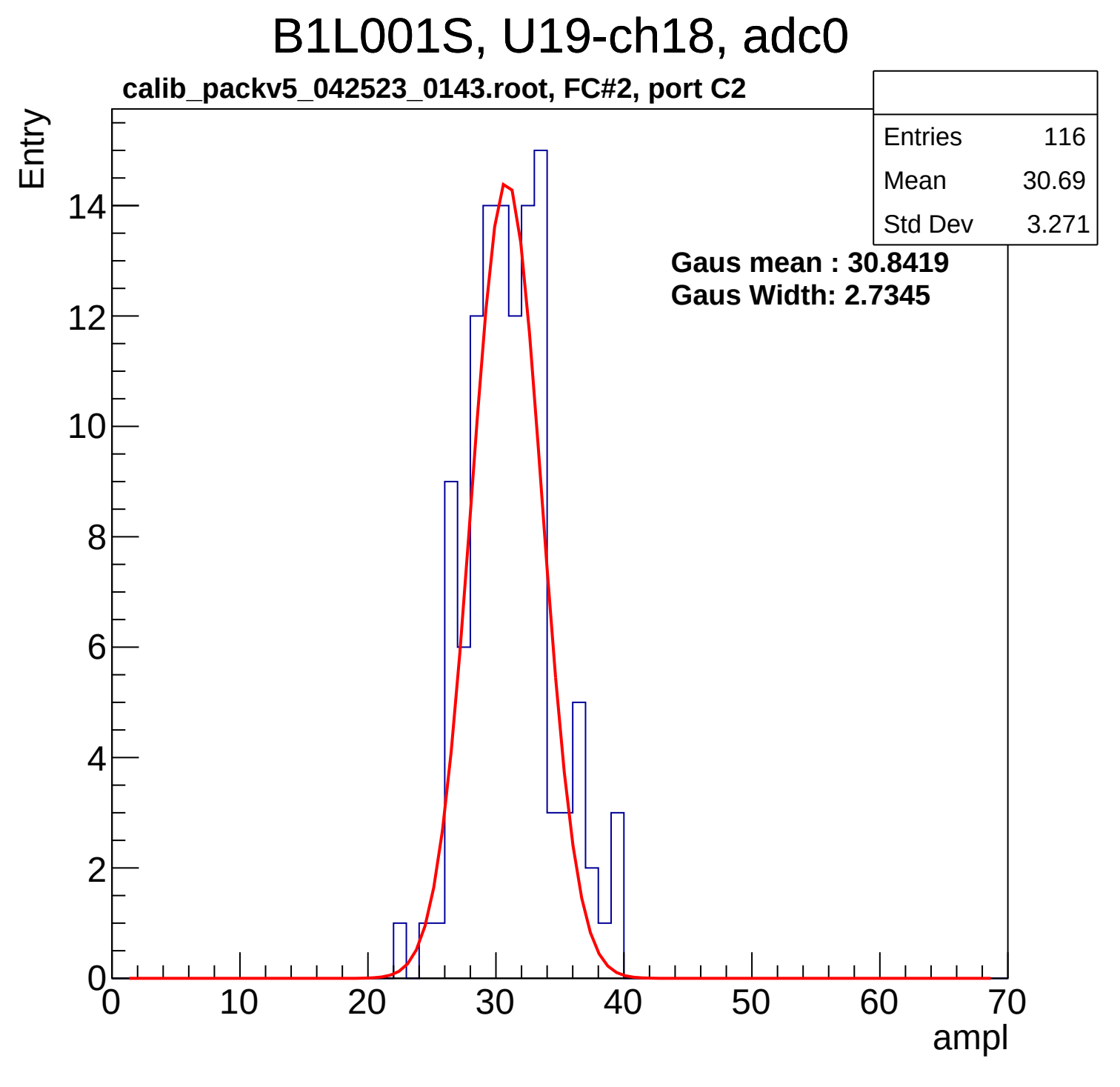
50
60
70
ampl


B1L001S, U19-ch18, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 116
Mean 30.69
Std Dev 3.271
Gaus mean : 30.8419
Gaus Width: 2.7345
Entry
ampl
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6
8
10
12
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0
10
20
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40
50
60
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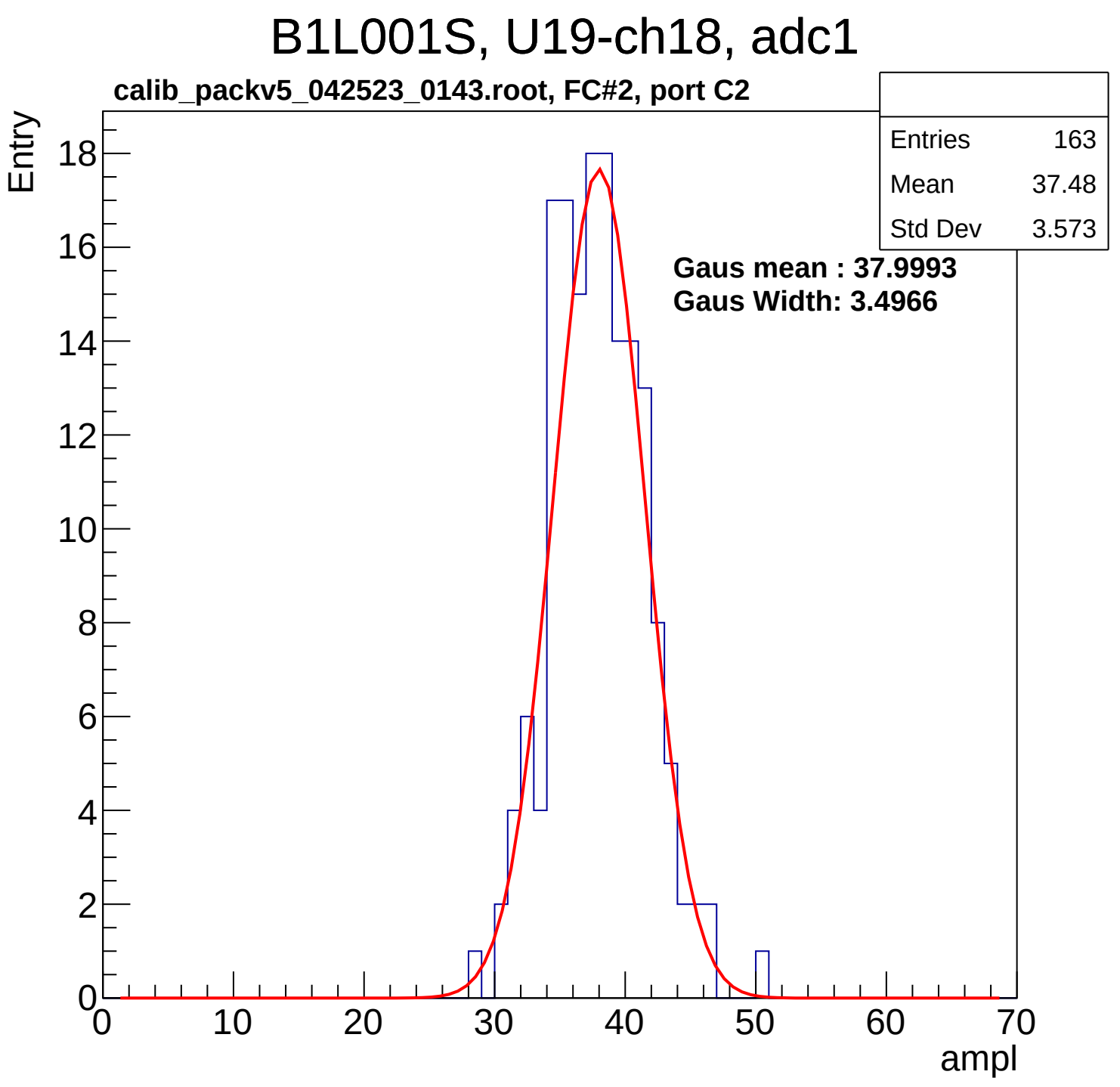
B1L001S, U19-ch18, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 163
Mean 37.48
Std Dev 3.573
Gaus mean : 37.9993
Gaus Width: 3.4966
Entry
ampl
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2
4
6
8
10
12
14
16
18
0
10
20
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40
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60
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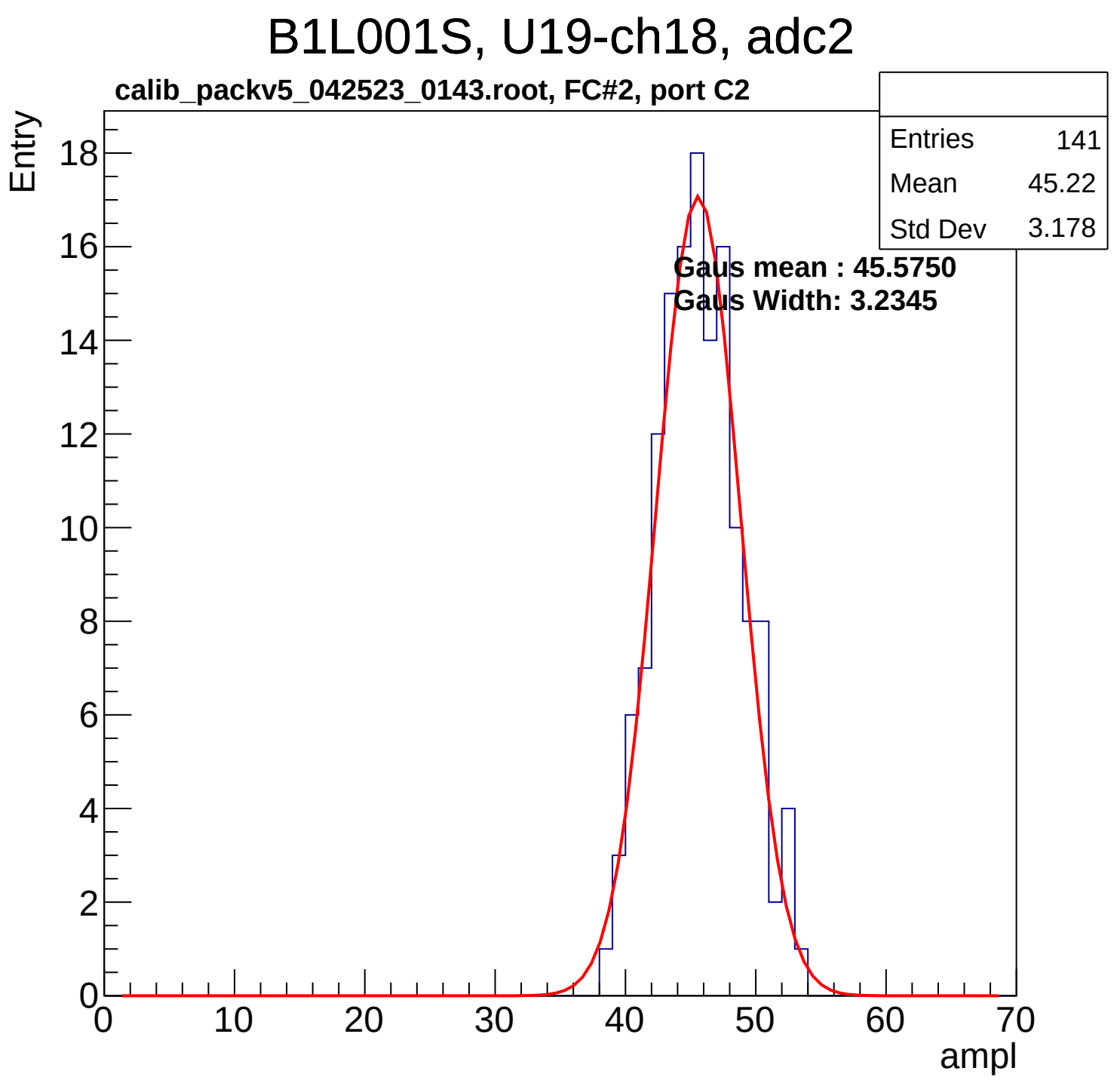
B1L001S, U19-ch18, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 141
Mean 45.22
Std Dev 3.178
Gaus mean : 45.5750
Gaus Width: 3.2345
Entry
ampl
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6
8
10
12
14
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18
0
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60
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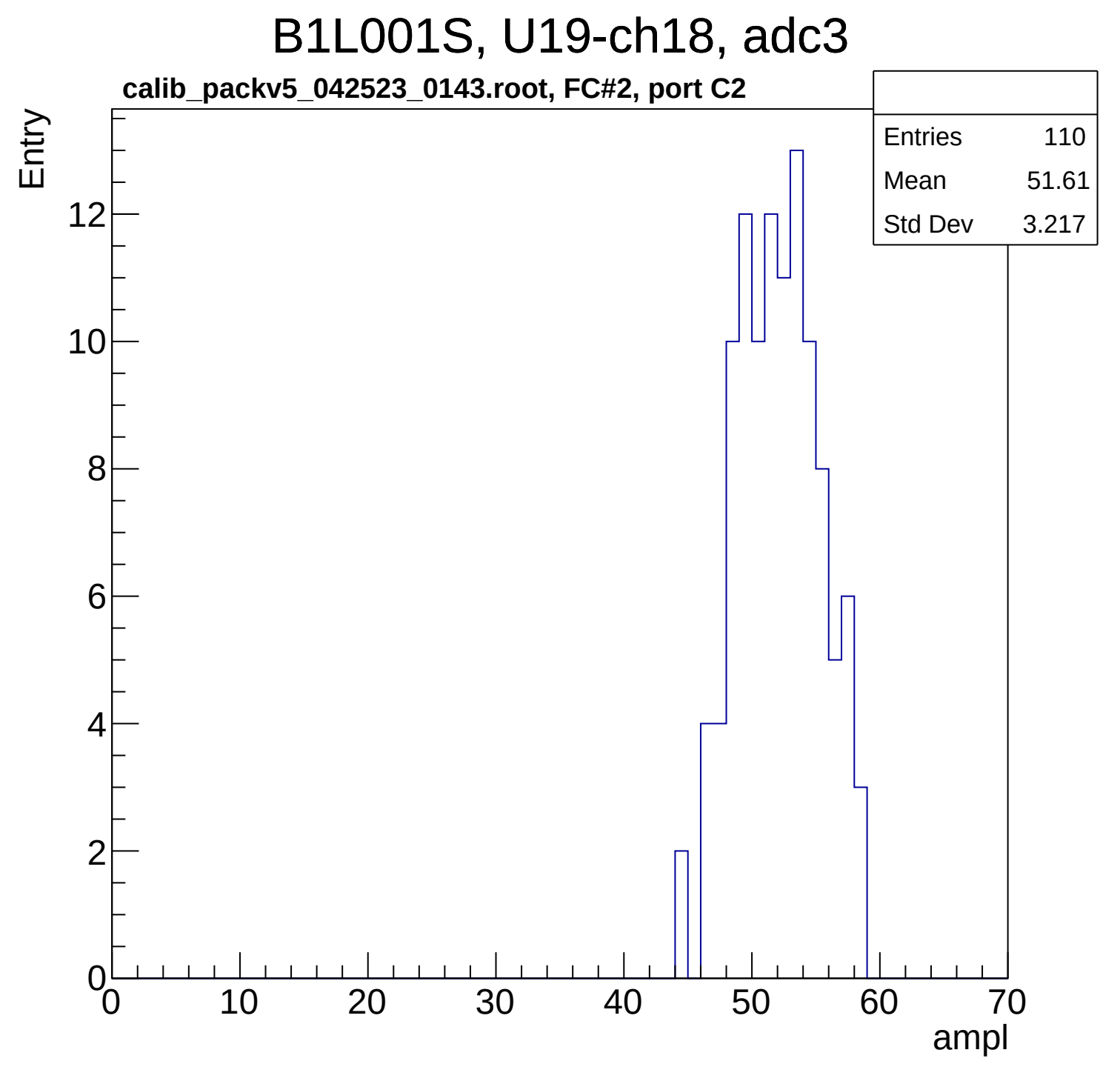
B1L001S, U19-ch18, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 110
Mean 51.61
Std Dev 3.217
Entry
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10
12
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10
20
30
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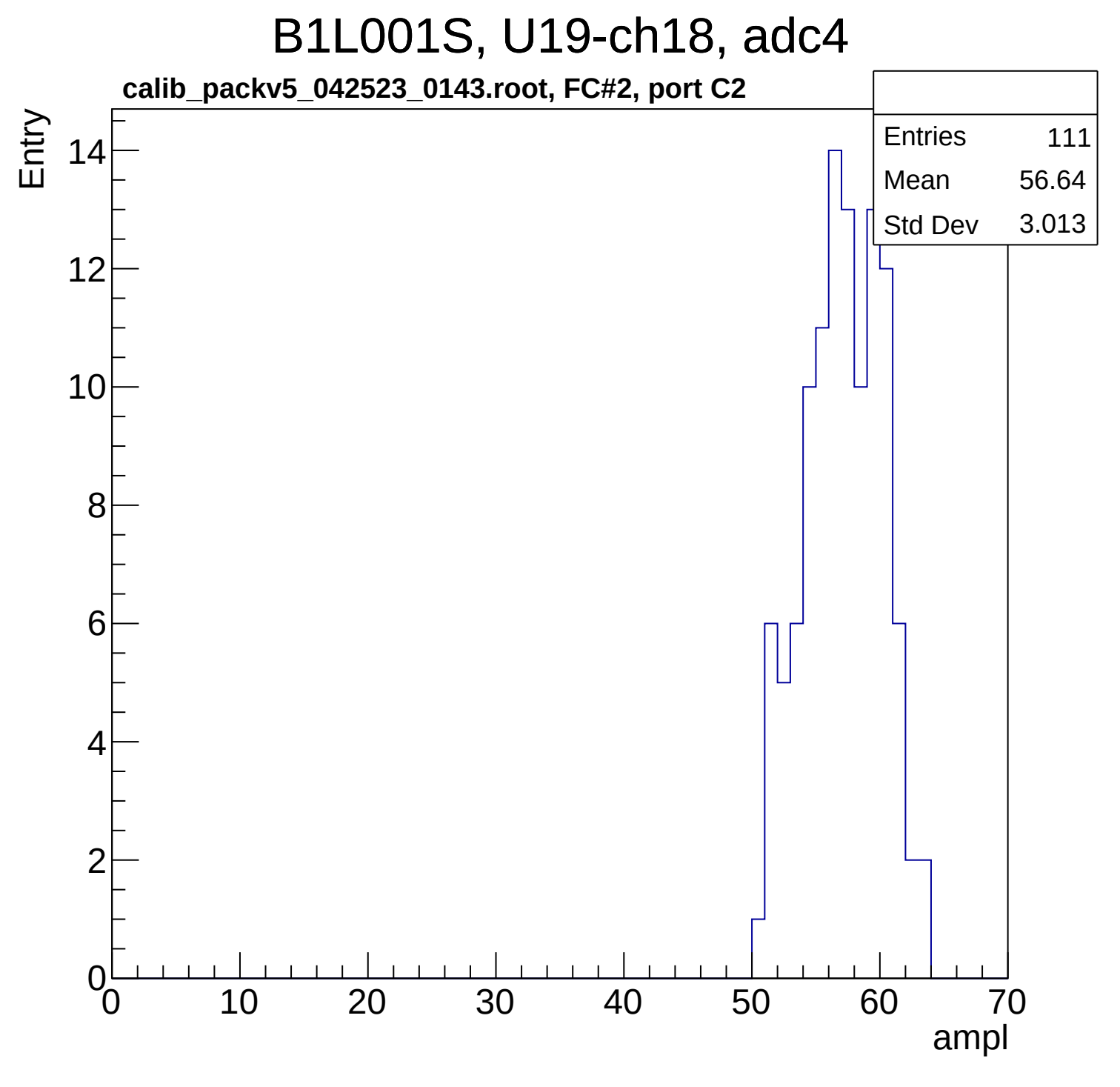
50
60
70
ampl


B1L001S, U19-ch18, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 111
Mean 56.64
Std Dev 3.013
Entry
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10
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14
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10
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30
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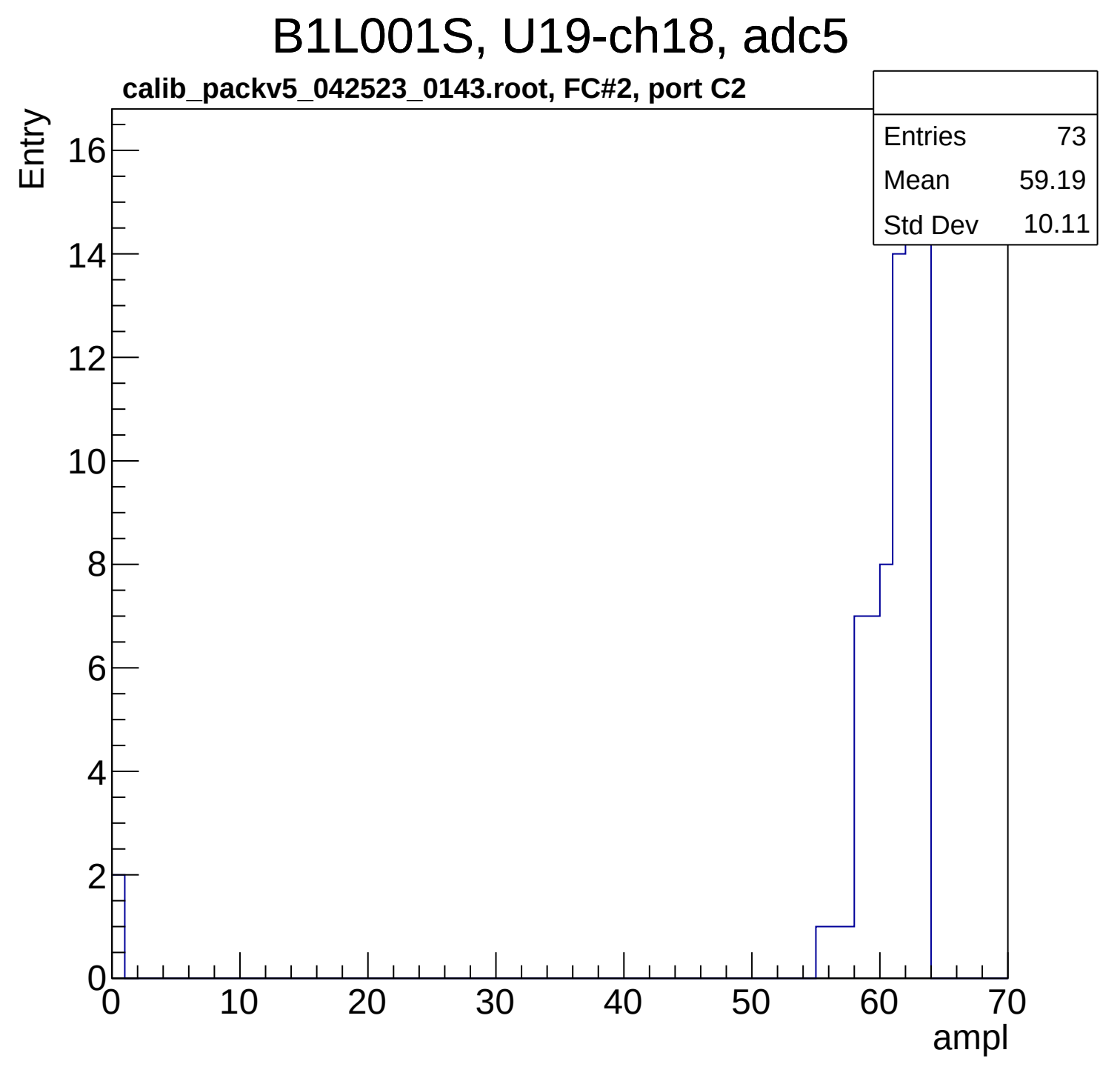
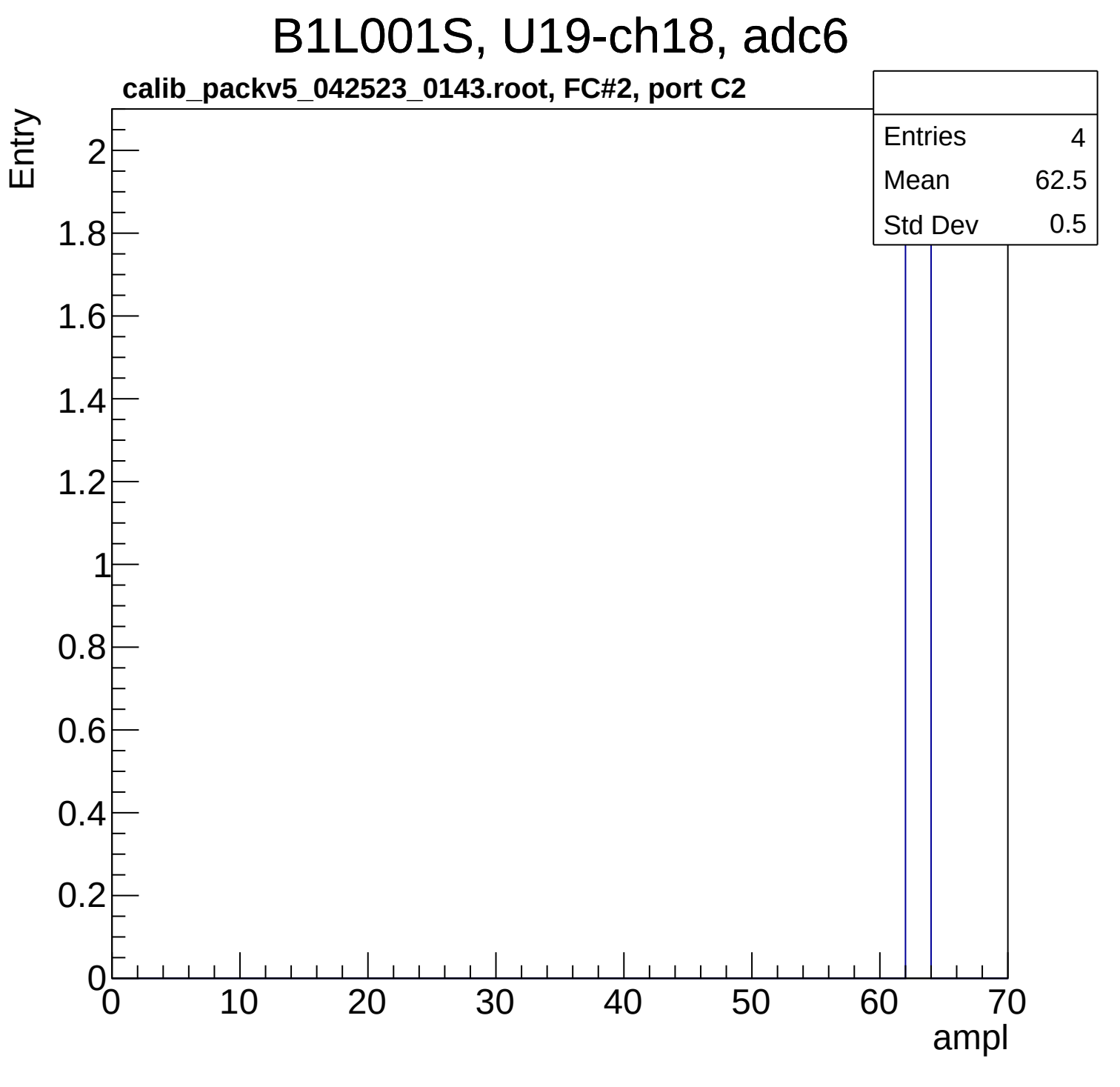
50
60
70
ampl


B1L001S, U19-ch18, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 73
Mean 59.19
Std Dev 10.11
Entry
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch18, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 4
Mean 62.5
Std Dev 0.5
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
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40
50
60
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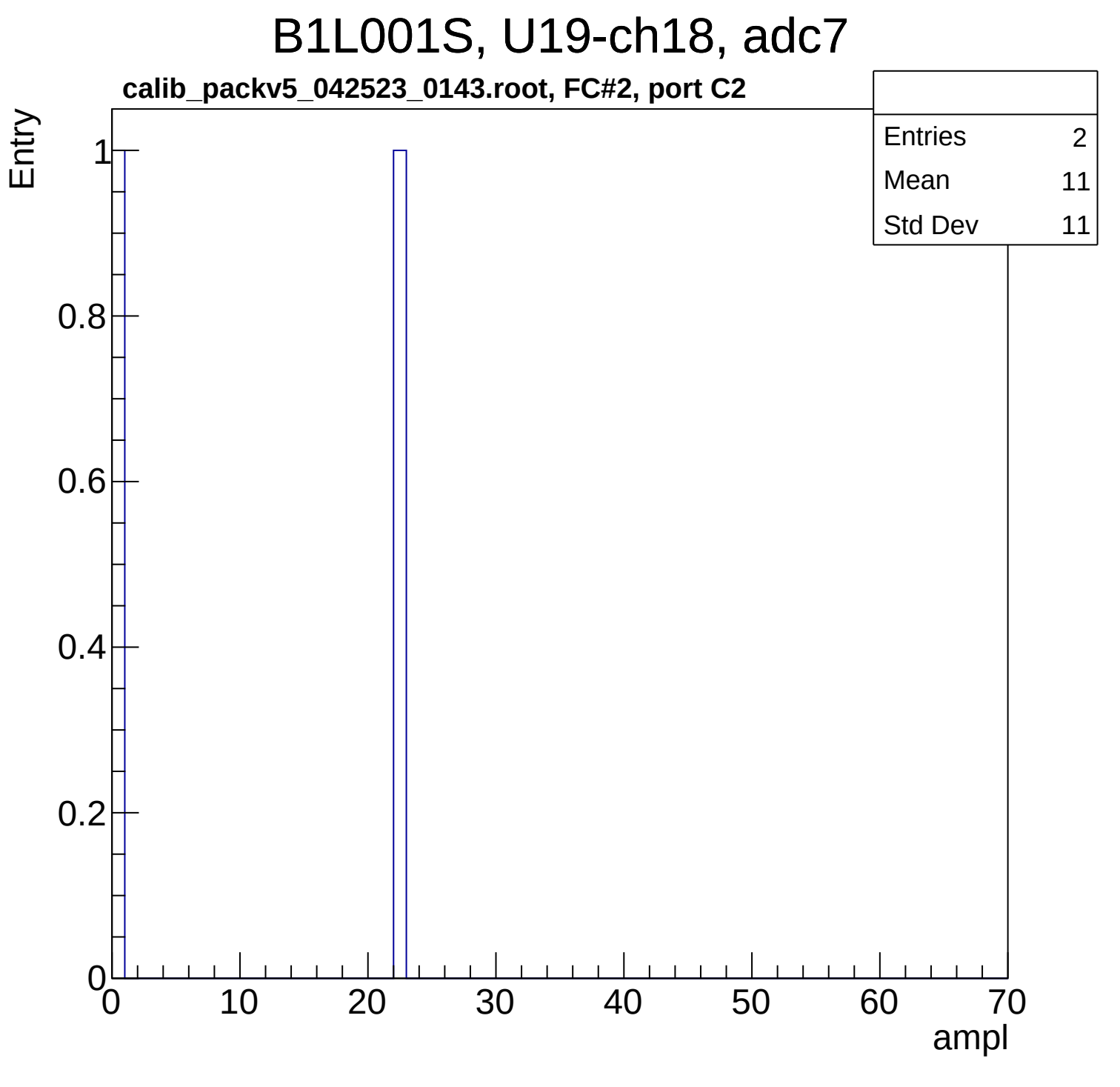
B1L001S, U19-ch18, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 11
Std Dev 11
Entry
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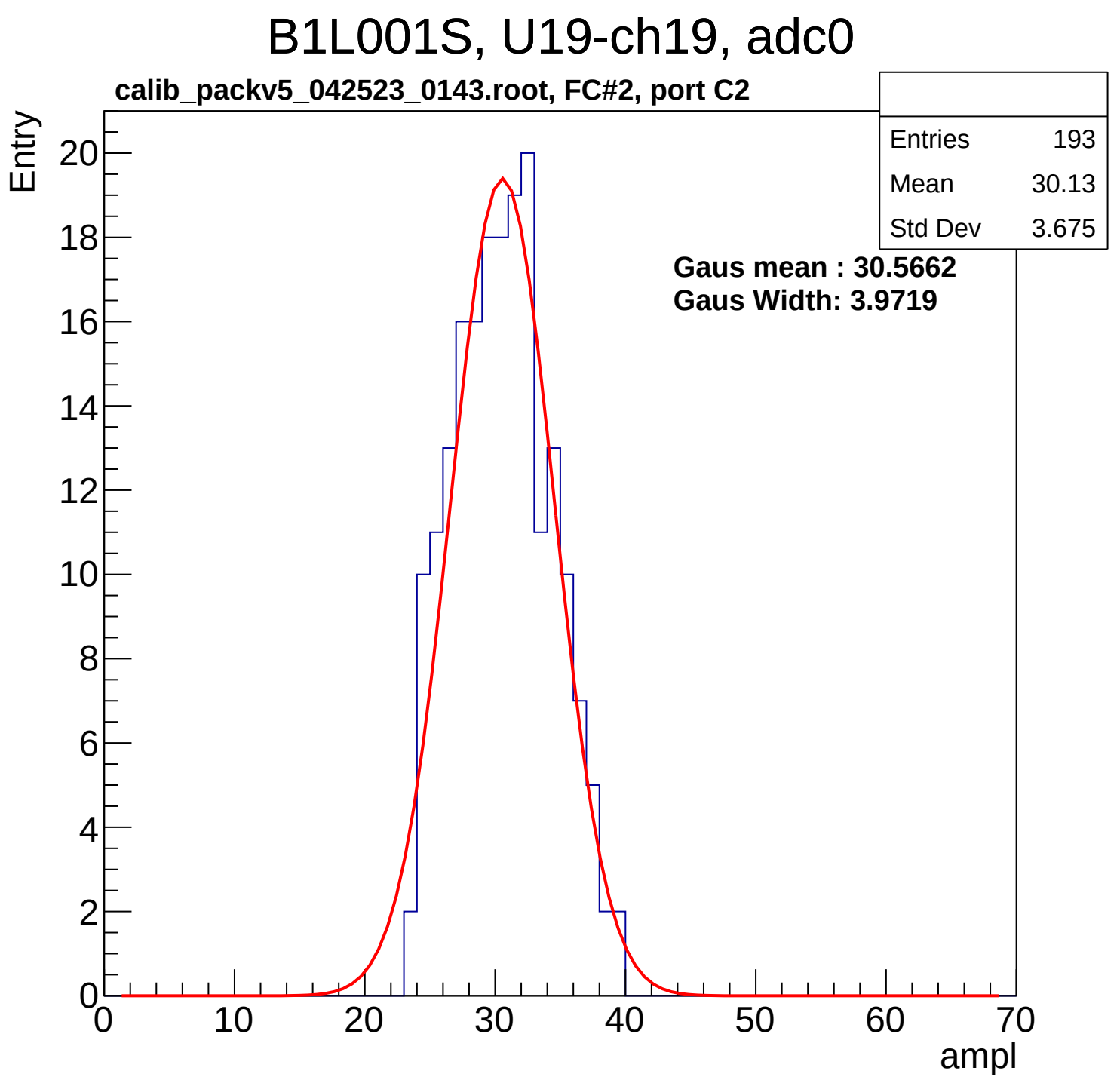
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch19, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 193
Mean 30.13
Std Dev 3.675
Gaus mean : 30.5662
Gaus Width: 3.9719
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
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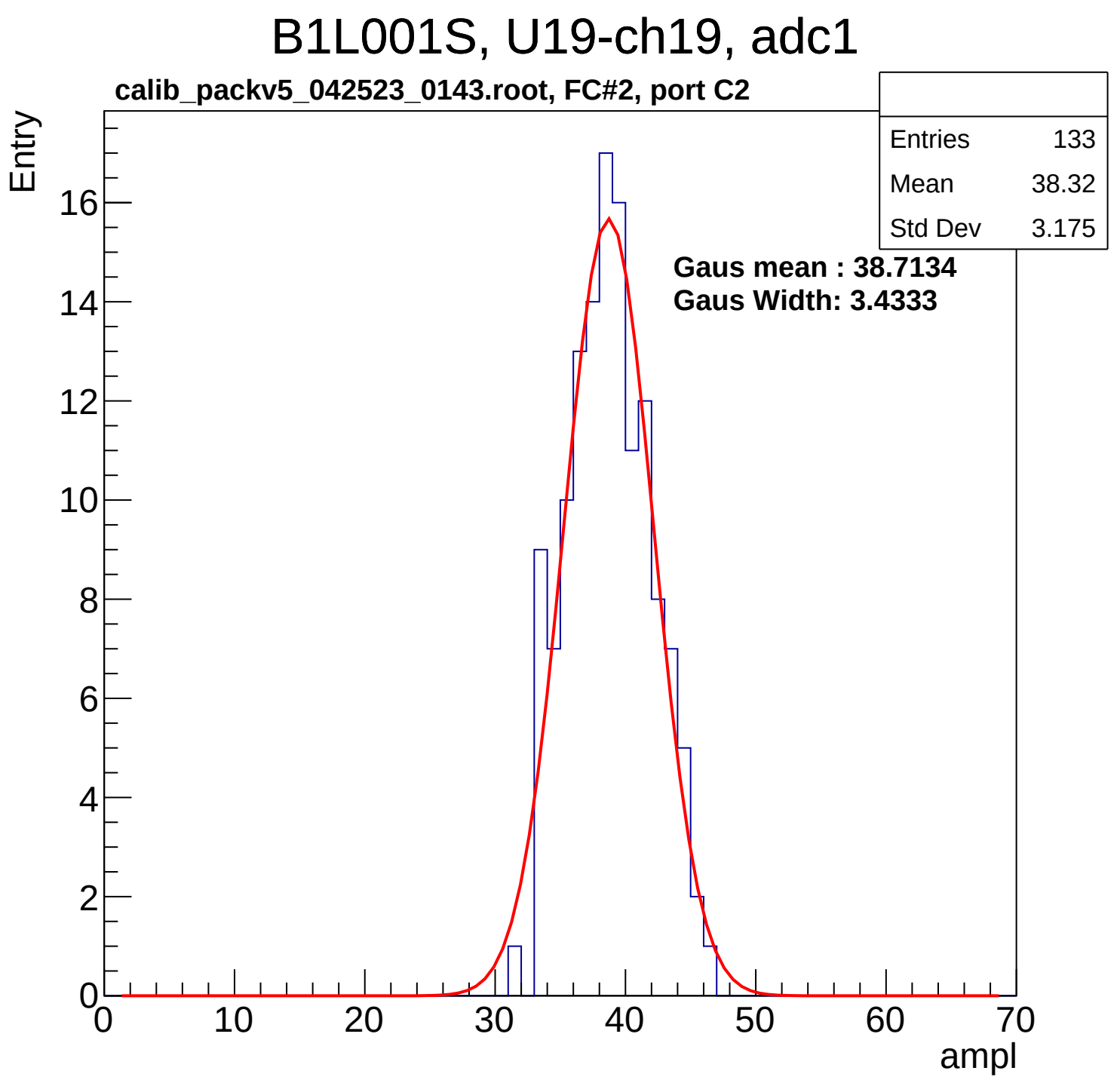
B1L001S, U19-ch19, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 133
Mean 38.32
Std Dev 3.175
Gaus mean : 38.7134
Gaus Width: 3.4333
Entry
ampl
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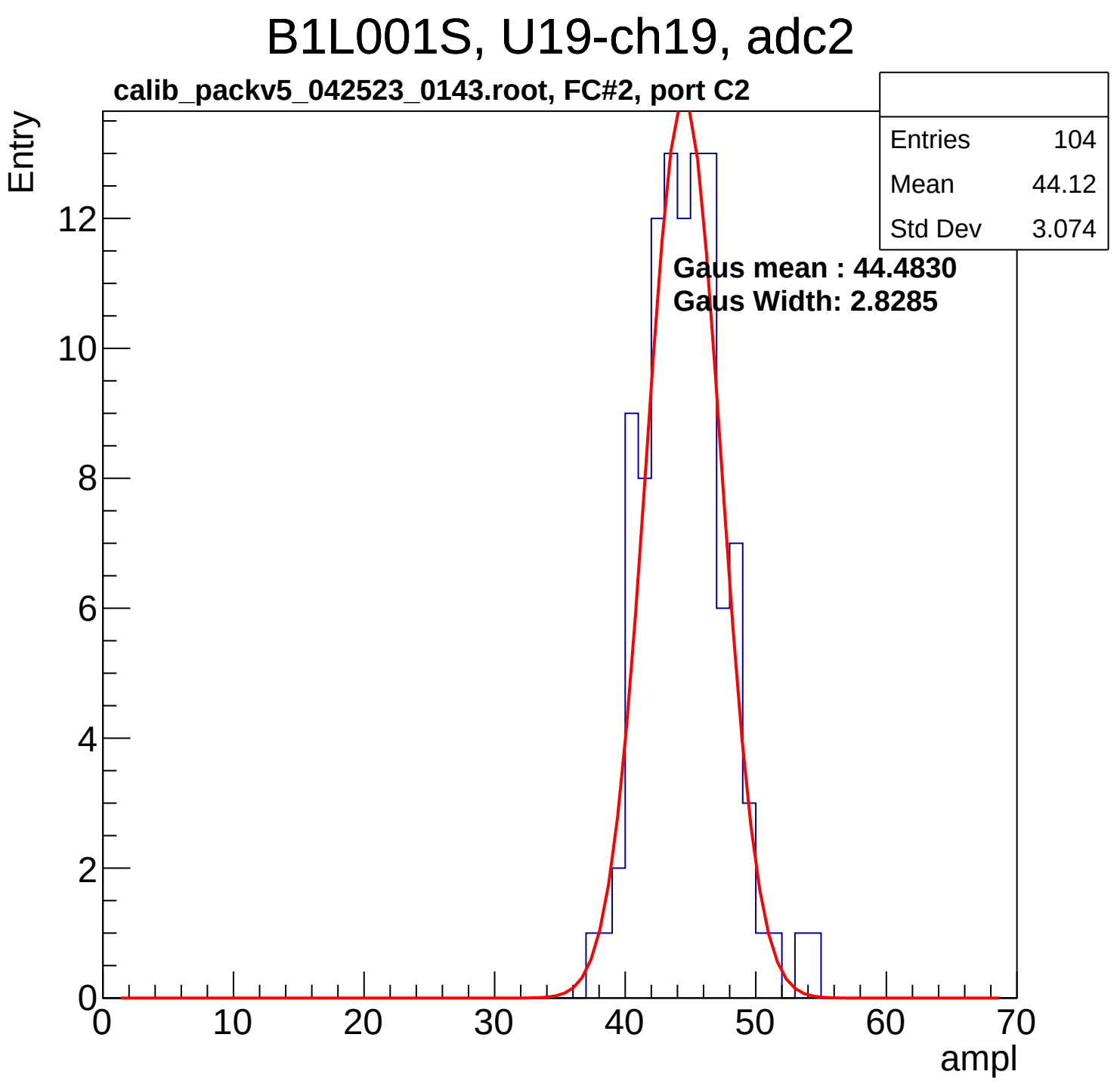
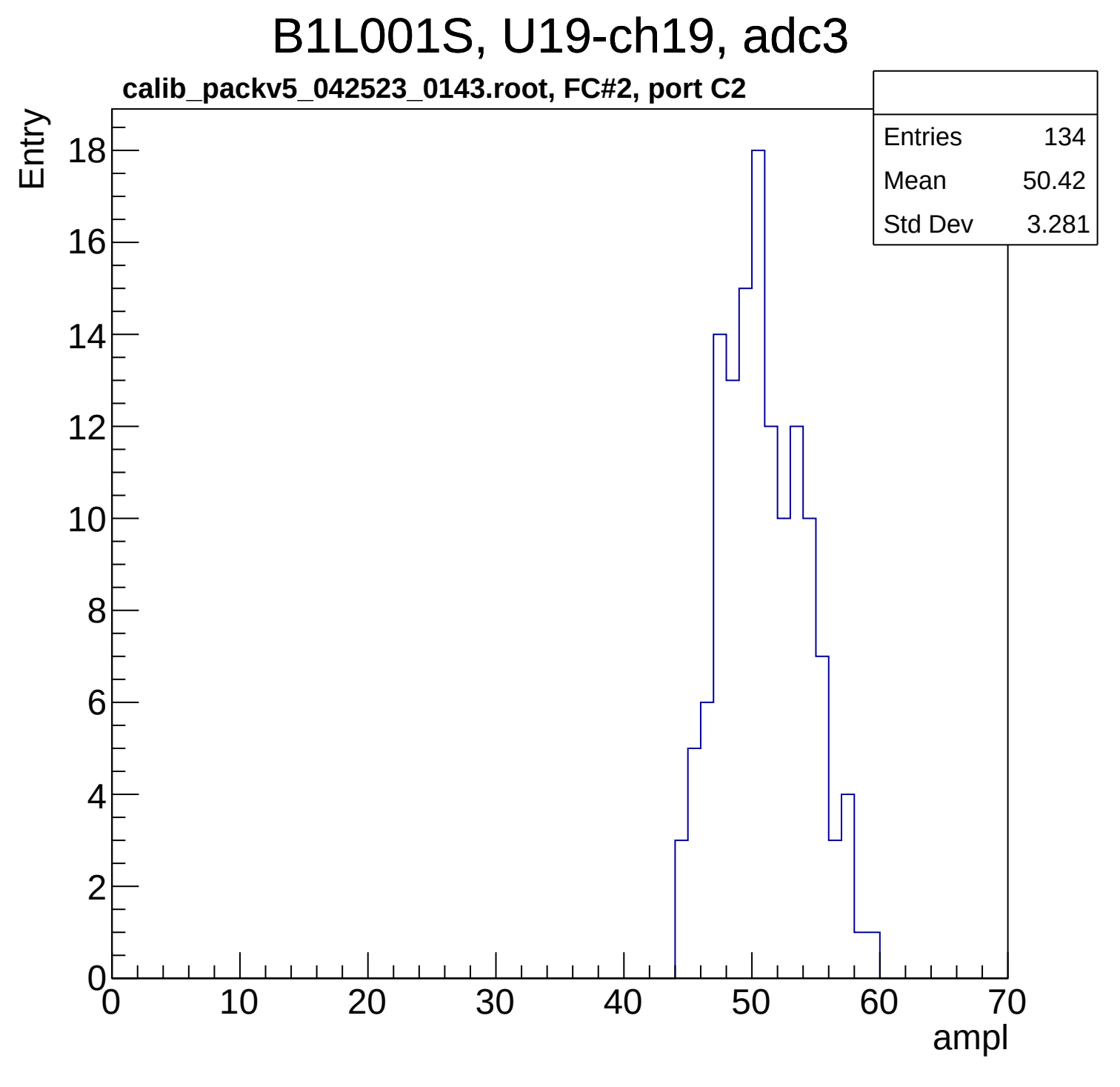
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70


B1L001S, U19-ch19, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 104
Mean 44.12
Std Dev 3.074
Gaus mean : 44.4830
Gaus Width: 2.8285
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70


B1L001S, U19-ch19, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 134
Mean 50.42
Std Dev 3.281
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
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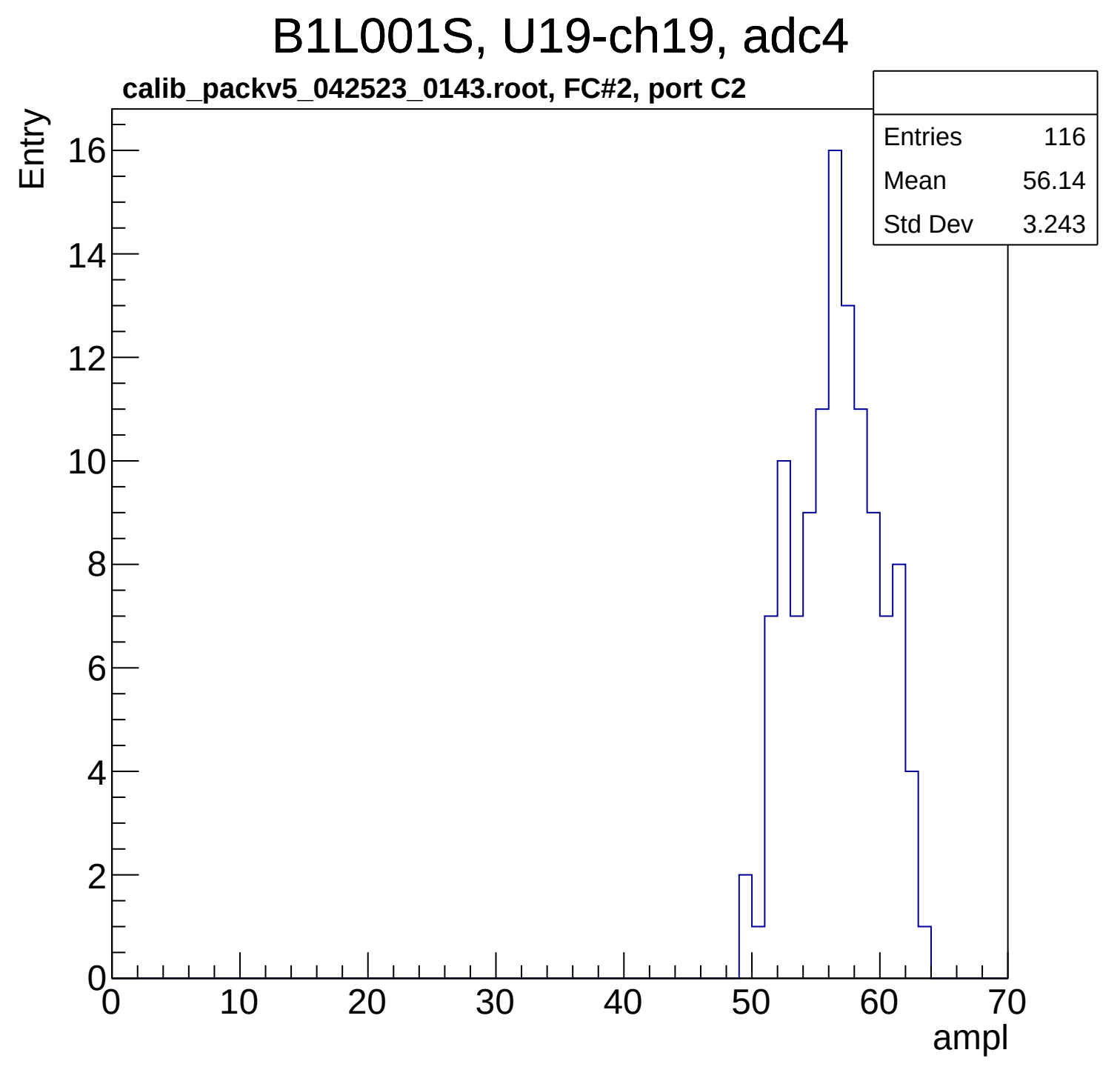
B1L001S, U19-ch19, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 116
Mean 56.14
Std Dev 3.243
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
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40
50
60
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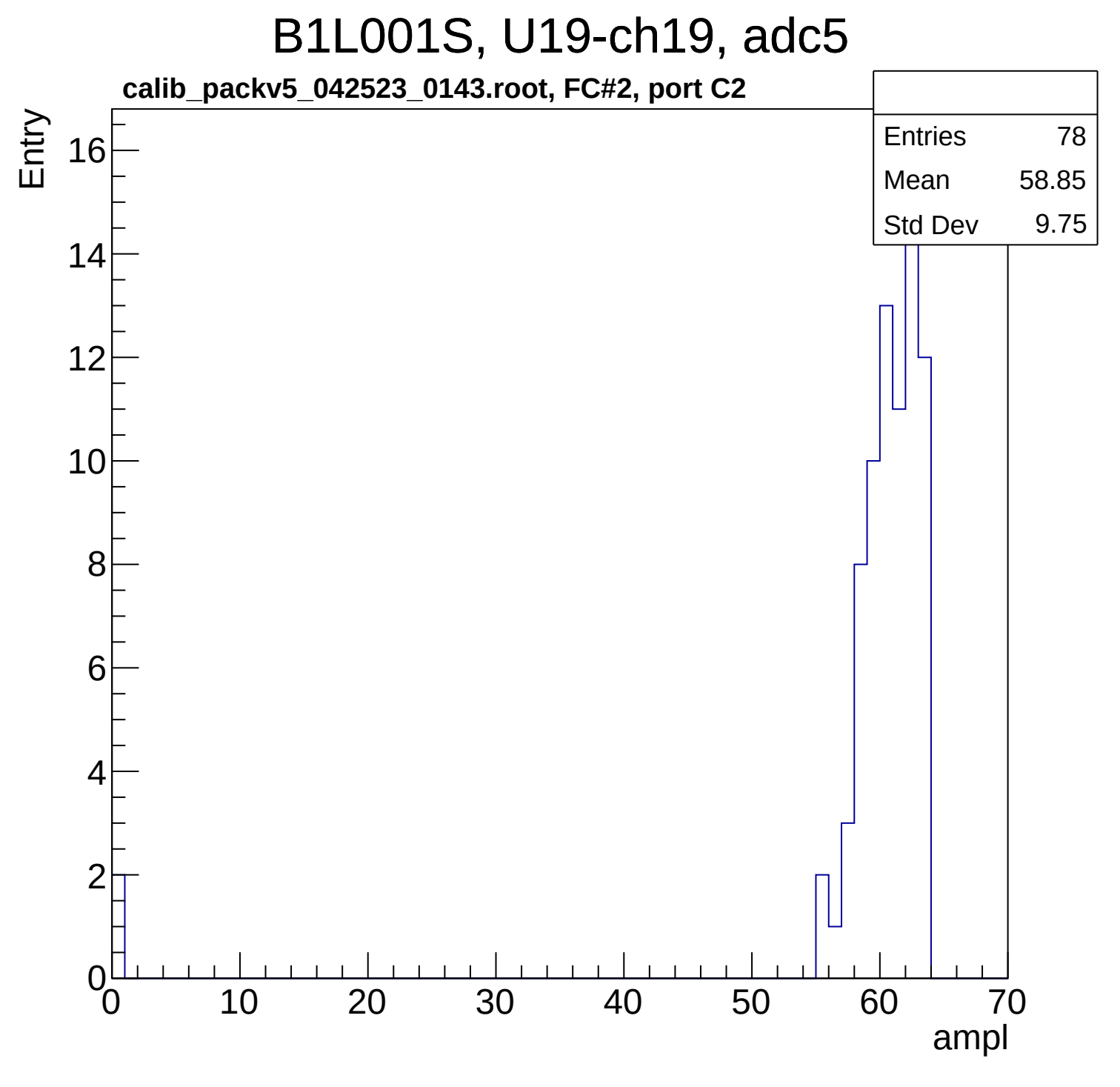
B1L001S, U19-ch19, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 78
Mean 58.85
Std Dev 9.75
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
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40
50
60
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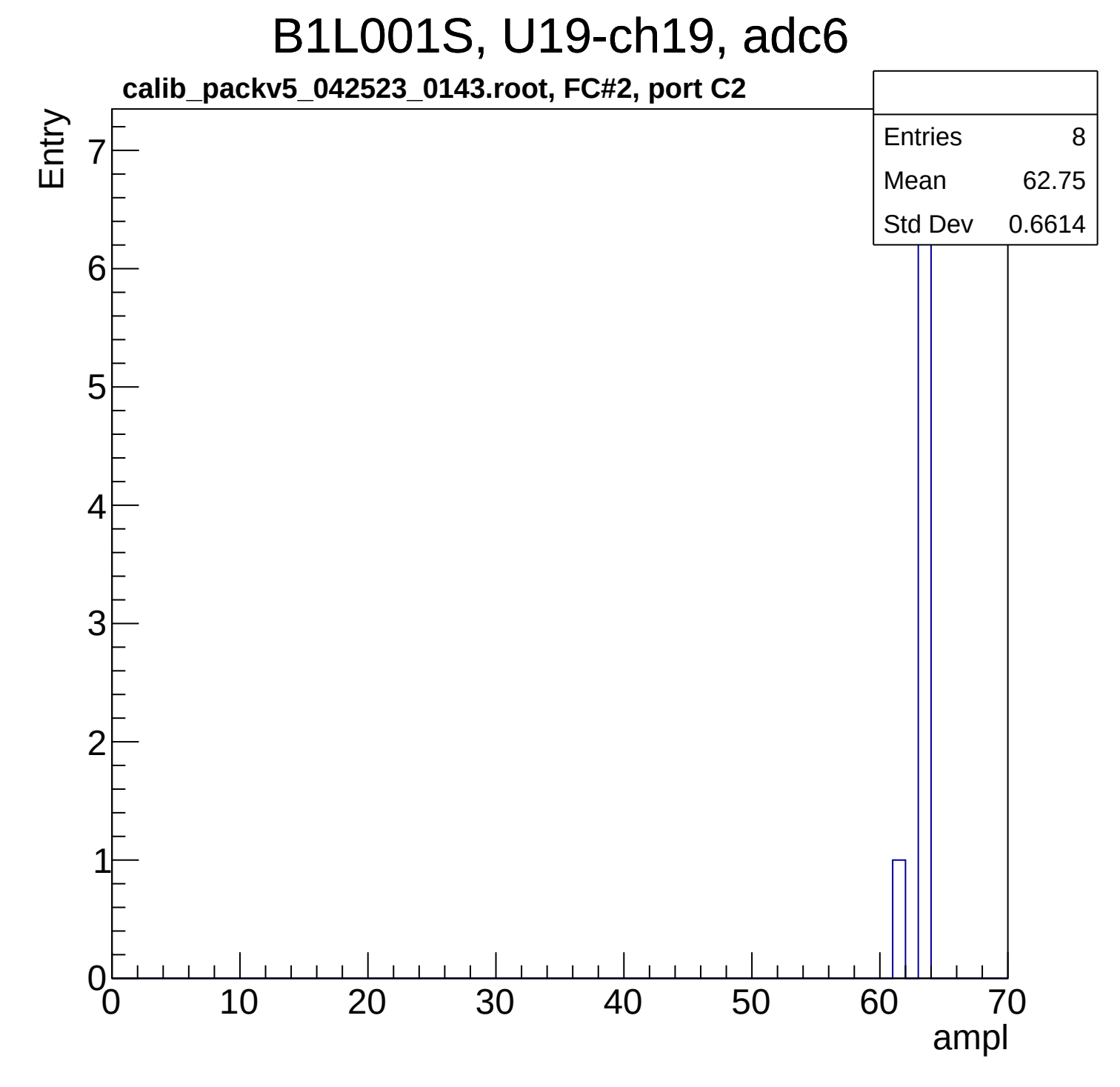
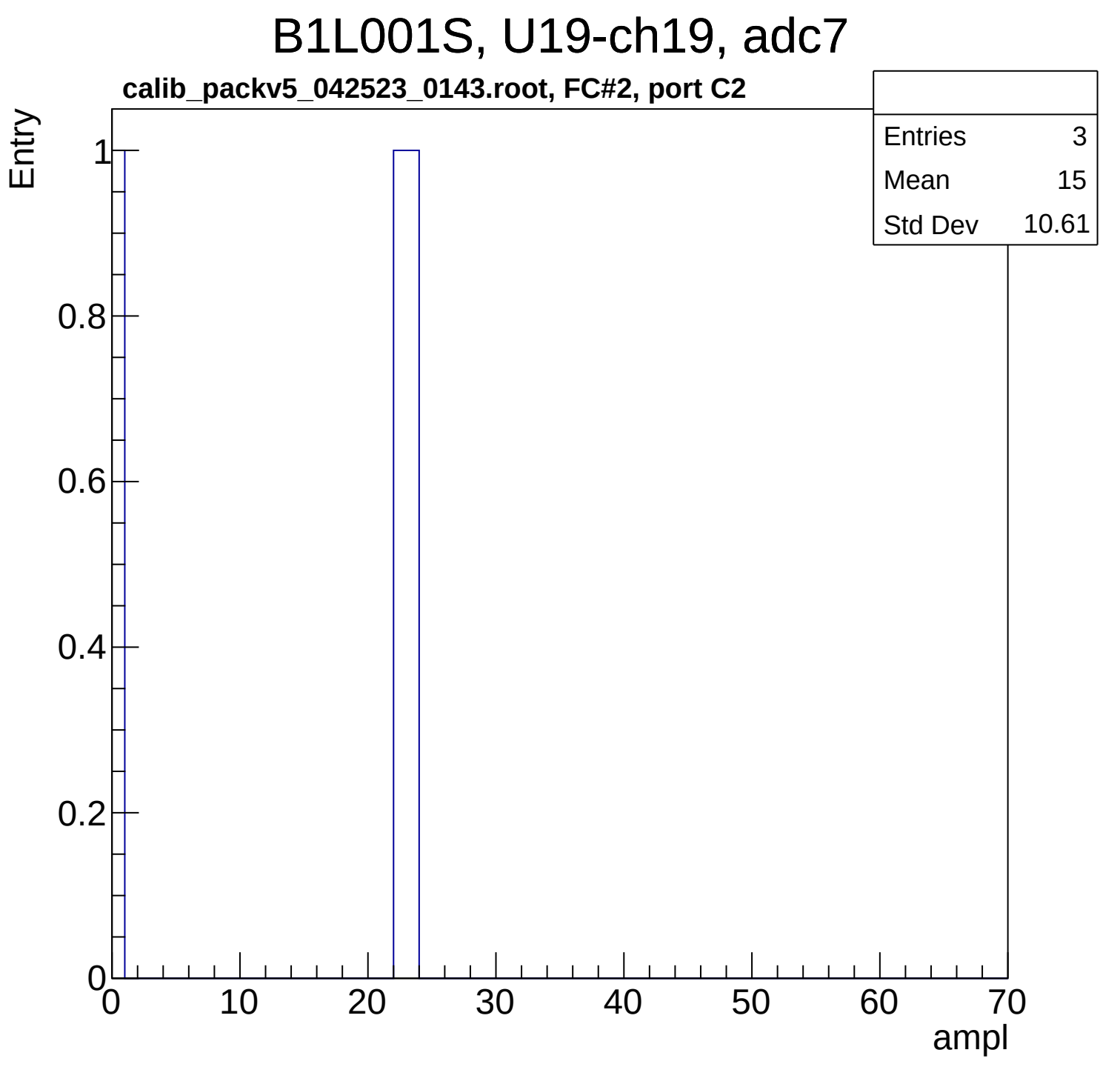
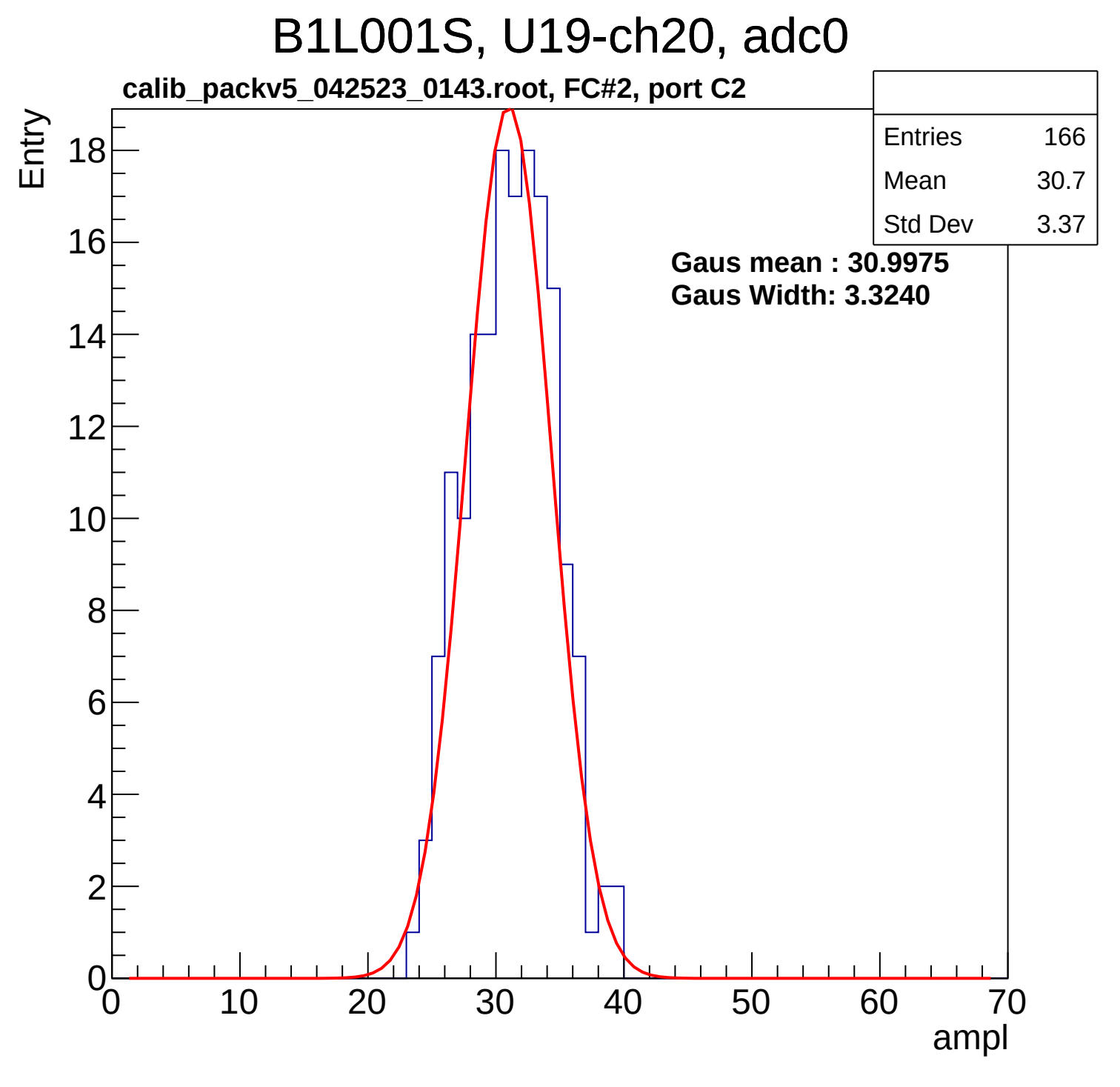

B1L001S, U19-ch19, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 8
Mean 62.75
Std Dev 0.6614
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L001S, U19-ch19, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 3
Mean 15
Std Dev 10.61
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70


B1L001S, U19-ch20, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 166
Mean 30.7
Std Dev 3.37
Gaus mean : 30.9975
Gaus Width: 3.3240
Entry
ampl
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4
6
8
10
12
14
16
18
0
10
20
30
40
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60
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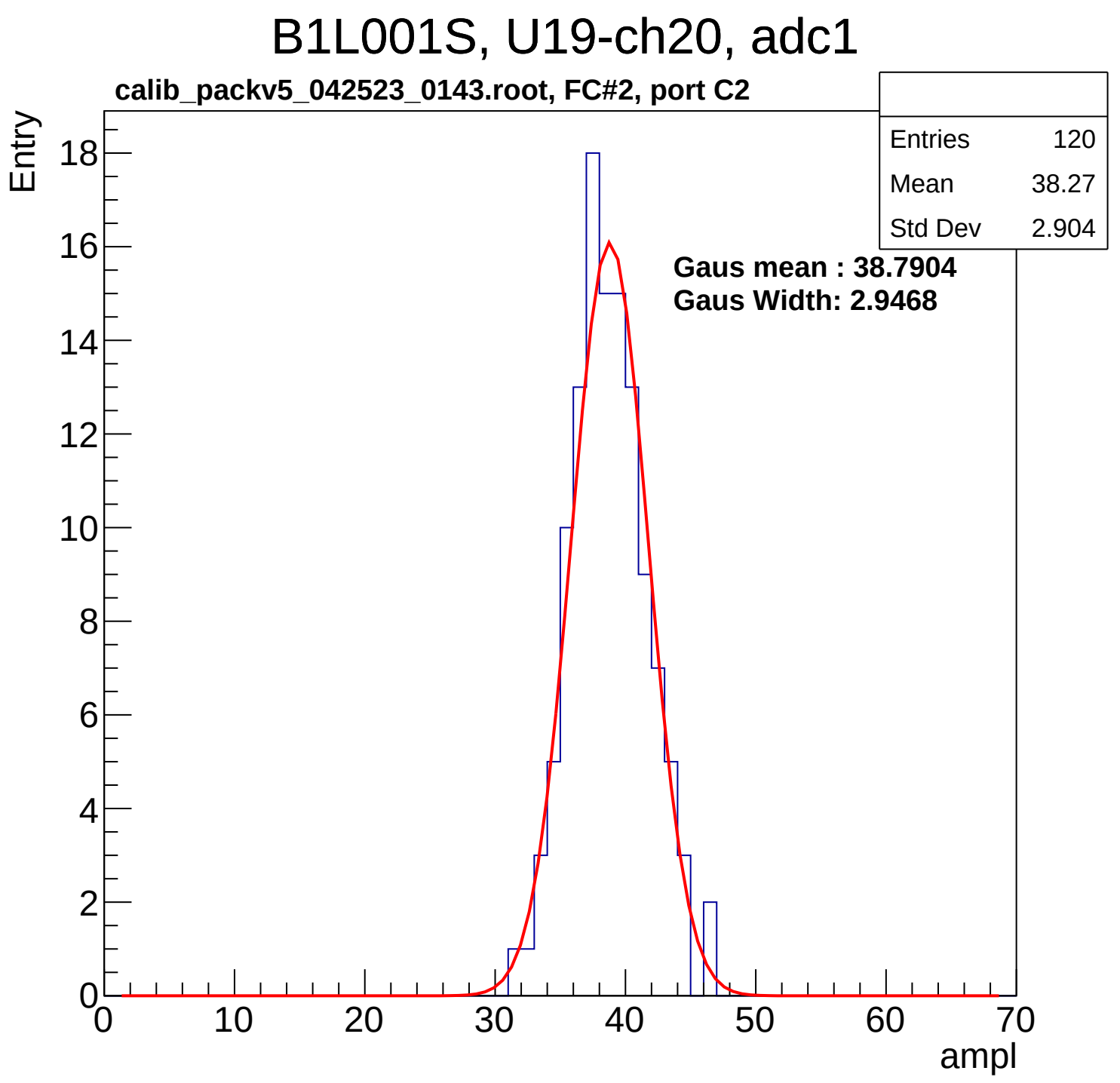
B1L001S, U19-ch20, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 120
Mean 38.27
Std Dev 2.904
Gaus mean : 38.7904
Gaus Width: 2.9468
Entry
ampl
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2
4
6
8
10
12
14
16
18
0
10
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30
40
50
60
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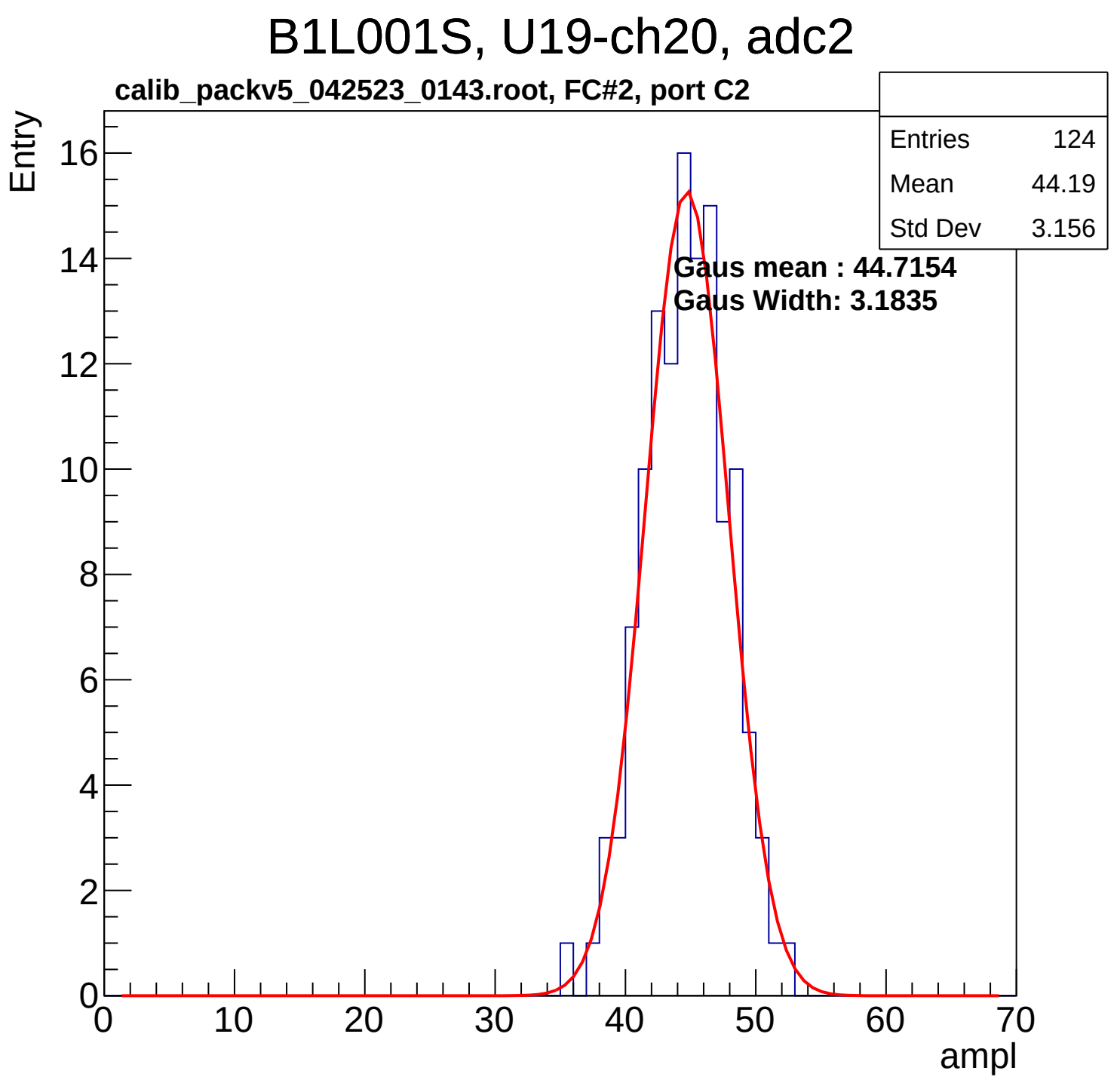
B1L001S, U19-ch20, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 124
Mean 44.19
Std Dev 3.156
Gaus mean : 44.7154
Gaus Width: 3.1835
Entry
ampl
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2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
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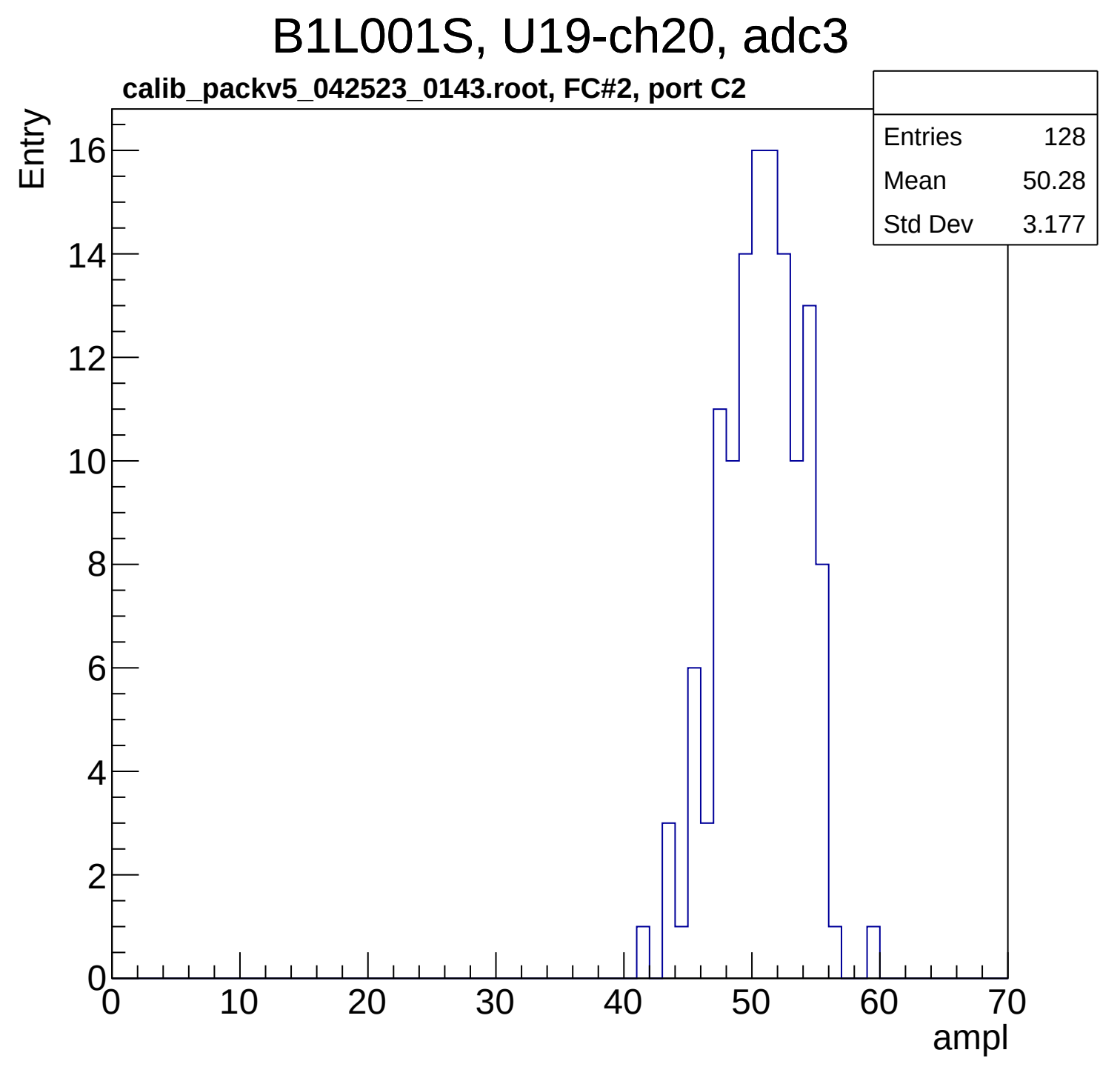
B1L001S, U19-ch20, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 128
Mean 50.28
Std Dev 3.177
Entry
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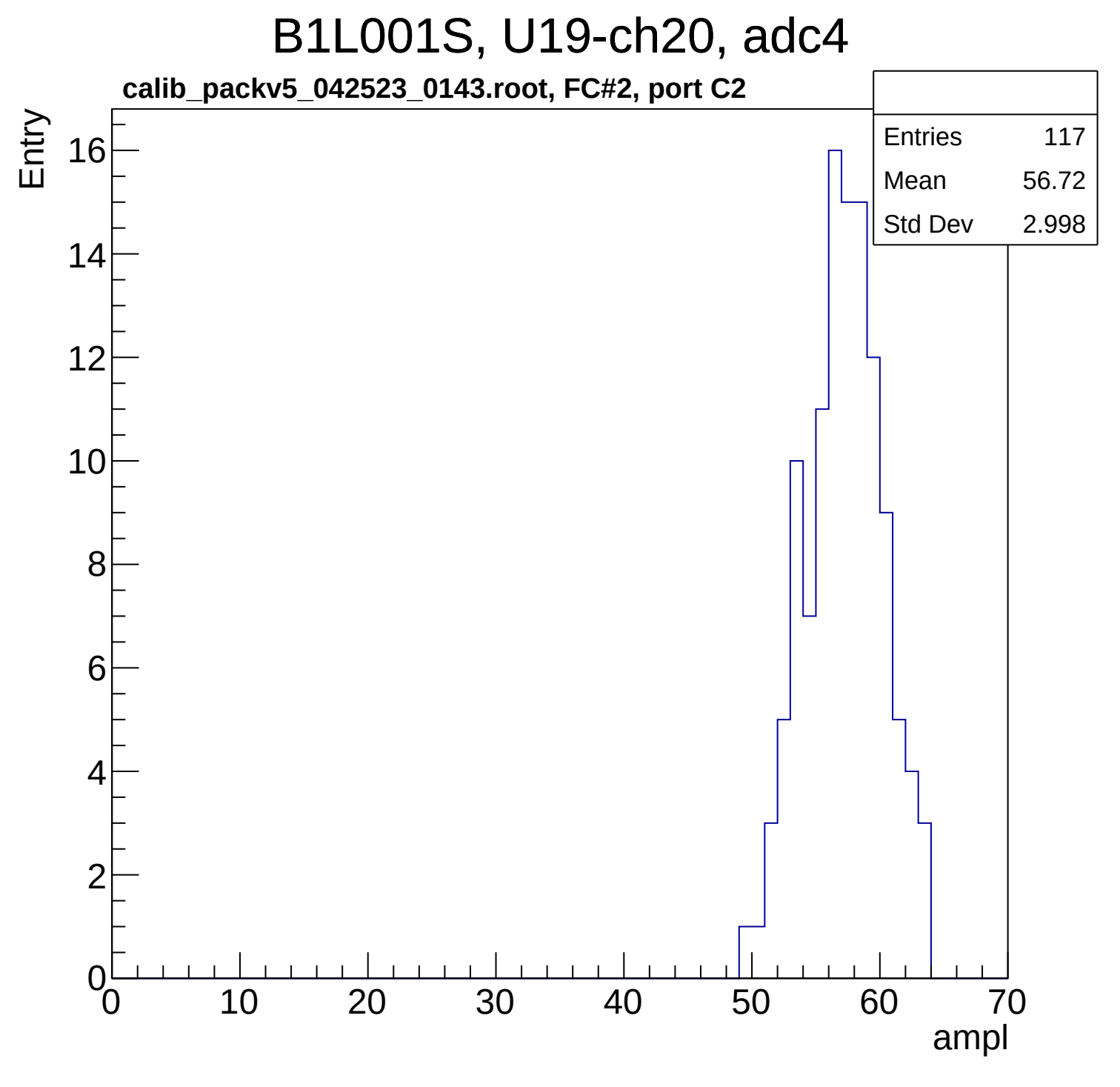
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch20, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 117
Mean 56.72
Std Dev 2.998
Entry
0
2
4
6
8
10
12
14
16
0
10
20
30
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50
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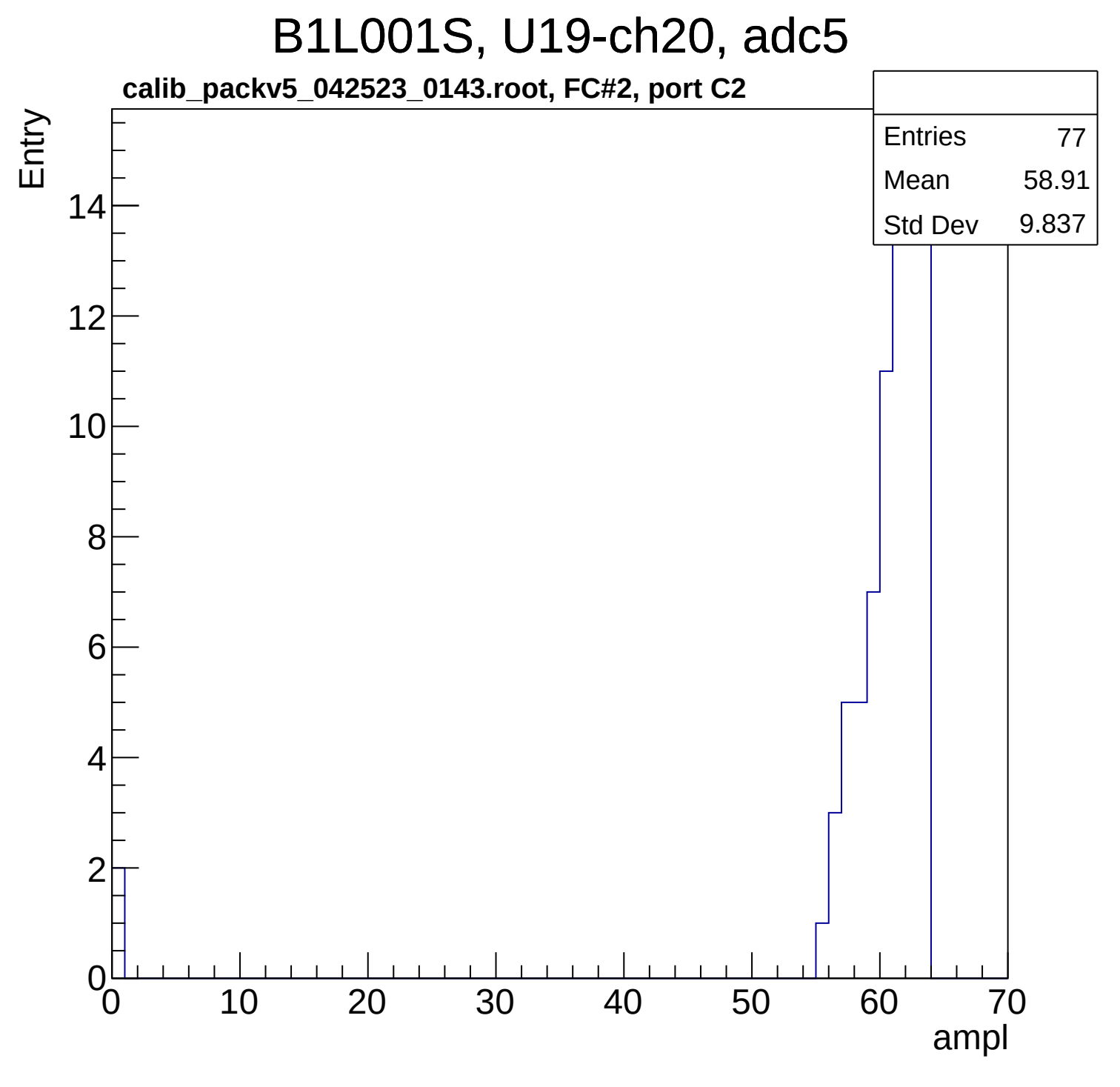
70
ampl


B1L001S, U19-ch20, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 77
Mean 58.91
Std Dev 9.837
Entry
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2
4
6
8
10
12
14
0
10
20
30
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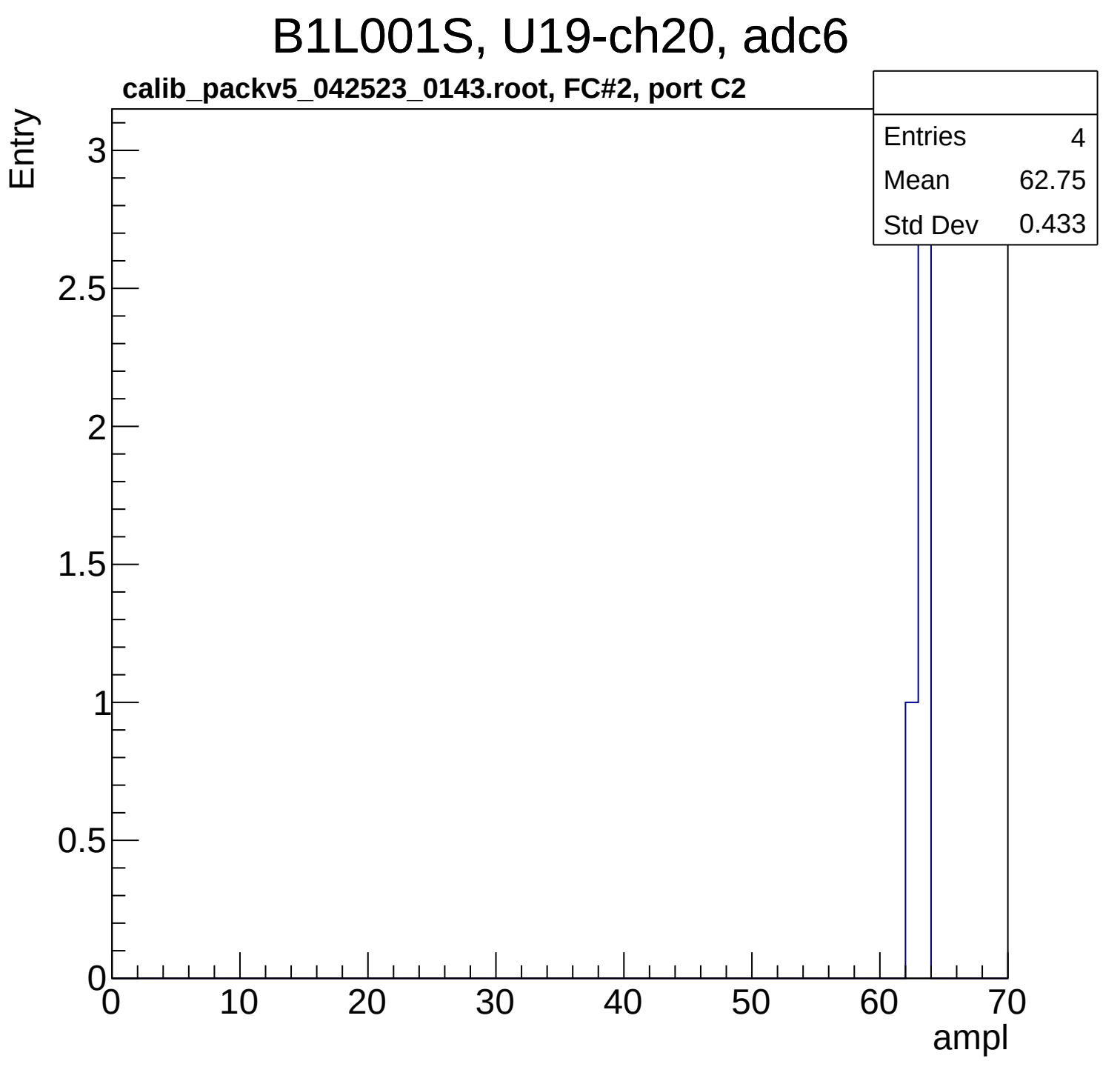
50
60
70
ampl


B1L001S, U19-ch20, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 4
Mean 62.75
Std Dev 0.433
Entry
ampl
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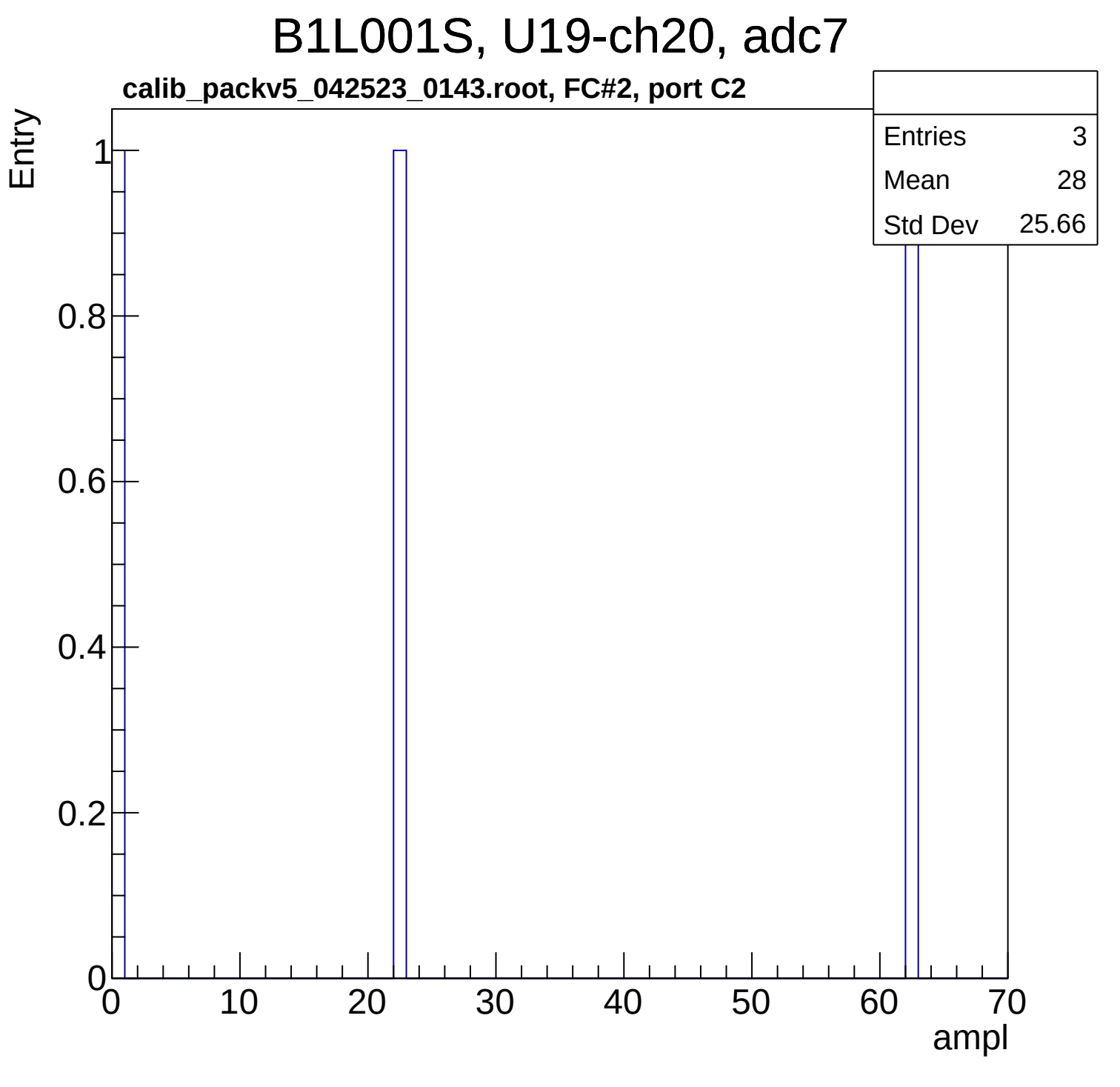
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L001S, U19-ch20, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 3
Mean 28
Std Dev 25.66
Entry
ampl
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0.2
0.4
0.6
0.8
1
0
10
20
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40
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60
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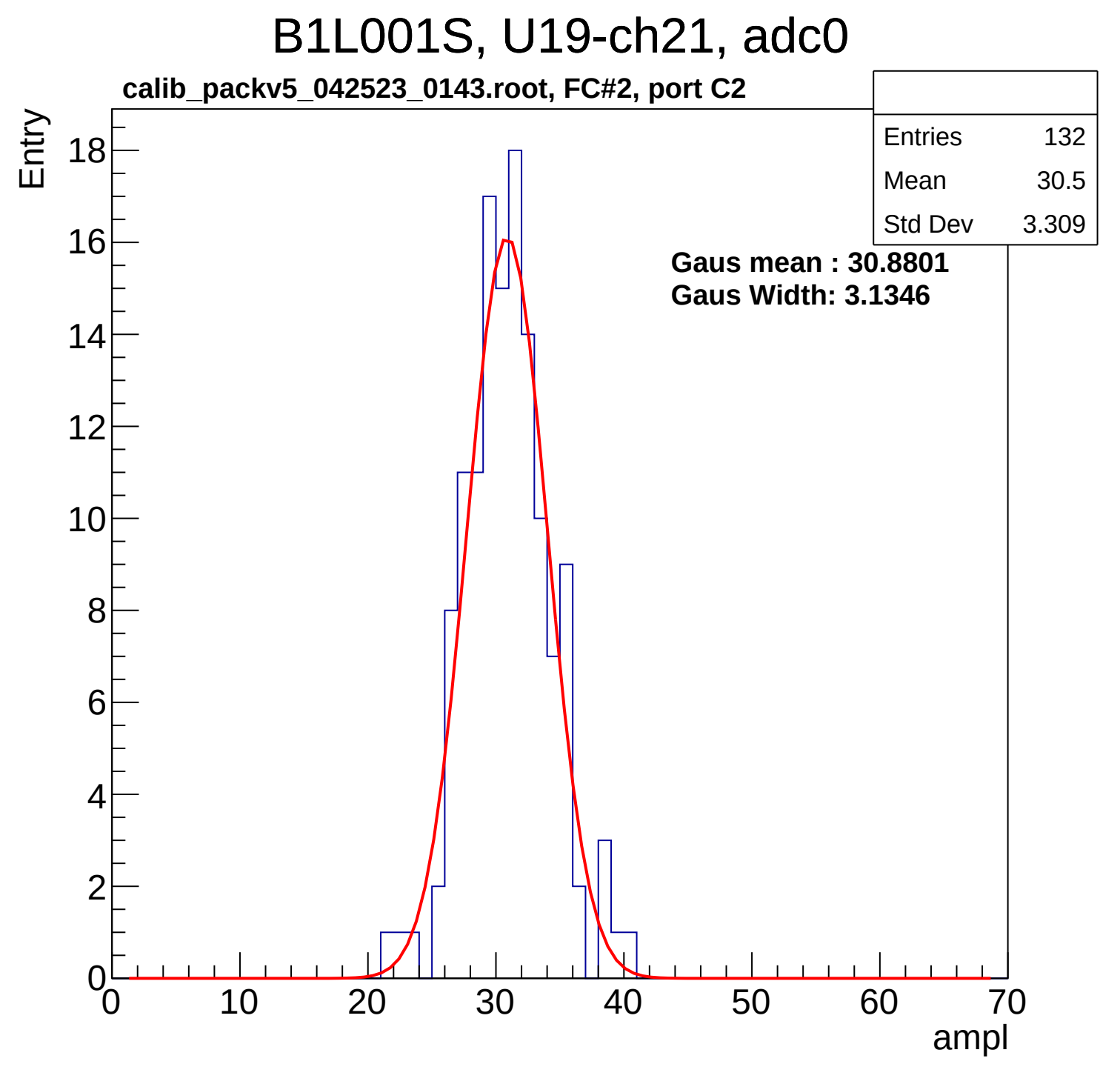
B1L001S, U19-ch21, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 132
Mean 30.5
Std Dev 3.309
Gaus mean : 30.8801
Gaus Width: 3.1346
Entry
ampl
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4
6
8
10
12
14
16
18
0
10
20
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40
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60
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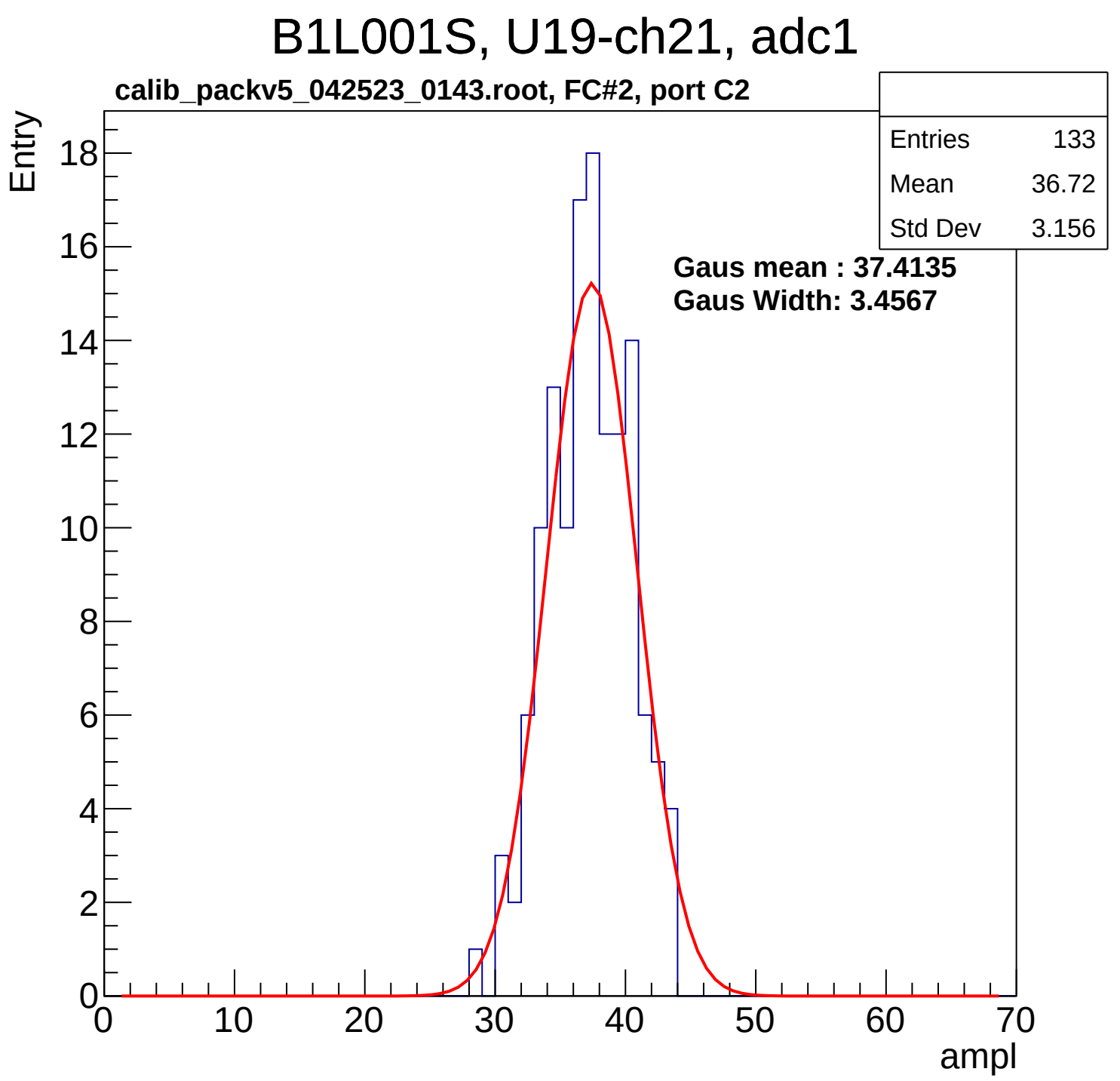
B1L001S, U19-ch21, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 133
Mean 36.72
Std Dev 3.156
Gaus mean : 37.4135
Gaus Width: 3.4567
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
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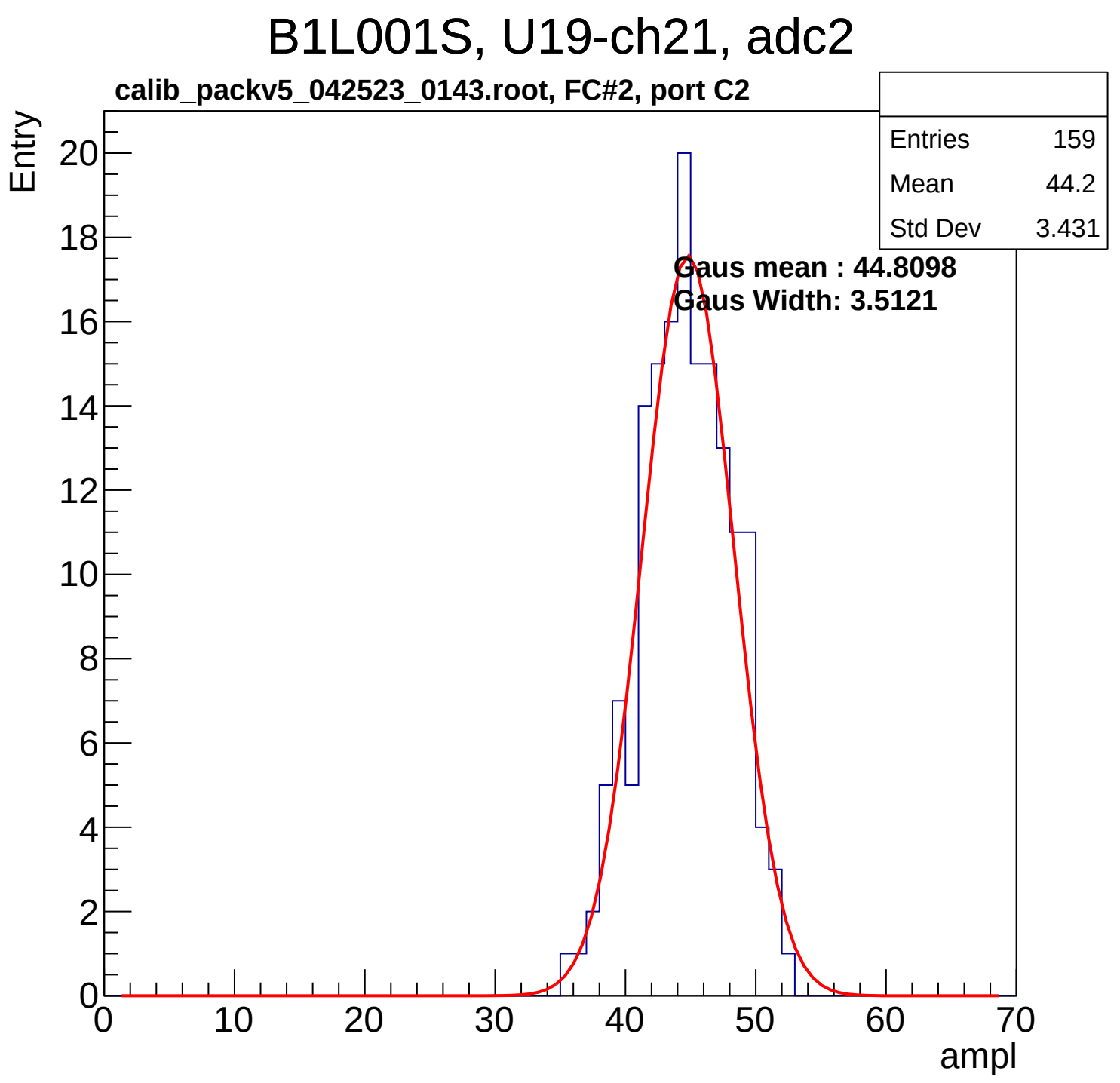
60
70


B1L001S, U19-ch21, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 159
Mean 44.2
Std Dev 3.431
Gaus mean : 44.8098
Gaus Width: 3.5121
Entry
ampl
0
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6
8
10
12
14
16
18
20
0
10
20
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60
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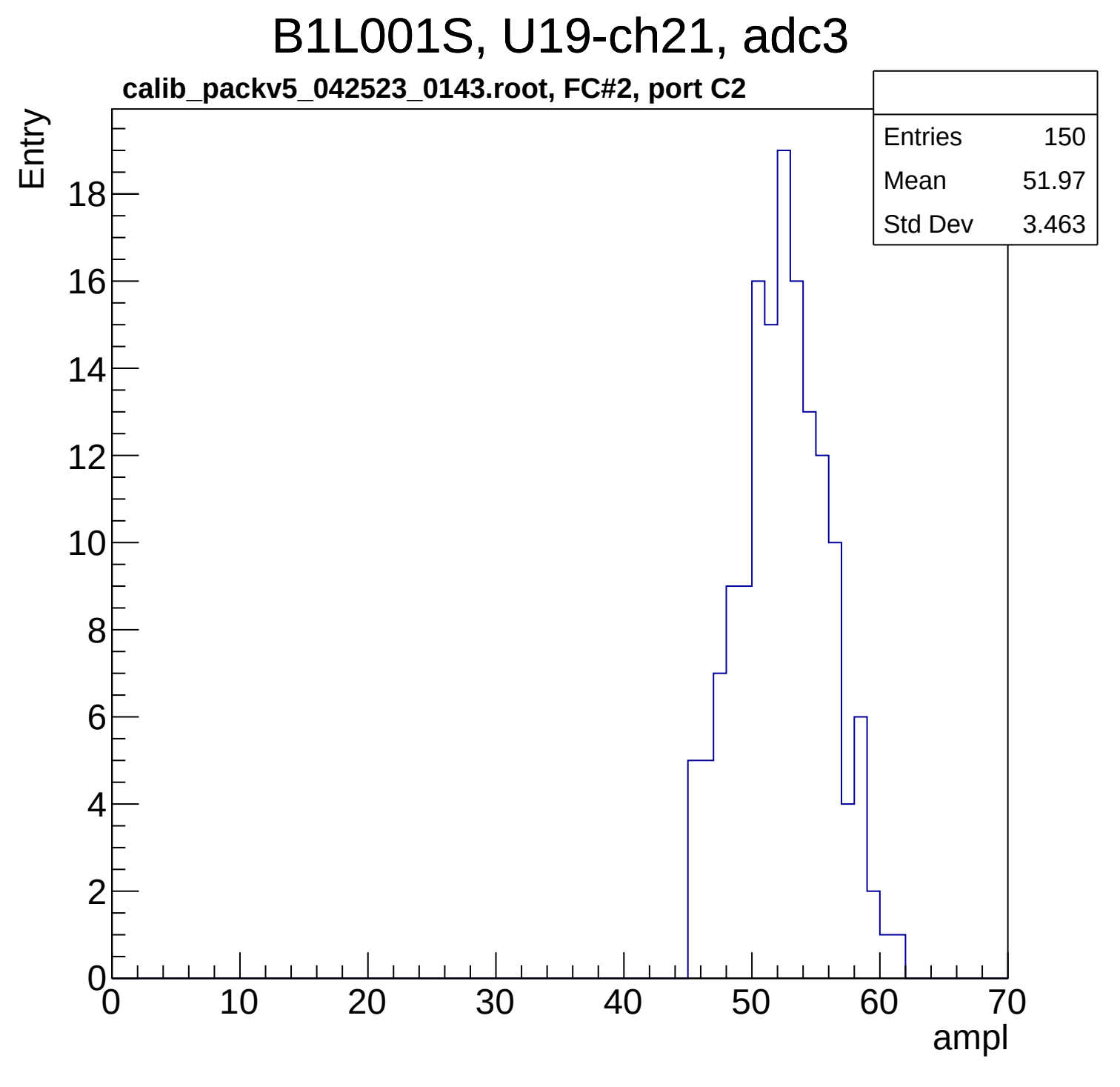
B1L001S, U19-ch21, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 150
Mean 51.97
Std Dev 3.463
Entry
ampl
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4
6
8
10
12
14
16
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0
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60
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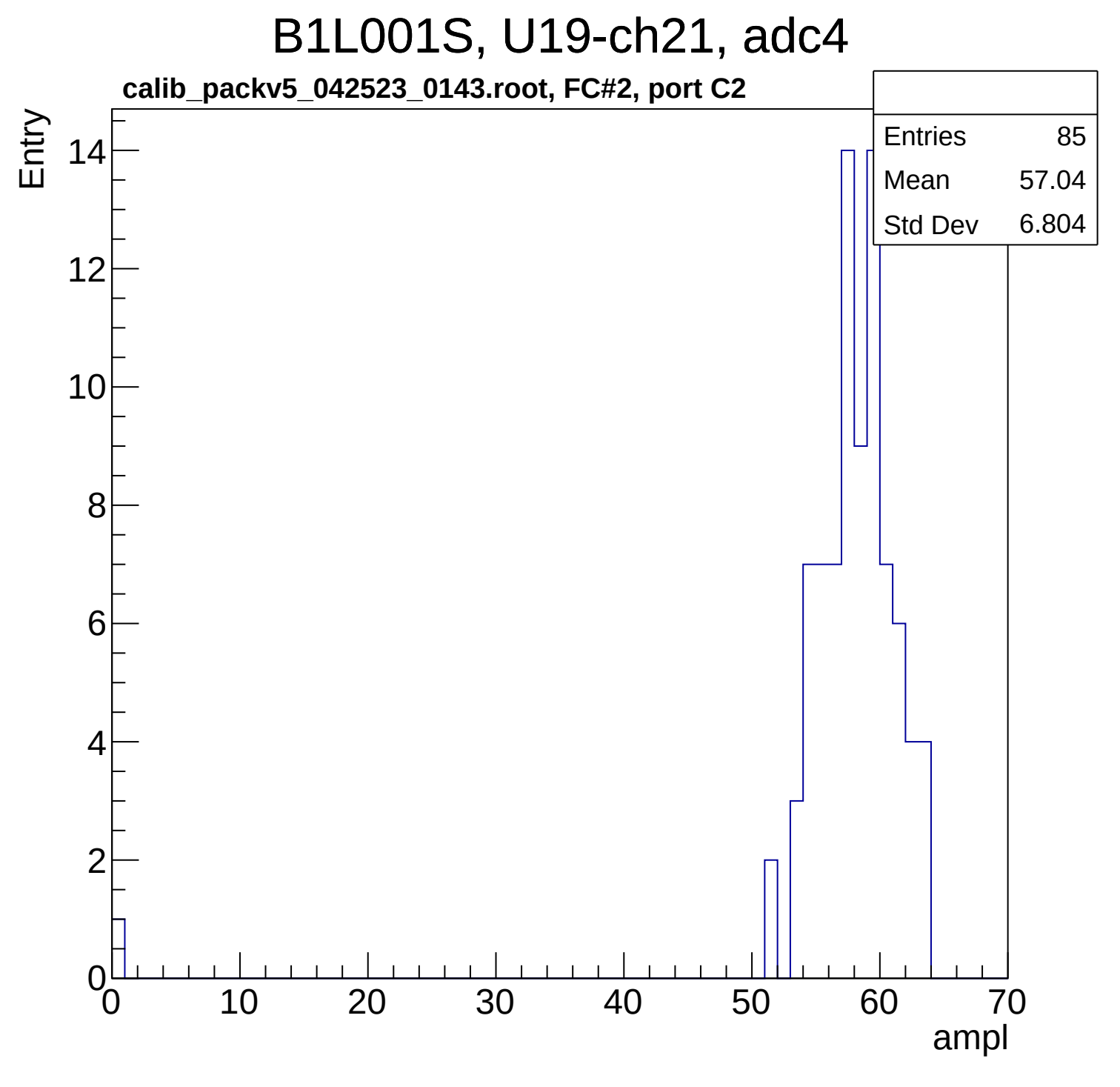
B1L001S, U19-ch21, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 85
Mean 57.04
Std Dev 6.804
Entry
ampl
0
2
4
6
8
10
12
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0
10
20
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60
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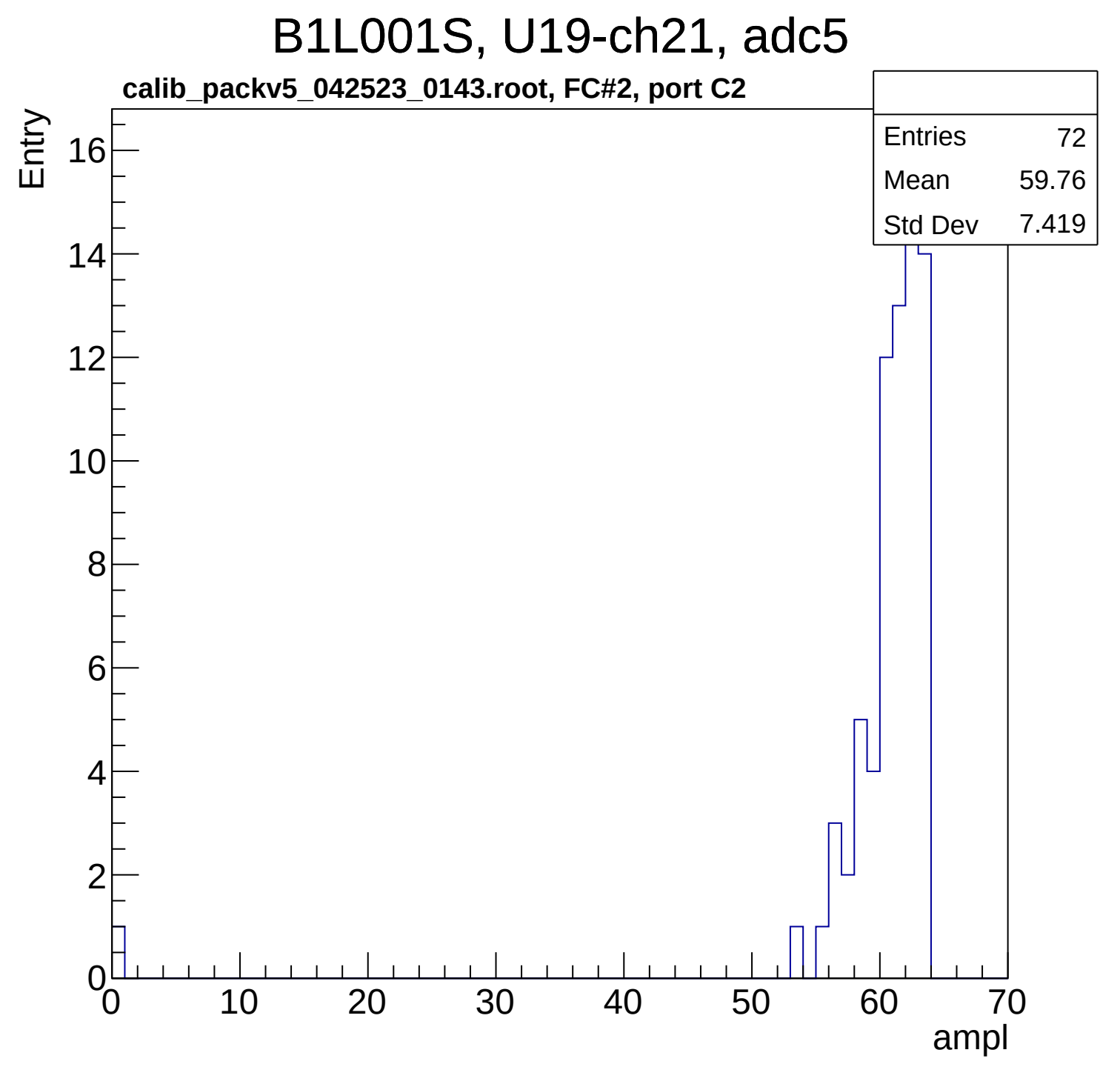
B1L001S, U19-ch21, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 72
Mean 59.76
Std Dev 7.419
Entry
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2
4
6
8
10
12
14
16
0
10
20
30
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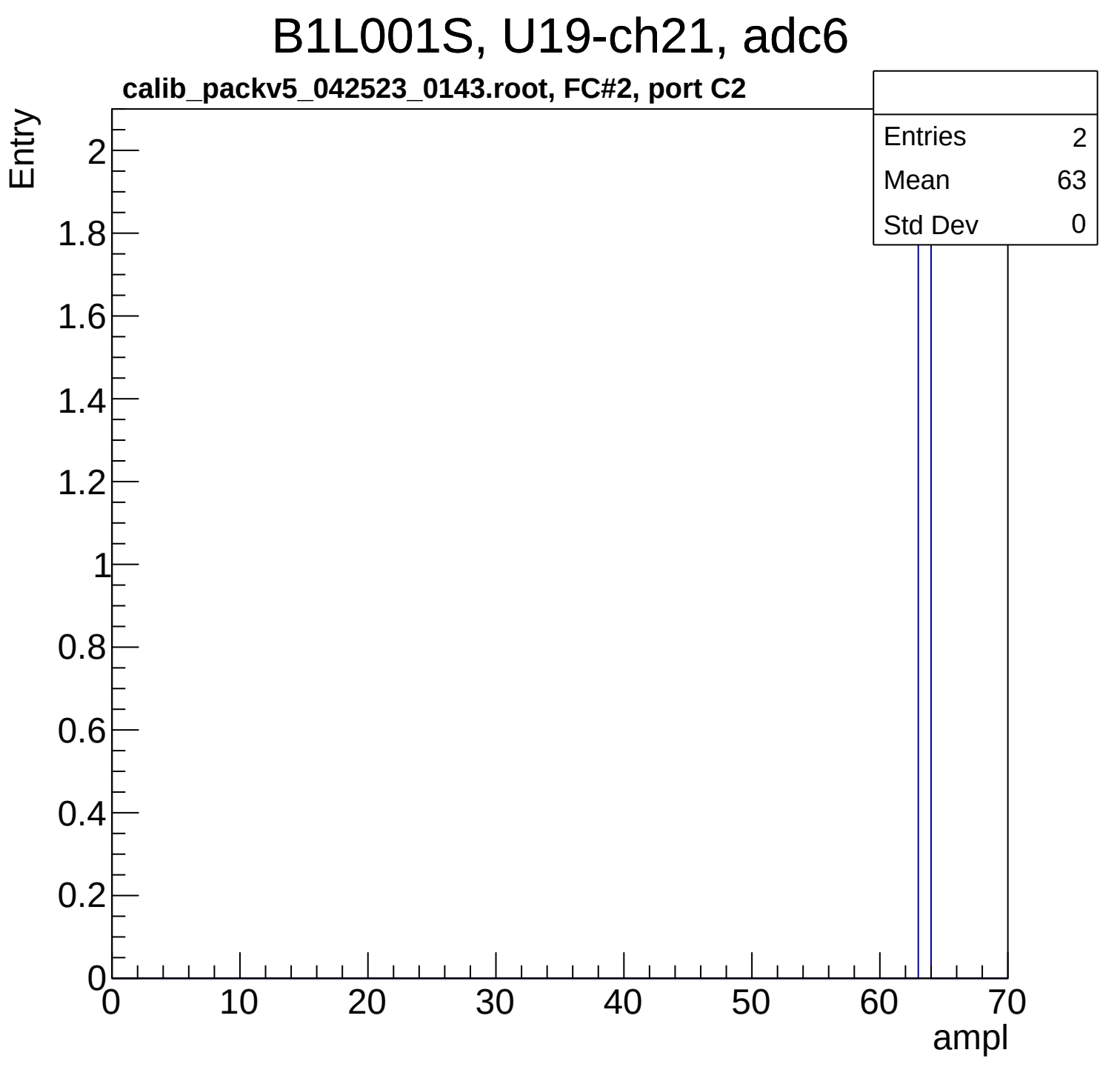
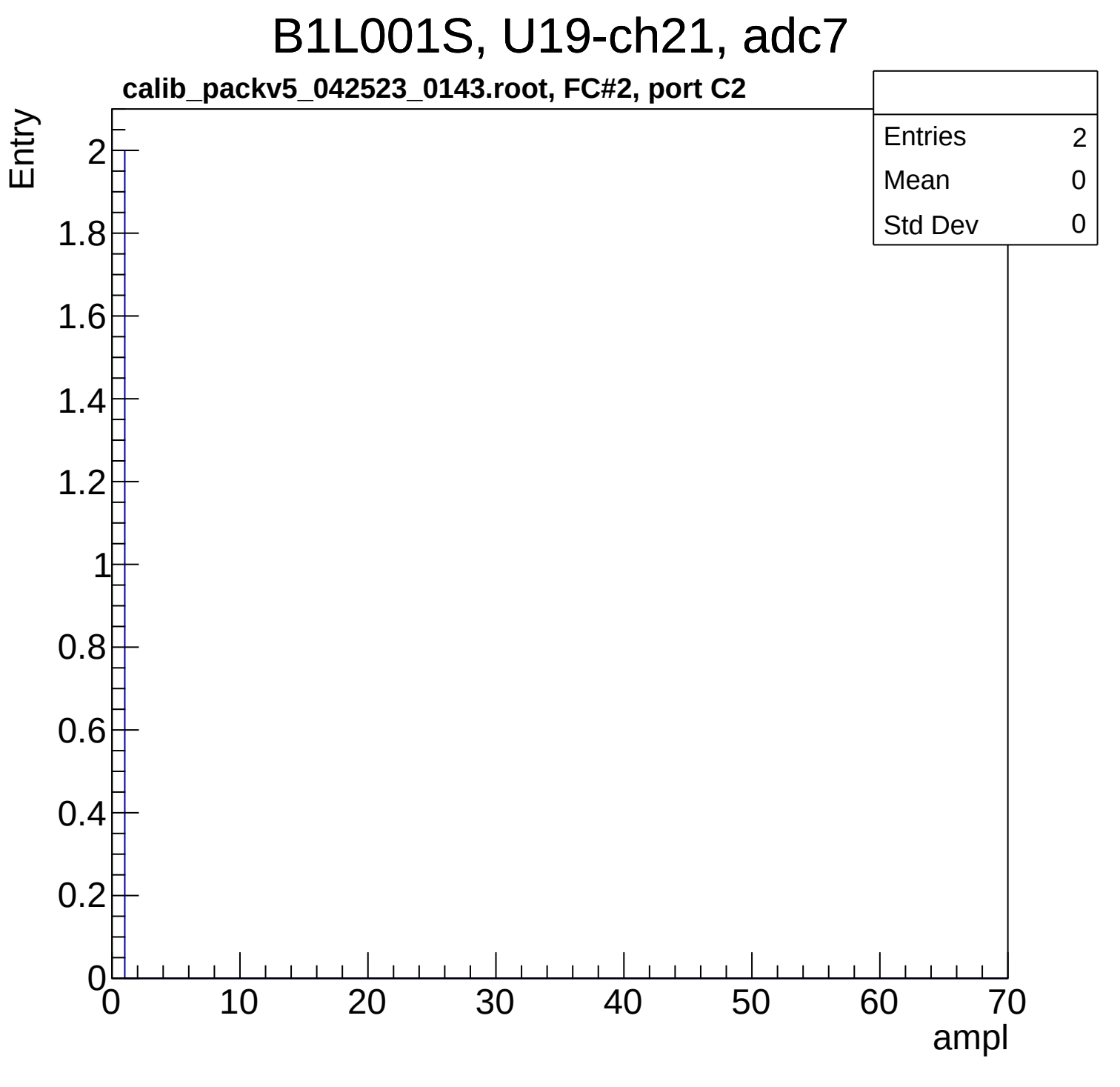
50
60
70
ampl


B1L001S, U19-ch21, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 63
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L001S, U19-ch21, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 0
Std Dev 0
Entry
2
1.8
1.6
1.4
1.2
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0.8
0.6
0.4
0.2
0
0
10
20
30
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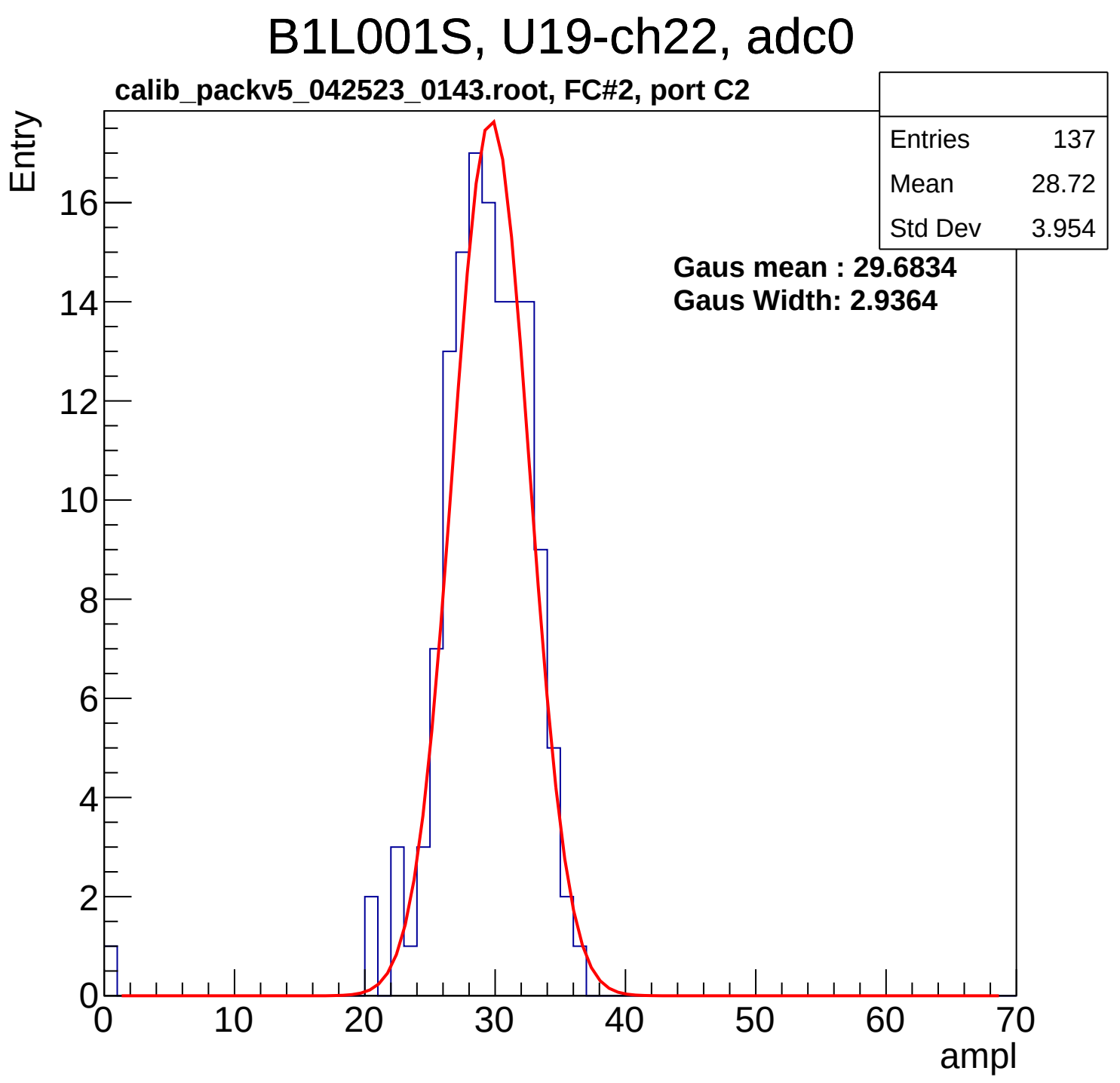
50
60
70
ampl


B1L001S, U19-ch22, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 137
Mean 28.72
Std Dev 3.954
Gaus mean : 29.6834
Gaus Width: 2.9364
Entry
ampl
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2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
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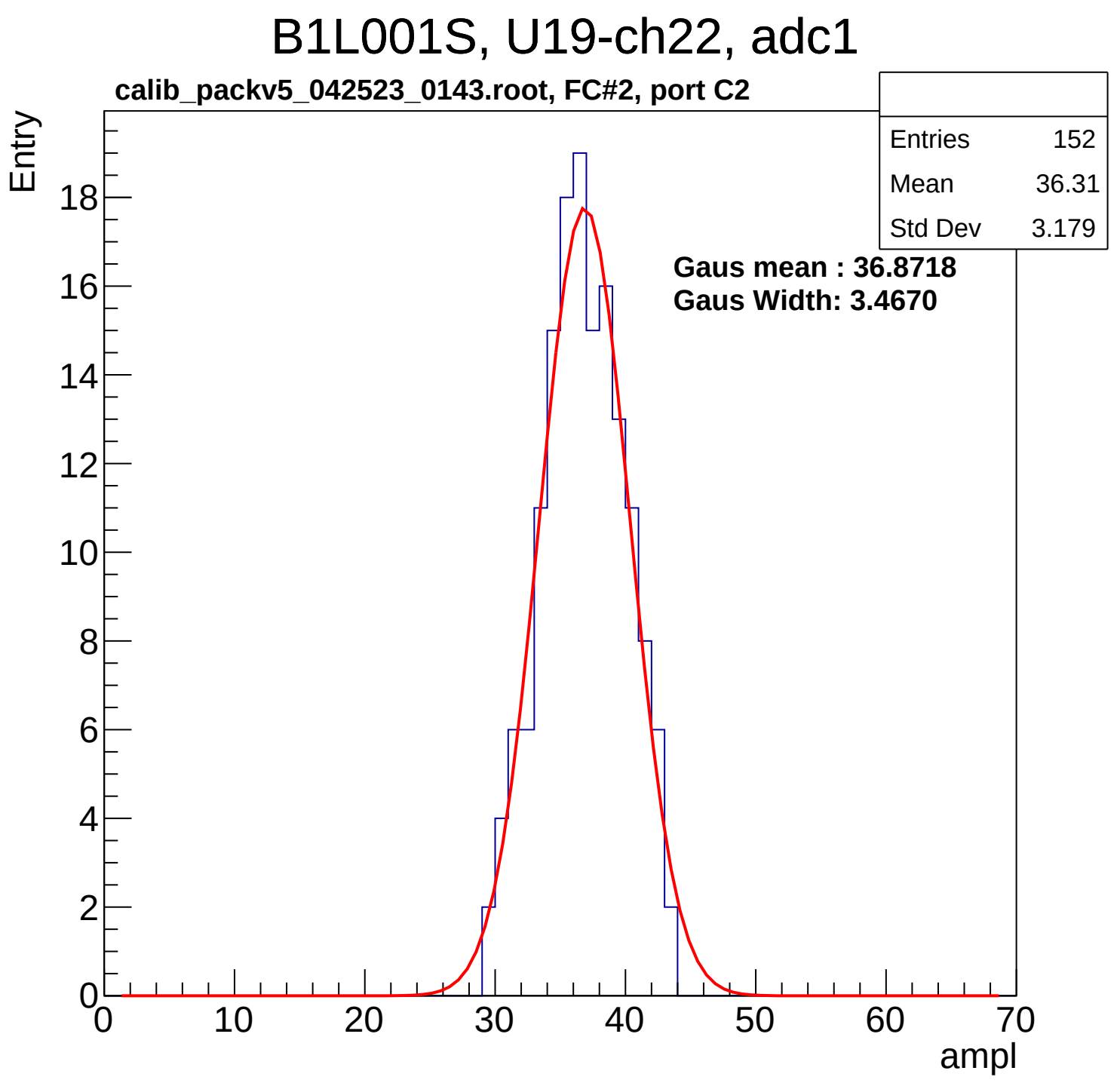
B1L001S, U19-ch22, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 152
Mean 36.31
Std Dev 3.179
Gaus mean : 36.8718
Gaus Width: 3.4670
Entry
ampl
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2
4
6
8
10
12
14
16
18
0
10
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30
40
50
60
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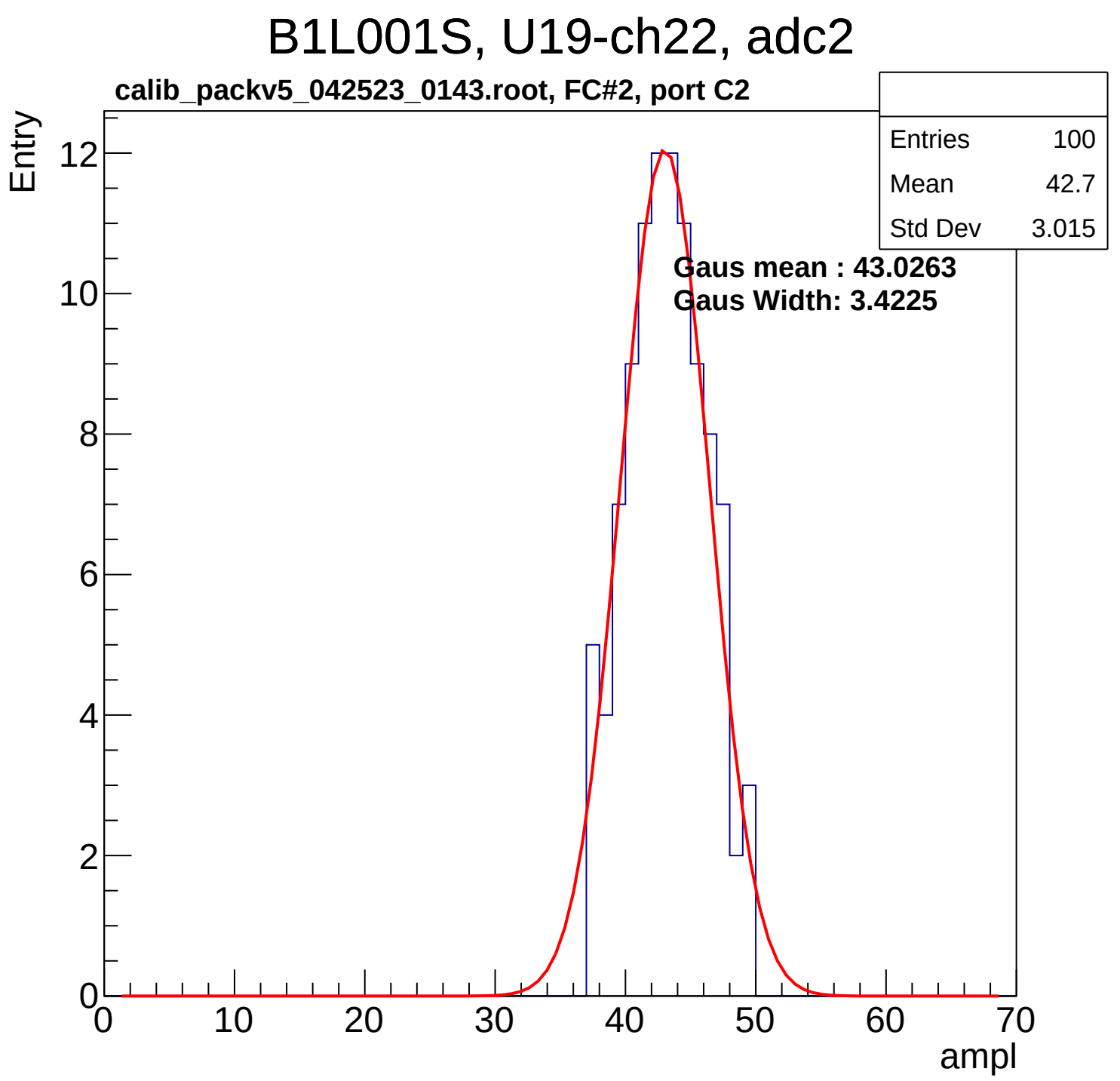
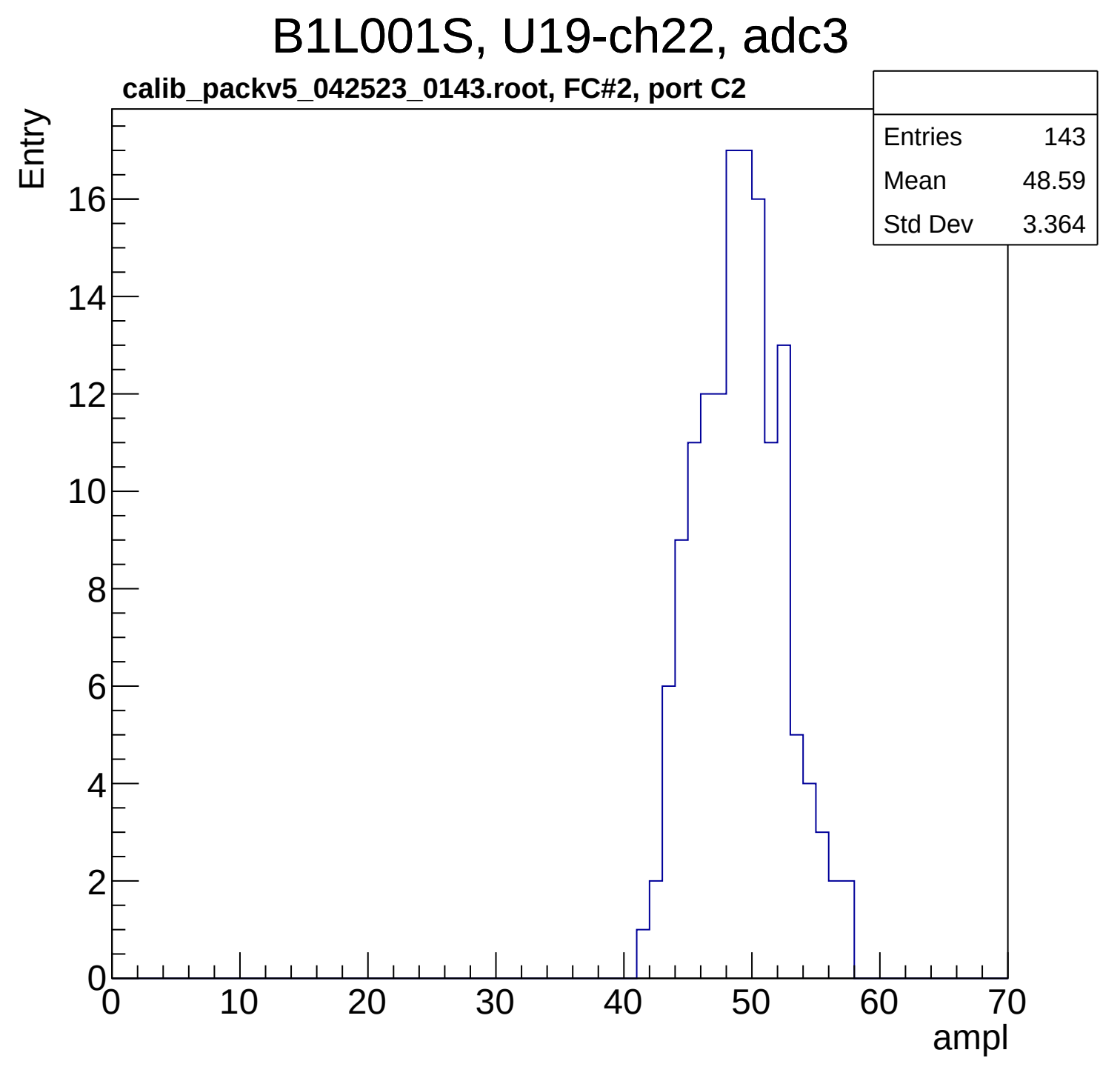
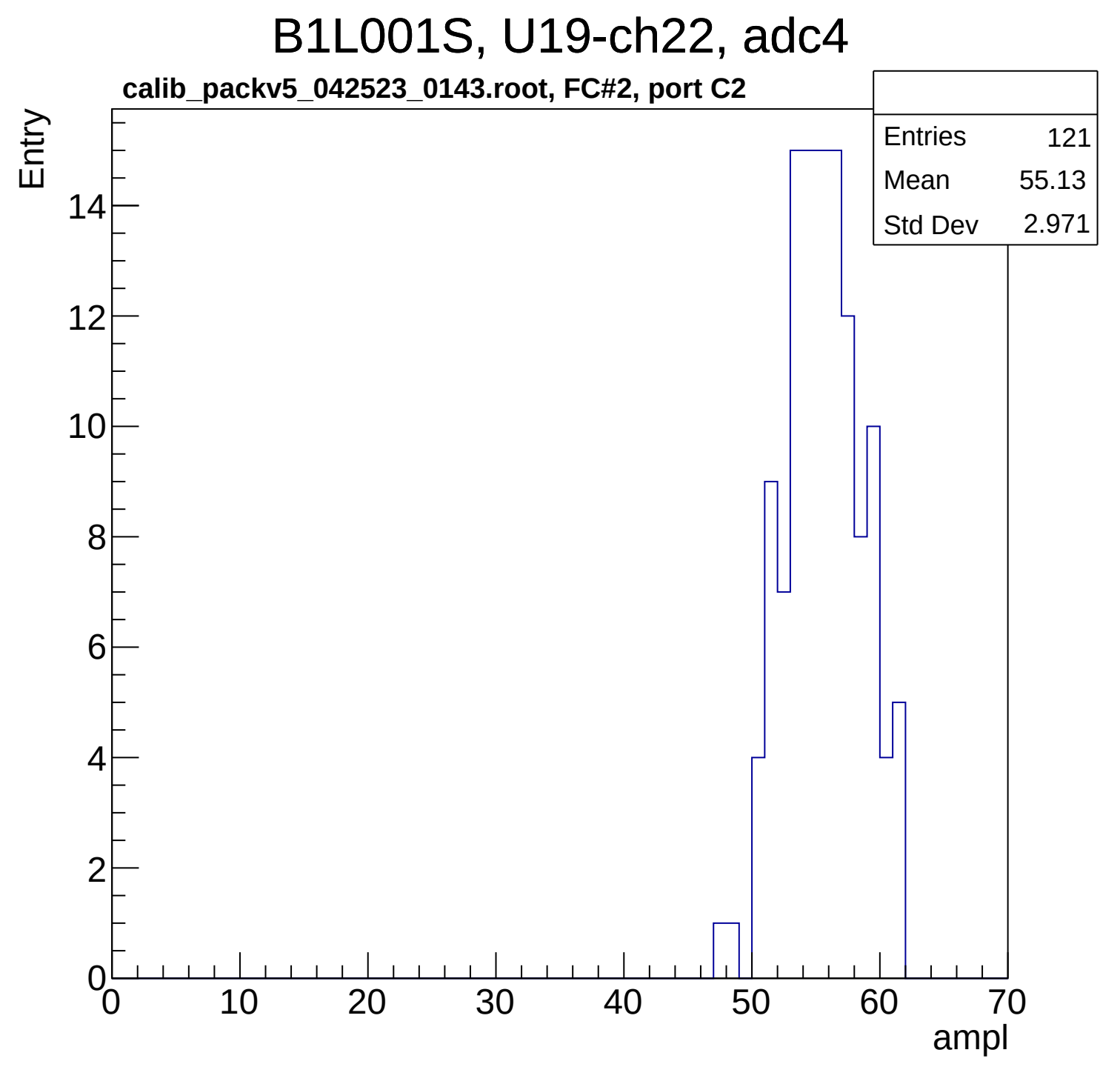

B1L001S, U19-ch22, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 100
Mean 42.7
Std Dev 3.015
Gaus mean : 43.0263
Gaus Width: 3.4225
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70


B1L001S, U19-ch22, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 143
Mean 48.59
Std Dev 3.364
Entry
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch22, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 121
Mean 55.13
Std Dev 2.971
Entry
ampl
0
2
4
6
8
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12
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0
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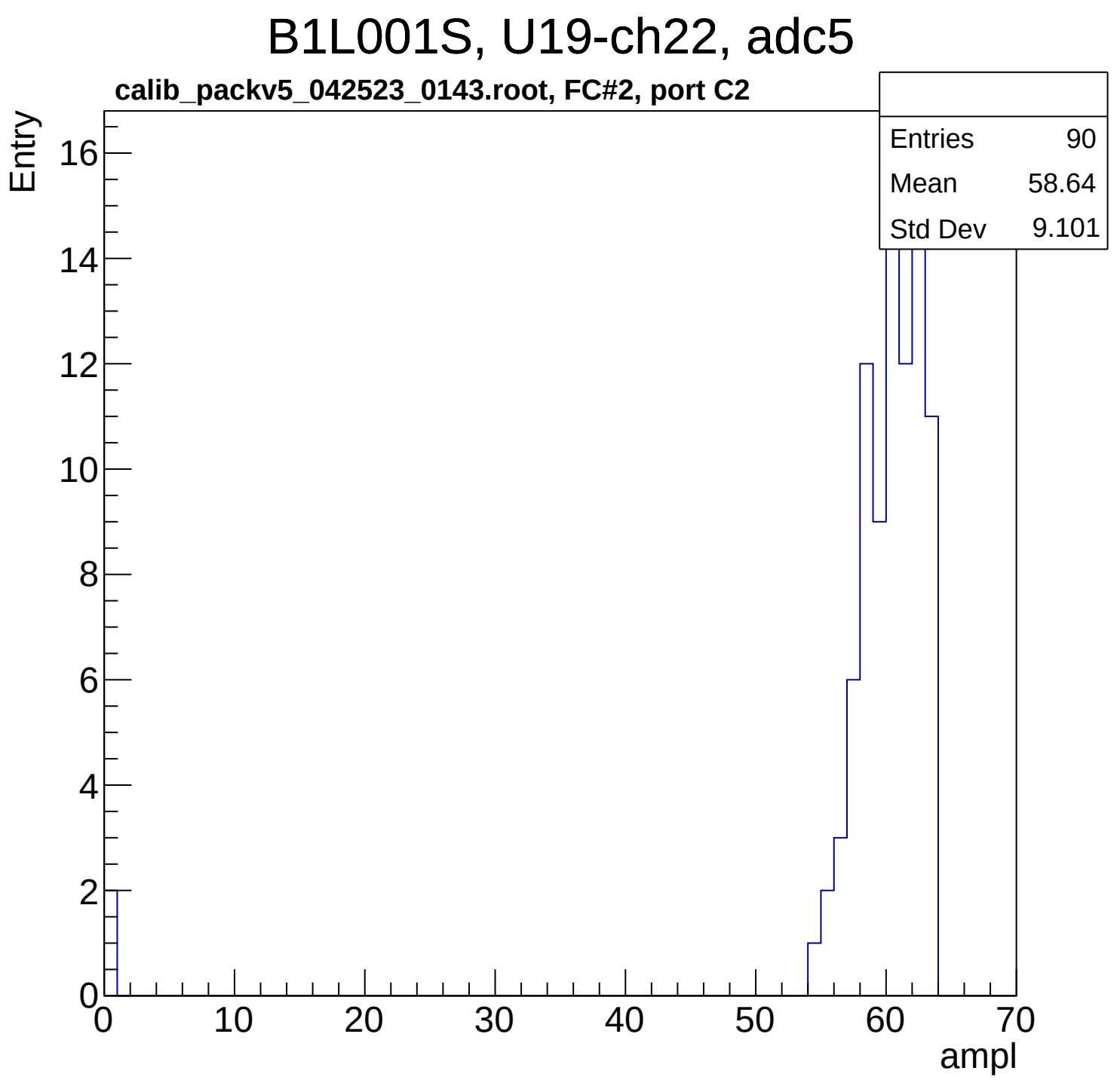
60
70


B1L001S, U19-ch22, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 90
Mean 58.64
Std Dev 9.101
Entry
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4
6
8
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50
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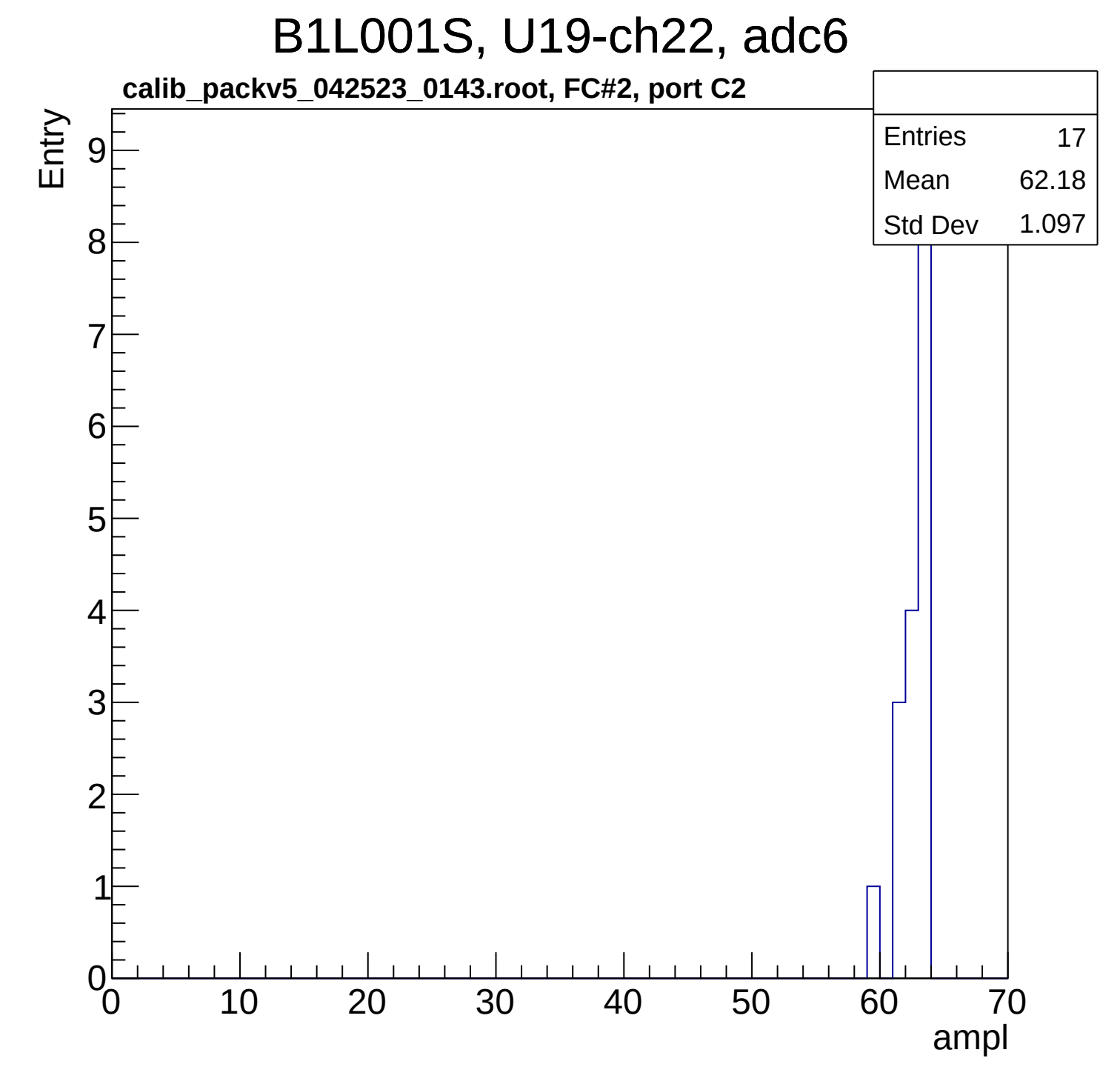
70
ampl


B1L001S, U19-ch22, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 17
Mean 62.18
Std Dev 1.097
Entry
ampl
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3
4
5
6
7
8
9
0
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40
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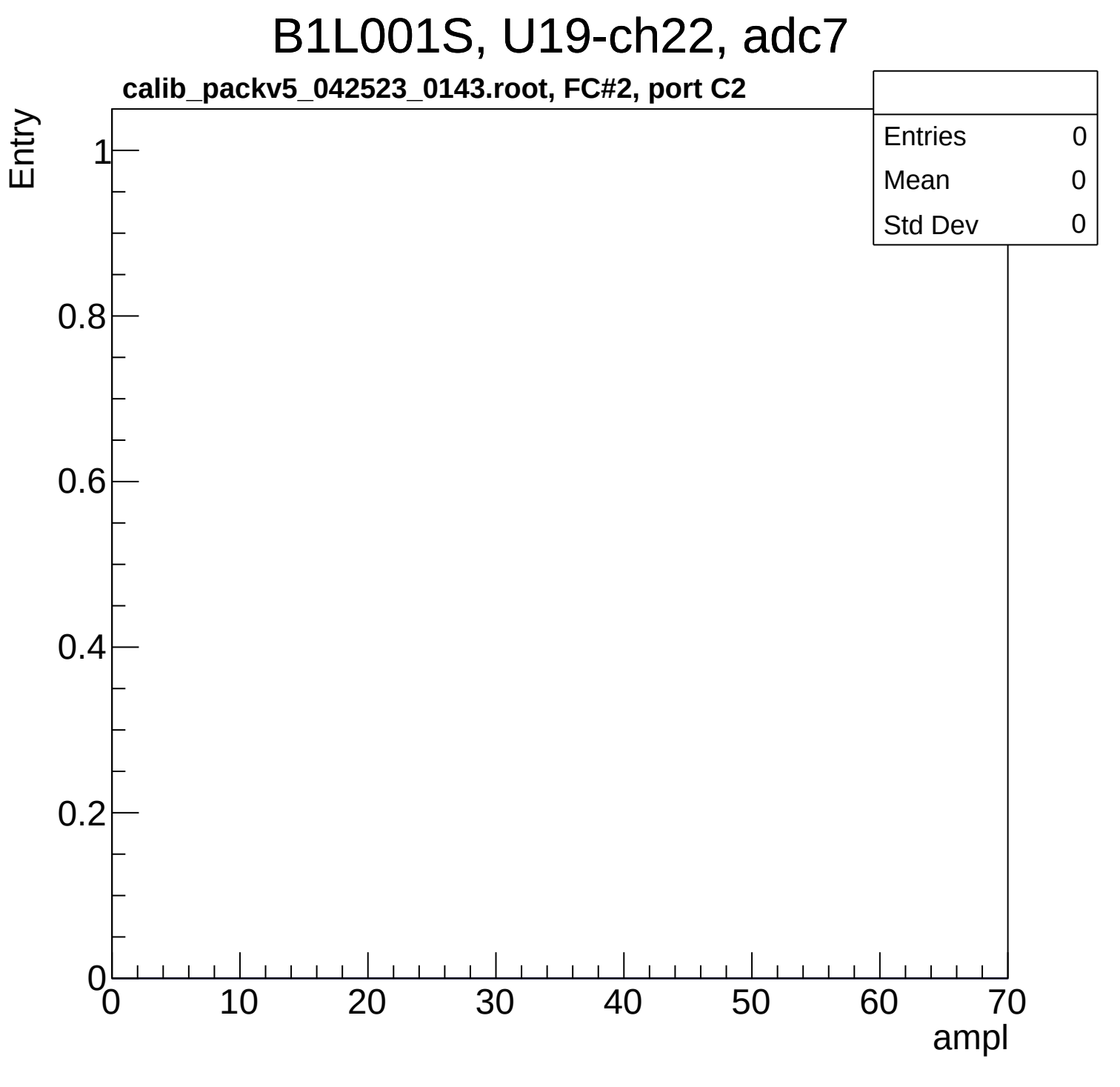
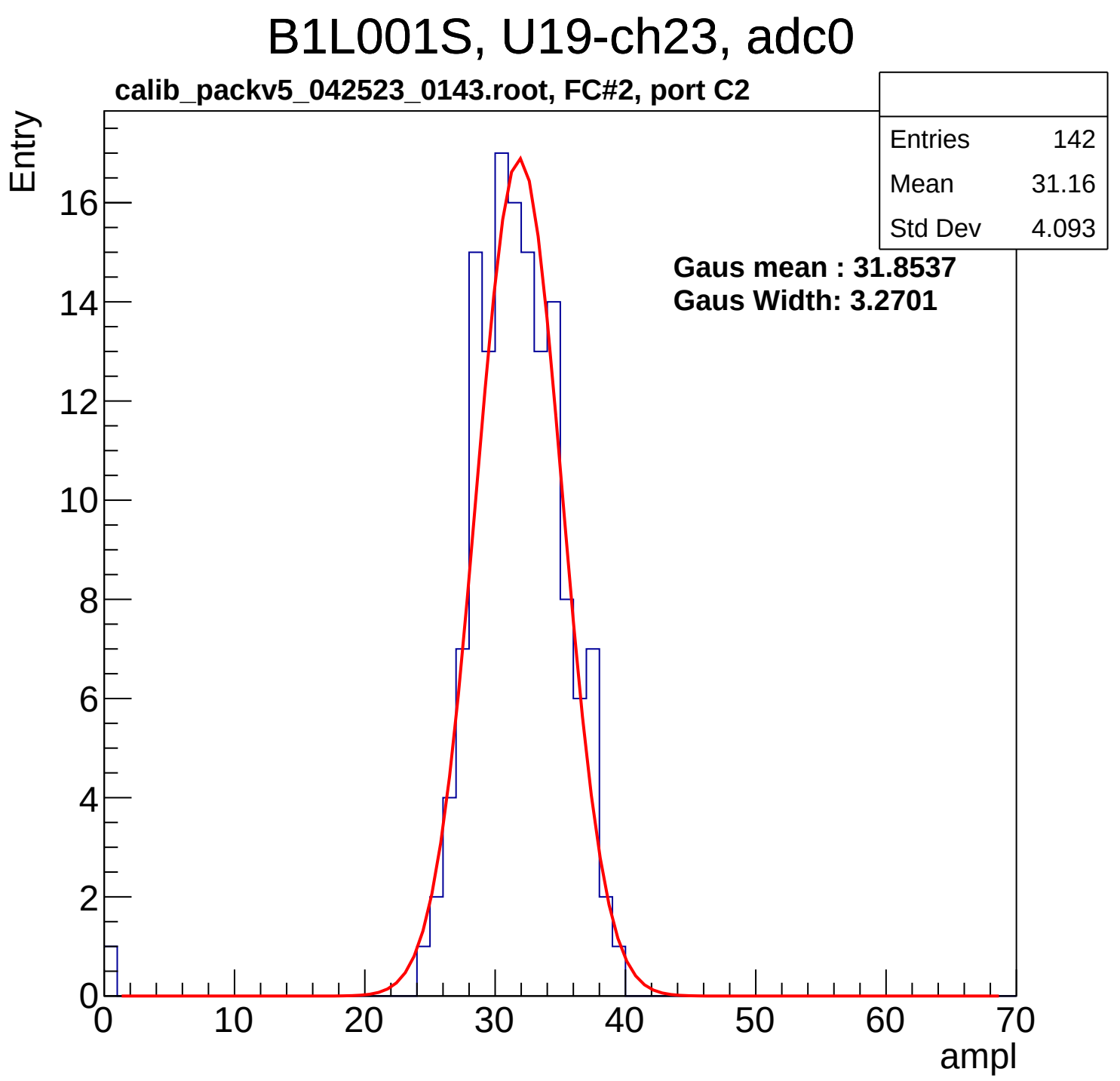
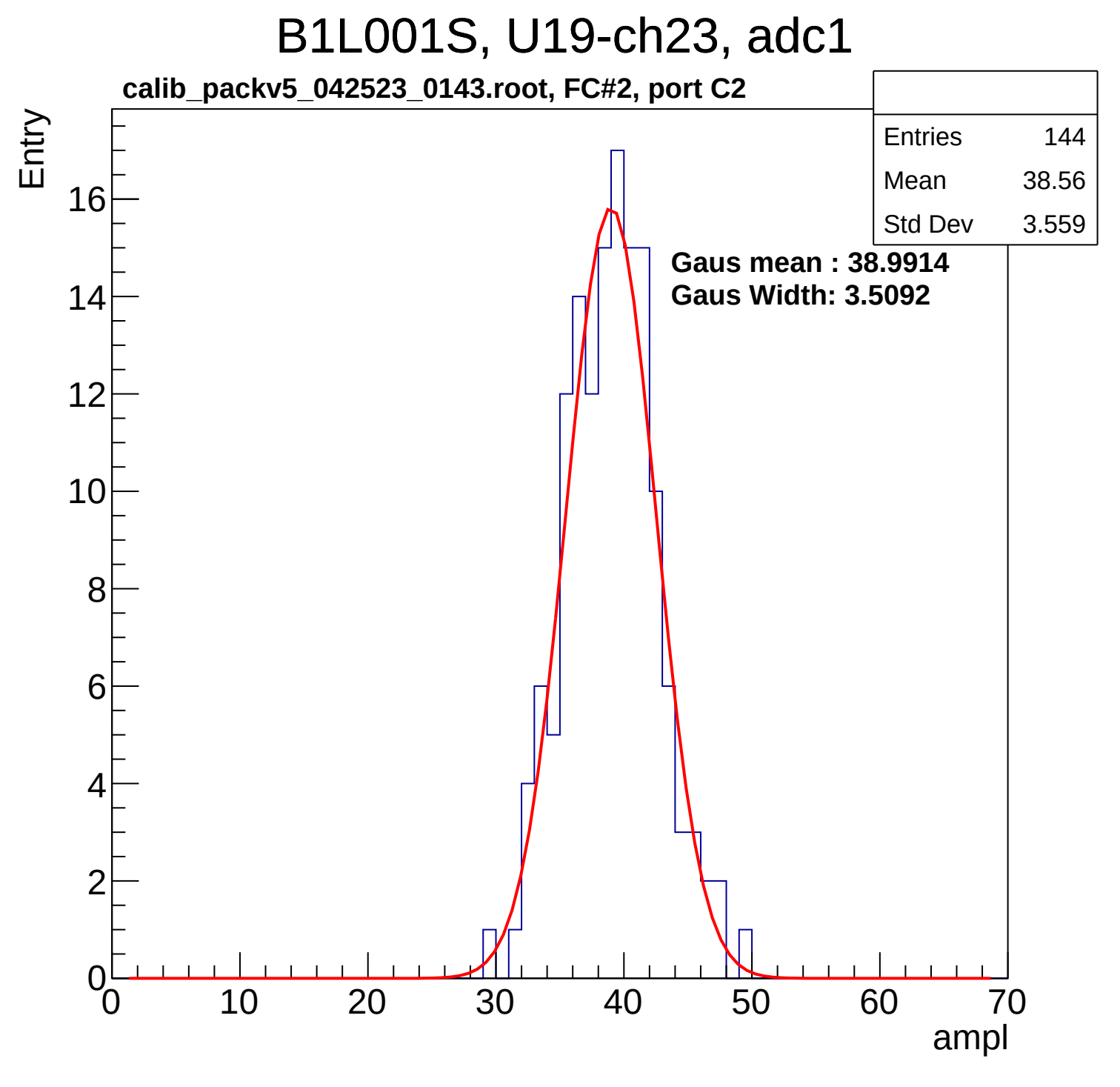
60
70


B1L001S, U19-ch22, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch23, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 142
Mean 31.16
Std Dev 4.093
Gaus mean : 31.8537
Gaus Width: 3.2701
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70


B1L001S, U19-ch23, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 144
Mean 38.56
Std Dev 3.559
Gaus mean : 38.9914
Gaus Width: 3.5092
Entry
ampl
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2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
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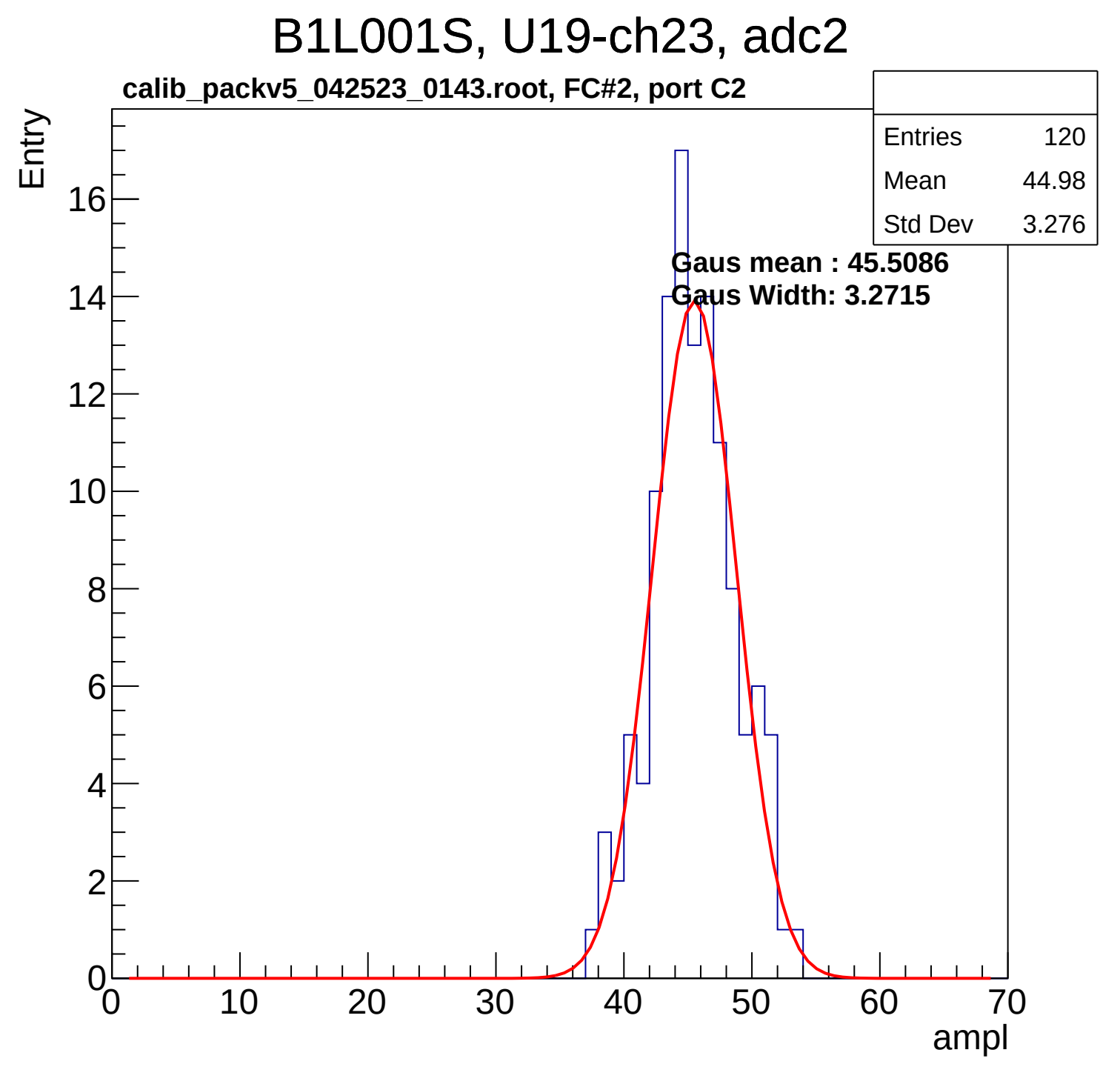
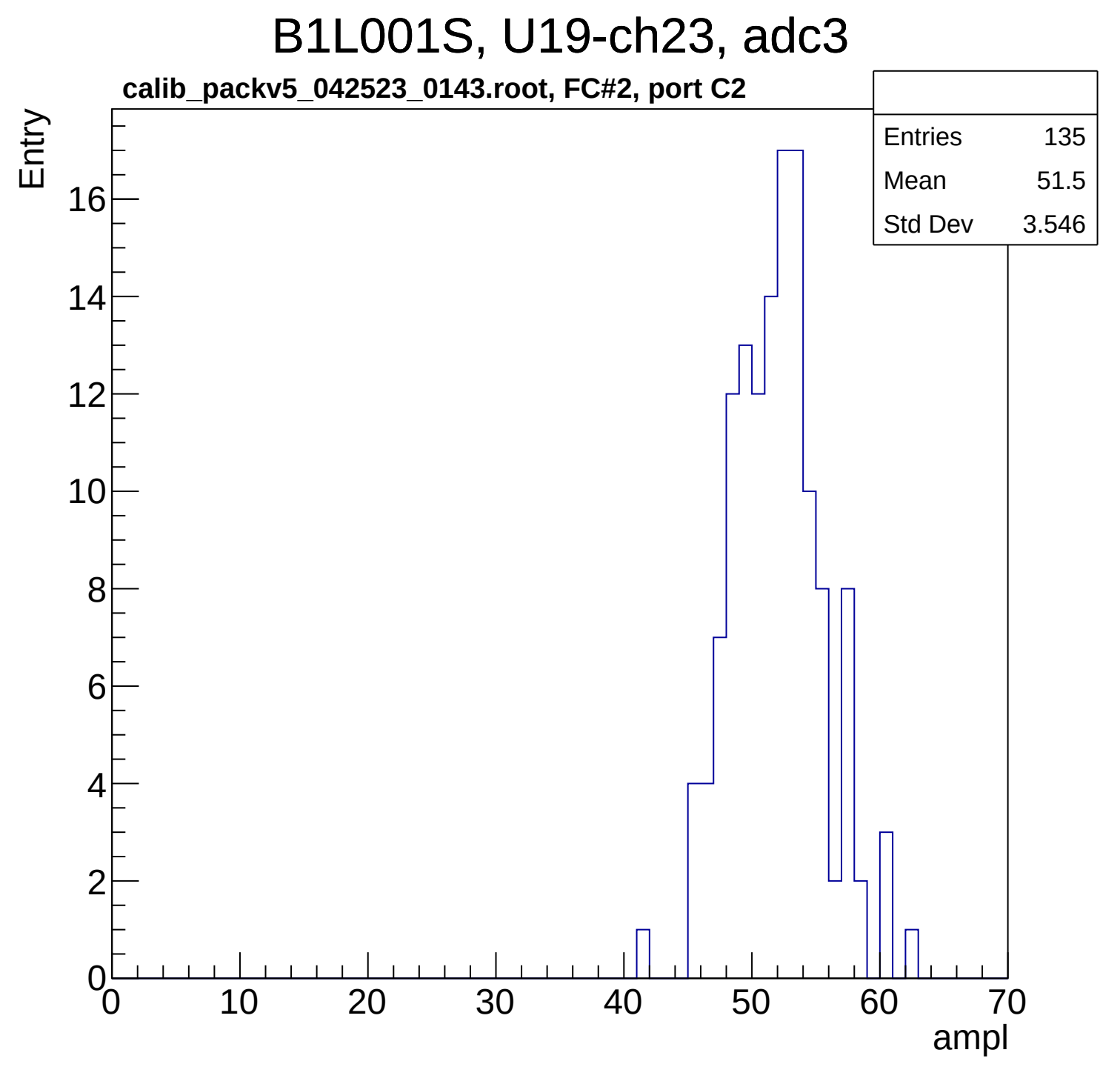
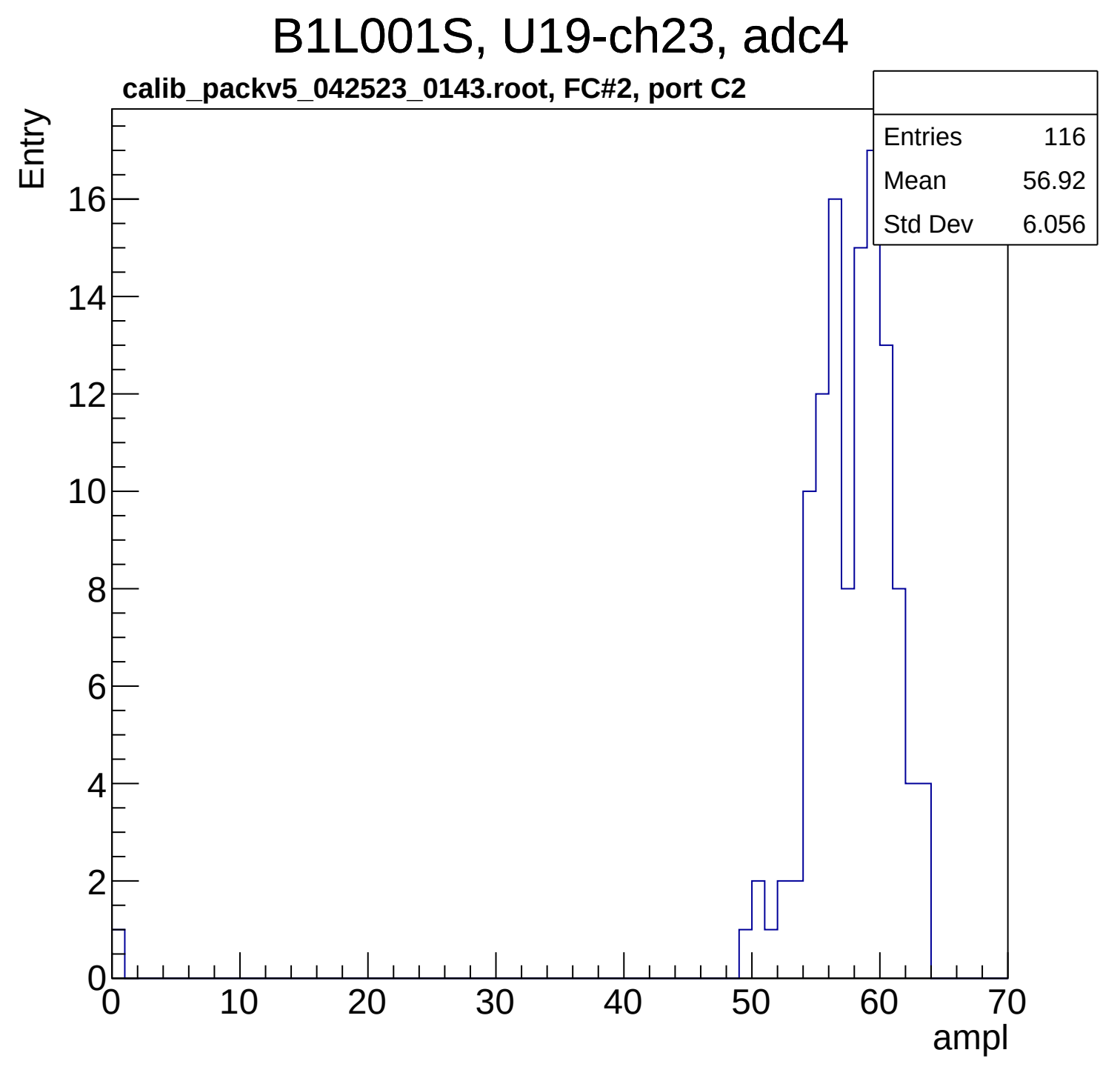

B1L001S, U19-ch23, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 120
Mean 44.98
Std Dev 3.276
Gaus mean : 45.5086
Gaus Width: 3.2715
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70


B1L001S, U19-ch23, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 135
Mean 51.5
Std Dev 3.546
Entry
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch23, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 116
Mean 56.92
Std Dev 6.056
Entry
ampl
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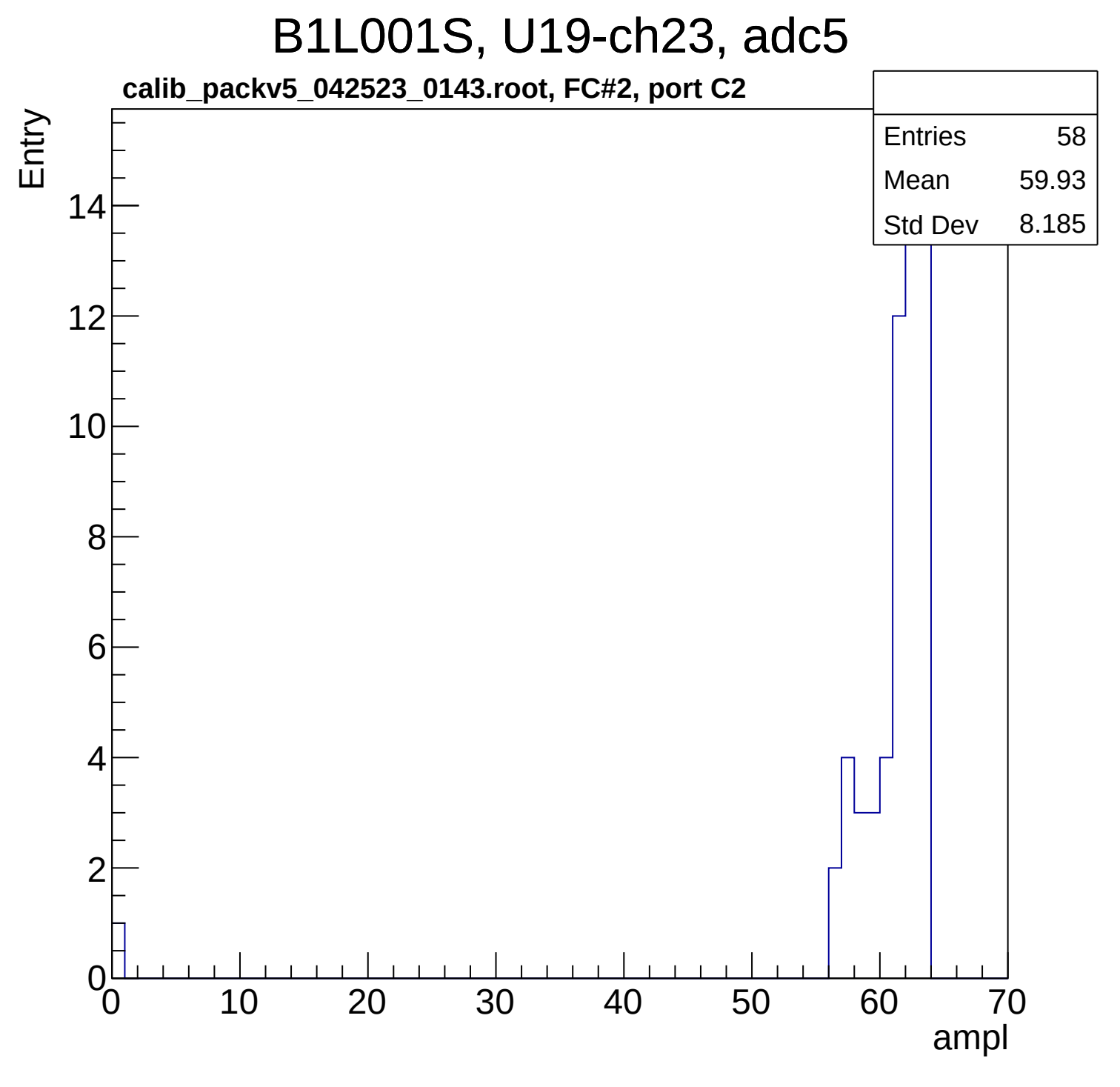
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70


B1L001S, U19-ch23, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 58
Mean 59.93
Std Dev 8.185
Entry
ampl
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2
4
6
8
10
12
14
0
10
20
30
40
50
60
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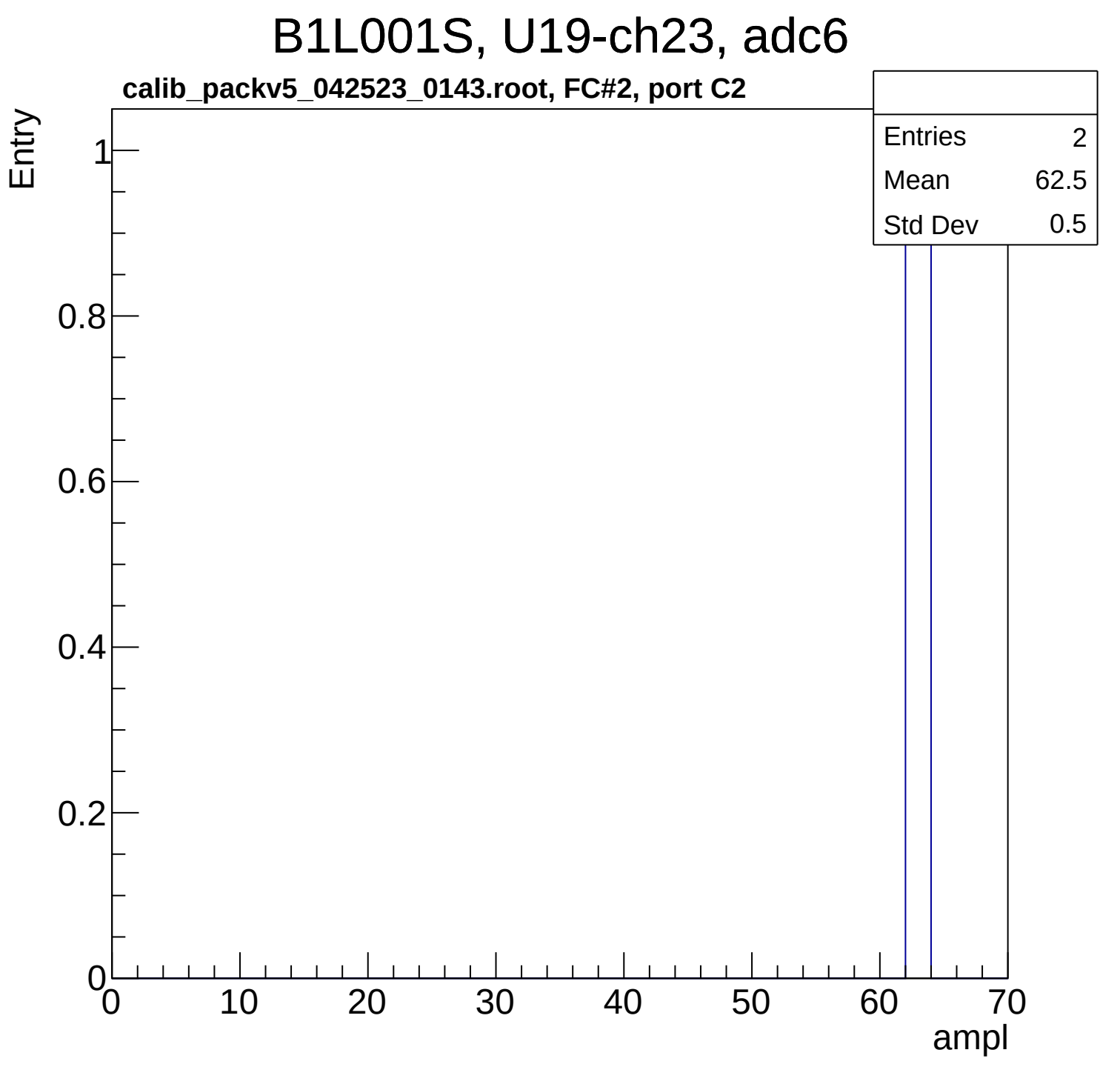
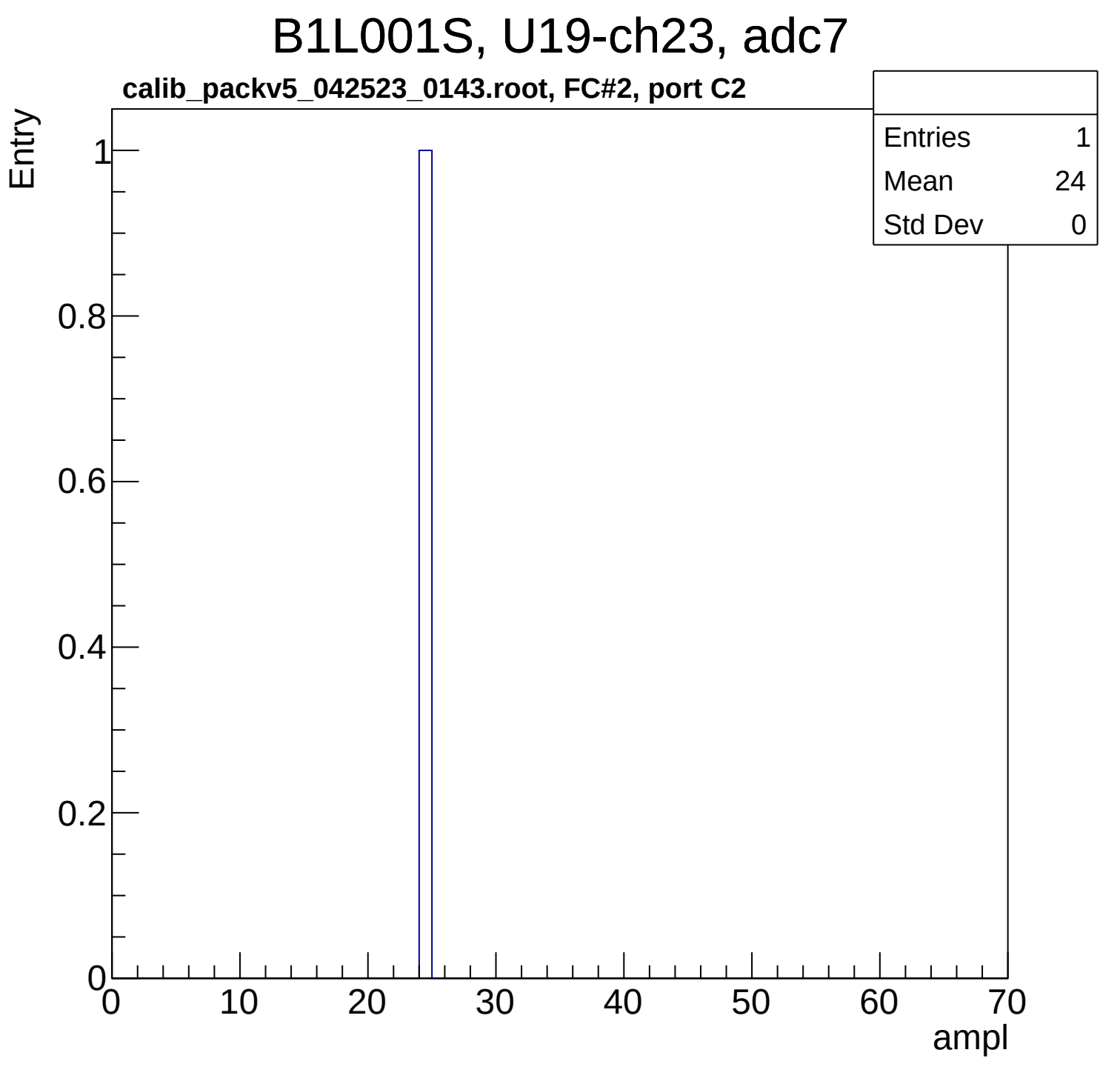

B1L001S, U19-ch23, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 62.5
Std Dev 0.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch23, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 24
Std Dev 0
Entry
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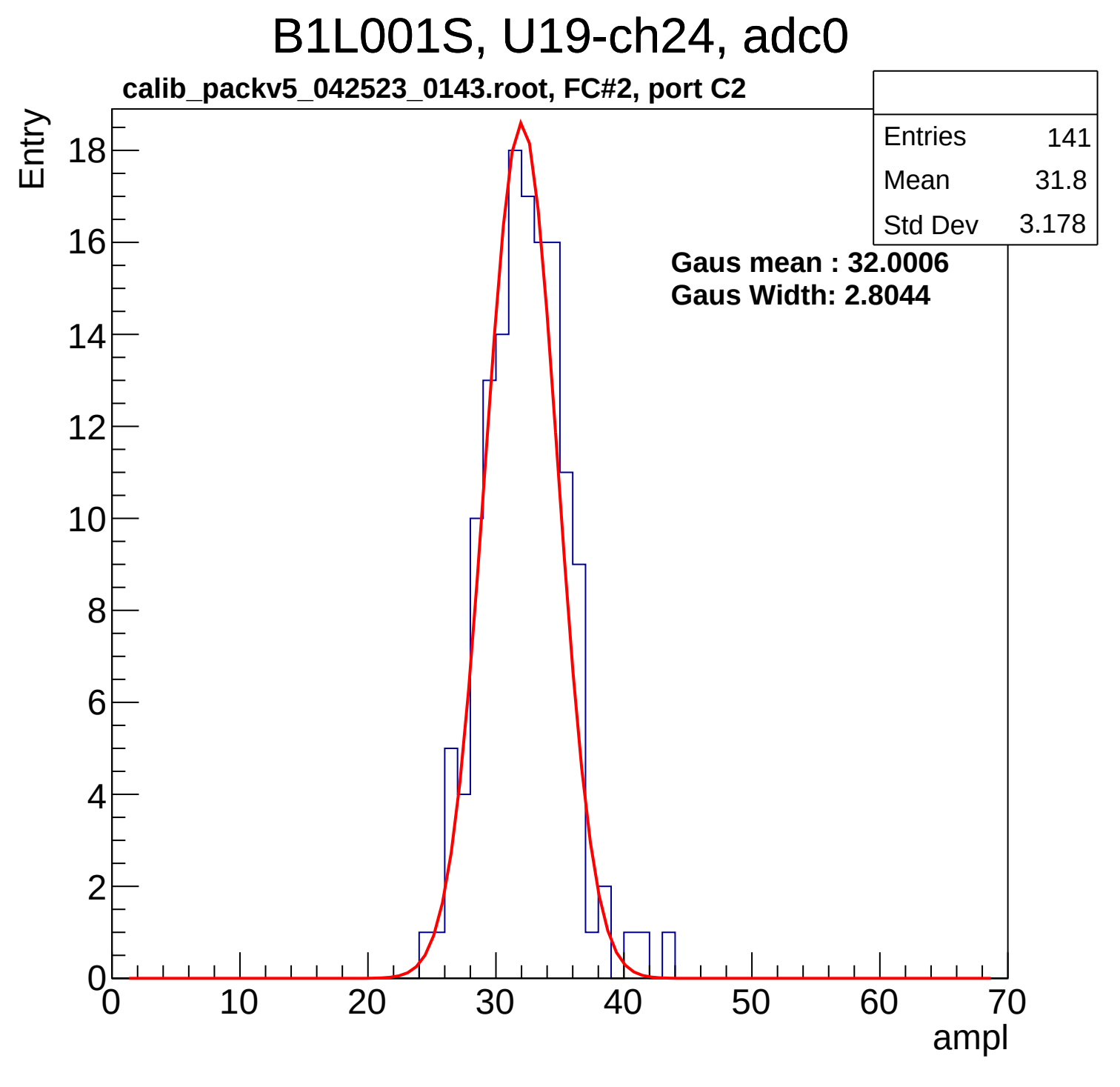
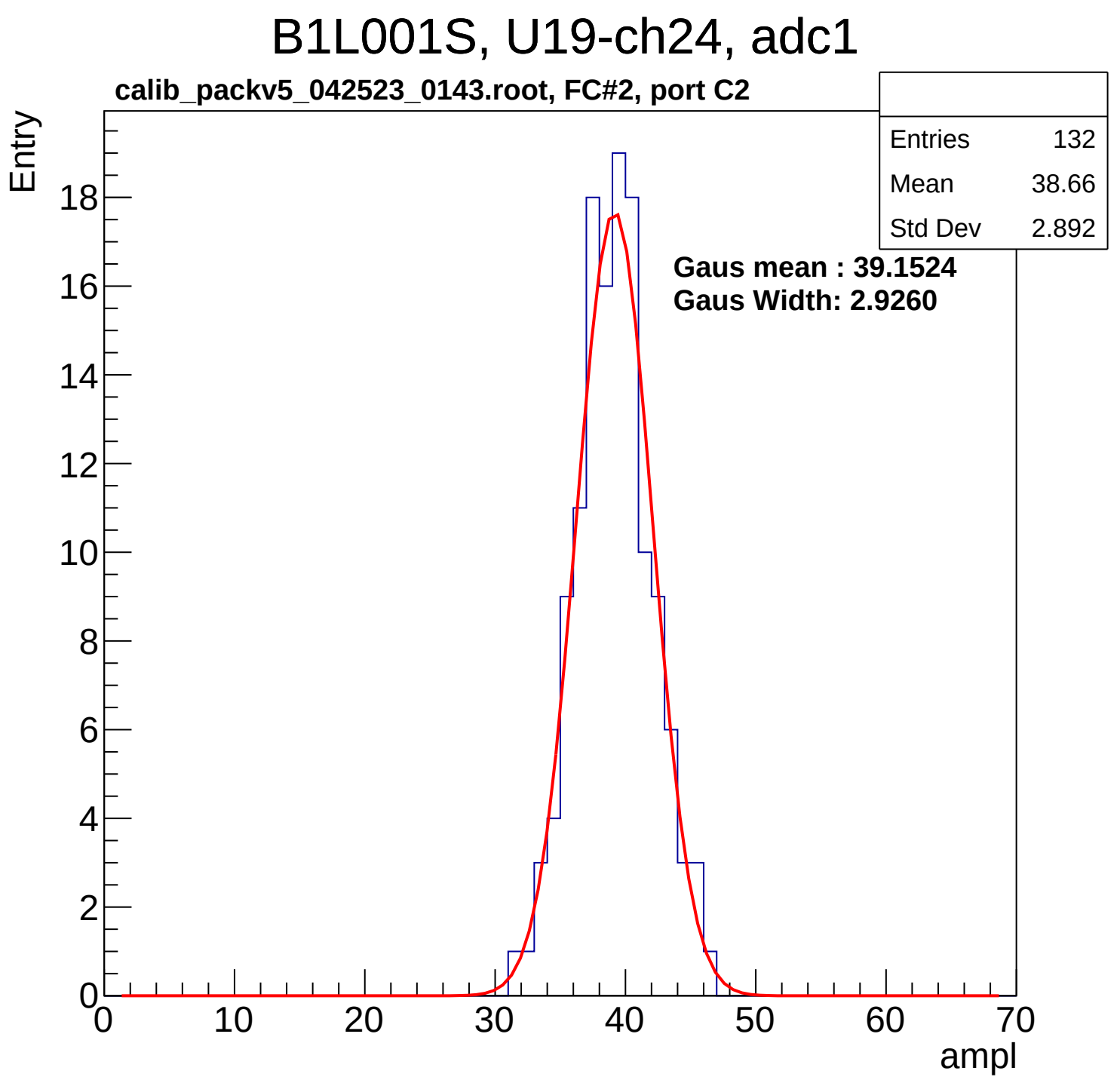
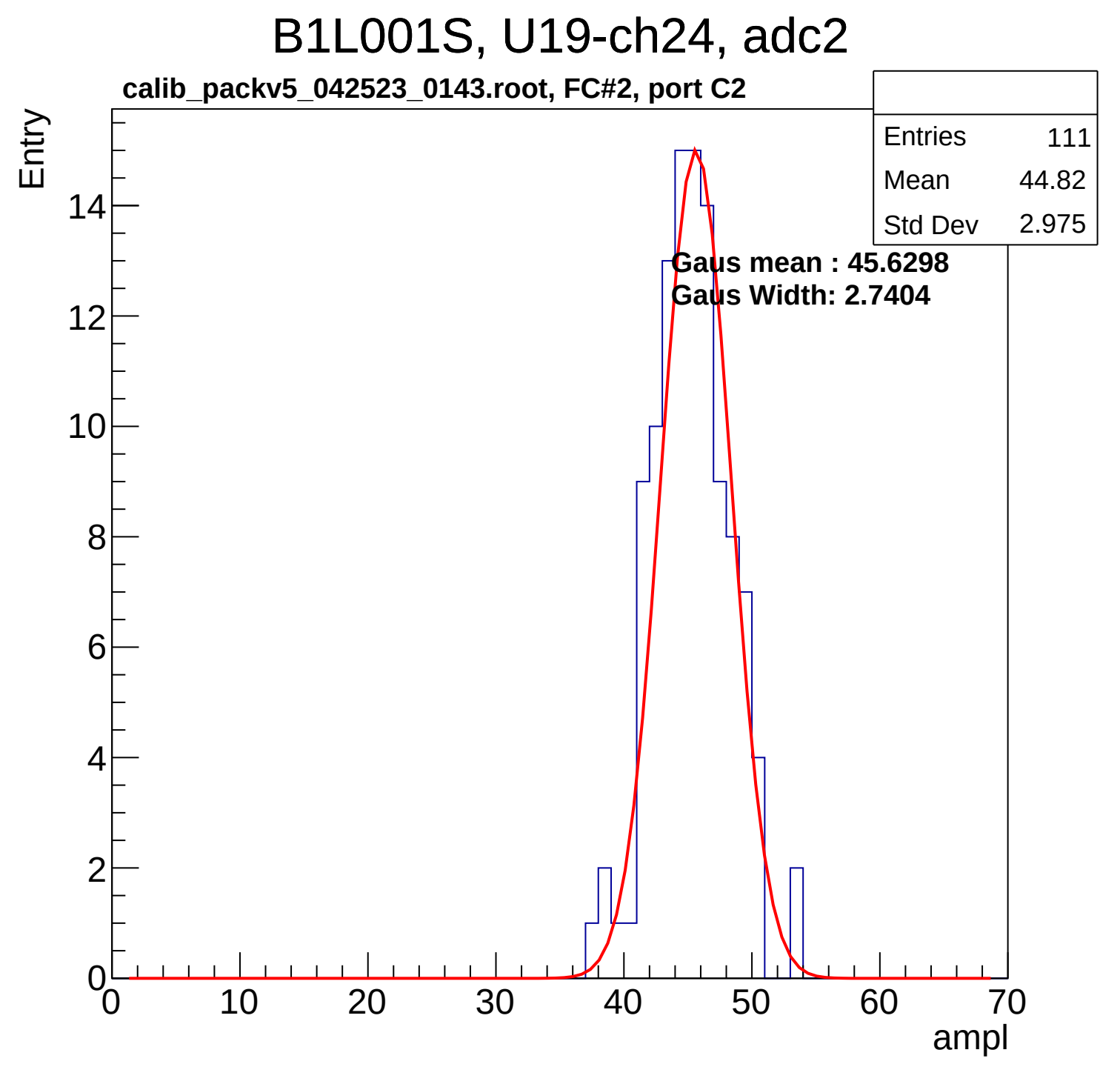
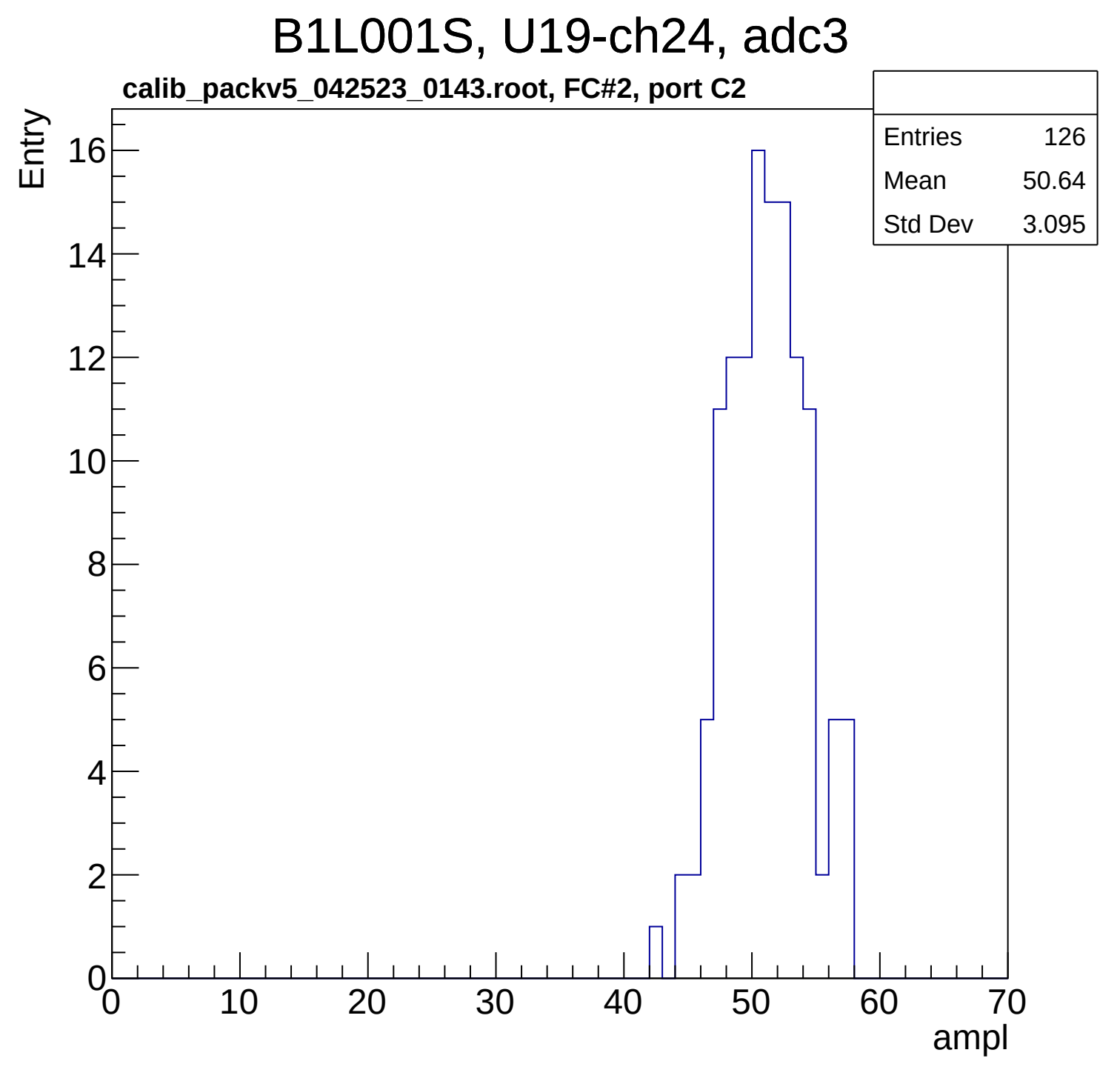
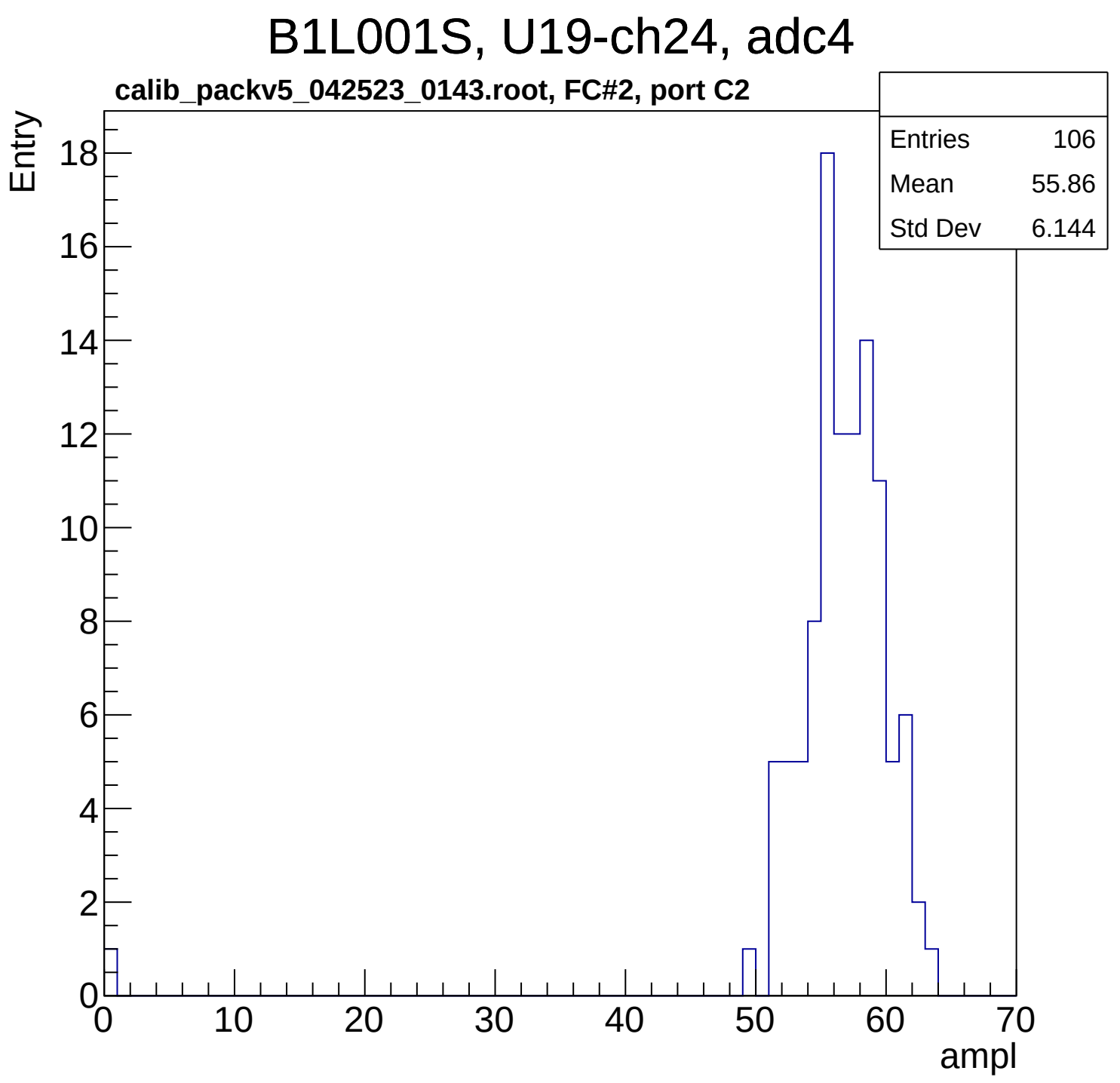
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

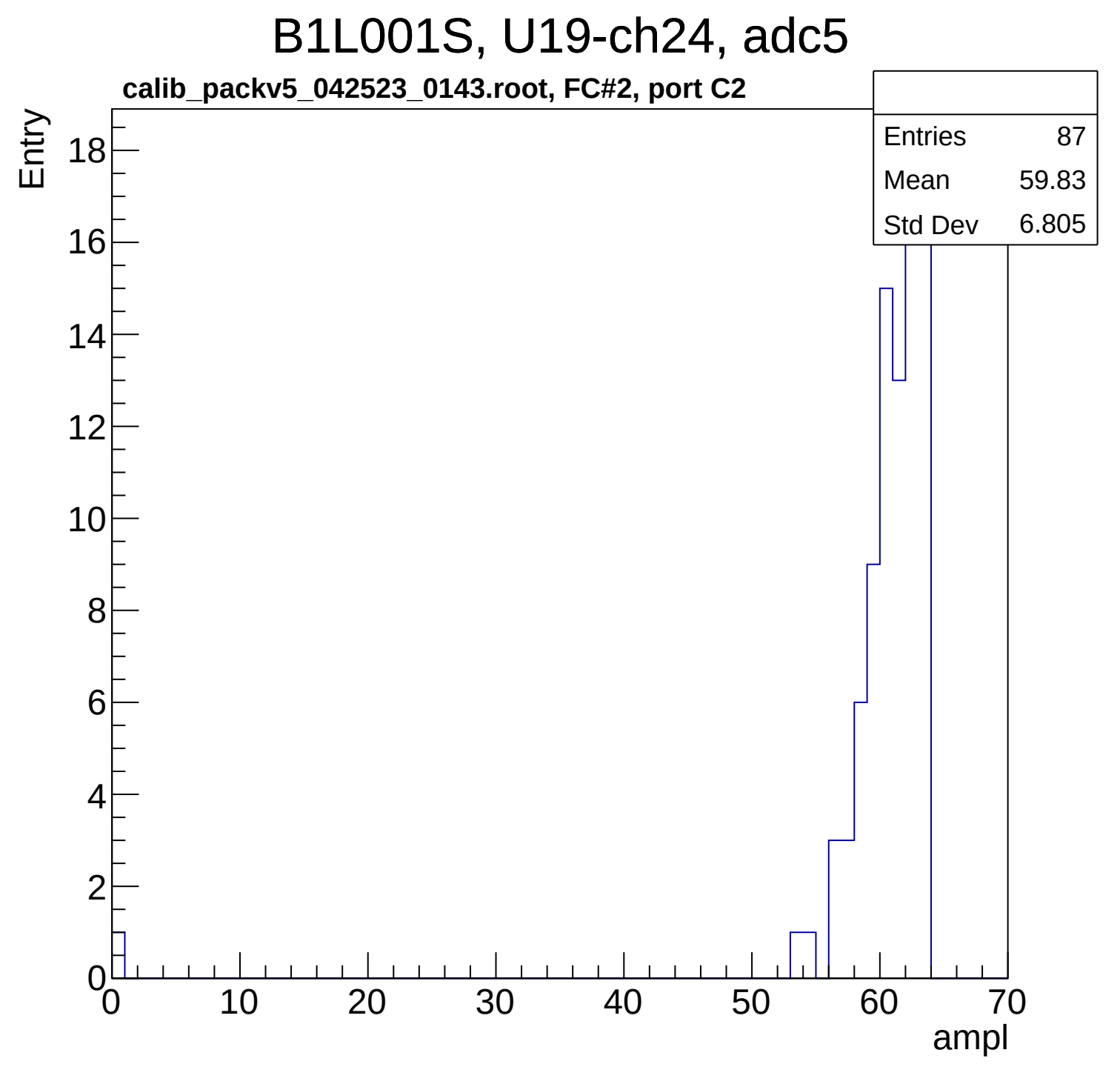

B1L001S, U19-ch24, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 141
Mean 31.8
Std Dev 3.178
Gaus mean : 32.0006
Gaus Width: 2.8044
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70


B1L001S, U19-ch24, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 132
Mean 38.66
Std Dev 2.892
Gaus mean : 39.1524
Gaus Width: 2.9260
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70


B1L001S, U19-ch24, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 111
Mean 44.82
Std Dev 2.975
Gaus mean : 45.6298
Gaus Width: 2.7404
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L001S, U19-ch24, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 126
Mean 50.64
Std Dev 3.095
Entry
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch24, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 106
Mean 55.86
Std Dev 6.144
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch24, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 87
Mean 59.83
Std Dev 6.805
Entry
ampl
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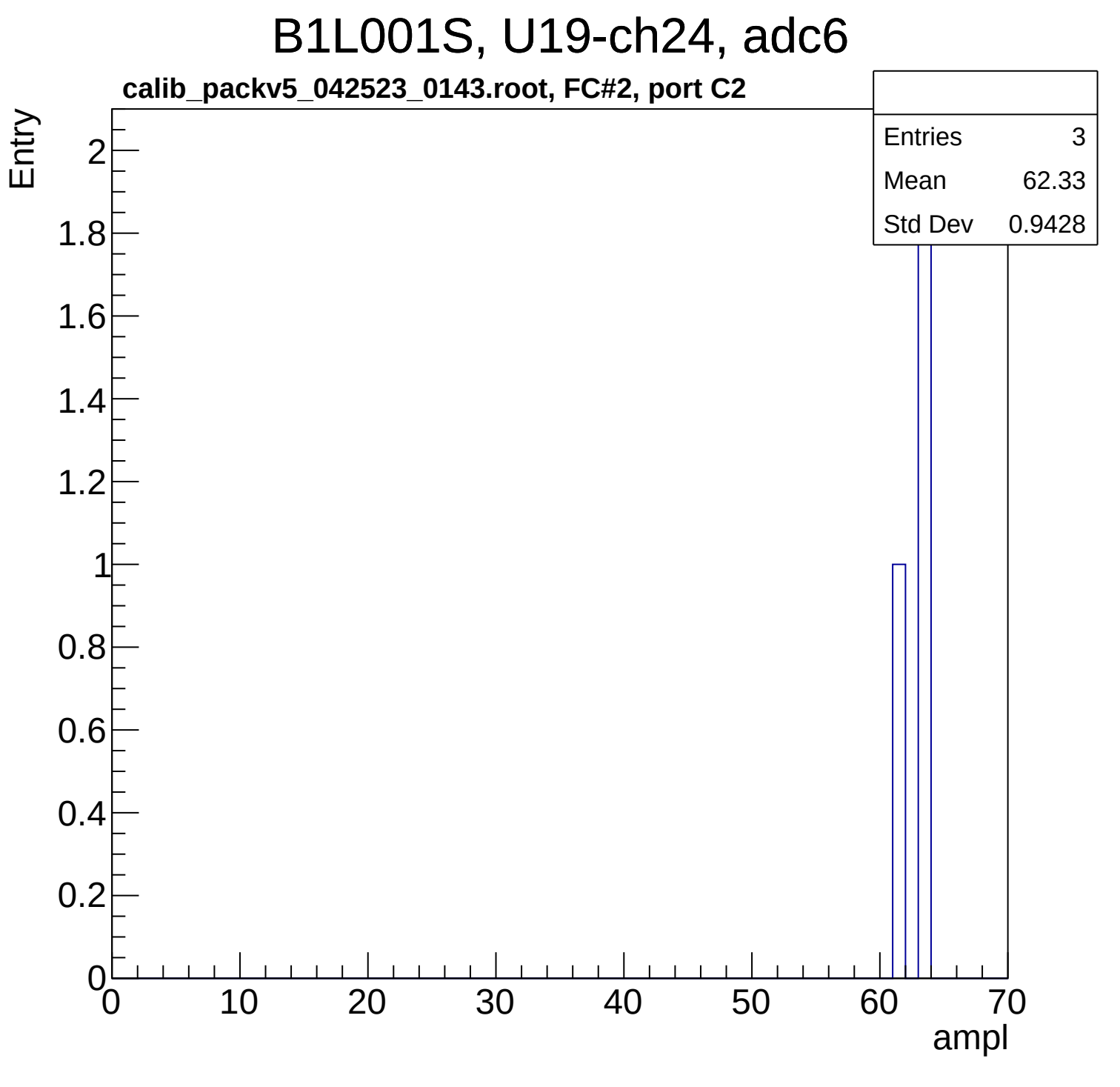
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70


B1L001S, U19-ch24, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 3
Mean 62.33
Std Dev 0.9428
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
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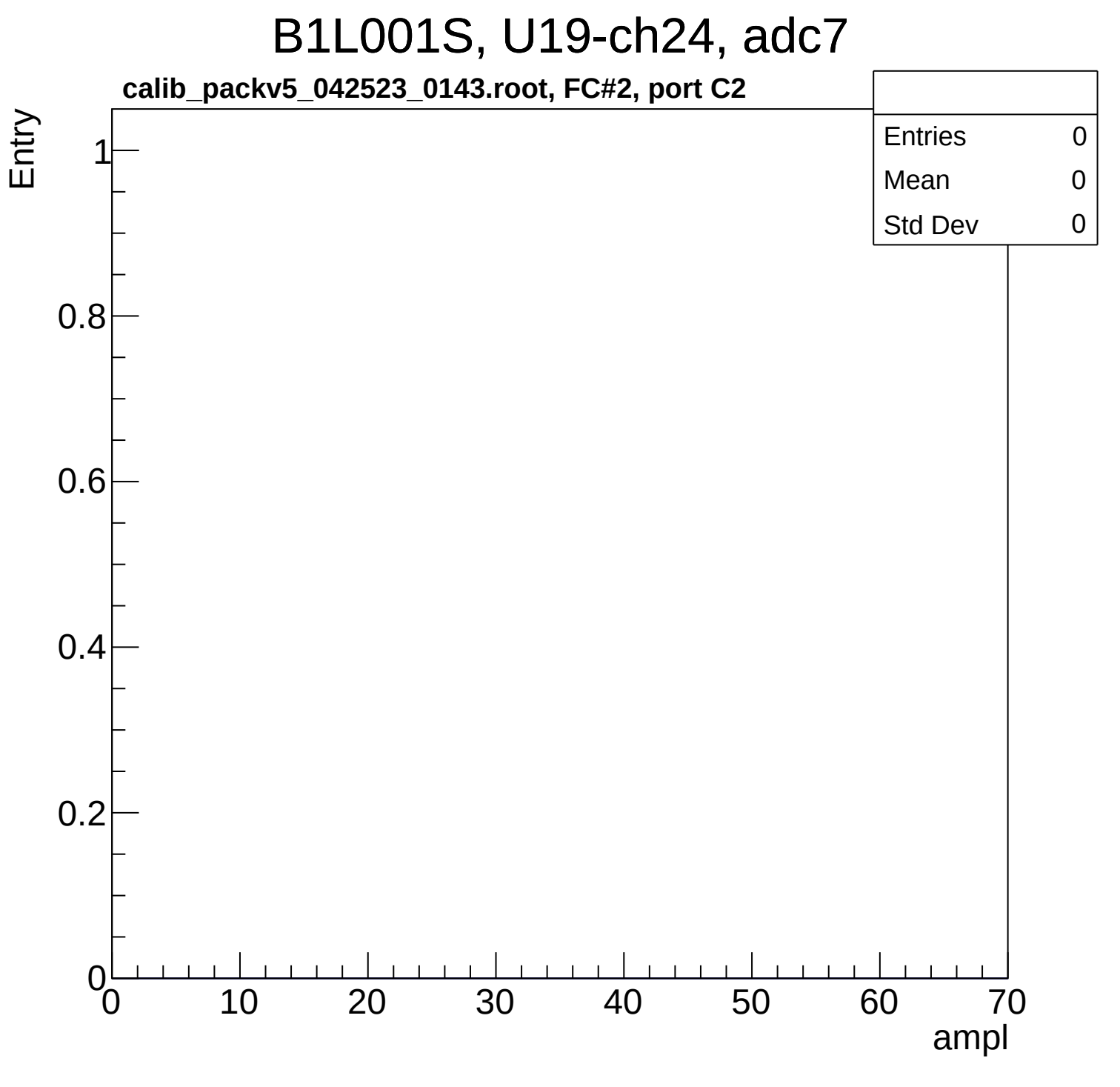
60
70


B1L001S, U19-ch24, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 0
Mean 0
Std Dev 0
Entry
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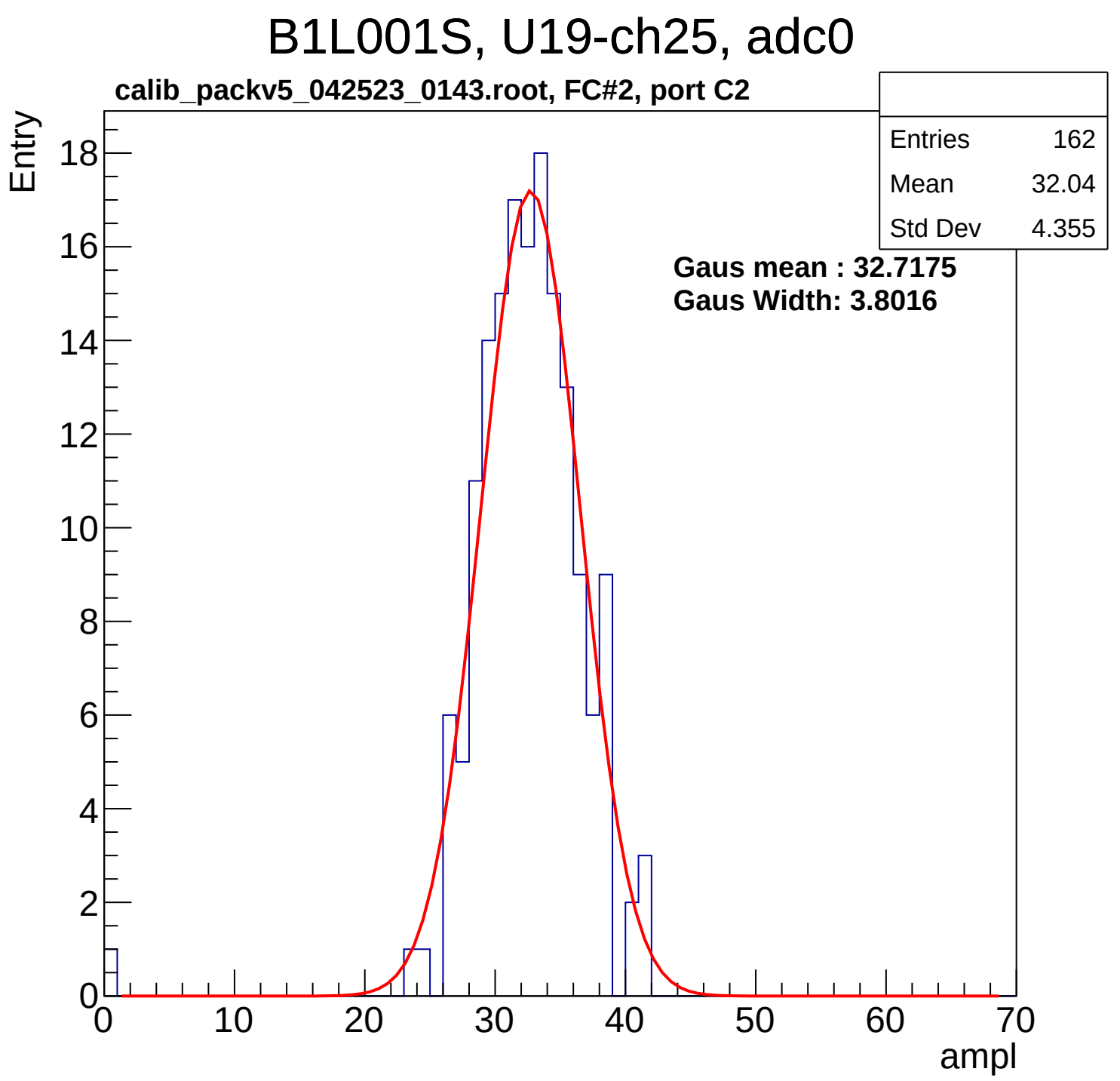
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch25, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 162
Mean 32.04
Std Dev 4.355
Gaus mean : 32.7175
Gaus Width: 3.8016
Entry
ampl
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4
6
8
10
12
14
16
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0
10
20
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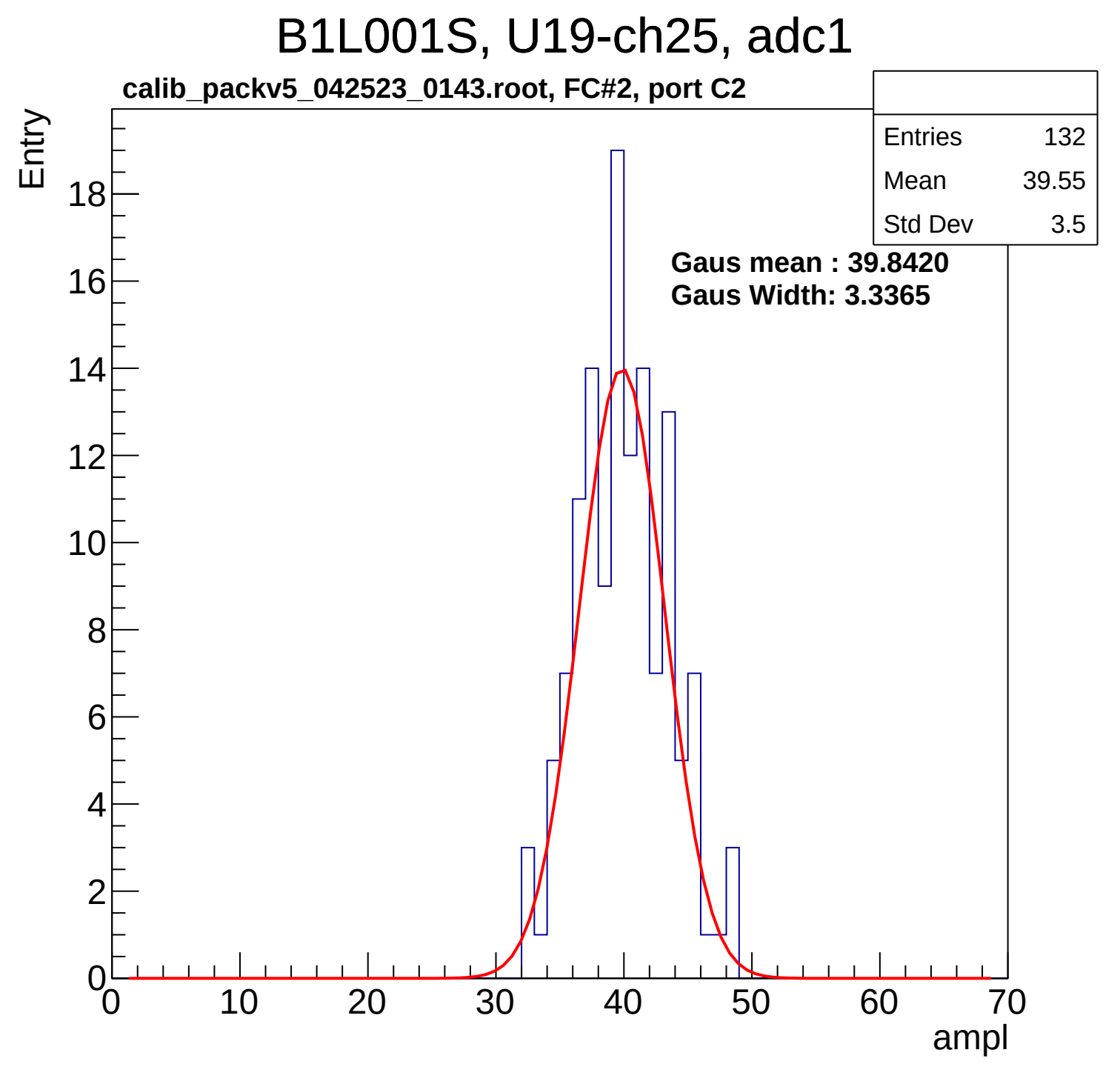
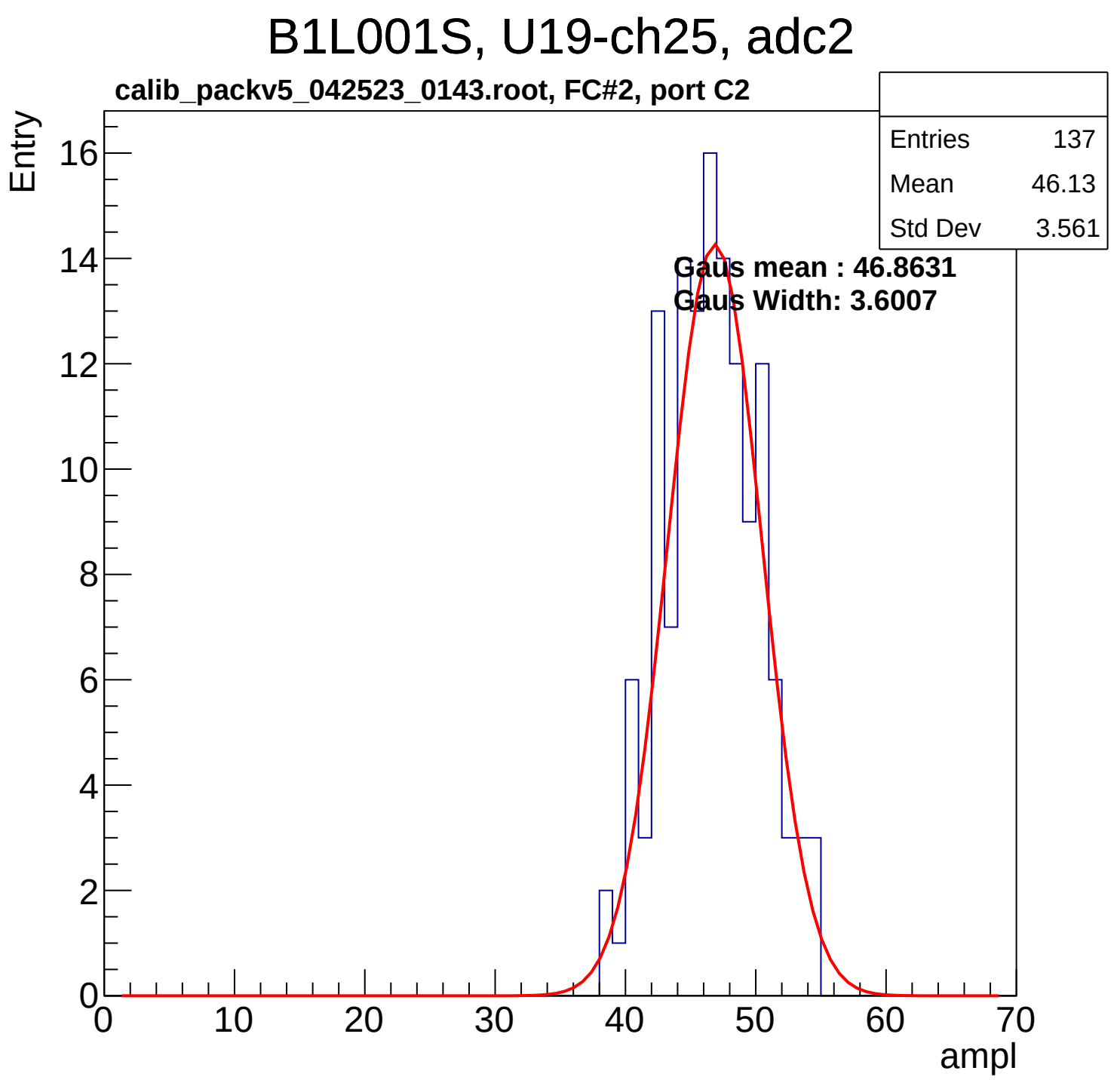
40
50
60
70


B1L001S, U19-ch25, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 132
Mean 39.55
Std Dev 3.5
Gaus mean : 39.8420
Gaus Width: 3.3365
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70


B1L001S, U19-ch25, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 137
Mean 46.13
Std Dev 3.561
Gaus mean : 46.8631
Gaus Width: 3.6007
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
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50
60
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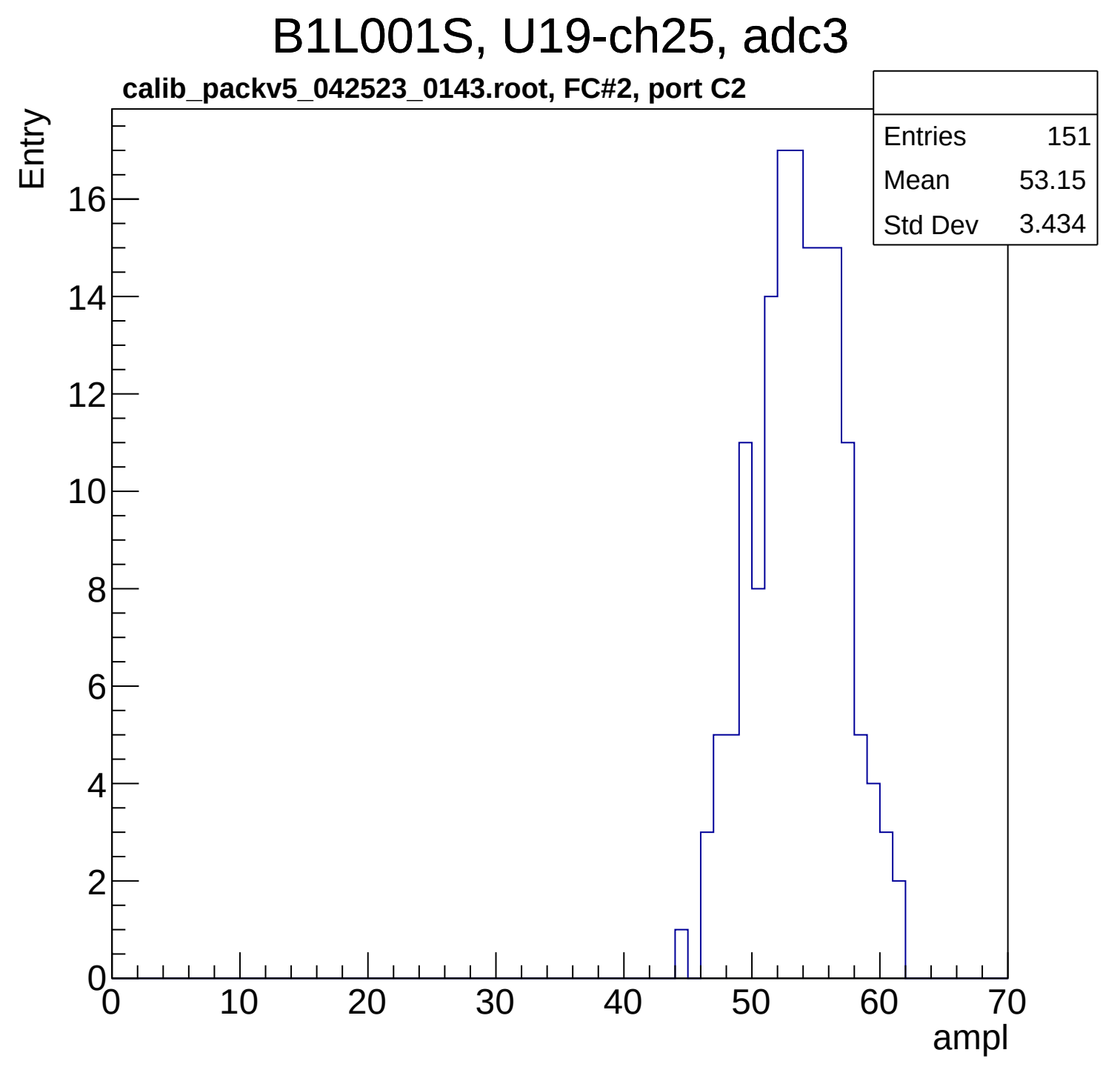
B1L001S, U19-ch25, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 151
Mean 53.15
Std Dev 3.434
Entry
ampl
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2
4
6
8
10
12
14
16
0
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60
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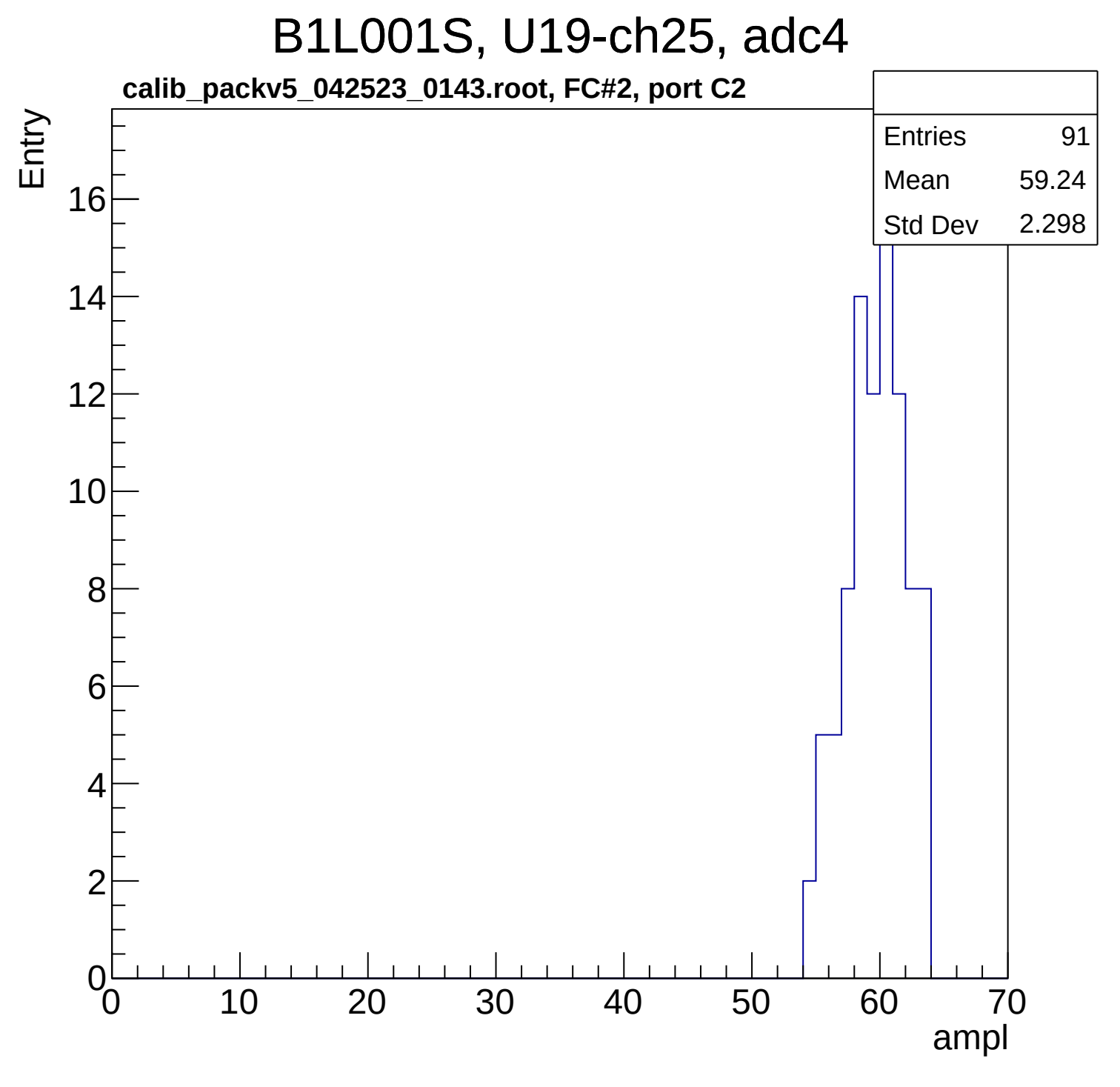
B1L001S, U19-ch25, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 91
Mean 59.24
Std Dev 2.298
Entry
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4
6
8
10
12
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16
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10
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50
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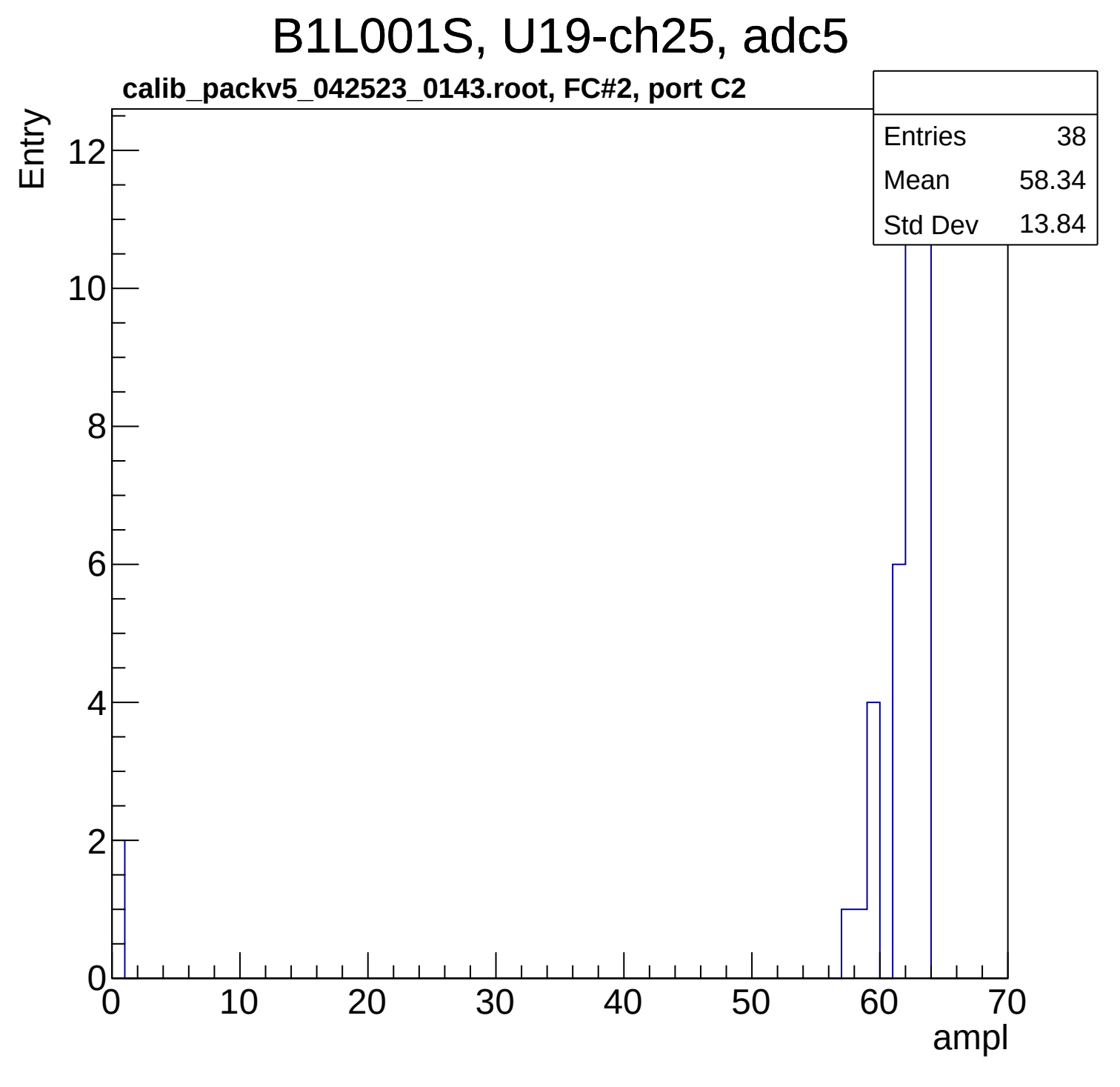
70
ampl


B1L001S, U19-ch25, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 38
Mean 58.34
Std Dev 13.84
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
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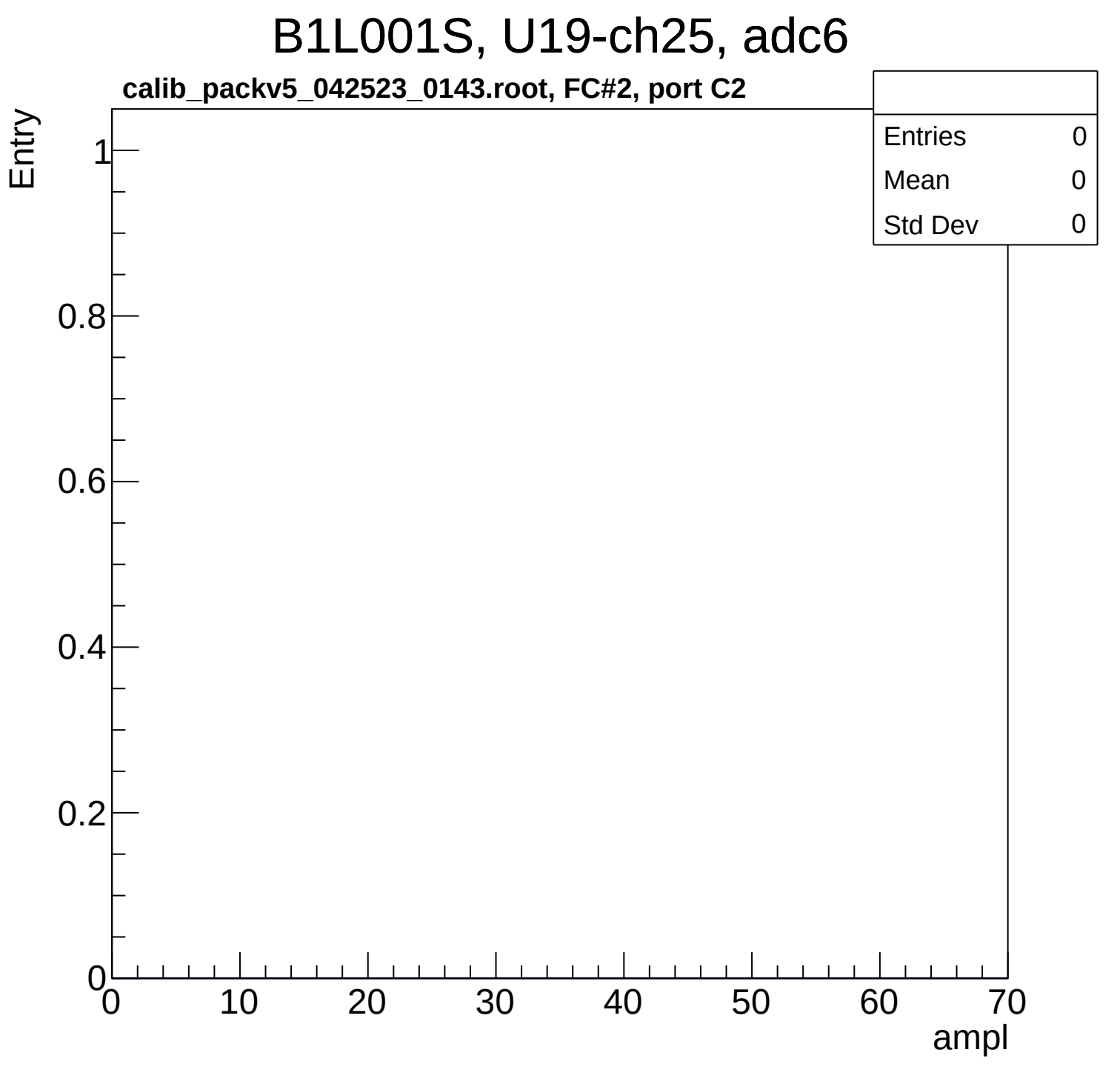
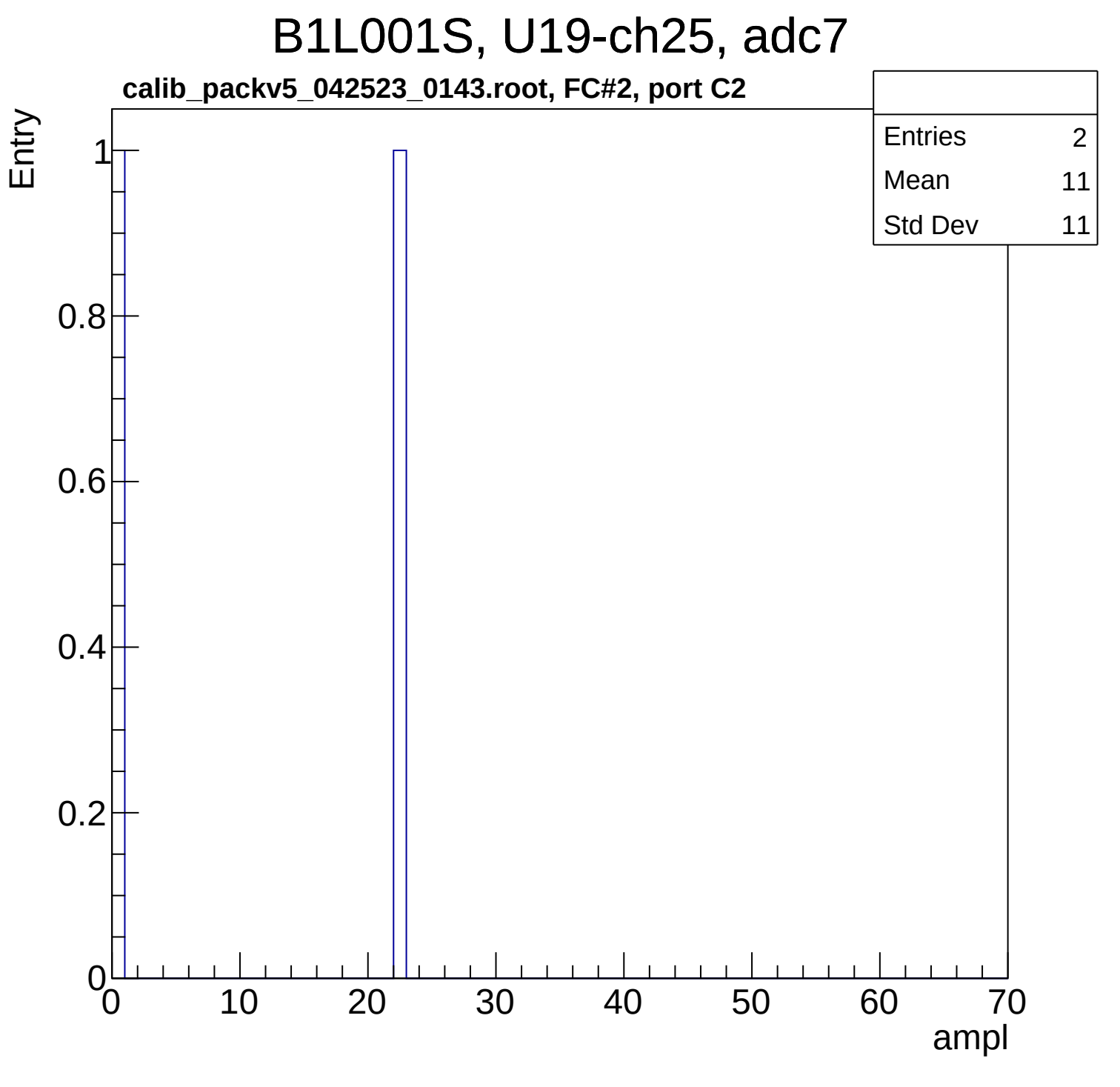
70
ampl


B1L001S, U19-ch25, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch25, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 11
Std Dev 11
Entry
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0.6
0.4
0.2
0
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10
20
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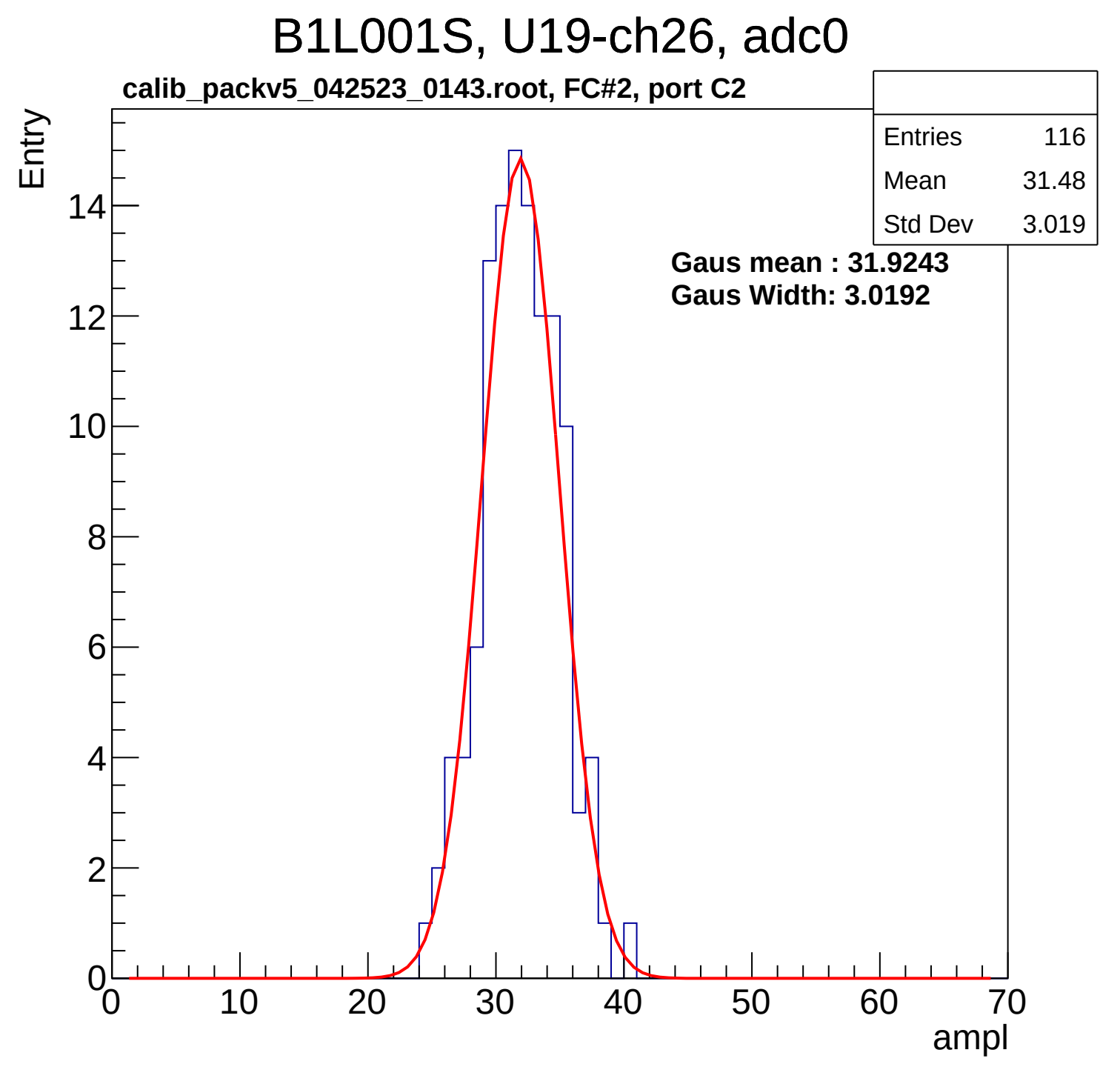
70
ampl


B1L001S, U19-ch26, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 116
Mean 31.48
Std Dev 3.019
Gaus mean : 31.9243
Gaus Width: 3.0192
Entry
ampl
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2
4
6
8
10
12
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0
10
20
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40
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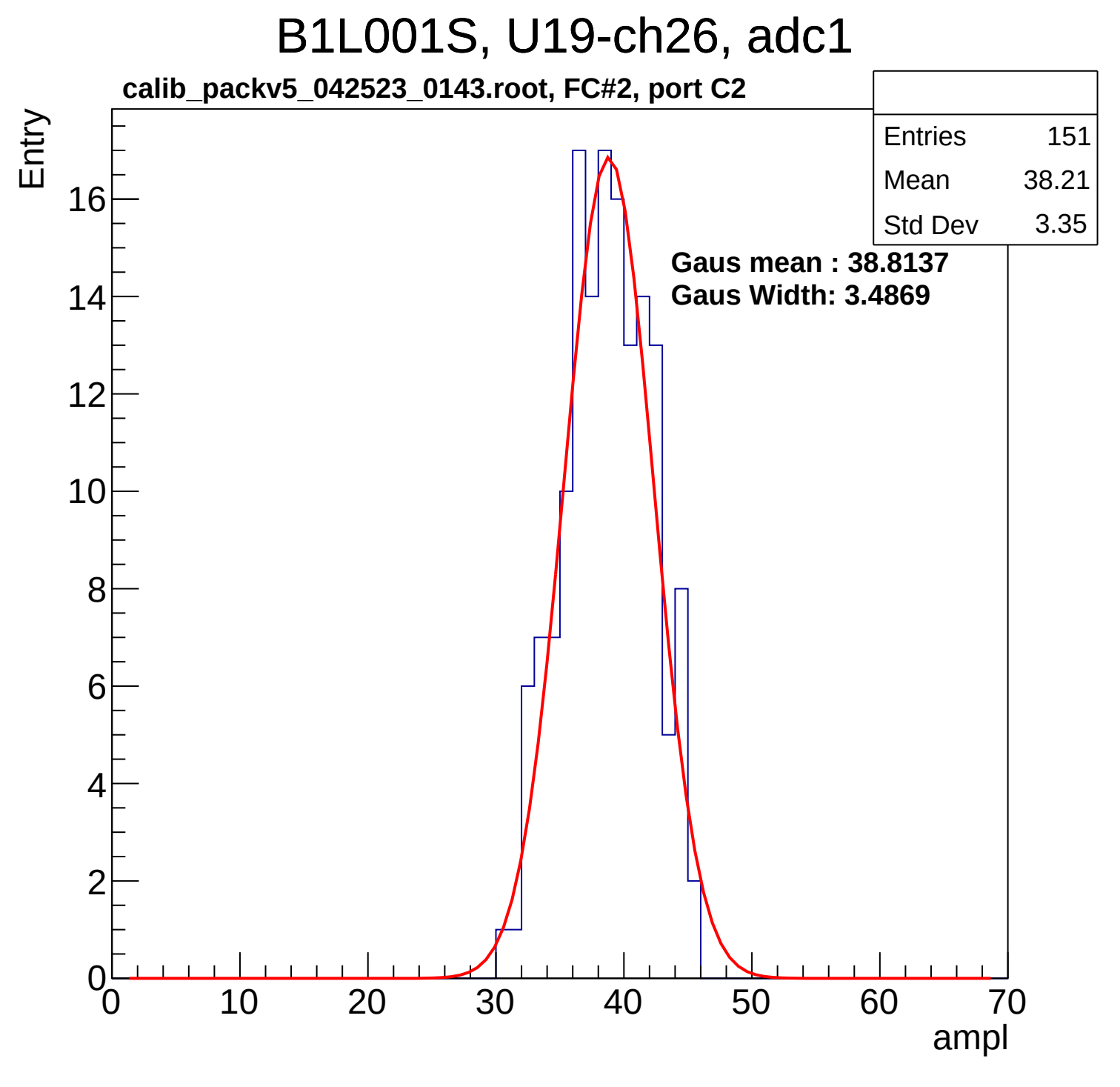
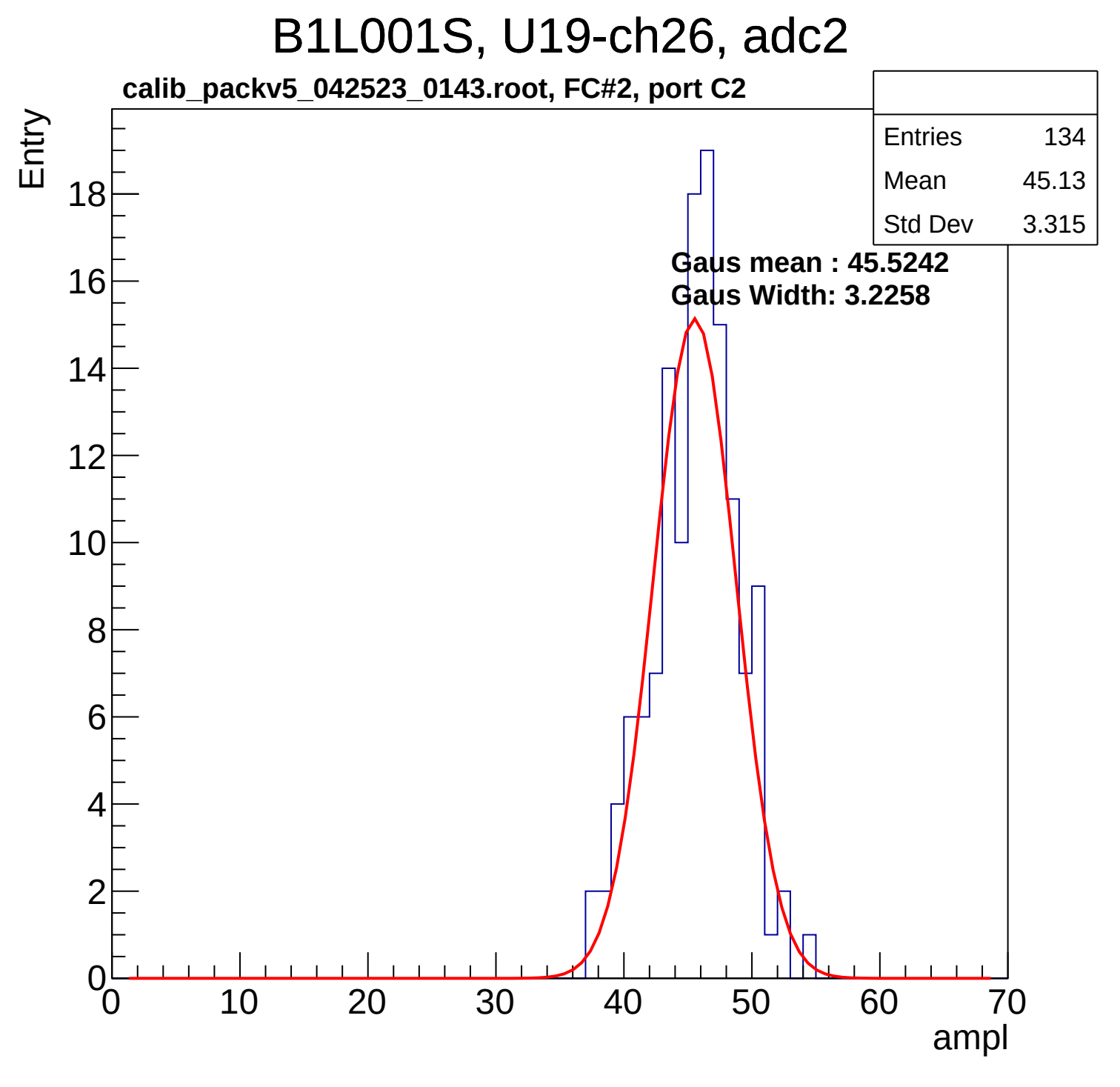

B1L001S, U19-ch26, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 151
Mean 38.21
Std Dev 3.35
Gaus mean : 38.8137
Gaus Width: 3.4869
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70


B1L001S, U19-ch26, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 134
Mean 45.13
Std Dev 3.315
Gaus mean : 45.5242
Gaus Width: 3.2258
Entry
ampl
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4
6
8
10
12
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16
18
0
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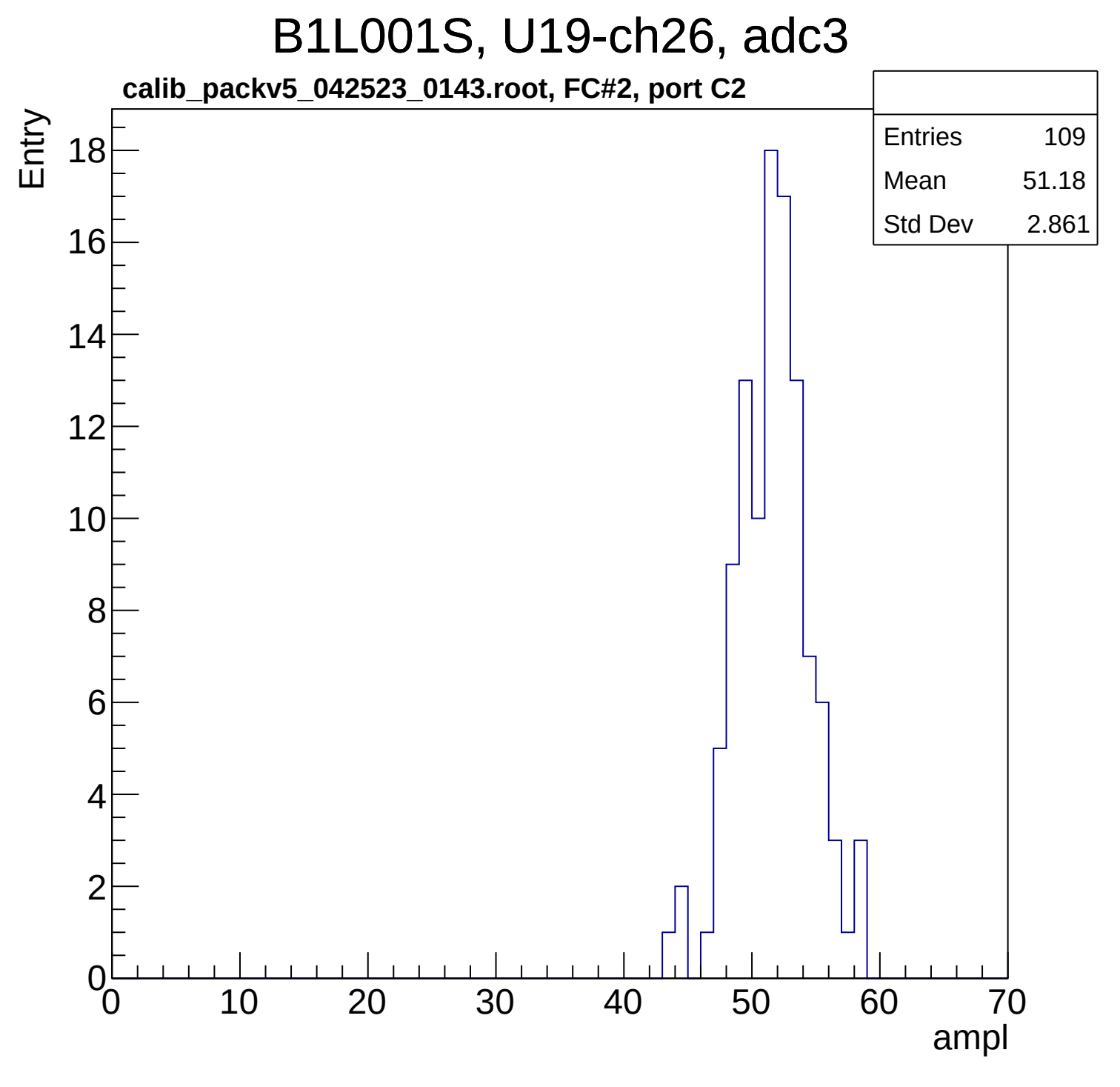
B1L001S, U19-ch26, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 109
Mean 51.18
Std Dev 2.861
Entry
0
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6
8
10
12
14
16
18
0
10
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30
40
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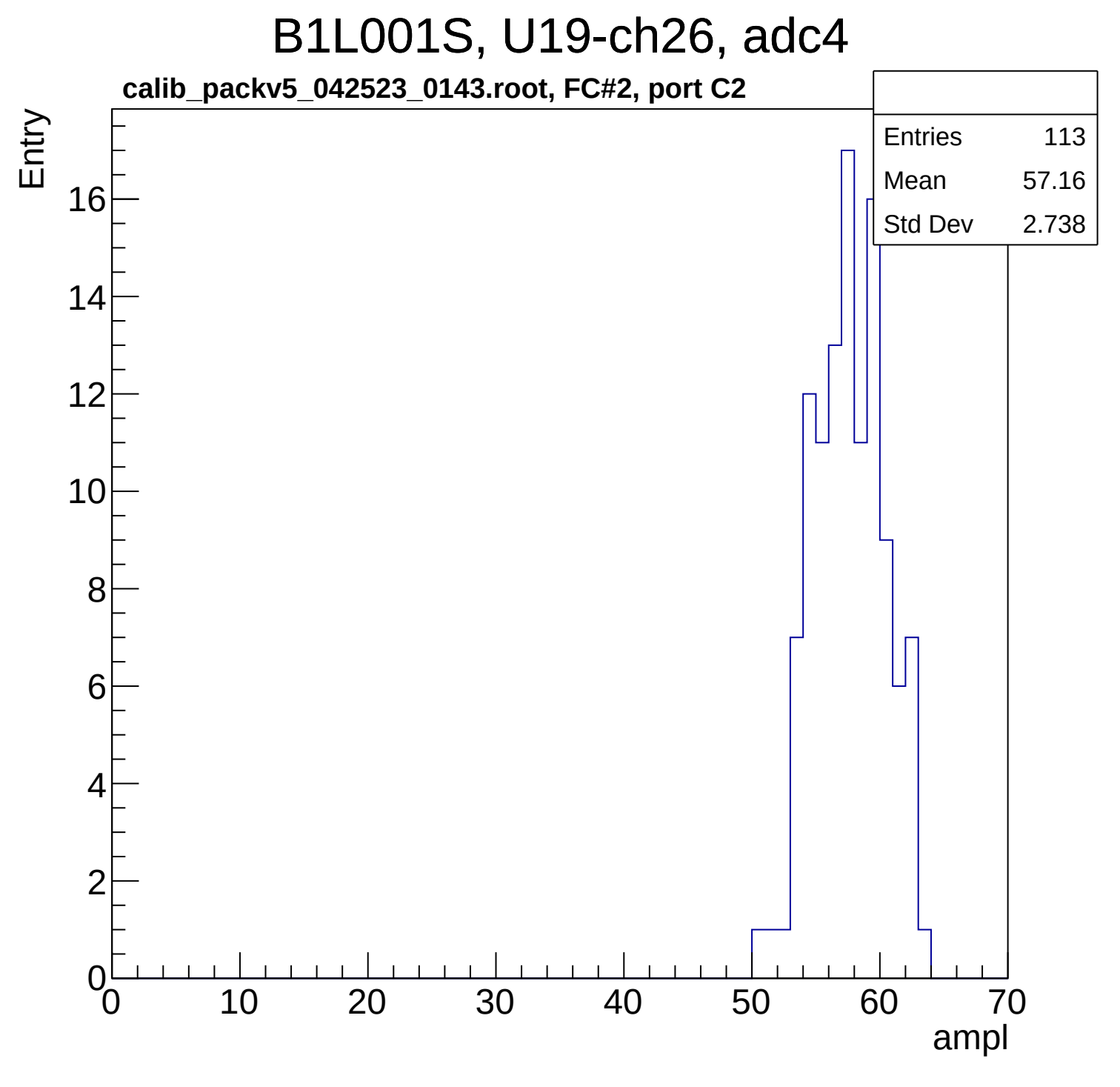
60
70
ampl


B1L001S, U19-ch26, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 113
Mean 57.16
Std Dev 2.738
Entry
ampl
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2
4
6
8
10
12
14
16
0
10
20
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40
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60
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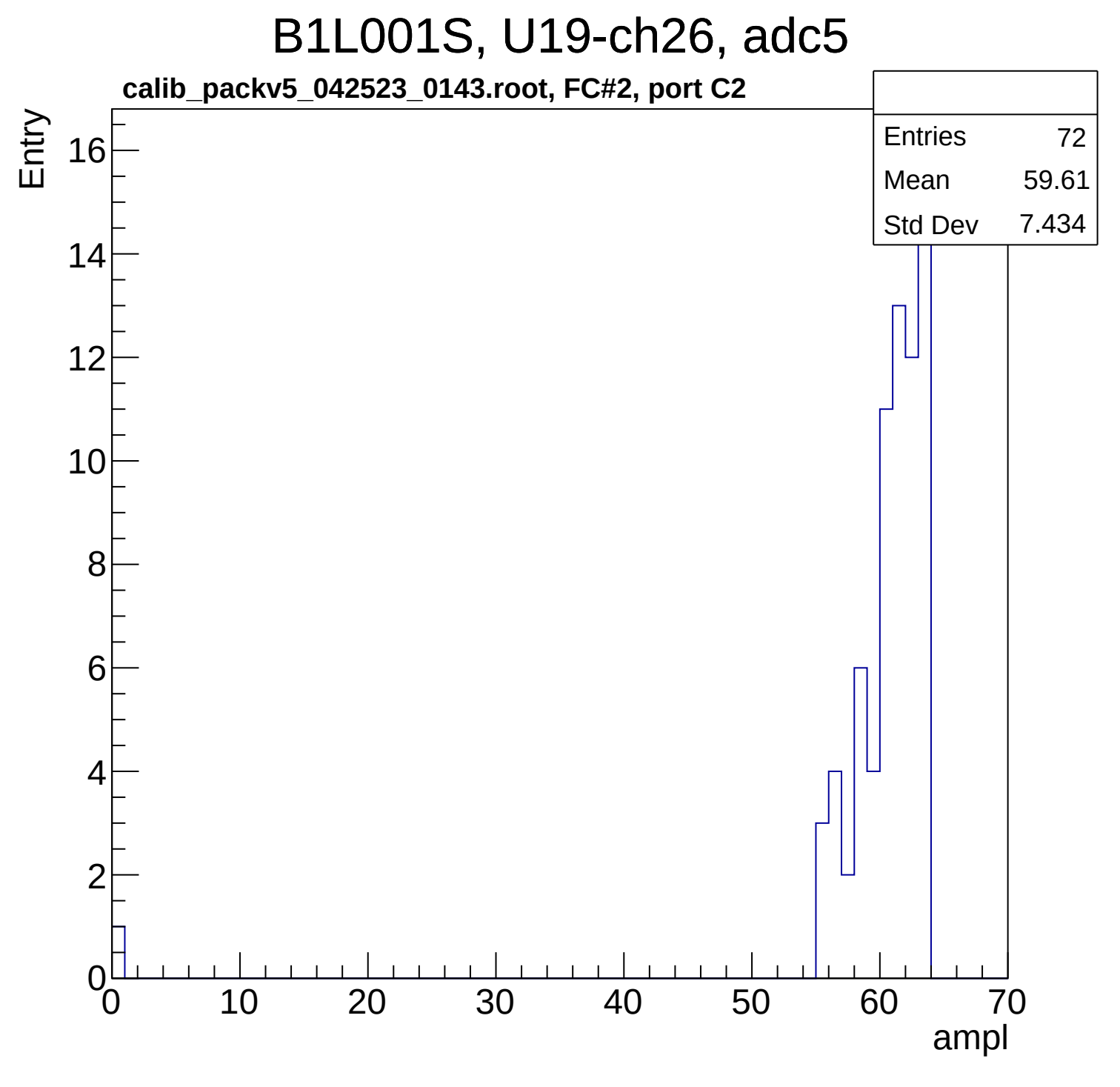
B1L001S, U19-ch26, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 72
Mean 59.61
Std Dev 7.434
Entry
0
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6
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10
12
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16
0
10
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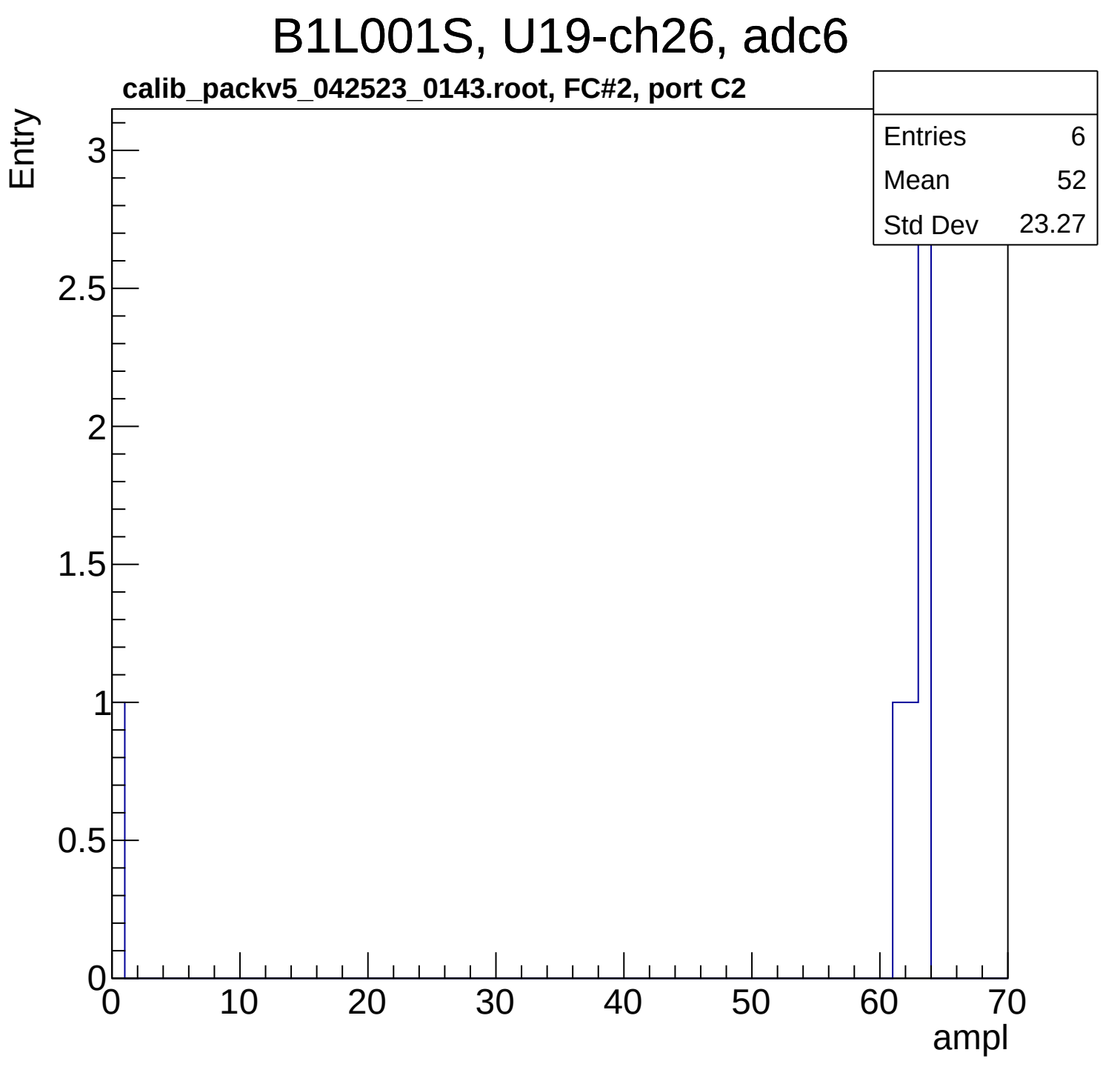
50
60
70
ampl


B1L001S, U19-ch26, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 6
Mean 52
Std Dev 23.27
Entry
ampl
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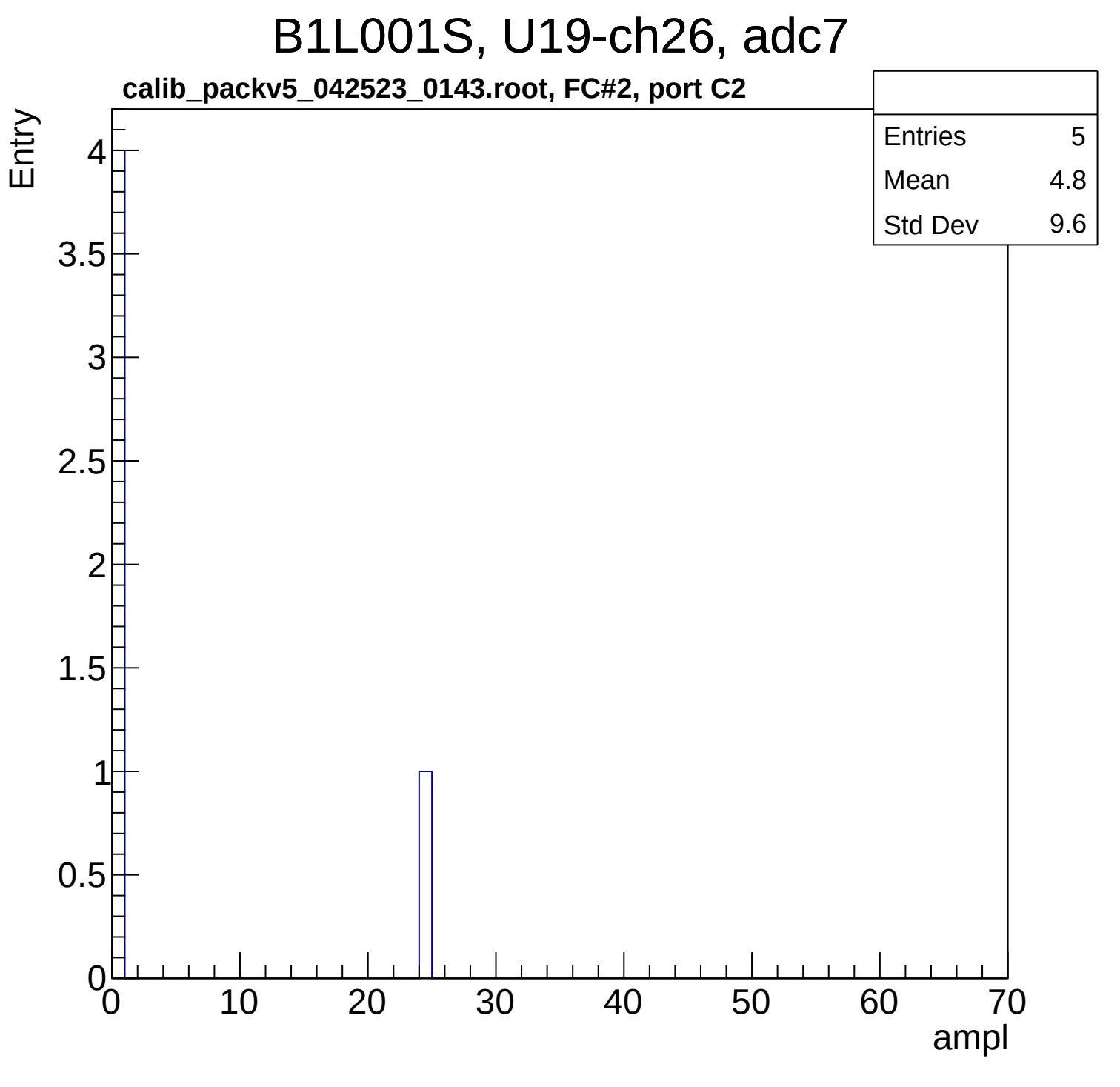
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L001S, U19-ch26, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 5
Mean 4.8
Std Dev 9.6
Entry
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
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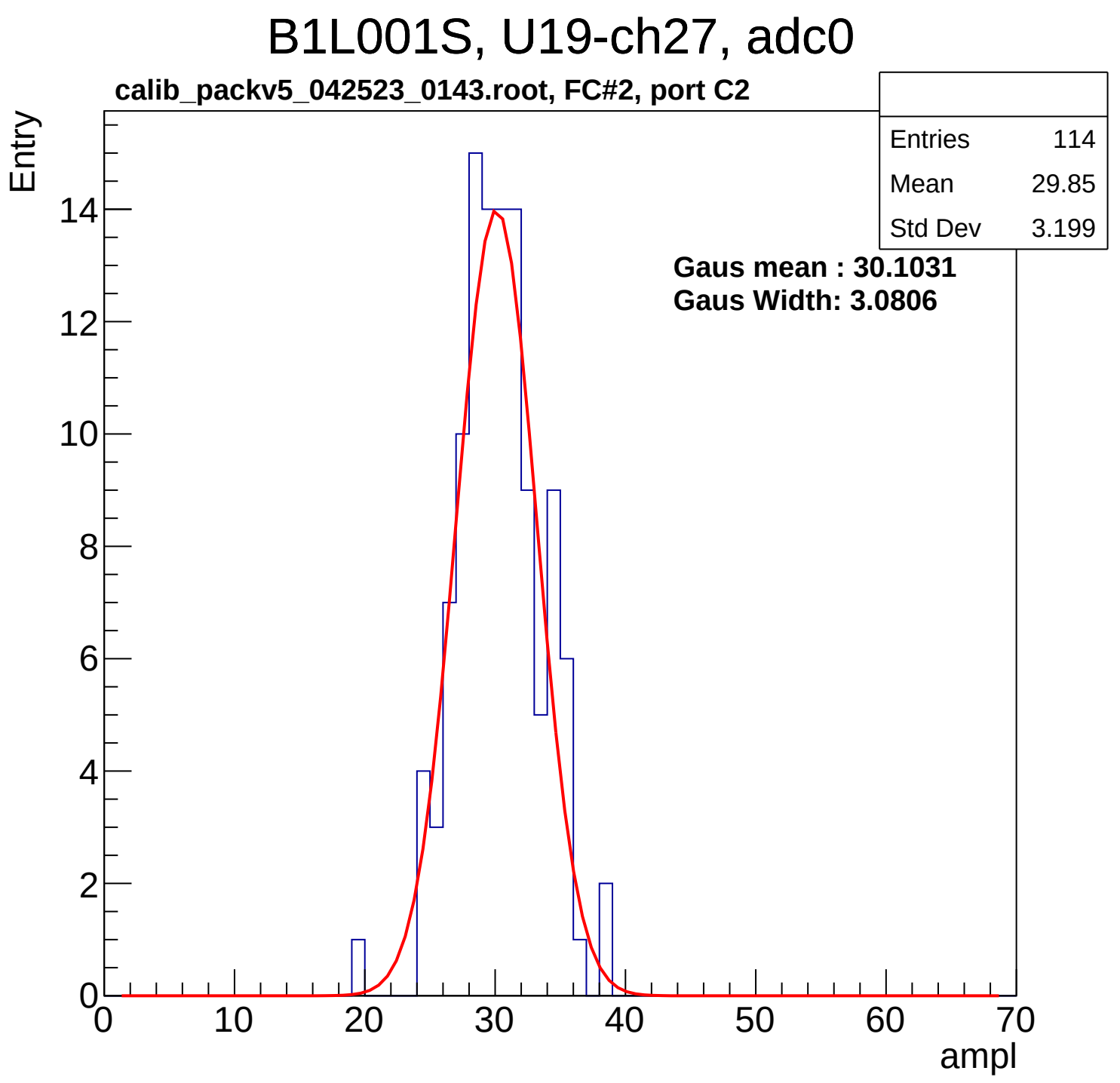
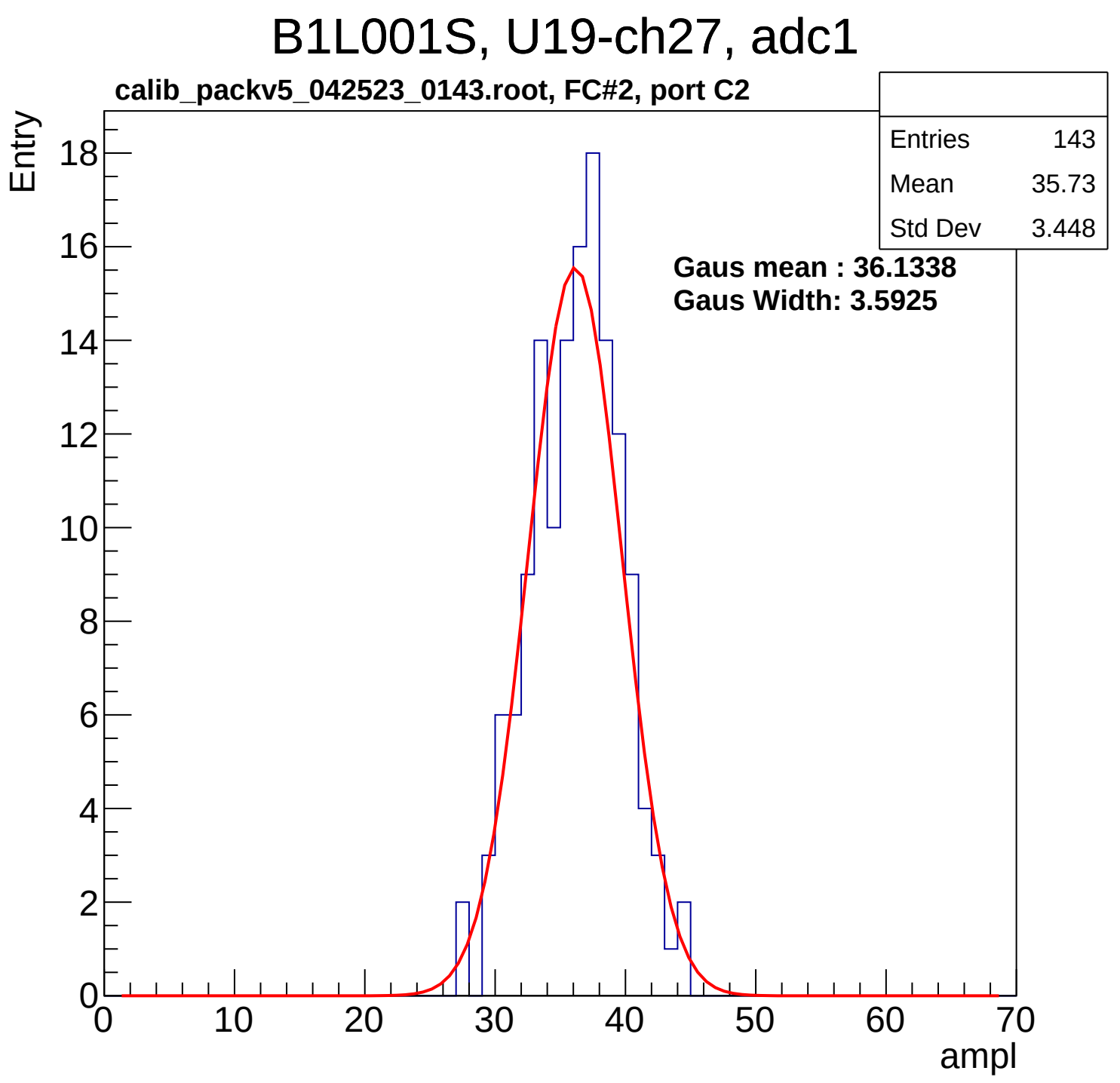
50
60
70
ampl


B1L001S, U19-ch27, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 114
Mean 29.85
Std Dev 3.199
Gaus mean : 30.1031
Gaus Width: 3.0806
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L001S, U19-ch27, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 143
Mean 35.73
Std Dev 3.448
Gaus mean : 36.1338
Gaus Width: 3.5925
Entry
ampl
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4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
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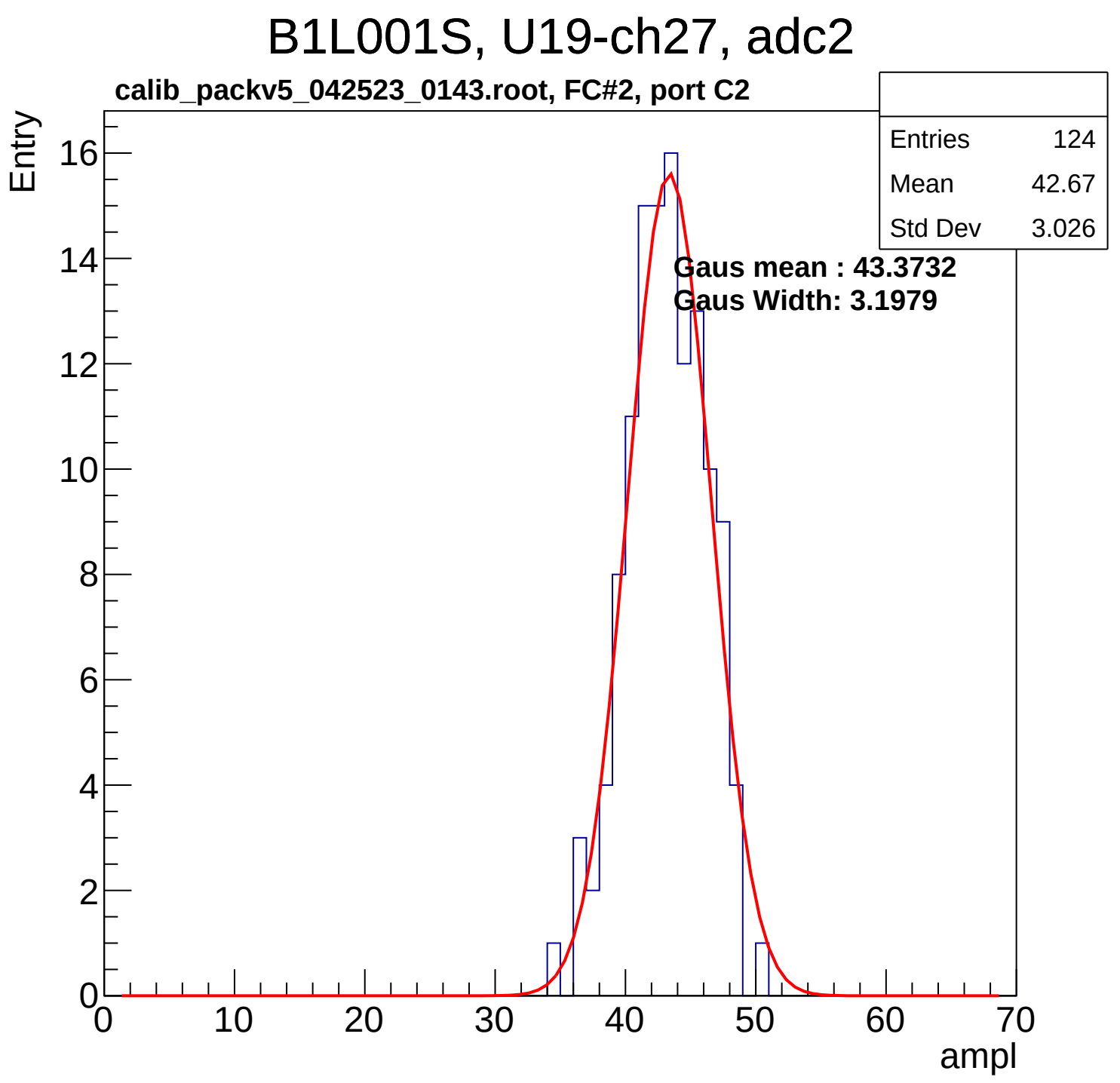
B1L001S, U19-ch27, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 124
Mean 42.67
Std Dev 3.026
Gaus mean : 43.3732
Gaus Width: 3.1979
Entry
ampl
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2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
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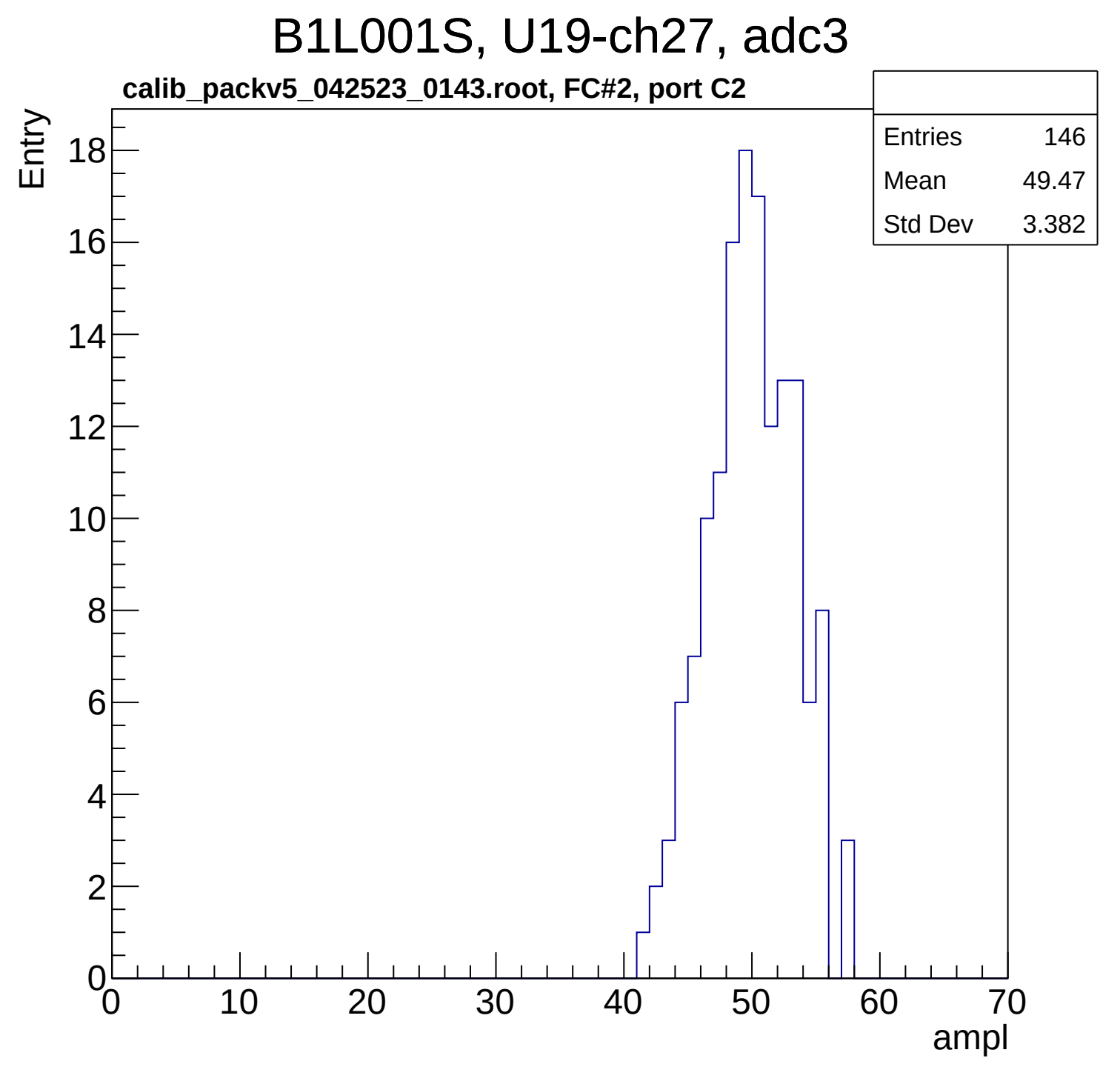
B1L001S, U19-ch27, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 146
Mean 49.47
Std Dev 3.382
Entry
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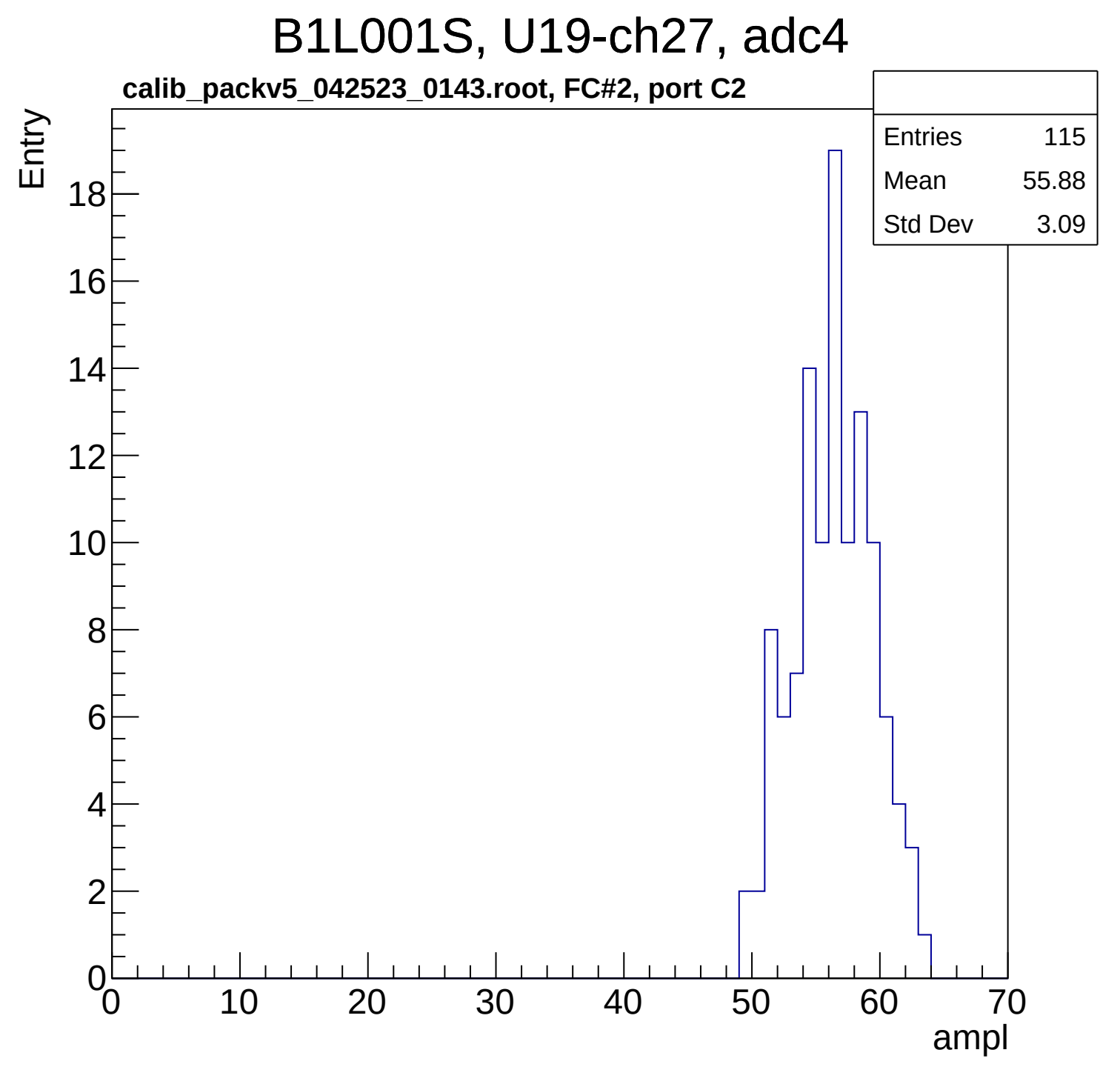
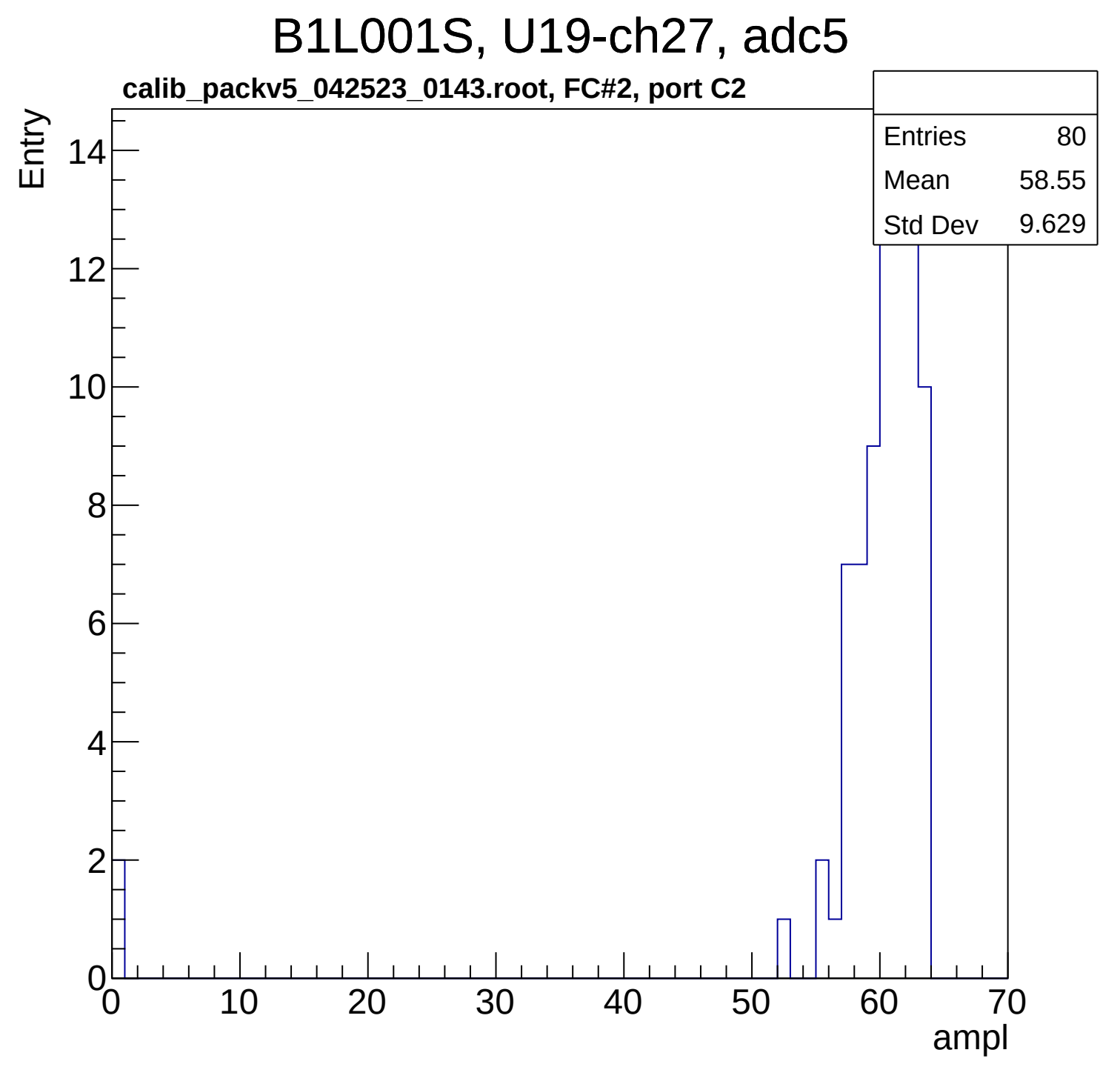
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch27, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 115
Mean 55.88
Std Dev 3.09
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch27, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 80
Mean 58.55
Std Dev 9.629
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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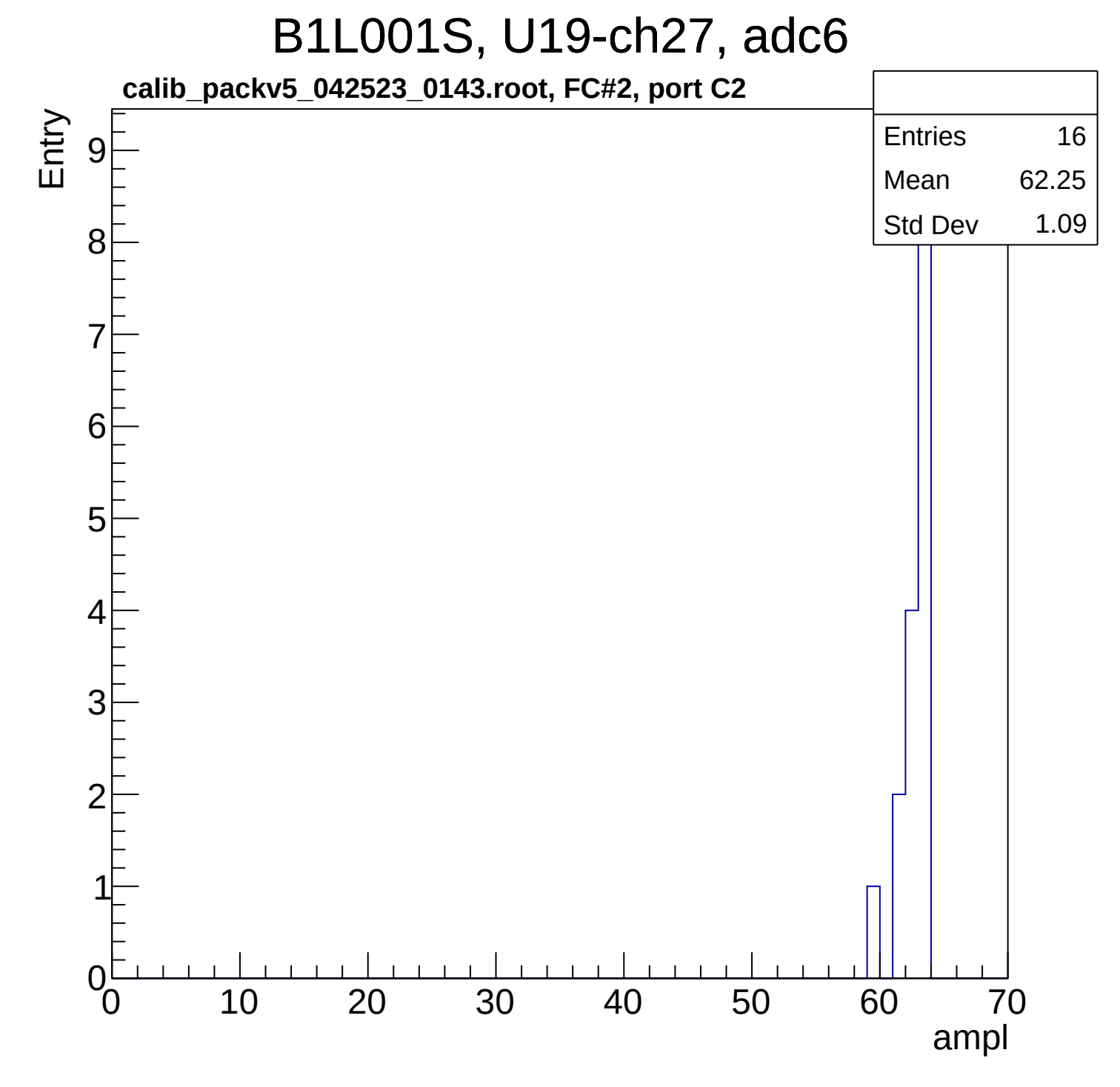
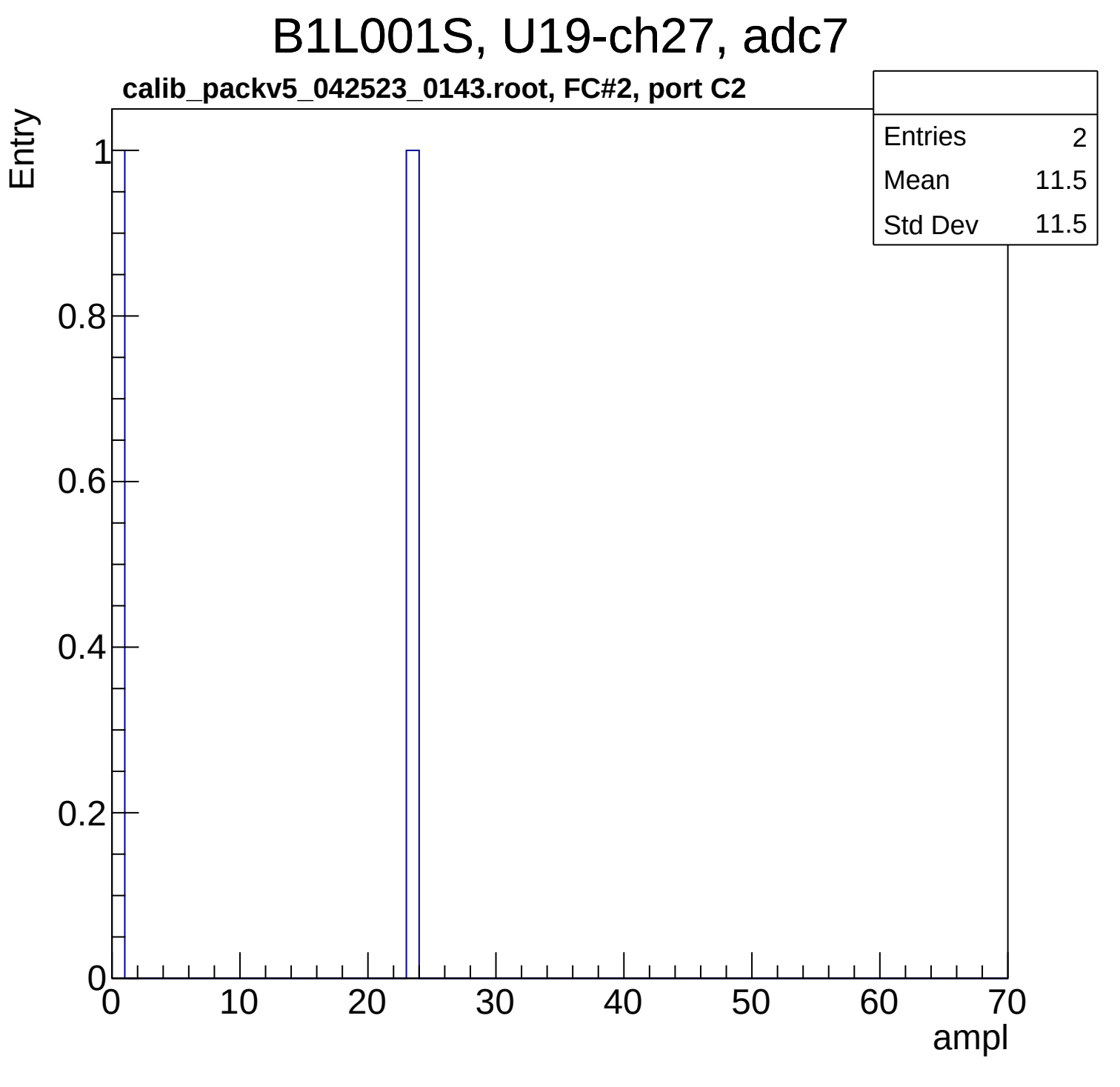
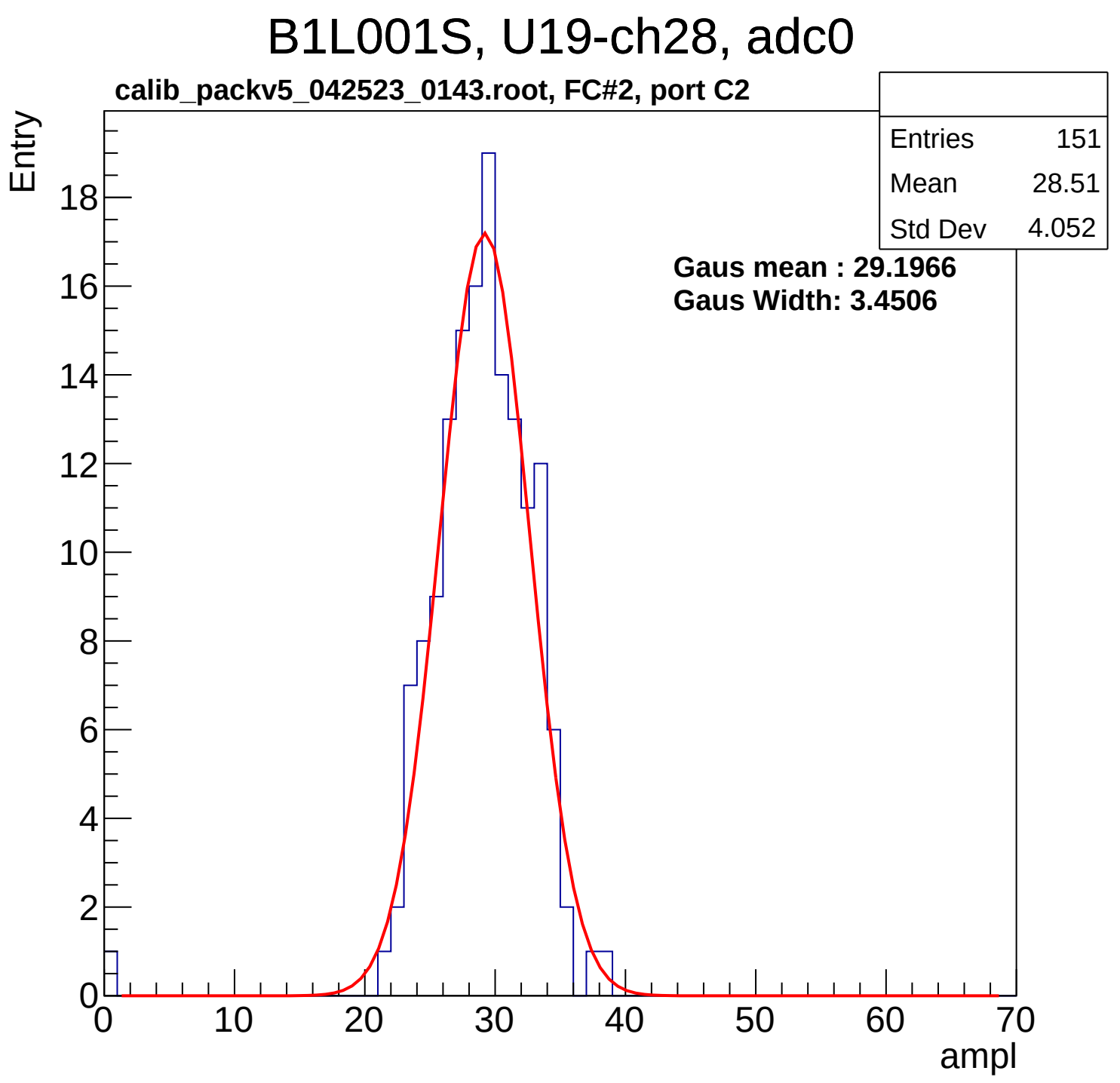

B1L001S, U19-ch27, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 16
Mean 62.25
Std Dev 1.09
Entry
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch27, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 11.5
Std Dev 11.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch28, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 151
Mean 28.51
Std Dev 4.052
Gaus mean : 29.1966
Gaus Width: 3.4506
Entry
ampl
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4
6
8
10
12
14
16
18
0
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20
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60
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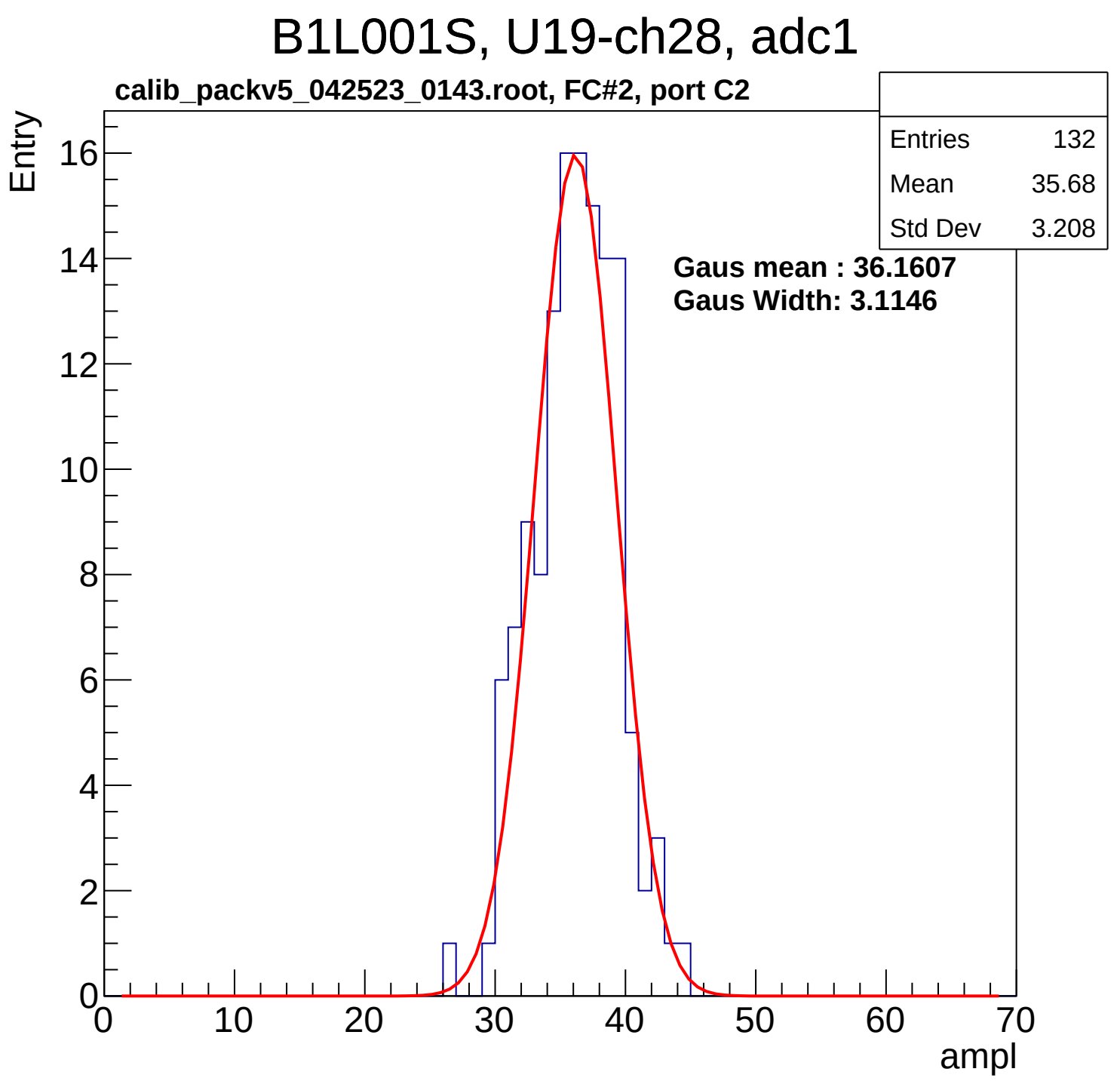
B1L001S, U19-ch28, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 132
Mean 35.68
Std Dev 3.208
Gaus mean : 36.1607
Gaus Width: 3.1146
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
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60
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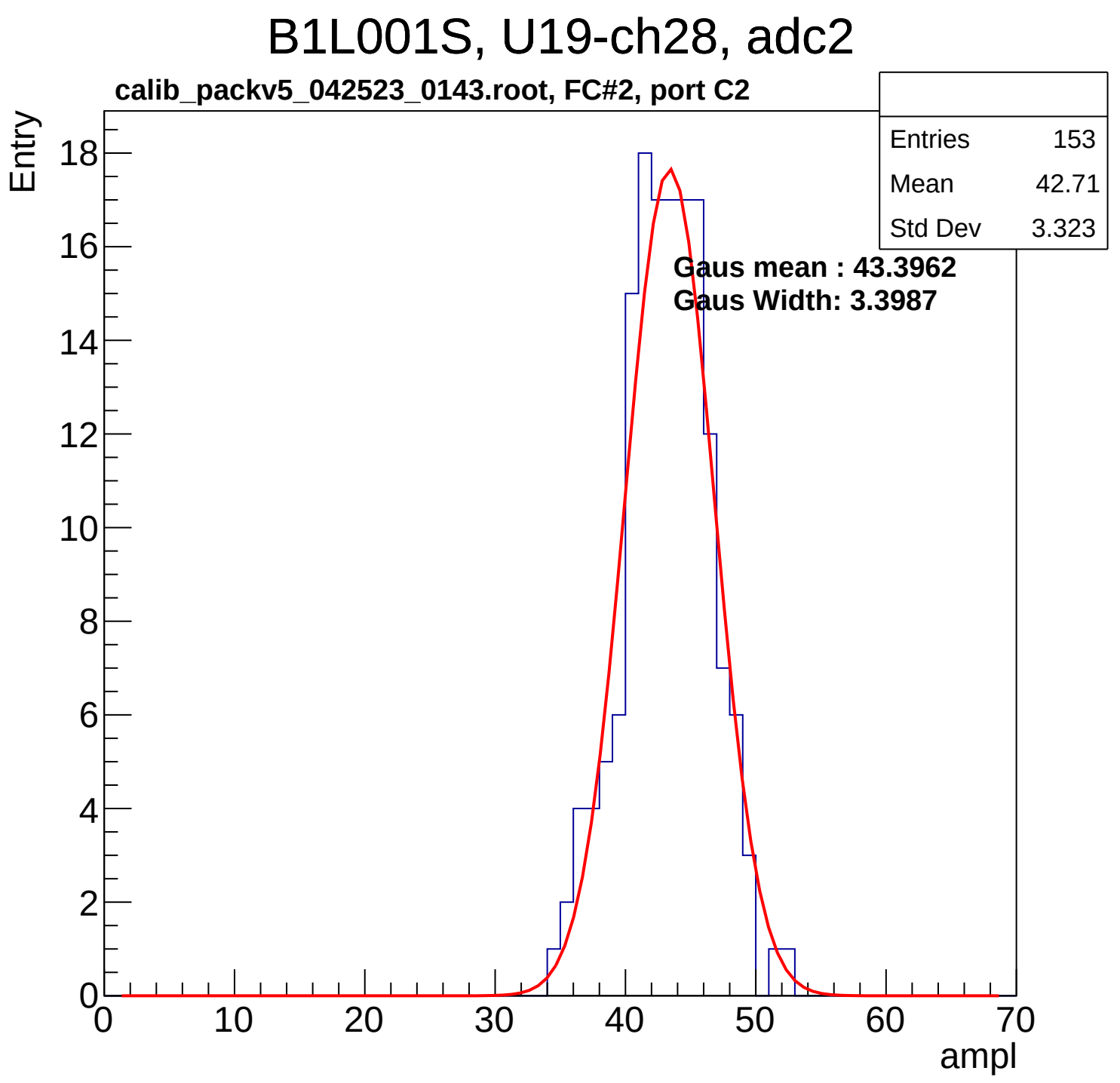
B1L001S, U19-ch28, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 153
Mean 42.71
Std Dev 3.323
Gaus mean : 43.3962
Gaus Width: 3.3987
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
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60
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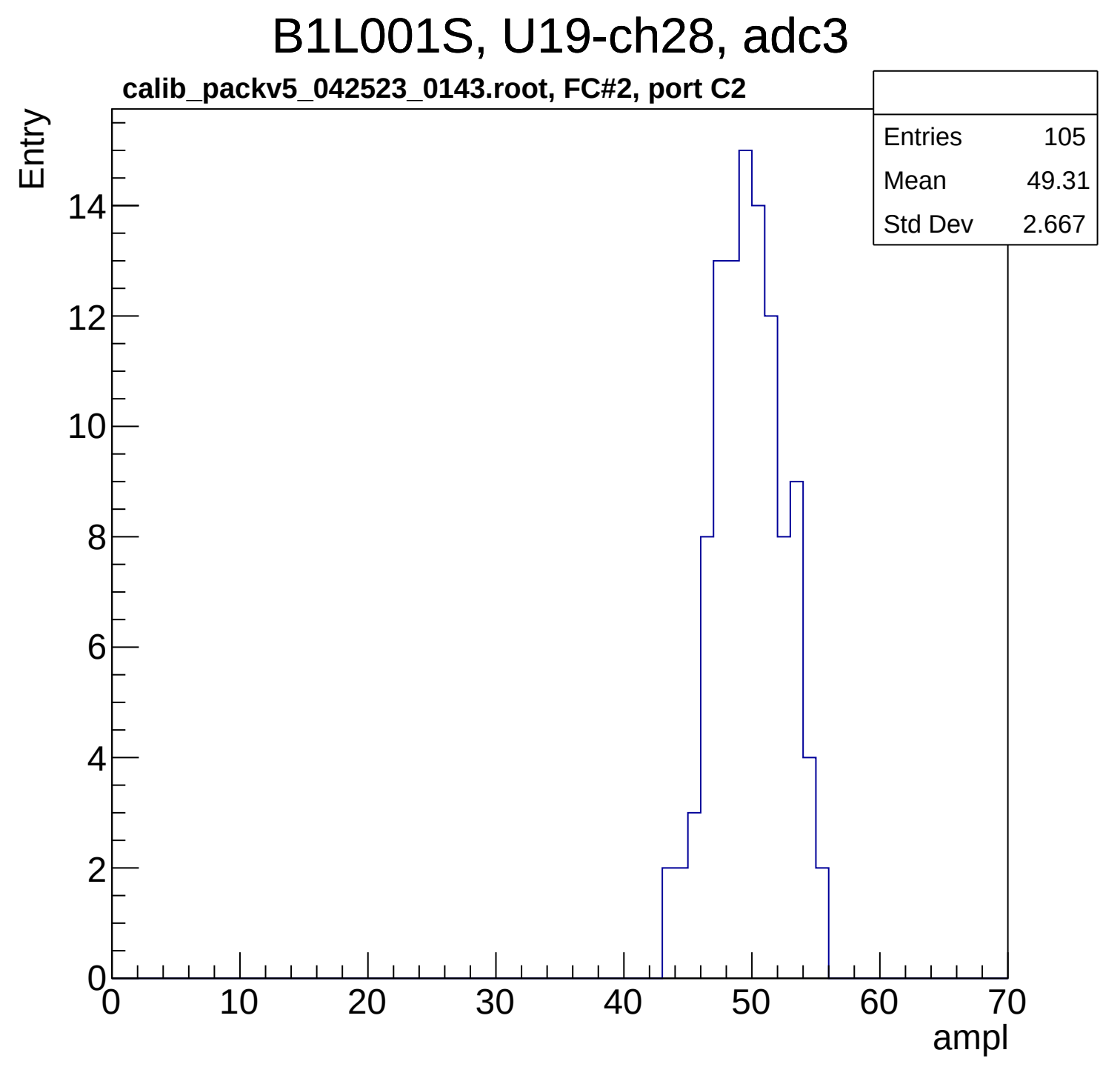
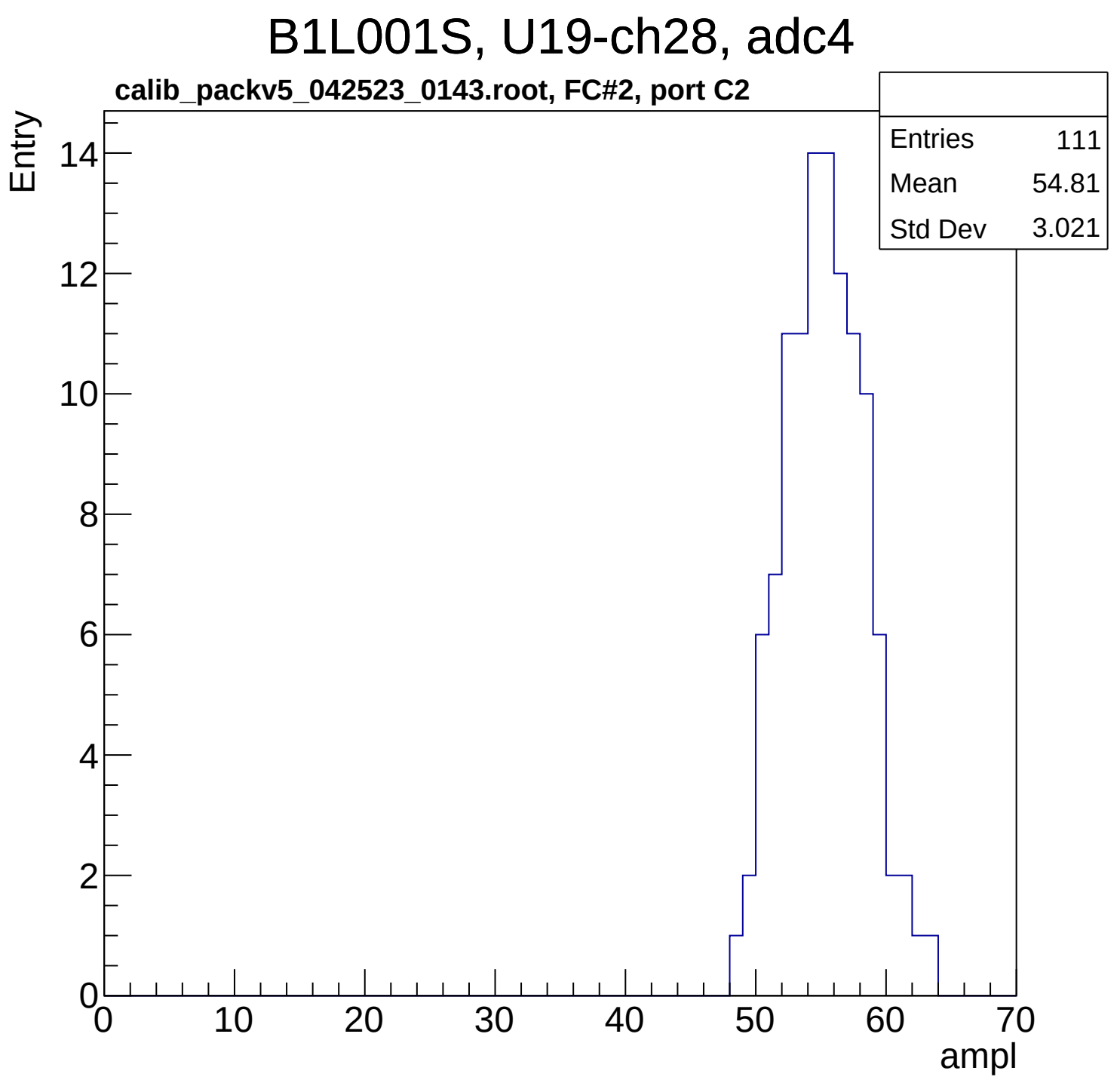

B1L001S, U19-ch28, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 105
Mean 49.31
Std Dev 2.667
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch28, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 111
Mean 54.81
Std Dev 3.021
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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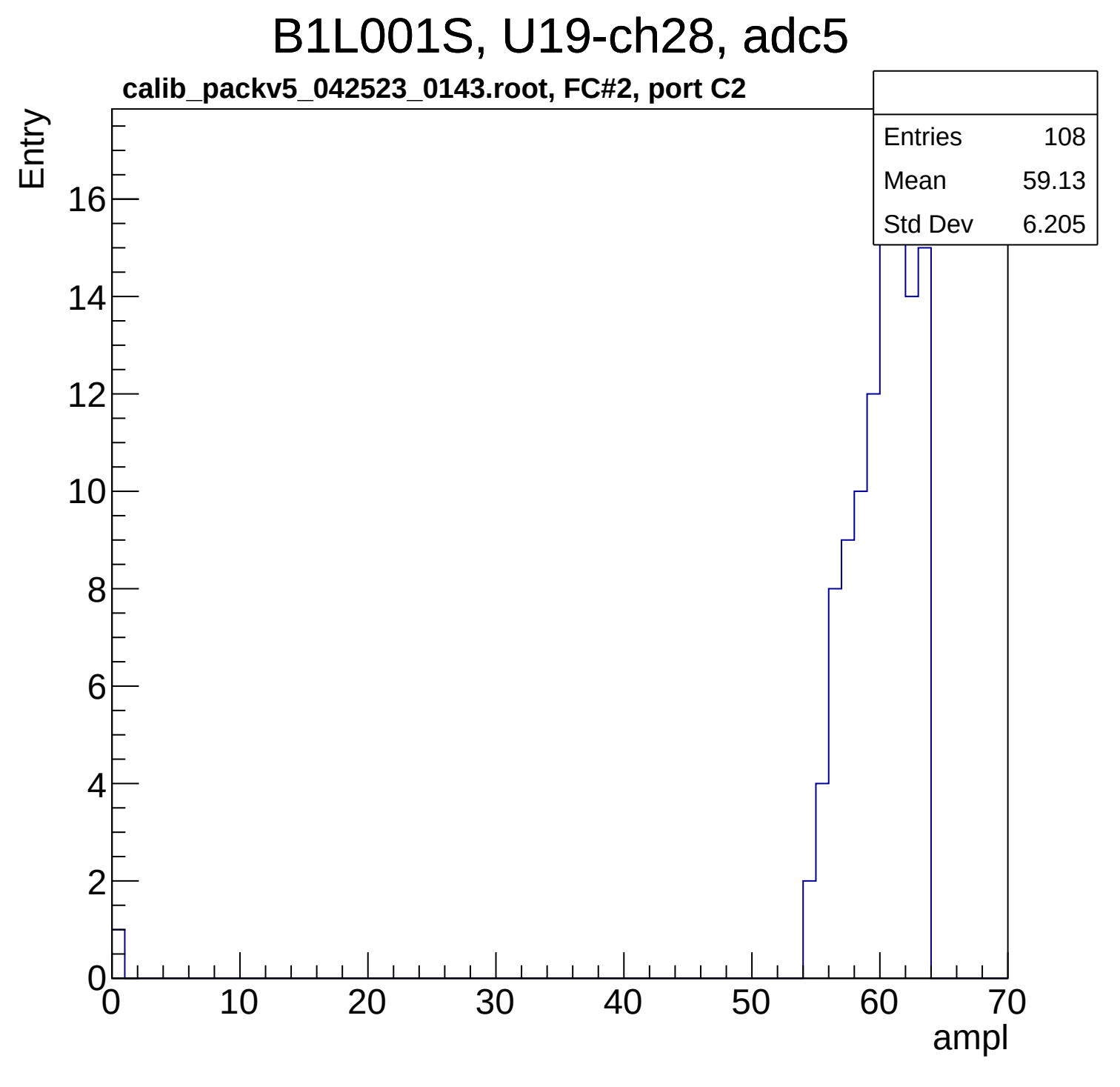
60
70


B1L001S, U19-ch28, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 108
Mean 59.13
Std Dev 6.205
Entry
ampl
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2
4
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10
12
14
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0
10
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60
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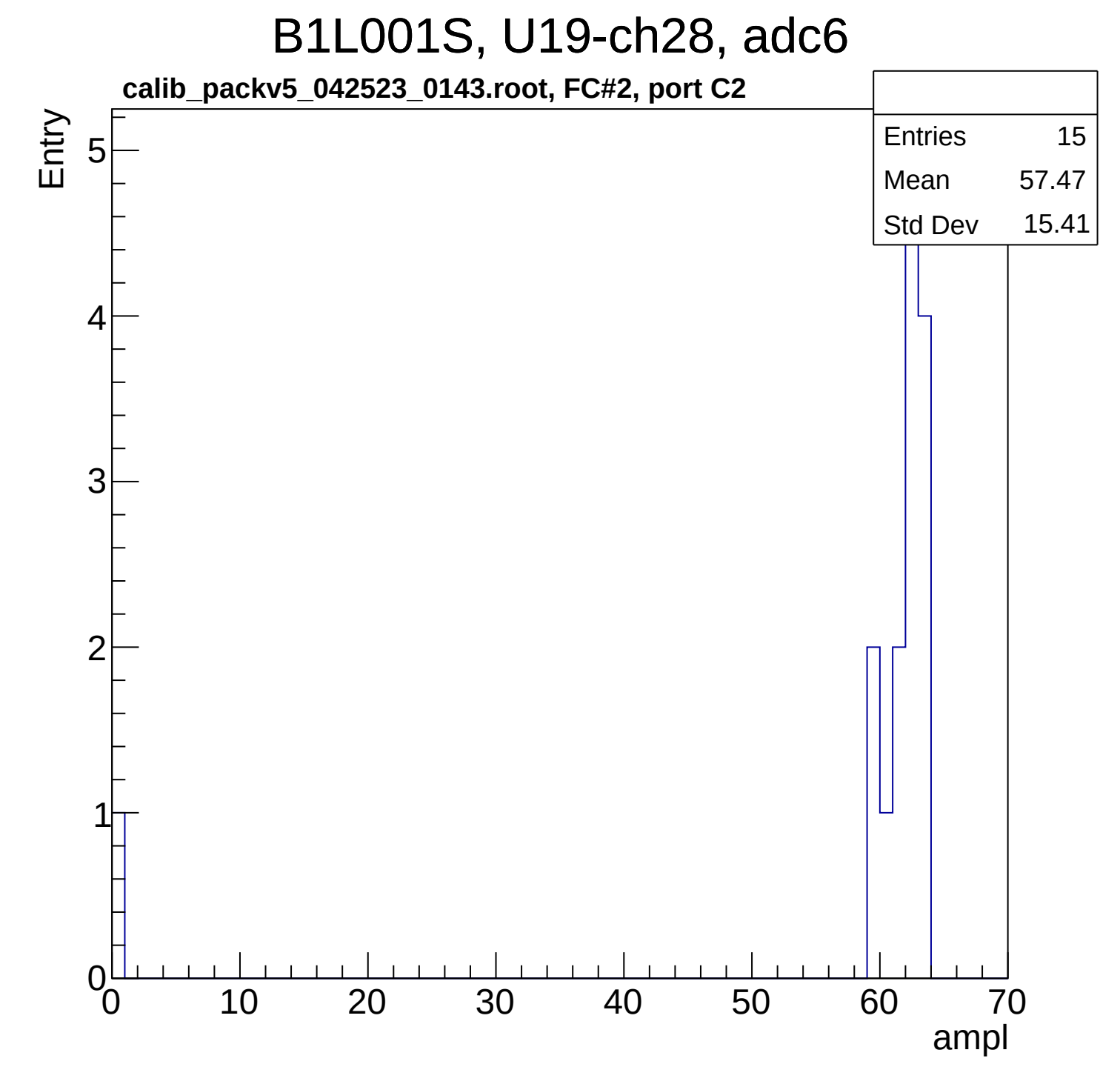
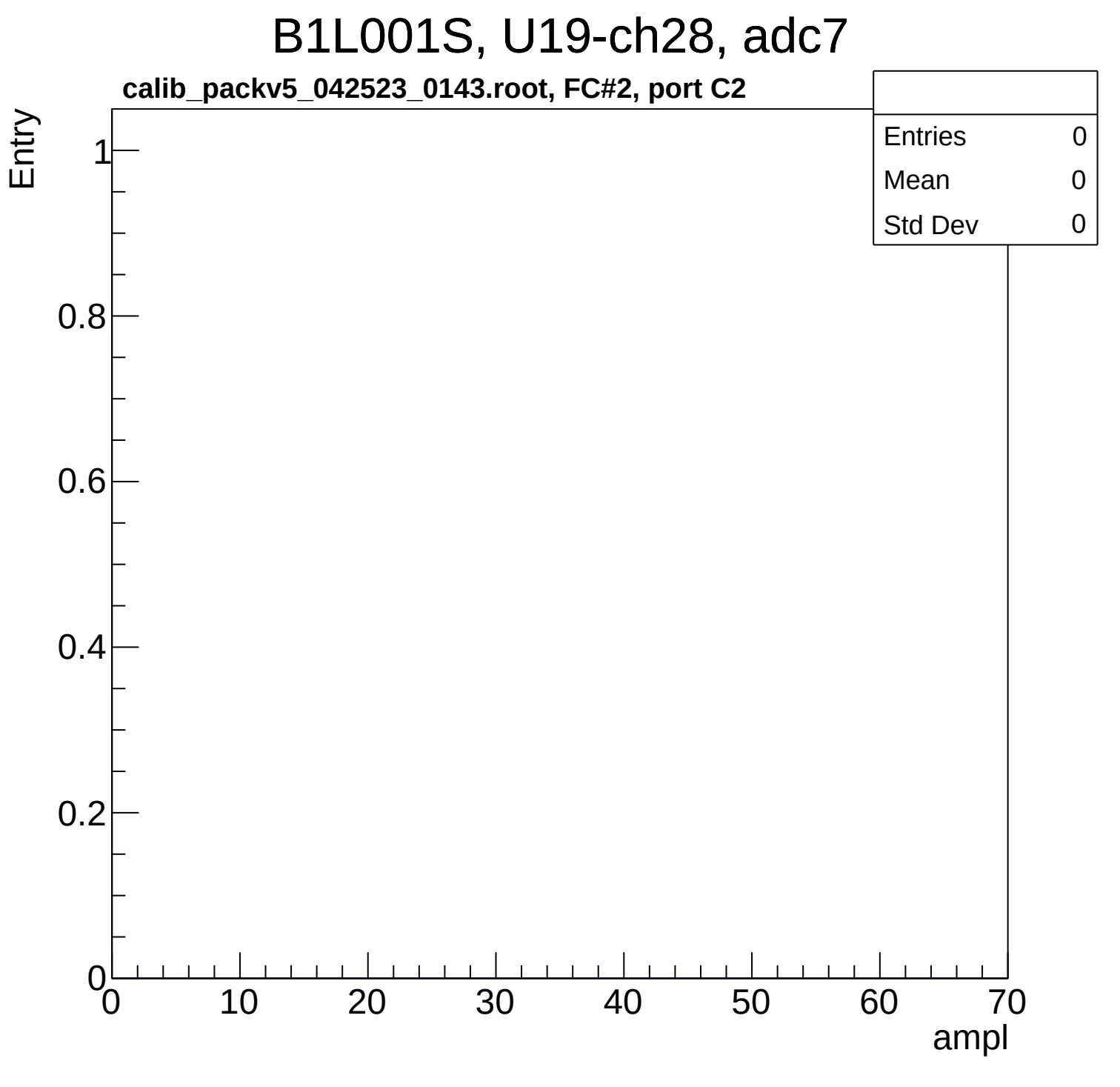

B1L001S, U19-ch28, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 15
Mean 57.47
Std Dev 15.41
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L001S, U19-ch28, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 0
Mean 0
Std Dev 0
Entry
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0.6
0.4
0.2
0
0
10
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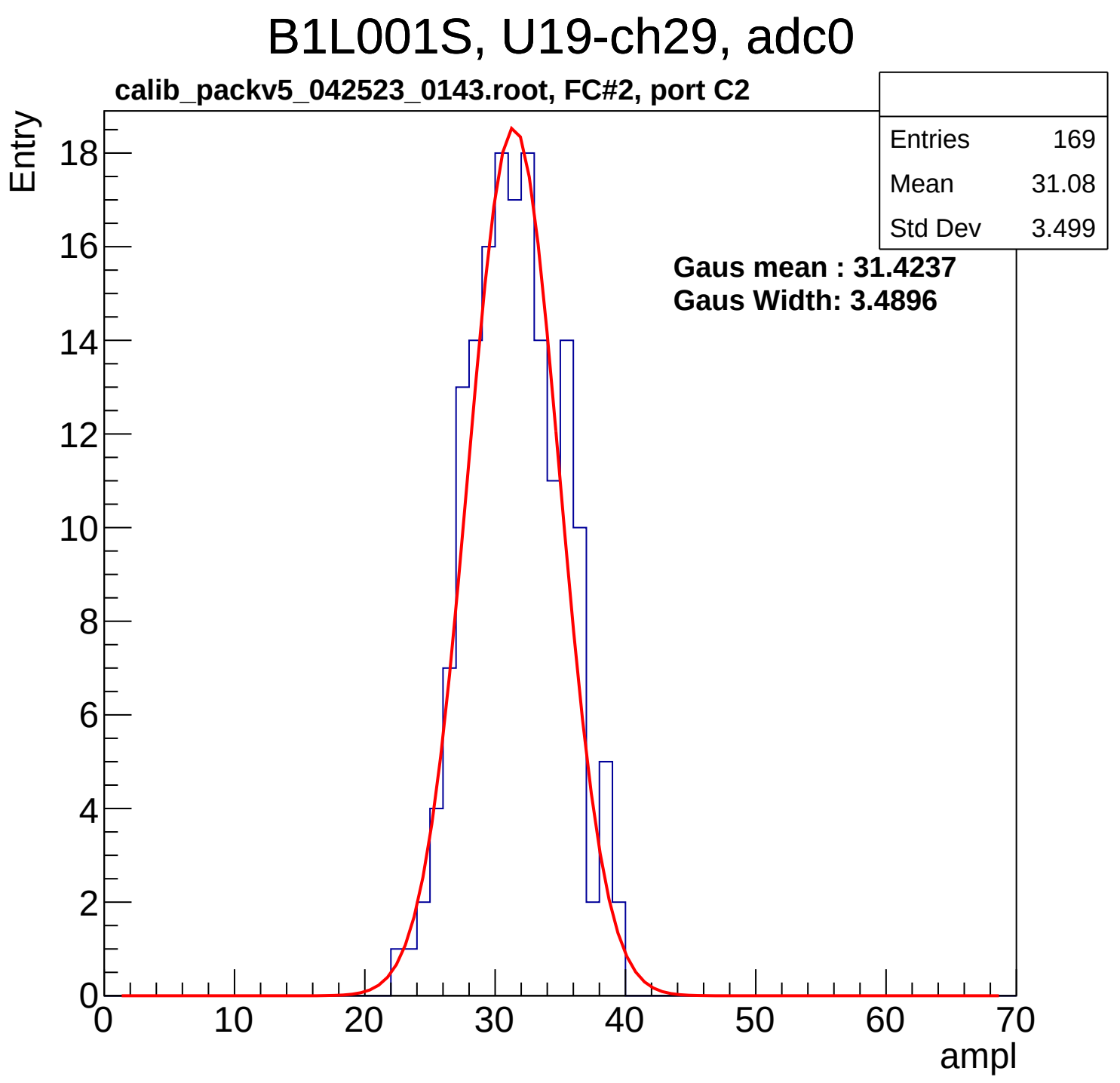
30
40
50
60
70
ampl


B1L001S, U19-ch29, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 169
Mean 31.08
Std Dev 3.499
Gaus mean : 31.4237
Gaus Width: 3.4896
Entry
ampl
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4
6
8
10
12
14
16
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0
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20
30
40
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60
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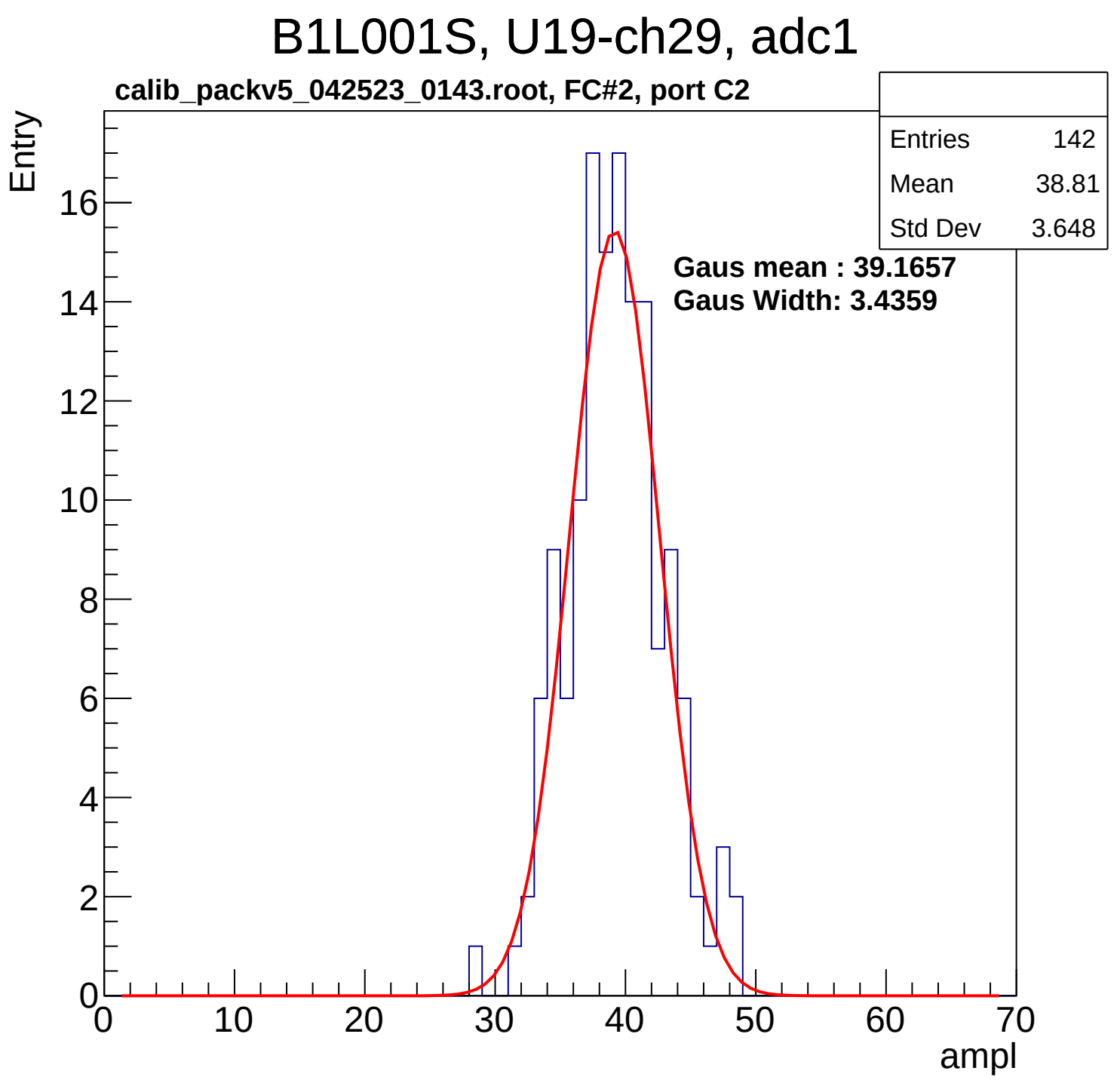
B1L001S, U19-ch29, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 142
Mean 38.81
Std Dev 3.648
Gaus mean : 39.1657
Gaus Width: 3.4359
Entry
ampl
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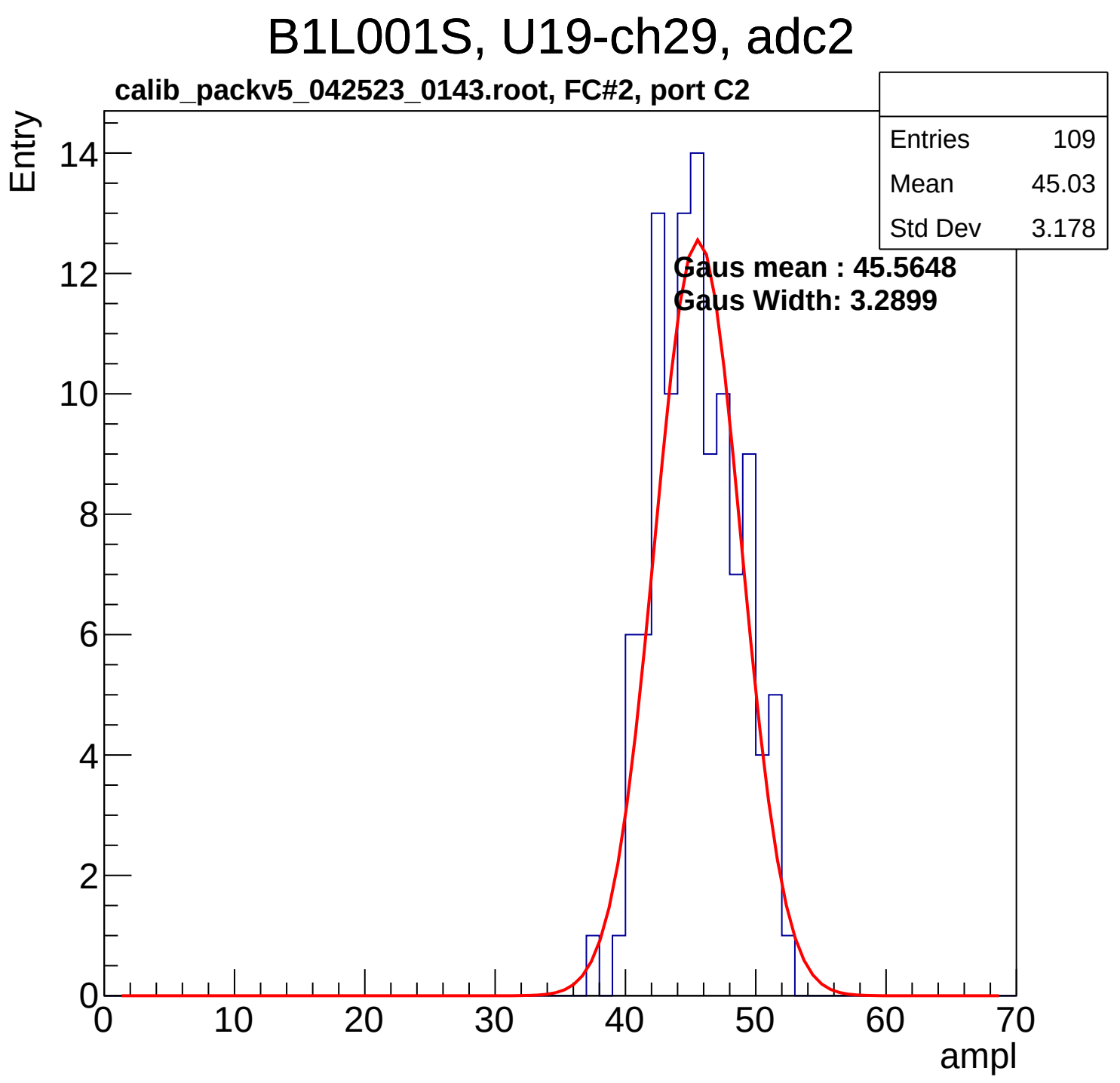
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70


B1L001S, U19-ch29, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 109
Mean 45.03
Std Dev 3.178
Gaus mean : 45.5648
Gaus Width: 3.2899
Entry
ampl
0
2
4
6
8
10
12
14
0
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40
50
60
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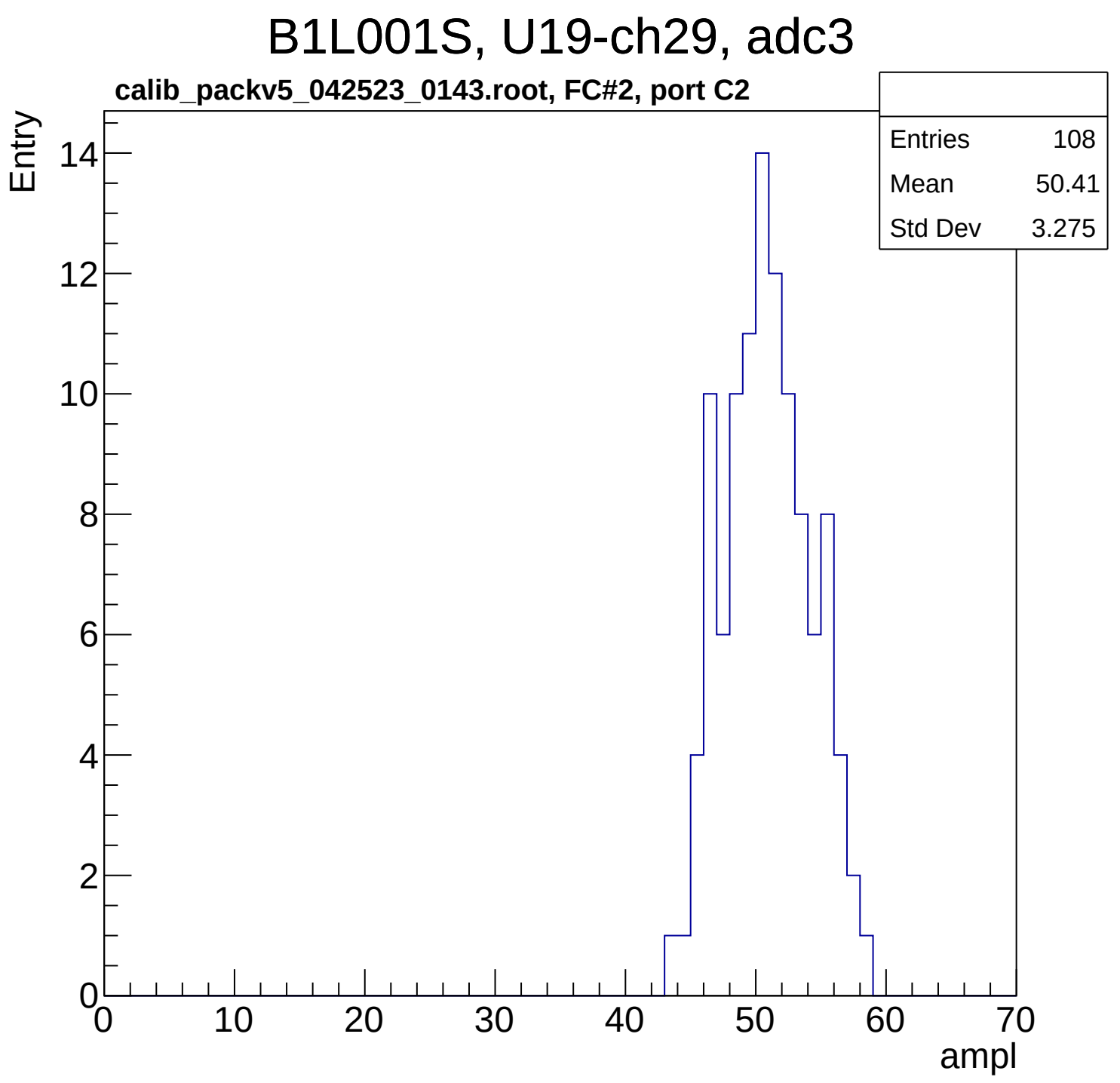
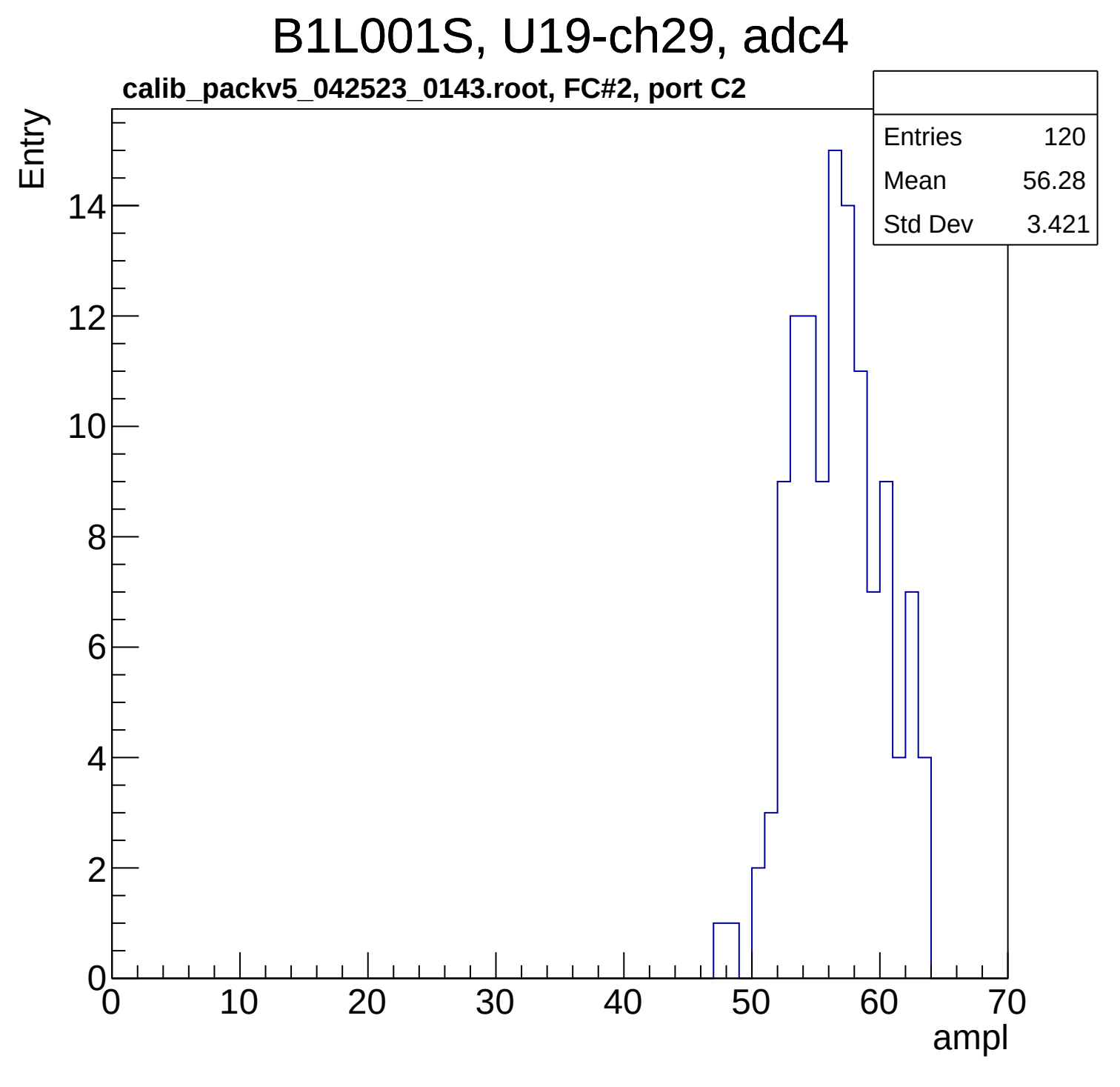

B1L001S, U19-ch29, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 108
Mean 50.41
Std Dev 3.275
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L001S, U19-ch29, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 120
Mean 56.28
Std Dev 3.421
Entry
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2
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6
8
10
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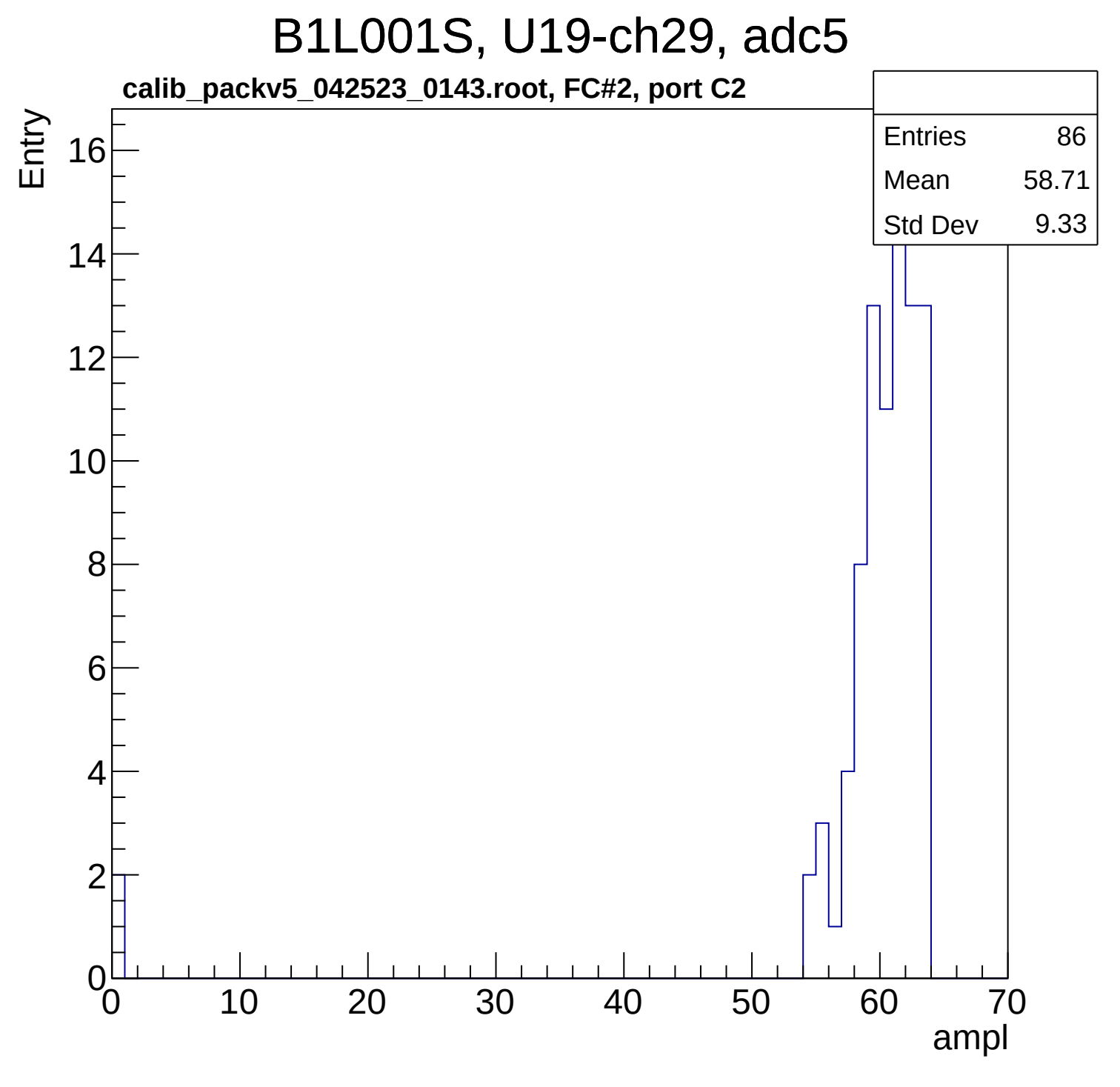
14
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch29, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 86
Mean 58.71
Std Dev 9.33
Entry
ampl
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2
4
6
8
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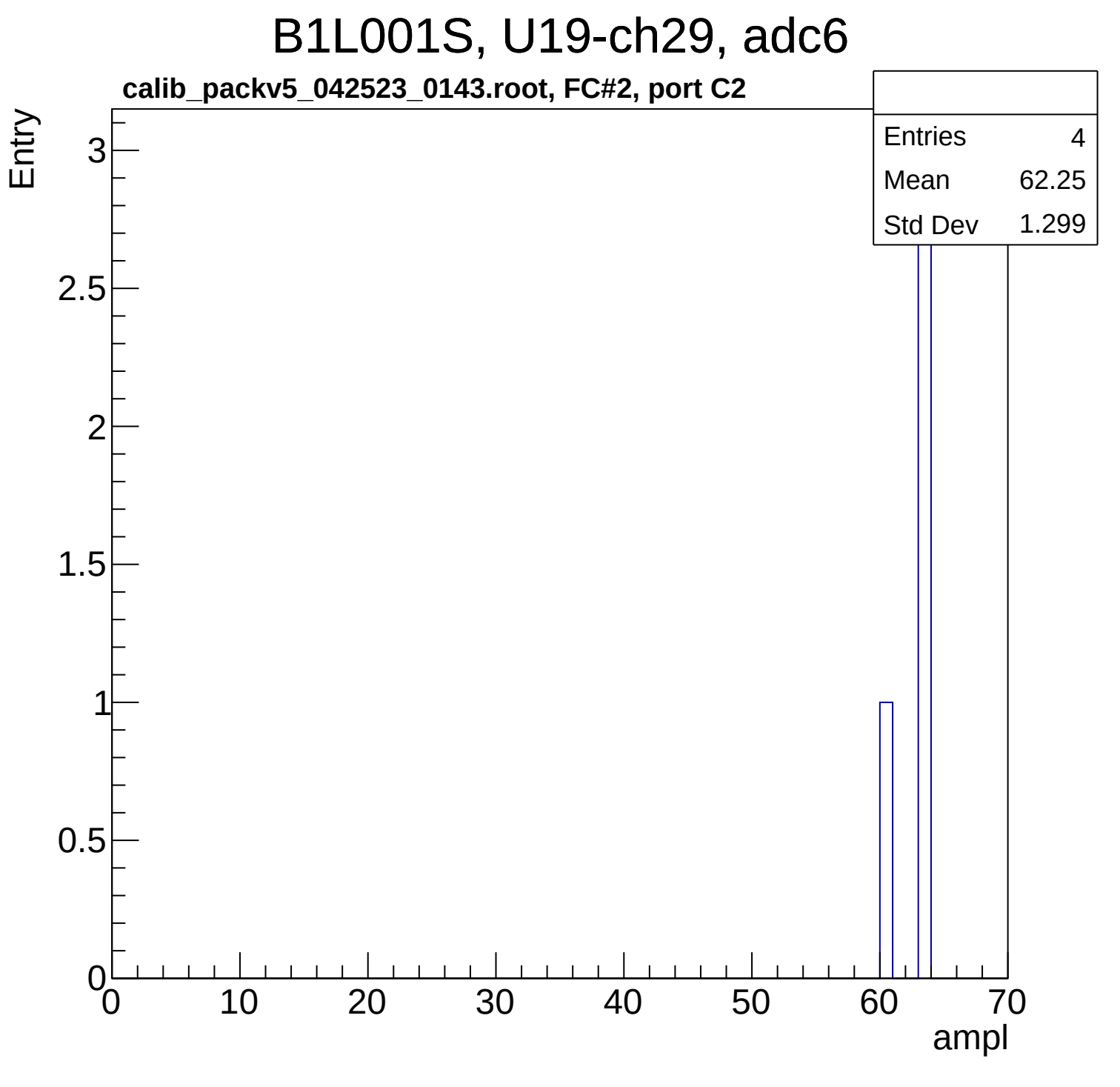
B1L001S, U19-ch29, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 4
Mean 62.25
Std Dev 1.299
Entry
ampl
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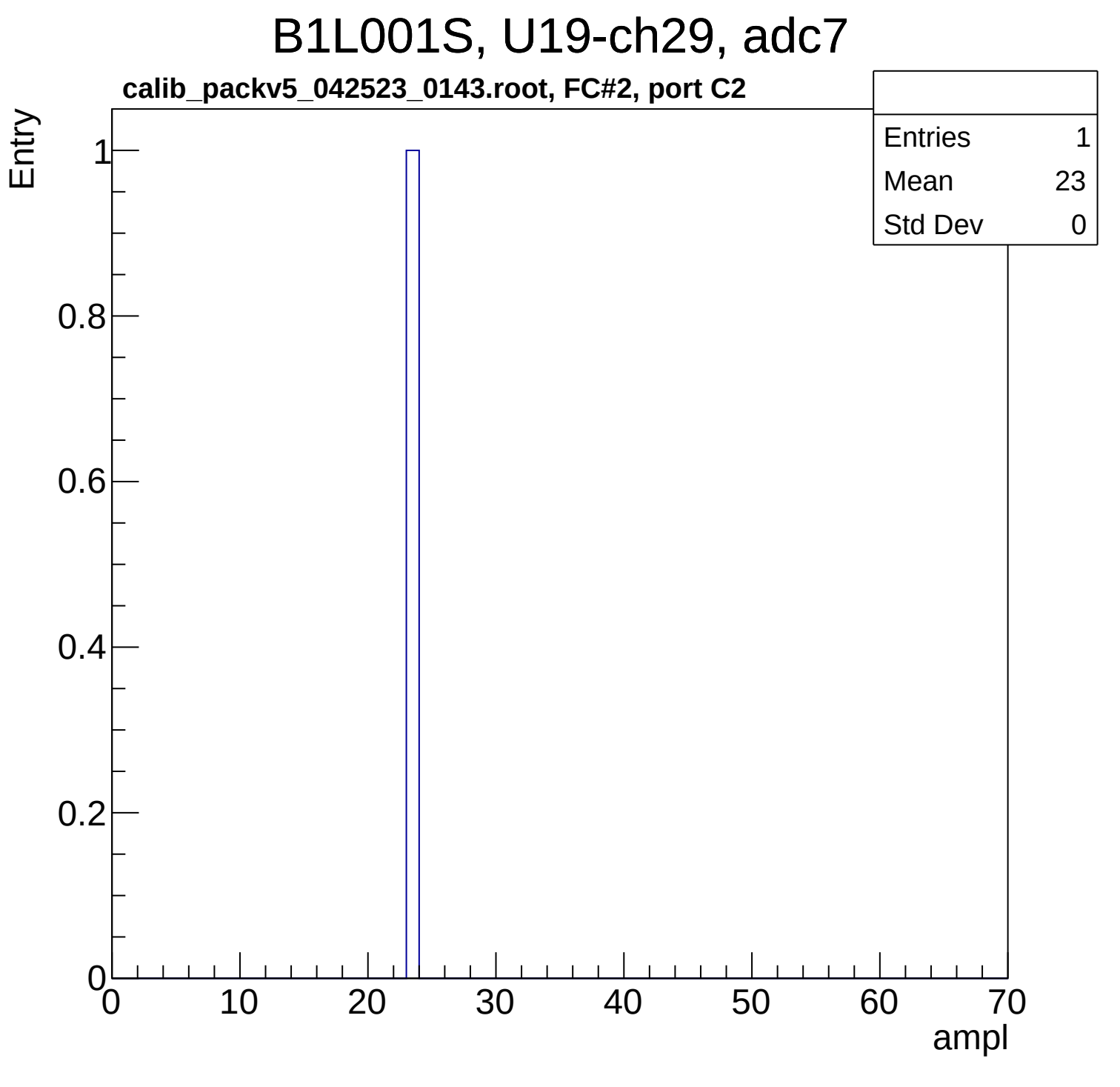
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L001S, U19-ch29, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 23
Std Dev 0
Entry
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0.6
0.4
0.2
0
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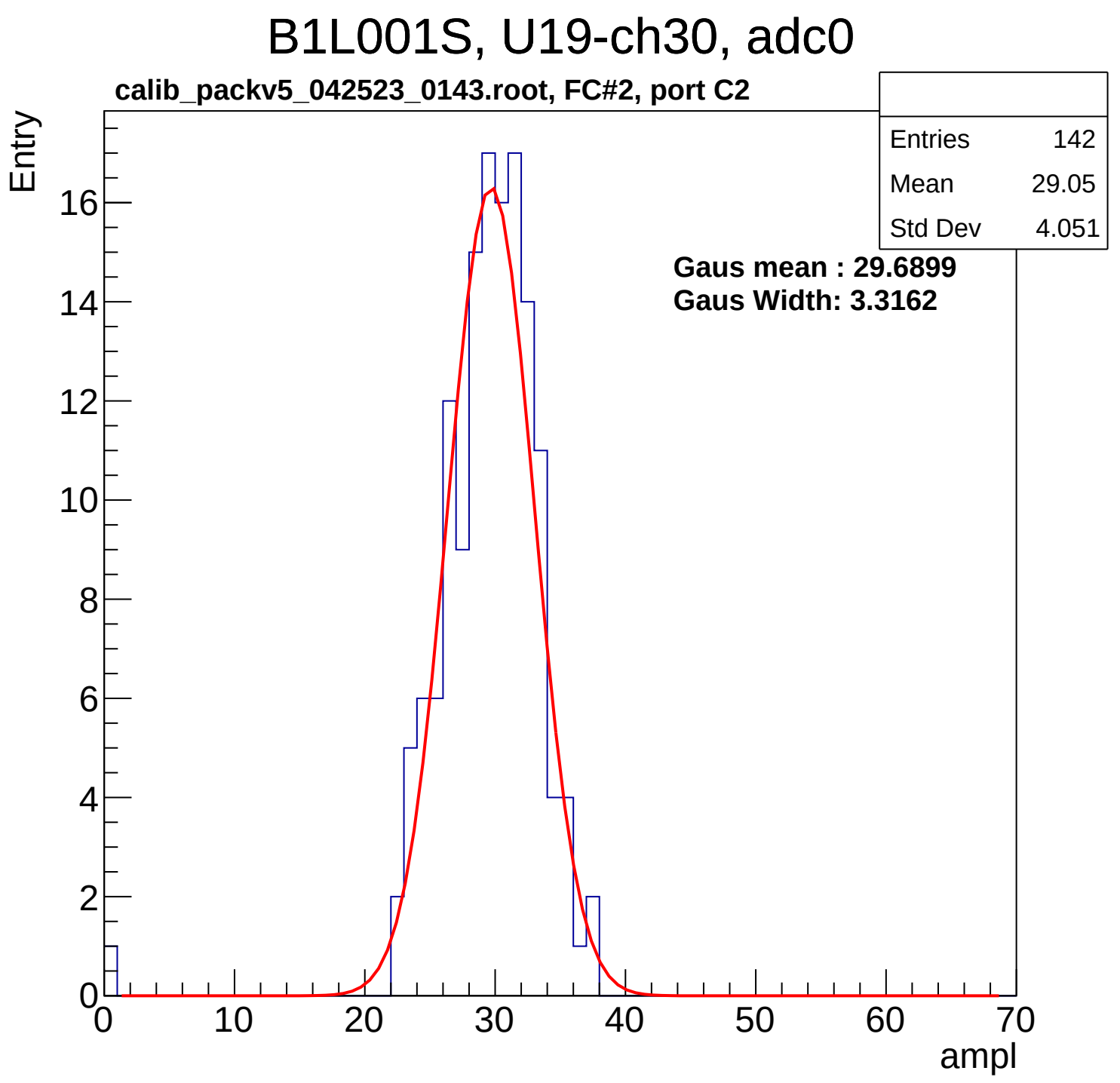
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch30, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 142
Mean 29.05
Std Dev 4.051
Gaus mean : 29.6899
Gaus Width: 3.3162
Entry
ampl
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2
4
6
8
10
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16
0
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40
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60
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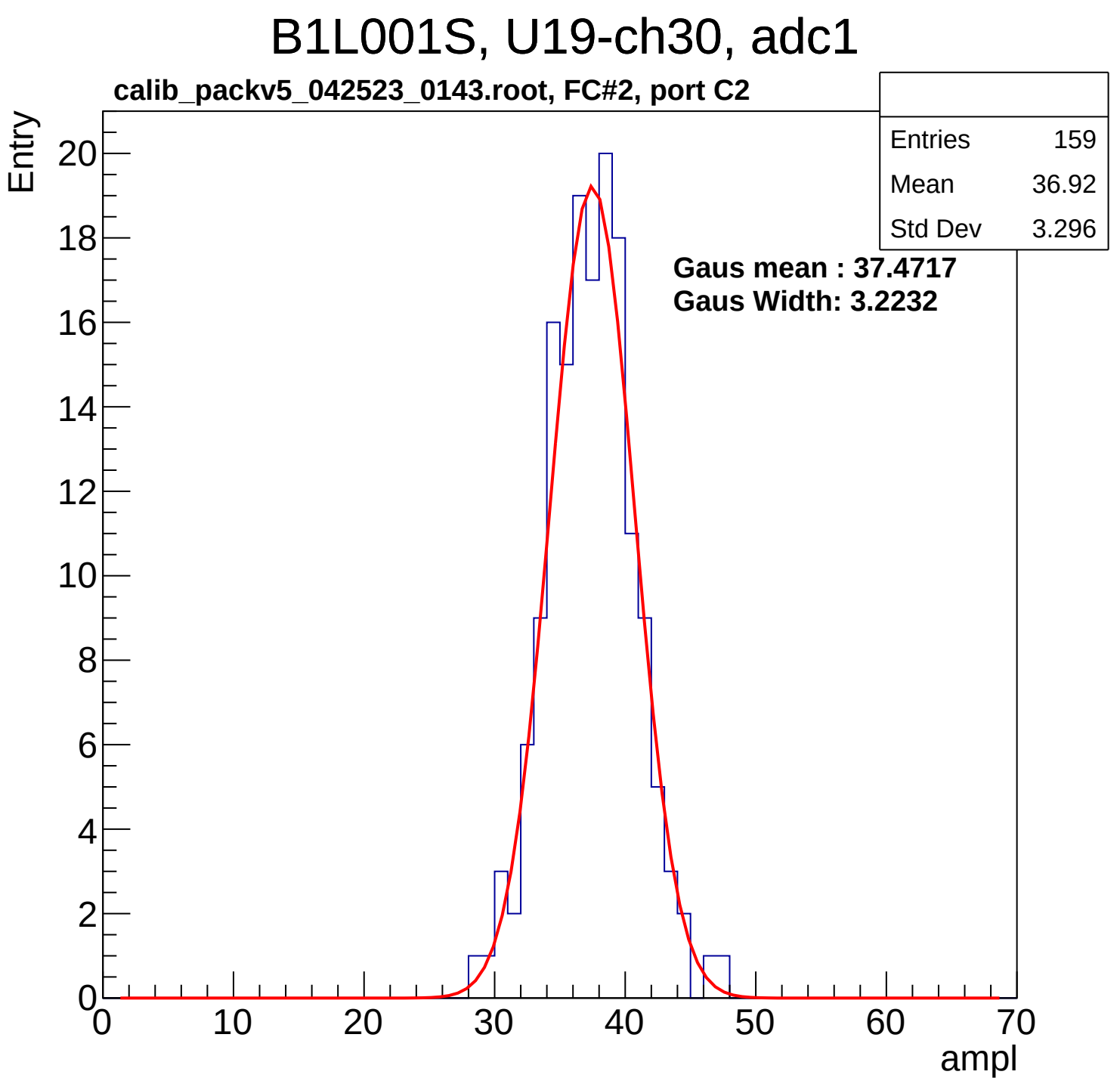
B1L001S, U19-ch30, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 159
Mean 36.92
Std Dev 3.296
Gaus mean : 37.4717
Gaus Width: 3.2232
Entry
ampl
0
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4
6
8
10
12
14
16
18
20
0
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20
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40
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60
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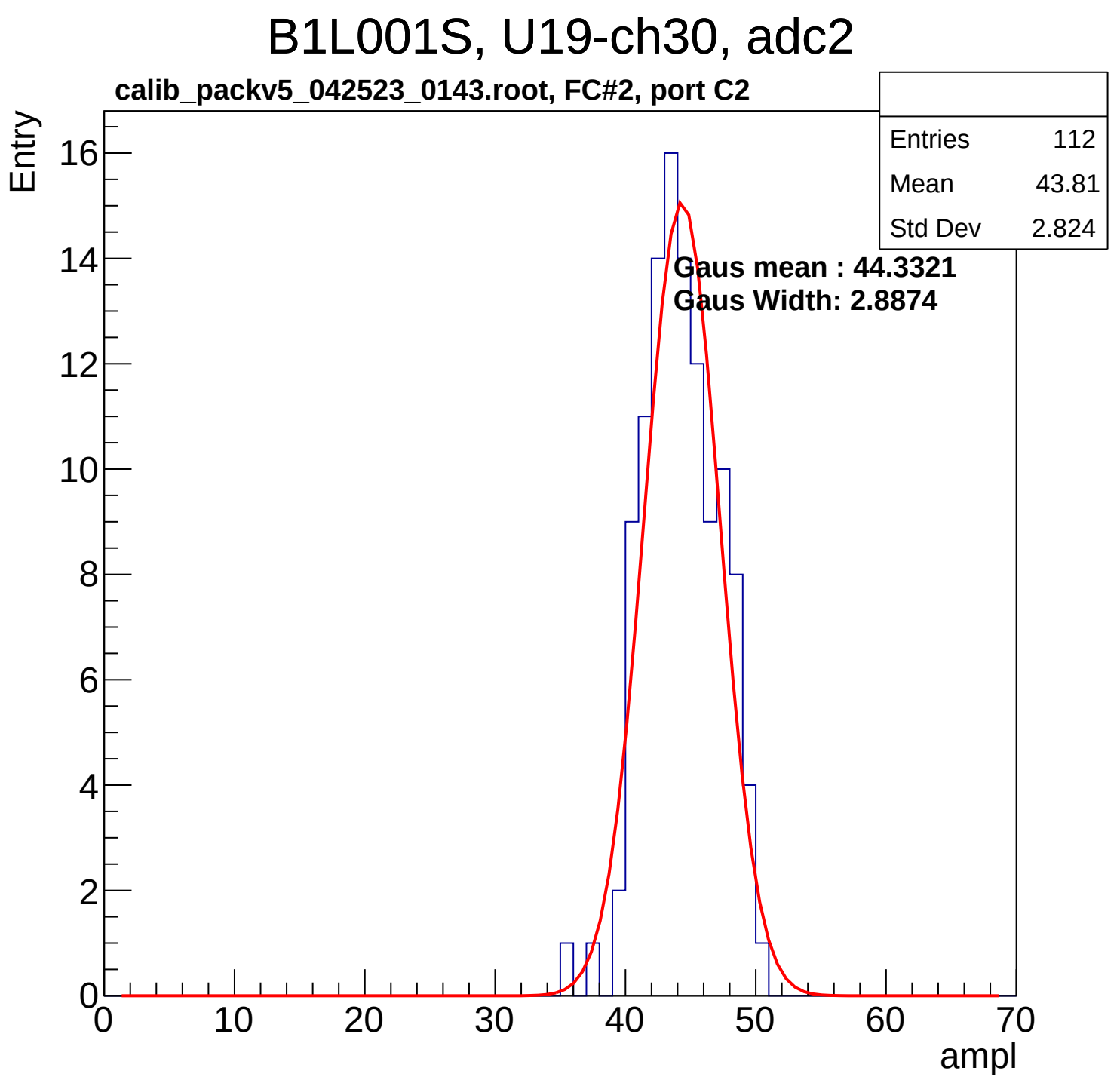
B1L001S, U19-ch30, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 112
Mean 43.81
Std Dev 2.824
Gaus mean : 44.3321
Gaus Width: 2.8874
Entry
ampl
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2
4
6
8
10
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14
16
0
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60
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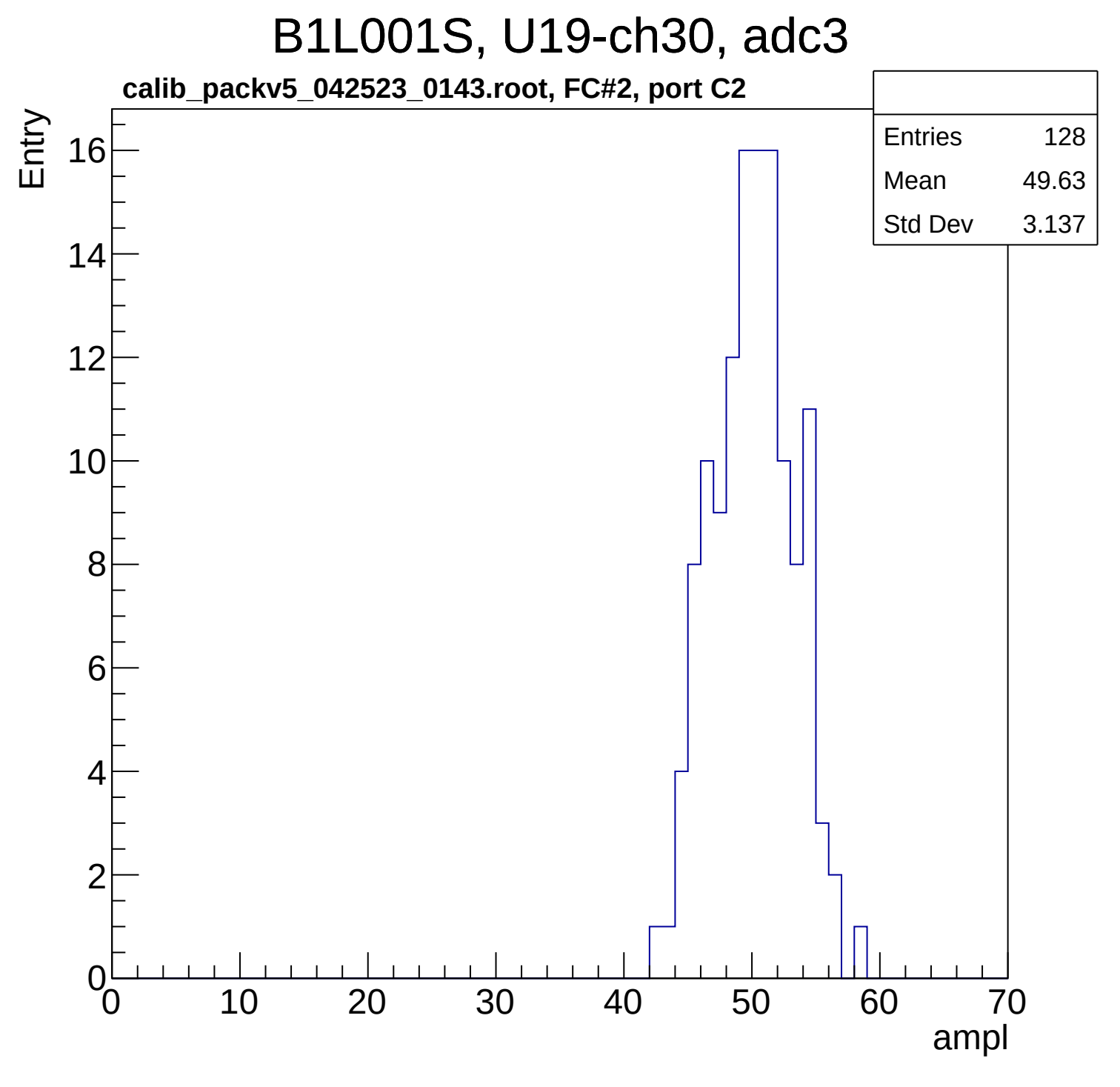
B1L001S, U19-ch30, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 128
Mean 49.63
Std Dev 3.137
Entry
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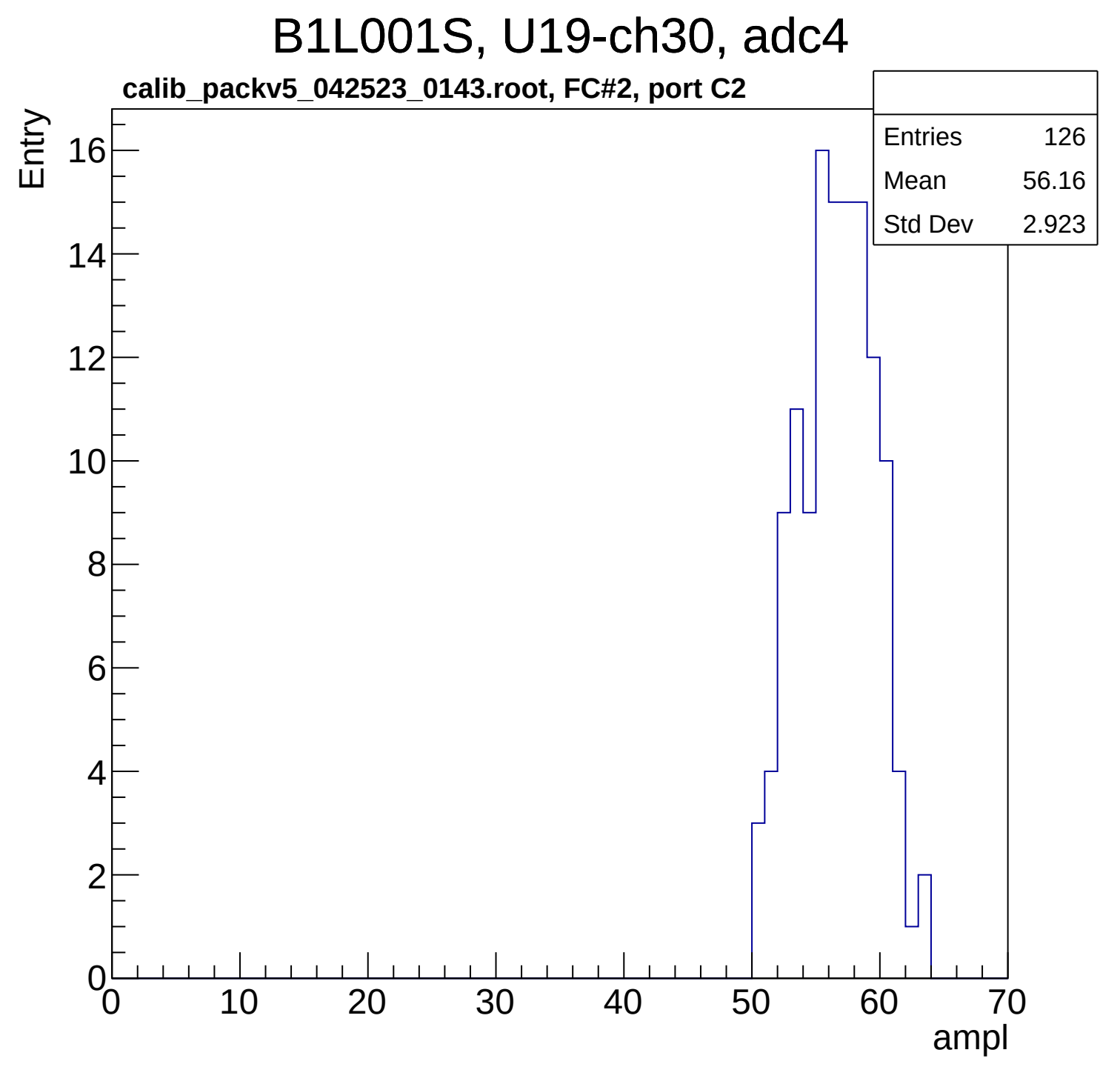
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch30, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 126
Mean 56.16
Std Dev 2.923
Entry
ampl
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2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
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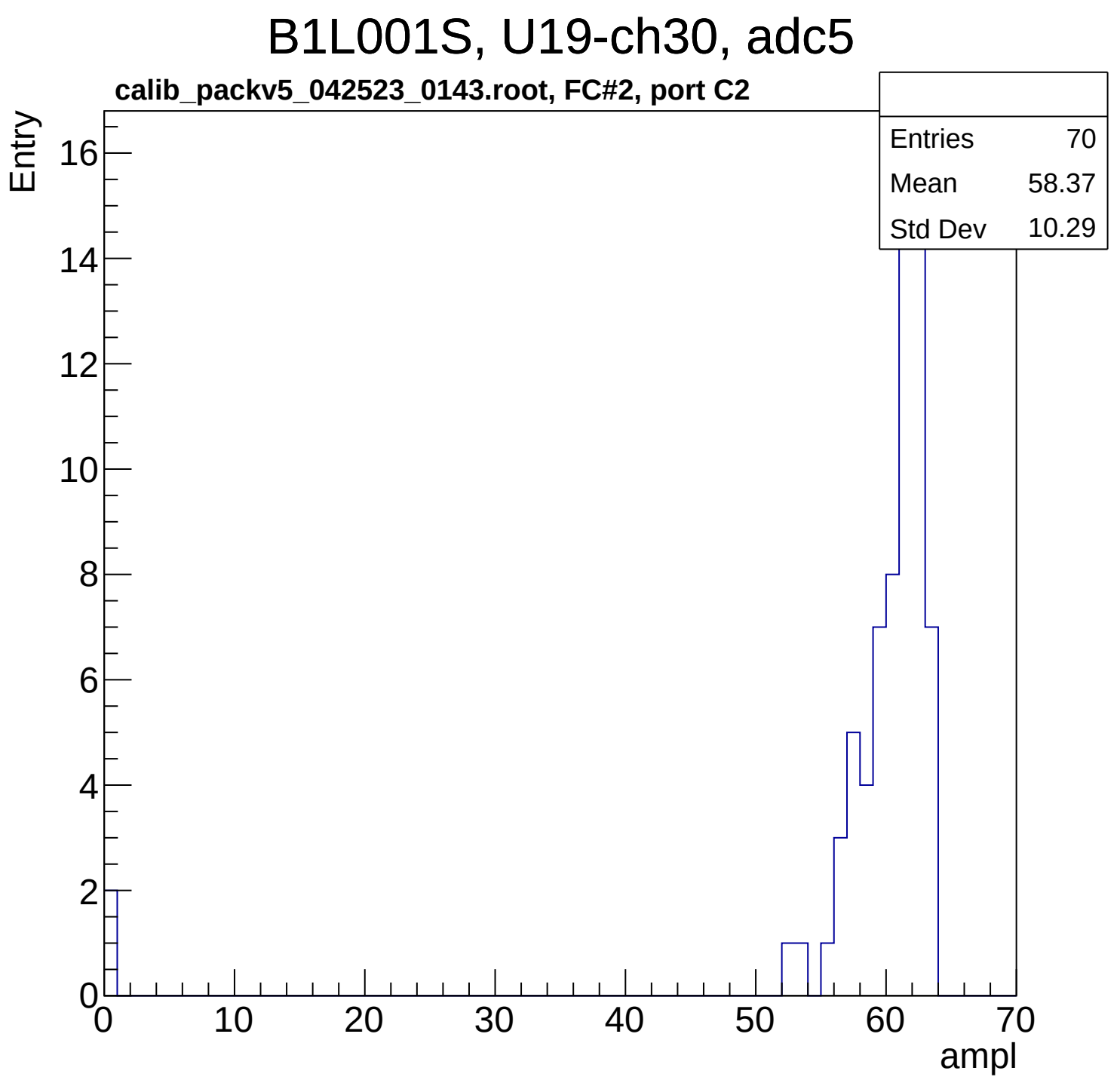
B1L001S, U19-ch30, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 70
Mean 58.37
Std Dev 10.29
Entry
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10
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16
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10
20
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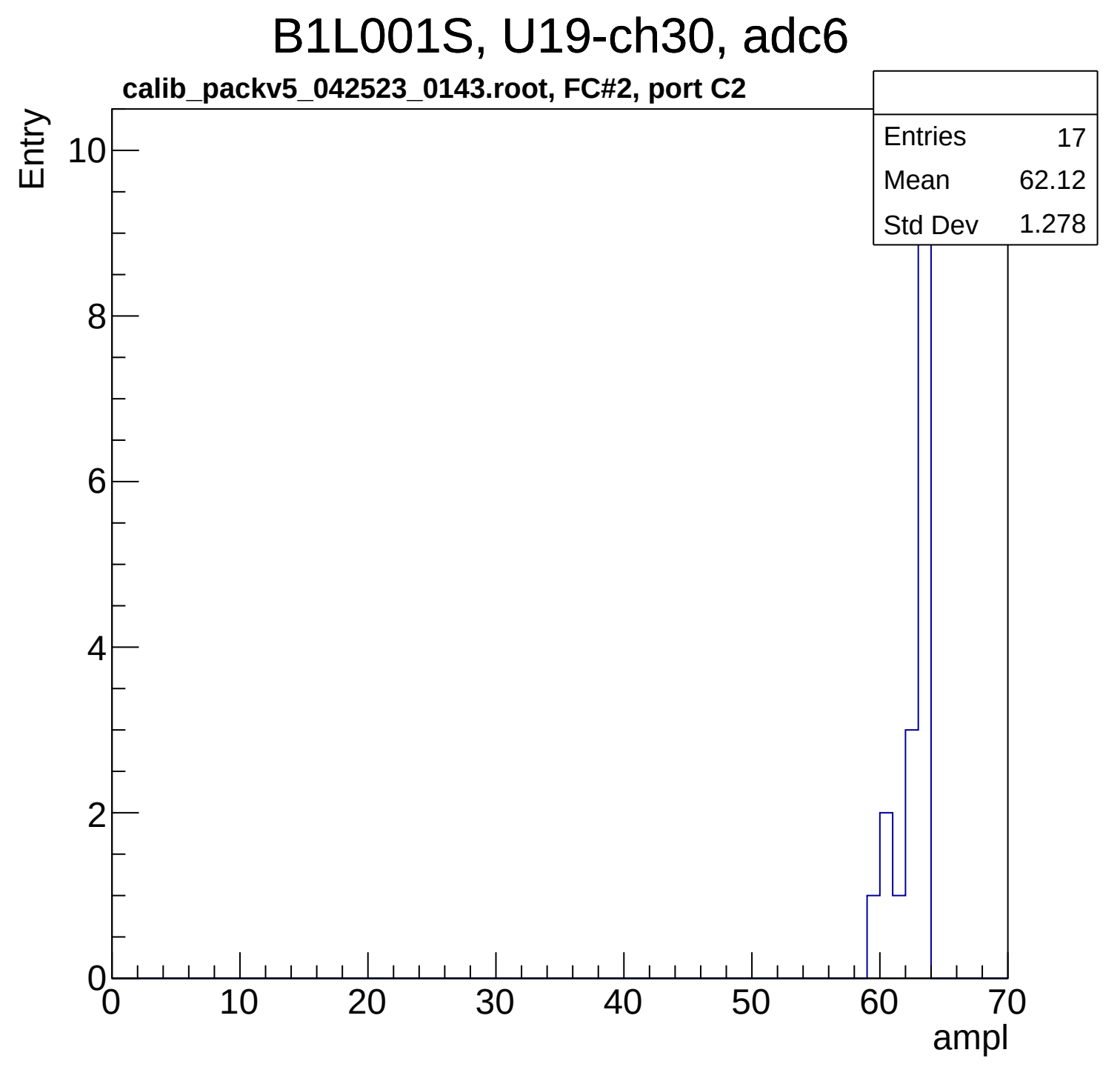
50
60
70
ampl


B1L001S, U19-ch30, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 17
Mean 62.12
Std Dev 1.278
Entry
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2
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6
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10
0
10
20
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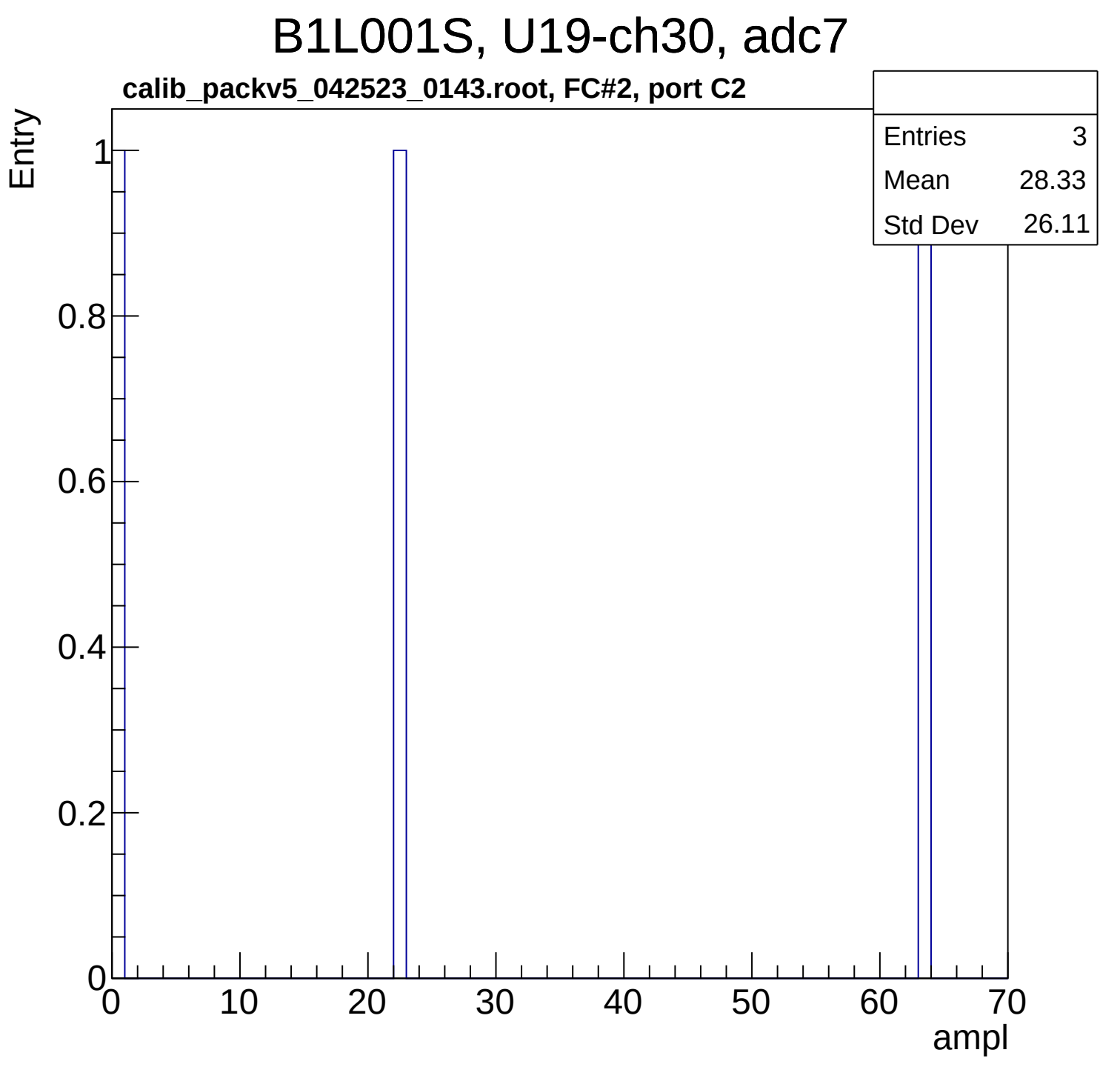
50
60
70
ampl


B1L001S, U19-ch30, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 3
Mean 28.33
Std Dev 26.11
Entry
ampl
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0.4
0.6
0.8
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0
10
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60
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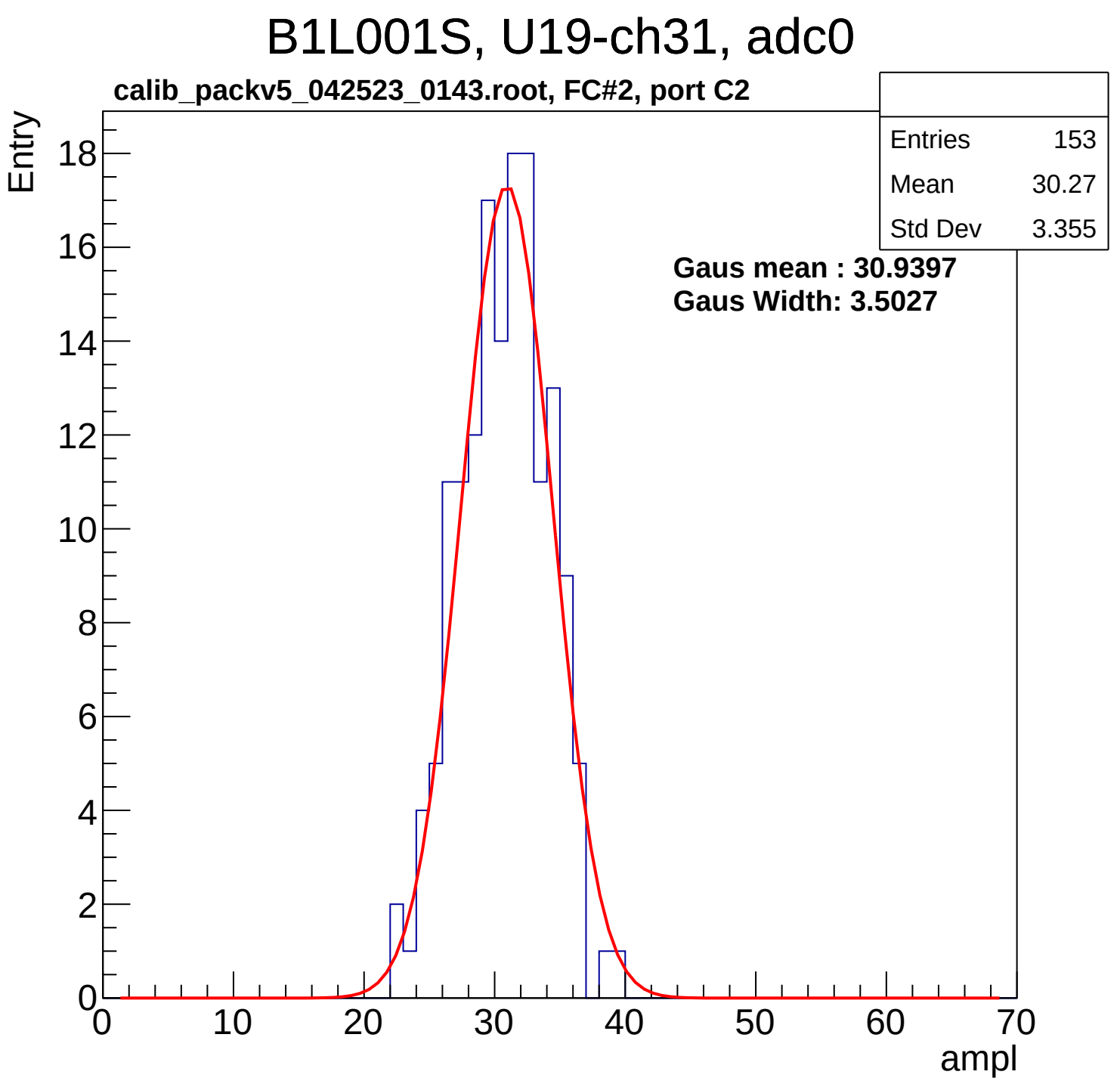
B1L001S, U19-ch31, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 153
Mean 30.27
Std Dev 3.355
Gaus mean : 30.9397
Gaus Width: 3.5027
Entry
ampl
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4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
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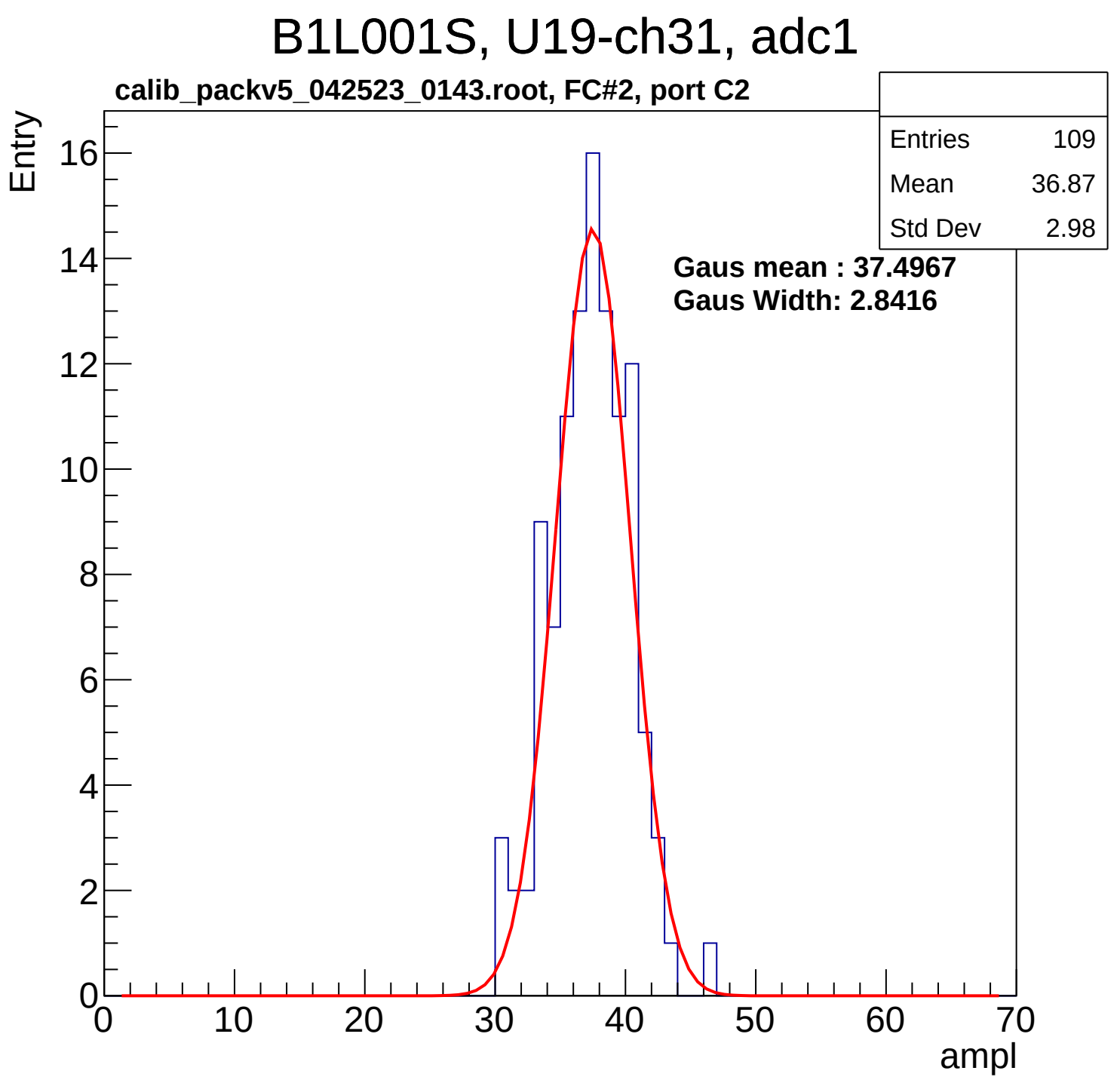
B1L001S, U19-ch31, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 109
Mean 36.87
Std Dev 2.98
Gaus mean : 37.4967
Gaus Width: 2.8416
Entry
ampl
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2
4
6
8
10
12
14
16
0
10
20
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40
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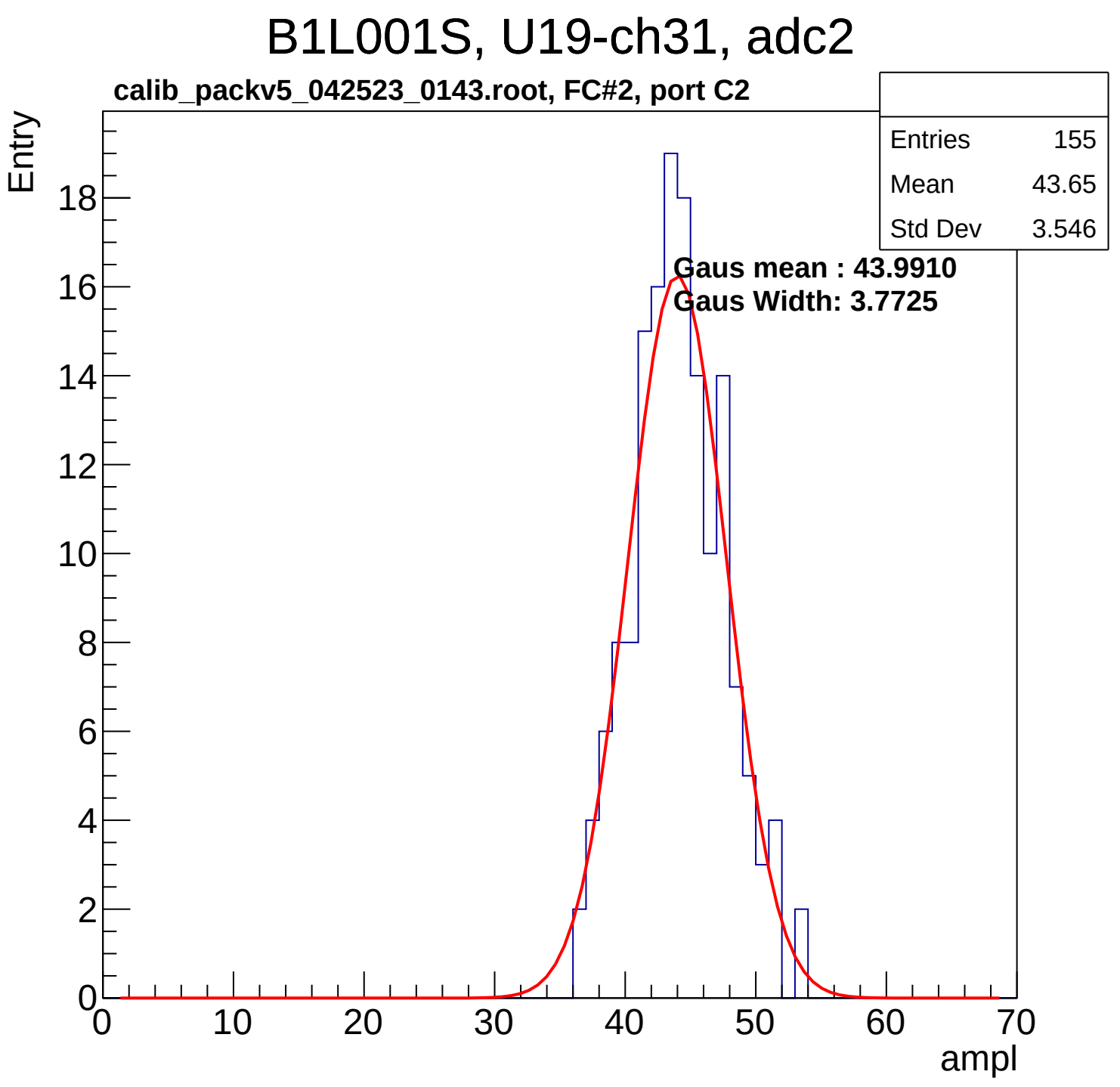
B1L001S, U19-ch31, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 155
Mean 43.65
Std Dev 3.546
Gaus mean : 43.9910
Gaus Width: 3.7725
Entry
ampl
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4
6
8
10
12
14
16
18
0
10
20
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40
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60
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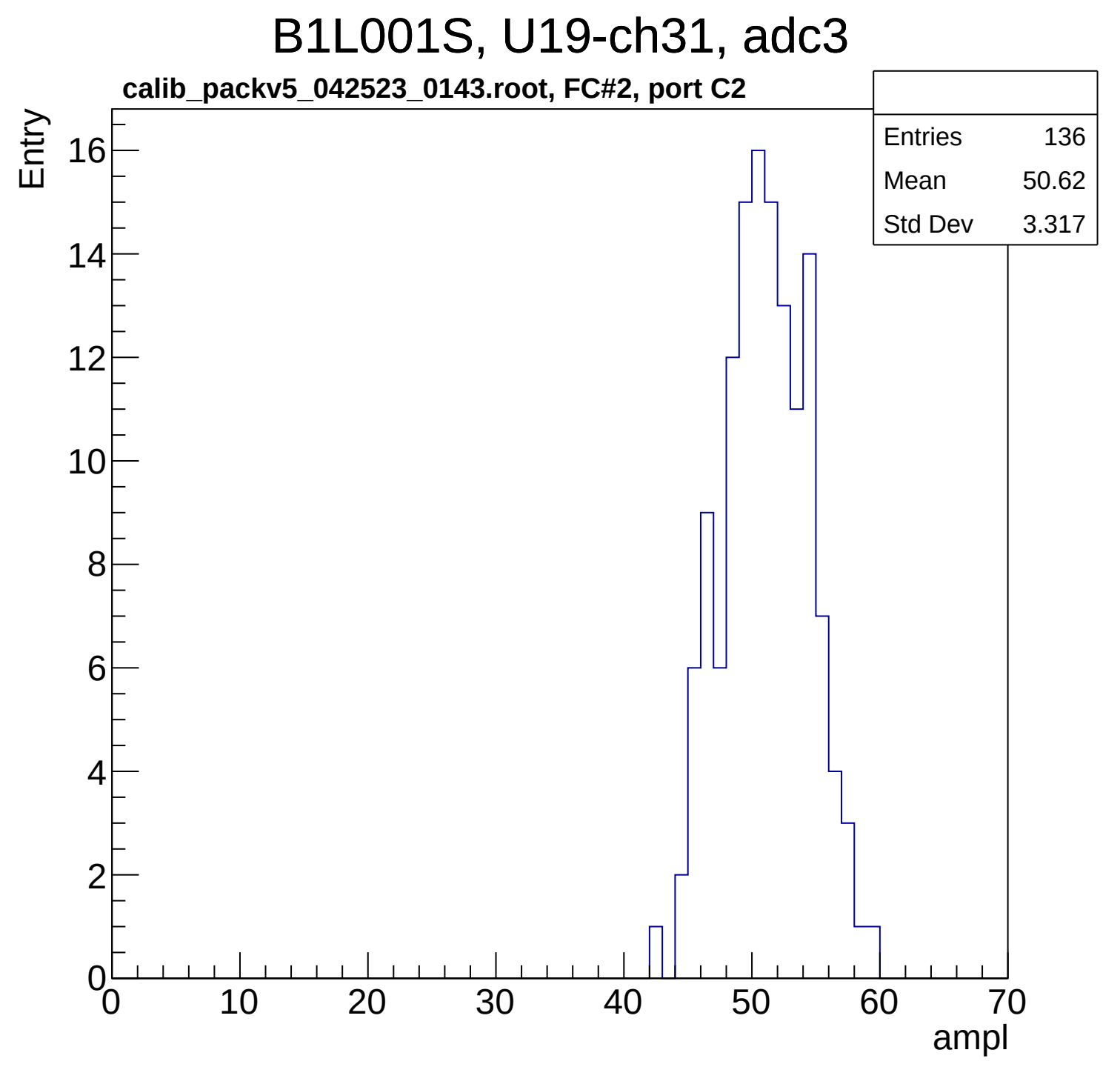
B1L001S, U19-ch31, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 136
Mean 50.62
Std Dev 3.317
Entry
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4
6
8
10
12
14
16
0
10
20
30
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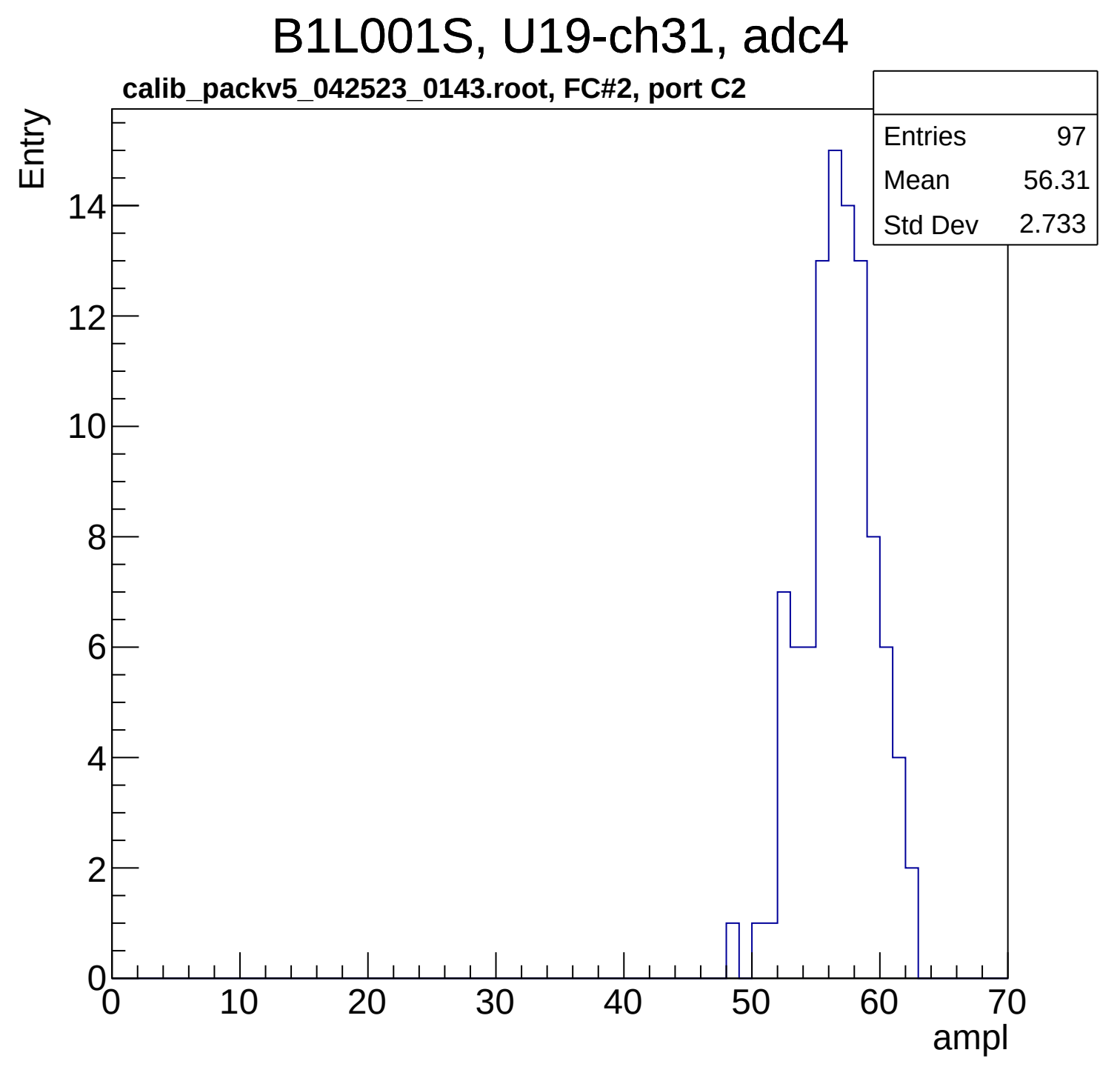
50
60
70
ampl


B1L001S, U19-ch31, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 97
Mean 56.31
Std Dev 2.733
Entry
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2
4
6
8
10
12
14
0
10
20
30
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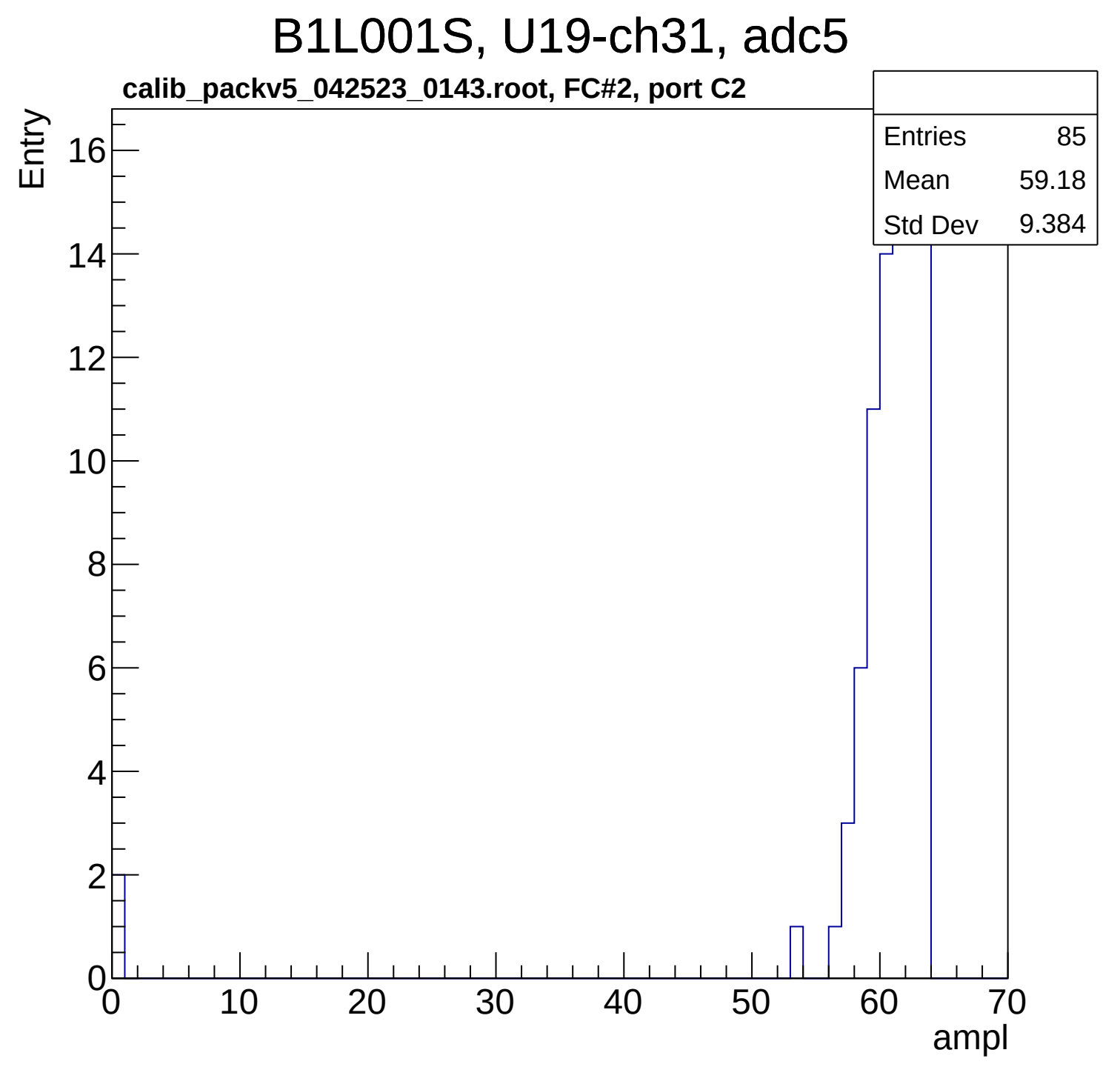
50
60
70
ampl


B1L001S, U19-ch31, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 85
Mean 59.18
Std Dev 9.384
Entry
ampl
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6
8
10
12
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0
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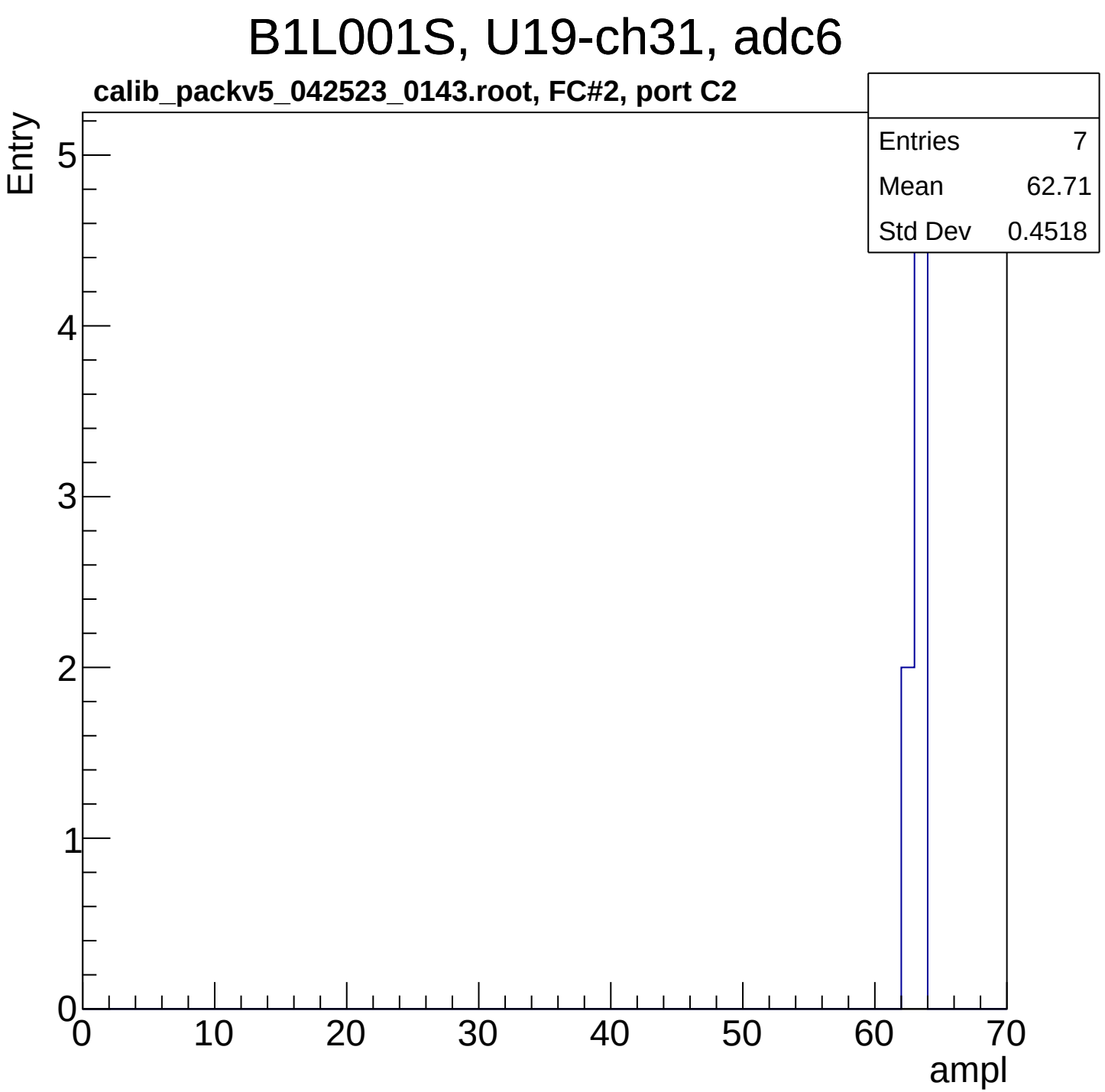
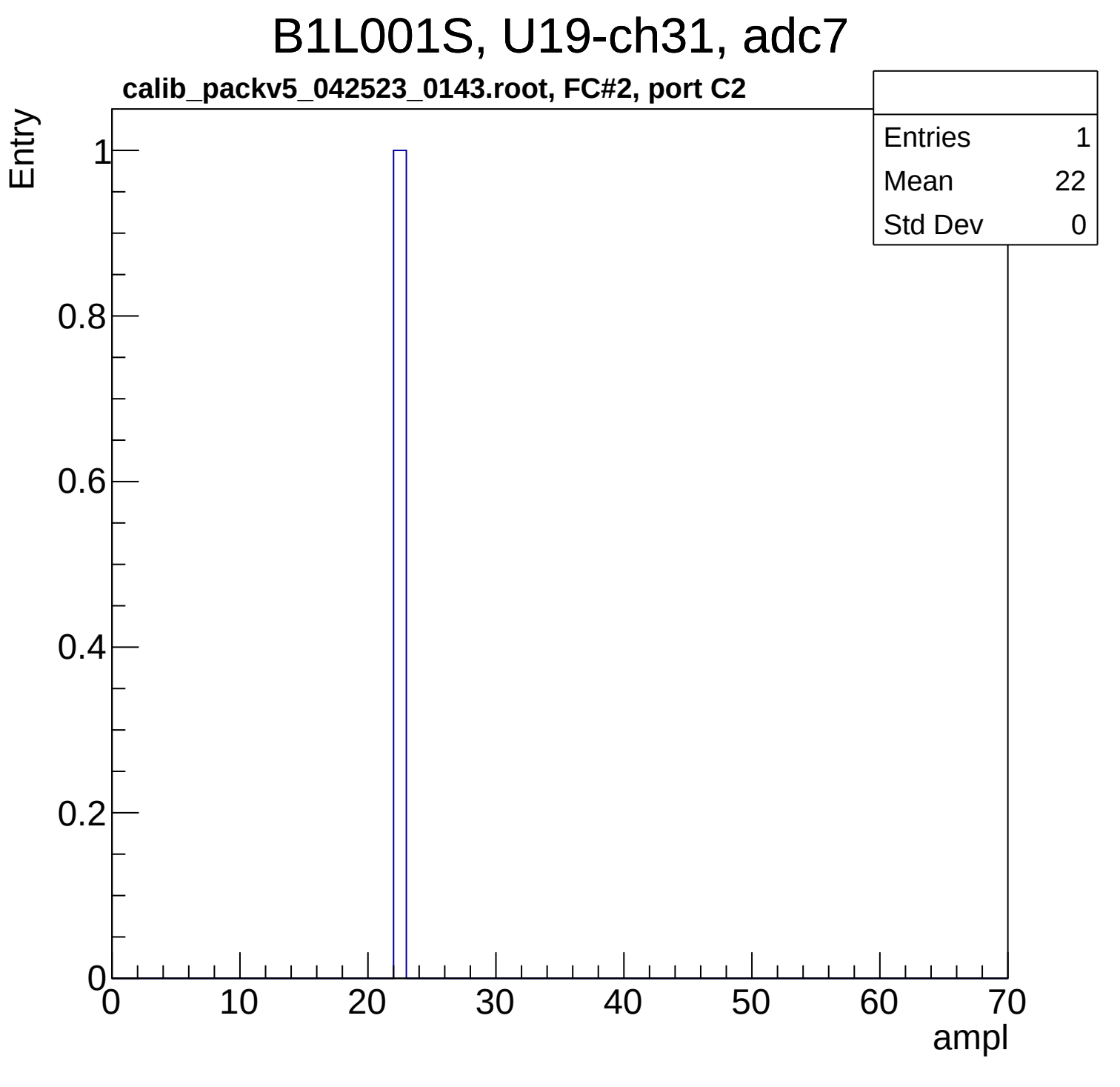

B1L001S, U19-ch31, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 7
Mean 62.71
Std Dev 0.4518
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch31, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 22
Std Dev 0
Entry
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0.6
0.4
0.2
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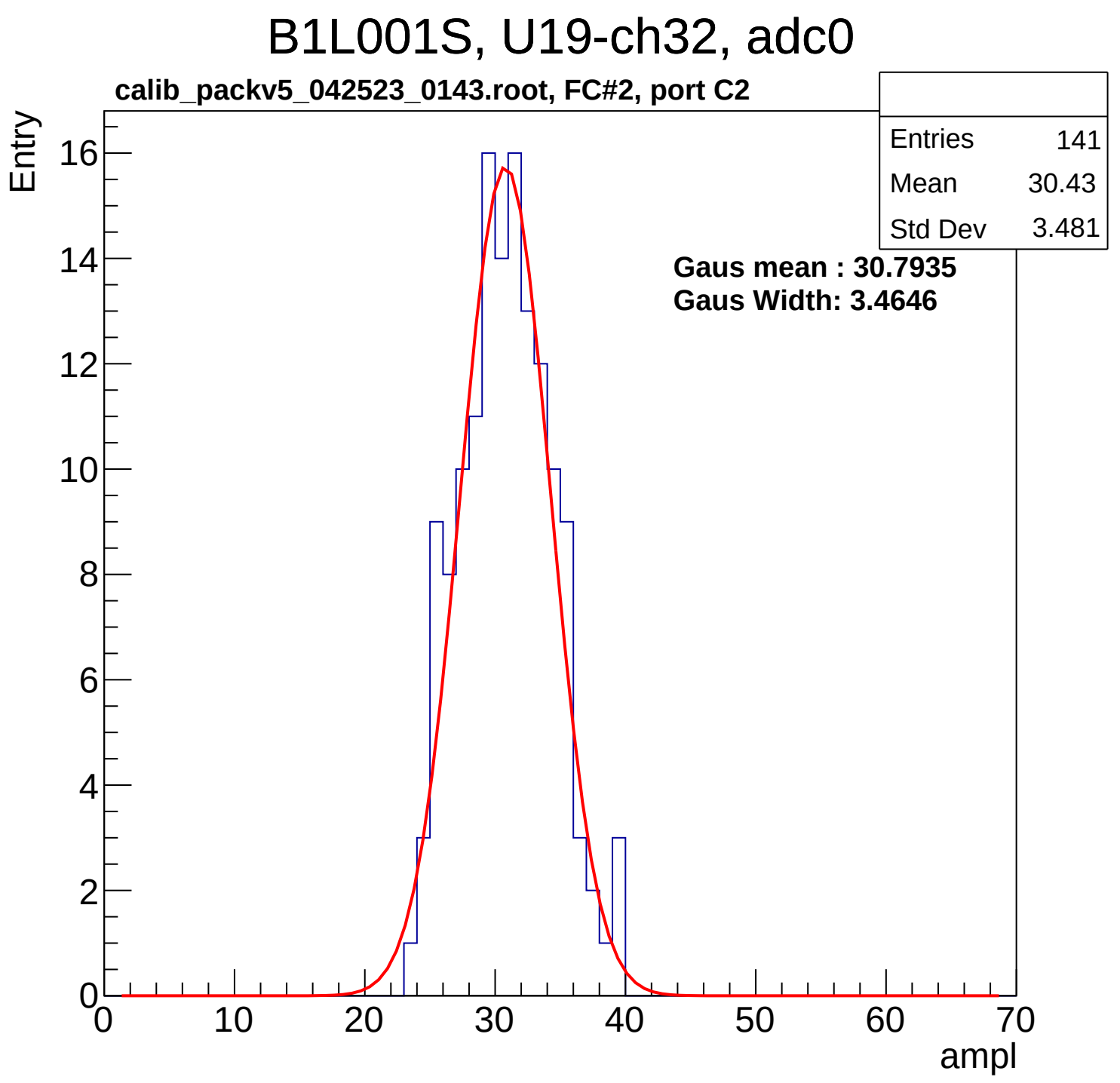
50
60
70
ampl


B1L001S, U19-ch32, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 141
Mean 30.43
Std Dev 3.481
Gaus mean : 30.7935
Gaus Width: 3.4646
Entry
ampl
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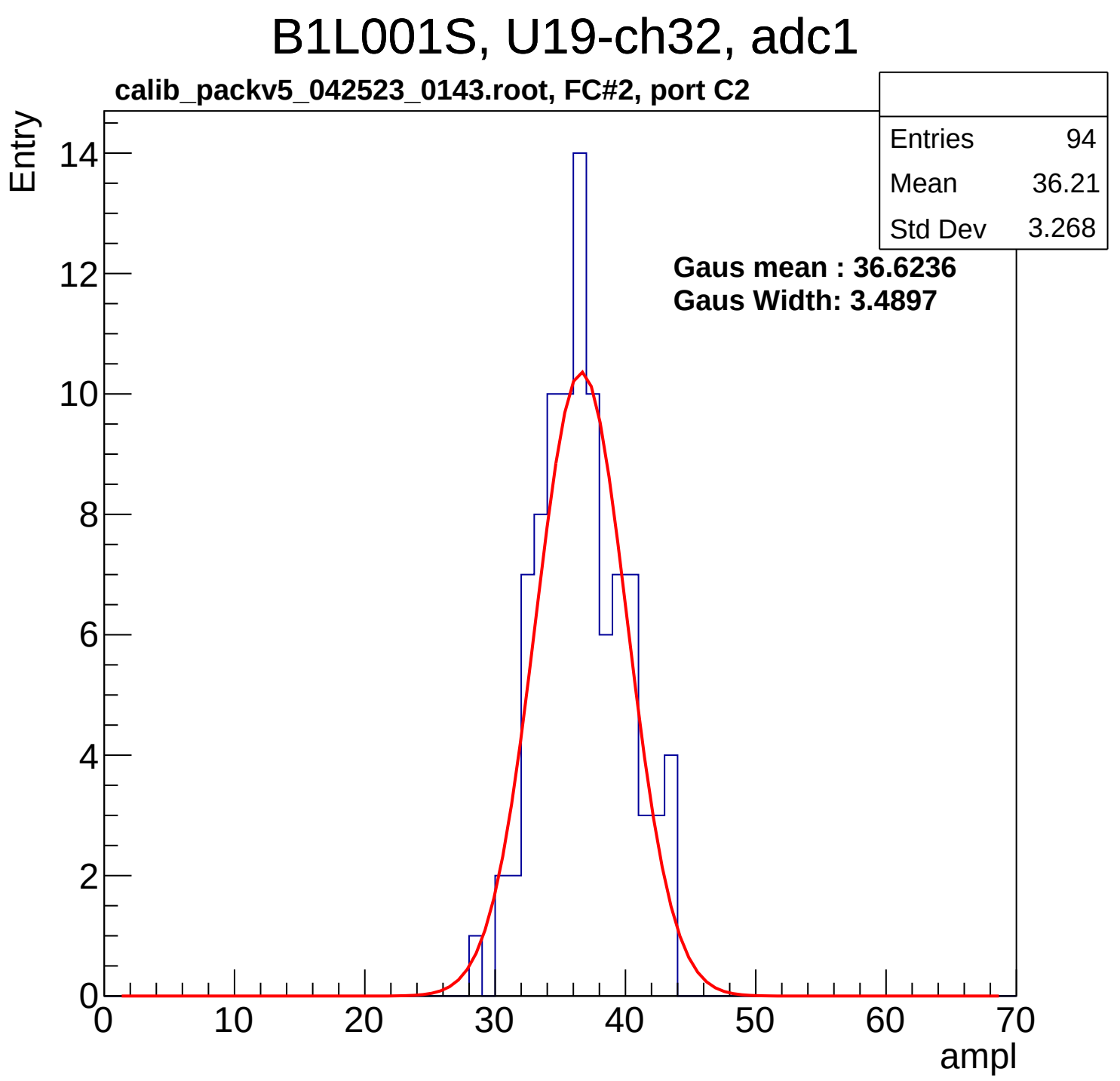
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70


B1L001S, U19-ch32, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 94
Mean 36.21
Std Dev 3.268
Gaus mean : 36.6236
Gaus Width: 3.4897
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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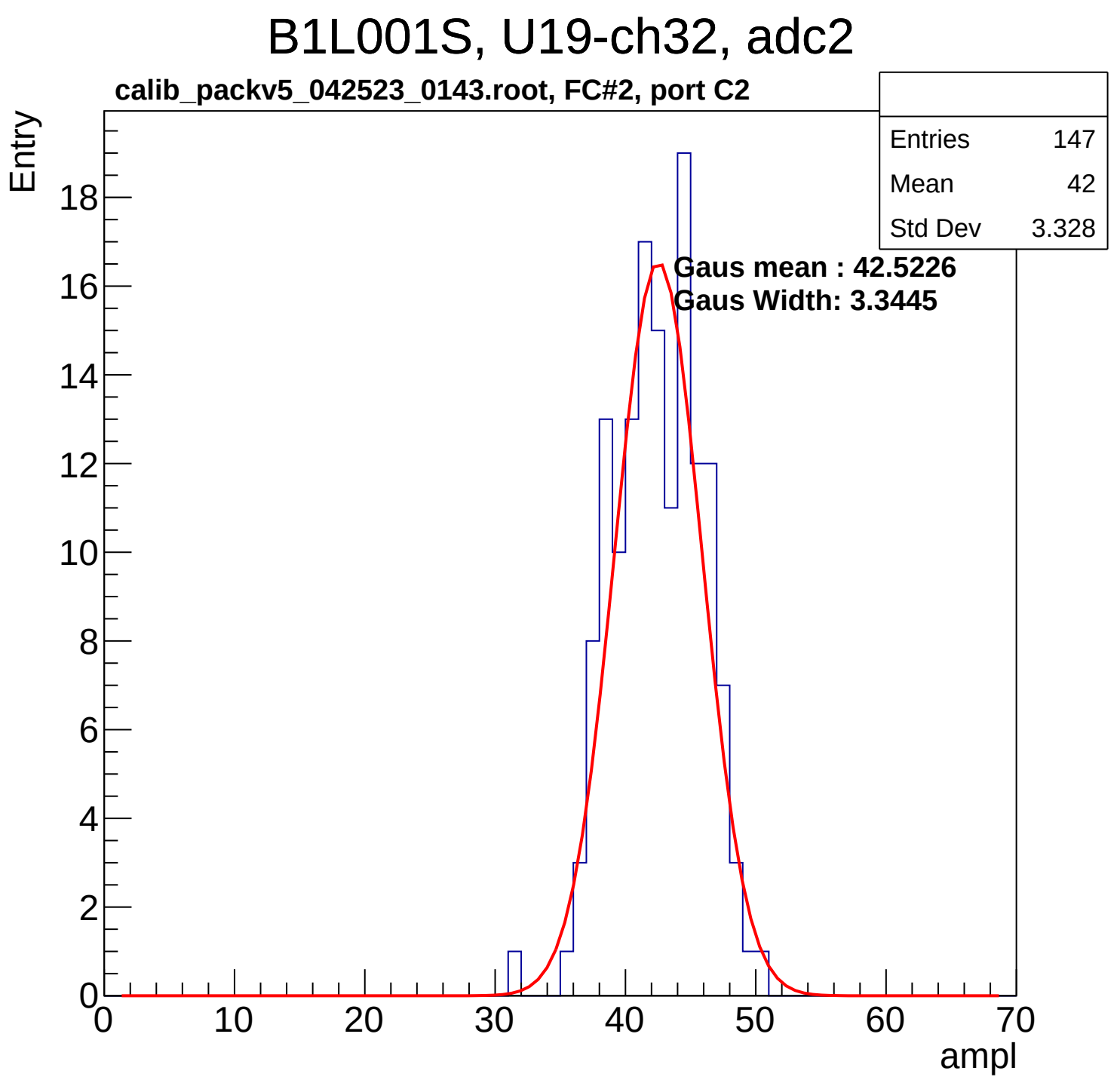
B1L001S, U19-ch32, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 147
Mean 42
Std Dev 3.328
Gaus mean : 42.5226
Gaus Width: 3.3445
Entry
ampl
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4
6
8
10
12
14
16
18
0
10
20
30
40
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60
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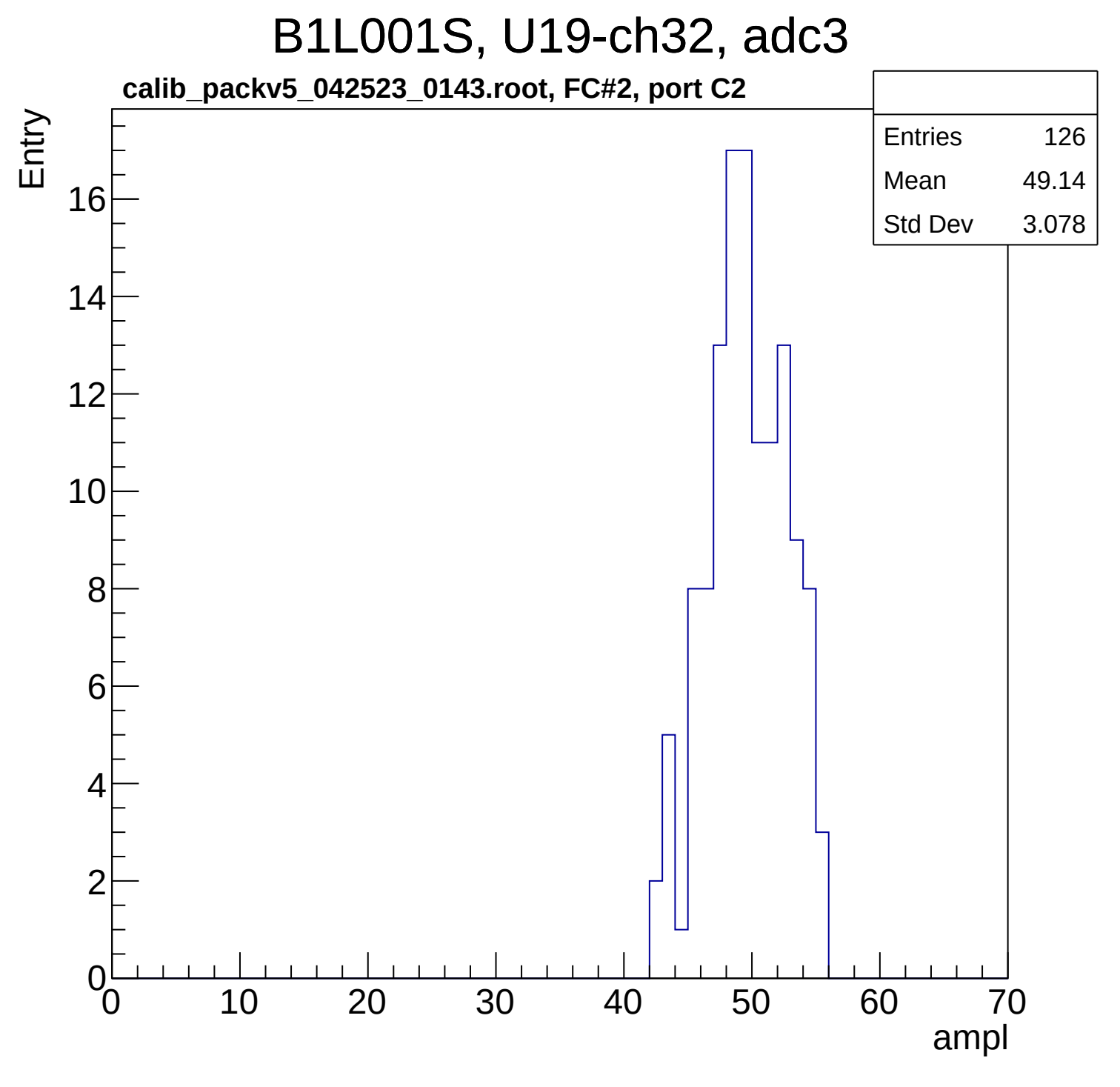
B1L001S, U19-ch32, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 126
Mean 49.14
Std Dev 3.078
Entry
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8
10
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16
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10
20
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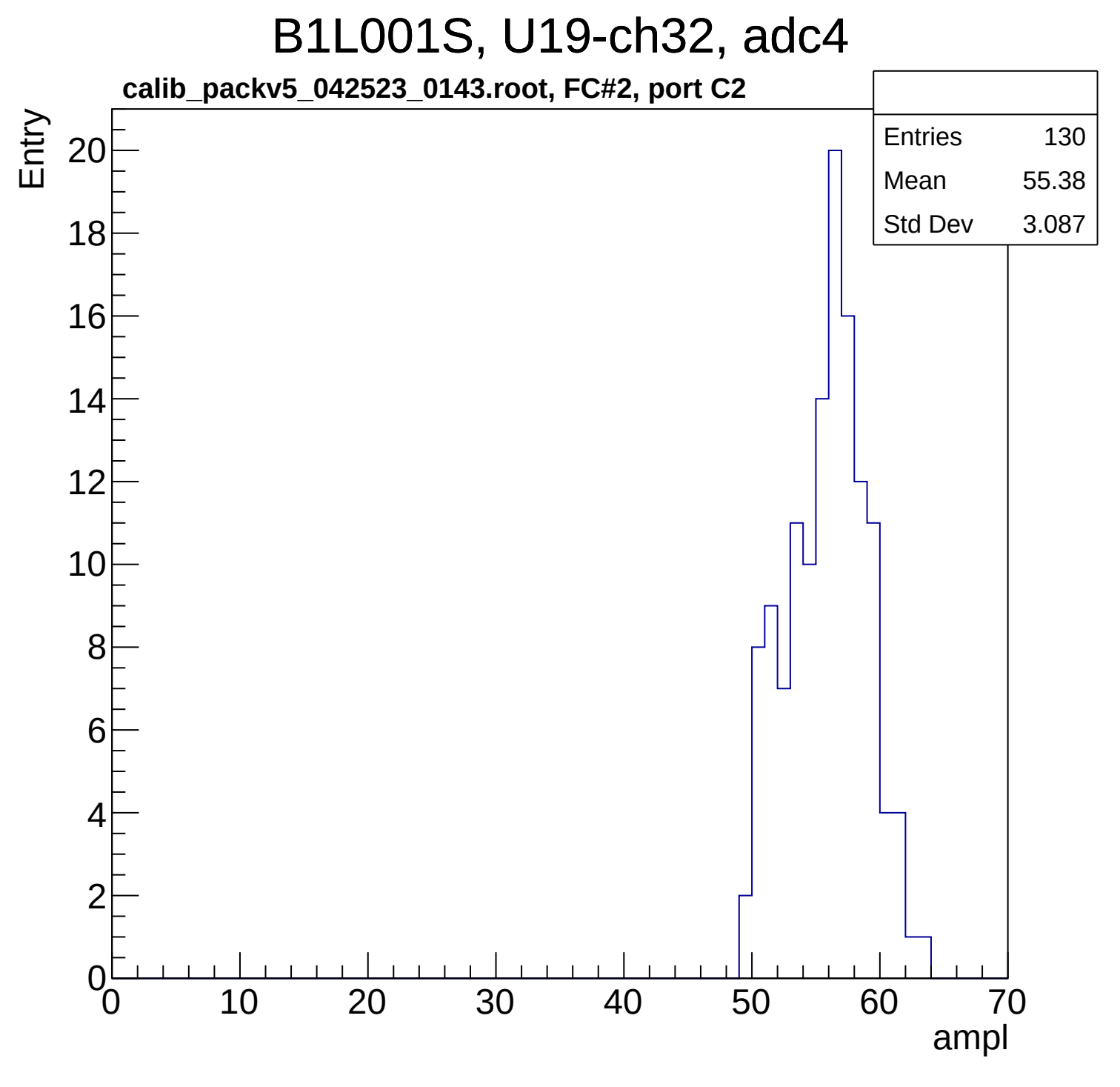
50
60
70
ampl


B1L001S, U19-ch32, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 130
Mean 55.38
Std Dev 3.087
Entry
ampl
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8
10
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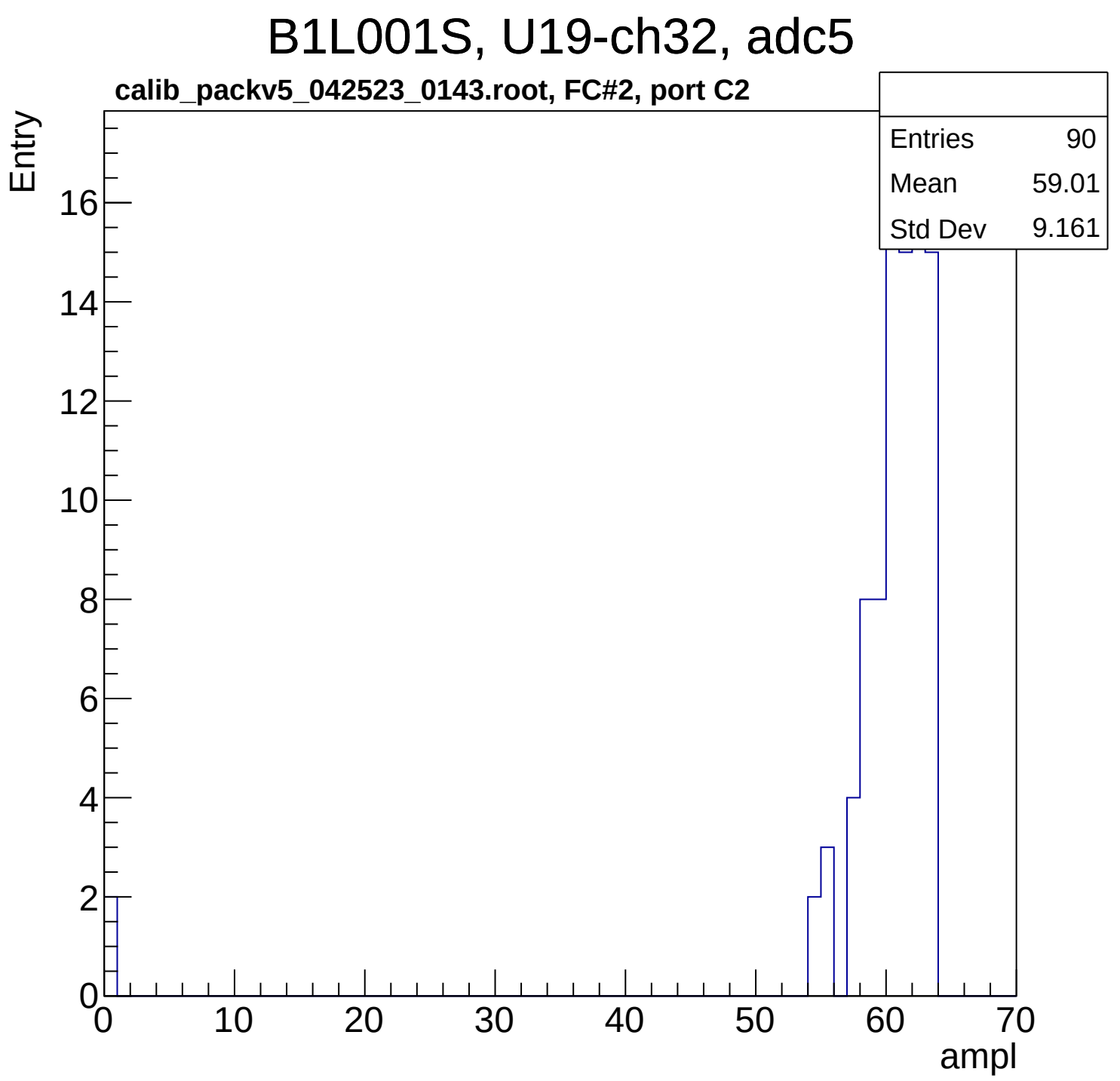
B1L001S, U19-ch32, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 90
Mean 59.01
Std Dev 9.161
Entry
ampl
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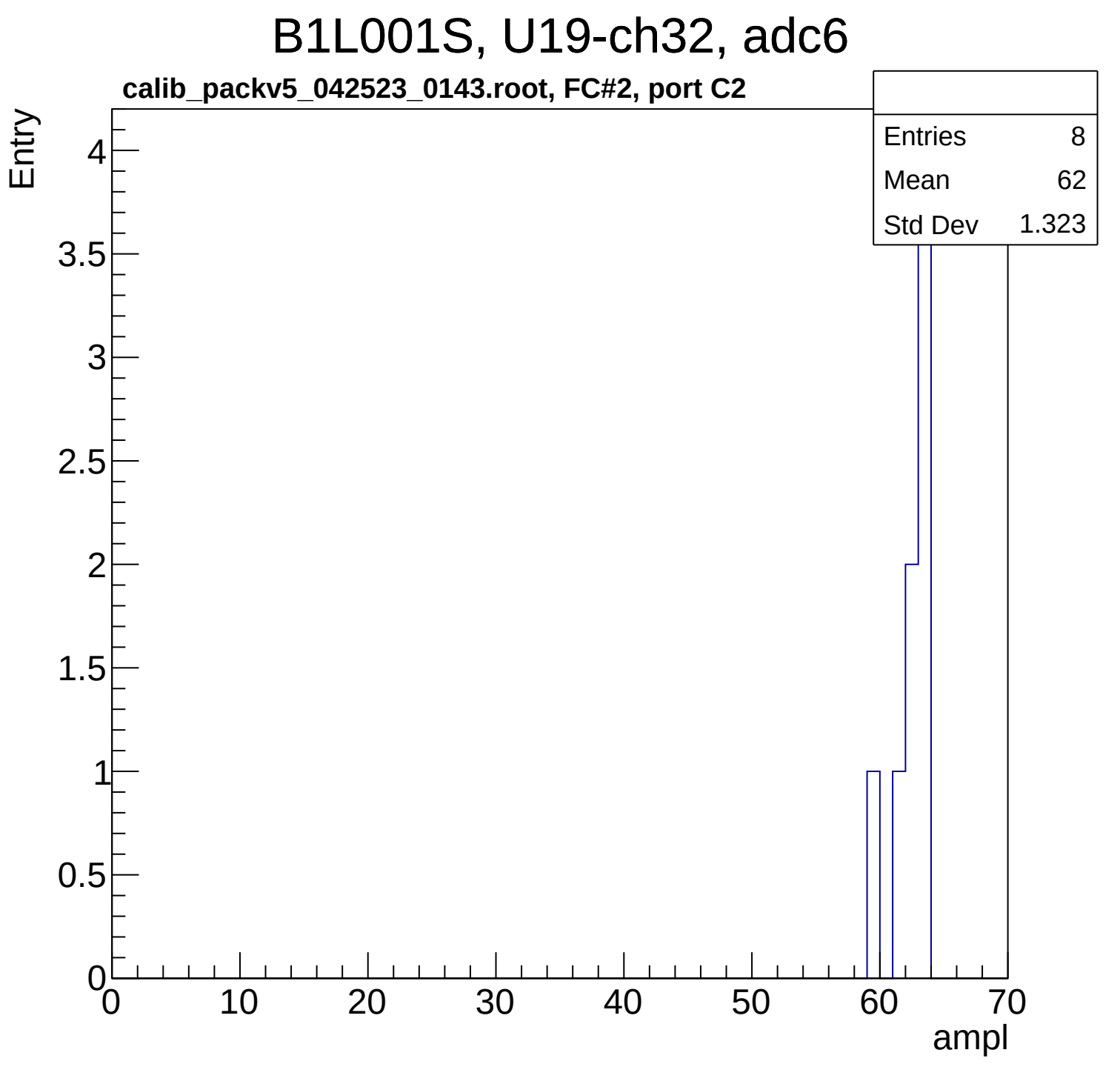
B1L001S, U19-ch32, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 8
Mean 62
Std Dev 1.323
Entry
ampl
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1.5
2
2.5
3
3.5
4
0
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40
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60
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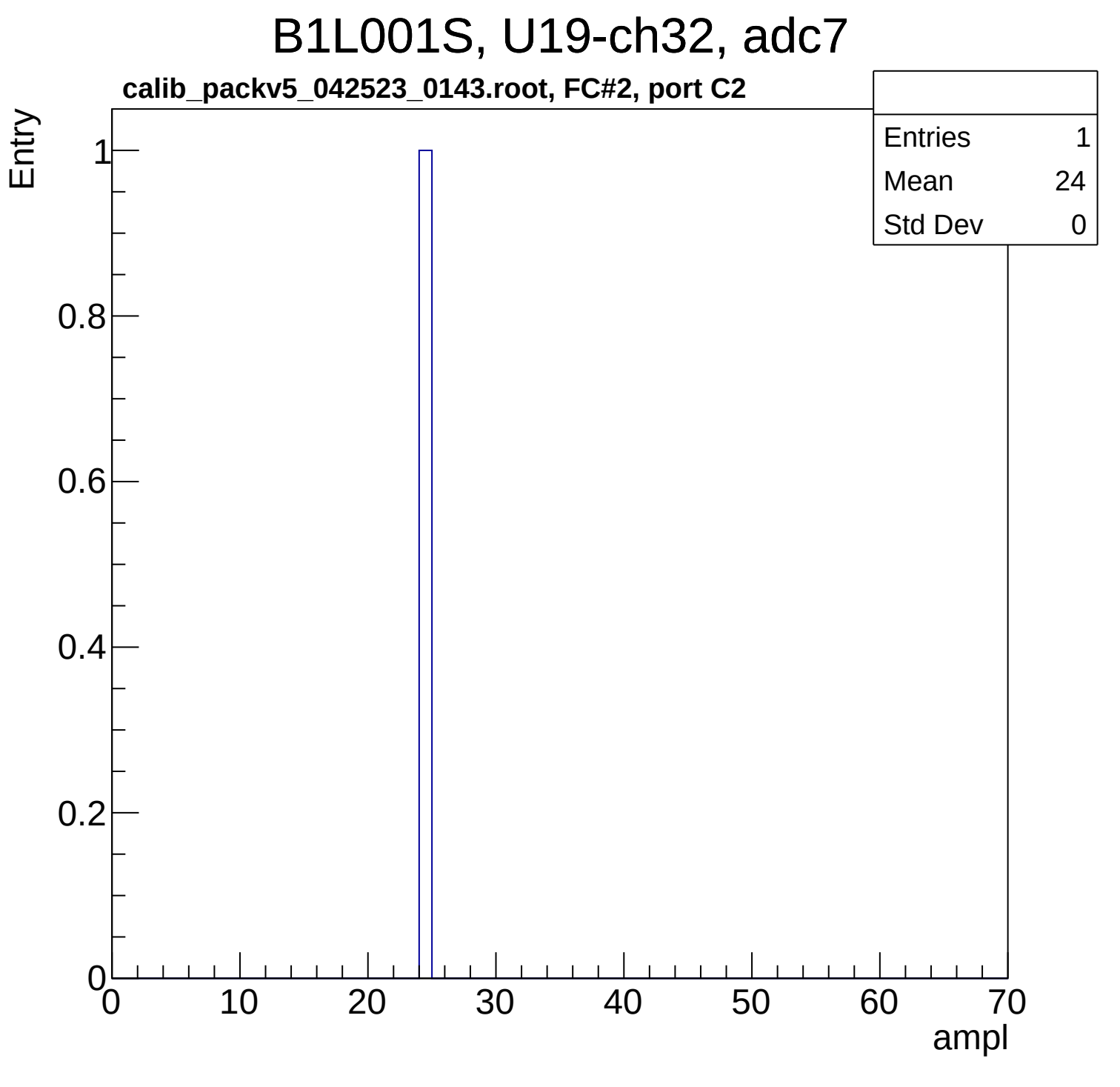
B1L001S, U19-ch32, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 24
Std Dev 0
Entry
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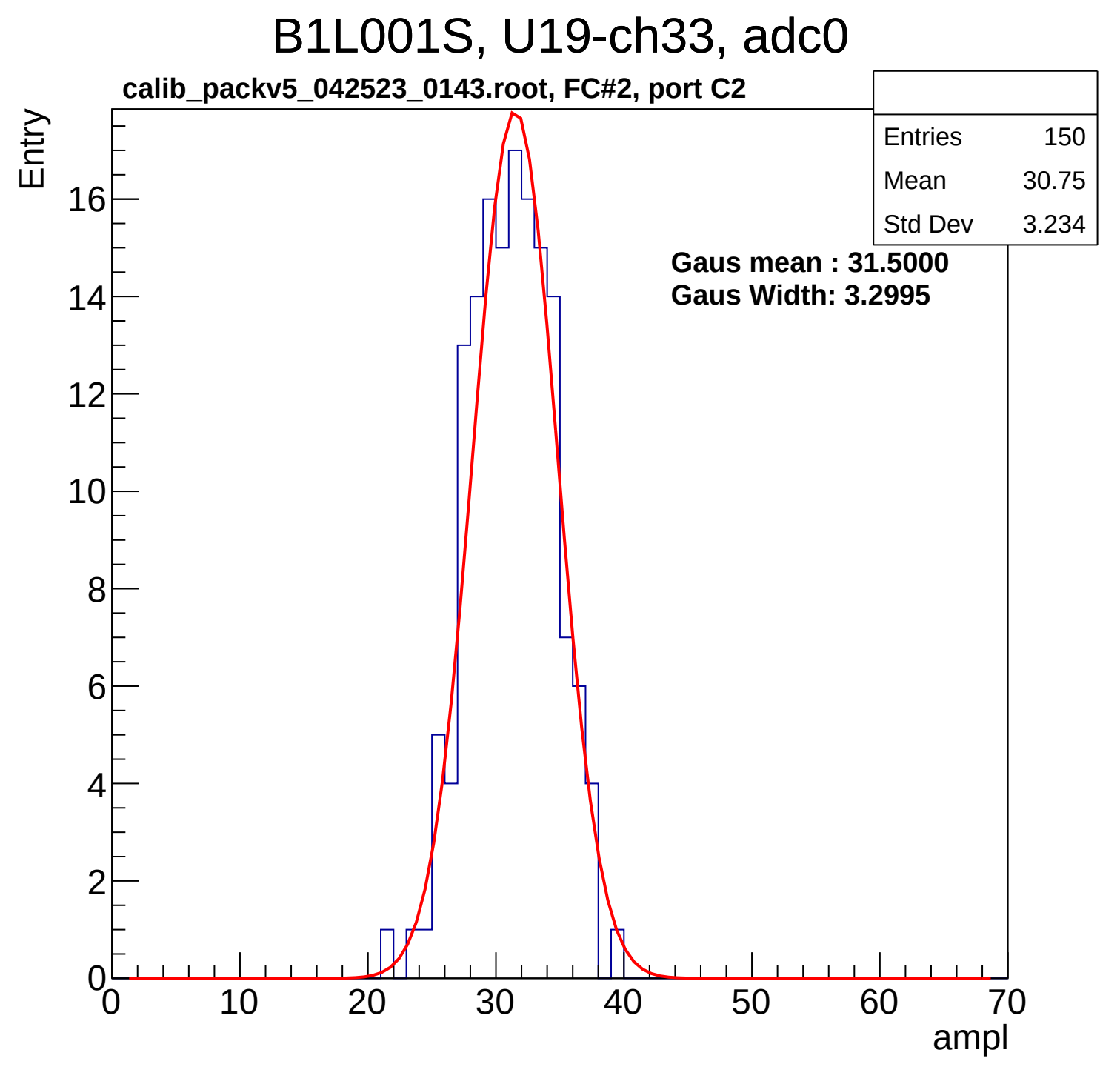
60
70
ampl


B1L001S, U19-ch33, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 150
Mean 30.75
Std Dev 3.234
Gaus mean : 31.5000
Gaus Width: 3.2995
Entry
ampl
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6
8
10
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14
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0
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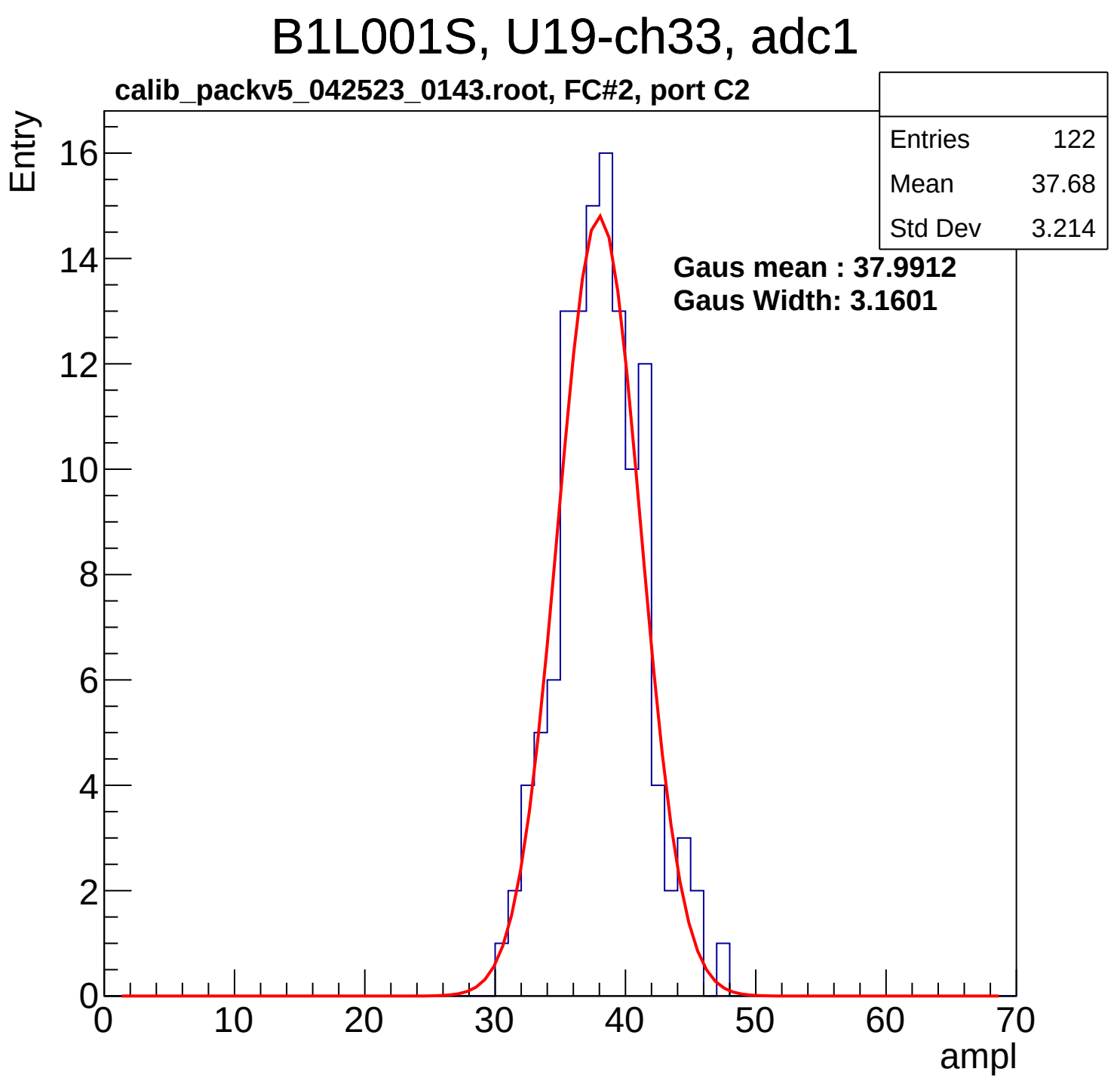
B1L001S, U19-ch33, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 122
Mean 37.68
Std Dev 3.214
Gaus mean : 37.9912
Gaus Width: 3.1601
Entry
ampl
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4
6
8
10
12
14
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0
10
20
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40
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60
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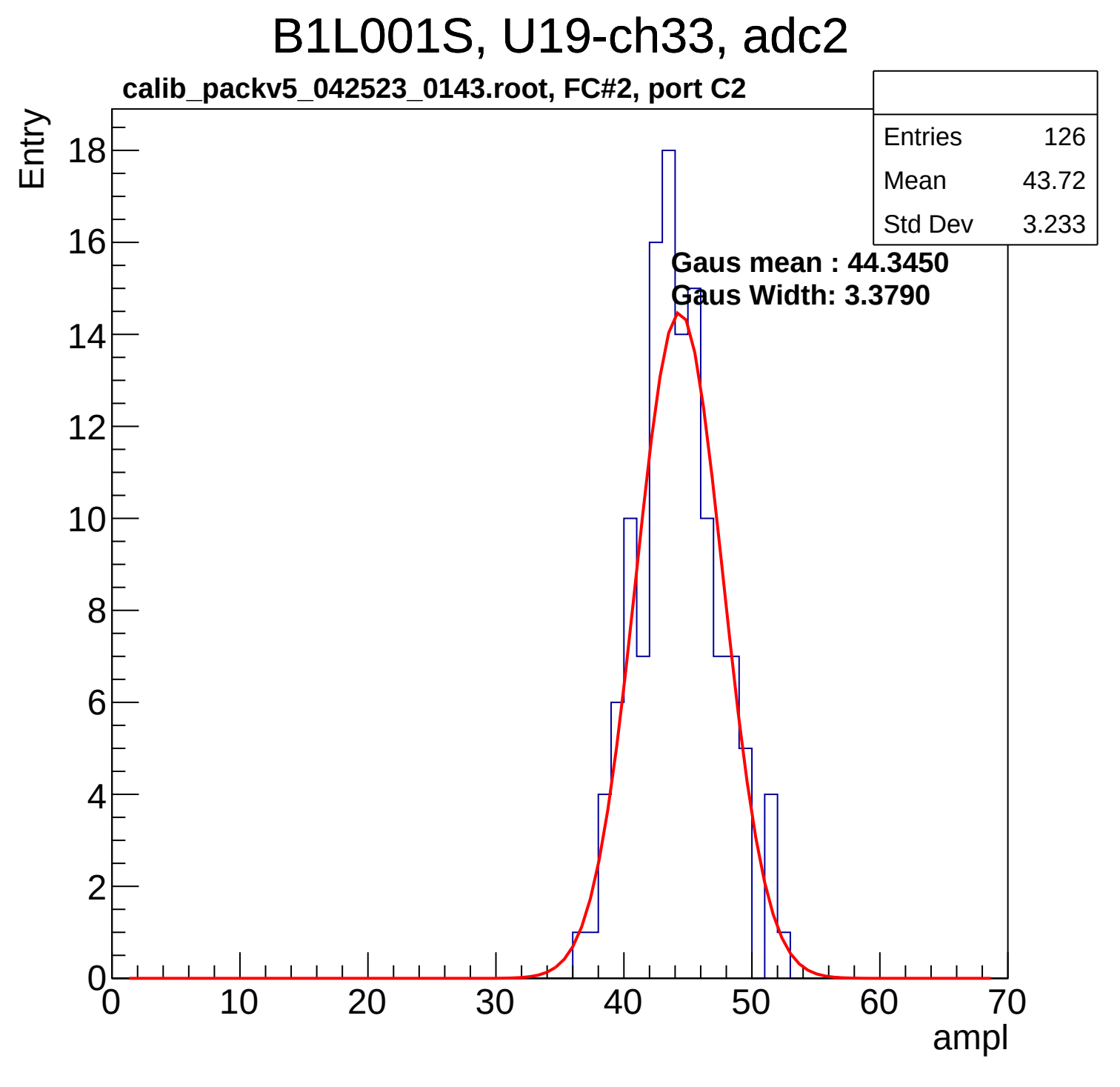
B1L001S, U19-ch33, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 126
Mean 43.72
Std Dev 3.233
Gaus mean : 44.3450
Gaus Width: 3.3790
Entry
ampl
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4
6
8
10
12
14
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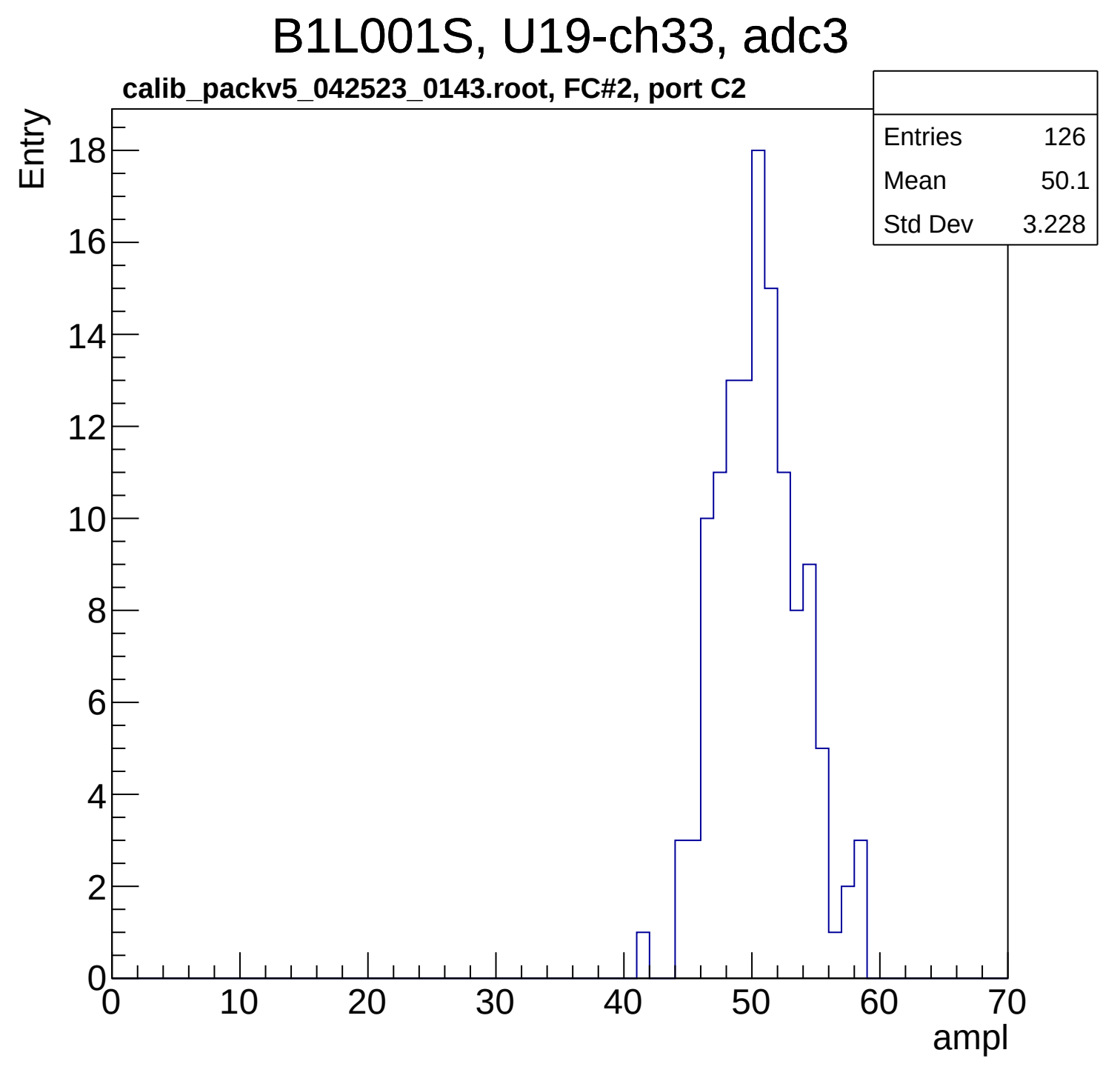
B1L001S, U19-ch33, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 126
Mean 50.1
Std Dev 3.228
Entry
ampl
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6
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10
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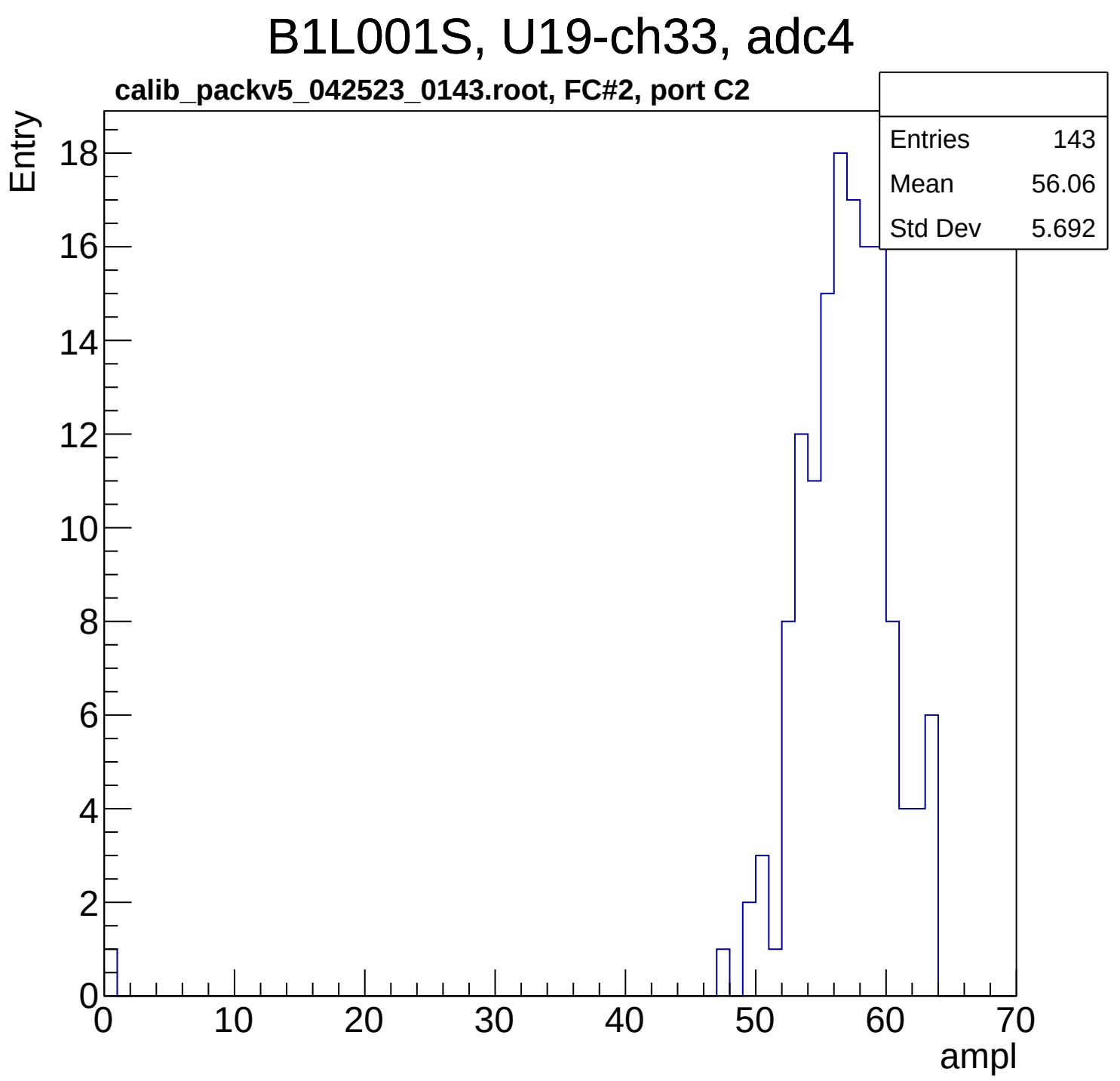
B1L001S, U19-ch33, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 143
Mean 56.06
Std Dev 5.692
Entry
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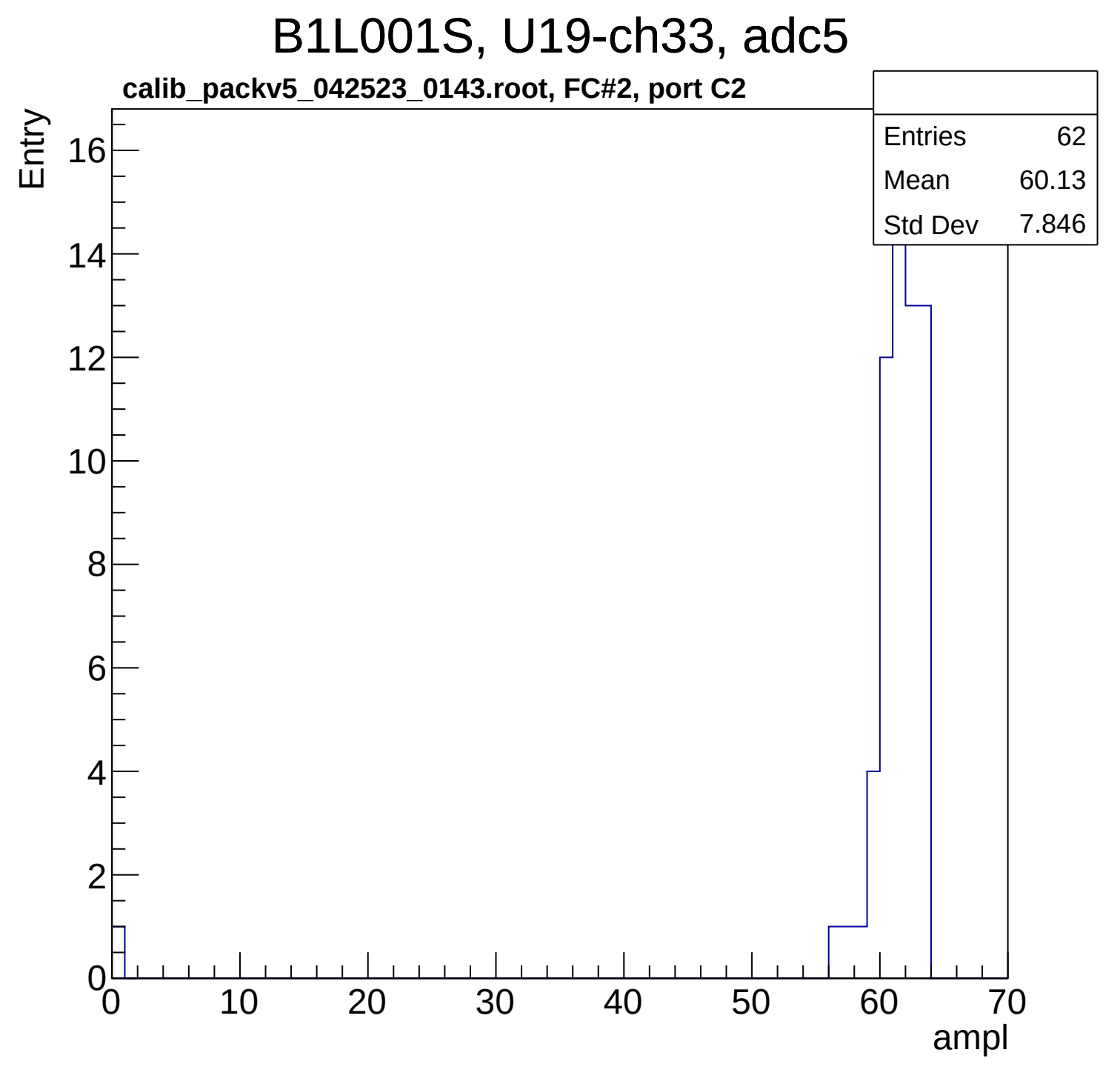
ampl


B1L001S, U19-ch33, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 62
Mean 60.13
Std Dev 7.846
Entry
ampl
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6
8
10
12
14
16
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50
60
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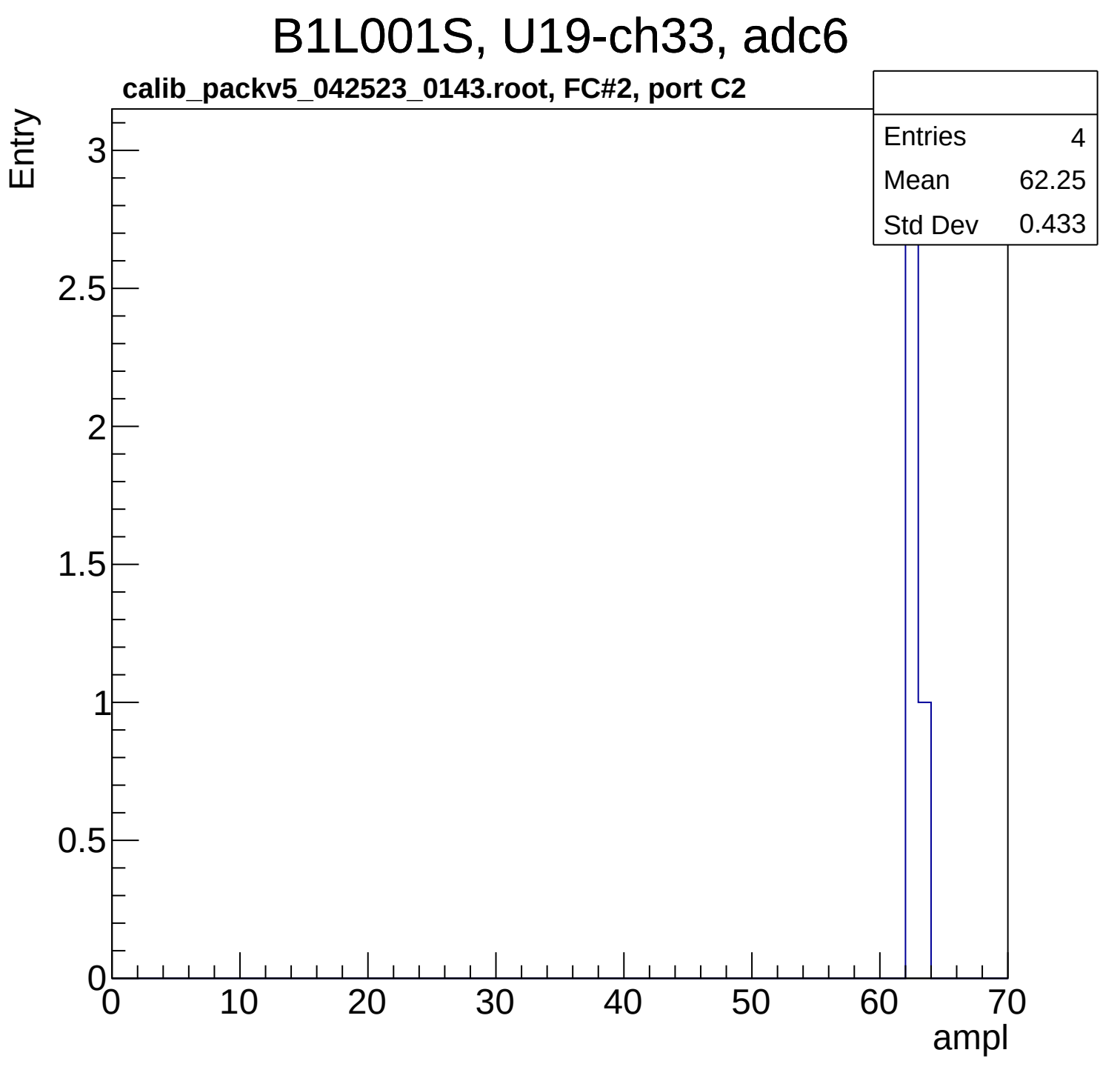
B1L001S, U19-ch33, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 4
Mean 62.25
Std Dev 0.433
Entry
ampl
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0.5
1
1.5
2
2.5
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0
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20
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40
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60
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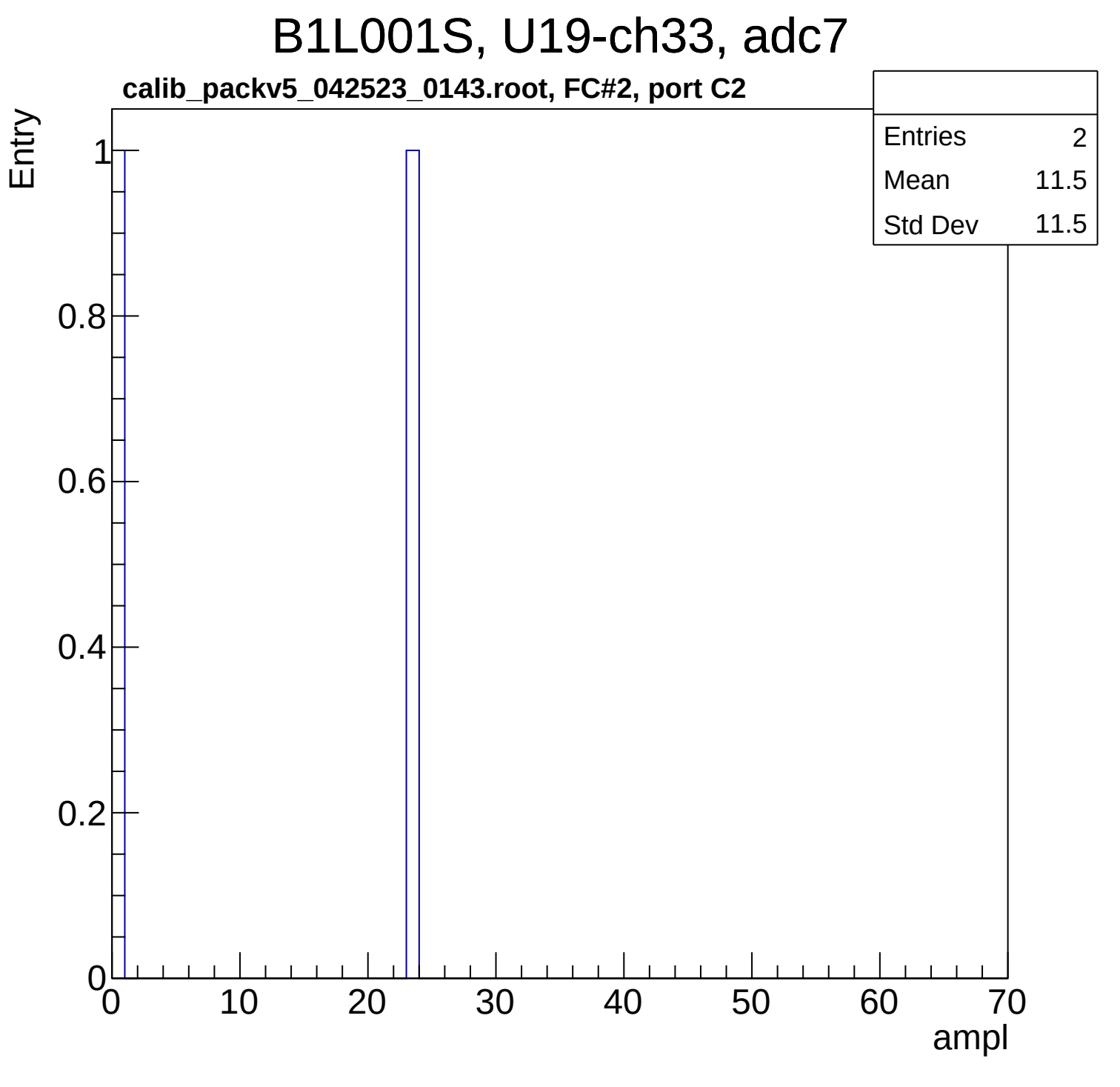
B1L001S, U19-ch33, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 11.5
Std Dev 11.5
Entry
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0.8
0.6
0.4
0.2
0
0
10
20
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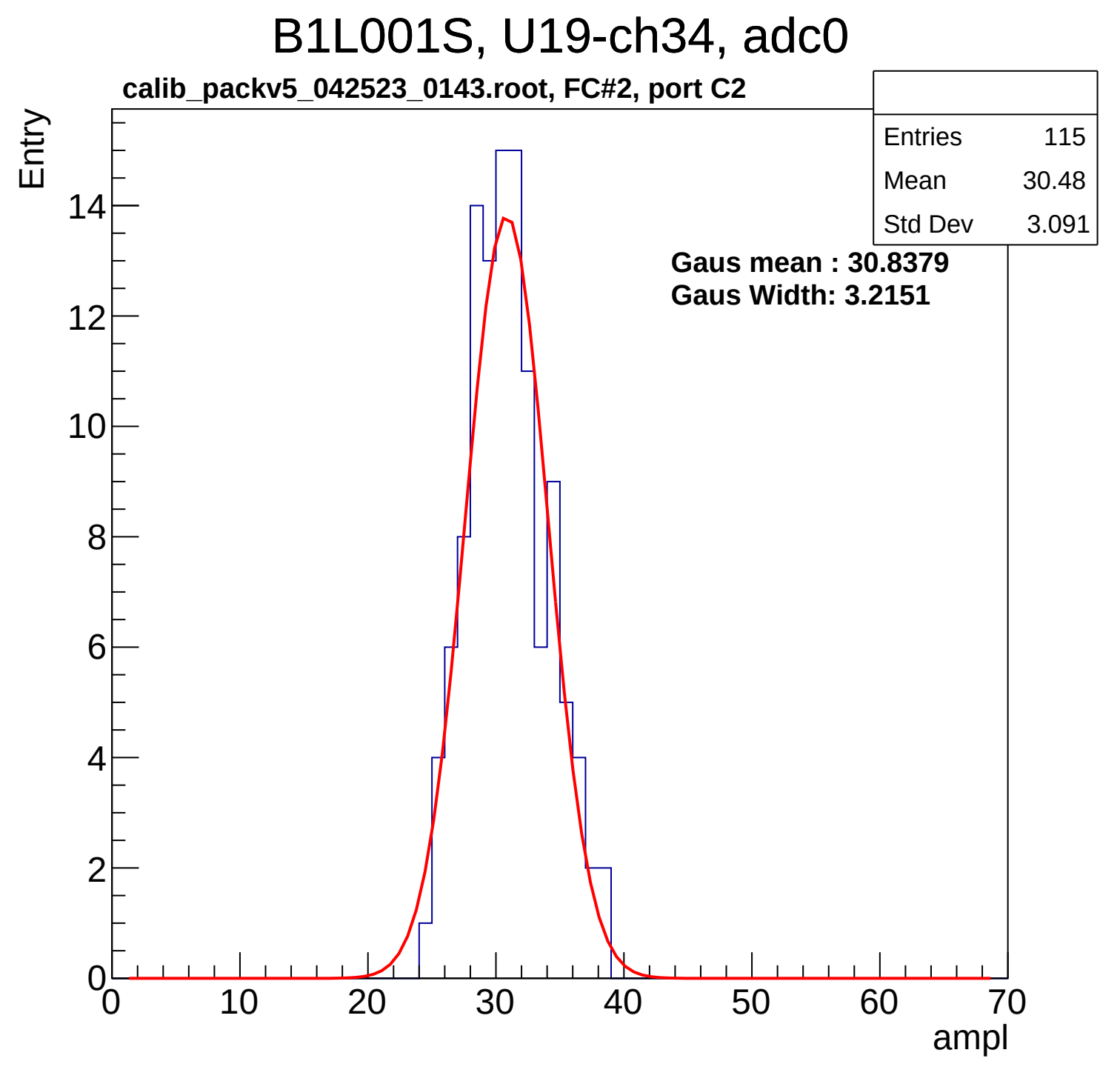
40
50
60
70
ampl


B1L001S, U19-ch34, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 115
Mean 30.48
Std Dev 3.091
Gaus mean : 30.8379
Gaus Width: 3.2151
Entry
ampl
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2
4
6
8
10
12
14
0
10
20
30
40
50
60
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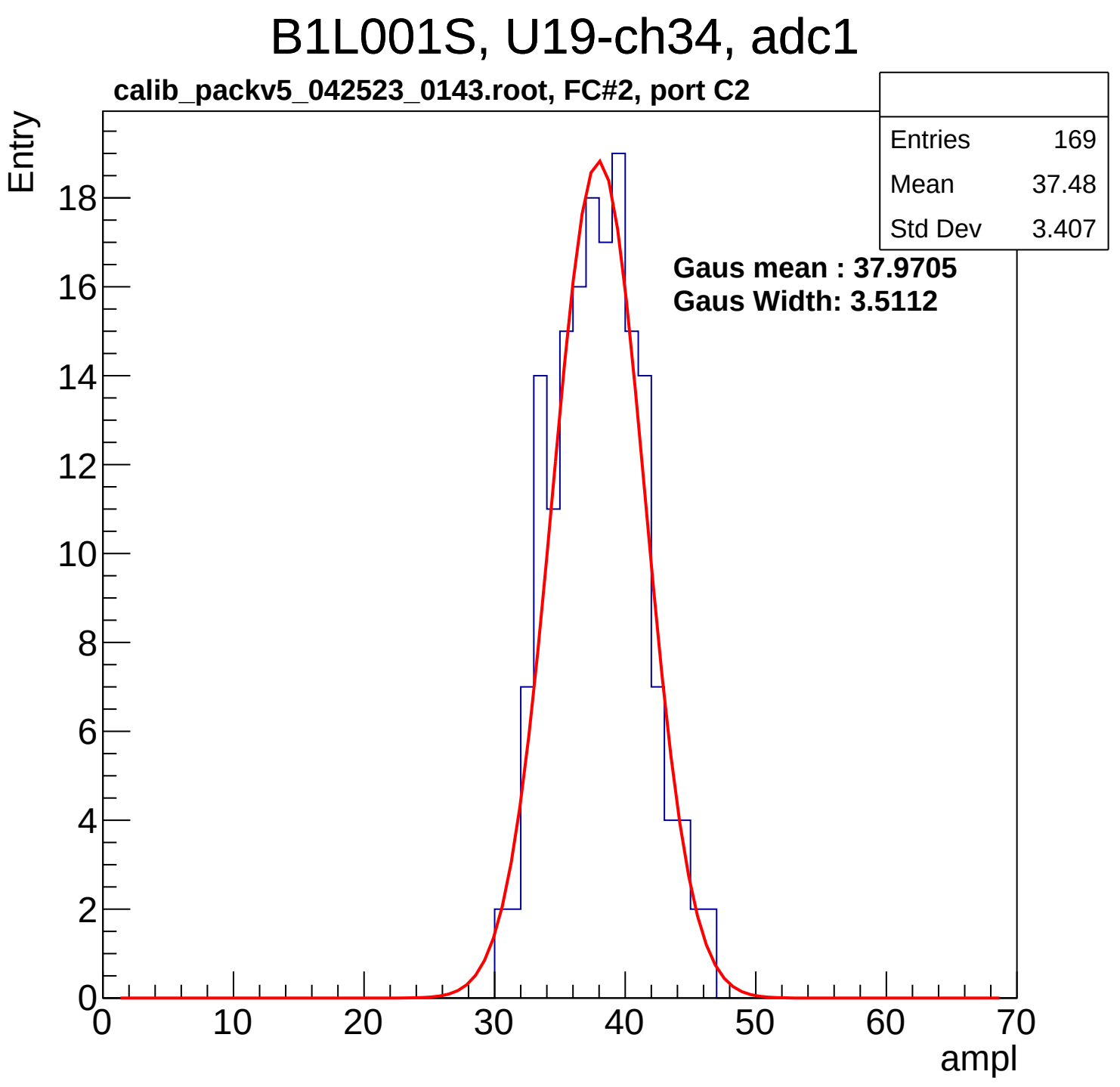
B1L001S, U19-ch34, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 169
Mean 37.48
Std Dev 3.407
Gaus mean : 37.9705
Gaus Width: 3.5112
Entry
ampl
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4
6
8
10
12
14
16
18
0
10
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40
50
60
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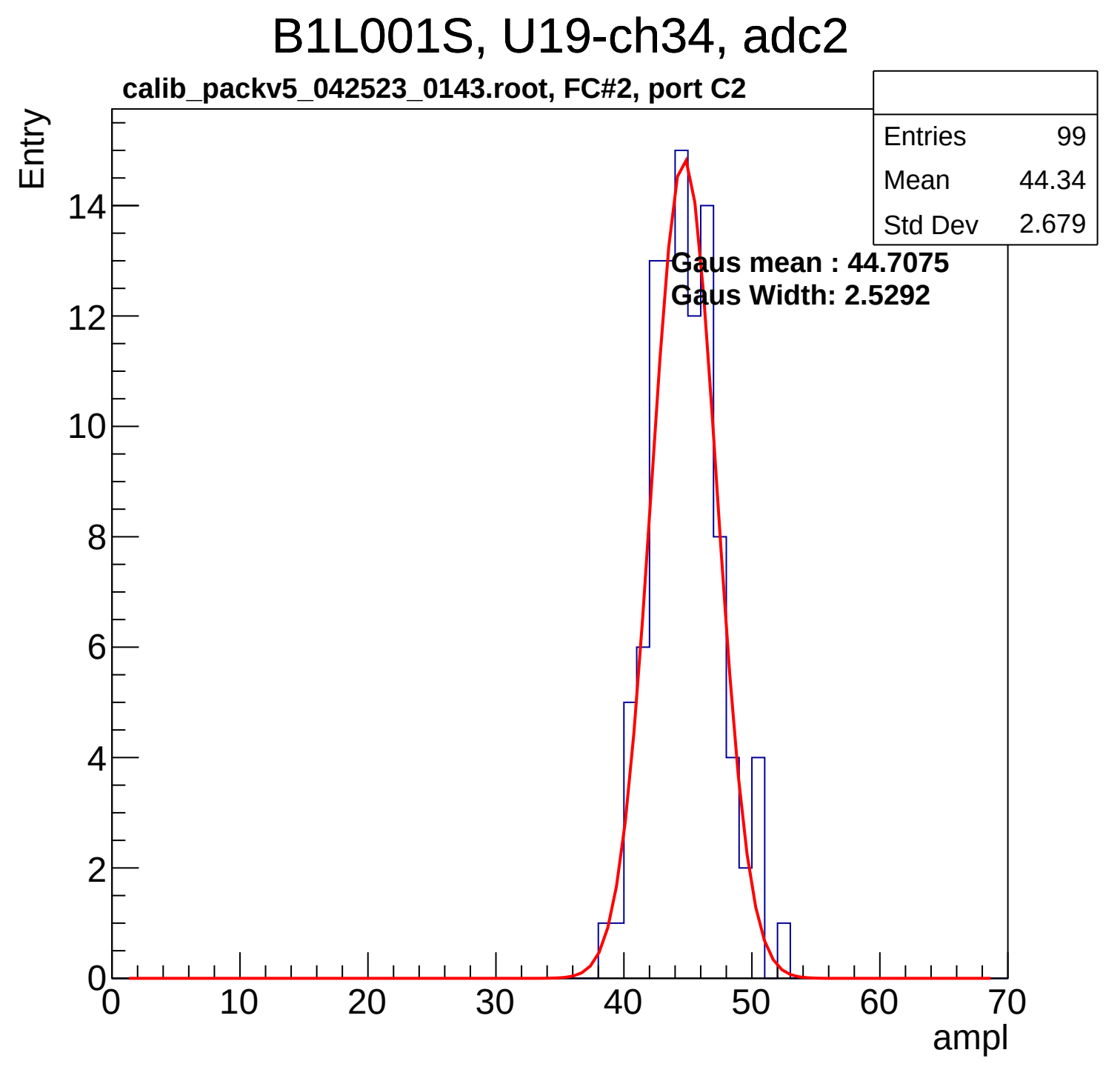
B1L001S, U19-ch34, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 99
Mean 44.34
Std Dev 2.679
Gaus mean : 44.7075
Gaus Width: 2.5292
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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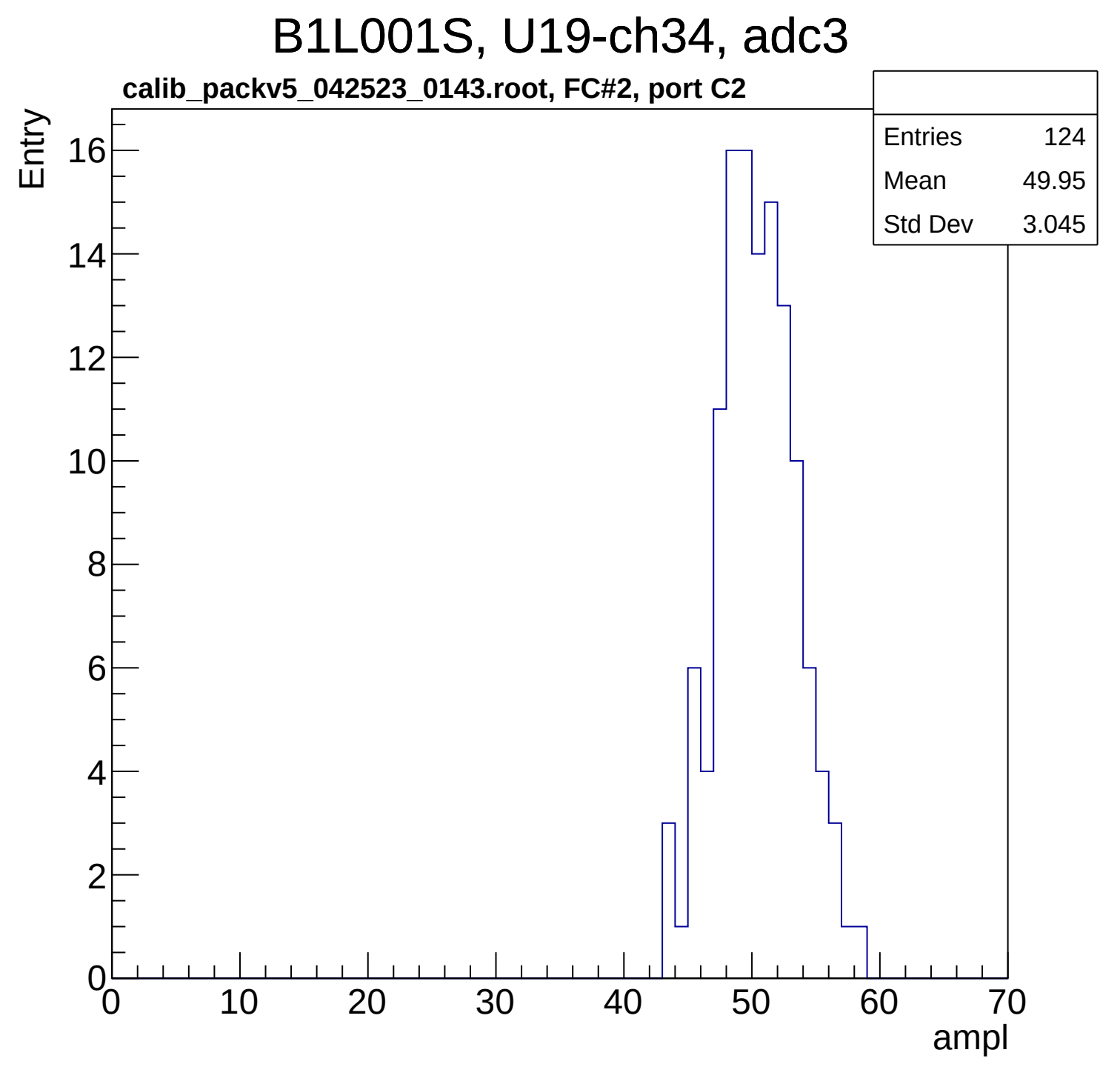
B1L001S, U19-ch34, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 124
Mean 49.95
Std Dev 3.045
Entry
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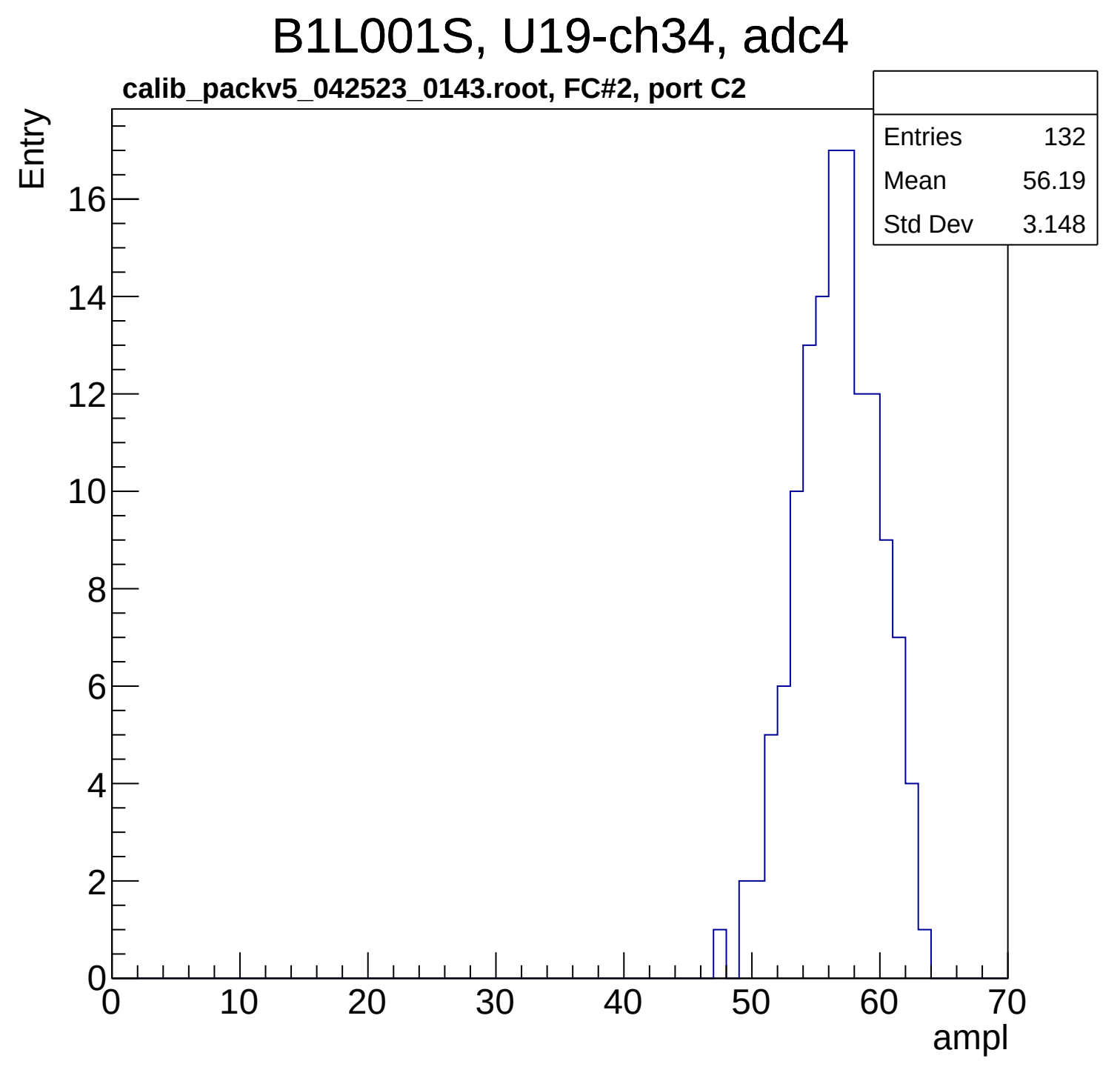
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch34, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 132
Mean 56.19
Std Dev 3.148
Entry
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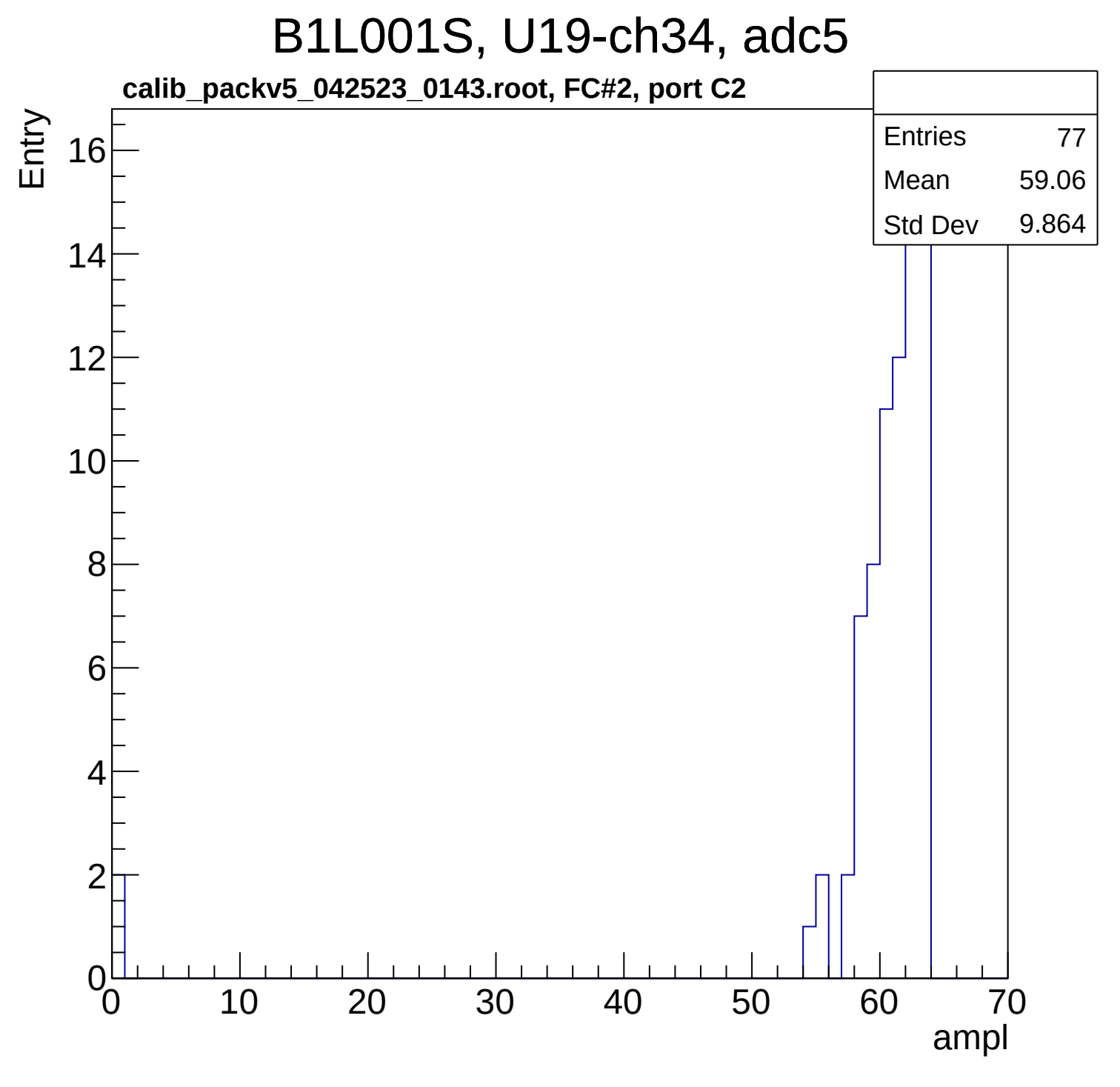
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch34, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 77
Mean 59.06
Std Dev 9.864
Entry
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4
6
8
10
12
14
16
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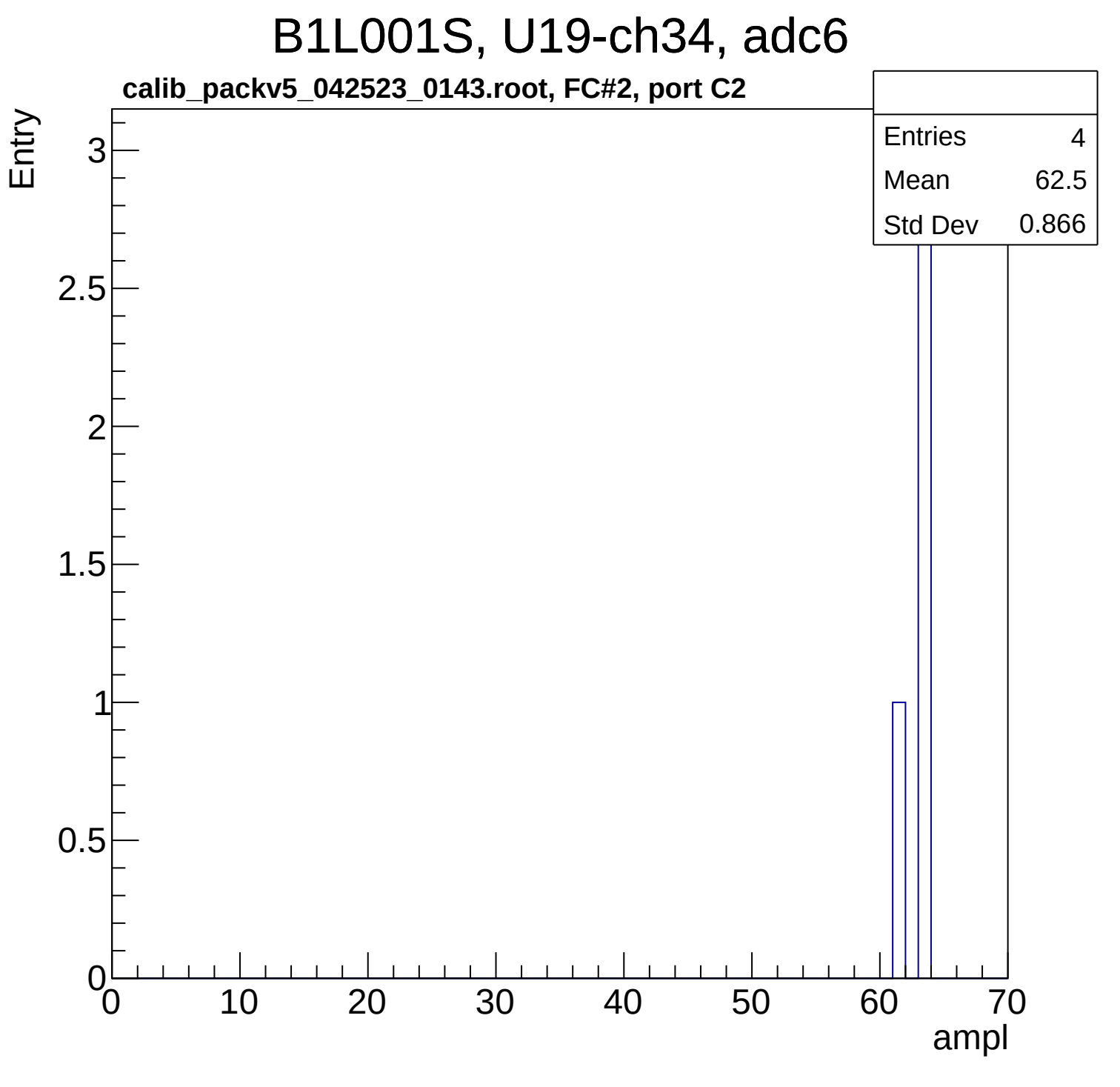
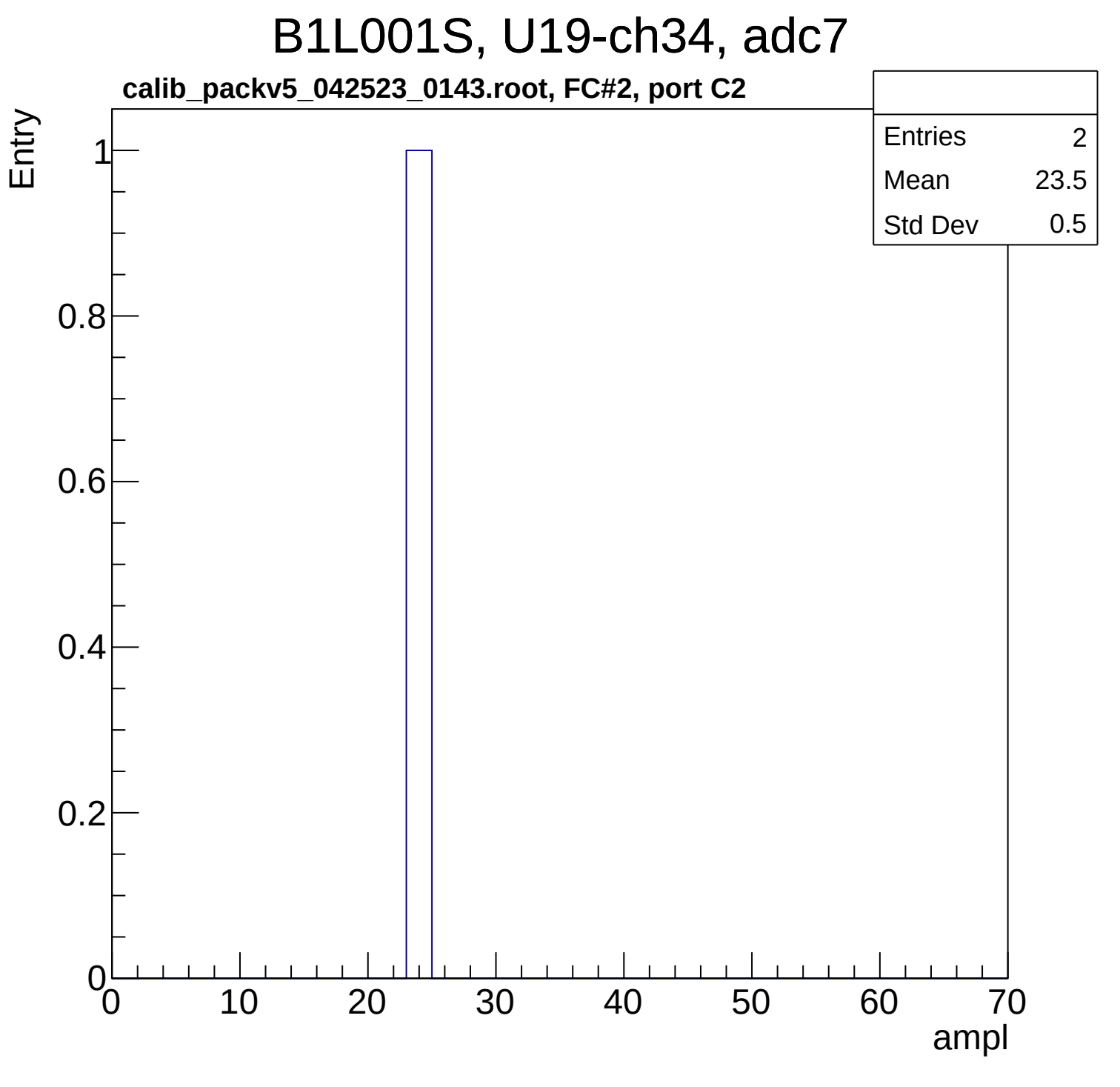
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch34, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 4
Mean 62.5
Std Dev 0.866
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L001S, U19-ch34, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 23.5
Std Dev 0.5
Entry
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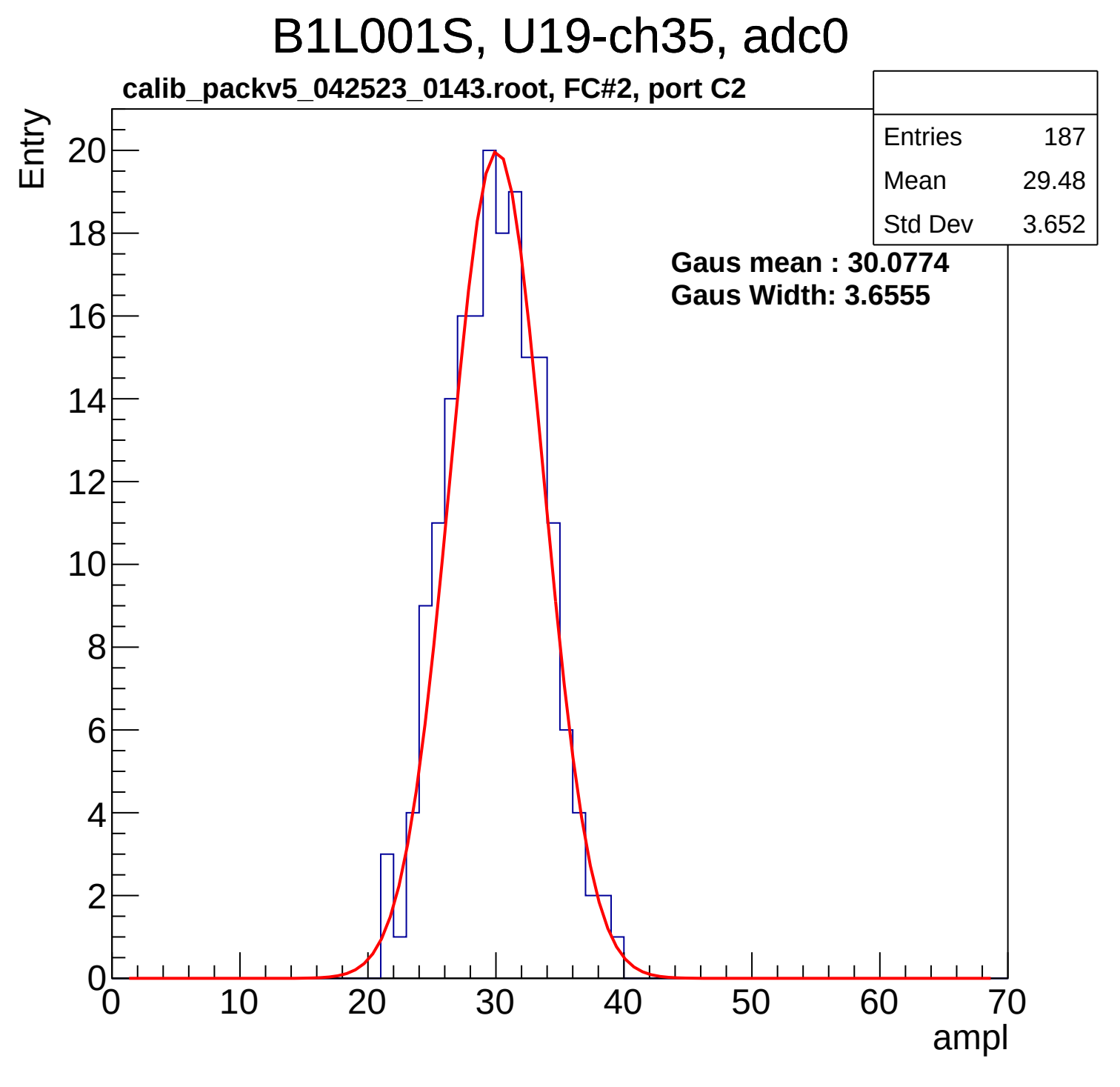
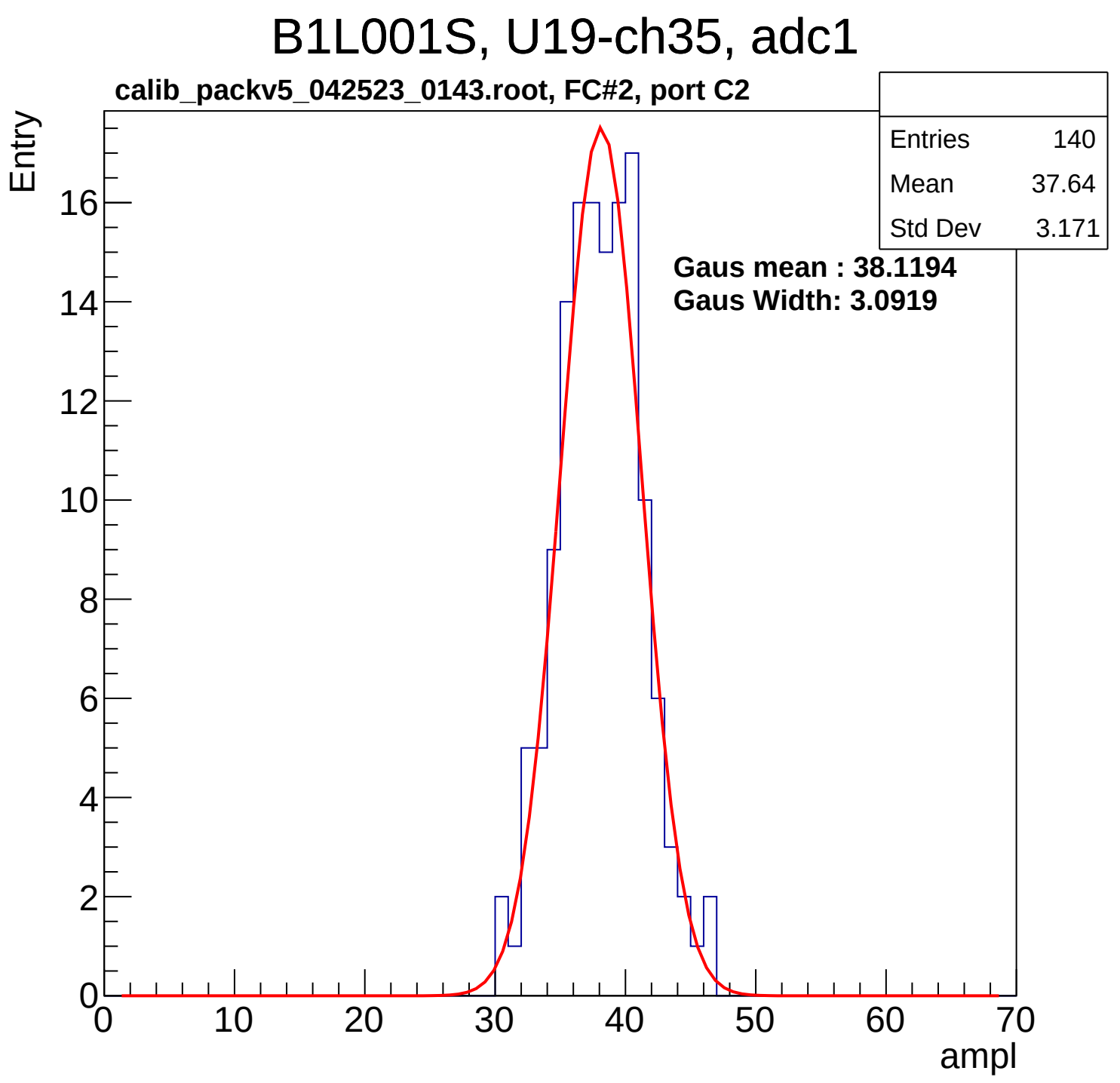
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch35, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 187
Mean 29.48
Std Dev 3.652
Gaus mean : 30.0774
Gaus Width: 3.6555
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70


B1L001S, U19-ch35, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 140
Mean 37.64
Std Dev 3.171
Gaus mean : 38.1194
Gaus Width: 3.0919
Entry
ampl
0
2
4
6
8
10
12
14
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0
10
20
30
40
50
60
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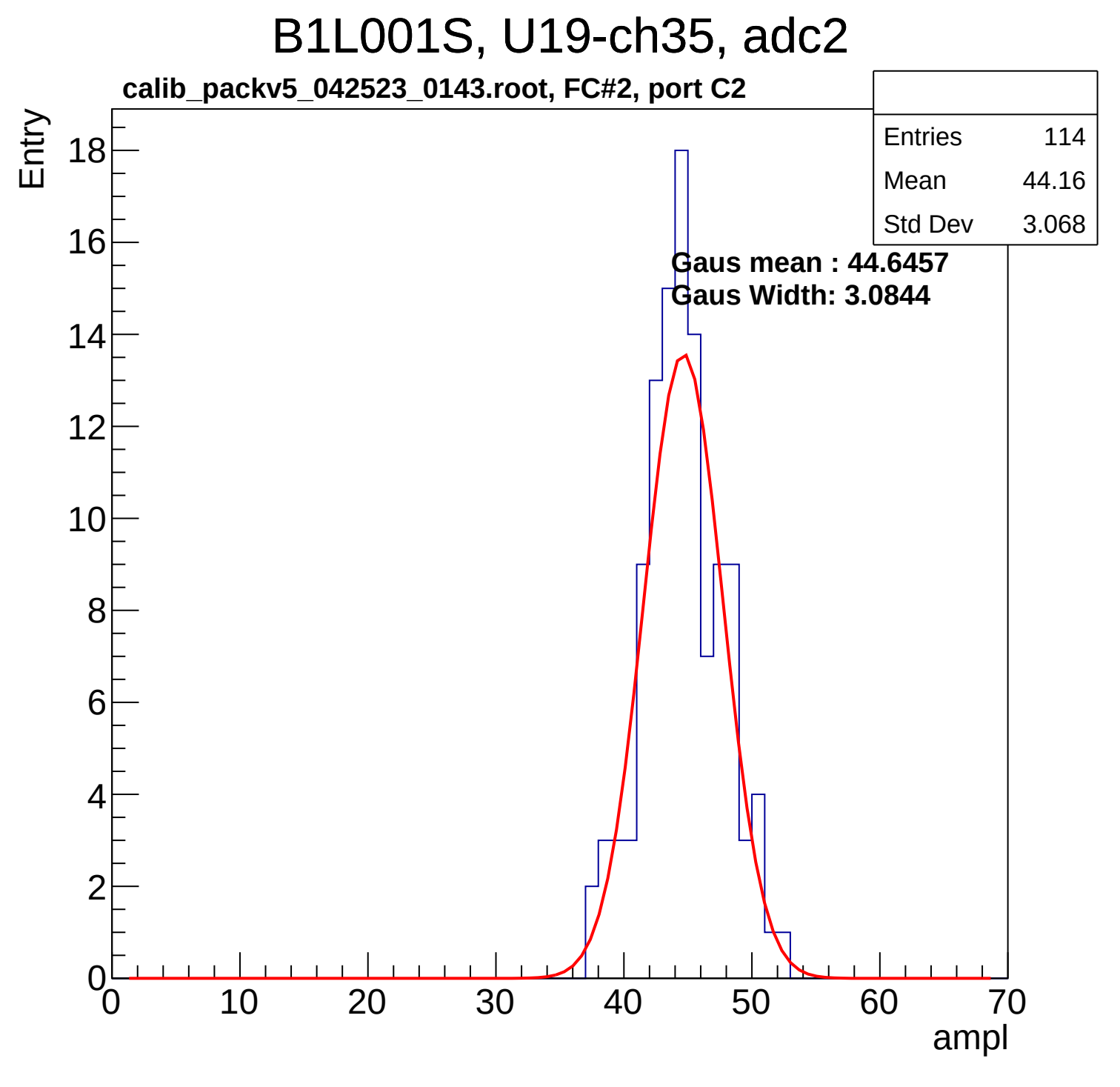
B1L001S, U19-ch35, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 114
Mean 44.16
Std Dev 3.068
Gaus mean : 44.6457
Gaus Width: 3.0844
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
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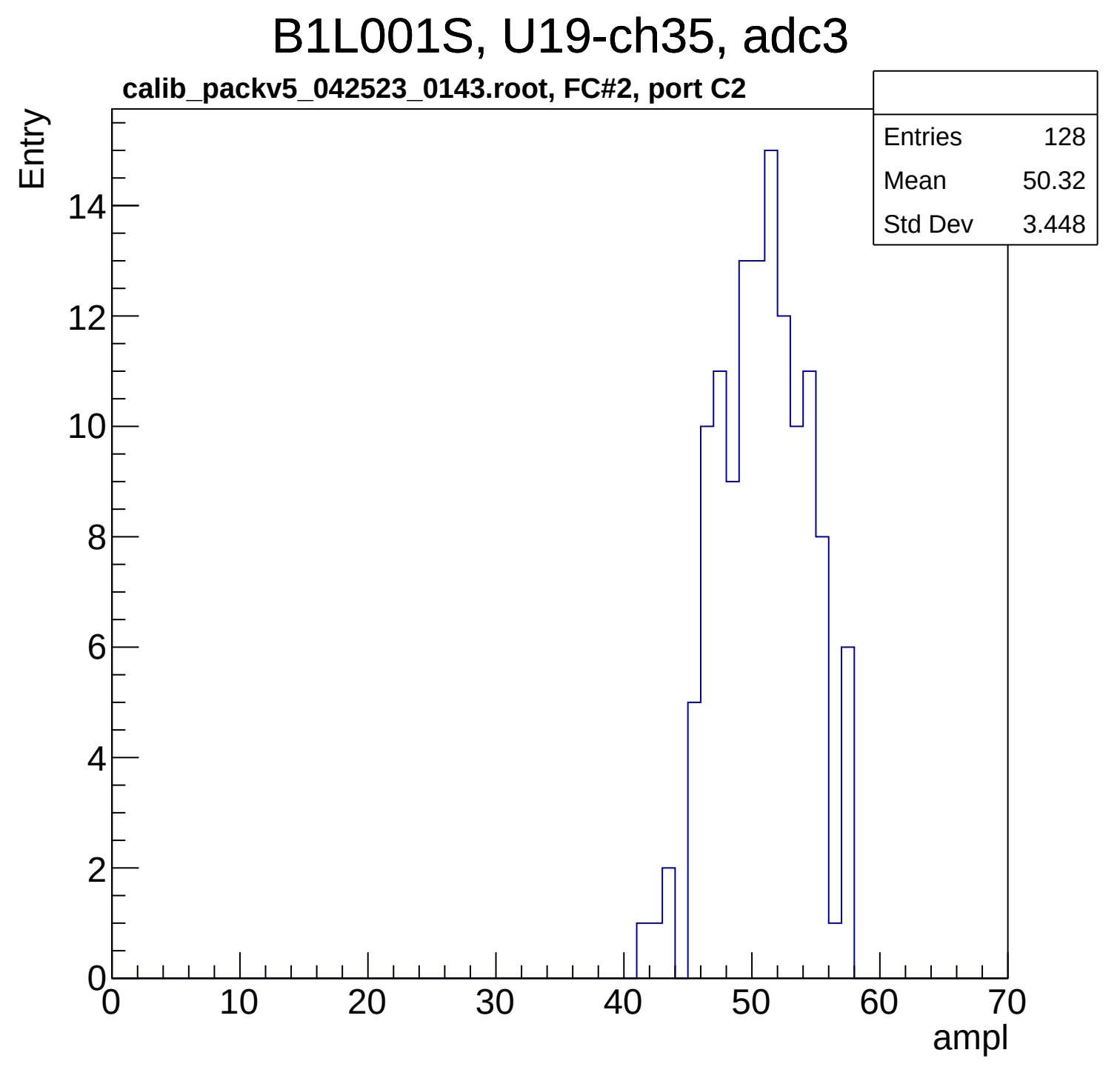
B1L001S, U19-ch35, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 128
Mean 50.32
Std Dev 3.448
Entry
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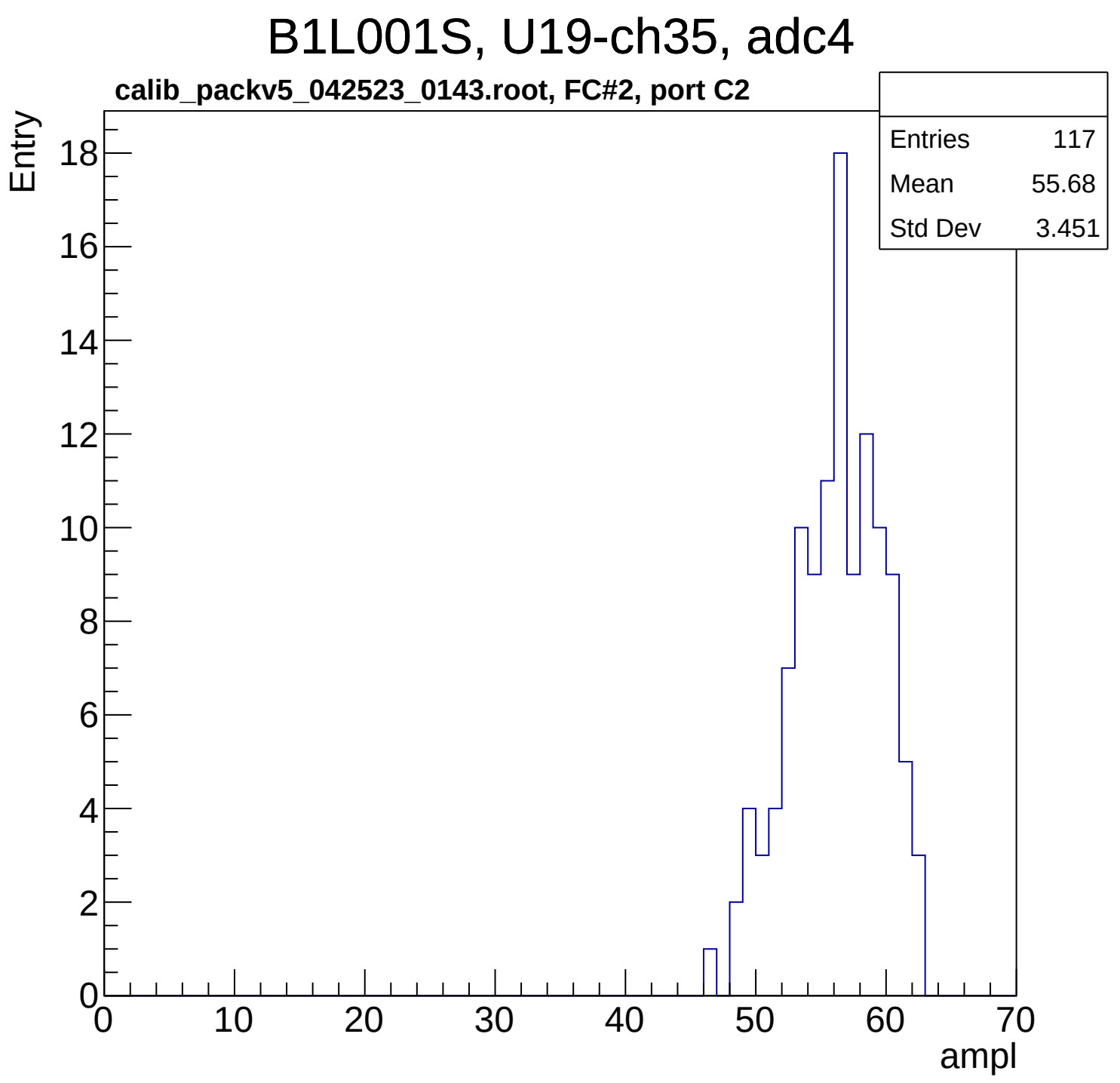
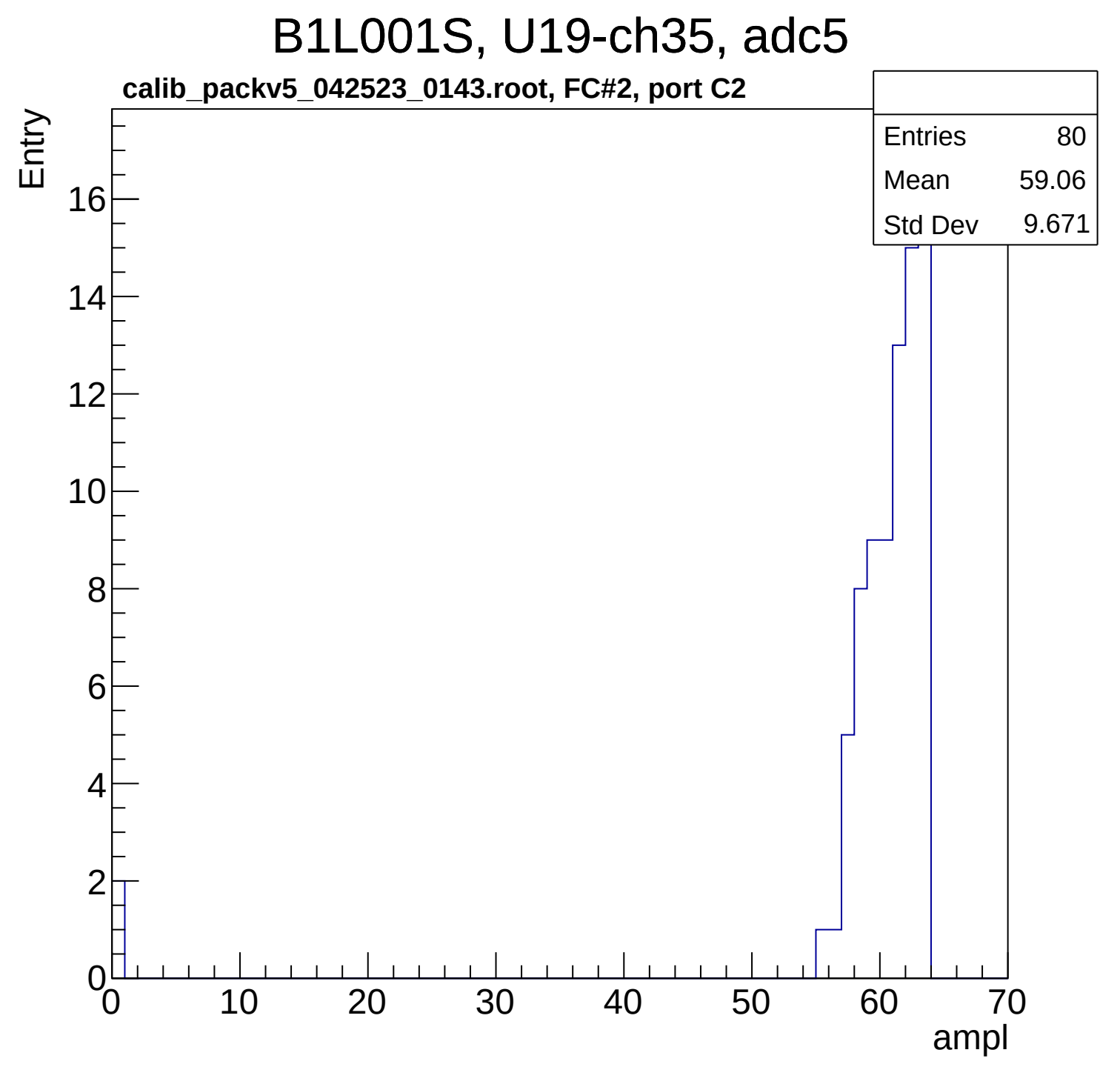
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch35, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 117
Mean 55.68
Std Dev 3.451
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch35, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 80
Mean 59.06
Std Dev 9.671
Entry
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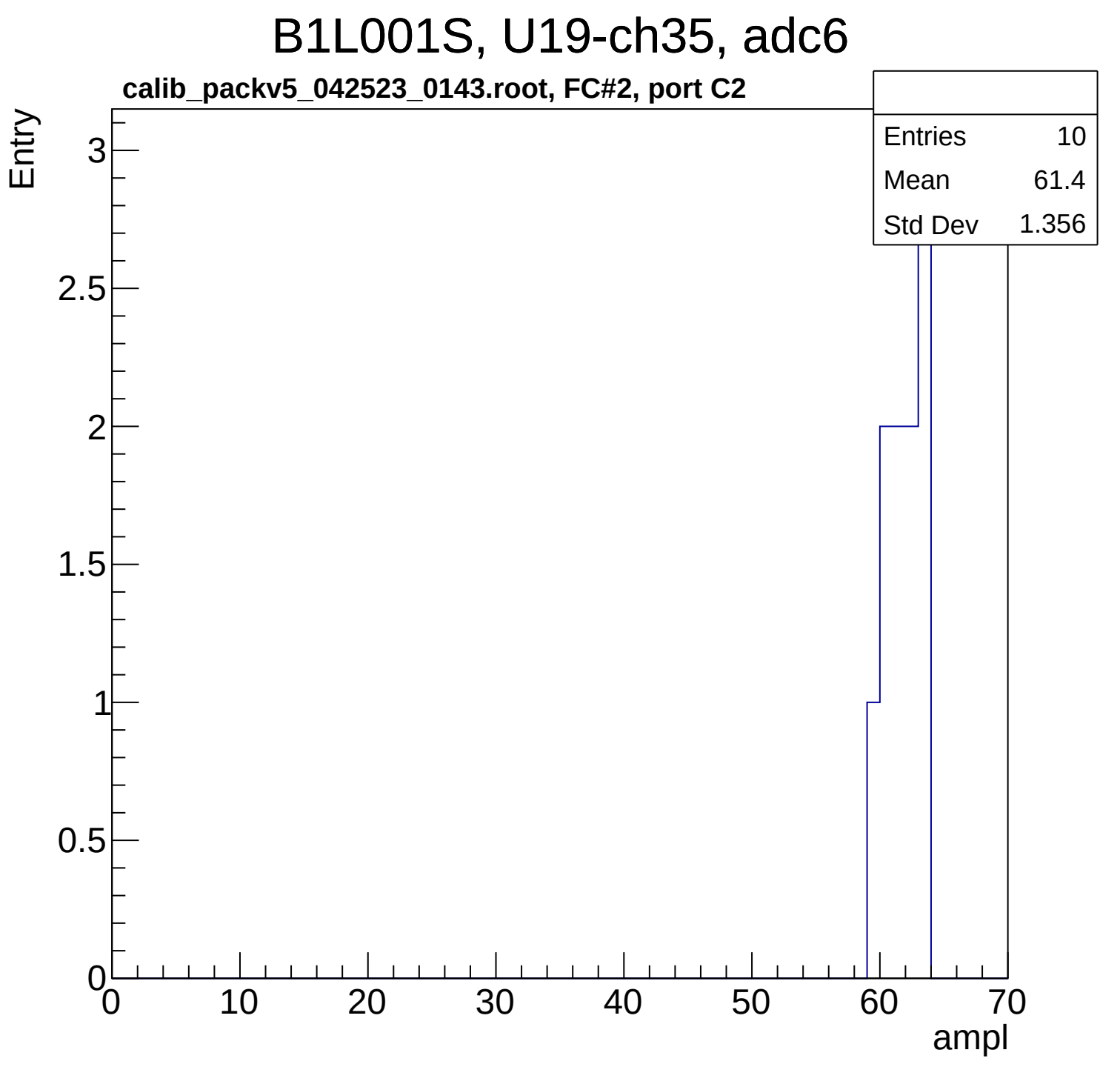
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch35, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 10
Mean 61.4
Std Dev 1.356
Entry
ampl
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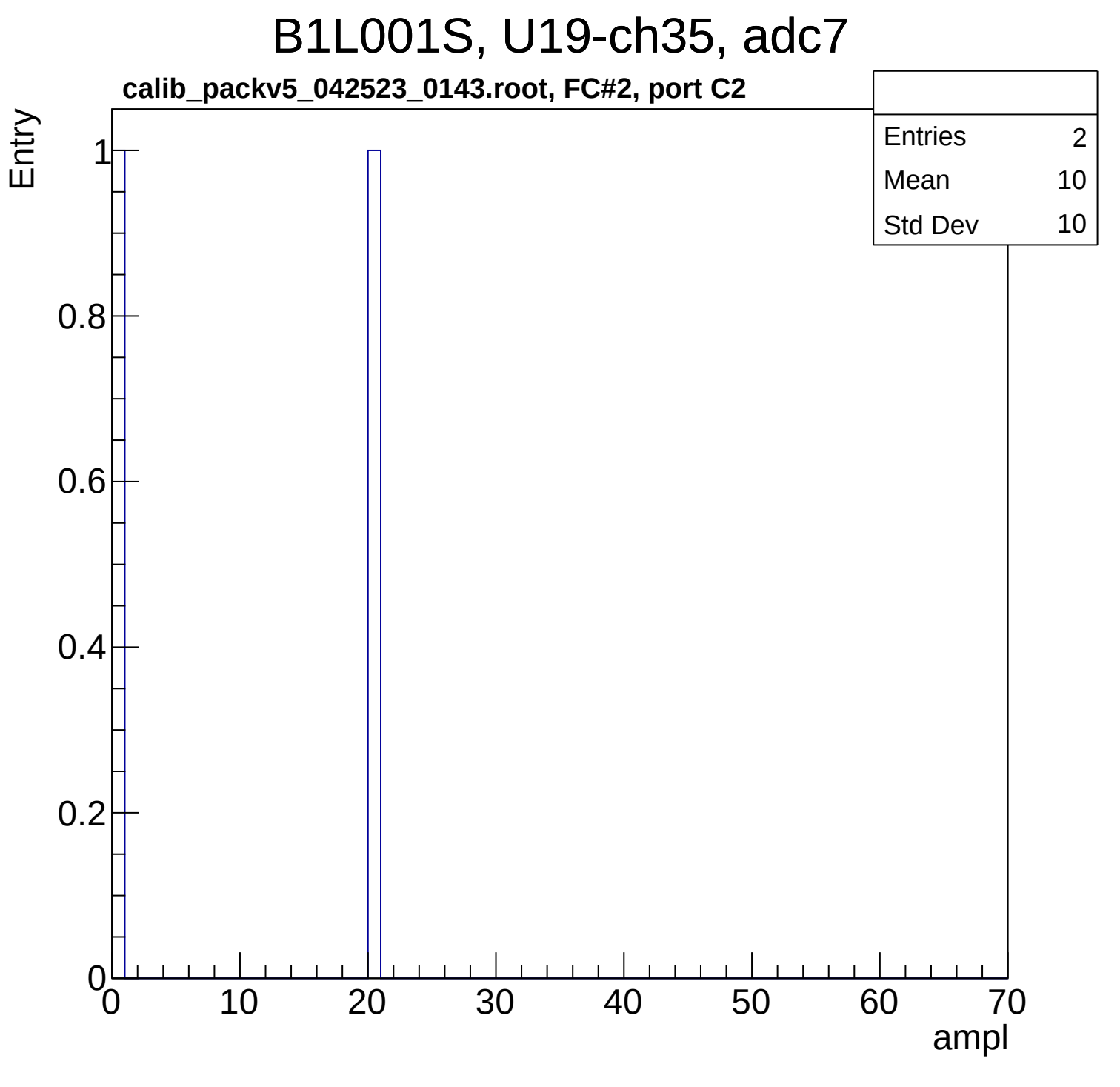
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L001S, U19-ch35, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 10
Std Dev 10
Entry
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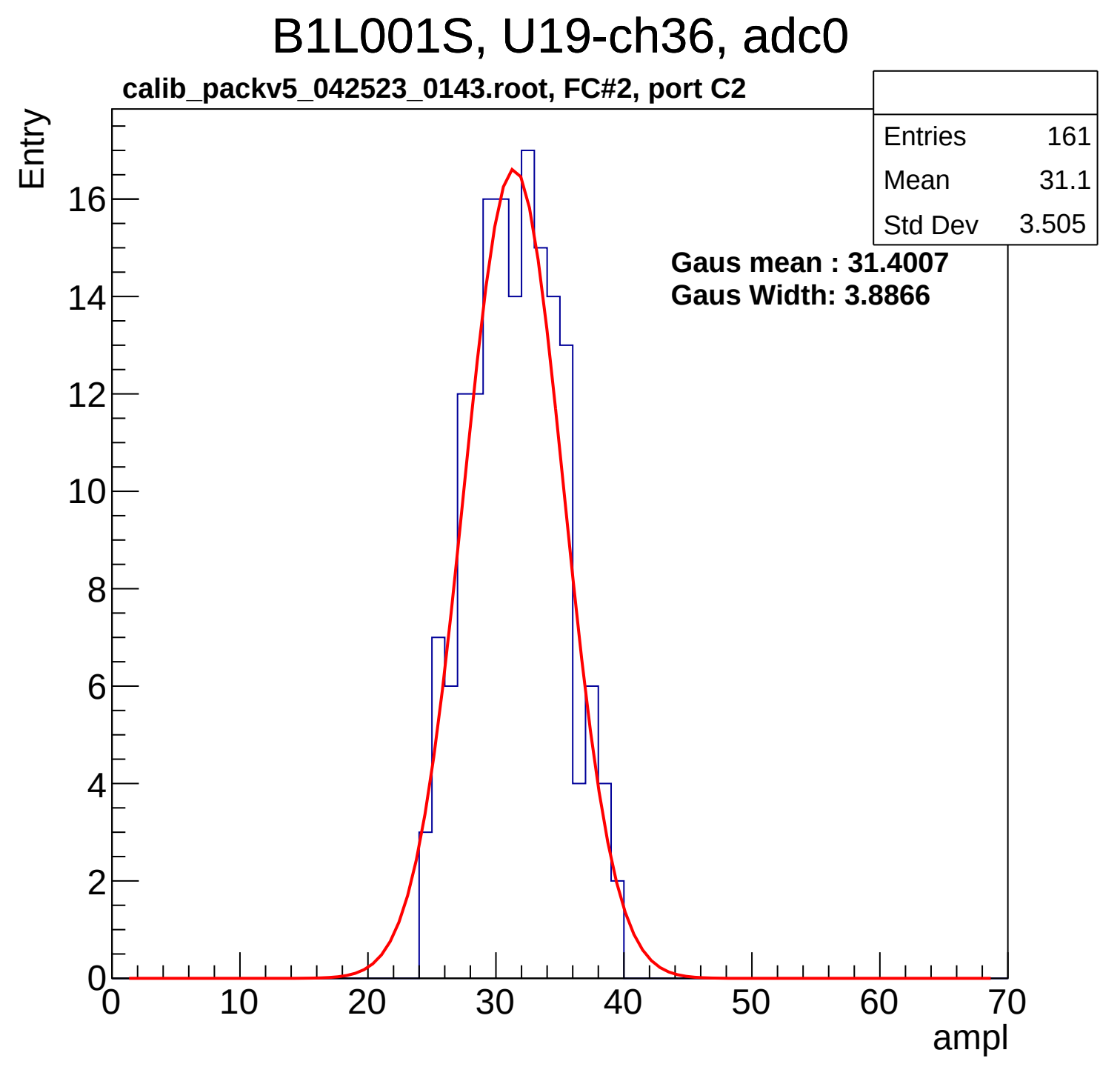
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch36, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 161
Mean 31.1
Std Dev 3.505
Gaus mean : 31.4007
Gaus Width: 3.8866
Entry
ampl
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4
6
8
10
12
14
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0
10
20
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40
50
60
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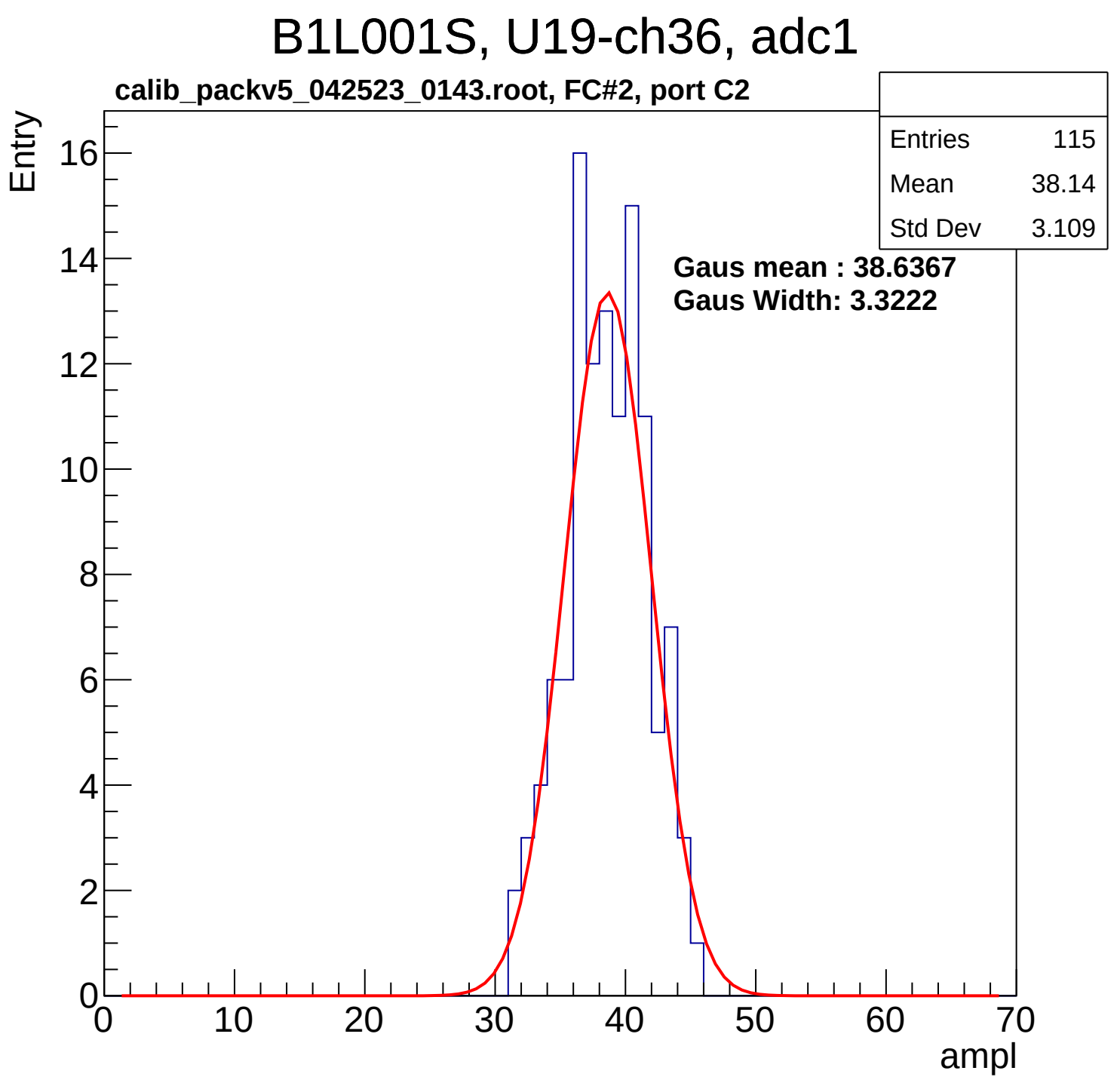
B1L001S, U19-ch36, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 115
Mean 38.14
Std Dev 3.109
Gaus mean : 38.6367
Gaus Width: 3.3222
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
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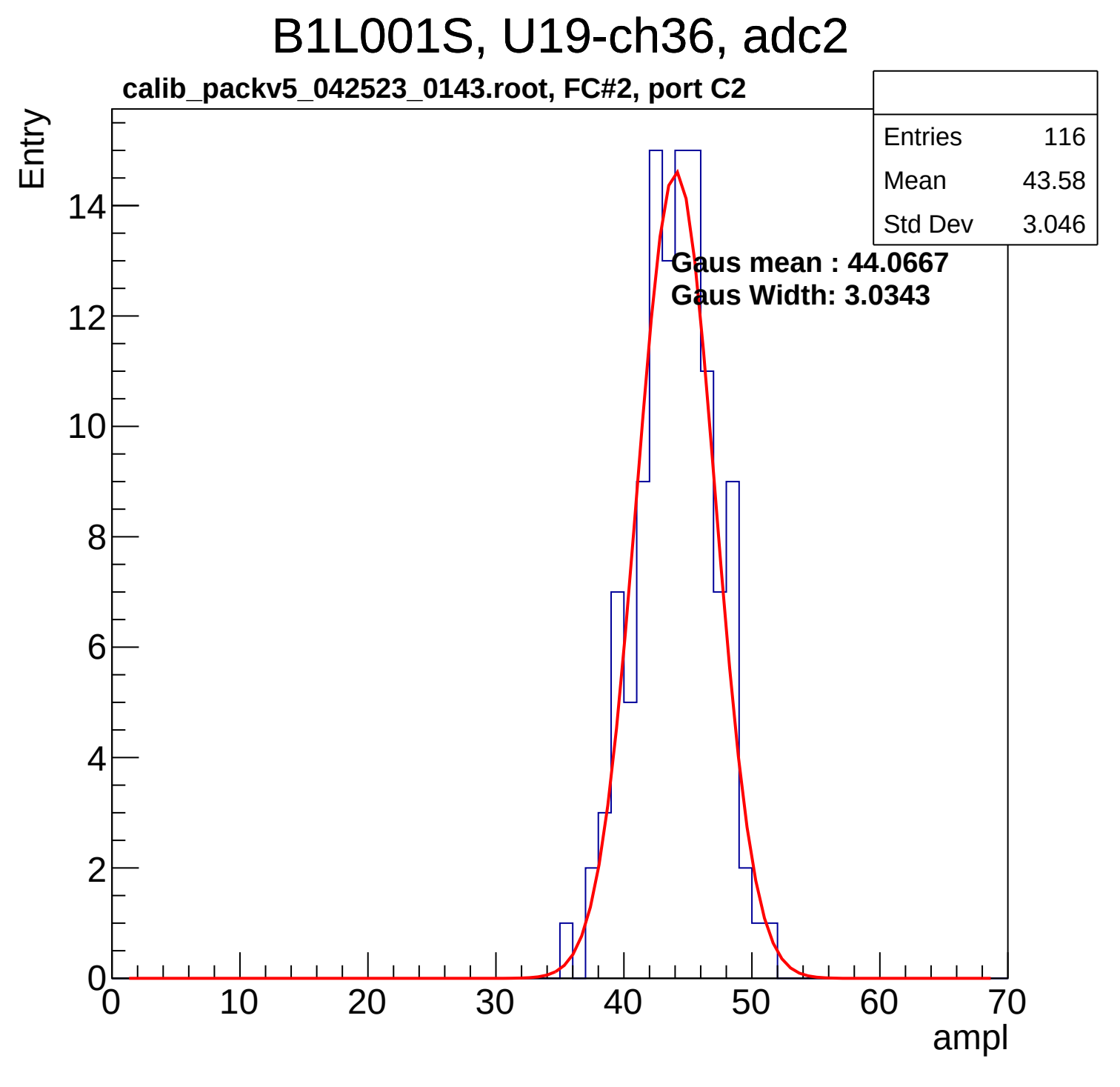
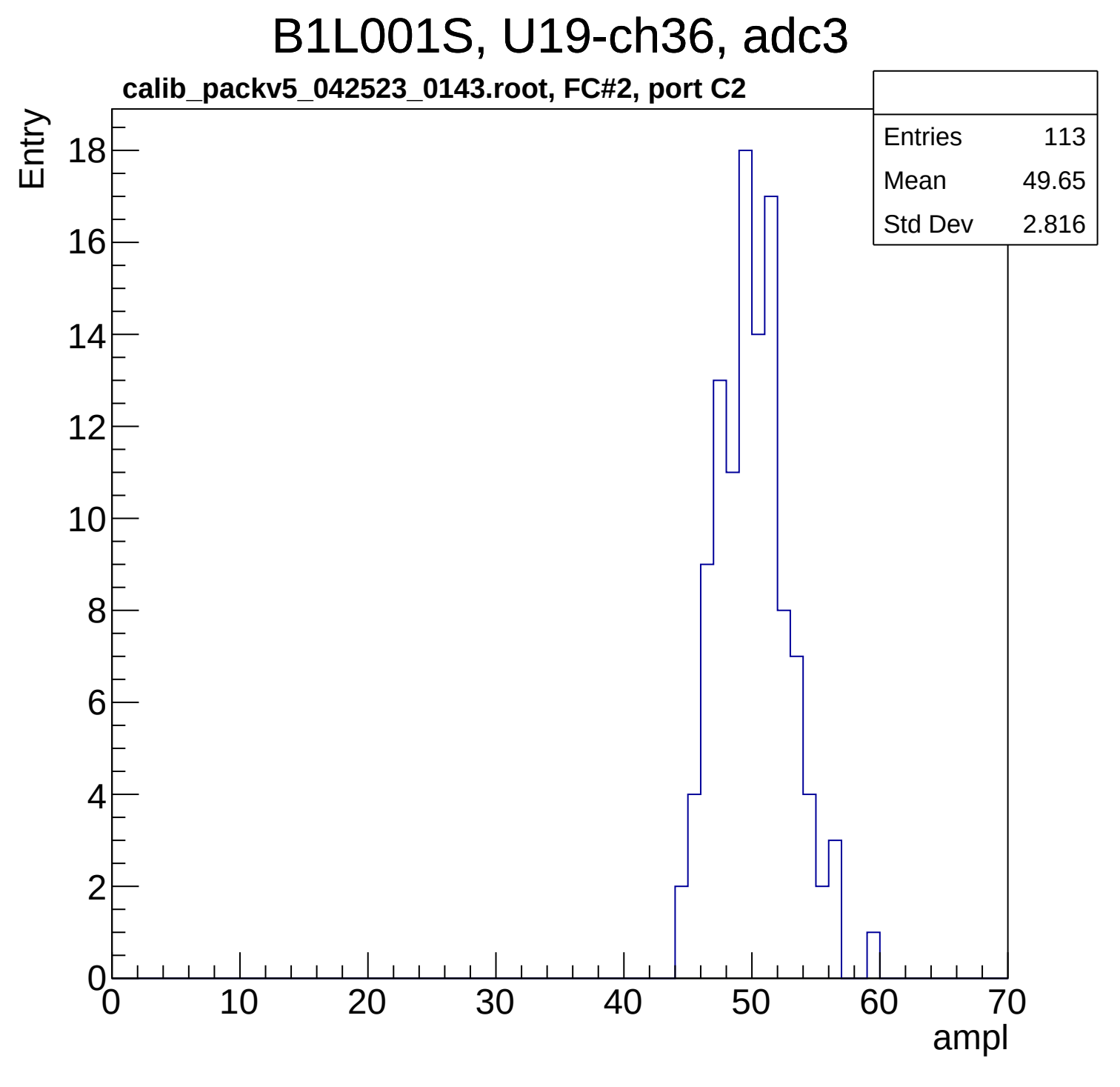
60
70


B1L001S, U19-ch36, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 116
Mean 43.58
Std Dev 3.046
Gaus mean : 44.0667
Gaus Width: 3.0343
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L001S, U19-ch36, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 113
Mean 49.65
Std Dev 2.816
Entry
ampl
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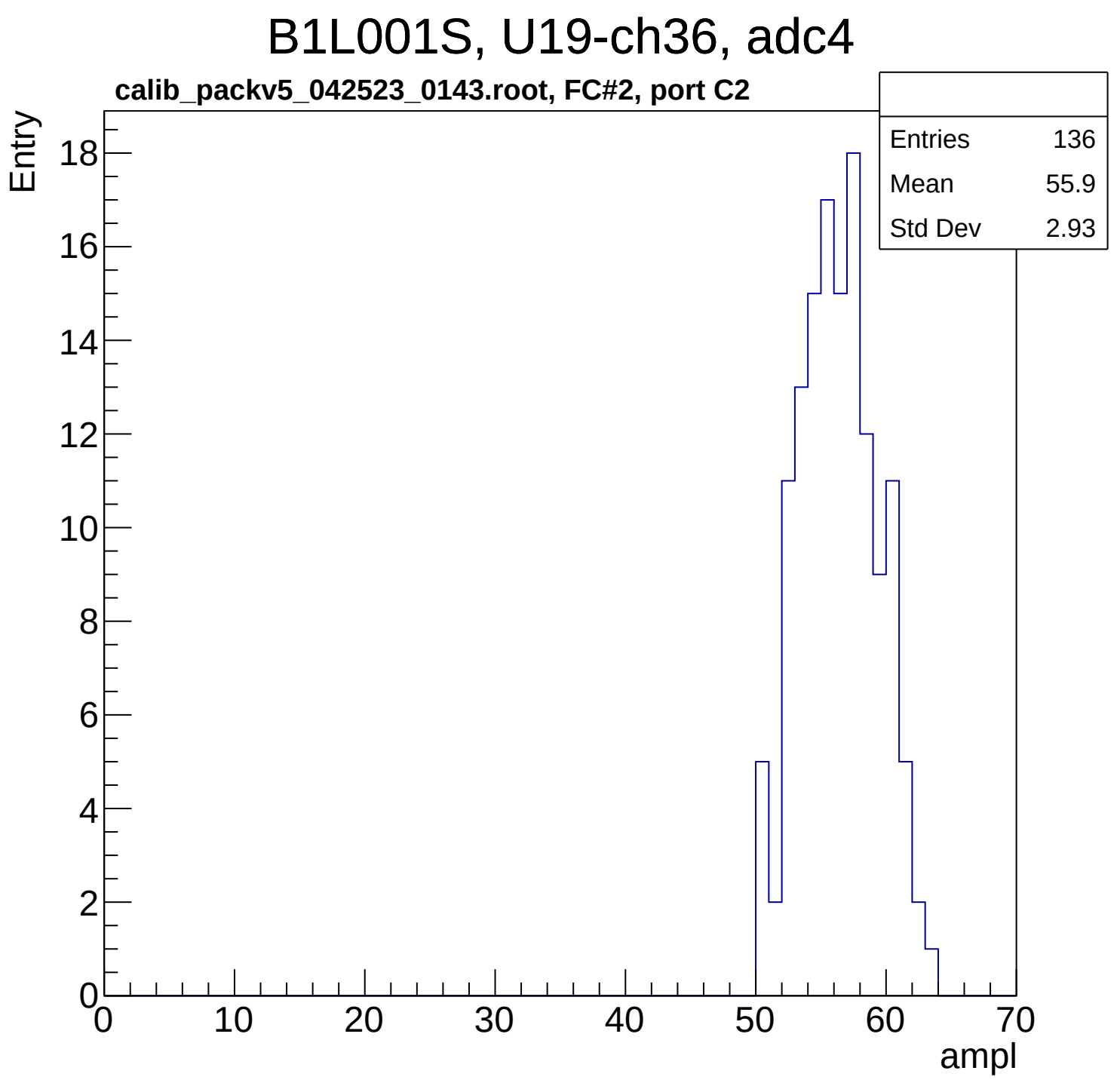
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70


B1L001S, U19-ch36, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 136
Mean 55.9
Std Dev 2.93
Entry
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6
8
10
12
14
16
18
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10
20
30
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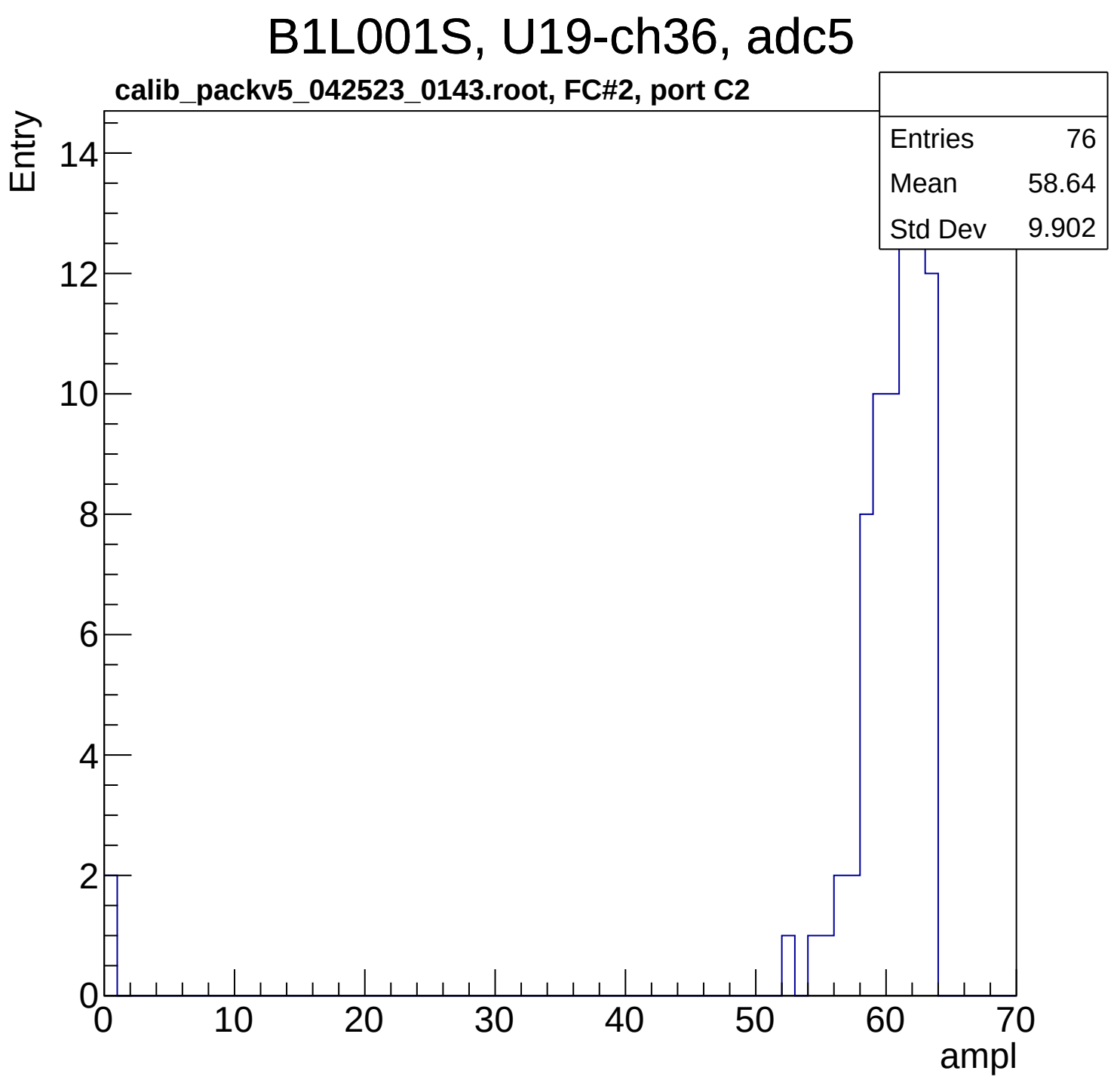
50
60
70
ampl


B1L001S, U19-ch36, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 76
Mean 58.64
Std Dev 9.902
Entry
ampl
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2
4
6
8
10
12
14
0
10
20
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40
50
60
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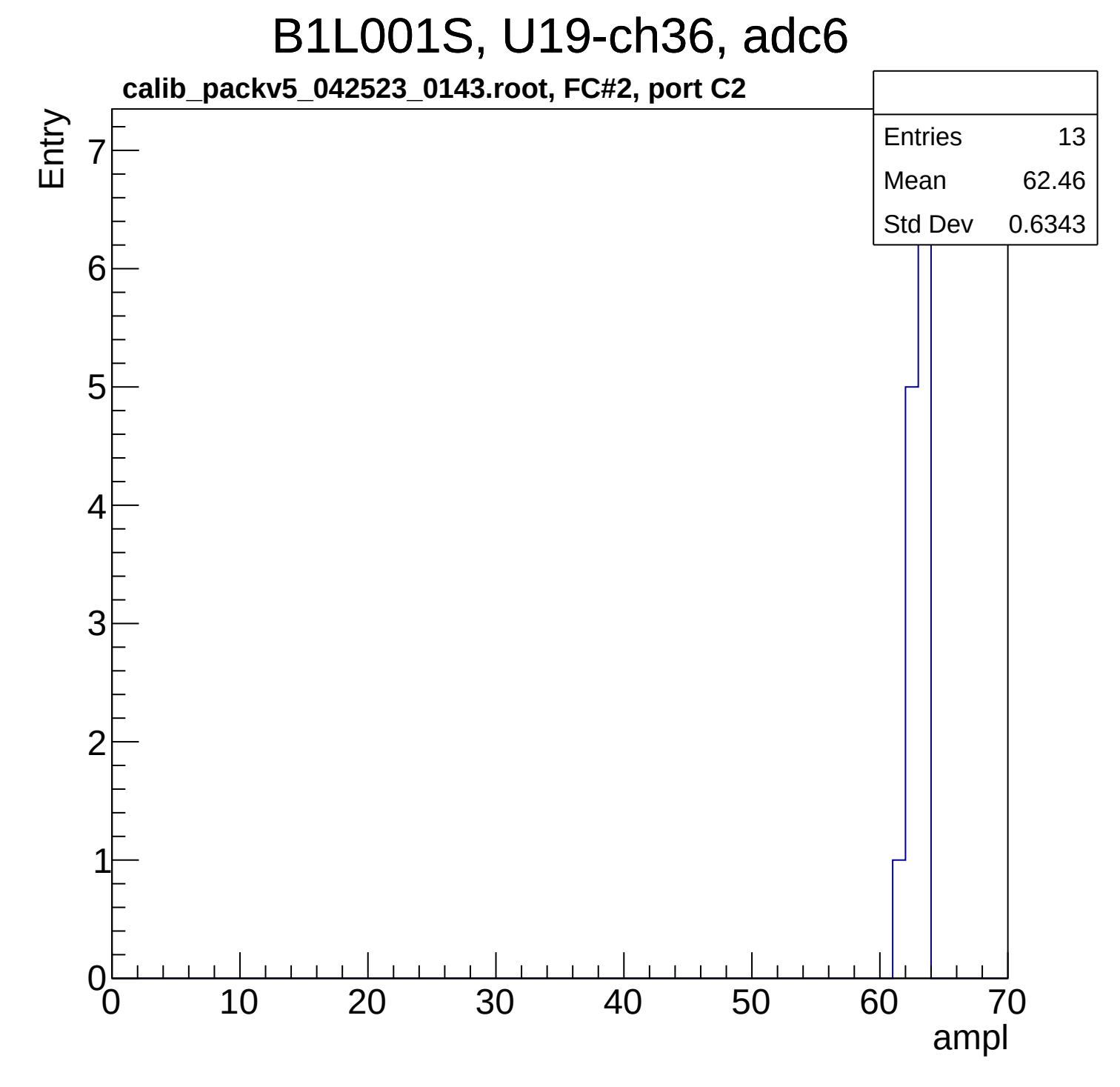
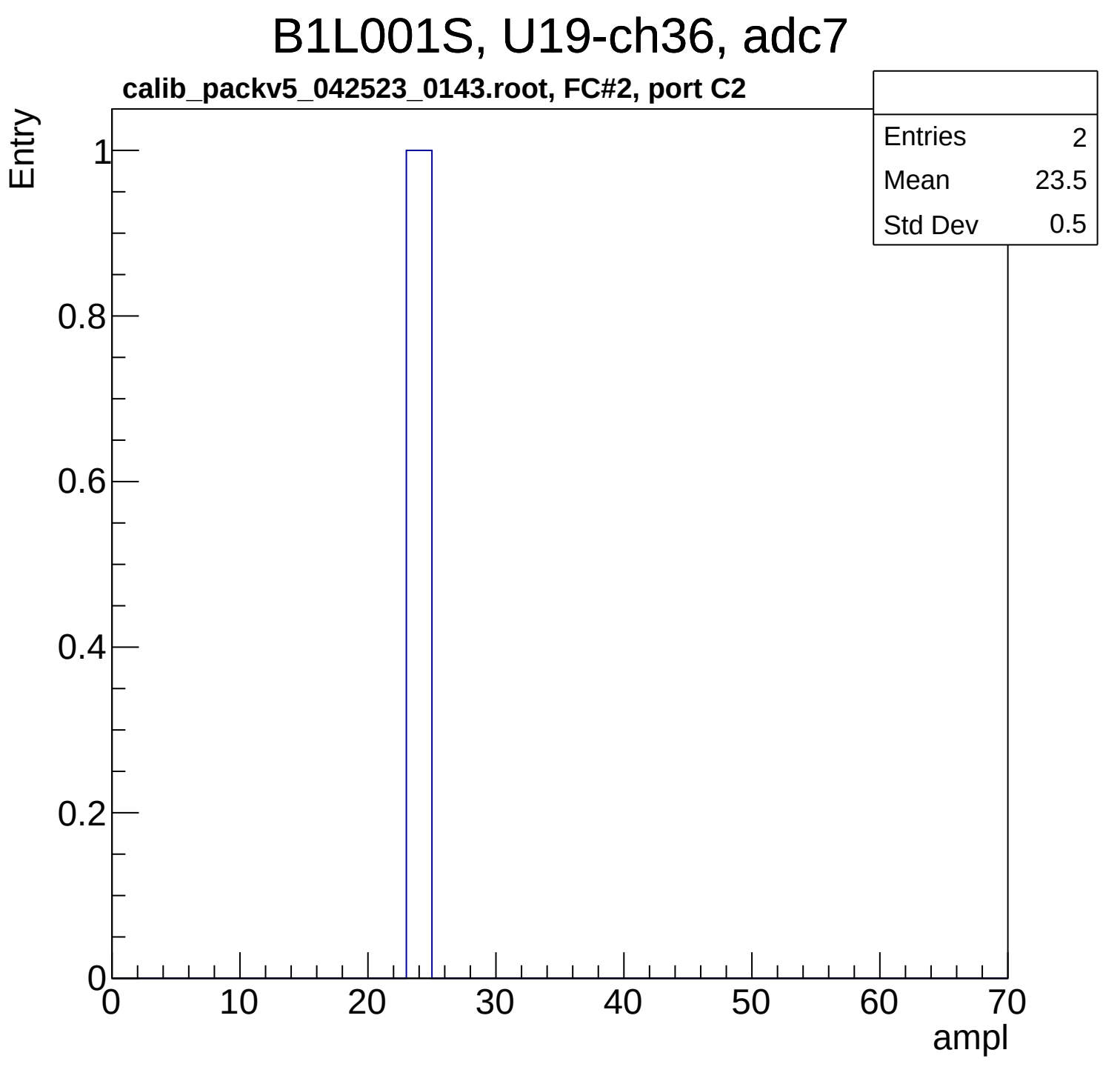

B1L001S, U19-ch36, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 13
Mean 62.46
Std Dev 0.6343
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L001S, U19-ch36, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 23.5
Std Dev 0.5
Entry
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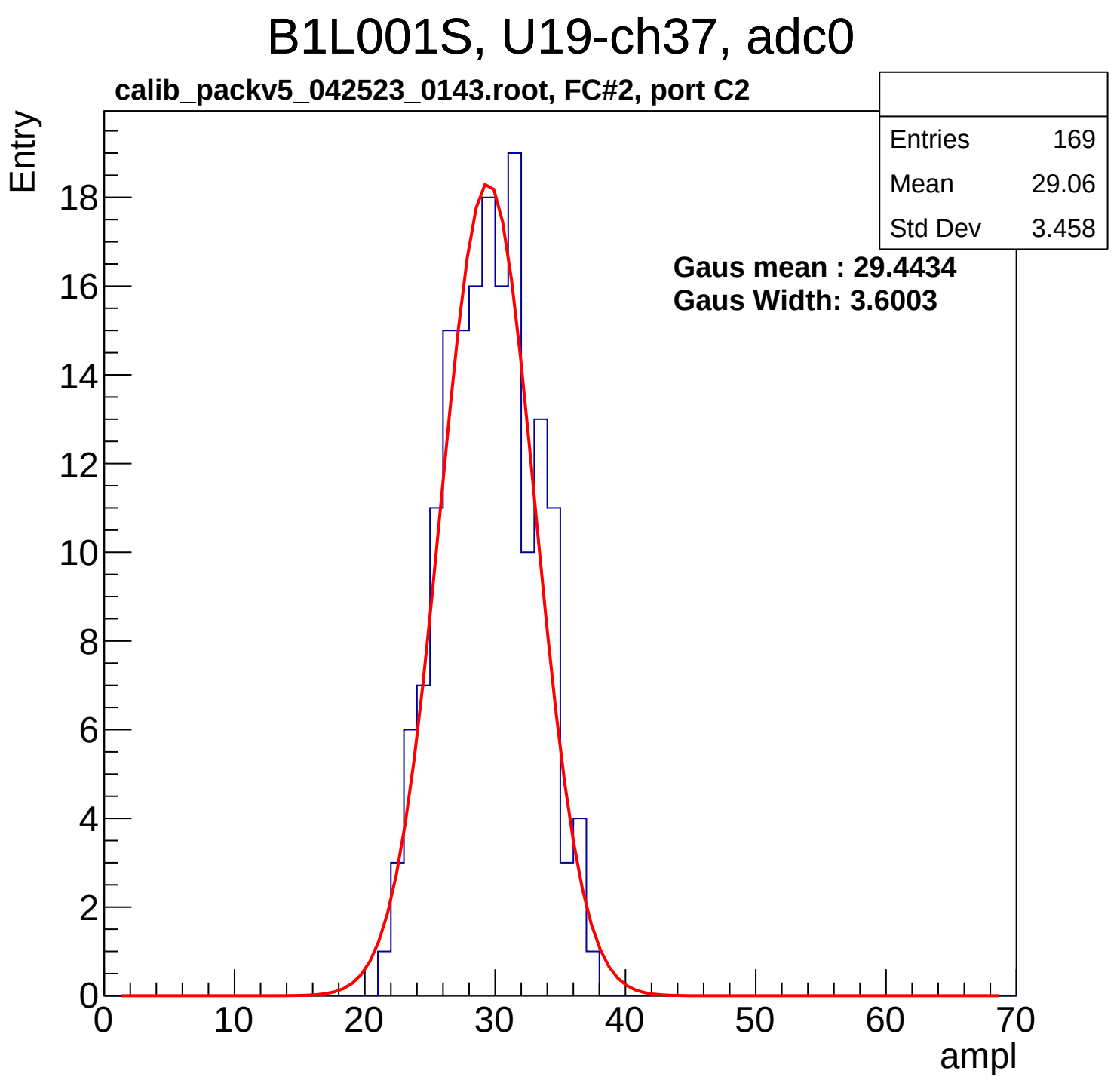
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch37, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 169
Mean 29.06
Std Dev 3.458
Gaus mean : 29.4434
Gaus Width: 3.6003
Entry
ampl
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4
6
8
10
12
14
16
18
0
10
20
30
40
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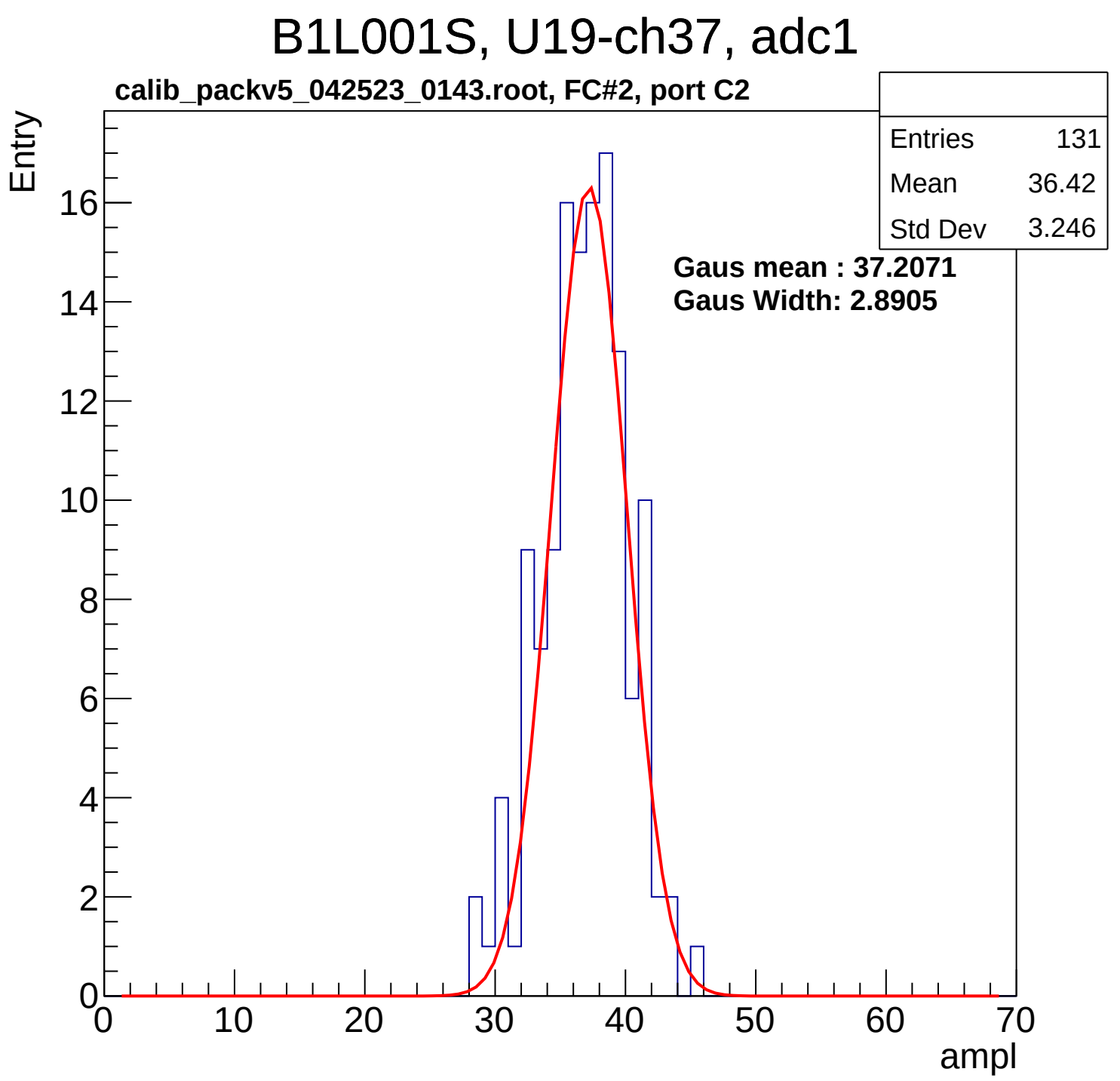
60
70


B1L001S, U19-ch37, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 131
Mean 36.42
Std Dev 3.246
Gaus mean : 37.2071
Gaus Width: 2.8905
Entry
ampl
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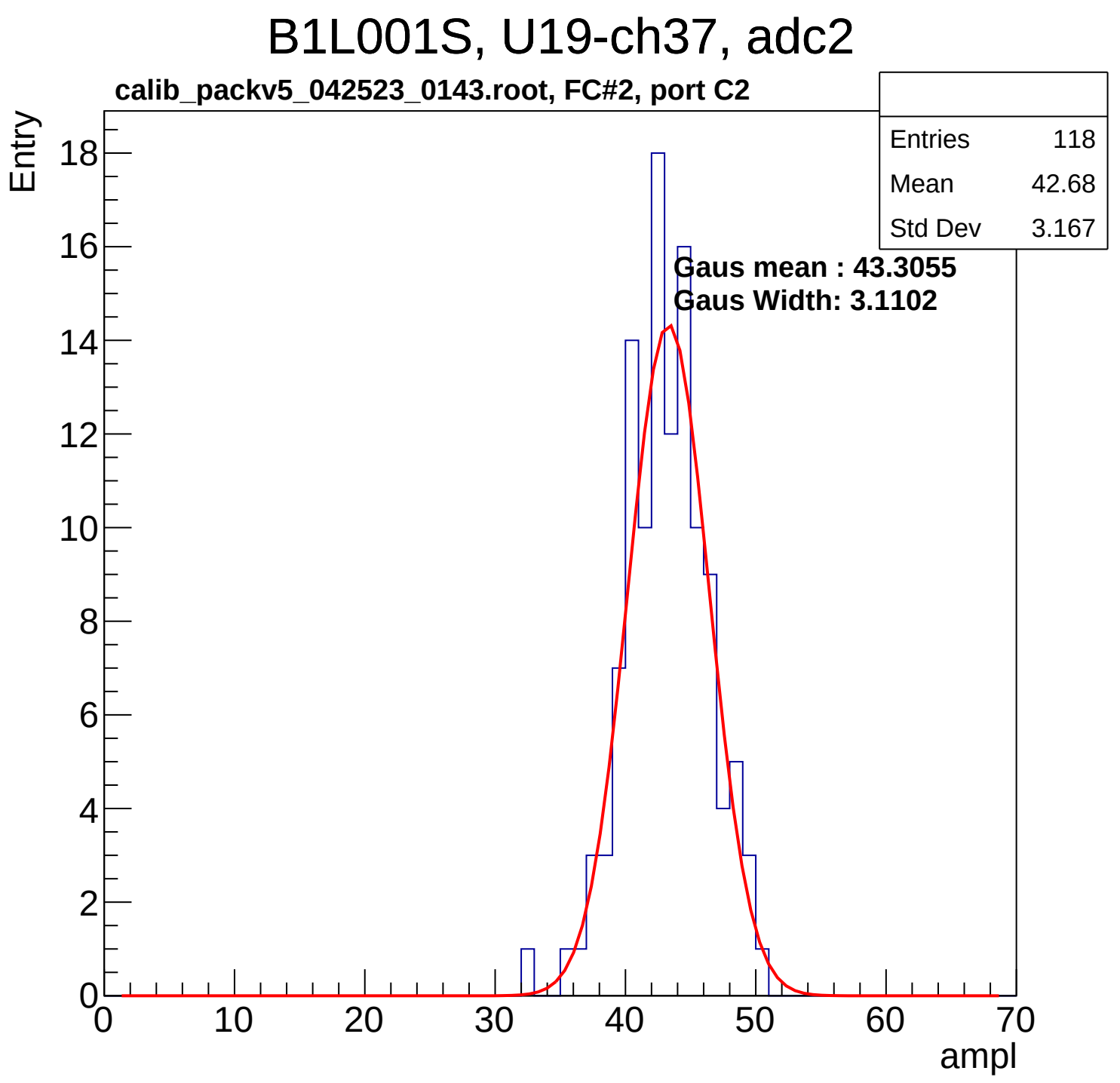
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70


B1L001S, U19-ch37, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 118
Mean 42.68
Std Dev 3.167
Gaus mean : 43.3055
Gaus Width: 3.1102
Entry
ampl
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6
8
10
12
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16
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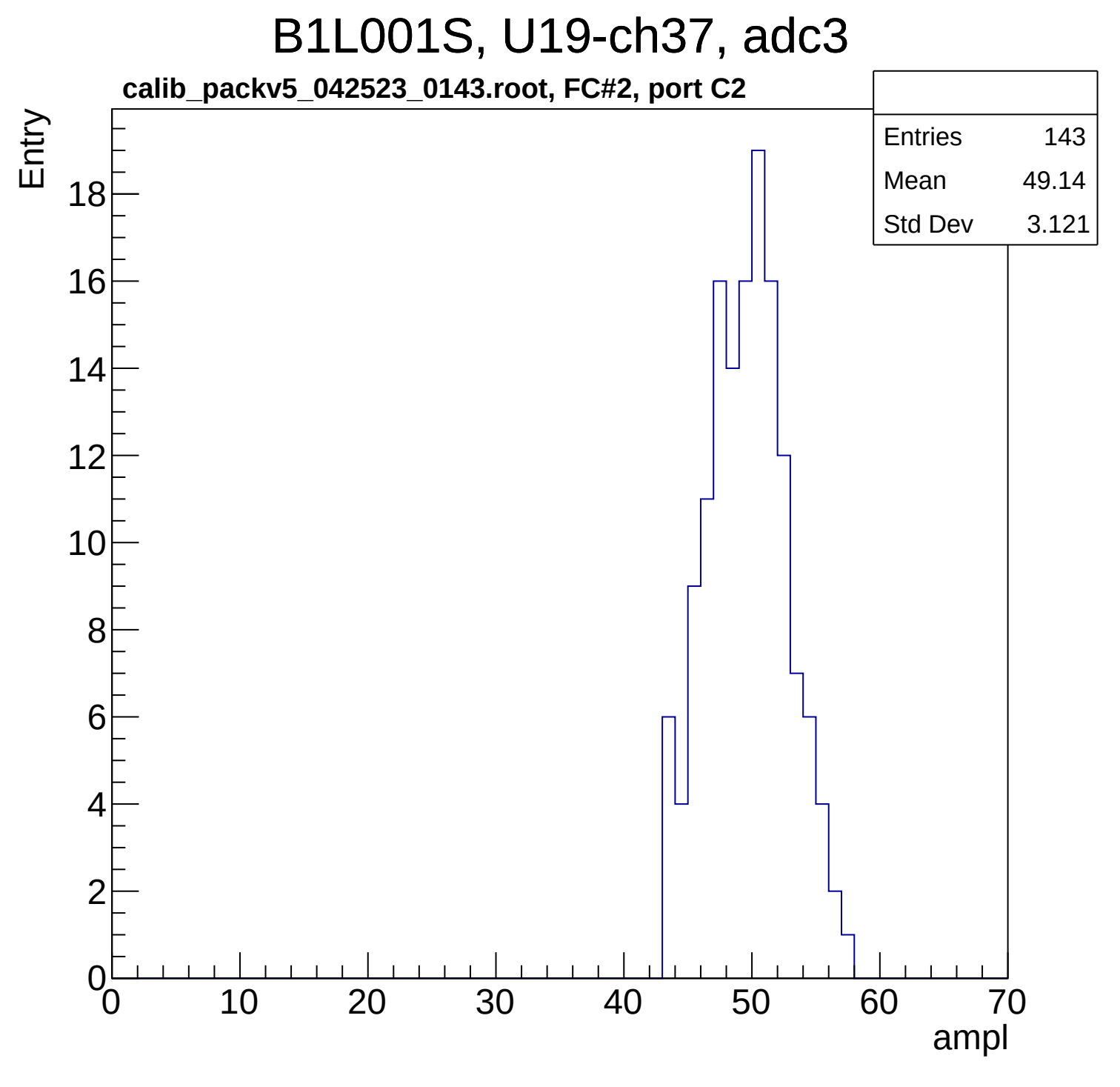
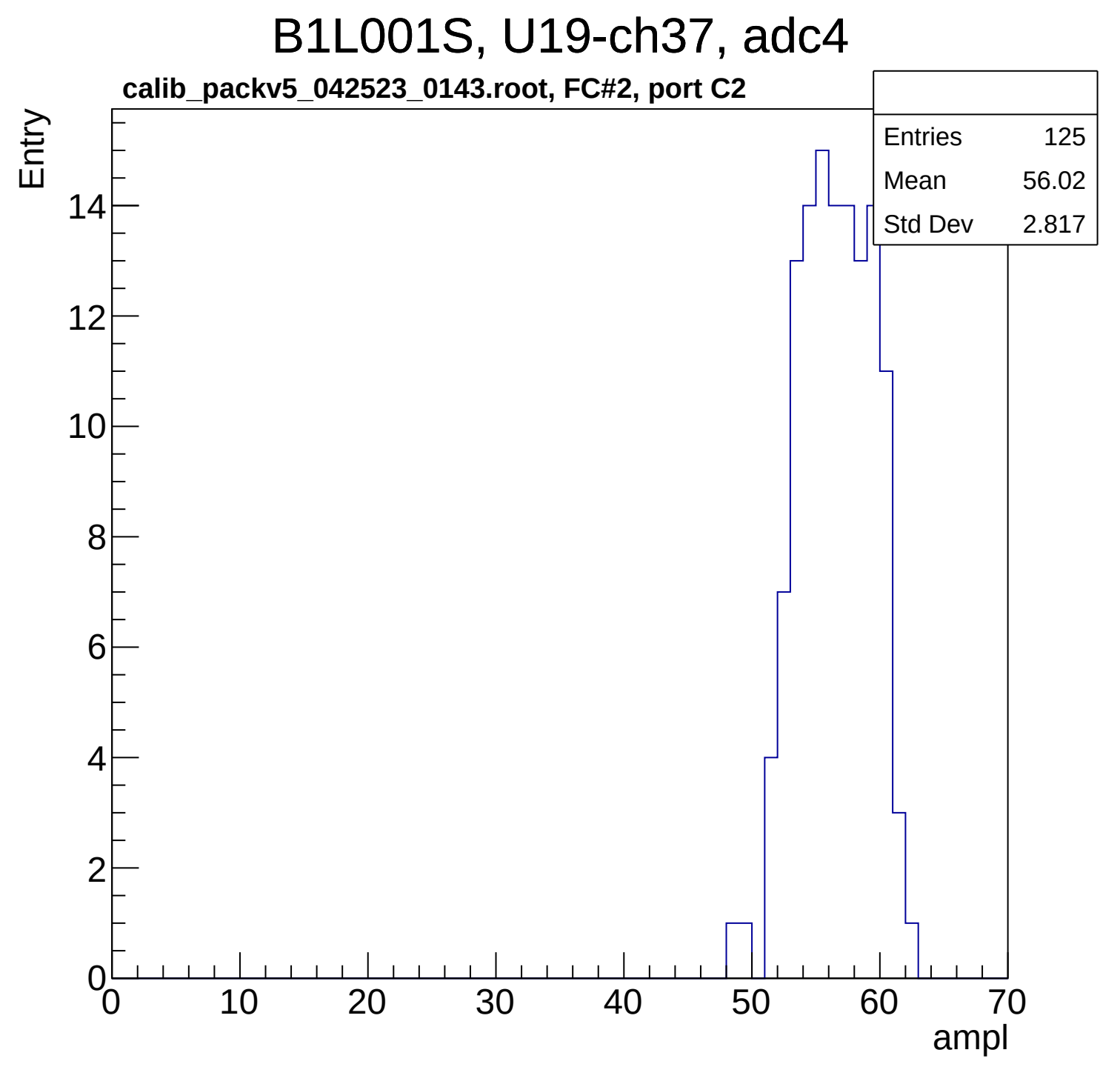

B1L001S, U19-ch37, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 143
Mean 49.14
Std Dev 3.121
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch37, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 125
Mean 56.02
Std Dev 2.817
Entry
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2
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6
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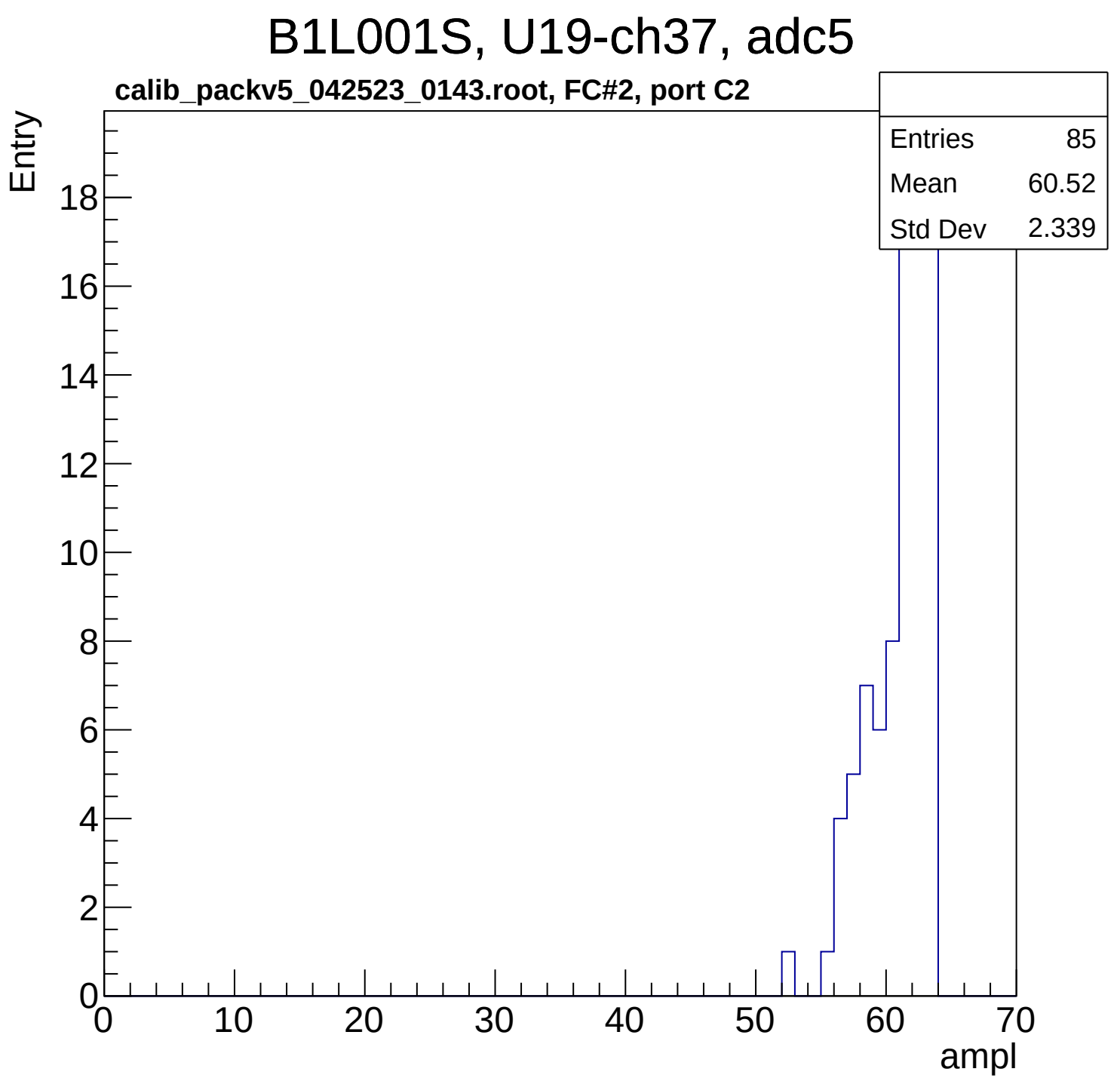
ampl


B1L001S, U19-ch37, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 85
Mean 60.52
Std Dev 2.339
Entry
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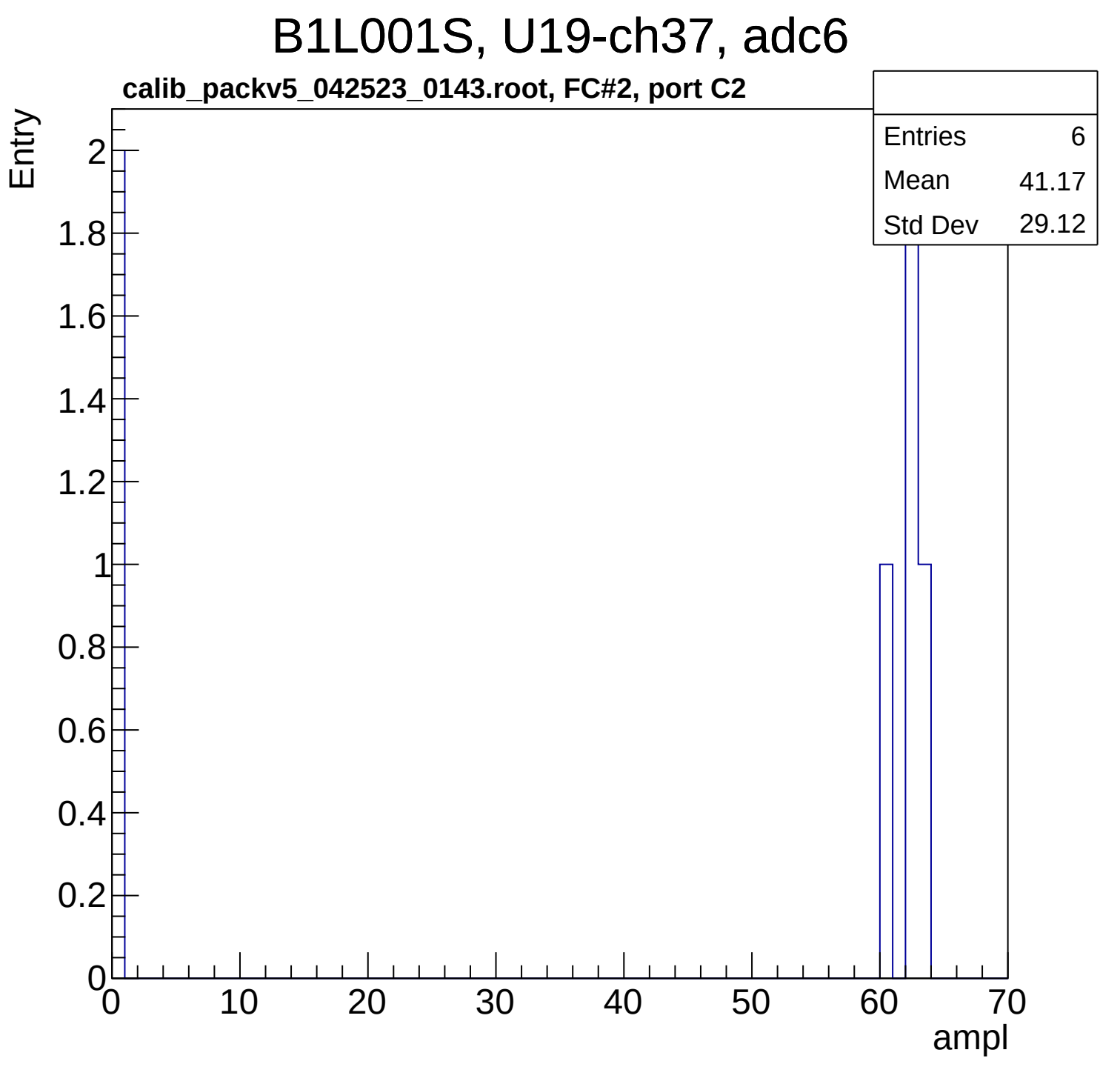
ampl


B1L001S, U19-ch37, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 6
Mean 41.17
Std Dev 29.12
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
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40
50
60
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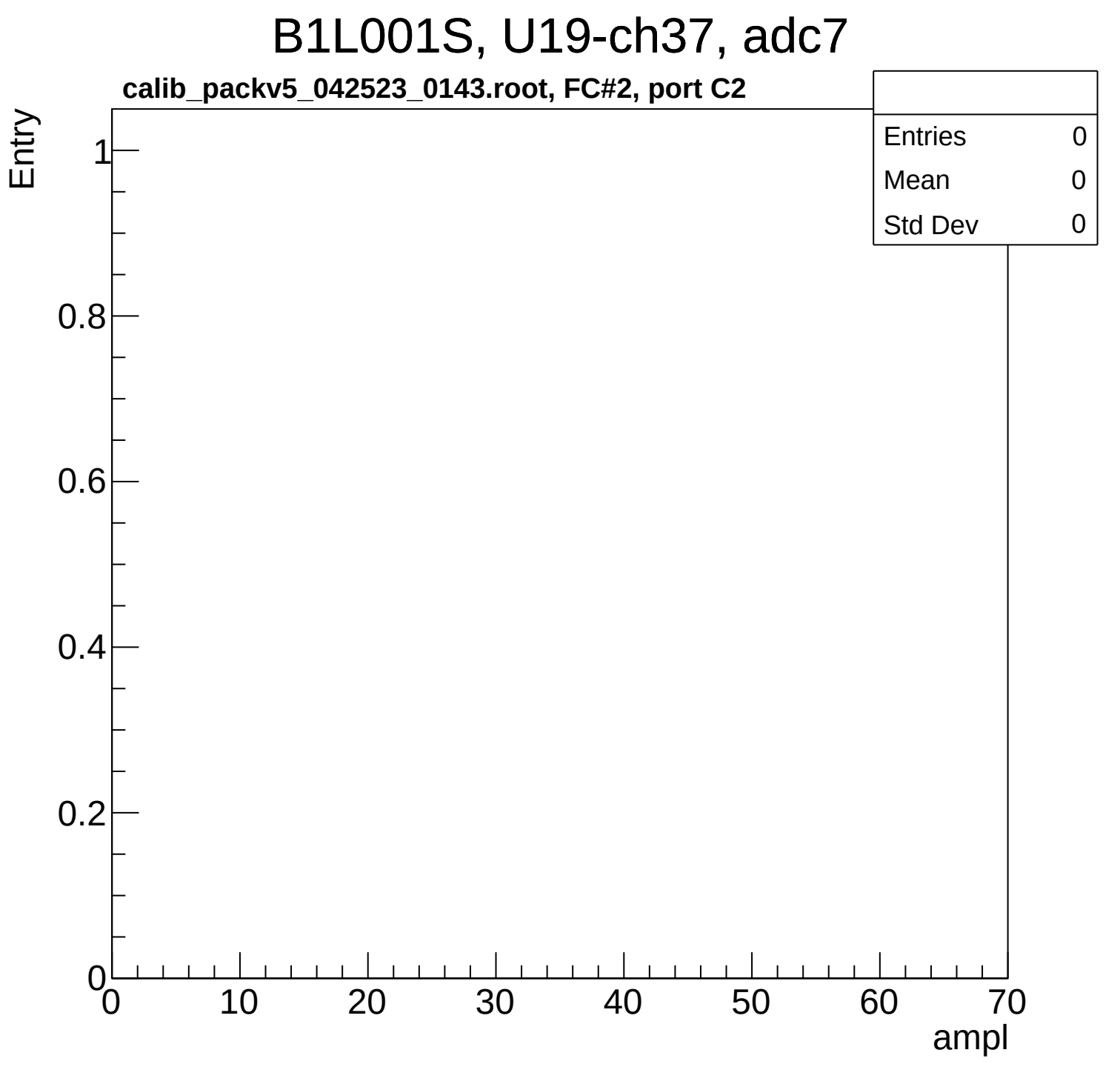
B1L001S, U19-ch37, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 0
Mean 0
Std Dev 0
Entry
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0.8
0.6
0.4
0.2
0
0
10
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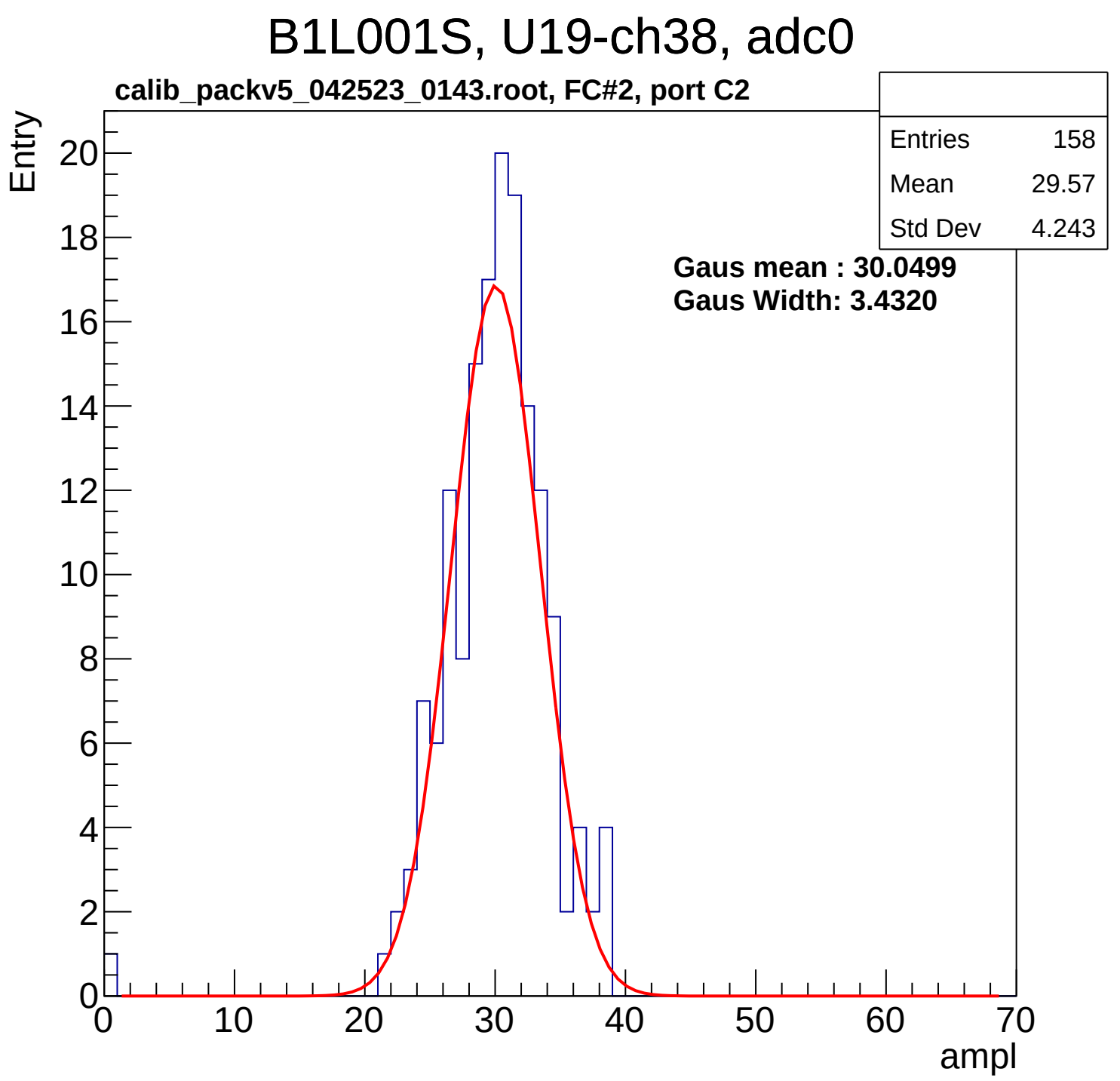
50
60
70
ampl


B1L001S, U19-ch38, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 158
Mean 29.57
Std Dev 4.243
Gaus mean : 30.0499
Gaus Width: 3.4320
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
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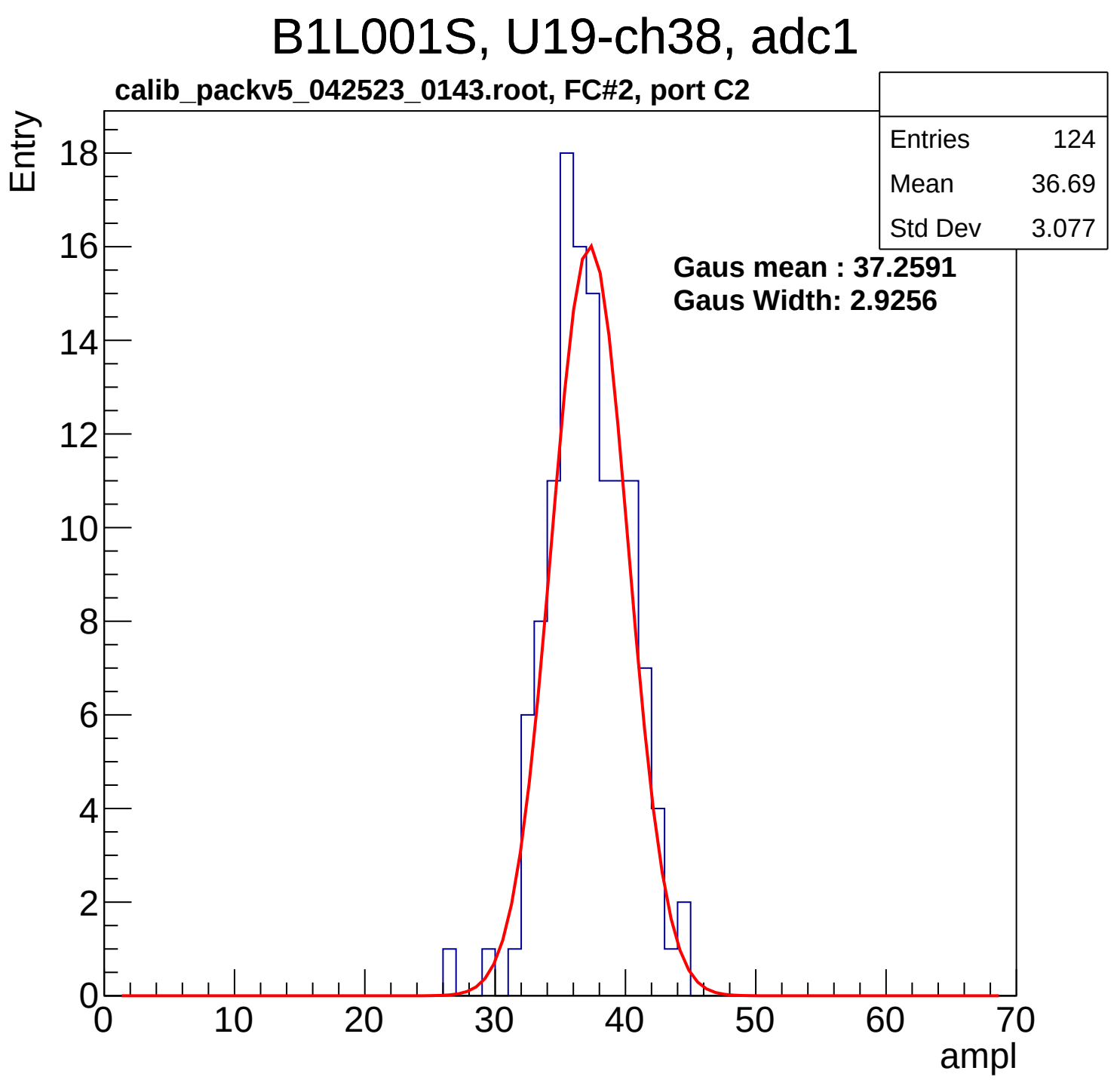
B1L001S, U19-ch38, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 124
Mean 36.69
Std Dev 3.077
Gaus mean : 37.2591
Gaus Width: 2.9256
Entry
ampl
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2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
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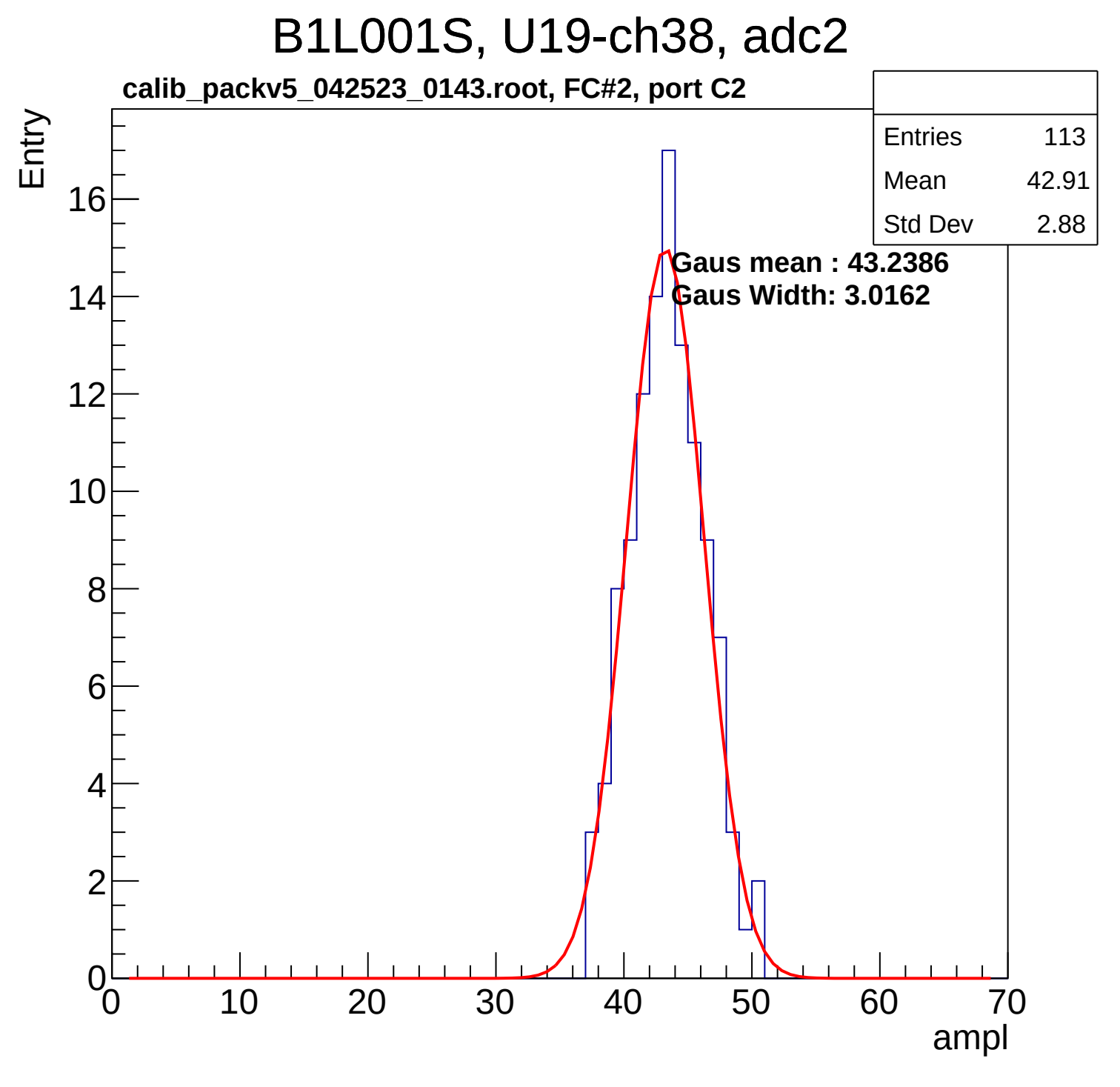
B1L001S, U19-ch38, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 113
Mean 42.91
Std Dev 2.88
Gaus mean : 43.2386
Gaus Width: 3.0162
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
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40
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60
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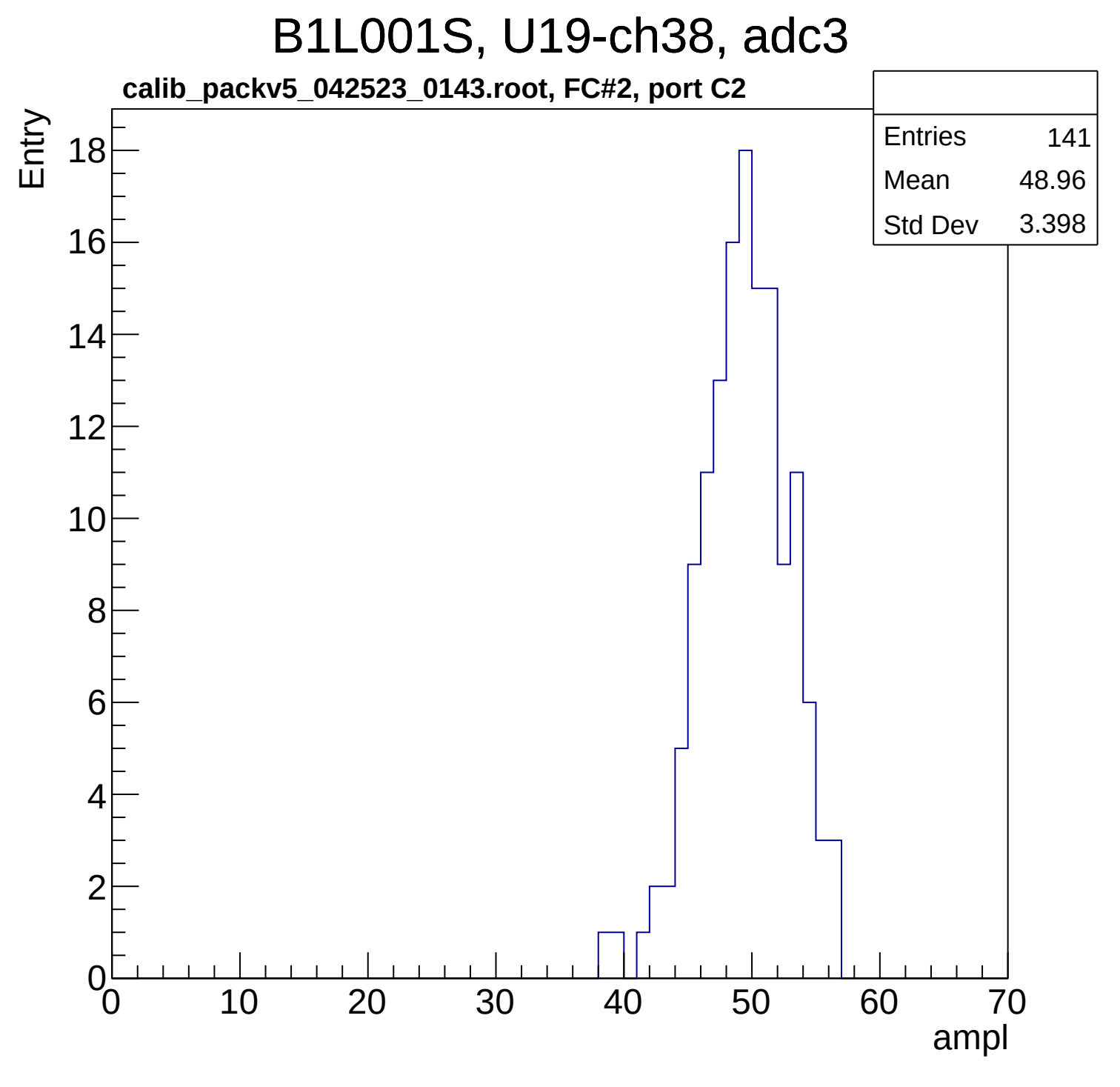
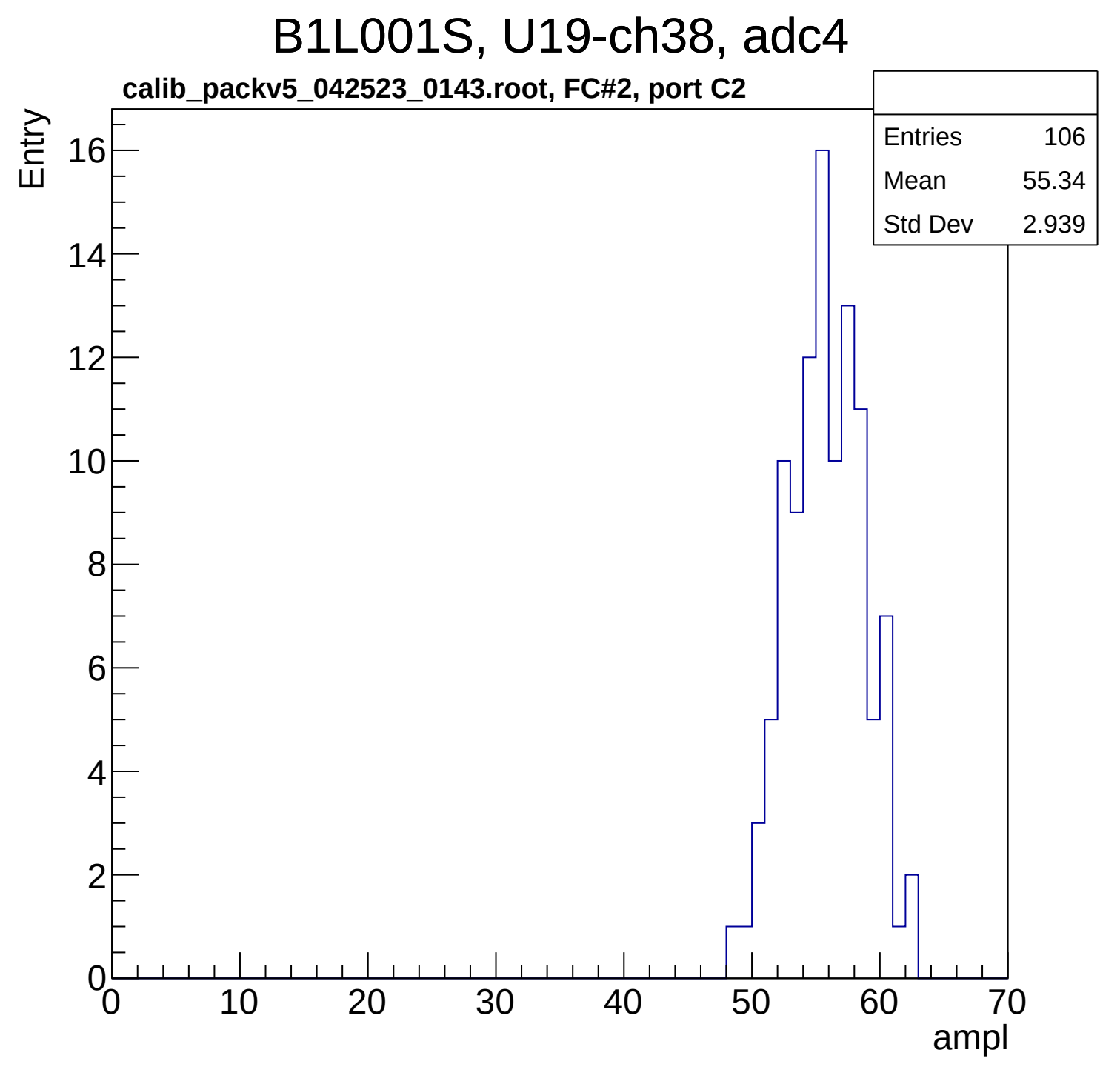

B1L001S, U19-ch38, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 141
Mean 48.96
Std Dev 3.398
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70


B1L001S, U19-ch38, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 106
Mean 55.34
Std Dev 2.939
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
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60
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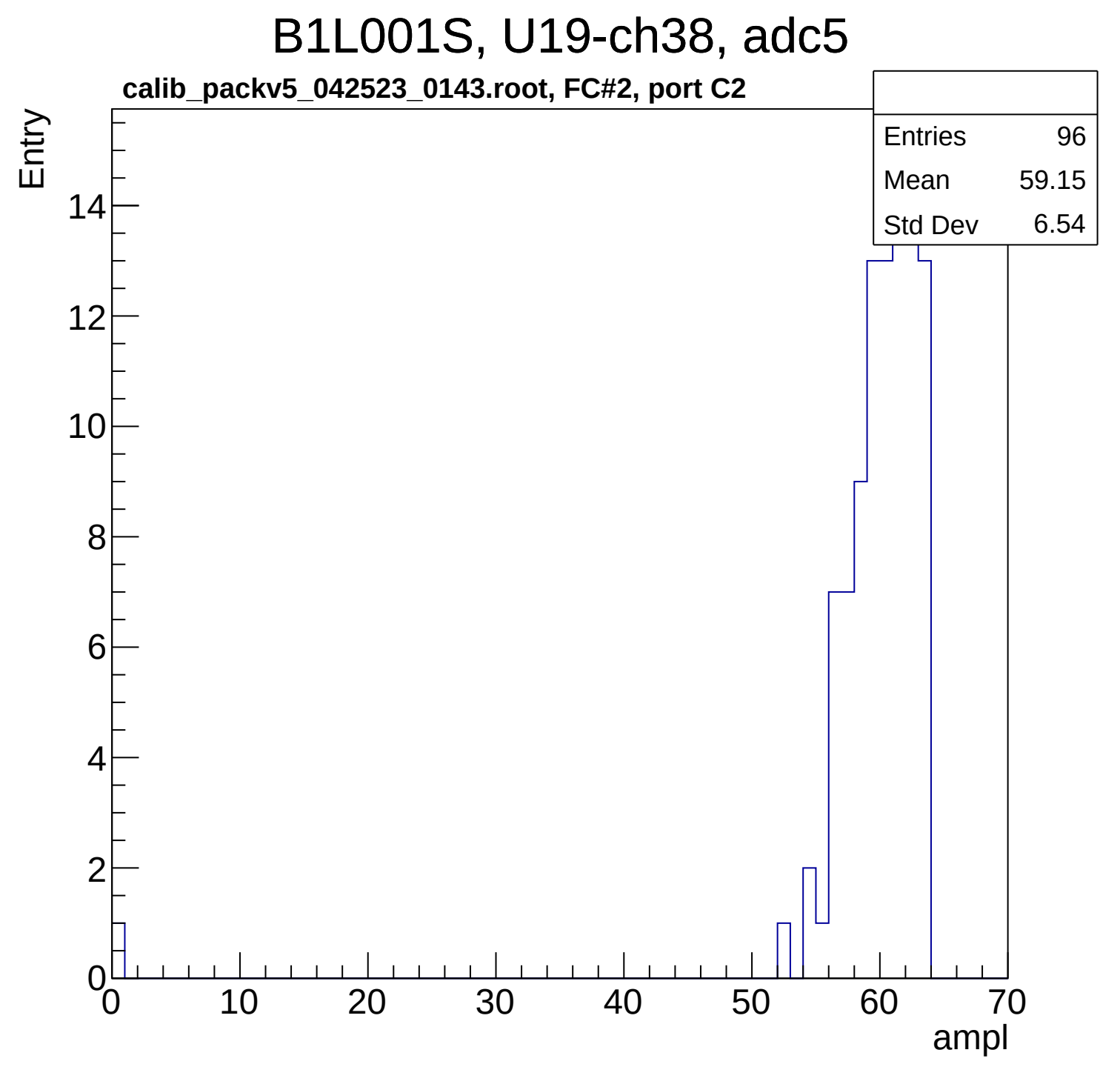
B1L001S, U19-ch38, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 96
Mean 59.15
Std Dev 6.54
Entry
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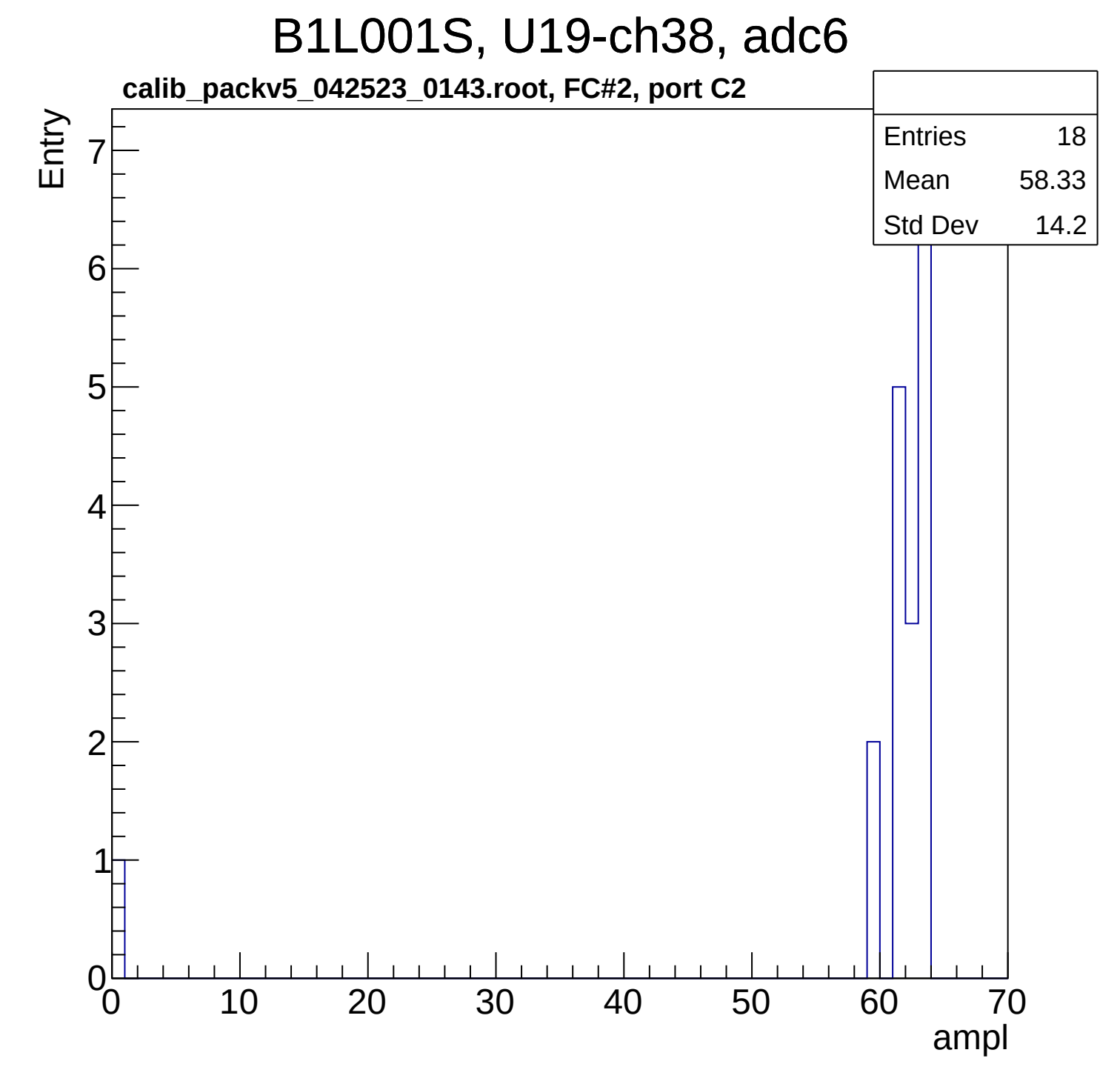
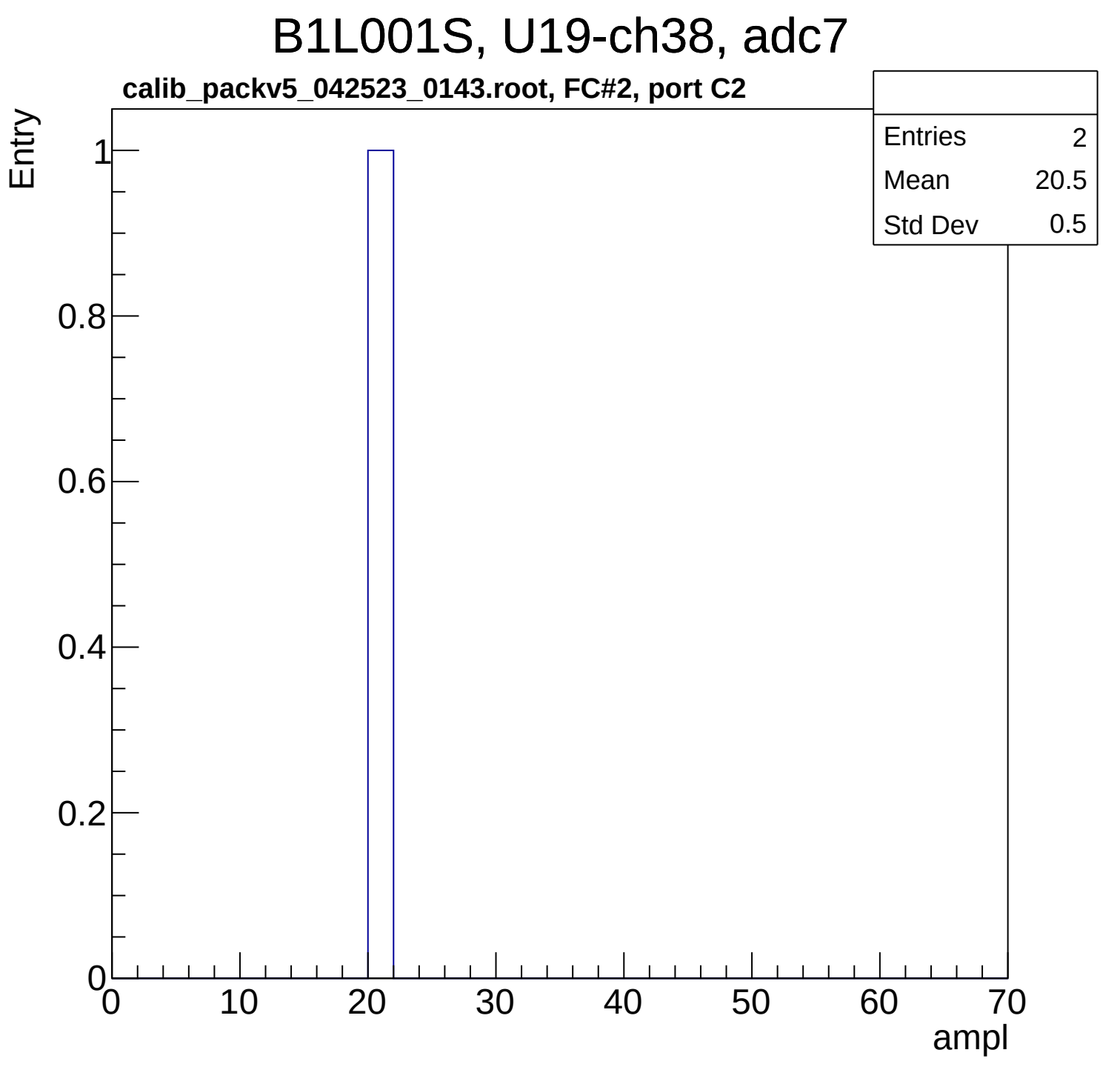
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch38, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 18
Mean 58.33
Std Dev 14.2
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L001S, U19-ch38, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 20.5
Std Dev 0.5
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
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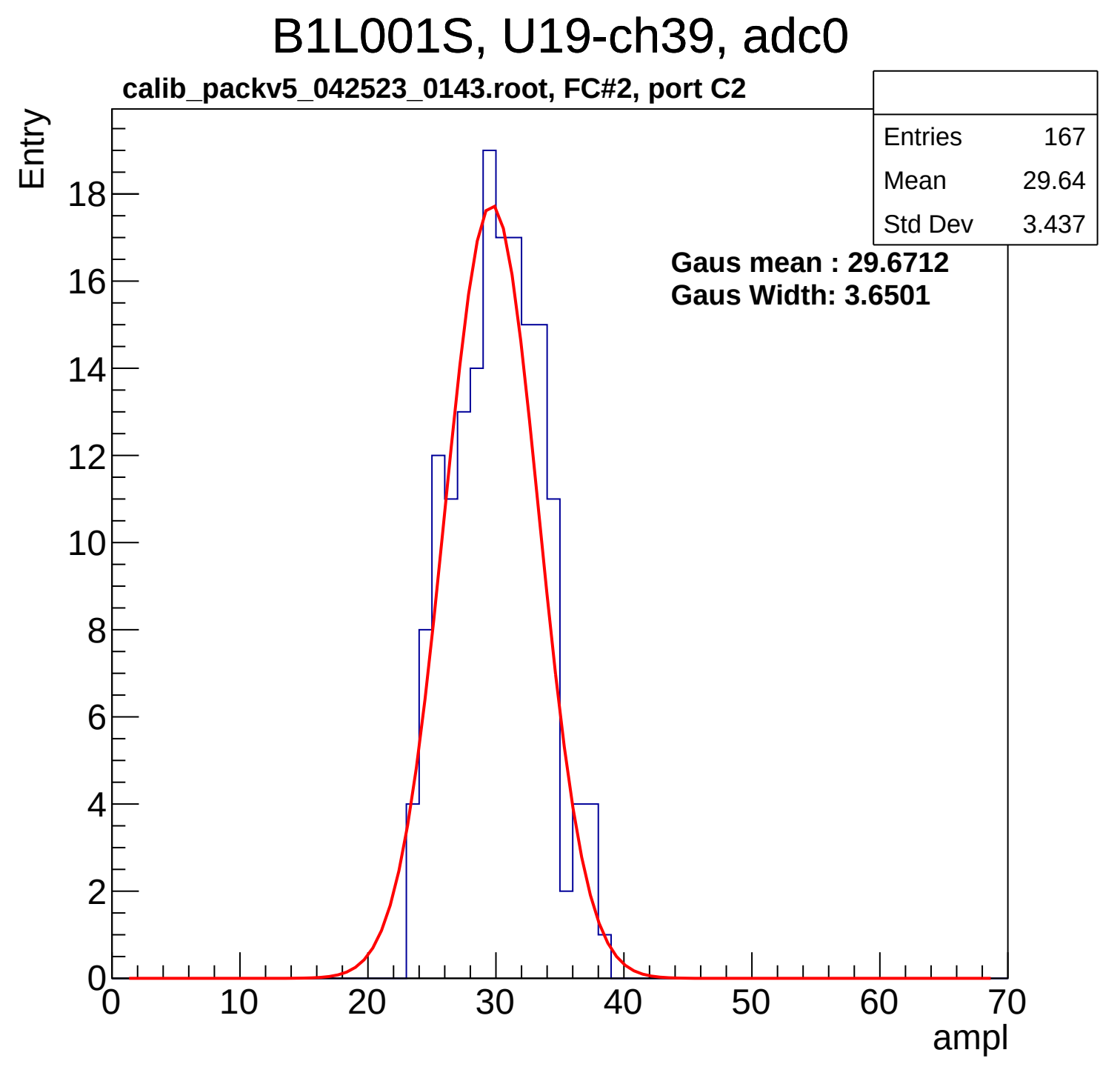
B1L001S, U19-ch39, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 167
Mean 29.64
Std Dev 3.437
Gaus mean : 29.6712
Gaus Width: 3.6501
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
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40
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60
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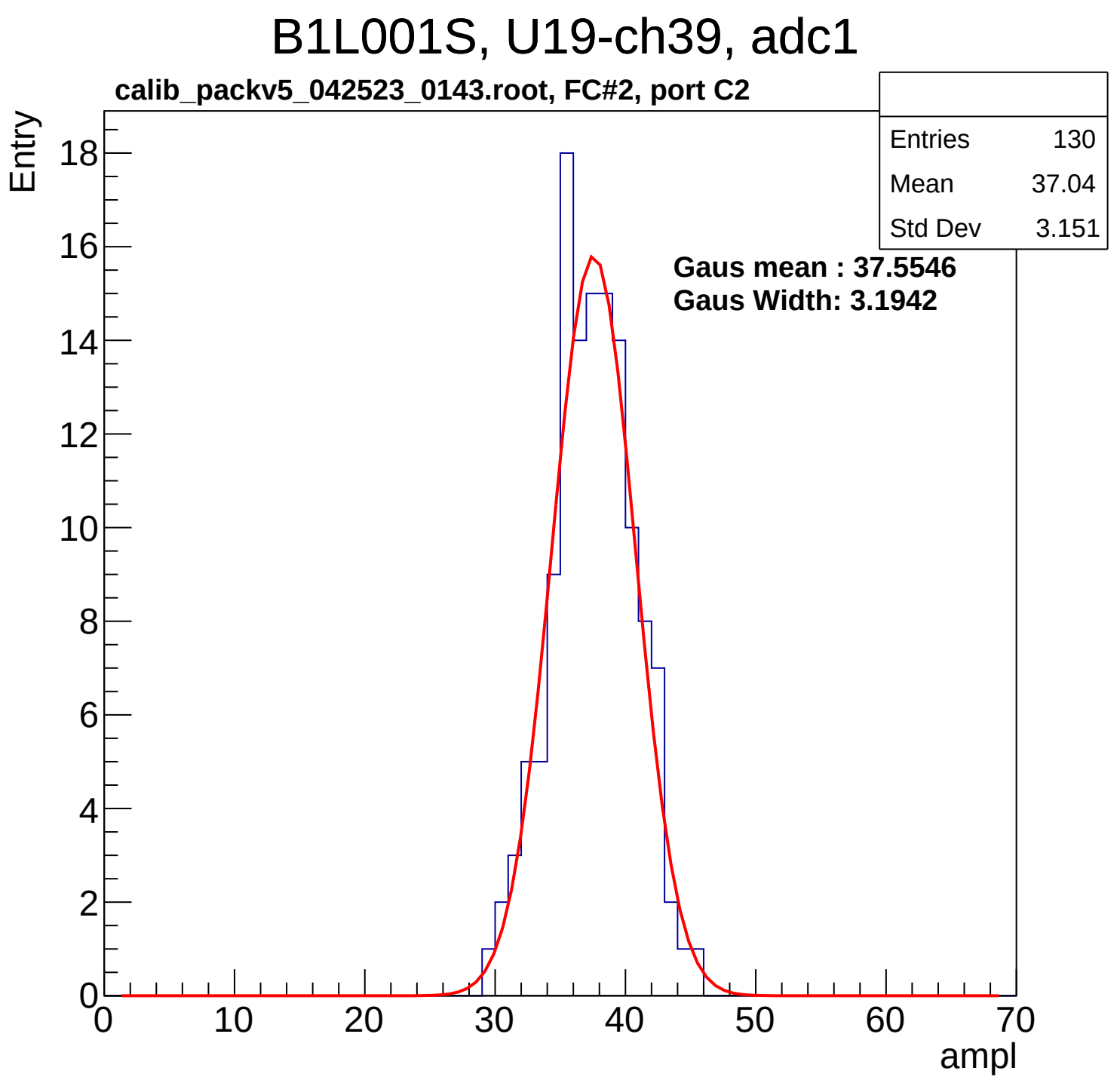
B1L001S, U19-ch39, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 130
Mean 37.04
Std Dev 3.151
Gaus mean : 37.5546
Gaus Width: 3.1942
Entry
ampl
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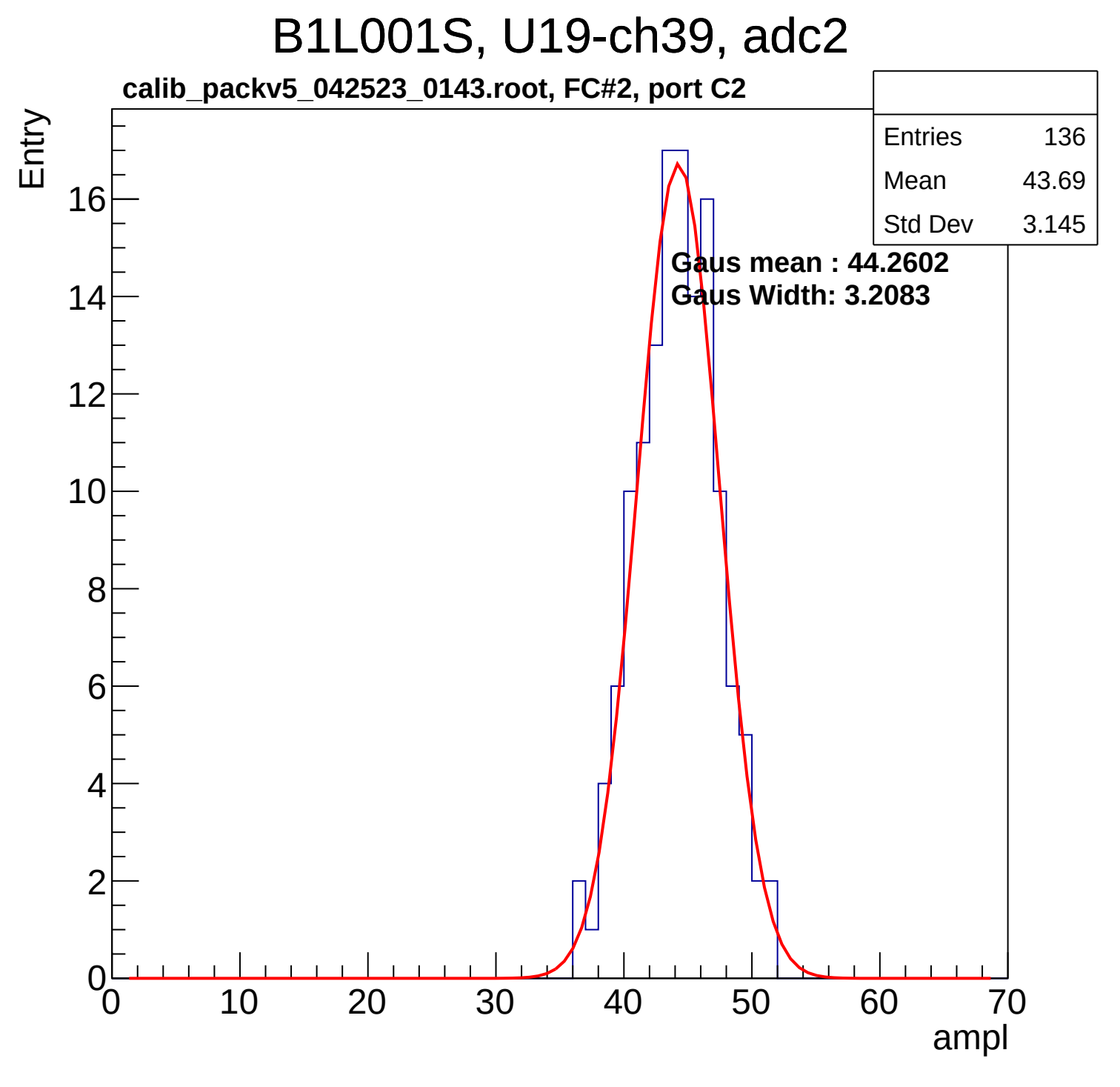
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70


B1L001S, U19-ch39, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 136
Mean 43.69
Std Dev 3.145
Gaus mean : 44.2602
Gaus Width: 3.2083
Entry
ampl
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2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
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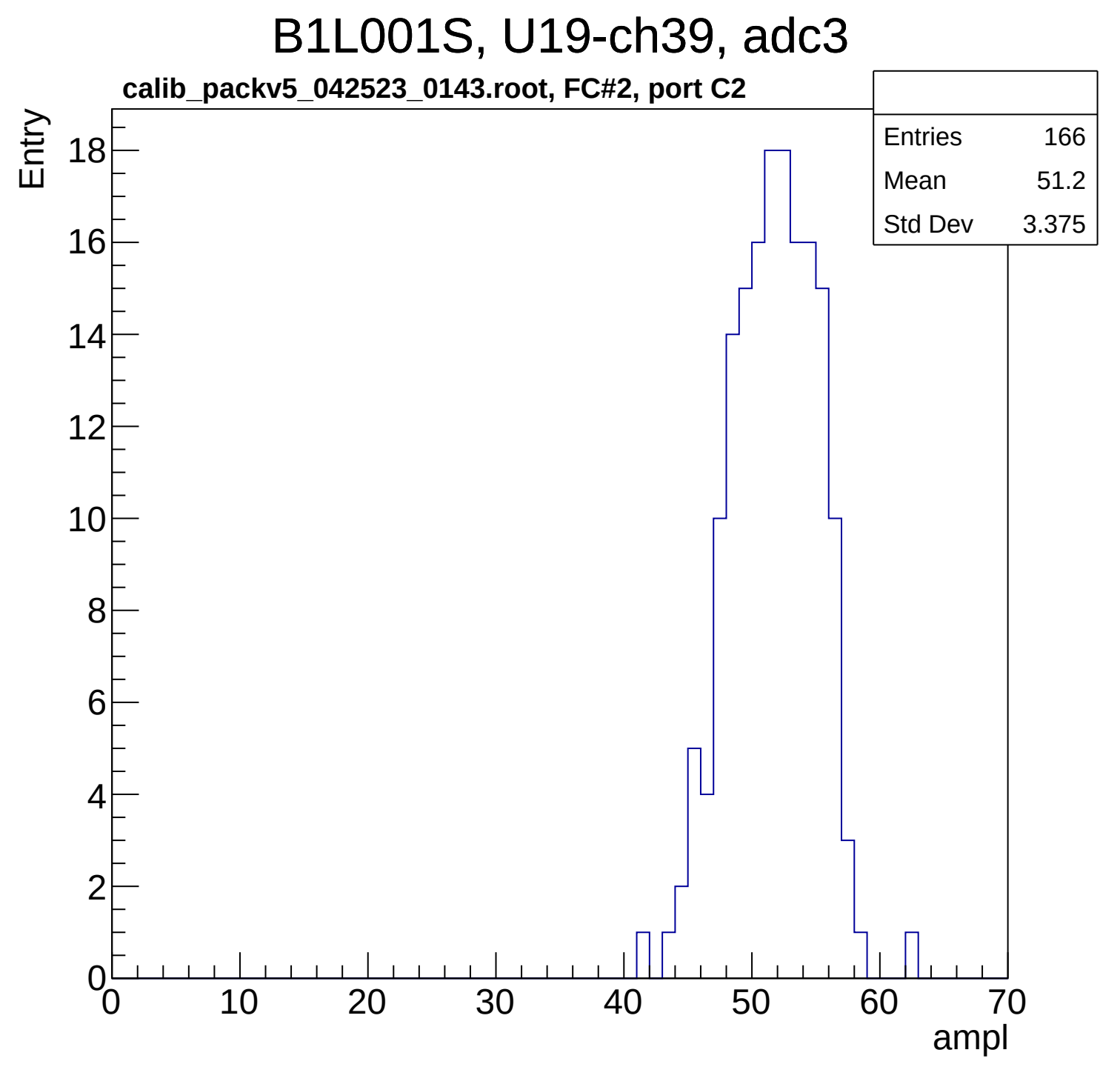
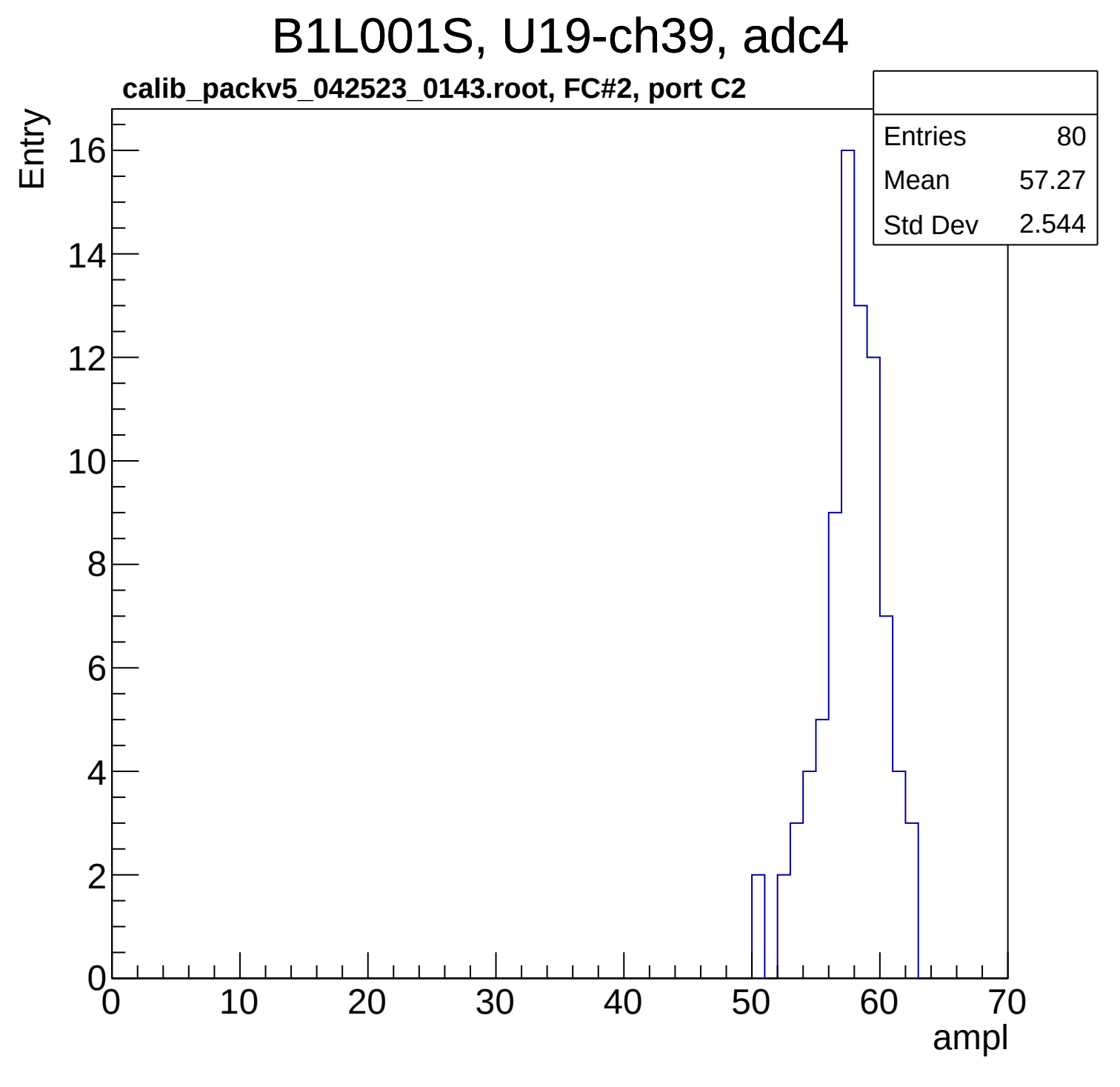

B1L001S, U19-ch39, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 166
Mean 51.2
Std Dev 3.375
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch39, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 80
Mean 57.27
Std Dev 2.544
Entry
ampl
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2
4
6
8
10
12
14
16
0
10
20
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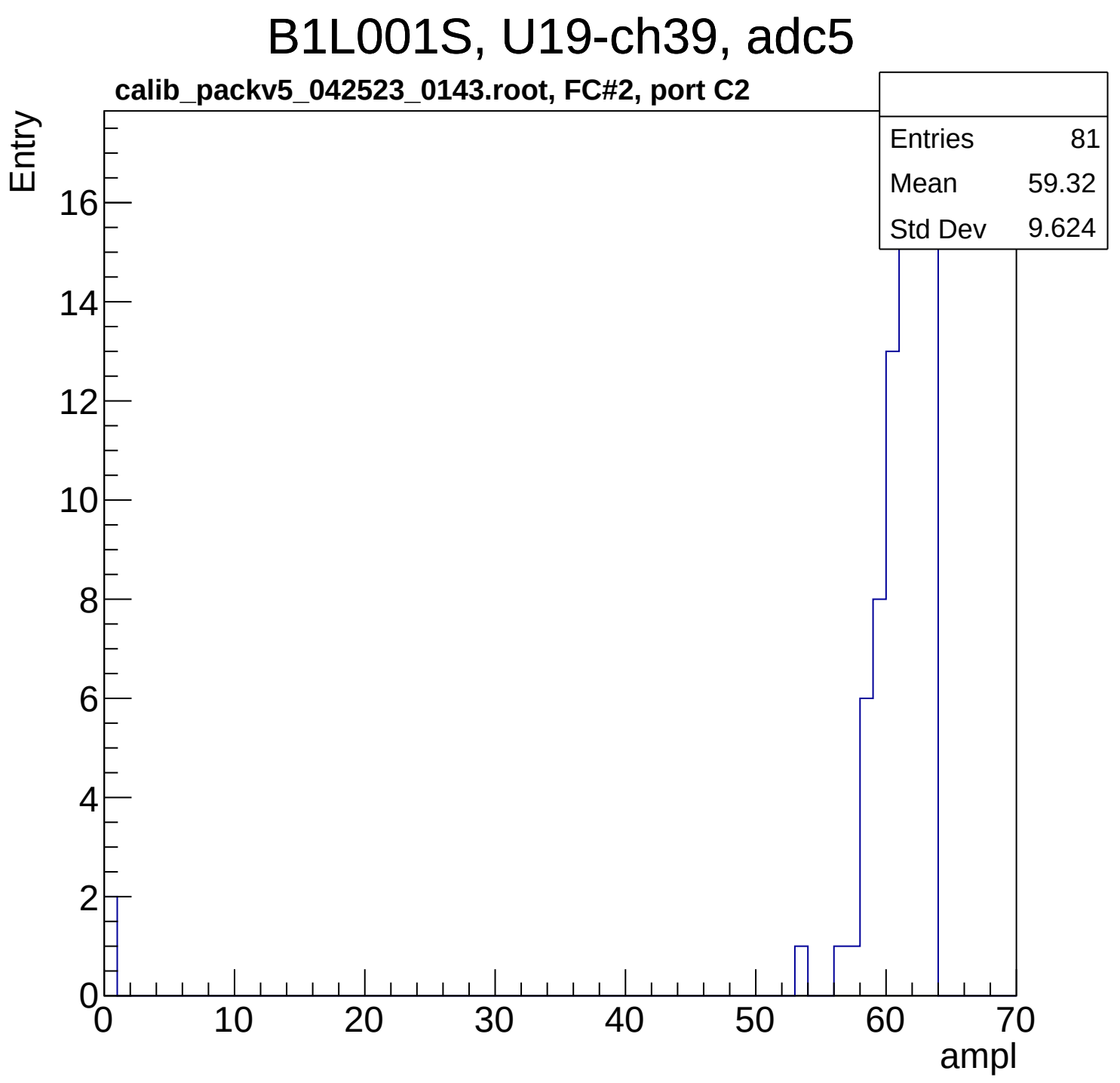
40
50
60
70


B1L001S, U19-ch39, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 81
Mean 59.32
Std Dev 9.624
Entry
0
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4
6
8
10
12
14
16
0
10
20
30
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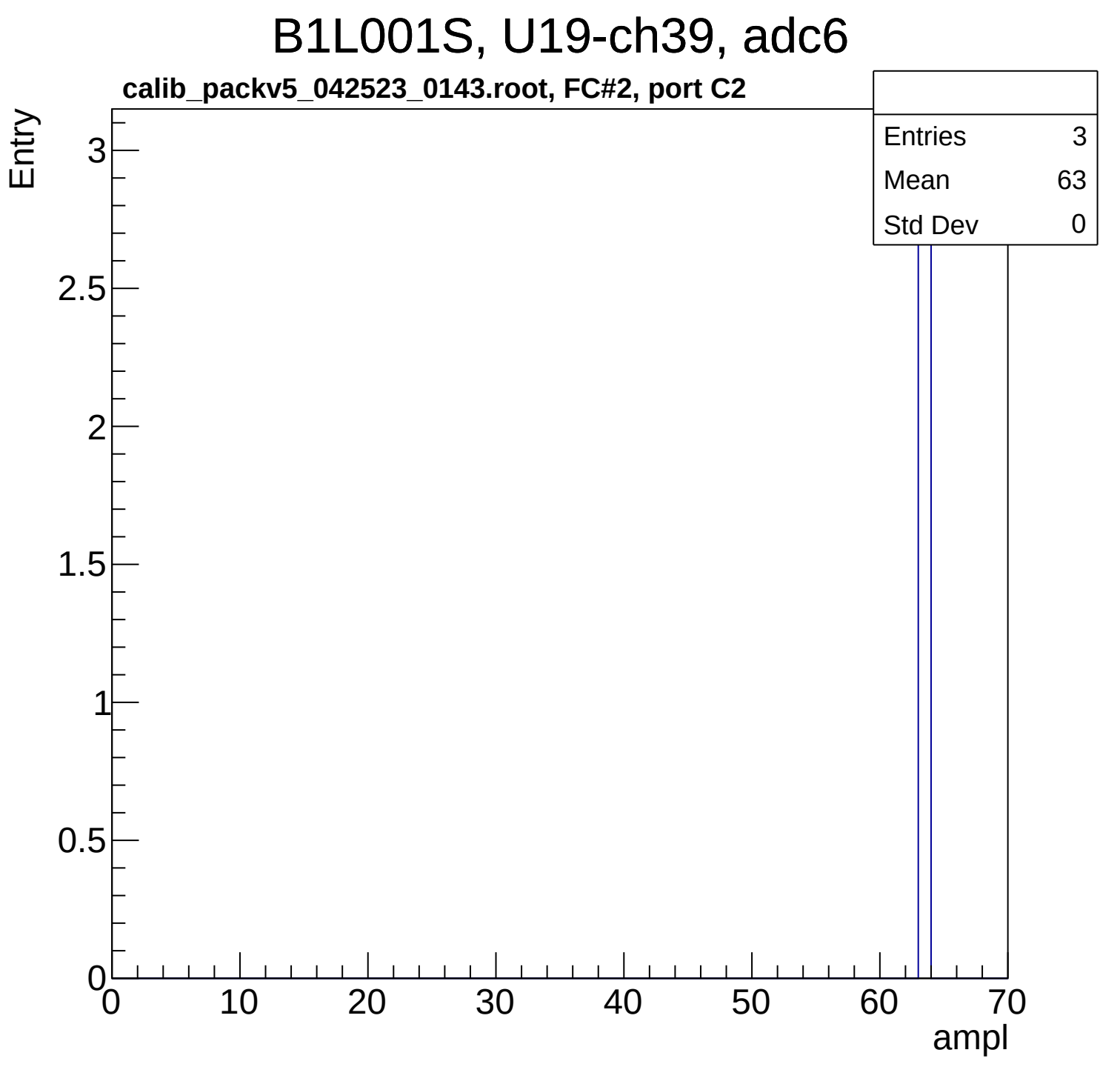
50
60
70
ampl


B1L001S, U19-ch39, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 3
Mean 63
Std Dev 0
Entry
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0.5
1
1.5
2
2.5
3
0
10
20
30
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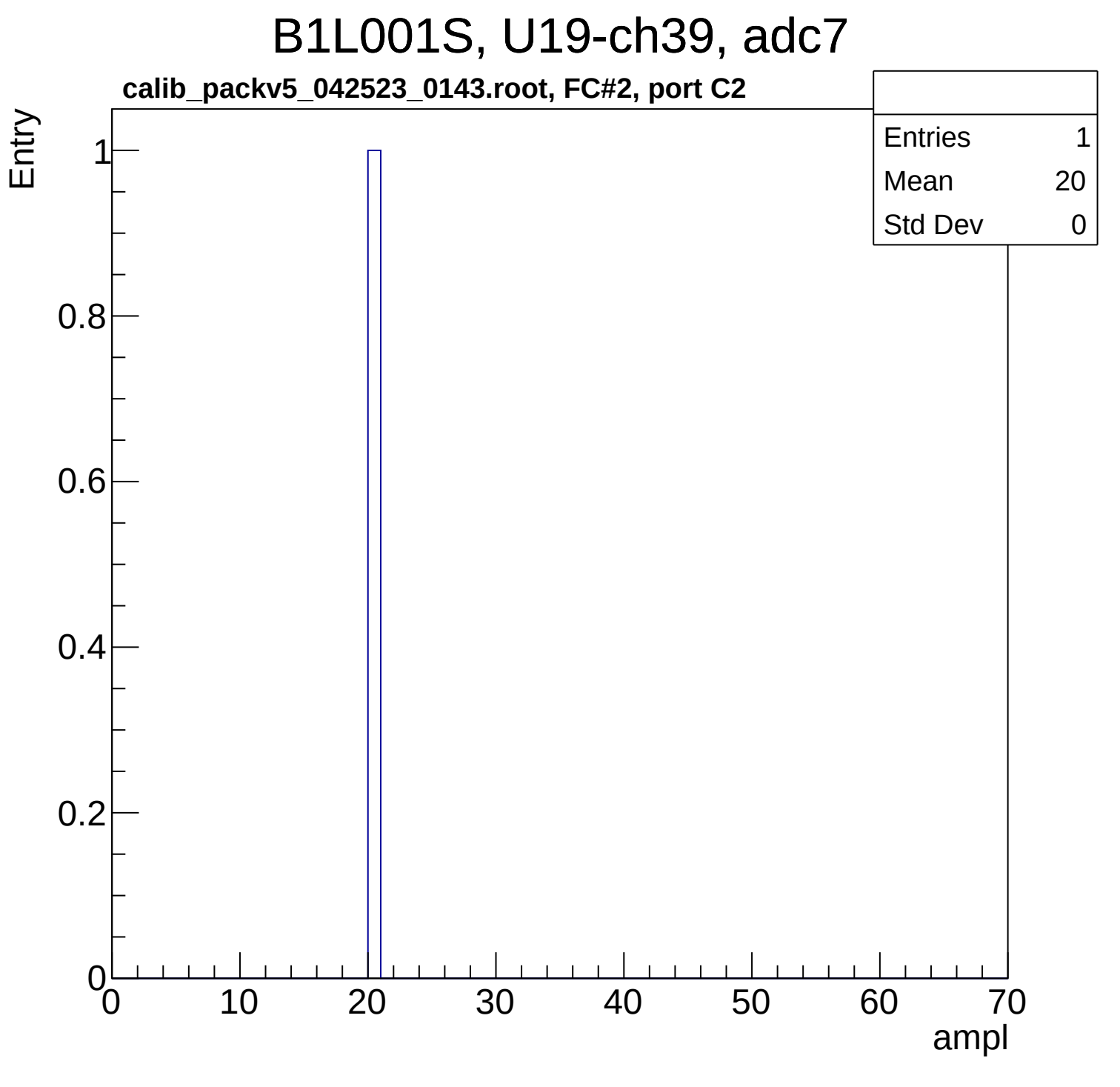
50
60
70
ampl


B1L001S, U19-ch39, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 20
Std Dev 0
Entry
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0.6
0.4
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10
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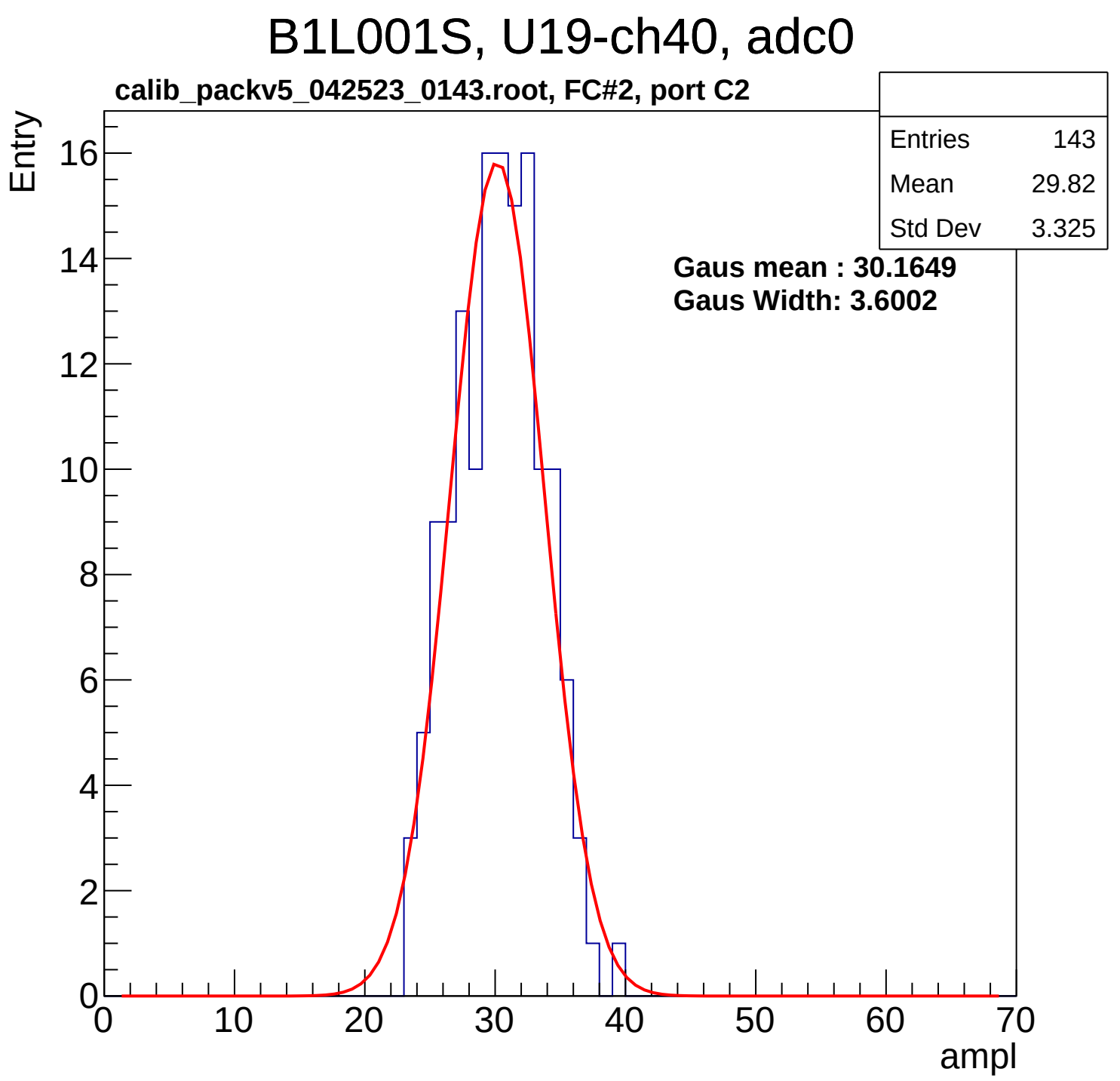
50
60
70
ampl


B1L001S, U19-ch40, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 143
Mean 29.82
Std Dev 3.325
Gaus mean : 30.1649
Gaus Width: 3.6002
Entry
ampl
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2
4
6
8
10
12
14
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0
10
20
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40
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60
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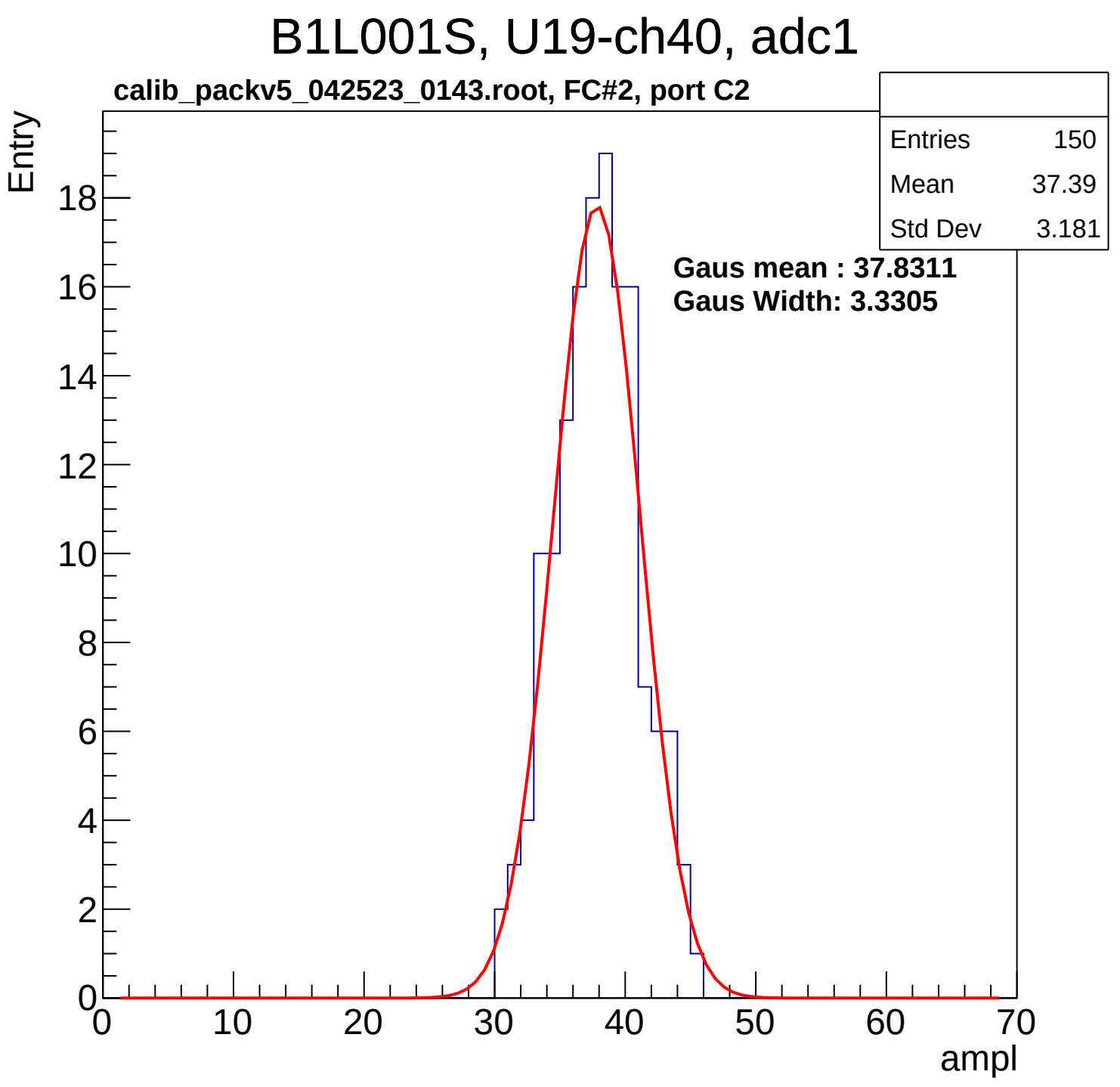
B1L001S, U19-ch40, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 150
Mean 37.39
Std Dev 3.181
Gaus mean : 37.8311
Gaus Width: 3.3305
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
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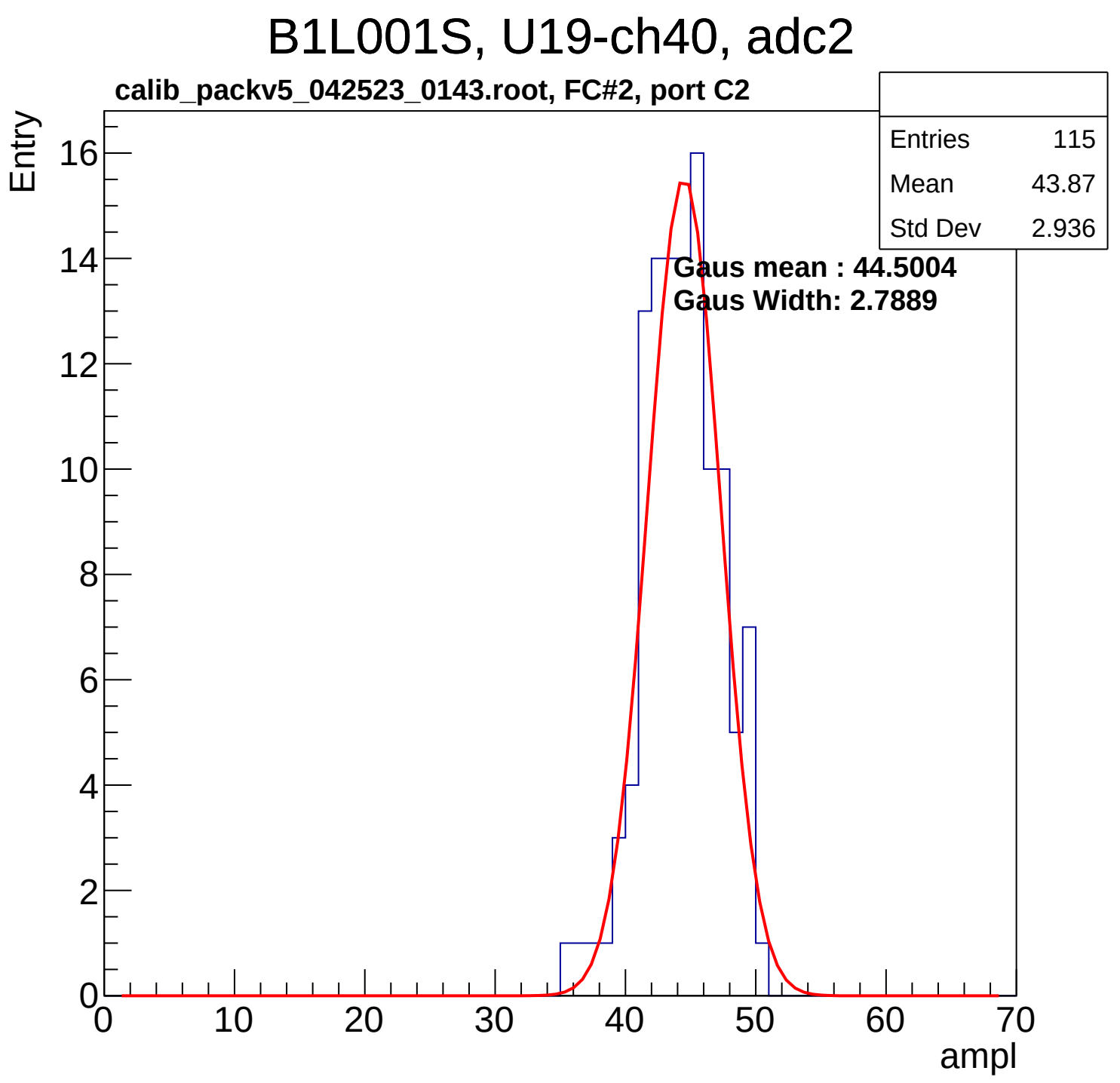
B1L001S, U19-ch40, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 115
Mean 43.87
Std Dev 2.936
Gaus mean : 44.5004
Gaus Width: 2.7889
Entry
ampl
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2
4
6
8
10
12
14
16
0
10
20
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60
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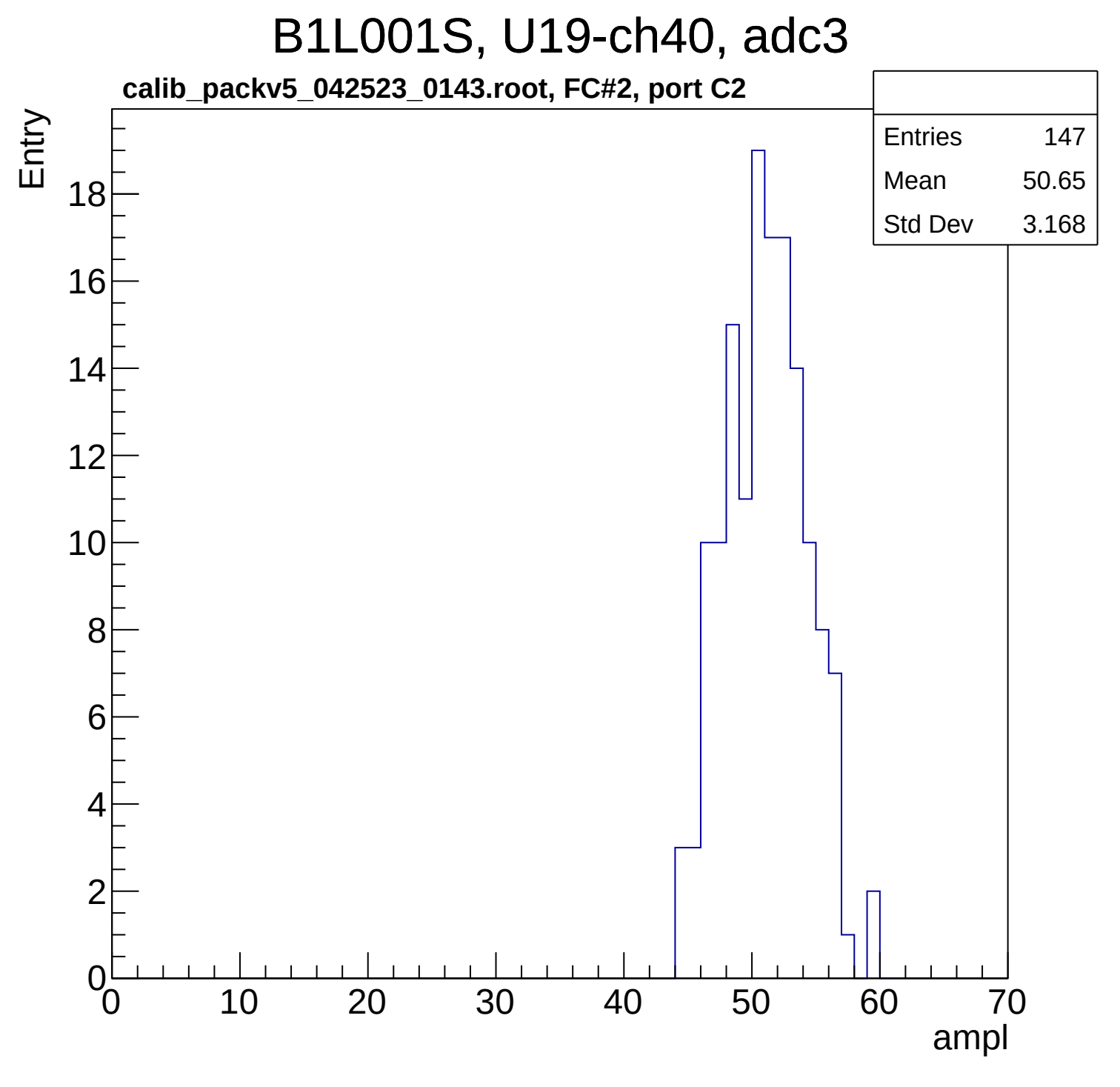
B1L001S, U19-ch40, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 147
Mean 50.65
Std Dev 3.168
Entry
ampl
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4
6
8
10
12
14
16
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0
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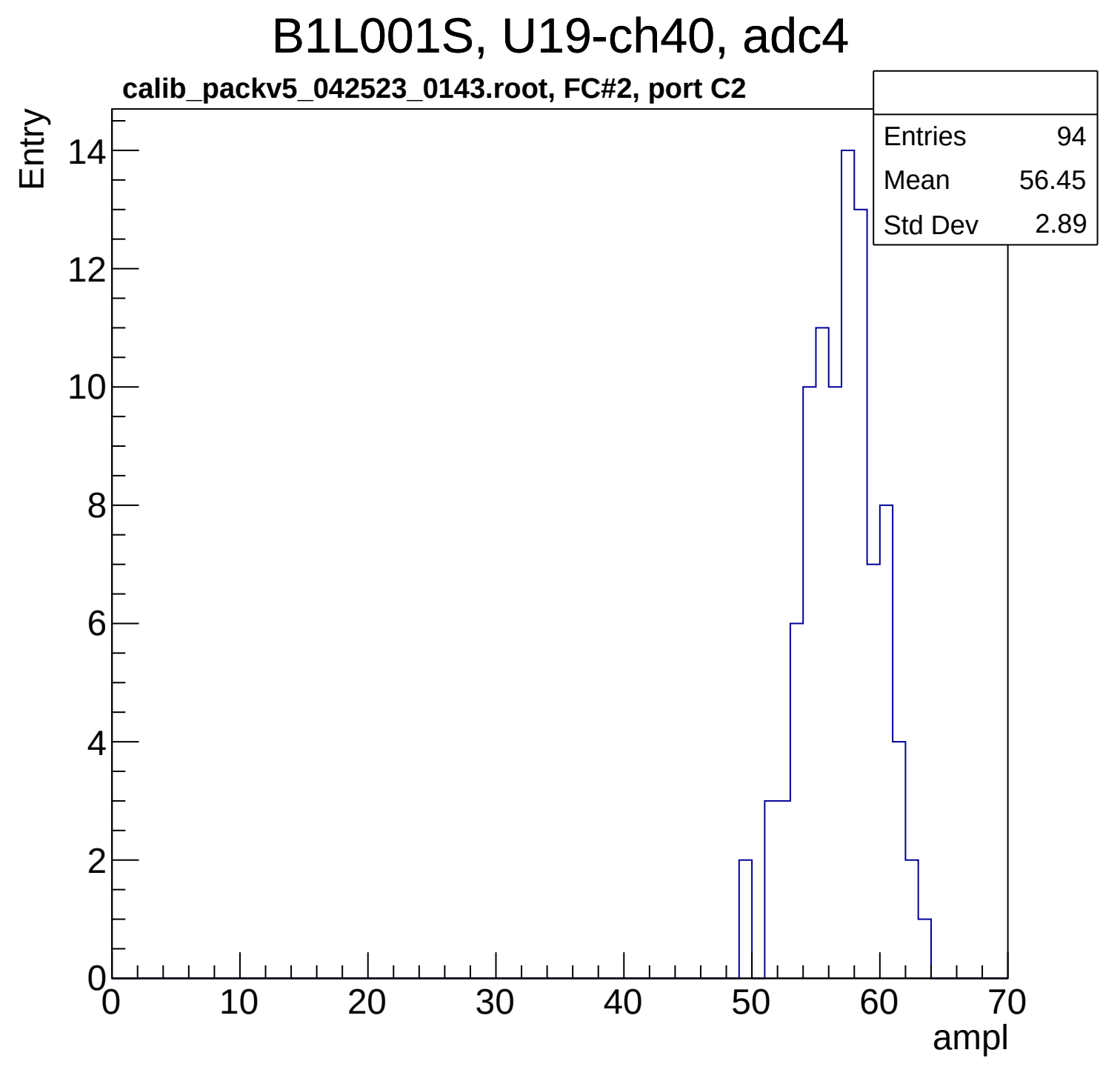
B1L001S, U19-ch40, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 94
Mean 56.45
Std Dev 2.89
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
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60
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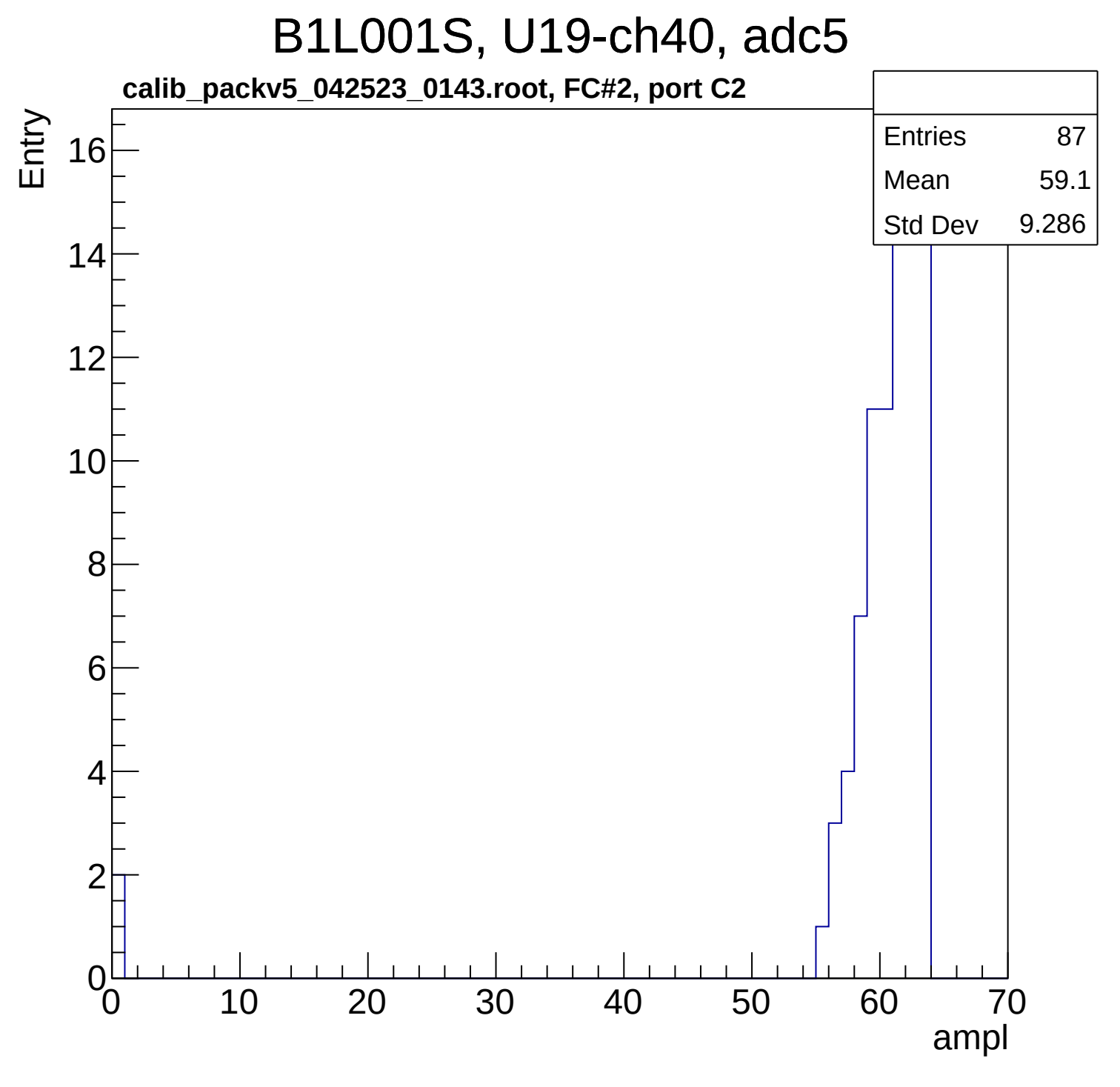
B1L001S, U19-ch40, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 87
Mean 59.1
Std Dev 9.286
Entry
ampl
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2
4
6
8
10
12
14
16
0
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20
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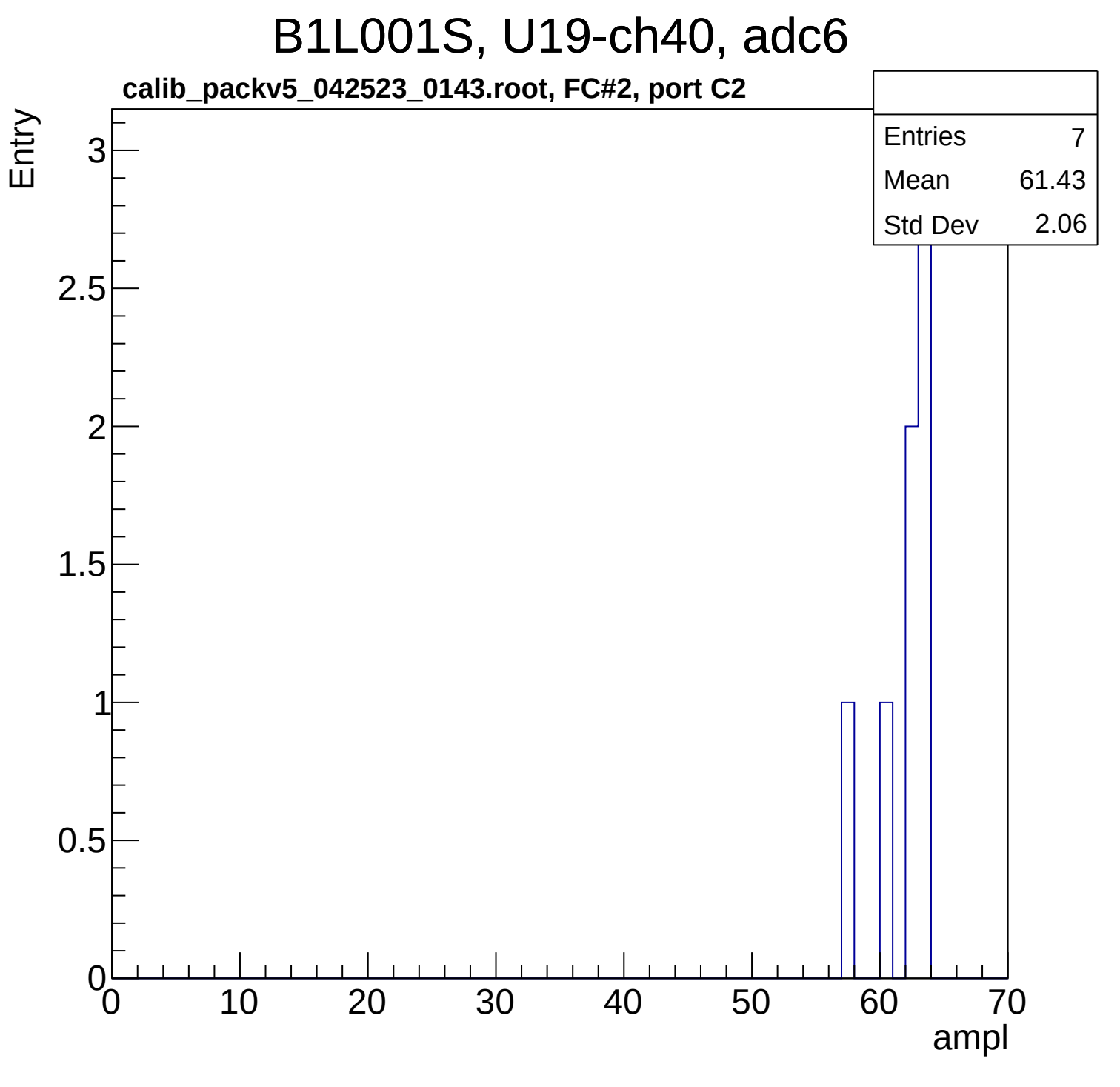
B1L001S, U19-ch40, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 7
Mean 61.43
Std Dev 2.06
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
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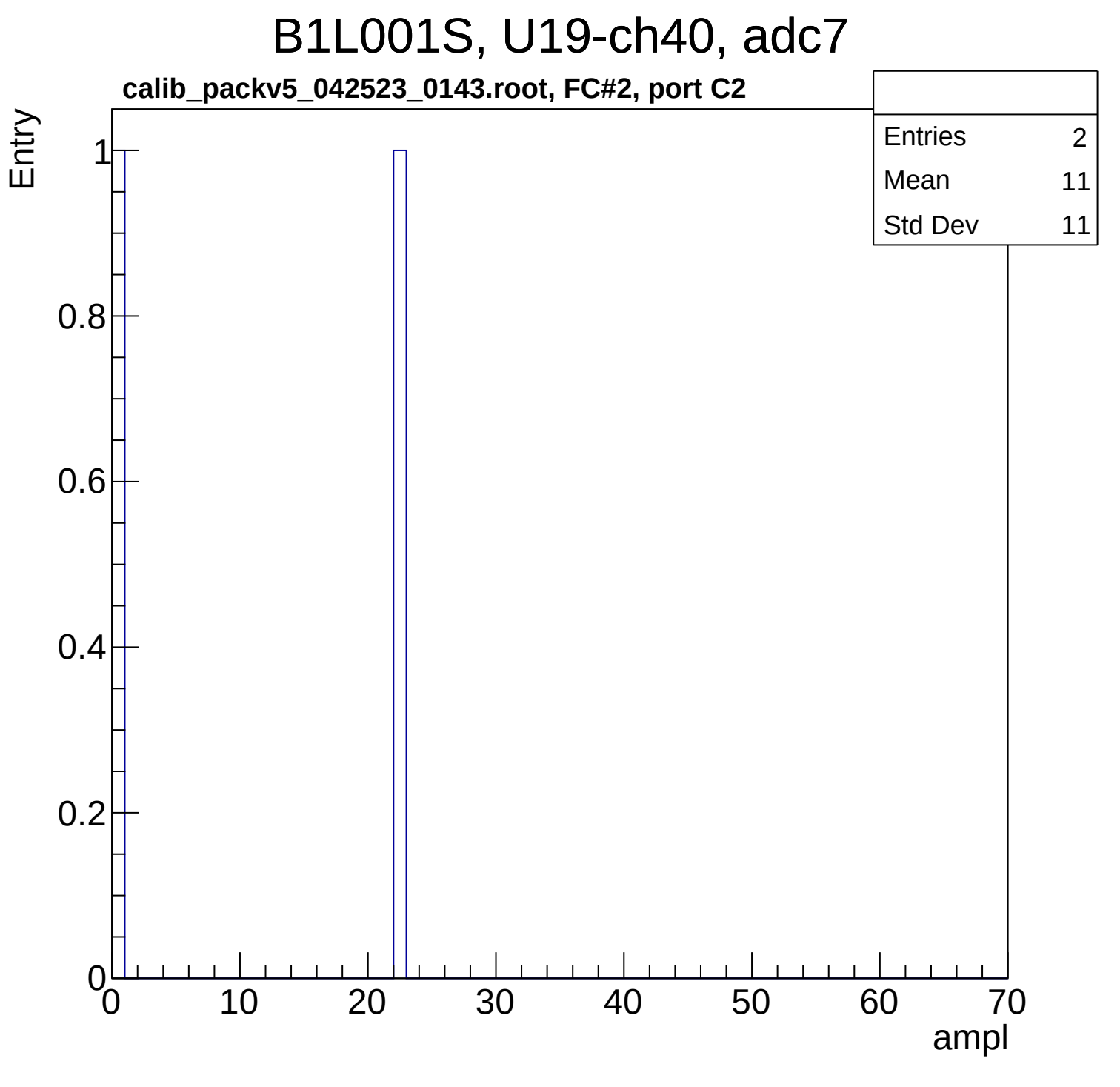
B1L001S, U19-ch40, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 11
Std Dev 11
Entry
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0.6
0.4
0.2
0
0
10
20
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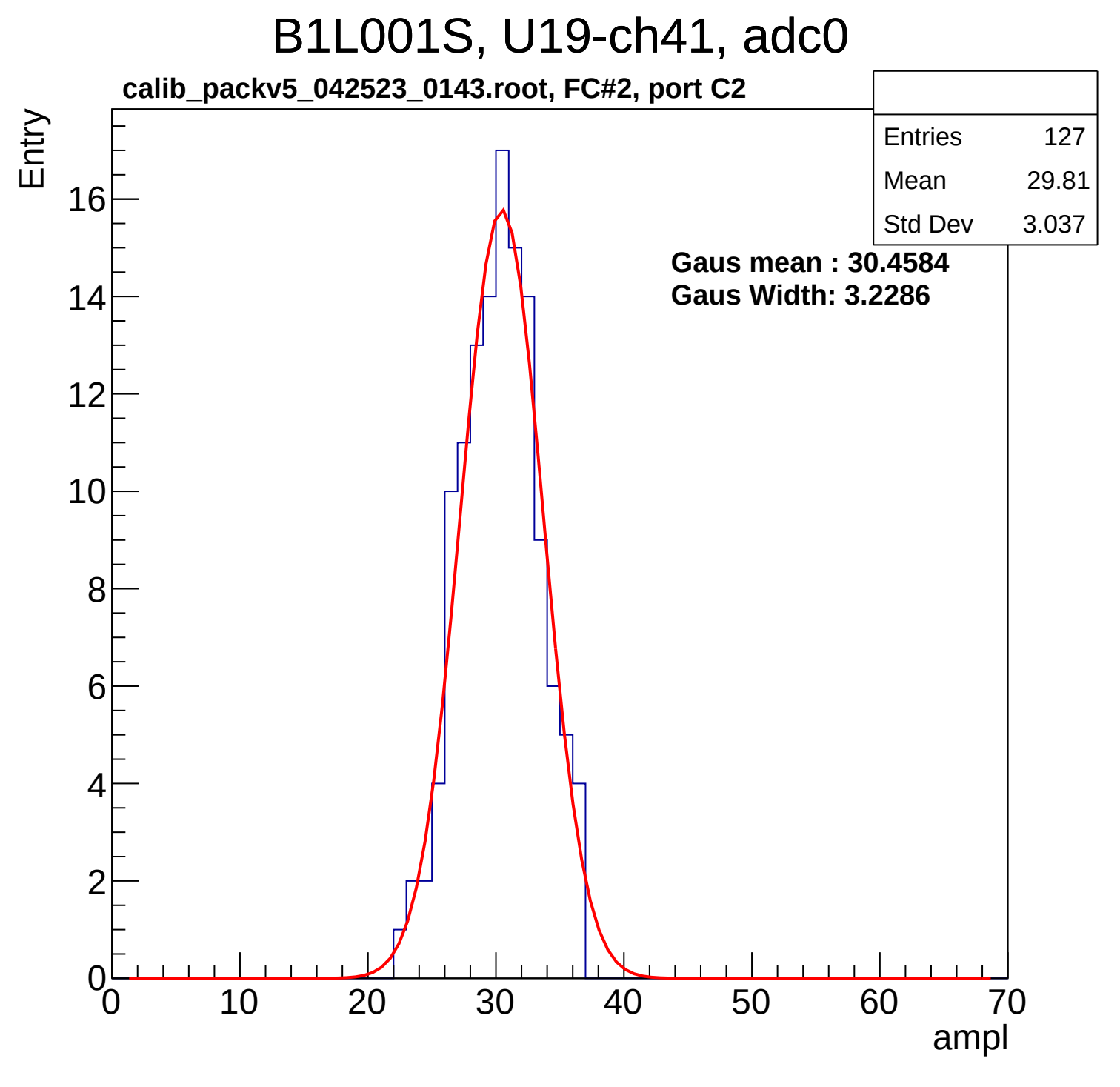
50
60
70
ampl


B1L001S, U19-ch41, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 127
Mean 29.81
Std Dev 3.037
Gaus mean : 30.4584
Gaus Width: 3.2286
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
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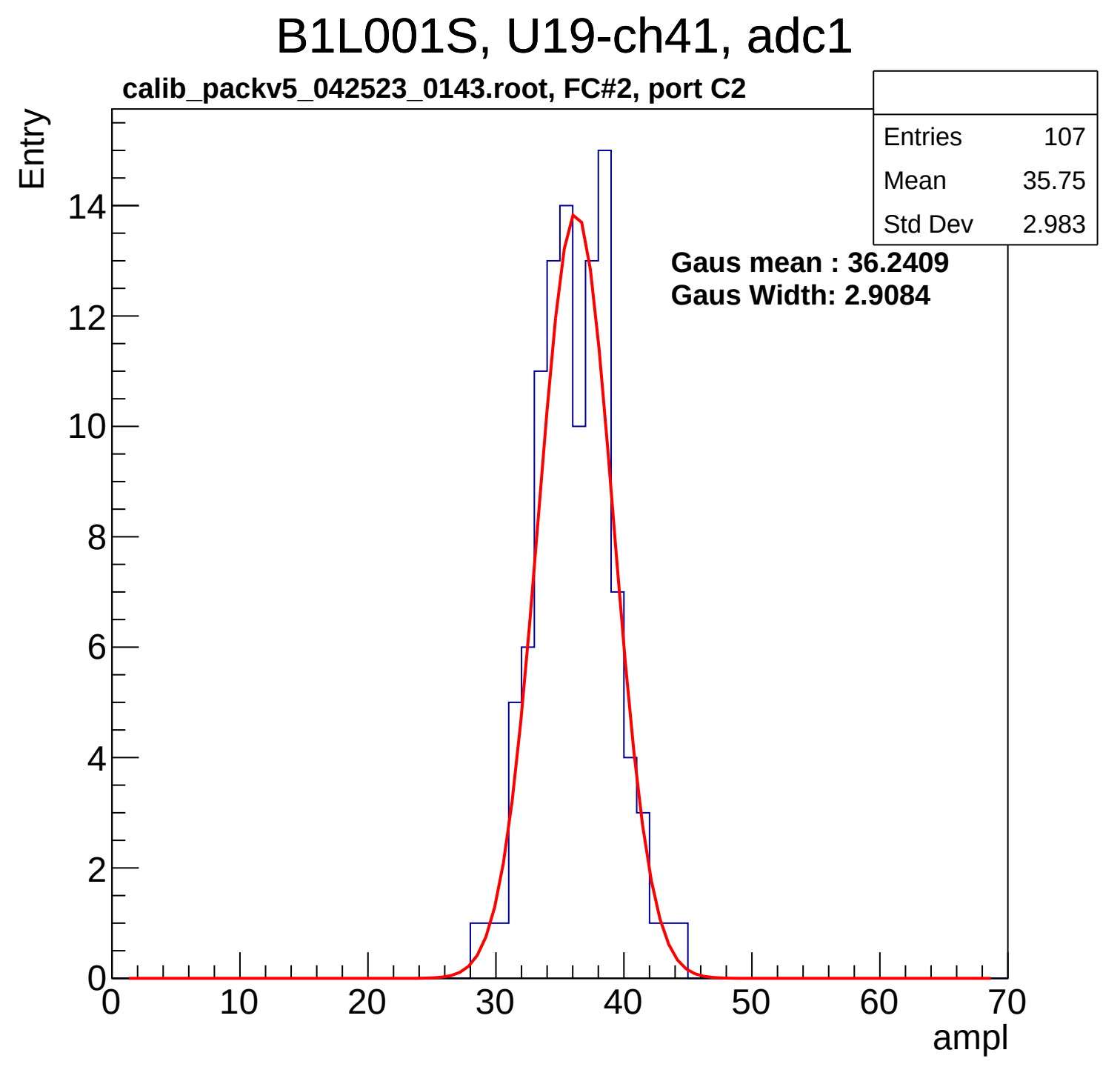
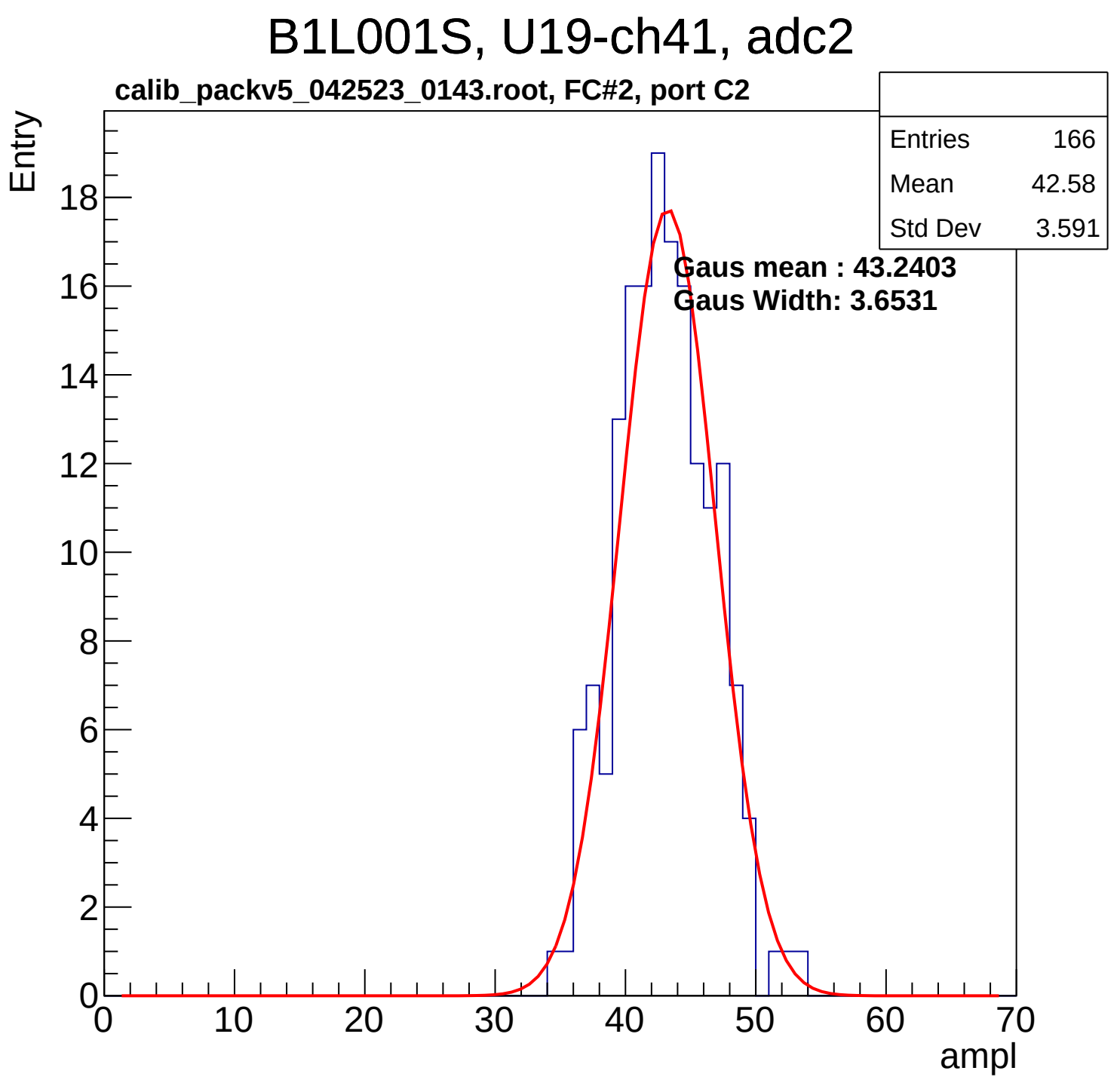

B1L001S, U19-ch41, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 107
Mean 35.75
Std Dev 2.983
Gaus mean : 36.2409
Gaus Width: 2.9084
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L001S, U19-ch41, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 166
Mean 42.58
Std Dev 3.591
Gaus mean : 43.2403
Gaus Width: 3.6531
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
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40
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60
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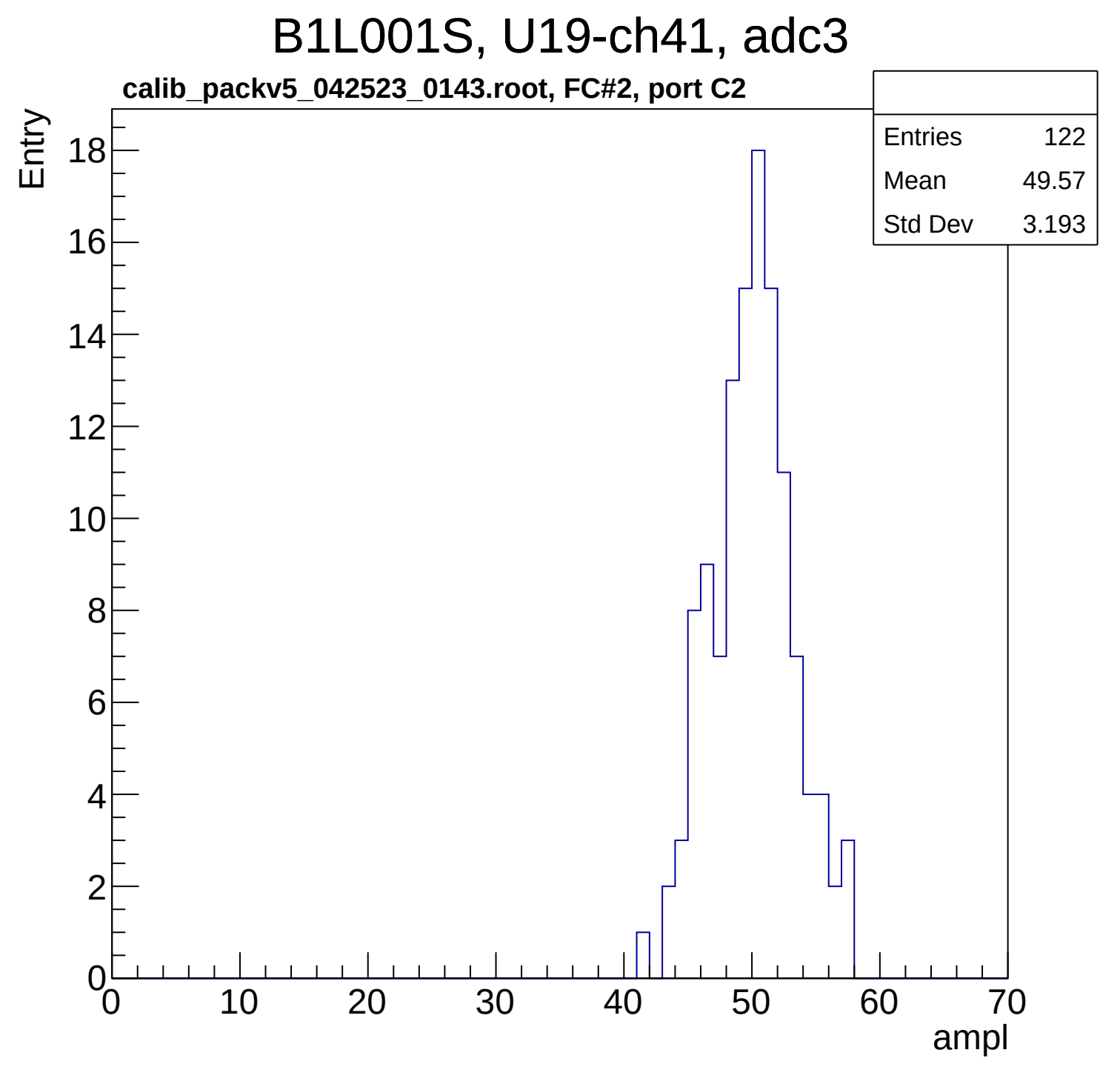
B1L001S, U19-ch41, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 122
Mean 49.57
Std Dev 3.193
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
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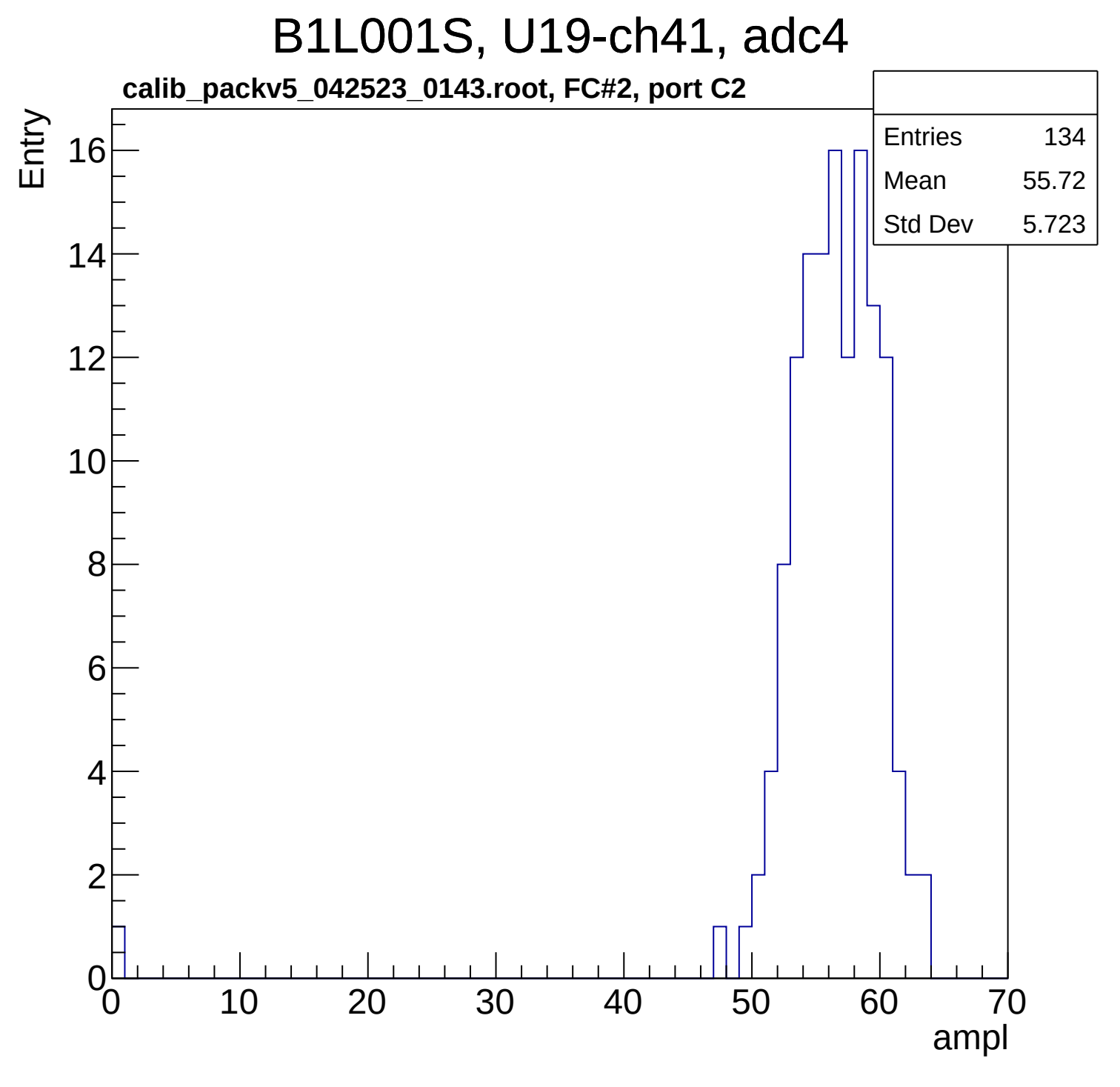
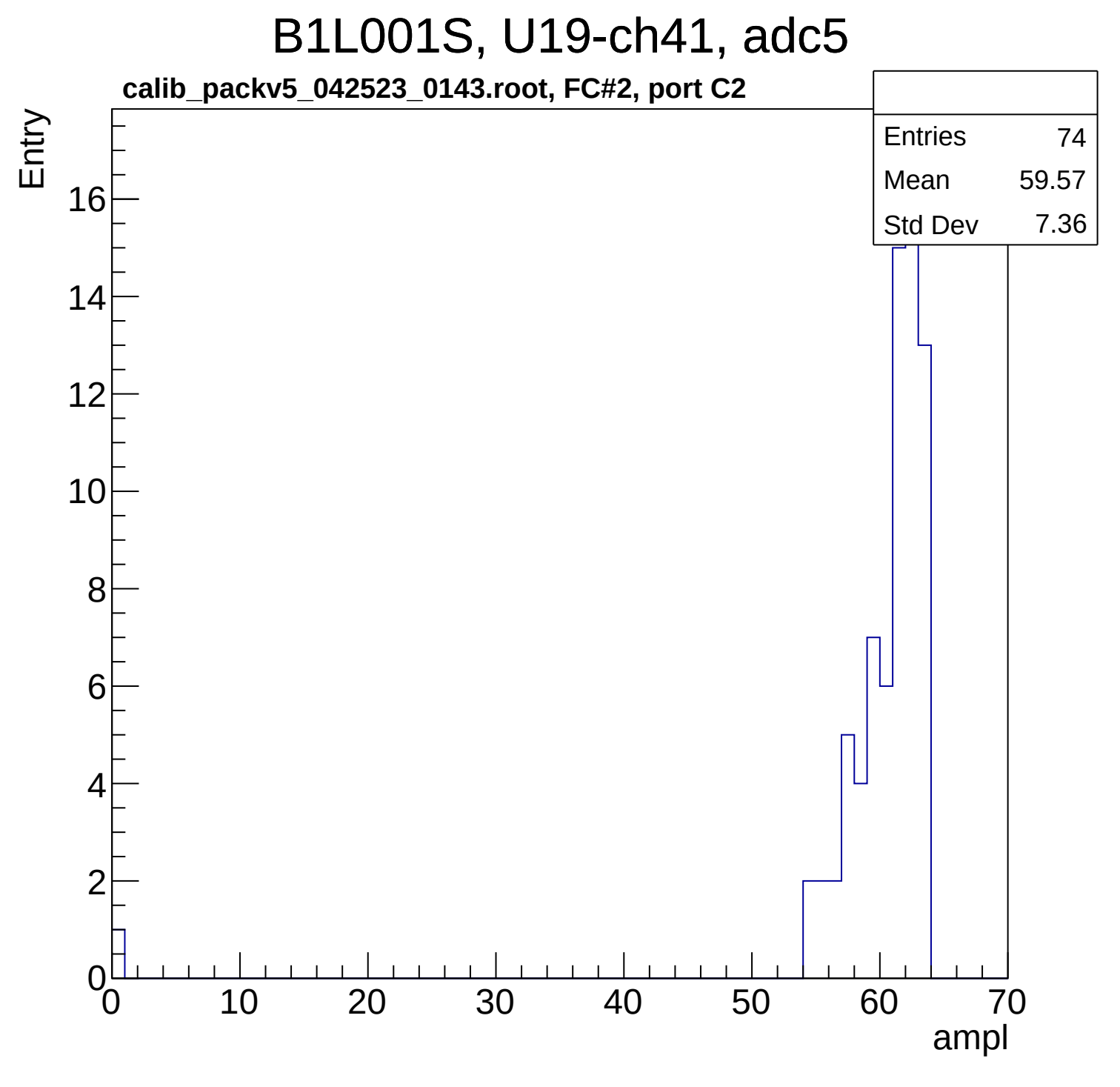
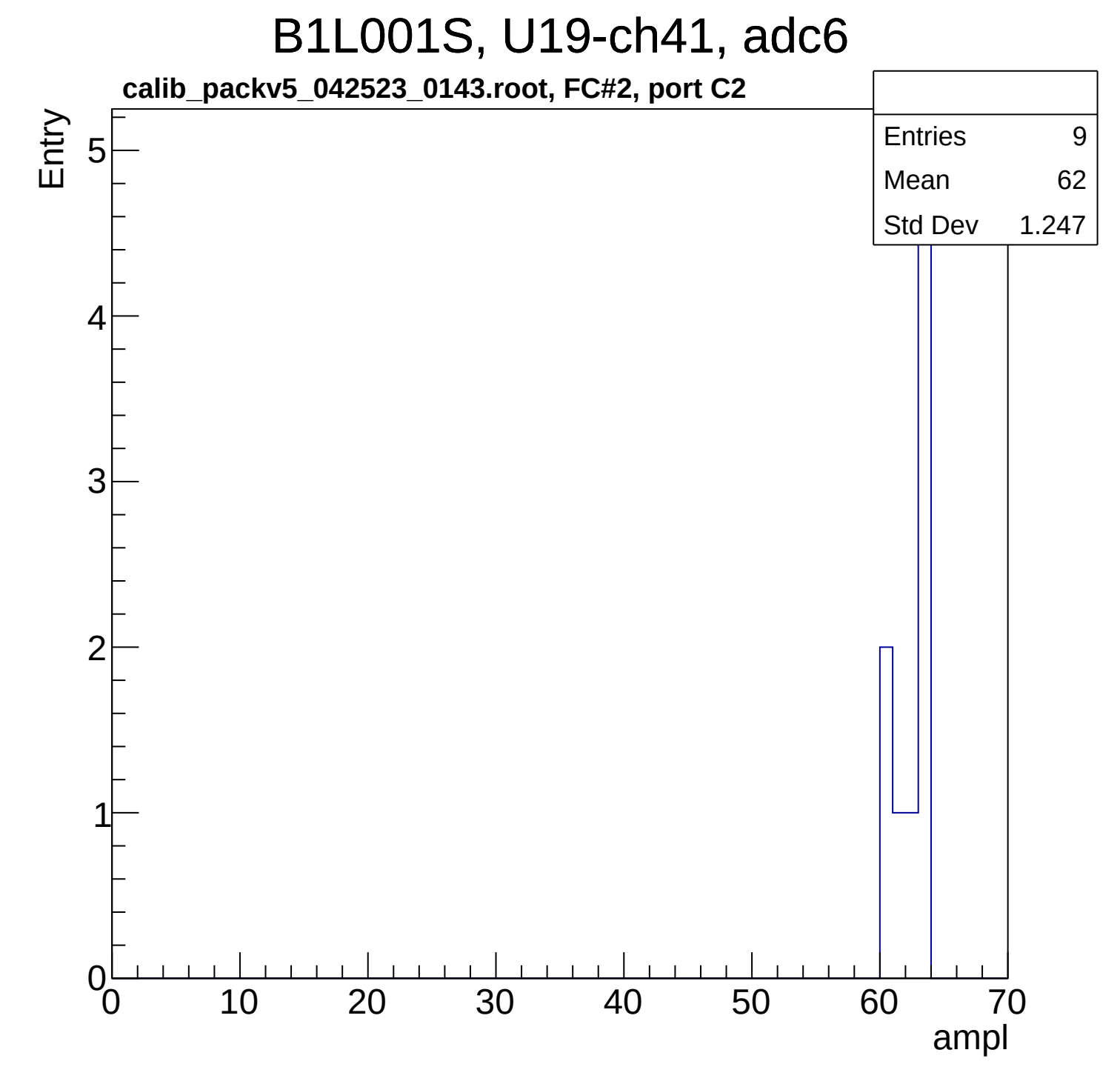
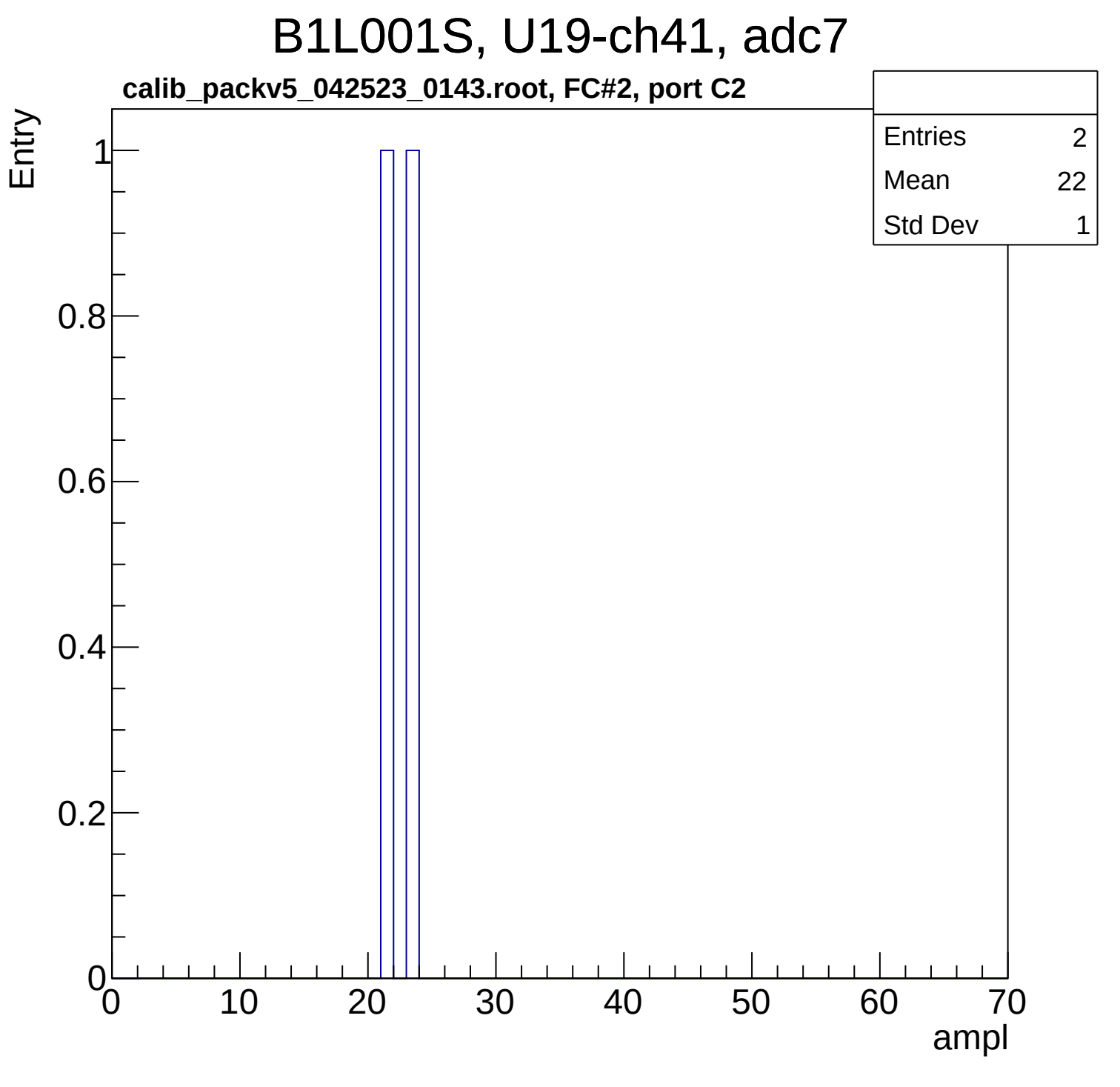
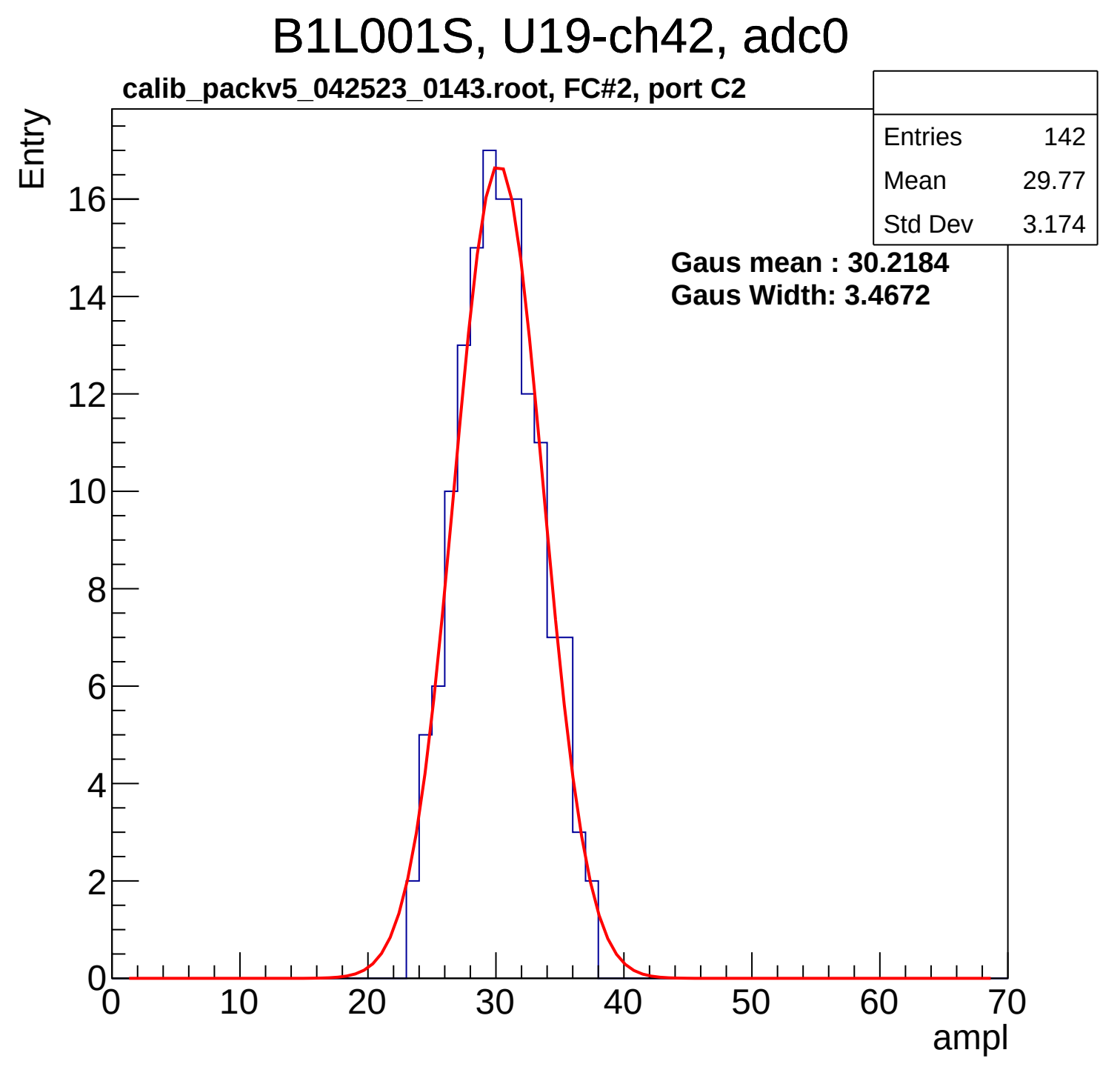
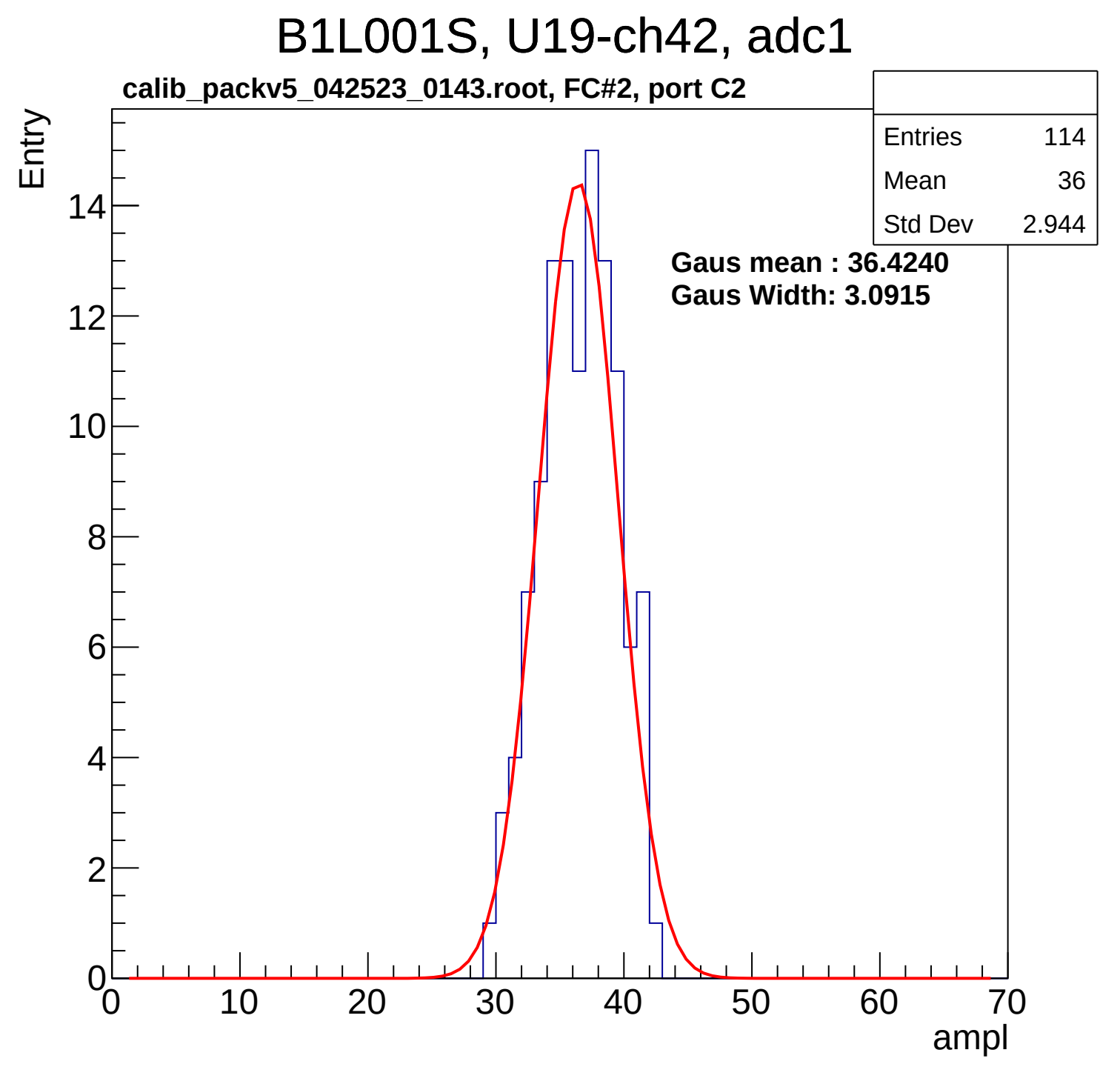

B1L001S, U19-ch41, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 134
Mean 55.72
Std Dev 5.723
Entry
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl

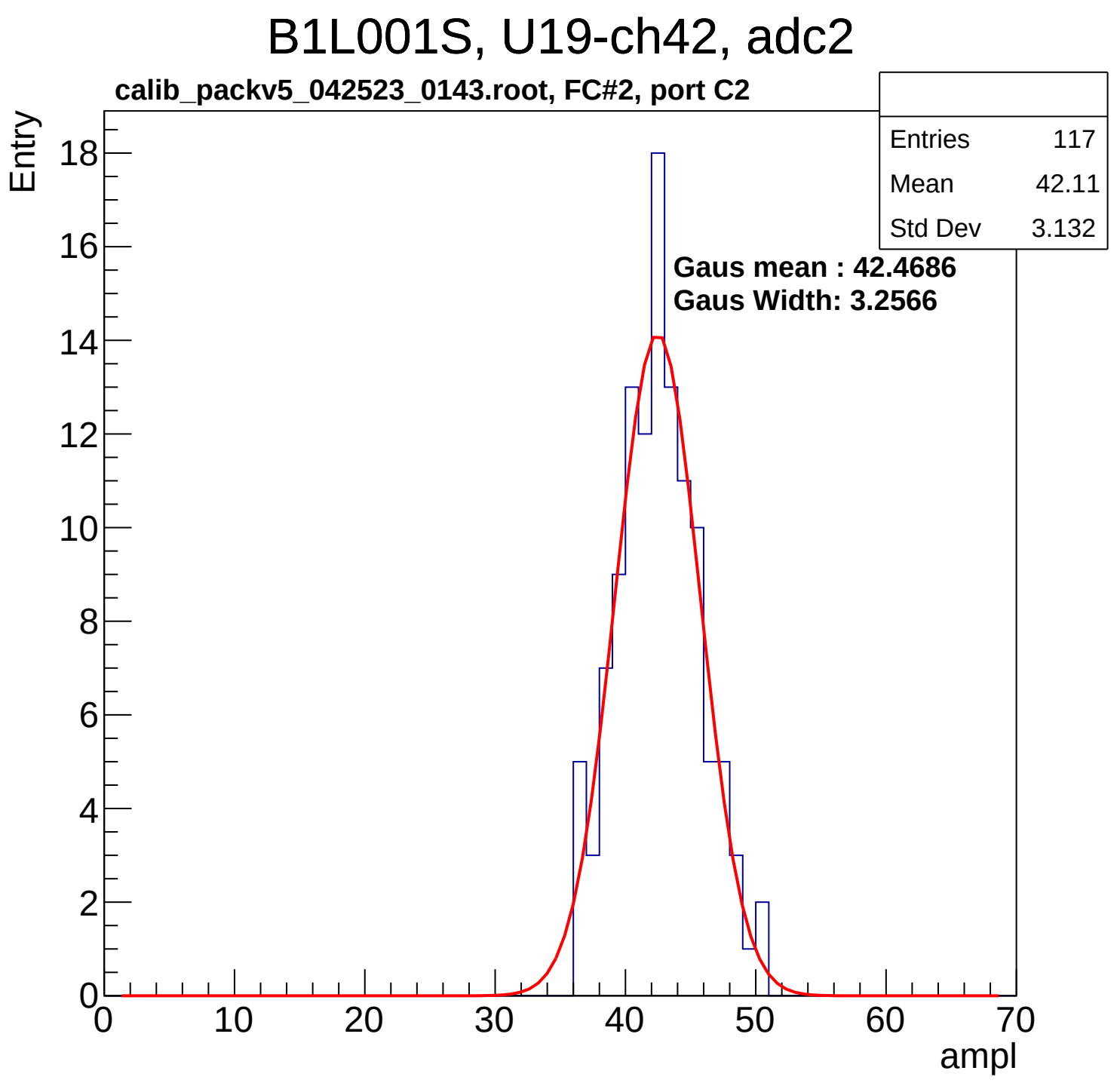

B1L001S, U19-ch41, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 74
Mean 59.57
Std Dev 7.36
Entry
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl

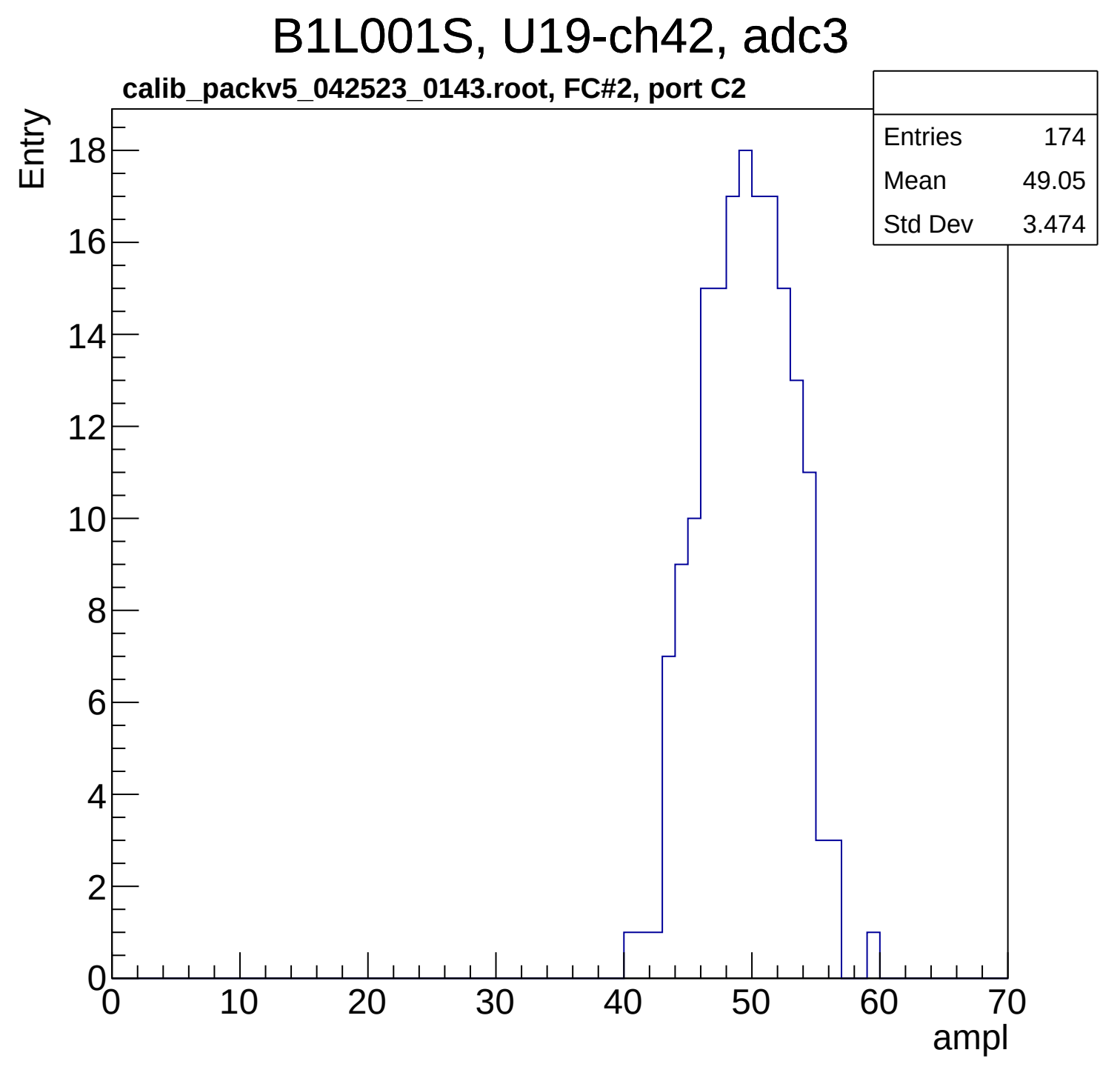

B1L001S, U19-ch41, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 9
Mean 62
Std Dev 1.247
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

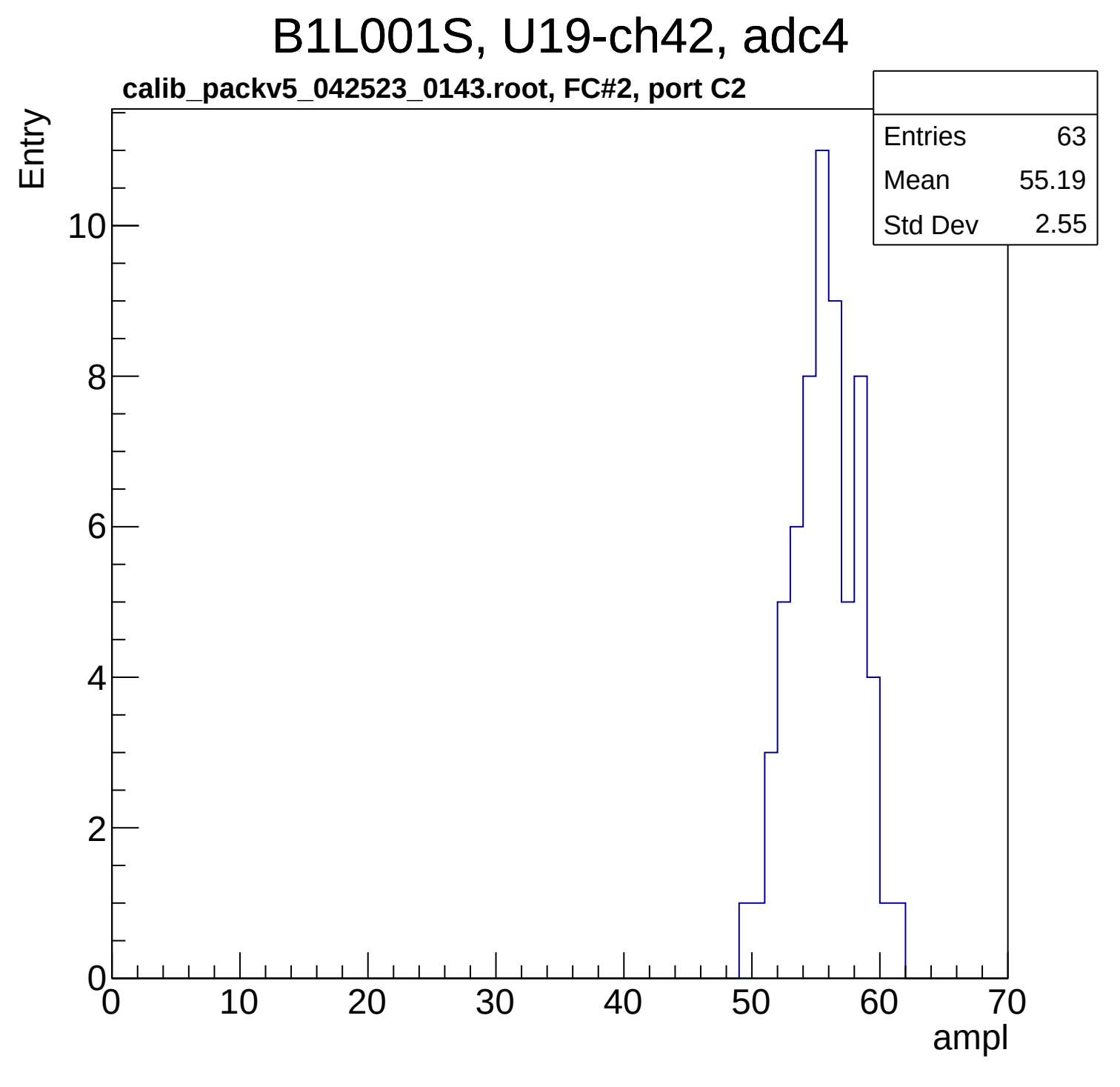

B1L001S, U19-ch41, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 22
Std Dev 1
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

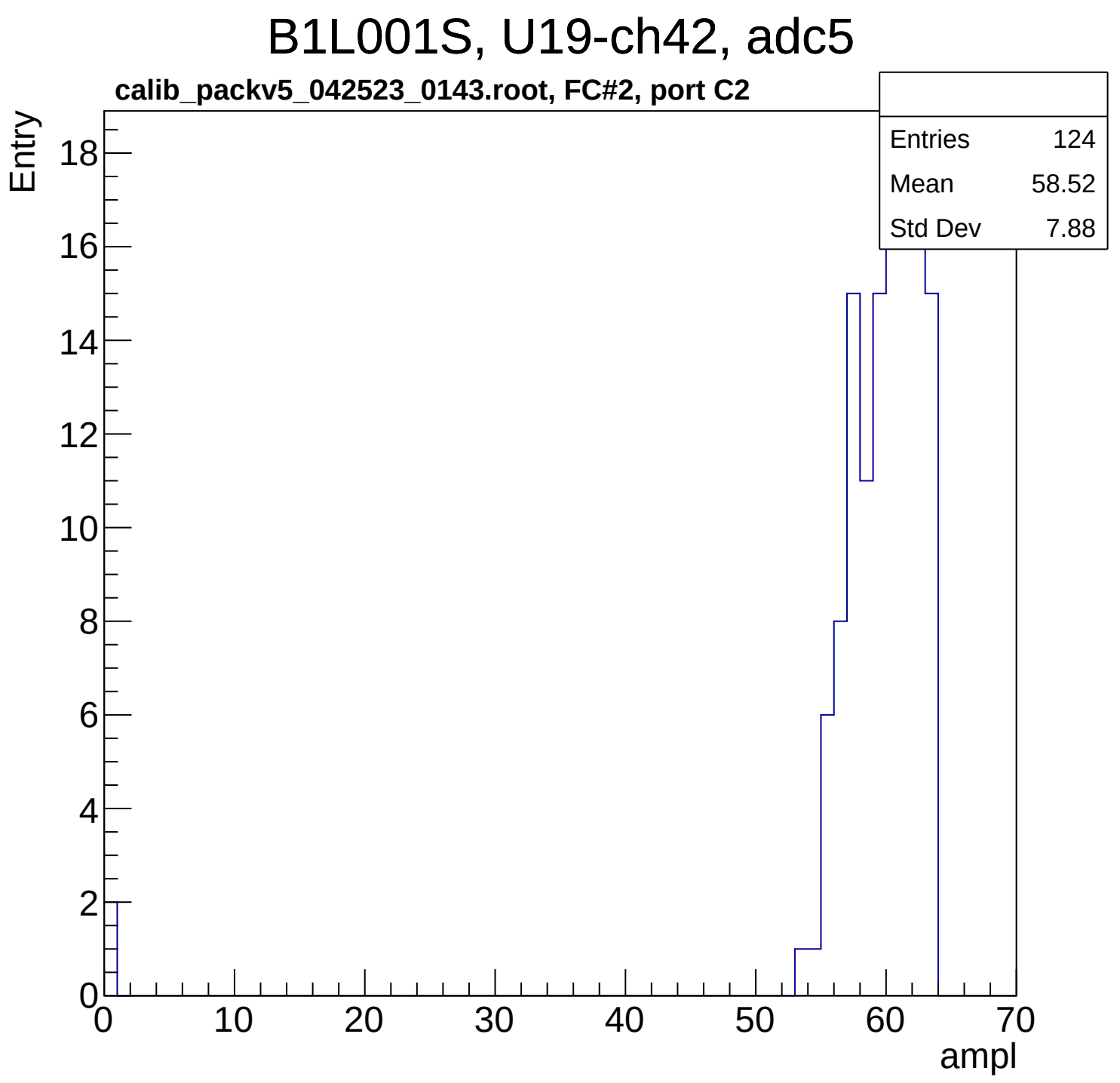

B1L001S, U19-ch42, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 142
Mean 29.77
Std Dev 3.174
Gaus mean : 30.2184
Gaus Width: 3.4672
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70


B1L001S, U19-ch42, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 114
Mean 36
Std Dev 2.944
Gaus mean : 36.4240
Gaus Width: 3.0915
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L001S, U19-ch42, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 117
Mean 42.11
Std Dev 3.132
Gaus mean : 42.4686
Gaus Width: 3.2566
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70


B1L001S, U19-ch42, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 174
Mean 49.05
Std Dev 3.474
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70


B1L001S, U19-ch42, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 63
Mean 55.19
Std Dev 2.55
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch42, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 124
Mean 58.52
Std Dev 7.88
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
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60
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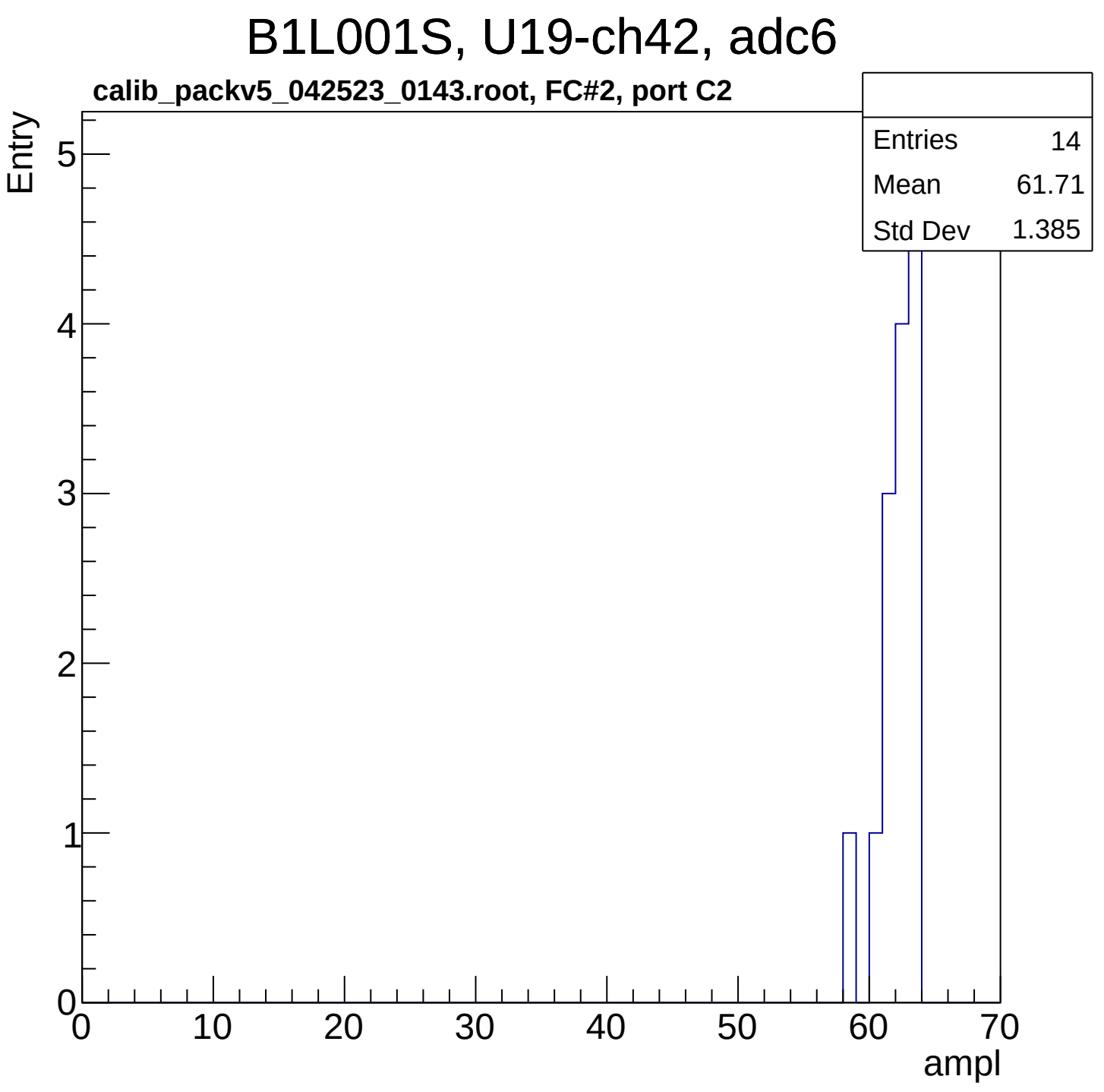
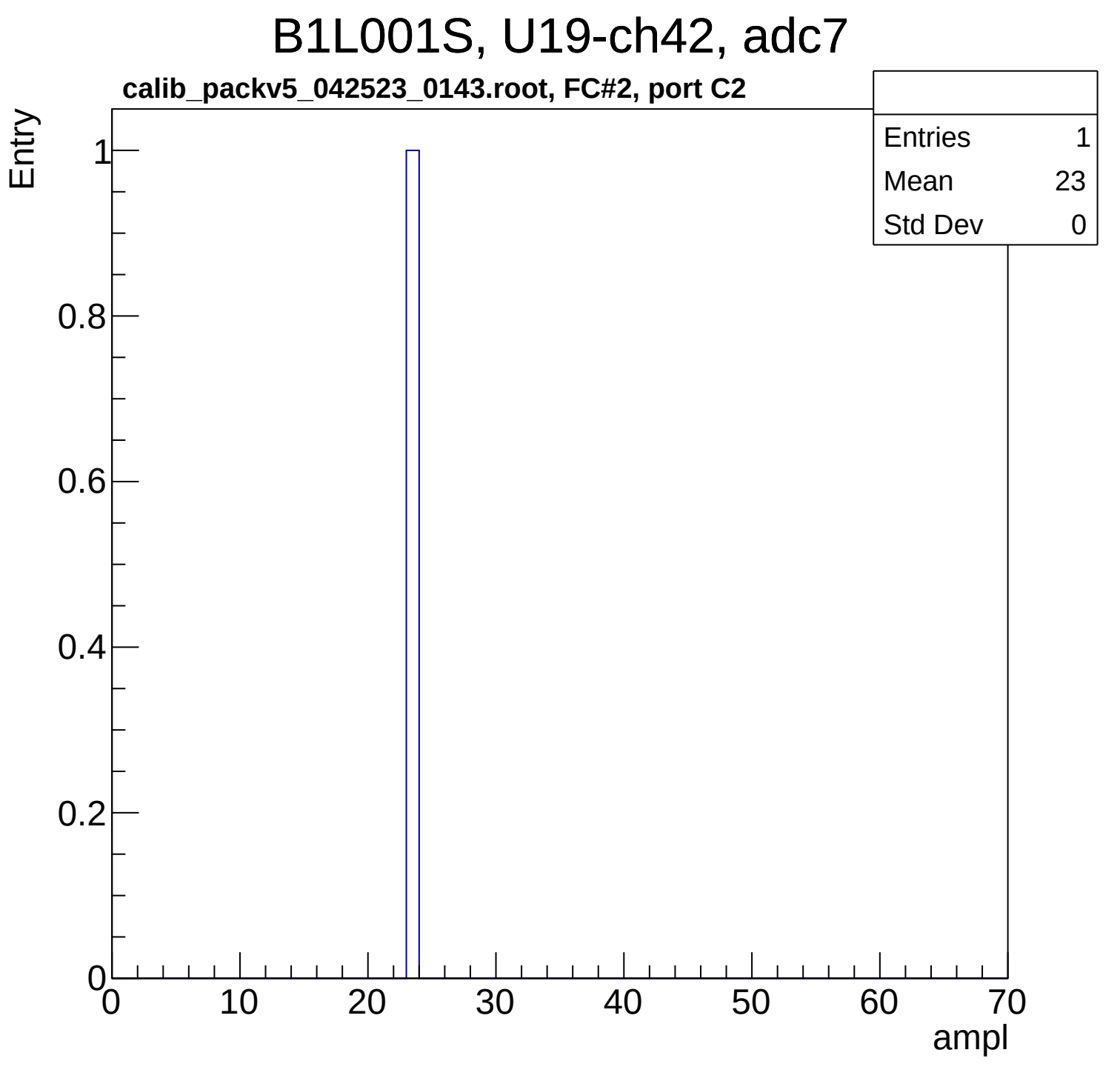
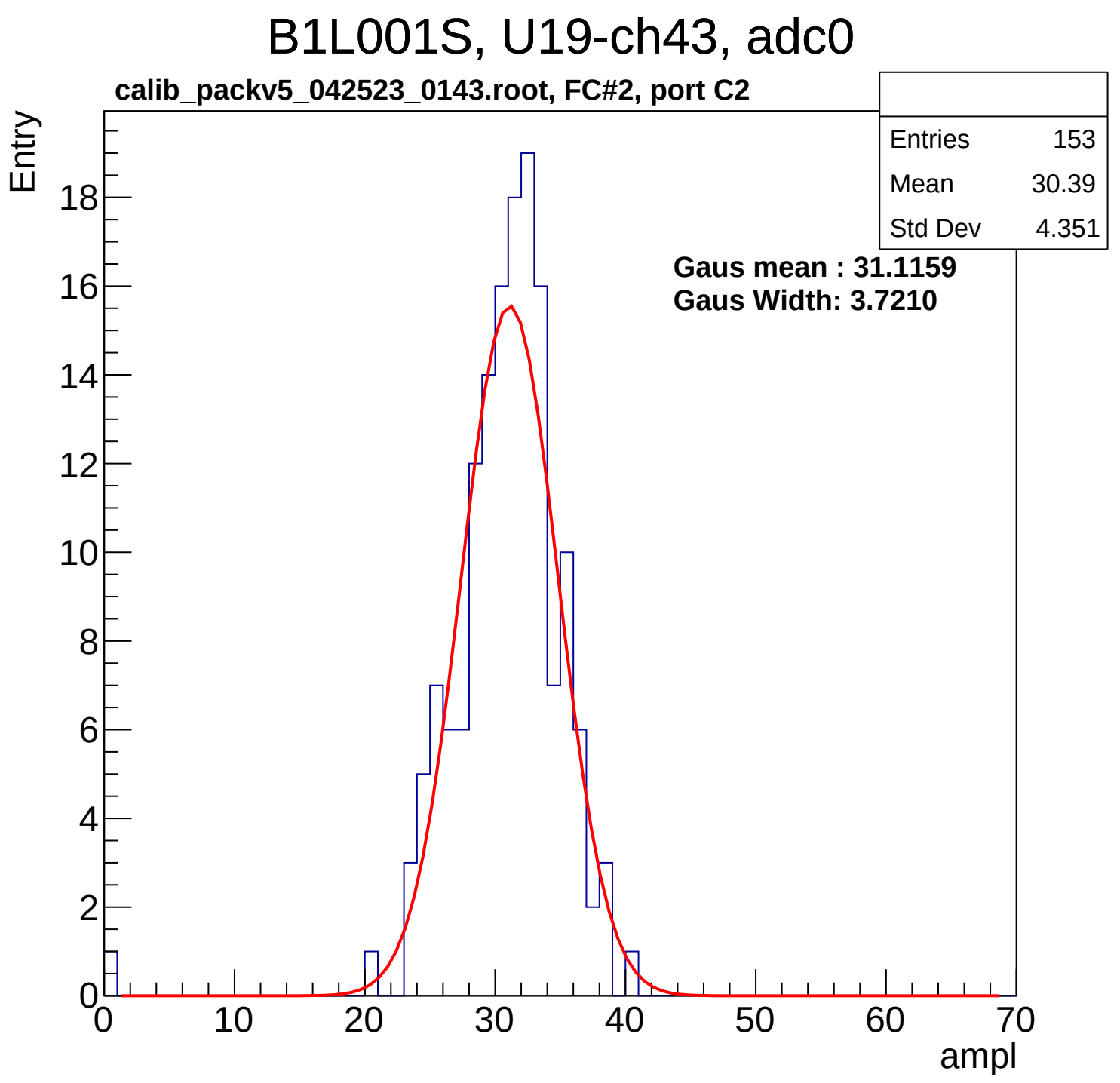
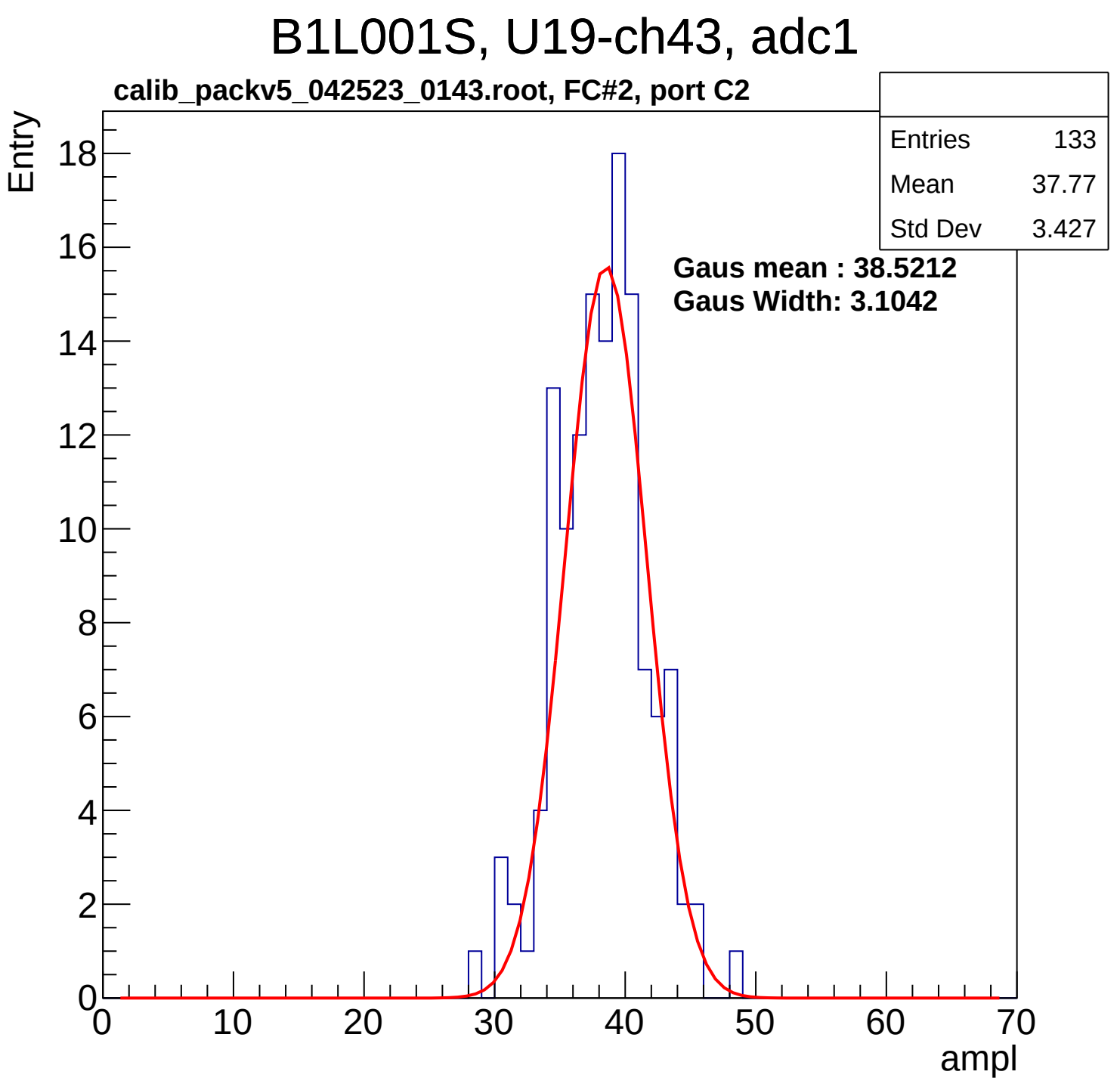
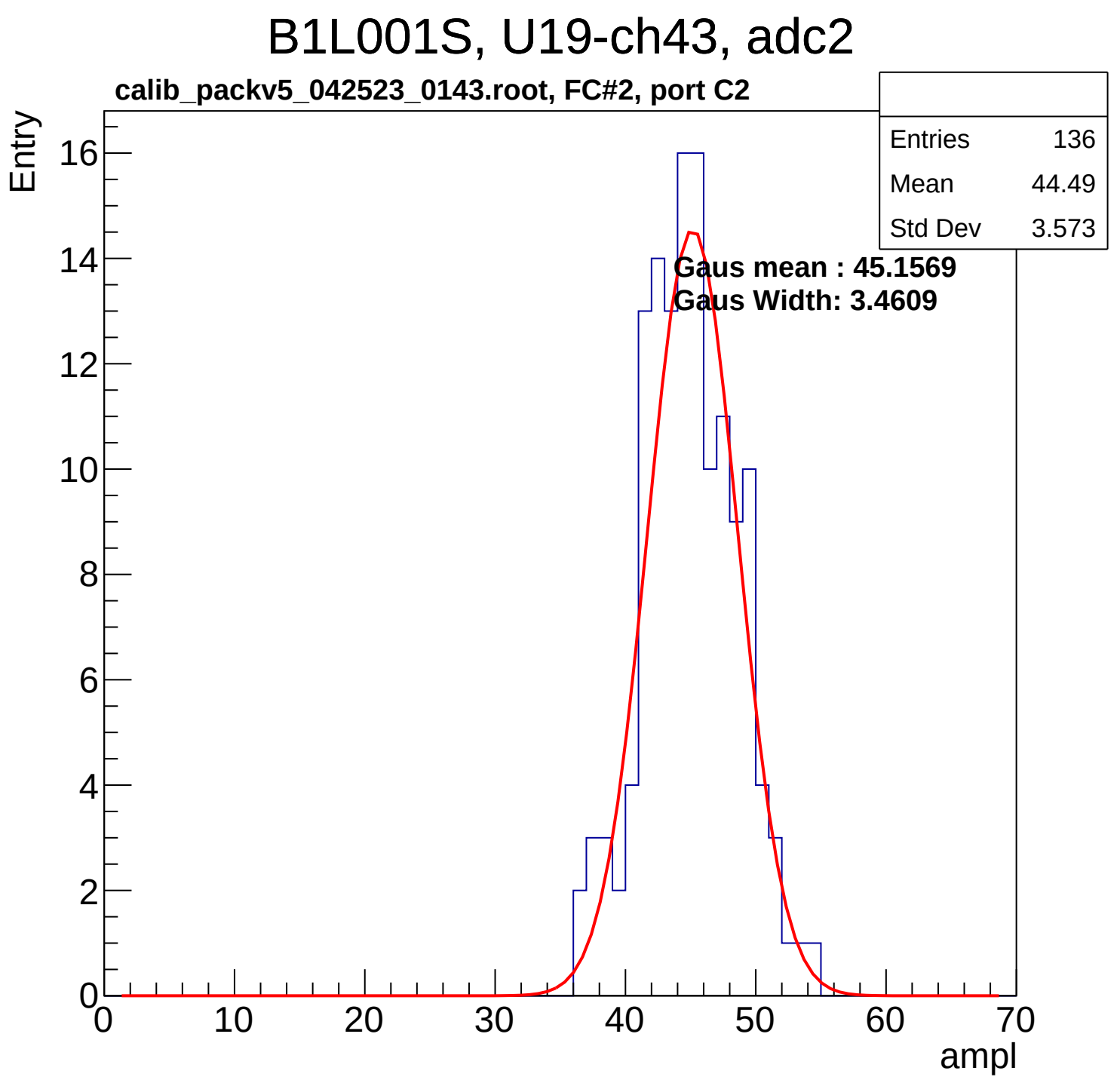
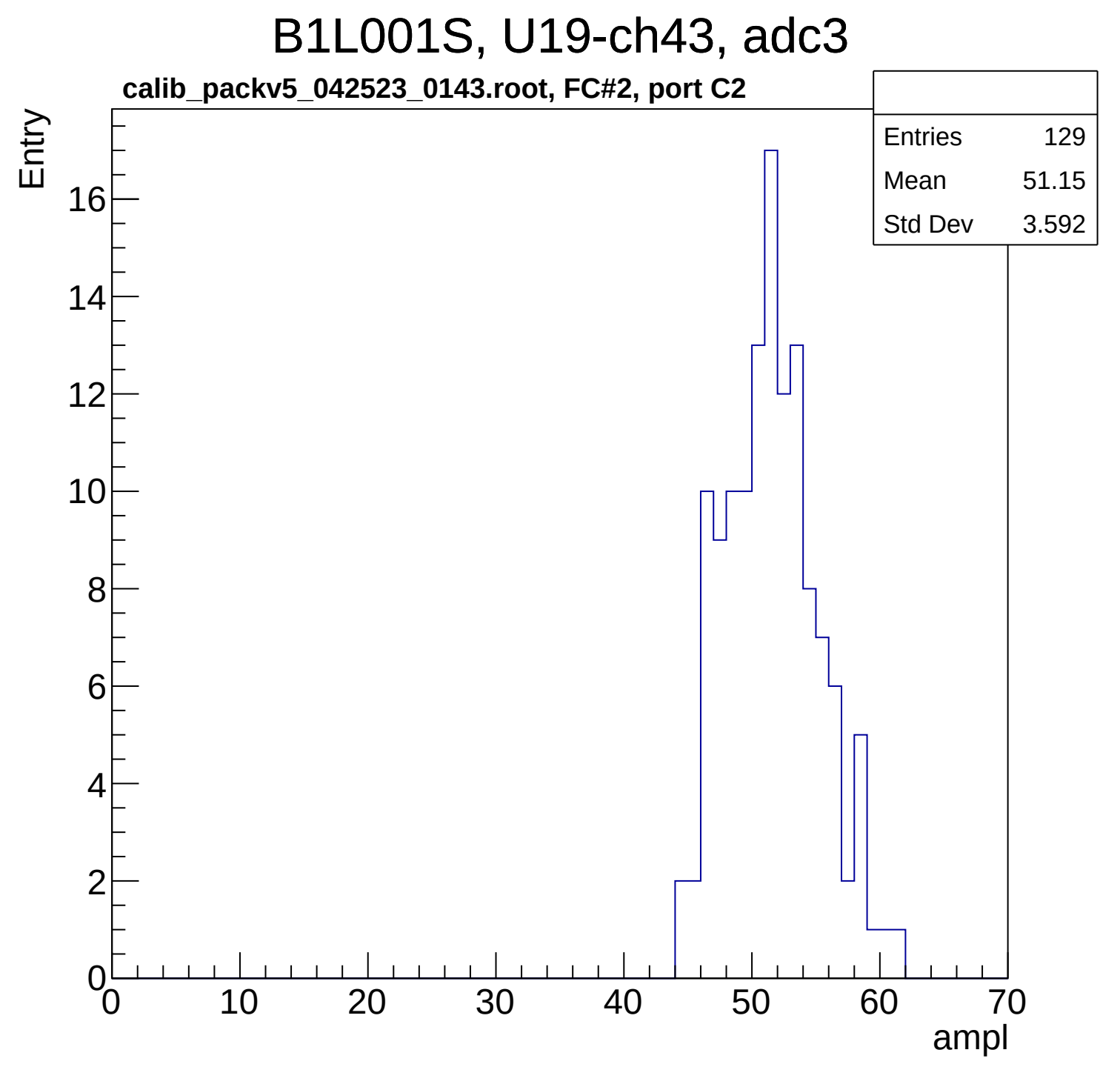

B1L001S, U19-ch42, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 14
Mean 61.71
Std Dev 1.385
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

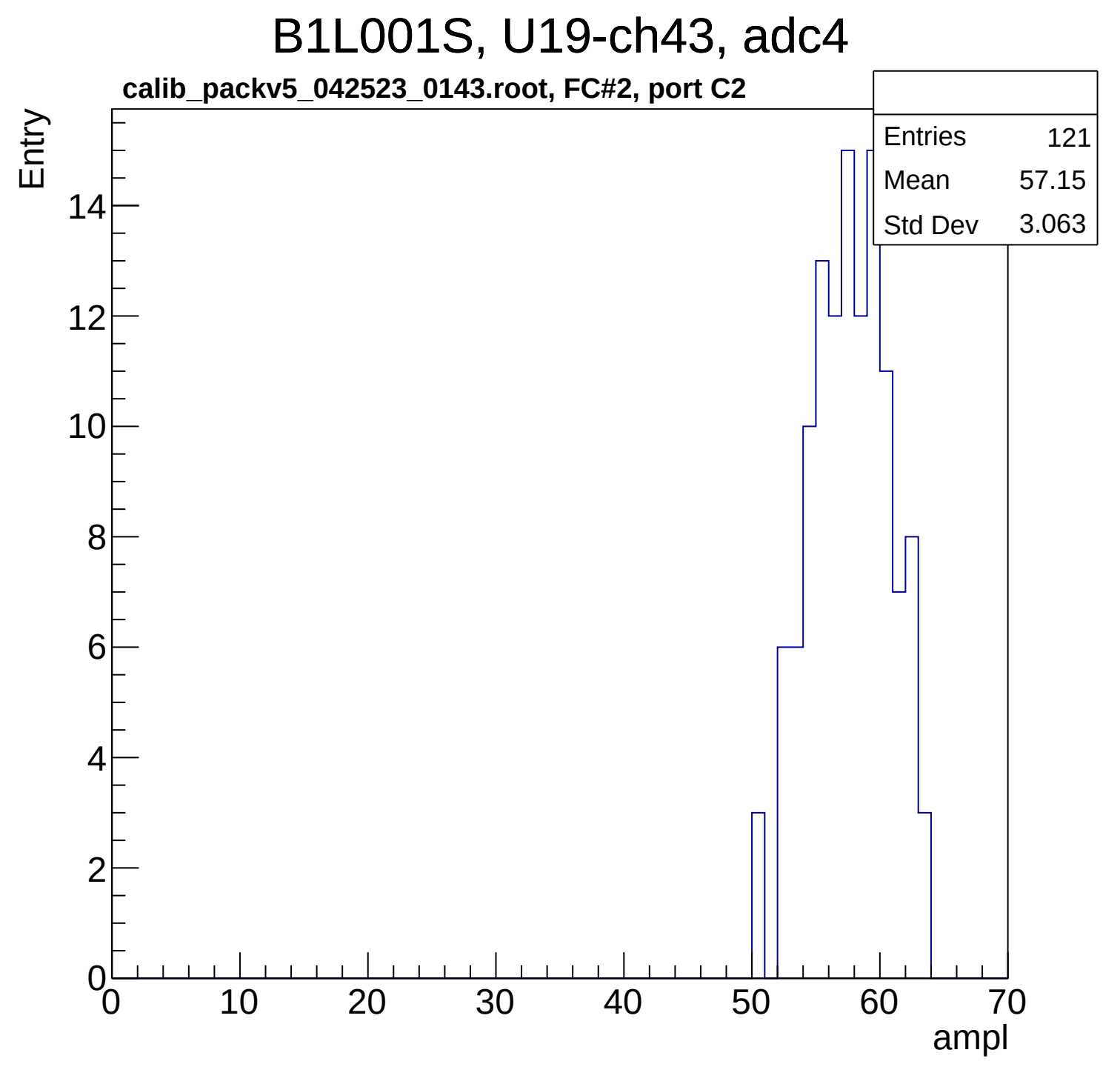

B1L001S, U19-ch42, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 23
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

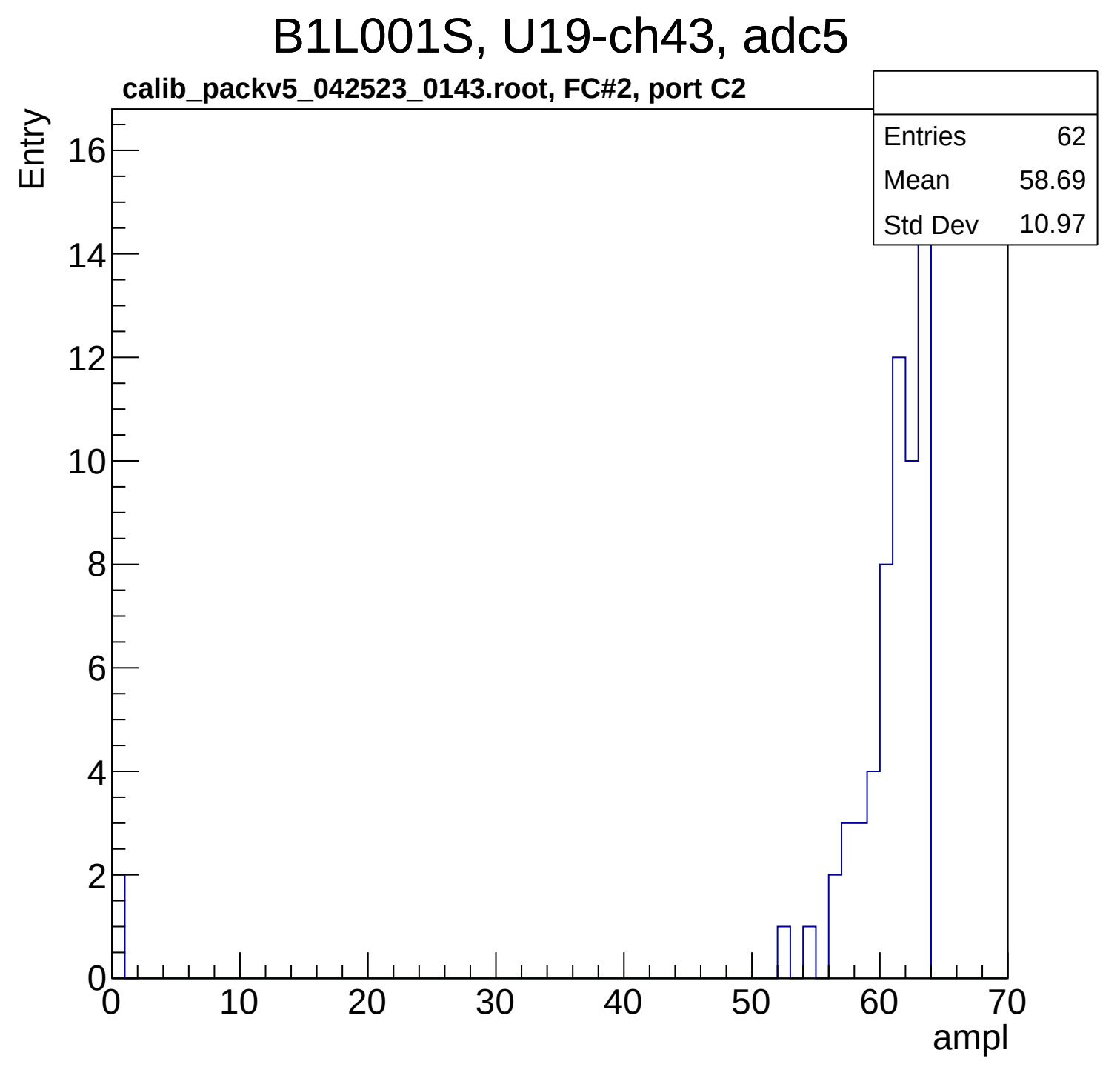

B1L001S, U19-ch43, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 153
Mean 30.39
Std Dev 4.351
Gaus mean : 31.1159
Gaus Width: 3.7210
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70


B1L001S, U19-ch43, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 133
Mean 37.77
Std Dev 3.427
Gaus mean : 38.5212
Gaus Width: 3.1042
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70


B1L001S, U19-ch43, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 136
Mean 44.49
Std Dev 3.573
Gaus mean : 45.1569
Gaus Width: 3.4609
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70


B1L001S, U19-ch43, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 129
Mean 51.15
Std Dev 3.592
Entry
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch43, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 121
Mean 57.15
Std Dev 3.063
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch43, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 62
Mean 58.69
Std Dev 10.97
Entry
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4
6
8
10
12
14
16
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10
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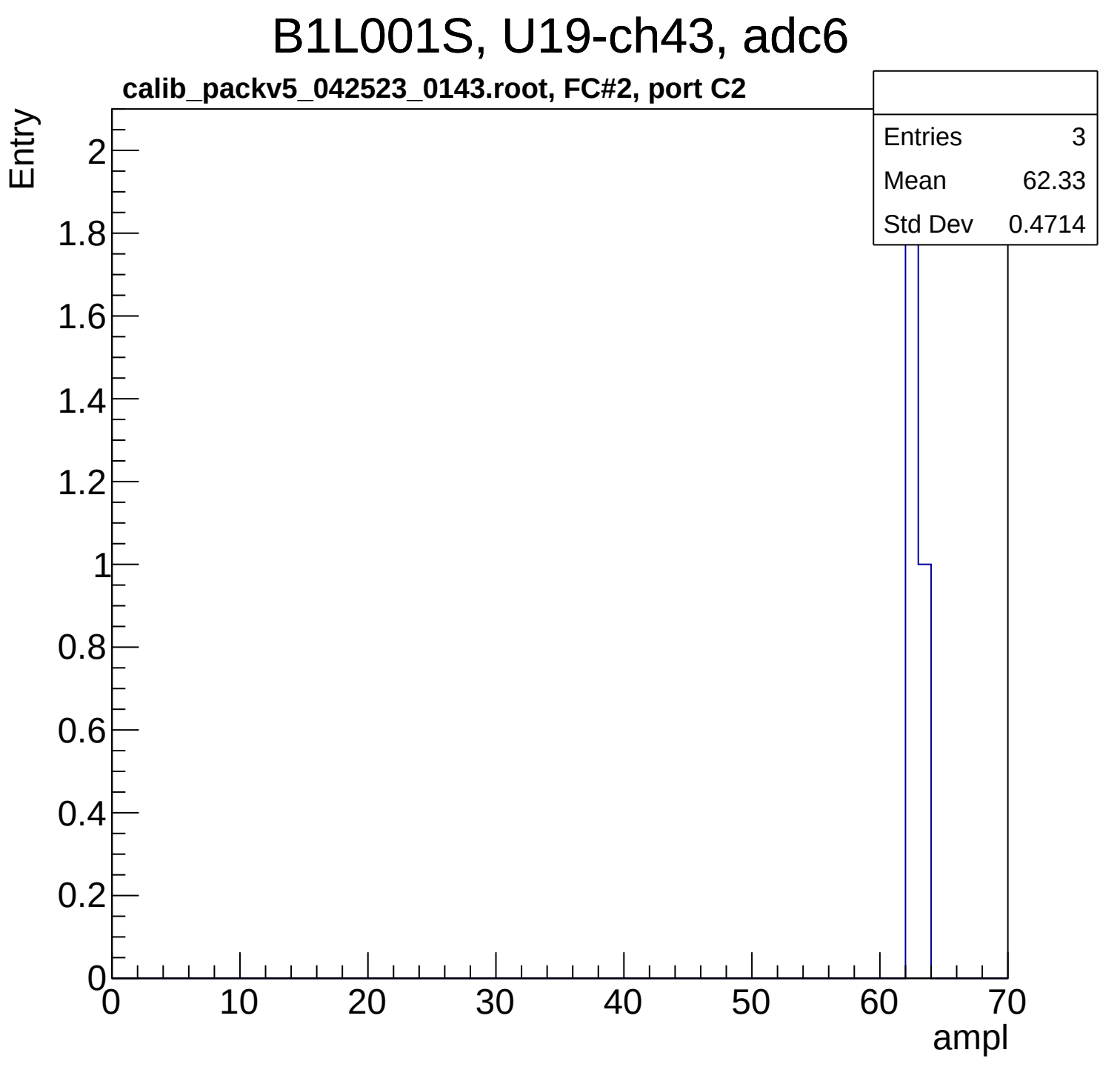
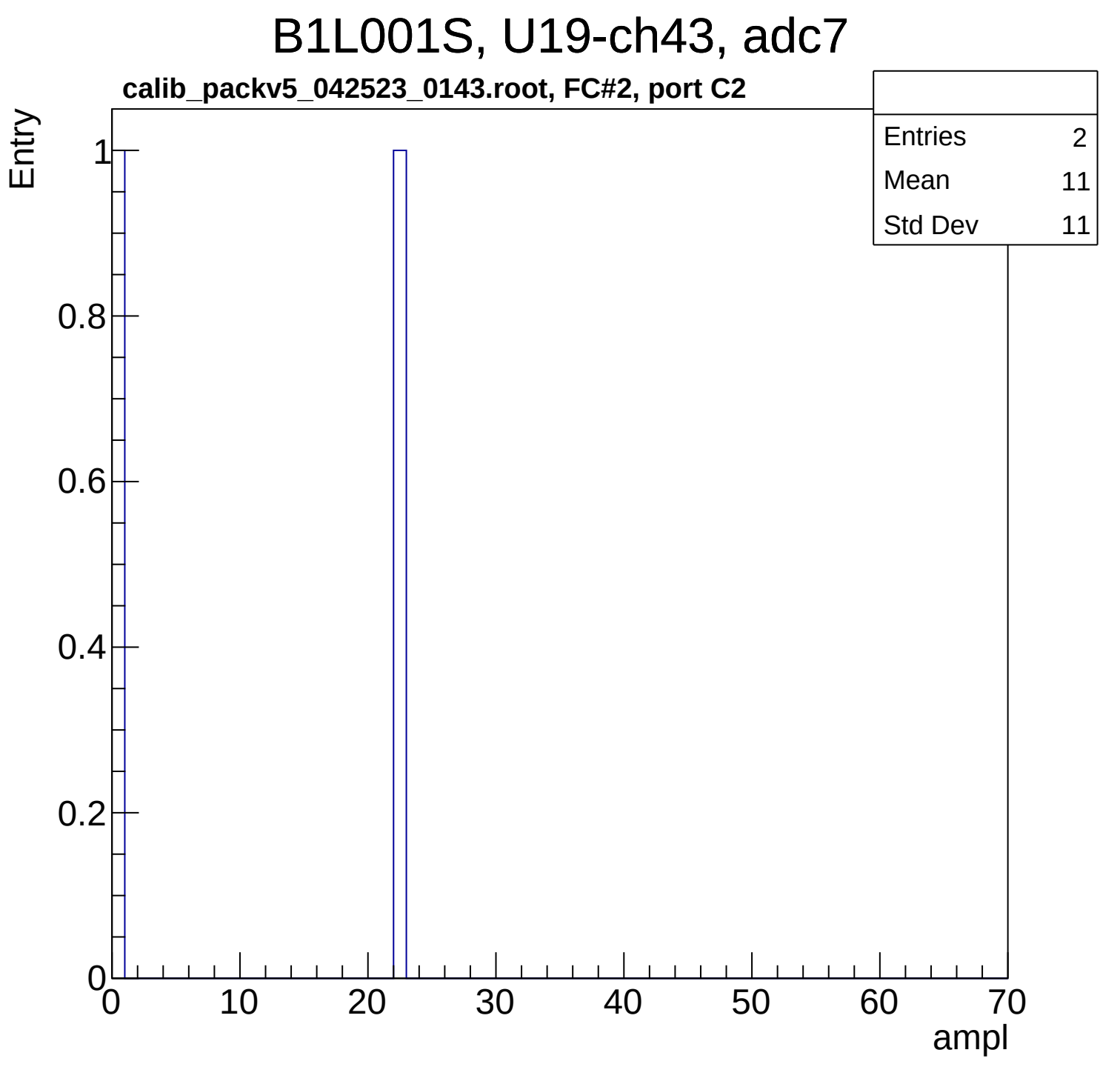
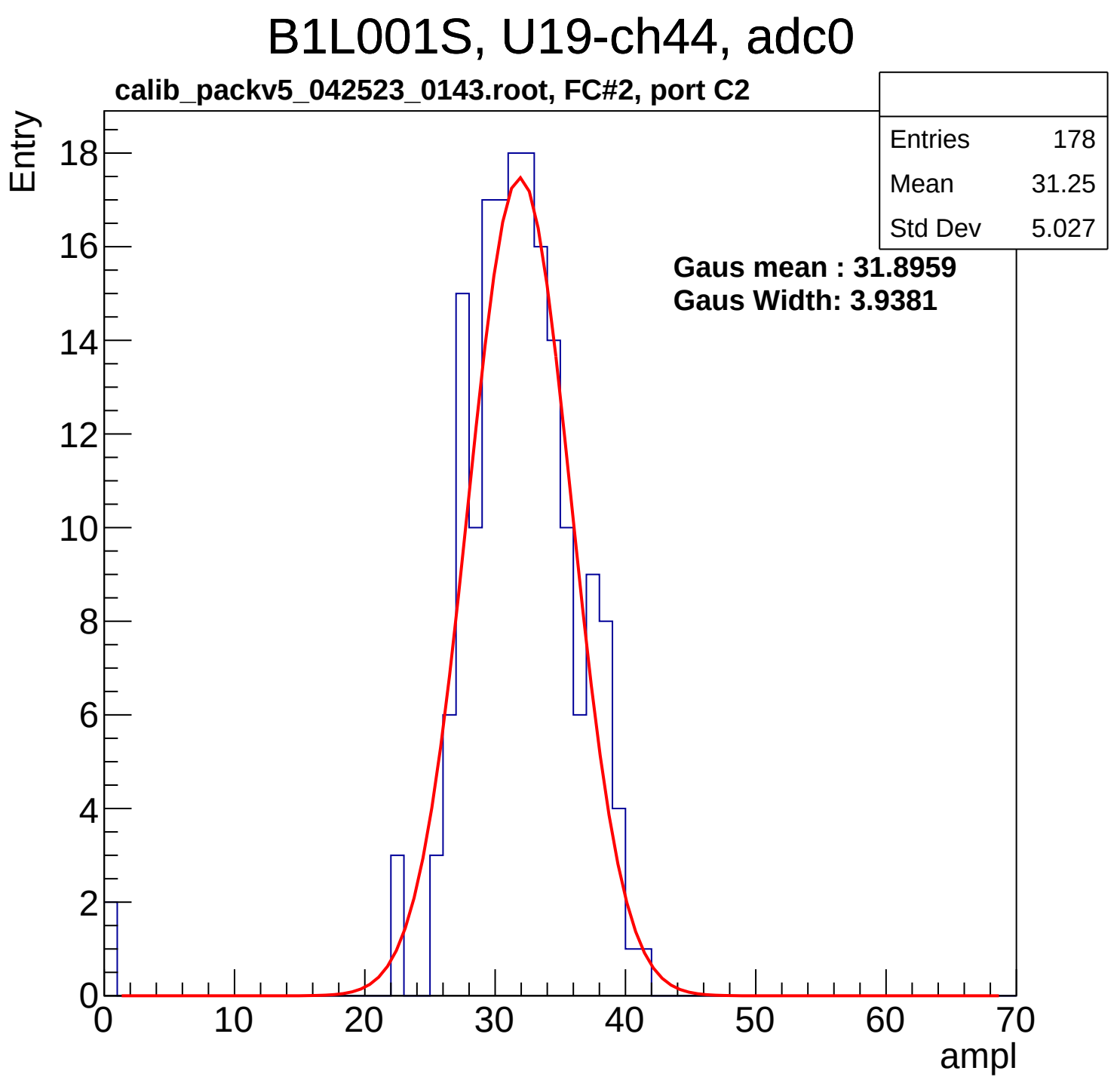
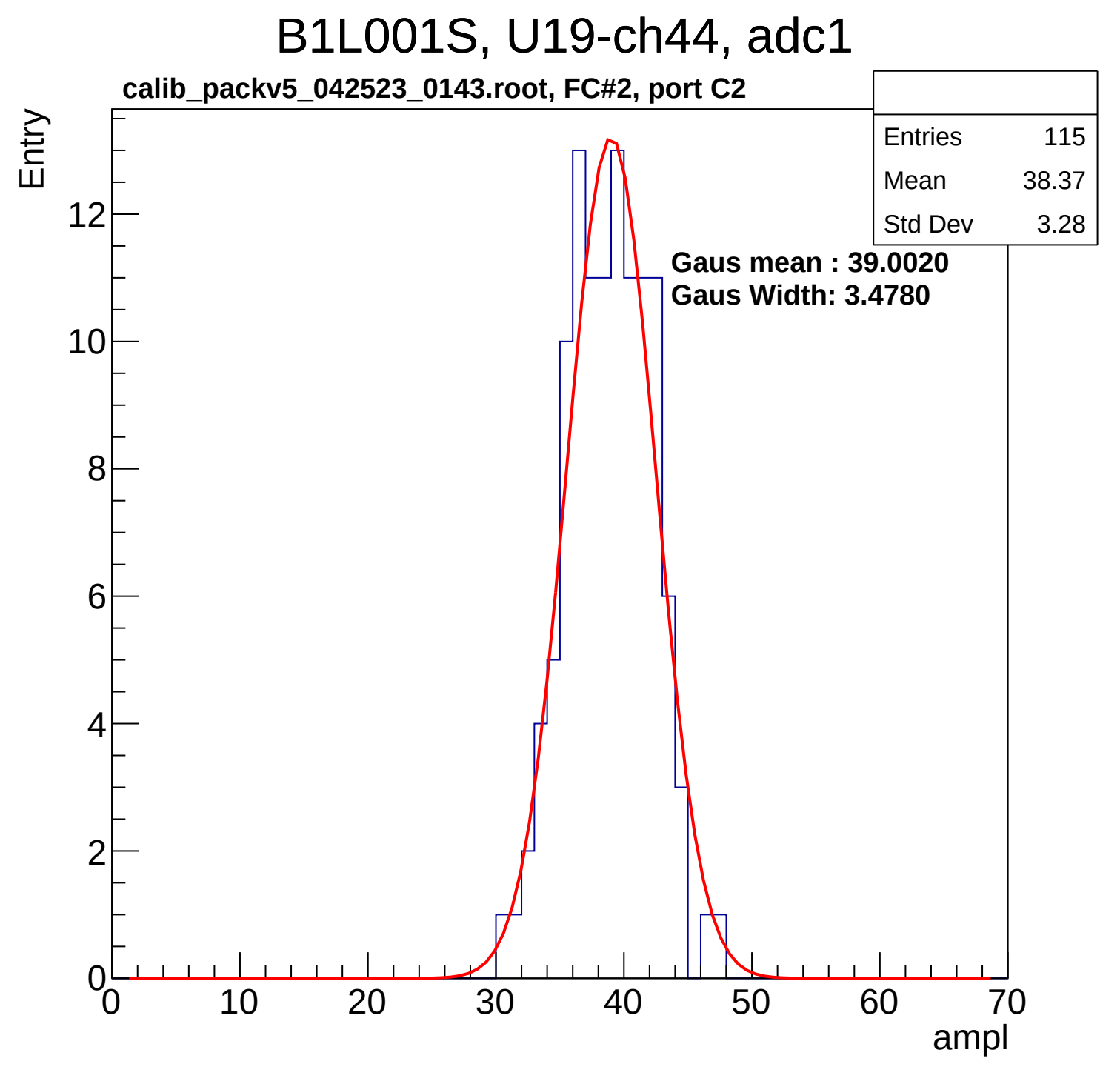
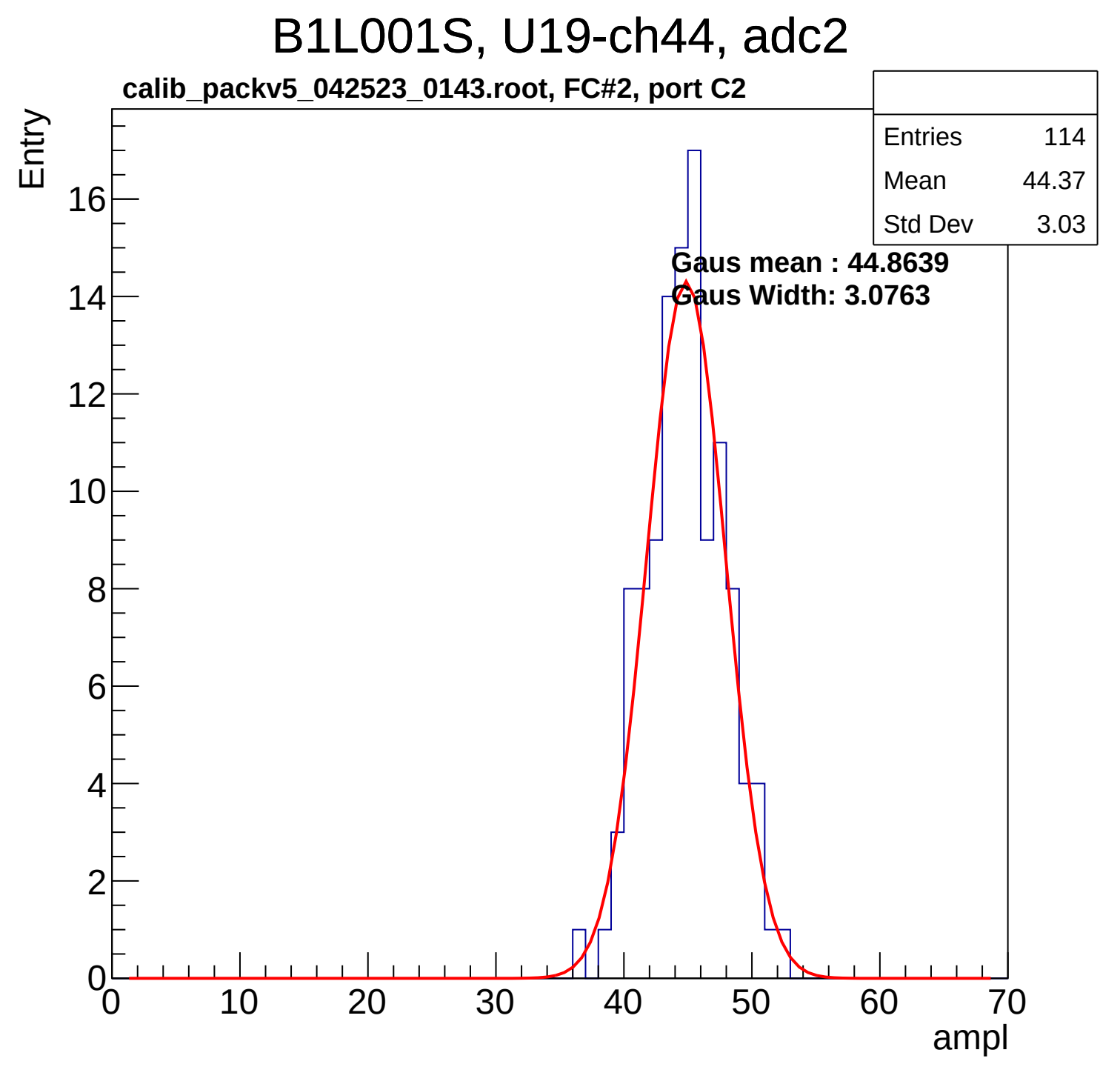
30
40
50
60
70
ampl


B1L001S, U19-ch43, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 3
Mean 62.33
Std Dev 0.4714
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L001S, U19-ch43, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 11
Std Dev 11
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch44, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 178
Mean 31.25
Std Dev 5.027
Gaus mean : 31.8959
Gaus Width: 3.9381
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70


B1L001S, U19-ch44, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 115
Mean 38.37
Std Dev 3.28
Gaus mean : 39.0020
Gaus Width: 3.4780
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70


B1L001S, U19-ch44, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 114
Mean 44.37
Std Dev 3.03
Gaus mean : 44.8639
Gaus Width: 3.0763
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
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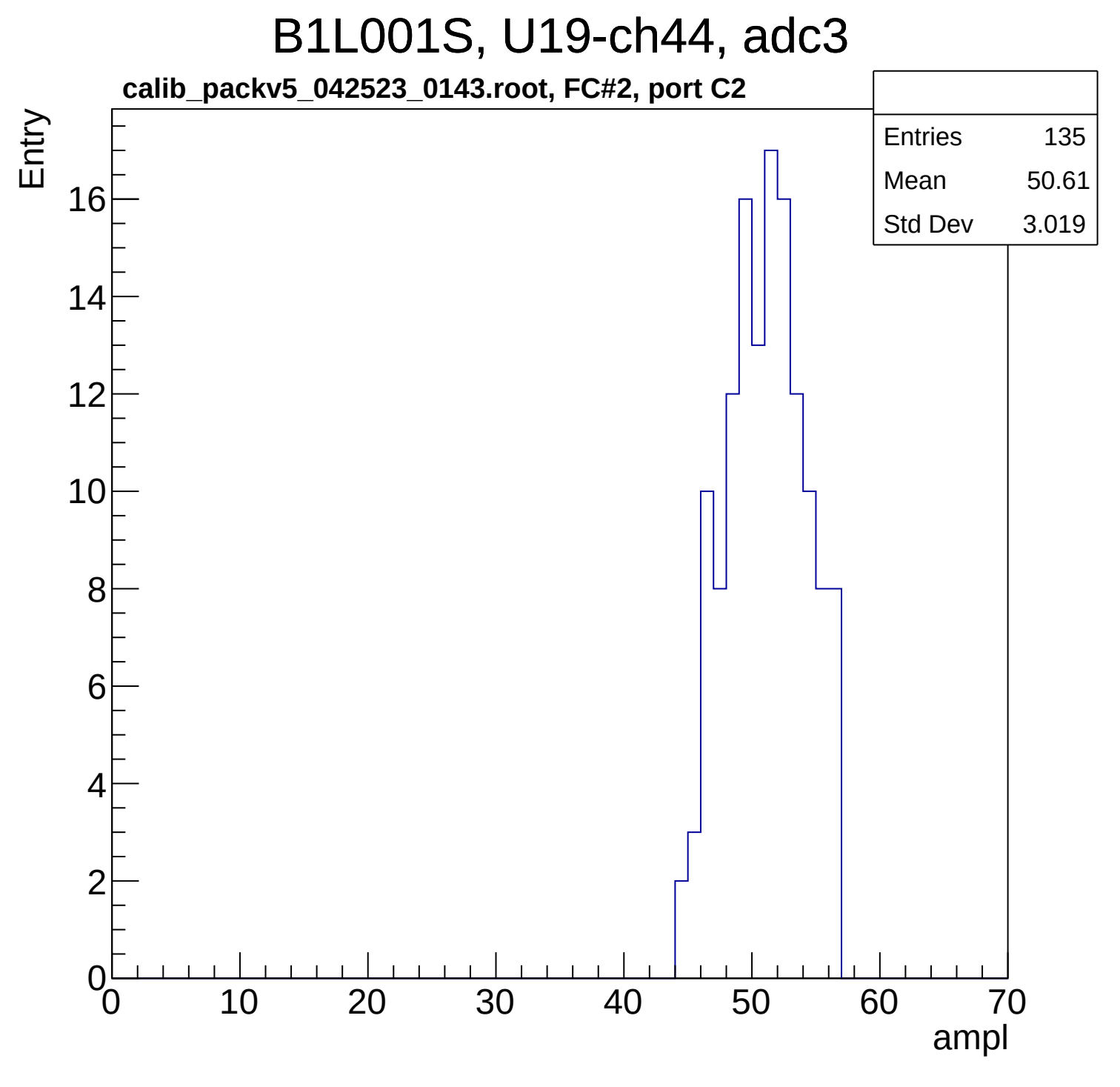
B1L001S, U19-ch44, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 135
Mean 50.61
Std Dev 3.019
Entry
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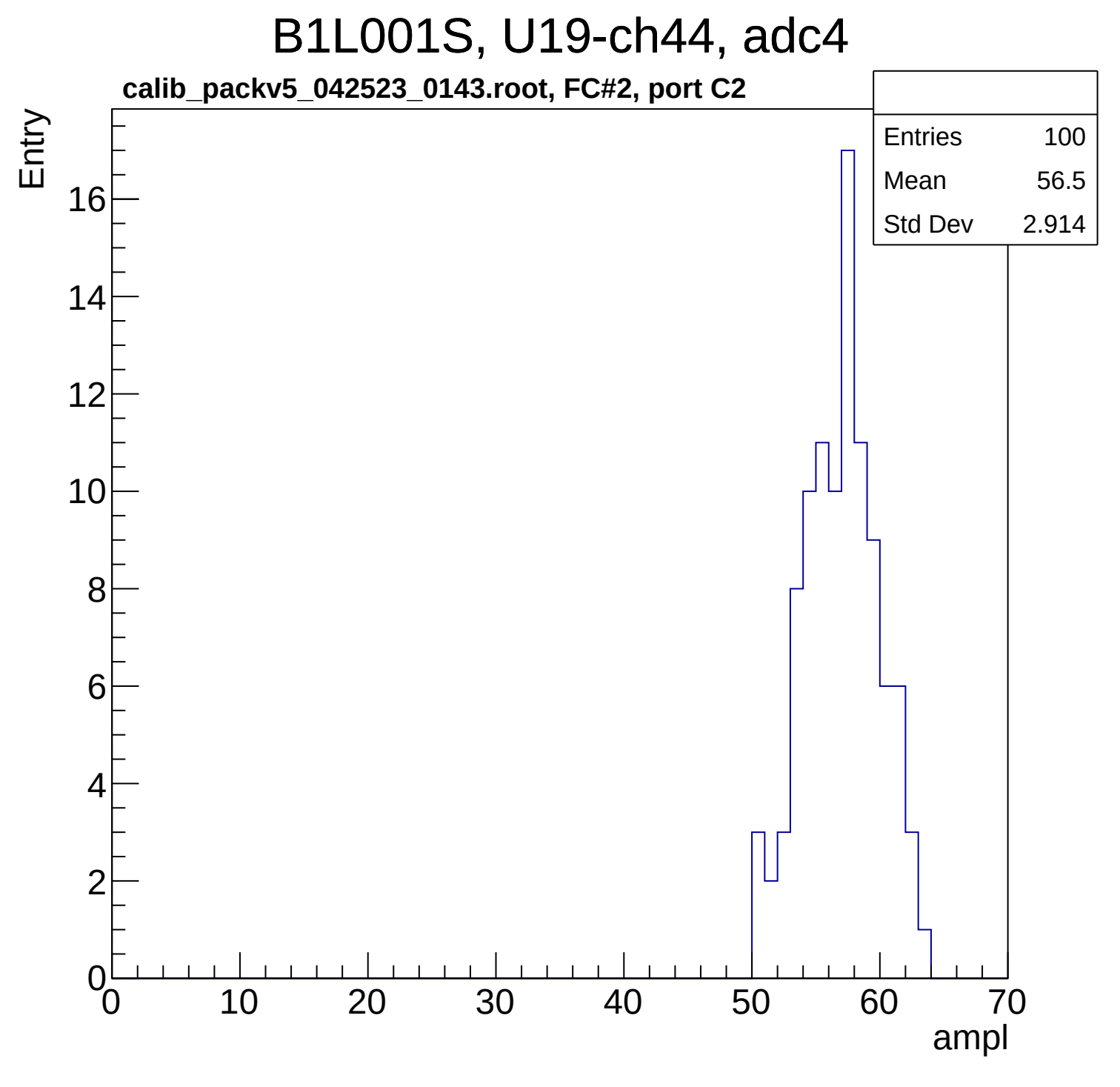
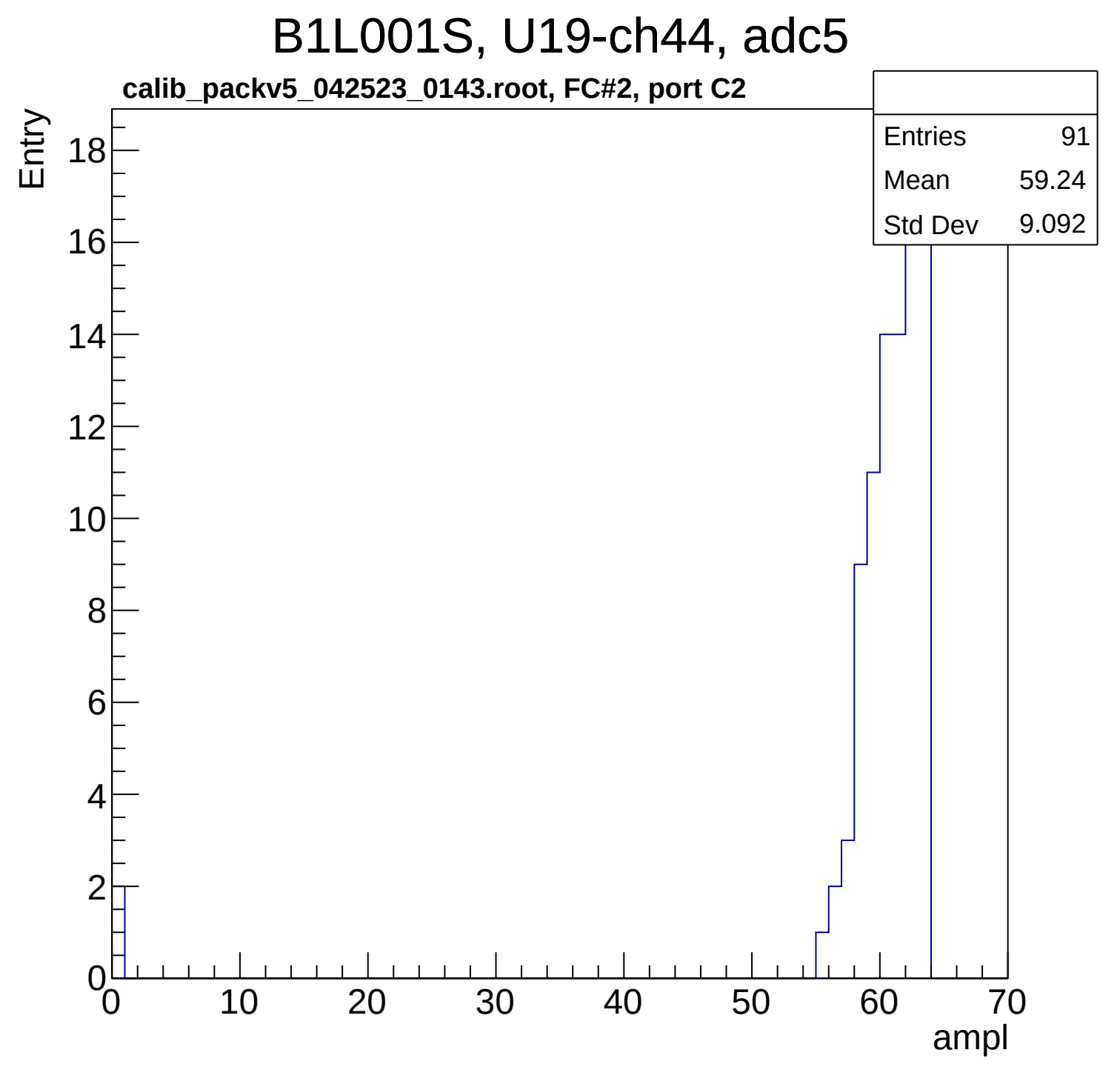
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch44, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 100
Mean 56.5
Std Dev 2.914
Entry
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch44, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 91
Mean 59.24
Std Dev 9.092
Entry
0
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6
8
10
12
14
16
18
0
10
20
30
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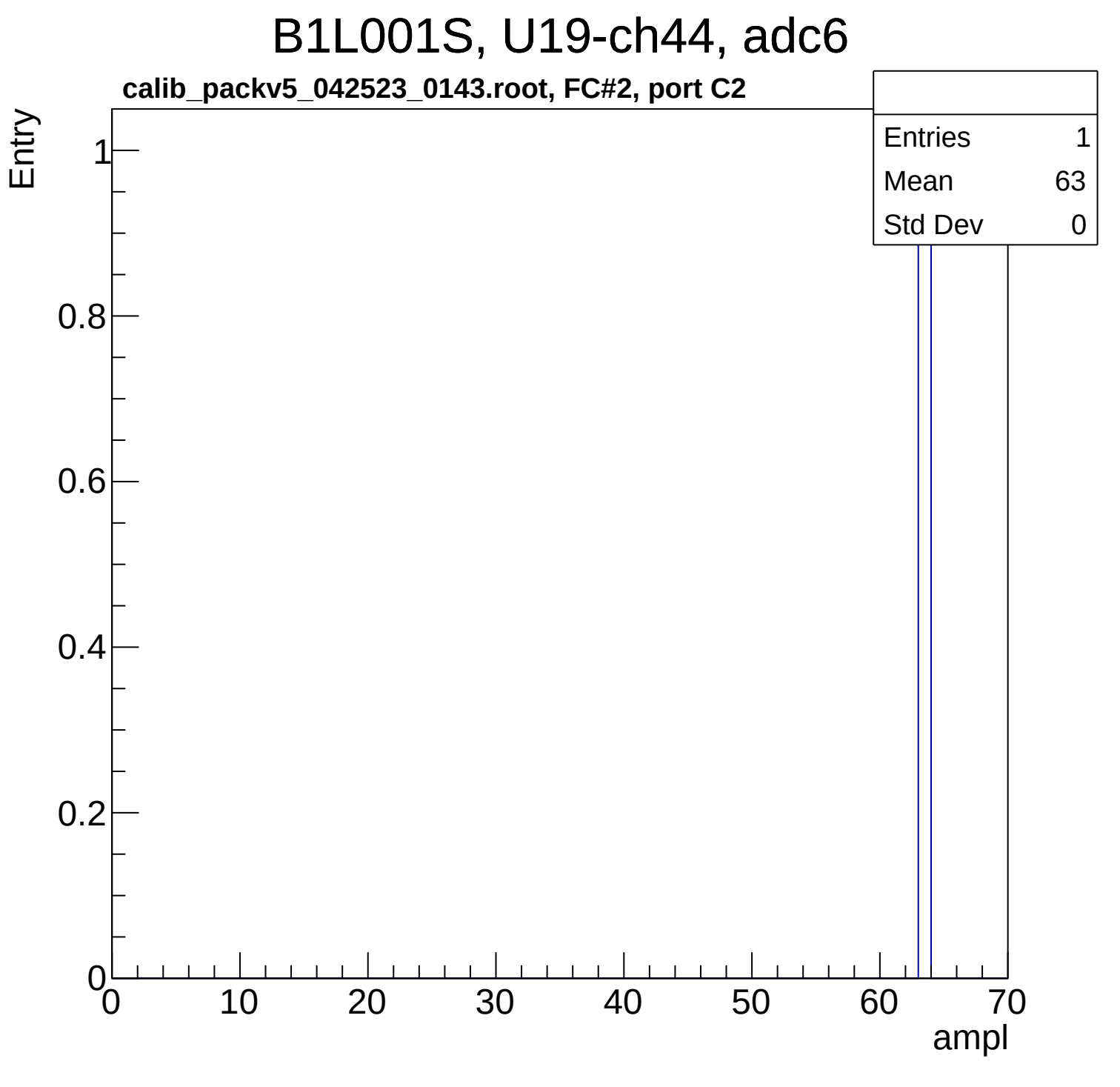
50
60
70
ampl


B1L001S, U19-ch44, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 63
Std Dev 0
Entry
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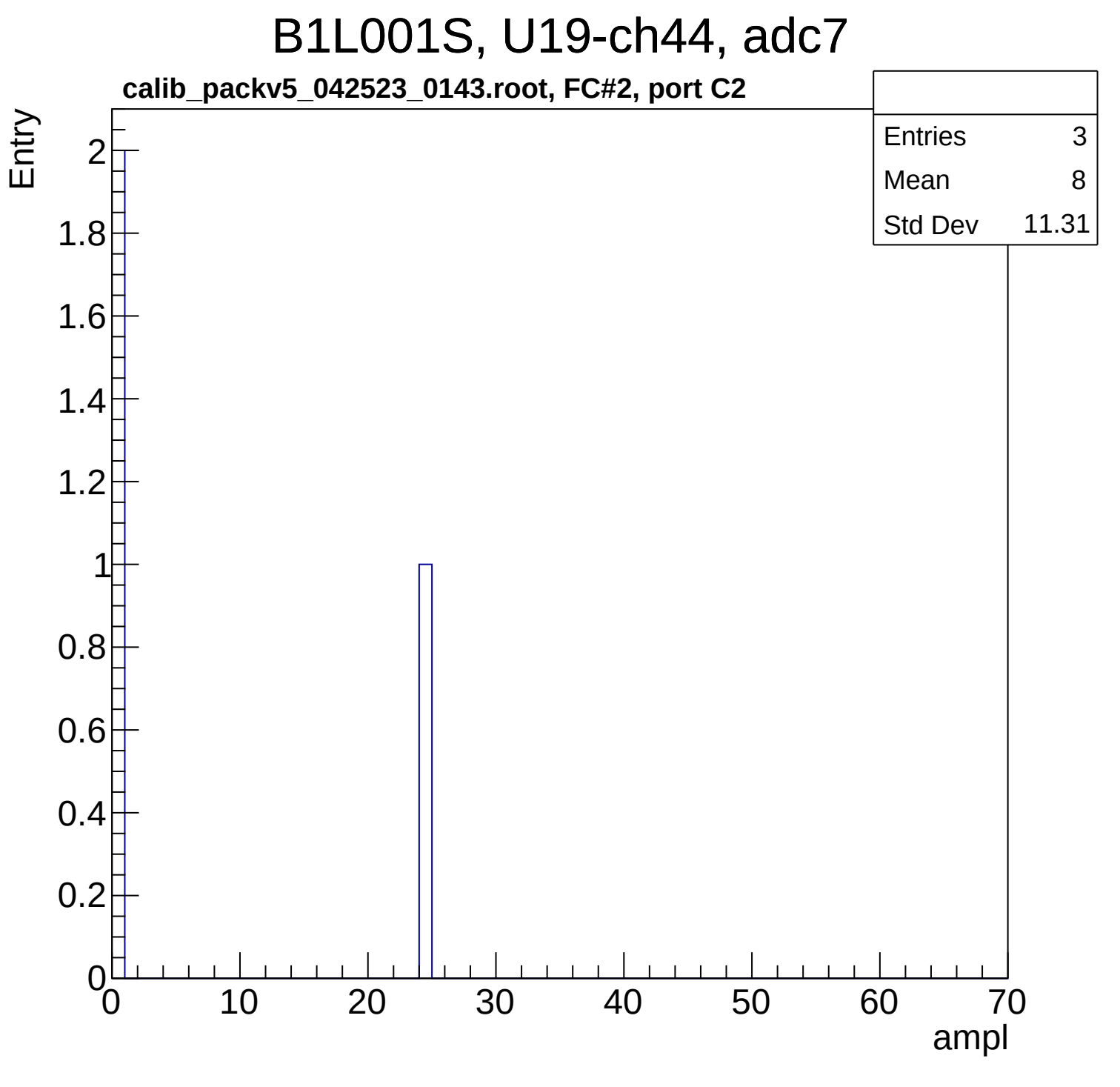
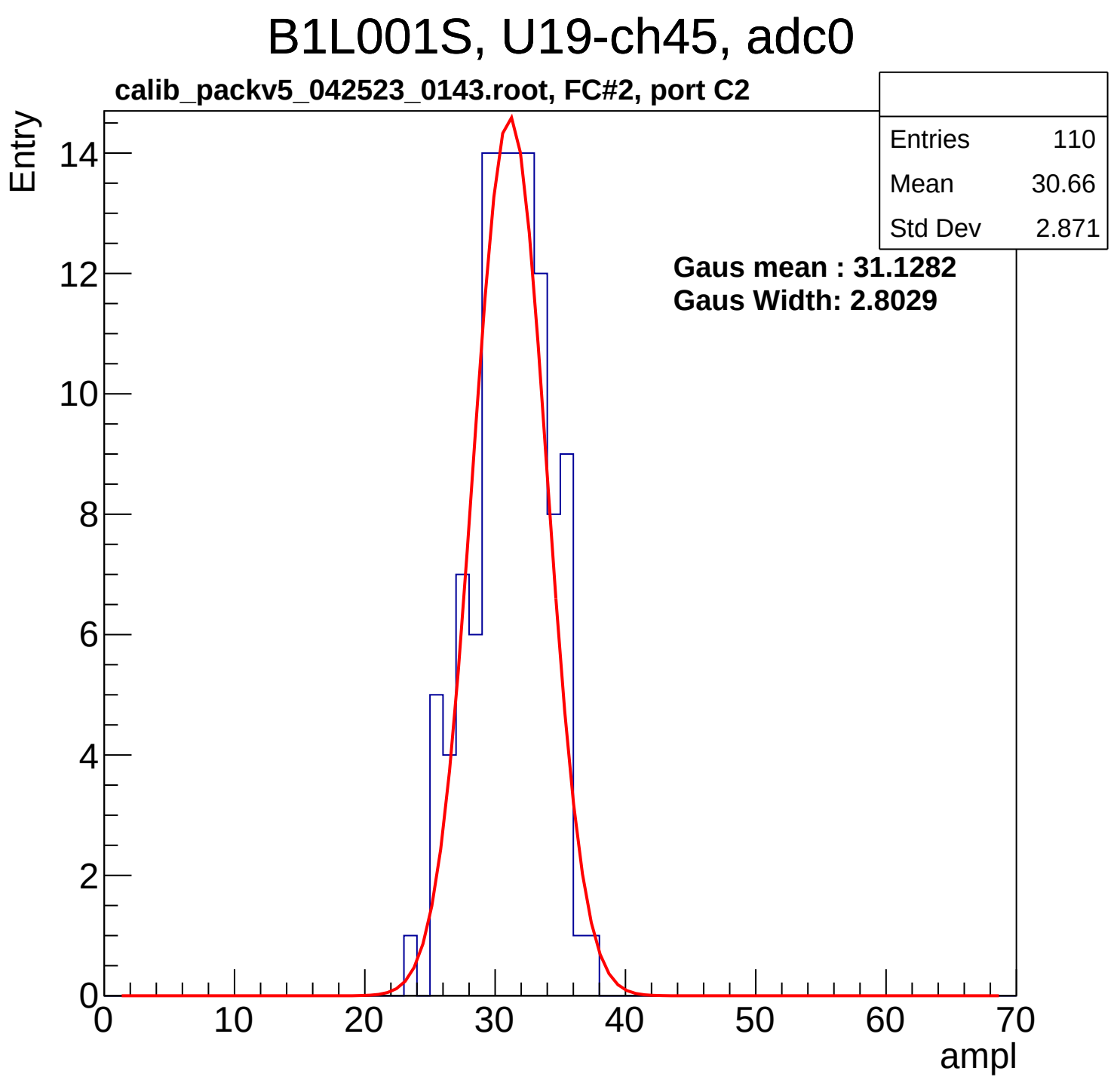
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch44, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 3
Mean 8
Std Dev 11.31
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L001S, U19-ch45, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 110
Mean 30.66
Std Dev 2.871
Gaus mean : 31.1282
Gaus Width: 2.8029
Entry
ampl
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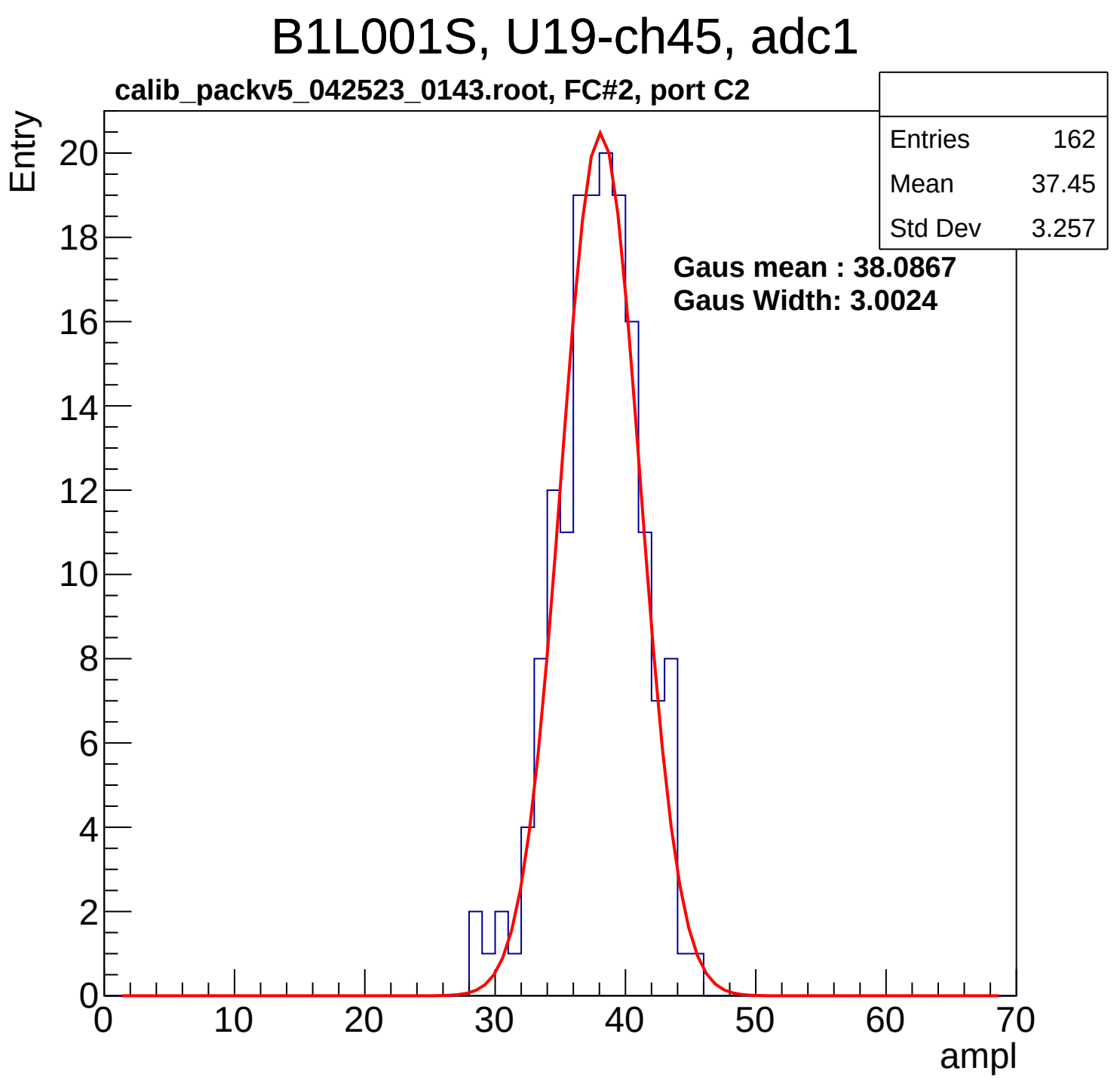
B1L001S, U19-ch45, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 162
Mean 37.45
Std Dev 3.257
Gaus mean : 38.0867
Gaus Width: 3.0024
Entry
ampl
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6
8
10
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14
16
18
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0
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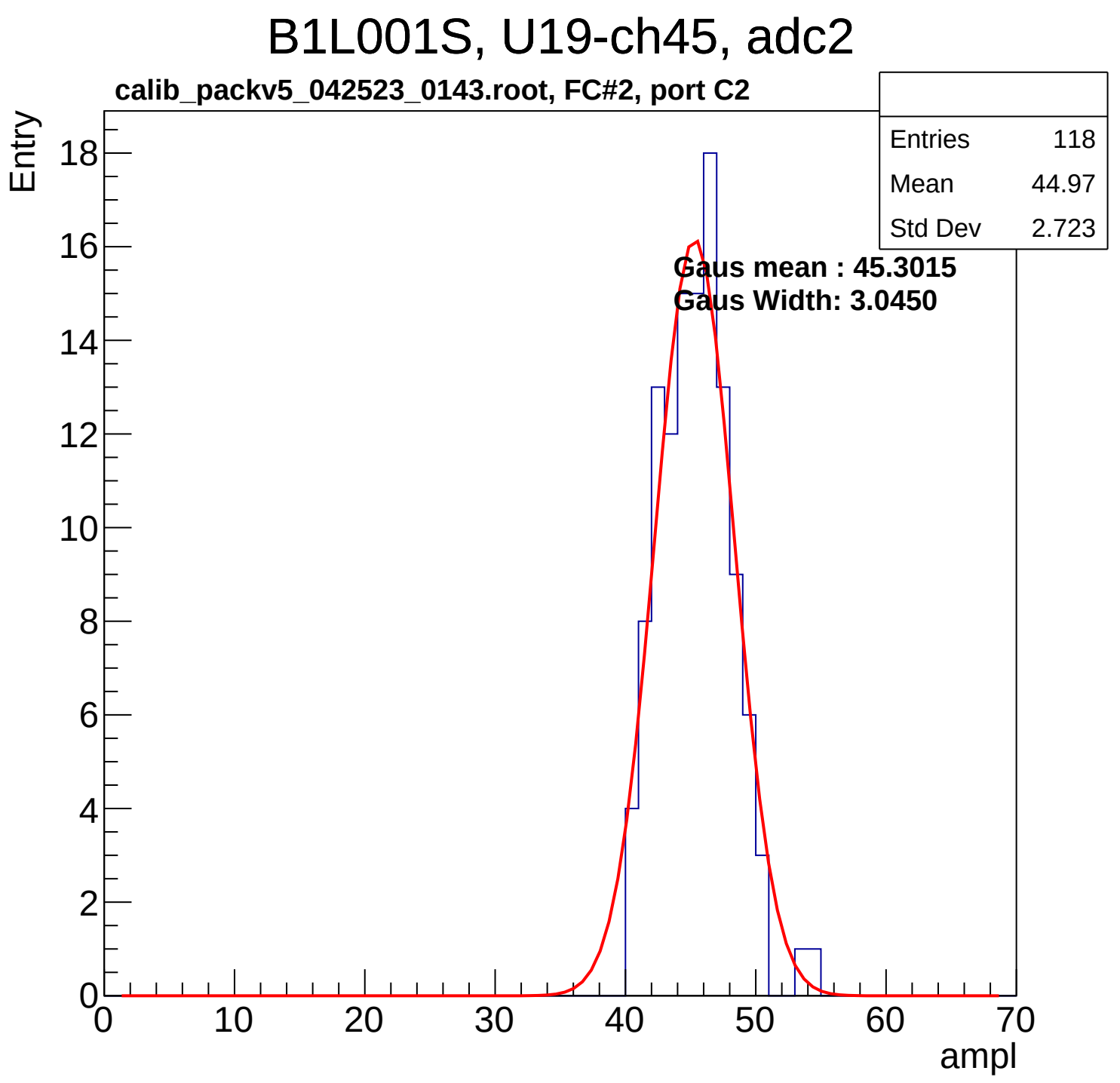
B1L001S, U19-ch45, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 118
Mean 44.97
Std Dev 2.723
Gaus mean : 45.3015
Gaus Width: 3.0450
Entry
ampl
0
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4
6
8
10
12
14
16
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0
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20
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40
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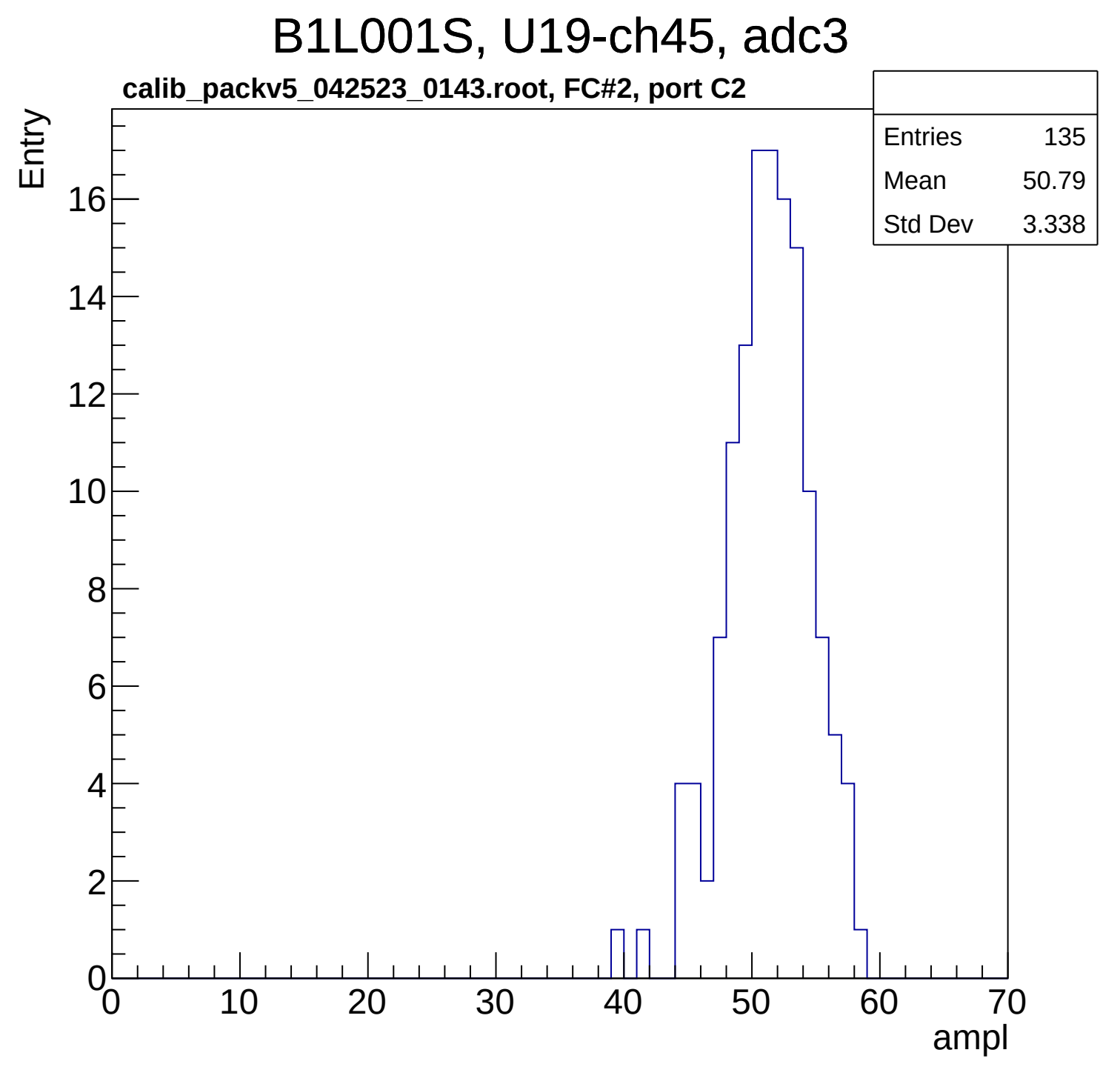
B1L001S, U19-ch45, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 135
Mean 50.79
Std Dev 3.338
Entry
ampl
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2
4
6
8
10
12
14
16
0
10
20
30
40
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60
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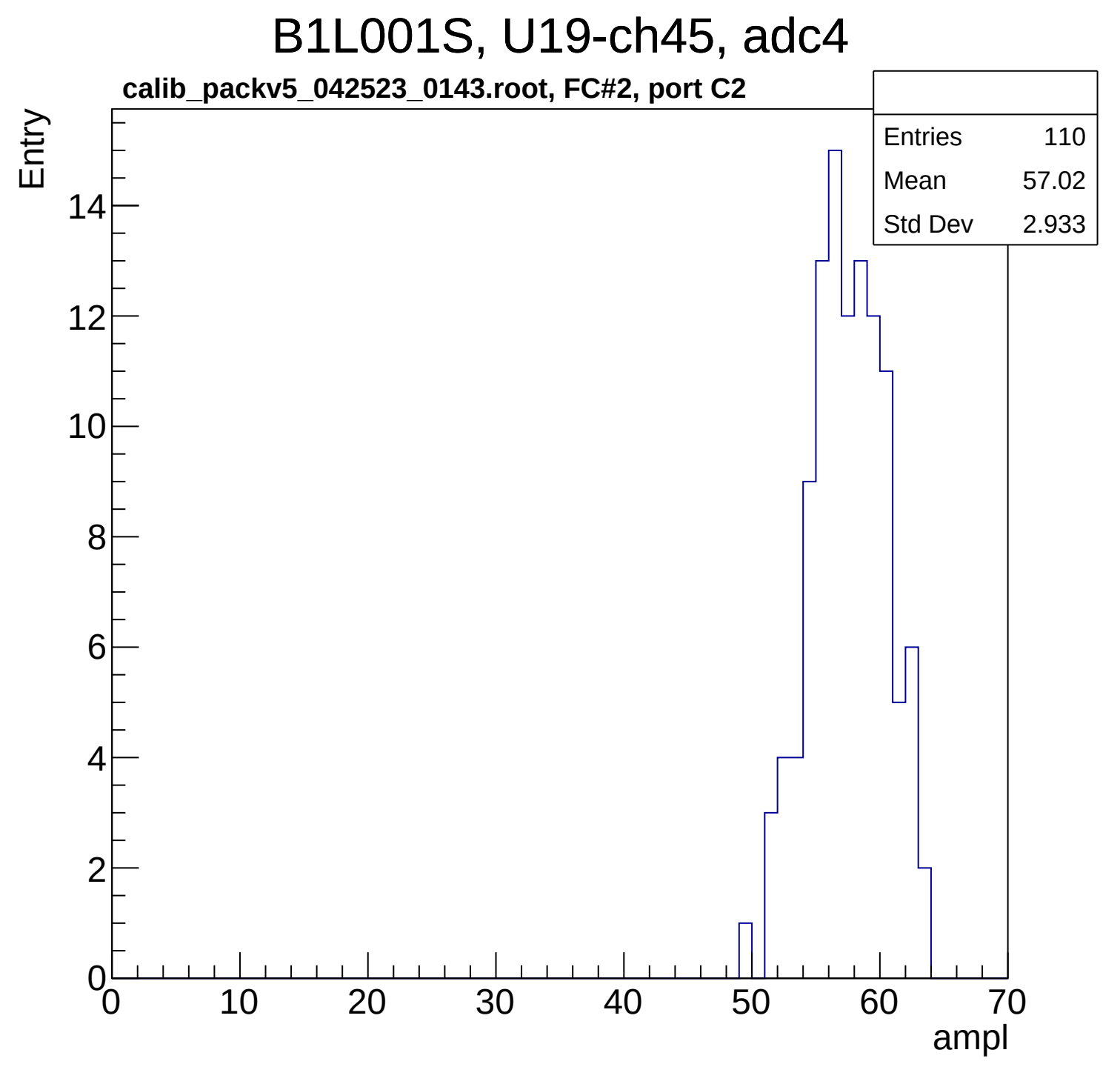
B1L001S, U19-ch45, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 110
Mean 57.02
Std Dev 2.933
Entry
ampl
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2
4
6
8
10
12
14
0
10
20
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40
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60
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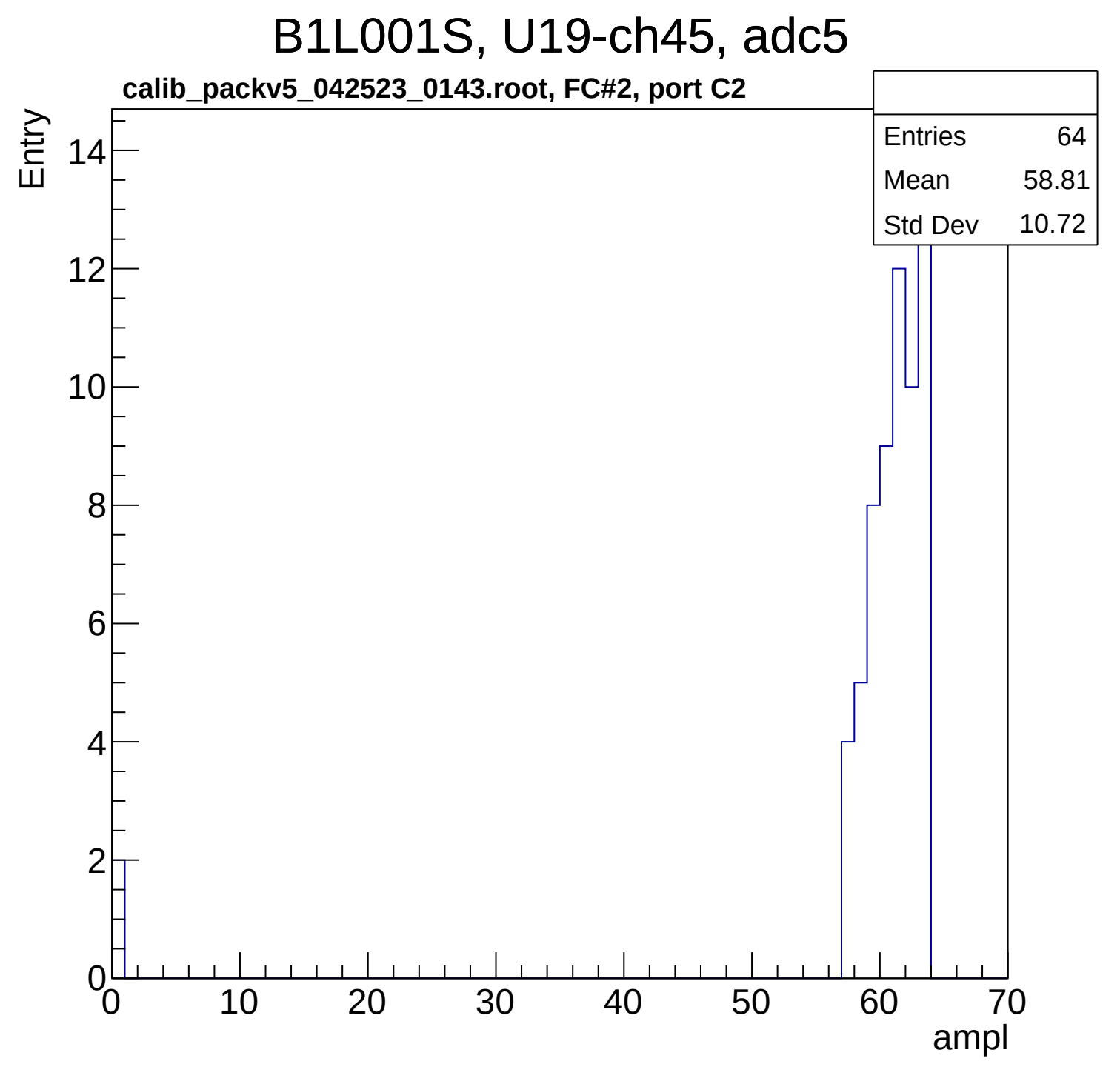
B1L001S, U19-ch45, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 64
Mean 58.81
Std Dev 10.72
Entry
ampl
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2
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0
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40
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60
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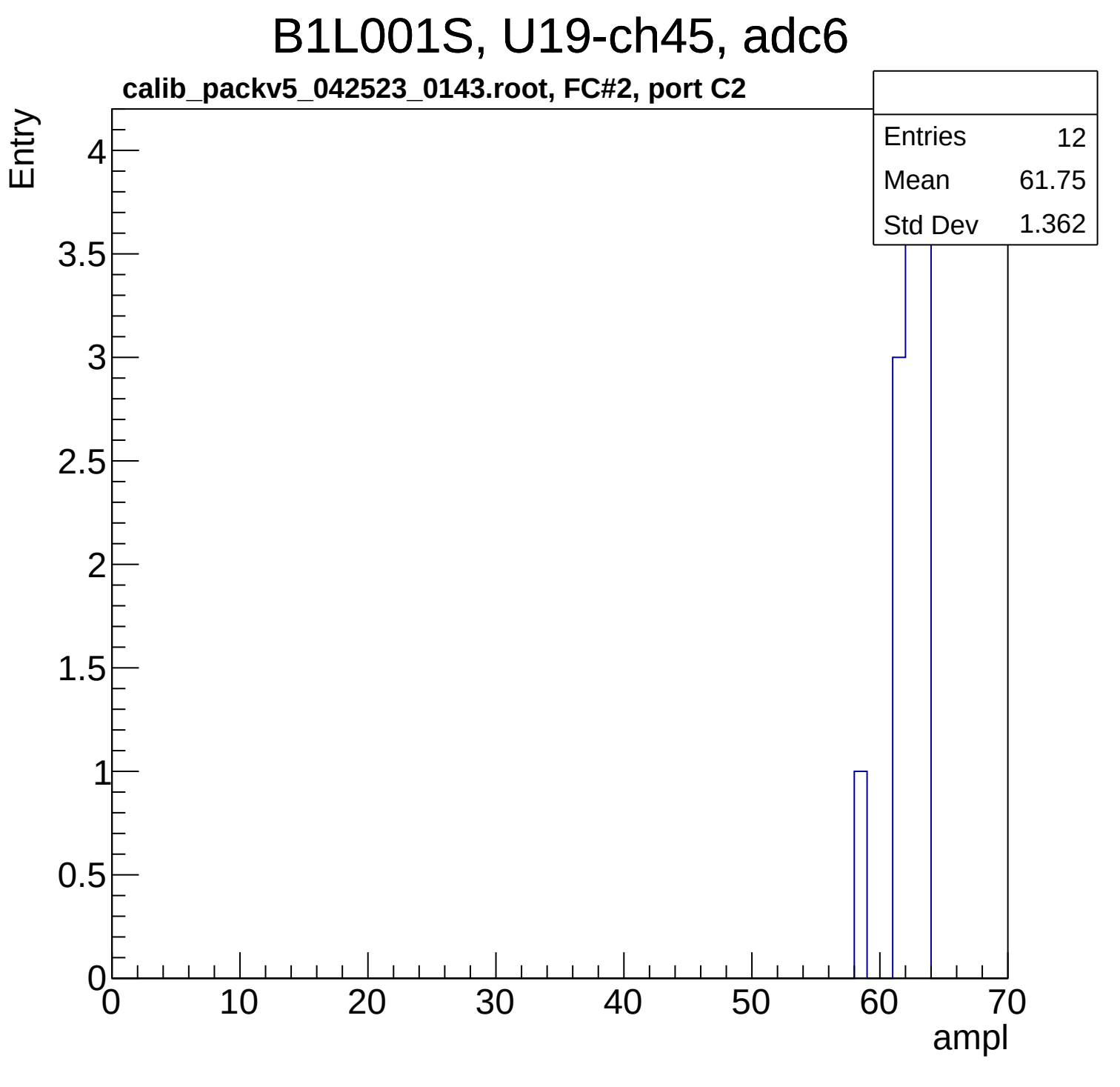
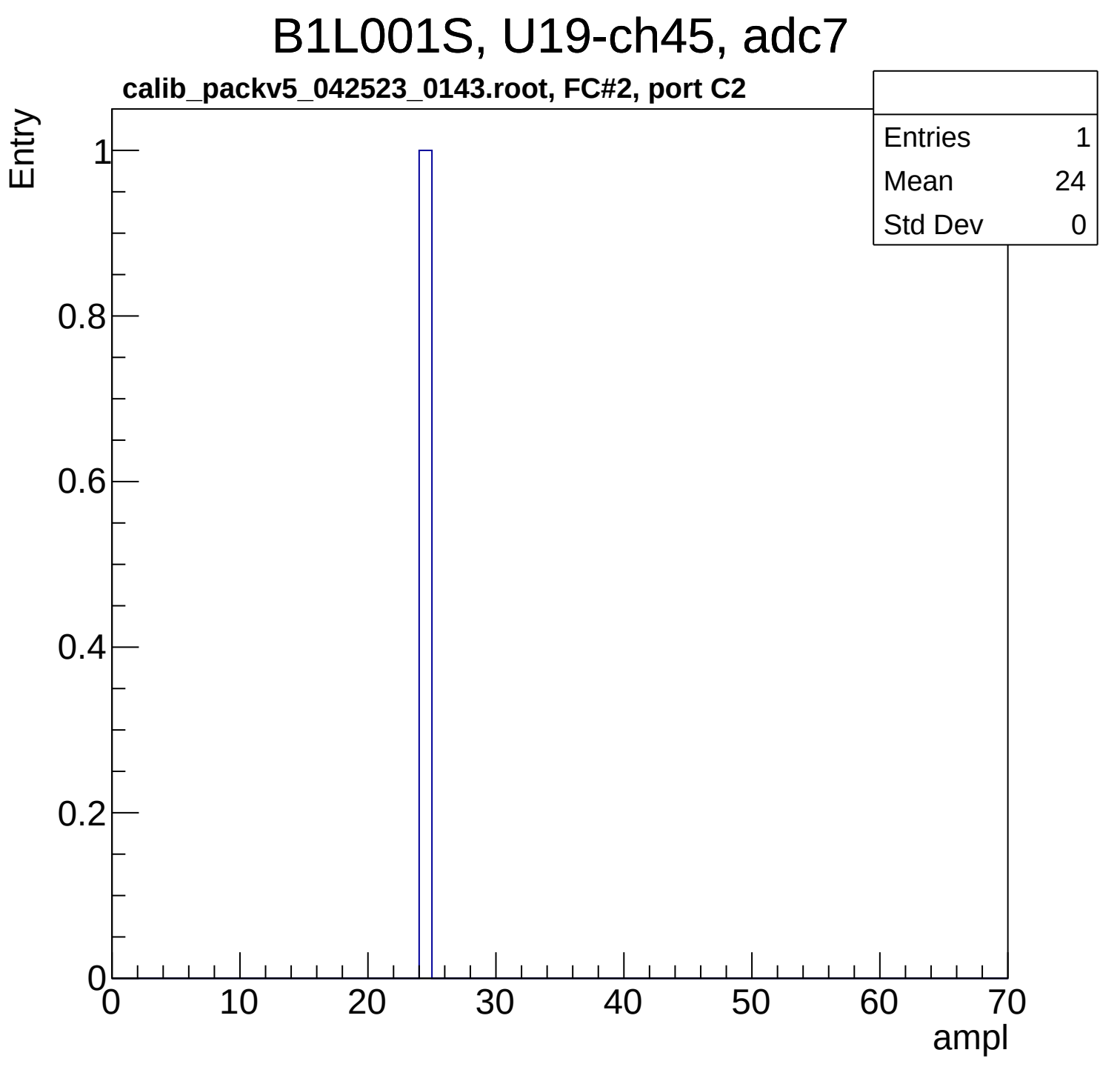

B1L001S, U19-ch45, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 12
Mean 61.75
Std Dev 1.362
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L001S, U19-ch45, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 24
Std Dev 0
Entry
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0.6
0.4
0.2
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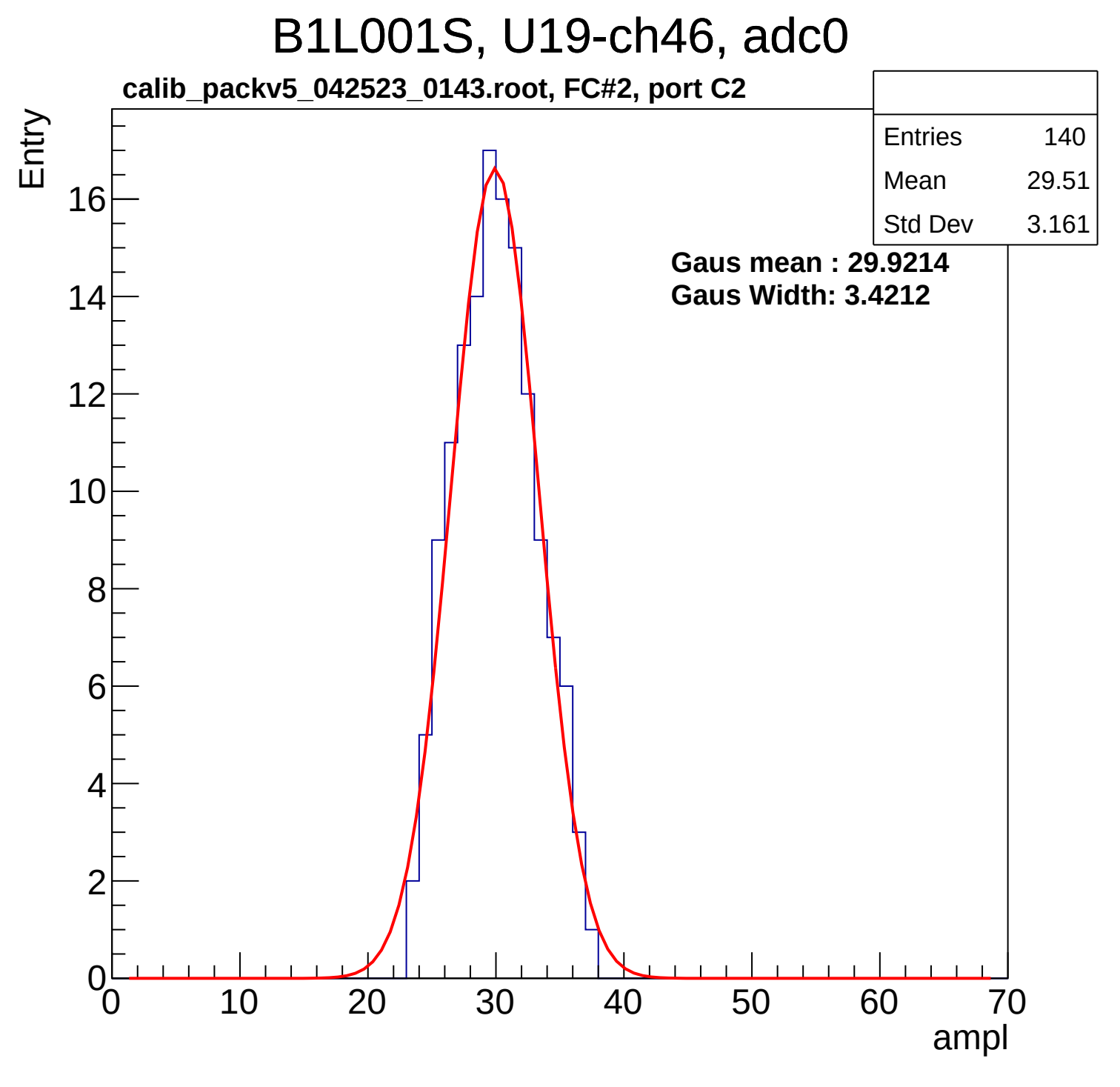
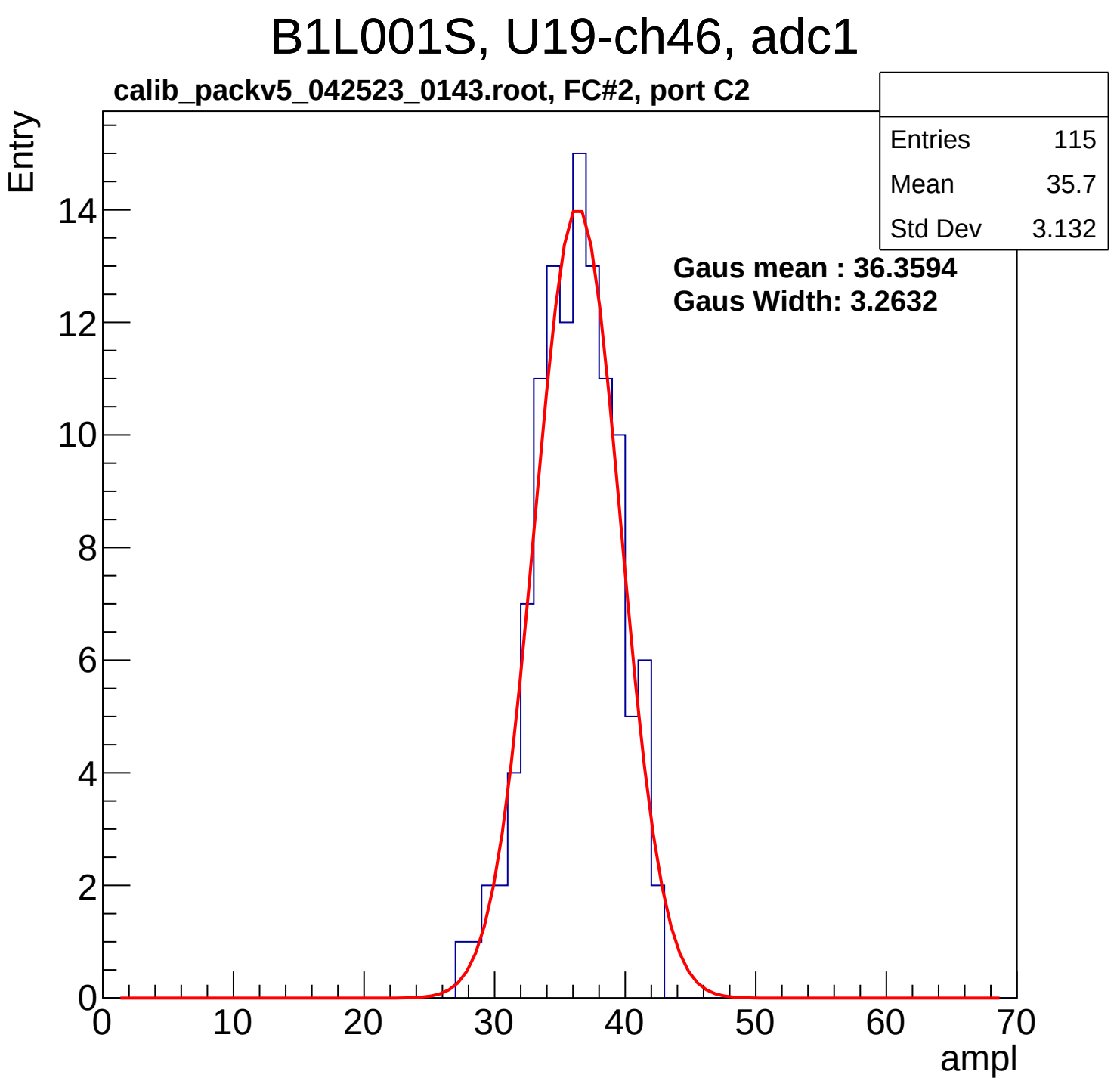
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch46, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 140
Mean 29.51
Std Dev 3.161
Gaus mean : 29.9214
Gaus Width: 3.4212
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70


B1L001S, U19-ch46, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 115
Mean 35.7
Std Dev 3.132
Gaus mean : 36.3594
Gaus Width: 3.2632
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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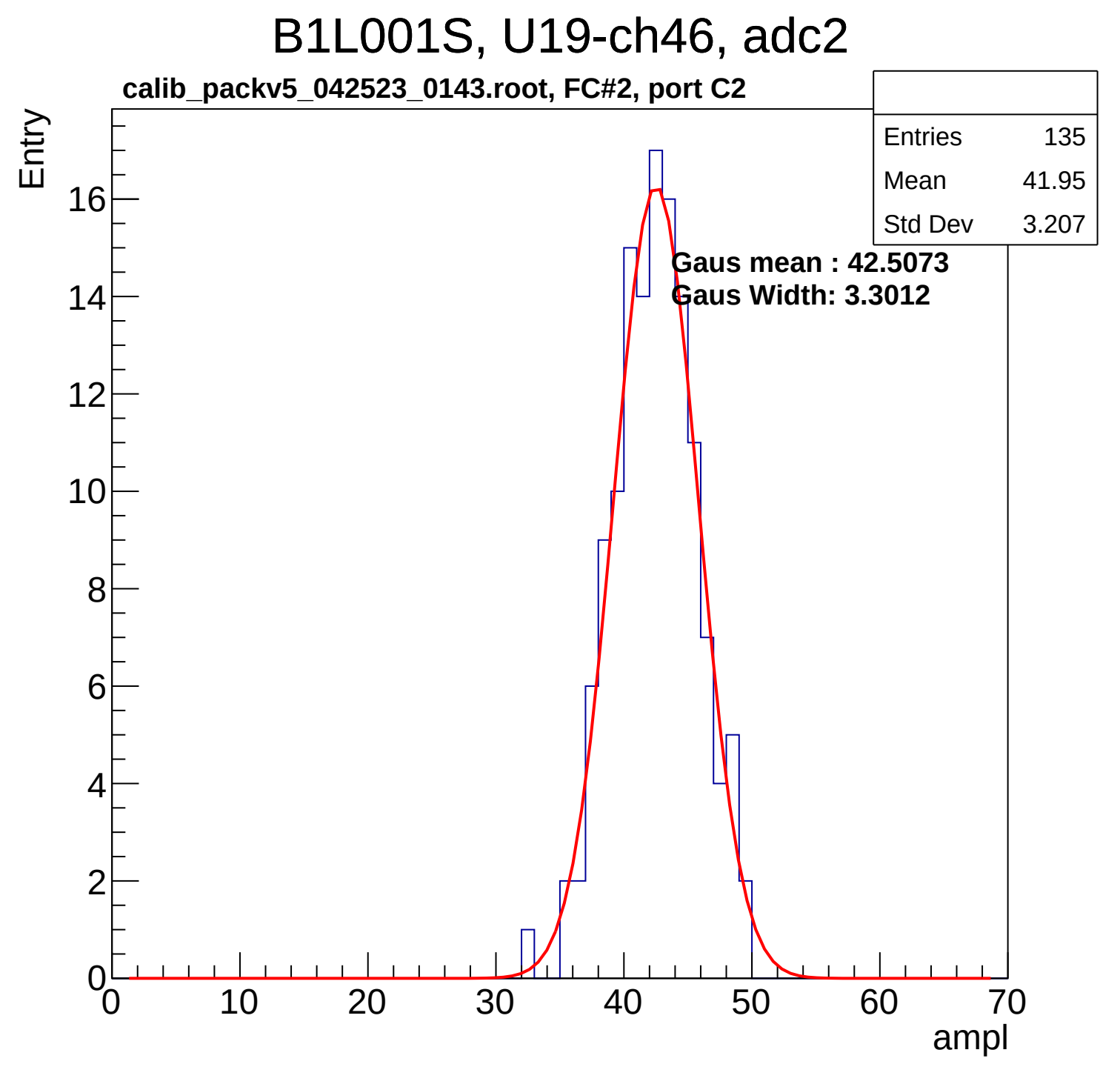
B1L001S, U19-ch46, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 135
Mean 41.95
Std Dev 3.207
Gaus mean : 42.5073
Gaus Width: 3.3012
Entry
ampl
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4
6
8
10
12
14
16
0
10
20
30
40
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60
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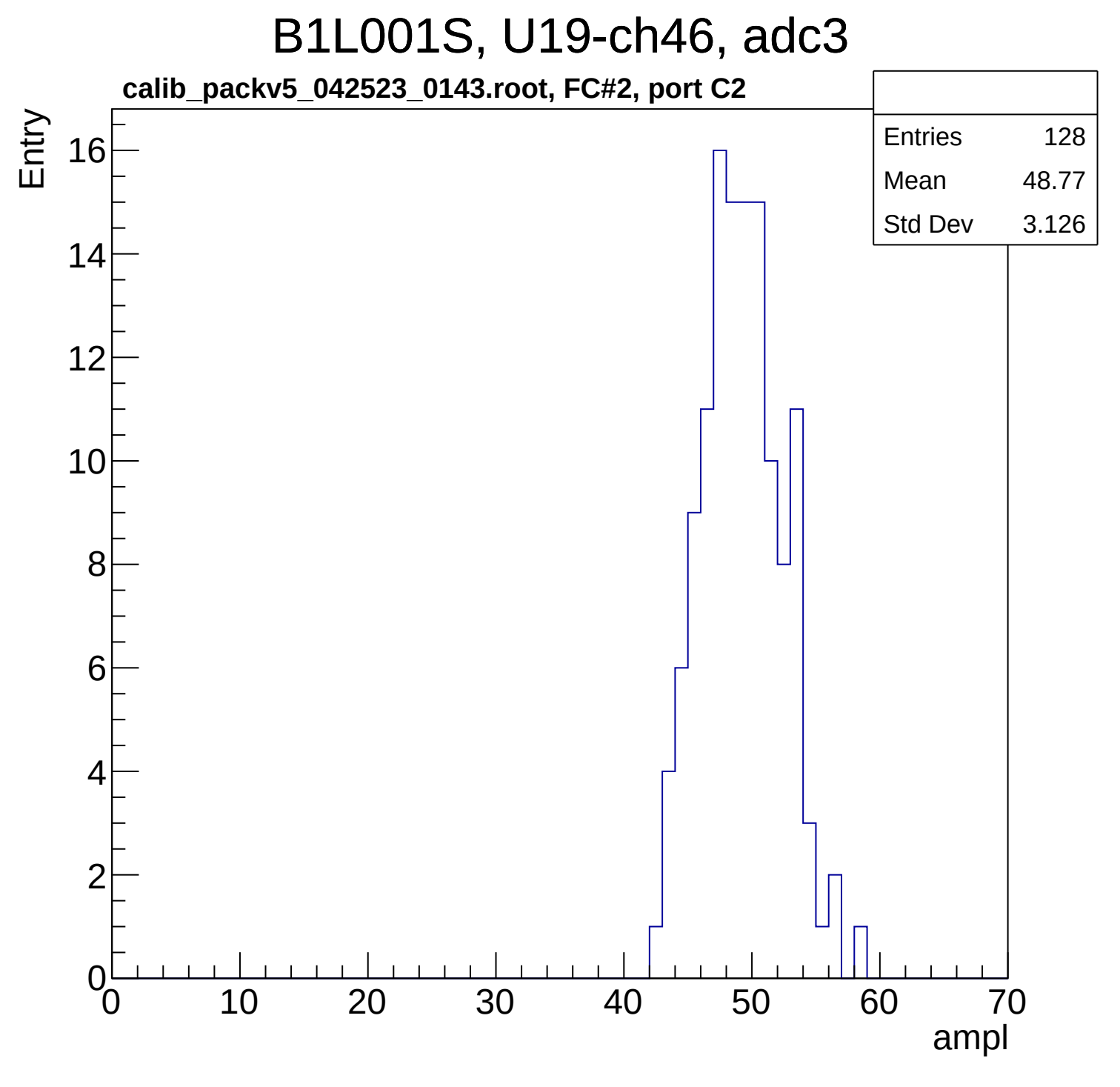
B1L001S, U19-ch46, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 128
Mean 48.77
Std Dev 3.126
Entry
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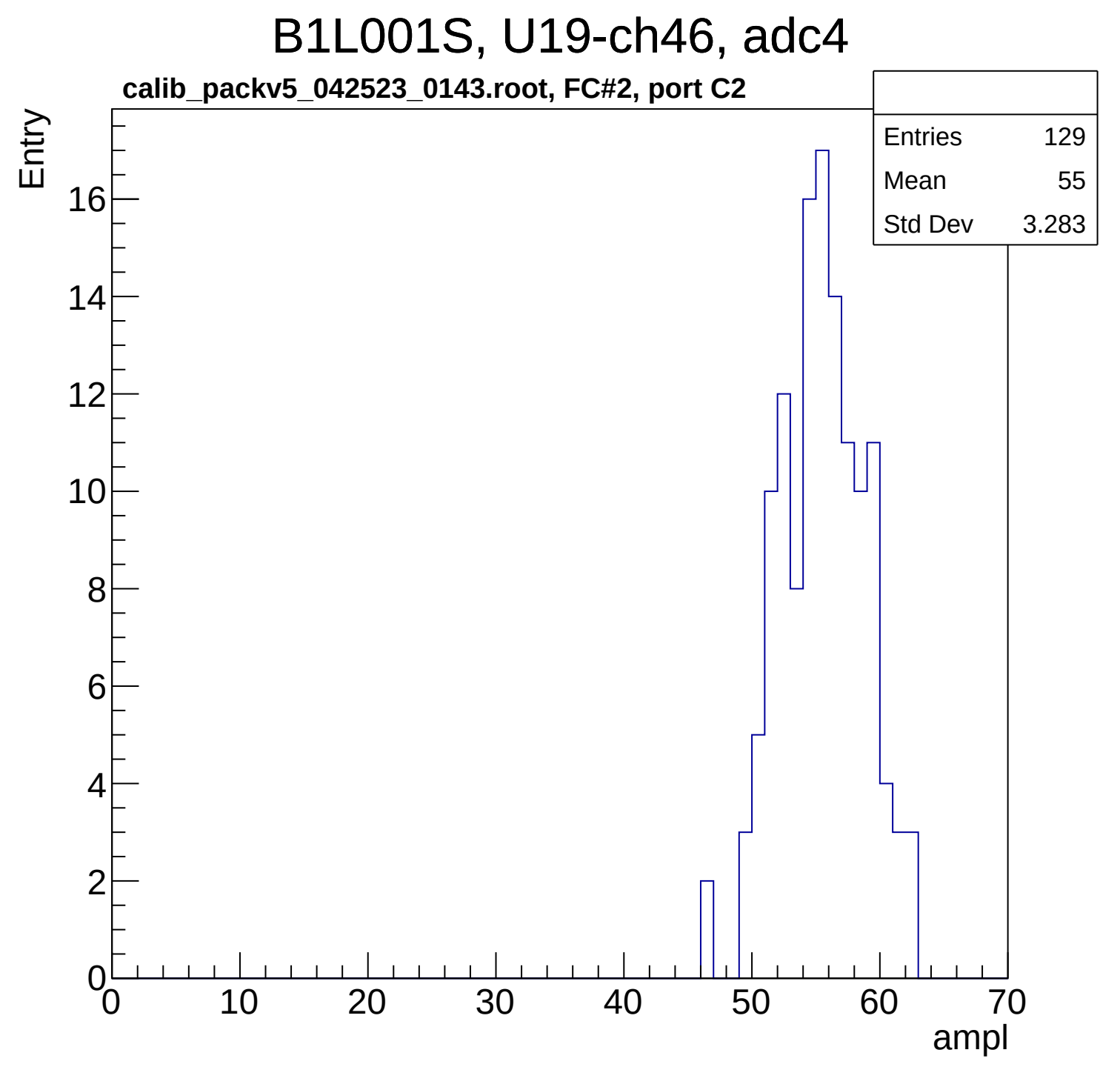
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch46, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 129
Mean 55
Std Dev 3.283
Entry
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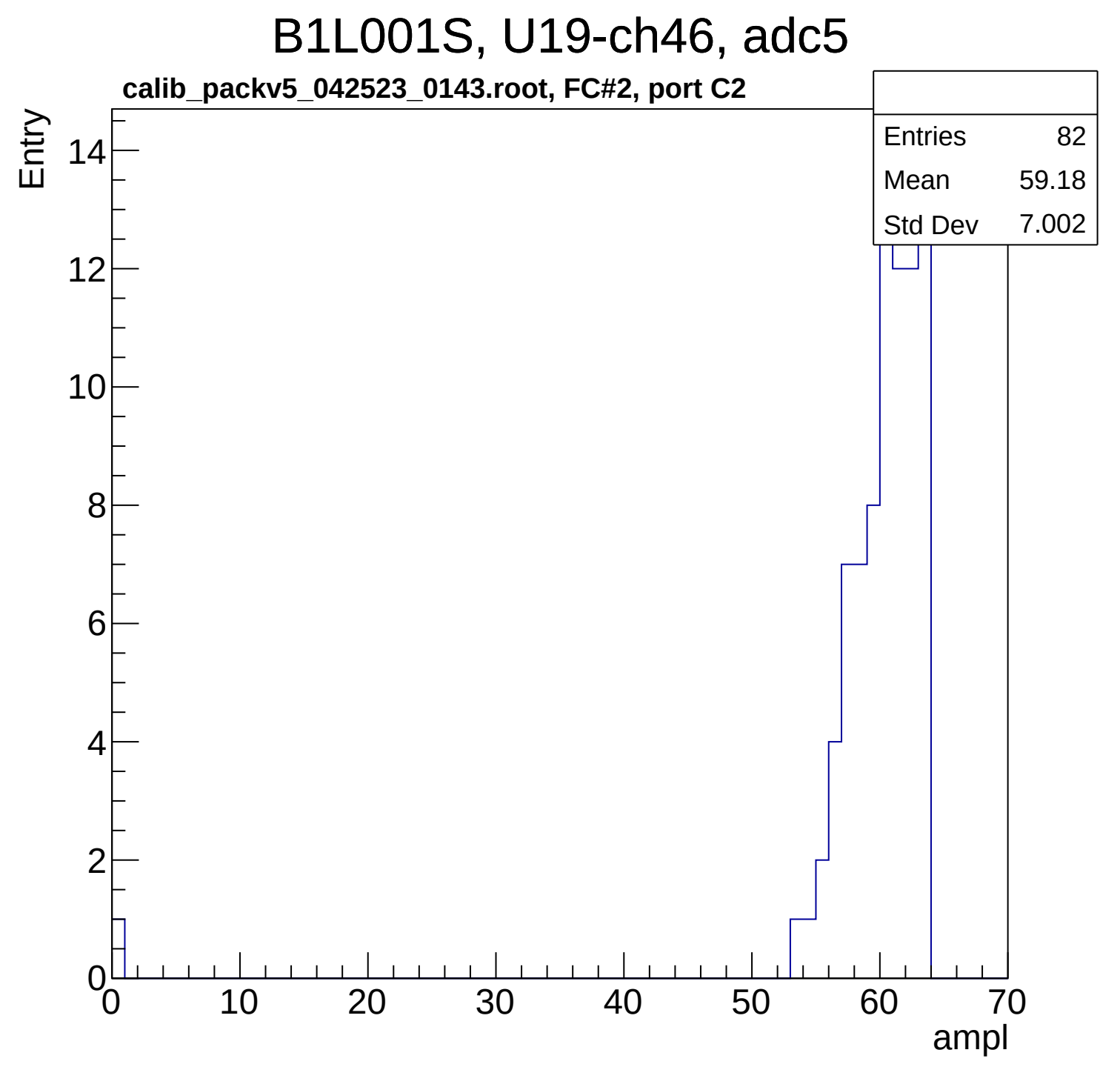
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch46, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 82
Mean 59.18
Std Dev 7.002
Entry
ampl
0
2
4
6
8
10
12
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0
10
20
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40
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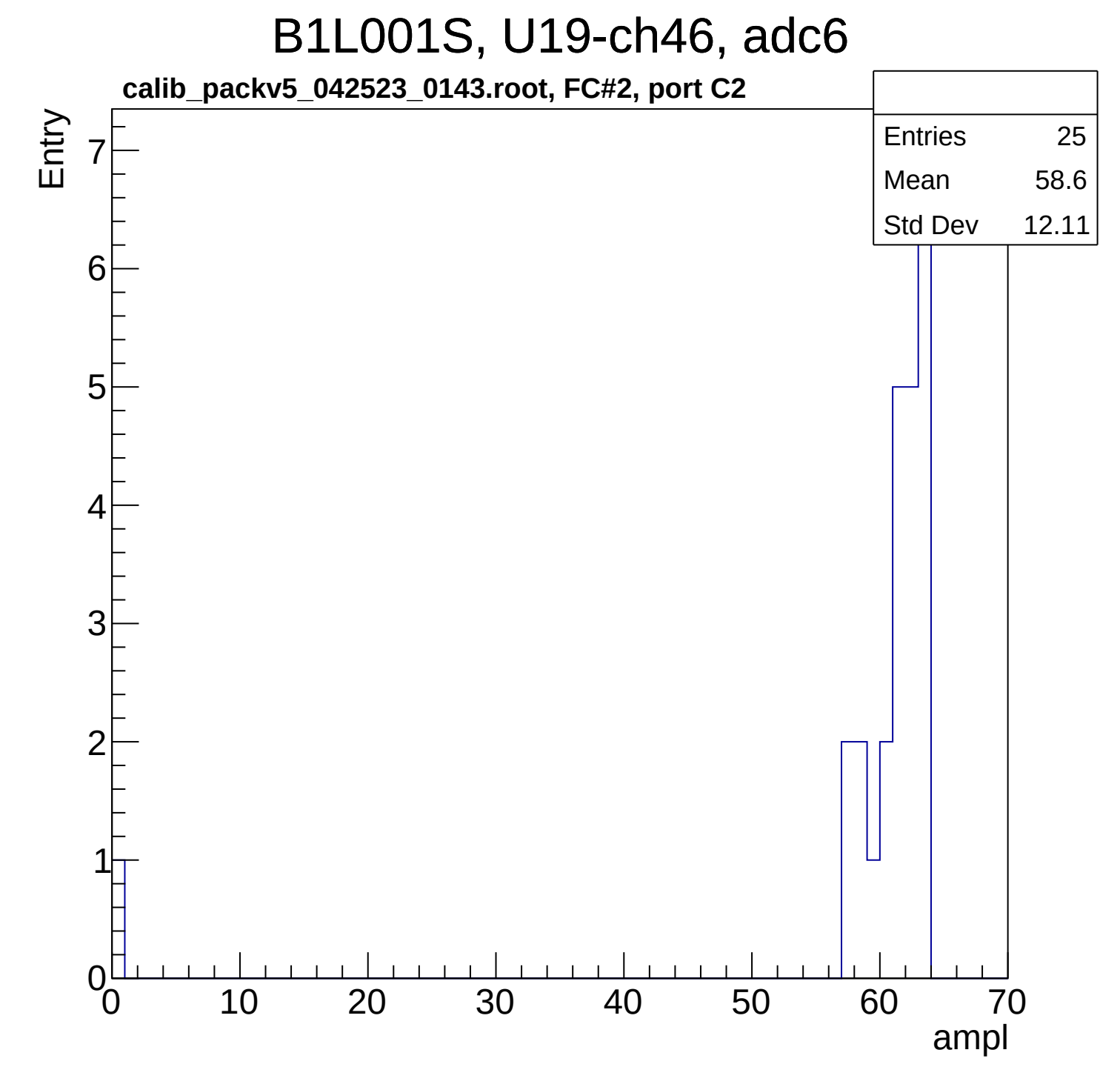
B1L001S, U19-ch46, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 25
Mean 58.6
Std Dev 12.11
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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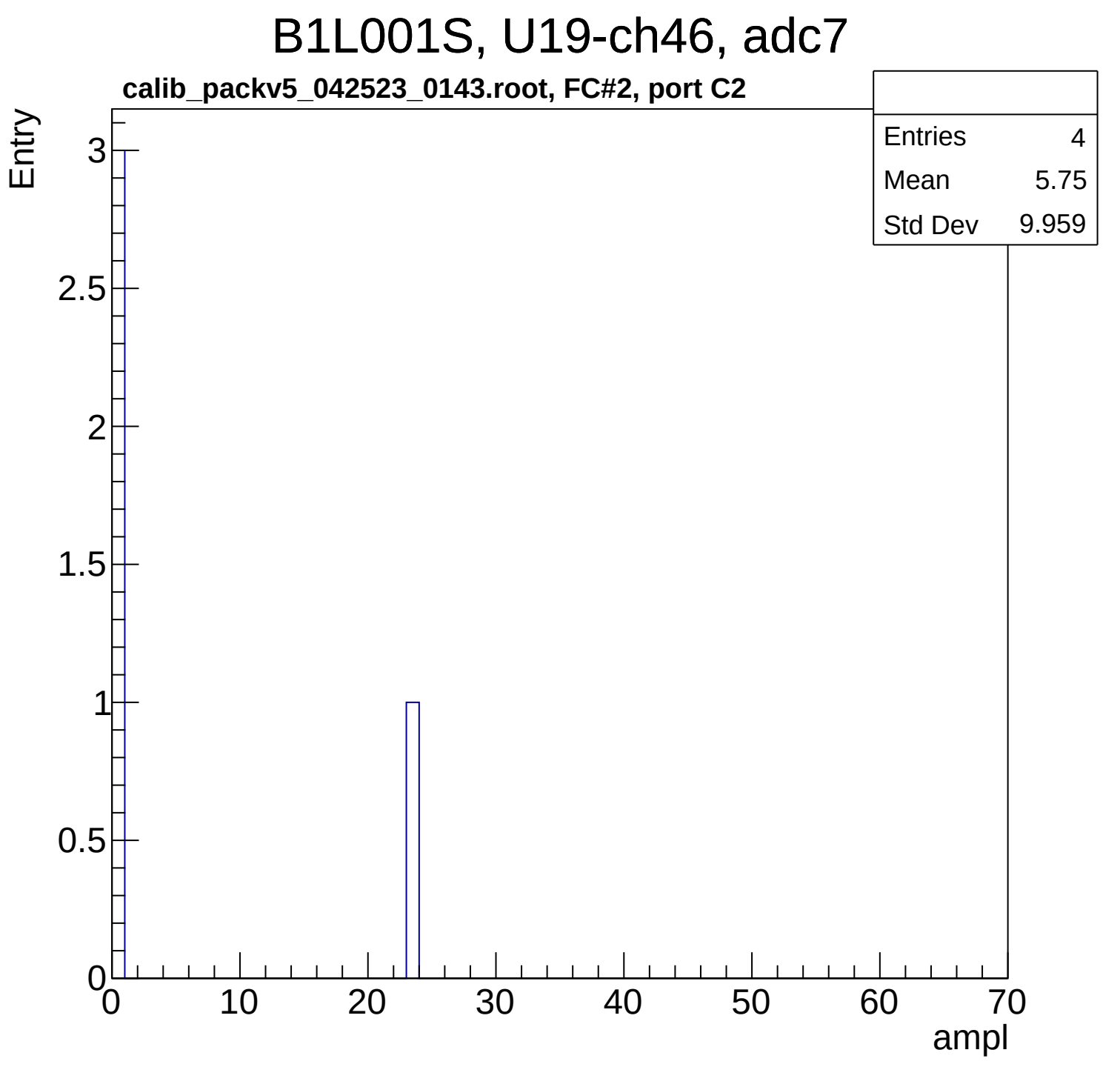
B1L001S, U19-ch46, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 4
Mean 5.75
Std Dev 9.959
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
10
20
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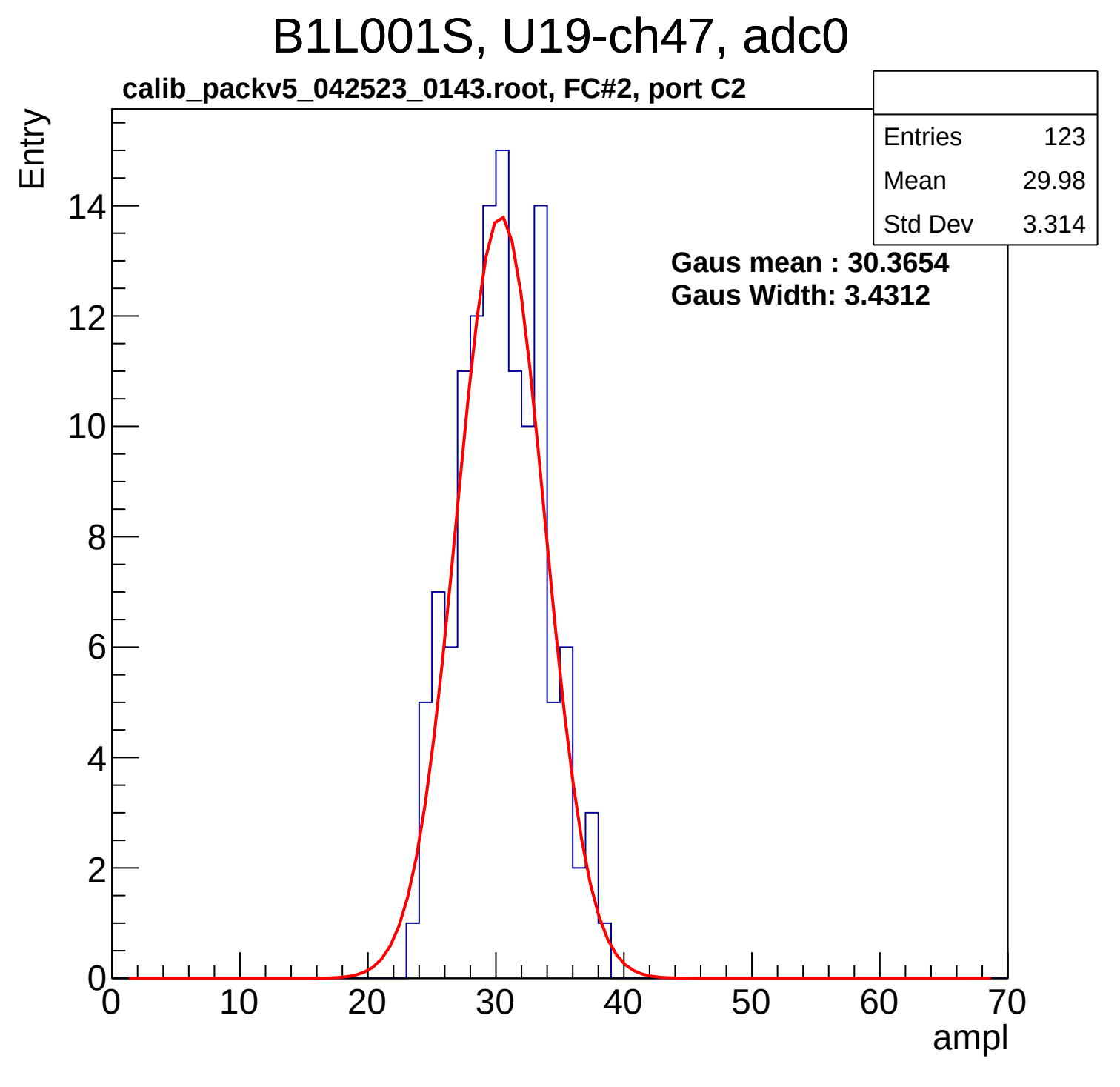
40
50
60
70


B1L001S, U19-ch47, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 123
Mean 29.98
Std Dev 3.314
Gaus mean : 30.3654
Gaus Width: 3.4312
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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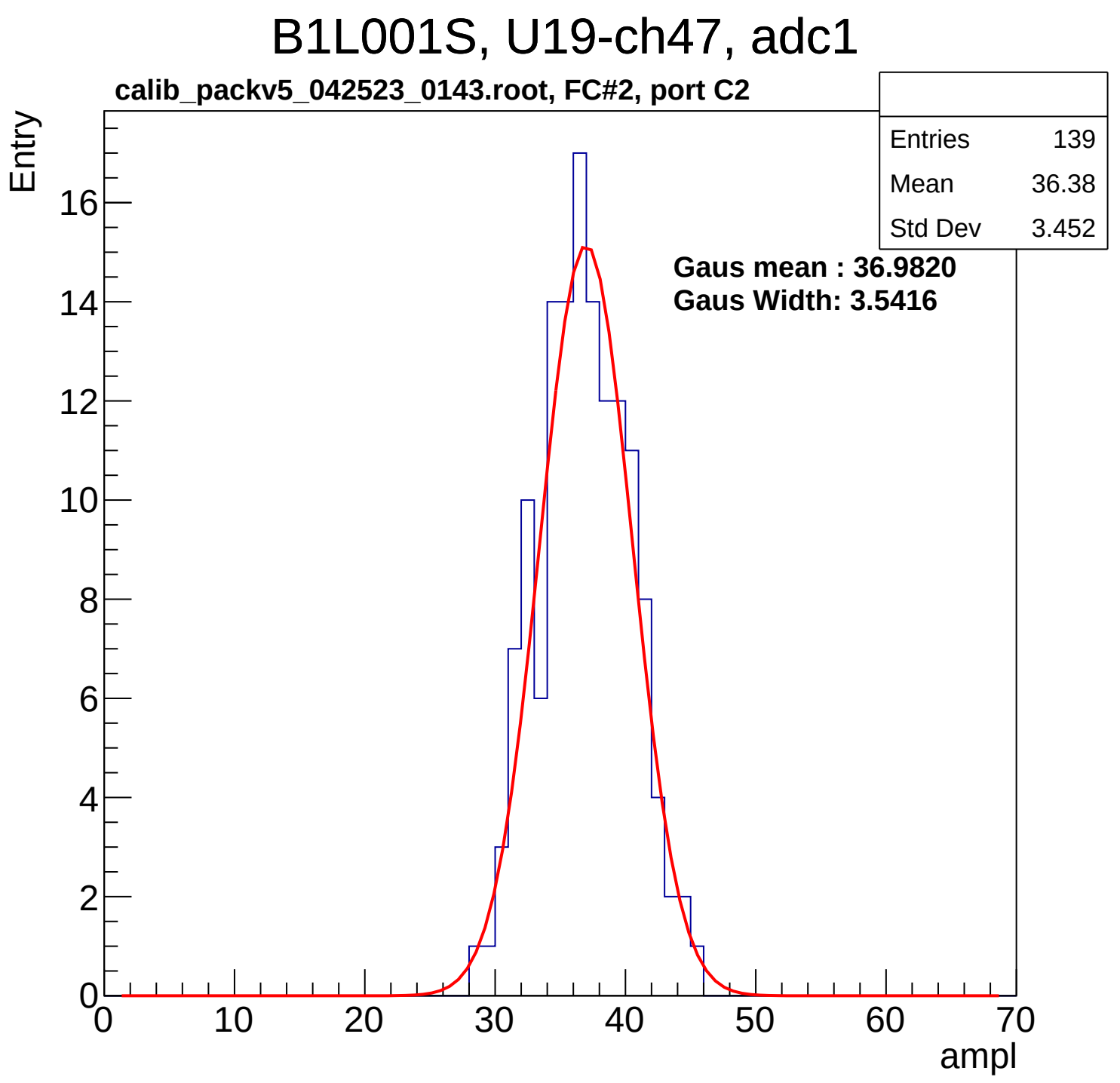
40
50
60
70


B1L001S, U19-ch47, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 139
Mean 36.38
Std Dev 3.452
Gaus mean : 36.9820
Gaus Width: 3.5416
Entry
ampl
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2
4
6
8
10
12
14
16
0
10
20
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40
50
60
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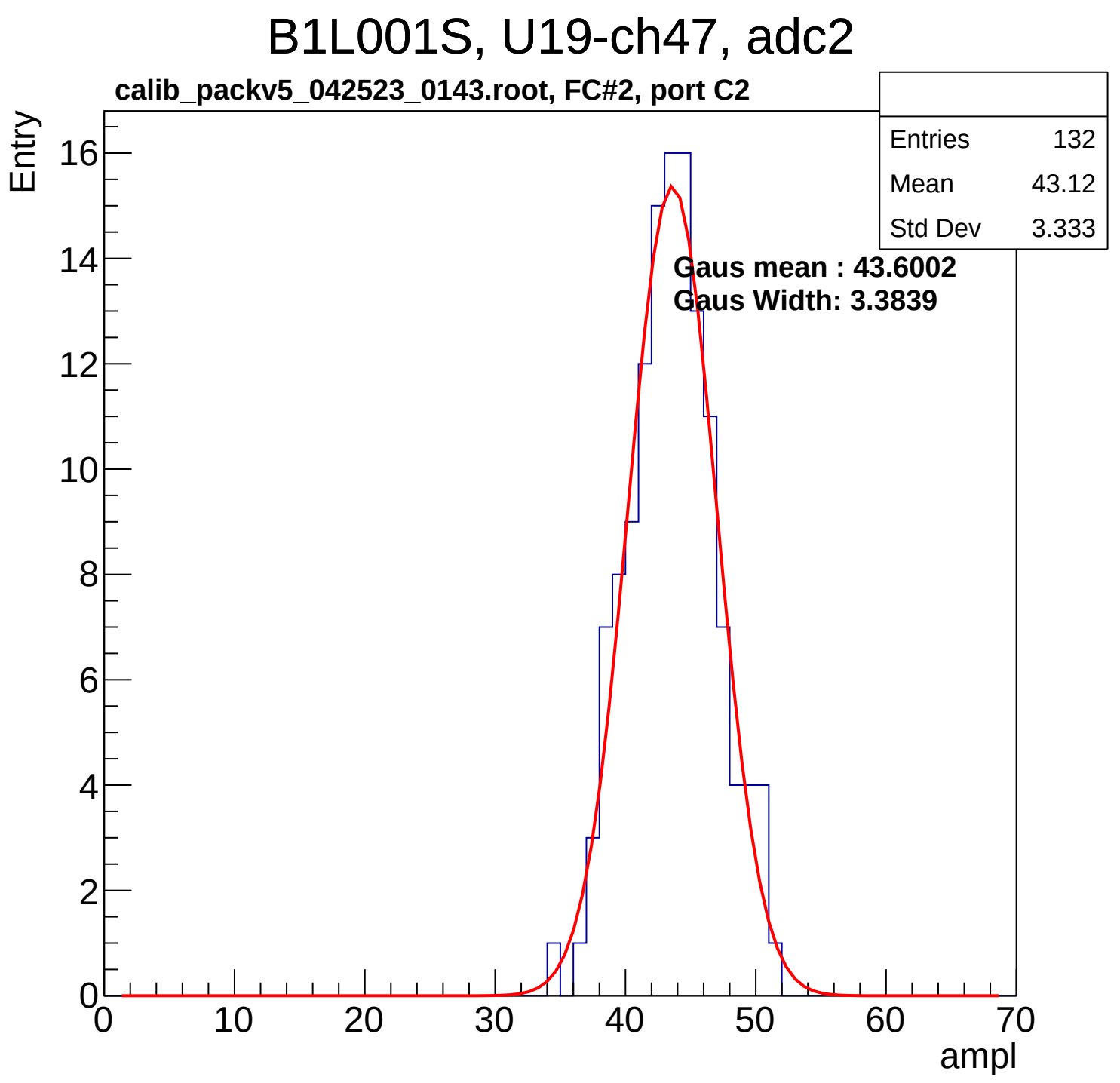
B1L001S, U19-ch47, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 132
Mean 43.12
Std Dev 3.333
Gaus mean : 43.6002
Gaus Width: 3.3839
Entry
ampl
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4
6
8
10
12
14
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0
10
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40
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60
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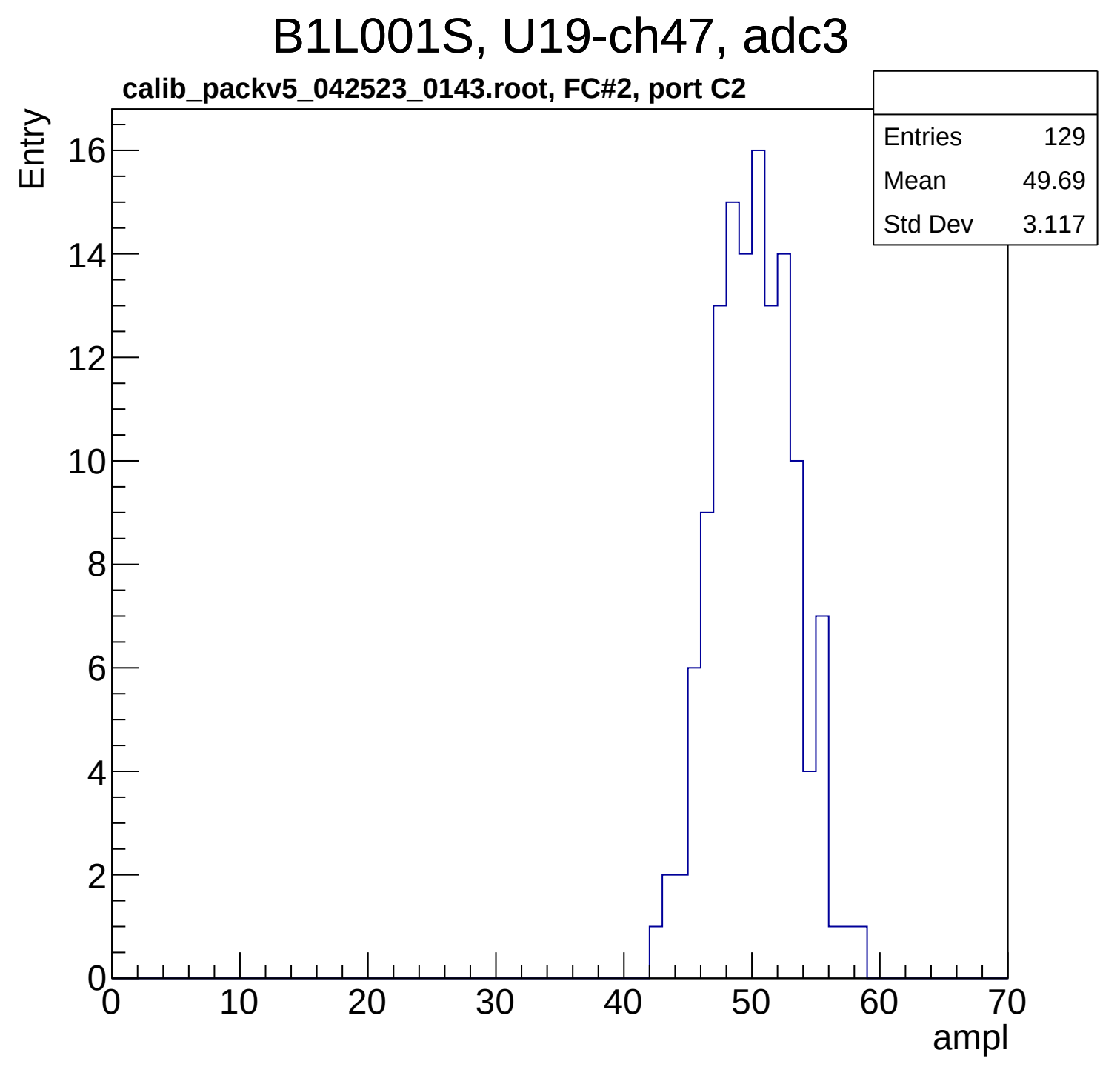
B1L001S, U19-ch47, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 129
Mean 49.69
Std Dev 3.117
Entry
ampl
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10
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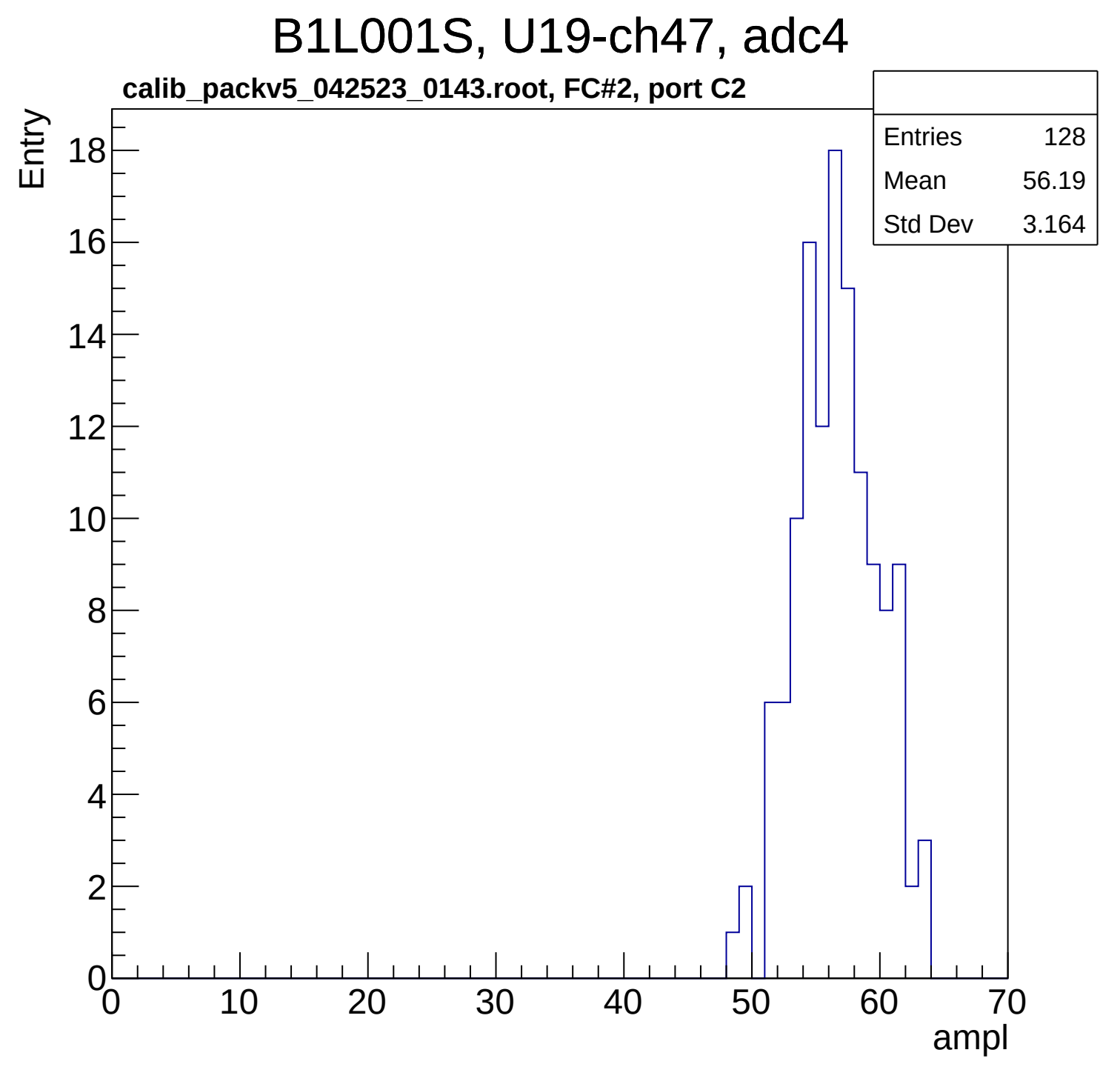
B1L001S, U19-ch47, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 128
Mean 56.19
Std Dev 3.164
Entry
ampl
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4
6
8
10
12
14
16
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0
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40
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60
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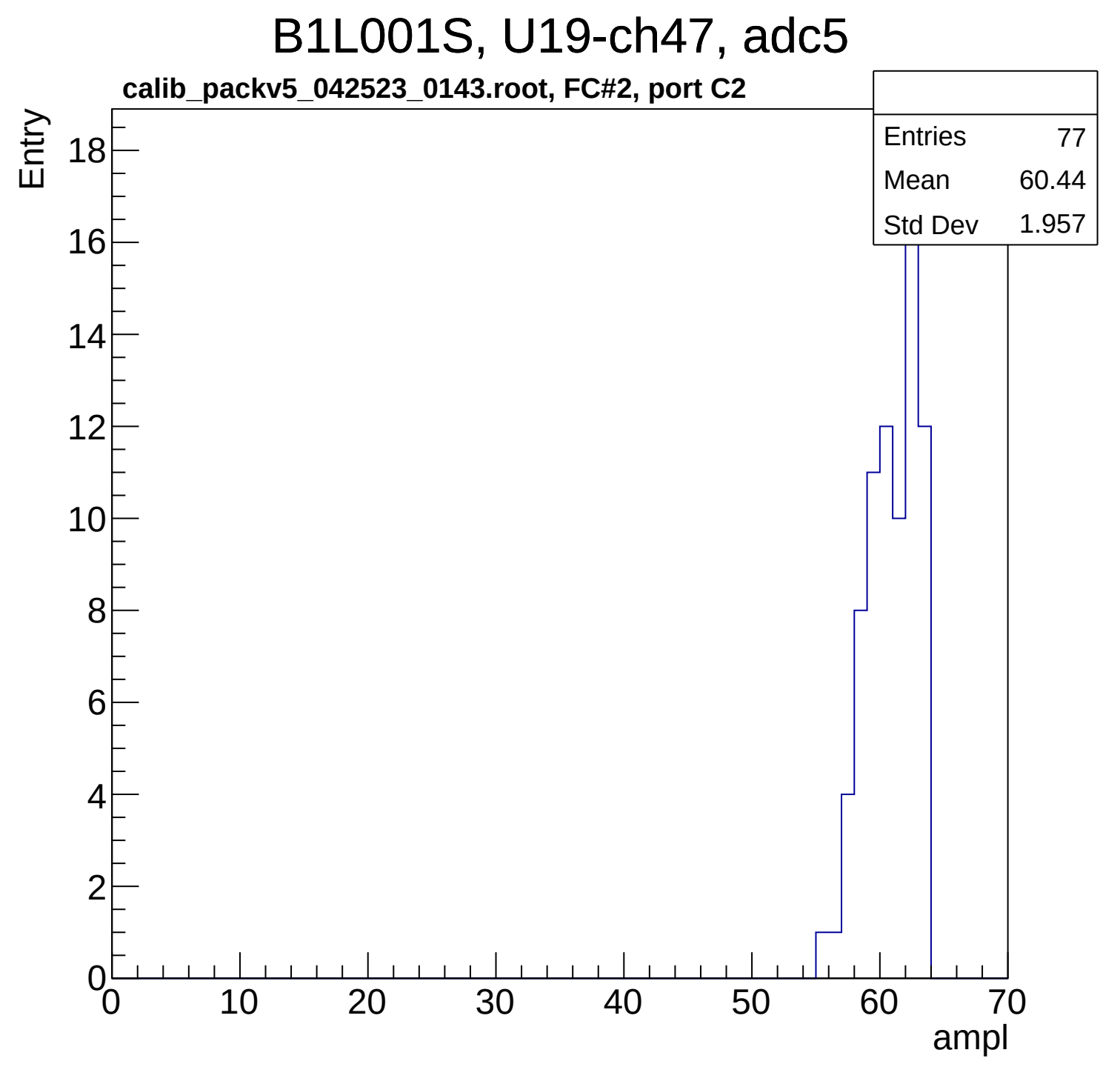
B1L001S, U19-ch47, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 77
Mean 60.44
Std Dev 1.957
Entry
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6
8
10
12
14
16
18
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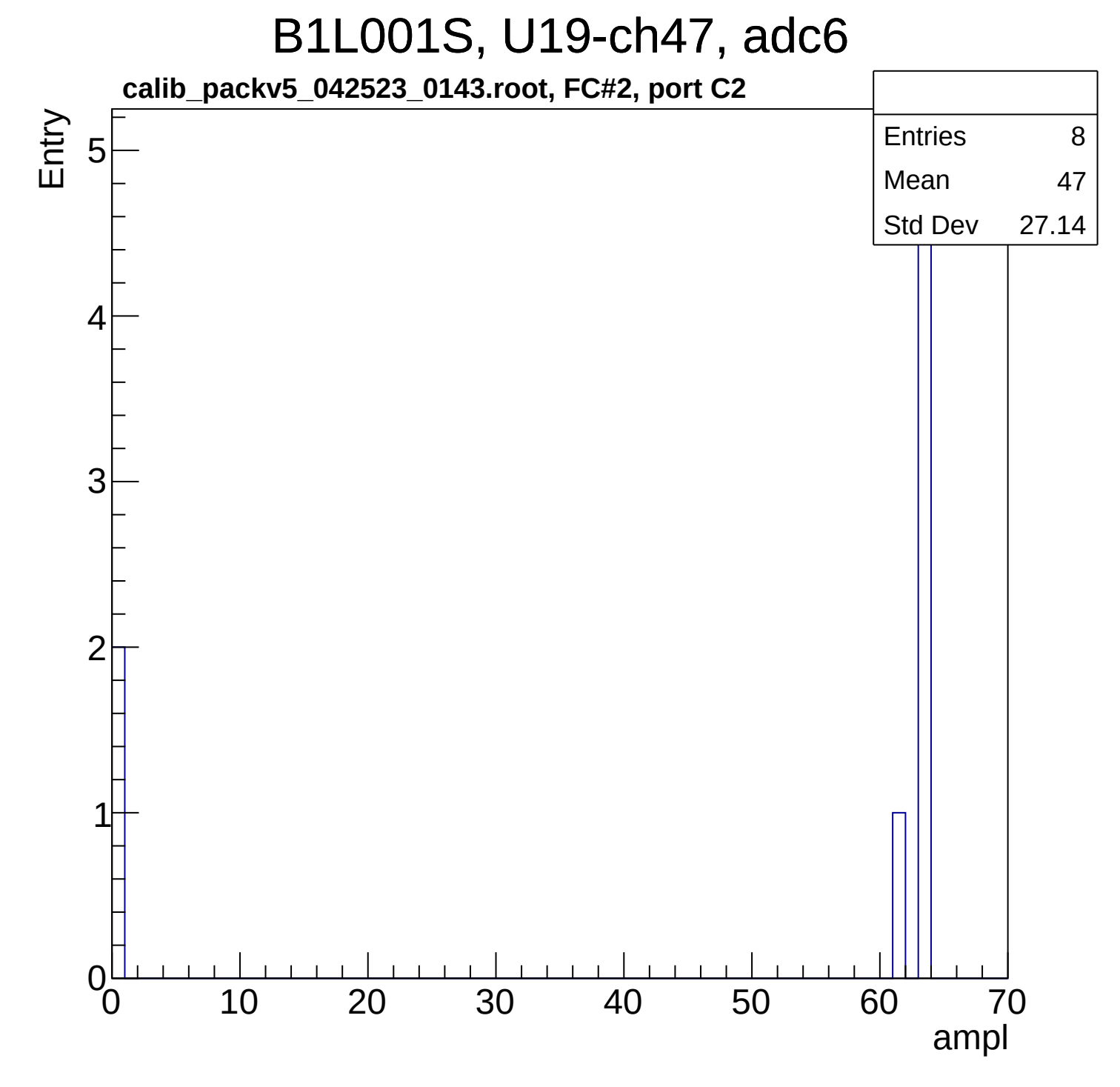
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch47, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 8
Mean 47
Std Dev 27.14
Entry
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1
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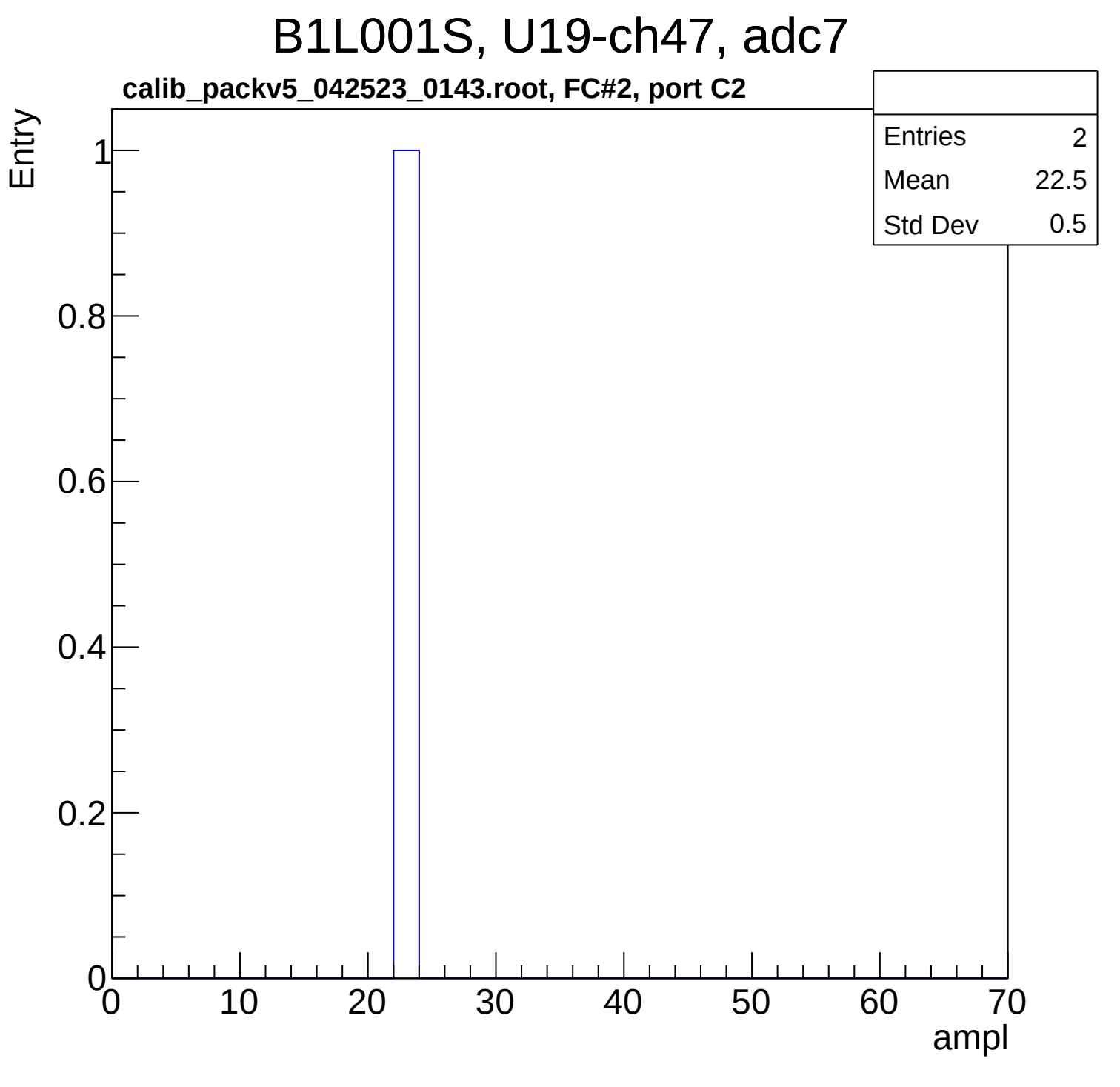
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch47, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 22.5
Std Dev 0.5
Entry
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0.6
0.4
0.2
0
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10
20
30
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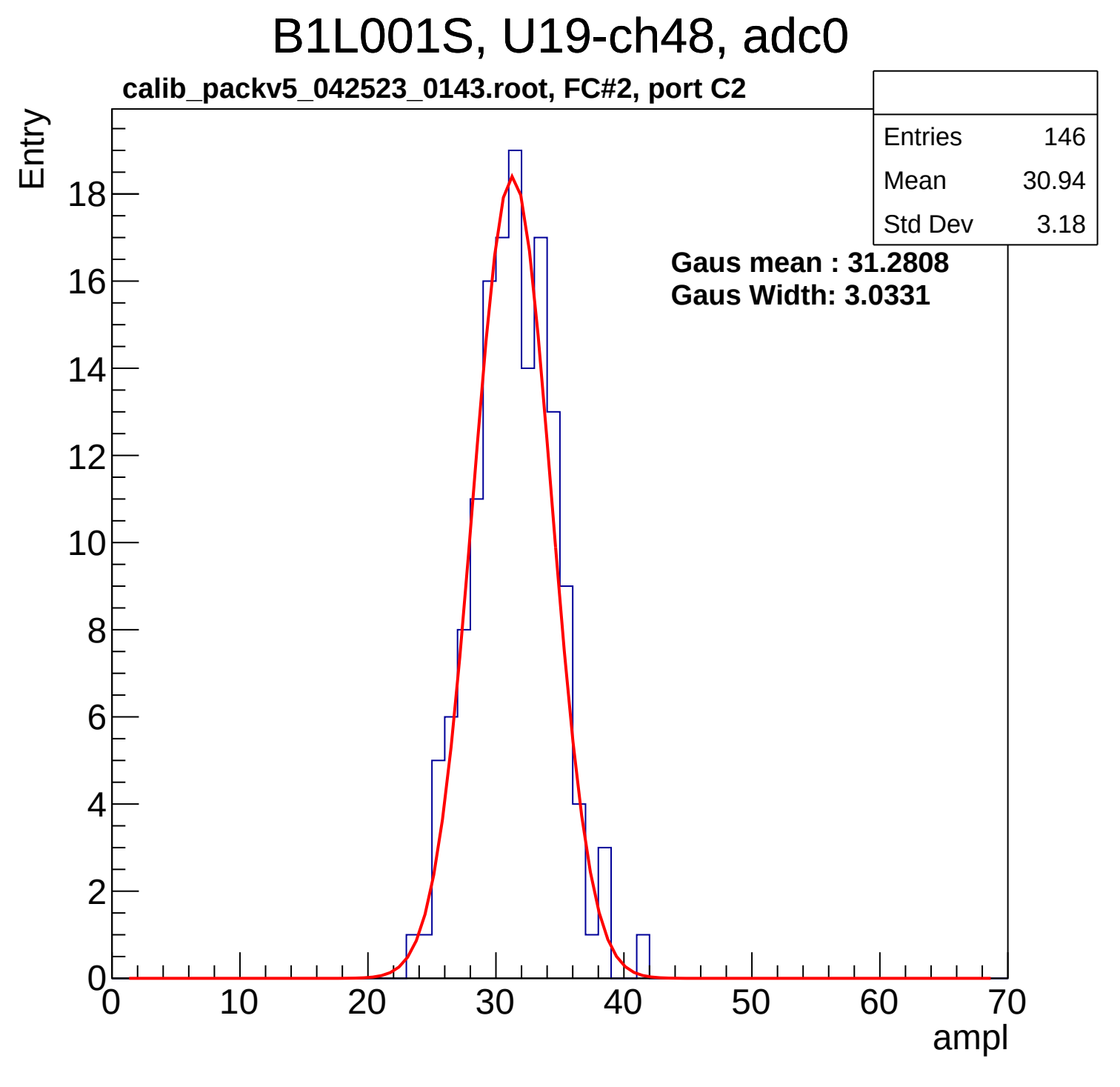
50
60
70
ampl


B1L001S, U19-ch48, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 146
Mean 30.94
Std Dev 3.18
Gaus mean : 31.2808
Gaus Width: 3.0331
Entry
ampl
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4
6
8
10
12
14
16
18
0
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20
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40
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60
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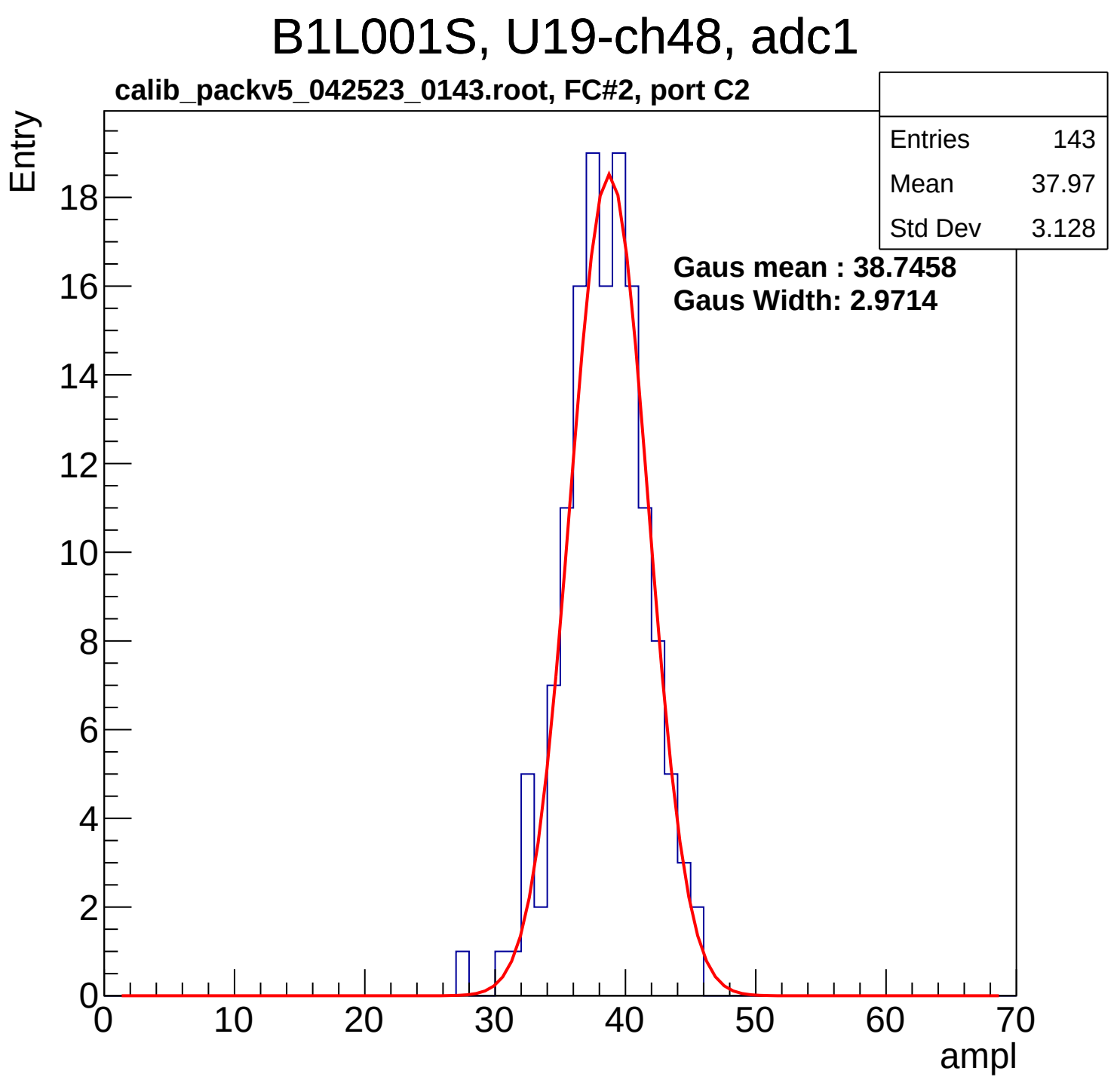
B1L001S, U19-ch48, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 143
Mean 37.97
Std Dev 3.128
Gaus mean : 38.7458
Gaus Width: 2.9714
Entry
ampl
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2
4
6
8
10
12
14
16
18
0
10
20
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40
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60
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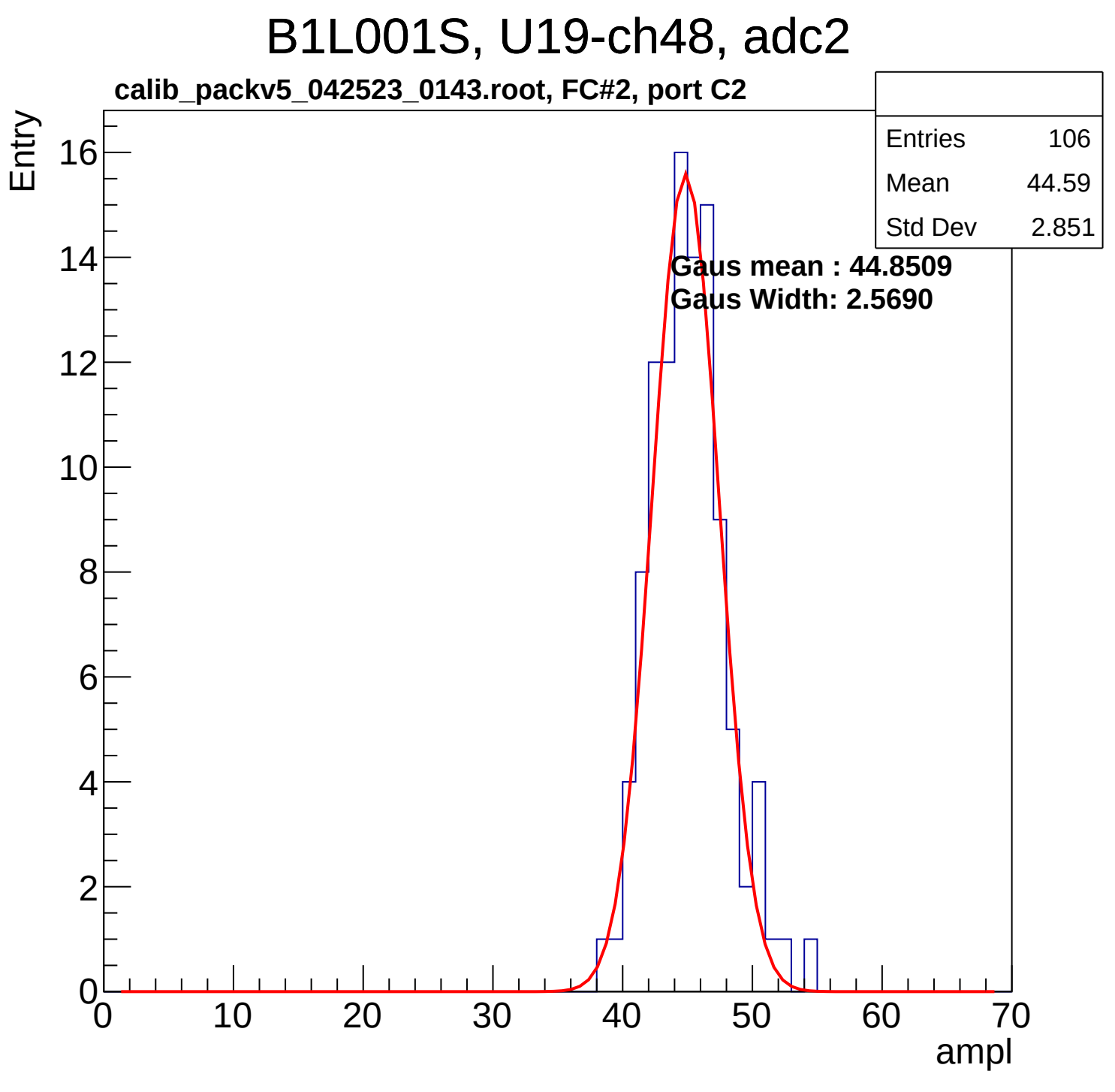
B1L001S, U19-ch48, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 106
Mean 44.59
Std Dev 2.851
Gaus mean : 44.8509
Gaus Width: 2.5690
Entry
ampl
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2
4
6
8
10
12
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0
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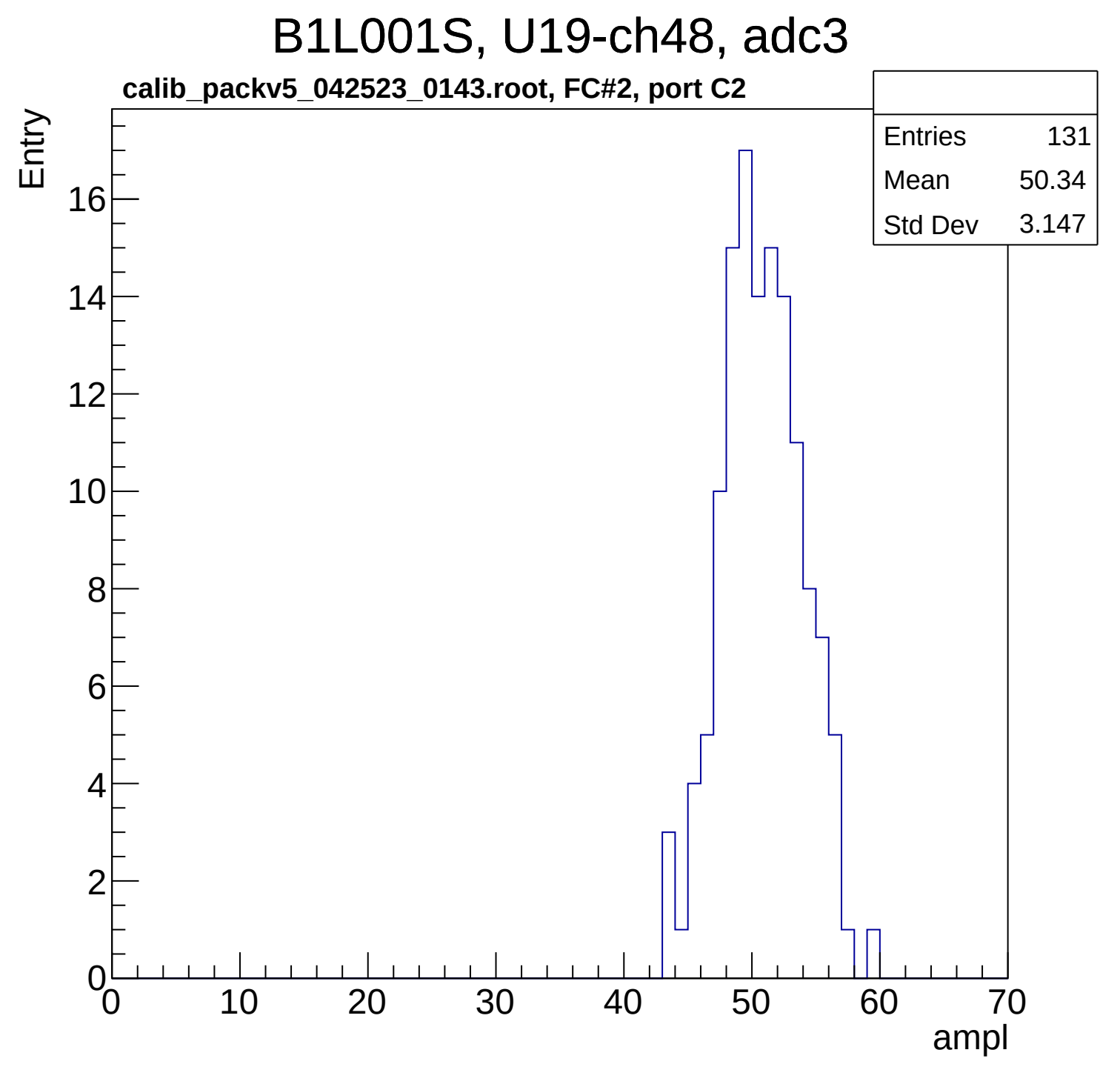
B1L001S, U19-ch48, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 131
Mean 50.34
Std Dev 3.147
Entry
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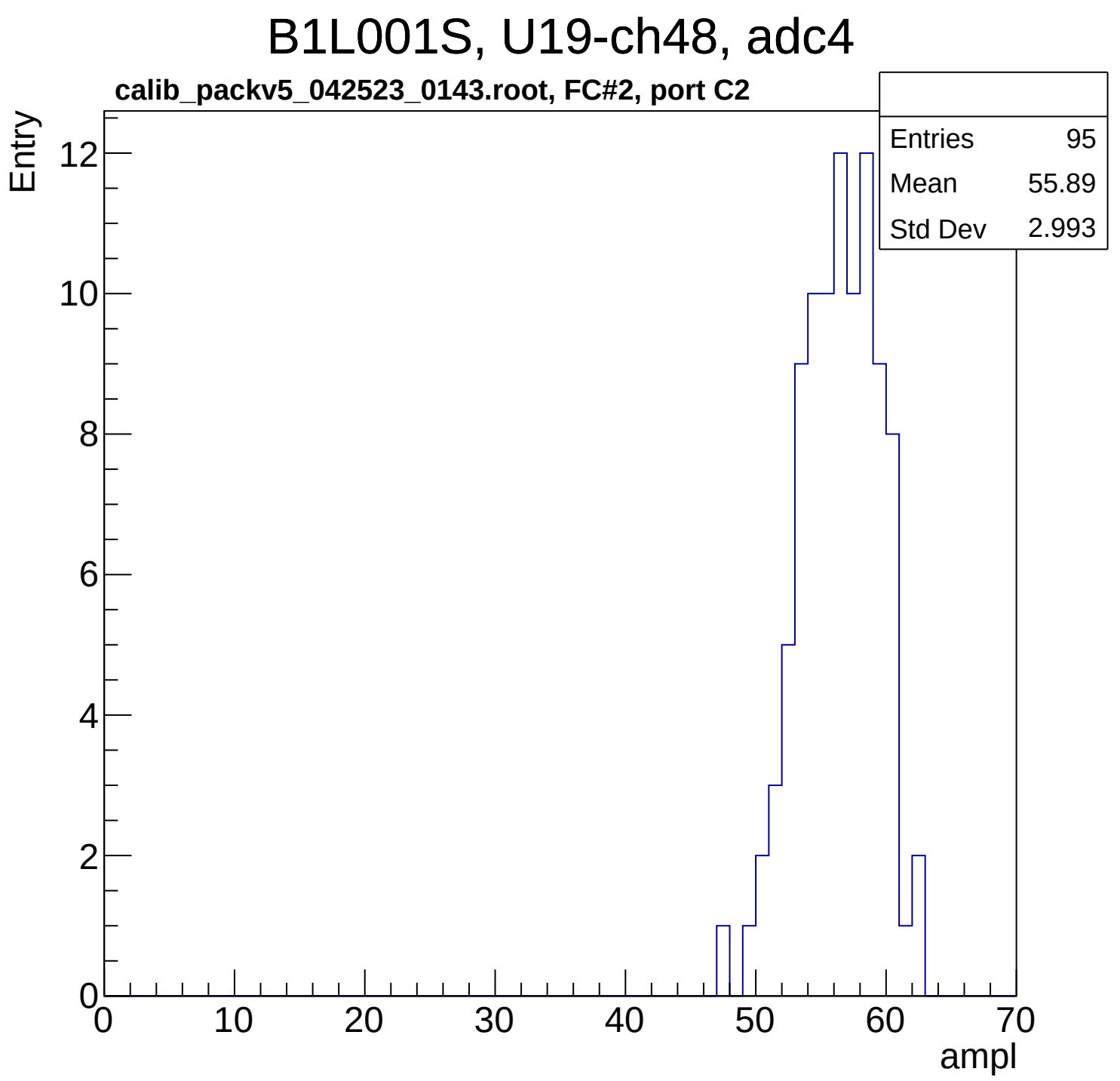
50
60
70
ampl


B1L001S, U19-ch48, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 95
Mean 55.89
Std Dev 2.993
Entry
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10
20
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40
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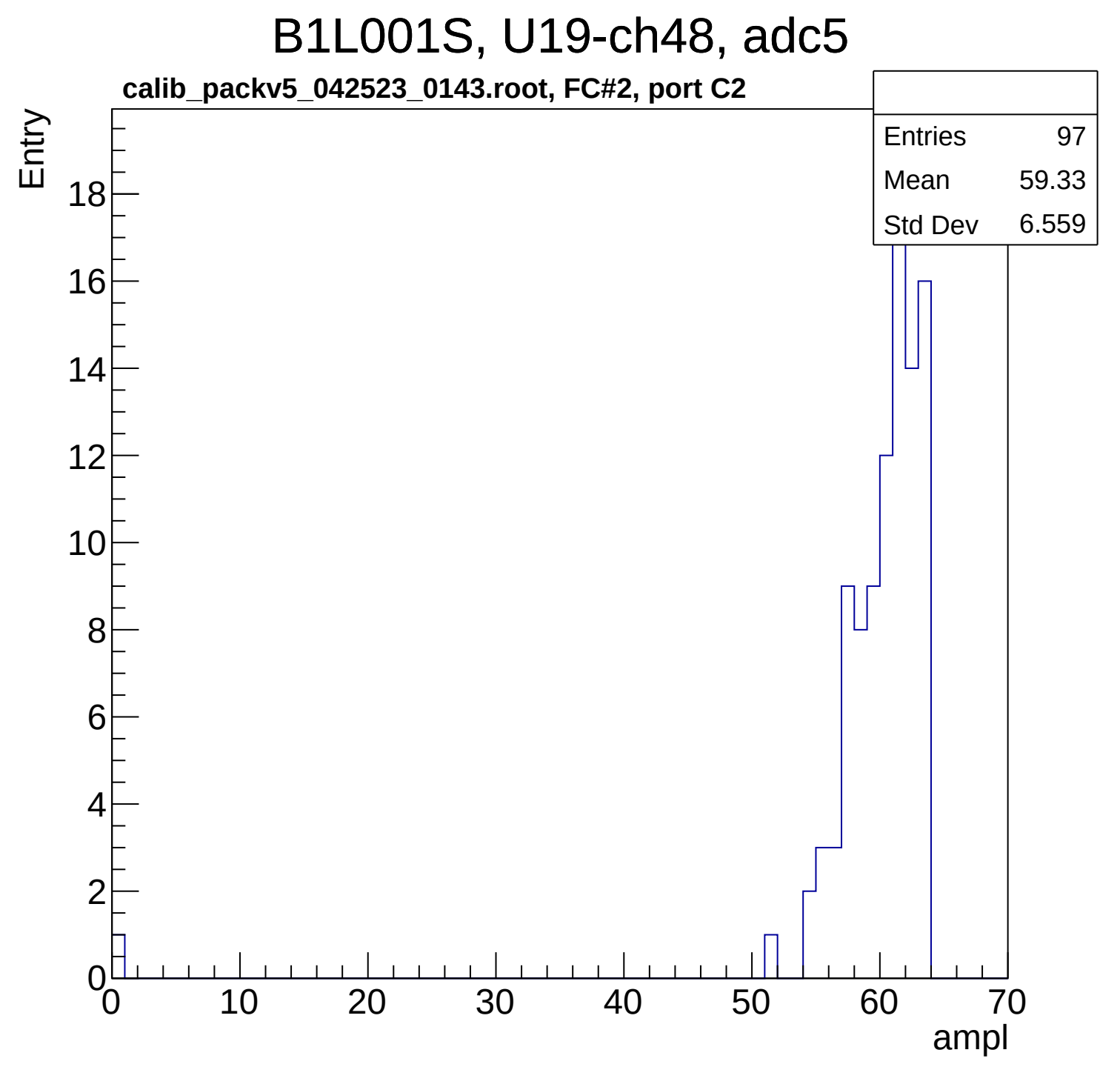
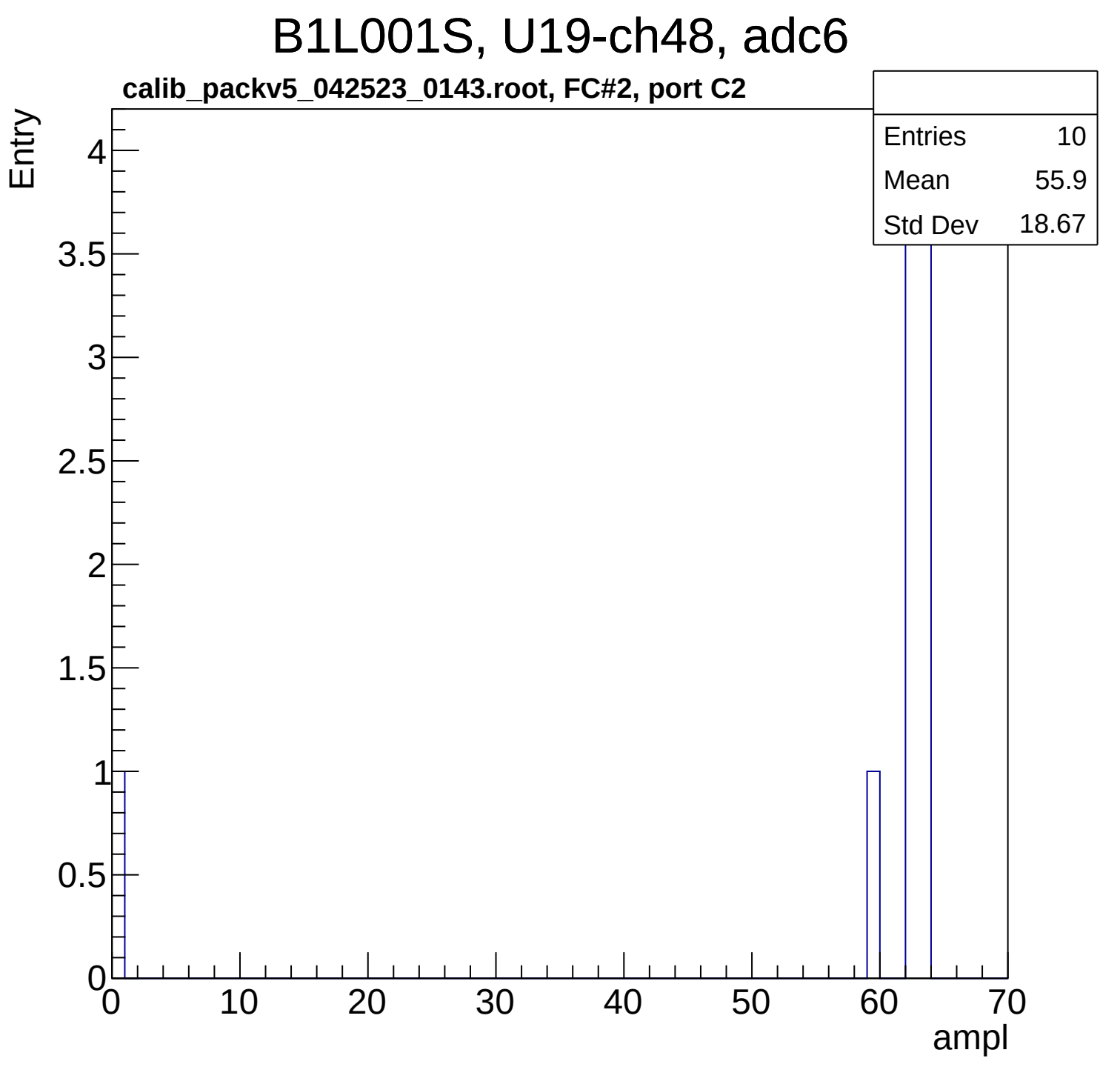
60
70
ampl


B1L001S, U19-ch48, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 97
Mean 59.33
Std Dev 6.559
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70


B1L001S, U19-ch48, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 10
Mean 55.9
Std Dev 18.67
Entry
ampl
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0.5
1
1.5
2
2.5
3
3.5
4
0
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60
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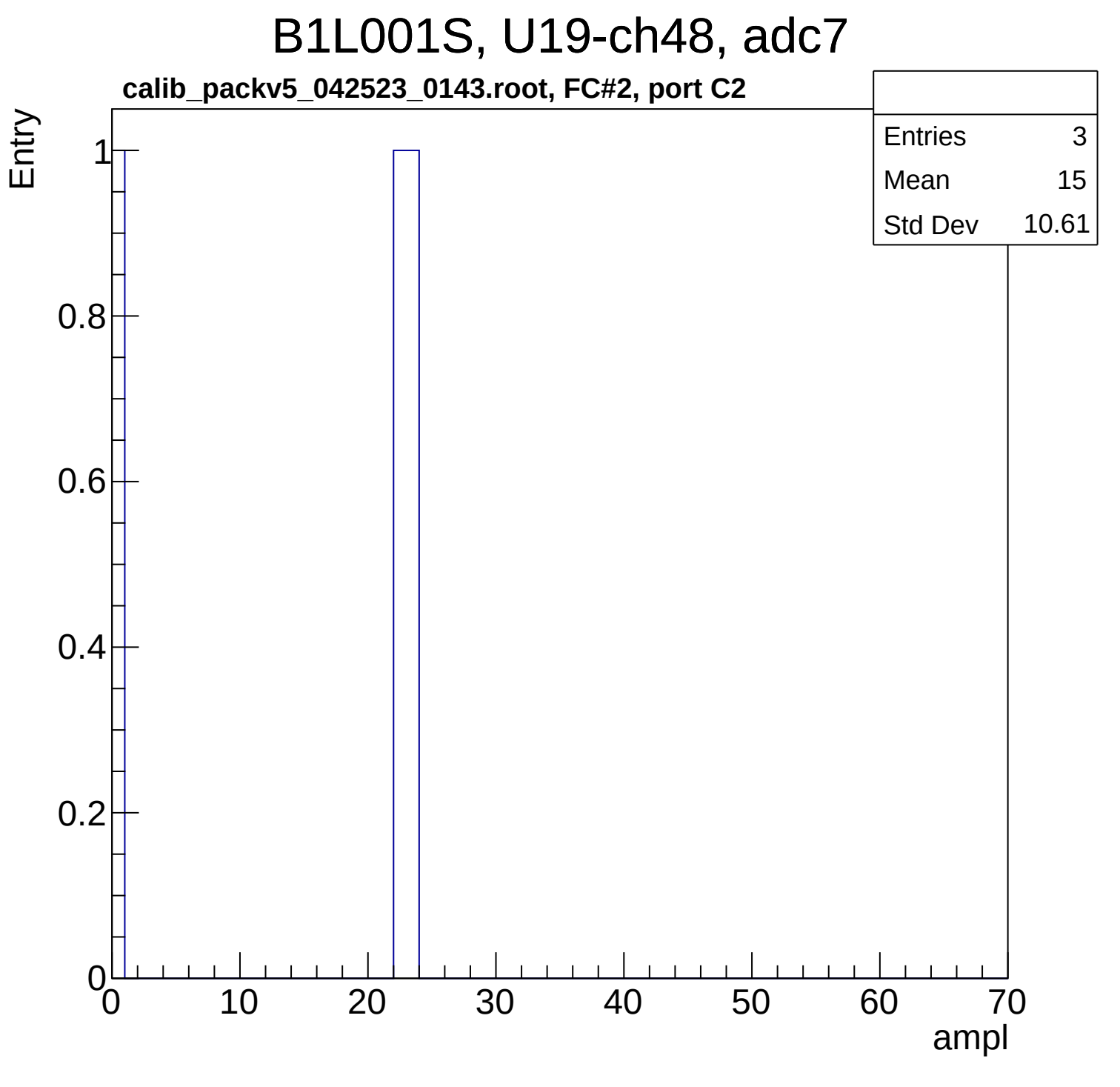
B1L001S, U19-ch48, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 3
Mean 15
Std Dev 10.61
Entry
ampl
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0.2
0.4
0.6
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1
0
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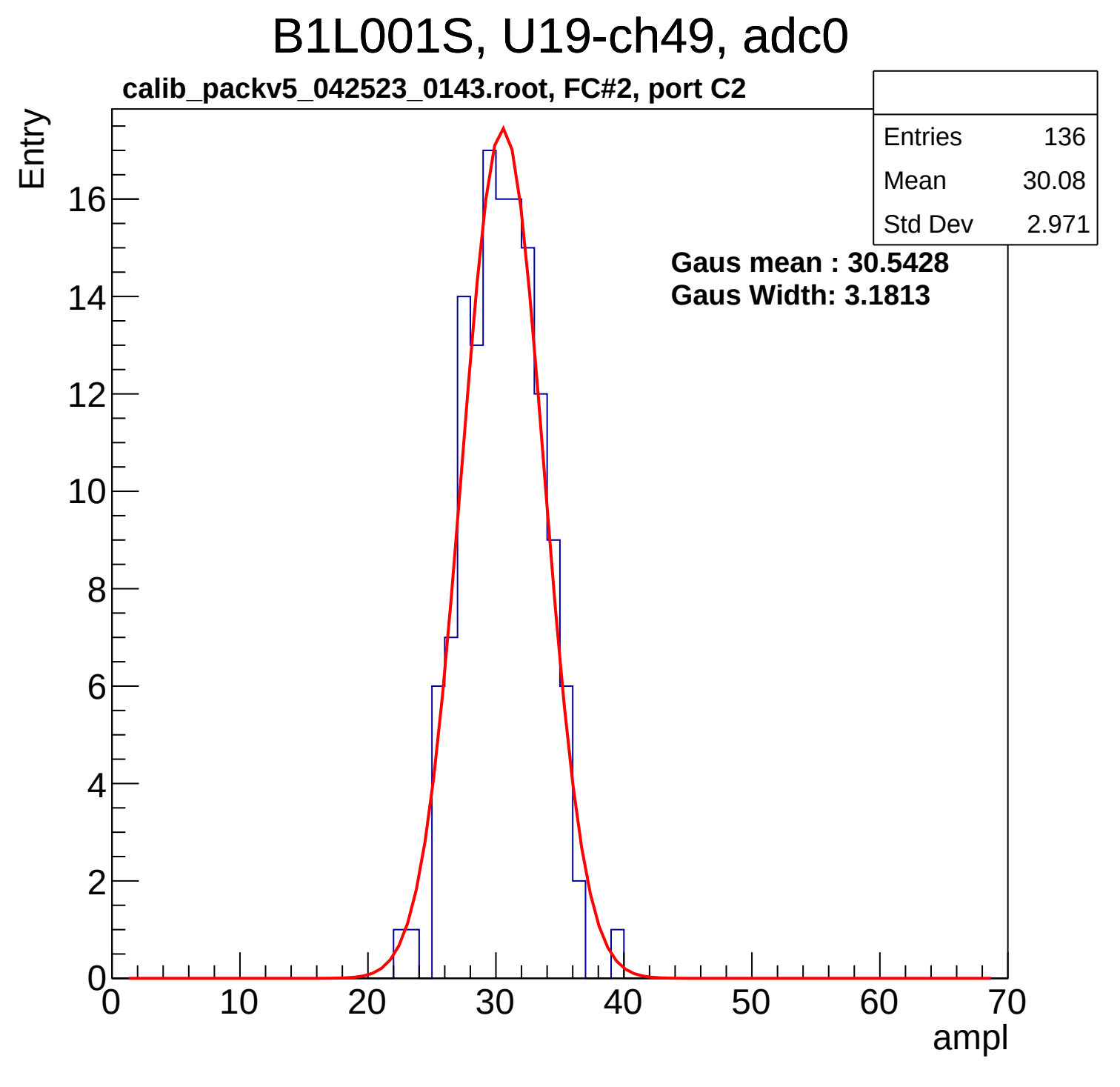
B1L001S, U19-ch49, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 136
Mean 30.08
Std Dev 2.971
Gaus mean : 30.5428
Gaus Width: 3.1813
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
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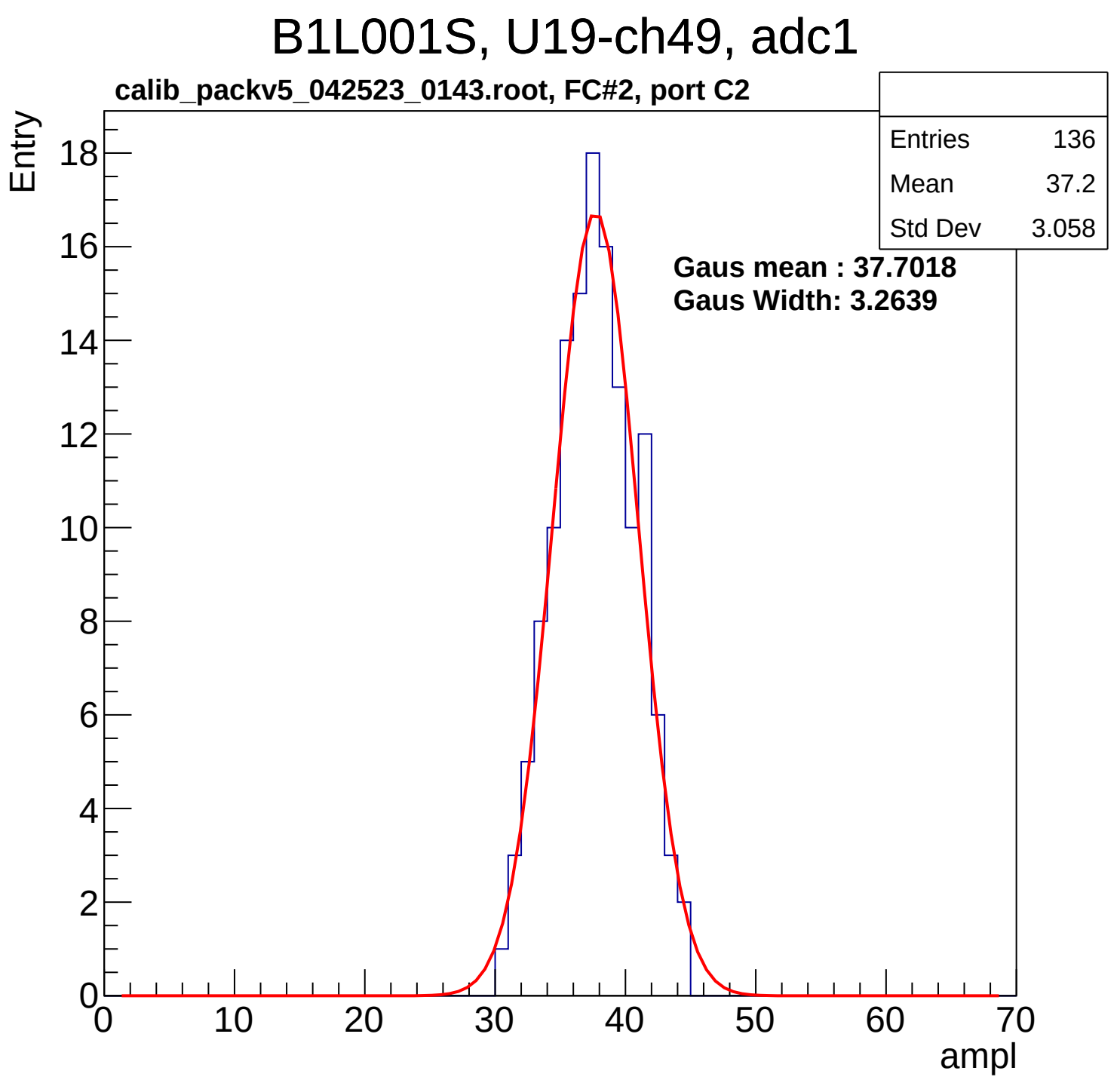
B1L001S, U19-ch49, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 136
Mean 37.2
Std Dev 3.058
Gaus mean : 37.7018
Gaus Width: 3.2639
Entry
ampl
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4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
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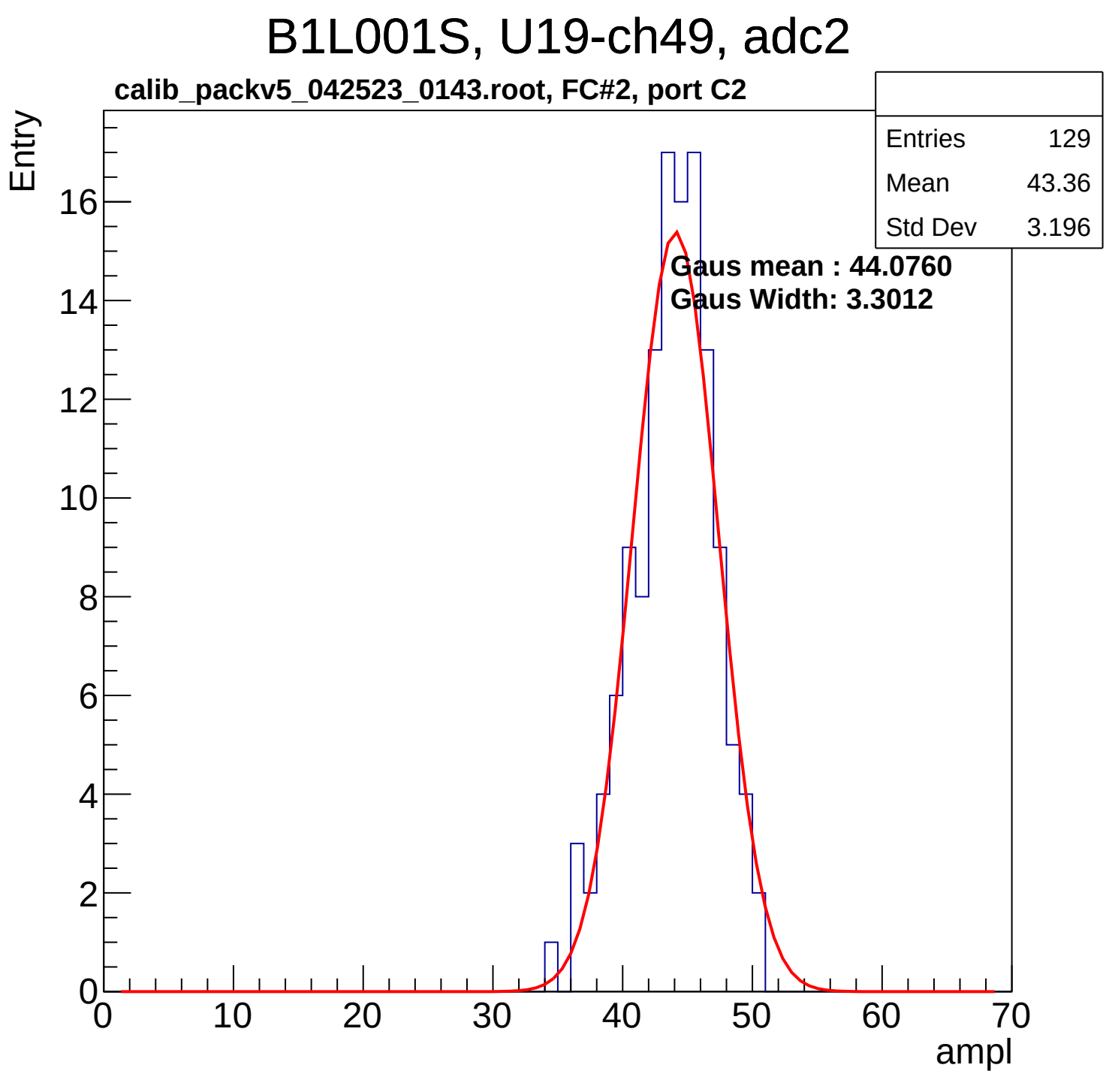
B1L001S, U19-ch49, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 129
Mean 43.36
Std Dev 3.196
Gaus mean : 44.0760
Gaus Width: 3.3012
Entry
ampl
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2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
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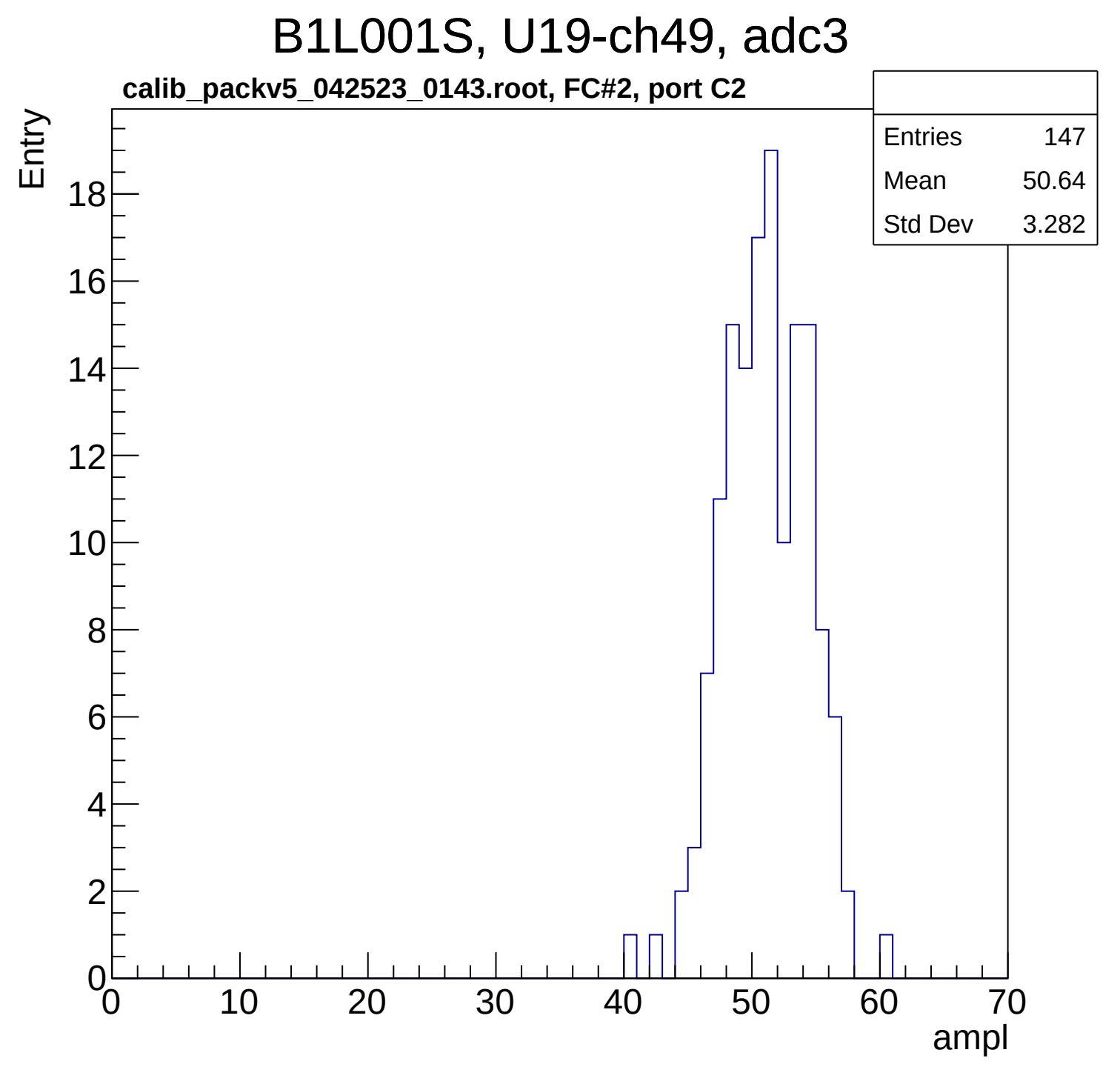
B1L001S, U19-ch49, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 147
Mean 50.64
Std Dev 3.282
Entry
ampl
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4
6
8
10
12
14
16
18
0
10
20
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60
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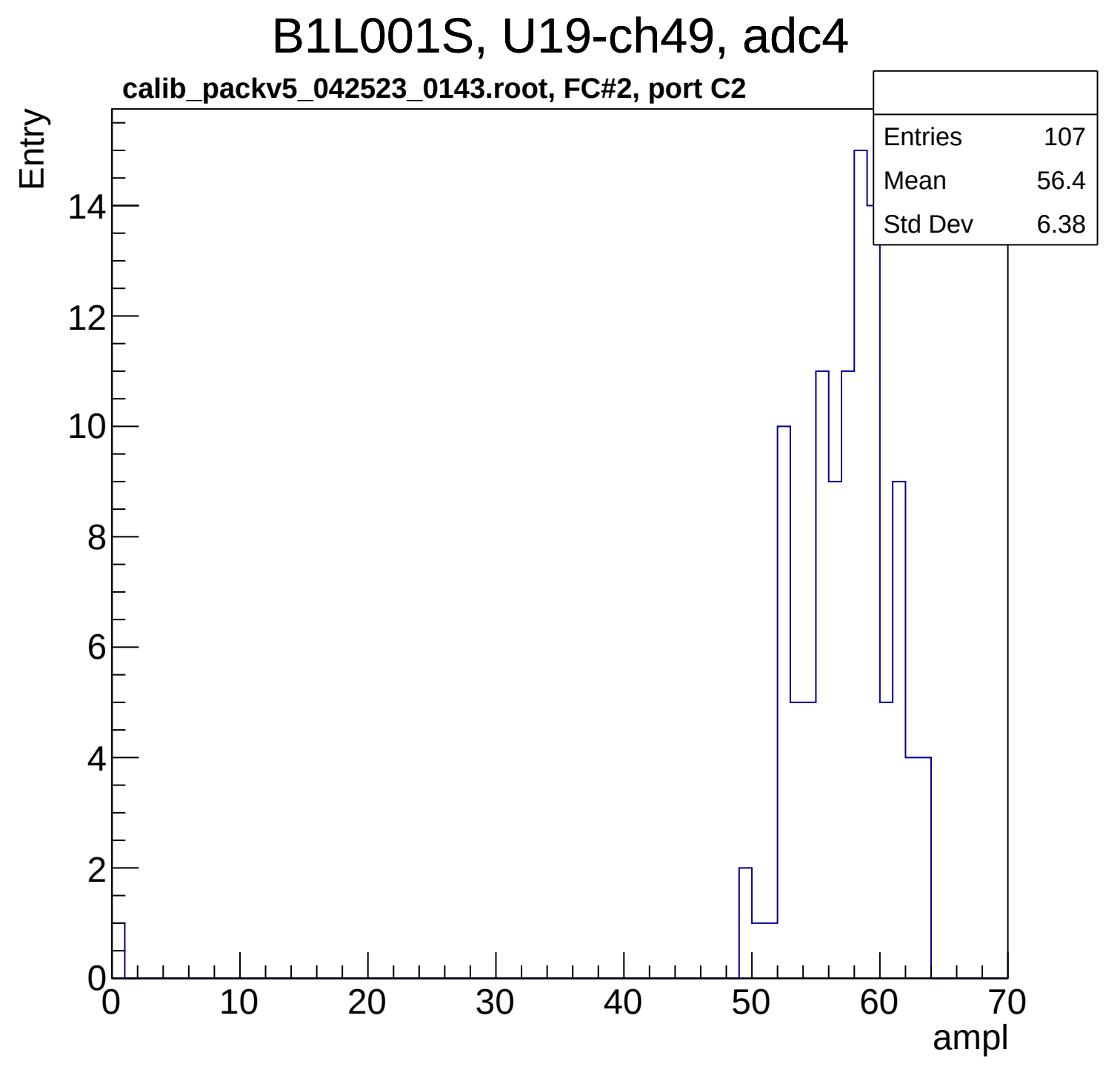
B1L001S, U19-ch49, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 107
Mean 56.4
Std Dev 6.38
Entry
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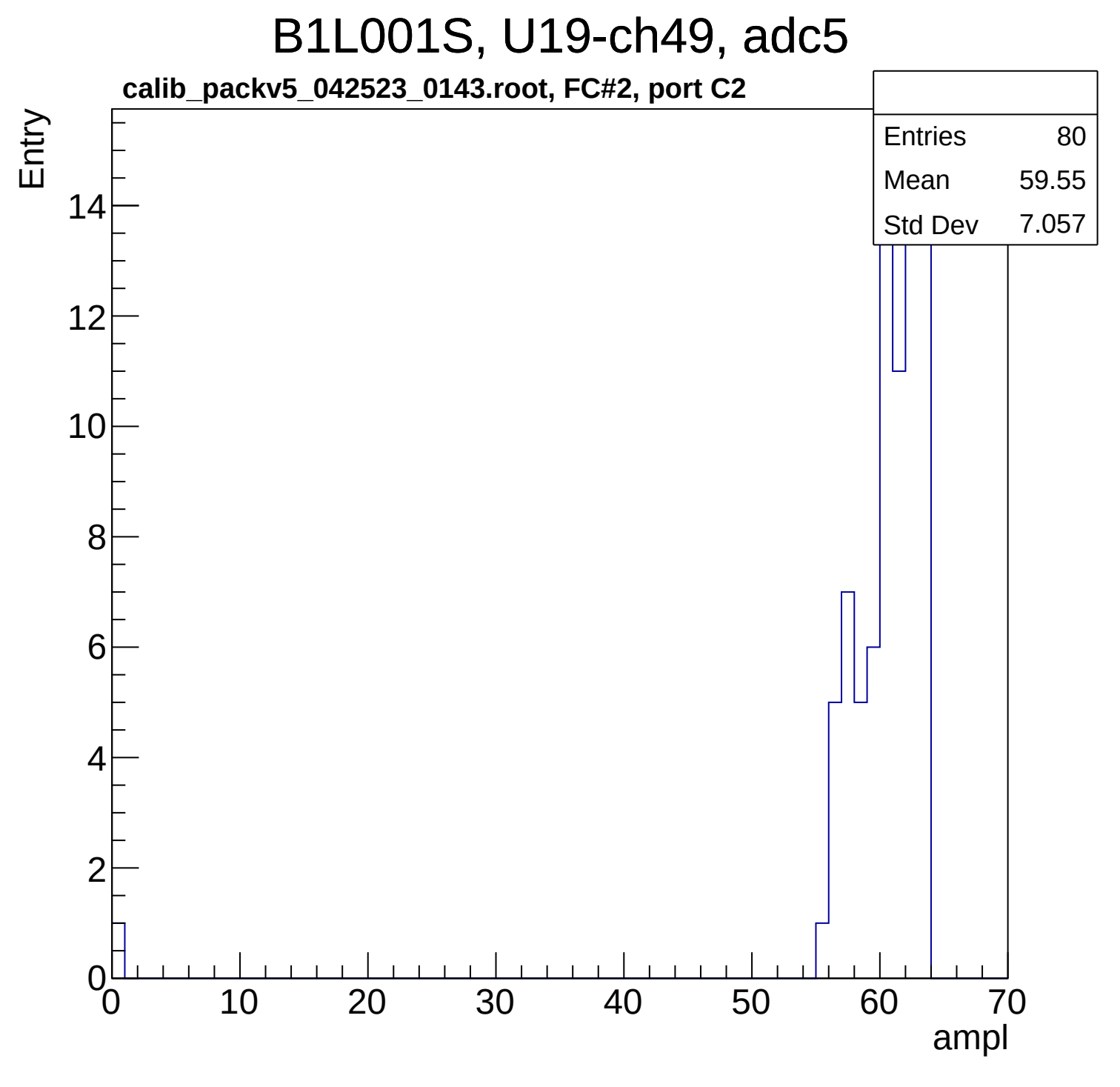
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch49, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 80
Mean 59.55
Std Dev 7.057
Entry
ampl
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0
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40
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60
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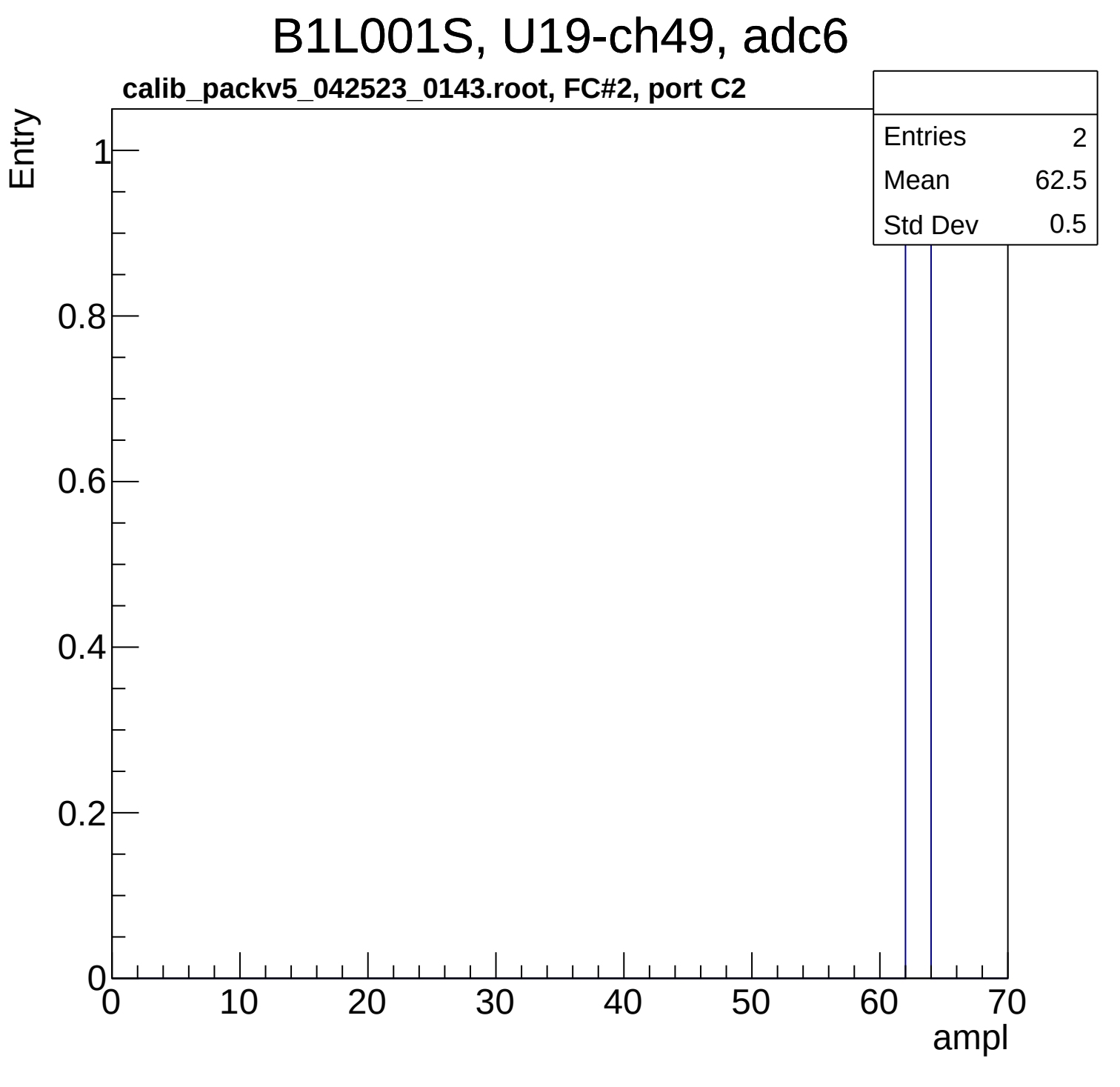
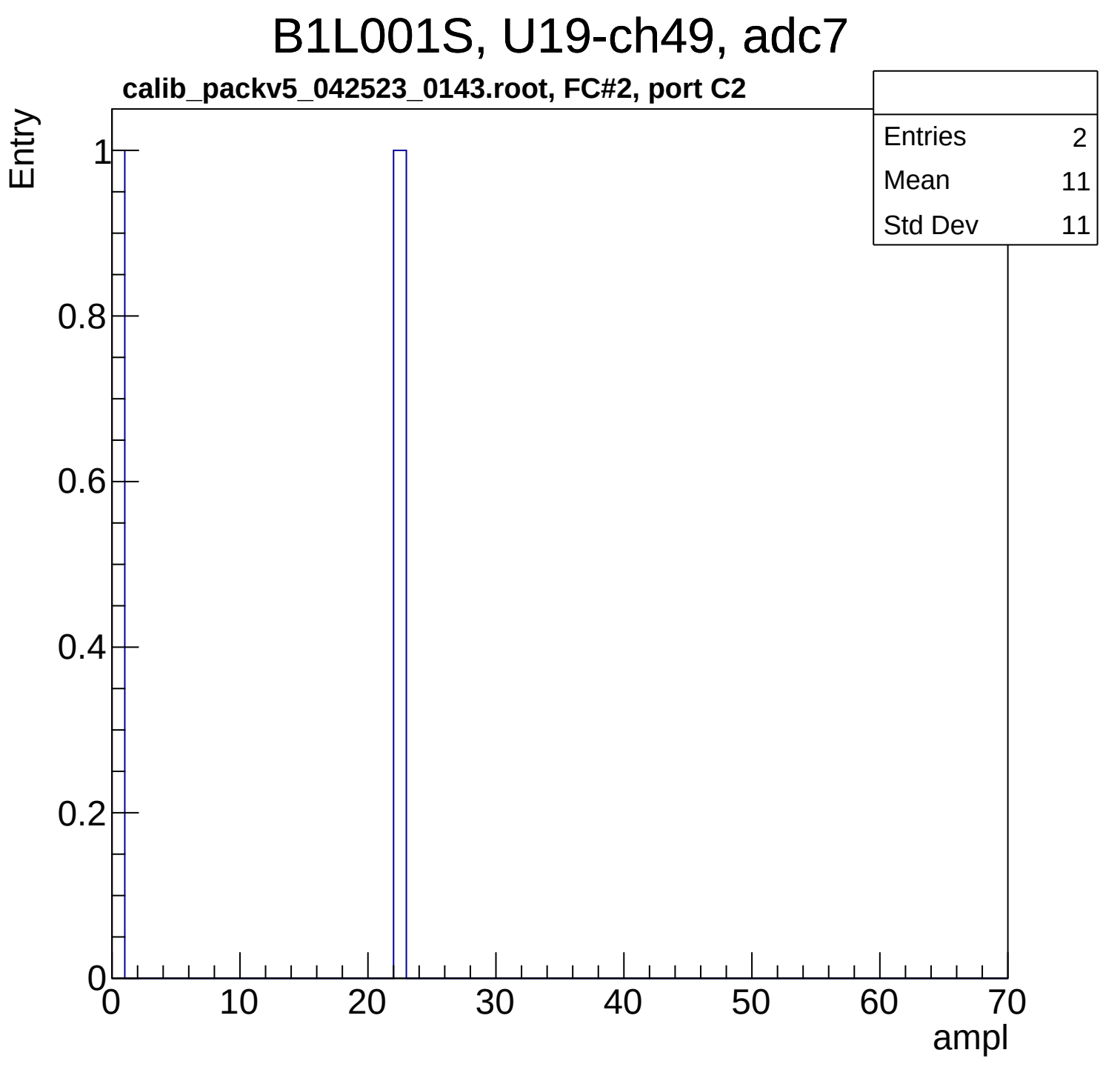
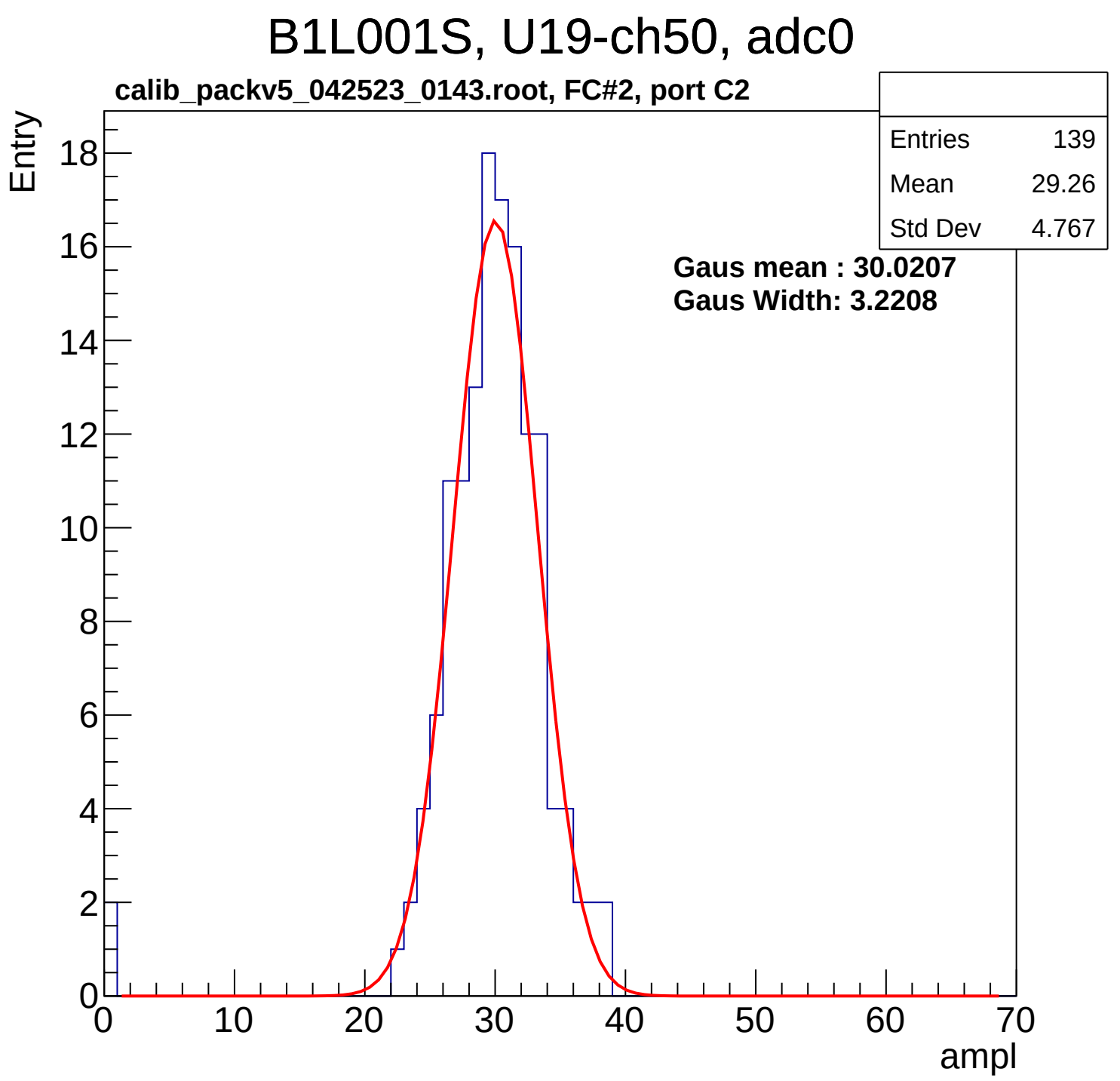

B1L001S, U19-ch49, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 62.5
Std Dev 0.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch49, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 11
Std Dev 11
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch50, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 139
Mean 29.26
Std Dev 4.767
Gaus mean : 30.0207
Gaus Width: 3.2208
Entry
ampl
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2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
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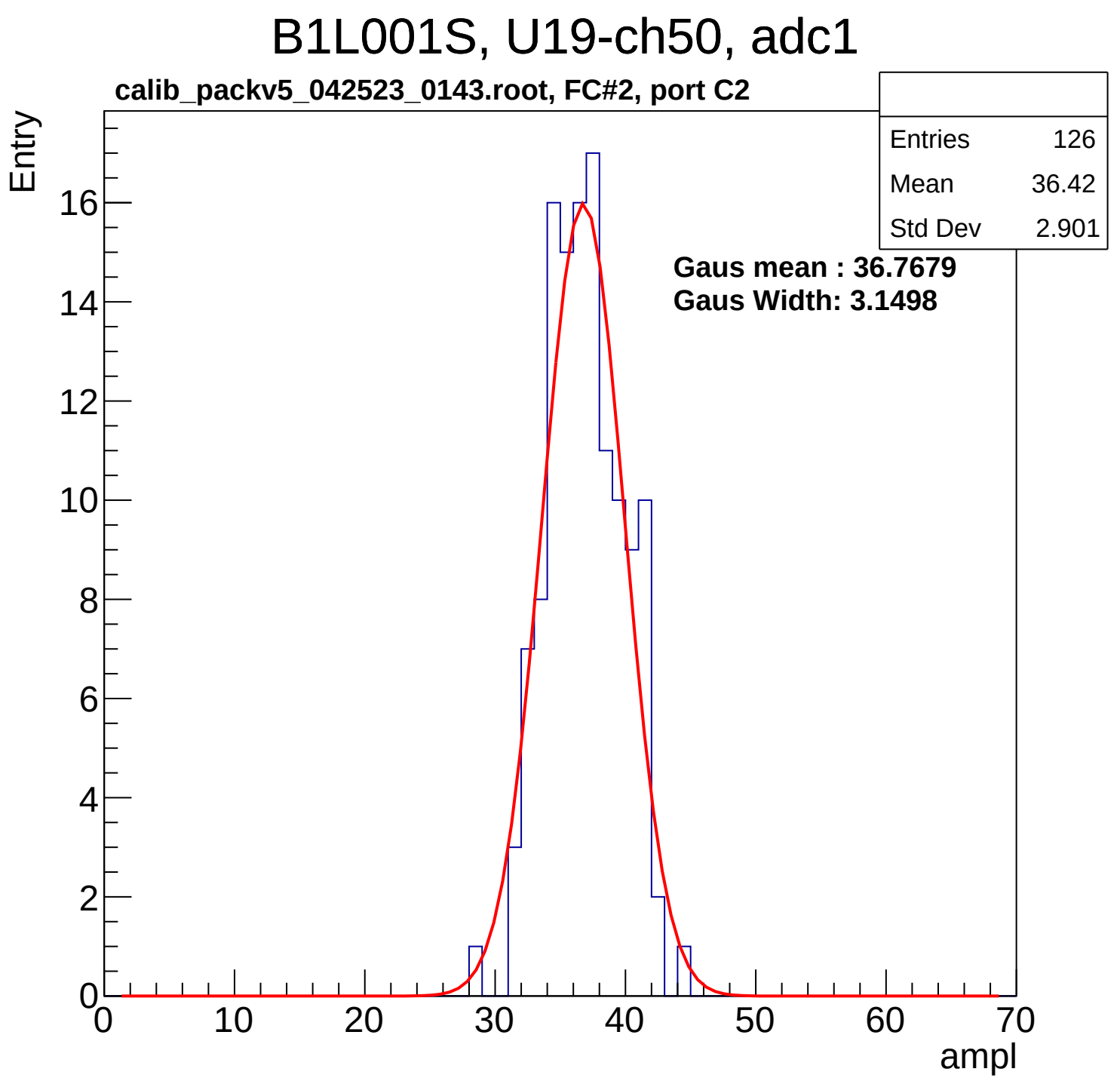
B1L001S, U19-ch50, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 126
Mean 36.42
Std Dev 2.901
Gaus mean : 36.7679
Gaus Width: 3.1498
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
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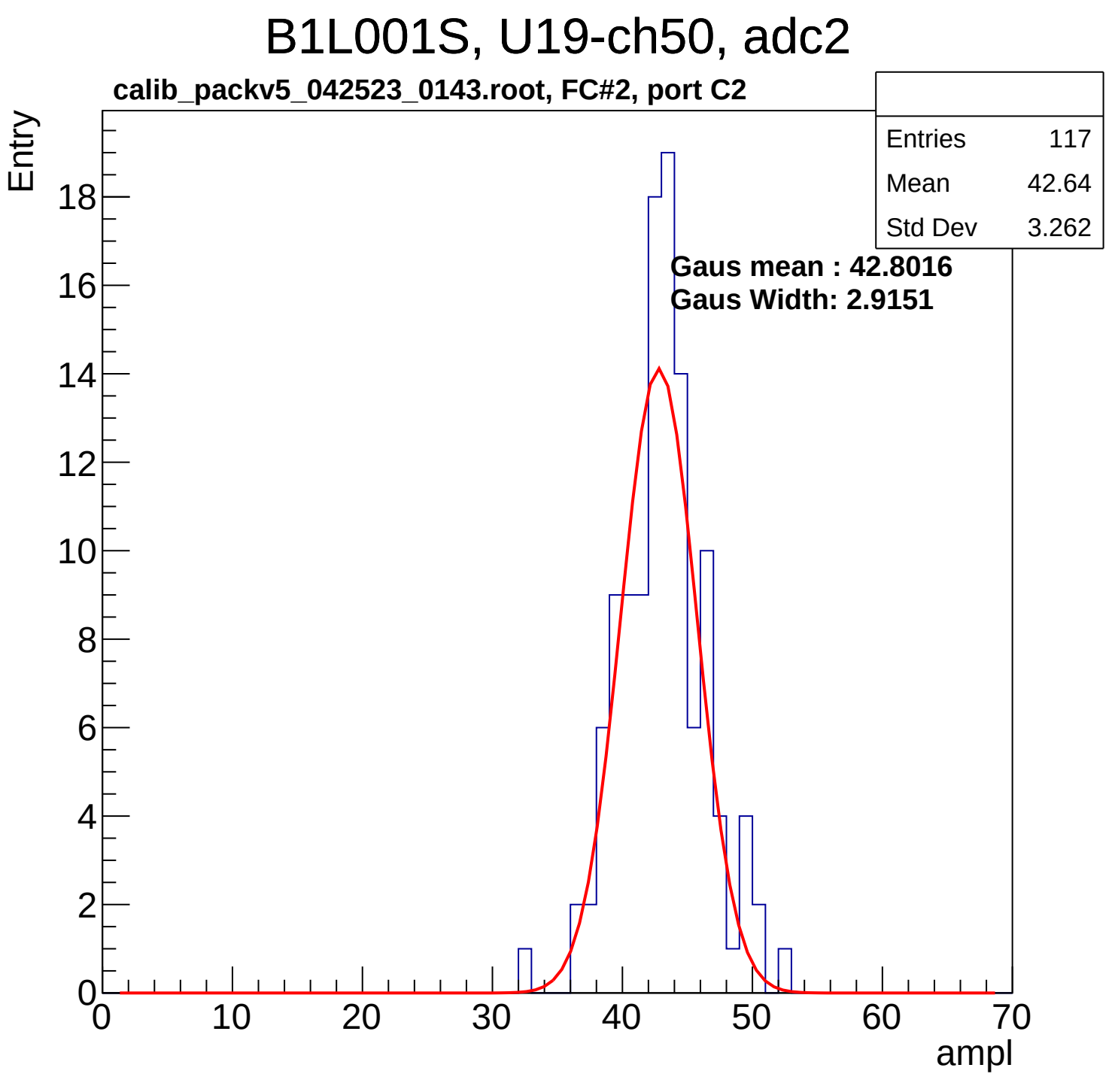
B1L001S, U19-ch50, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 117
Mean 42.64
Std Dev 3.262
Gaus mean : 42.8016
Gaus Width: 2.9151
Entry
ampl
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2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
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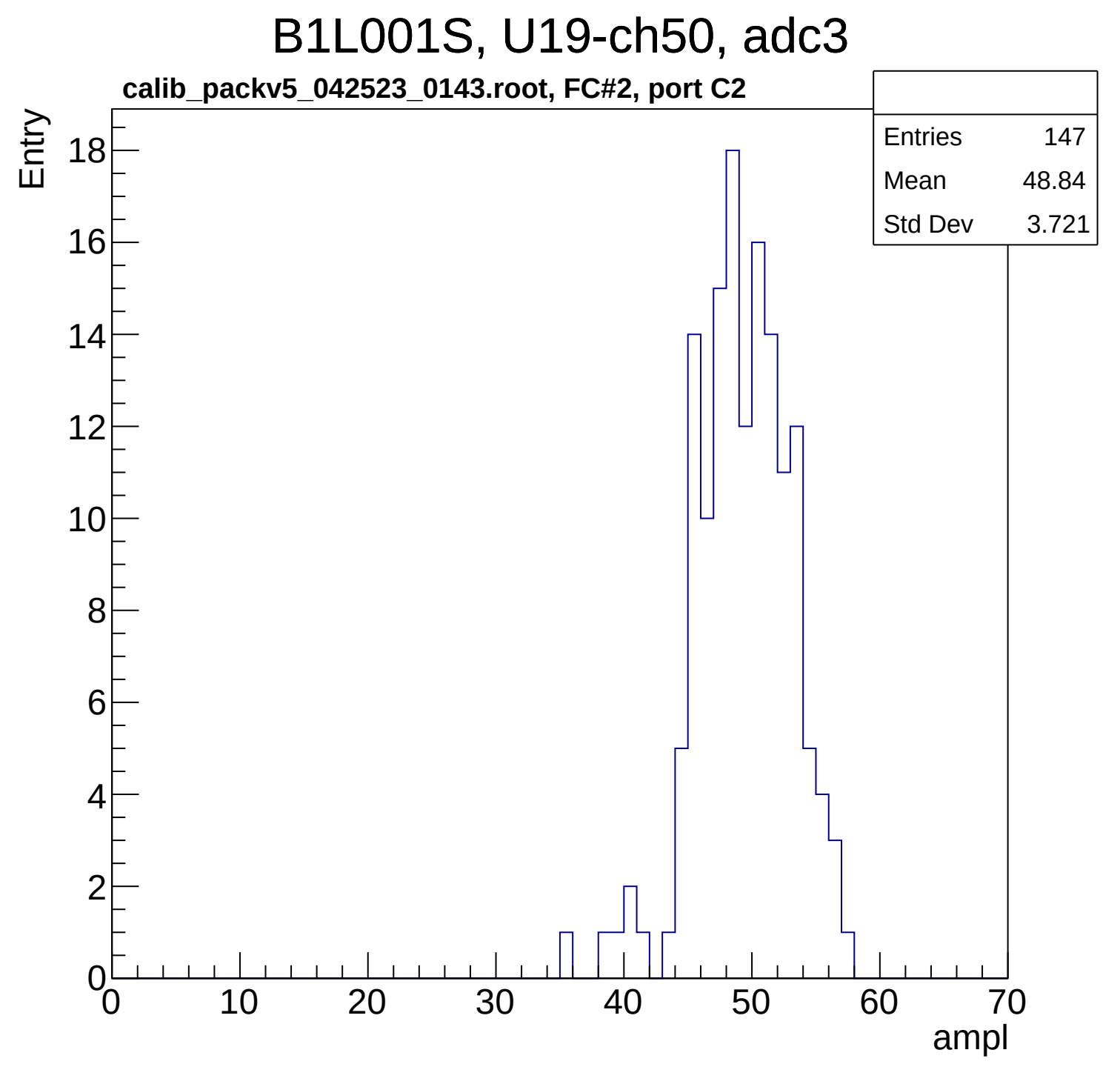
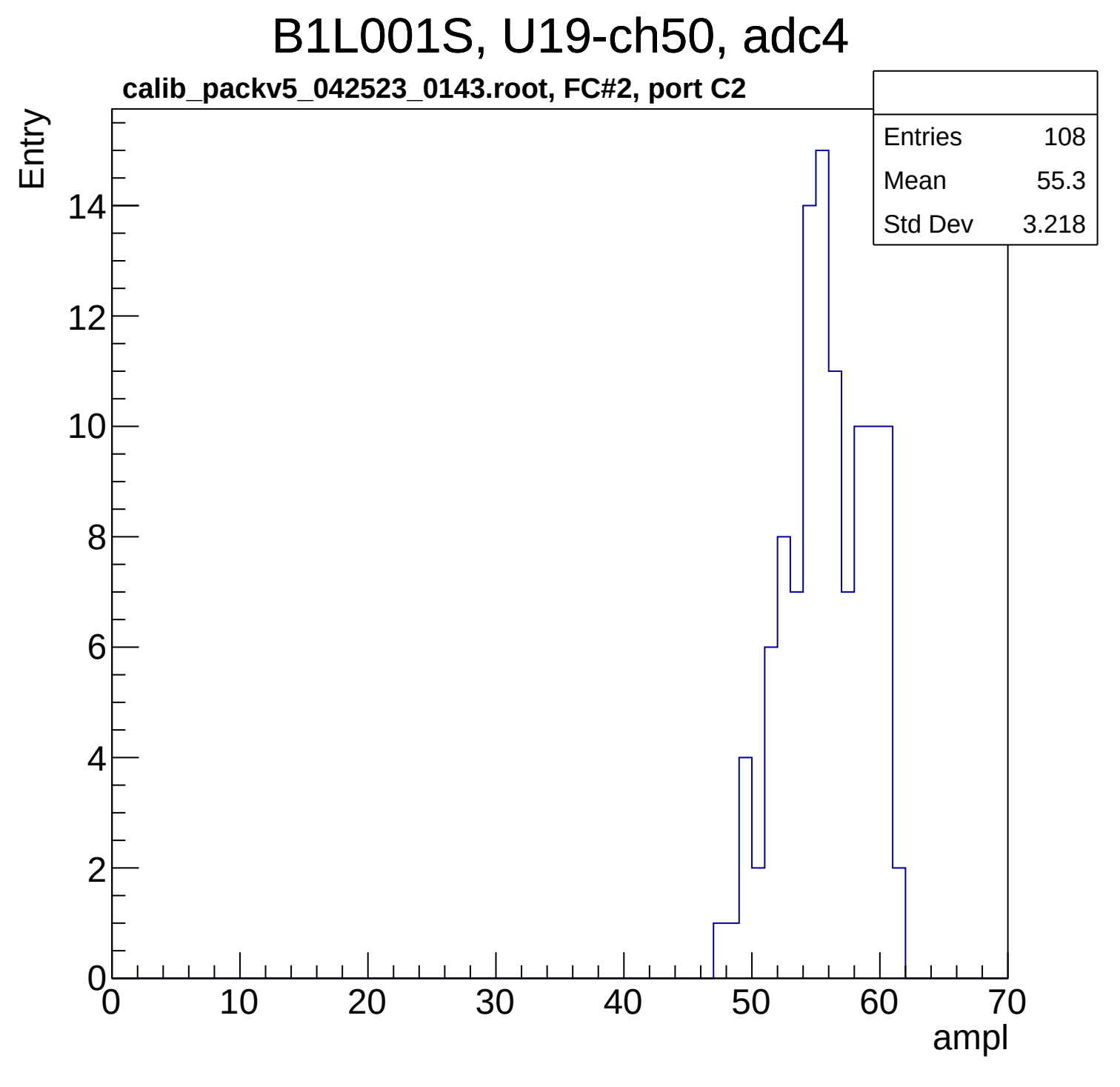
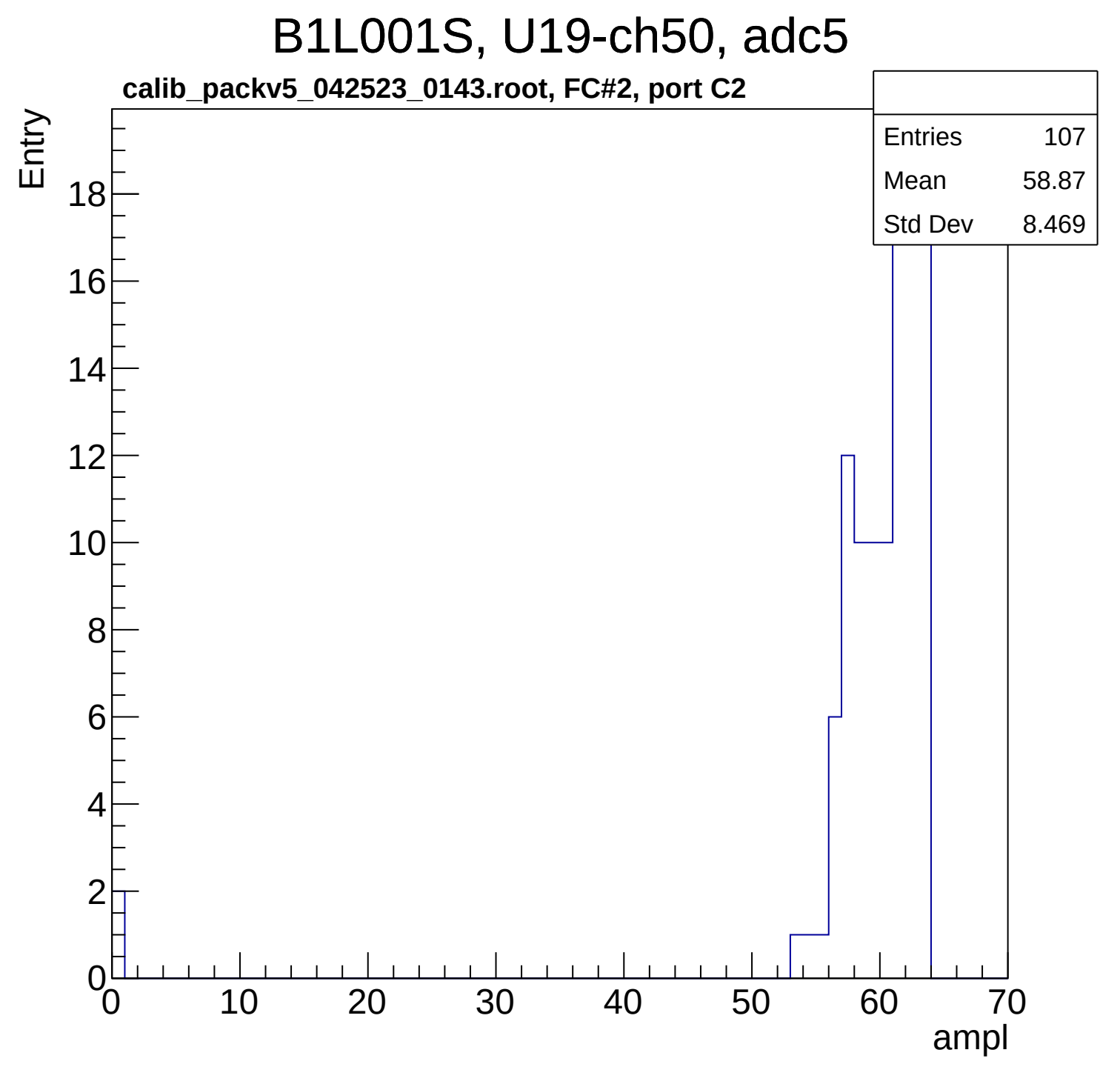

B1L001S, U19-ch50, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 147
Mean 48.84
Std Dev 3.721
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch50, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 108
Mean 55.3
Std Dev 3.218
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch50, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 107
Mean 58.87
Std Dev 8.469
Entry
0
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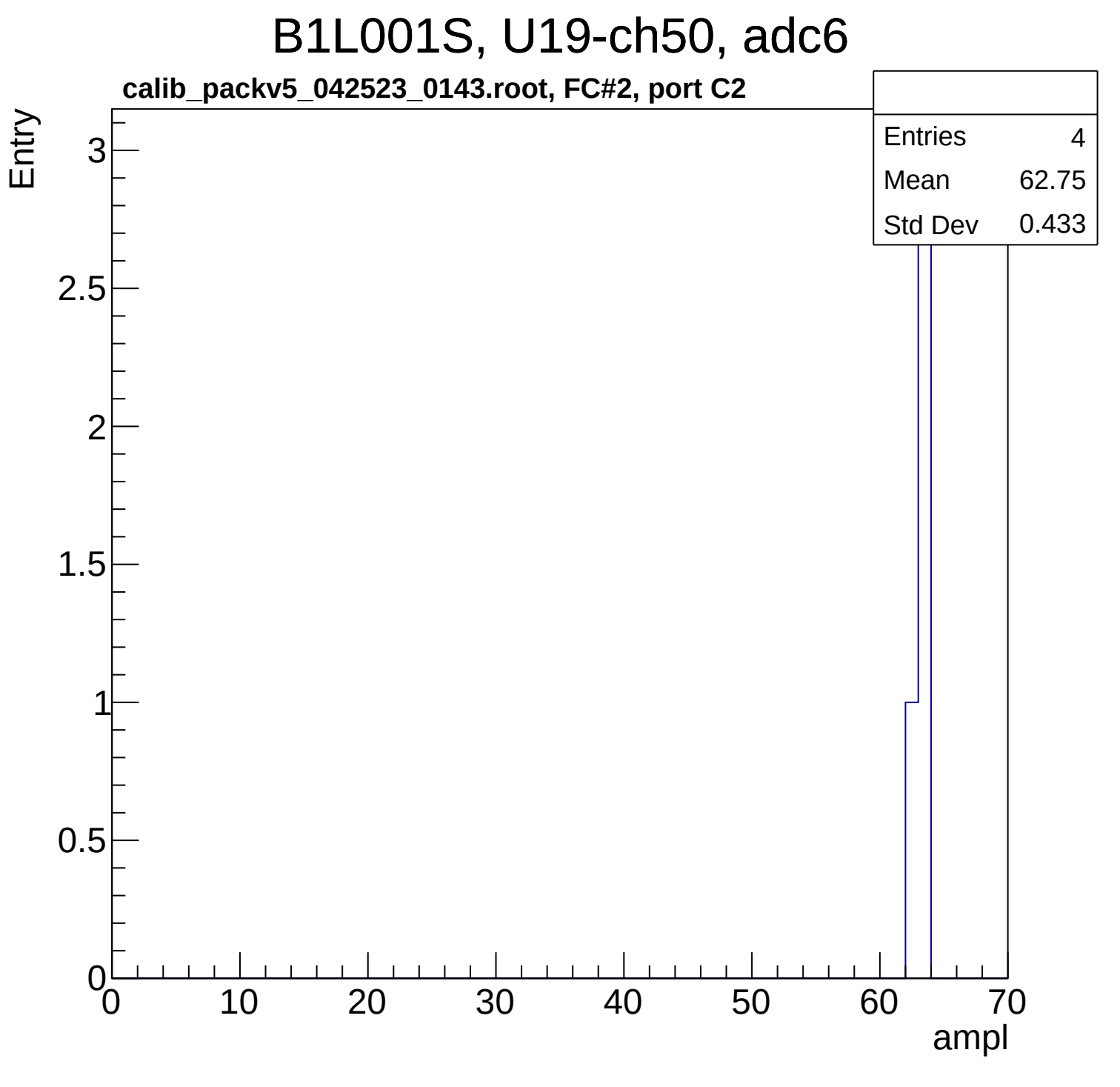
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch50, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 4
Mean 62.75
Std Dev 0.433
Entry
ampl
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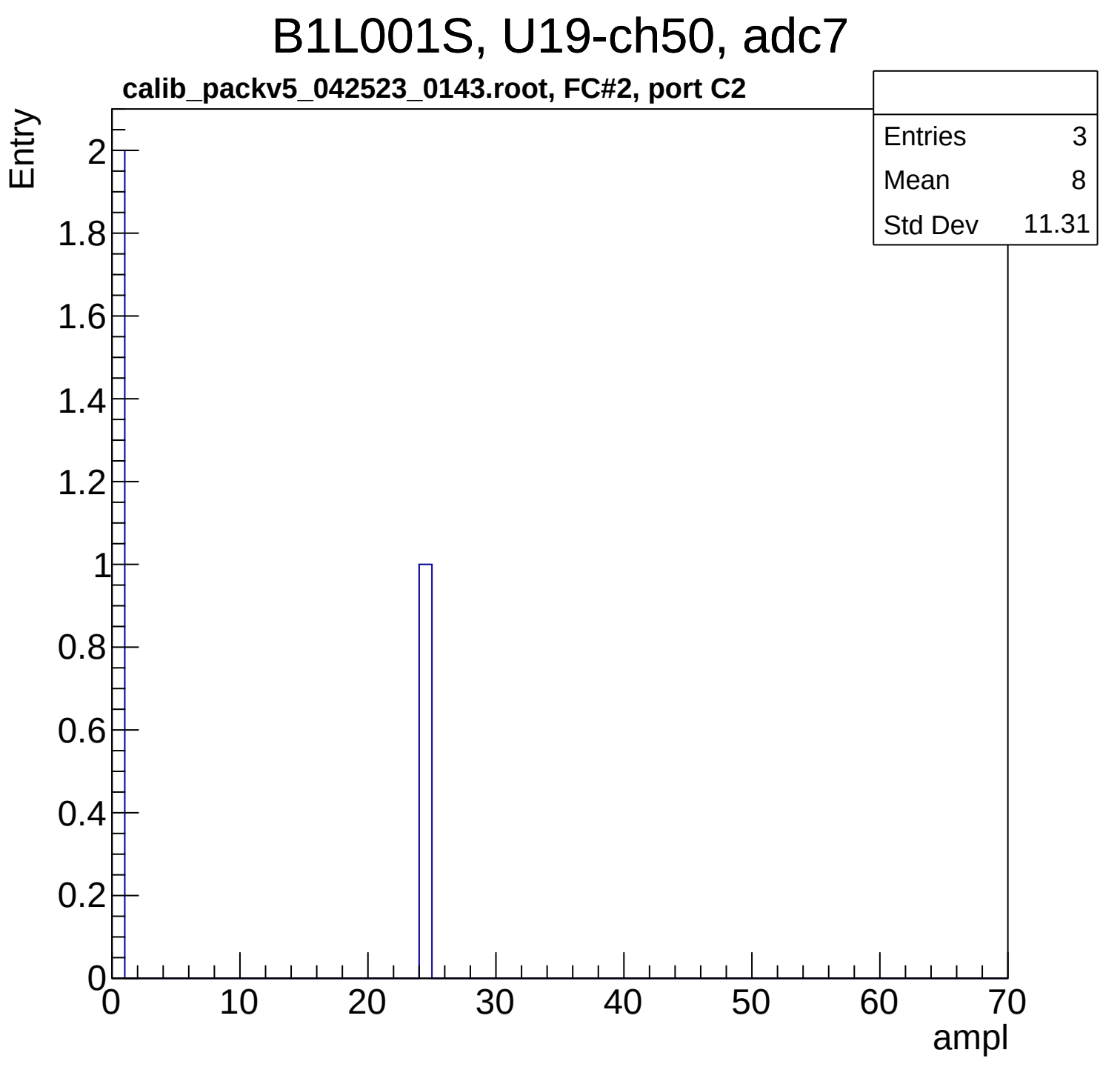
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L001S, U19-ch50, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 3
Mean 8
Std Dev 11.31
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
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20
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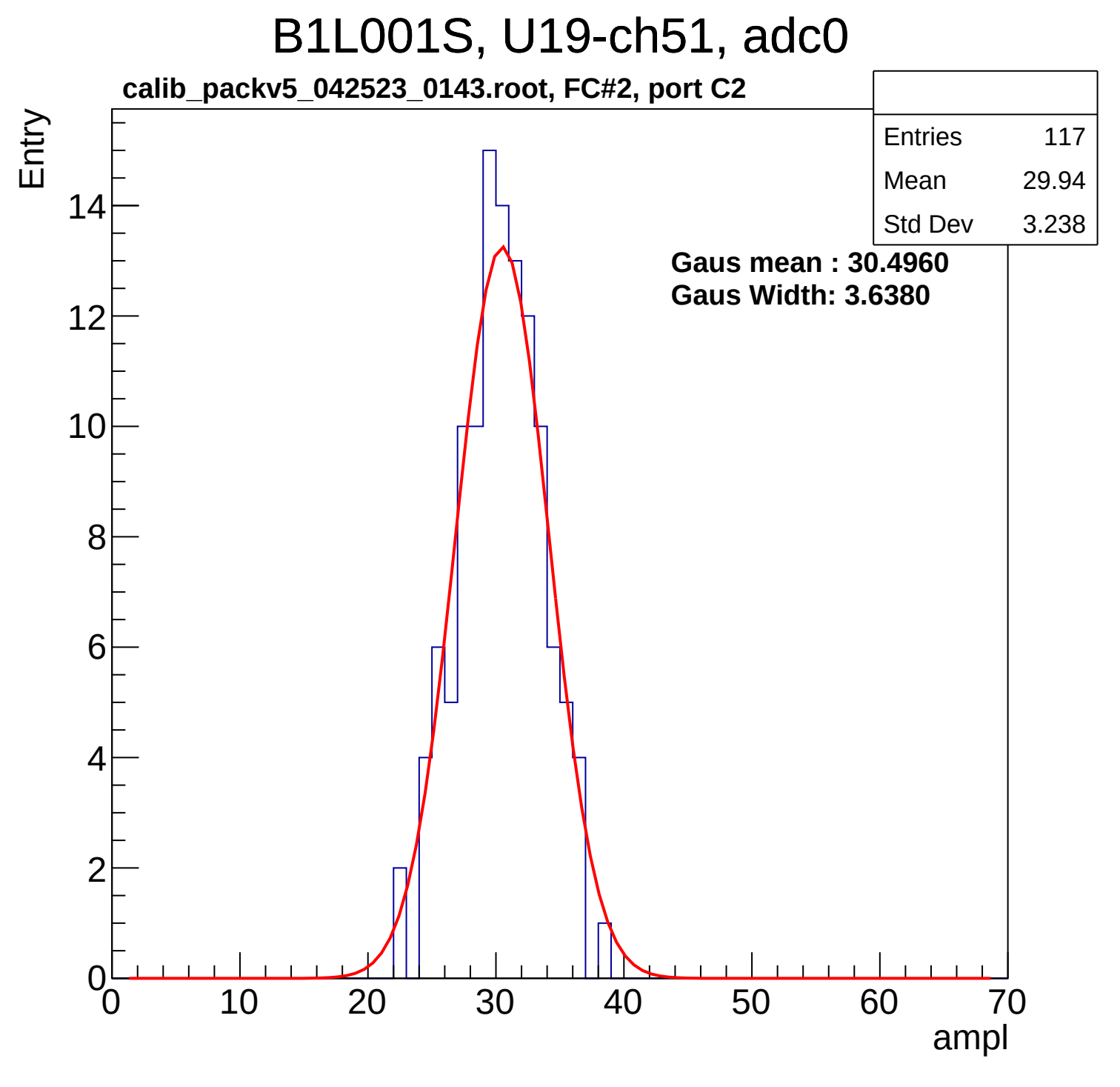
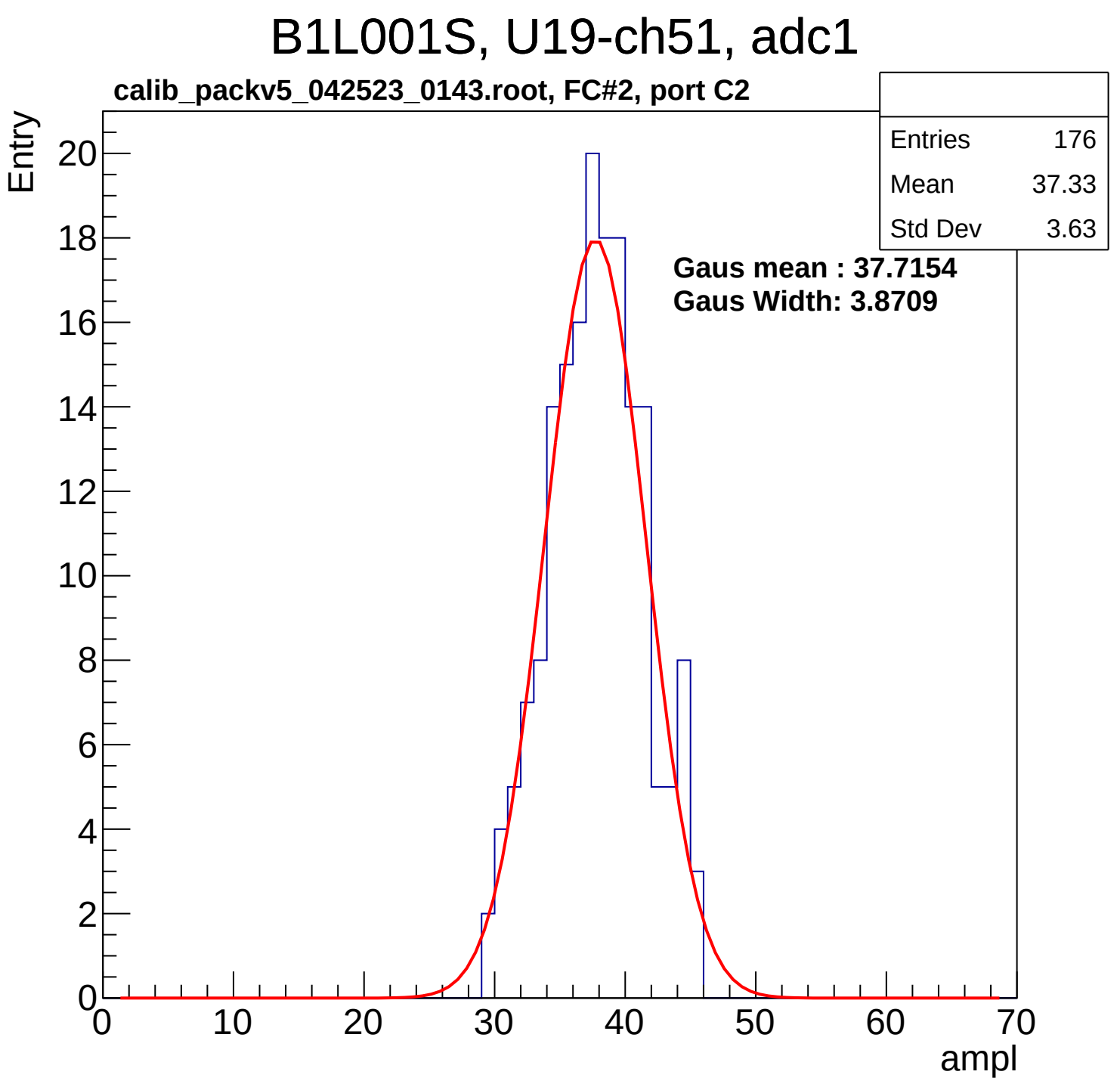
50
60
70


B1L001S, U19-ch51, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 117
Mean 29.94
Std Dev 3.238
Gaus mean : 30.4960
Gaus Width: 3.6380
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L001S, U19-ch51, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 176
Mean 37.33
Std Dev 3.63
Gaus mean : 37.7154
Gaus Width: 3.8709
Entry
ampl
0
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4
6
8
10
12
14
16
18
20
0
10
20
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60
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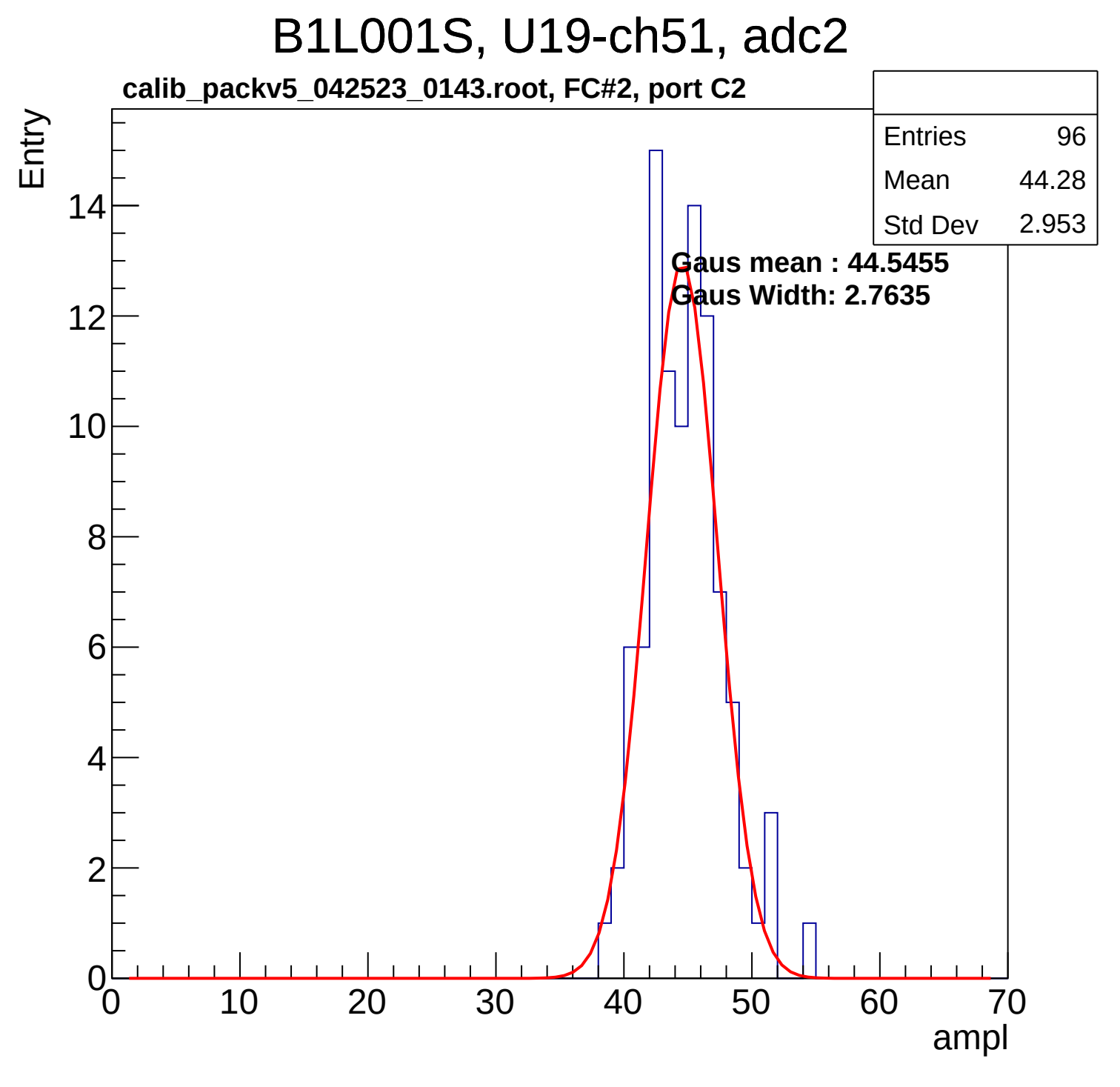
B1L001S, U19-ch51, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 96
Mean 44.28
Std Dev 2.953
Gaus mean : 44.5455
Gaus Width: 2.7635
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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60
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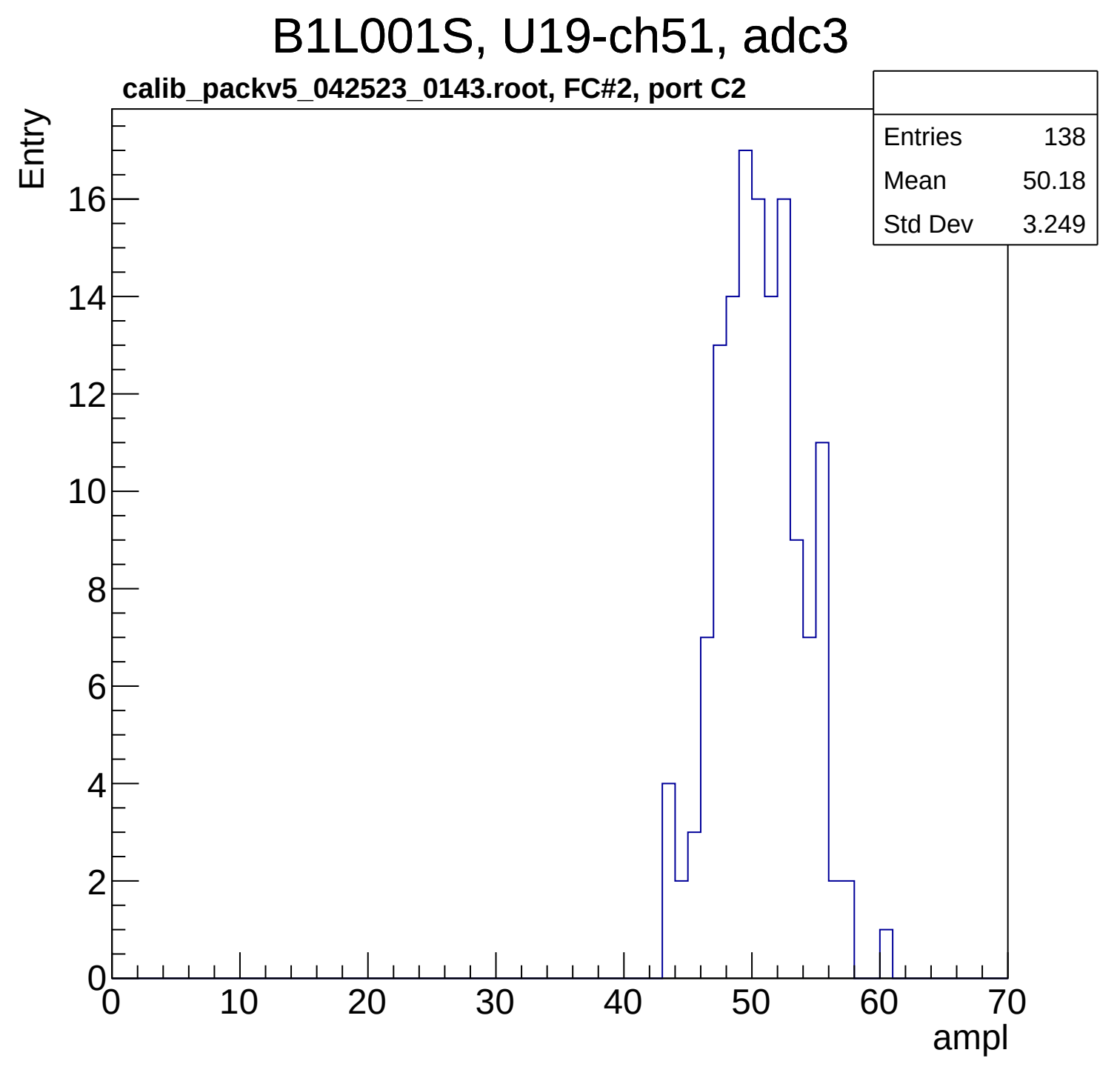
B1L001S, U19-ch51, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 138
Mean 50.18
Std Dev 3.249
Entry
ampl
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2
4
6
8
10
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14
16
0
10
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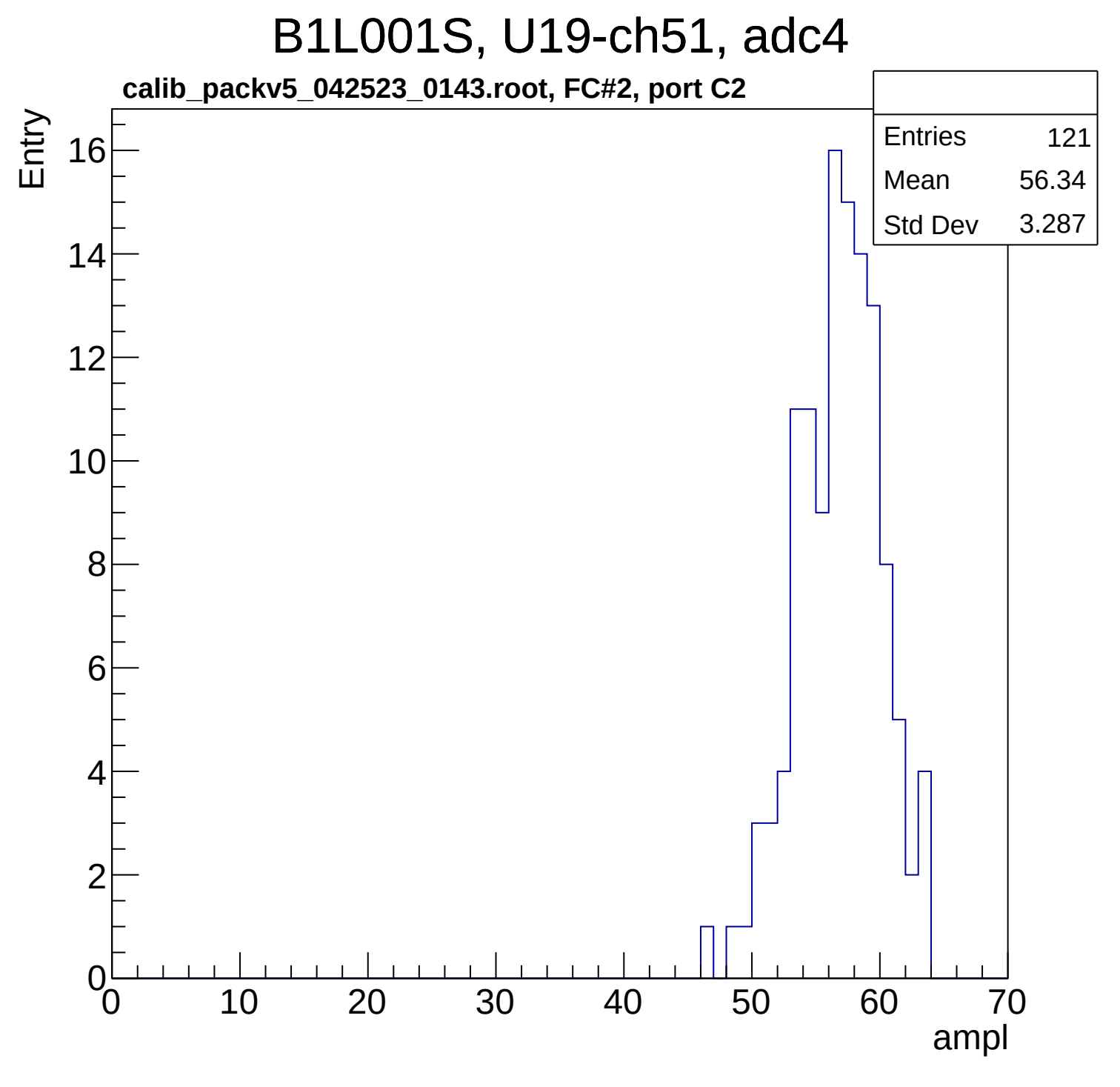
B1L001S, U19-ch51, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 121
Mean 56.34
Std Dev 3.287
Entry
ampl
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8
10
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0
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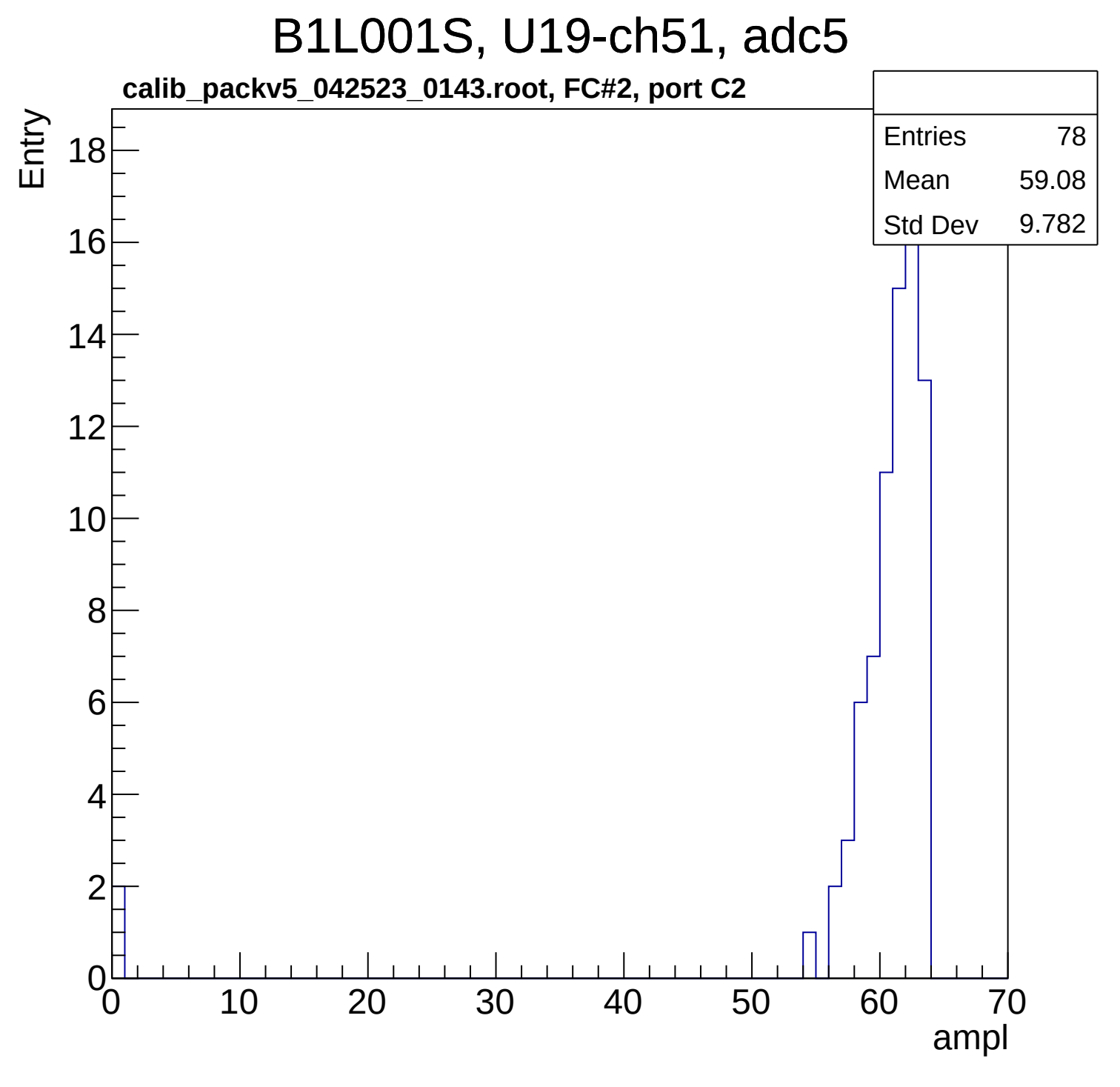
B1L001S, U19-ch51, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 78
Mean 59.08
Std Dev 9.782
Entry
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10
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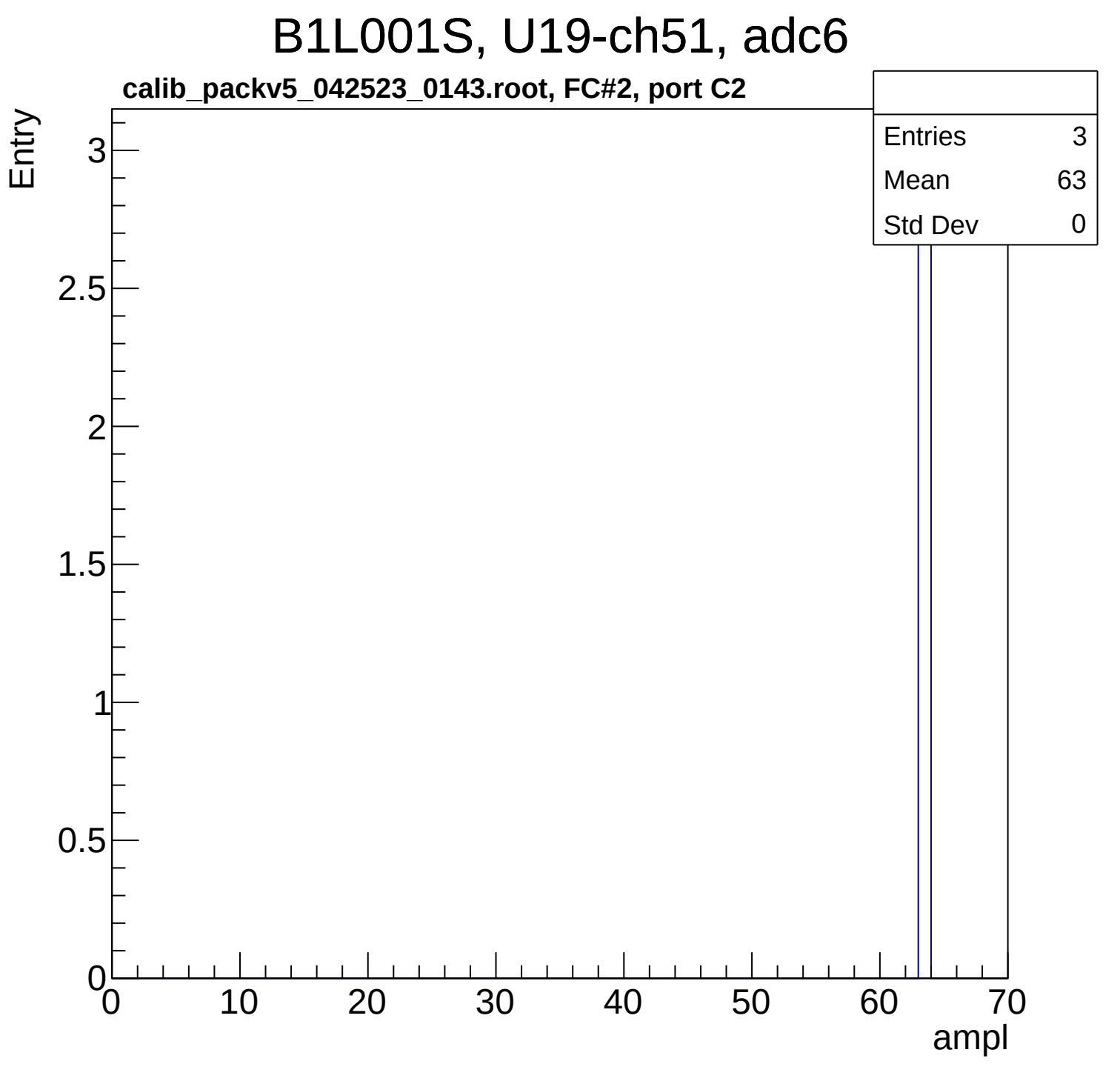
70
ampl


B1L001S, U19-ch51, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 3
Mean 63
Std Dev 0
Entry
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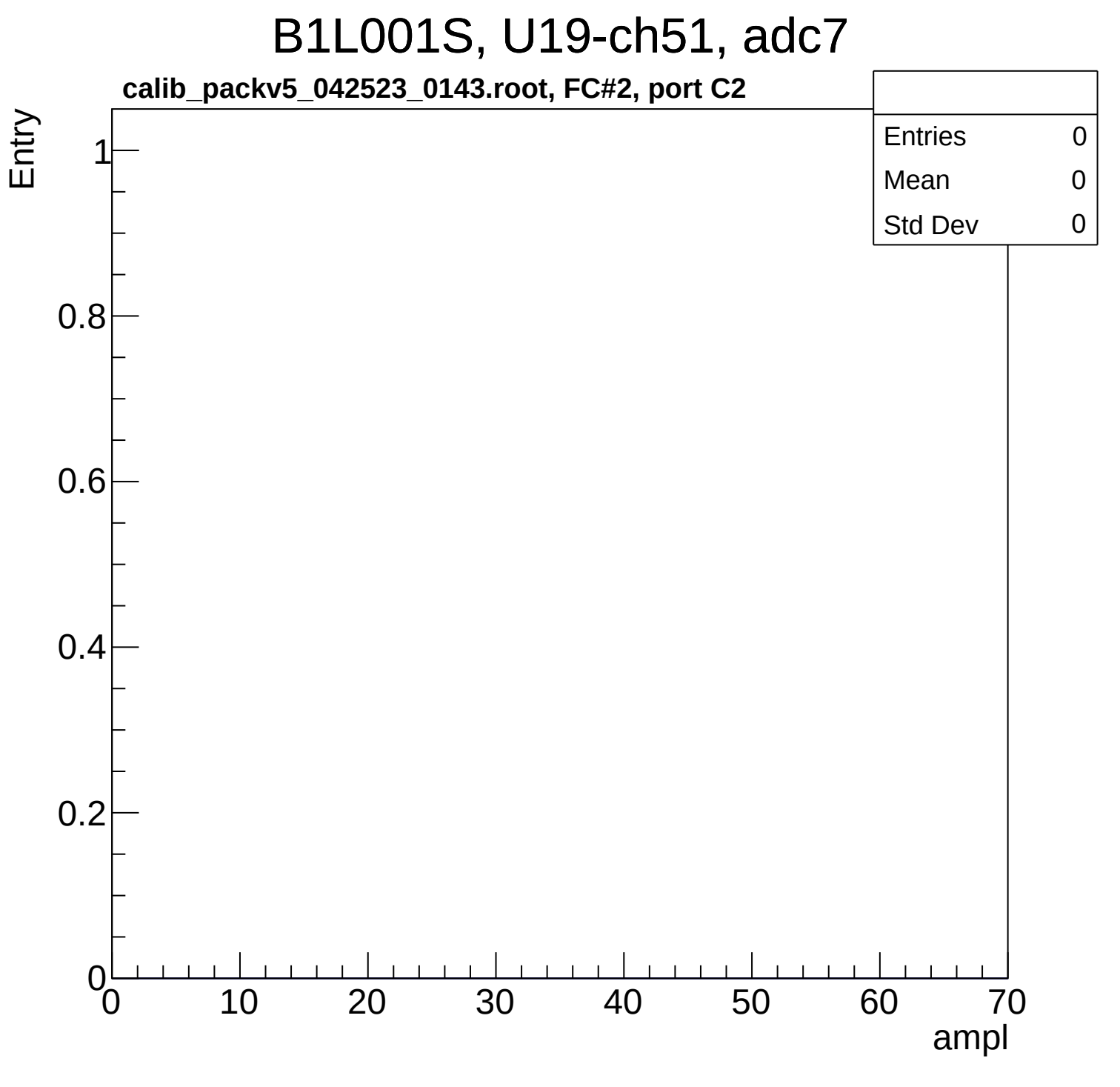
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch51, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 0
Mean 0
Std Dev 0
Entry
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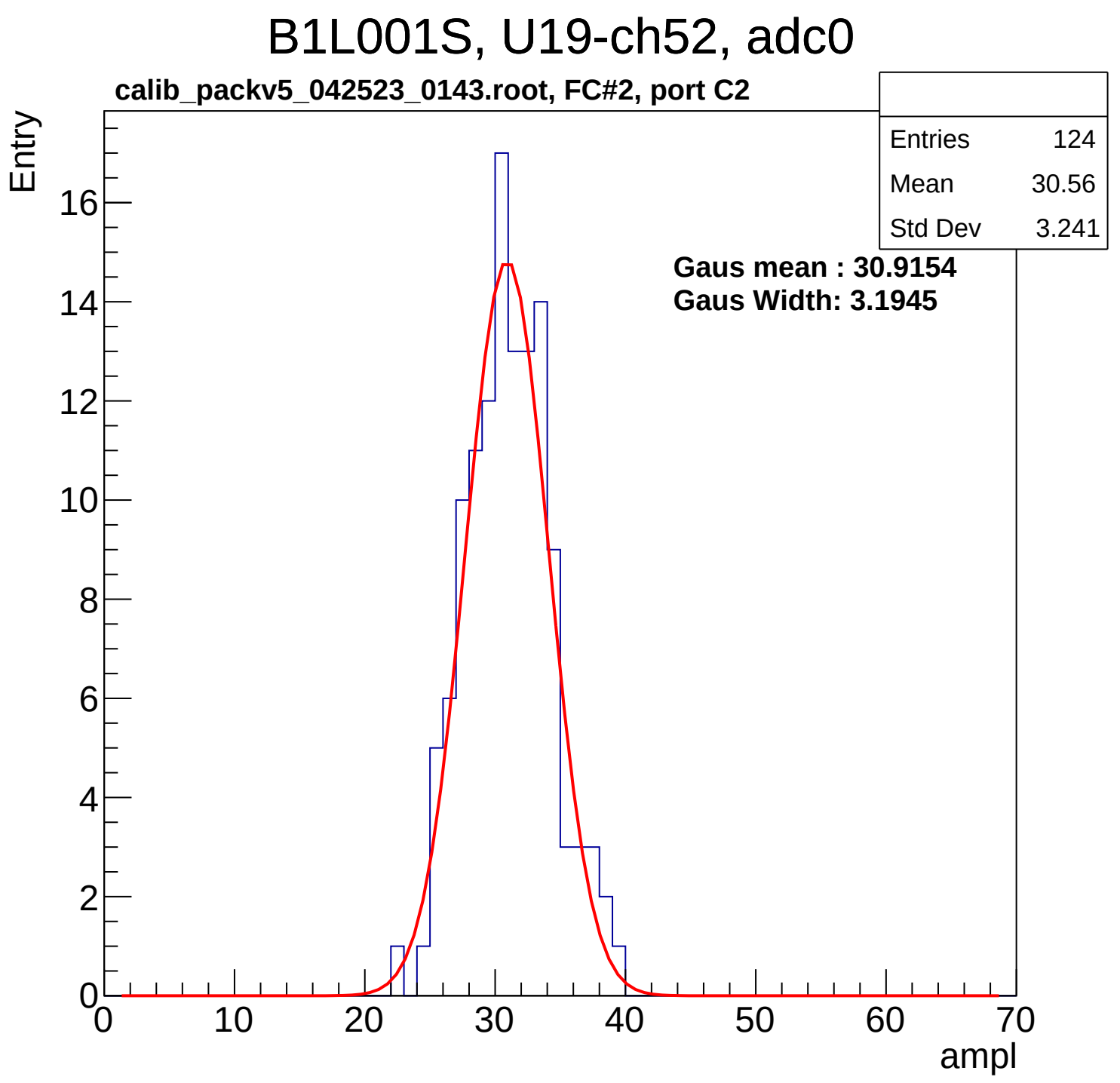
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch52, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 124
Mean 30.56
Std Dev 3.241
Gaus mean : 30.9154
Gaus Width: 3.1945
Entry
ampl
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2
4
6
8
10
12
14
16
0
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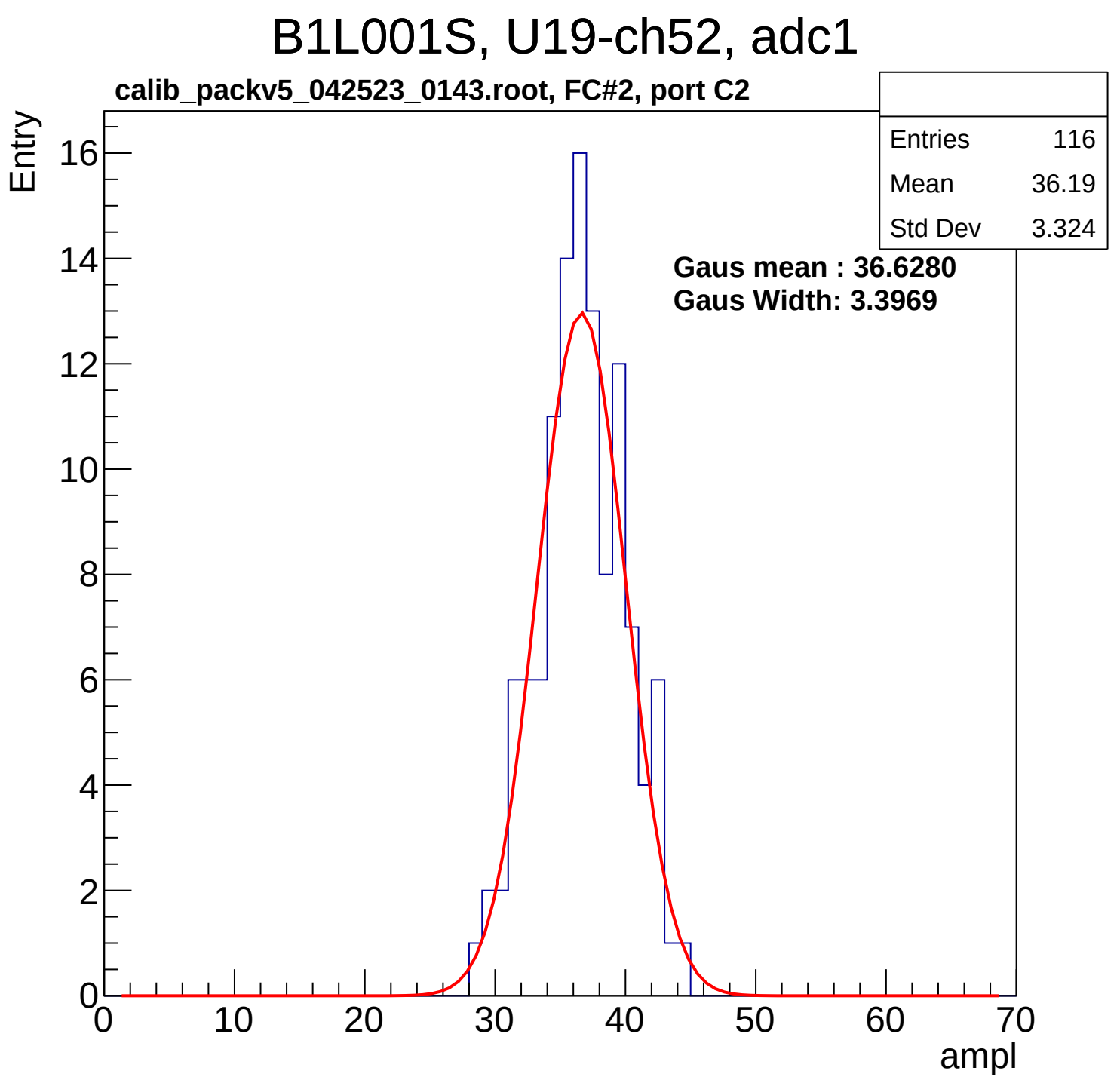
20
30
40
50
60
70


B1L001S, U19-ch52, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 116
Mean 36.19
Std Dev 3.324
Gaus mean : 36.6280
Gaus Width: 3.3969
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
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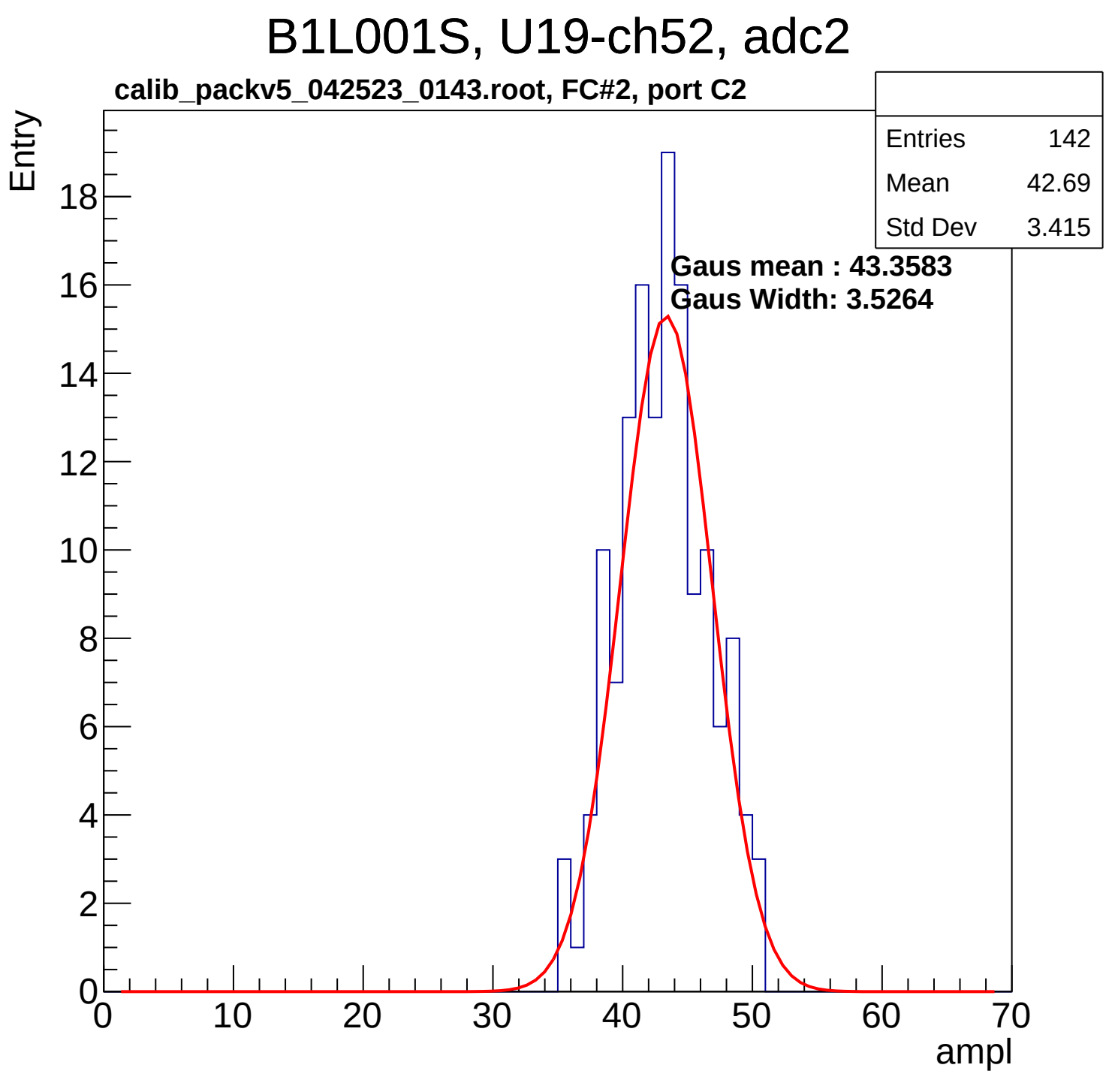
50
60
70


B1L001S, U19-ch52, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 142
Mean 42.69
Std Dev 3.415
Gaus mean : 43.3583
Gaus Width: 3.5264
Entry
ampl
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2
4
6
8
10
12
14
16
18
0
10
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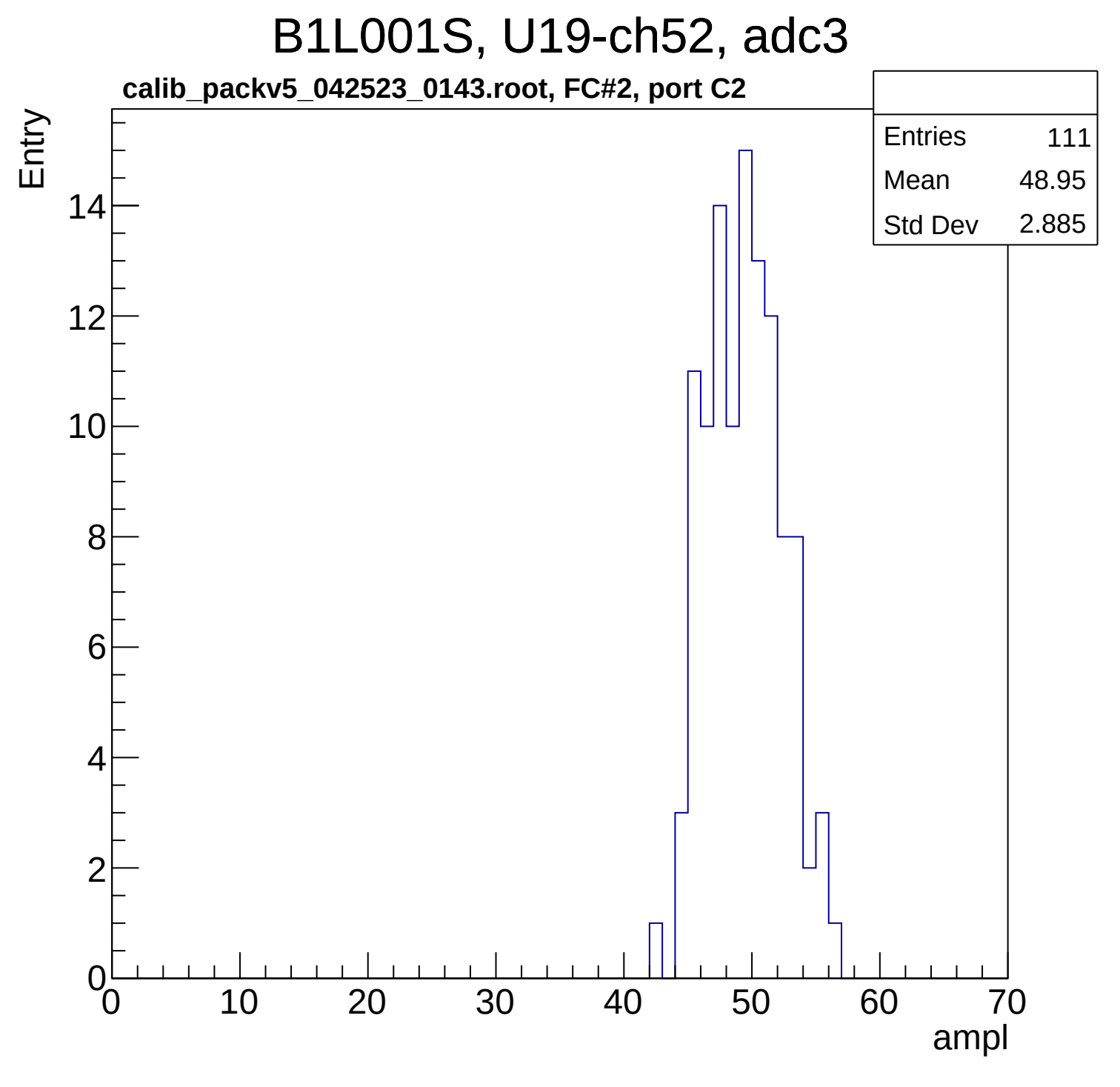
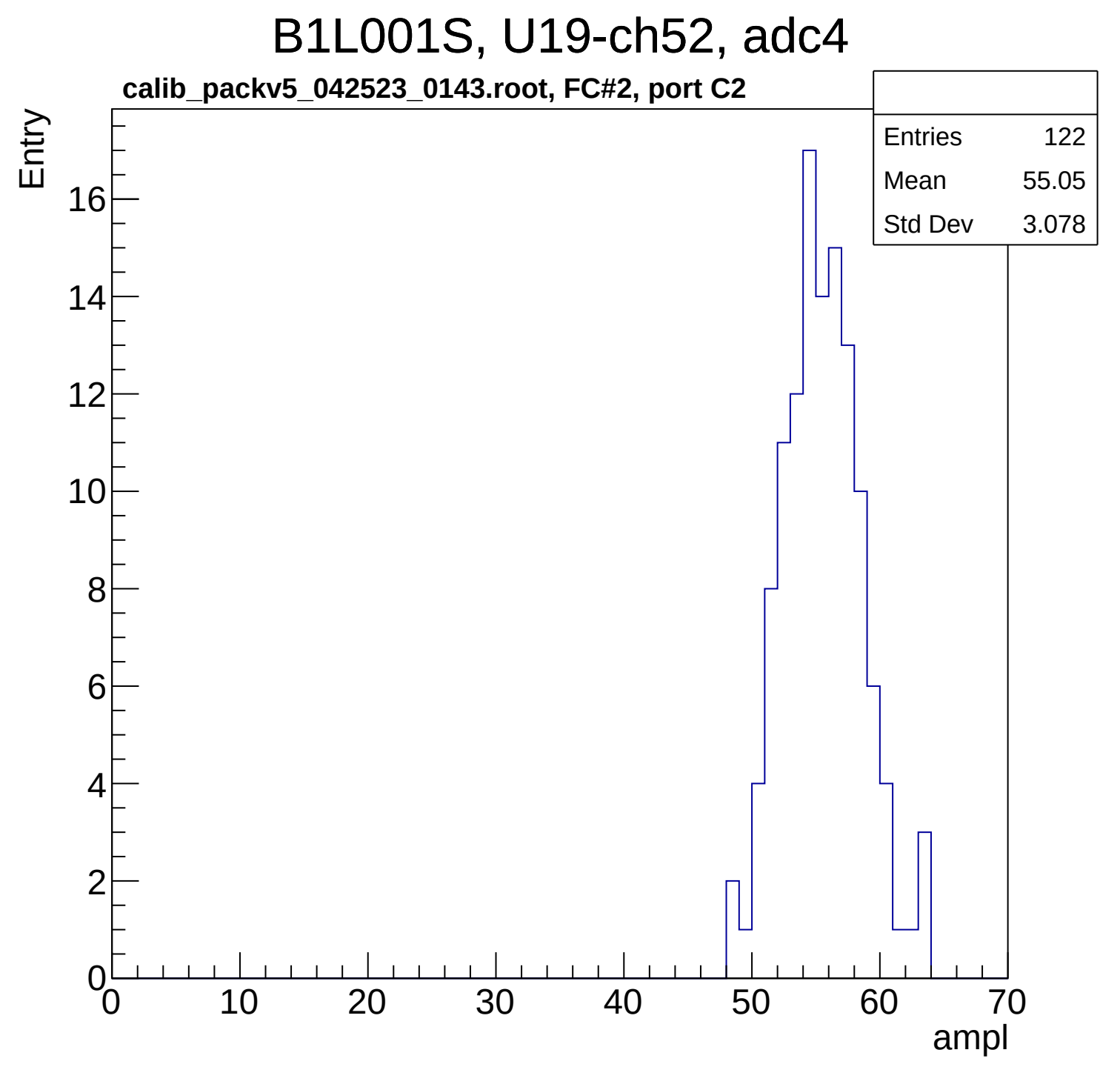
40
50
60
70


B1L001S, U19-ch52, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 111
Mean 48.95
Std Dev 2.885
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch52, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 122
Mean 55.05
Std Dev 3.078
Entry
0
2
4
6
8
10
12
14
16
0
10
20
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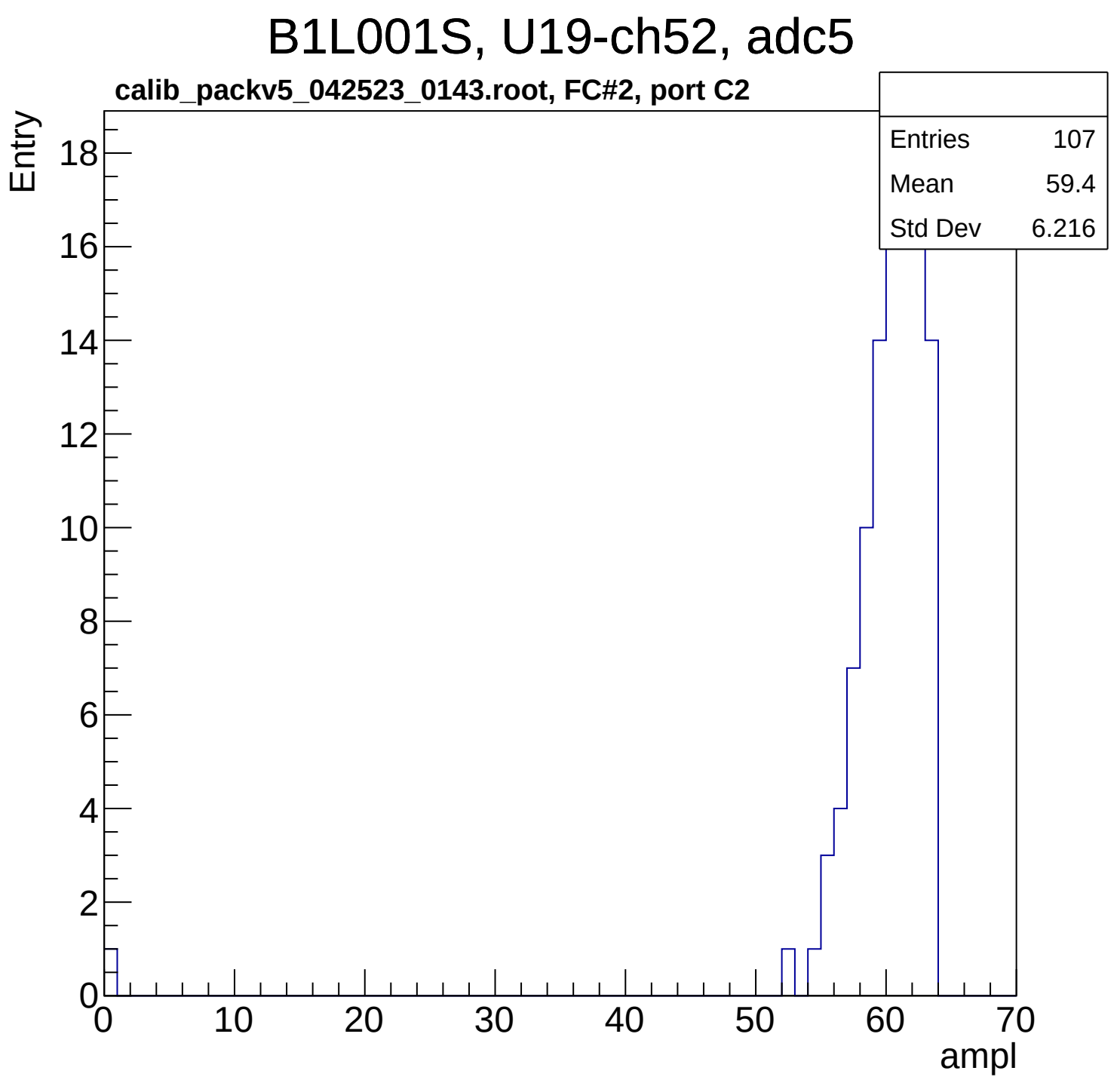
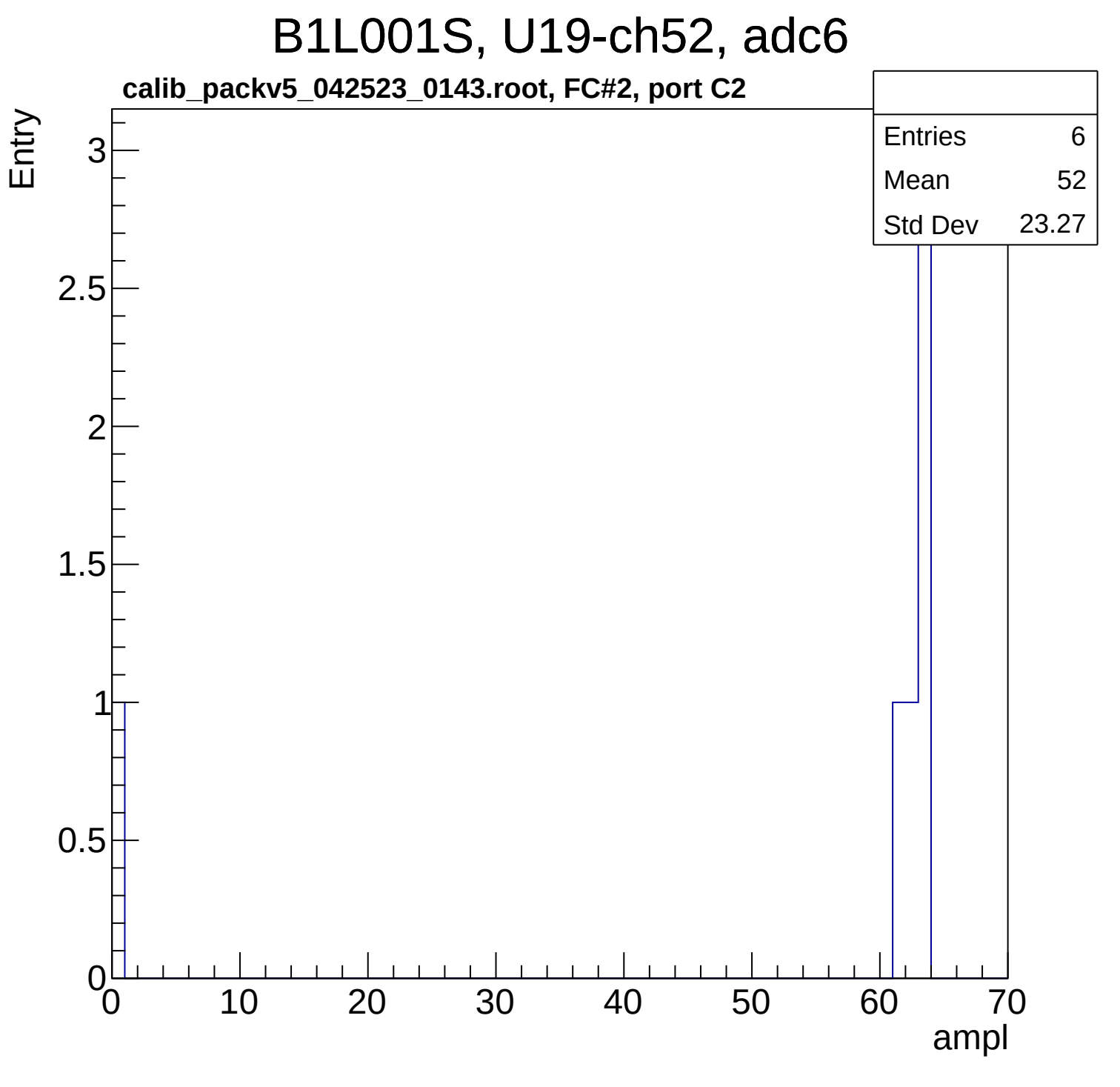
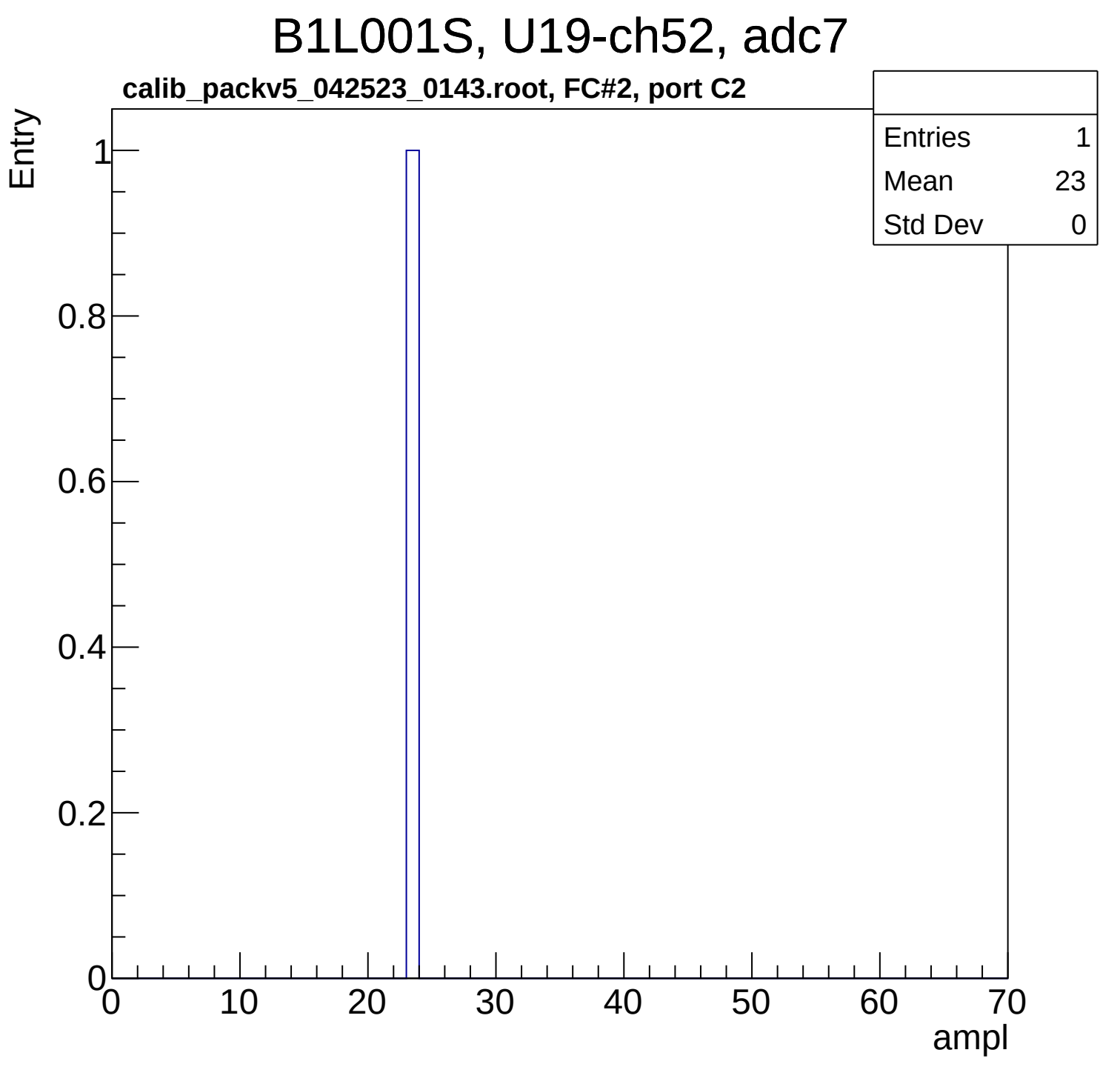
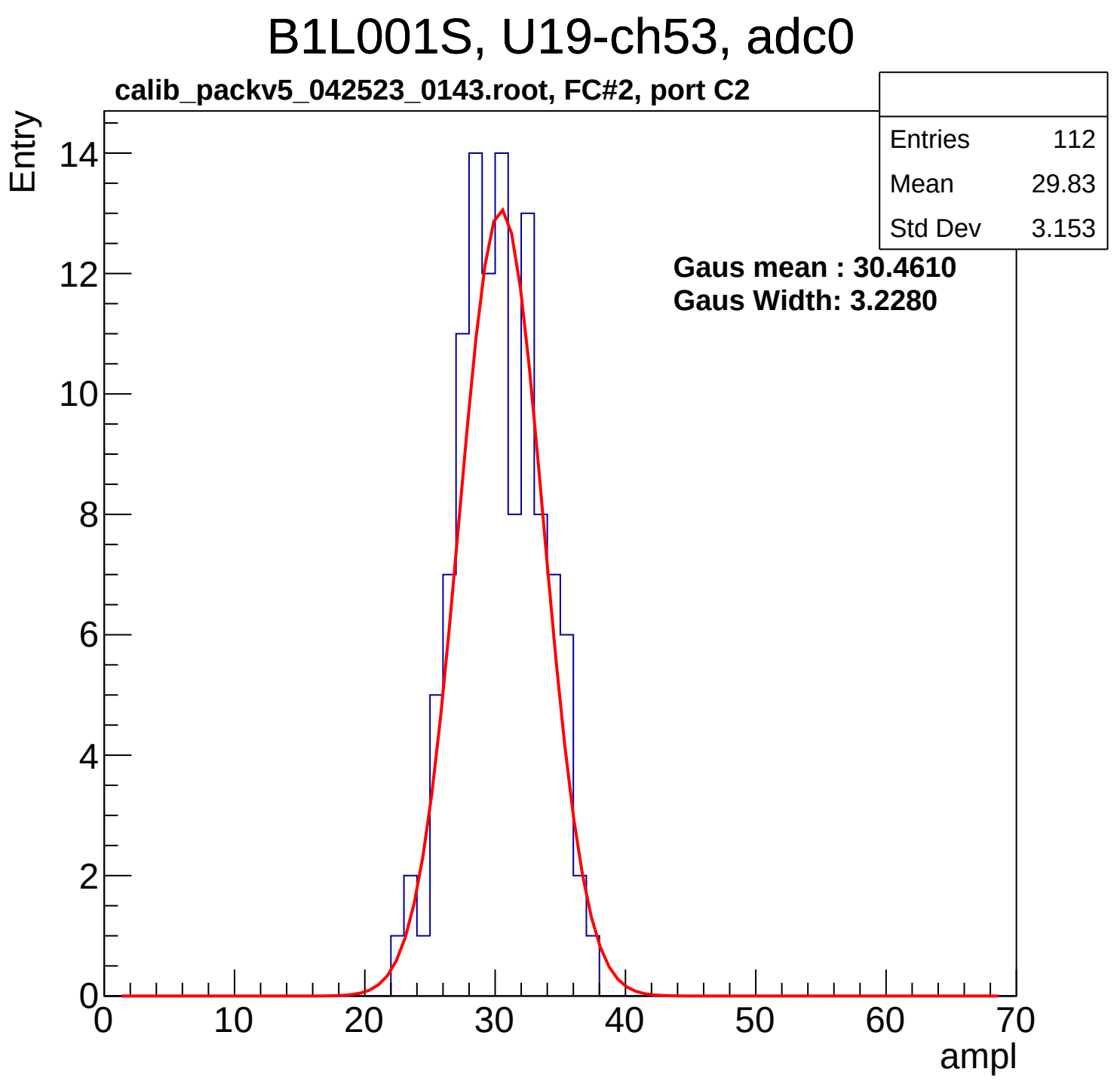
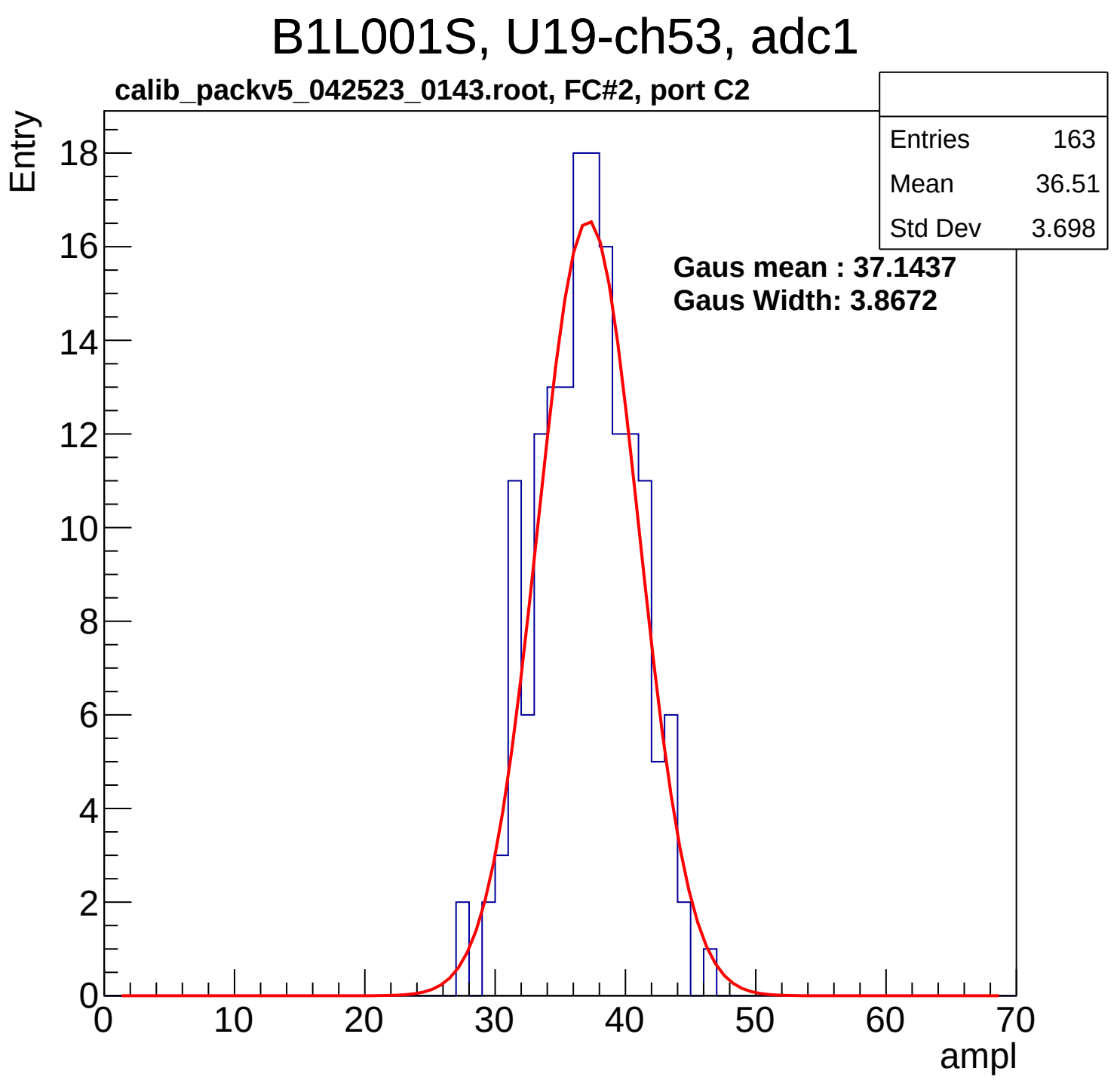
40
50
60
70
ampl

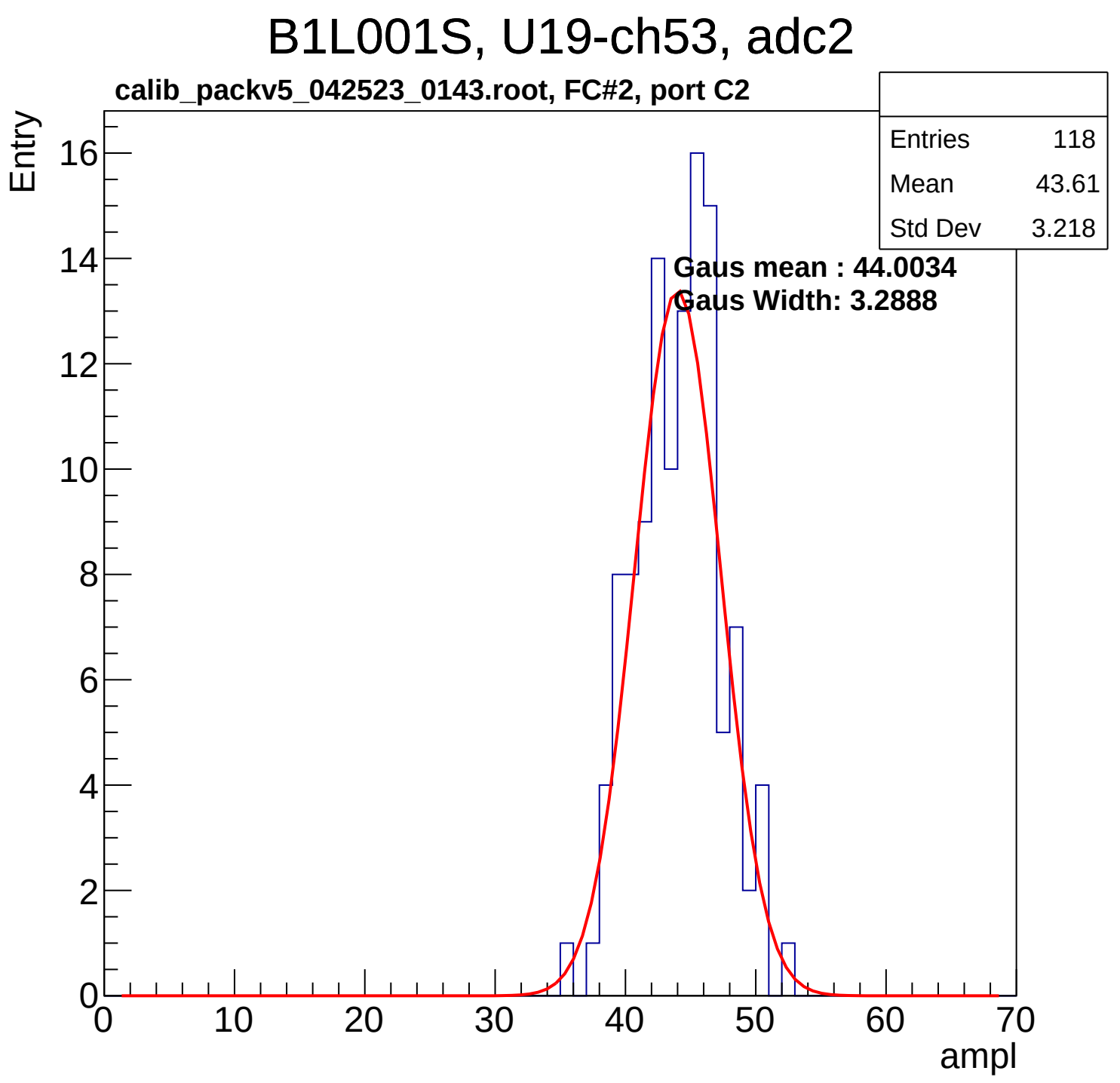

B1L001S, U19-ch52, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 107
Mean 59.4
Std Dev 6.216
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

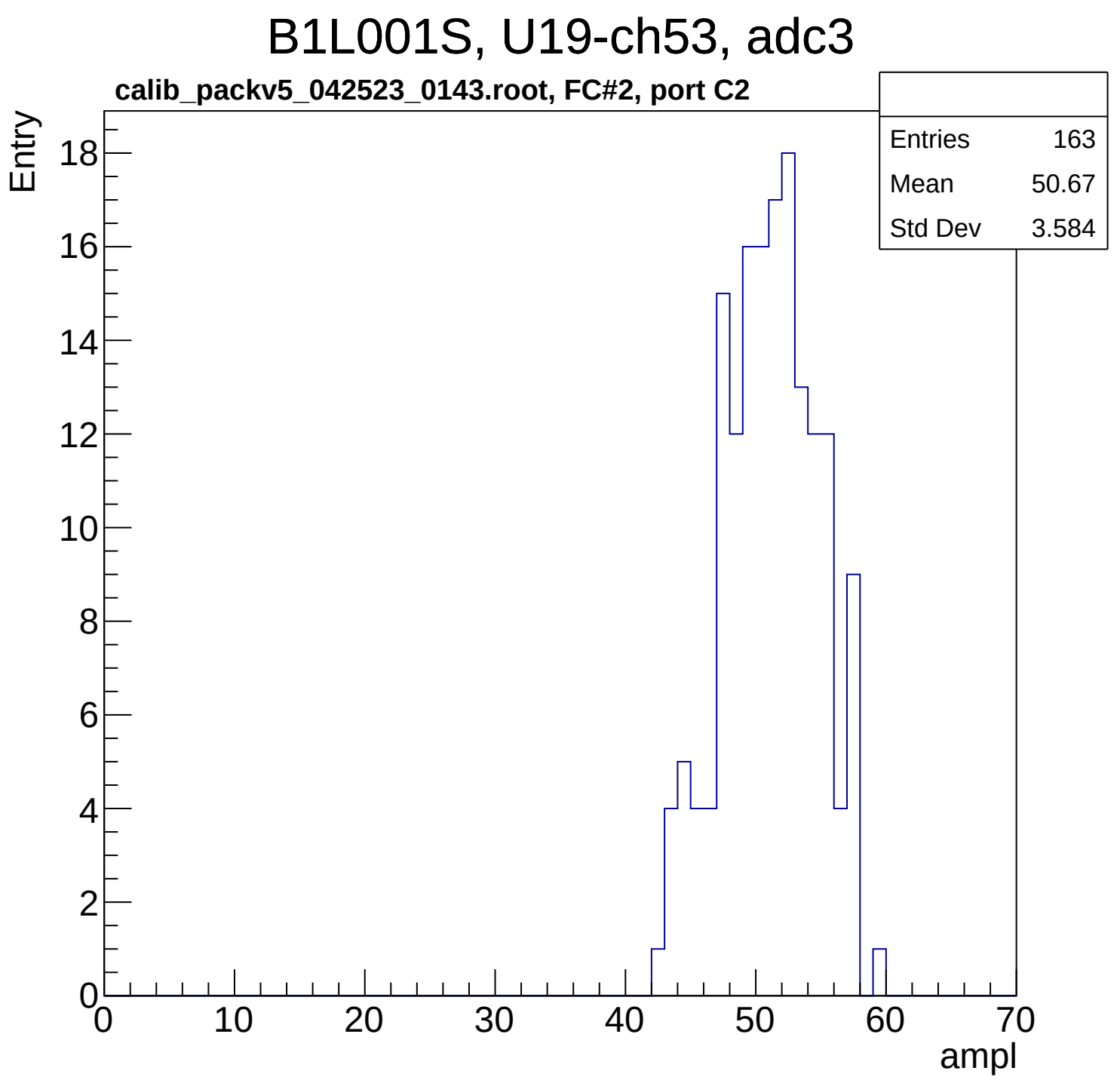

B1L001S, U19-ch52, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 6
Mean 52
Std Dev 23.27
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

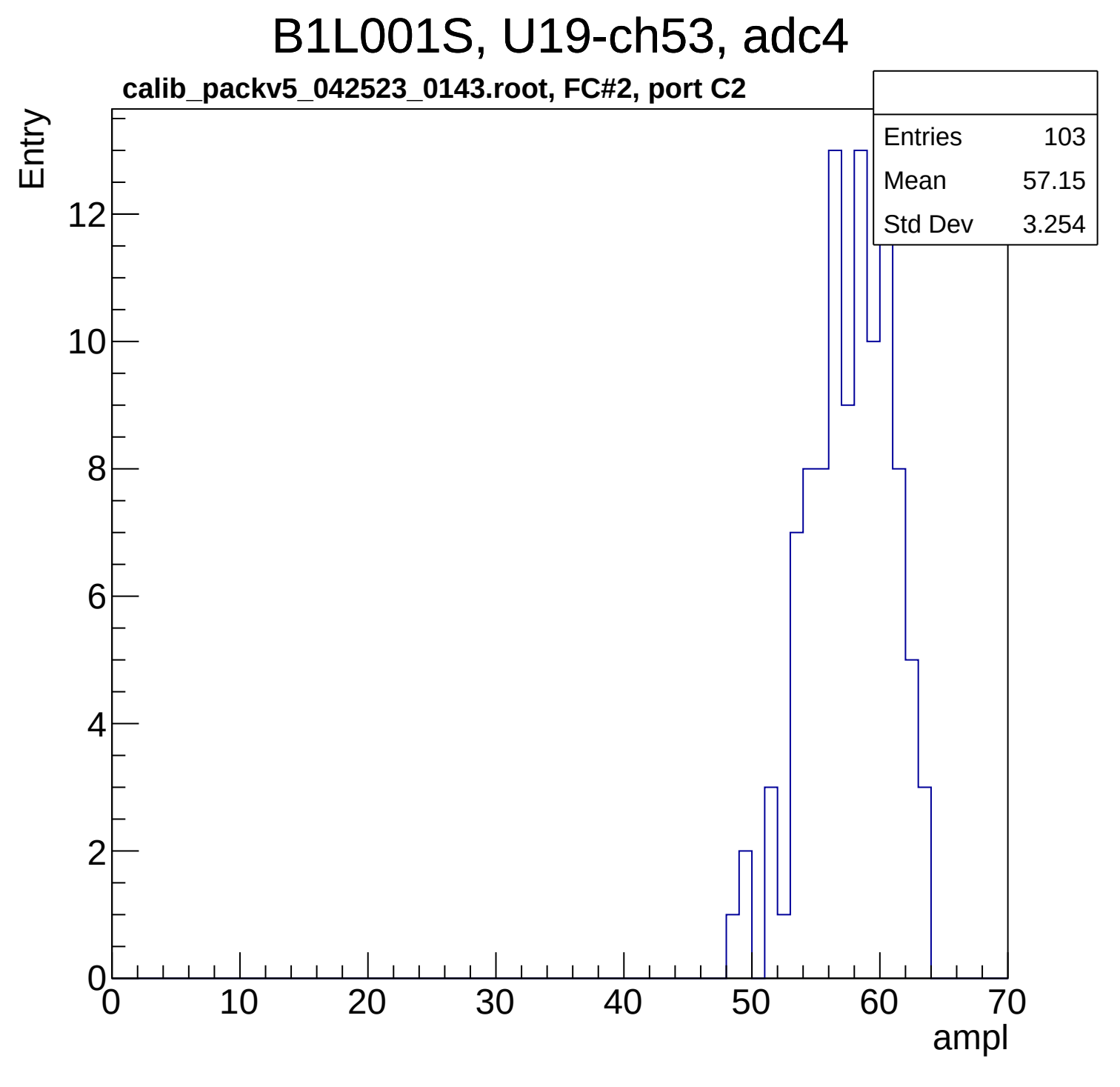

B1L001S, U19-ch52, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 23
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

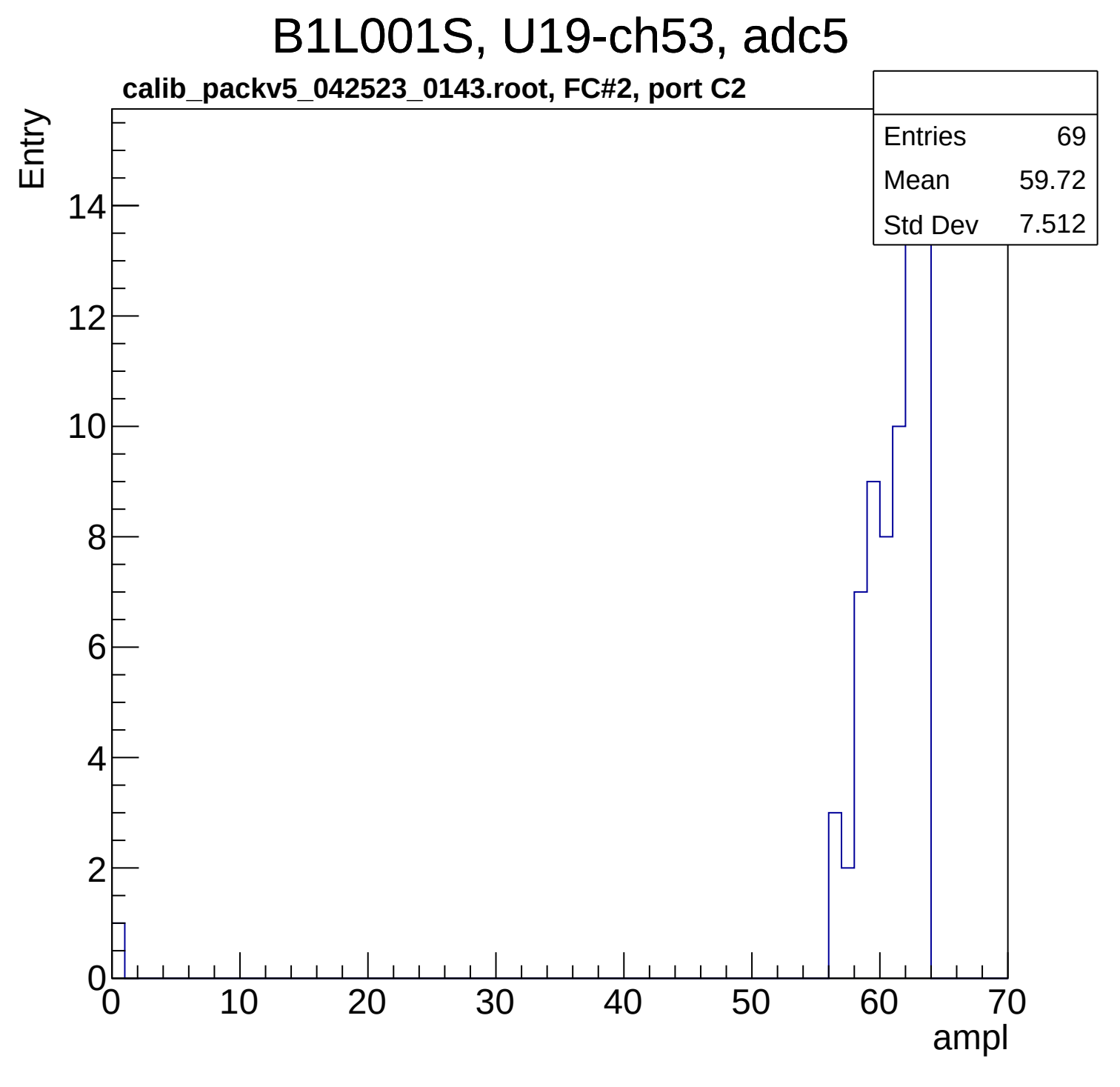

B1L001S, U19-ch53, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 112
Mean 29.83
Std Dev 3.153
Gaus mean : 30.4610
Gaus Width: 3.2280
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

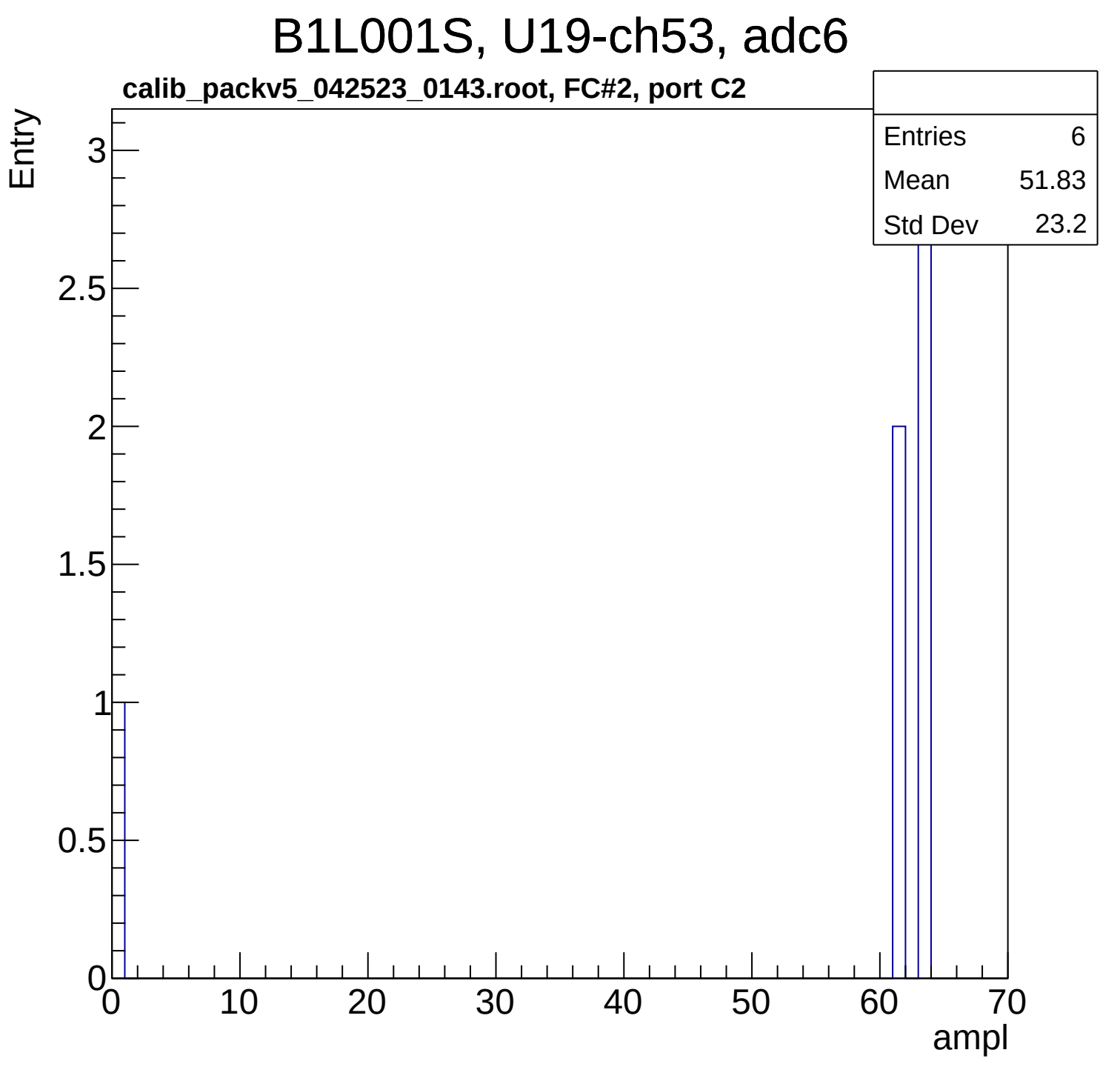

B1L001S, U19-ch53, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 163
Mean 36.51
Std Dev 3.698
Gaus mean : 37.1437
Gaus Width: 3.8672
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

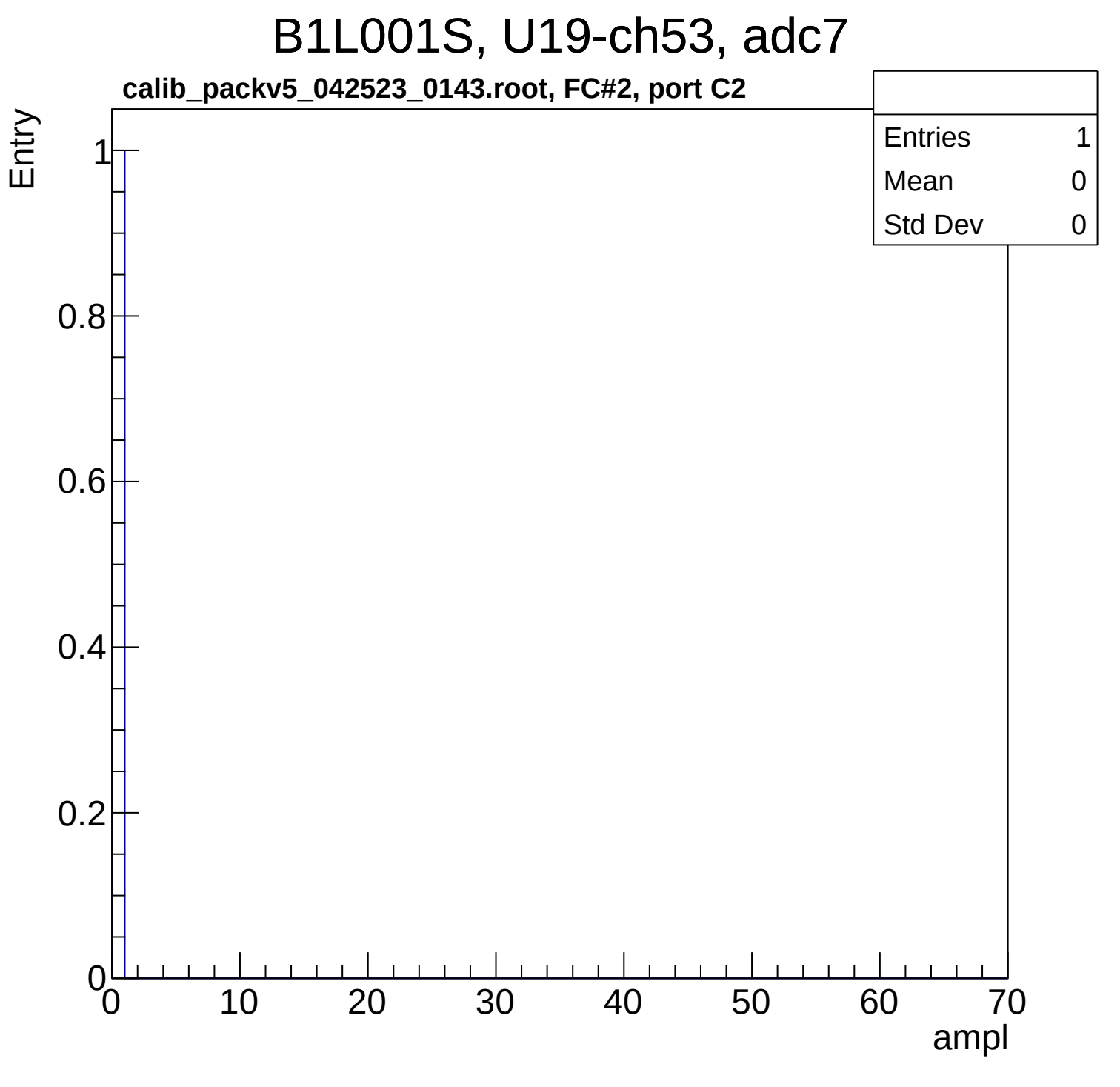

B1L001S, U19-ch53, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 118
Mean 43.61
Std Dev 3.218
Gaus mean : 44.0034
Gaus Width: 3.2888
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

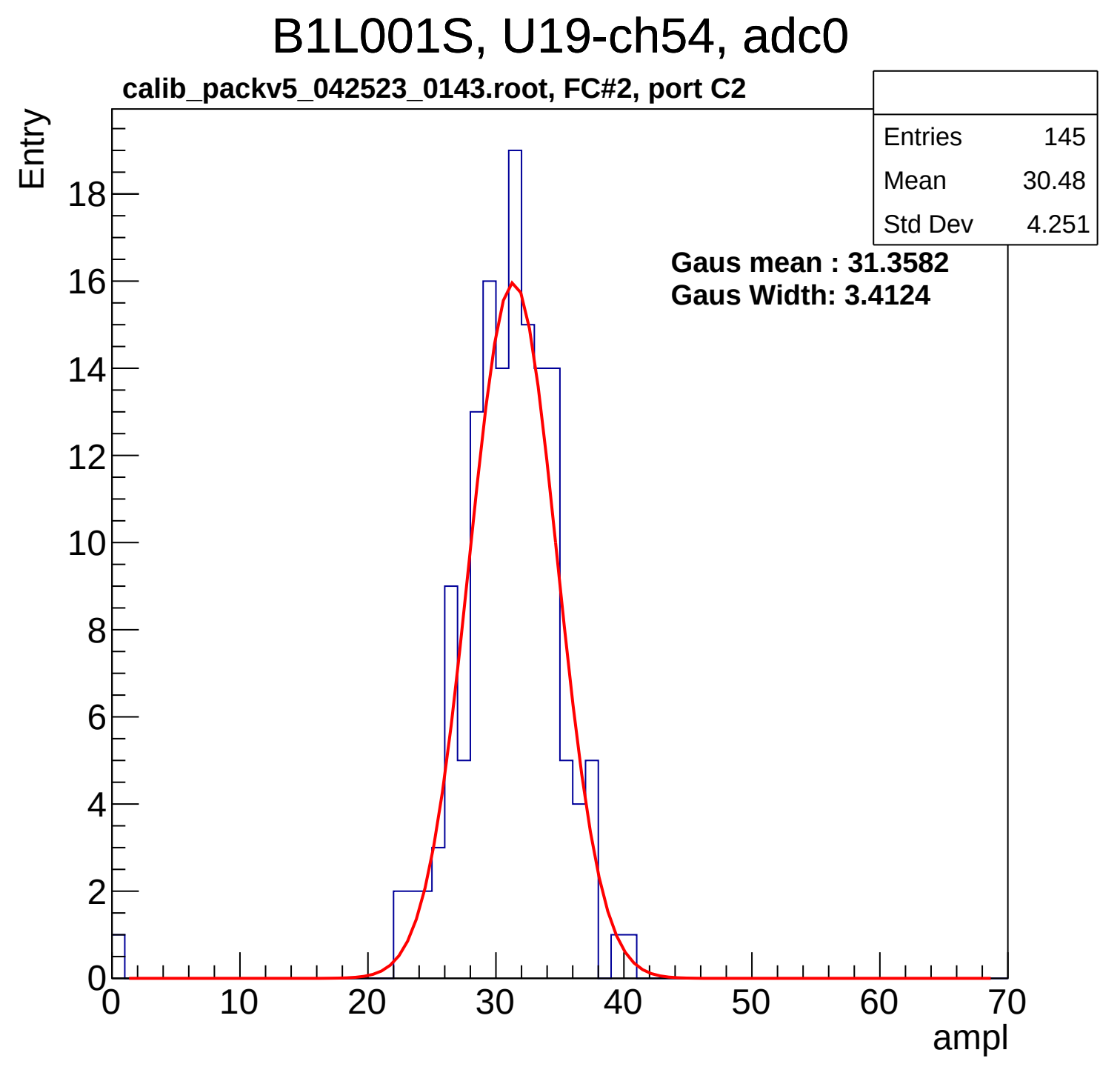

B1L001S, U19-ch53, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 163
Mean 50.67
Std Dev 3.584
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

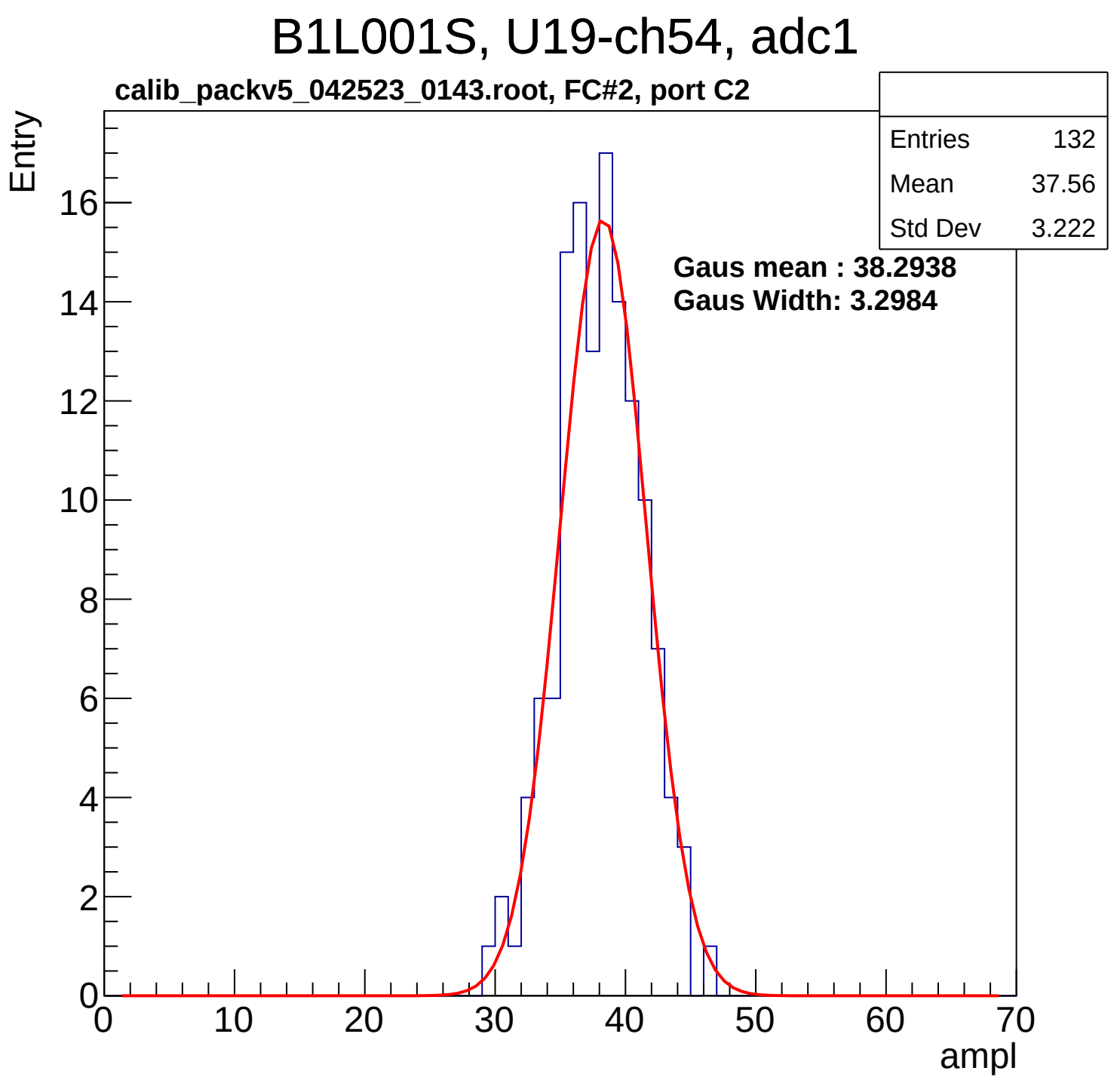

B1L001S, U19-ch53, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 103
Mean 57.15
Std Dev 3.254
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl

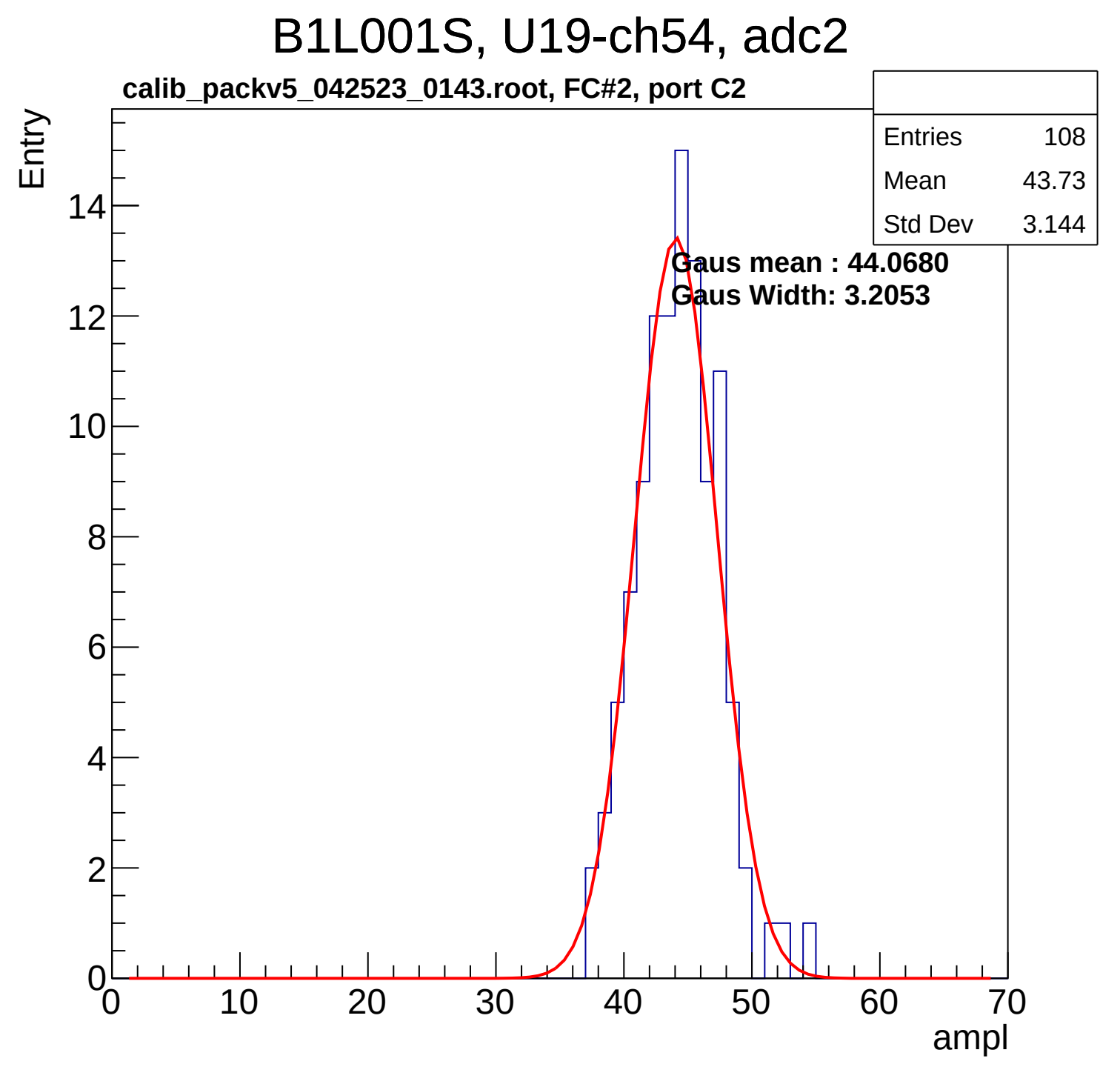

B1L001S, U19-ch53, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 69
Mean 59.72
Std Dev 7.512
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

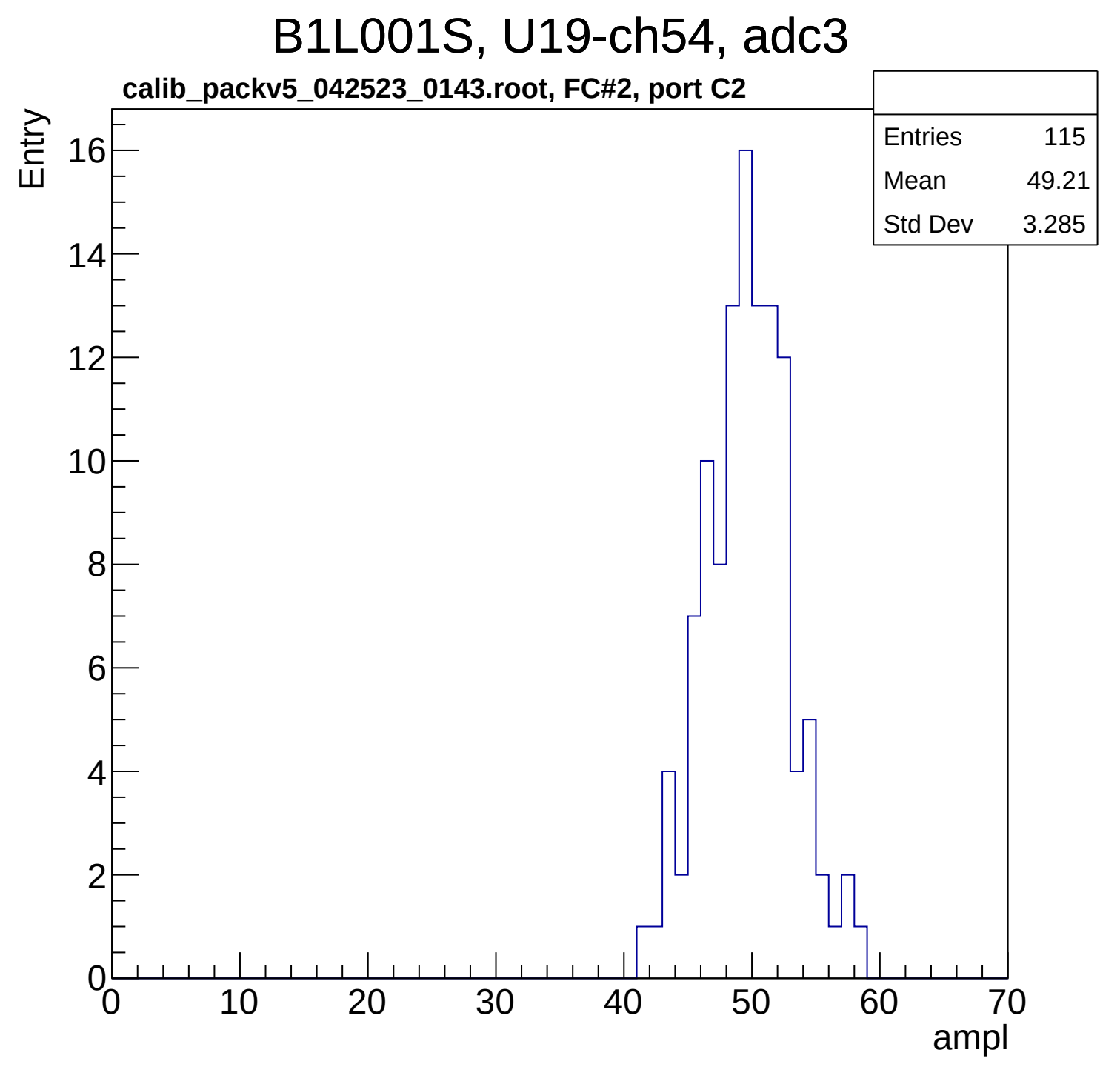

B1L001S, U19-ch53, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 6
Mean 51.83
Std Dev 23.2
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

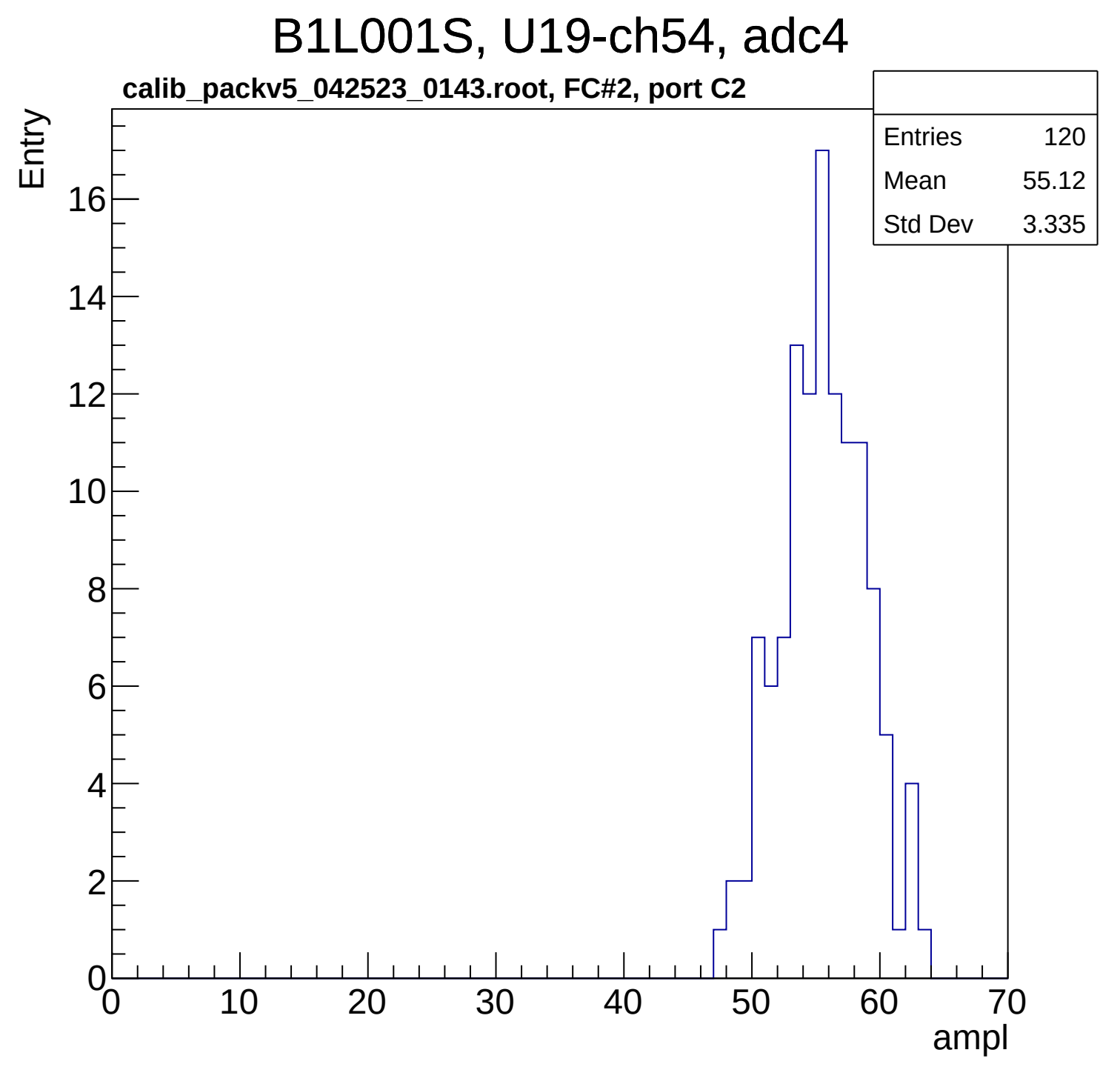

B1L001S, U19-ch53, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

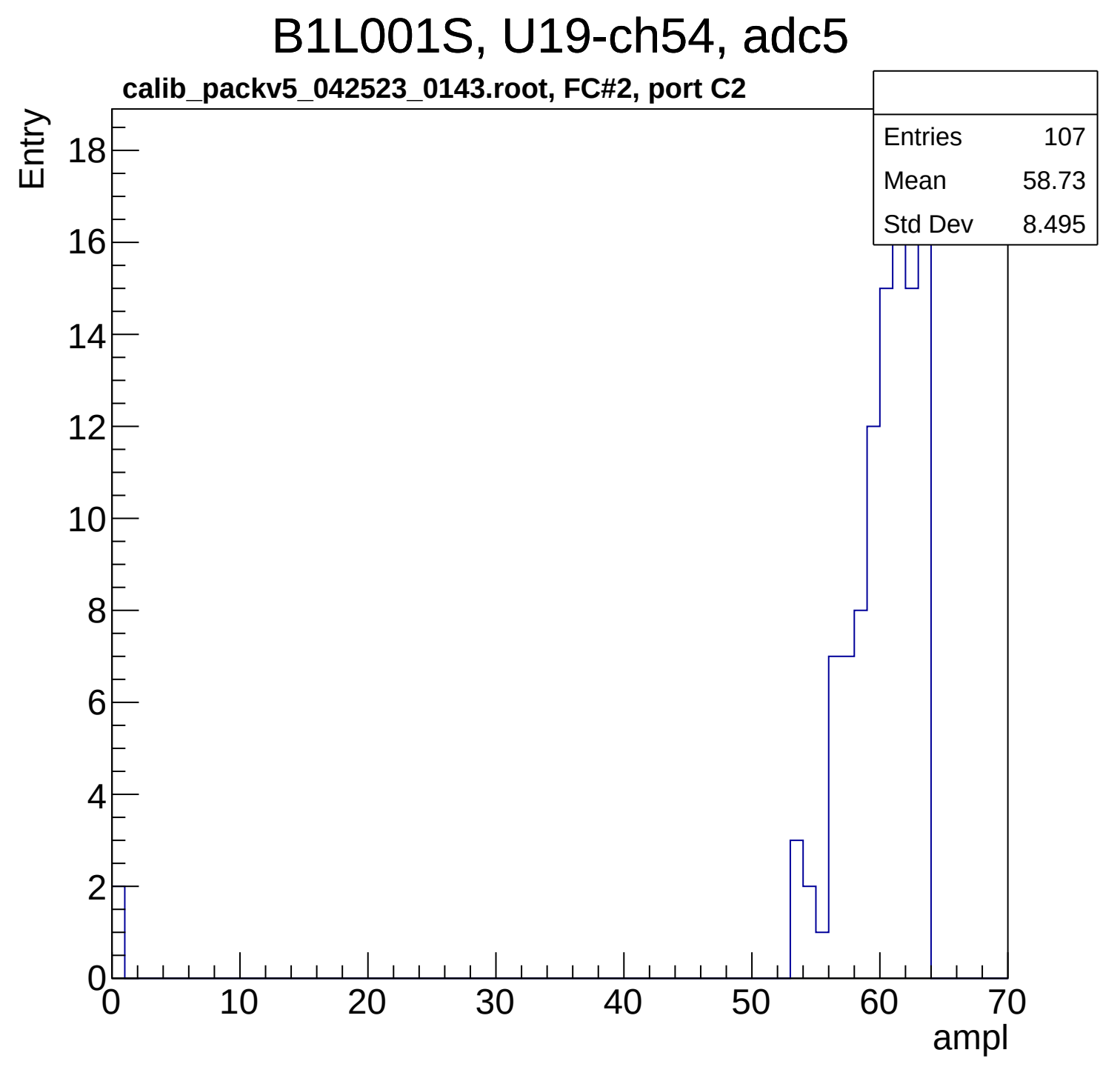

B1L001S, U19-ch54, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 145
Mean 30.48
Std Dev 4.251
Gaus mean : 31.3582
Gaus Width: 3.4124
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

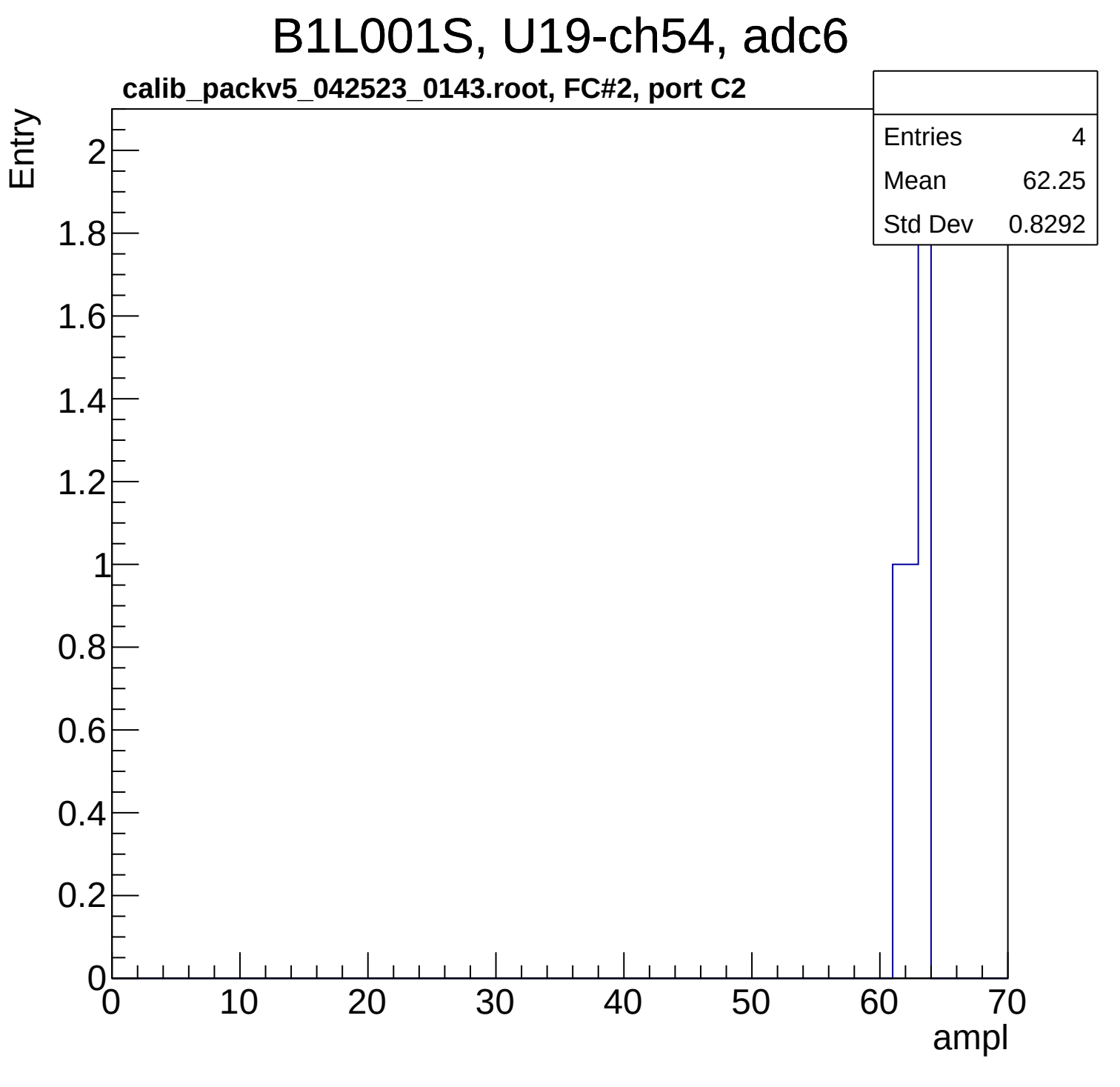

B1L001S, U19-ch54, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 132
Mean 37.56
Std Dev 3.222
Gaus mean : 38.2938
Gaus Width: 3.2984
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

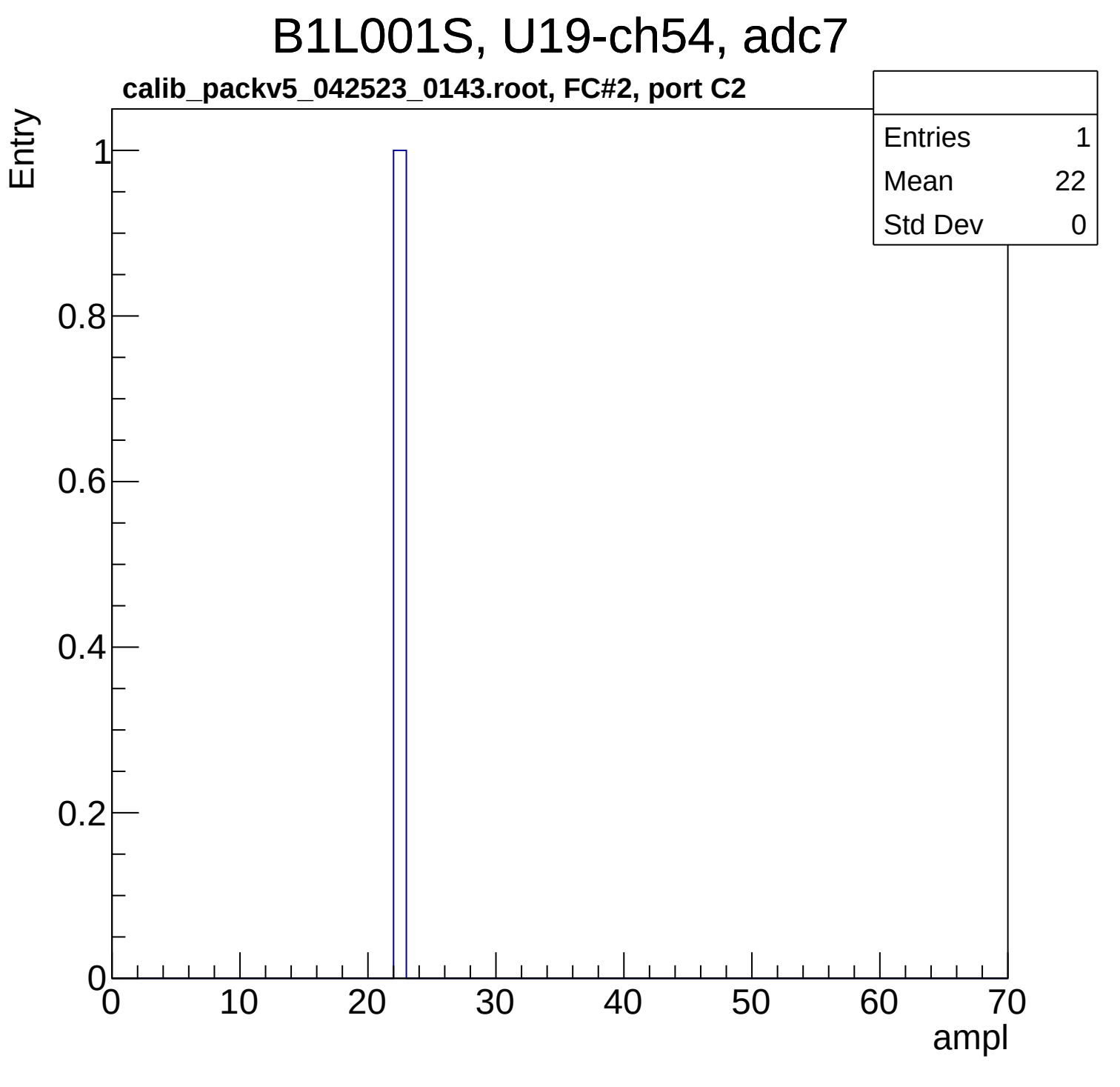

B1L001S, U19-ch54, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 108
Mean 43.73
Std Dev 3.144
Gaus mean : 44.0680
Gaus Width: 3.2053
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

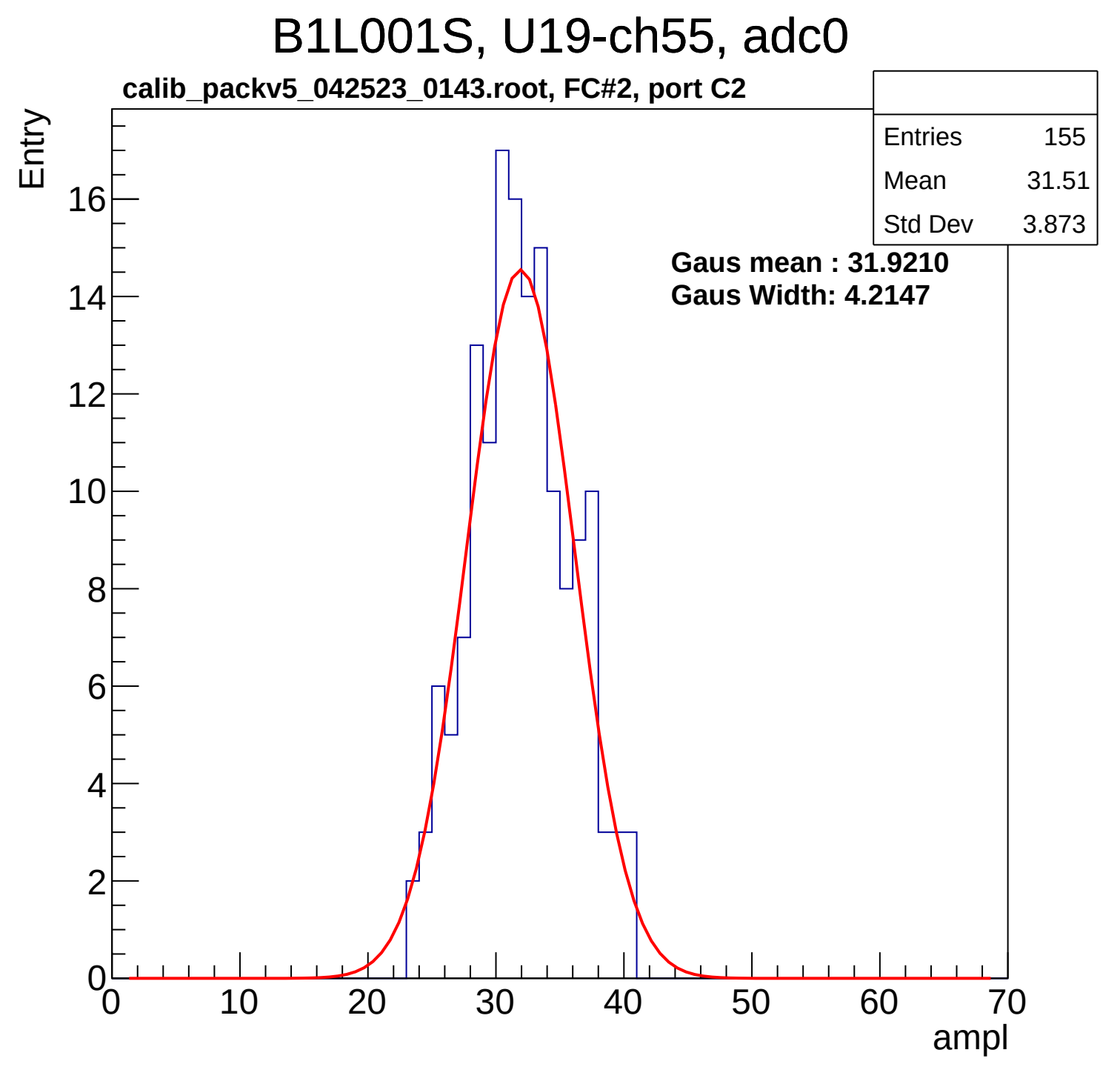

B1L001S, U19-ch54, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 115
Mean 49.21
Std Dev 3.285
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70


B1L001S, U19-ch54, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 120
Mean 55.12
Std Dev 3.335
Entry
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch54, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 107
Mean 58.73
Std Dev 8.495
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70


B1L001S, U19-ch54, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 4
Mean 62.25
Std Dev 0.8292
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L001S, U19-ch54, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 22
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch55, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 155
Mean 31.51
Std Dev 3.873
Gaus mean : 31.9210
Gaus Width: 4.2147
Entry
ampl
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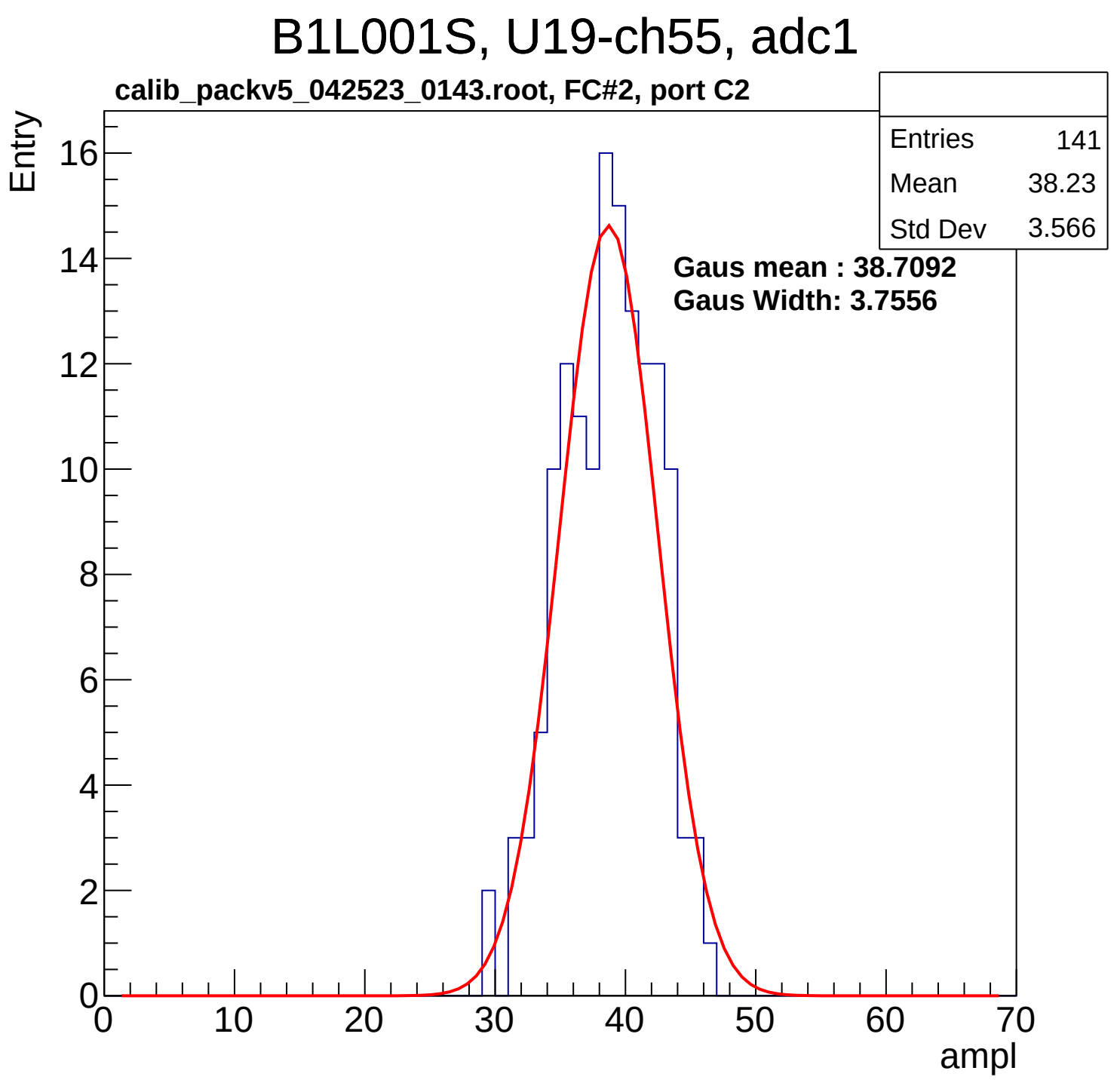
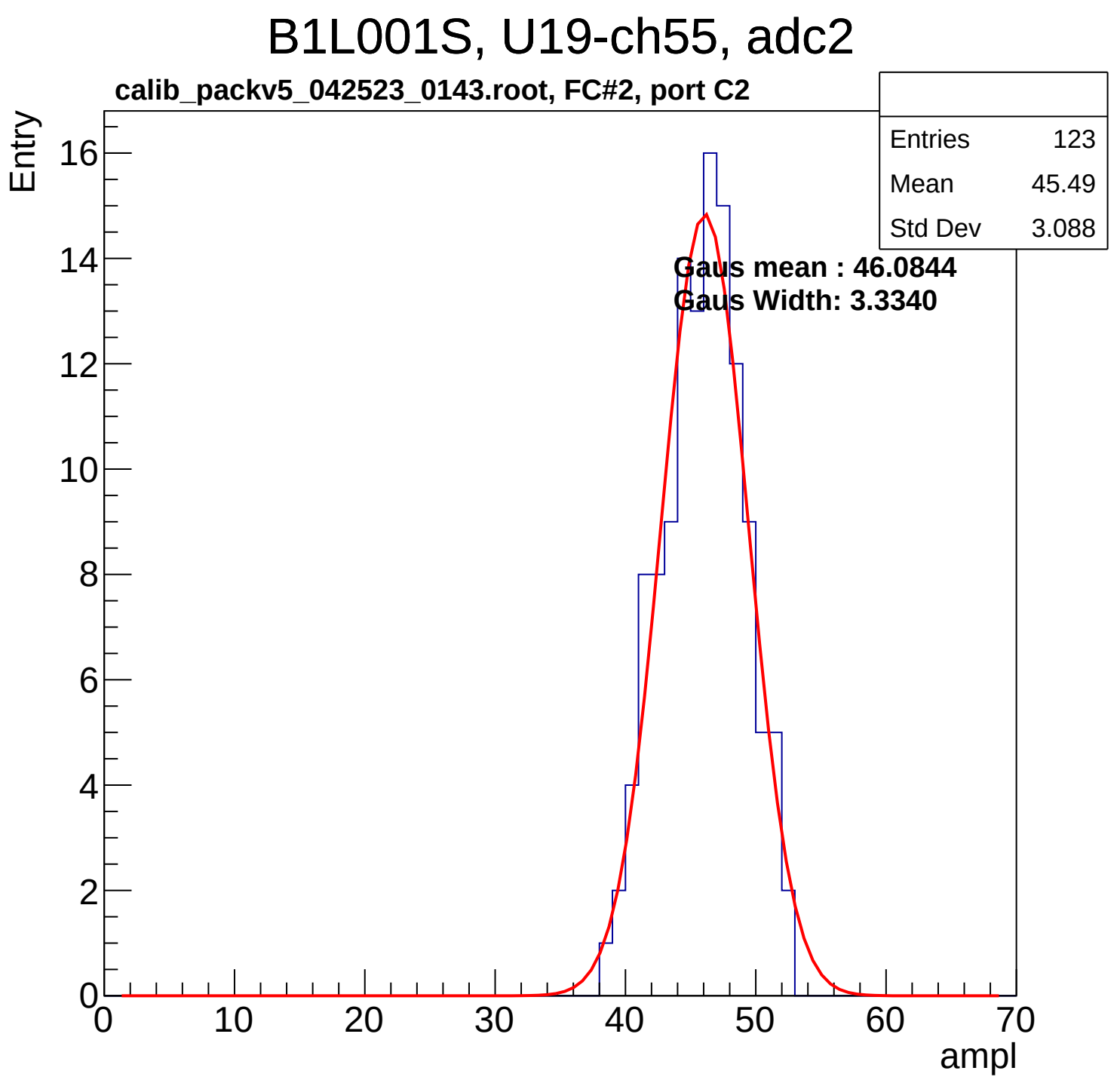
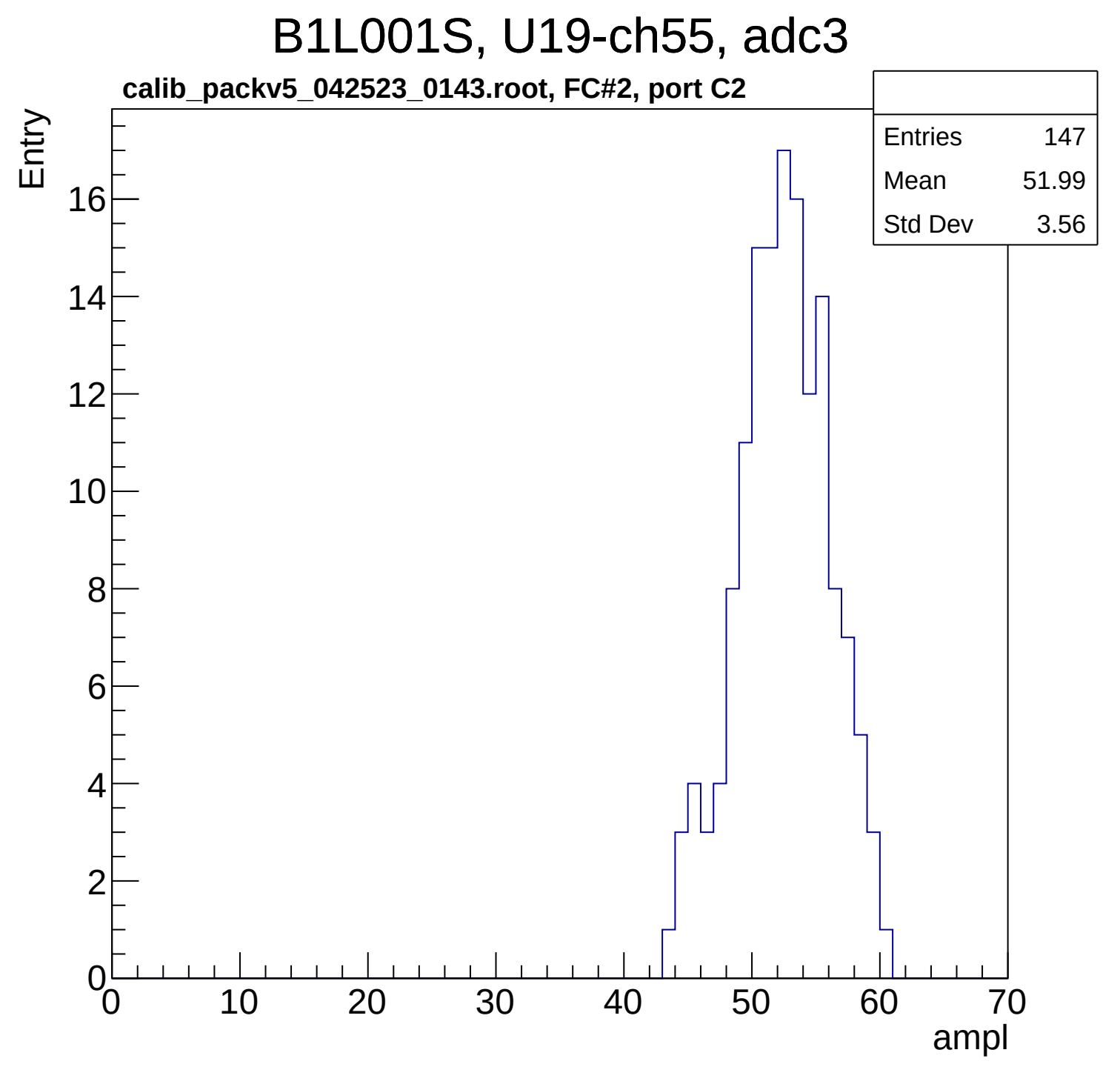
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70


B1L001S, U19-ch55, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 141
Mean 38.23
Std Dev 3.566
Gaus mean : 38.7092
Gaus Width: 3.7556
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70


B1L001S, U19-ch55, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 123
Mean 45.49
Std Dev 3.088
Gaus mean : 46.0844
Gaus Width: 3.3340
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70


B1L001S, U19-ch55, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 147
Mean 51.99
Std Dev 3.56
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
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40
50
60
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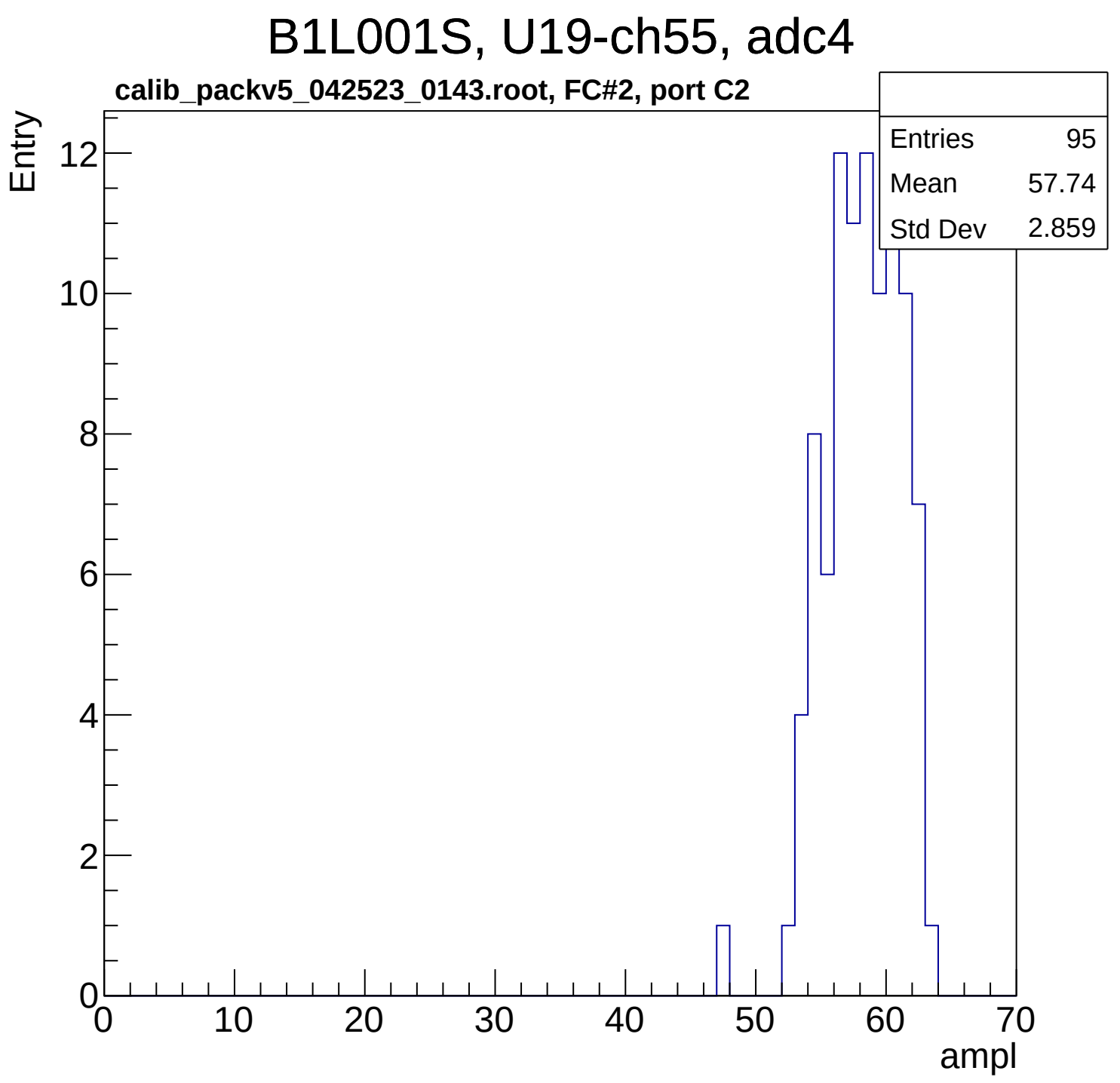
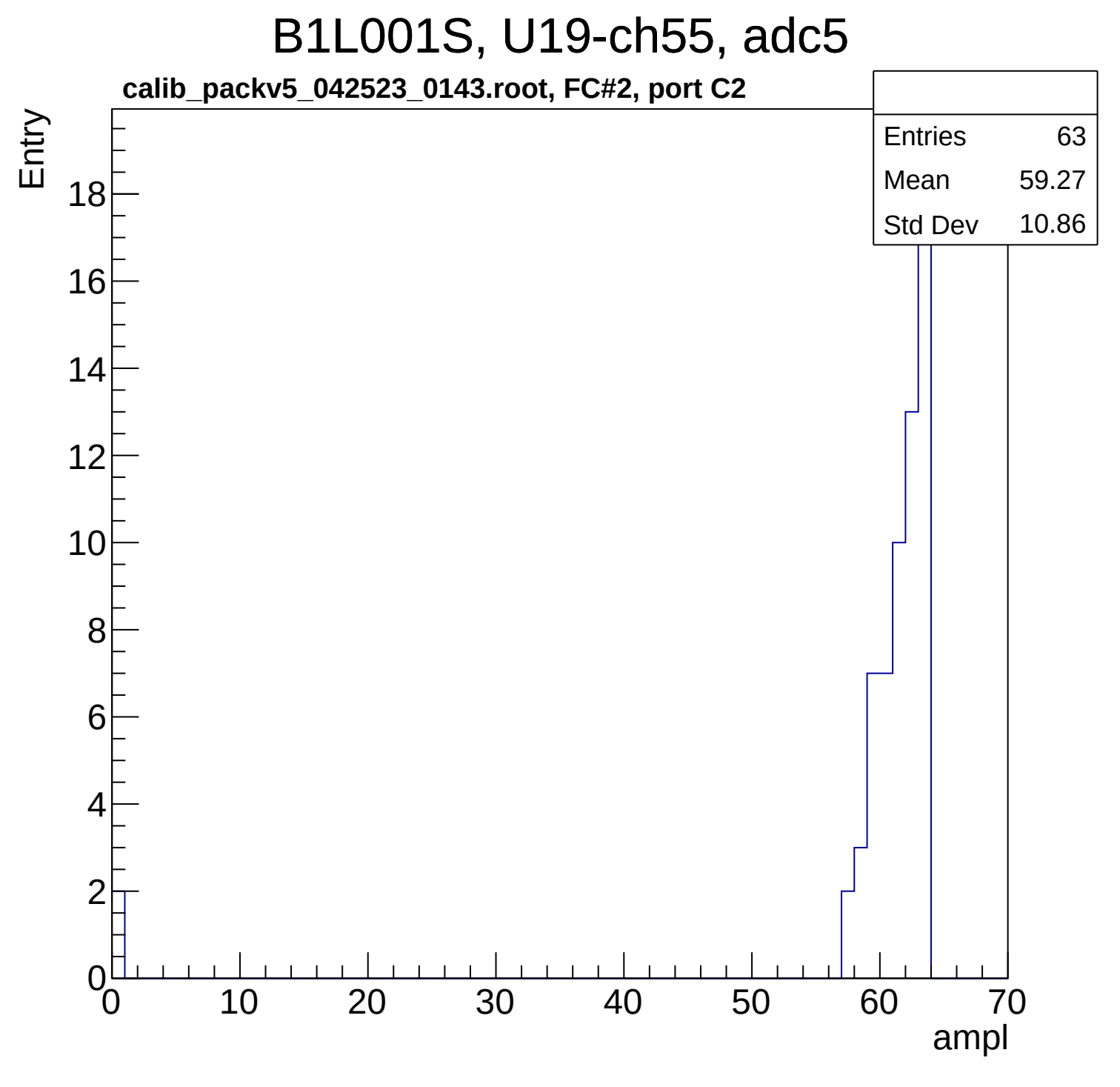
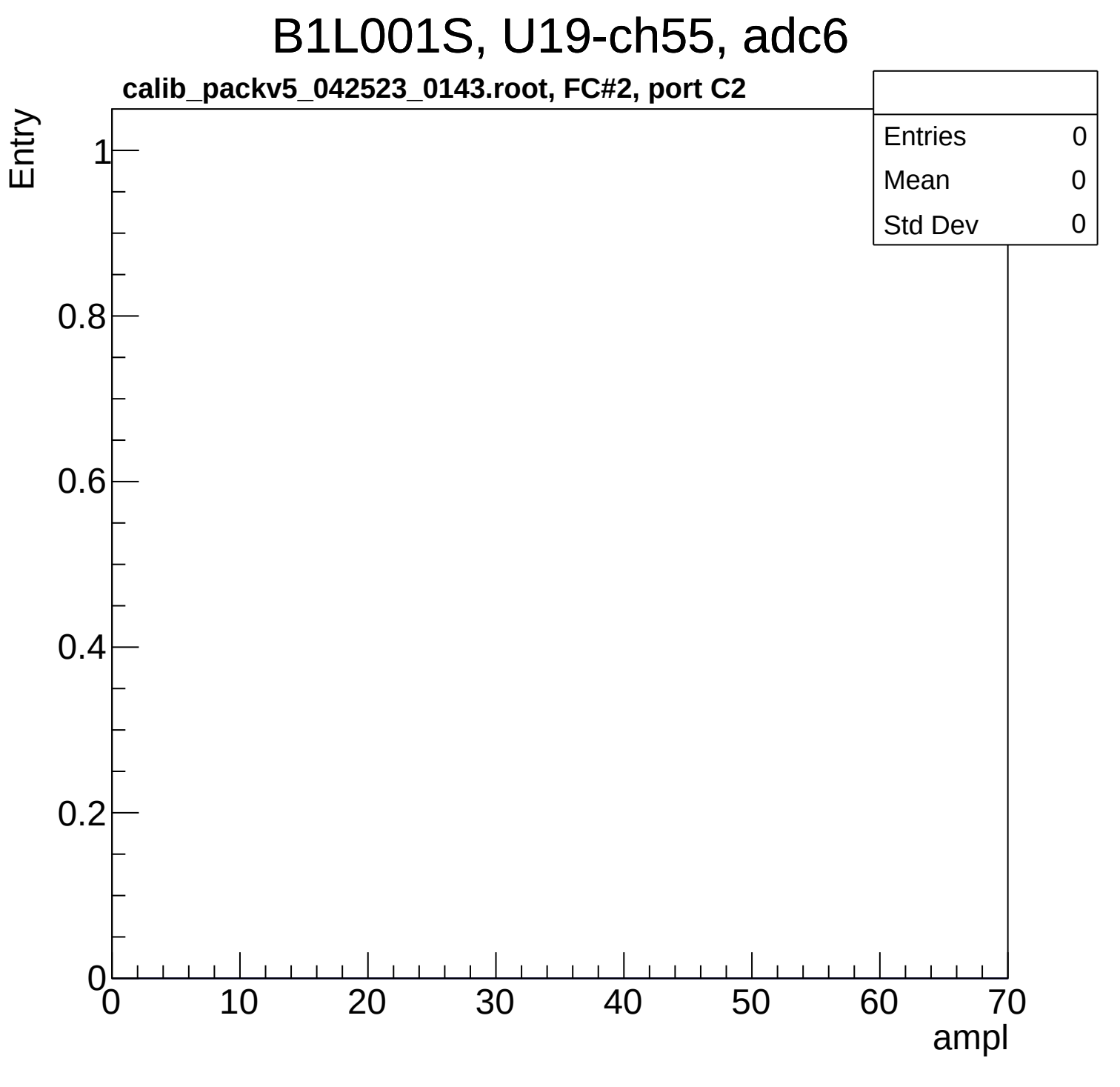
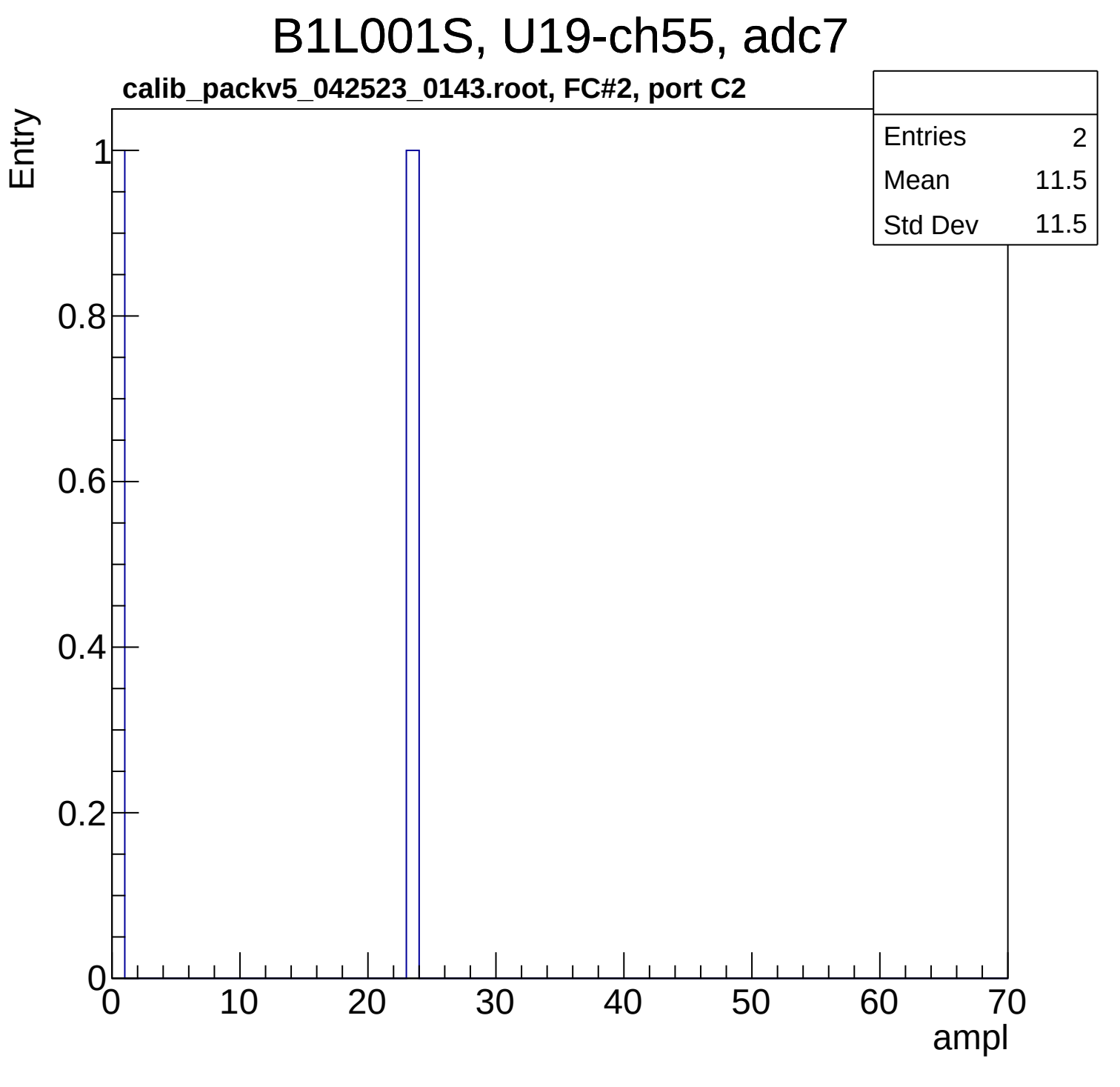
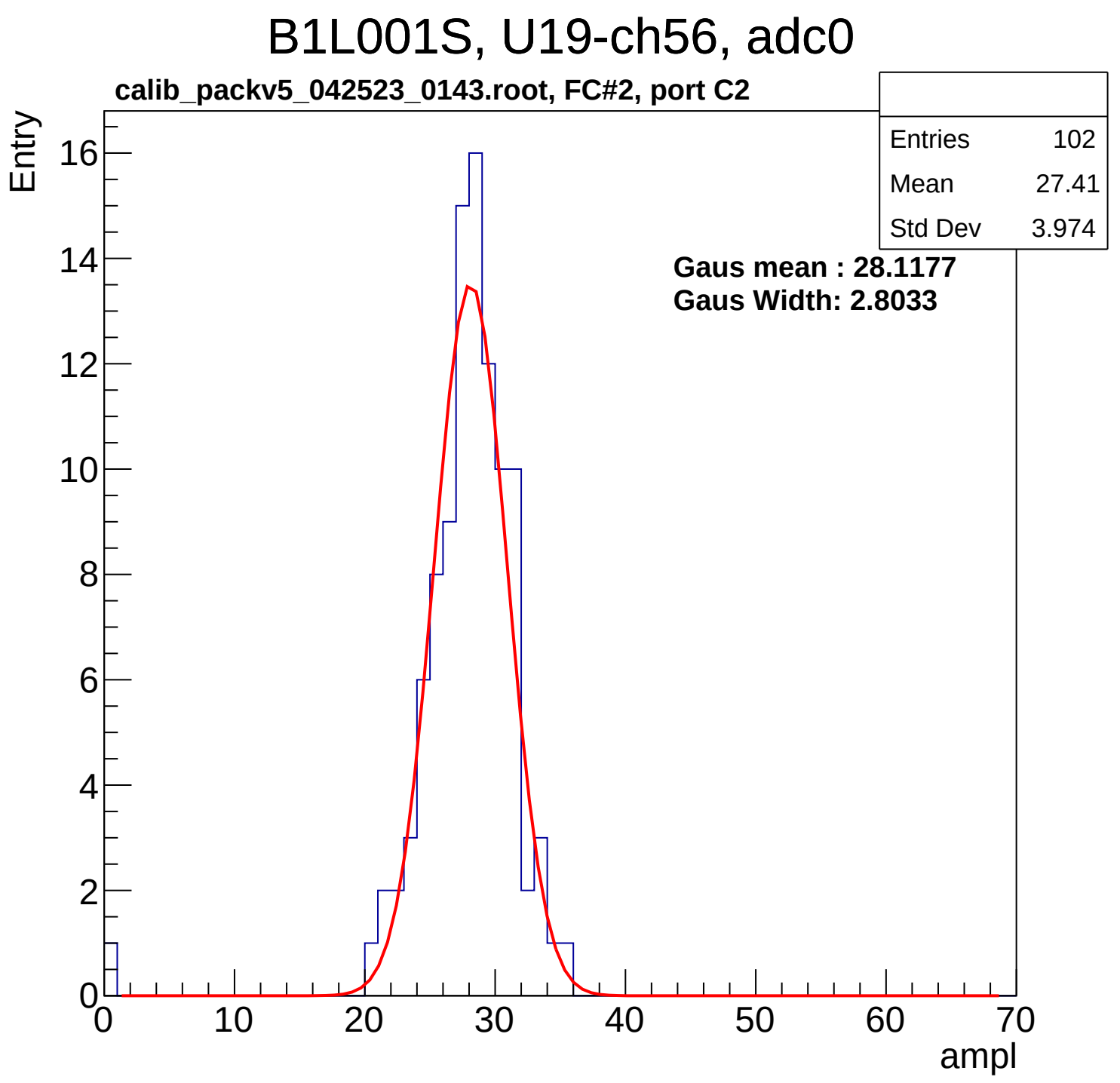
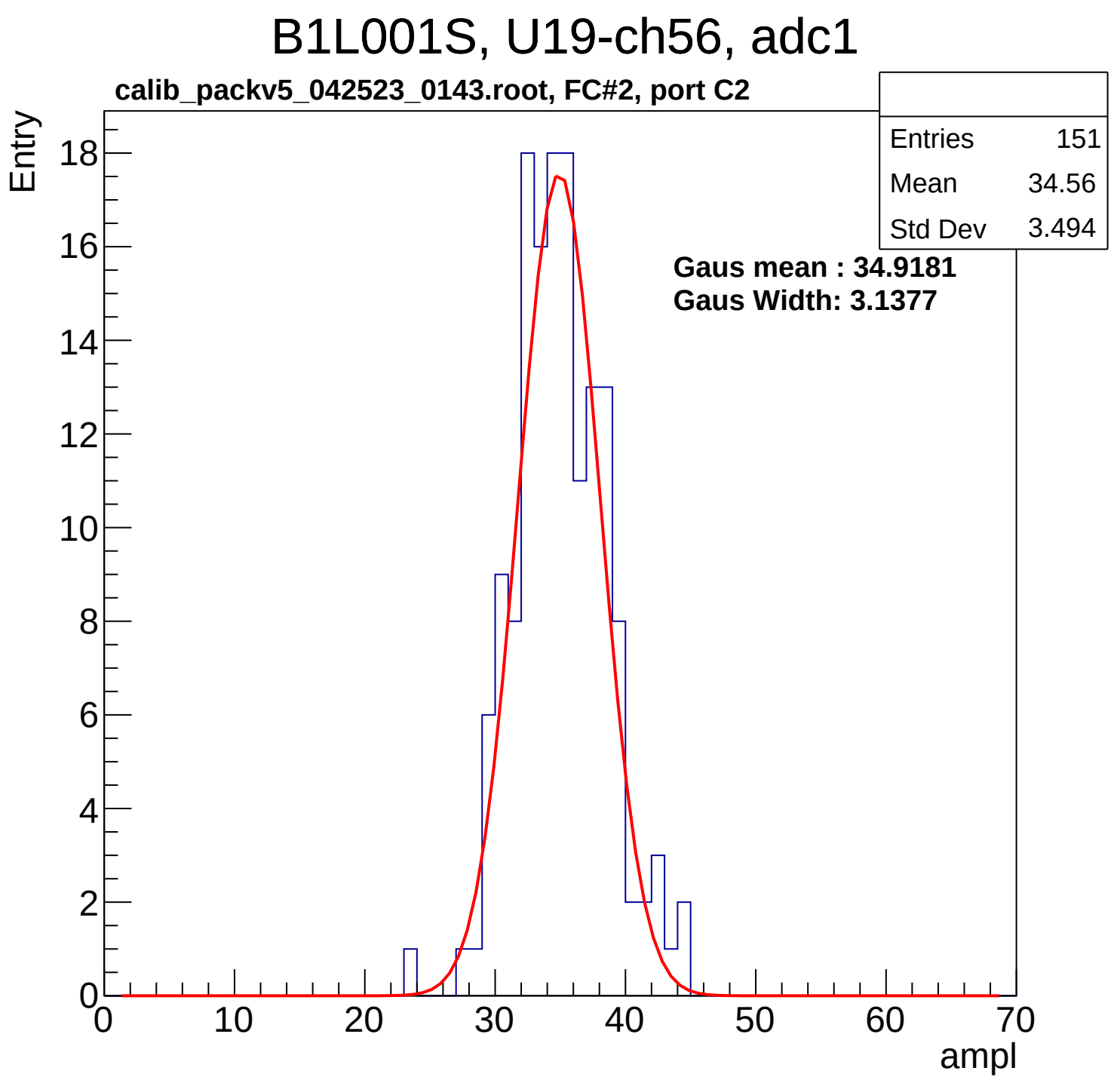

B1L001S, U19-ch55, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 95
Mean 57.74
Std Dev 2.859
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl

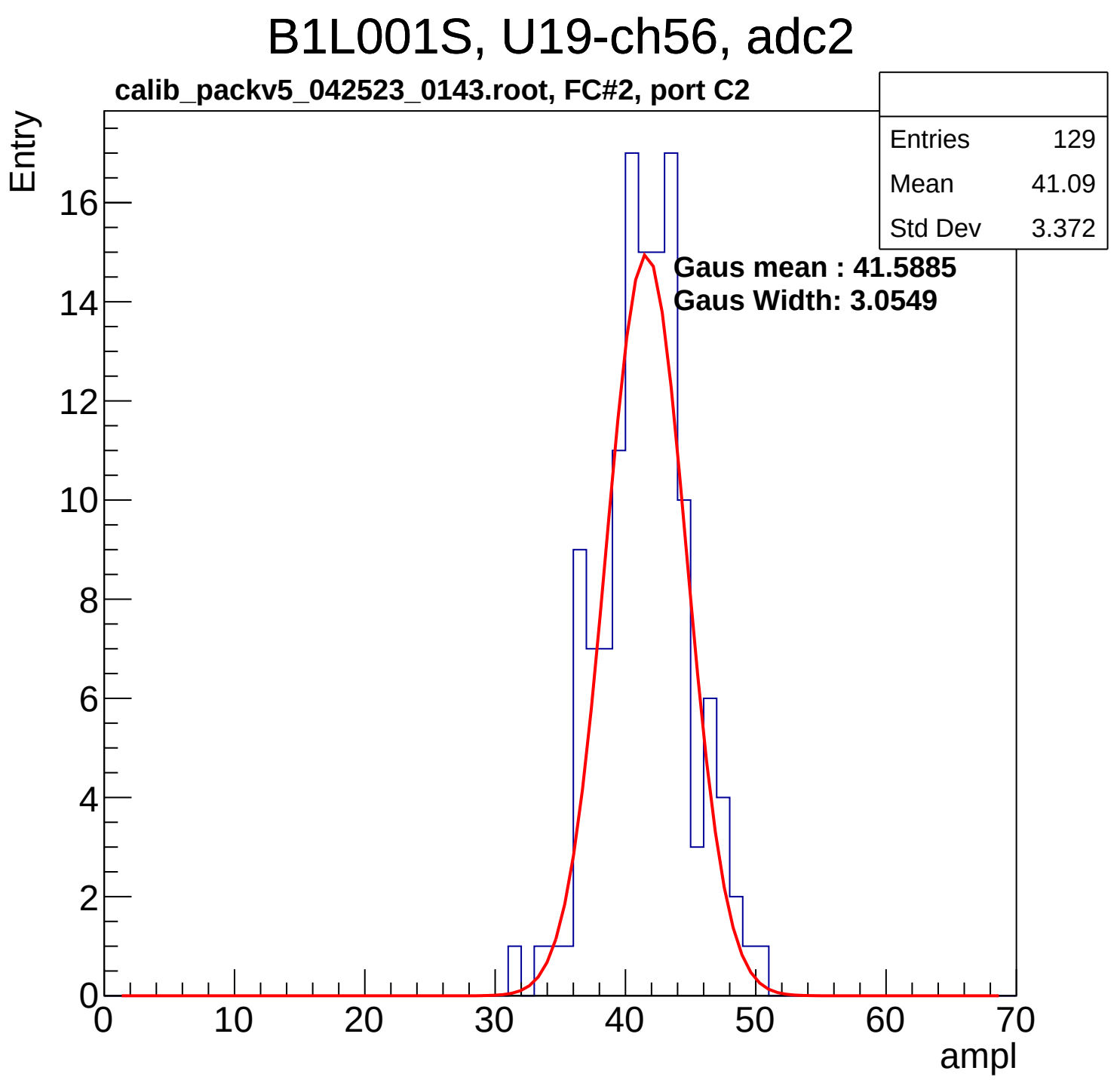

B1L001S, U19-ch55, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 63
Mean 59.27
Std Dev 10.86
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch55, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch55, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 11.5
Std Dev 11.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch56, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 102
Mean 27.41
Std Dev 3.974
Gaus mean : 28.1177
Gaus Width: 2.8033
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70


B1L001S, U19-ch56, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 151
Mean 34.56
Std Dev 3.494
Gaus mean : 34.9181
Gaus Width: 3.1377
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70


B1L001S, U19-ch56, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 129
Mean 41.09
Std Dev 3.372
Gaus mean : 41.5885
Gaus Width: 3.0549
Entry
ampl
0
2
4
6
8
10
12
14
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0
10
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40
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60
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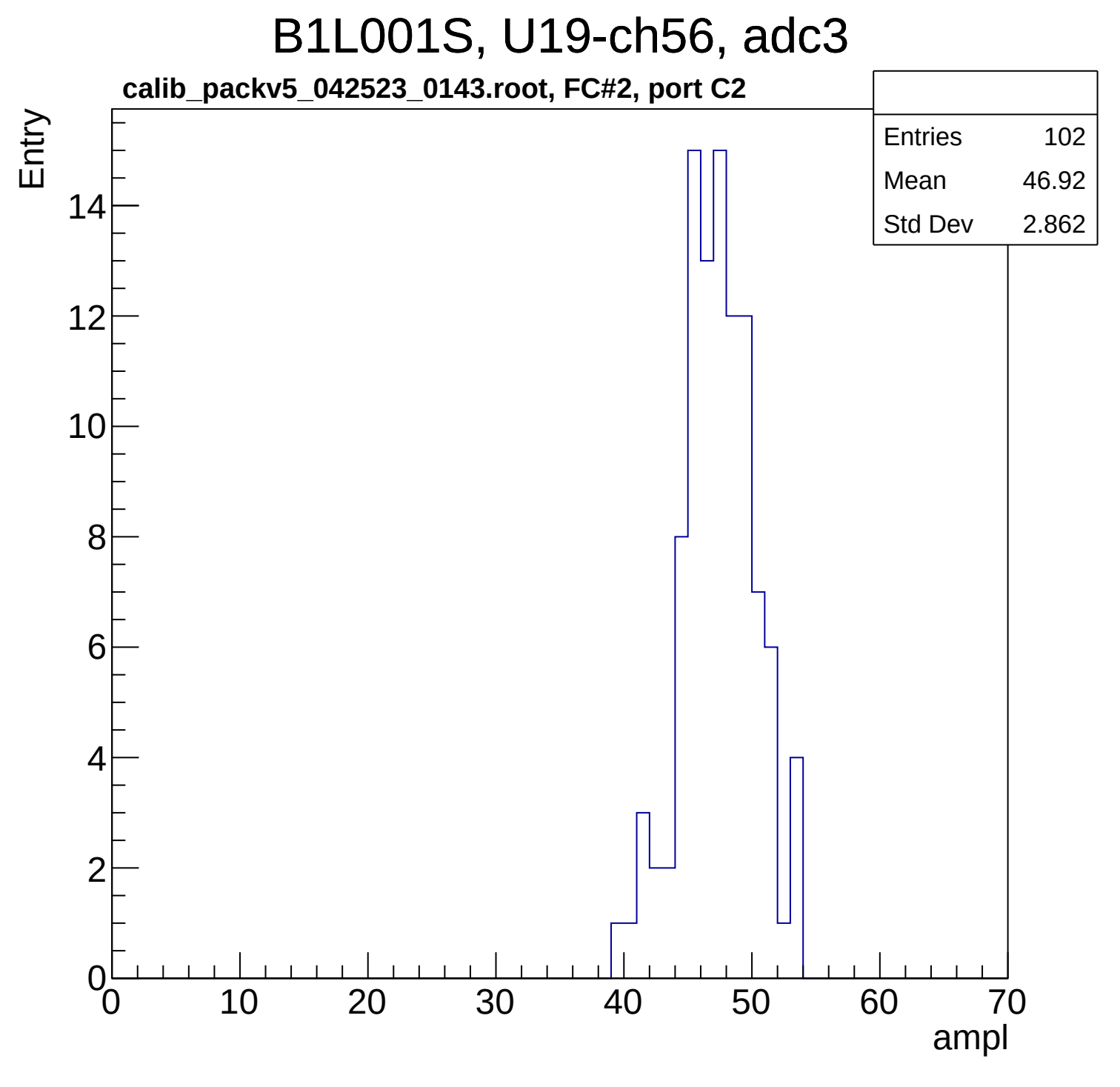
B1L001S, U19-ch56, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 102
Mean 46.92
Std Dev 2.862
Entry
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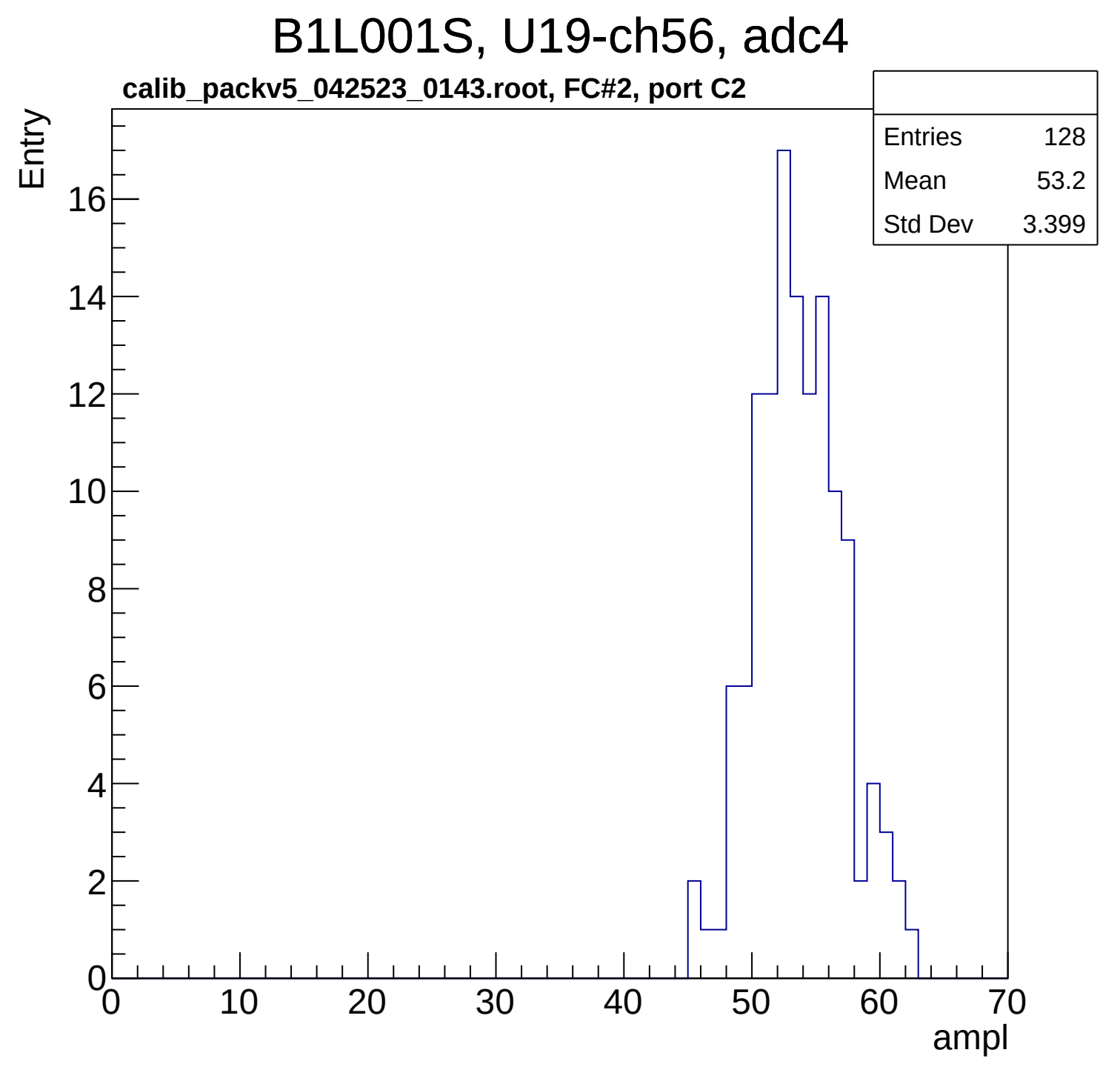
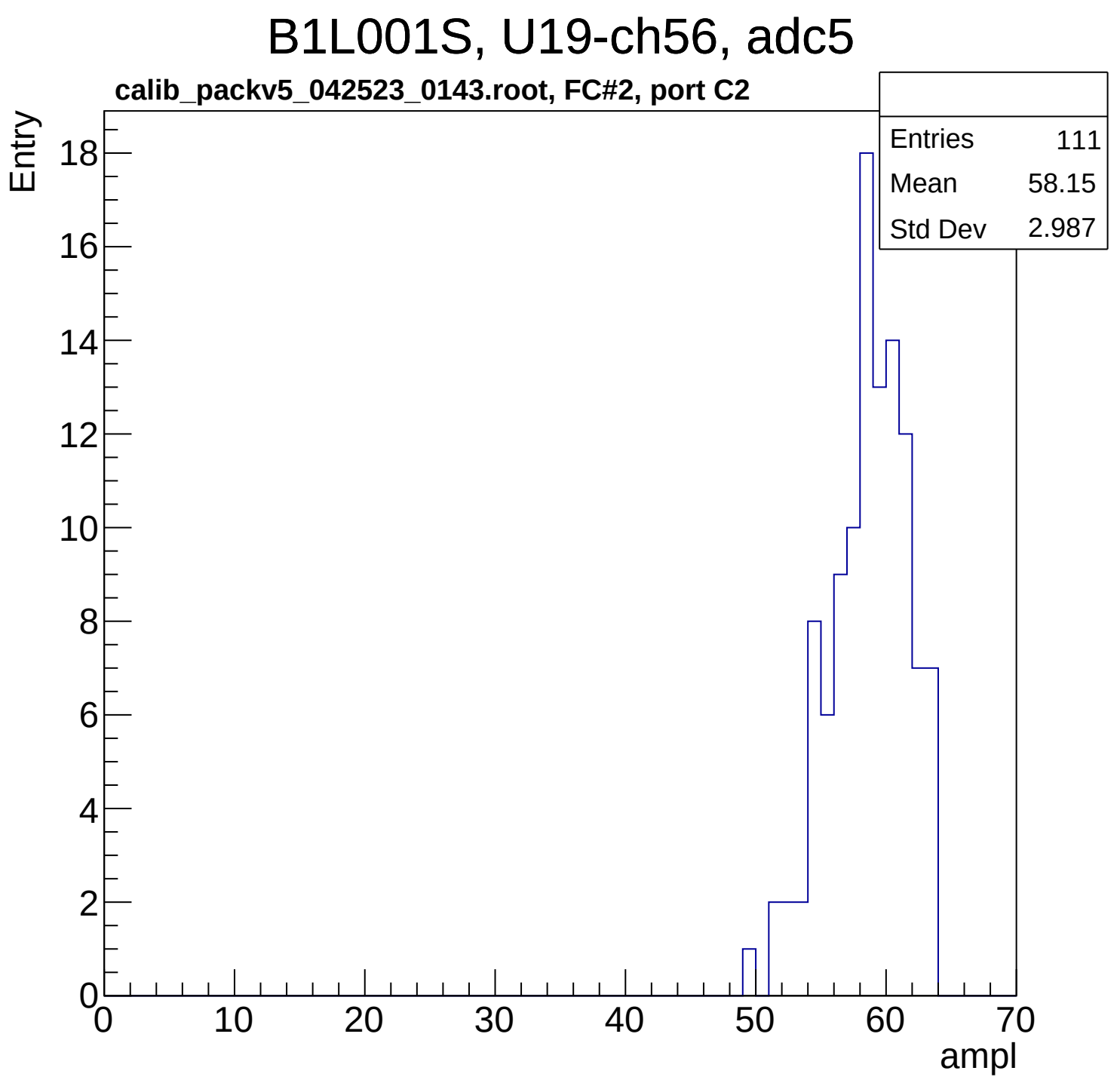
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch56, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 128
Mean 53.2
Std Dev 3.399
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70


B1L001S, U19-ch56, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 111
Mean 58.15
Std Dev 2.987
Entry
ampl
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4
6
8
10
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16
18
0
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40
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60
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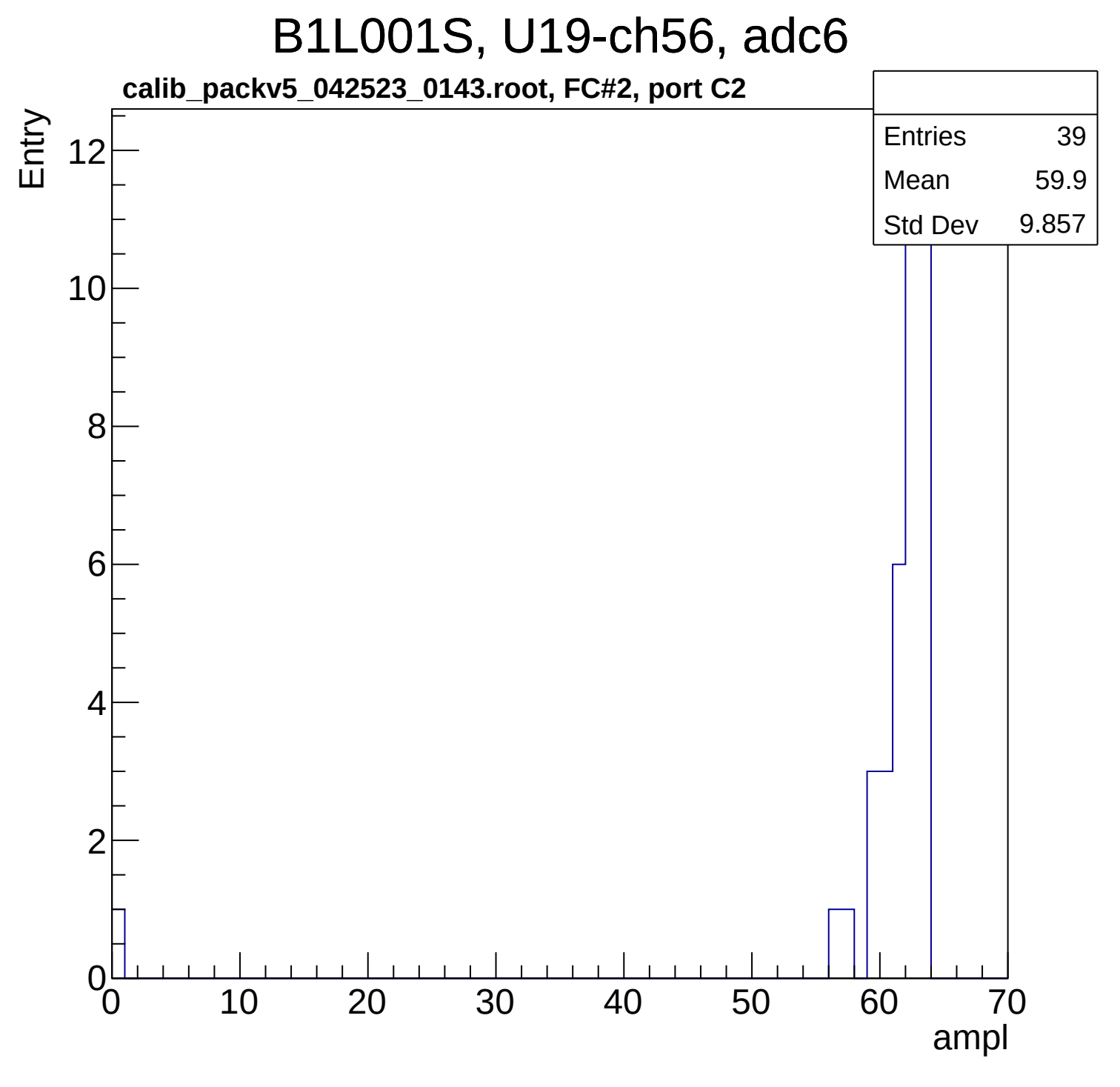
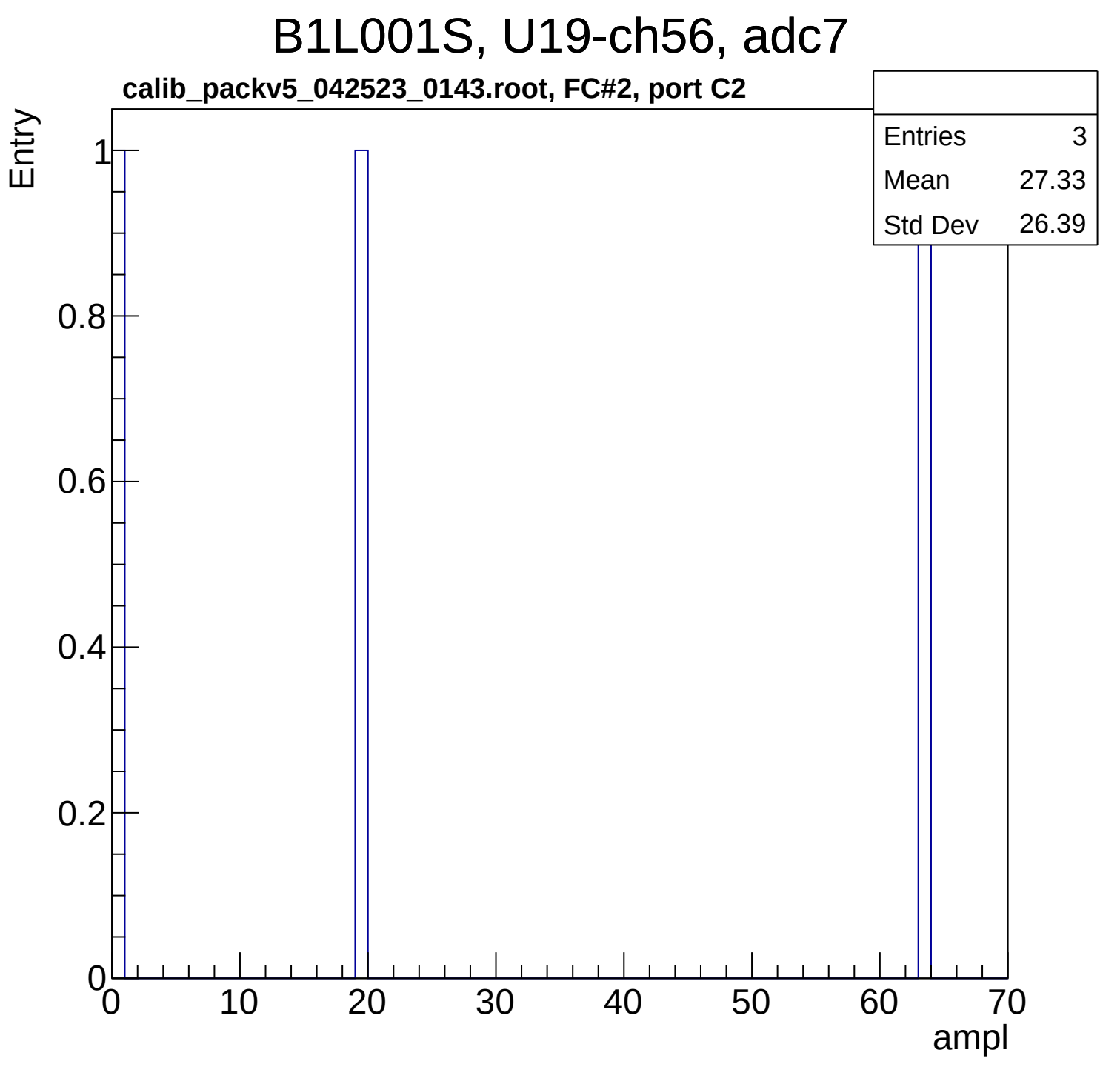
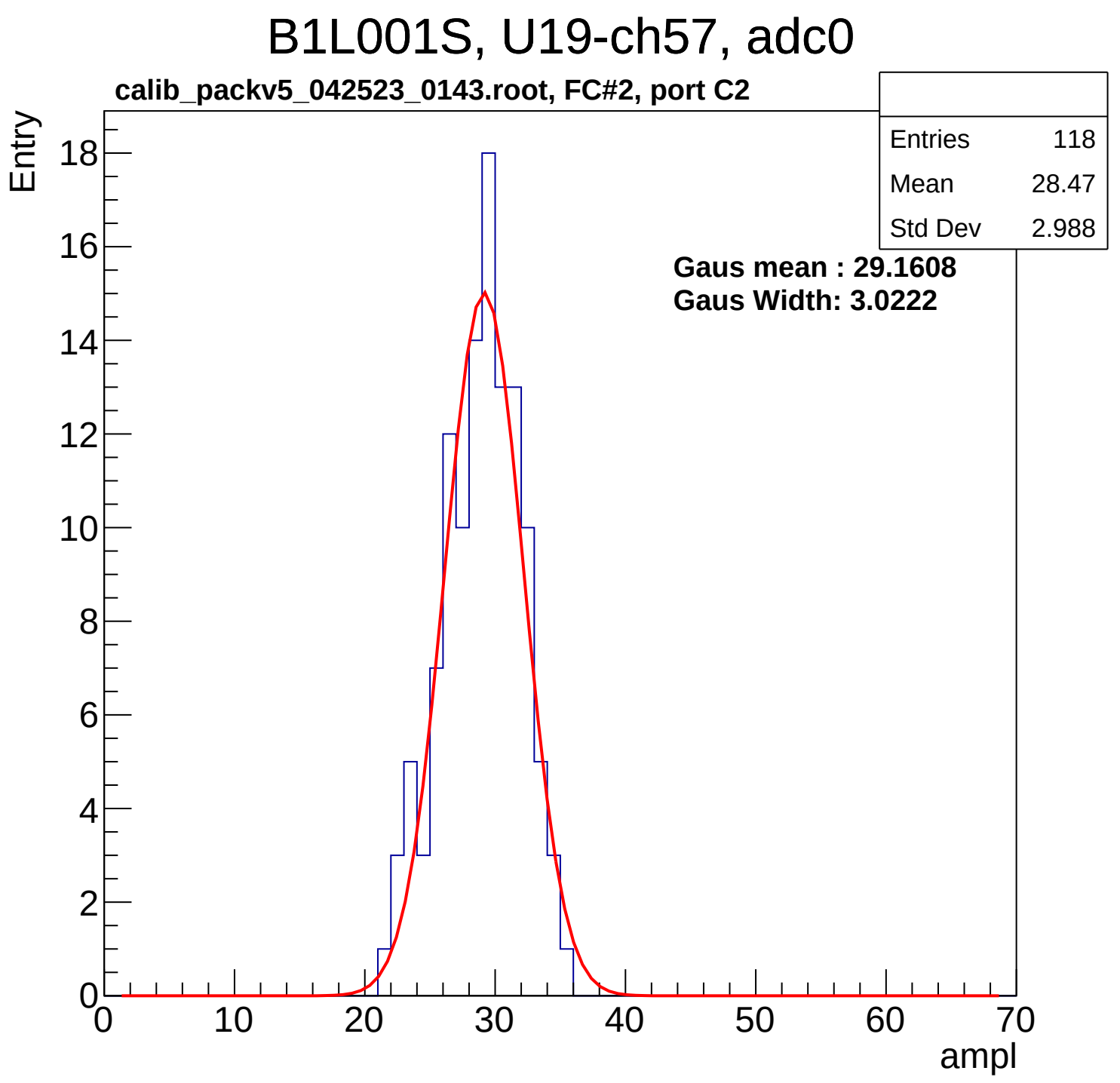

B1L001S, U19-ch56, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 39
Mean 59.9
Std Dev 9.857
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch56, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 3
Mean 27.33
Std Dev 26.39
Entry
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch57, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 118
Mean 28.47
Std Dev 2.988
Gaus mean : 29.1608
Gaus Width: 3.0222
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
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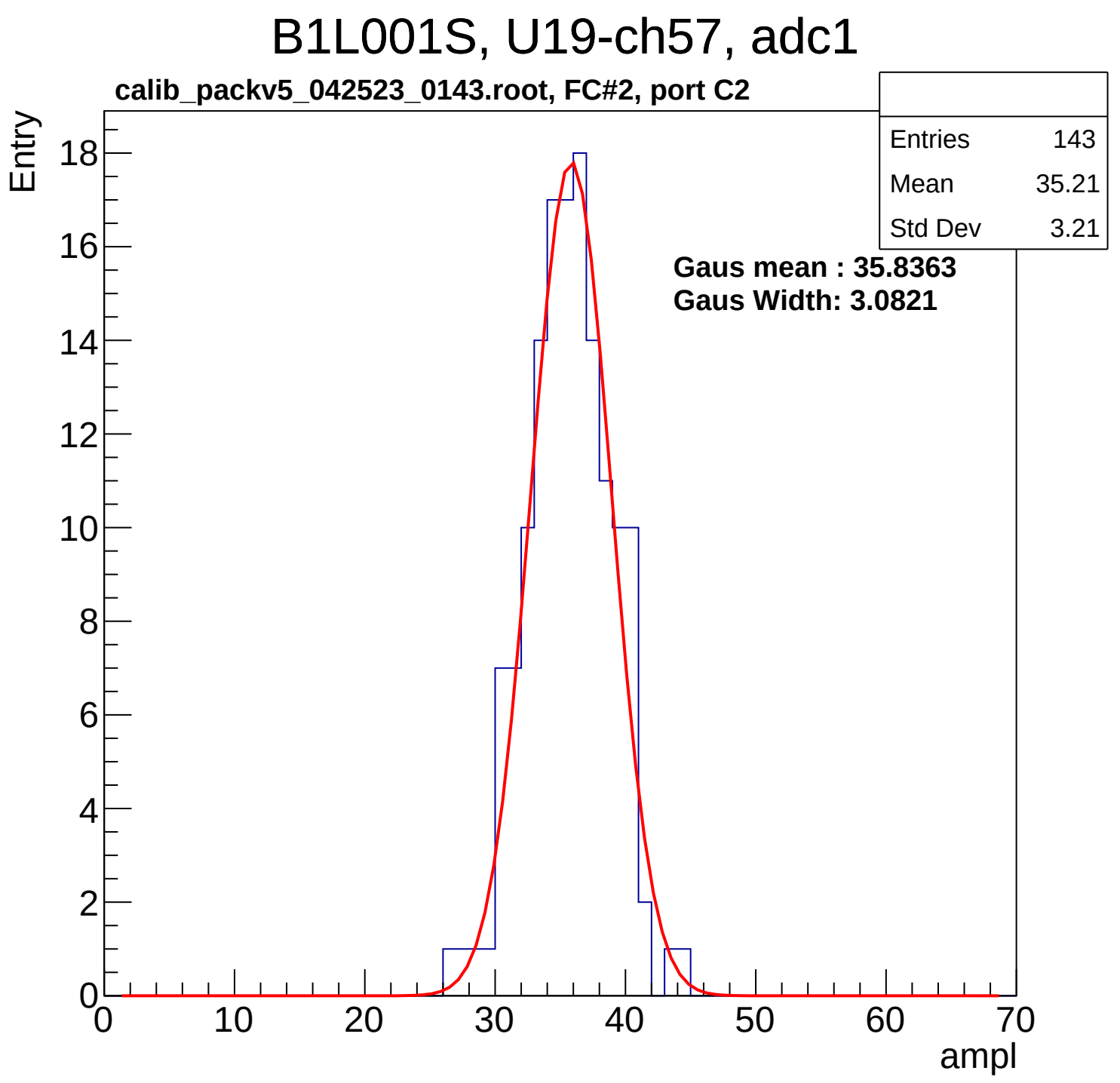
B1L001S, U19-ch57, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 143
Mean 35.21
Std Dev 3.21
Gaus mean : 35.8363
Gaus Width: 3.0821
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
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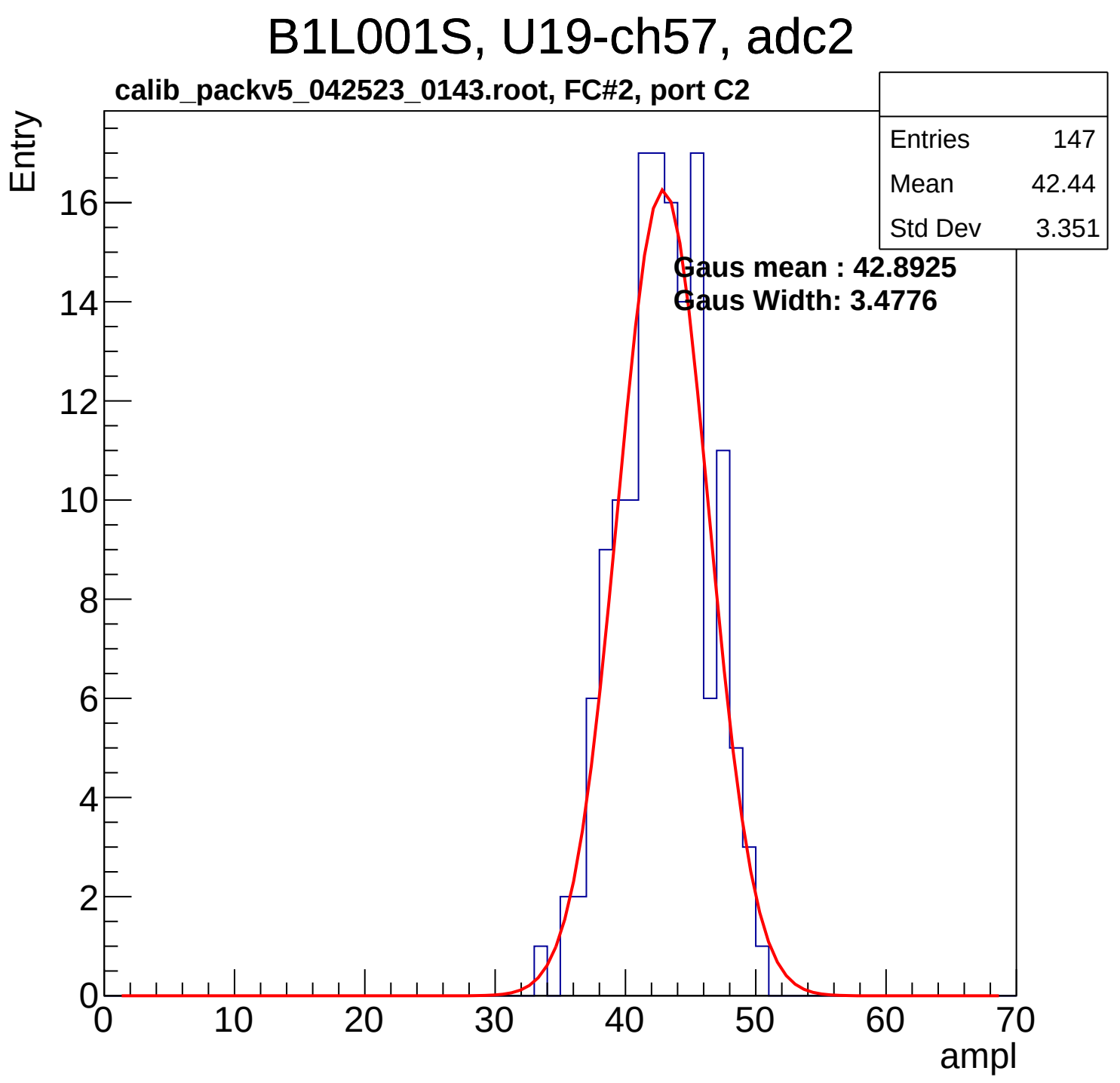
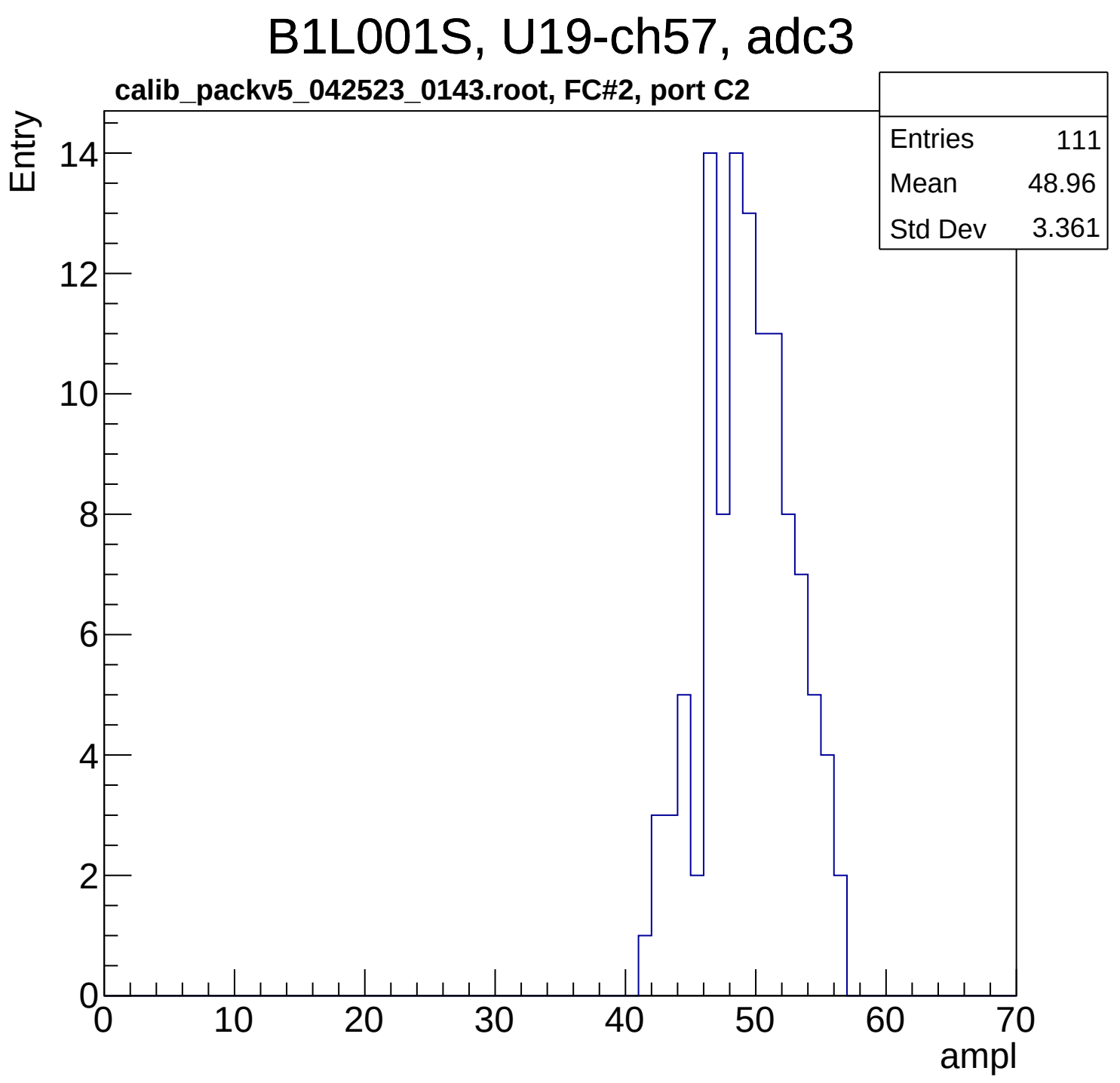
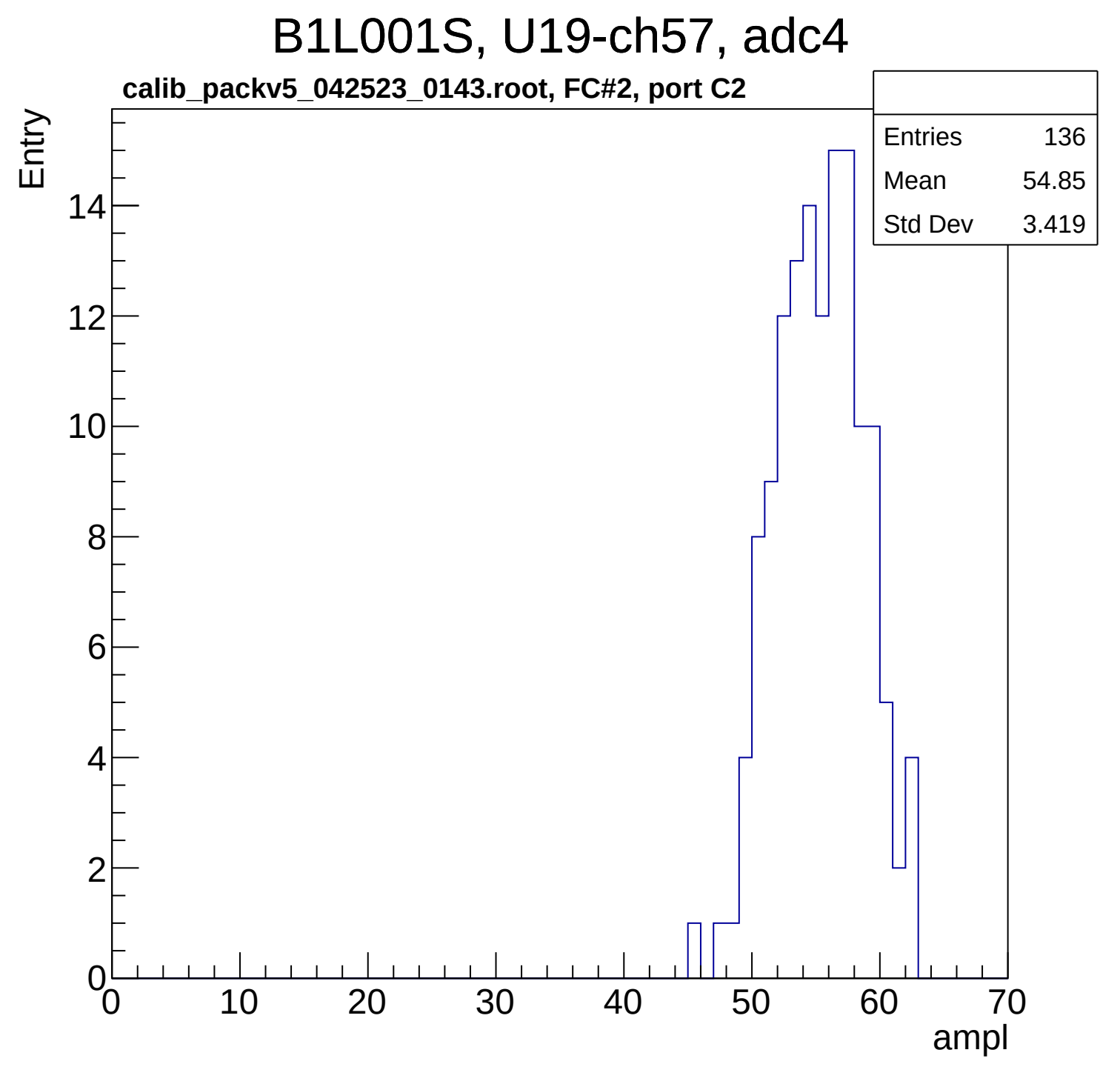
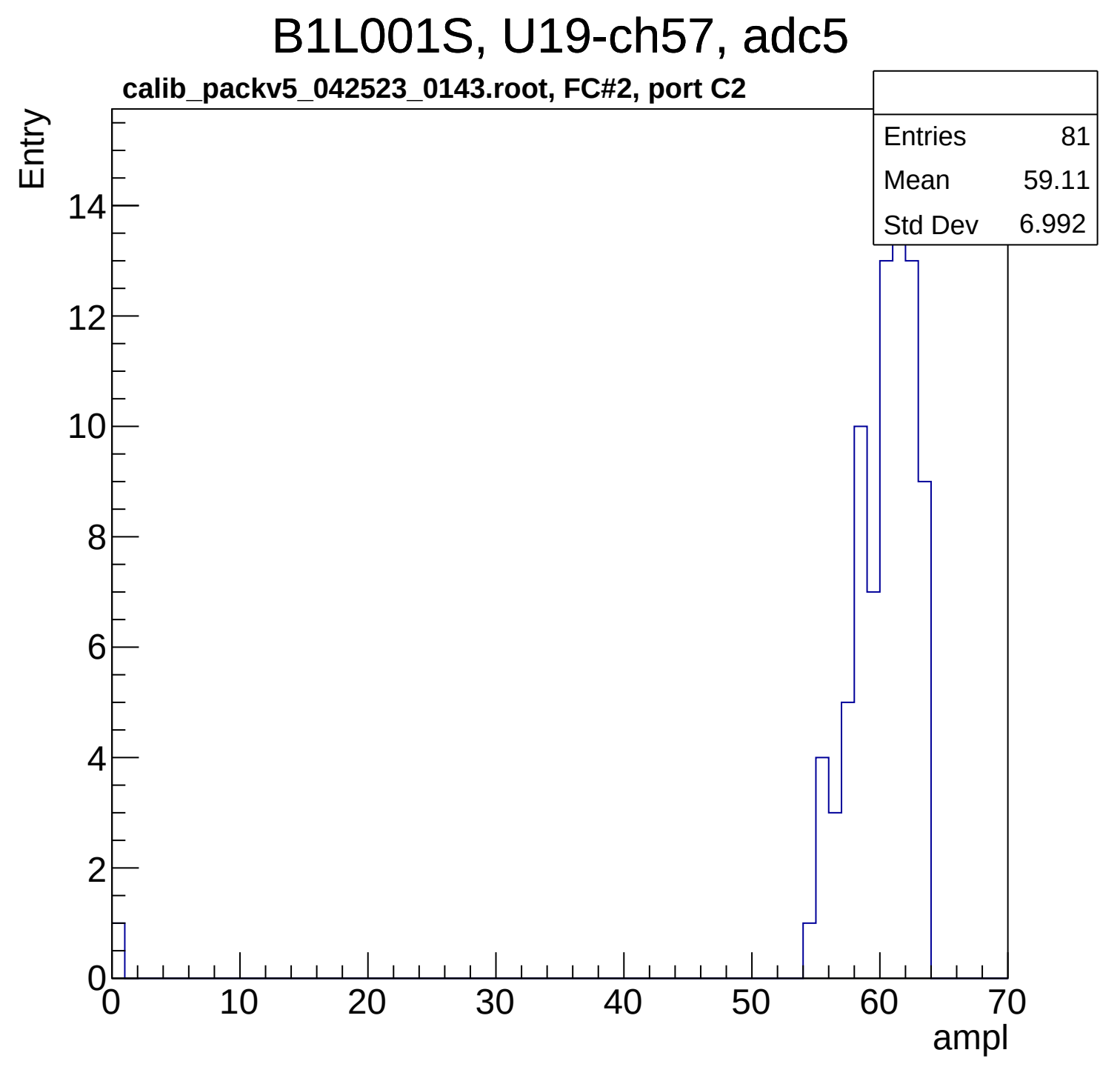
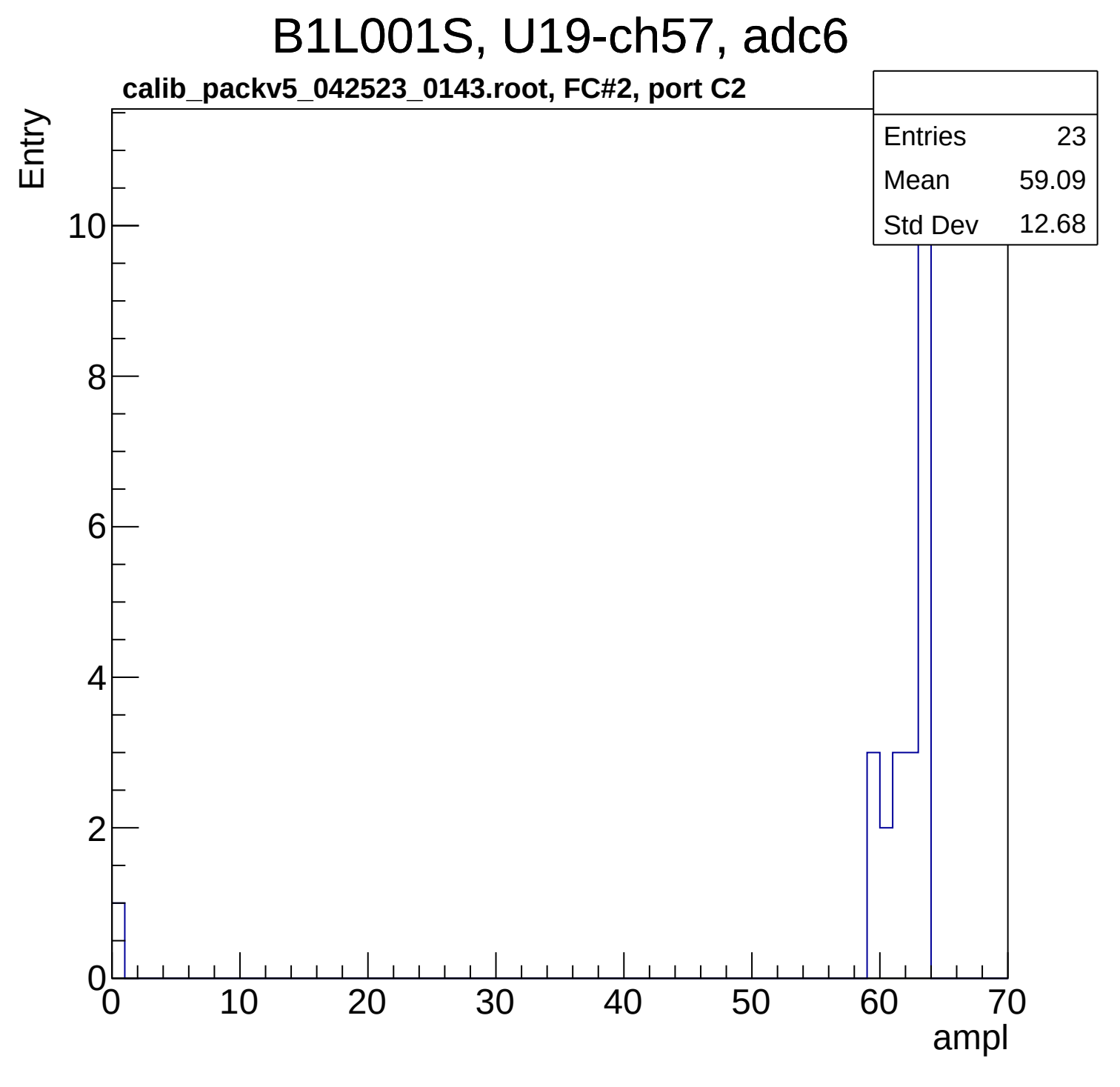
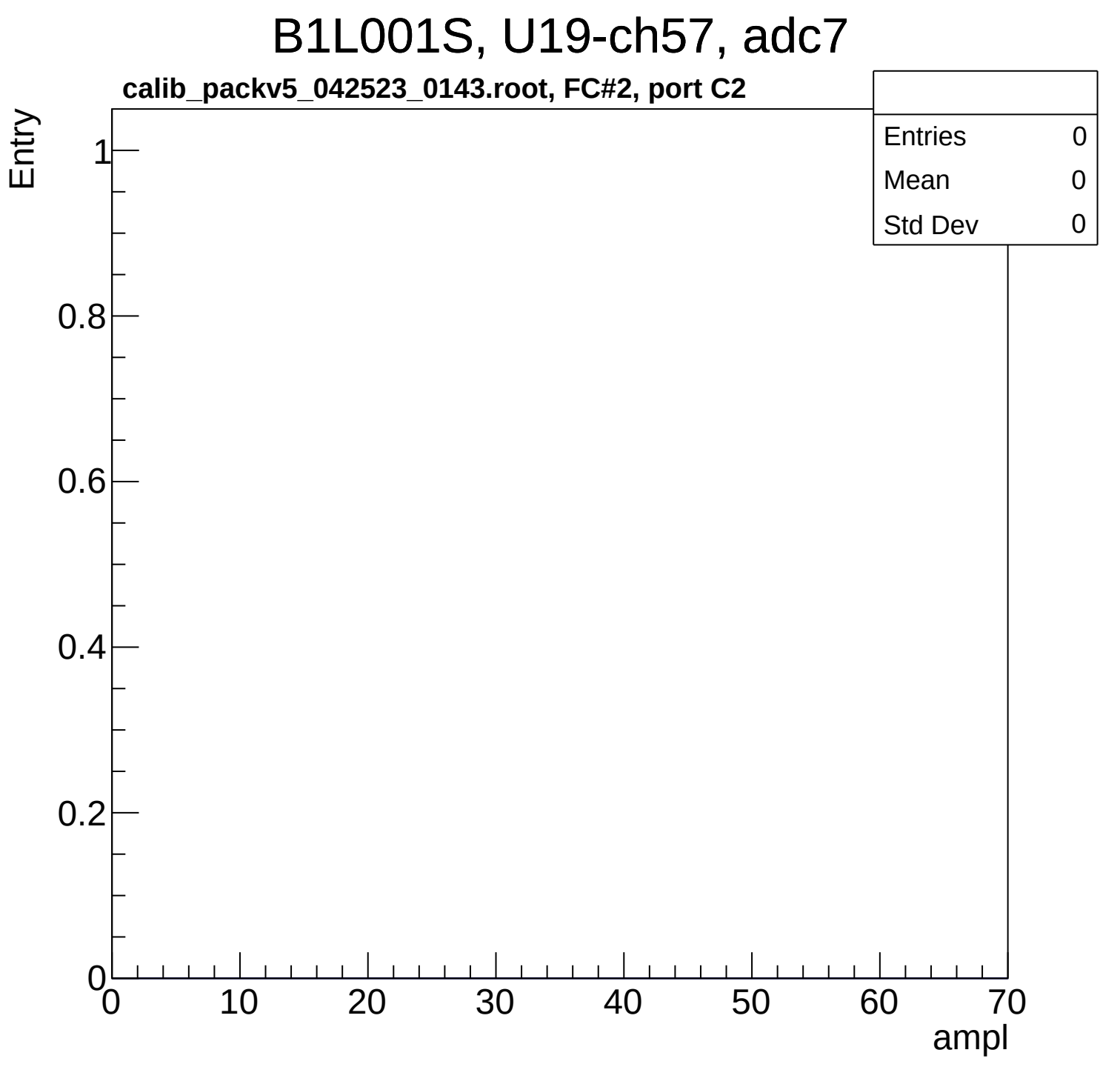

B1L001S, U19-ch57, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 147
Mean 42.44
Std Dev 3.351
Gaus mean : 42.8925
Gaus Width: 3.4776
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

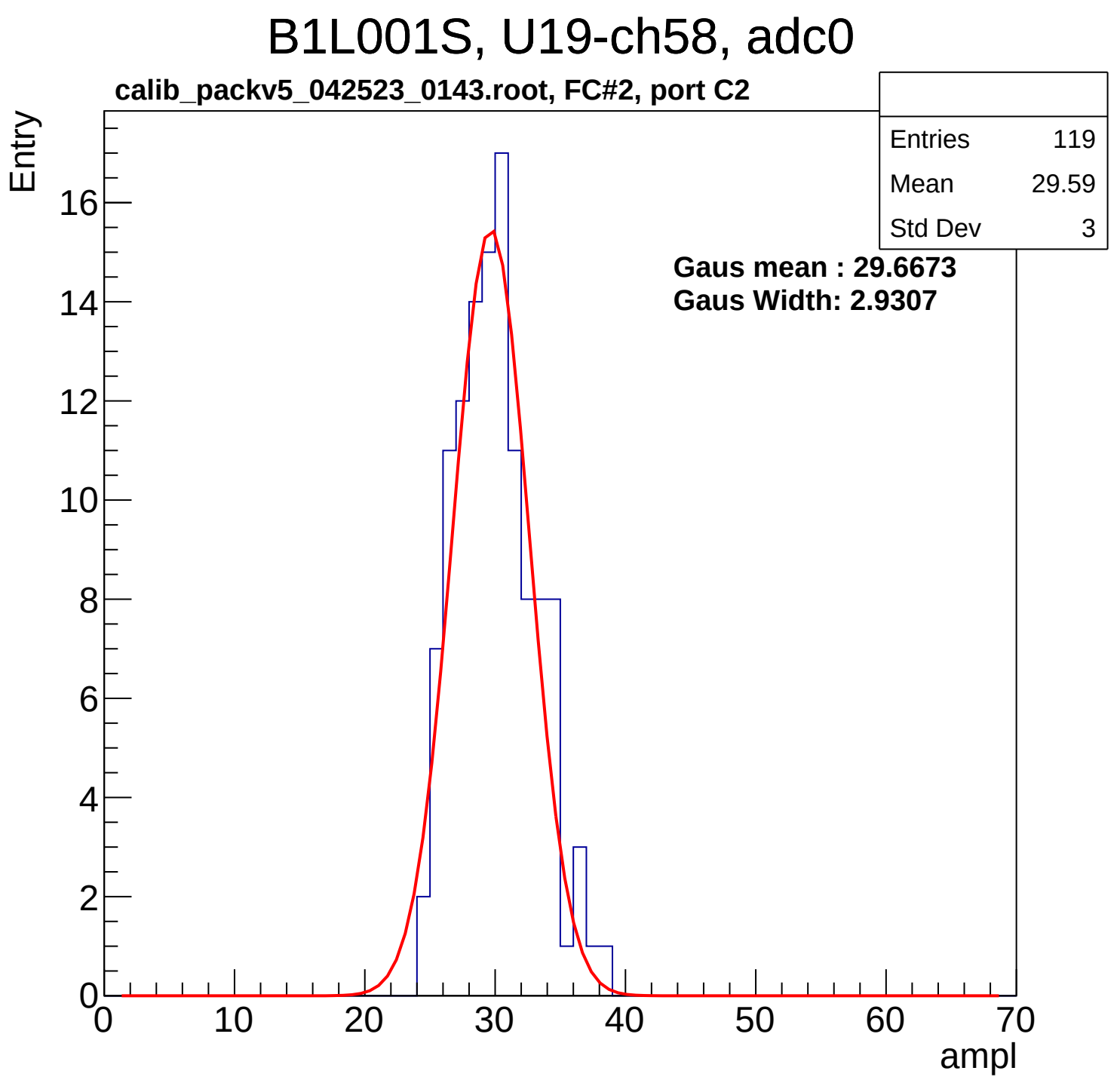

B1L001S, U19-ch57, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 111
Mean 48.96
Std Dev 3.361
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

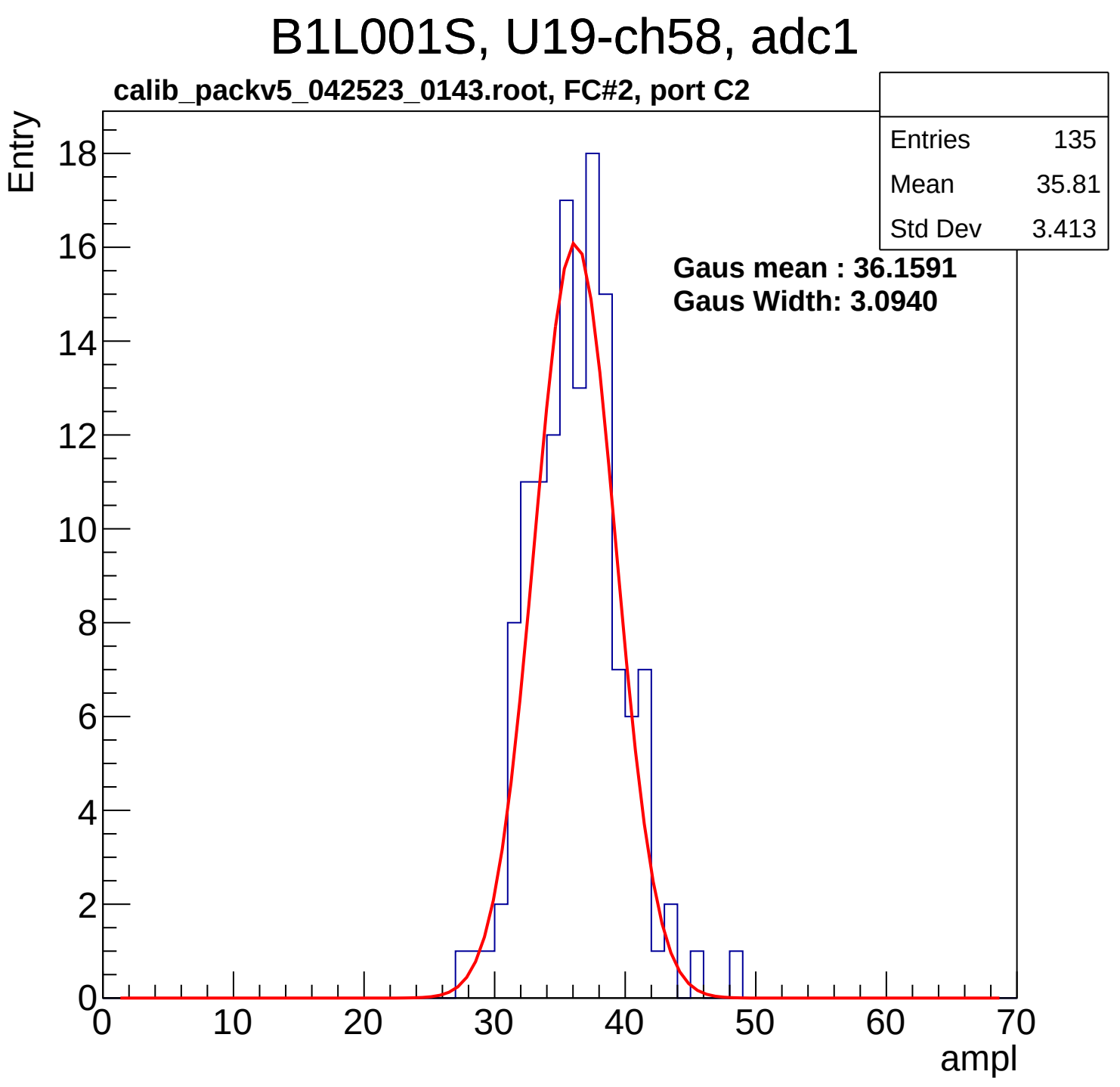

B1L001S, U19-ch57, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 136
Mean 54.85
Std Dev 3.419
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl

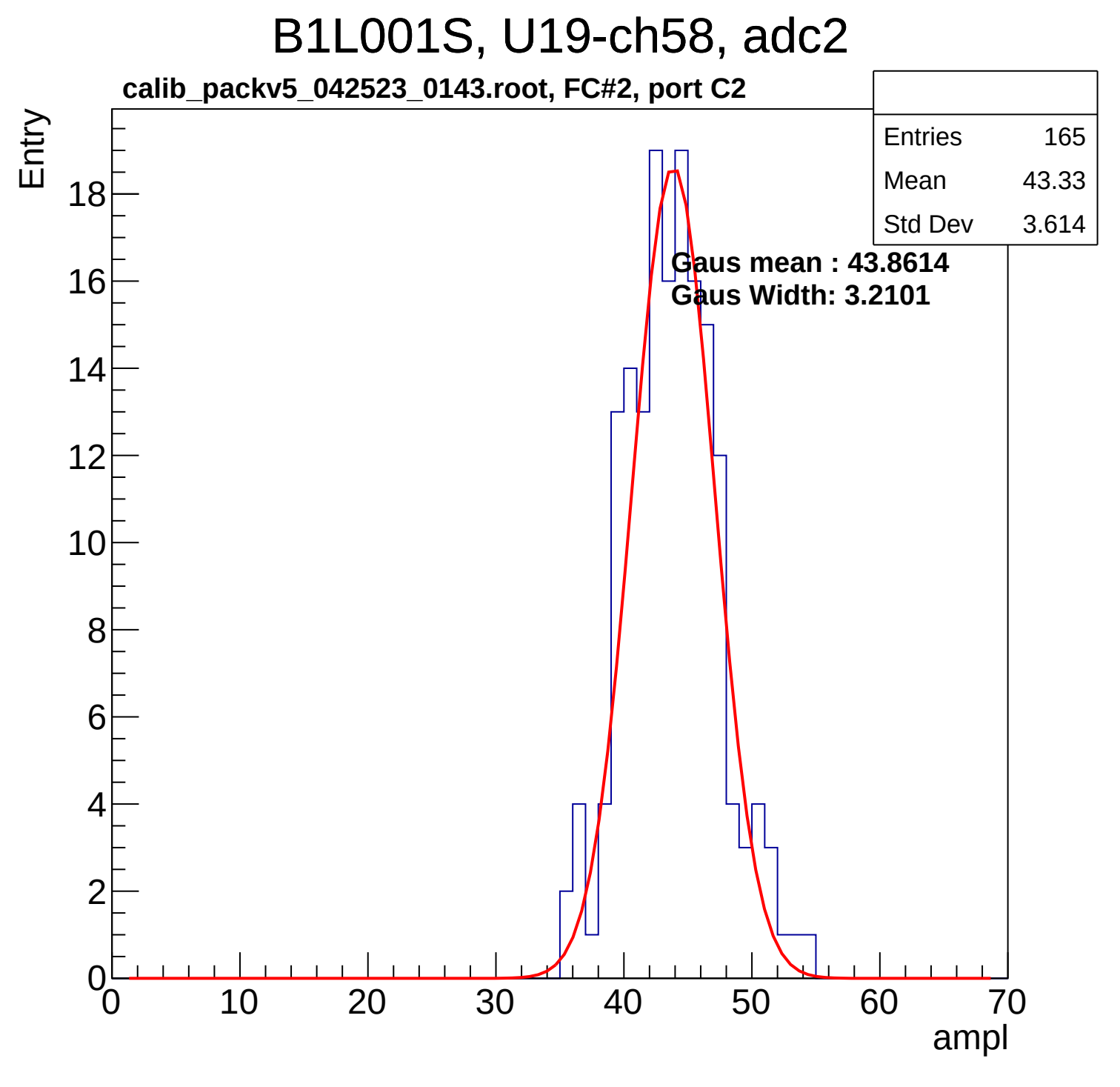

B1L001S, U19-ch57, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 81
Mean 59.11
Std Dev 6.992
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

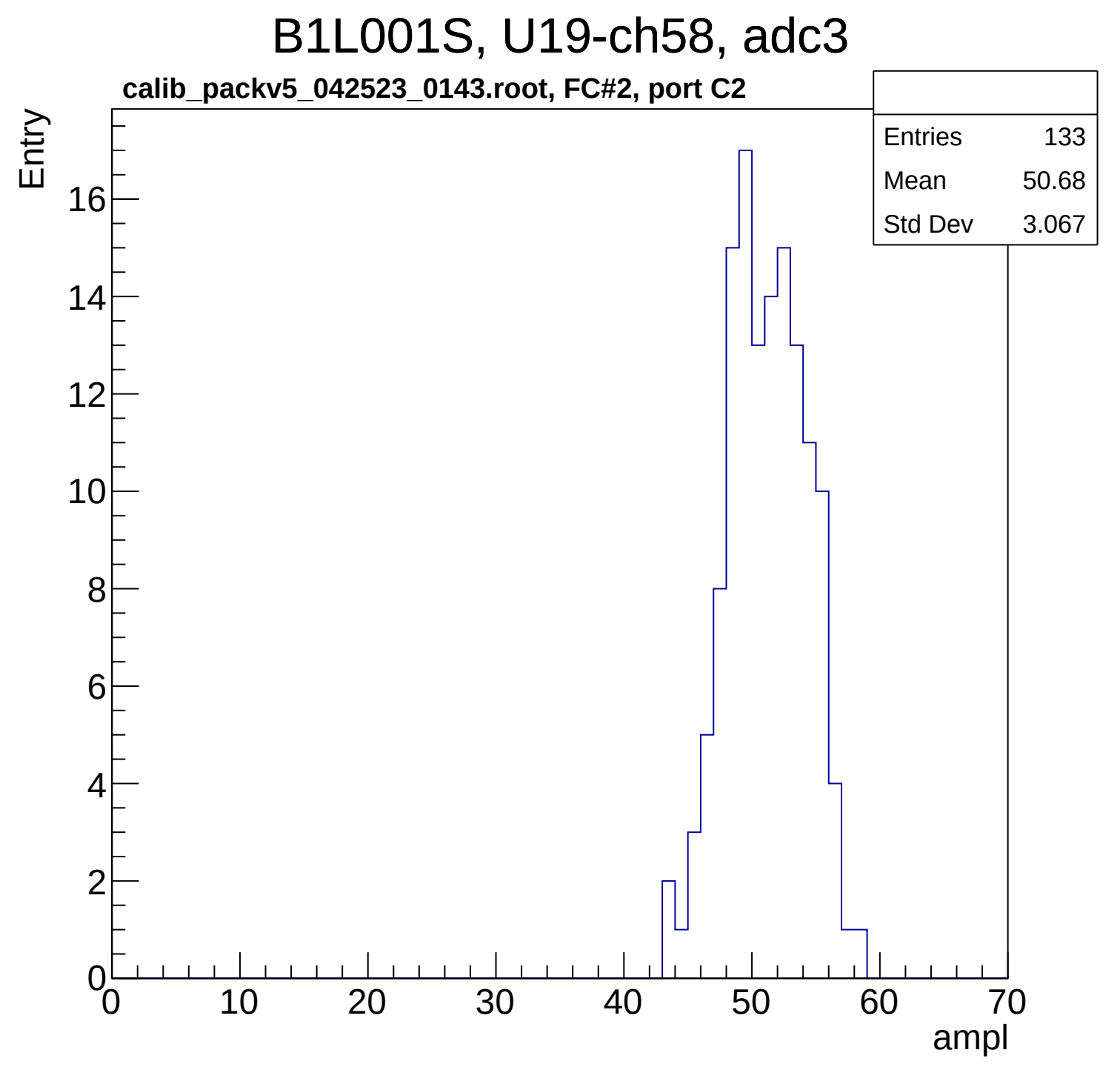

B1L001S, U19-ch57, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 23
Mean 59.09
Std Dev 12.68
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

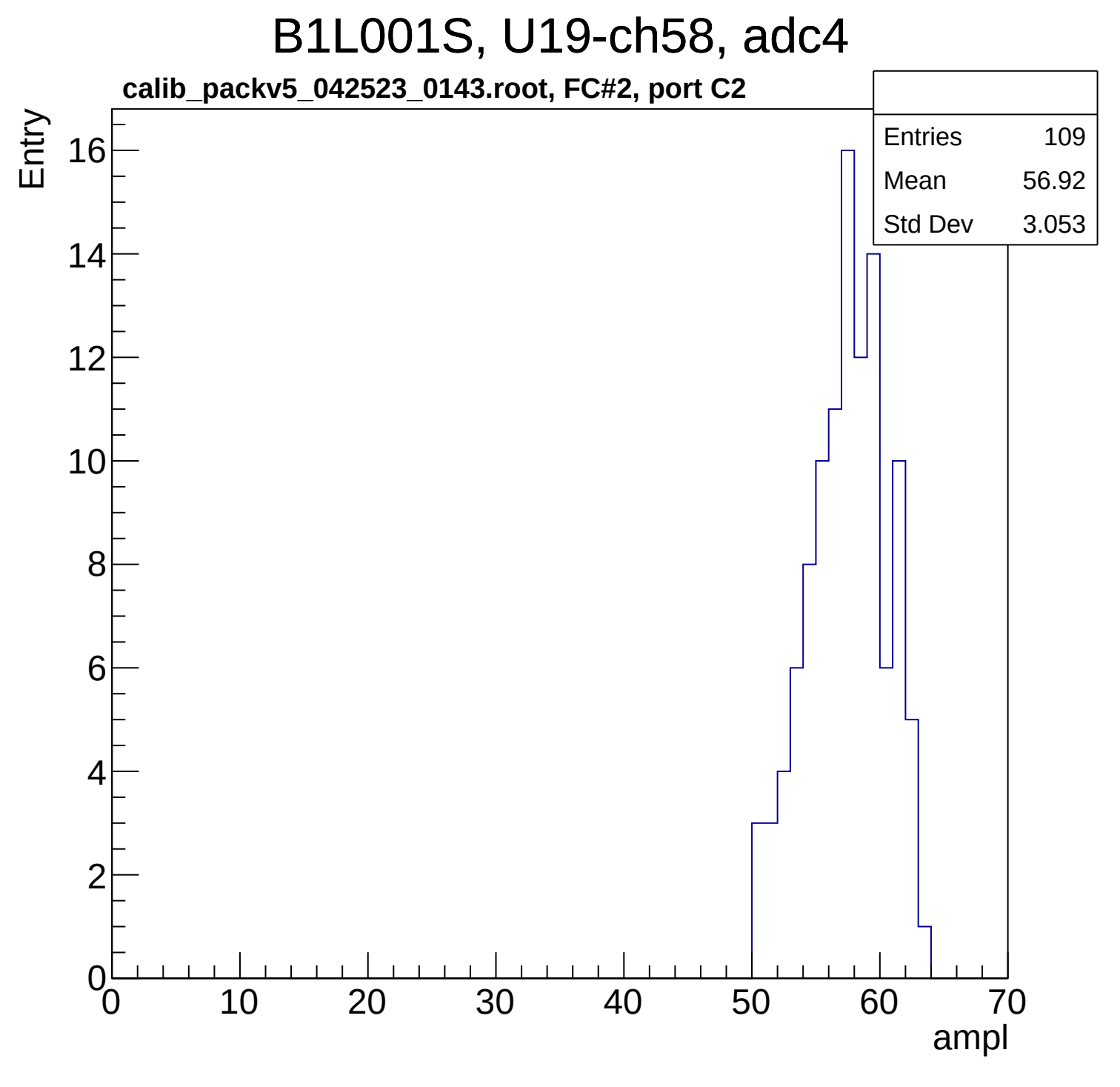

B1L001S, U19-ch57, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

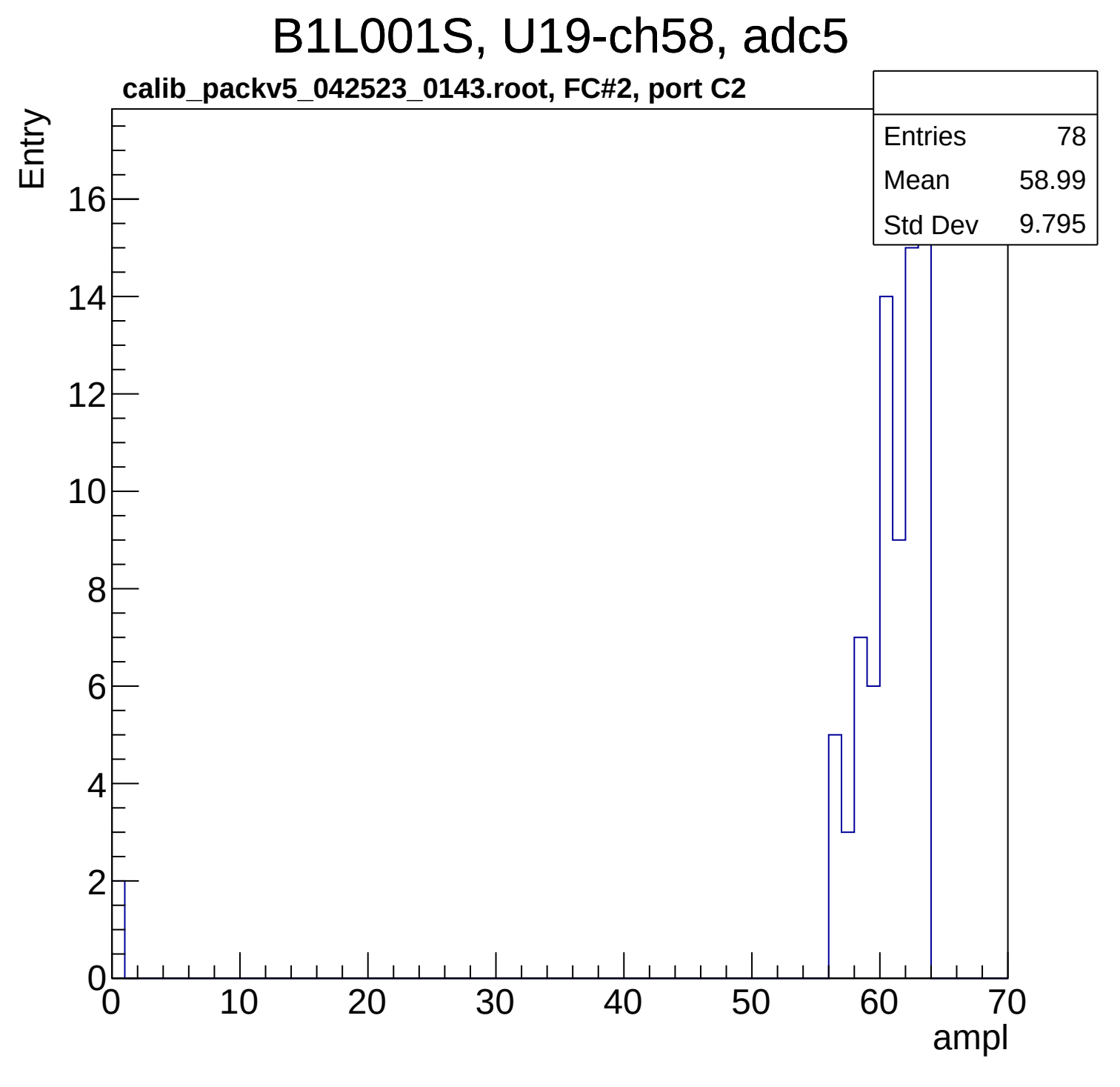

B1L001S, U19-ch58, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 119
Mean 29.59
Std Dev 3
Gaus mean : 29.6673
Gaus Width: 2.9307
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70


B1L001S, U19-ch58, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 135
Mean 35.81
Std Dev 3.413
Gaus mean : 36.1591
Gaus Width: 3.0940
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70


B1L001S, U19-ch58, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 165
Mean 43.33
Std Dev 3.614
Gaus mean : 43.8614
Gaus Width: 3.2101
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70


B1L001S, U19-ch58, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 133
Mean 50.68
Std Dev 3.067
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70


B1L001S, U19-ch58, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 109
Mean 56.92
Std Dev 3.053
Entry
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch58, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 78
Mean 58.99
Std Dev 9.795
Entry
ampl
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2
4
6
8
10
12
14
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0
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60
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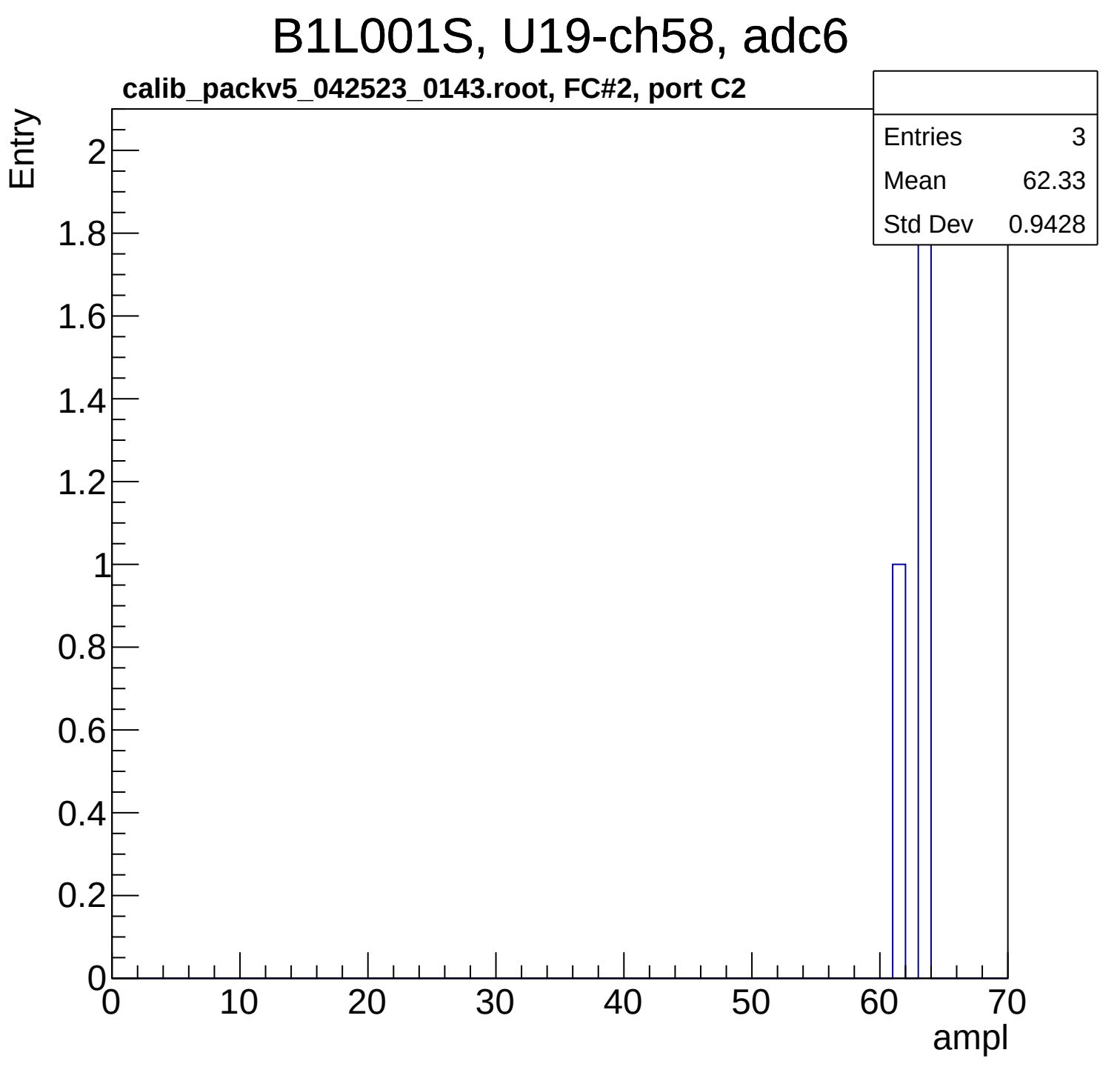
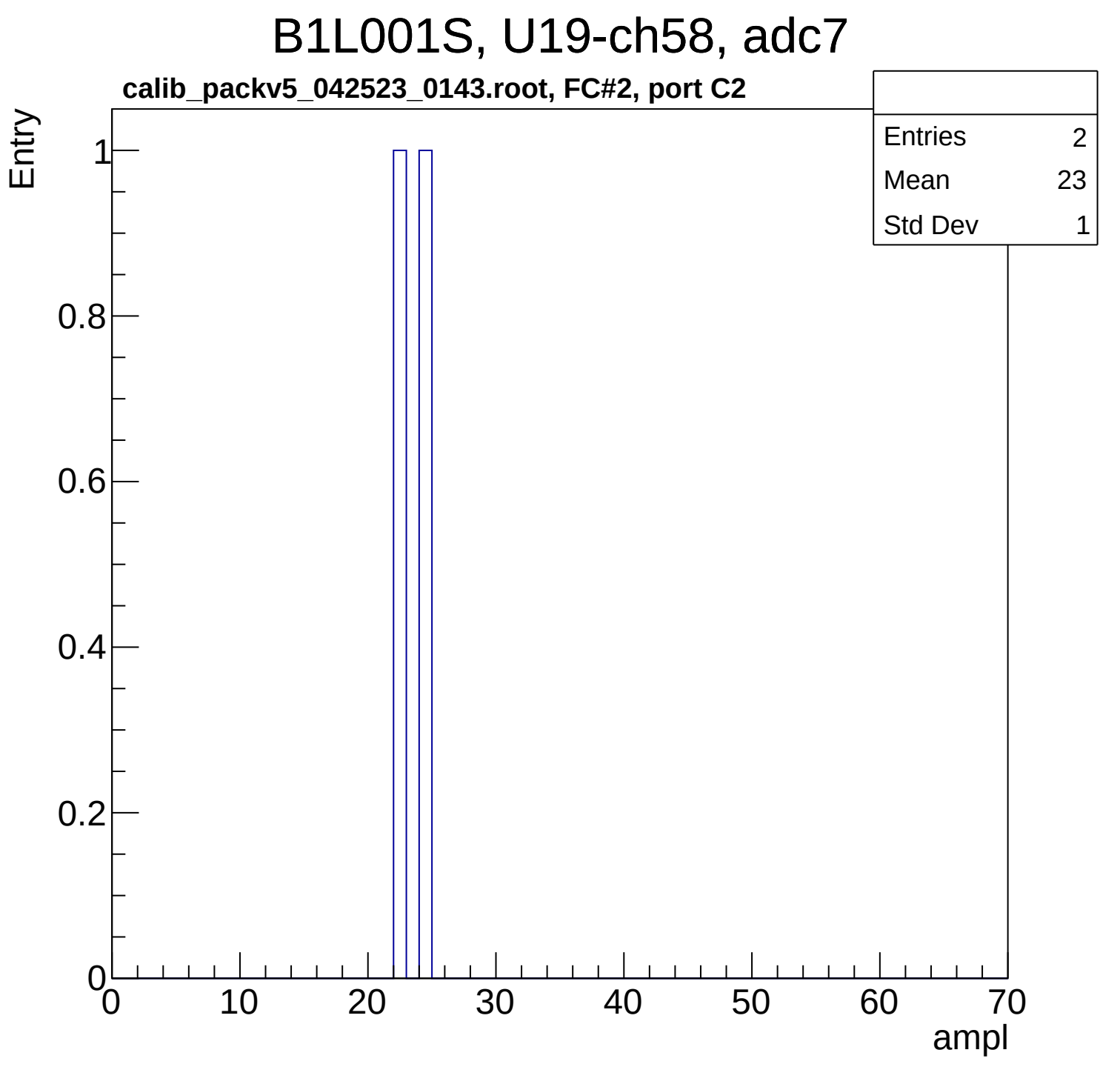
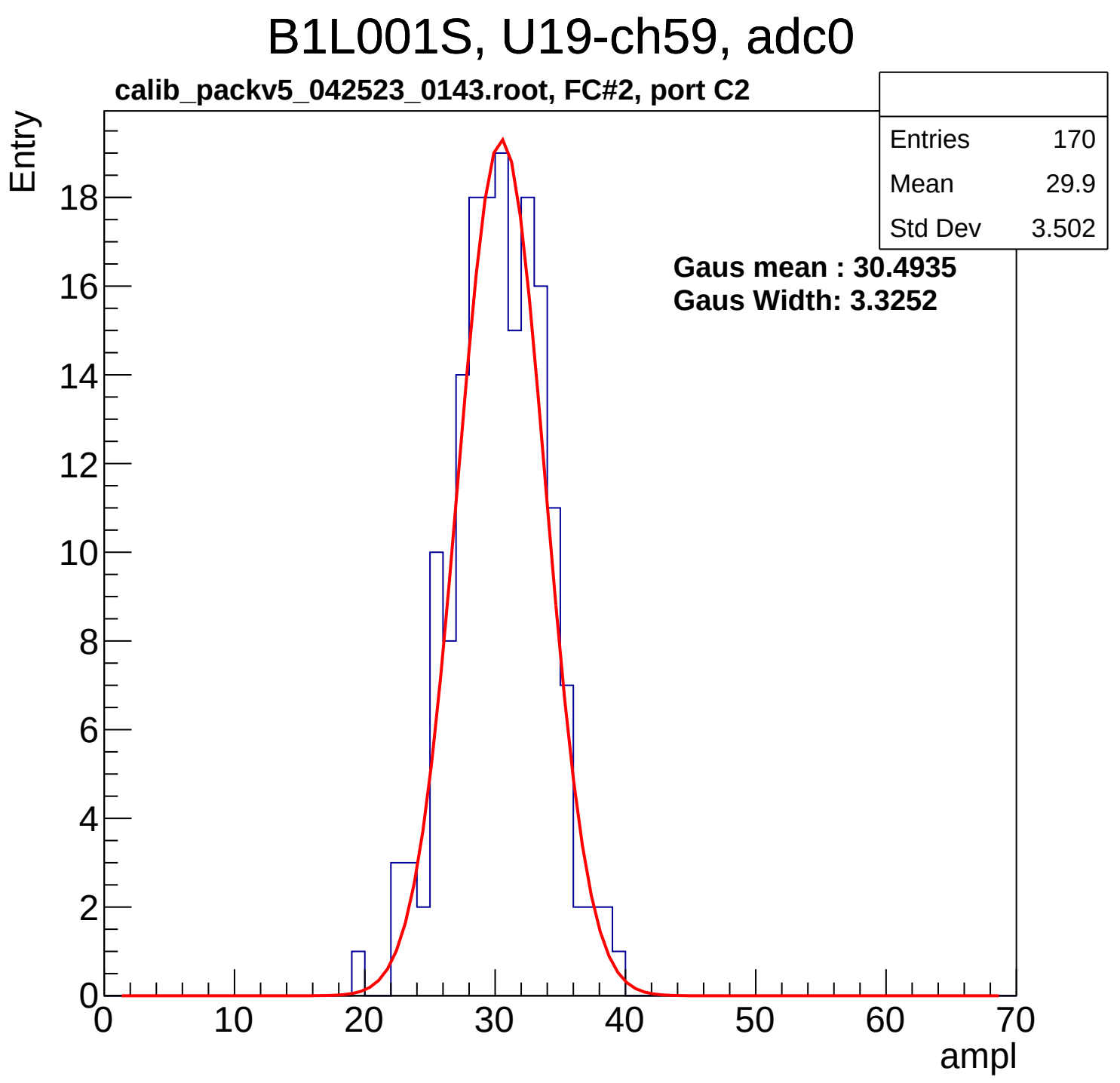

B1L001S, U19-ch58, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 3
Mean 62.33
Std Dev 0.9428
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L001S, U19-ch58, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 23
Std Dev 1
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch59, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 170
Mean 29.9
Std Dev 3.502
Gaus mean : 30.4935
Gaus Width: 3.3252
Entry
ampl
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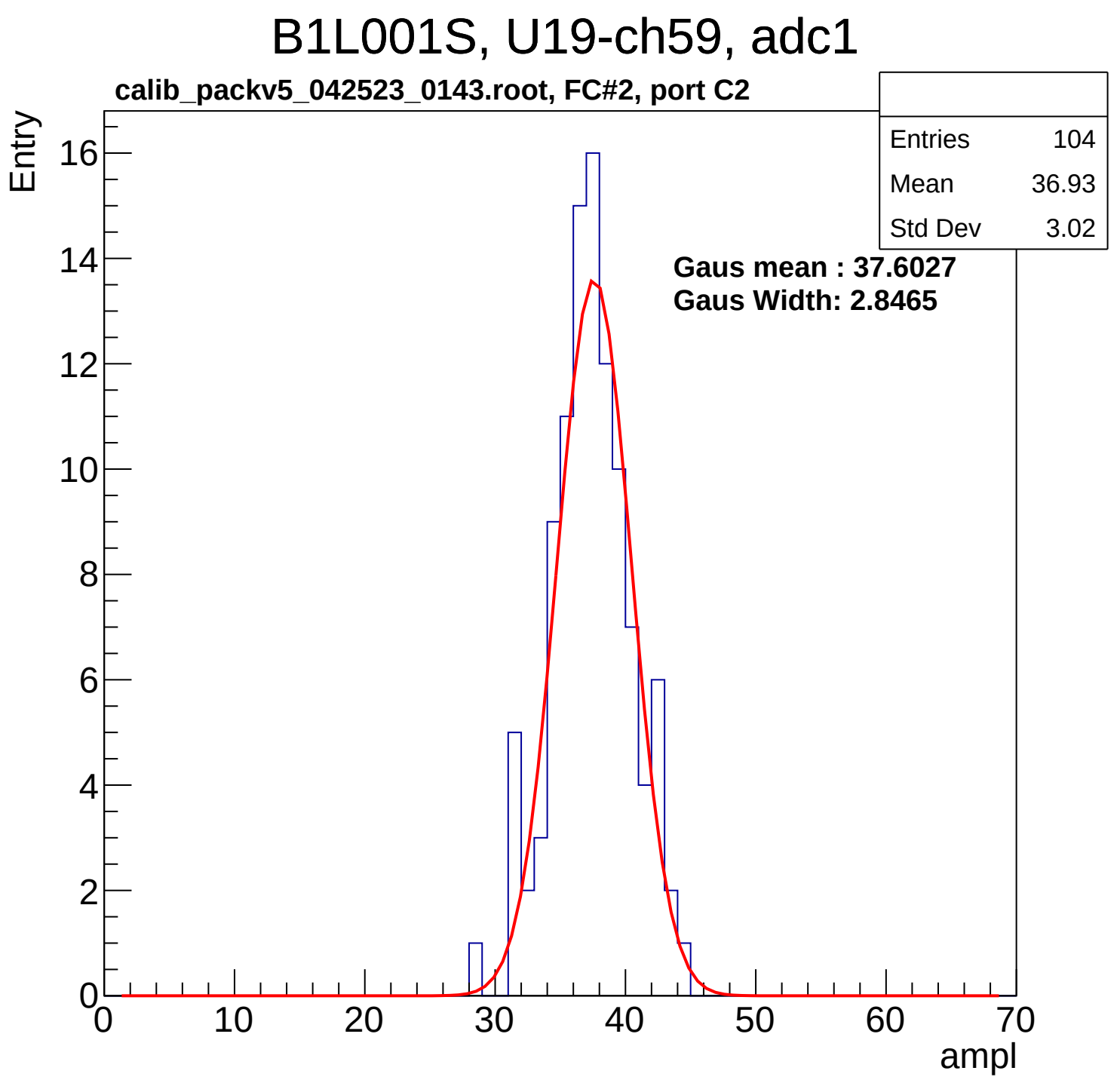
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70


B1L001S, U19-ch59, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 104
Mean 36.93
Std Dev 3.02
Gaus mean : 37.6027
Gaus Width: 2.8465
Entry
ampl
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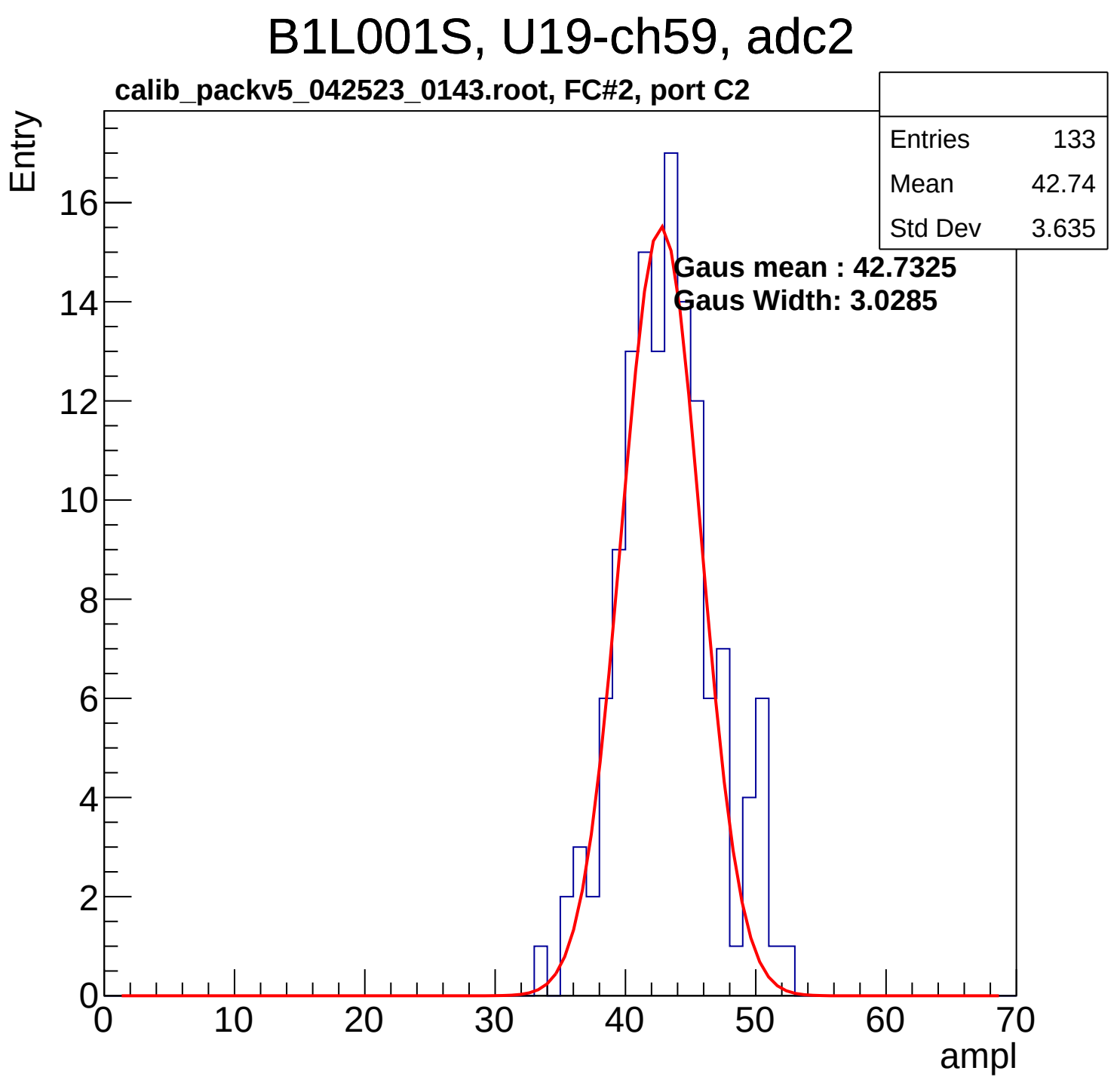
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70


B1L001S, U19-ch59, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 133
Mean 42.74
Std Dev 3.635
Gaus mean : 42.7325
Gaus Width: 3.0285
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
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40
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60
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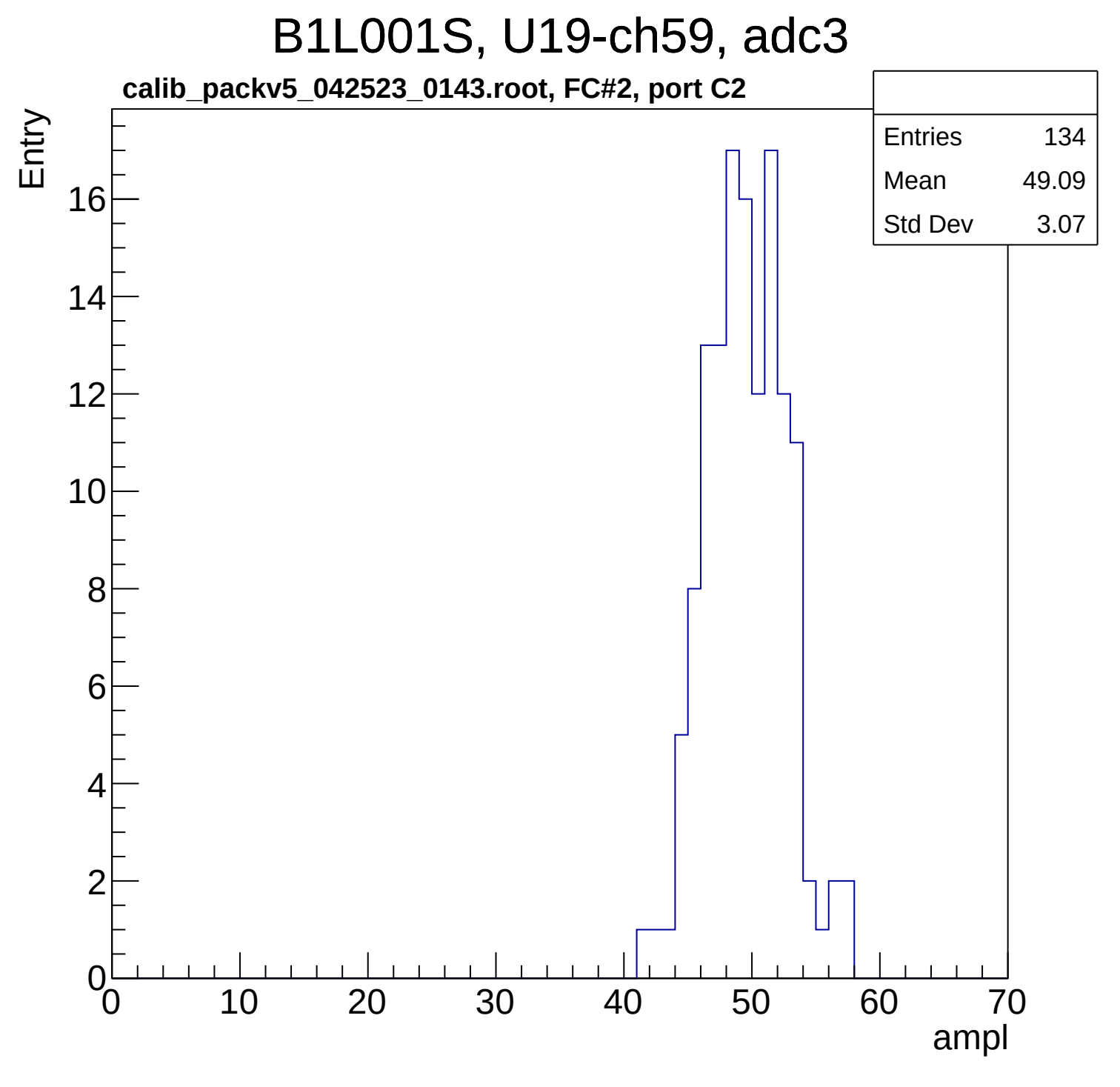
B1L001S, U19-ch59, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 134
Mean 49.09
Std Dev 3.07
Entry
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4
6
8
10
12
14
16
0
10
20
30
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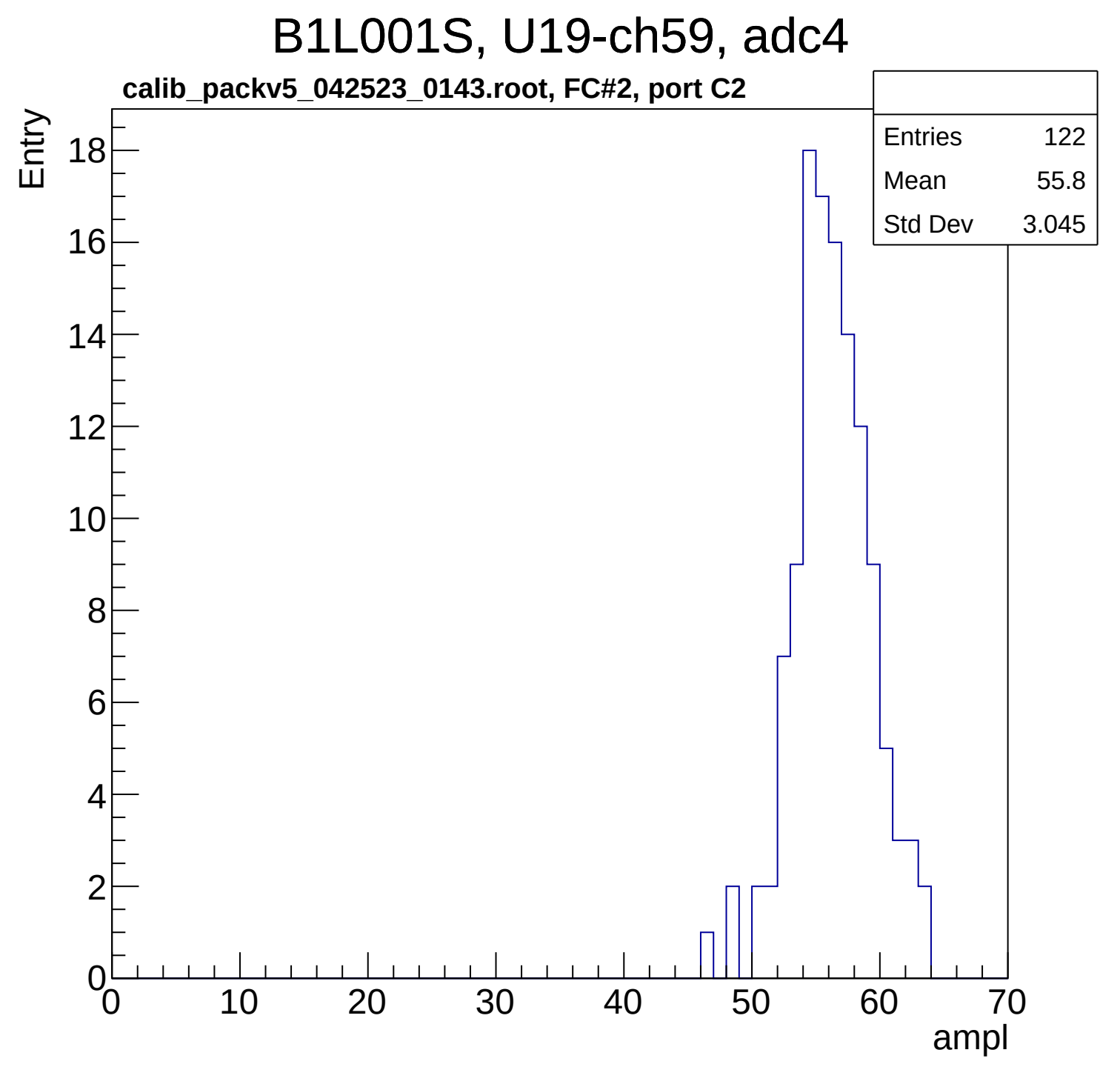
50
60
70
ampl


B1L001S, U19-ch59, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 122
Mean 55.8
Std Dev 3.045
Entry
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6
8
10
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14
16
18
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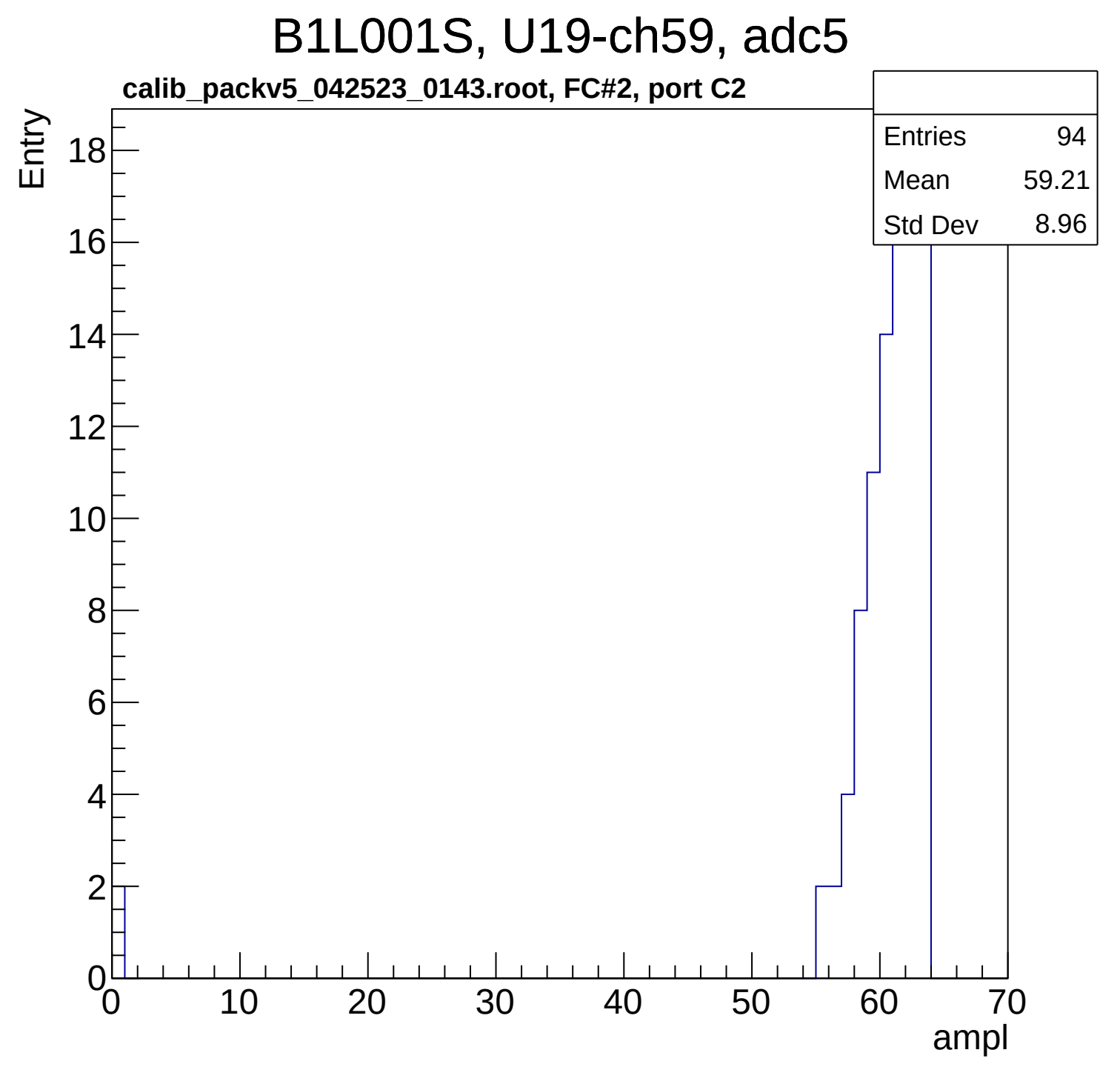
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch59, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 94
Mean 59.21
Std Dev 8.96
Entry
ampl
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4
6
8
10
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18
0
10
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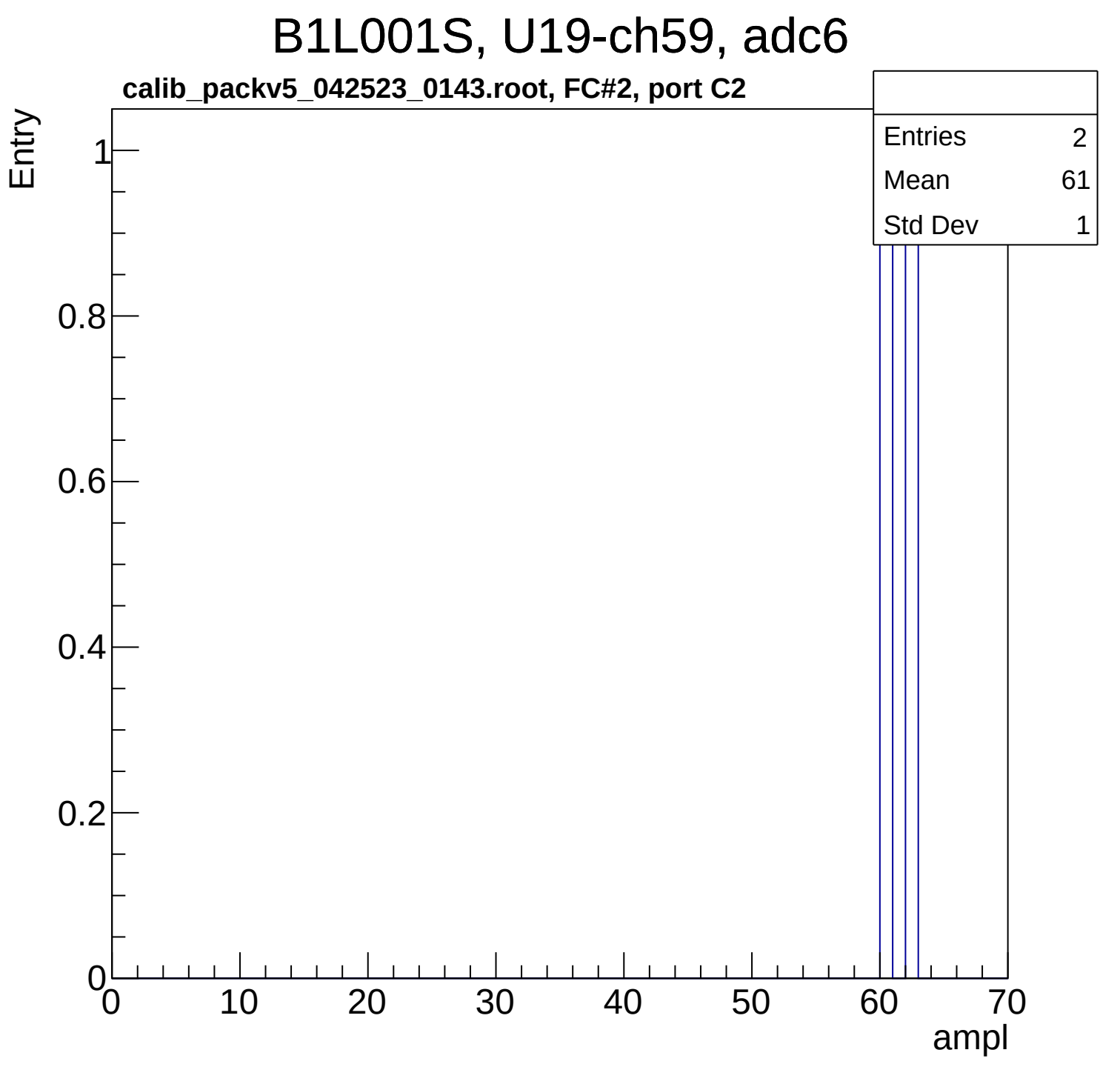
B1L001S, U19-ch59, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 61
Std Dev 1
Entry
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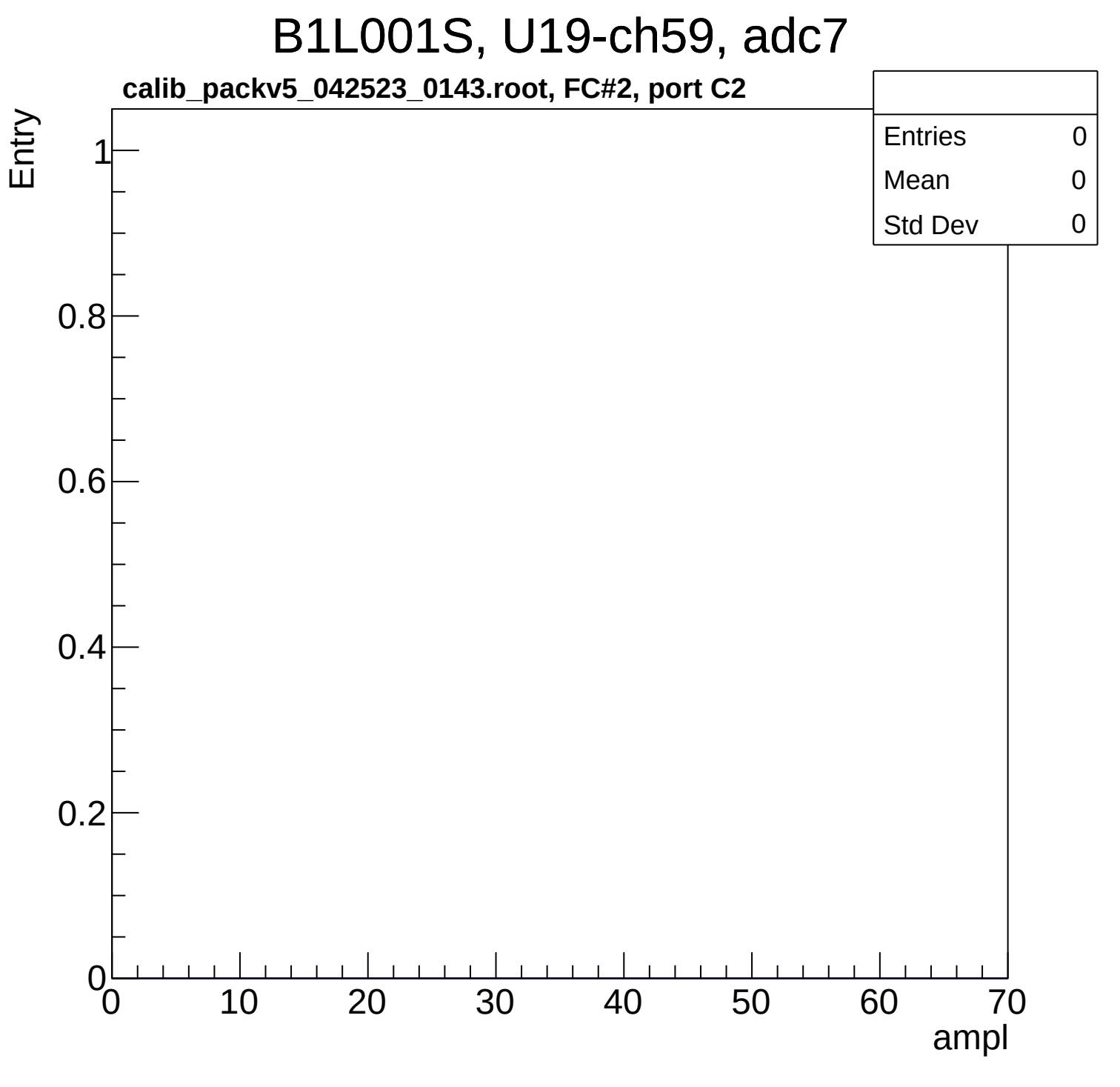
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch59, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 0
Mean 0
Std Dev 0
Entry
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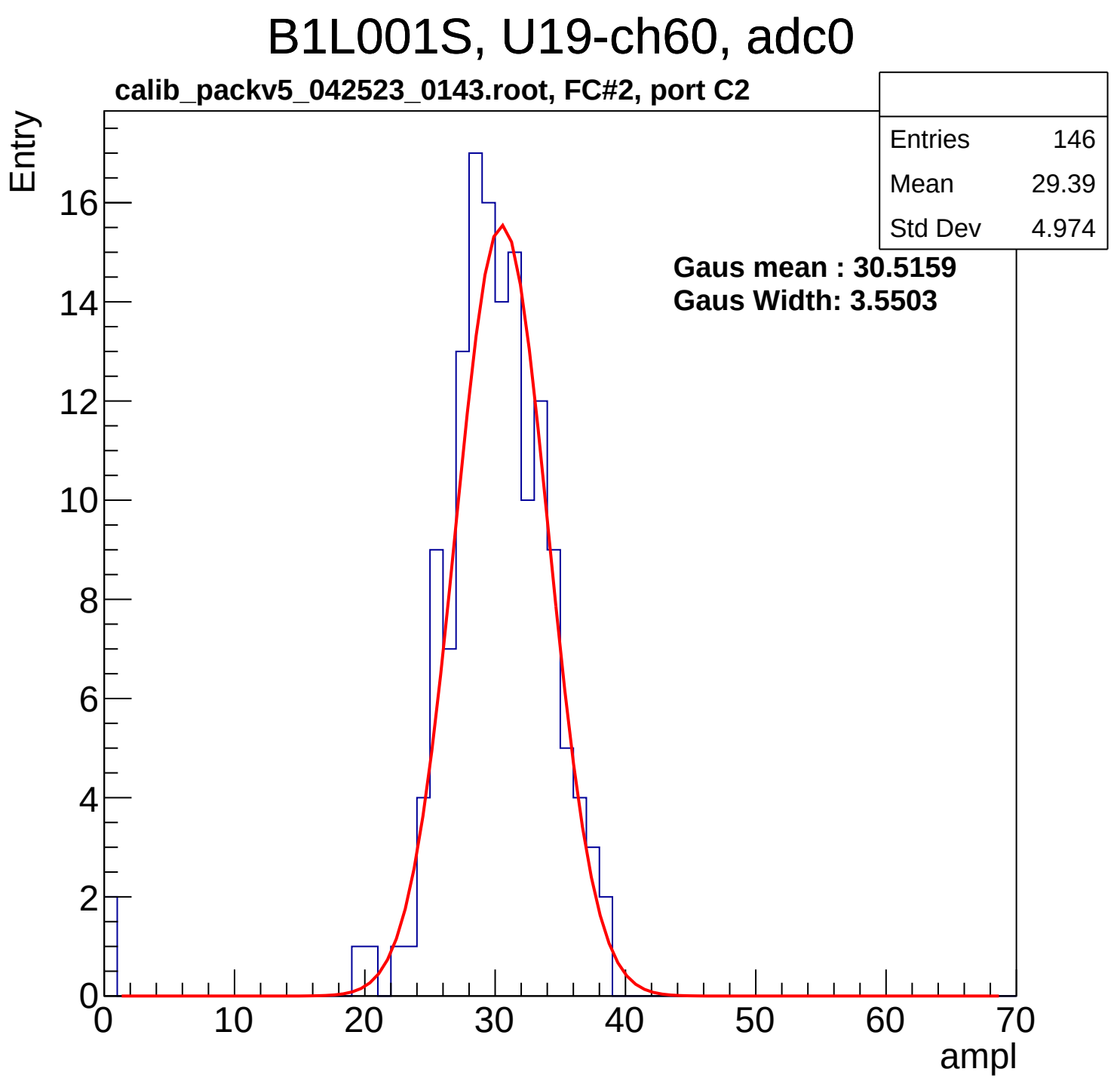
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch60, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 146
Mean 29.39
Std Dev 4.974
Gaus mean : 30.5159
Gaus Width: 3.5503
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
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60
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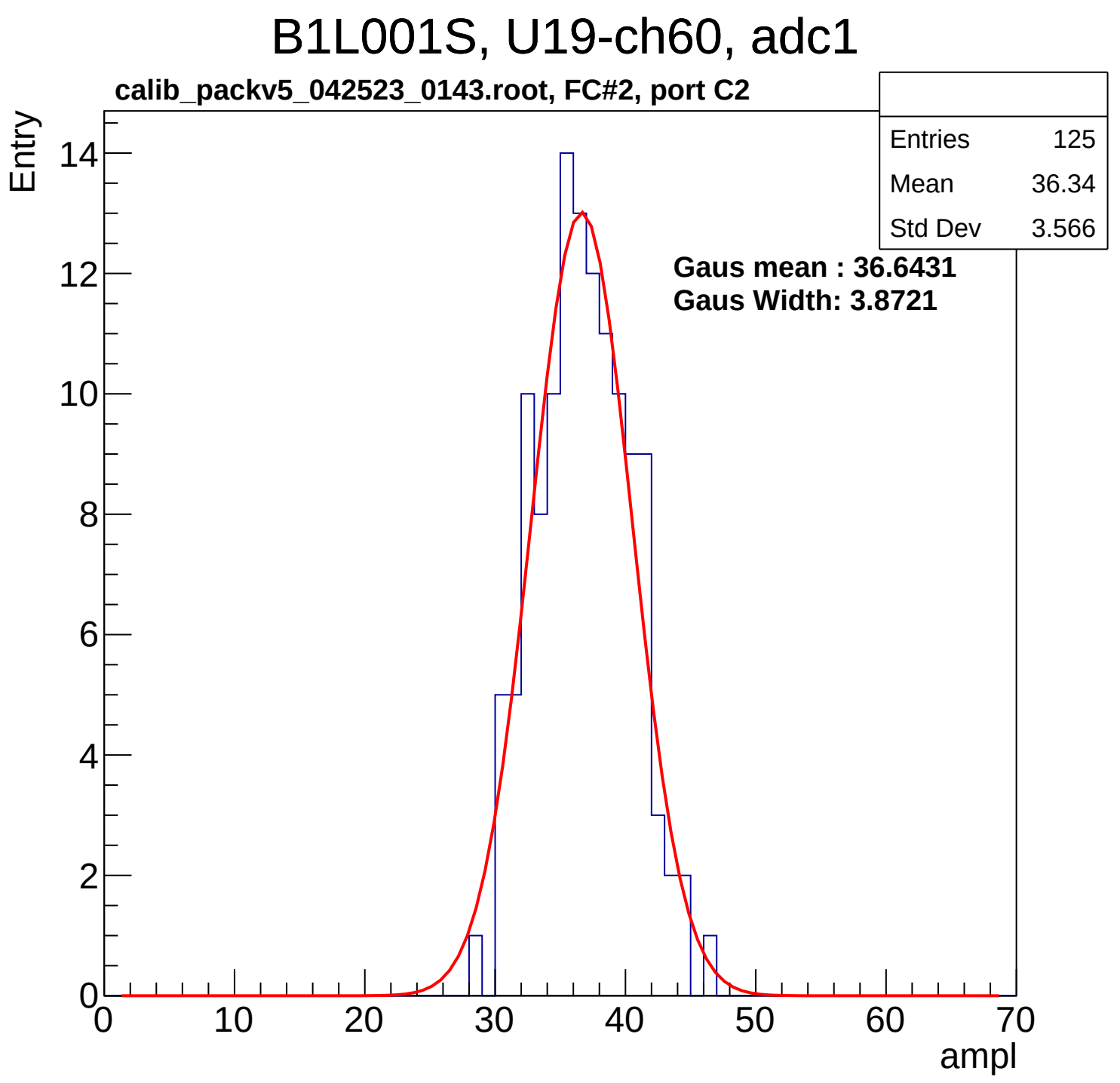
B1L001S, U19-ch60, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 125
Mean 36.34
Std Dev 3.566
Gaus mean : 36.6431
Gaus Width: 3.8721
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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40
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60
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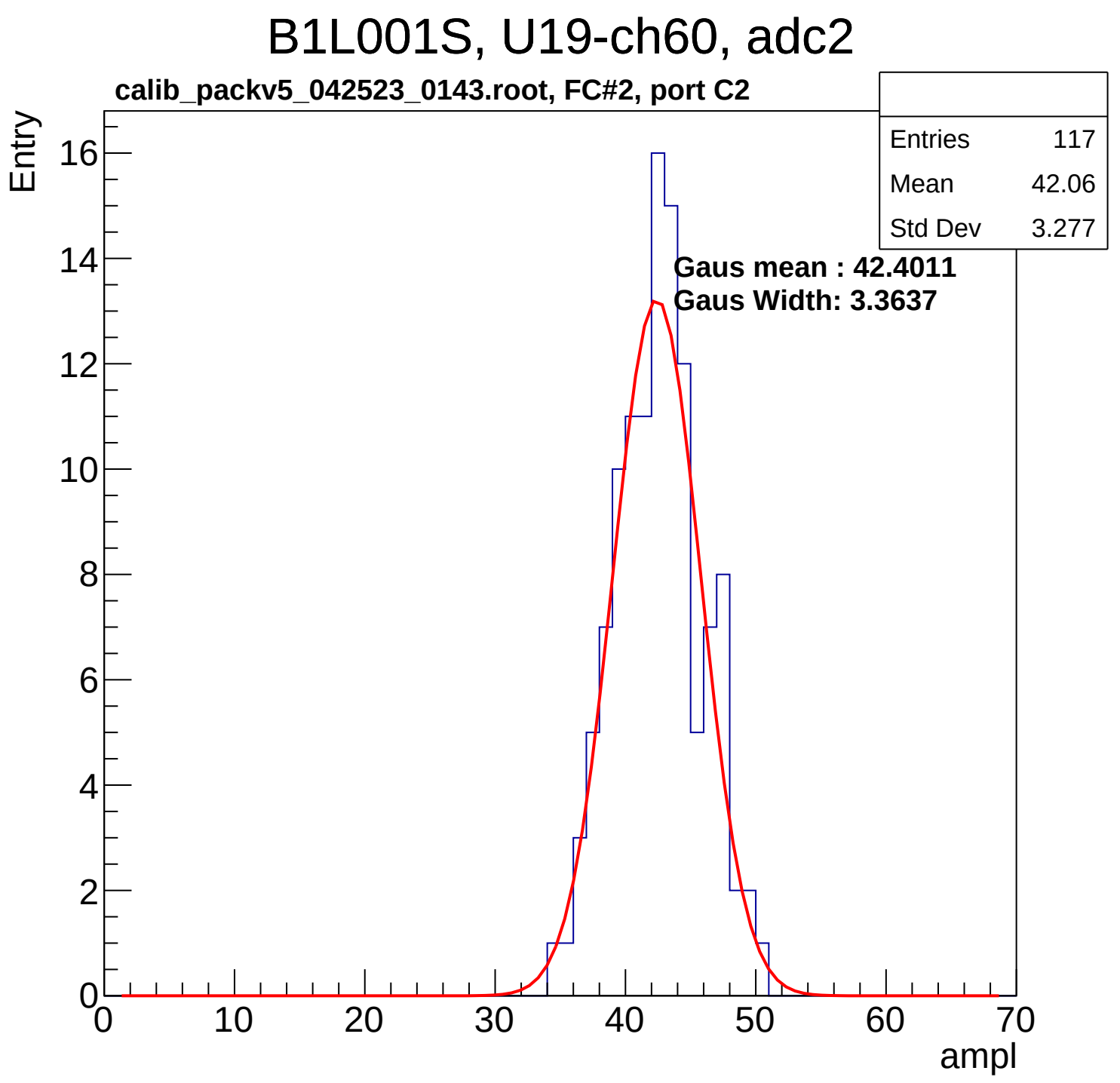
B1L001S, U19-ch60, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 117
Mean 42.06
Std Dev 3.277
Gaus mean : 42.4011
Gaus Width: 3.3637
Entry
ampl
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2
4
6
8
10
12
14
16
0
10
20
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40
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60
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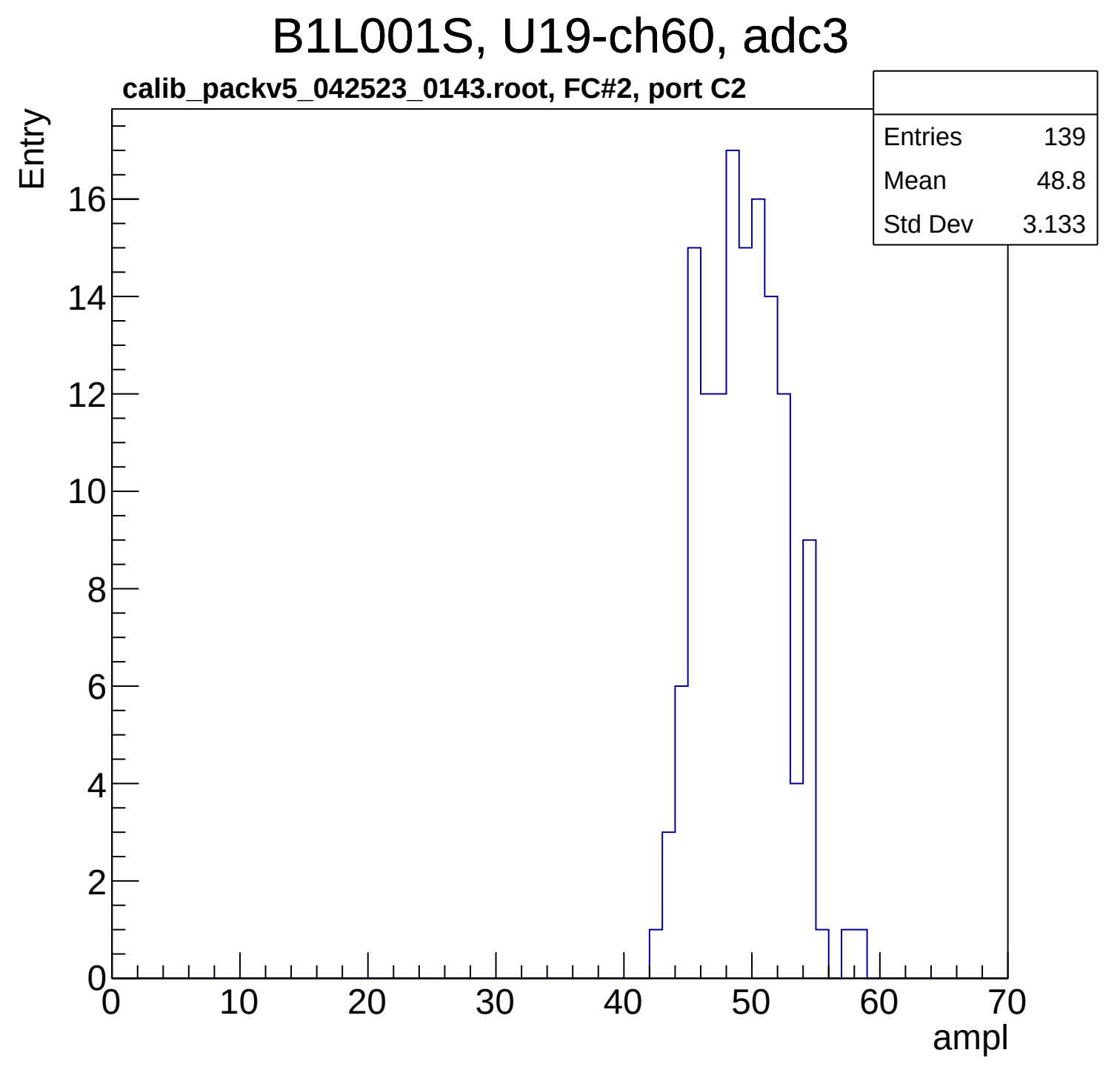
B1L001S, U19-ch60, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 139
Mean 48.8
Std Dev 3.133
Entry
0
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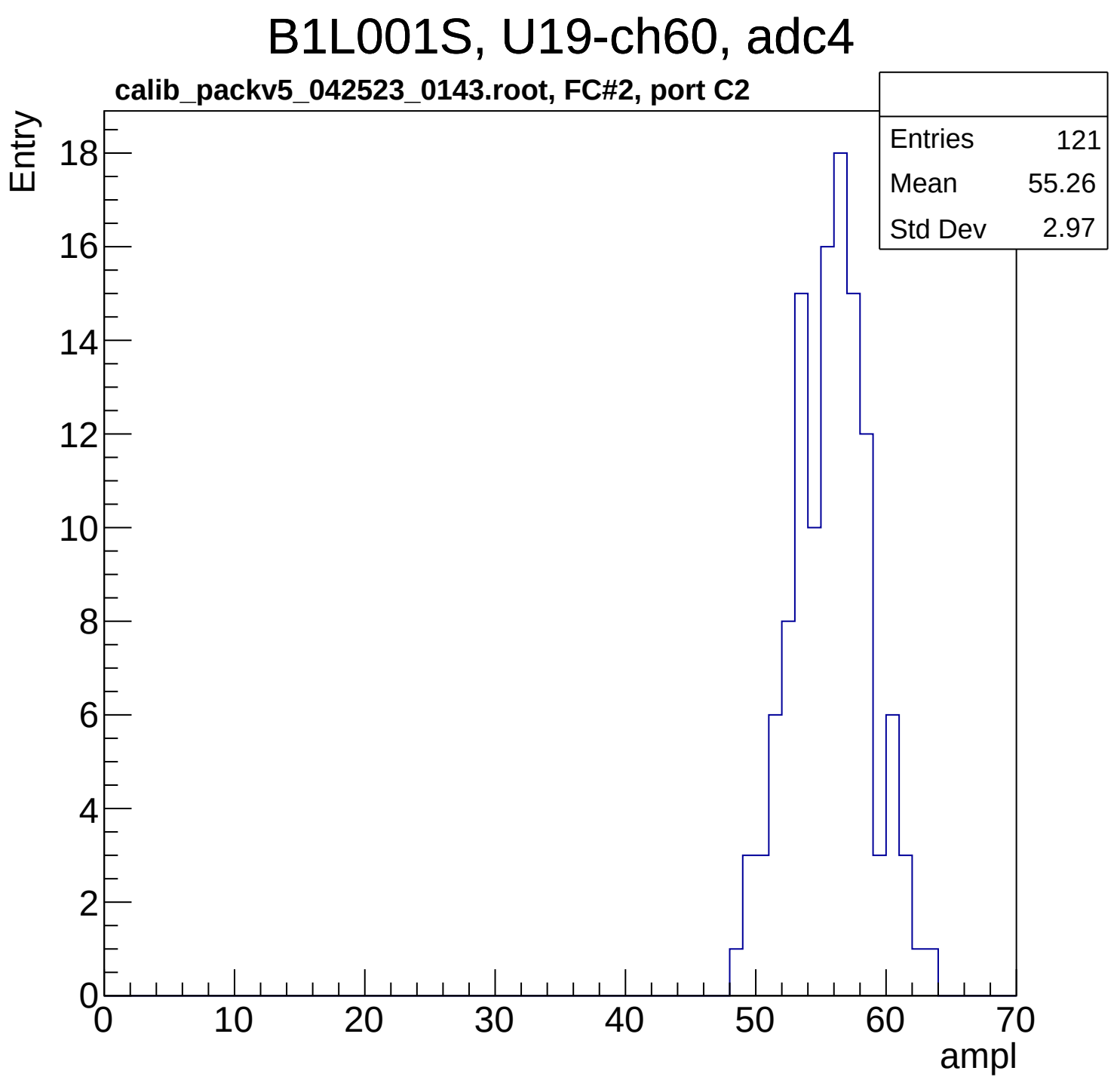
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch60, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 121
Mean 55.26
Std Dev 2.97
Entry
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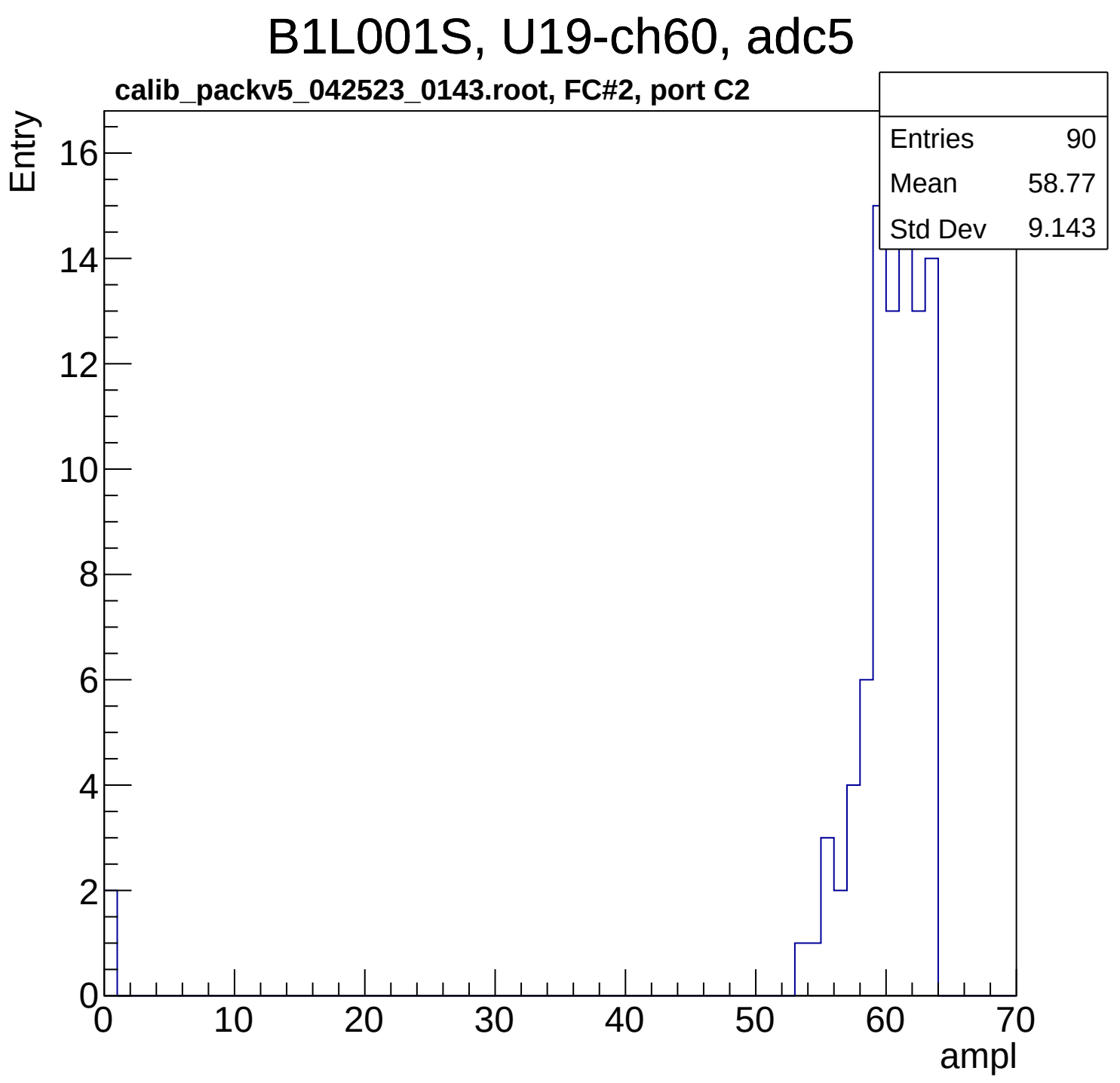
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch60, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 90
Mean 58.77
Std Dev 9.143
Entry
0
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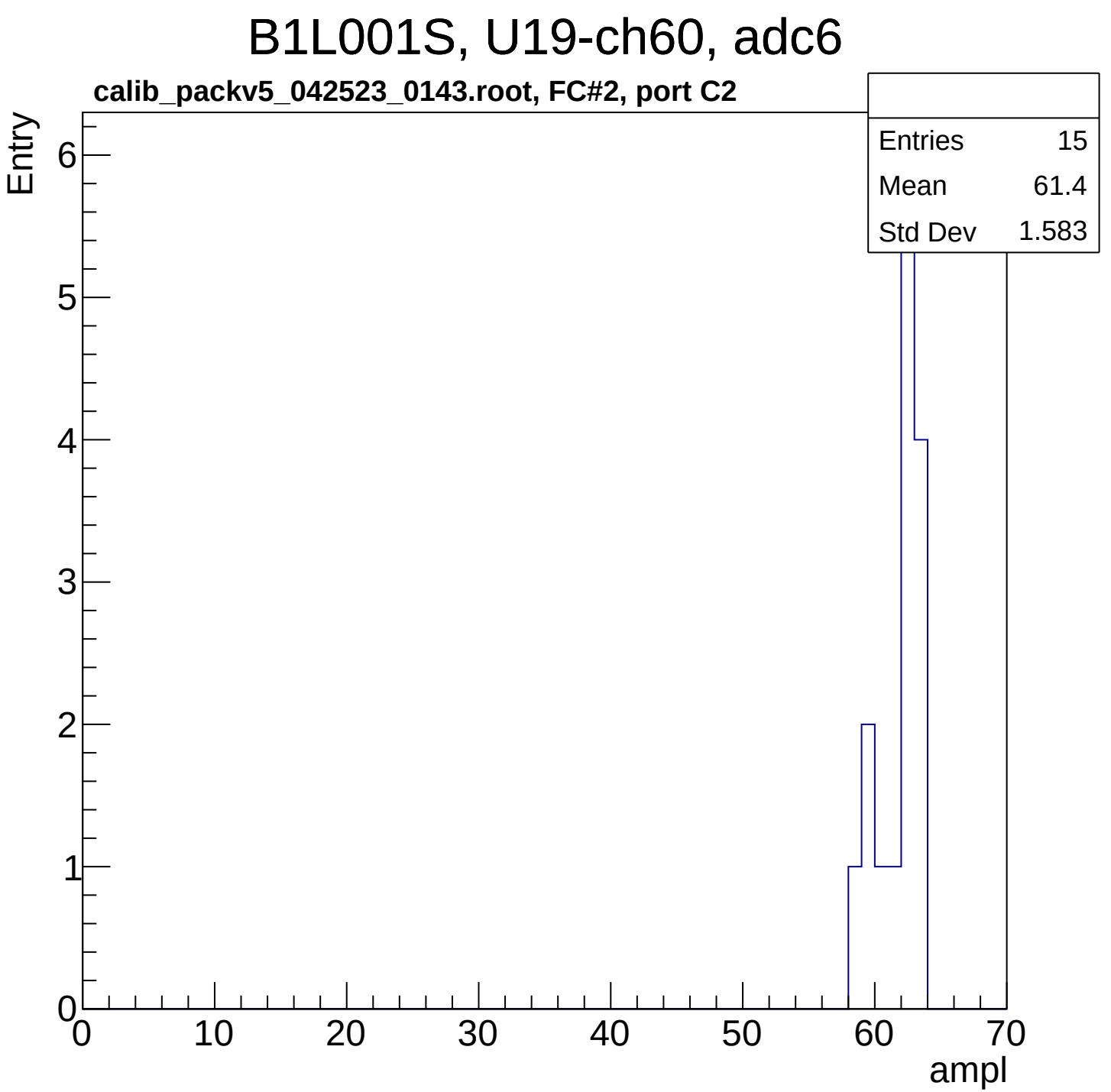
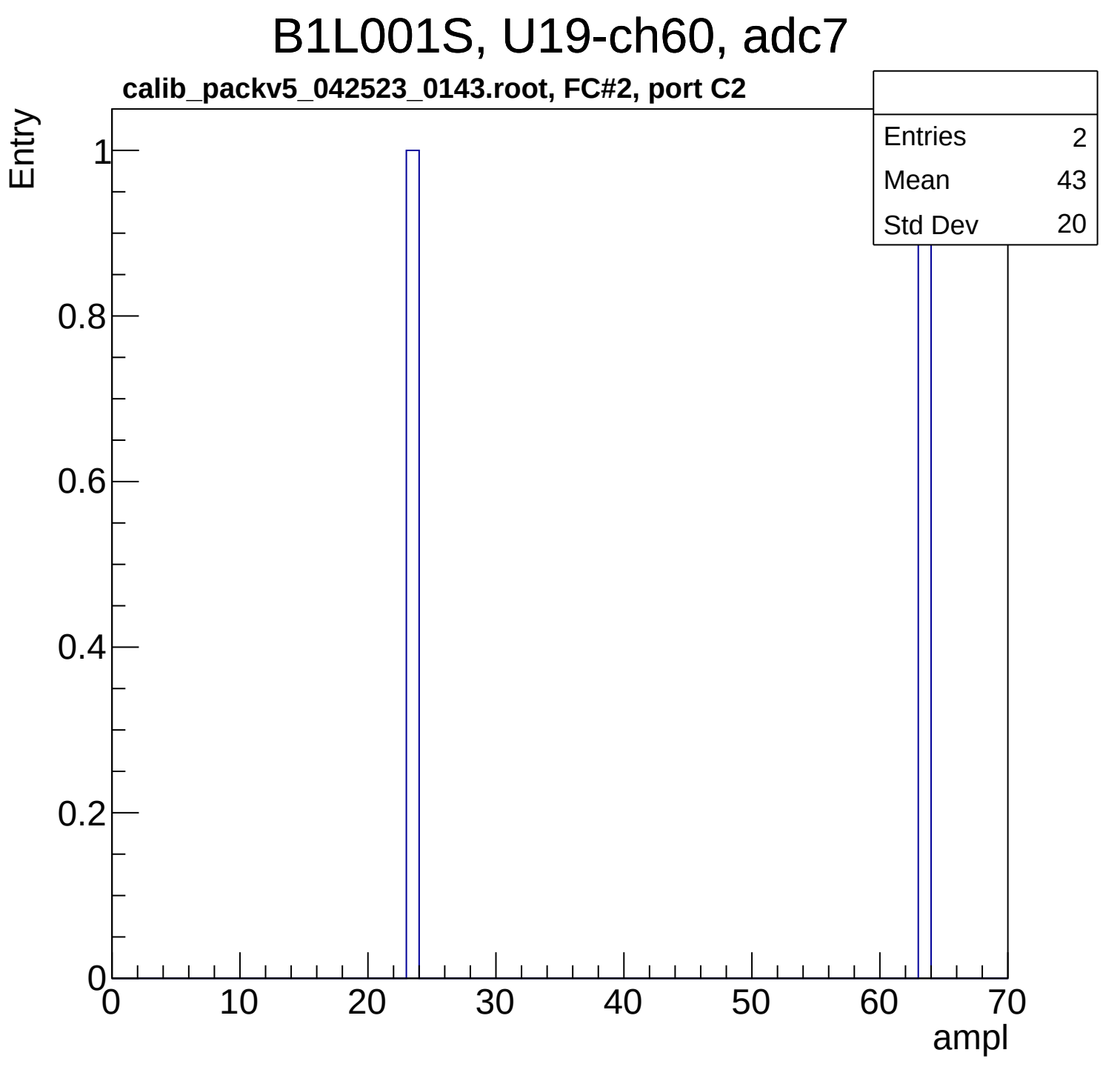
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch60, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 15
Mean 61.4
Std Dev 1.583
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch60, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 43
Std Dev 20
Entry
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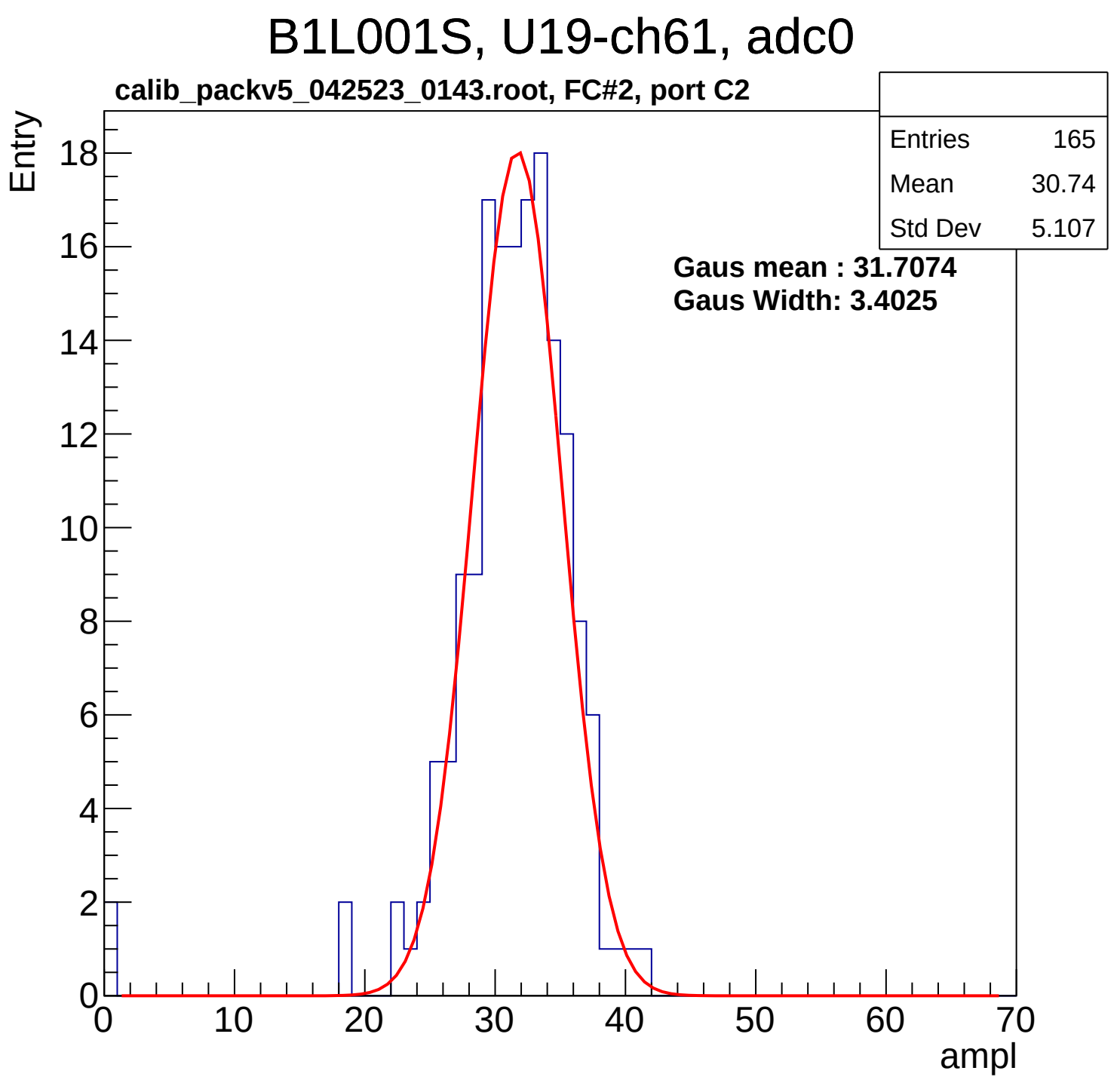
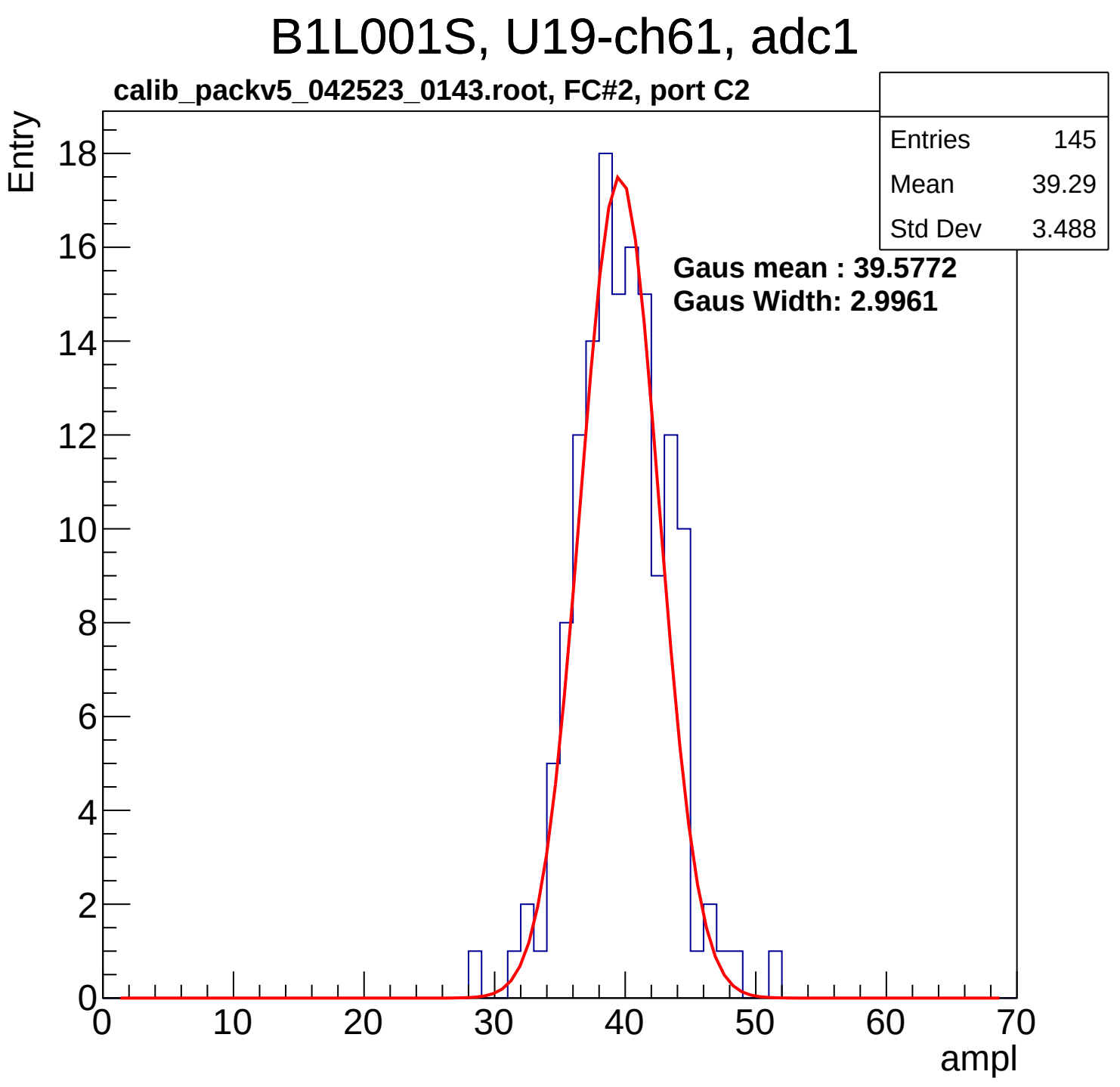
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch61, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 165
Mean 30.74
Std Dev 5.107
Gaus mean : 31.7074
Gaus Width: 3.4025
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70


B1L001S, U19-ch61, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 145
Mean 39.29
Std Dev 3.488
Gaus mean : 39.5772
Gaus Width: 2.9961
Entry
ampl
0
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4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
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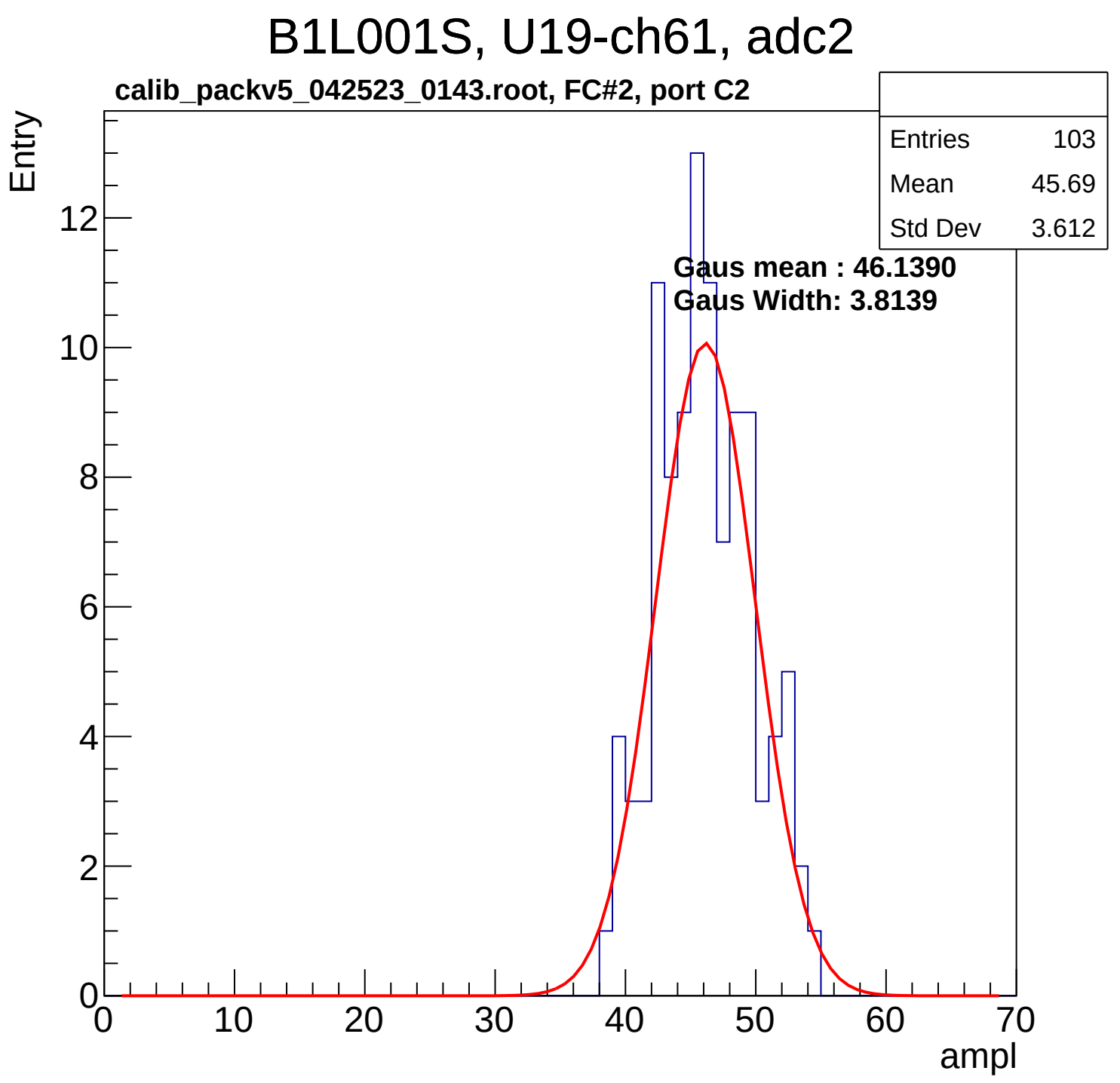
B1L001S, U19-ch61, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 103
Mean 45.69
Std Dev 3.612
Gaus mean : 46.1390
Gaus Width: 3.8139
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
50
60
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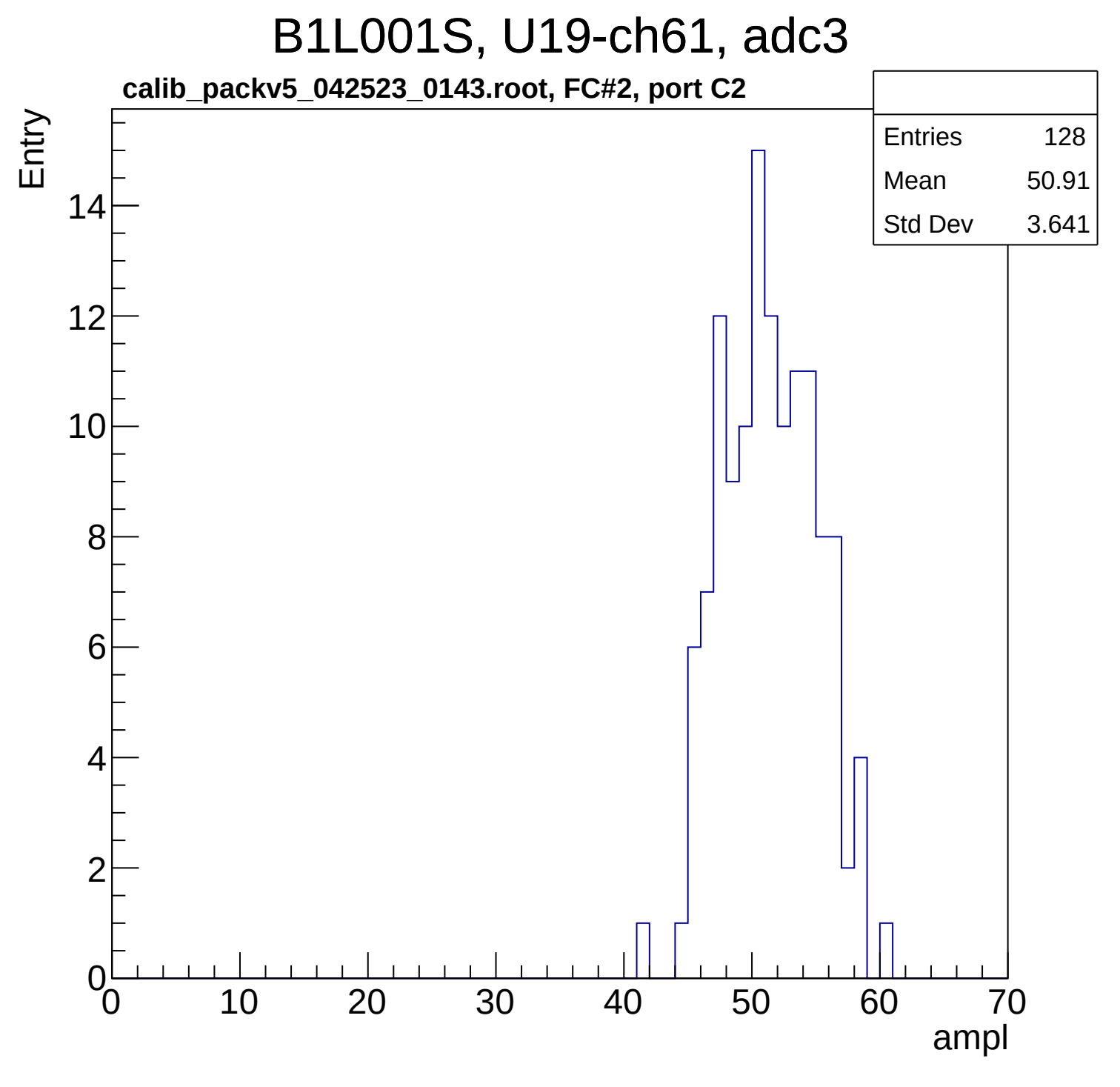
B1L001S, U19-ch61, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 128
Mean 50.91
Std Dev 3.641
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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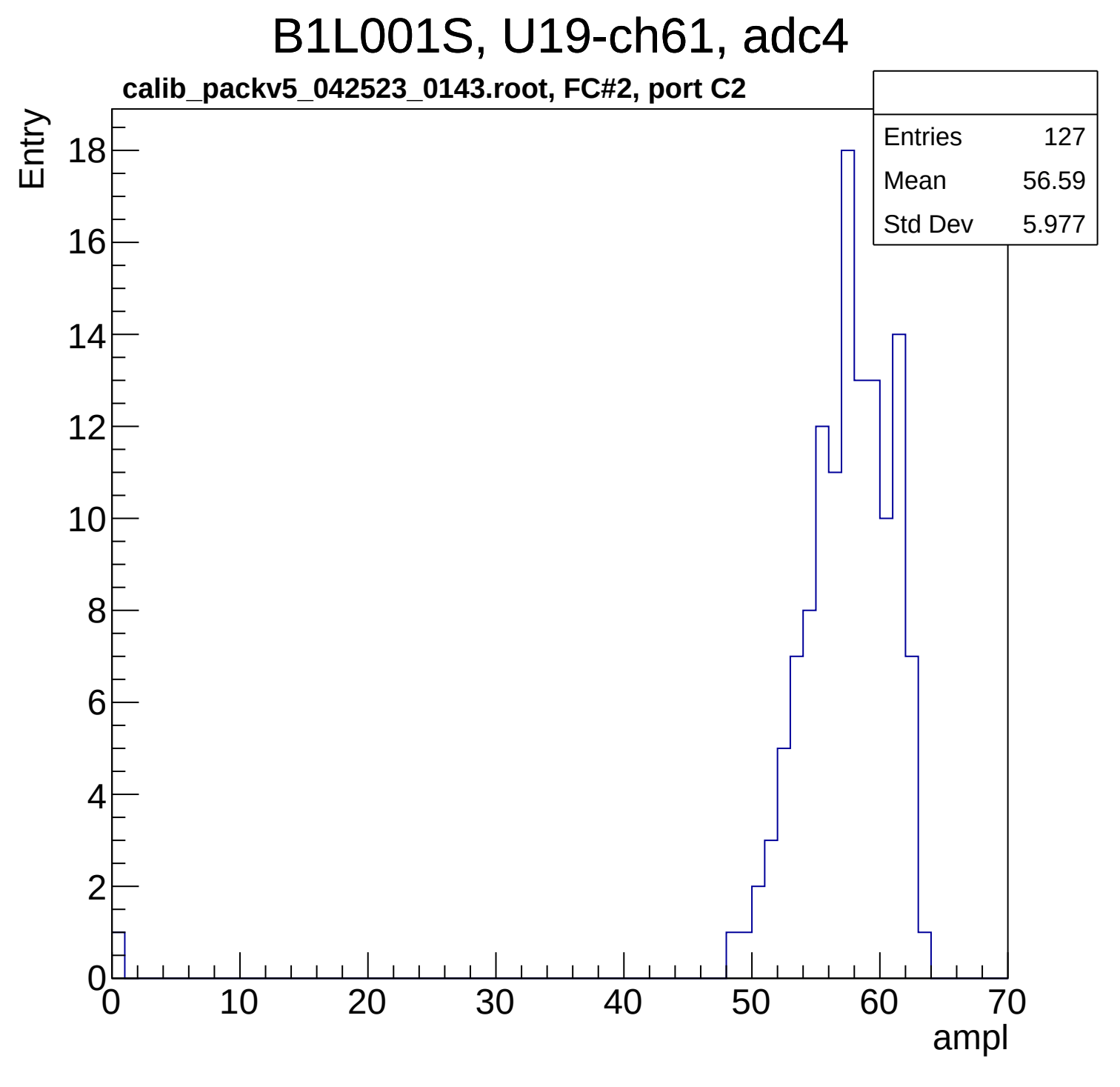
B1L001S, U19-ch61, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 127
Mean 56.59
Std Dev 5.977
Entry
ampl
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2
4
6
8
10
12
14
16
18
0
10
20
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40
50
60
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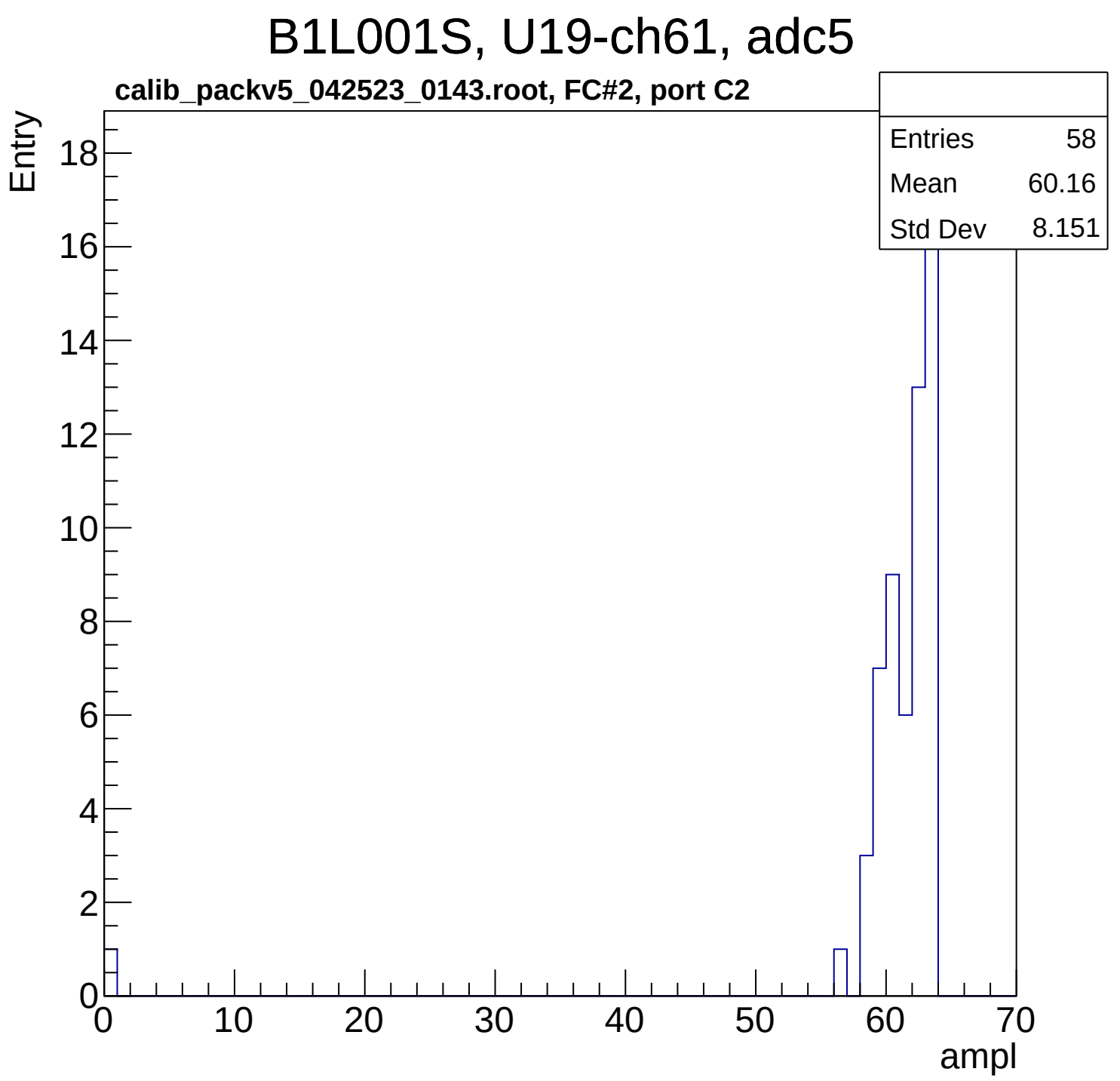
B1L001S, U19-ch61, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 58
Mean 60.16
Std Dev 8.151
Entry
ampl
0
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4
6
8
10
12
14
16
18
0
10
20
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40
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60
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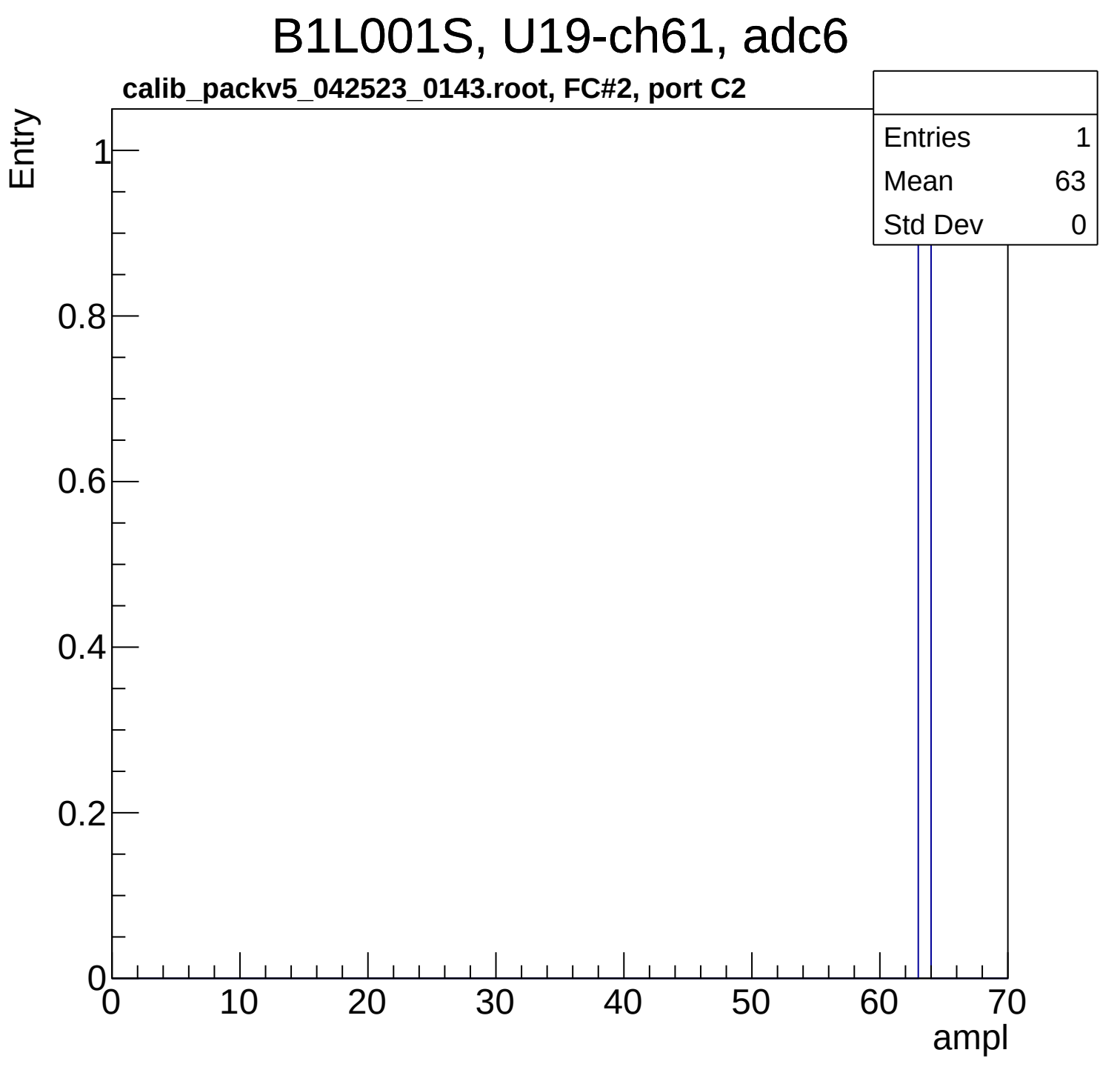
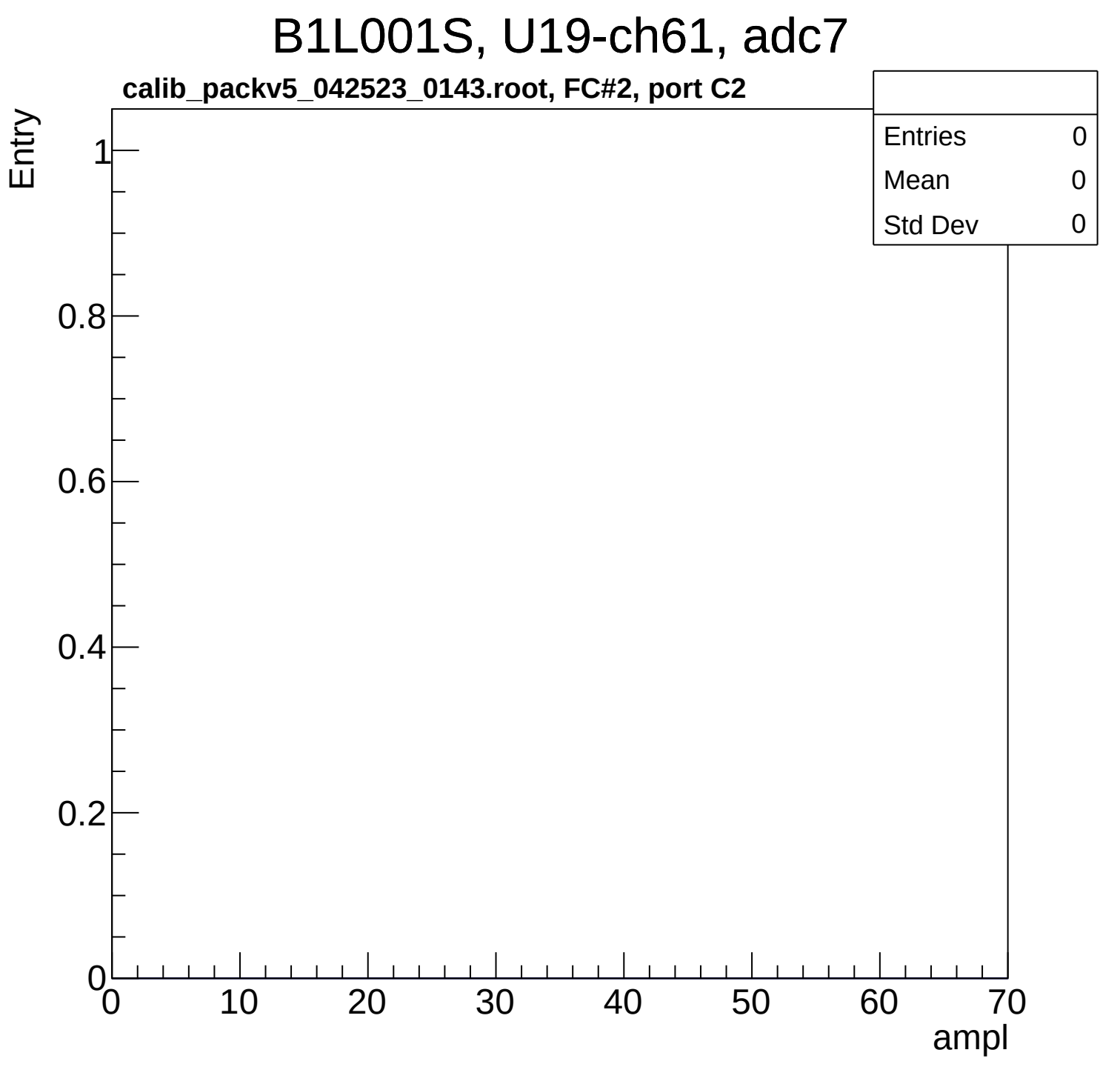
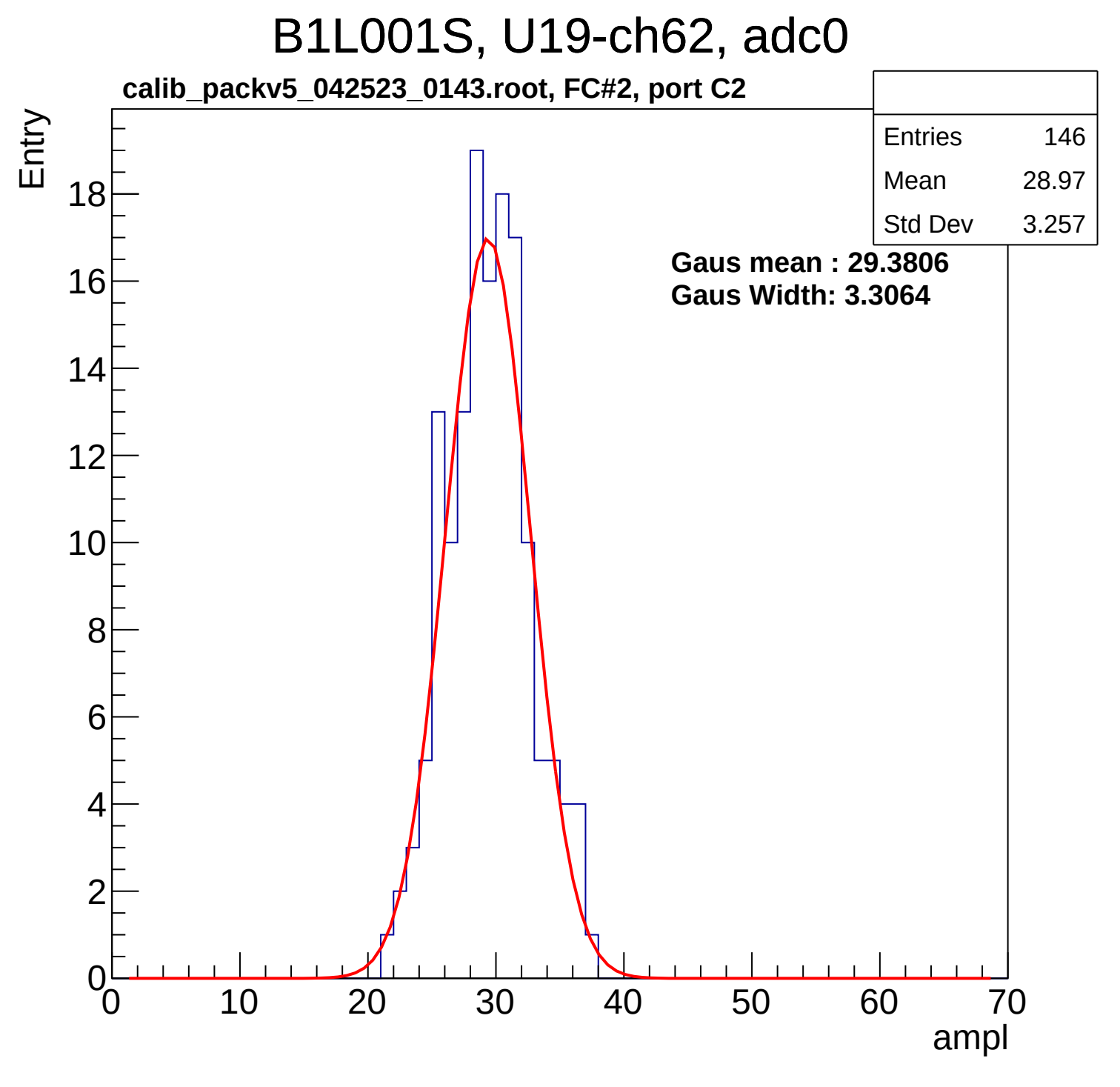

B1L001S, U19-ch61, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 63
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch61, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch62, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 146
Mean 28.97
Std Dev 3.257
Gaus mean : 29.3806
Gaus Width: 3.3064
Entry
ampl
0
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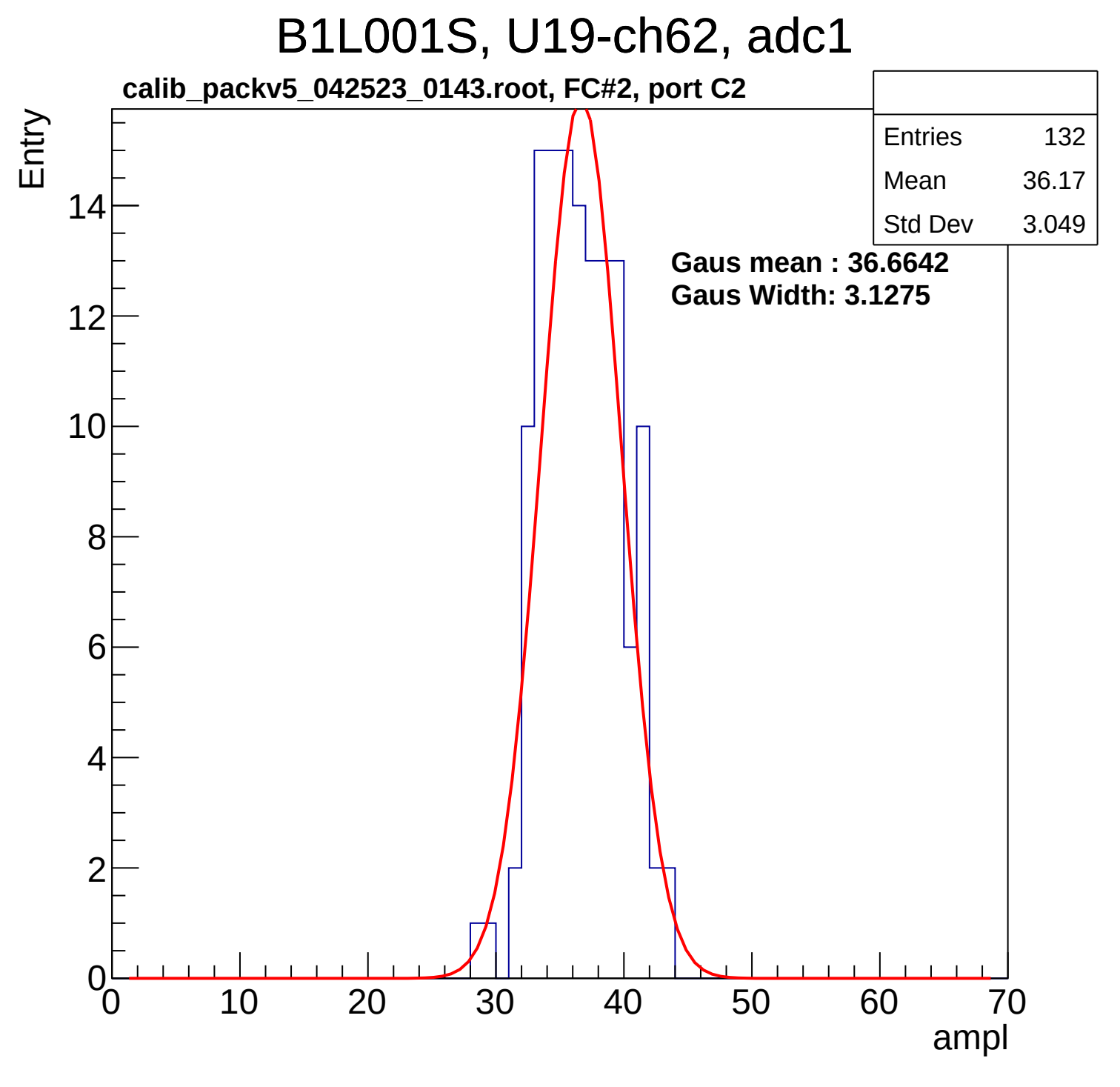
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70


B1L001S, U19-ch62, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 132
Mean 36.17
Std Dev 3.049
Gaus mean : 36.6642
Gaus Width: 3.1275
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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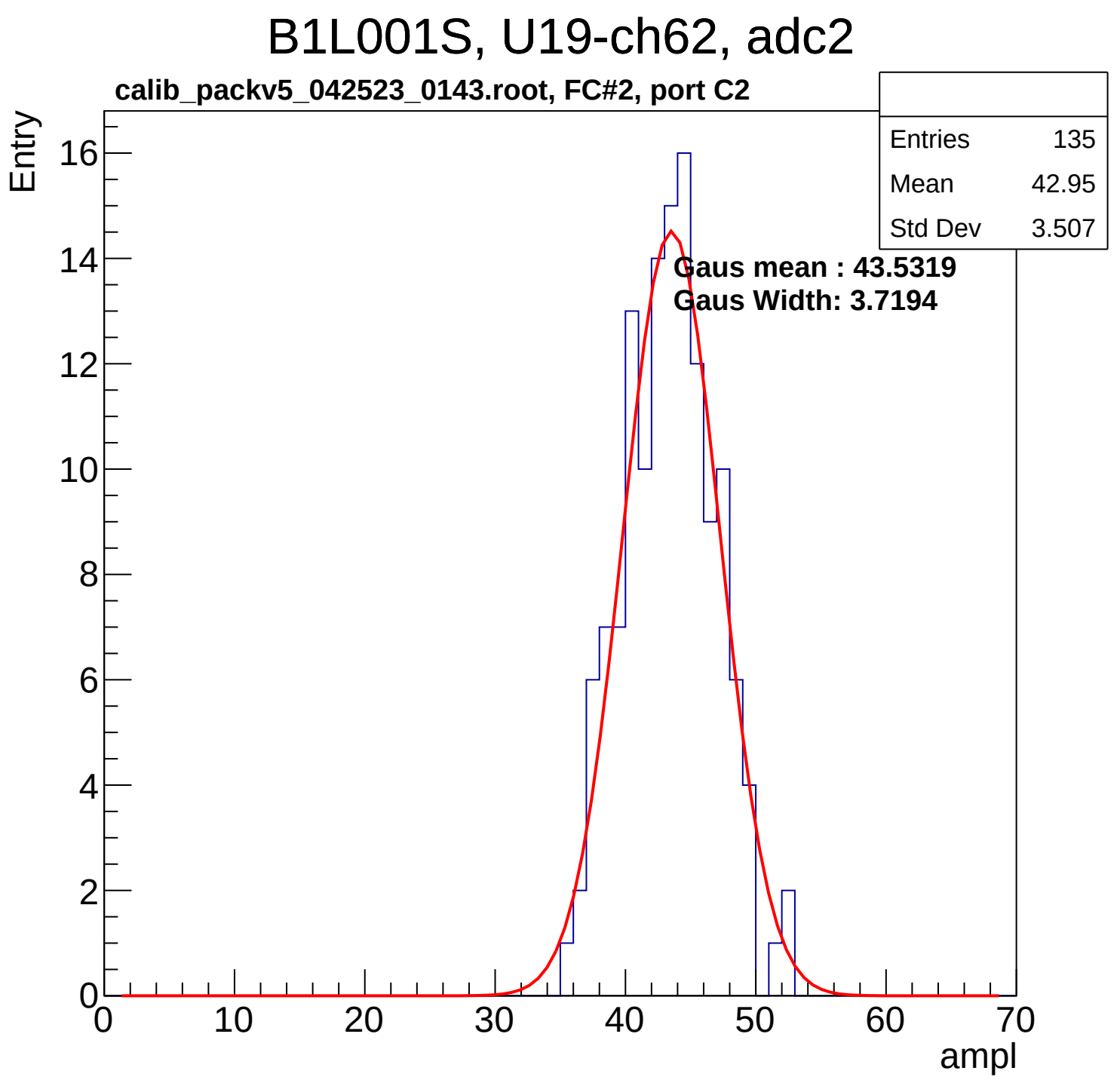
B1L001S, U19-ch62, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 135
Mean 42.95
Std Dev 3.507
Gaus mean : 43.5319
Gaus Width: 3.7194
Entry
ampl
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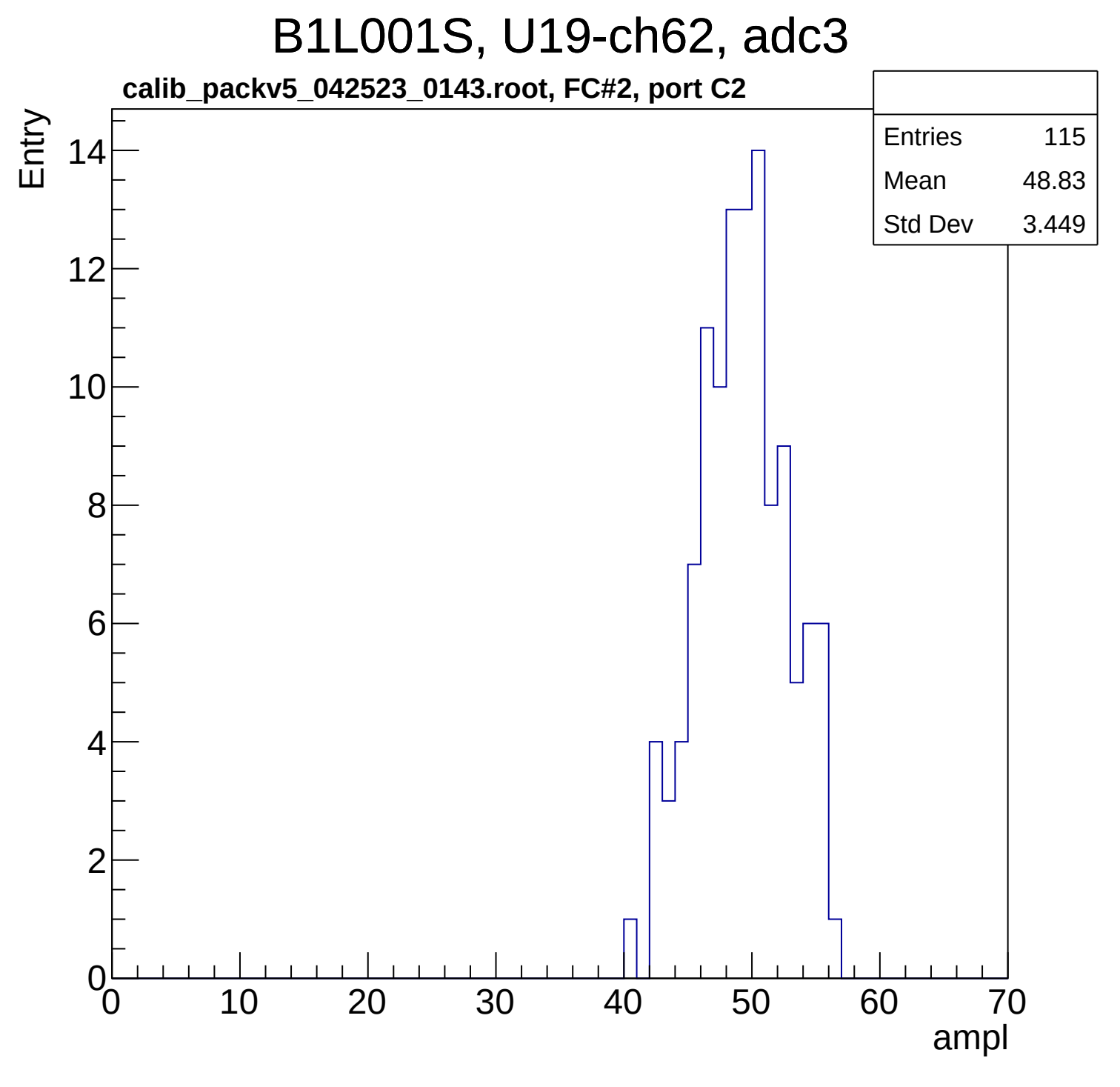
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70


B1L001S, U19-ch62, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 115
Mean 48.83
Std Dev 3.449
Entry
ampl
0
2
4
6
8
10
12
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0
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60
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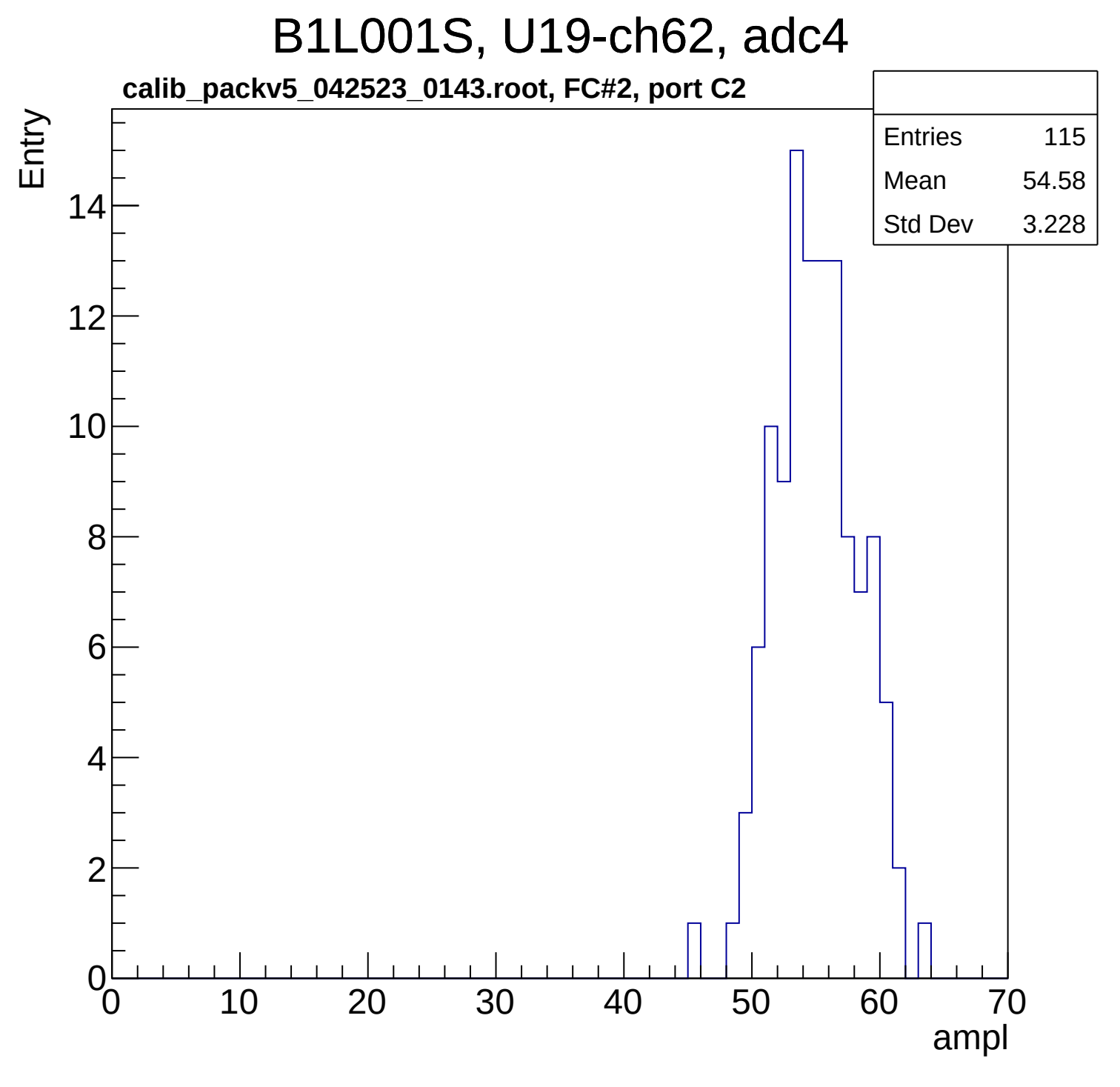
B1L001S, U19-ch62, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 115
Mean 54.58
Std Dev 3.228
Entry
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10
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10
20
30
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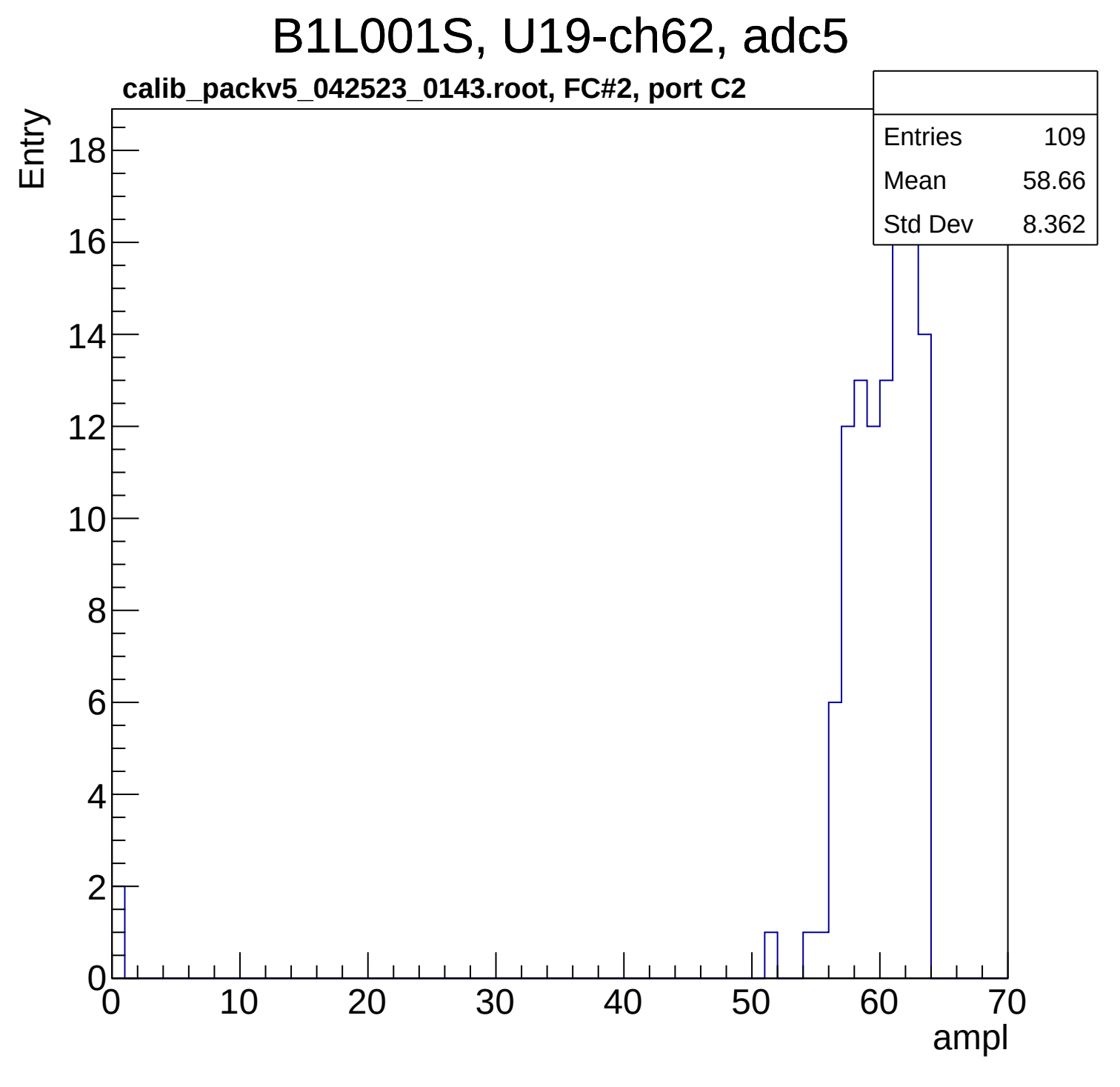
50
60
70
ampl


B1L001S, U19-ch62, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 109
Mean 58.66
Std Dev 8.362
Entry
ampl
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6
8
10
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16
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0
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60
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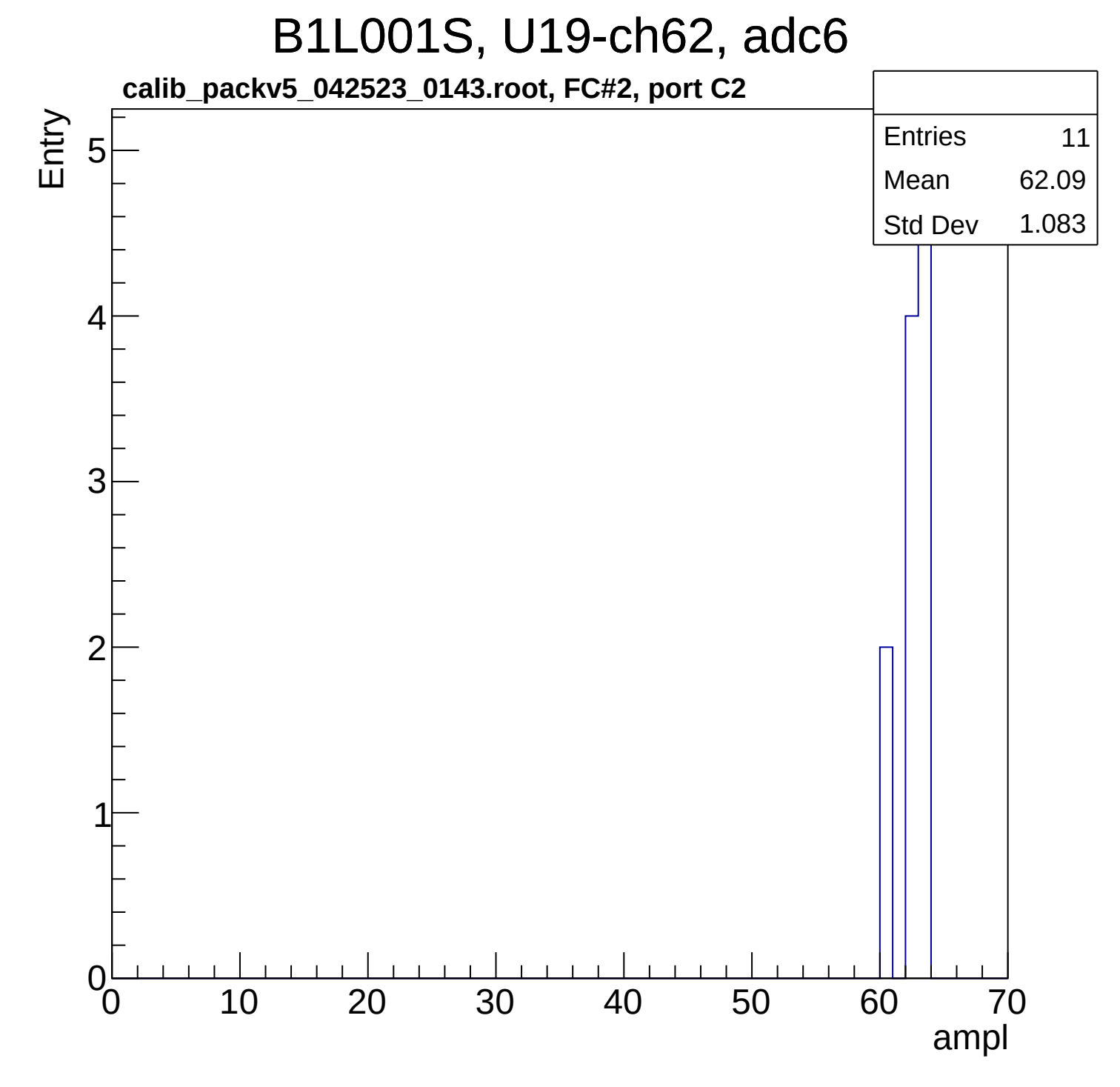
B1L001S, U19-ch62, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 11
Mean 62.09
Std Dev 1.083
Entry
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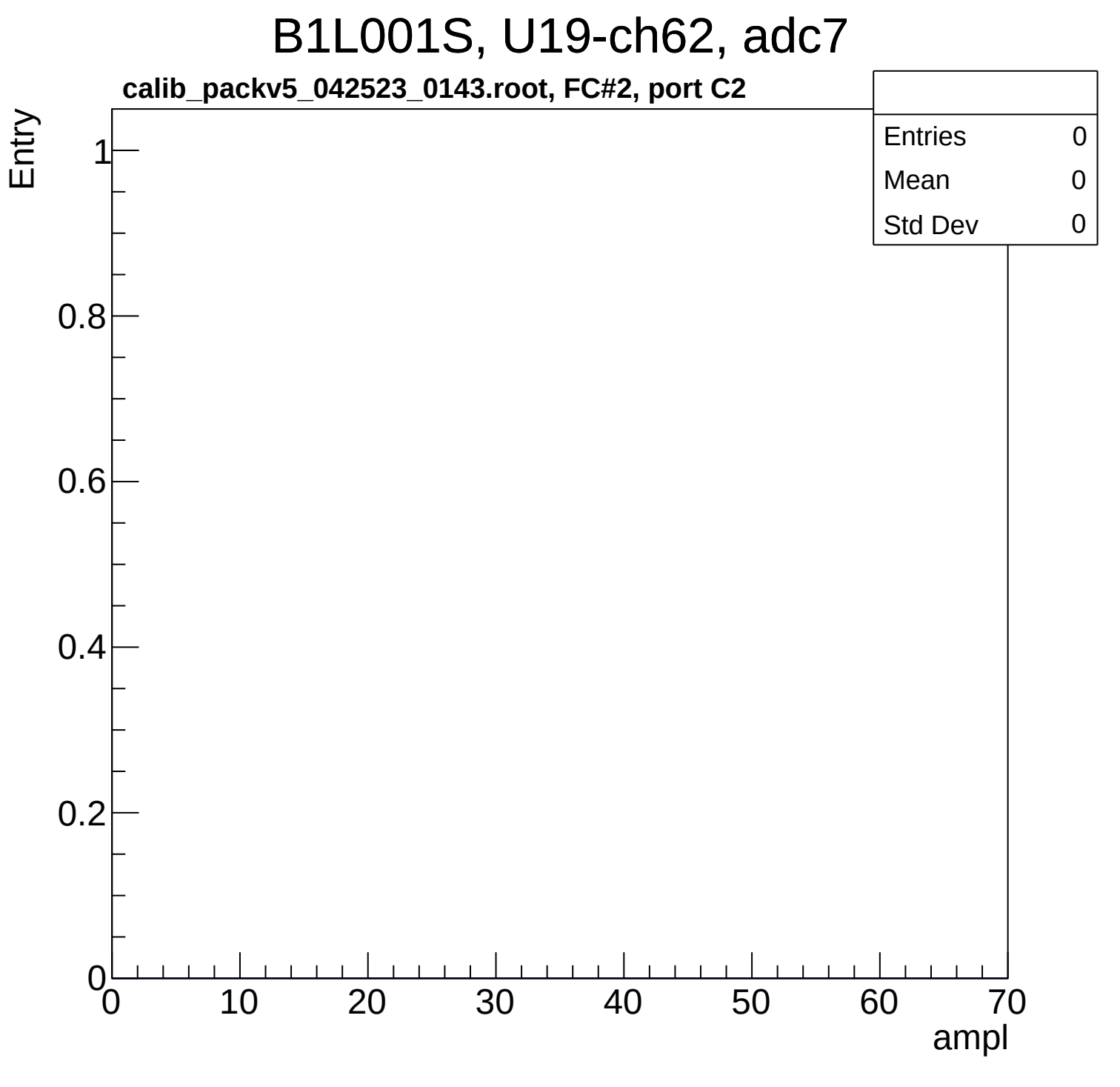
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch62, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 0
Mean 0
Std Dev 0
Entry
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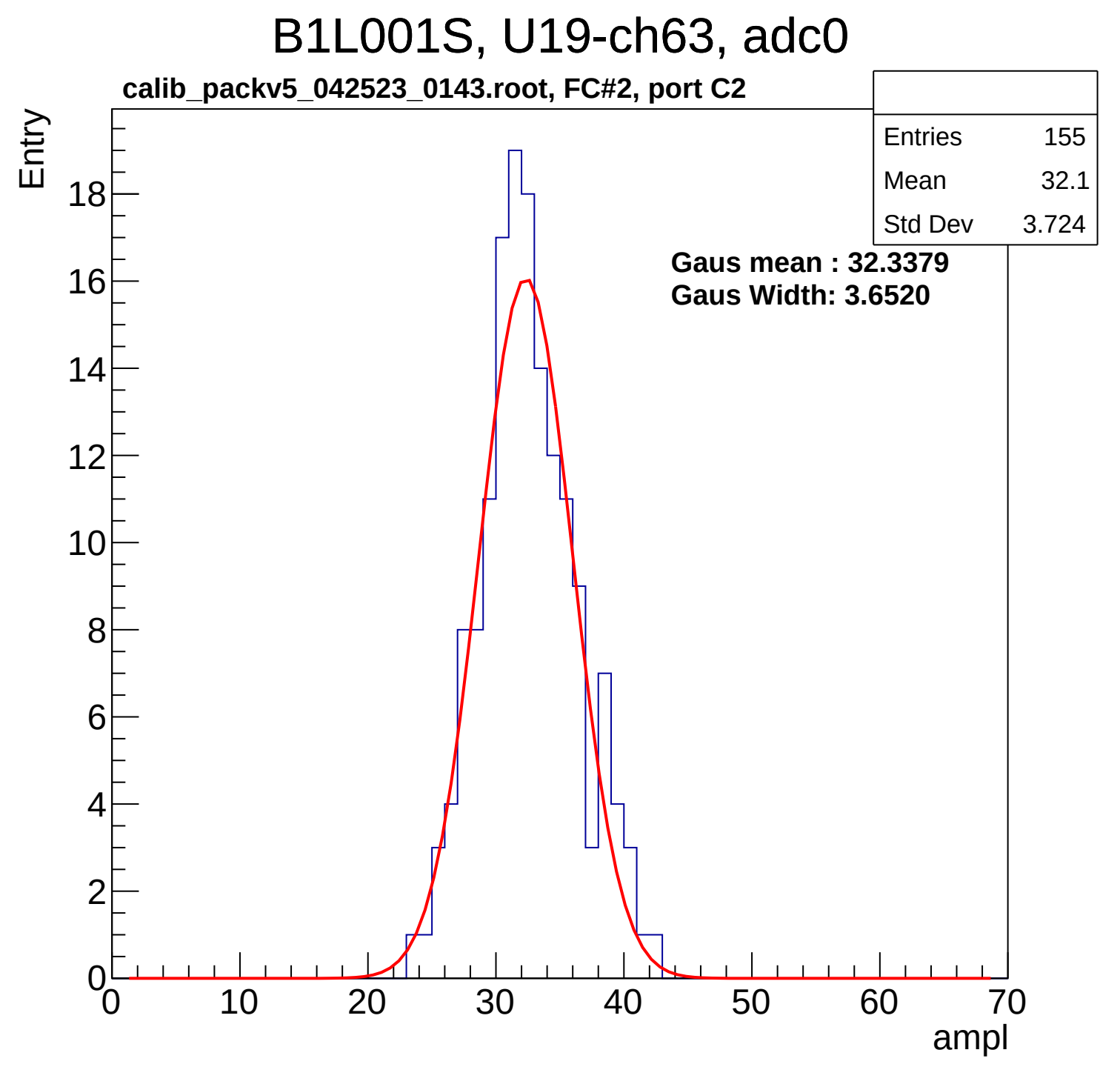
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch63, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 155
Mean 32.1
Std Dev 3.724
Gaus mean : 32.3379
Gaus Width: 3.6520
Entry
ampl
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4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
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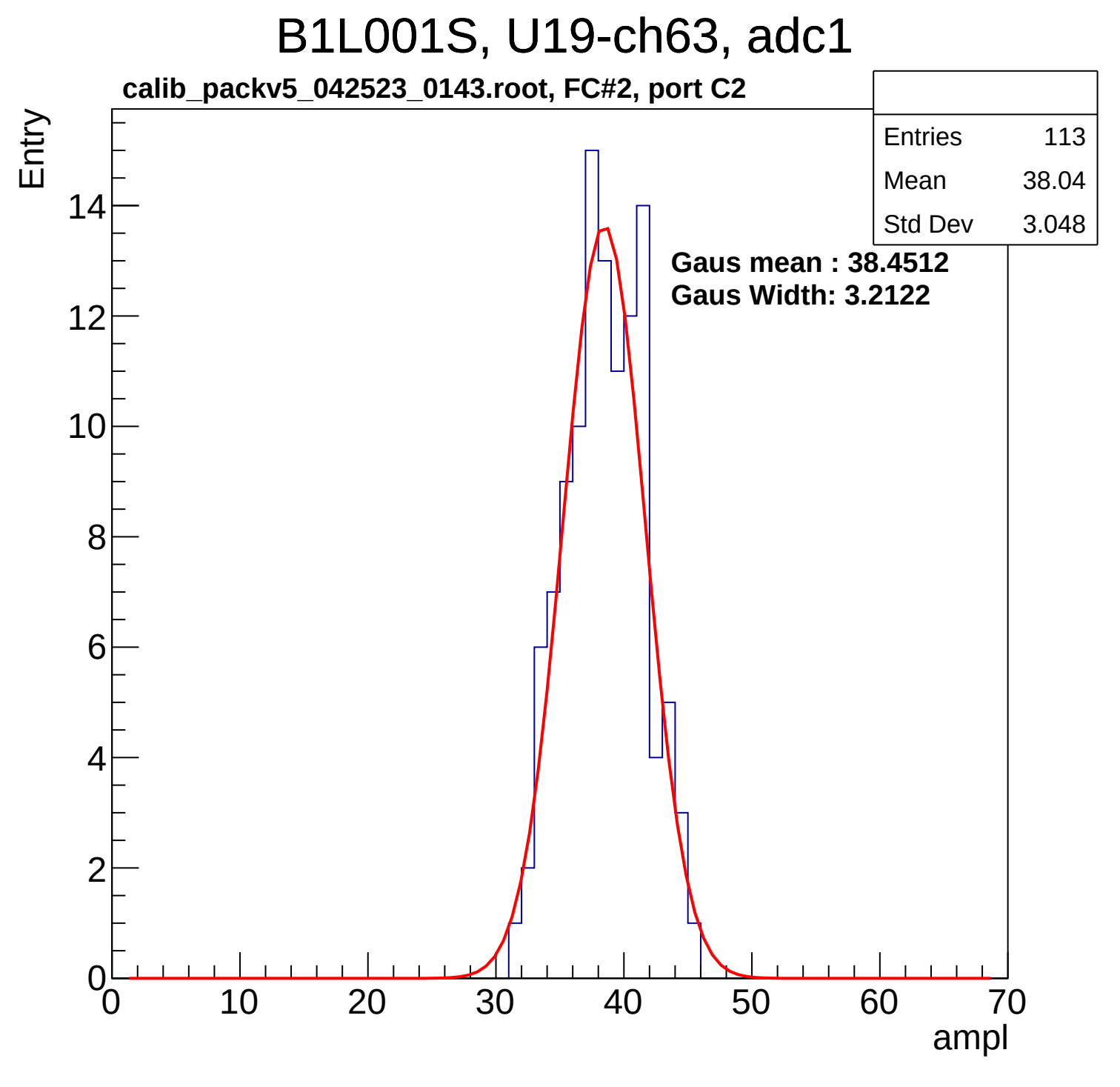
B1L001S, U19-ch63, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 113
Mean 38.04
Std Dev 3.048
Gaus mean : 38.4512
Gaus Width: 3.2122
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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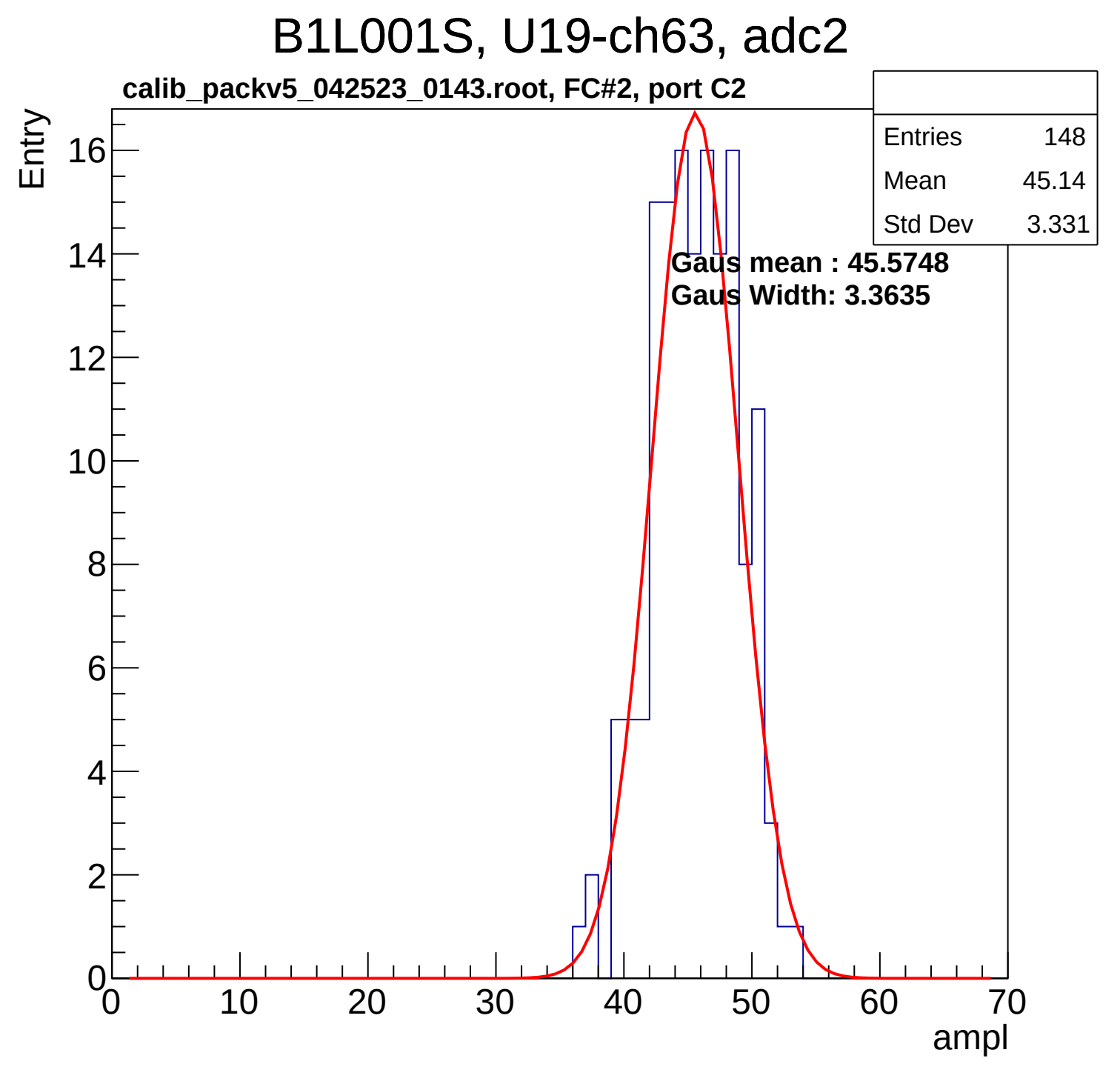
B1L001S, U19-ch63, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 148
Mean 45.14
Std Dev 3.331
Gaus mean : 45.5748
Gaus Width: 3.3635
Entry
ampl
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2
4
6
8
10
12
14
16
0
10
20
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40
50
60
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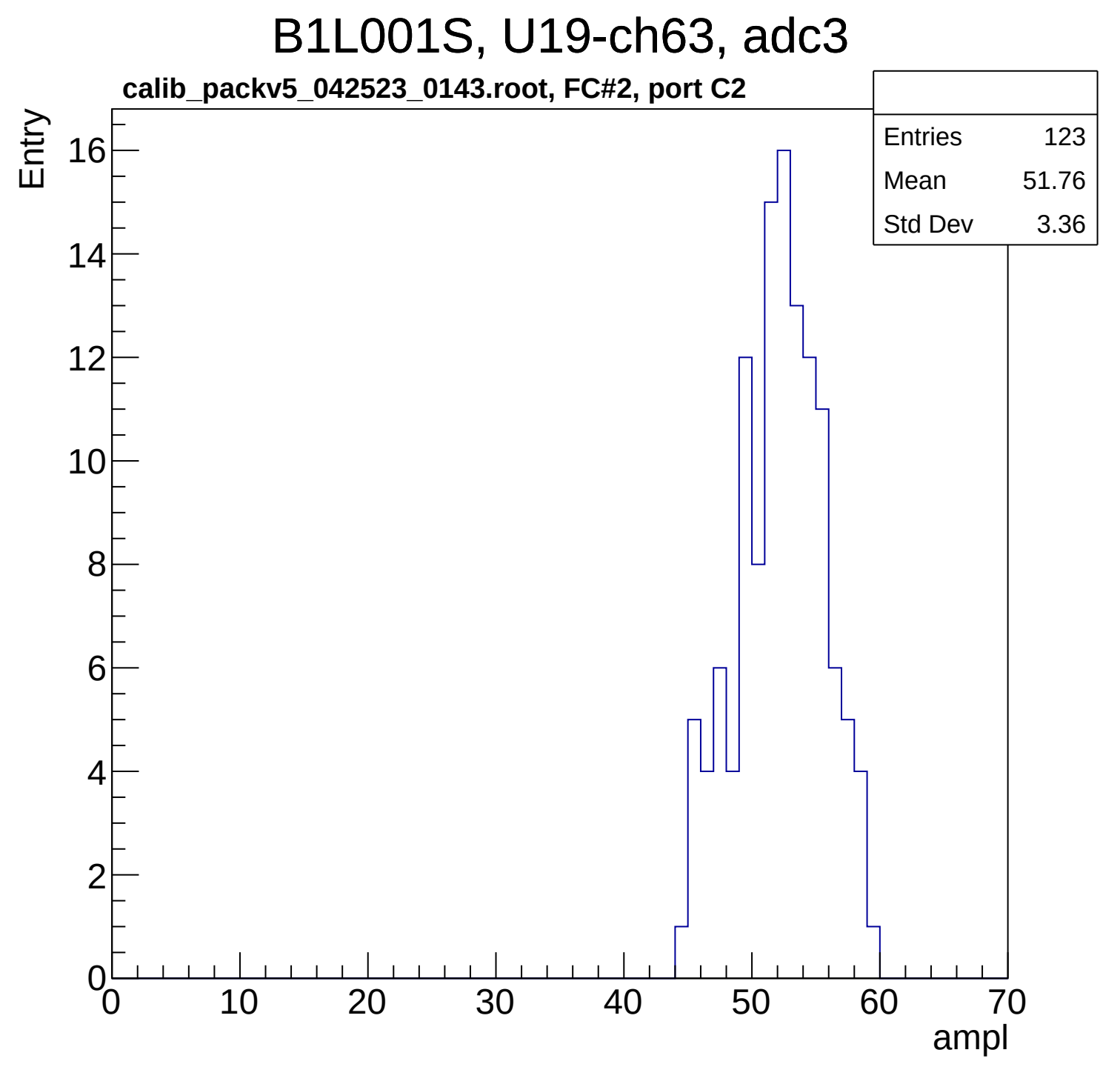
B1L001S, U19-ch63, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 123
Mean 51.76
Std Dev 3.36
Entry
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6
8
10
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16
0
10
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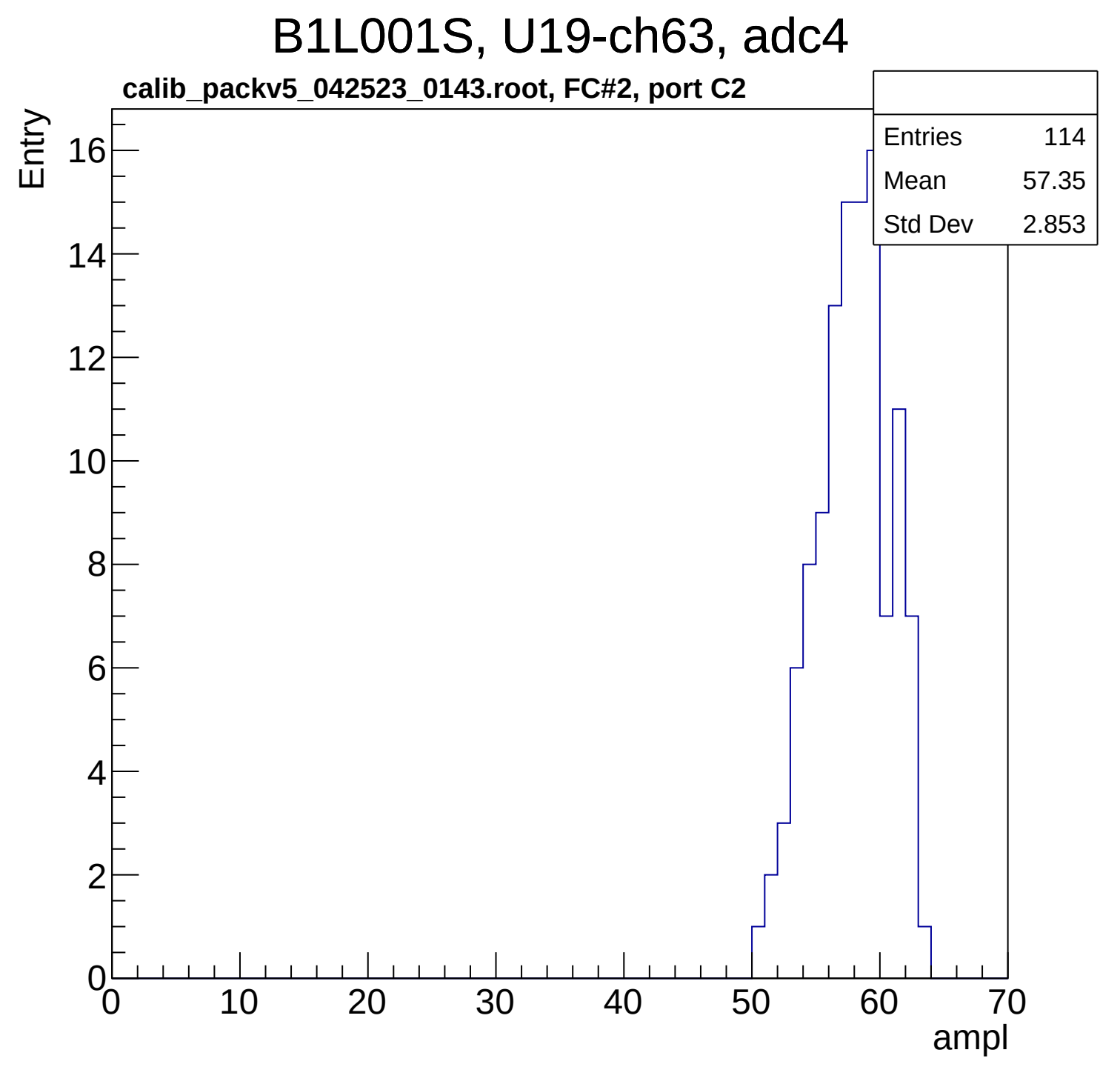
30
40
50
60
70
ampl


B1L001S, U19-ch63, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 114
Mean 57.35
Std Dev 2.853
Entry
ampl
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8
10
12
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16
0
10
20
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60
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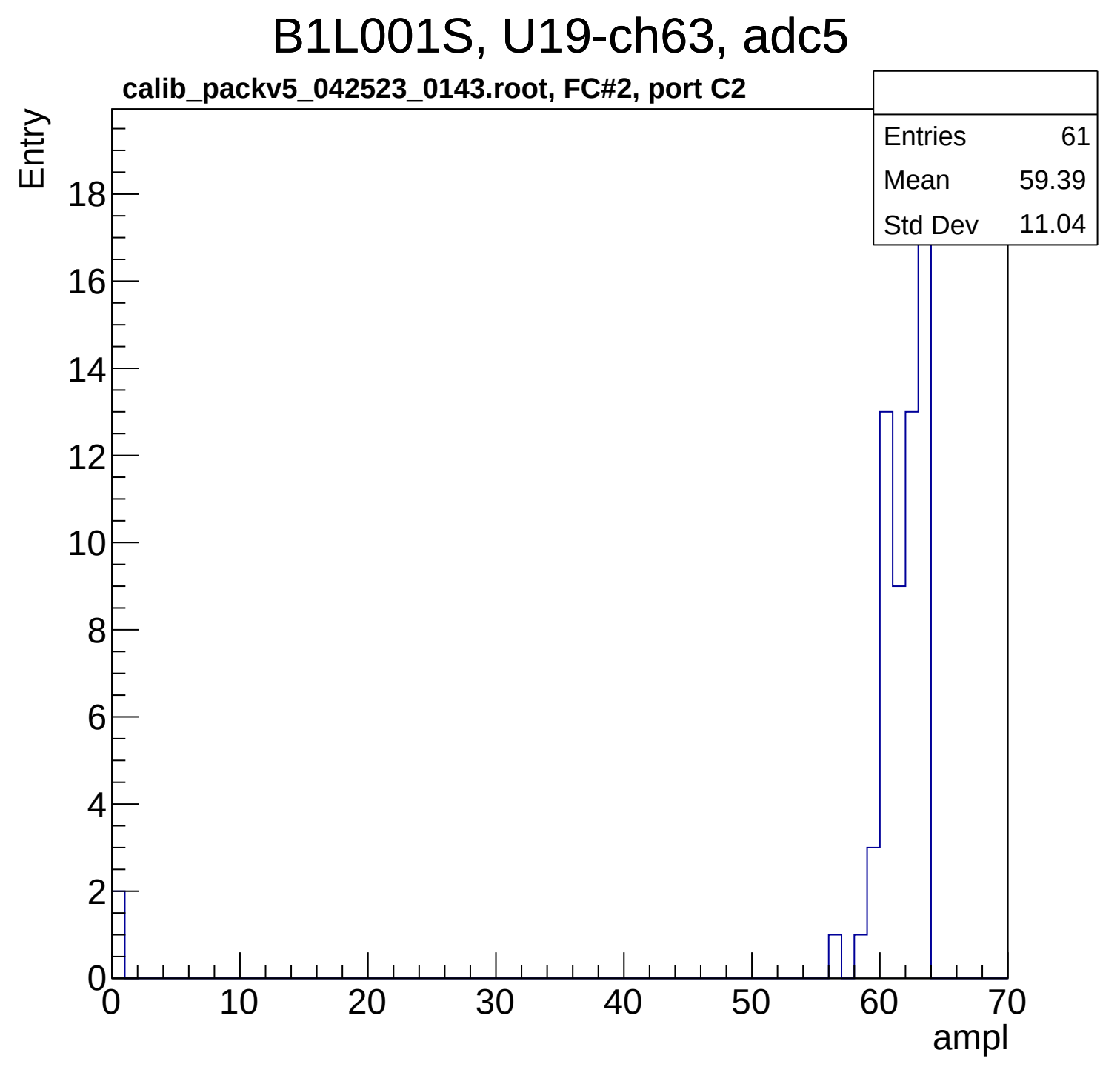
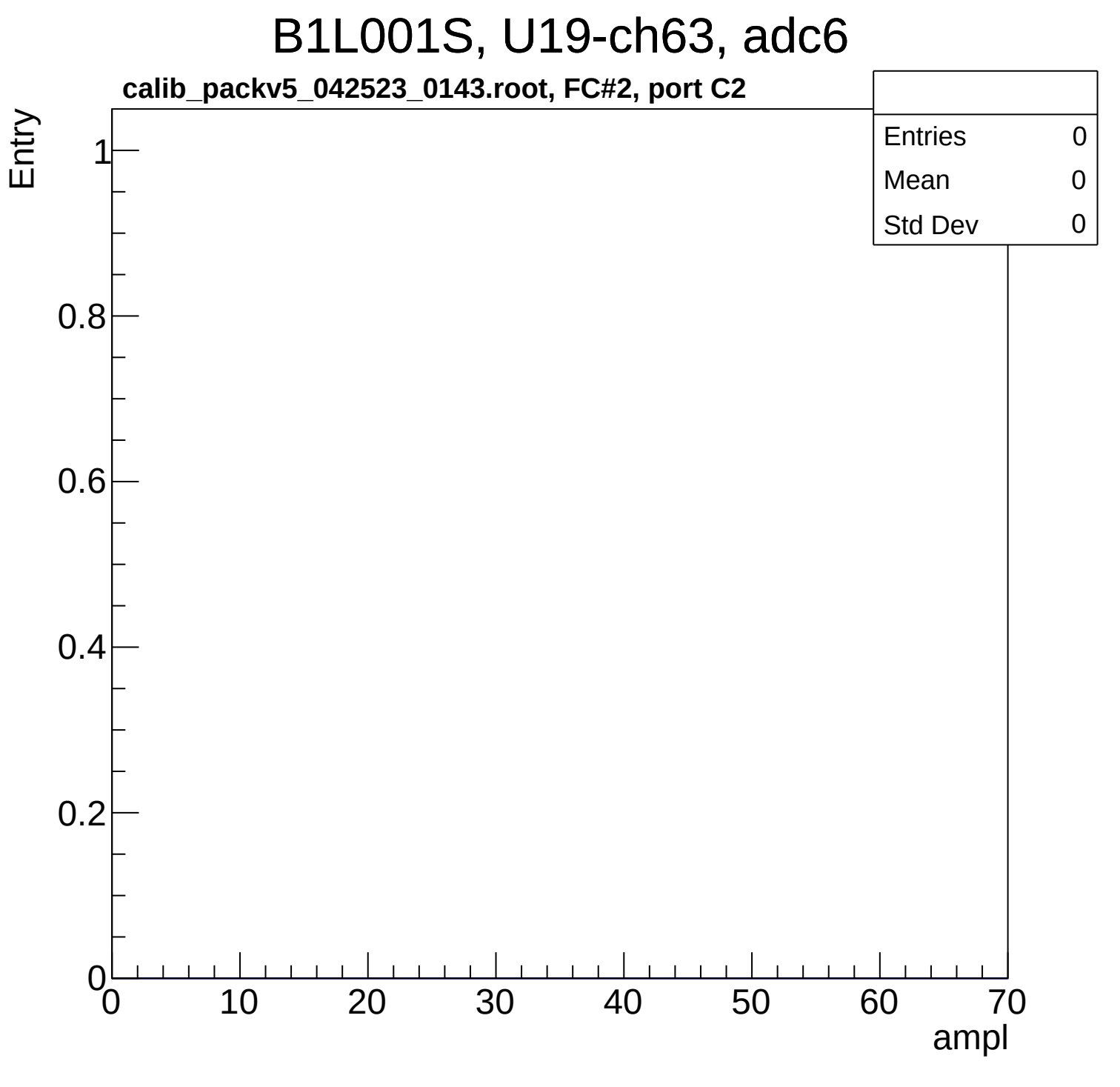
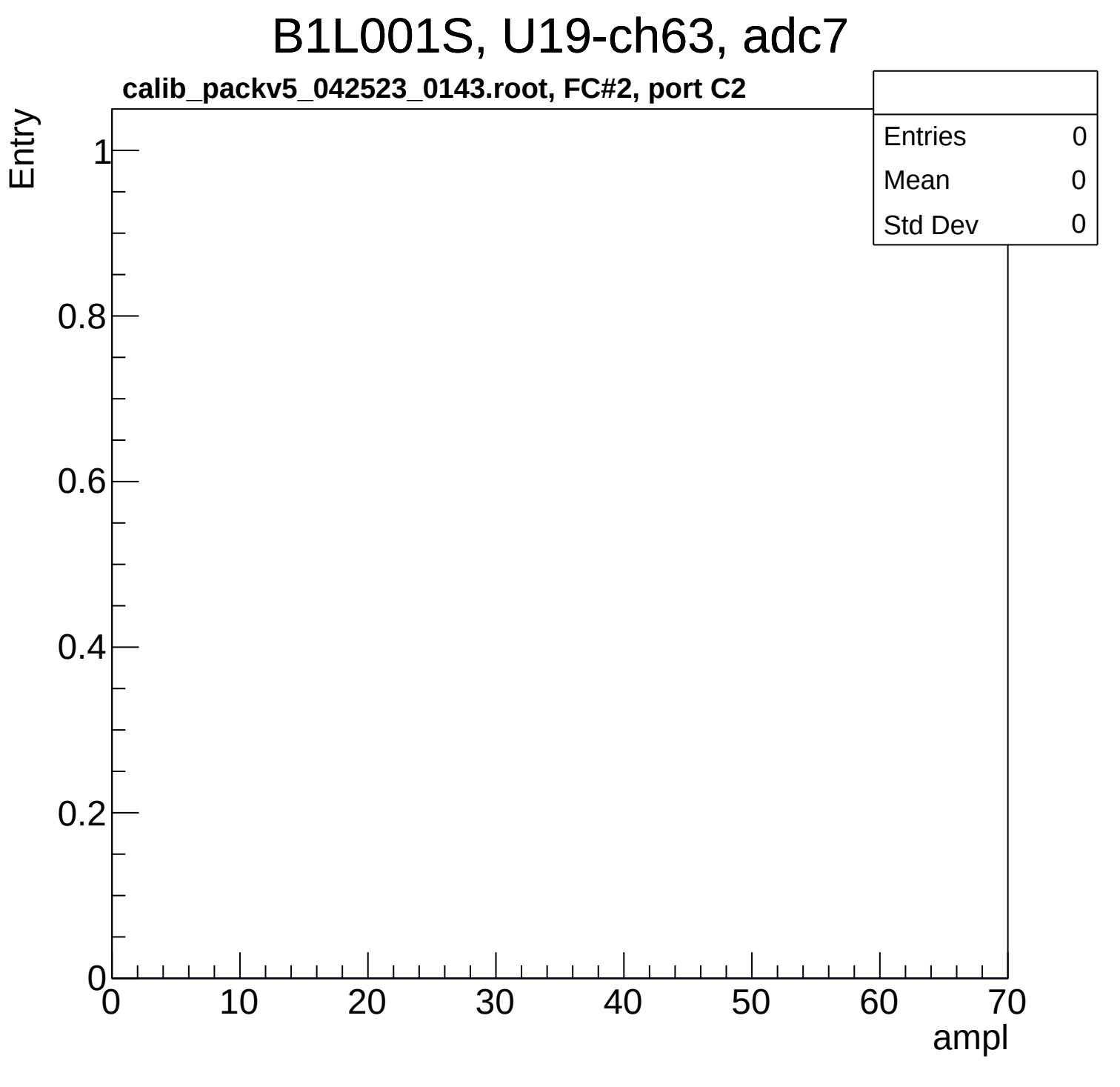

B1L001S, U19-ch63, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 61
Mean 59.39
Std Dev 11.04
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch63, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch63, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 0
Mean 0
Std Dev 0
Entry
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0.8
0.6
0.4
0.2
0
0
10
20
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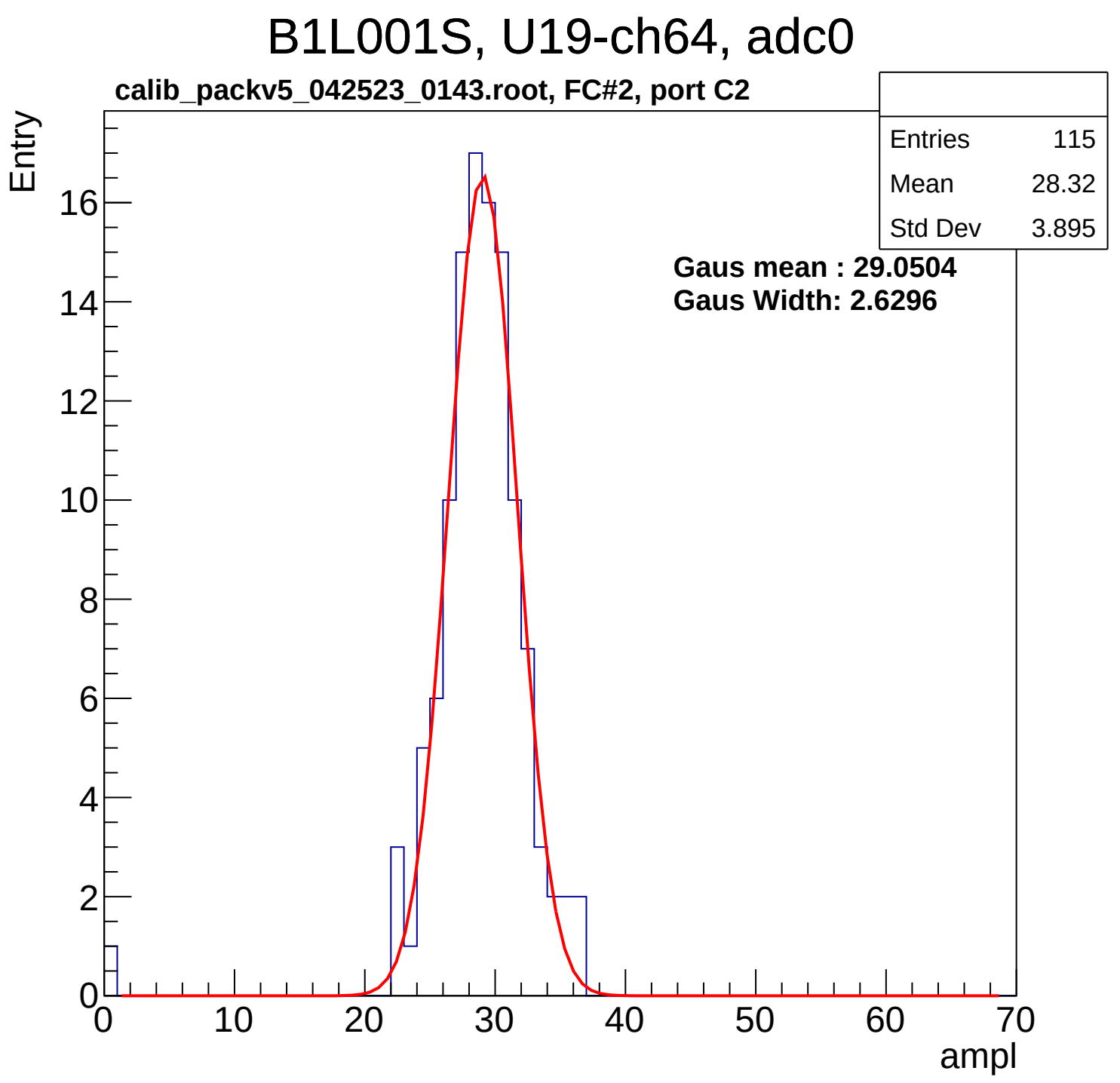
40
50
60
70
ampl


B1L001S, U19-ch64, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 115
Mean 28.32
Std Dev 3.895
Gaus mean : 29.0504
Gaus Width: 2.6296
Entry
ampl
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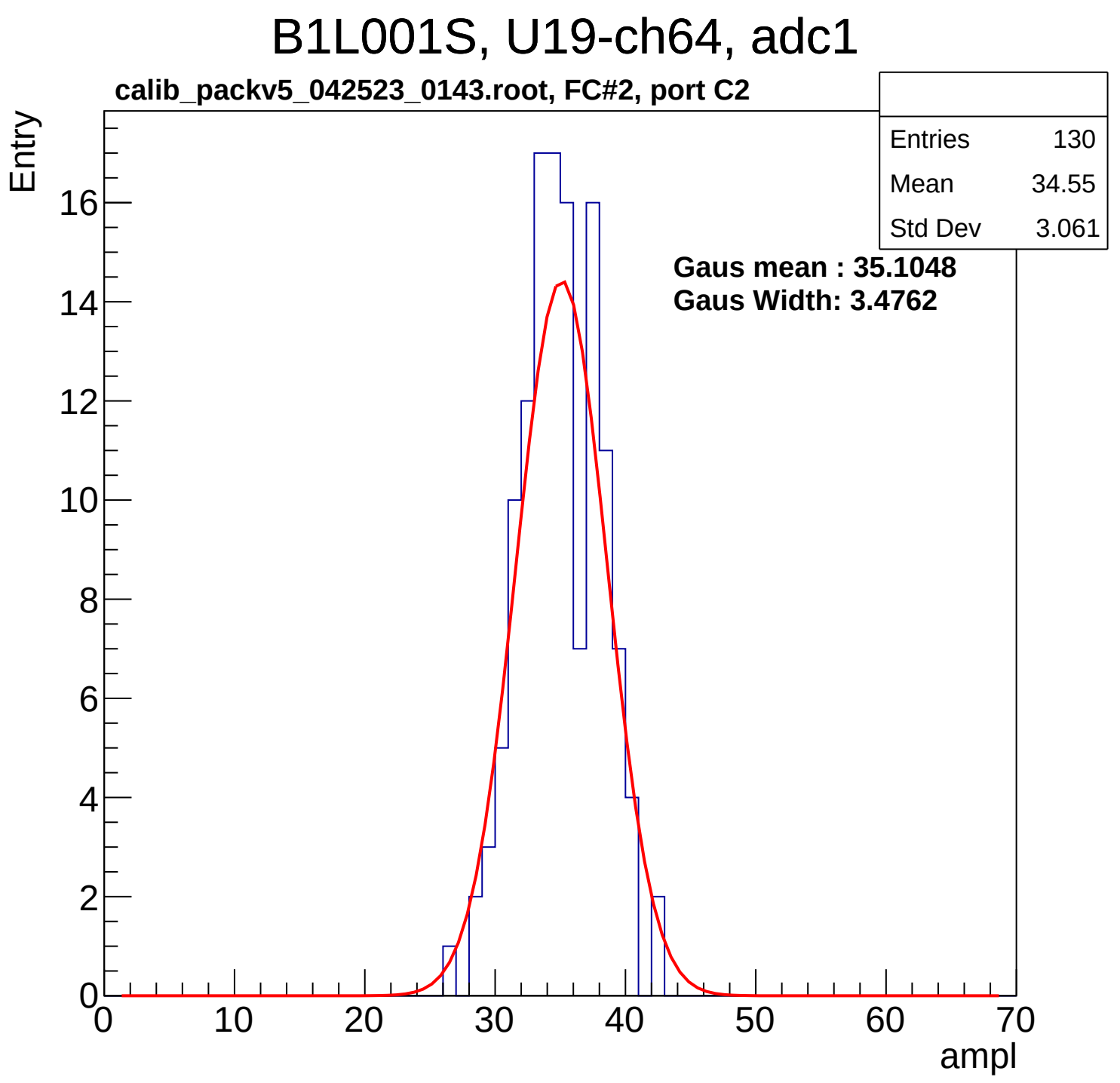
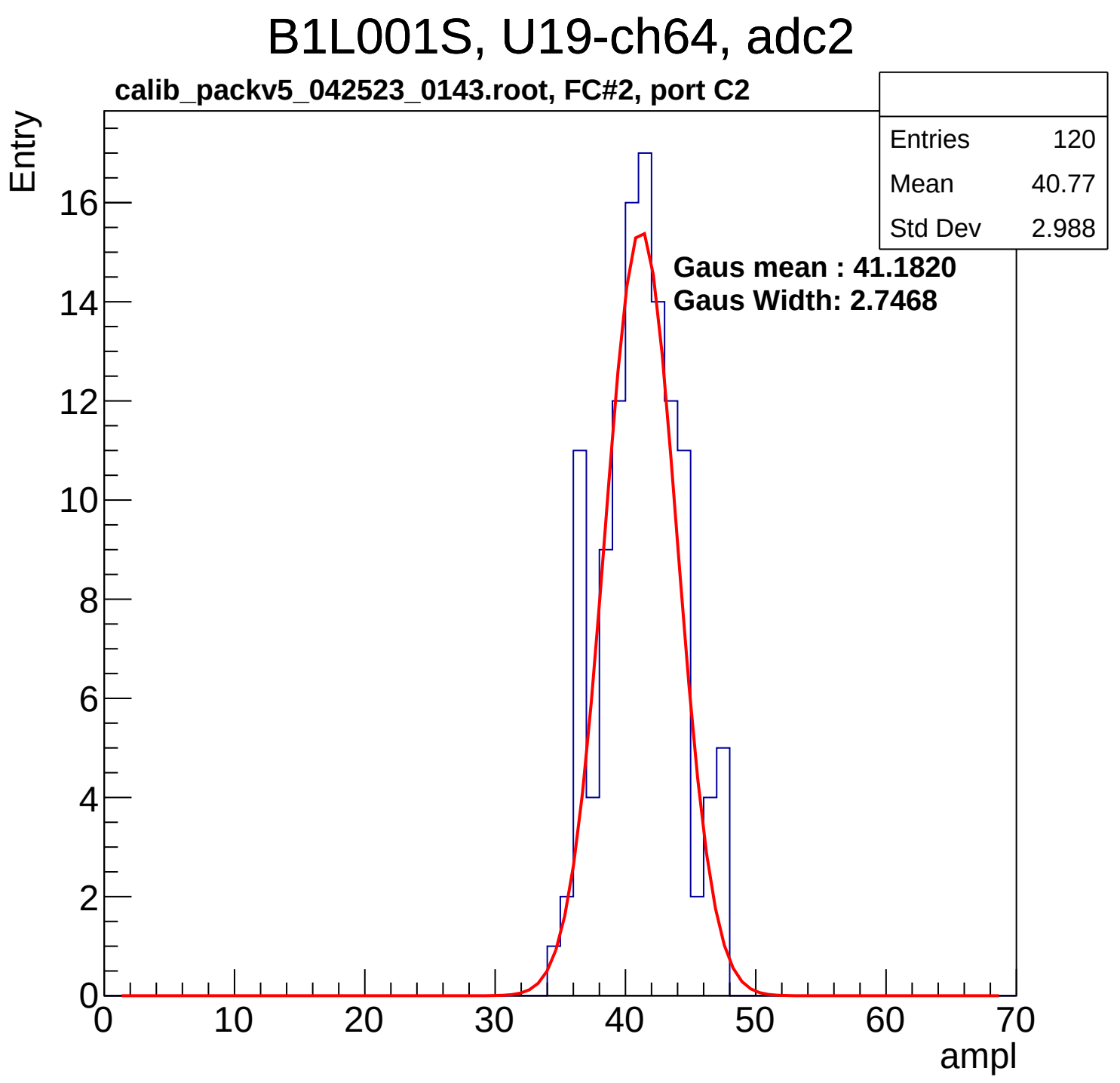
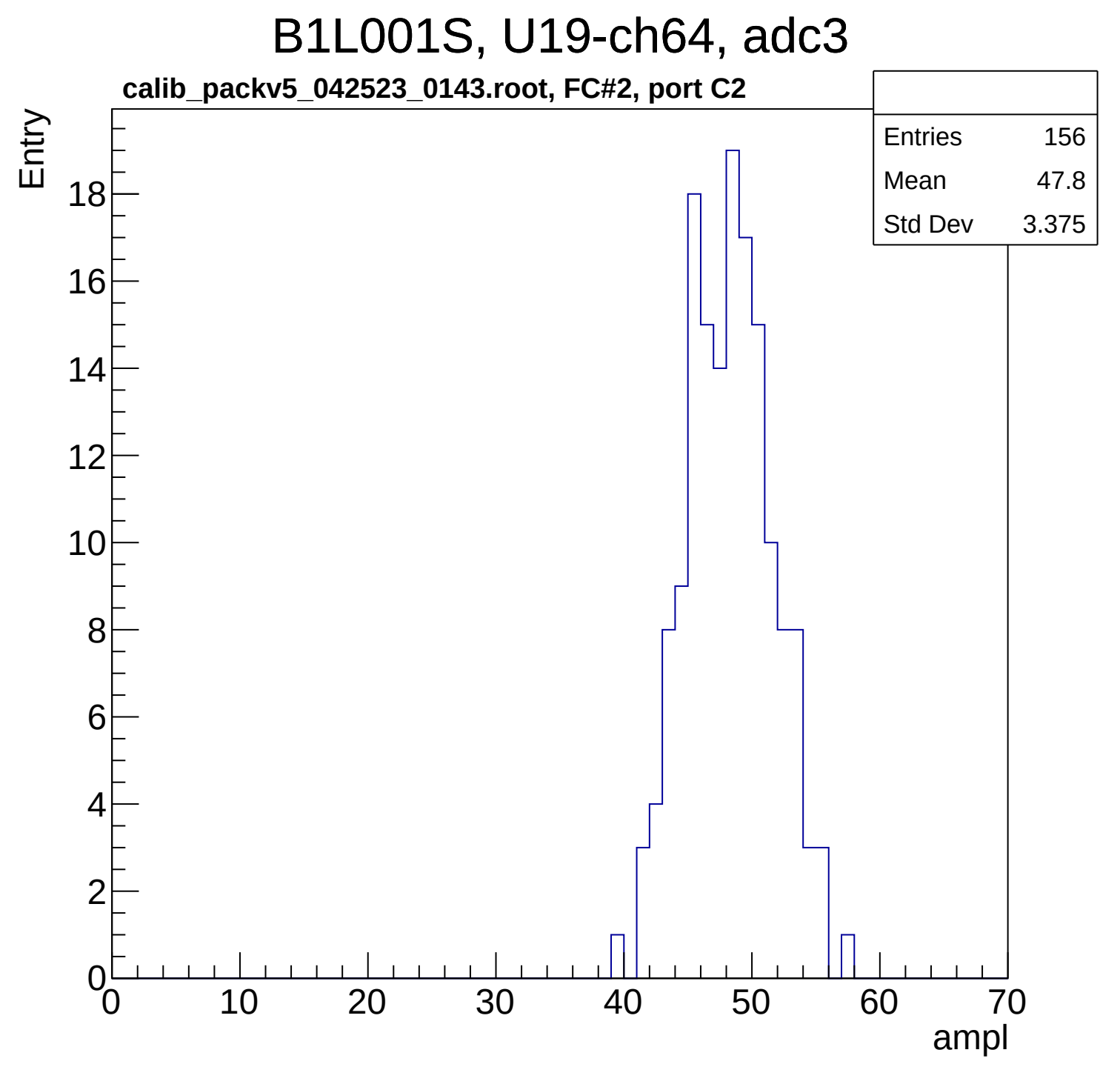
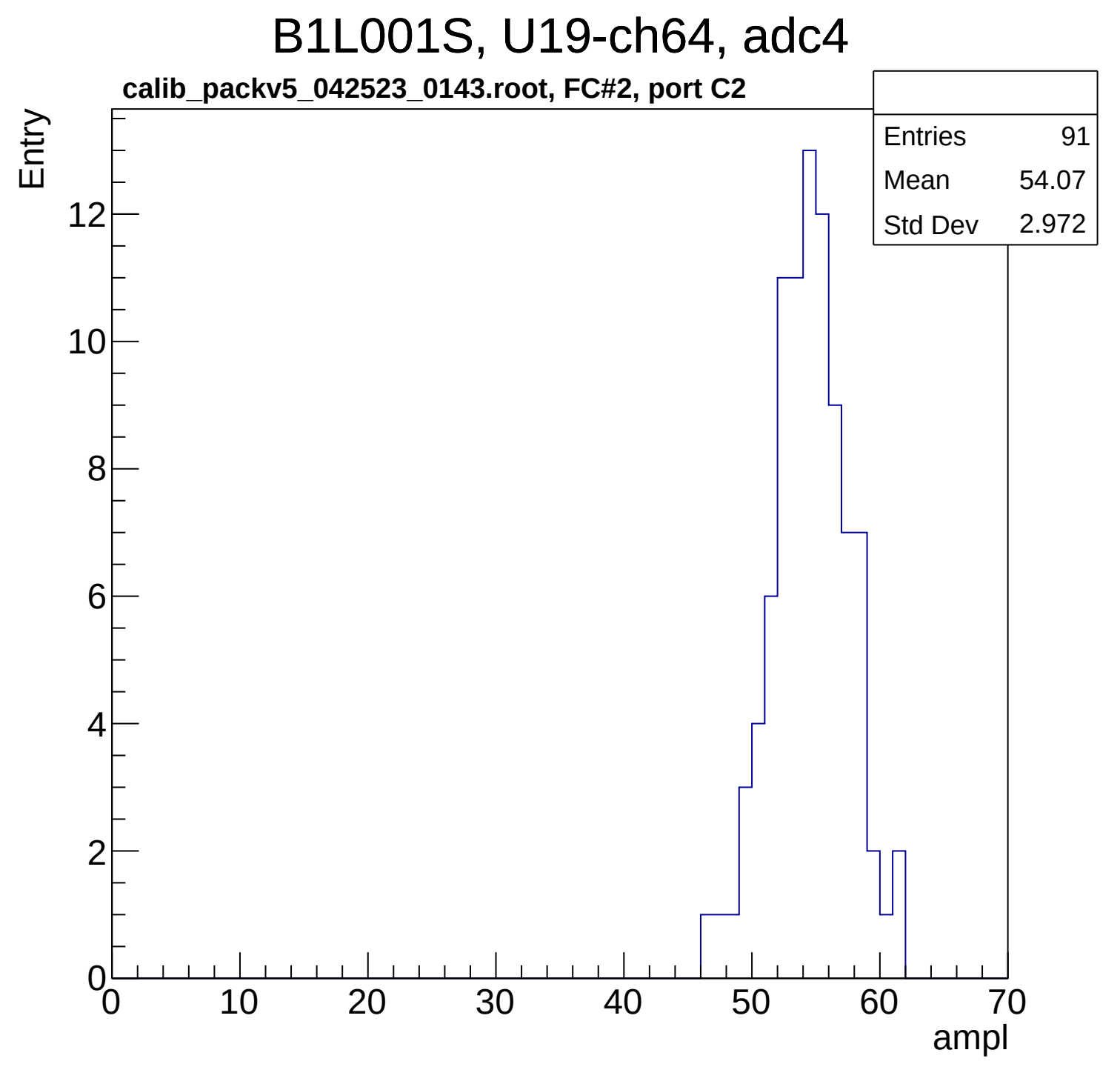
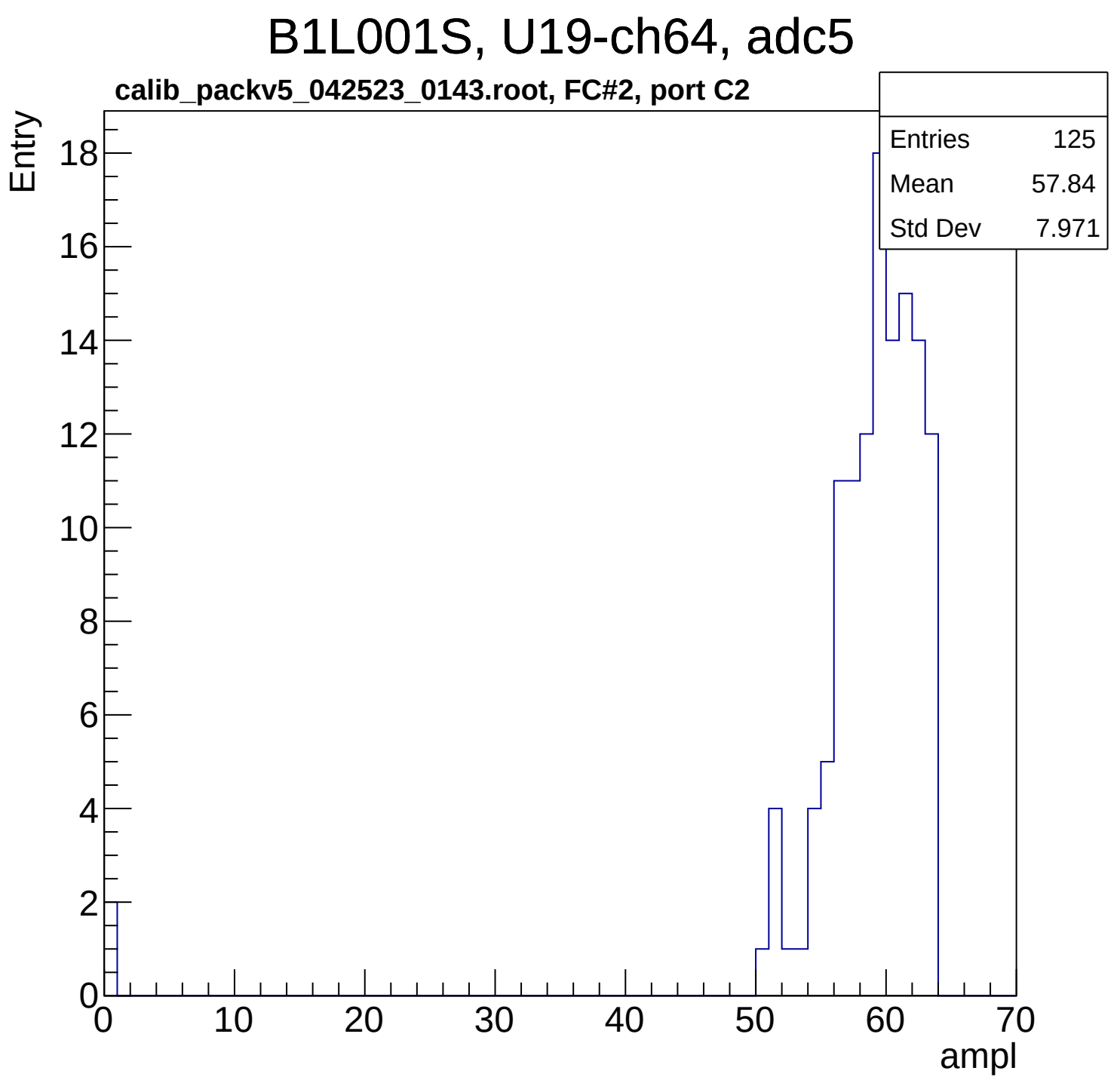
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

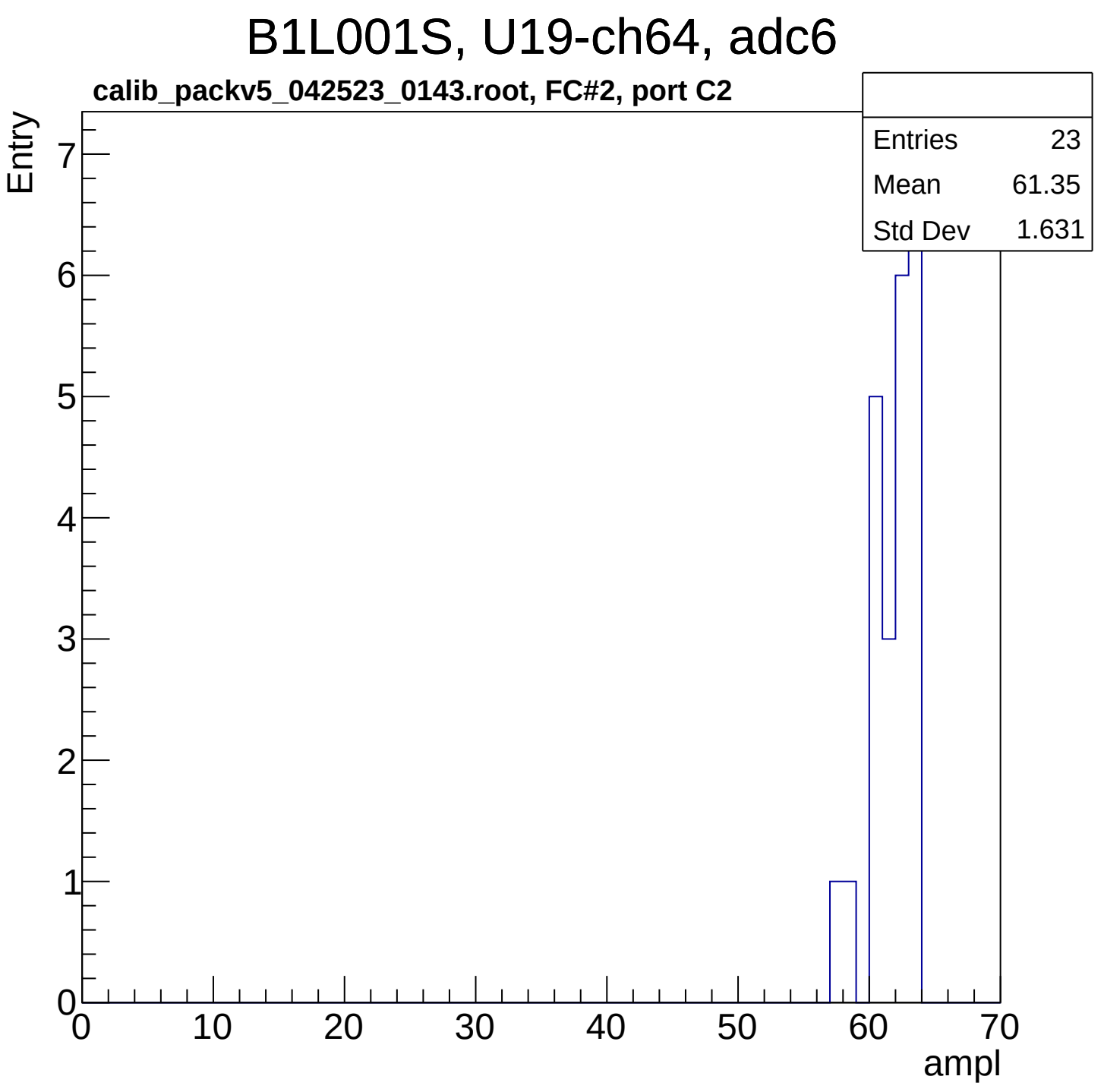

B1L001S, U19-ch64, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 130
Mean 34.55
Std Dev 3.061
Gaus mean : 35.1048
Gaus Width: 3.4762
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

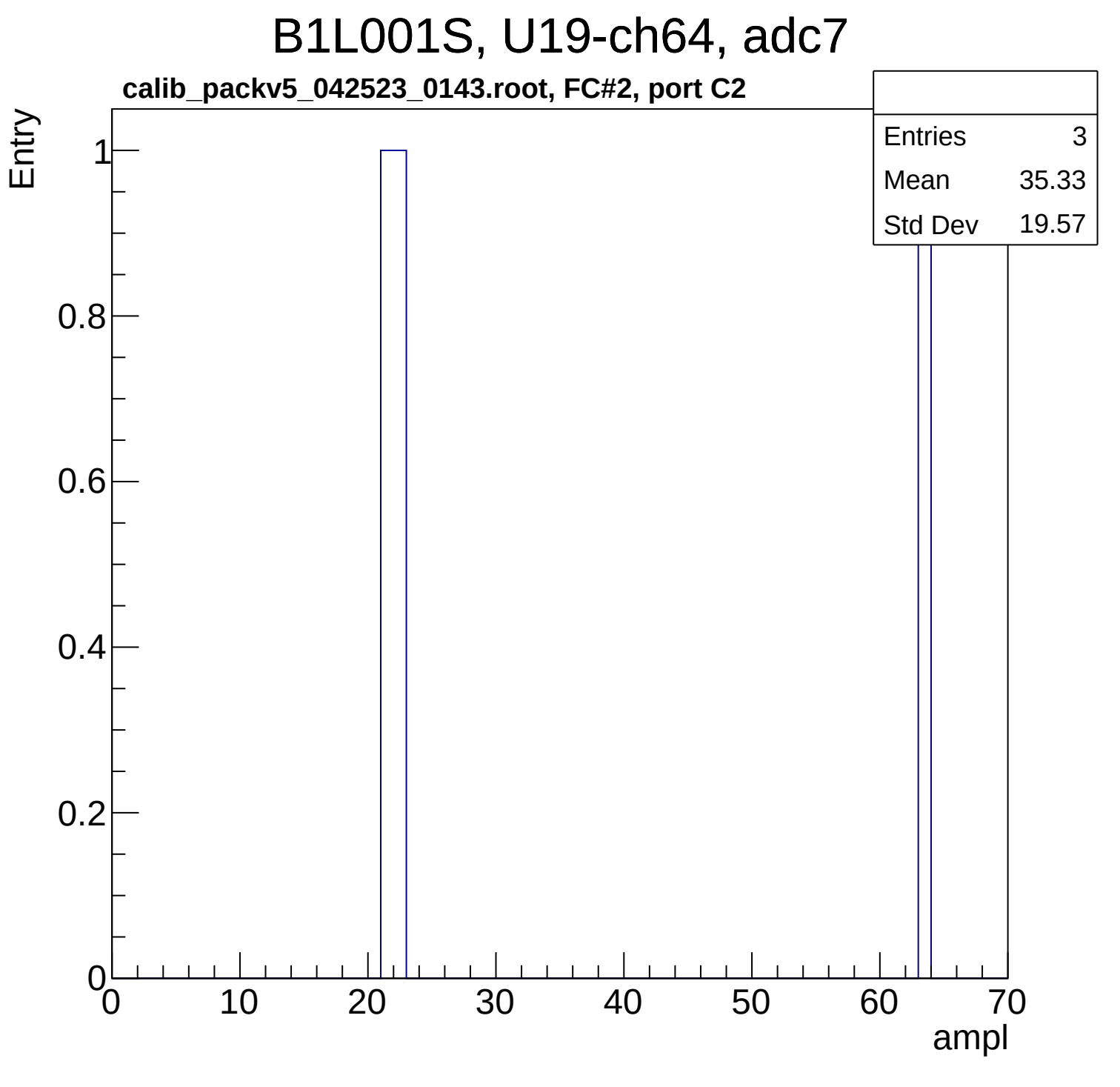

B1L001S, U19-ch64, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 120
Mean 40.77
Std Dev 2.988
Gaus mean : 41.1820
Gaus Width: 2.7468
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70


B1L001S, U19-ch64, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 156
Mean 47.8
Std Dev 3.375
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch64, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 91
Mean 54.07
Std Dev 2.972
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch64, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 125
Mean 57.84
Std Dev 7.971
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70


B1L001S, U19-ch64, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 23
Mean 61.35
Std Dev 1.631
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L001S, U19-ch64, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 3
Mean 35.33
Std Dev 19.57
Entry
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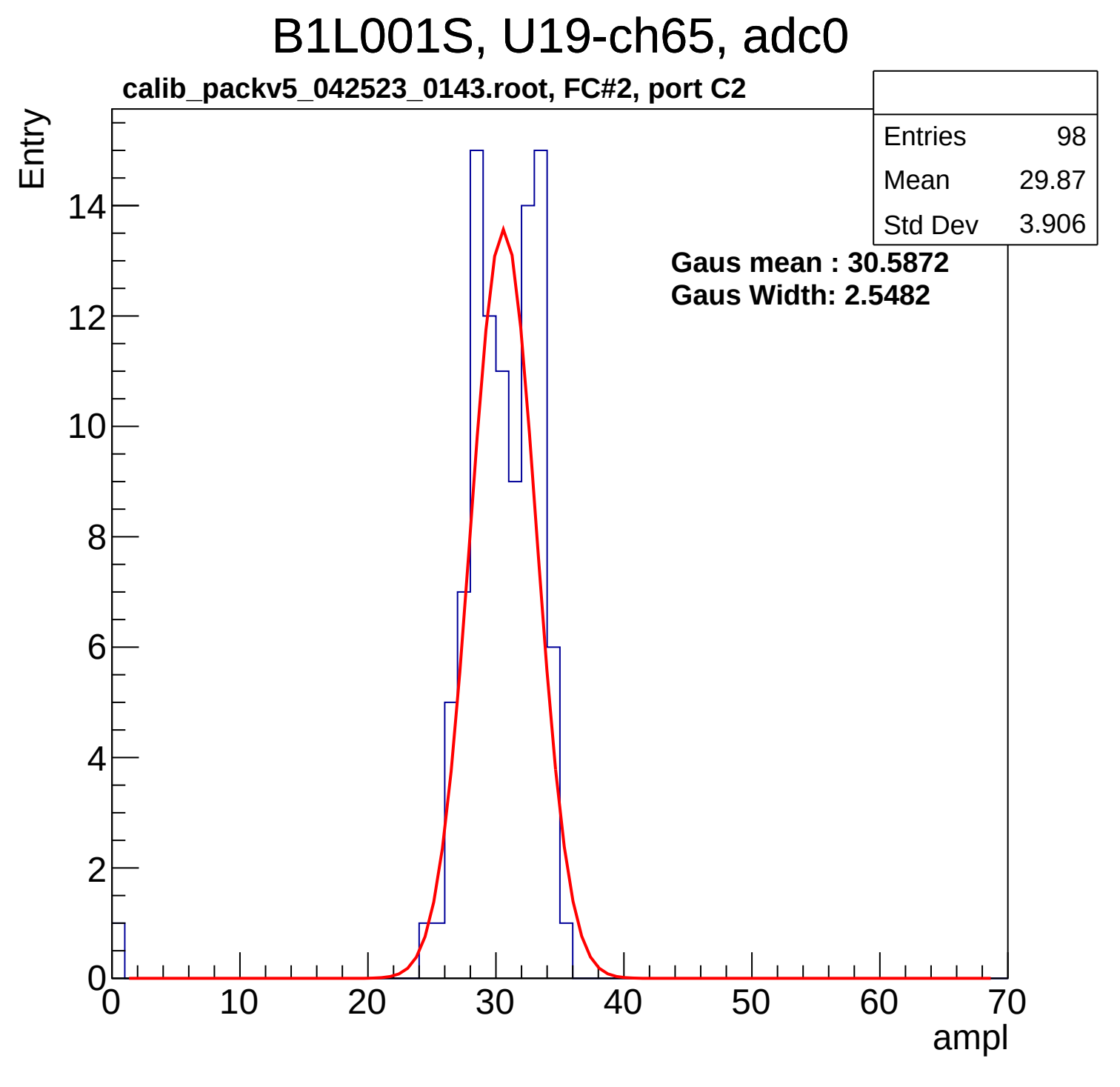
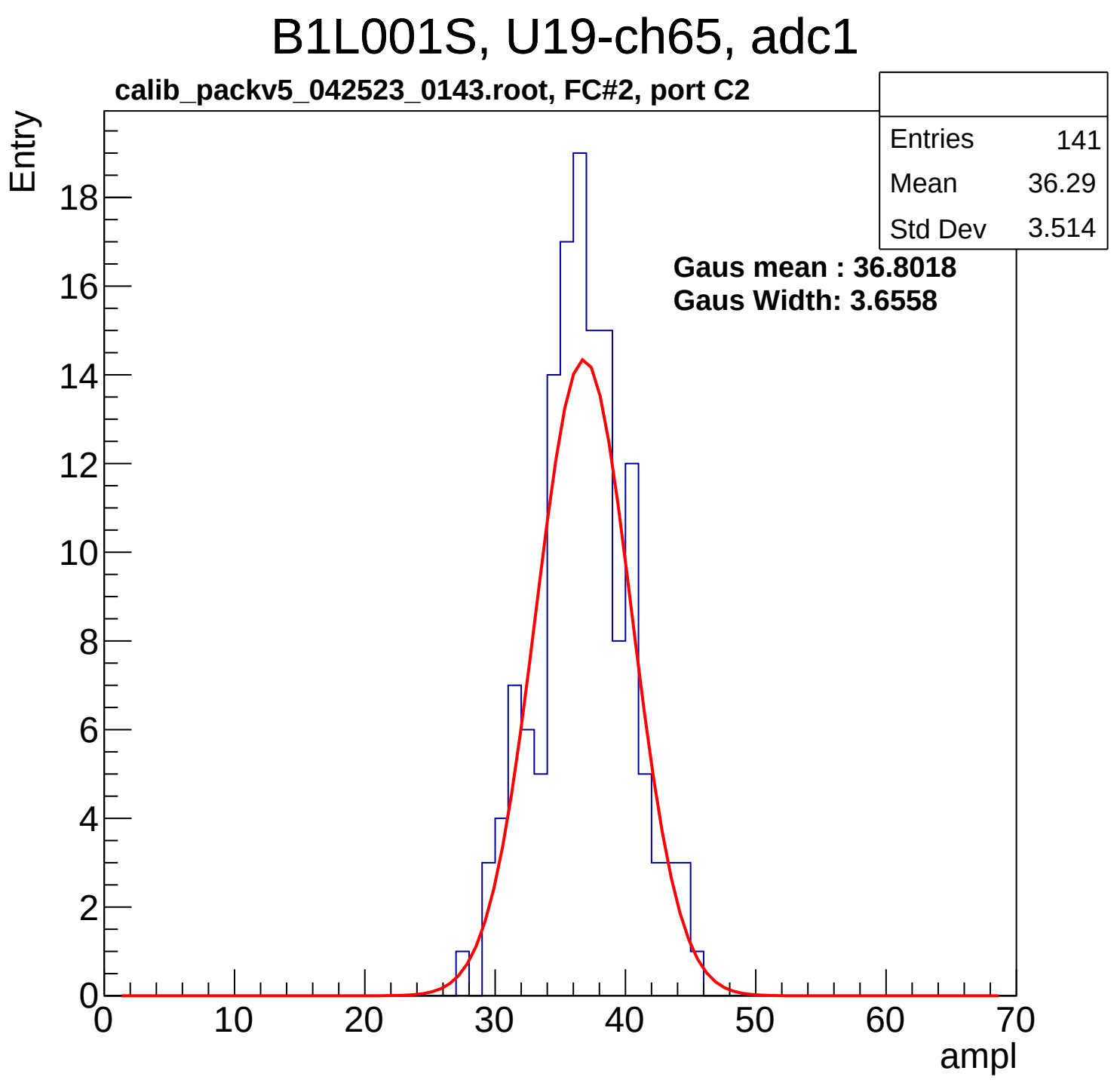
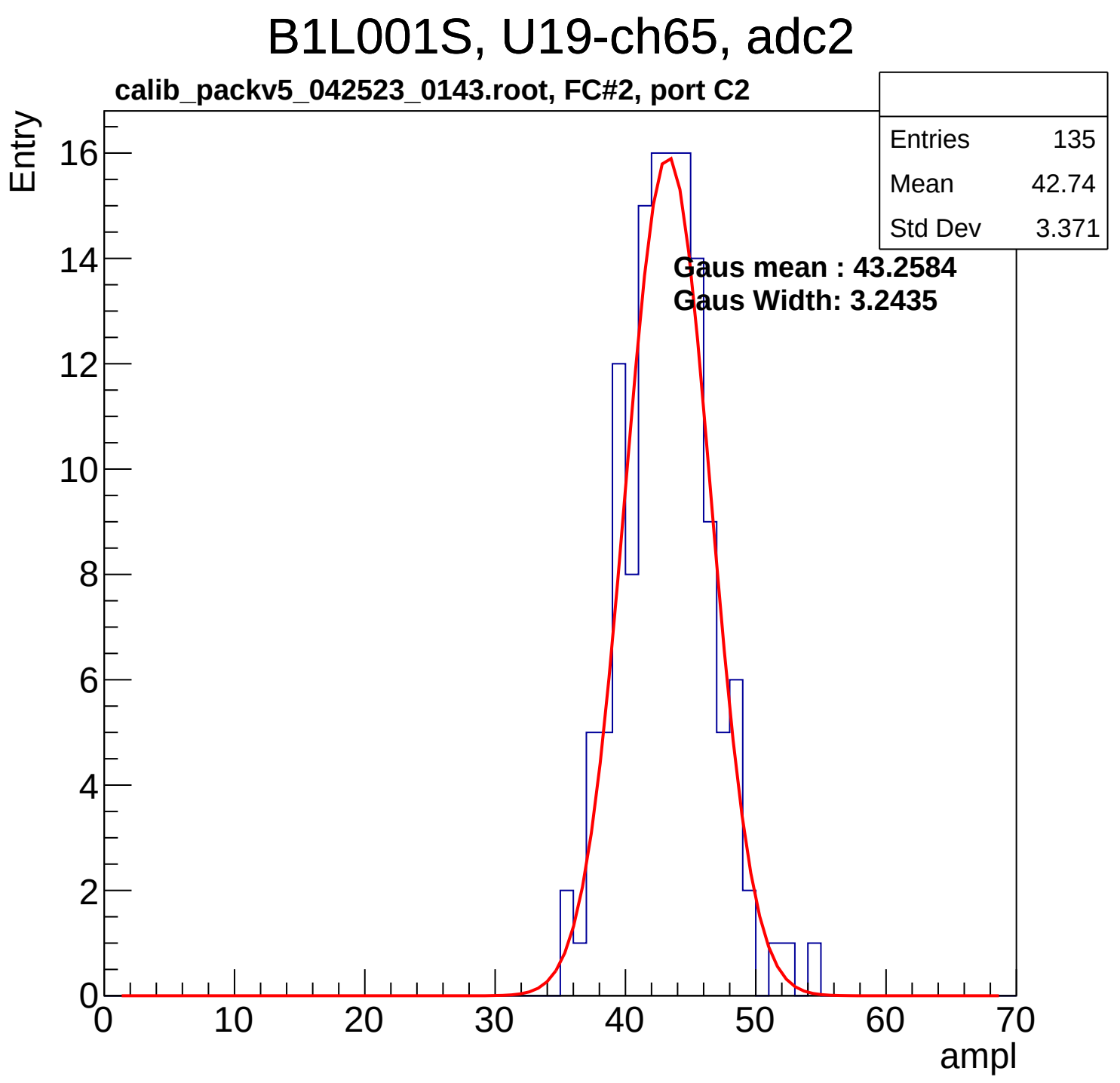
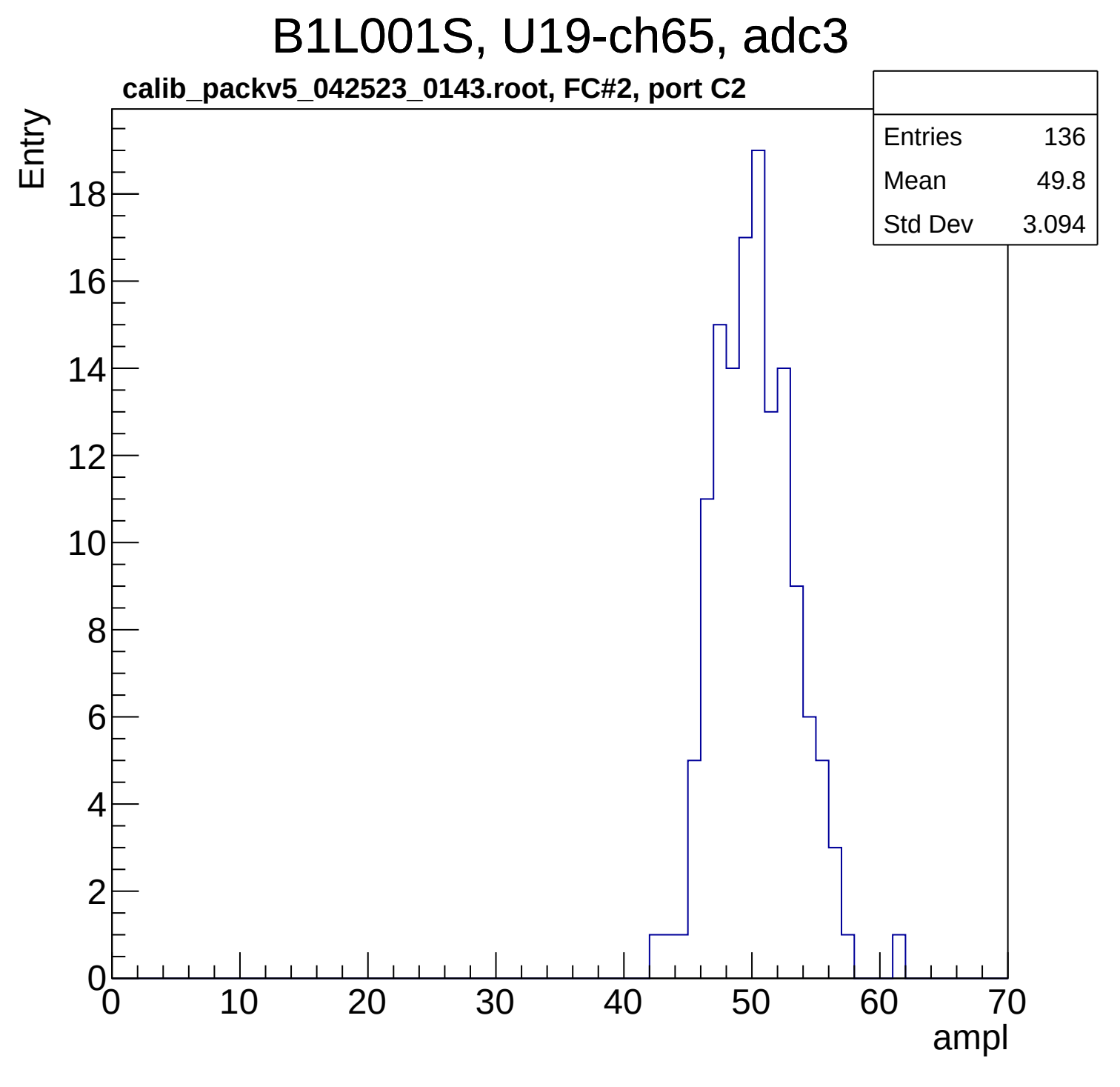
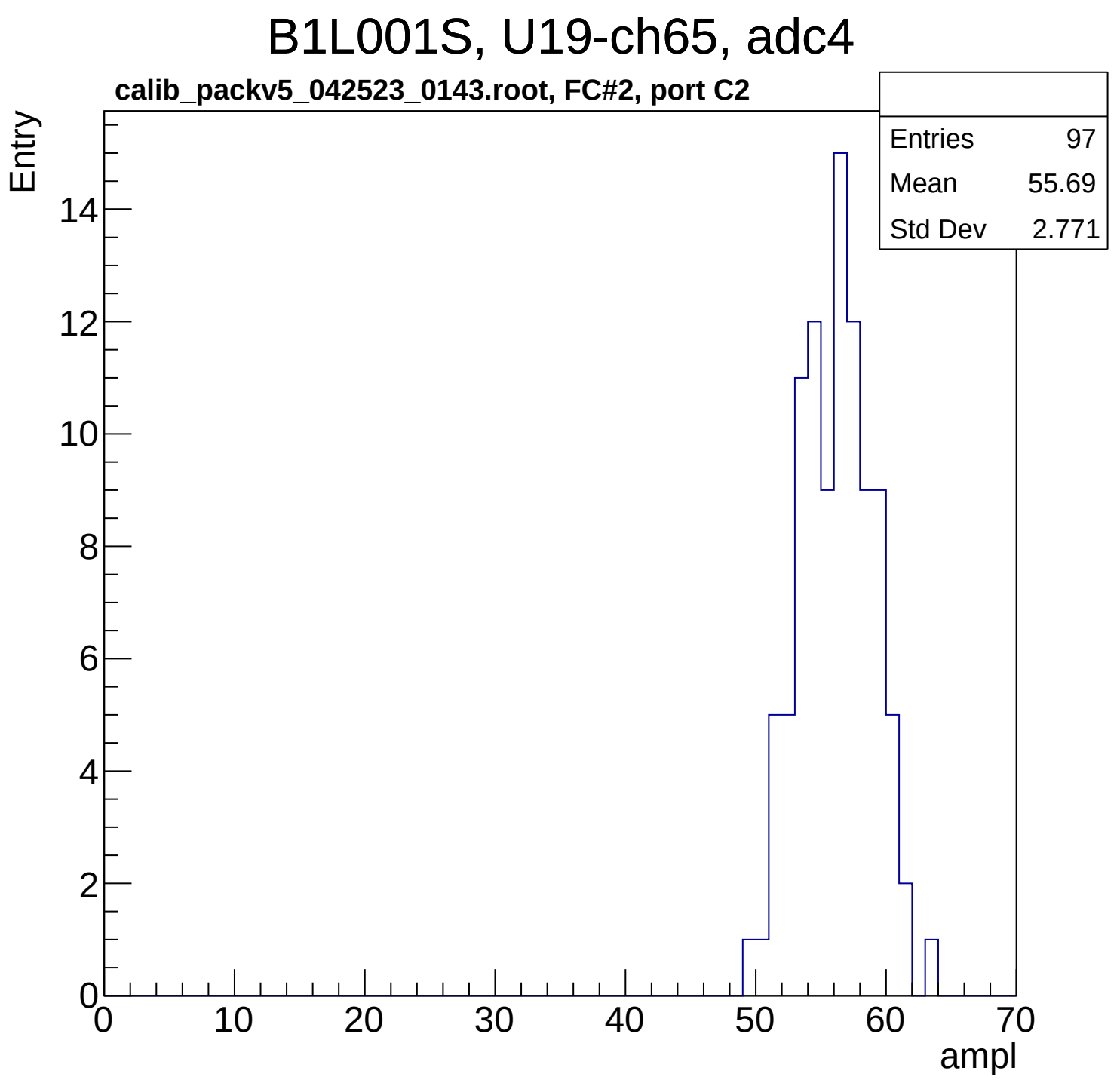
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

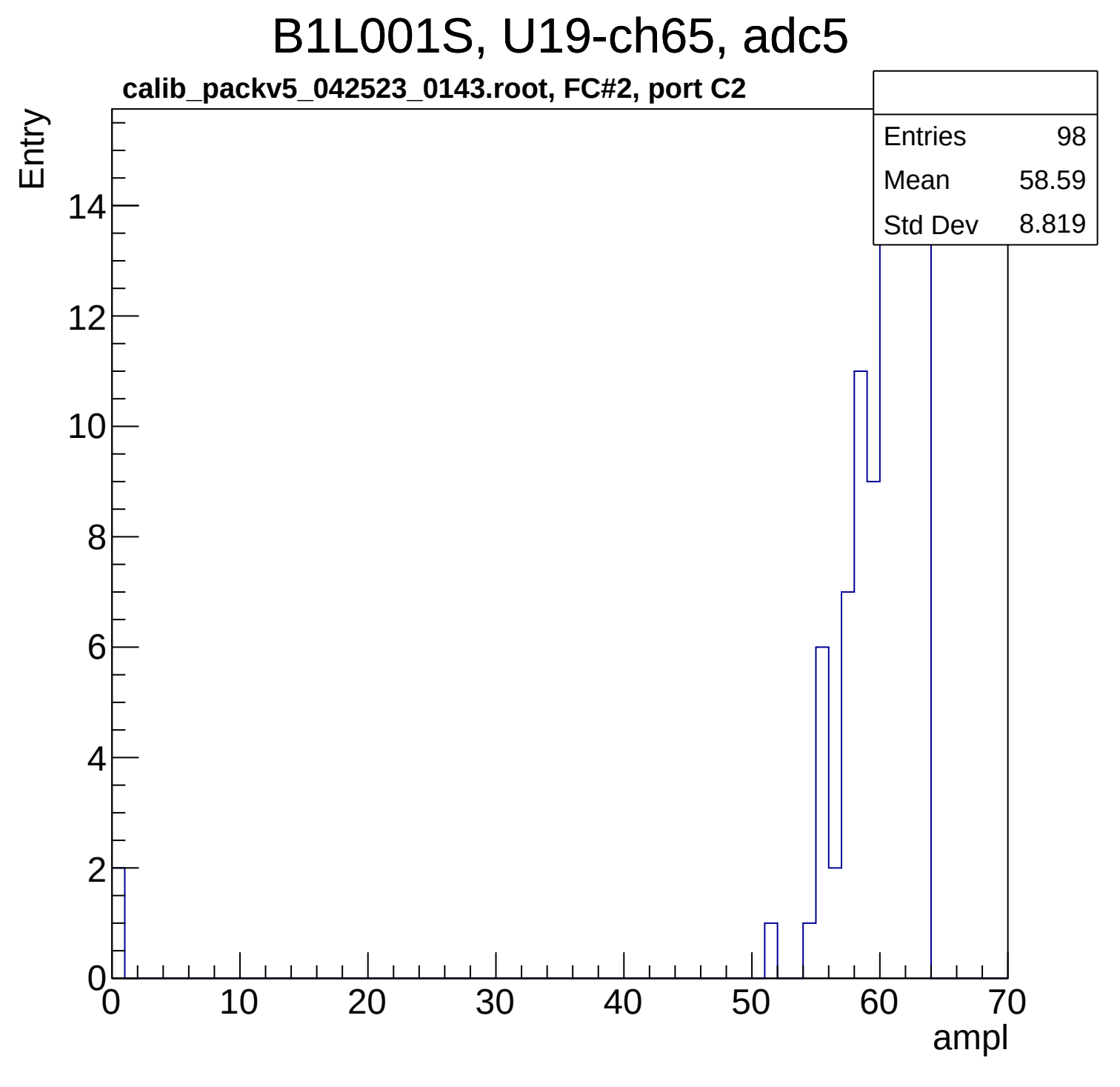

B1L001S, U19-ch65, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 98
Mean 29.87
Std Dev 3.906
Gaus mean : 30.5872
Gaus Width: 2.5482
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L001S, U19-ch65, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 141
Mean 36.29
Std Dev 3.514
Gaus mean : 36.8018
Gaus Width: 3.6558
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70


B1L001S, U19-ch65, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 135
Mean 42.74
Std Dev 3.371
Gaus mean : 43.2584
Gaus Width: 3.2435
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70


B1L001S, U19-ch65, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 136
Mean 49.8
Std Dev 3.094
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch65, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 97
Mean 55.69
Std Dev 2.771
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch65, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 98
Mean 58.59
Std Dev 8.819
Entry
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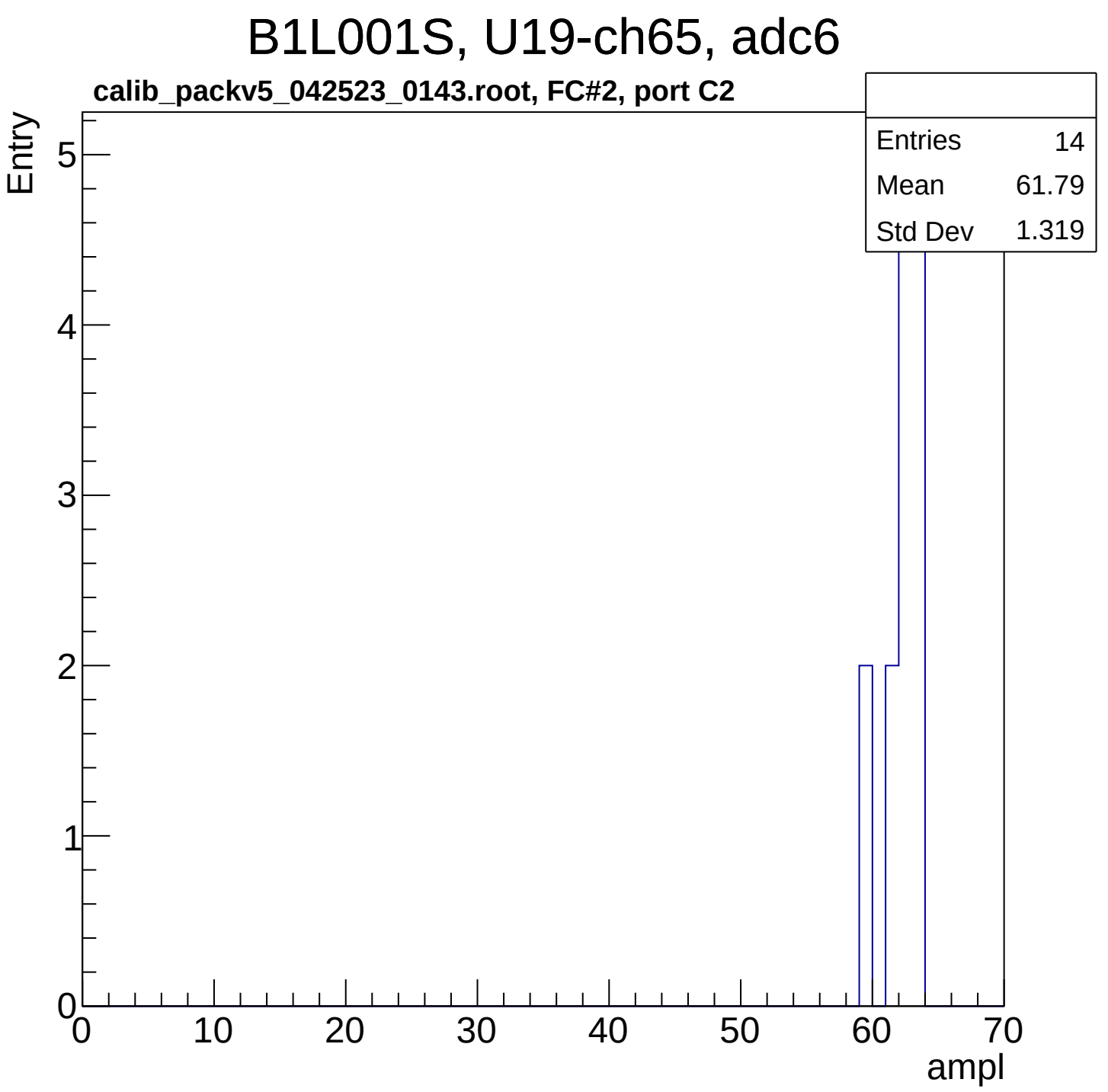
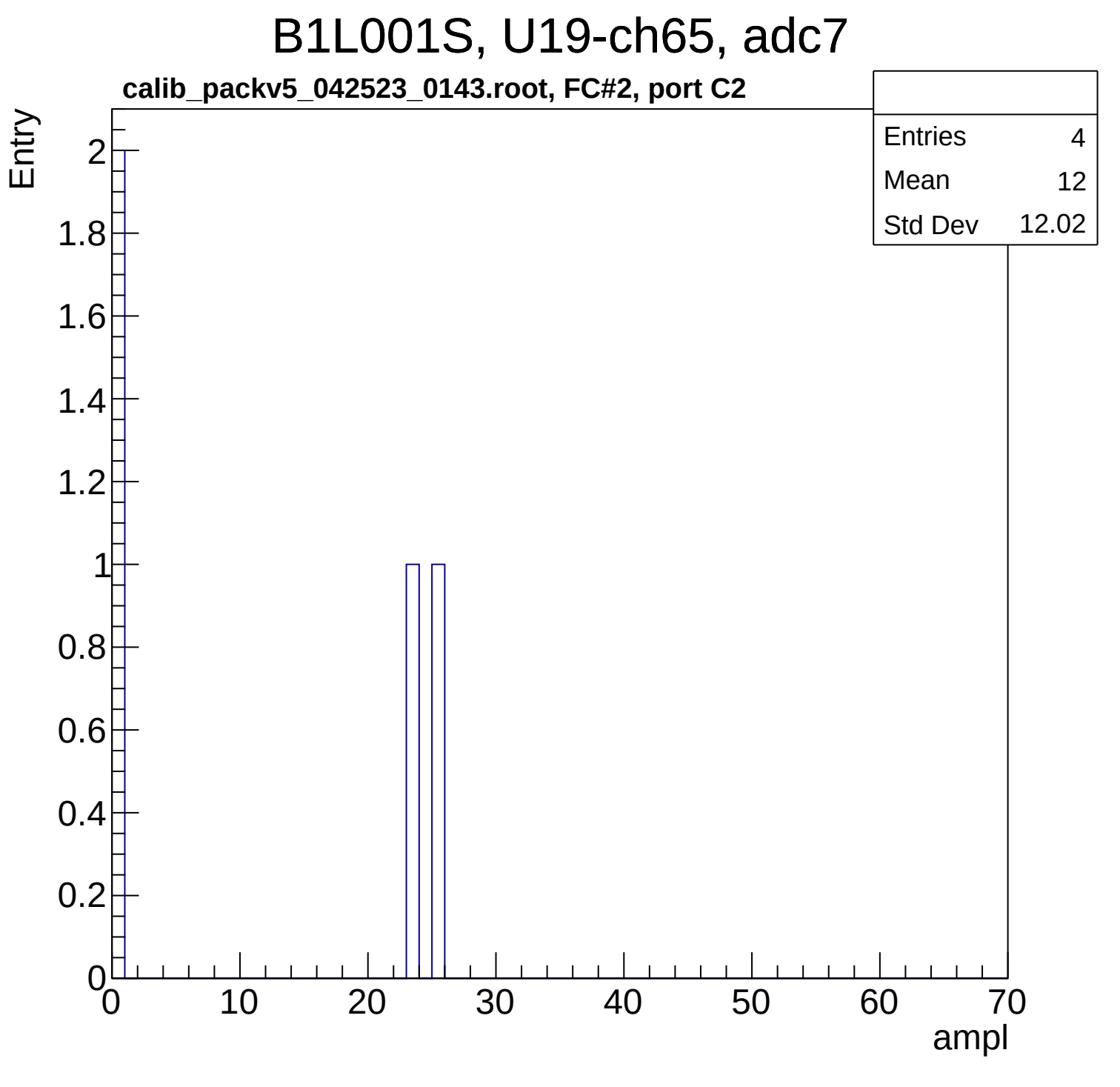
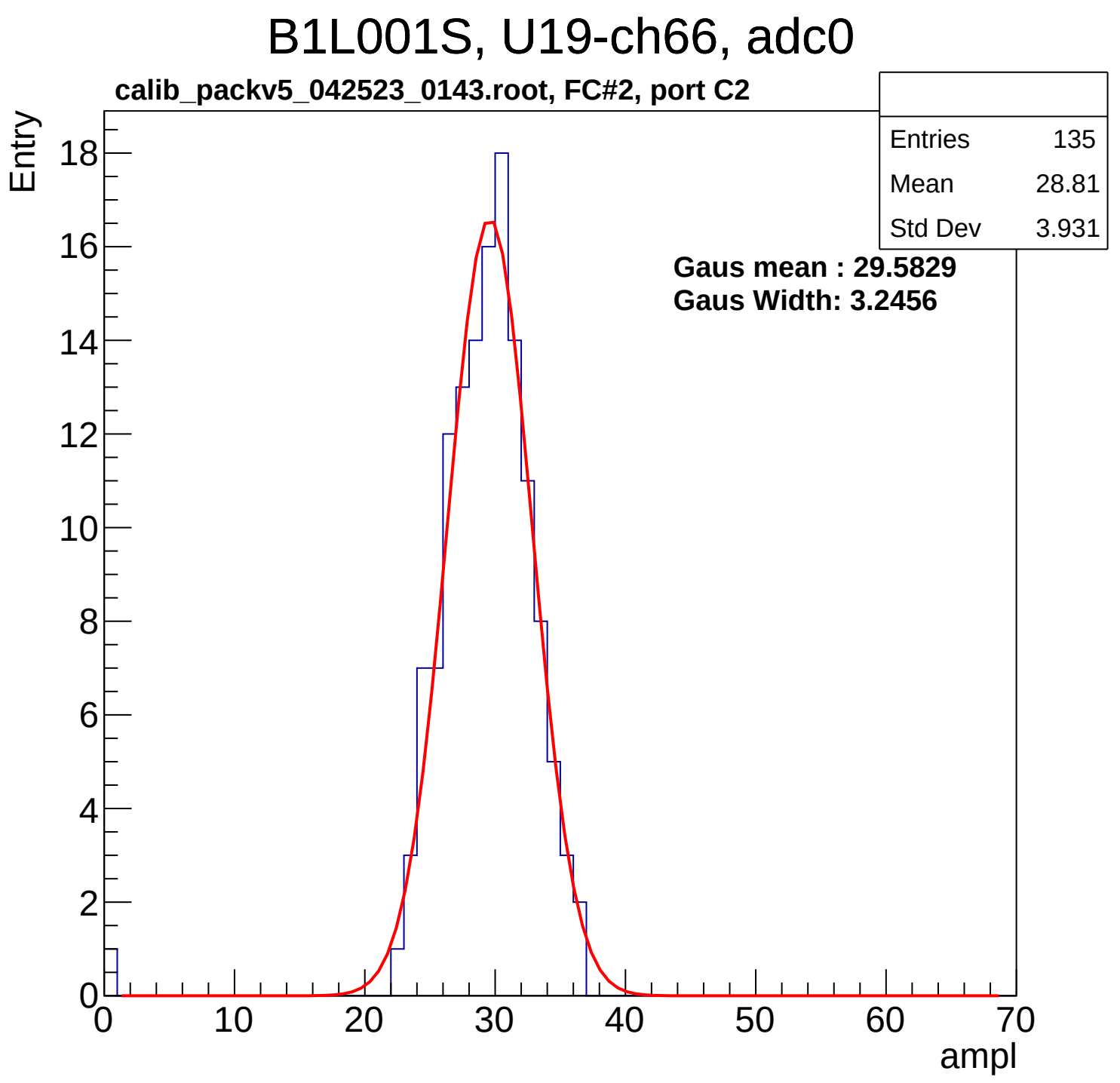
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch65, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 14
Mean 61.79
Std Dev 1.319
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch65, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 4
Mean 12
Std Dev 12.02
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L001S, U19-ch66, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 135
Mean 28.81
Std Dev 3.931
Gaus mean : 29.5829
Gaus Width: 3.2456
Entry
ampl
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2
4
6
8
10
12
14
16
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0
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20
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40
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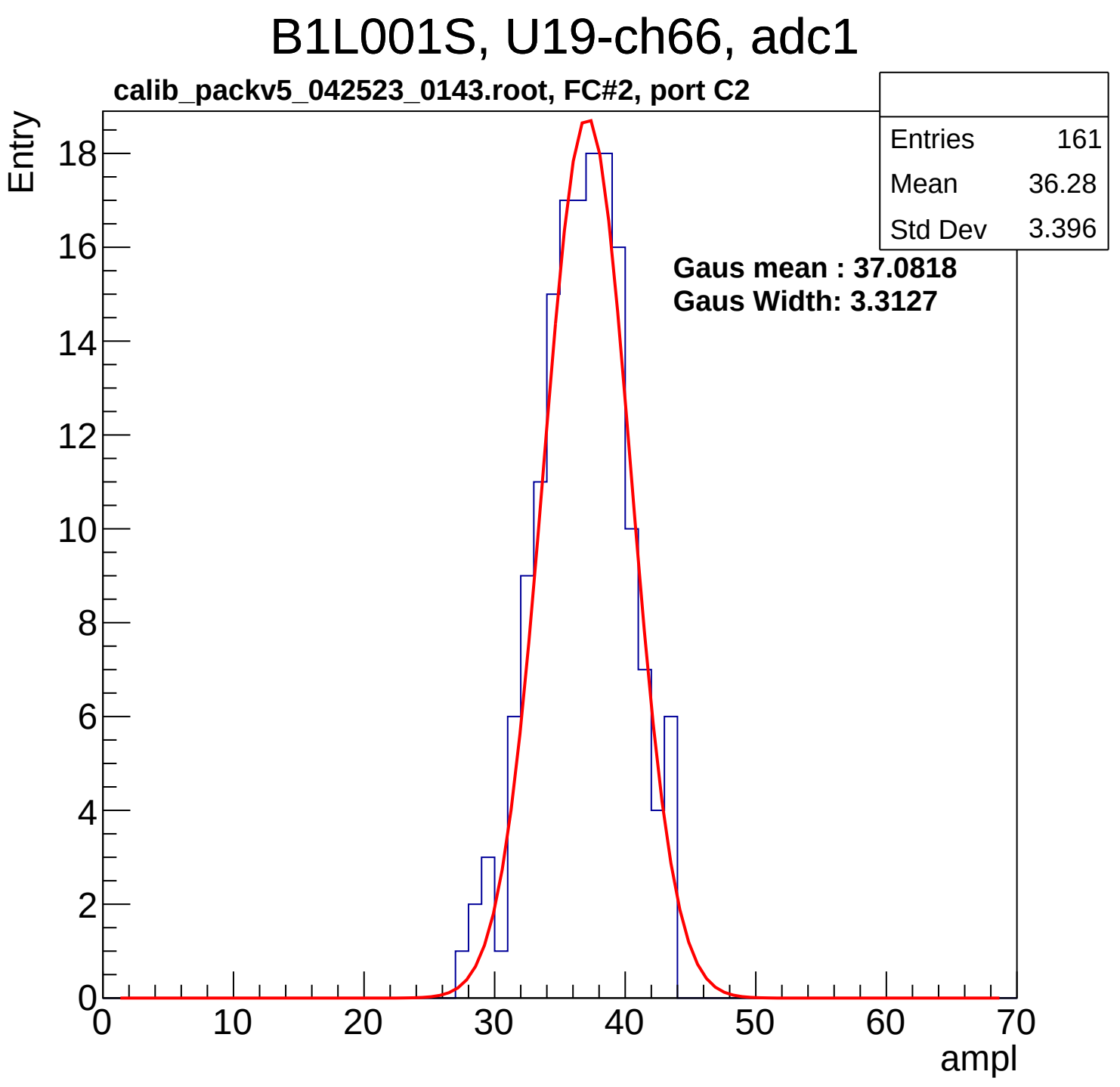
60
70


B1L001S, U19-ch66, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 161
Mean 36.28
Std Dev 3.396
Gaus mean : 37.0818
Gaus Width: 3.3127
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
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60
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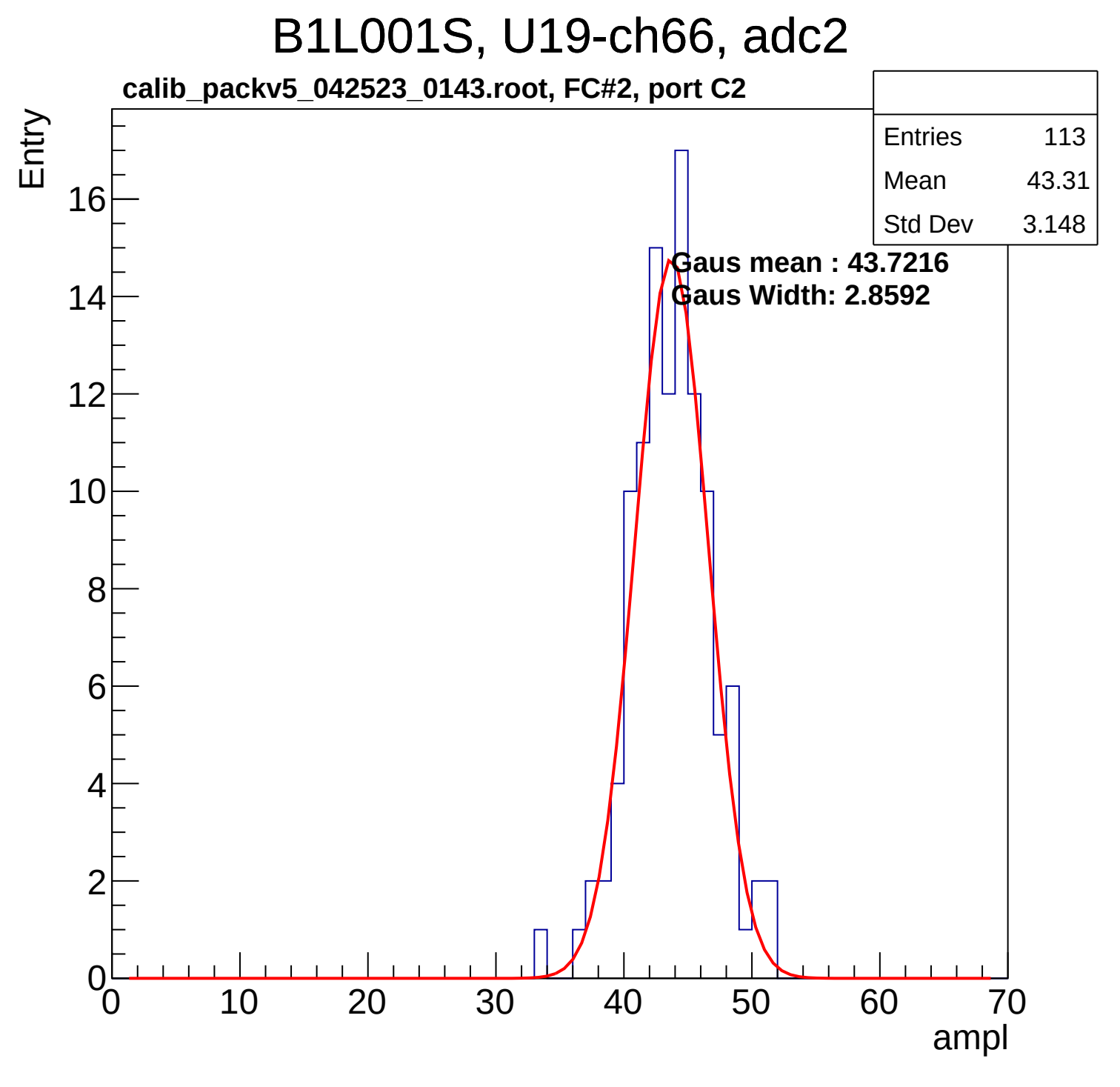
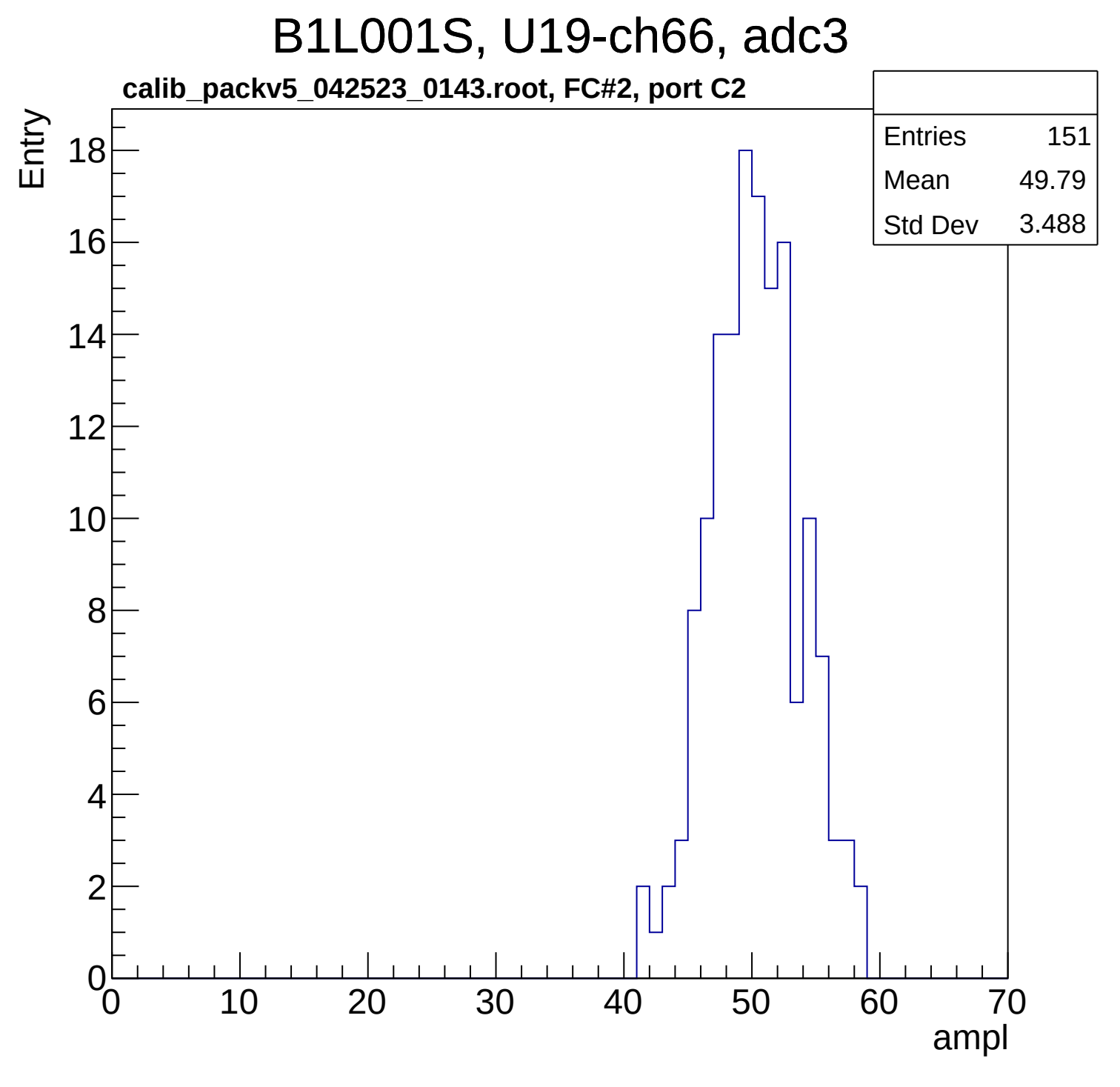

B1L001S, U19-ch66, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 113
Mean 43.31
Std Dev 3.148
Gaus mean : 43.7216
Gaus Width: 2.8592
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70


B1L001S, U19-ch66, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 151
Mean 49.79
Std Dev 3.488
Entry
0
2
4
6
8
10
12
14
16
18
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10
20
30
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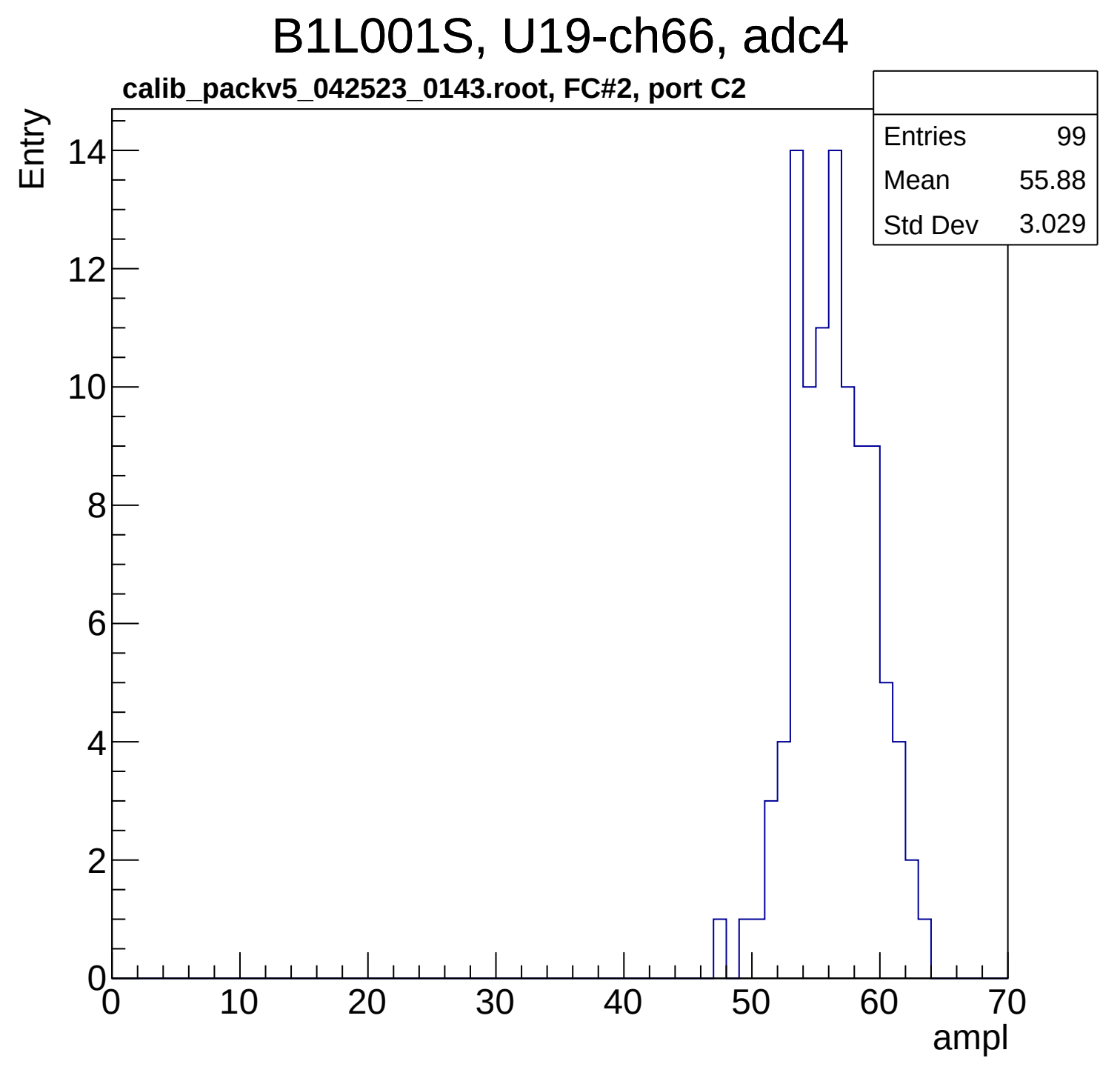
50
60
70
ampl


B1L001S, U19-ch66, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 99
Mean 55.88
Std Dev 3.029
Entry
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2
4
6
8
10
12
14
0
10
20
30
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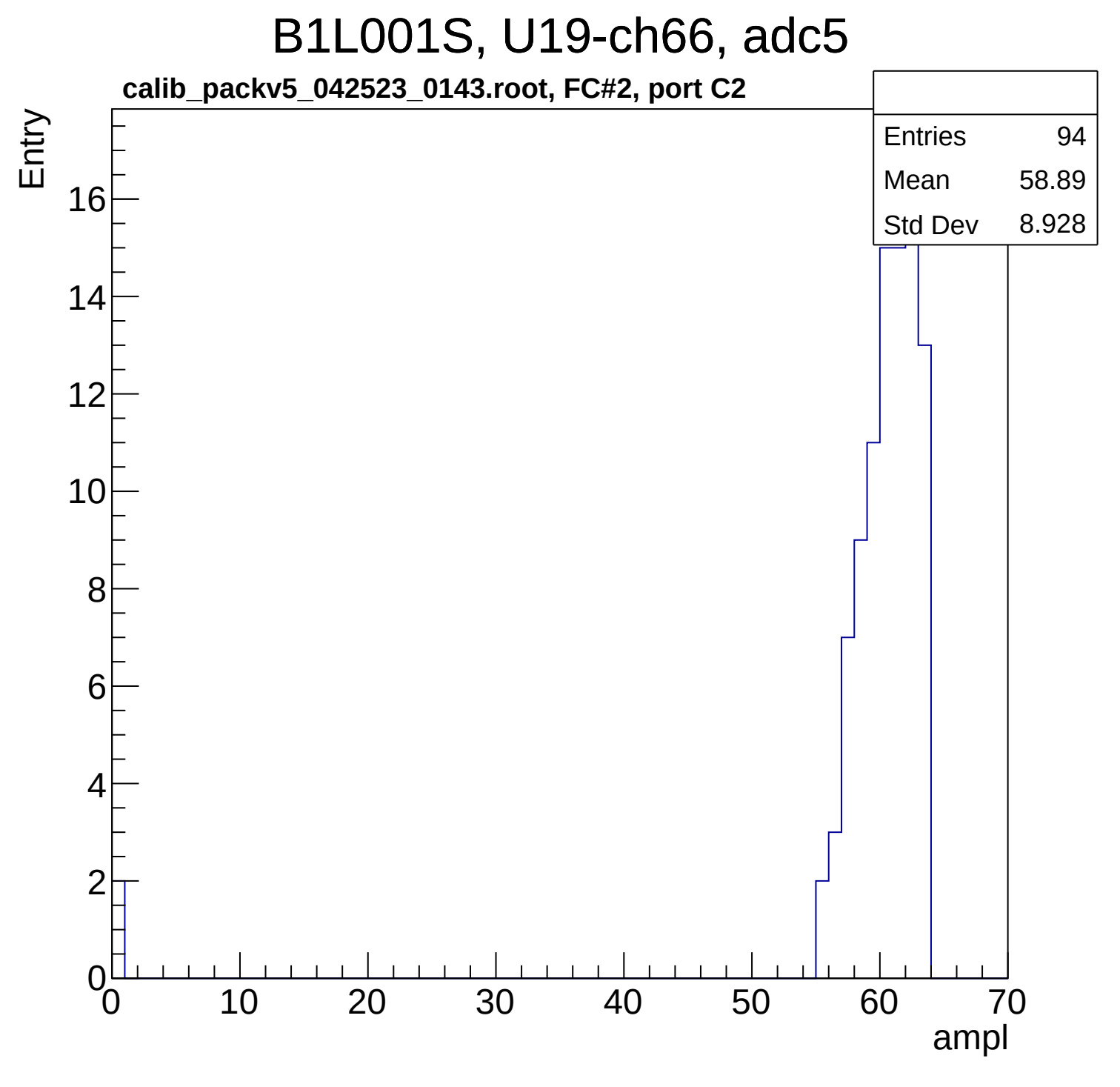
50
60
70
ampl


B1L001S, U19-ch66, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 94
Mean 58.89
Std Dev 8.928
Entry
ampl
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2
4
6
8
10
12
14
16
0
10
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40
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60
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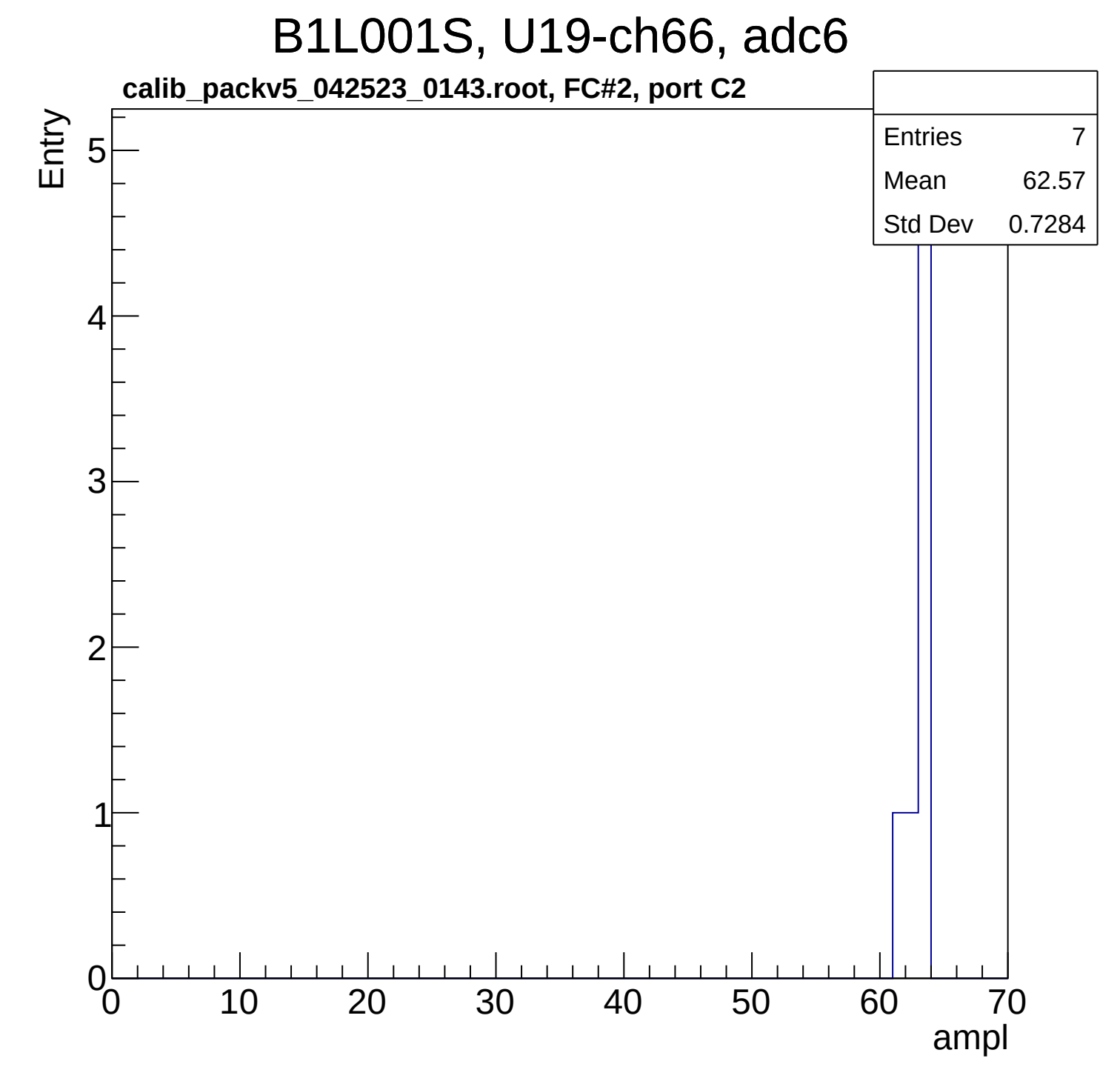
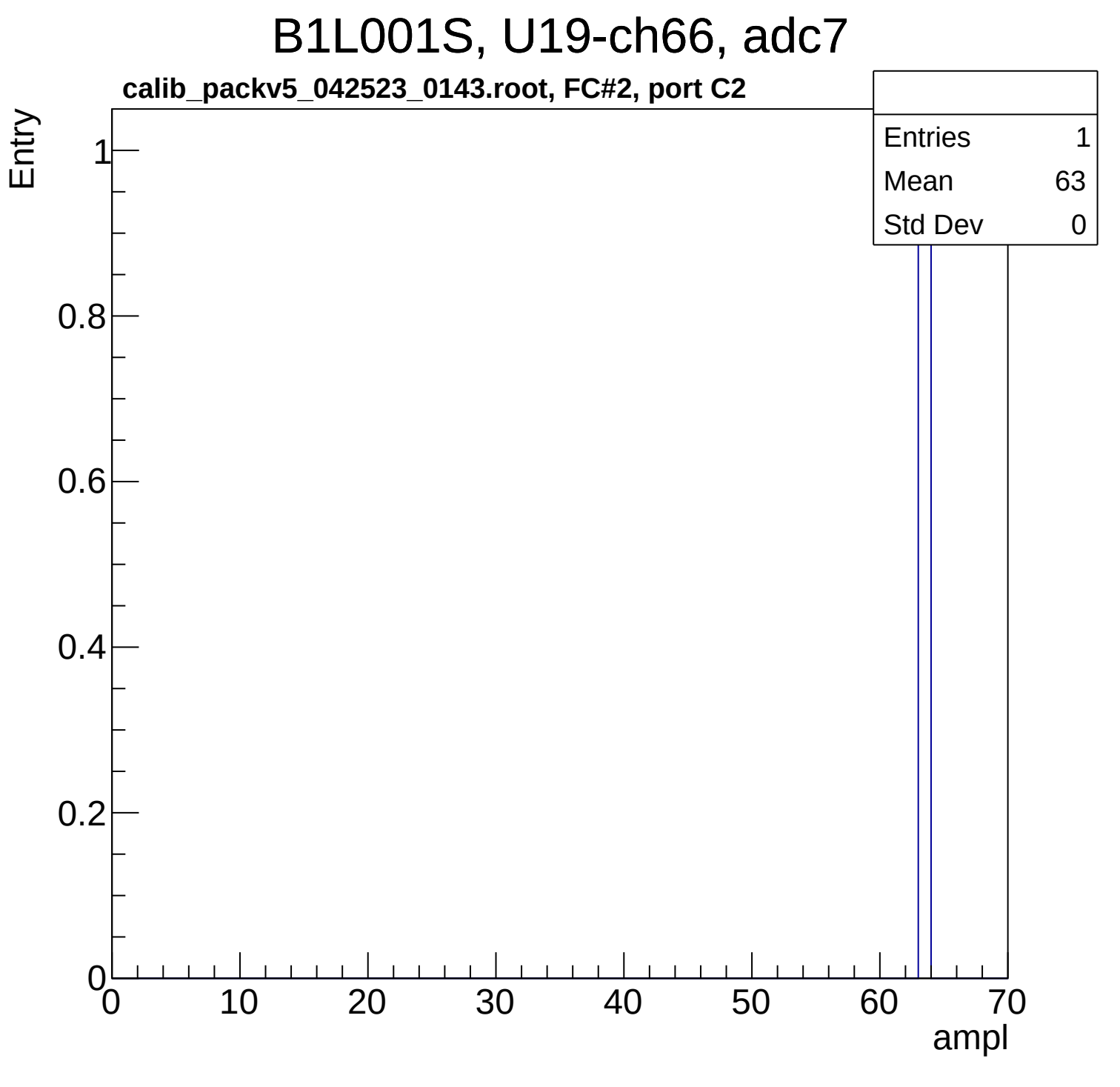

B1L001S, U19-ch66, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 7
Mean 62.57
Std Dev 0.7284
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch66, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 63
Std Dev 0
Entry
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0.6
0.4
0.2
0
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10
20
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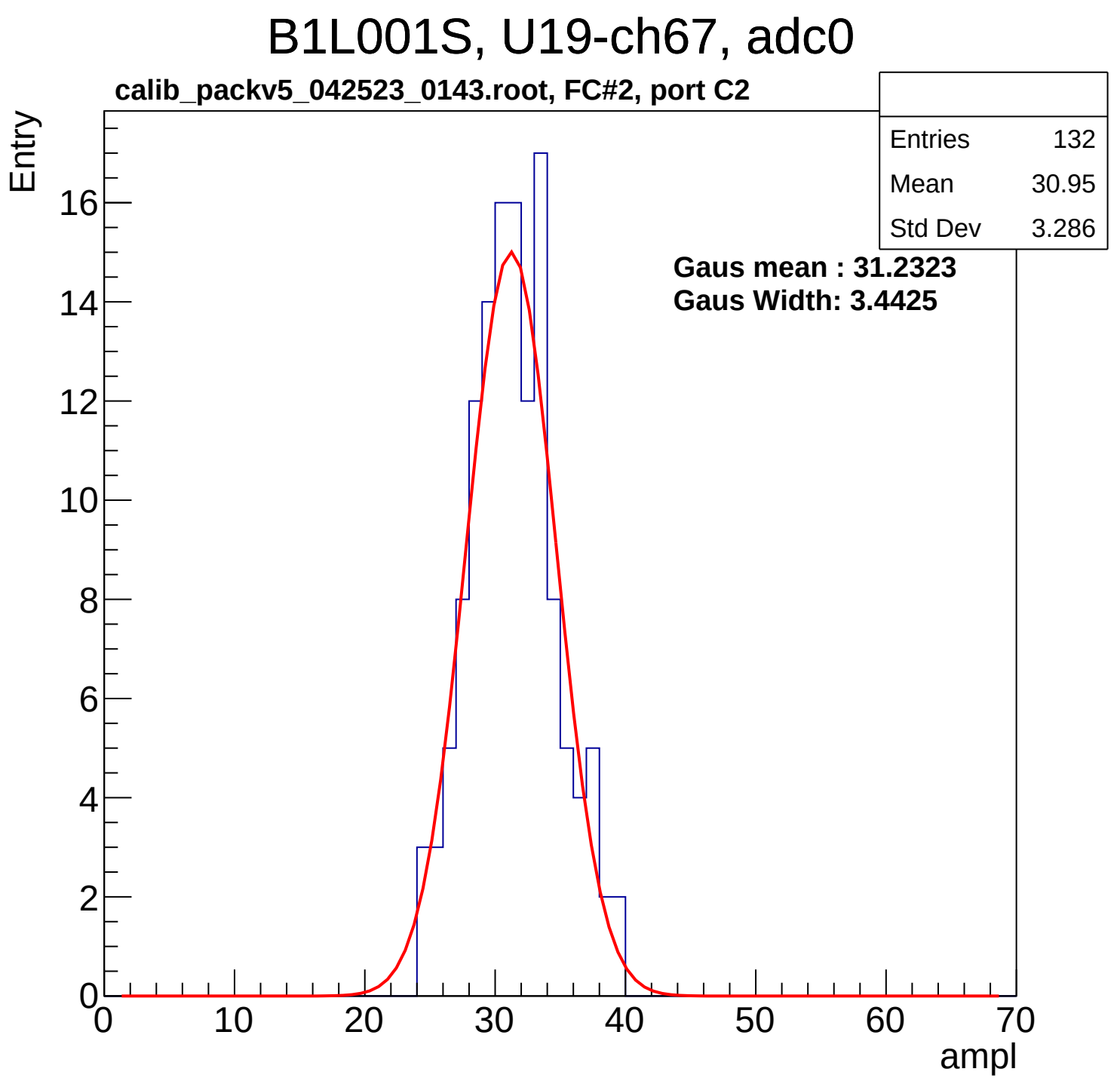
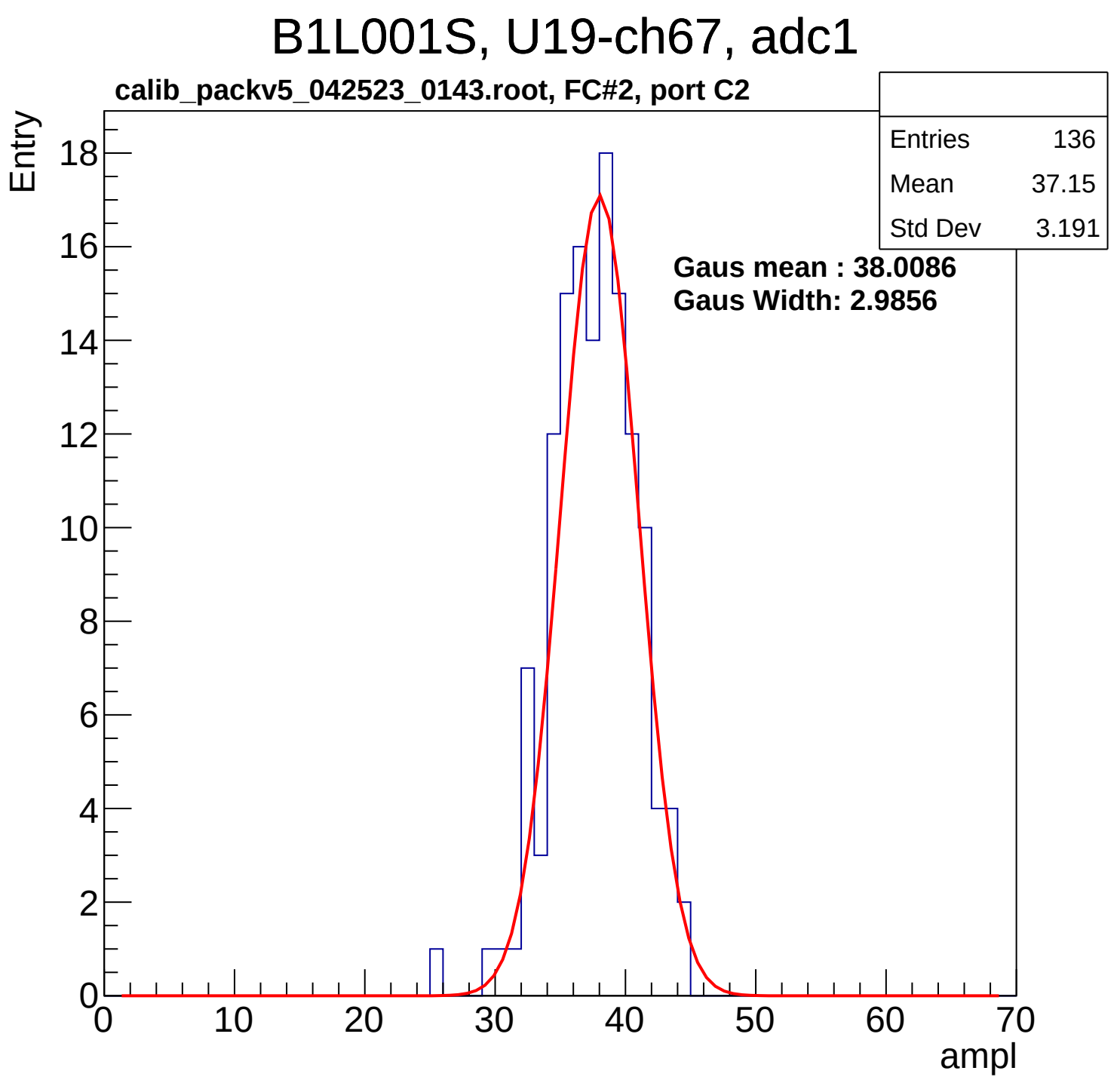
50
60
70
ampl


B1L001S, U19-ch67, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 132
Mean 30.95
Std Dev 3.286
Gaus mean : 31.2323
Gaus Width: 3.4425
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70


B1L001S, U19-ch67, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 136
Mean 37.15
Std Dev 3.191
Gaus mean : 38.0086
Gaus Width: 2.9856
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
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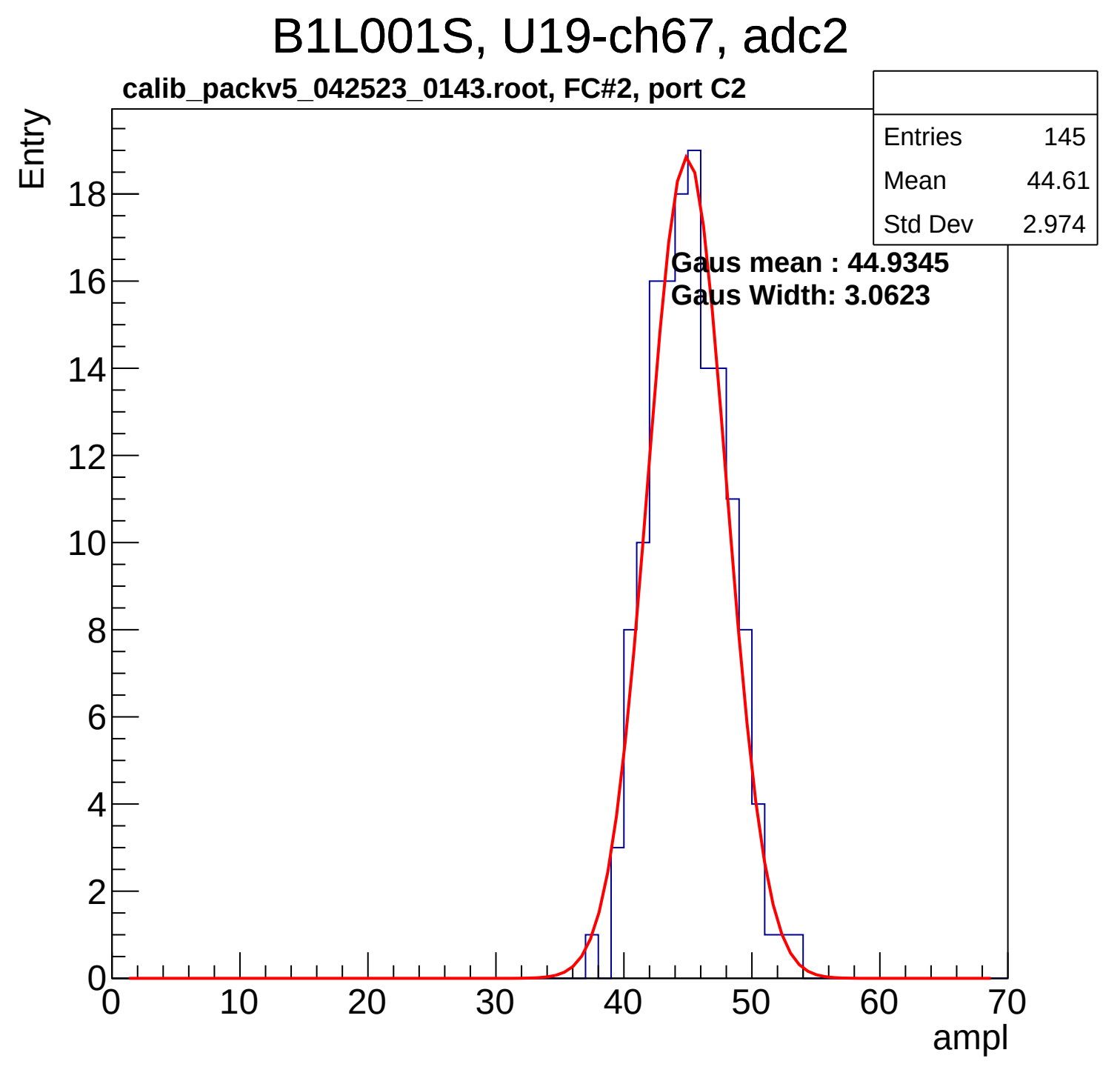
B1L001S, U19-ch67, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 145
Mean 44.61
Std Dev 2.974
Gaus mean : 44.9345
Gaus Width: 3.0623
Entry
ampl
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2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
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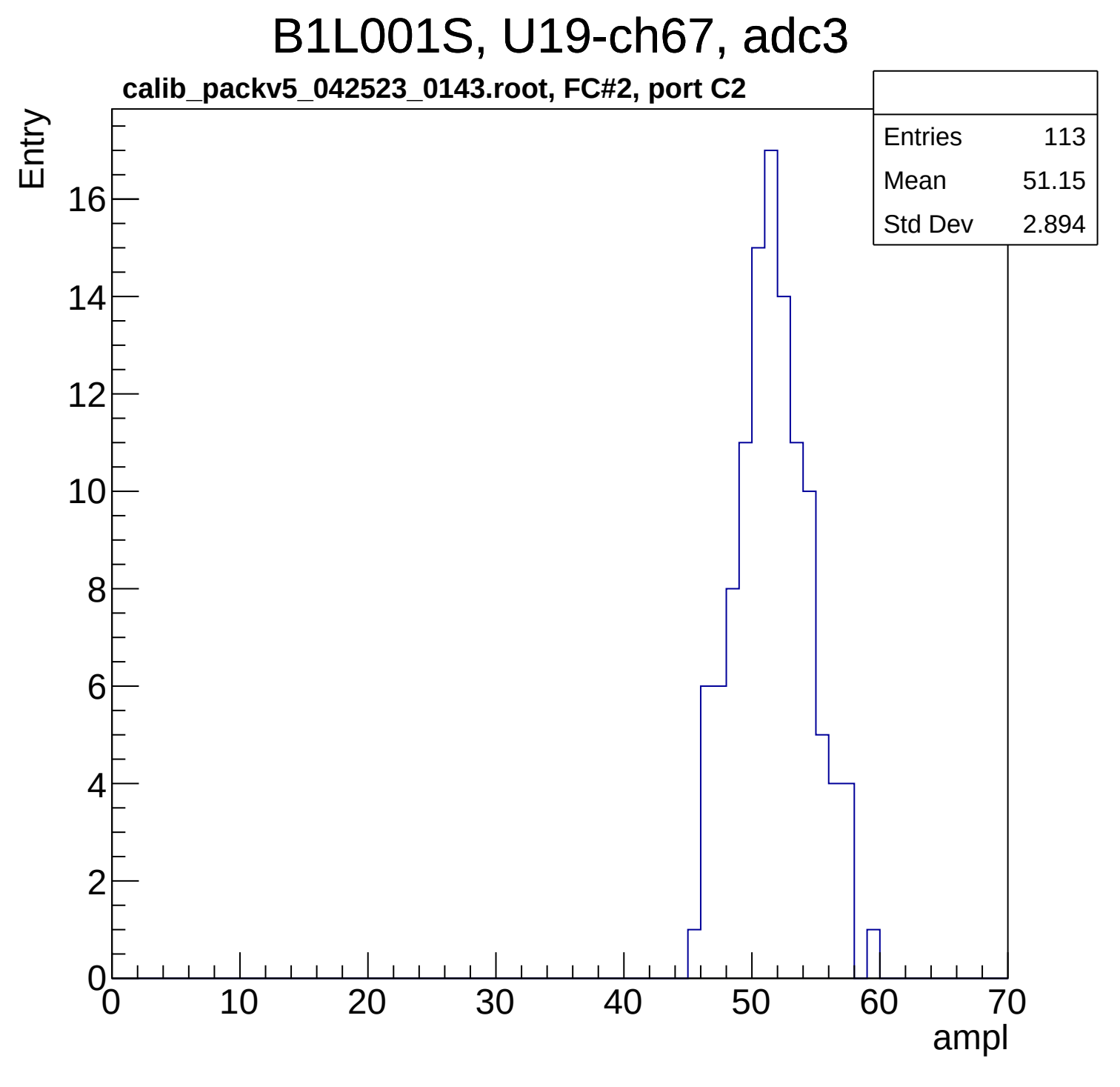
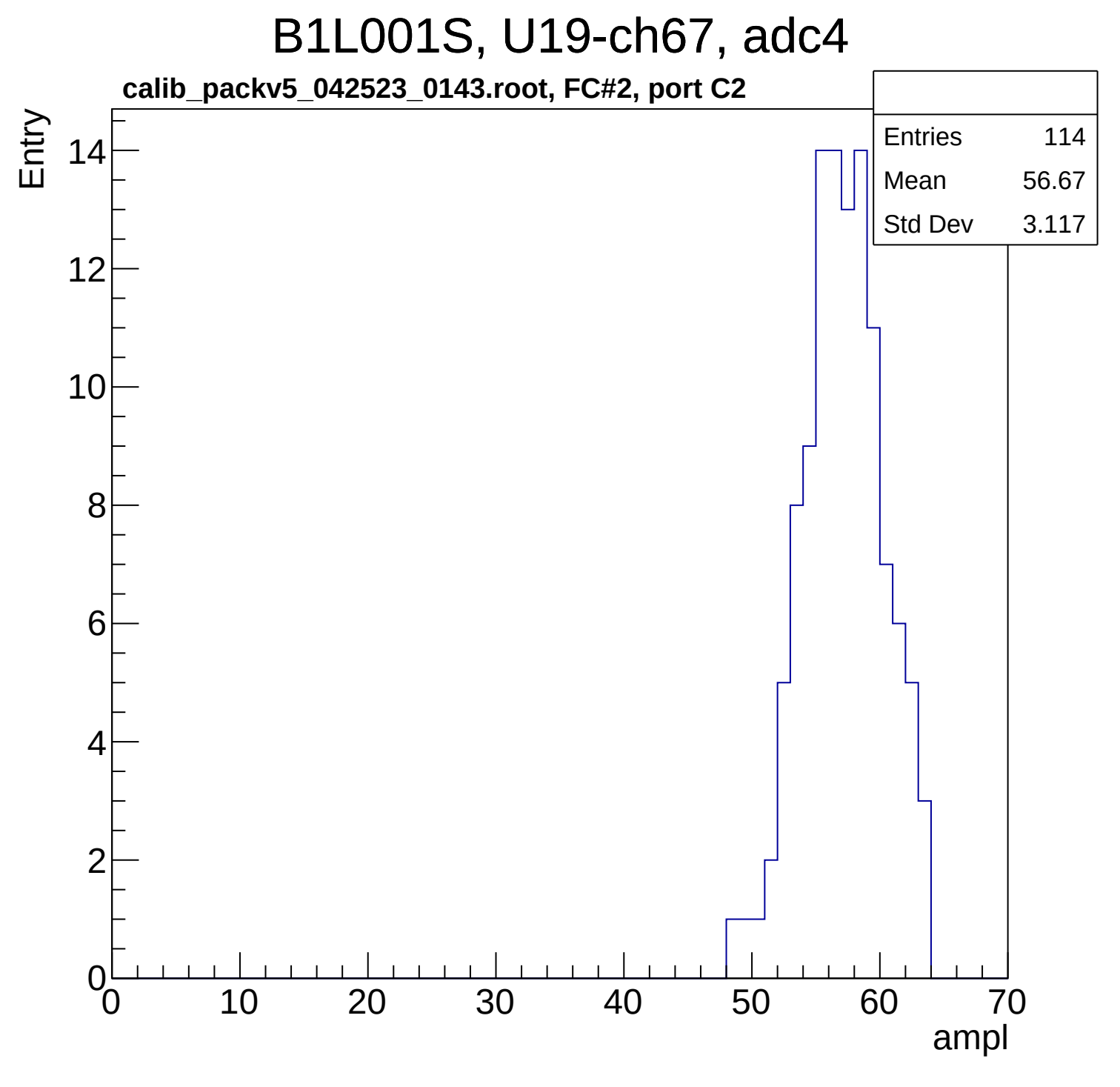

B1L001S, U19-ch67, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 113
Mean 51.15
Std Dev 2.894
Entry
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch67, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 114
Mean 56.67
Std Dev 3.117
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
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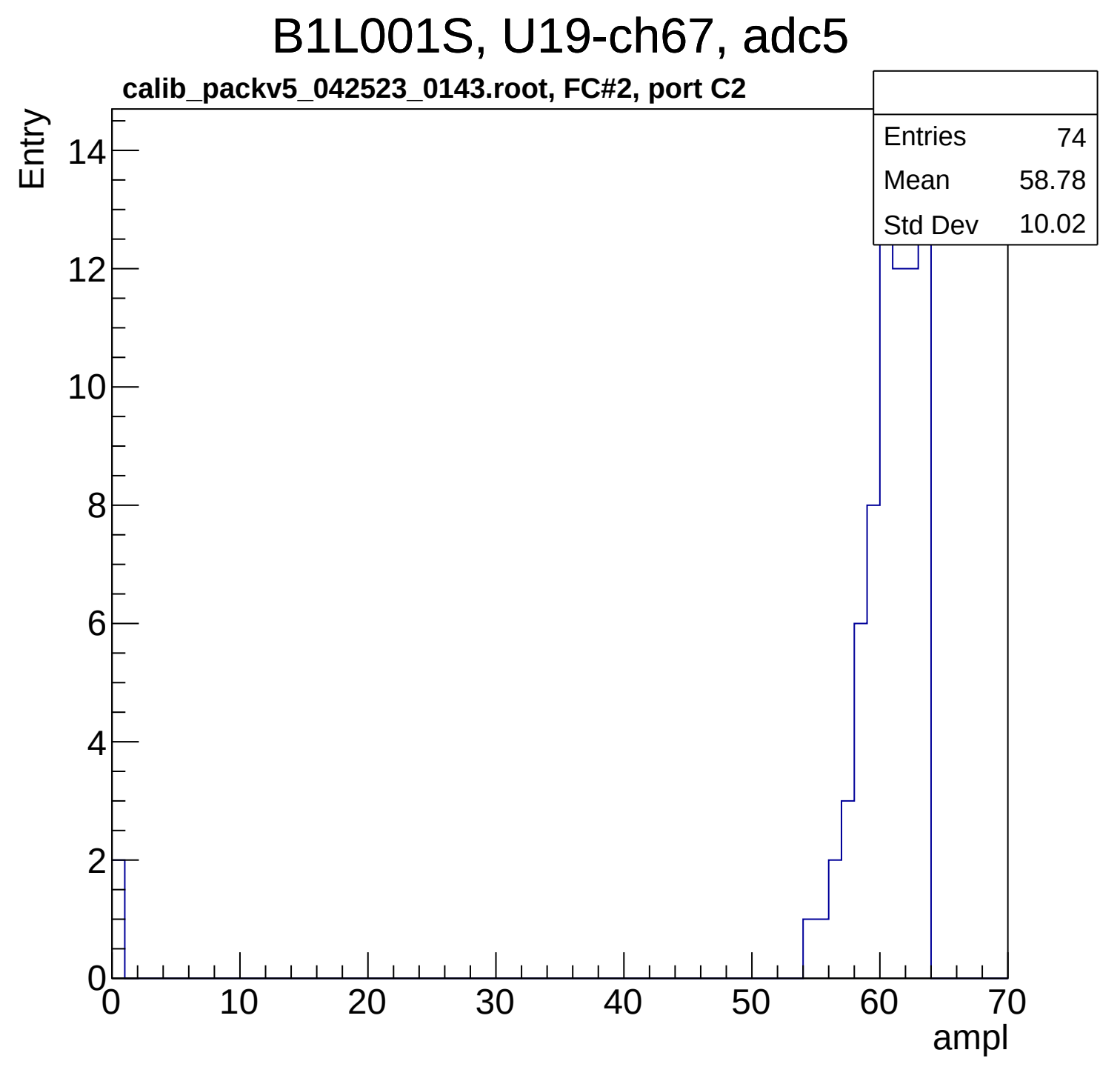
60
70


B1L001S, U19-ch67, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 74
Mean 58.78
Std Dev 10.02
Entry
ampl
0
2
4
6
8
10
12
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0
10
20
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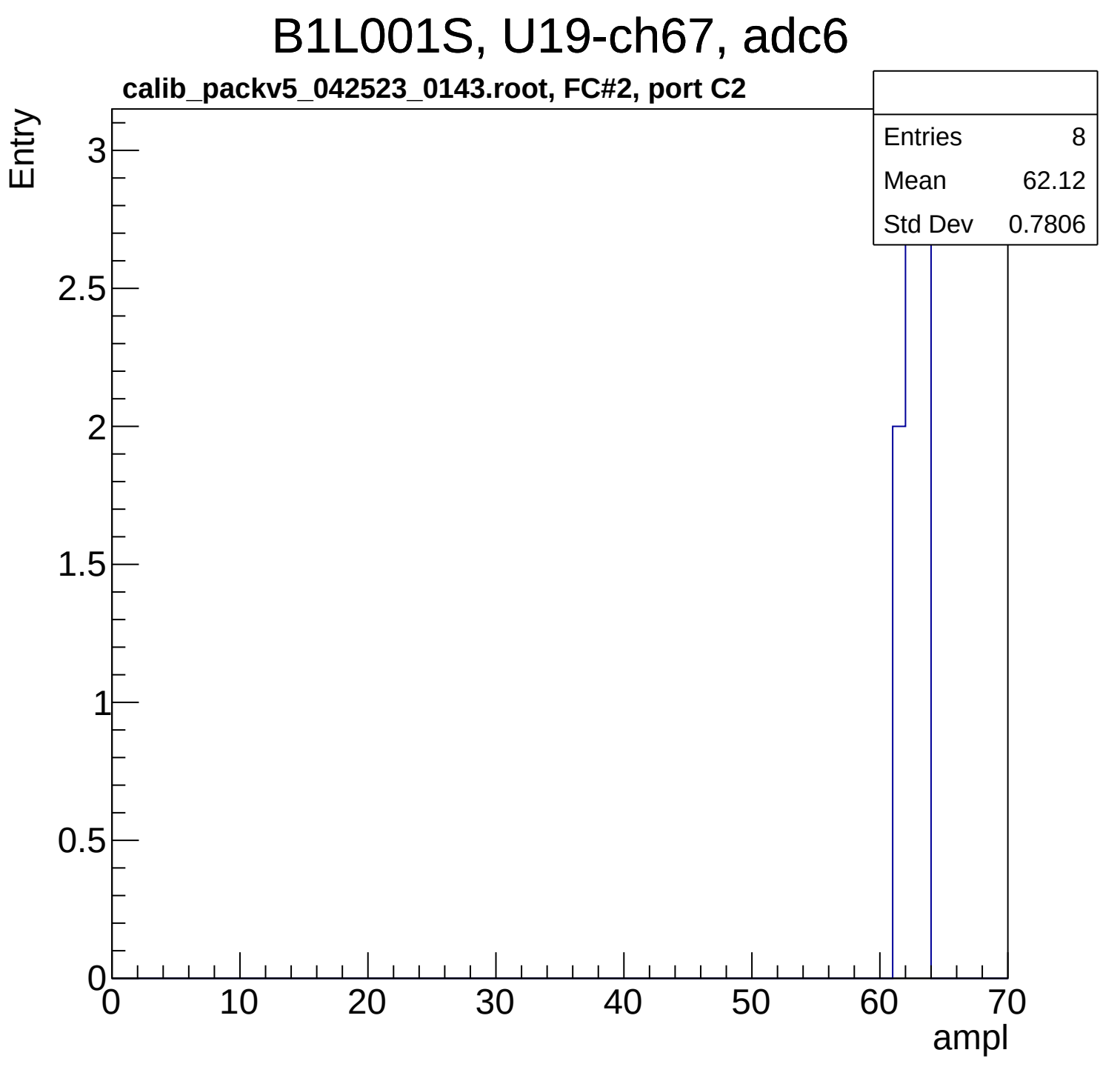
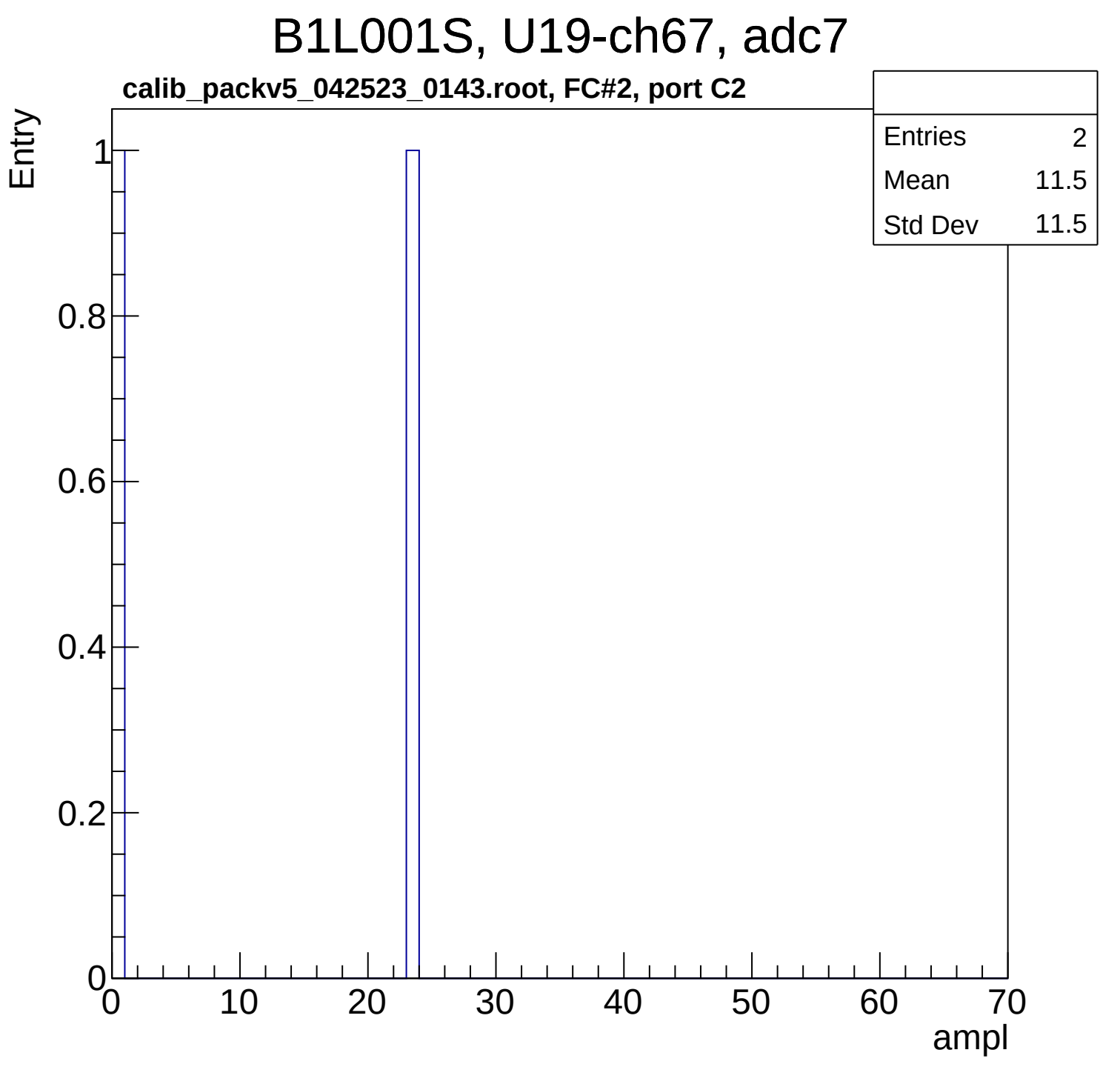
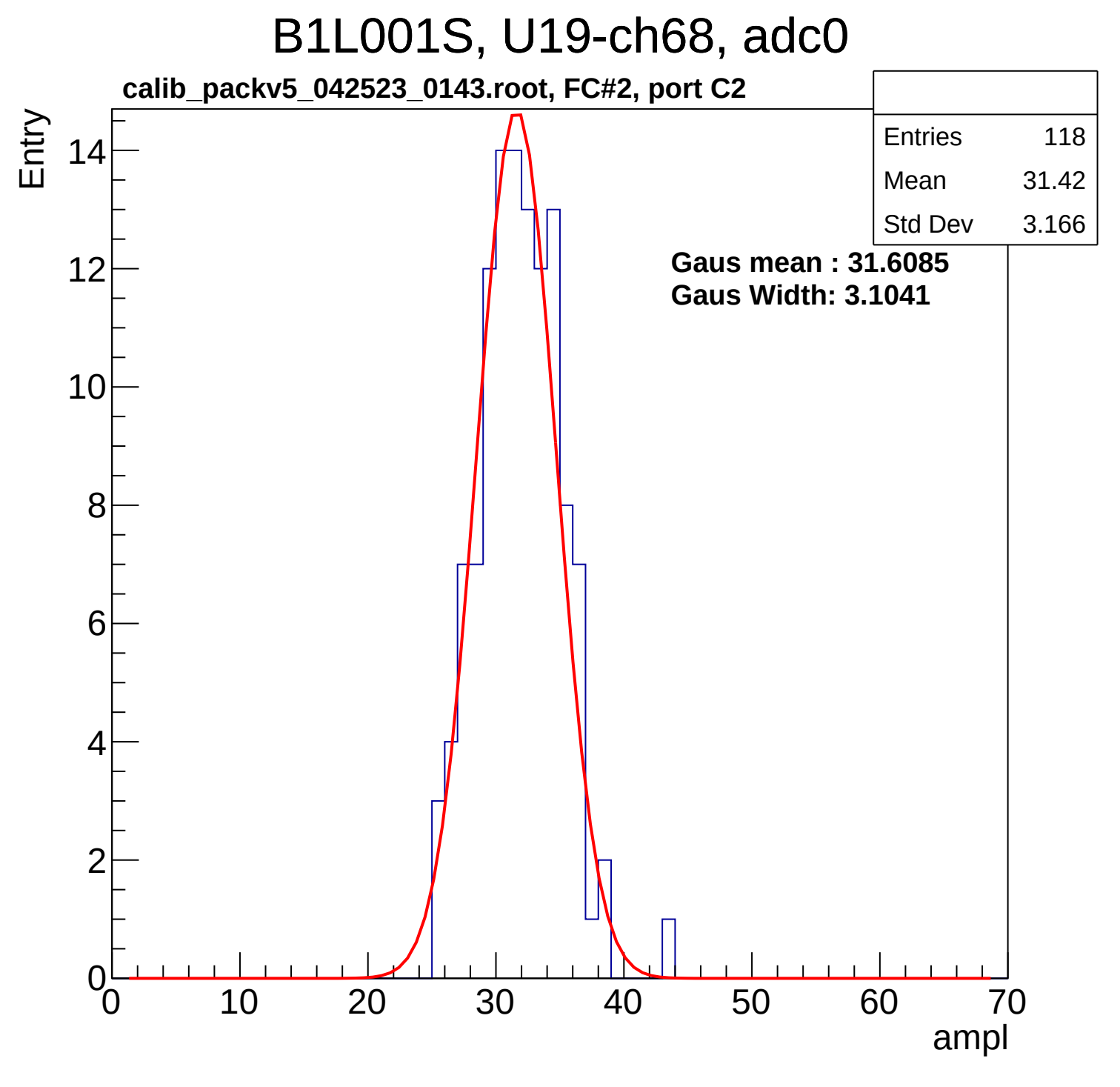
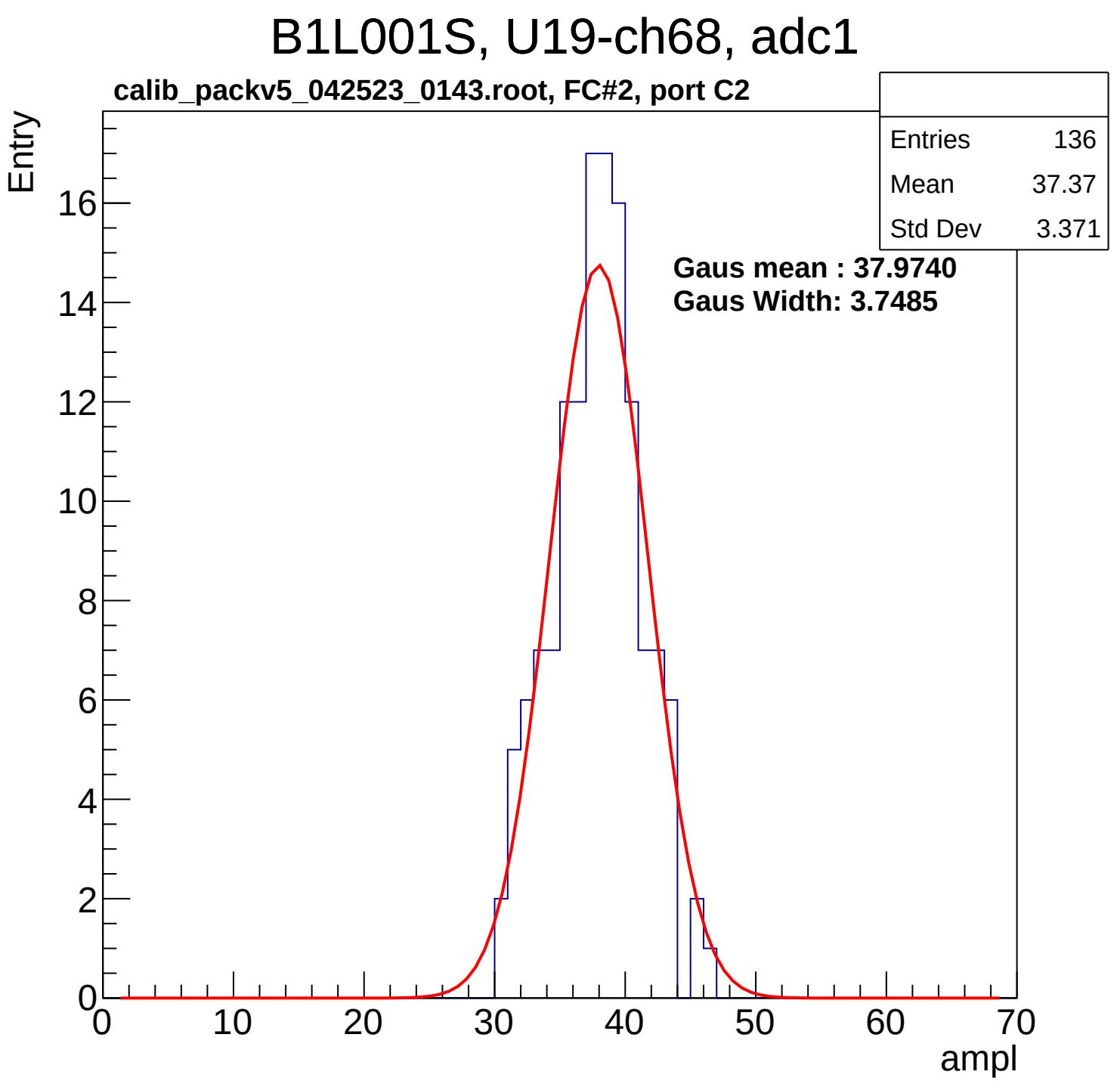
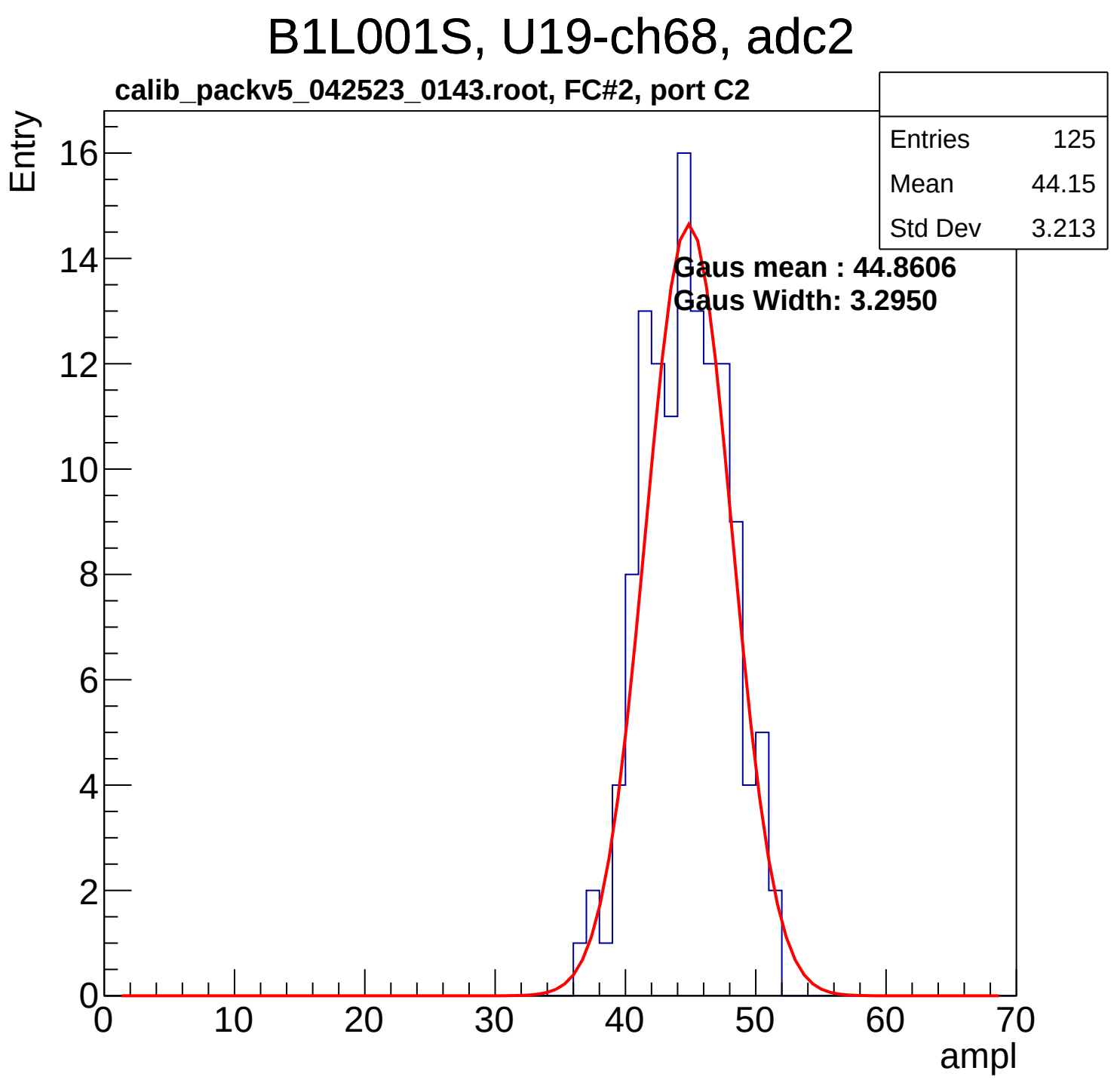
40
50
60
70

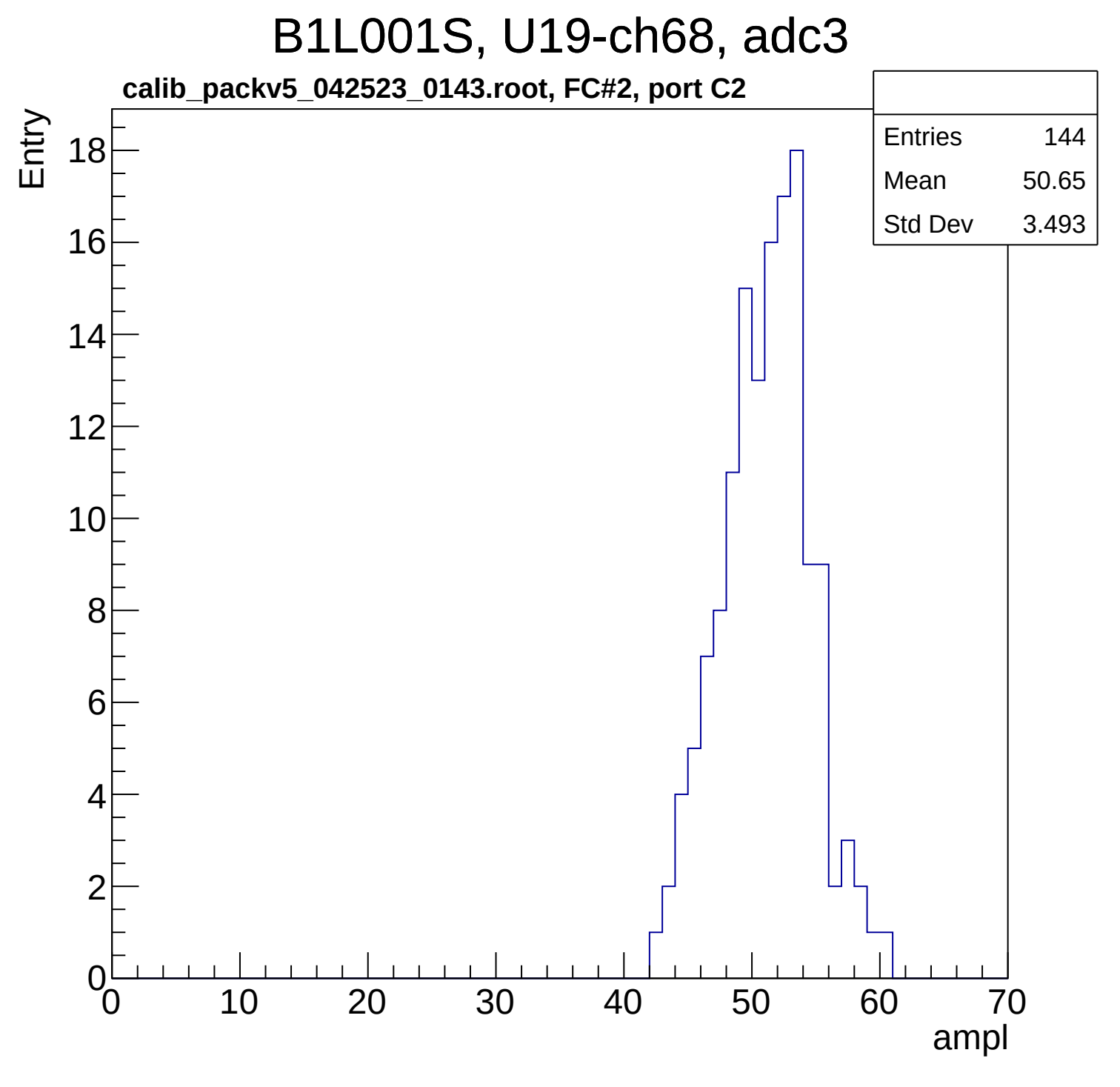

B1L001S, U19-ch67, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 8
Mean 62.12
Std Dev 0.7806
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L001S, U19-ch67, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 11.5
Std Dev 11.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch68, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 118
Mean 31.42
Std Dev 3.166
Gaus mean : 31.6085
Gaus Width: 3.1041
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L001S, U19-ch68, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 136
Mean 37.37
Std Dev 3.371
Gaus mean : 37.9740
Gaus Width: 3.7485
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70


B1L001S, U19-ch68, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 125
Mean 44.15
Std Dev 3.213
Gaus mean : 44.8606
Gaus Width: 3.2950
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70


B1L001S, U19-ch68, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 144
Mean 50.65
Std Dev 3.493
Entry
ampl
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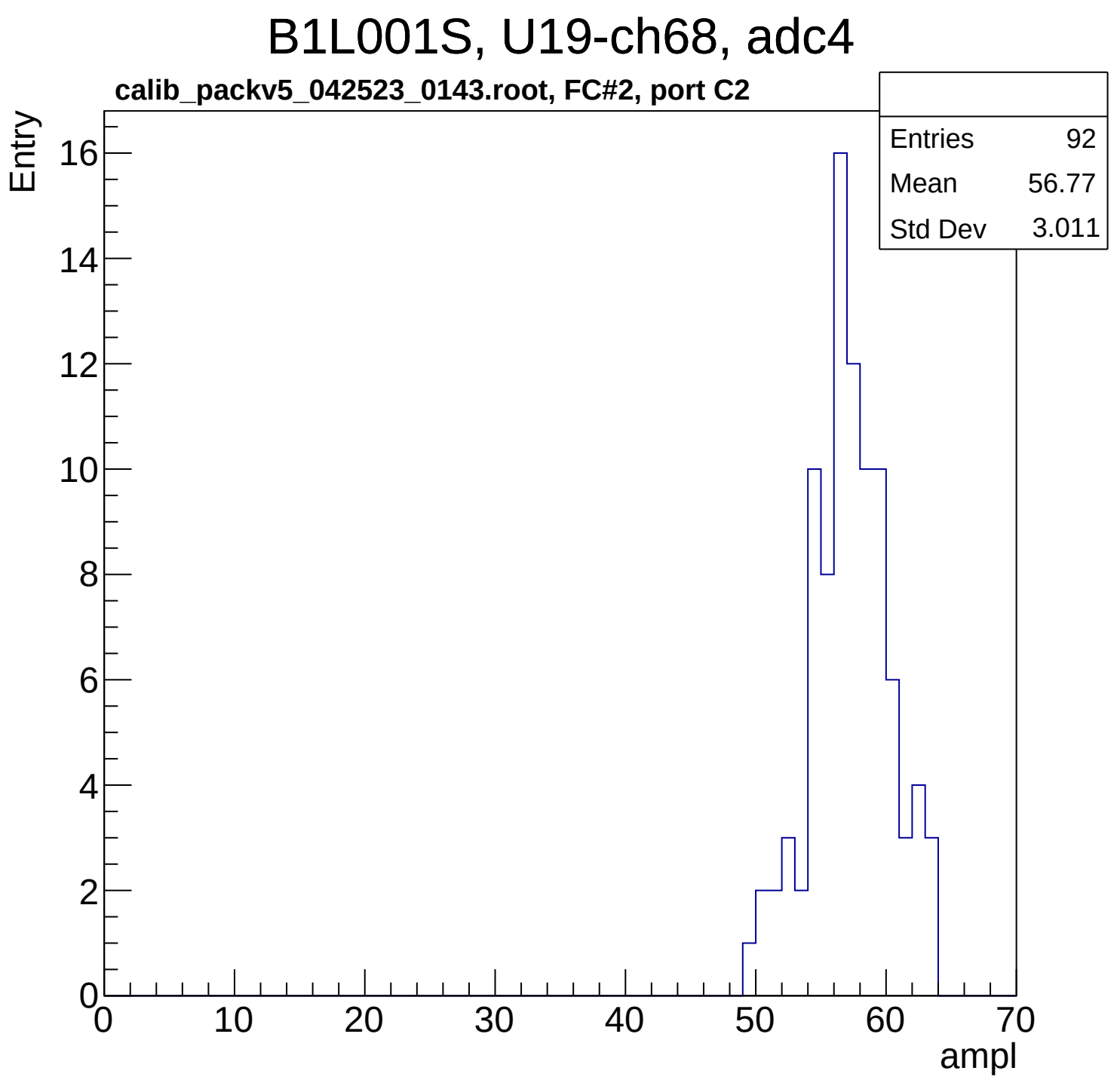
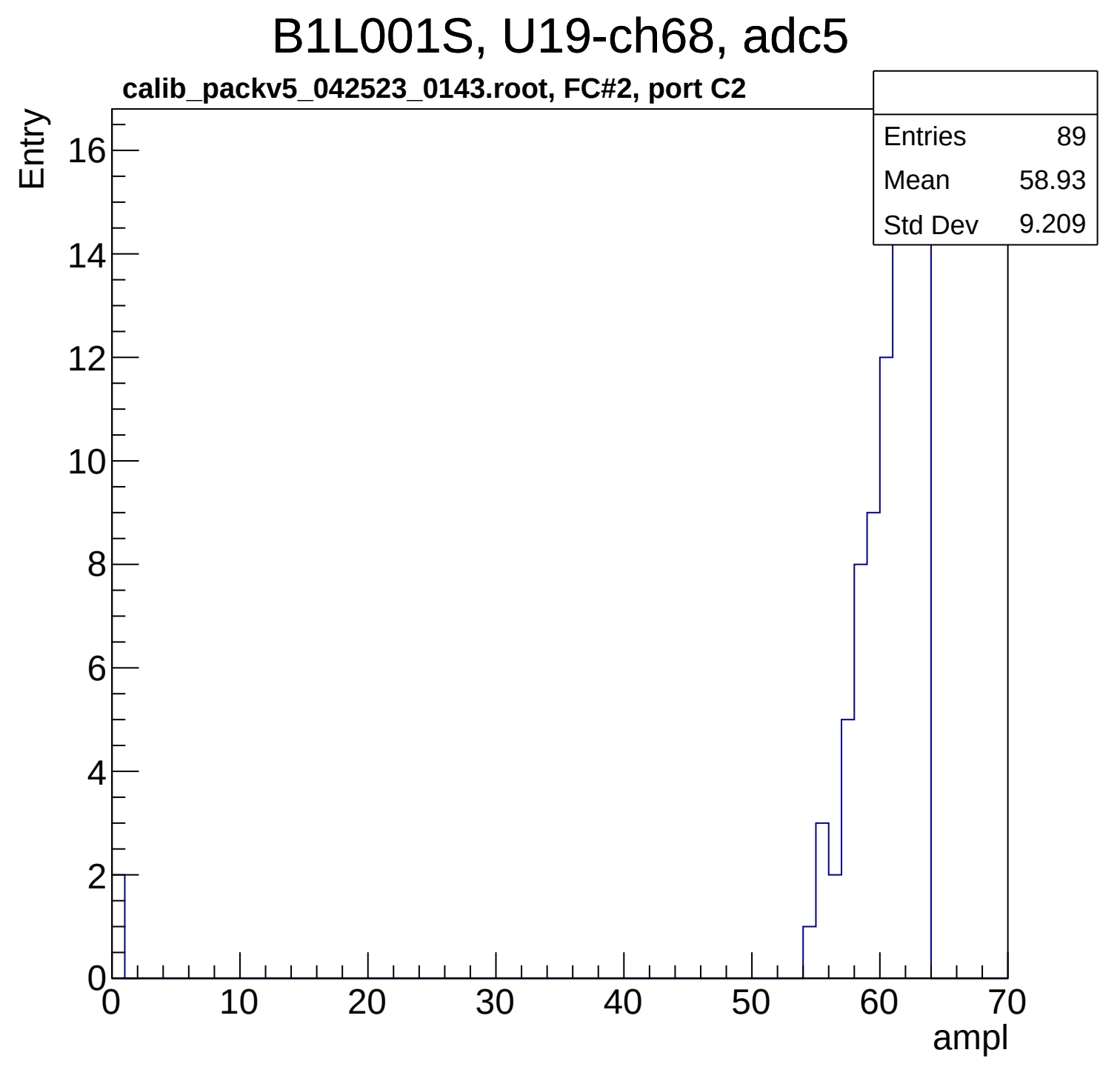
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70


B1L001S, U19-ch68, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 92
Mean 56.77
Std Dev 3.011
Entry
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch68, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 89
Mean 58.93
Std Dev 9.209
Entry
ampl
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2
4
6
8
10
12
14
16
0
10
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40
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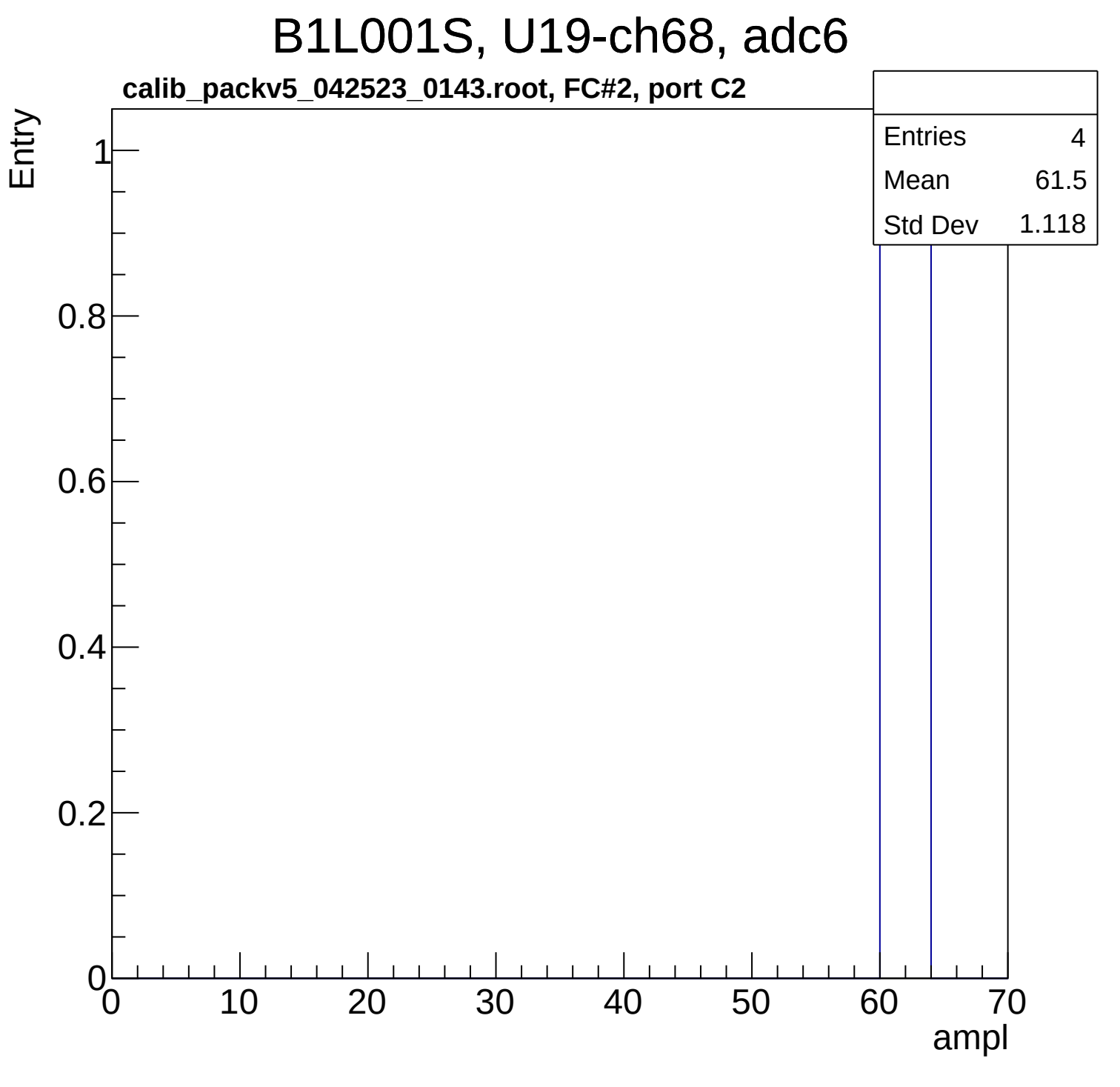
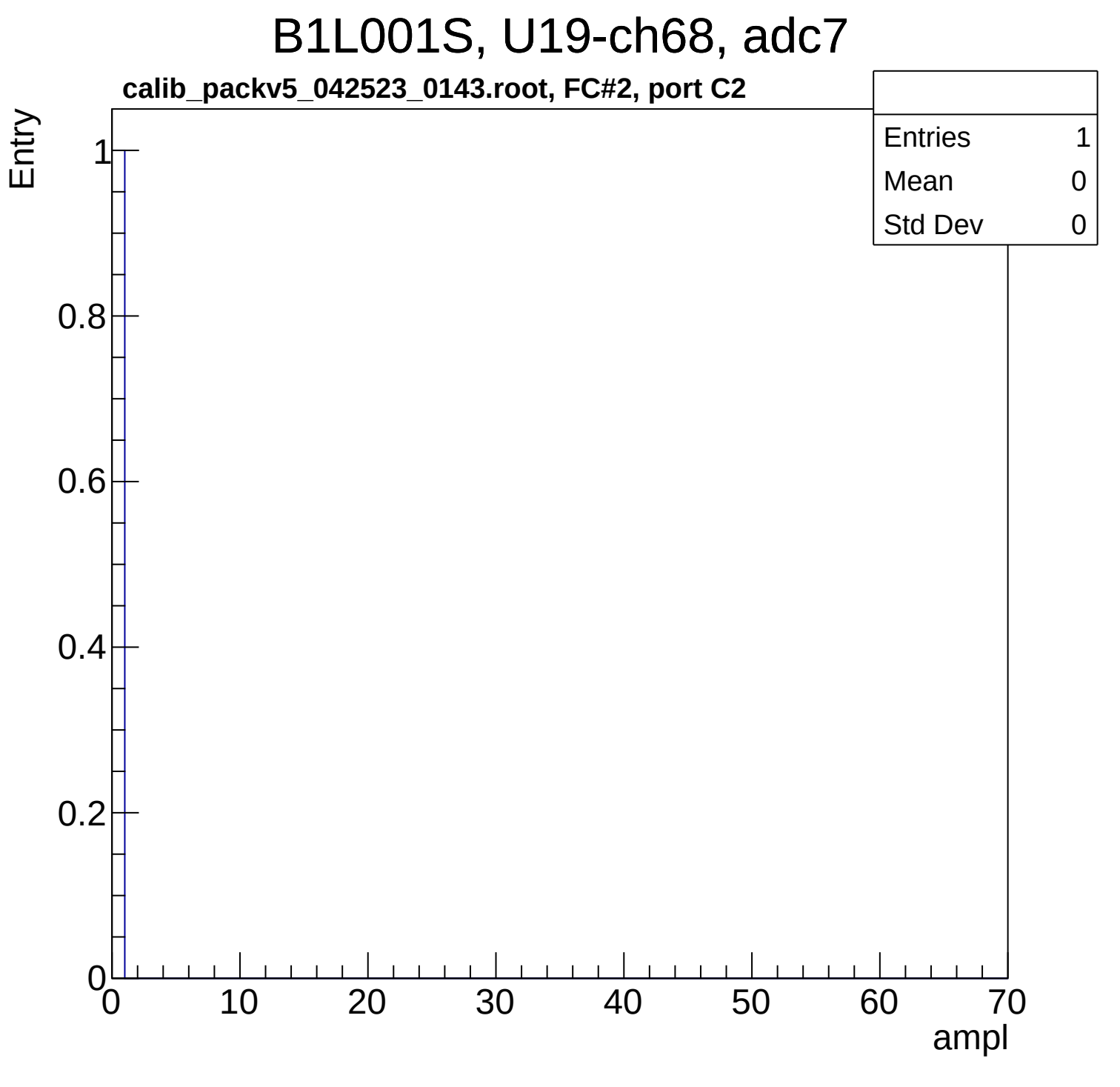
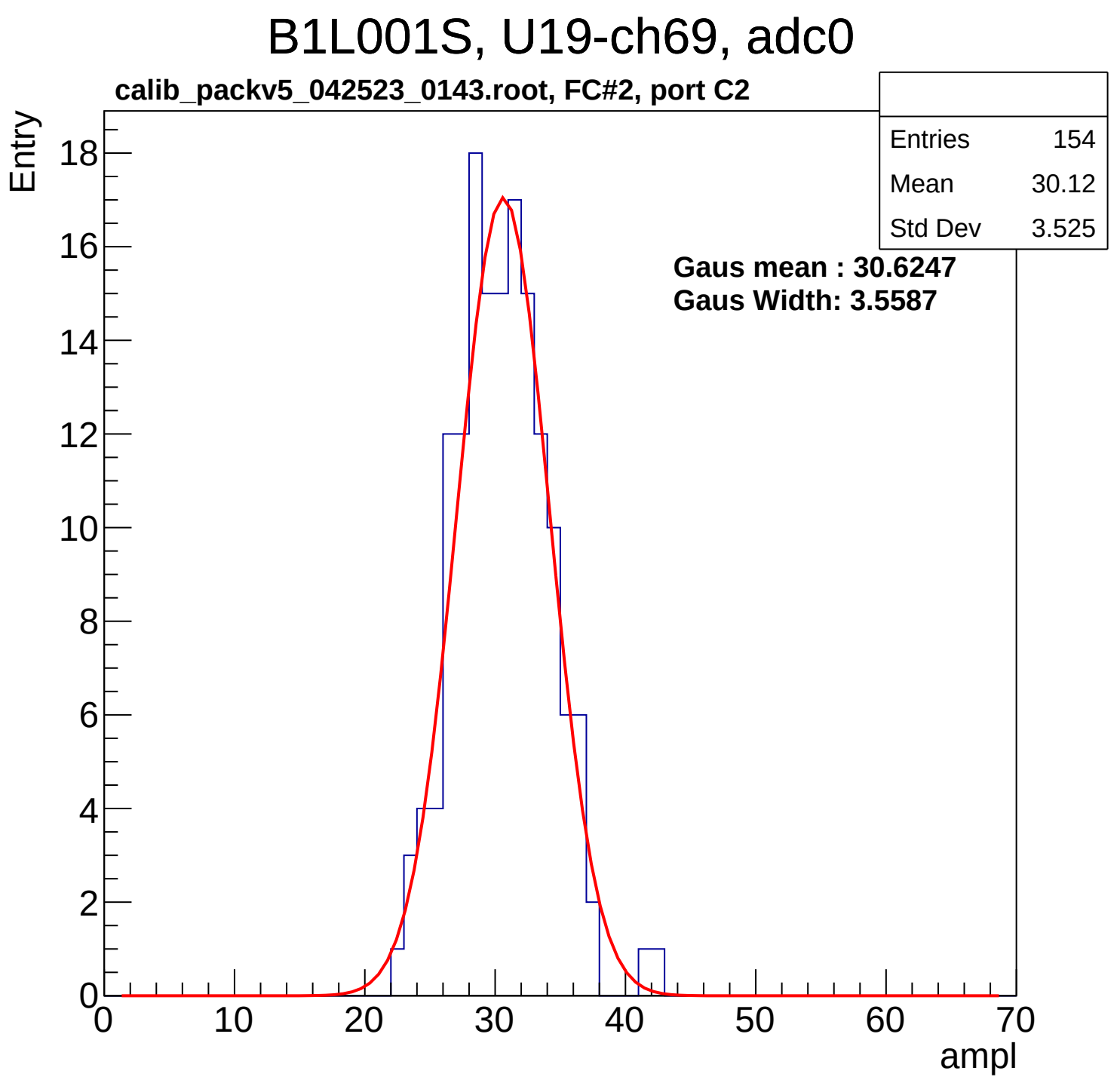
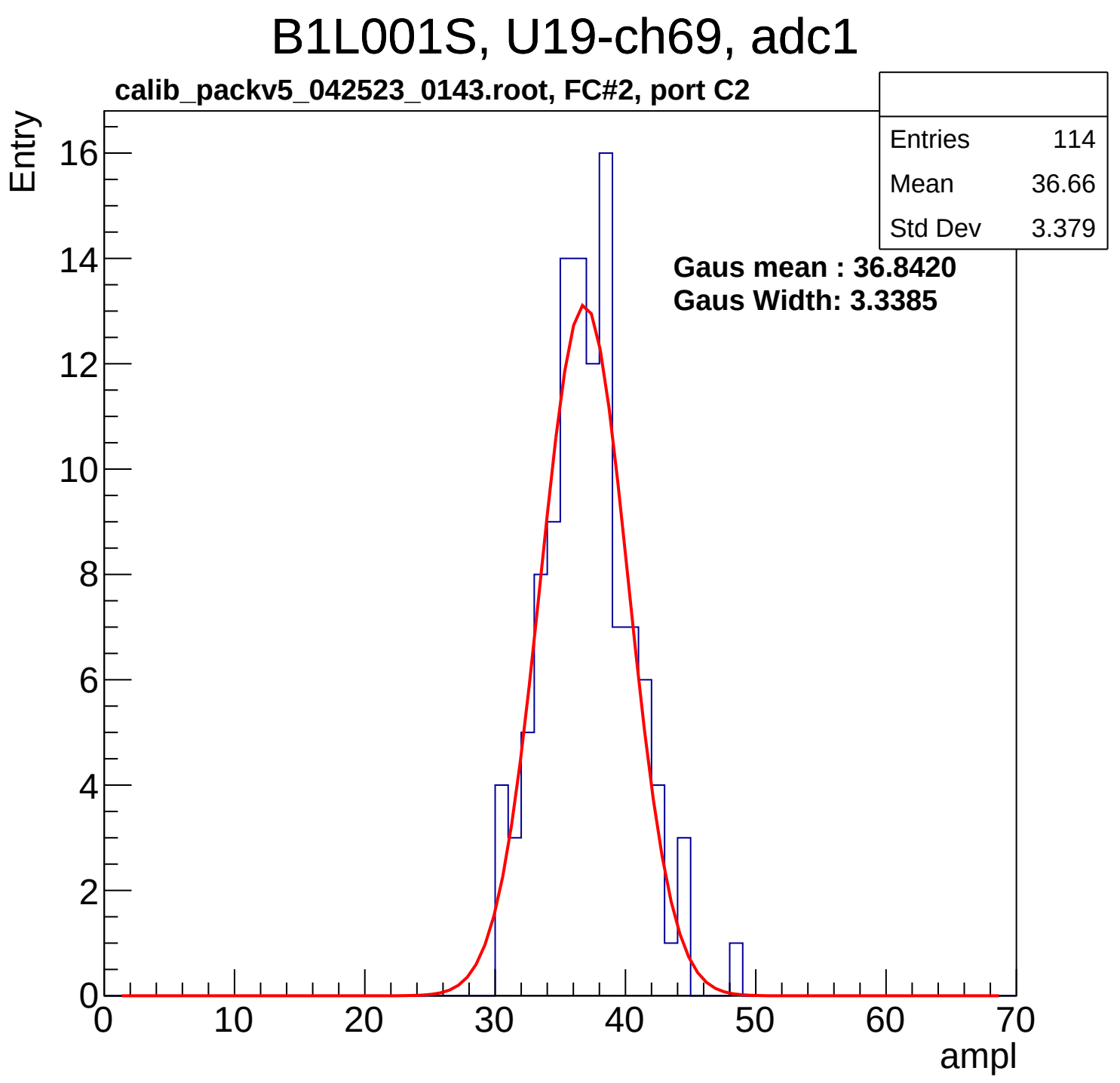
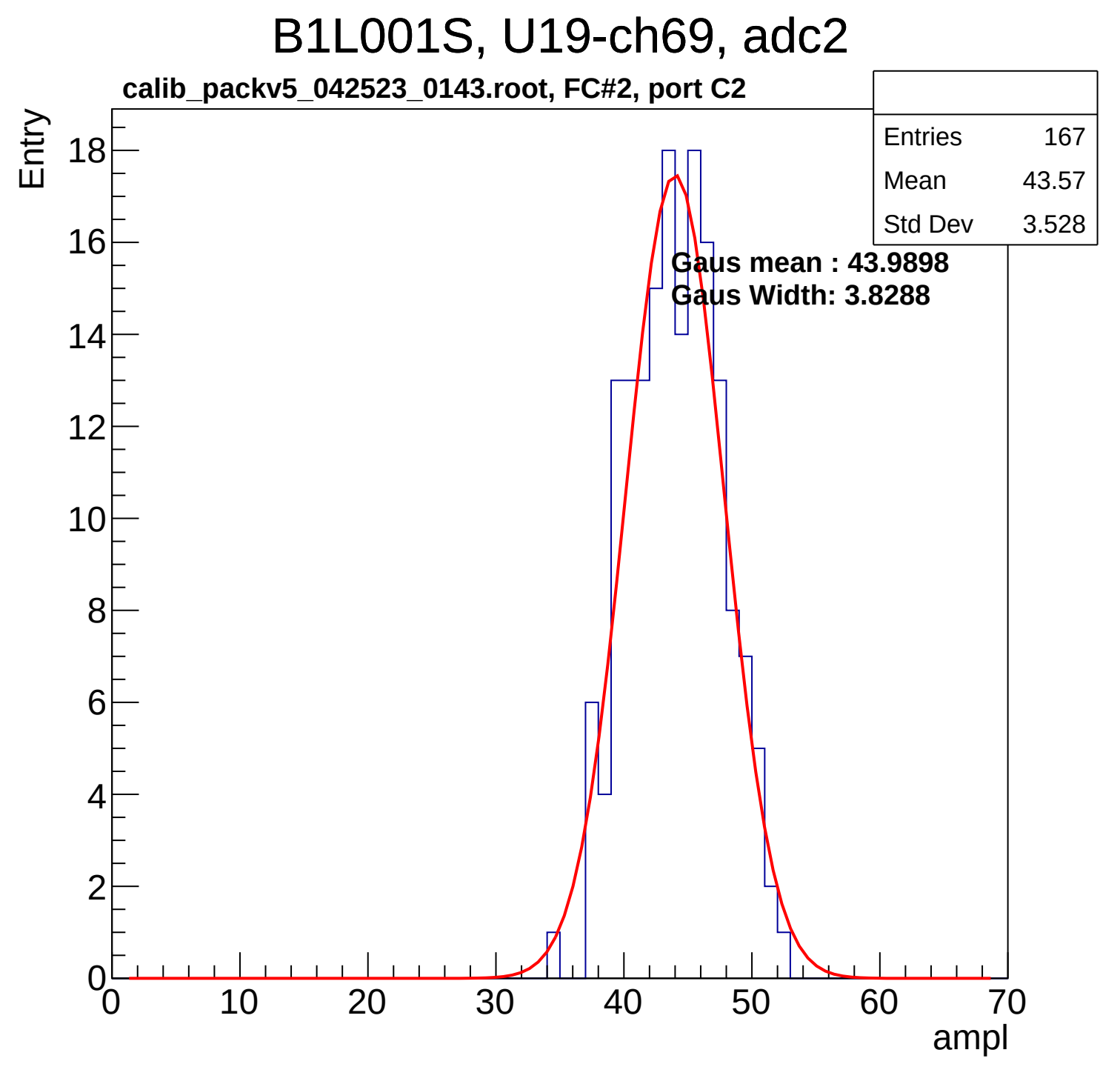
60
70

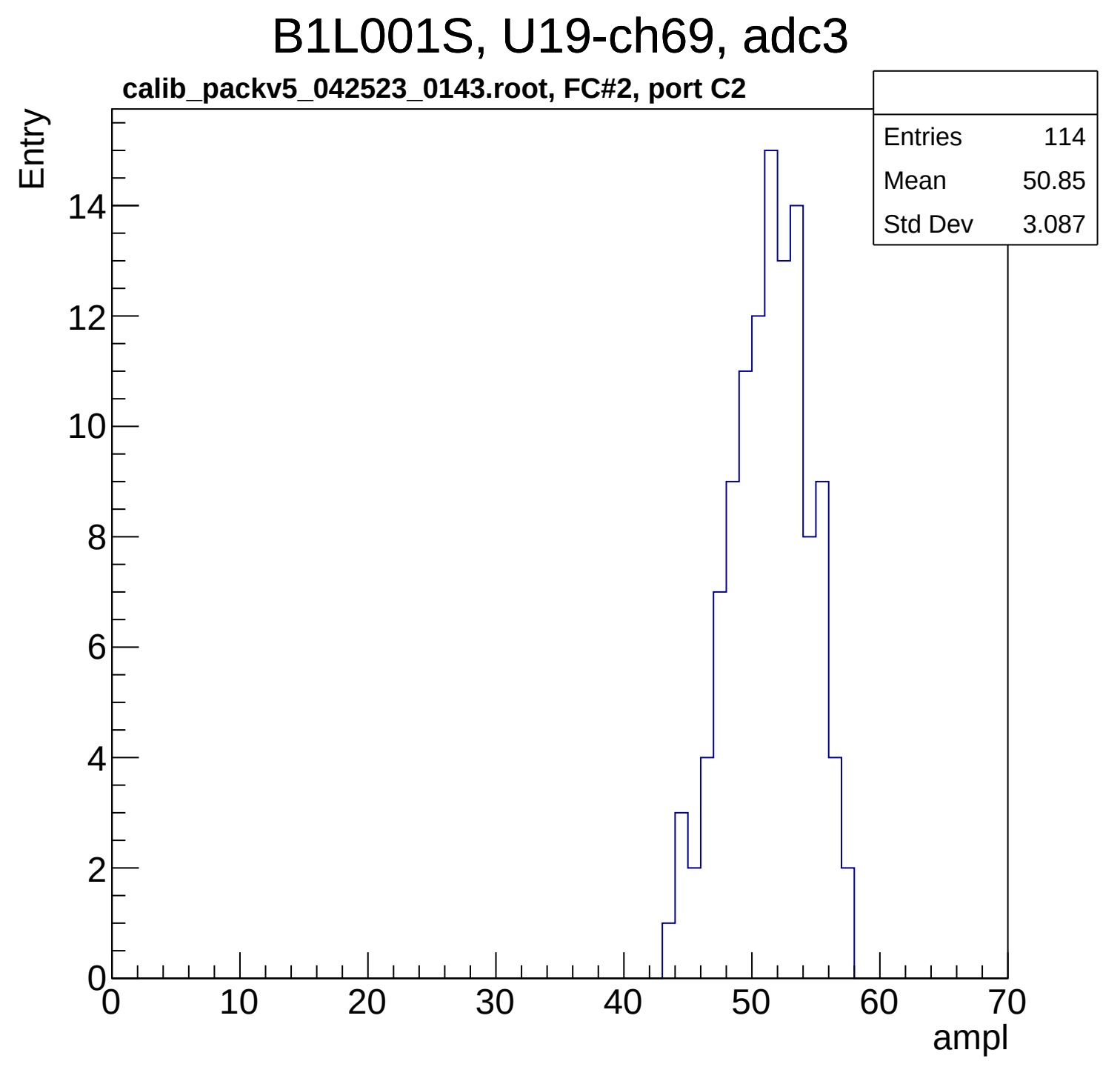

B1L001S, U19-ch68, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 4
Mean 61.5
Std Dev 1.118
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

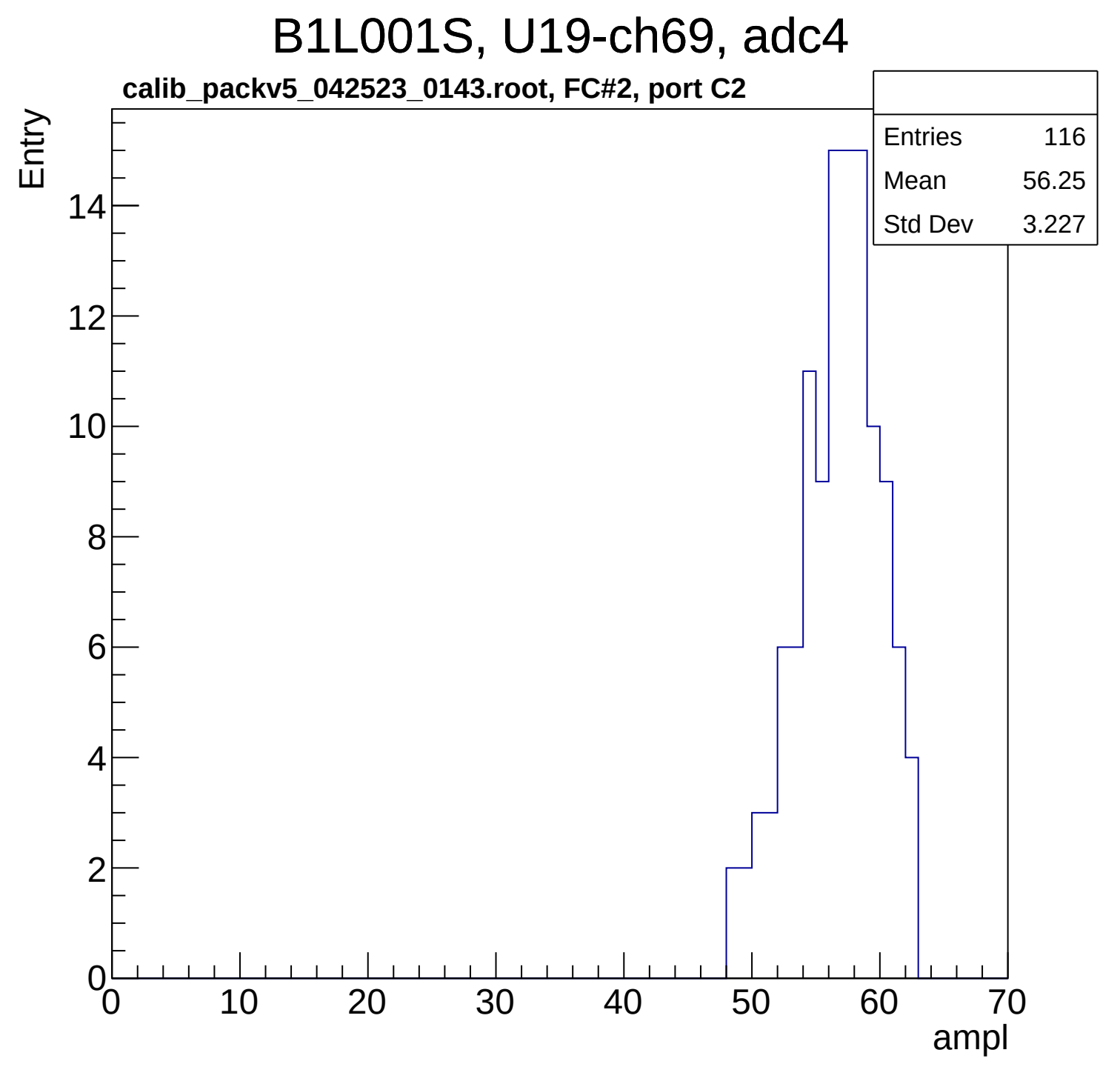

B1L001S, U19-ch68, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

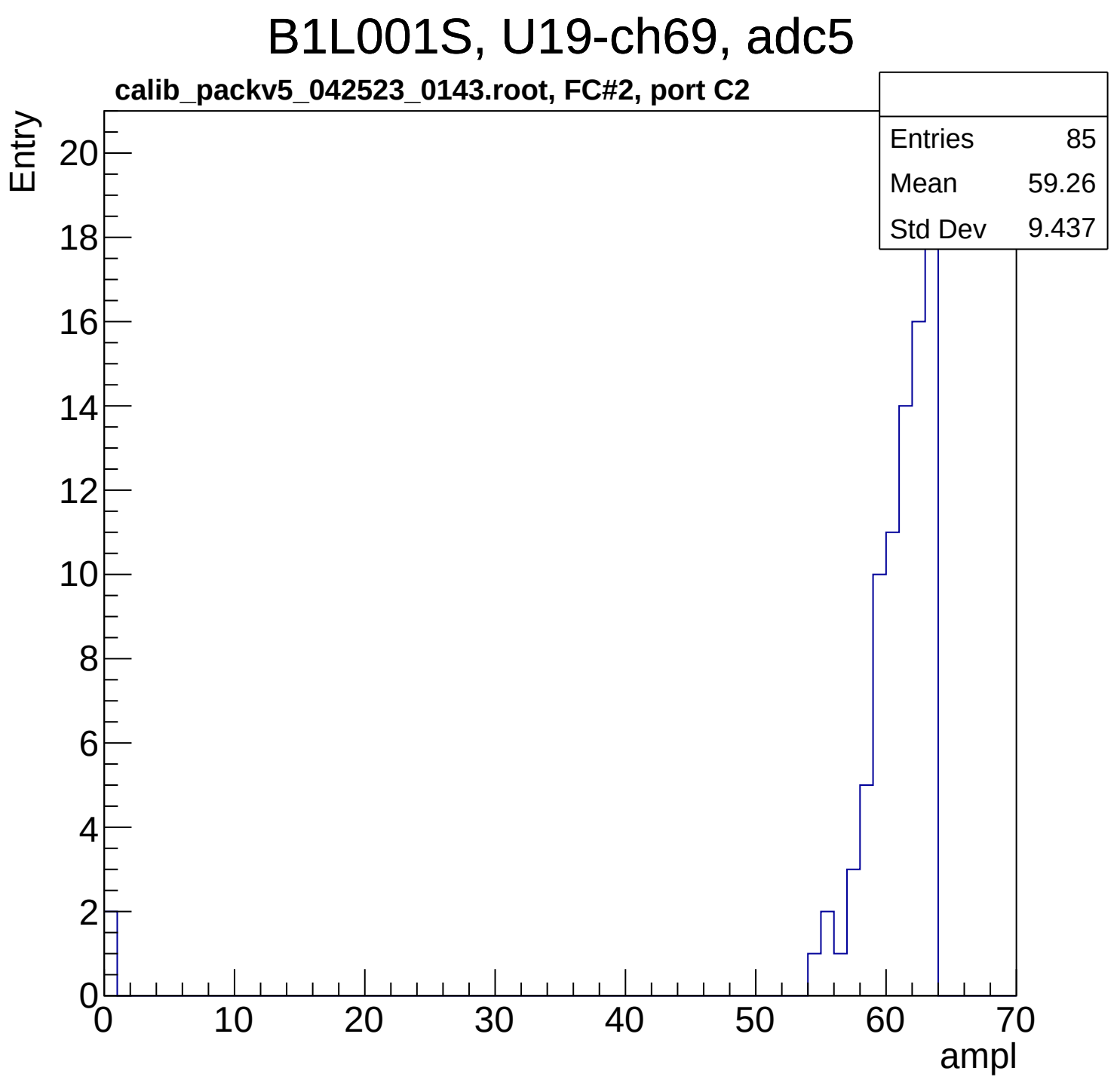

B1L001S, U19-ch69, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 154
Mean 30.12
Std Dev 3.525
Gaus mean : 30.6247
Gaus Width: 3.5587
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70


B1L001S, U19-ch69, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 114
Mean 36.66
Std Dev 3.379
Gaus mean : 36.8420
Gaus Width: 3.3385
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70


B1L001S, U19-ch69, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 167
Mean 43.57
Std Dev 3.528
Gaus mean : 43.9898
Gaus Width: 3.8288
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70


B1L001S, U19-ch69, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 114
Mean 50.85
Std Dev 3.087
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch69, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 116
Mean 56.25
Std Dev 3.227
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch69, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 85
Mean 59.26
Std Dev 9.437
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
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20
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60
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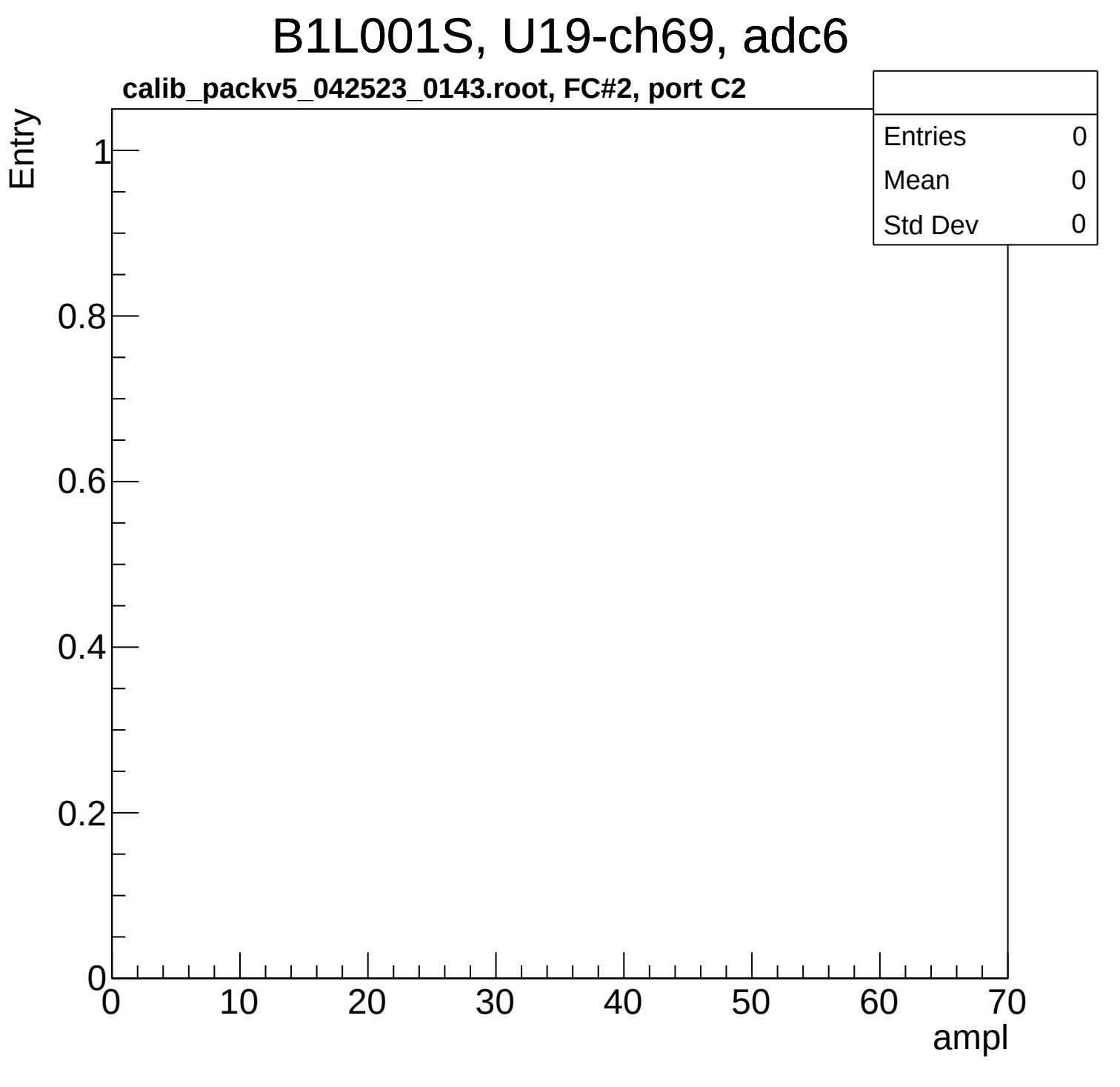
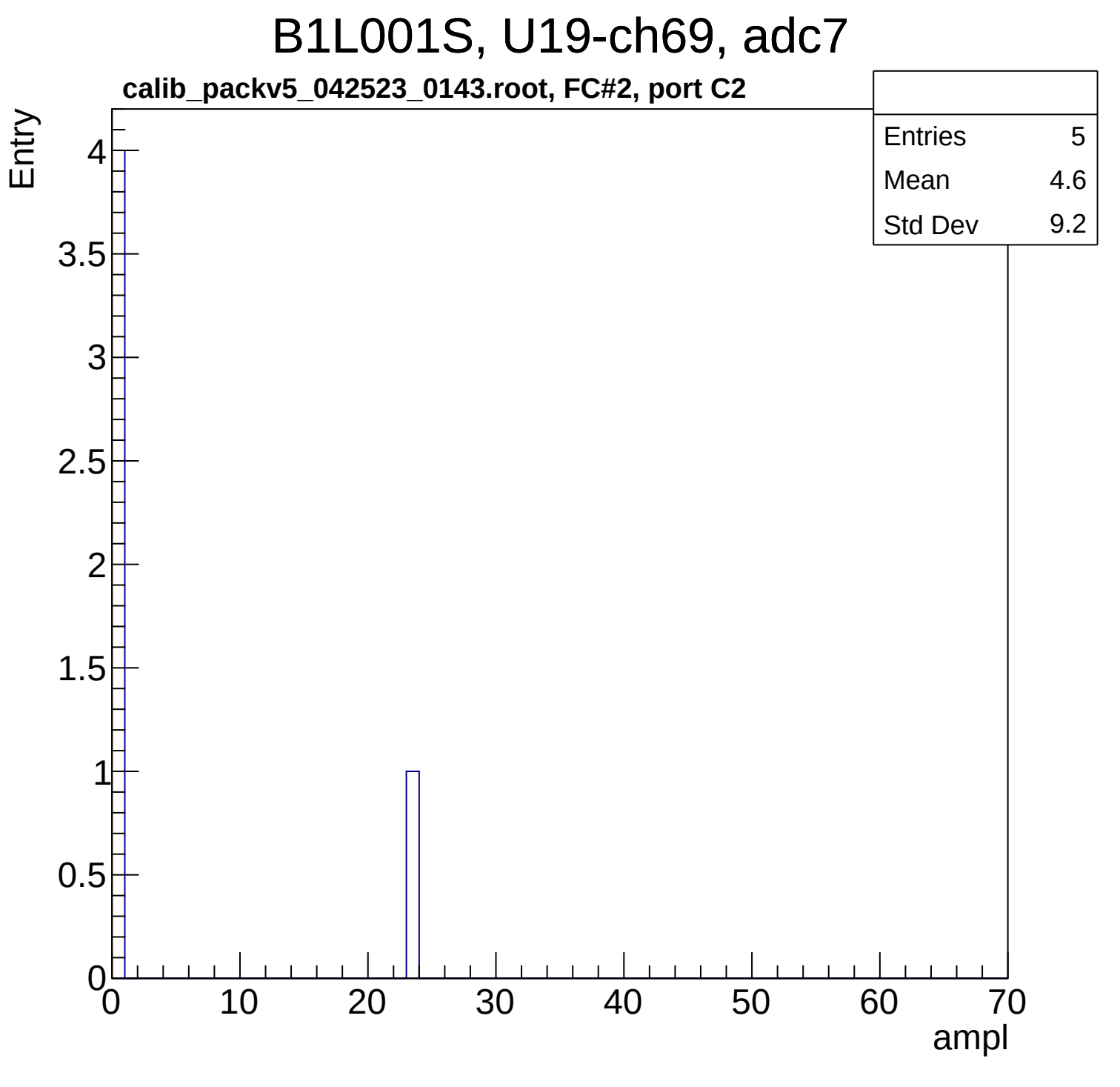

B1L001S, U19-ch69, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch69, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 5
Mean 4.6
Std Dev 9.2
Entry
ampl
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0.5
1
1.5
2
2.5
3
3.5
4
0
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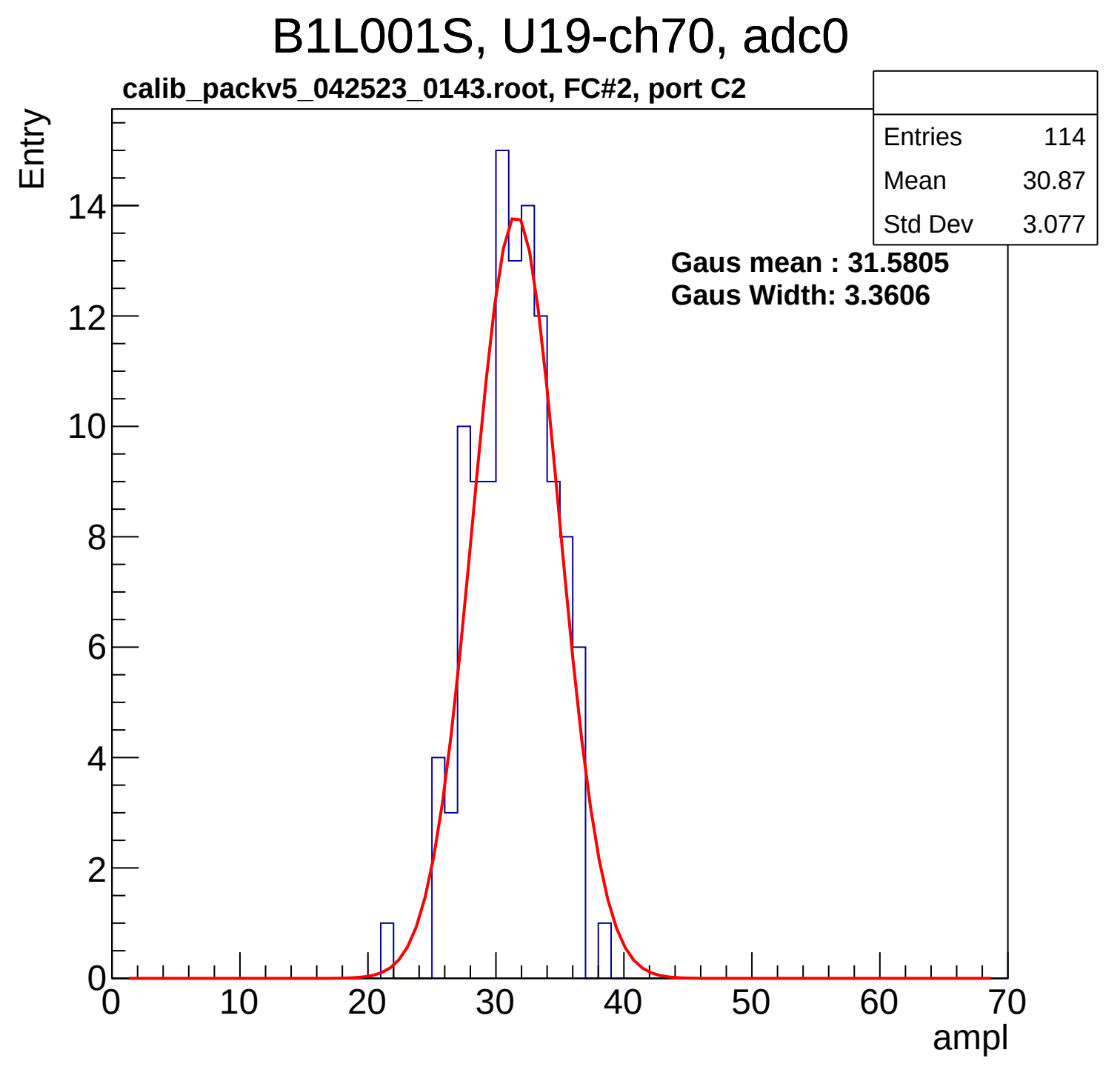
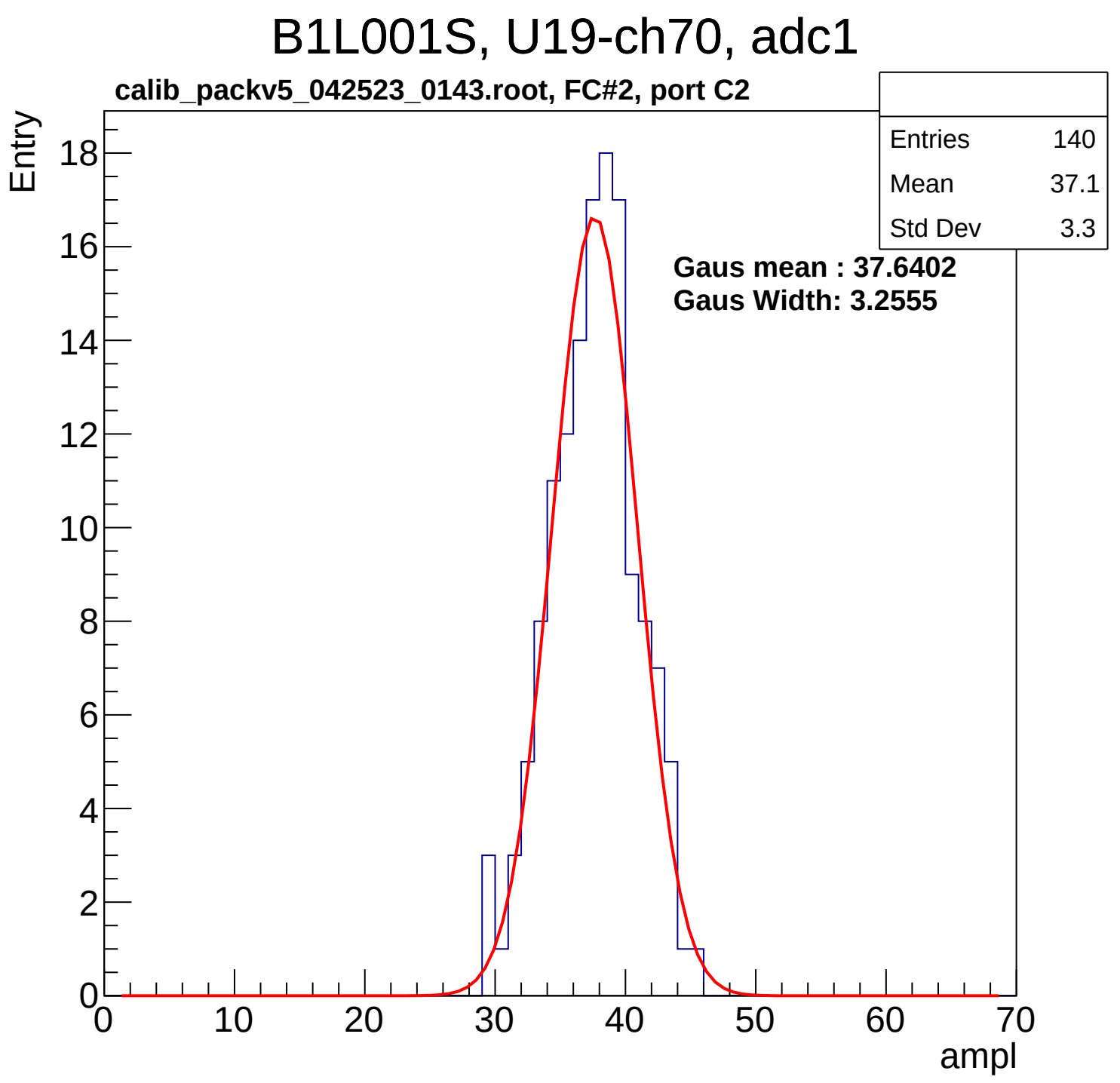
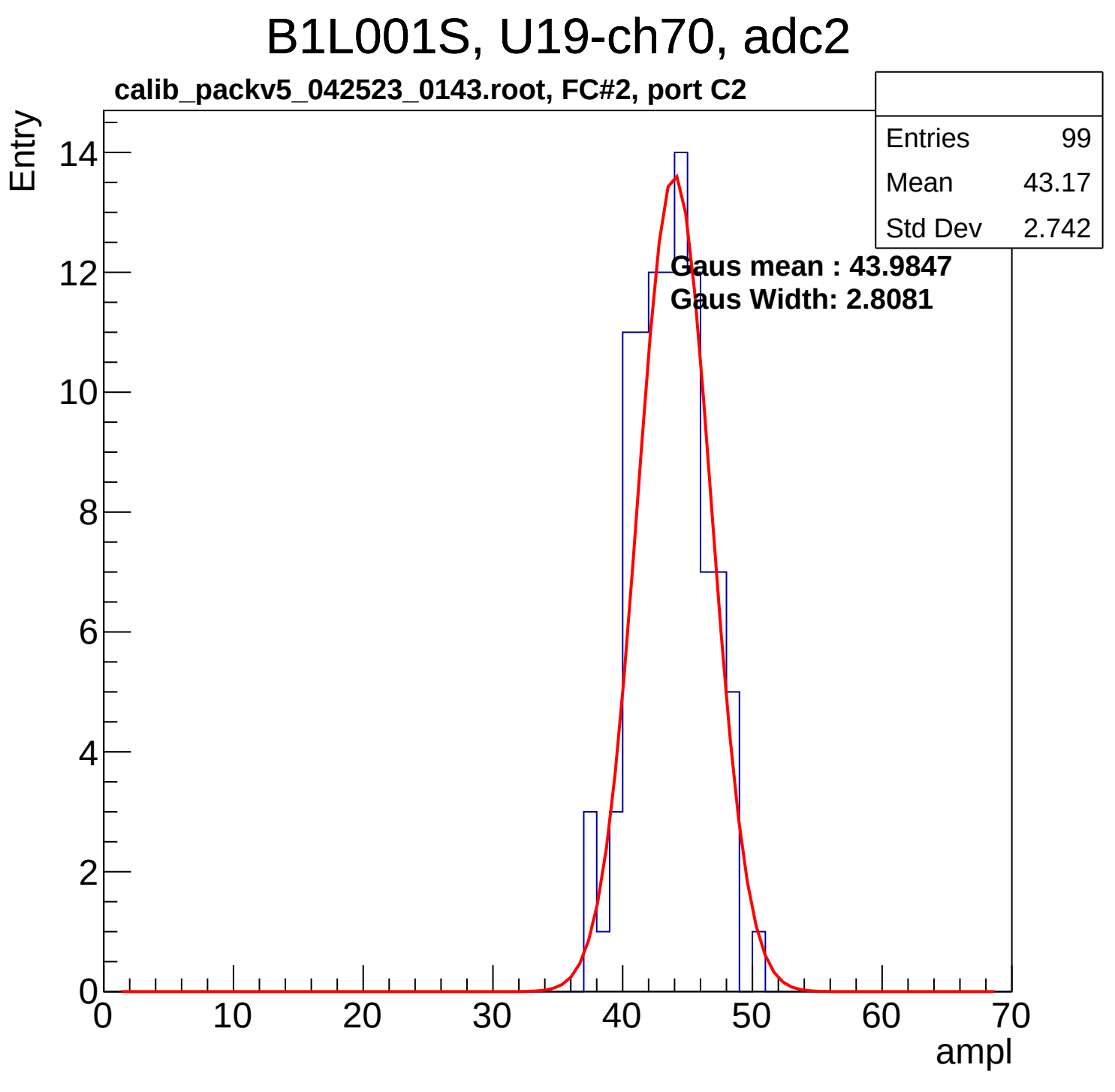
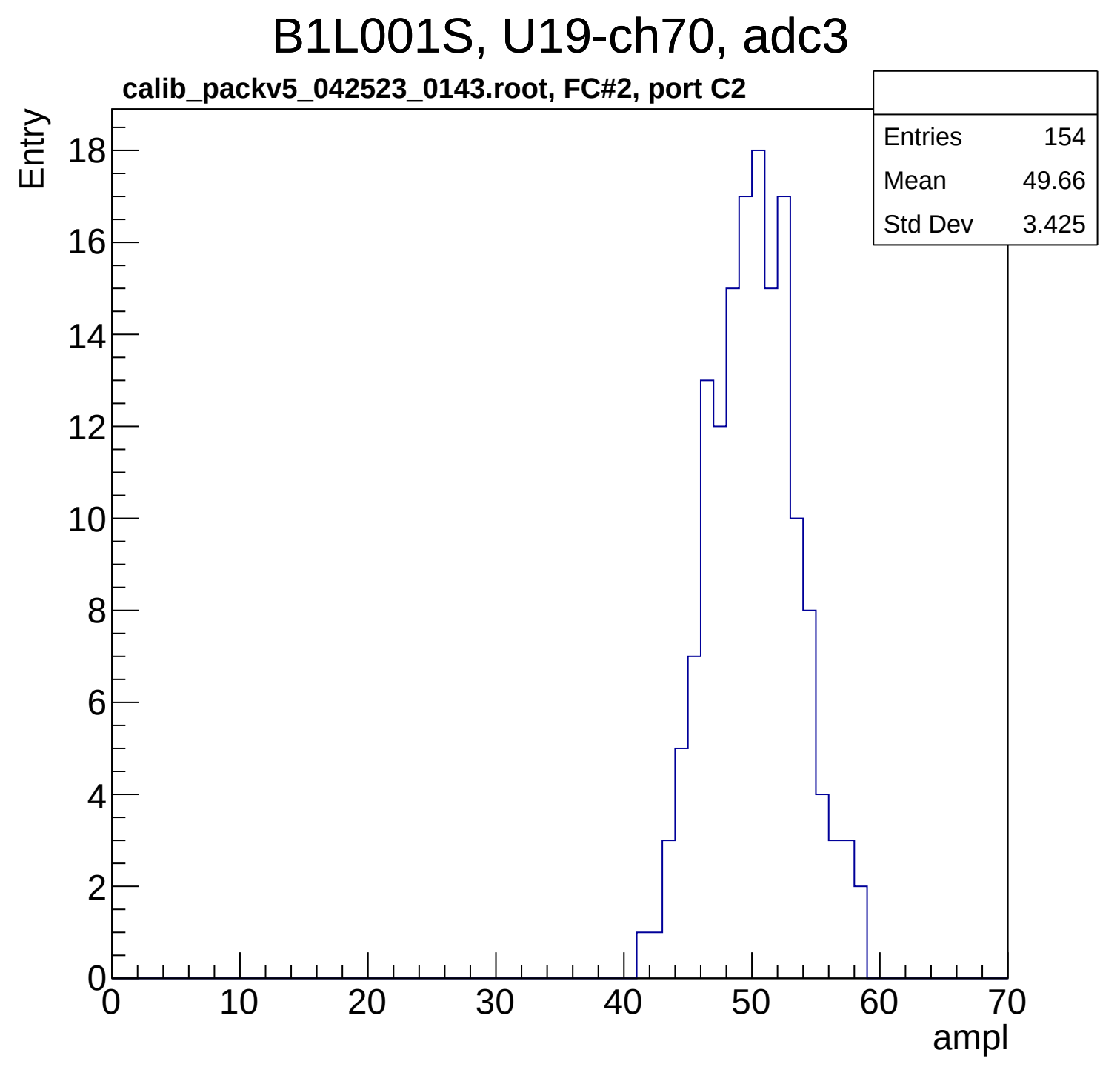
60
70


B1L001S, U19-ch70, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 114
Mean 30.87
Std Dev 3.077
Gaus mean : 31.5805
Gaus Width: 3.3606
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L001S, U19-ch70, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 140
Mean 37.1
Std Dev 3.3
Gaus mean : 37.6402
Gaus Width: 3.2555
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70


B1L001S, U19-ch70, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 99
Mean 43.17
Std Dev 2.742
Gaus mean : 43.9847
Gaus Width: 2.8081
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L001S, U19-ch70, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 154
Mean 49.66
Std Dev 3.425
Entry
0
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4
6
8
10
12
14
16
18
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10
20
30
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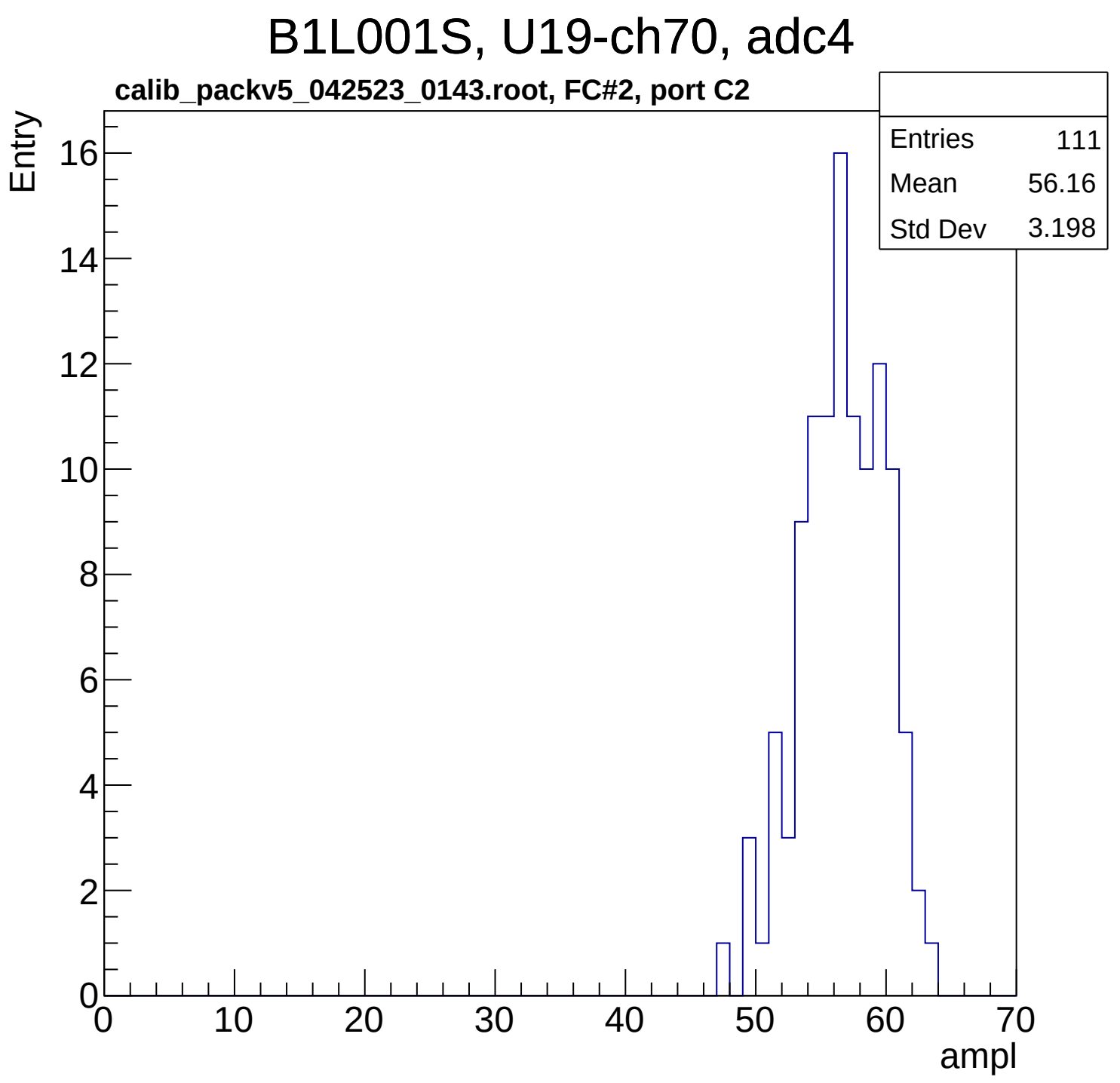
50
60
70
ampl


B1L001S, U19-ch70, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 111
Mean 56.16
Std Dev 3.198
Entry
0
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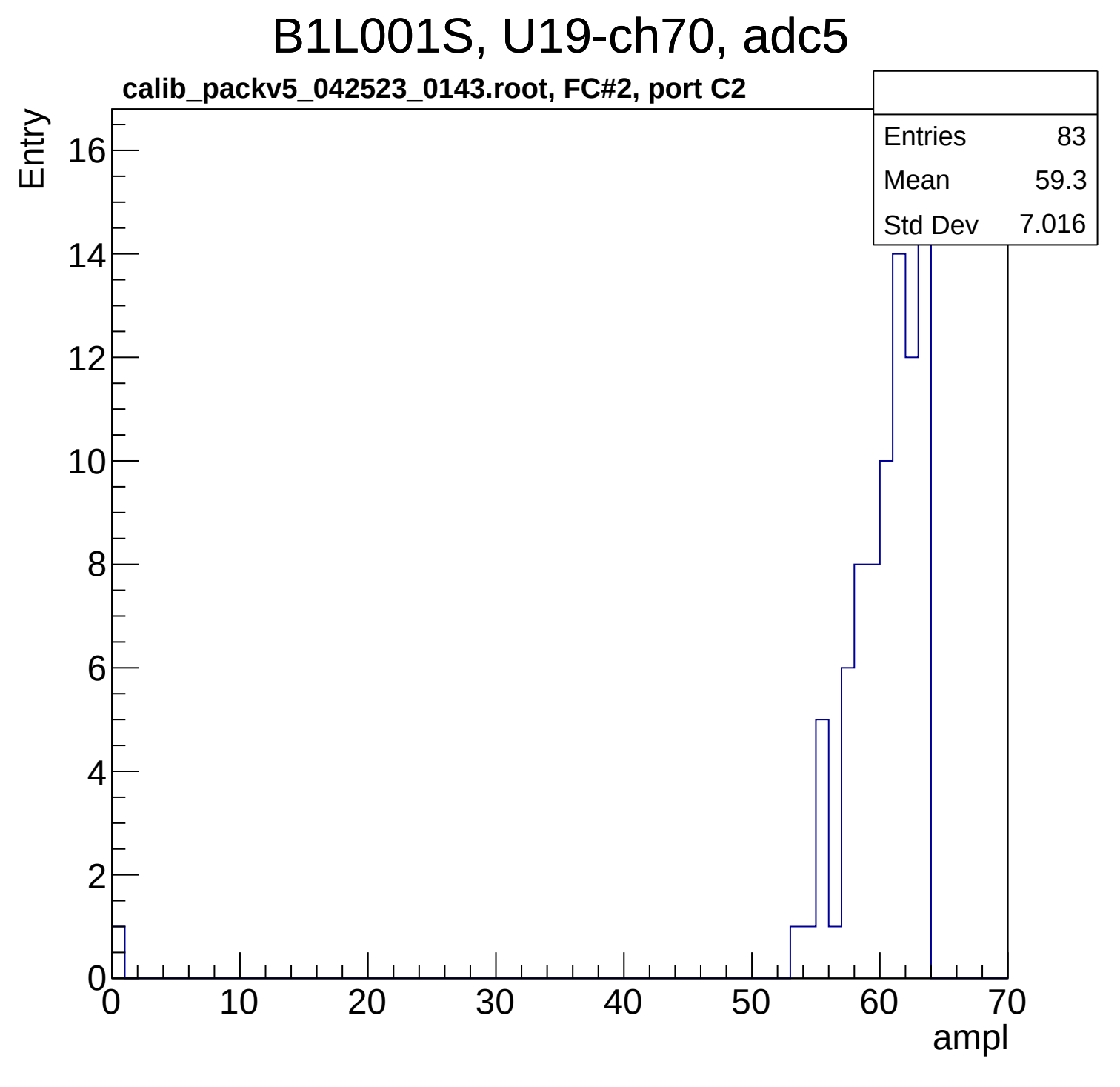
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch70, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 83
Mean 59.3
Std Dev 7.016
Entry
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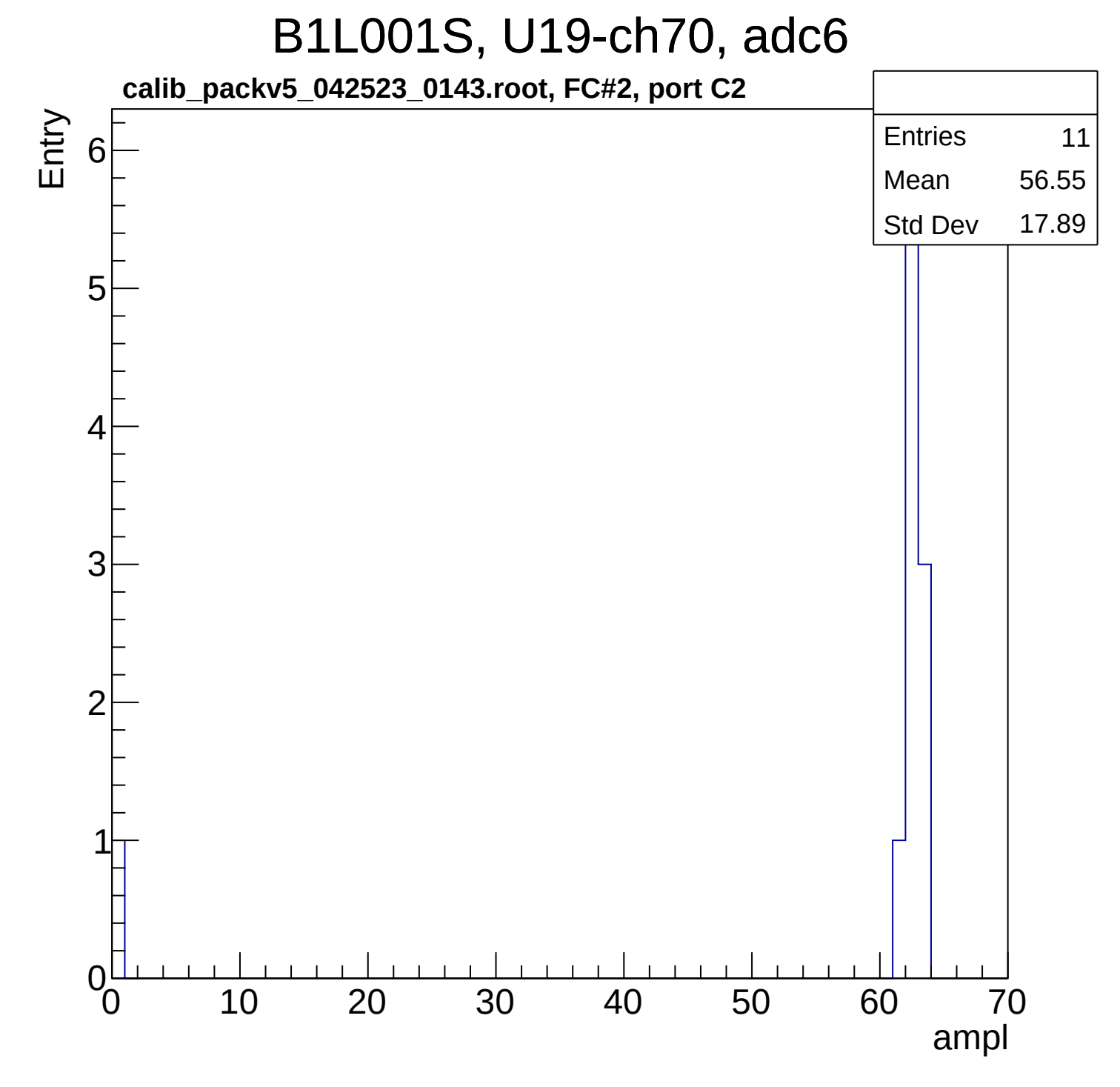
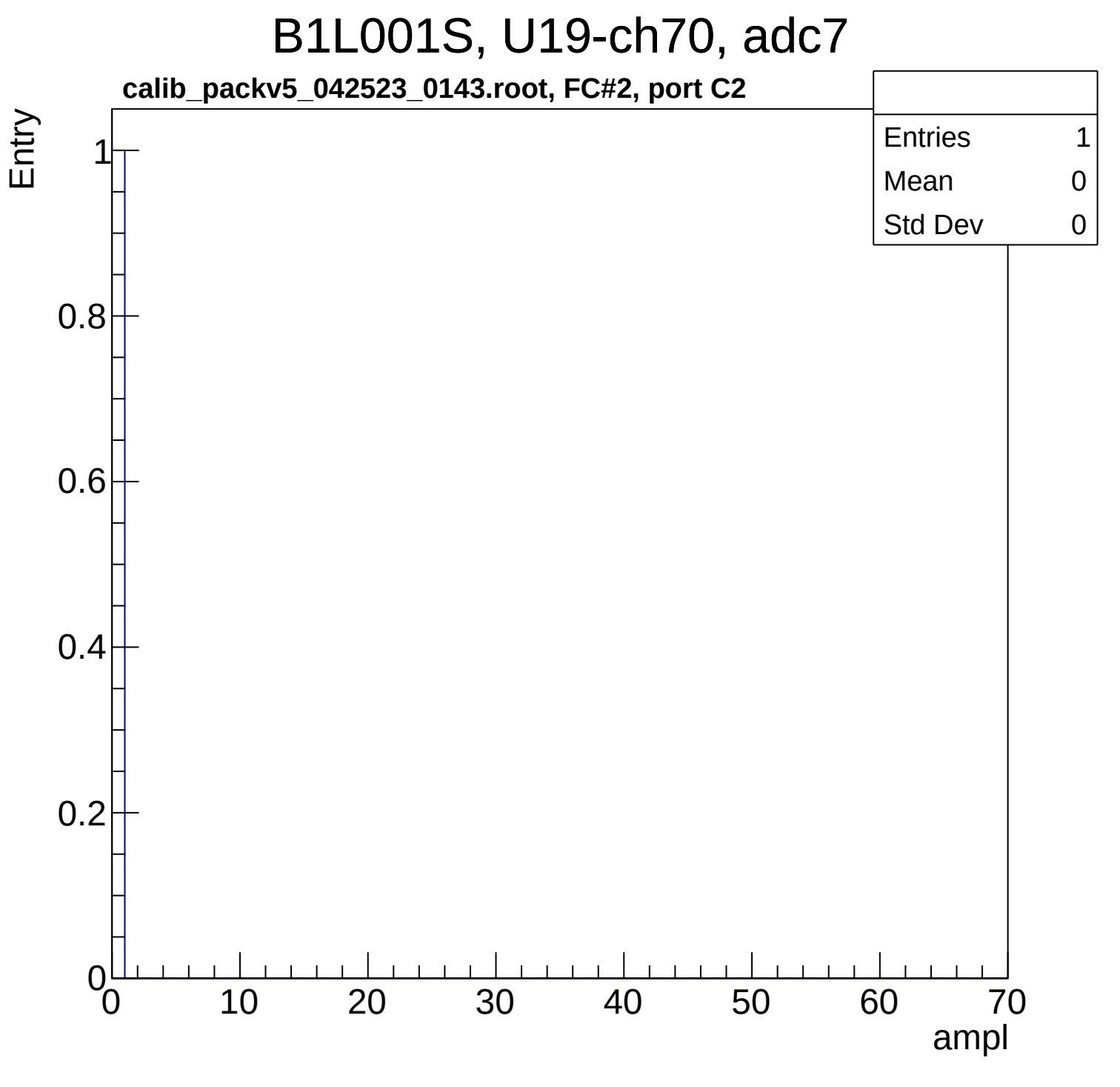
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch70, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 11
Mean 56.55
Std Dev 17.89
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch70, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 0
Std Dev 0
Entry
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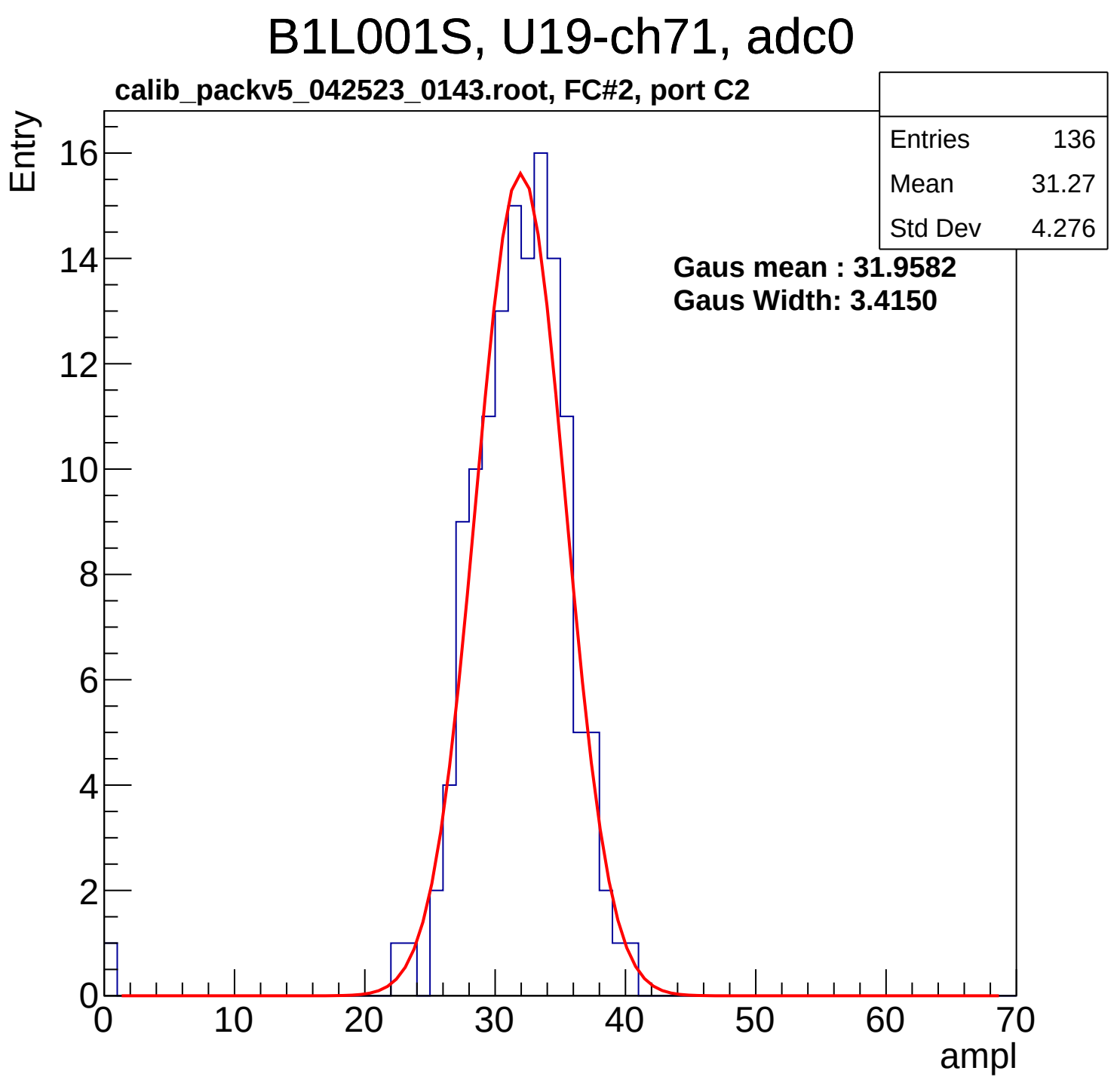
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch71, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 136
Mean 31.27
Std Dev 4.276
Gaus mean : 31.9582
Gaus Width: 3.4150
Entry
ampl
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2
4
6
8
10
12
14
16
0
10
20
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40
50
60
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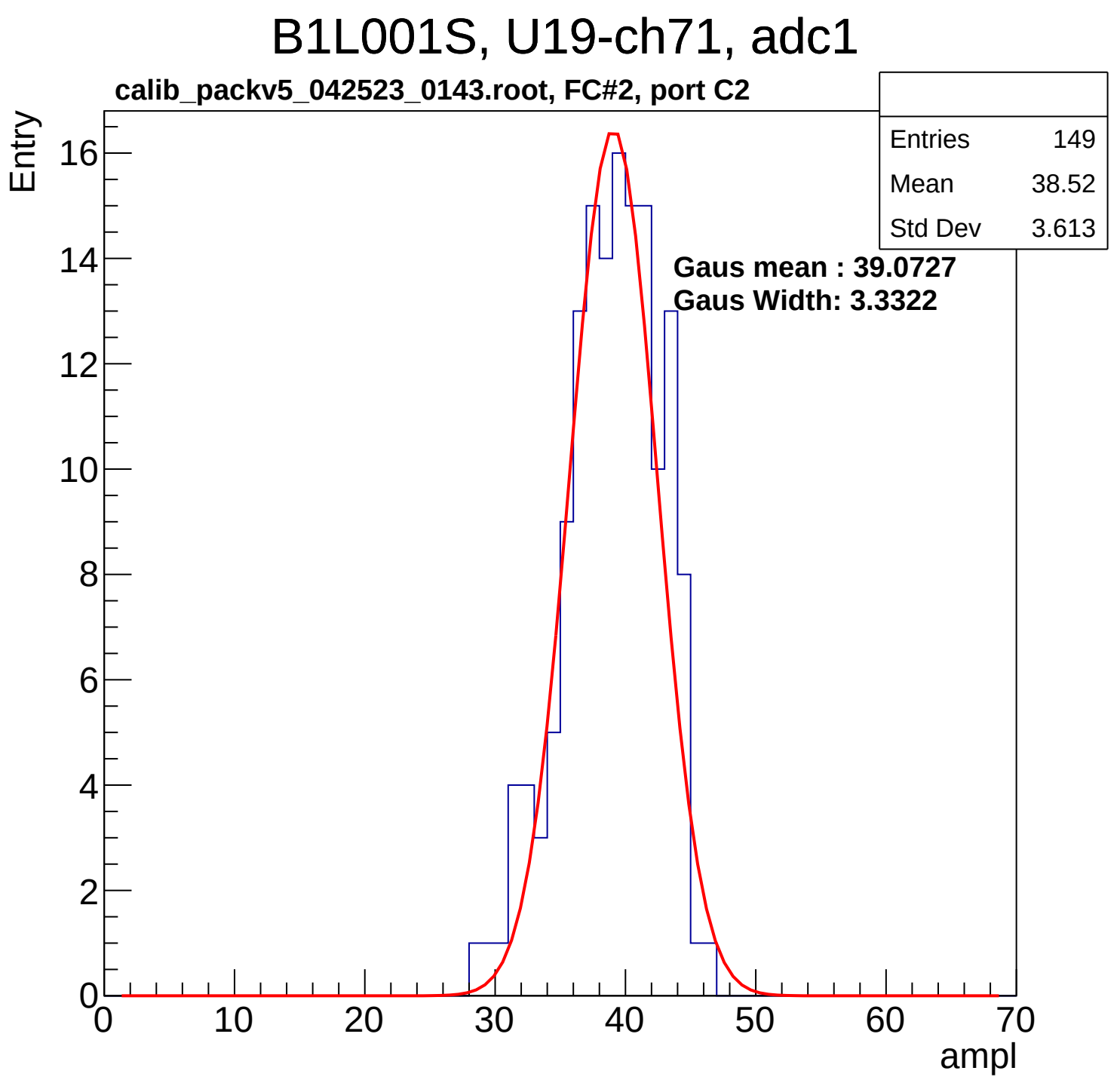
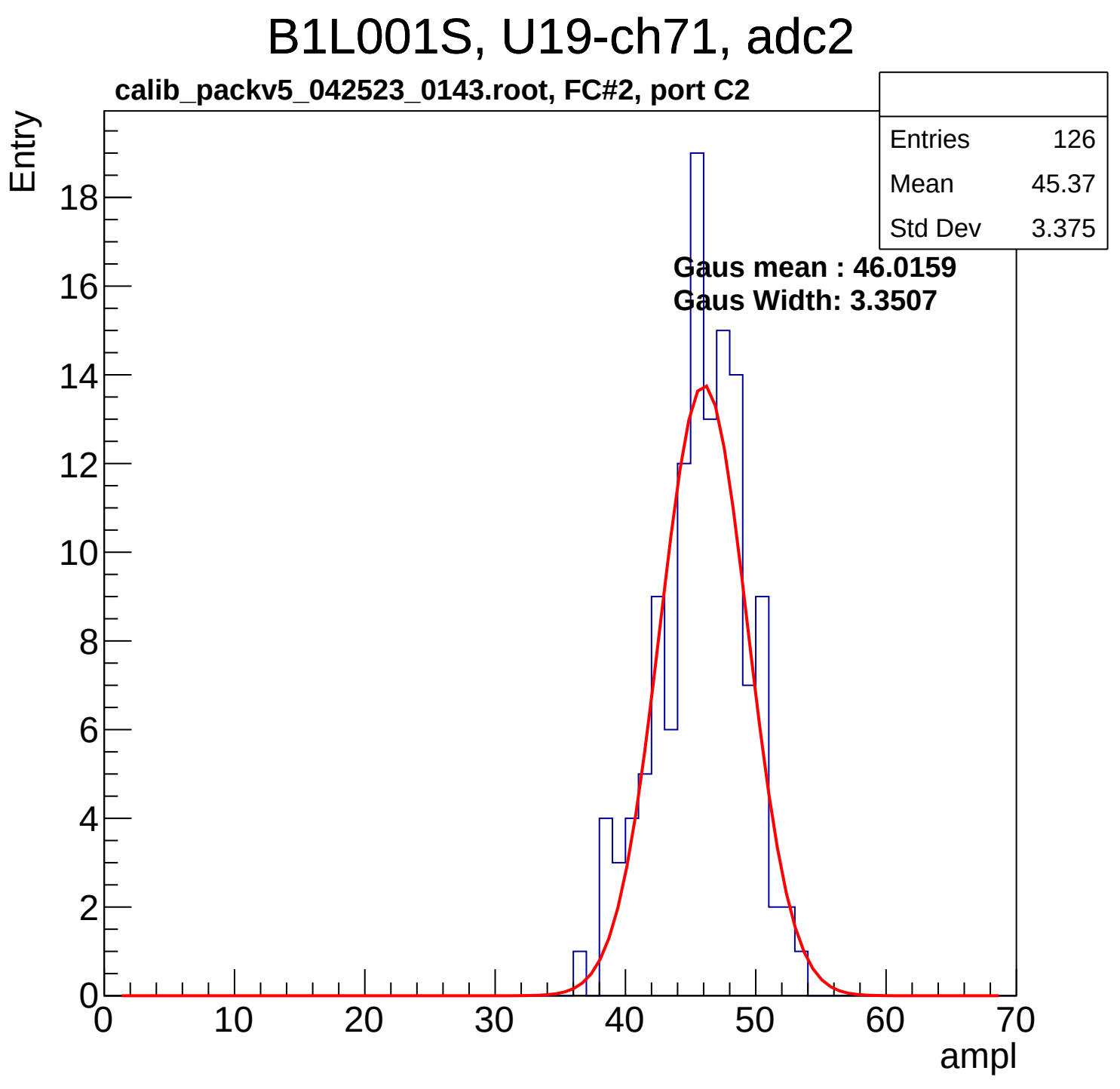

B1L001S, U19-ch71, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 149
Mean 38.52
Std Dev 3.613
Gaus mean : 39.0727
Gaus Width: 3.3322
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70


B1L001S, U19-ch71, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 126
Mean 45.37
Std Dev 3.375
Gaus mean : 46.0159
Gaus Width: 3.3507
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
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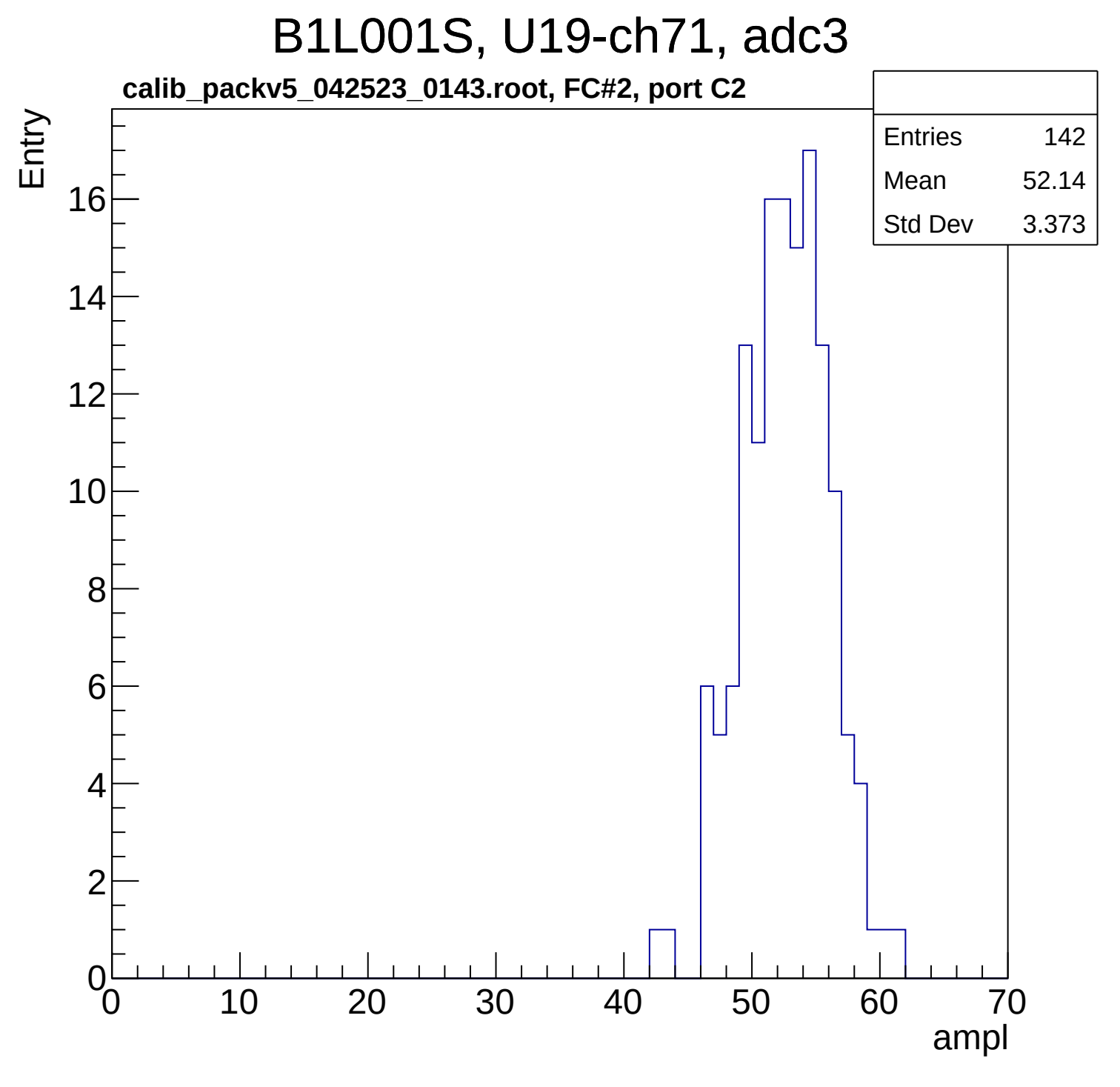
B1L001S, U19-ch71, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 142
Mean 52.14
Std Dev 3.373
Entry
ampl
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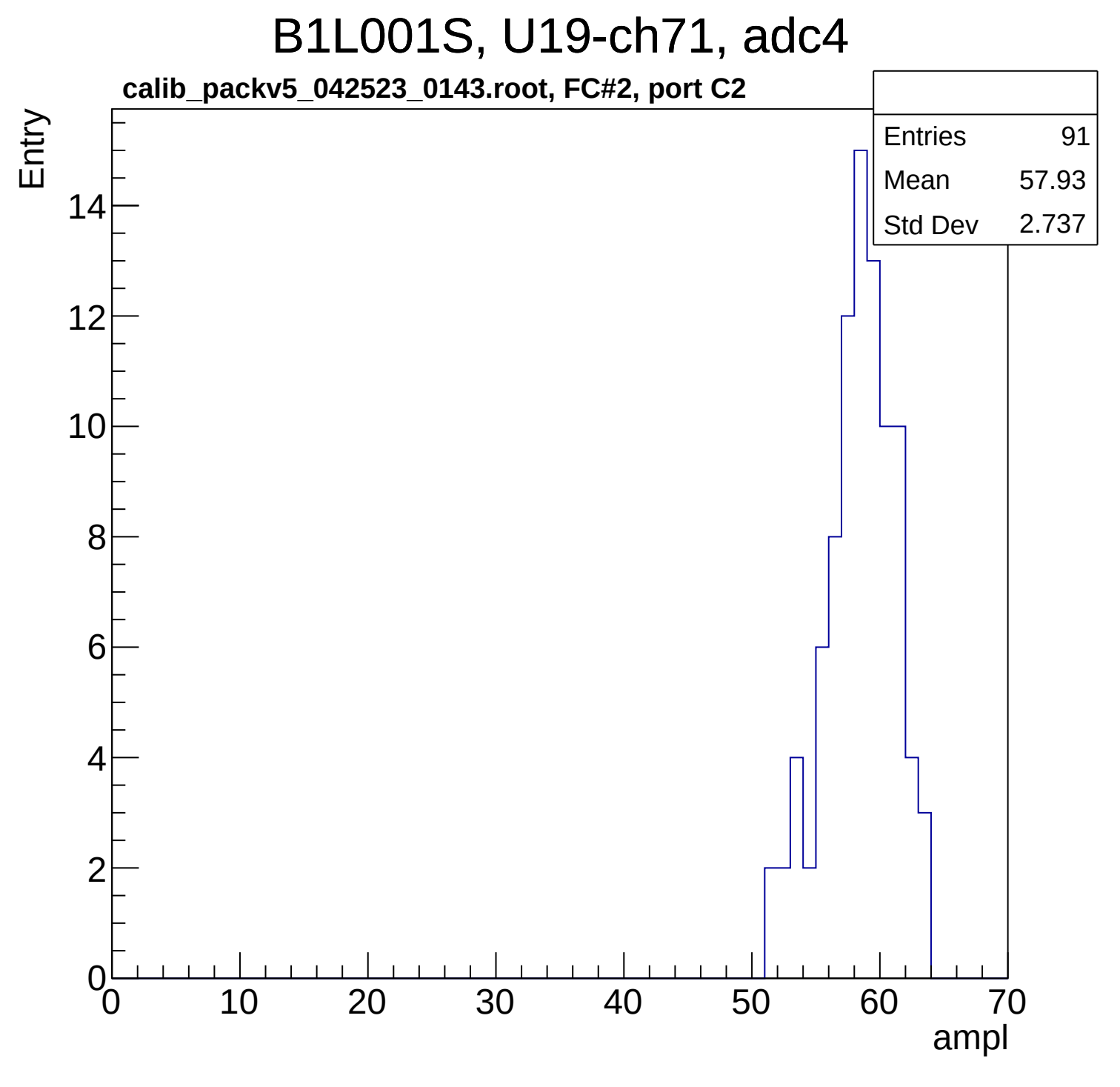
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70


B1L001S, U19-ch71, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 91
Mean 57.93
Std Dev 2.737
Entry
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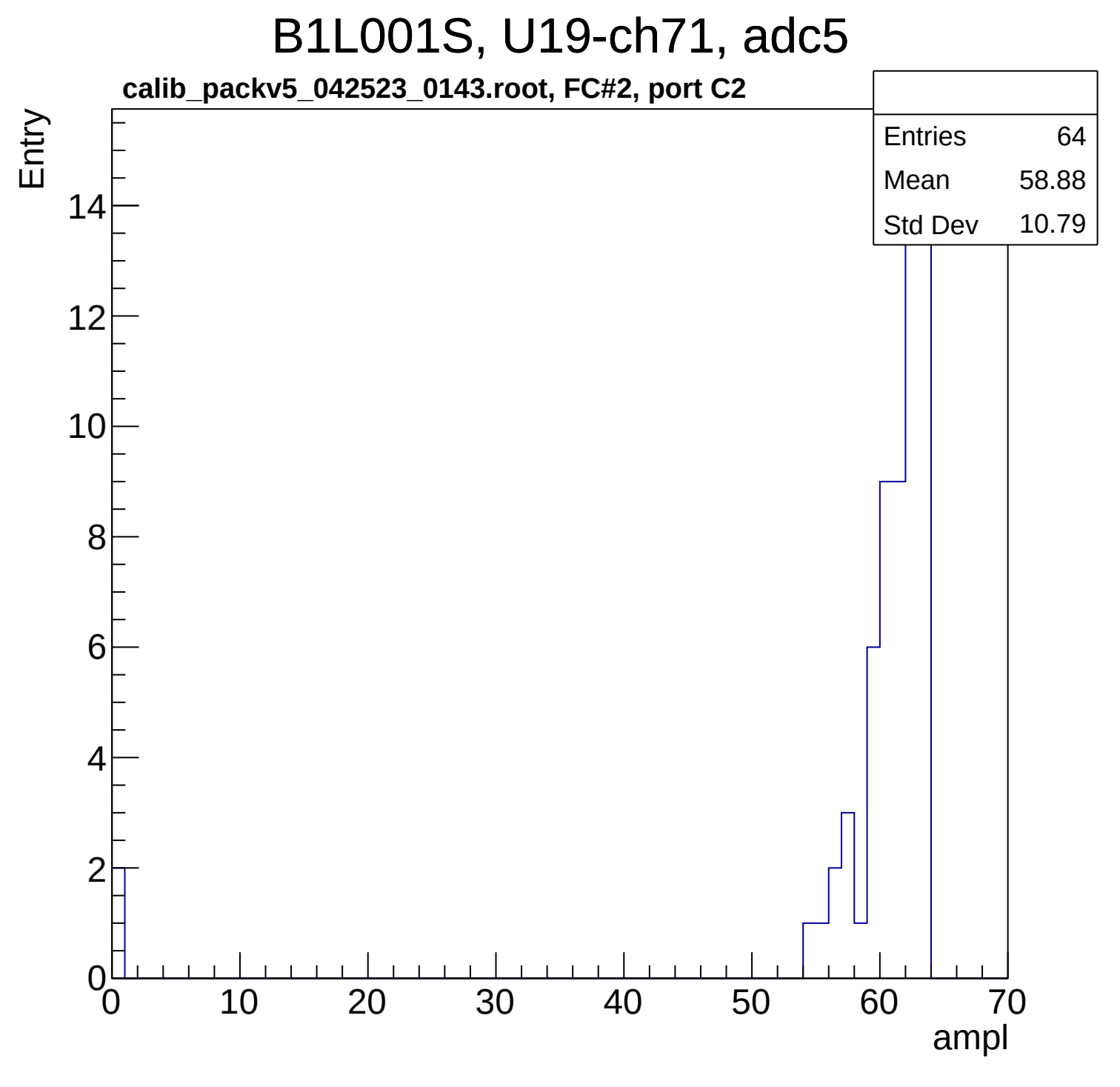
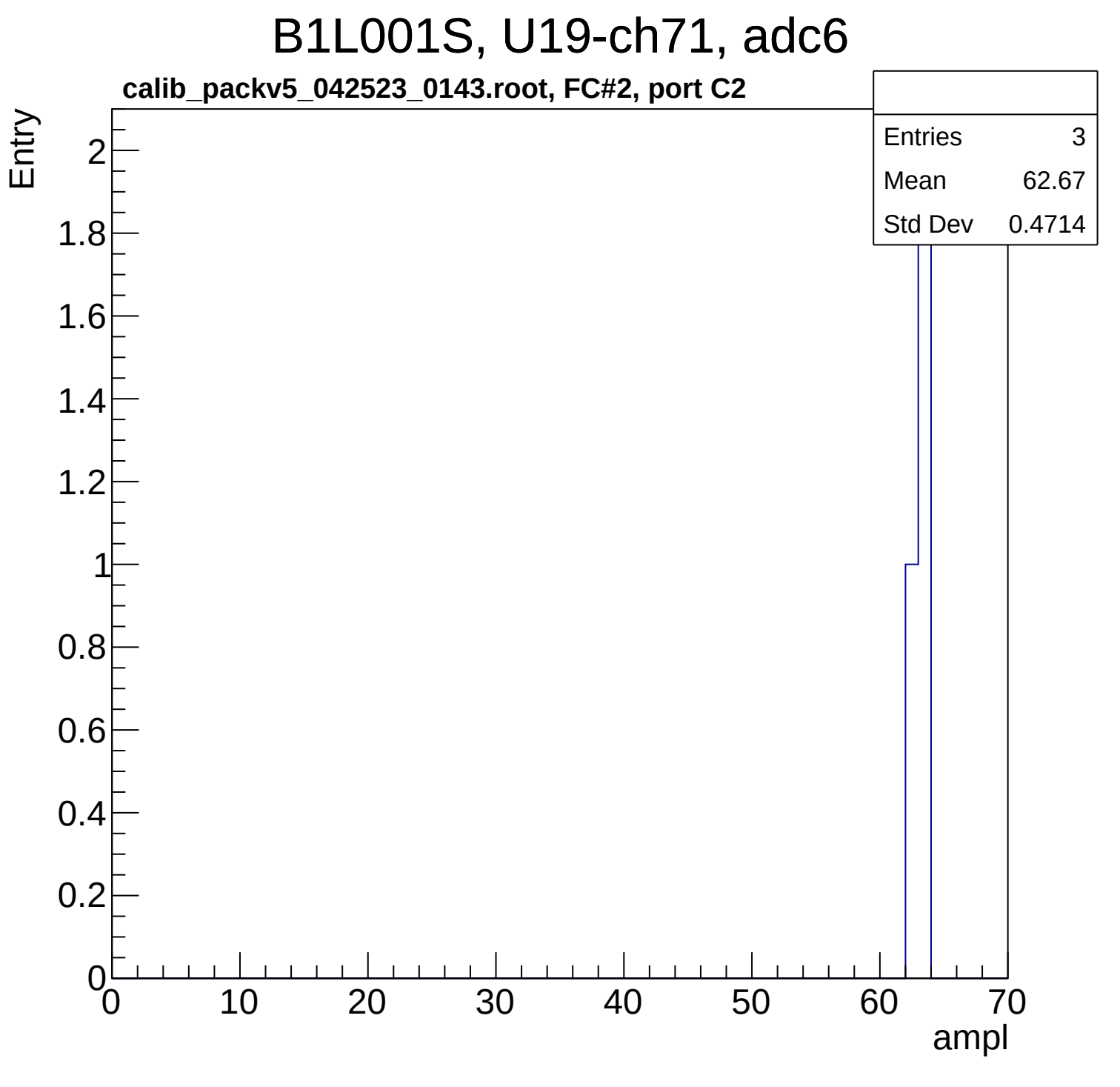
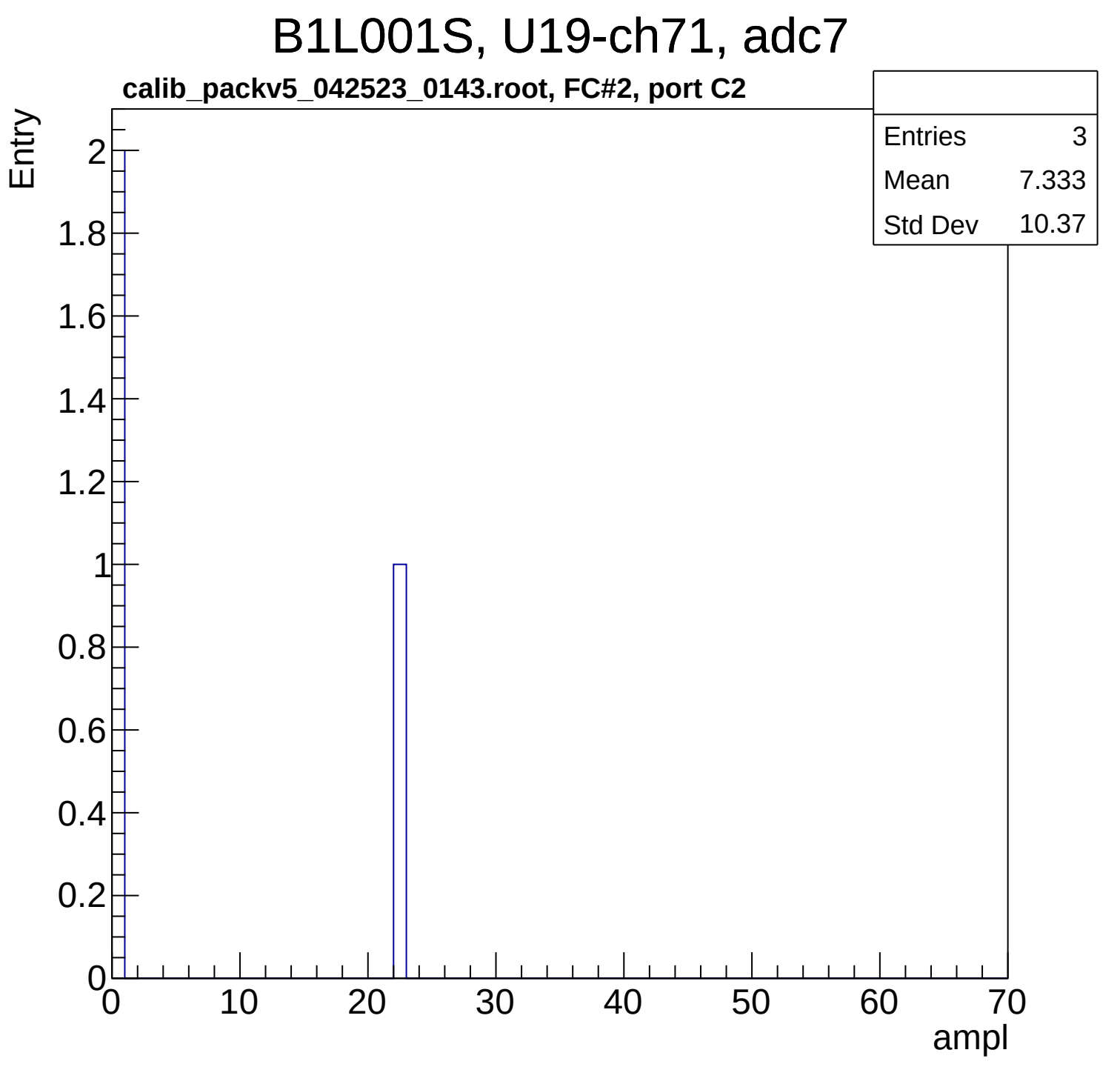
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch71, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 64
Mean 58.88
Std Dev 10.79
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch71, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 3
Mean 62.67
Std Dev 0.4714
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L001S, U19-ch71, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 3
Mean 7.333
Std Dev 10.37
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
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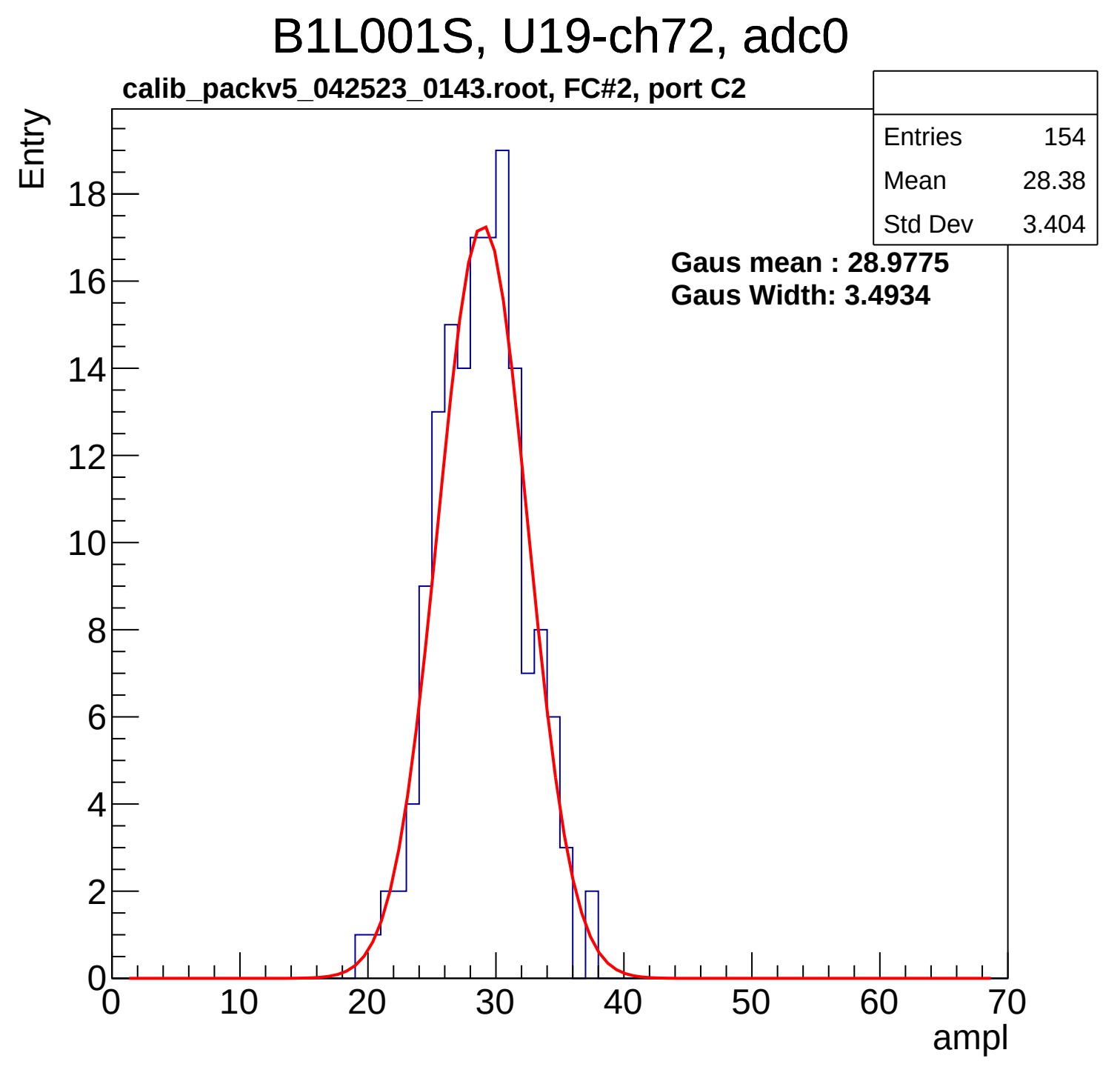
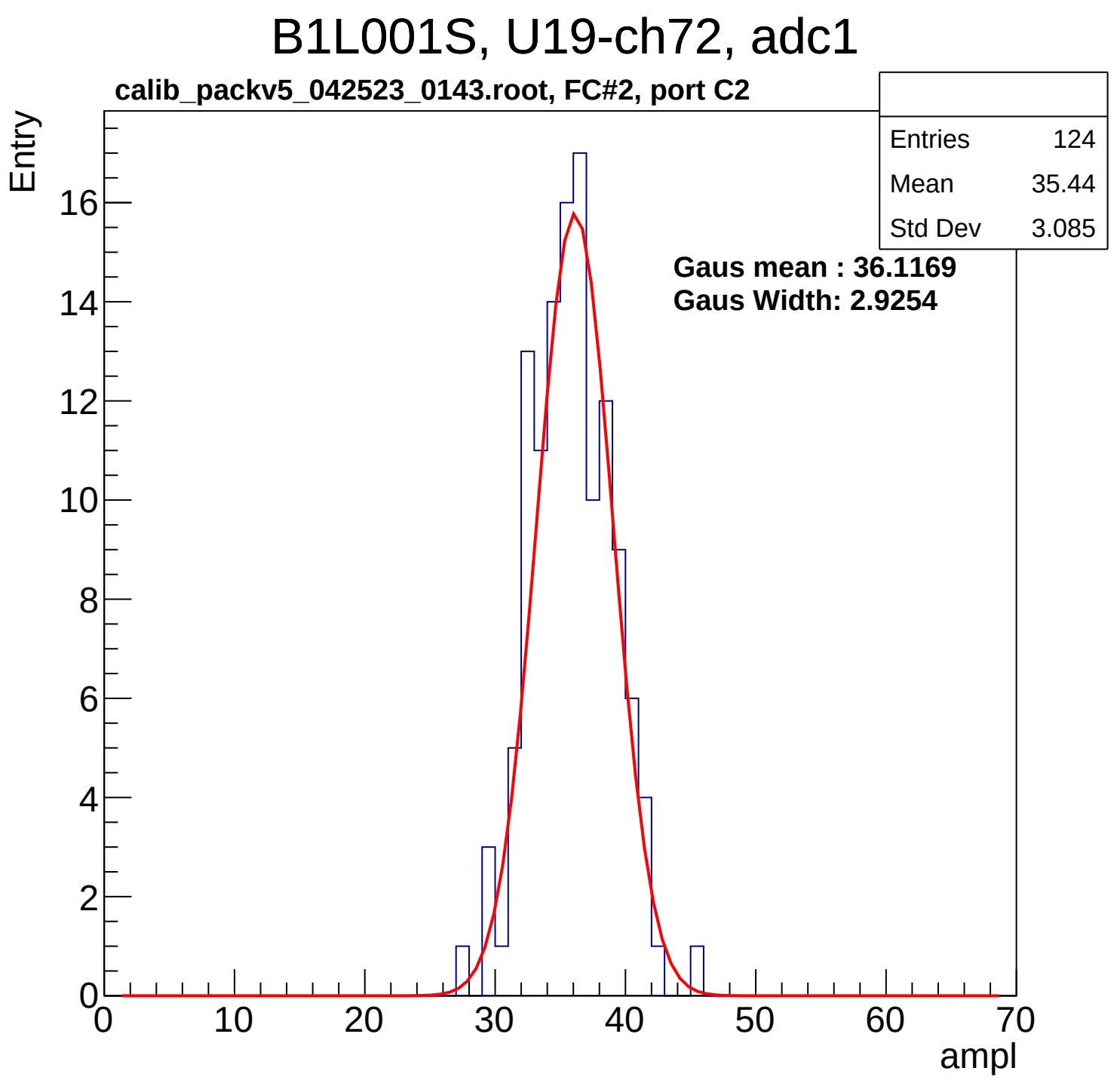
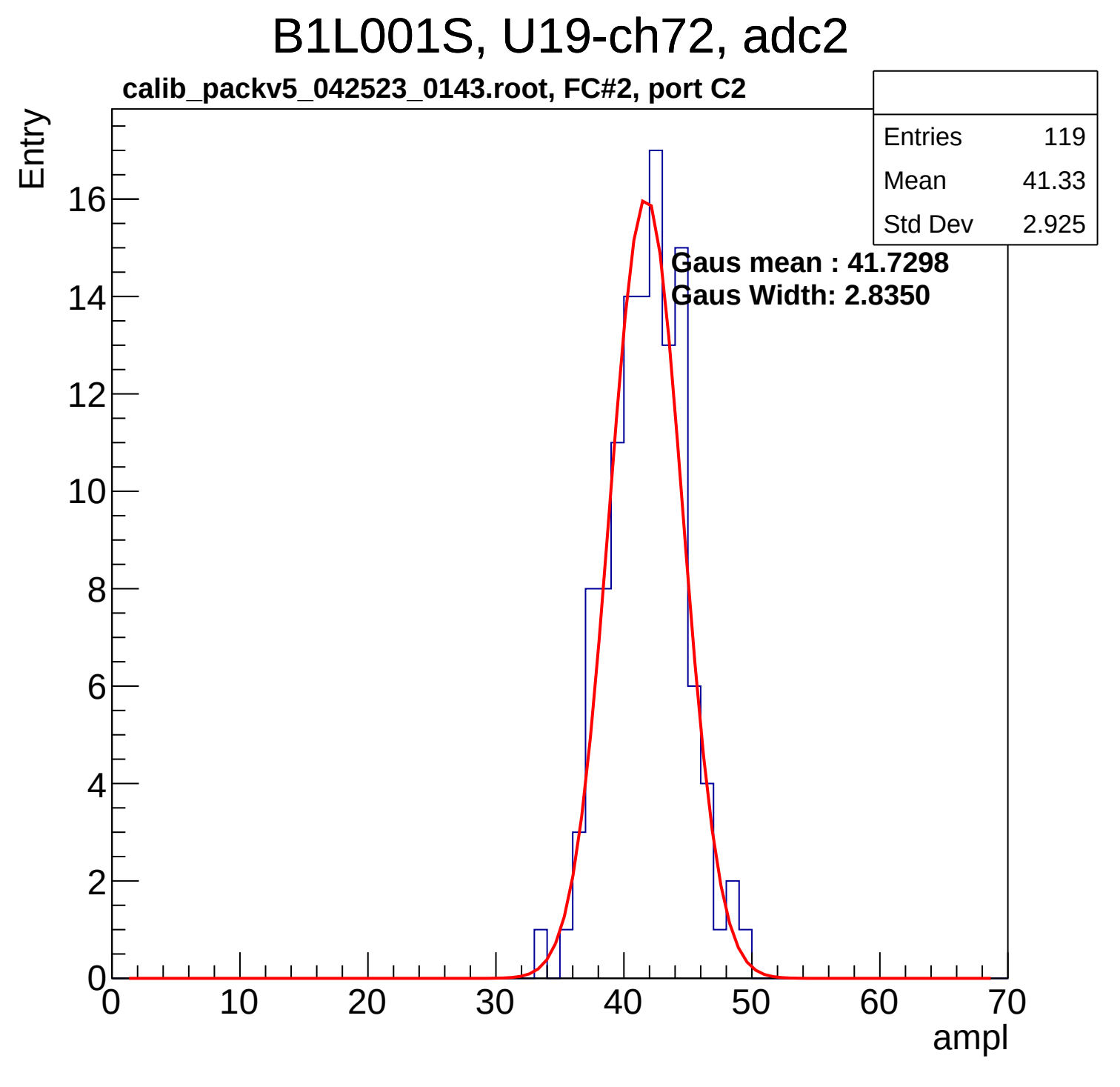
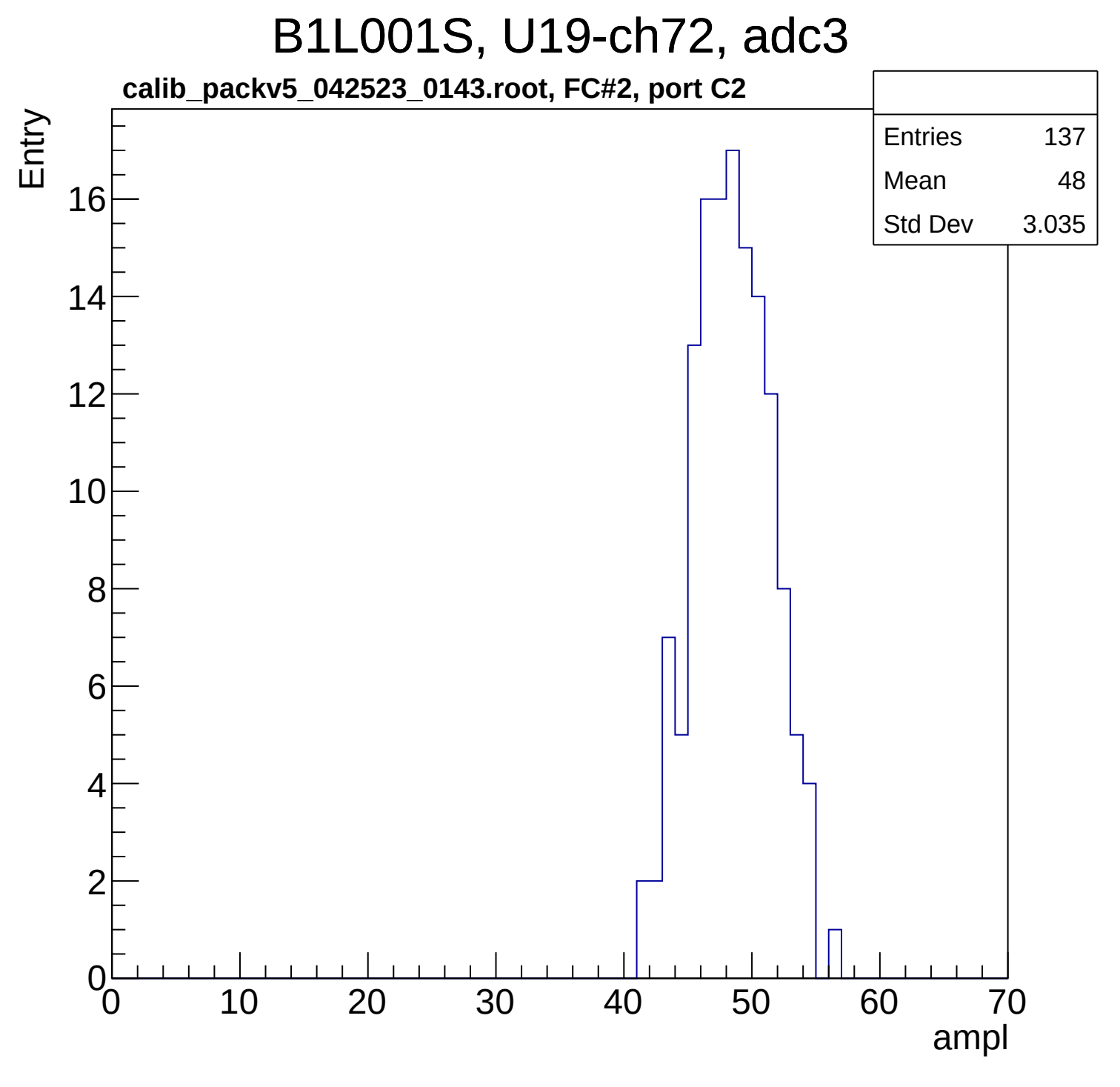
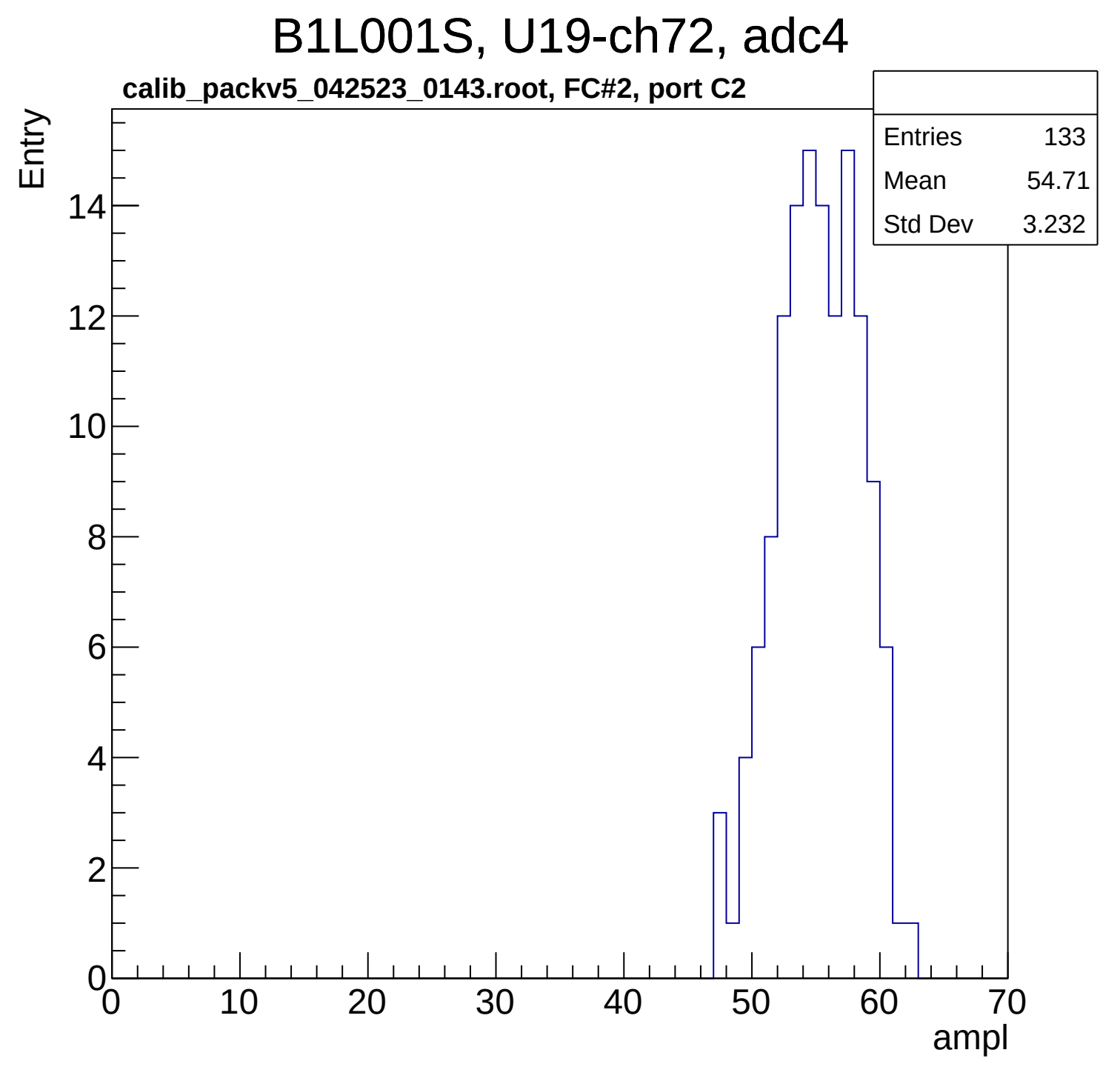
40
50
60
70


B1L001S, U19-ch72, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 154
Mean 28.38
Std Dev 3.404
Gaus mean : 28.9775
Gaus Width: 3.4934
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70


B1L001S, U19-ch72, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 124
Mean 35.44
Std Dev 3.085
Gaus mean : 36.1169
Gaus Width: 2.9254
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70


B1L001S, U19-ch72, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 119
Mean 41.33
Std Dev 2.925
Gaus mean : 41.7298
Gaus Width: 2.8350
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70


B1L001S, U19-ch72, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 137
Mean 48
Std Dev 3.035
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70


B1L001S, U19-ch72, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 133
Mean 54.71
Std Dev 3.232
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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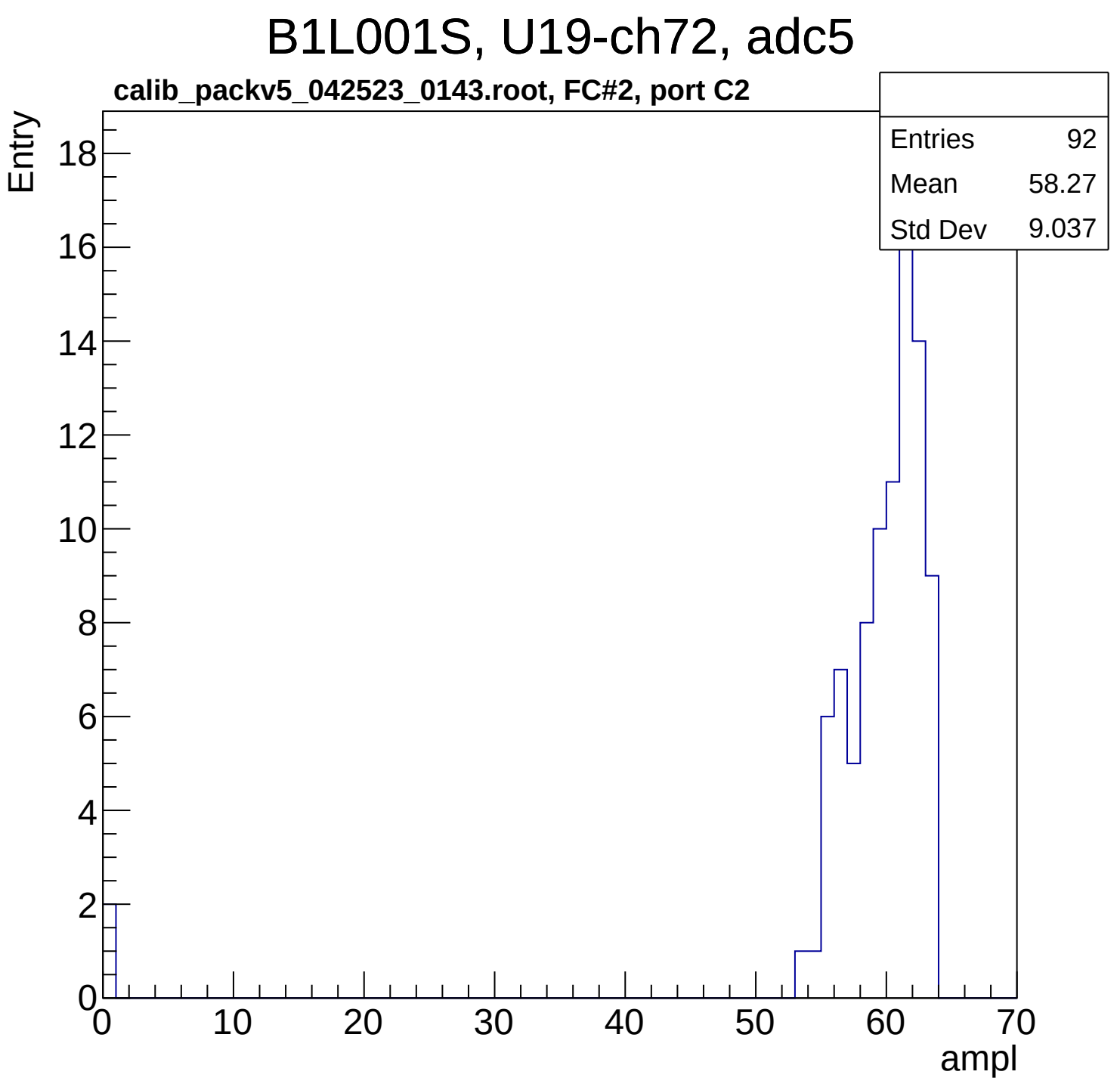
B1L001S, U19-ch72, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 92
Mean 58.27
Std Dev 9.037
Entry
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6
8
10
12
14
16
18
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10
20
30
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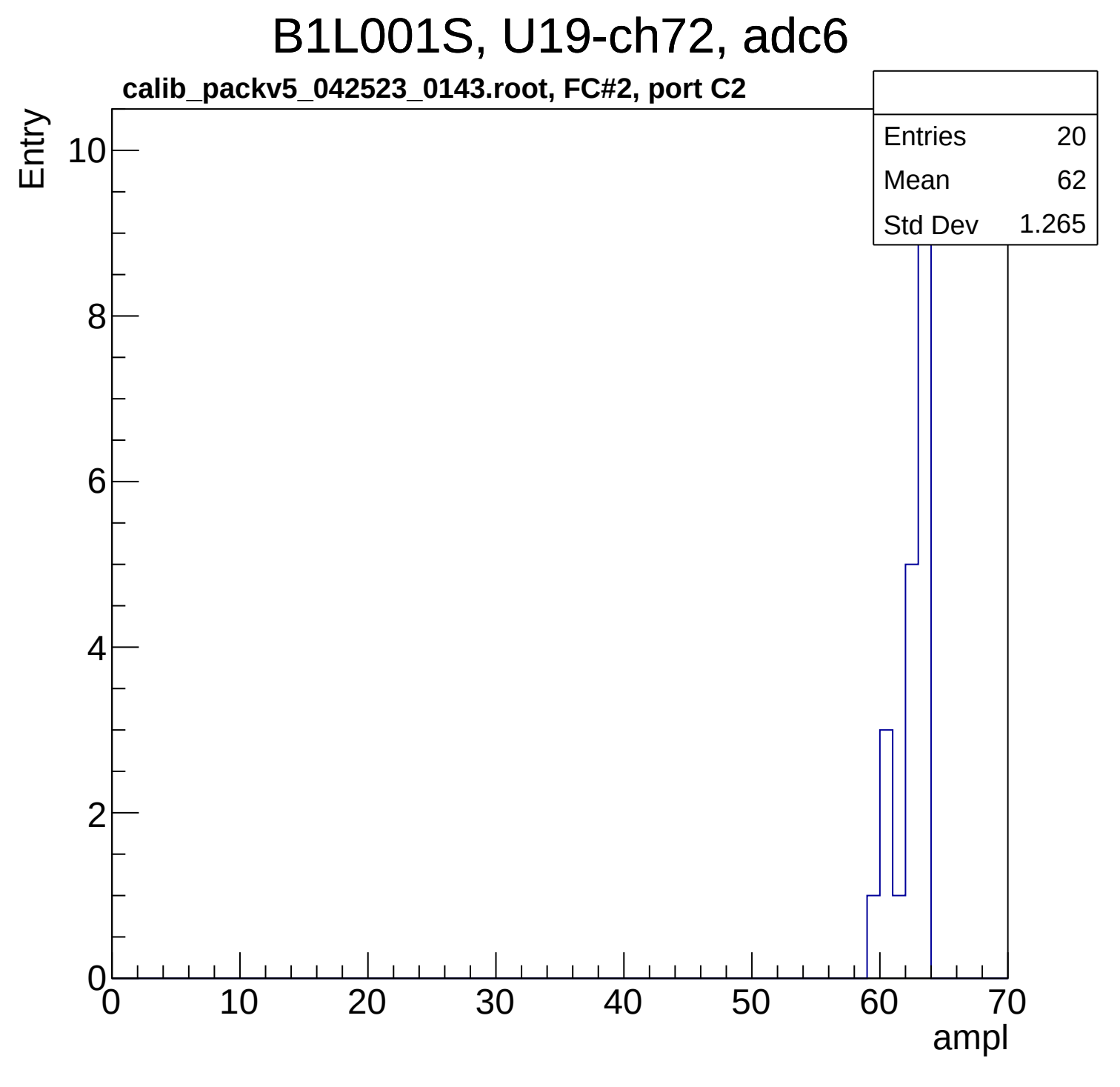
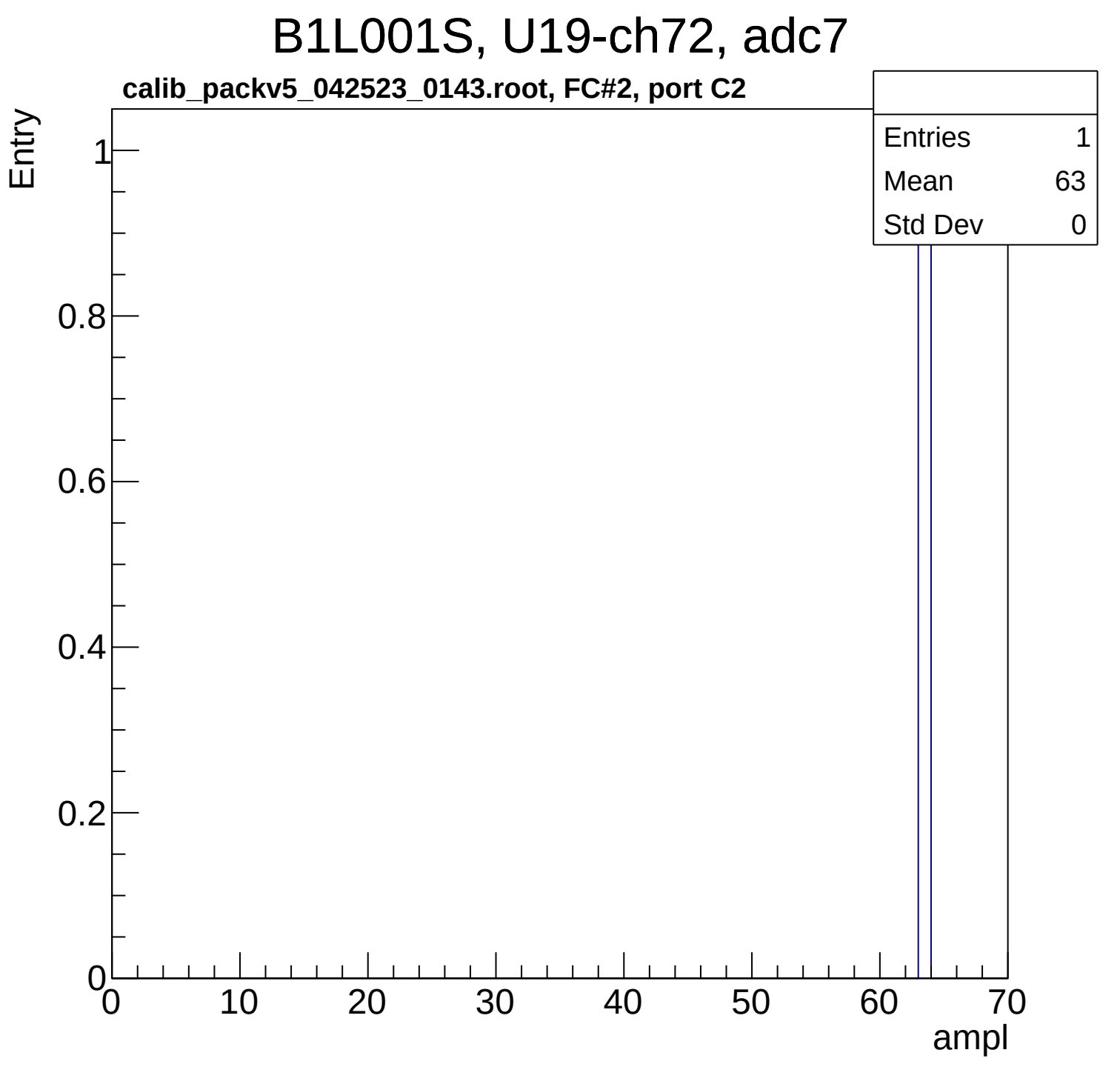
50
60
70
ampl


B1L001S, U19-ch72, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 20
Mean 62
Std Dev 1.265
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch72, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 63
Std Dev 0
Entry
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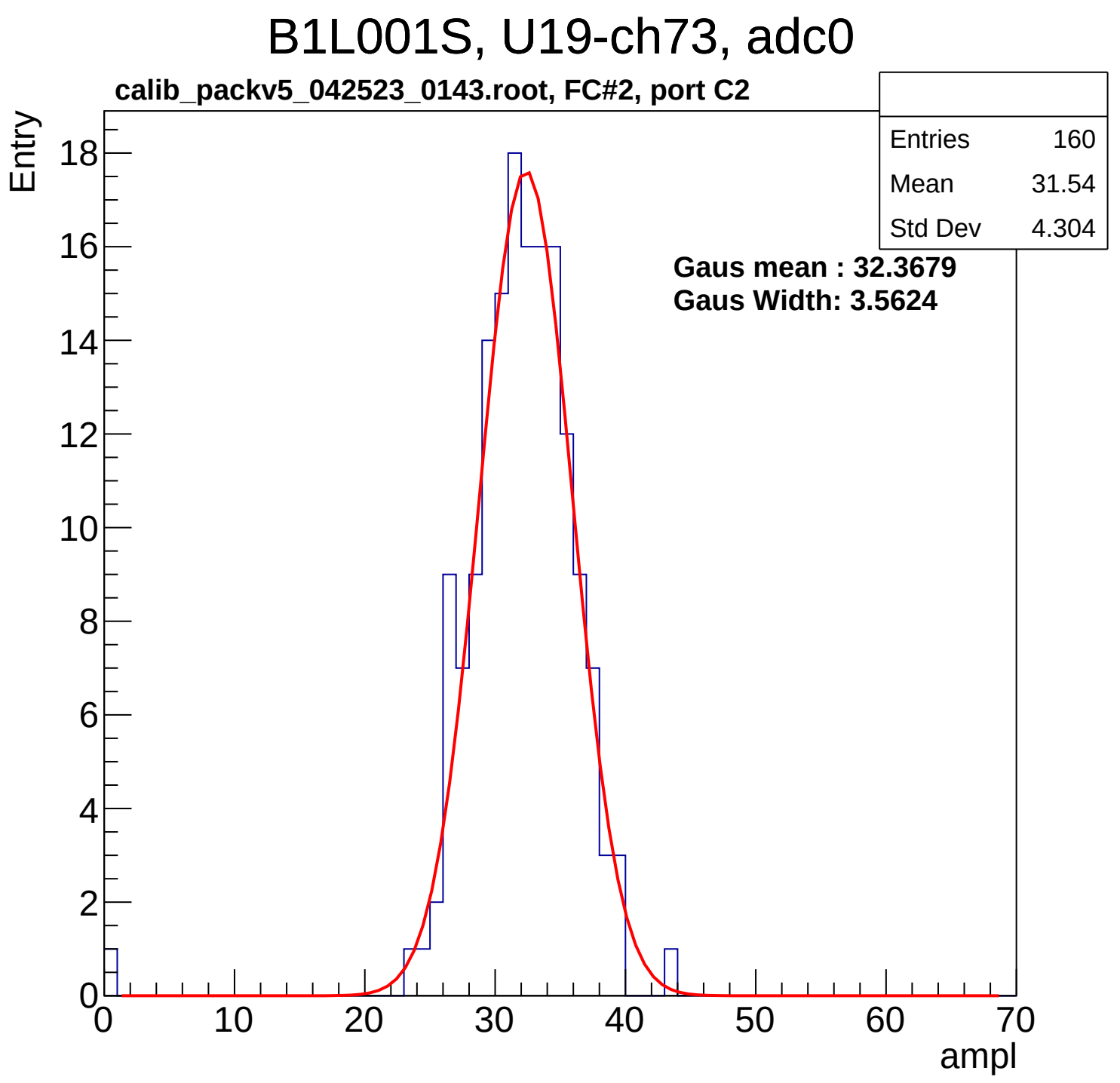
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch73, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 160
Mean 31.54
Std Dev 4.304
Gaus mean : 32.3679
Gaus Width: 3.5624
Entry
ampl
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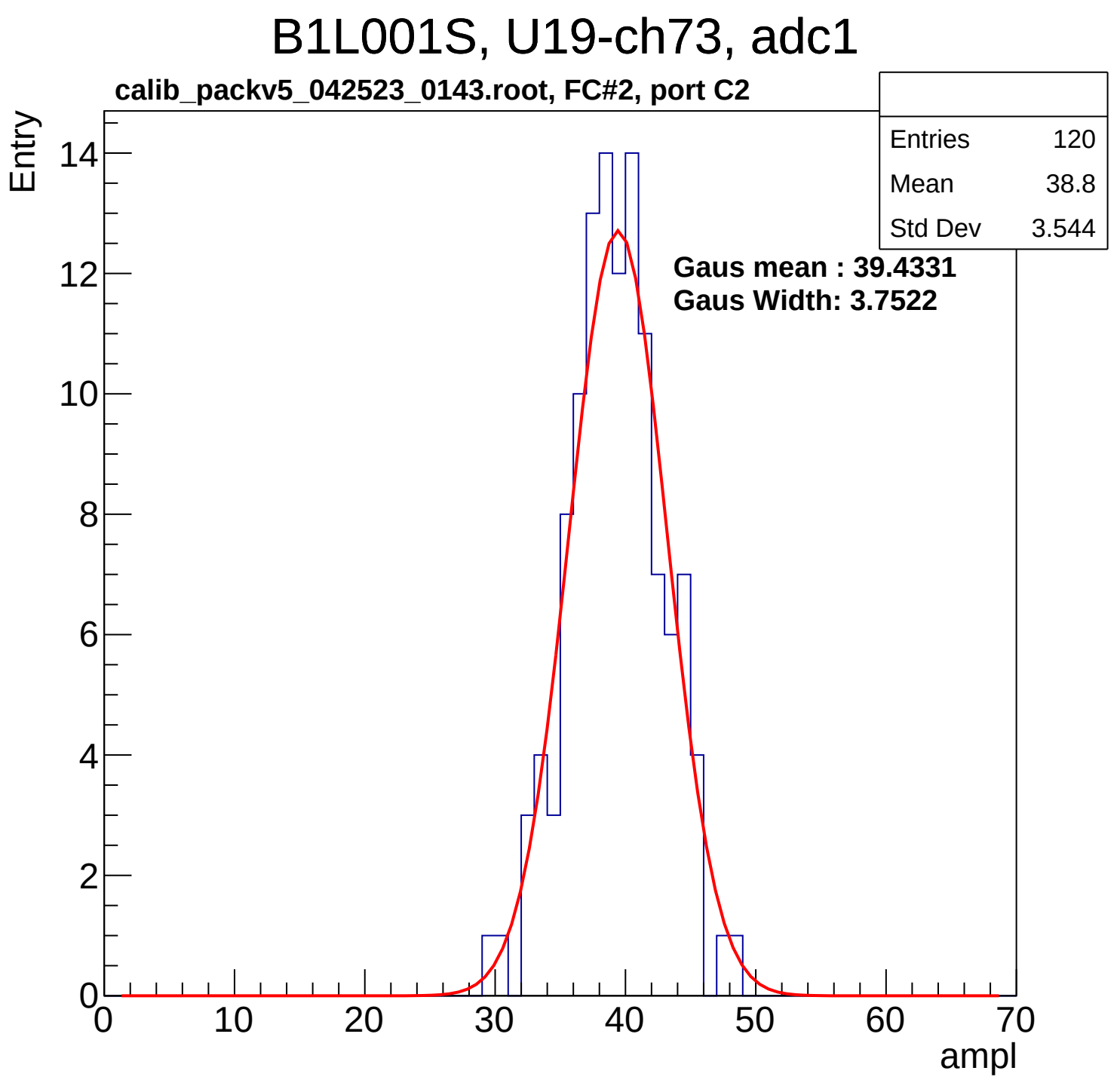
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70


B1L001S, U19-ch73, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 120
Mean 38.8
Std Dev 3.544
Gaus mean : 39.4331
Gaus Width: 3.7522
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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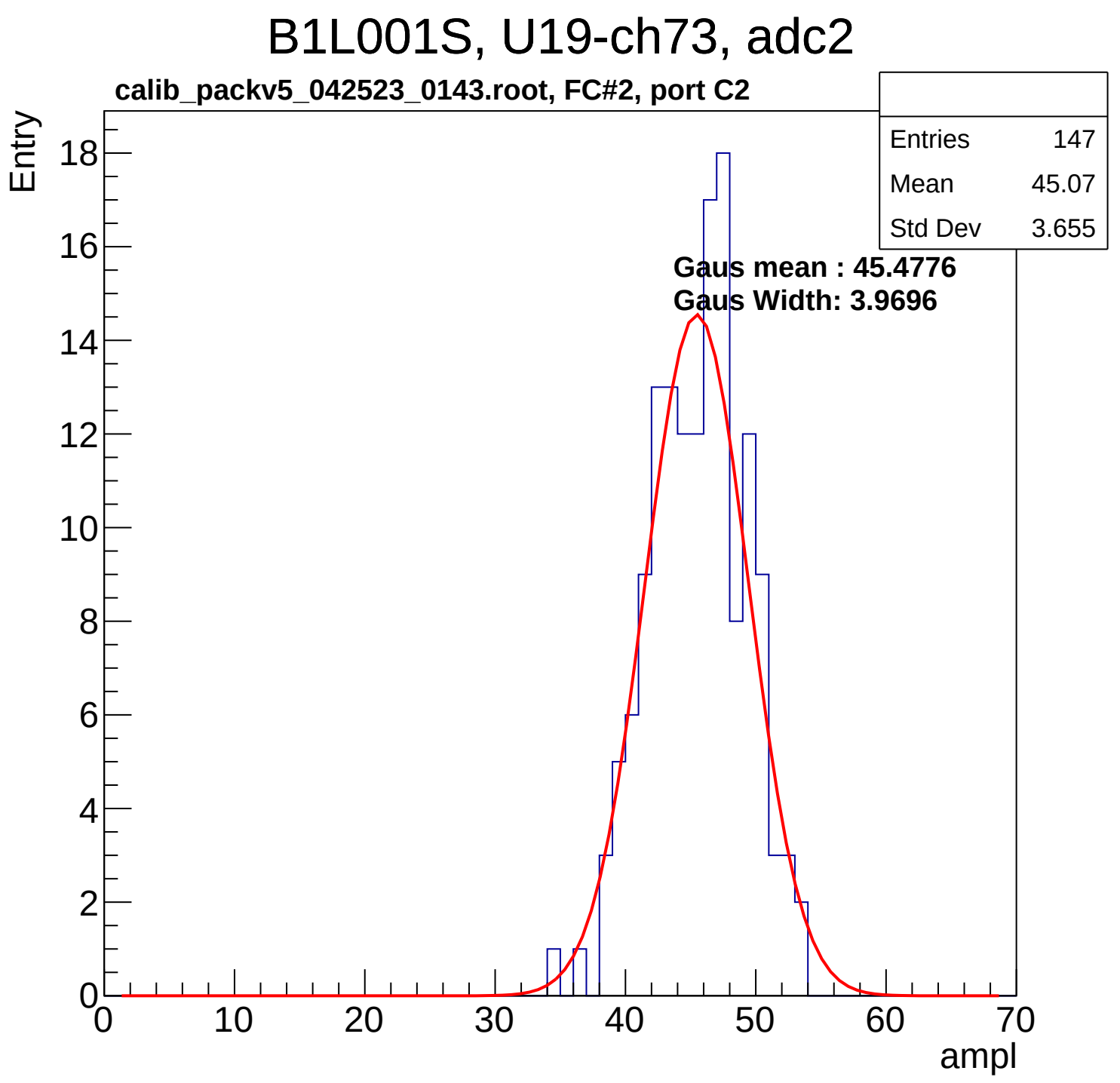
B1L001S, U19-ch73, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 147
Mean 45.07
Std Dev 3.655
Gaus mean : 45.4776
Gaus Width: 3.9696
Entry
ampl
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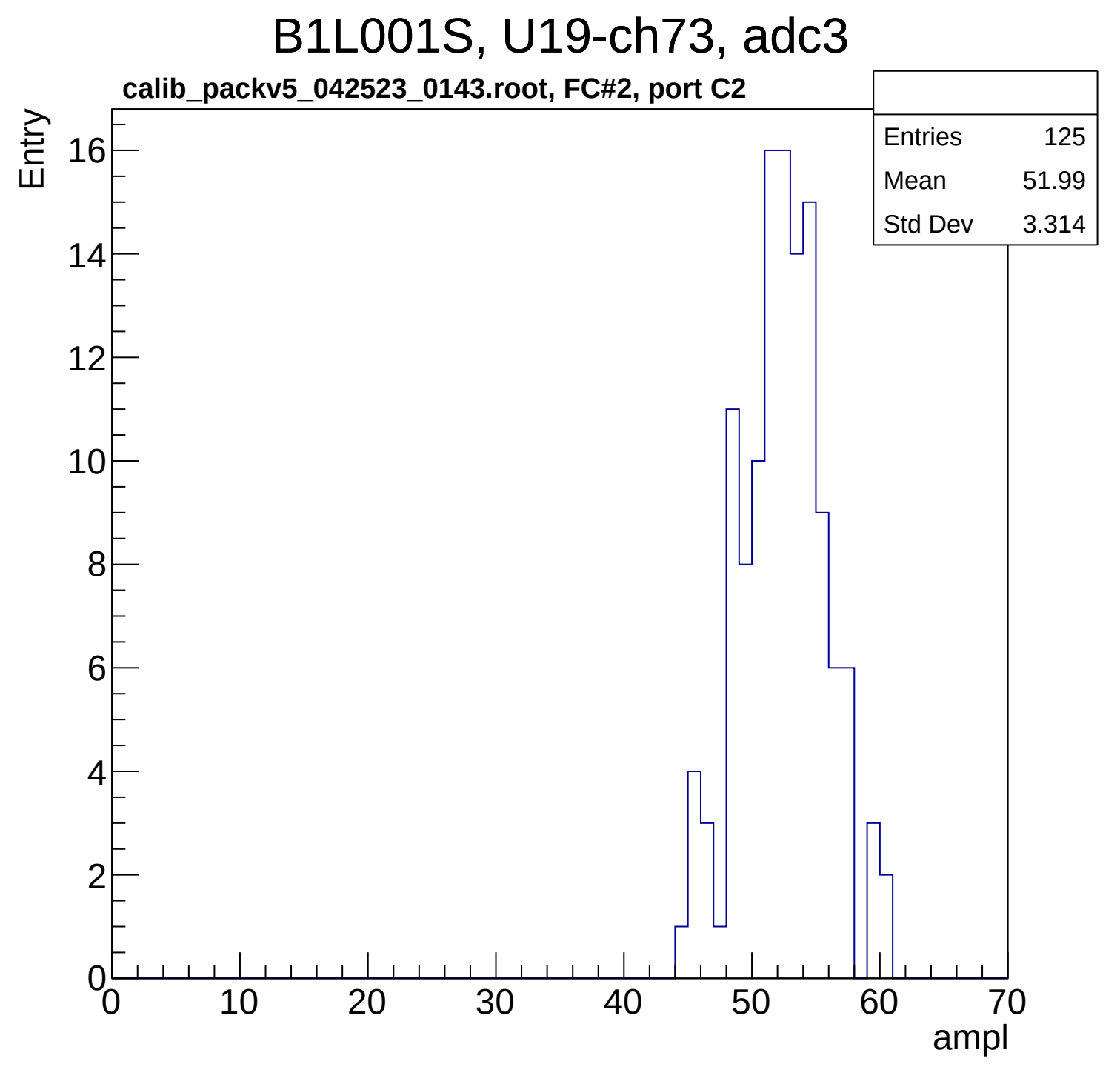
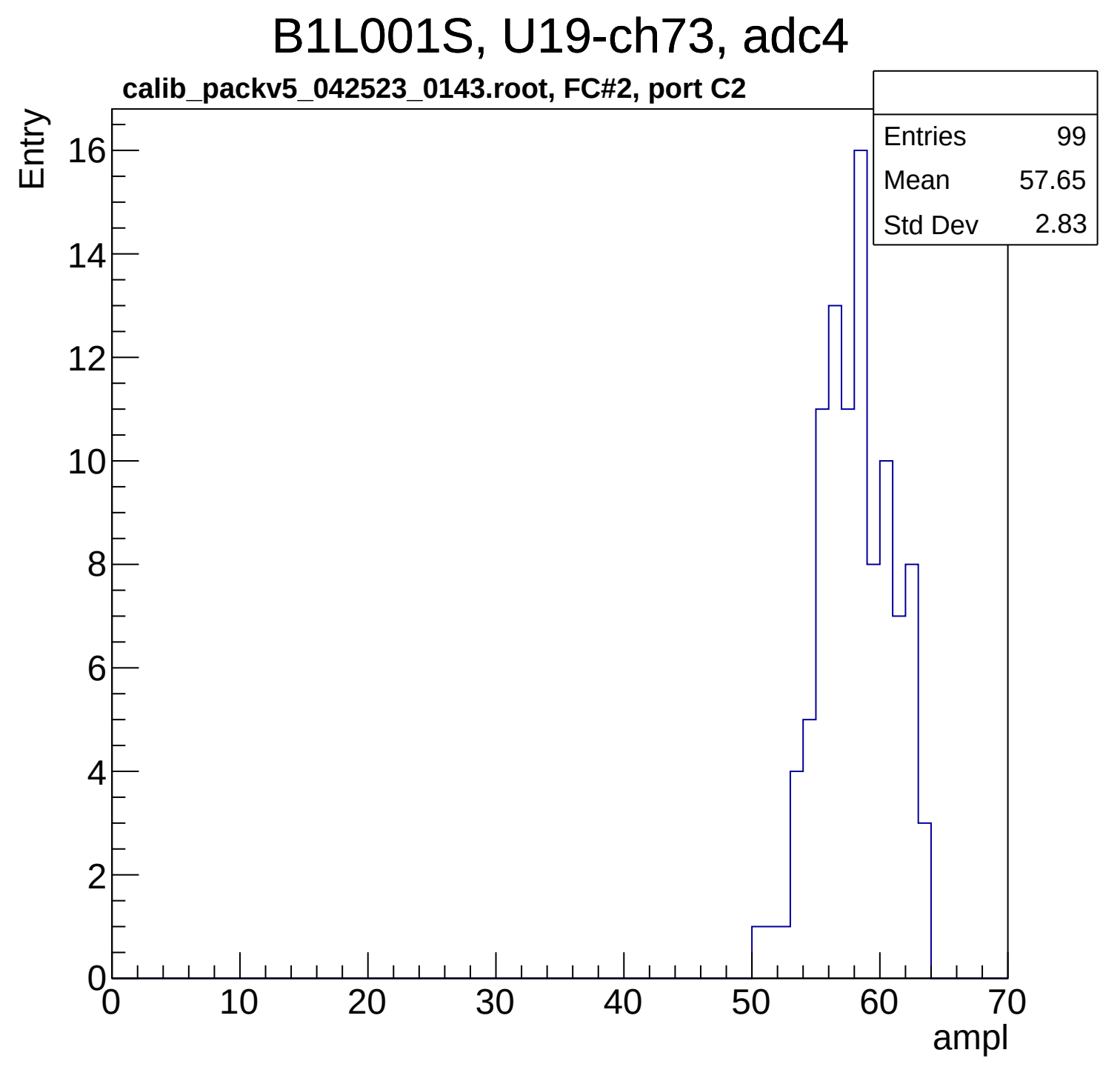
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70


B1L001S, U19-ch73, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 125
Mean 51.99
Std Dev 3.314
Entry
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch73, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 99
Mean 57.65
Std Dev 2.83
Entry
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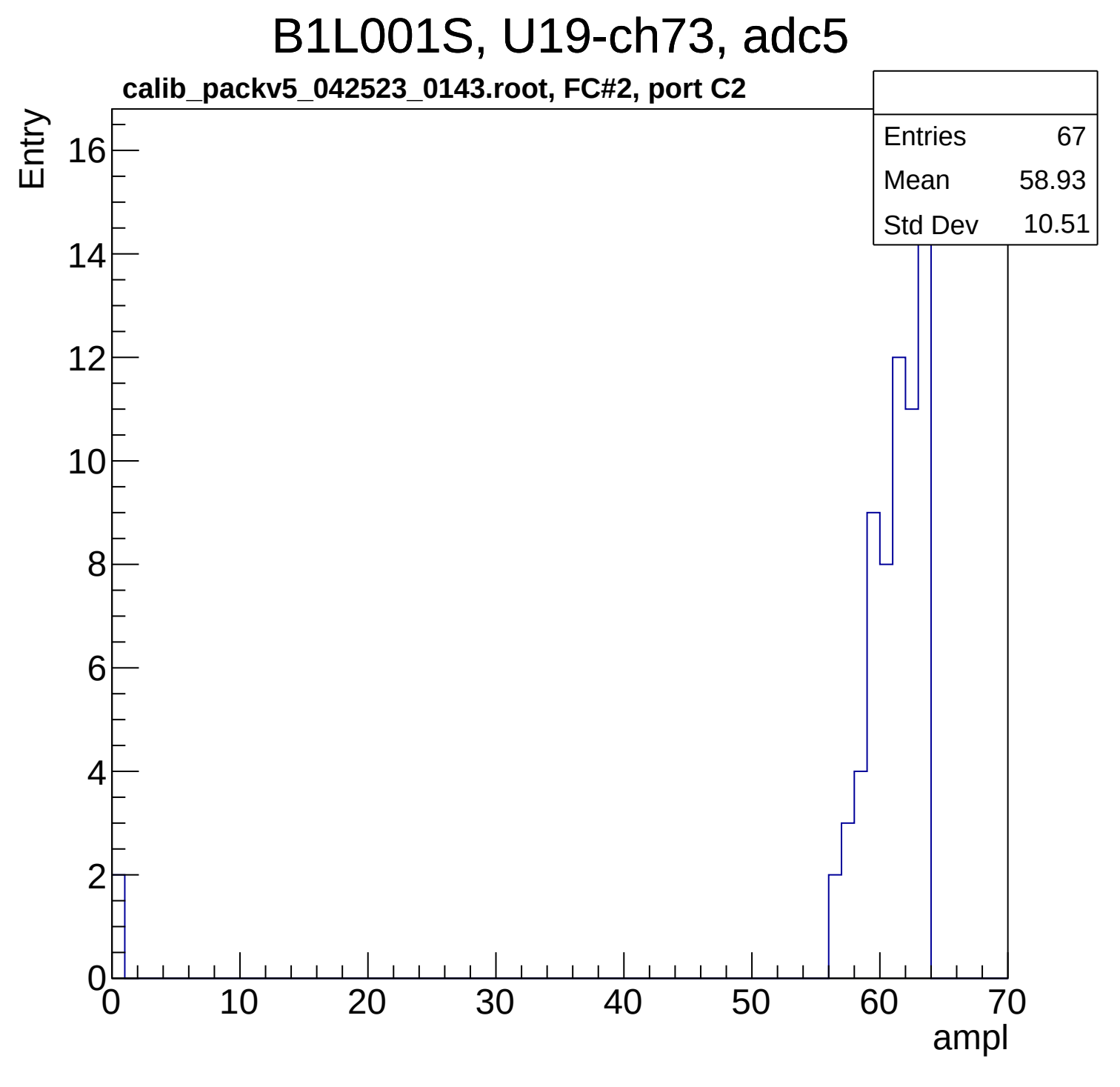
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch73, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 67
Mean 58.93
Std Dev 10.51
Entry
ampl
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2
4
6
8
10
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0
10
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60
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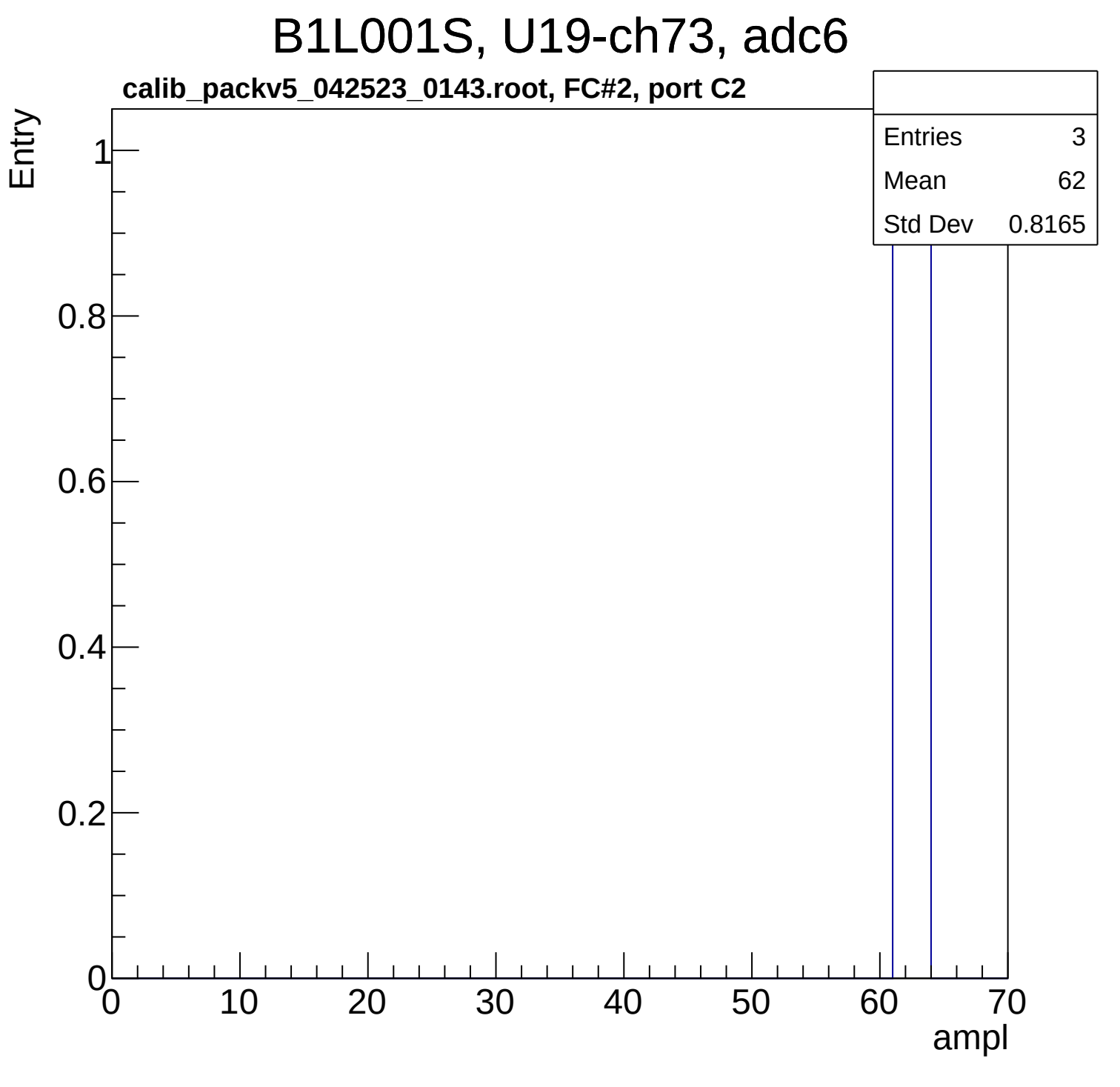
B1L001S, U19-ch73, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 3
Mean 62
Std Dev 0.8165
Entry
1
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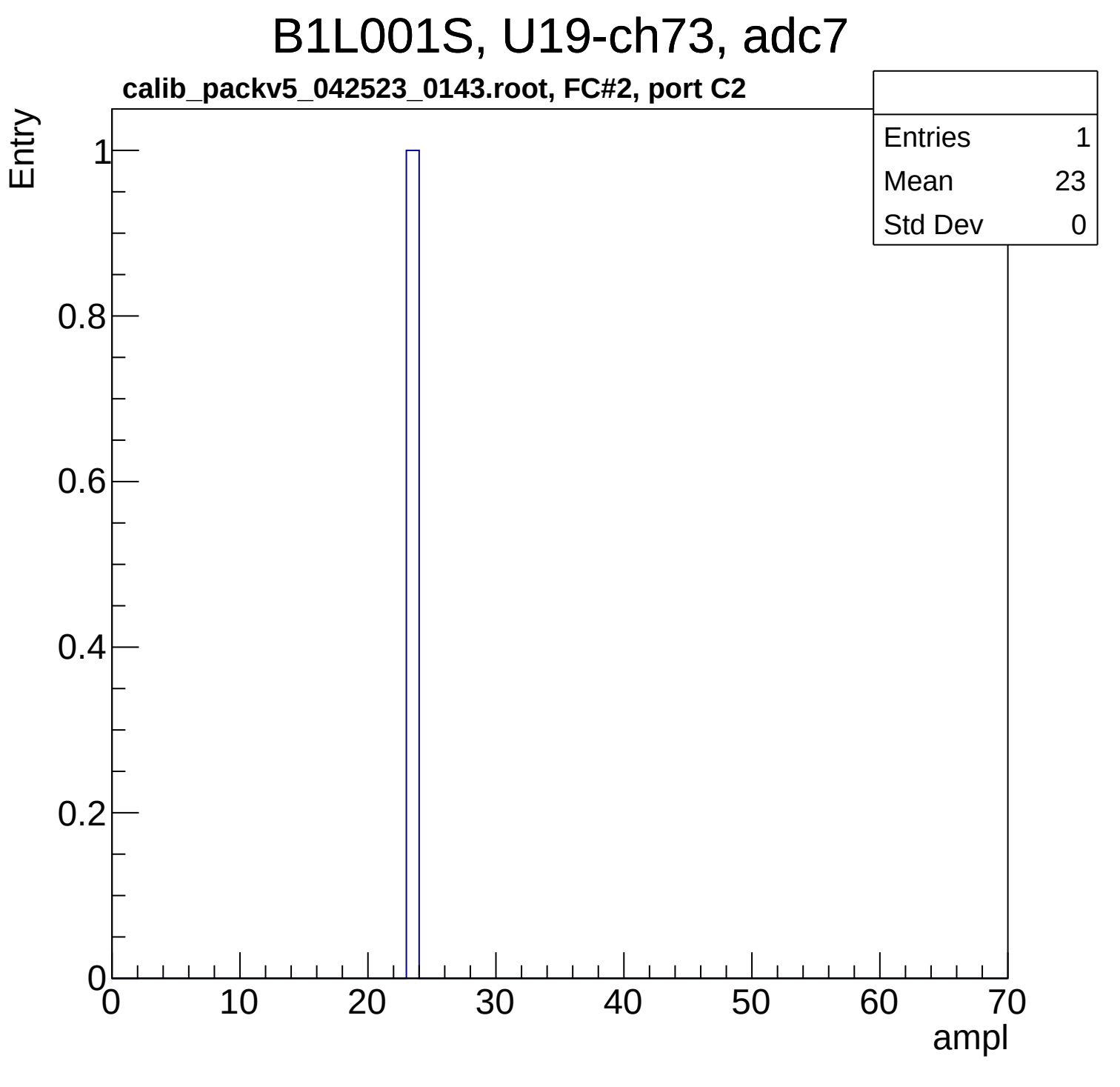
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch73, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 23
Std Dev 0
Entry
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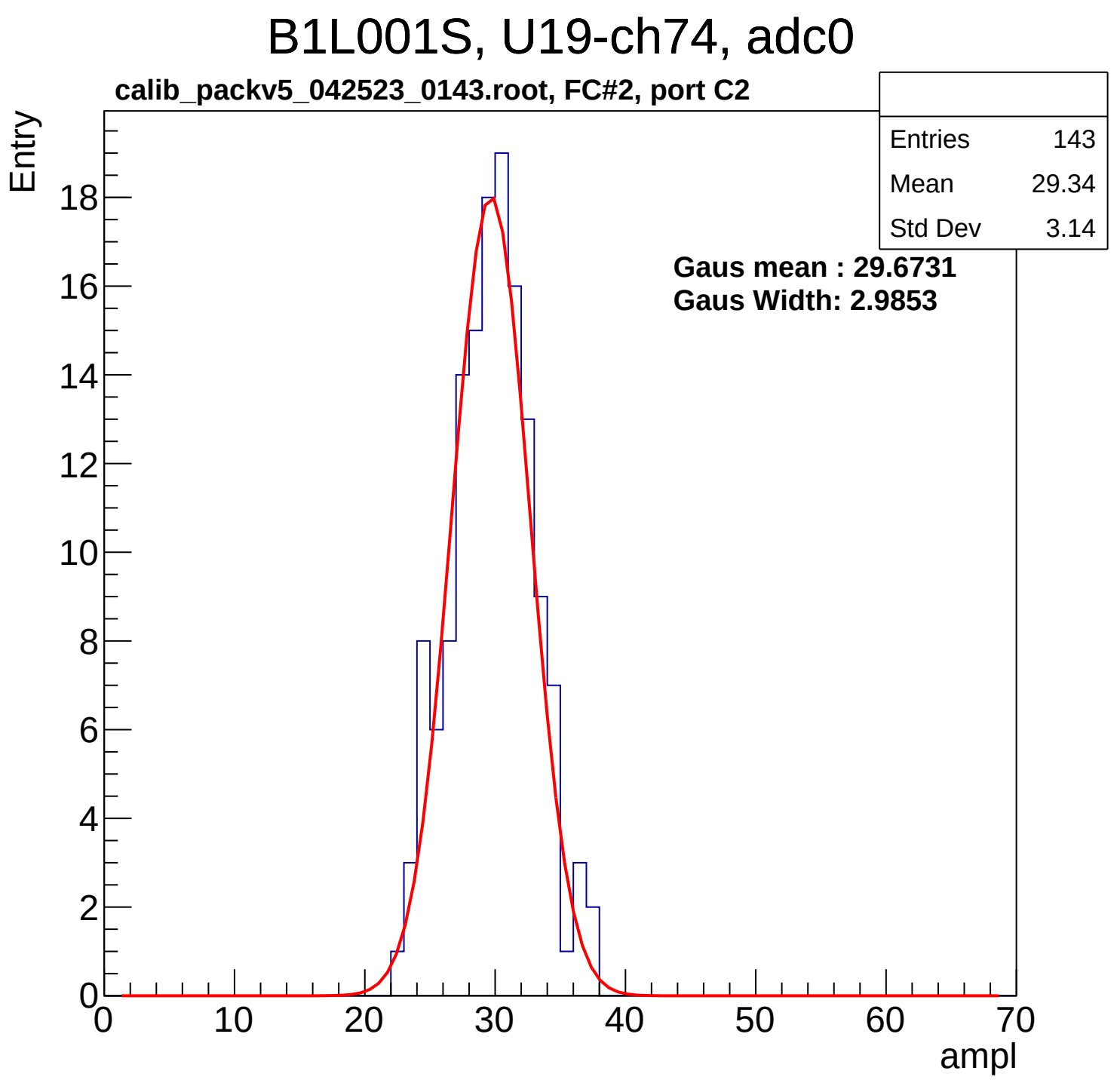
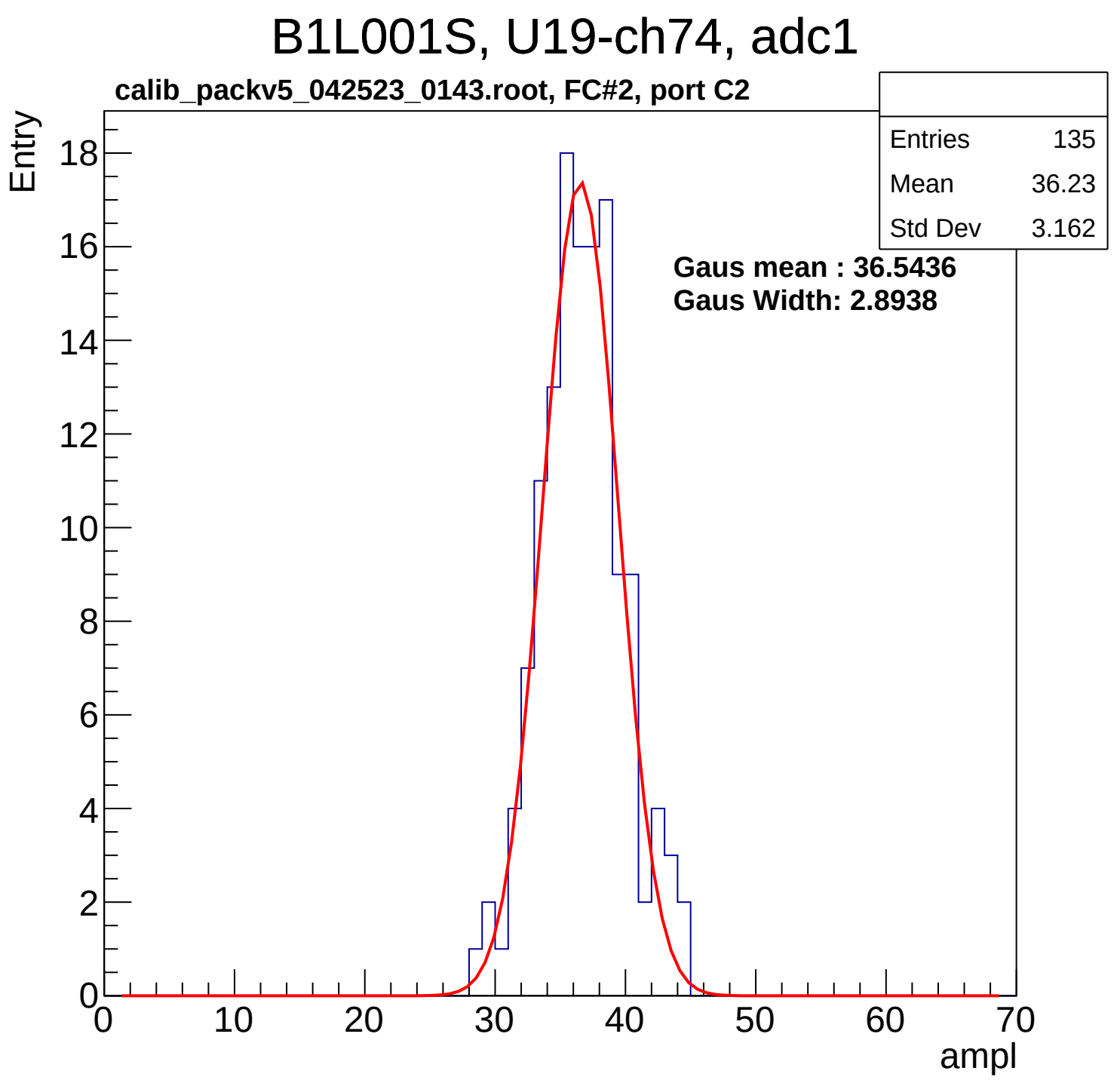
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch74, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 143
Mean 29.34
Std Dev 3.14
Gaus mean : 29.6731
Gaus Width: 2.9853
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70


B1L001S, U19-ch74, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 135
Mean 36.23
Std Dev 3.162
Gaus mean : 36.5436
Gaus Width: 2.8938
Entry
ampl
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2
4
6
8
10
12
14
16
18
0
10
20
30
40
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60
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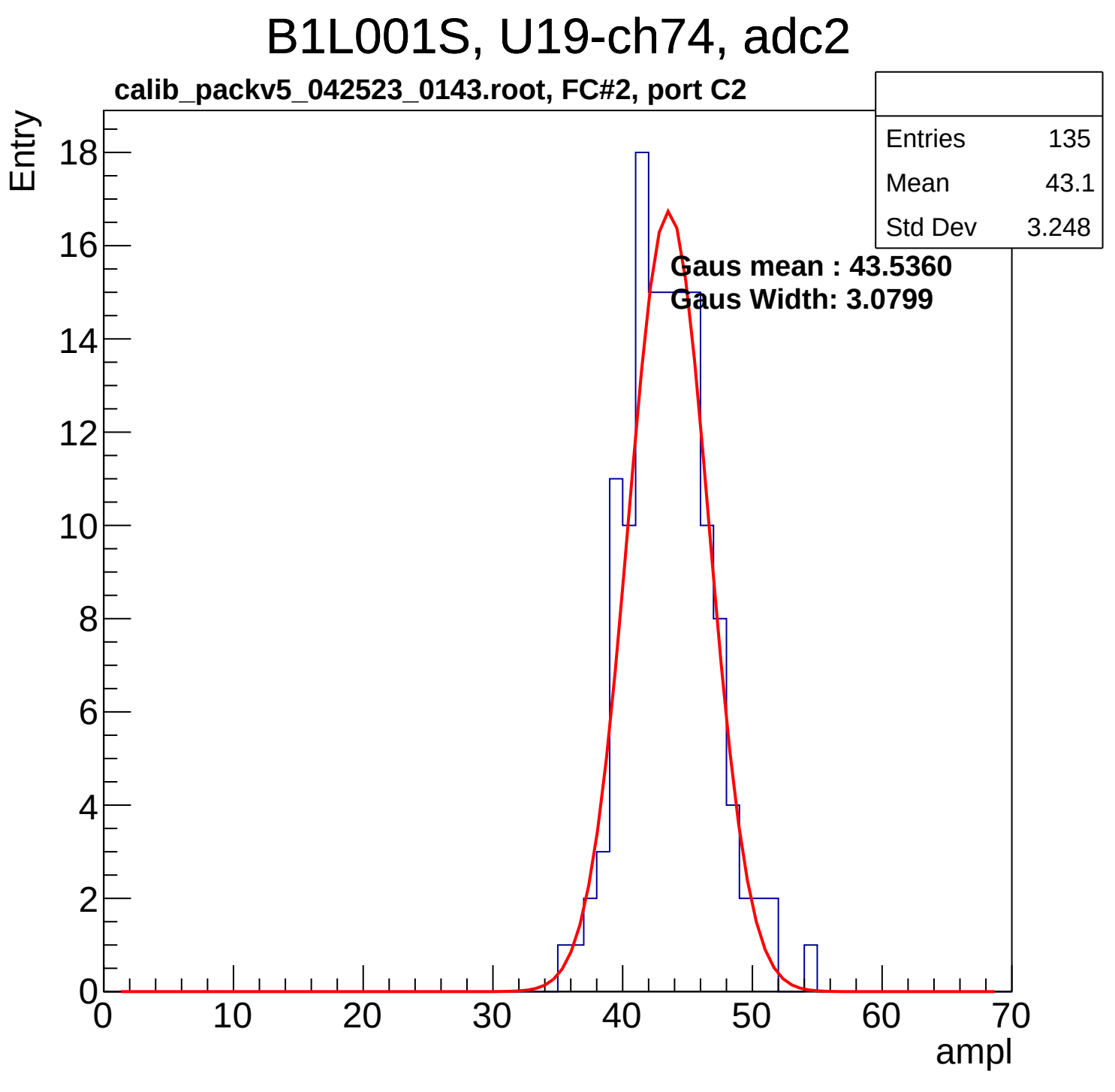
B1L001S, U19-ch74, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 135
Mean 43.1
Std Dev 3.248
Gaus mean : 43.5360
Gaus Width: 3.0799
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
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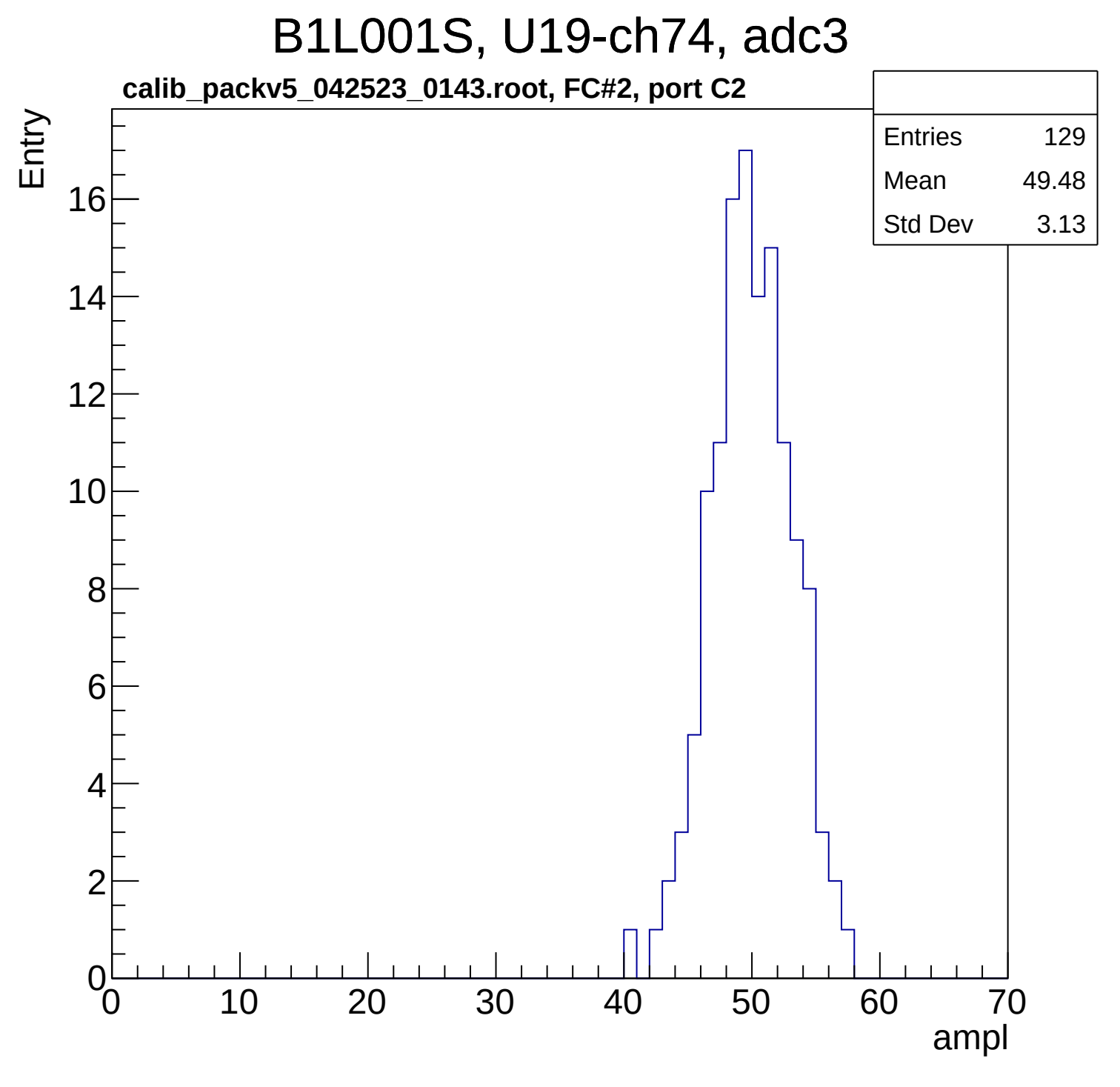
B1L001S, U19-ch74, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 129
Mean 49.48
Std Dev 3.13
Entry
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4
6
8
10
12
14
16
0
10
20
30
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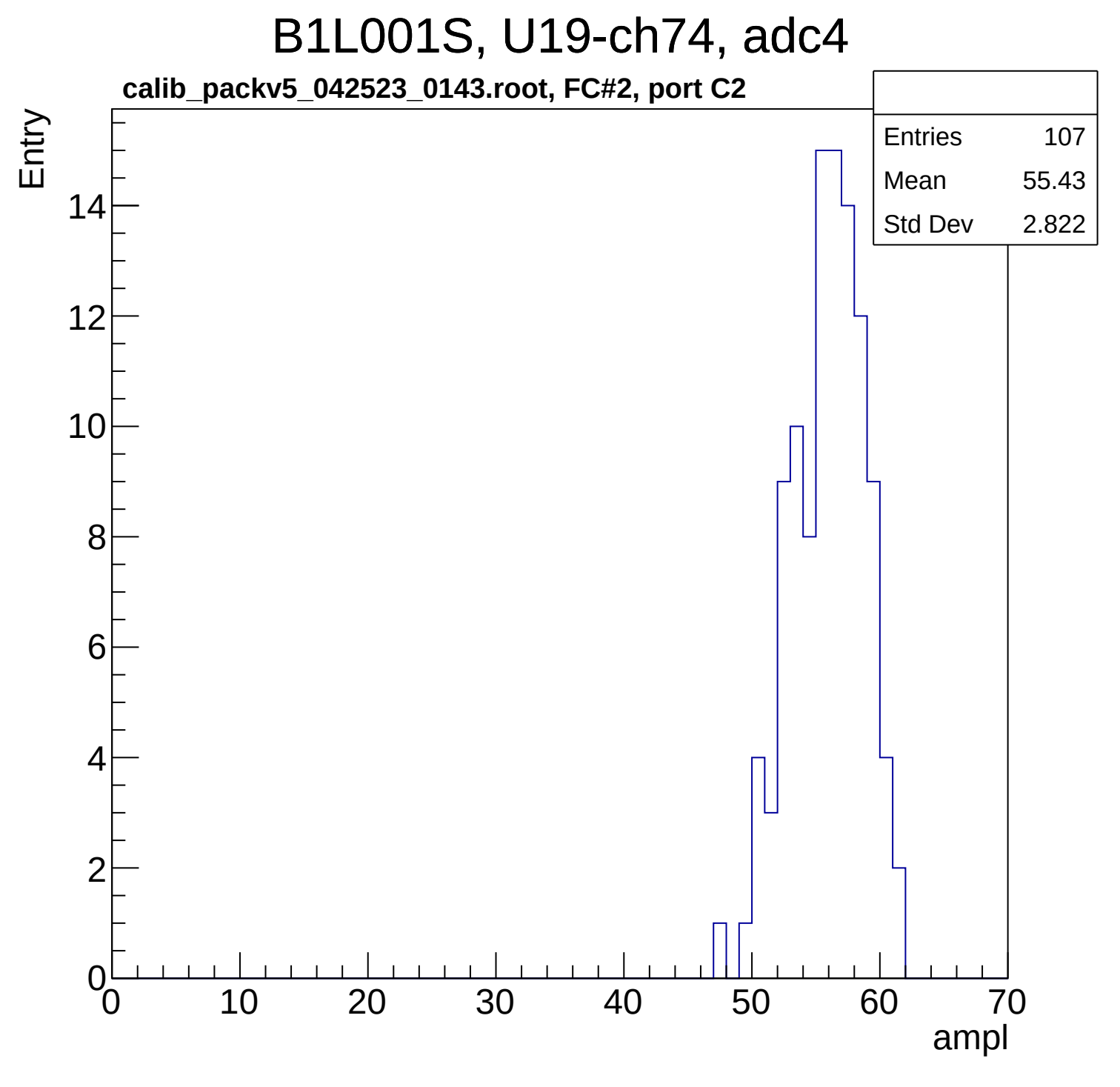
50
60
70
ampl


B1L001S, U19-ch74, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 107
Mean 55.43
Std Dev 2.822
Entry
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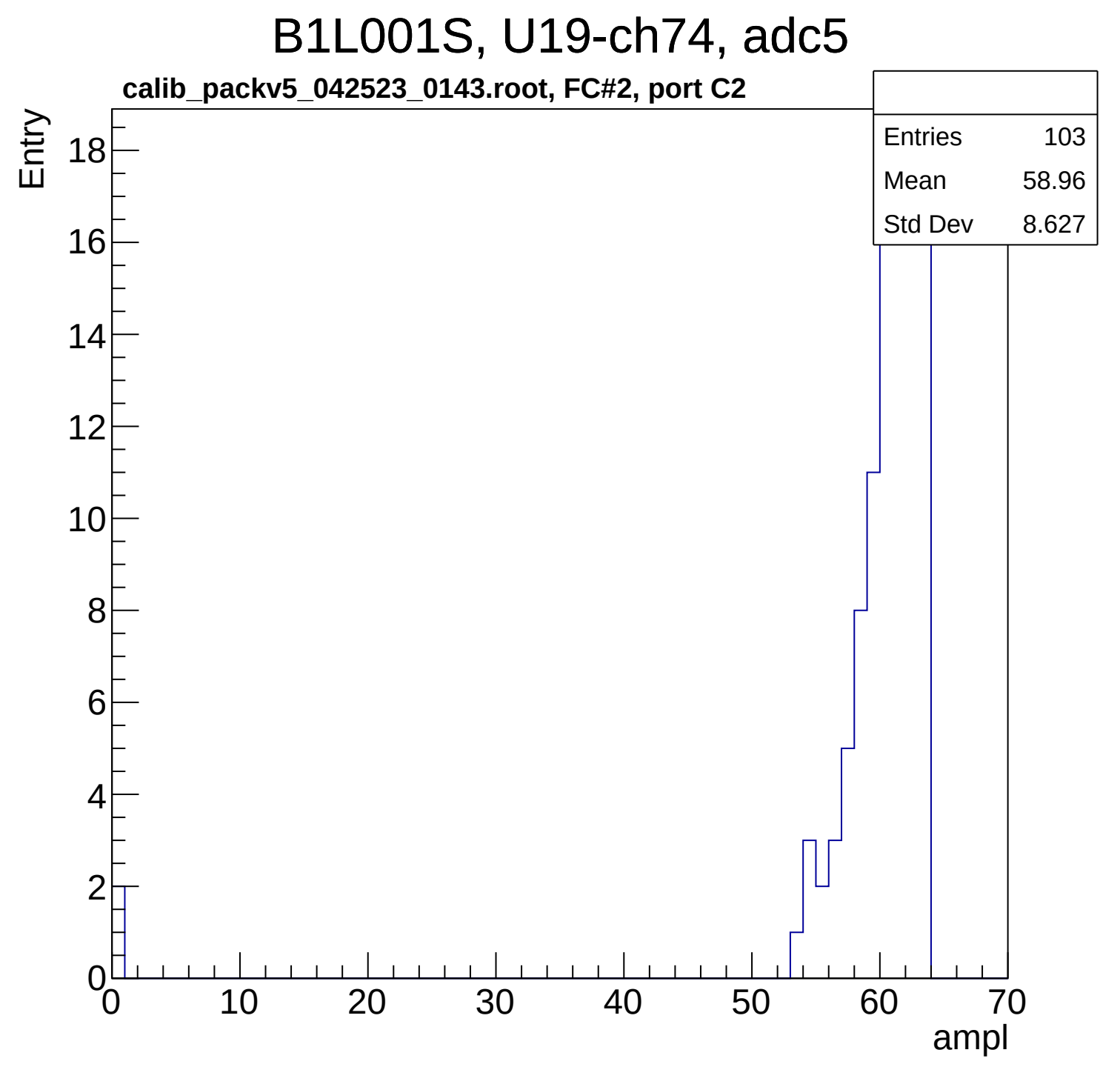
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch74, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 103
Mean 58.96
Std Dev 8.627
Entry
ampl
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2
4
6
8
10
12
14
16
18
0
10
20
30
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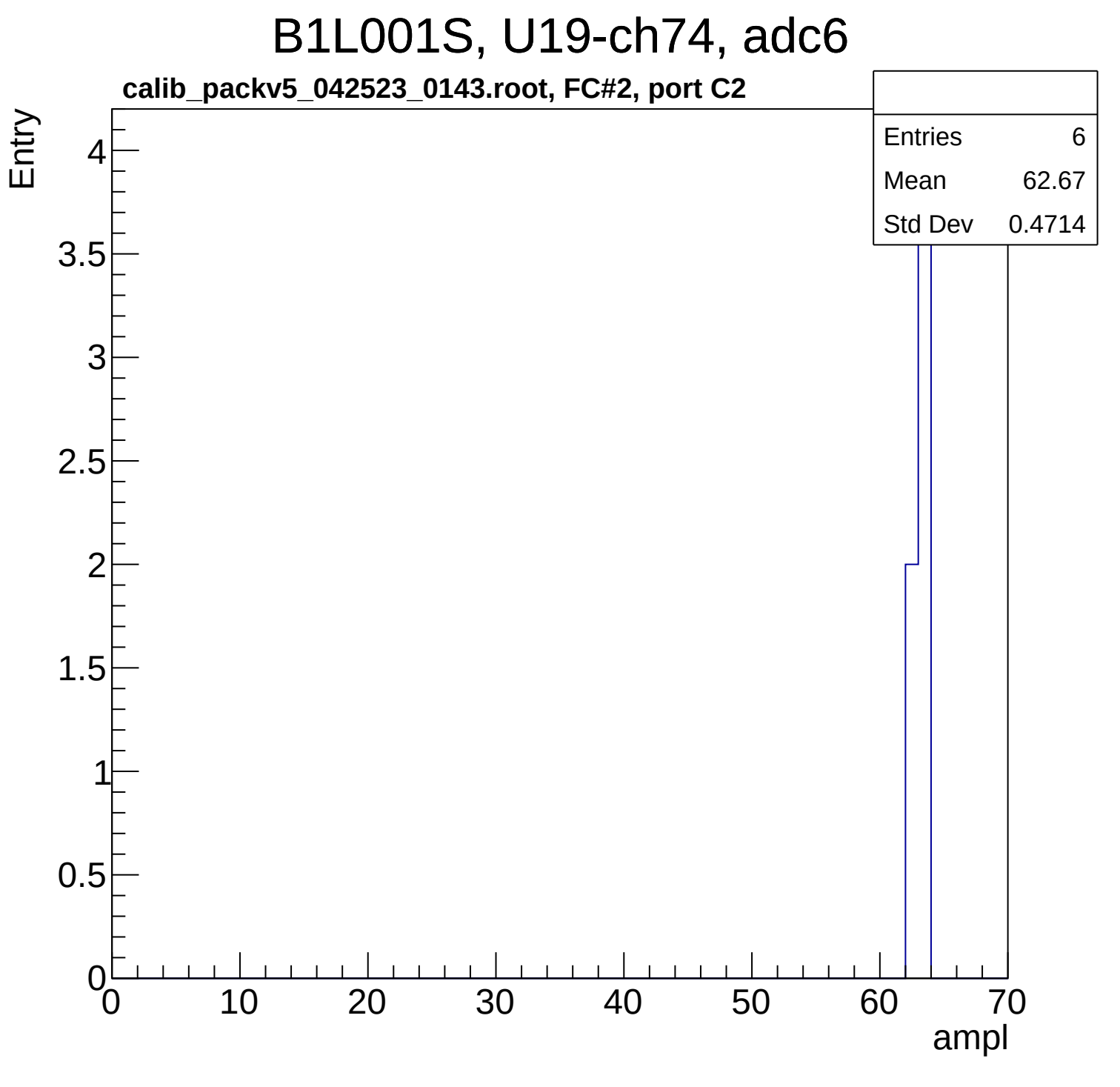
B1L001S, U19-ch74, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 6
Mean 62.67
Std Dev 0.4714
Entry
ampl
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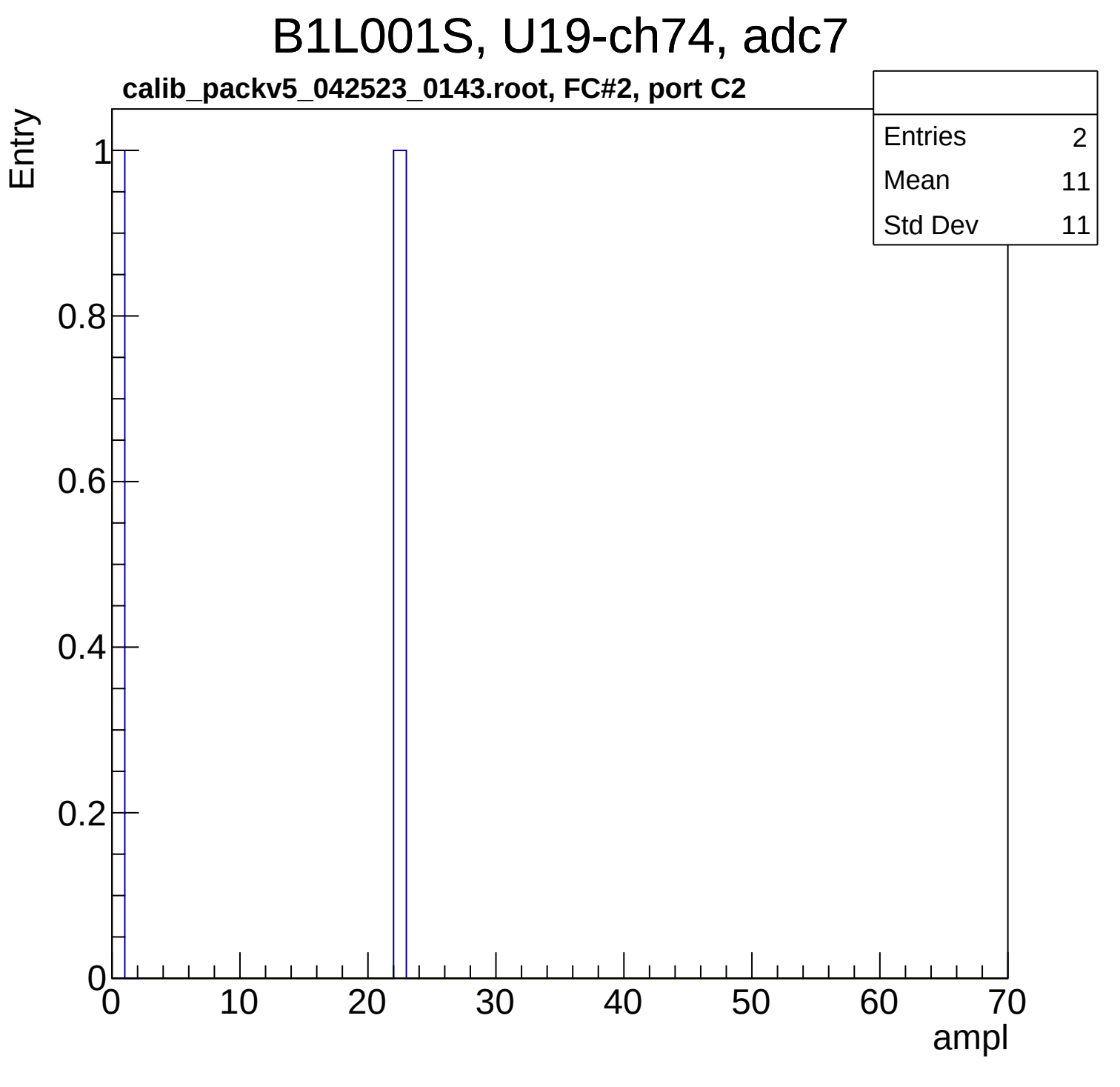
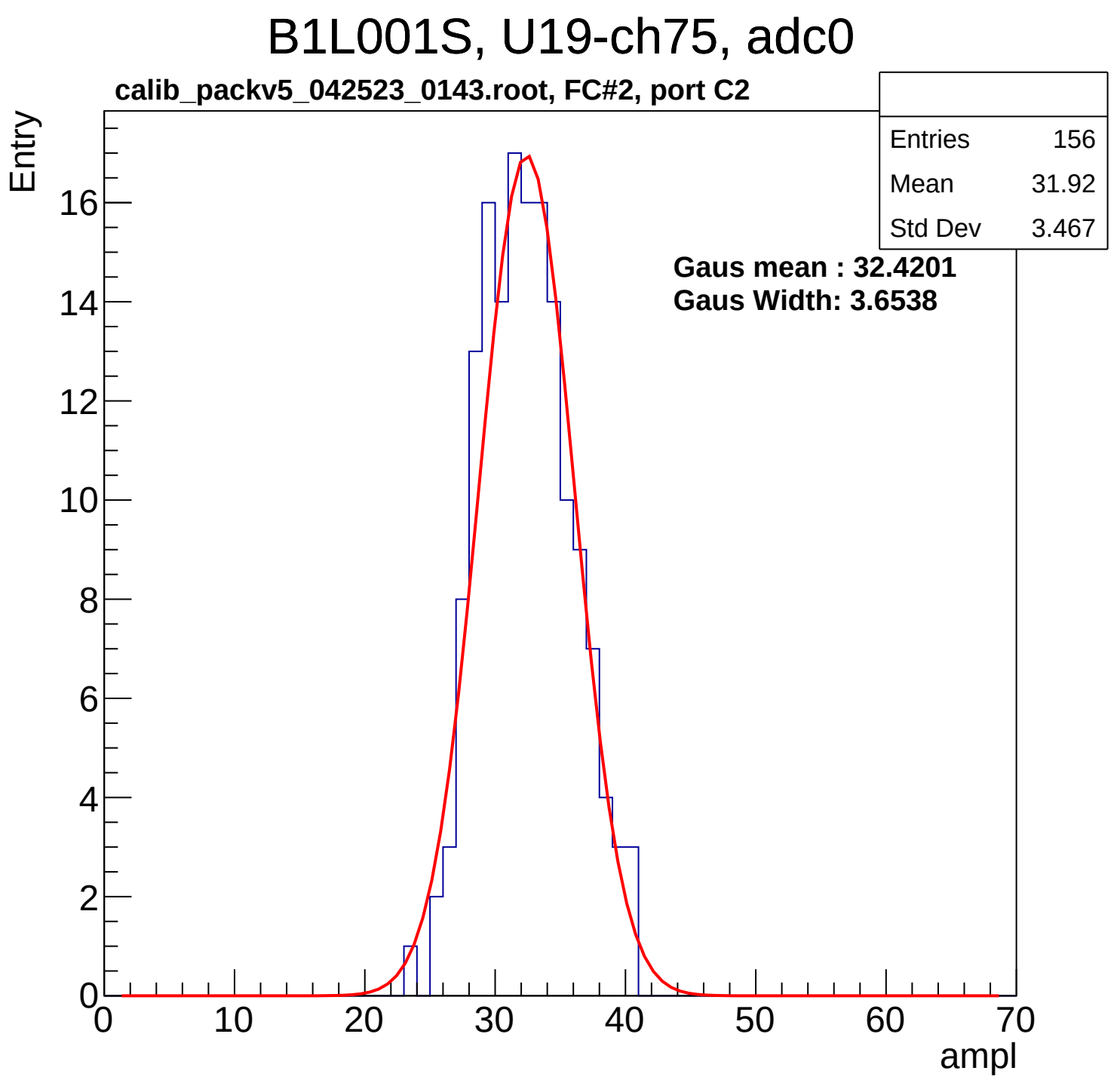
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L001S, U19-ch74, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 11
Std Dev 11
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch75, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 156
Mean 31.92
Std Dev 3.467
Gaus mean : 32.4201
Gaus Width: 3.6538
Entry
ampl
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2
4
6
8
10
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14
16
0
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40
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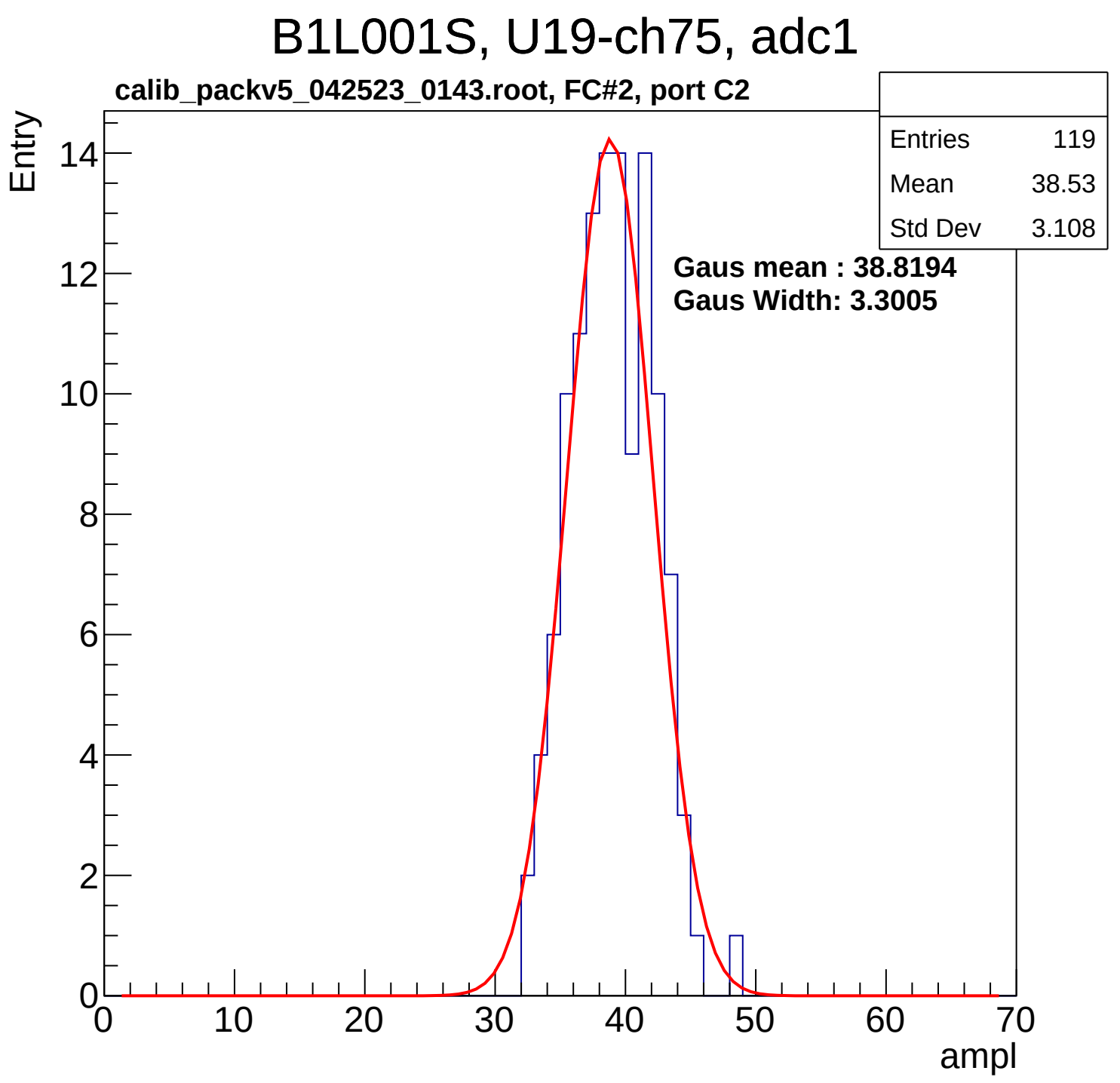
B1L001S, U19-ch75, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 119
Mean 38.53
Std Dev 3.108
Gaus mean : 38.8194
Gaus Width: 3.3005
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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40
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60
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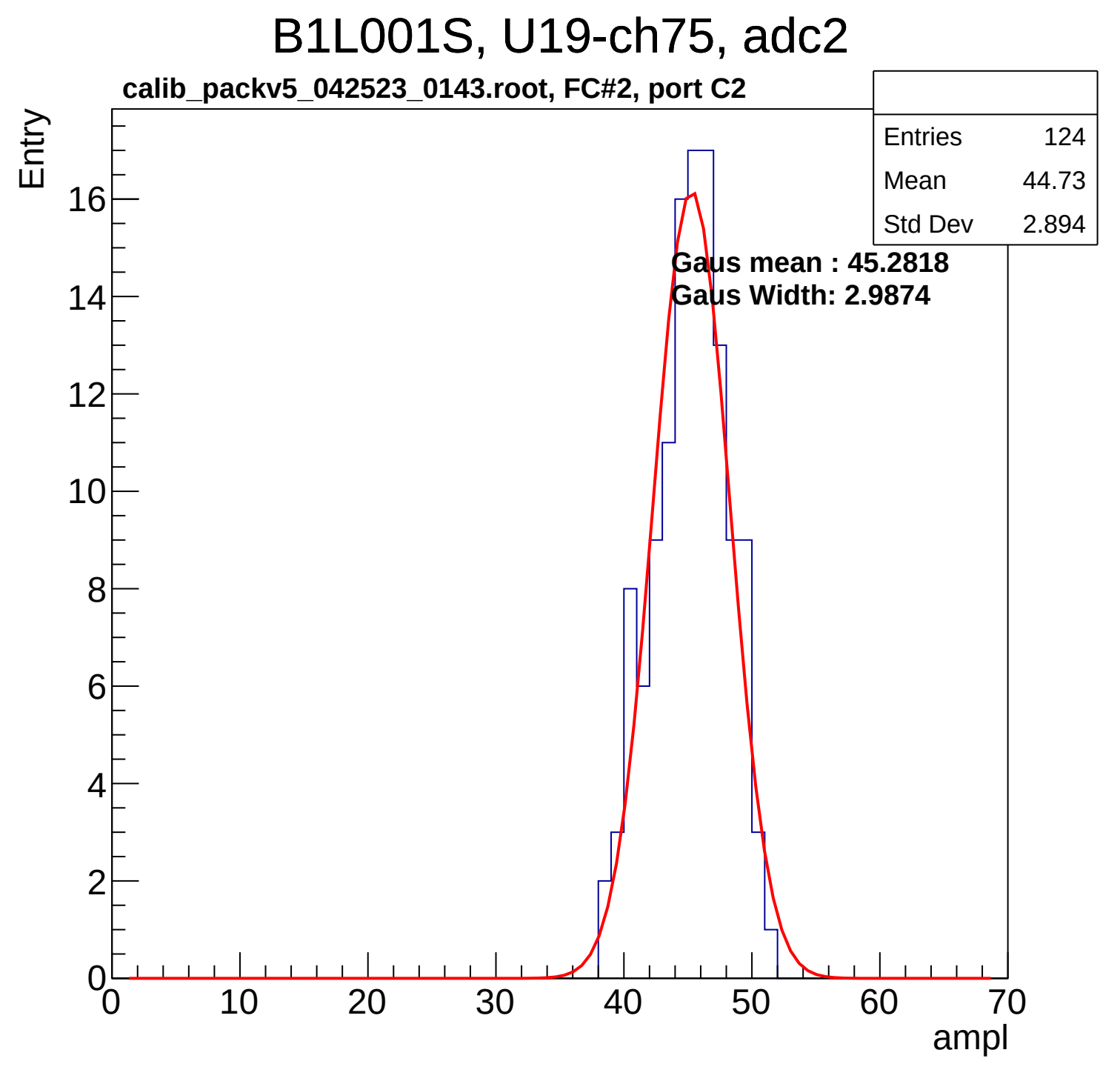
B1L001S, U19-ch75, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 124
Mean 44.73
Std Dev 2.894
Gaus mean : 45.2818
Gaus Width: 2.9874
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
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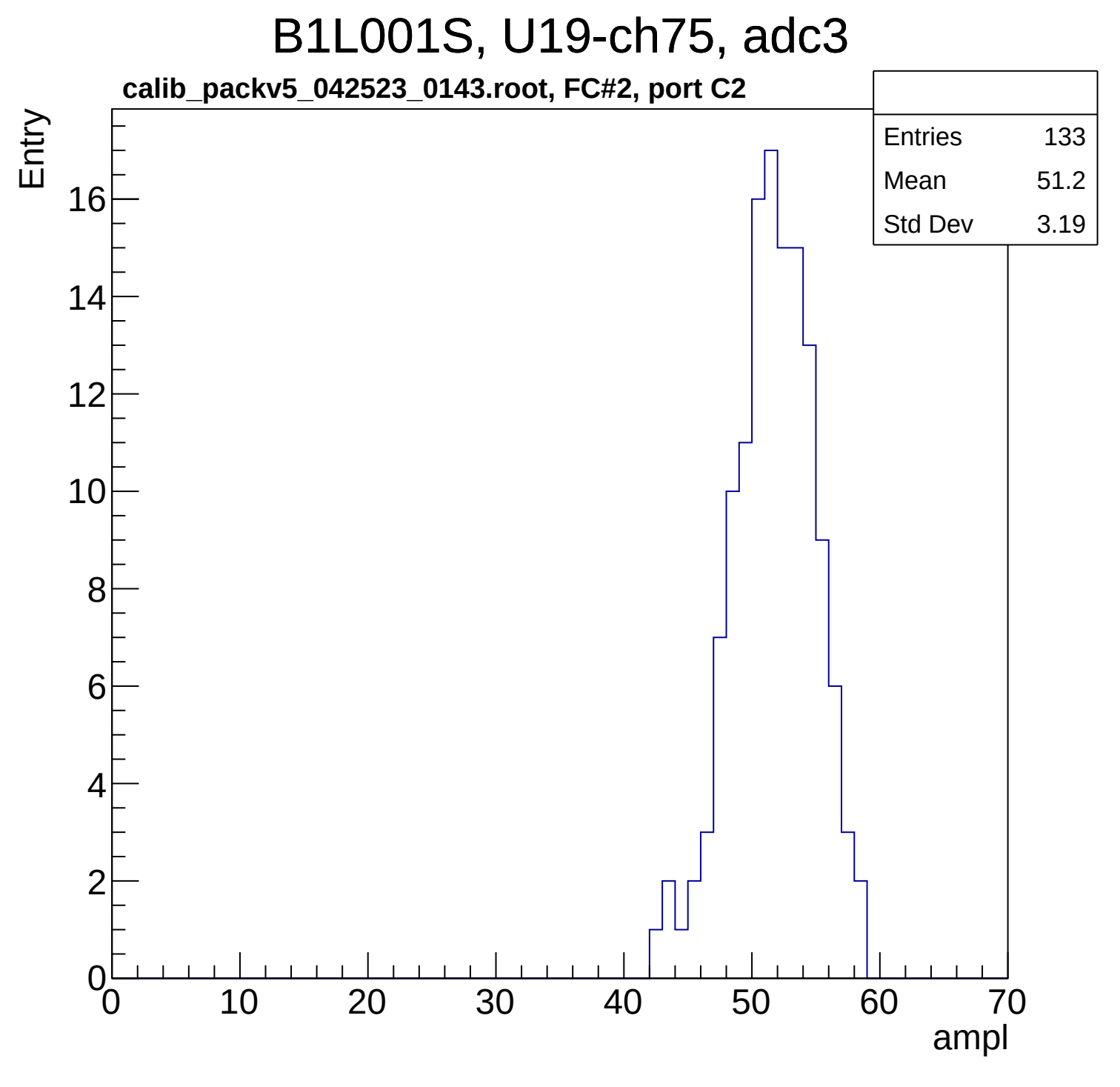
B1L001S, U19-ch75, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 133
Mean 51.2
Std Dev 3.19
Entry
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2
4
6
8
10
12
14
16
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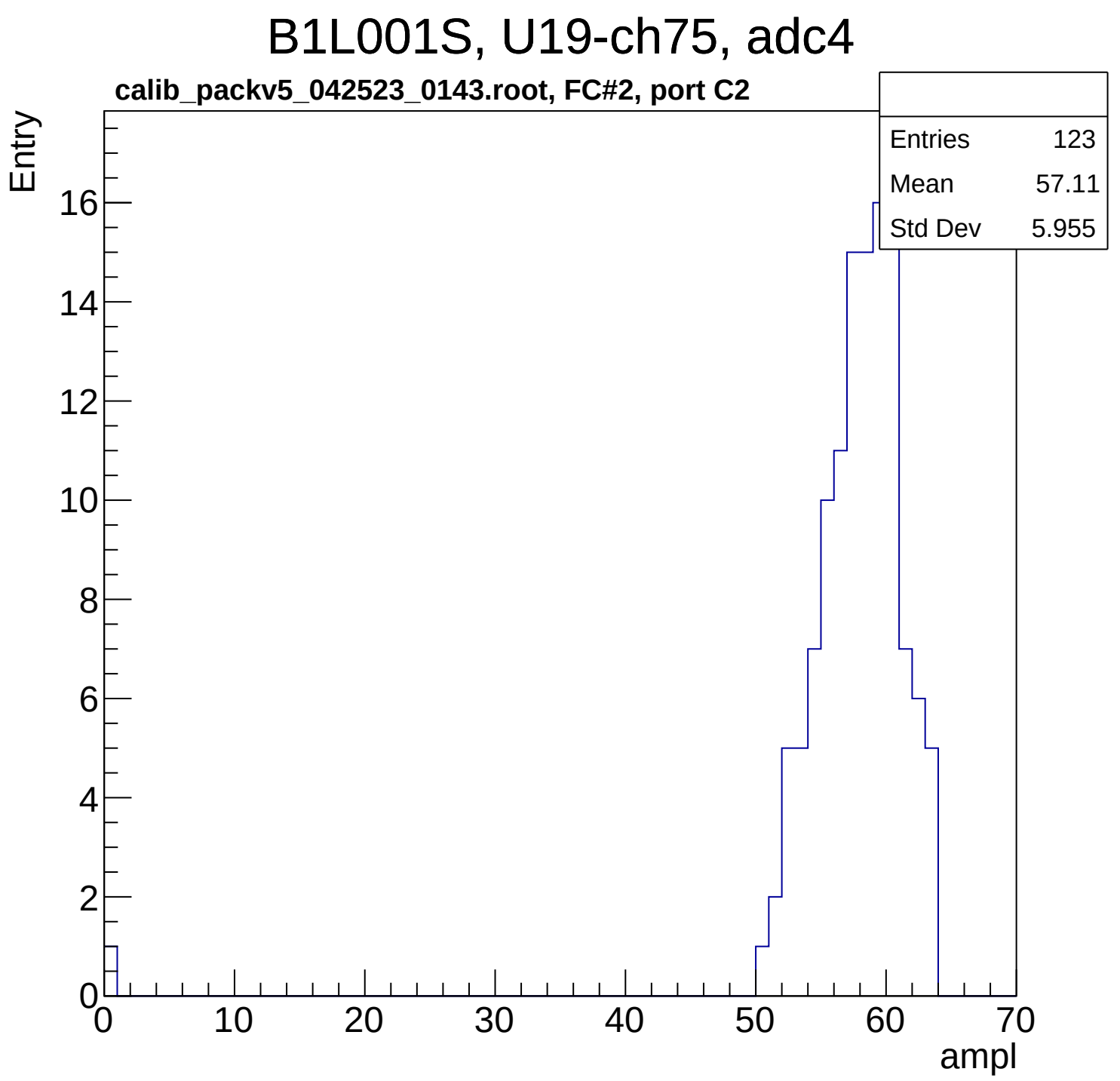
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch75, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 123
Mean 57.11
Std Dev 5.955
Entry
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4
6
8
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16
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10
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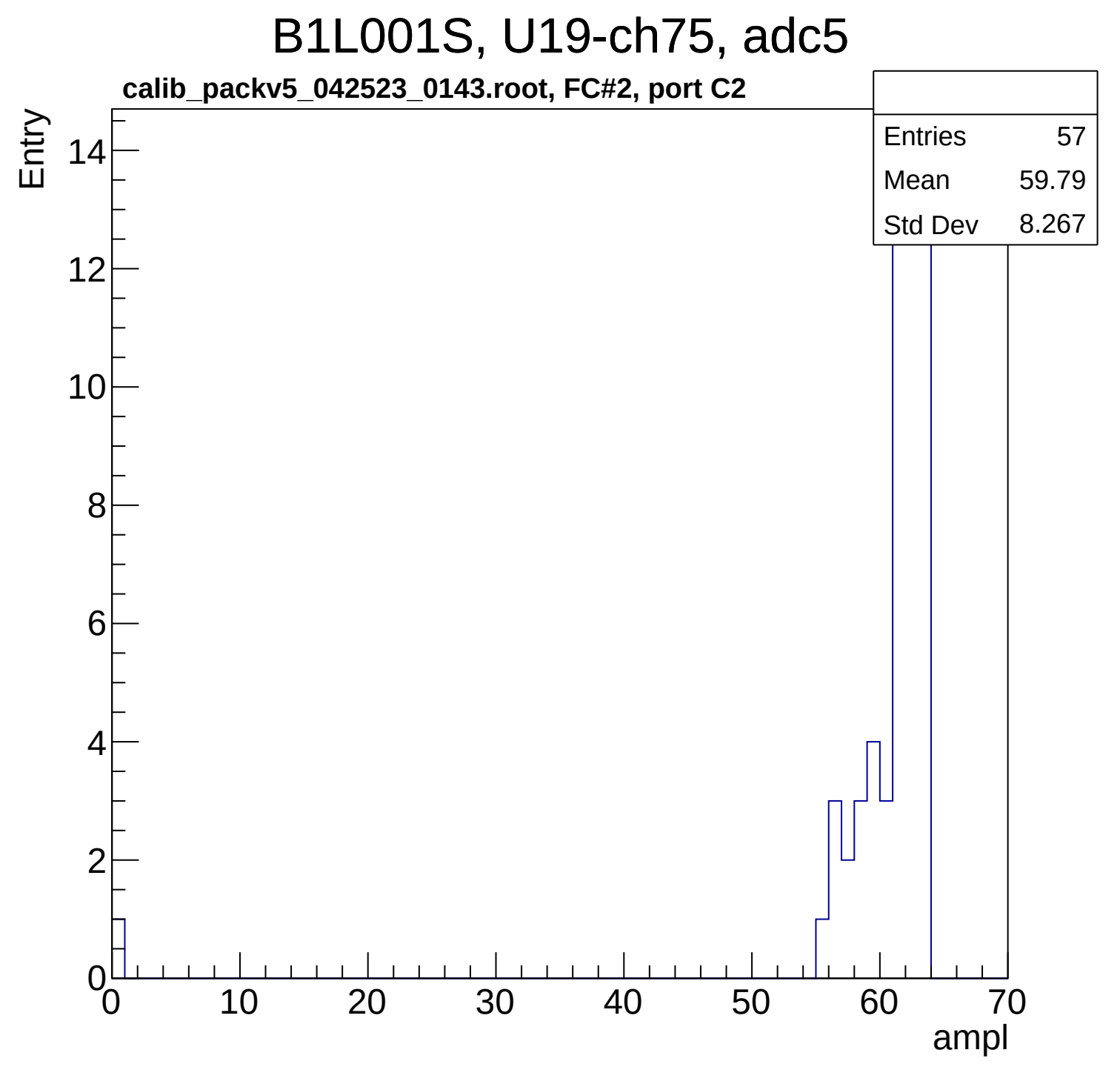
70
ampl


B1L001S, U19-ch75, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 57
Mean 59.79
Std Dev 8.267
Entry
ampl
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2
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0
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60
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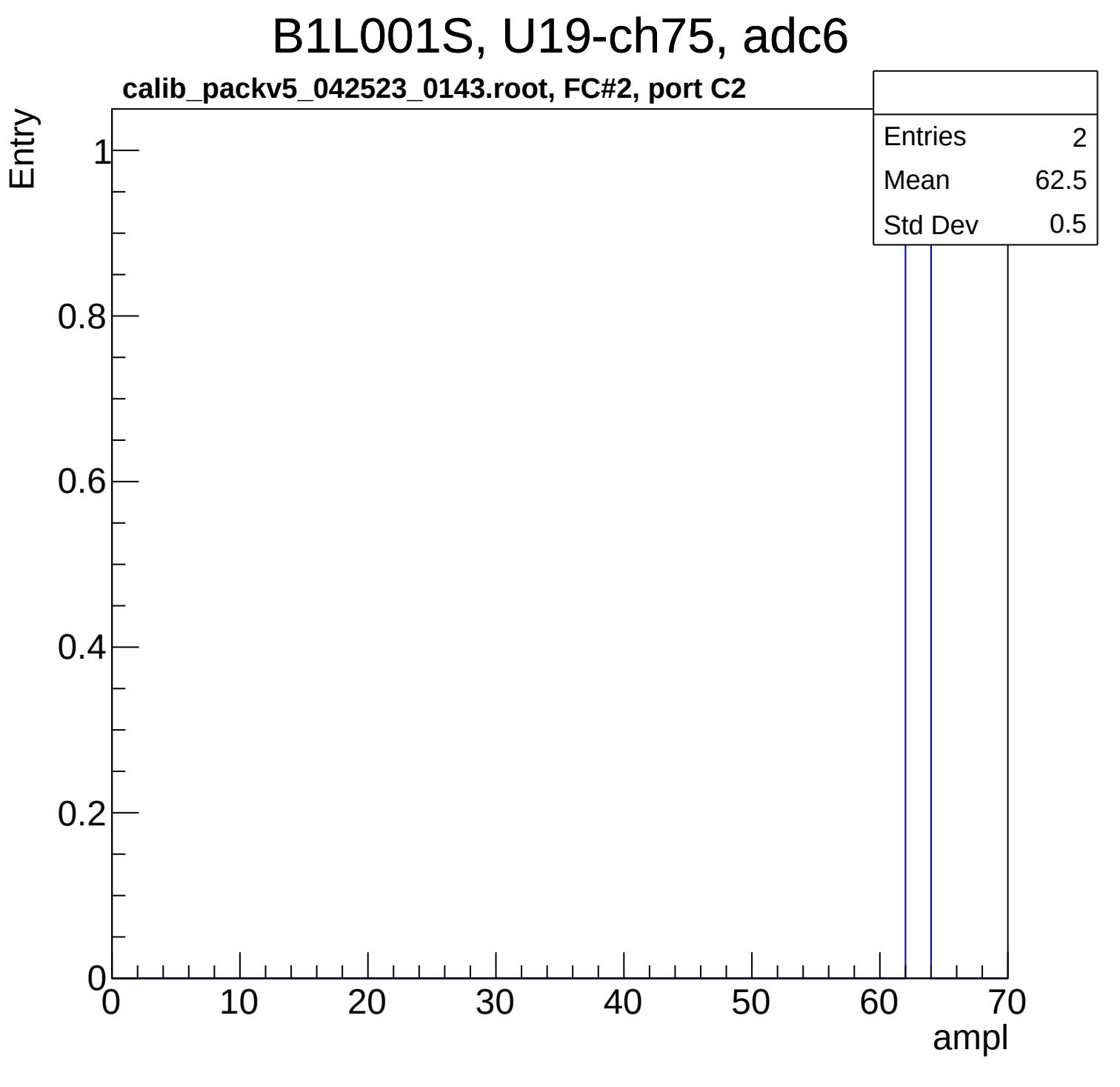
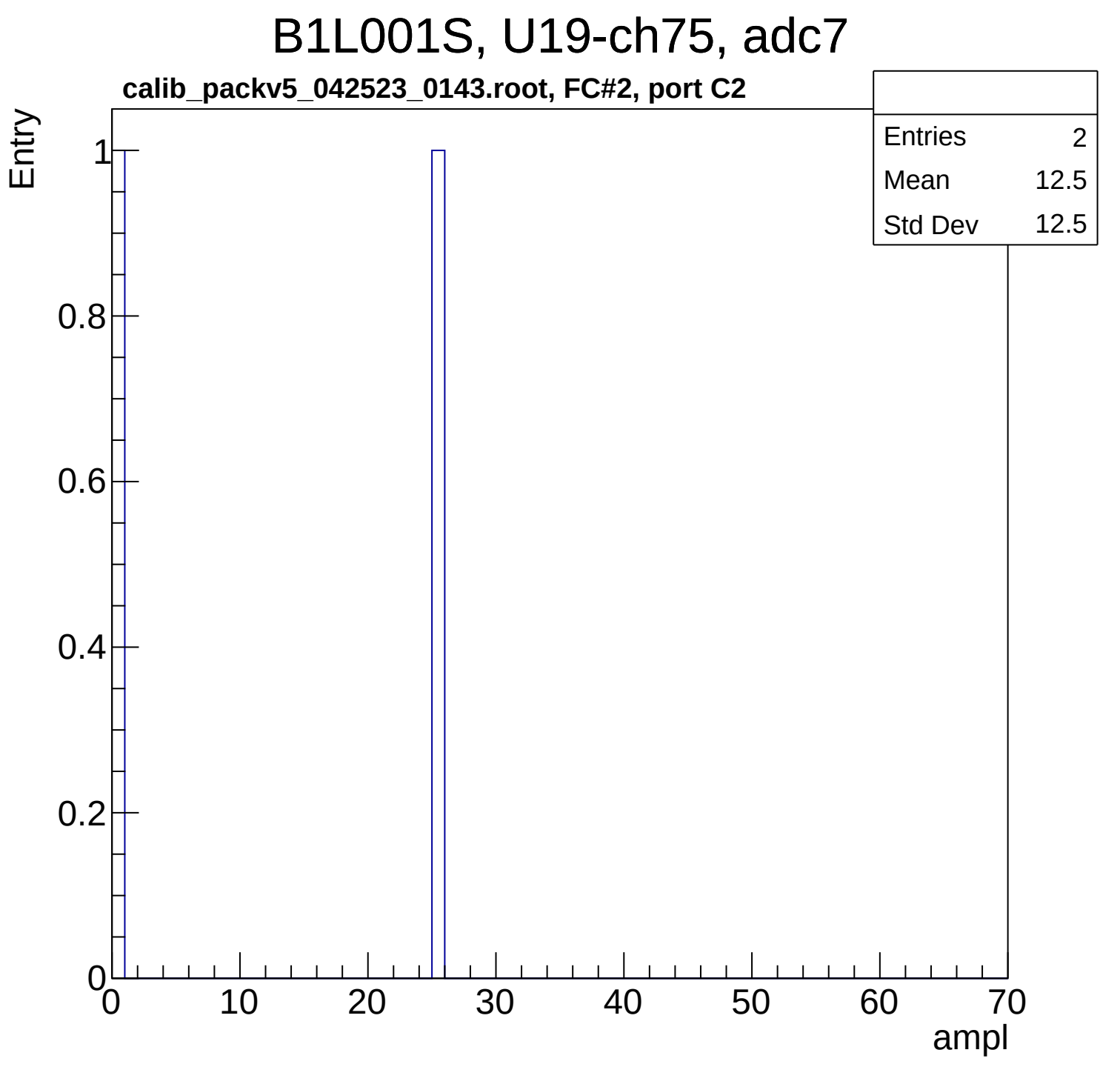

B1L001S, U19-ch75, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 62.5
Std Dev 0.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch75, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 12.5
Std Dev 12.5
Entry
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0.6
0.4
0.2
0
0
10
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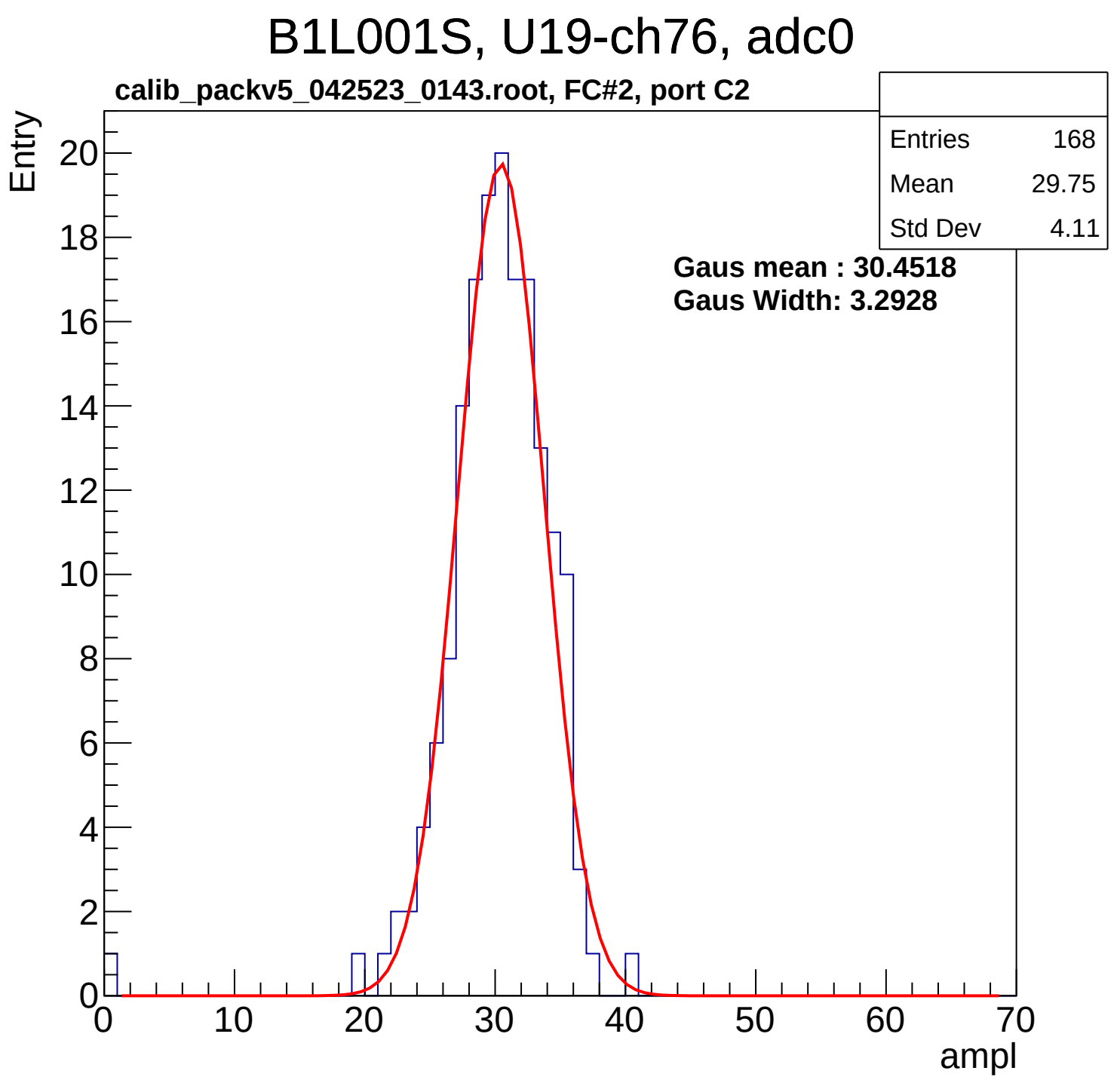
50
60
70
ampl


B1L001S, U19-ch76, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 168
Mean 29.75
Std Dev 4.11
Gaus mean : 30.4518
Gaus Width: 3.2928
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
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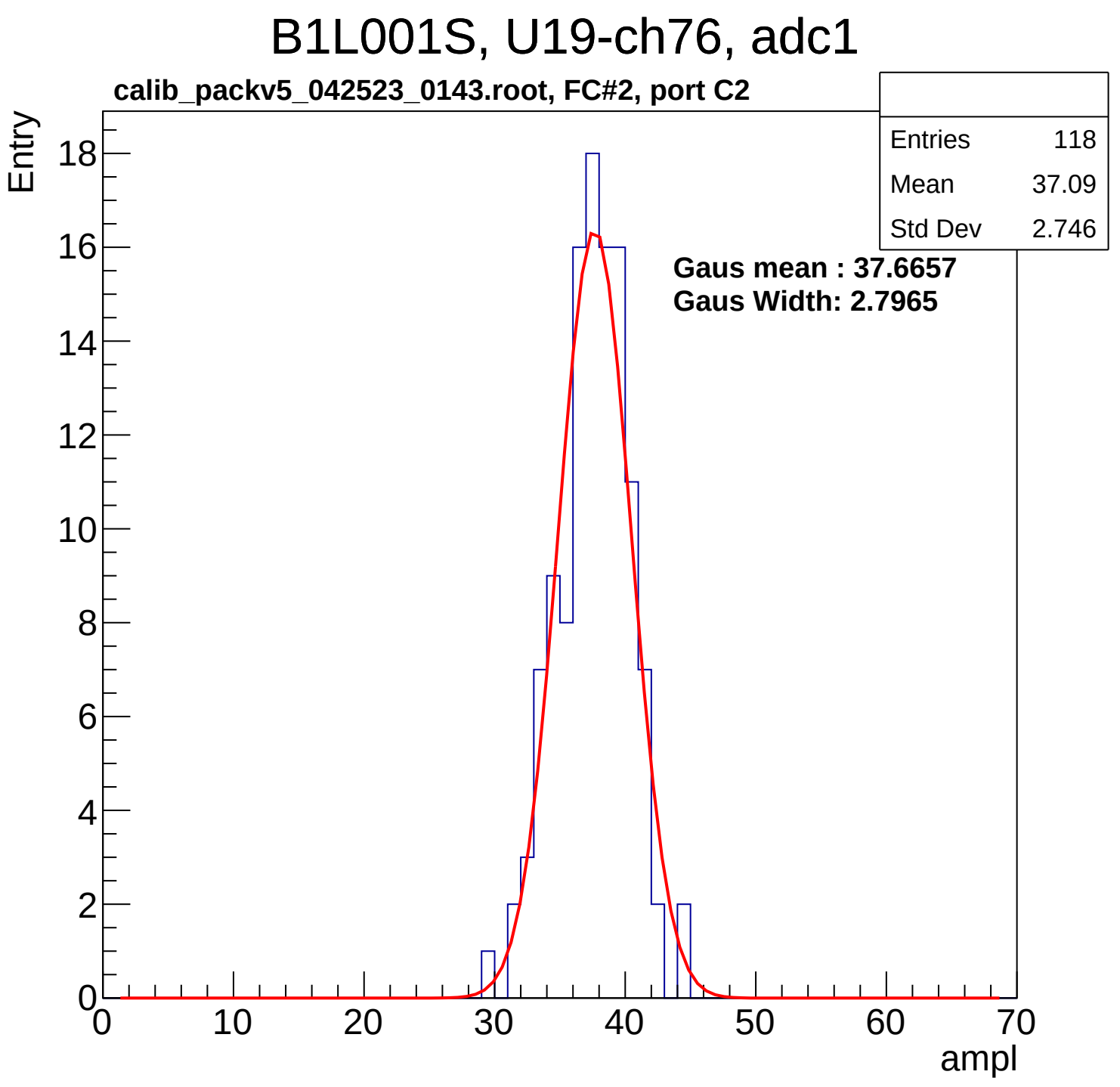
B1L001S, U19-ch76, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 118
Mean 37.09
Std Dev 2.746
Gaus mean : 37.6657
Gaus Width: 2.7965
Entry
ampl
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2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
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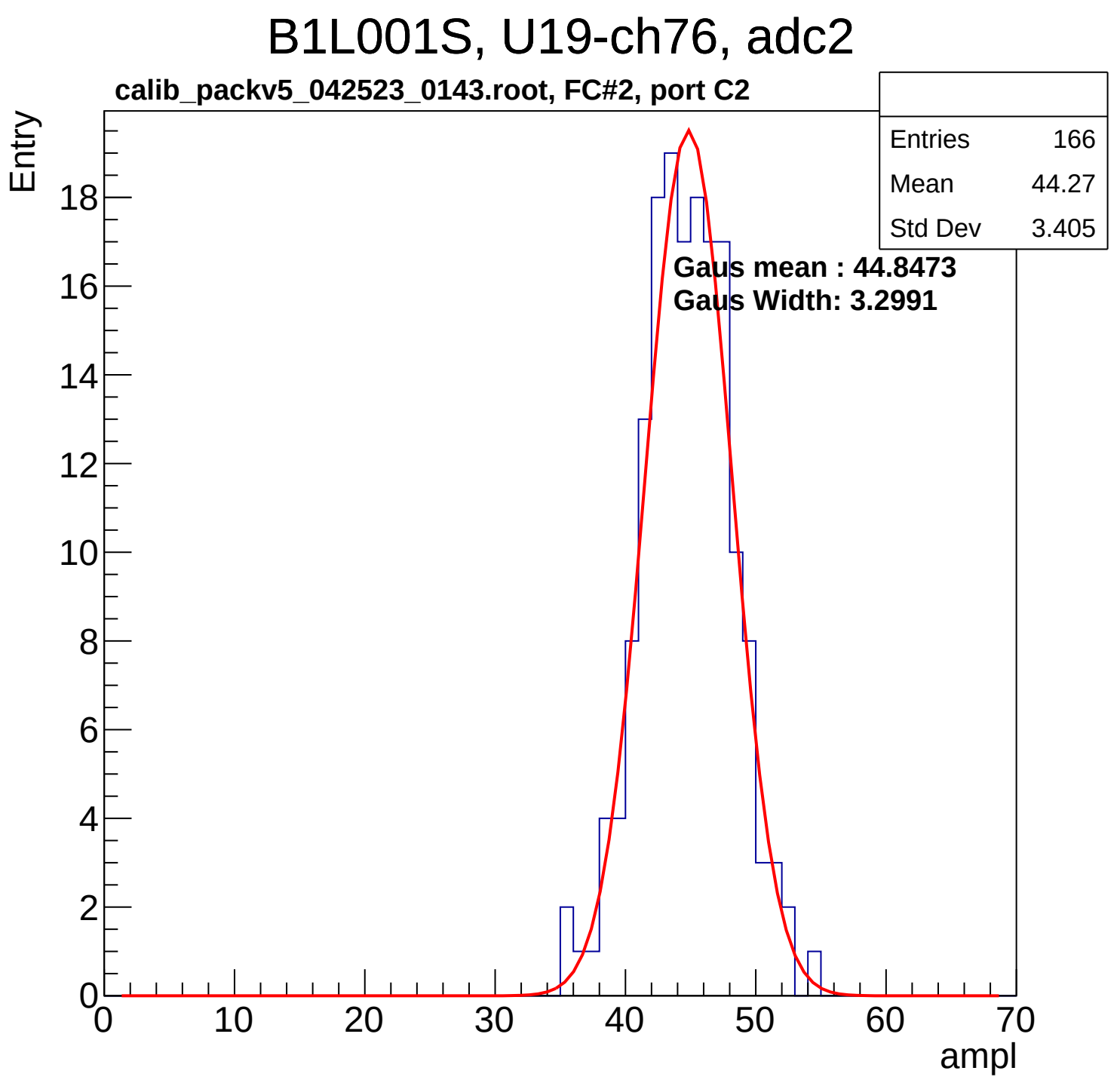
B1L001S, U19-ch76, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 166
Mean 44.27
Std Dev 3.405
Gaus mean : 44.8473
Gaus Width: 3.2991
Entry
ampl
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4
6
8
10
12
14
16
18
0
10
20
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40
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60
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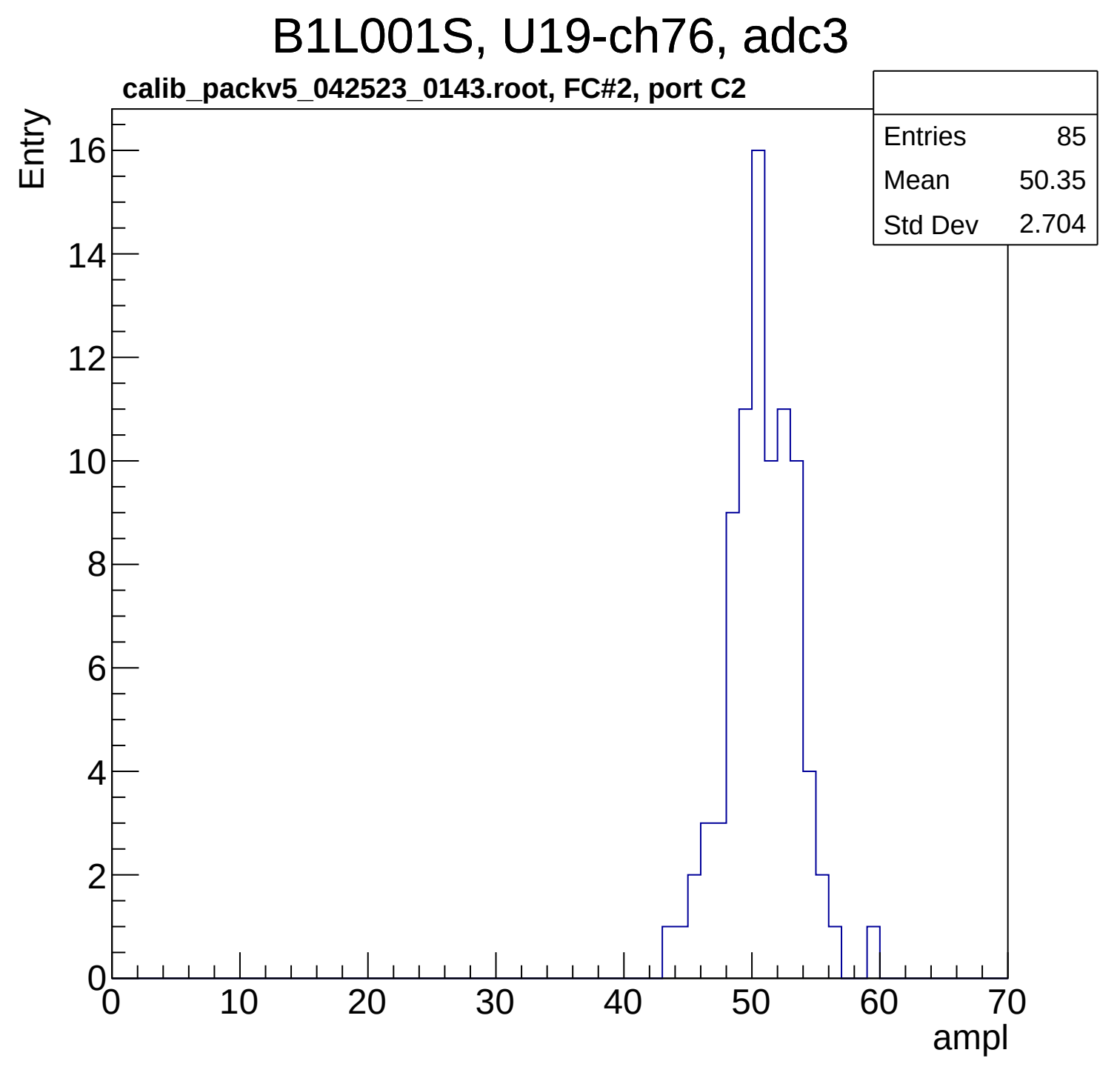
B1L001S, U19-ch76, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 85
Mean 50.35
Std Dev 2.704
Entry
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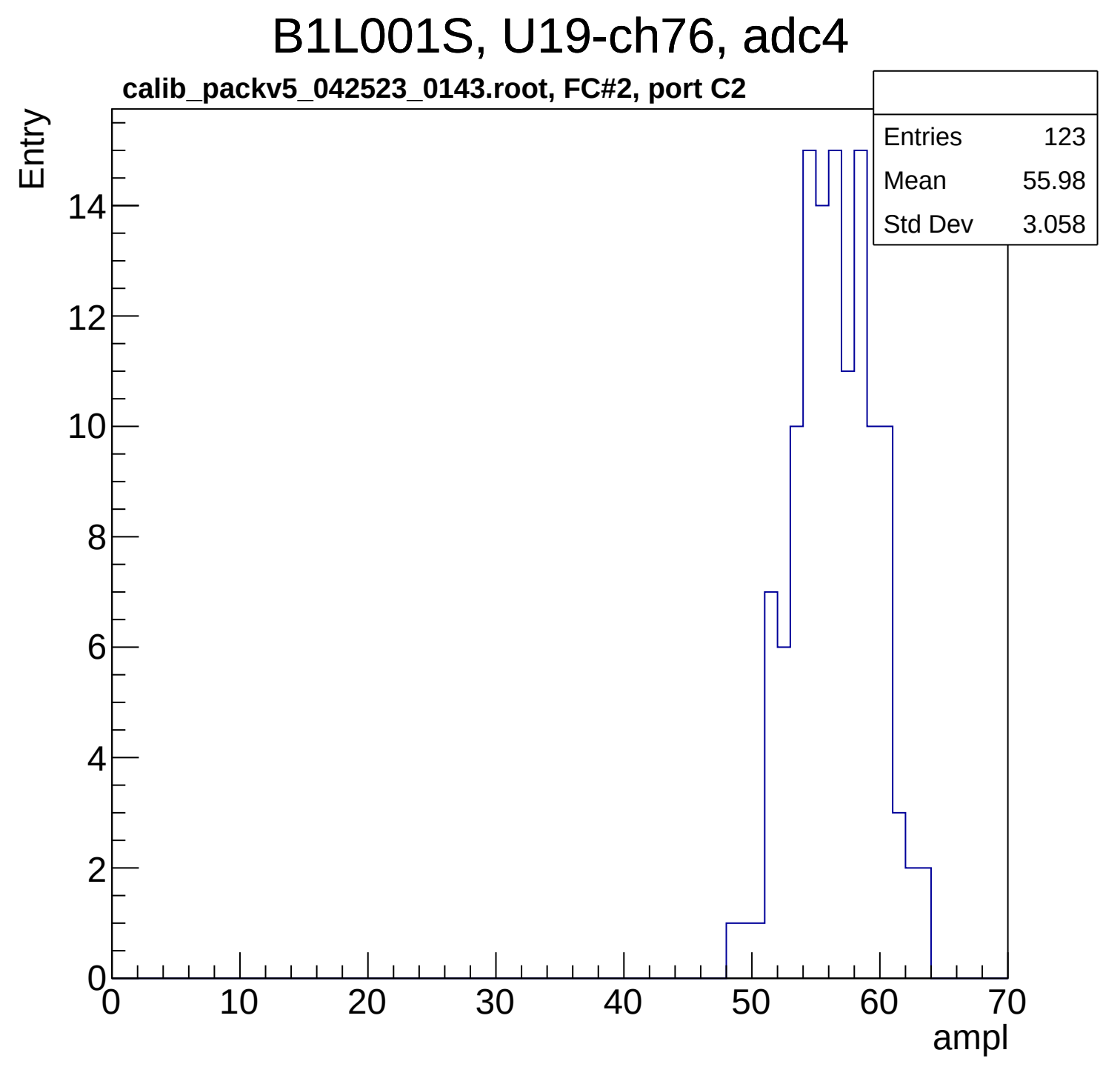
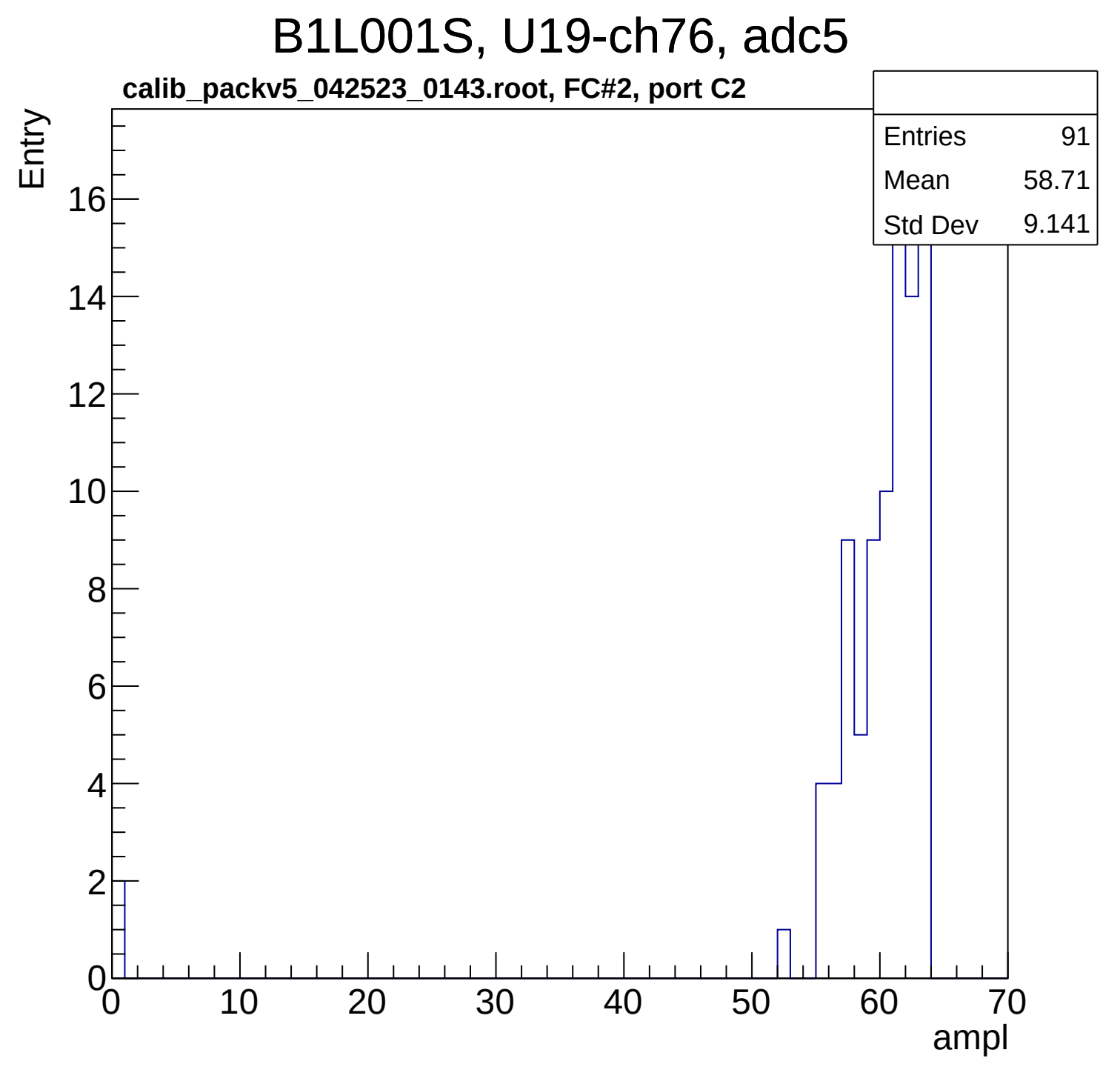
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch76, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 123
Mean 55.98
Std Dev 3.058
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch76, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 91
Mean 58.71
Std Dev 9.141
Entry
ampl
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2
4
6
8
10
12
14
16
0
10
20
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40
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60
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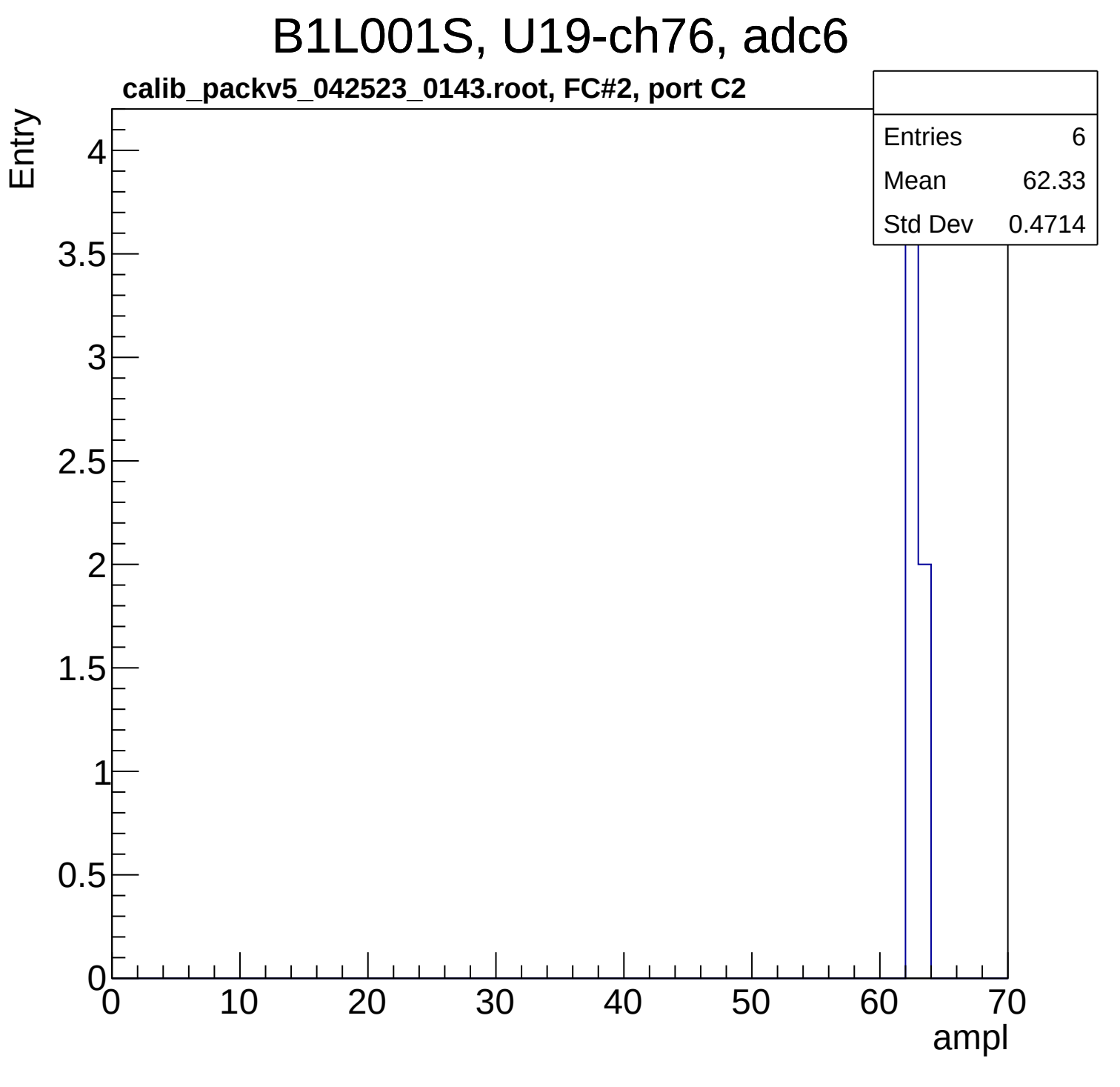
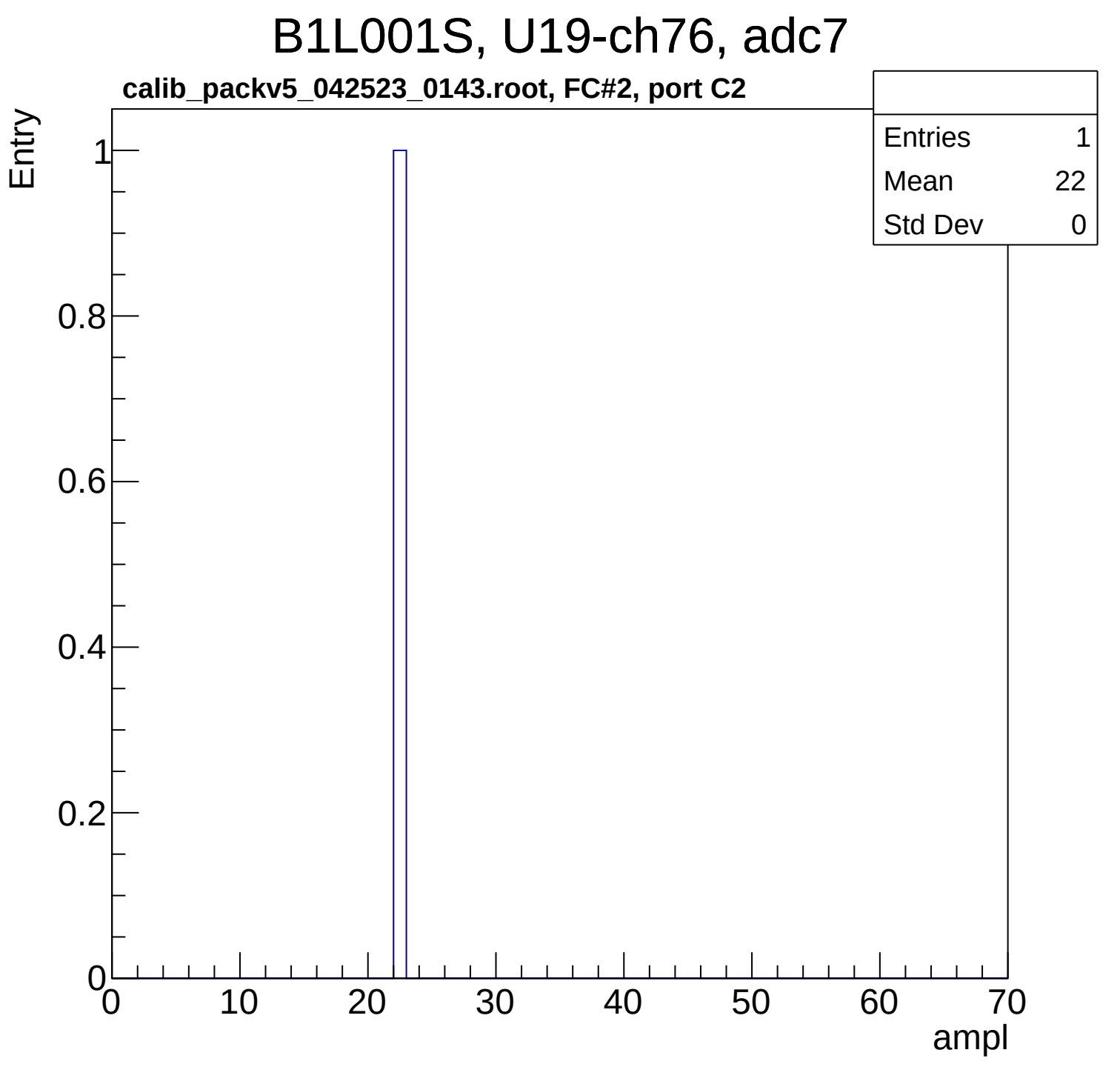
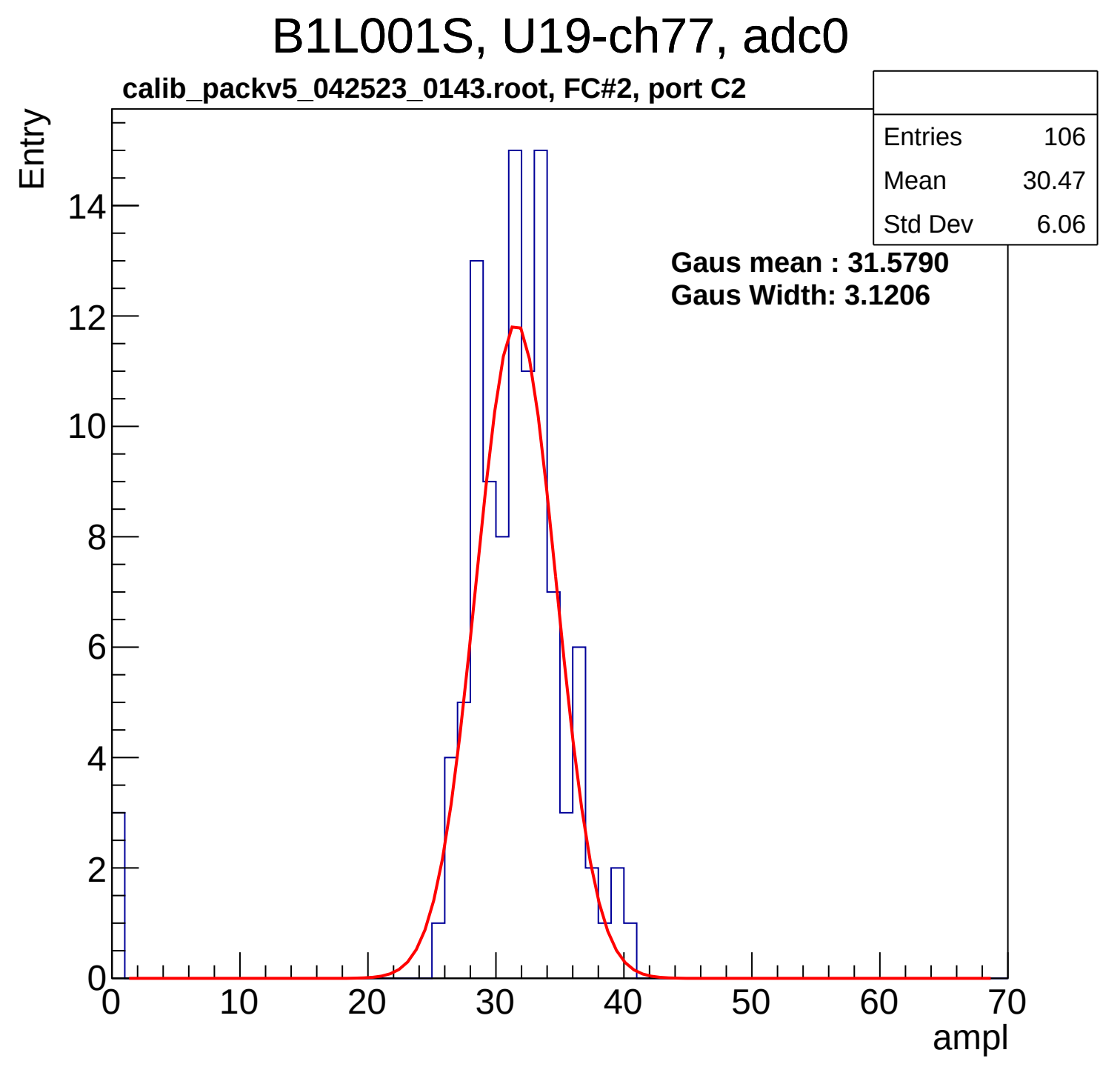
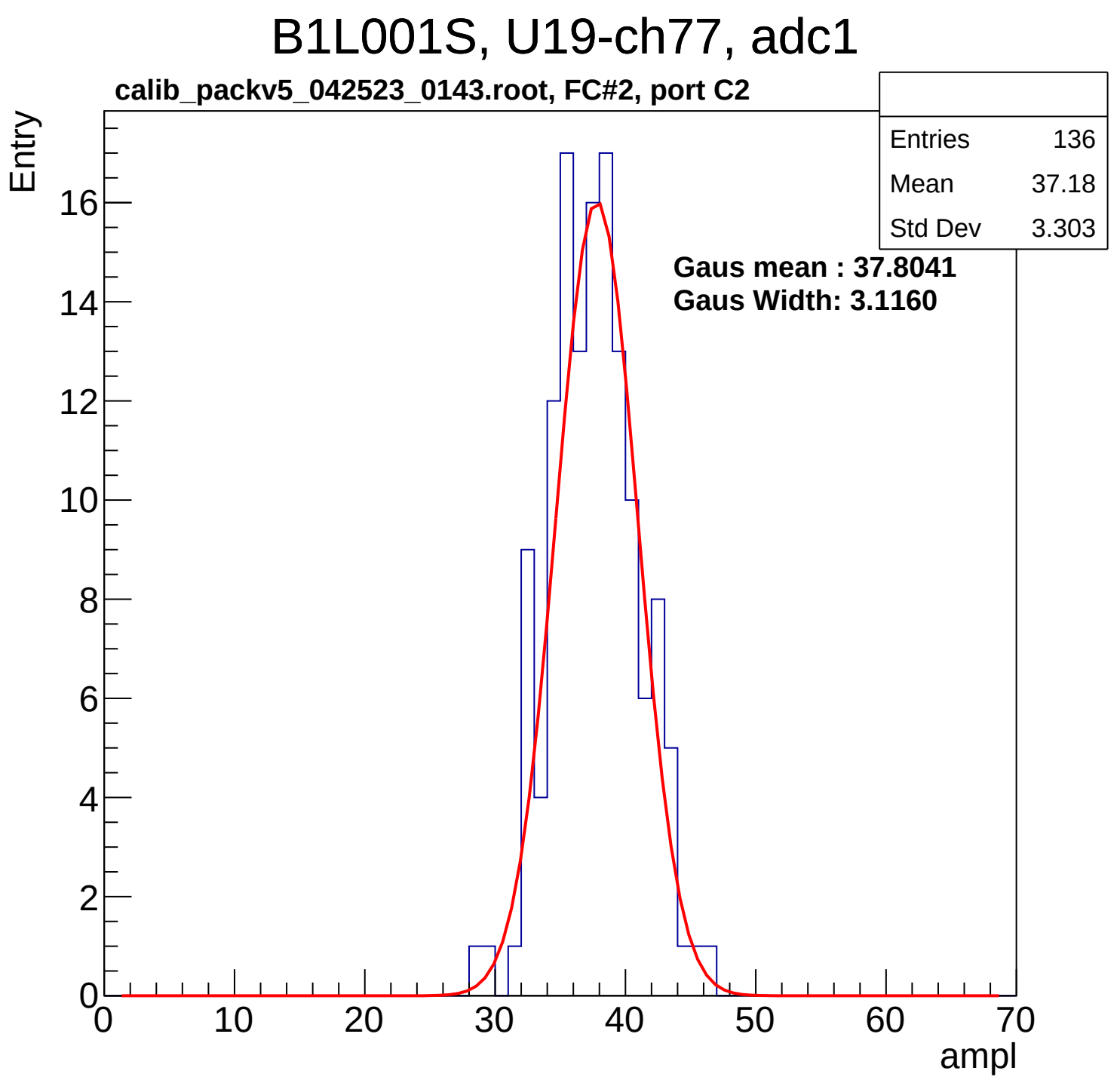
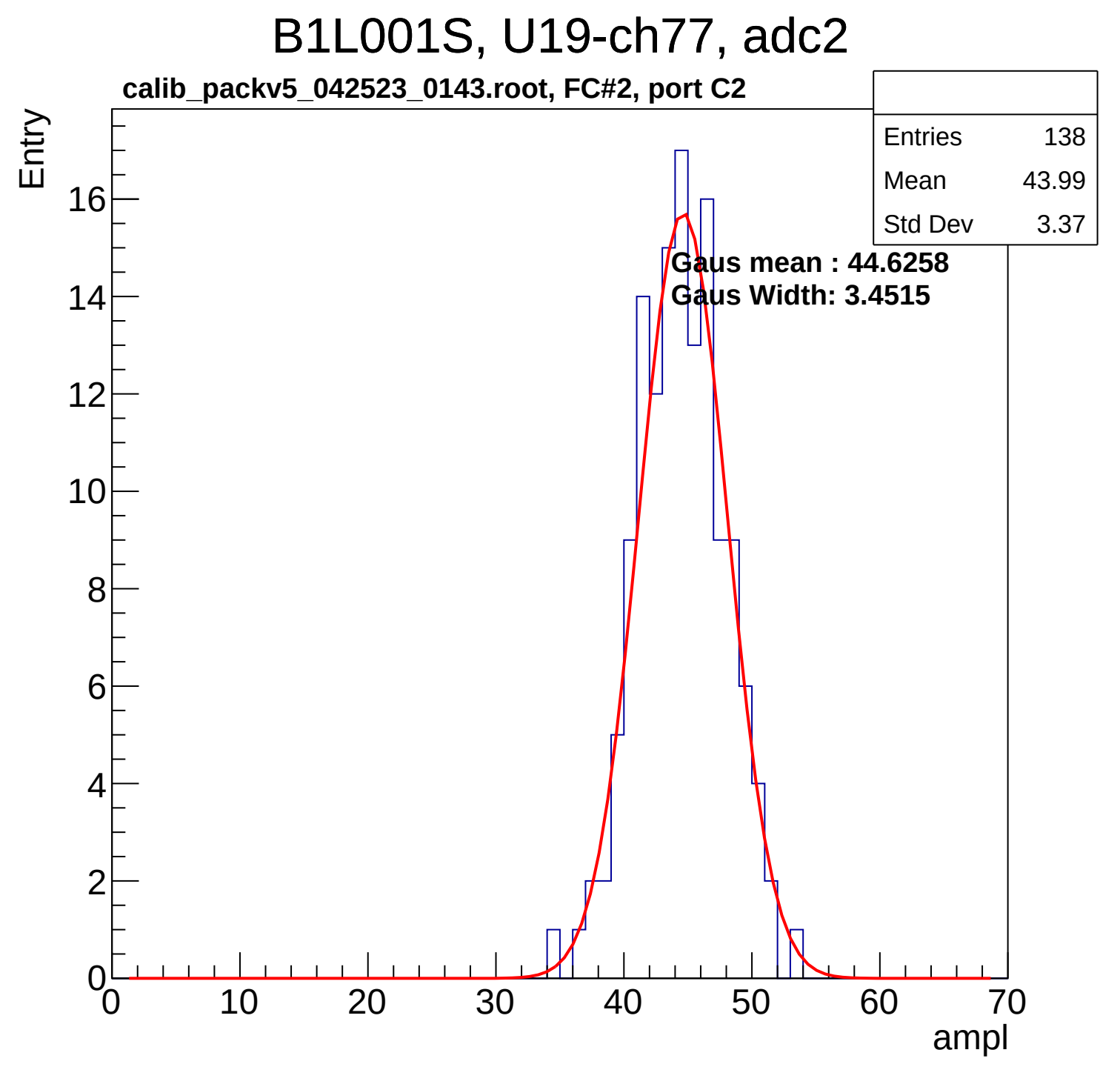

B1L001S, U19-ch76, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 6
Mean 62.33
Std Dev 0.4714
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L001S, U19-ch76, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 22
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch77, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 106
Mean 30.47
Std Dev 6.06
Gaus mean : 31.5790
Gaus Width: 3.1206
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L001S, U19-ch77, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 136
Mean 37.18
Std Dev 3.303
Gaus mean : 37.8041
Gaus Width: 3.1160
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70


B1L001S, U19-ch77, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 138
Mean 43.99
Std Dev 3.37
Gaus mean : 44.6258
Gaus Width: 3.4515
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
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40
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60
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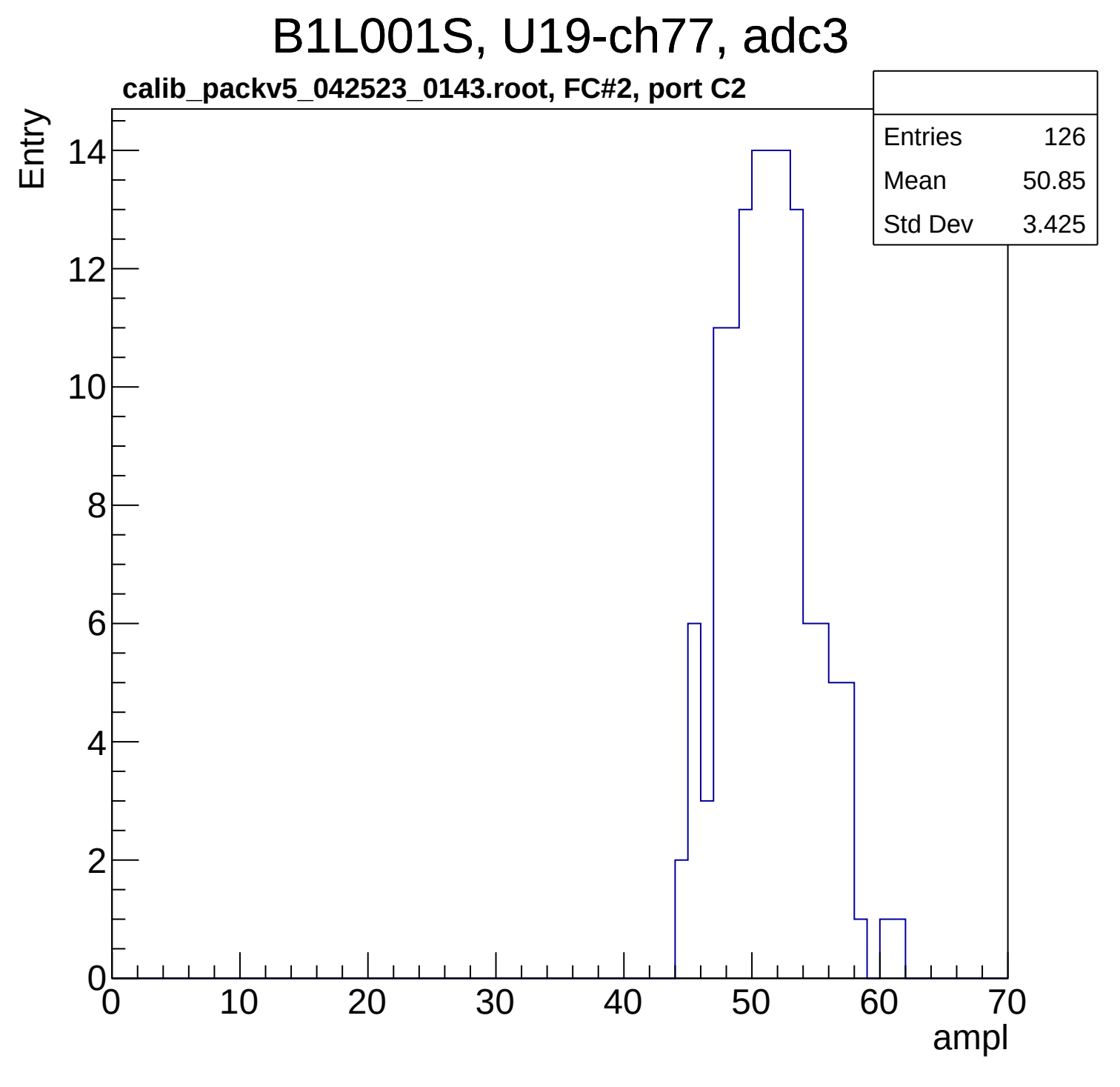
B1L001S, U19-ch77, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 126
Mean 50.85
Std Dev 3.425
Entry
ampl
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8
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0
10
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60
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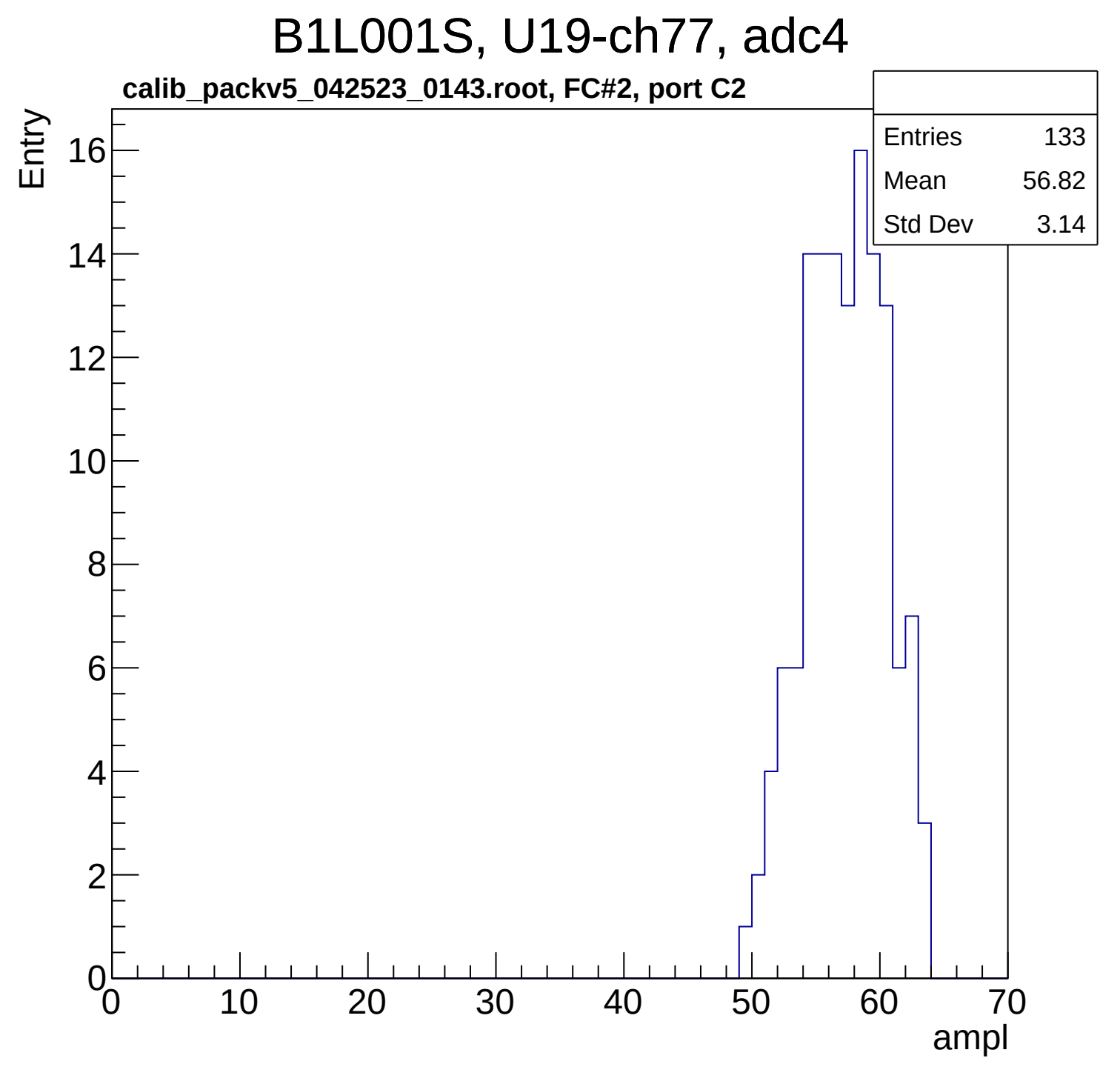
B1L001S, U19-ch77, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 133
Mean 56.82
Std Dev 3.14
Entry
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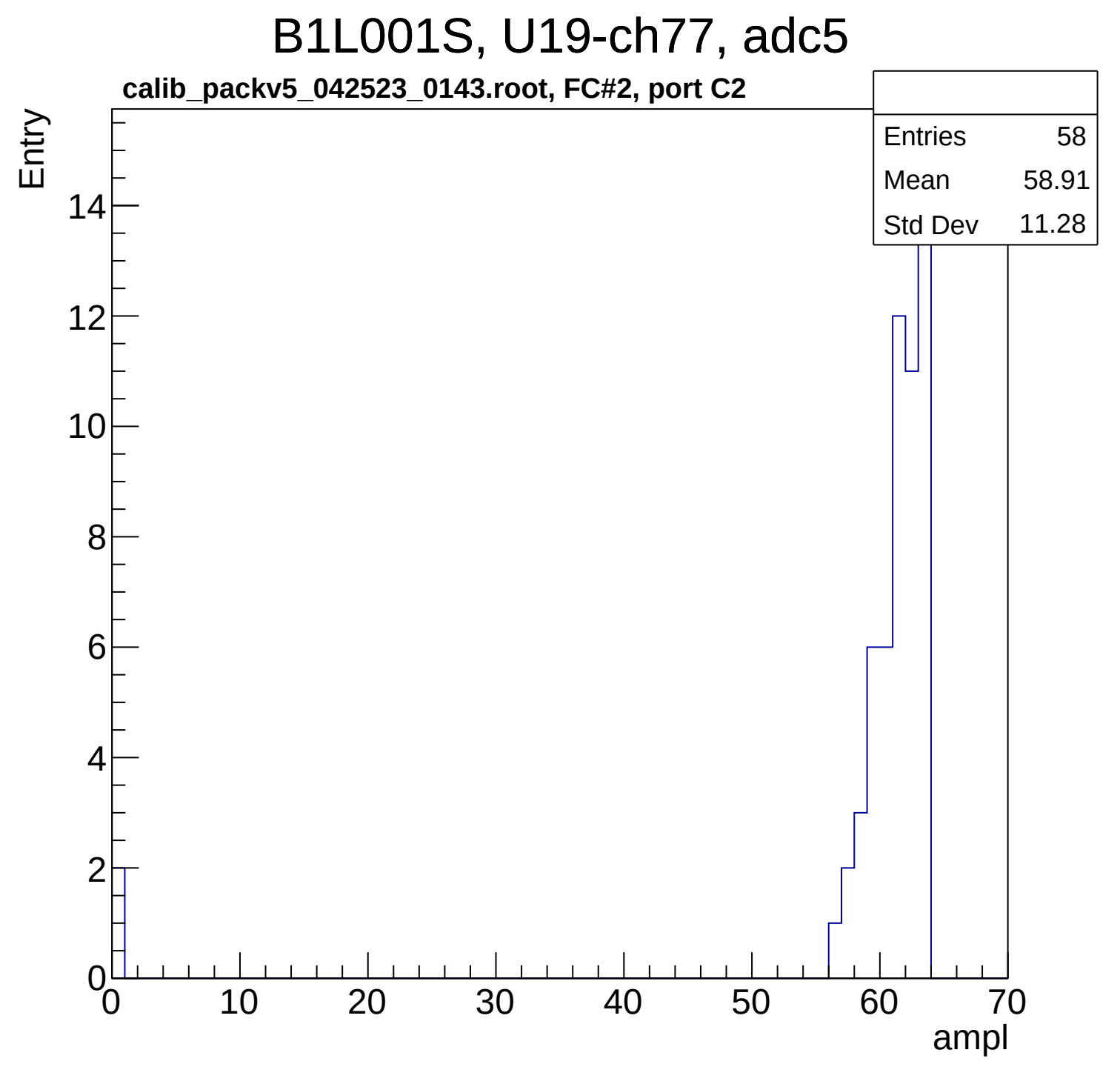
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch77, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 58
Mean 58.91
Std Dev 11.28
Entry
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2
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6
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10
12
14
0
10
20
30
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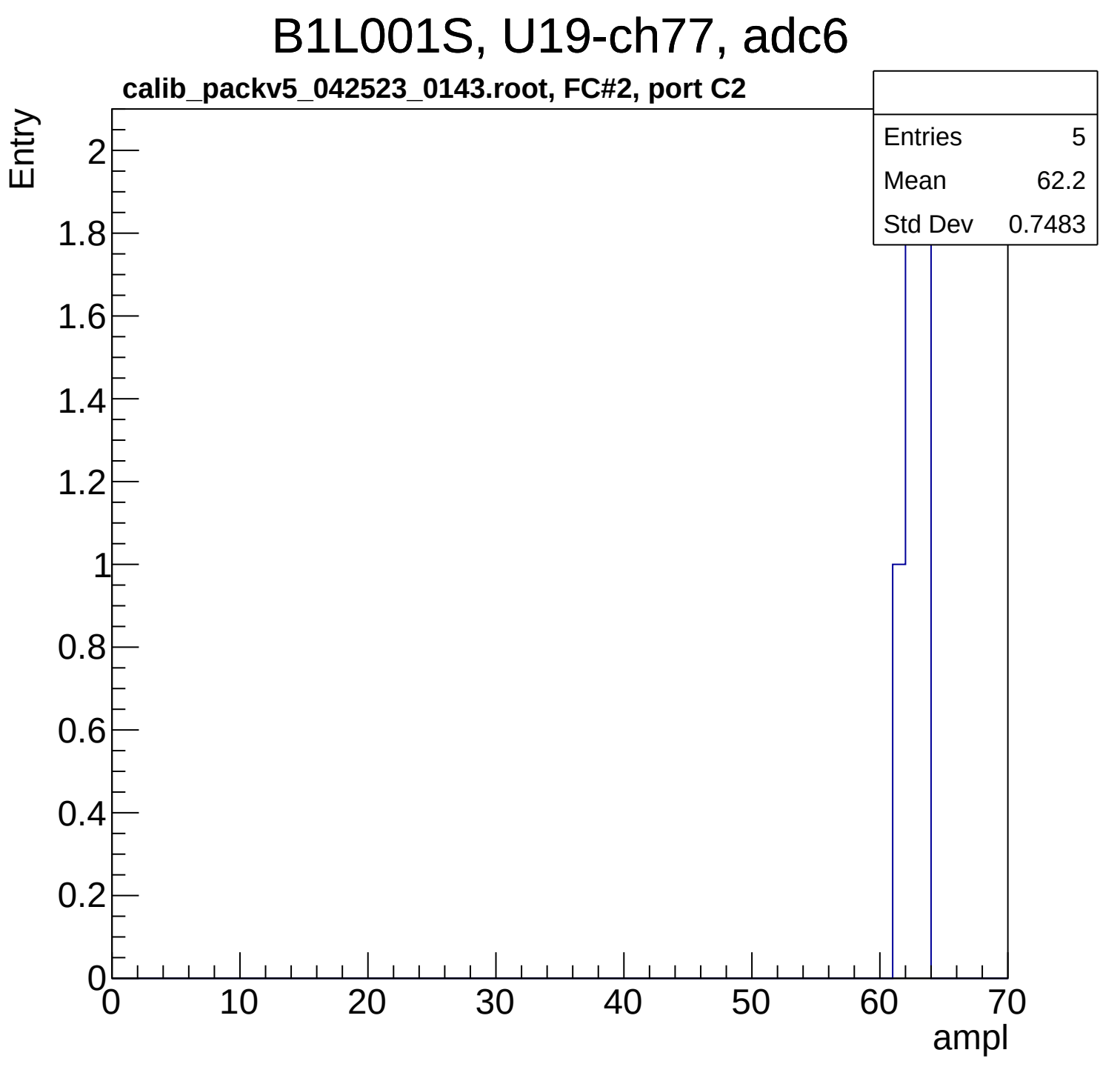
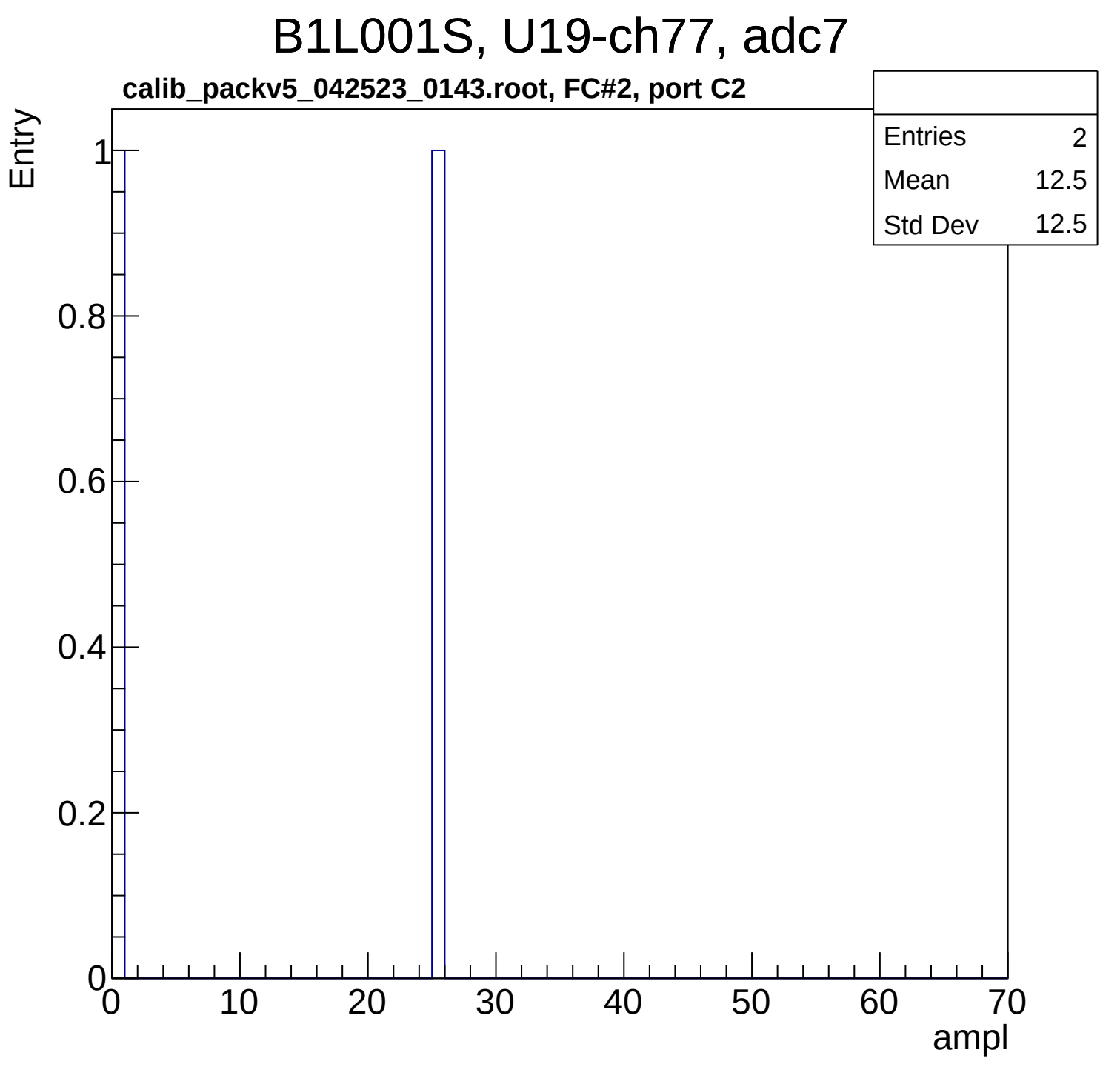
50
60
70
ampl


B1L001S, U19-ch77, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 5
Mean 62.2
Std Dev 0.7483
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L001S, U19-ch77, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 12.5
Std Dev 12.5
Entry
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0.6
0.4
0.2
0
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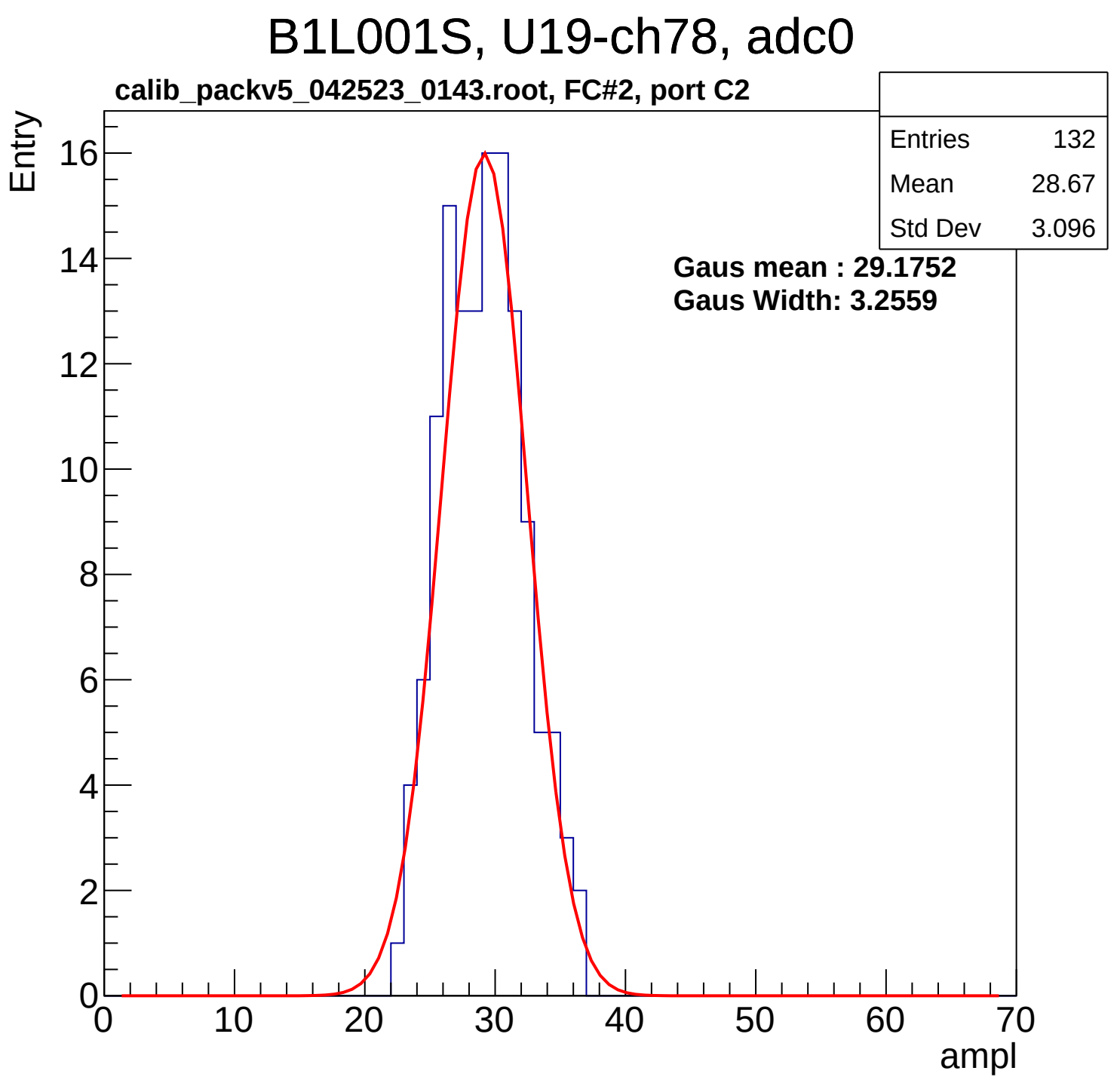
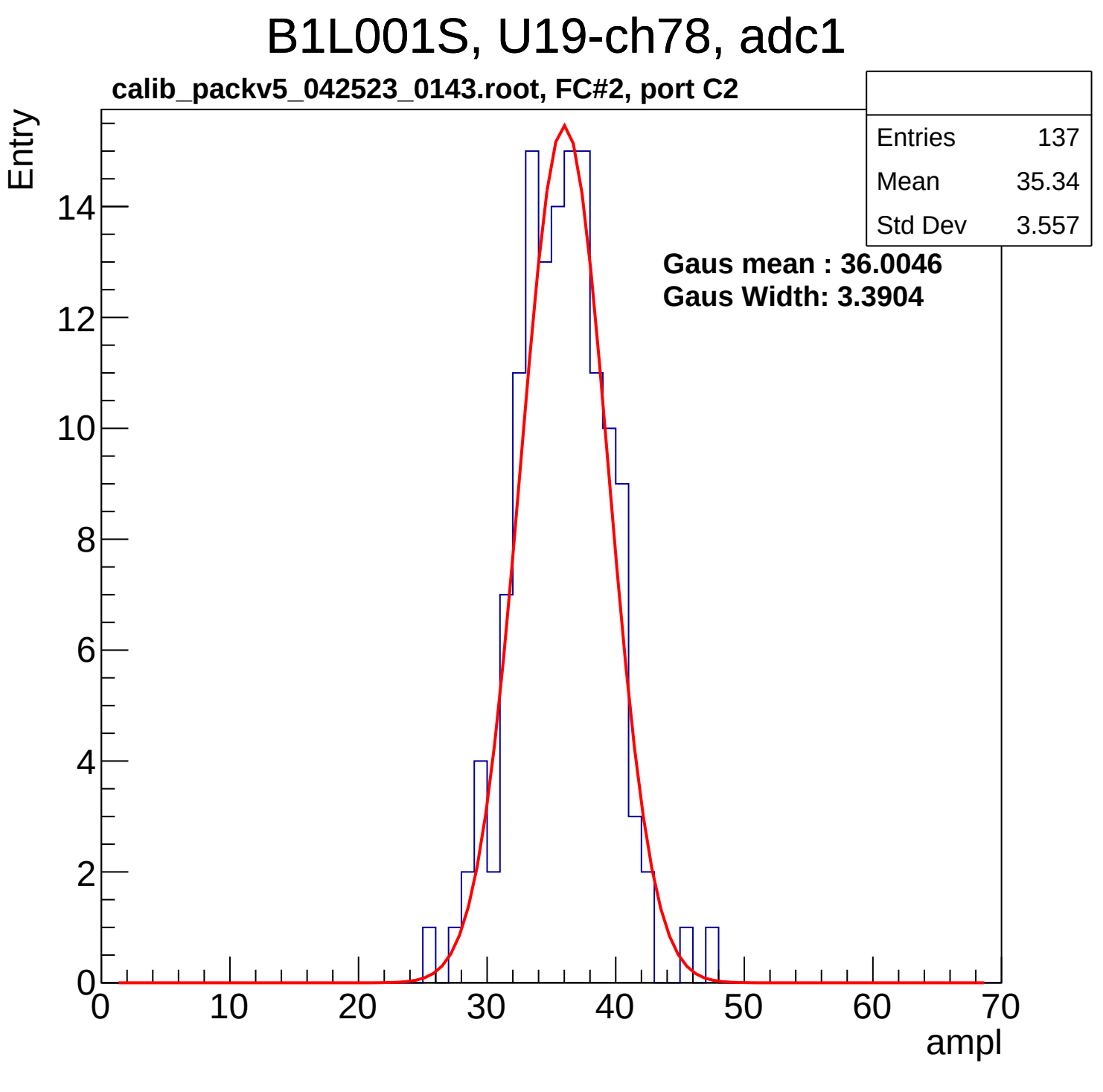
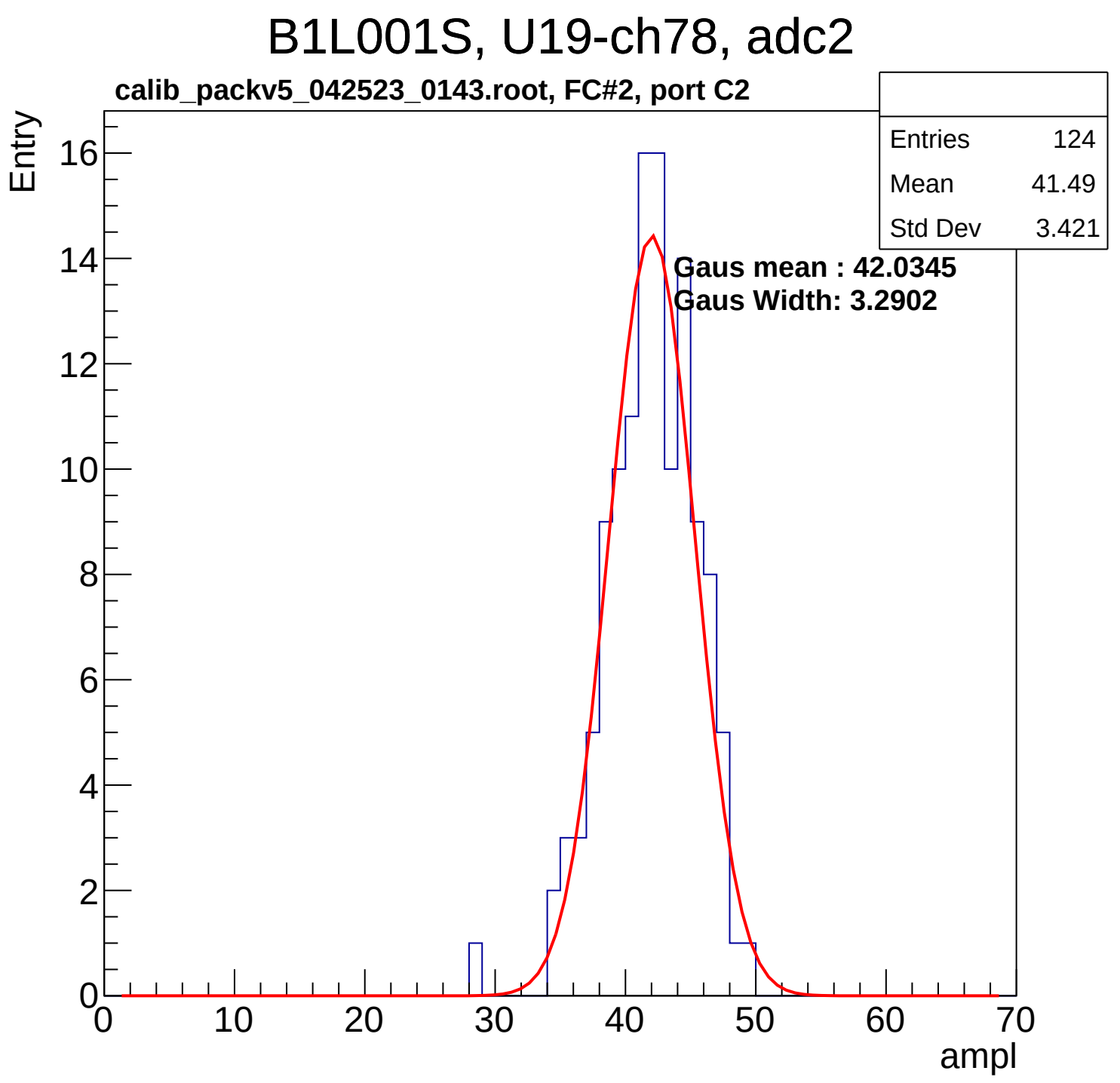
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch78, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 132
Mean 28.67
Std Dev 3.096
Gaus mean : 29.1752
Gaus Width: 3.2559
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70


B1L001S, U19-ch78, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 137
Mean 35.34
Std Dev 3.557
Gaus mean : 36.0046
Gaus Width: 3.3904
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L001S, U19-ch78, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 124
Mean 41.49
Std Dev 3.421
Gaus mean : 42.0345
Gaus Width: 3.2902
Entry
ampl
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2
4
6
8
10
12
14
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0
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60
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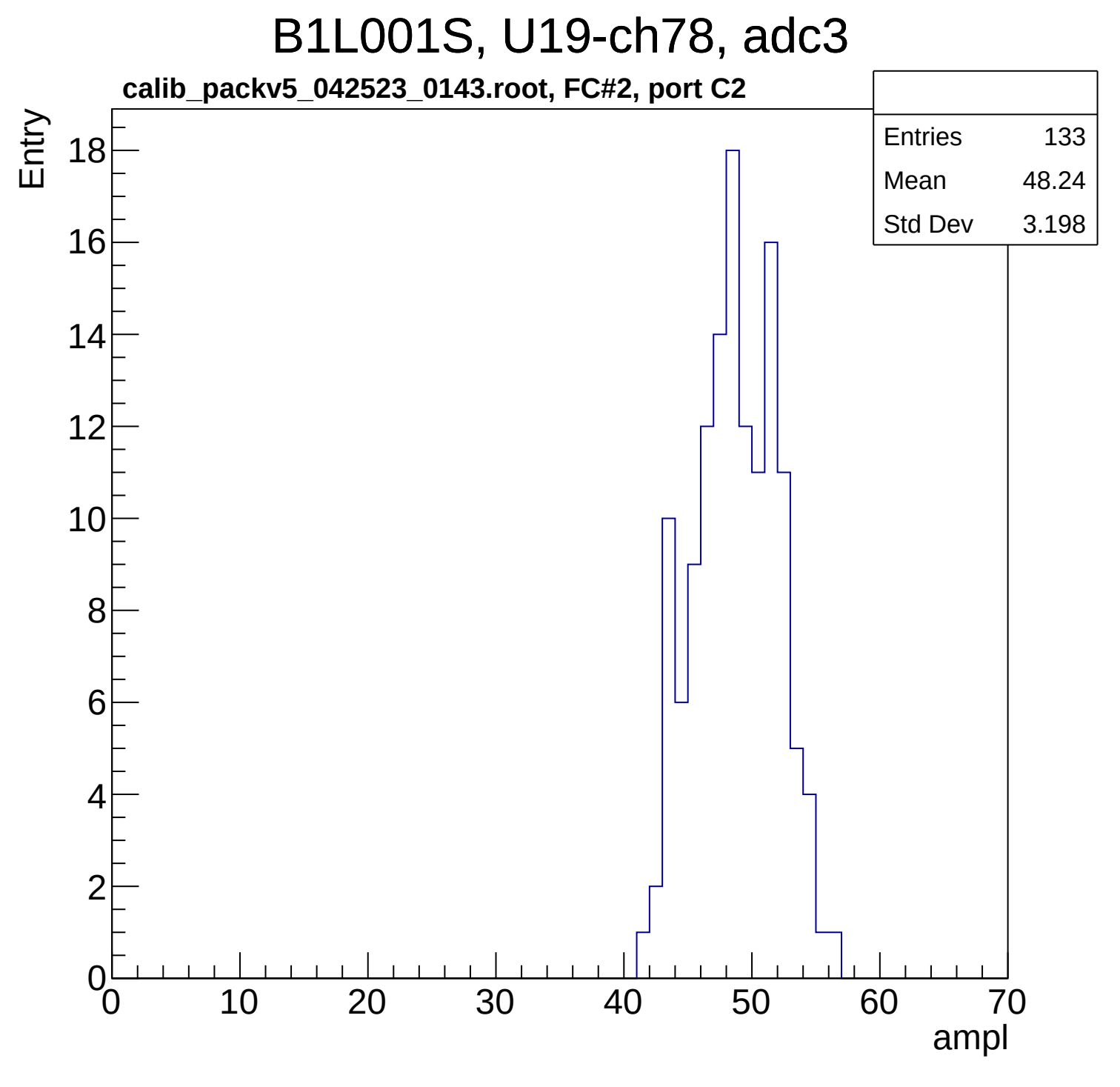
B1L001S, U19-ch78, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 133
Mean 48.24
Std Dev 3.198
Entry
ampl
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6
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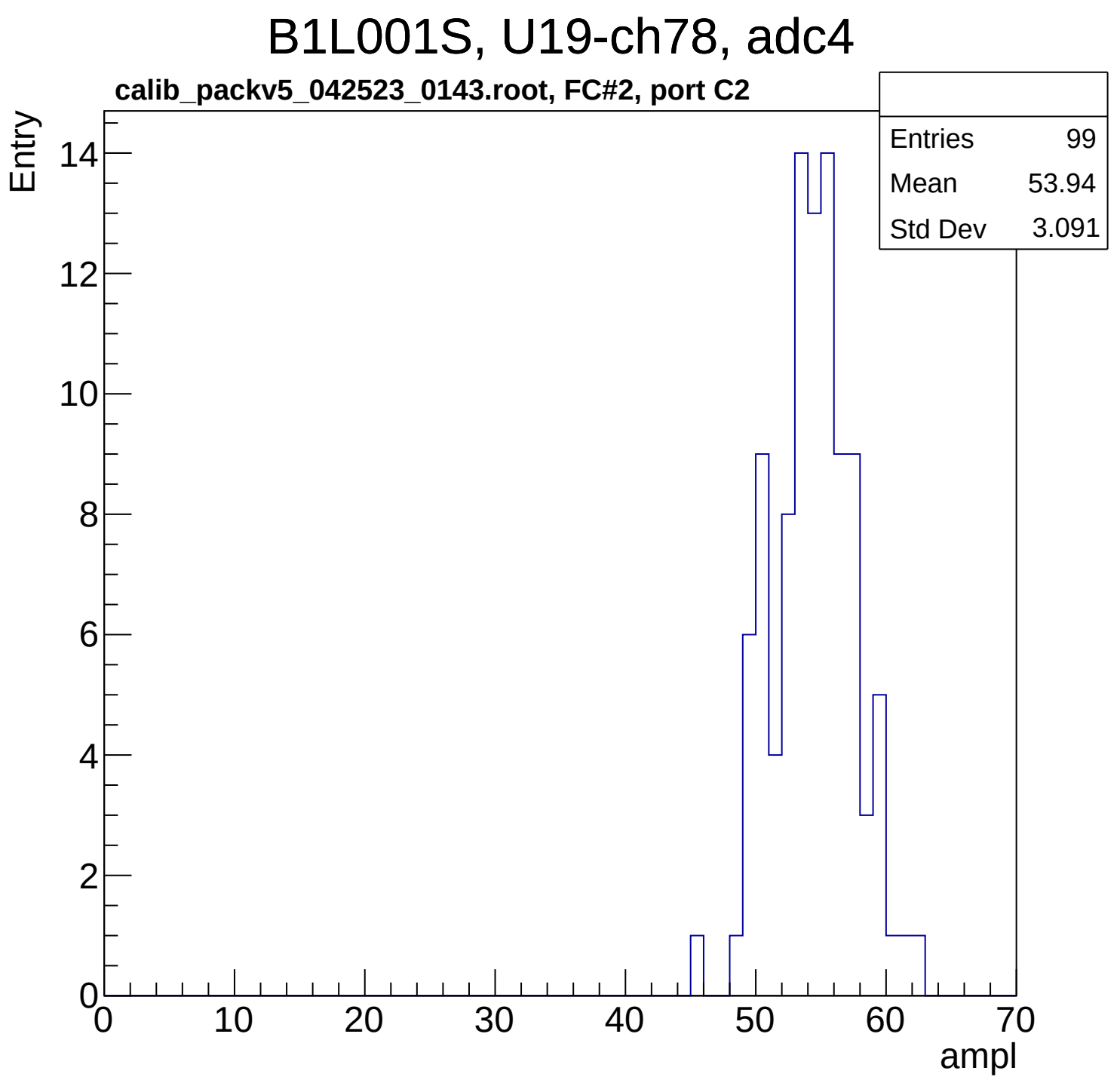
B1L001S, U19-ch78, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 99
Mean 53.94
Std Dev 3.091
Entry
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10
20
30
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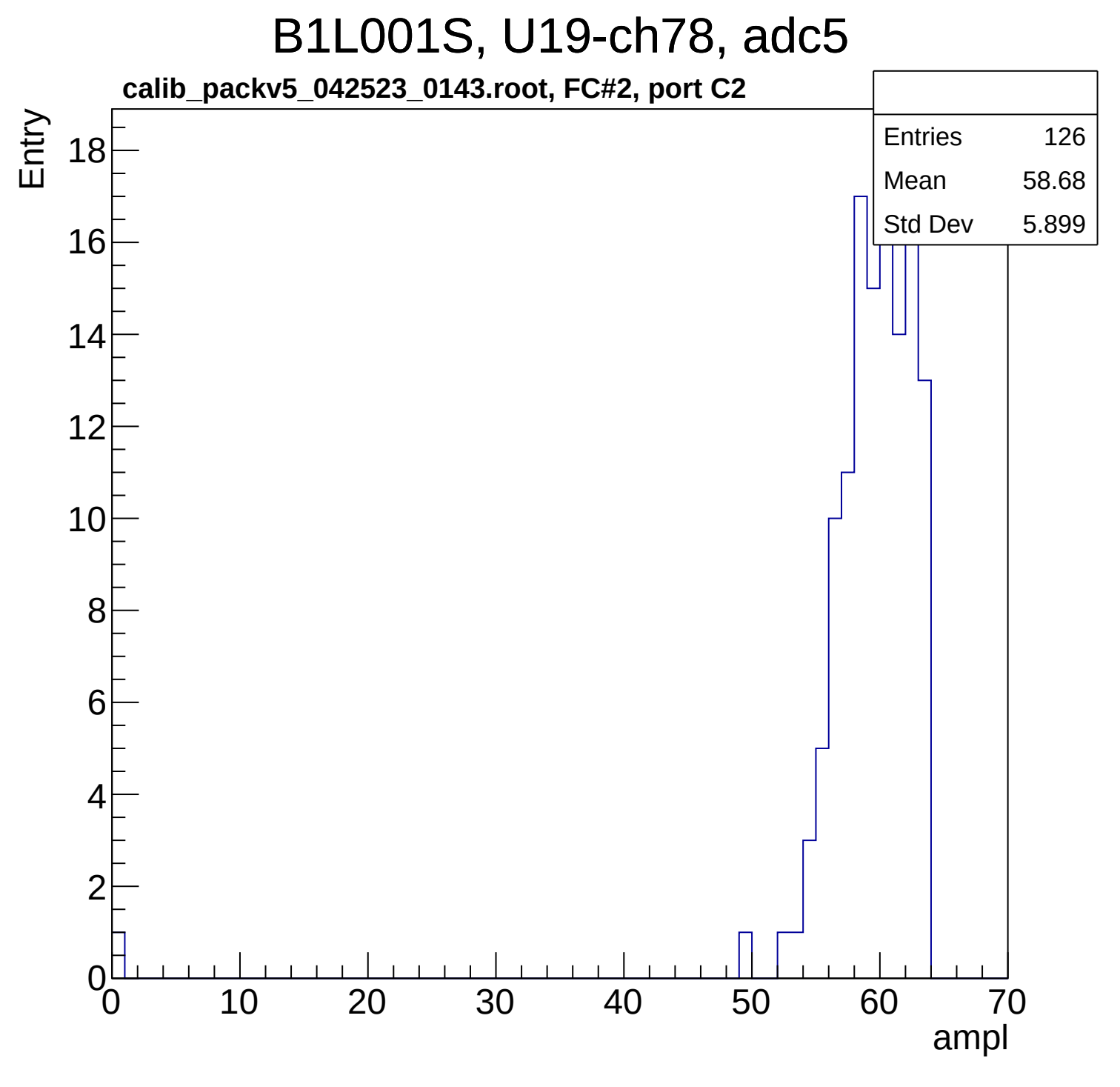
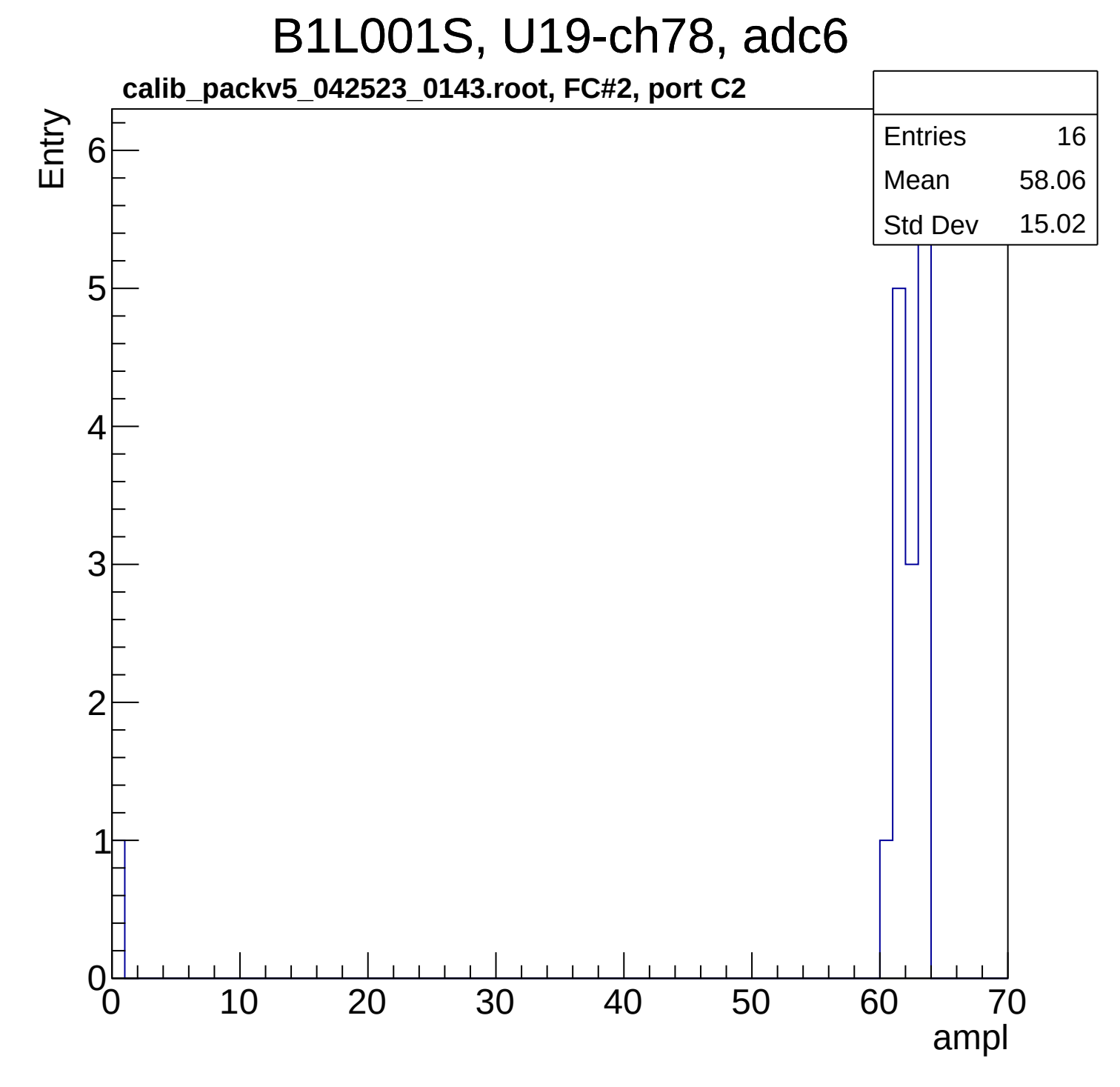
50
60
70
ampl


B1L001S, U19-ch78, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 126
Mean 58.68
Std Dev 5.899
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70


B1L001S, U19-ch78, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 16
Mean 58.06
Std Dev 15.02
Entry
ampl
0
1
2
3
4
5
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0
10
20
30
40
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60
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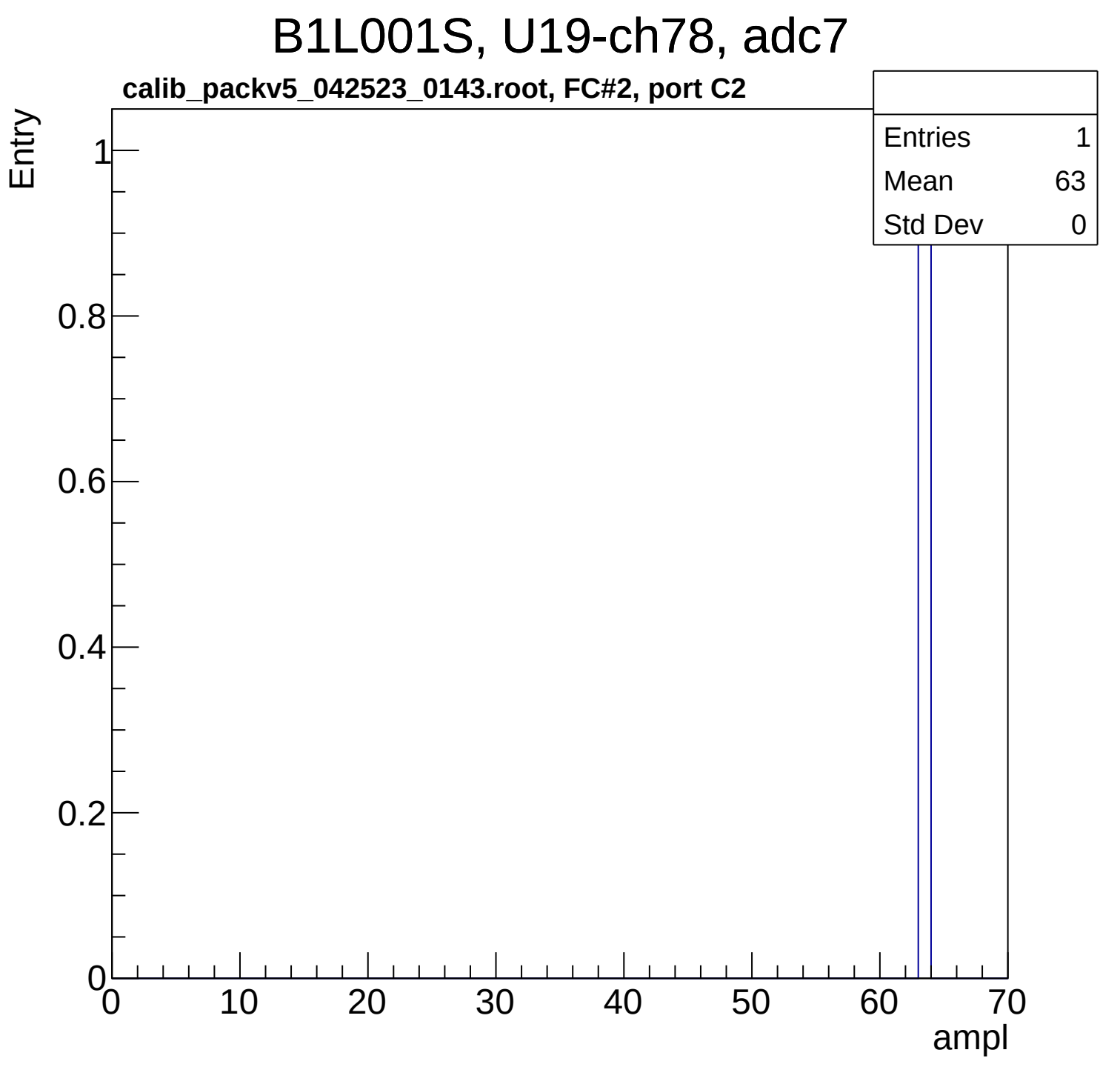
B1L001S, U19-ch78, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 63
Std Dev 0
Entry
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0.8
0.6
0.4
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10
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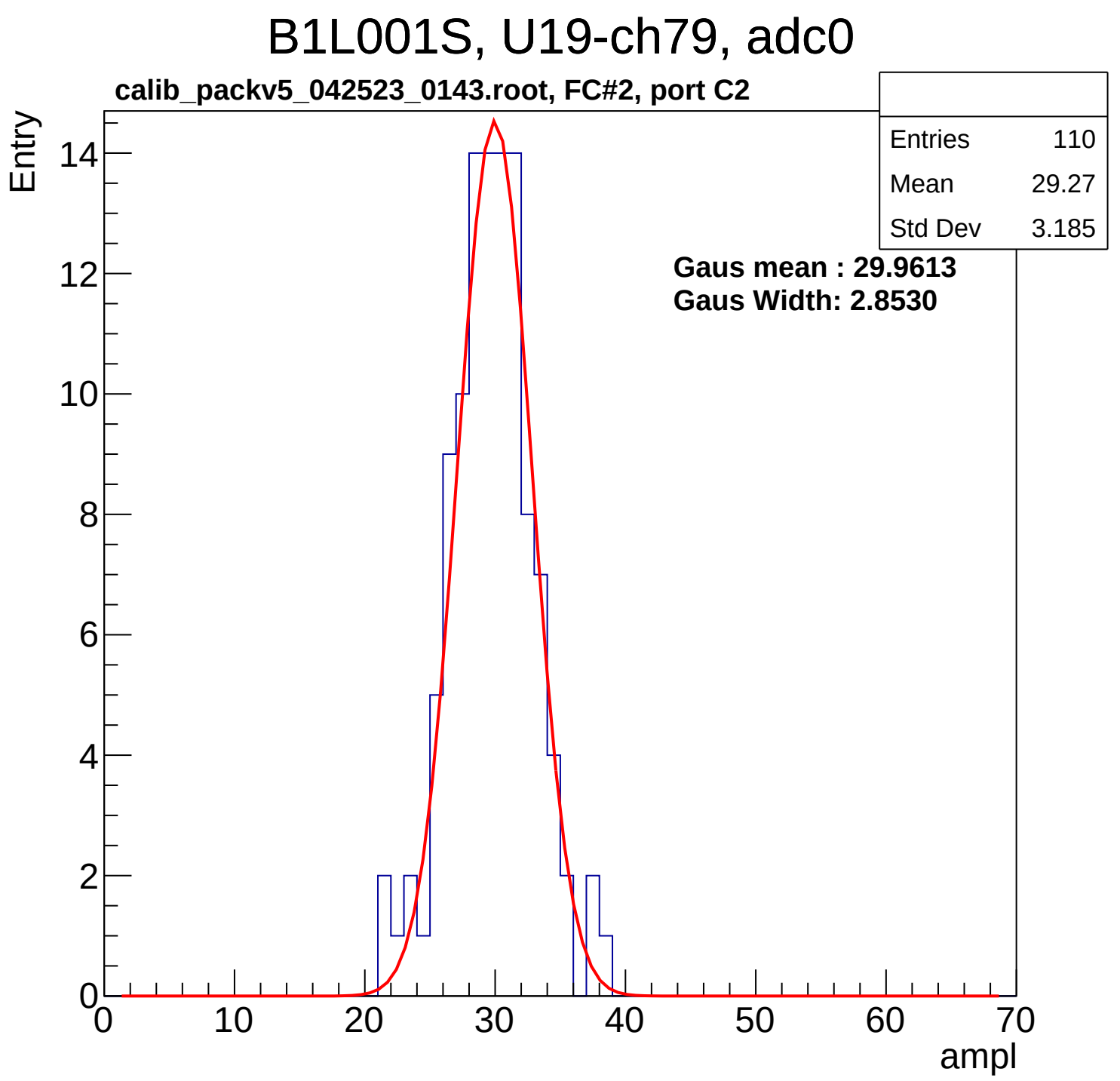
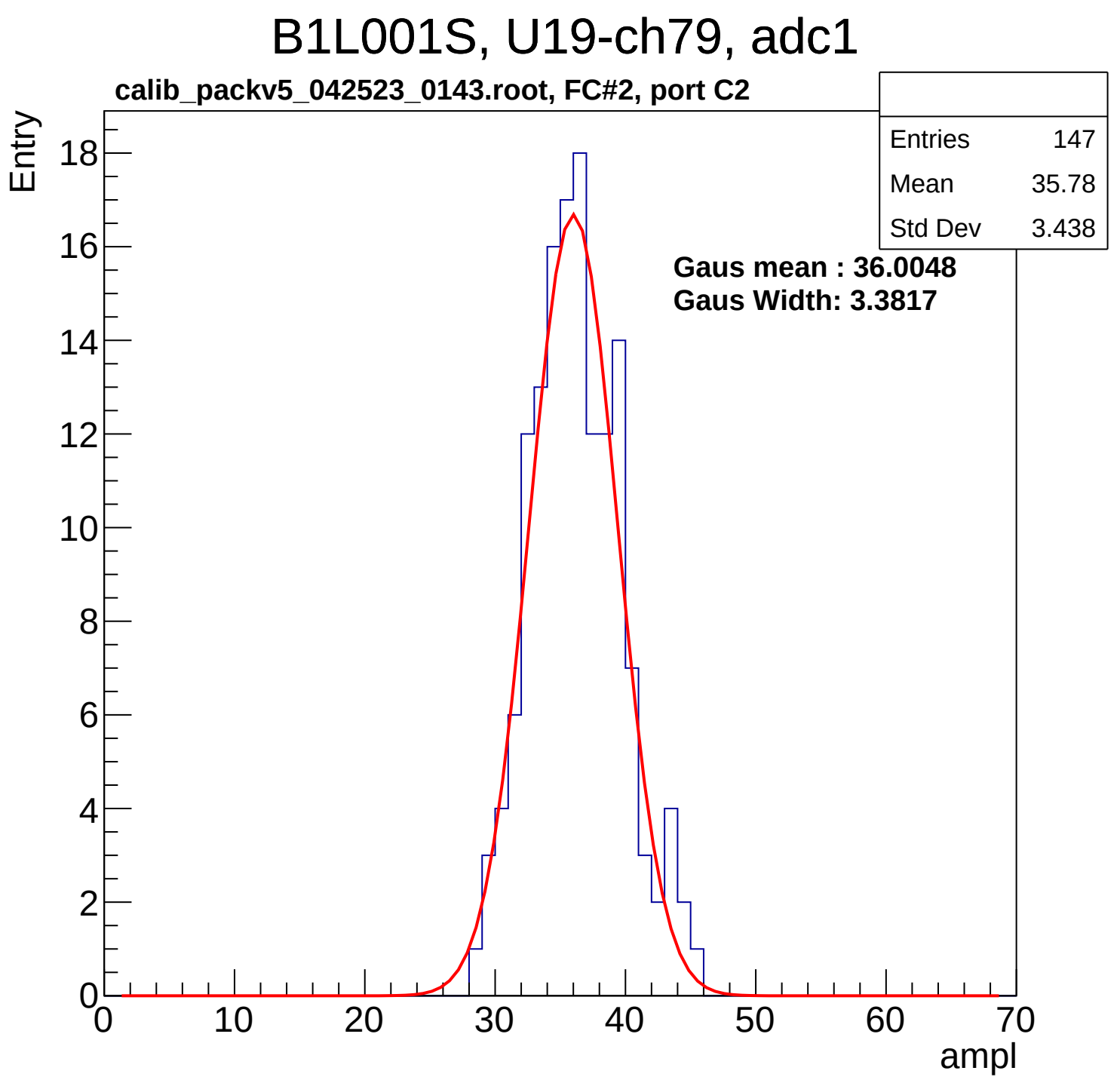
50
60
70
ampl


B1L001S, U19-ch79, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 110
Mean 29.27
Std Dev 3.185
Gaus mean : 29.9613
Gaus Width: 2.8530
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L001S, U19-ch79, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 147
Mean 35.78
Std Dev 3.438
Gaus mean : 36.0048
Gaus Width: 3.3817
Entry
ampl
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4
6
8
10
12
14
16
18
0
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40
50
60
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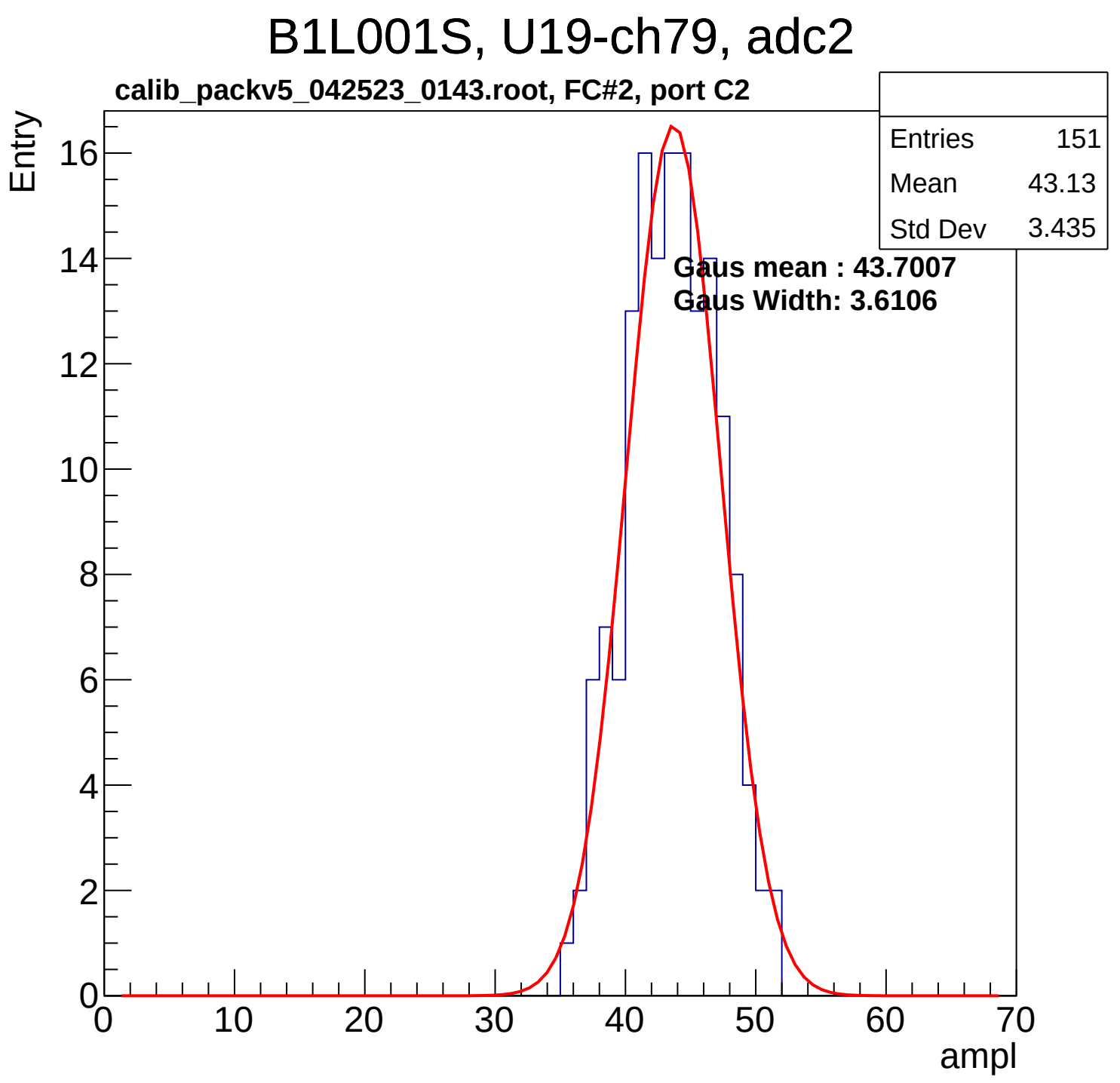
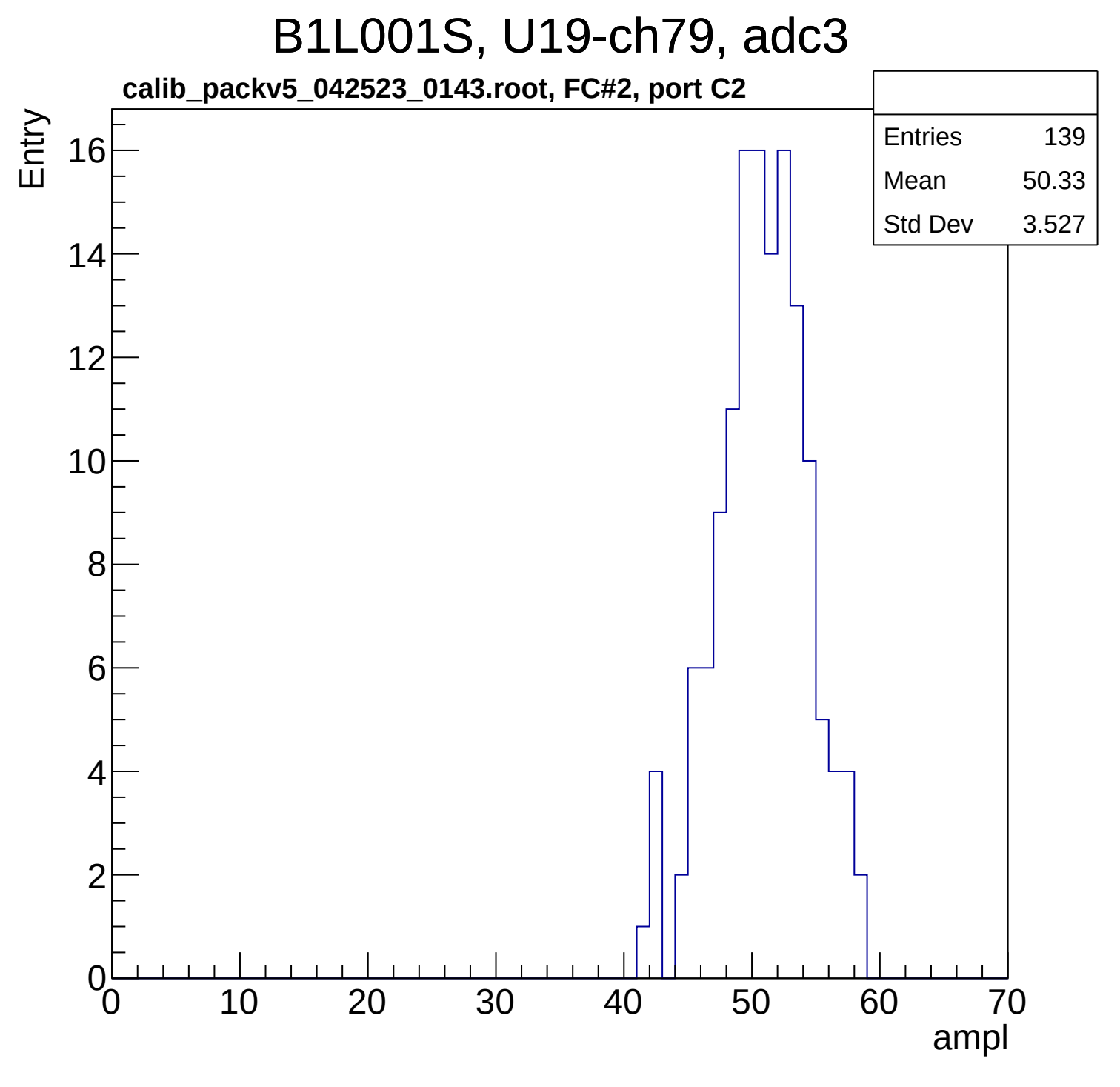
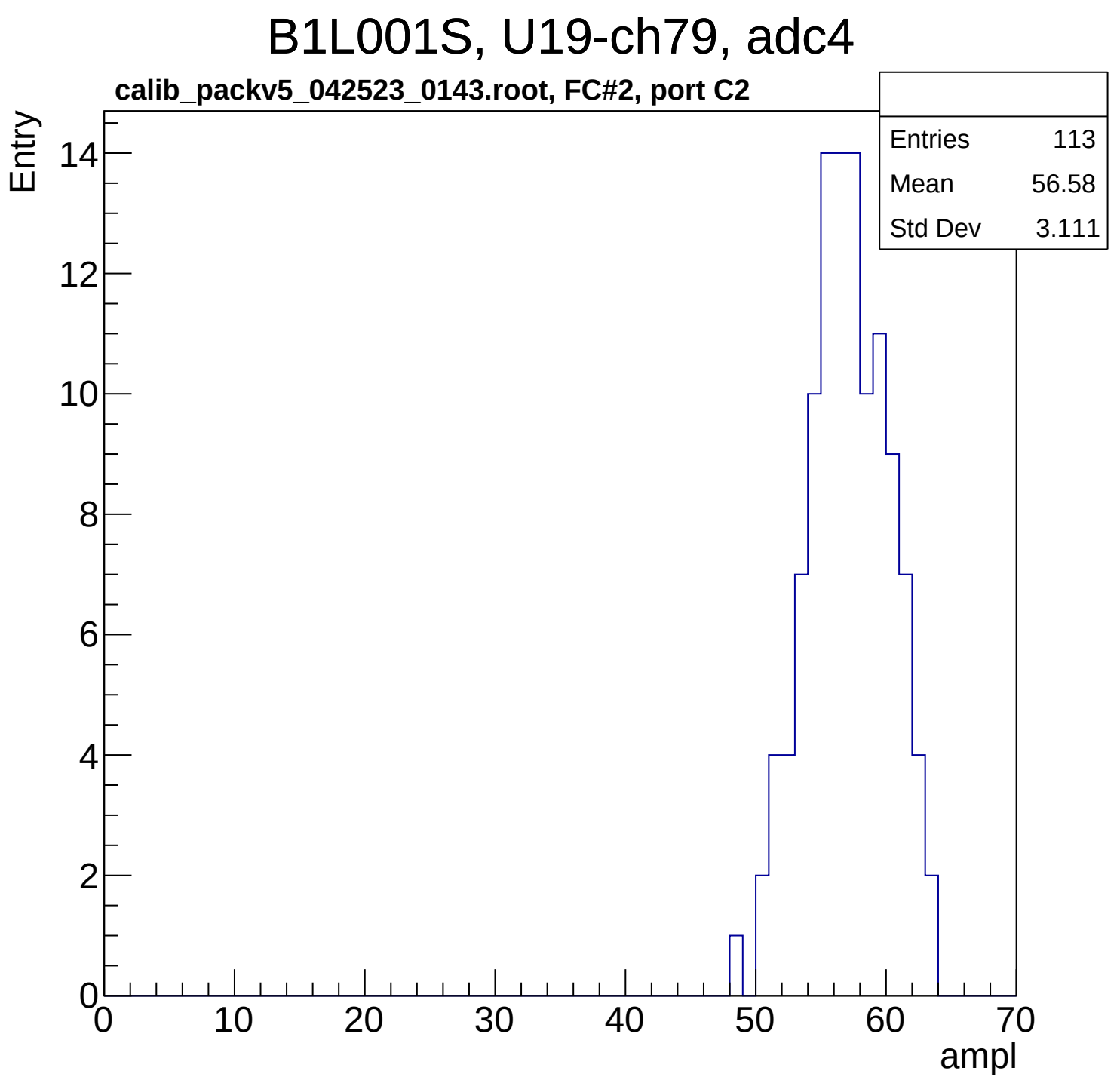
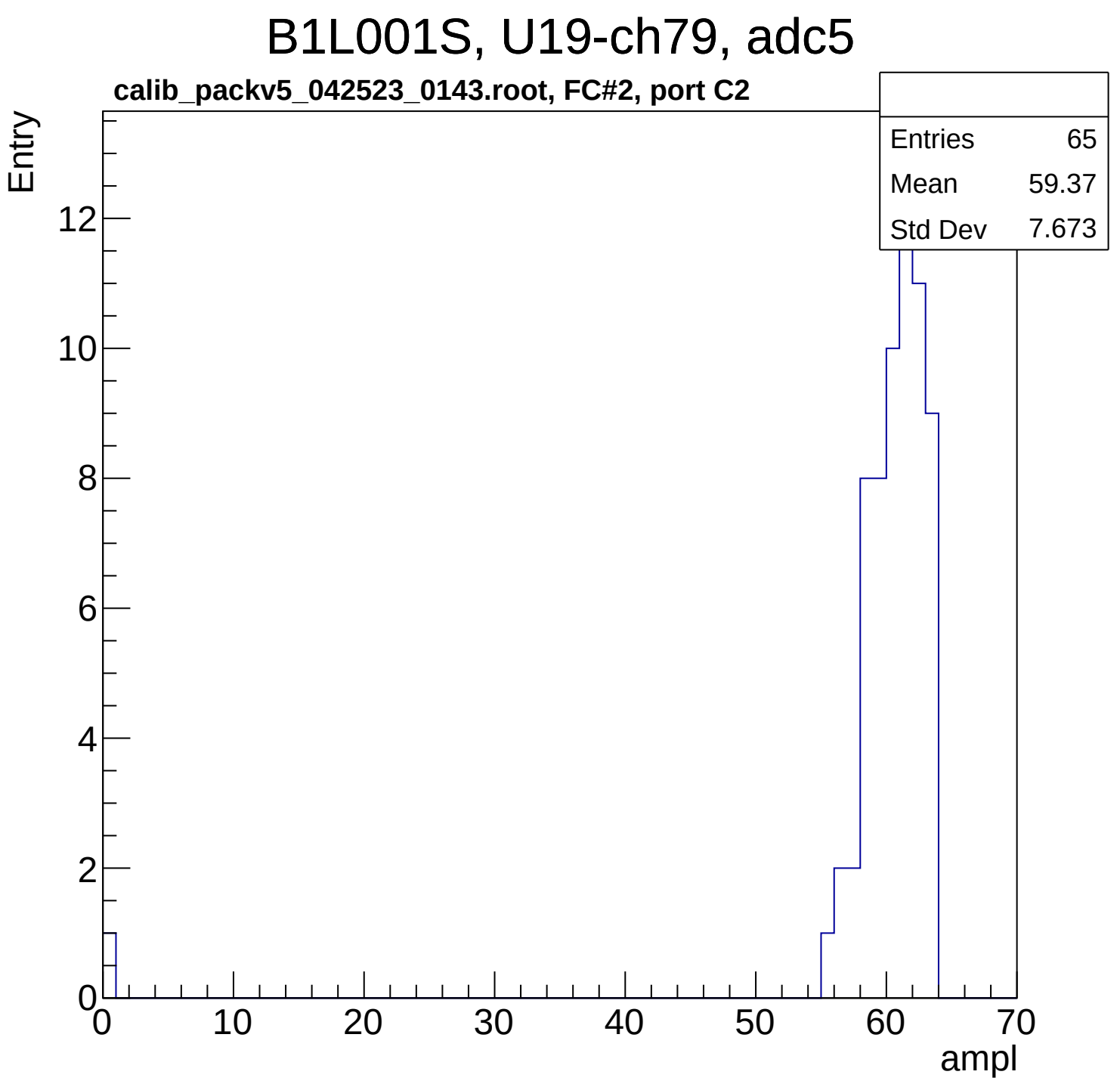
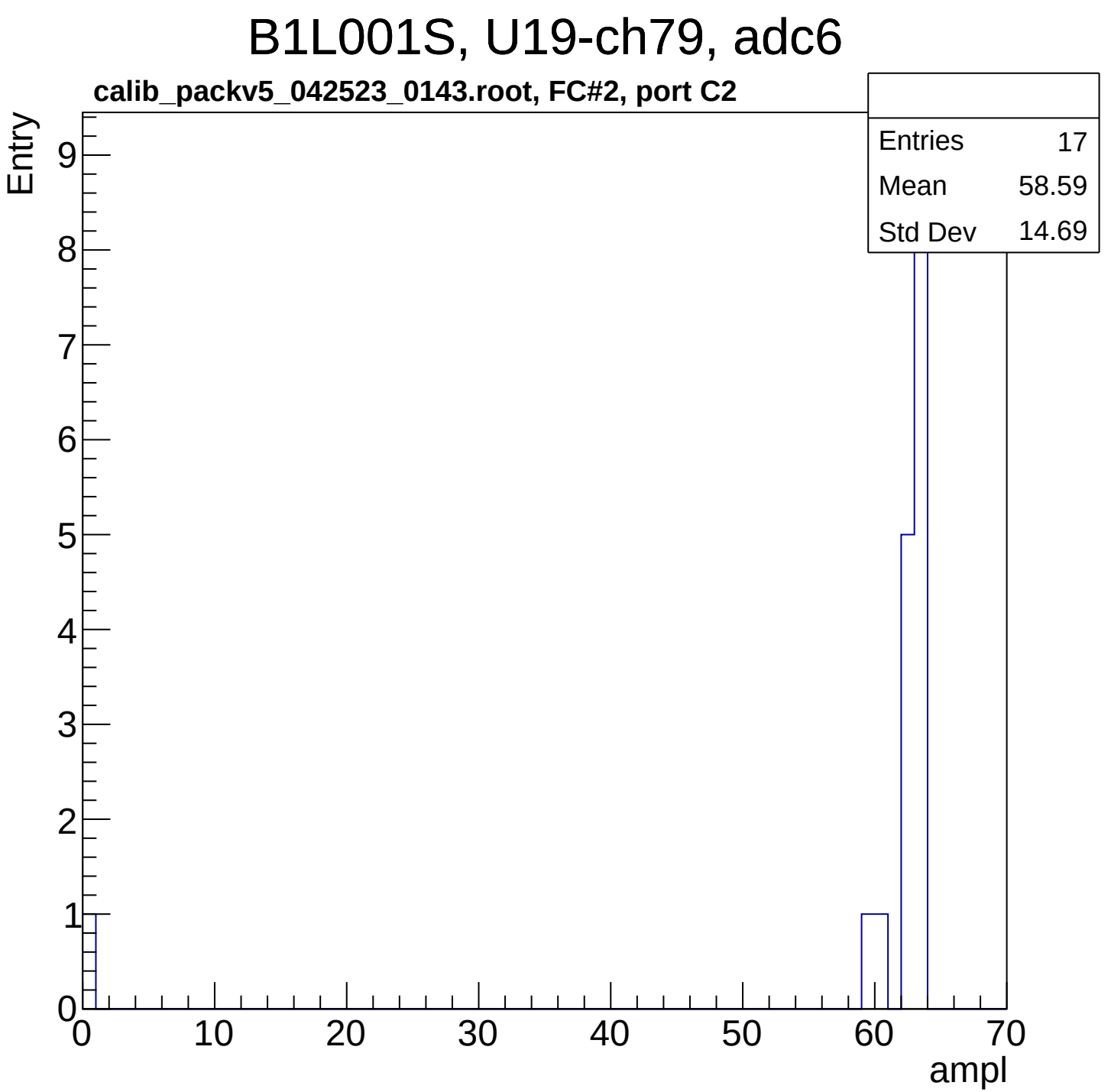

B1L001S, U19-ch79, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 151
Mean 43.13
Std Dev 3.435
Gaus mean : 43.7007
Gaus Width: 3.6106
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70


B1L001S, U19-ch79, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 139
Mean 50.33
Std Dev 3.527
Entry
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch79, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 113
Mean 56.58
Std Dev 3.111
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L001S, U19-ch79, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 65
Mean 59.37
Std Dev 7.673
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch79, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 17
Mean 58.59
Std Dev 14.69
Entry
0
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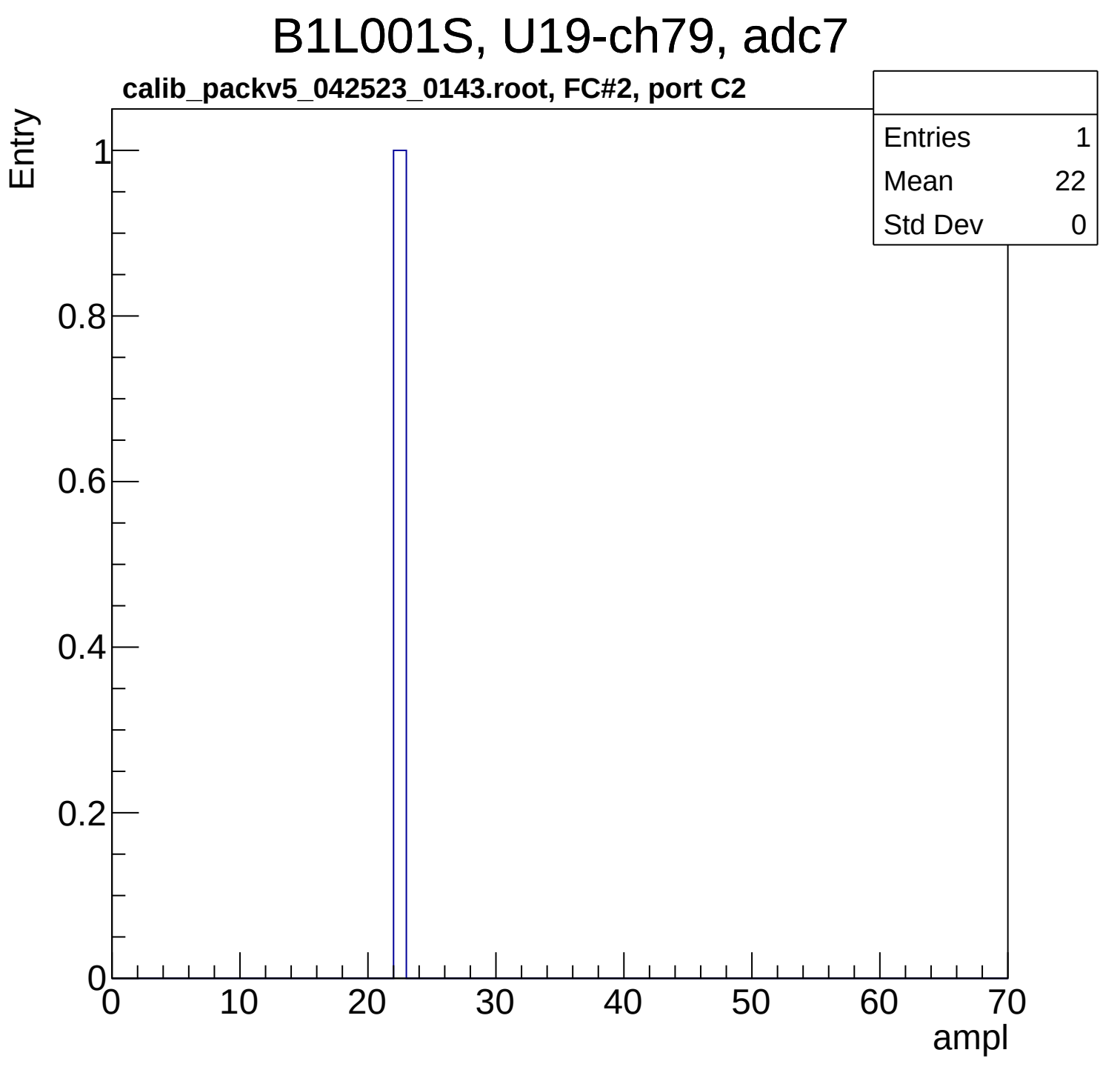
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch79, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 22
Std Dev 0
Entry
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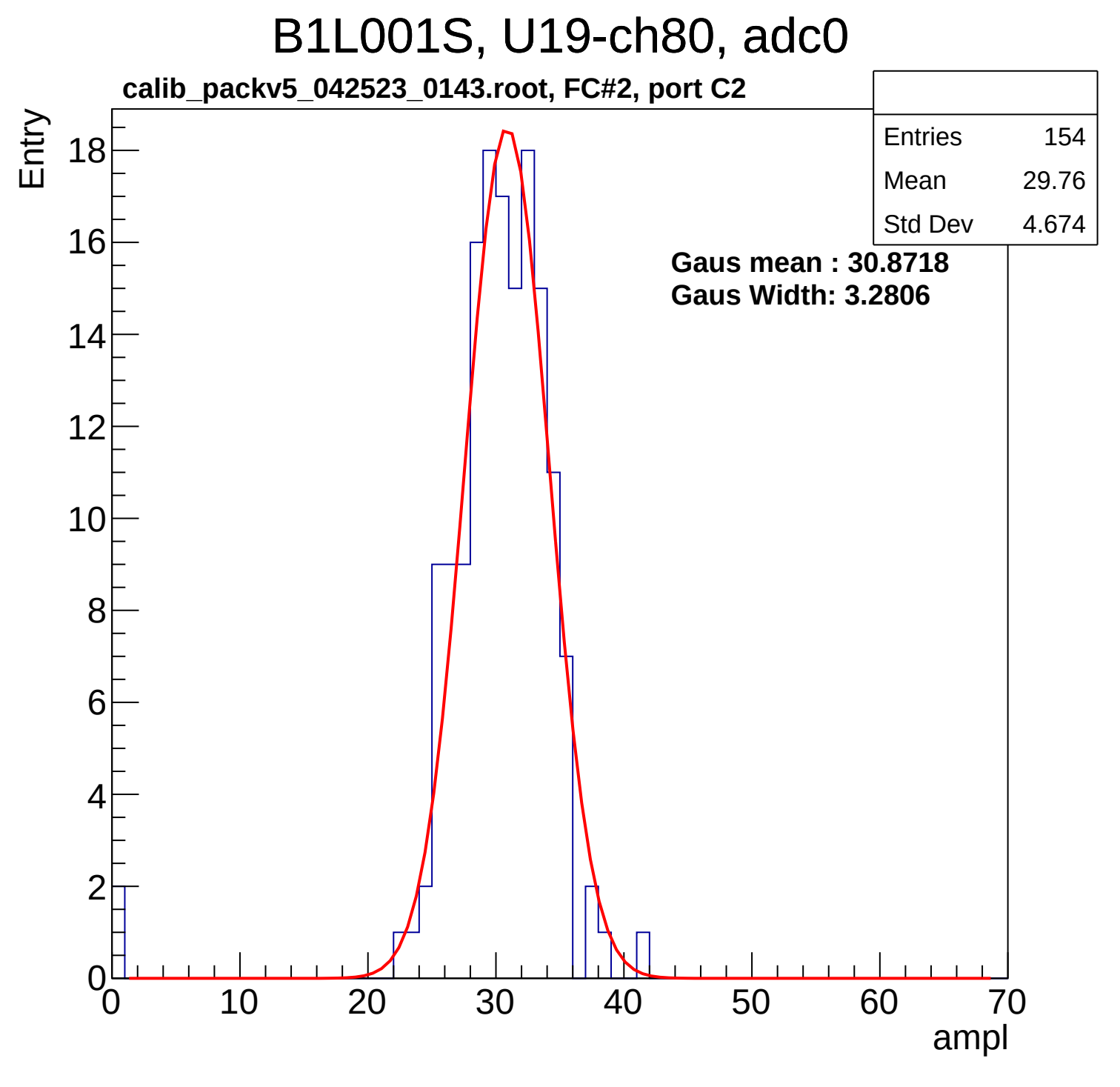
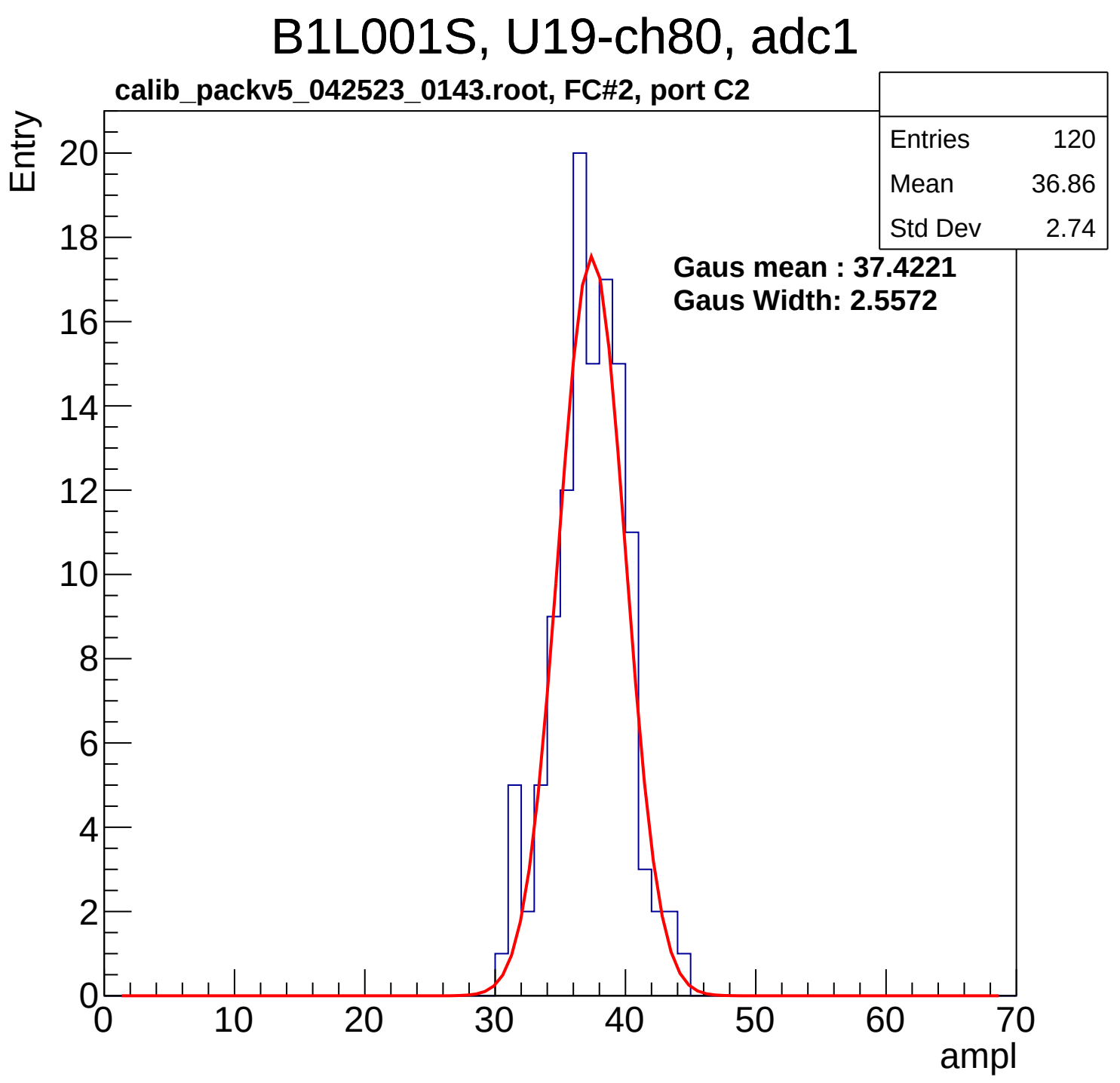
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch80, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 154
Mean 29.76
Std Dev 4.674
Gaus mean : 30.8718
Gaus Width: 3.2806
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70


B1L001S, U19-ch80, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 120
Mean 36.86
Std Dev 2.74
Gaus mean : 37.4221
Gaus Width: 2.5572
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
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60
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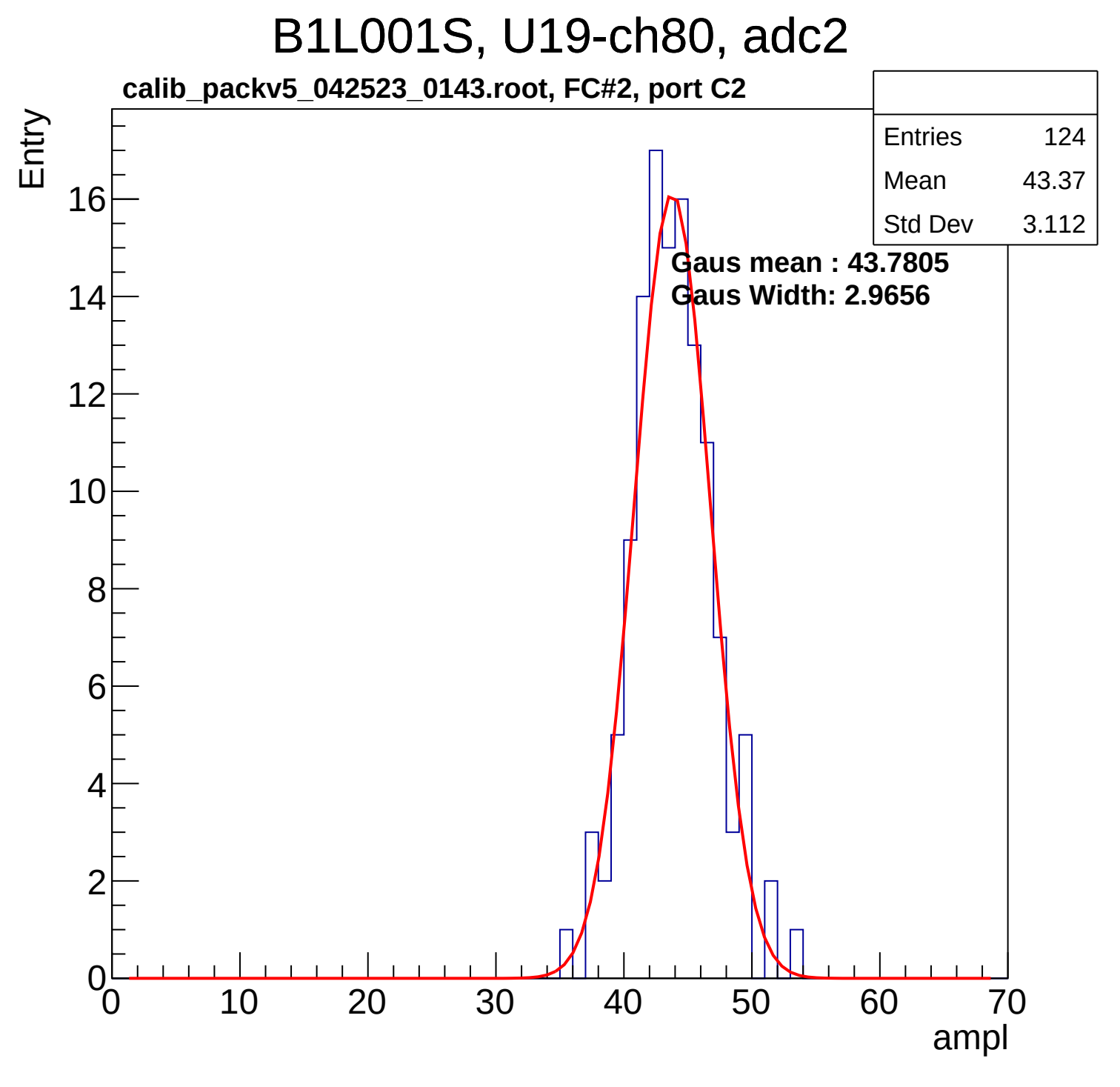
B1L001S, U19-ch80, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 124
Mean 43.37
Std Dev 3.112
Gaus mean : 43.7805
Gaus Width: 2.9656
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
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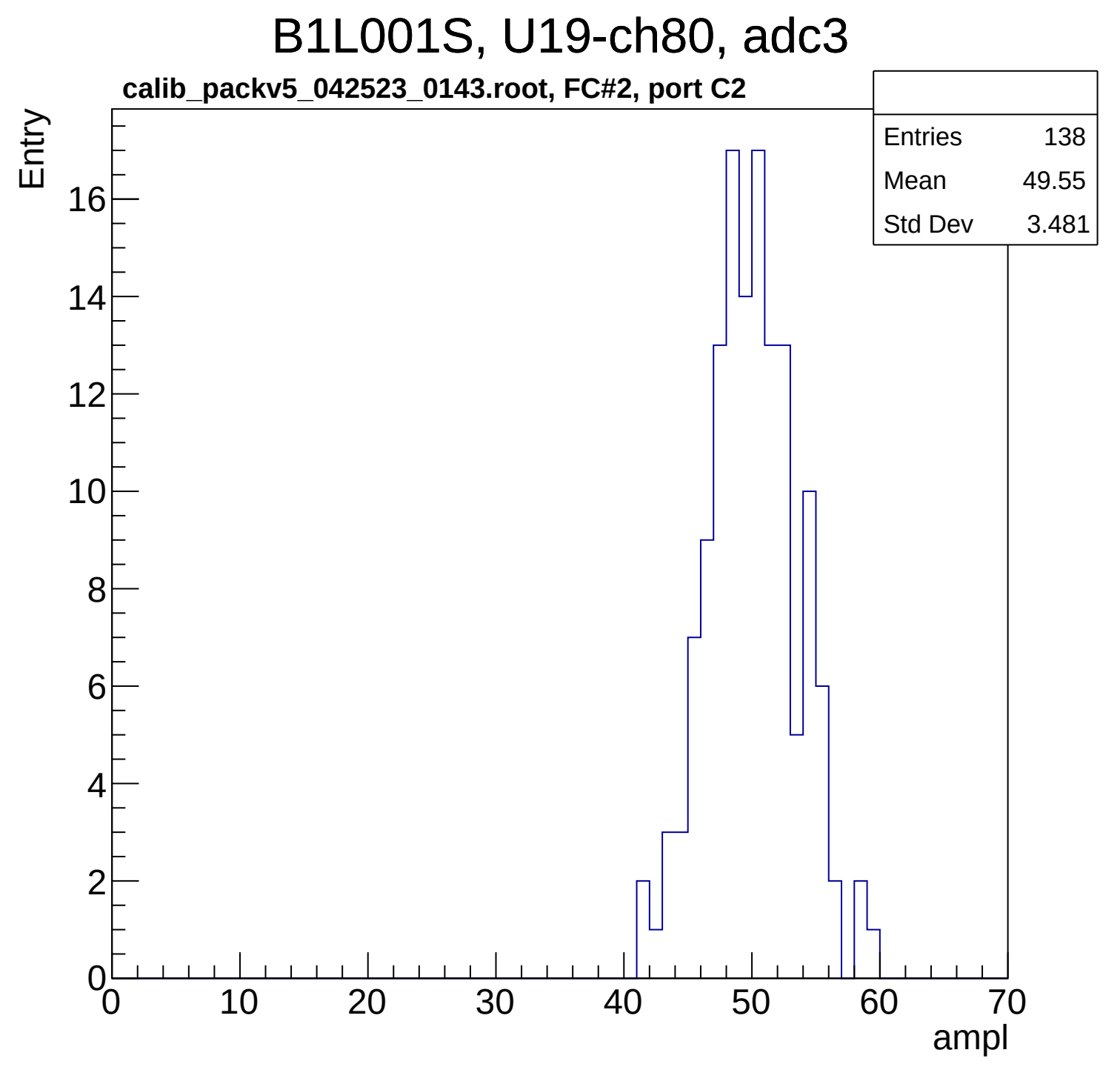
B1L001S, U19-ch80, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 138
Mean 49.55
Std Dev 3.481
Entry
ampl
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2
4
6
8
10
12
14
16
0
10
20
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40
50
60
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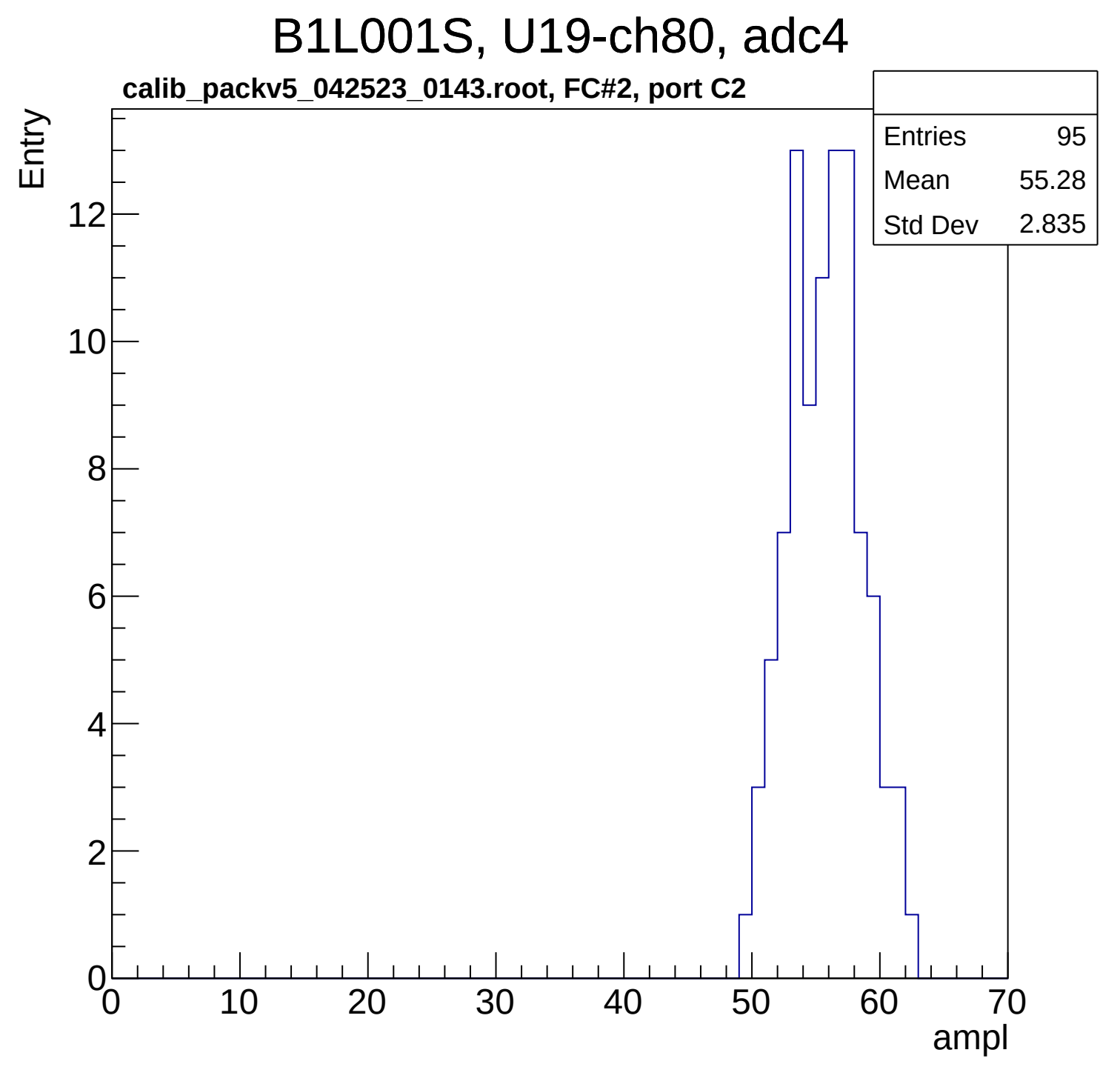
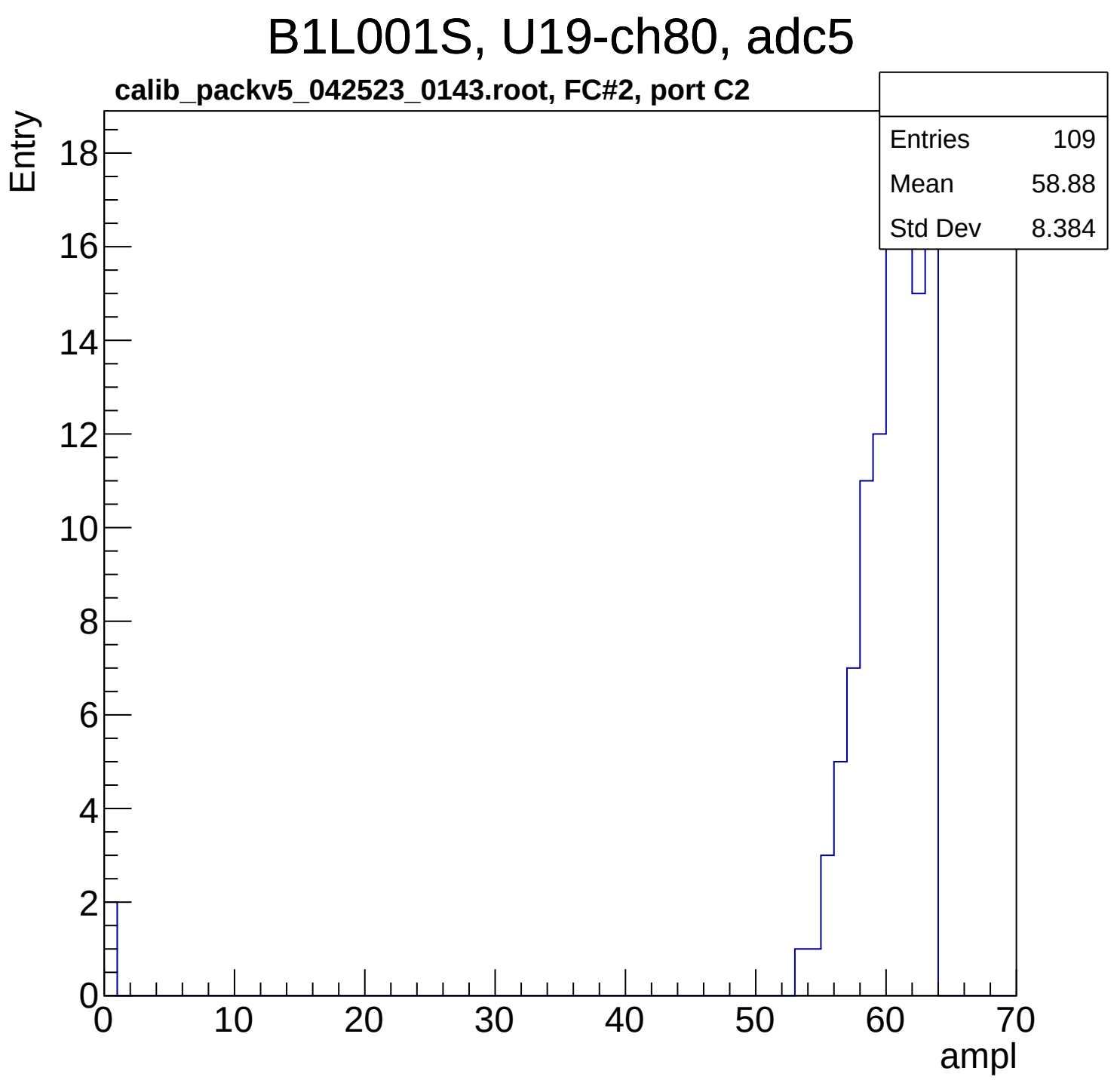

B1L001S, U19-ch80, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 95
Mean 55.28
Std Dev 2.835
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch80, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 109
Mean 58.88
Std Dev 8.384
Entry
ampl
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4
6
8
10
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14
16
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0
10
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30
40
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60
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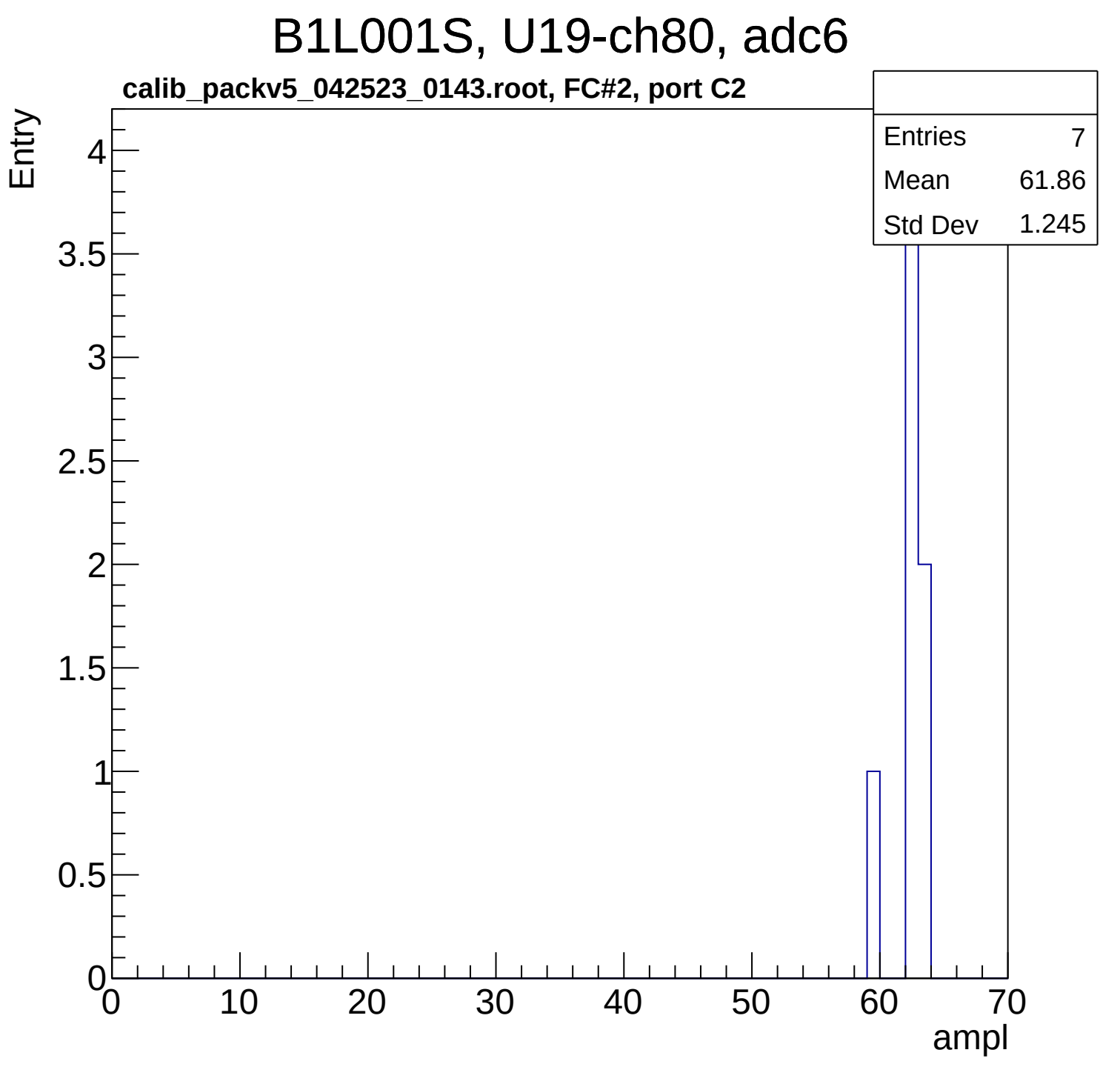
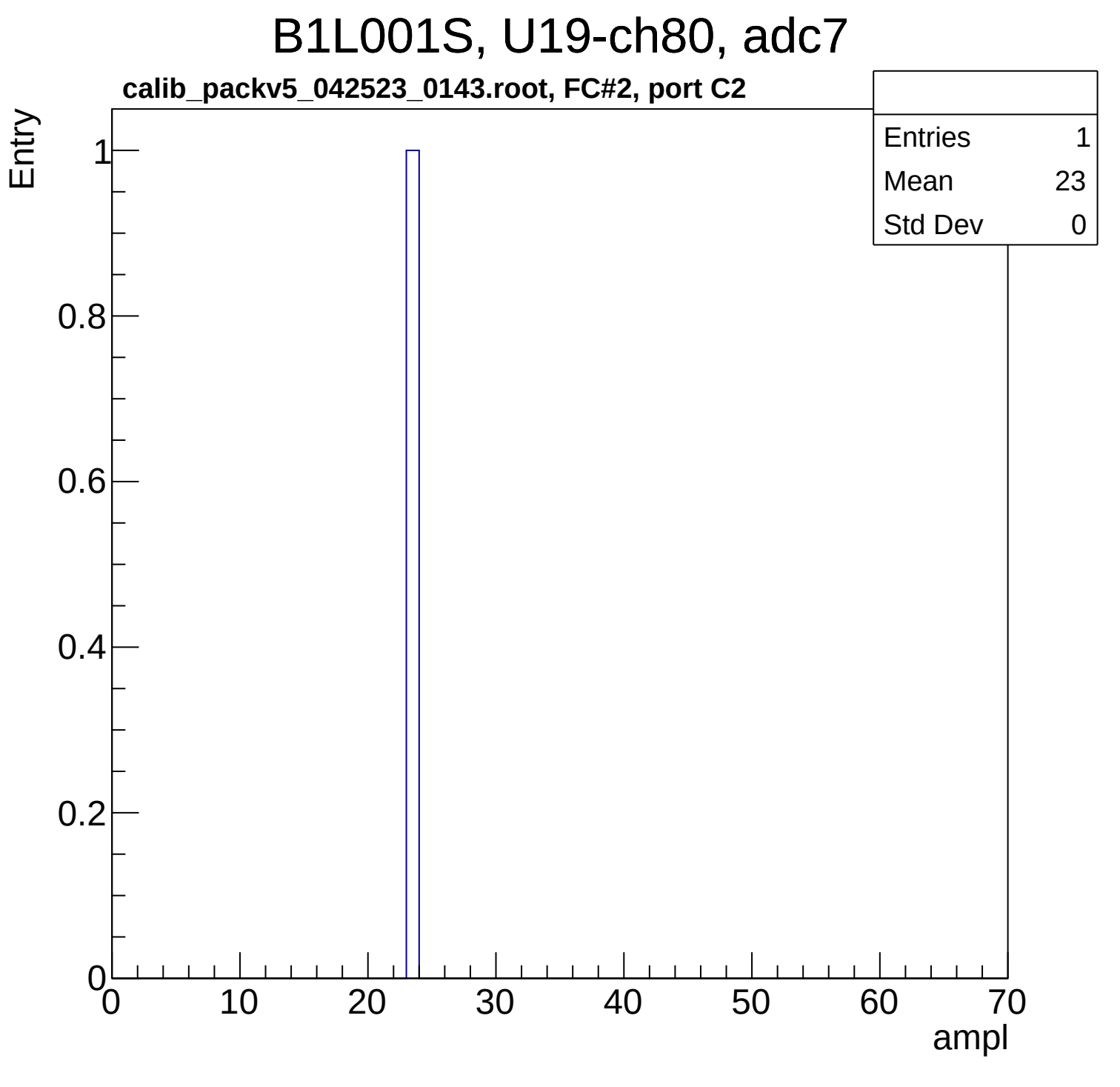

B1L001S, U19-ch80, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 7
Mean 61.86
Std Dev 1.245
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L001S, U19-ch80, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 23
Std Dev 0
Entry
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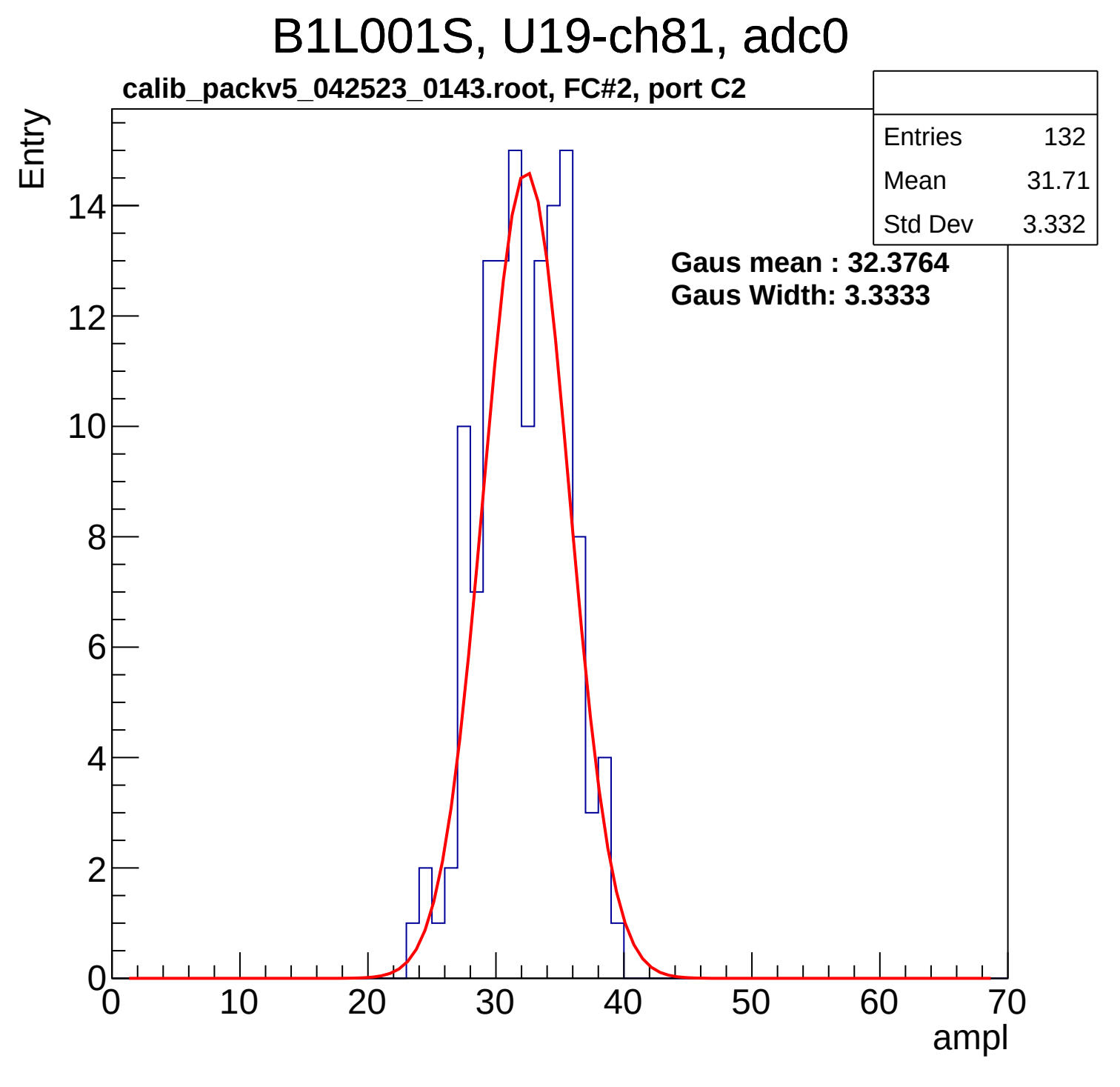
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch81, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 132
Mean 31.71
Std Dev 3.332
Gaus mean : 32.3764
Gaus Width: 3.3333
Entry
ampl
0
2
4
6
8
10
12
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0
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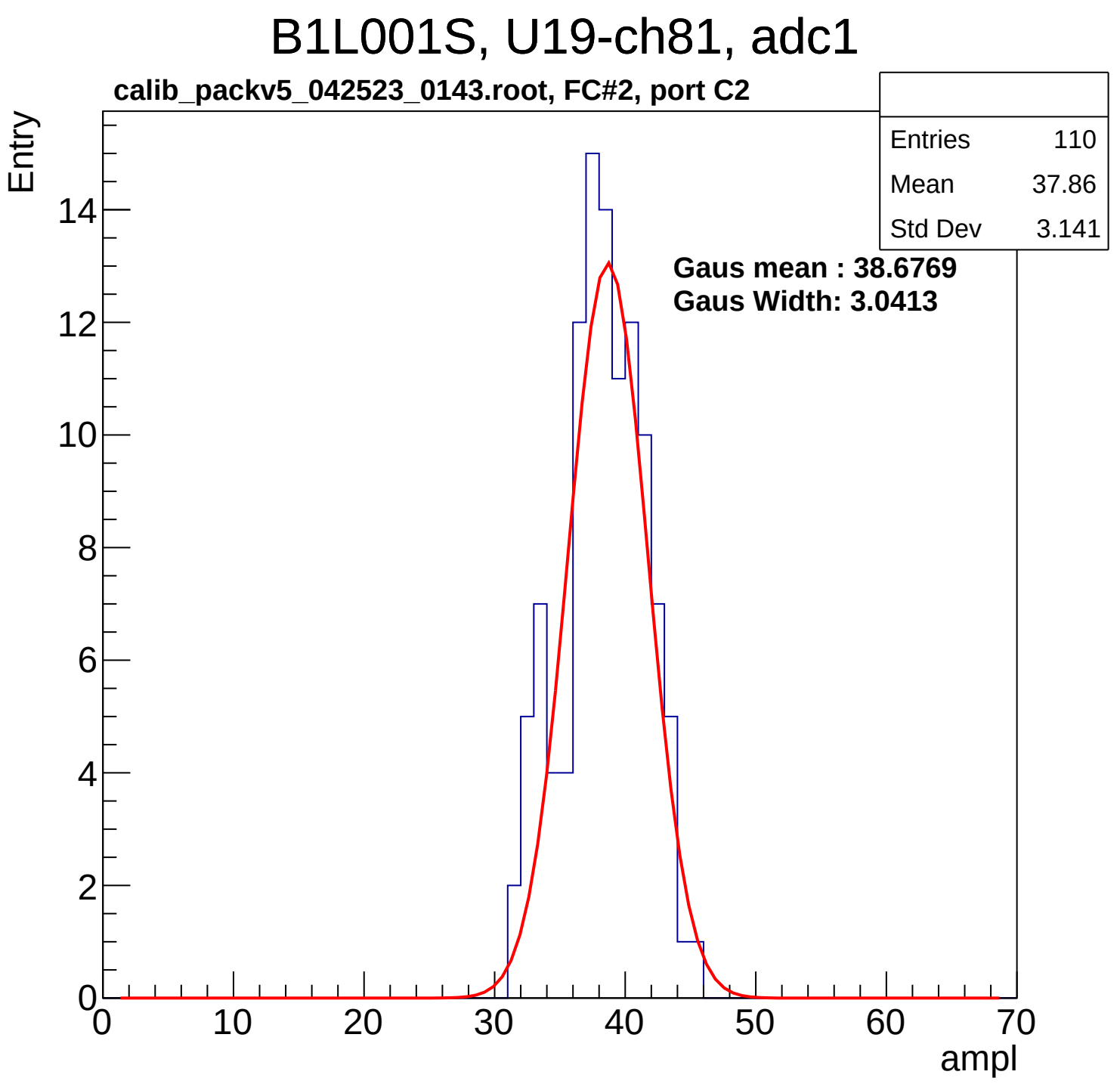
20
30
40
50
60
70


B1L001S, U19-ch81, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 110
Mean 37.86
Std Dev 3.141
Gaus mean : 38.6769
Gaus Width: 3.0413
Entry
ampl
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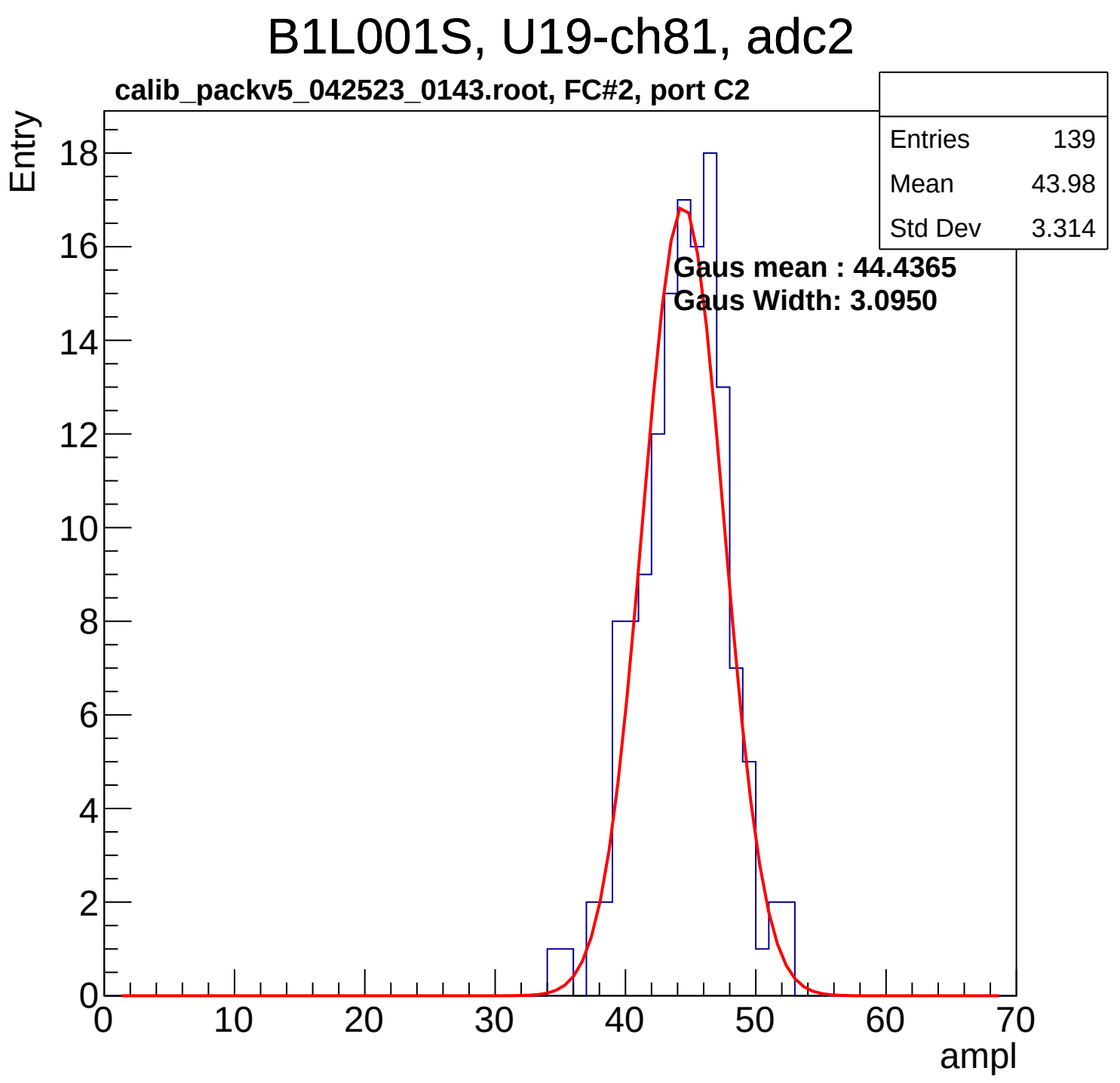
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L001S, U19-ch81, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 139
Mean 43.98
Std Dev 3.314
Gaus mean : 44.4365
Gaus Width: 3.0950
Entry
ampl
0
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4
6
8
10
12
14
16
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0
10
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40
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60
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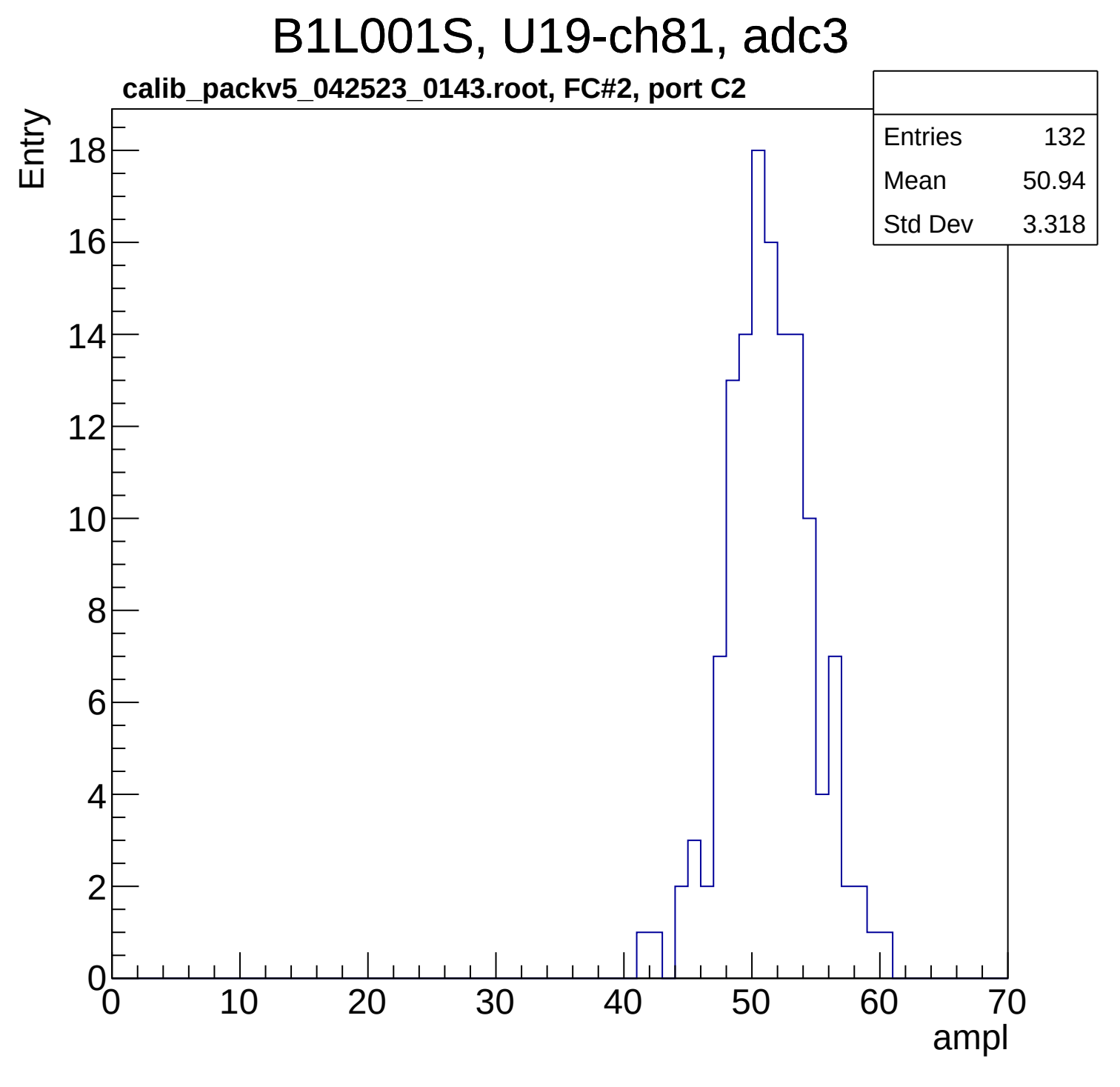
B1L001S, U19-ch81, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 132
Mean 50.94
Std Dev 3.318
Entry
ampl
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4
6
8
10
12
14
16
18
0
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20
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40
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60
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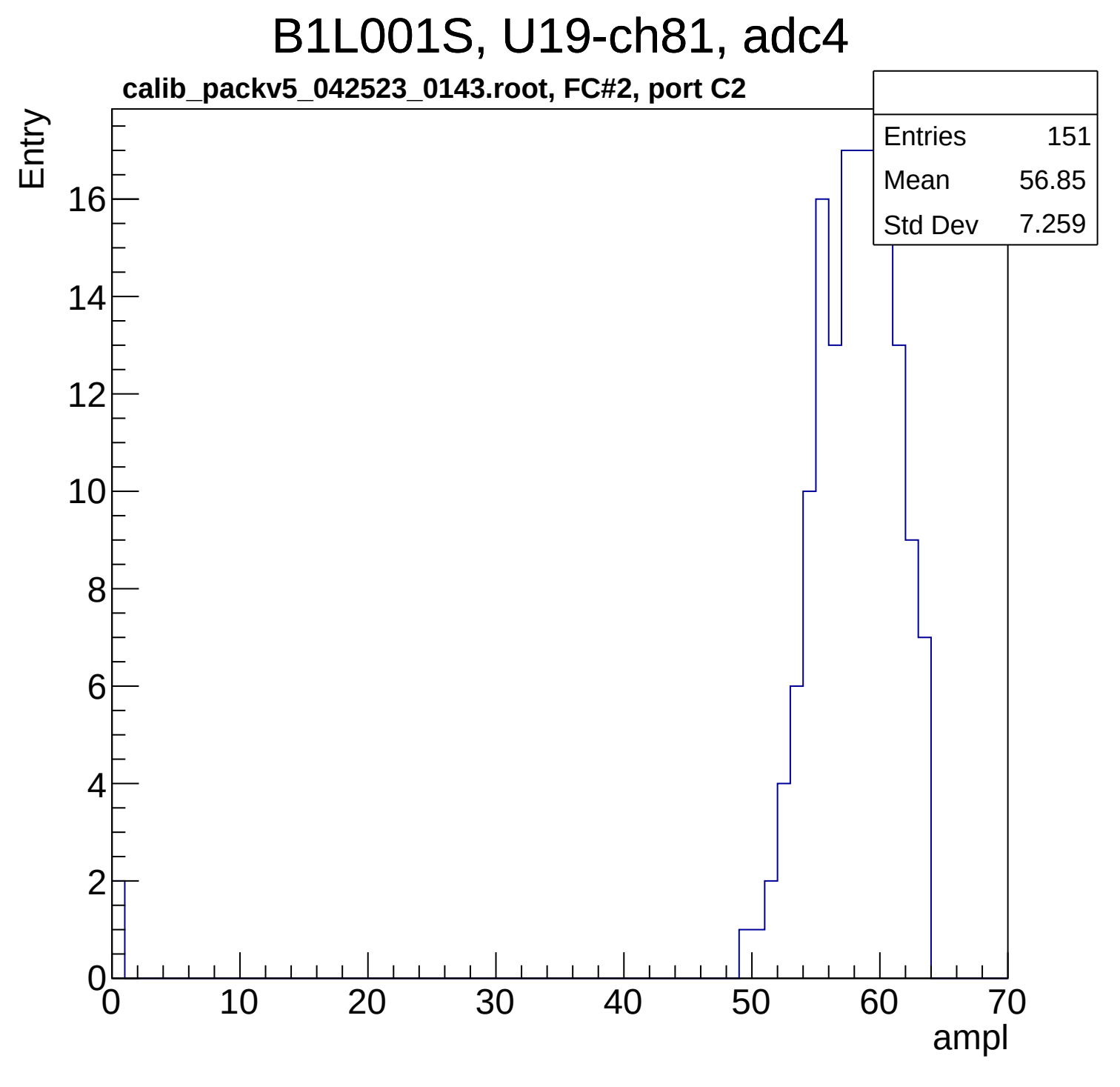
B1L001S, U19-ch81, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 151
Mean 56.85
Std Dev 7.259
Entry
ampl
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2
4
6
8
10
12
14
16
0
10
20
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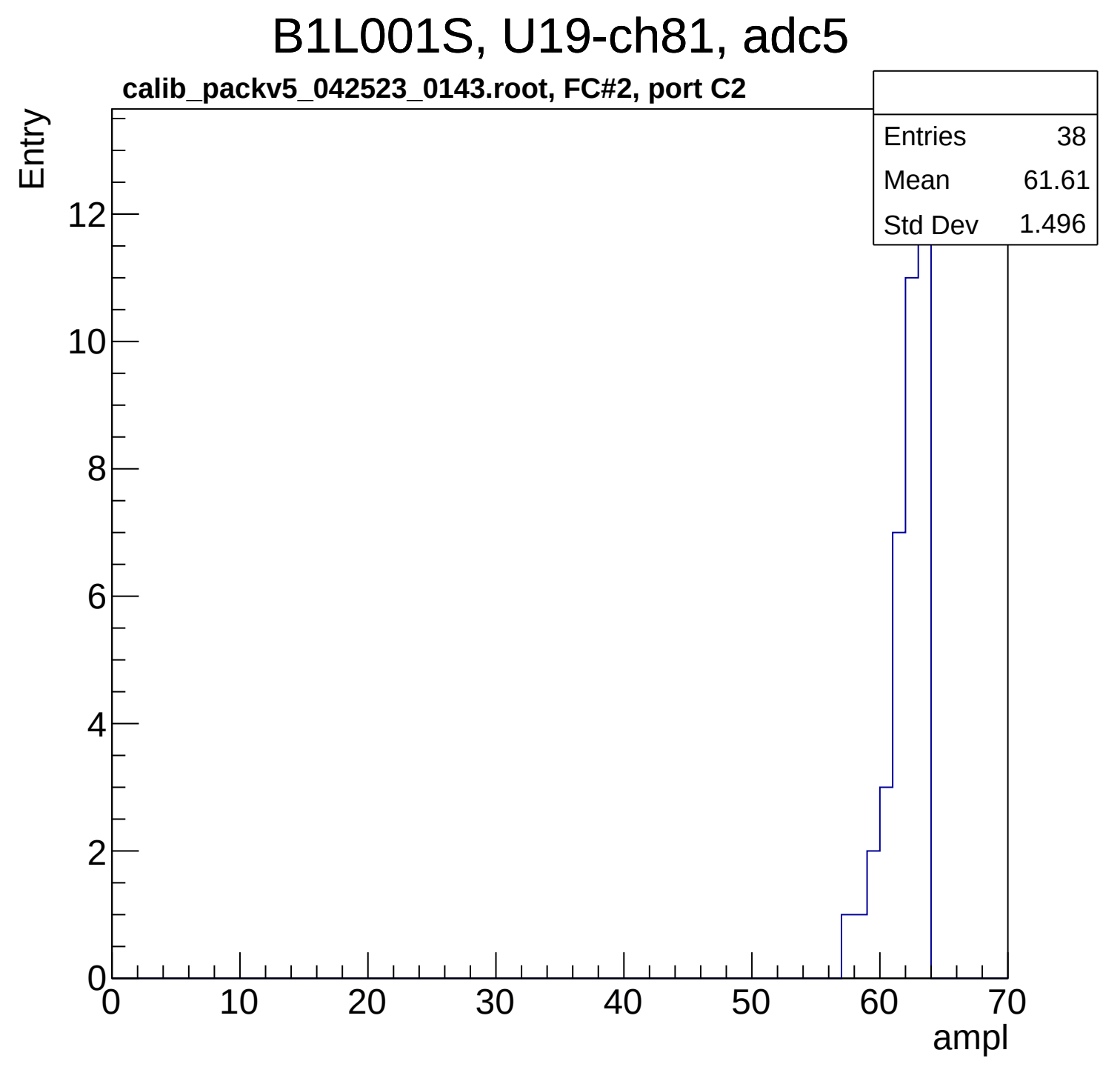
40
50
60
70


B1L001S, U19-ch81, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 38
Mean 61.61
Std Dev 1.496
Entry
0
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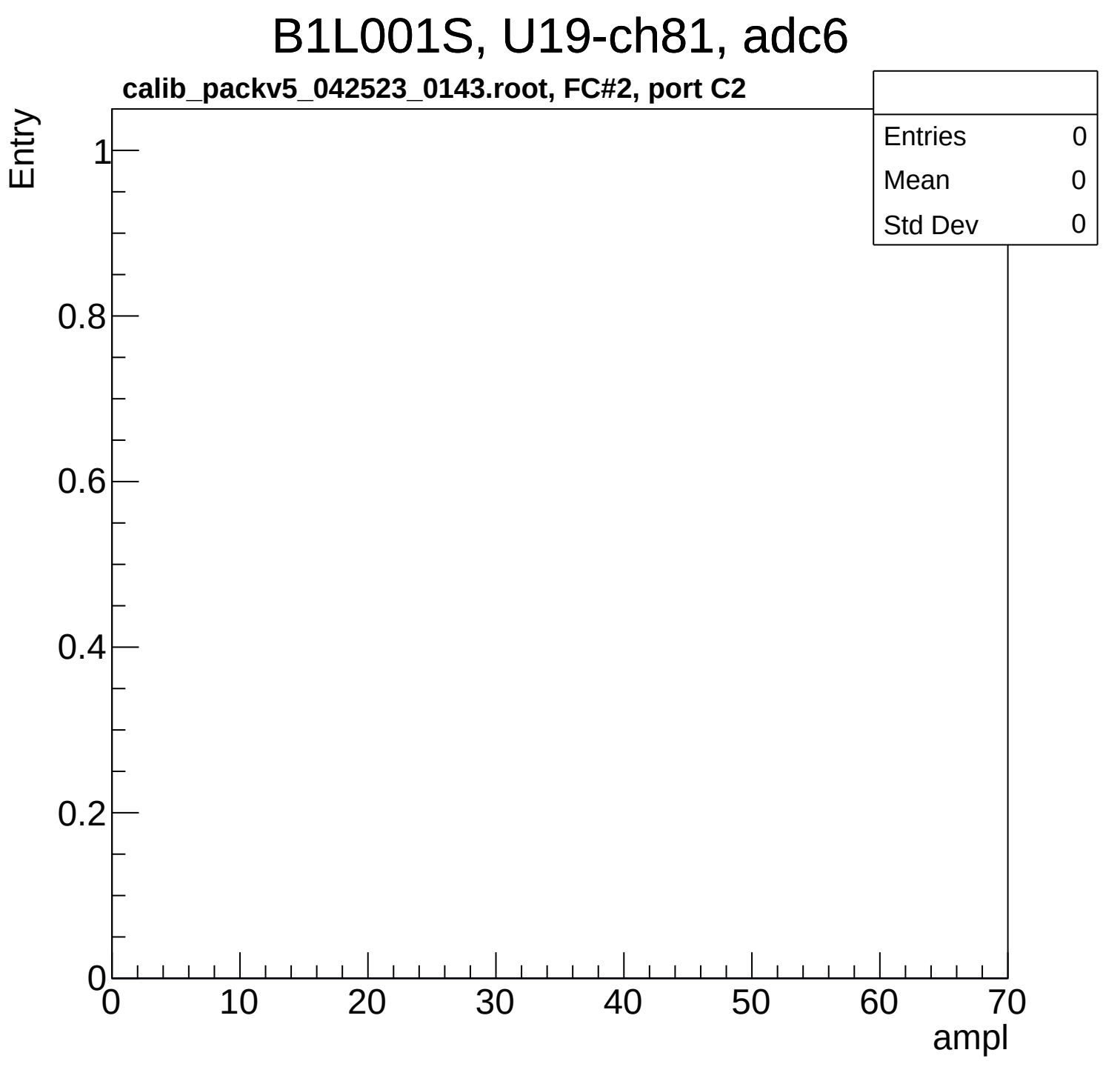
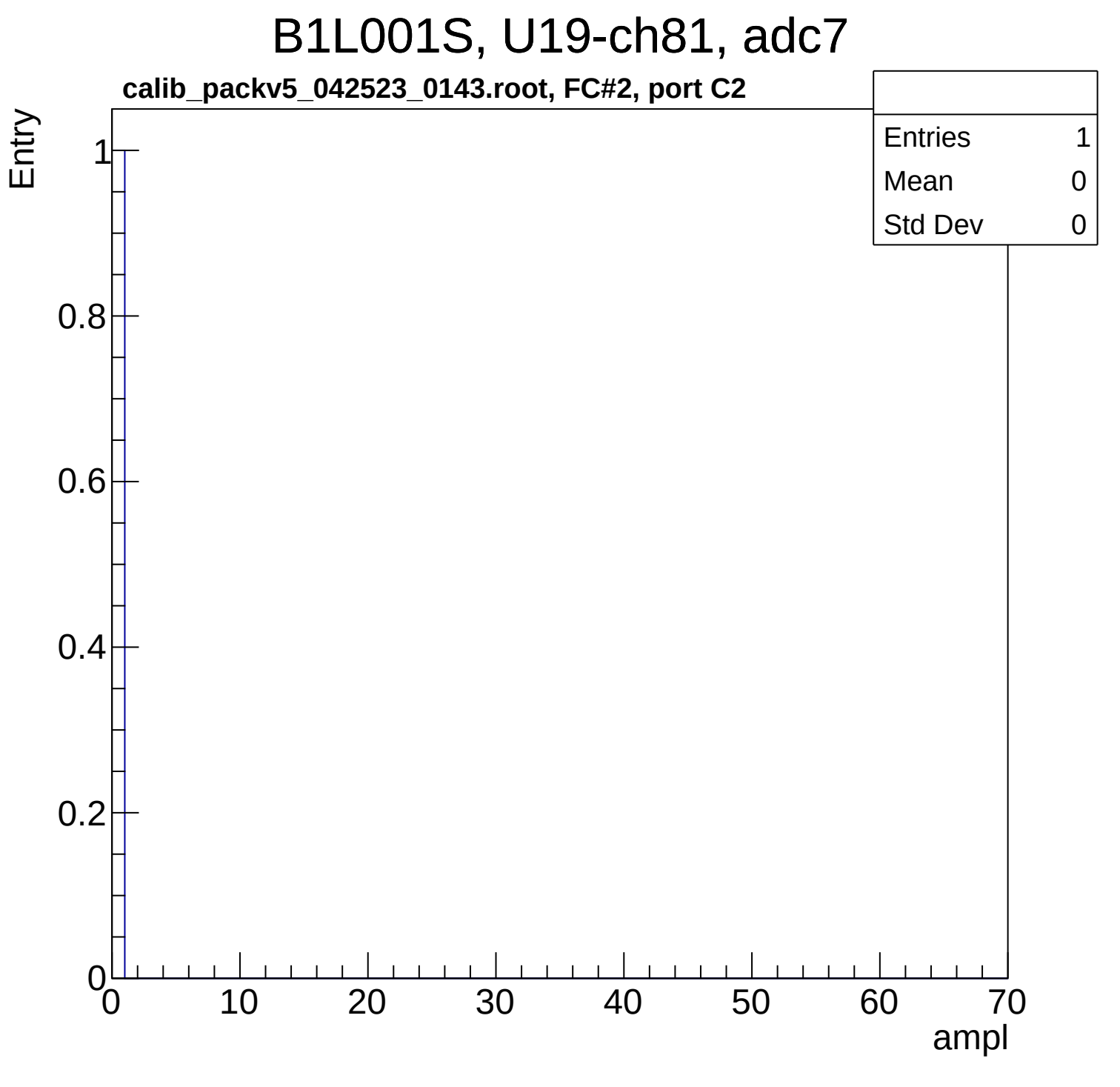
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch81, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch81, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 0
Std Dev 0
Entry
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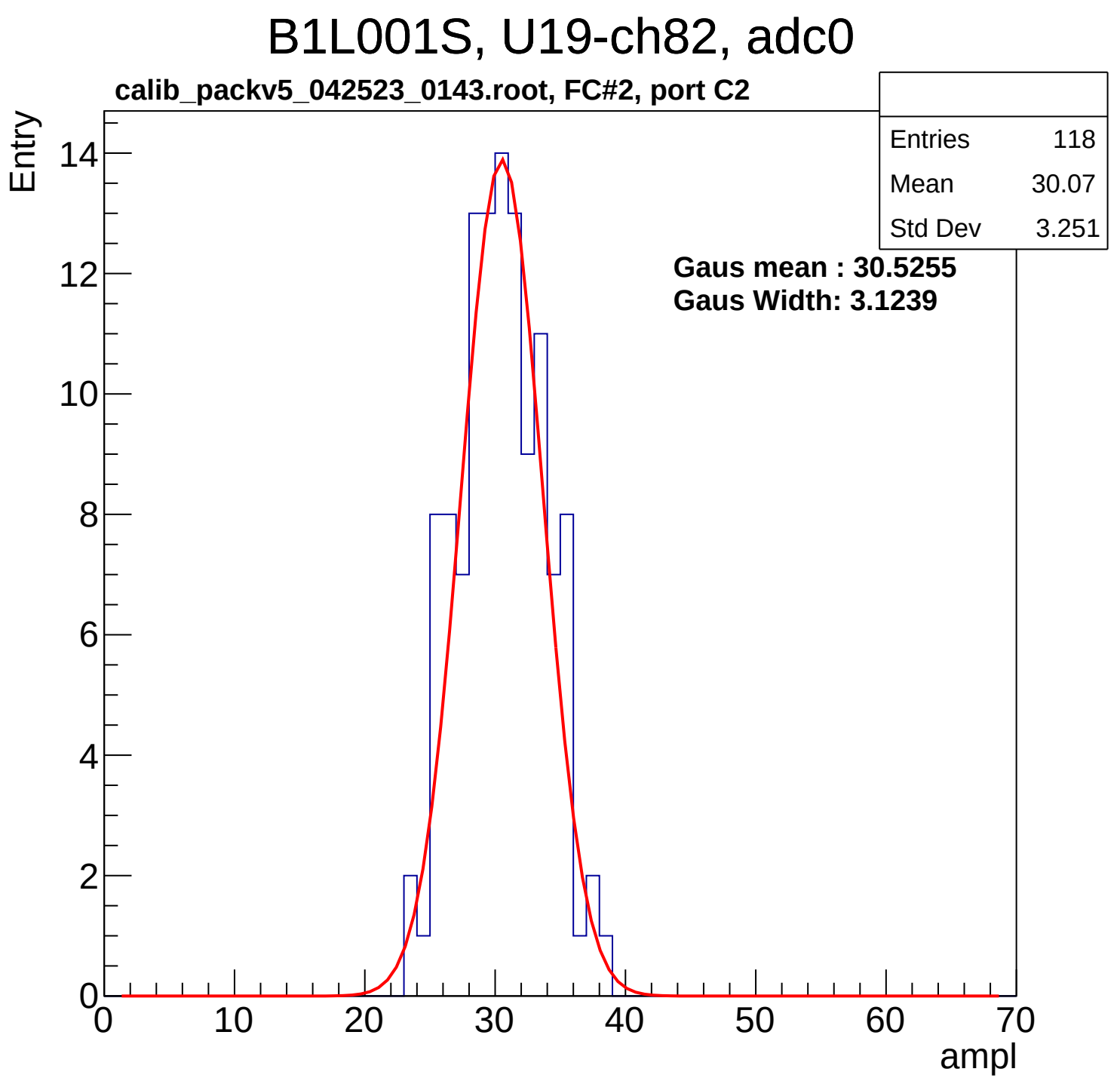
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch82, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 118
Mean 30.07
Std Dev 3.251
Gaus mean : 30.5255
Gaus Width: 3.1239
Entry
ampl
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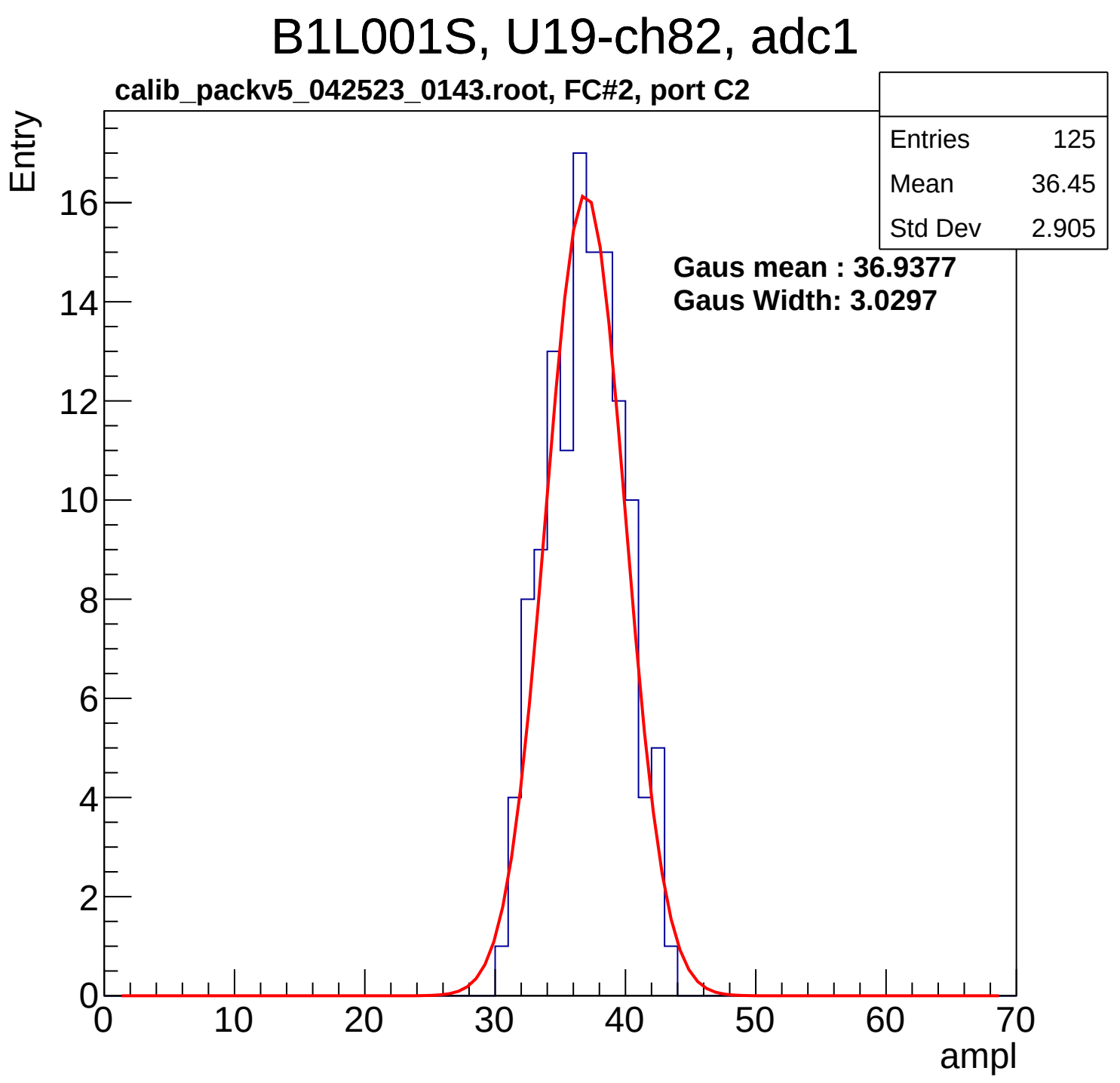
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L001S, U19-ch82, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 125
Mean 36.45
Std Dev 2.905
Gaus mean : 36.9377
Gaus Width: 3.0297
Entry
ampl
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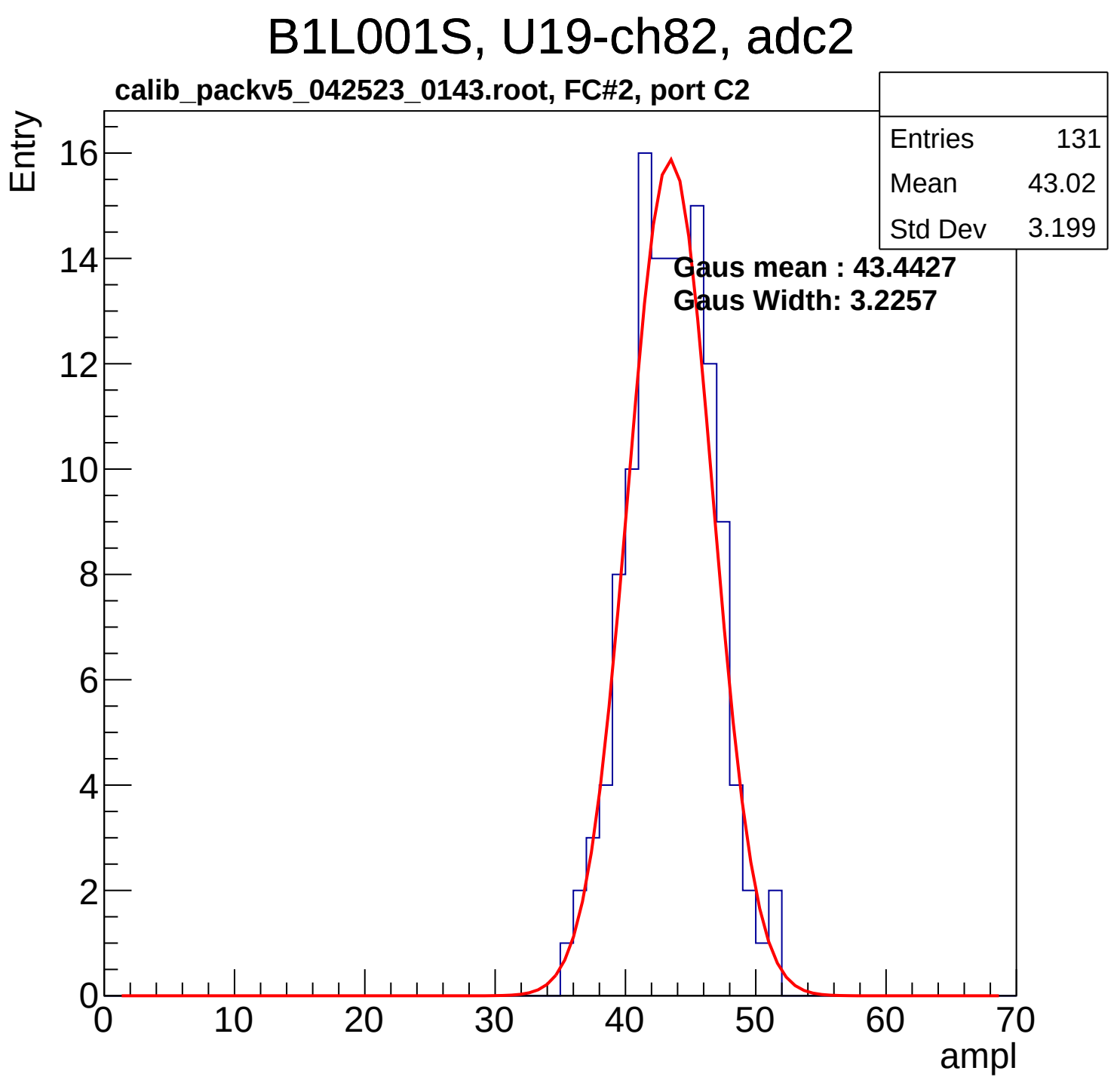
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70


B1L001S, U19-ch82, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 131
Mean 43.02
Std Dev 3.199
Gaus mean : 43.4427
Gaus Width: 3.2257
Entry
ampl
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4
6
8
10
12
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0
10
20
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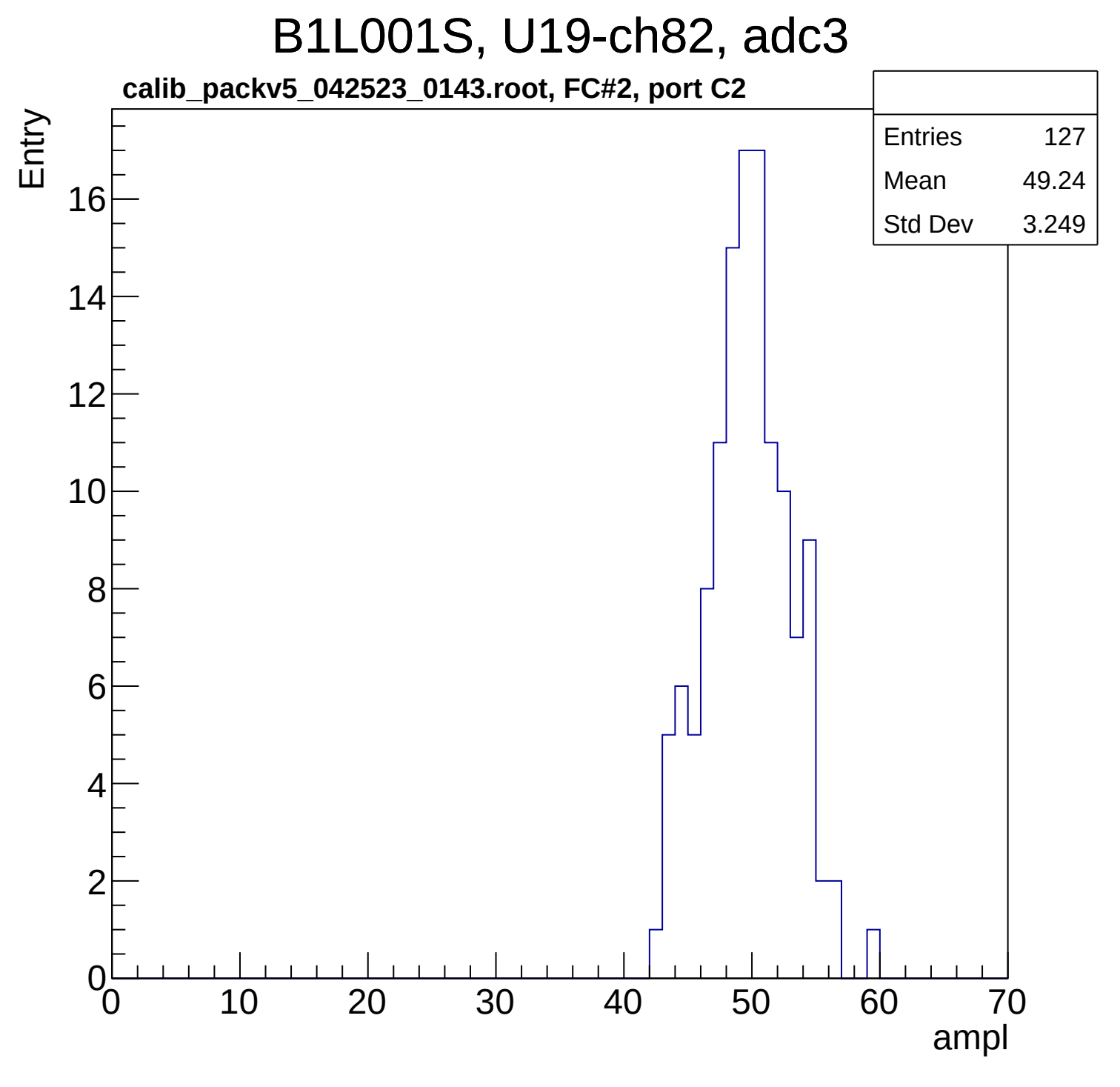
B1L001S, U19-ch82, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 127
Mean 49.24
Std Dev 3.249
Entry
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4
6
8
10
12
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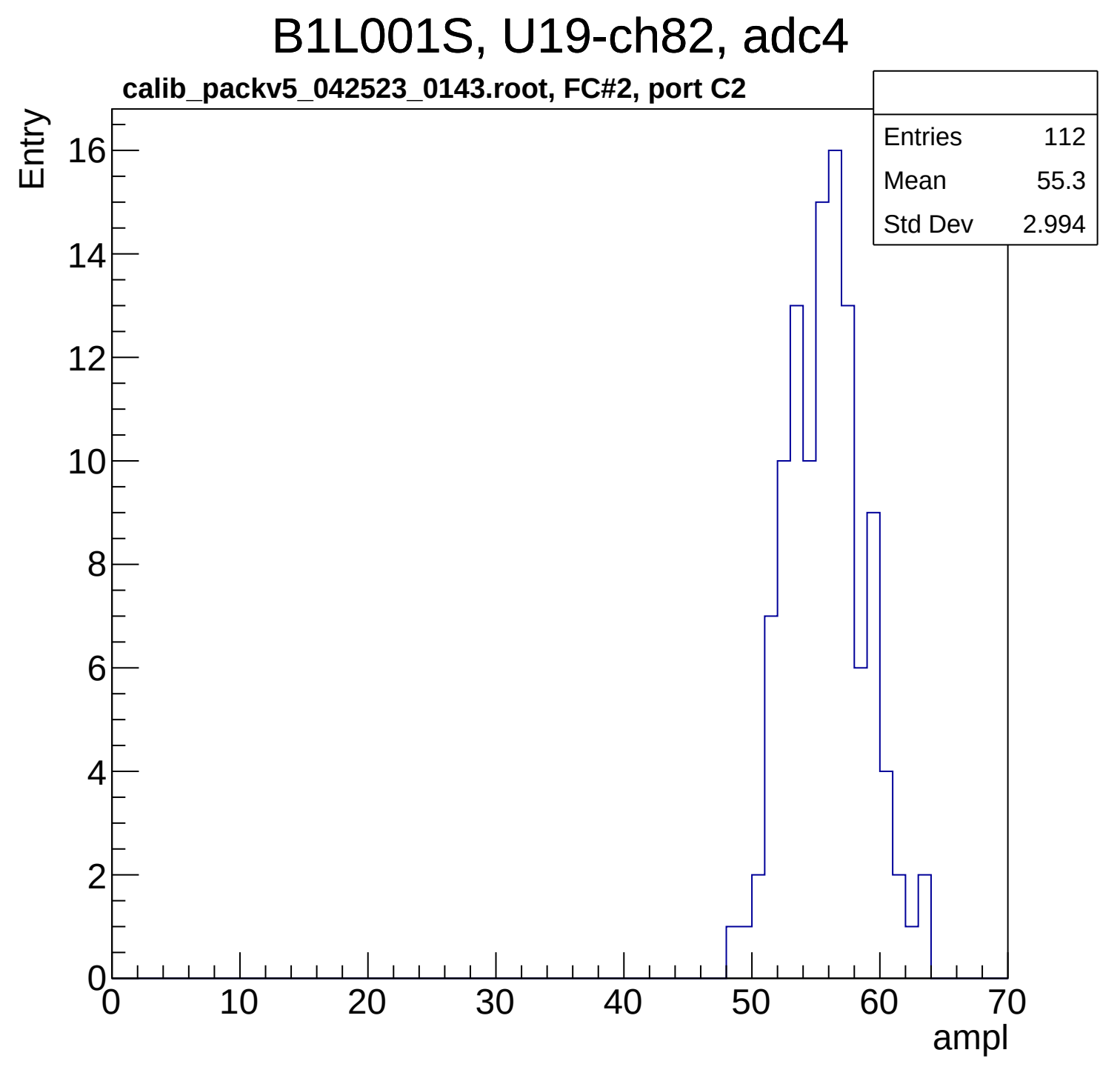
16
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch82, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 112
Mean 55.3
Std Dev 2.994
Entry
0
2
4
6
8
10
12
14
16
0
10
20
30
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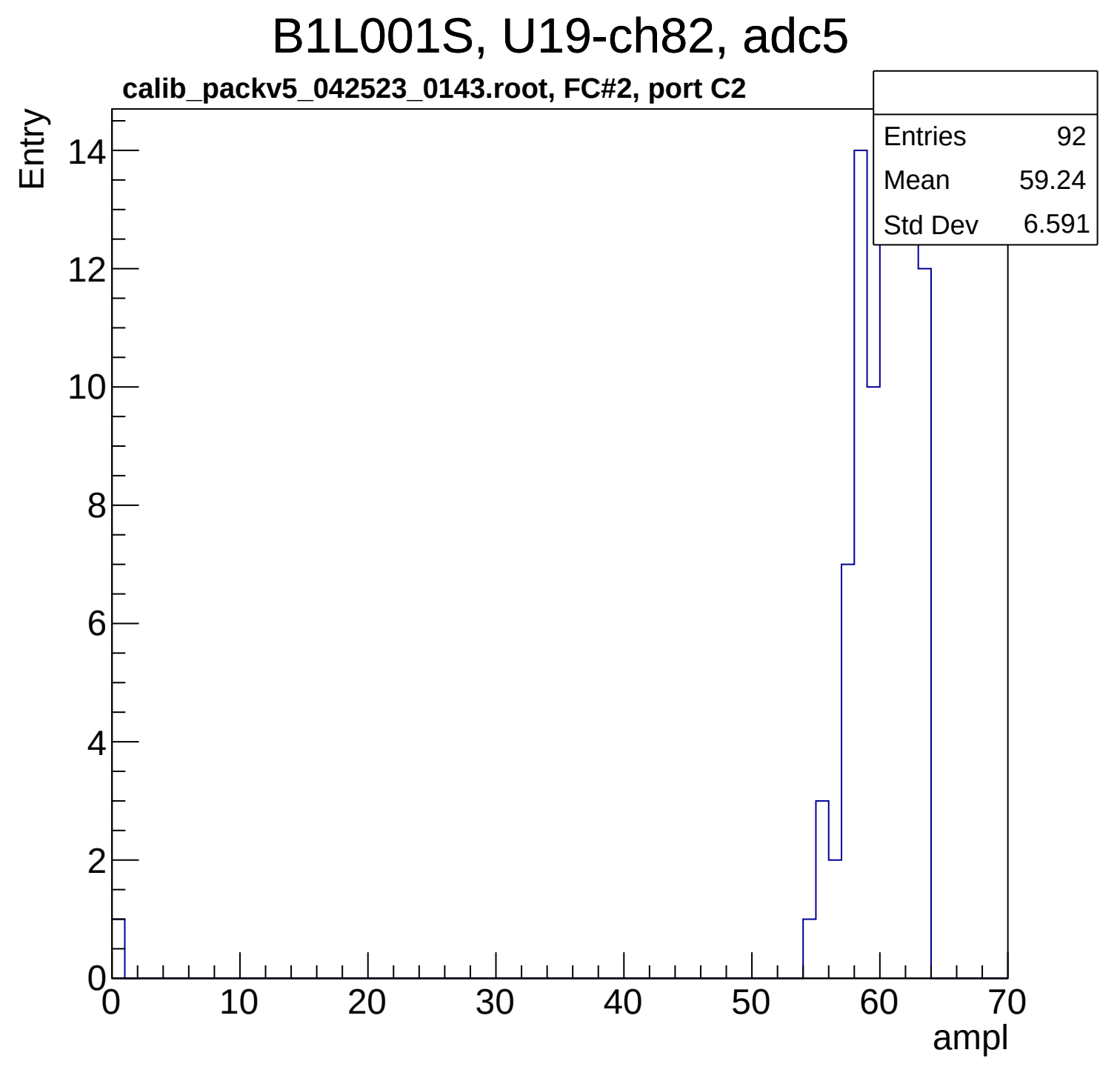
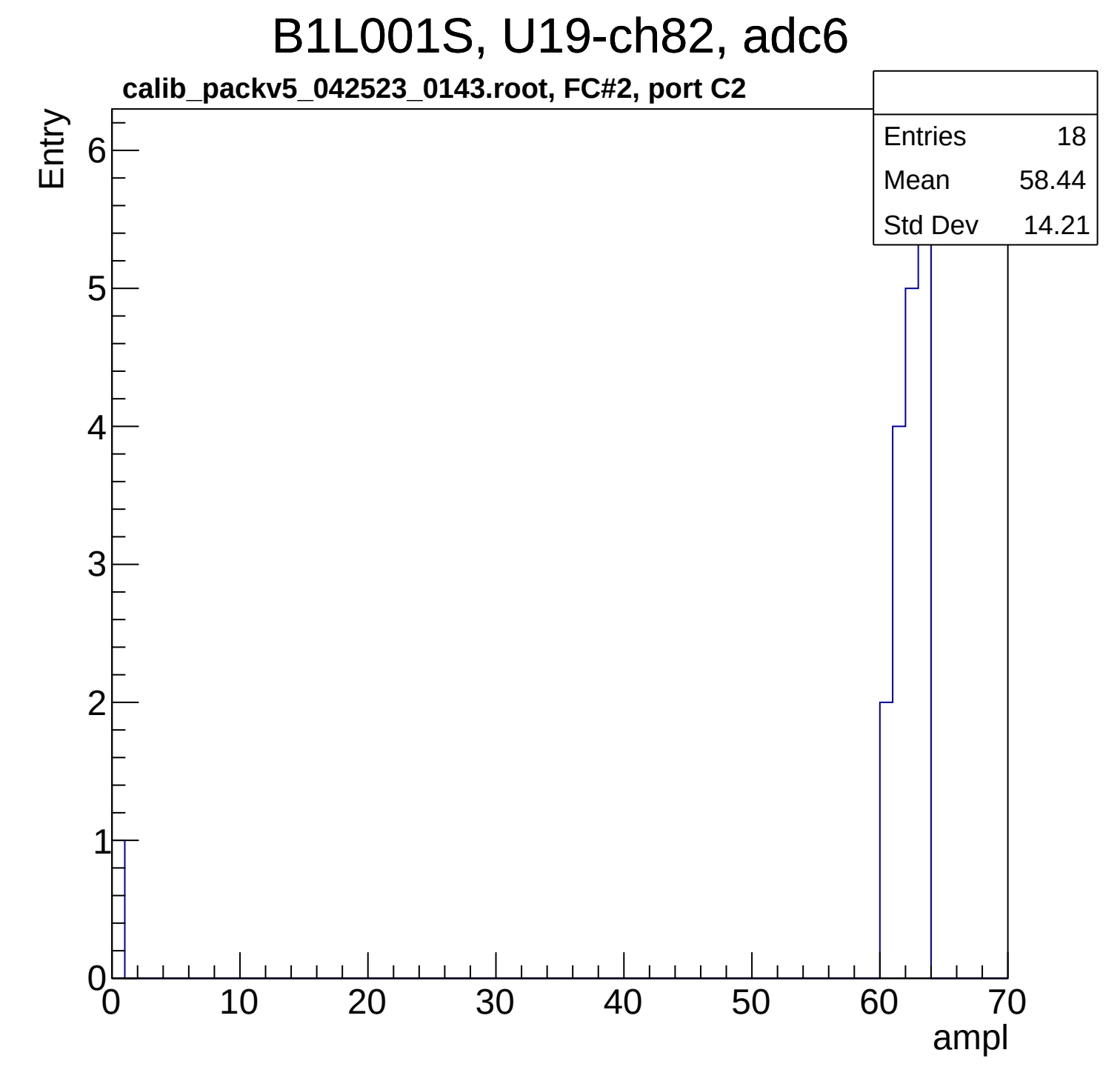
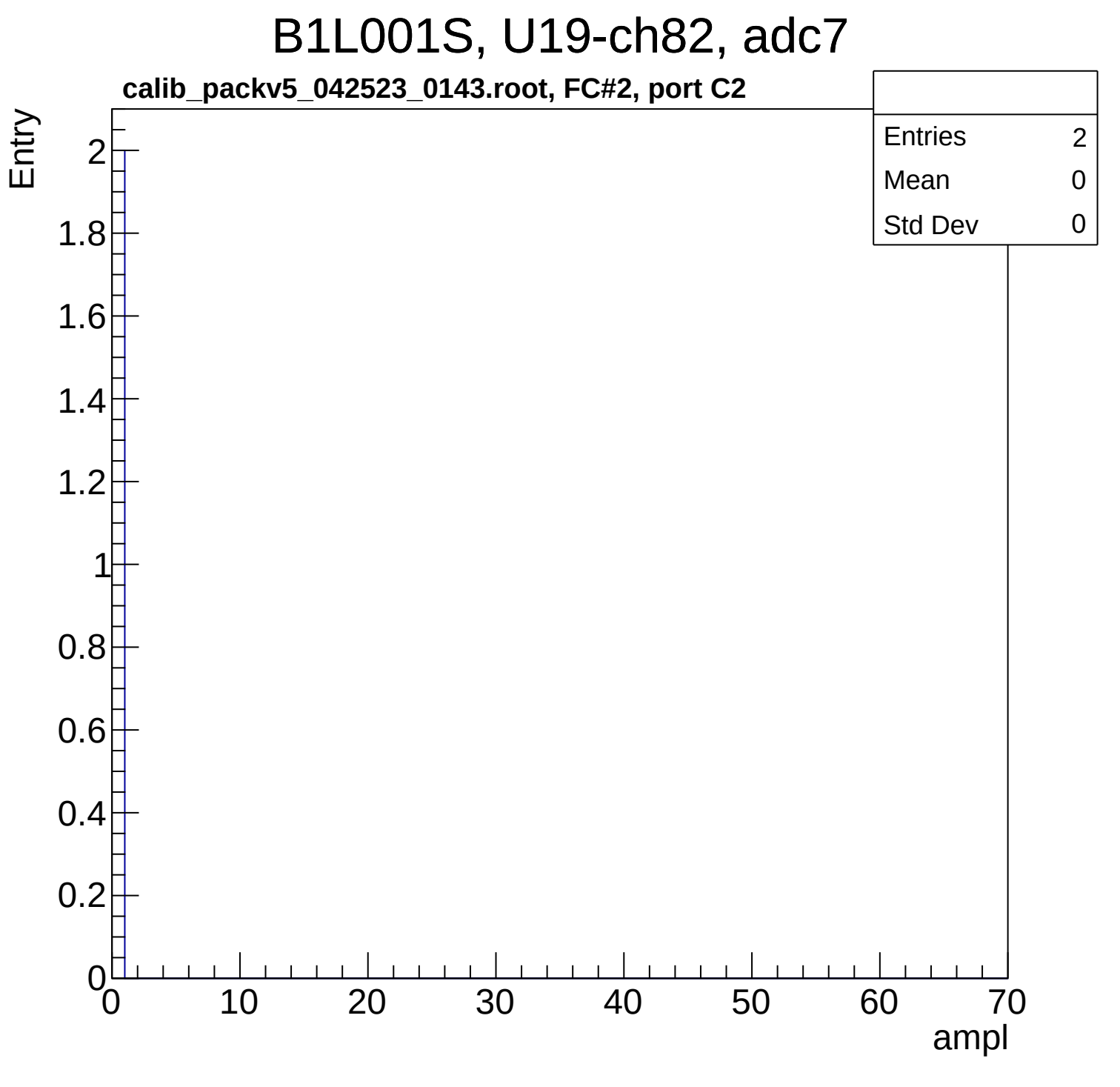
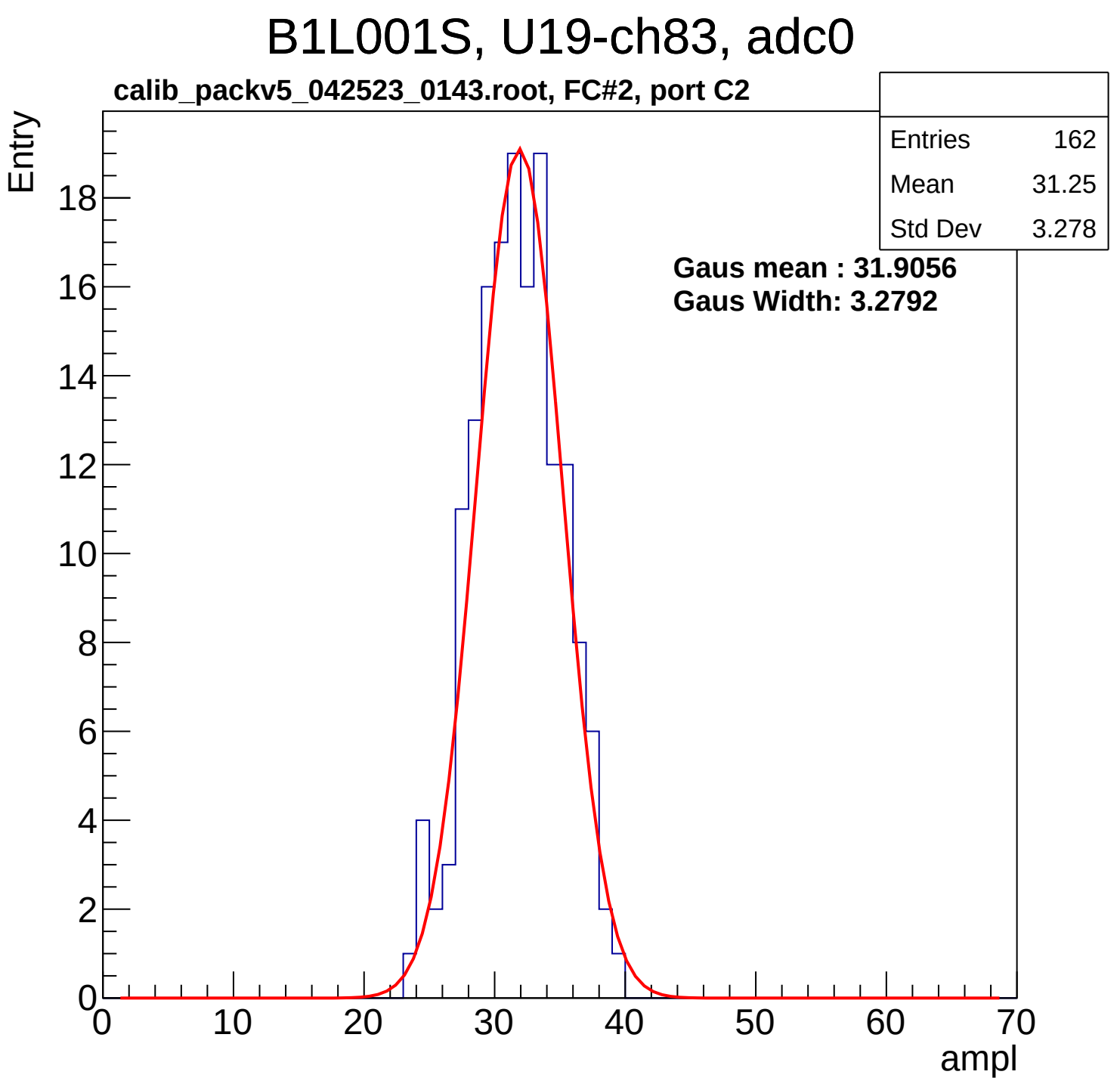
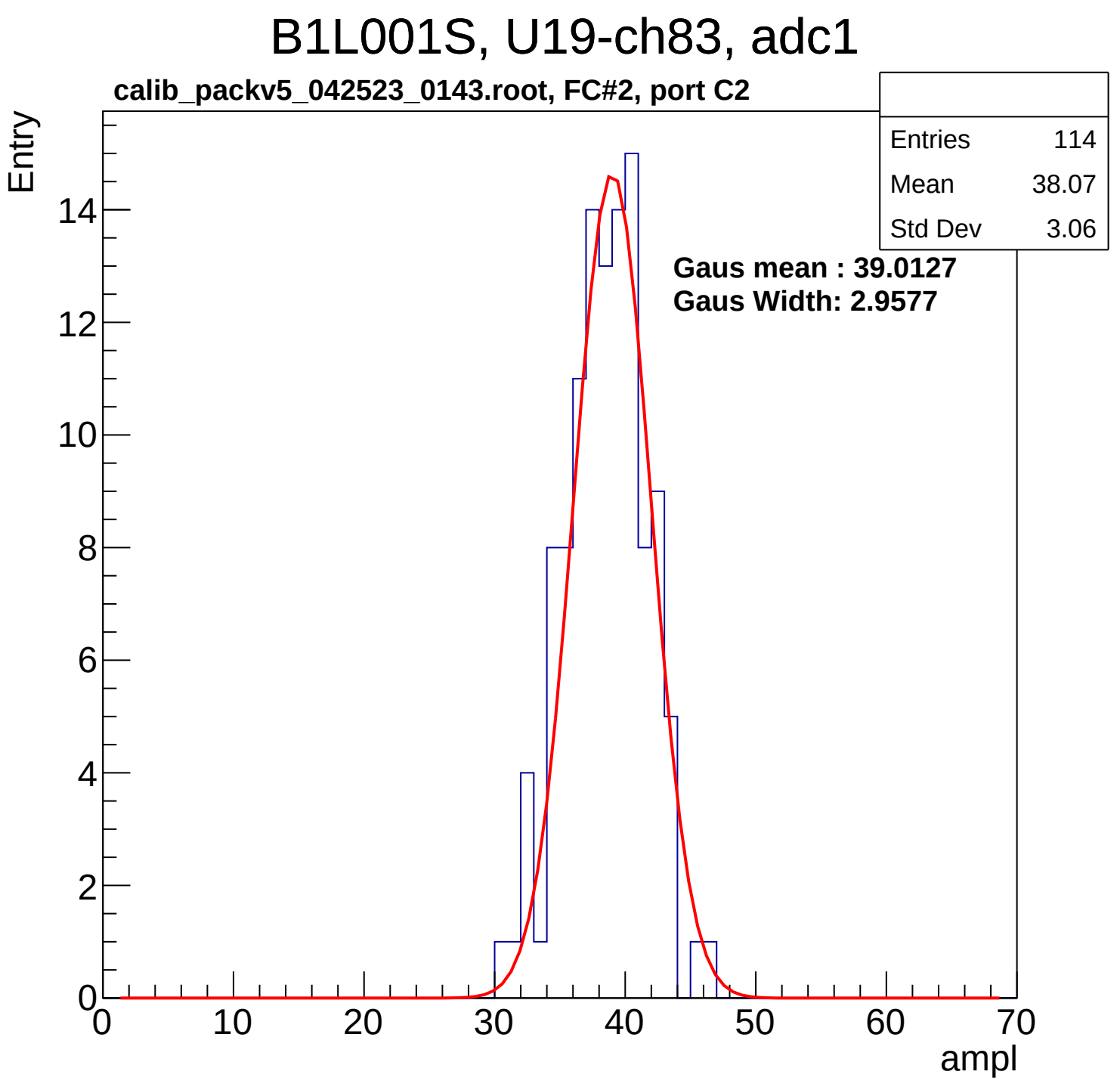
50
60
70
ampl

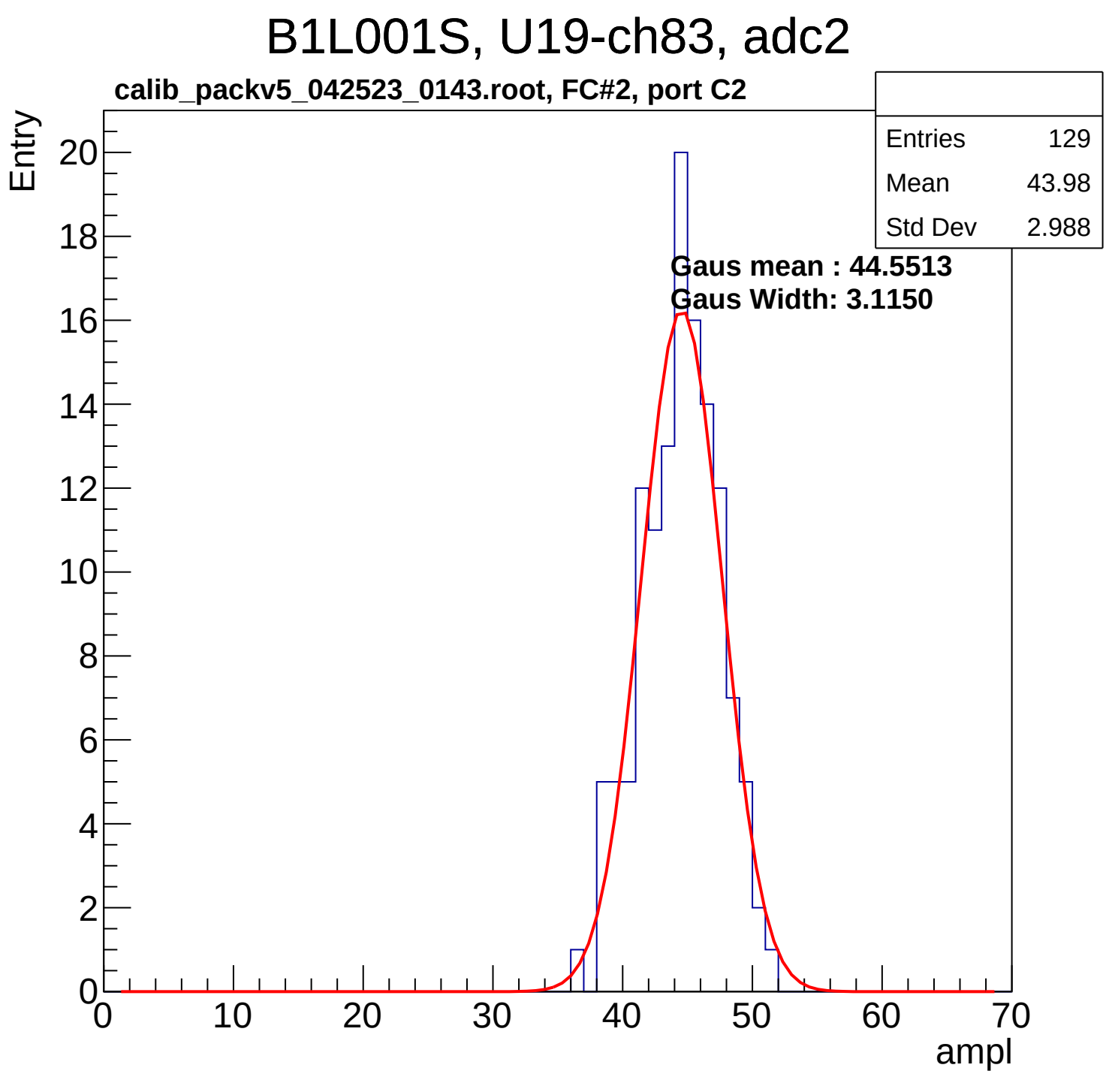

B1L001S, U19-ch82, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 92
Mean 59.24
Std Dev 6.591
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

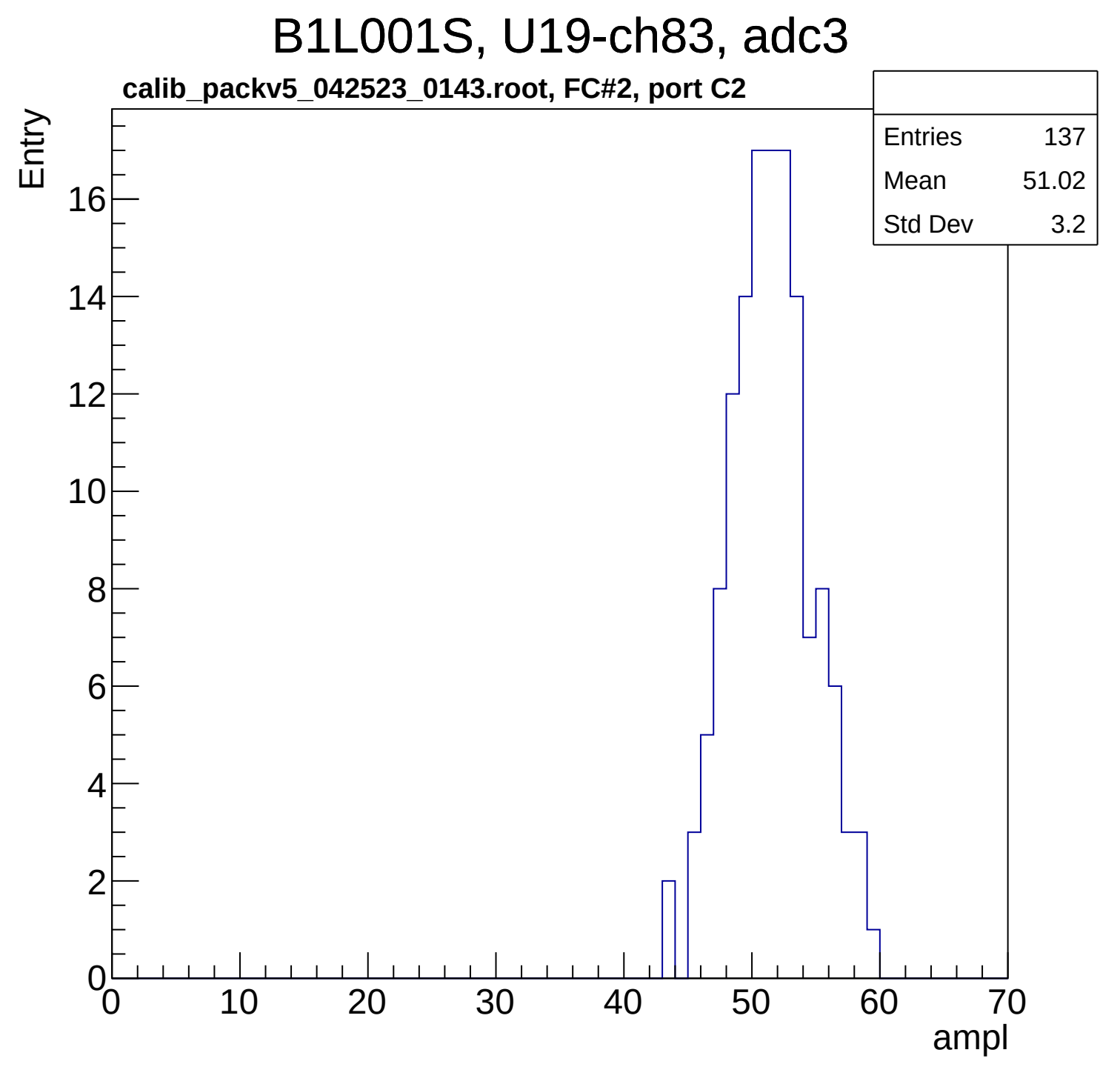

B1L001S, U19-ch82, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 18
Mean 58.44
Std Dev 14.21
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl

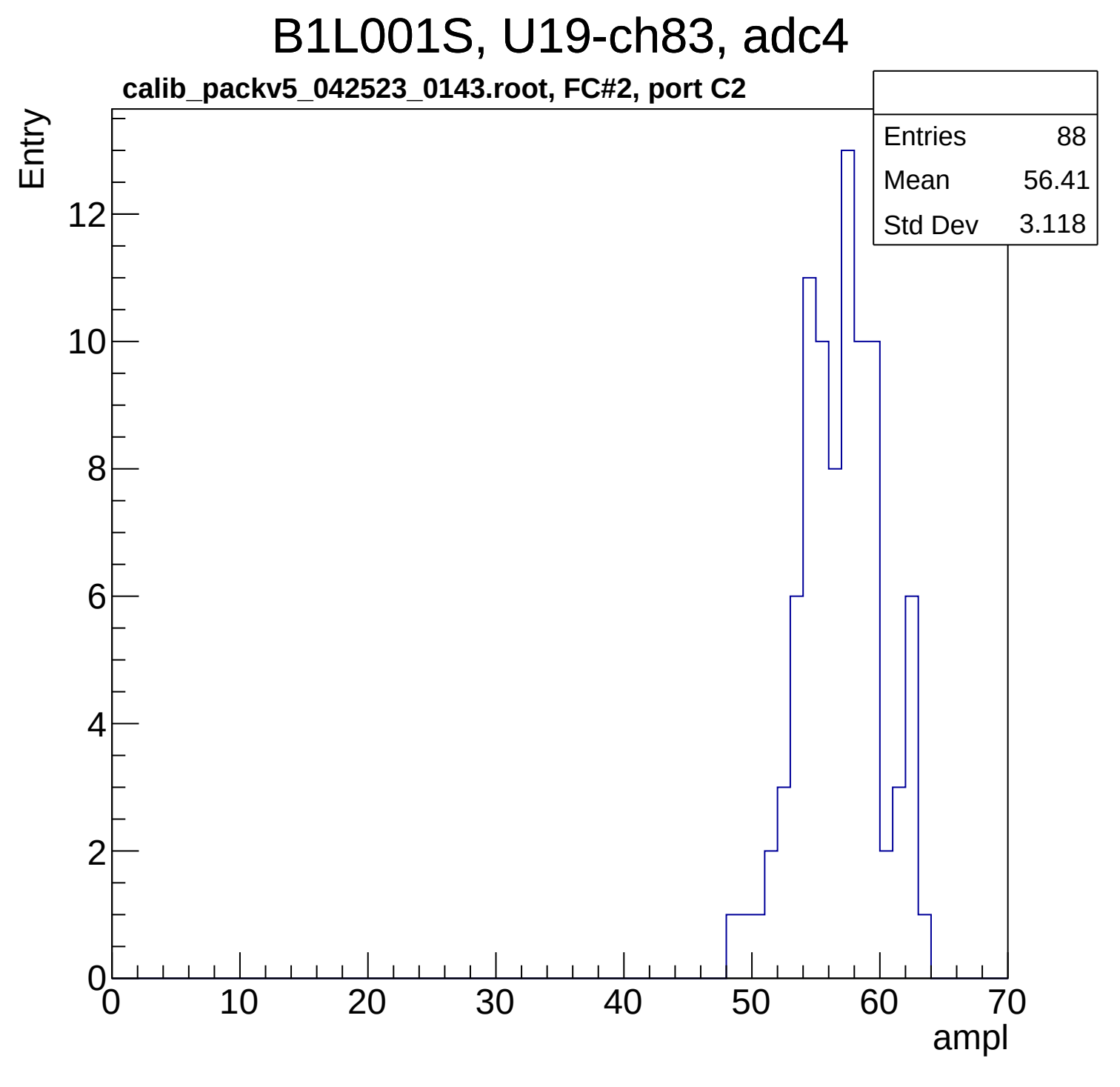

B1L001S, U19-ch82, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 0
Std Dev 0
Entry
2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

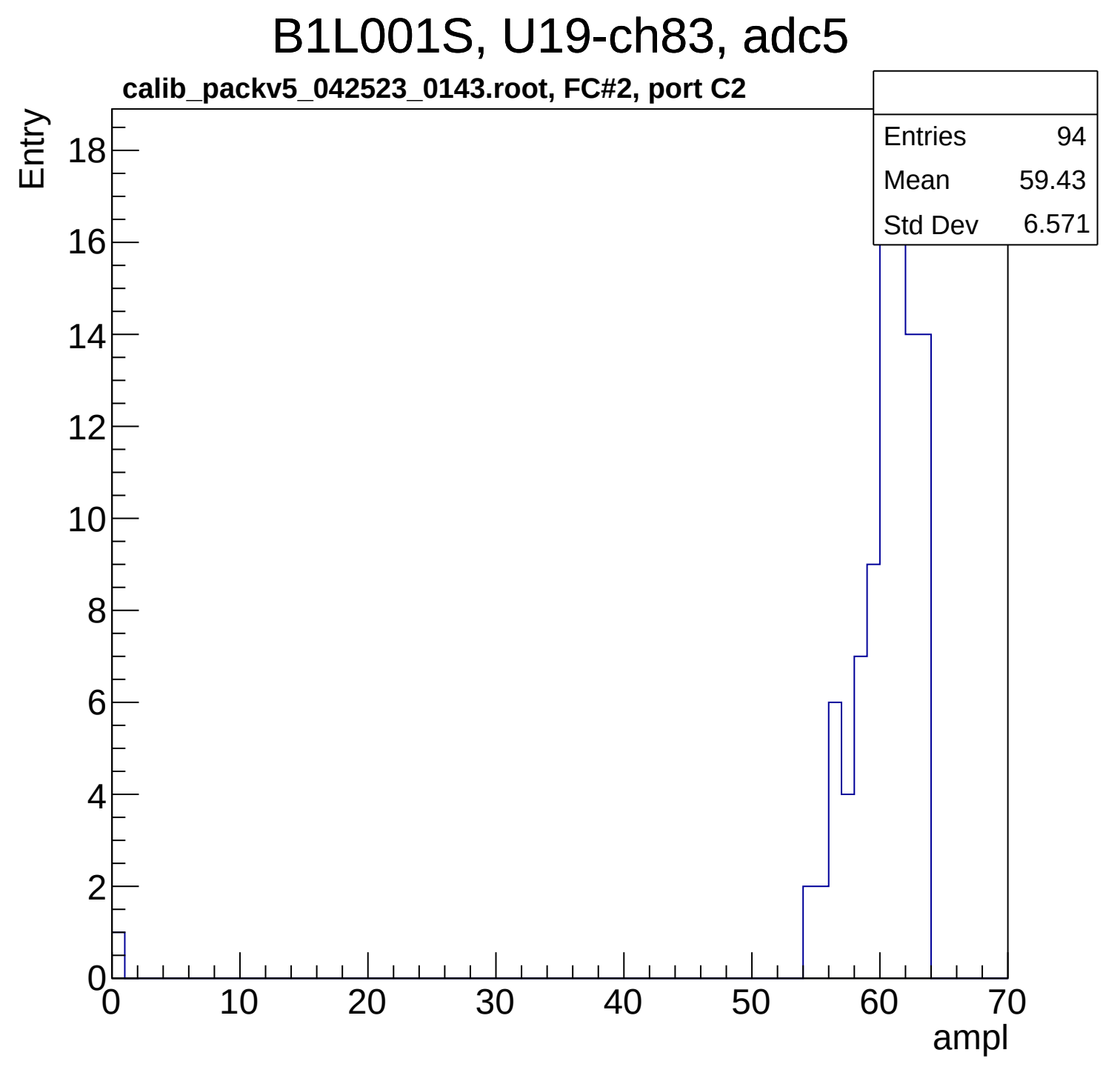

B1L001S, U19-ch83, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 162
Mean 31.25
Std Dev 3.278
Gaus mean : 31.9056
Gaus Width: 3.2792
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

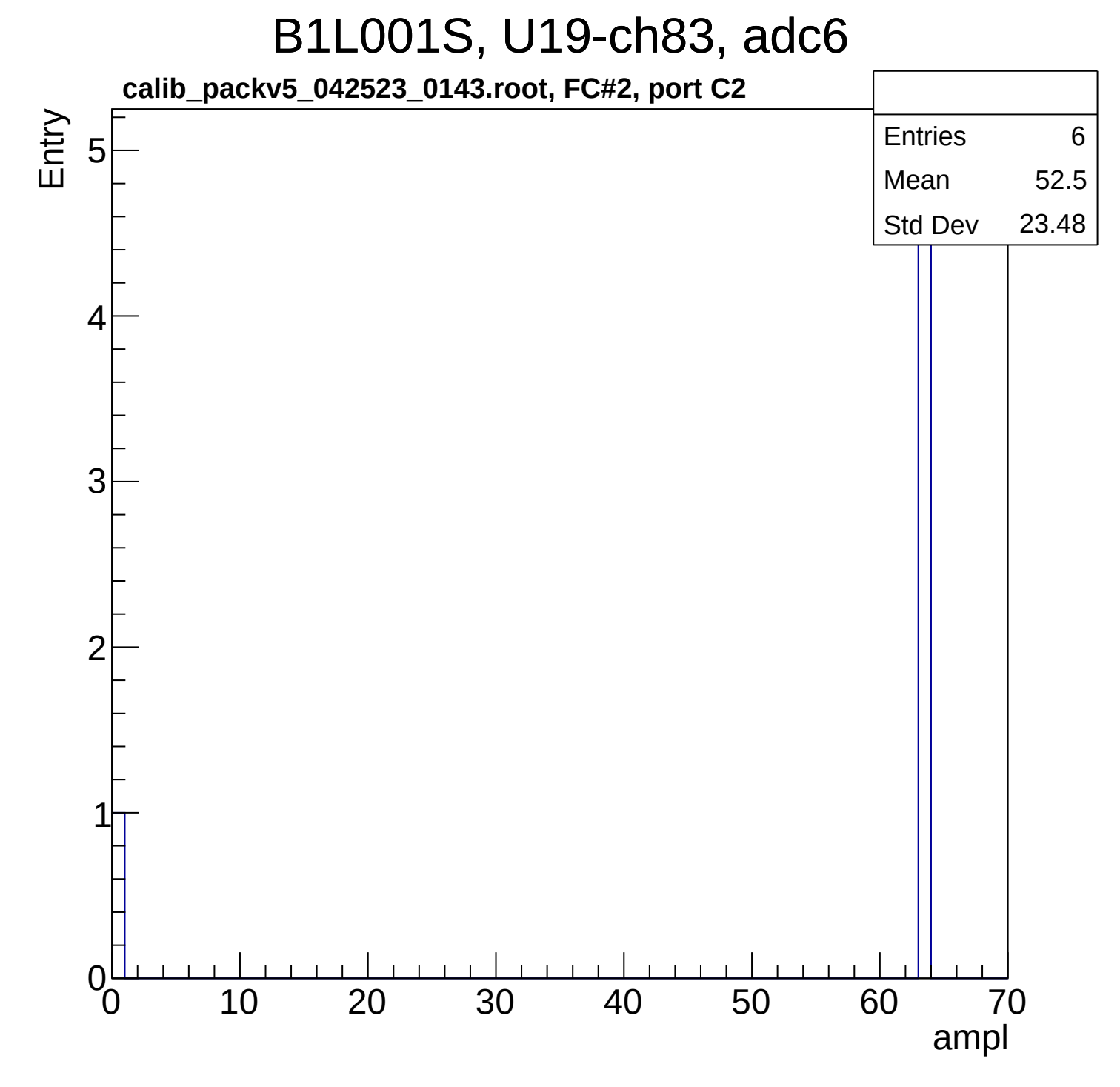

B1L001S, U19-ch83, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 114
Mean 38.07
Std Dev 3.06
Gaus mean : 39.0127
Gaus Width: 2.9577
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

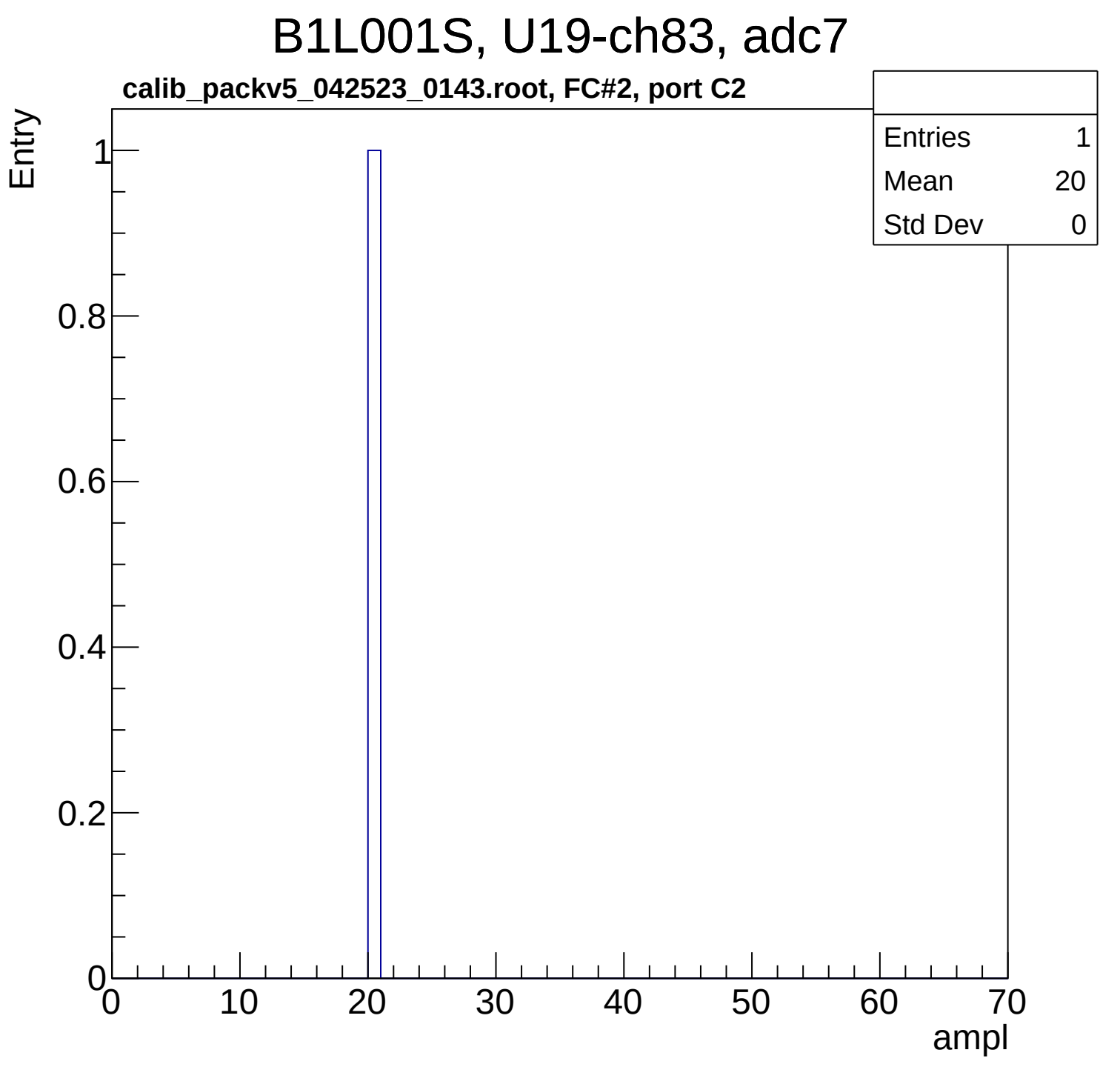

B1L001S, U19-ch83, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 129
Mean 43.98
Std Dev 2.988
Gaus mean : 44.5513
Gaus Width: 3.1150
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

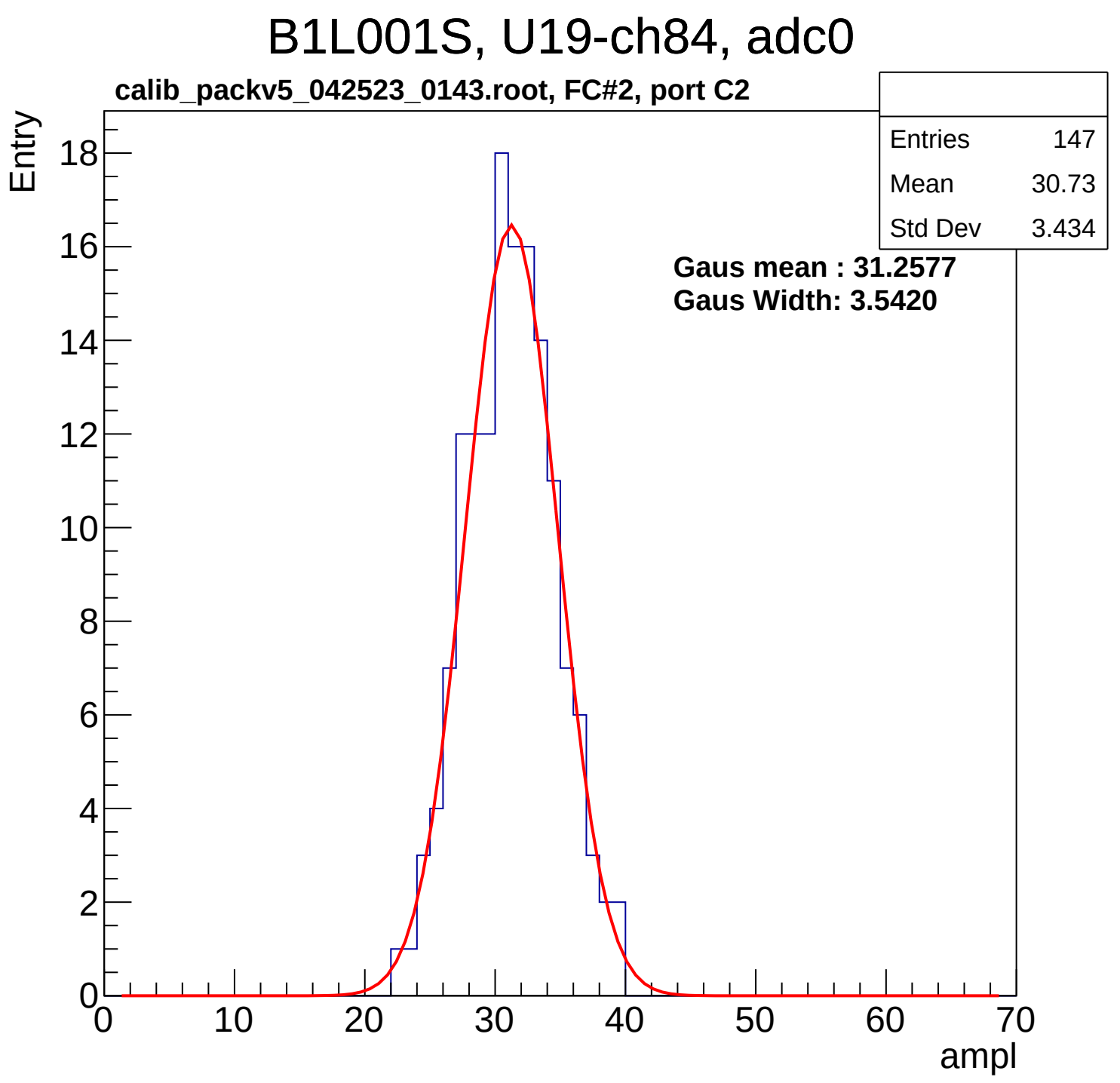

B1L001S, U19-ch83, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 137
Mean 51.02
Std Dev 3.2
Entry
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl

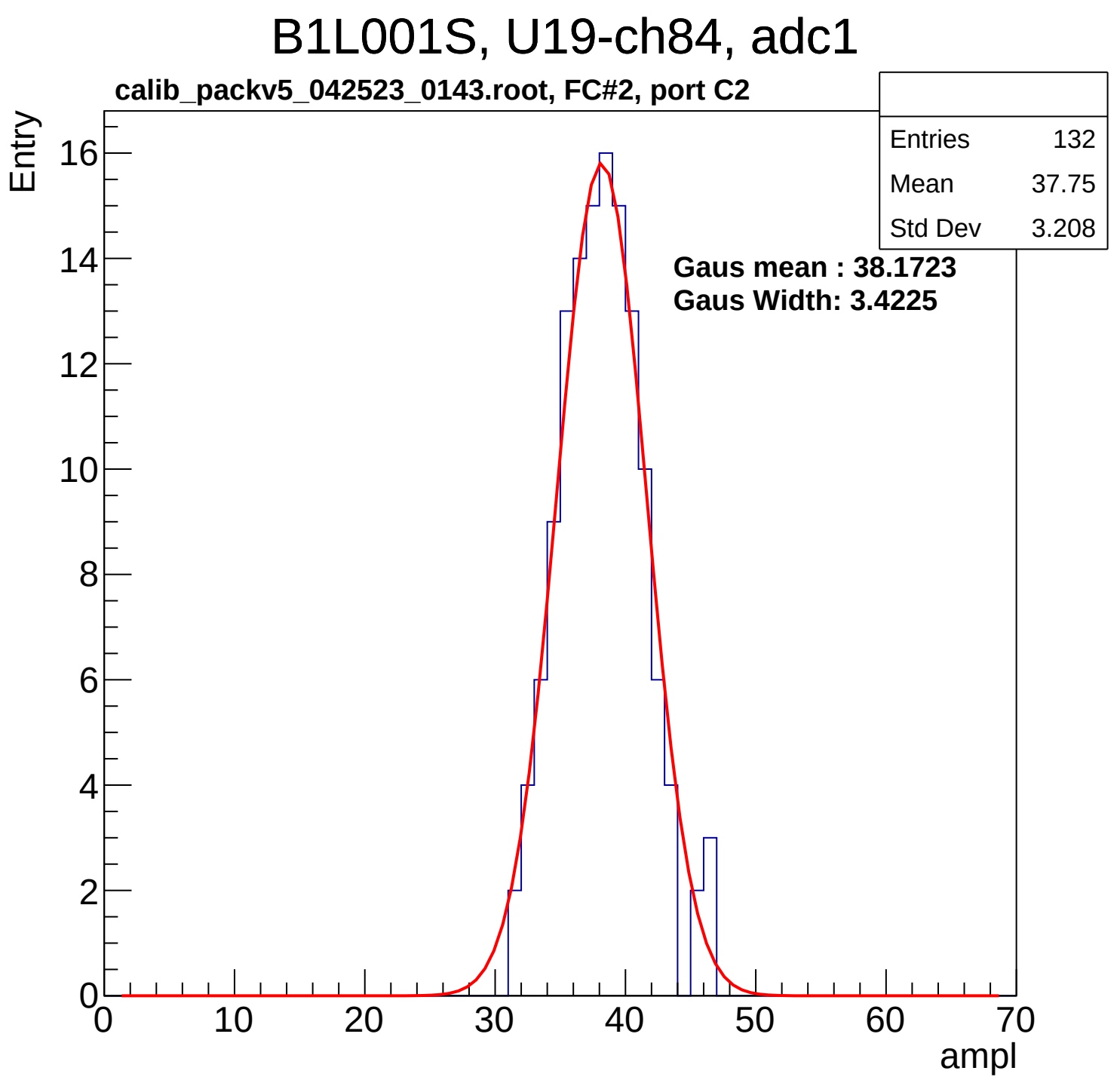

B1L001S, U19-ch83, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 88
Mean 56.41
Std Dev 3.118
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl

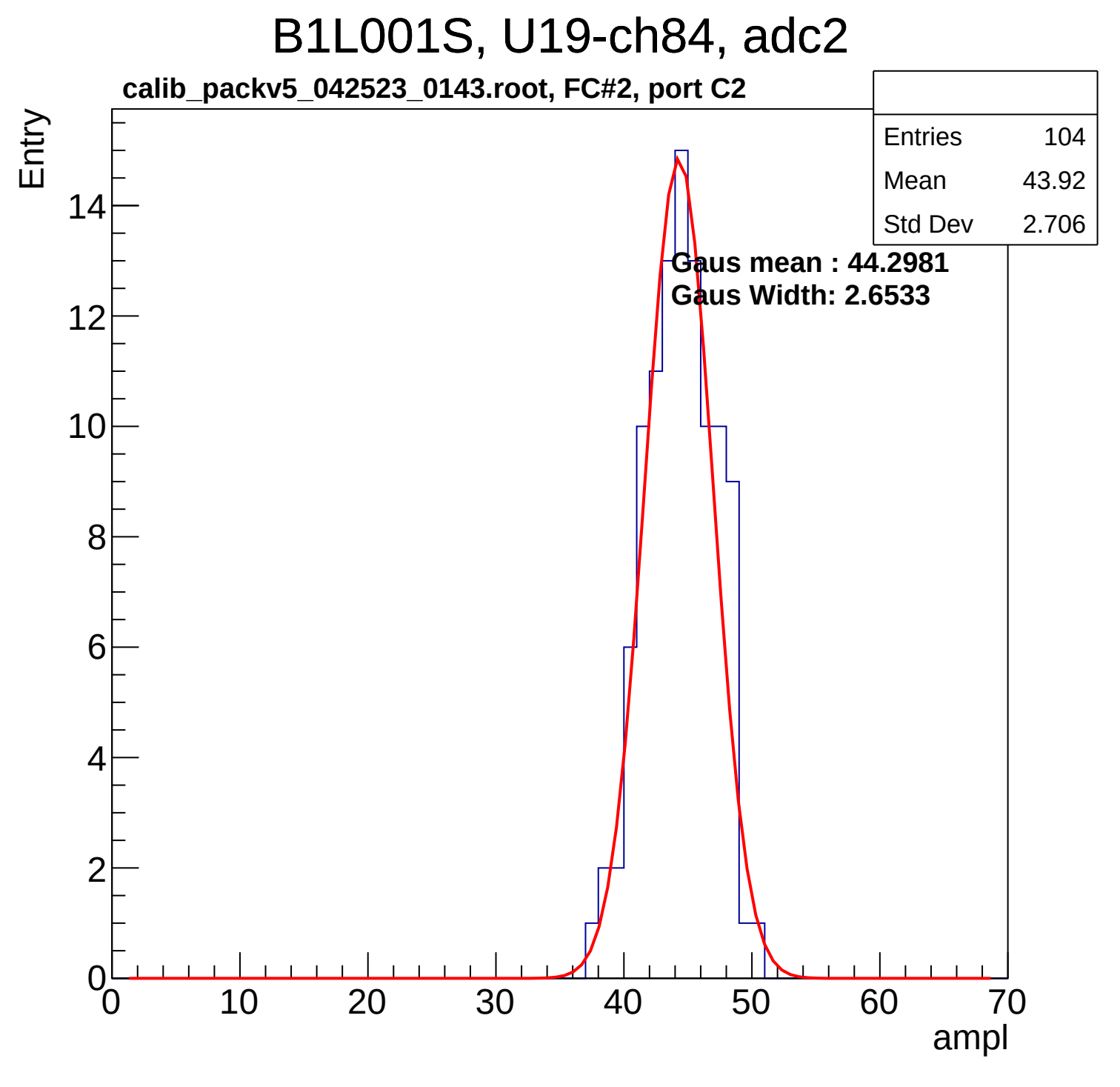

B1L001S, U19-ch83, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 94
Mean 59.43
Std Dev 6.571
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

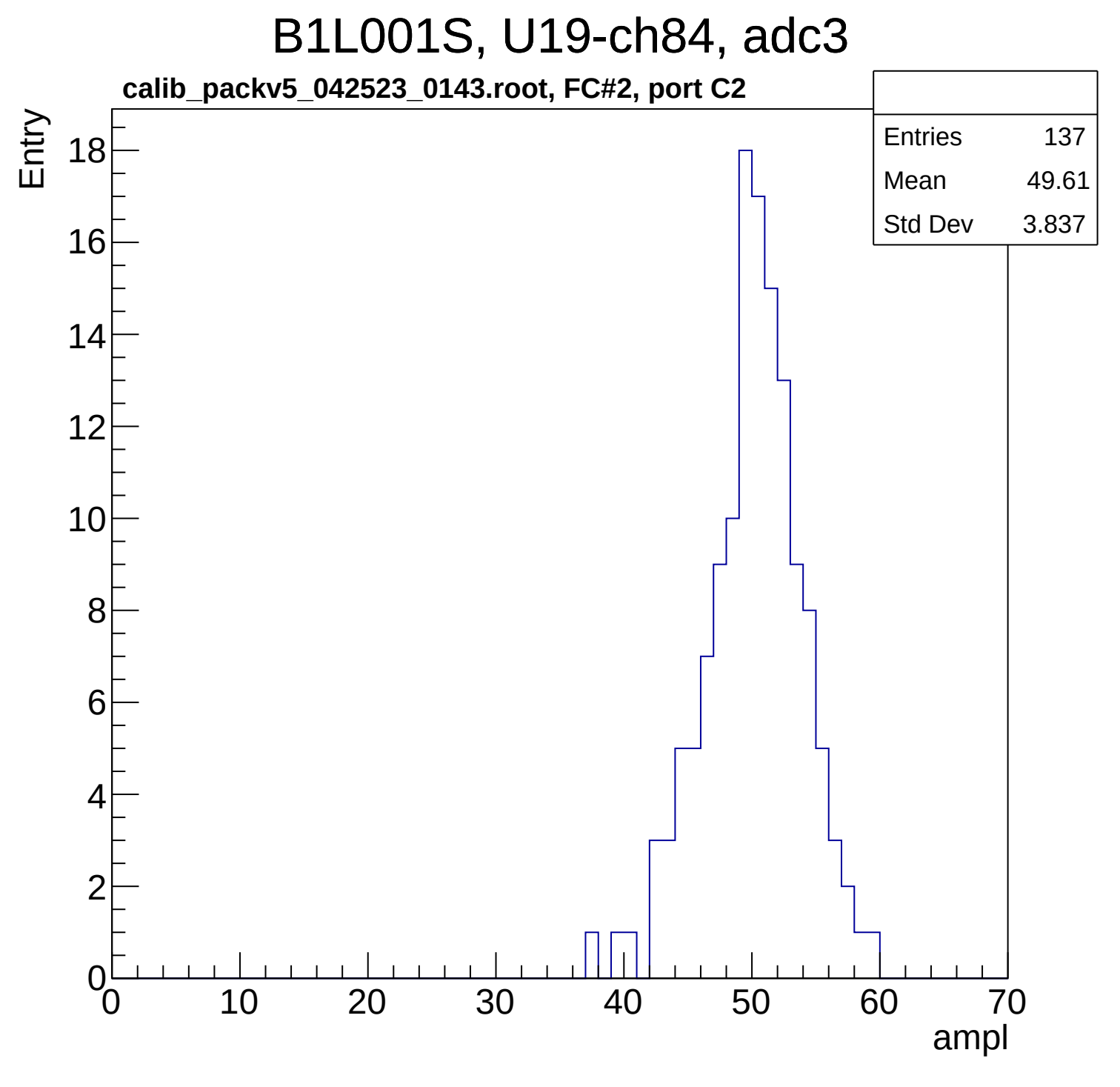

B1L001S, U19-ch83, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 6
Mean 52.5
Std Dev 23.48
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

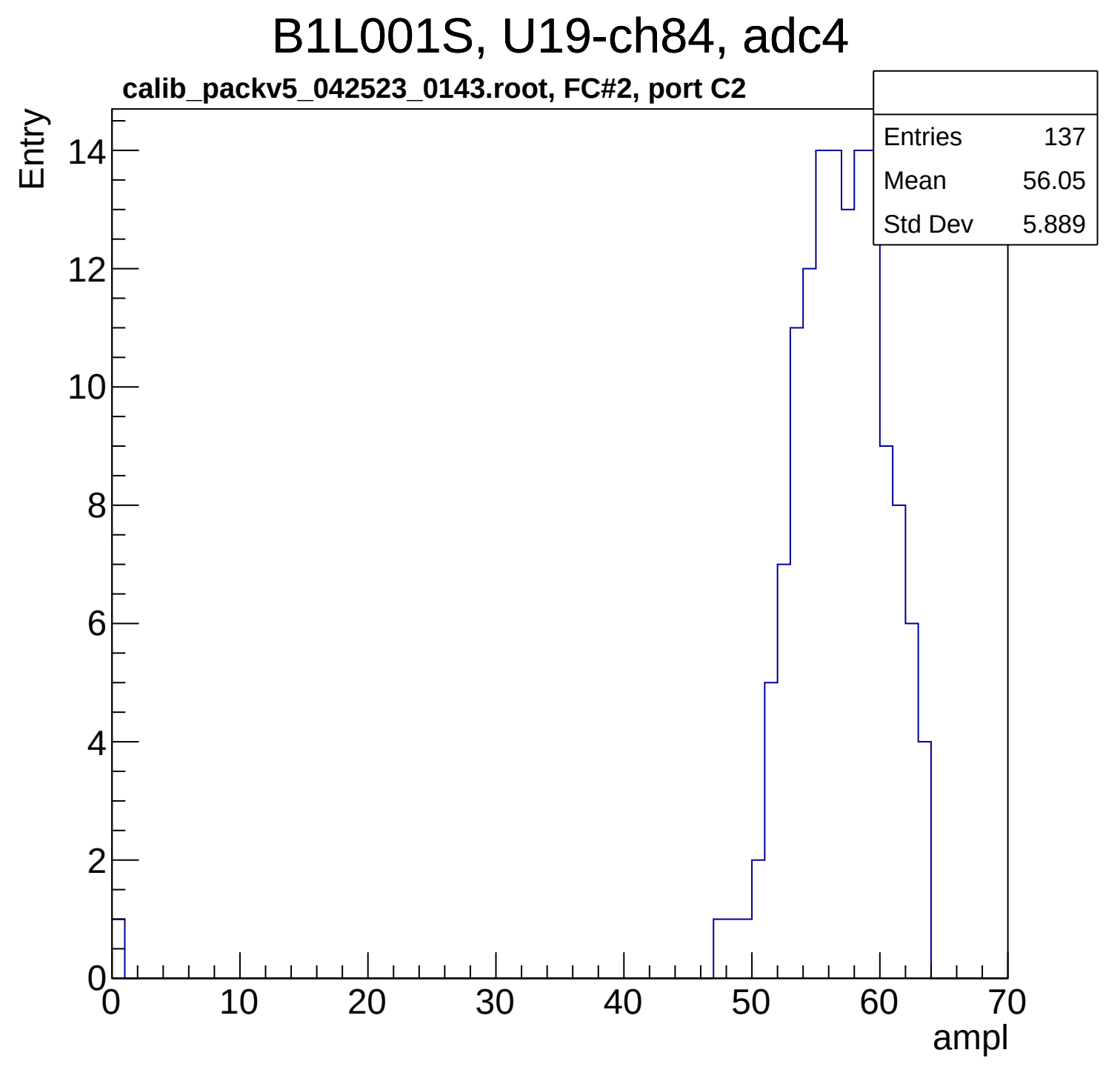

B1L001S, U19-ch83, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 20
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

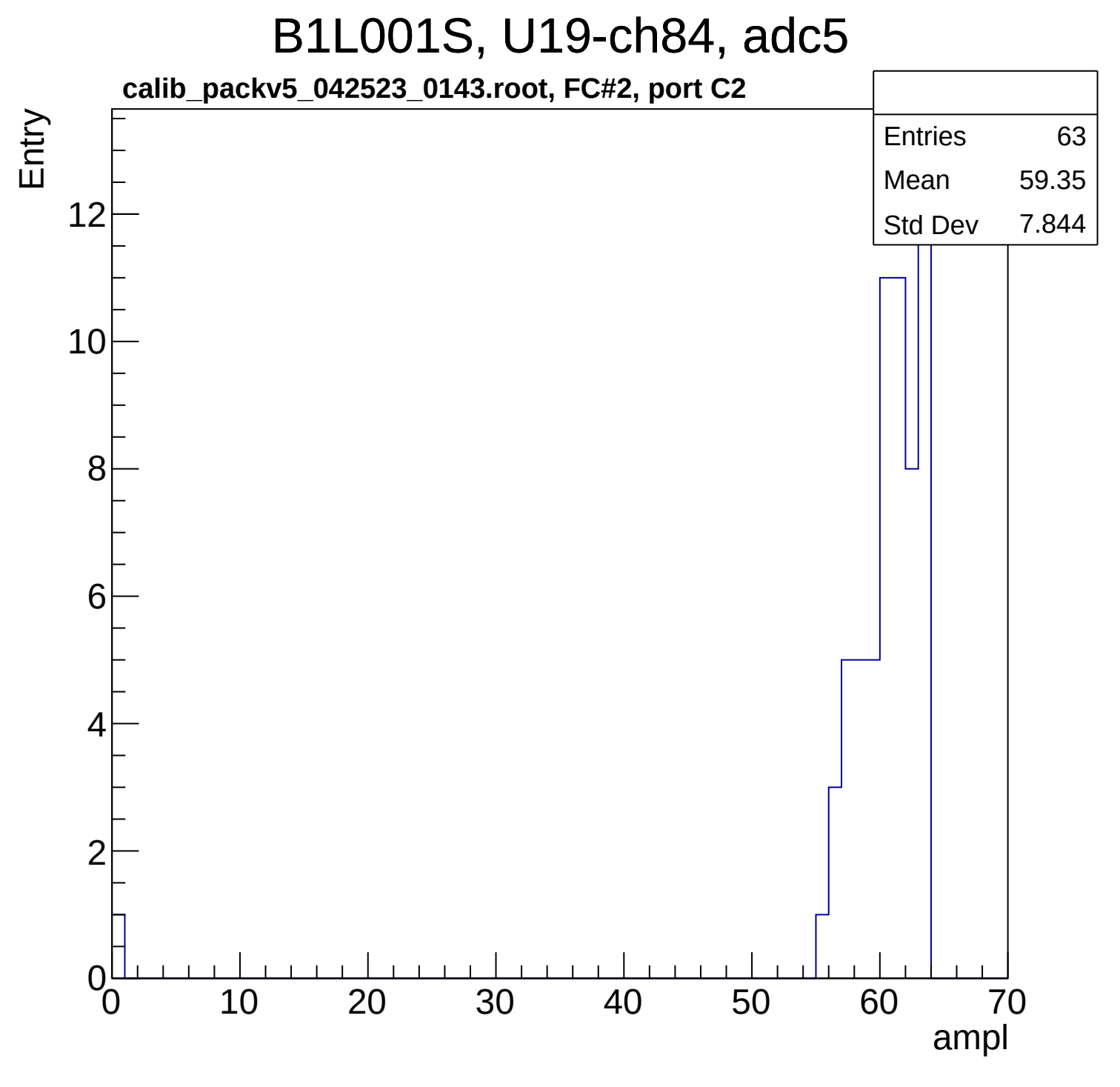

B1L001S, U19-ch84, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 147
Mean 30.73
Std Dev 3.434
Gaus mean : 31.2577
Gaus Width: 3.5420
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

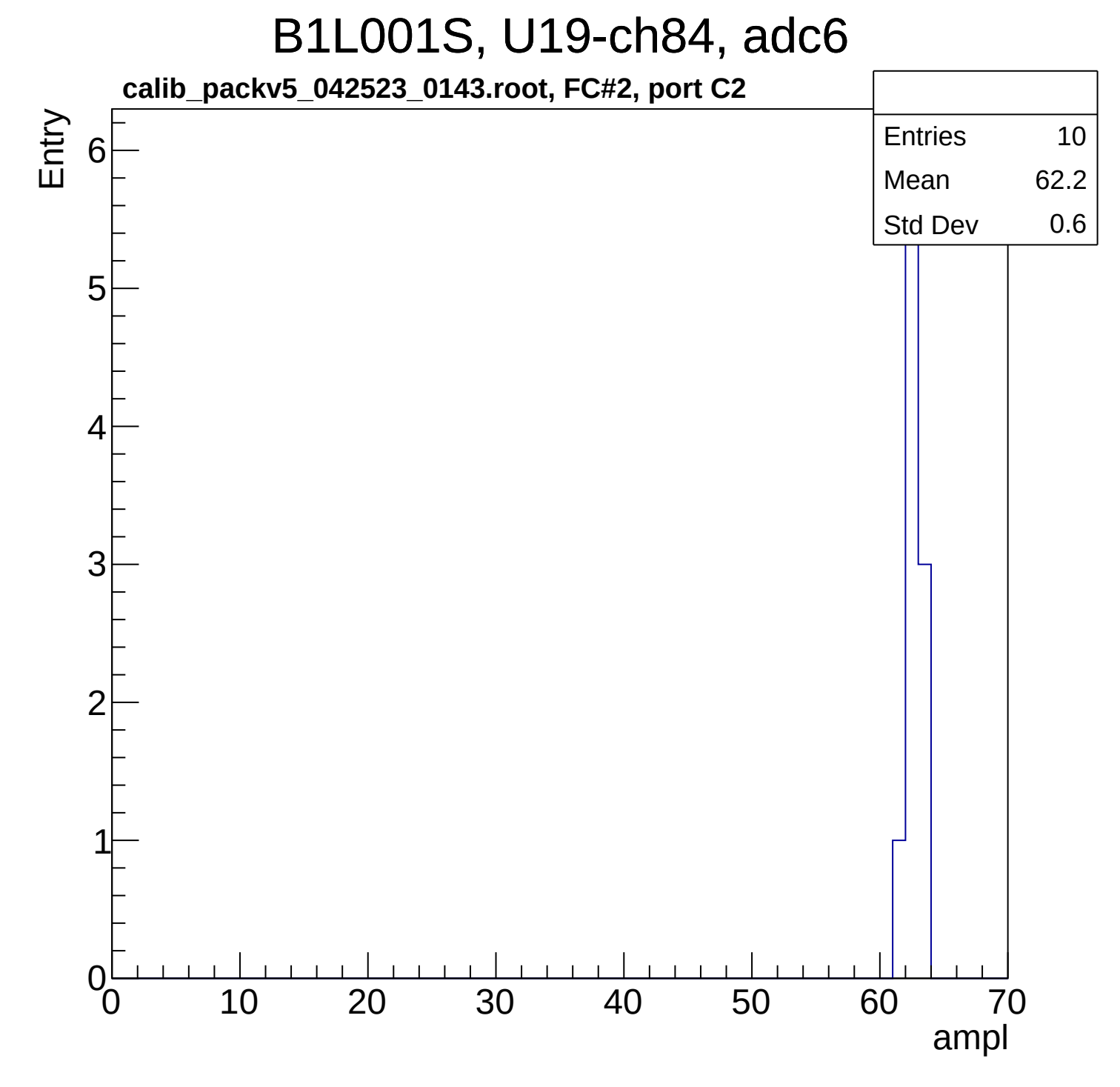

B1L001S, U19-ch84, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 132
Mean 37.75
Std Dev 3.208
Gaus mean : 38.1723
Gaus Width: 3.4225
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

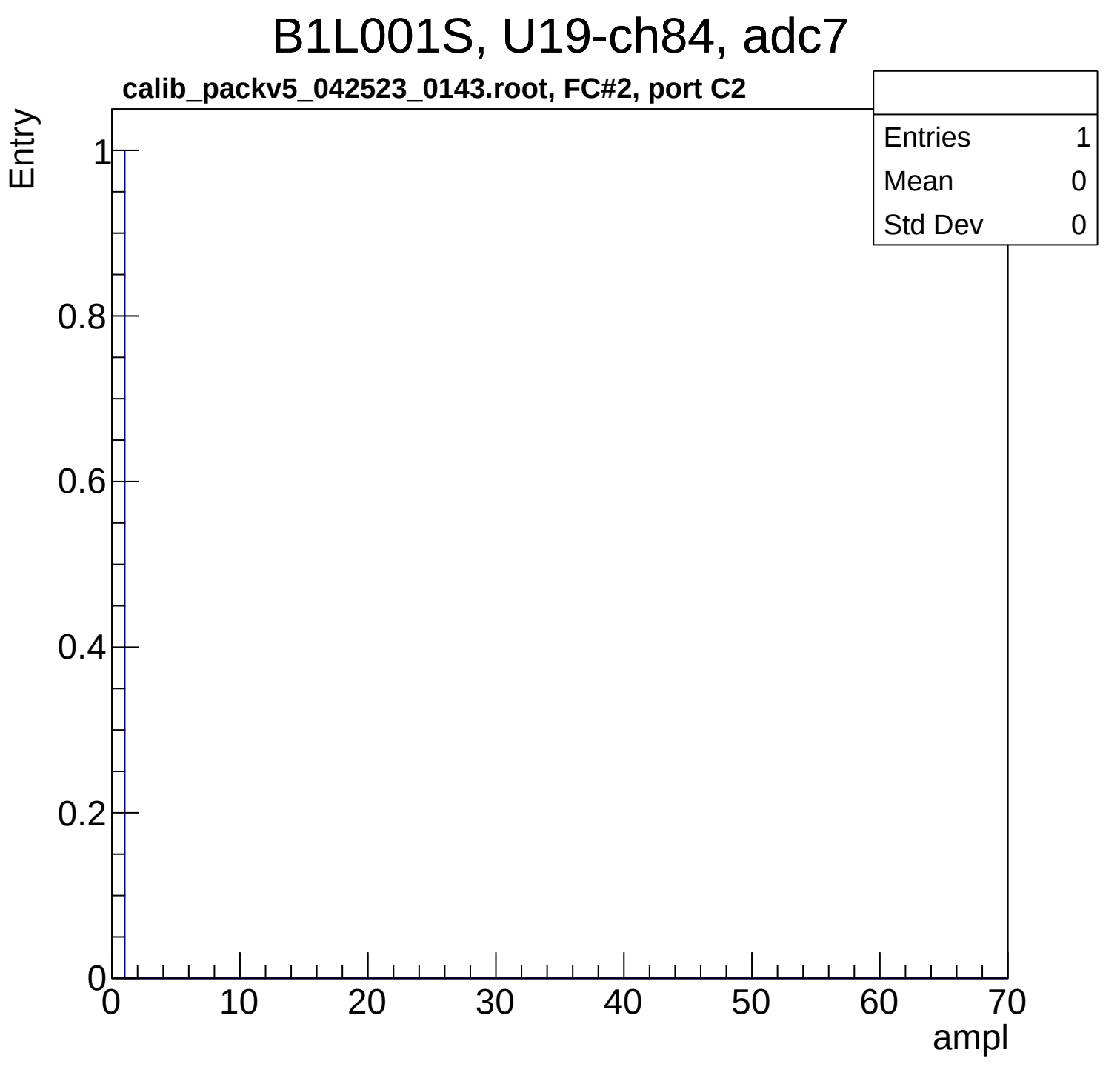

B1L001S, U19-ch84, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 104
Mean 43.92
Std Dev 2.706
Gaus mean : 44.2981
Gaus Width: 2.6533
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

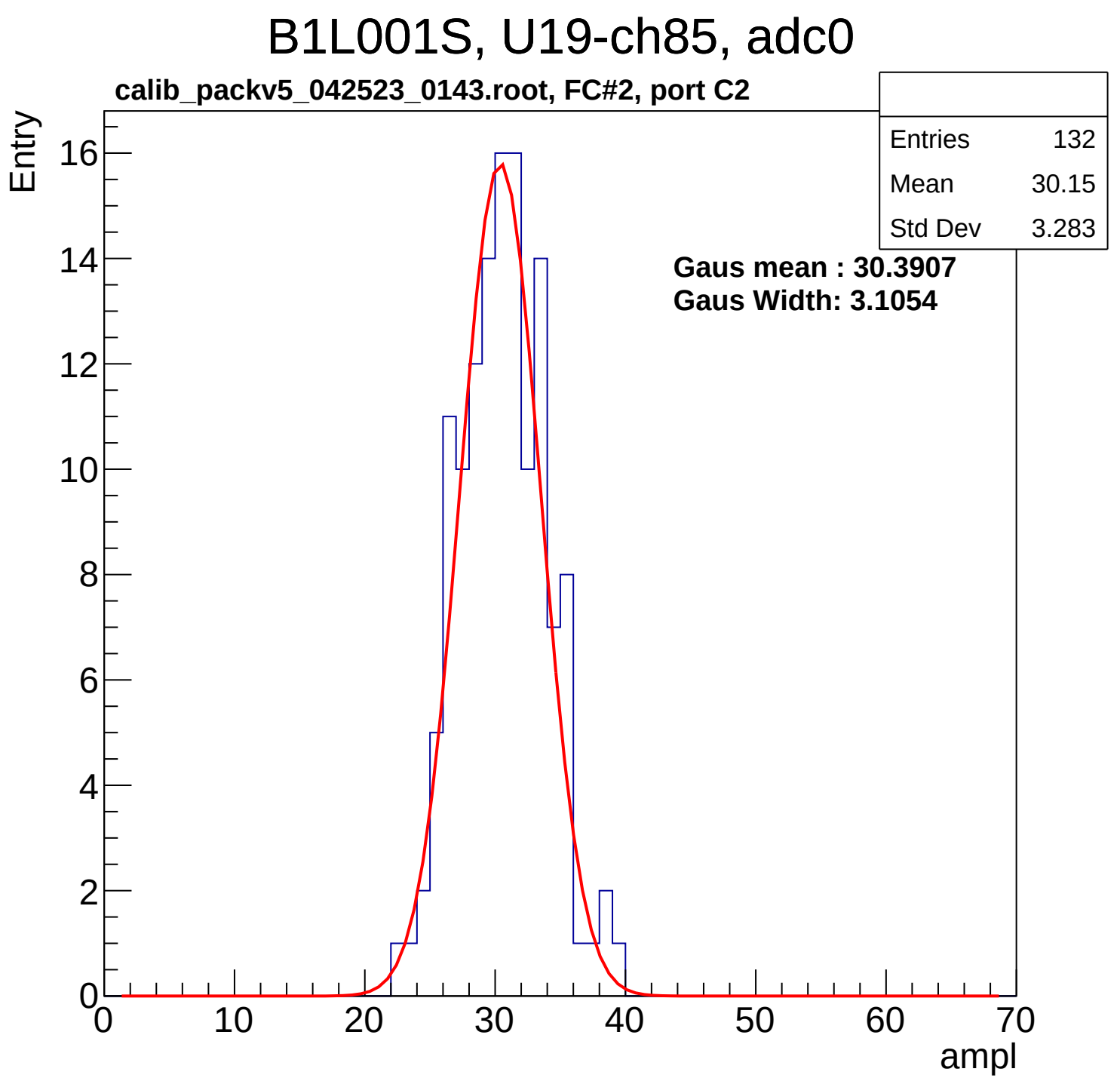

B1L001S, U19-ch84, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 137
Mean 49.61
Std Dev 3.837
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

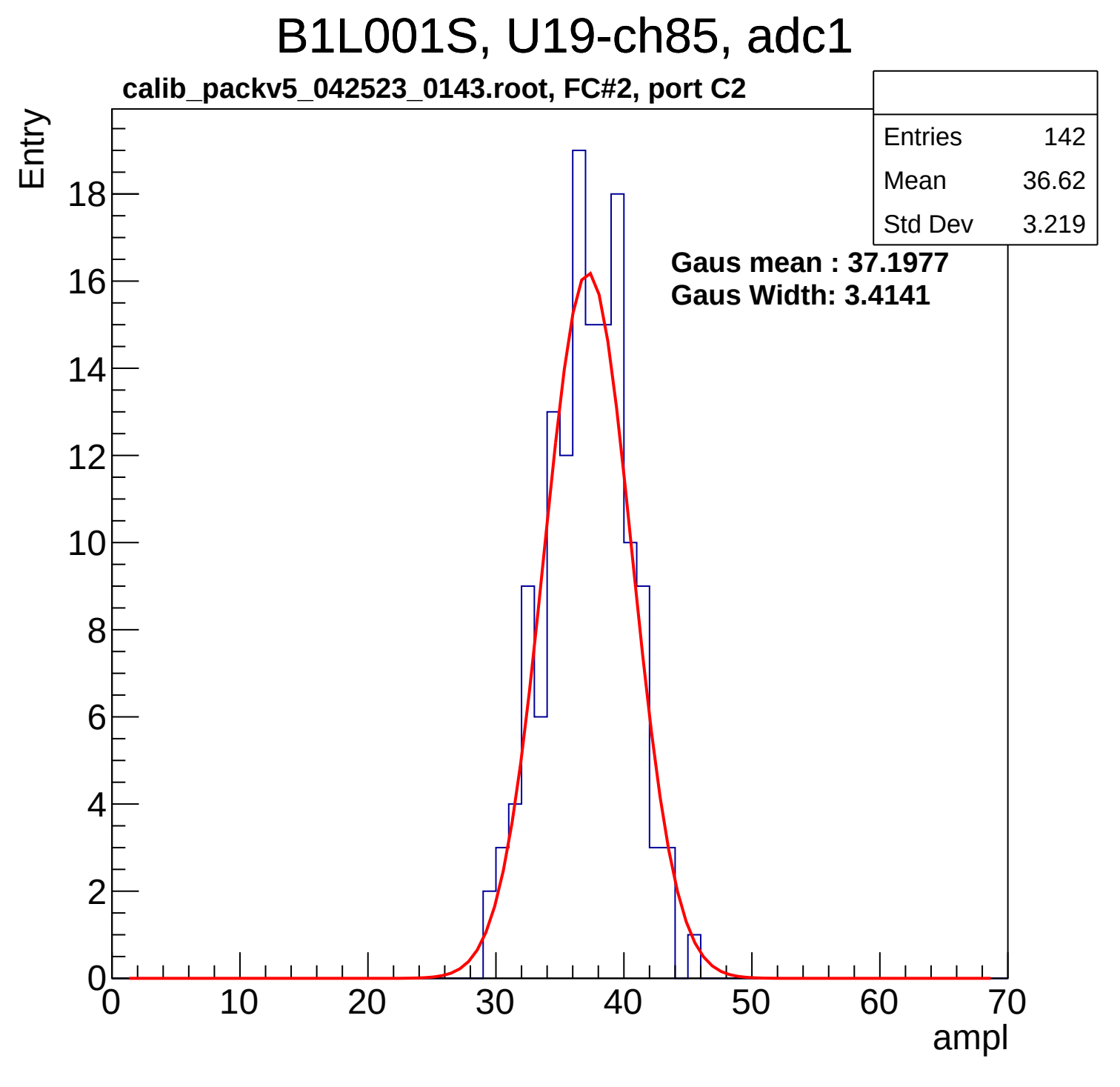

B1L001S, U19-ch84, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 137
Mean 56.05
Std Dev 5.889
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

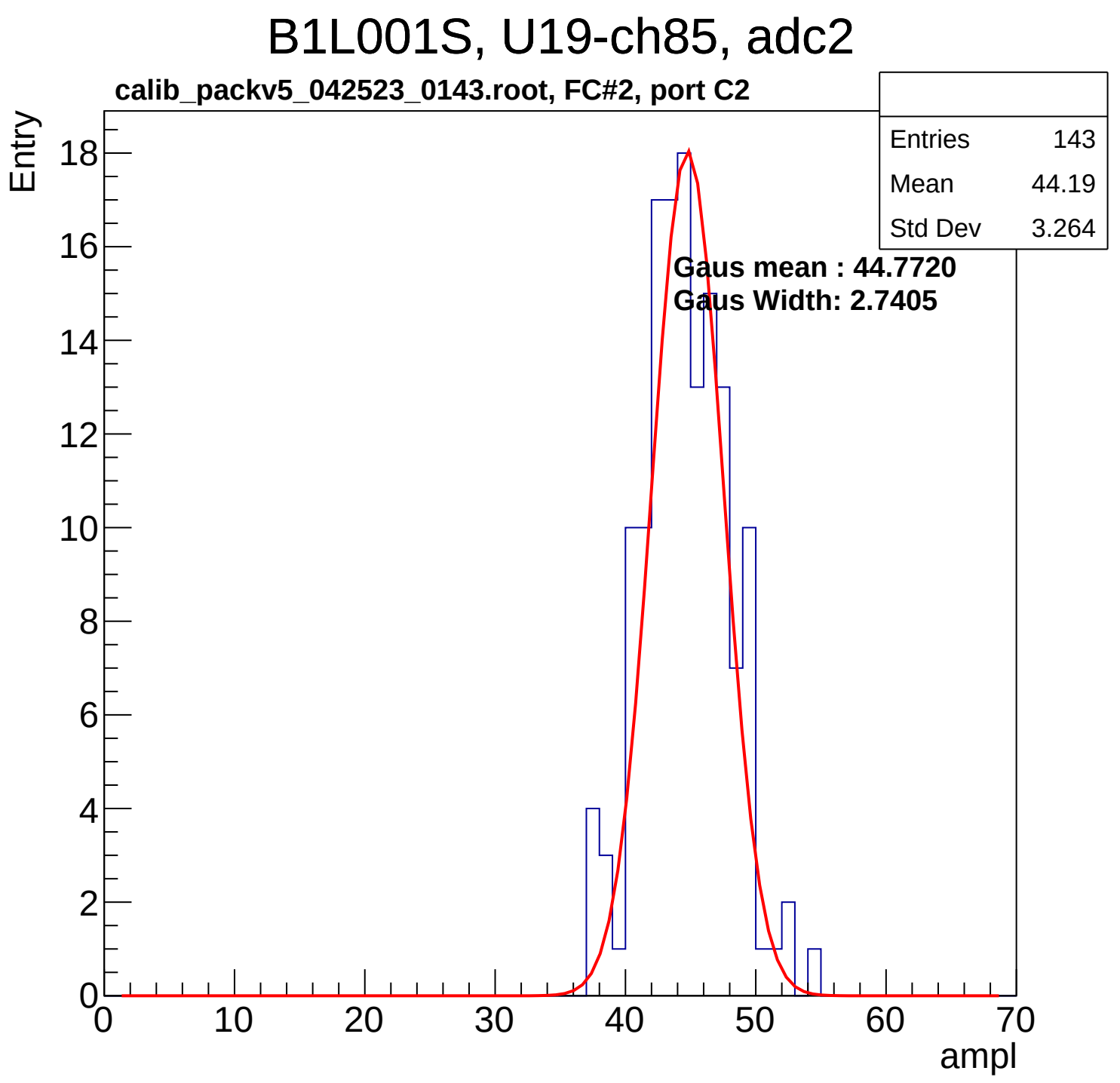

B1L001S, U19-ch84, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 63
Mean 59.35
Std Dev 7.844
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl

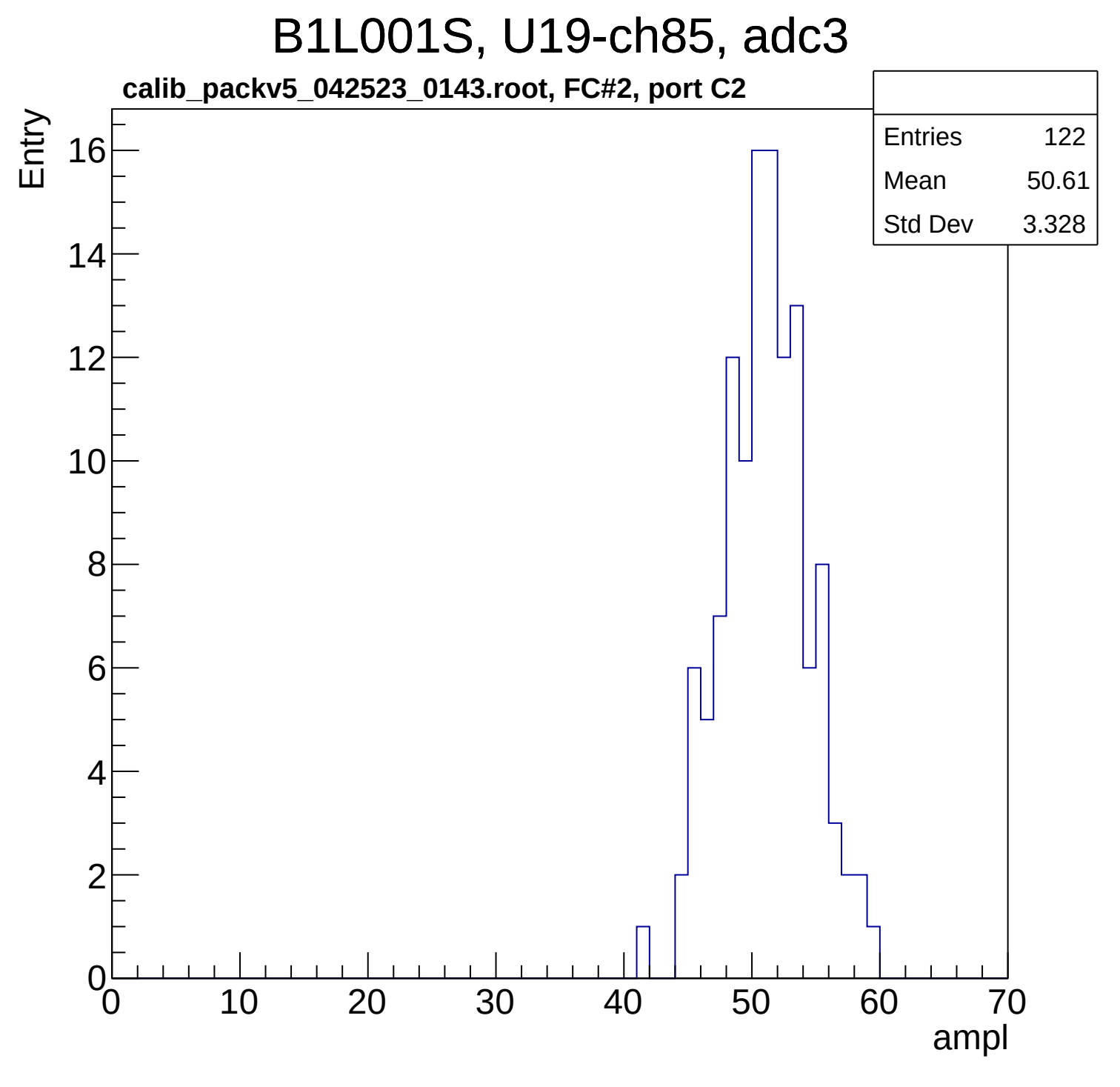

B1L001S, U19-ch84, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 10
Mean 62.2
Std Dev 0.6
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch84, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch85, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 132
Mean 30.15
Std Dev 3.283
Gaus mean : 30.3907
Gaus Width: 3.1054
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70


B1L001S, U19-ch85, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 142
Mean 36.62
Std Dev 3.219
Gaus mean : 37.1977
Gaus Width: 3.4141
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70


B1L001S, U19-ch85, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 143
Mean 44.19
Std Dev 3.264
Gaus mean : 44.7720
Gaus Width: 2.7405
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70


B1L001S, U19-ch85, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 122
Mean 50.61
Std Dev 3.328
Entry
ampl
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2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
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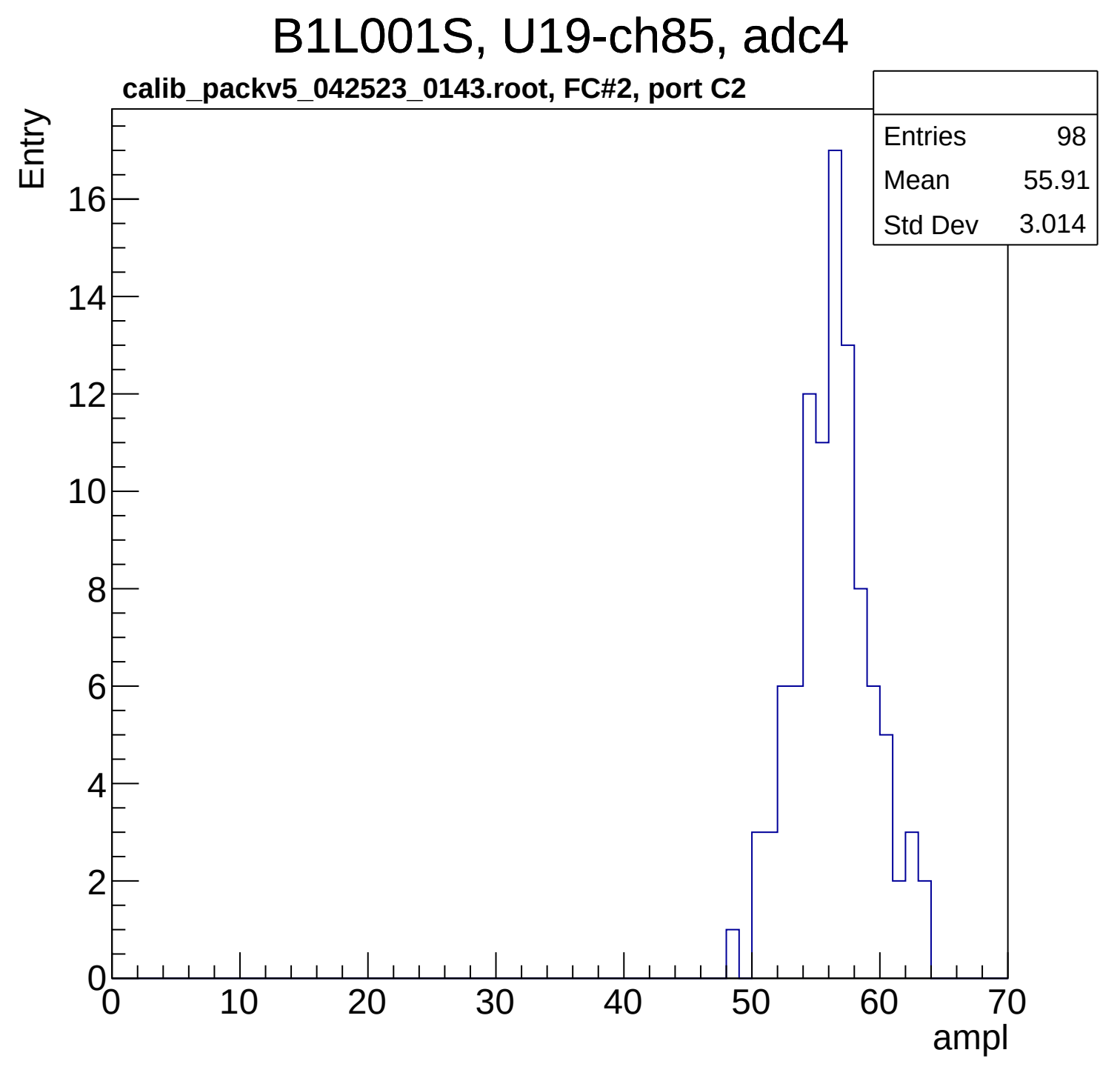
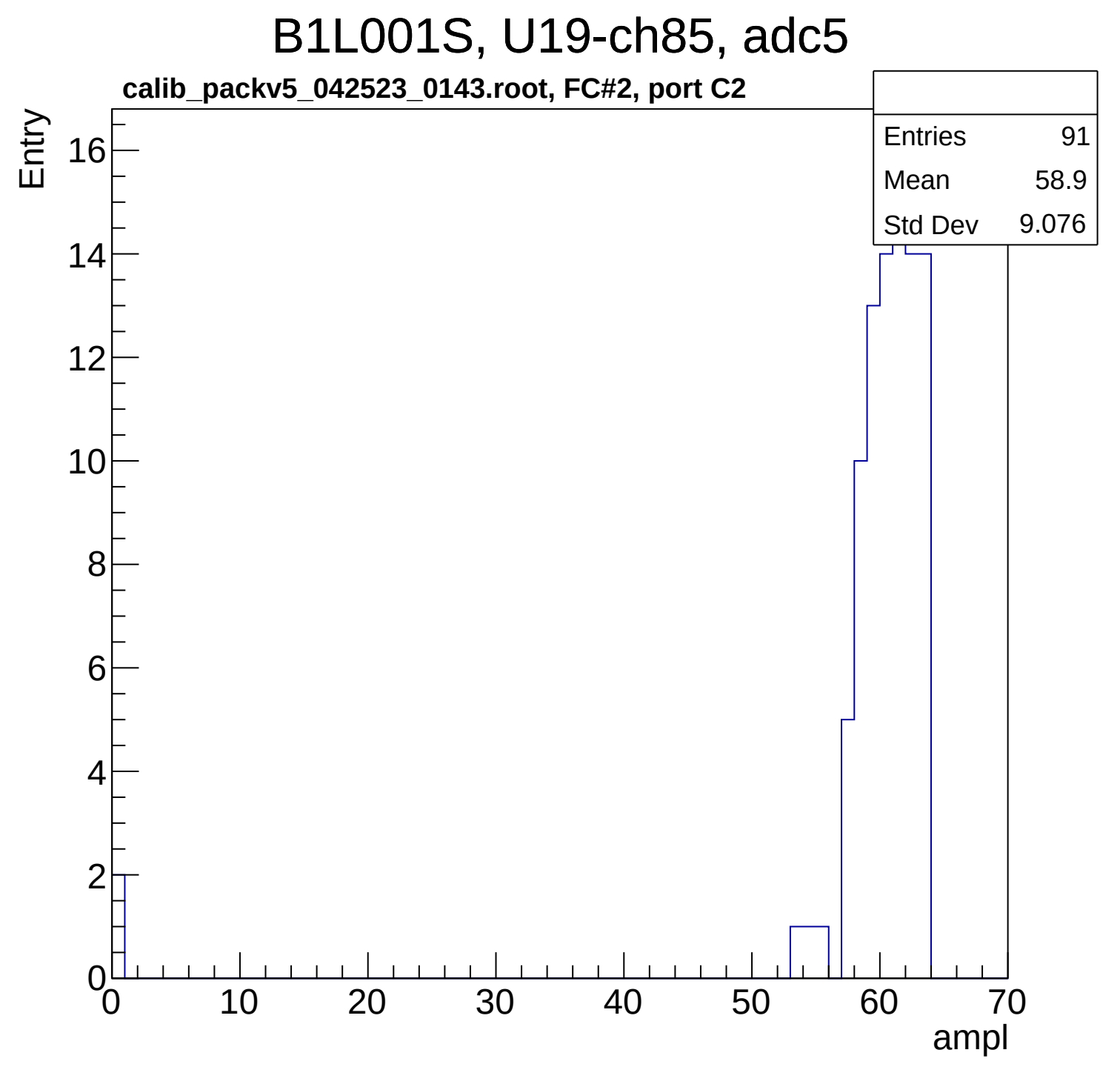

B1L001S, U19-ch85, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 98
Mean 55.91
Std Dev 3.014
Entry
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch85, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 91
Mean 58.9
Std Dev 9.076
Entry
ampl
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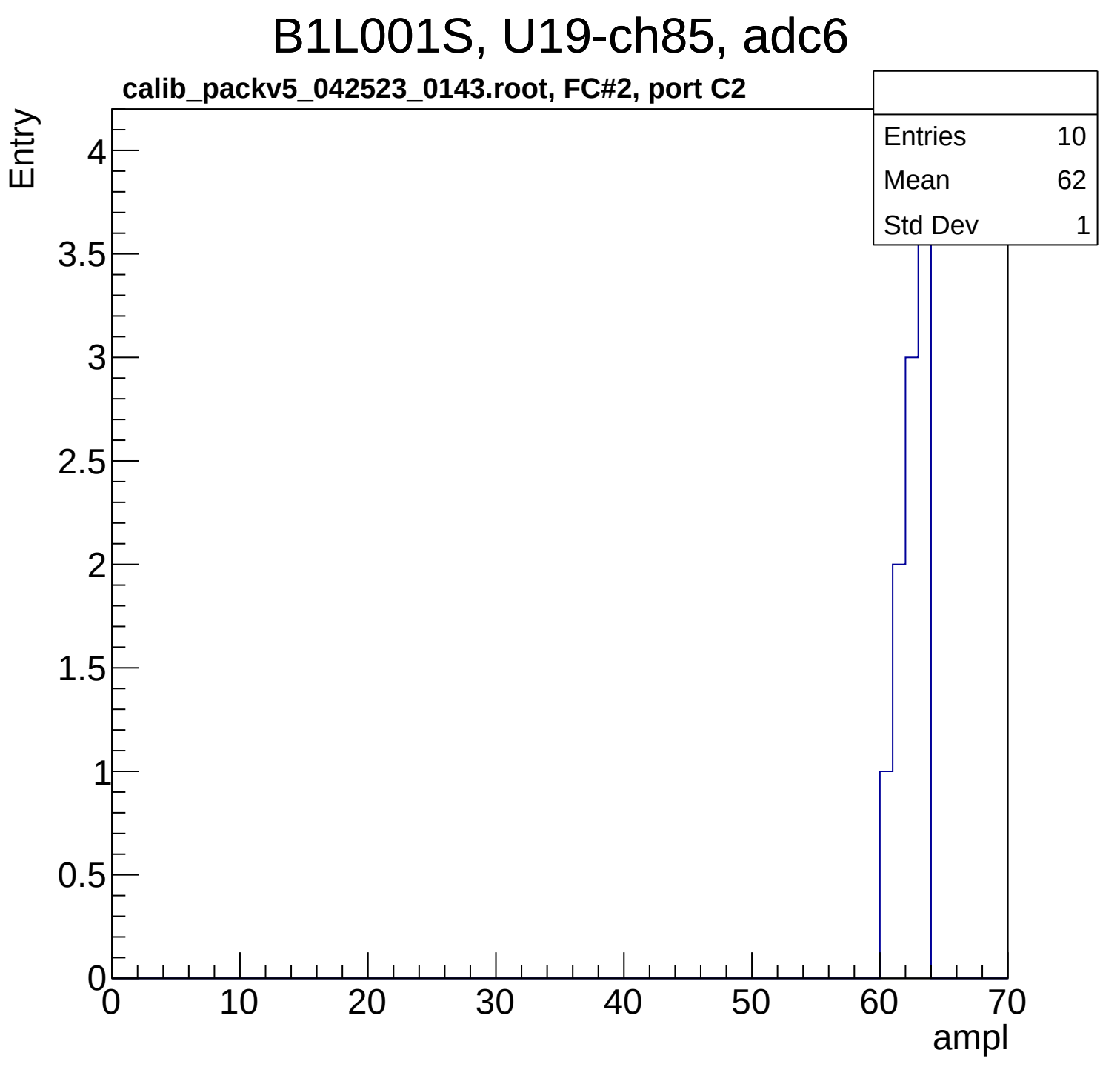
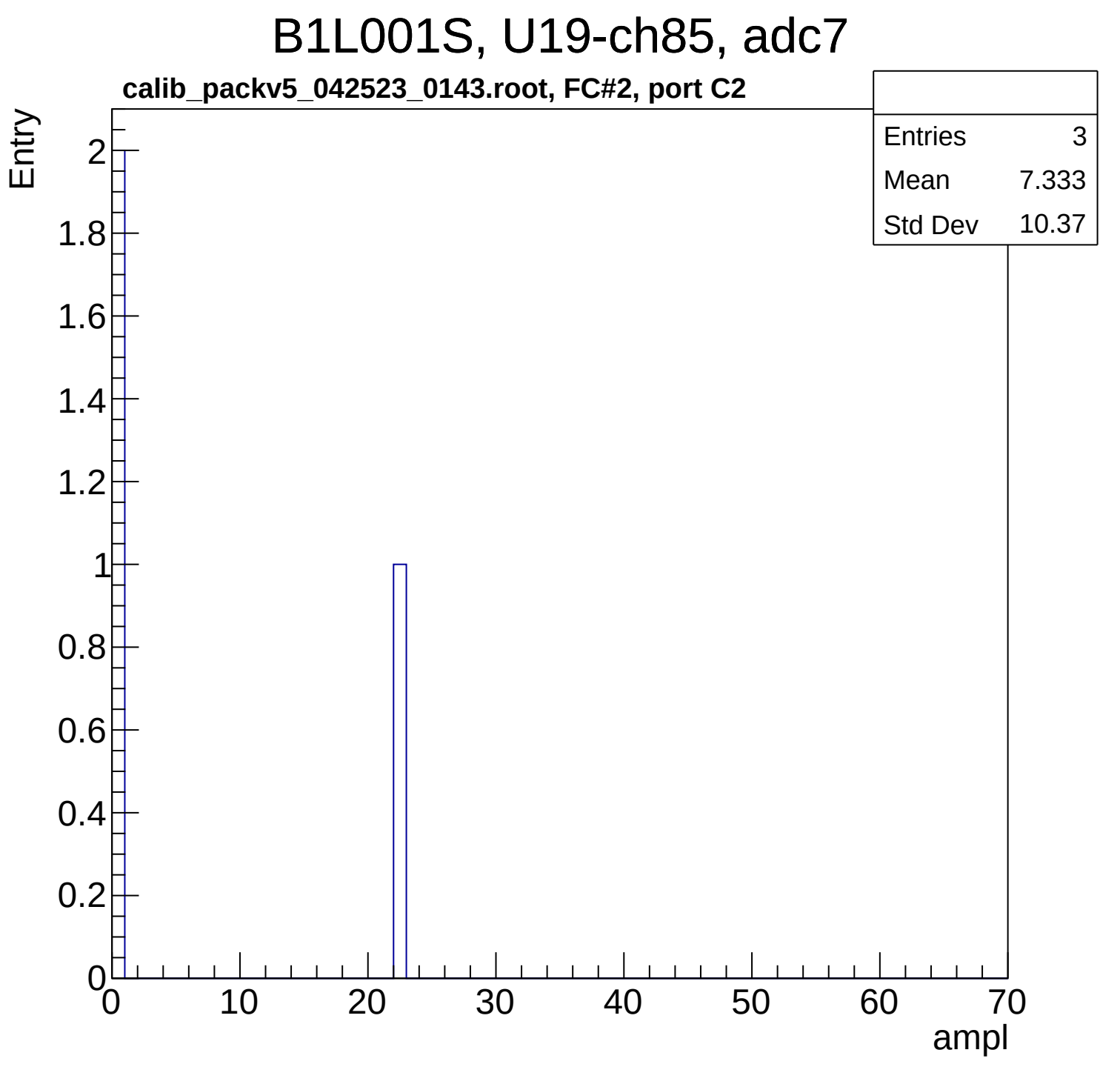
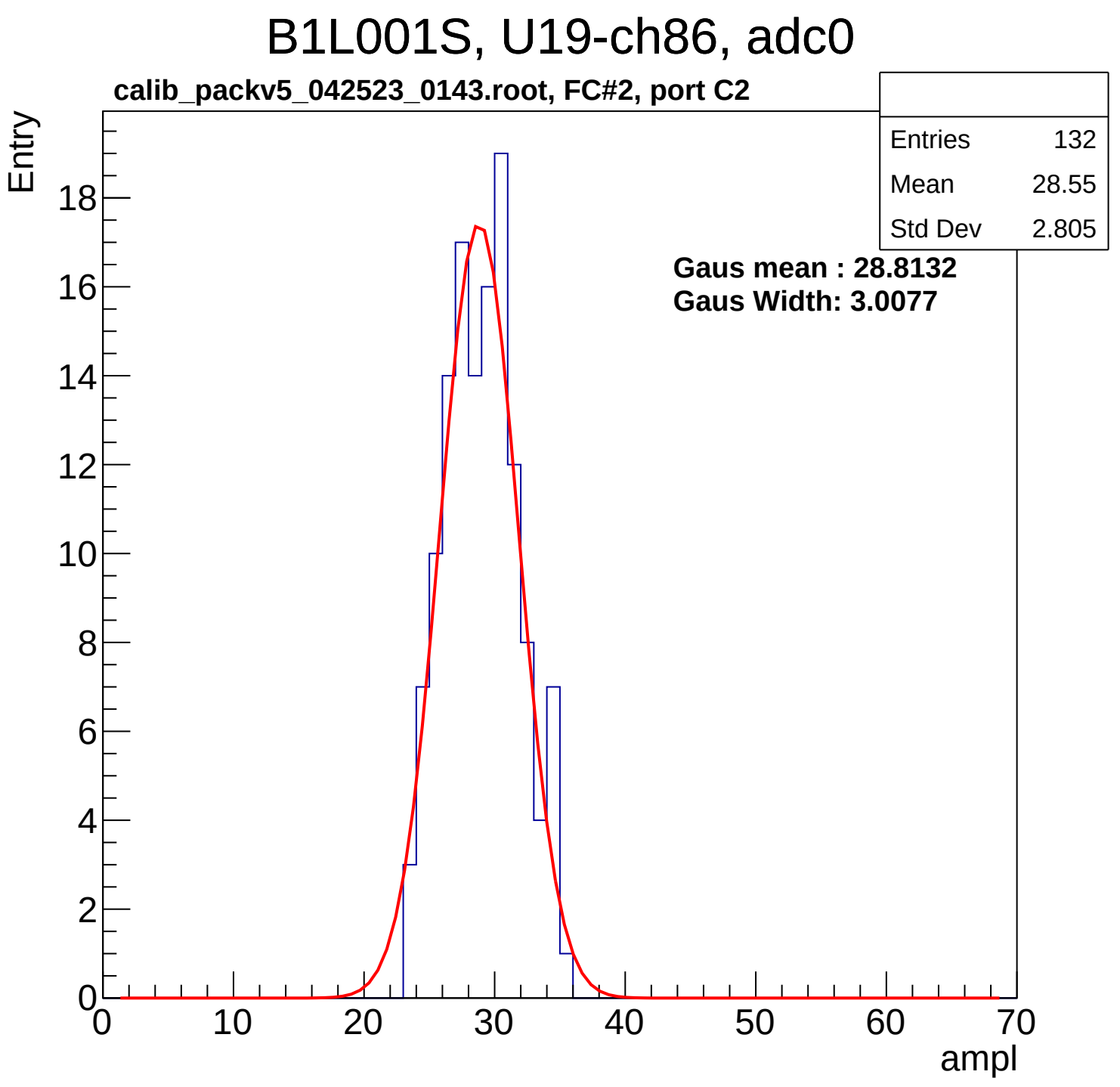
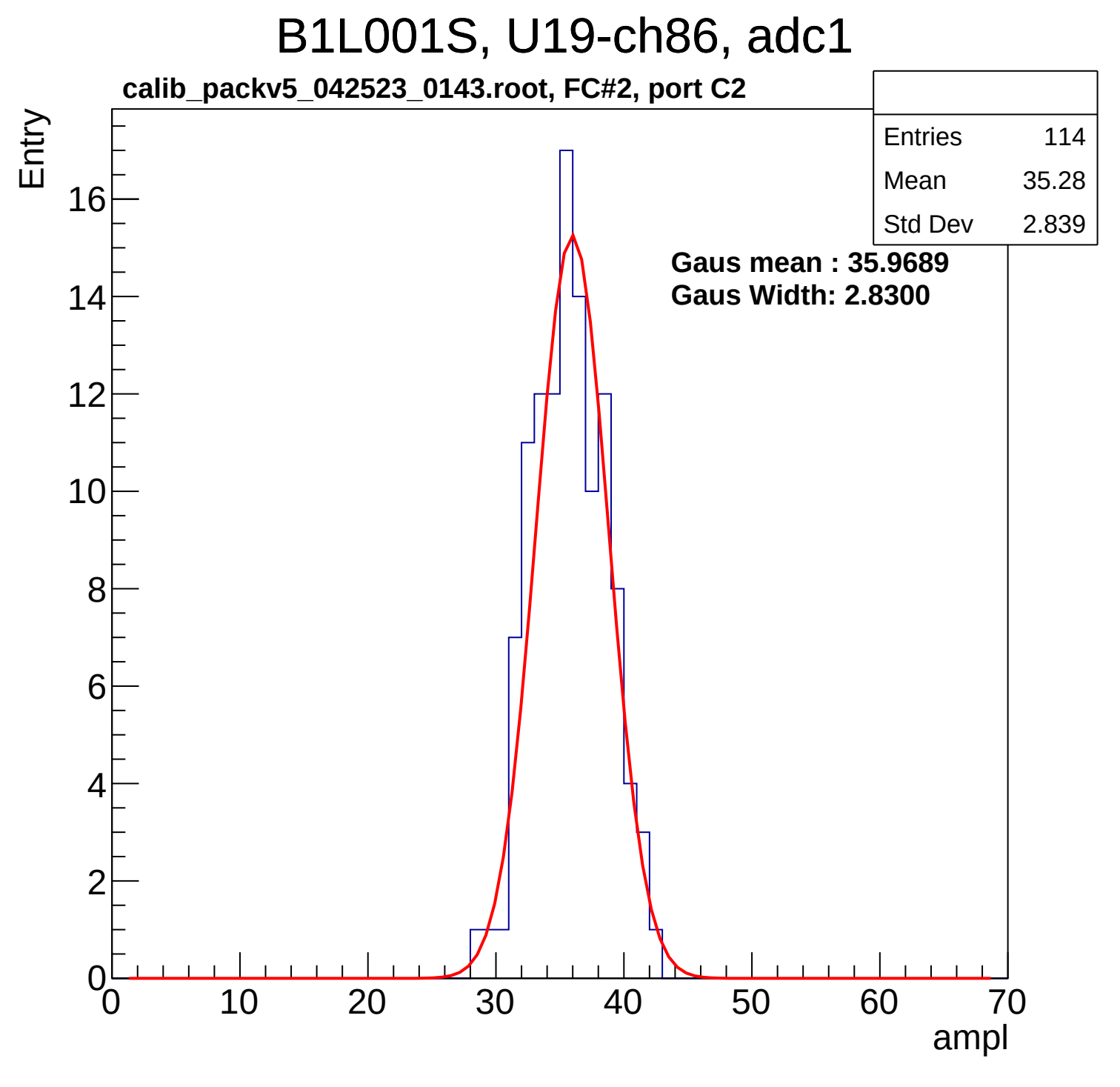
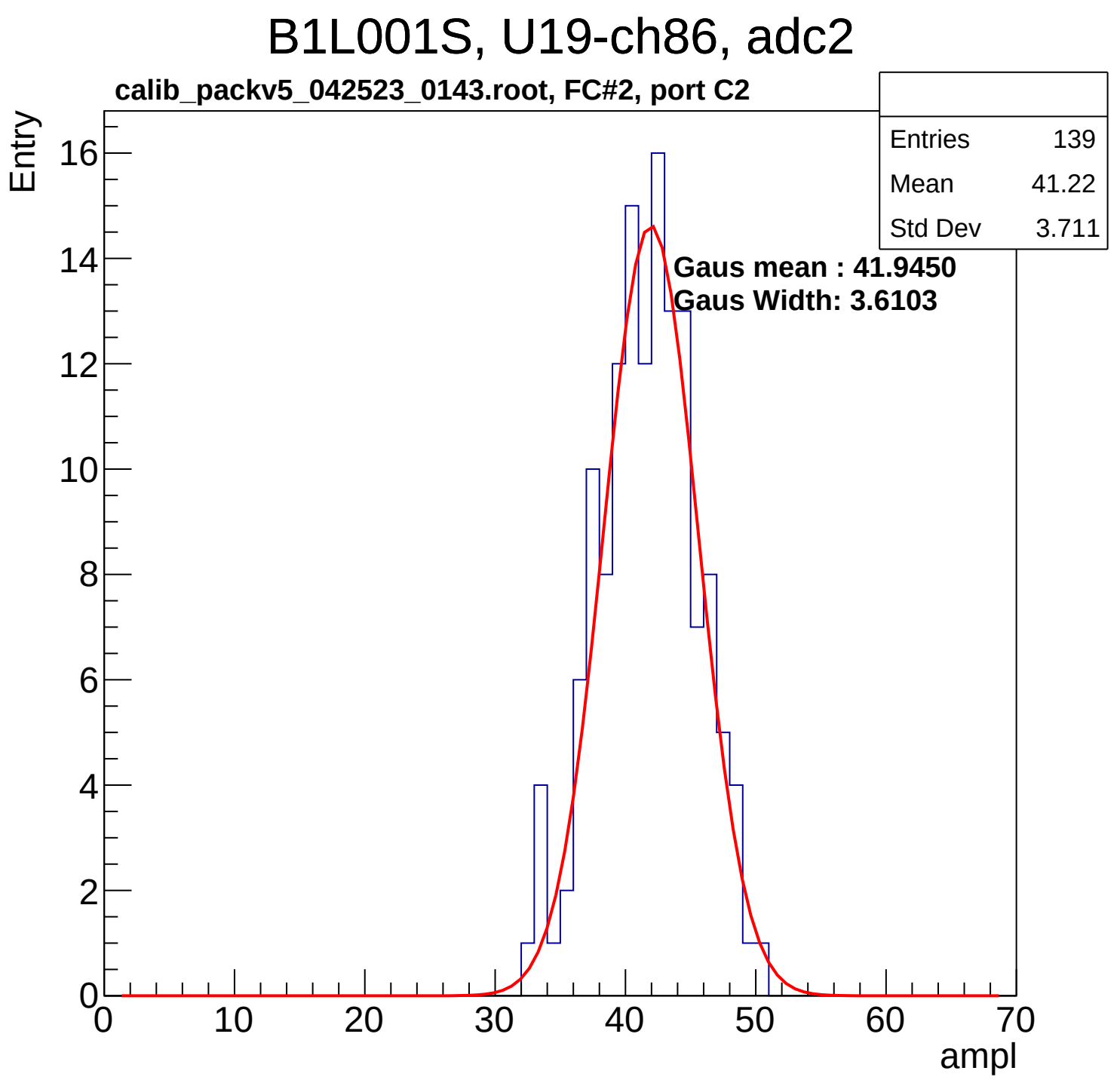
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70


B1L001S, U19-ch85, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 10
Mean 62
Std Dev 1
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L001S, U19-ch85, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 3
Mean 7.333
Std Dev 10.37
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L001S, U19-ch86, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 132
Mean 28.55
Std Dev 2.805
Gaus mean : 28.8132
Gaus Width: 3.0077
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70


B1L001S, U19-ch86, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 114
Mean 35.28
Std Dev 2.839
Gaus mean : 35.9689
Gaus Width: 2.8300
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70


B1L001S, U19-ch86, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 139
Mean 41.22
Std Dev 3.711
Gaus mean : 41.9450
Gaus Width: 3.6103
Entry
ampl
0
2
4
6
8
10
12
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16
0
10
20
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40
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60
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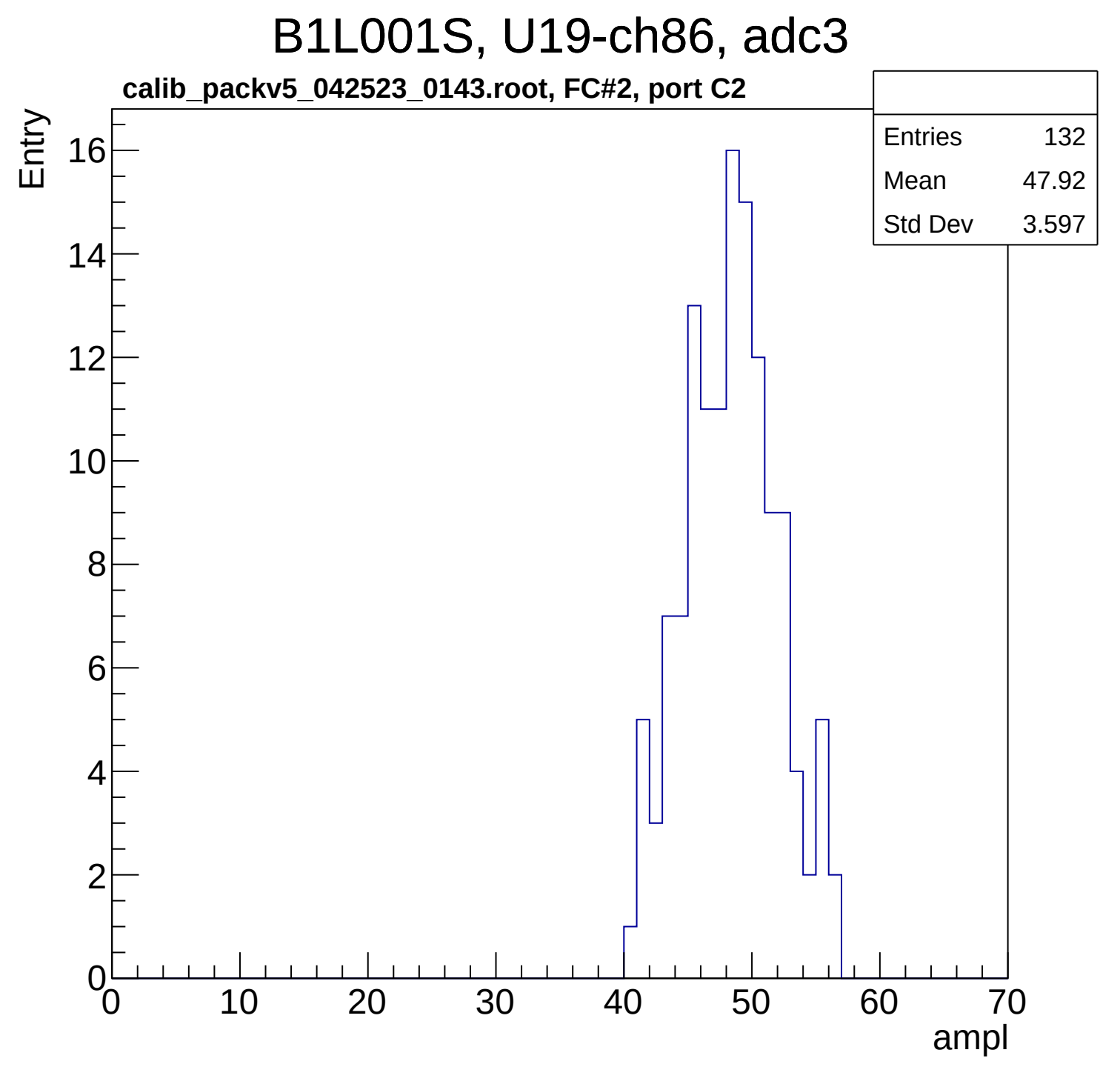
B1L001S, U19-ch86, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 132
Mean 47.92
Std Dev 3.597
Entry
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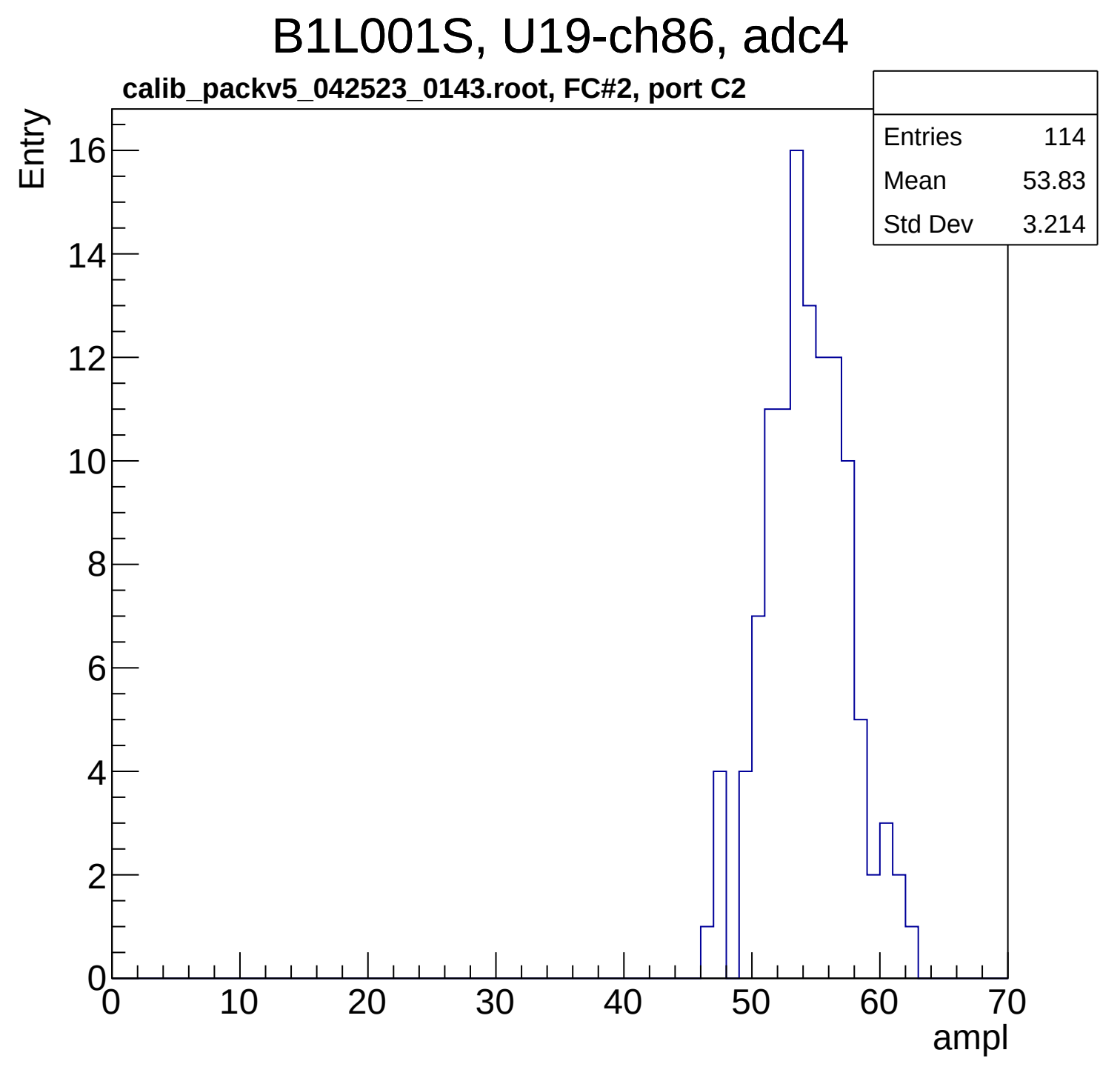
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch86, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 114
Mean 53.83
Std Dev 3.214
Entry
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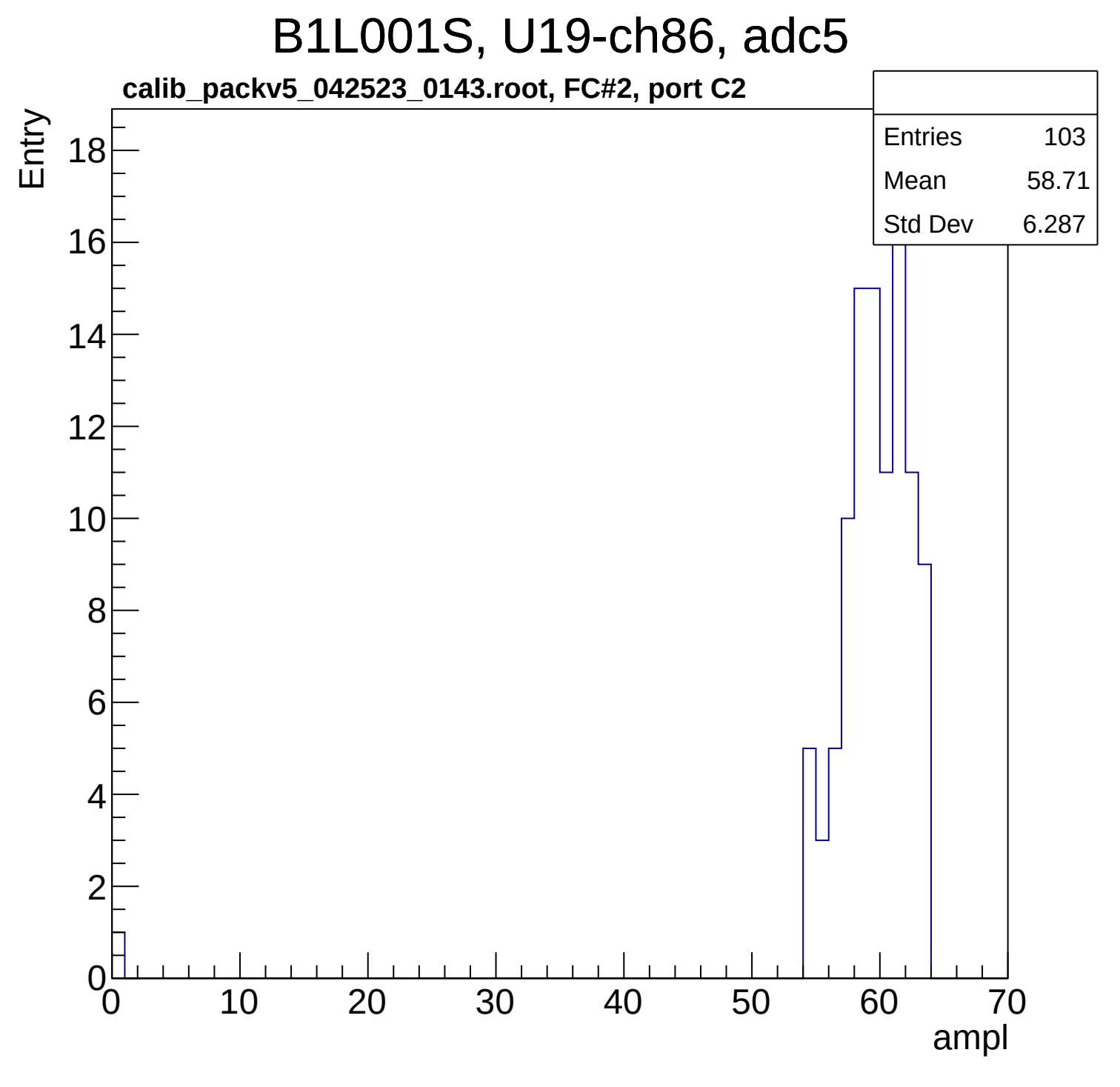
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch86, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 103
Mean 58.71
Std Dev 6.287
Entry
ampl
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6
8
10
12
14
16
18
0
10
20
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40
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60
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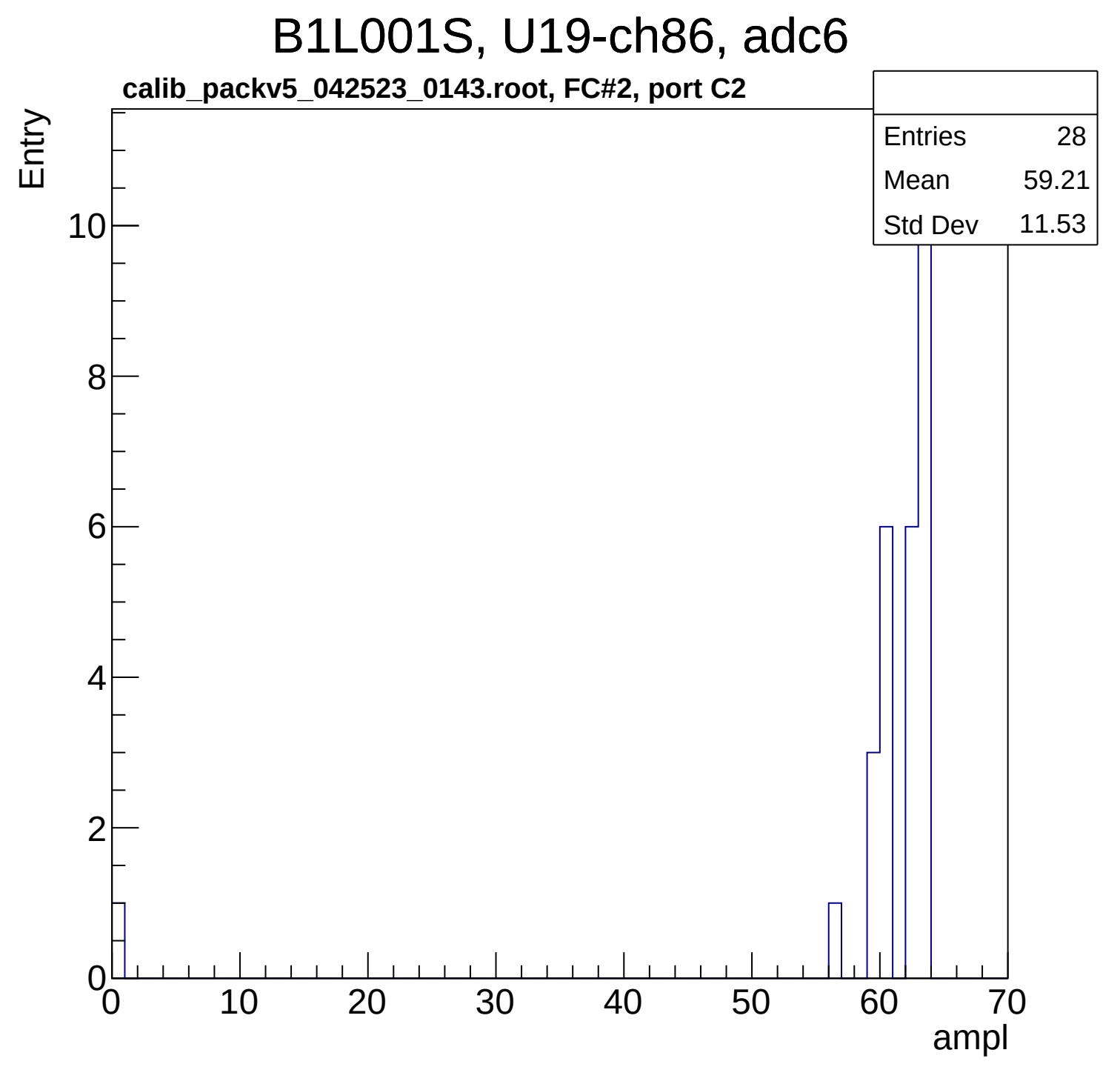
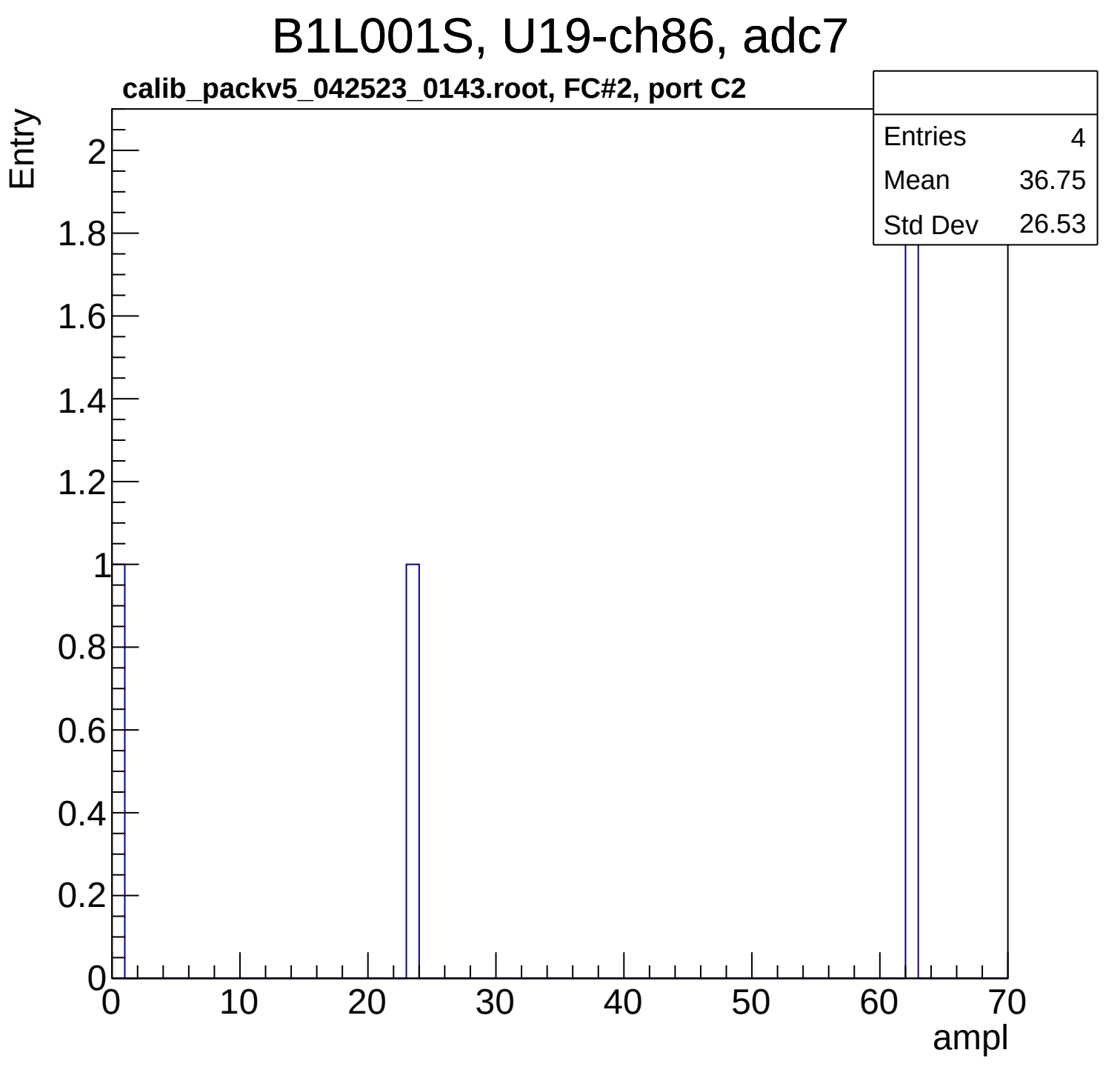
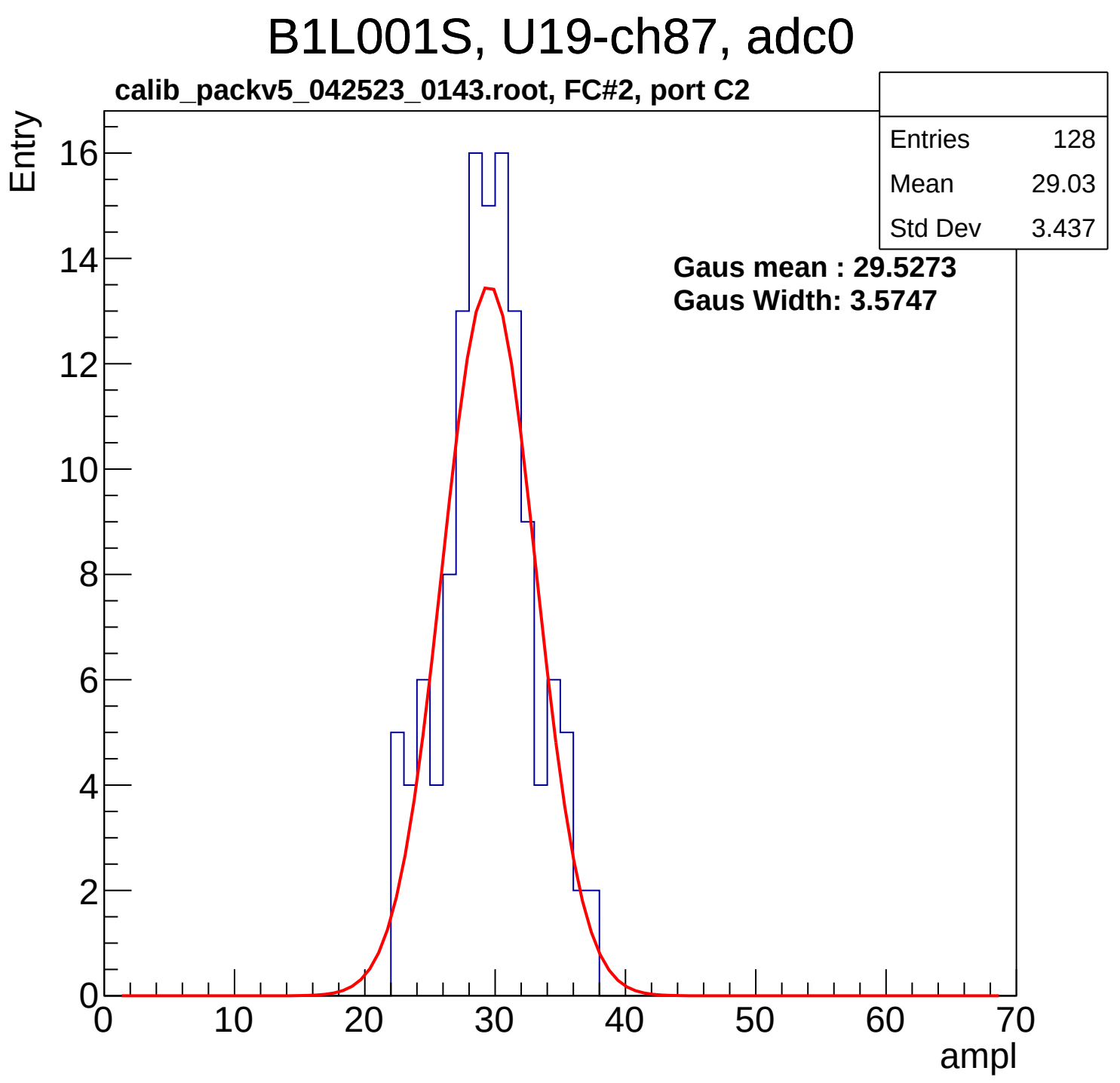

B1L001S, U19-ch86, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 28
Mean 59.21
Std Dev 11.53
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch86, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 4
Mean 36.75
Std Dev 26.53
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L001S, U19-ch87, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 128
Mean 29.03
Std Dev 3.437
Gaus mean : 29.5273
Gaus Width: 3.5747
Entry
ampl
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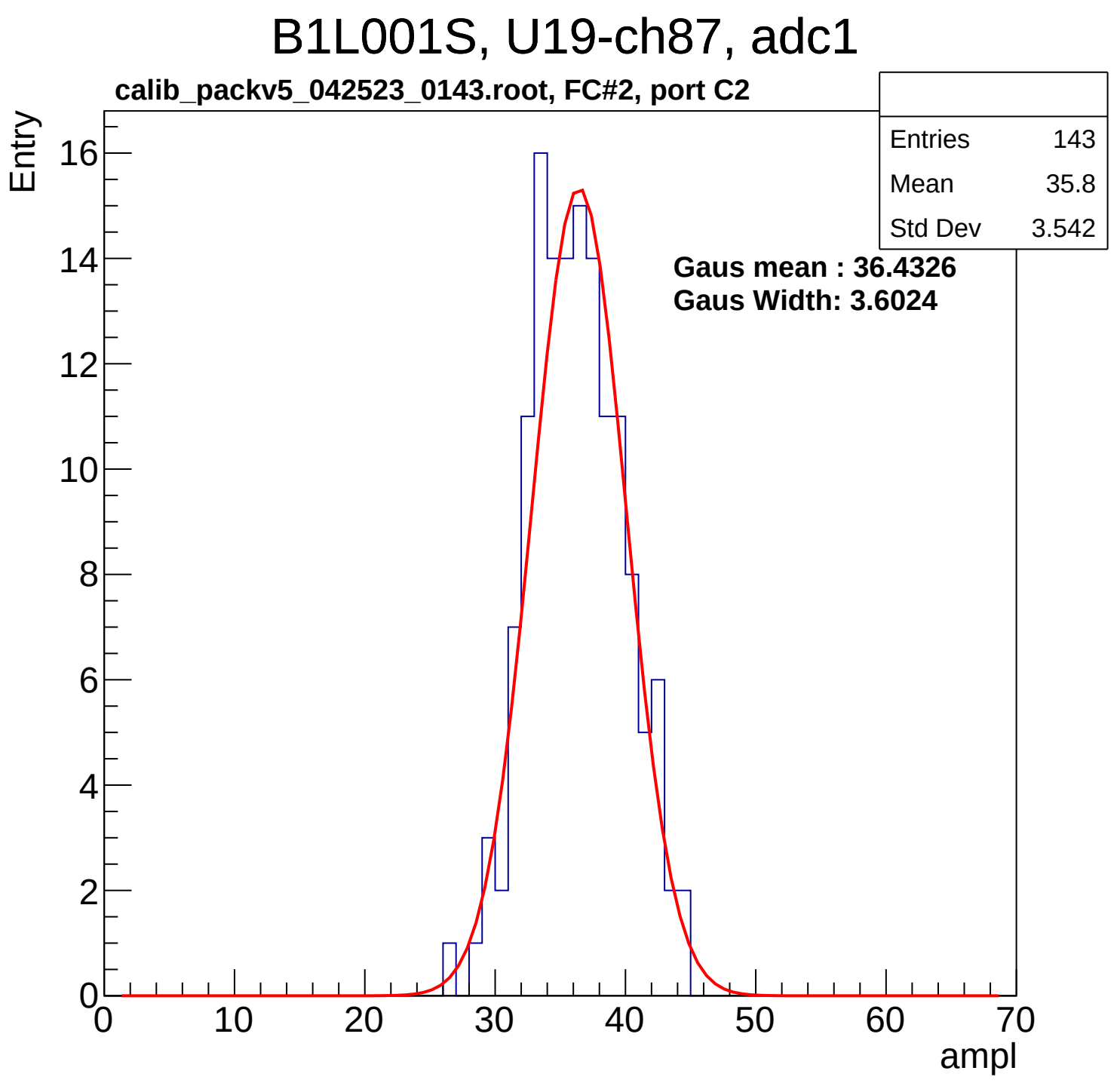
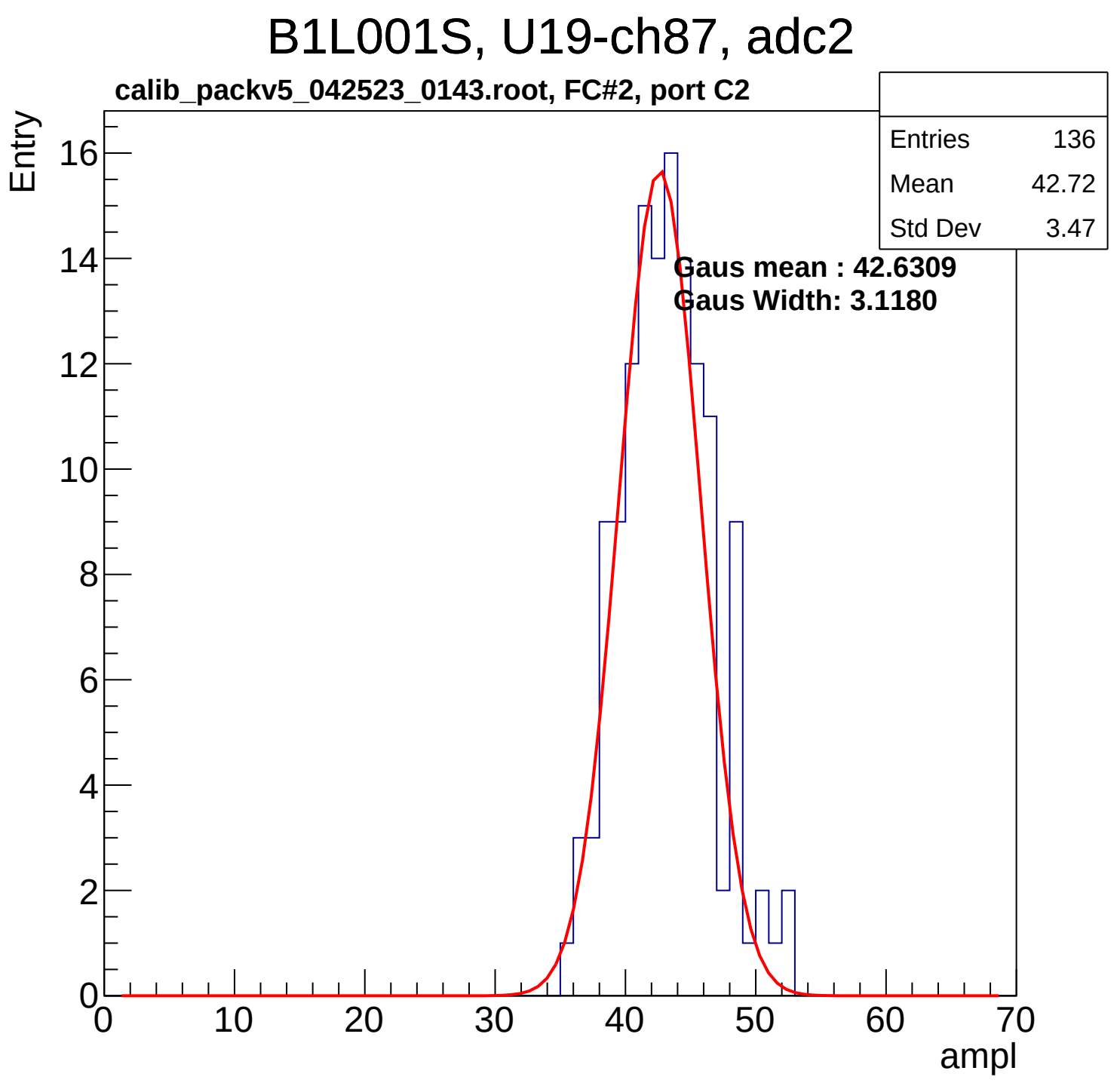
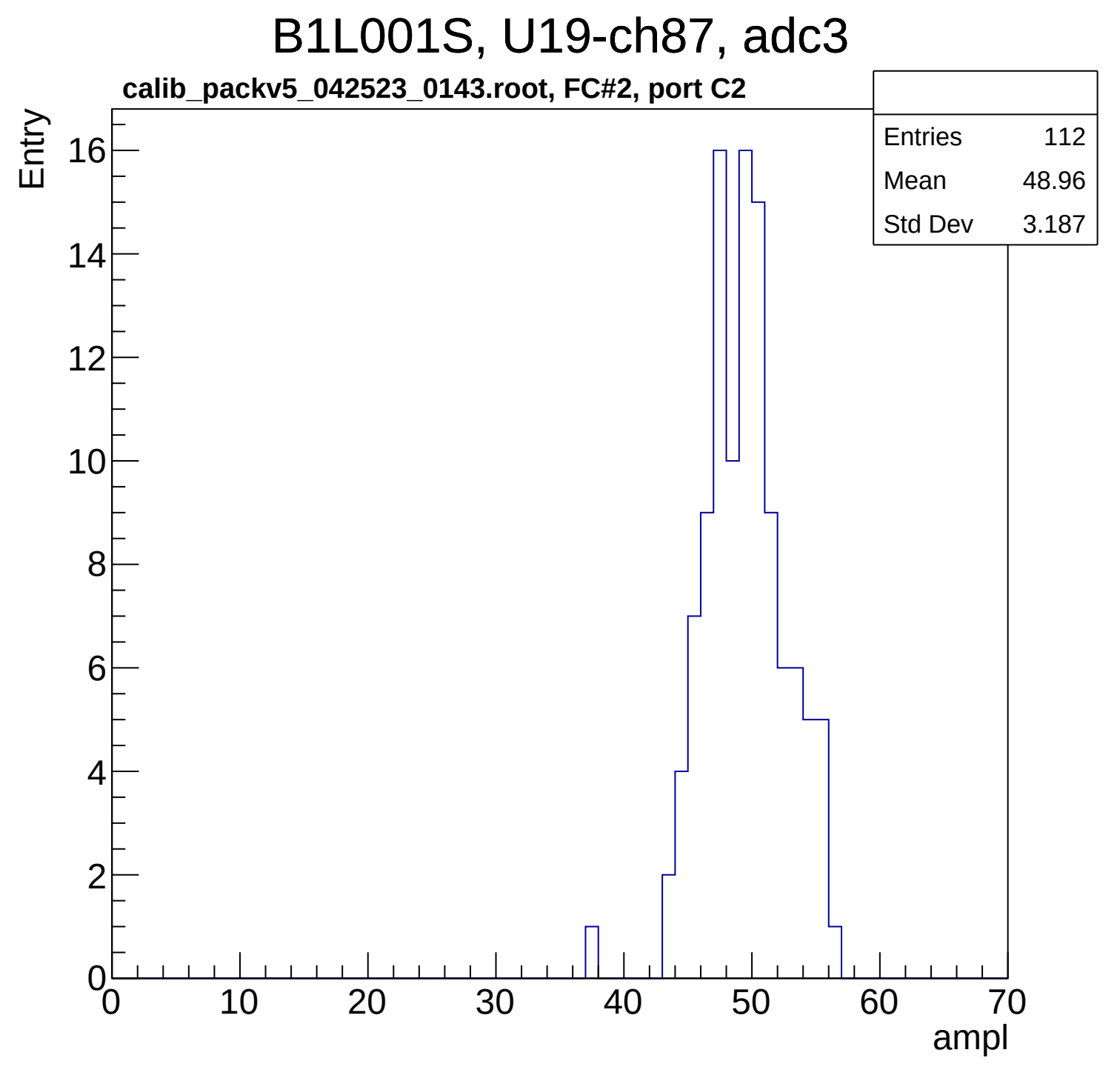
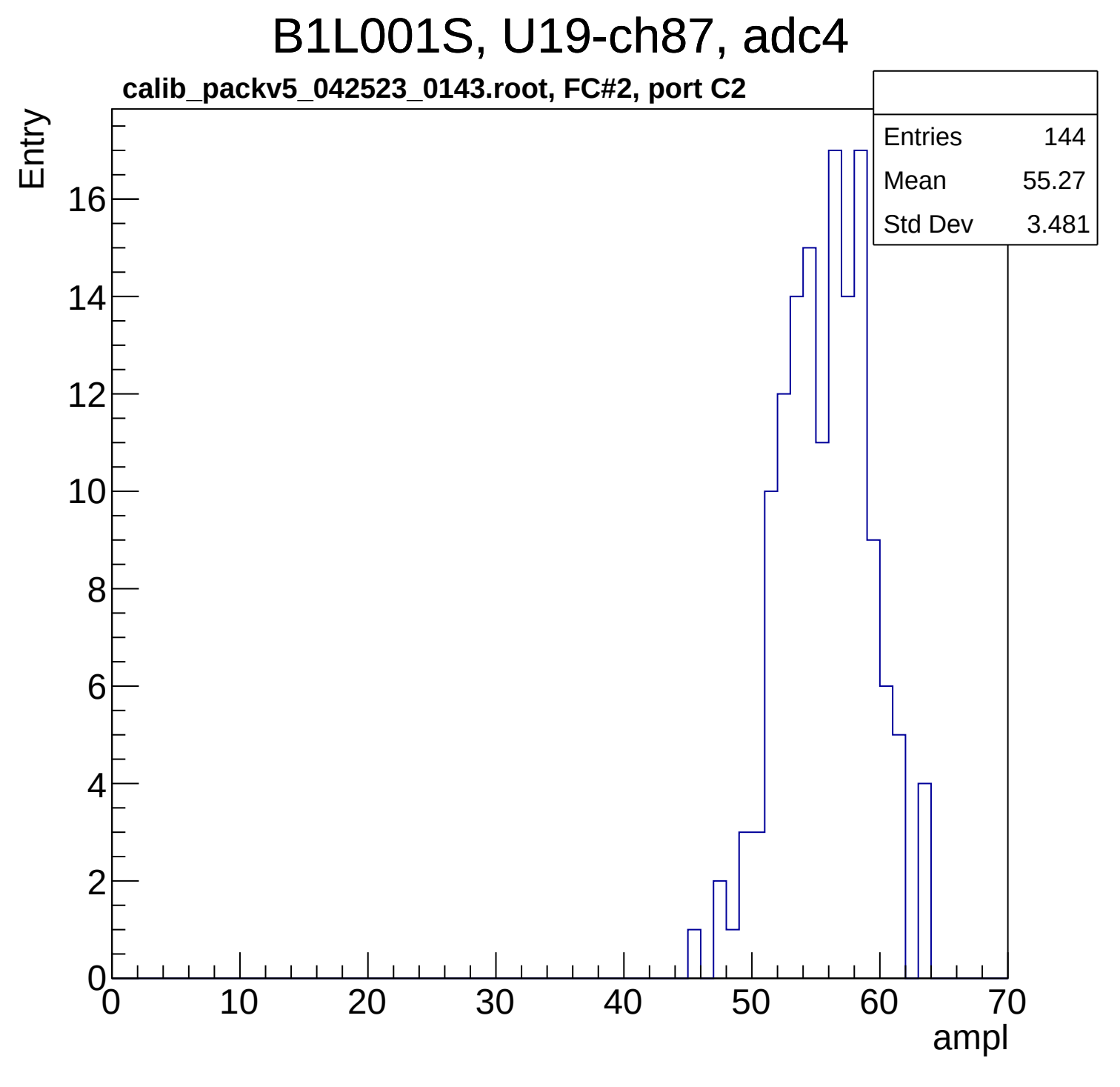
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70


B1L001S, U19-ch87, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 143
Mean 35.8
Std Dev 3.542
Gaus mean : 36.4326
Gaus Width: 3.6024
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70


B1L001S, U19-ch87, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 136
Mean 42.72
Std Dev 3.47
Gaus mean : 42.6309
Gaus Width: 3.1180
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70


B1L001S, U19-ch87, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 112
Mean 48.96
Std Dev 3.187
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70


B1L001S, U19-ch87, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 144
Mean 55.27
Std Dev 3.481
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
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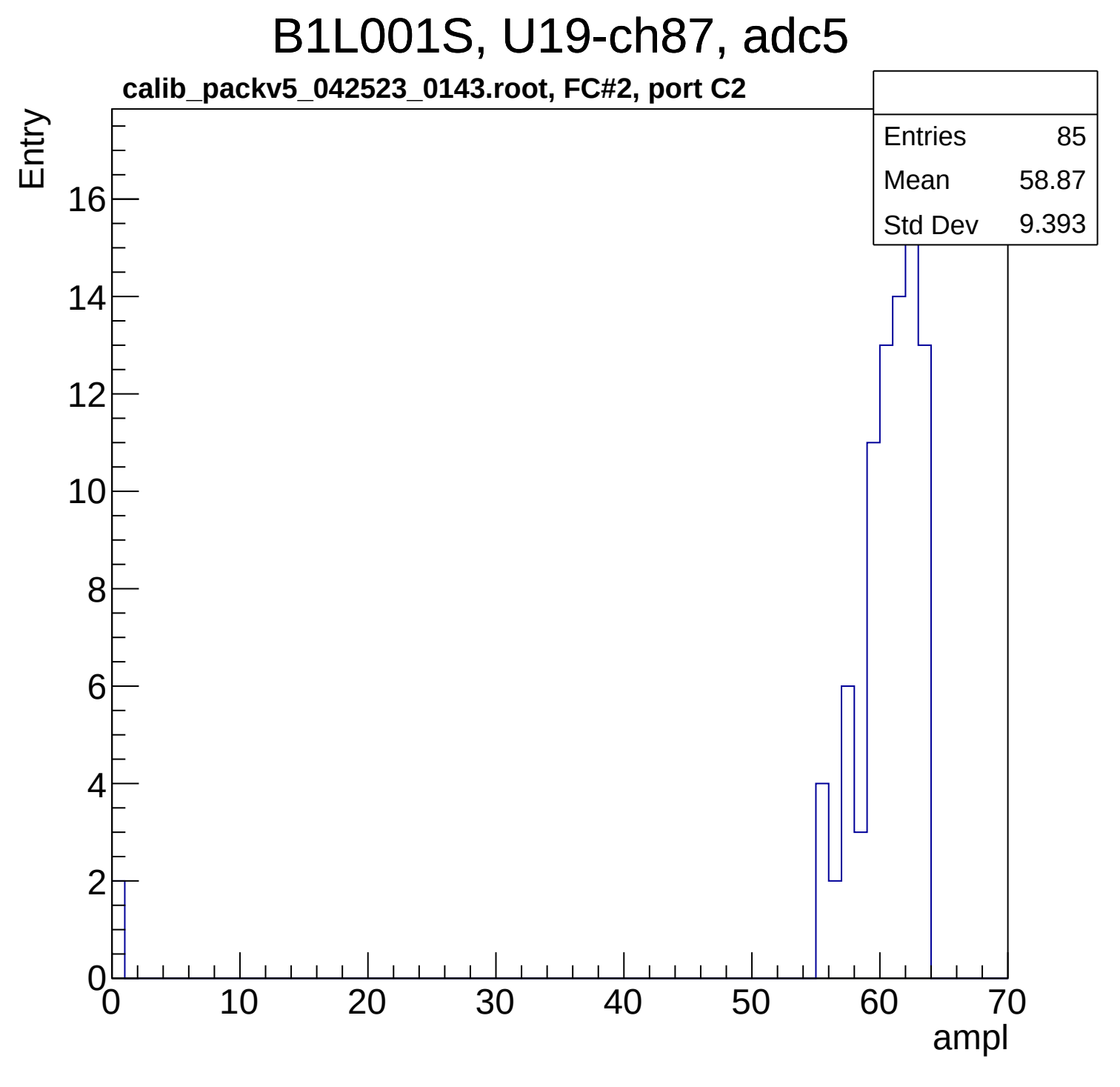
B1L001S, U19-ch87, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 85
Mean 58.87
Std Dev 9.393
Entry
ampl
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2
4
6
8
10
12
14
16
0
10
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40
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60
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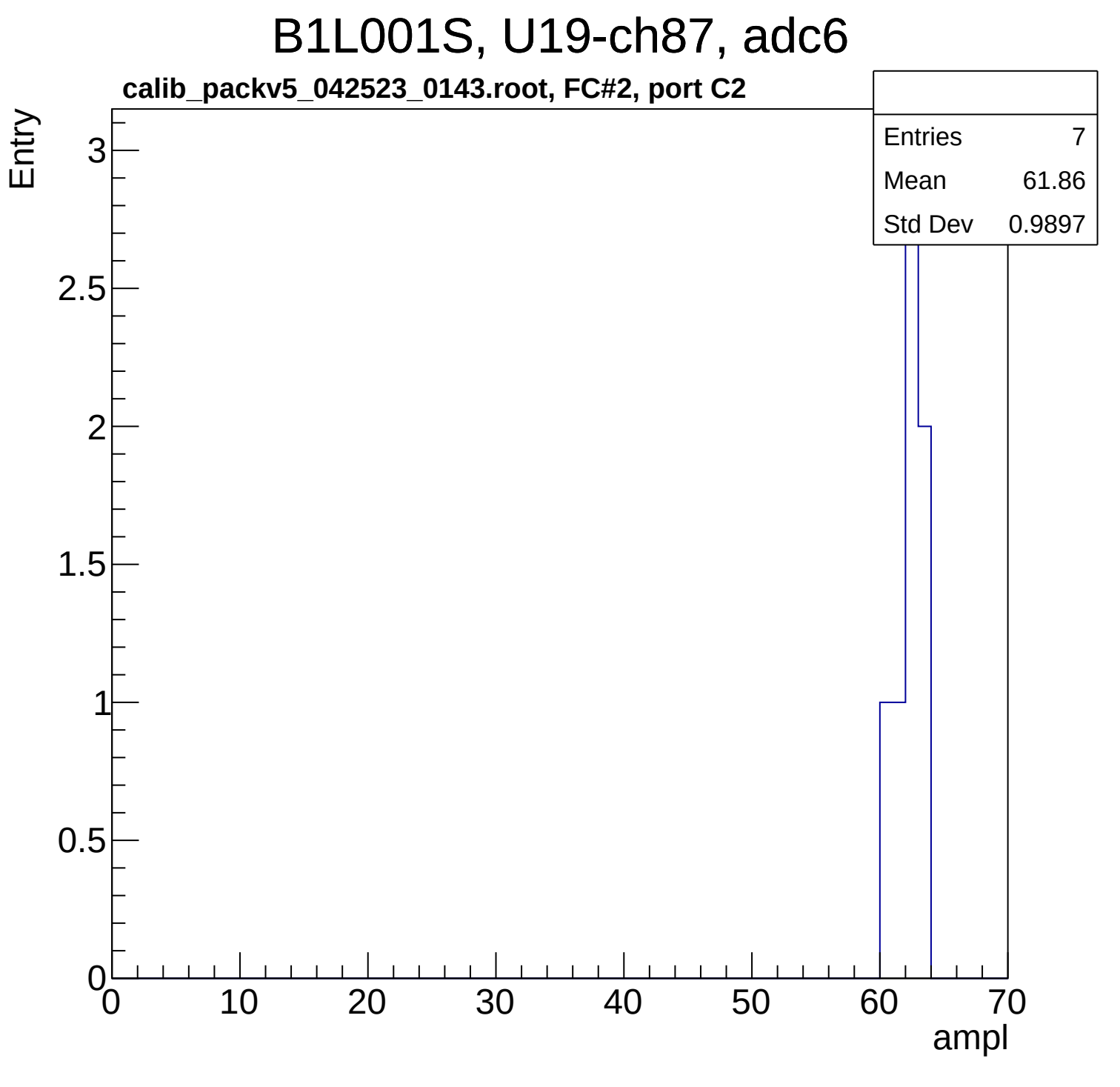
B1L001S, U19-ch87, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 7
Mean 61.86
Std Dev 0.9897
Entry
ampl
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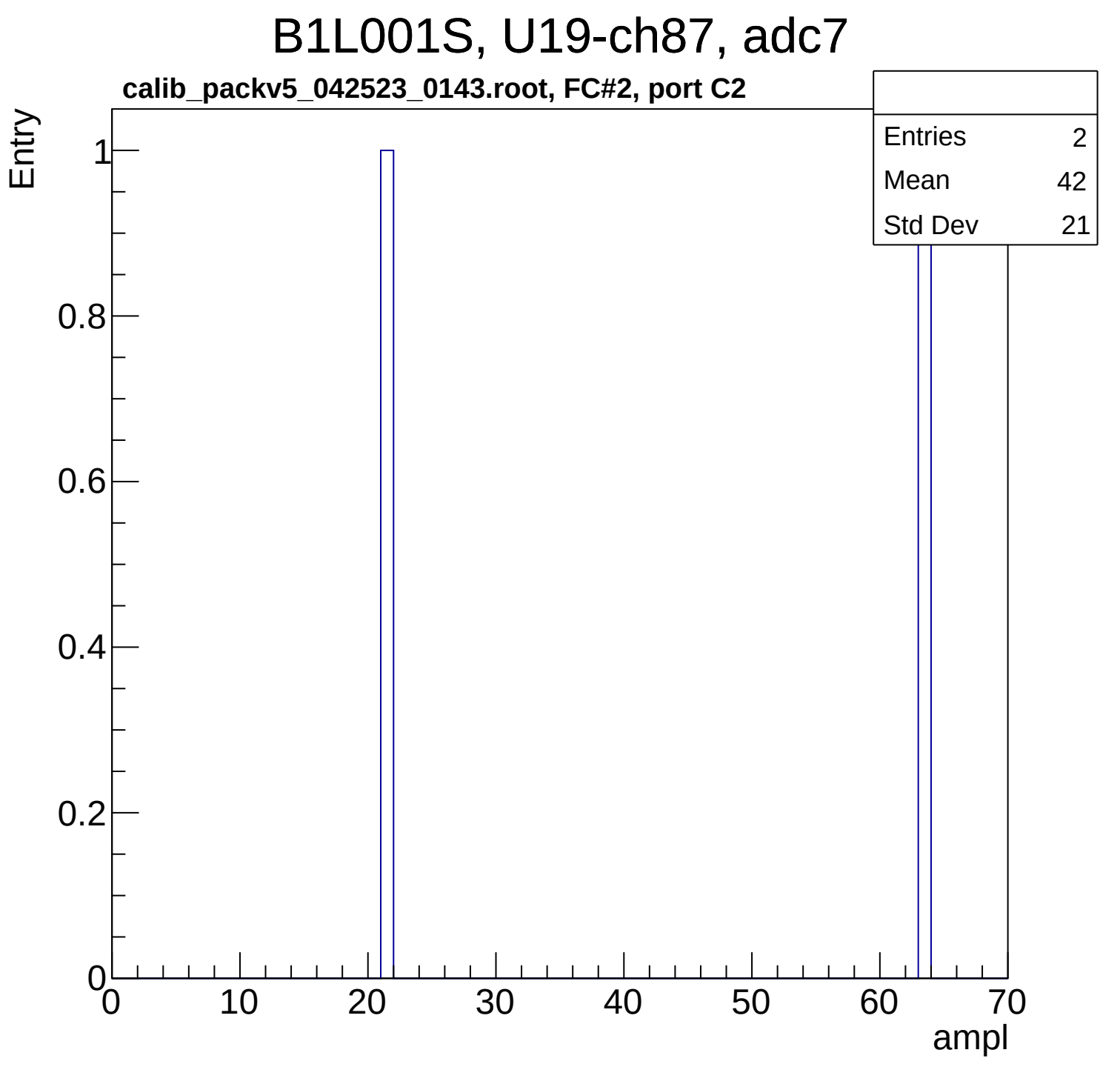
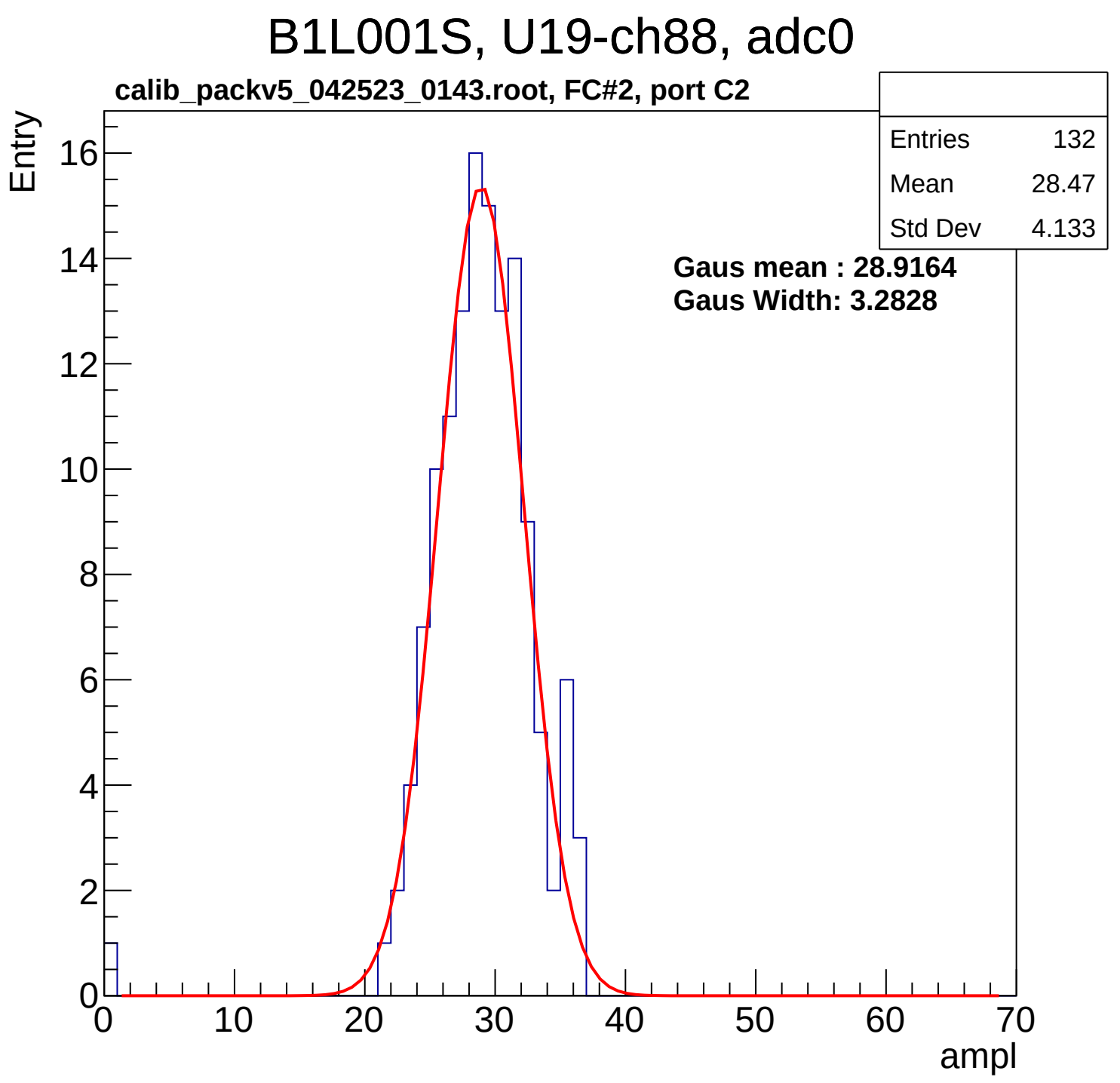
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L001S, U19-ch87, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 42
Std Dev 21
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70


B1L001S, U19-ch88, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 132
Mean 28.47
Std Dev 4.133
Gaus mean : 28.9164
Gaus Width: 3.2828
Entry
ampl
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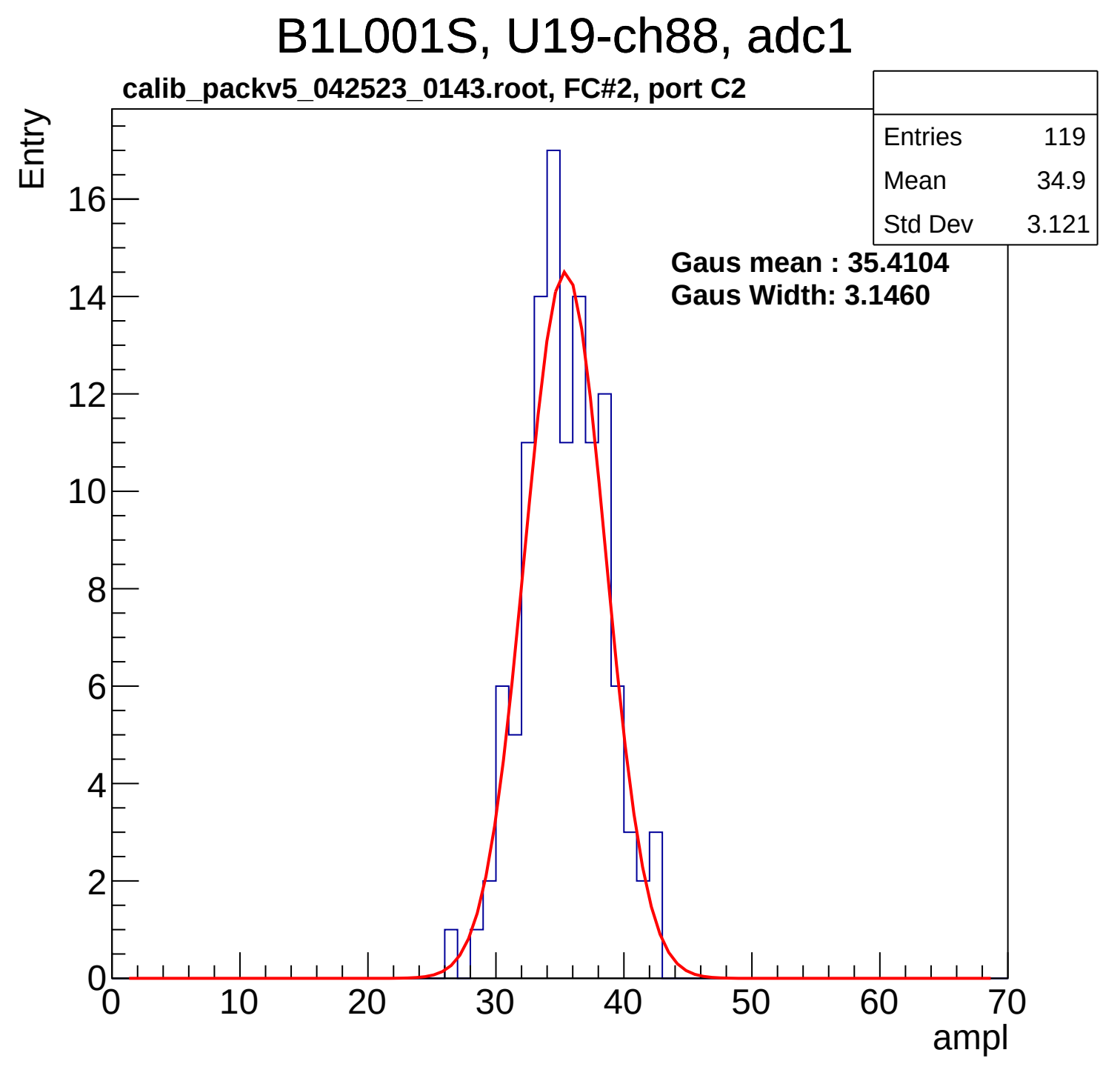
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70


B1L001S, U19-ch88, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 119
Mean 34.9
Std Dev 3.121
Gaus mean : 35.4104
Gaus Width: 3.1460
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
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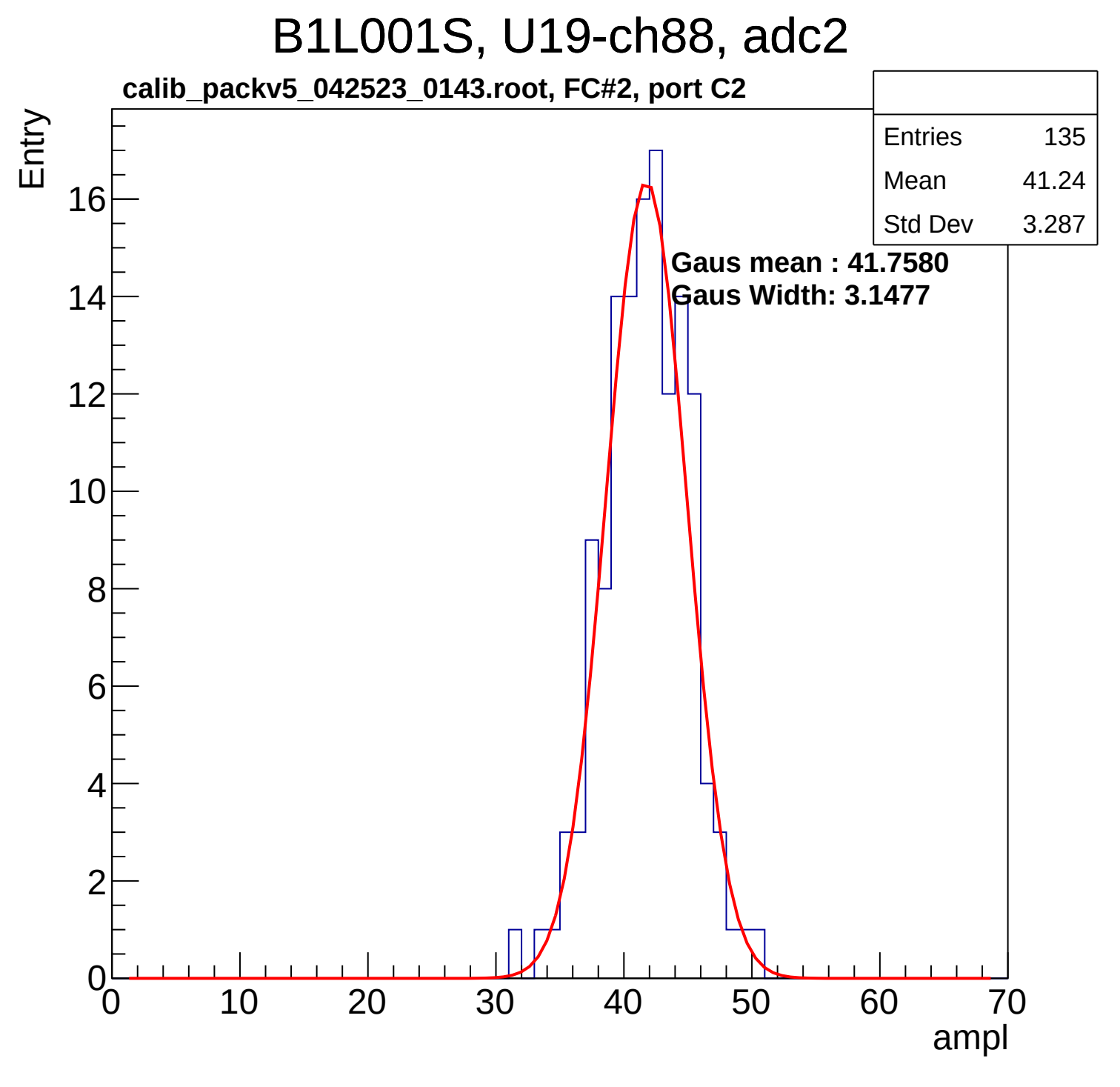
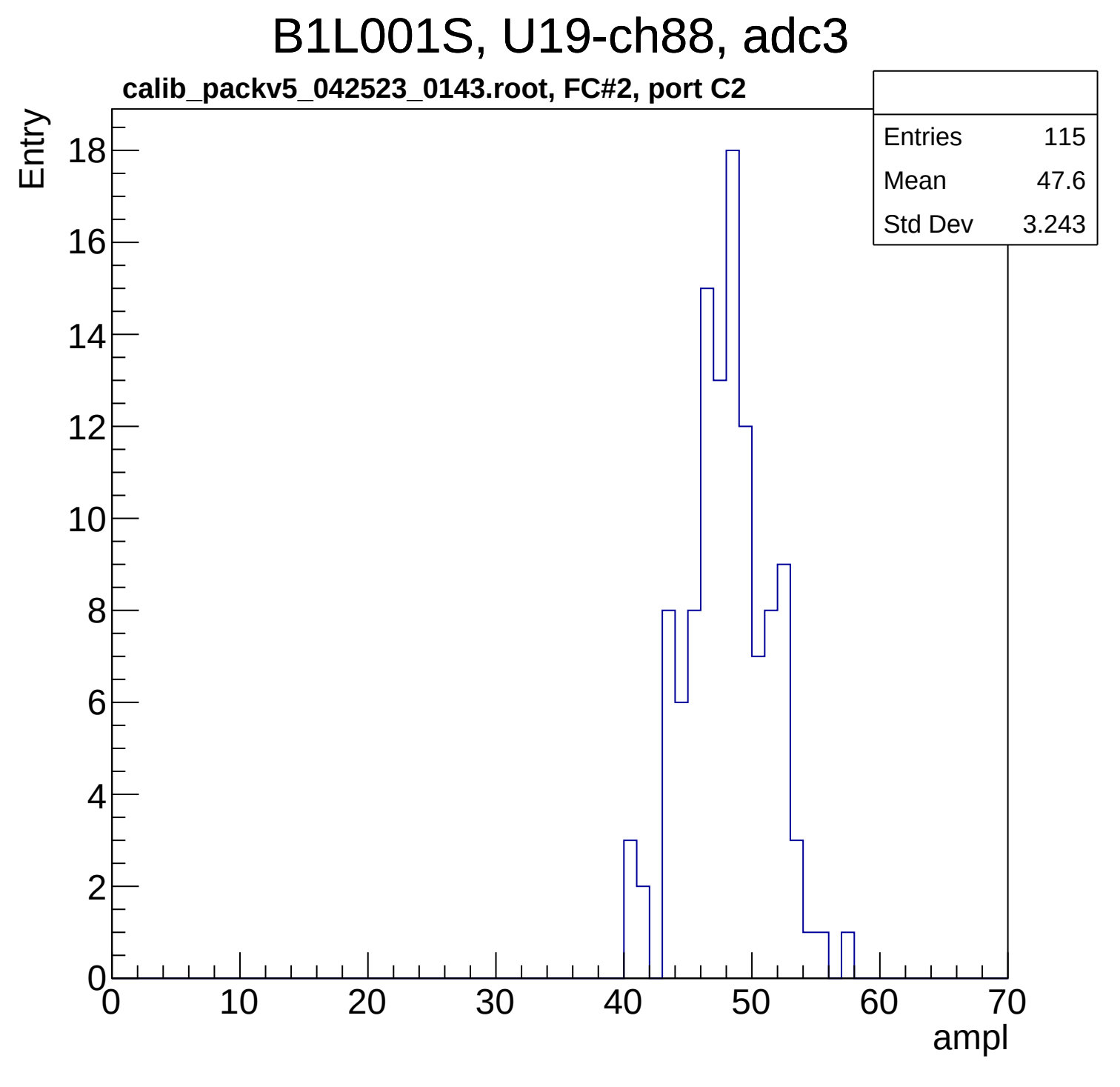
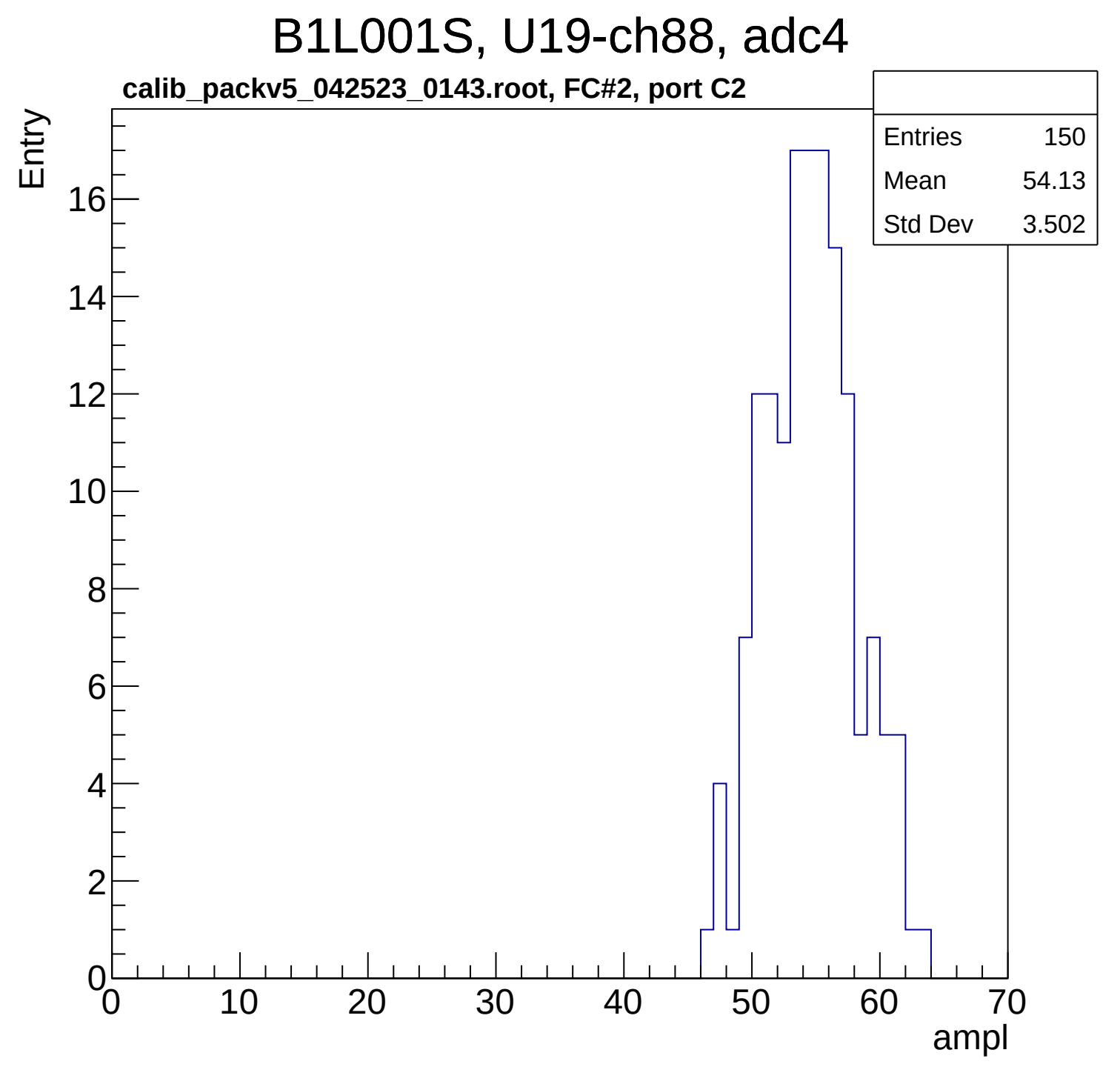

B1L001S, U19-ch88, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 135
Mean 41.24
Std Dev 3.287
Gaus mean : 41.7580
Gaus Width: 3.1477
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70


B1L001S, U19-ch88, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 115
Mean 47.6
Std Dev 3.243
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch88, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 150
Mean 54.13
Std Dev 3.502
Entry
ampl
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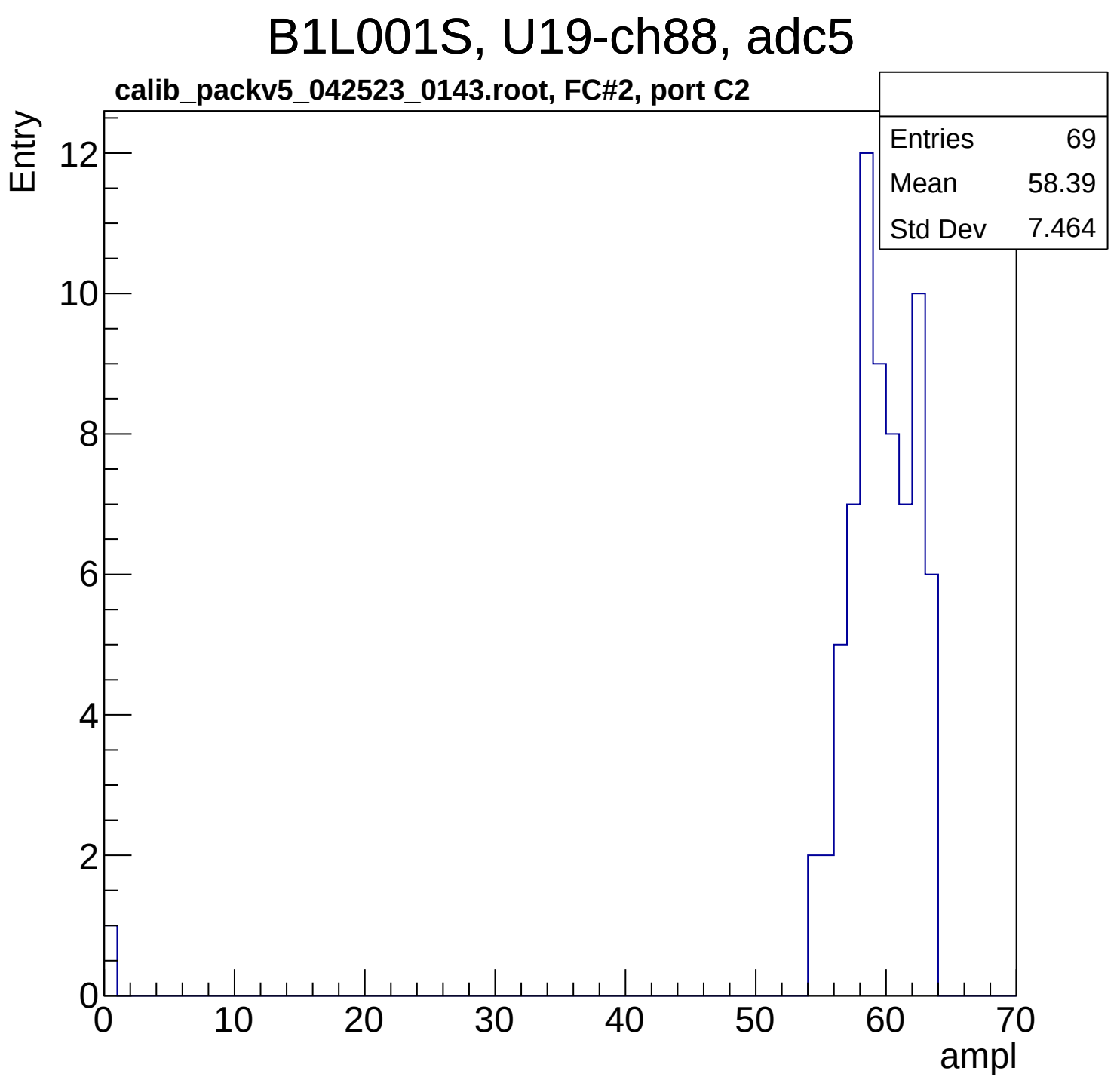
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70


B1L001S, U19-ch88, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 69
Mean 58.39
Std Dev 7.464
Entry
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30
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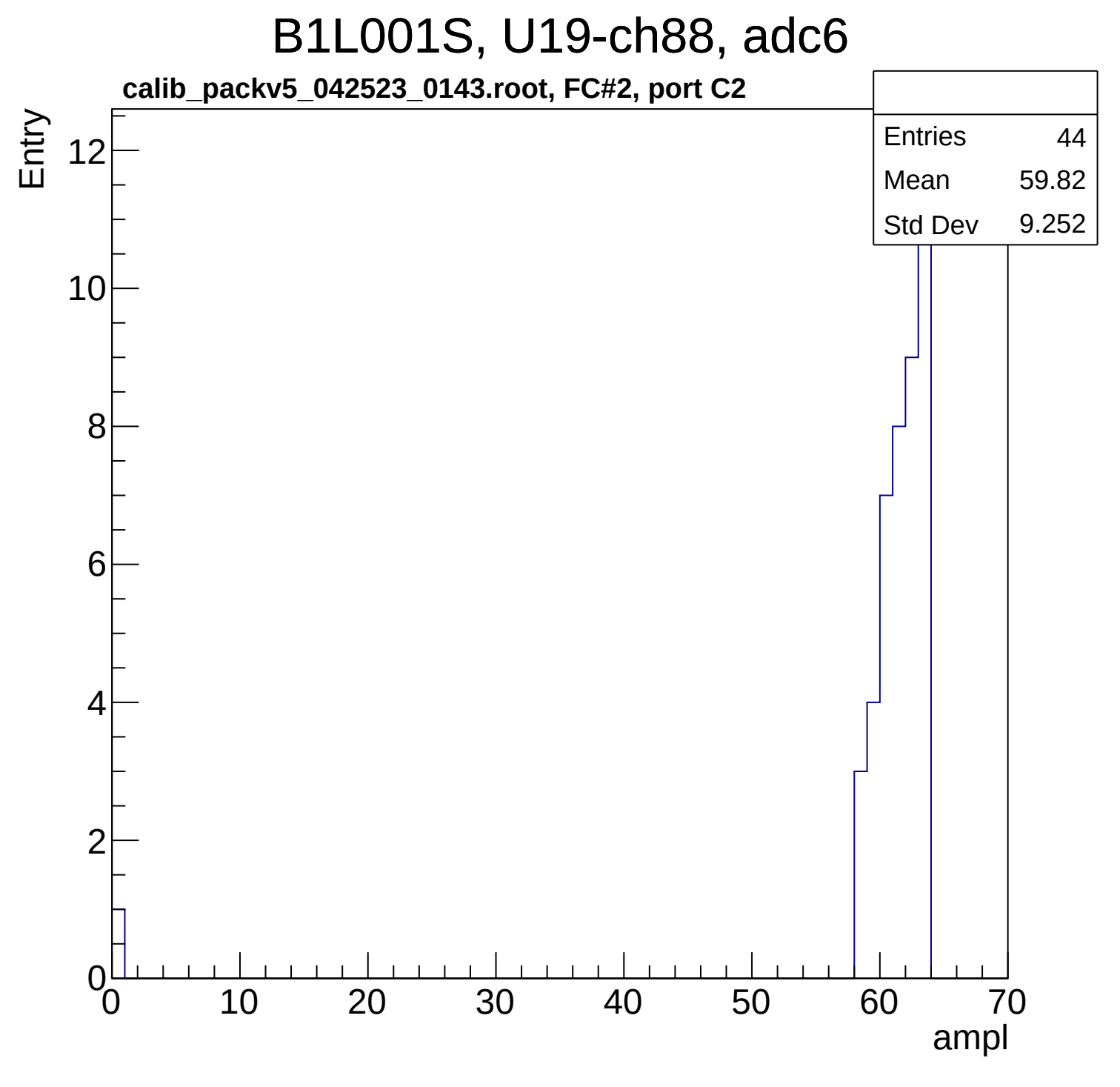
50
60
70
ampl


B1L001S, U19-ch88, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 44
Mean 59.82
Std Dev 9.252
Entry
ampl
0
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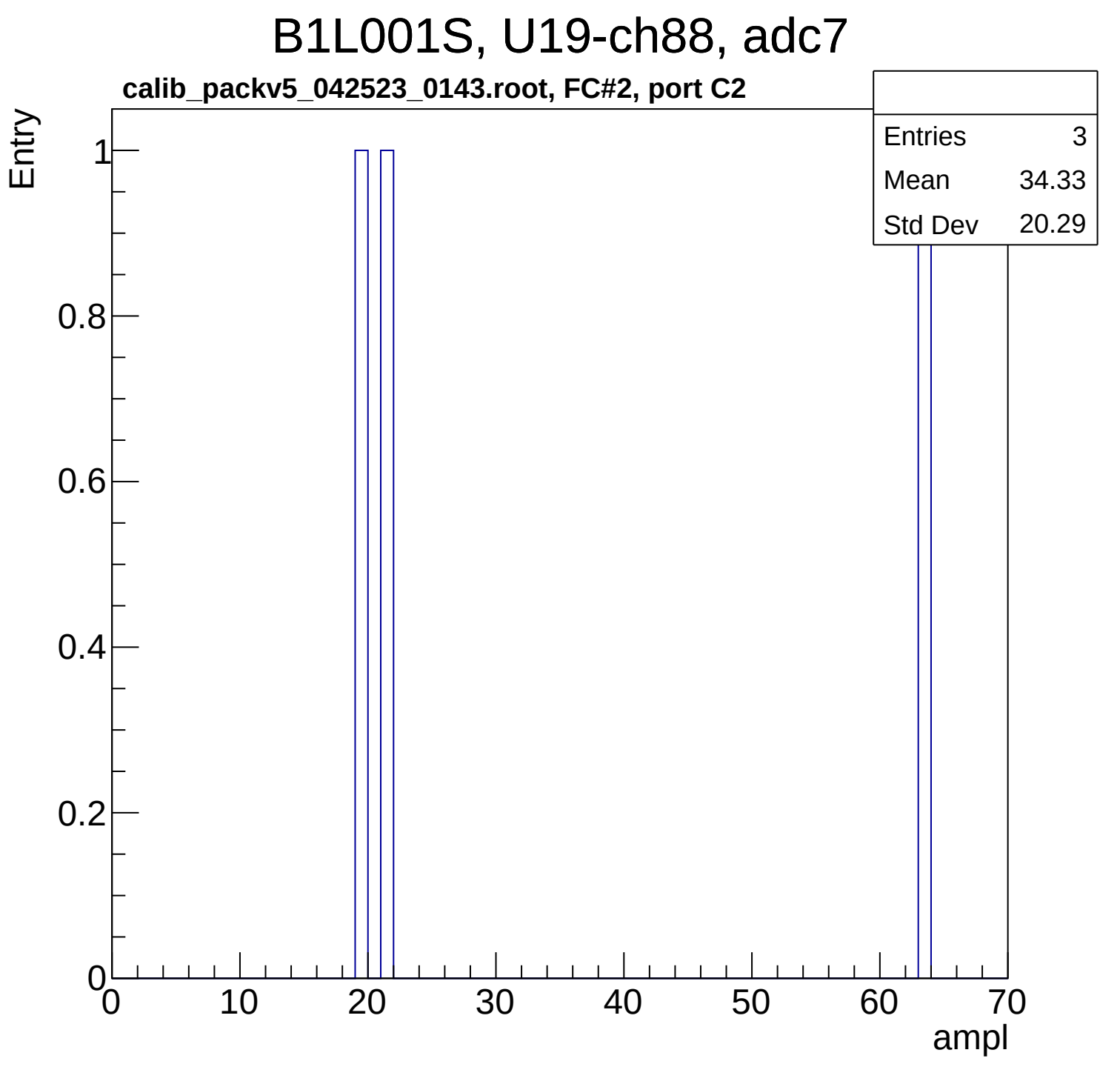
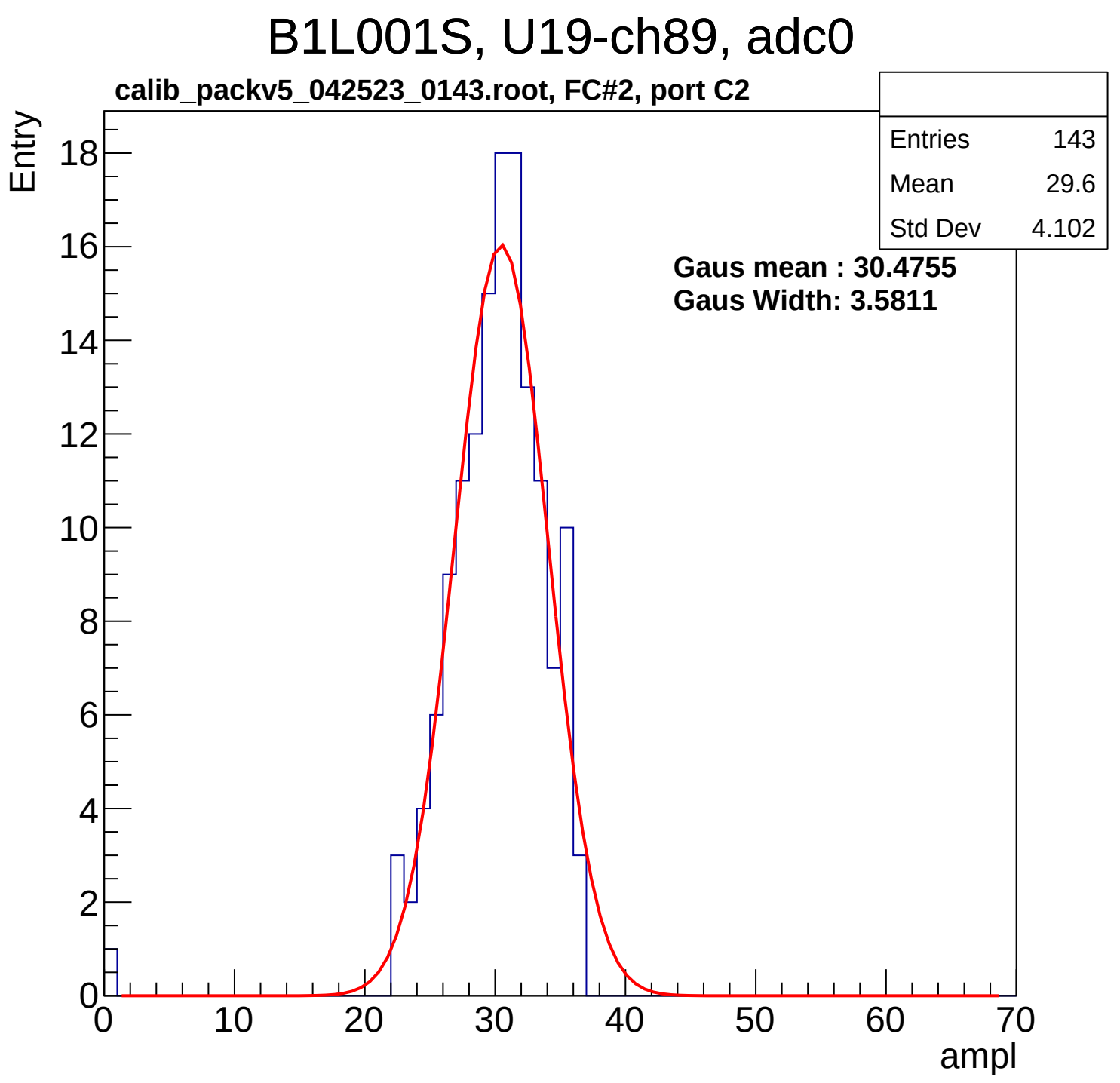
4
6
8
10
12
0
10
20
30
40
50
60
70


B1L001S, U19-ch88, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 3
Mean 34.33
Std Dev 20.29
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70


B1L001S, U19-ch89, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 143
Mean 29.6
Std Dev 4.102
Gaus mean : 30.4755
Gaus Width: 3.5811
Entry
ampl
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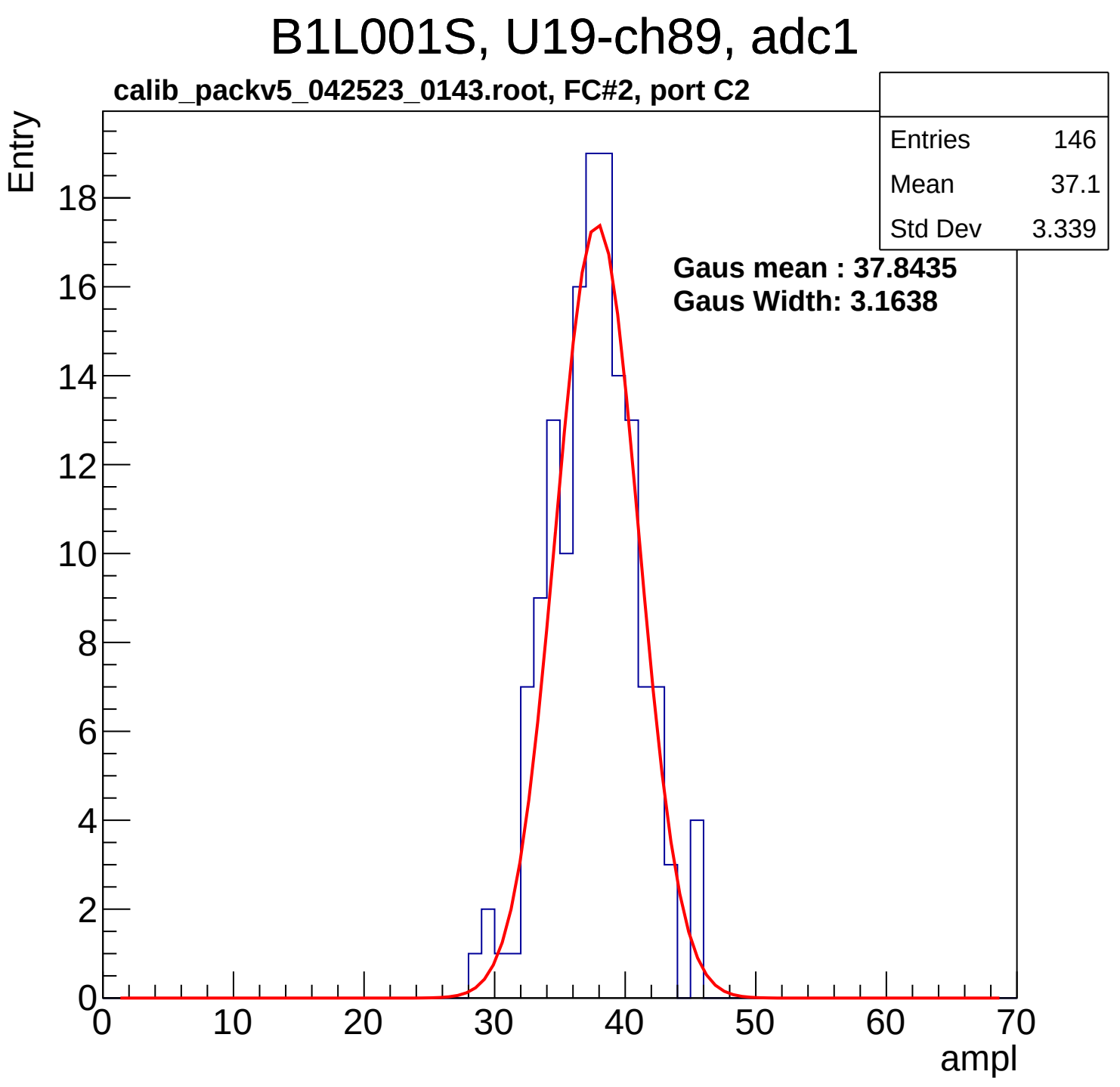
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70


B1L001S, U19-ch89, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 146
Mean 37.1
Std Dev 3.339
Gaus mean : 37.8435
Gaus Width: 3.1638
Entry
ampl
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4
6
8
10
12
14
16
18
0
10
20
30
40
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60
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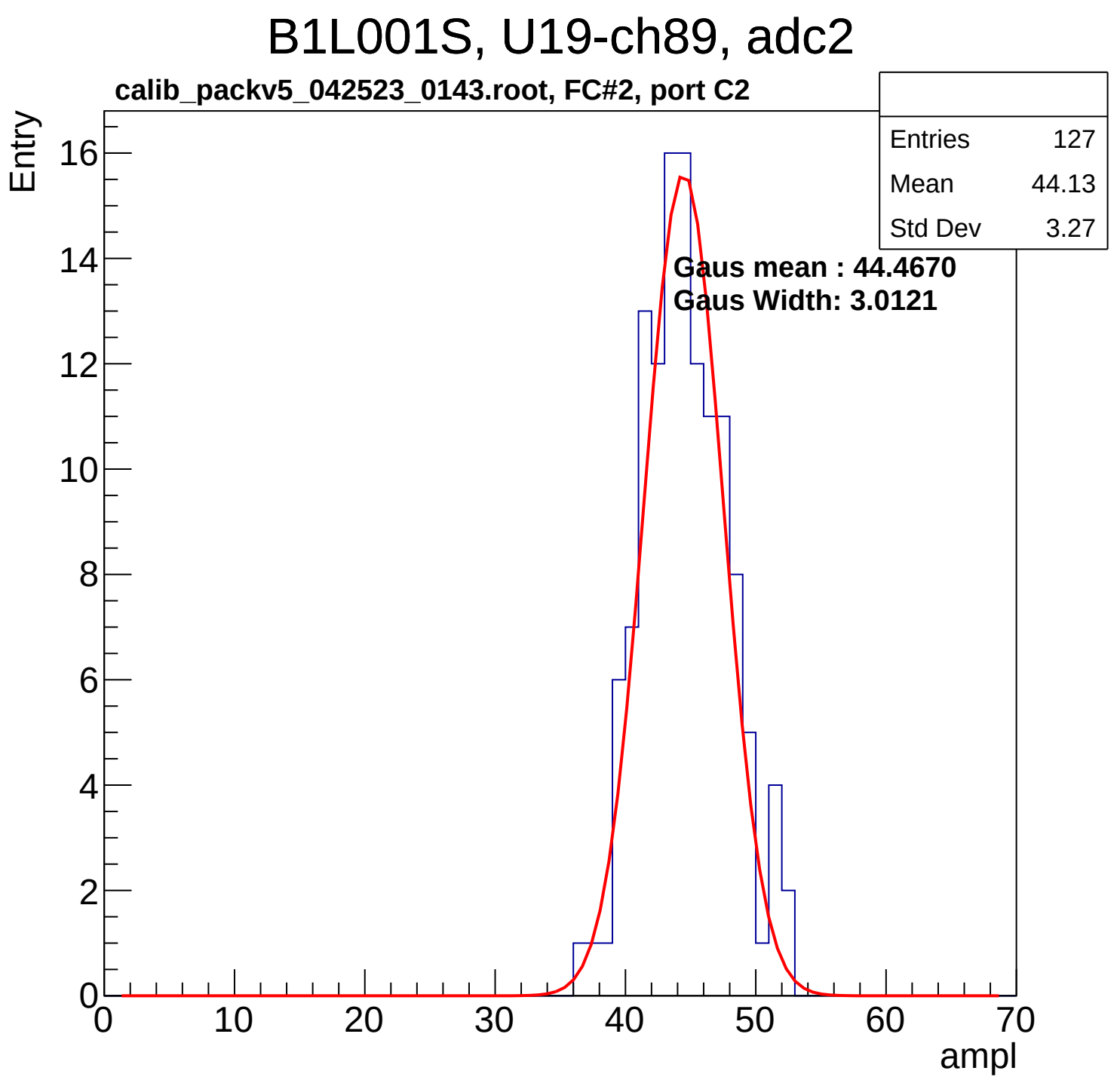
B1L001S, U19-ch89, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 127
Mean 44.13
Std Dev 3.27
Gaus mean : 44.4670
Gaus Width: 3.0121
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
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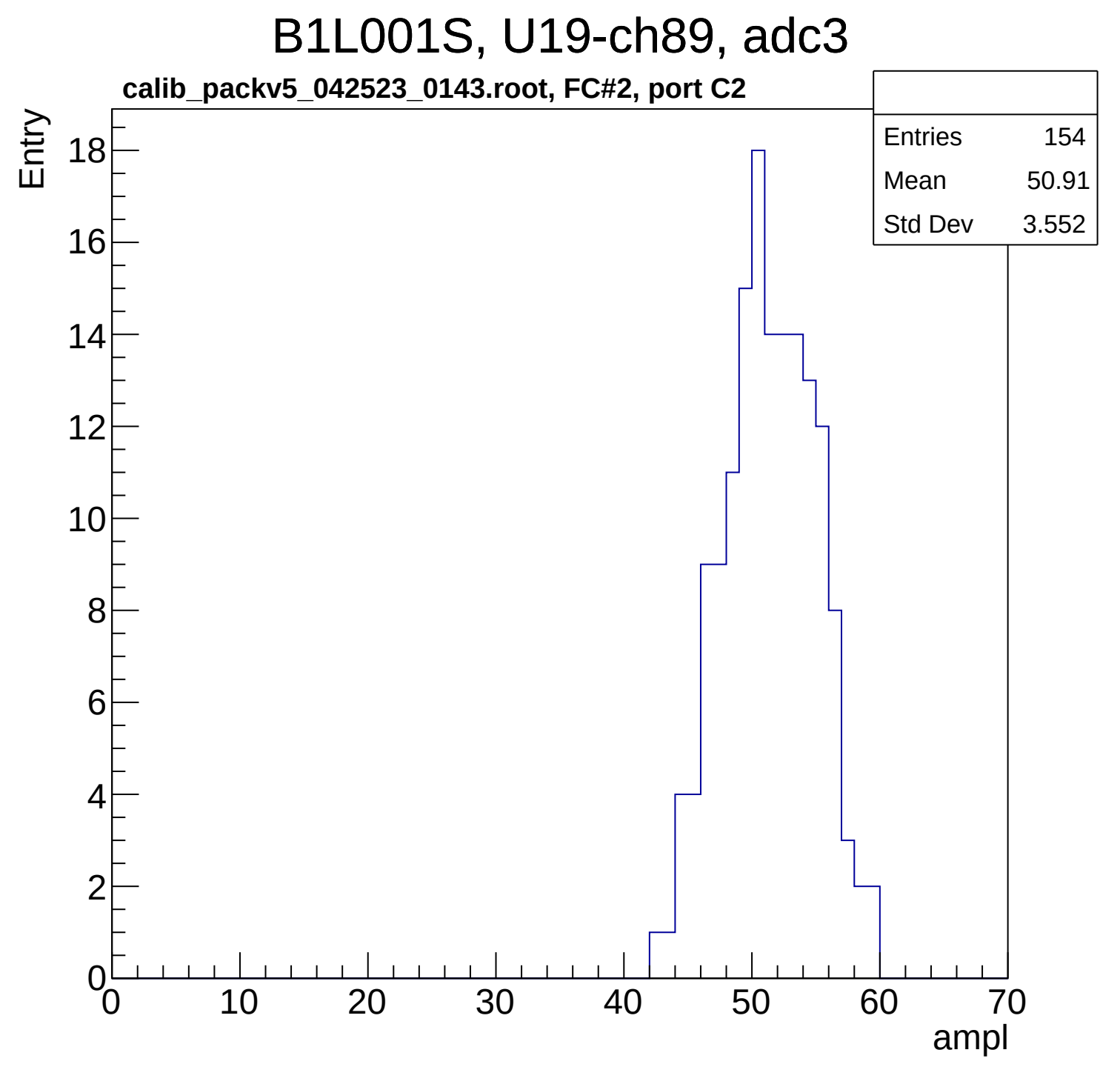
B1L001S, U19-ch89, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 154
Mean 50.91
Std Dev 3.552
Entry
ampl
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4
6
8
10
12
14
16
18
0
10
20
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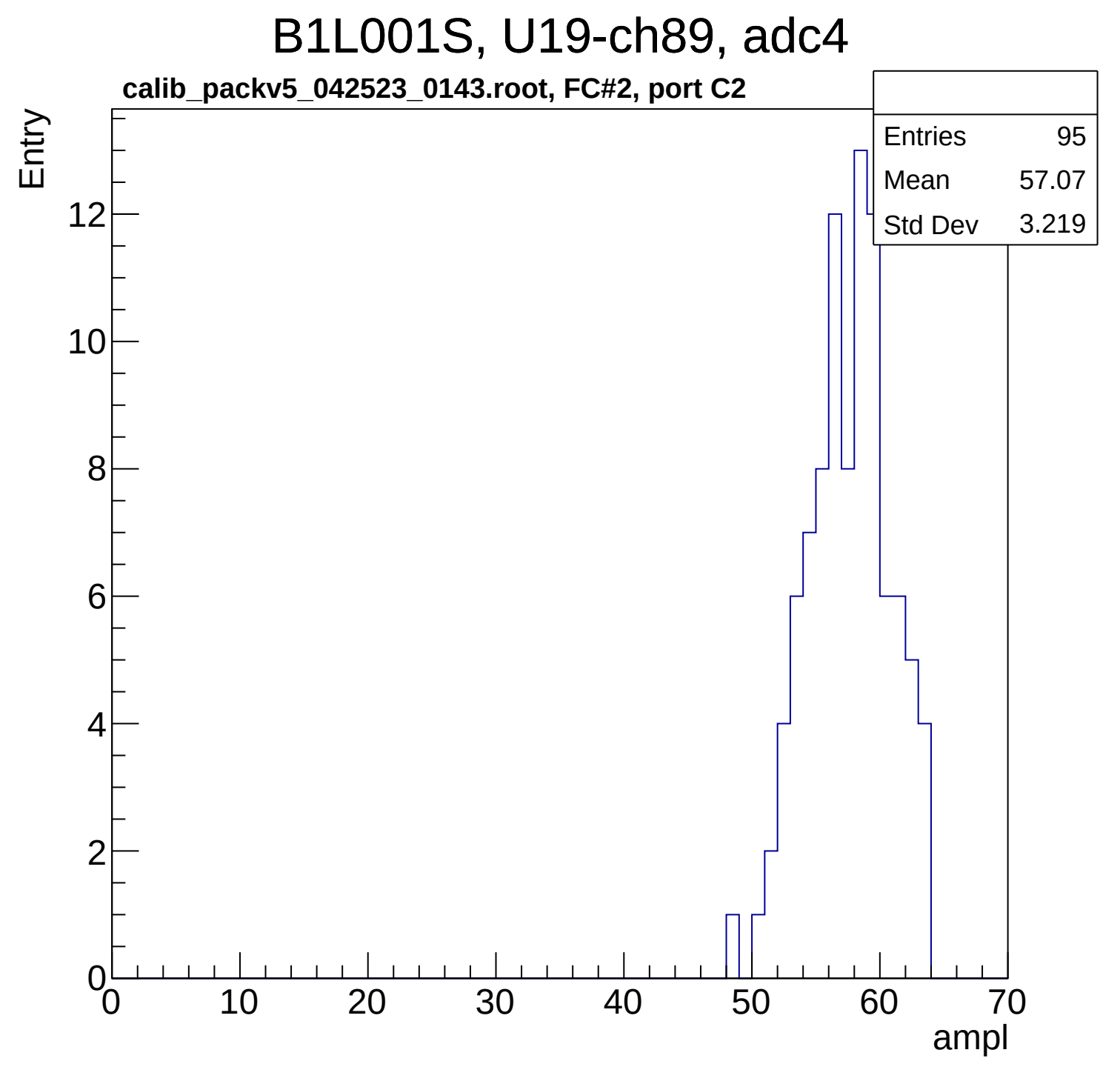
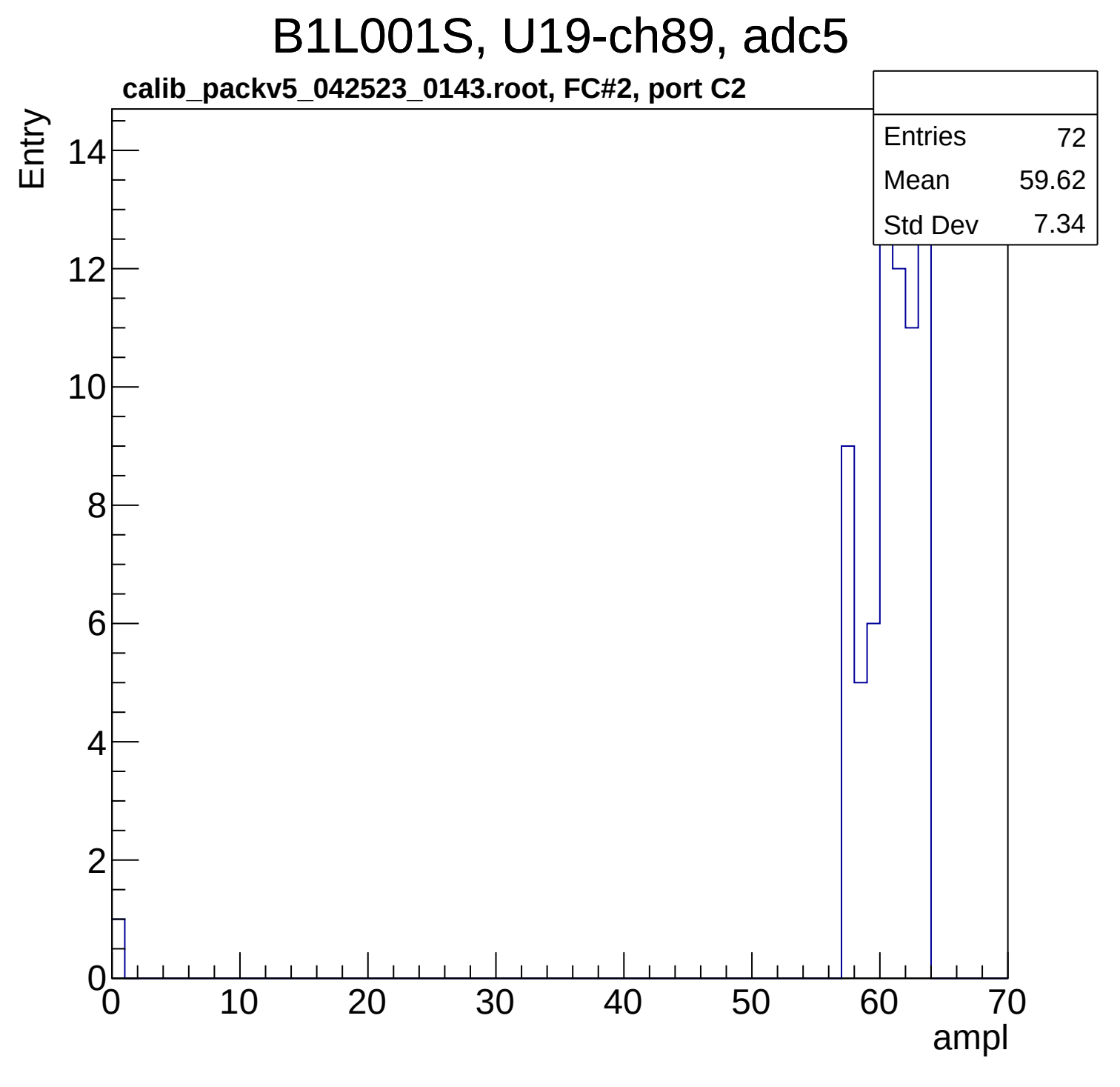

B1L001S, U19-ch89, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 95
Mean 57.07
Std Dev 3.219
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch89, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 72
Mean 59.62
Std Dev 7.34
Entry
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2
4
6
8
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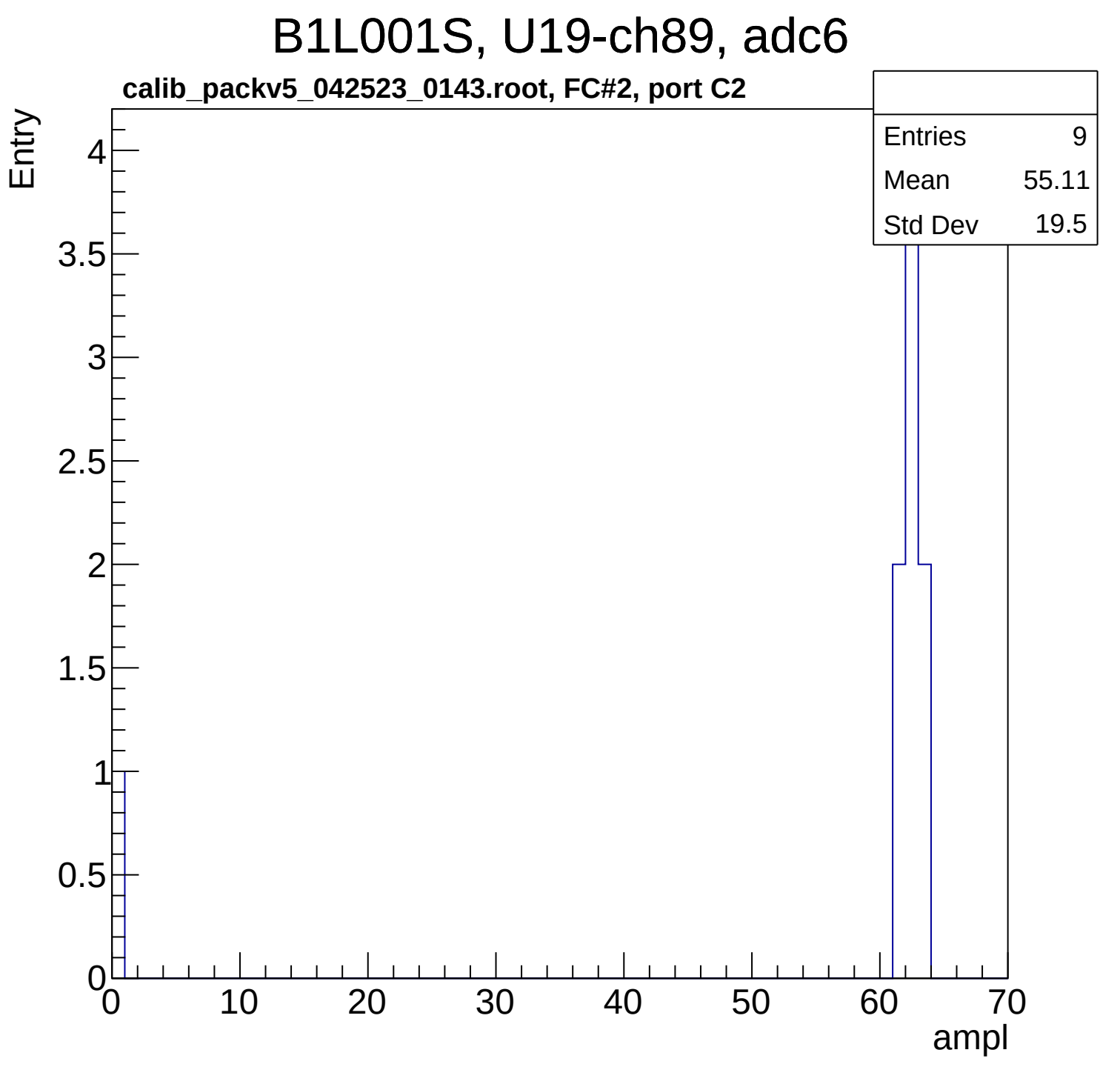
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch89, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 9
Mean 55.11
Std Dev 19.5
Entry
ampl
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0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
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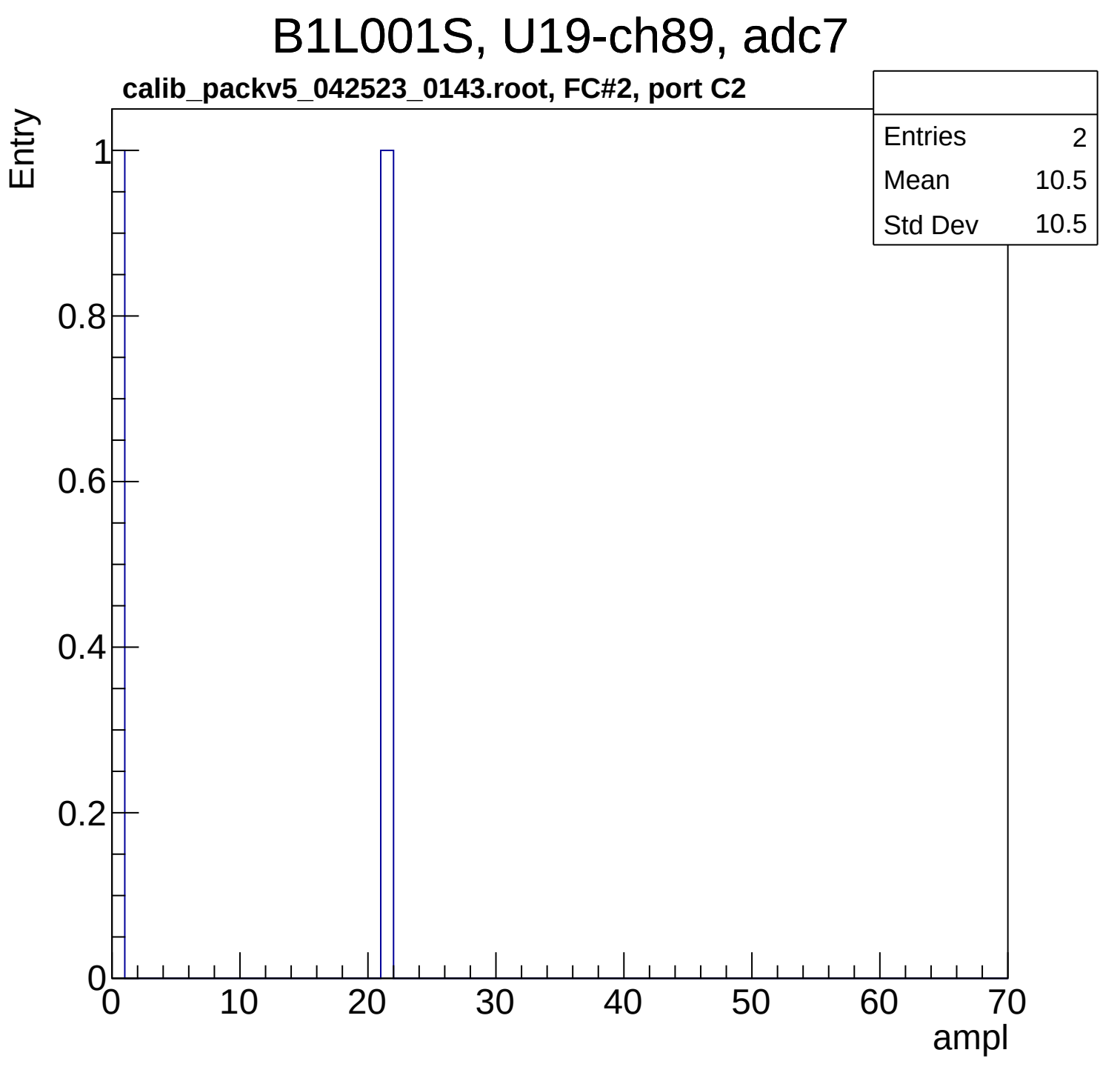
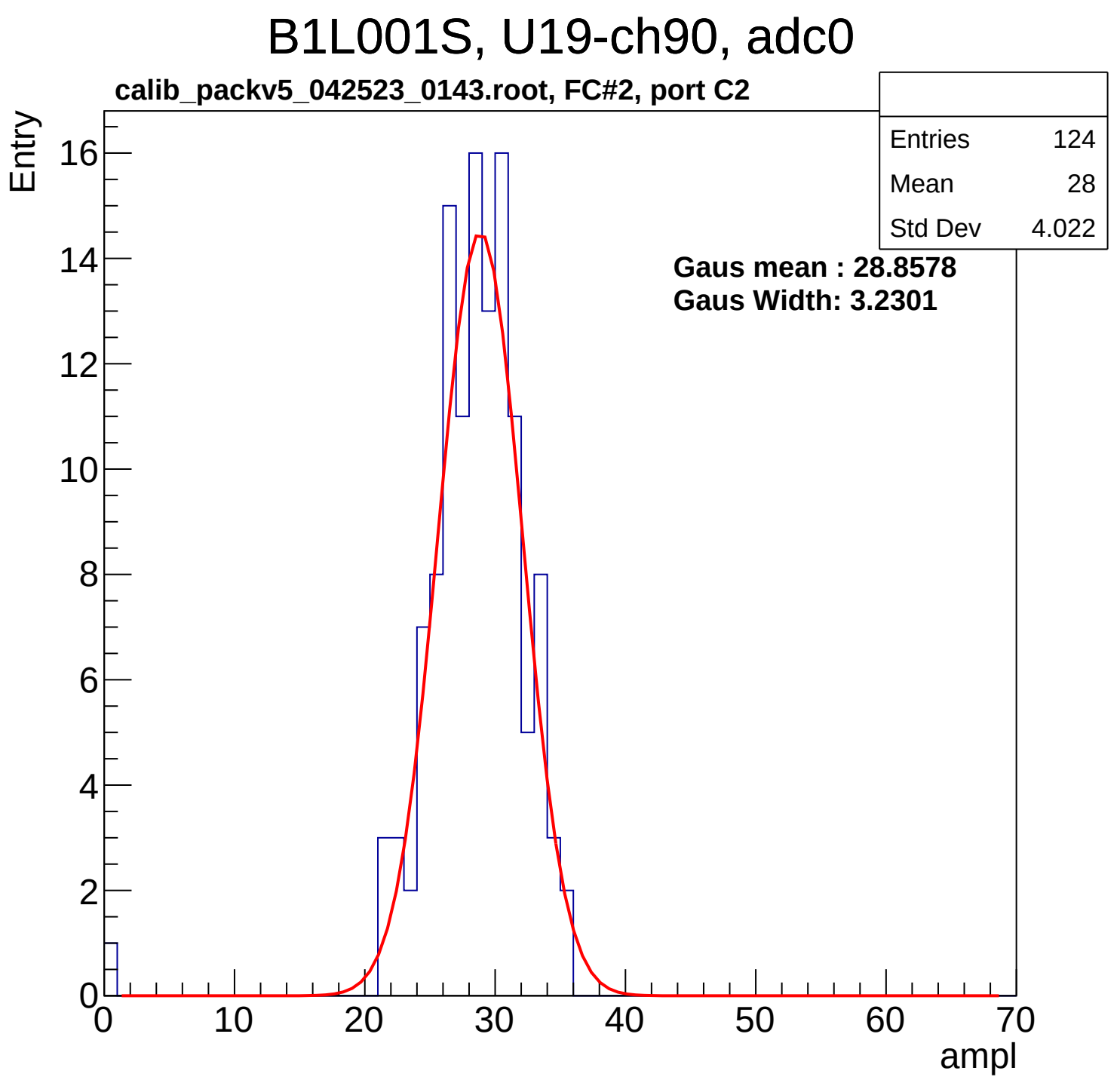
40
50
60
70


B1L001S, U19-ch89, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 10.5
Std Dev 10.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch90, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 124
Mean 28
Std Dev 4.022
Gaus mean : 28.8578
Gaus Width: 3.2301
Entry
ampl
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6
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0
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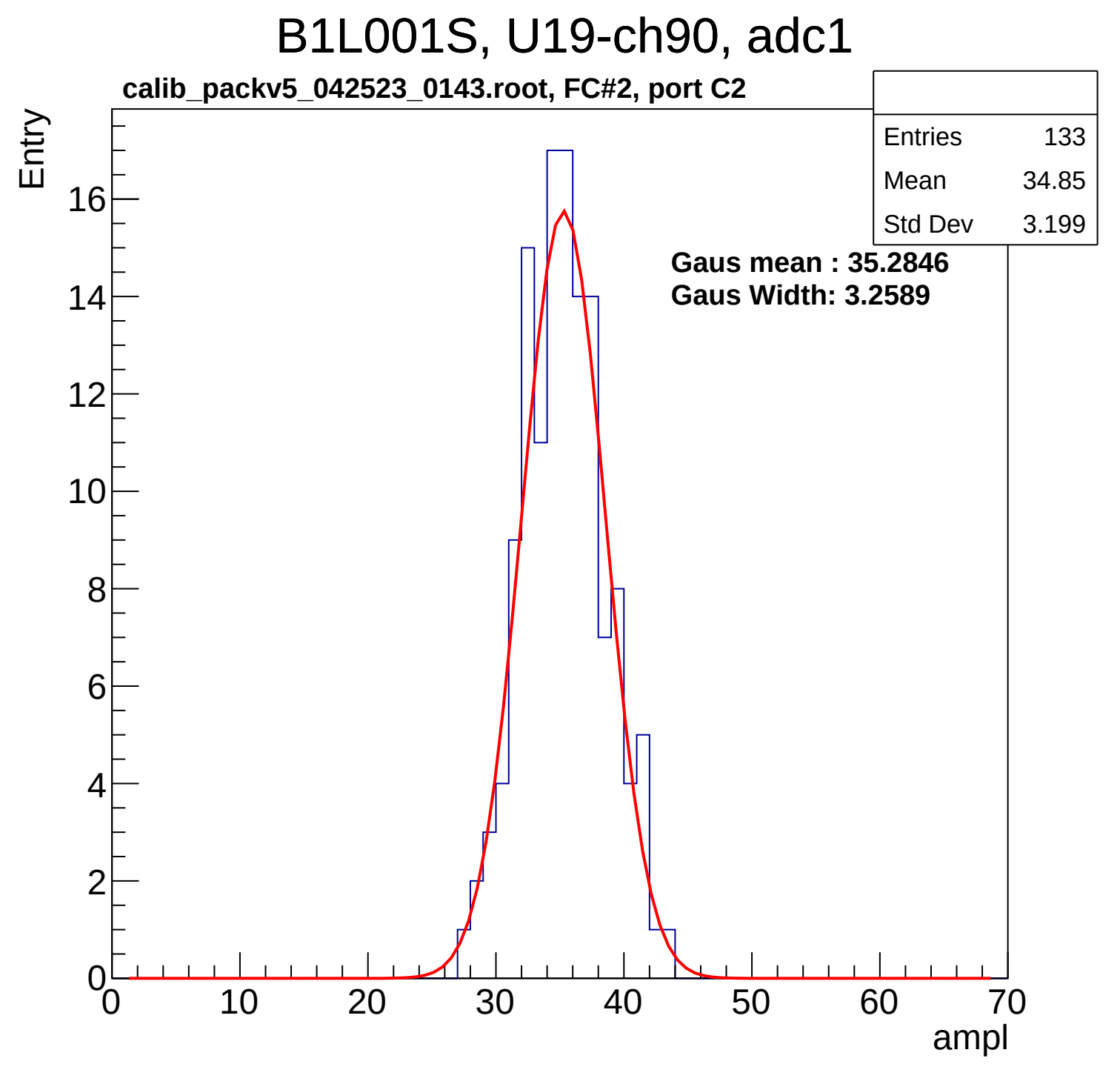
B1L001S, U19-ch90, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 133
Mean 34.85
Std Dev 3.199
Gaus mean : 35.2846
Gaus Width: 3.2589
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
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40
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60
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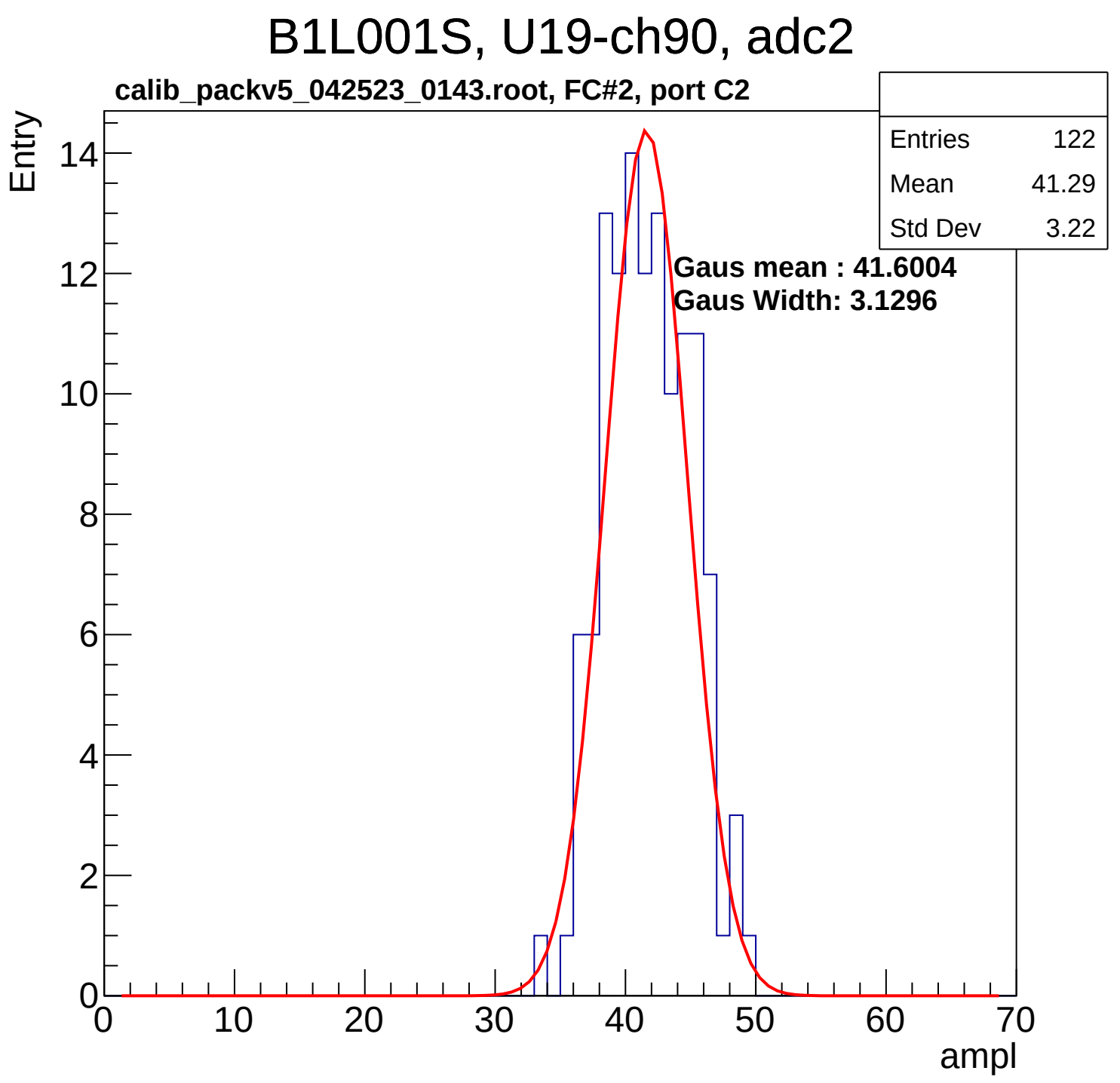
B1L001S, U19-ch90, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 122
Mean 41.29
Std Dev 3.22
Gaus mean : 41.6004
Gaus Width: 3.1296
Entry
ampl
0
2
4
6
8
10
12
14
0
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60
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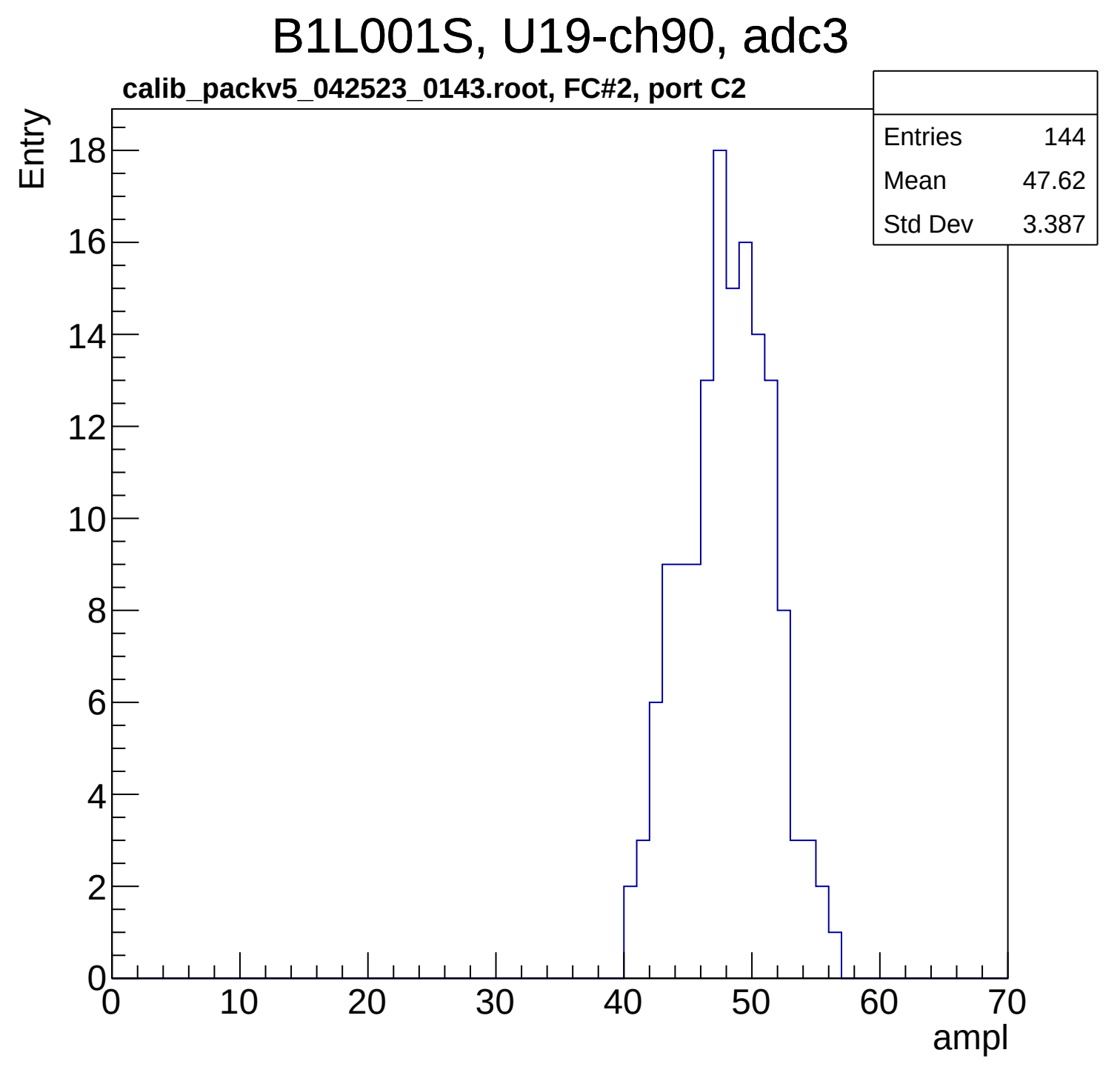
B1L001S, U19-ch90, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 144
Mean 47.62
Std Dev 3.387
Entry
ampl
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4
6
8
10
12
14
16
18
0
10
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60
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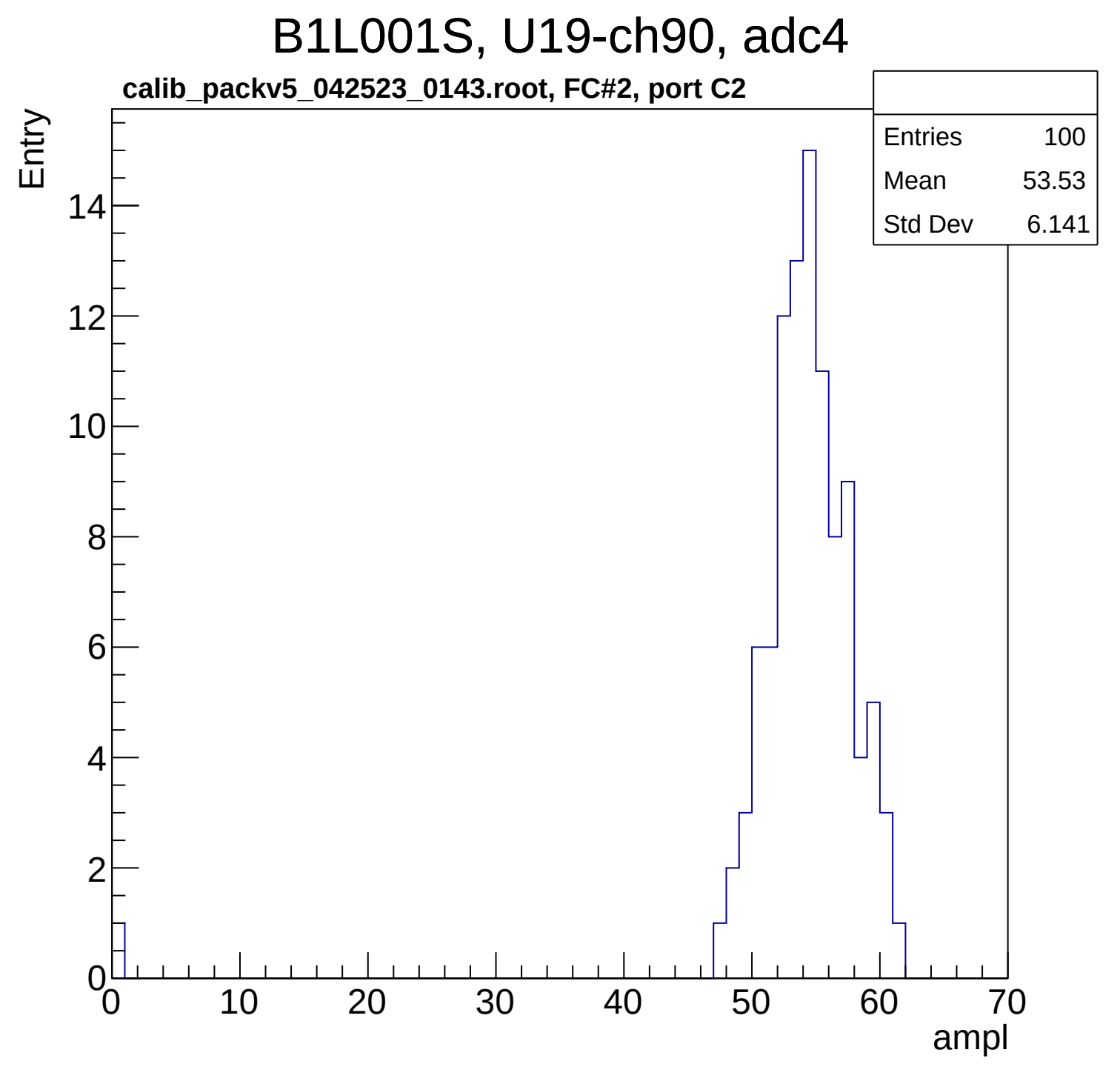
B1L001S, U19-ch90, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 100
Mean 53.53
Std Dev 6.141
Entry
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2
4
6
8
10
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14
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10
20
30
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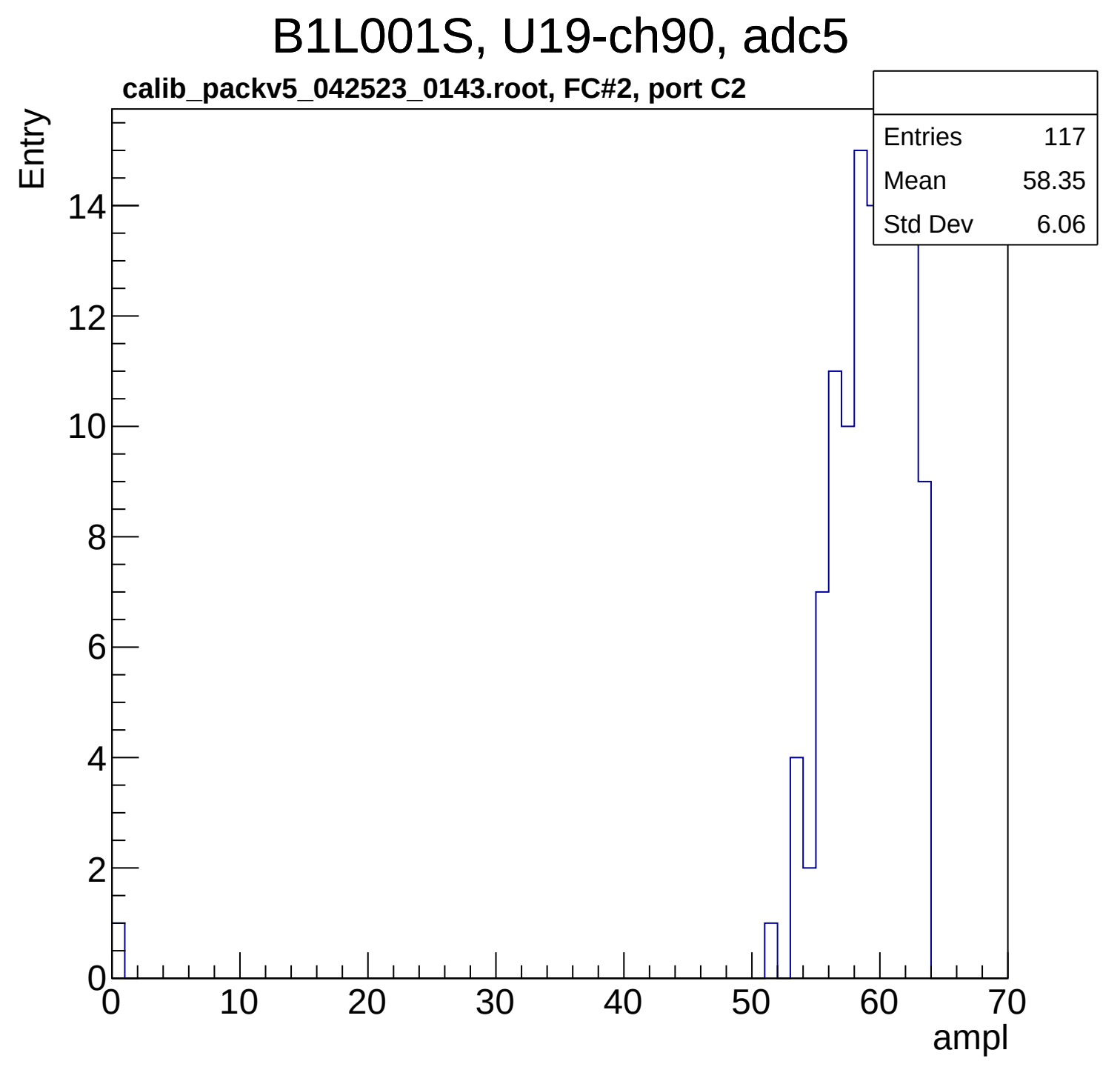
50
60
70
ampl


B1L001S, U19-ch90, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 117
Mean 58.35
Std Dev 6.06
Entry
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2
4
6
8
10
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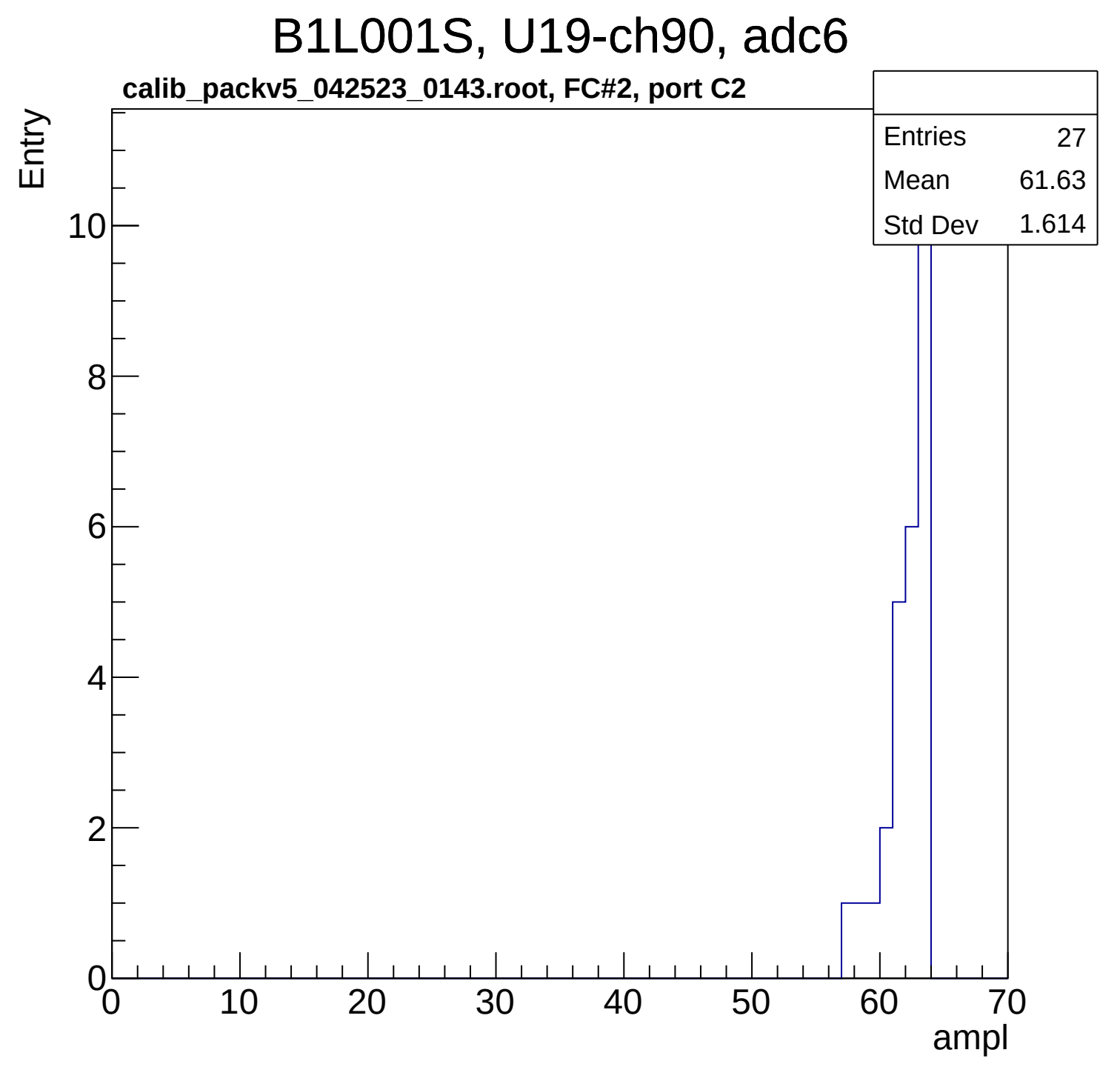
14
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch90, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 27
Mean 61.63
Std Dev 1.614
Entry
0
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8
10
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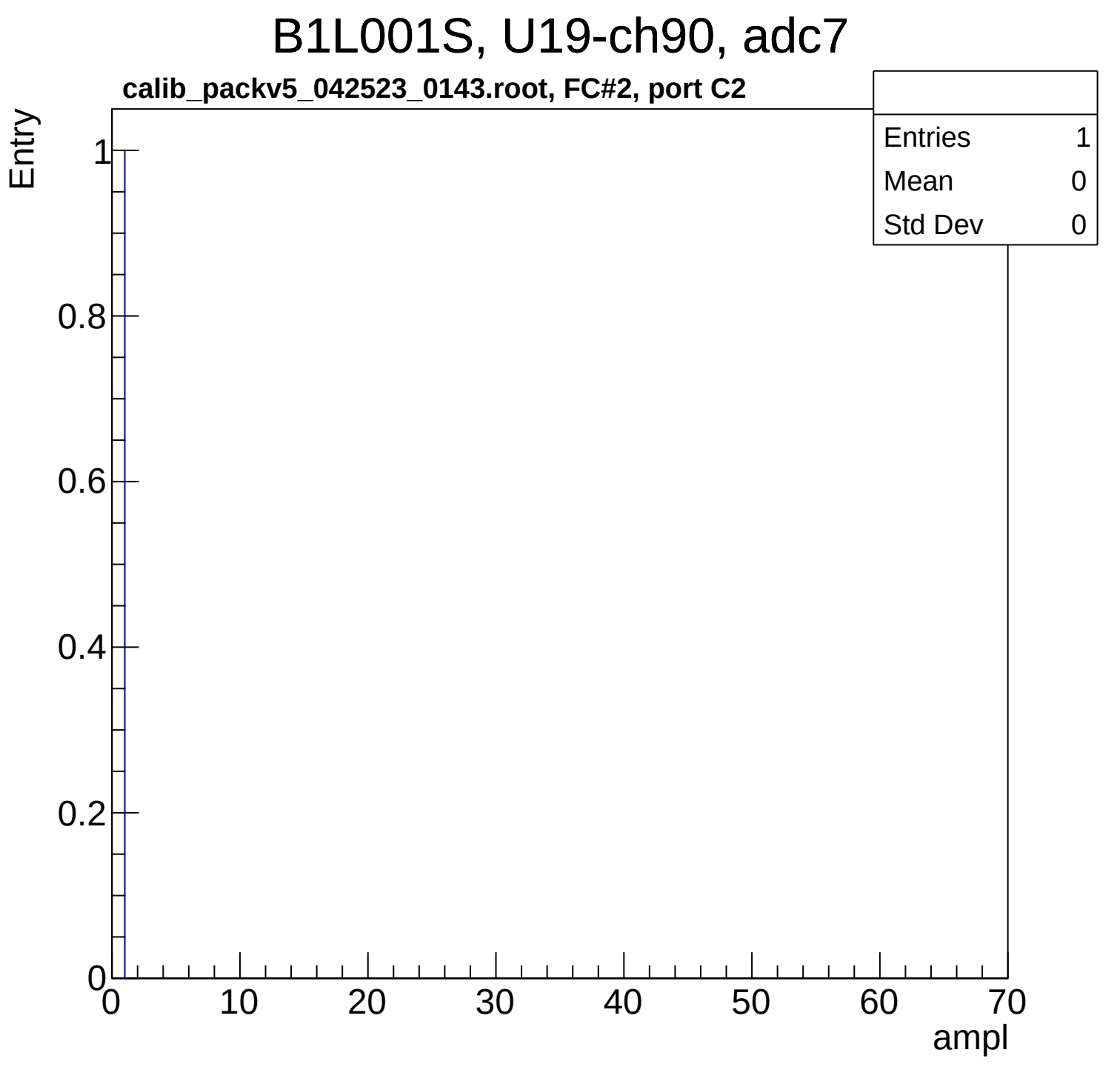
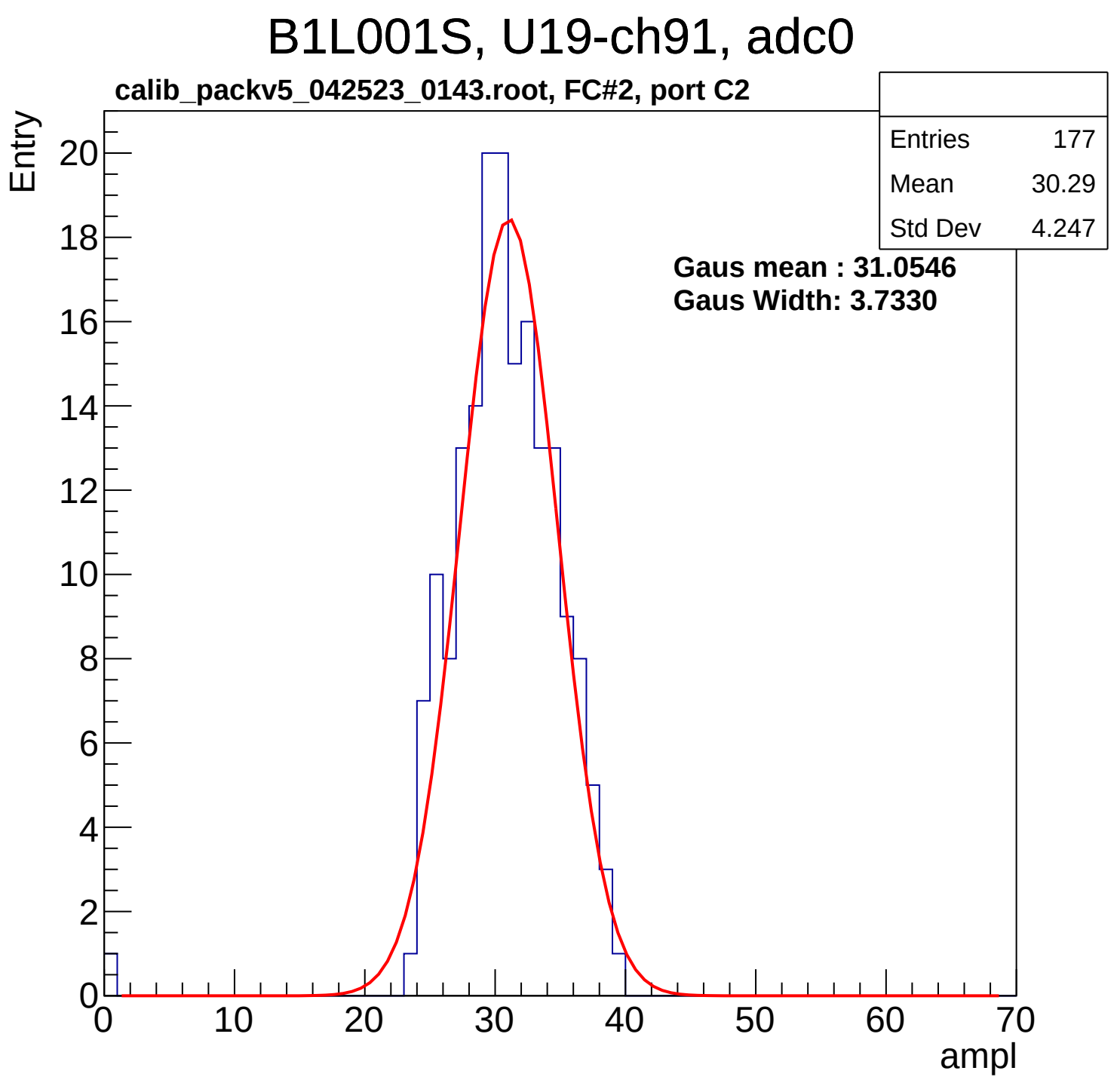
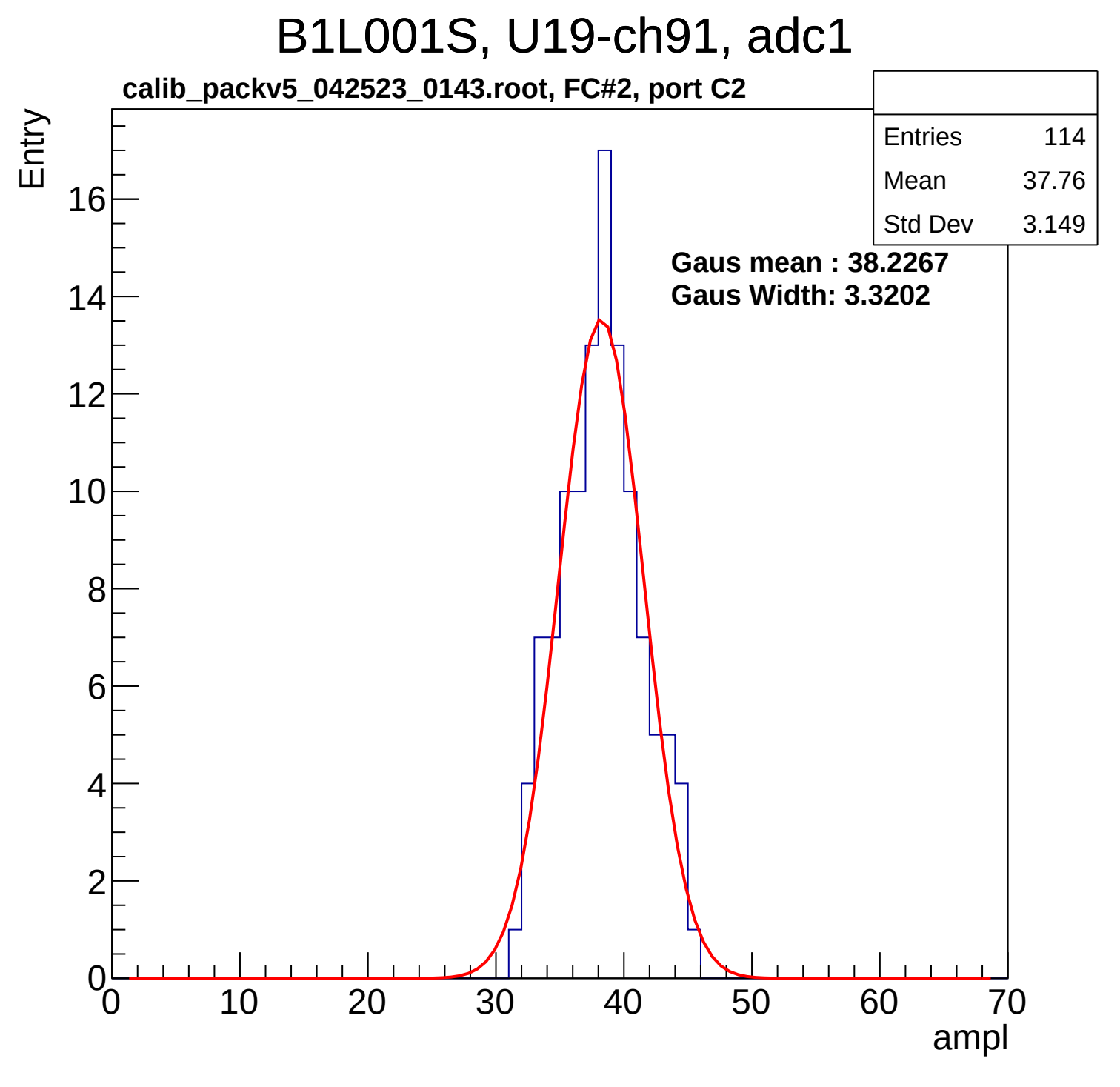
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch90, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch91, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 177
Mean 30.29
Std Dev 4.247
Gaus mean : 31.0546
Gaus Width: 3.7330
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70


B1L001S, U19-ch91, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 114
Mean 37.76
Std Dev 3.149
Gaus mean : 38.2267
Gaus Width: 3.3202
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
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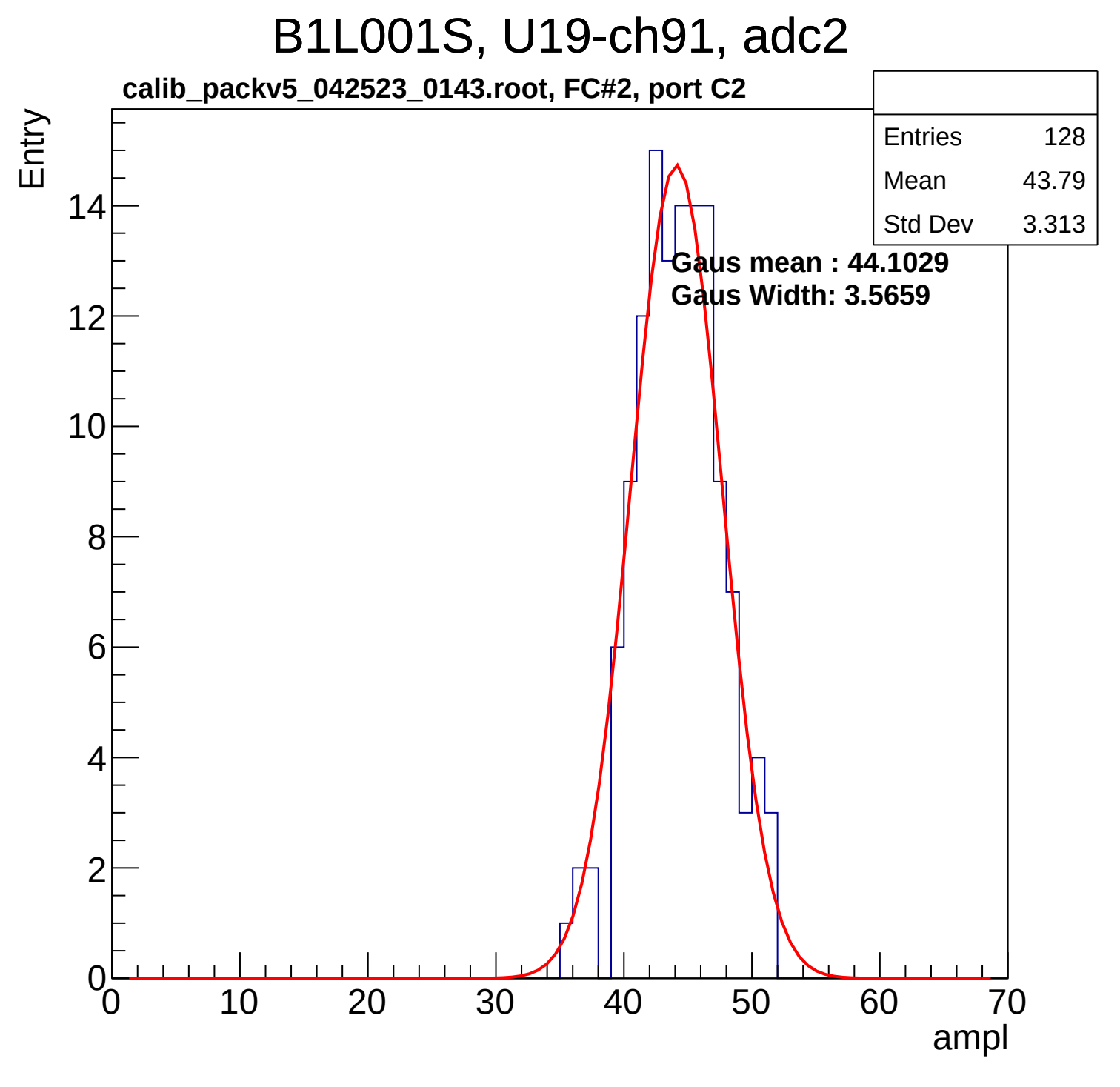
B1L001S, U19-ch91, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 128
Mean 43.79
Std Dev 3.313
Gaus mean : 44.1029
Gaus Width: 3.5659
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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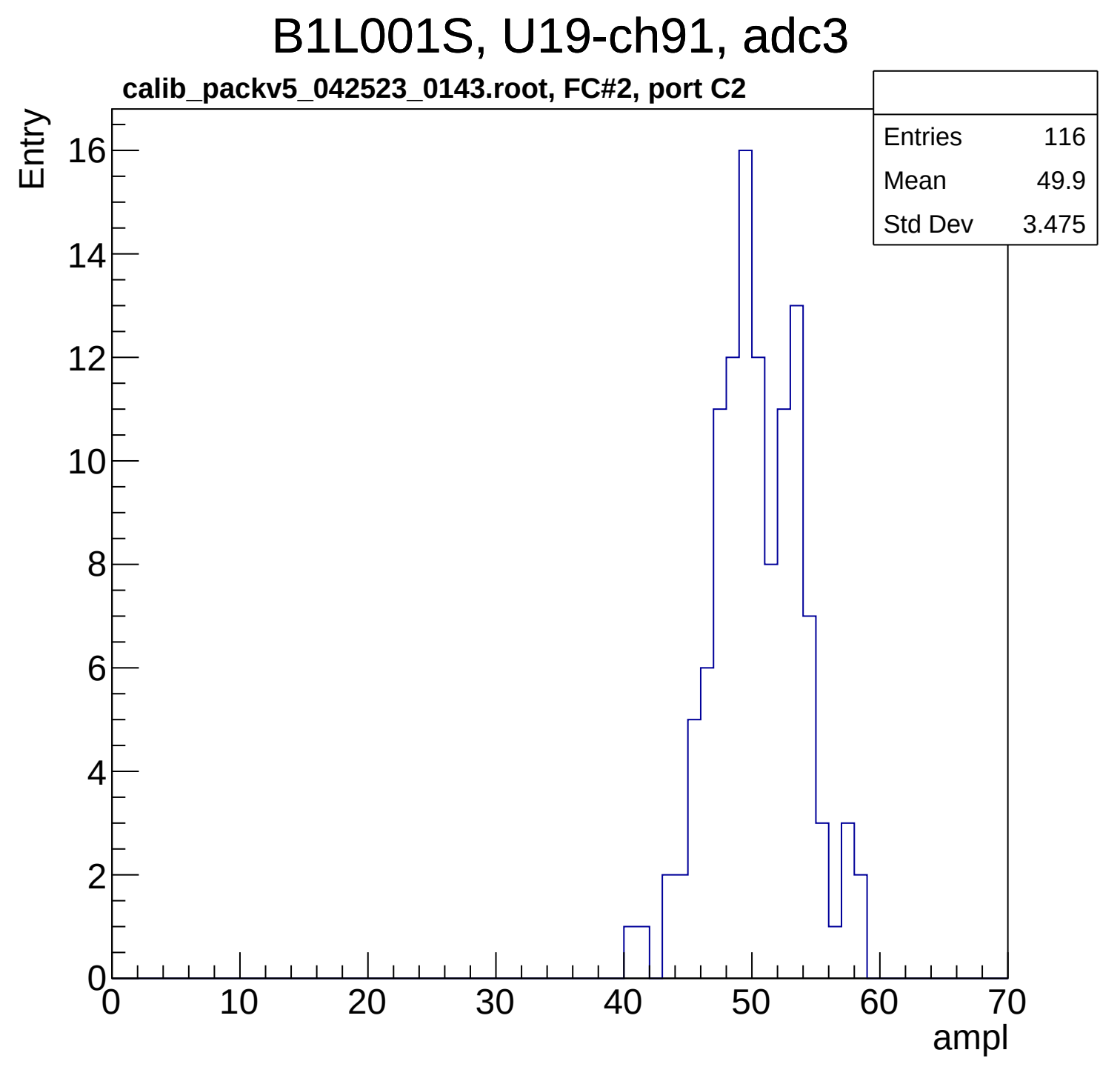
B1L001S, U19-ch91, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 116
Mean 49.9
Std Dev 3.475
Entry
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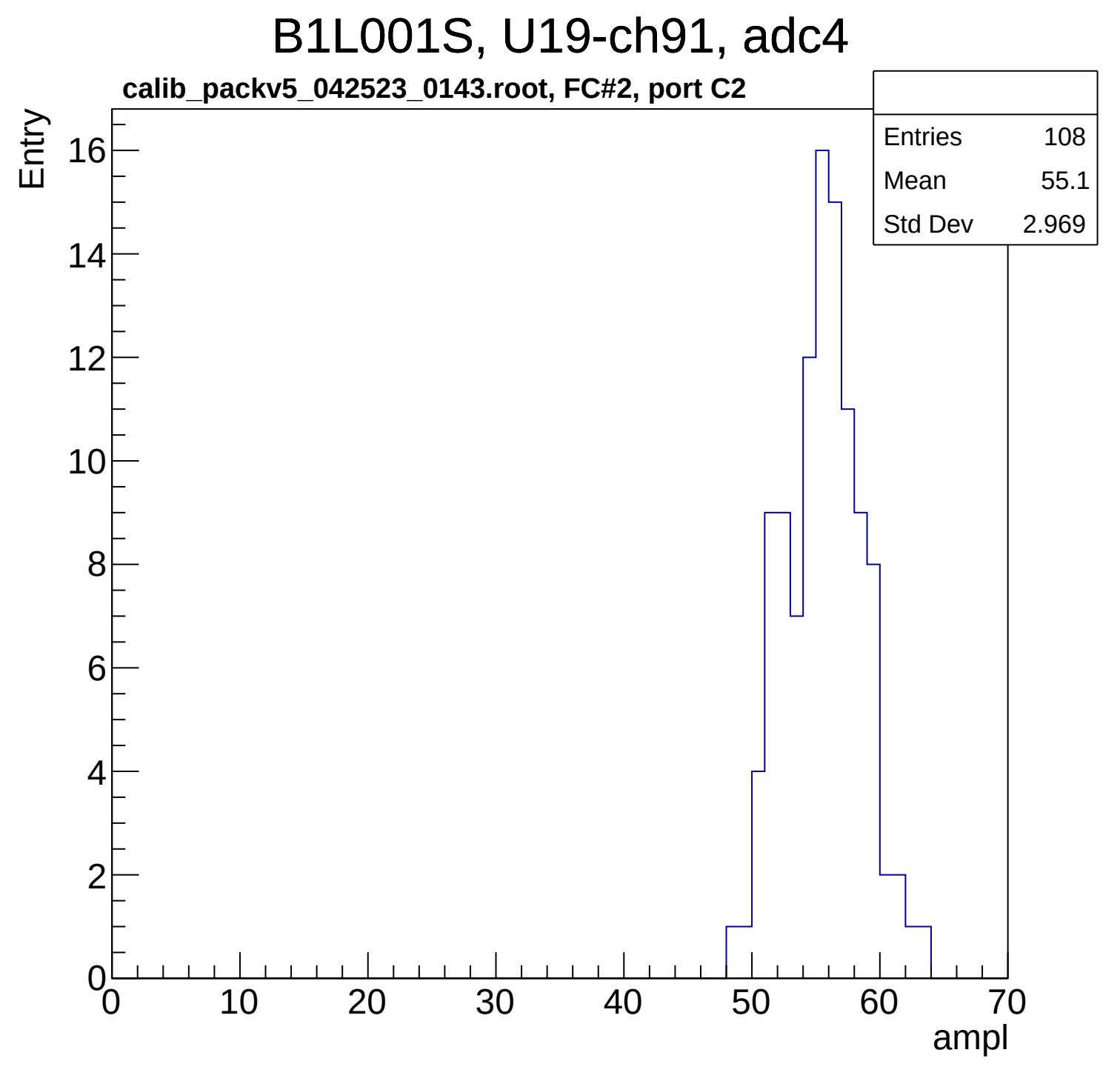
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch91, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 108
Mean 55.1
Std Dev 2.969
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
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40
50
60
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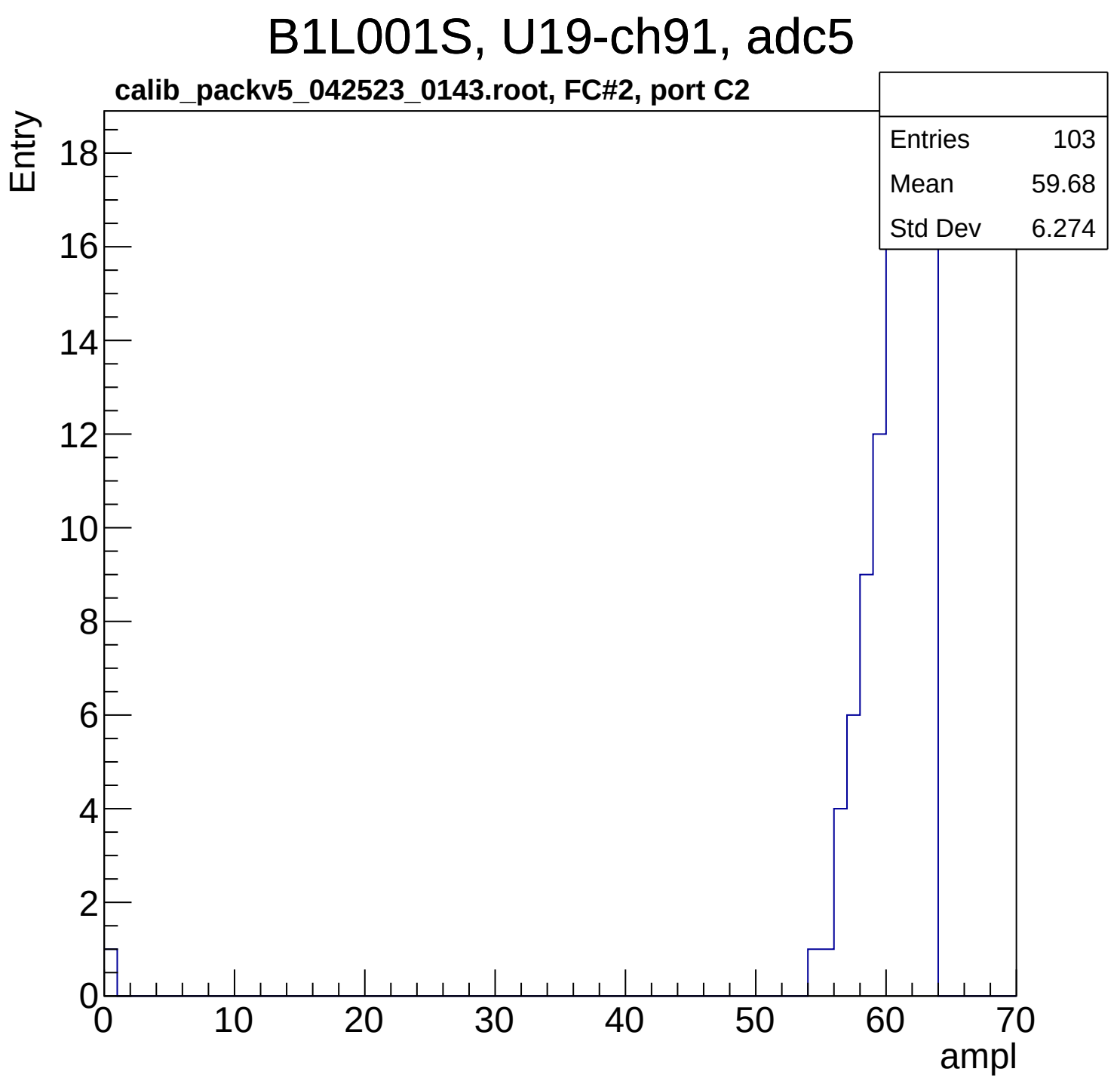
B1L001S, U19-ch91, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 103
Mean 59.68
Std Dev 6.274
Entry
0
2
4
6
8
10
12
14
16
18
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10
20
30
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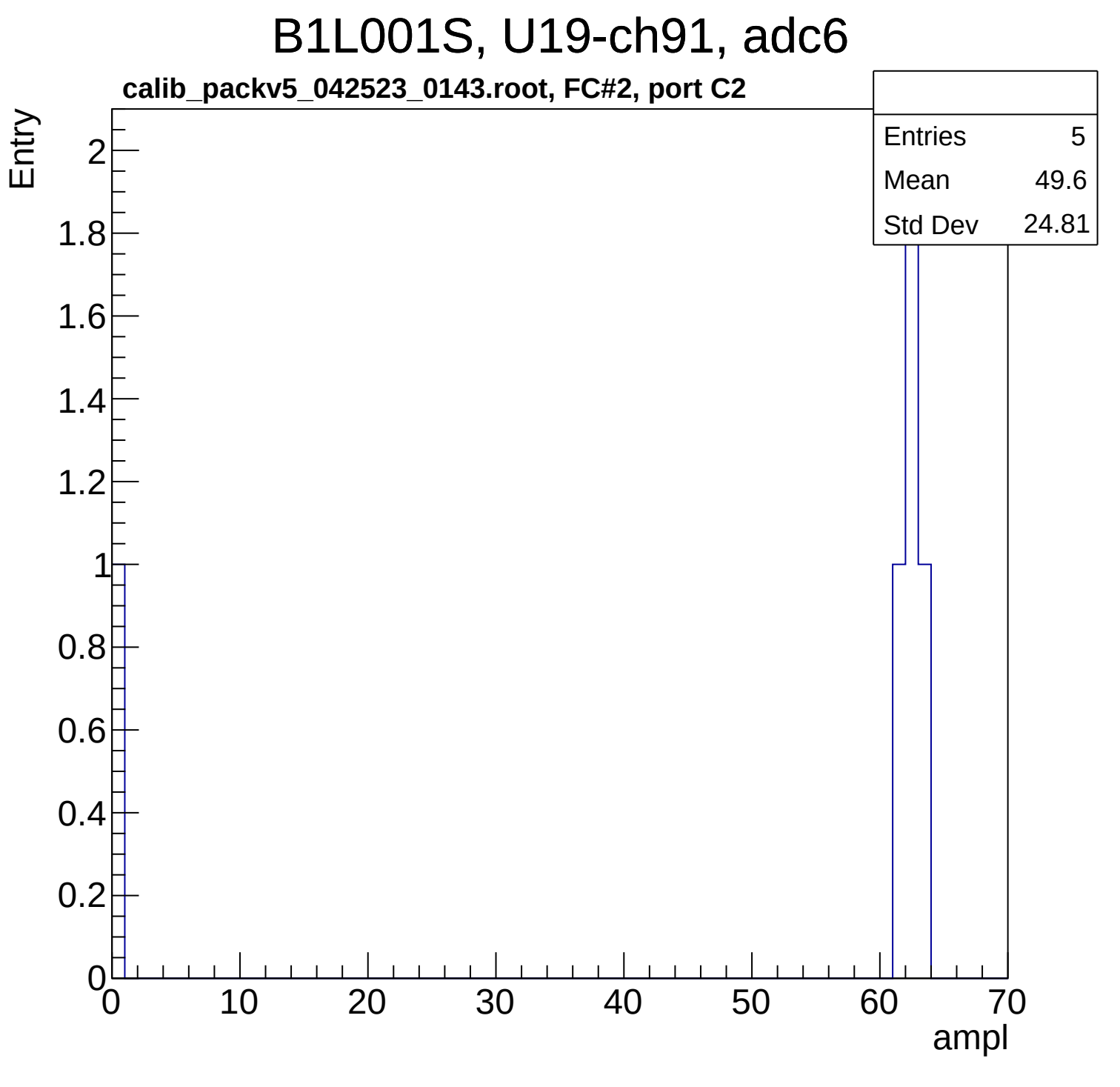
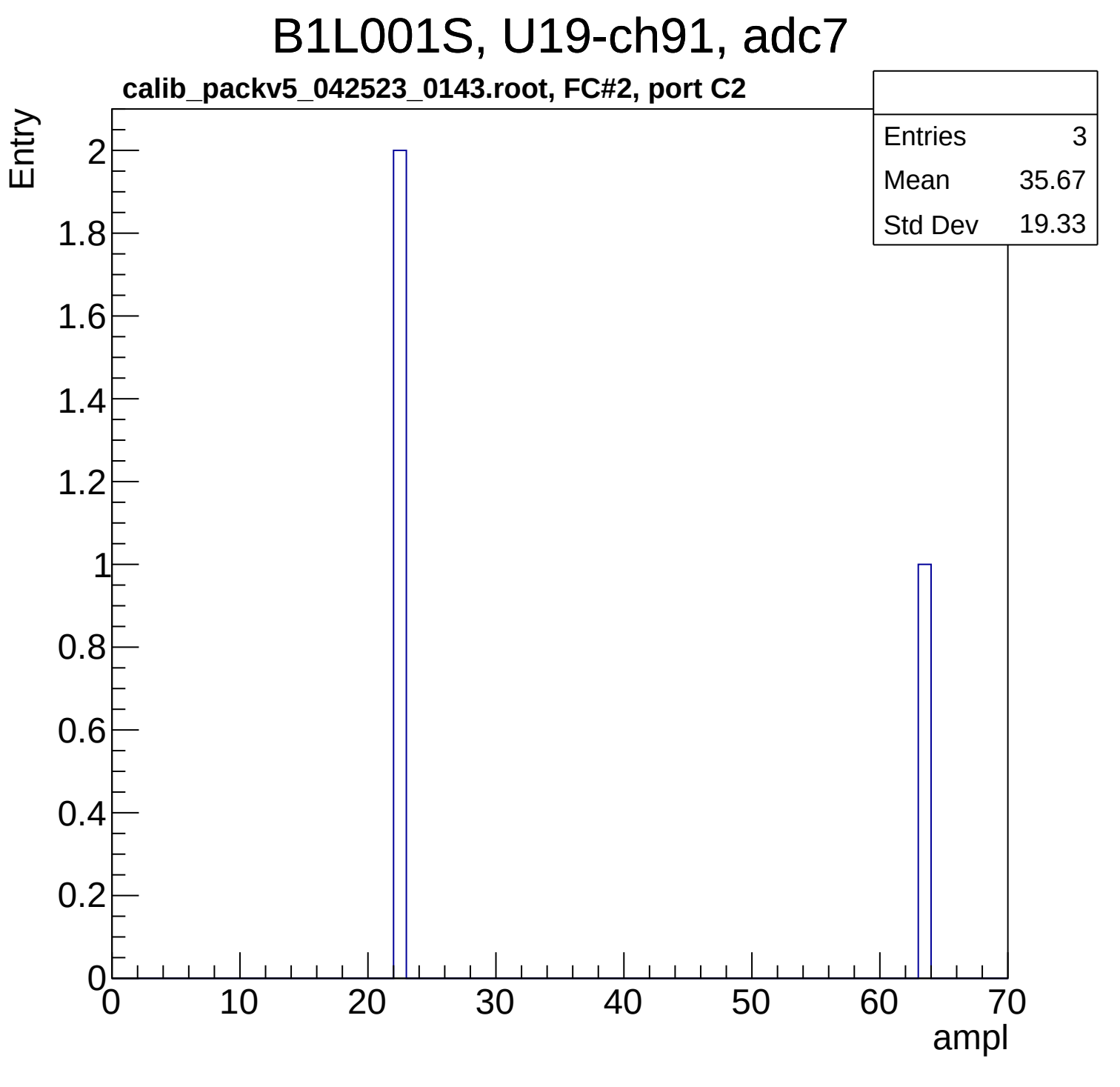
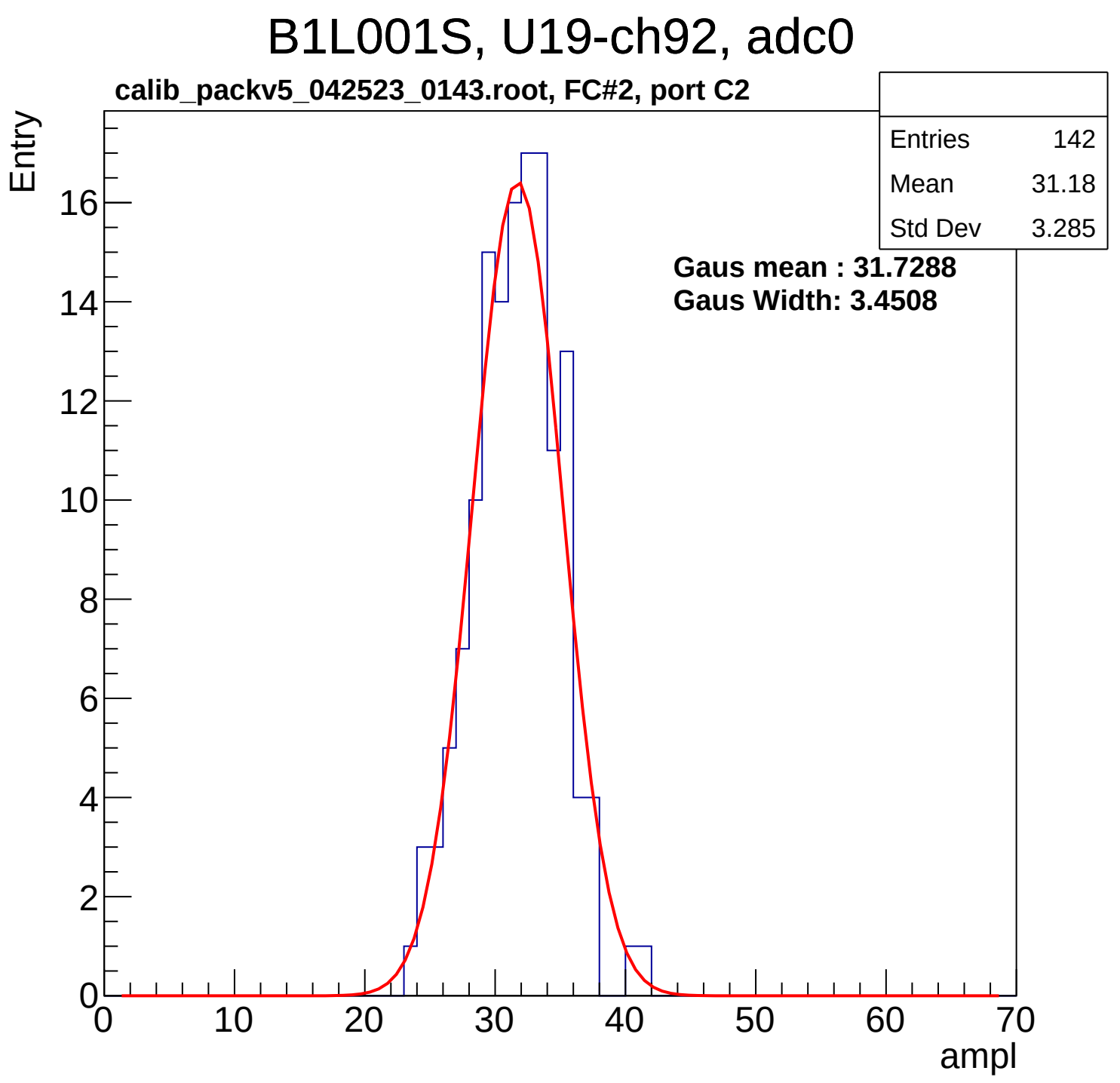
50
60
70
ampl


B1L001S, U19-ch91, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 5
Mean 49.6
Std Dev 24.81
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L001S, U19-ch91, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 3
Mean 35.67
Std Dev 19.33
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L001S, U19-ch92, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 142
Mean 31.18
Std Dev 3.285
Gaus mean : 31.7288
Gaus Width: 3.4508
Entry
ampl
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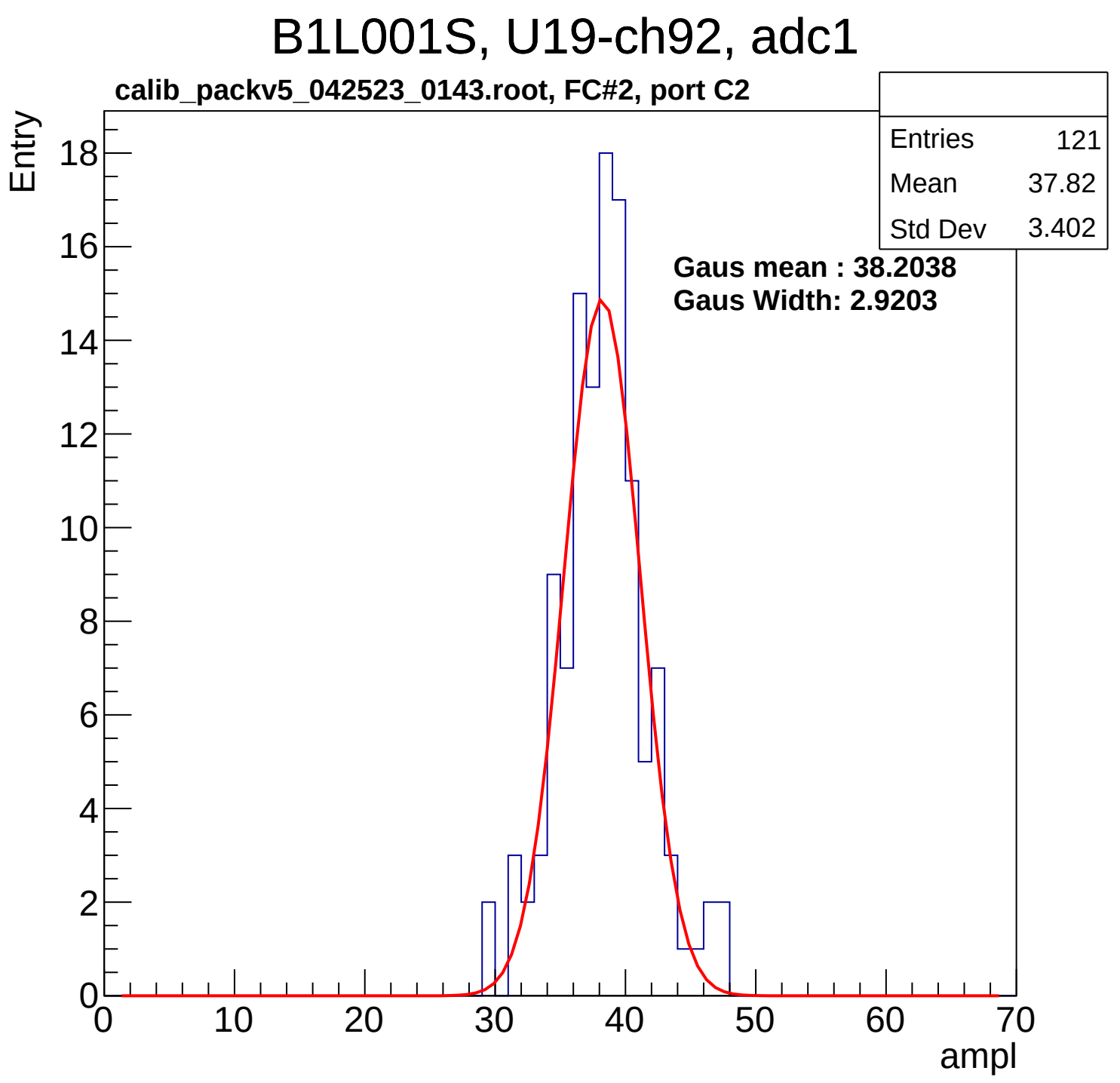
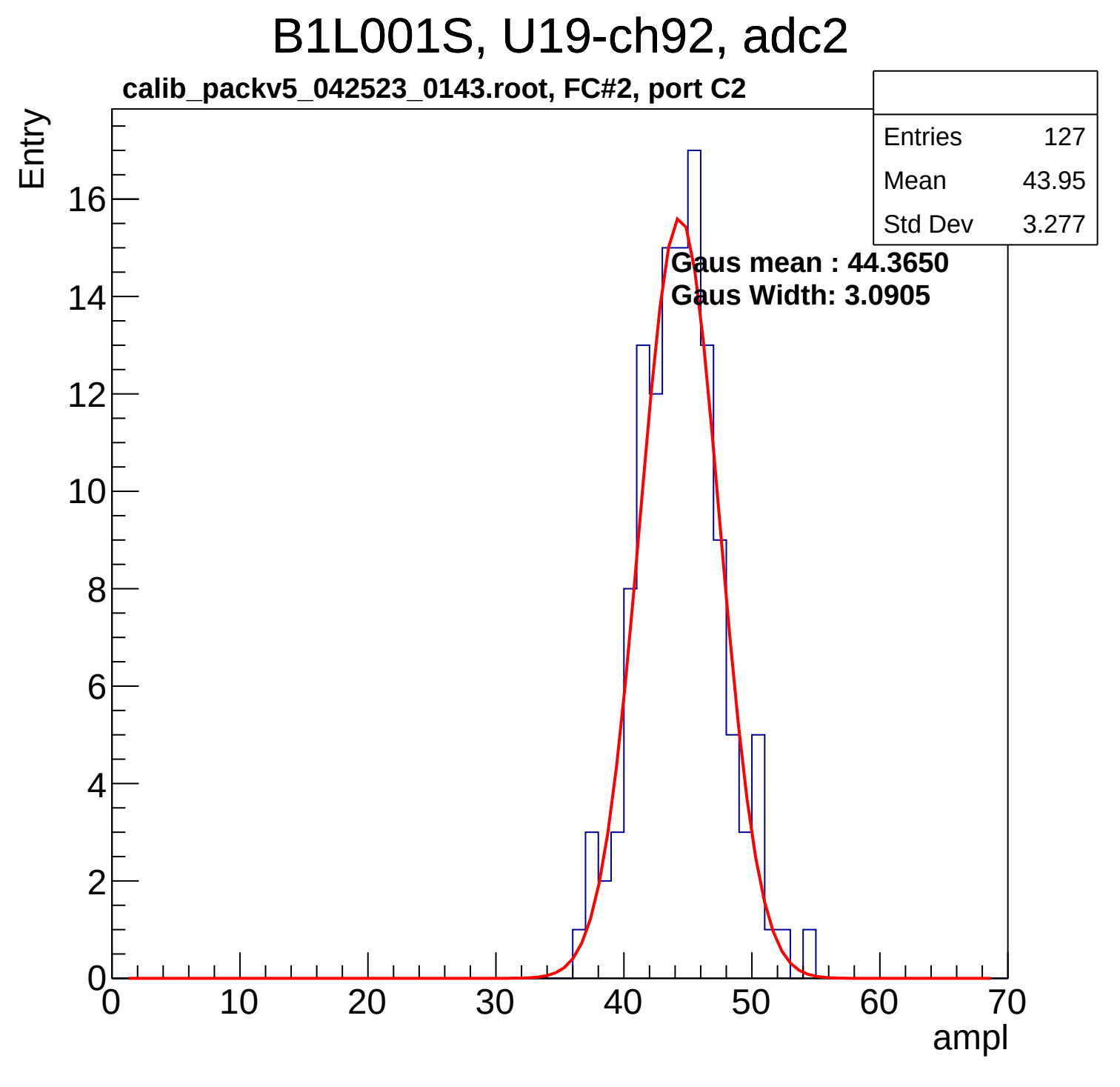
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70


B1L001S, U19-ch92, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 121
Mean 37.82
Std Dev 3.402
Gaus mean : 38.2038
Gaus Width: 2.9203
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70


B1L001S, U19-ch92, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 127
Mean 43.95
Std Dev 3.277
Gaus mean : 44.3650
Gaus Width: 3.0905
Entry
ampl
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2
4
6
8
10
12
14
16
0
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20
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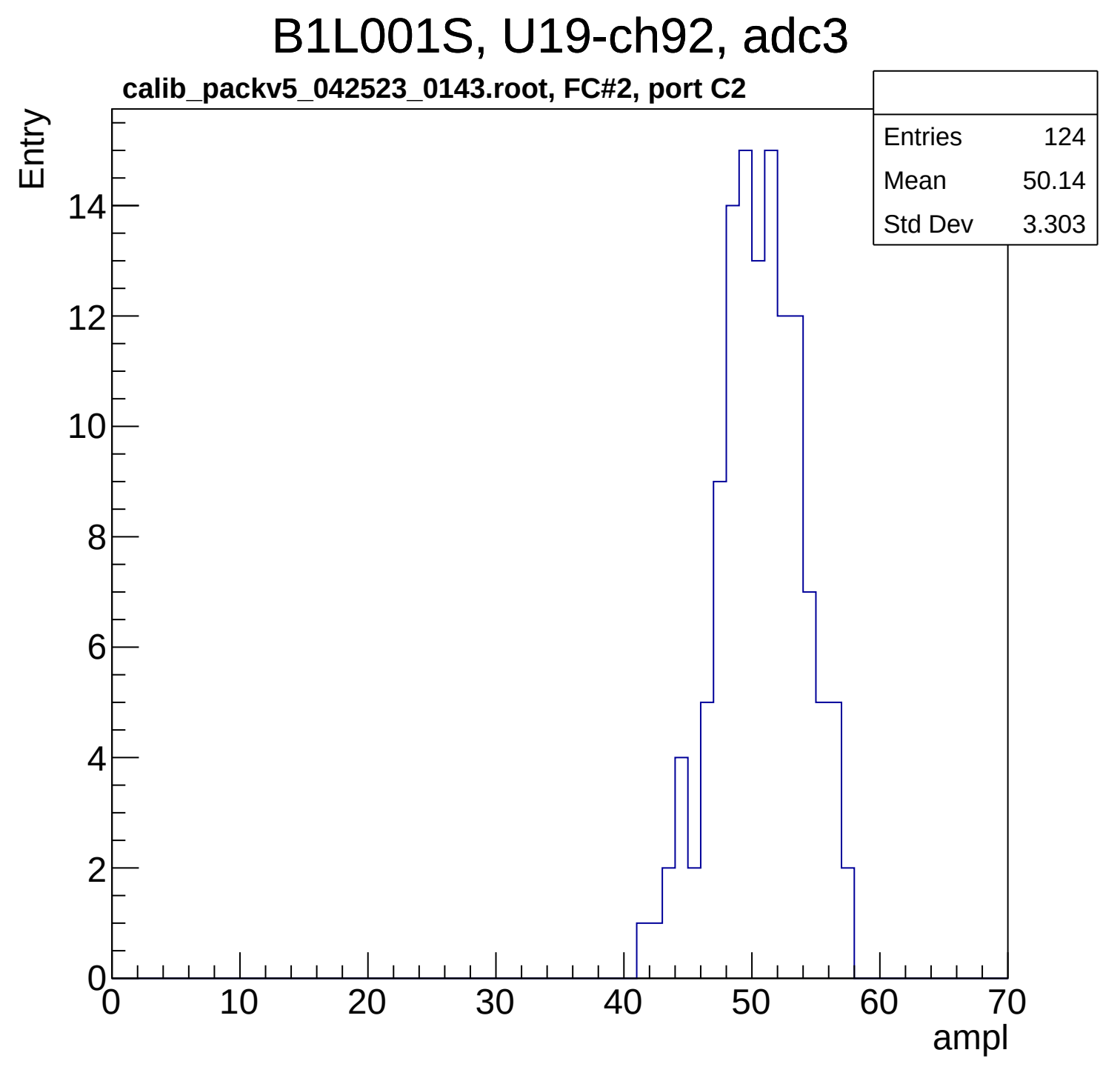
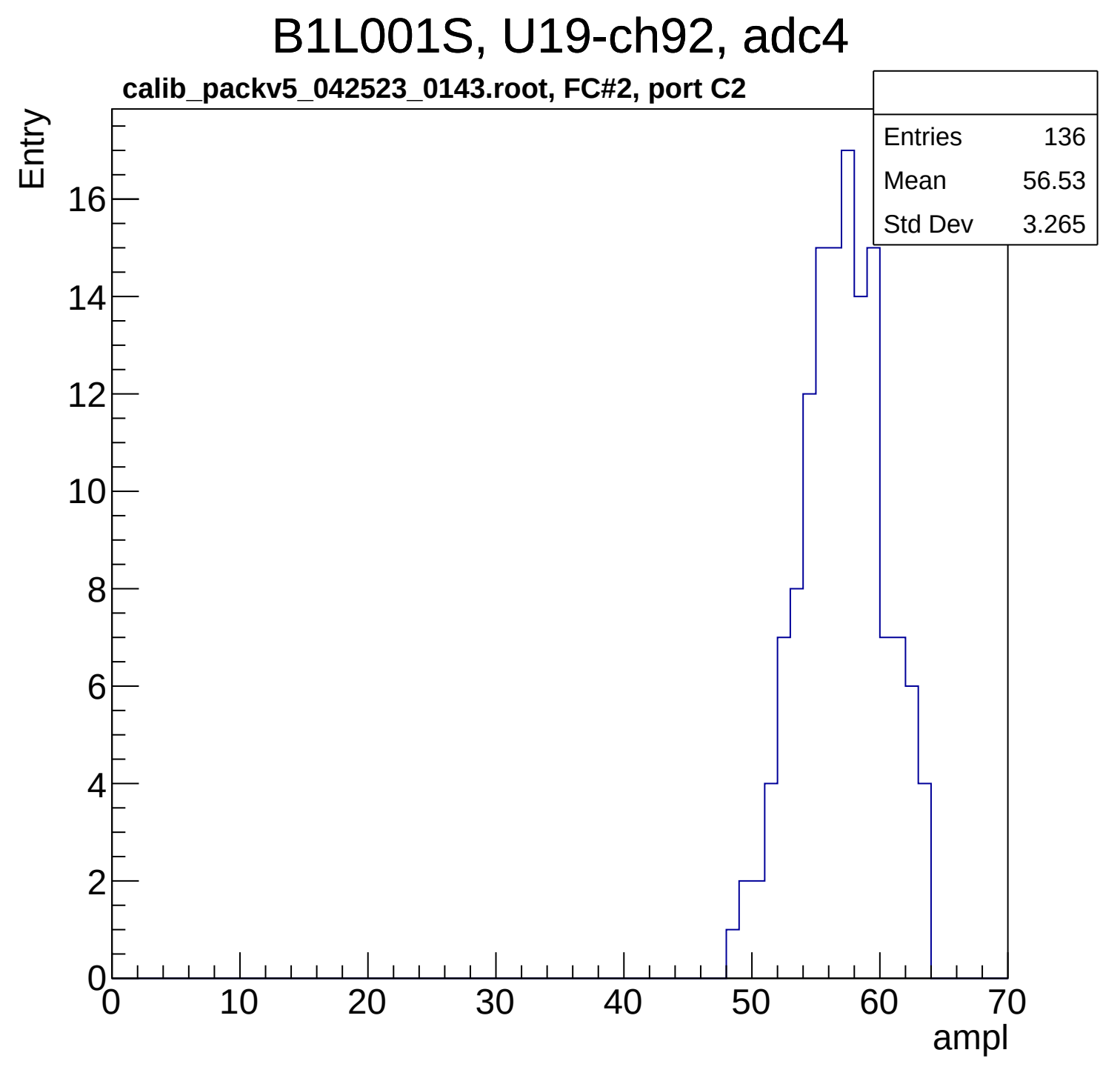

B1L001S, U19-ch92, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 124
Mean 50.14
Std Dev 3.303
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L001S, U19-ch92, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 136
Mean 56.53
Std Dev 3.265
Entry
ampl
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2
4
6
8
10
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0
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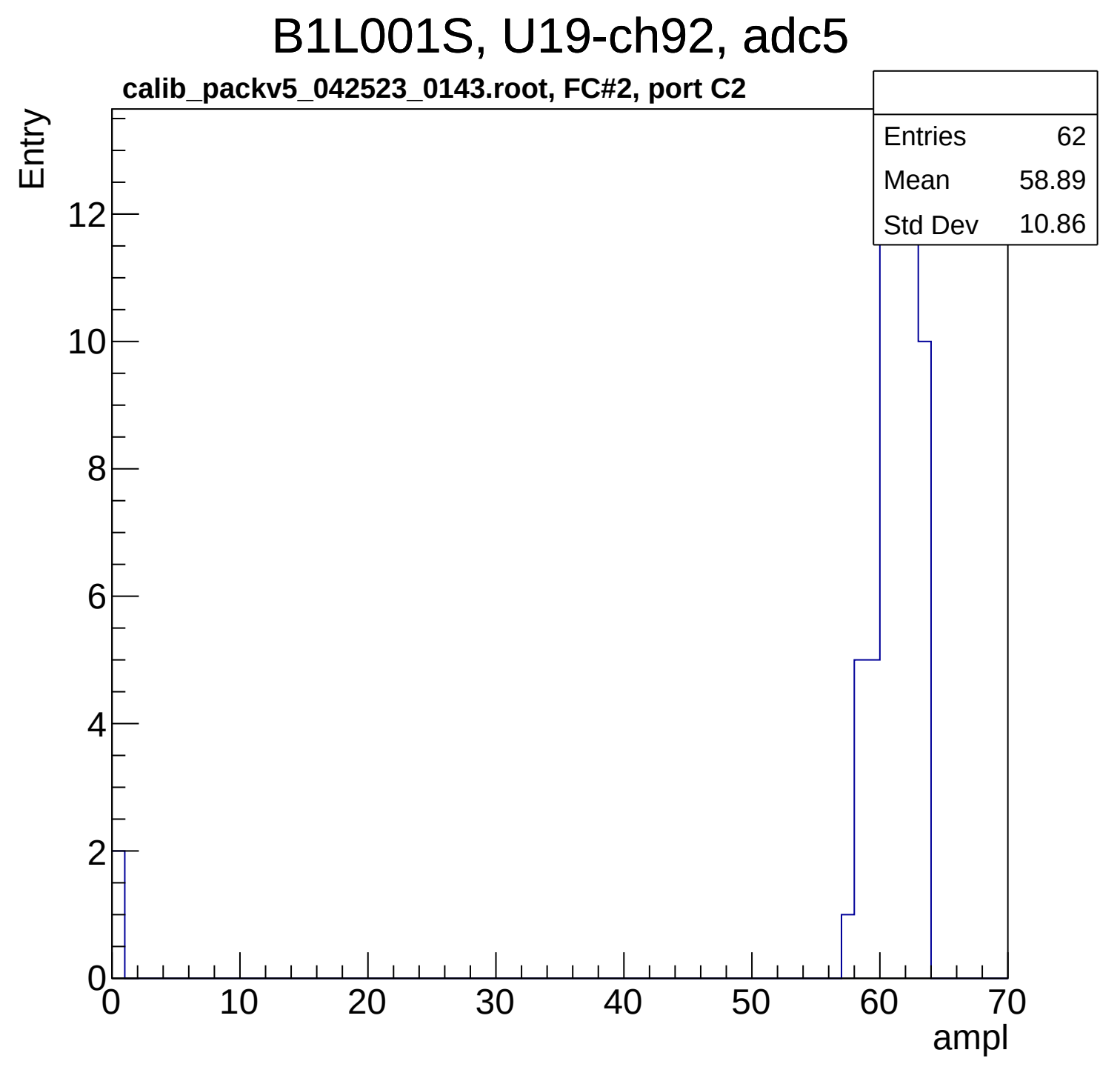
B1L001S, U19-ch92, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 62
Mean 58.89
Std Dev 10.86
Entry
0
2
4
6
8
10
12
0
10
20
30
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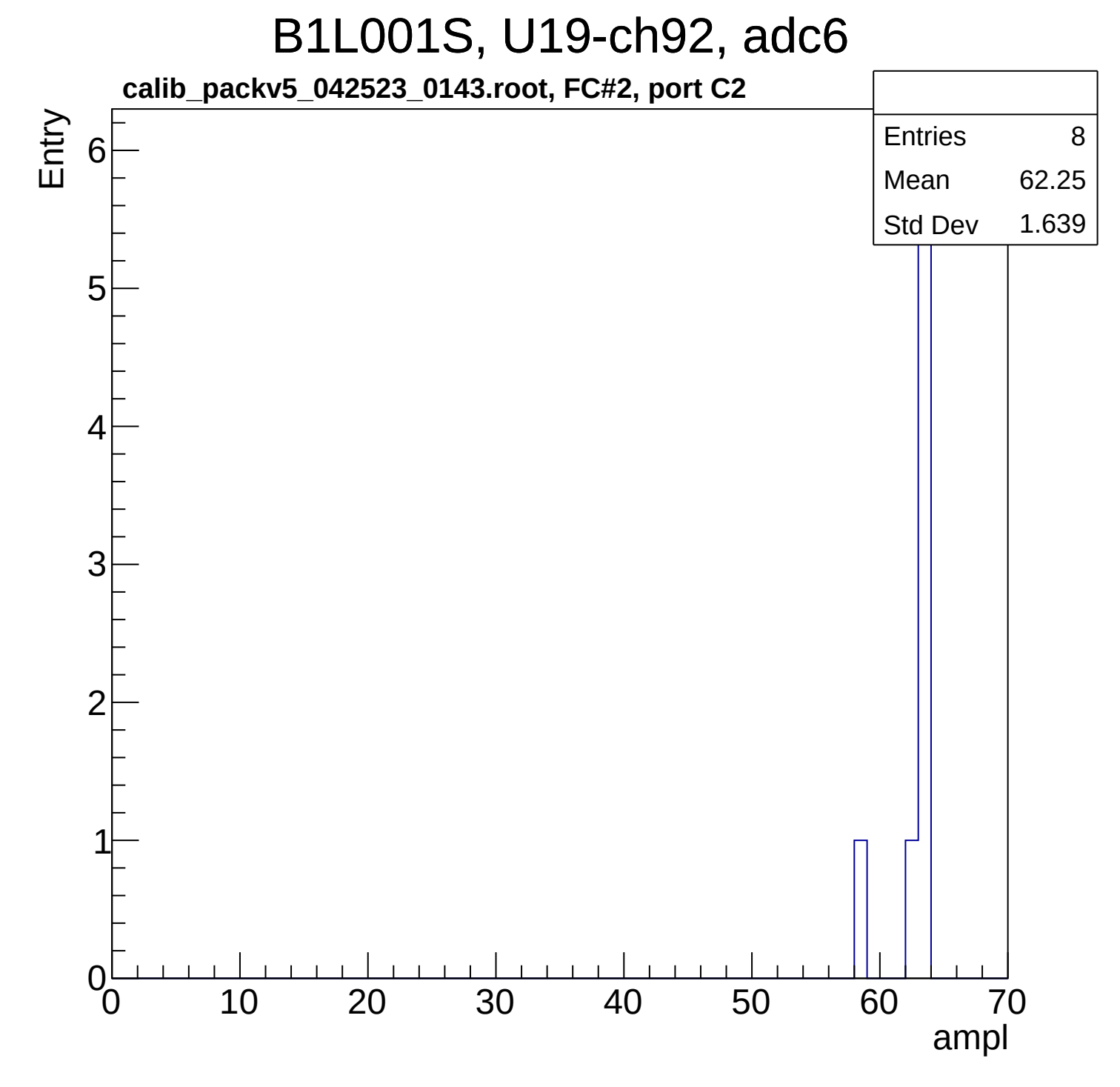
50
60
70
ampl


B1L001S, U19-ch92, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 8
Mean 62.25
Std Dev 1.639
Entry
0
1
2
3
4
5
6
0
10
20
30
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50
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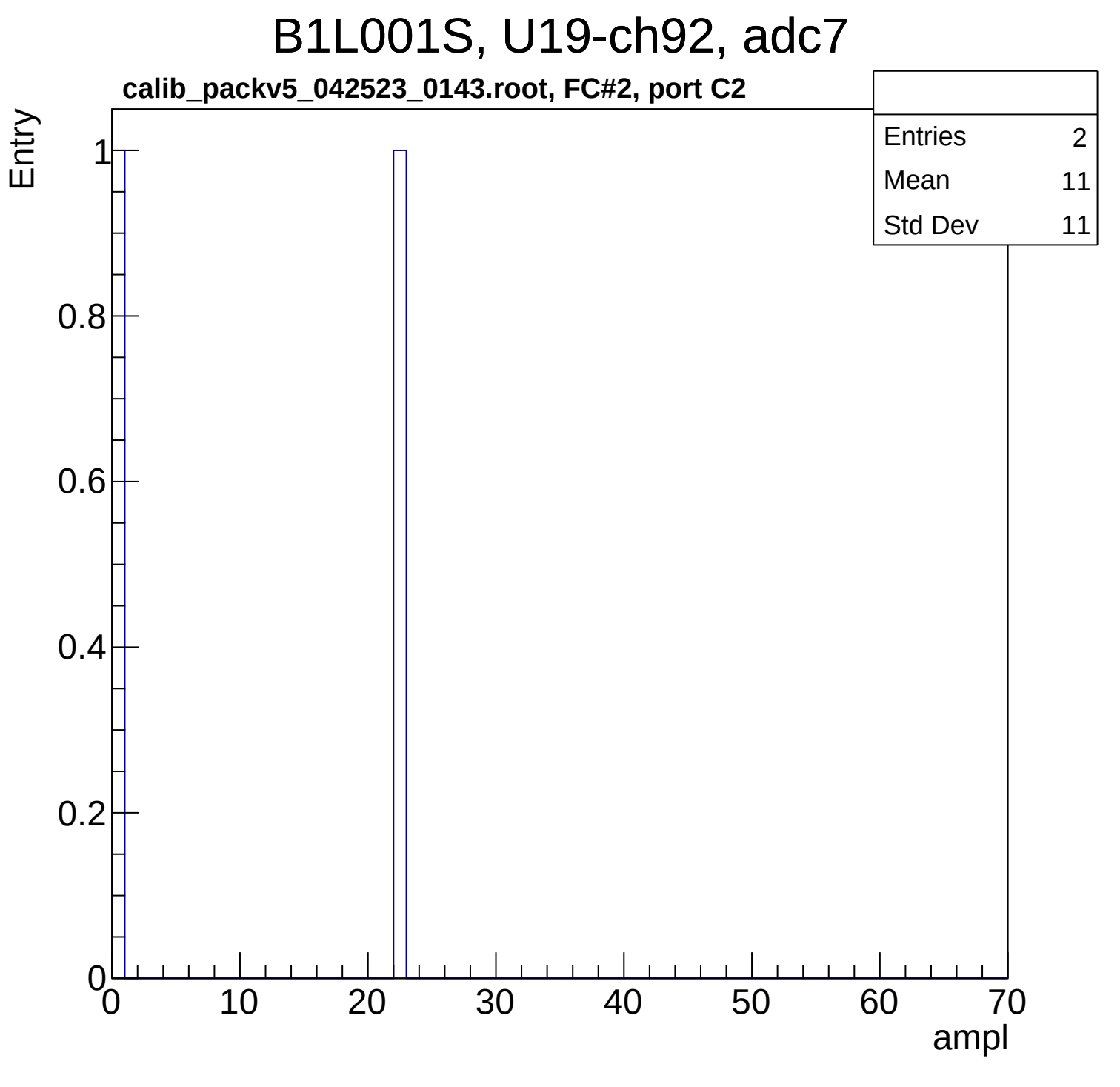
70
ampl


B1L001S, U19-ch92, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 11
Std Dev 11
Entry
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0.6
0.4
0.2
0
0
10
20
30
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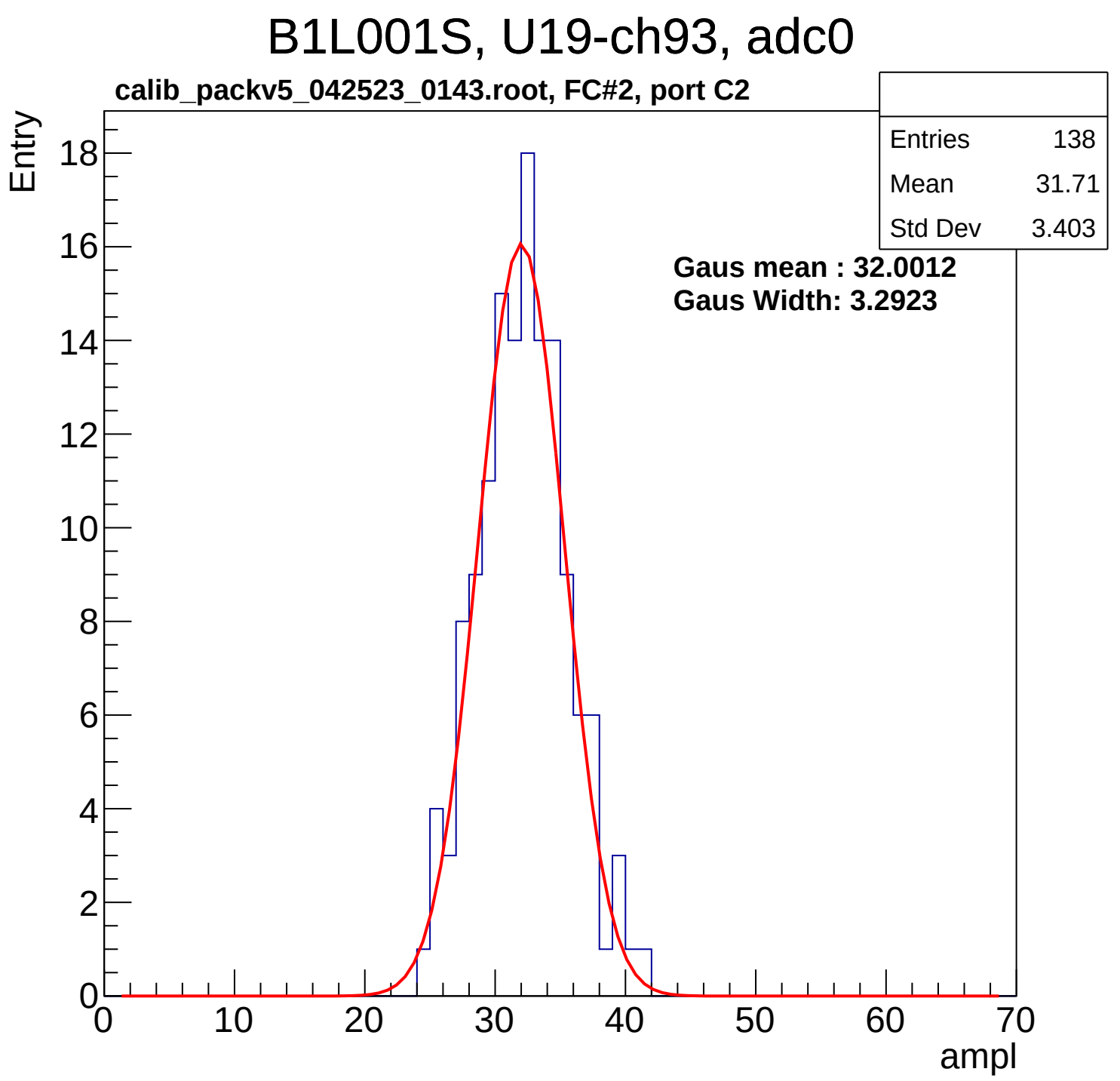
50
60
70
ampl


B1L001S, U19-ch93, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 138
Mean 31.71
Std Dev 3.403
Gaus mean : 32.0012
Gaus Width: 3.2923
Entry
ampl
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4
6
8
10
12
14
16
18
0
10
20
30
40
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60
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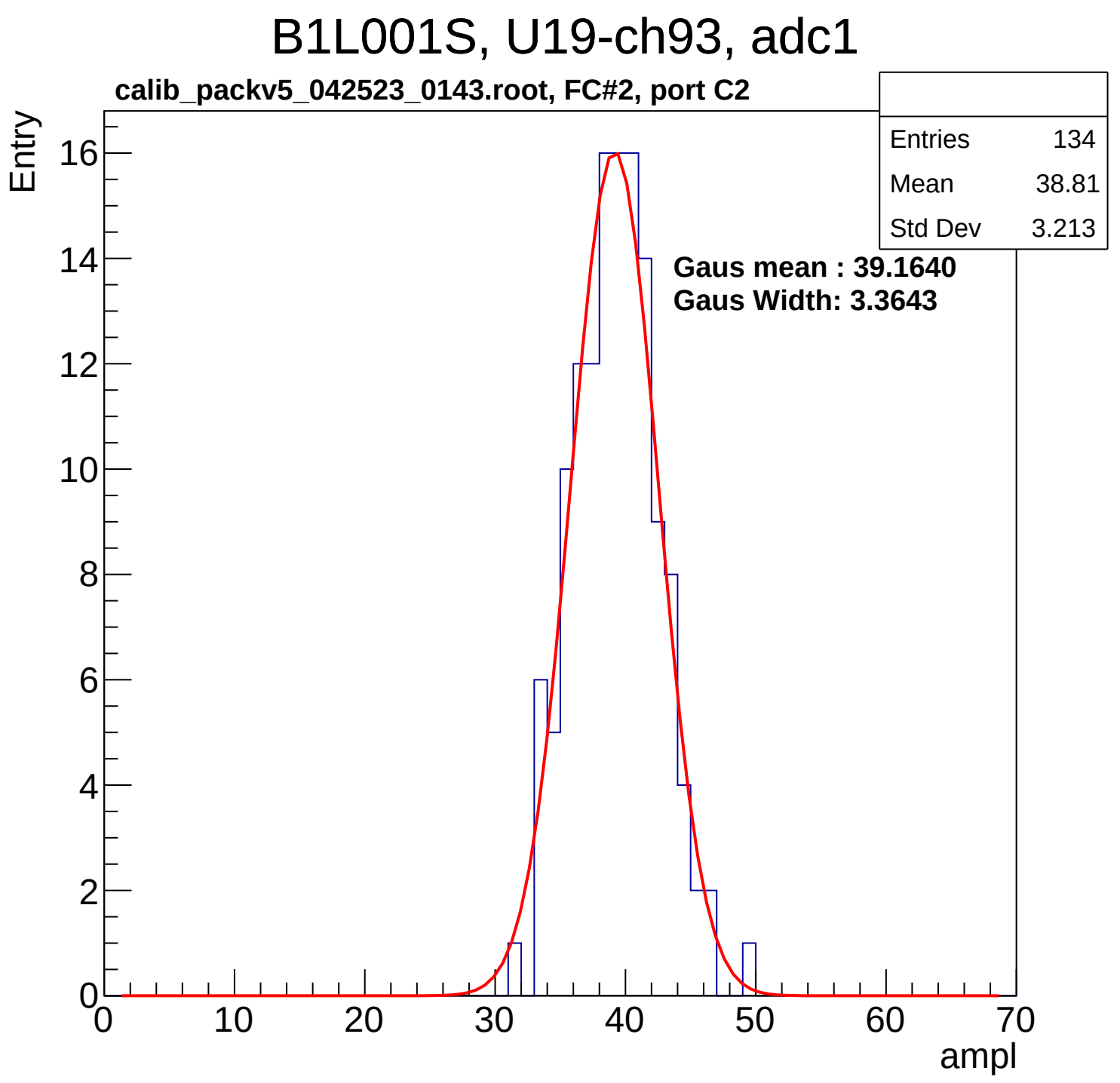
B1L001S, U19-ch93, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 134
Mean 38.81
Std Dev 3.213
Gaus mean : 39.1640
Gaus Width: 3.3643
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
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60
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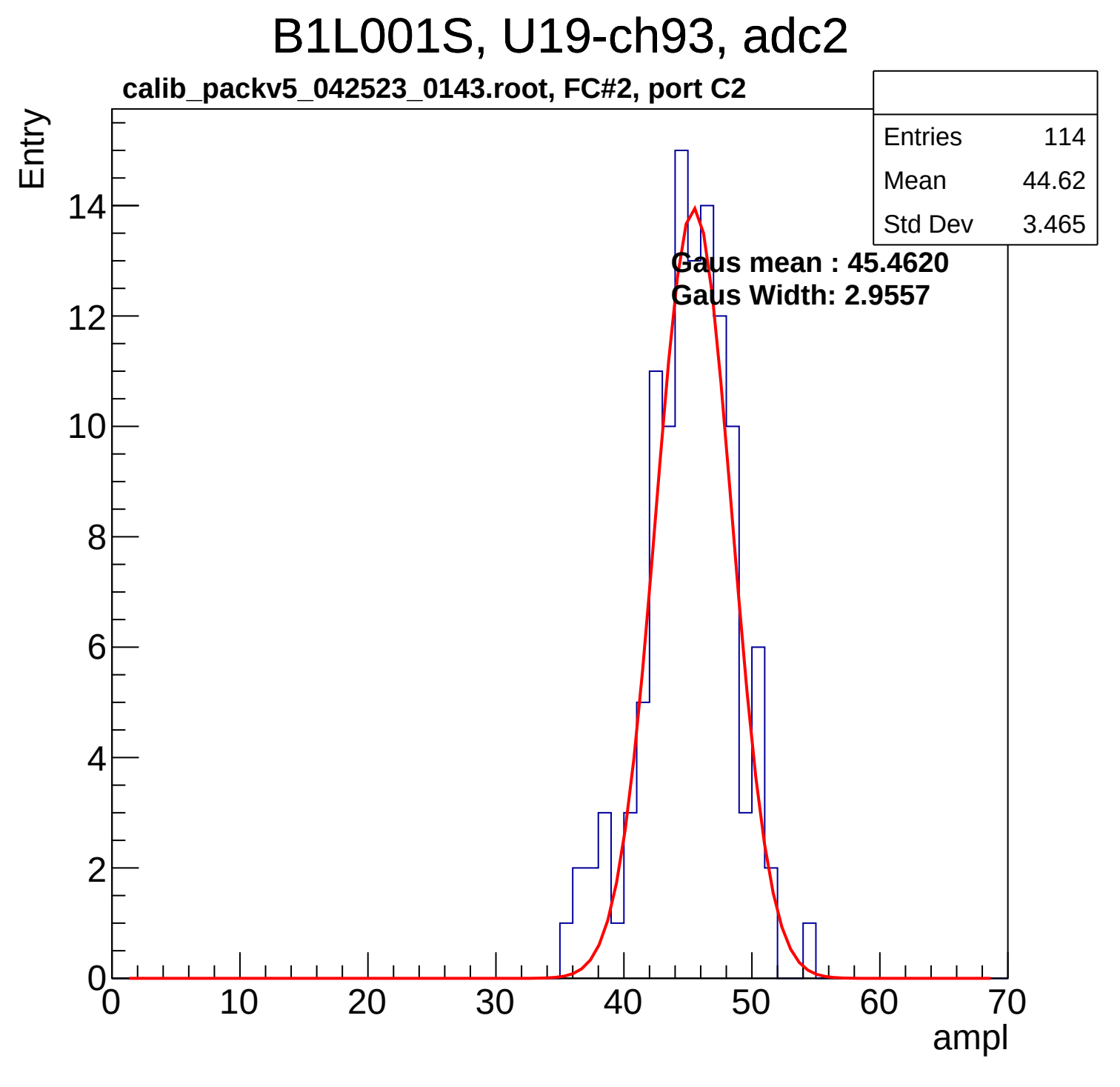
B1L001S, U19-ch93, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 114
Mean 44.62
Std Dev 3.465
Gaus mean : 45.4620
Gaus Width: 2.9557
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
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60
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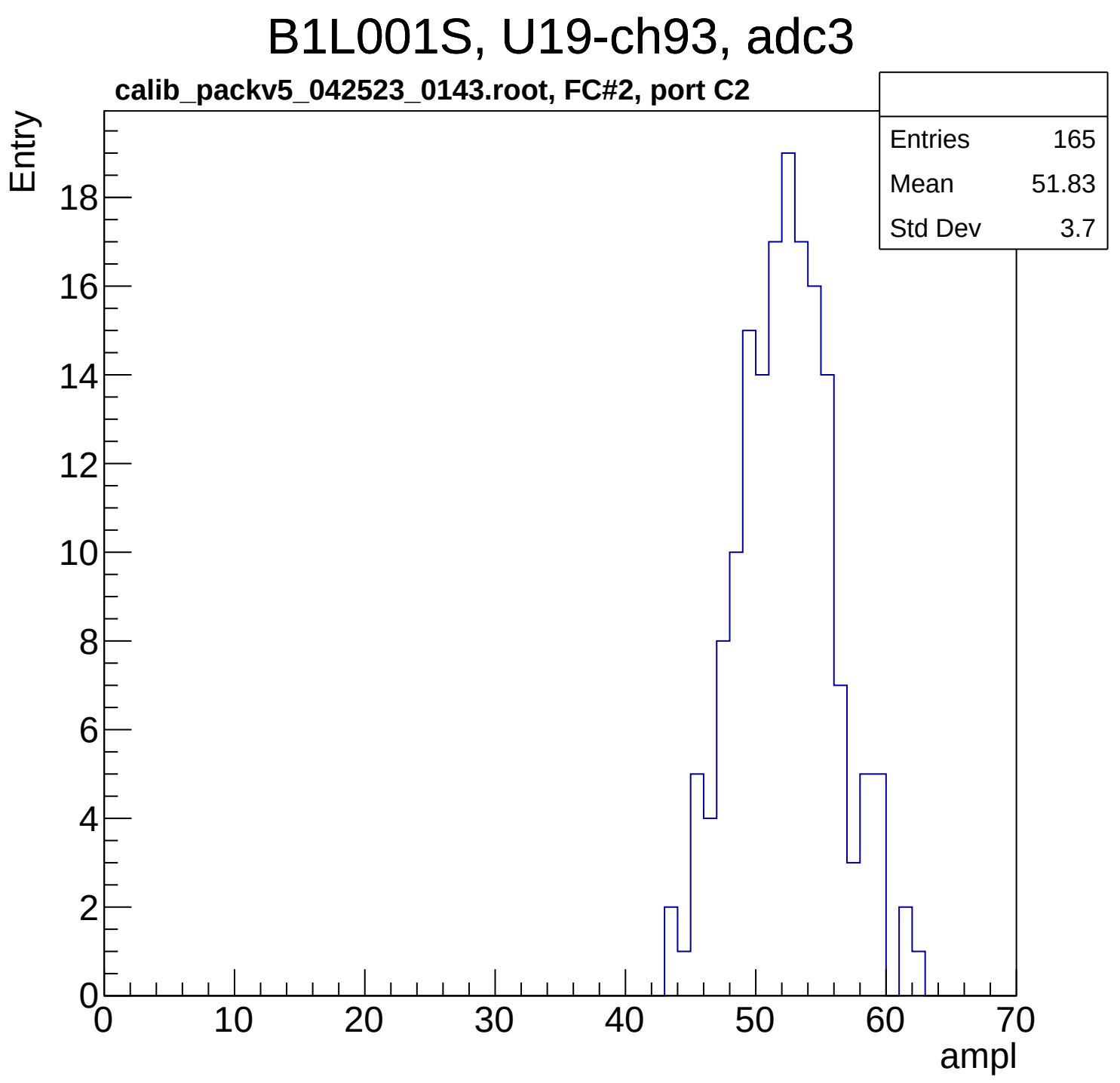
B1L001S, U19-ch93, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 165
Mean 51.83
Std Dev 3.7
Entry
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6
8
10
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14
16
18
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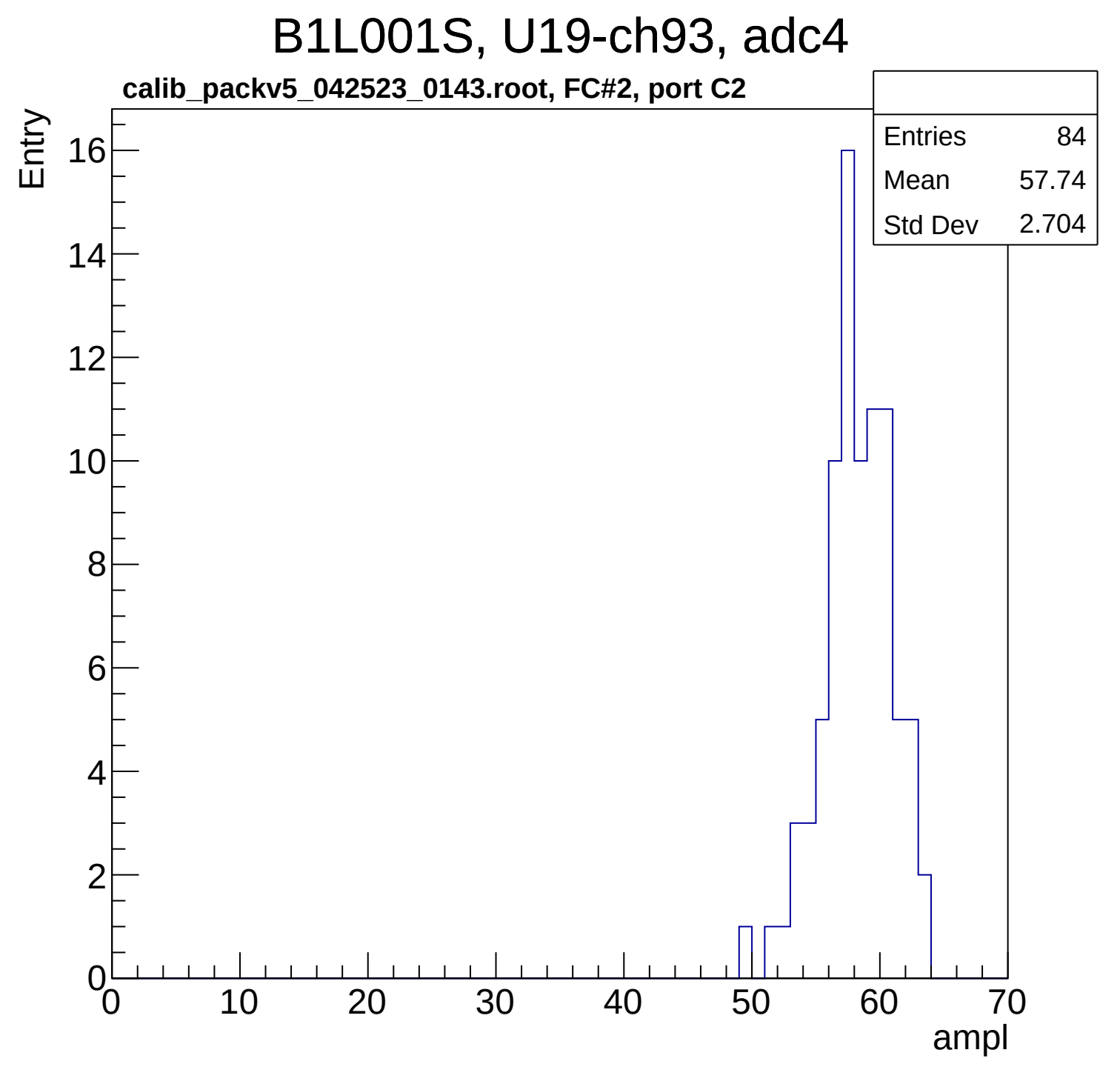
70
ampl


B1L001S, U19-ch93, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 84
Mean 57.74
Std Dev 2.704
Entry
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10
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16
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10
20
30
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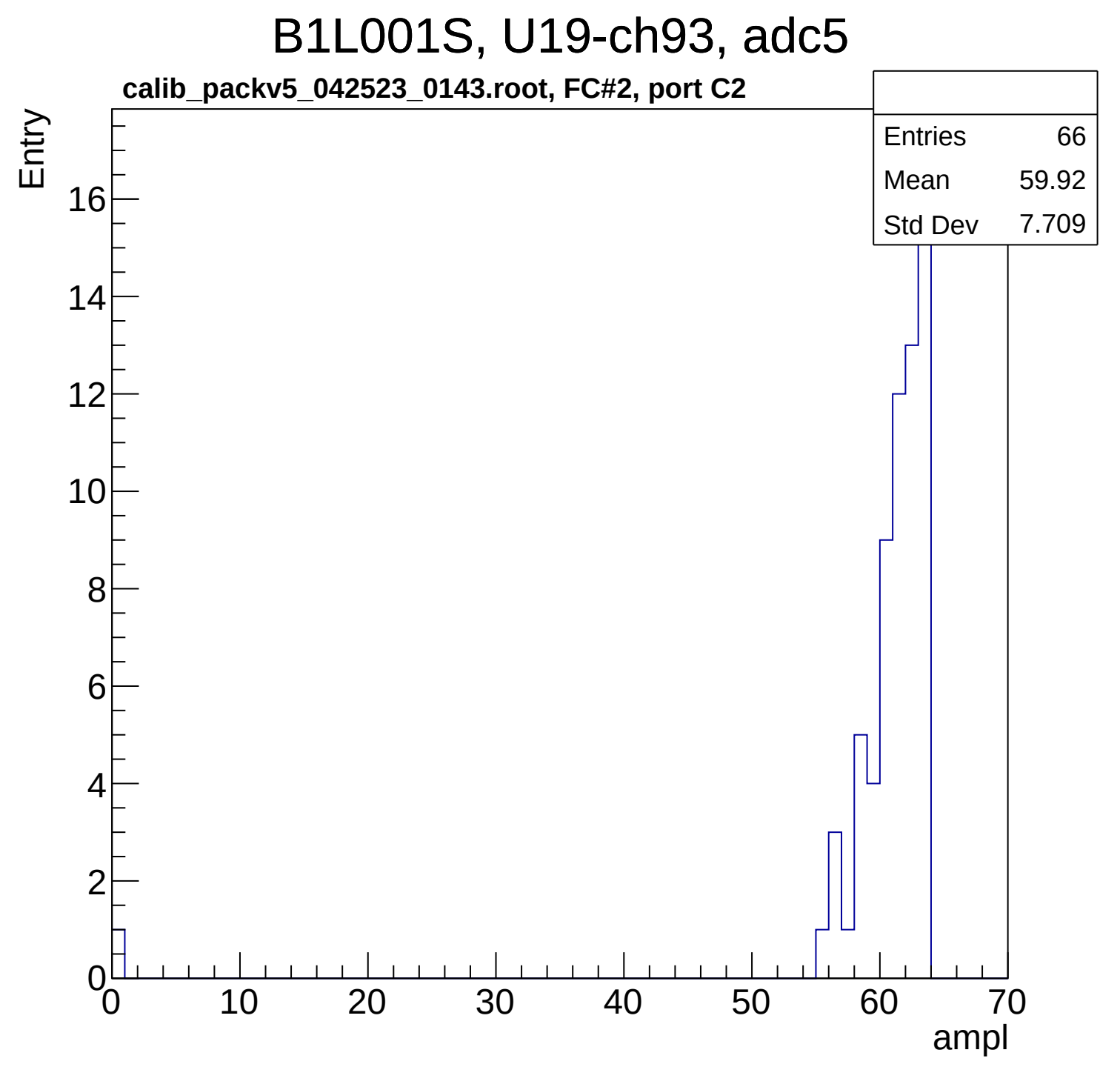
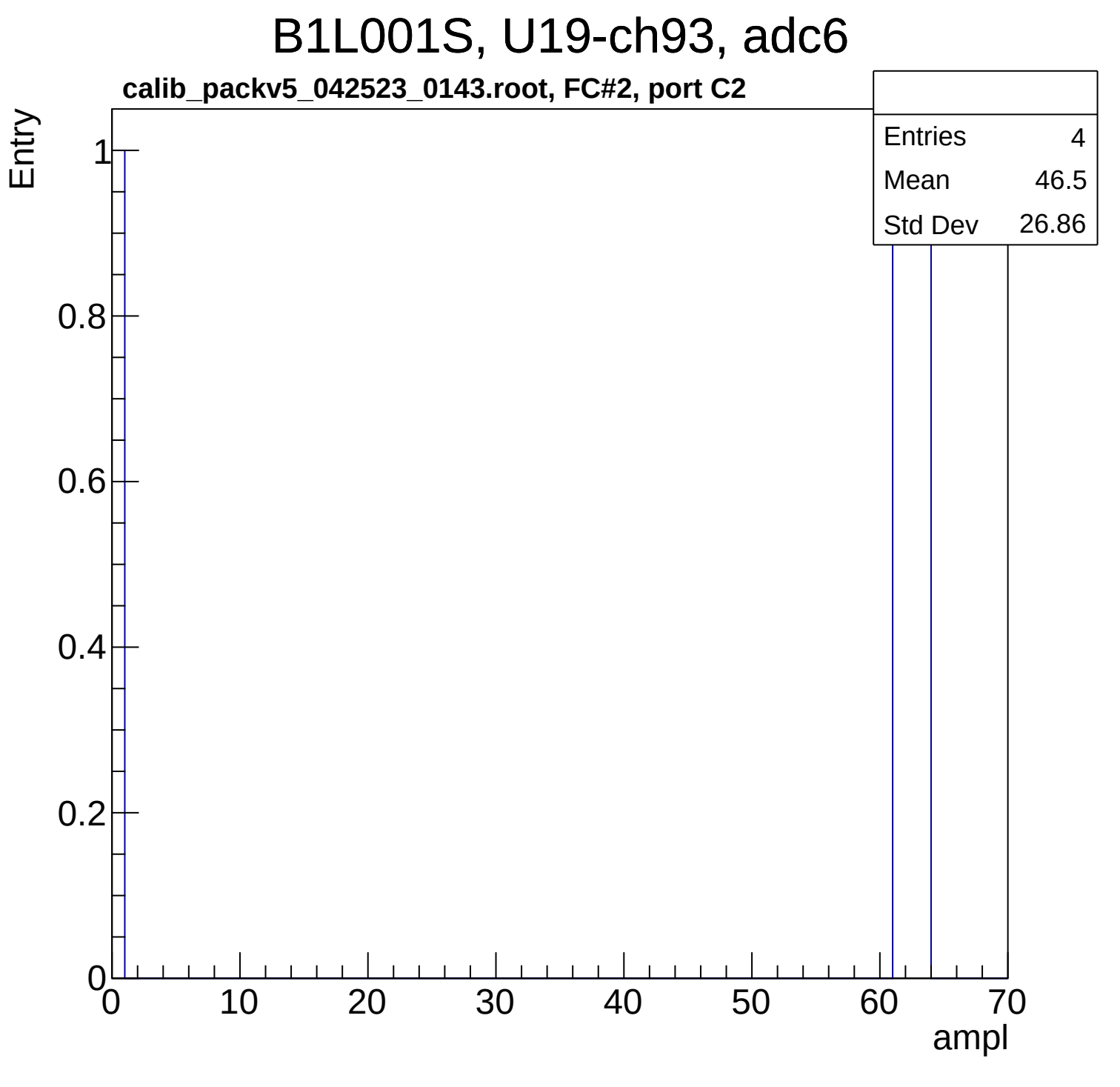
50
60
70
ampl


B1L001S, U19-ch93, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 66
Mean 59.92
Std Dev 7.709
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70


B1L001S, U19-ch93, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 4
Mean 46.5
Std Dev 26.86
Entry
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0.6
0.4
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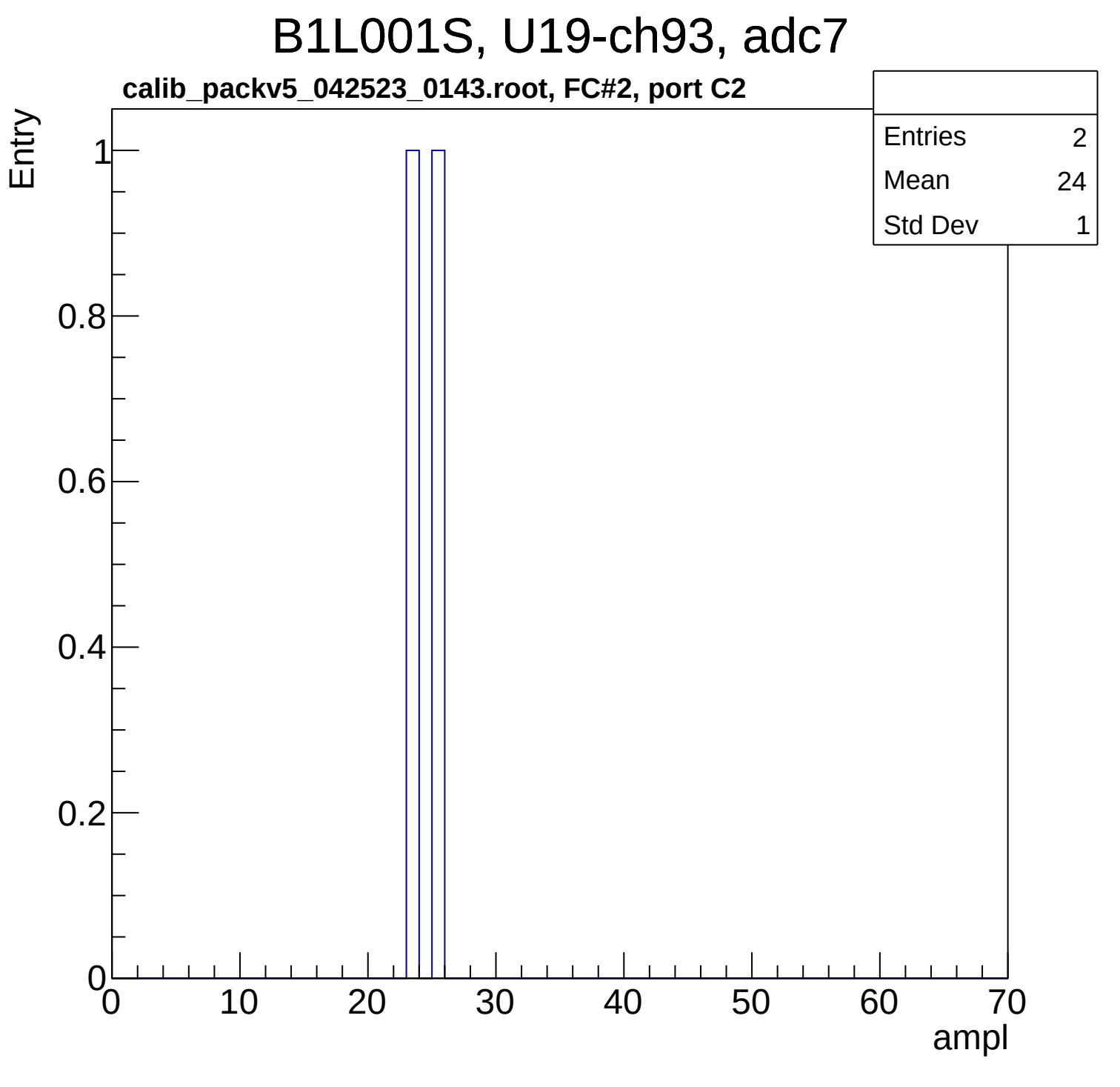
ampl


B1L001S, U19-ch93, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 24
Std Dev 1
Entry
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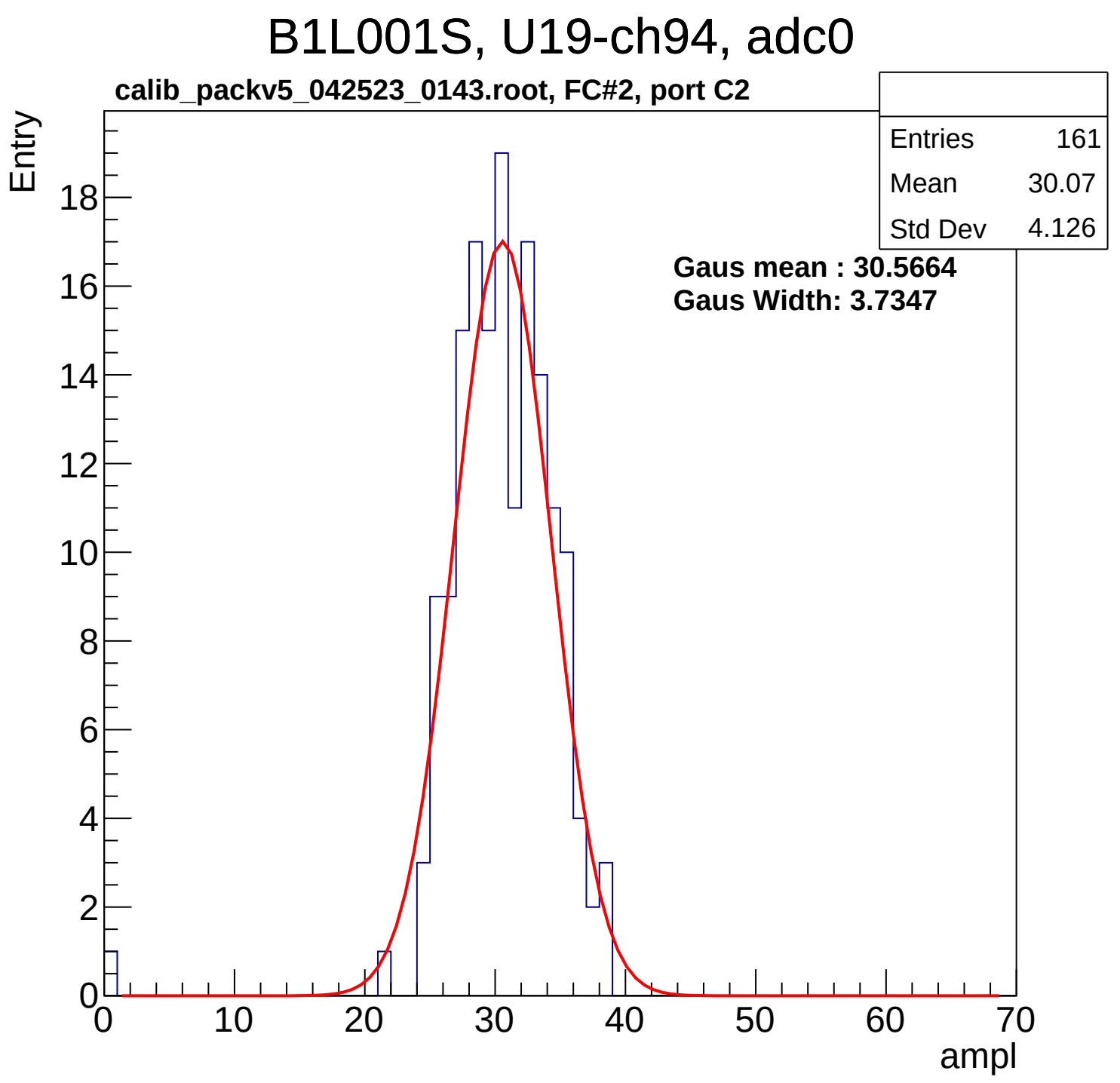
ampl


B1L001S, U19-ch94, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 161
Mean 30.07
Std Dev 4.126
Gaus mean : 30.5664
Gaus Width: 3.7347
Entry
ampl
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4
6
8
10
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14
16
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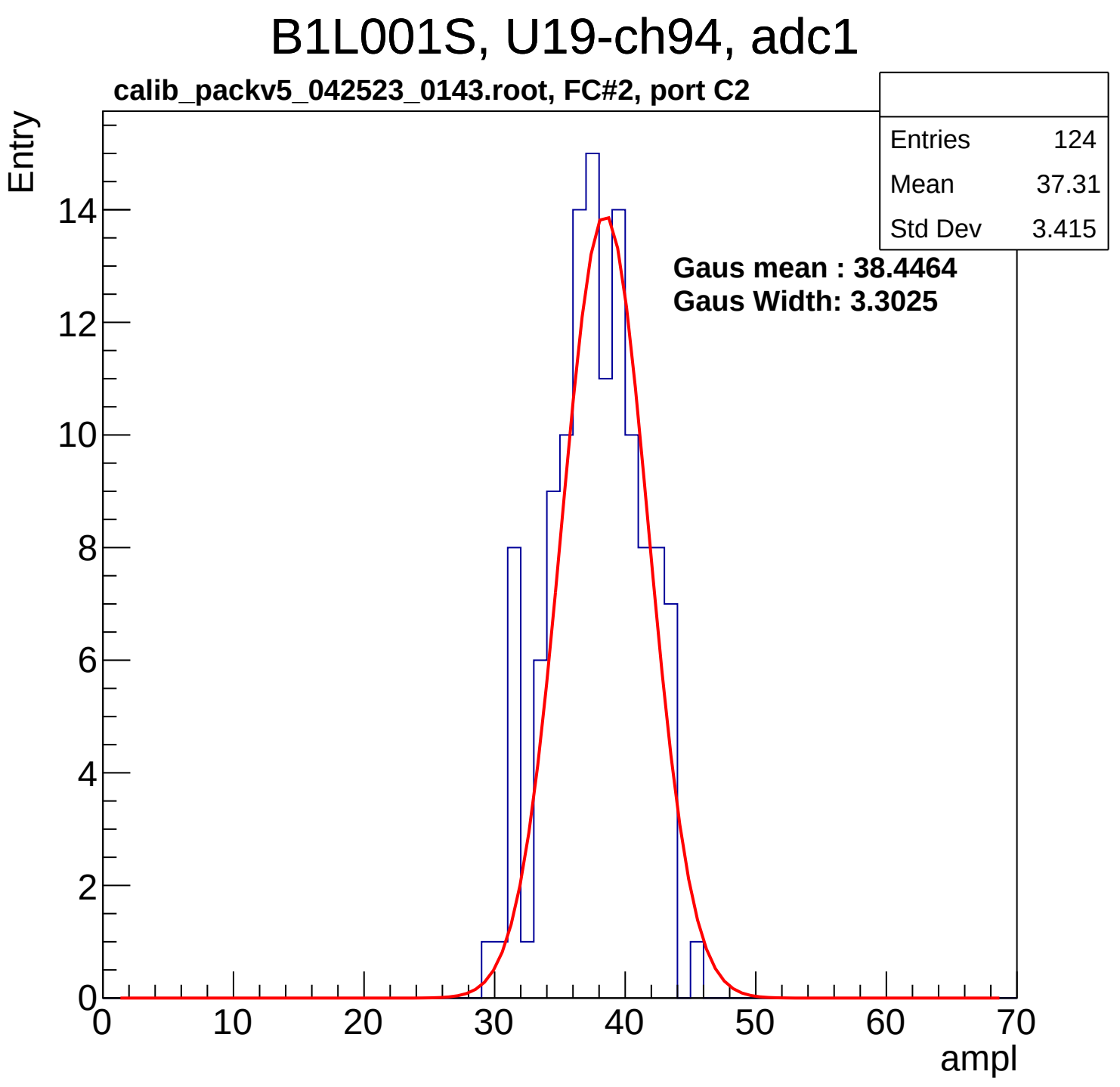
B1L001S, U19-ch94, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 124
Mean 37.31
Std Dev 3.415
Gaus mean : 38.4464
Gaus Width: 3.3025
Entry
ampl
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2
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8
10
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0
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40
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60
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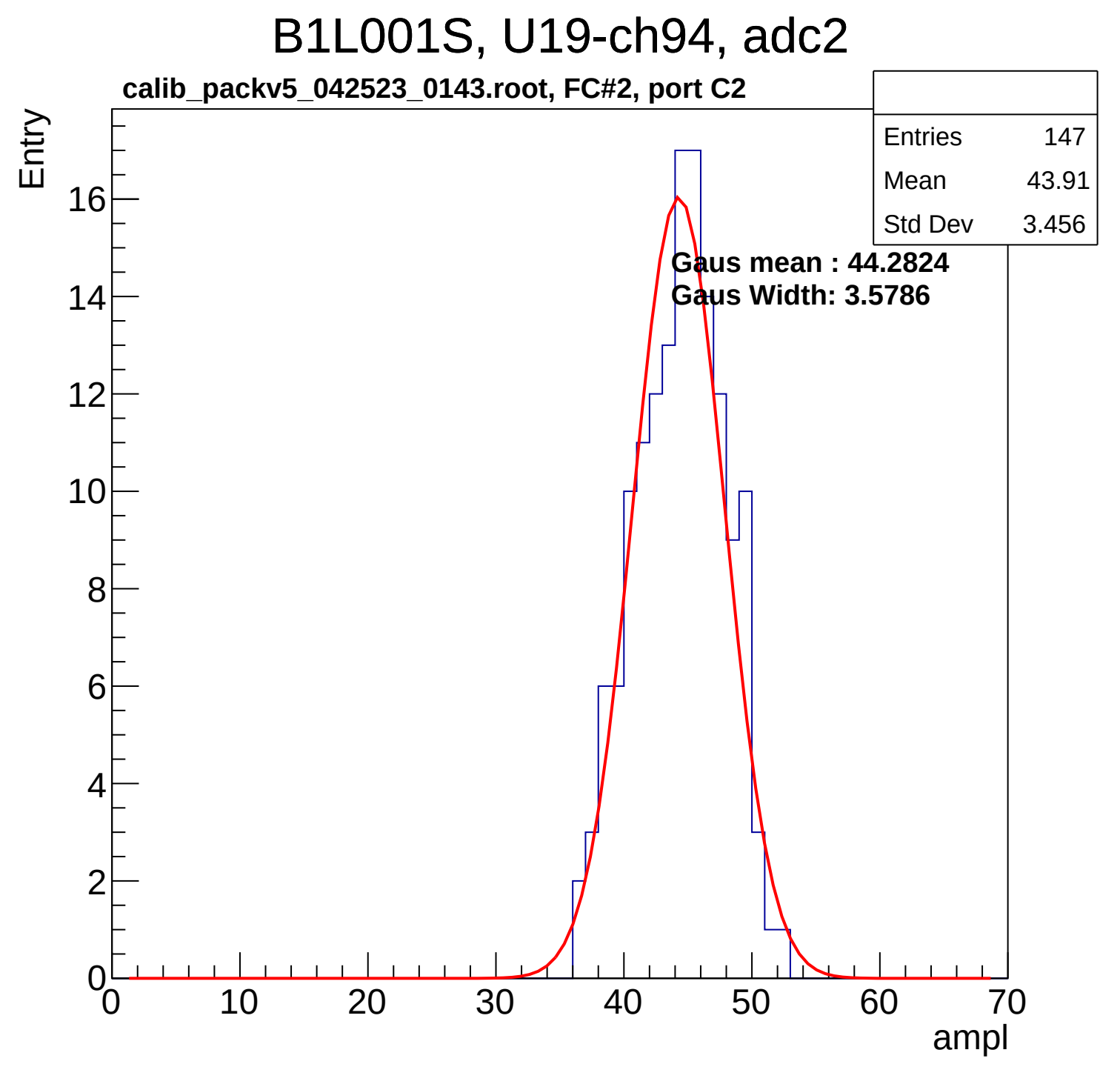
B1L001S, U19-ch94, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 147
Mean 43.91
Std Dev 3.456
Gaus mean : 44.2824
Gaus Width: 3.5786
Entry
ampl
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2
4
6
8
10
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14
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0
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40
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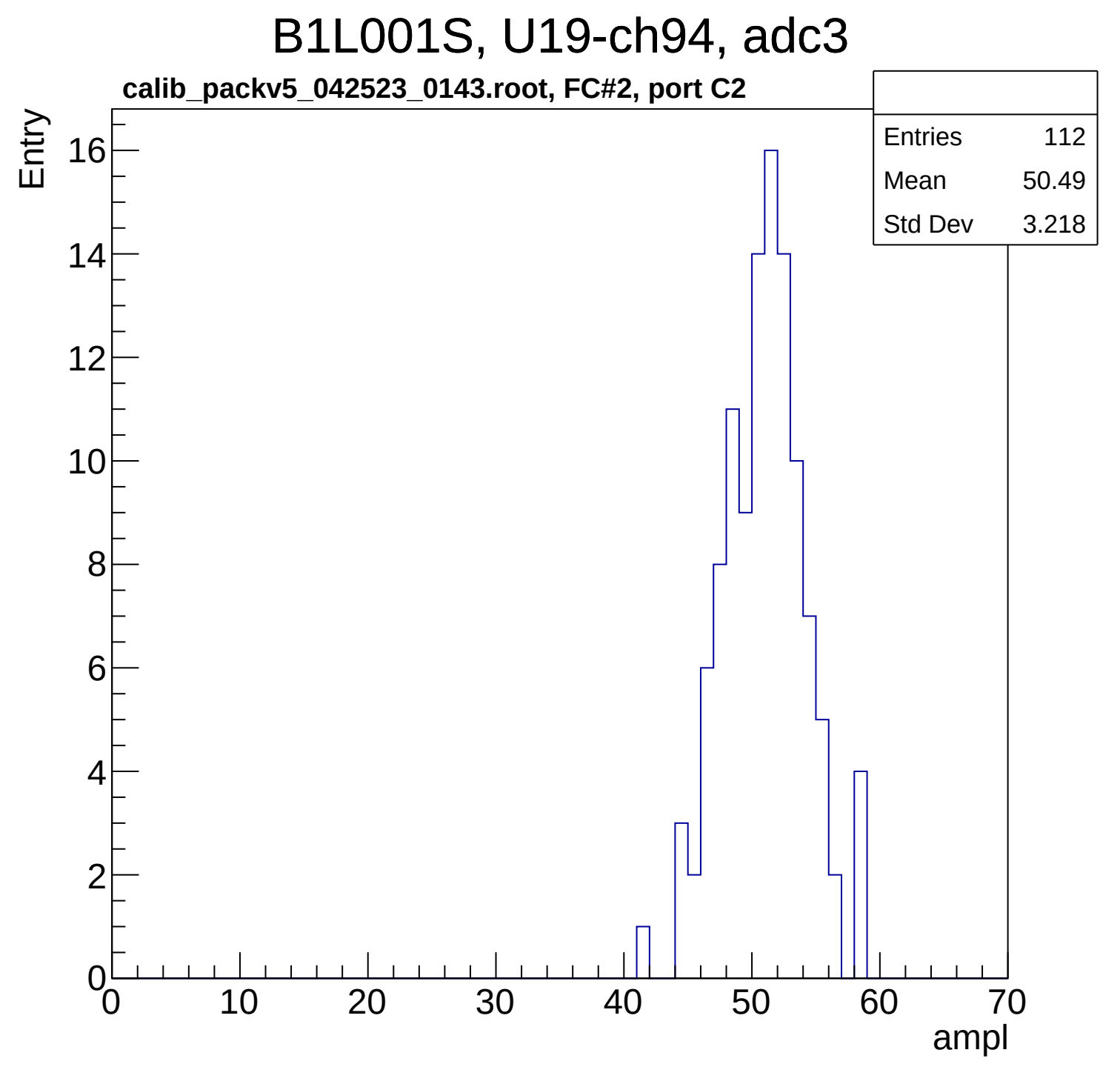
B1L001S, U19-ch94, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 112
Mean 50.49
Std Dev 3.218
Entry
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2
4
6
8
10
12
14
16
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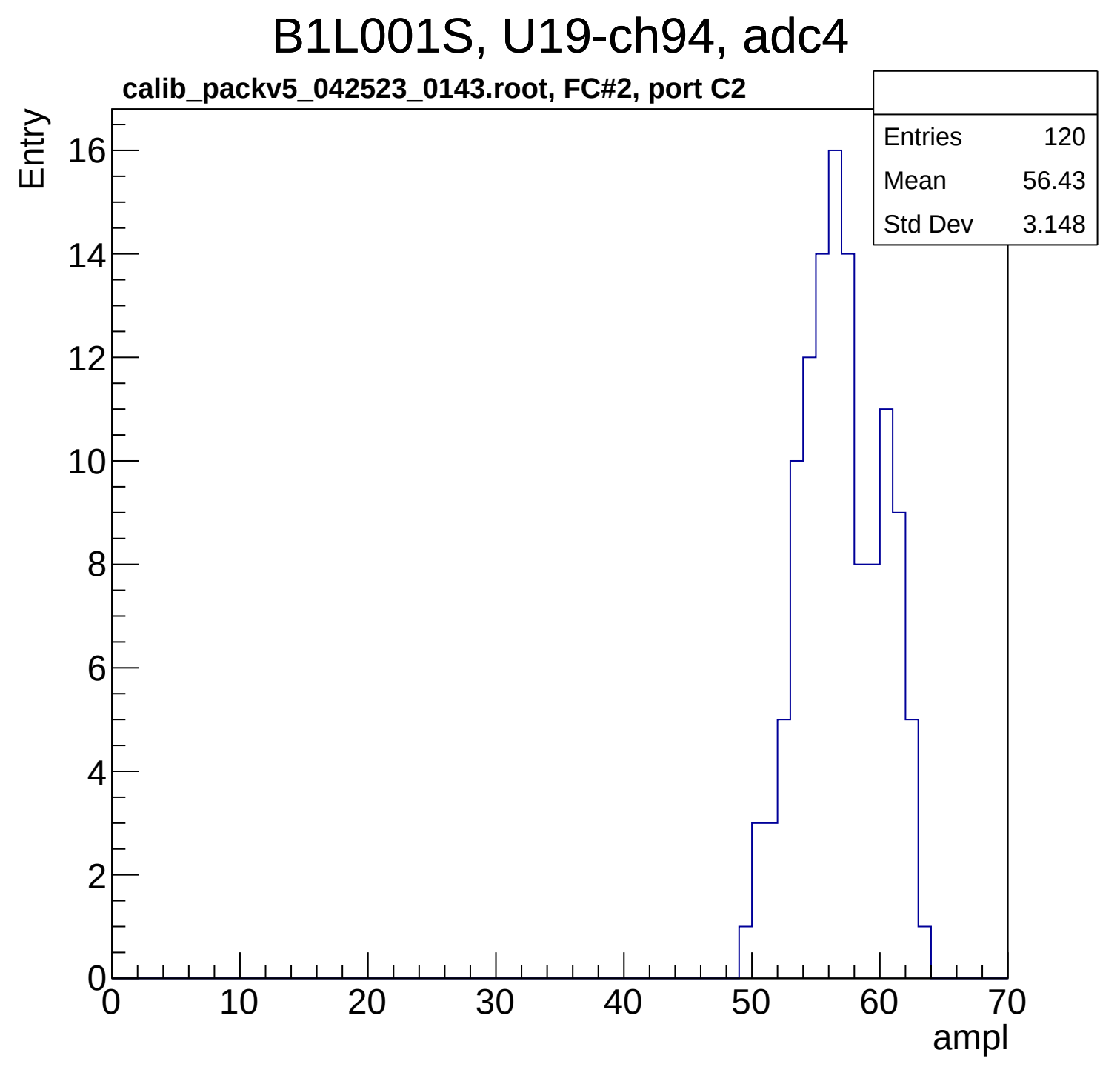
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch94, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 120
Mean 56.43
Std Dev 3.148
Entry
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2
4
6
8
10
12
14
16
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10
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50
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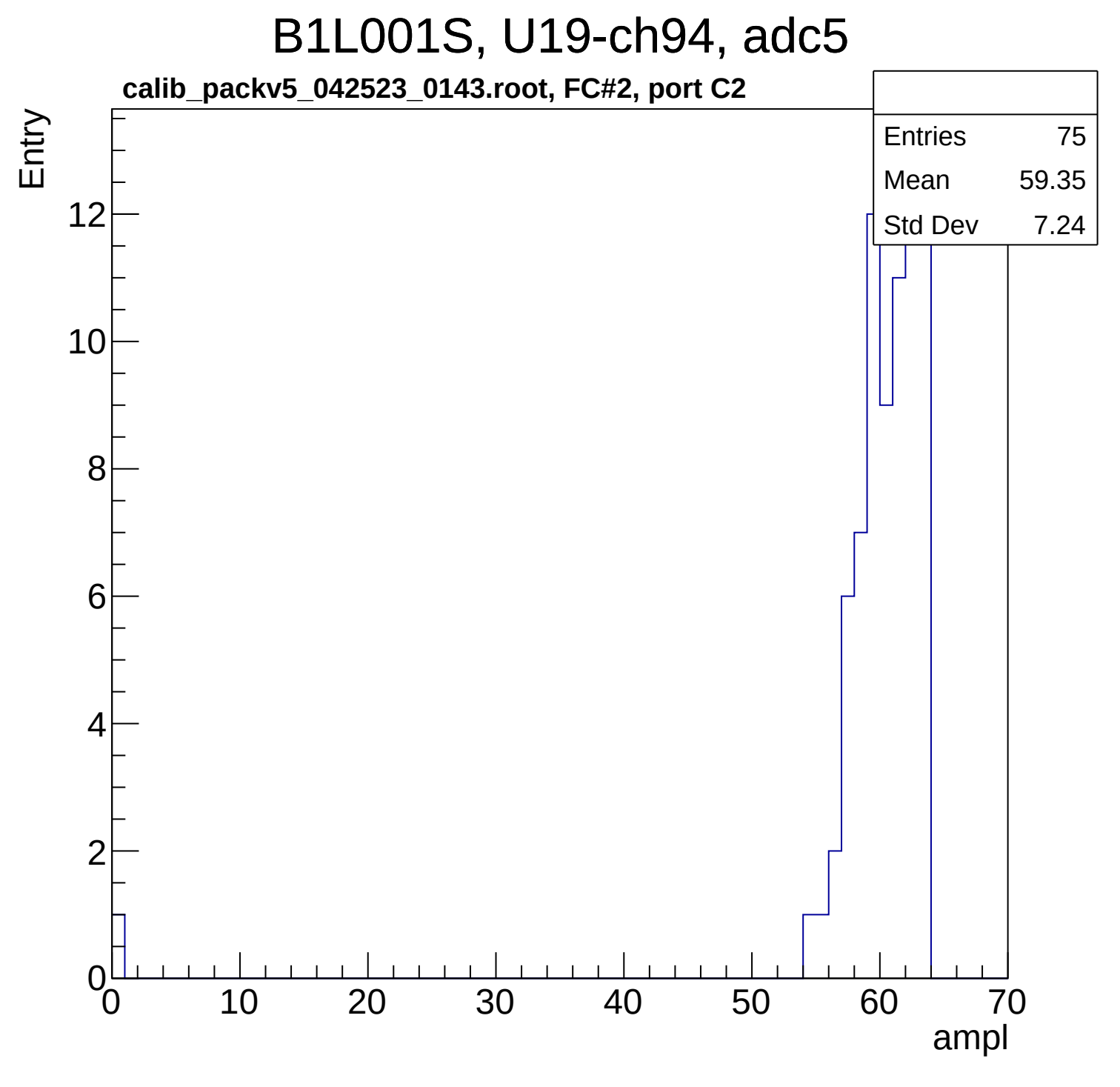
70
ampl


B1L001S, U19-ch94, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 75
Mean 59.35
Std Dev 7.24
Entry
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8
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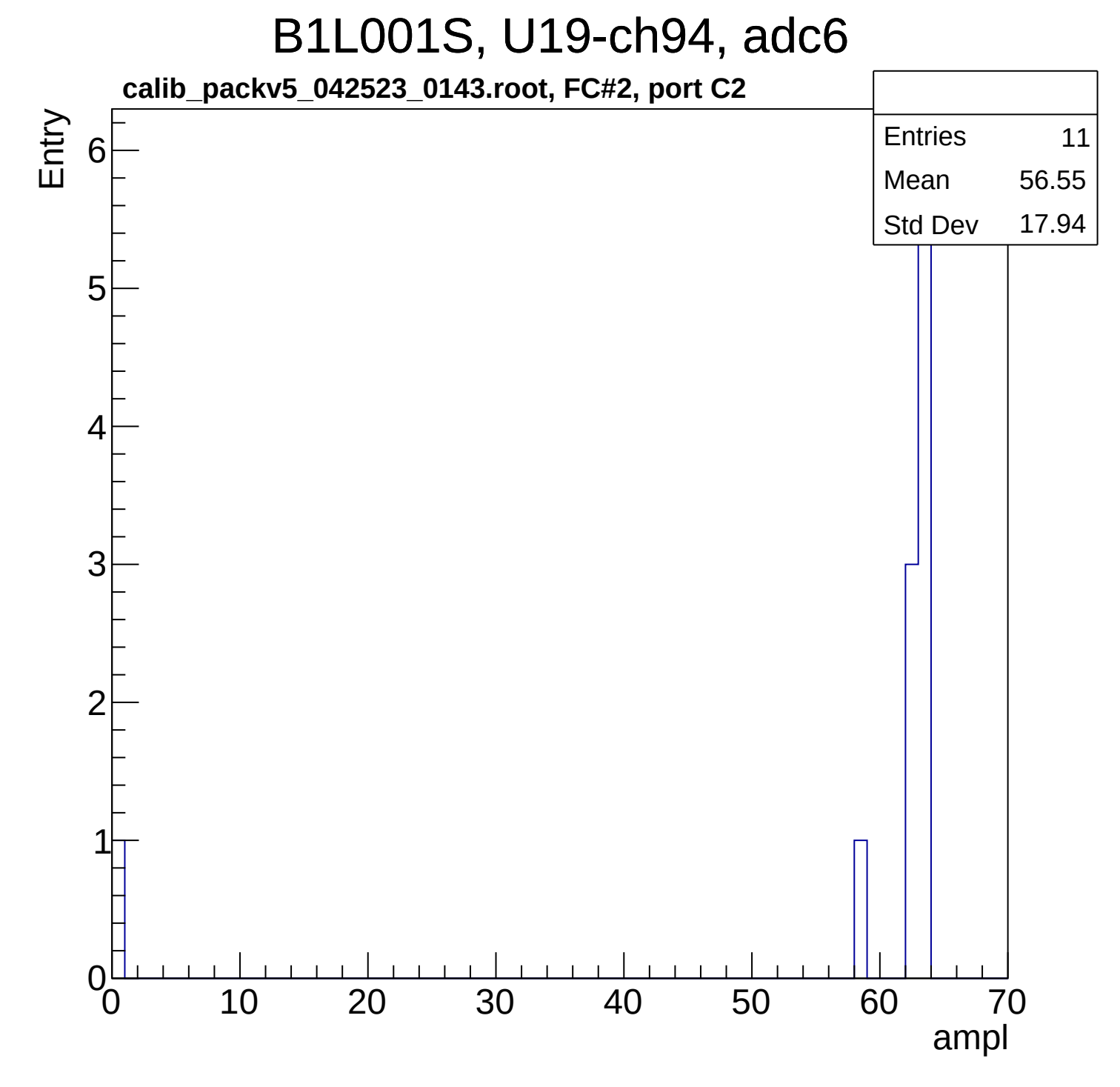
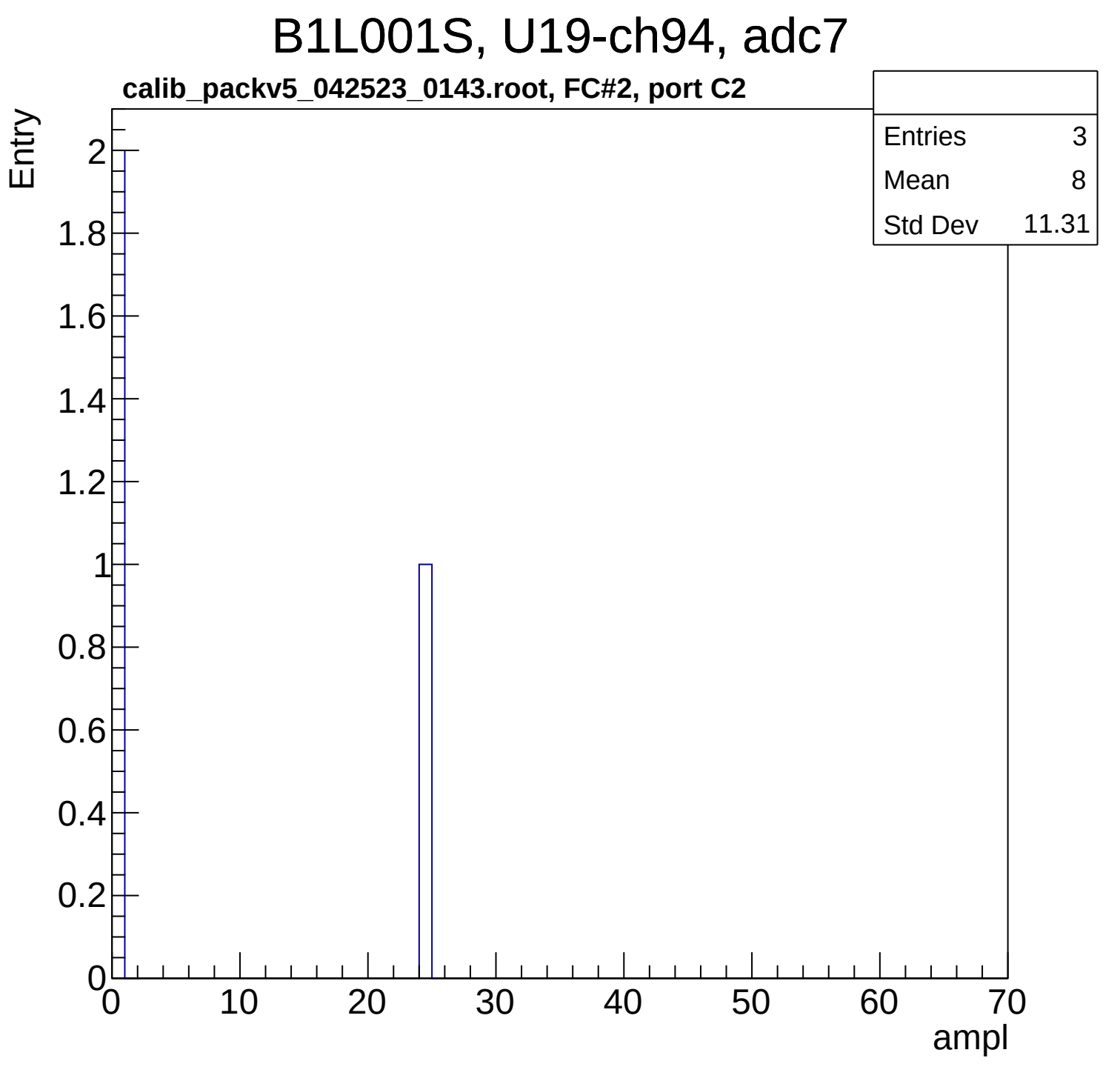
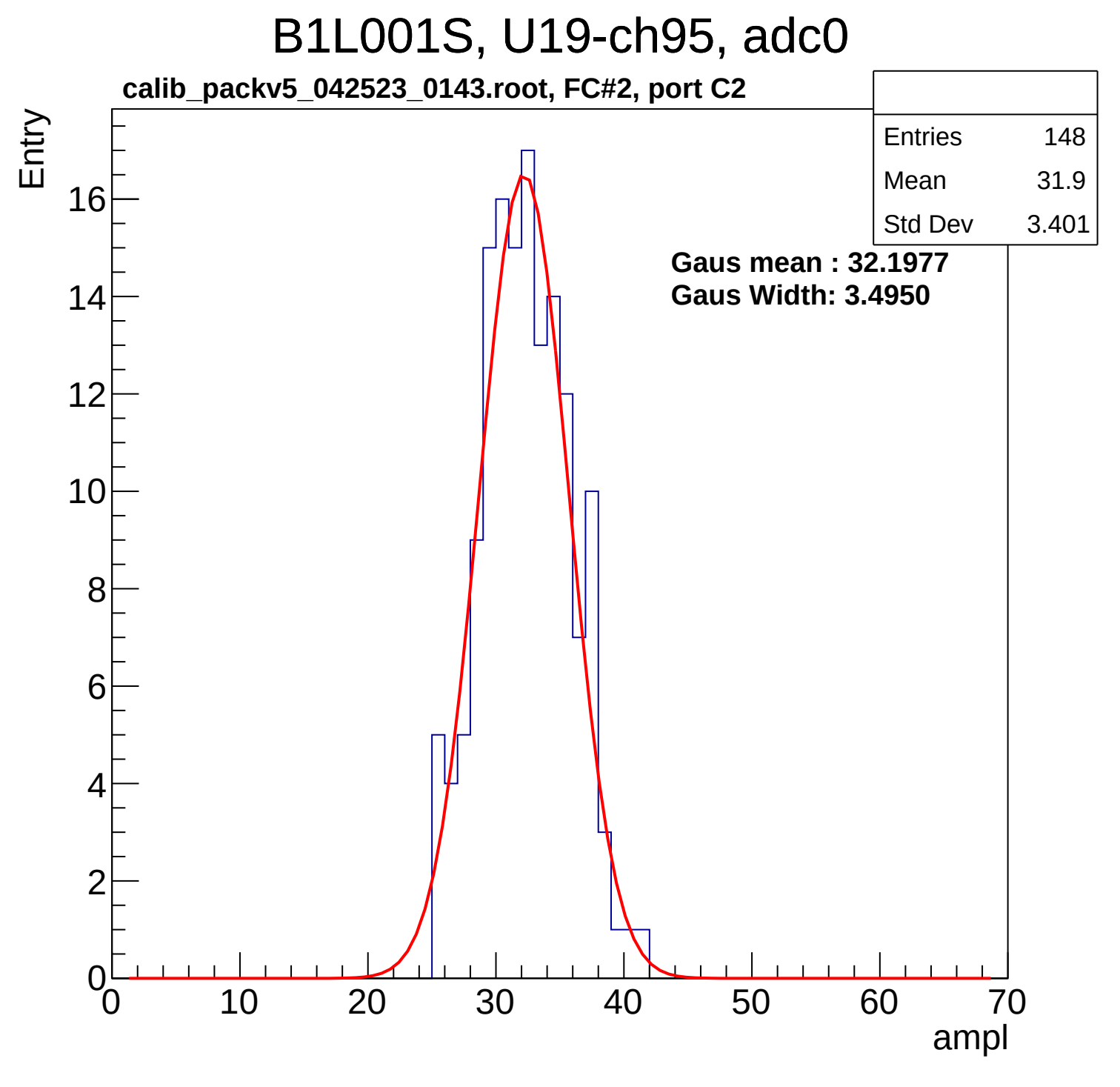
70
ampl


B1L001S, U19-ch94, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 11
Mean 56.55
Std Dev 17.94
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch94, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 3
Mean 8
Std Dev 11.31
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L001S, U19-ch95, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 148
Mean 31.9
Std Dev 3.401
Gaus mean : 32.1977
Gaus Width: 3.4950
Entry
ampl
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2
4
6
8
10
12
14
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0
10
20
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40
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60
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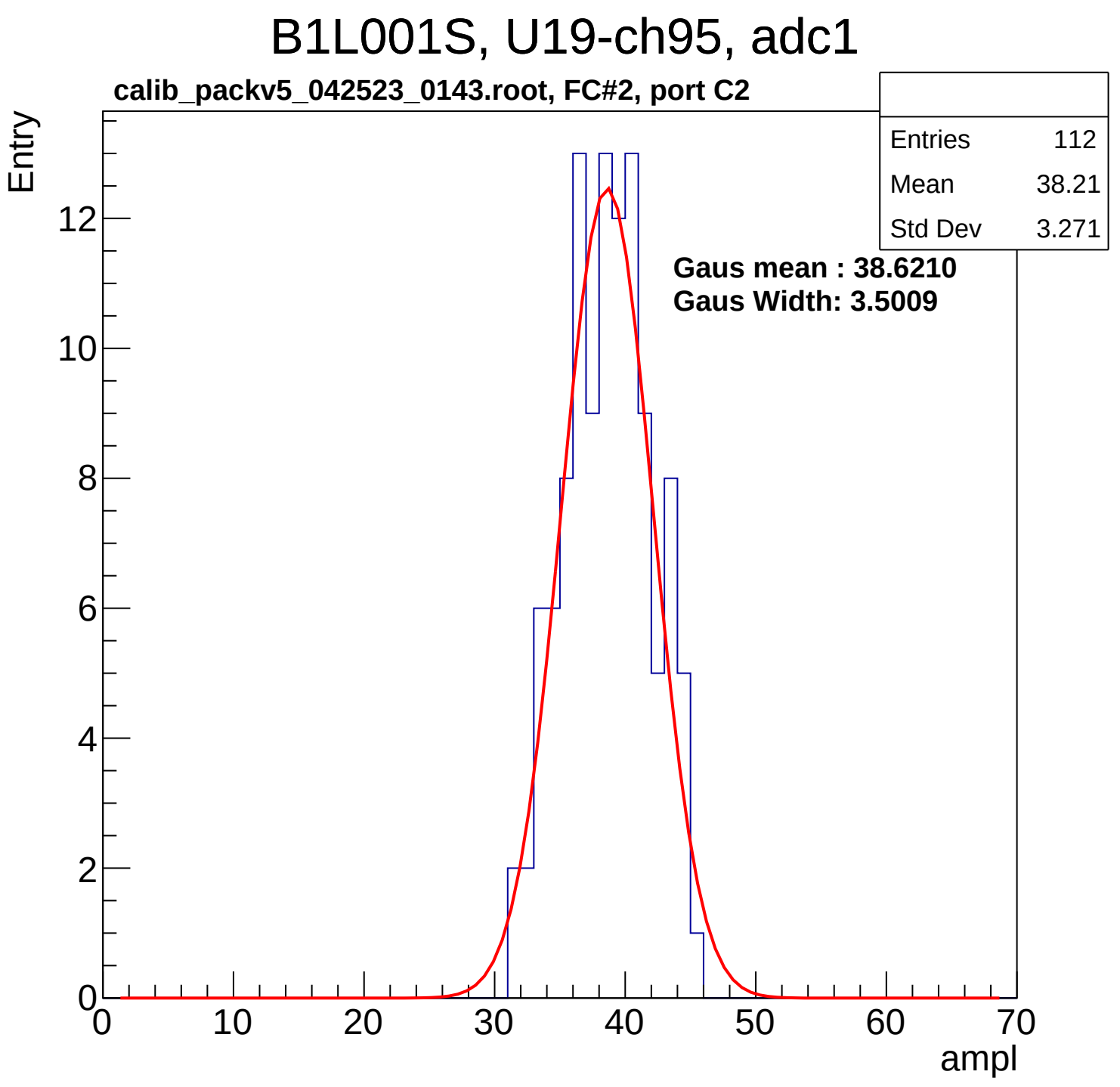
B1L001S, U19-ch95, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 112
Mean 38.21
Std Dev 3.271
Gaus mean : 38.6210
Gaus Width: 3.5009
Entry
ampl
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2
4
6
8
10
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0
10
20
30
40
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60
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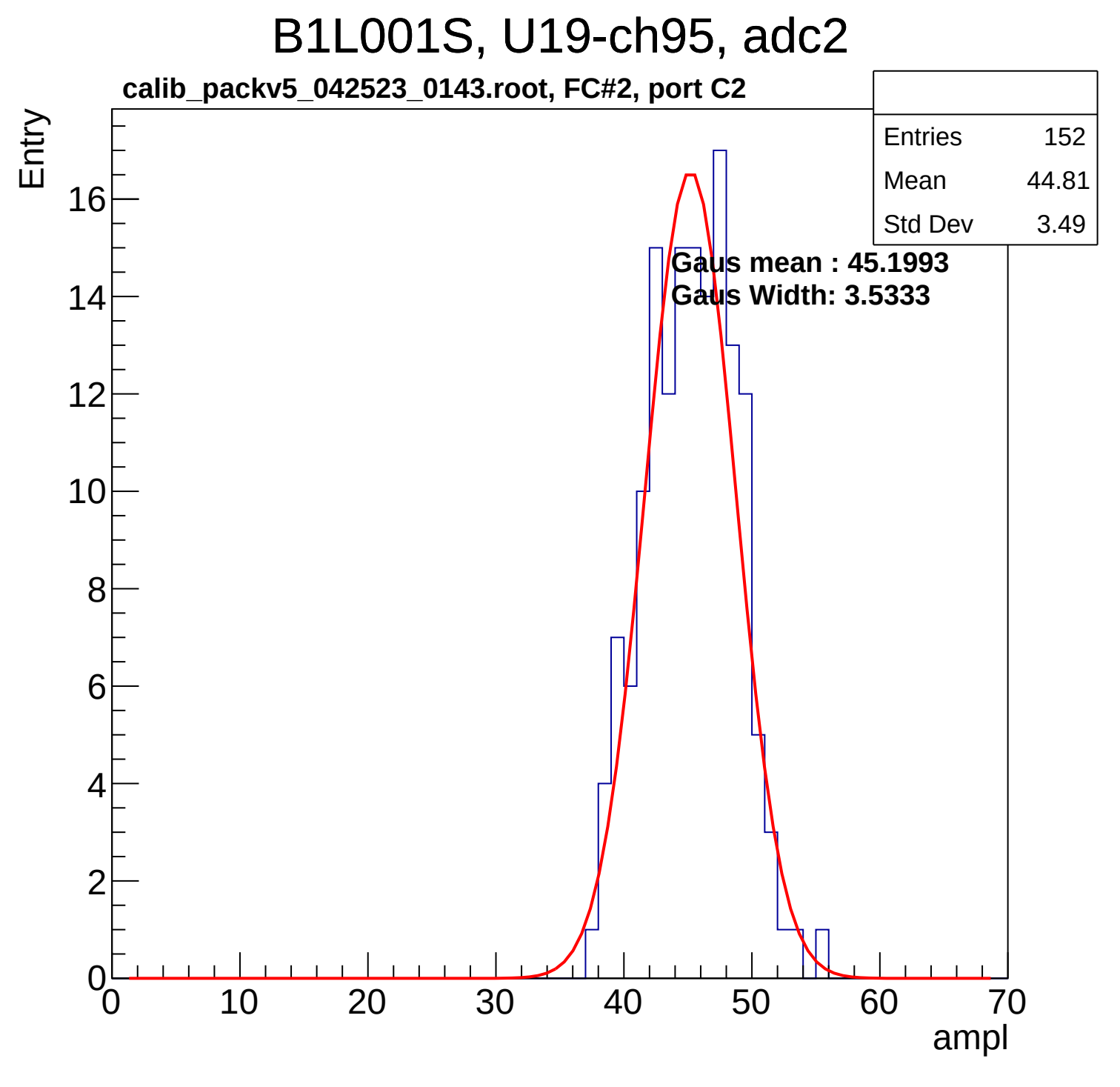
B1L001S, U19-ch95, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 152
Mean 44.81
Std Dev 3.49
Gaus mean : 45.1993
Gaus Width: 3.5333
Entry
ampl
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4
6
8
10
12
14
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0
10
20
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40
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60
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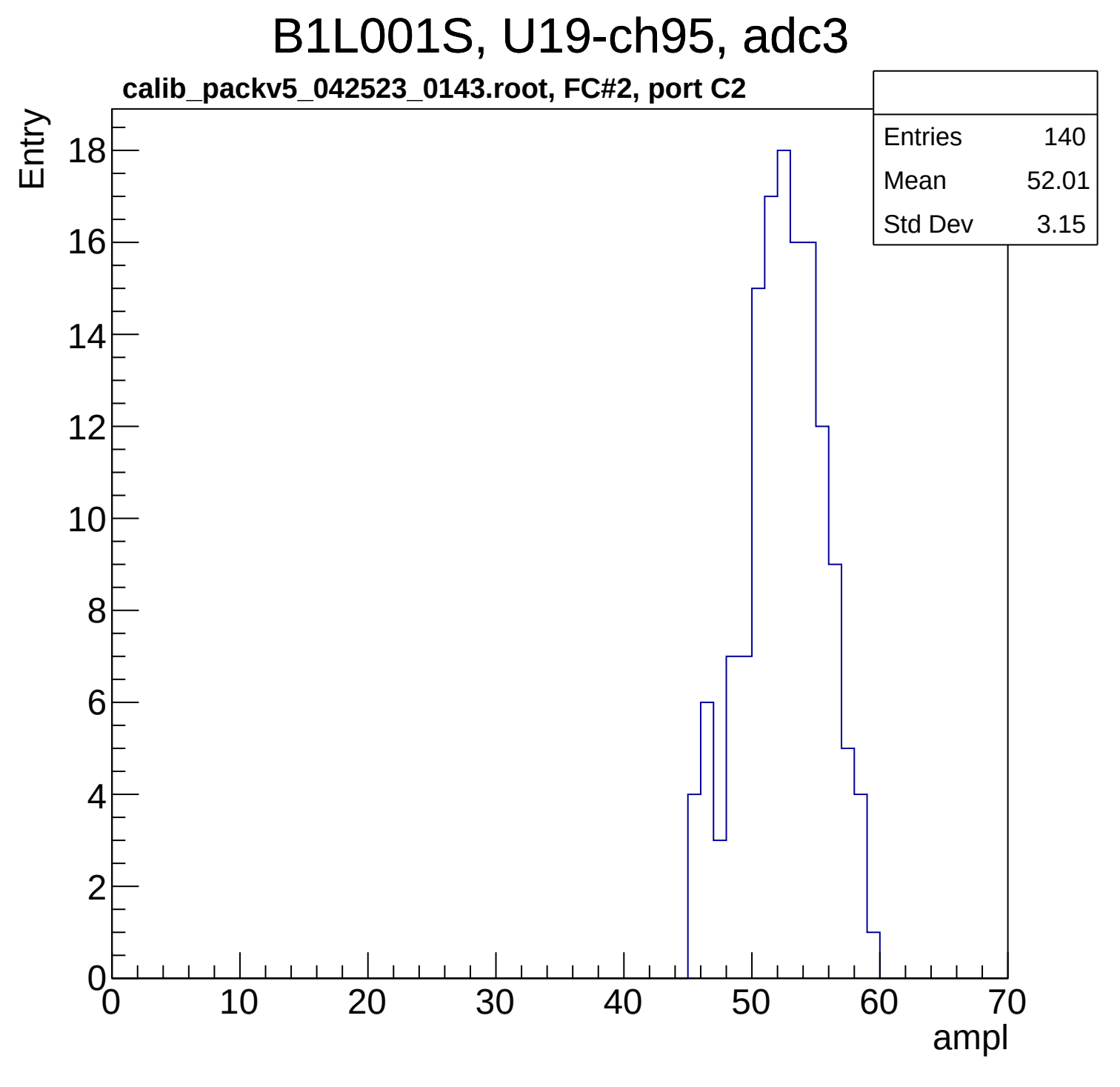
B1L001S, U19-ch95, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 140
Mean 52.01
Std Dev 3.15
Entry
ampl
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4
6
8
10
12
14
16
18
0
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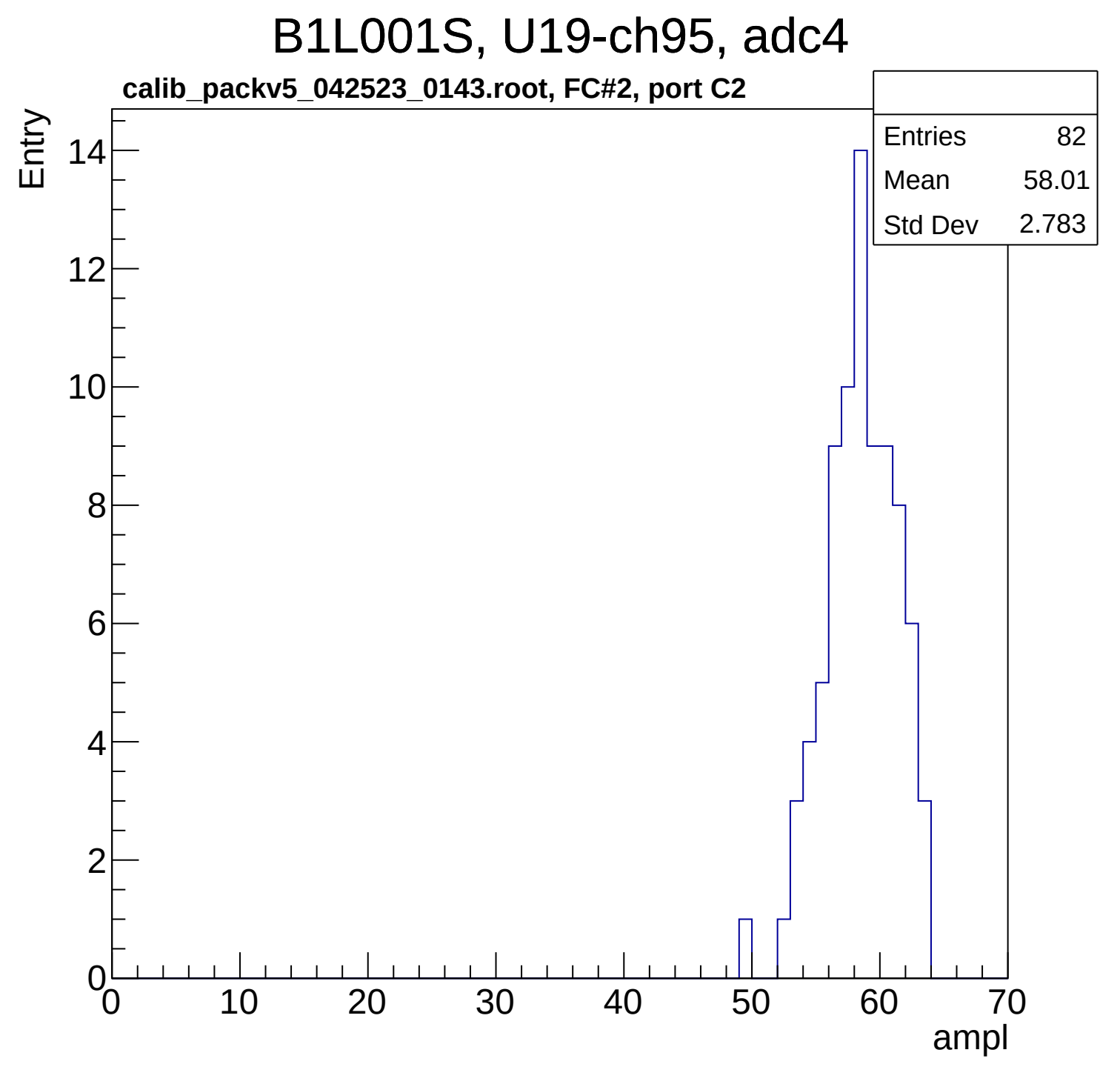
B1L001S, U19-ch95, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 82
Mean 58.01
Std Dev 2.783
Entry
ampl
0
2
4
6
8
10
12
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0
10
20
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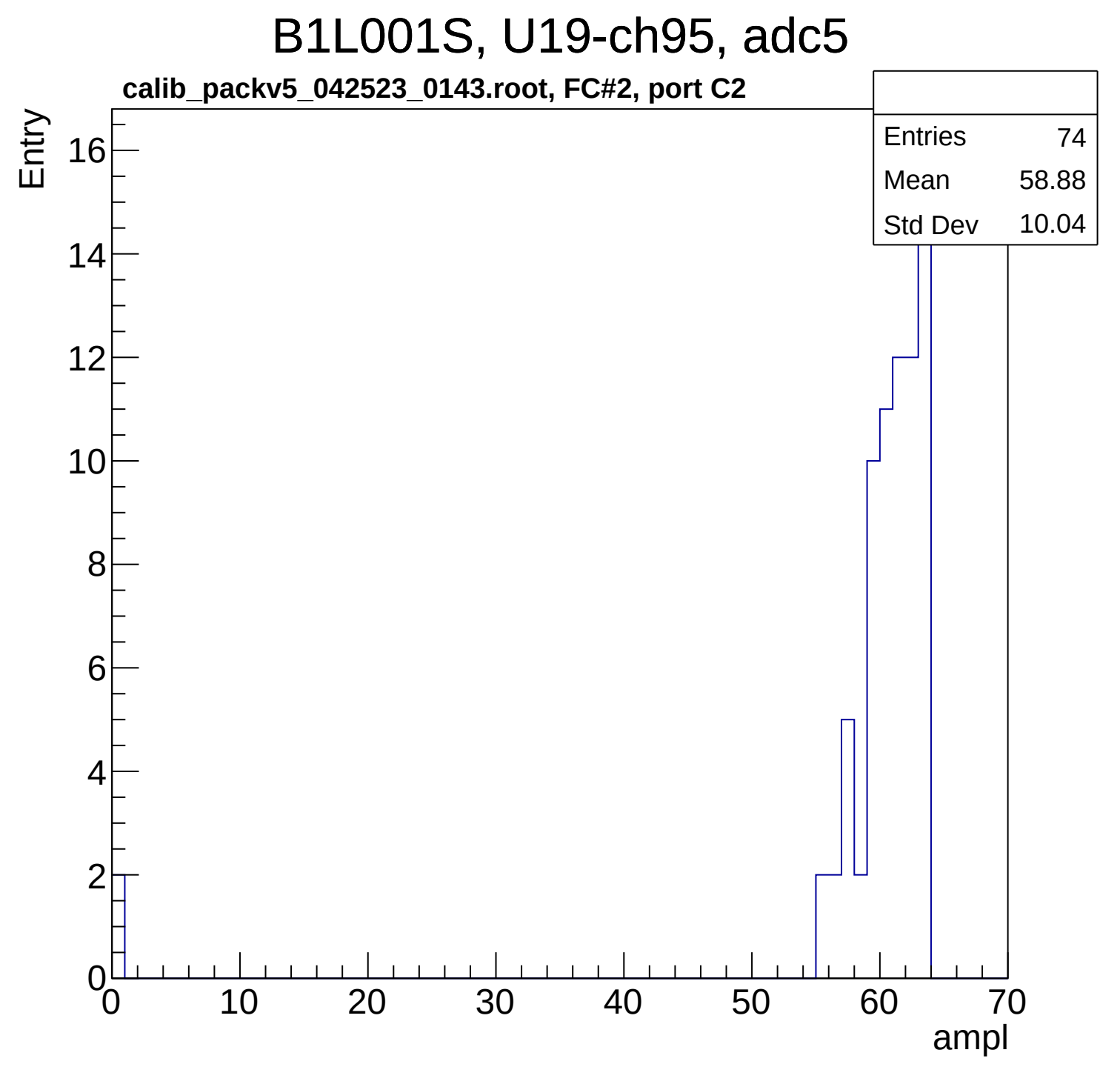
B1L001S, U19-ch95, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 74
Mean 58.88
Std Dev 10.04
Entry
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4
6
8
10
12
14
16
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10
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50
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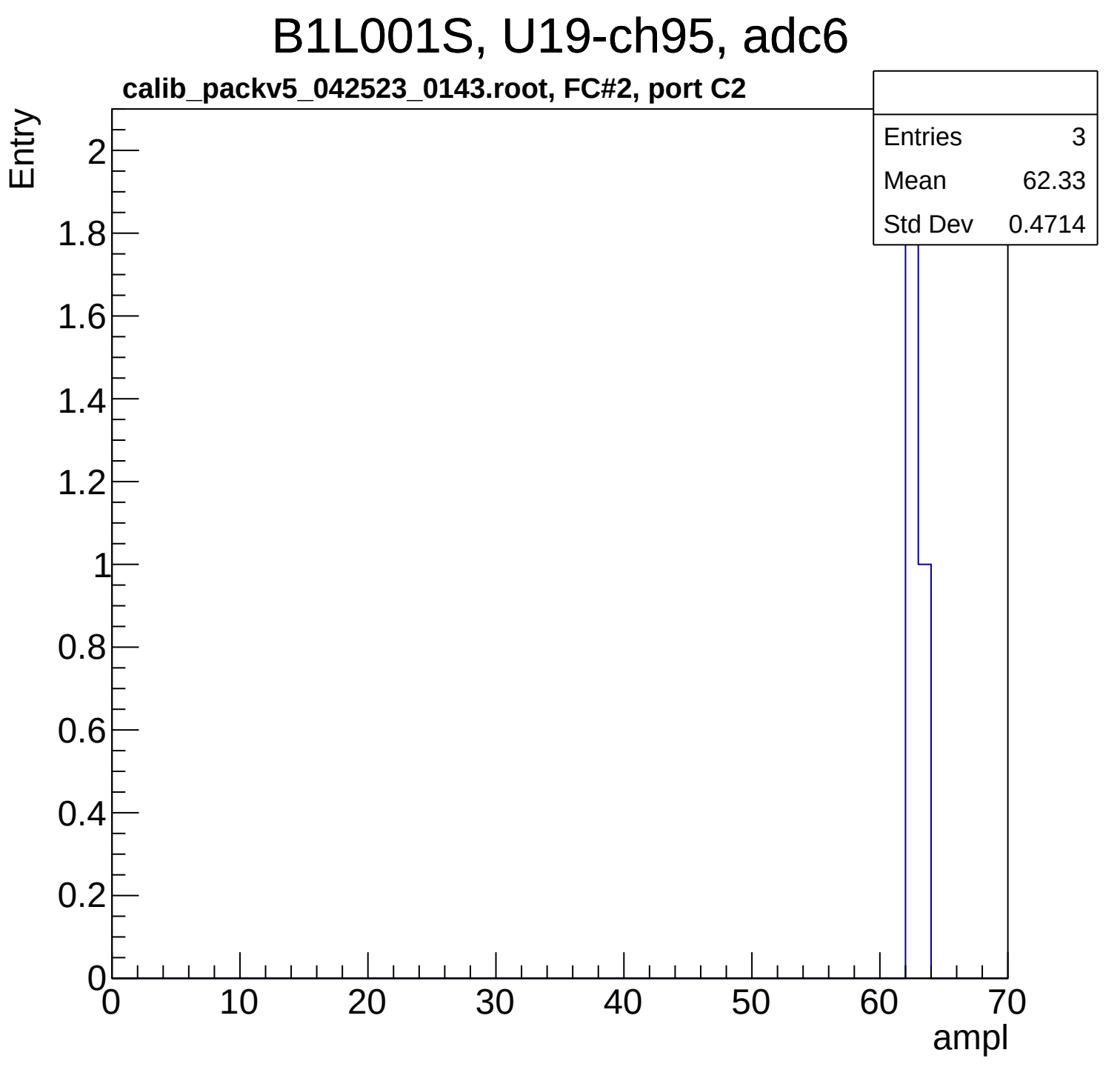
70
ampl


B1L001S, U19-ch95, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 3
Mean 62.33
Std Dev 0.4714
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
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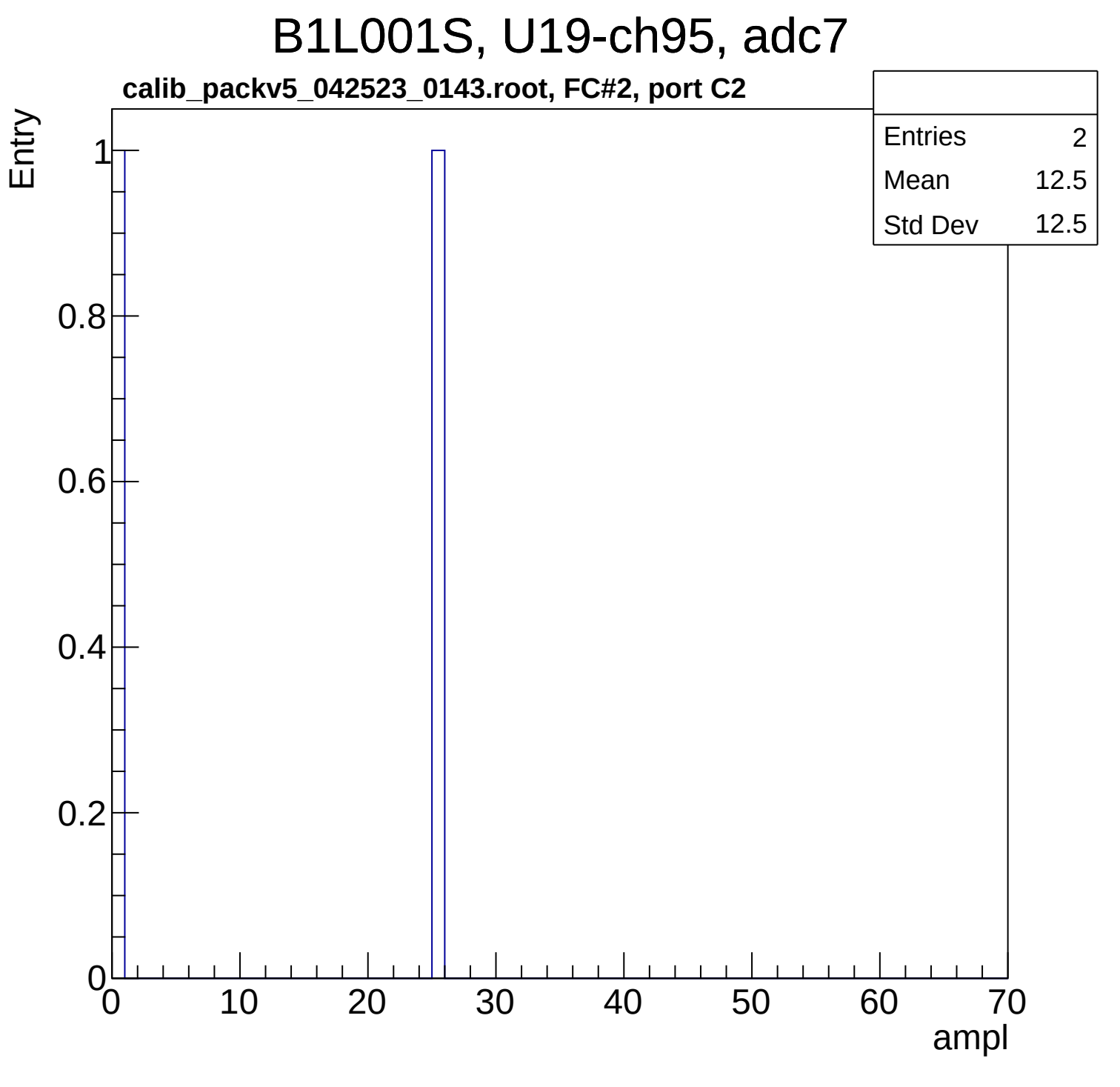
B1L001S, U19-ch95, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 12.5
Std Dev 12.5
Entry
1
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0.6
0.4
0.2
0
0
10
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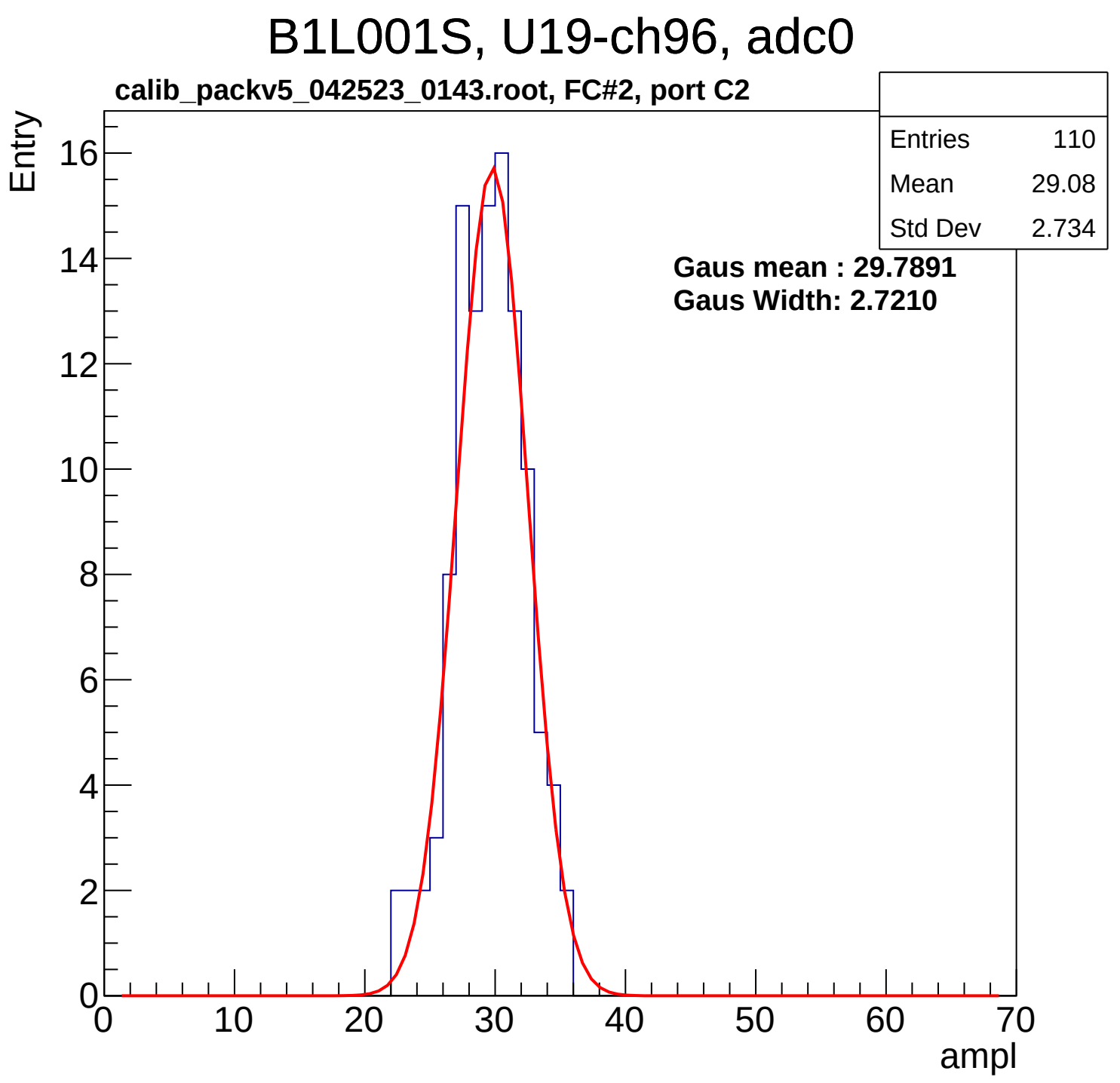
60
70
ampl


B1L001S, U19-ch96, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 110
Mean 29.08
Std Dev 2.734
Gaus mean : 29.7891
Gaus Width: 2.7210
Entry
ampl
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2
4
6
8
10
12
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0
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20
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40
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60
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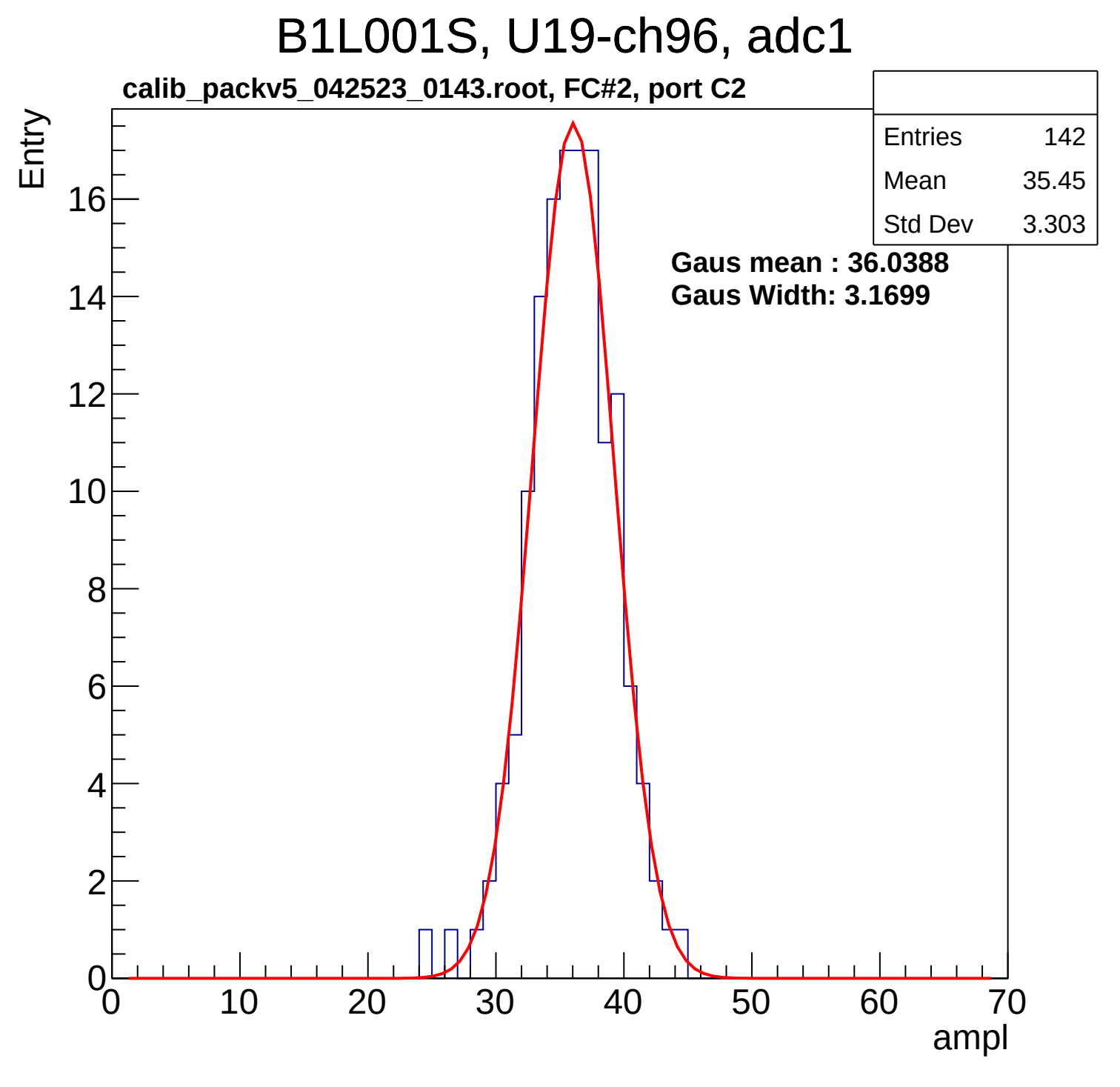
B1L001S, U19-ch96, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 142
Mean 35.45
Std Dev 3.303
Gaus mean : 36.0388
Gaus Width: 3.1699
Entry
ampl
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2
4
6
8
10
12
14
16
0
10
20
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50
60
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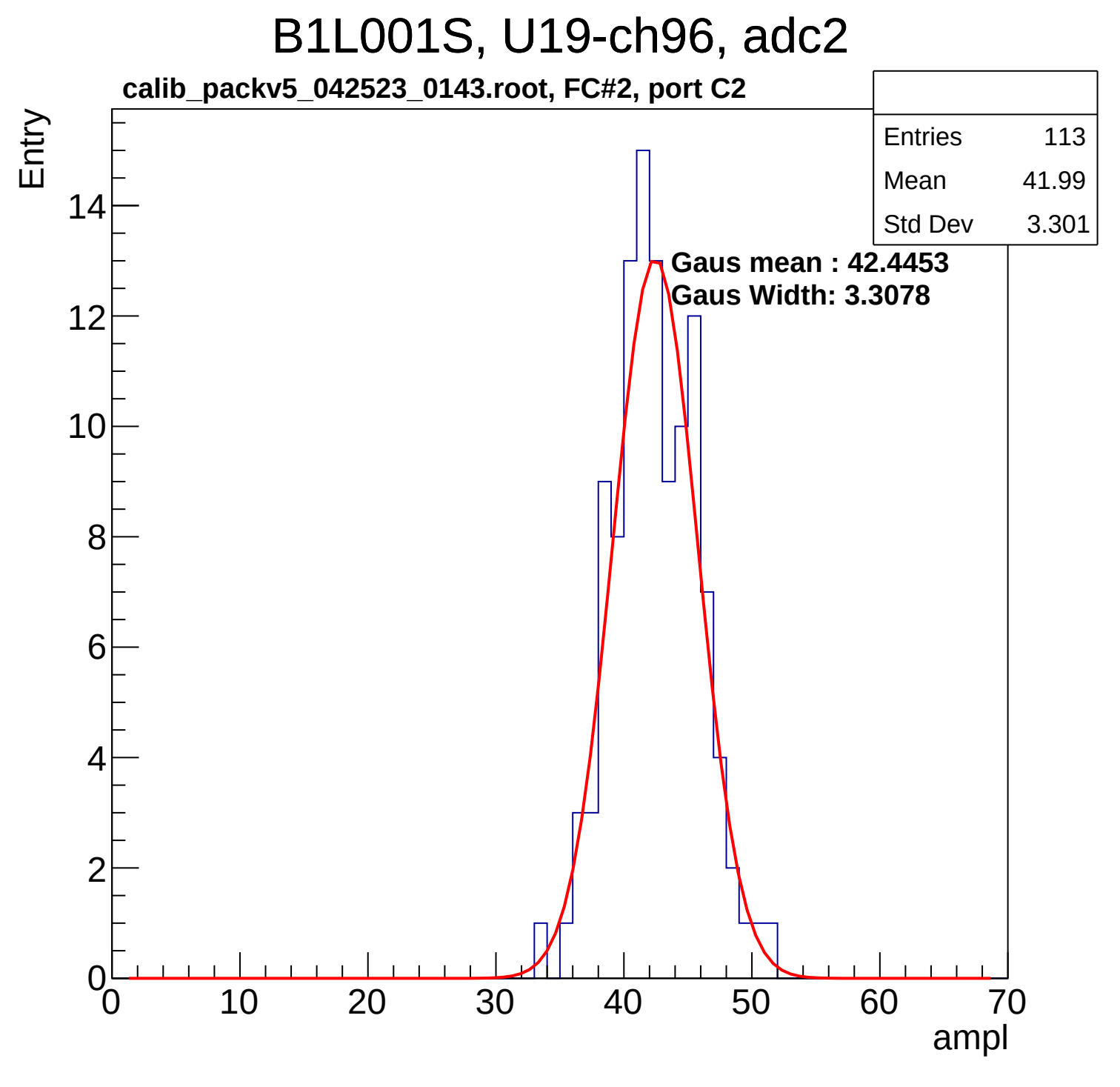
B1L001S, U19-ch96, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 113
Mean 41.99
Std Dev 3.301
Gaus mean : 42.4453
Gaus Width: 3.3078
Entry
ampl
0
2
4
6
8
10
12
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0
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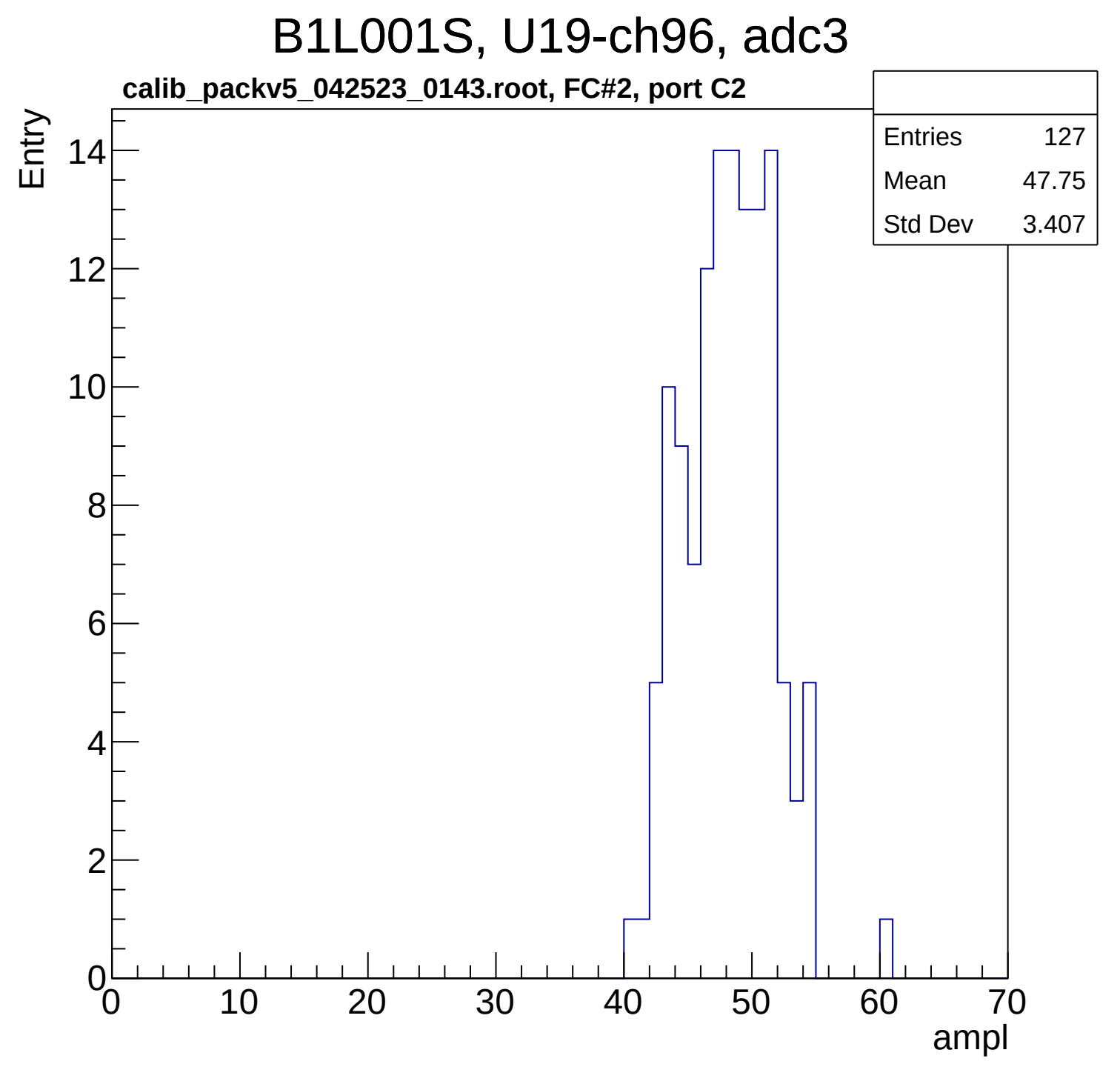
B1L001S, U19-ch96, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 127
Mean 47.75
Std Dev 3.407
Entry
ampl
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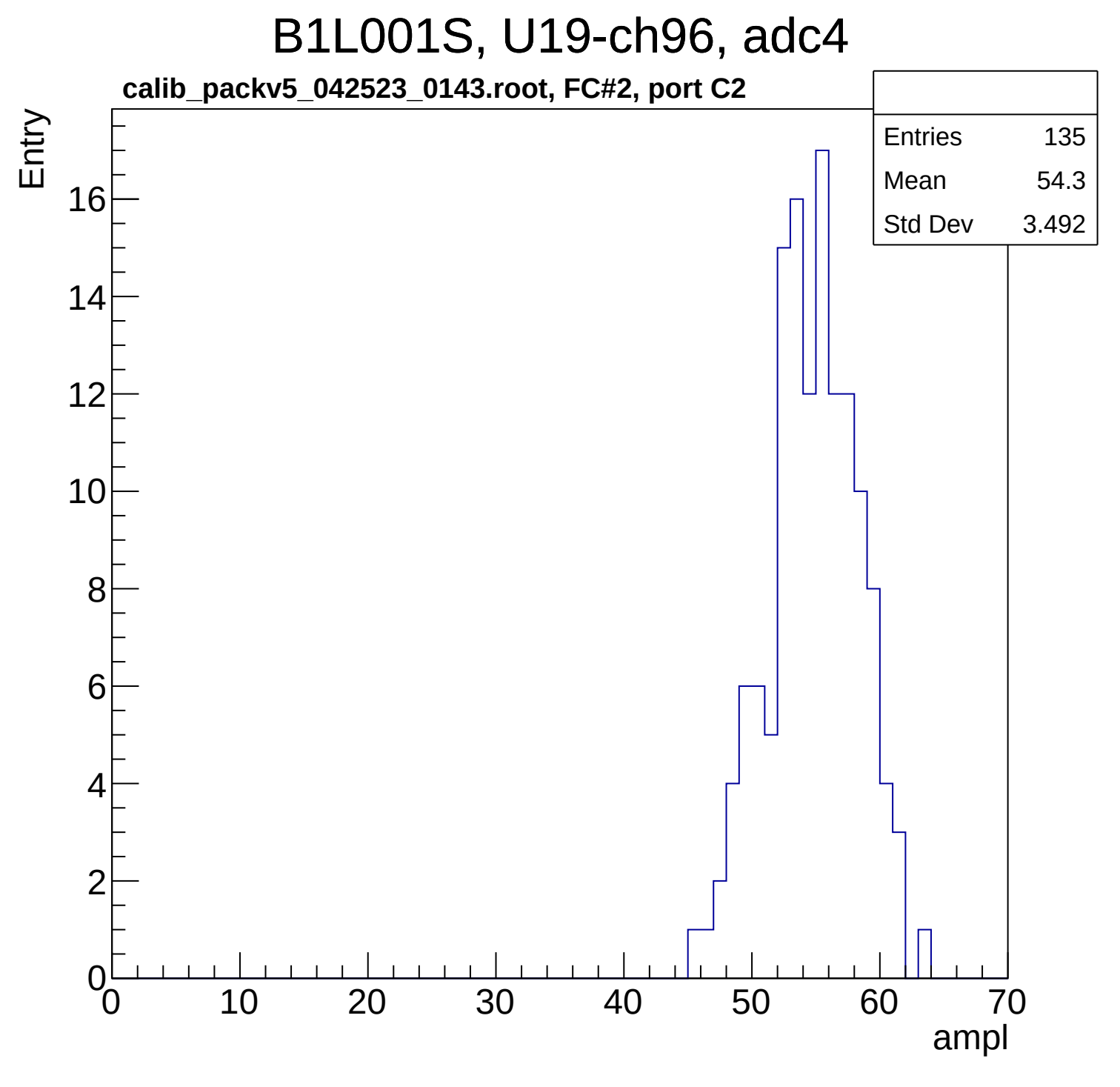
B1L001S, U19-ch96, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 135
Mean 54.3
Std Dev 3.492
Entry
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10
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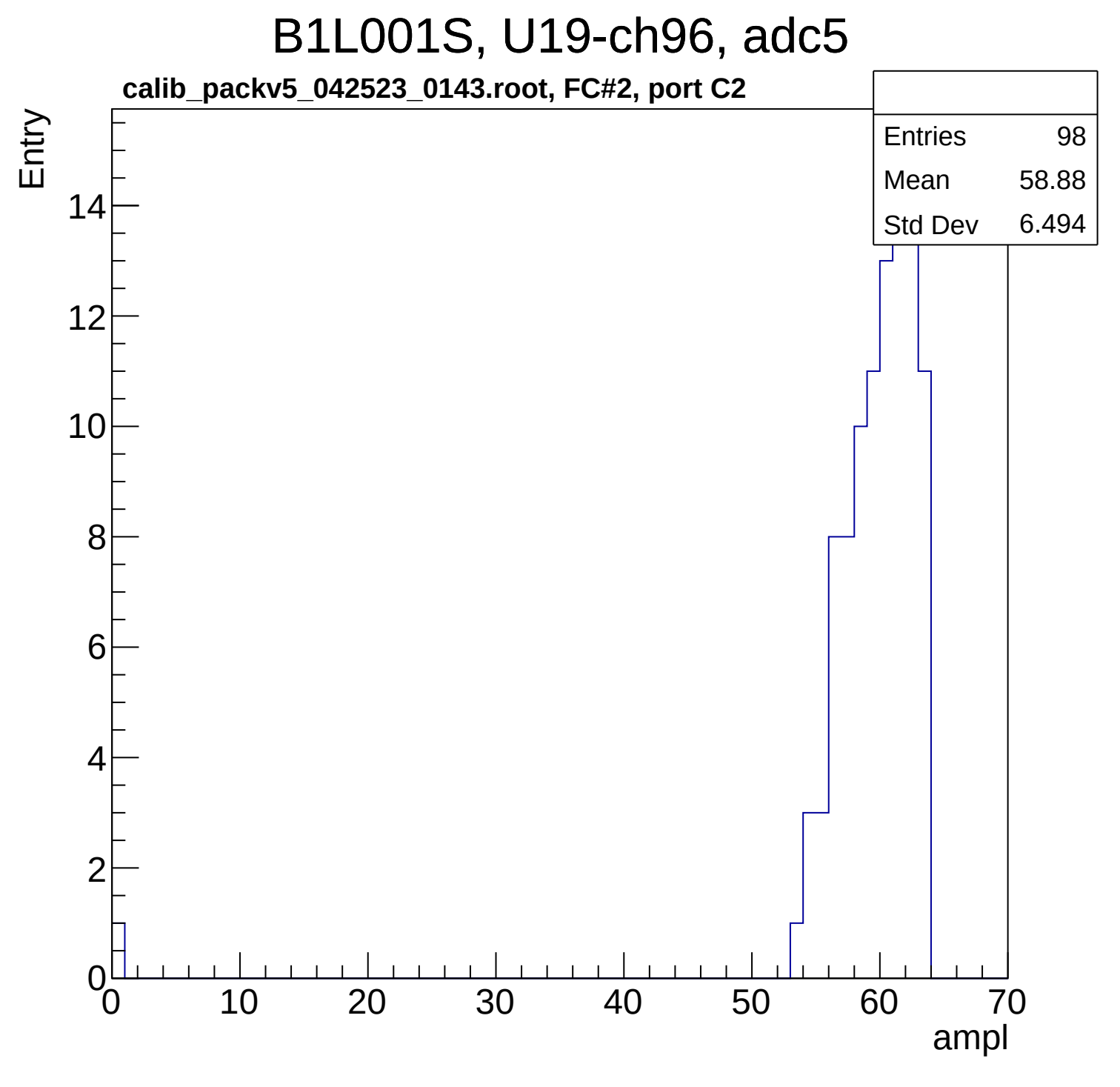
ampl


B1L001S, U19-ch96, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 98
Mean 58.88
Std Dev 6.494
Entry
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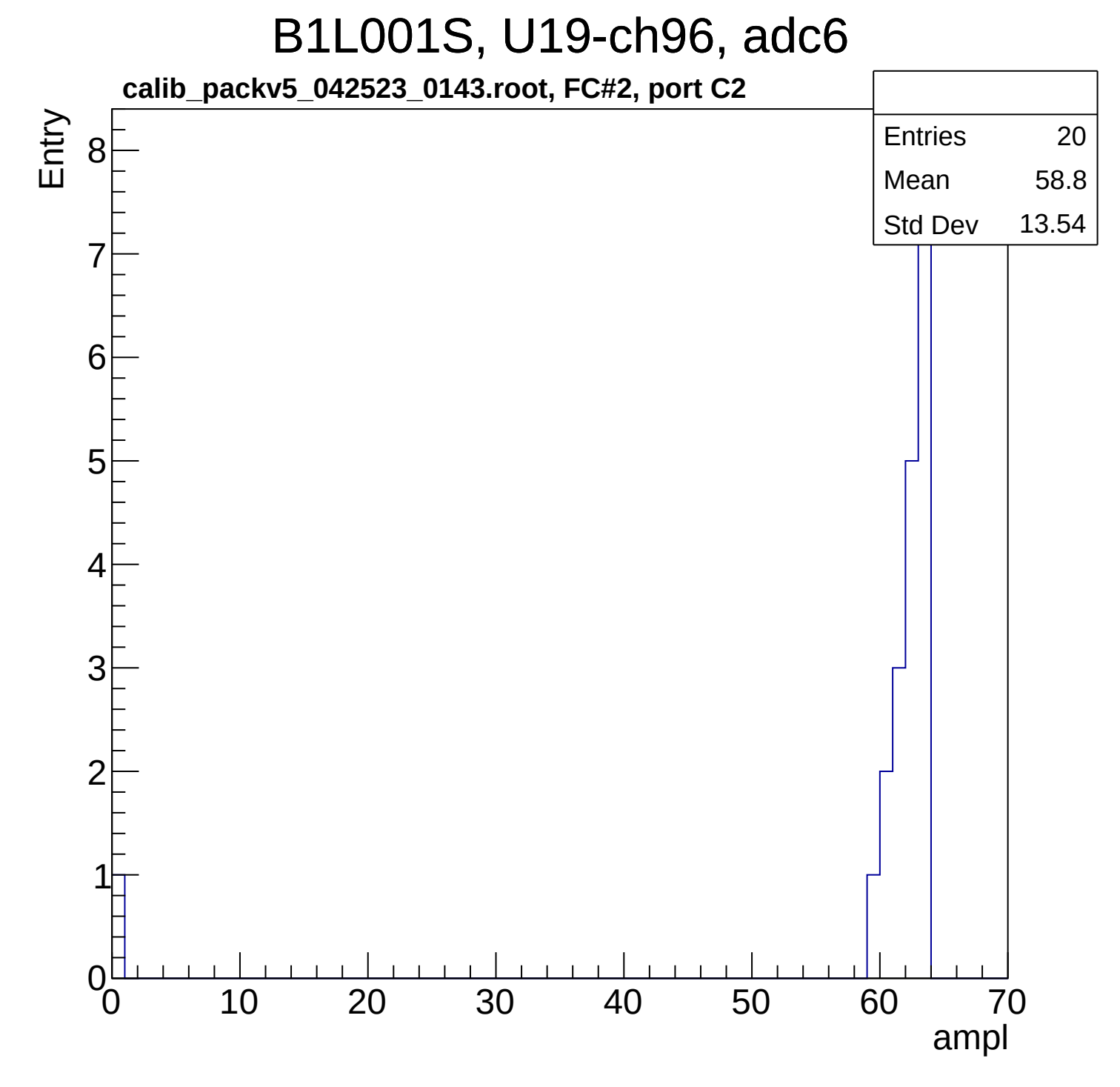
ampl


B1L001S, U19-ch96, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 20
Mean 58.8
Std Dev 13.54
Entry
ampl
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7
8
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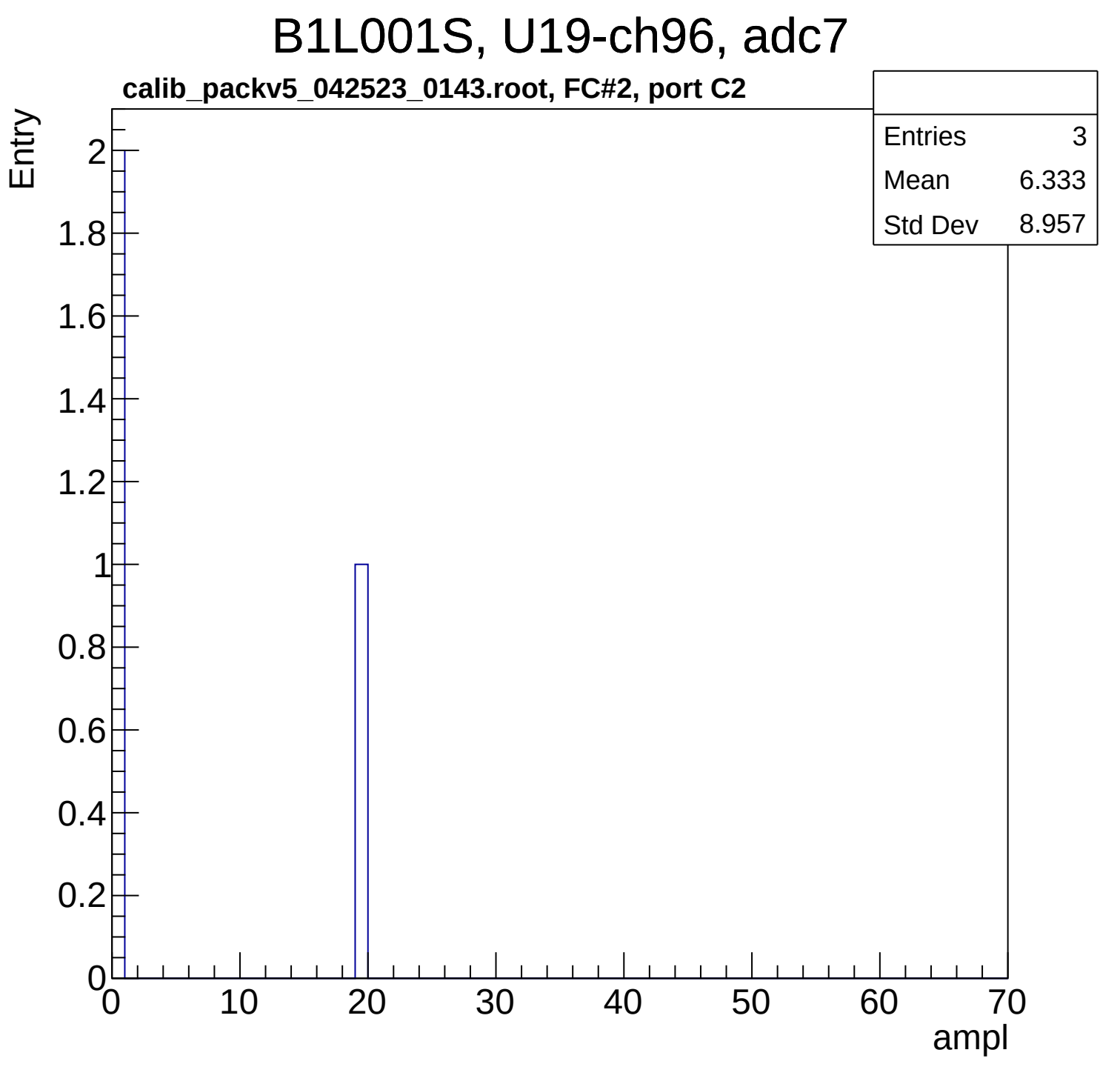
B1L001S, U19-ch96, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 3
Mean 6.333
Std Dev 8.957
Entry
ampl
0
0.2
0.4
0.6
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1.2
1.4
1.6
1.8
2
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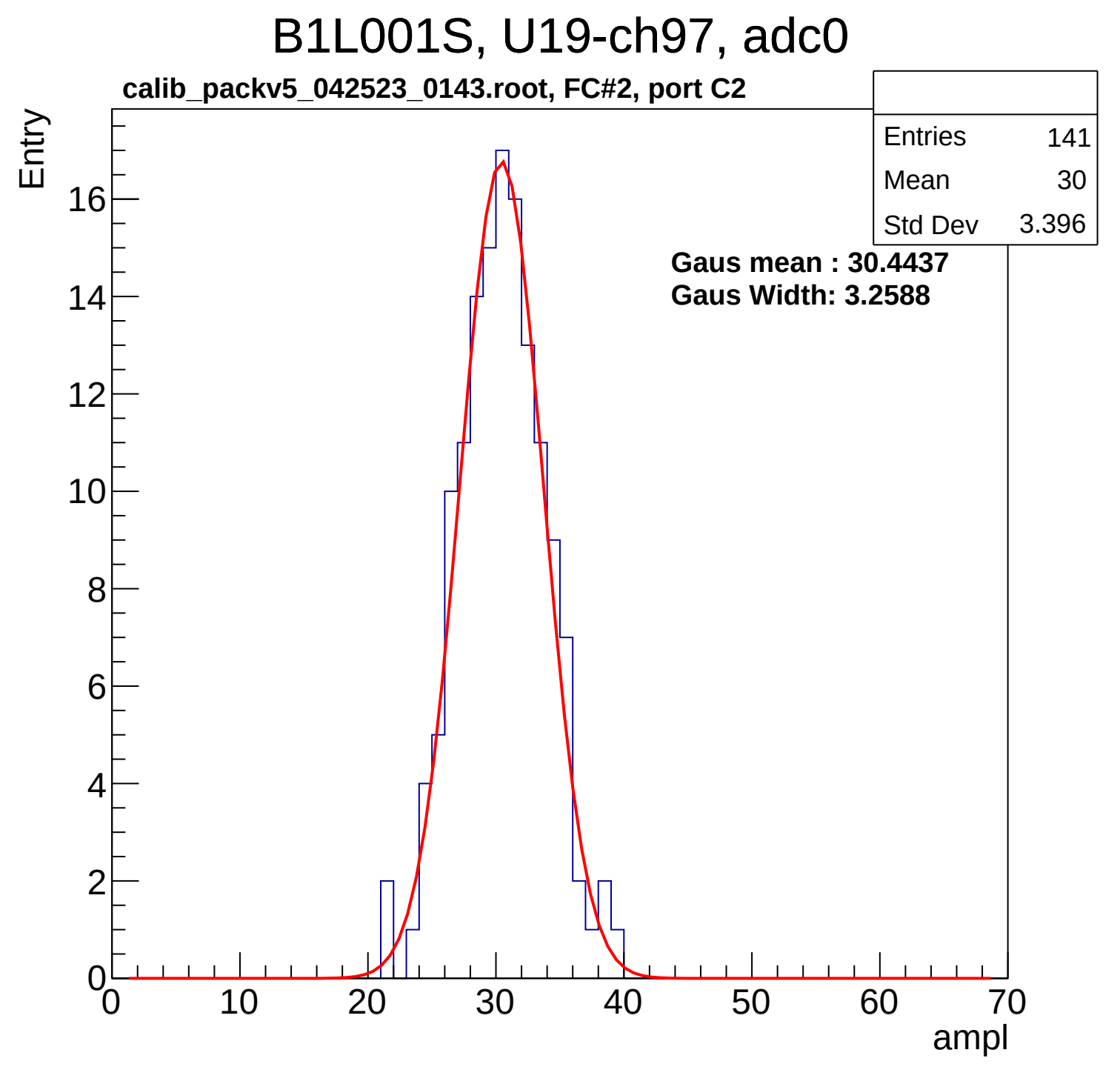
B1L001S, U19-ch97, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 141
Mean 30
Std Dev 3.396
Gaus mean : 30.4437
Gaus Width: 3.2588
Entry
ampl
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2
4
6
8
10
12
14
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0
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20
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50
60
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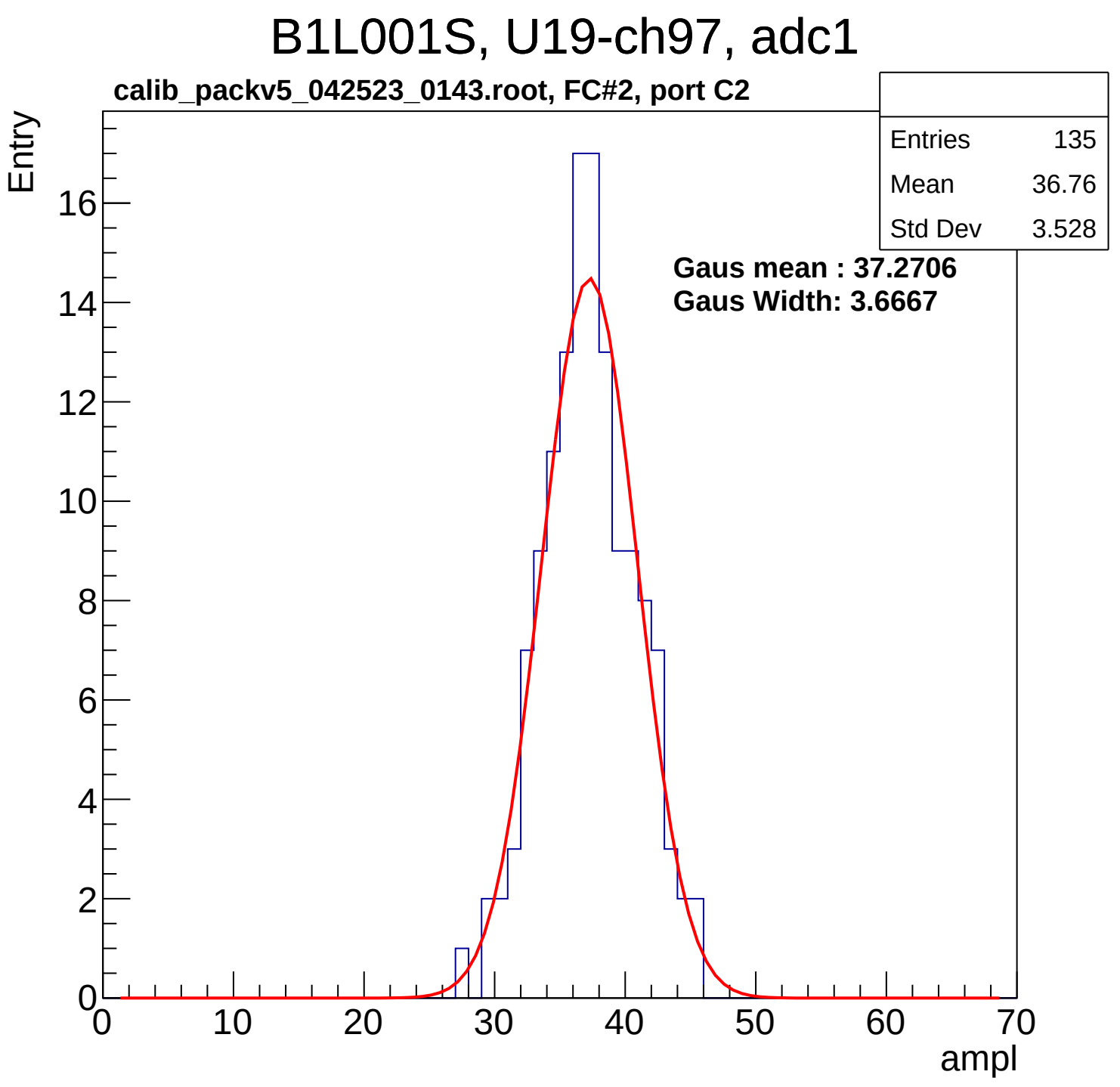
B1L001S, U19-ch97, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 135
Mean 36.76
Std Dev 3.528
Gaus mean : 37.2706
Gaus Width: 3.6667
Entry
ampl
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4
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8
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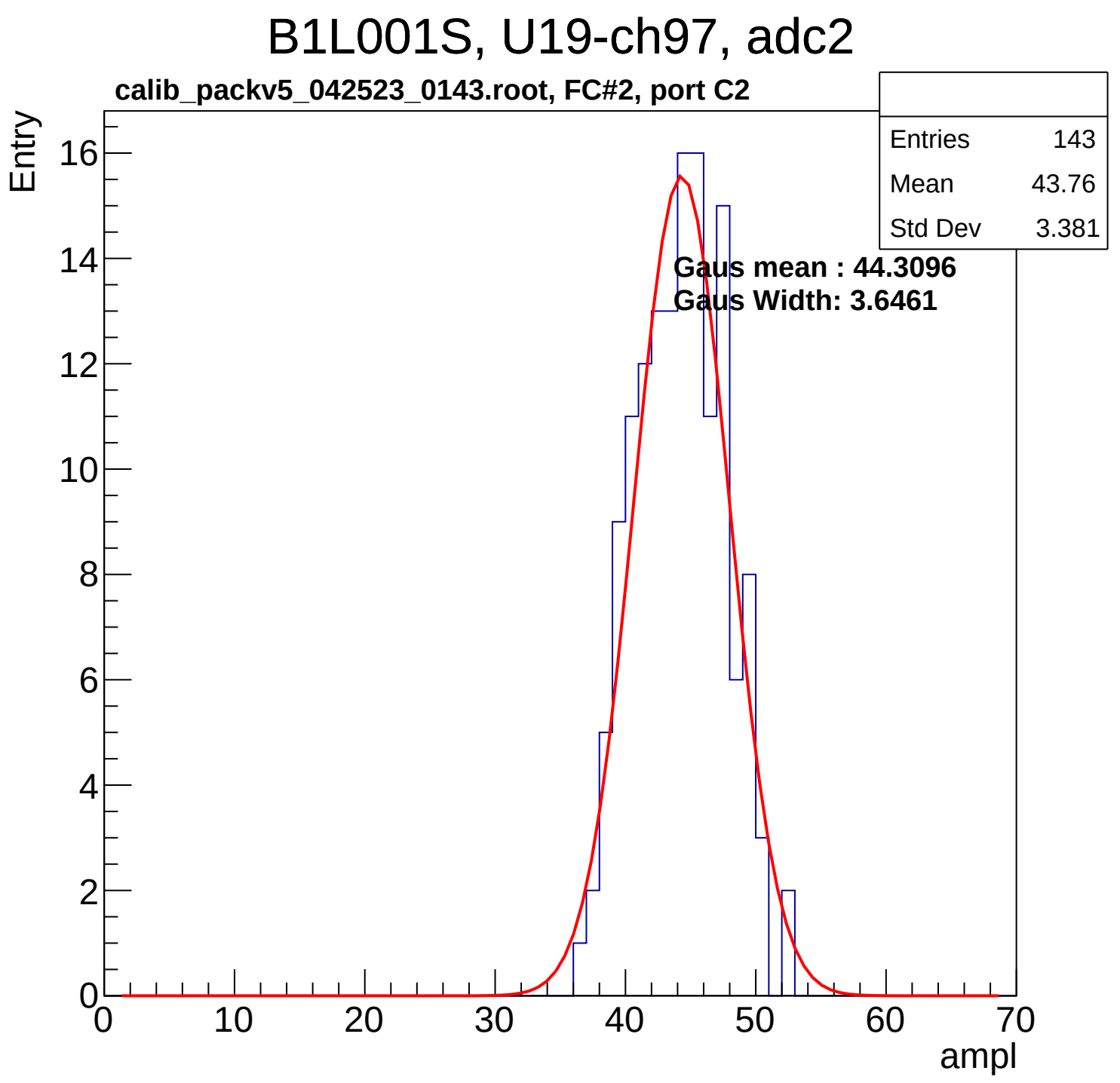
B1L001S, U19-ch97, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 143
Mean 43.76
Std Dev 3.381
Gaus mean : 44.3096
Gaus Width: 3.6461
Entry
ampl
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6
8
10
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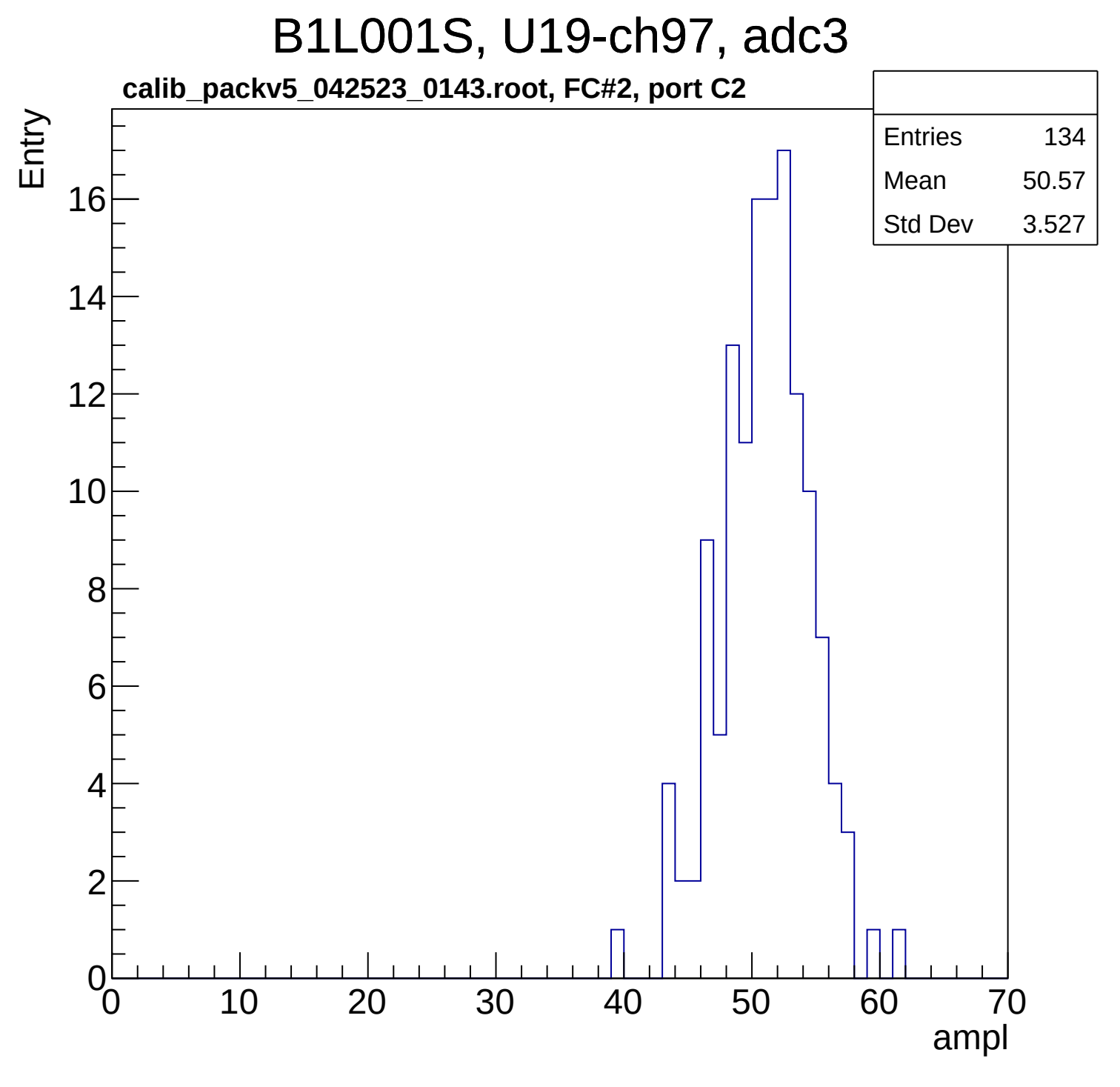
B1L001S, U19-ch97, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 134
Mean 50.57
Std Dev 3.527
Entry
ampl
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6
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10
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14
16
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10
20
30
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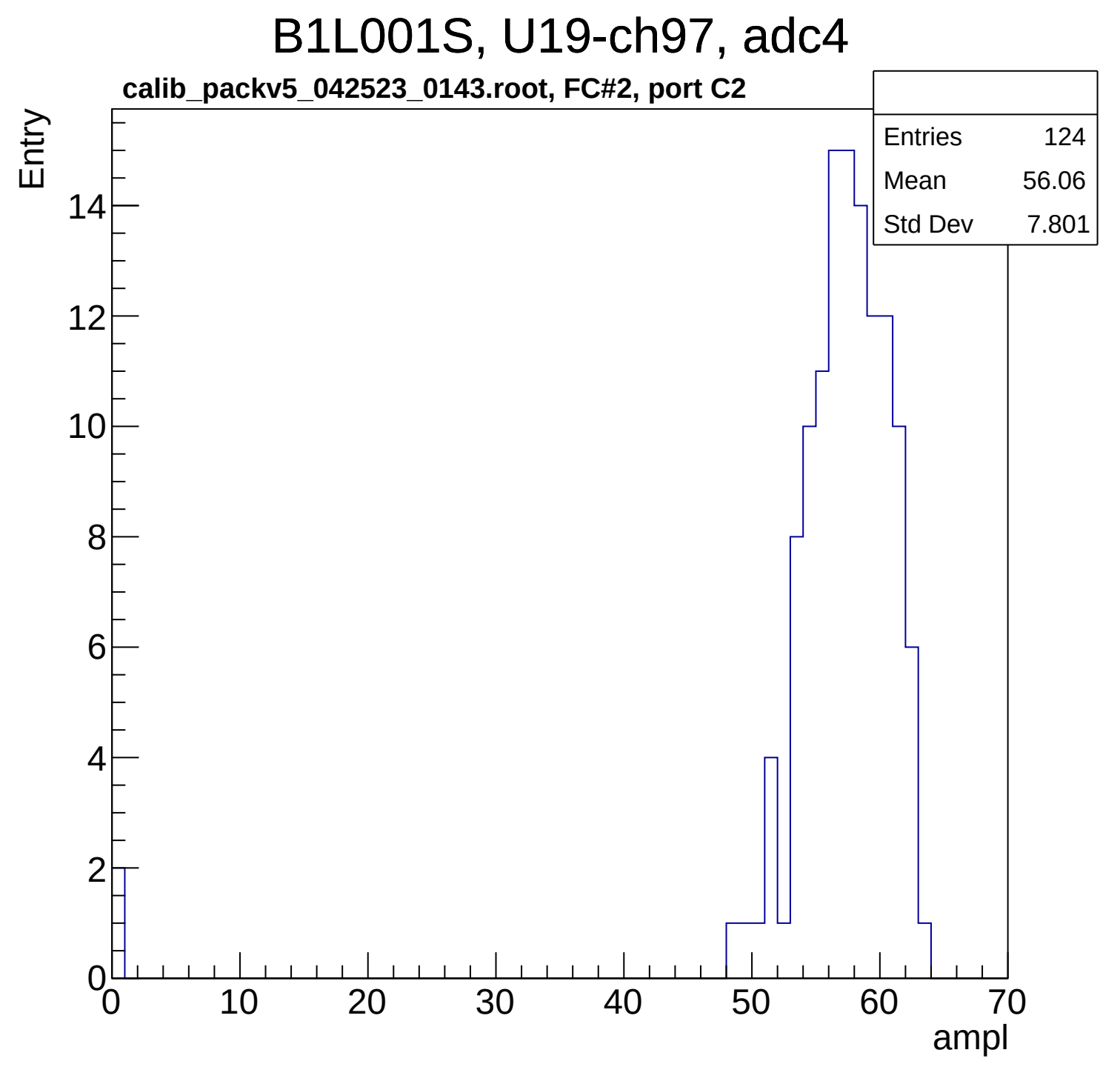
50
60
70


B1L001S, U19-ch97, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 124
Mean 56.06
Std Dev 7.801
Entry
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2
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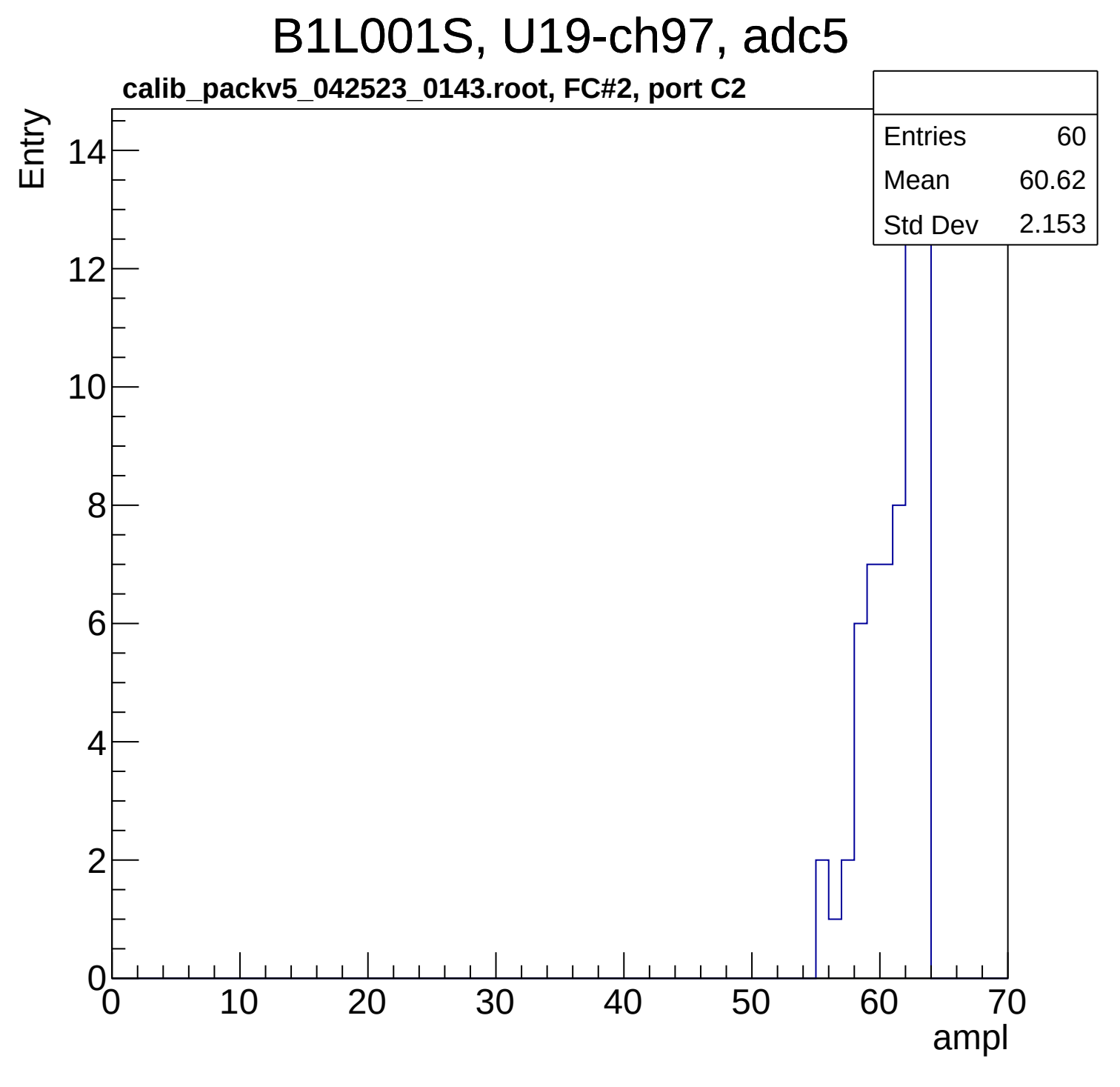
70
ampl


B1L001S, U19-ch97, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 60
Mean 60.62
Std Dev 2.153
Entry
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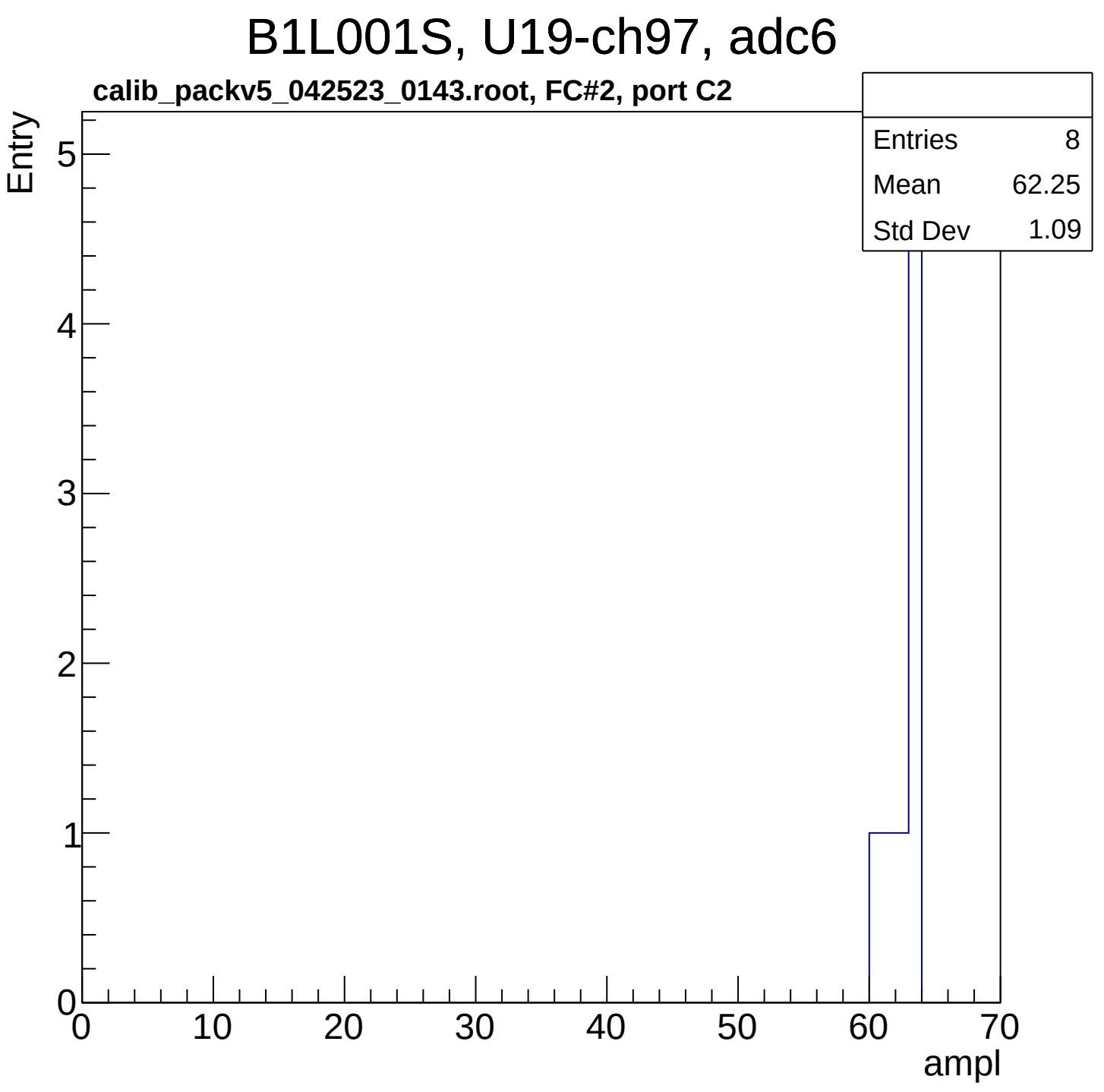
70
ampl


B1L001S, U19-ch97, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 8
Mean 62.25
Std Dev 1.09
Entry
0
1
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3
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5
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10
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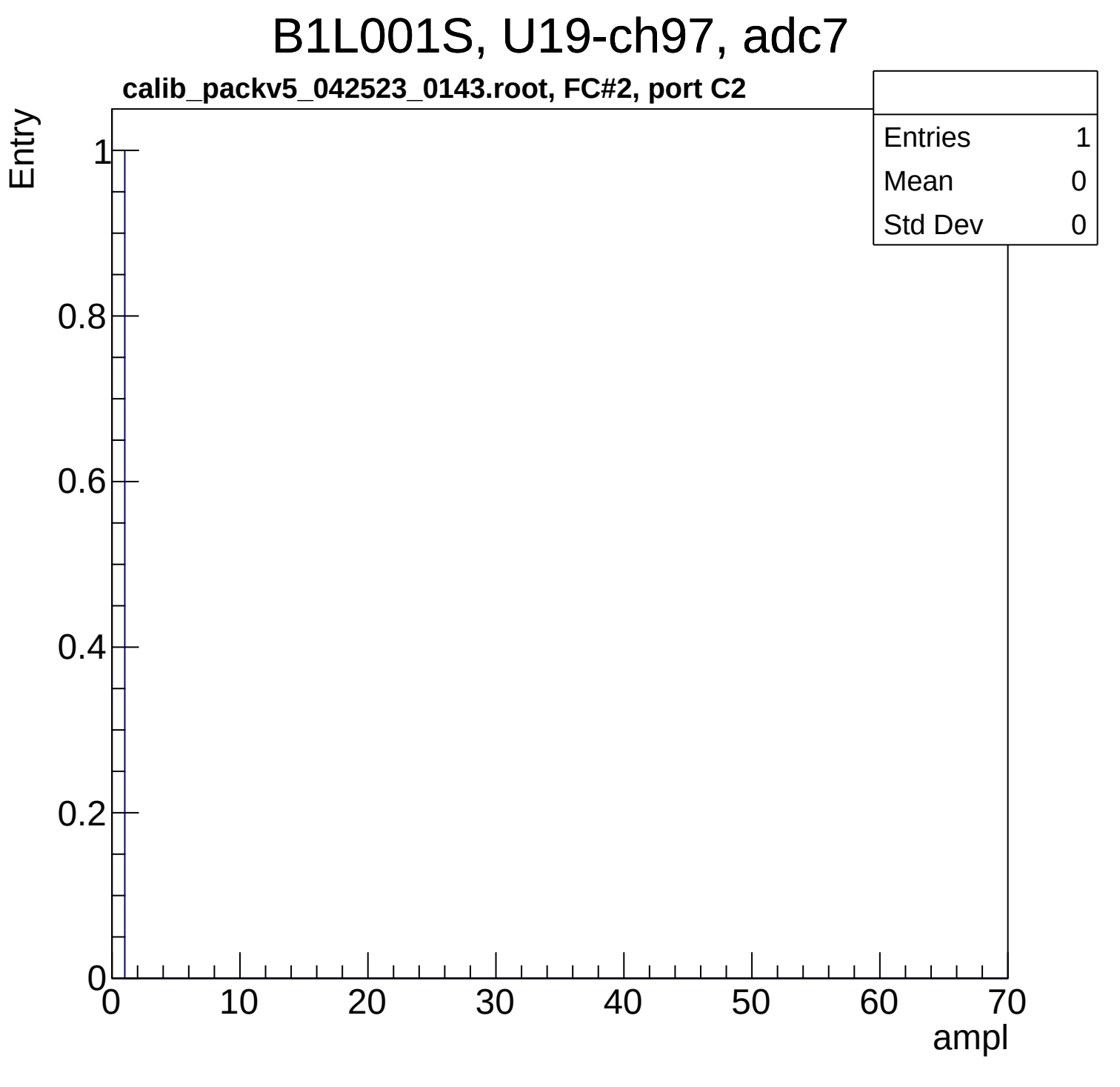
50
60
70
ampl


B1L001S, U19-ch97, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 0
Std Dev 0
Entry
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0.8
0.6
0.4
0.2
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0
10
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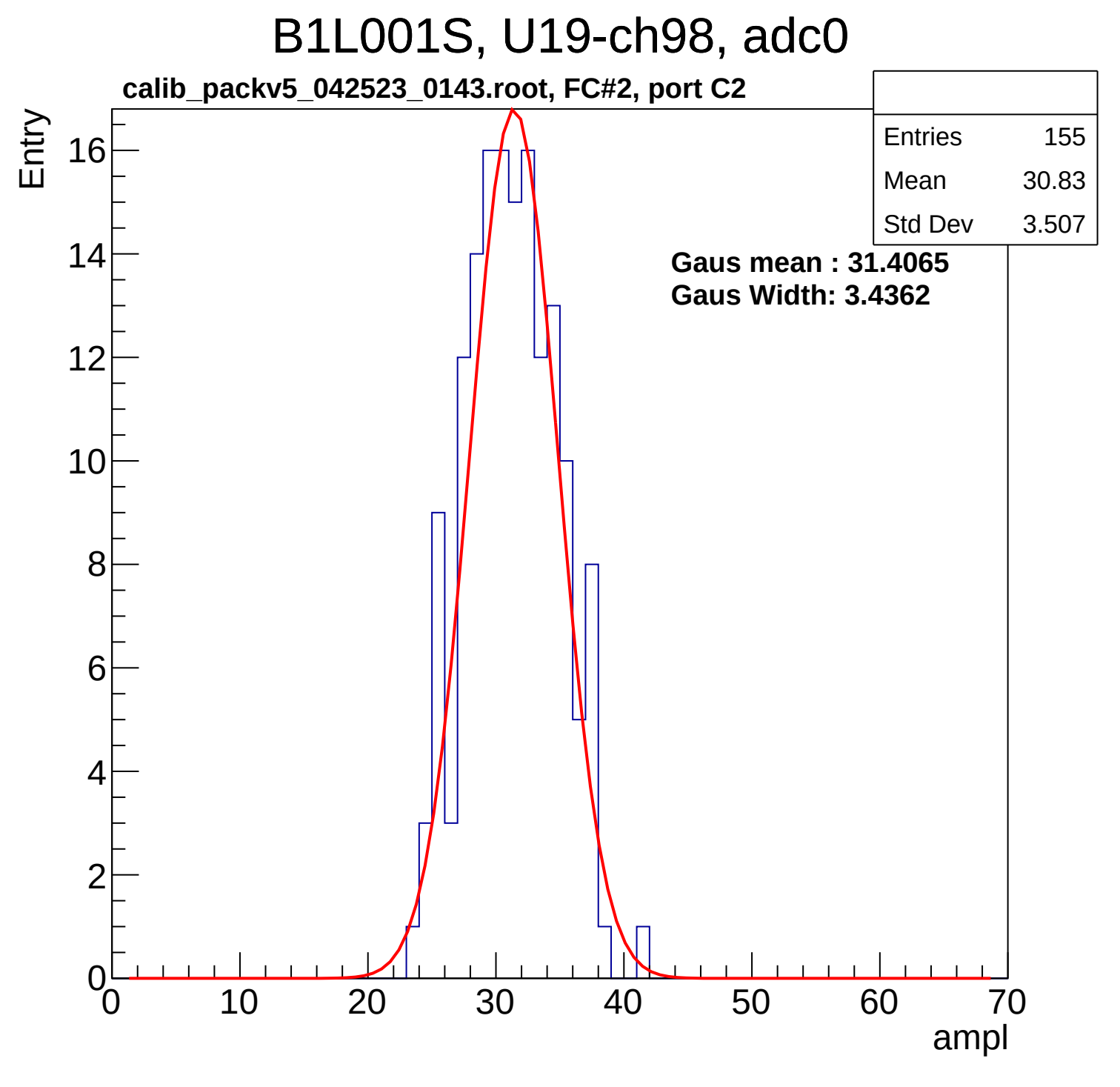
50
60
70
ampl


B1L001S, U19-ch98, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 155
Mean 30.83
Std Dev 3.507
Gaus mean : 31.4065
Gaus Width: 3.4362
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
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30
40
50
60
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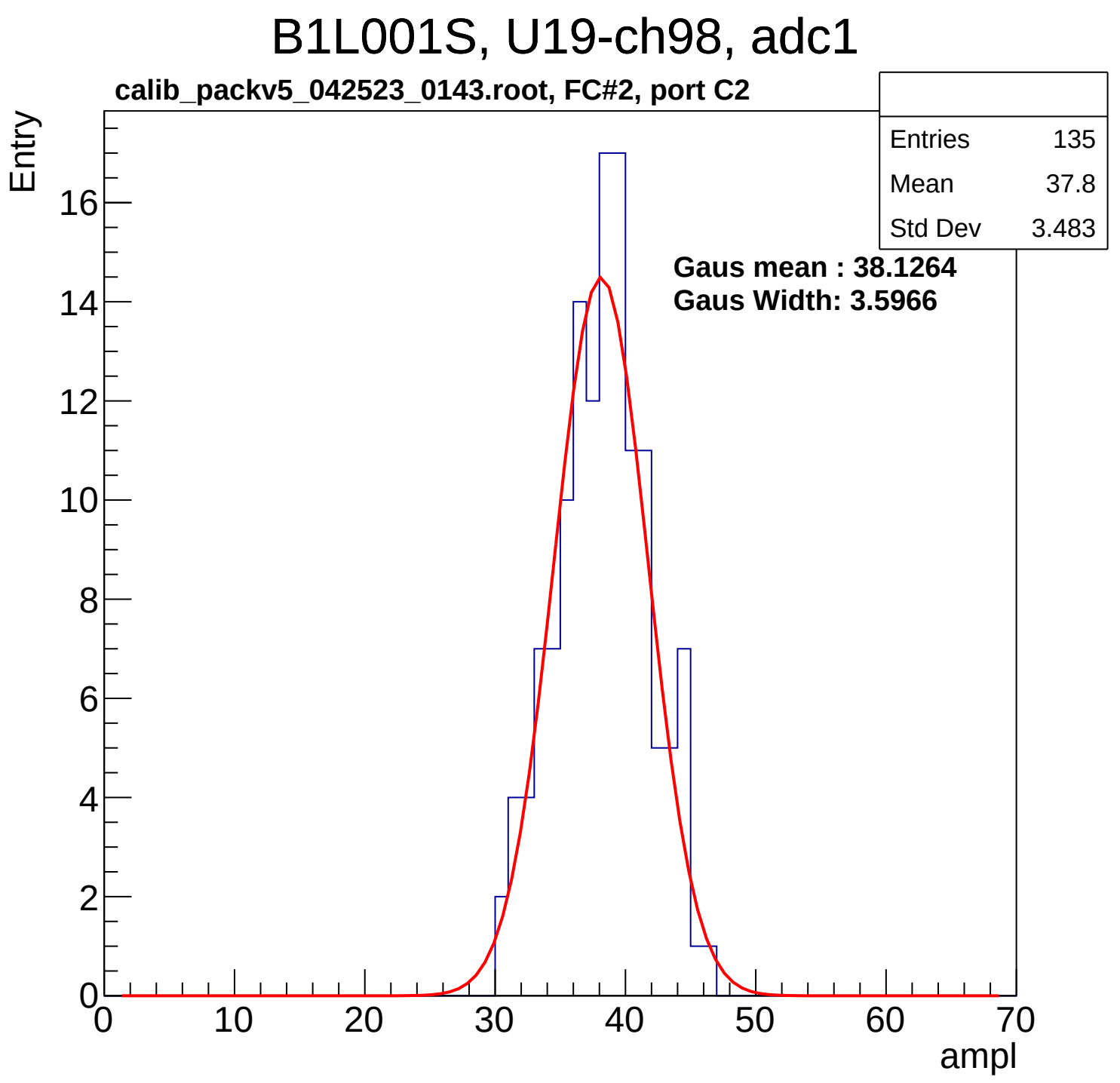
B1L001S, U19-ch98, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 135
Mean 37.8
Std Dev 3.483
Gaus mean : 38.1264
Gaus Width: 3.5966
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
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40
50
60
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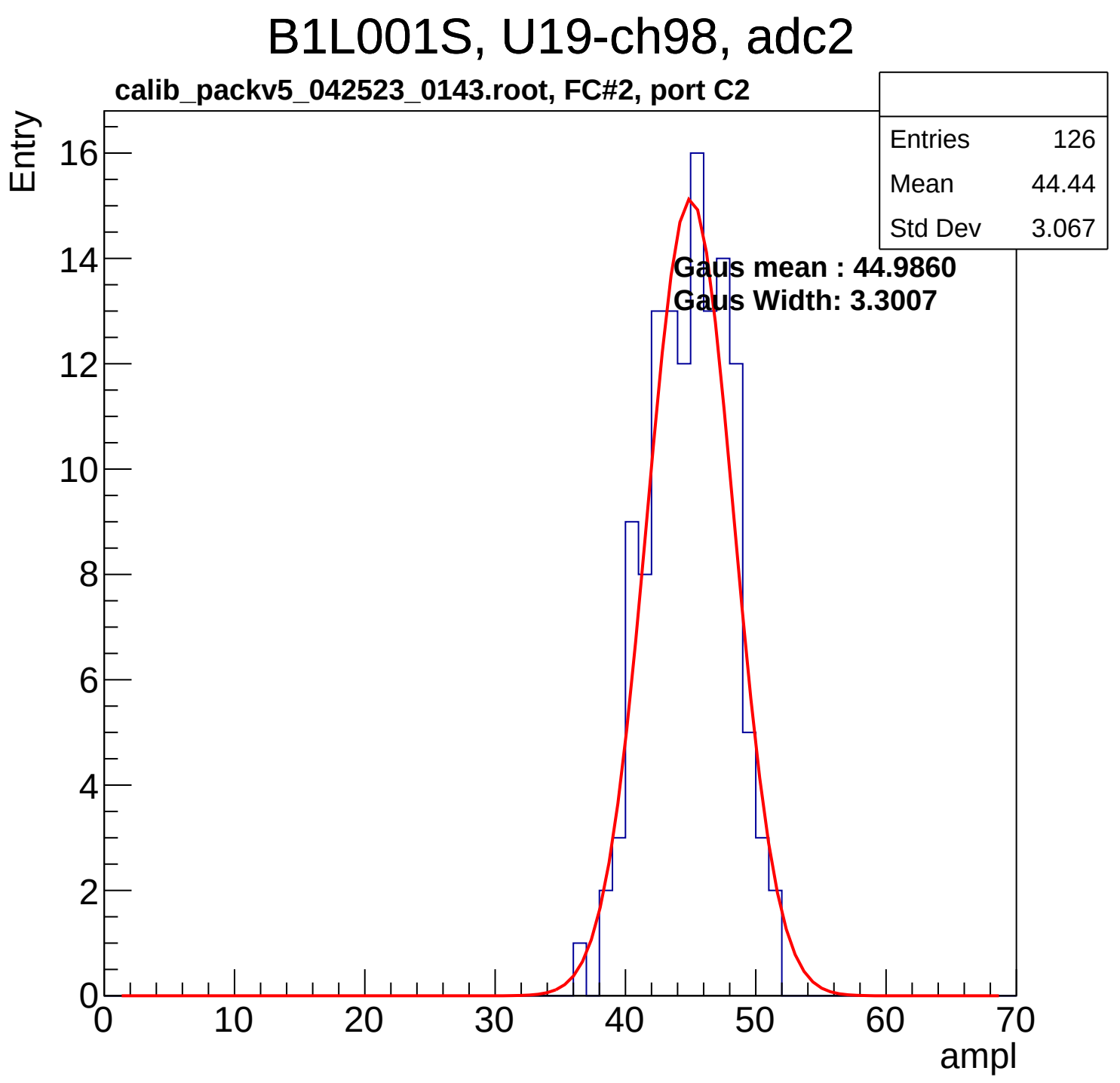
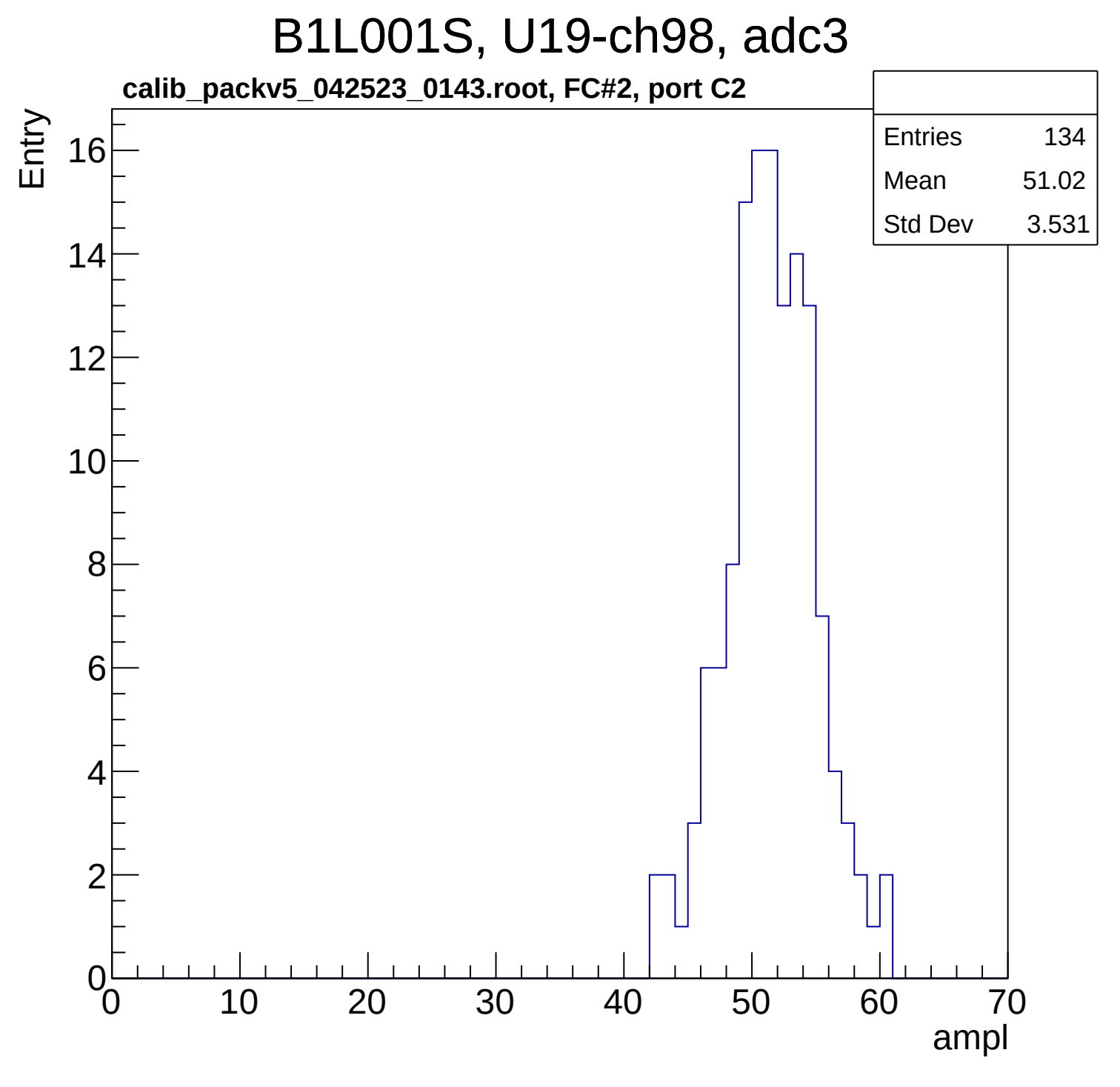

B1L001S, U19-ch98, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 126
Mean 44.44
Std Dev 3.067
Gaus mean : 44.9860
Gaus Width: 3.3007
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70


B1L001S, U19-ch98, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 134
Mean 51.02
Std Dev 3.531
Entry
ampl
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2
4
6
8
10
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0
10
20
30
40
50
60
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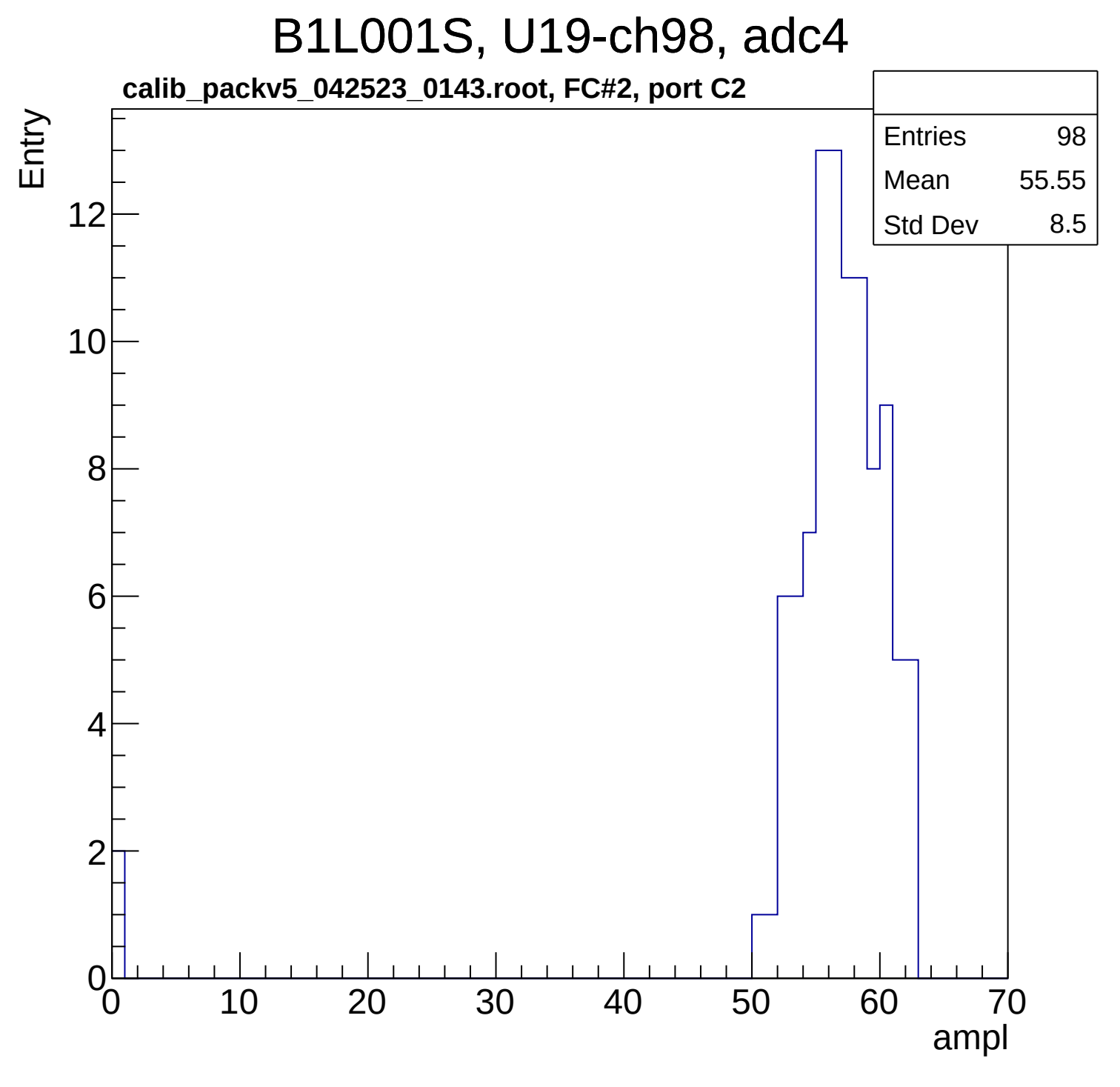
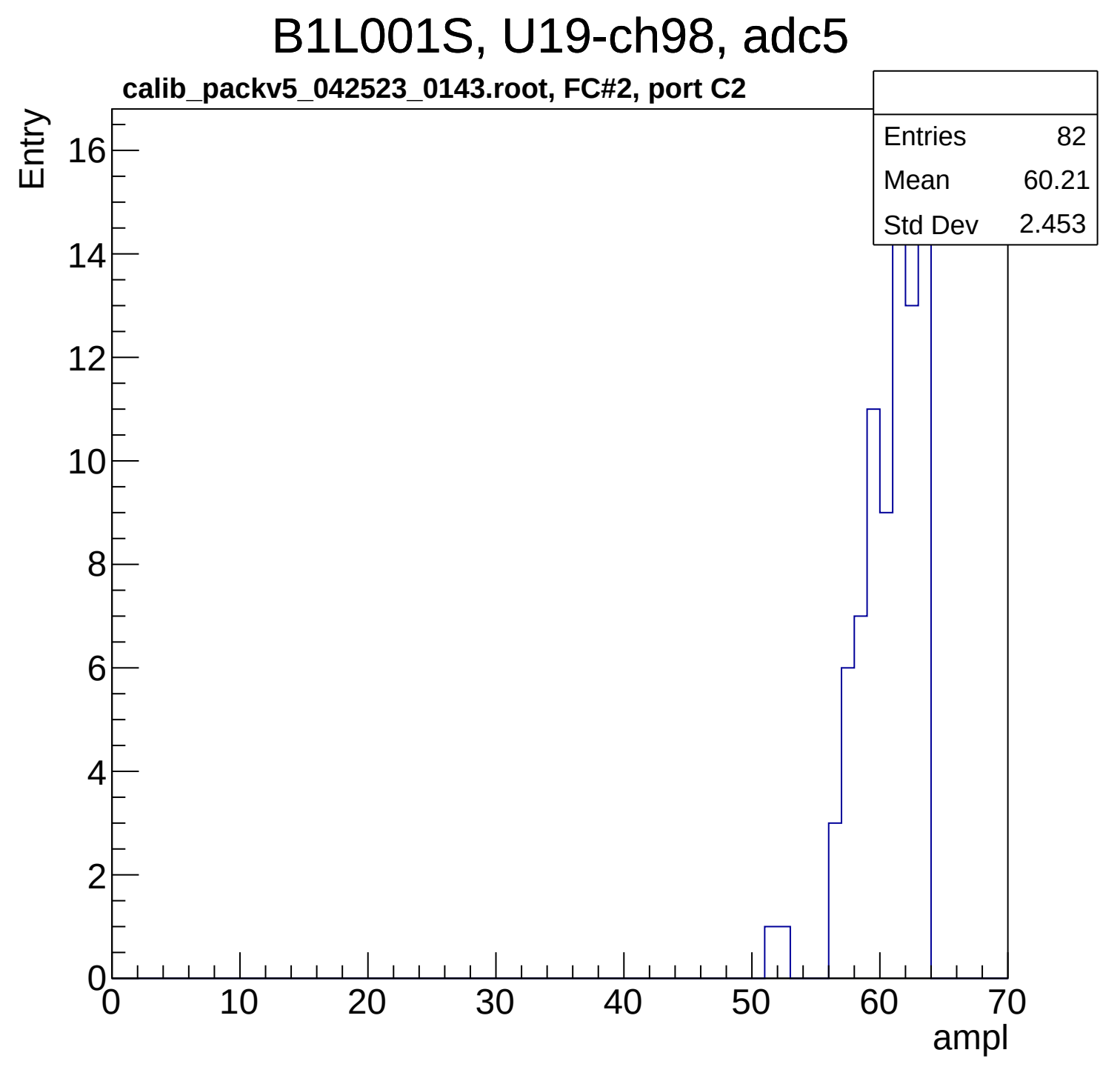

B1L001S, U19-ch98, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 98
Mean 55.55
Std Dev 8.5
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch98, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 82
Mean 60.21
Std Dev 2.453
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
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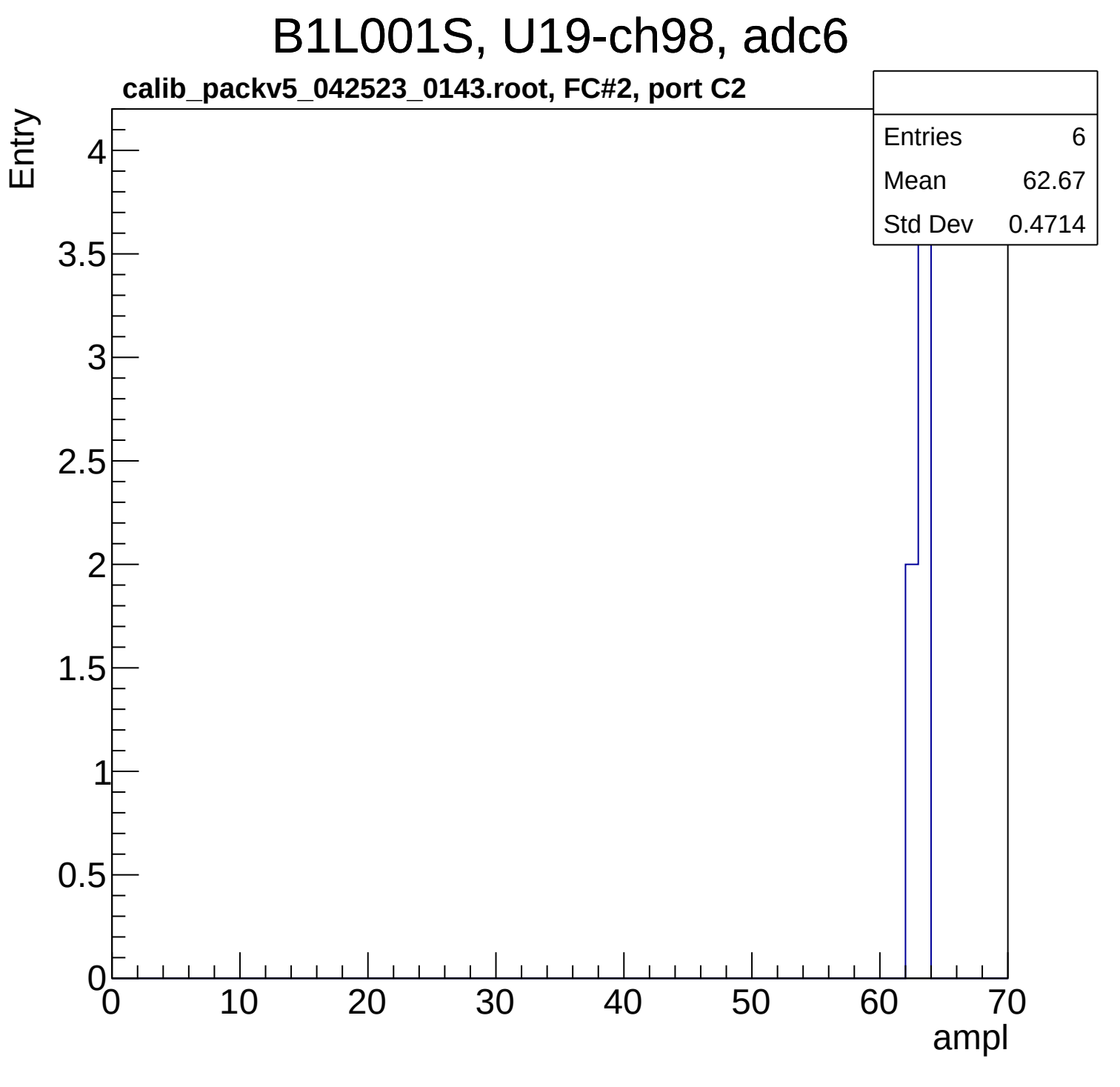
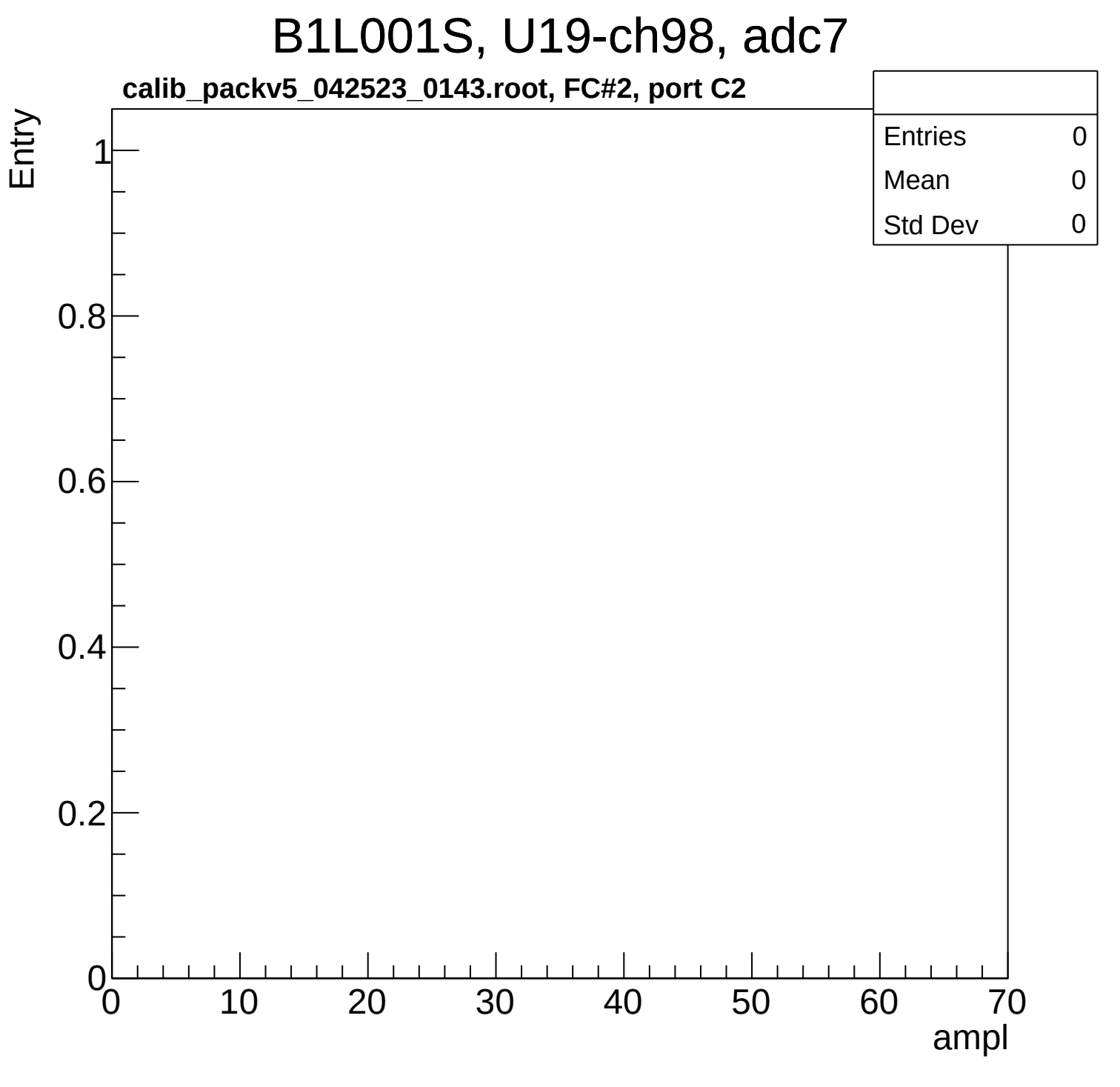

B1L001S, U19-ch98, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 6
Mean 62.67
Std Dev 0.4714
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L001S, U19-ch98, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 0
Mean 0
Std Dev 0
Entry
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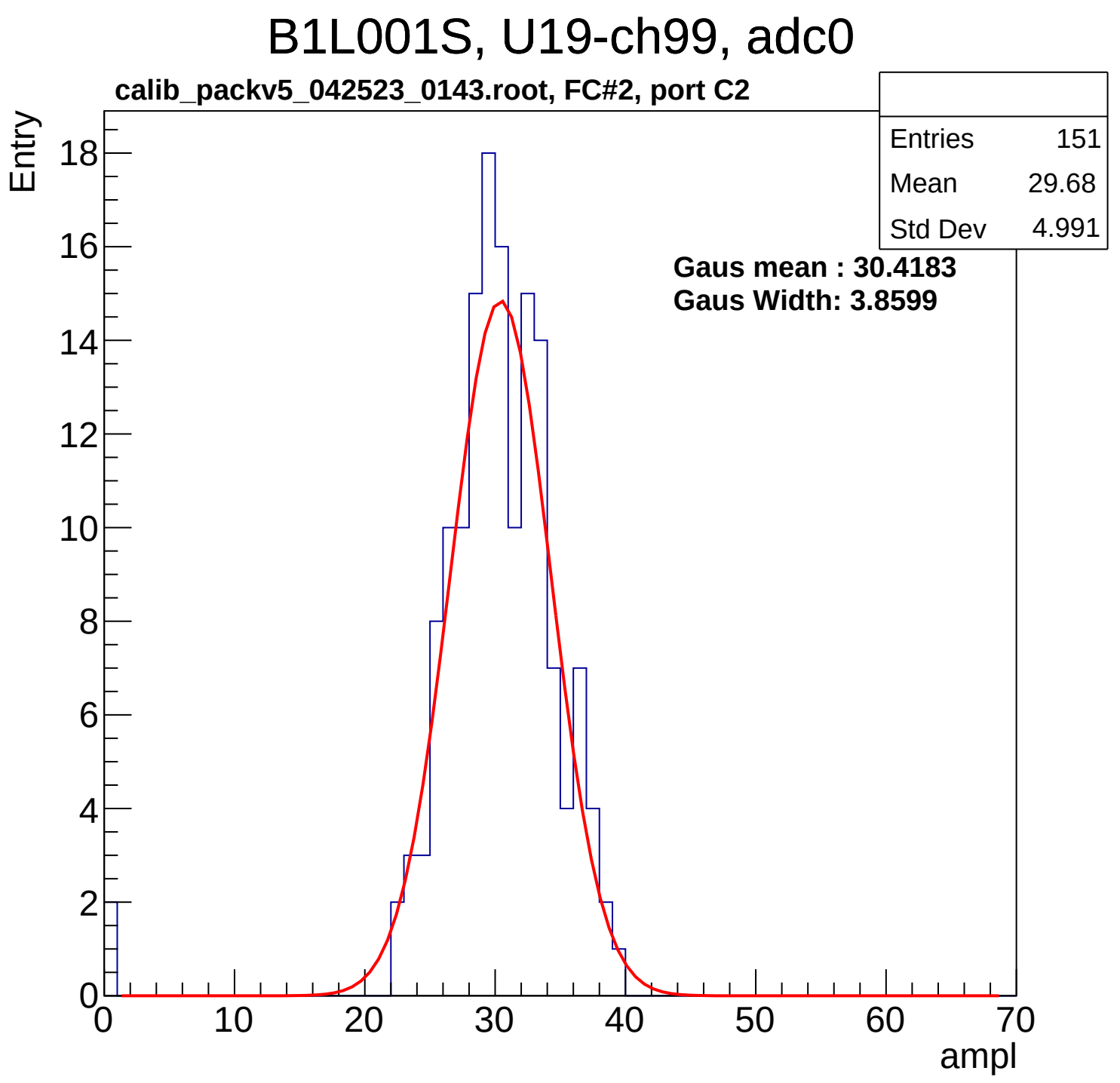
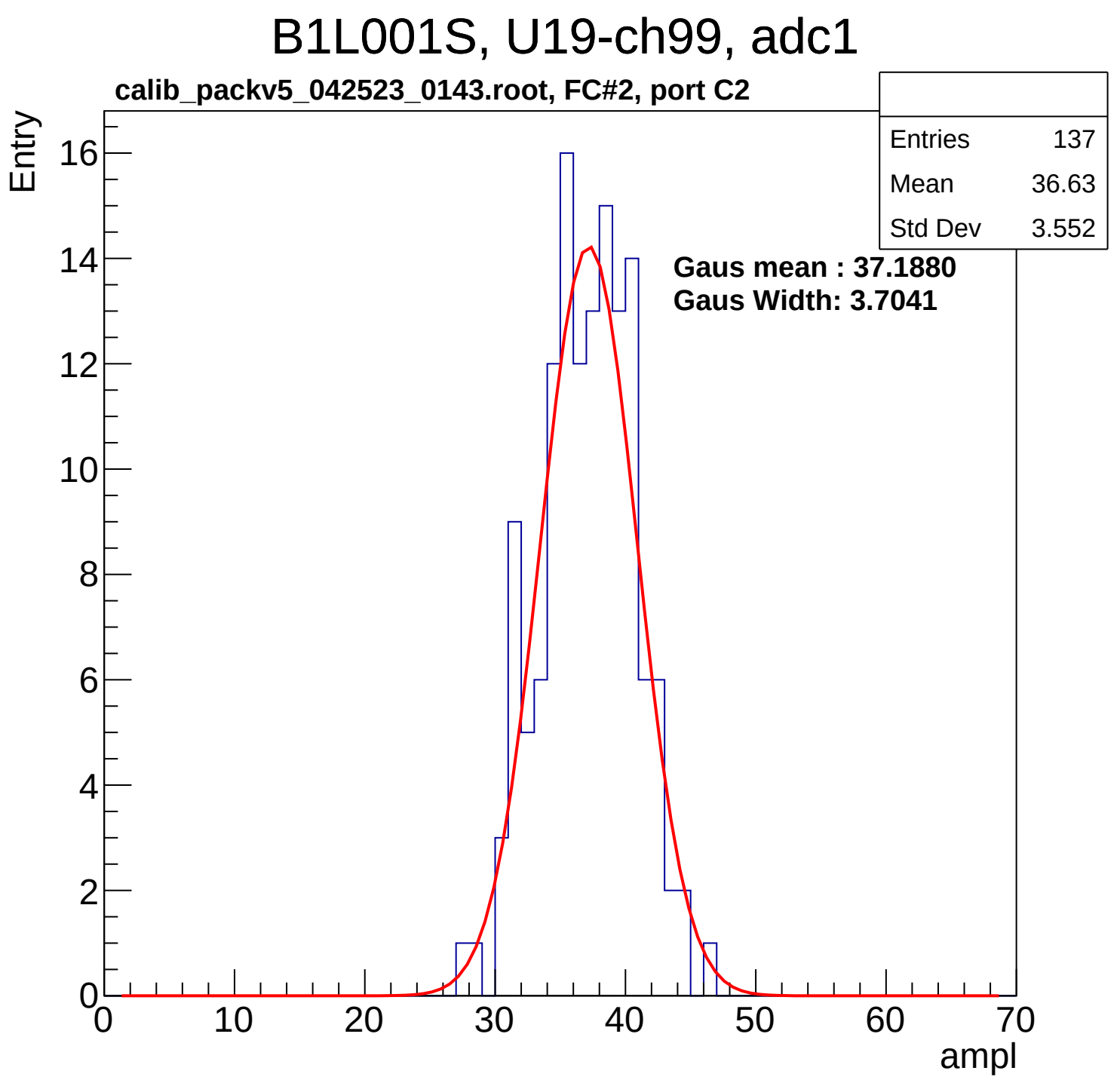
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch99, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 151
Mean 29.68
Std Dev 4.991
Gaus mean : 30.4183
Gaus Width: 3.8599
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70


B1L001S, U19-ch99, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 137
Mean 36.63
Std Dev 3.552
Gaus mean : 37.1880
Gaus Width: 3.7041
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
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40
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60
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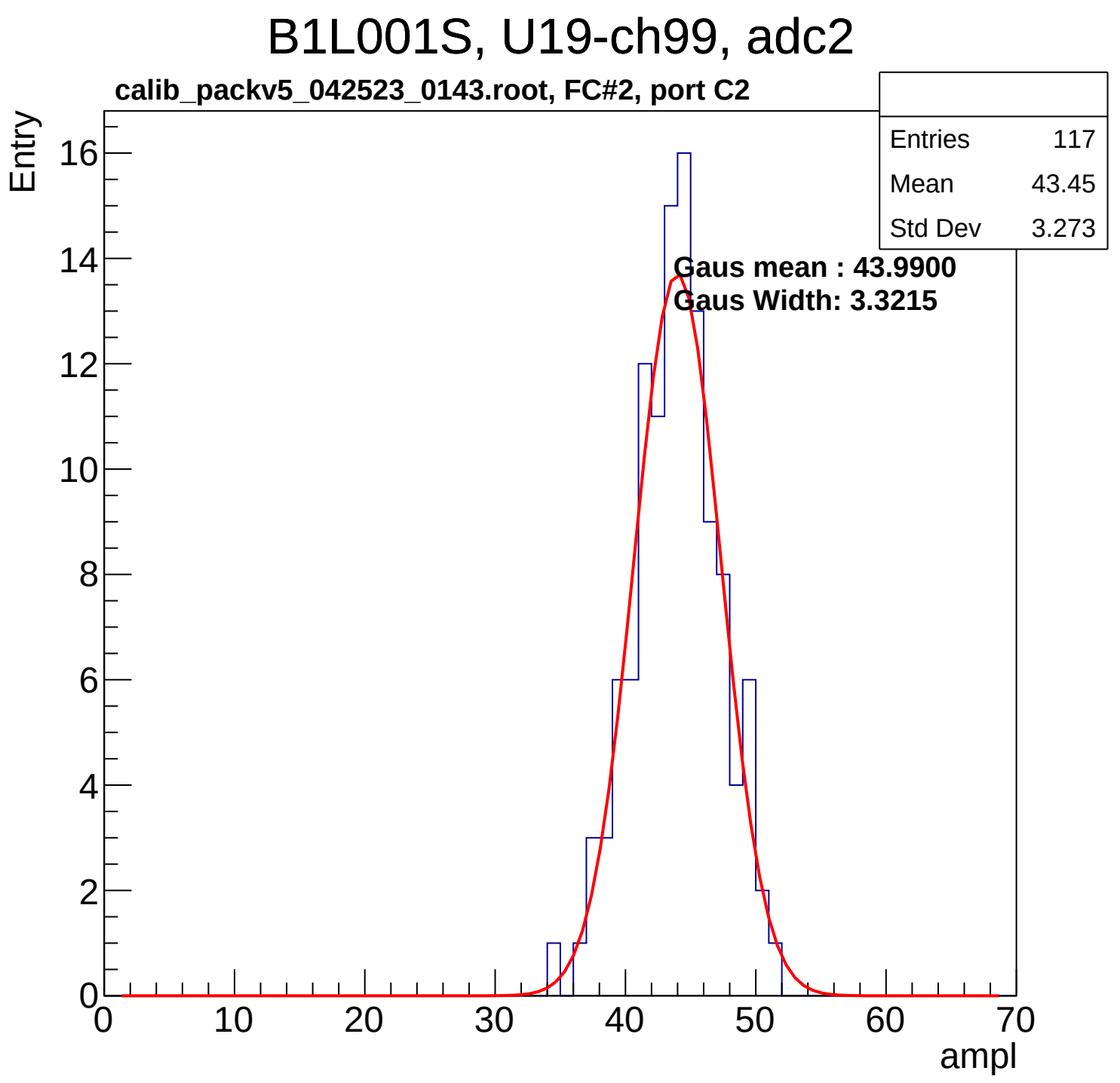
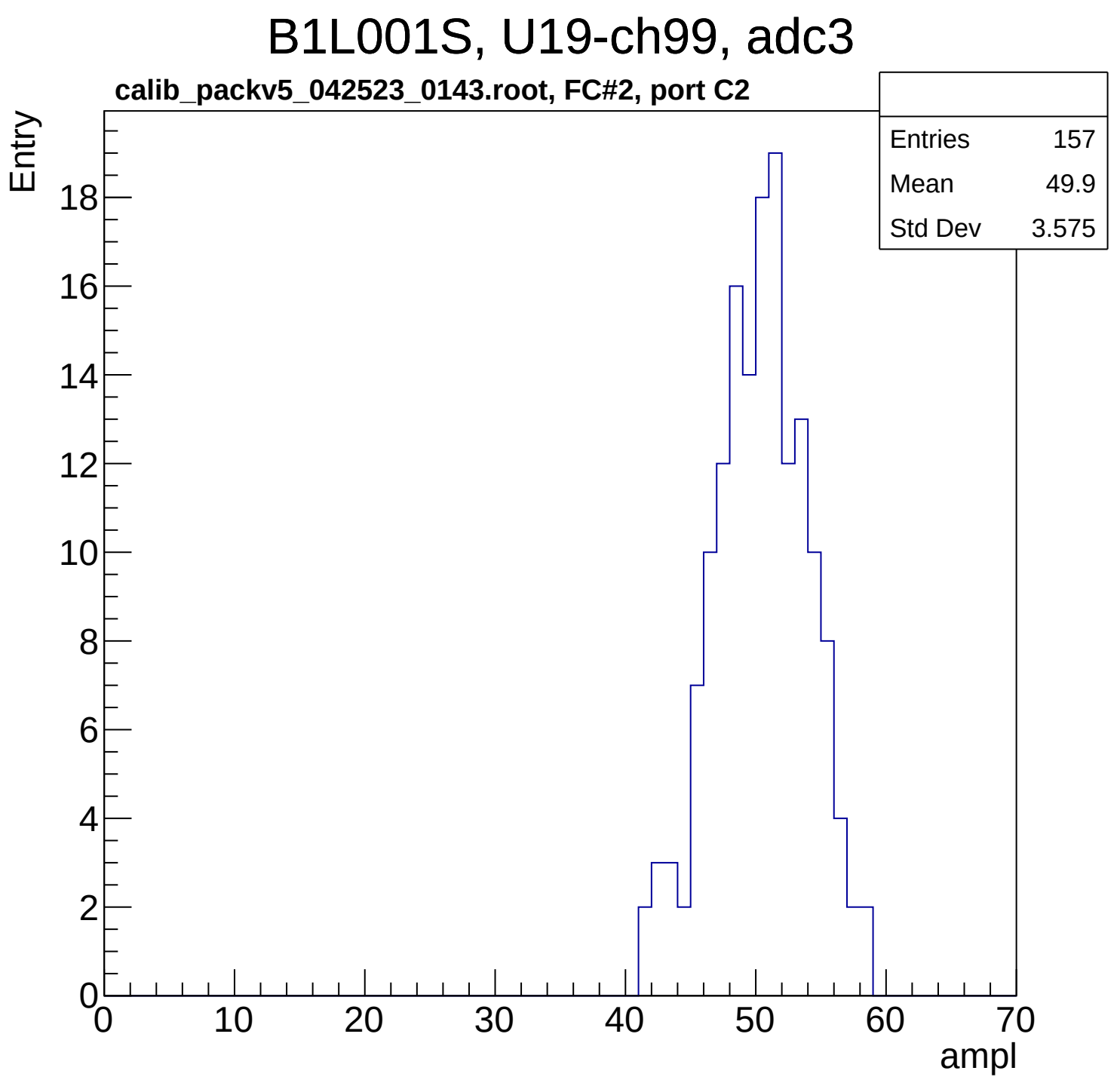
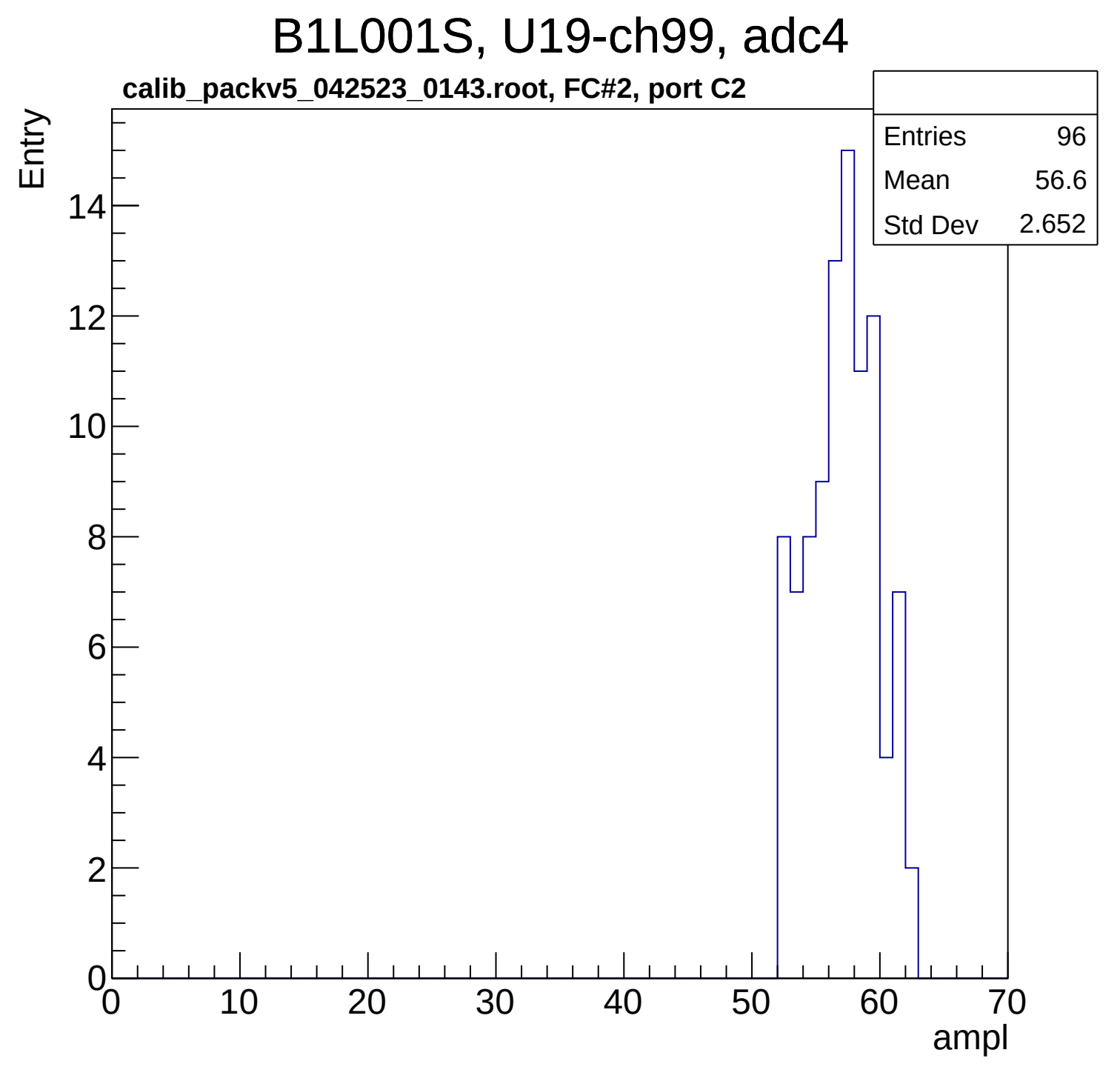

B1L001S, U19-ch99, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 117
Mean 43.45
Std Dev 3.273
Gaus mean : 43.9900
Gaus Width: 3.3215
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70


B1L001S, U19-ch99, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 157
Mean 49.9
Std Dev 3.575
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch99, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 96
Mean 56.6
Std Dev 2.652
Entry
ampl
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2
4
6
8
10
12
14
0
10
20
30
40
50
60
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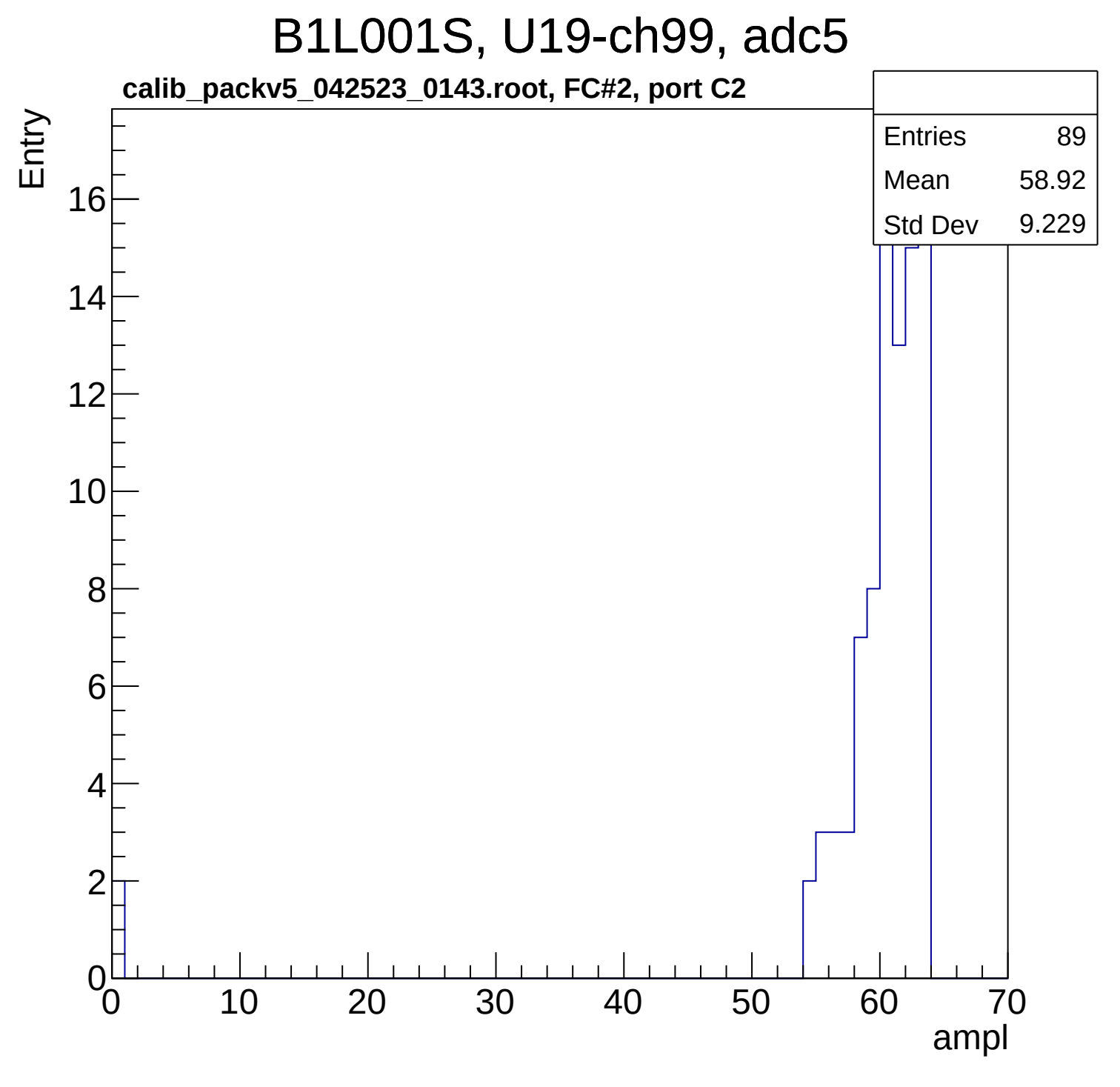
B1L001S, U19-ch99, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 89
Mean 58.92
Std Dev 9.229
Entry
ampl
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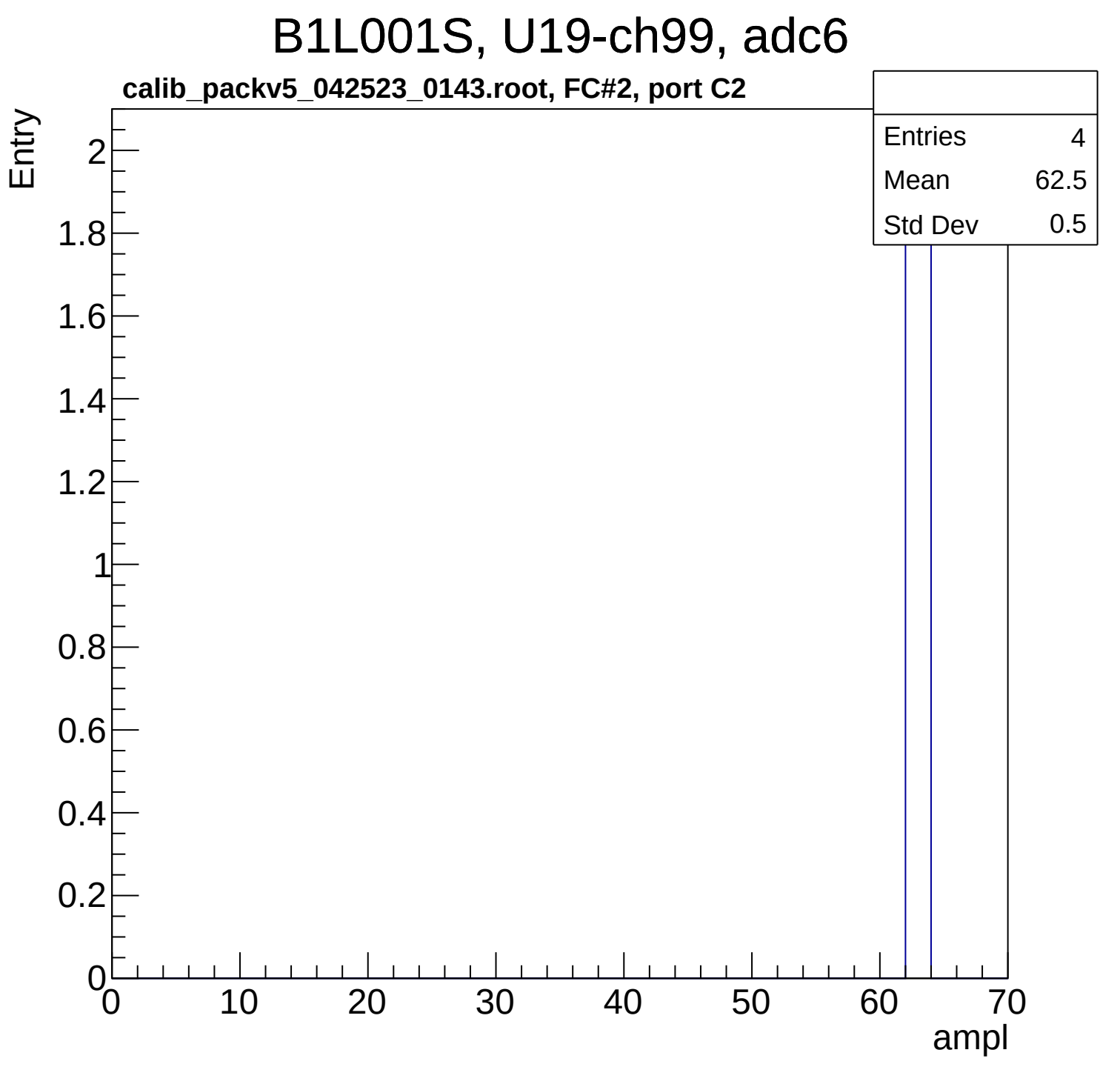
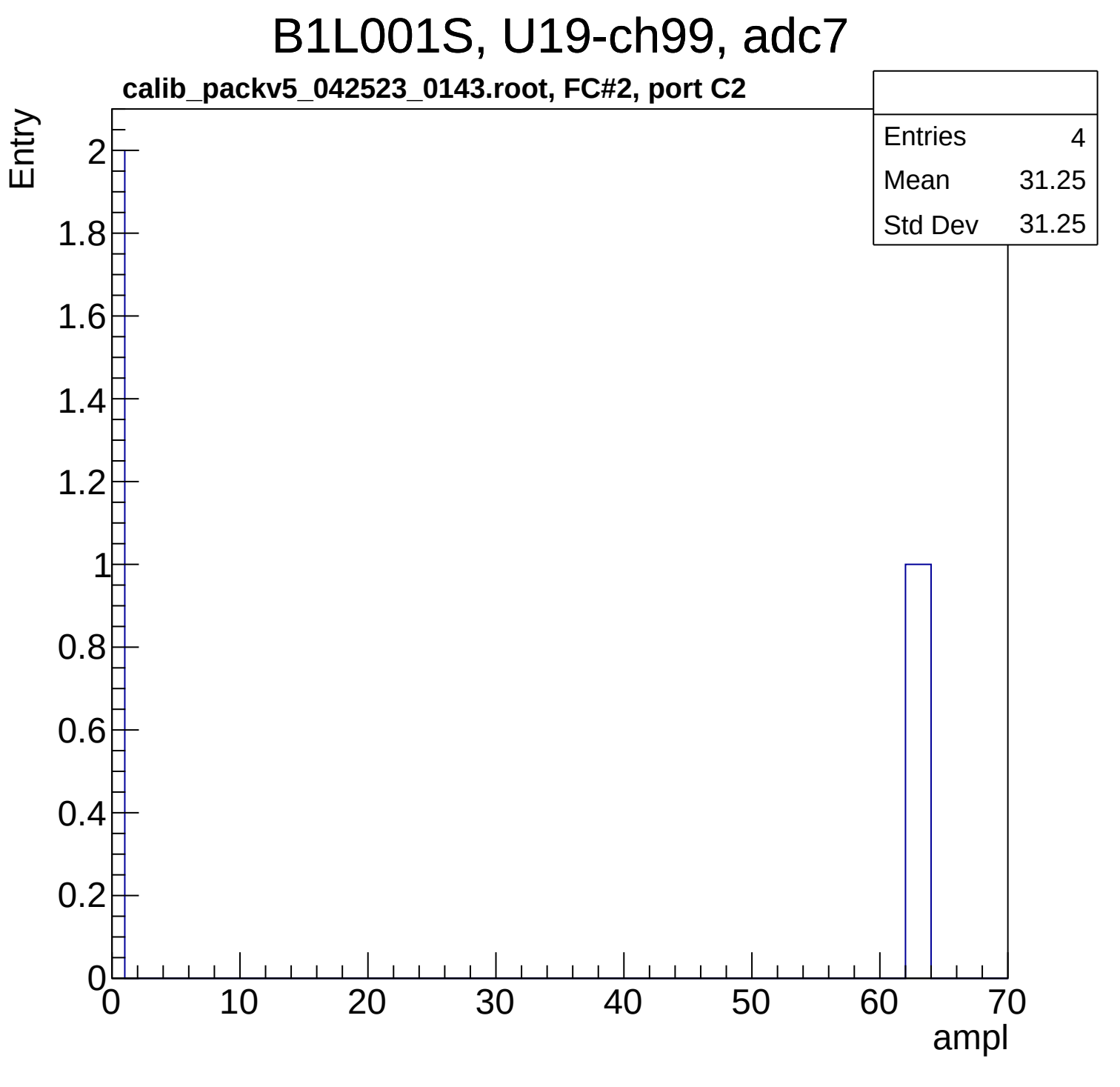
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70


B1L001S, U19-ch99, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 4
Mean 62.5
Std Dev 0.5
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L001S, U19-ch99, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 4
Mean 31.25
Std Dev 31.25
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
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40
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60
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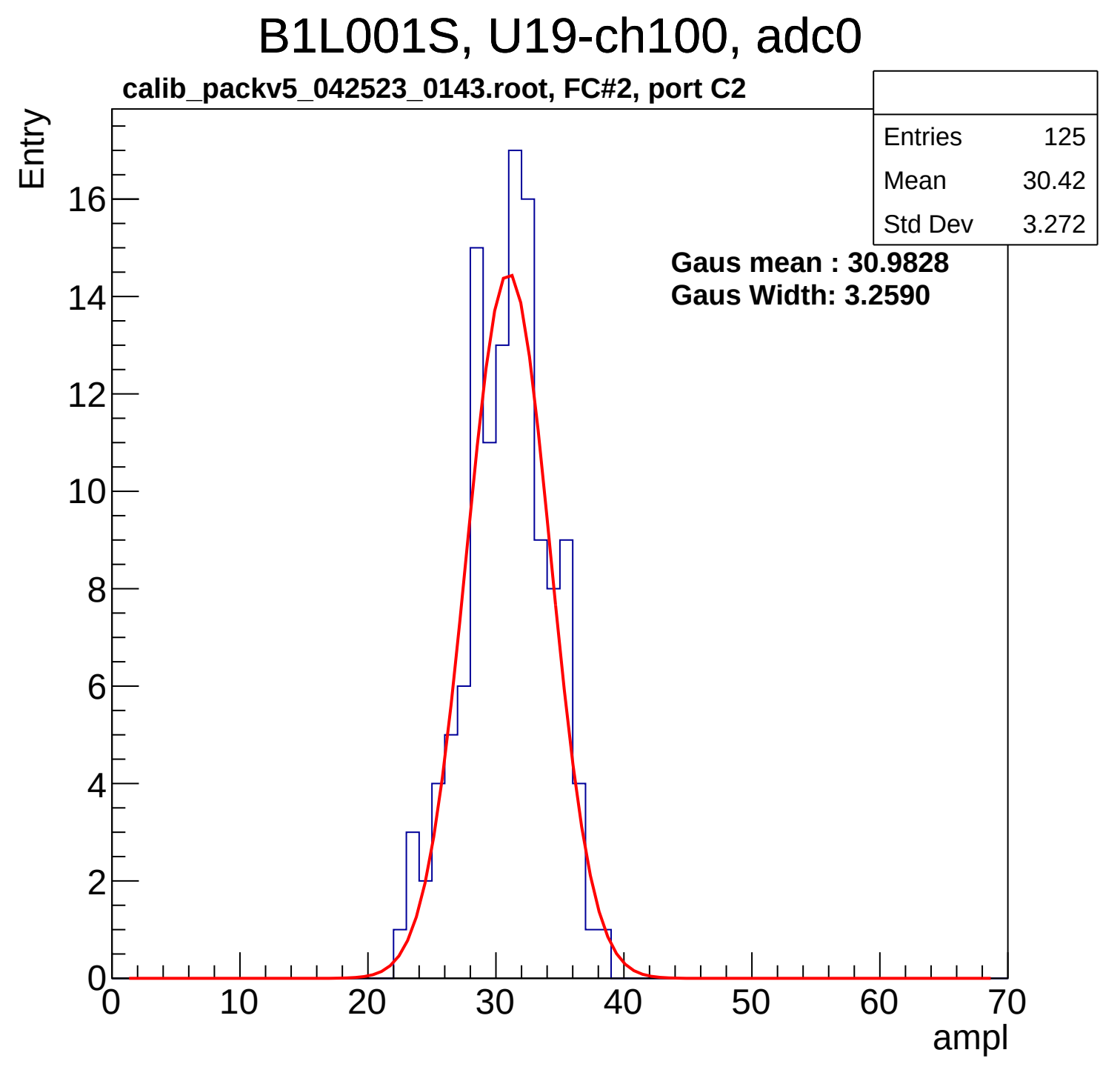
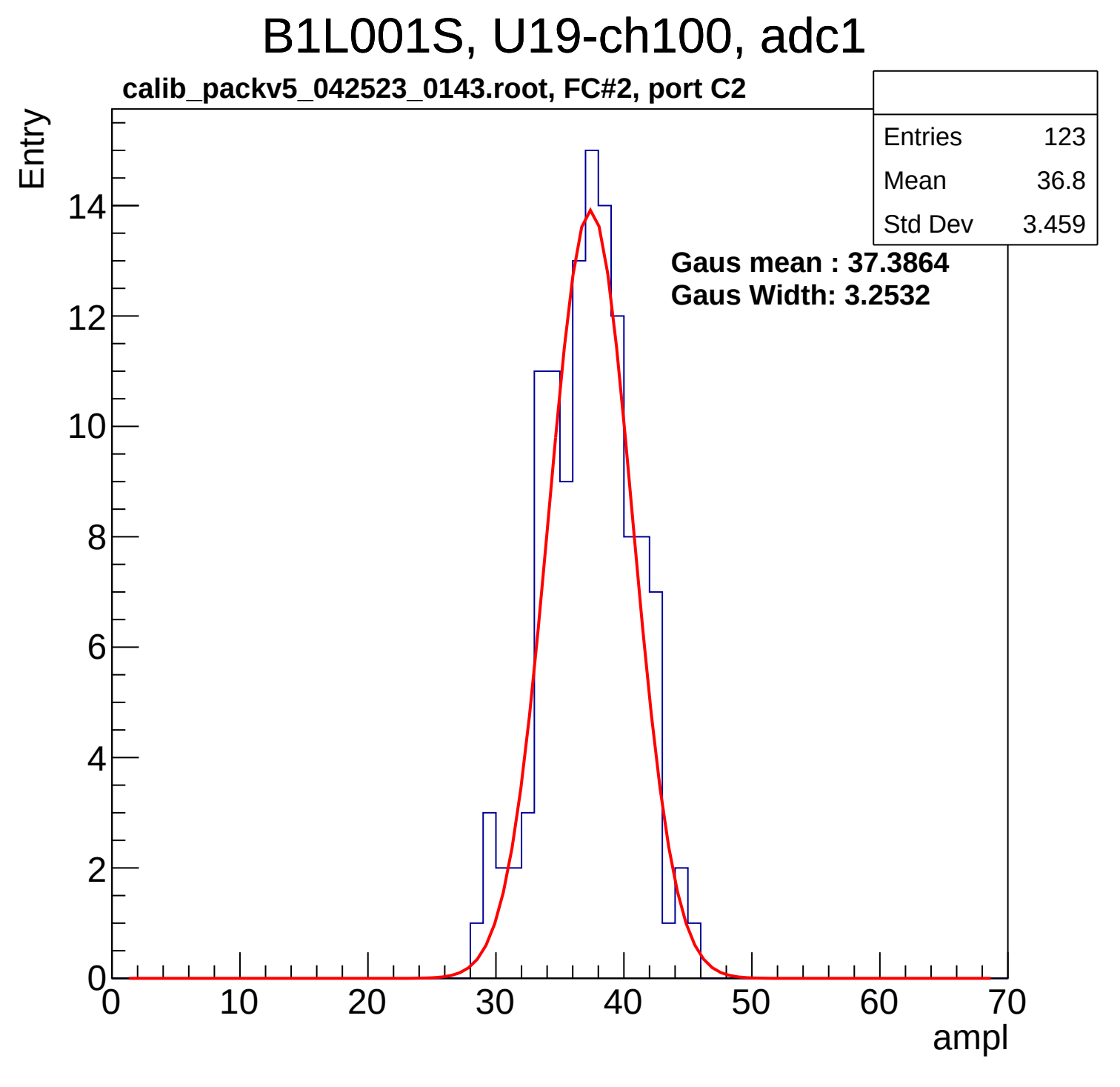
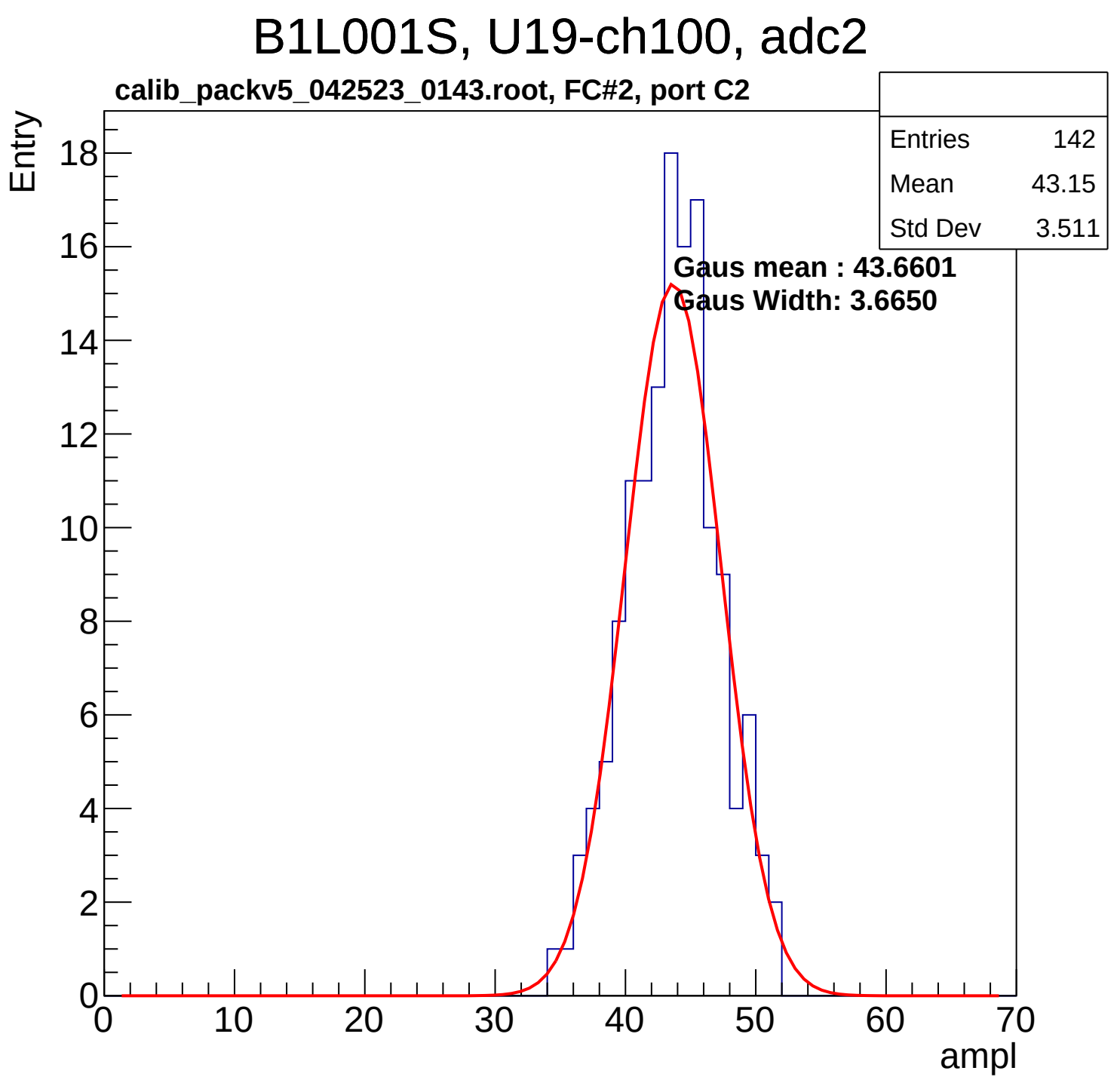

B1L001S, U19-ch100, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 125
Mean 30.42
Std Dev 3.272
Gaus mean : 30.9828
Gaus Width: 3.2590
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70


B1L001S, U19-ch100, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 123
Mean 36.8
Std Dev 3.459
Gaus mean : 37.3864
Gaus Width: 3.2532
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L001S, U19-ch100, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 142
Mean 43.15
Std Dev 3.511
Gaus mean : 43.6601
Gaus Width: 3.6650
Entry
ampl
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2
4
6
8
10
12
14
16
18
0
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20
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60
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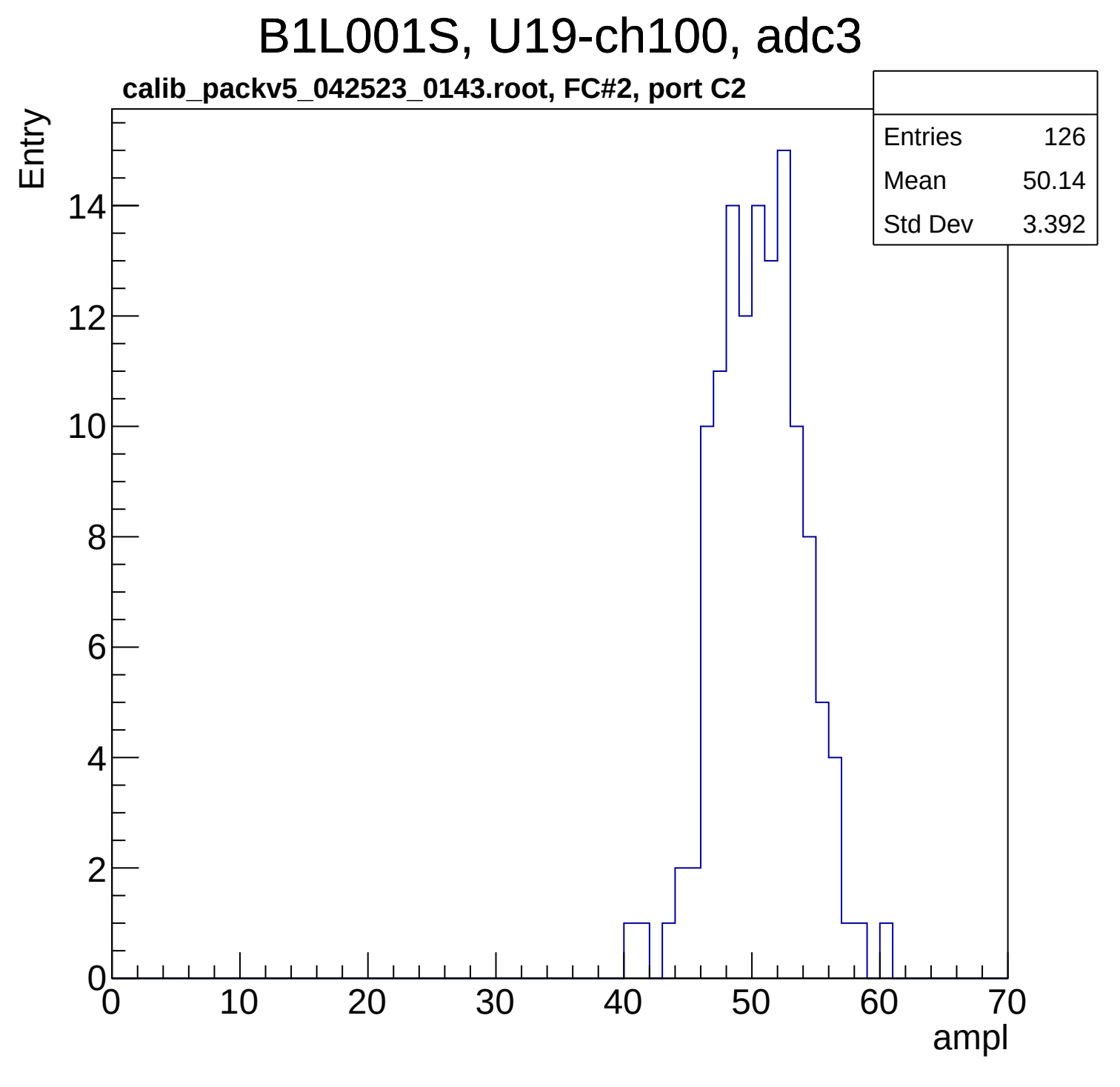
B1L001S, U19-ch100, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 126
Mean 50.14
Std Dev 3.392
Entry
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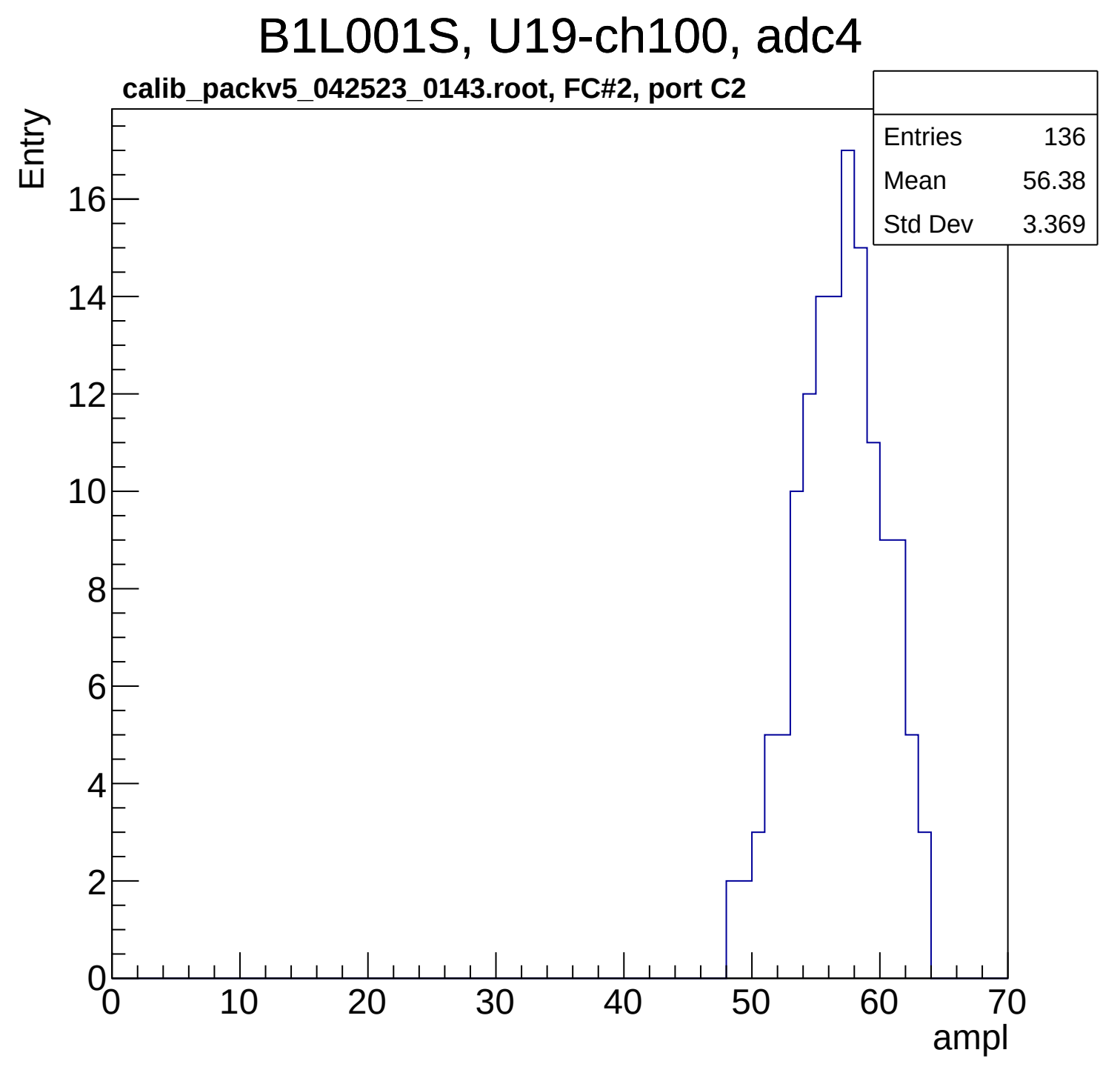
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch100, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 136
Mean 56.38
Std Dev 3.369
Entry
ampl
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2
4
6
8
10
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14
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0
10
20
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40
50
60
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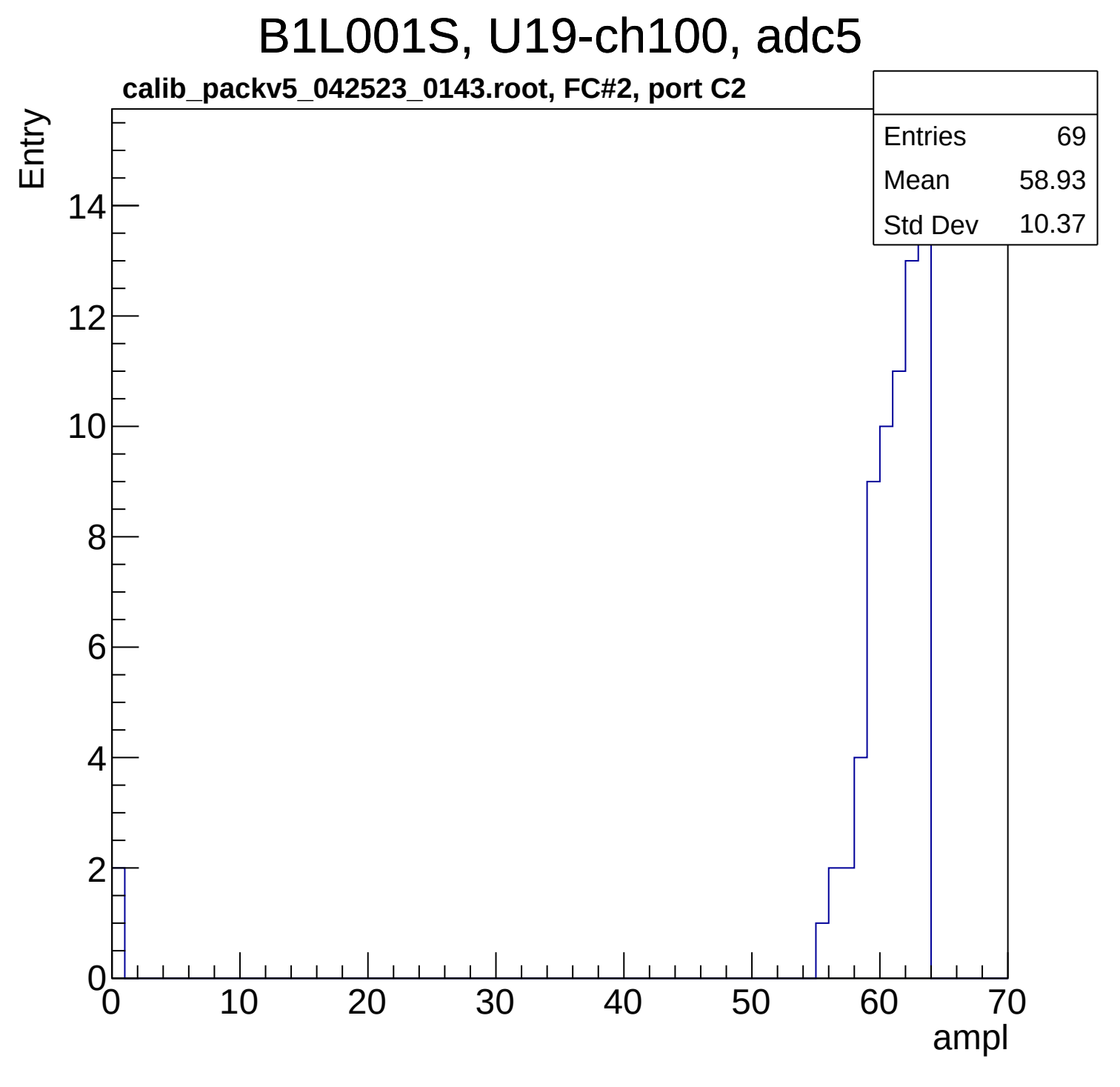
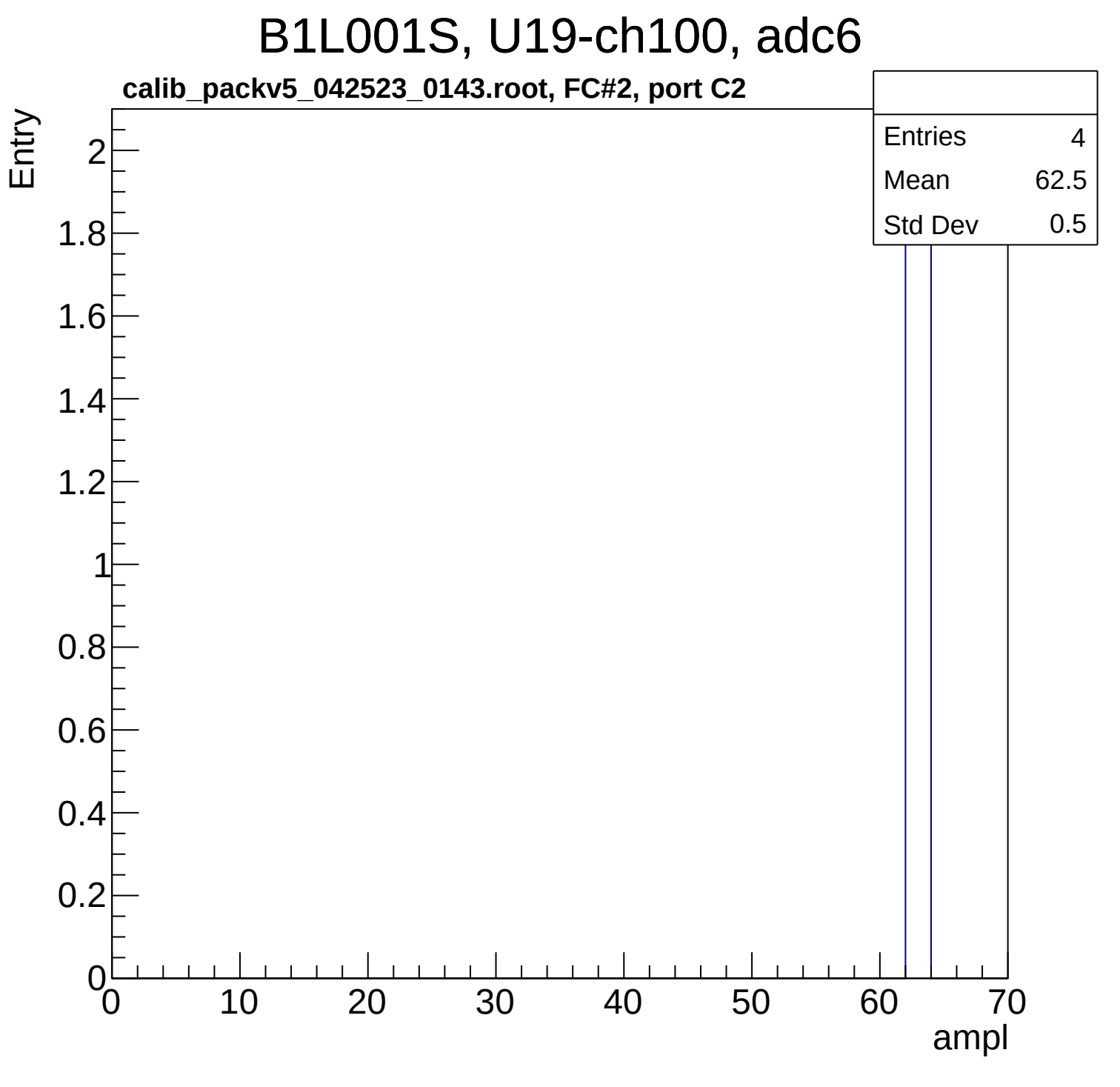
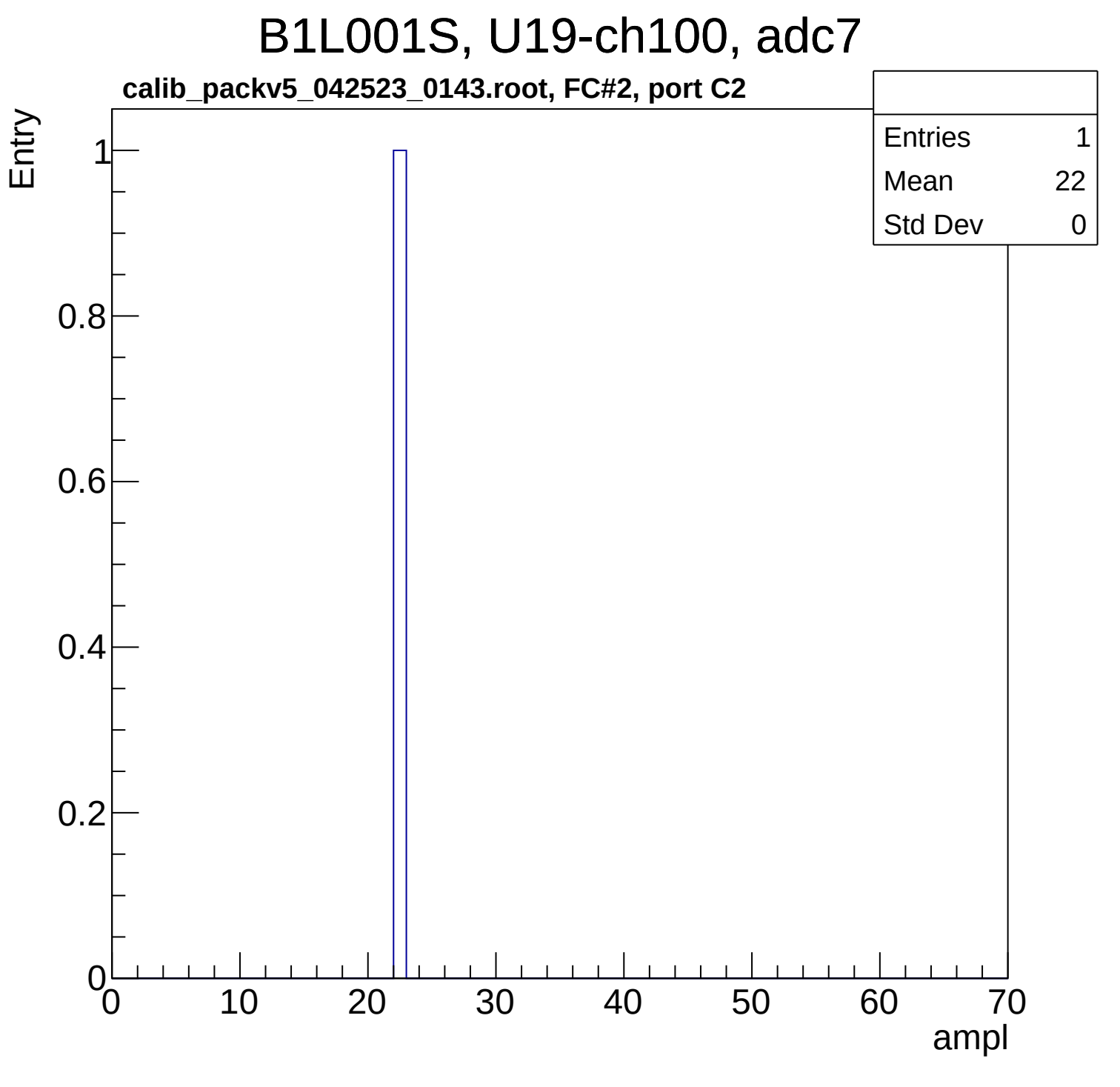

B1L001S, U19-ch100, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 69
Mean 58.93
Std Dev 10.37
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch100, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 4
Mean 62.5
Std Dev 0.5
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L001S, U19-ch100, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 22
Std Dev 0
Entry
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0.6
0.4
0.2
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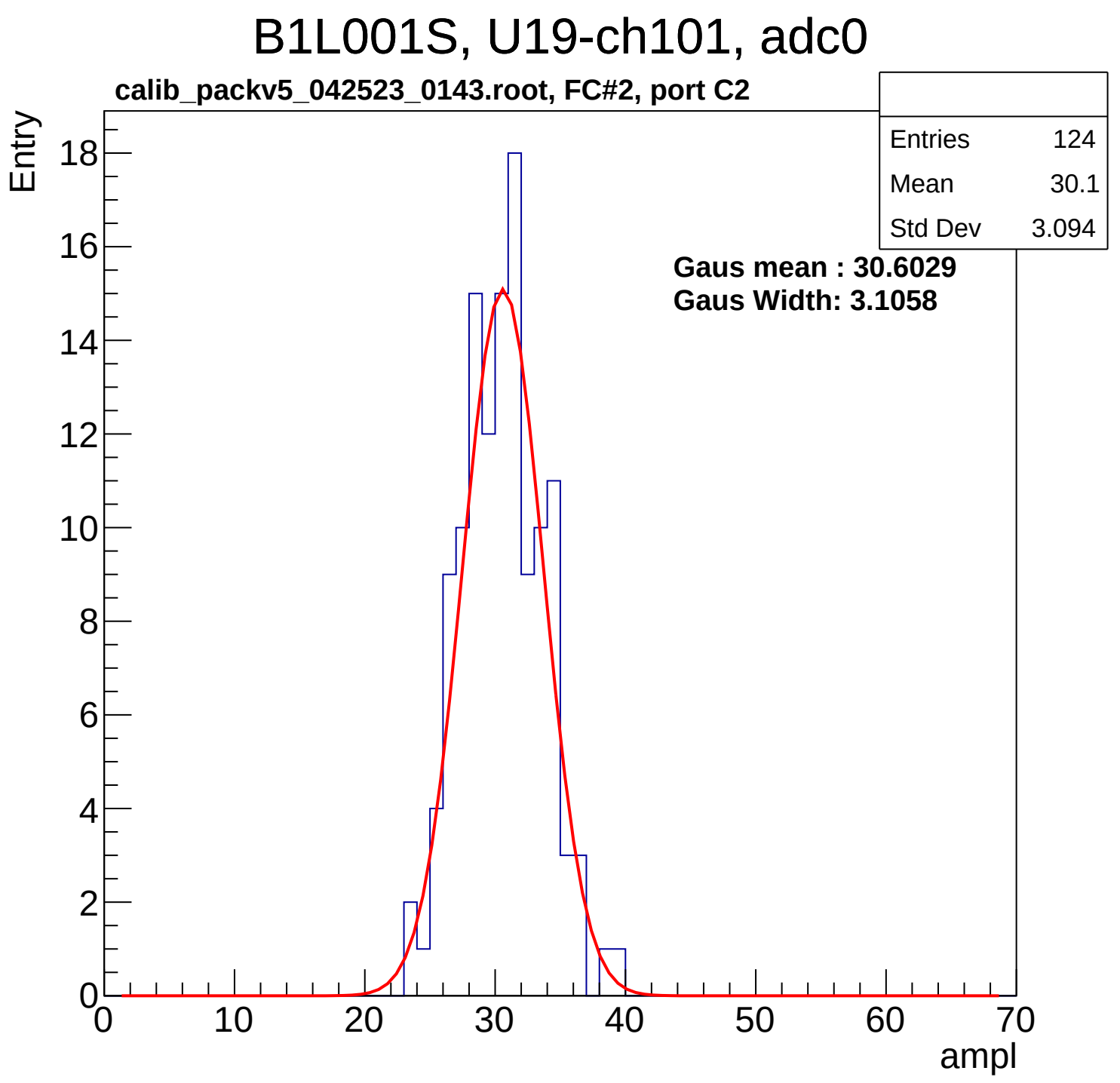
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch101, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 124
Mean 30.1
Std Dev 3.094
Gaus mean : 30.6029
Gaus Width: 3.1058
Entry
ampl
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6
8
10
12
14
16
18
0
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40
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60
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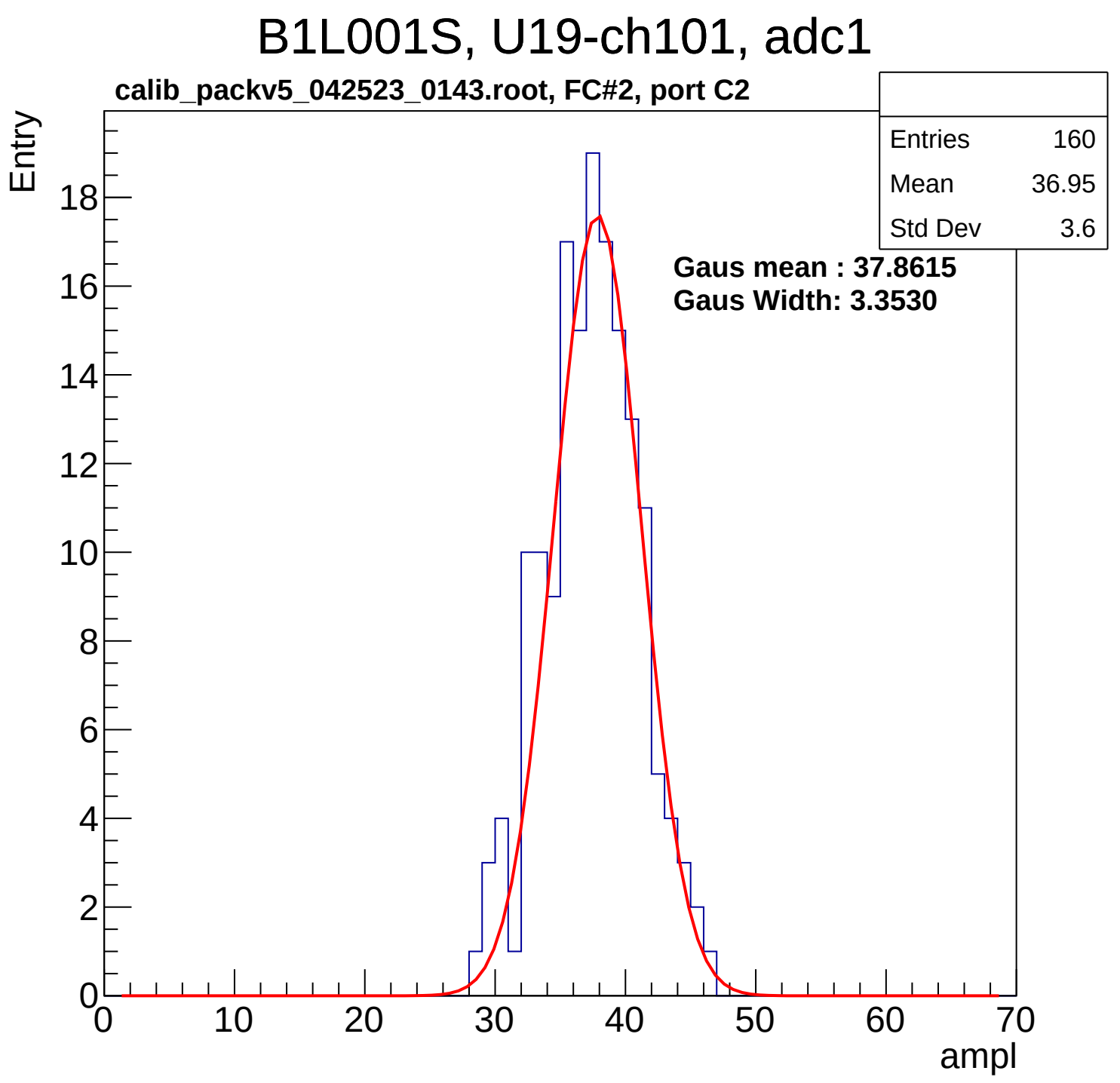
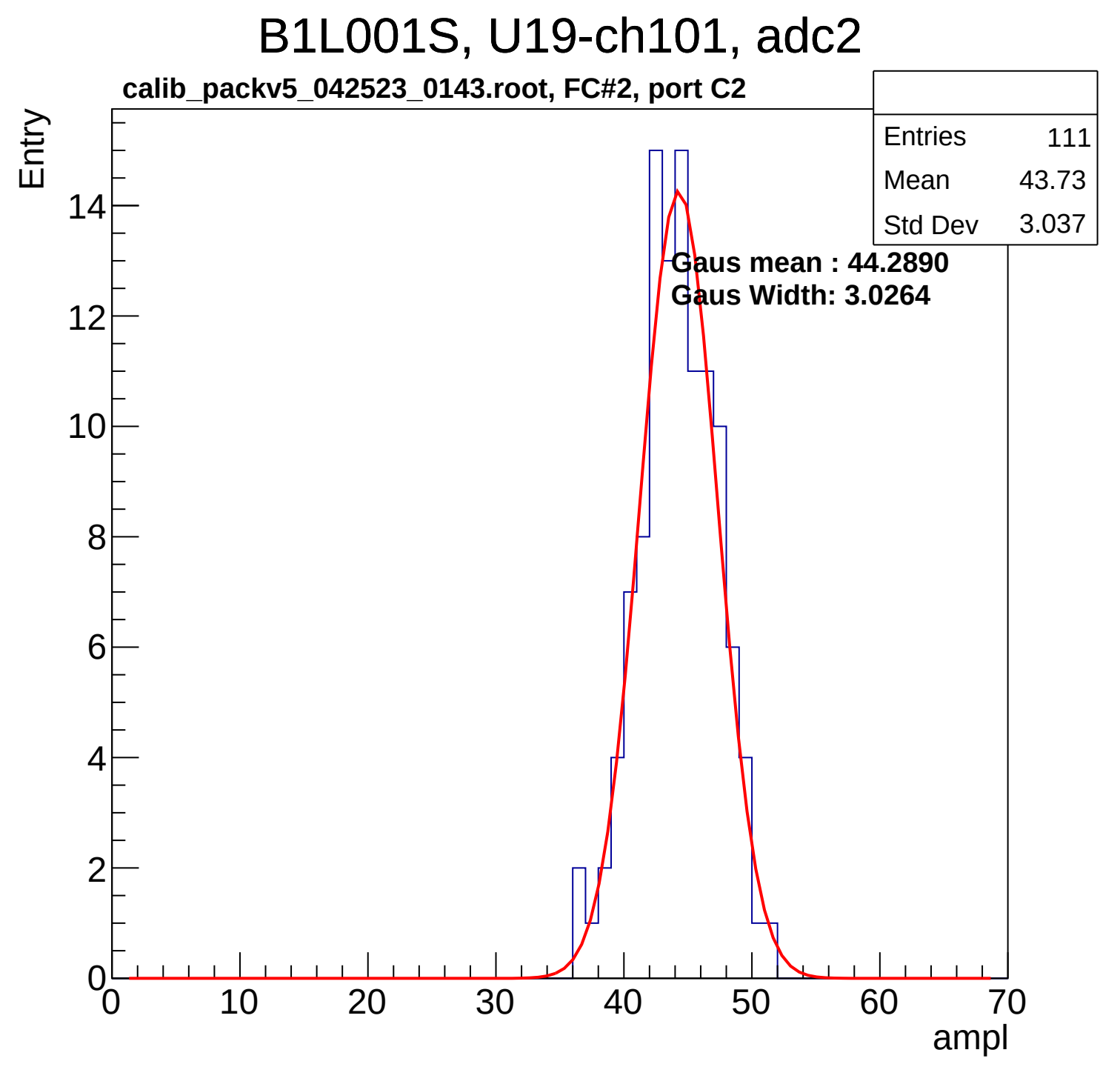

B1L001S, U19-ch101, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 160
Mean 36.95
Std Dev 3.6
Gaus mean : 37.8615
Gaus Width: 3.3530
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70


B1L001S, U19-ch101, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 111
Mean 43.73
Std Dev 3.037
Gaus mean : 44.2890
Gaus Width: 3.0264
Entry
ampl
0
2
4
6
8
10
12
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0
10
20
30
40
50
60
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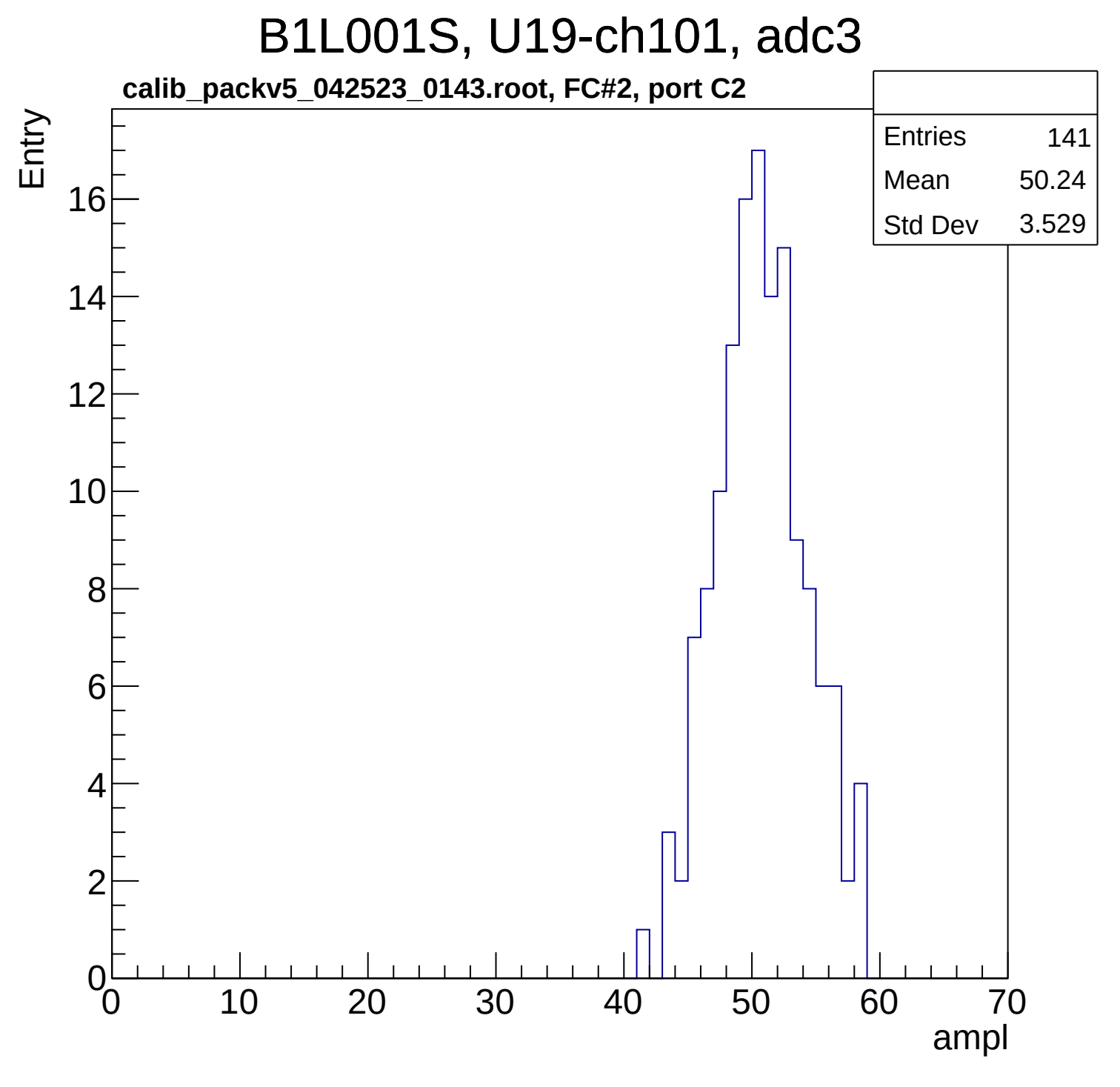
B1L001S, U19-ch101, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 141
Mean 50.24
Std Dev 3.529
Entry
ampl
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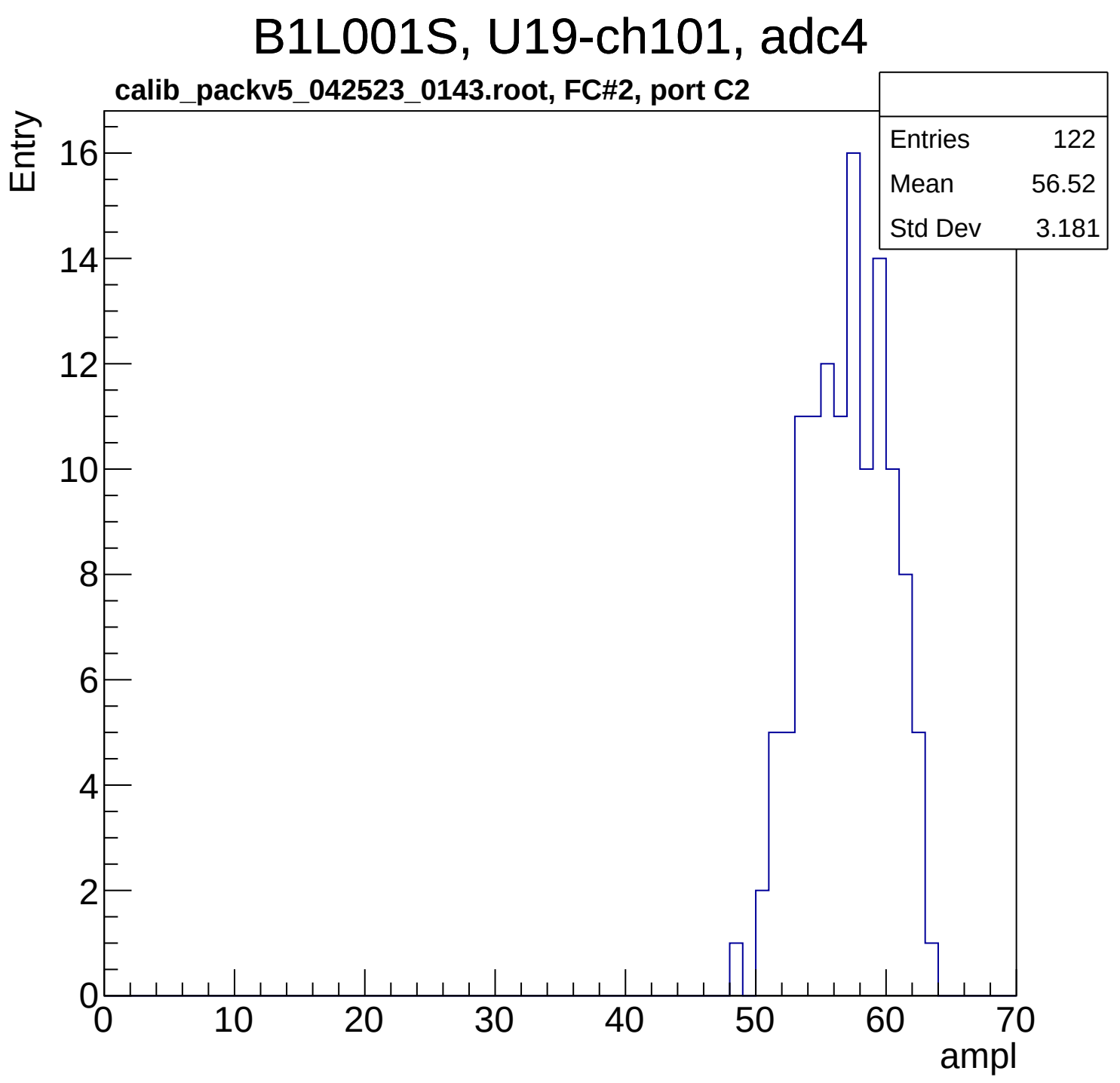
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70


B1L001S, U19-ch101, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 122
Mean 56.52
Std Dev 3.181
Entry
ampl
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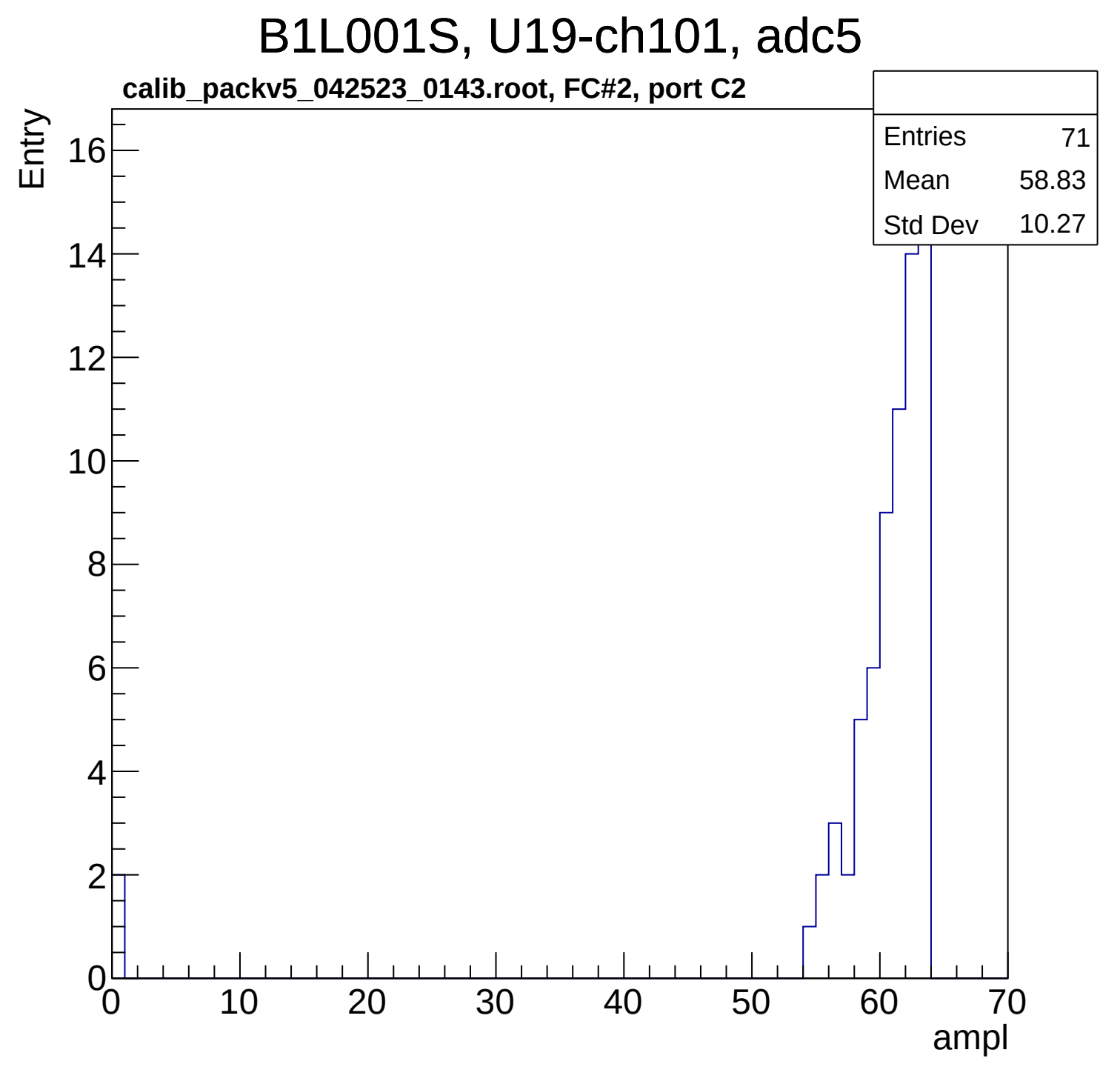
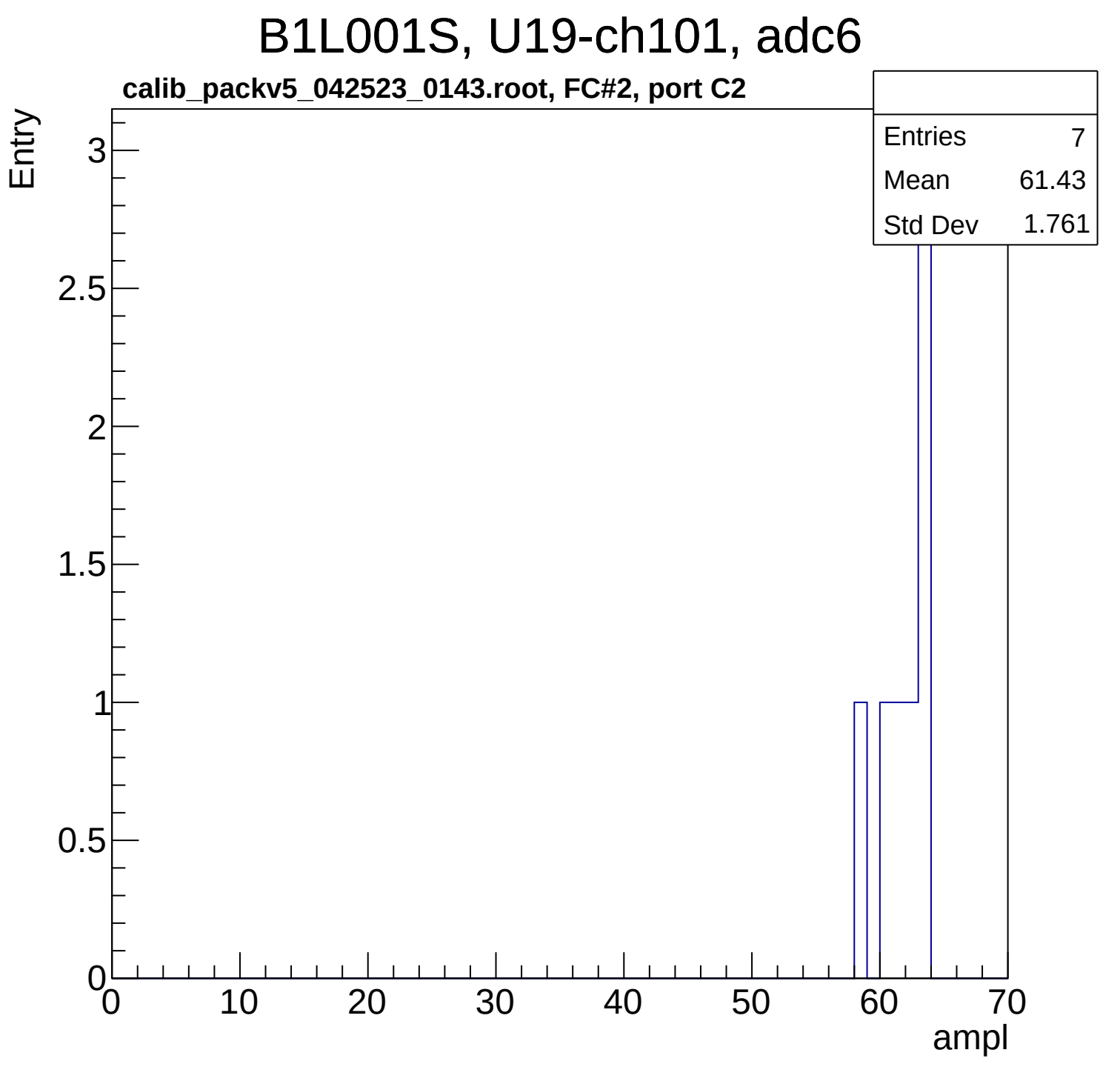
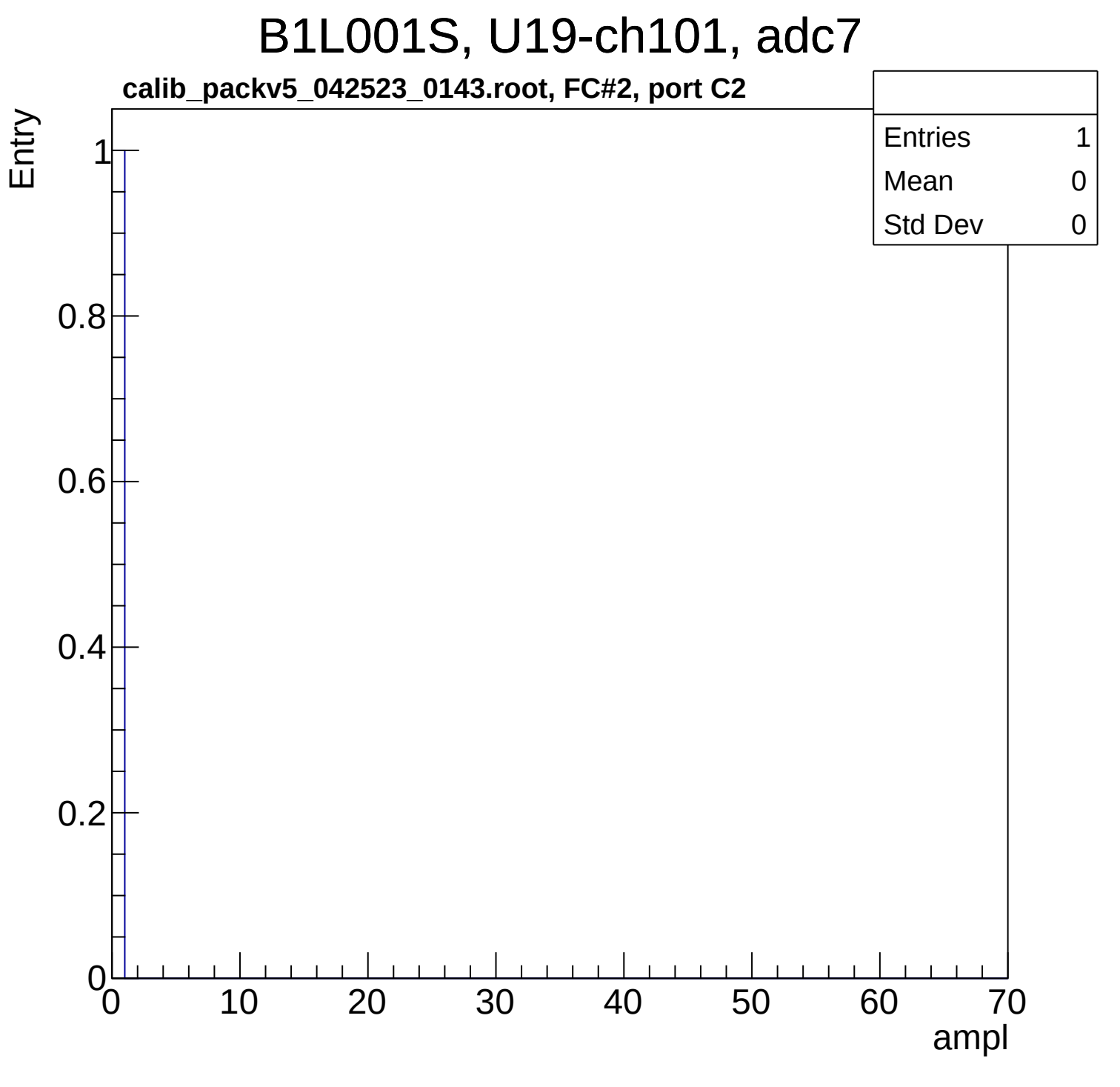
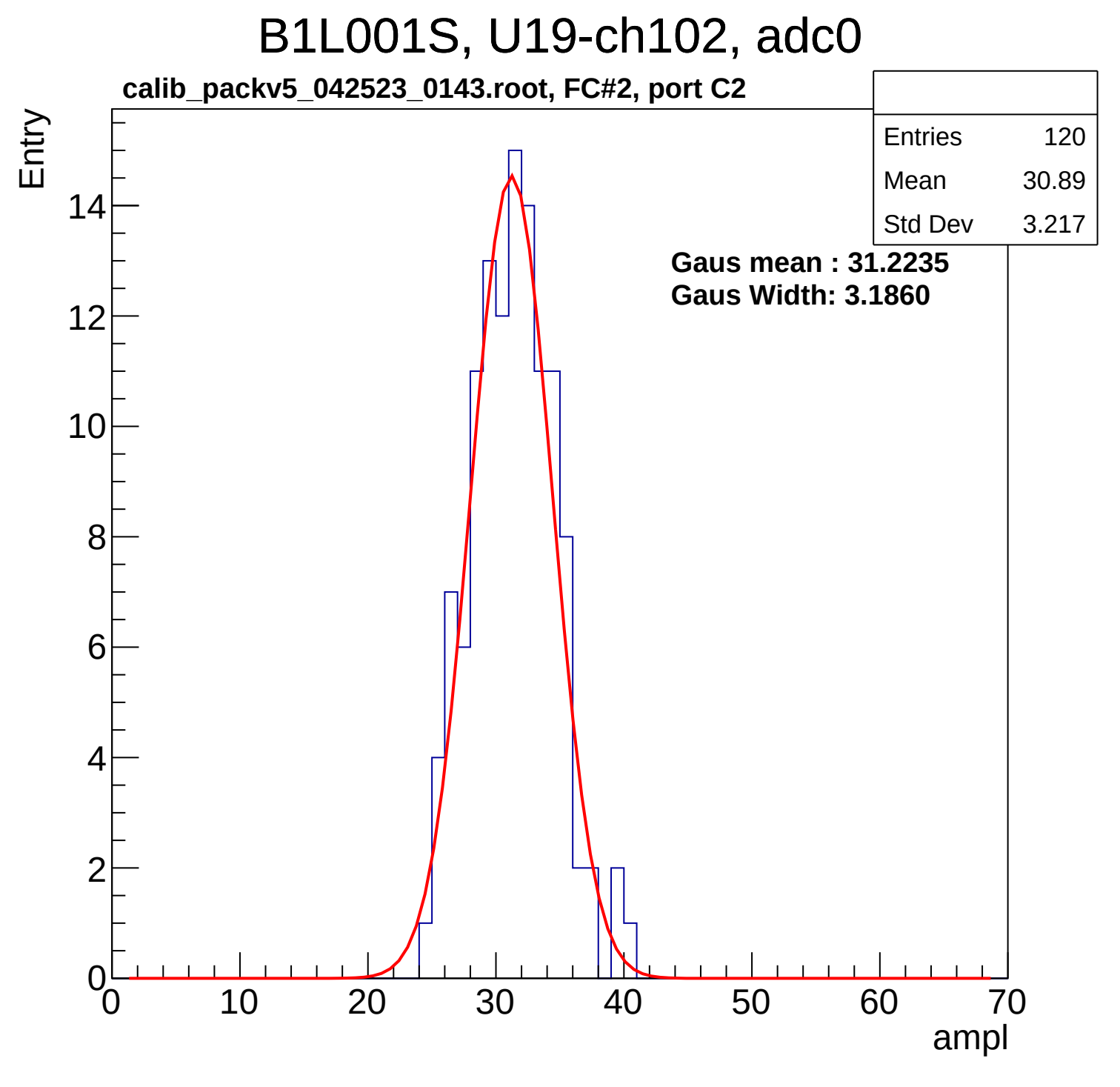
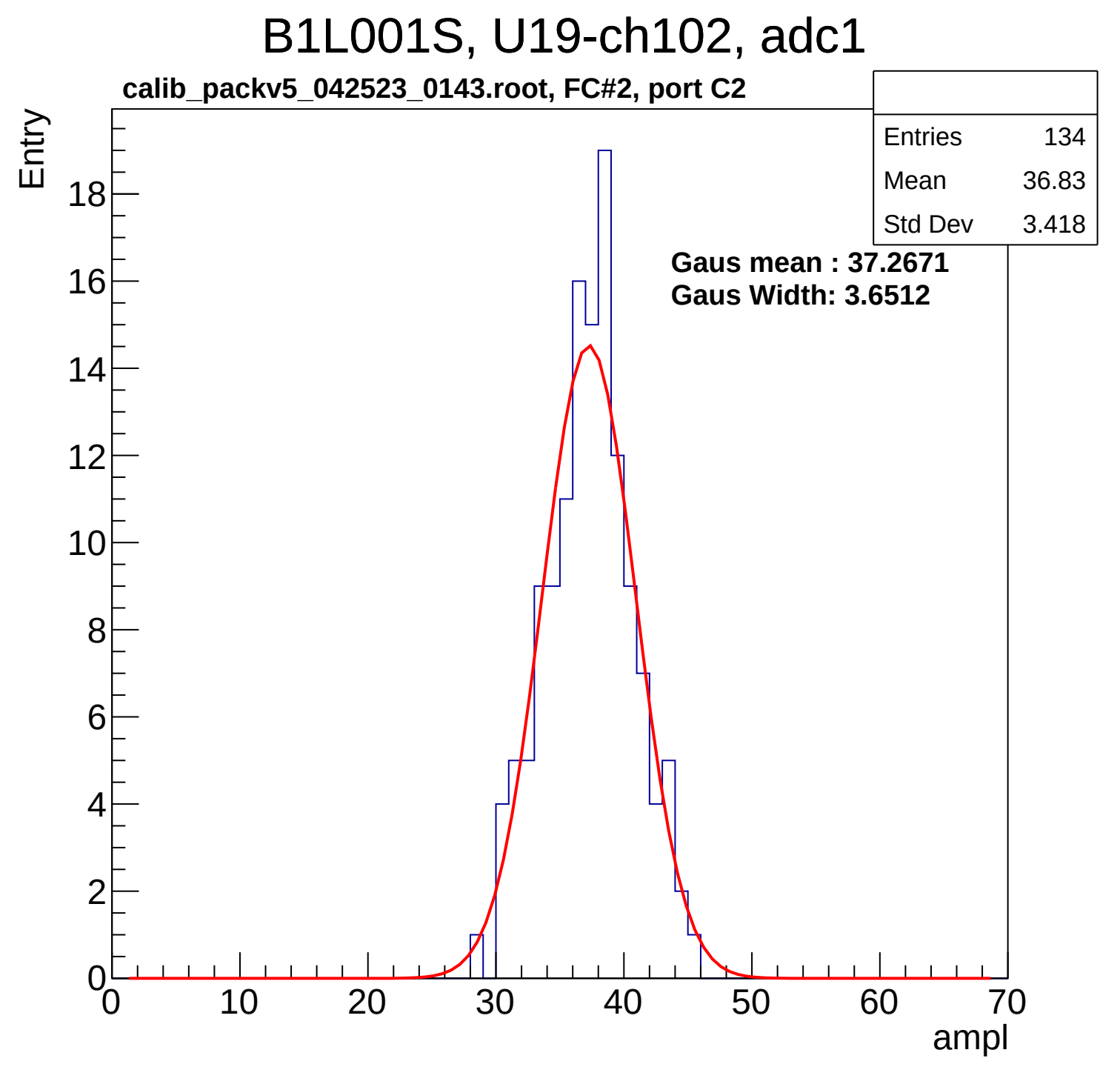
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

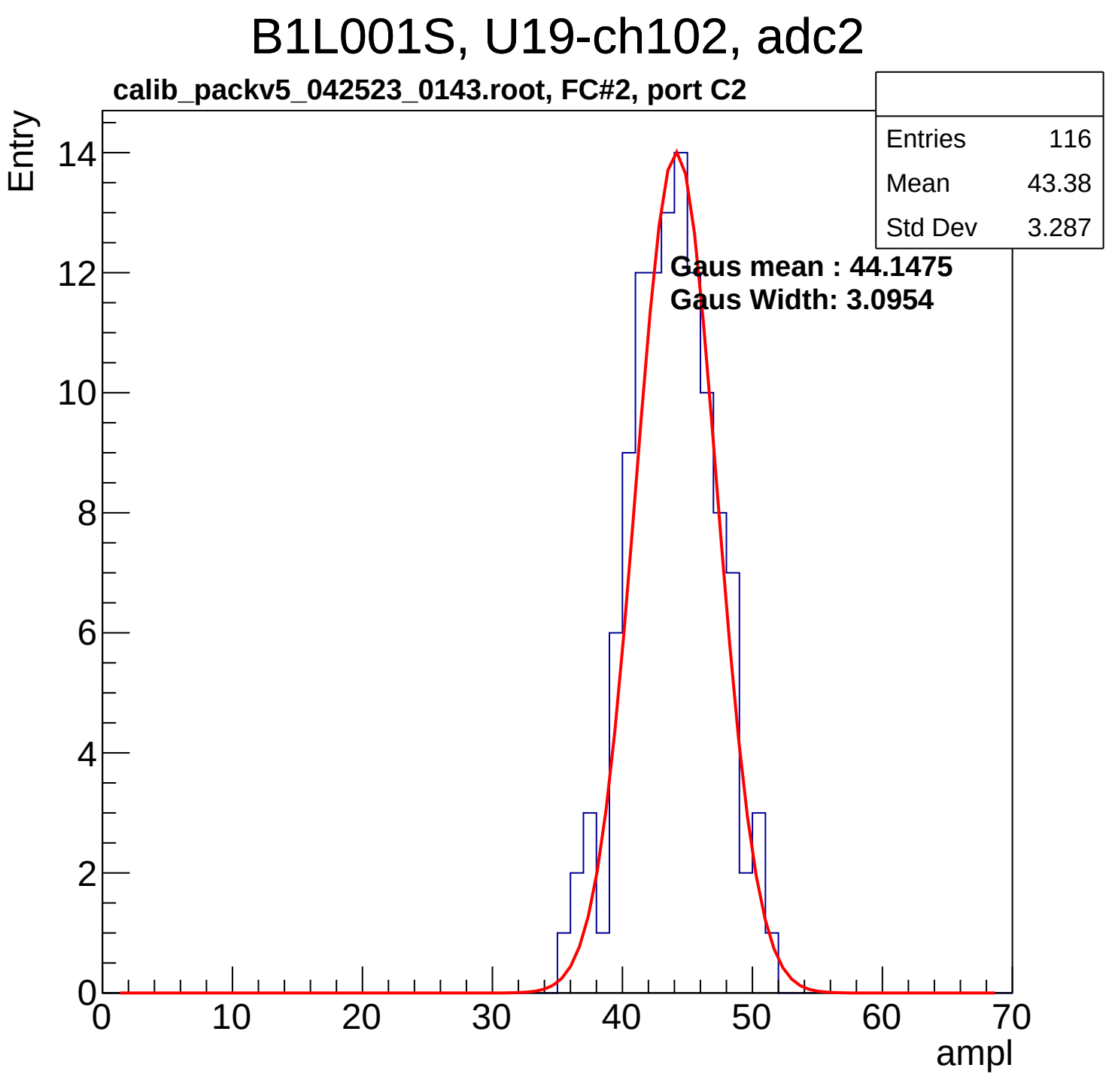

B1L001S, U19-ch101, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 71
Mean 58.83
Std Dev 10.27
Entry
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl

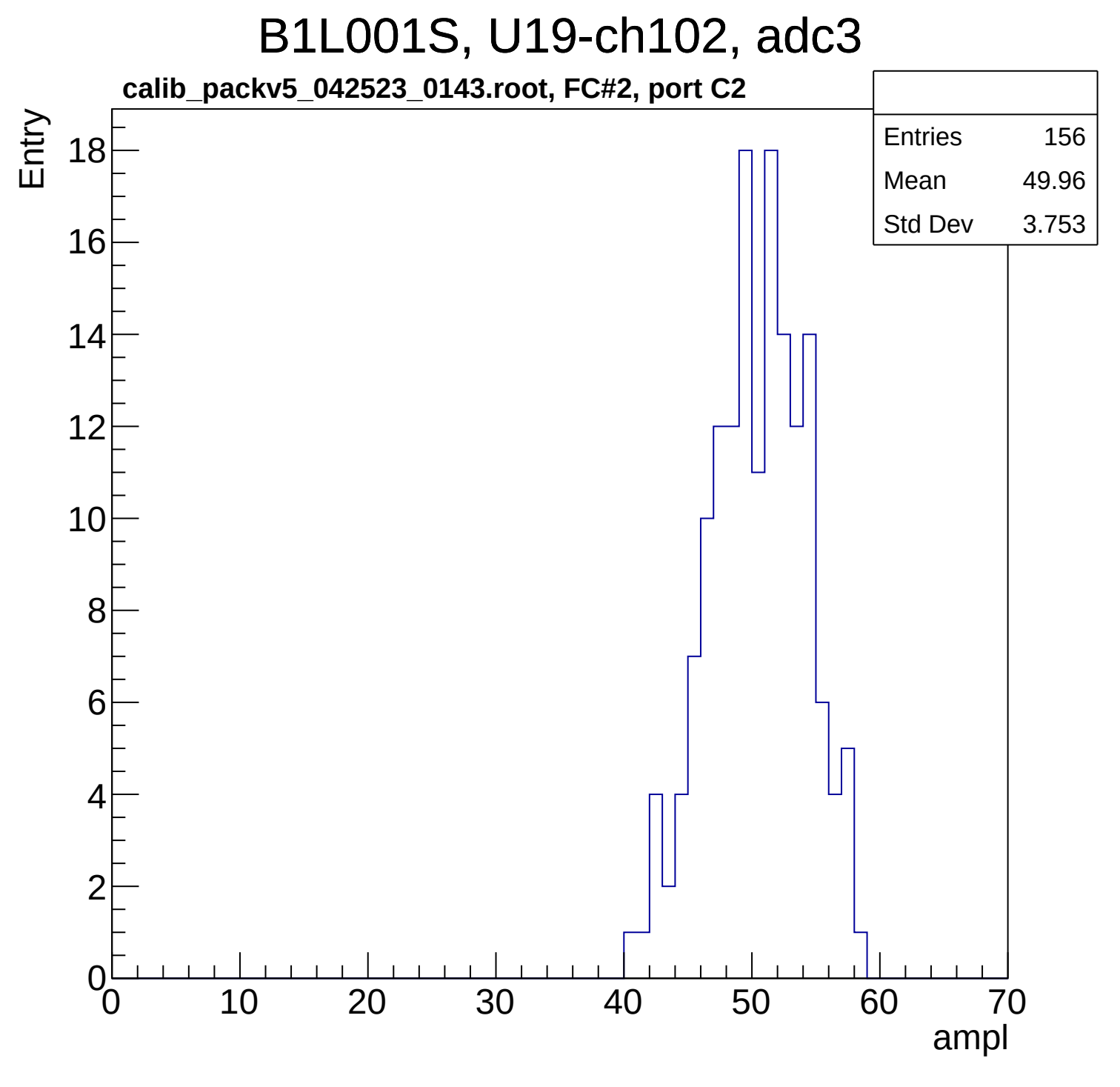

B1L001S, U19-ch101, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 7
Mean 61.43
Std Dev 1.761
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

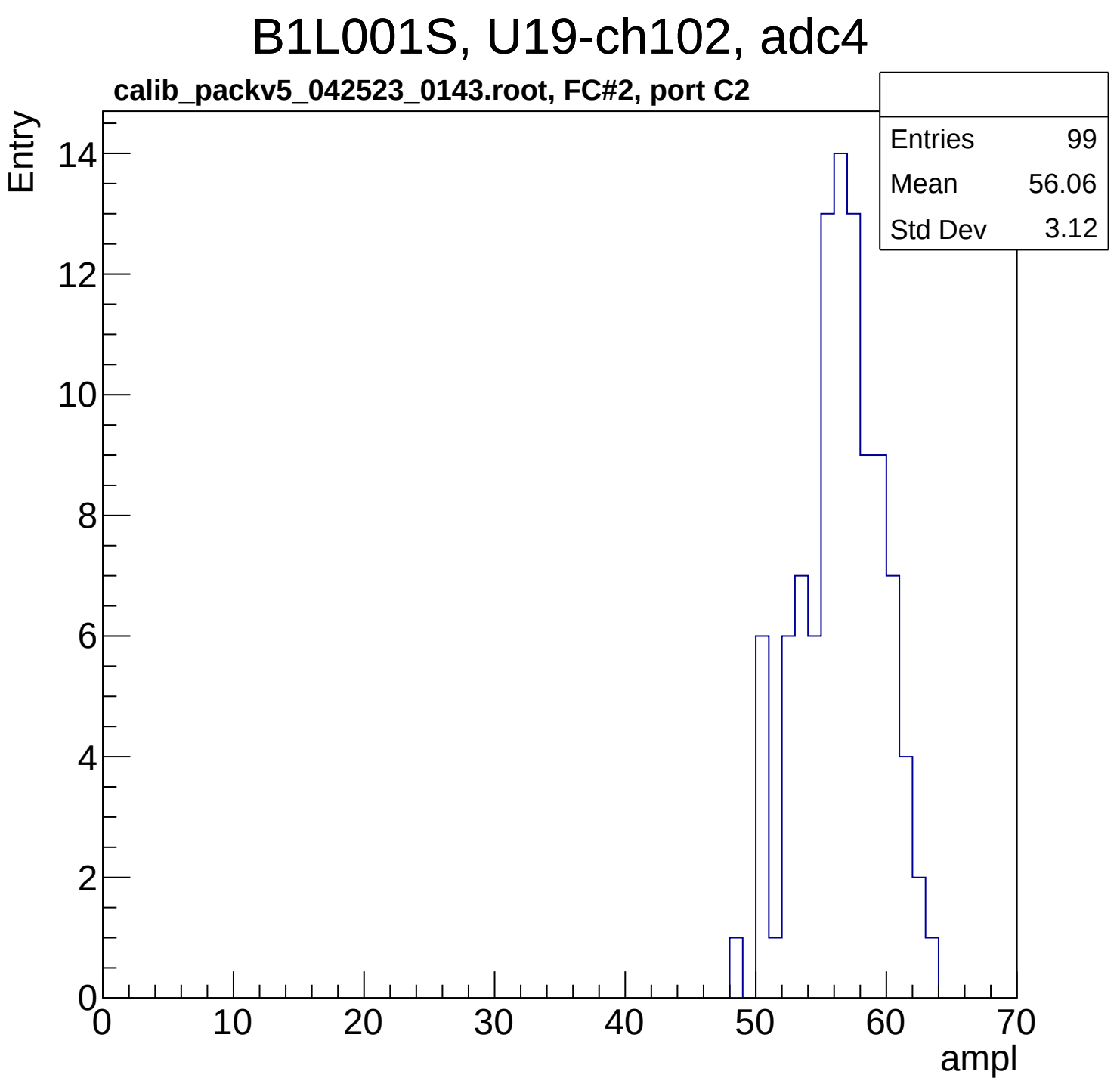

B1L001S, U19-ch101, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

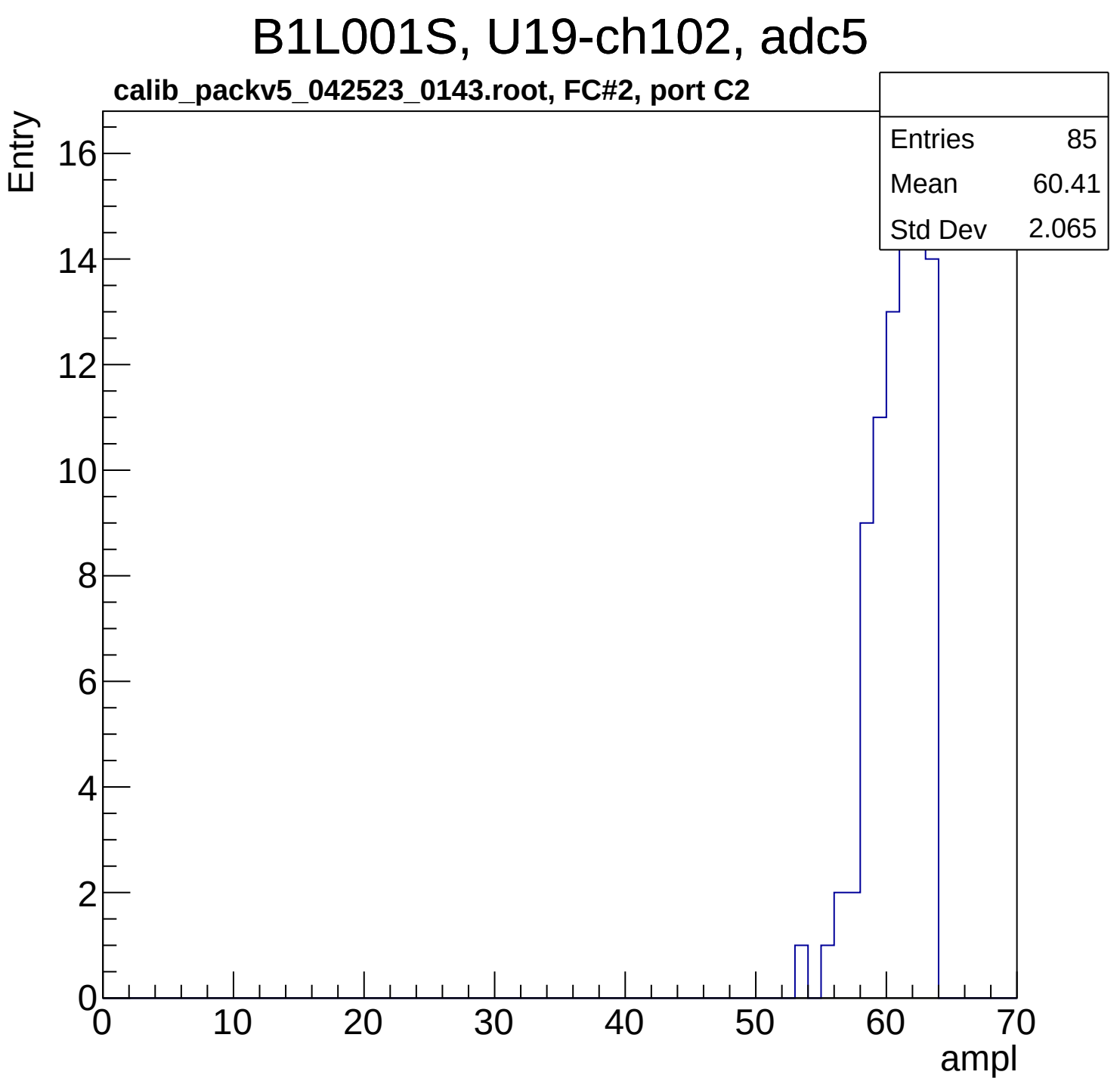

B1L001S, U19-ch102, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 120
Mean 30.89
Std Dev 3.217
Gaus mean : 31.2235
Gaus Width: 3.1860
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

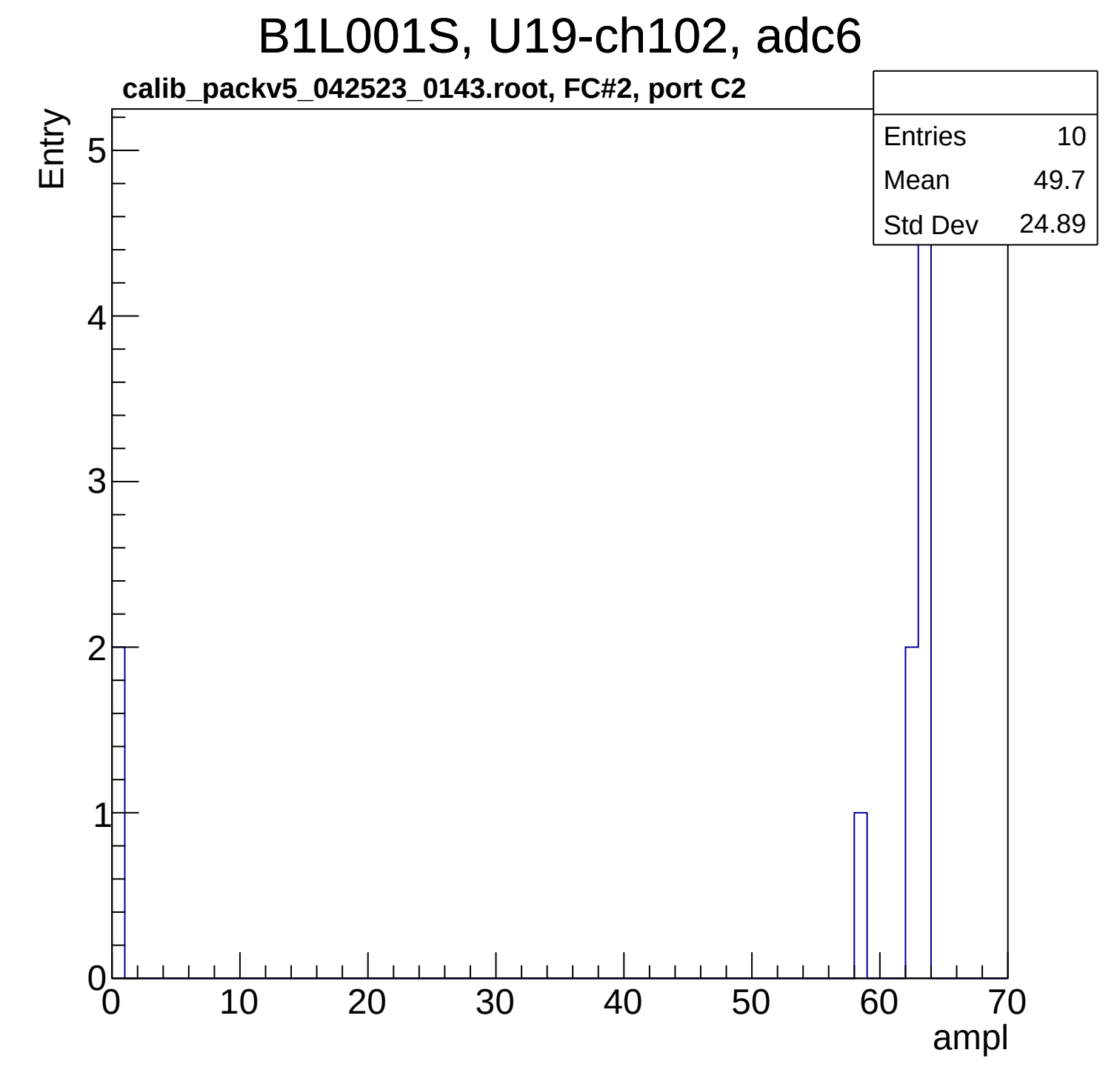

B1L001S, U19-ch102, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 134
Mean 36.83
Std Dev 3.418
Gaus mean : 37.2671
Gaus Width: 3.6512
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

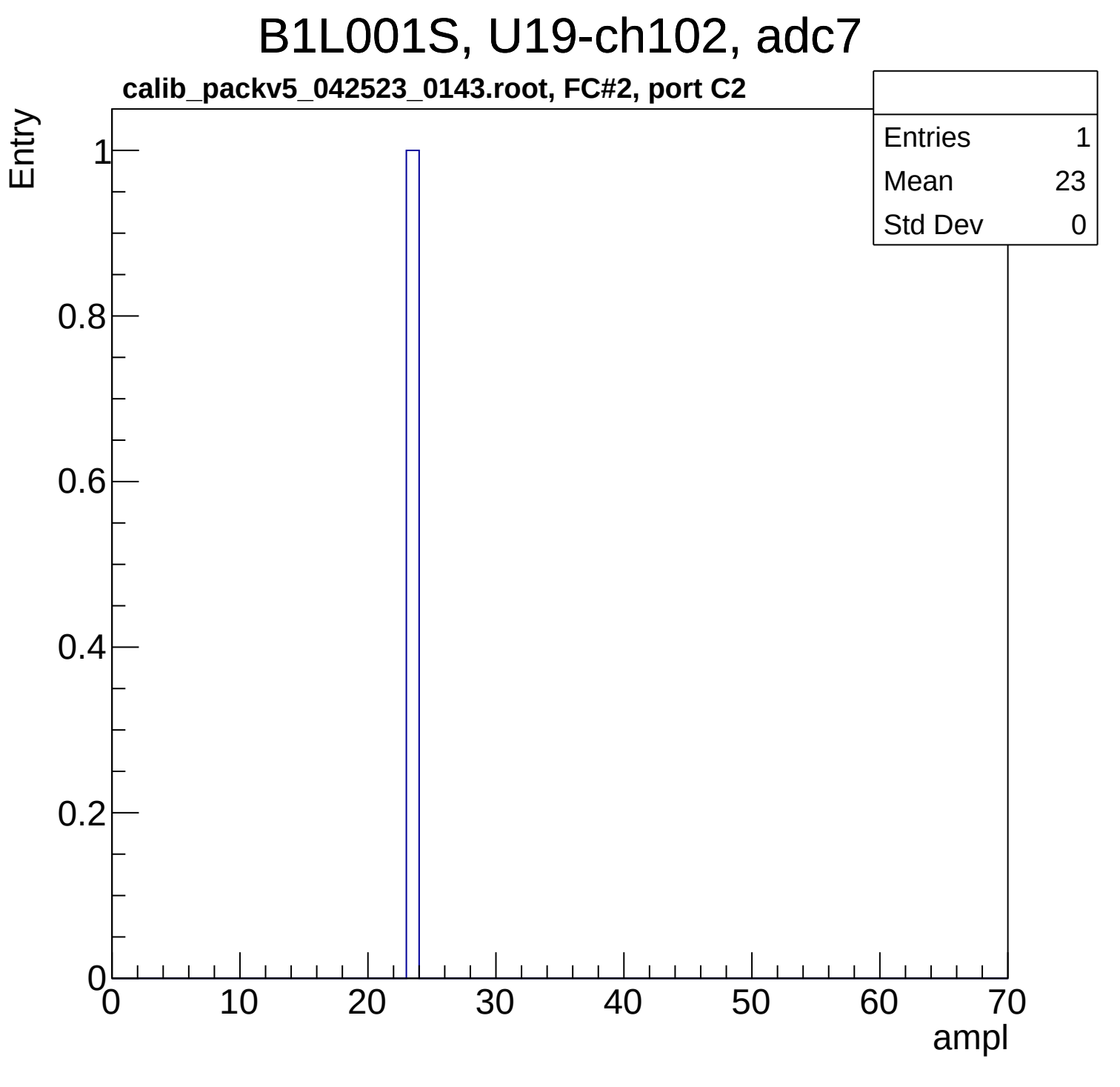

B1L001S, U19-ch102, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 116
Mean 43.38
Std Dev 3.287
Gaus mean : 44.1475
Gaus Width: 3.0954
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L001S, U19-ch102, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 156
Mean 49.96
Std Dev 3.753
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70


B1L001S, U19-ch102, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 99
Mean 56.06
Std Dev 3.12
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L001S, U19-ch102, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 85
Mean 60.41
Std Dev 2.065
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70


B1L001S, U19-ch102, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 10
Mean 49.7
Std Dev 24.89
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch102, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 23
Std Dev 0
Entry
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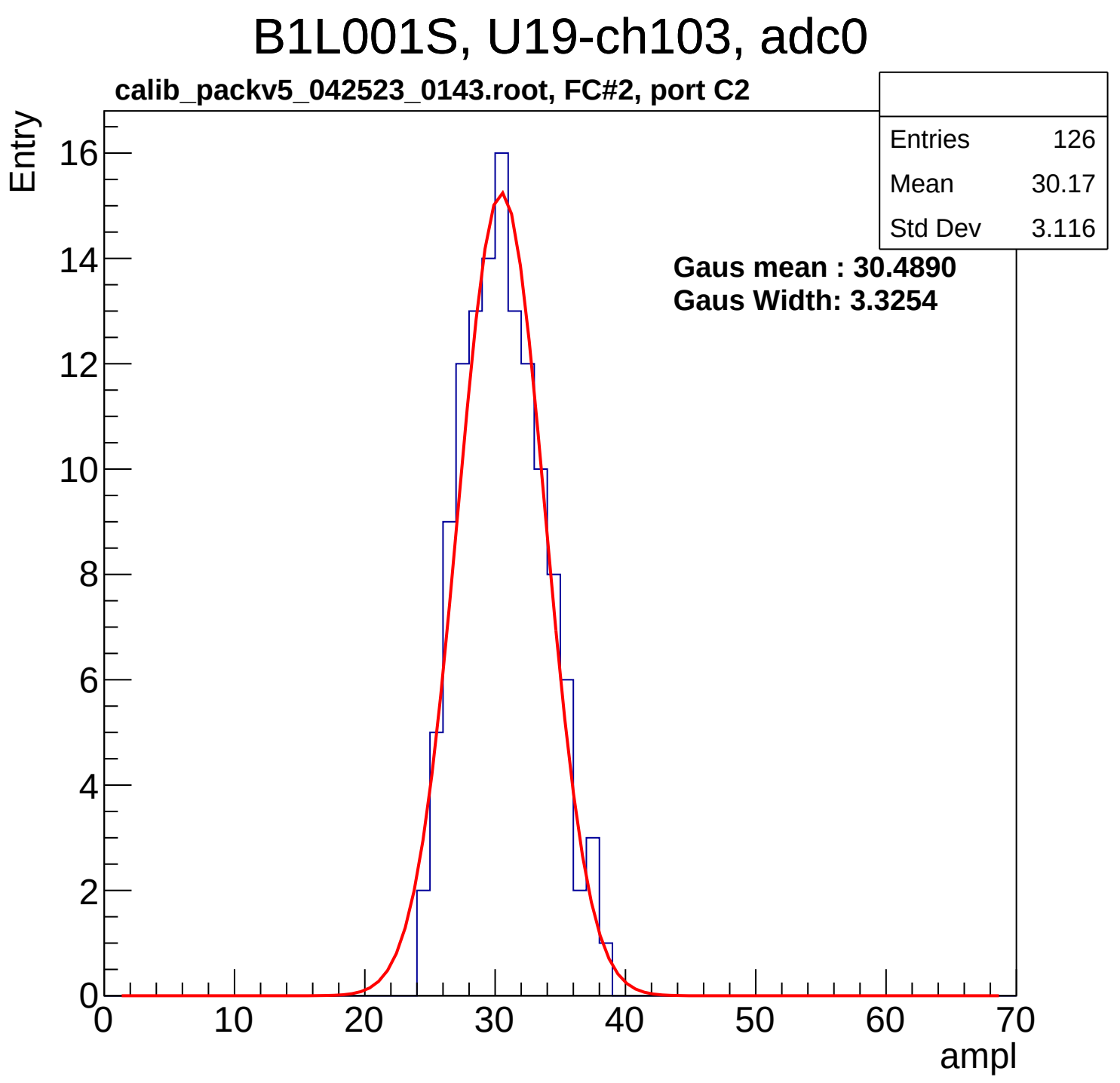
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch103, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 126
Mean 30.17
Std Dev 3.116
Gaus mean : 30.4890
Gaus Width: 3.3254
Entry
ampl
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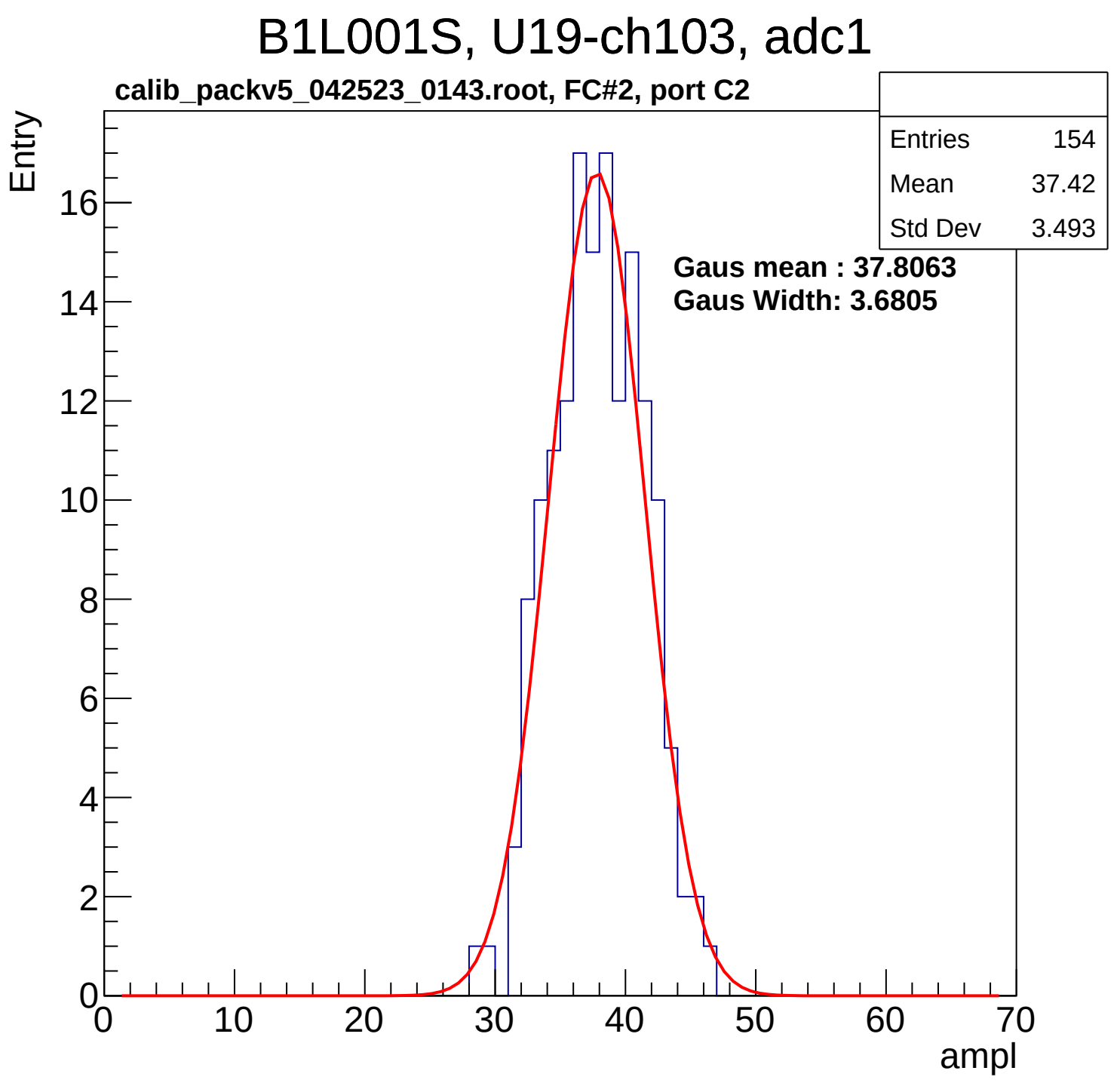
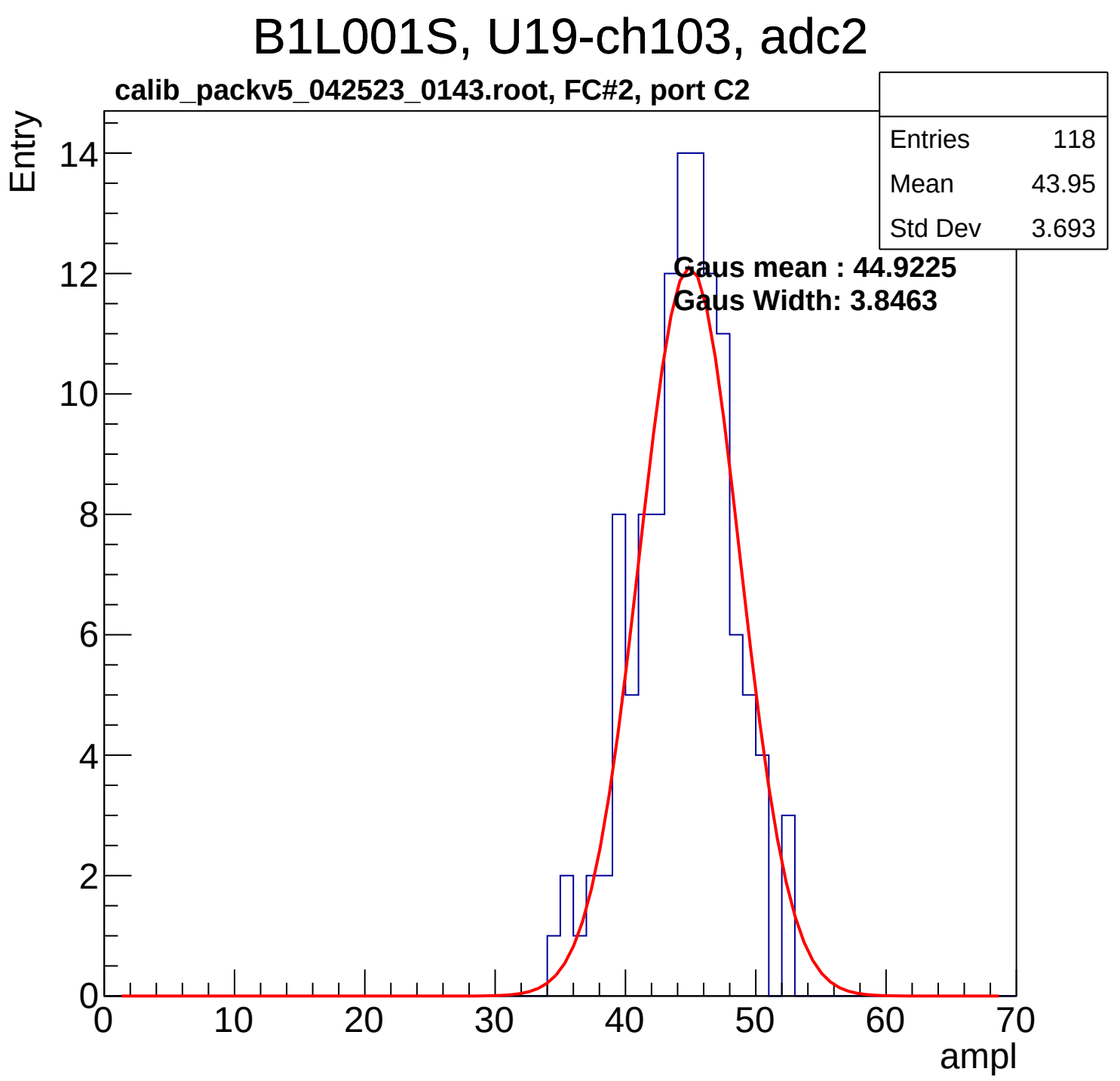
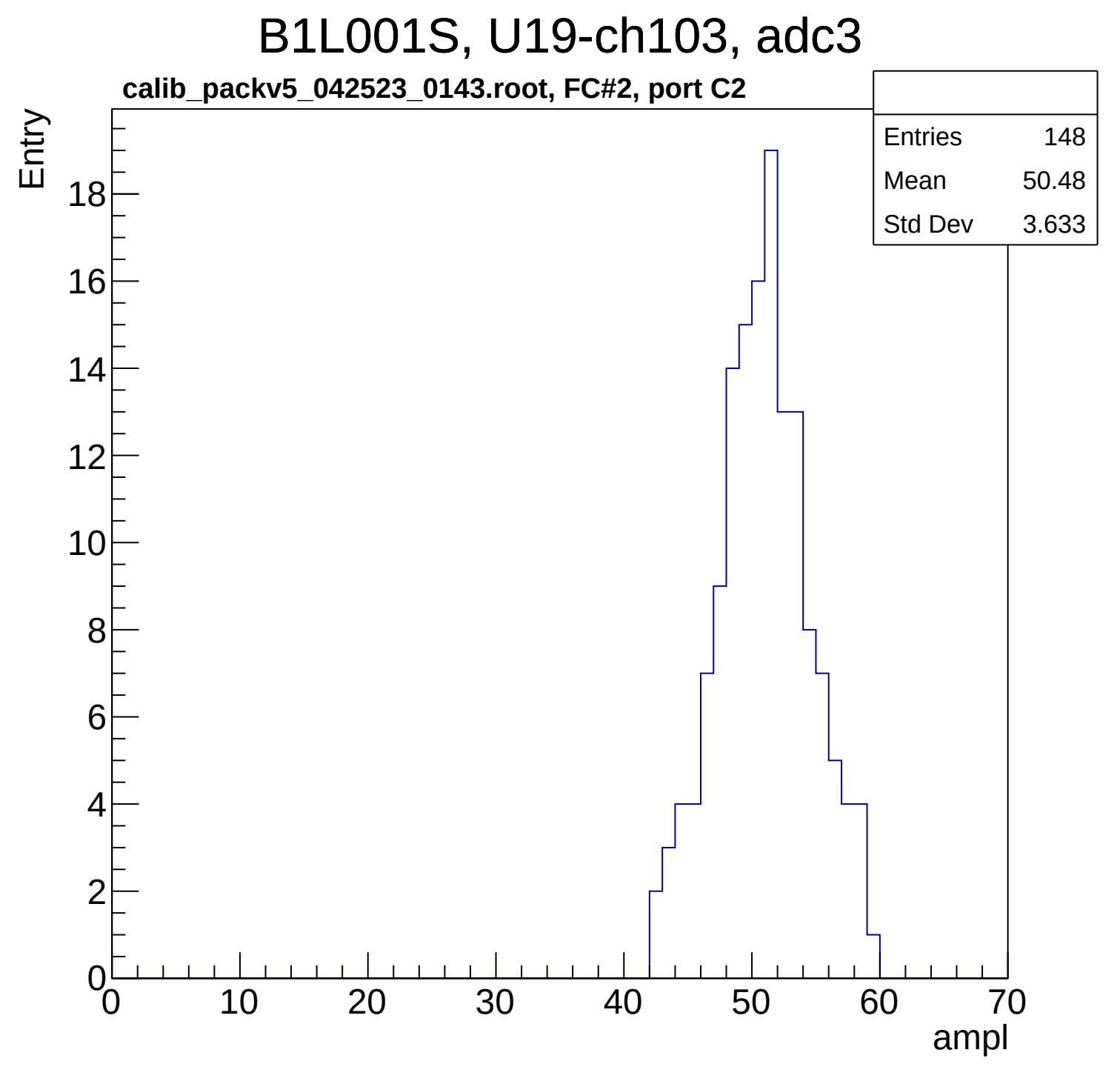
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70


B1L001S, U19-ch103, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 154
Mean 37.42
Std Dev 3.493
Gaus mean : 37.8063
Gaus Width: 3.6805
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70


B1L001S, U19-ch103, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 118
Mean 43.95
Std Dev 3.693
Gaus mean : 44.9225
Gaus Width: 3.8463
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L001S, U19-ch103, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 148
Mean 50.48
Std Dev 3.633
Entry
0
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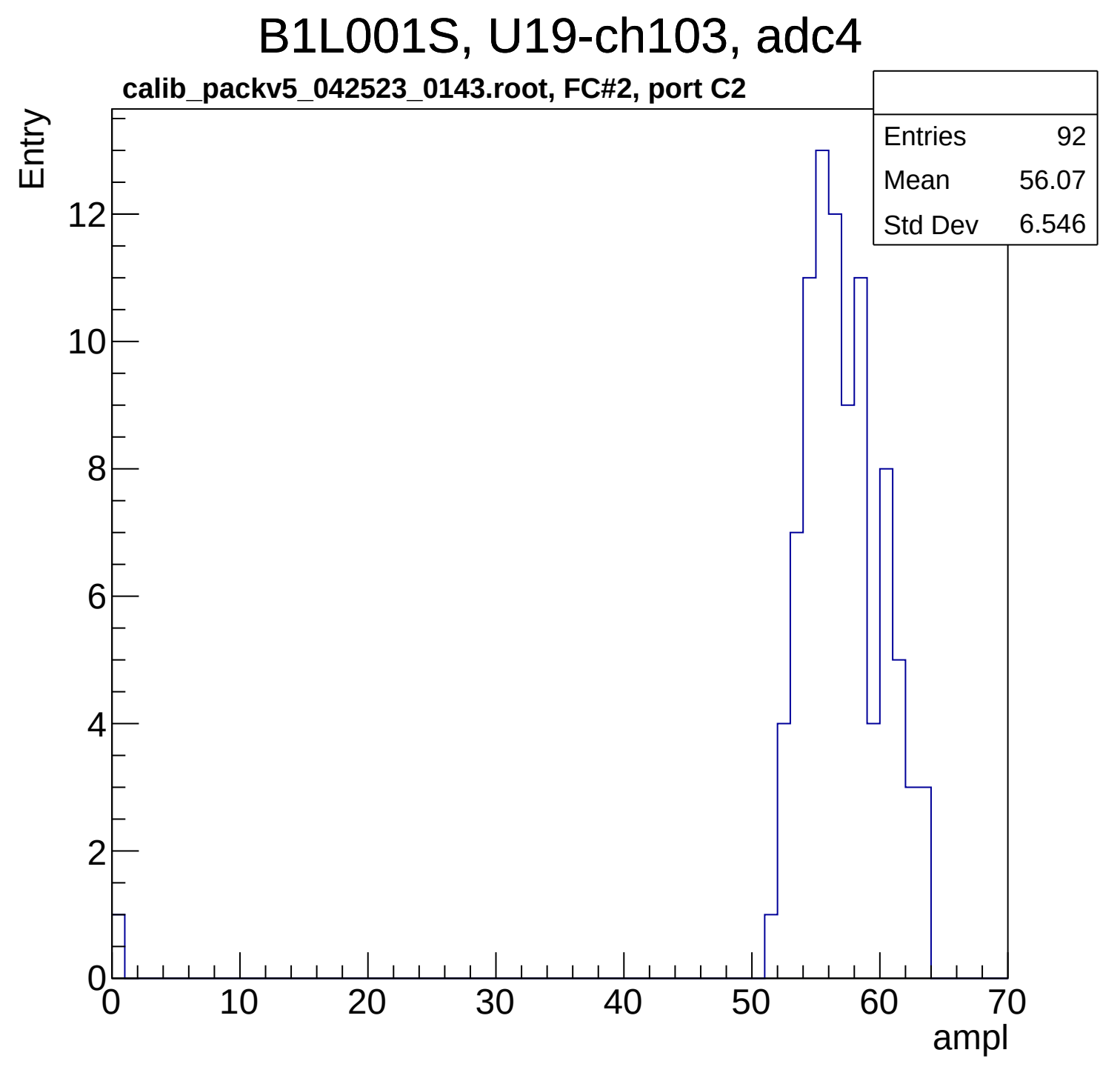
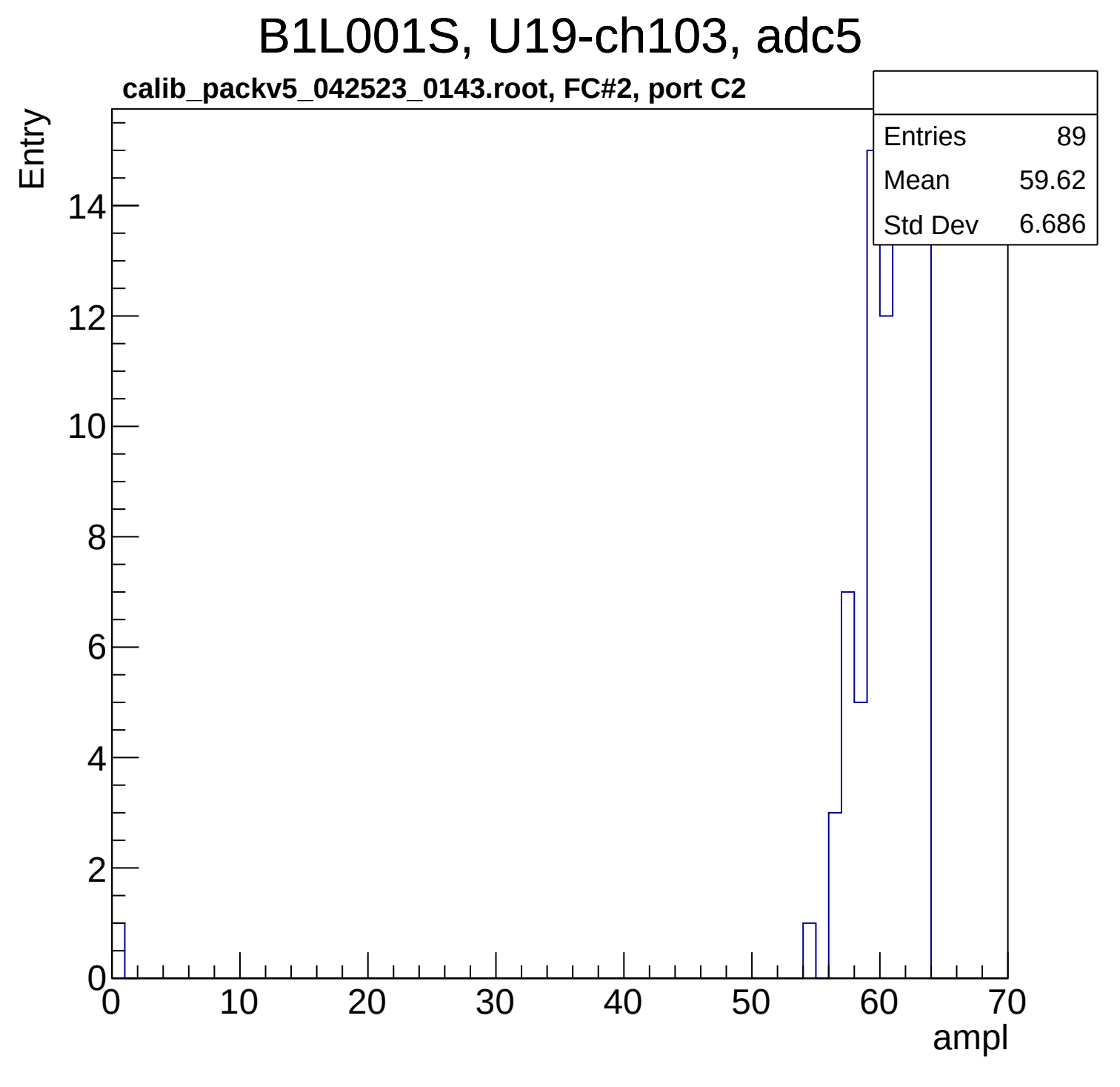
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch103, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 92
Mean 56.07
Std Dev 6.546
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch103, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 89
Mean 59.62
Std Dev 6.686
Entry
ampl
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8
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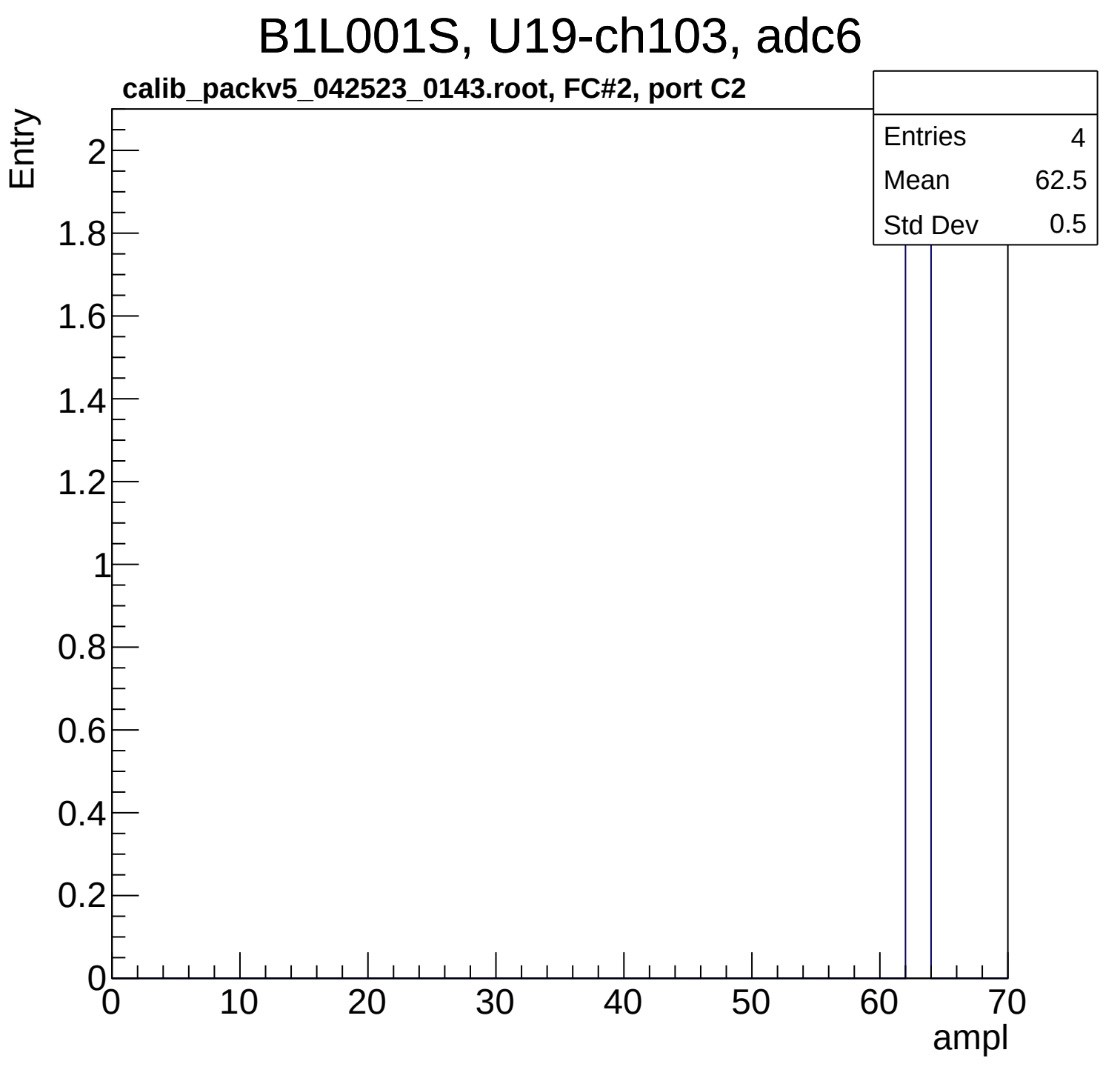
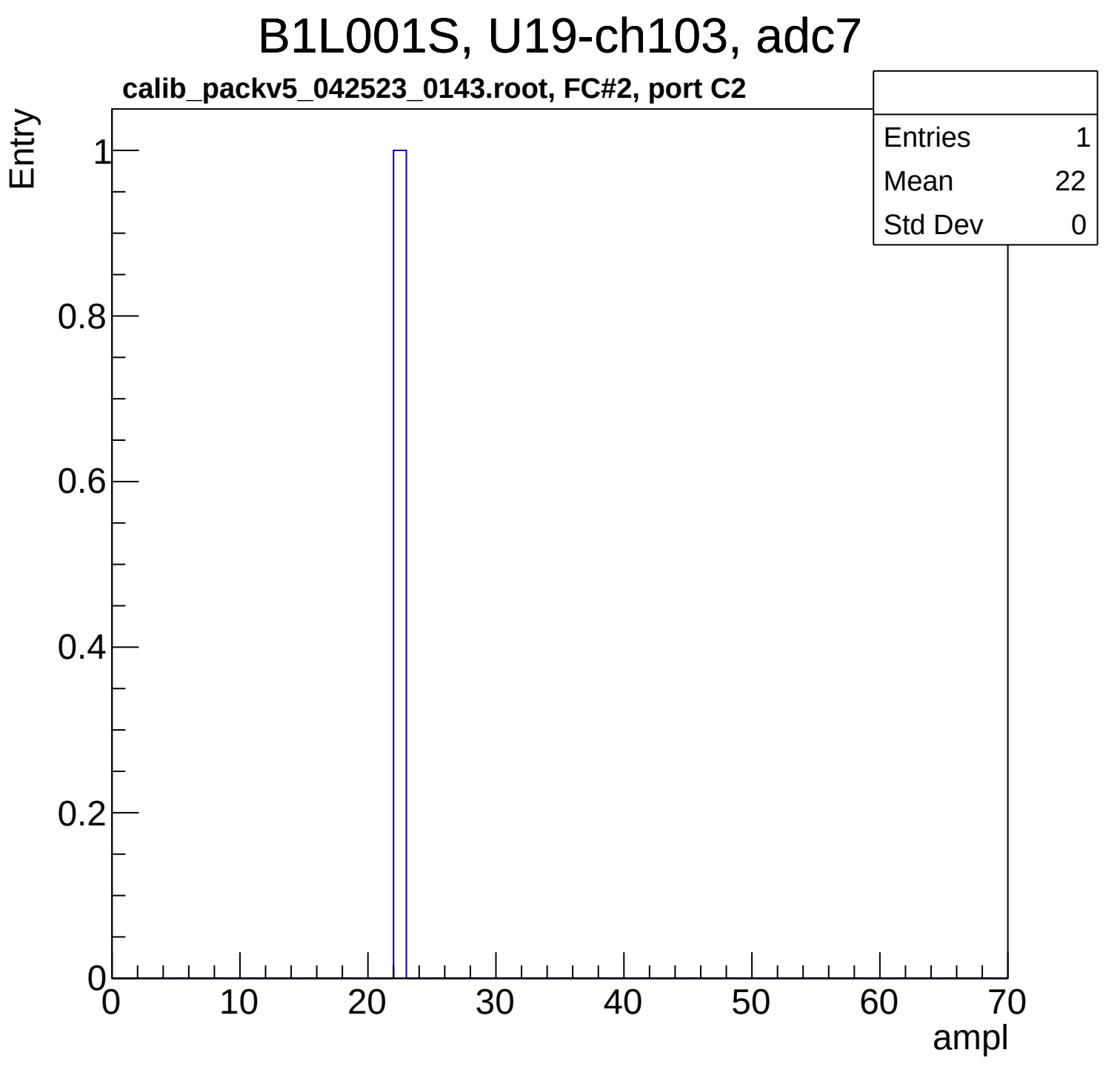

B1L001S, U19-ch103, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 4
Mean 62.5
Std Dev 0.5
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L001S, U19-ch103, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 22
Std Dev 0
Entry
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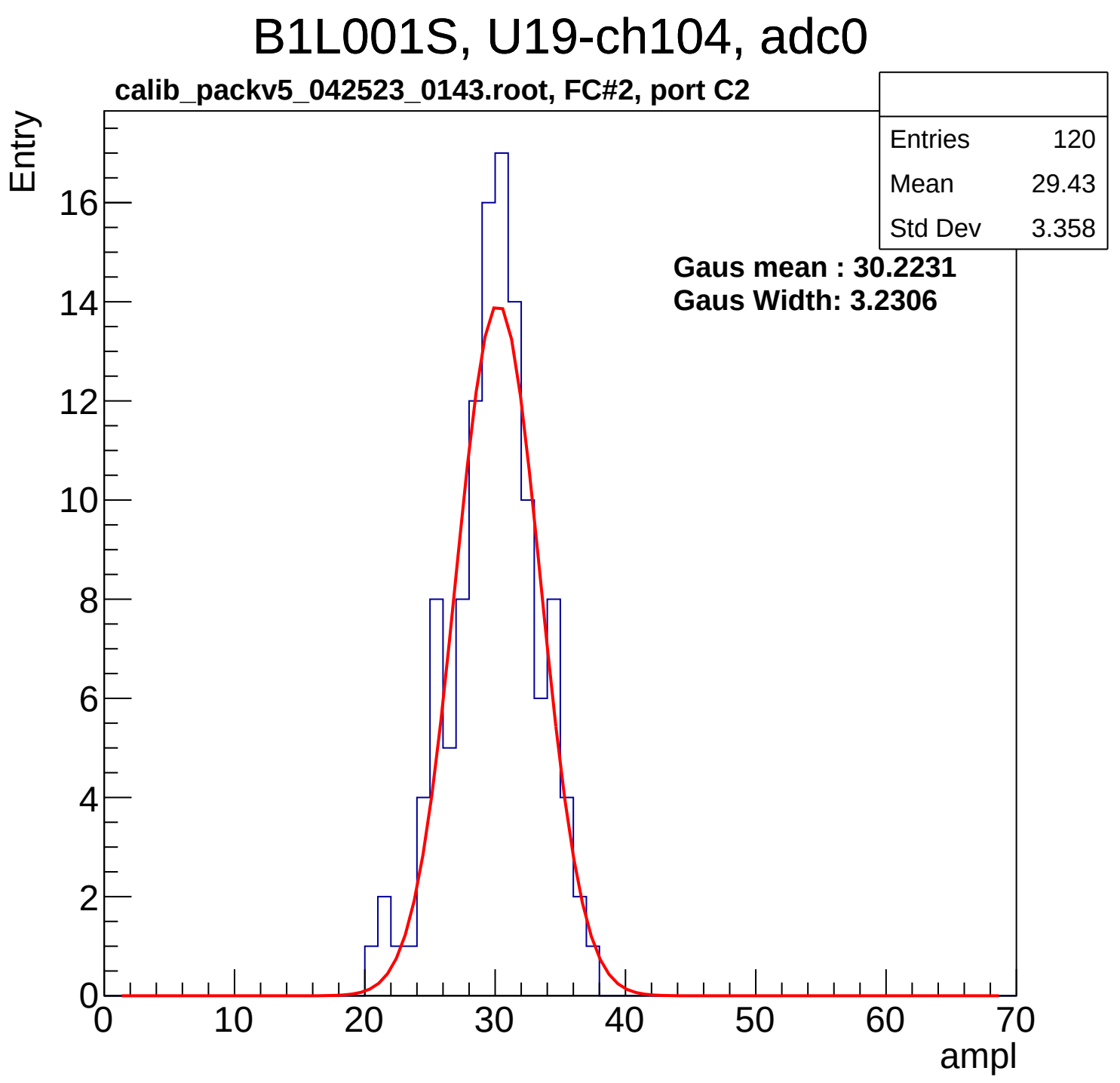
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch104, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 120
Mean 29.43
Std Dev 3.358
Gaus mean : 30.2231
Gaus Width: 3.2306
Entry
ampl
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2
4
6
8
10
12
14
16
0
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20
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40
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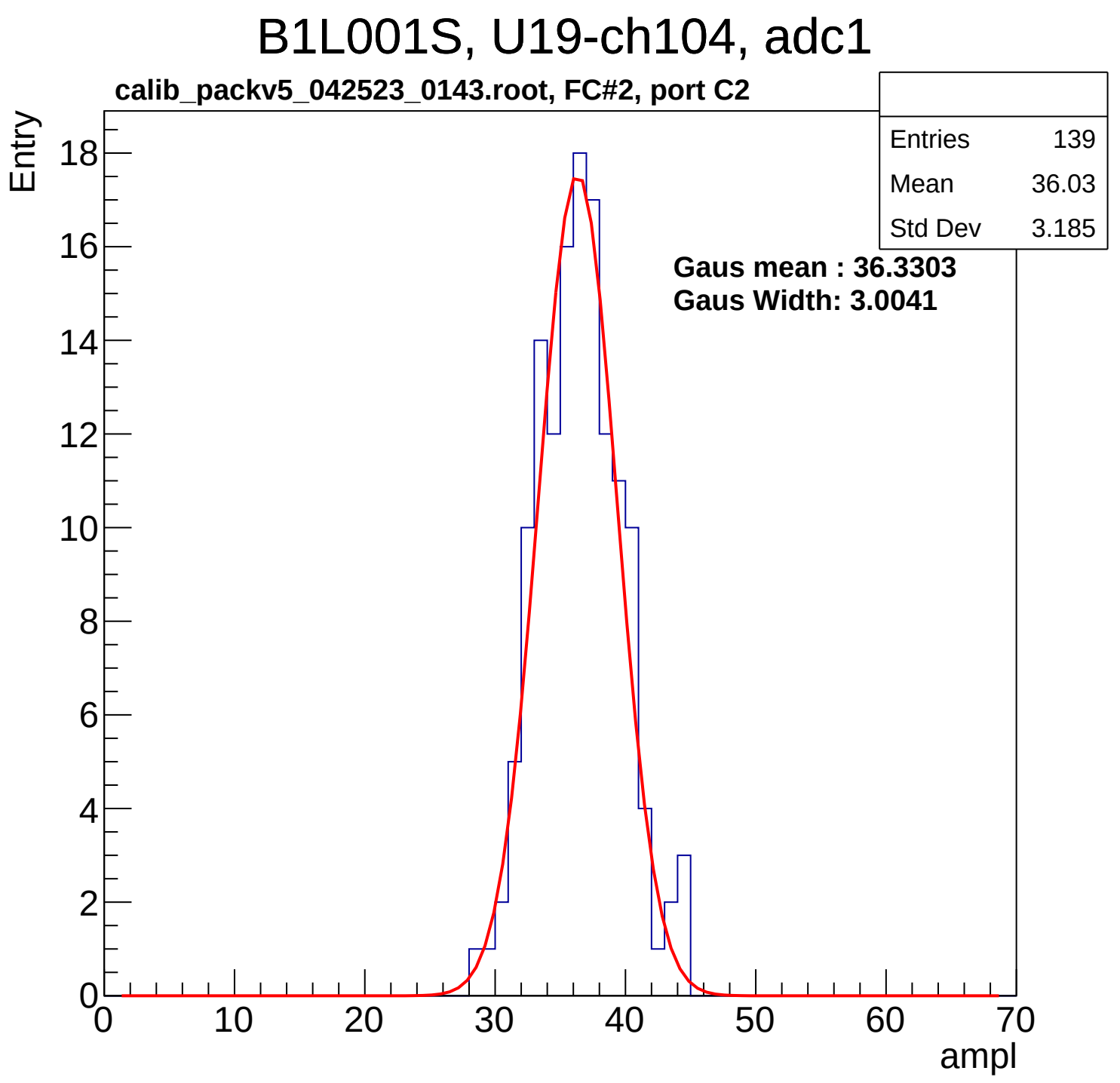
60
70


B1L001S, U19-ch104, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 139
Mean 36.03
Std Dev 3.185
Gaus mean : 36.3303
Gaus Width: 3.0041
Entry
ampl
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2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
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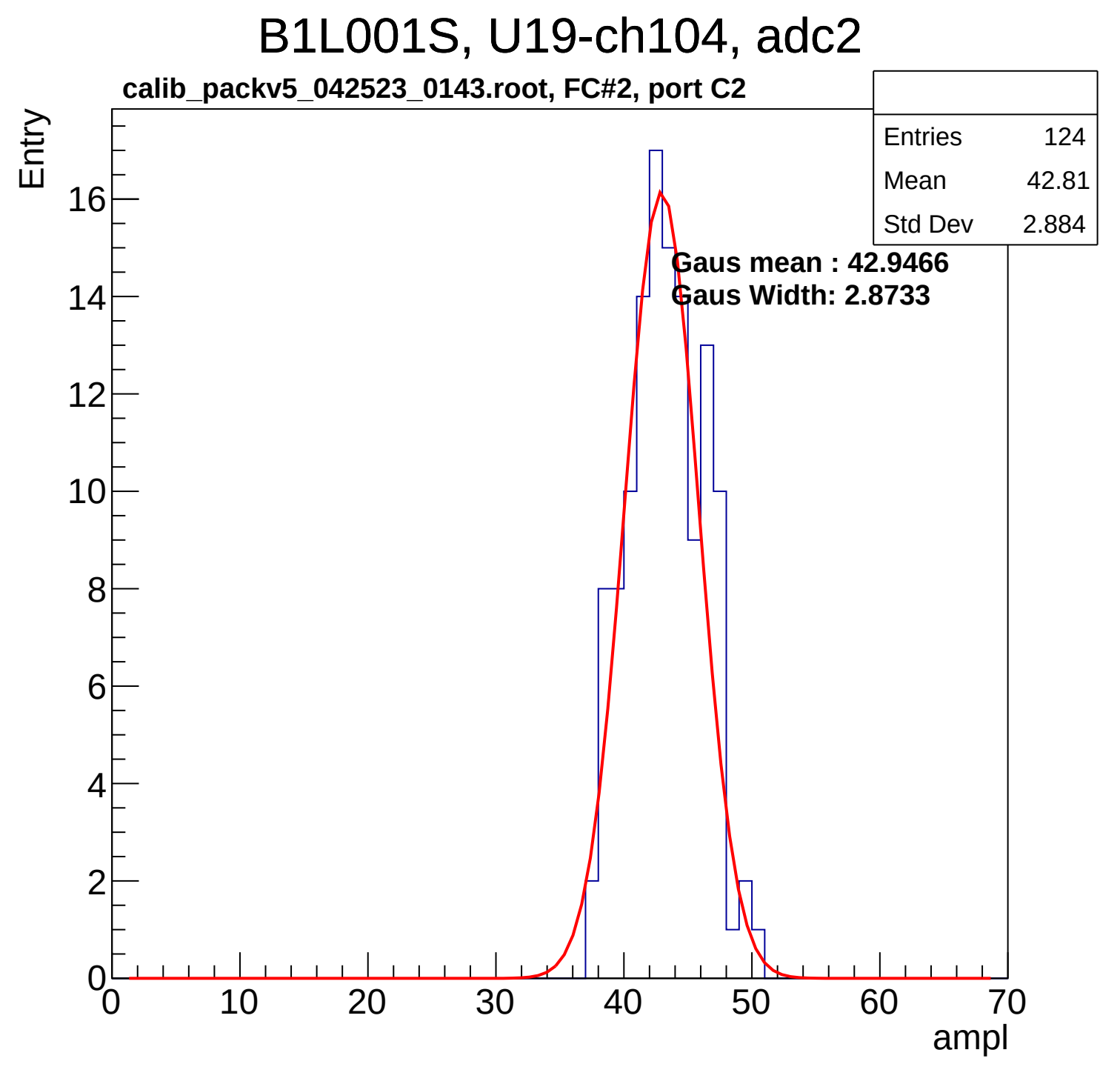
B1L001S, U19-ch104, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 124
Mean 42.81
Std Dev 2.884
Gaus mean : 42.9466
Gaus Width: 2.8733
Entry
ampl
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2
4
6
8
10
12
14
16
0
10
20
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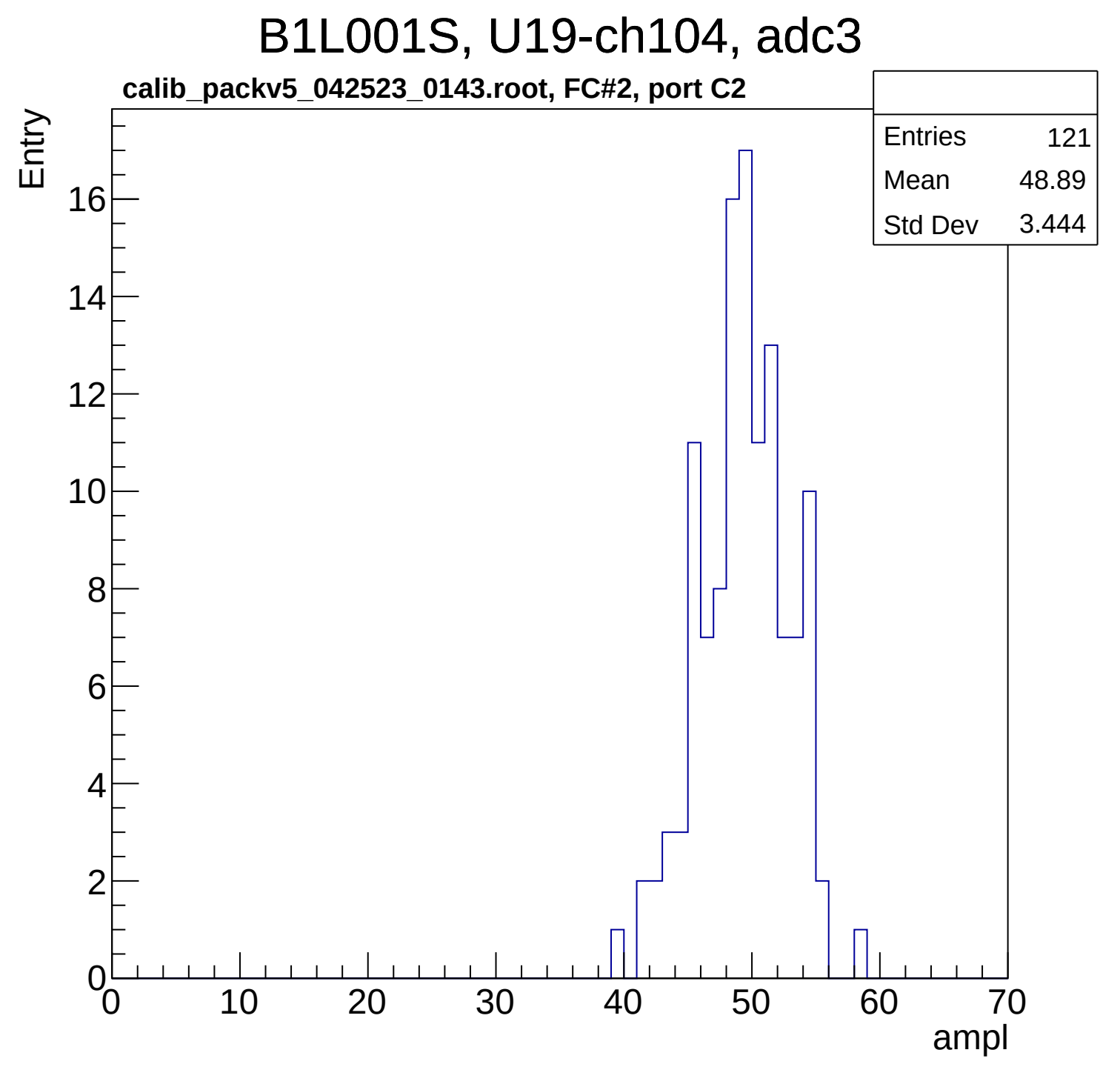
40
50
60
70


B1L001S, U19-ch104, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 121
Mean 48.89
Std Dev 3.444
Entry
ampl
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2
4
6
8
10
12
14
16
0
10
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40
50
60
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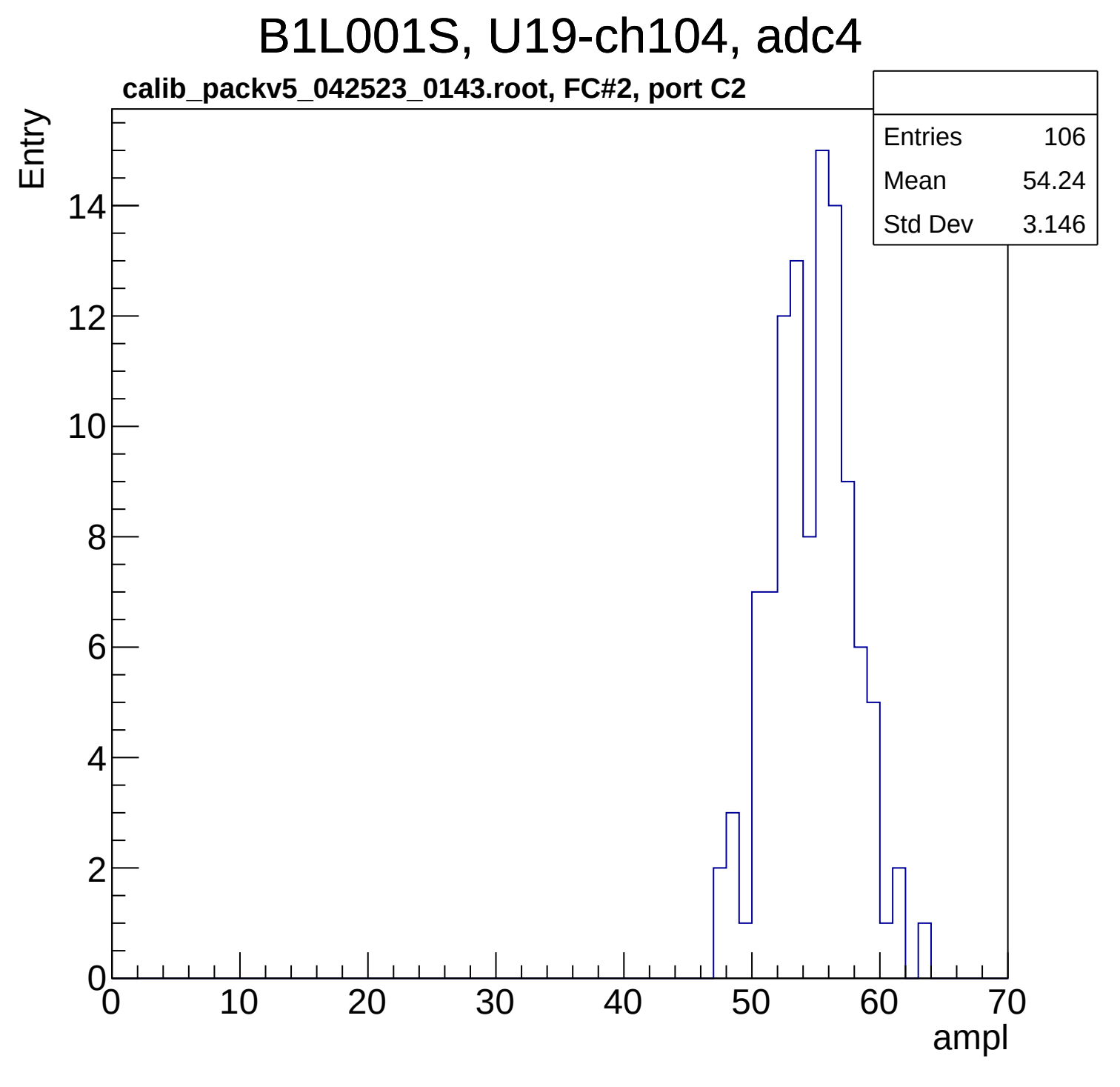
B1L001S, U19-ch104, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 106
Mean 54.24
Std Dev 3.146
Entry
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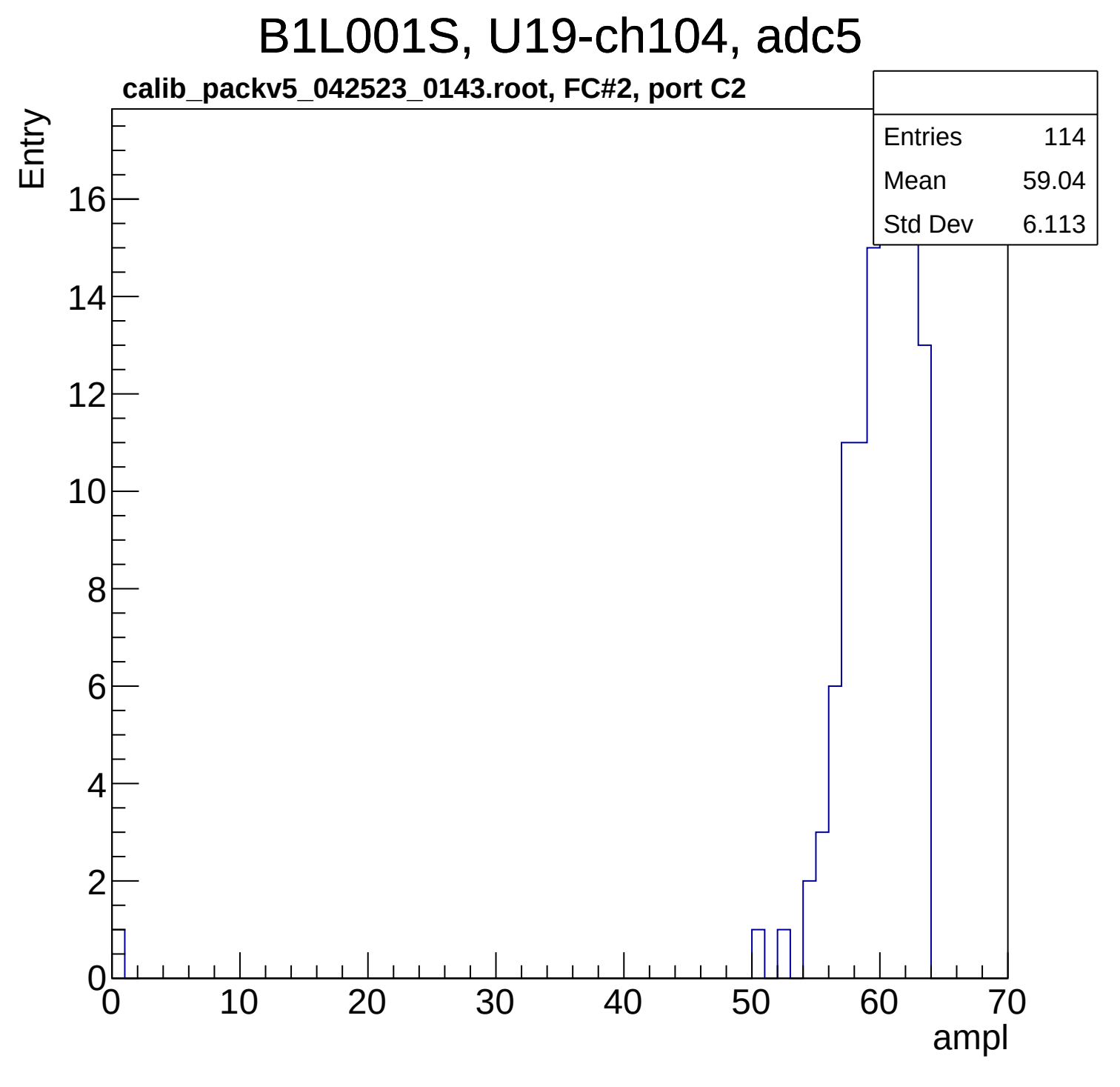
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch104, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 114
Mean 59.04
Std Dev 6.113
Entry
ampl
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2
4
6
8
10
12
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16
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10
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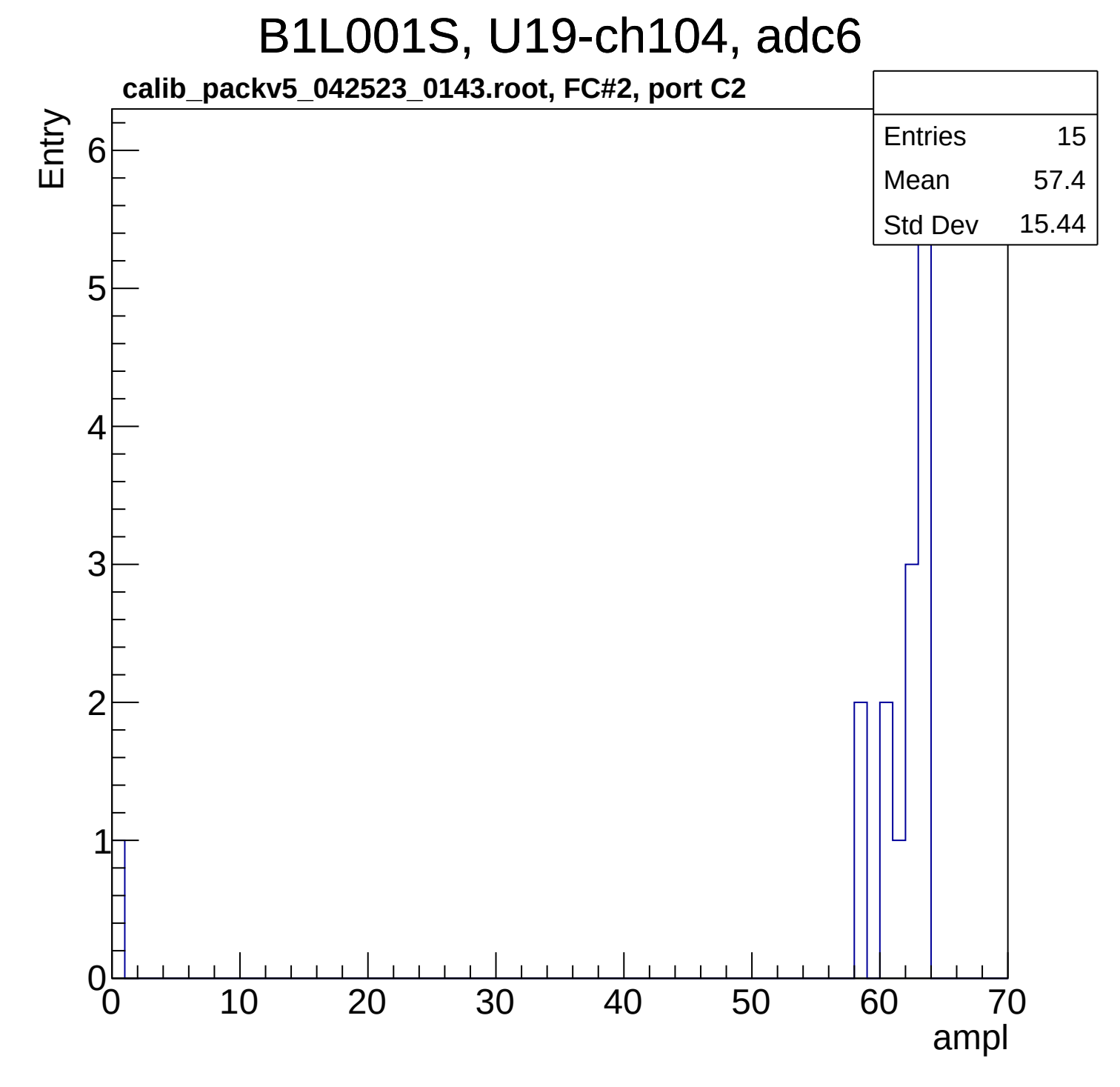
B1L001S, U19-ch104, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 15
Mean 57.4
Std Dev 15.44
Entry
ampl
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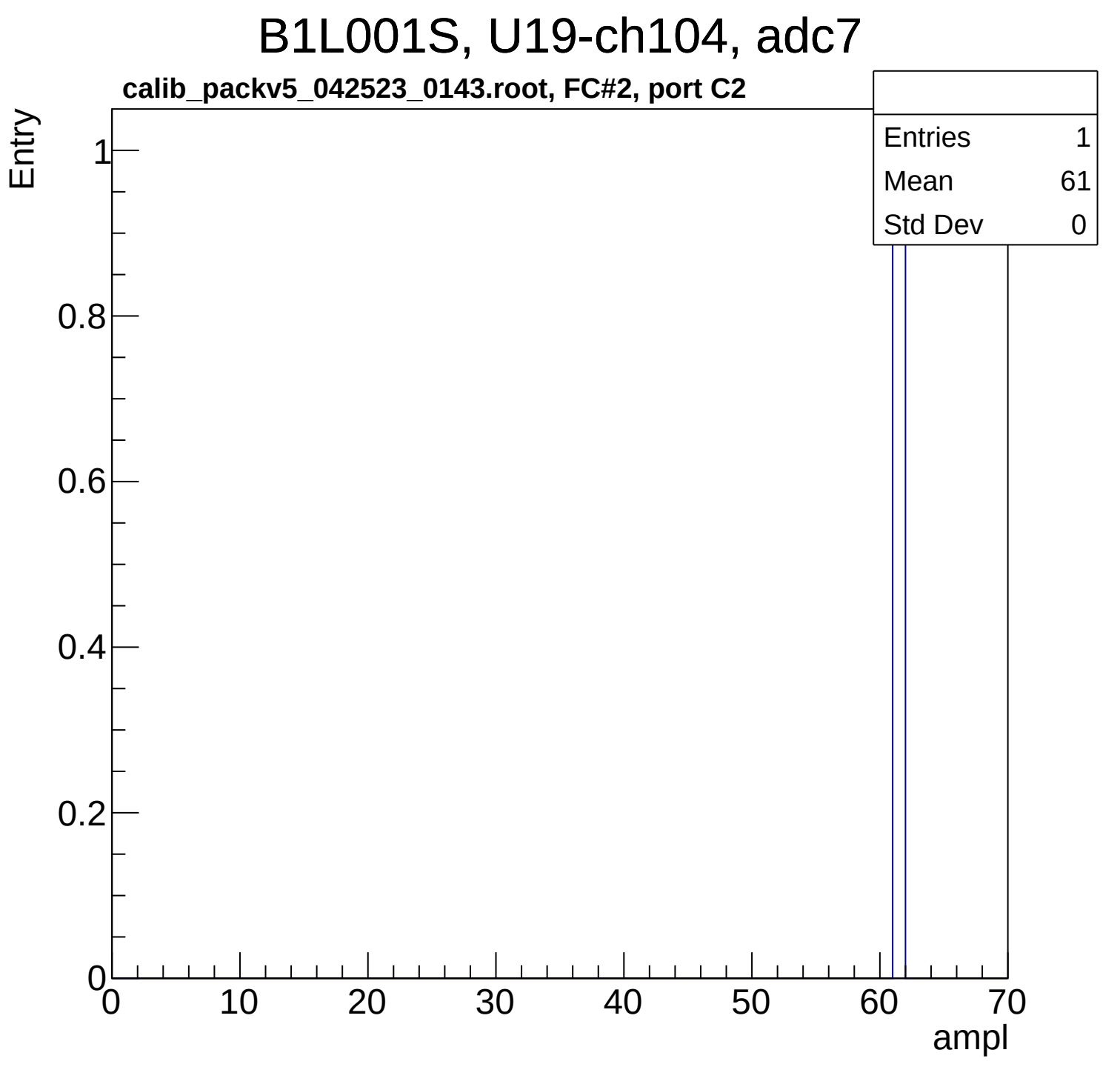
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L001S, U19-ch104, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 61
Std Dev 0
Entry
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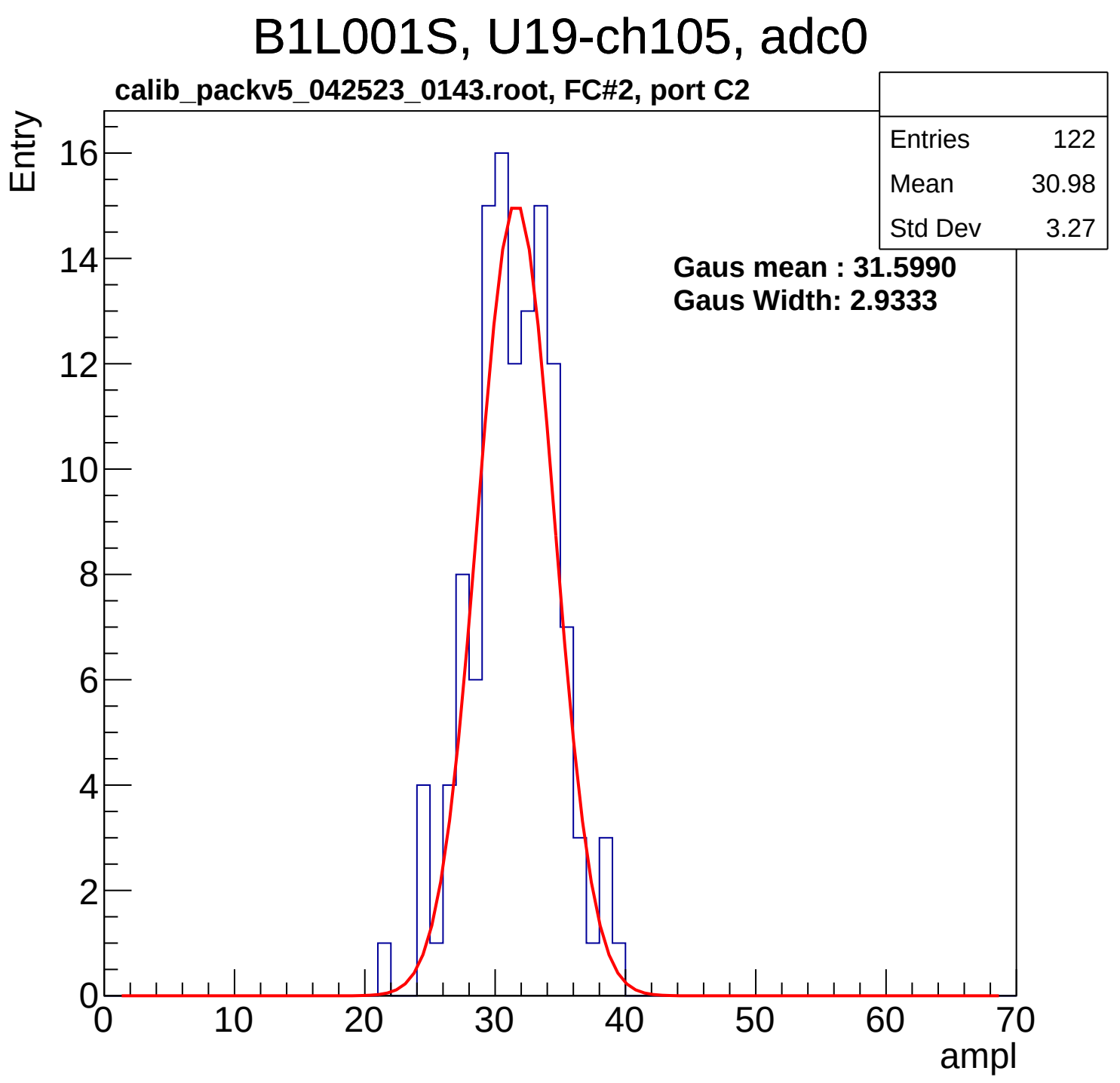
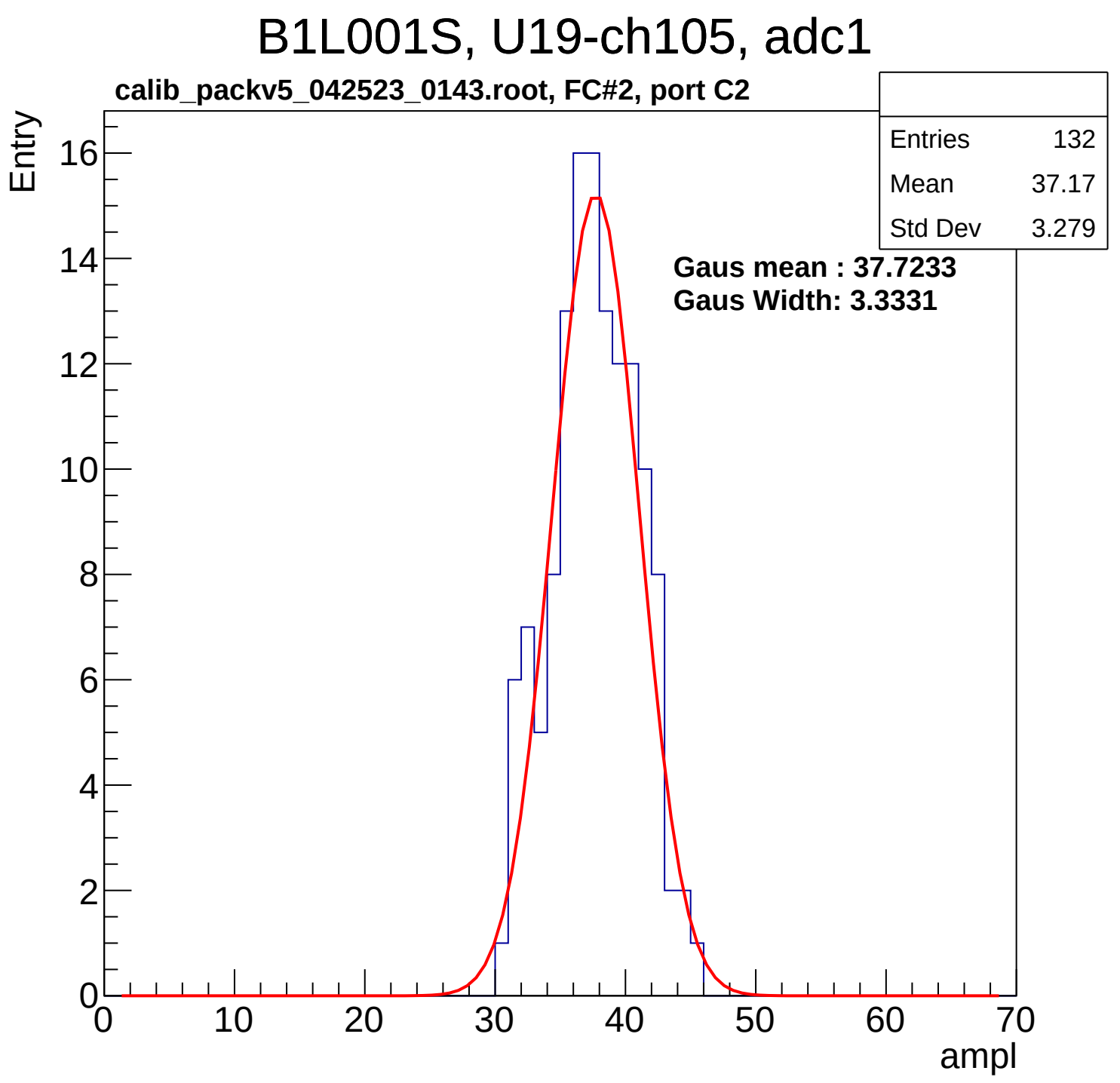
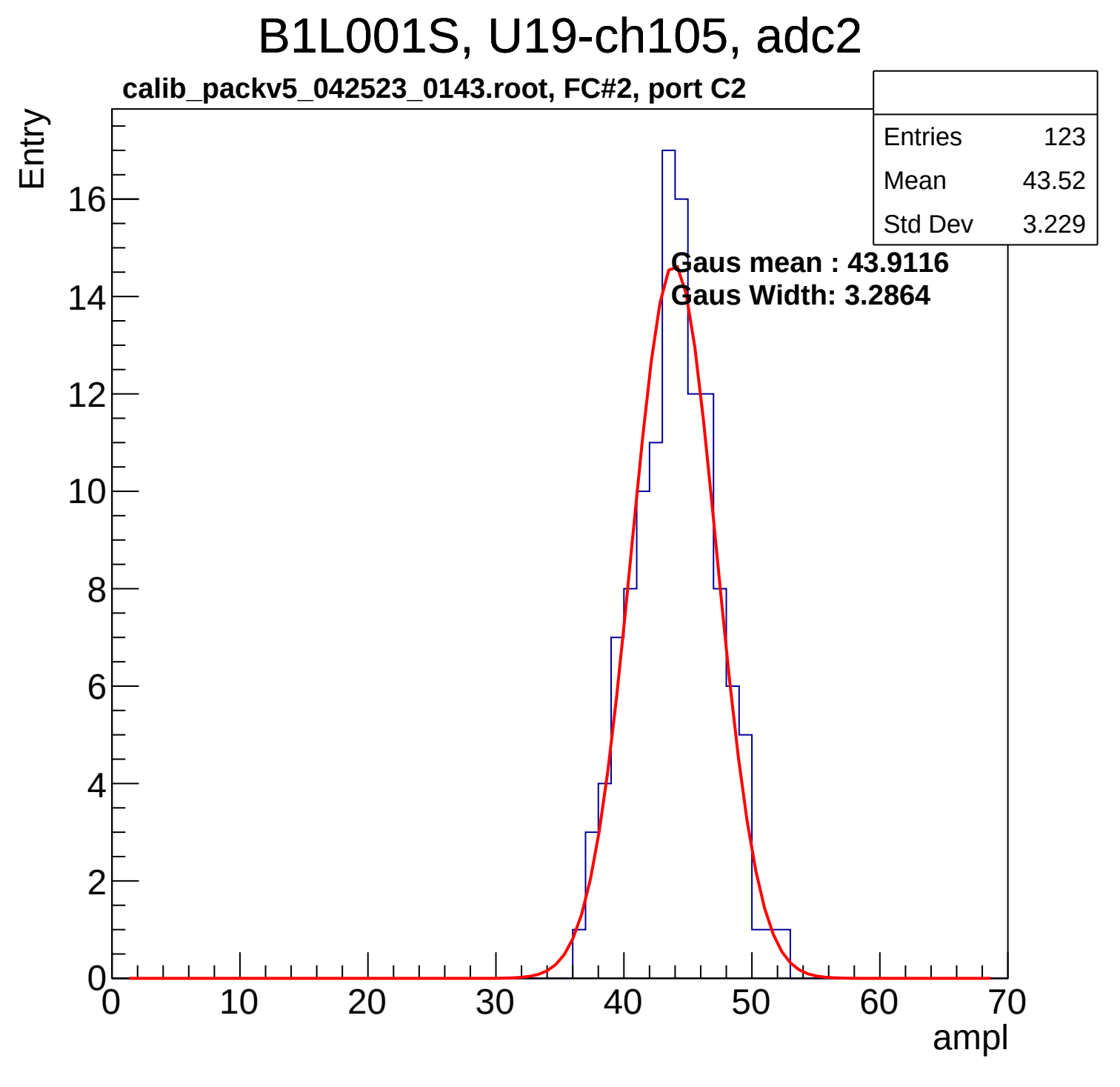
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch105, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 122
Mean 30.98
Std Dev 3.27
Gaus mean : 31.5990
Gaus Width: 2.9333
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70


B1L001S, U19-ch105, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 132
Mean 37.17
Std Dev 3.279
Gaus mean : 37.7233
Gaus Width: 3.3331
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70


B1L001S, U19-ch105, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 123
Mean 43.52
Std Dev 3.229
Gaus mean : 43.9116
Gaus Width: 3.2864
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
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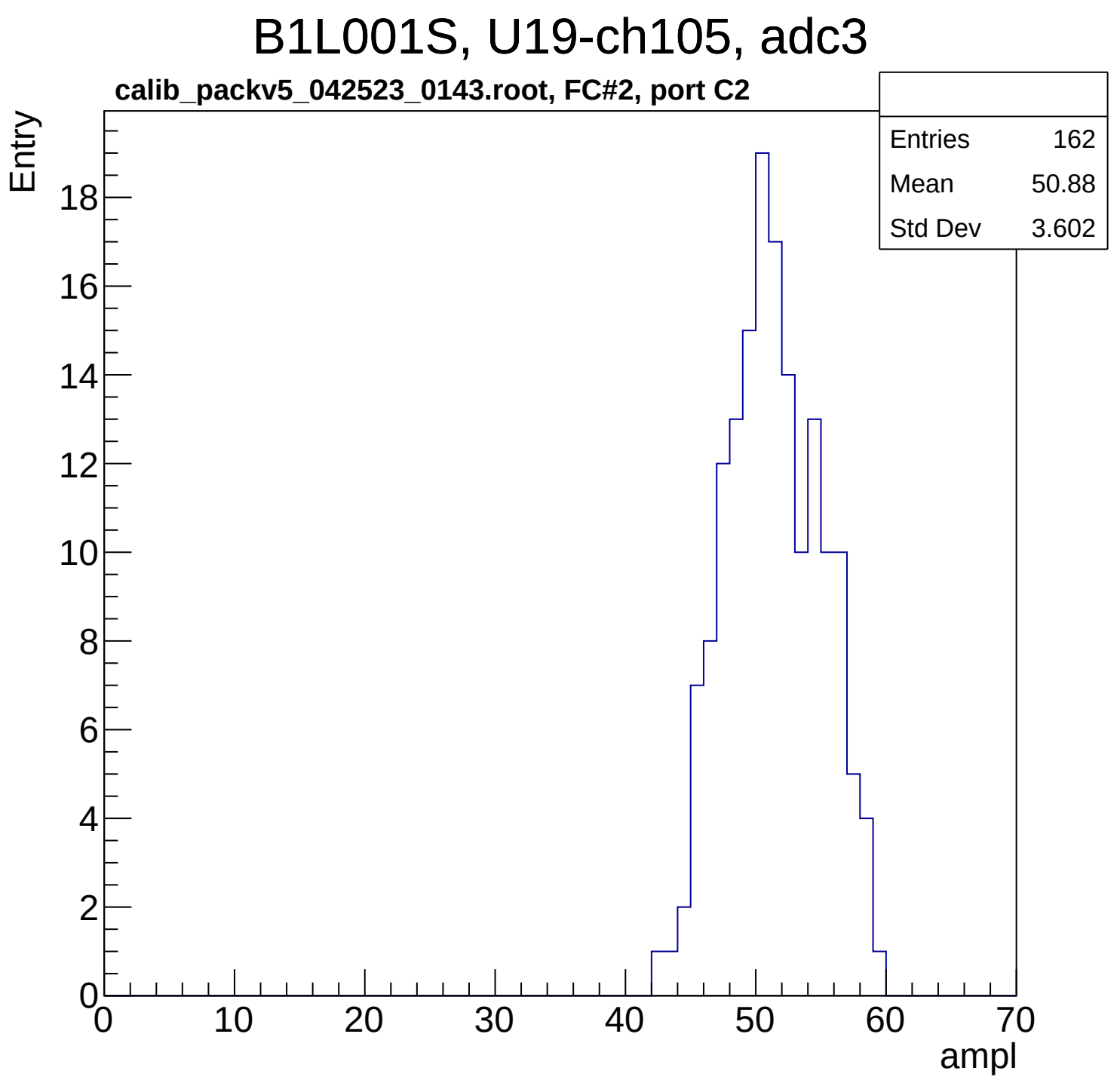
B1L001S, U19-ch105, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 162
Mean 50.88
Std Dev 3.602
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
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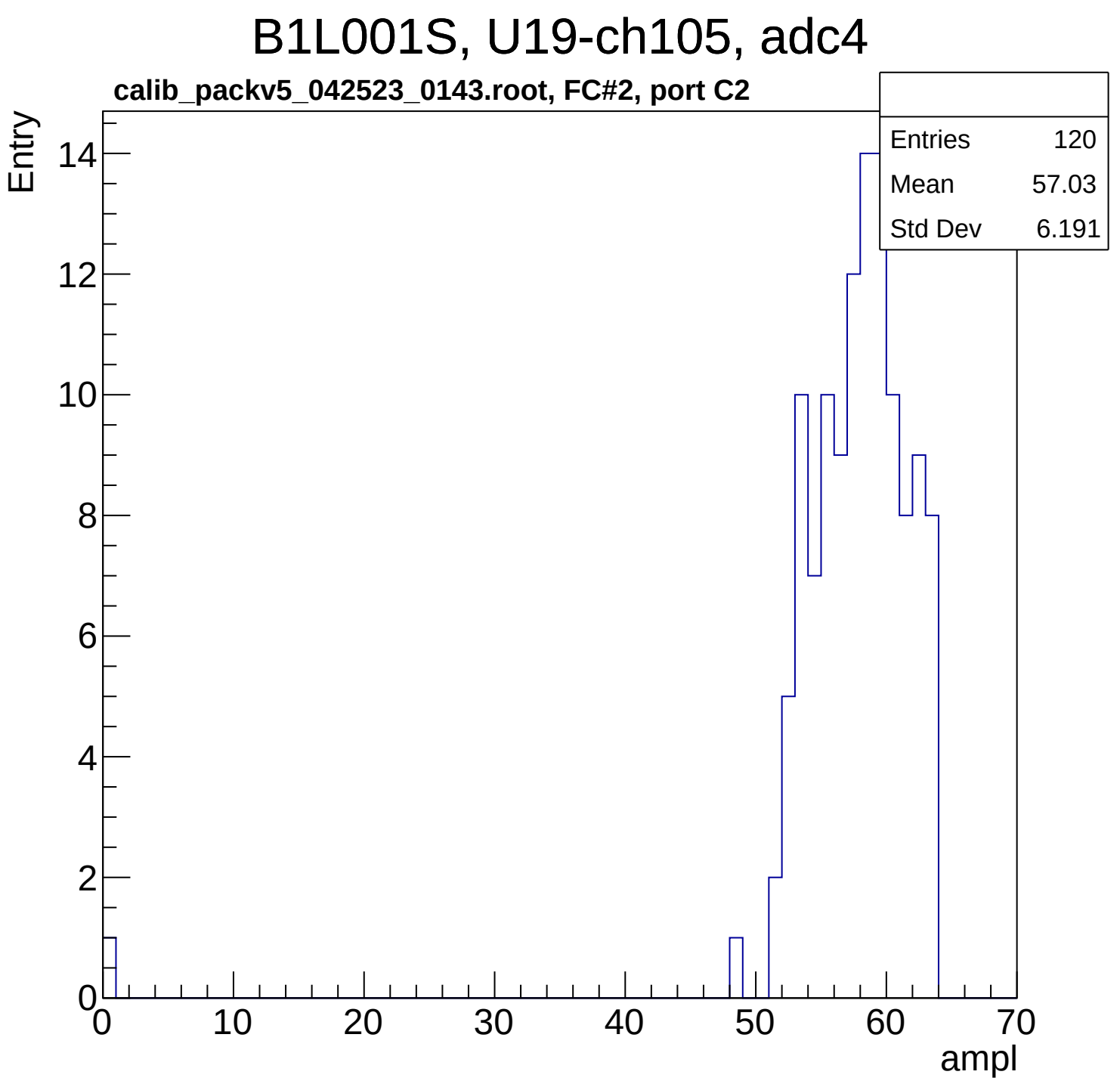
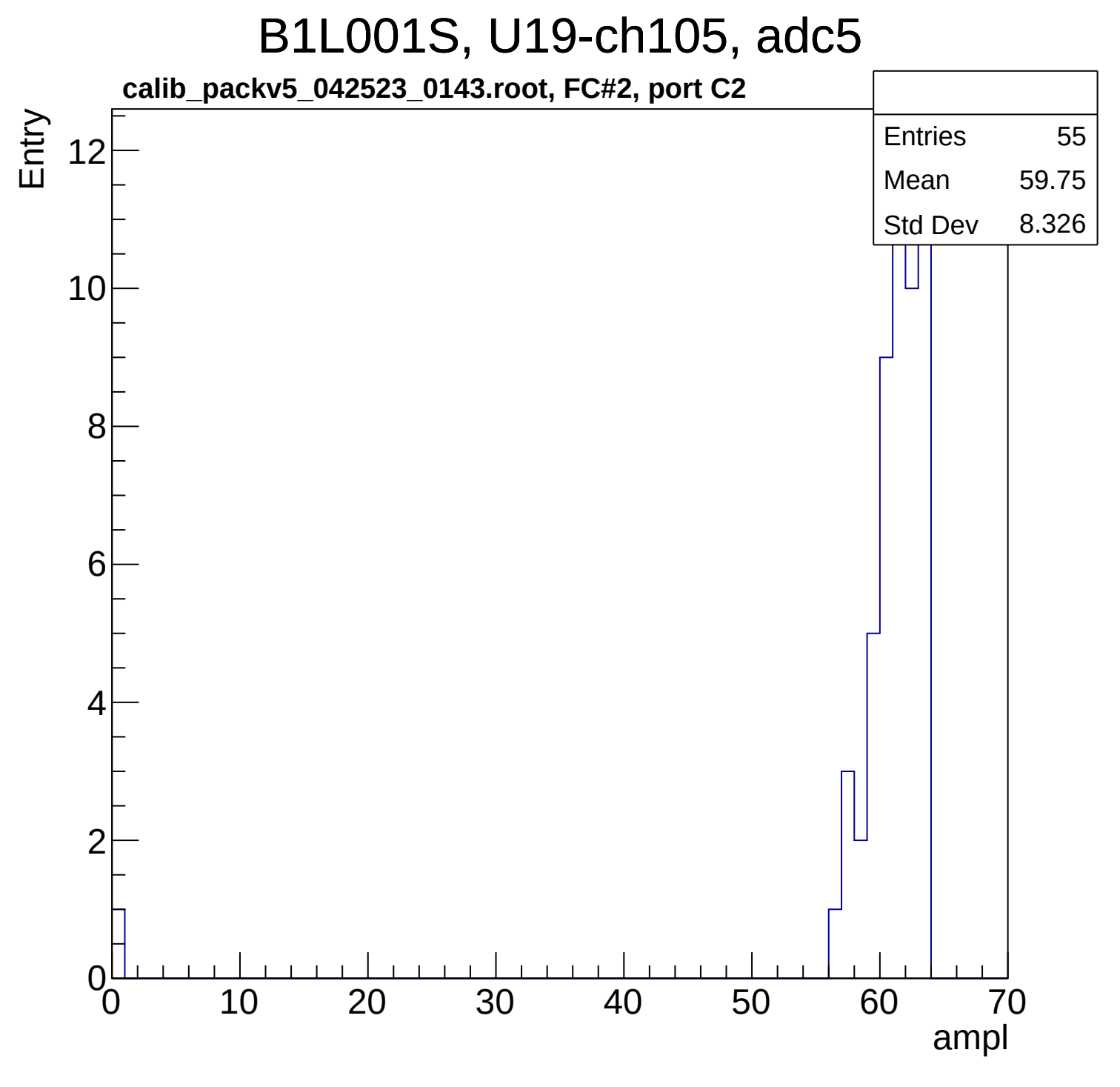
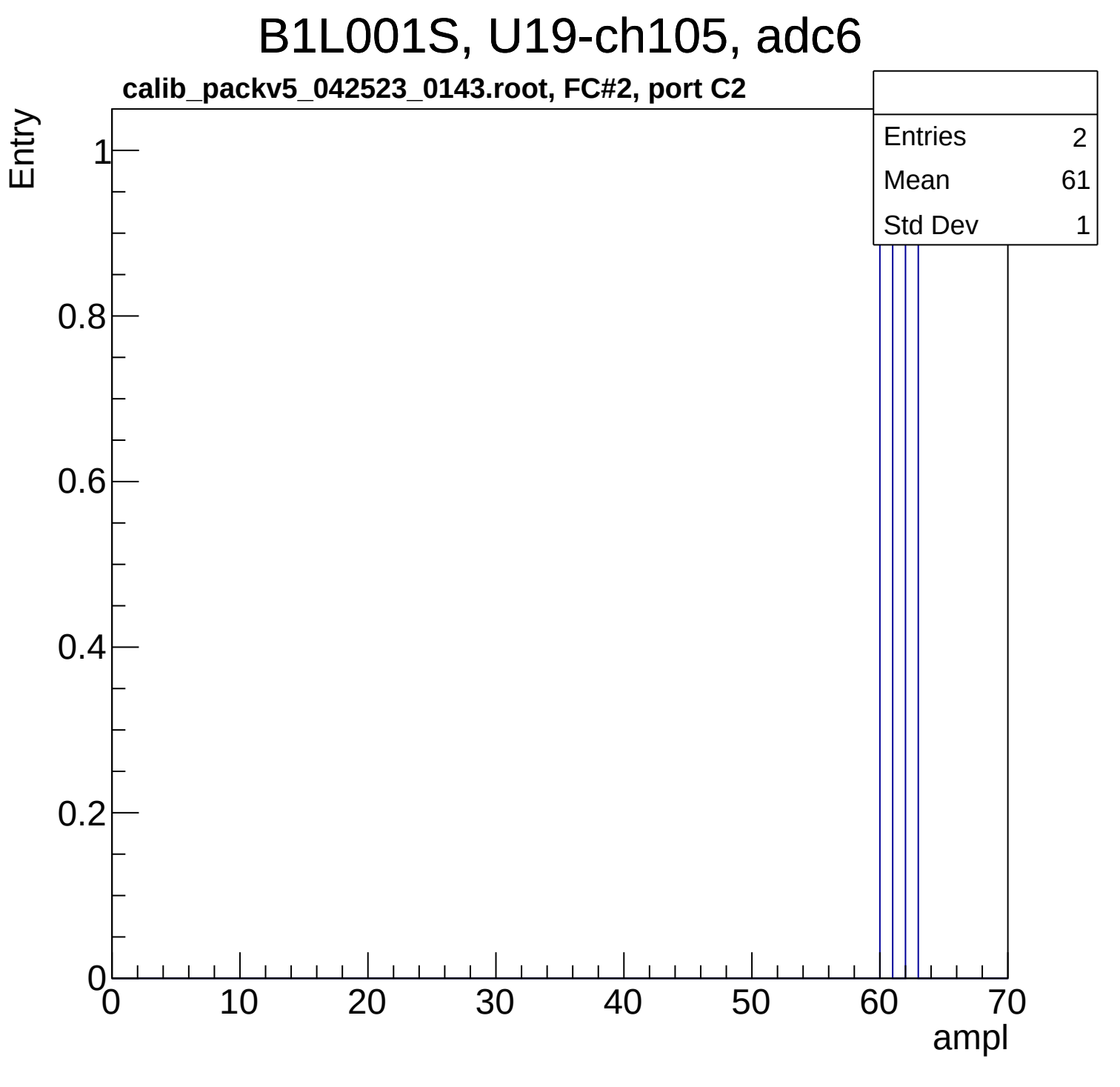
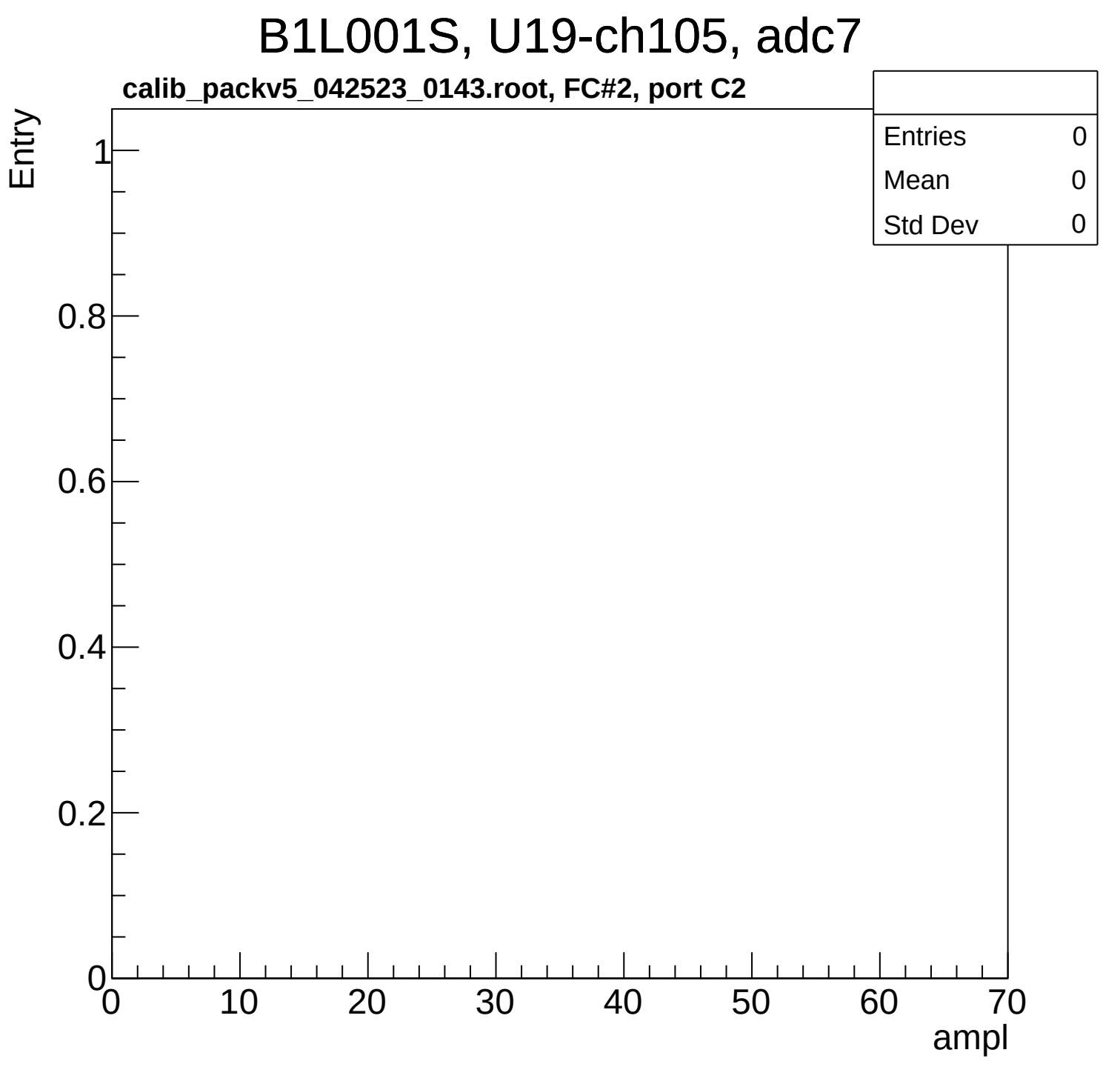

B1L001S, U19-ch105, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 120
Mean 57.03
Std Dev 6.191
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L001S, U19-ch105, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 55
Mean 59.75
Std Dev 8.326
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch105, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 61
Std Dev 1
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch105, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 0
Mean 0
Std Dev 0
Entry
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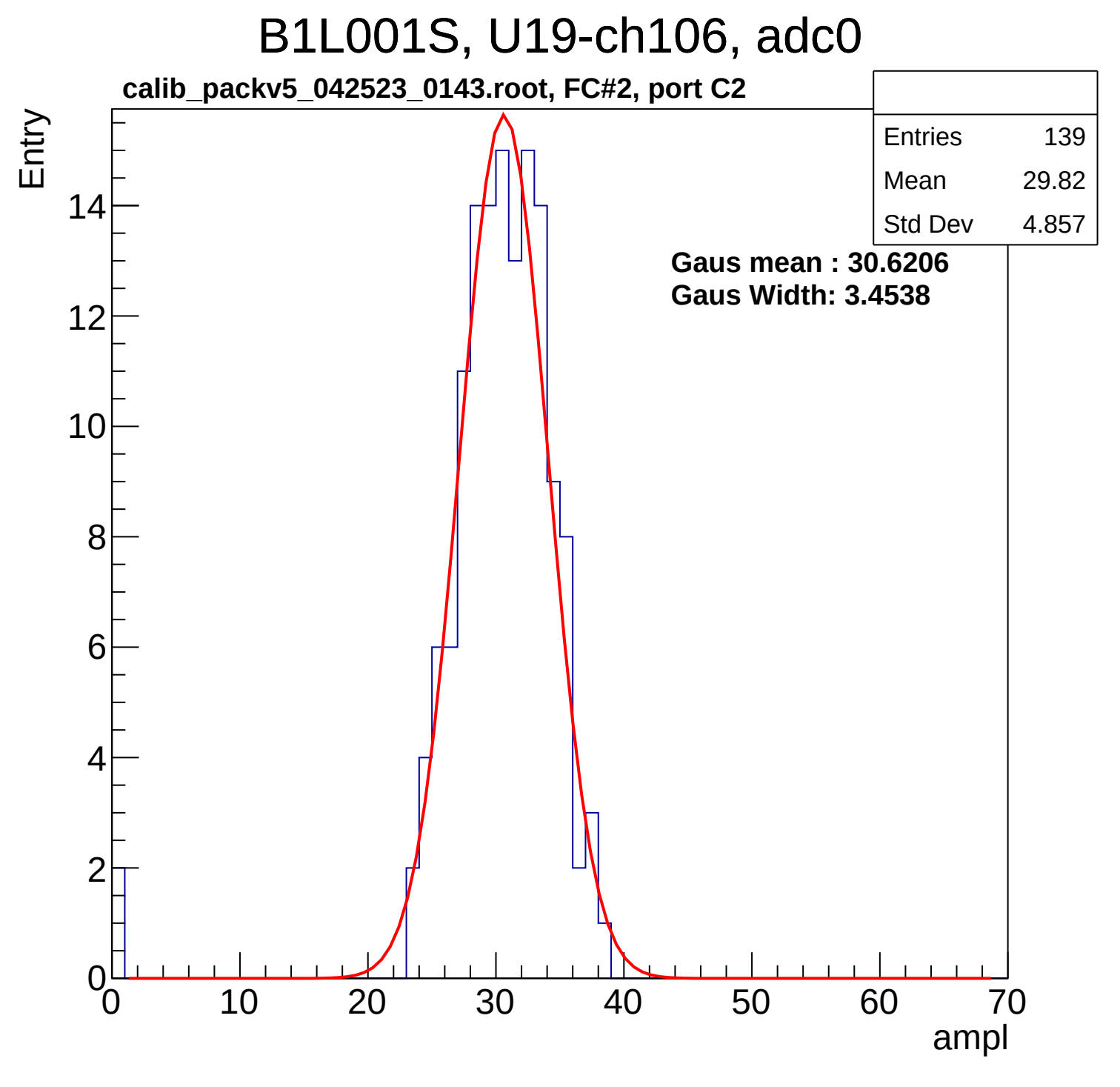
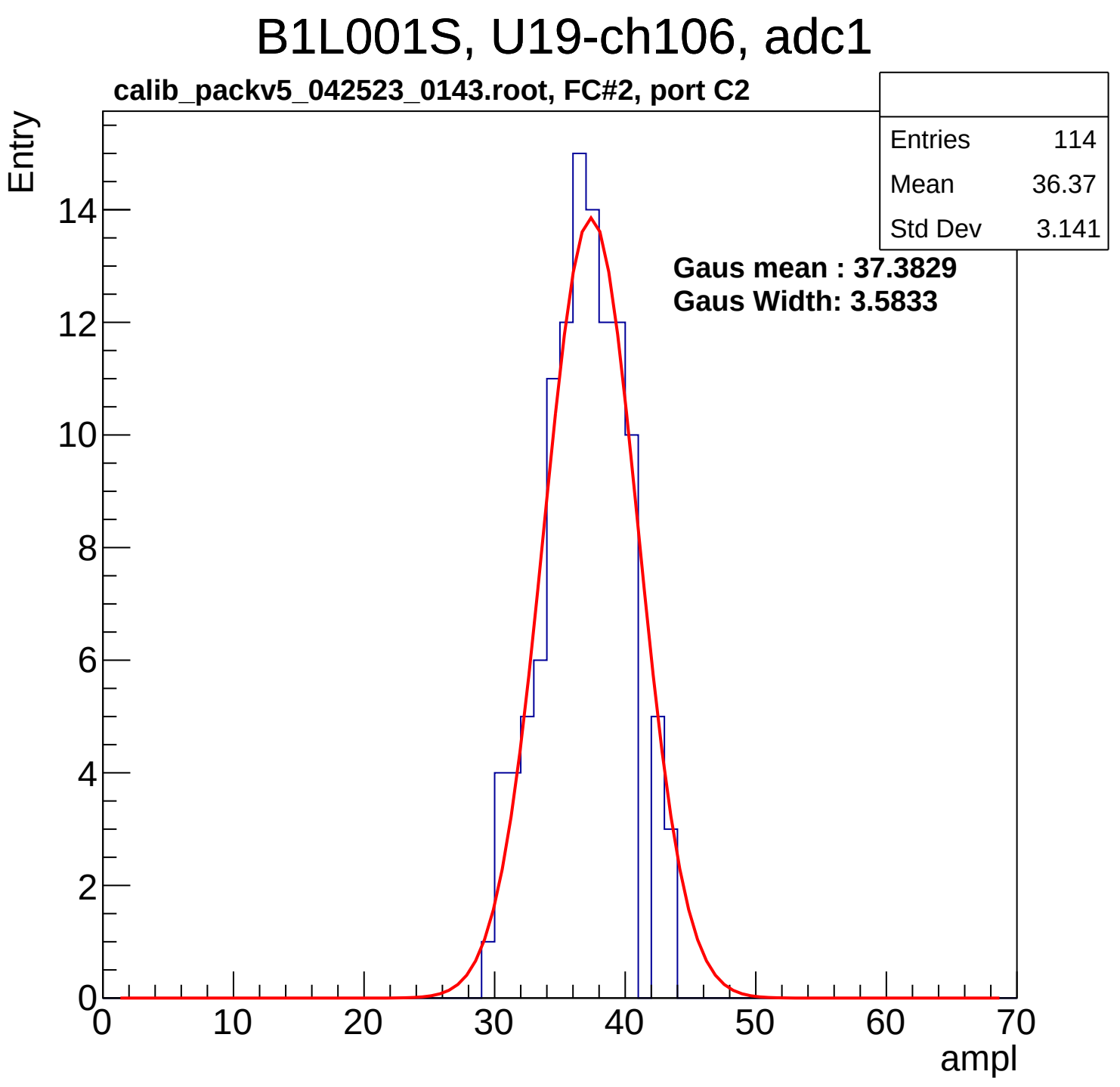
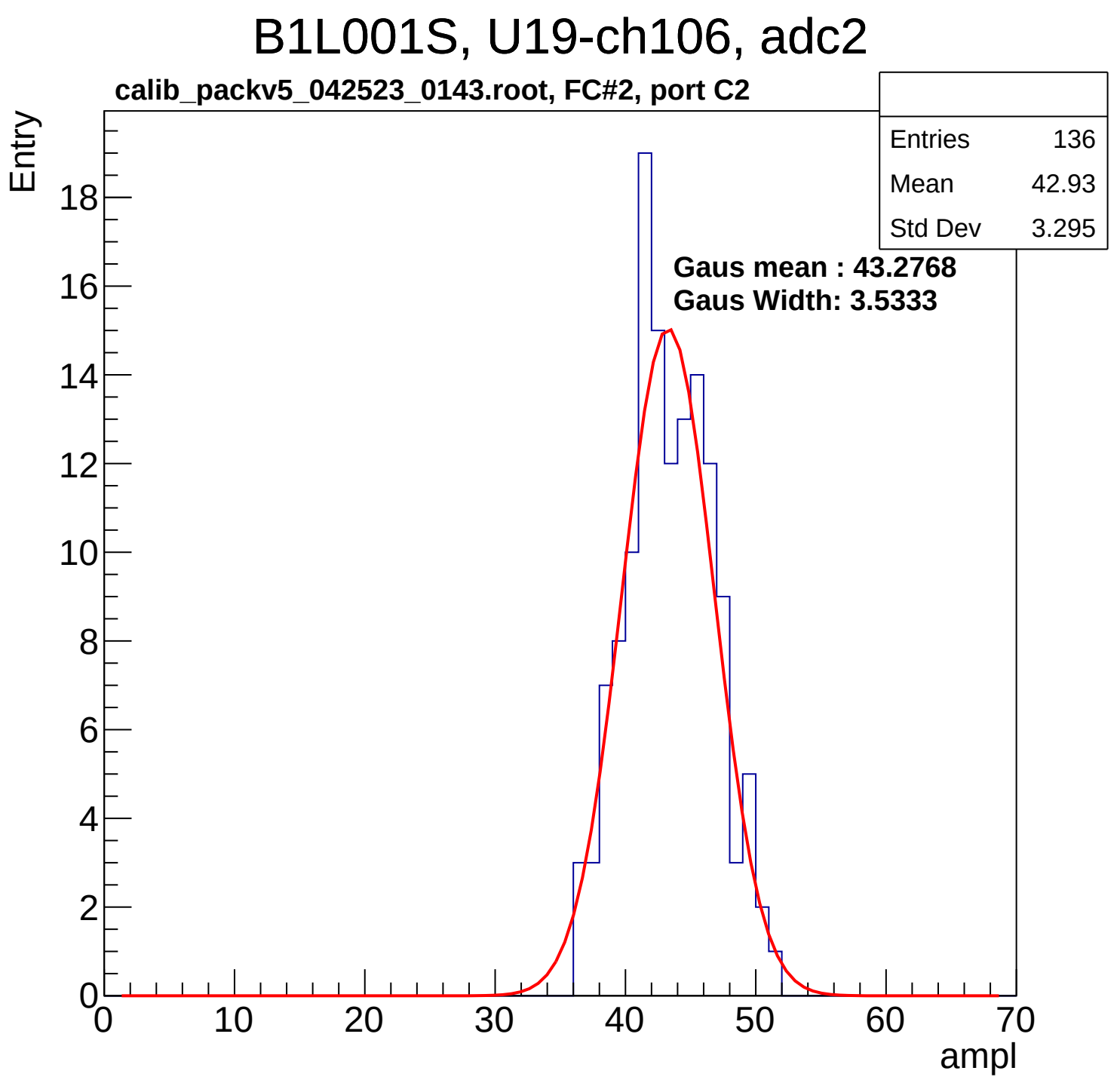
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch106, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 139
Mean 29.82
Std Dev 4.857
Gaus mean : 30.6206
Gaus Width: 3.4538
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L001S, U19-ch106, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 114
Mean 36.37
Std Dev 3.141
Gaus mean : 37.3829
Gaus Width: 3.5833
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L001S, U19-ch106, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 136
Mean 42.93
Std Dev 3.295
Gaus mean : 43.2768
Gaus Width: 3.5333
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
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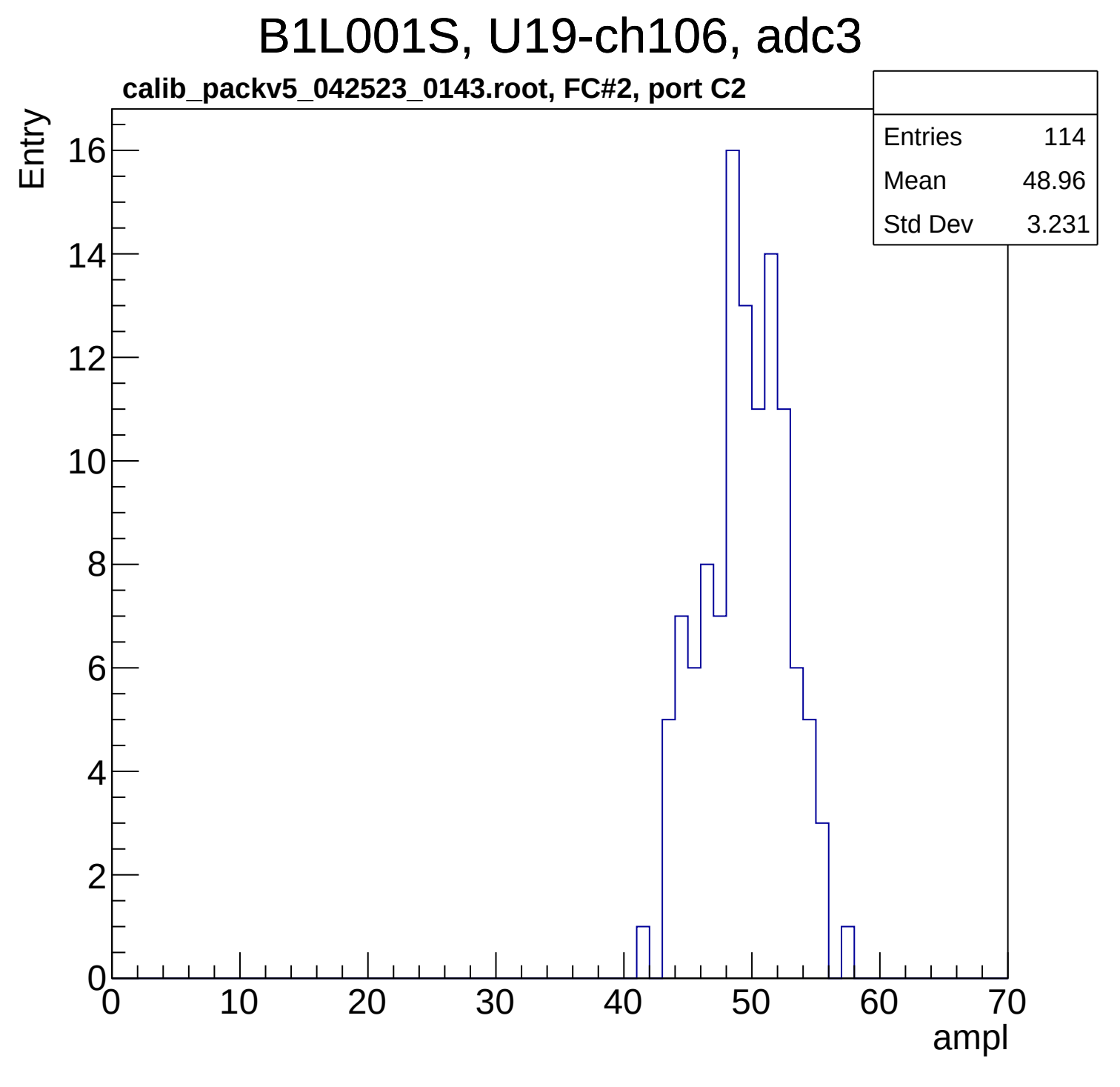
B1L001S, U19-ch106, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 114
Mean 48.96
Std Dev 3.231
Entry
ampl
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2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
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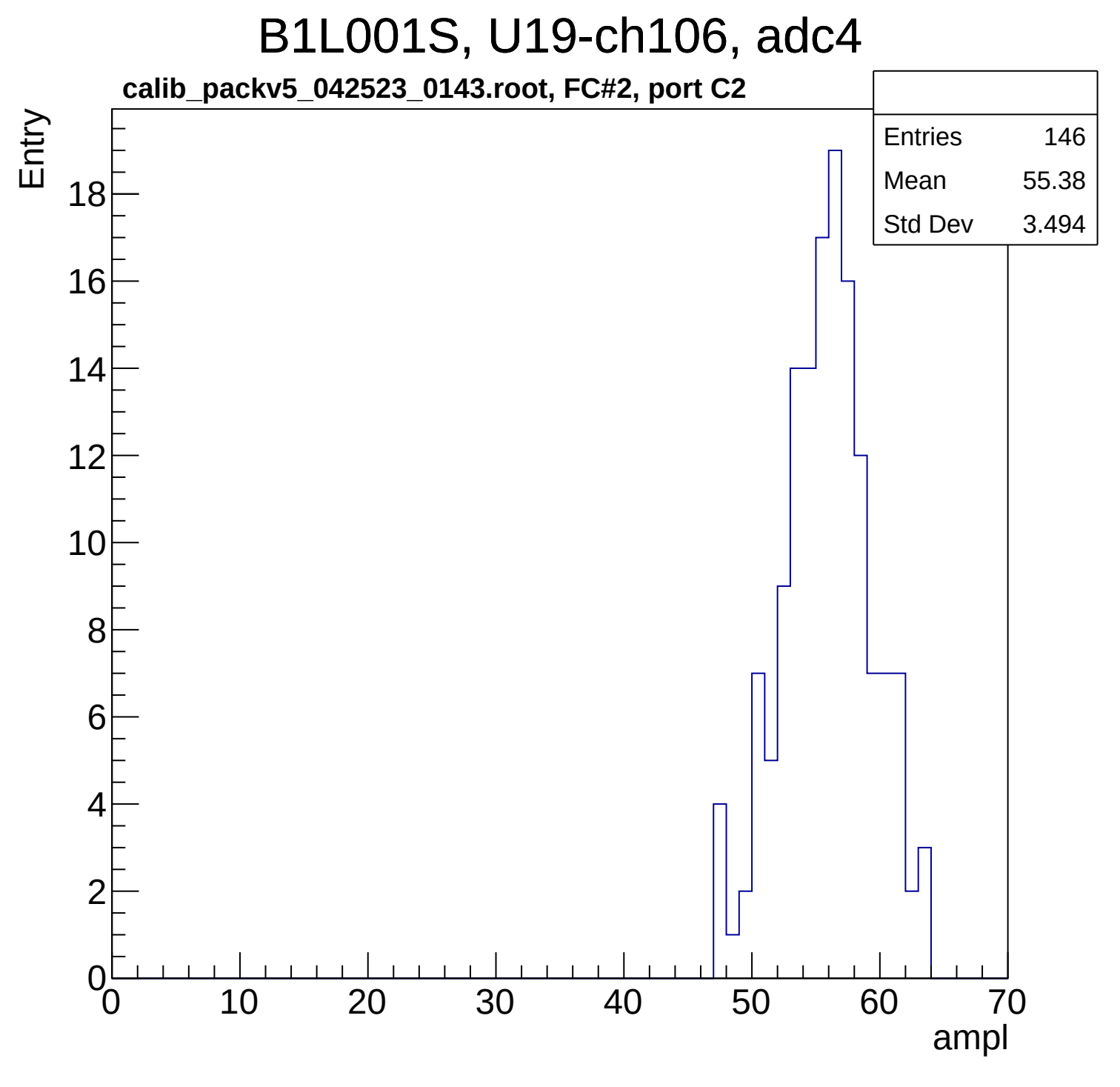
B1L001S, U19-ch106, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 146
Mean 55.38
Std Dev 3.494
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
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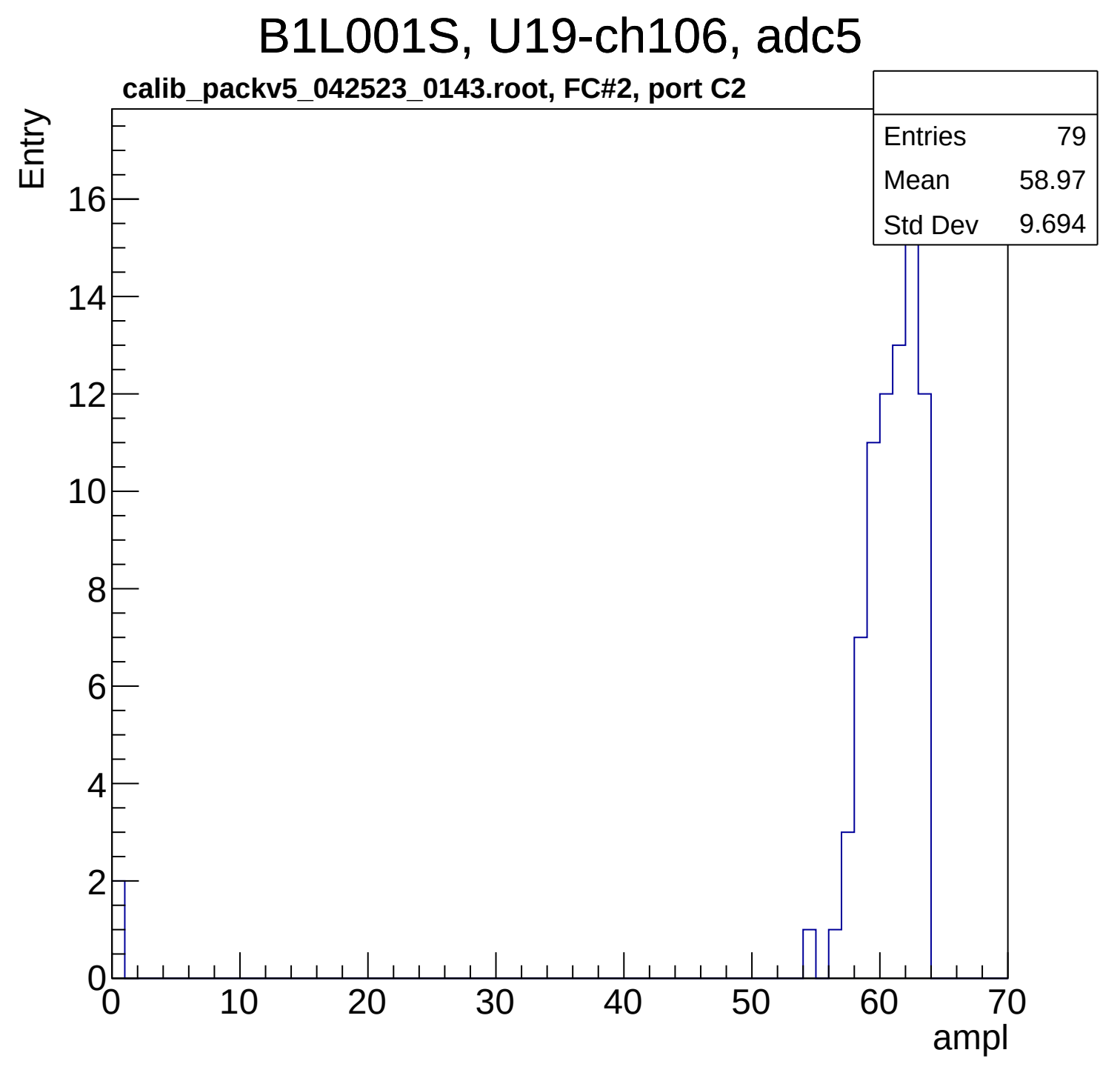
B1L001S, U19-ch106, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 79
Mean 58.97
Std Dev 9.694
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
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60
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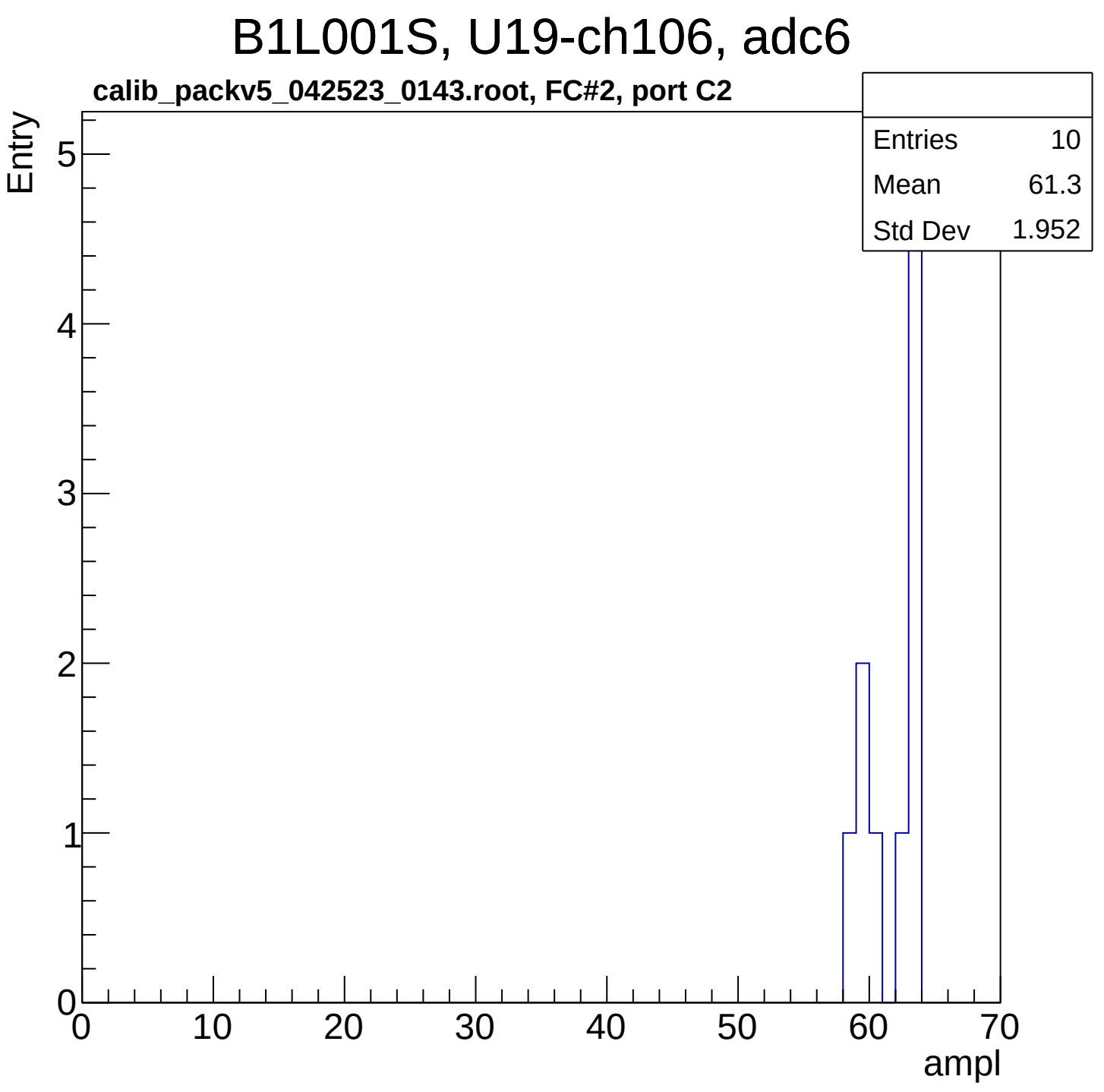
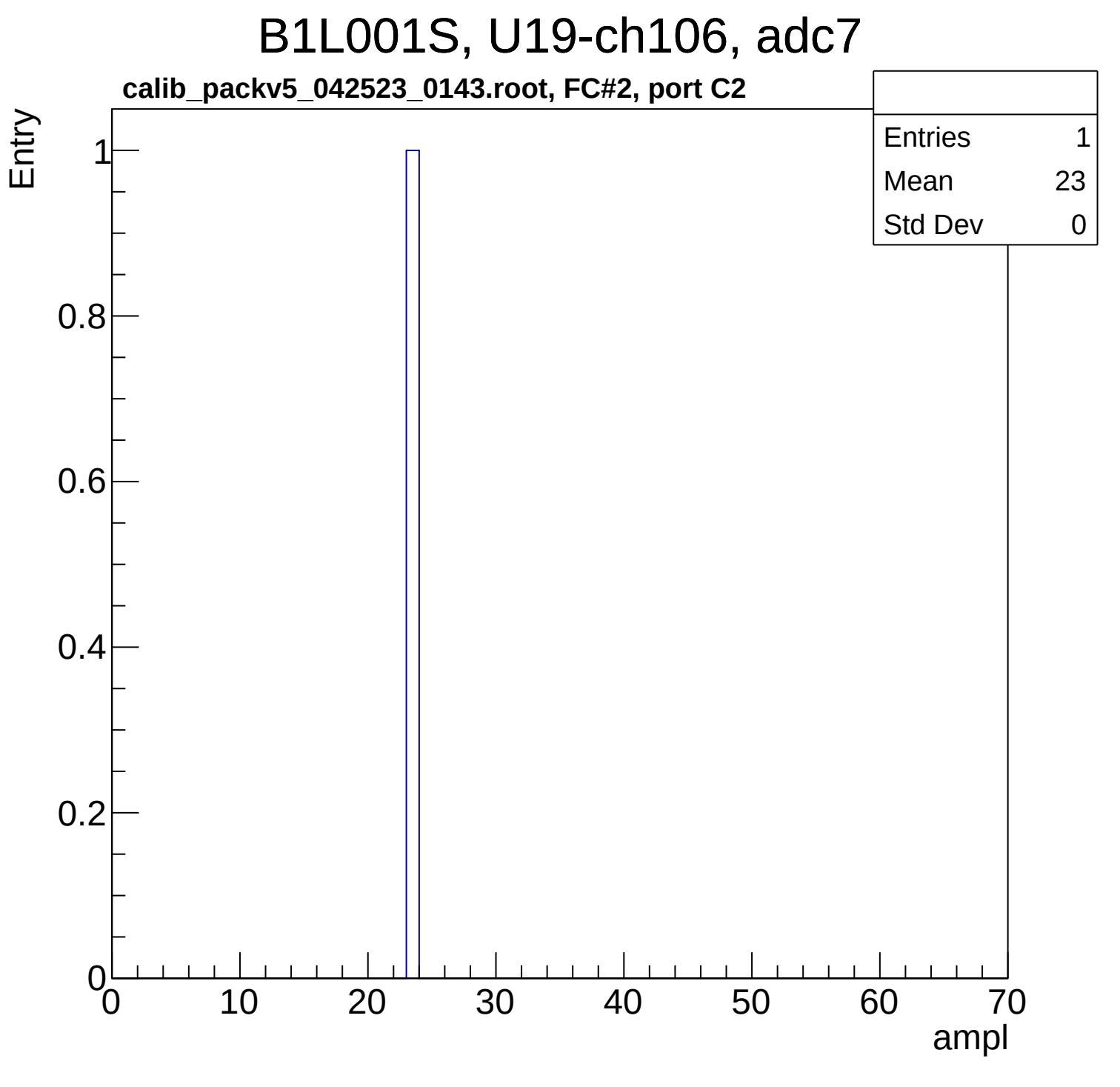

B1L001S, U19-ch106, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 10
Mean 61.3
Std Dev 1.952
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch106, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 23
Std Dev 0
Entry
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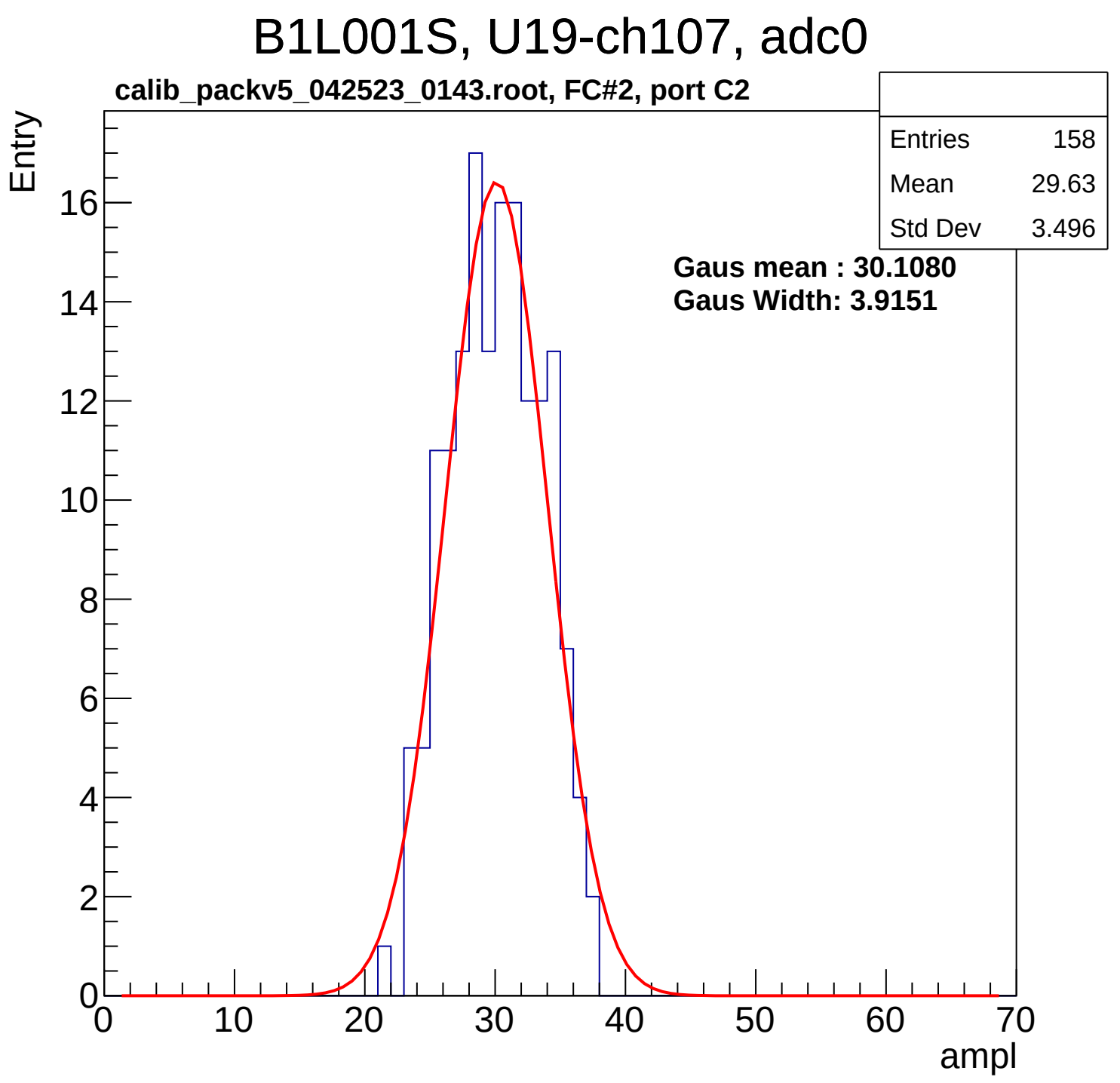
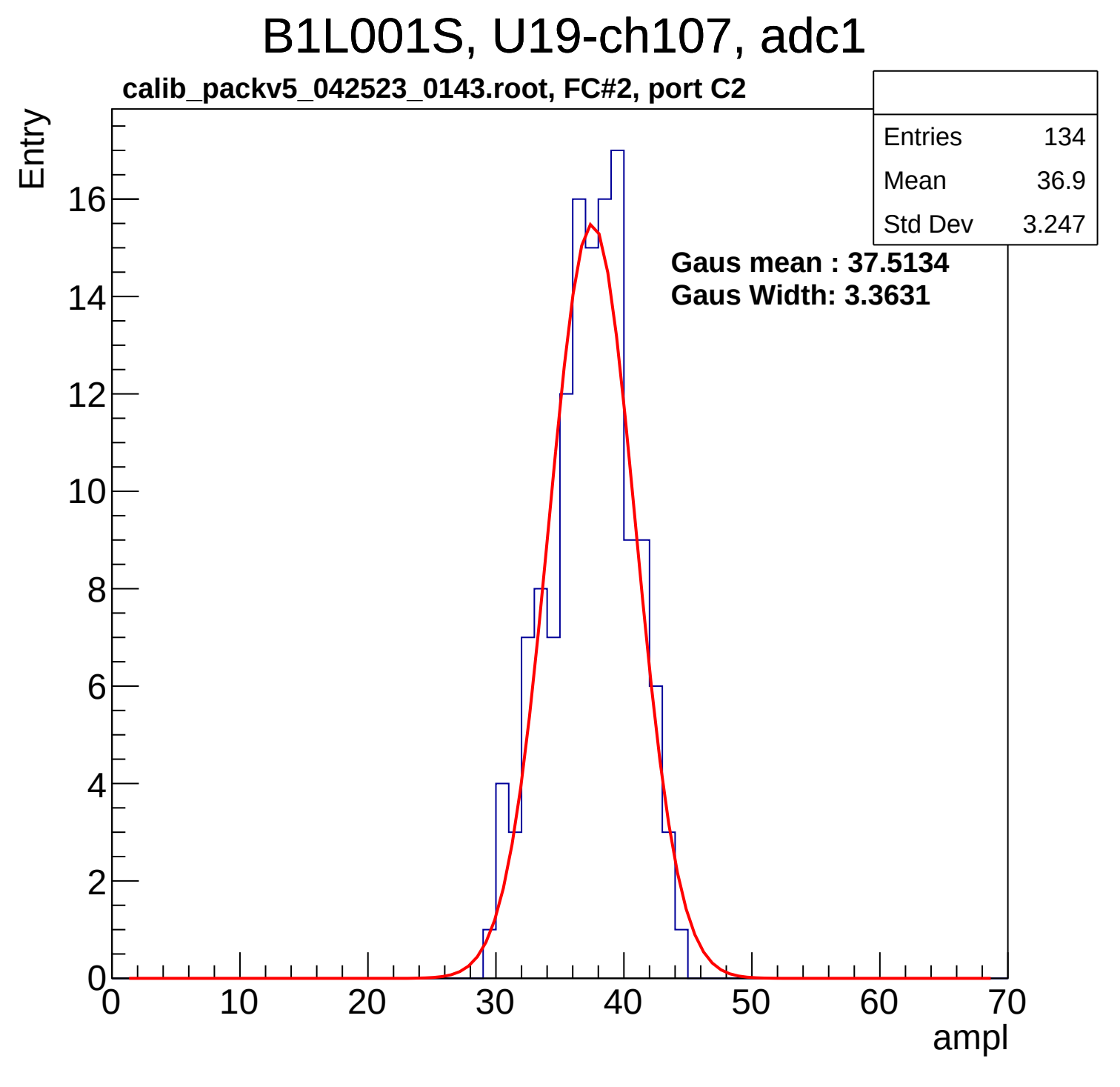
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch107, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 158
Mean 29.63
Std Dev 3.496
Gaus mean : 30.1080
Gaus Width: 3.9151
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70


B1L001S, U19-ch107, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 134
Mean 36.9
Std Dev 3.247
Gaus mean : 37.5134
Gaus Width: 3.3631
Entry
ampl
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2
4
6
8
10
12
14
16
0
10
20
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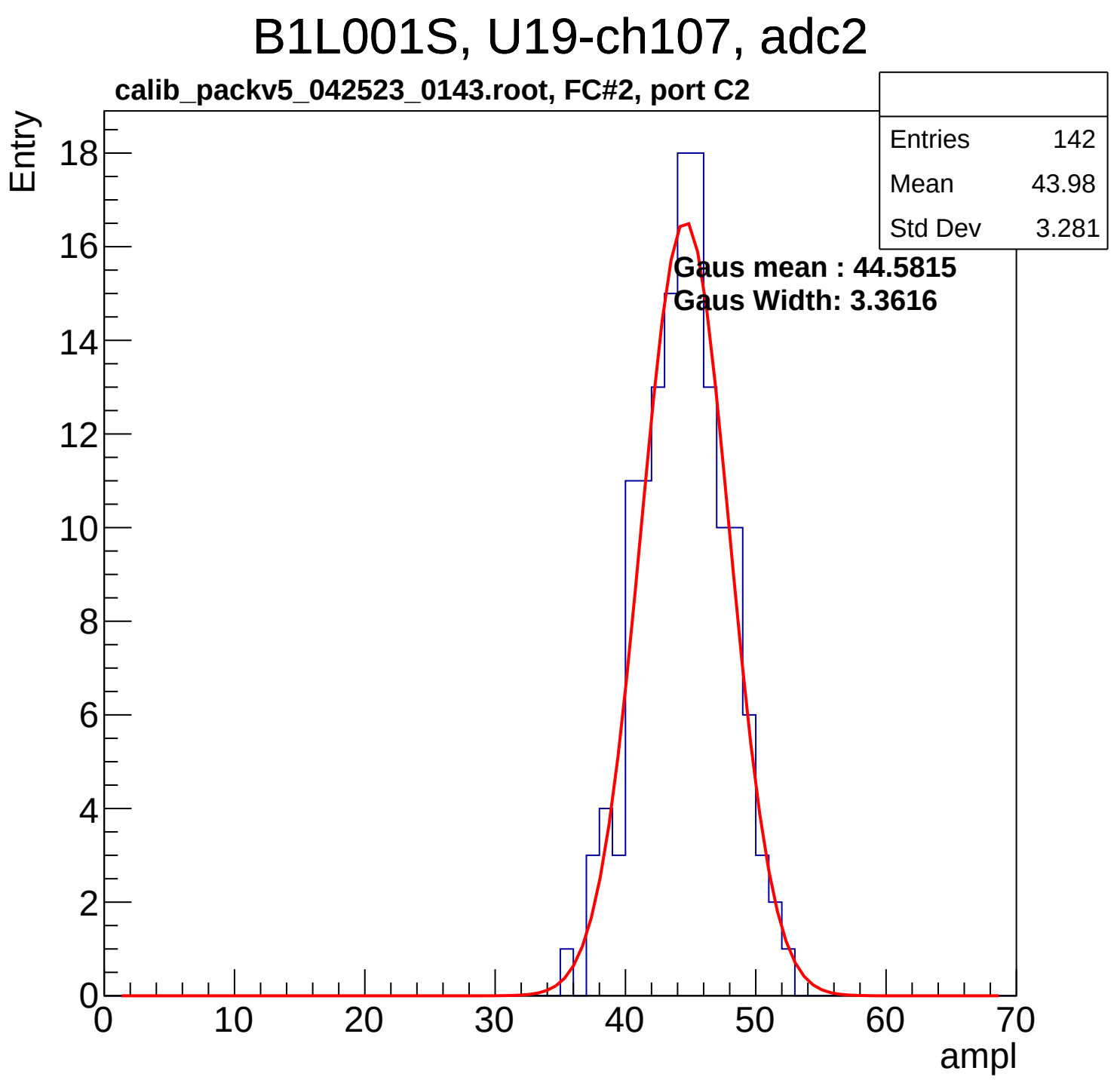
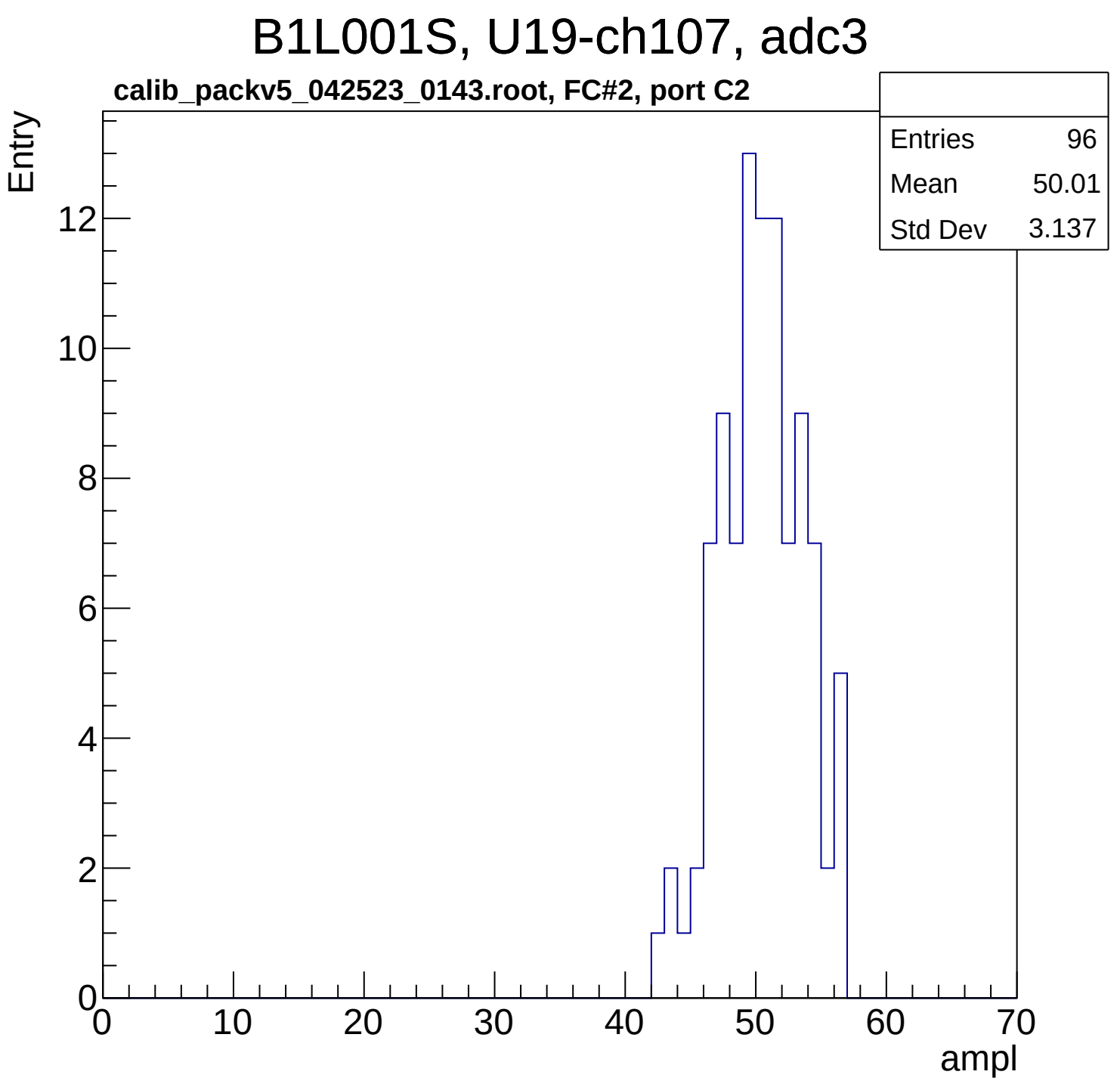
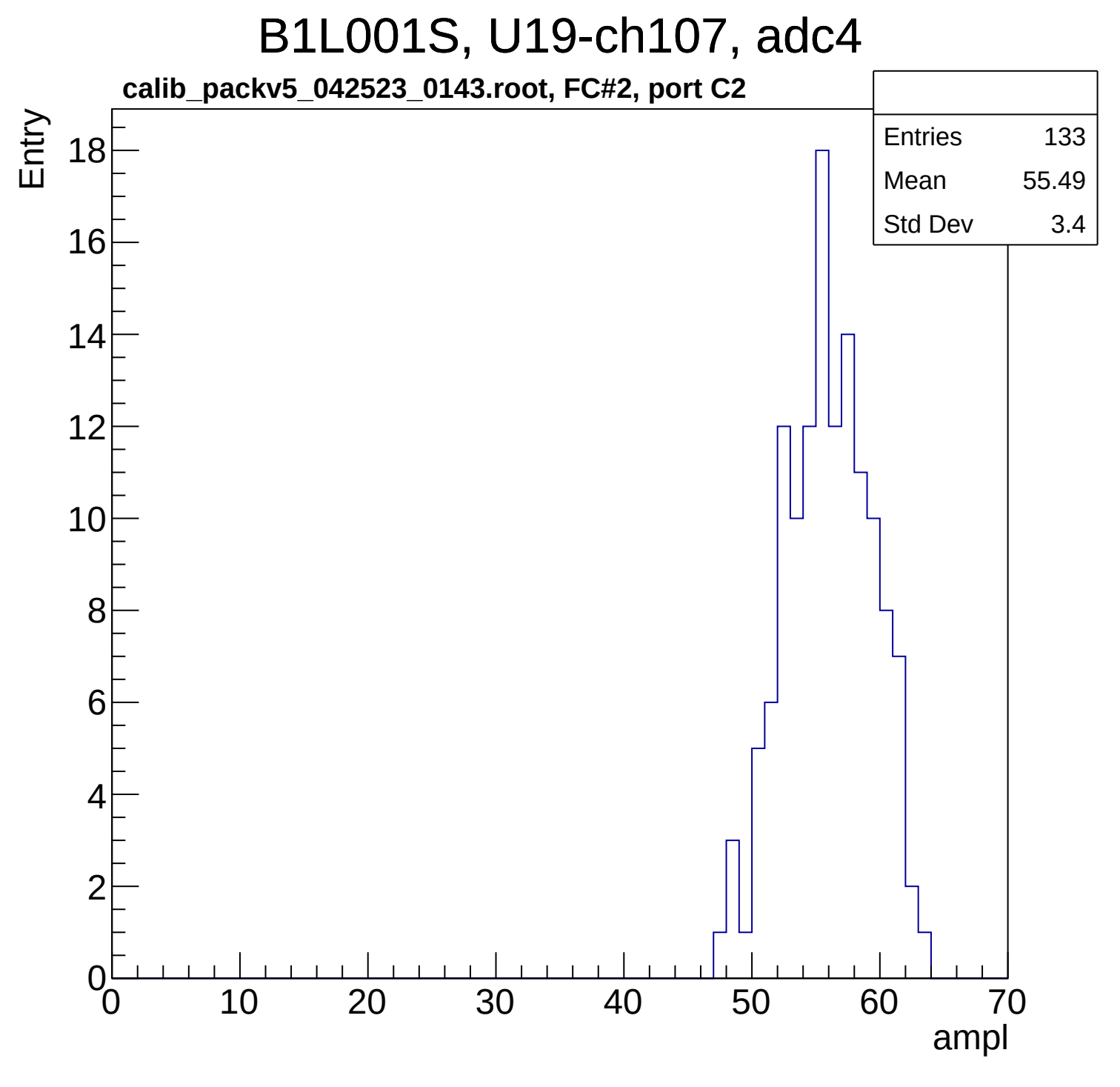
40
50
60
70


B1L001S, U19-ch107, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 142
Mean 43.98
Std Dev 3.281
Gaus mean : 44.5815
Gaus Width: 3.3616
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70


B1L001S, U19-ch107, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 96
Mean 50.01
Std Dev 3.137
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70


B1L001S, U19-ch107, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 133
Mean 55.49
Std Dev 3.4
Entry
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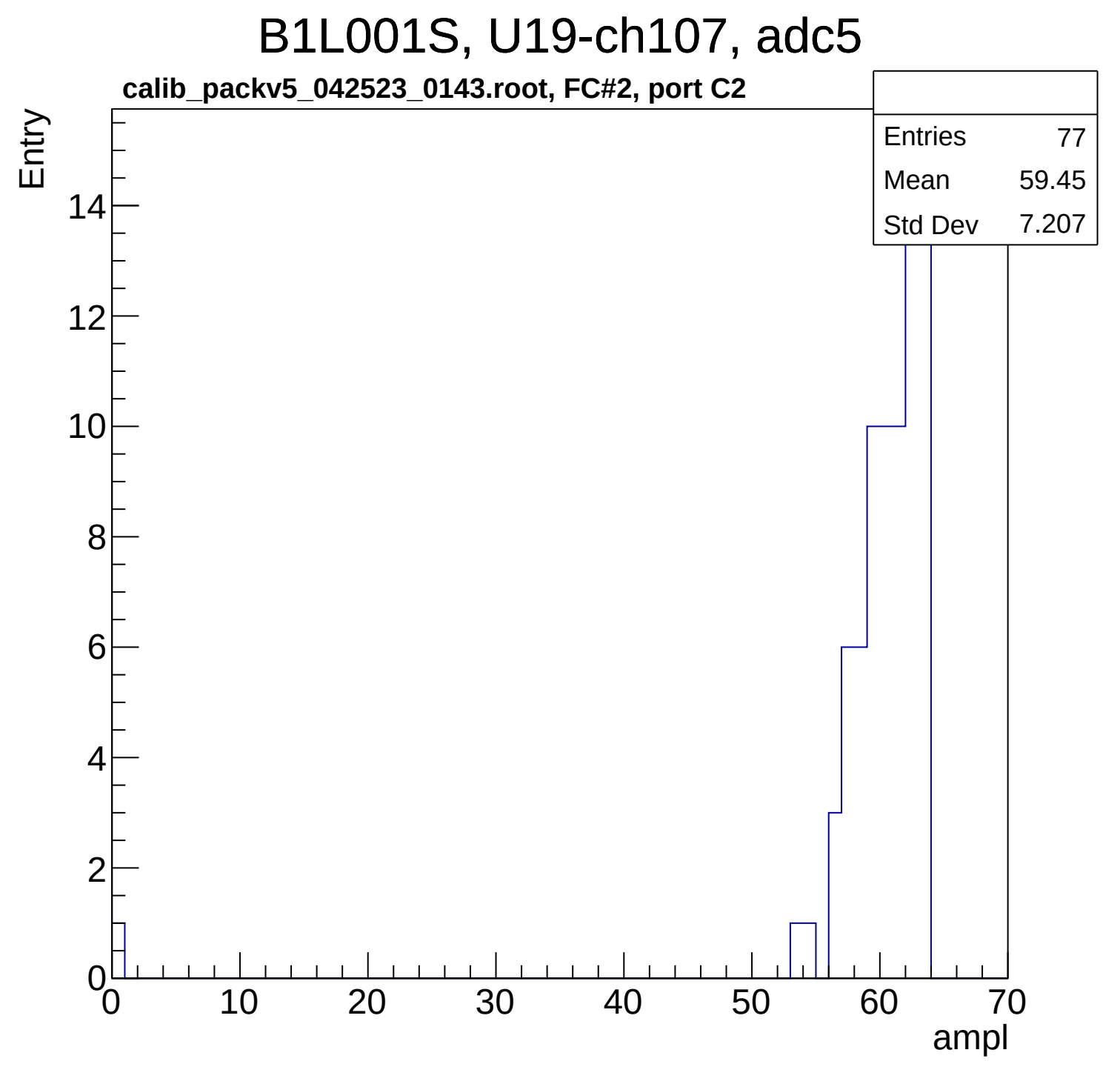
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch107, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 77
Mean 59.45
Std Dev 7.207
Entry
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10
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30
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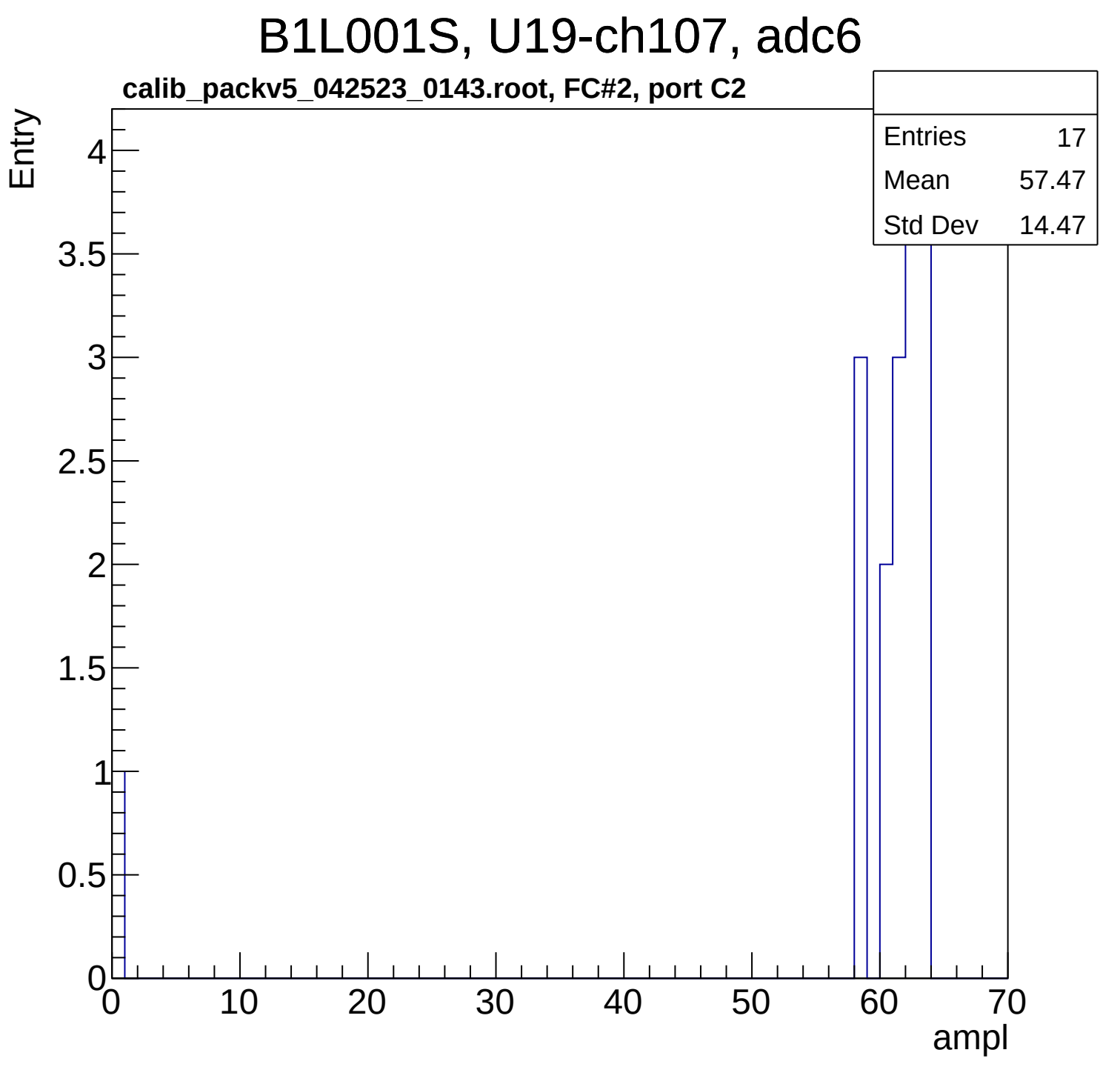
50
60
70
ampl


B1L001S, U19-ch107, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 17
Mean 57.47
Std Dev 14.47
Entry
ampl
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1
1.5
2
2.5
3
3.5
4
0
10
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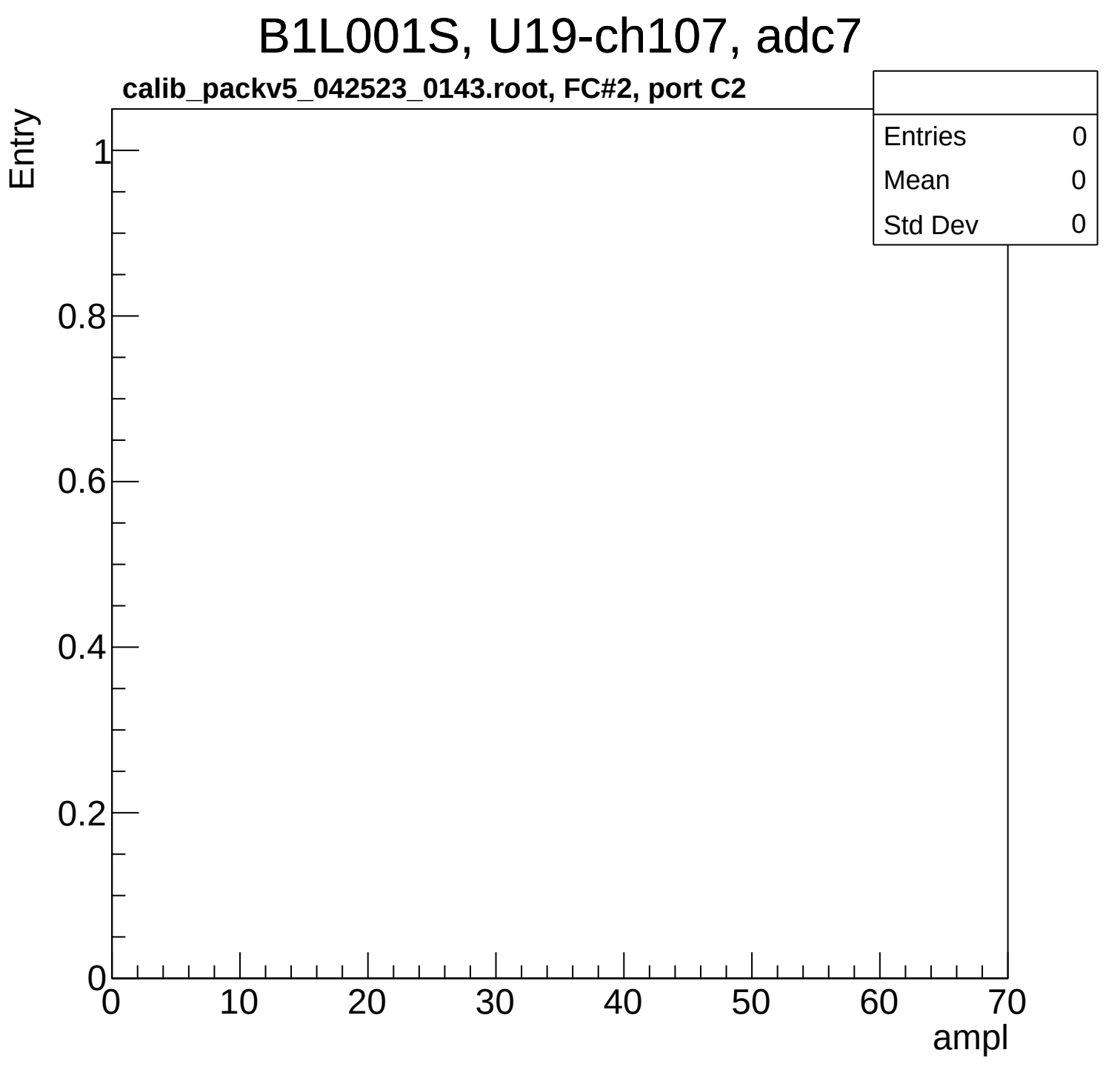
40
50
60
70


B1L001S, U19-ch107, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 0
Mean 0
Std Dev 0
Entry
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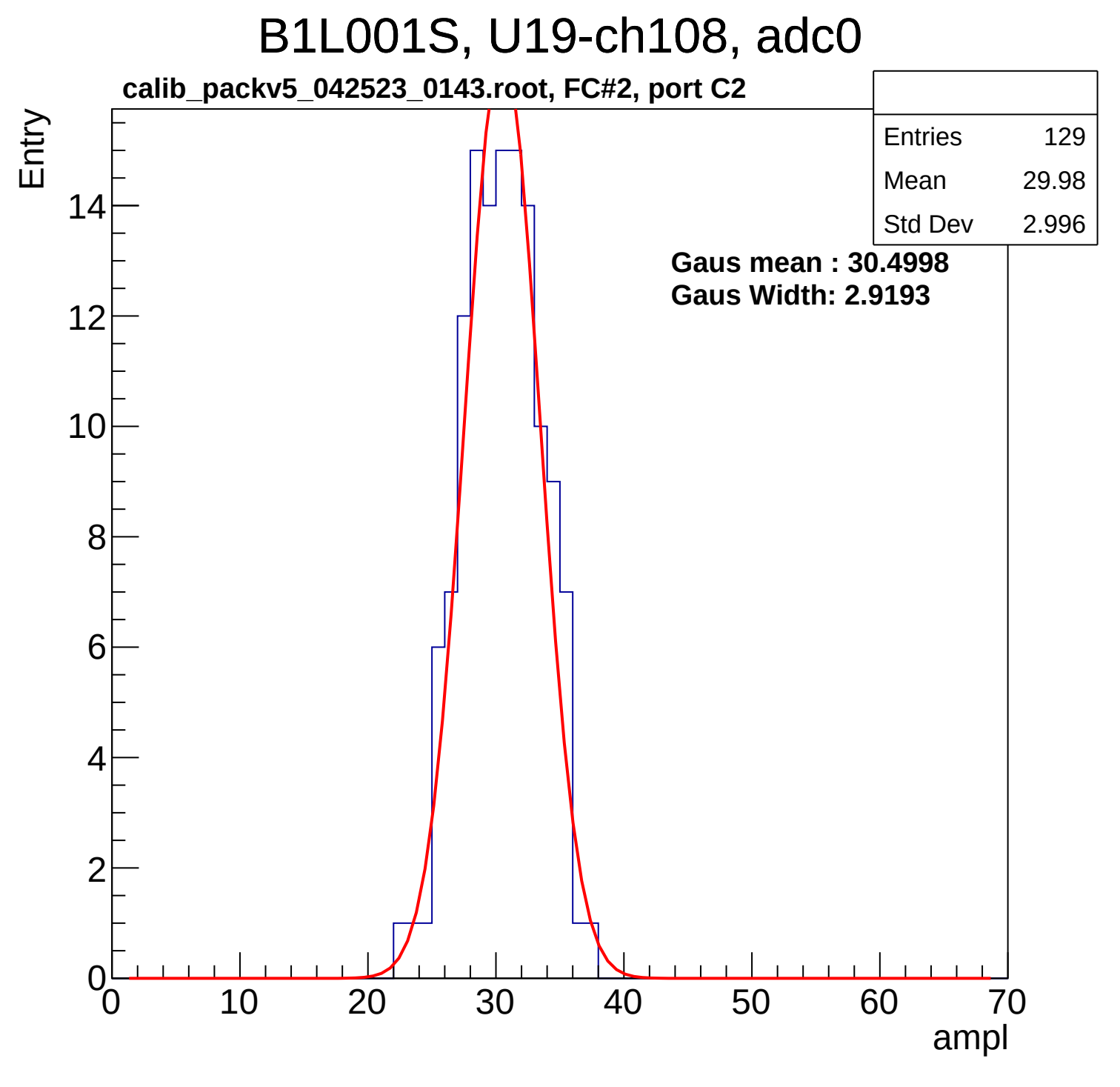
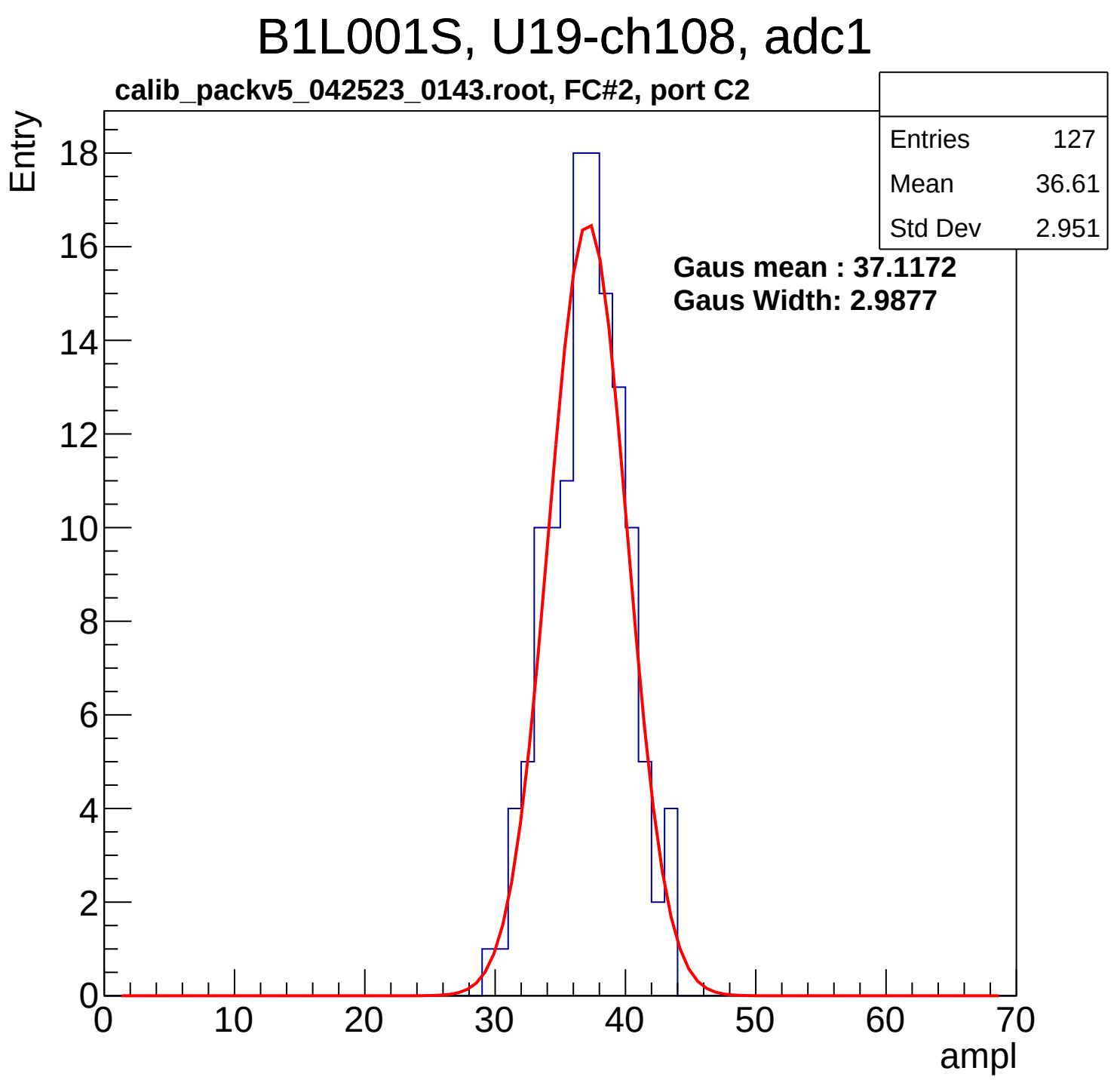
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch108, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 129
Mean 29.98
Std Dev 2.996
Gaus mean : 30.4998
Gaus Width: 2.9193
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L001S, U19-ch108, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 127
Mean 36.61
Std Dev 2.951
Gaus mean : 37.1172
Gaus Width: 2.9877
Entry
ampl
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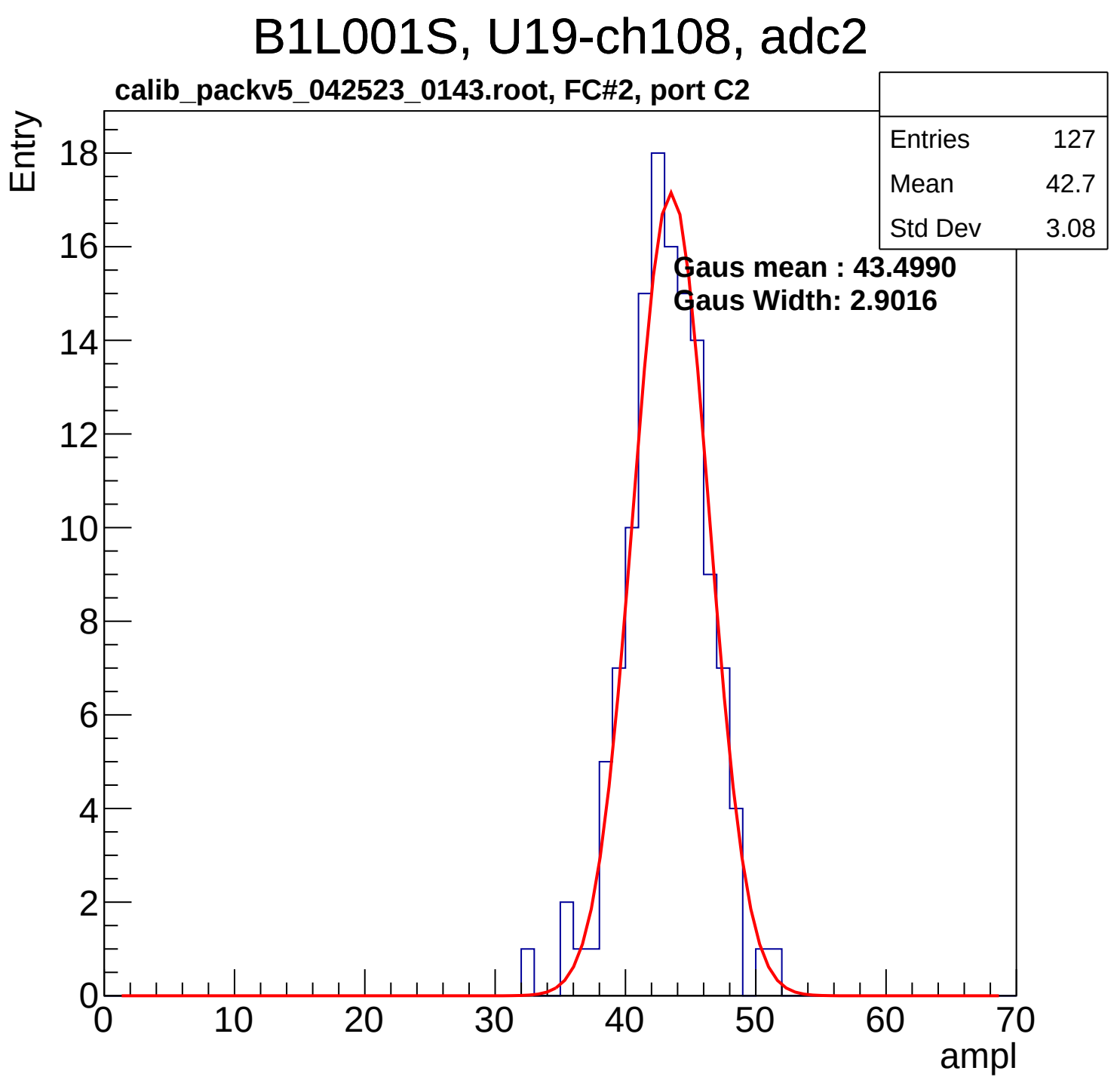
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70


B1L001S, U19-ch108, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 127
Mean 42.7
Std Dev 3.08
Gaus mean : 43.4990
Gaus Width: 2.9016
Entry
ampl
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4
6
8
10
12
14
16
18
0
10
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60
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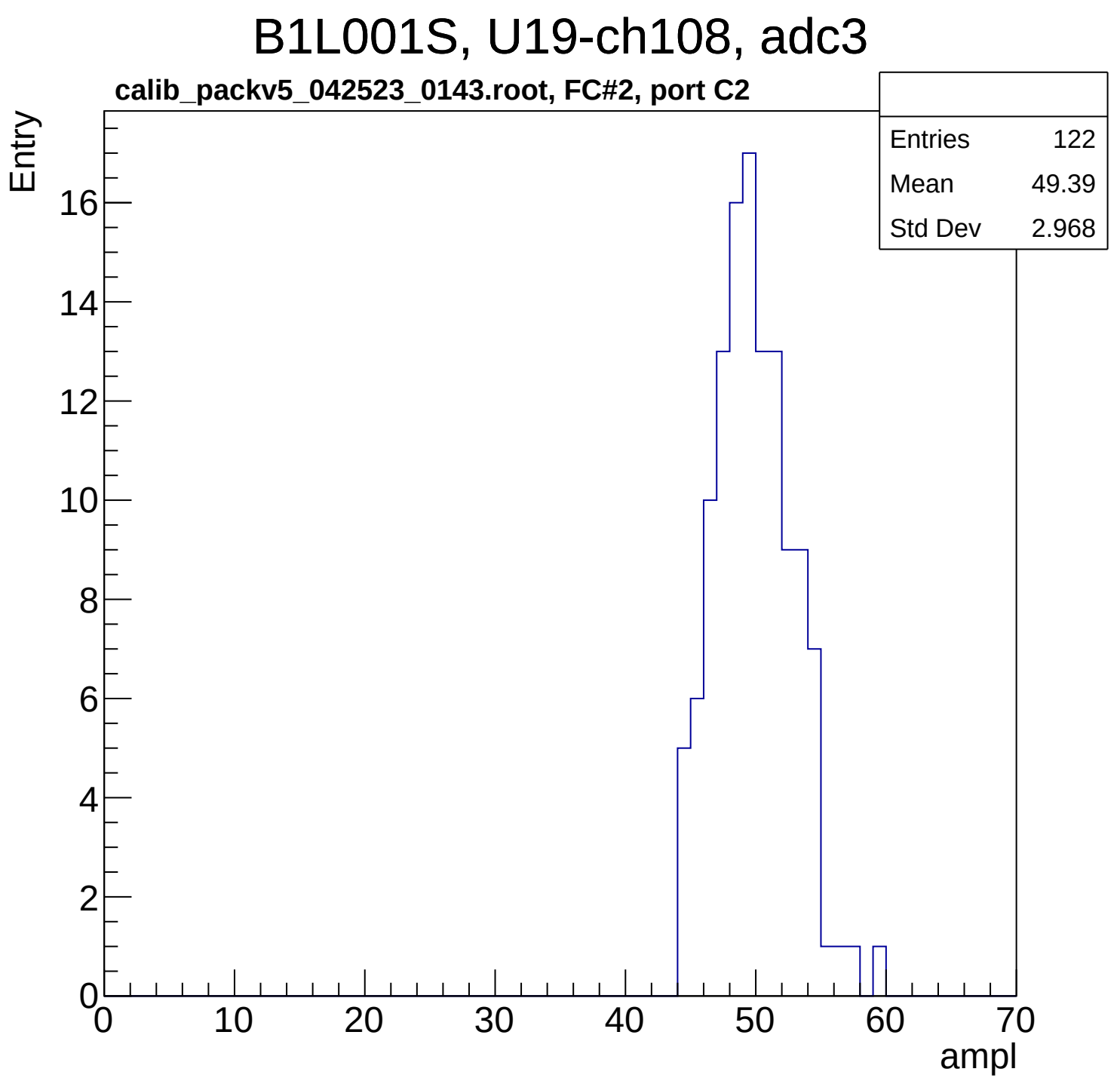
B1L001S, U19-ch108, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 122
Mean 49.39
Std Dev 2.968
Entry
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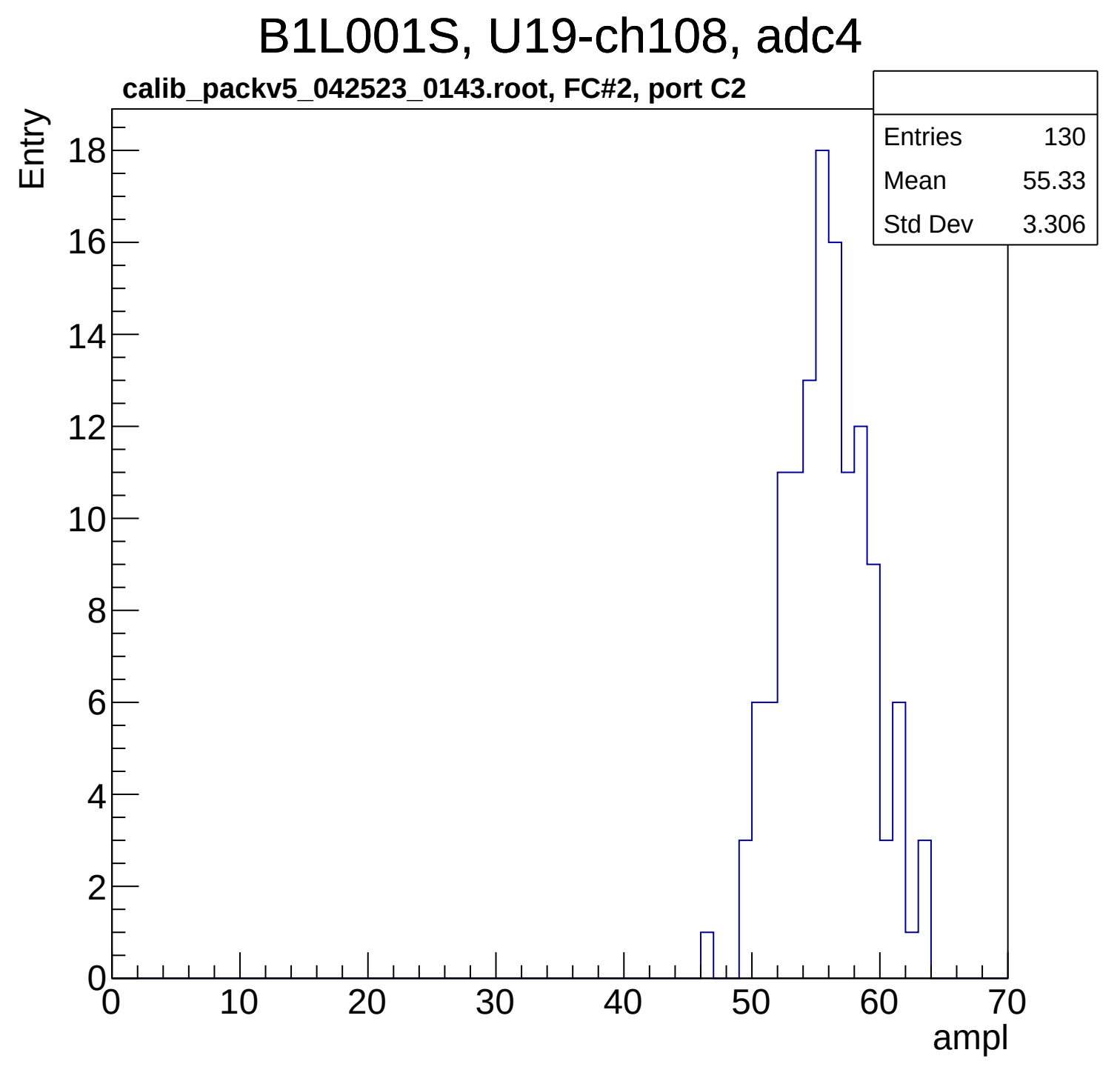
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch108, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 130
Mean 55.33
Std Dev 3.306
Entry
ampl
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2
4
6
8
10
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16
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0
10
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60
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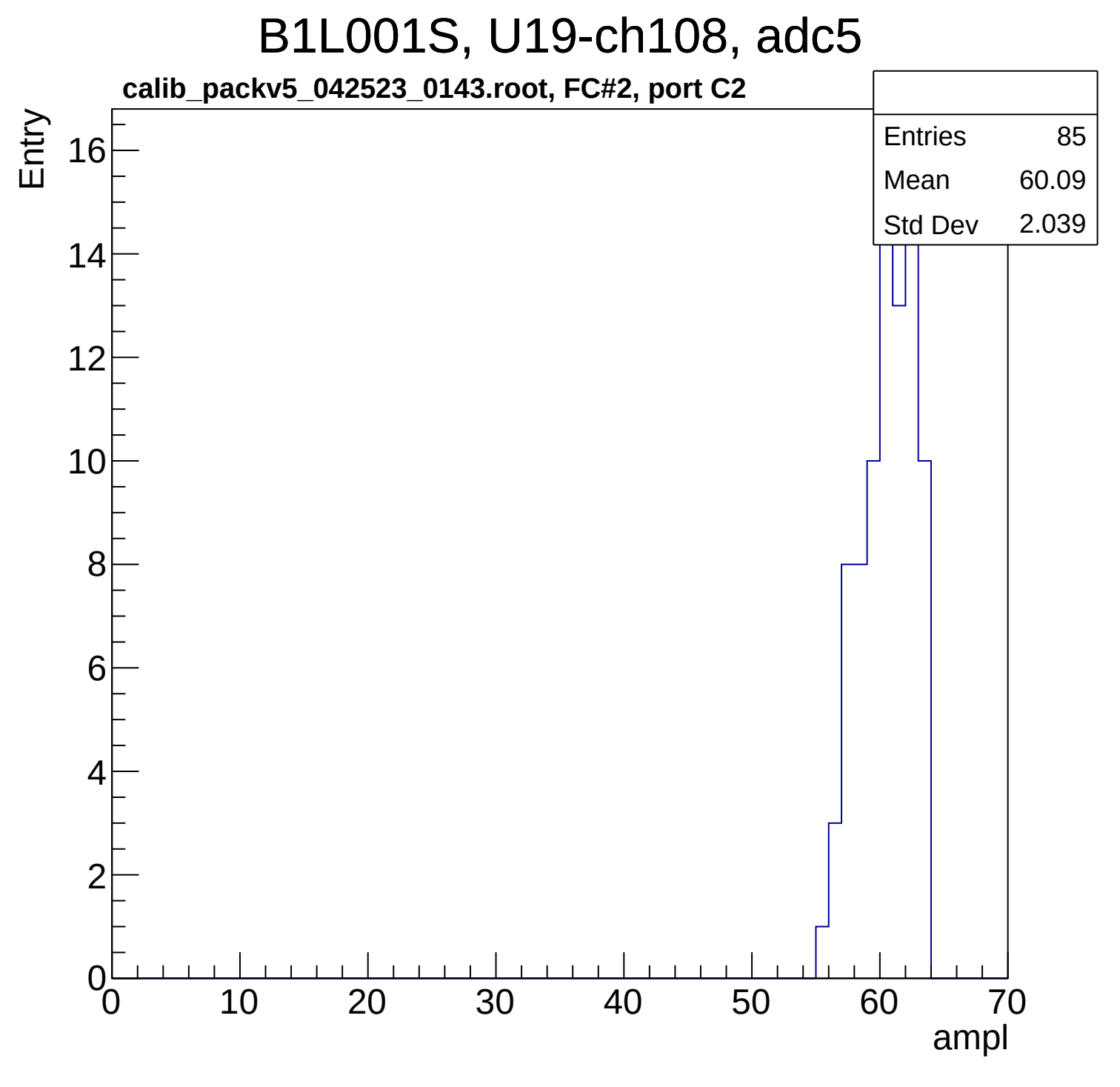
B1L001S, U19-ch108, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 85
Mean 60.09
Std Dev 2.039
Entry
ampl
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4
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8
10
12
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16
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10
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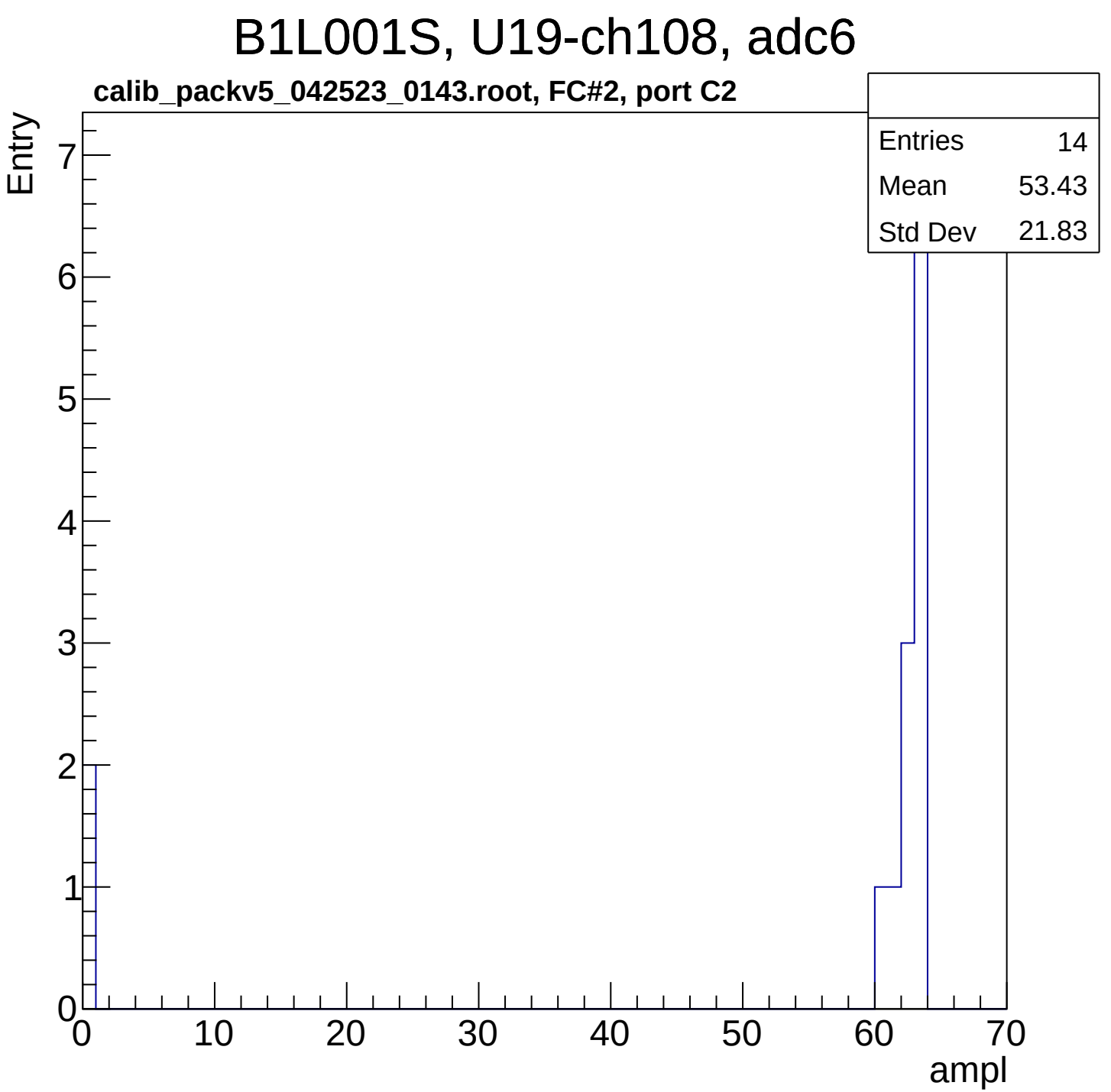
B1L001S, U19-ch108, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 14
Mean 53.43
Std Dev 21.83
Entry
ampl
0
1
2
3
4
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0
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60
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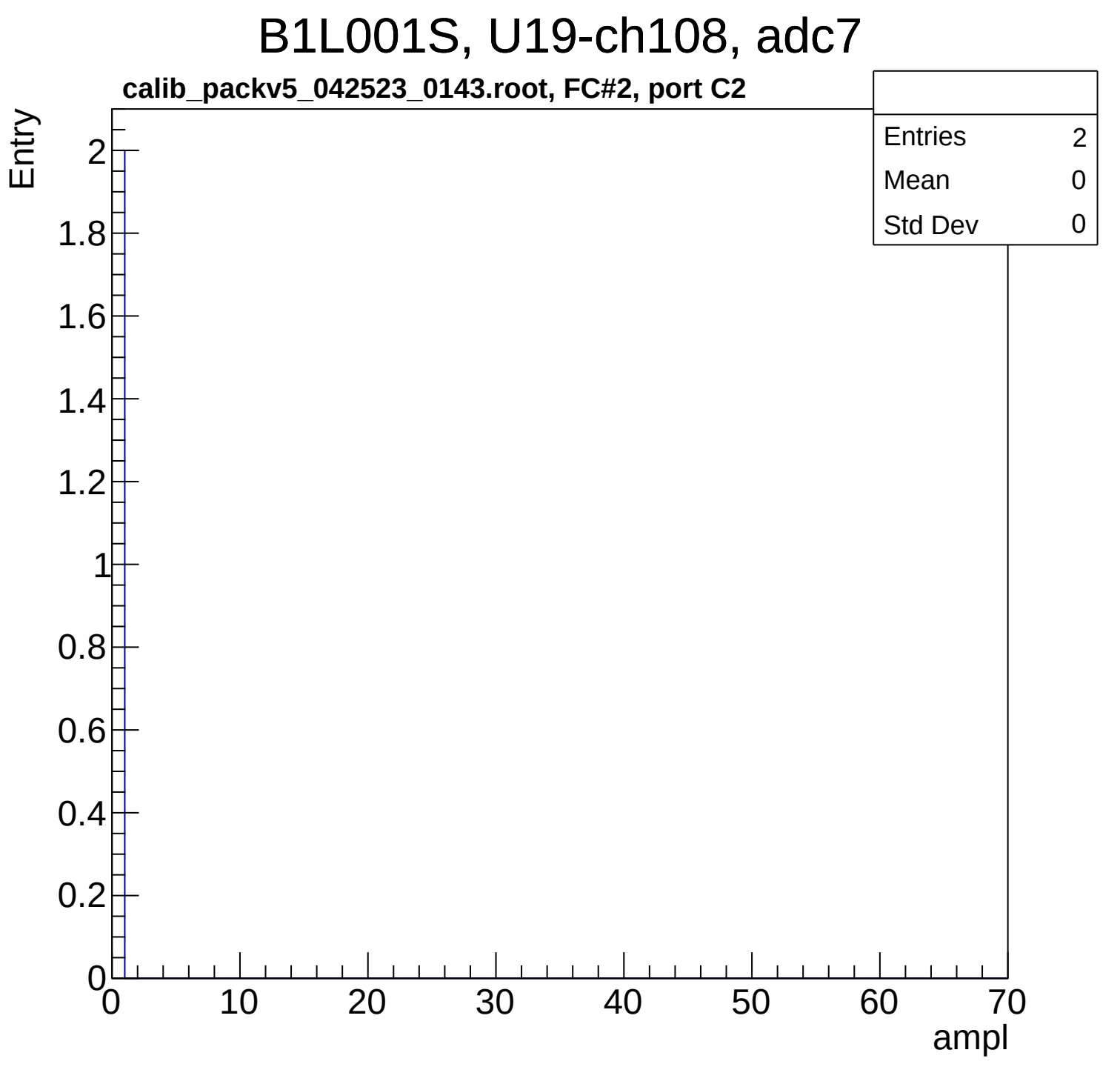
B1L001S, U19-ch108, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 0
Std Dev 0
Entry
2
1.8
1.6
1.4
1.2
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0.8
0.6
0.4
0.2
0
0
10
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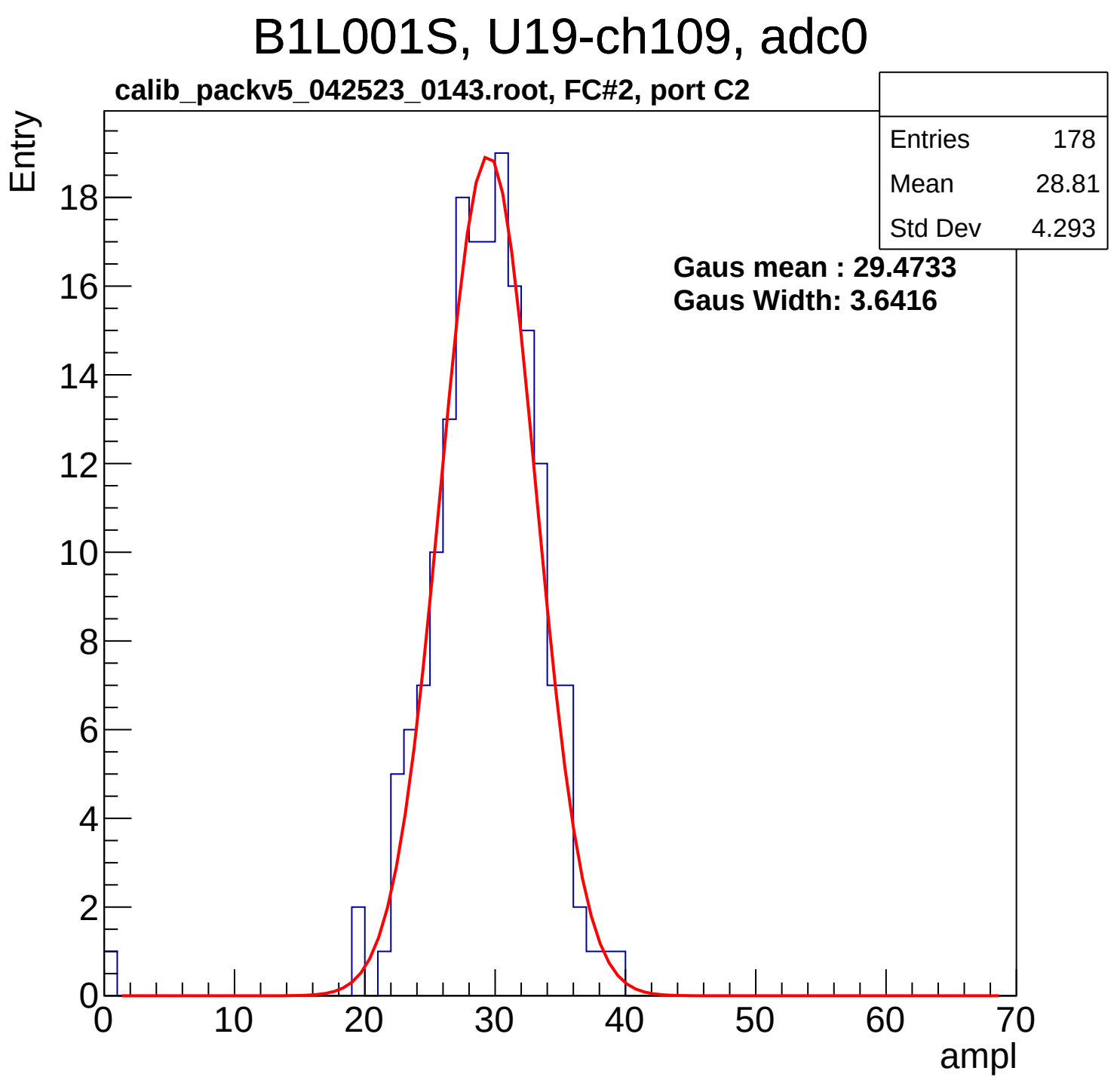
50
60
70
ampl


B1L001S, U19-ch109, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 178
Mean 28.81
Std Dev 4.293
Gaus mean : 29.4733
Gaus Width: 3.6416
Entry
ampl
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4
6
8
10
12
14
16
18
0
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40
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60
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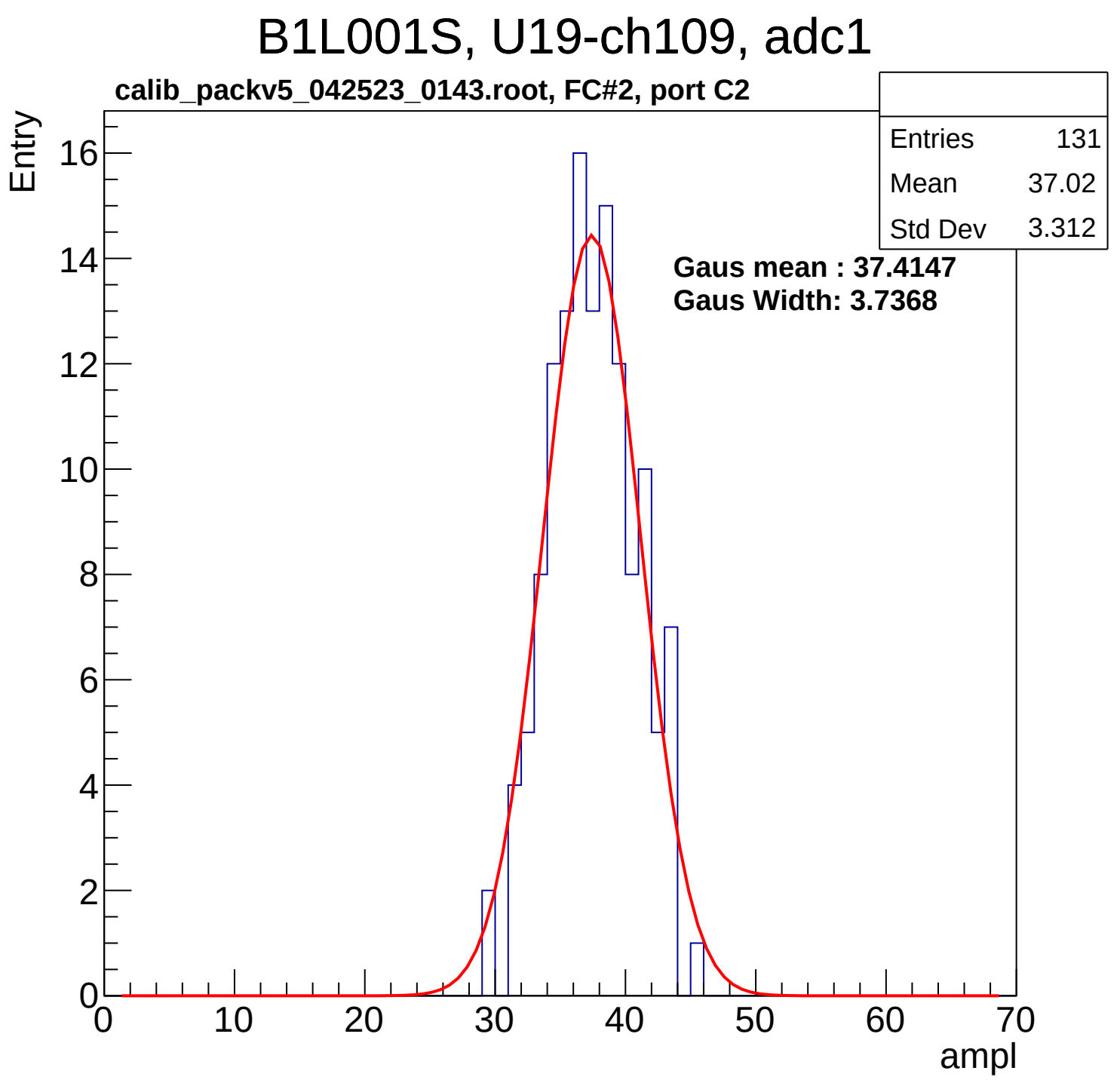
B1L001S, U19-ch109, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 131
Mean 37.02
Std Dev 3.312
Gaus mean : 37.4147
Gaus Width: 3.7368
Entry
ampl
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2
4
6
8
10
12
14
16
0
10
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40
50
60
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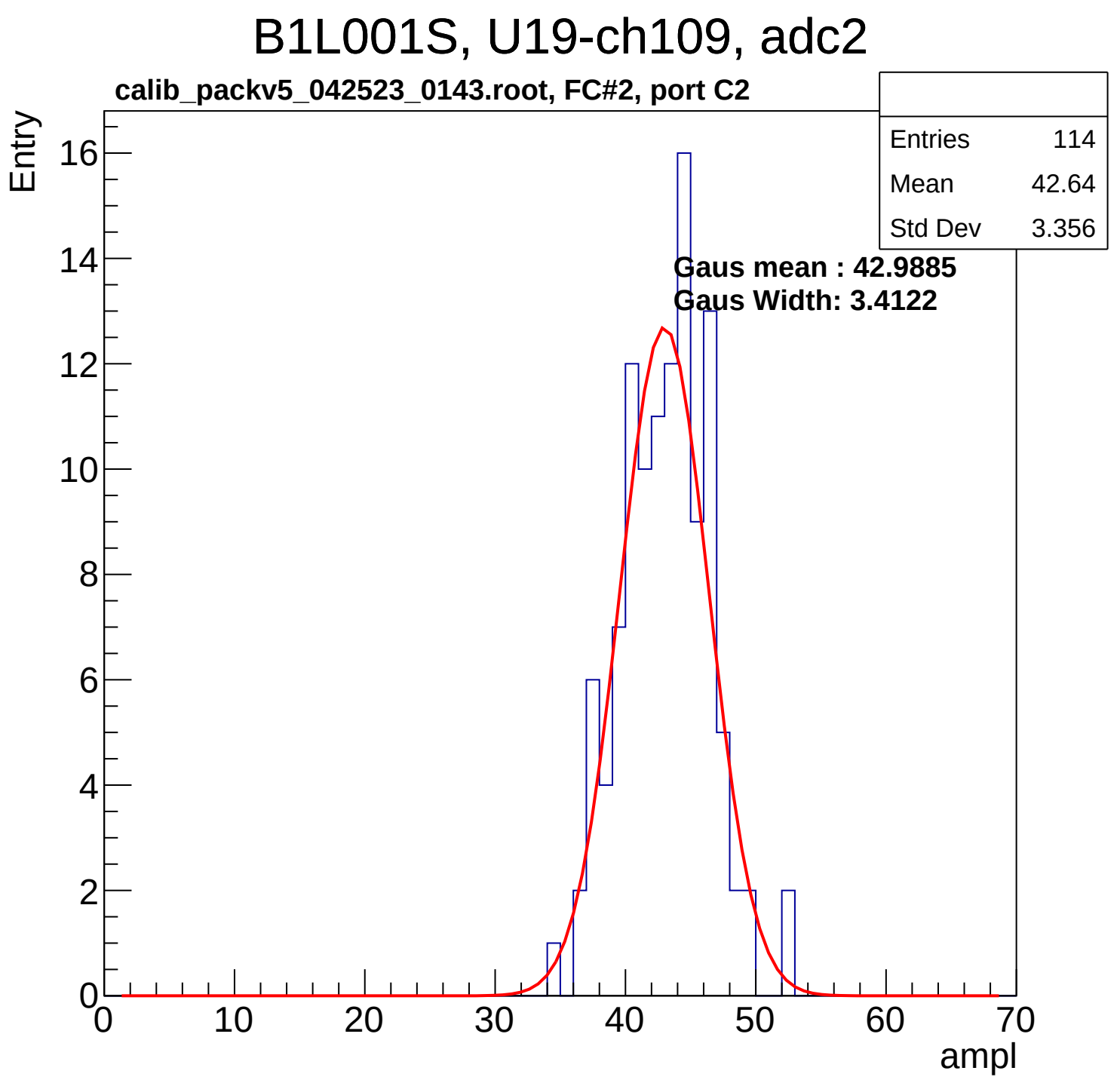
B1L001S, U19-ch109, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 114
Mean 42.64
Std Dev 3.356
Gaus mean : 42.9885
Gaus Width: 3.4122
Entry
ampl
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2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
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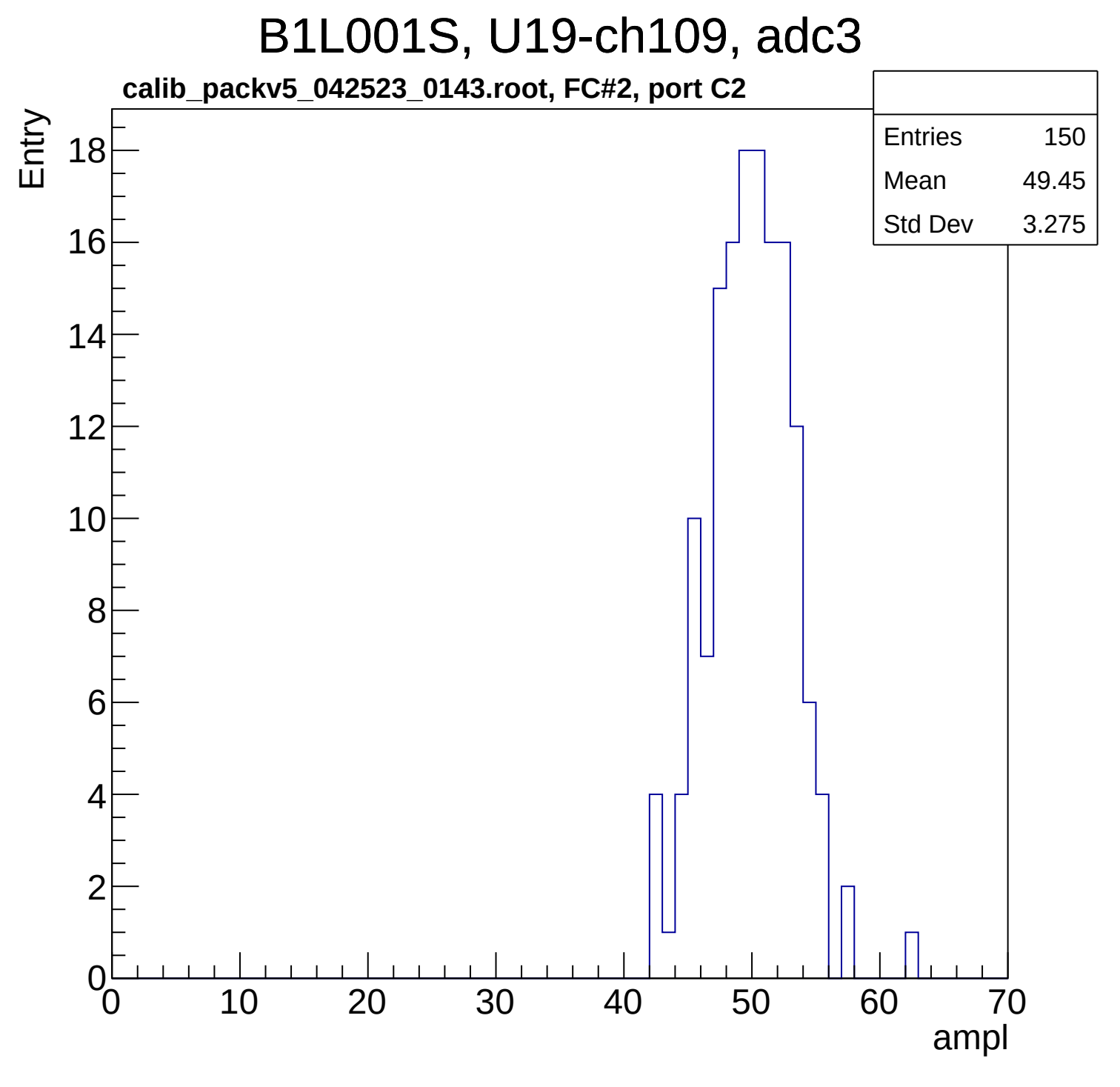
B1L001S, U19-ch109, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 150
Mean 49.45
Std Dev 3.275
Entry
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2
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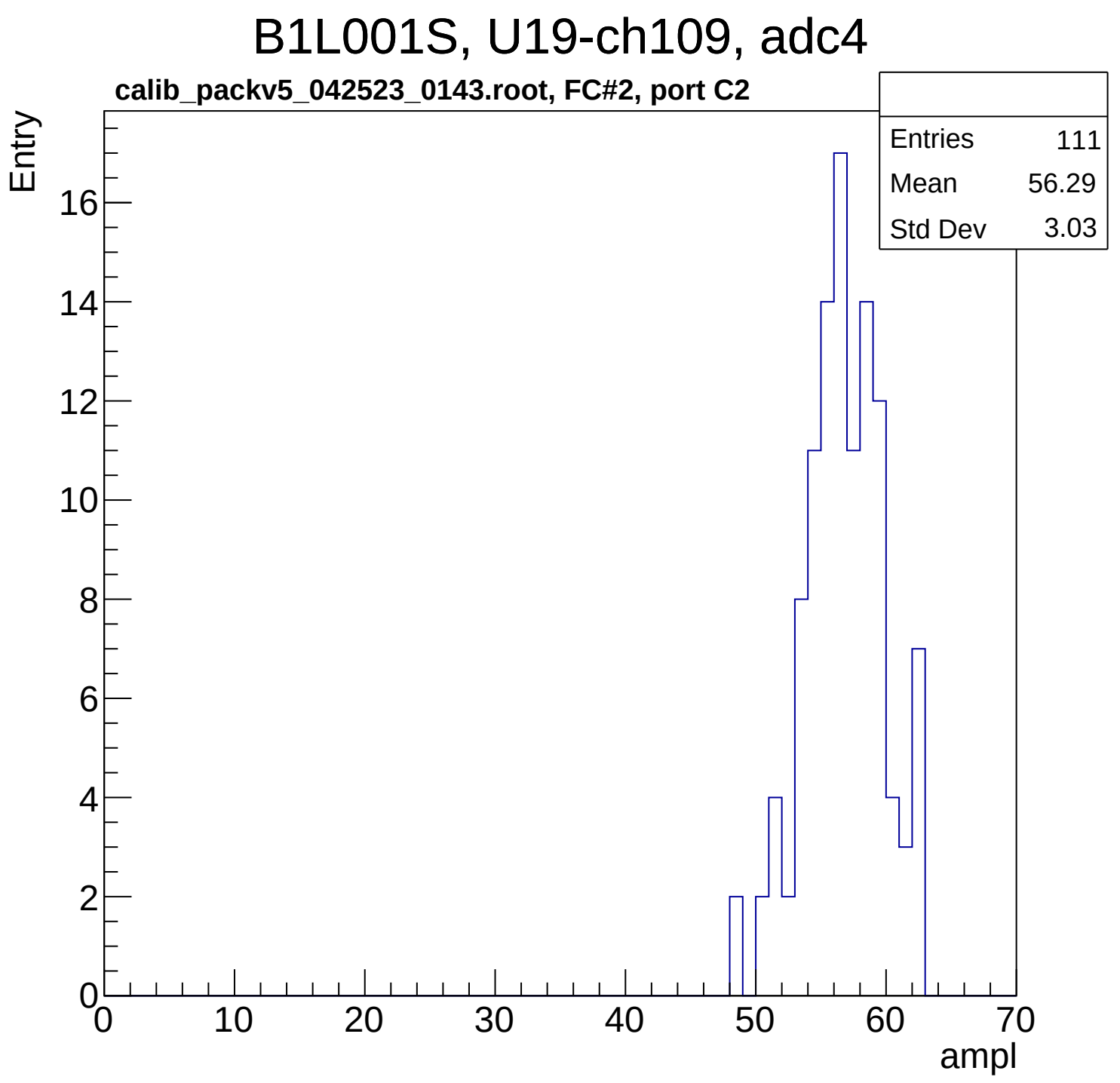
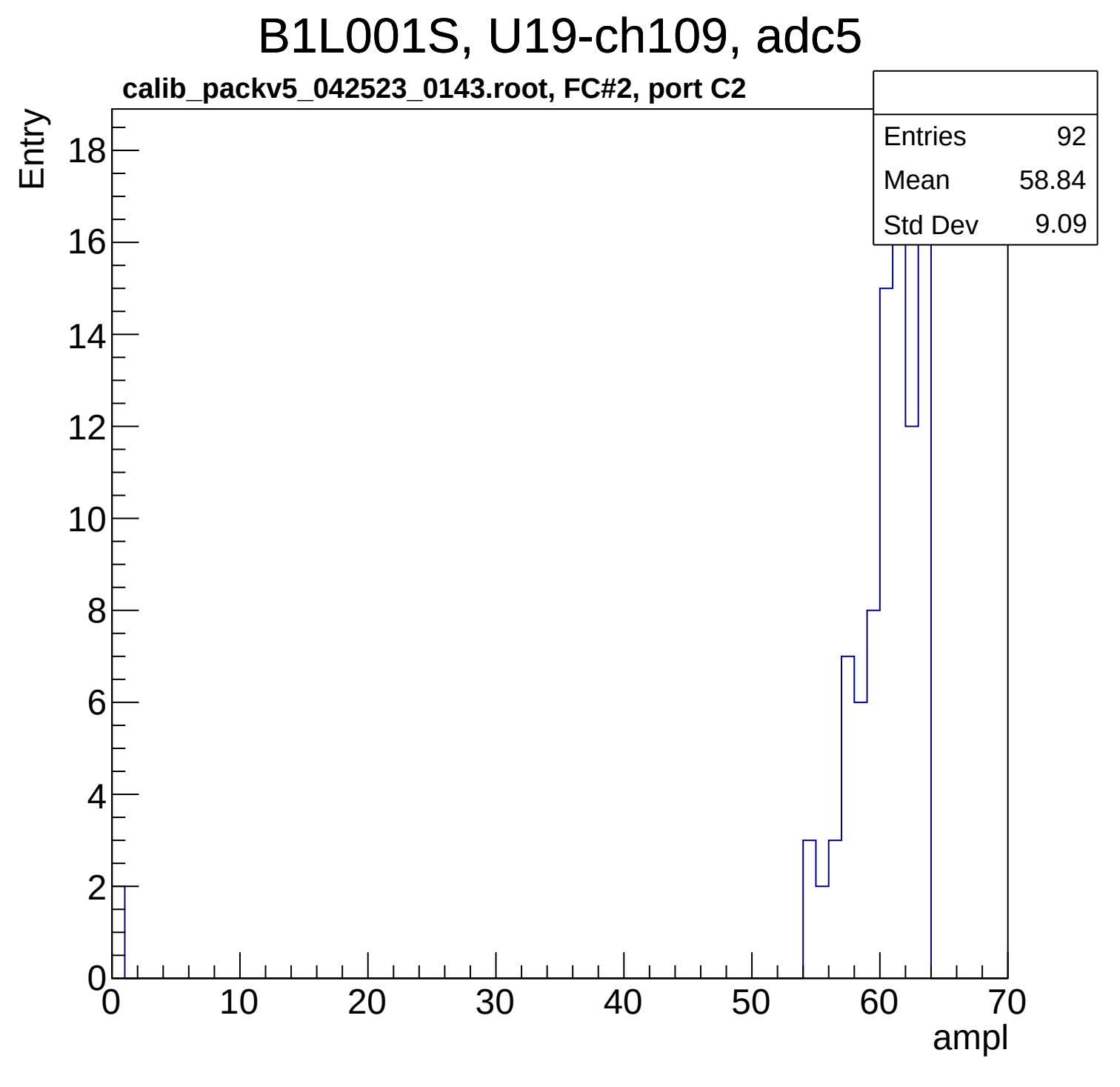
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch109, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 111
Mean 56.29
Std Dev 3.03
Entry
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch109, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 92
Mean 58.84
Std Dev 9.09
Entry
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6
8
10
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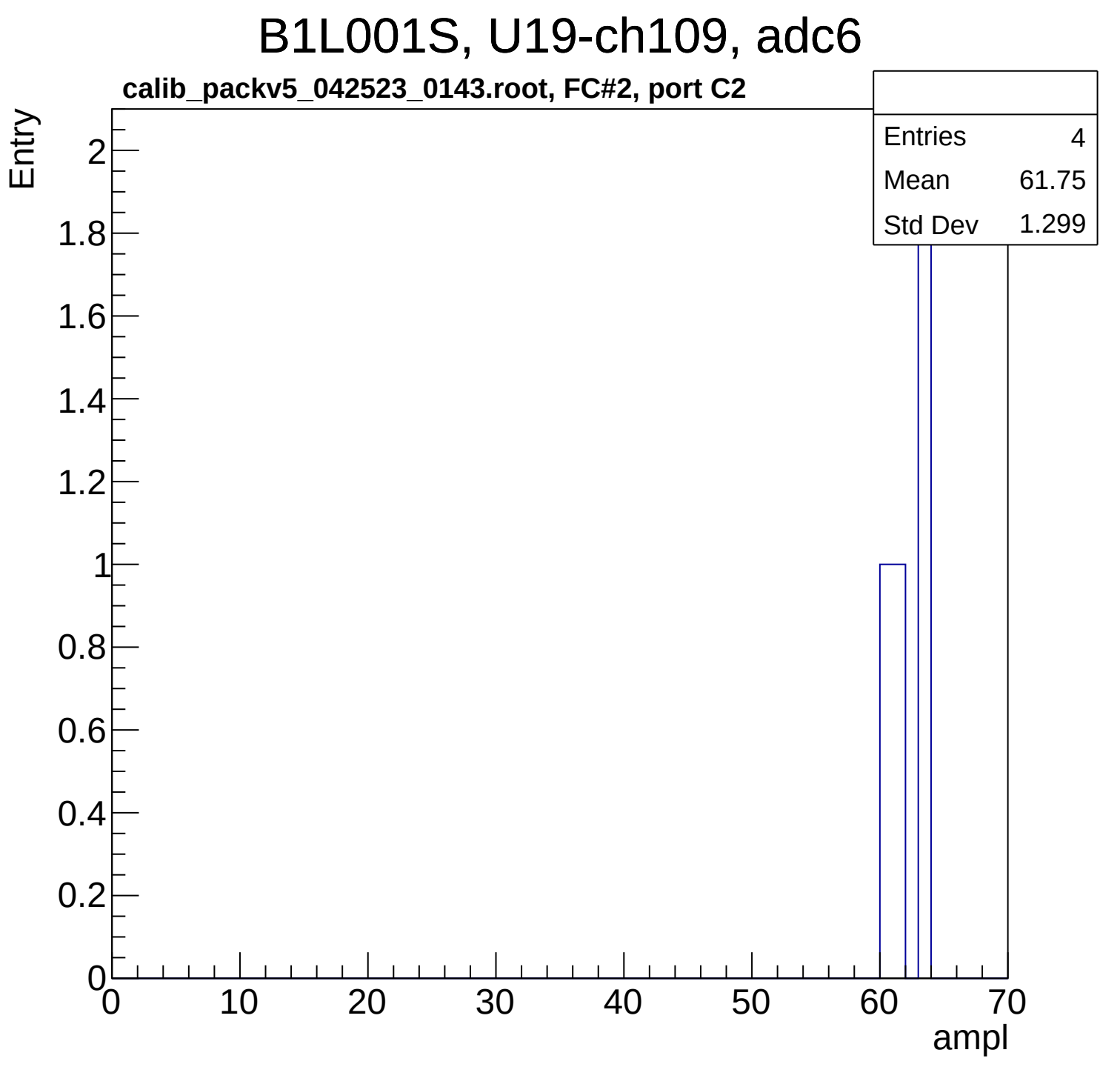
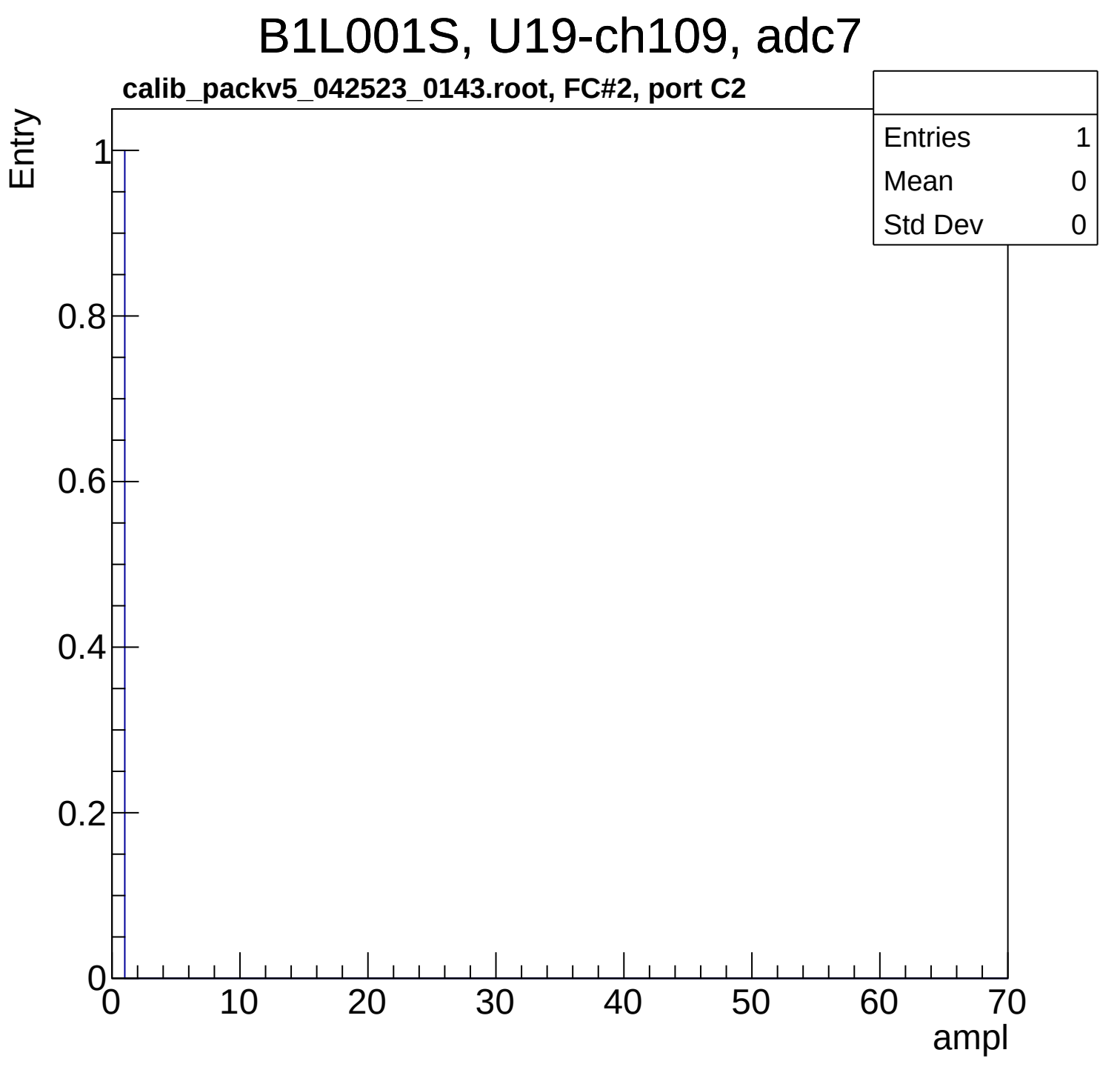
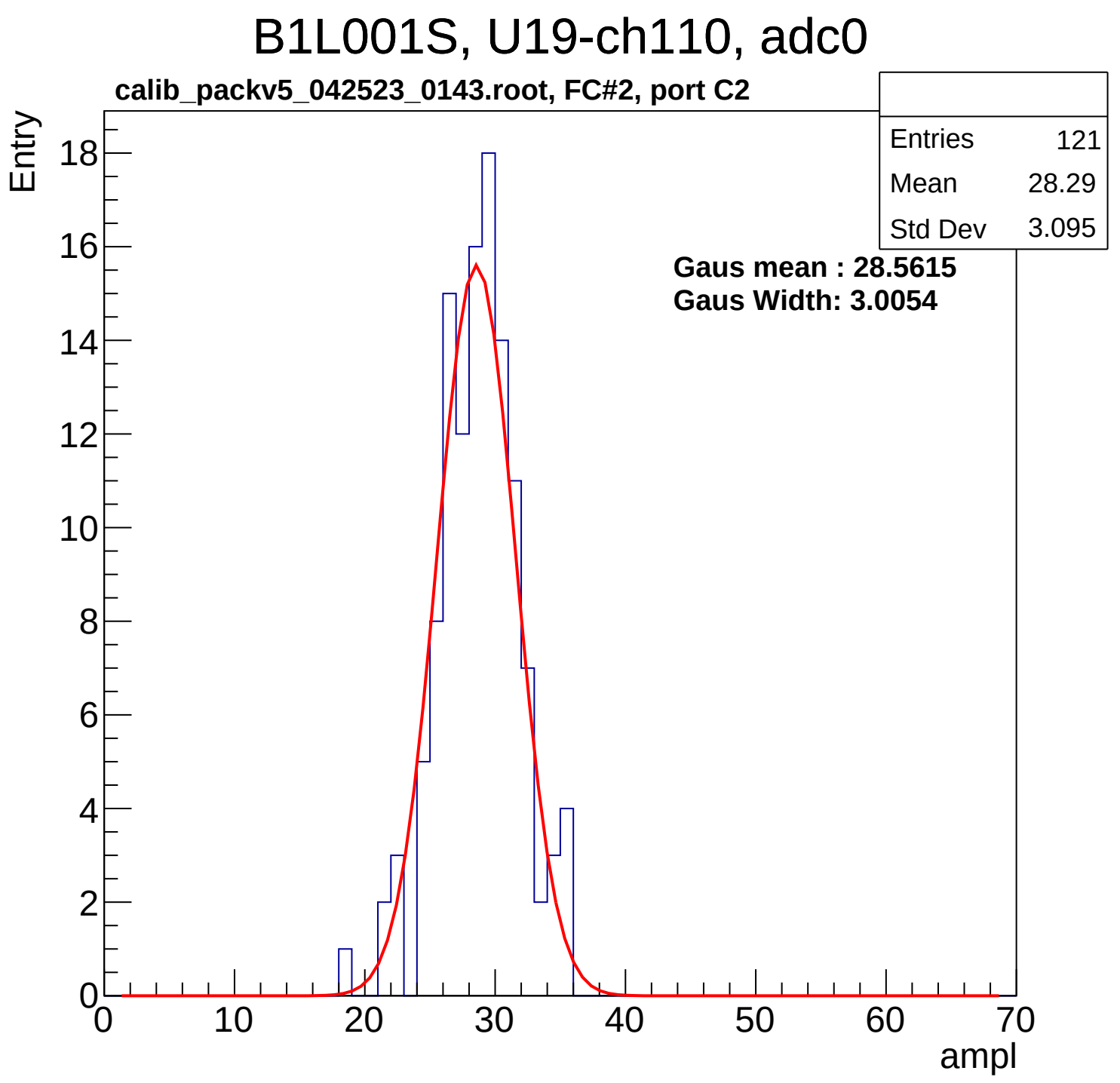
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch109, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 4
Mean 61.75
Std Dev 1.299
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L001S, U19-ch109, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch110, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 121
Mean 28.29
Std Dev 3.095
Gaus mean : 28.5615
Gaus Width: 3.0054
Entry
ampl
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4
6
8
10
12
14
16
18
0
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40
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60
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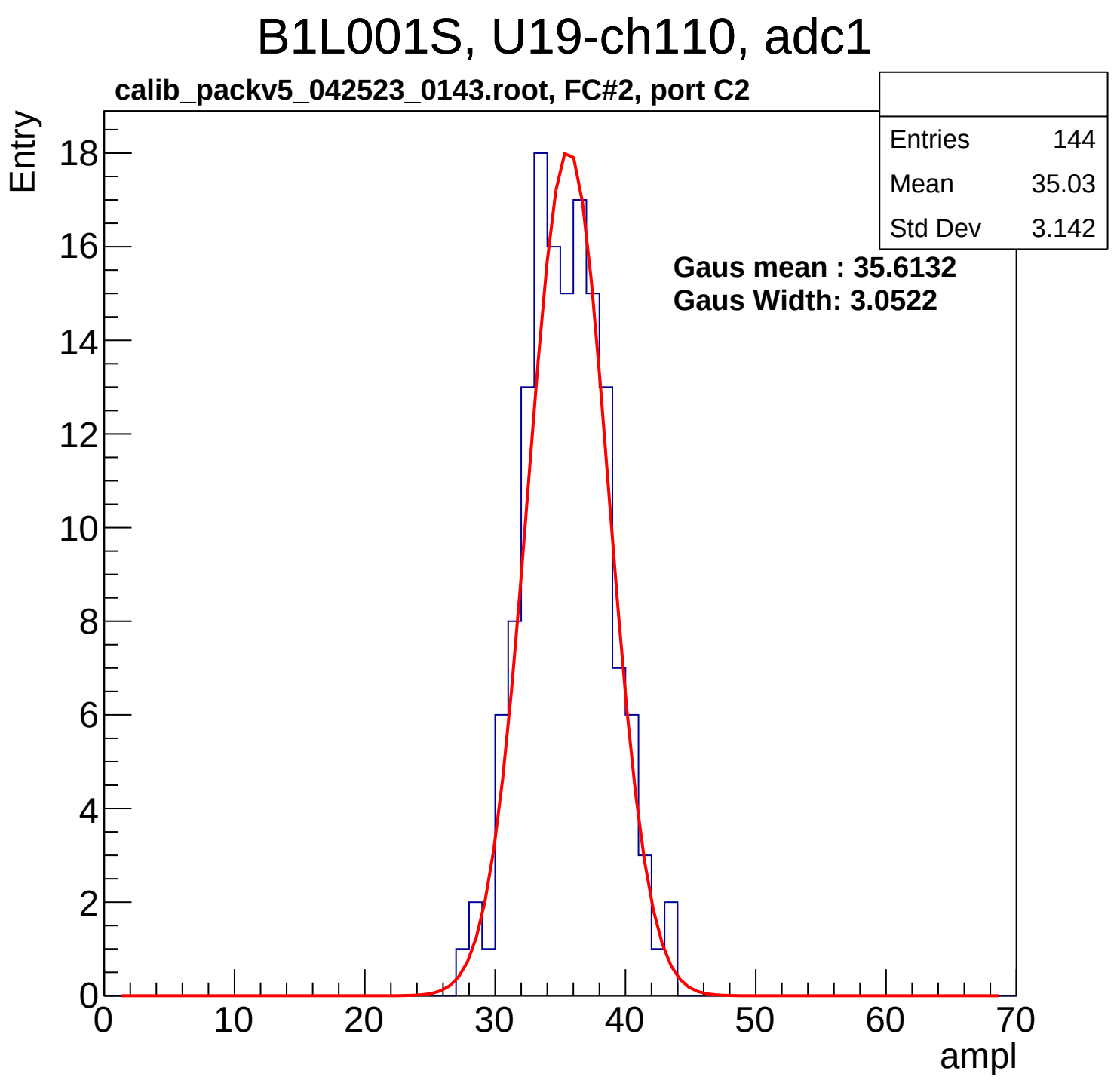
B1L001S, U19-ch110, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 144
Mean 35.03
Std Dev 3.142
Gaus mean : 35.6132
Gaus Width: 3.0522
Entry
ampl
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4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
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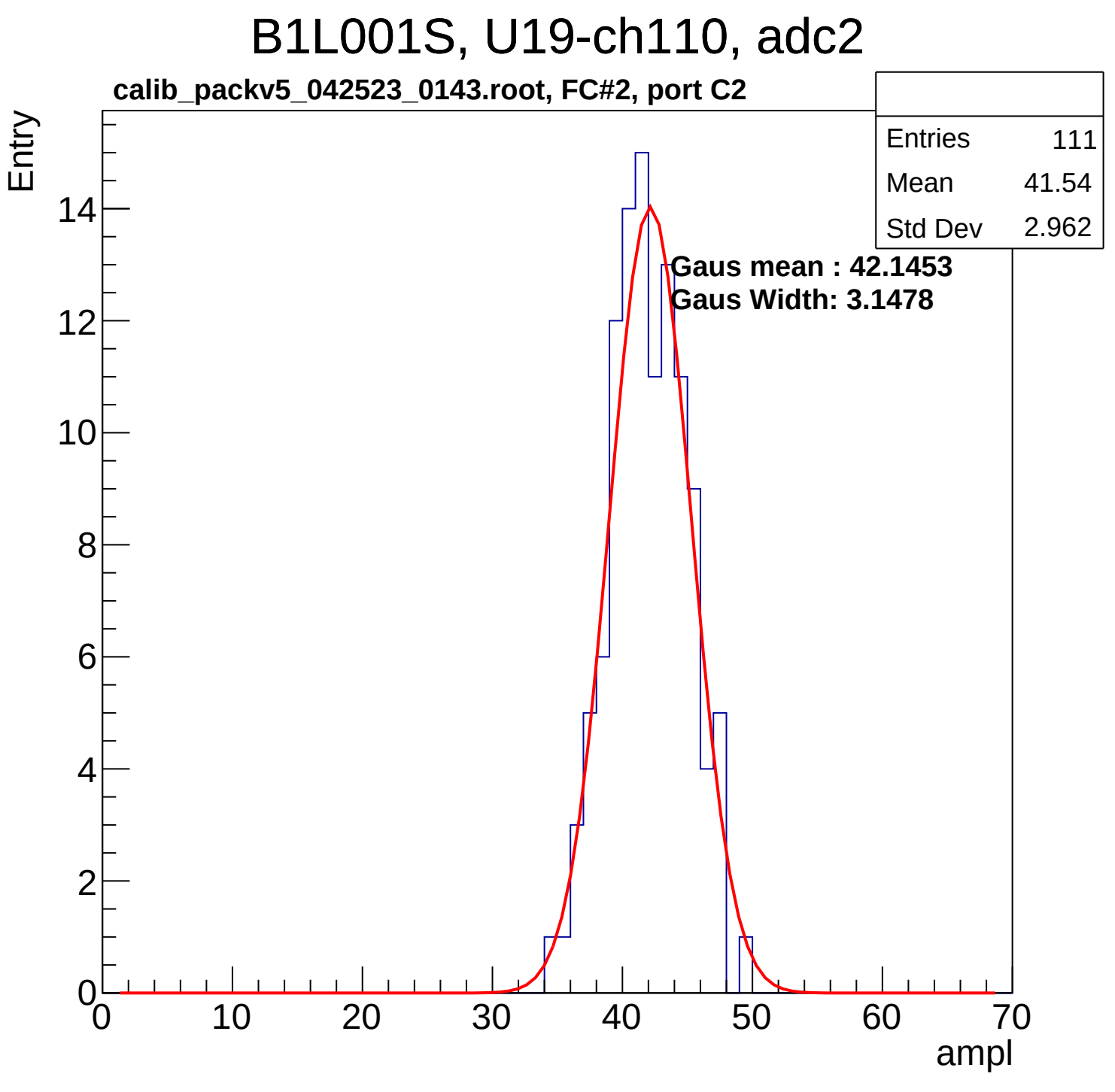
B1L001S, U19-ch110, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 111
Mean 41.54
Std Dev 2.962
Gaus mean : 42.1453
Gaus Width: 3.1478
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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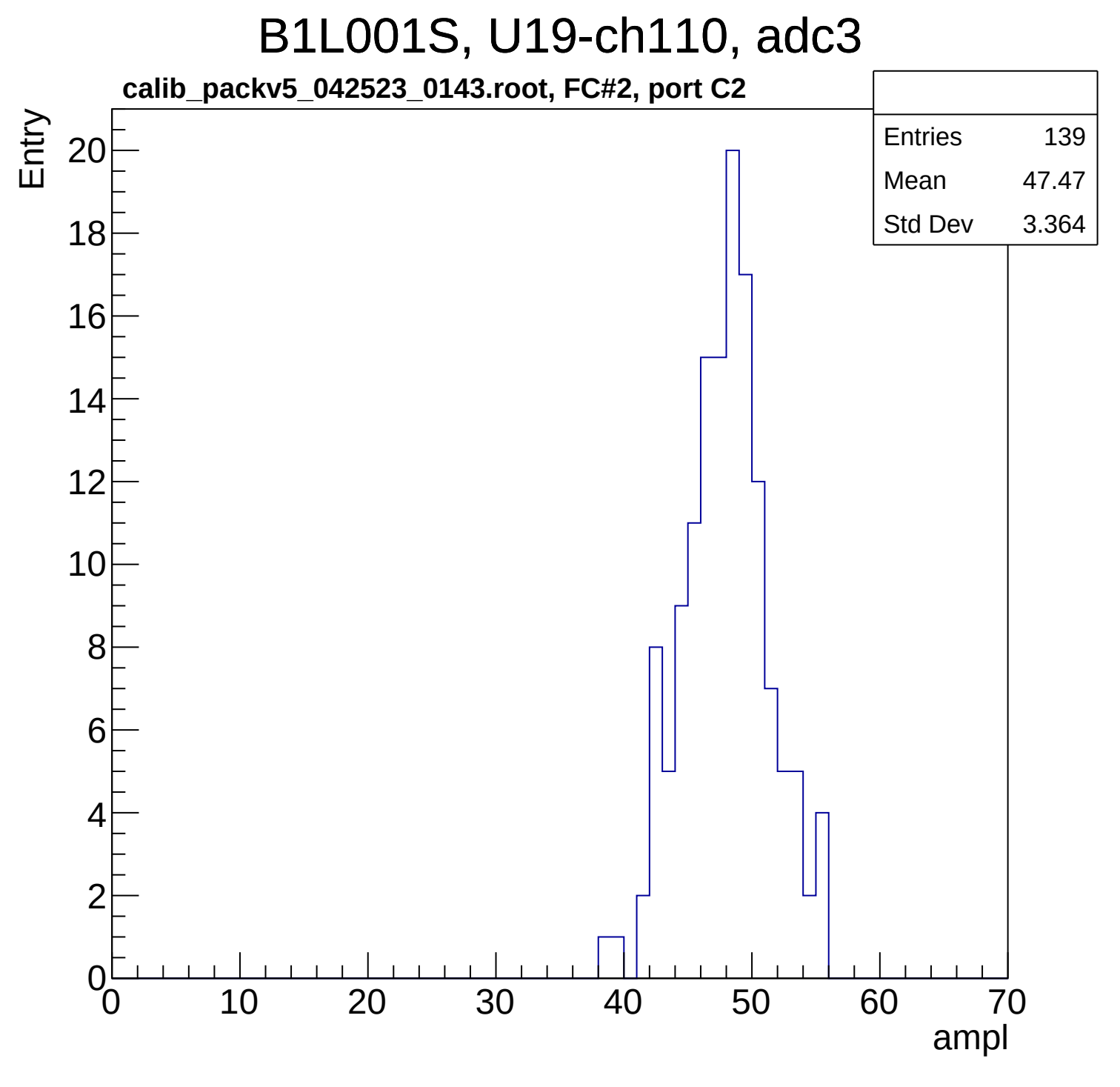
B1L001S, U19-ch110, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 139
Mean 47.47
Std Dev 3.364
Entry
ampl
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6
8
10
12
14
16
18
20
0
10
20
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50
60
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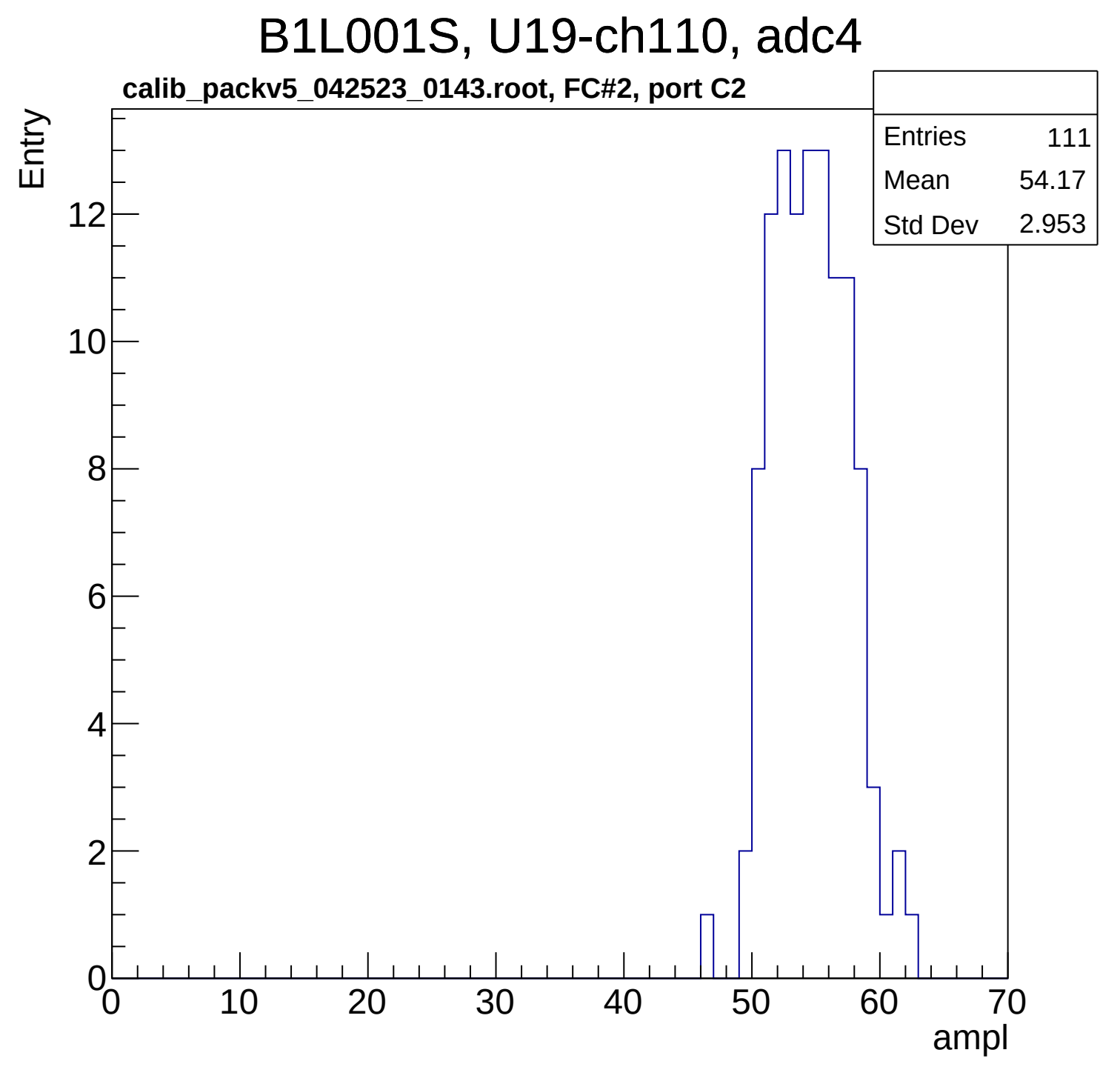
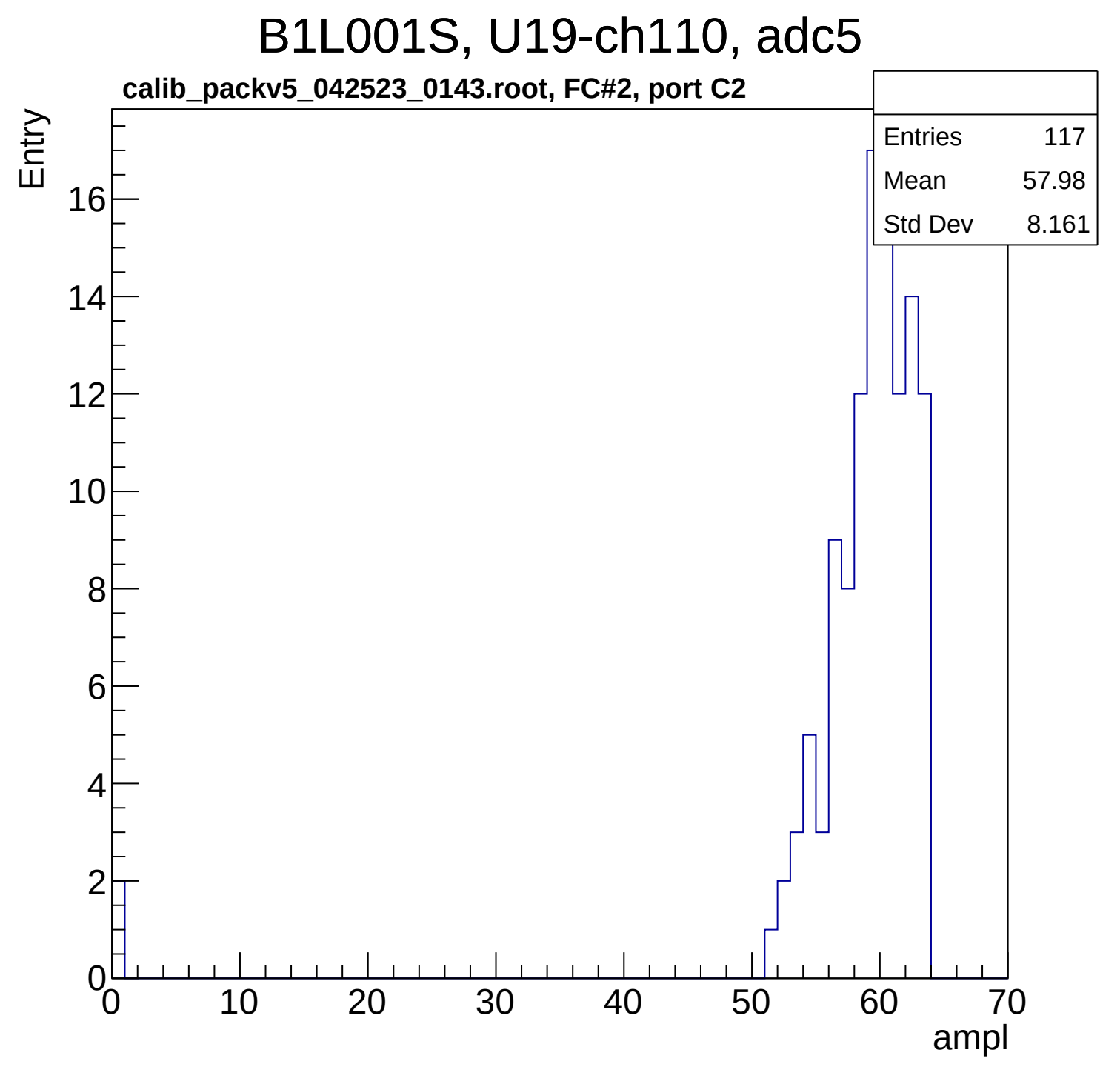

B1L001S, U19-ch110, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 111
Mean 54.17
Std Dev 2.953
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch110, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 117
Mean 57.98
Std Dev 8.161
Entry
ampl
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2
4
6
8
10
12
14
16
0
10
20
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40
50
60
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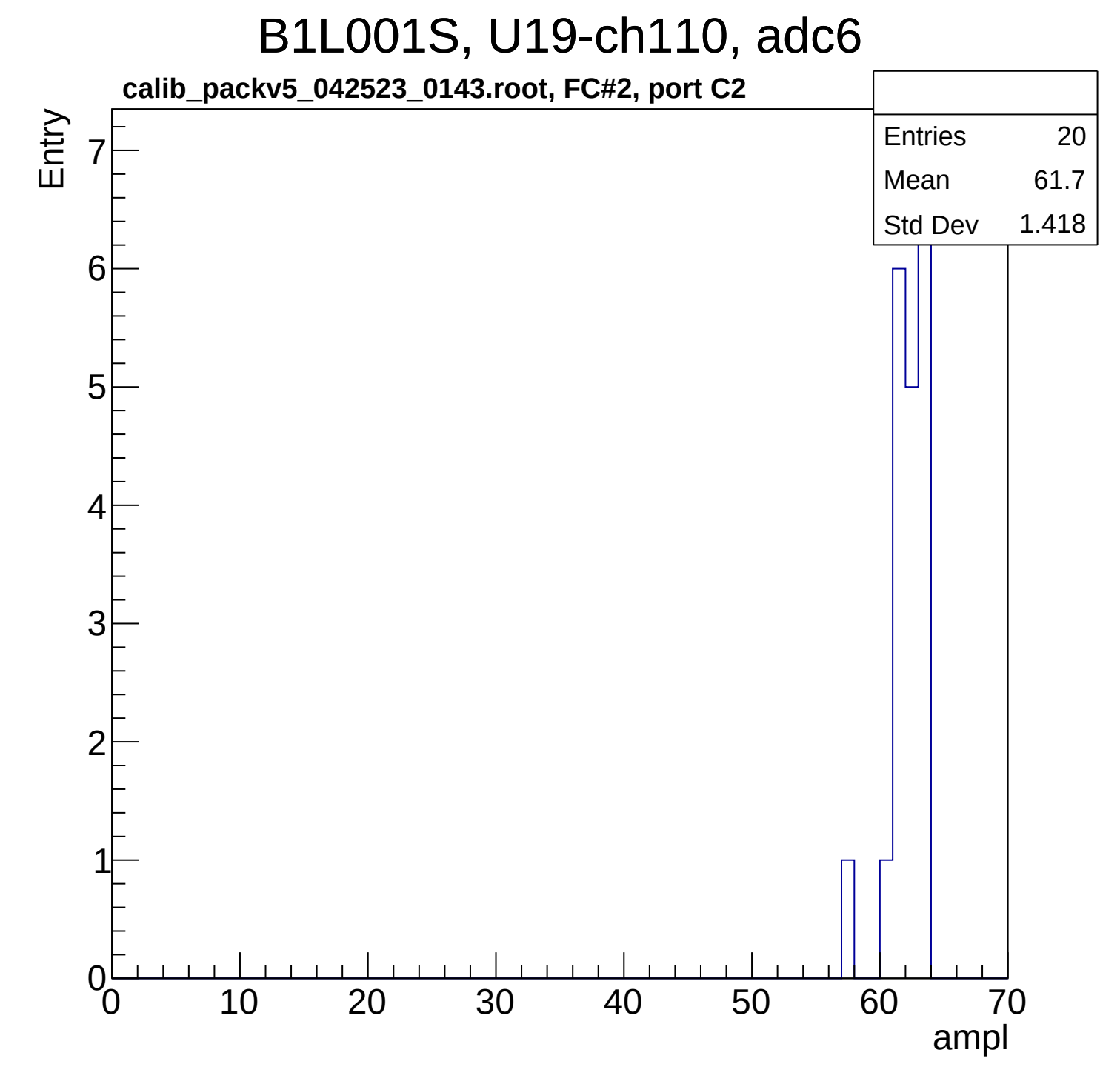
B1L001S, U19-ch110, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 20
Mean 61.7
Std Dev 1.418
Entry
ampl
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1
2
3
4
5
6
7
0
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40
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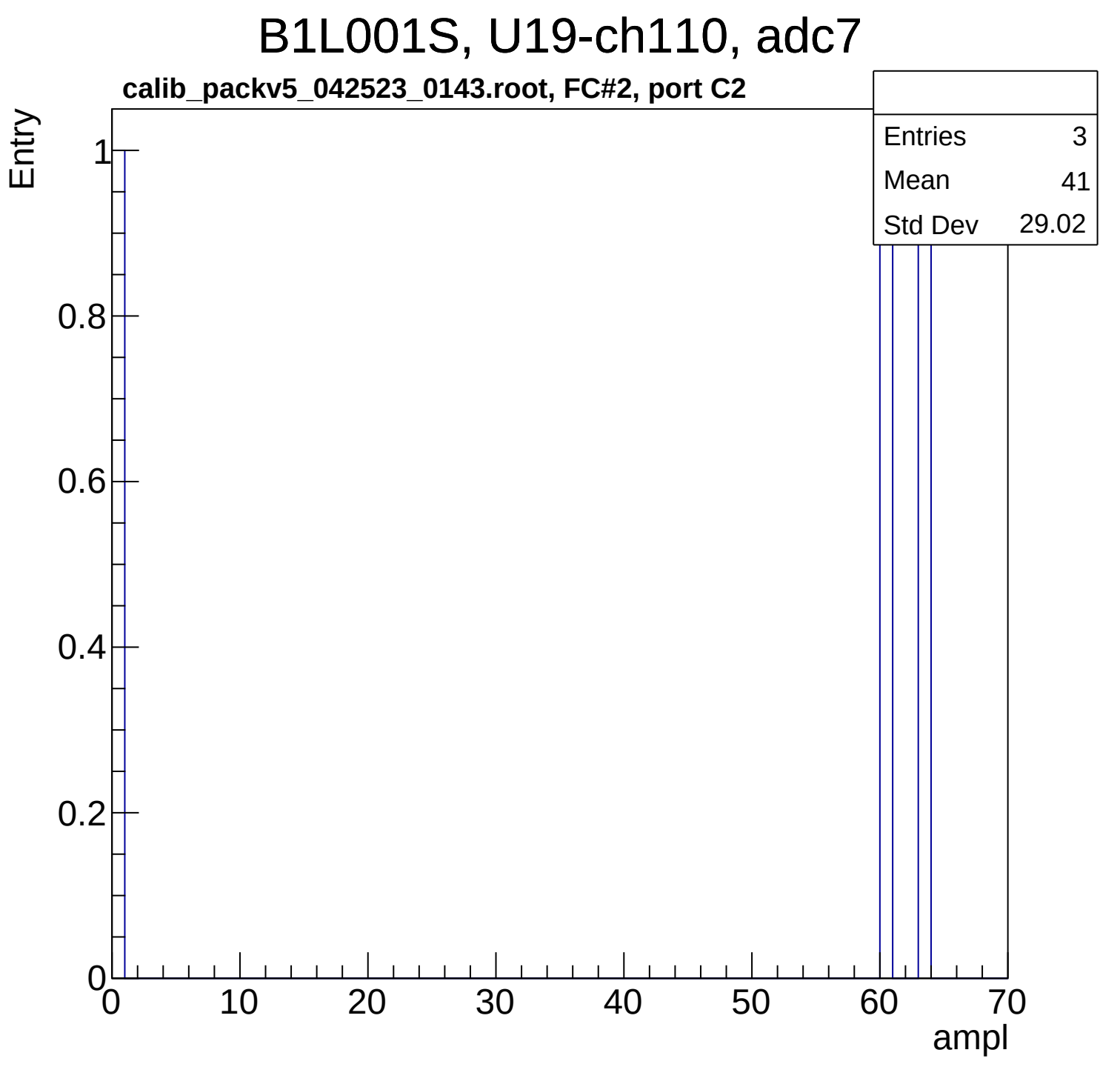
B1L001S, U19-ch110, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 3
Mean 41
Std Dev 29.02
Entry
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0.6
0.4
0.2
0
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20
30
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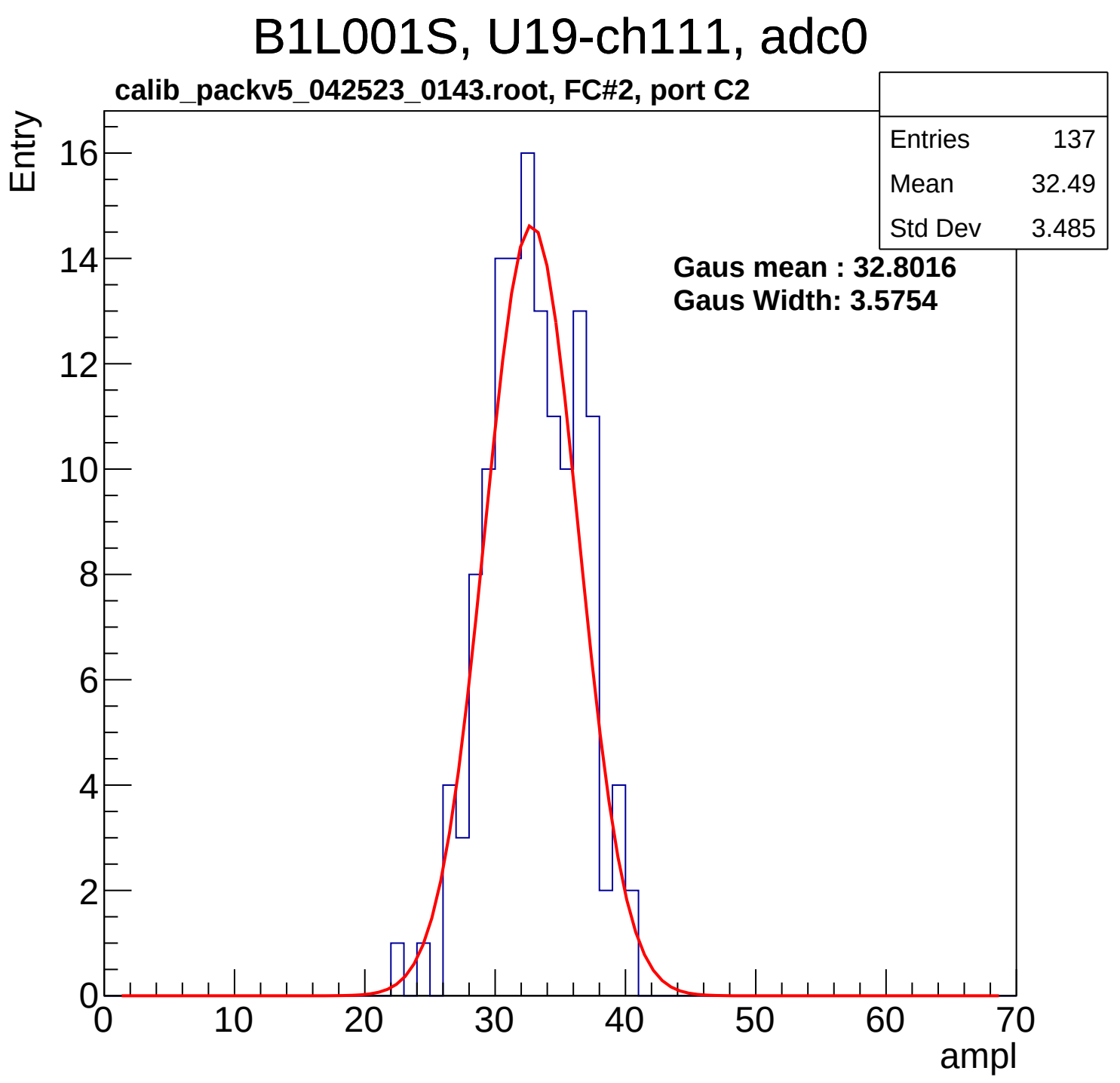
50
60
70
ampl


B1L001S, U19-ch111, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 137
Mean 32.49
Std Dev 3.485
Gaus mean : 32.8016
Gaus Width: 3.5754
Entry
ampl
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2
4
6
8
10
12
14
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0
10
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40
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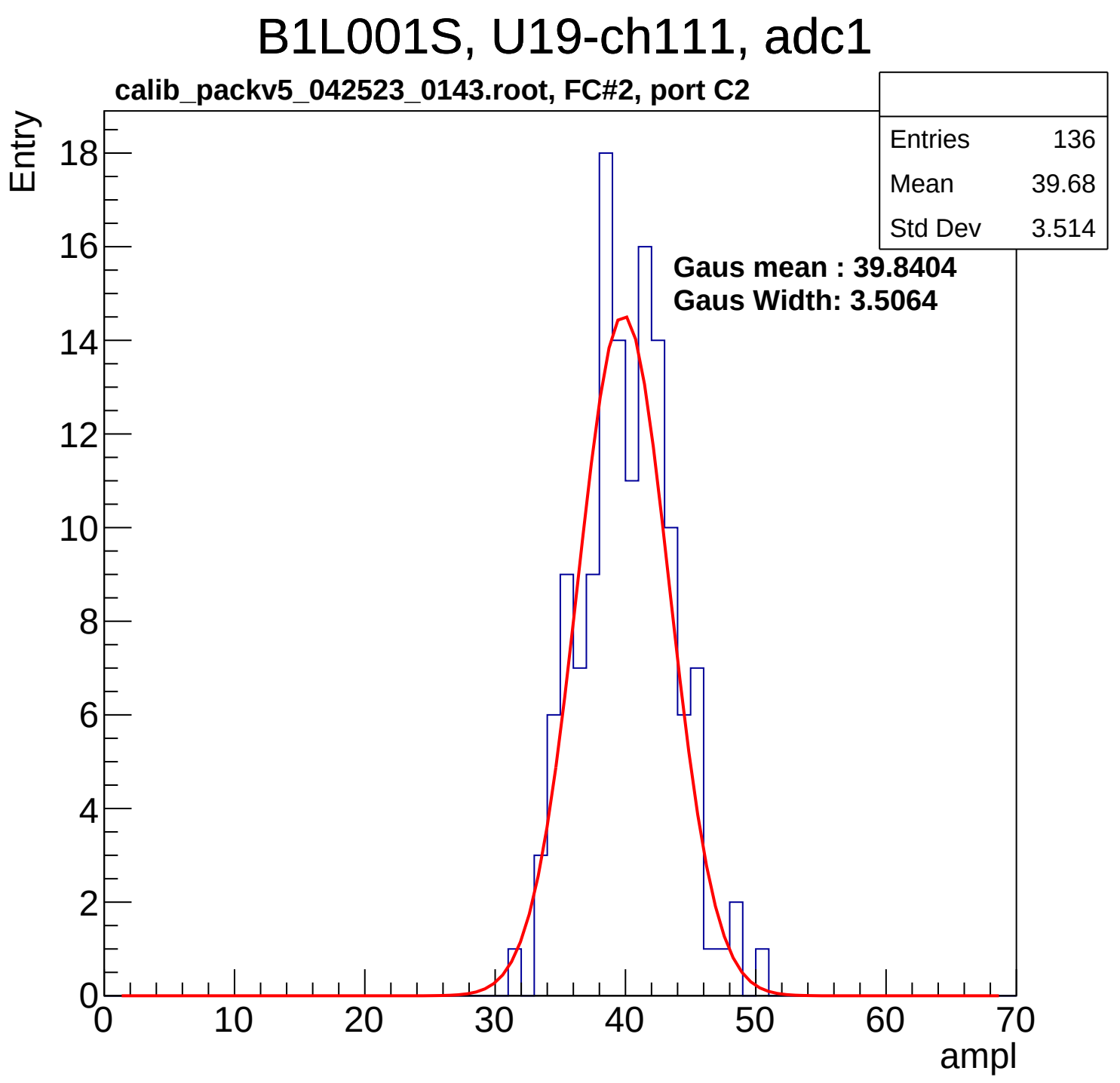
60
70


B1L001S, U19-ch111, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 136
Mean 39.68
Std Dev 3.514
Gaus mean : 39.8404
Gaus Width: 3.5064
Entry
ampl
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2
4
6
8
10
12
14
16
18
0
10
20
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40
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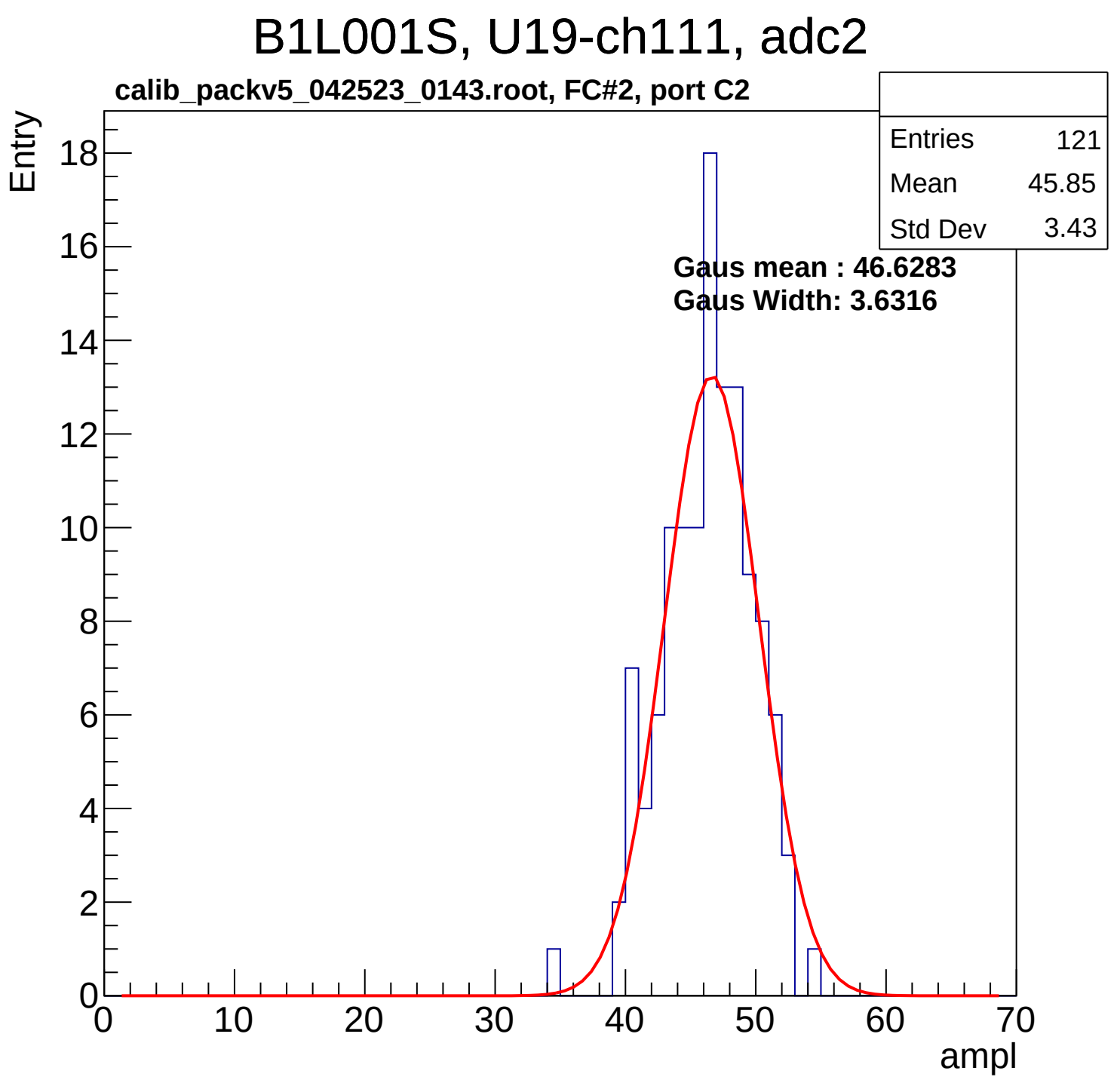
60
70


B1L001S, U19-ch111, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 121
Mean 45.85
Std Dev 3.43
Gaus mean : 46.6283
Gaus Width: 3.6316
Entry
ampl
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4
6
8
10
12
14
16
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0
10
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60
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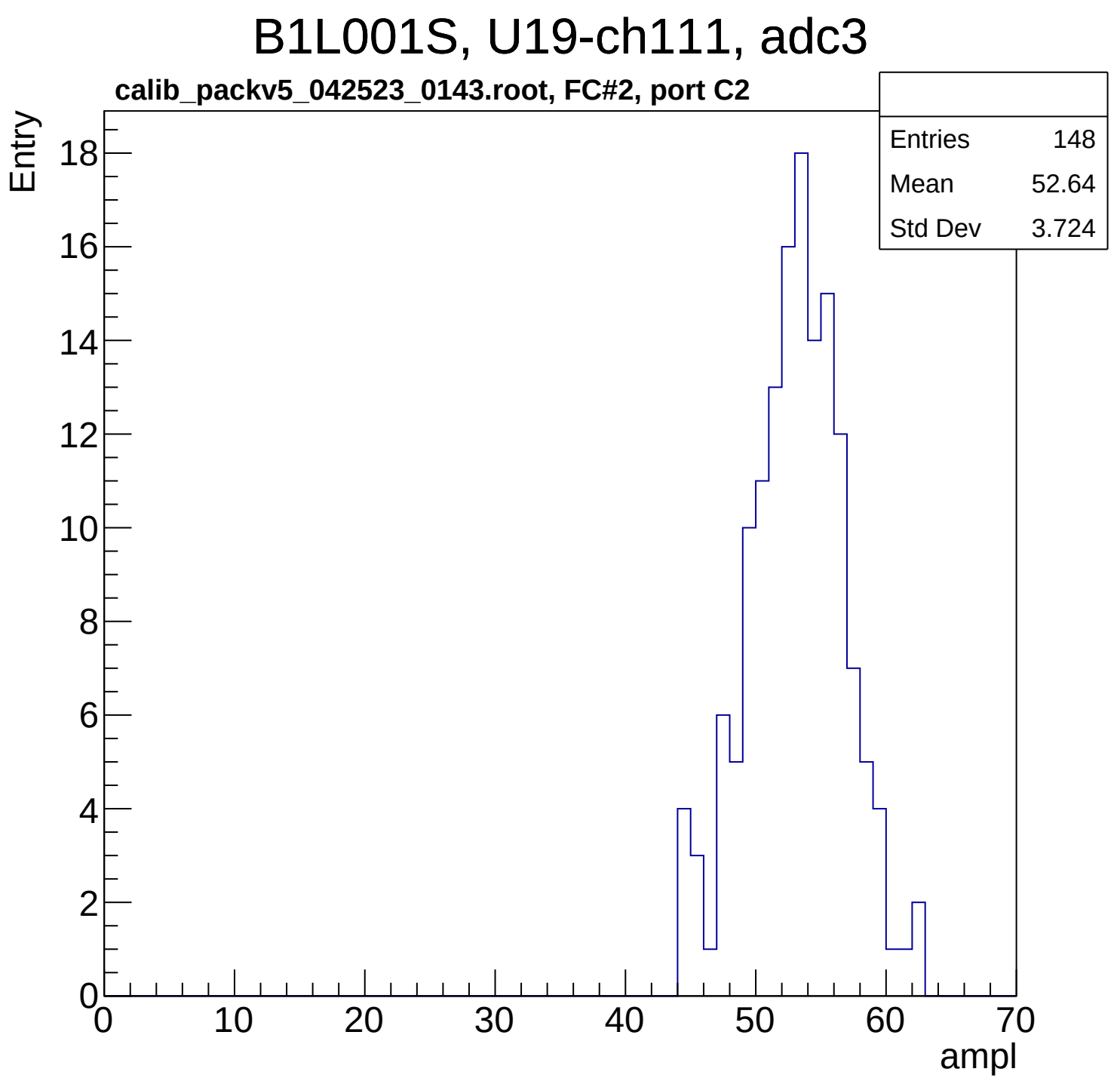
B1L001S, U19-ch111, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 148
Mean 52.64
Std Dev 3.724
Entry
ampl
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4
6
8
10
12
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16
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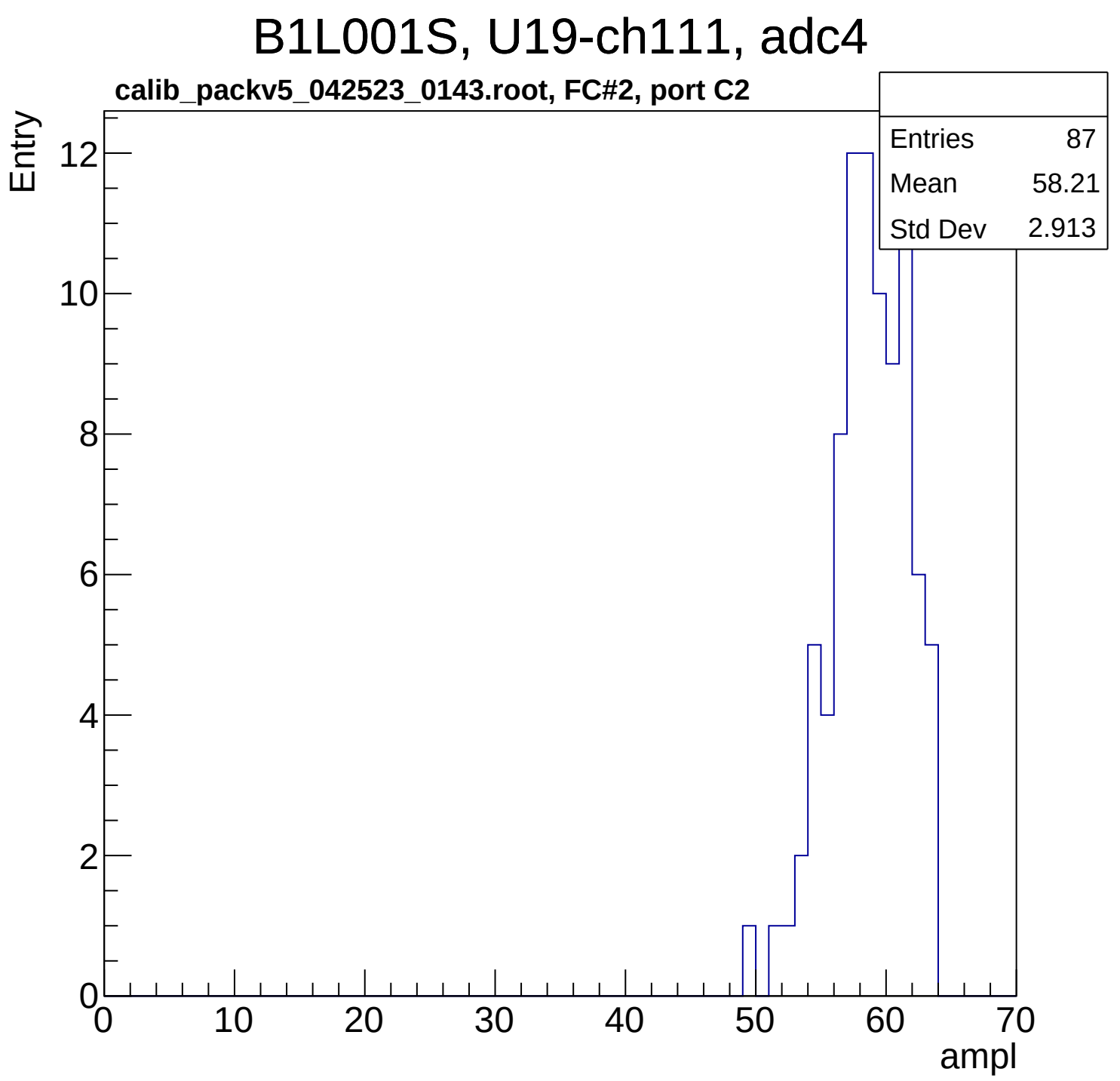
B1L001S, U19-ch111, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 87
Mean 58.21
Std Dev 2.913
Entry
ampl
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2
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0
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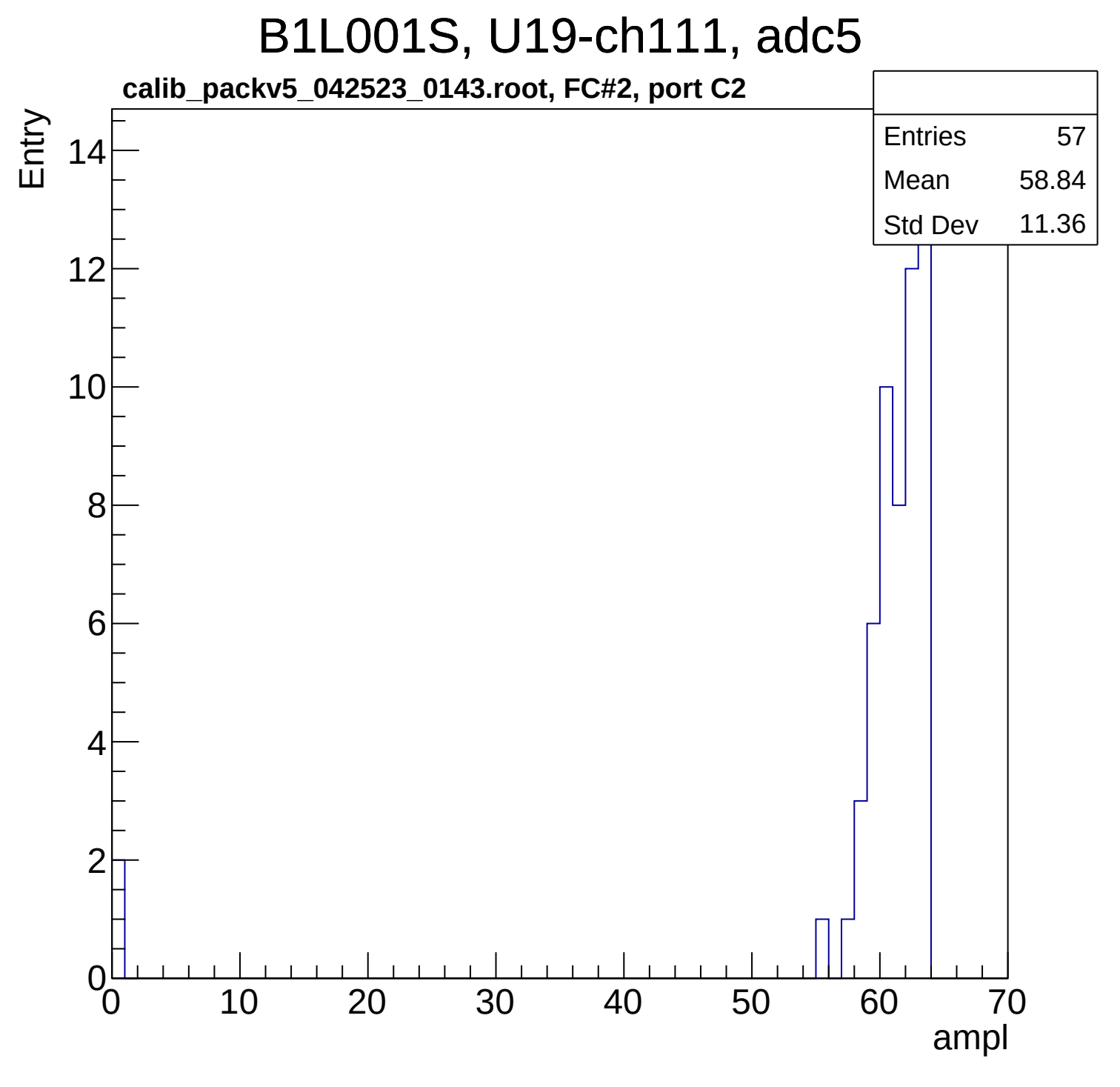
B1L001S, U19-ch111, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 57
Mean 58.84
Std Dev 11.36
Entry
ampl
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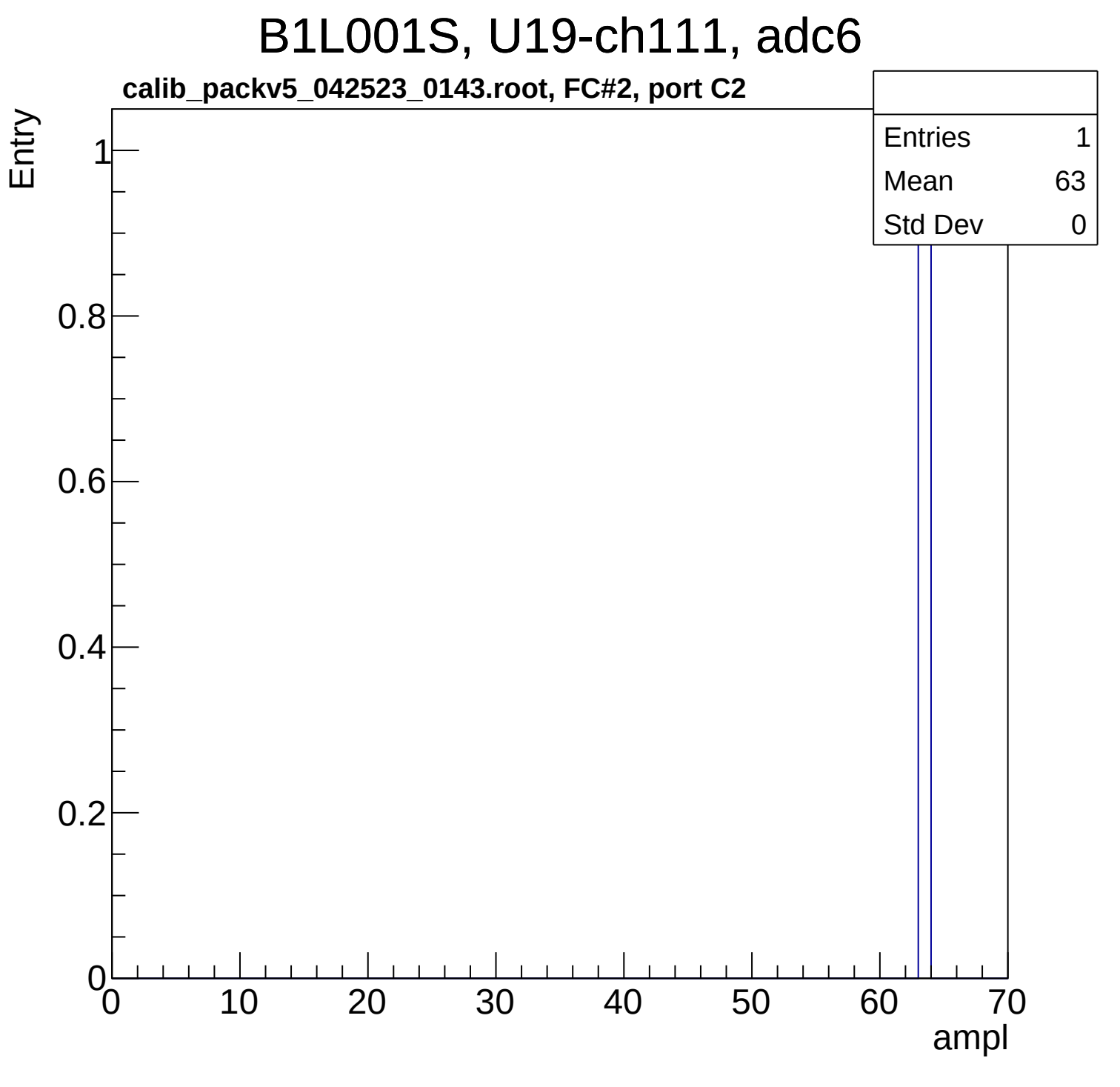
B1L001S, U19-ch111, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 63
Std Dev 0
Entry
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0.6
0.4
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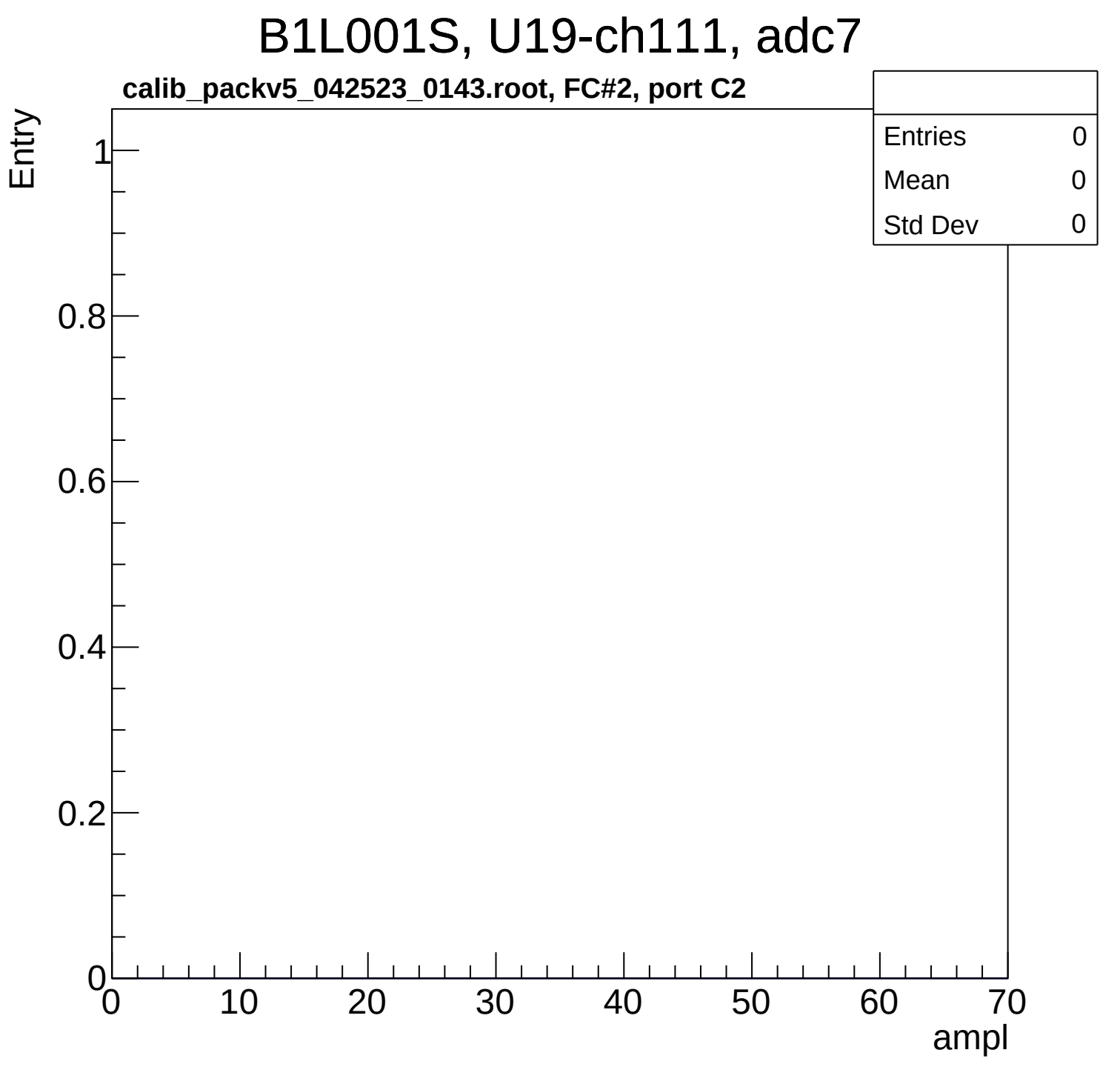
0
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch111, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 0
Mean 0
Std Dev 0
Entry
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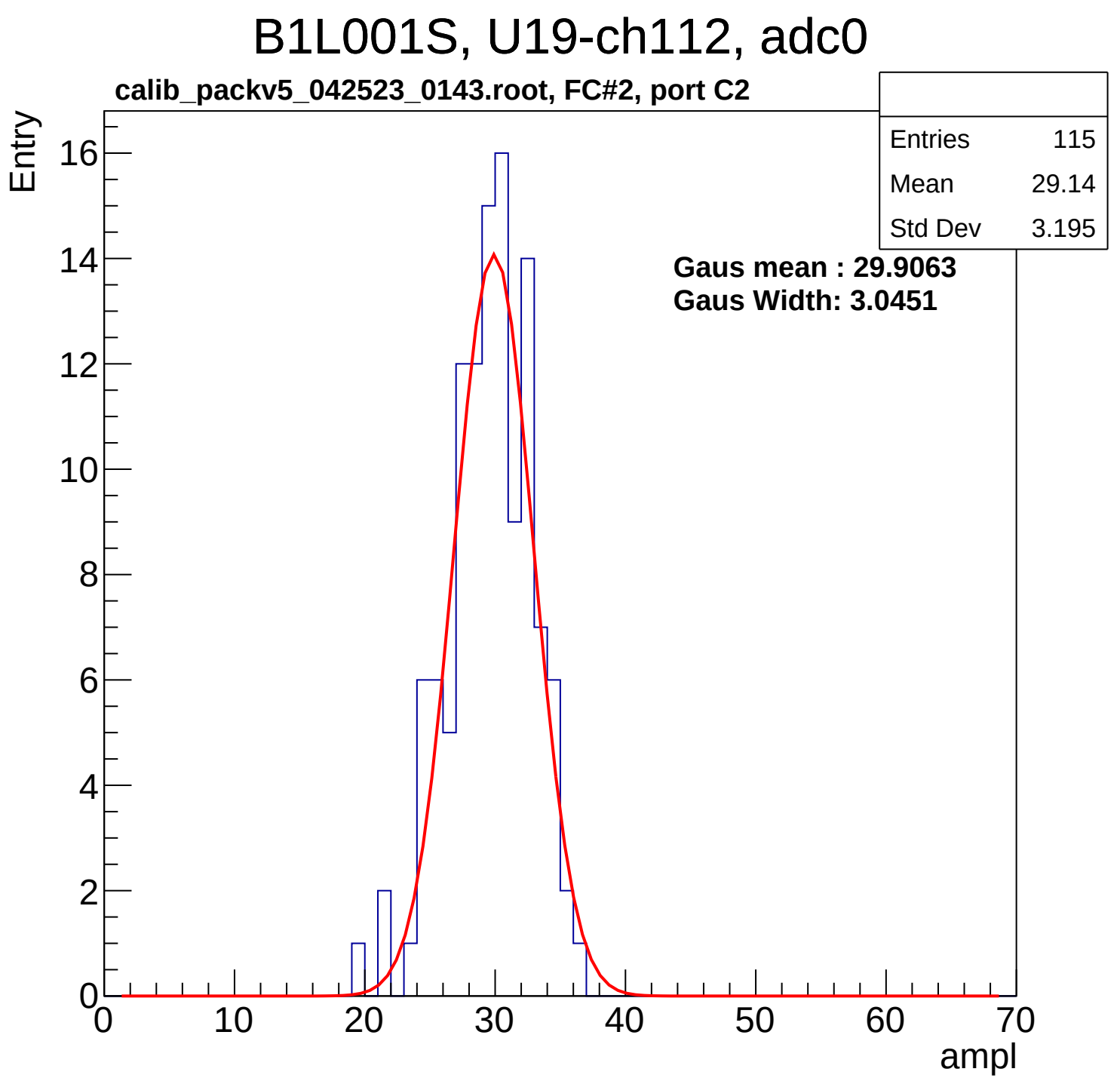
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch112, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 115
Mean 29.14
Std Dev 3.195
Gaus mean : 29.9063
Gaus Width: 3.0451
Entry
ampl
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2
4
6
8
10
12
14
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0
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20
30
40
50
60
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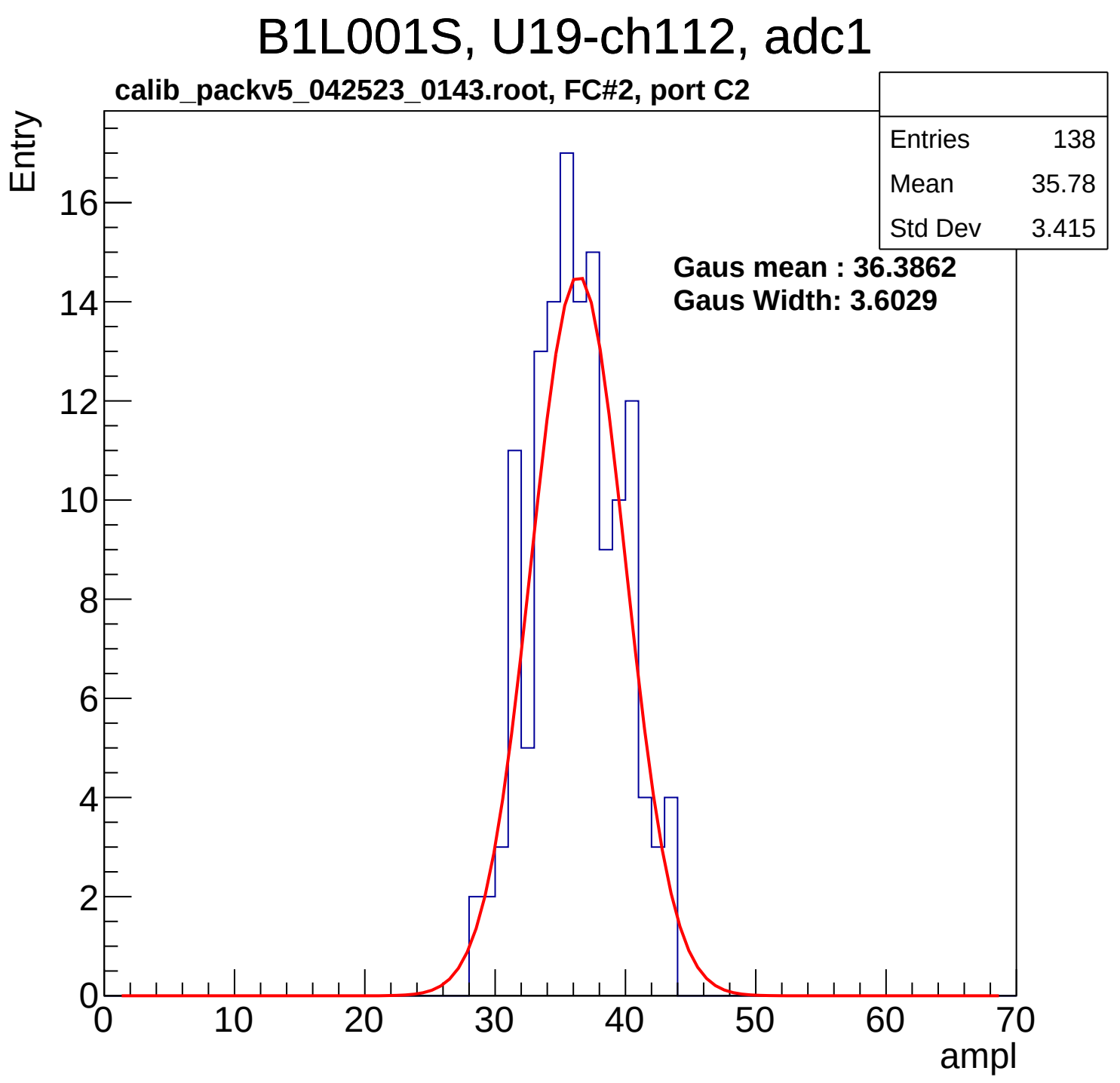
B1L001S, U19-ch112, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 138
Mean 35.78
Std Dev 3.415
Gaus mean : 36.3862
Gaus Width: 3.6029
Entry
ampl
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2
4
6
8
10
12
14
16
0
10
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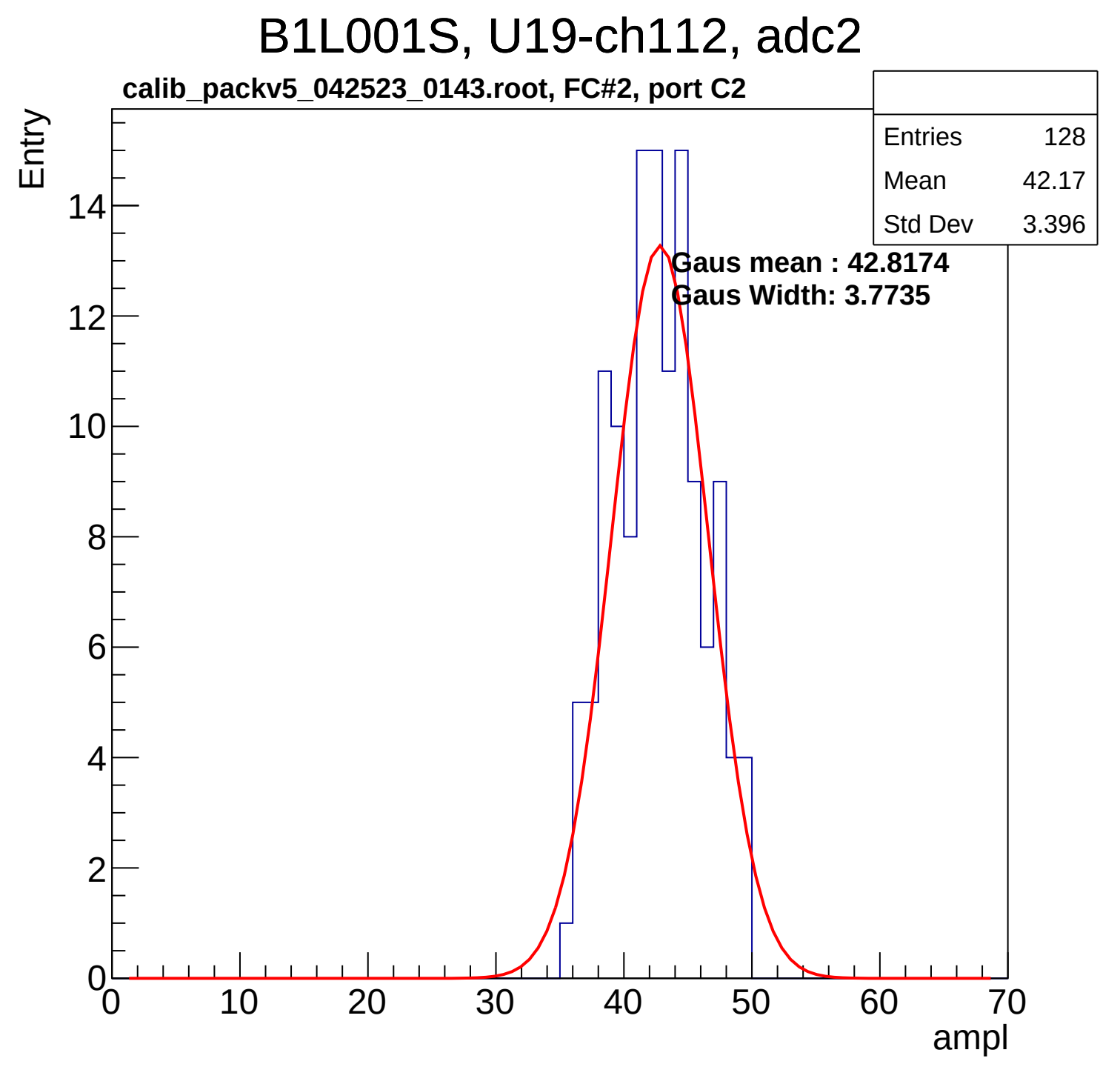
B1L001S, U19-ch112, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 128
Mean 42.17
Std Dev 3.396
Gaus mean : 42.8174
Gaus Width: 3.7735
Entry
ampl
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2
4
6
8
10
12
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0
10
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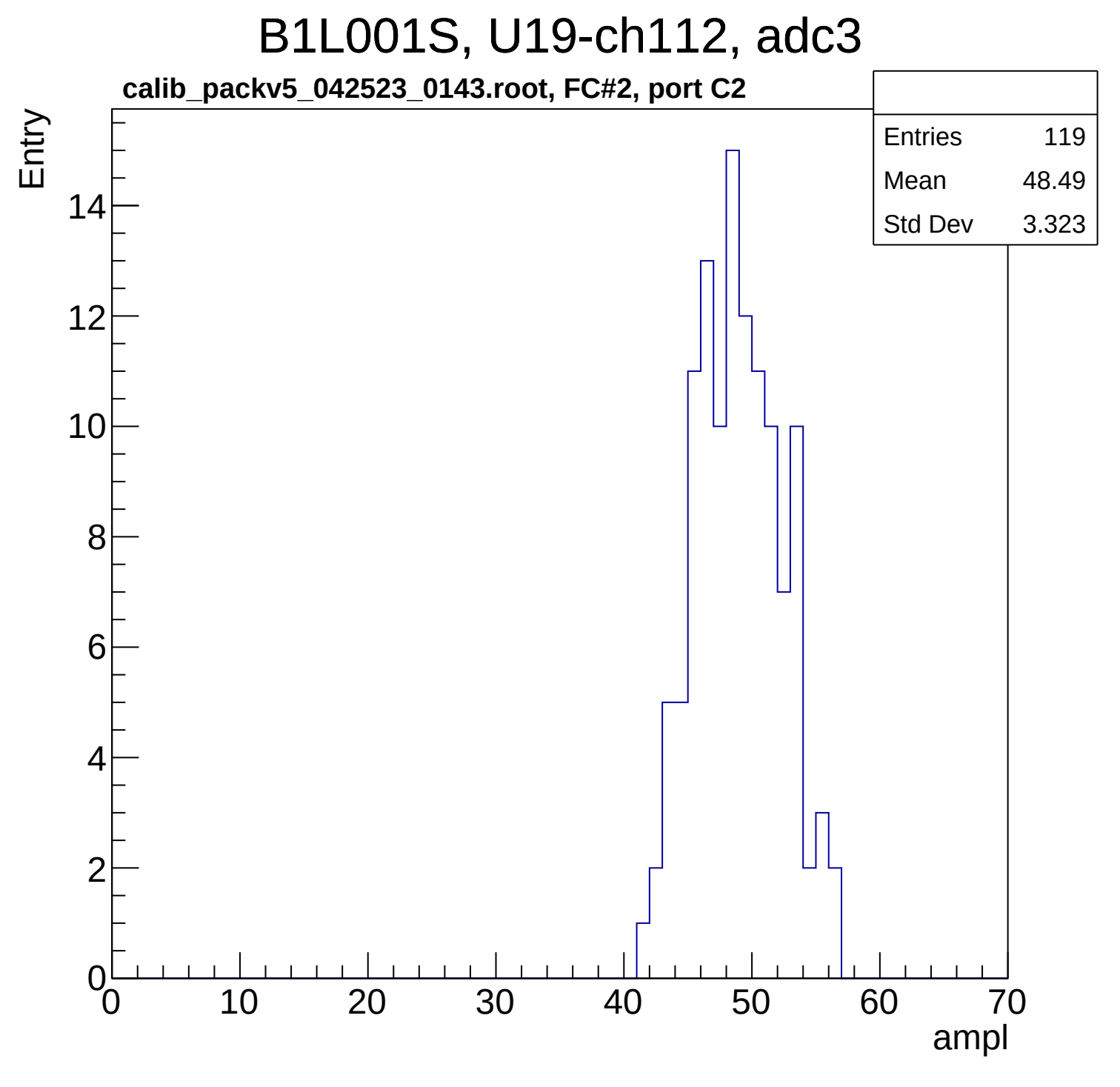
B1L001S, U19-ch112, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 119
Mean 48.49
Std Dev 3.323
Entry
ampl
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2
4
6
8
10
12
14
0
10
20
30
40
50
60
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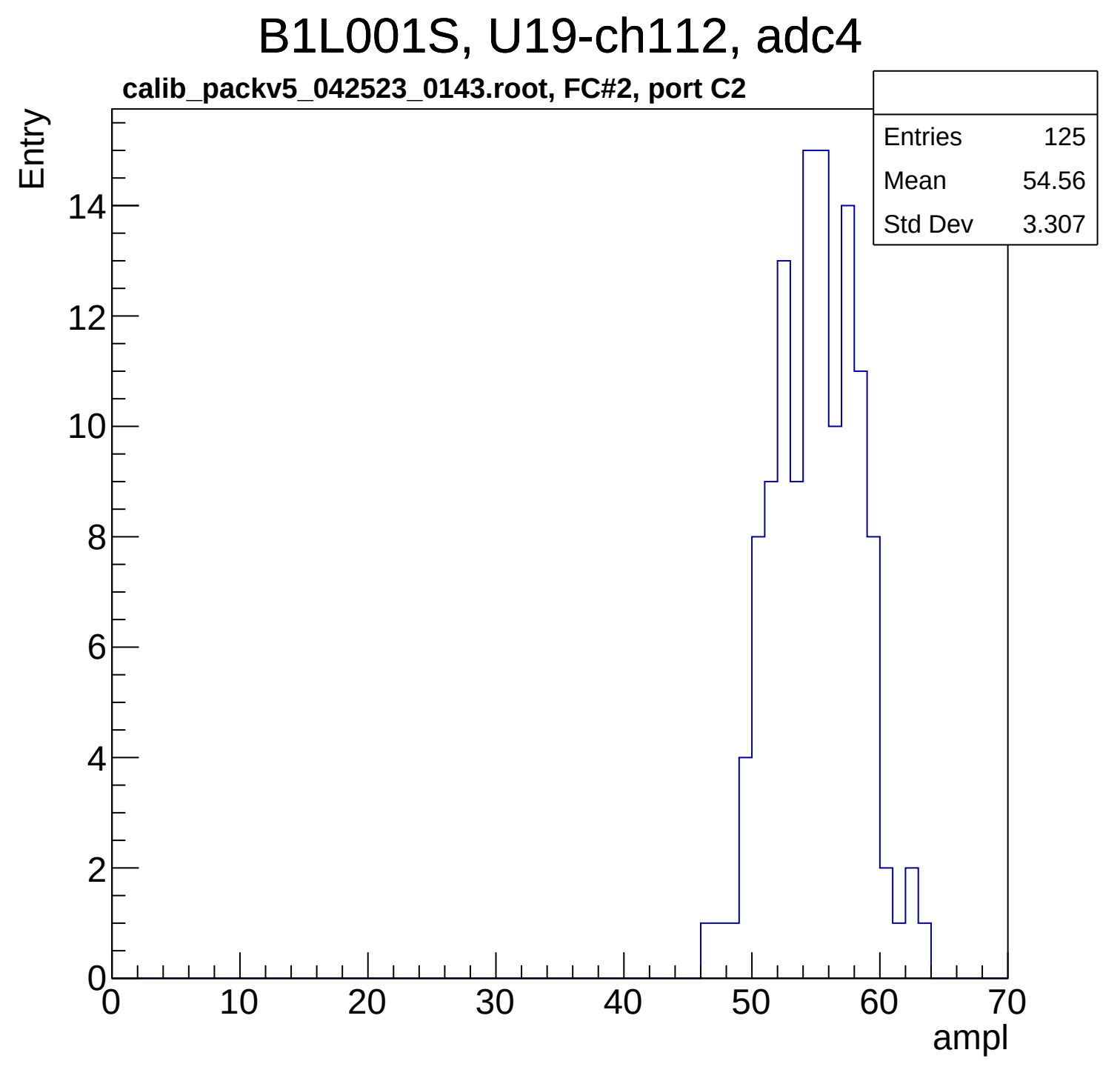
B1L001S, U19-ch112, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 125
Mean 54.56
Std Dev 3.307
Entry
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2
4
6
8
10
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10
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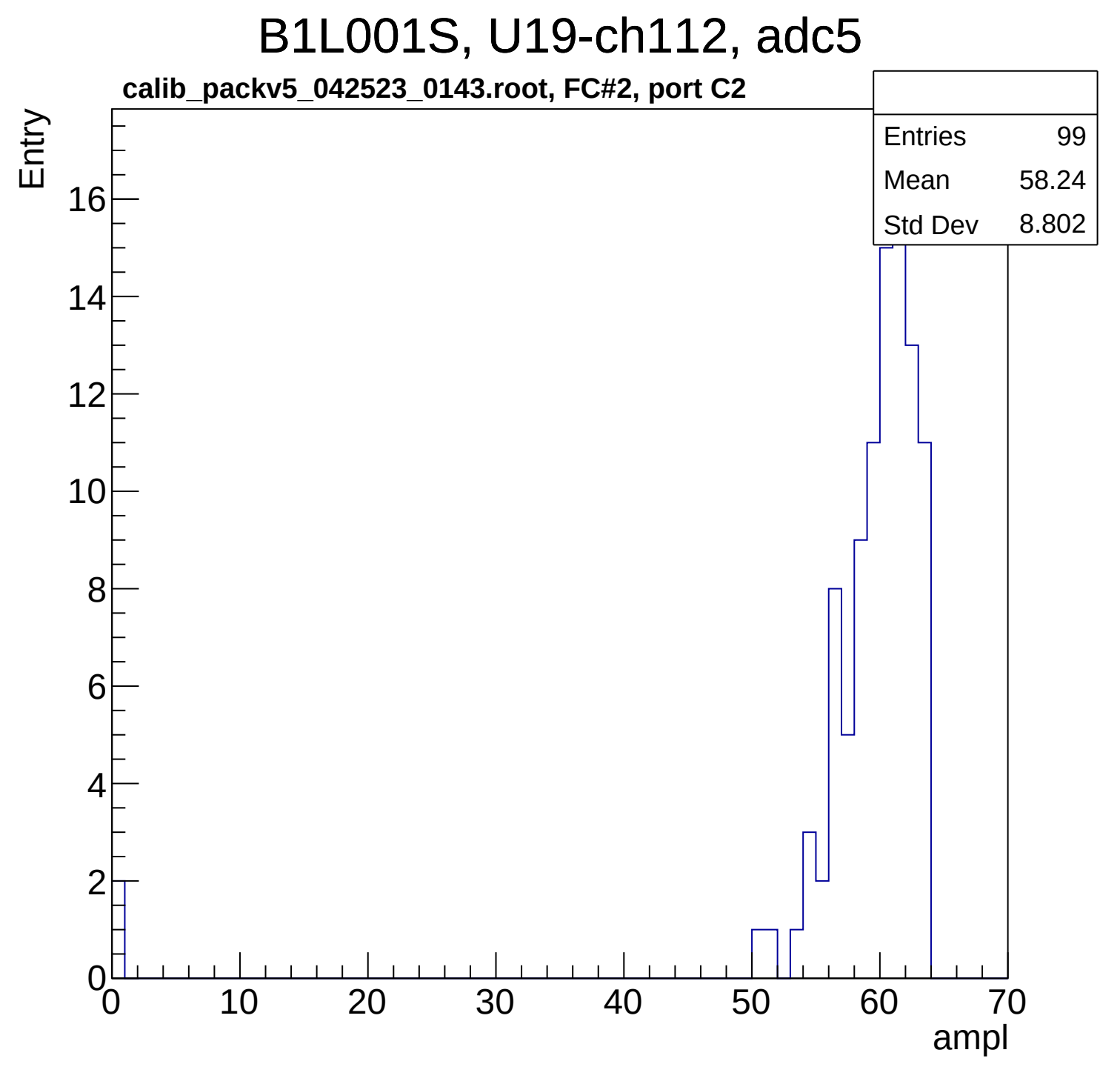
70
ampl


B1L001S, U19-ch112, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 99
Mean 58.24
Std Dev 8.802
Entry
ampl
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2
4
6
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0
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60
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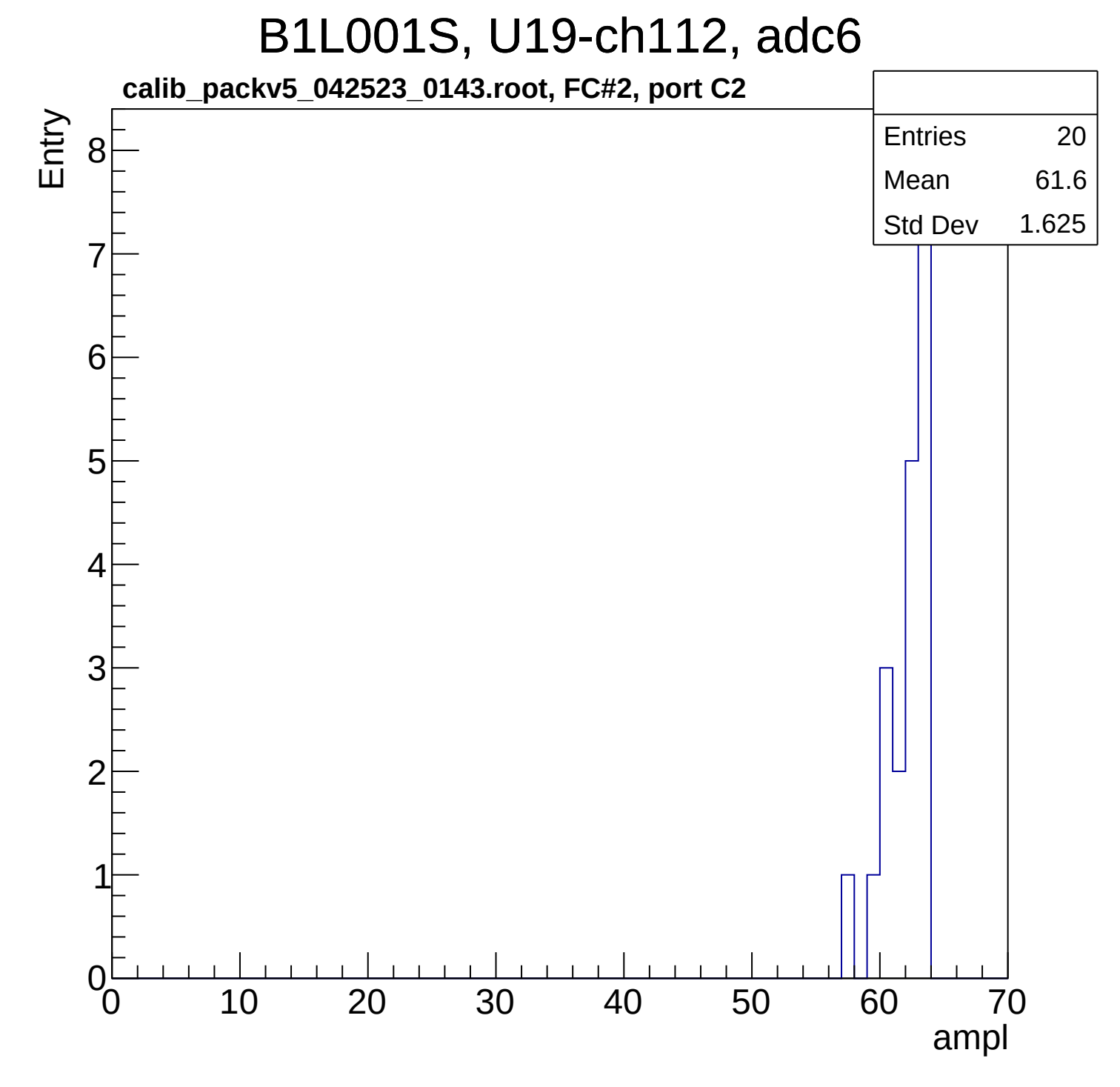
B1L001S, U19-ch112, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 20
Mean 61.6
Std Dev 1.625
Entry
ampl
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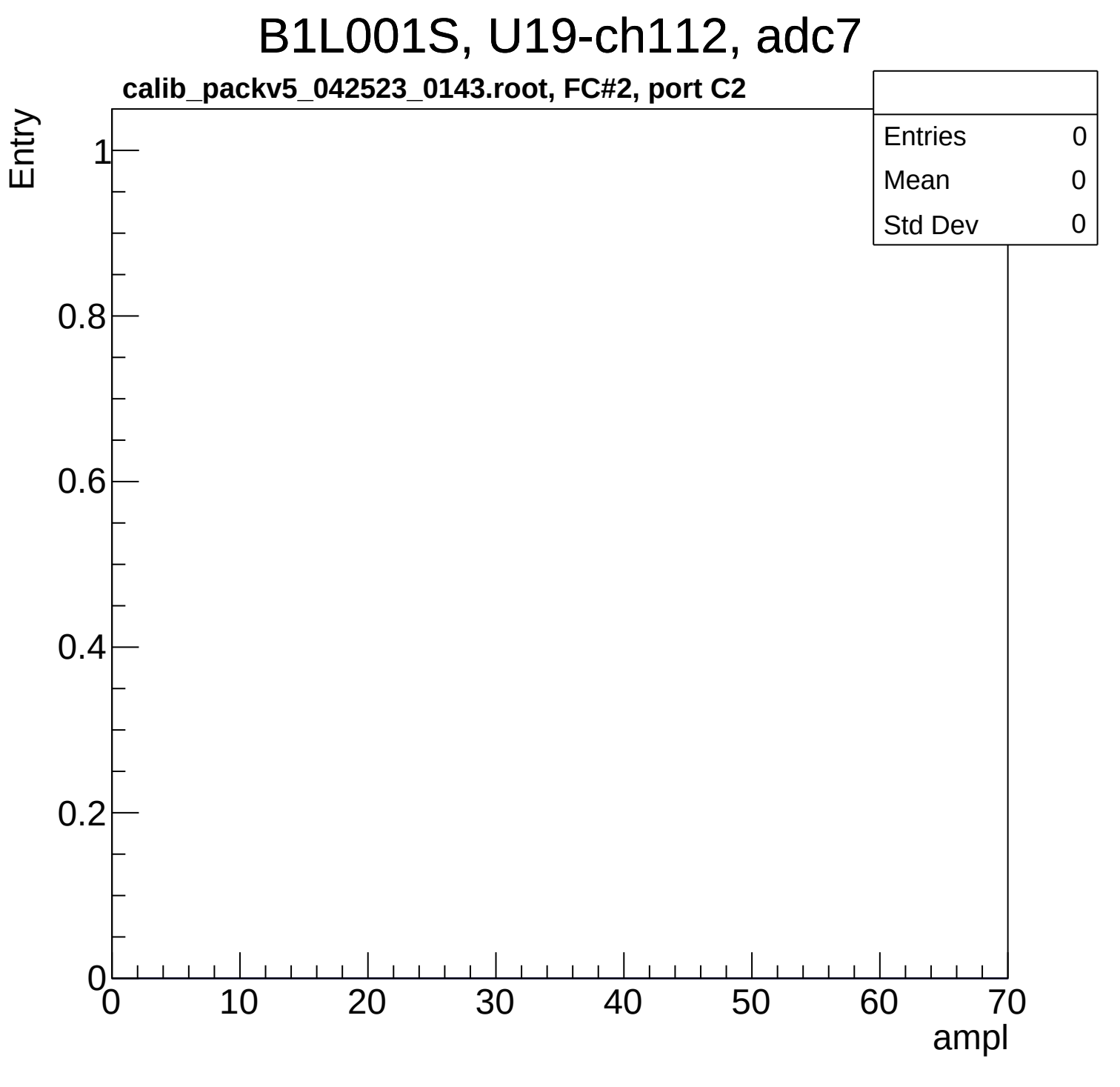
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L001S, U19-ch112, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 0
Mean 0
Std Dev 0
Entry
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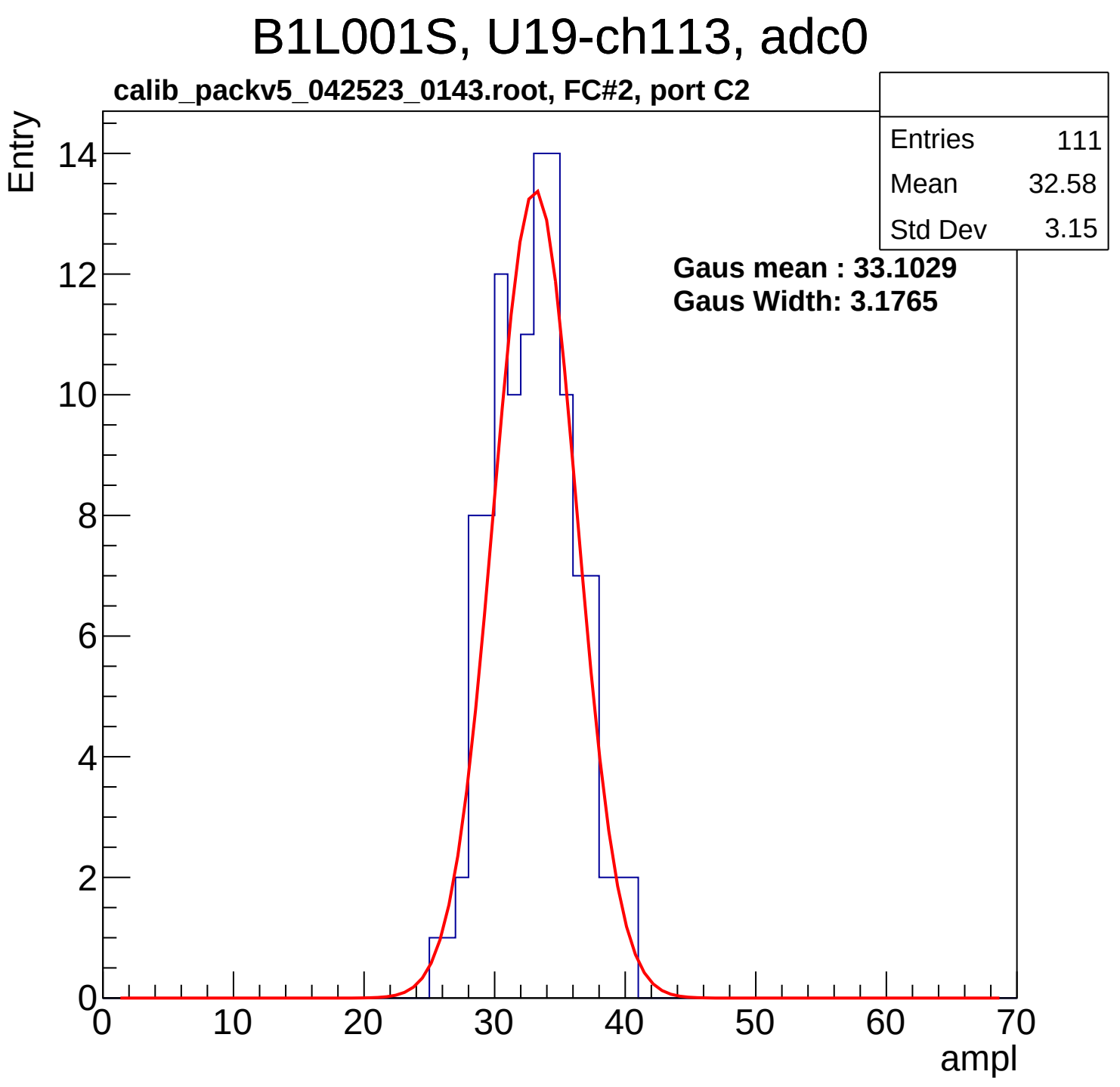
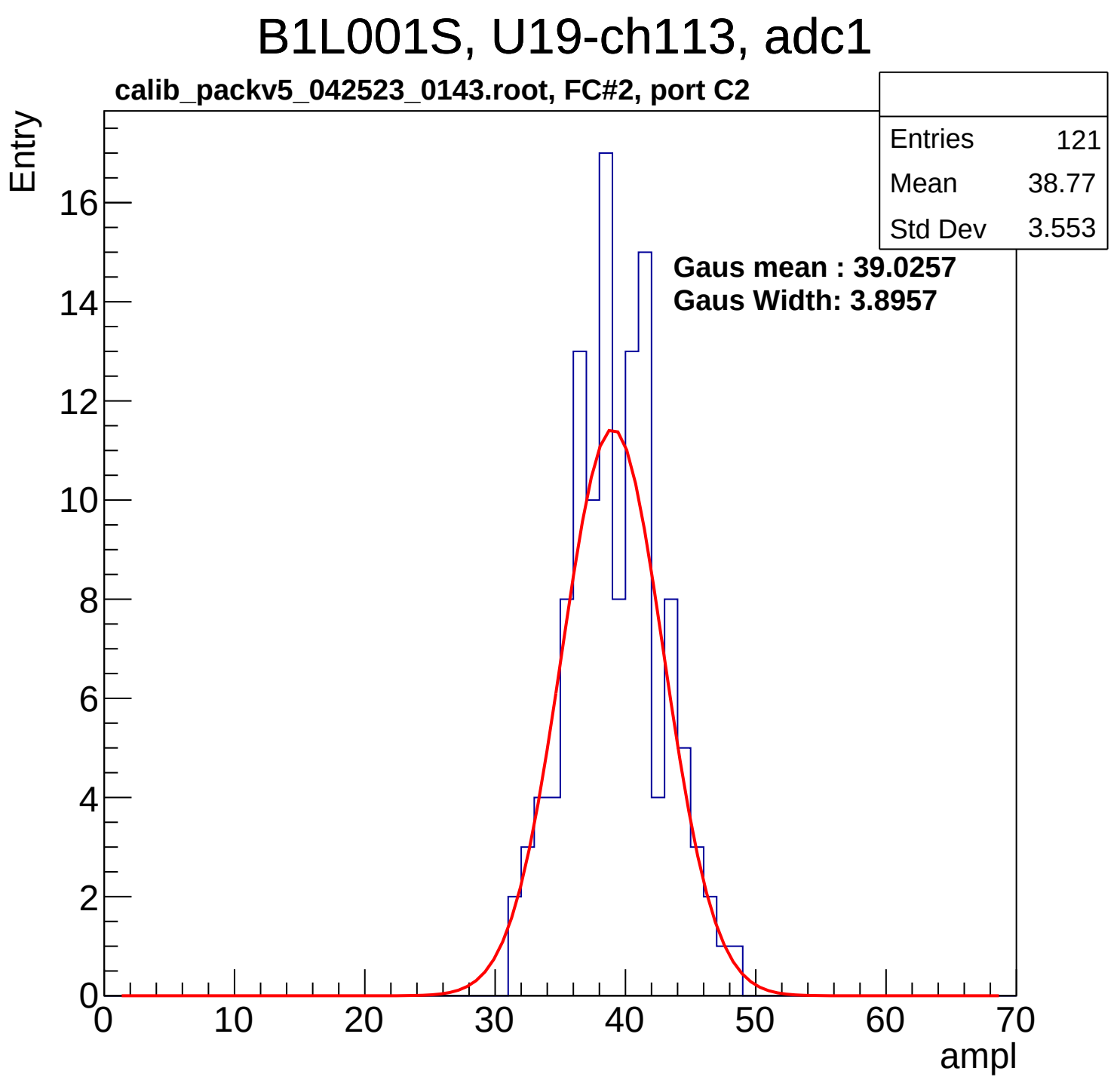
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch113, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 111
Mean 32.58
Std Dev 3.15
Gaus mean : 33.1029
Gaus Width: 3.1765
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L001S, U19-ch113, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 121
Mean 38.77
Std Dev 3.553
Gaus mean : 39.0257
Gaus Width: 3.8957
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
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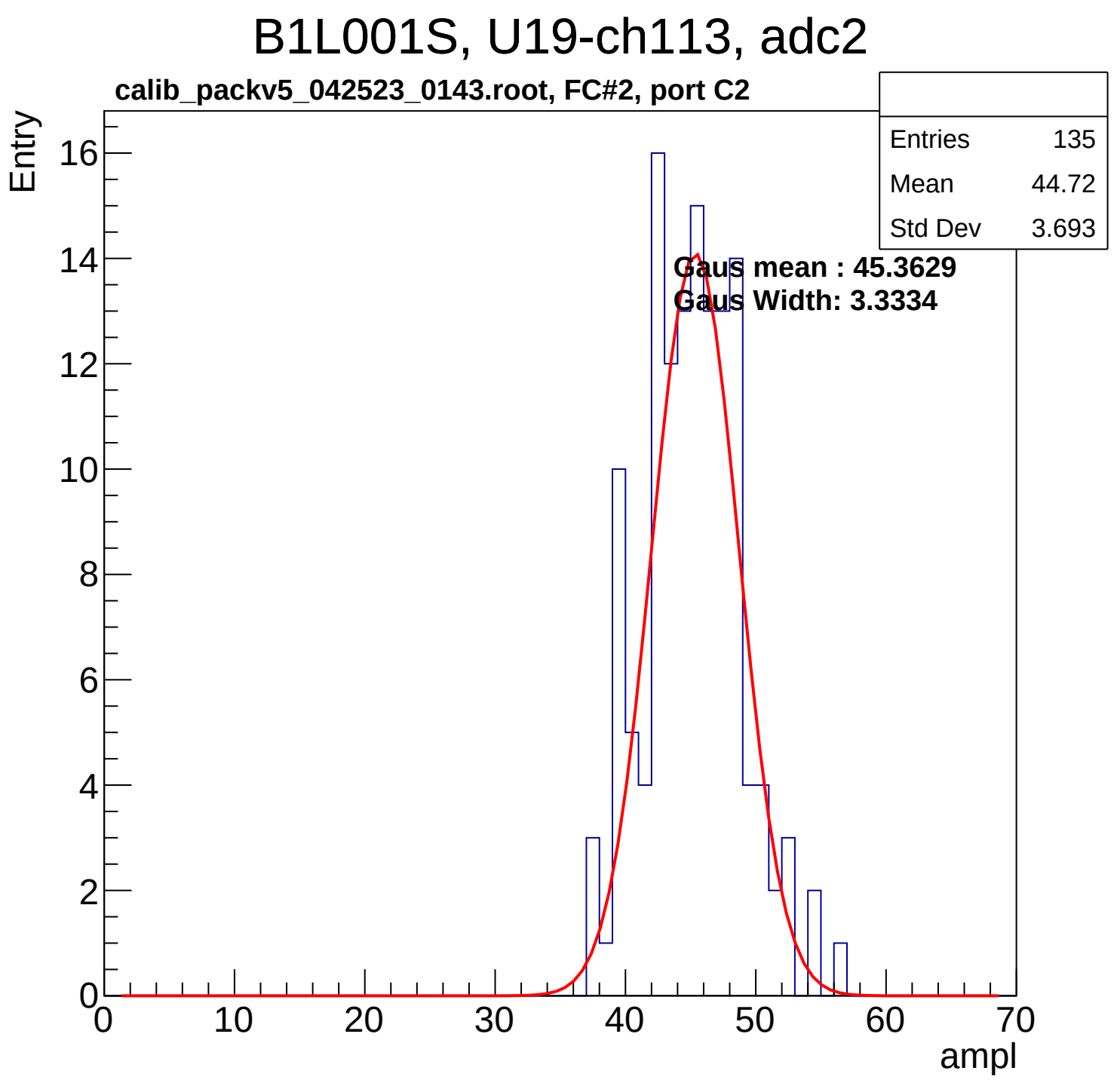
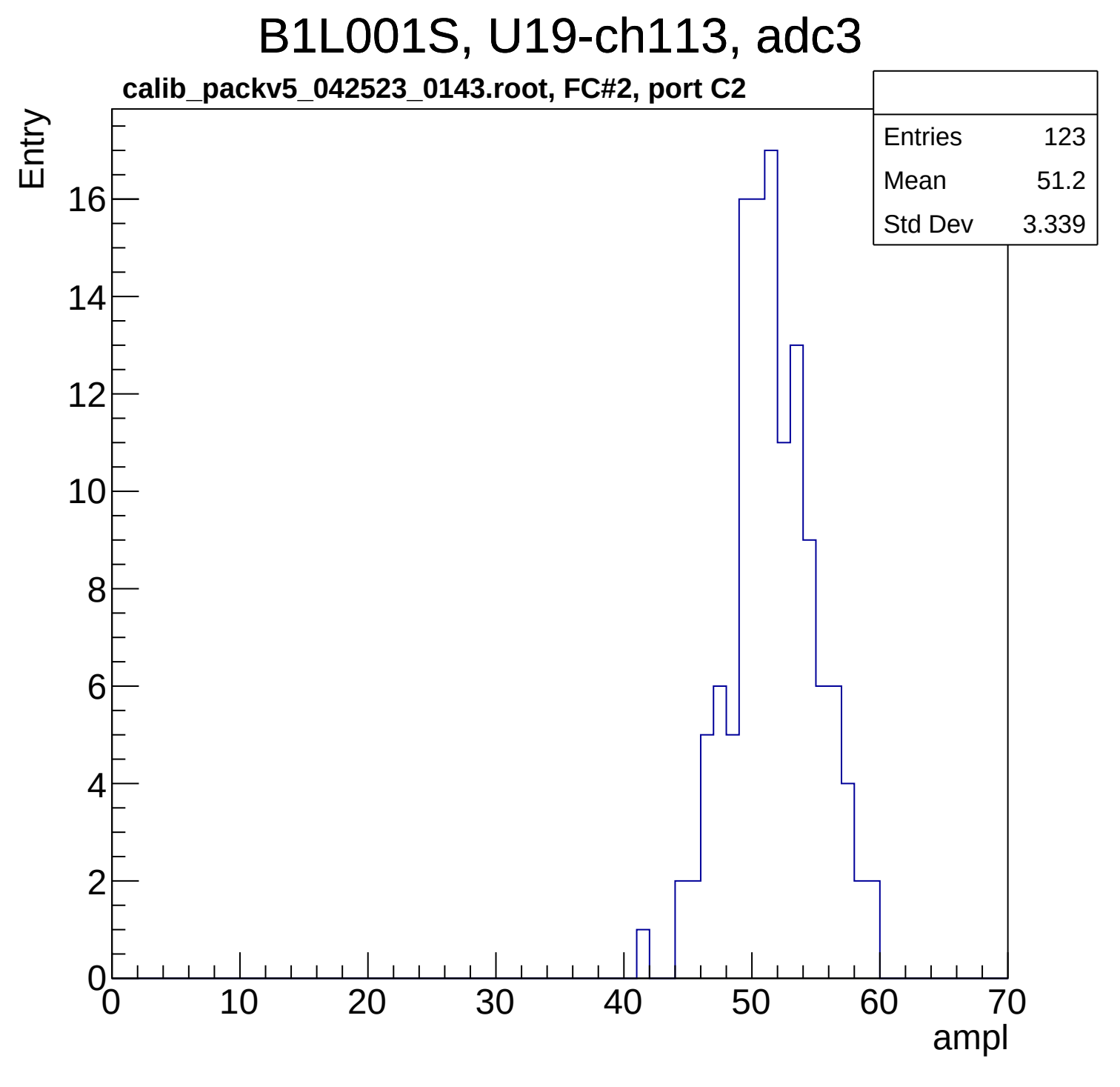

B1L001S, U19-ch113, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 135
Mean 44.72
Std Dev 3.693
Gaus mean : 45.3629
Gaus Width: 3.3334
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70


B1L001S, U19-ch113, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 123
Mean 51.2
Std Dev 3.339
Entry
ampl
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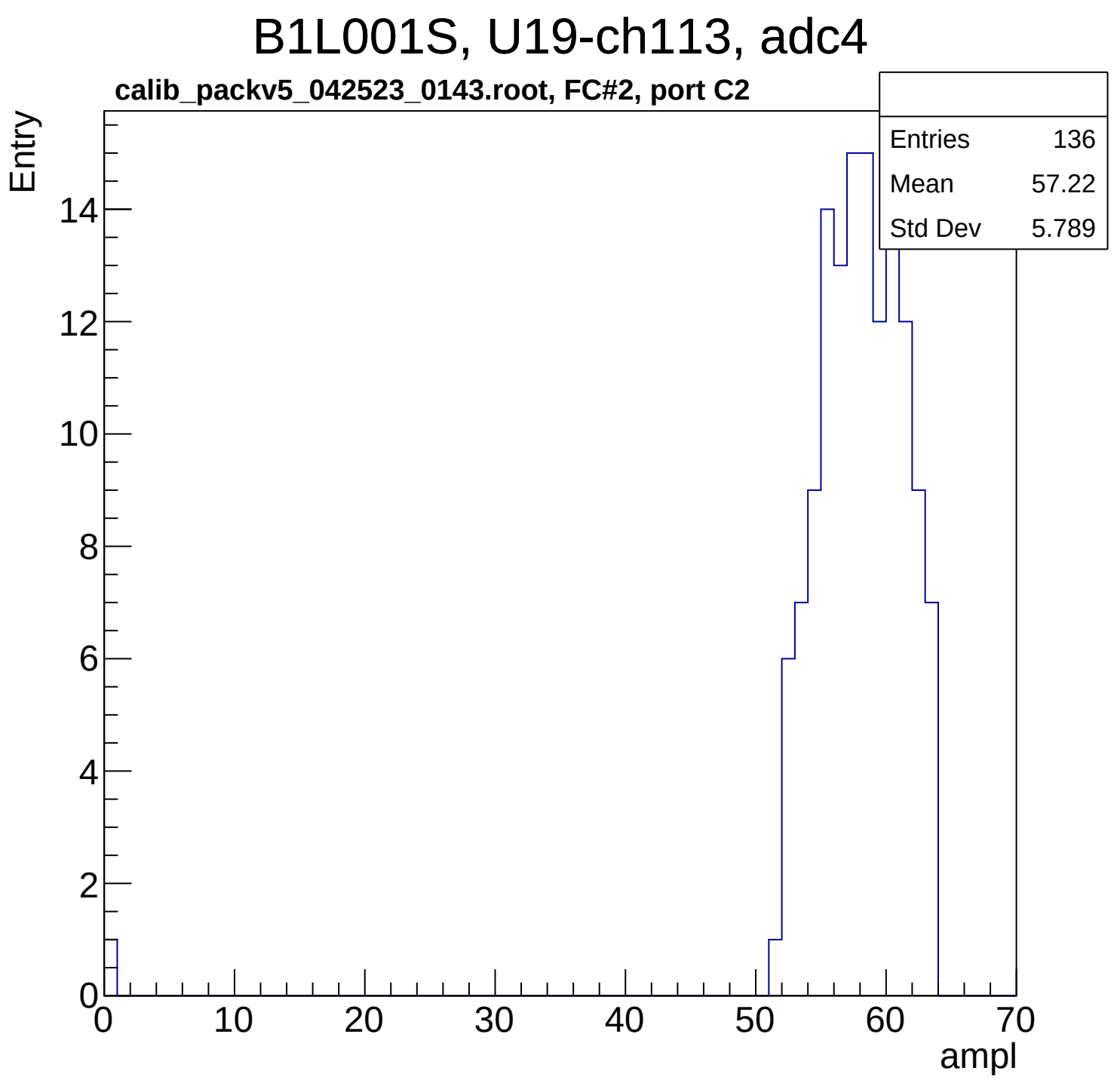
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70


B1L001S, U19-ch113, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 136
Mean 57.22
Std Dev 5.789
Entry
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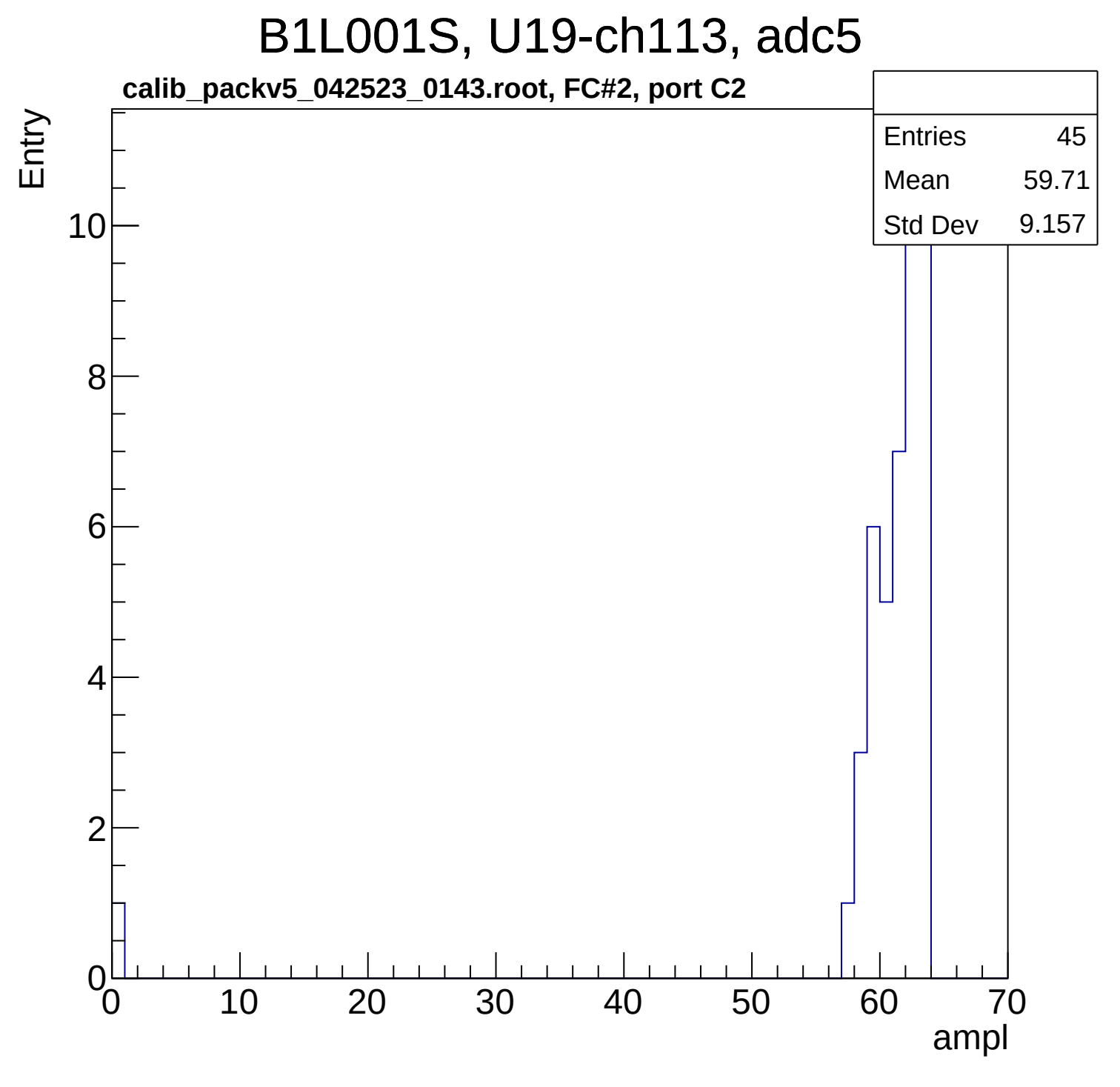
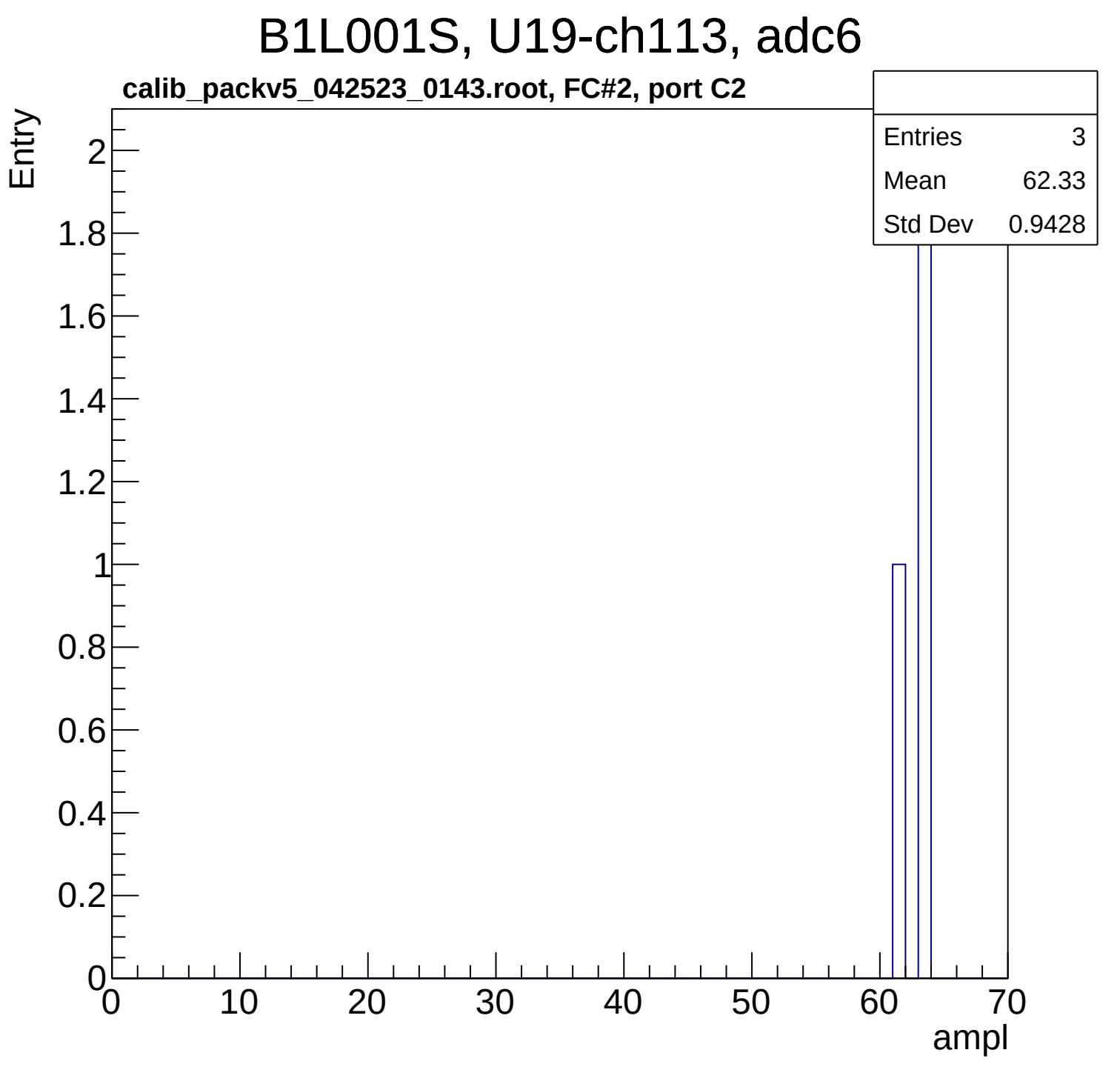
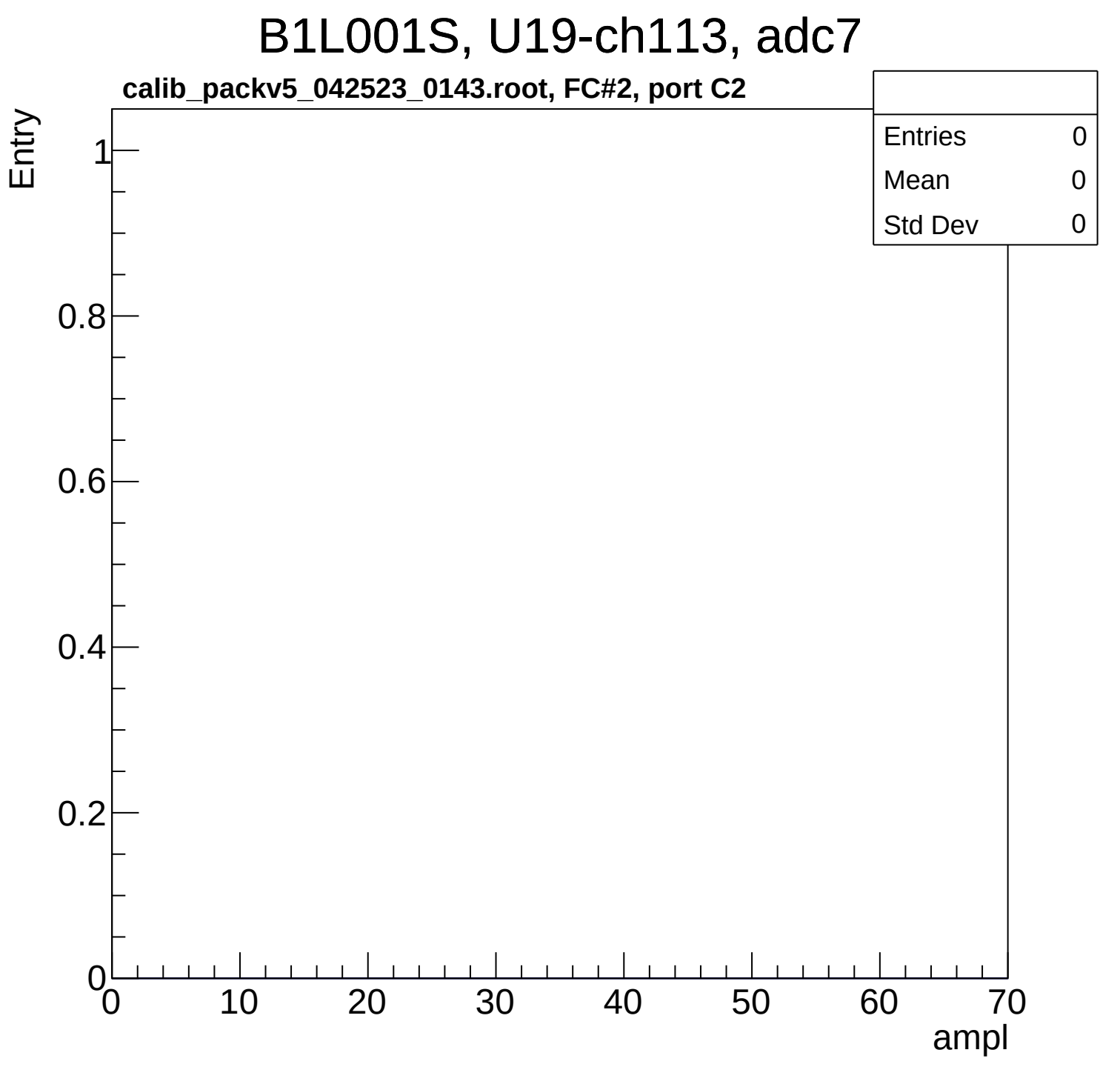
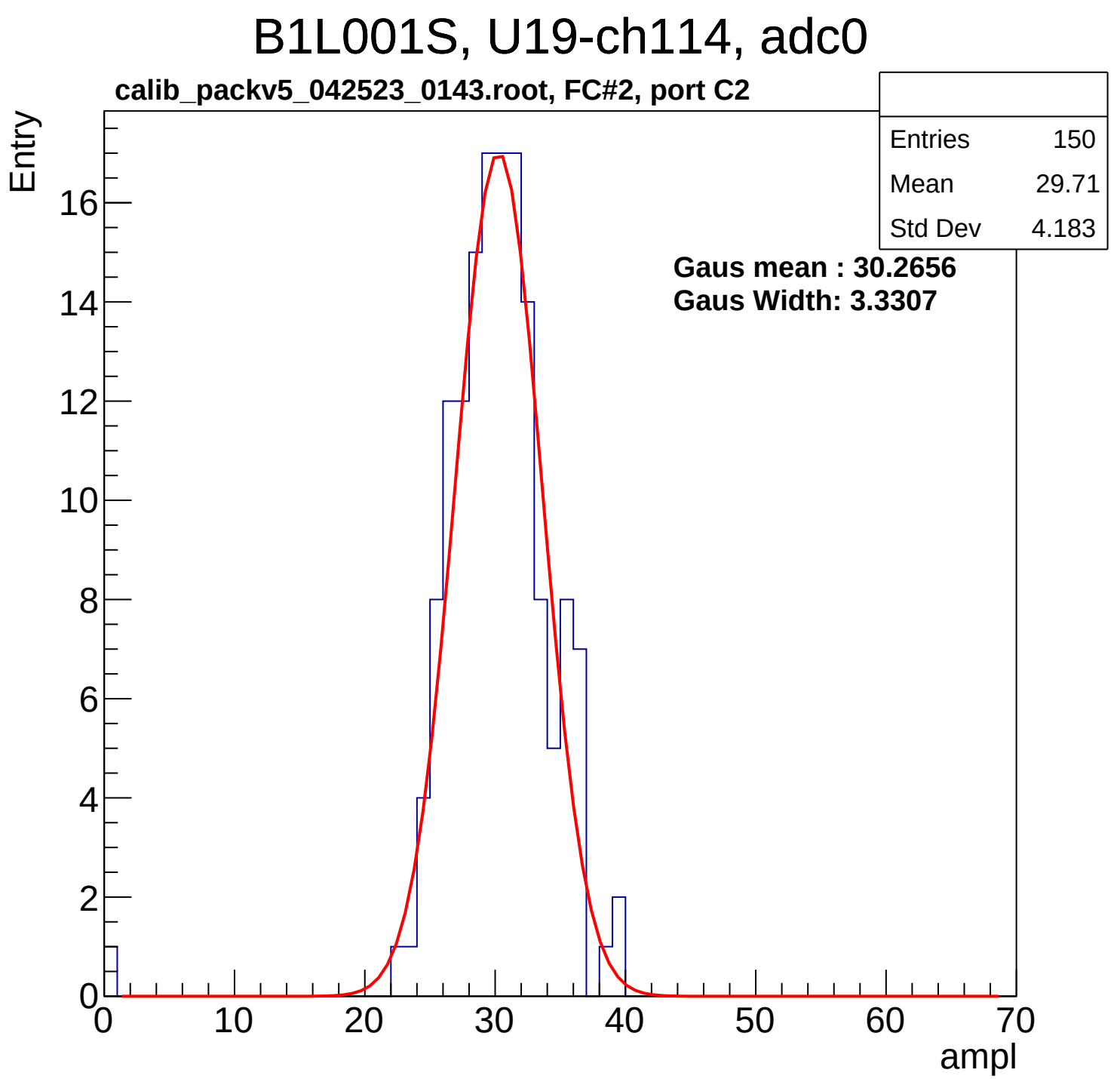
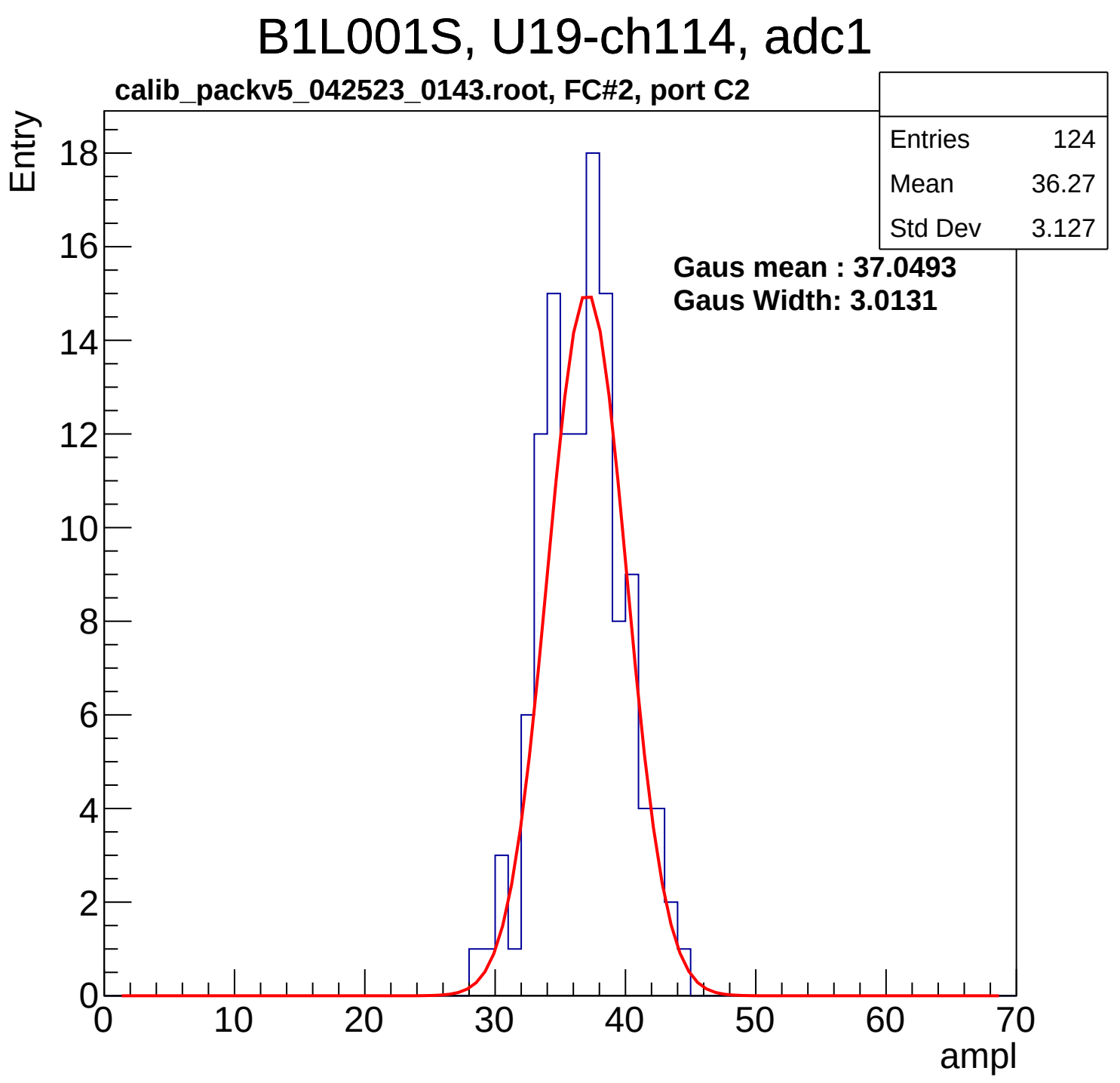
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl

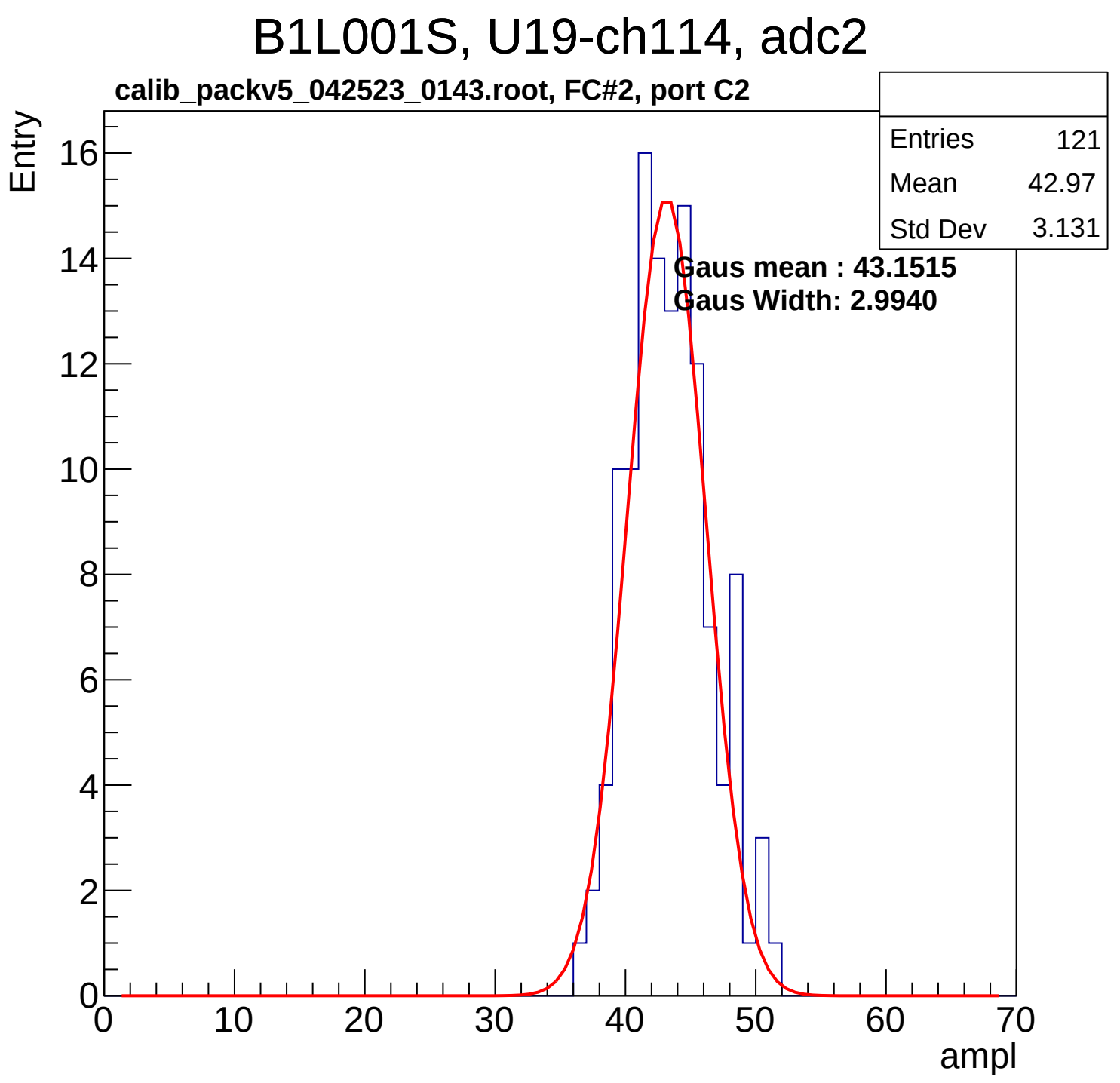

B1L001S, U19-ch113, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 45
Mean 59.71
Std Dev 9.157
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch113, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 3
Mean 62.33
Std Dev 0.9428
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L001S, U19-ch113, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch114, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 150
Mean 29.71
Std Dev 4.183
Gaus mean : 30.2656
Gaus Width: 3.3307
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70


B1L001S, U19-ch114, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 124
Mean 36.27
Std Dev 3.127
Gaus mean : 37.0493
Gaus Width: 3.0131
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70


B1L001S, U19-ch114, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 121
Mean 42.97
Std Dev 3.131
Gaus mean : 43.1515
Gaus Width: 2.9940
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
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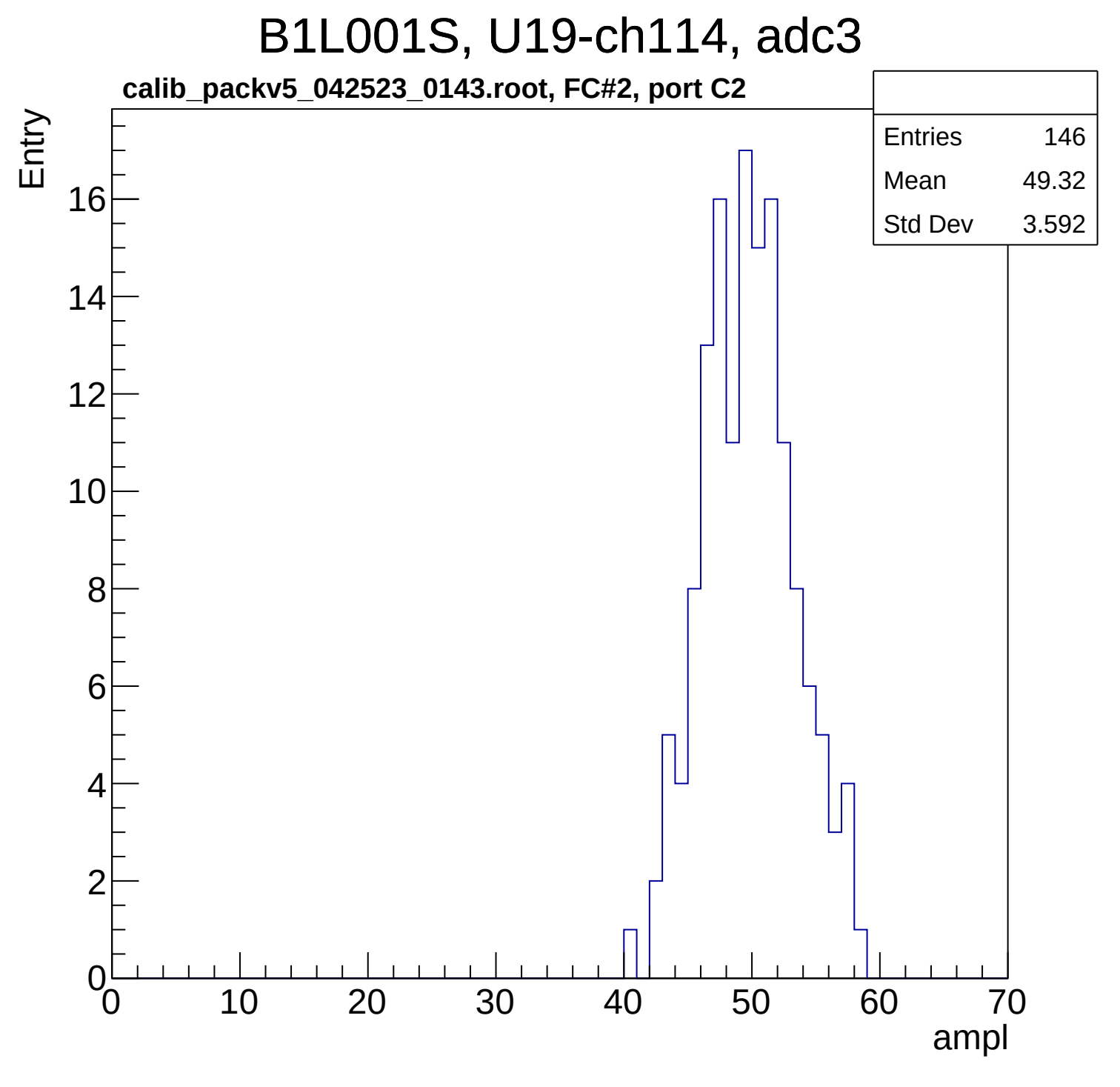
B1L001S, U19-ch114, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 146
Mean 49.32
Std Dev 3.592
Entry
ampl
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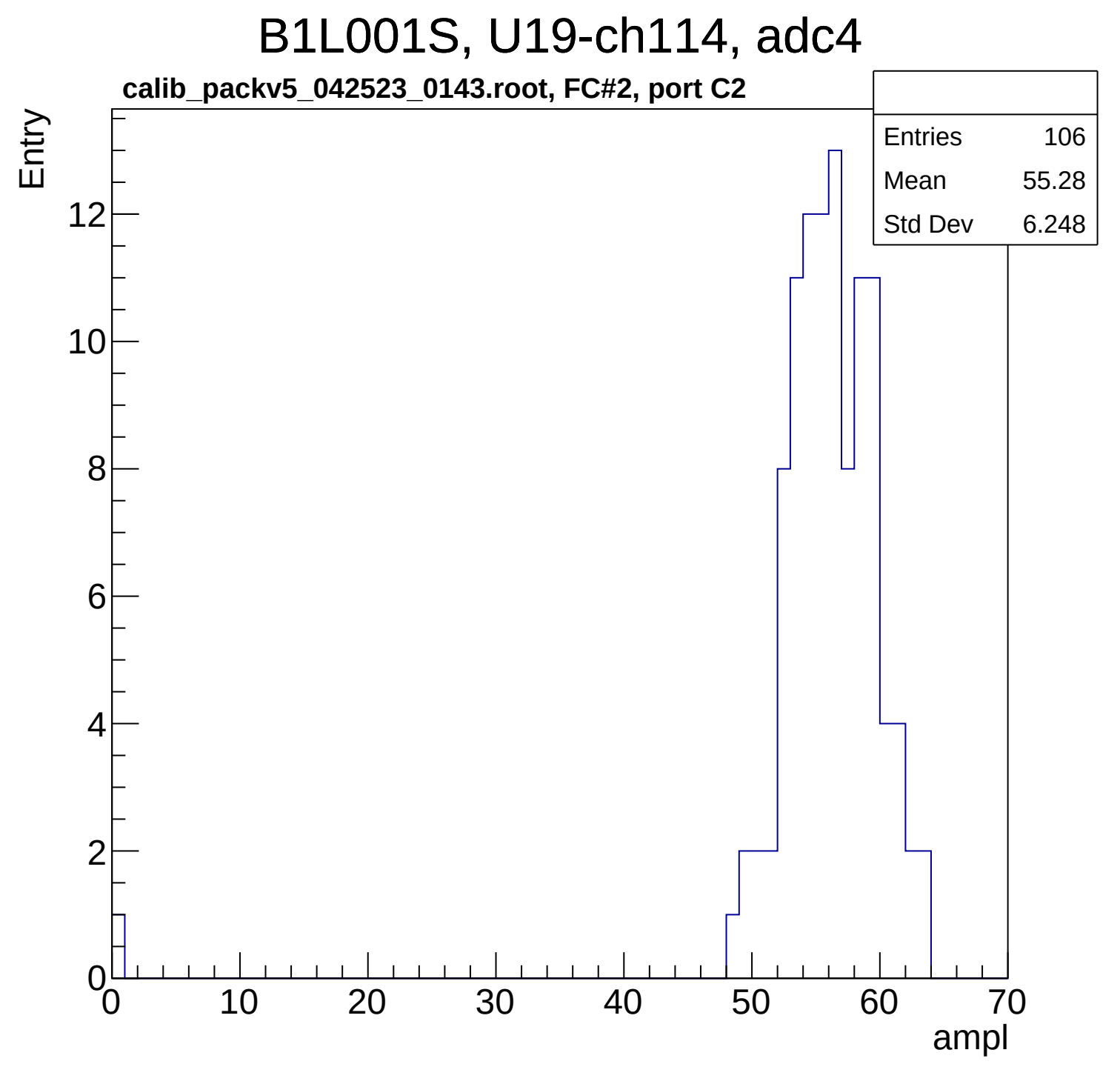
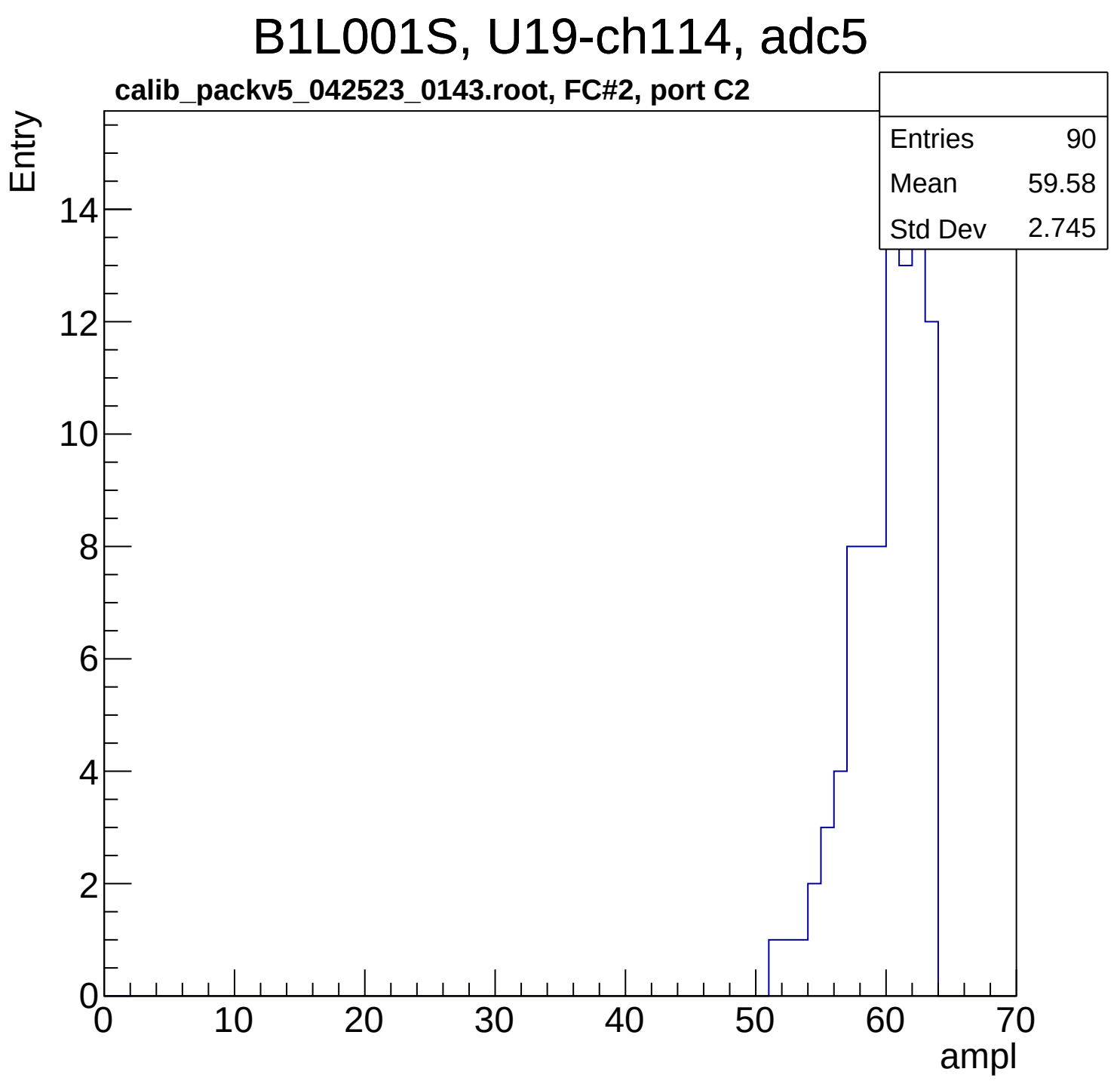
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70


B1L001S, U19-ch114, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 106
Mean 55.28
Std Dev 6.248
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch114, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 90
Mean 59.58
Std Dev 2.745
Entry
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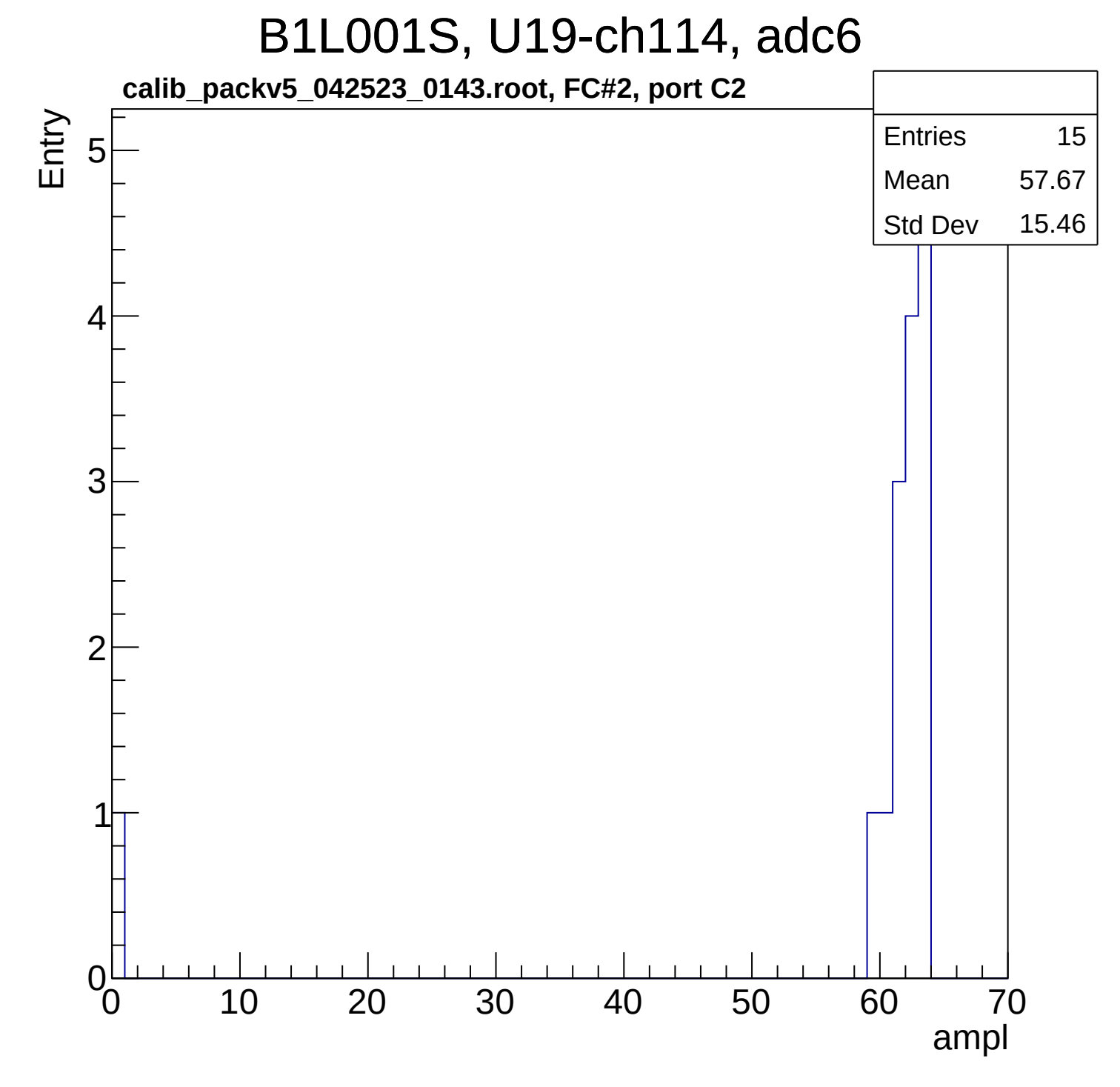
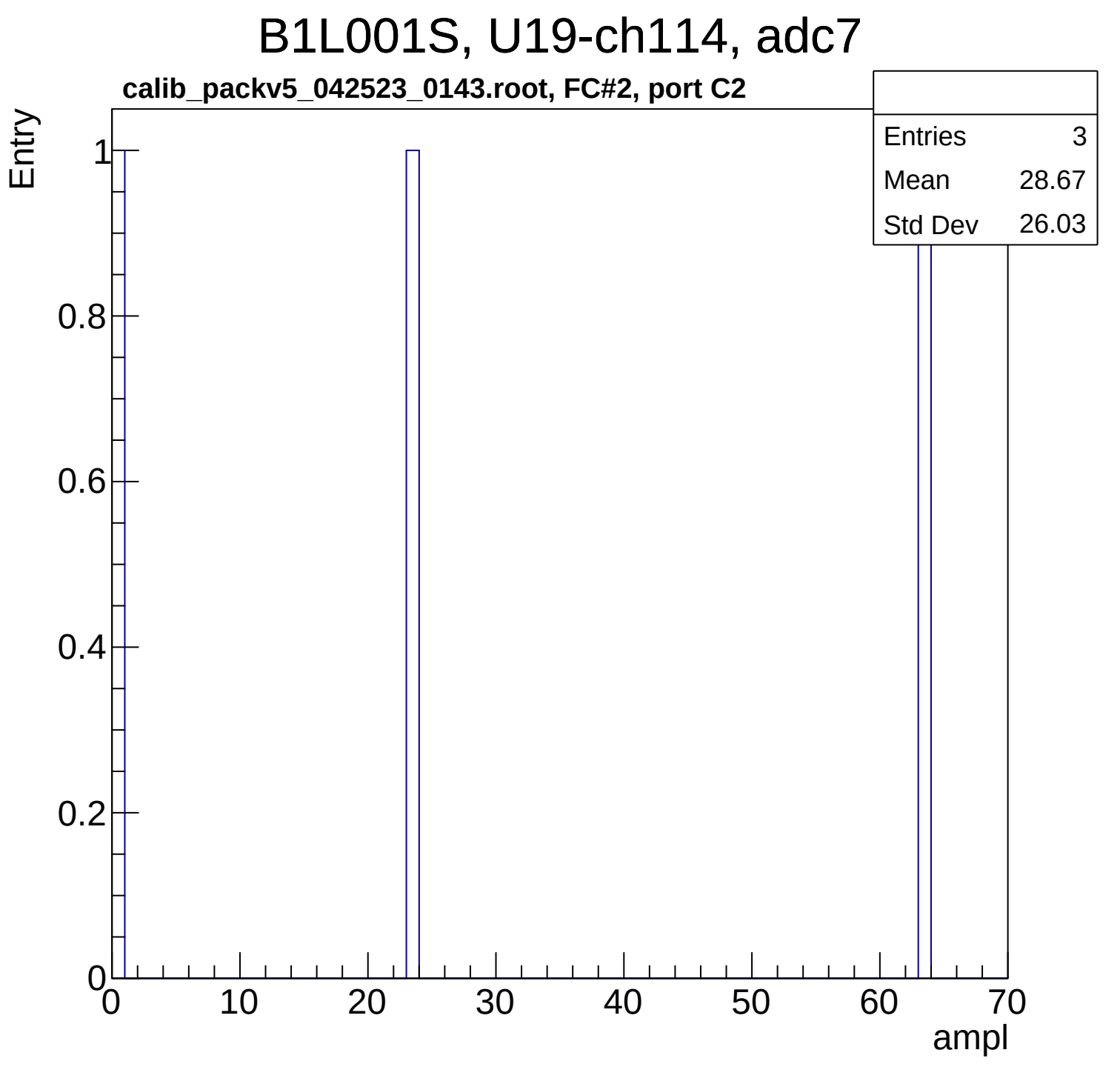
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch114, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 15
Mean 57.67
Std Dev 15.46
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch114, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 3
Mean 28.67
Std Dev 26.03
Entry
ampl
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0.4
0.6
0.8
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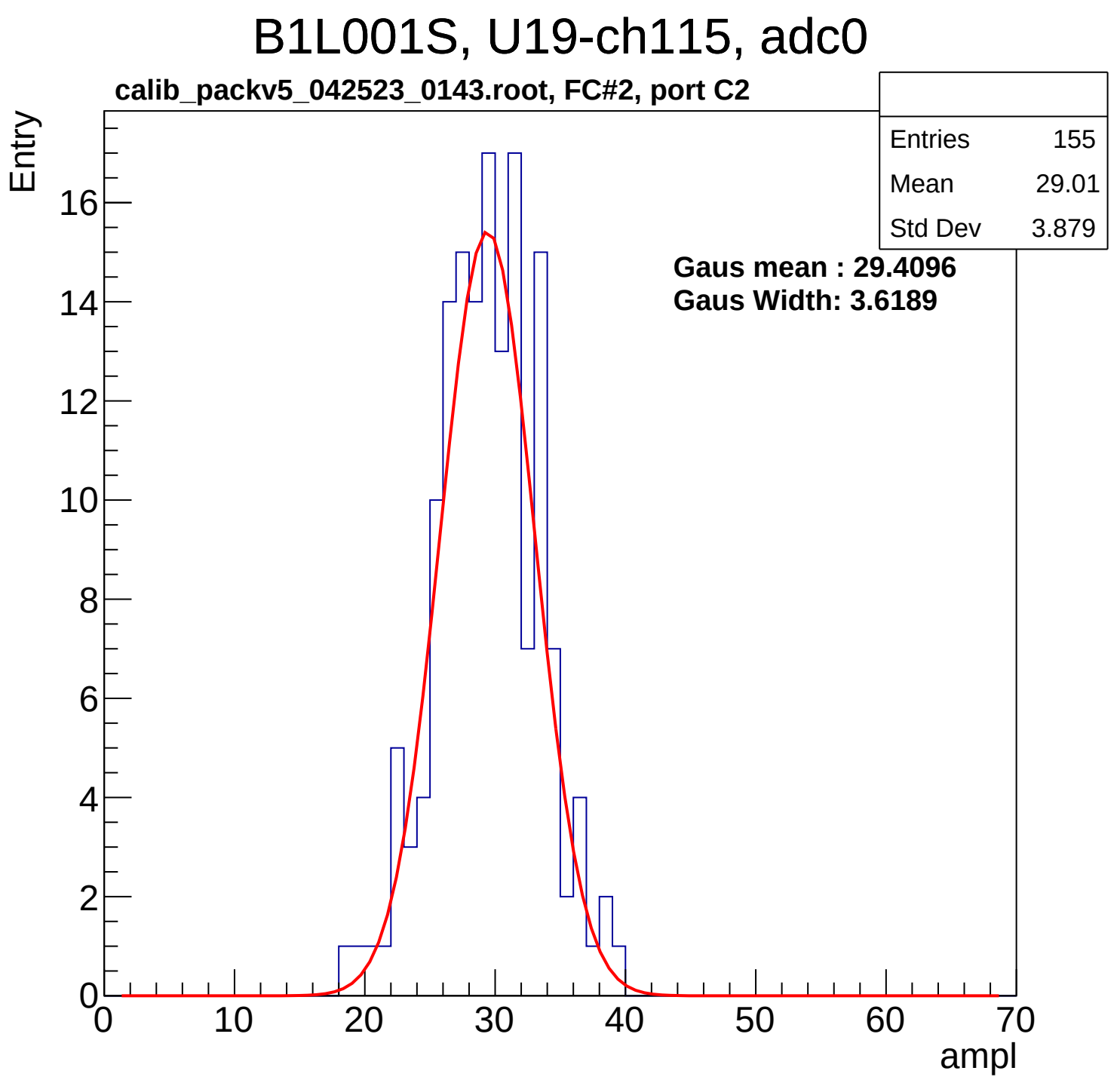
20
30
40
50
60
70


B1L001S, U19-ch115, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 155
Mean 29.01
Std Dev 3.879
Gaus mean : 29.4096
Gaus Width: 3.6189
Entry
ampl
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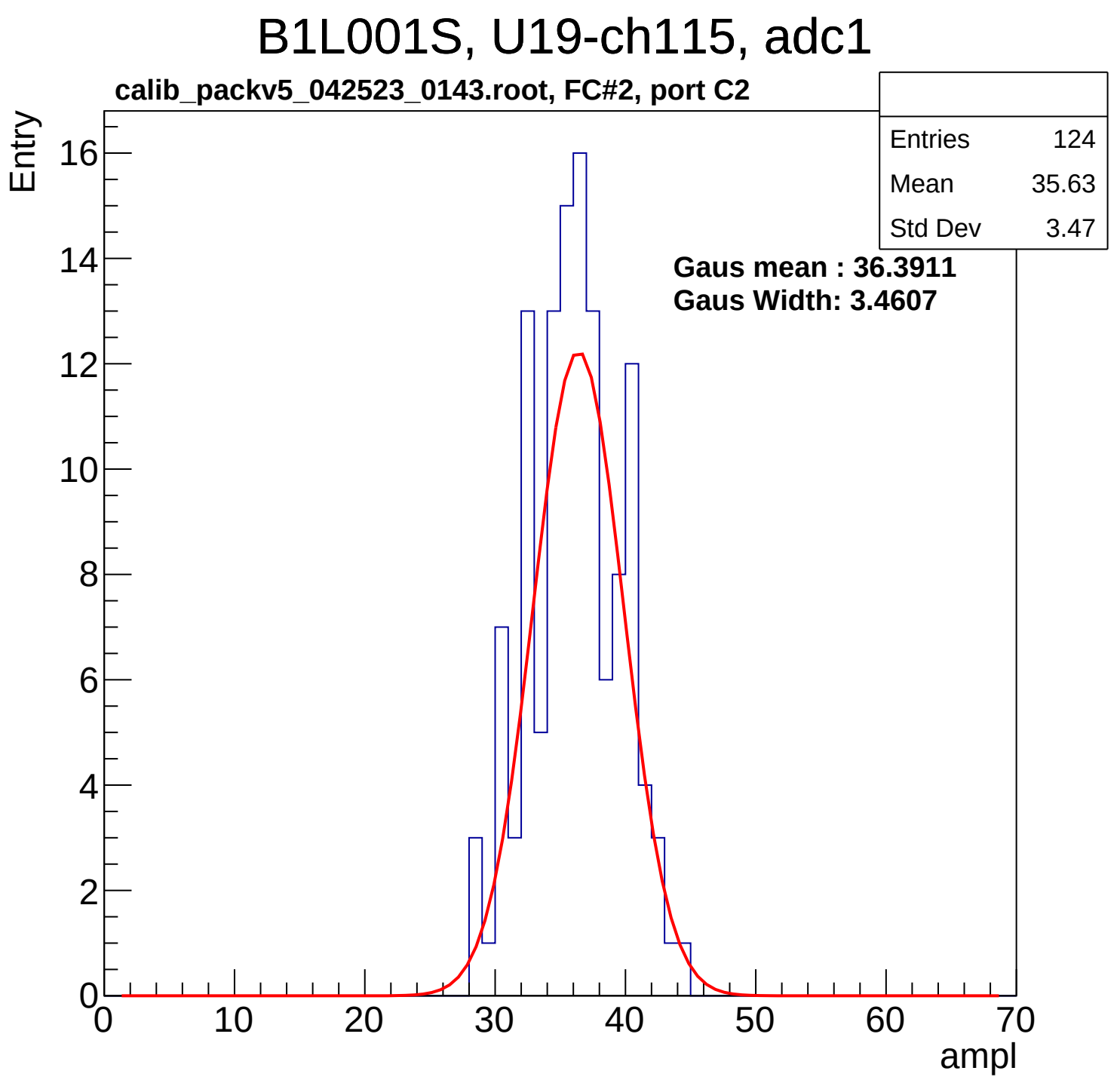
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70


B1L001S, U19-ch115, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 124
Mean 35.63
Std Dev 3.47
Gaus mean : 36.3911
Gaus Width: 3.4607
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
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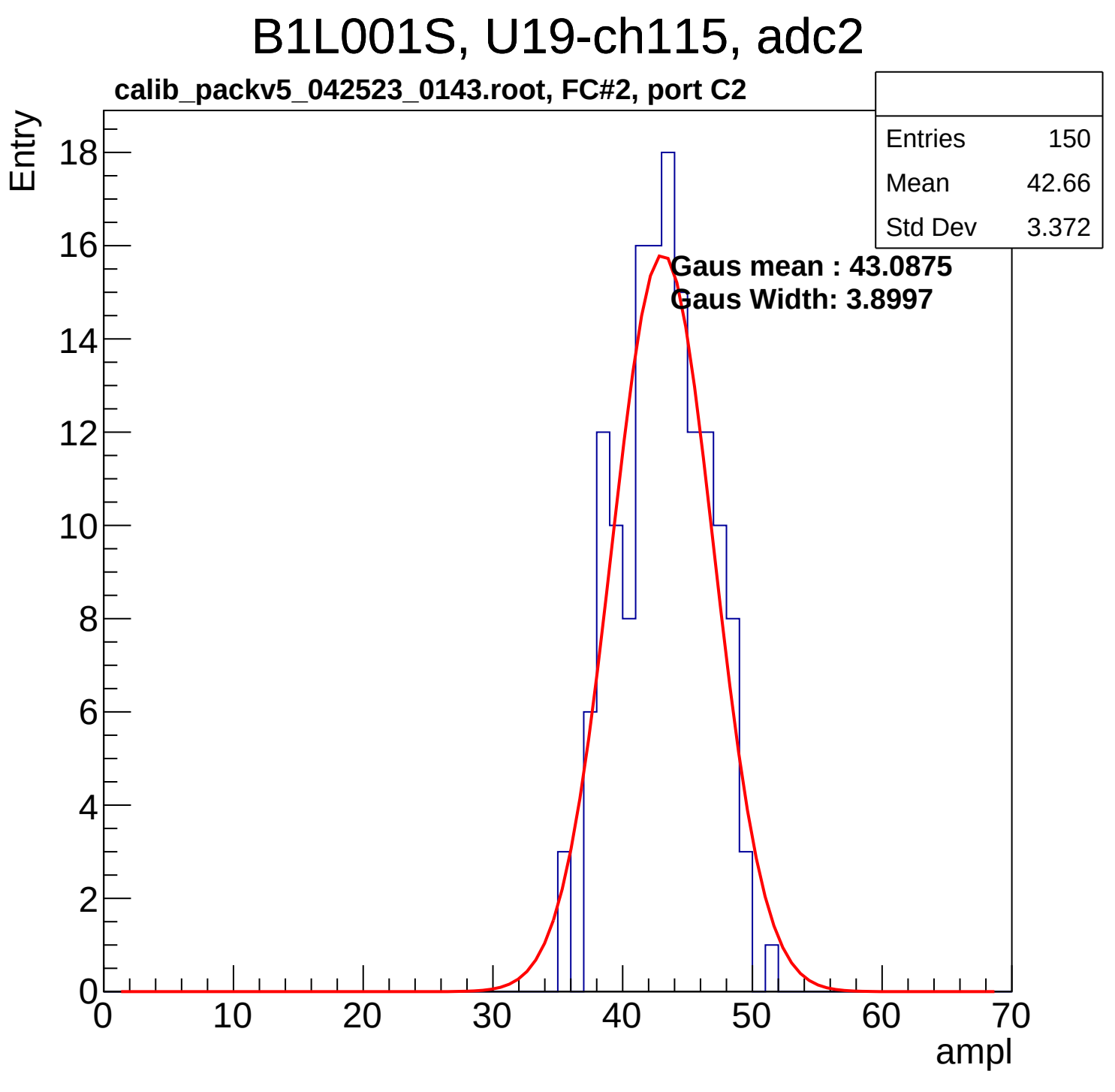
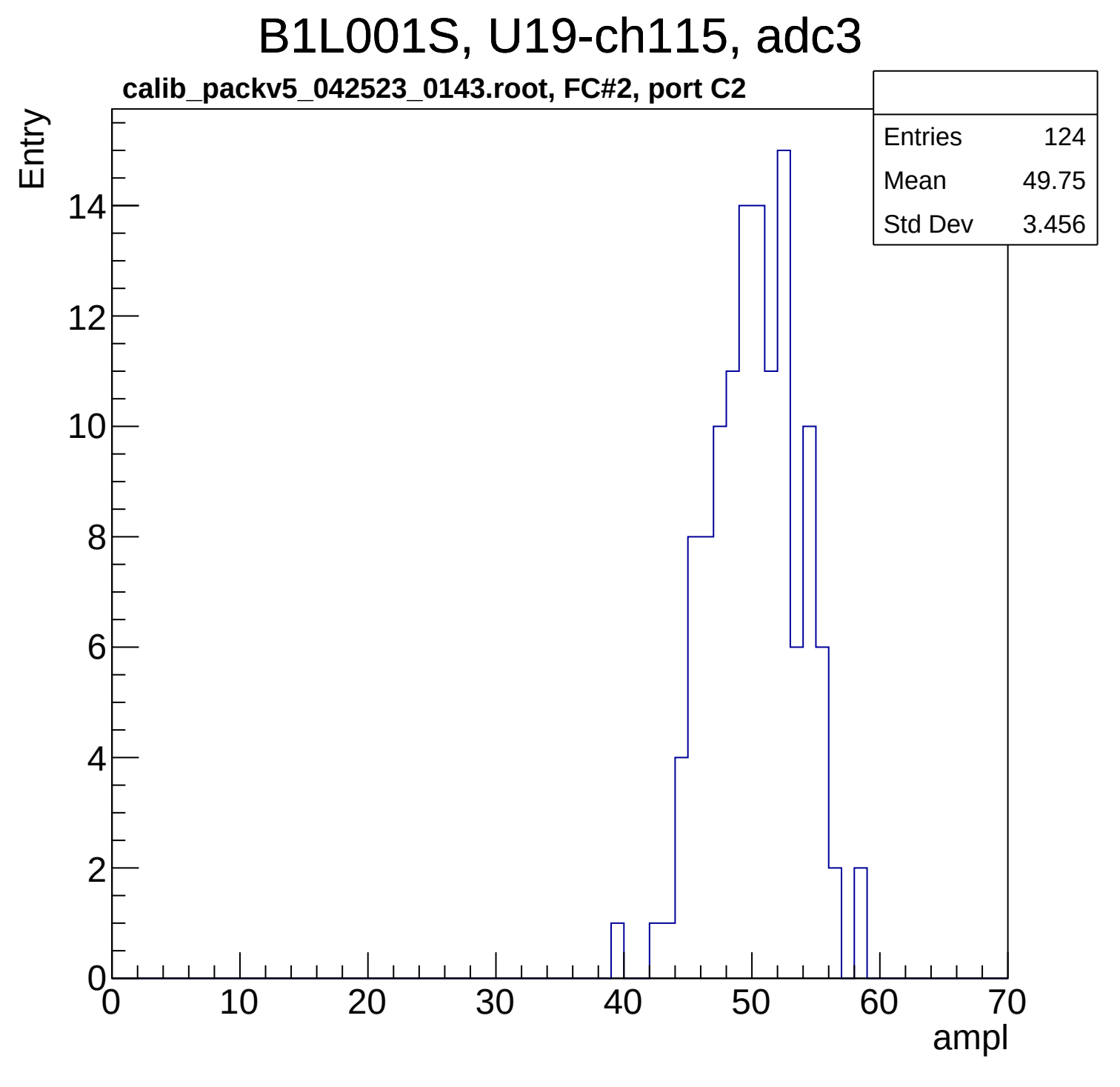

B1L001S, U19-ch115, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 150
Mean 42.66
Std Dev 3.372
Gaus mean : 43.0875
Gaus Width: 3.8997
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70


B1L001S, U19-ch115, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 124
Mean 49.75
Std Dev 3.456
Entry
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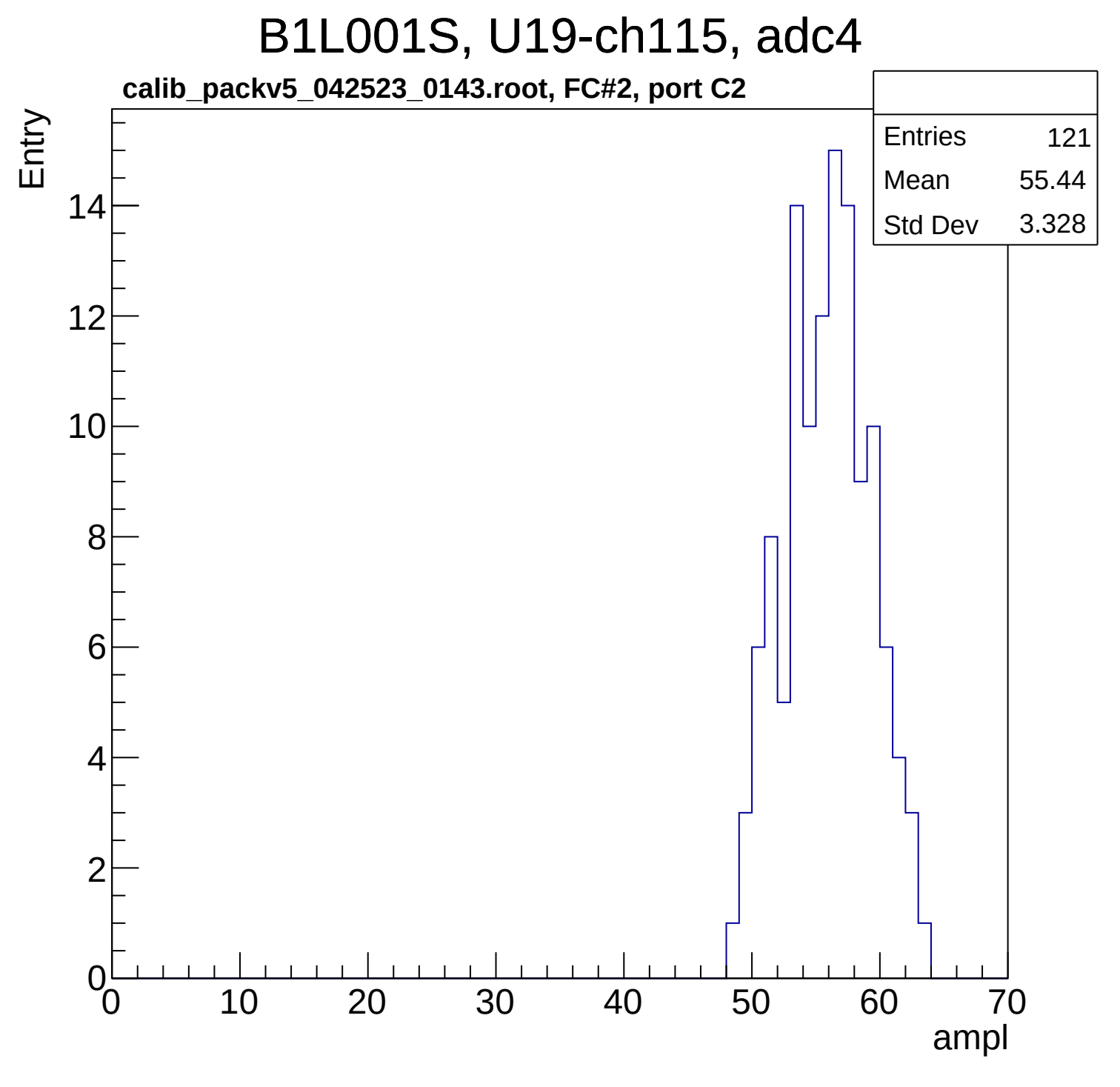
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch115, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 121
Mean 55.44
Std Dev 3.328
Entry
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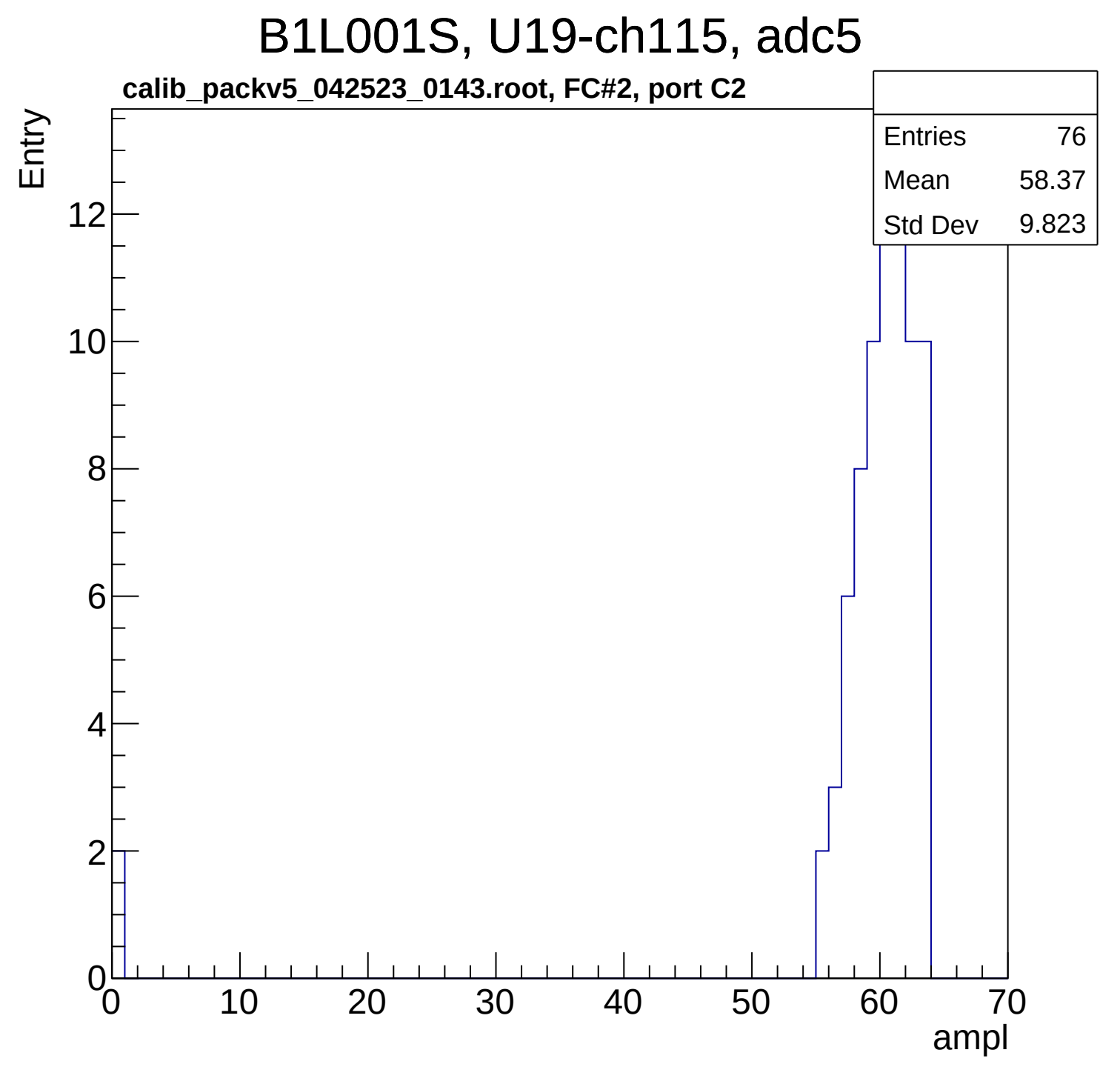
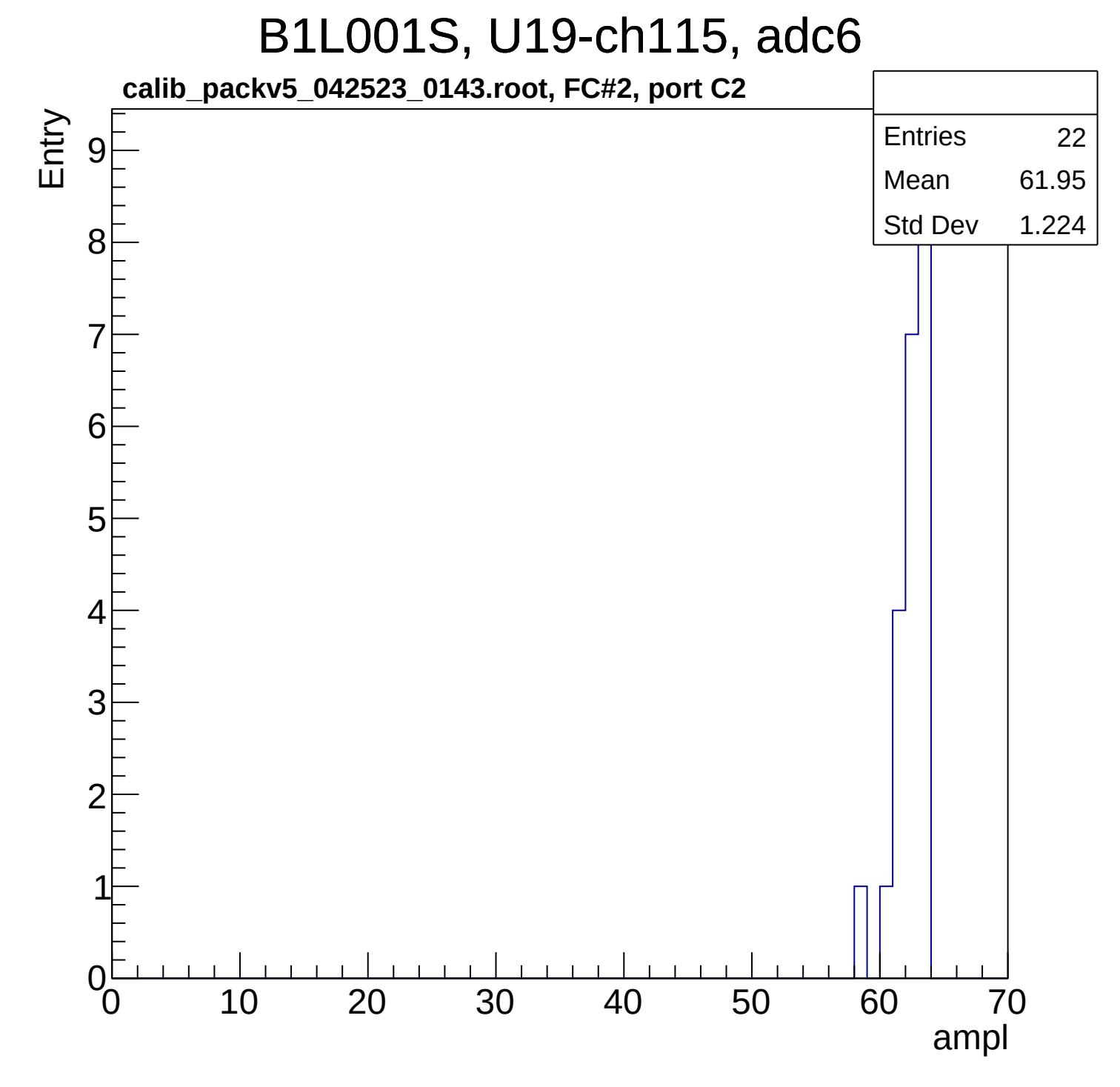
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch115, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 76
Mean 58.37
Std Dev 9.823
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70


B1L001S, U19-ch115, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 22
Mean 61.95
Std Dev 1.224
Entry
ampl
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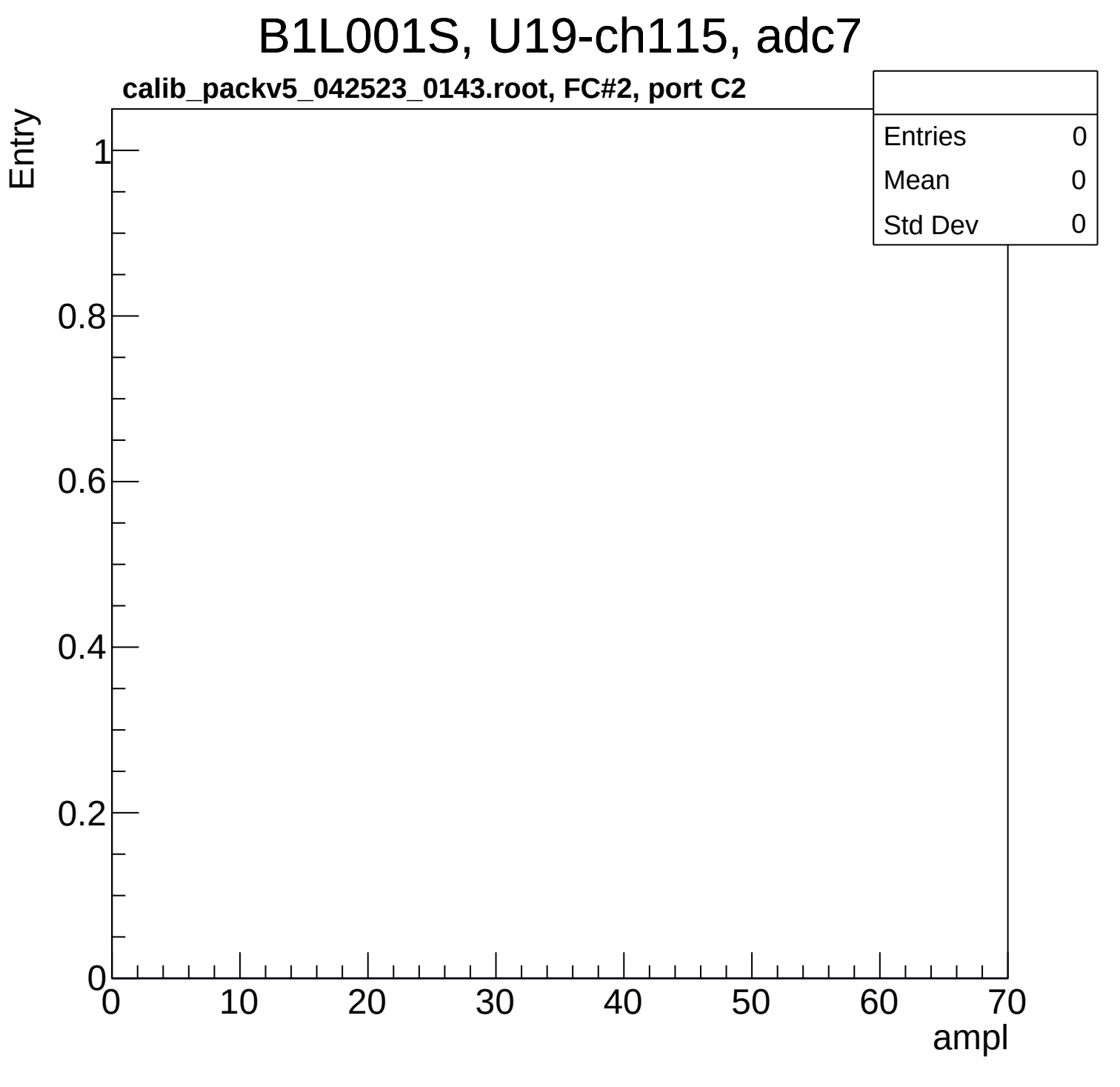
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L001S, U19-ch115, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 0
Mean 0
Std Dev 0
Entry
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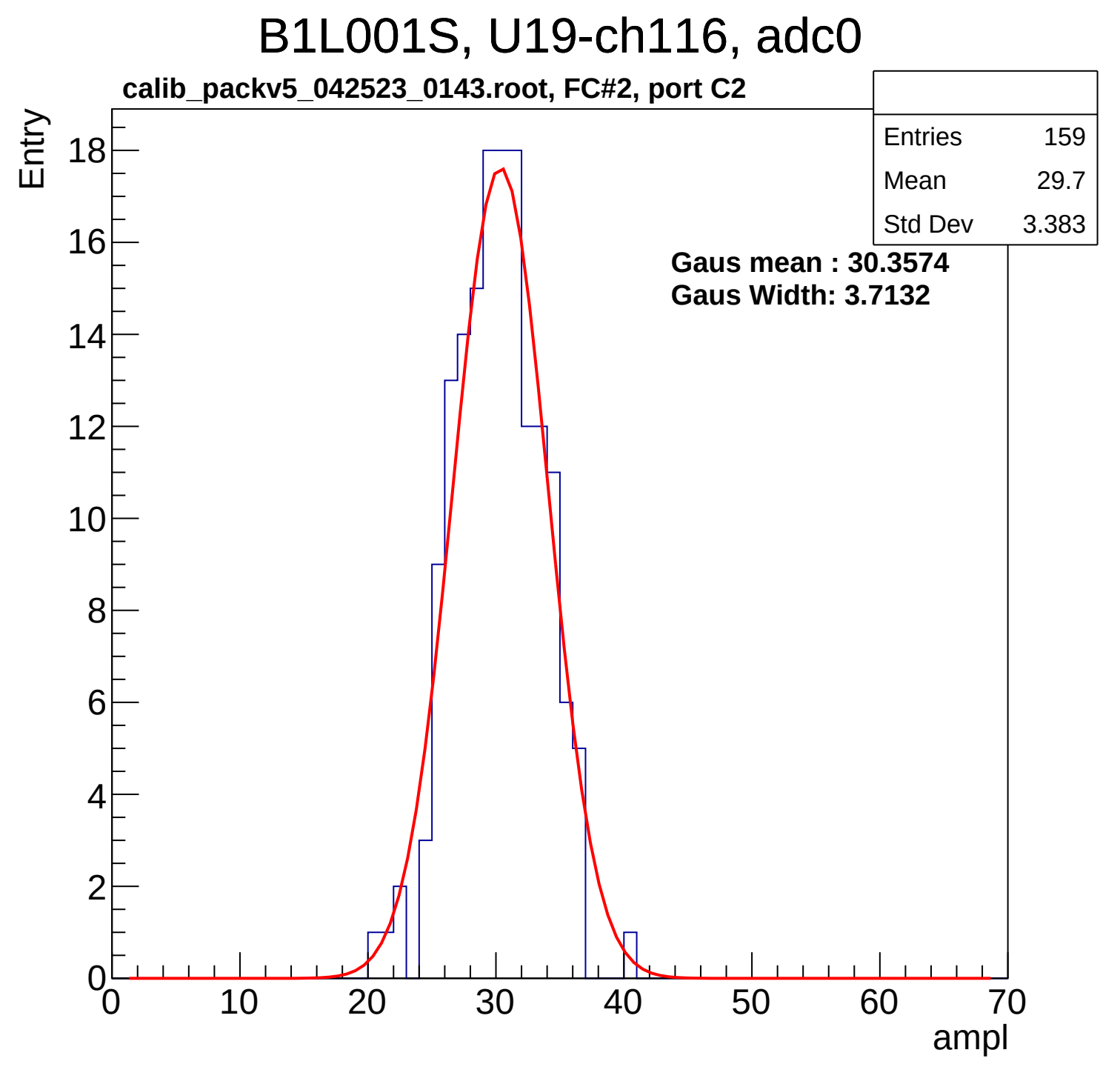
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch116, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 159
Mean 29.7
Std Dev 3.383
Gaus mean : 30.3574
Gaus Width: 3.7132
Entry
ampl
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2
4
6
8
10
12
14
16
18
0
10
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30
40
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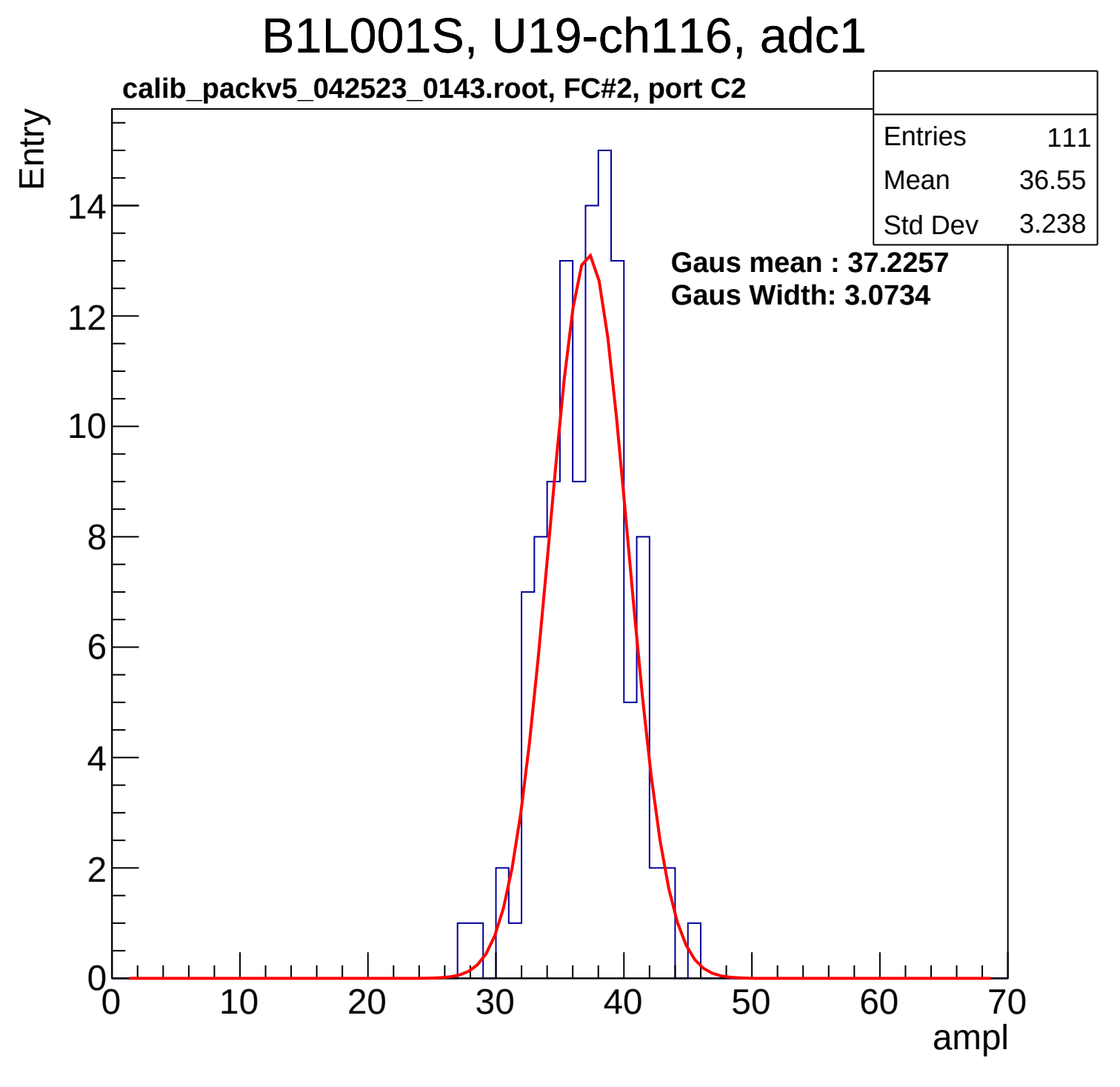
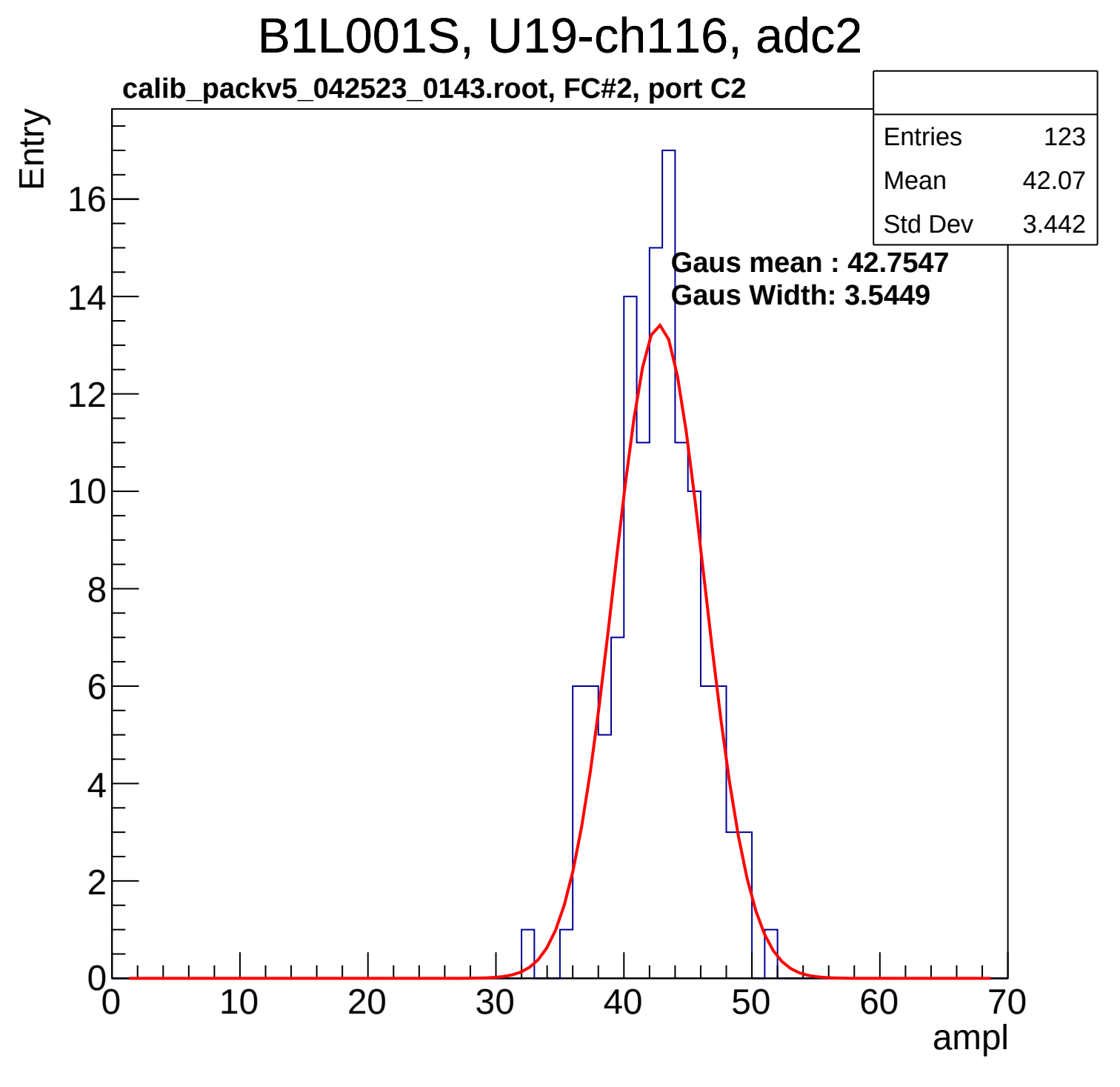
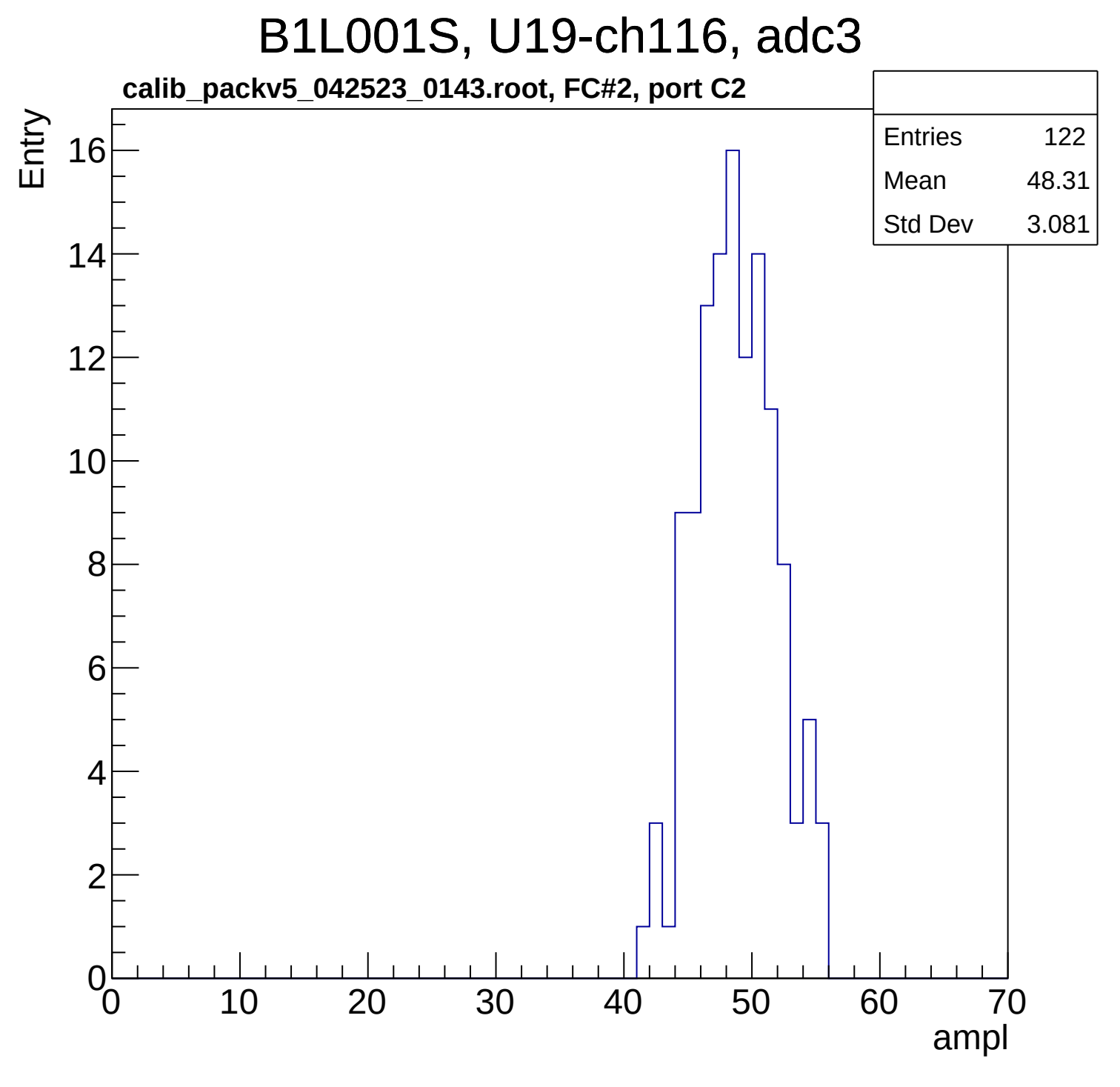
60
70


B1L001S, U19-ch116, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 111
Mean 36.55
Std Dev 3.238
Gaus mean : 37.2257
Gaus Width: 3.0734
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L001S, U19-ch116, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 123
Mean 42.07
Std Dev 3.442
Gaus mean : 42.7547
Gaus Width: 3.5449
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70


B1L001S, U19-ch116, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 122
Mean 48.31
Std Dev 3.081
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
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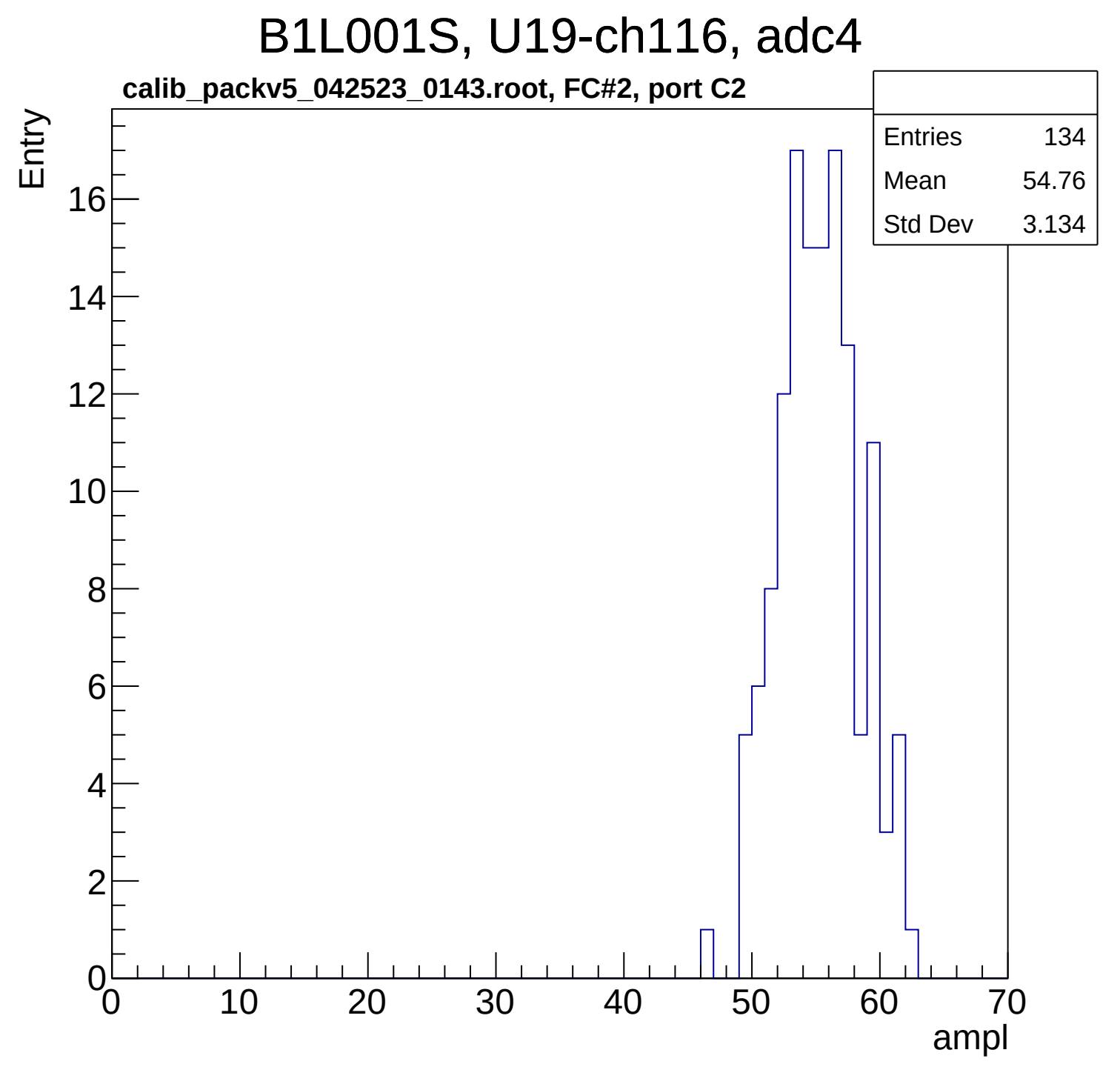
B1L001S, U19-ch116, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 134
Mean 54.76
Std Dev 3.134
Entry
ampl
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2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
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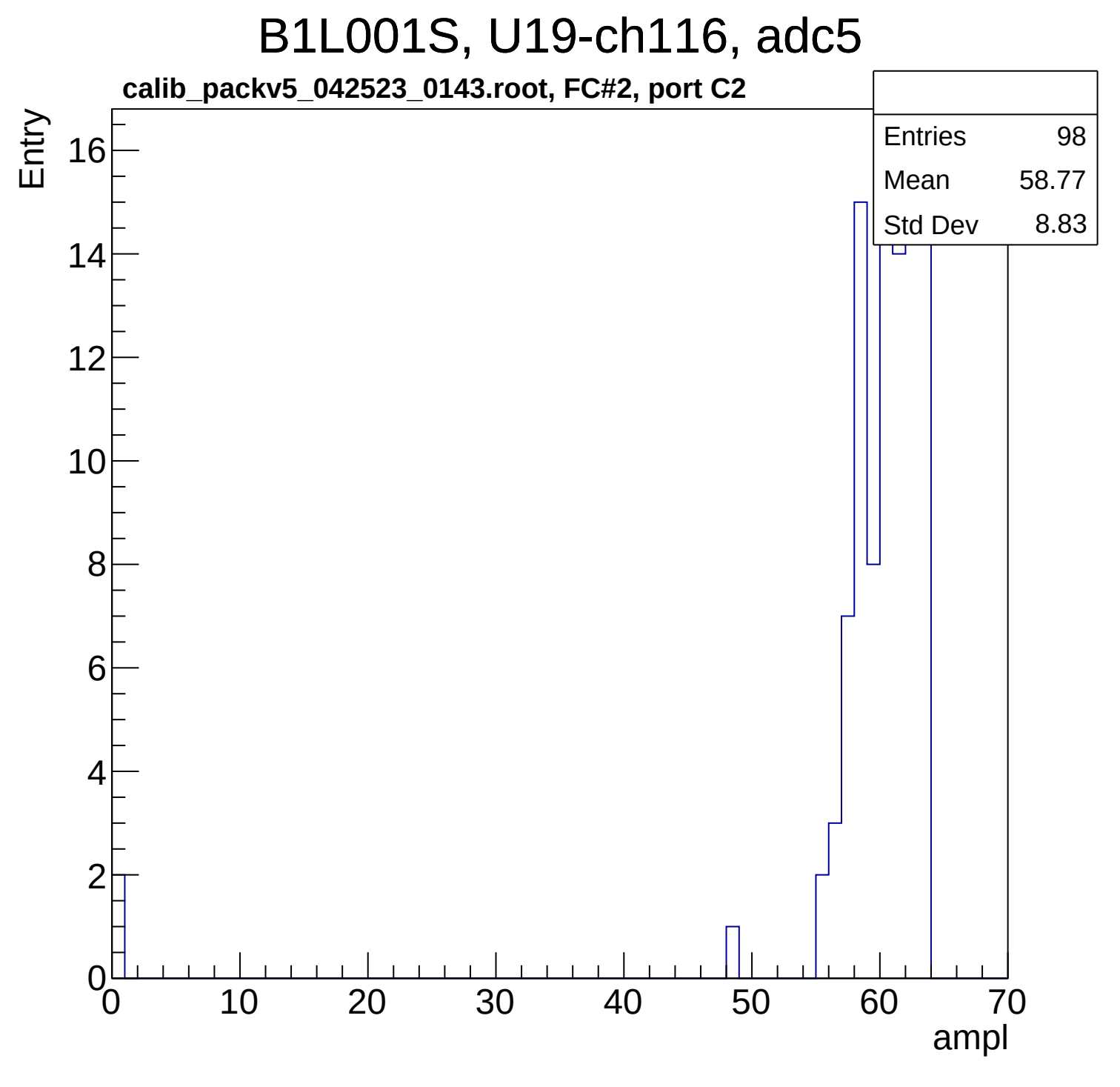
B1L001S, U19-ch116, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 98
Mean 58.77
Std Dev 8.83
Entry
ampl
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2
4
6
8
10
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0
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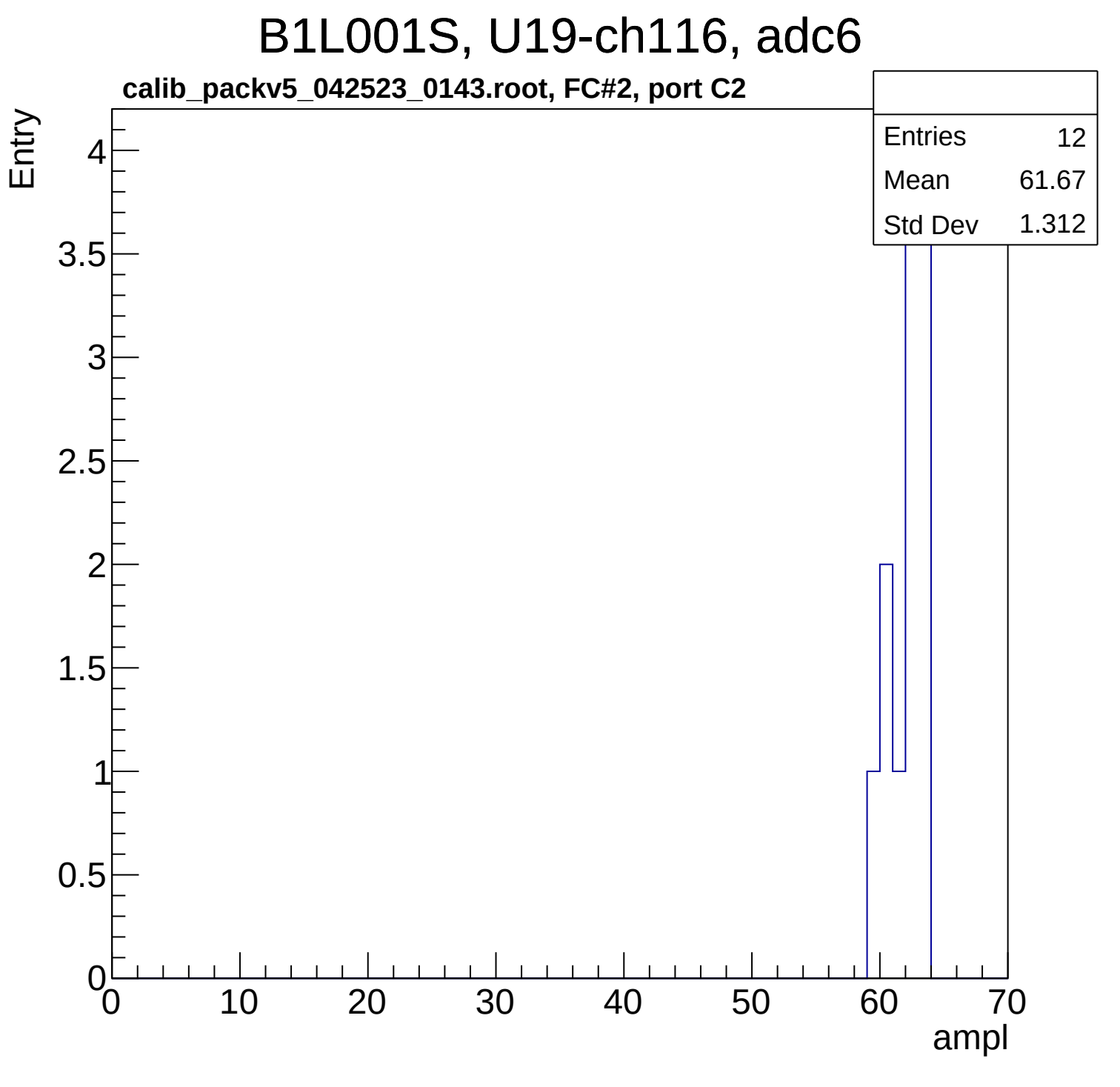
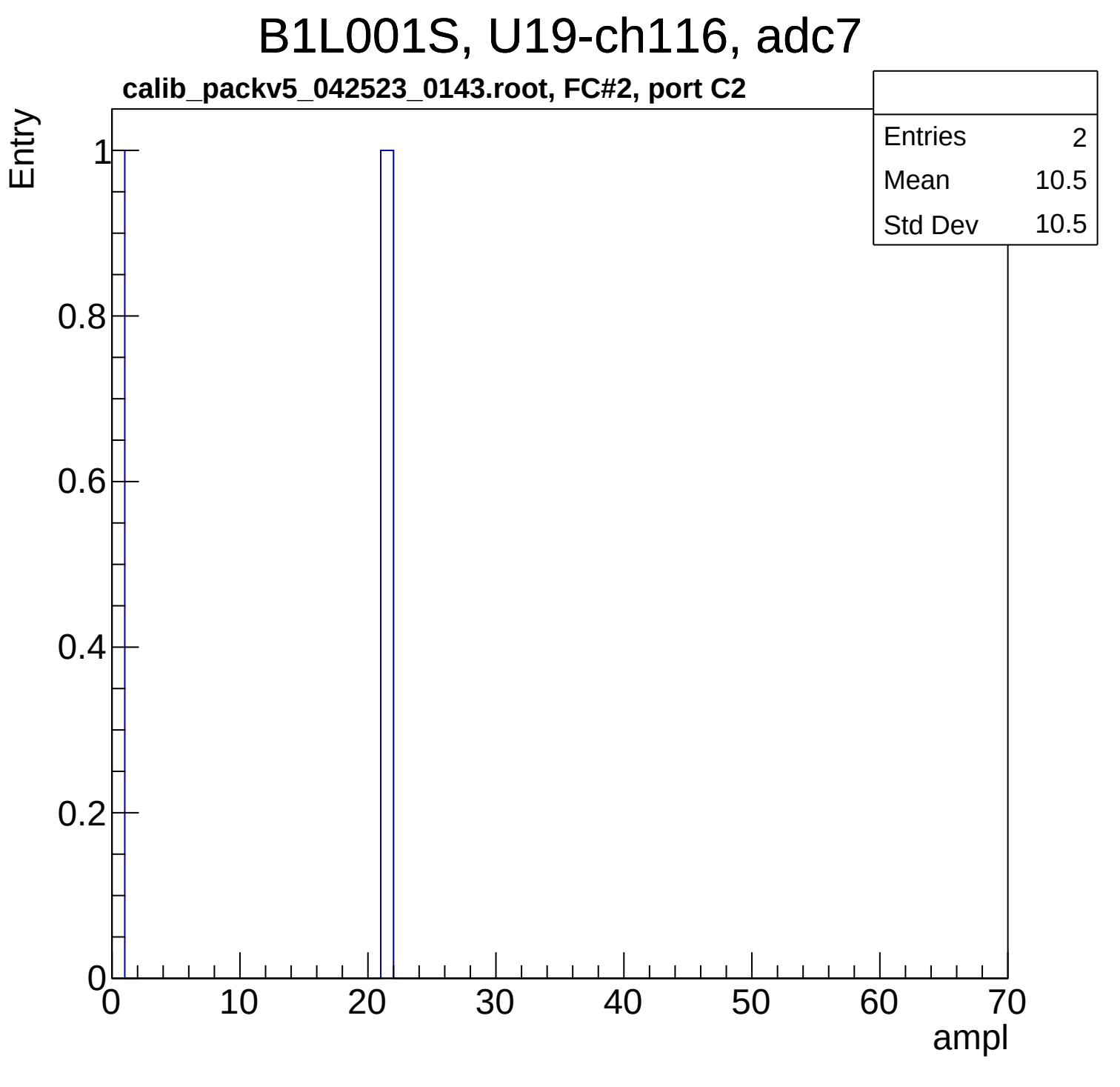
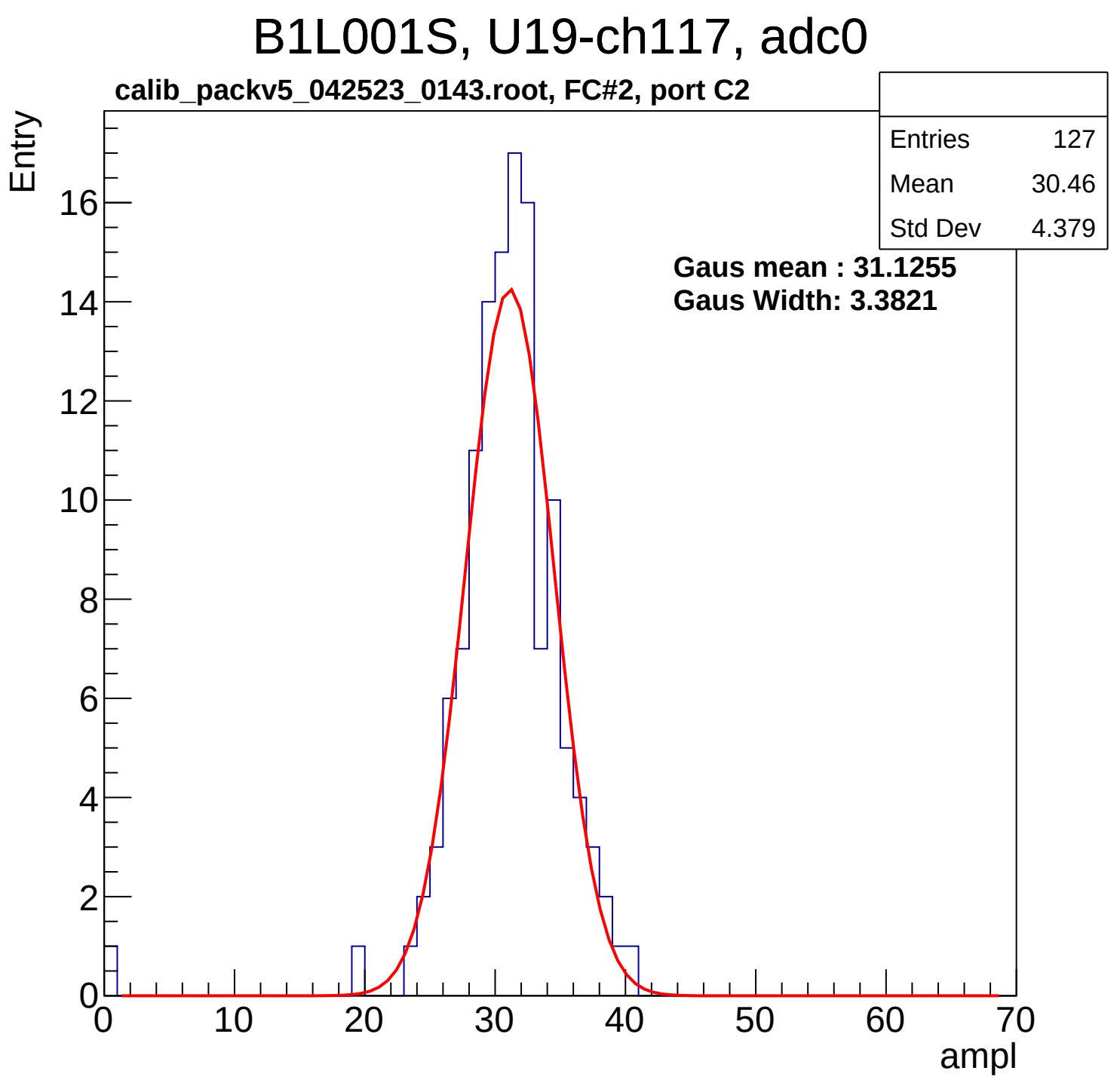
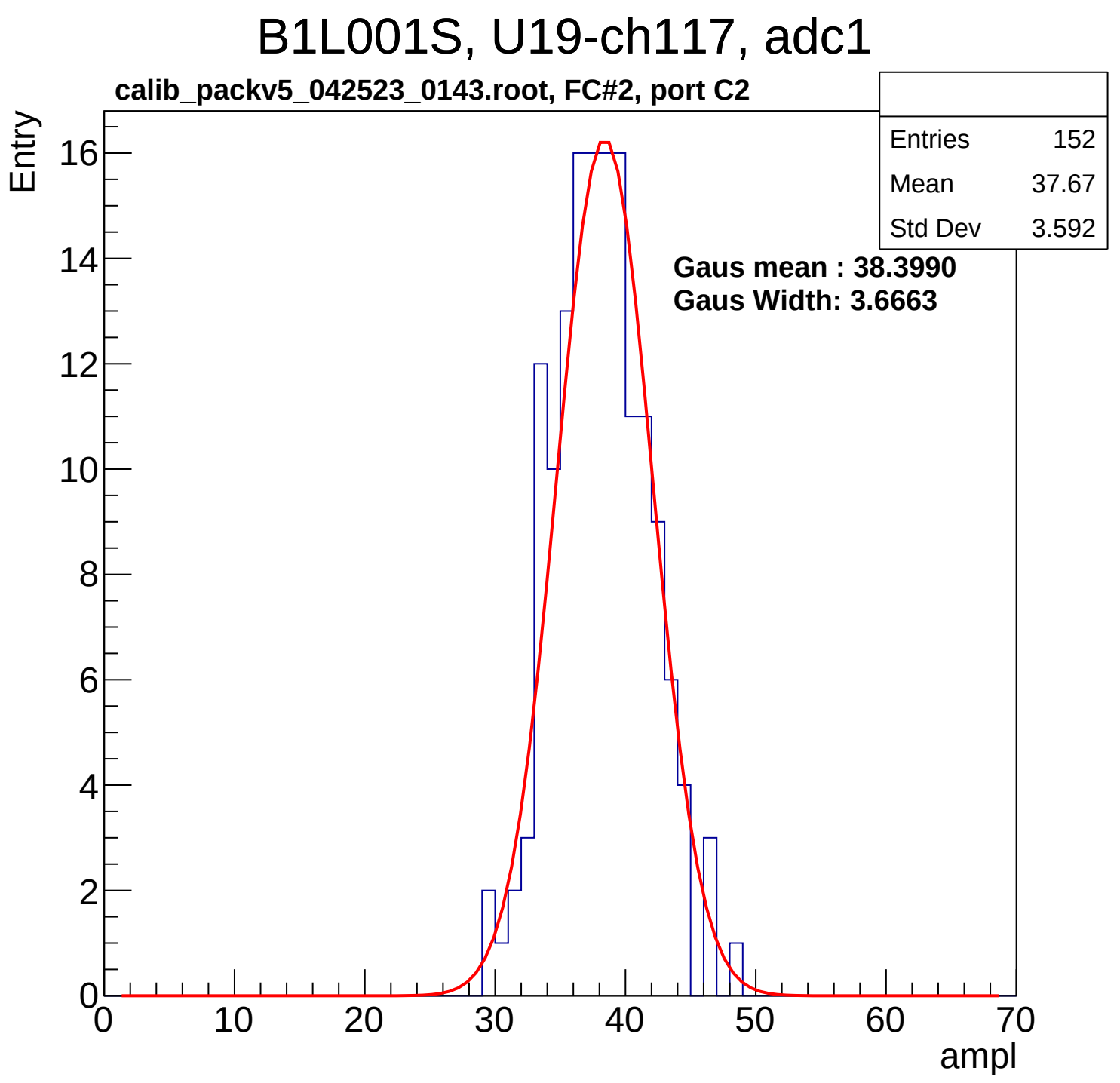
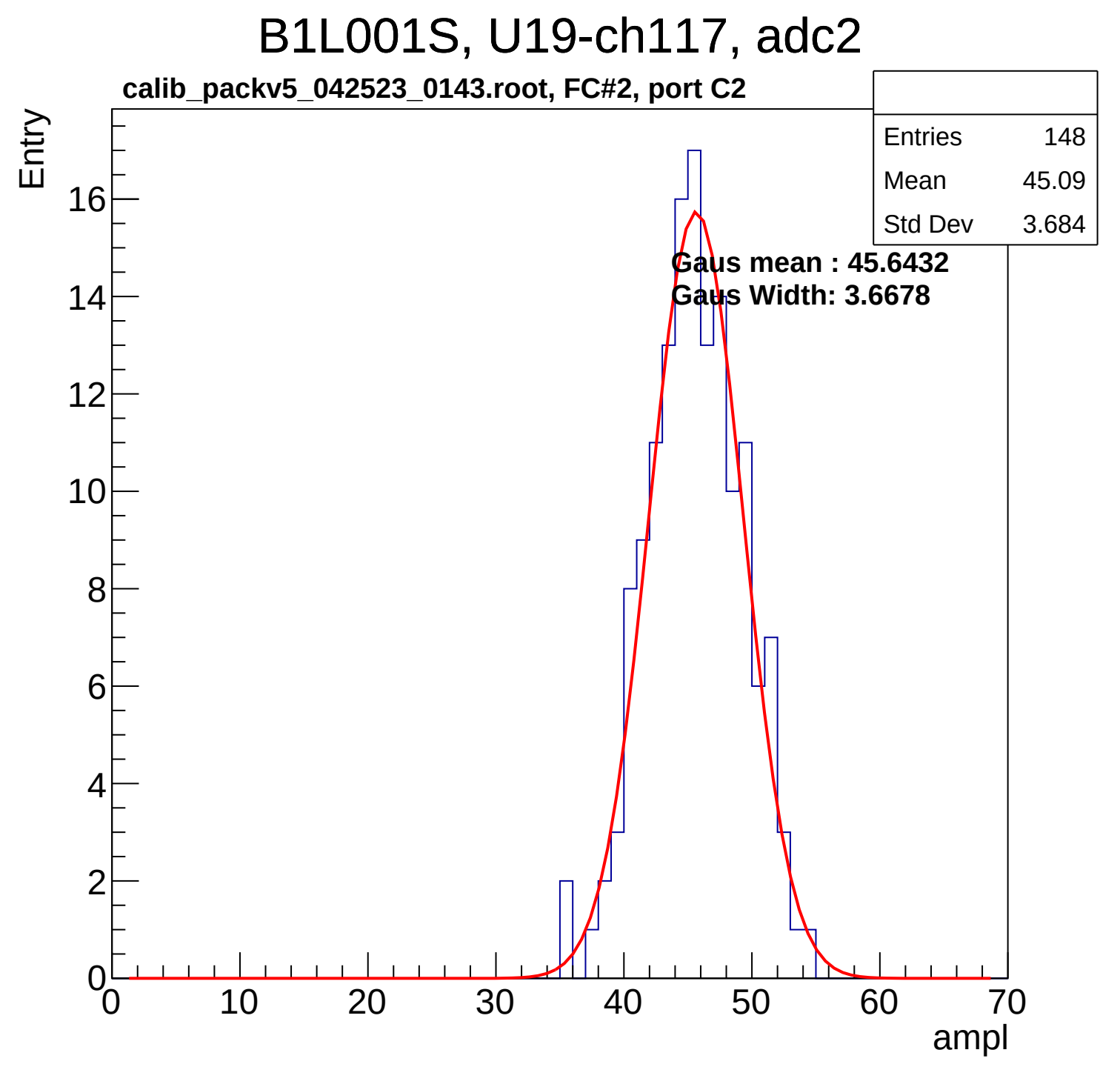
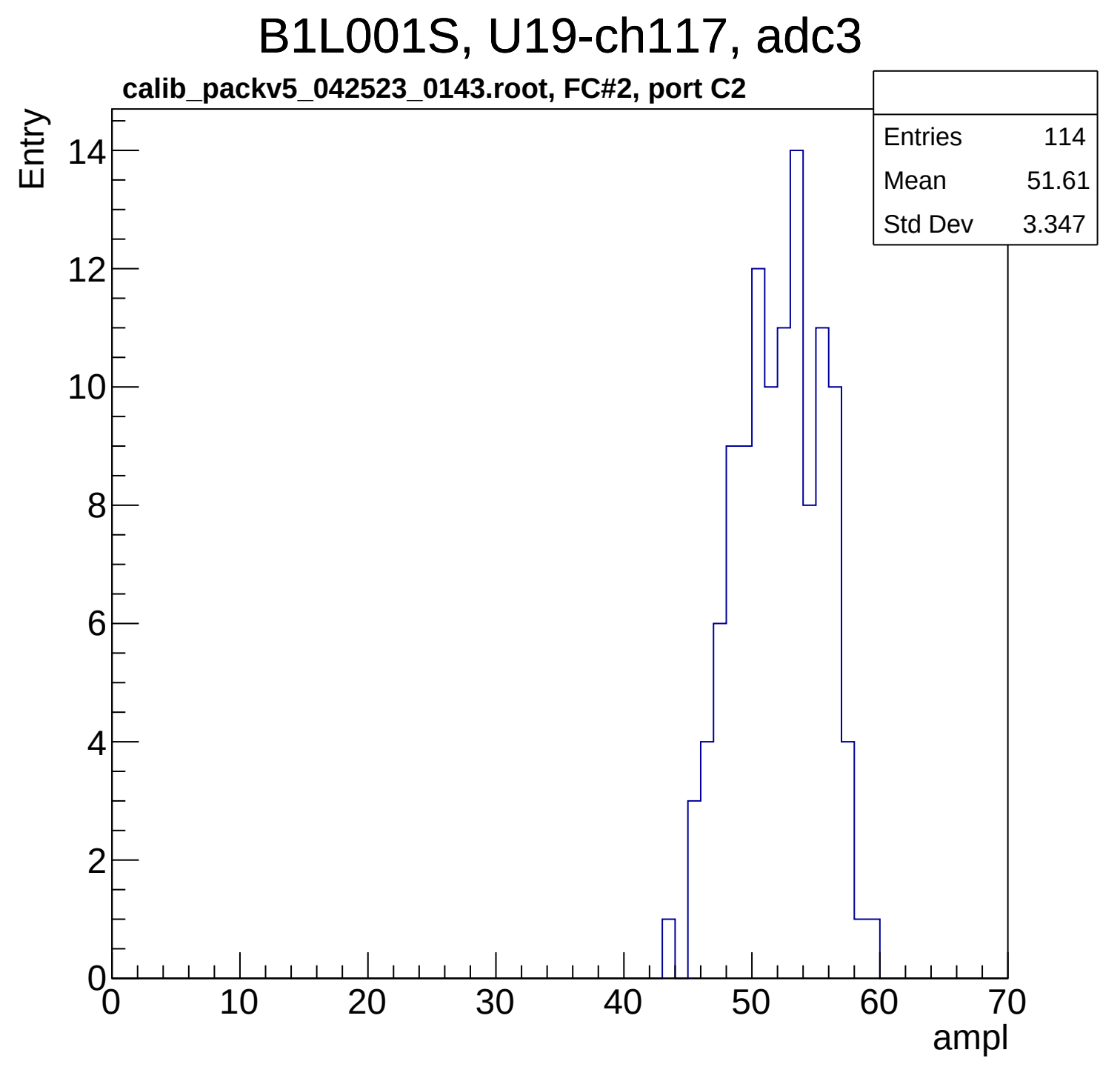

B1L001S, U19-ch116, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 12
Mean 61.67
Std Dev 1.312
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

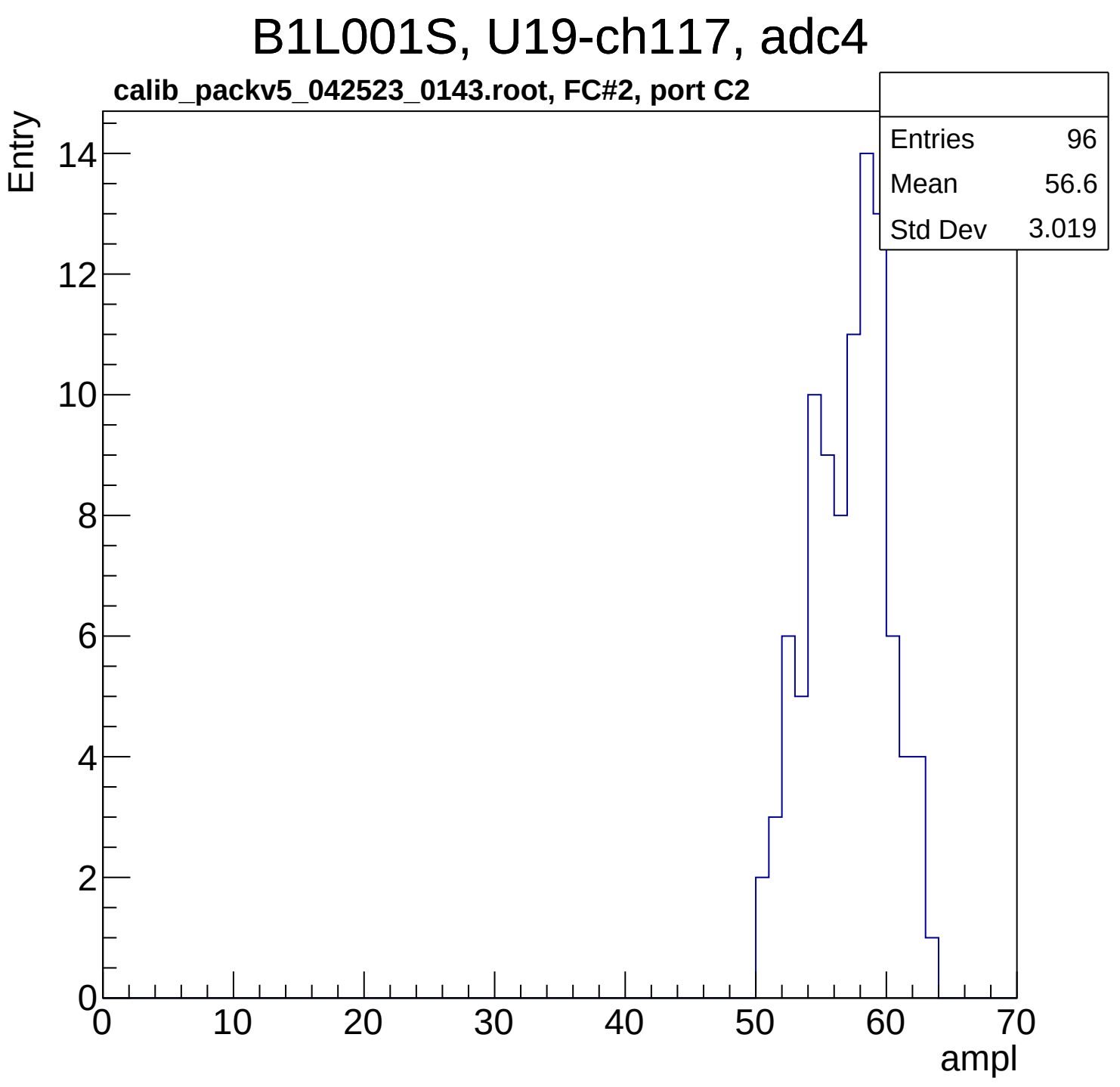

B1L001S, U19-ch116, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 10.5
Std Dev 10.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

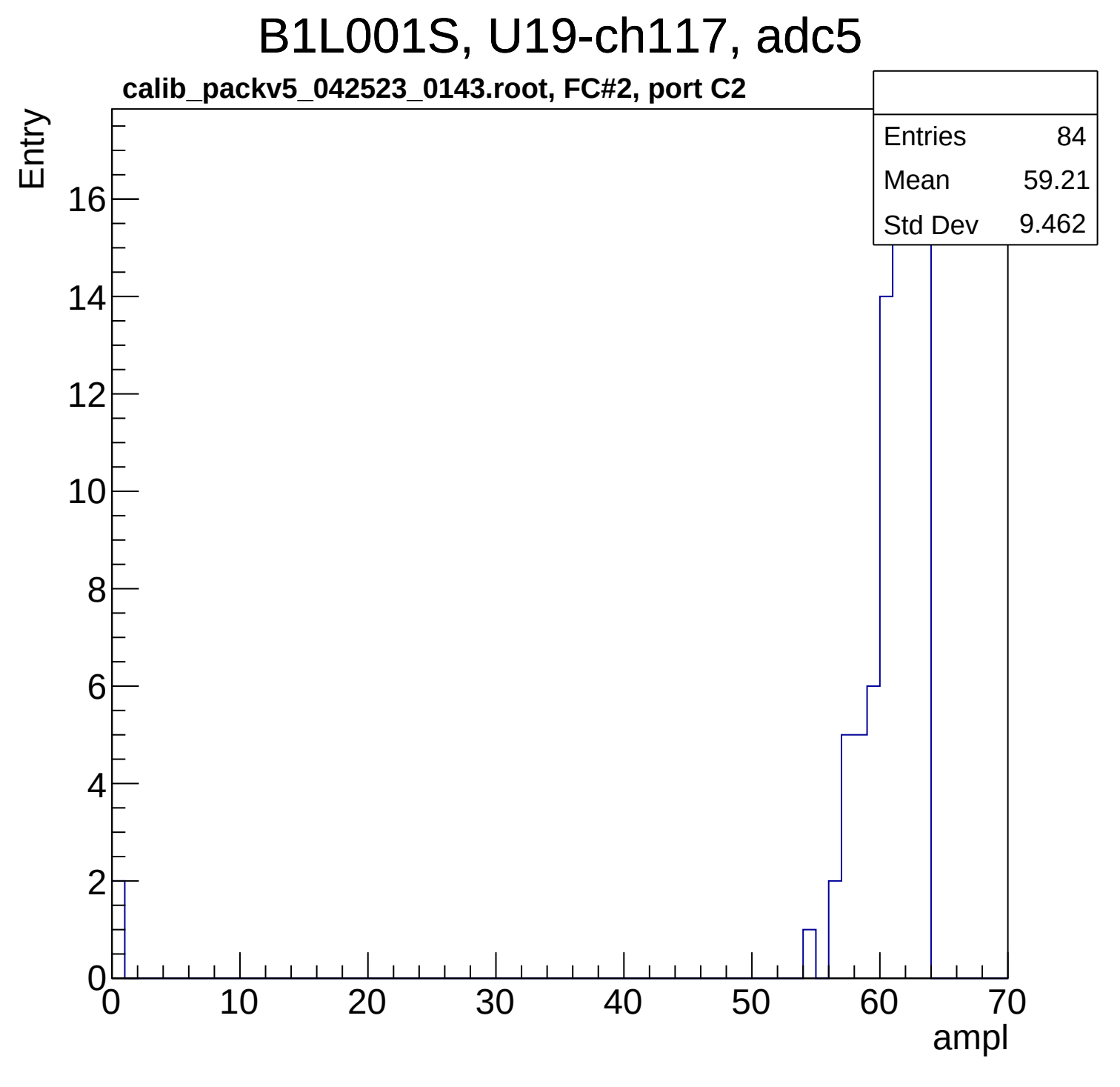

B1L001S, U19-ch117, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 127
Mean 30.46
Std Dev 4.379
Gaus mean : 31.1255
Gaus Width: 3.3821
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70


B1L001S, U19-ch117, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 152
Mean 37.67
Std Dev 3.592
Gaus mean : 38.3990
Gaus Width: 3.6663
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70


B1L001S, U19-ch117, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 148
Mean 45.09
Std Dev 3.684
Gaus mean : 45.6432
Gaus Width: 3.6678
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70


B1L001S, U19-ch117, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 114
Mean 51.61
Std Dev 3.347
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L001S, U19-ch117, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 96
Mean 56.6
Std Dev 3.019
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch117, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 84
Mean 59.21
Std Dev 9.462
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
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40
50
60
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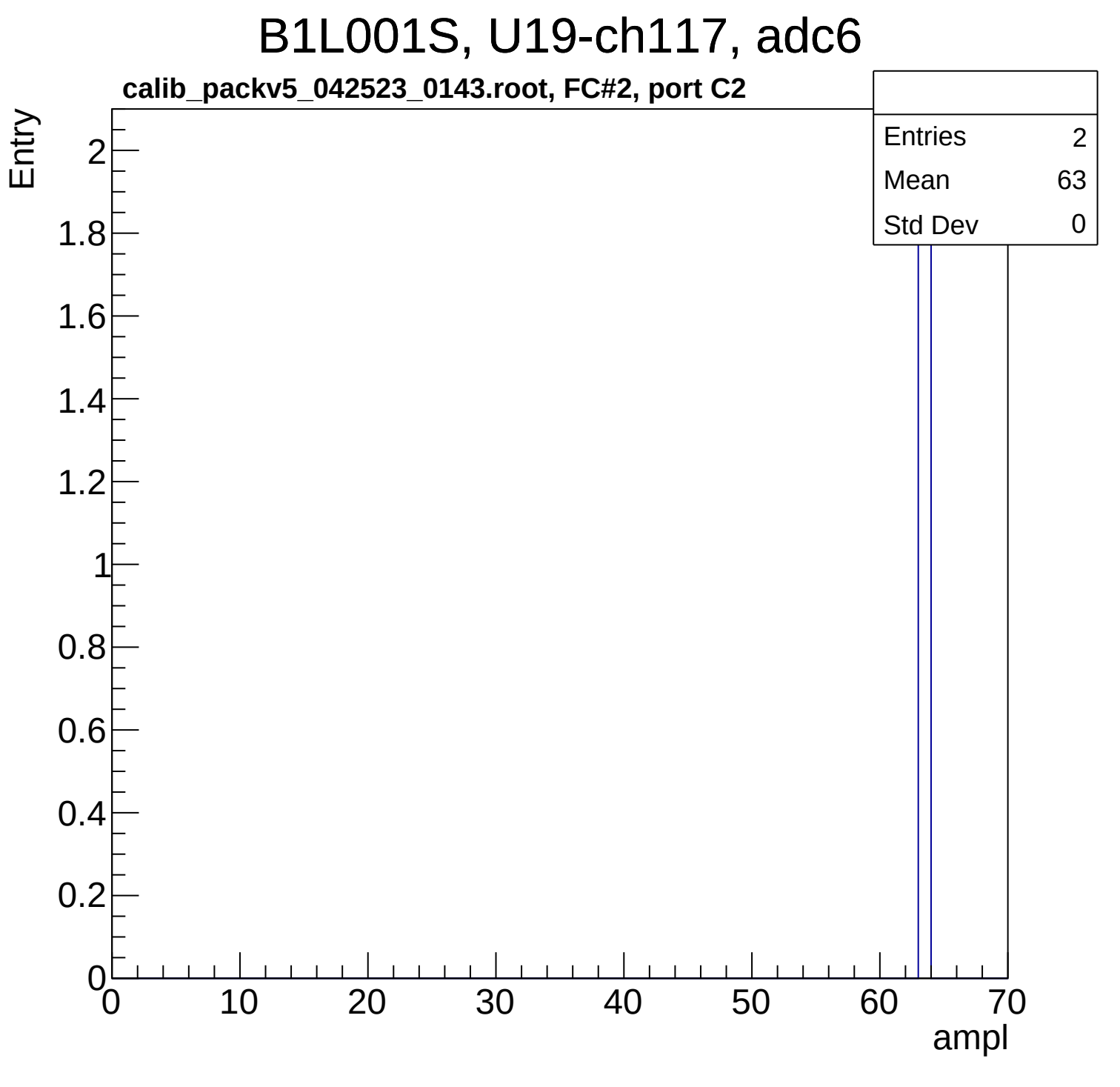
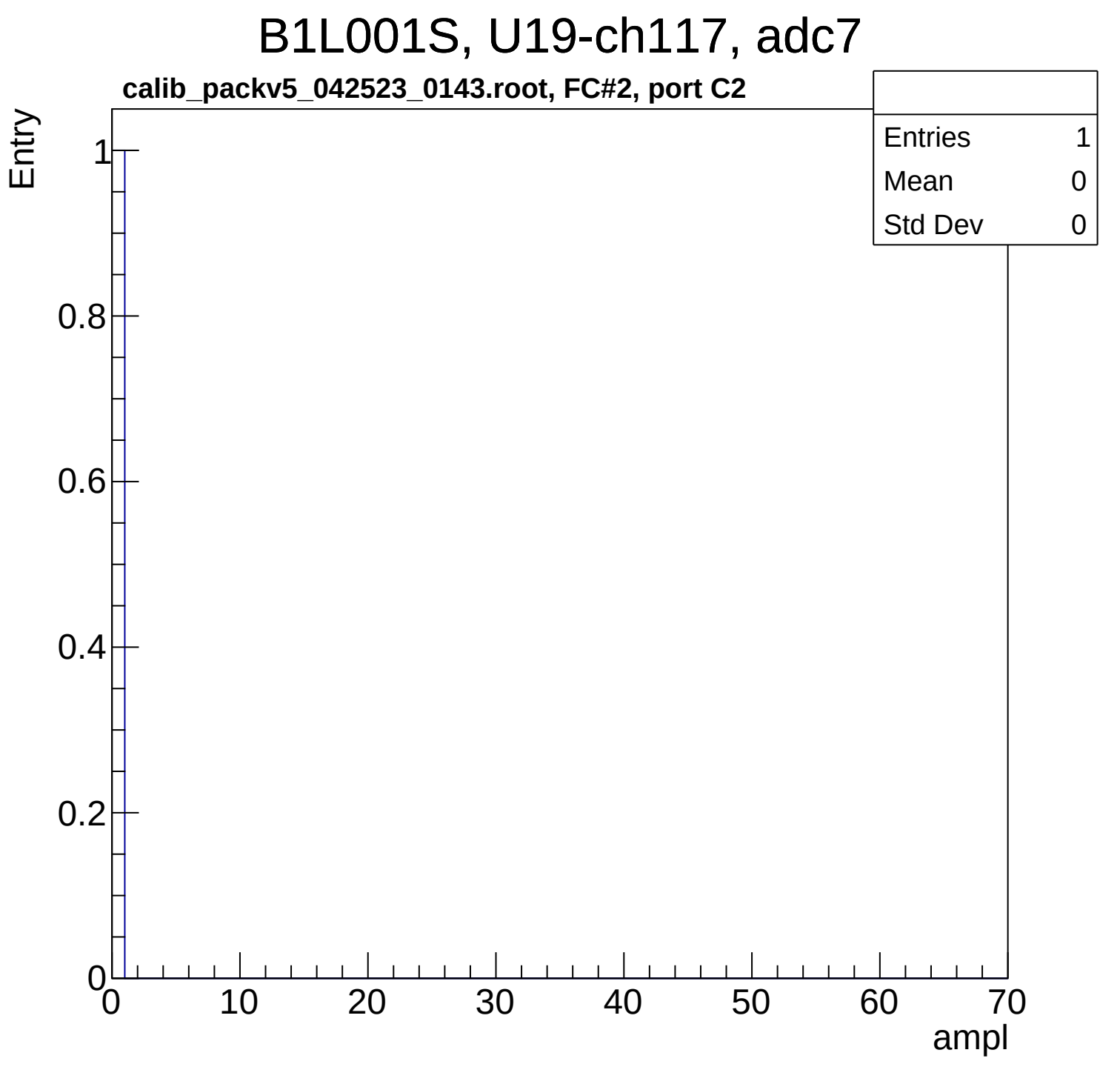
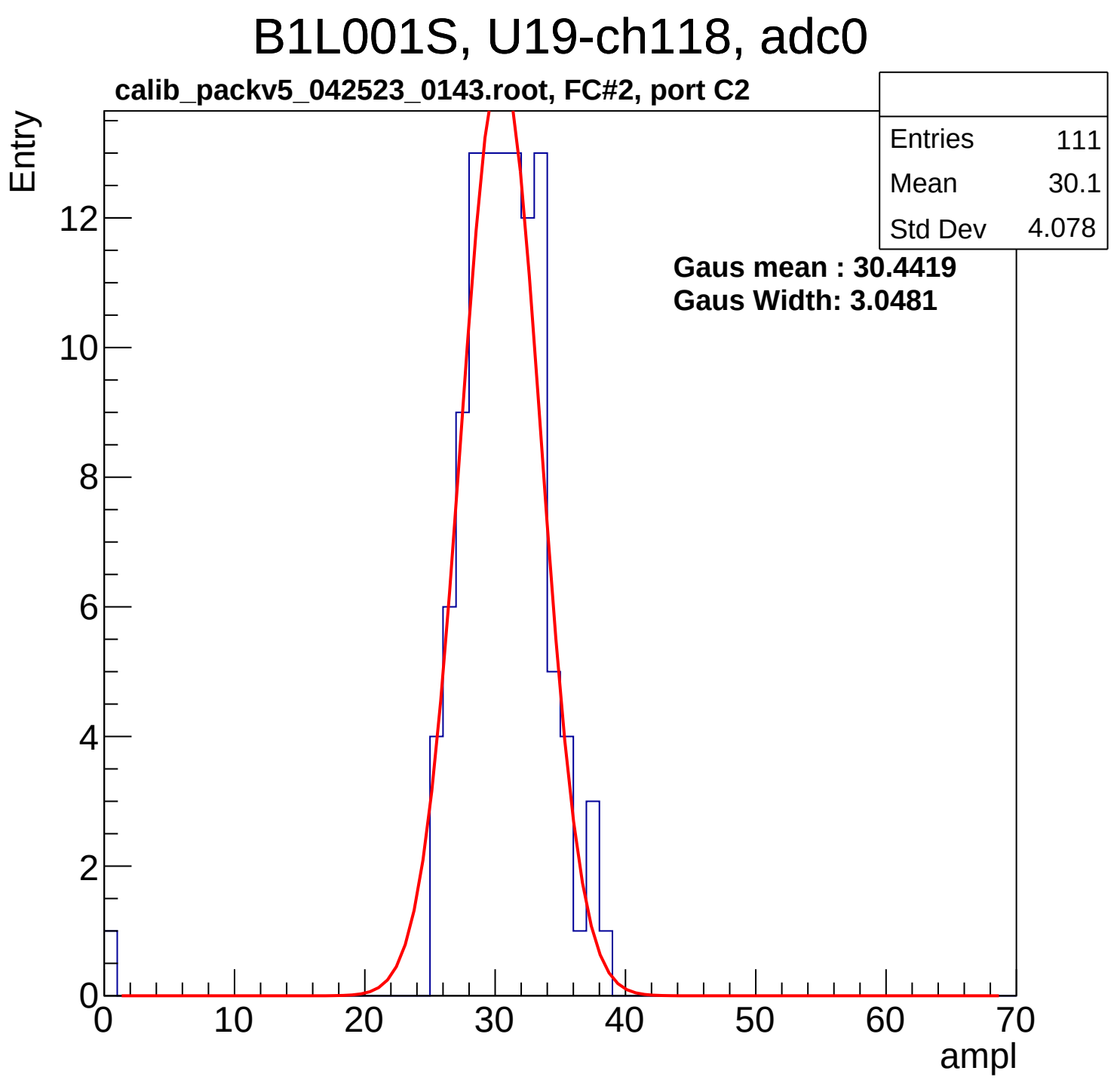
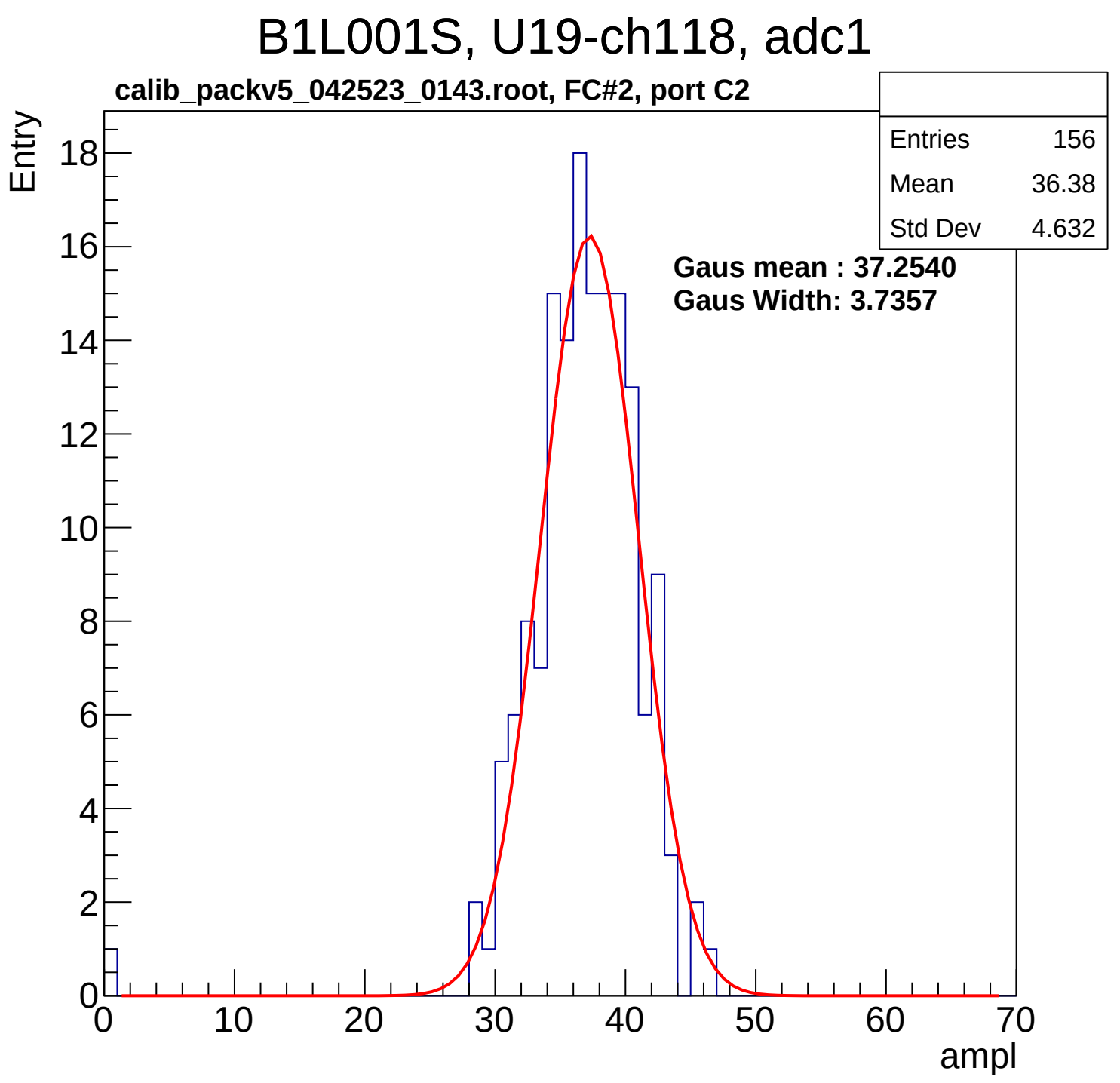
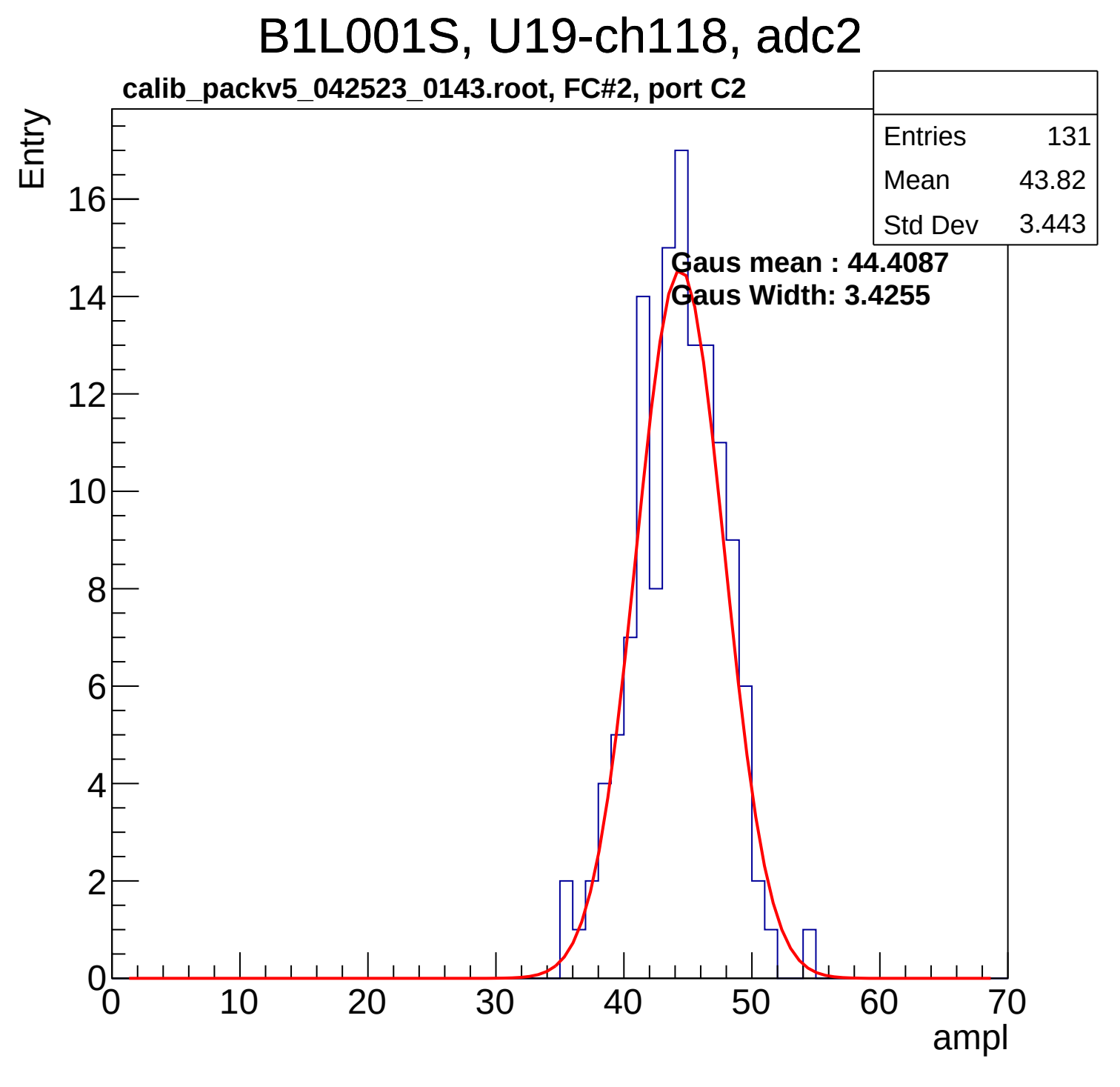
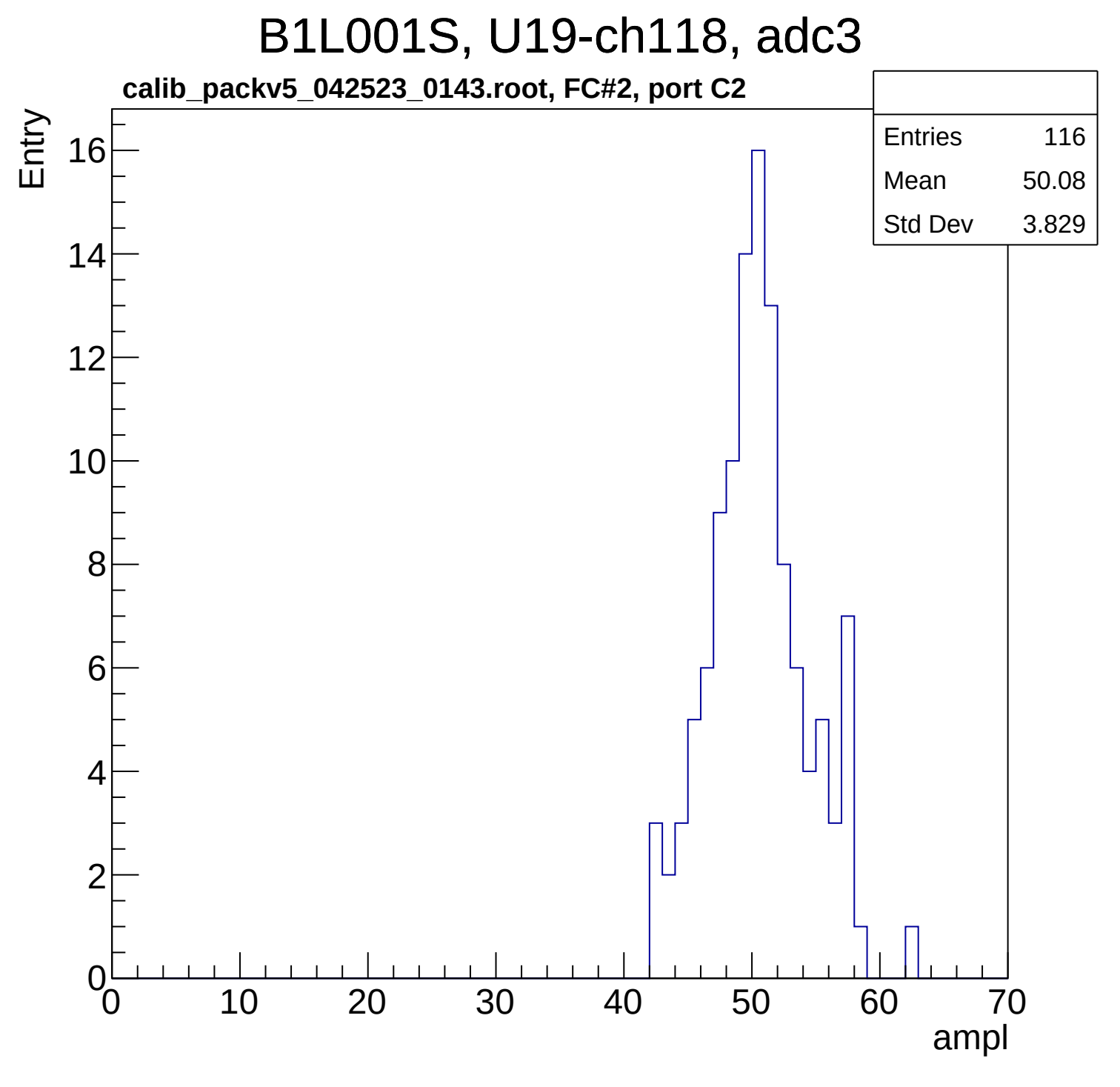

B1L001S, U19-ch117, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 63
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L001S, U19-ch117, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch118, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 111
Mean 30.1
Std Dev 4.078
Gaus mean : 30.4419
Gaus Width: 3.0481
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70


B1L001S, U19-ch118, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 156
Mean 36.38
Std Dev 4.632
Gaus mean : 37.2540
Gaus Width: 3.7357
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70


B1L001S, U19-ch118, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 131
Mean 43.82
Std Dev 3.443
Gaus mean : 44.4087
Gaus Width: 3.4255
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70


B1L001S, U19-ch118, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 116
Mean 50.08
Std Dev 3.829
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
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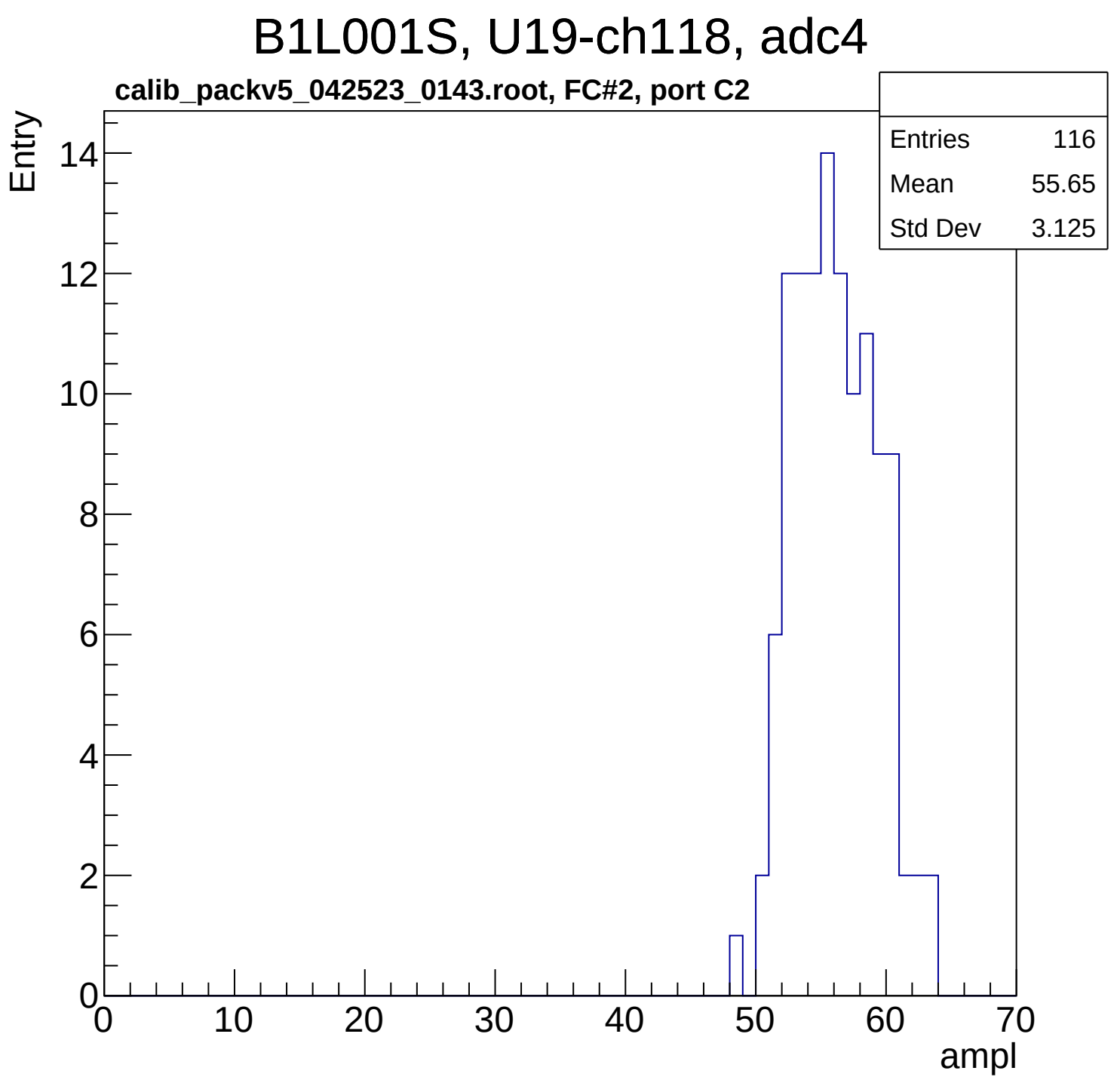
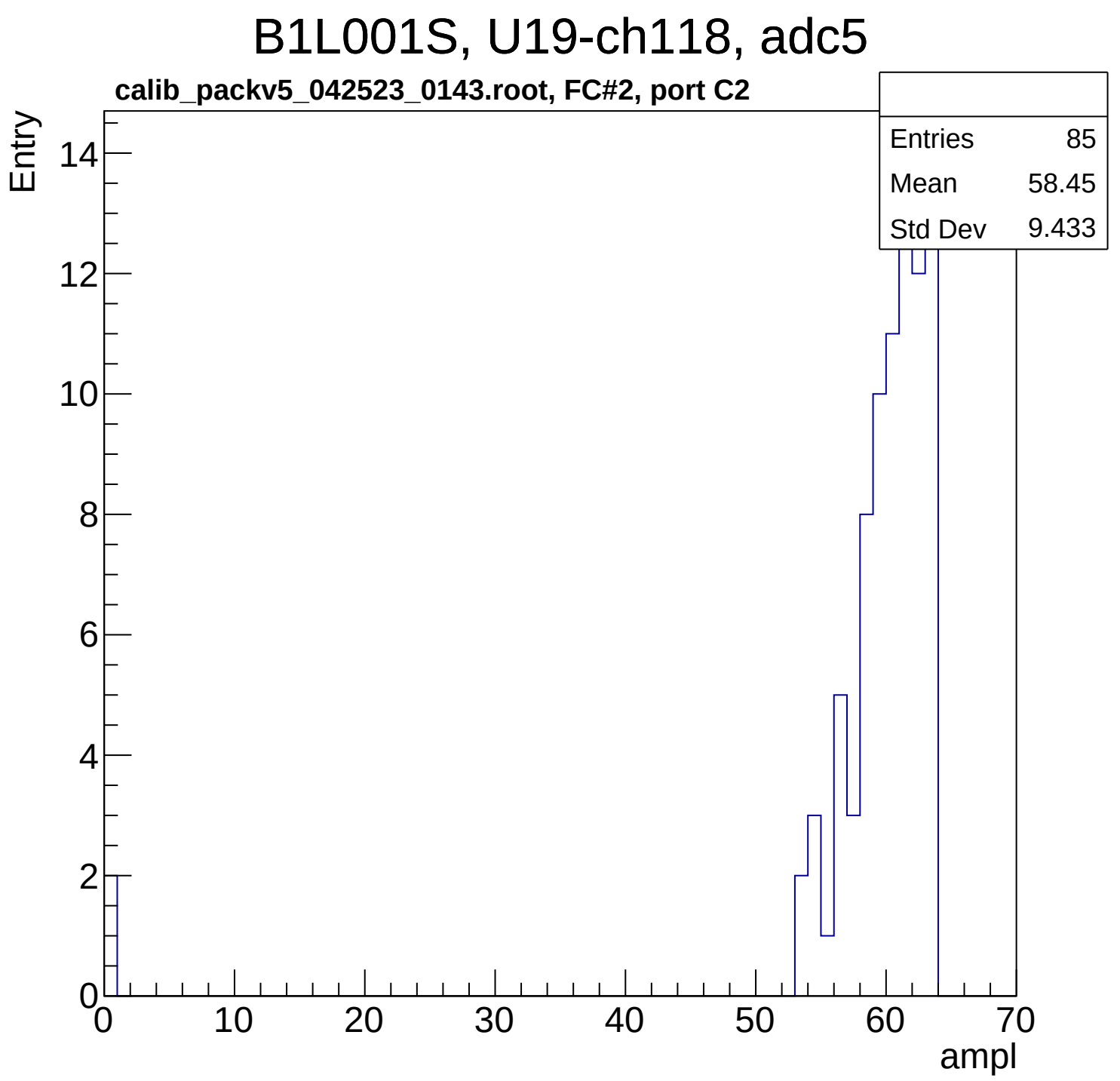

B1L001S, U19-ch118, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 116
Mean 55.65
Std Dev 3.125
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L001S, U19-ch118, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 85
Mean 58.45
Std Dev 9.433
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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40
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60
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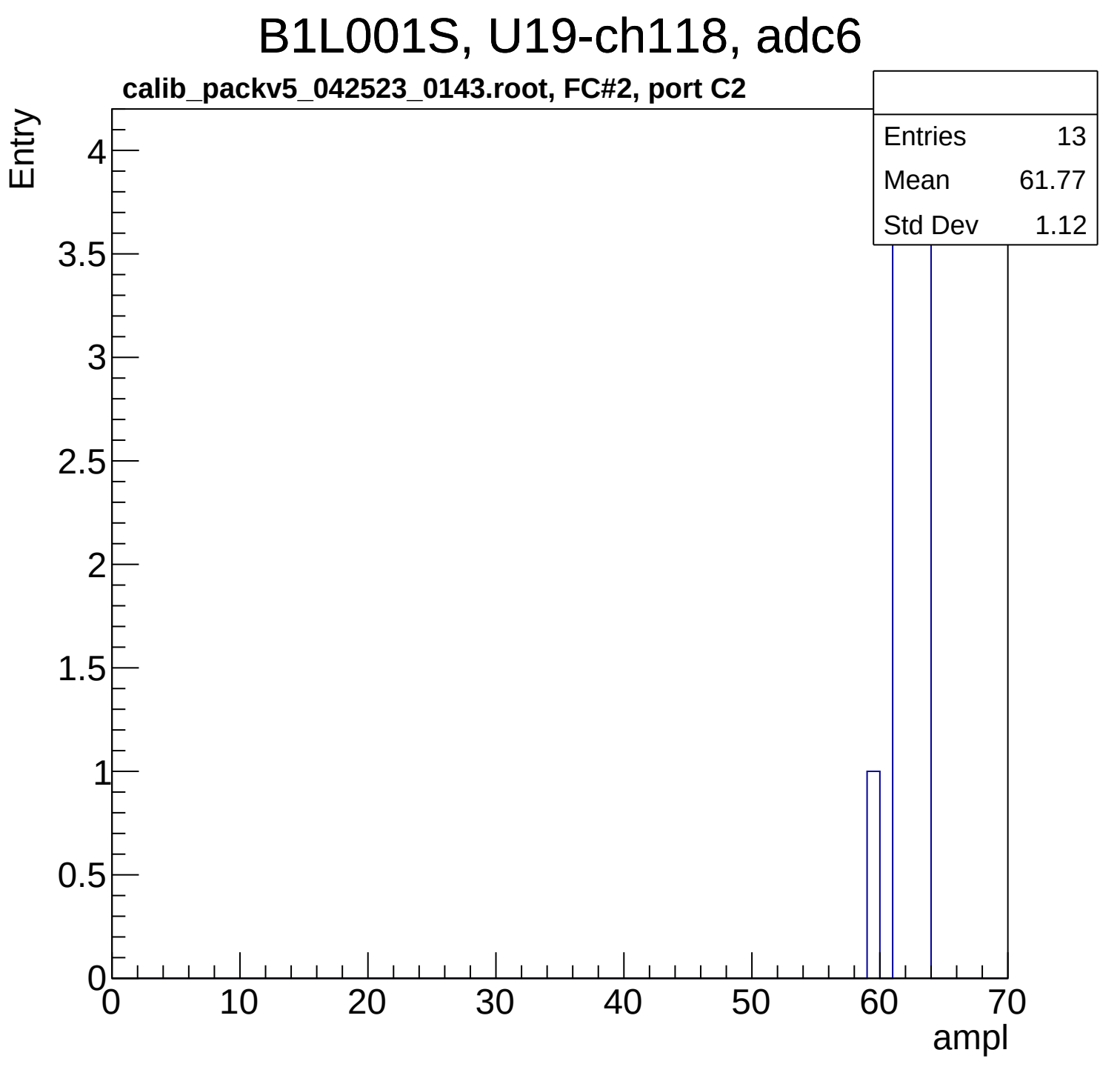
B1L001S, U19-ch118, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 13
Mean 61.77
Std Dev 1.12
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
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40
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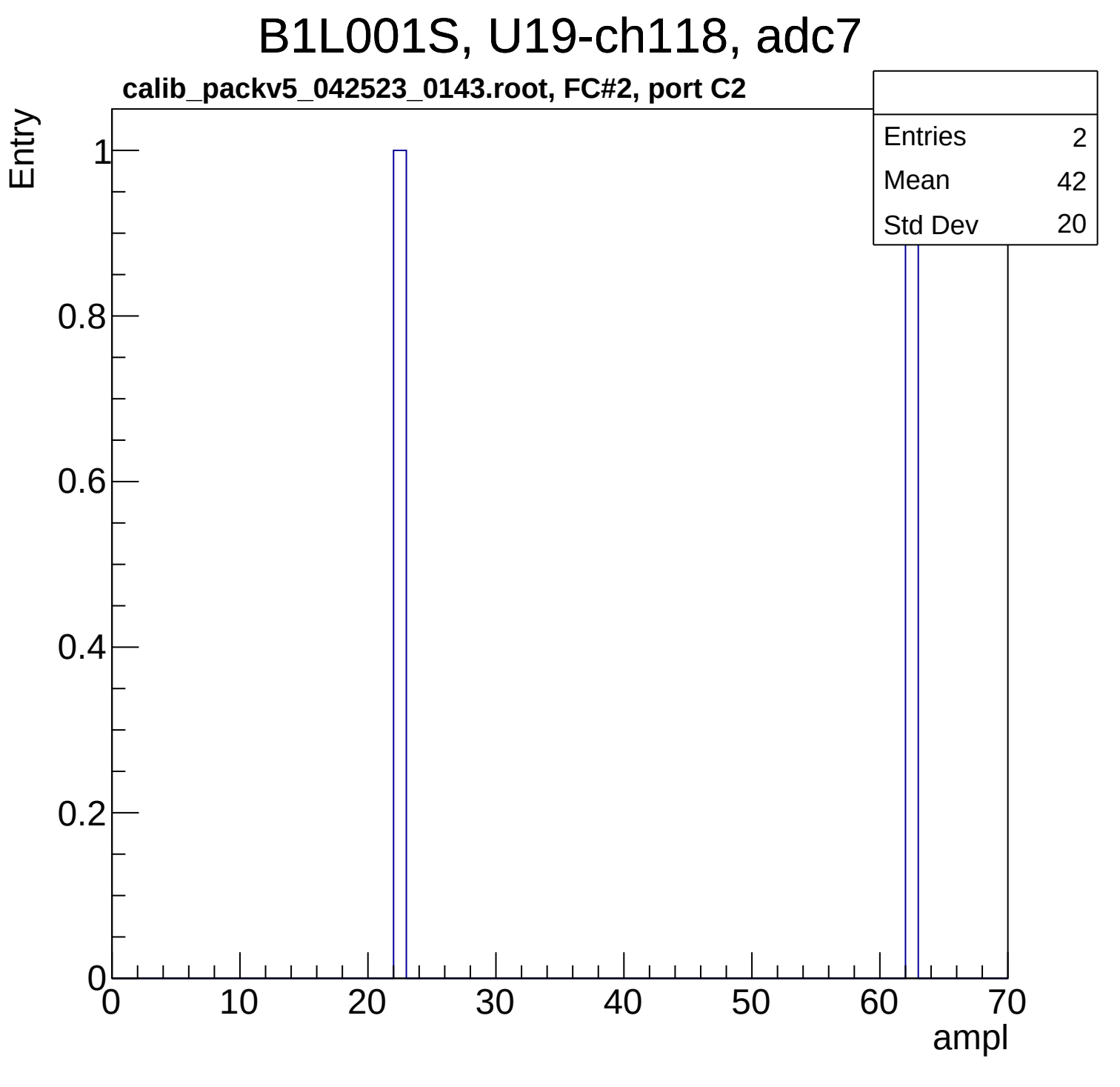
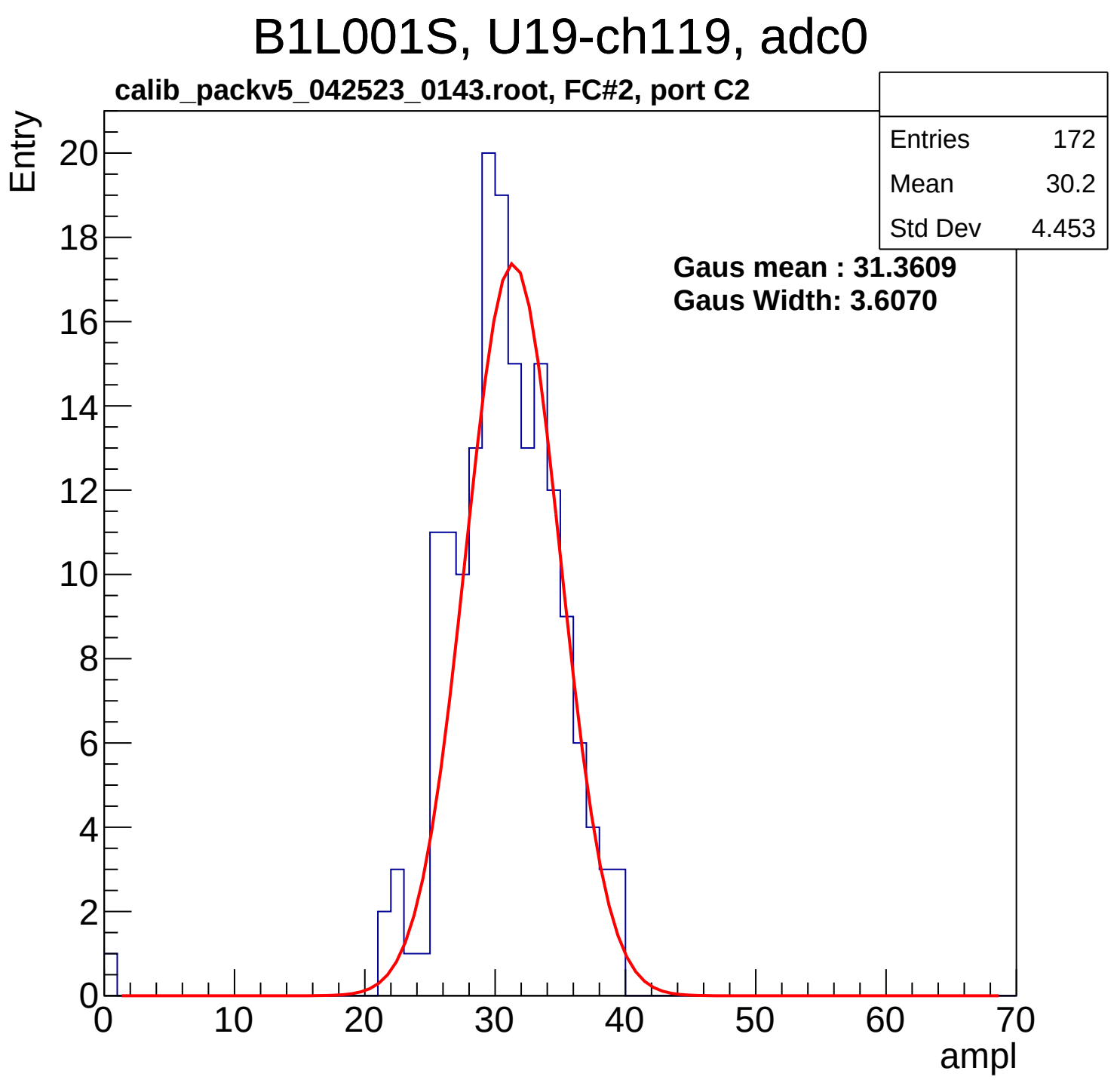
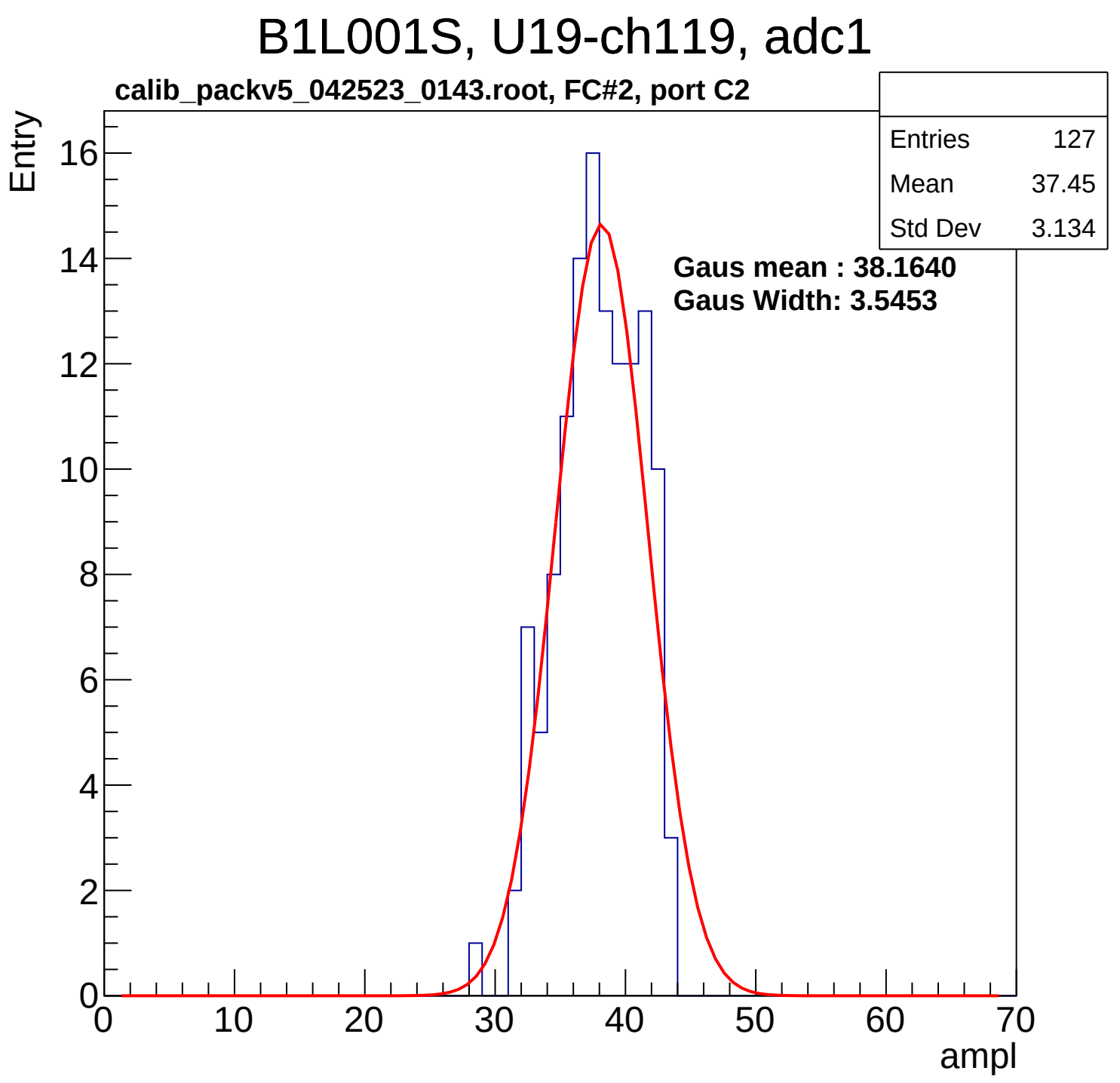
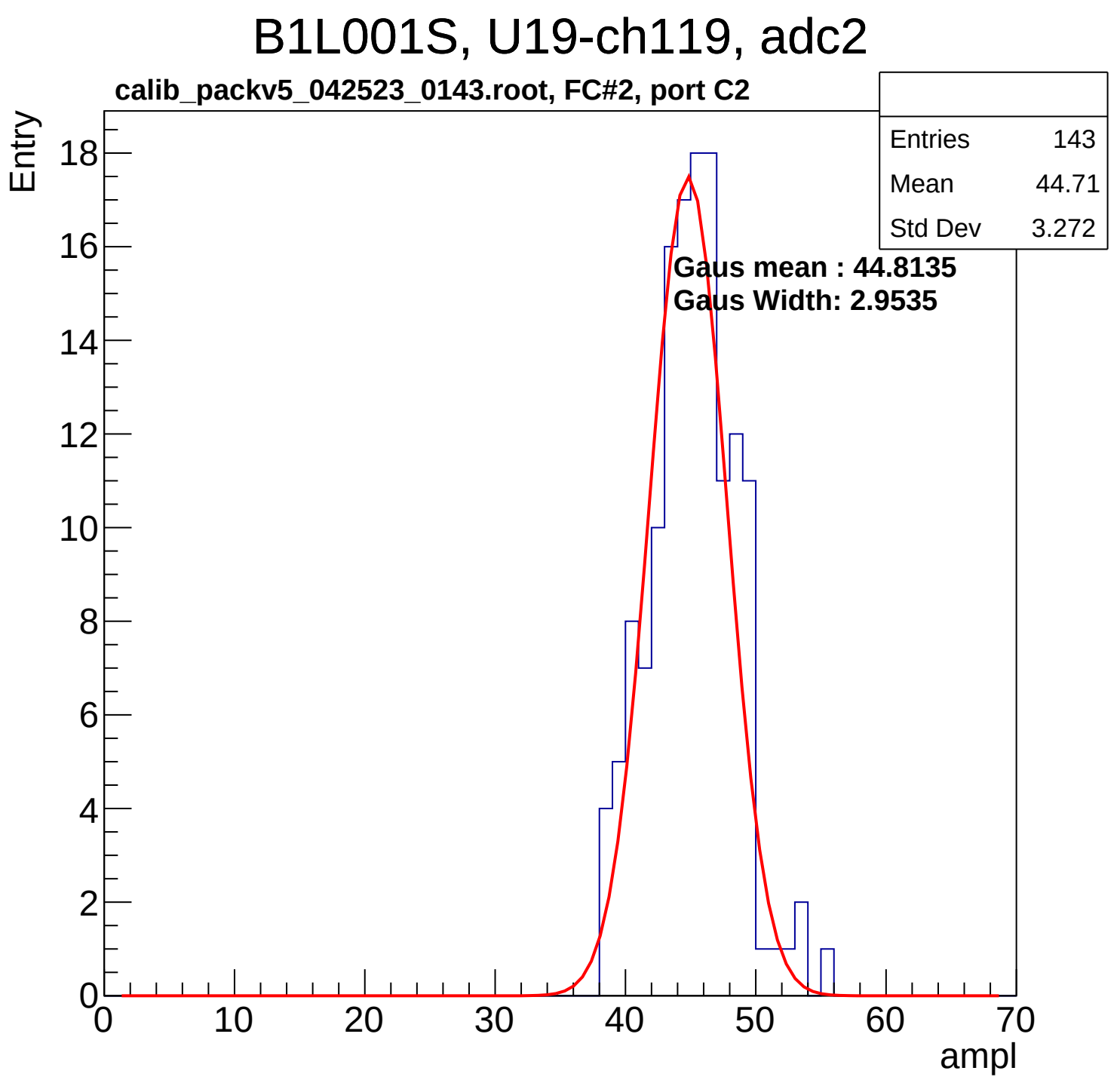
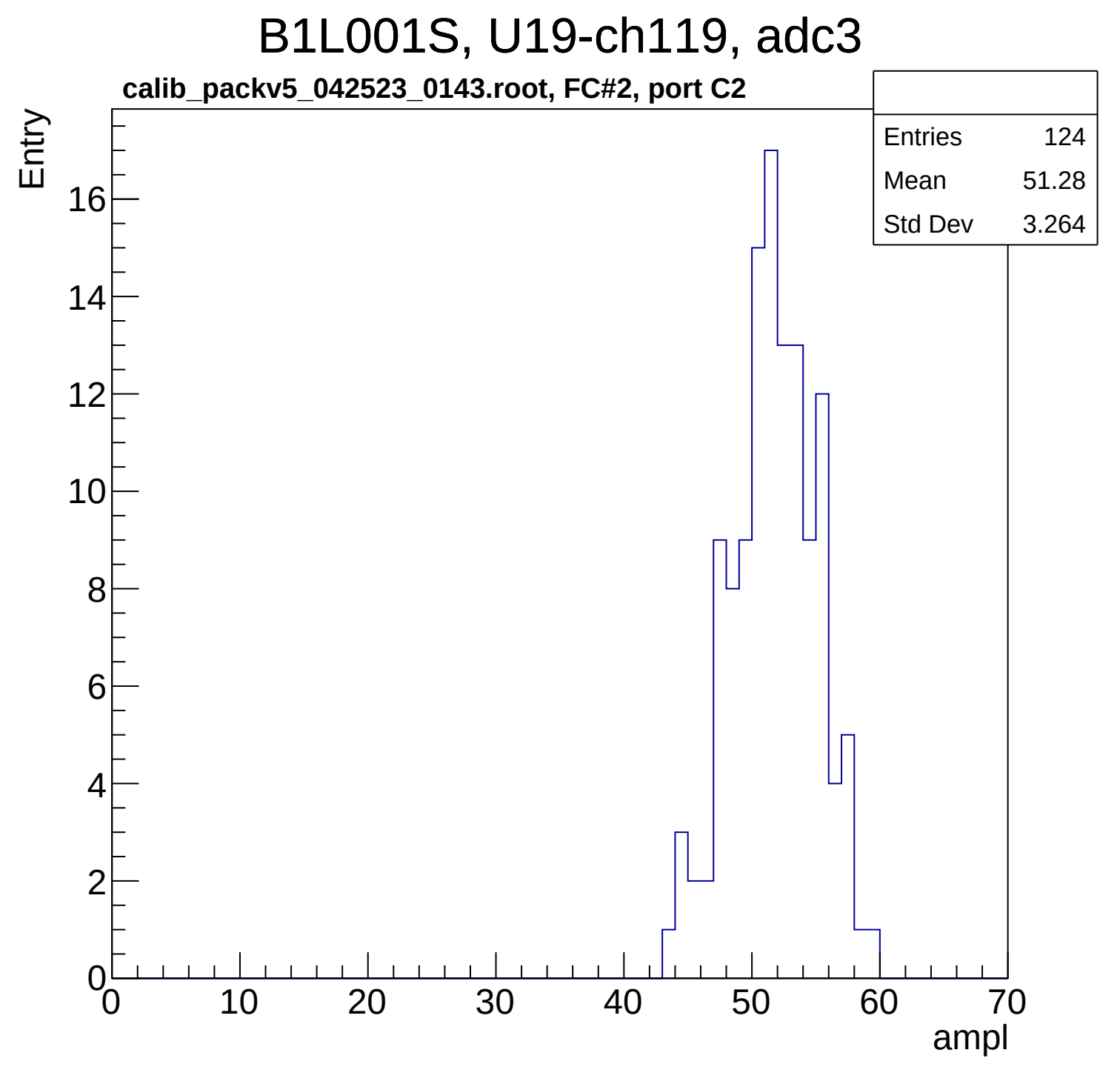
60
70


B1L001S, U19-ch118, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 42
Std Dev 20
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch119, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 172
Mean 30.2
Std Dev 4.453
Gaus mean : 31.3609
Gaus Width: 3.6070
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70


B1L001S, U19-ch119, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 127
Mean 37.45
Std Dev 3.134
Gaus mean : 38.1640
Gaus Width: 3.5453
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70


B1L001S, U19-ch119, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 143
Mean 44.71
Std Dev 3.272
Gaus mean : 44.8135
Gaus Width: 2.9535
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70


B1L001S, U19-ch119, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 124
Mean 51.28
Std Dev 3.264
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
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60
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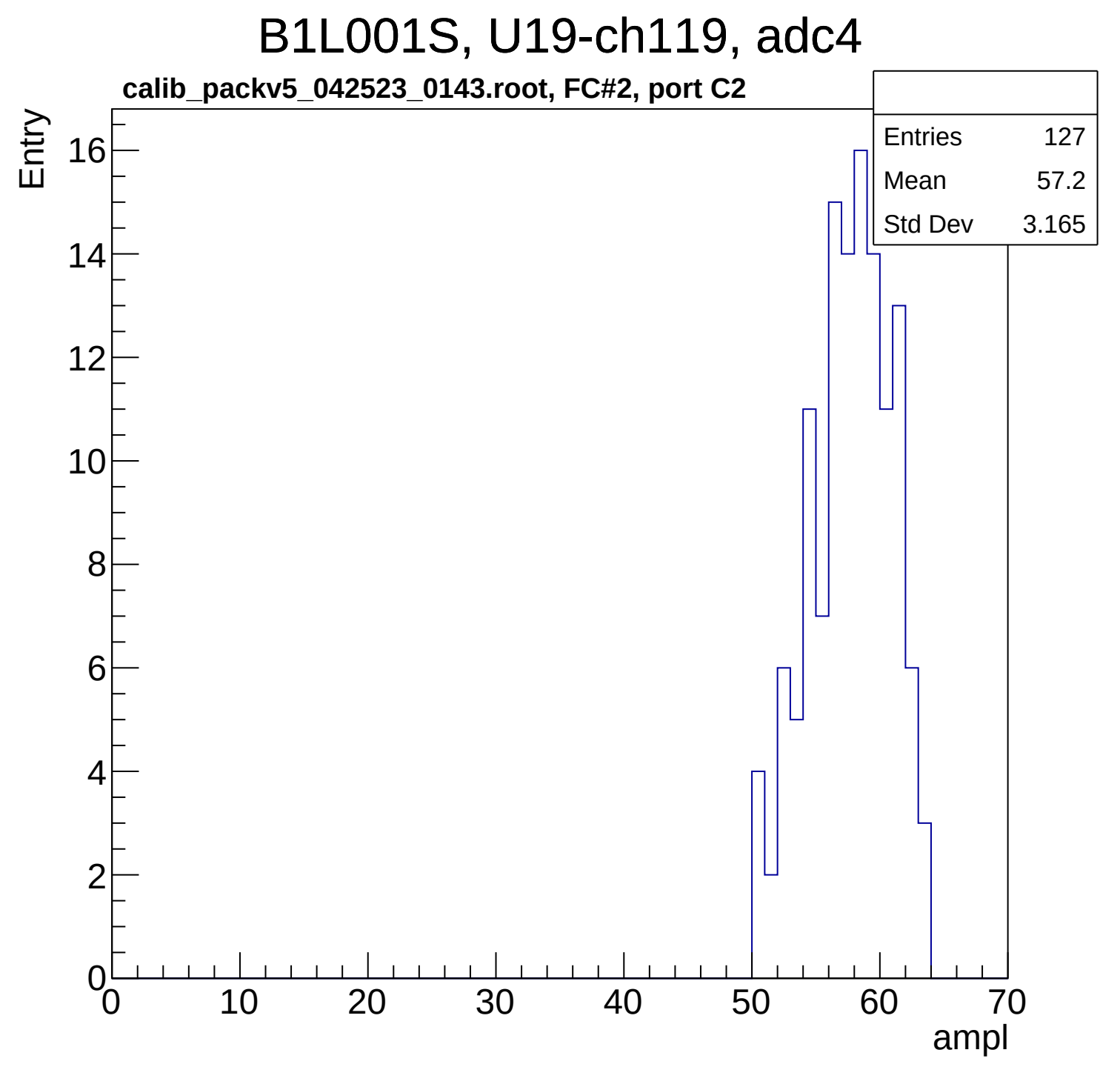
B1L001S, U19-ch119, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 127
Mean 57.2
Std Dev 3.165
Entry
ampl
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2
4
6
8
10
12
14
16
0
10
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40
50
60
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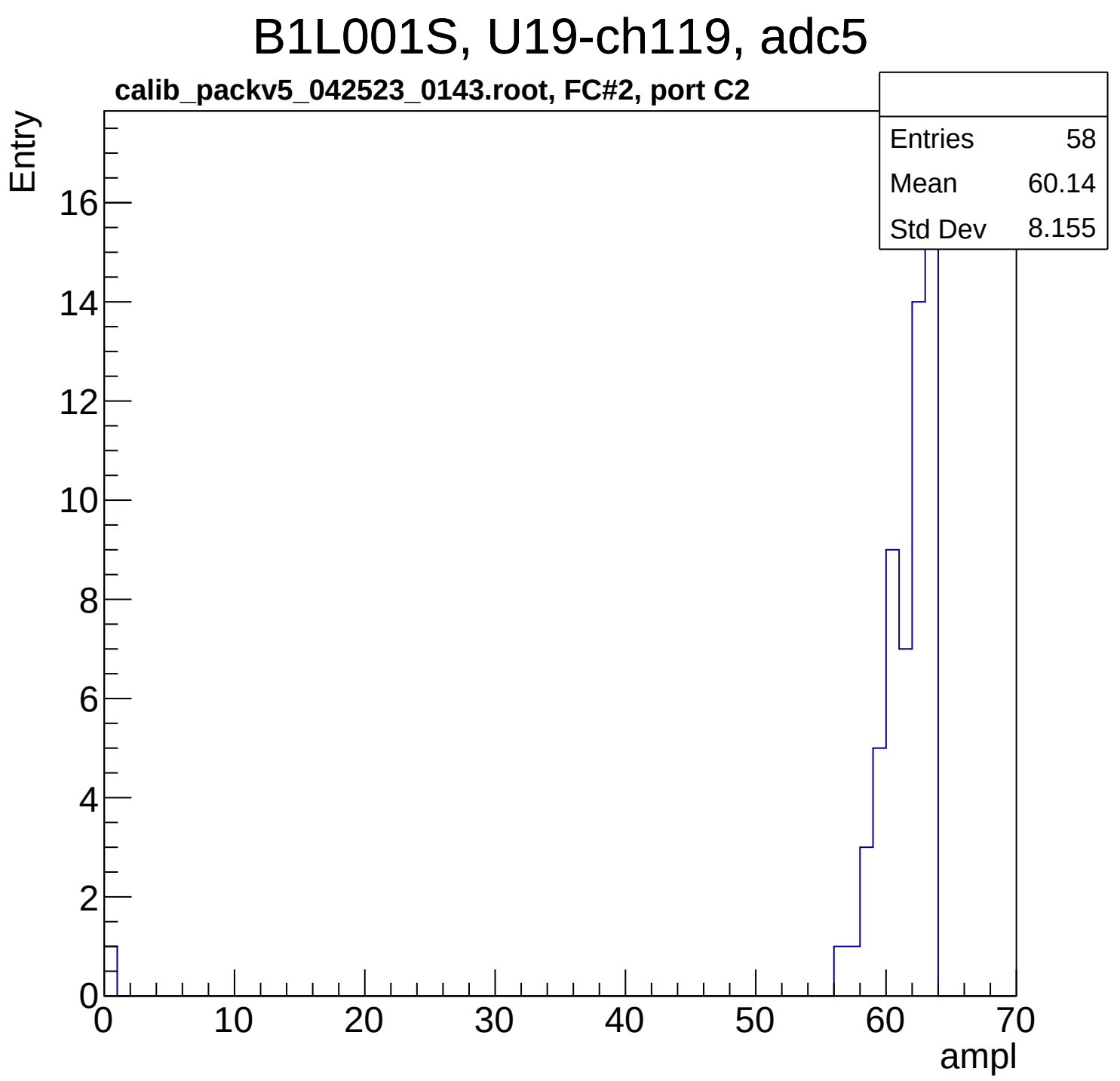
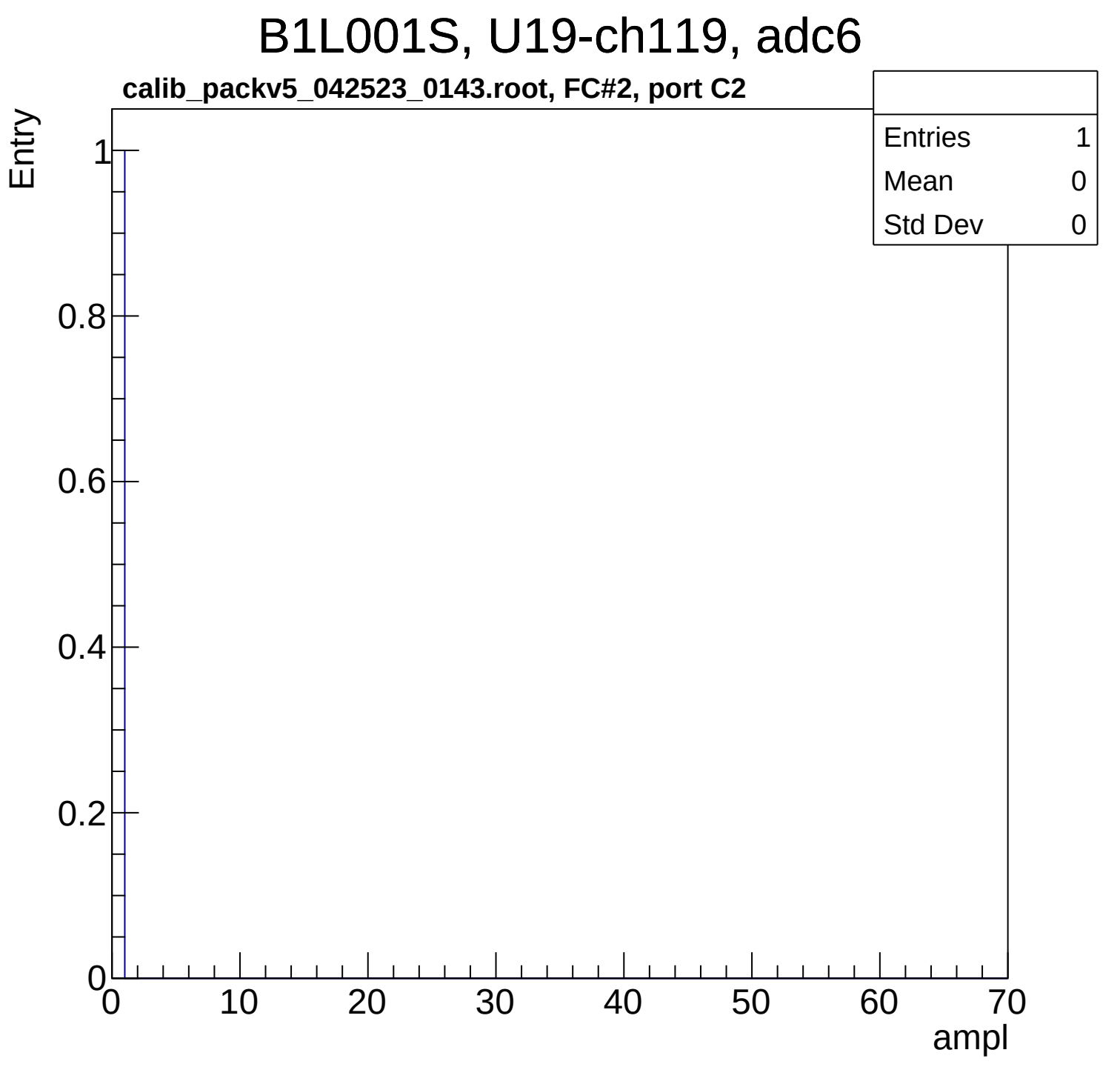
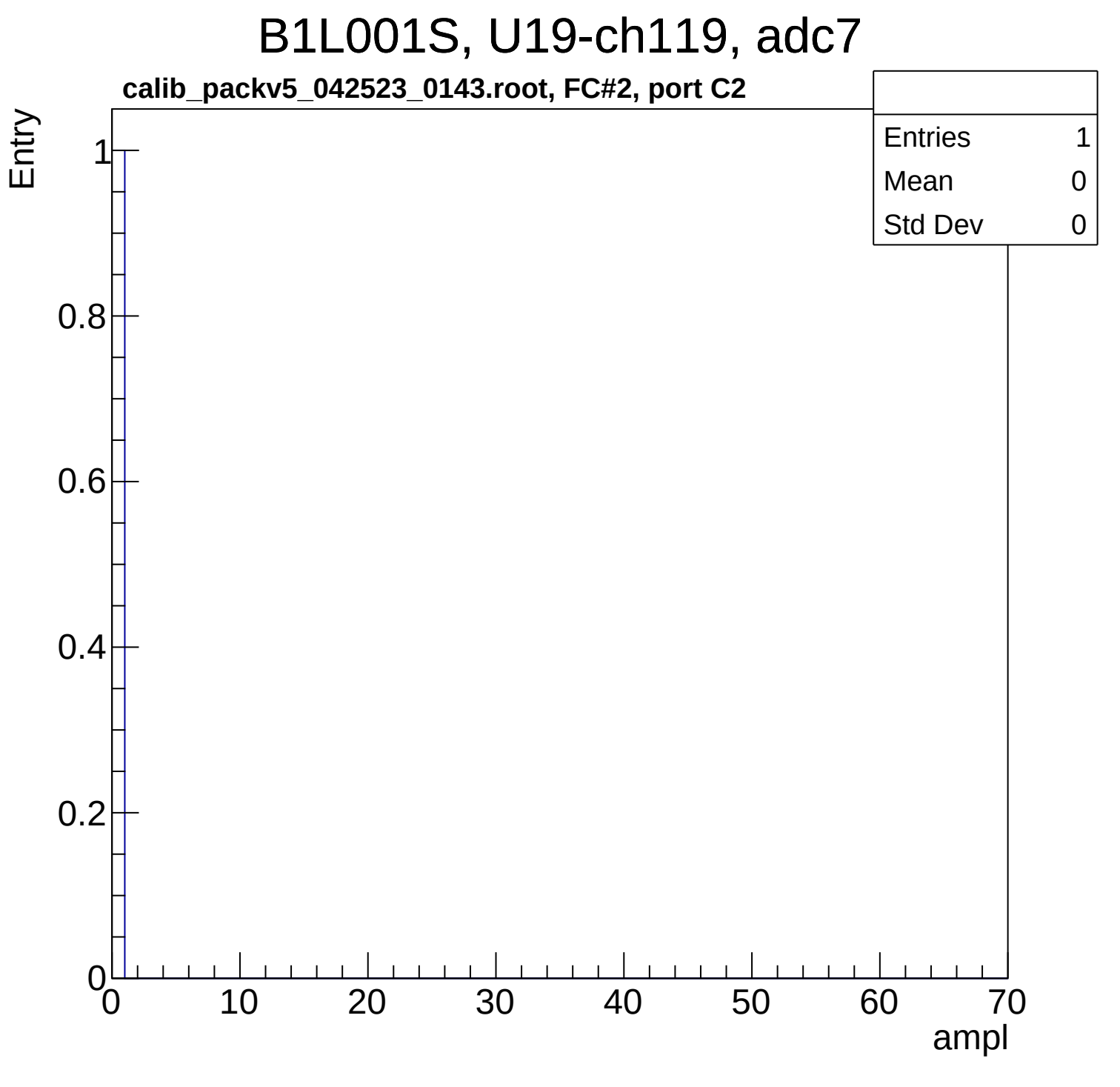

B1L001S, U19-ch119, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 58
Mean 60.14
Std Dev 8.155
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70


B1L001S, U19-ch119, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch119, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 0
Std Dev 0
Entry
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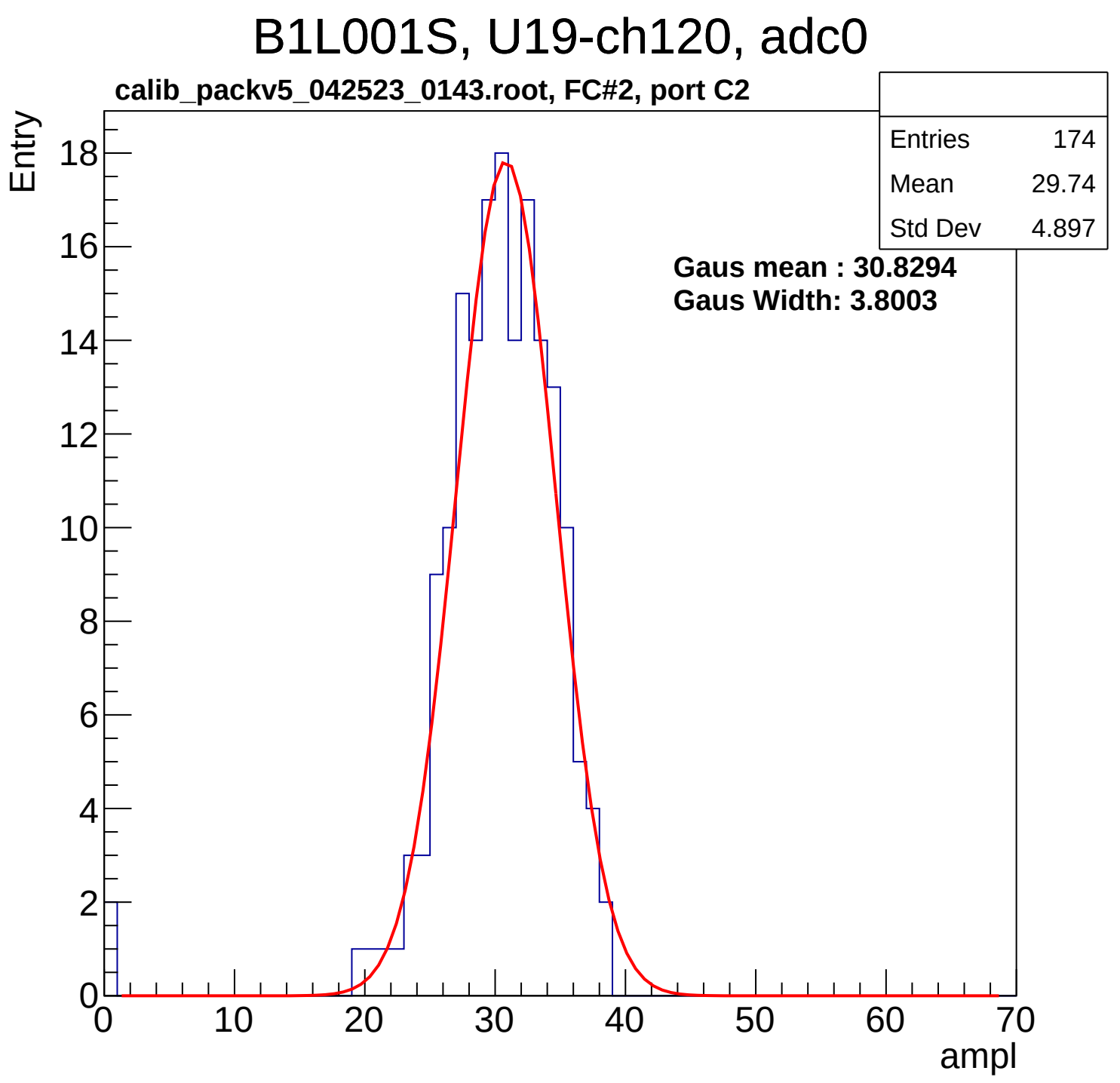
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch120, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 174
Mean 29.74
Std Dev 4.897
Gaus mean : 30.8294
Gaus Width: 3.8003
Entry
ampl
0
2
4
6
8
10
12
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16
18
0
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20
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40
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60
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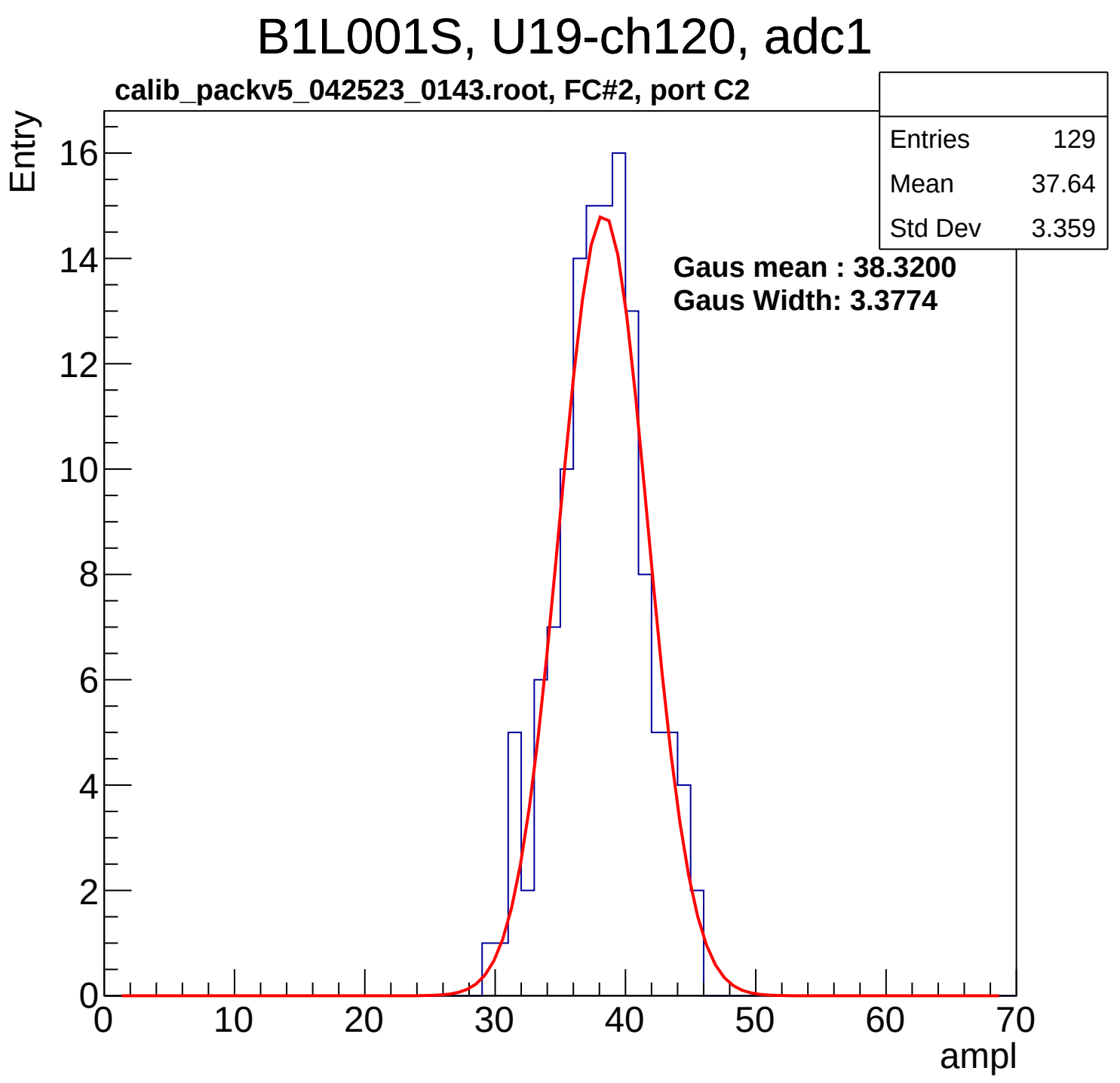
B1L001S, U19-ch120, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 129
Mean 37.64
Std Dev 3.359
Gaus mean : 38.3200
Gaus Width: 3.3774
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
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40
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60
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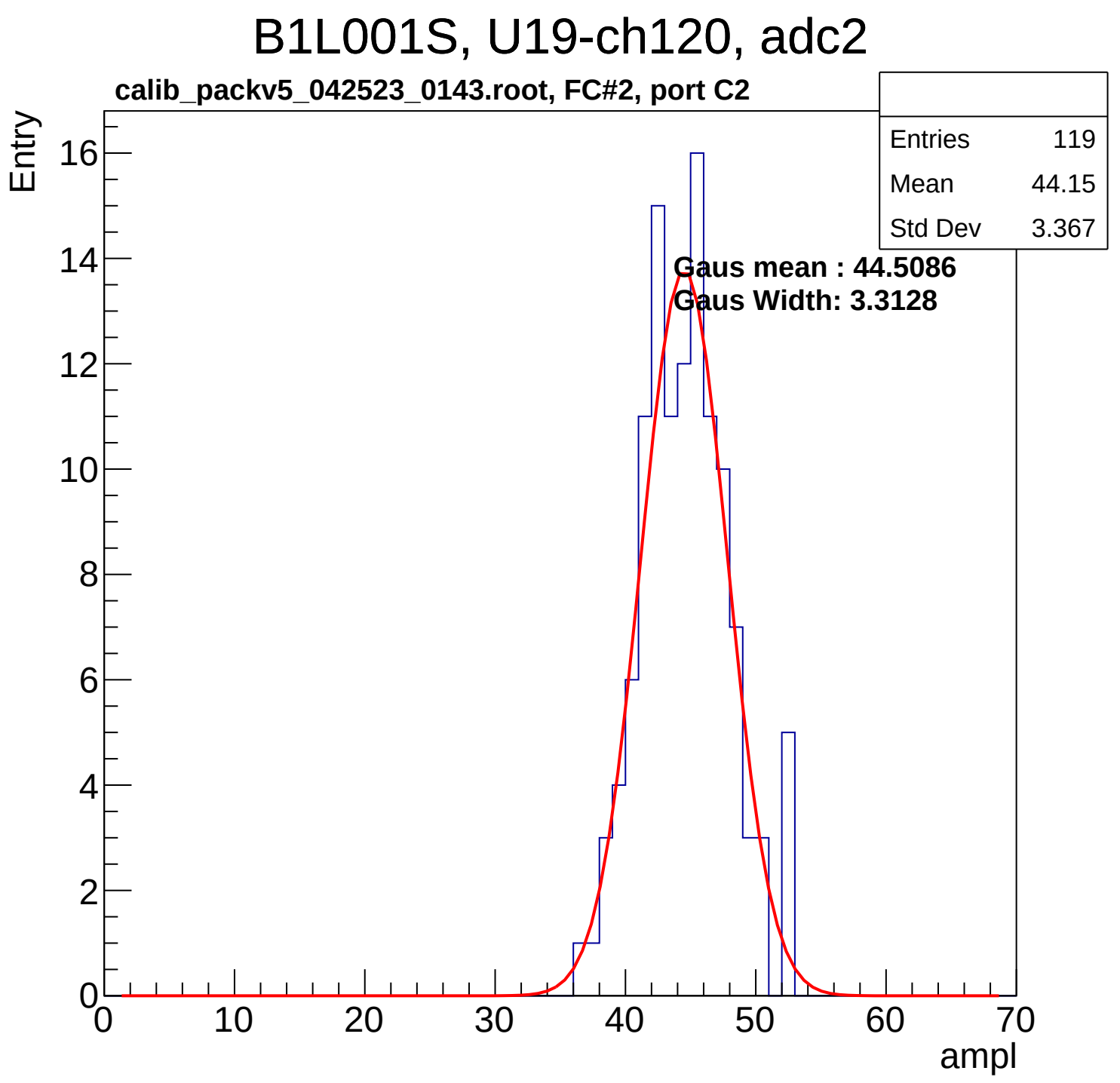
B1L001S, U19-ch120, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 119
Mean 44.15
Std Dev 3.367
Gaus mean : 44.5086
Gaus Width: 3.3128
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
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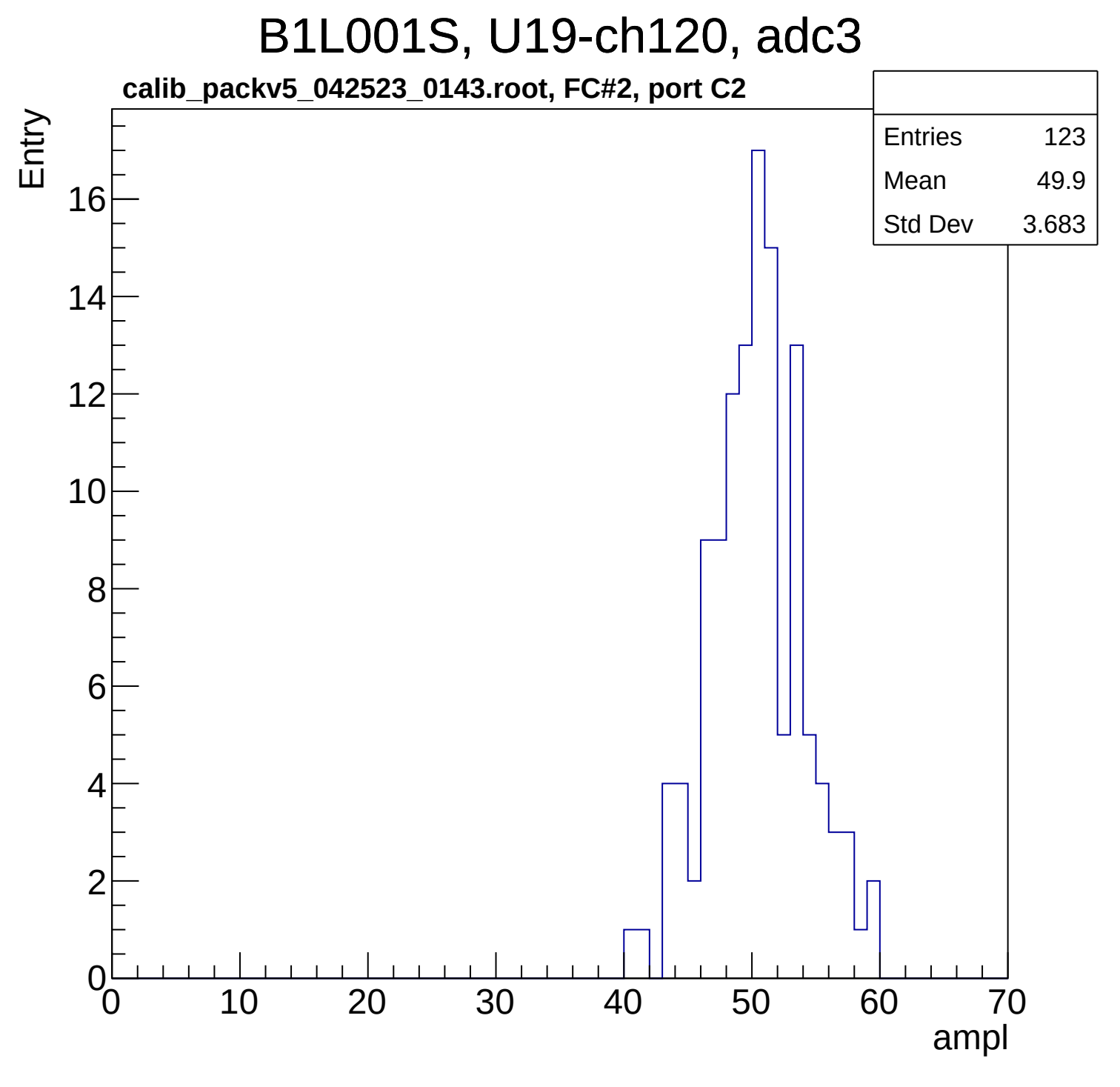
B1L001S, U19-ch120, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 123
Mean 49.9
Std Dev 3.683
Entry
ampl
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2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
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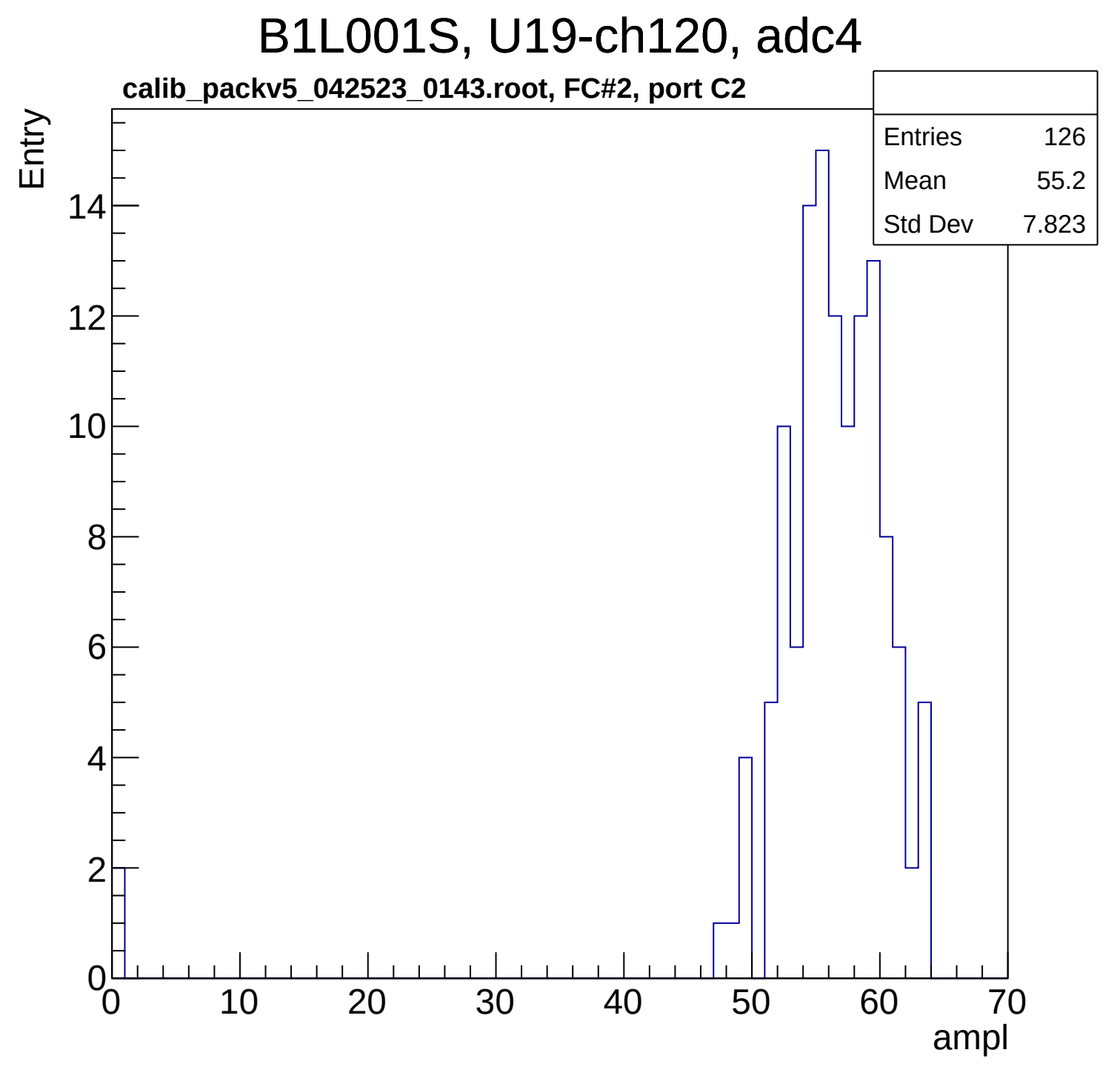
B1L001S, U19-ch120, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 126
Mean 55.2
Std Dev 7.823
Entry
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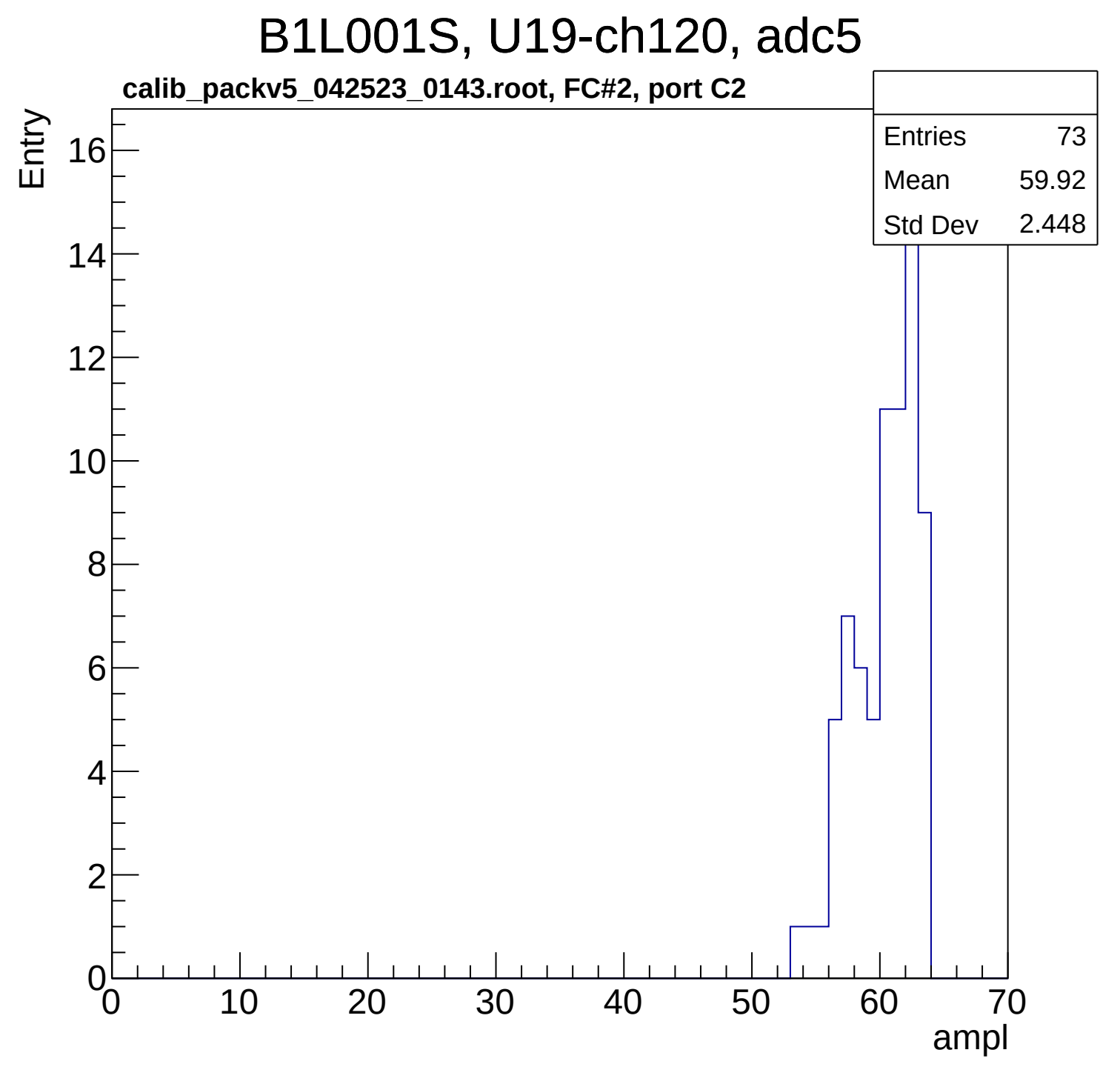
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch120, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 73
Mean 59.92
Std Dev 2.448
Entry
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6
8
10
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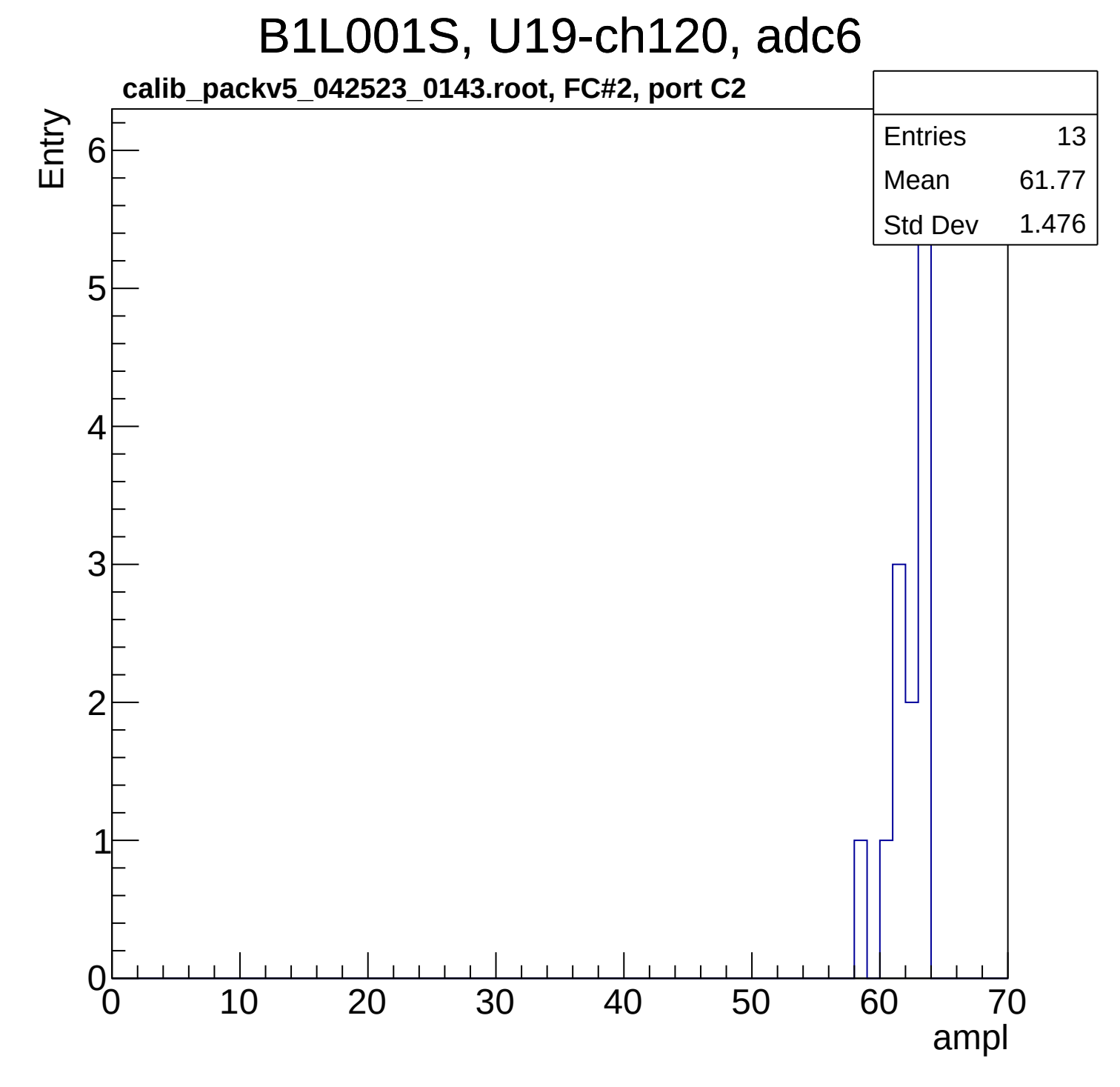
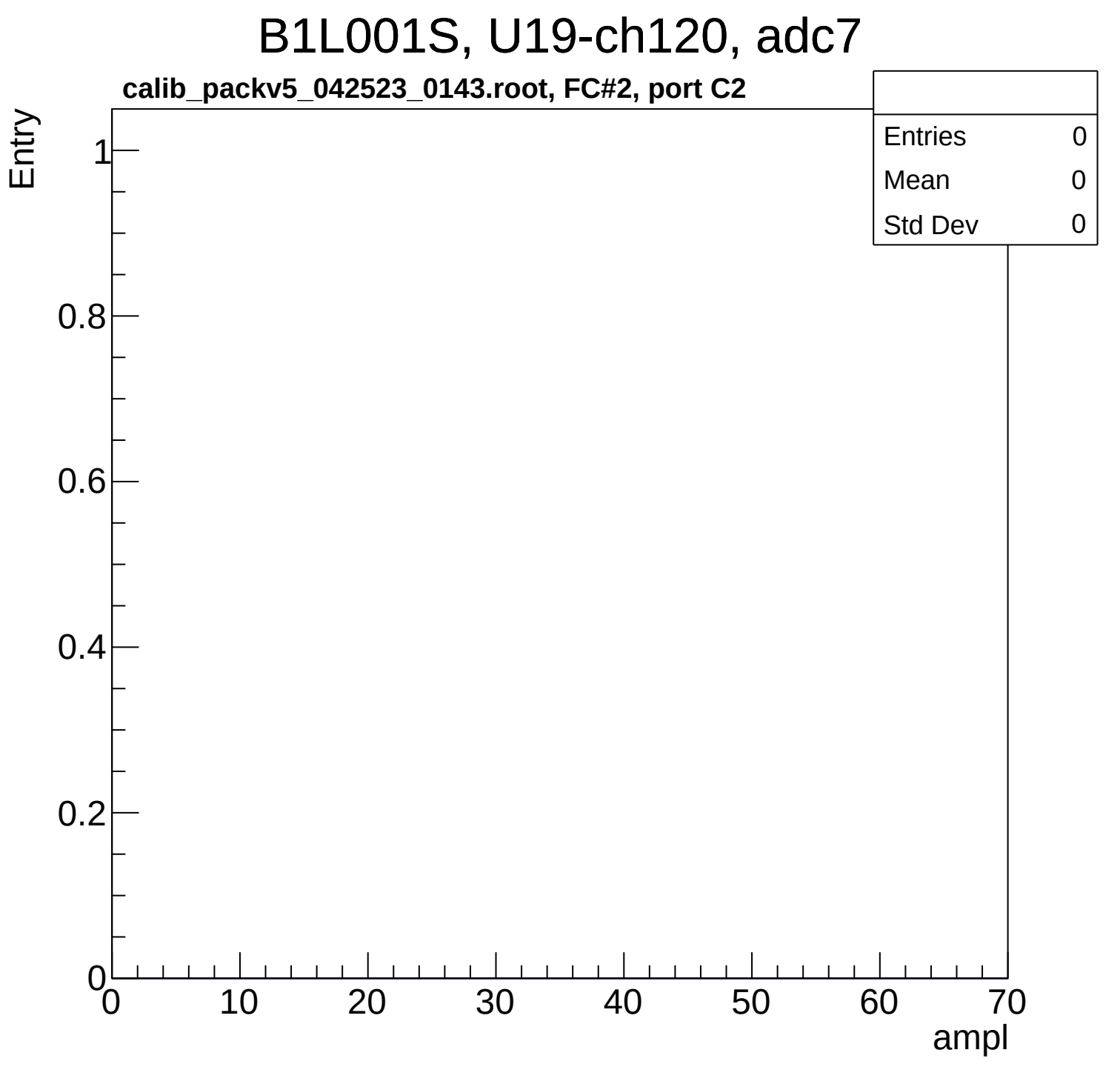
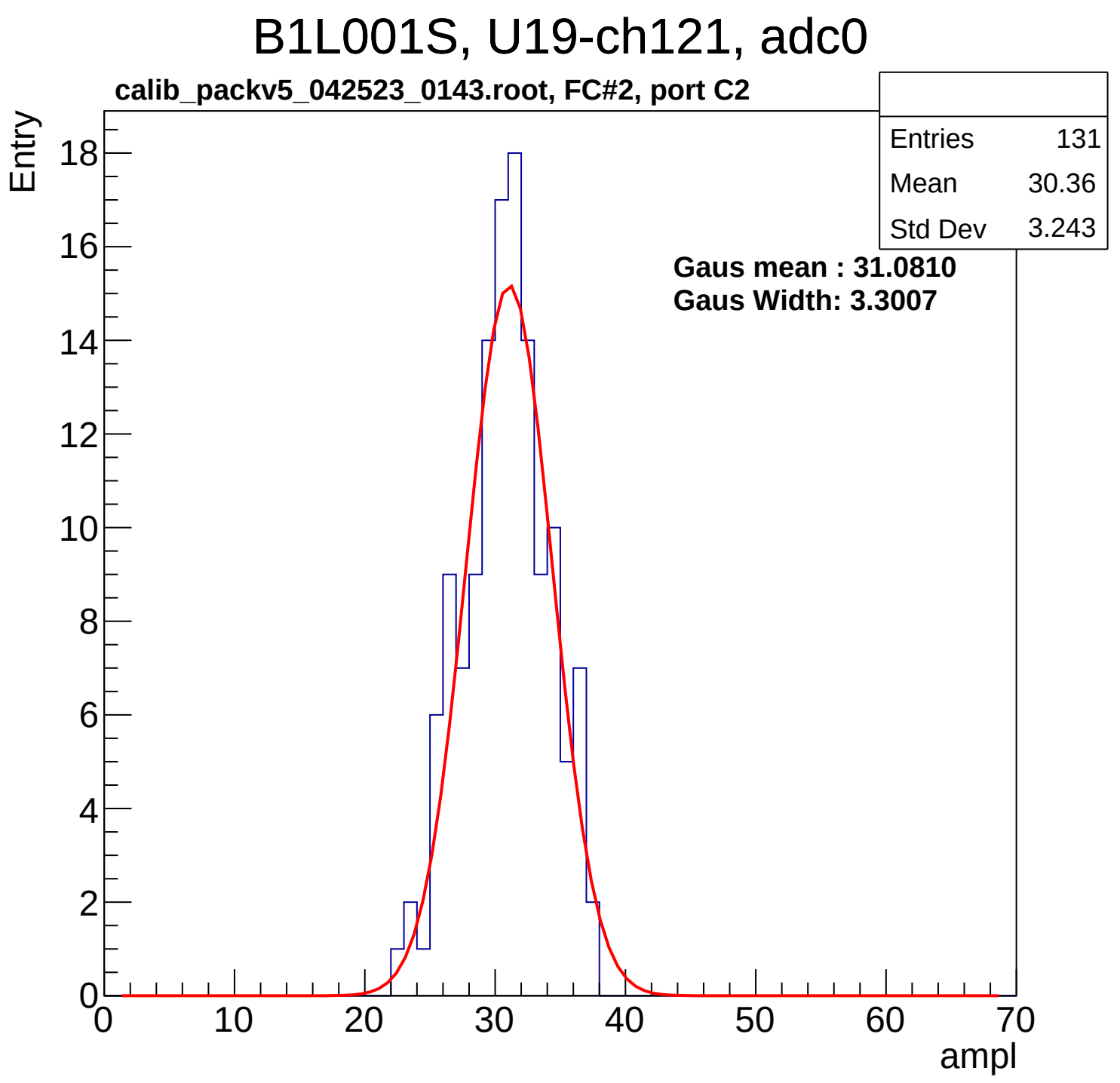
14
16
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch120, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 13
Mean 61.77
Std Dev 1.476
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L001S, U19-ch120, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch121, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 131
Mean 30.36
Std Dev 3.243
Gaus mean : 31.0810
Gaus Width: 3.3007
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
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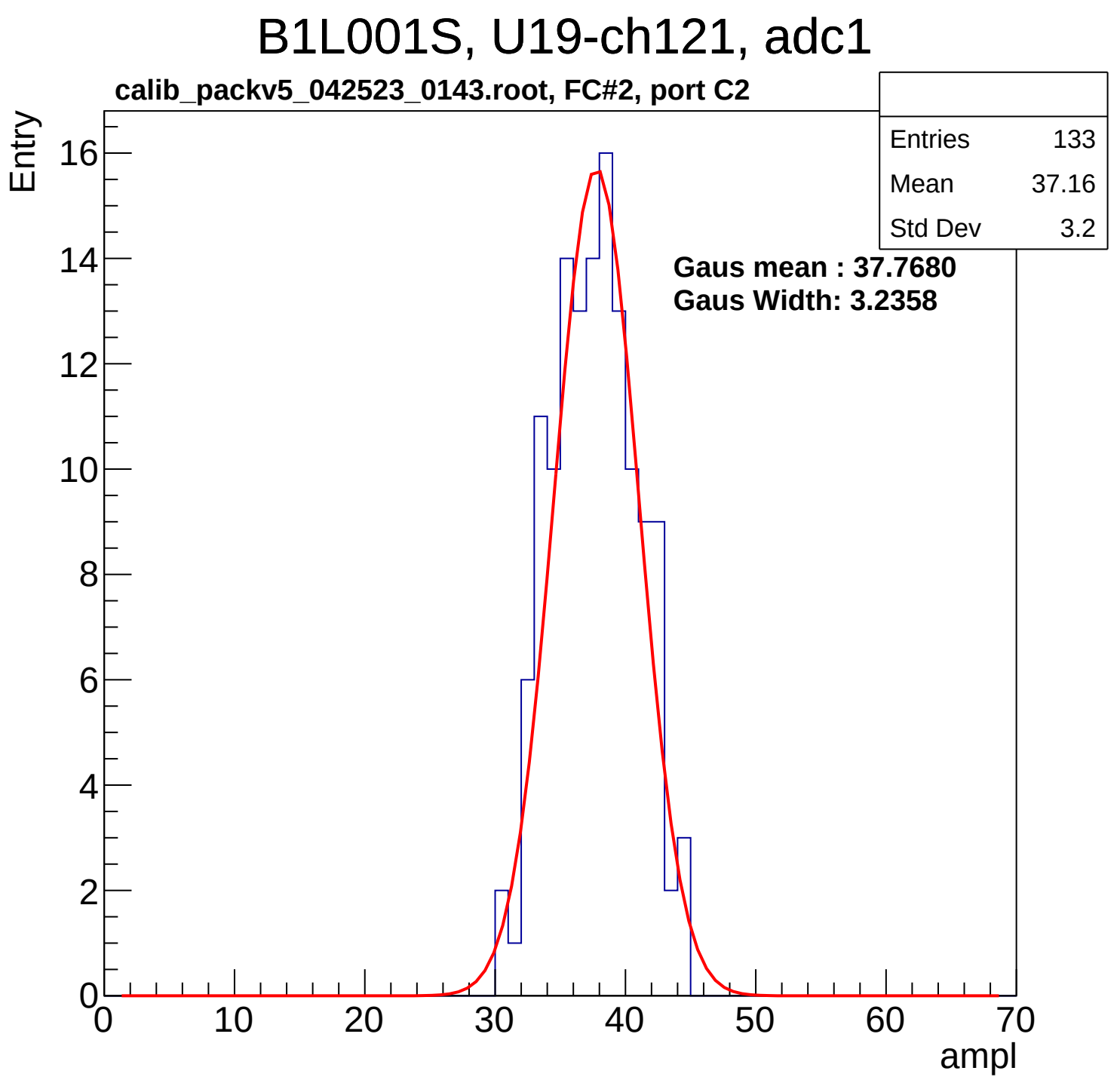
B1L001S, U19-ch121, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 133
Mean 37.16
Std Dev 3.2
Gaus mean : 37.7680
Gaus Width: 3.2358
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
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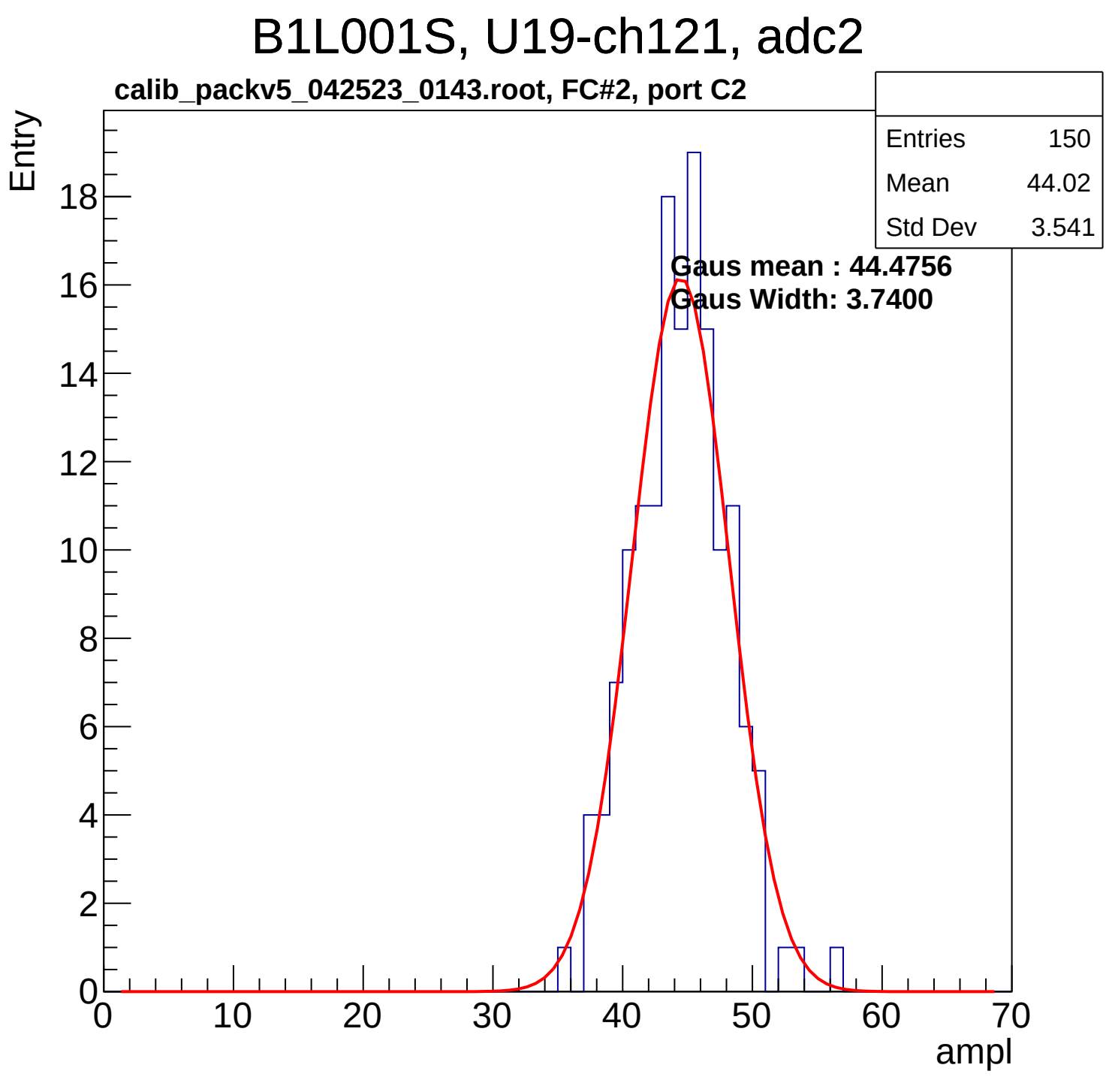
B1L001S, U19-ch121, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 150
Mean 44.02
Std Dev 3.541
Gaus mean : 44.4756
Gaus Width: 3.7400
Entry
ampl
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4
6
8
10
12
14
16
18
0
10
20
30
40
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60
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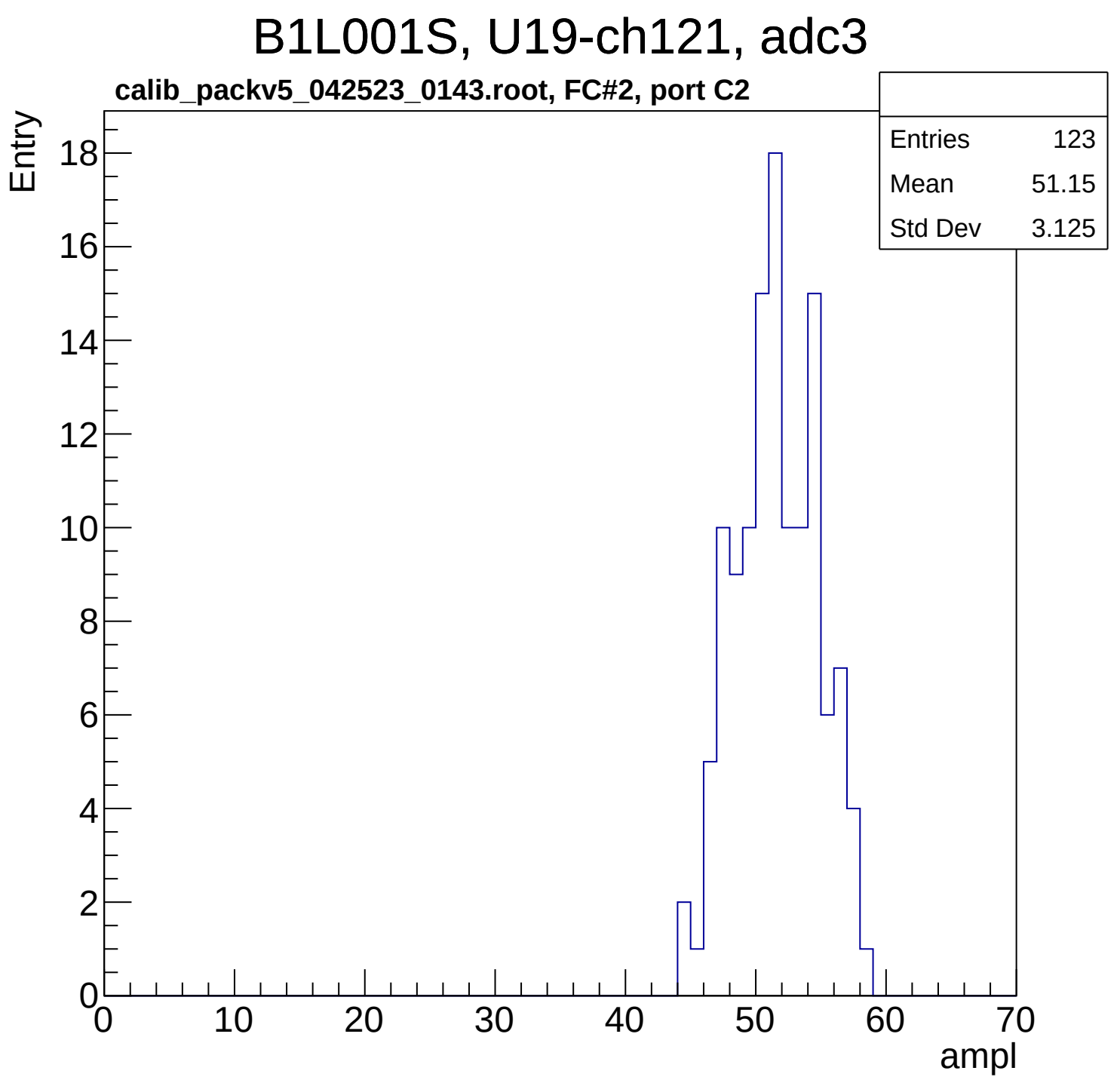
B1L001S, U19-ch121, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 123
Mean 51.15
Std Dev 3.125
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
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20
30
40
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60
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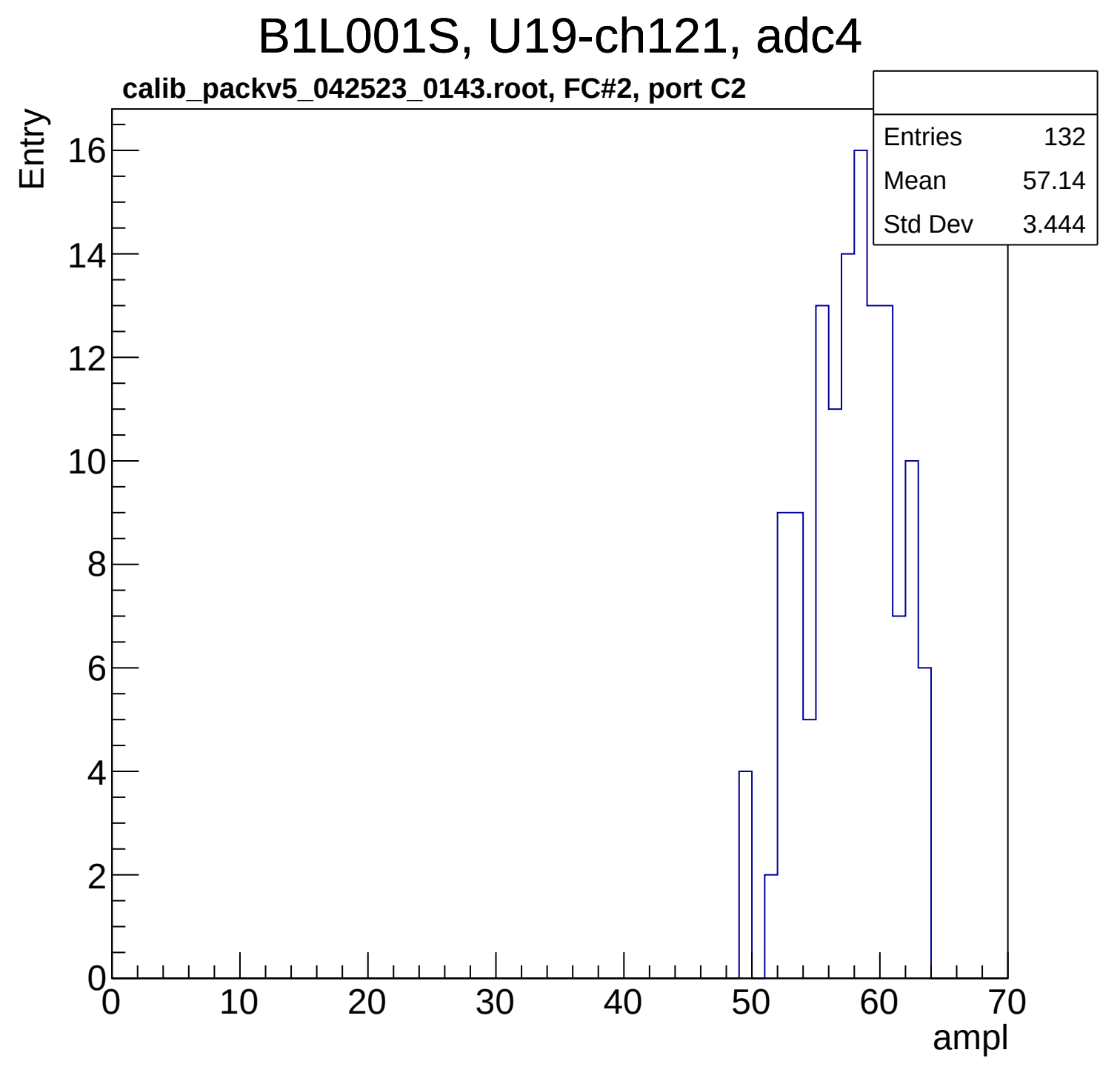
B1L001S, U19-ch121, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 132
Mean 57.14
Std Dev 3.444
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
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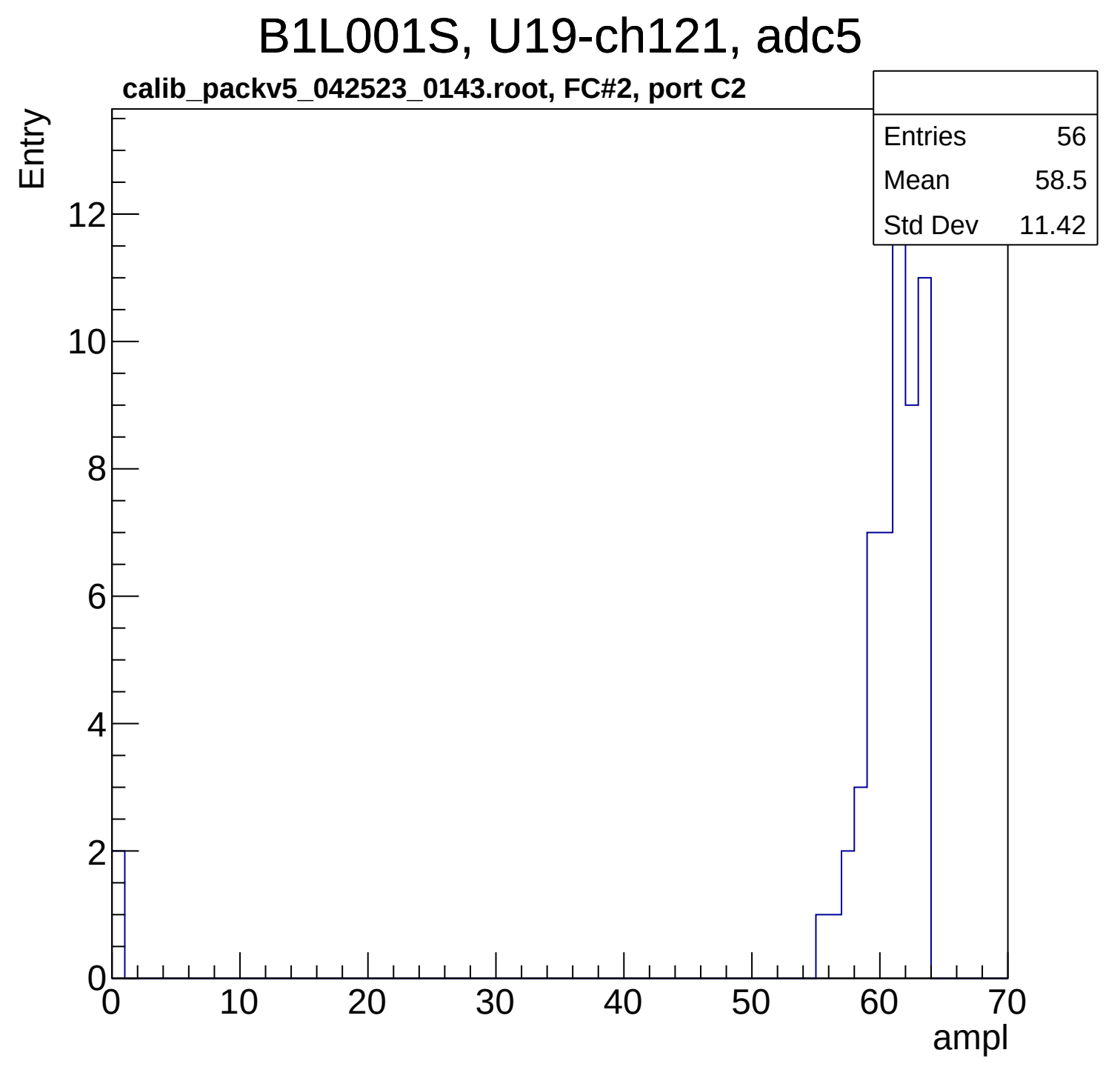
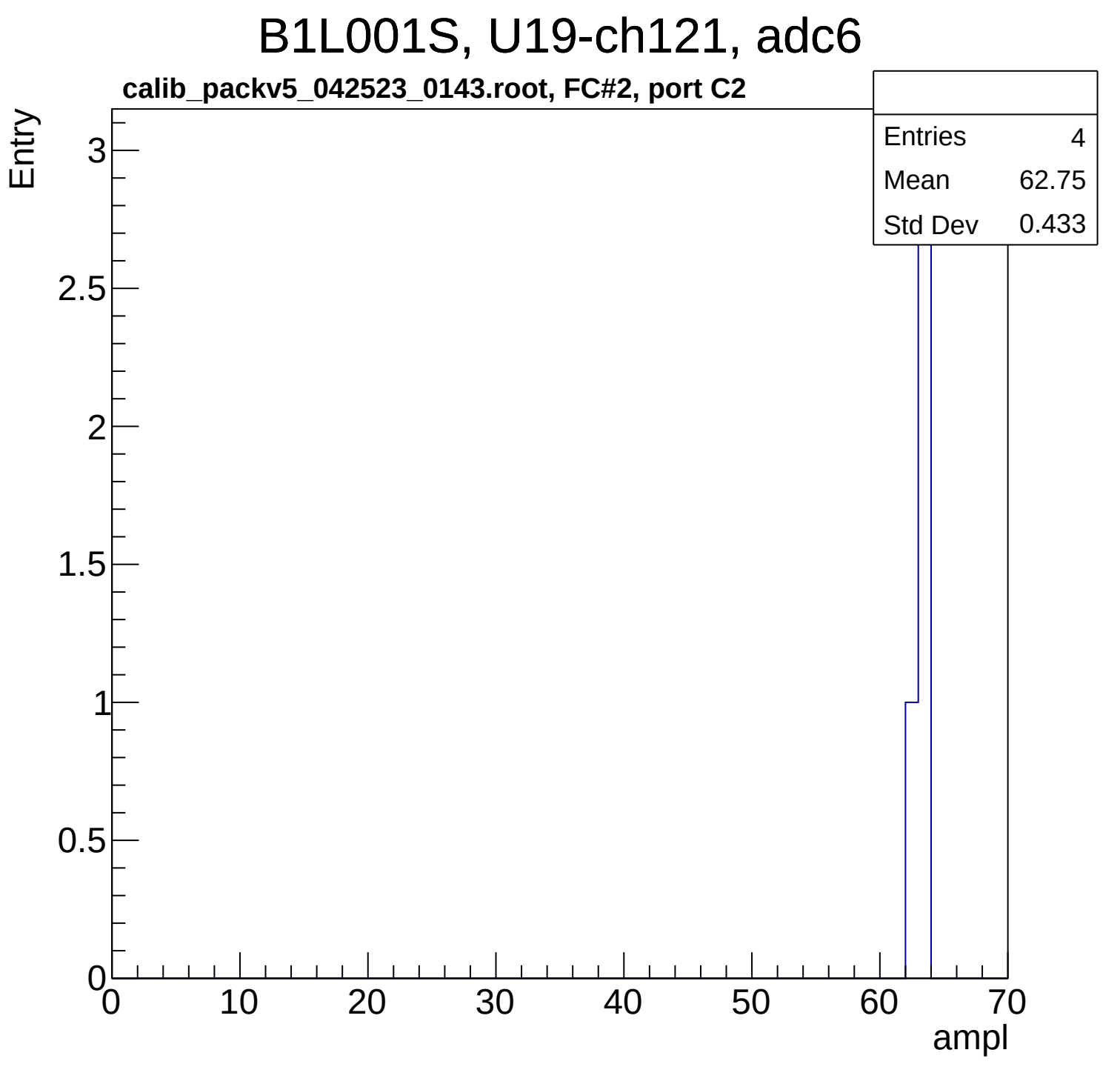
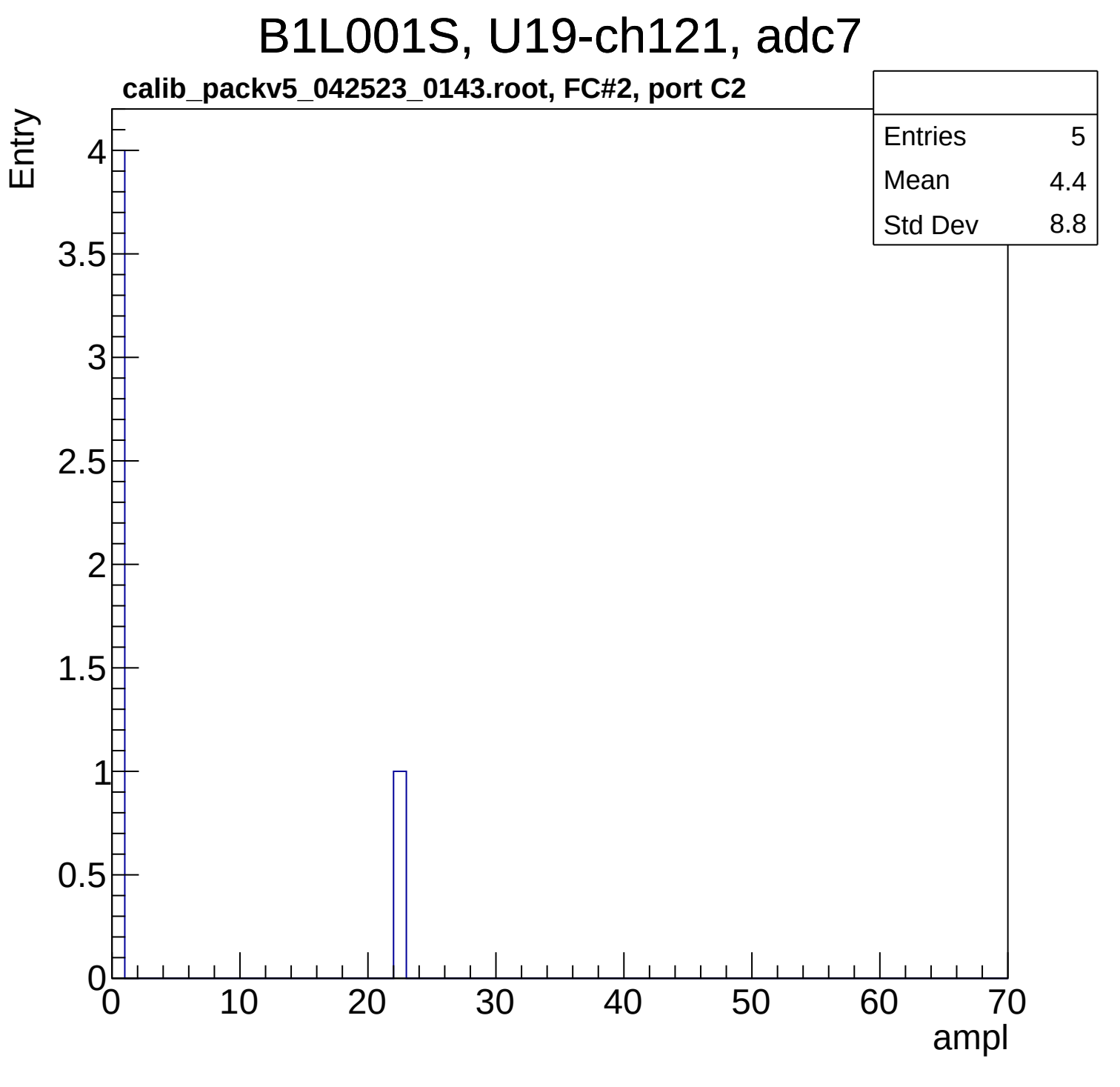

B1L001S, U19-ch121, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 56
Mean 58.5
Std Dev 11.42
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch121, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 4
Mean 62.75
Std Dev 0.433
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L001S, U19-ch121, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 5
Mean 4.4
Std Dev 8.8
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
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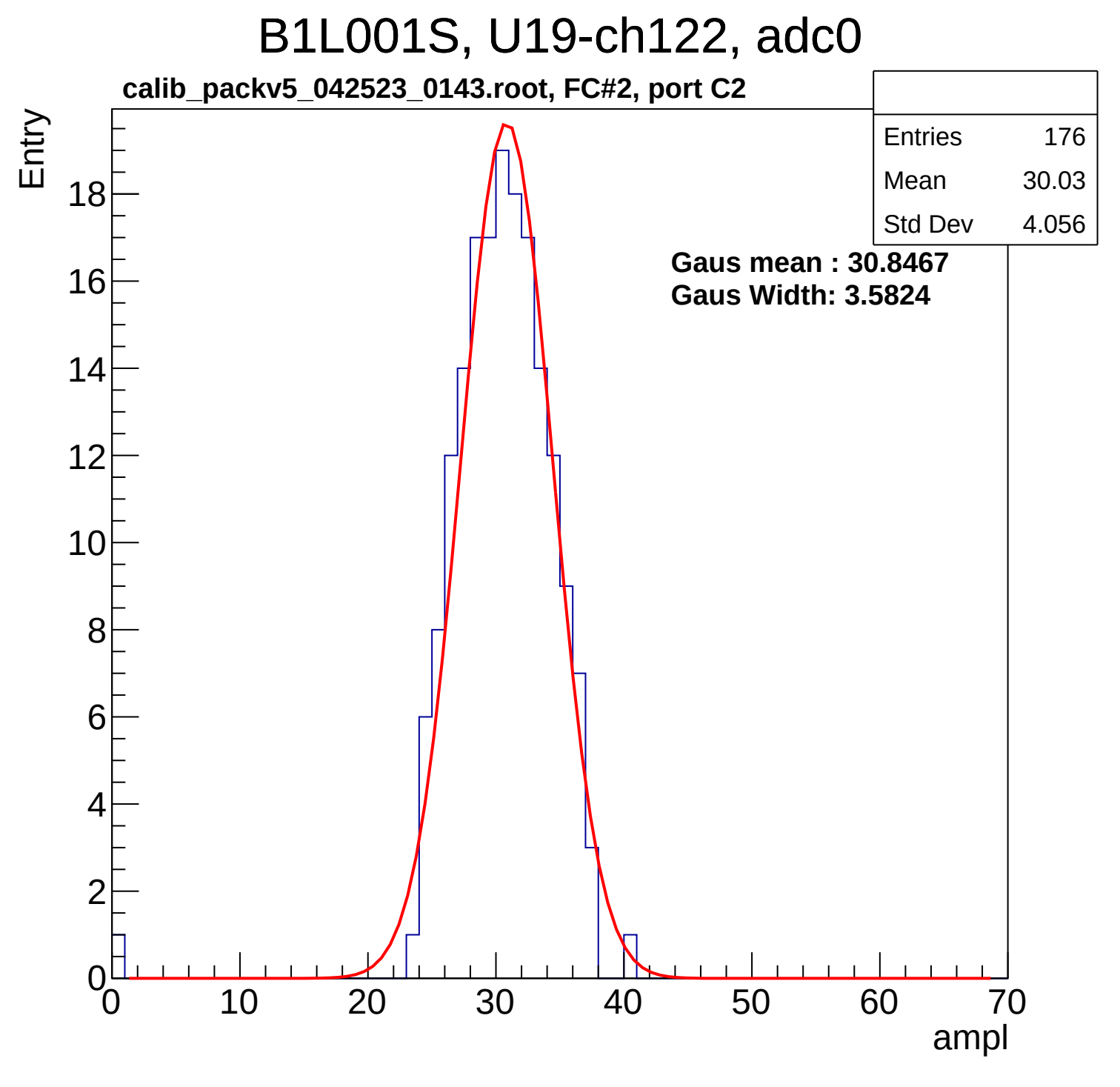
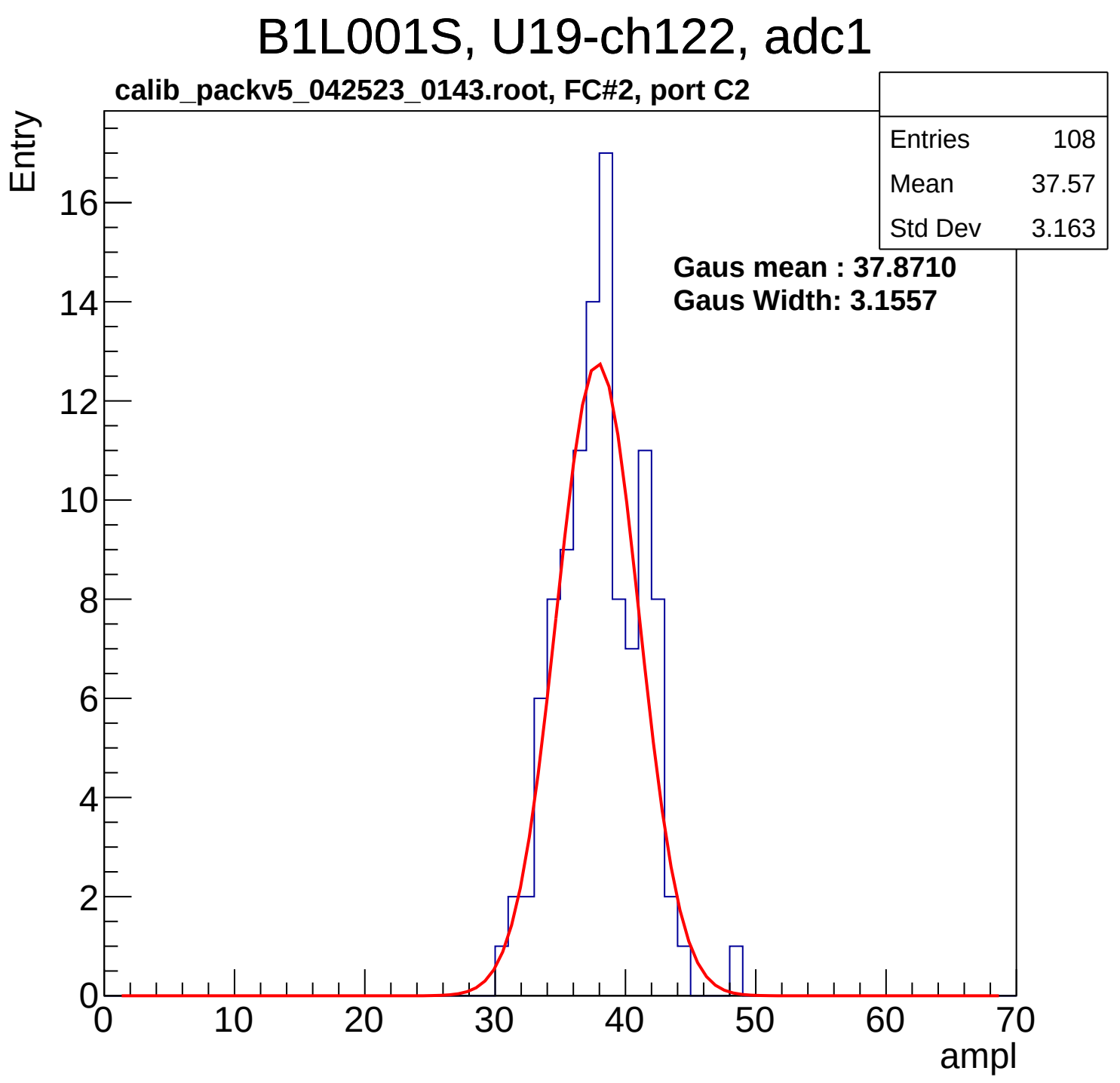
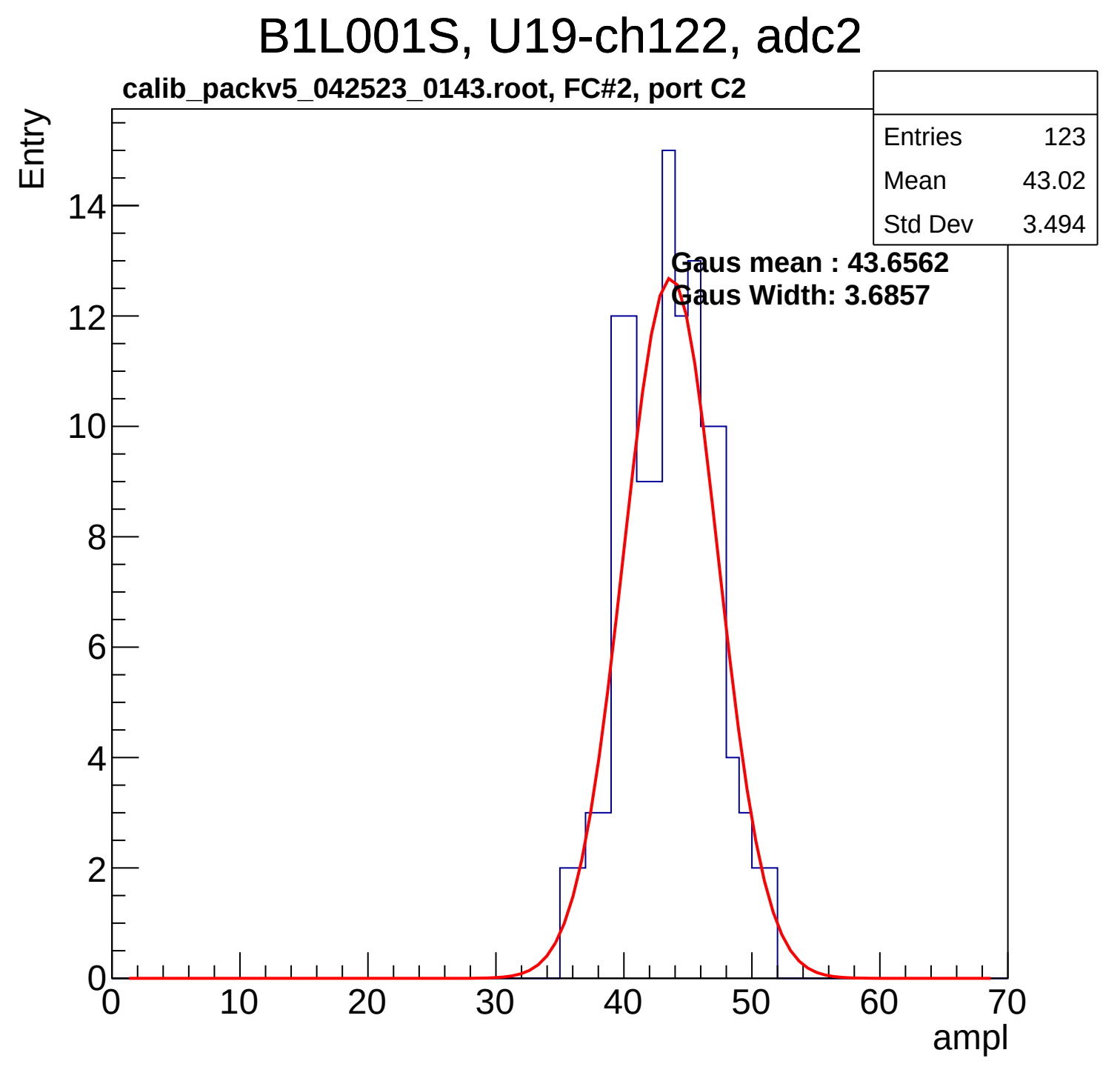

B1L001S, U19-ch122, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 176
Mean 30.03
Std Dev 4.056
Gaus mean : 30.8467
Gaus Width: 3.5824
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70


B1L001S, U19-ch122, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 108
Mean 37.57
Std Dev 3.163
Gaus mean : 37.8710
Gaus Width: 3.1557
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70


B1L001S, U19-ch122, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 123
Mean 43.02
Std Dev 3.494
Gaus mean : 43.6562
Gaus Width: 3.6857
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
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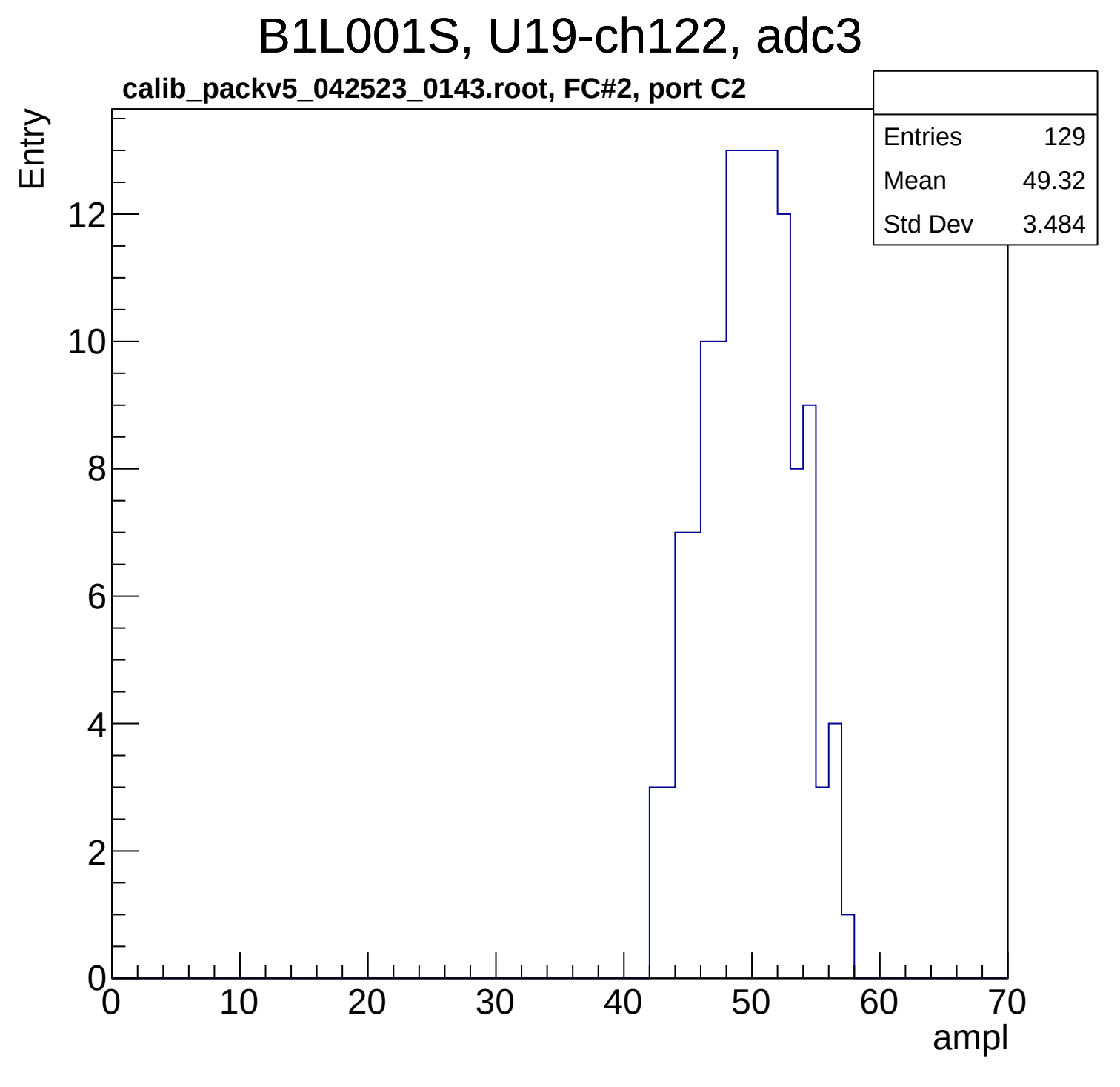
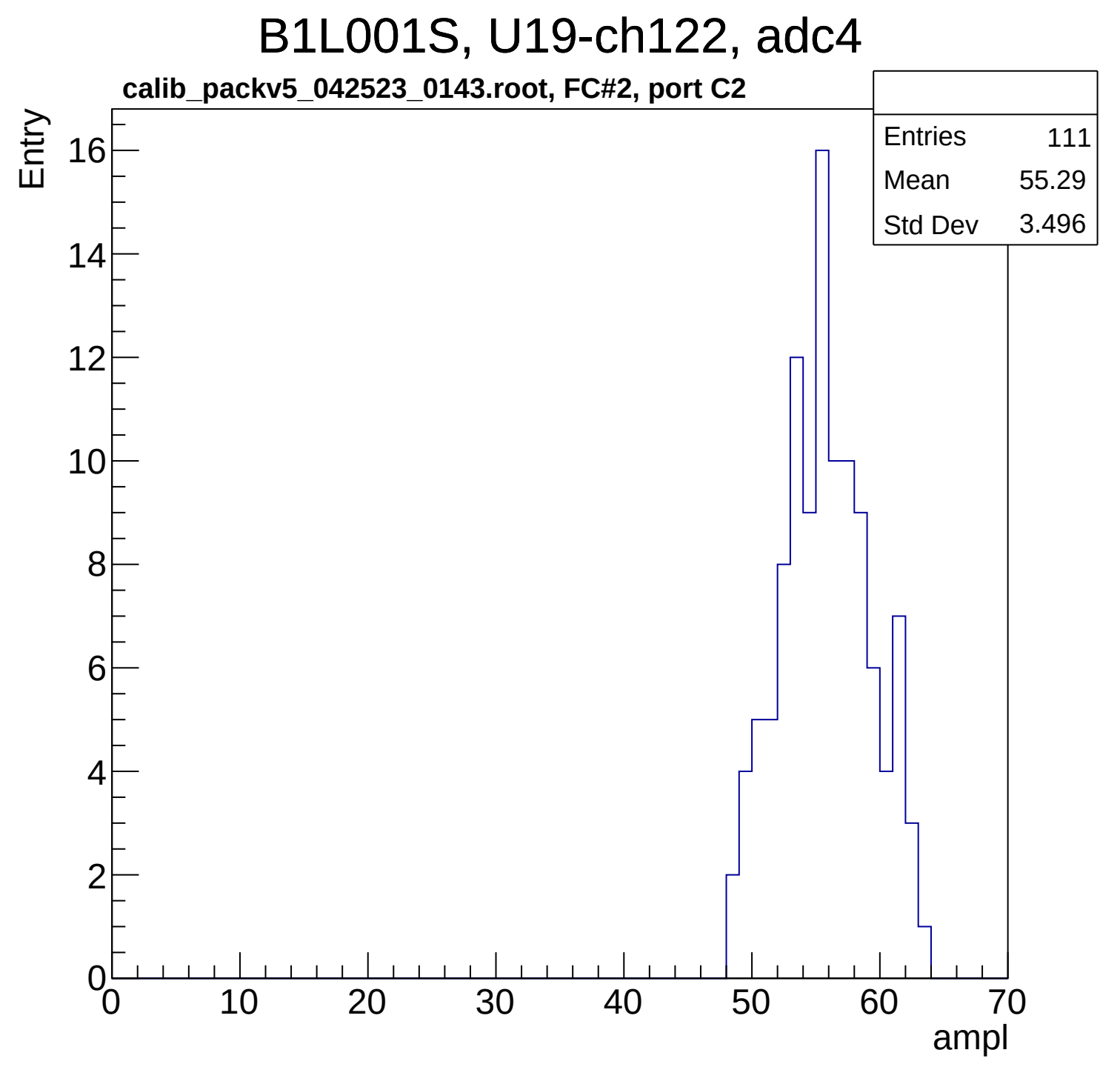
50
60
70


B1L001S, U19-ch122, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 129
Mean 49.32
Std Dev 3.484
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch122, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 111
Mean 55.29
Std Dev 3.496
Entry
ampl
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2
4
6
8
10
12
14
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0
10
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60
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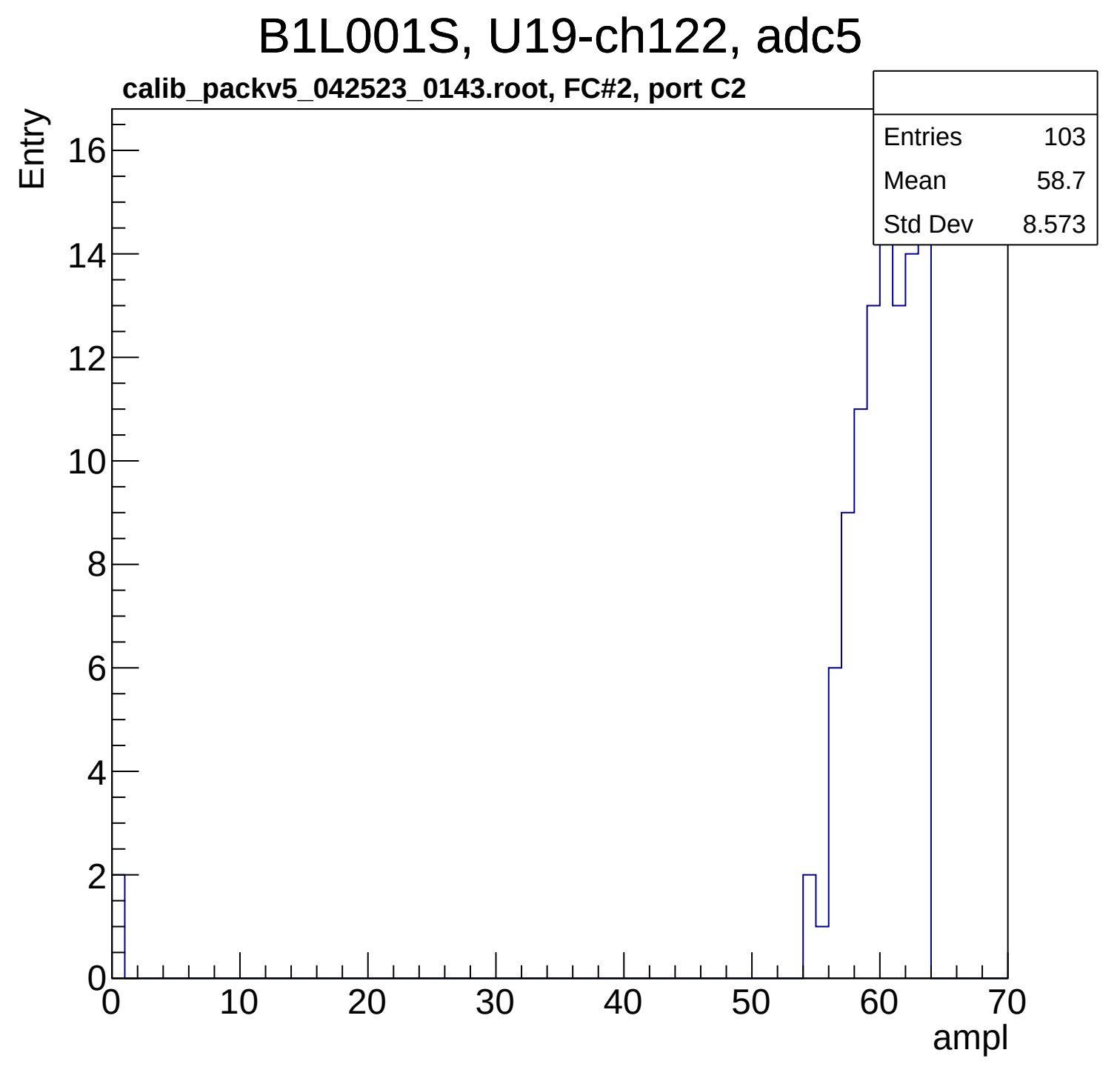
B1L001S, U19-ch122, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 103
Mean 58.7
Std Dev 8.573
Entry
ampl
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2
4
6
8
10
12
14
16
0
10
20
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40
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60
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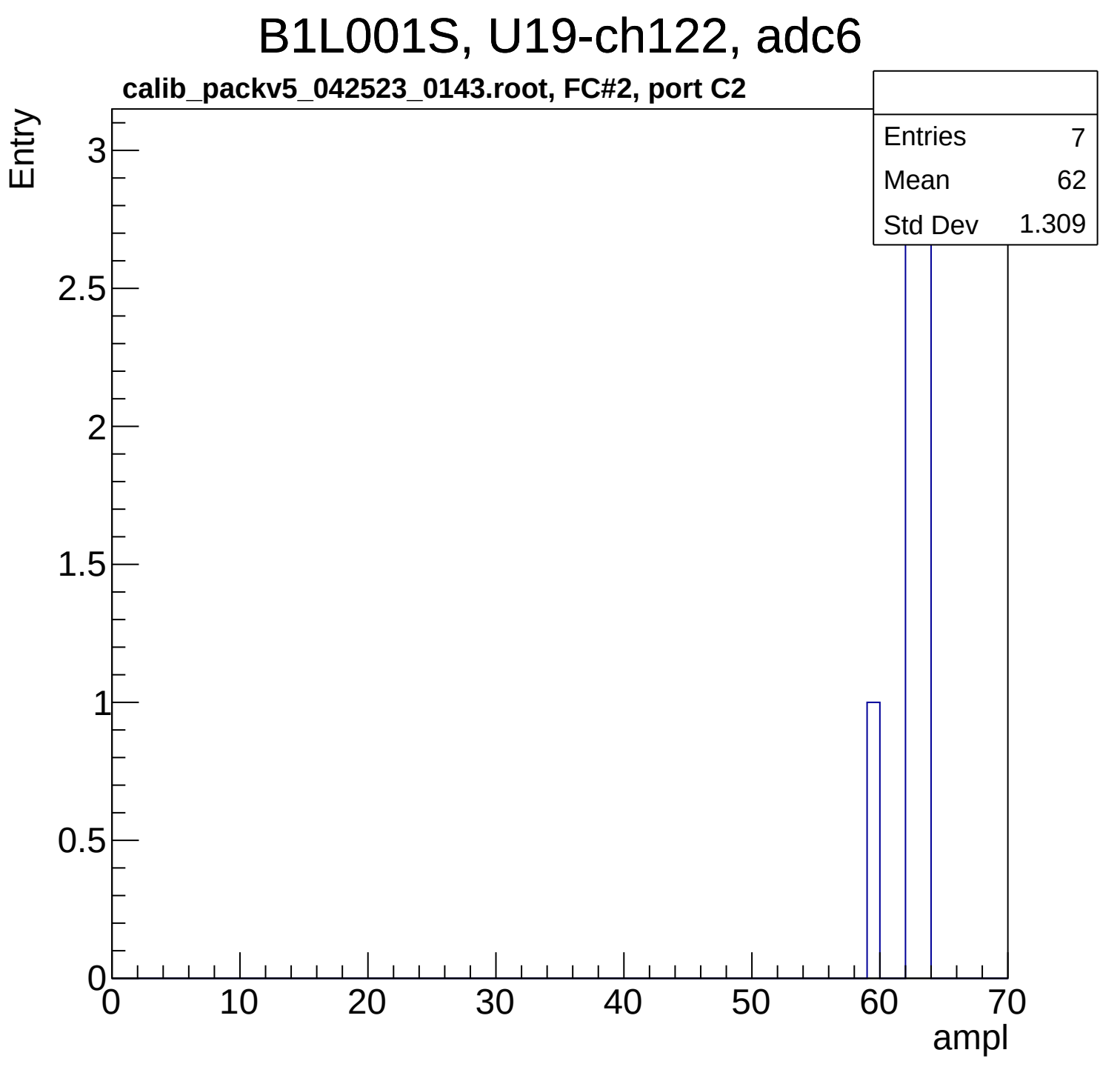
B1L001S, U19-ch122, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 7
Mean 62
Std Dev 1.309
Entry
ampl
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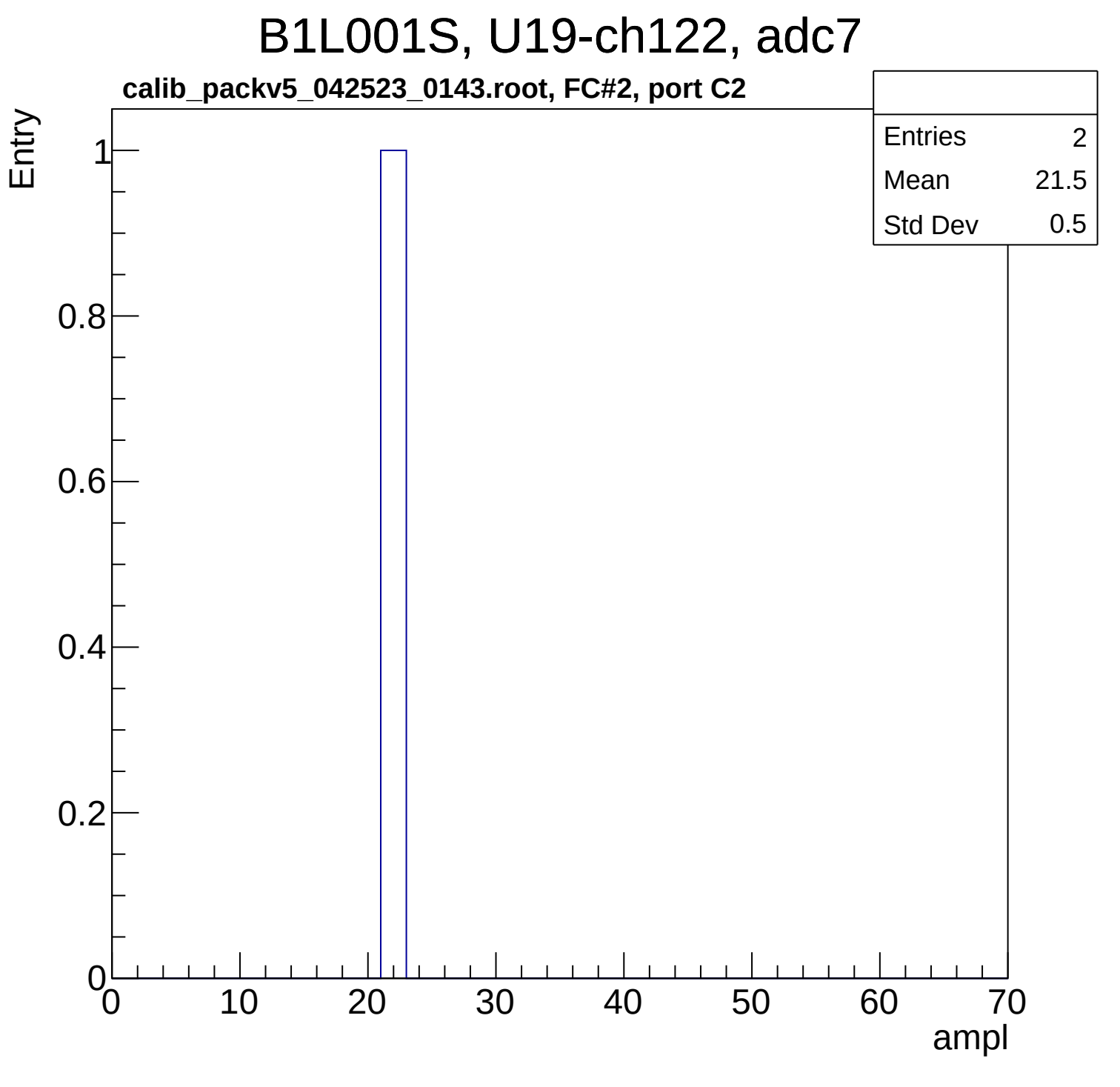
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L001S, U19-ch122, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 21.5
Std Dev 0.5
Entry
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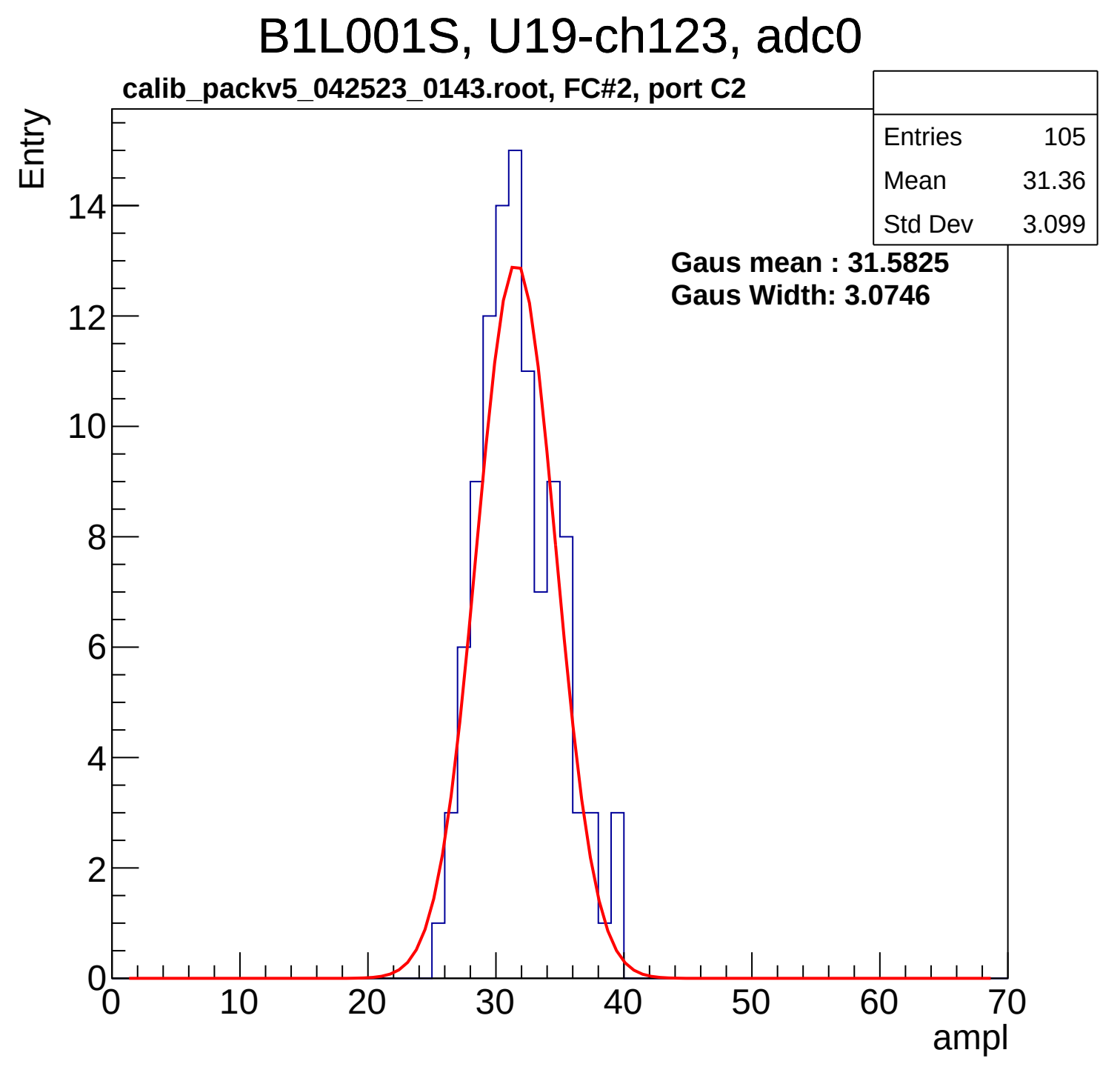
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch123, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 105
Mean 31.36
Std Dev 3.099
Gaus mean : 31.5825
Gaus Width: 3.0746
Entry
ampl
0
2
4
6
8
10
12
14
0
10
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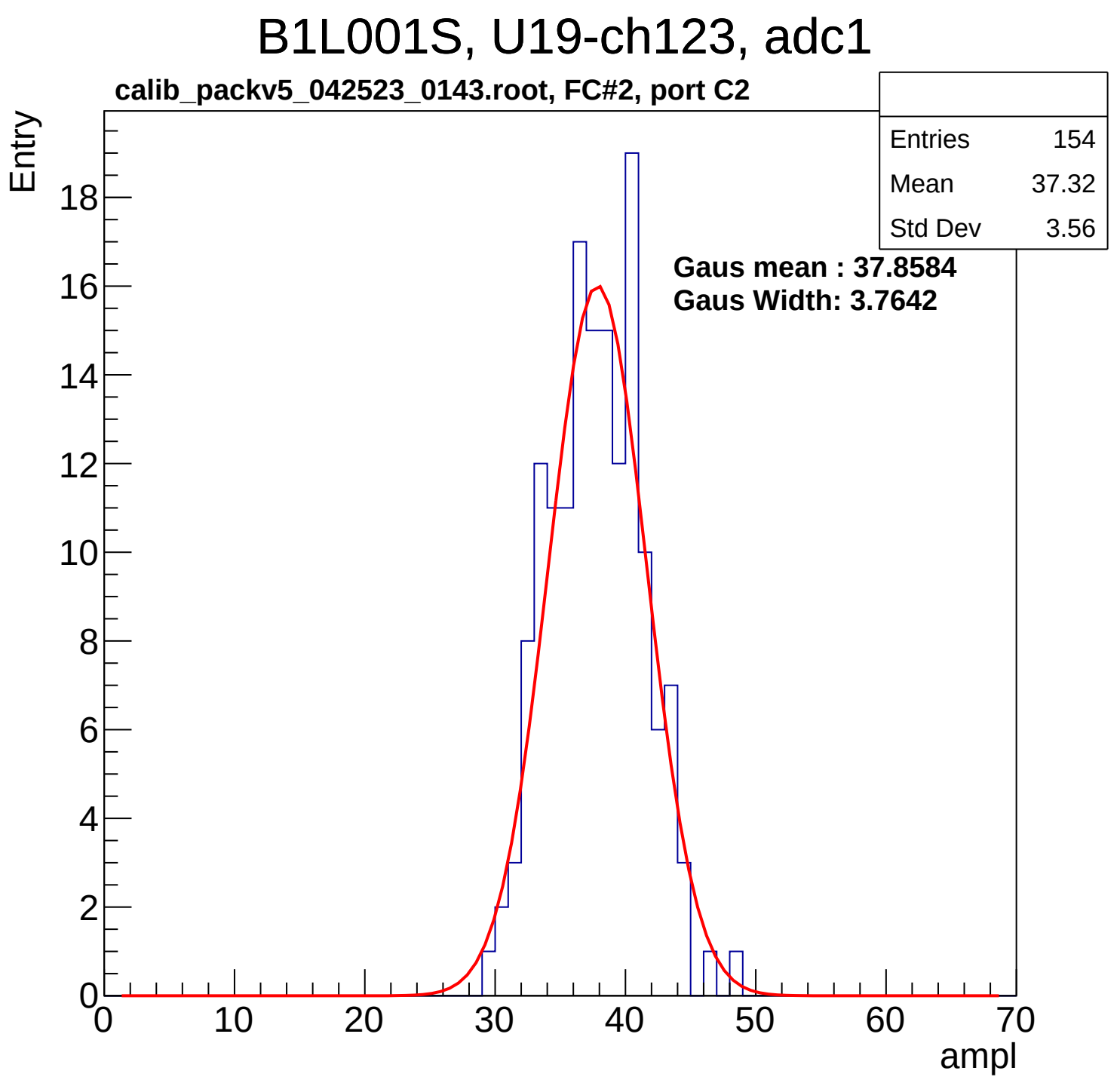
60
70


B1L001S, U19-ch123, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 154
Mean 37.32
Std Dev 3.56
Gaus mean : 37.8584
Gaus Width: 3.7642
Entry
ampl
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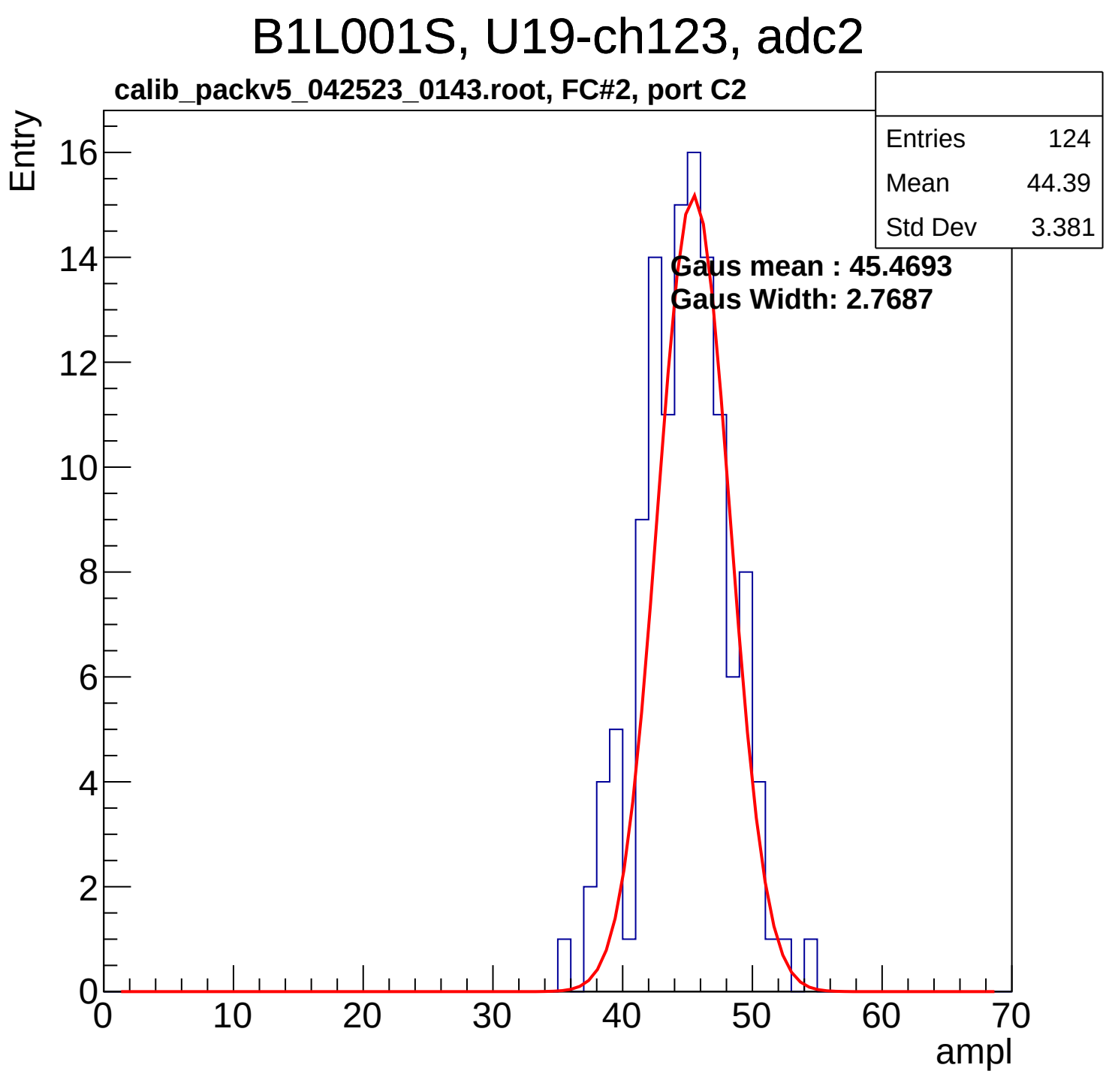
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70


B1L001S, U19-ch123, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 124
Mean 44.39
Std Dev 3.381
Gaus mean : 45.4693
Gaus Width: 2.7687
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
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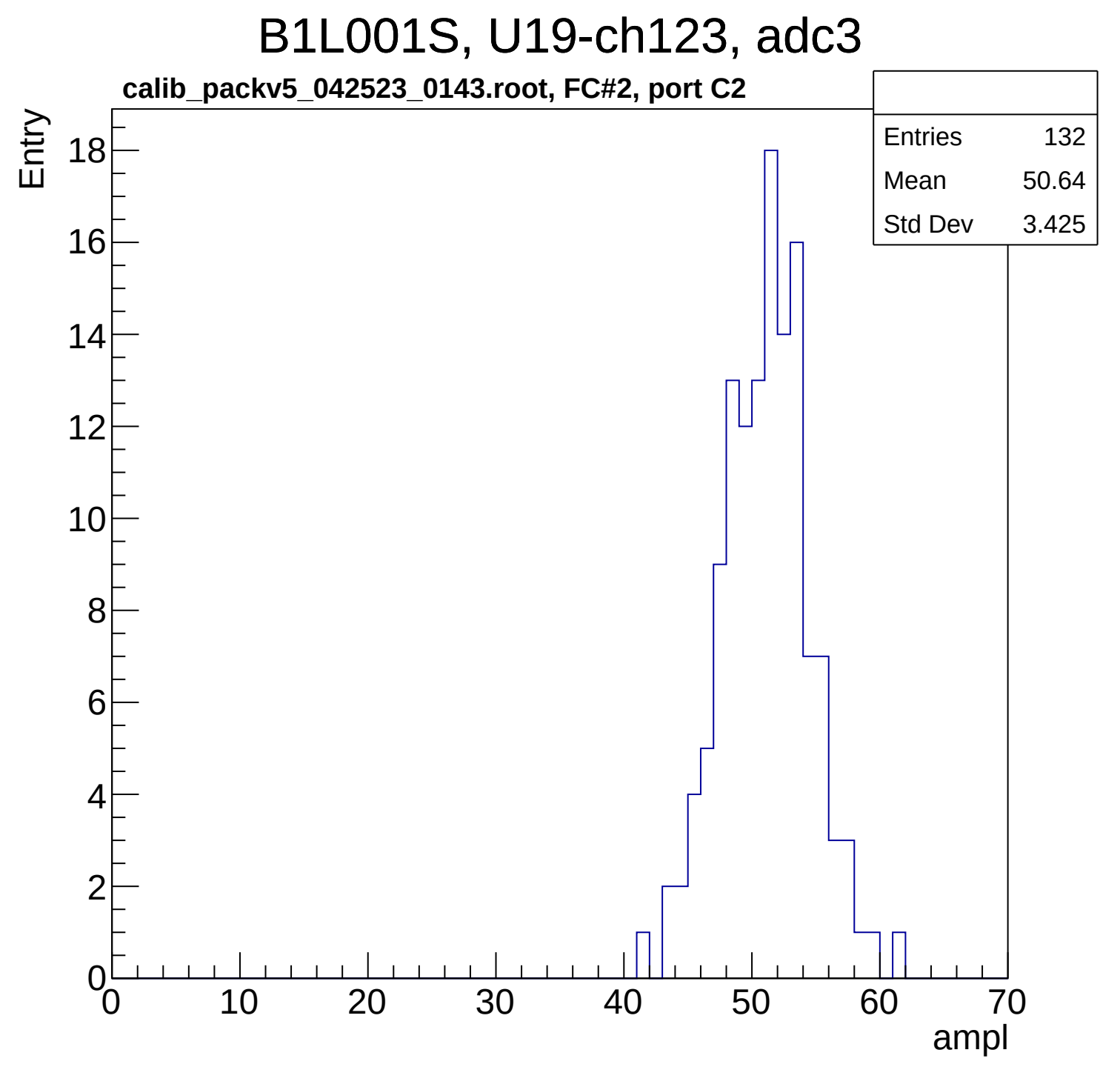
B1L001S, U19-ch123, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 132
Mean 50.64
Std Dev 3.425
Entry
ampl
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4
6
8
10
12
14
16
18
0
10
20
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40
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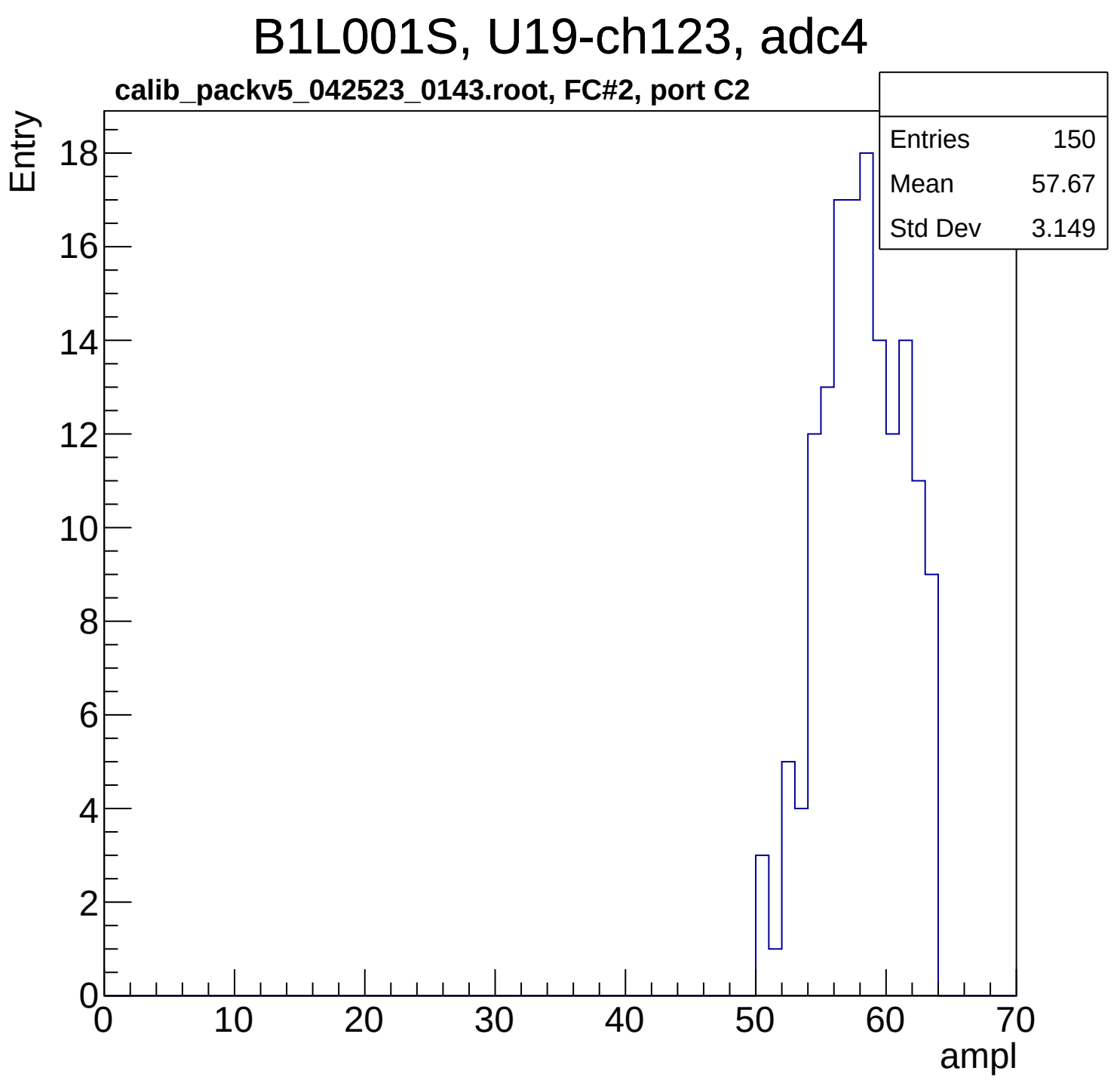
B1L001S, U19-ch123, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 150
Mean 57.67
Std Dev 3.149
Entry
ampl
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4
6
8
10
12
14
16
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0
10
20
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40
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60
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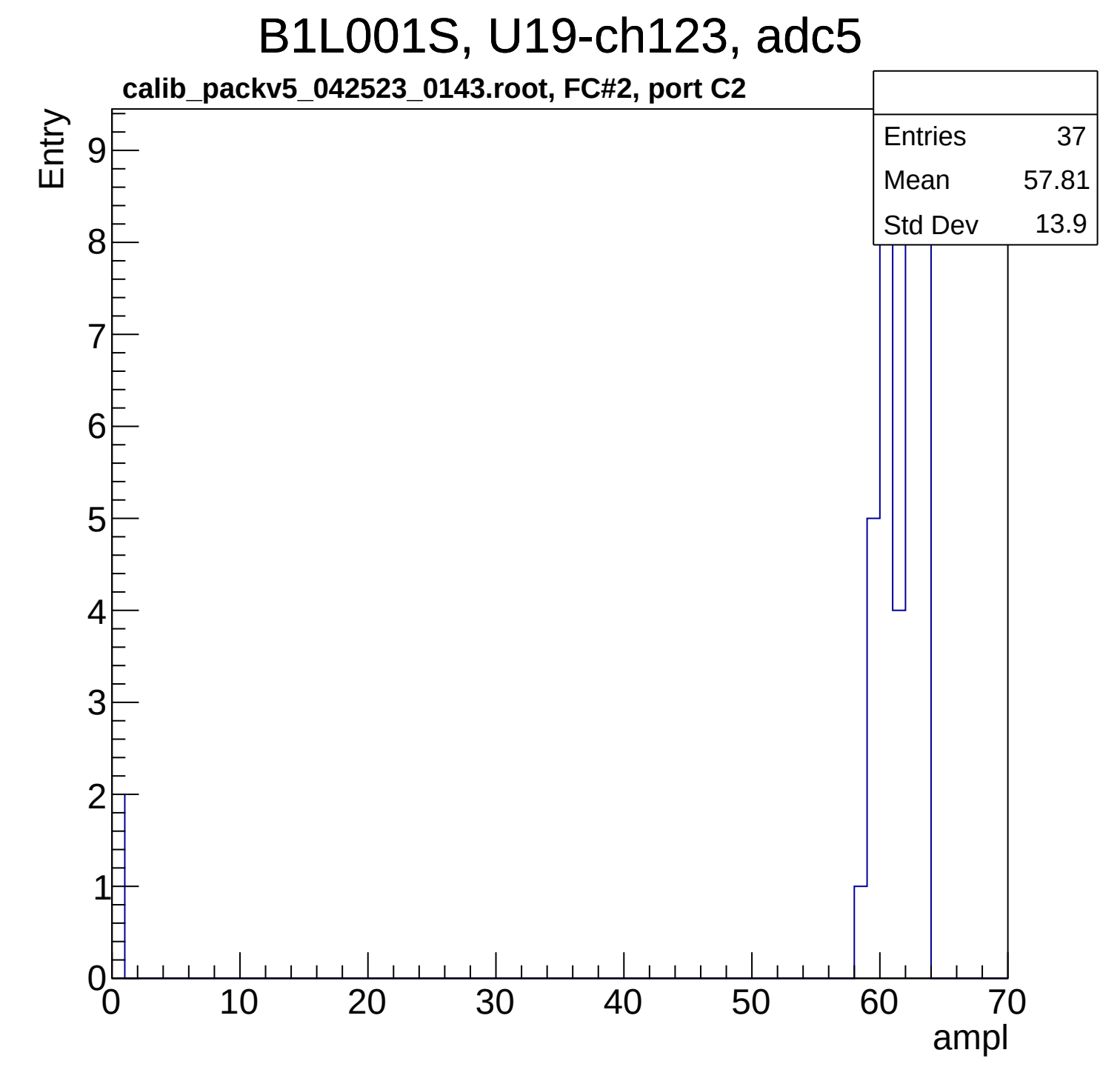
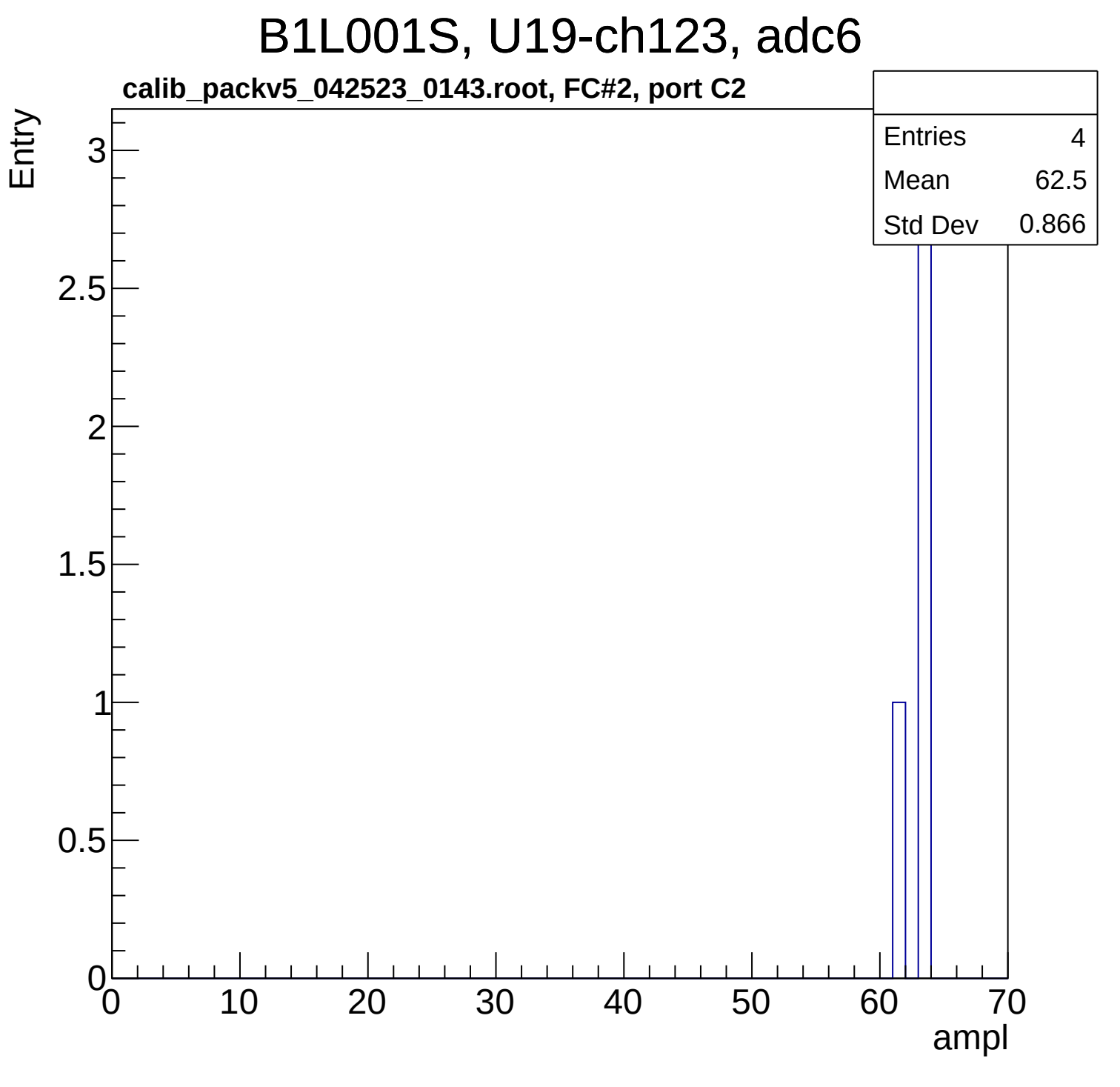

B1L001S, U19-ch123, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 37
Mean 57.81
Std Dev 13.9
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L001S, U19-ch123, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 4
Mean 62.5
Std Dev 0.866
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
10
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40
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60
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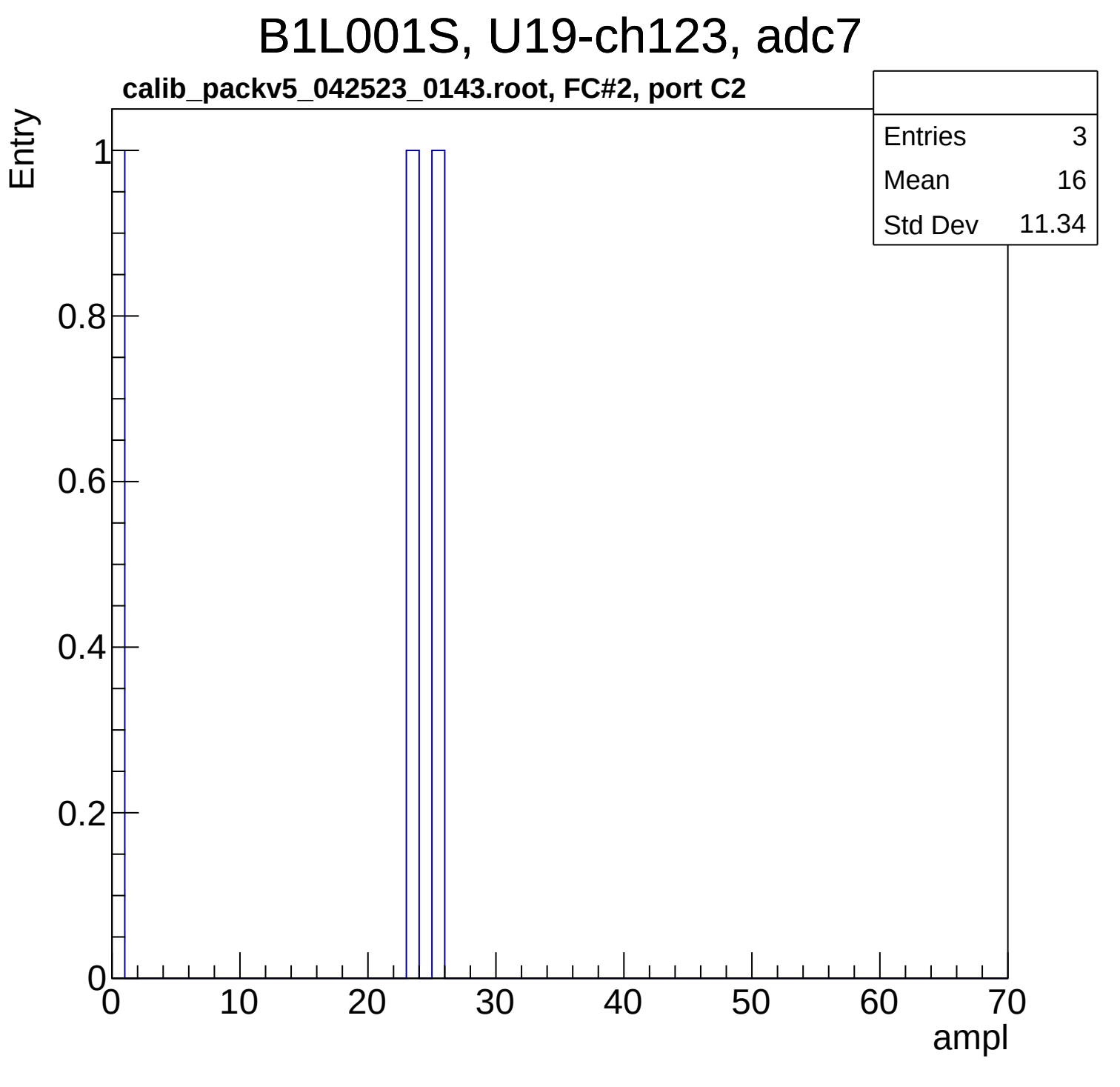
B1L001S, U19-ch123, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 3
Mean 16
Std Dev 11.34
Entry
ampl
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0.2
0.4
0.6
0.8
1
0
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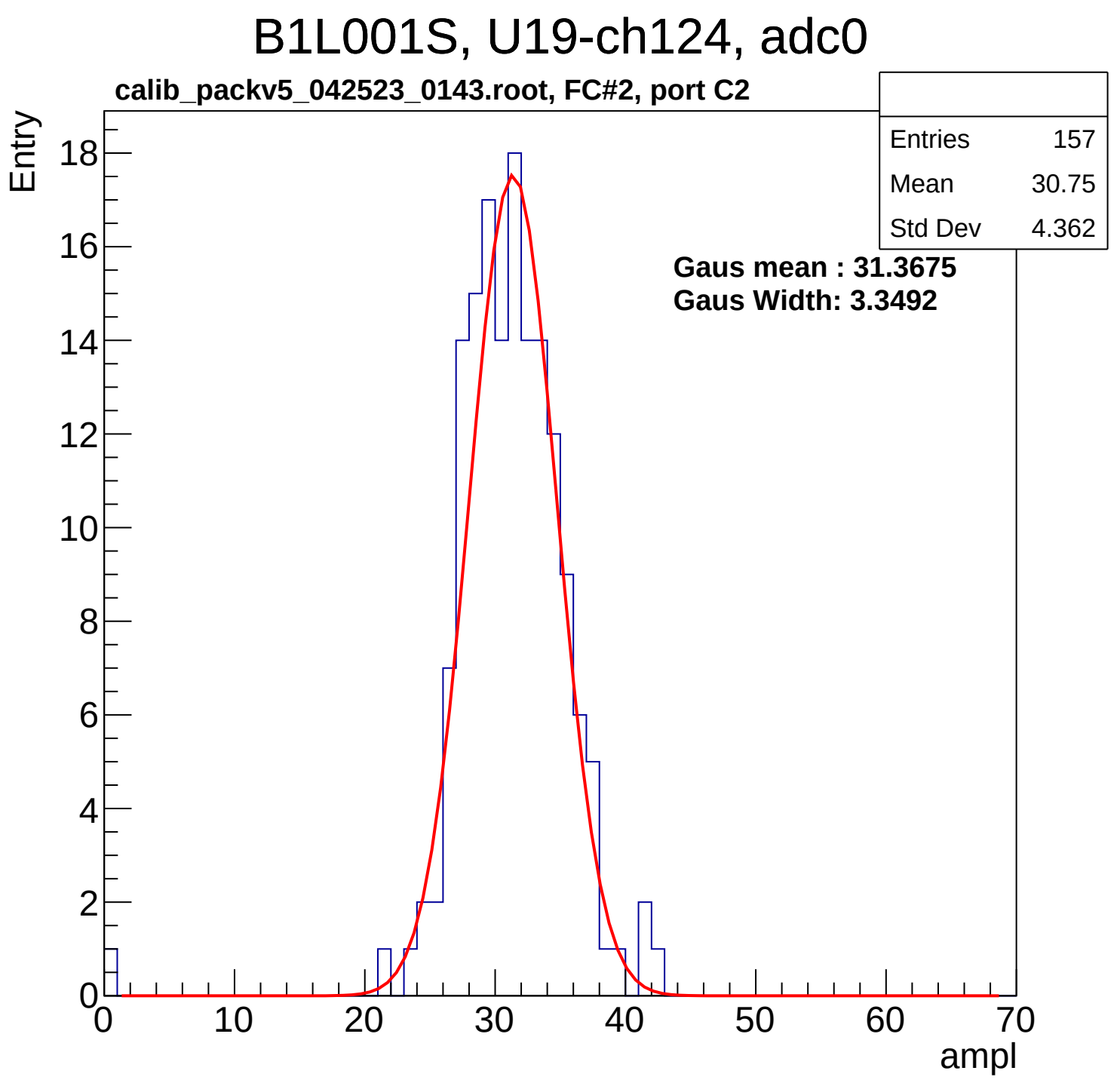
20
30
40
50
60
70


B1L001S, U19-ch124, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 157
Mean 30.75
Std Dev 4.362
Gaus mean : 31.3675
Gaus Width: 3.3492
Entry
ampl
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4
6
8
10
12
14
16
18
0
10
20
30
40
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60
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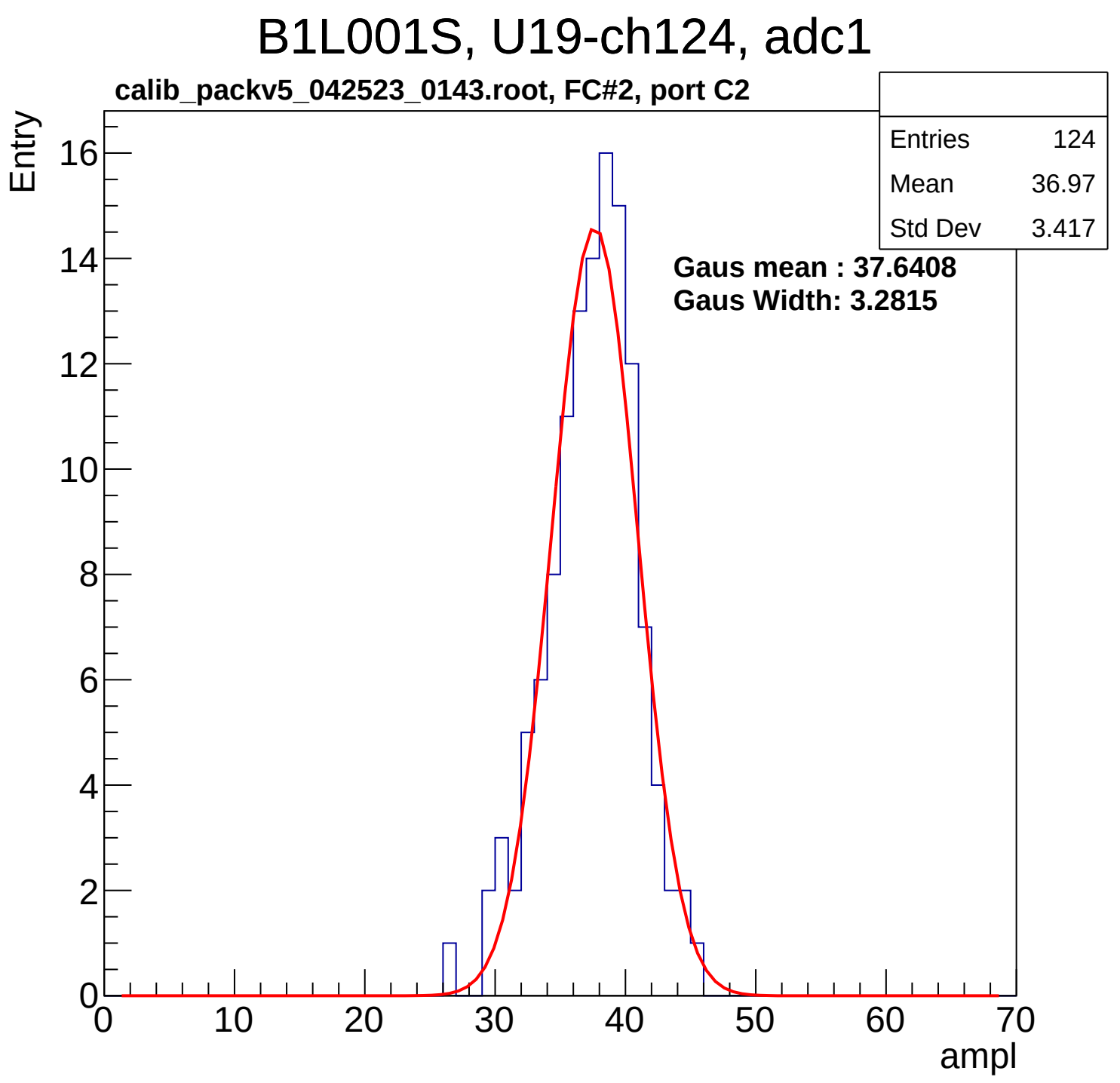
B1L001S, U19-ch124, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 124
Mean 36.97
Std Dev 3.417
Gaus mean : 37.6408
Gaus Width: 3.2815
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
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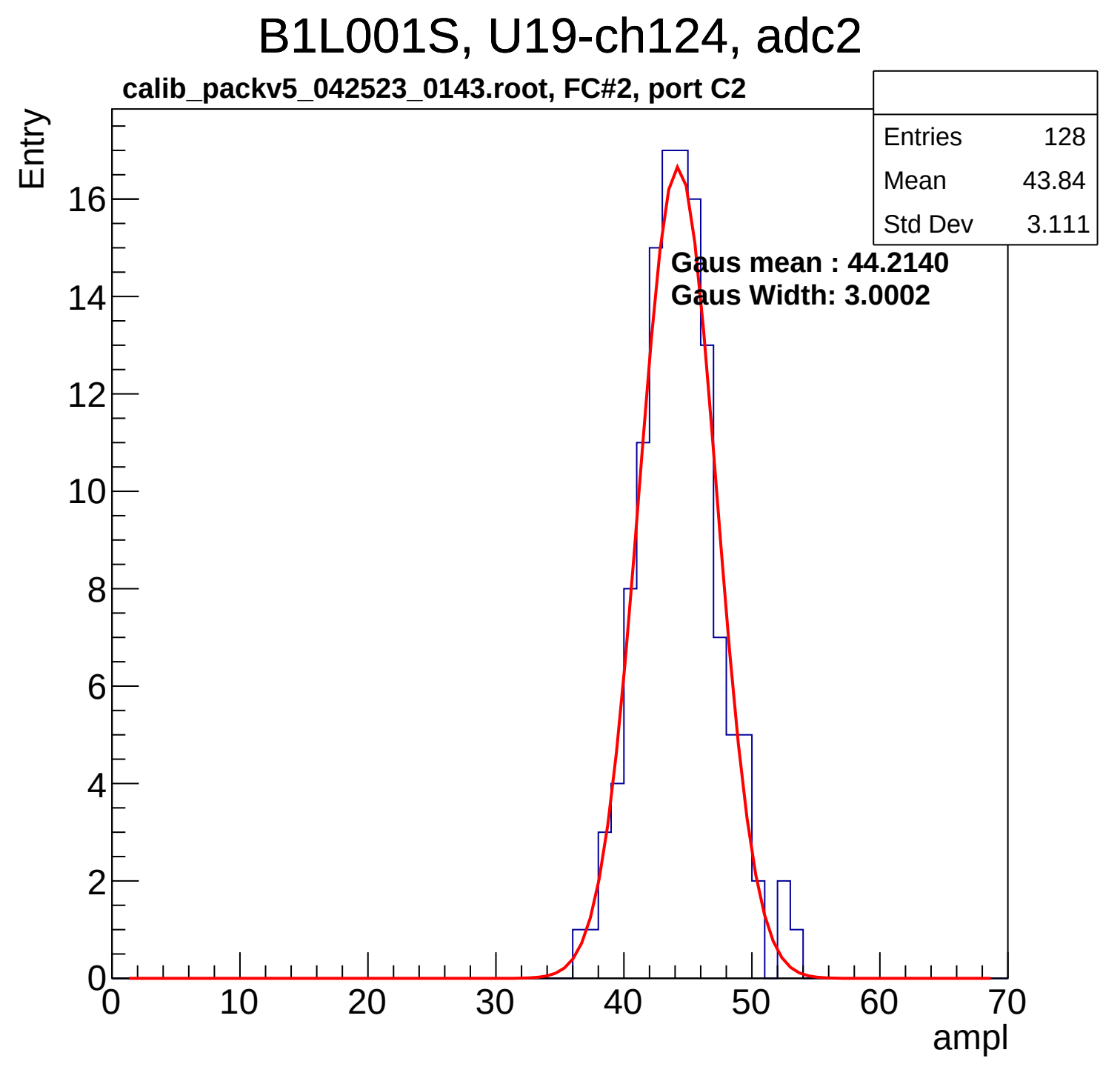
B1L001S, U19-ch124, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 128
Mean 43.84
Std Dev 3.111
Gaus mean : 44.2140
Gaus Width: 3.0002
Entry
ampl
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2
4
6
8
10
12
14
16
0
10
20
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40
50
60
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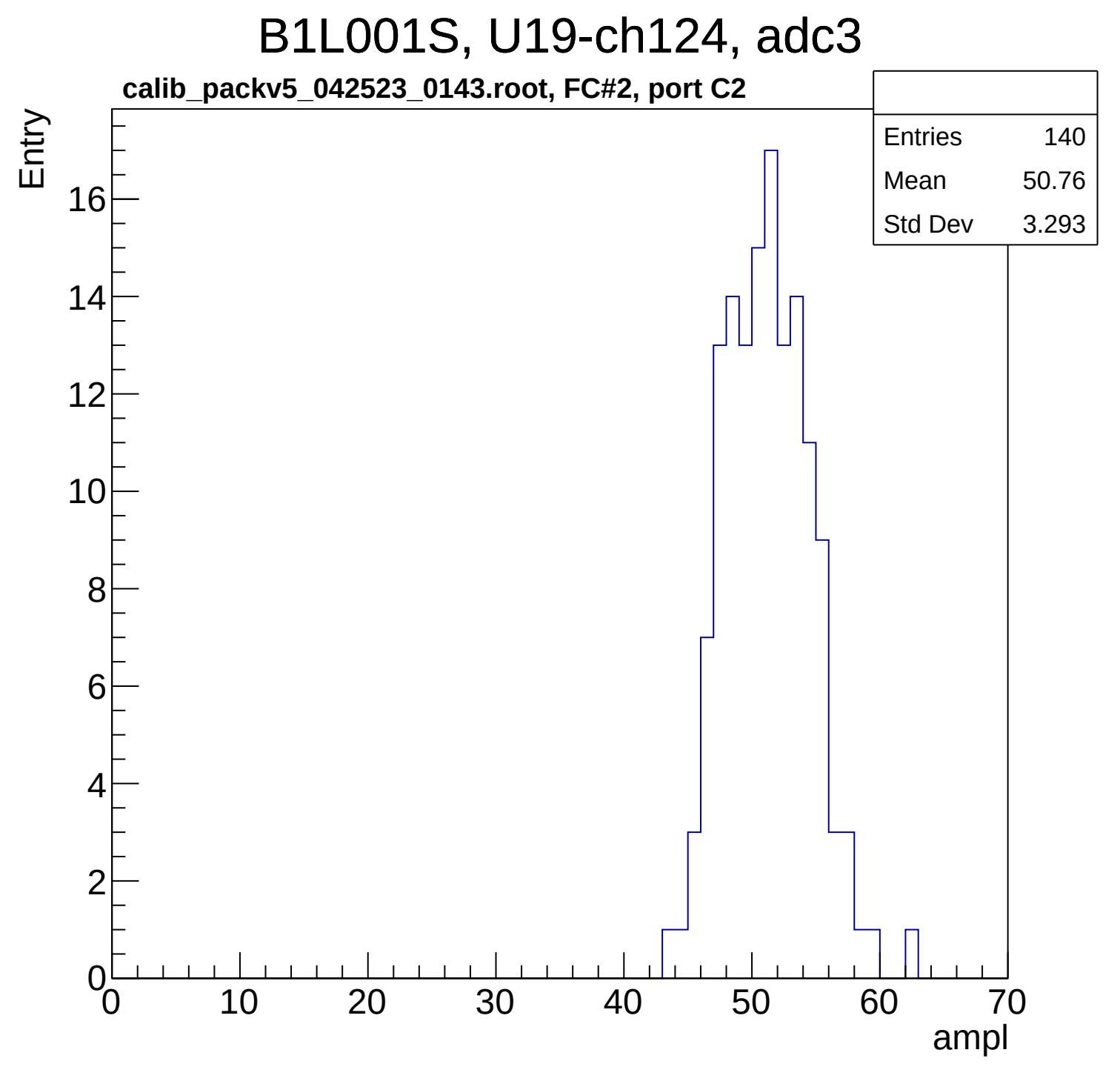
B1L001S, U19-ch124, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 140
Mean 50.76
Std Dev 3.293
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
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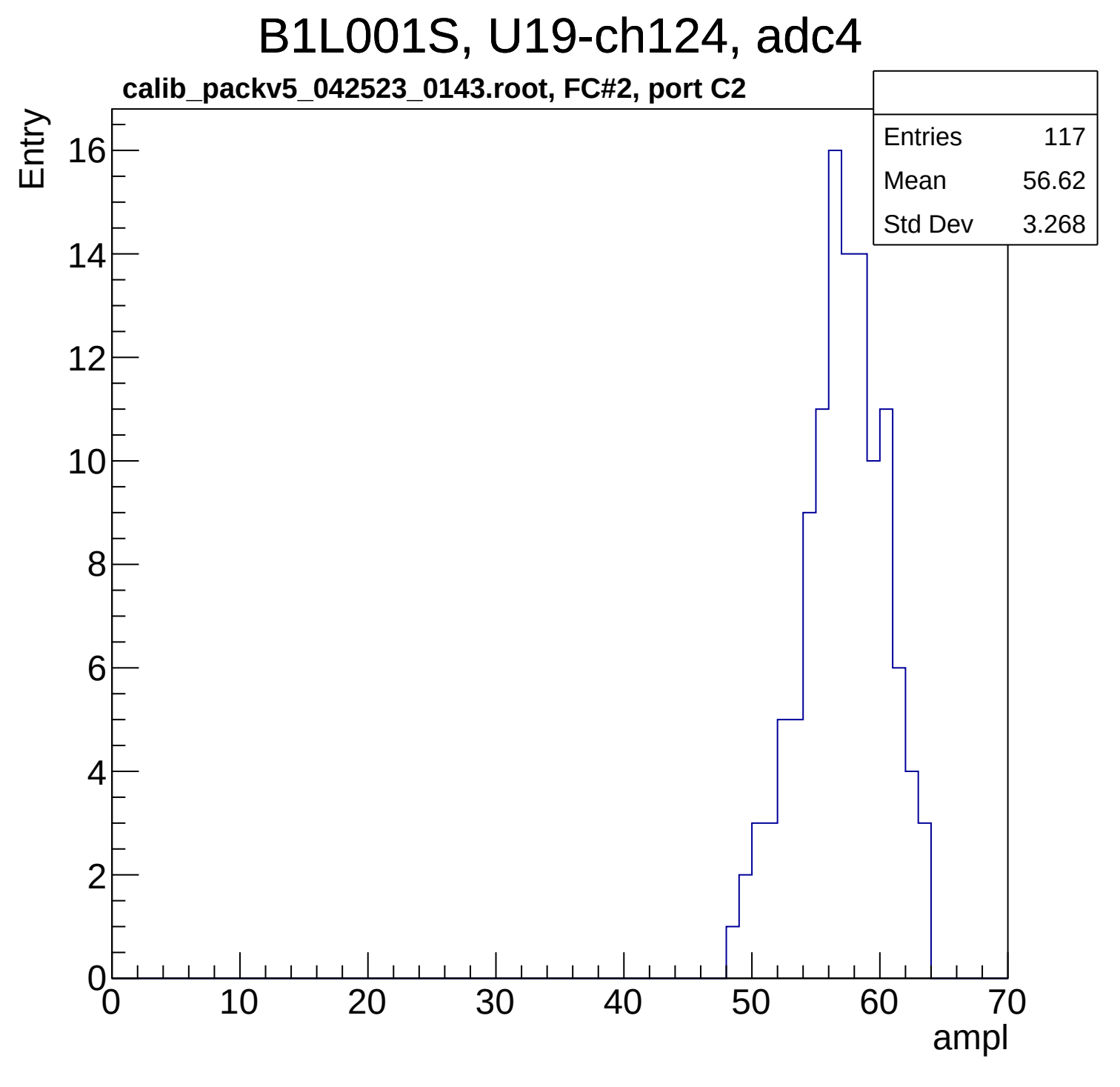
B1L001S, U19-ch124, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 117
Mean 56.62
Std Dev 3.268
Entry
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4
6
8
10
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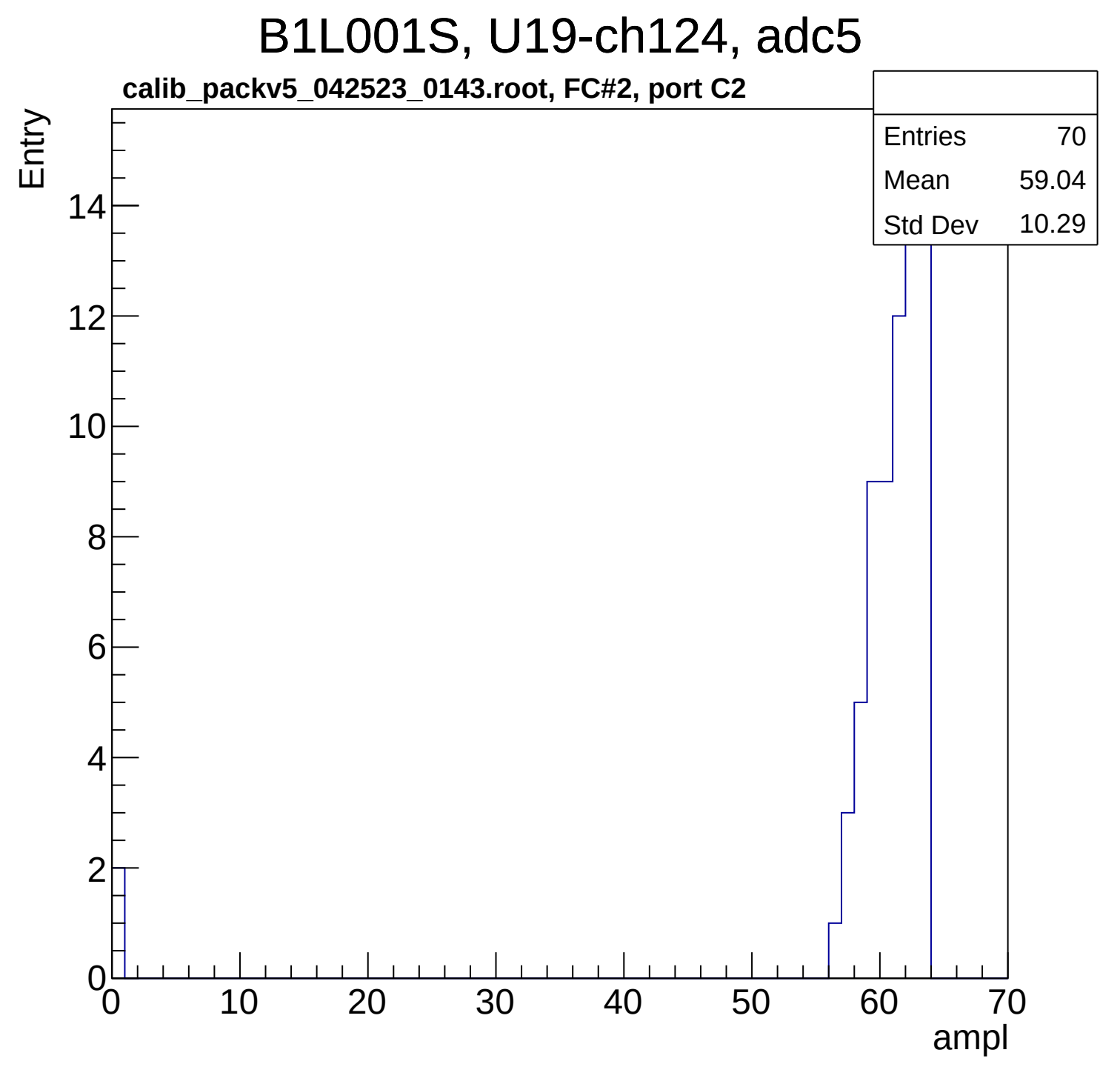
14
16
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch124, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 70
Mean 59.04
Std Dev 10.29
Entry
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6
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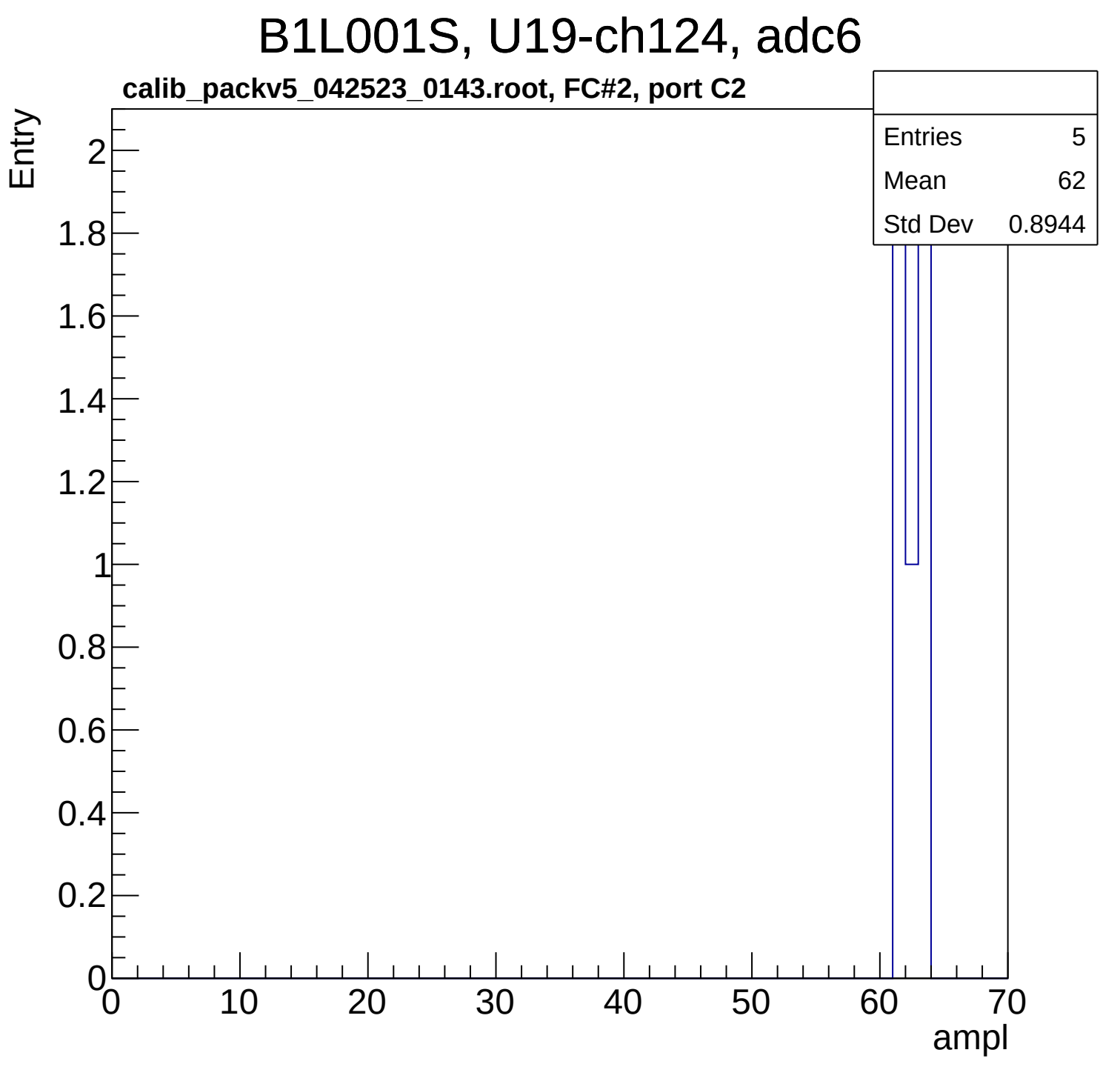
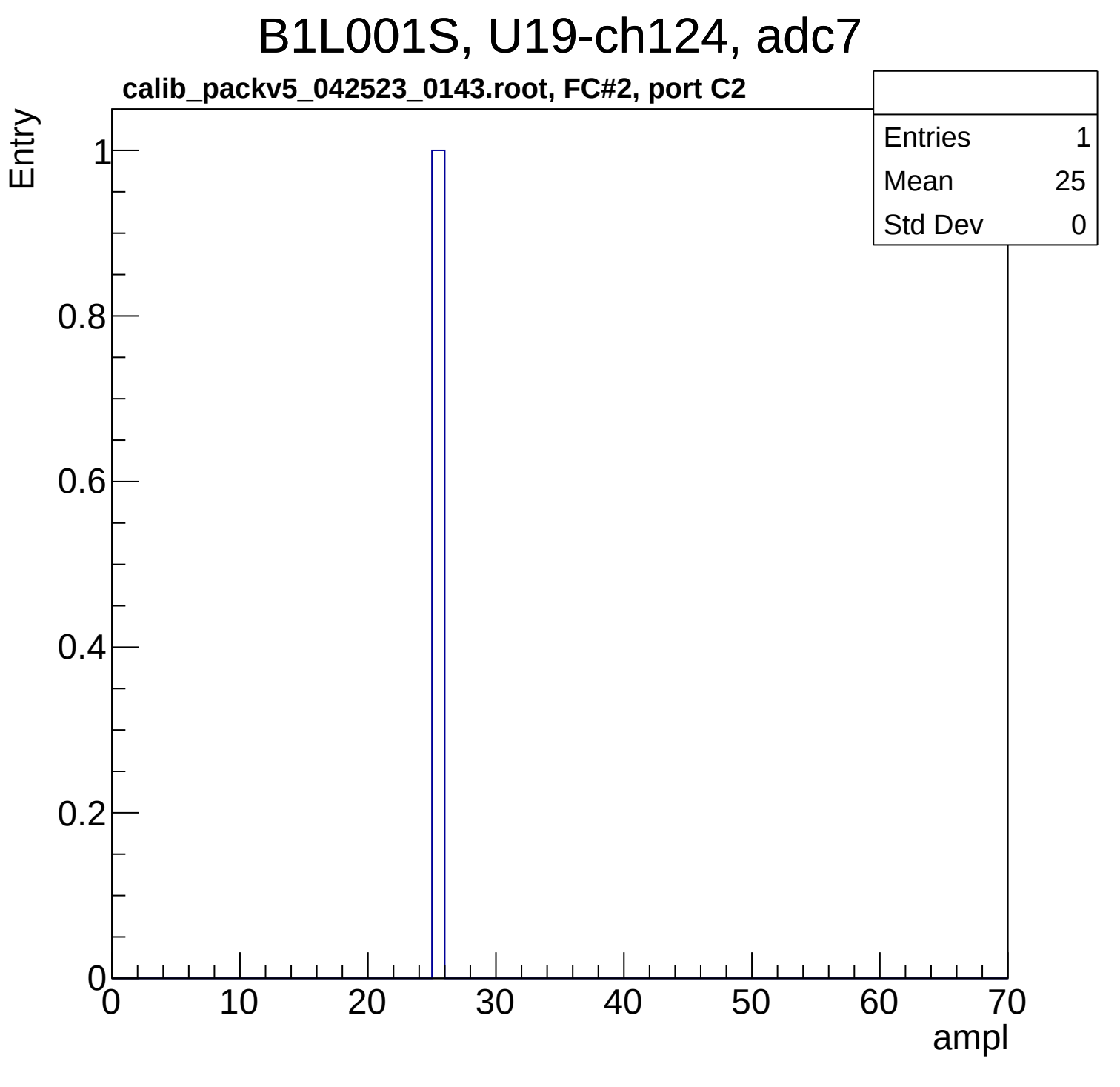
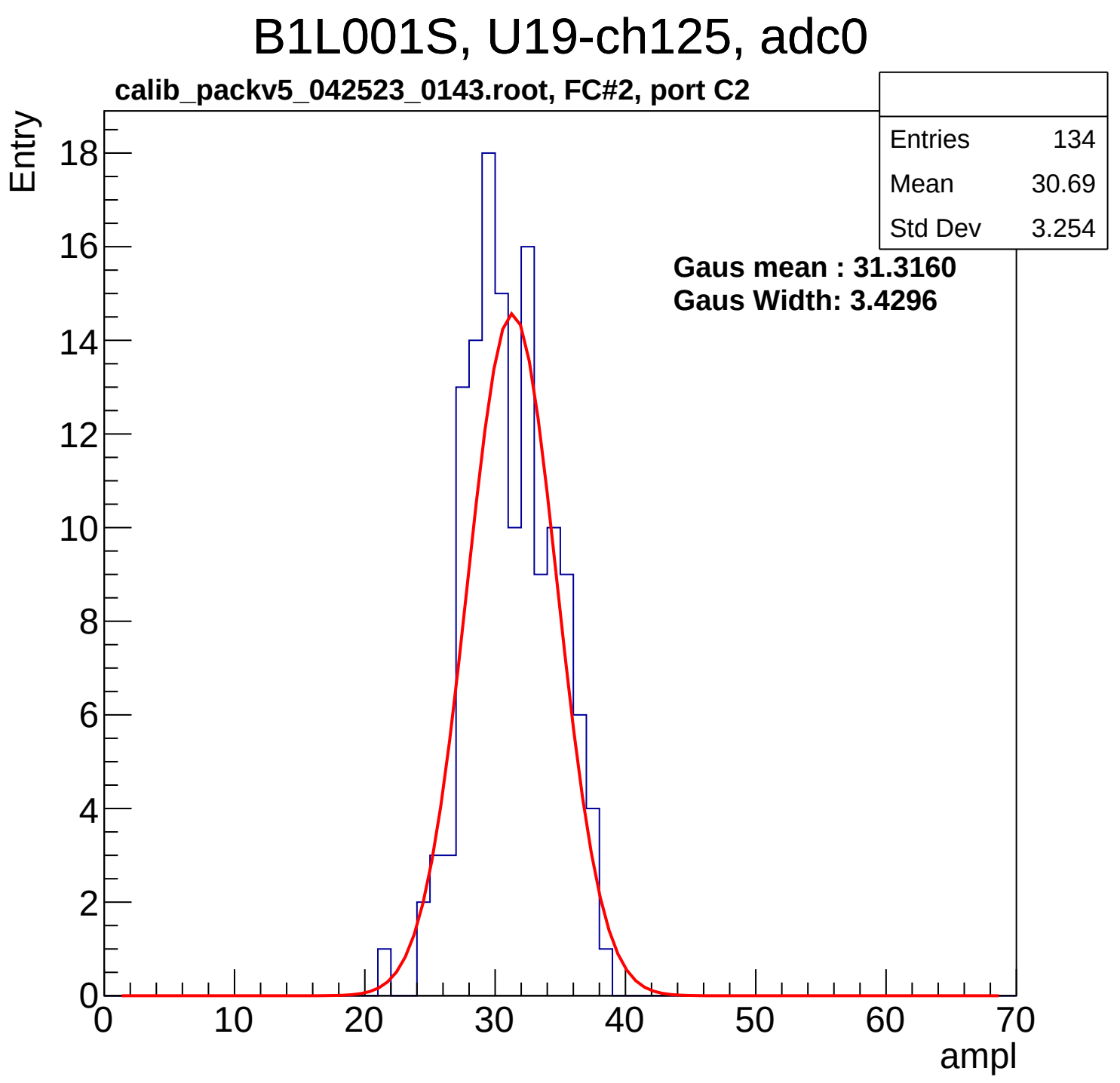
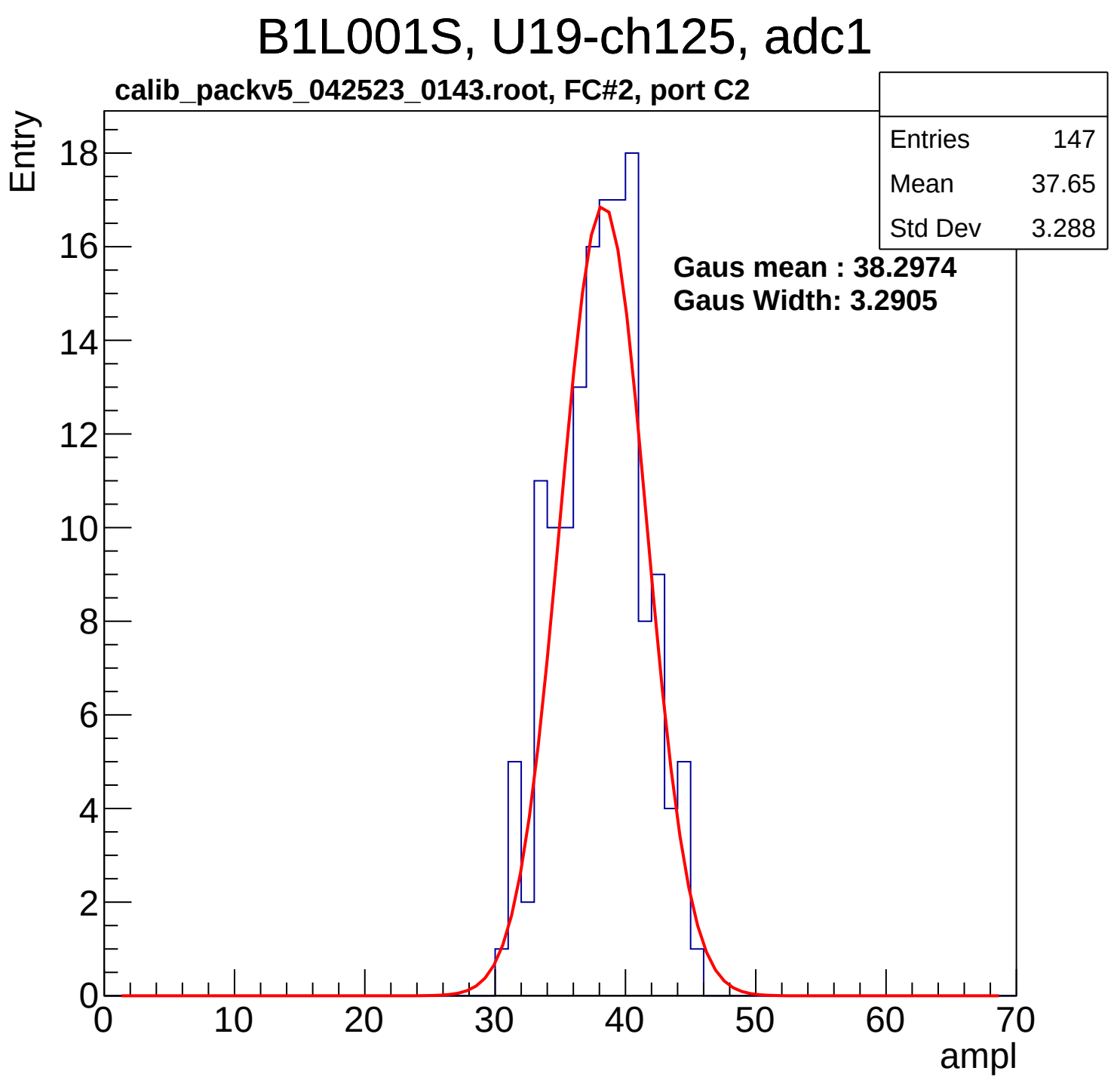
12
14
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch124, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 5
Mean 62
Std Dev 0.8944
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L001S, U19-ch124, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 25
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch125, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 134
Mean 30.69
Std Dev 3.254
Gaus mean : 31.3160
Gaus Width: 3.4296
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70


B1L001S, U19-ch125, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 147
Mean 37.65
Std Dev 3.288
Gaus mean : 38.2974
Gaus Width: 3.2905
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
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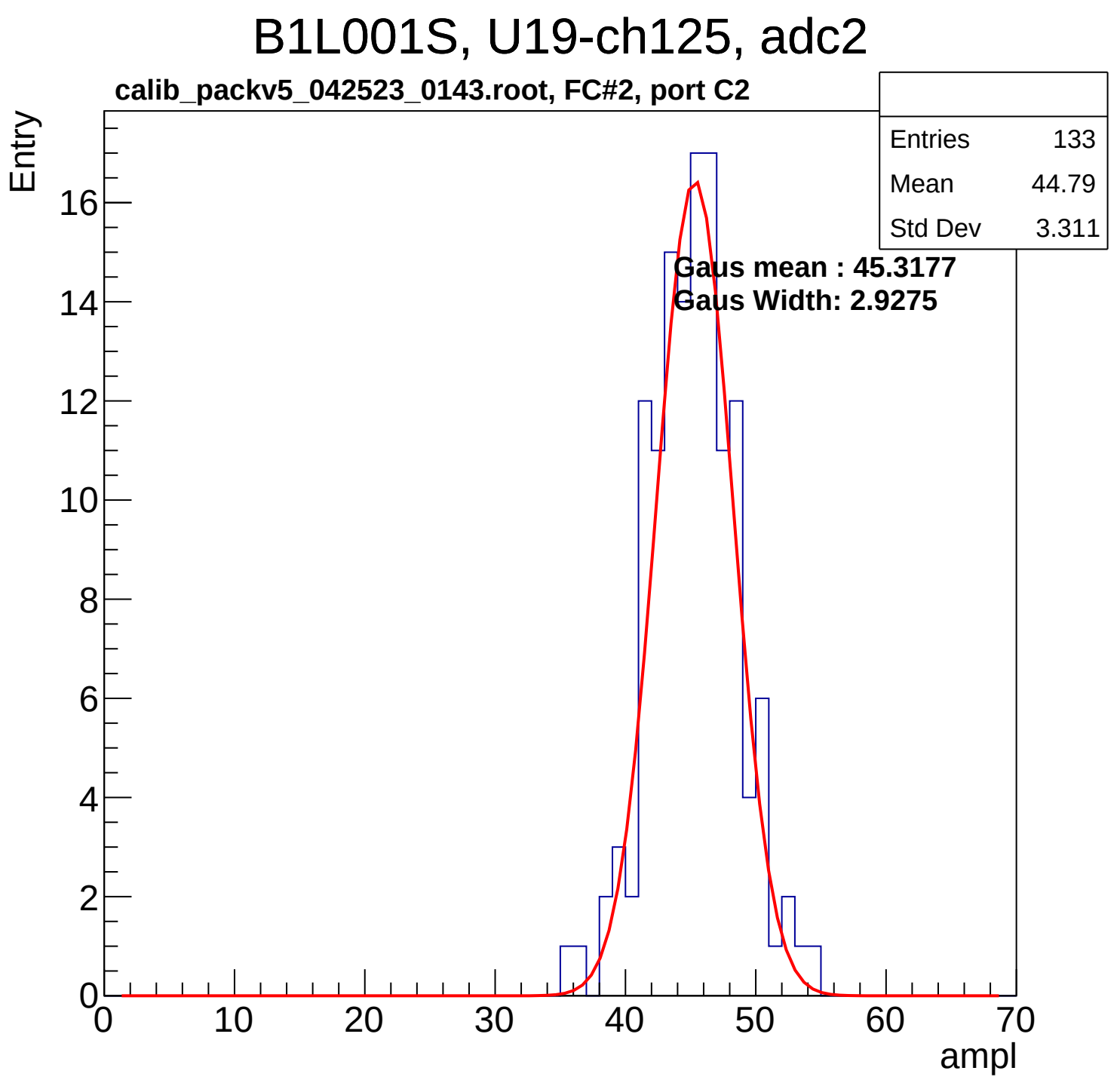
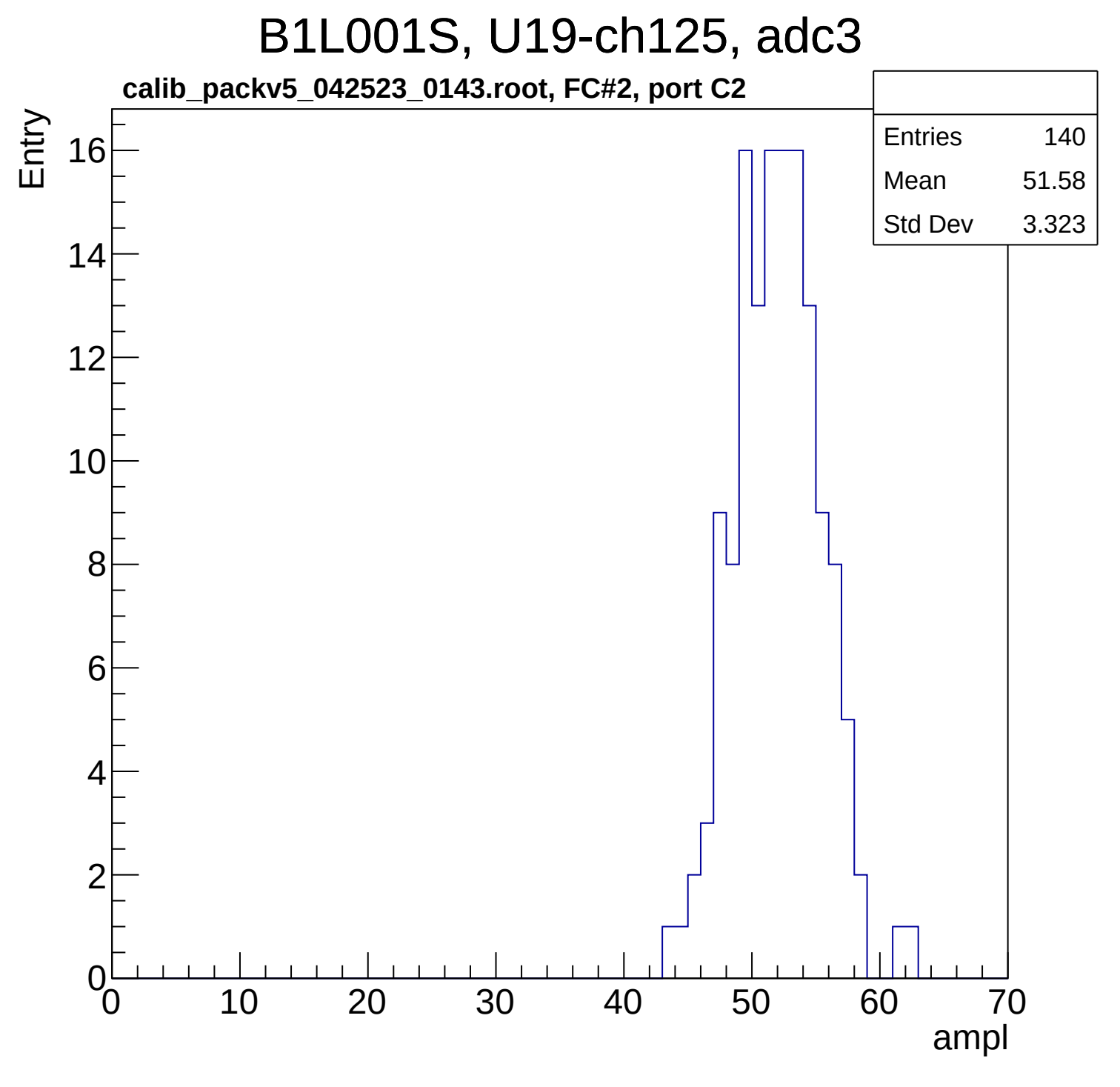

B1L001S, U19-ch125, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 133
Mean 44.79
Std Dev 3.311
Gaus mean : 45.3177
Gaus Width: 2.9275
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70


B1L001S, U19-ch125, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 140
Mean 51.58
Std Dev 3.323
Entry
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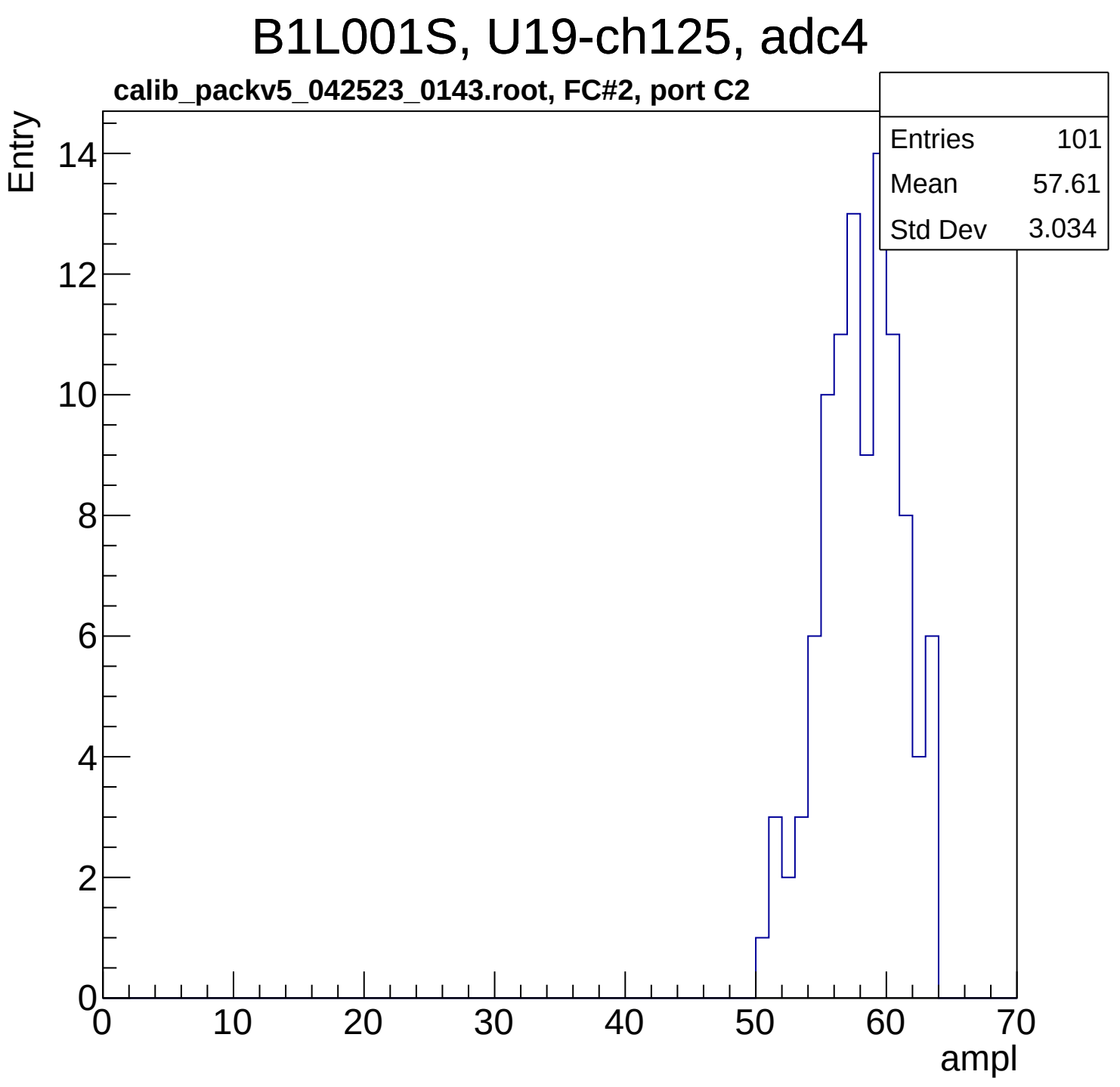
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch125, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 101
Mean 57.61
Std Dev 3.034
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
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60
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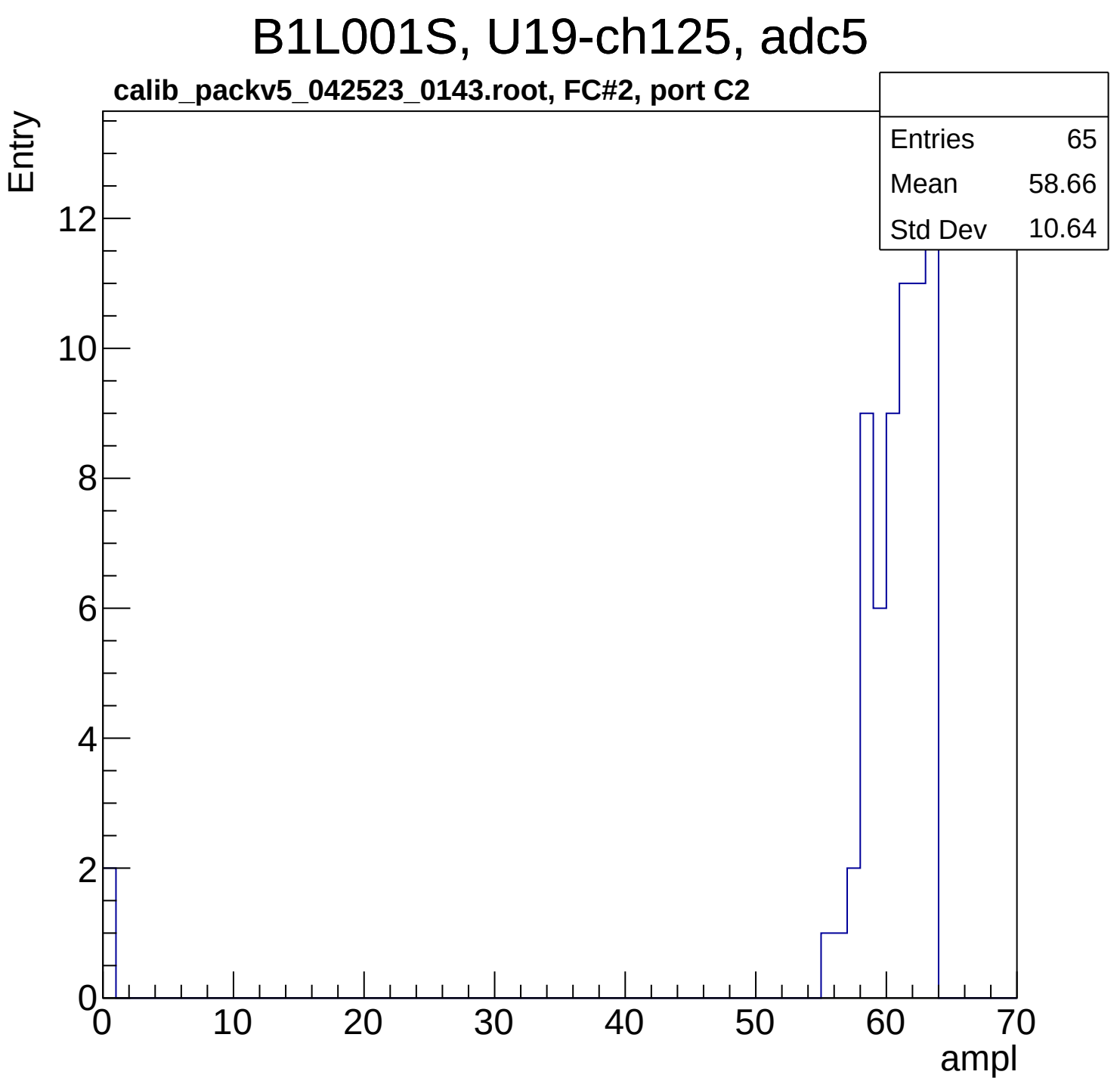
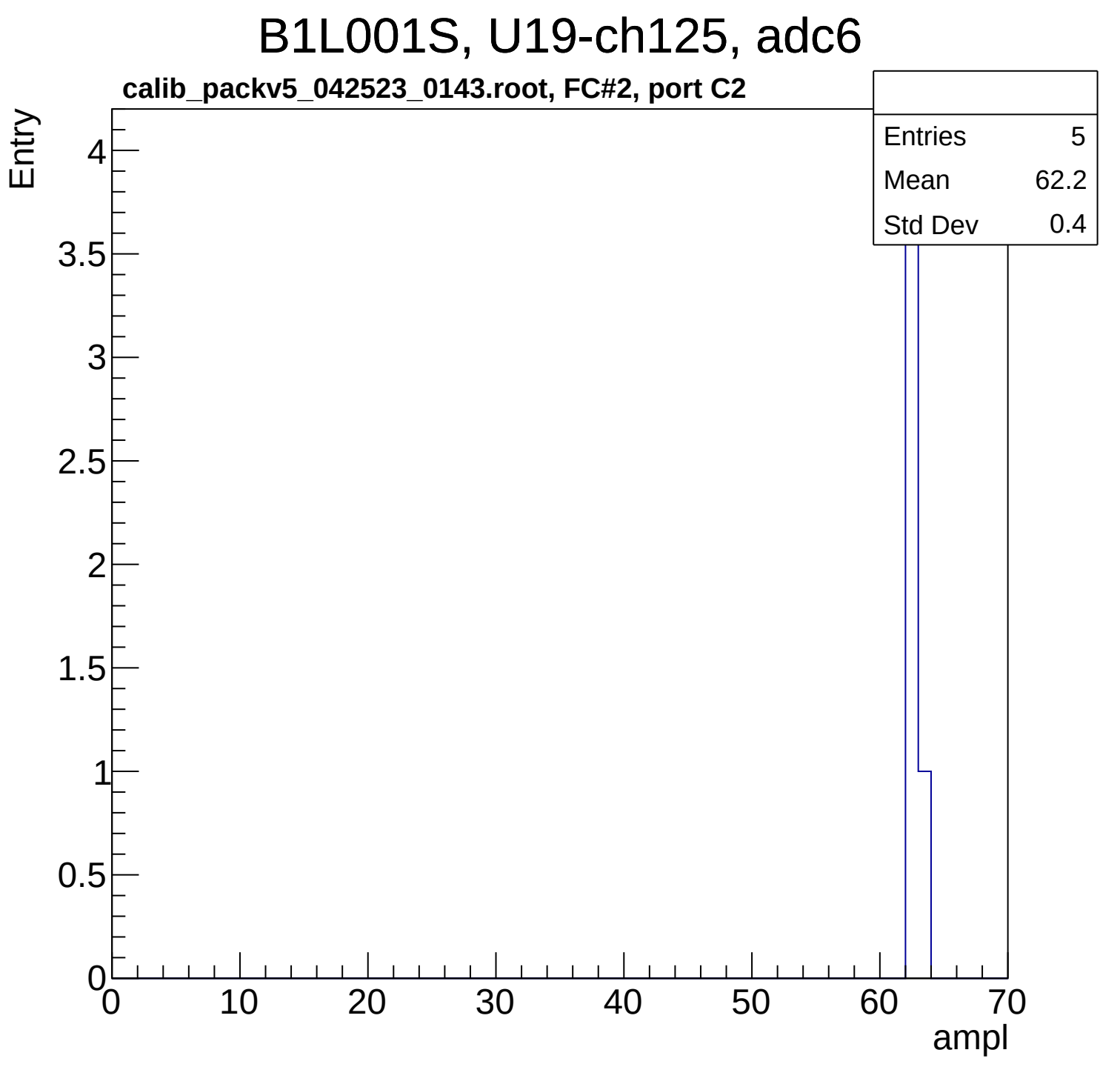
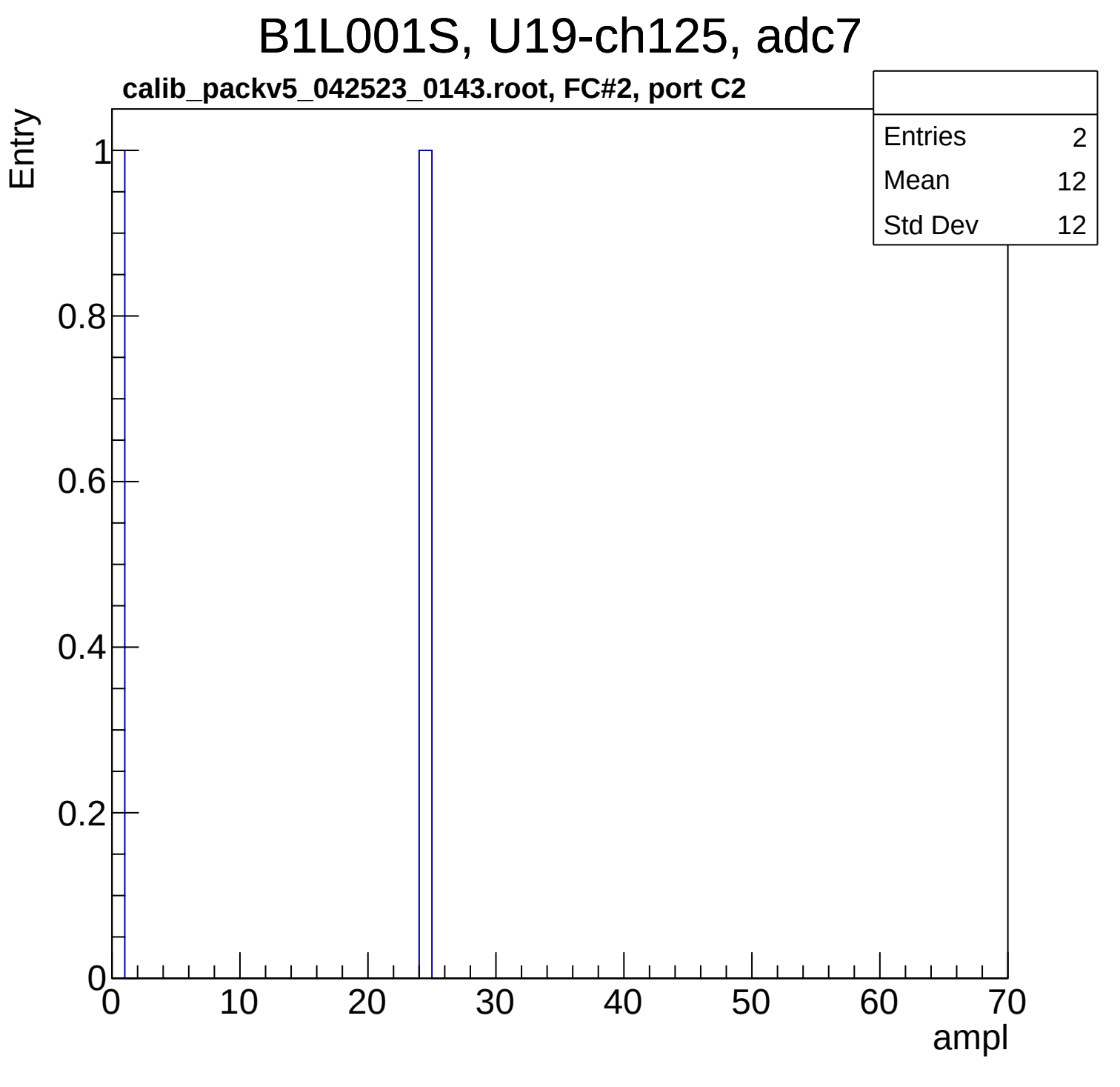

B1L001S, U19-ch125, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 65
Mean 58.66
Std Dev 10.64
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch125, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 5
Mean 62.2
Std Dev 0.4
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L001S, U19-ch125, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 12
Std Dev 12
Entry
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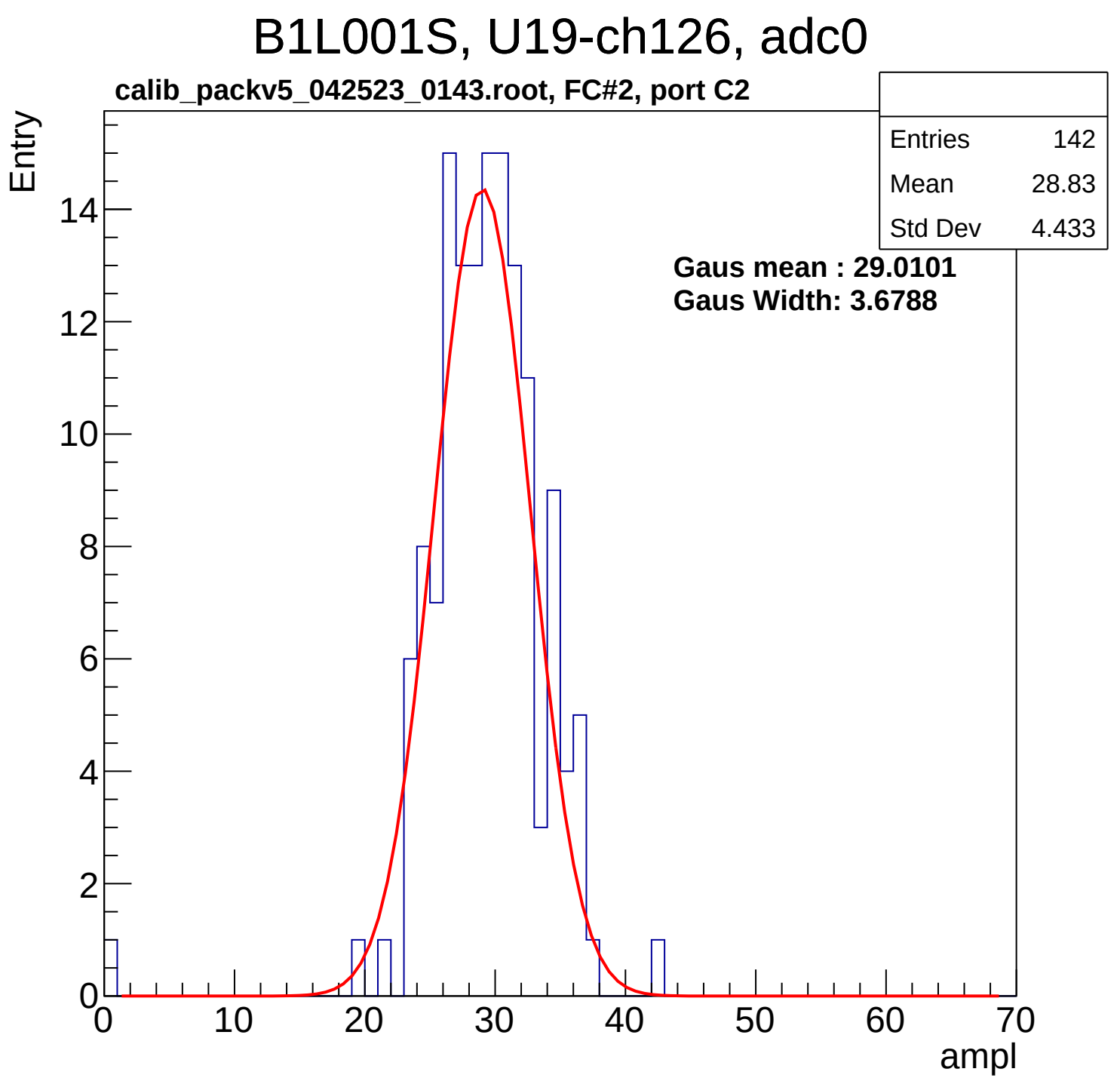
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch126, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 142
Mean 28.83
Std Dev 4.433
Gaus mean : 29.0101
Gaus Width: 3.6788
Entry
ampl
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2
4
6
8
10
12
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0
10
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60
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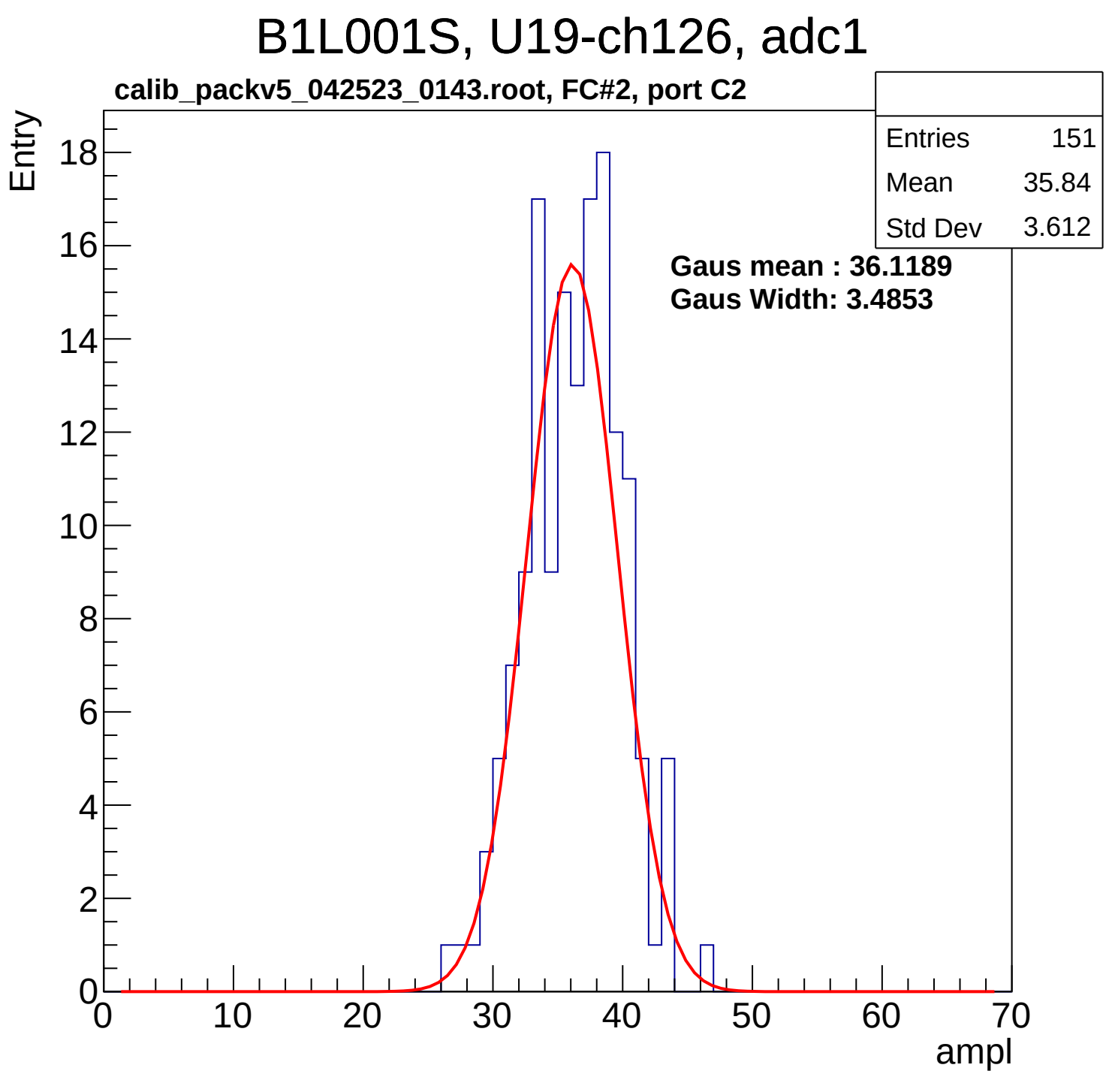
B1L001S, U19-ch126, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 151
Mean 35.84
Std Dev 3.612
Gaus mean : 36.1189
Gaus Width: 3.4853
Entry
ampl
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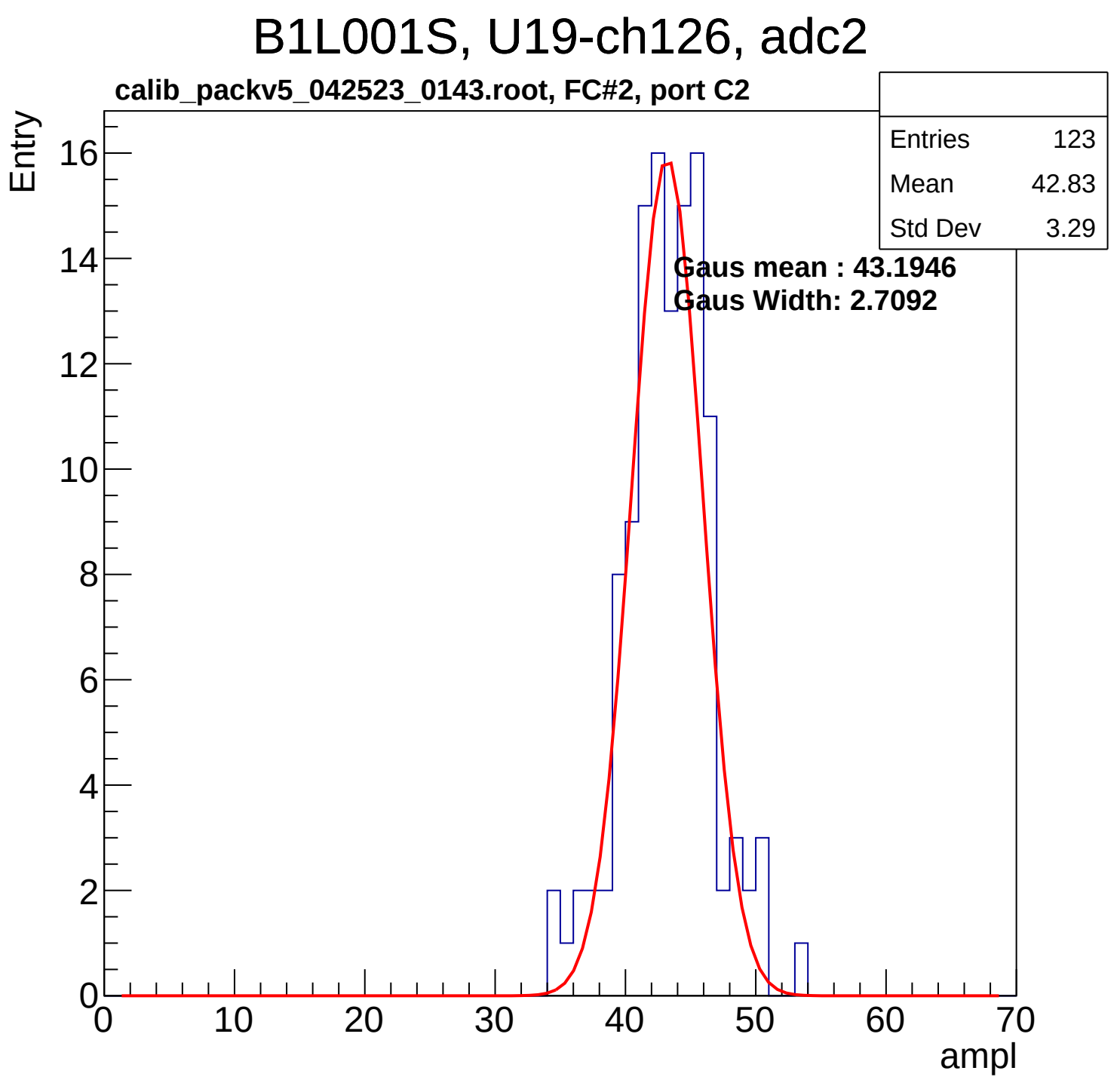
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70


B1L001S, U19-ch126, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 123
Mean 42.83
Std Dev 3.29
Gaus mean : 43.1946
Gaus Width: 2.7092
Entry
ampl
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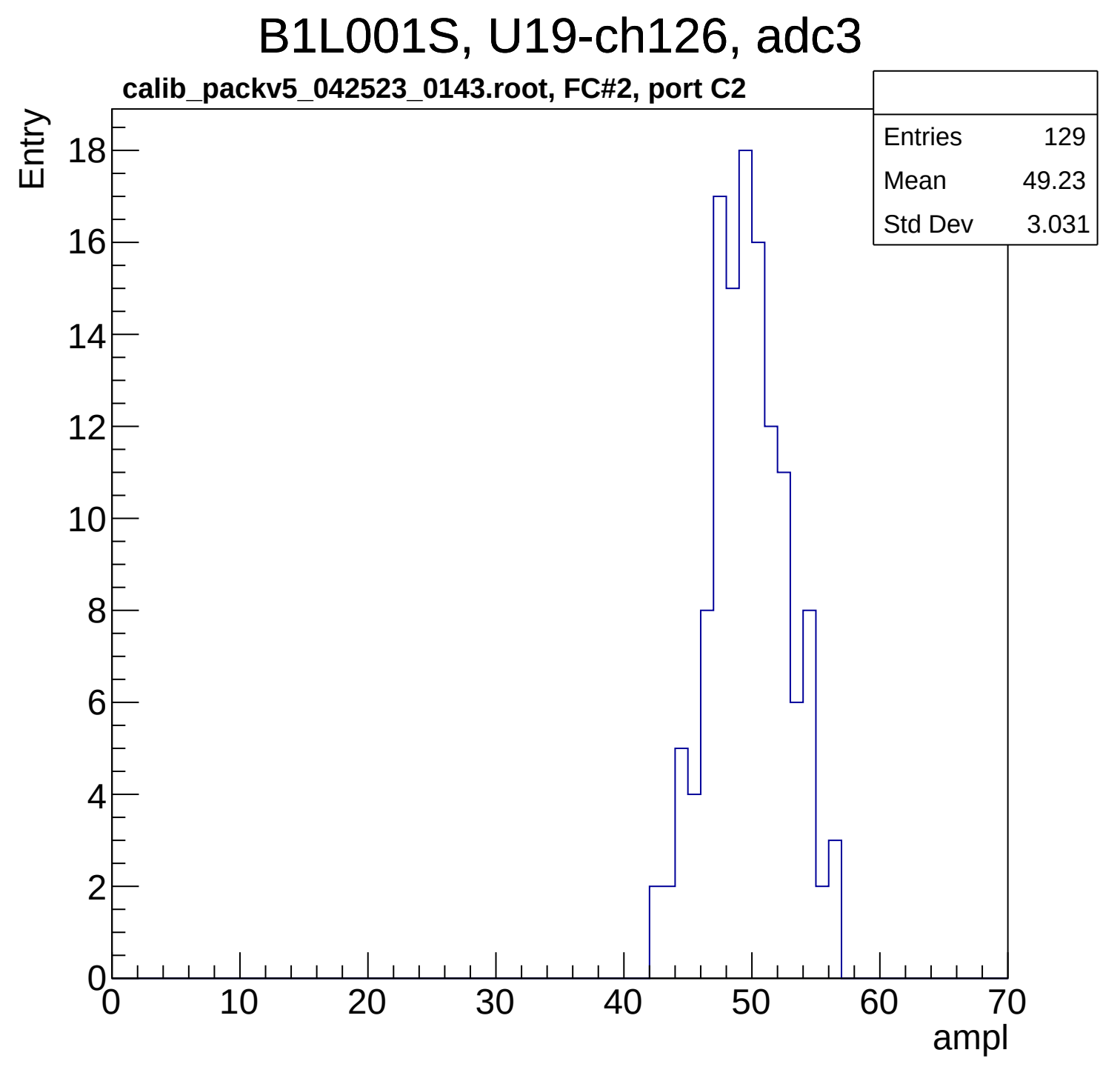
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70


B1L001S, U19-ch126, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 129
Mean 49.23
Std Dev 3.031
Entry
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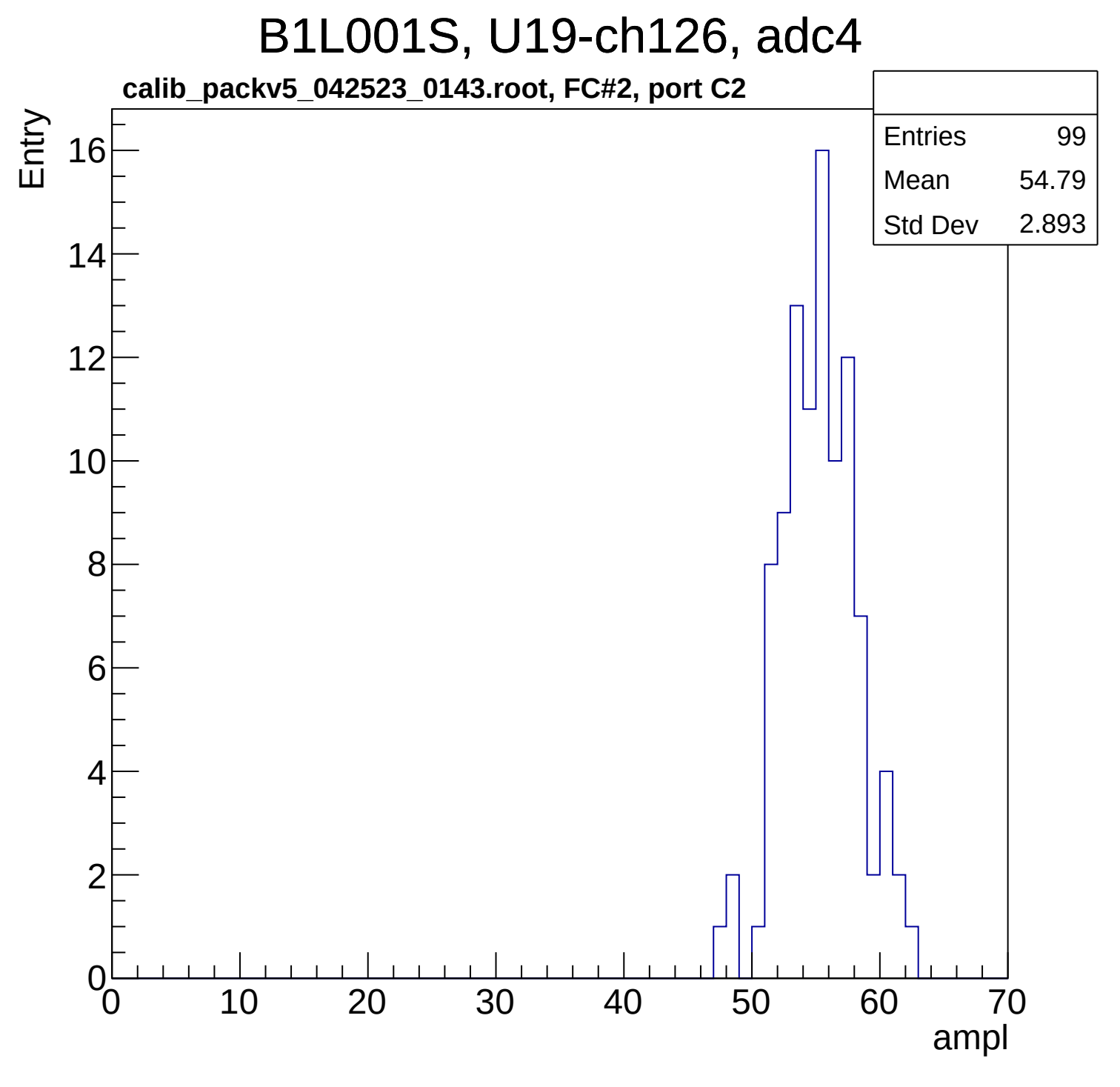
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch126, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 99
Mean 54.79
Std Dev 2.893
Entry
ampl
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2
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8
10
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14
16
0
10
20
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40
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60
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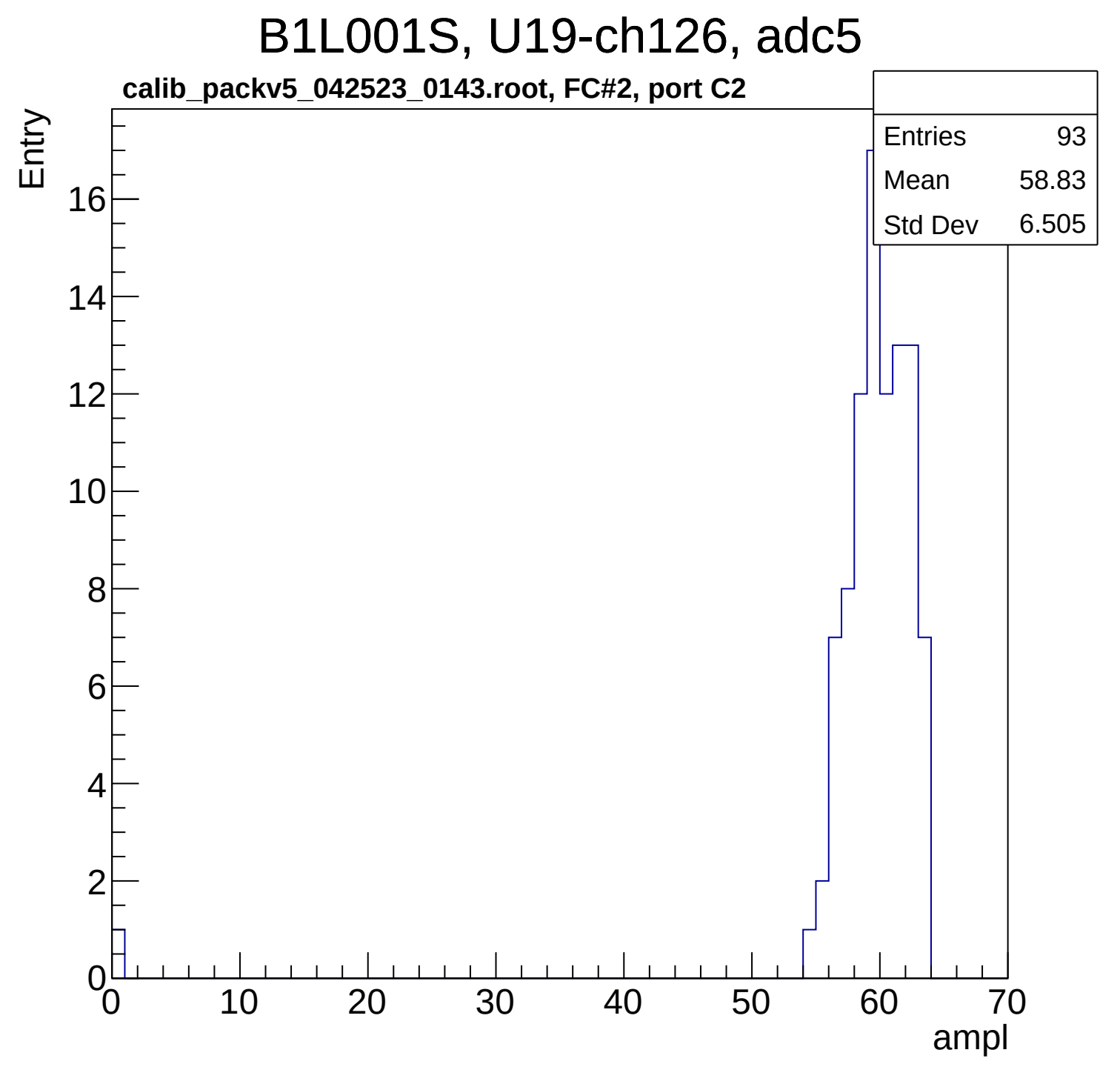
B1L001S, U19-ch126, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 93
Mean 58.83
Std Dev 6.505
Entry
ampl
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4
6
8
10
12
14
16
0
10
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40
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60
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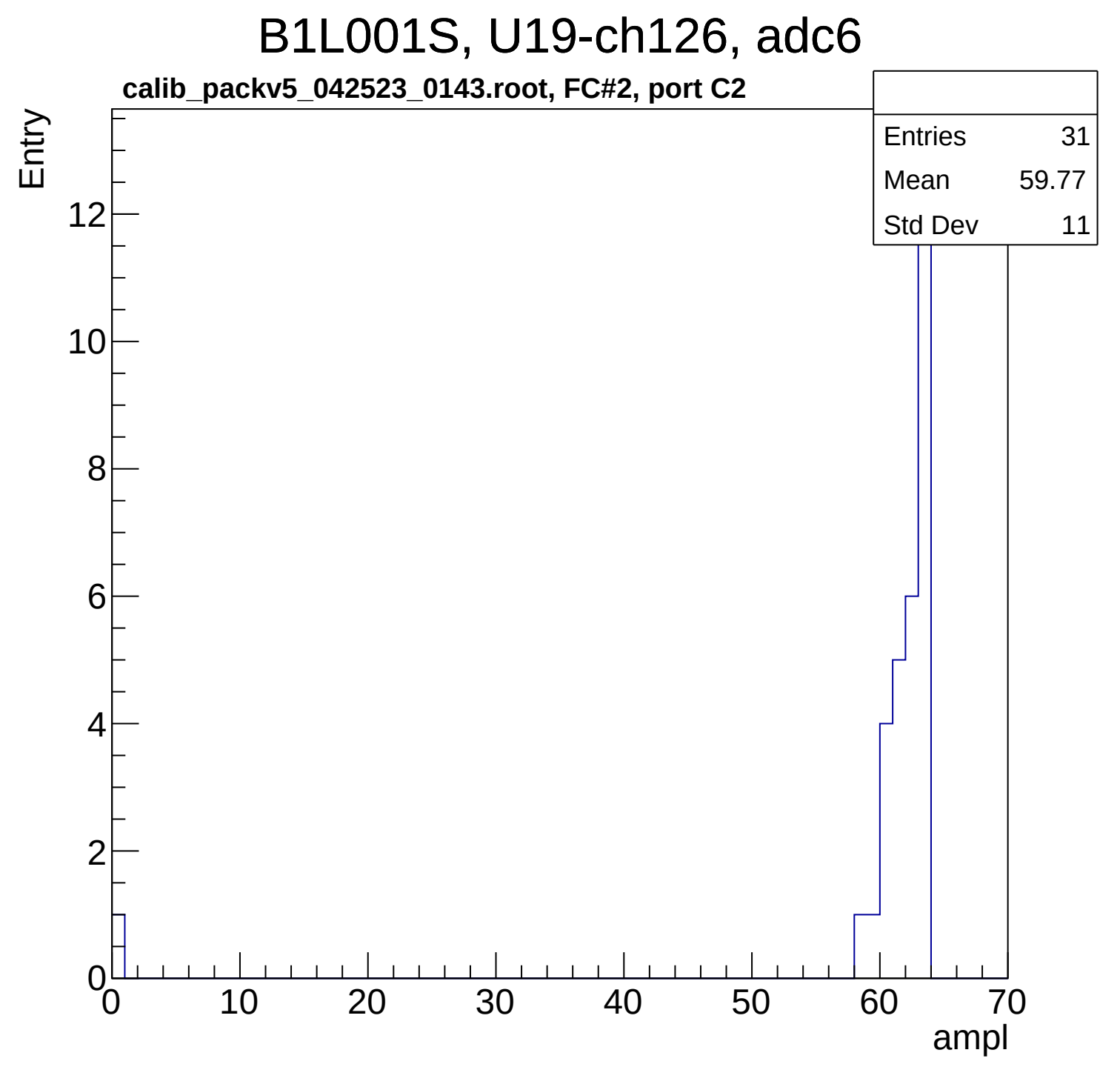
B1L001S, U19-ch126, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 31
Mean 59.77
Std Dev 11
Entry
0
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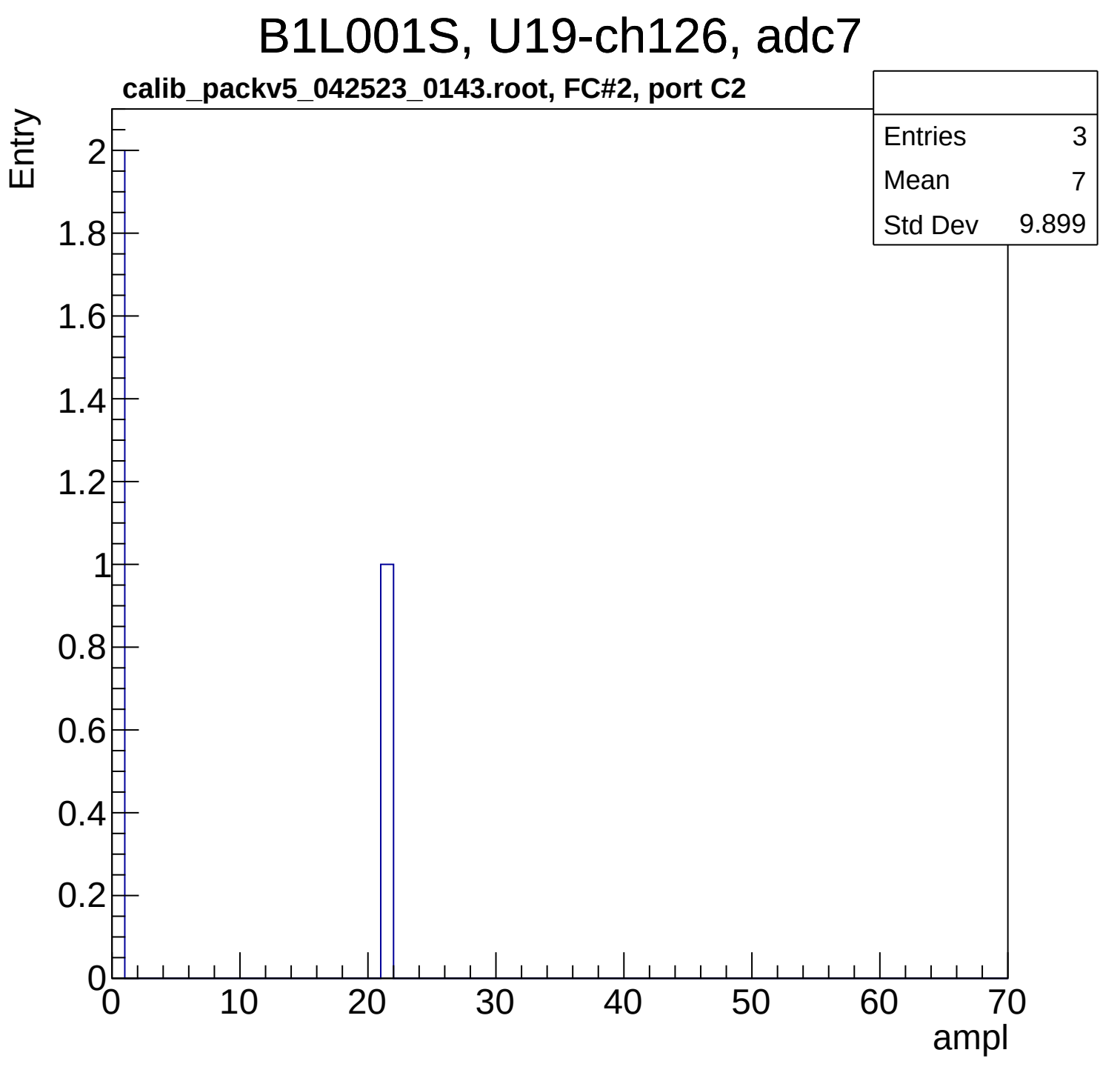
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch126, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 3
Mean 7
Std Dev 9.899
Entry
ampl
0
0.2
0.4
0.6
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1
1.2
1.4
1.6
1.8
2
0
10
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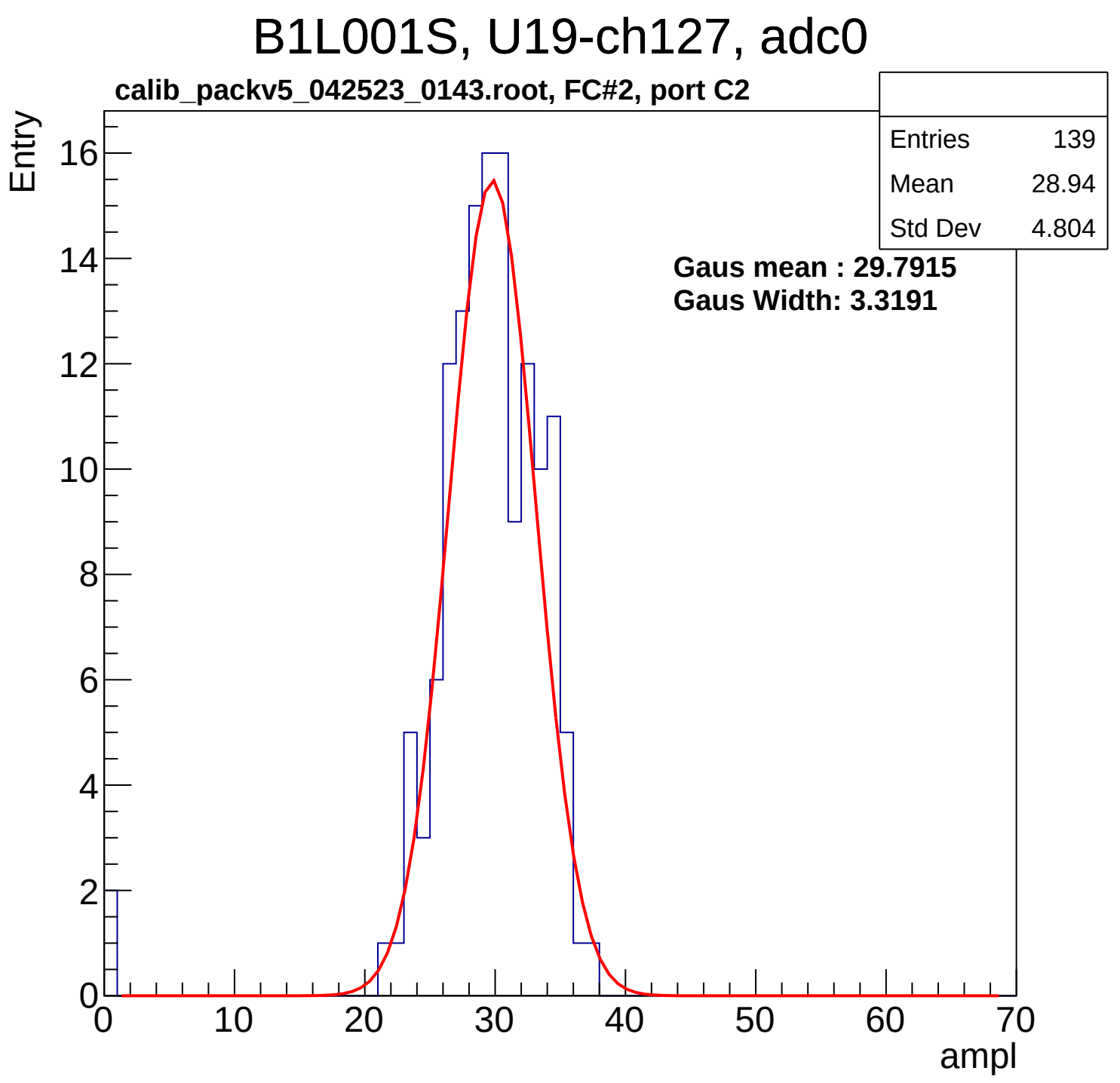
40
50
60
70


B1L001S, U19-ch127, adc0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 139
Mean 28.94
Std Dev 4.804
Gaus mean : 29.7915
Gaus Width: 3.3191
Entry
ampl
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2
4
6
8
10
12
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0
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20
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40
50
60
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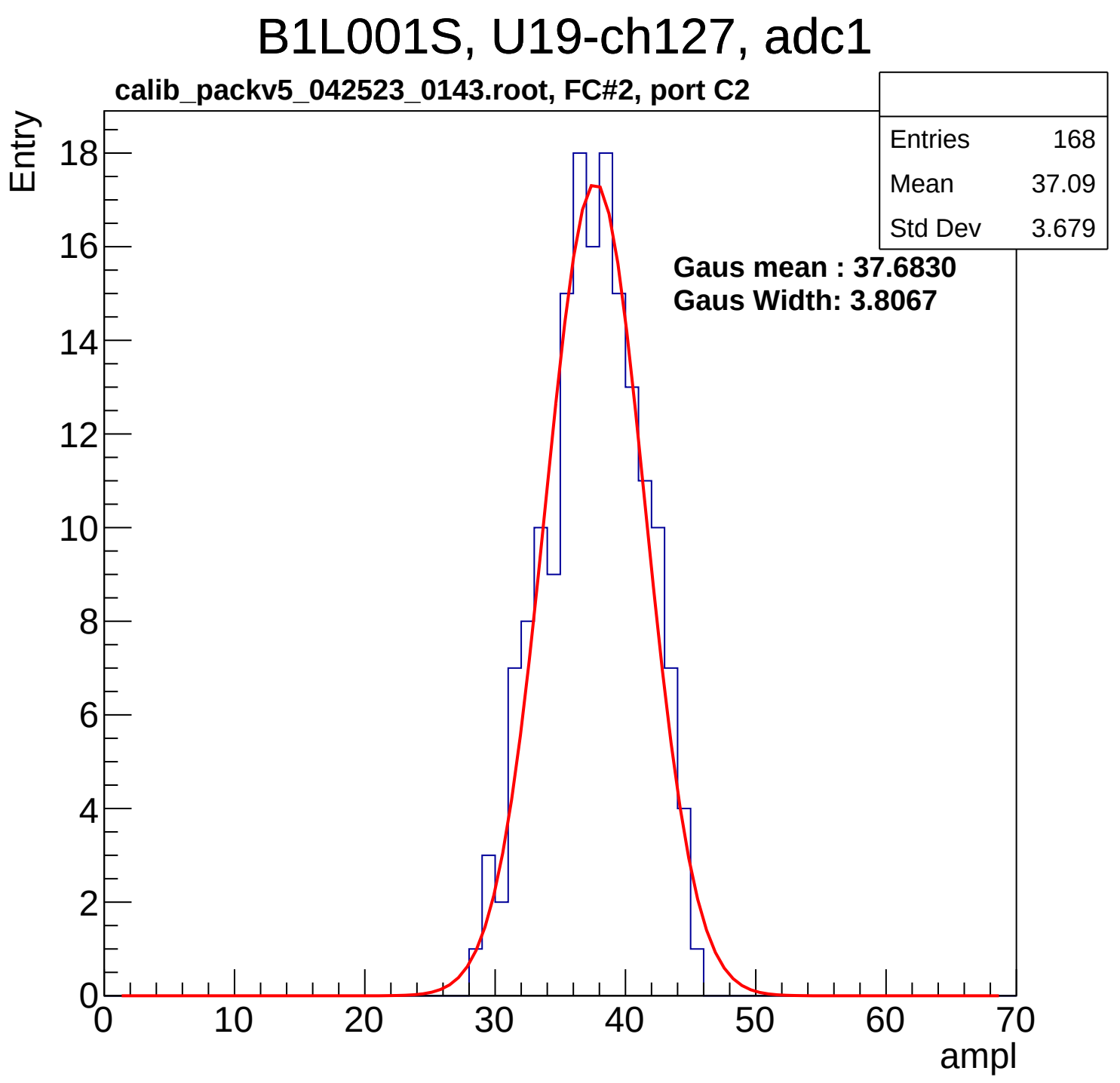
B1L001S, U19-ch127, adc1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 168
Mean 37.09
Std Dev 3.679
Gaus mean : 37.6830
Gaus Width: 3.8067
Entry
ampl
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4
6
8
10
12
14
16
18
0
10
20
30
40
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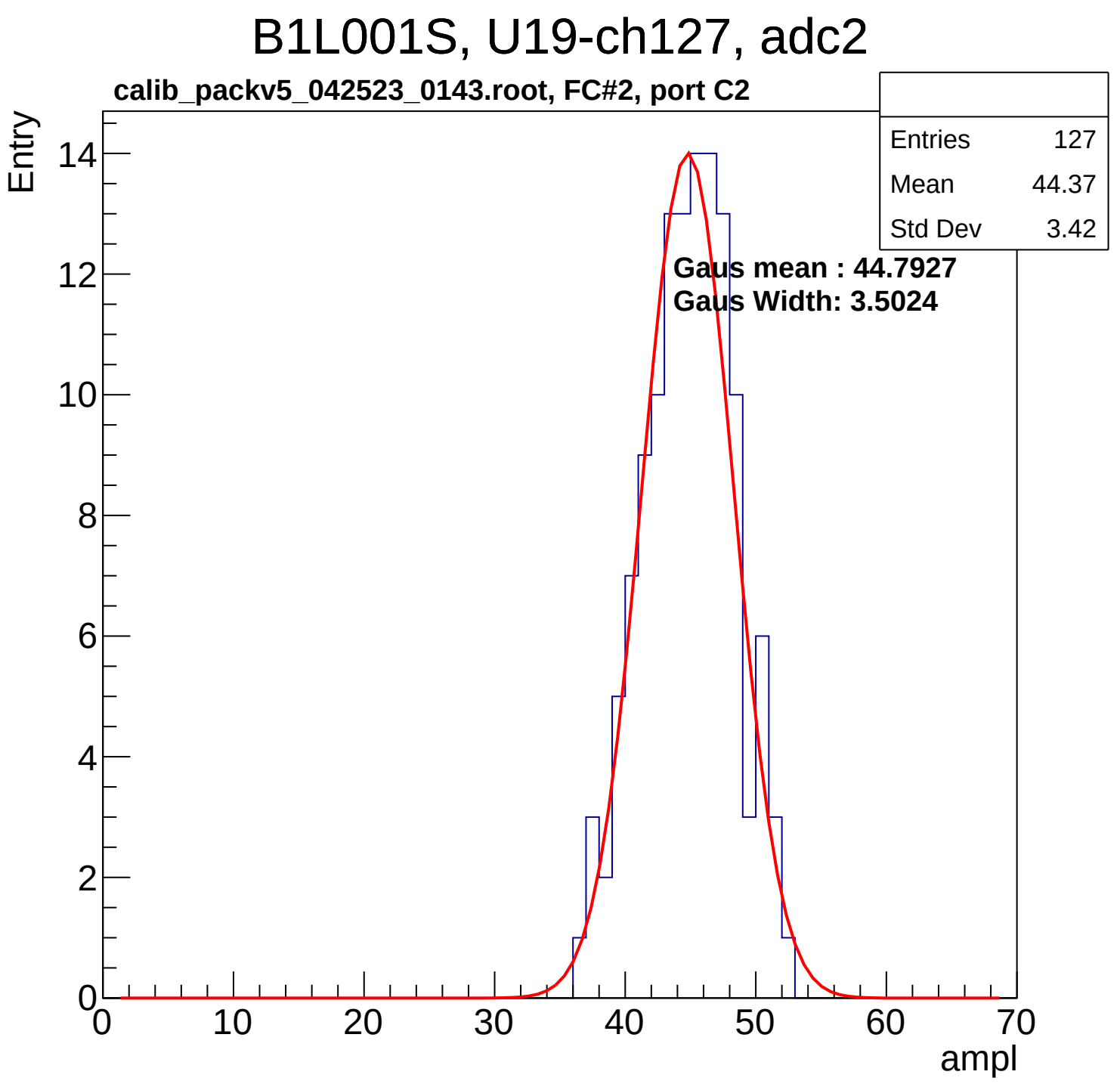
B1L001S, U19-ch127, adc2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 127
Mean 44.37
Std Dev 3.42
Gaus mean : 44.7927
Gaus Width: 3.5024
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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40
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60
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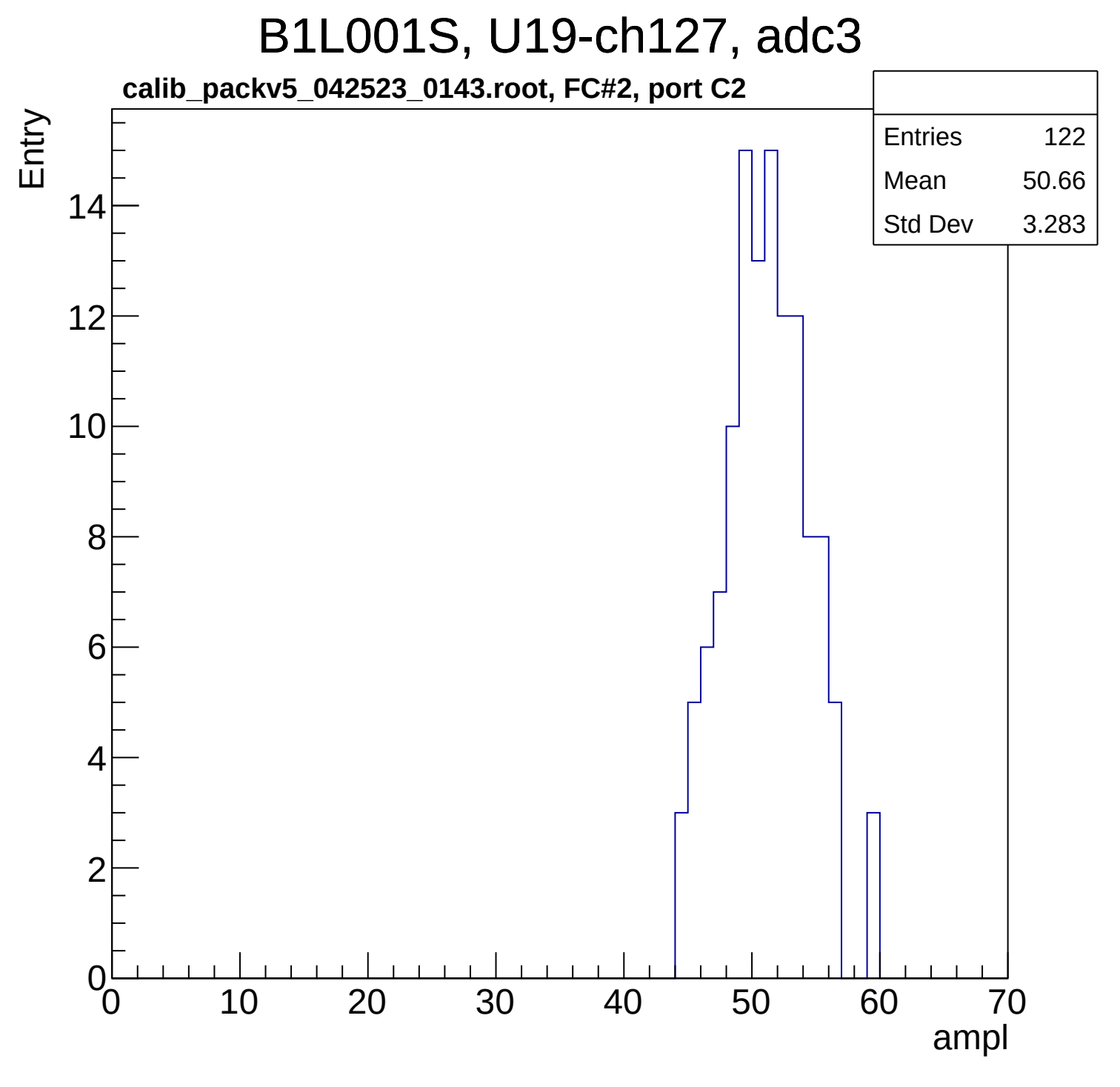
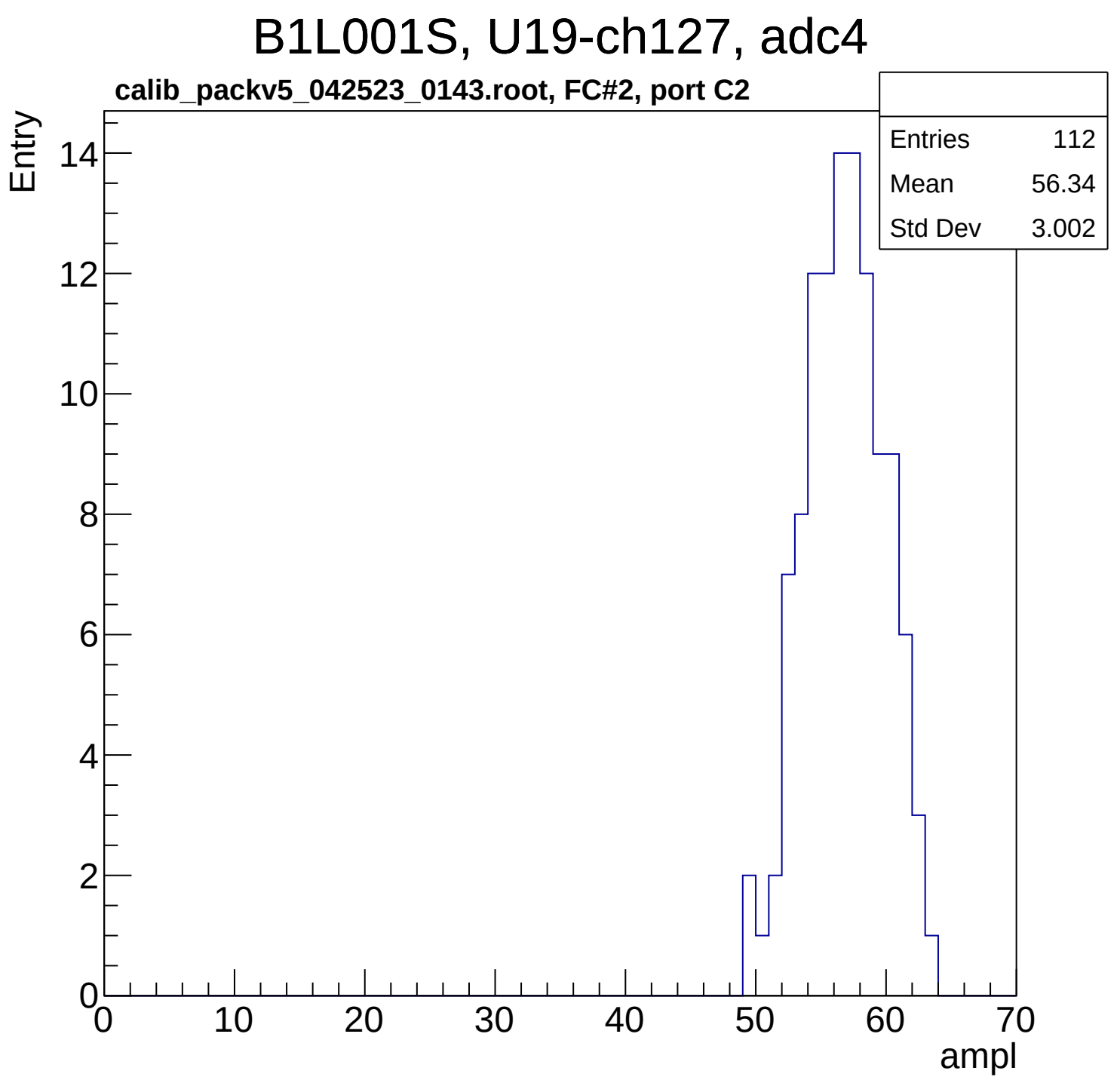
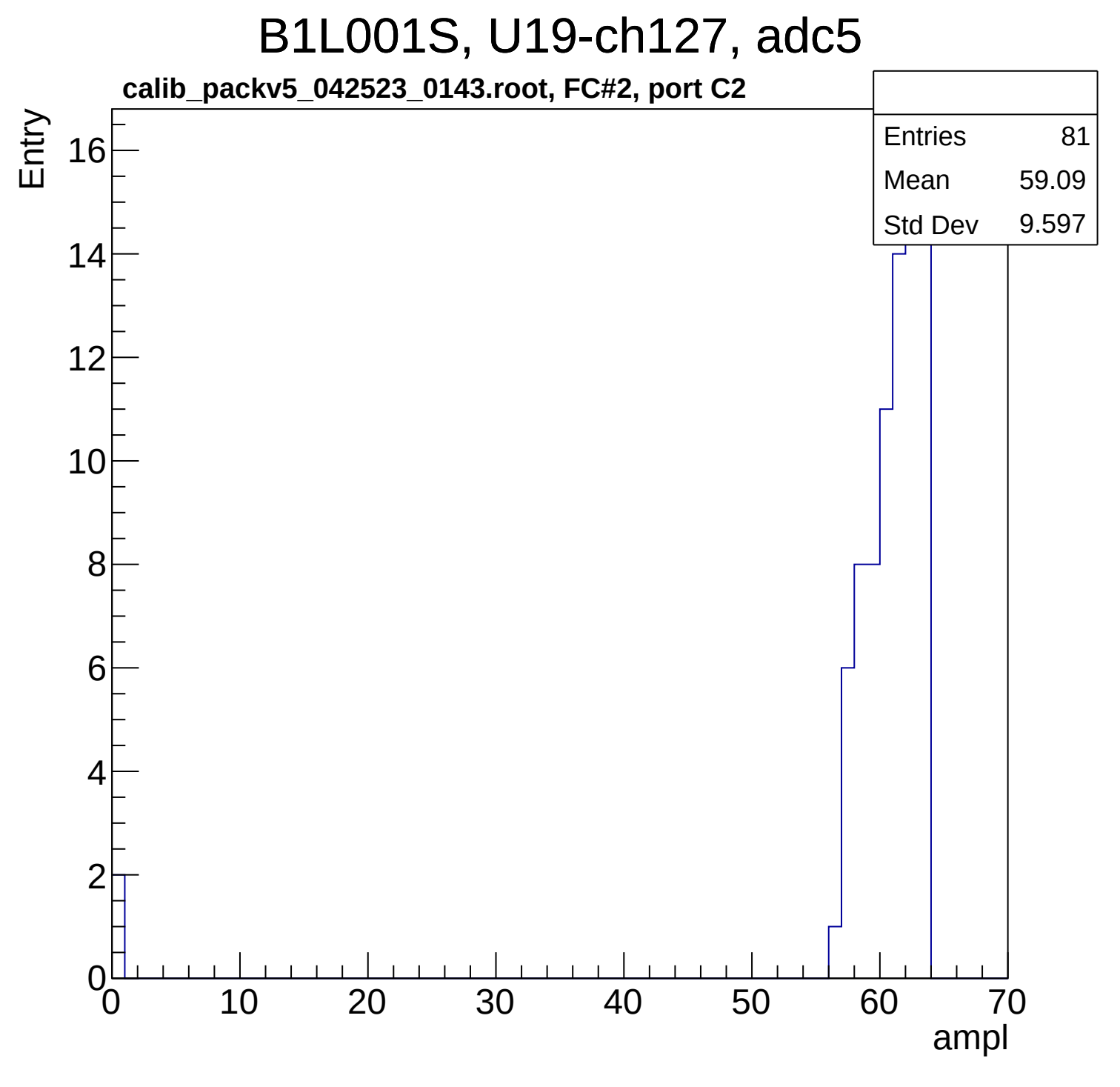
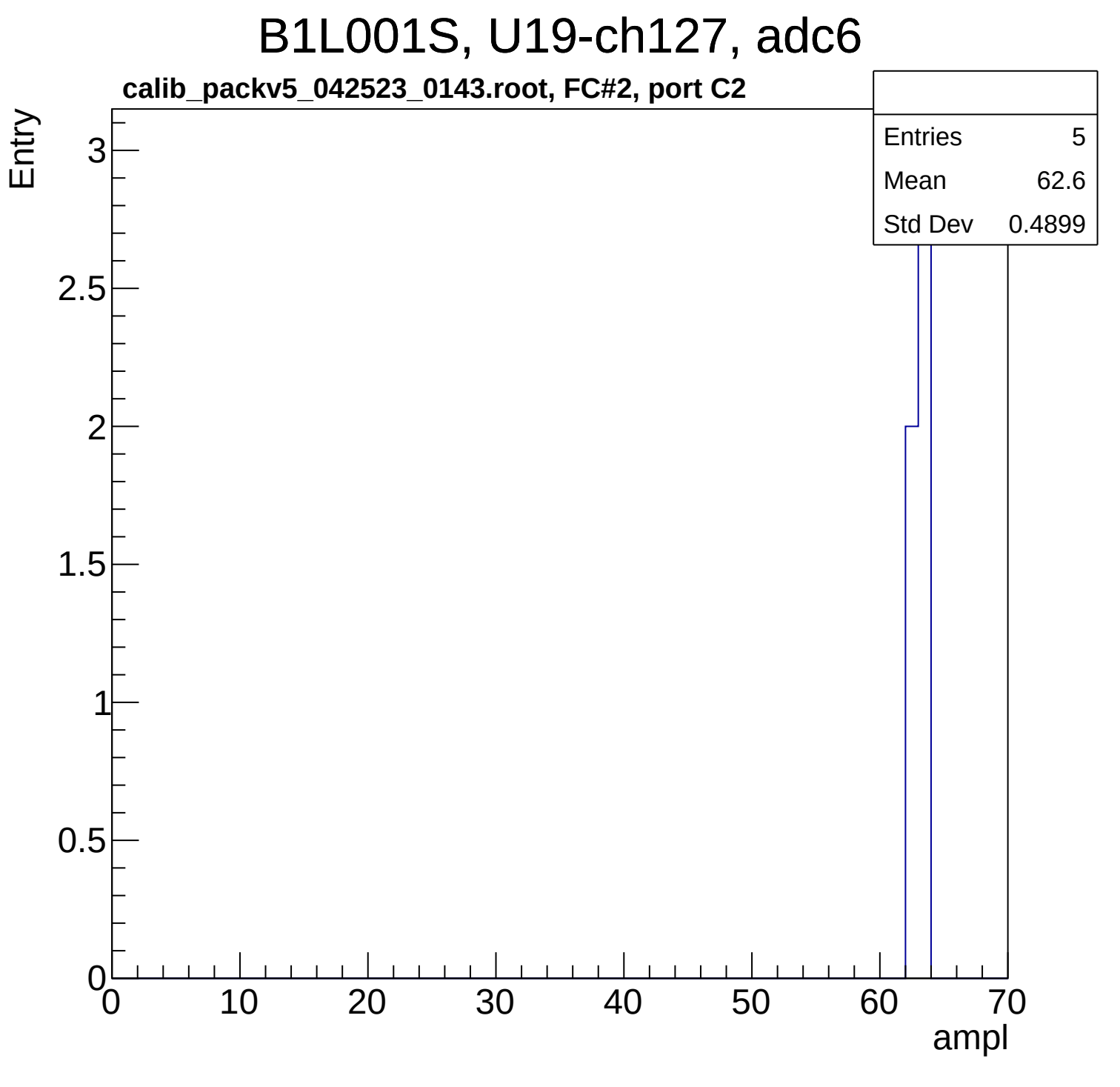
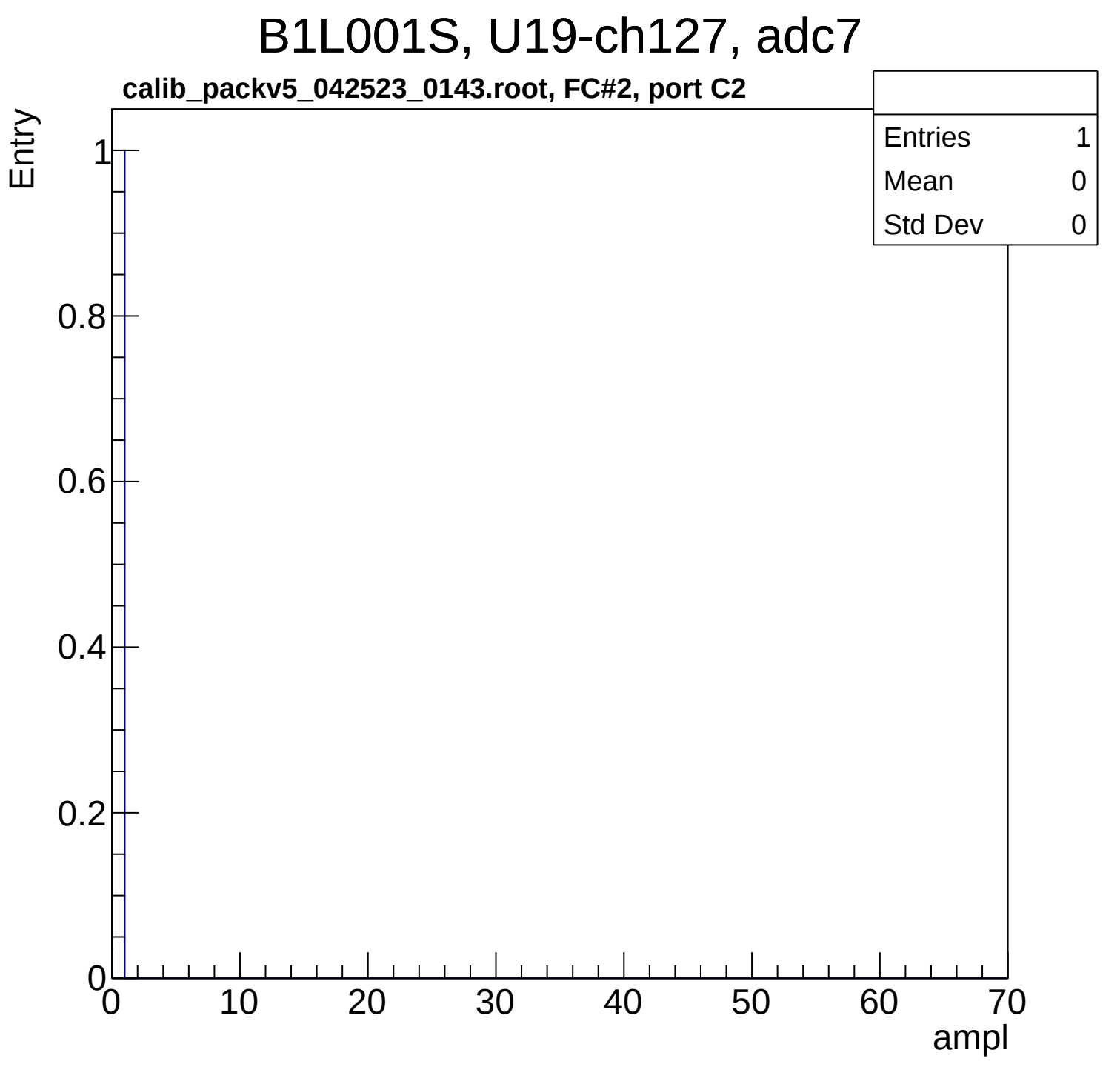
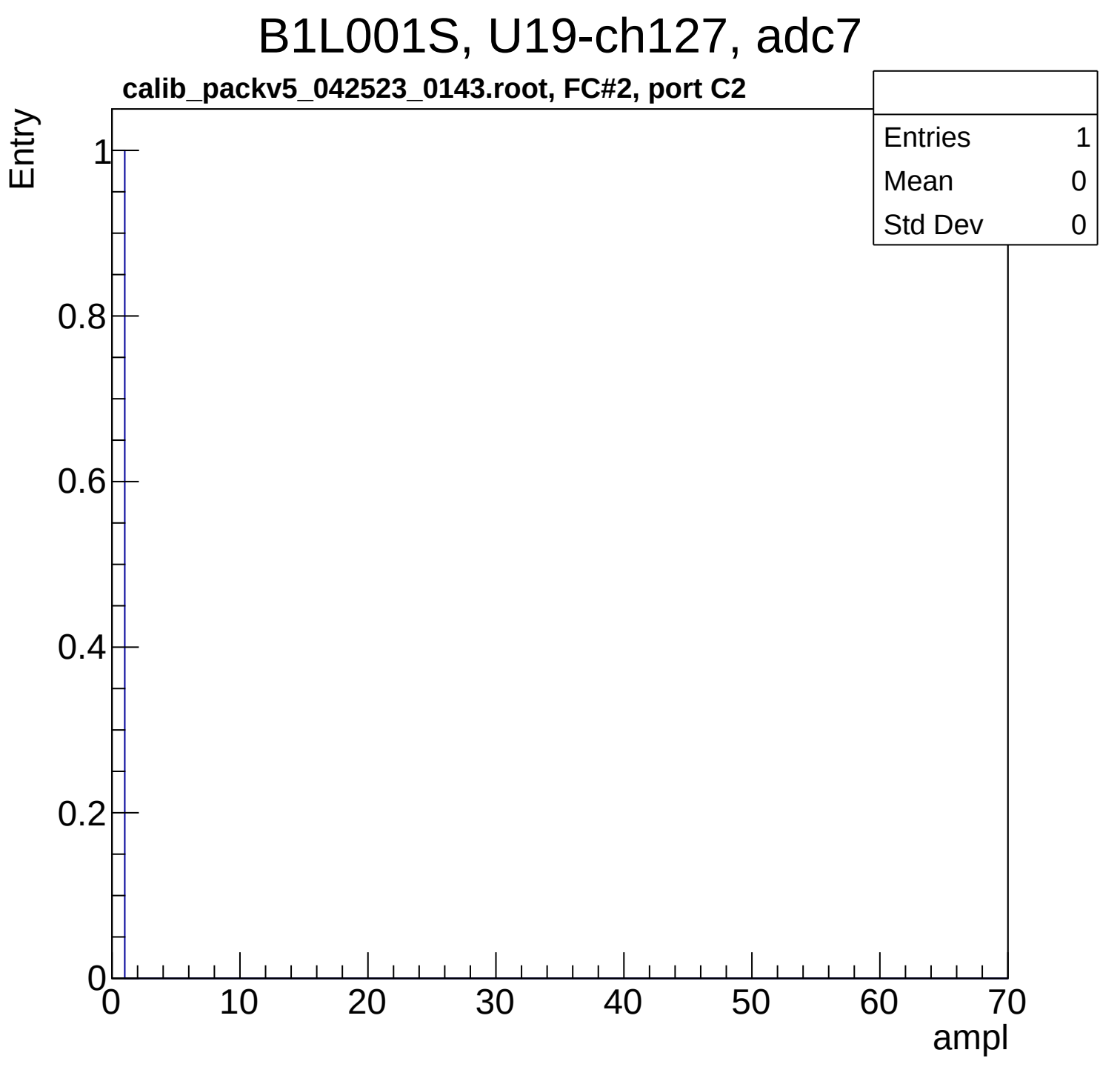

B1L001S, U19-ch127, adc3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 122
Mean 50.66
Std Dev 3.283
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch127, adc4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 112
Mean 56.34
Std Dev 3.002
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L001S, U19-ch127, adc5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 81
Mean 59.09
Std Dev 9.597
Entry
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch127, adc6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 5
Mean 62.6
Std Dev 0.4899
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L001S, U19-ch127, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L001S, U19-ch127, adc7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl