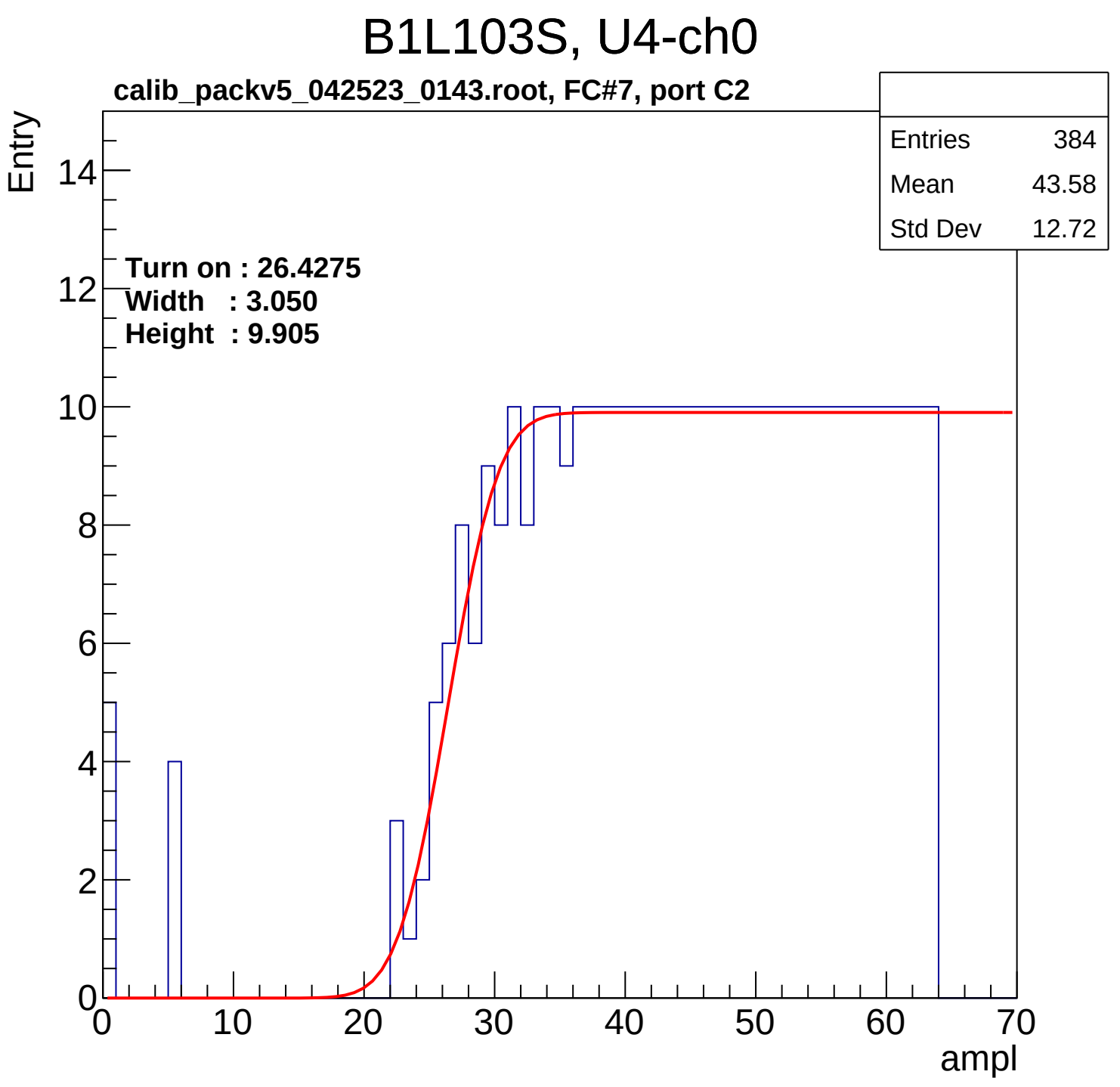
B1L103S, U4-ch0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 384
Mean 43.58
Std Dev 12.72
Turn on : 26.4275
Width : 3.050
Height : 9.905
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ampl
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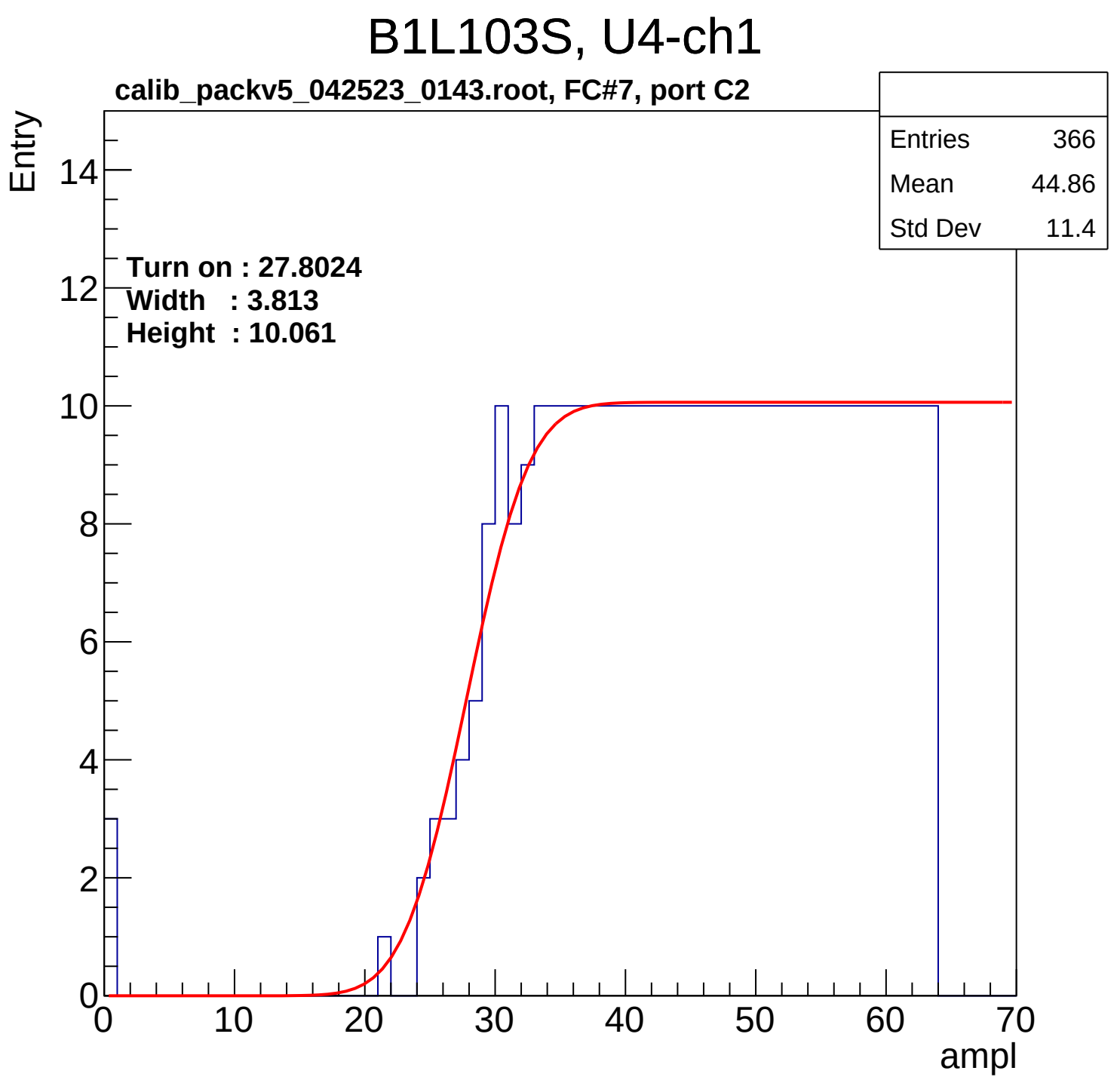
B1L103S, U4-ch1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 366
Mean 44.86
Std Dev 11.4
Turn on : 27.8024
Width : 3.813
Height : 10.061
Entry
ampl
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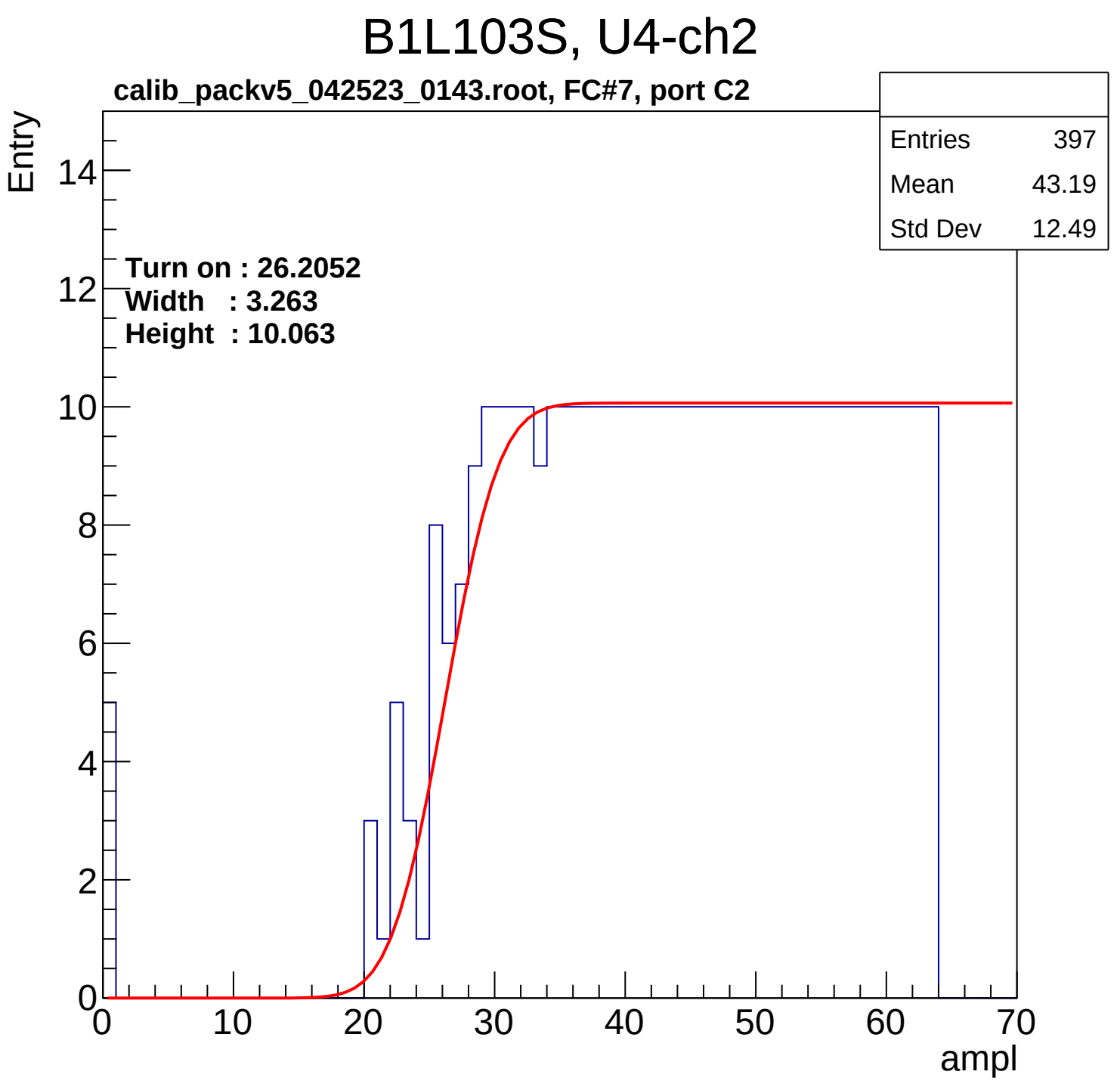
B1L103S, U4-ch2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 397
Mean 43.19
Std Dev 12.49
Turn on : 26.2052
Width : 3.263
Height : 10.063
Entry
ampl
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2
4
6
8
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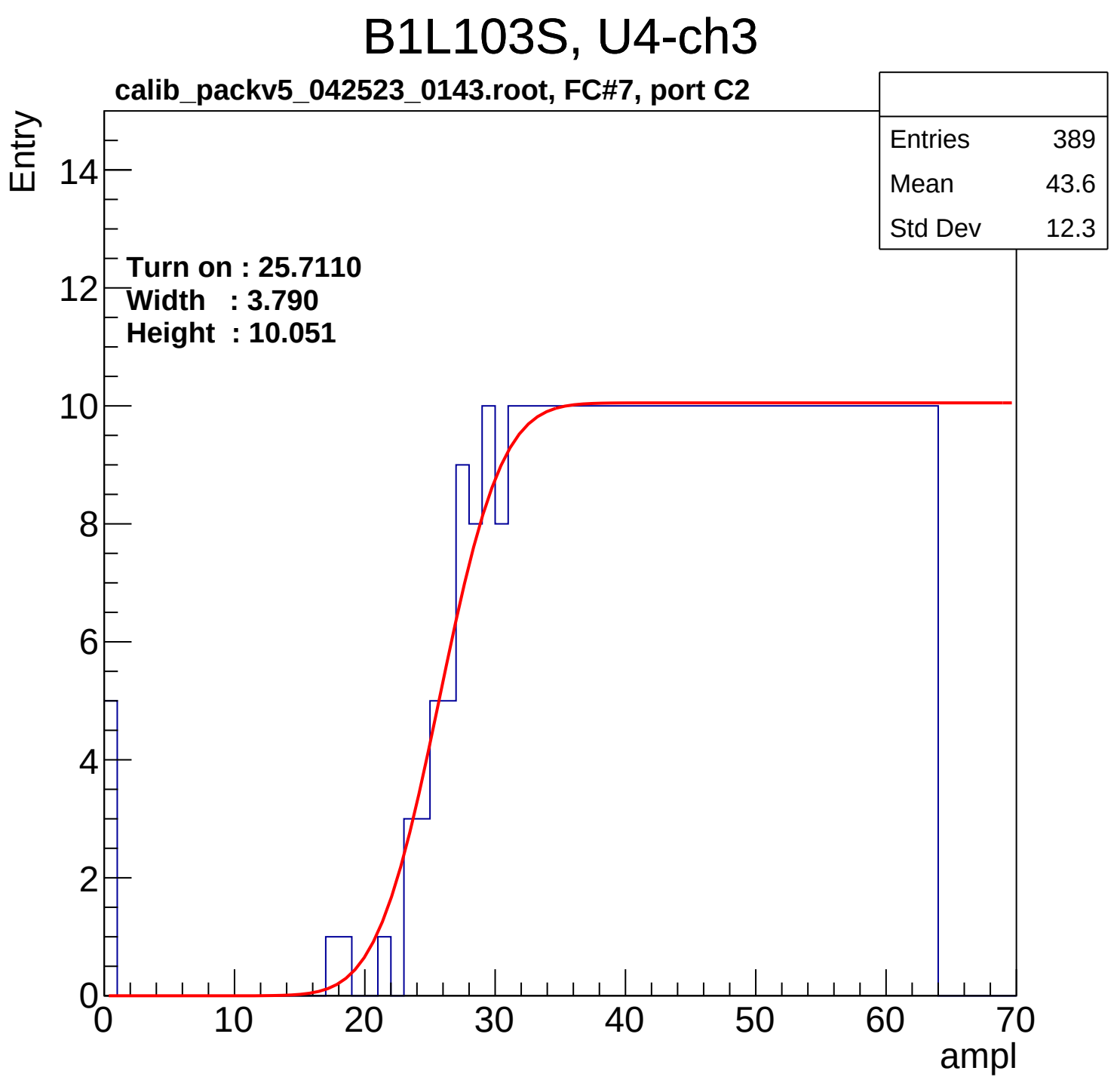
B1L103S, U4-ch3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 389
Mean 43.6
Std Dev 12.3
Turn on : 25.7110
Width : 3.790
Height : 10.051
Entry
ampl
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2
4
6
8
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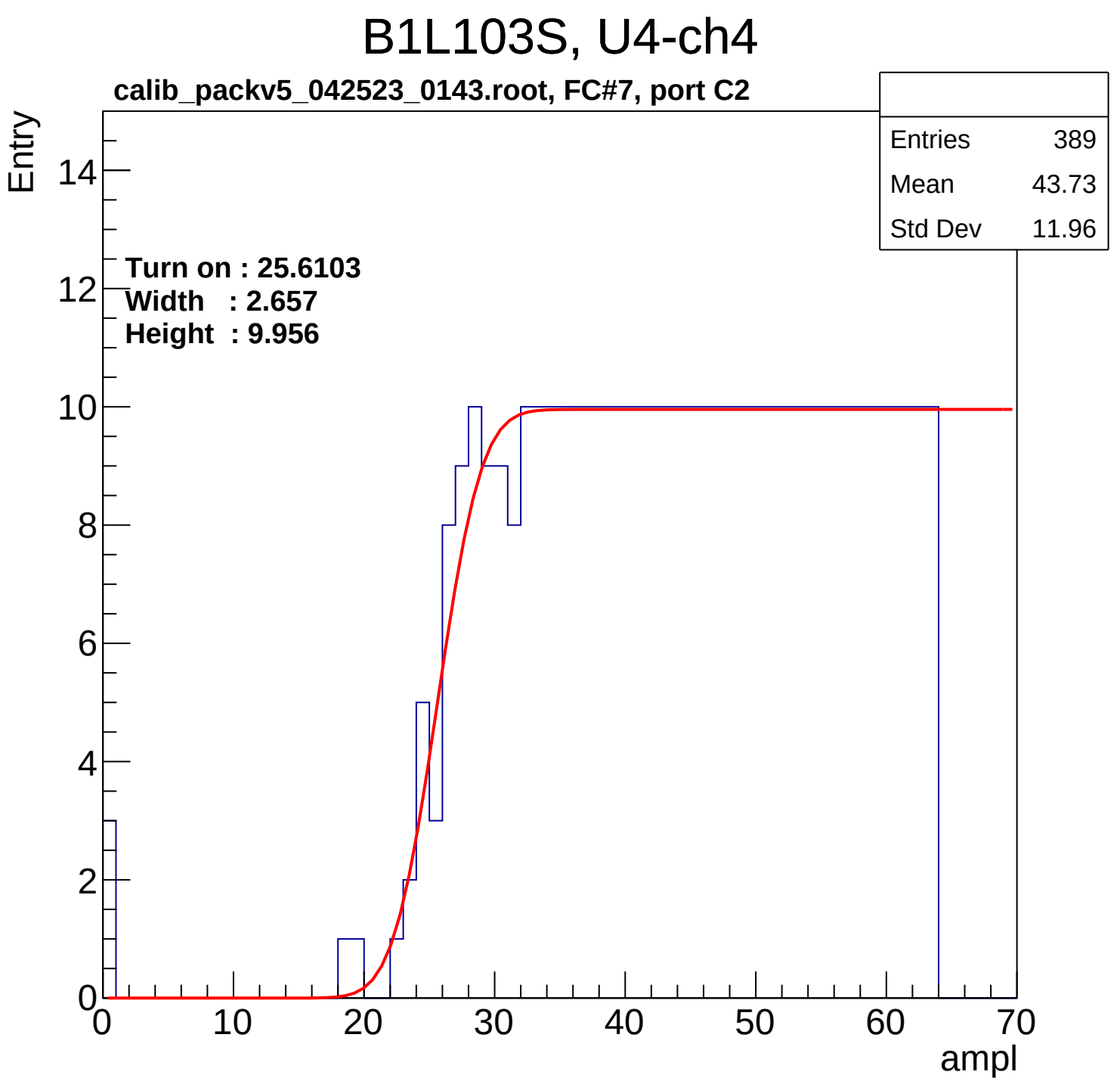
B1L103S, U4-ch4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 389
Mean 43.73
Std Dev 11.96
Turn on : 25.6103
Width : 2.657
Height : 9.956
Entry
ampl
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2
4
6
8
10
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0
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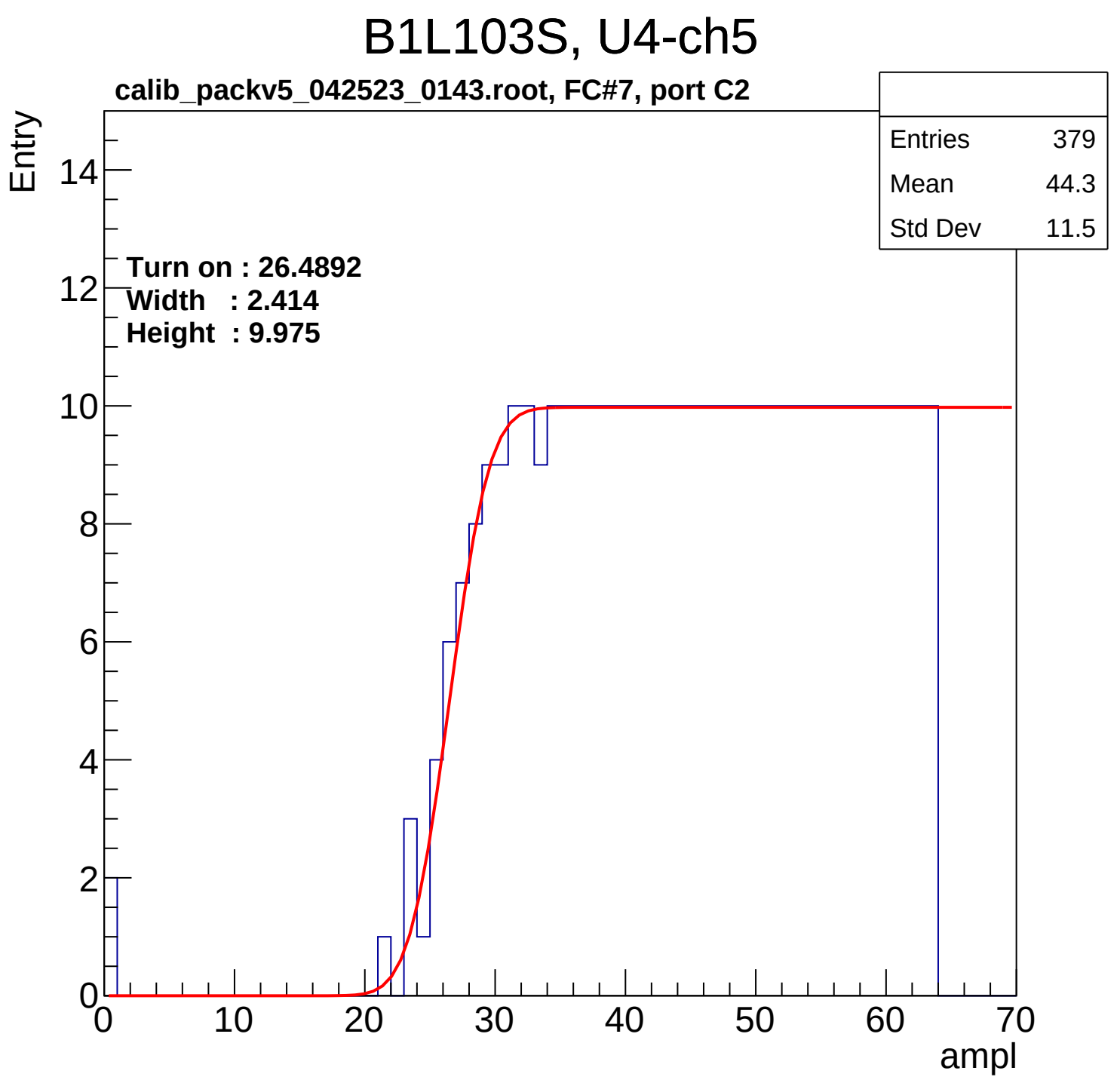
B1L103S, U4-ch5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 379
Mean 44.3
Std Dev 11.5
Turn on : 26.4892
Width : 2.414
Height : 9.975
Entry
ampl
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4
6
8
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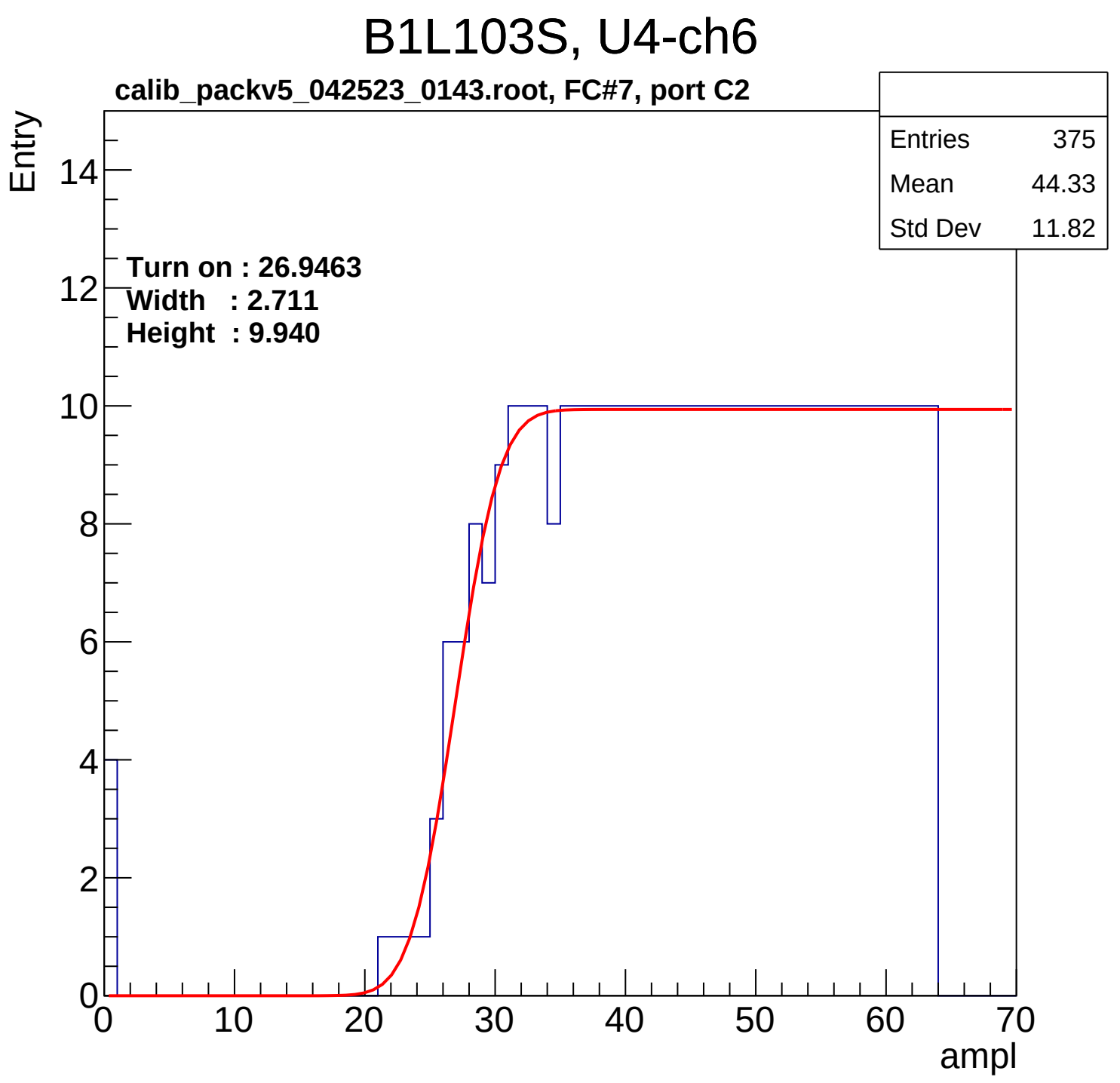
B1L103S, U4-ch6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 375
Mean 44.33
Std Dev 11.82
Turn on : 26.9463
Width : 2.711
Height : 9.940
Entry
ampl
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2
4
6
8
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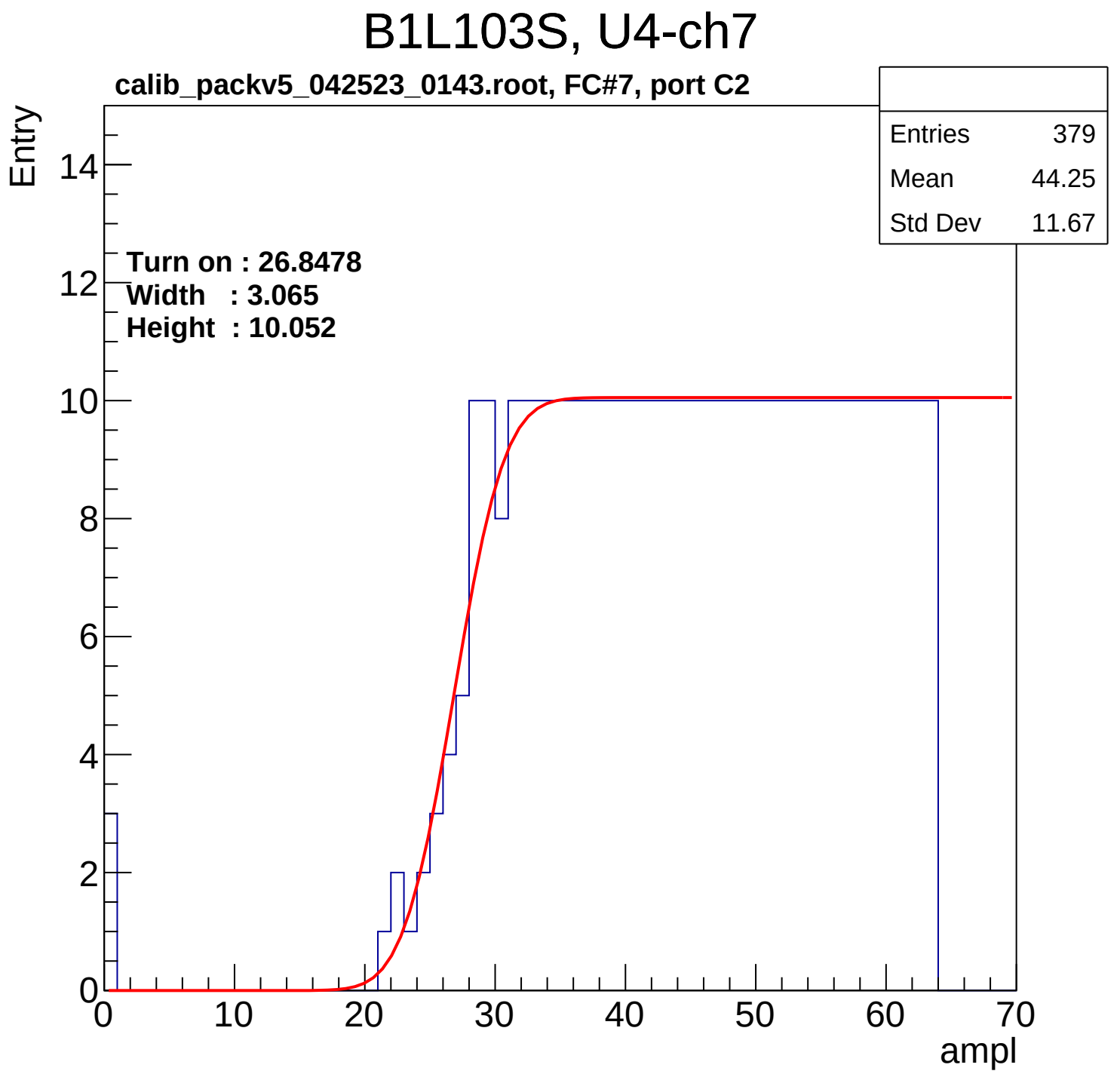
B1L103S, U4-ch7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 379
Mean 44.25
Std Dev 11.67
Turn on : 26.8478
Width : 3.065
Height : 10.052
Entry
ampl
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4
6
8
10
12
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0
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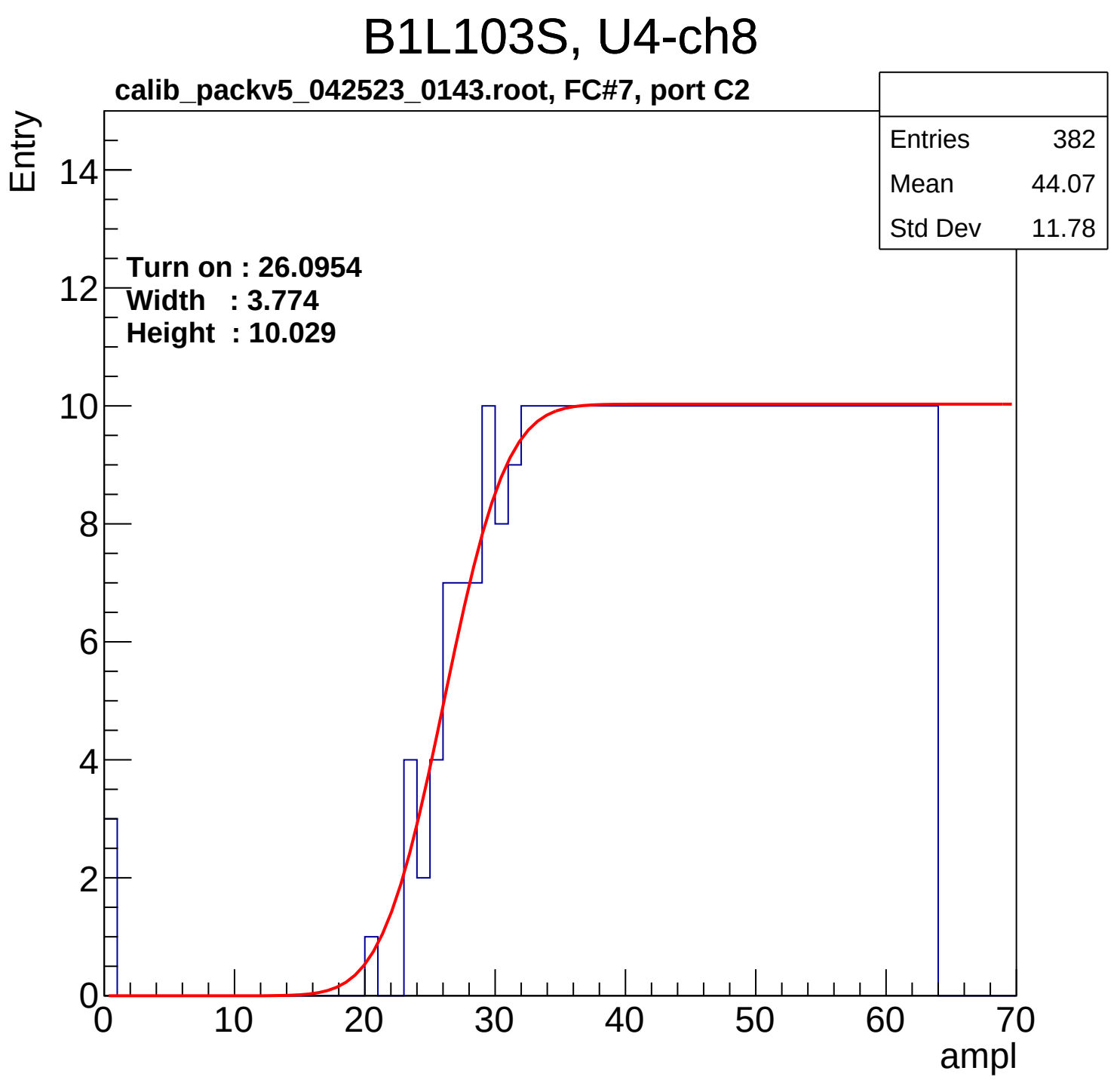
B1L103S, U4-ch8
calib_packv5_042523_0143.root, FC#7, port C2
Entries 382
Mean 44.07
Std Dev 11.78
Turn on : 26.0954
Width : 3.774
Height : 10.029
Entry
ampl
0
2
4
6
8
10
12
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0
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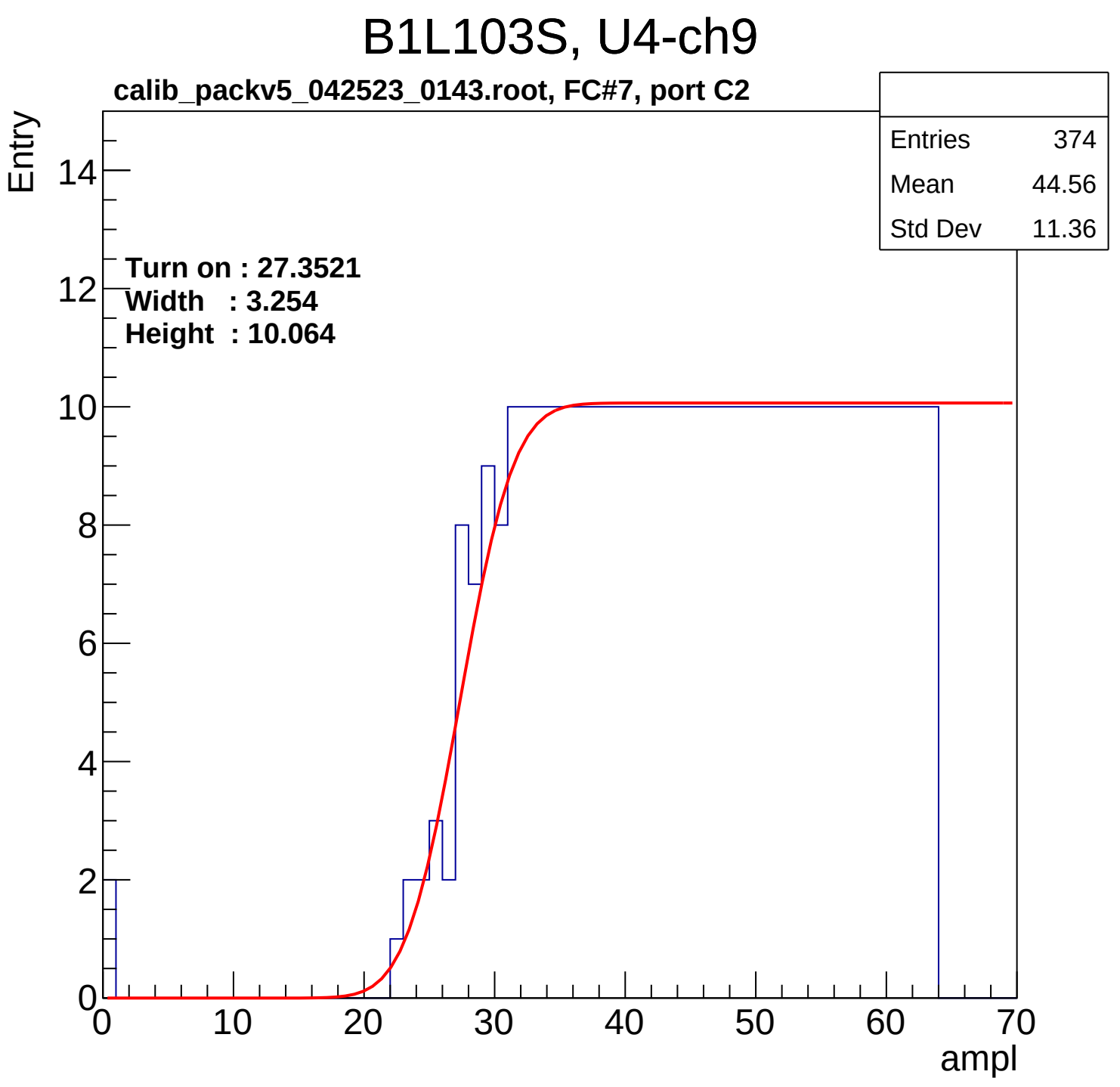
B1L103S, U4-ch9
calib_packv5_042523_0143.root, FC#7, port C2
Entries 374
Mean 44.56
Std Dev 11.36
Turn on : 27.3521
Width : 3.254
Height : 10.064
Entry
ampl
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6
8
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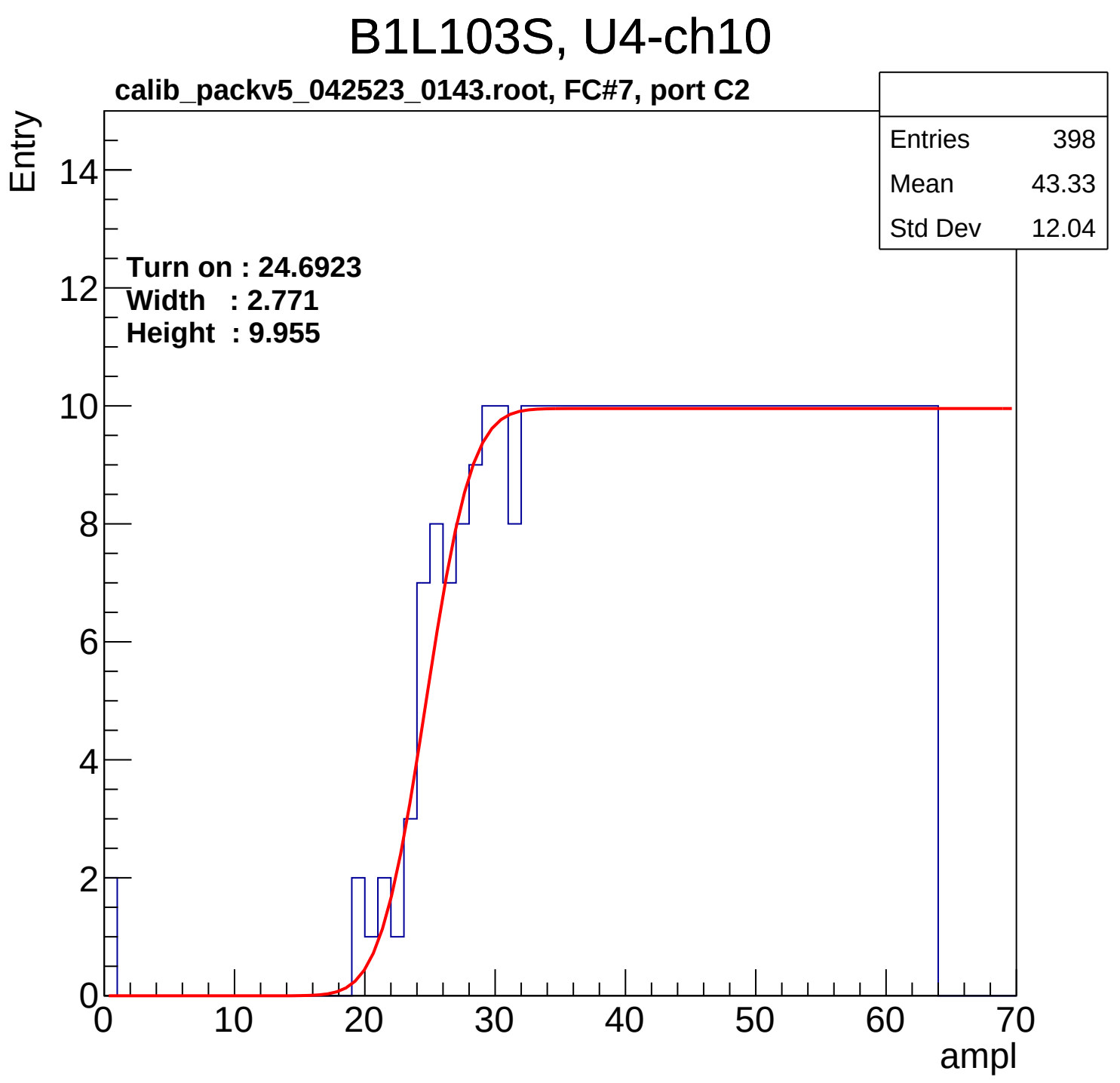
B1L103S, U4-ch10
calib_packv5_042523_0143.root, FC#7, port C2
Entries 398
Mean 43.33
Std Dev 12.04
Turn on : 24.6923
Width : 2.771
Height : 9.955
Entry
ampl
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6
8
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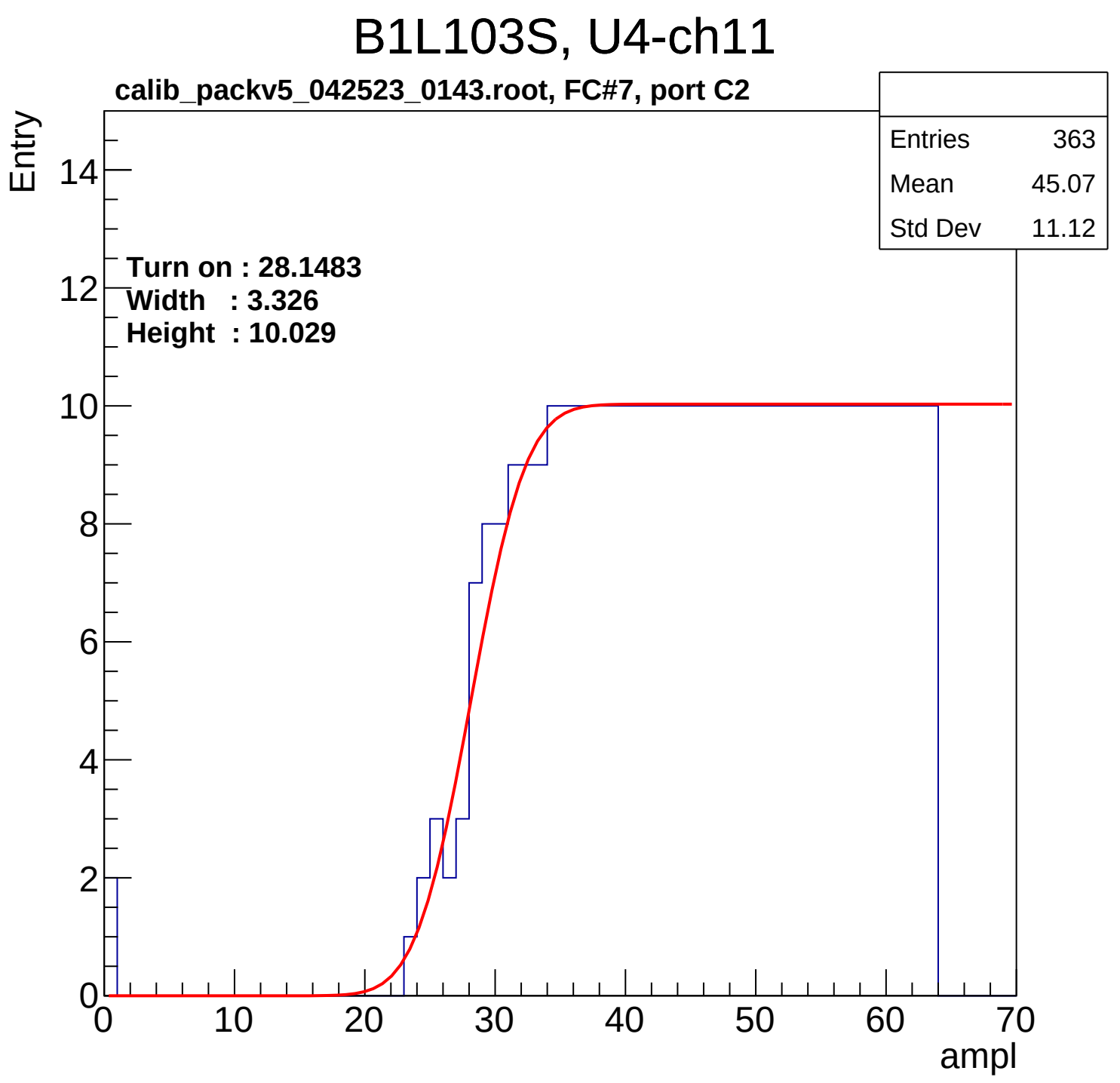
B1L103S, U4-ch11
calib_packv5_042523_0143.root, FC#7, port C2
Entries 363
Mean 45.07
Std Dev 11.12
Turn on : 28.1483
Width : 3.326
Height : 10.029
Entry
ampl
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6
8
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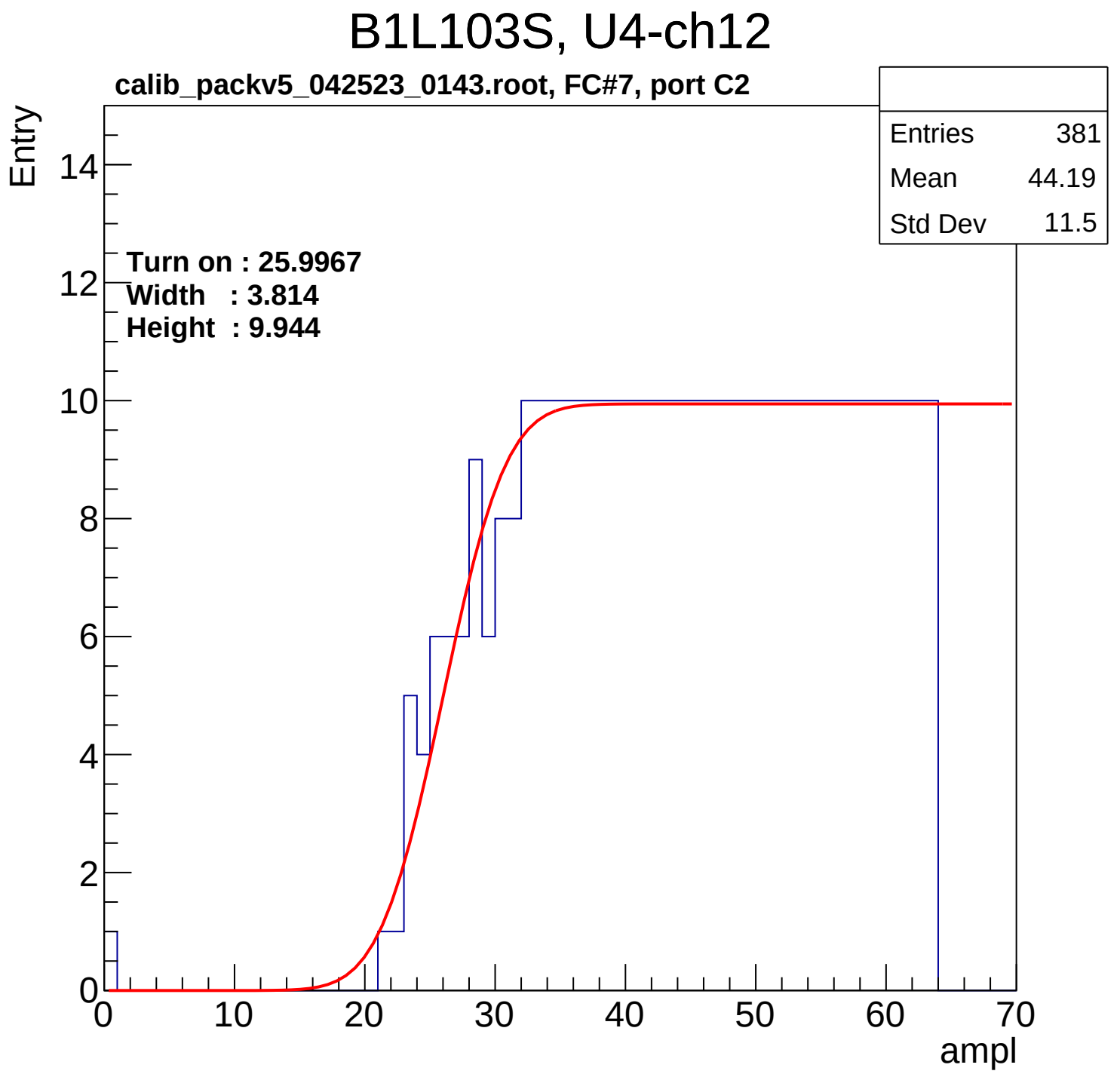
B1L103S, U4-ch12
calib_packv5_042523_0143.root, FC#7, port C2
Entries 381
Mean 44.19
Std Dev 11.5
Turn on : 25.9967
Width : 3.814
Height : 9.944
Entry
ampl
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8
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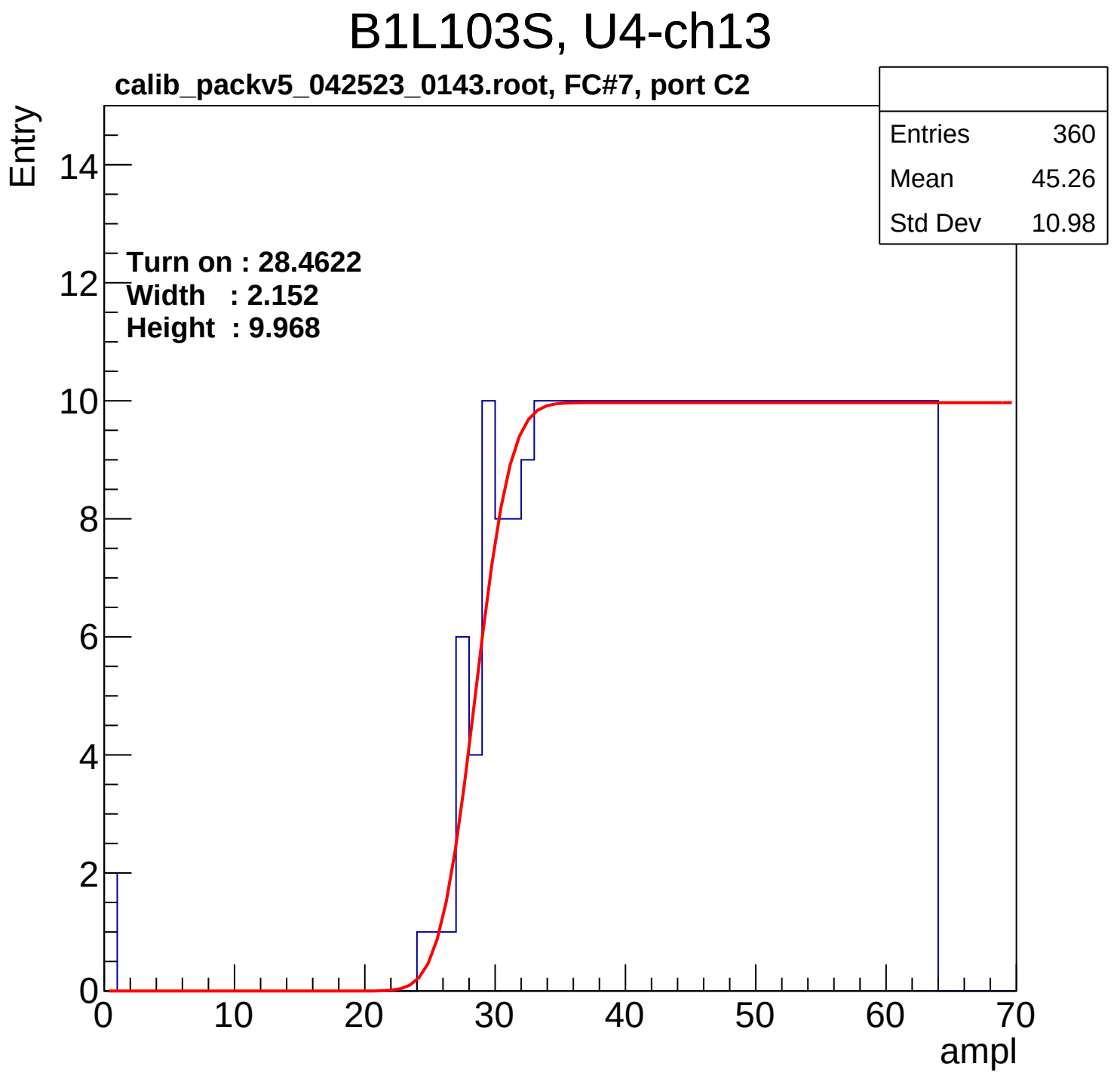
B1L103S, U4-ch13
calib_packv5_042523_0143.root, FC#7, port C2
Entries 360
Mean 45.26
Std Dev 10.98
Turn on : 28.4622
Width : 2.152
Height : 9.968
Entry
ampl
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6
8
10
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0
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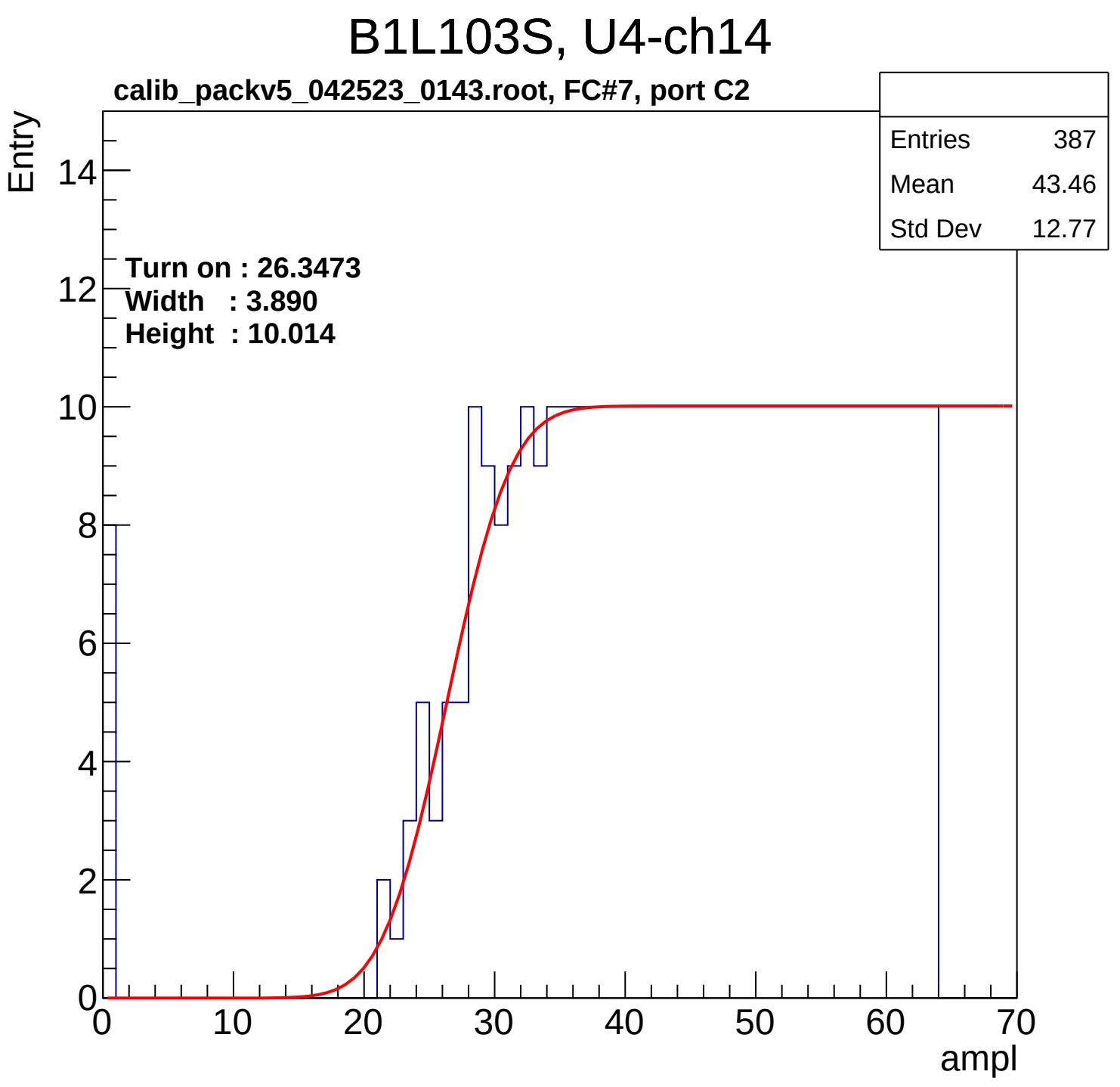
B1L103S, U4-ch14
calib_packv5_042523_0143.root, FC#7, port C2
Entries 387
Mean 43.46
Std Dev 12.77
Turn on : 26.3473
Width : 3.890
Height : 10.014
Entry
ampl
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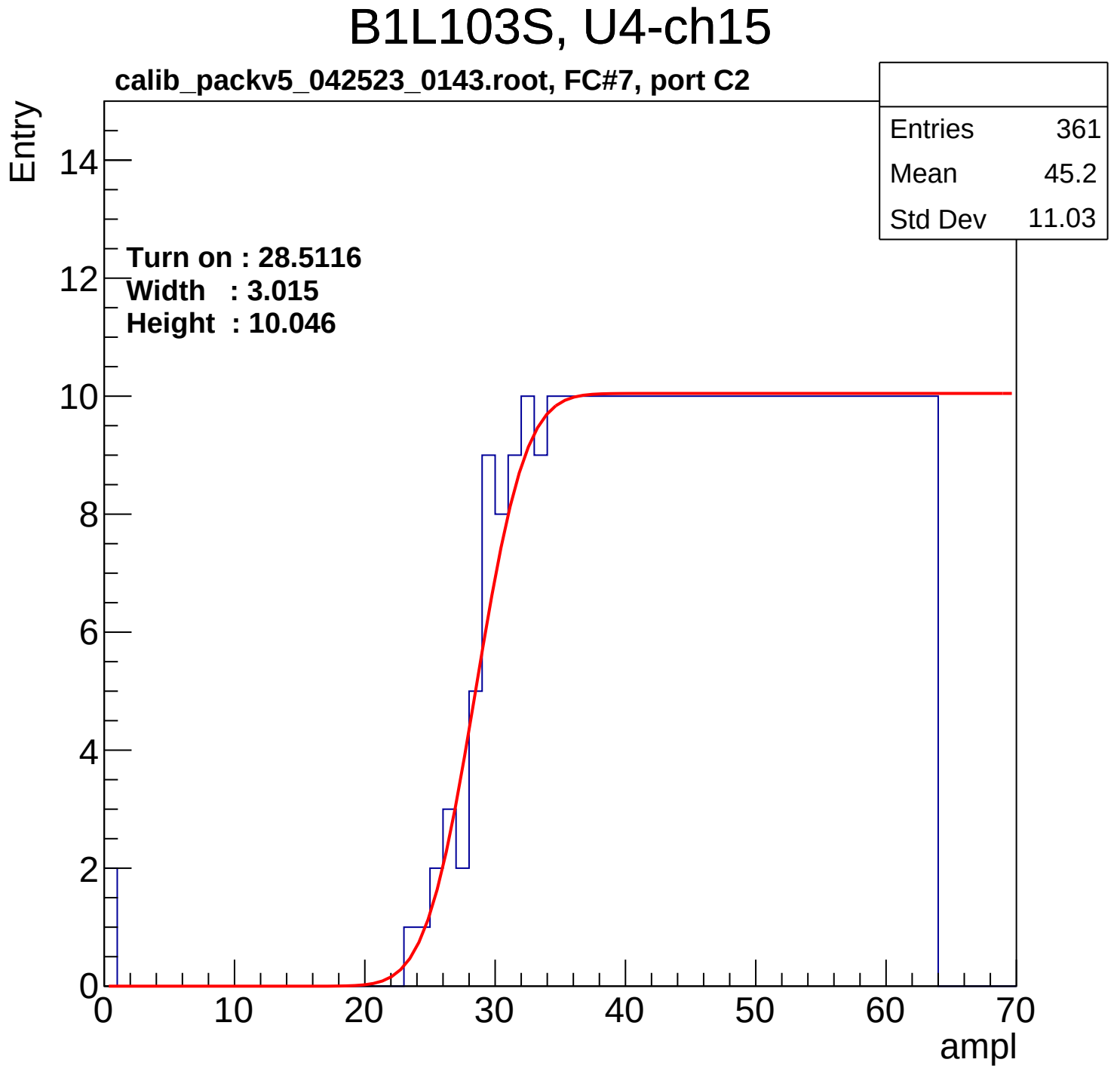
B1L103S, U4-ch15
calib_packv5_042523_0143.root, FC#7, port C2
Entries 361
Mean 45.2
Std Dev 11.03
Turn on : 28.5116
Width : 3.015
Height : 10.046
Entry
ampl
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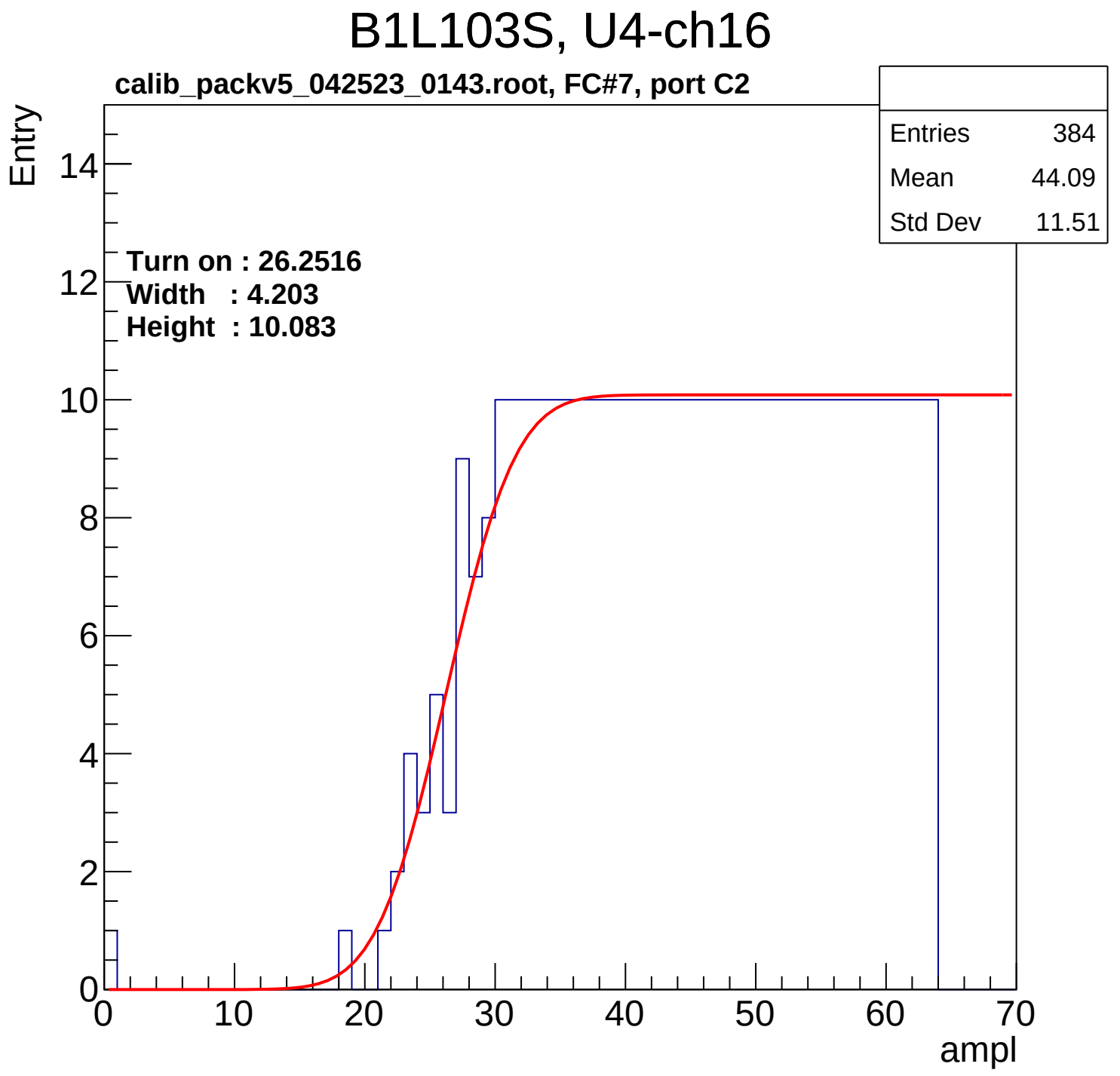
B1L103S, U4-ch16
calib_packv5_042523_0143.root, FC#7, port C2
Entries 384
Mean 44.09
Std Dev 11.51
Turn on : 26.2516
Width : 4.203
Height : 10.083
Entry
ampl
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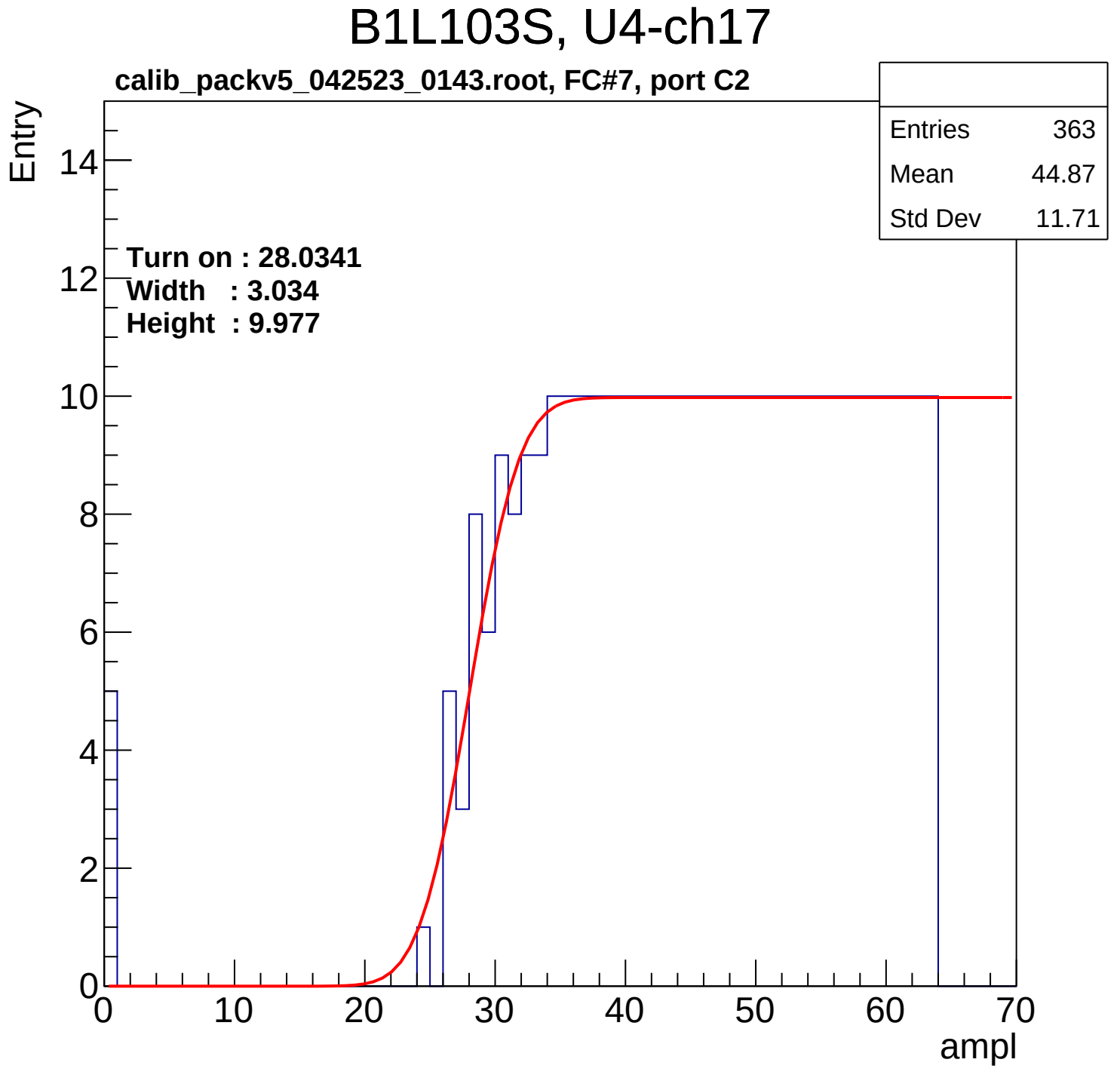
B1L103S, U4-ch17
calib_packv5_042523_0143.root, FC#7, port C2
Entries 363
Mean 44.87
Std Dev 11.71
Turn on : 28.0341
Width : 3.034
Height : 9.977
Entry
ampl
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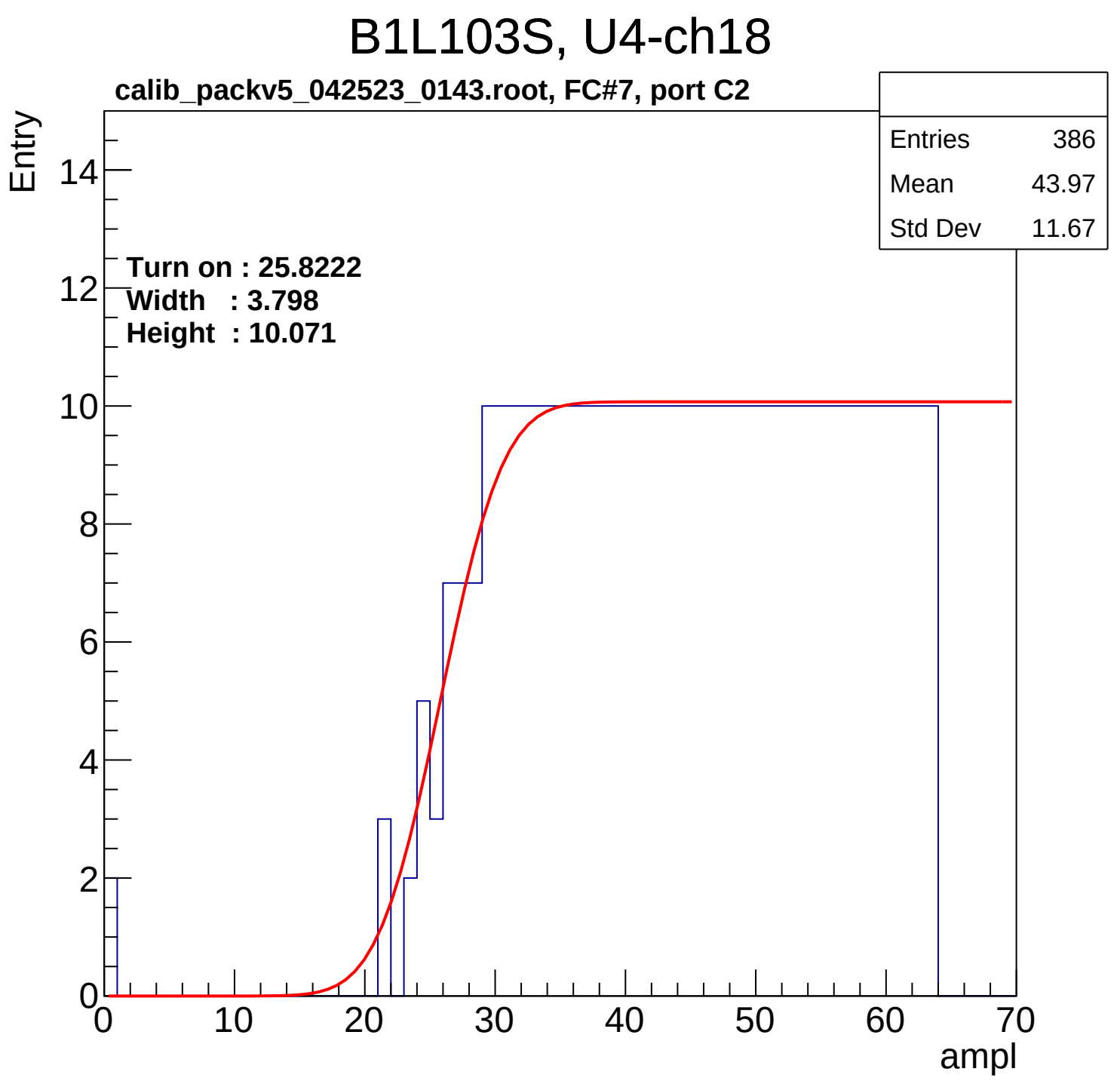
B1L103S, U4-ch18
calib_packv5_042523_0143.root, FC#7, port C2
Entries 386
Mean 43.97
Std Dev 11.67
Turn on : 25.8222
Width : 3.798
Height : 10.071
Entry
ampl
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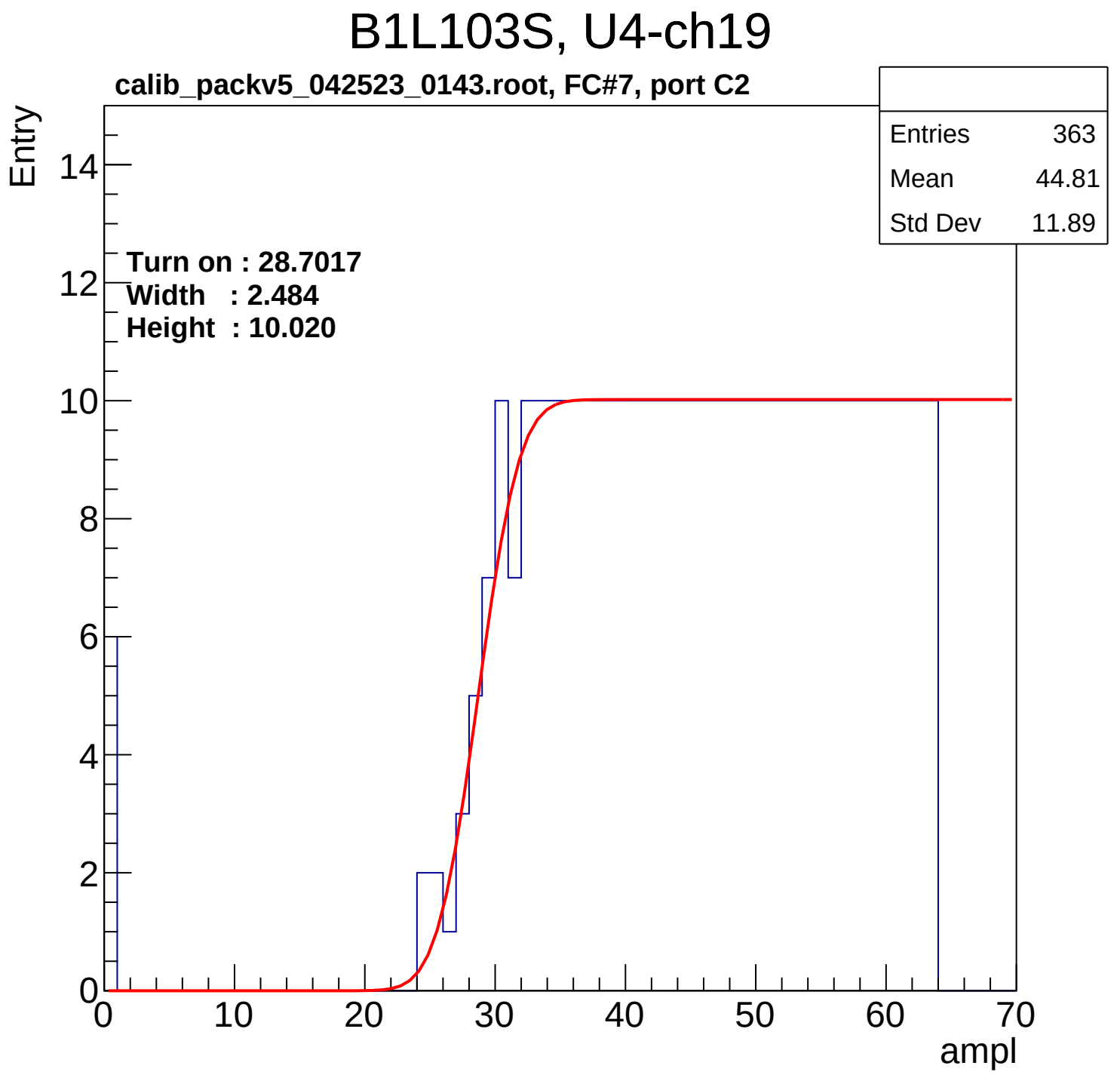
B1L103S, U4-ch19
calib_packv5_042523_0143.root, FC#7, port C2
Entries 363
Mean 44.81
Std Dev 11.89
Turn on : 28.7017
Width : 2.484
Height : 10.020
Entry
ampl
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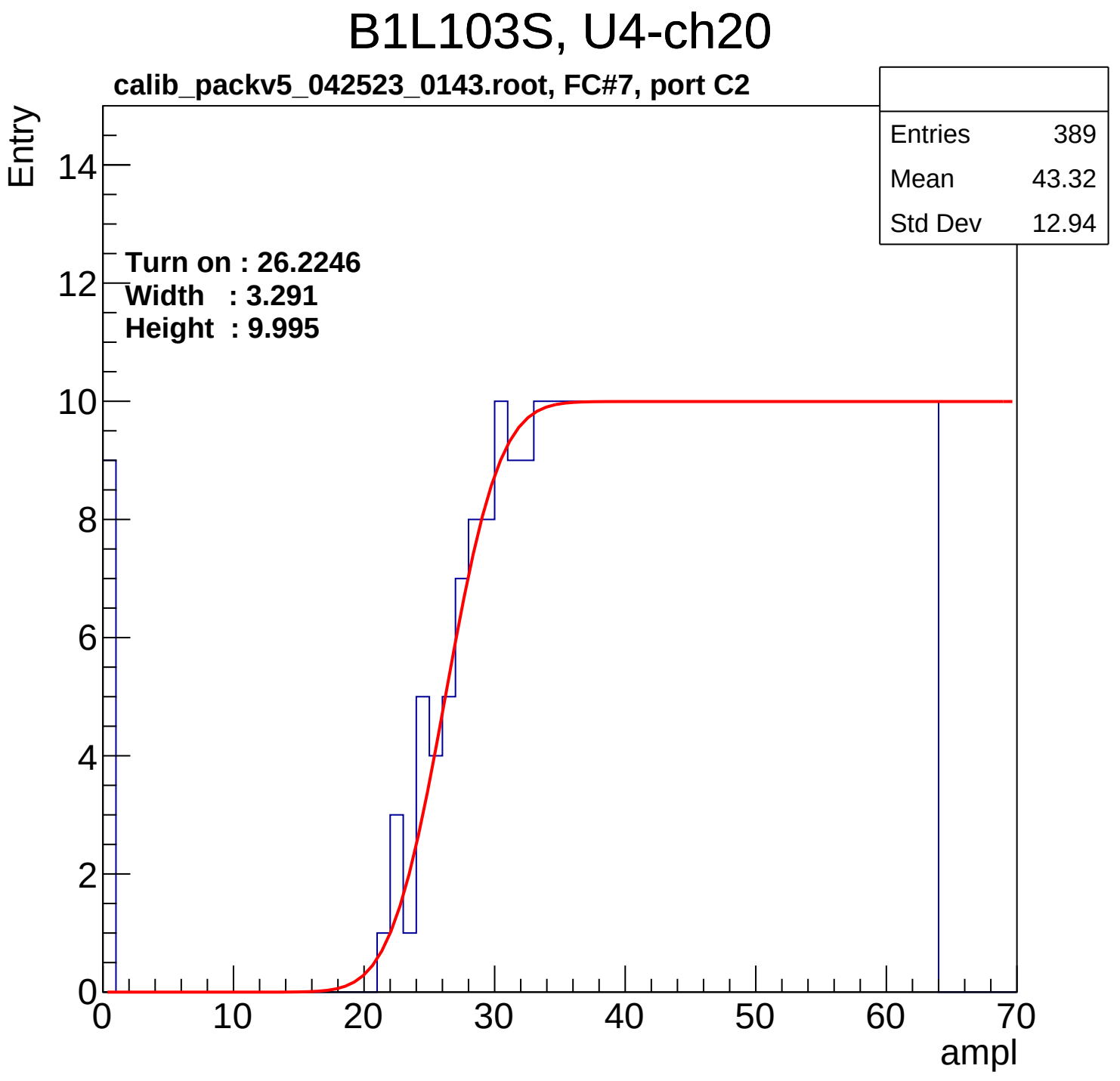
B1L103S, U4-ch20
calib_packv5_042523_0143.root, FC#7, port C2
Entries 389
Mean 43.32
Std Dev 12.94
Turn on : 26.2246
Width : 3.291
Height : 9.995
Entry
ampl
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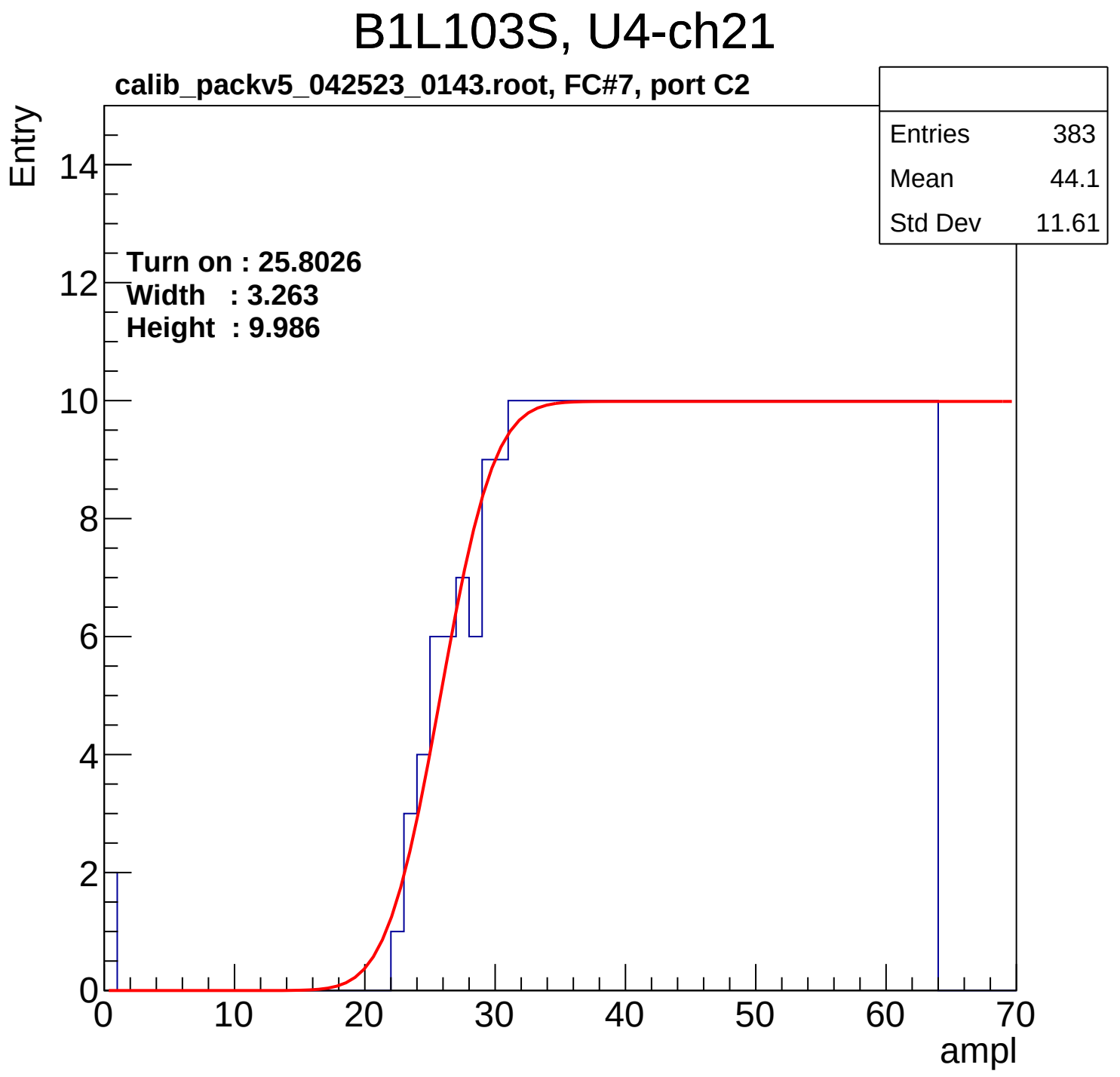
B1L103S, U4-ch21
calib_packv5_042523_0143.root, FC#7, port C2
Entries 383
Mean 44.1
Std Dev 11.61
Turn on : 25.8026
Width : 3.263
Height : 9.986
Entry
ampl
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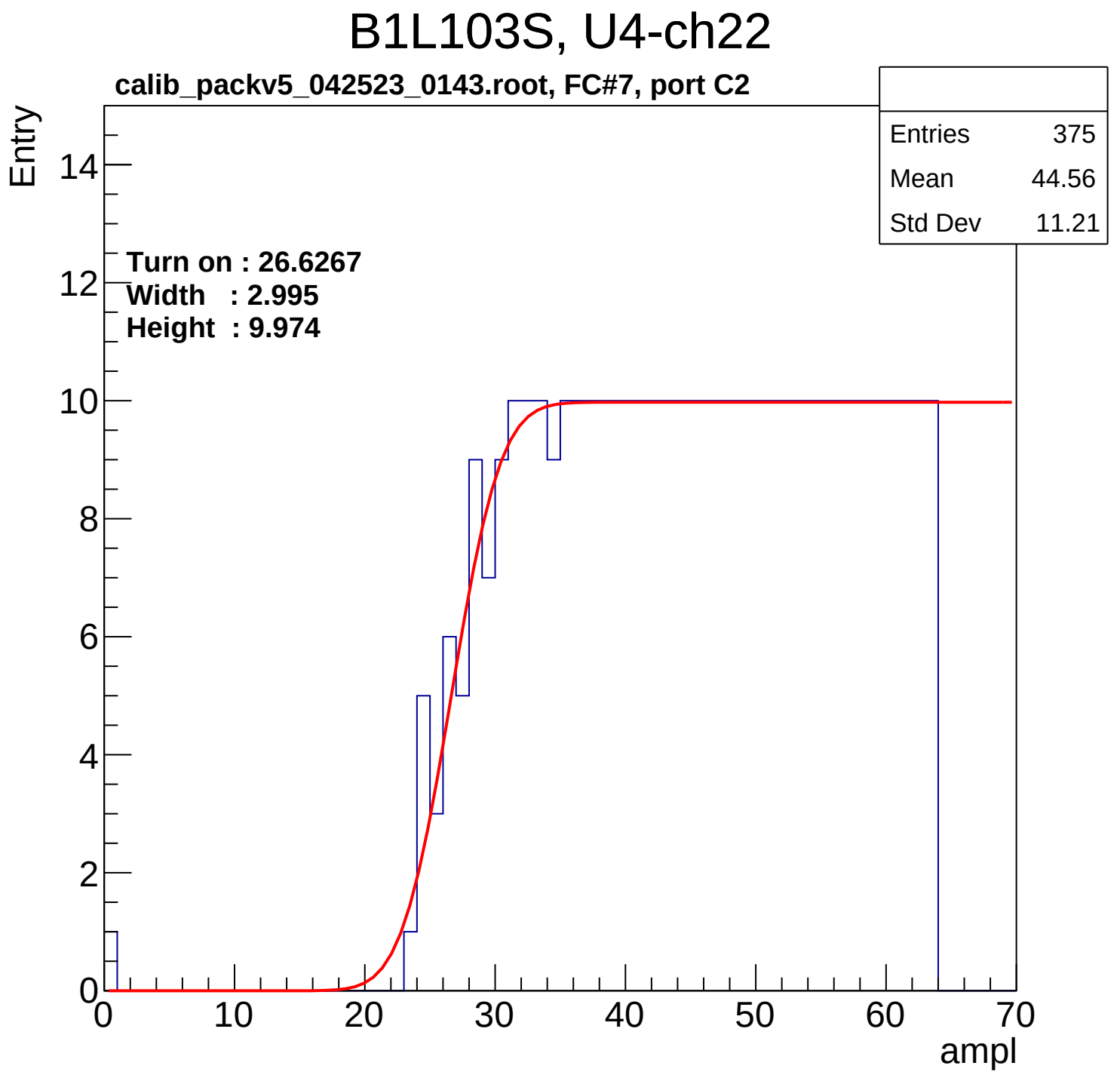
B1L103S, U4-ch22
calib_packv5_042523_0143.root, FC#7, port C2
Entries 375
Mean 44.56
Std Dev 11.21
Turn on : 26.6267
Width : 2.995
Height : 9.974
Entry
ampl
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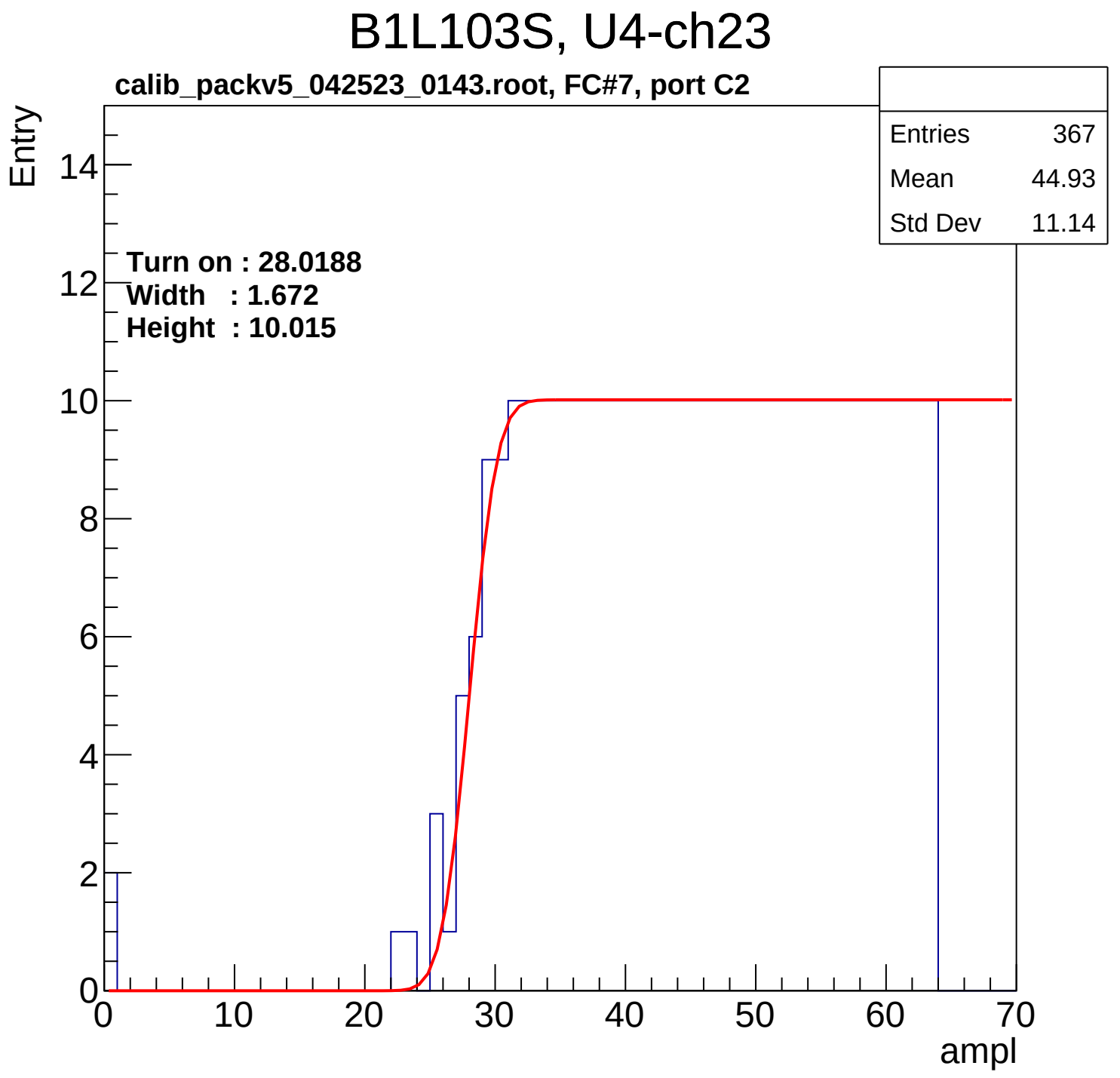
B1L103S, U4-ch23
calib_packv5_042523_0143.root, FC#7, port C2
Entries 367
Mean 44.93
Std Dev 11.14
Turn on : 28.0188
Width : 1.672
Height : 10.015
Entry
ampl
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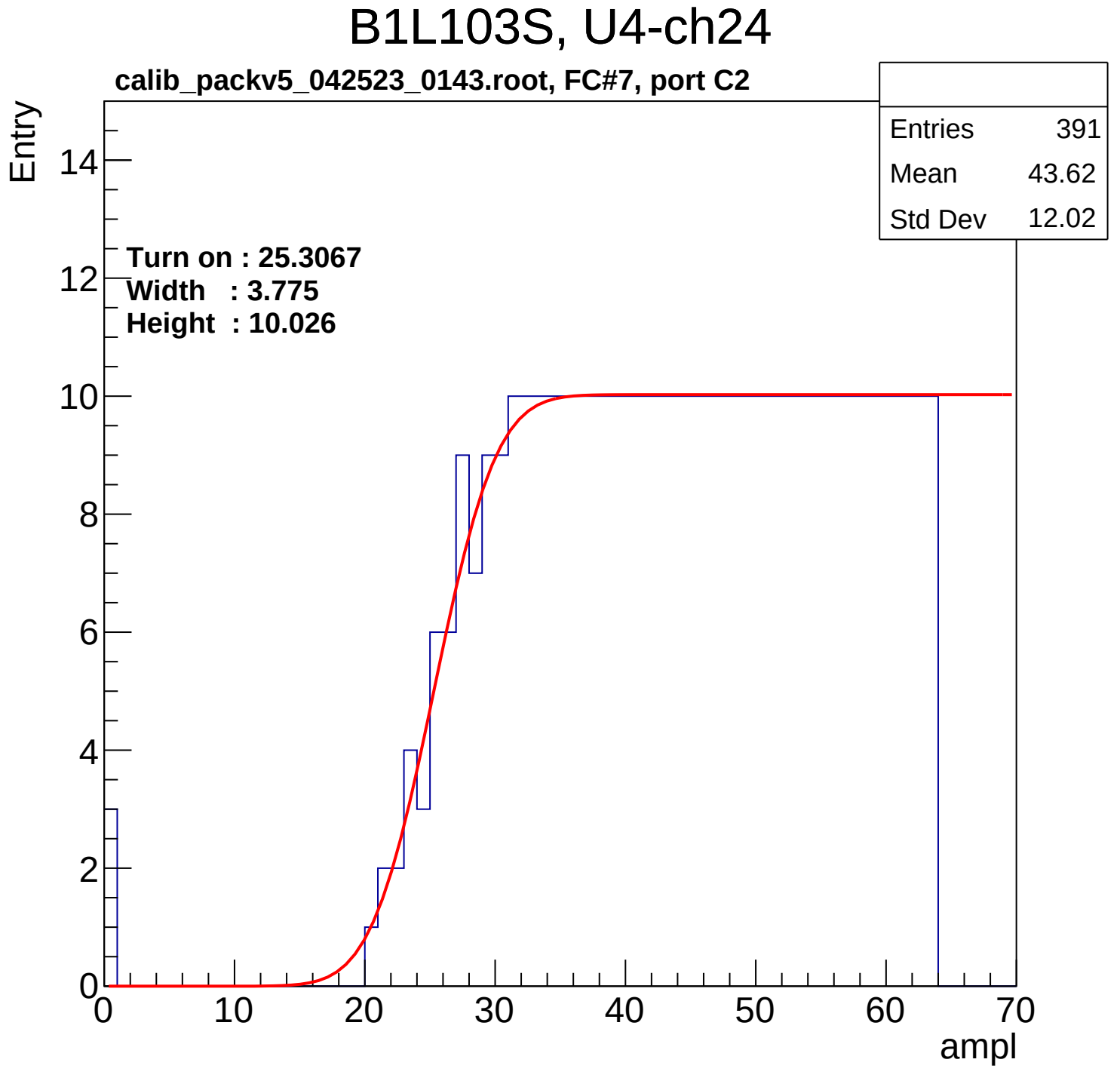
B1L103S, U4-ch24
calib_packv5_042523_0143.root, FC#7, port C2
Entries 391
Mean 43.62
Std Dev 12.02
Turn on : 25.3067
Width : 3.775
Height : 10.026
Entry
ampl
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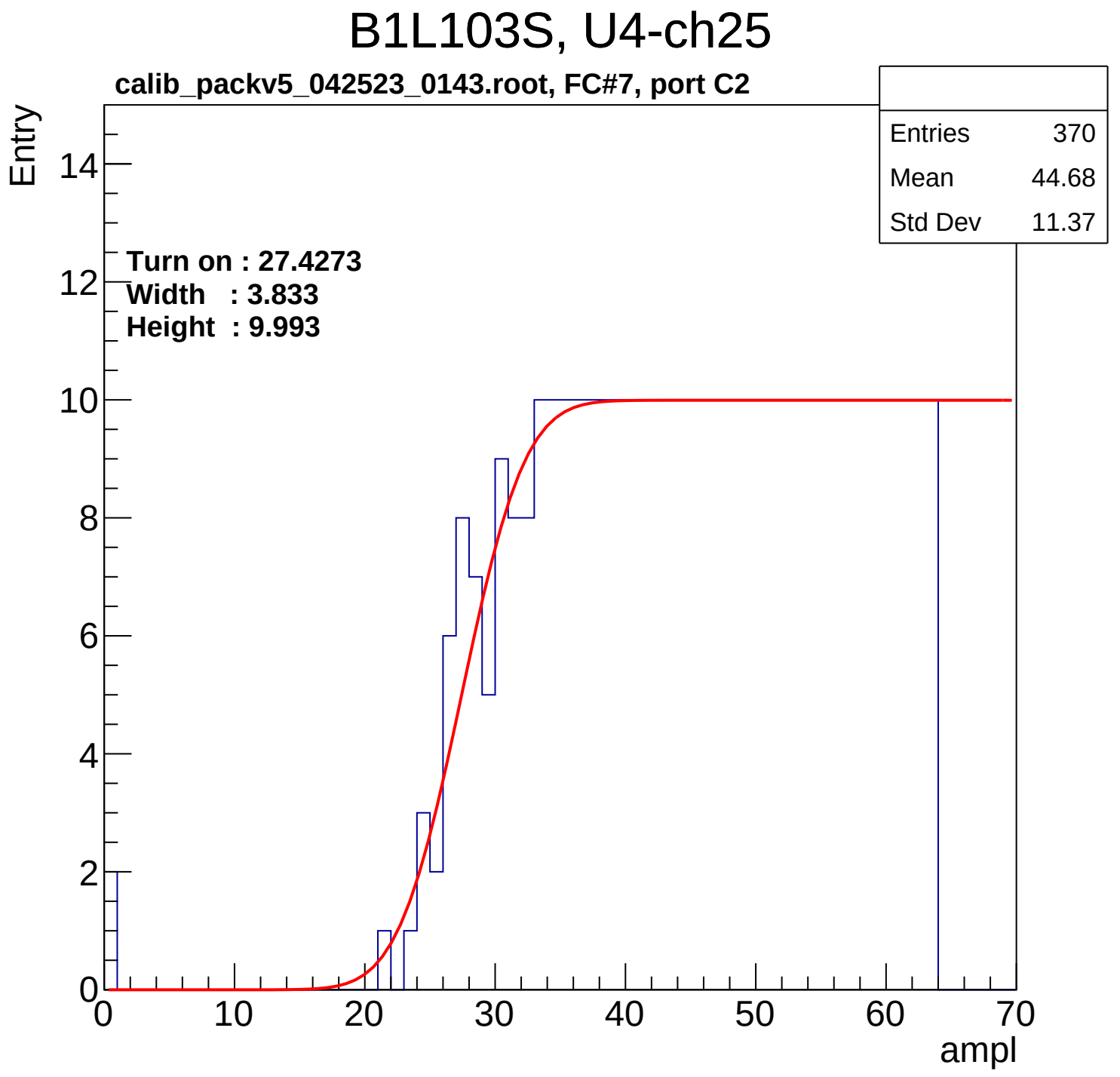
B1L103S, U4-ch25
calib_packv5_042523_0143.root, FC#7, port C2
Entries 370
Mean 44.68
Std Dev 11.37
Turn on : 27.4273
Width : 3.833
Height : 9.993
Entry
ampl
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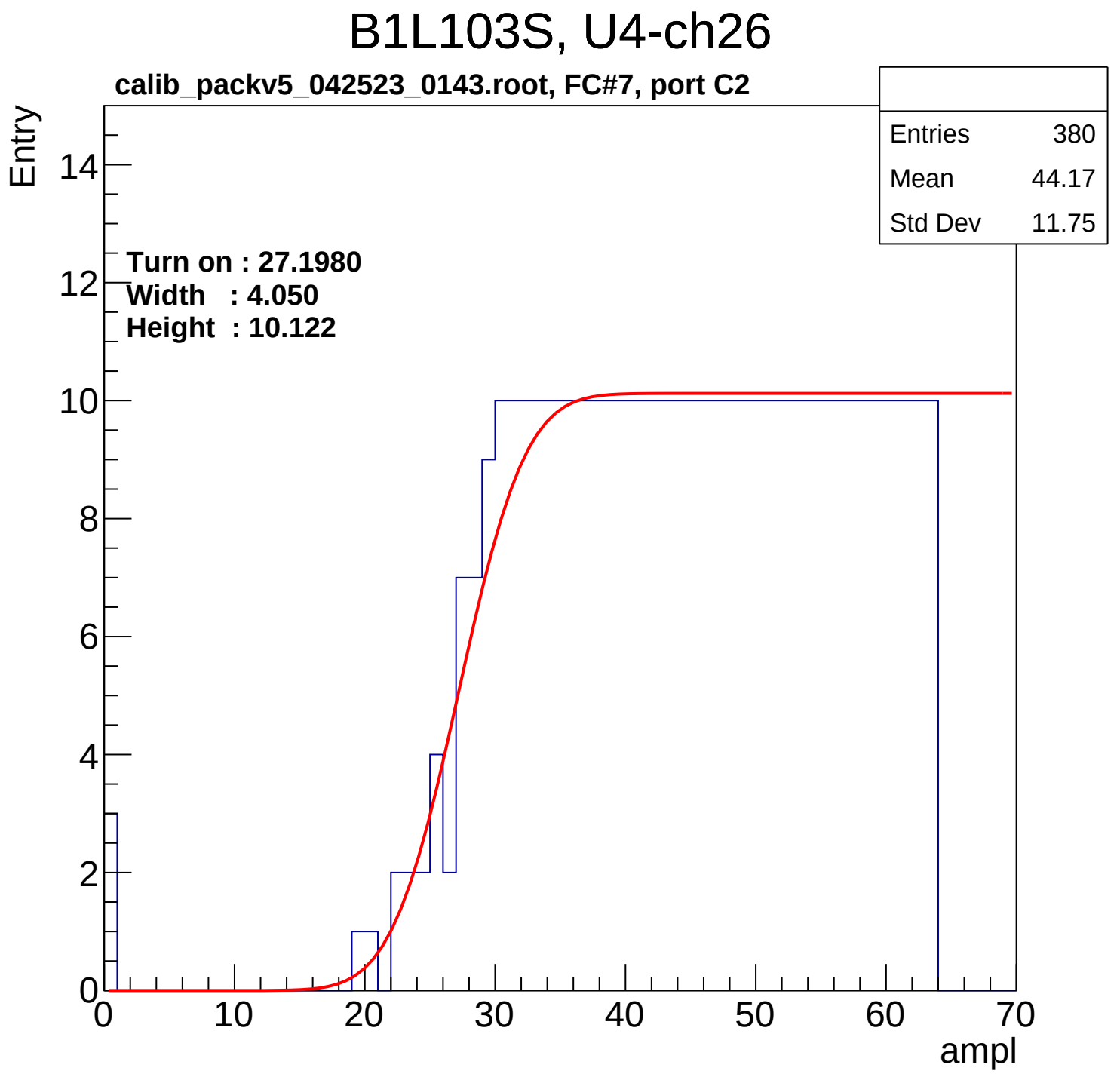
B1L103S, U4-ch26
calib_packv5_042523_0143.root, FC#7, port C2
Entries 380
Mean 44.17
Std Dev 11.75
Turn on : 27.1980
Width : 4.050
Height : 10.122
Entry
ampl
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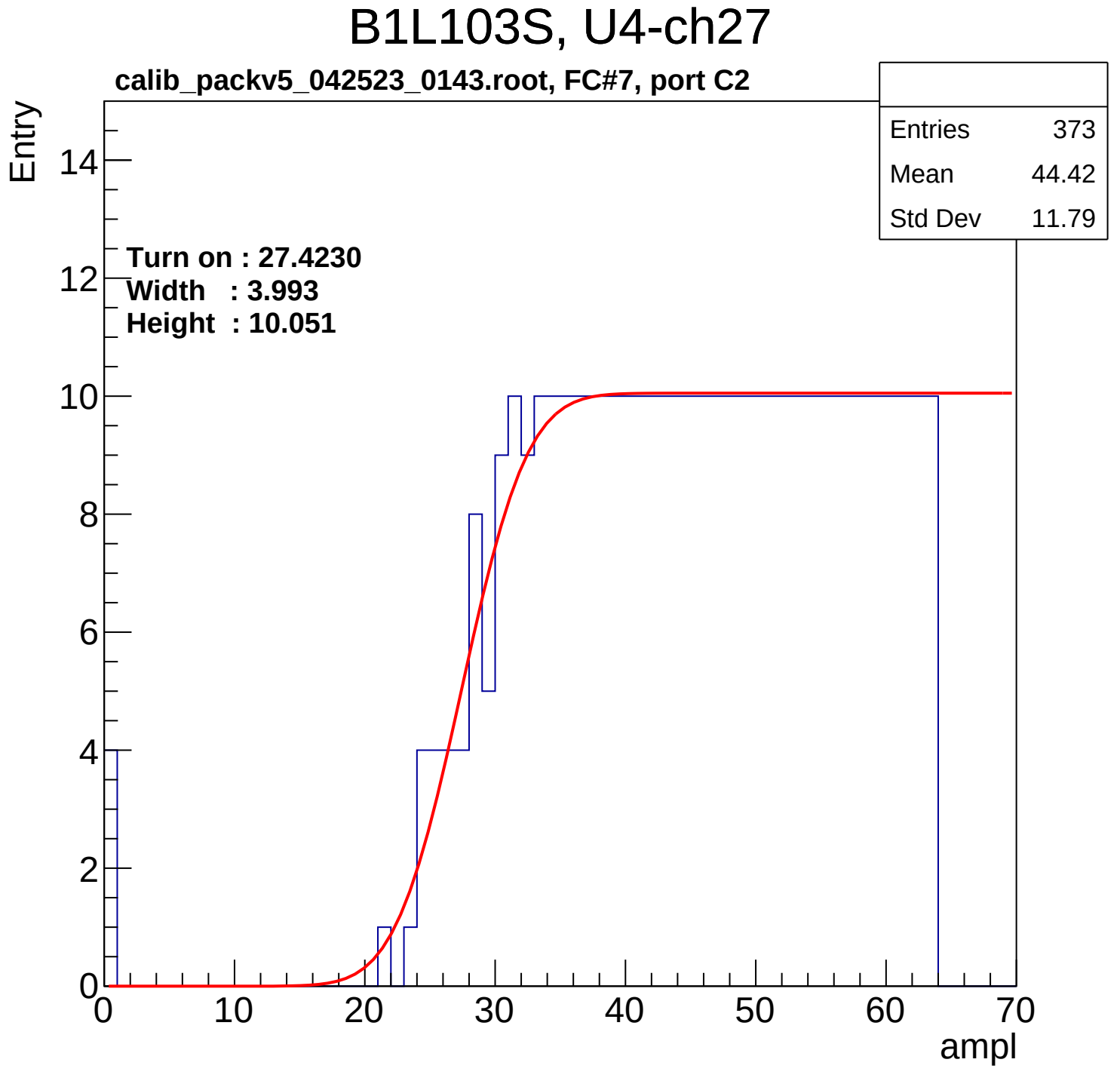
B1L103S, U4-ch27
calib_packv5_042523_0143.root, FC#7, port C2
Entries 373
Mean 44.42
Std Dev 11.79
Turn on : 27.4230
Width : 3.993
Height : 10.051
Entry
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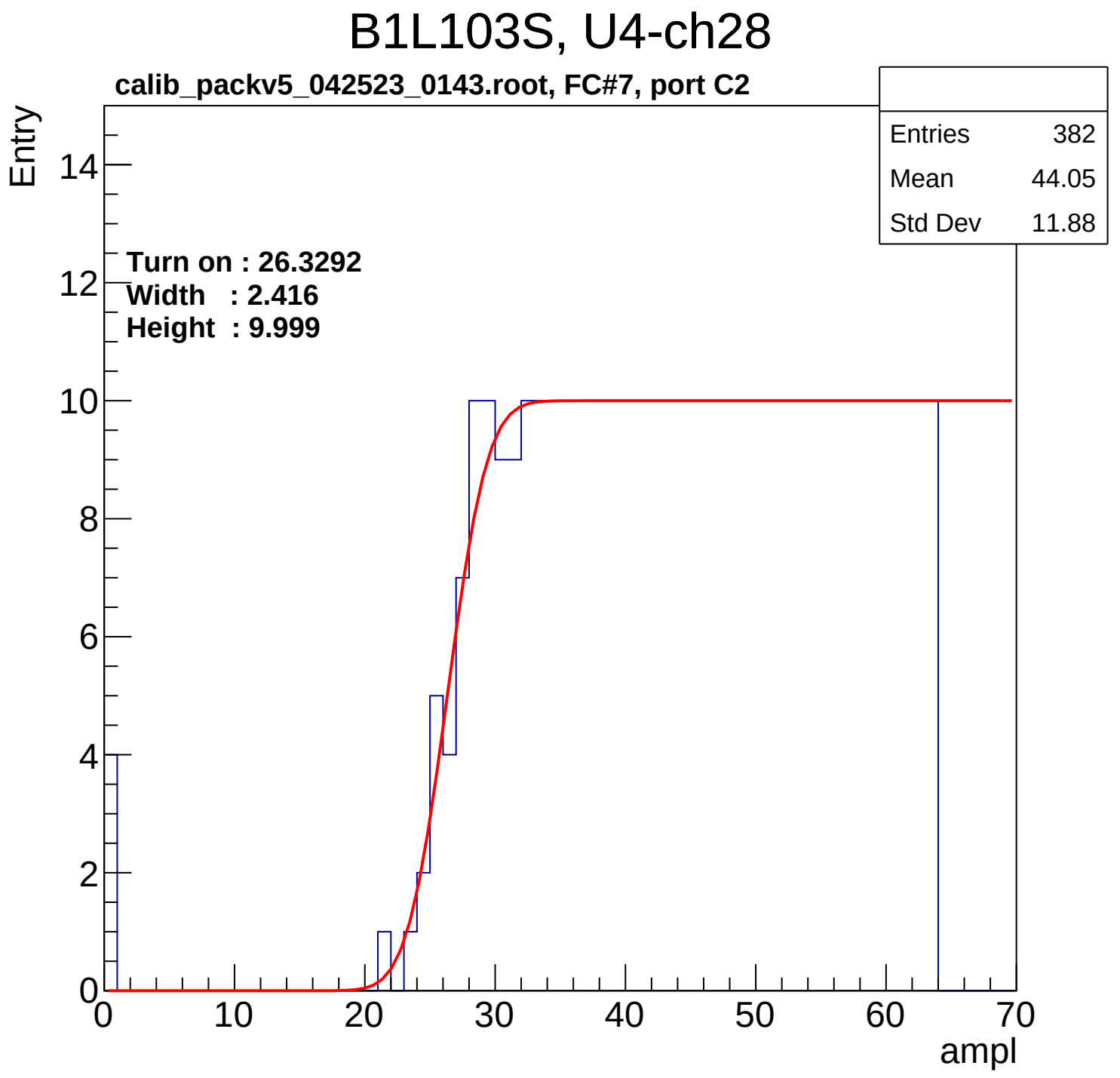
B1L103S, U4-ch28
calib_packv5_042523_0143.root, FC#7, port C2
Entries 382
Mean 44.05
Std Dev 11.88
Turn on : 26.3292
Width : 2.416
Height : 9.999
Entry
ampl
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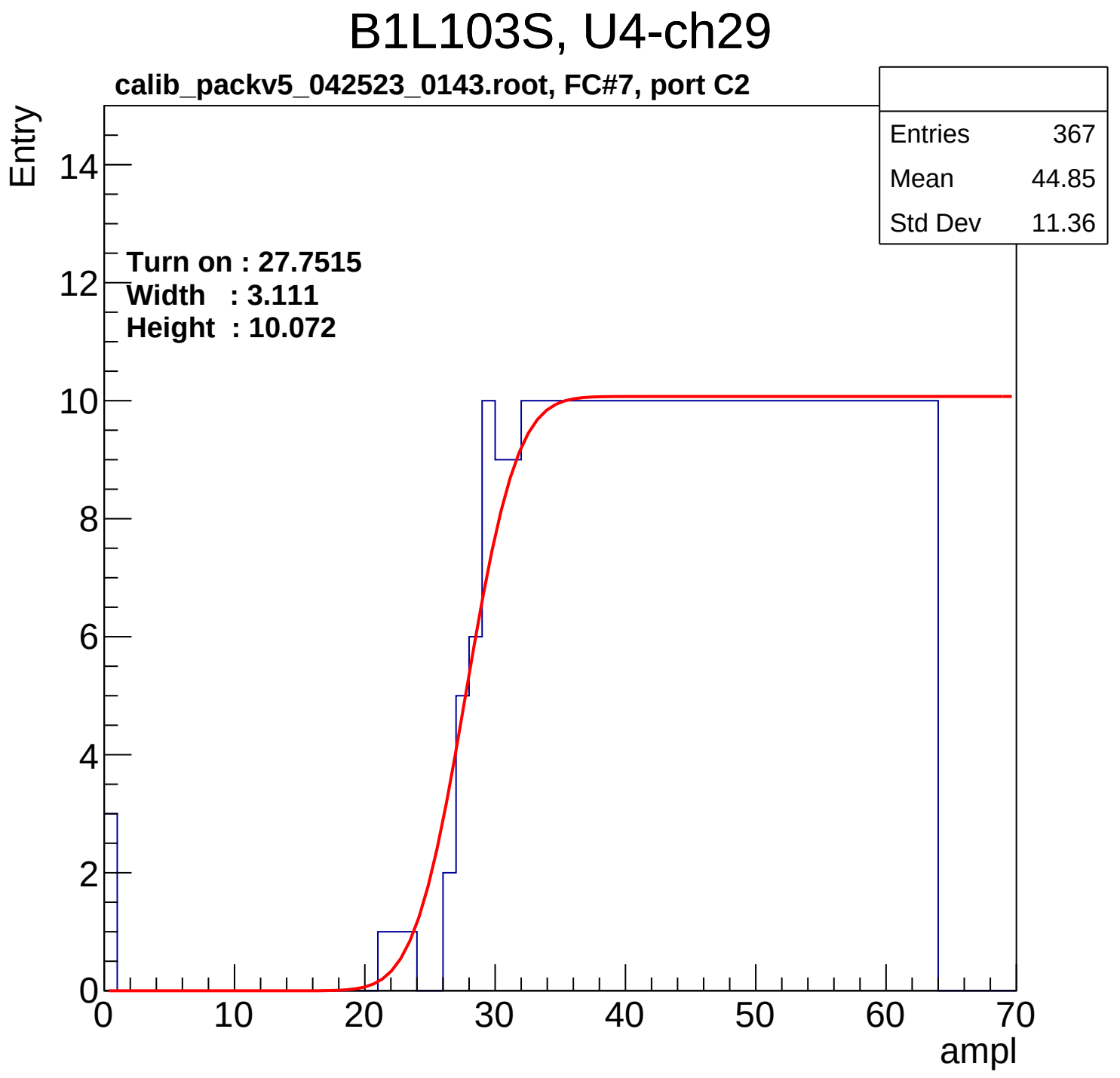
B1L103S, U4-ch29
calib_packv5_042523_0143.root, FC#7, port C2
Entries 367
Mean 44.85
Std Dev 11.36
Turn on : 27.7515
Width : 3.111
Height : 10.072
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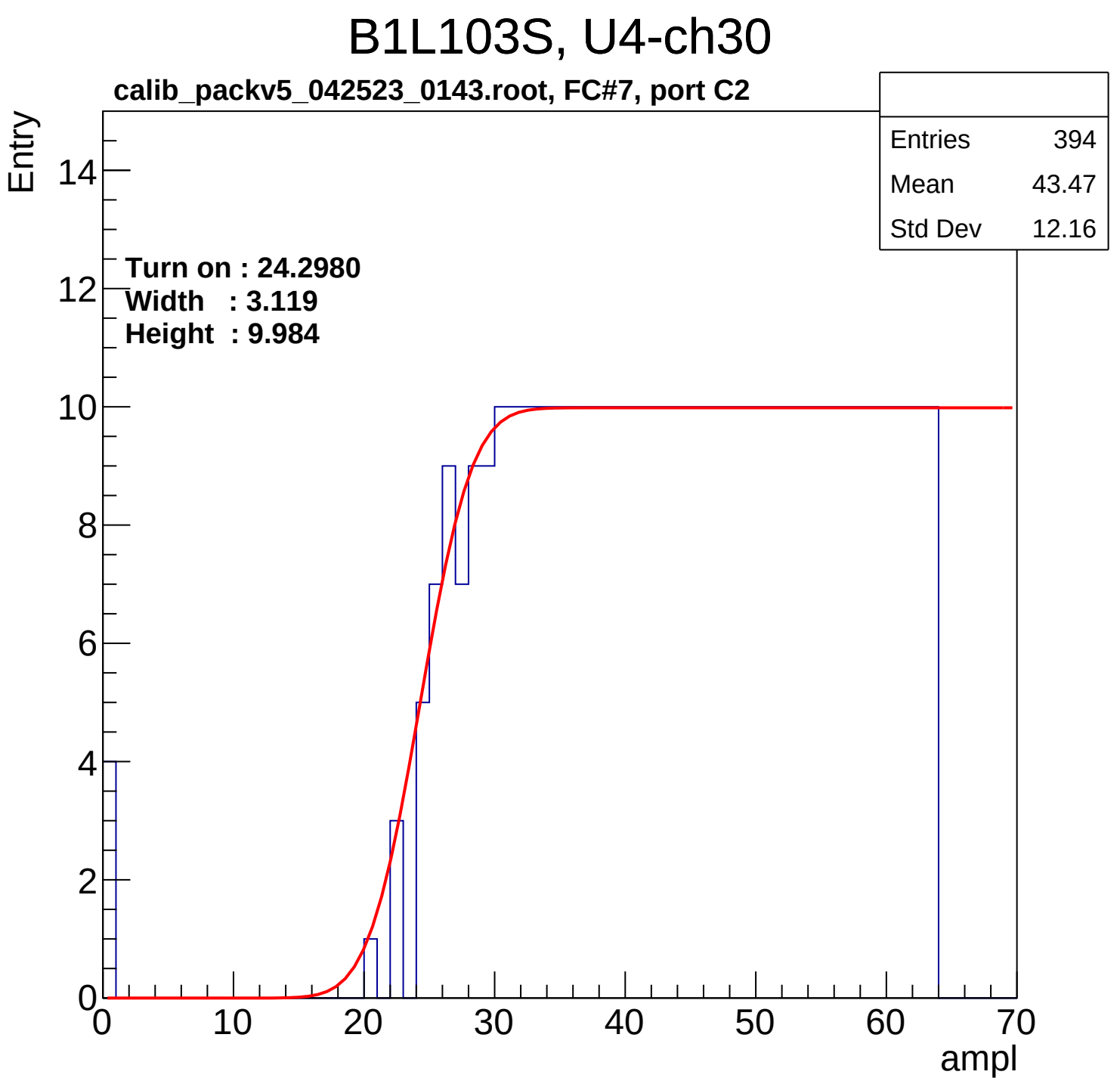
B1L103S, U4-ch30
calib_packv5_042523_0143.root, FC#7, port C2
Entries 394
Mean 43.47
Std Dev 12.16
Turn on : 24.2980
Width : 3.119
Height : 9.984
Entry
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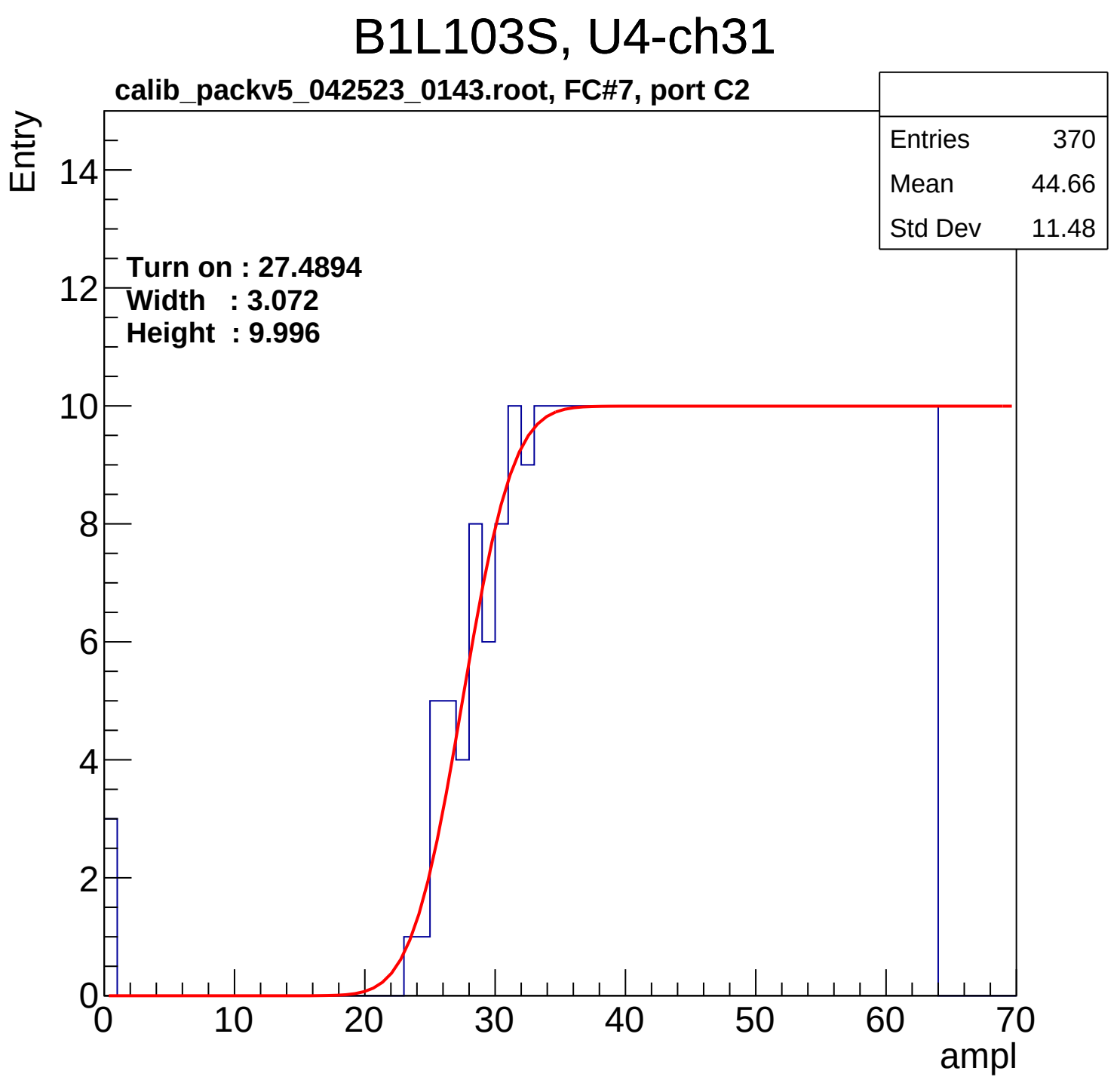
B1L103S, U4-ch31
calib_packv5_042523_0143.root, FC#7, port C2
Entries 370
Mean 44.66
Std Dev 11.48
Turn on : 27.4894
Width : 3.072
Height : 9.996
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ampl
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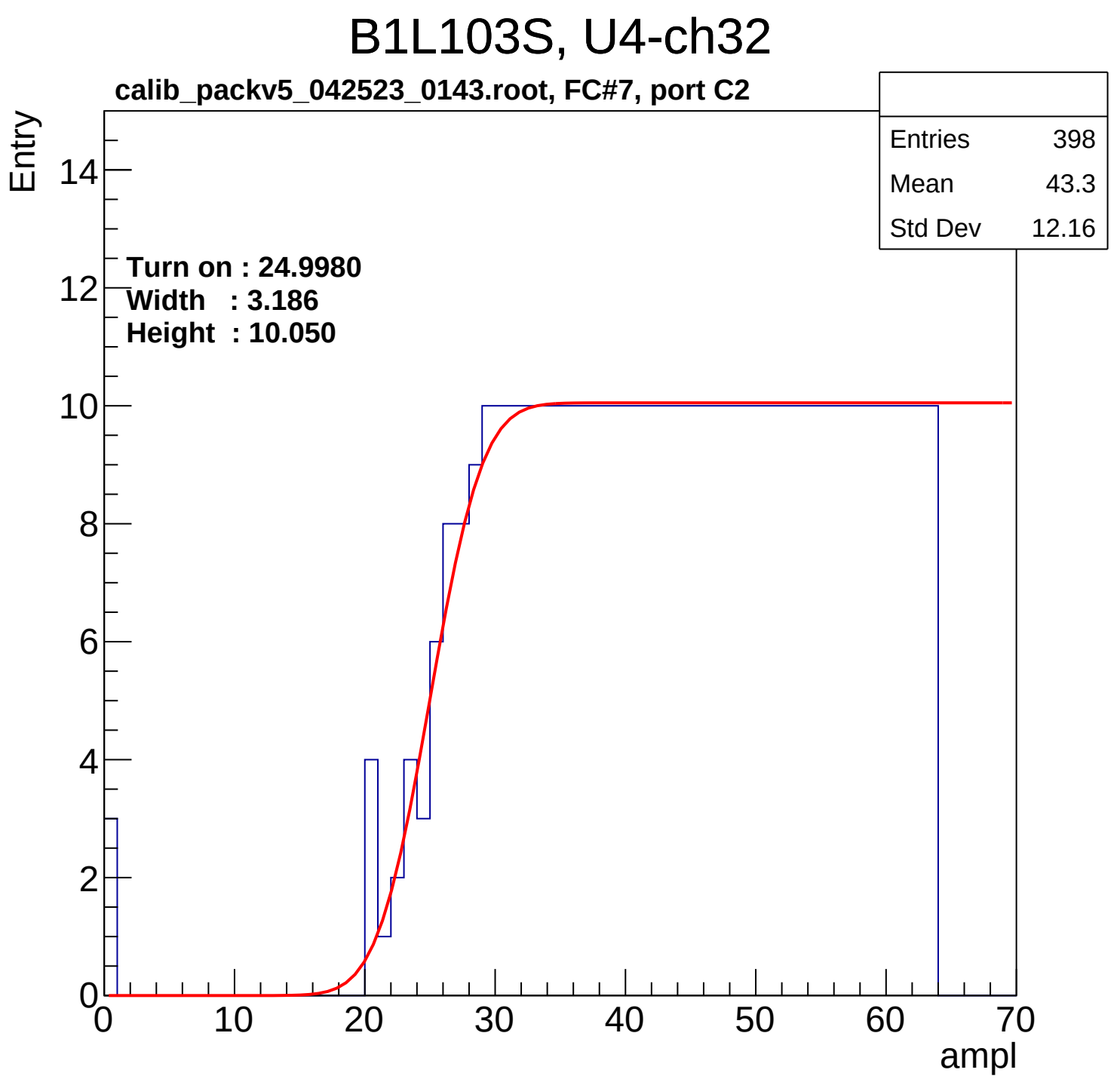
B1L103S, U4-ch32
calib_packv5_042523_0143.root, FC#7, port C2
Entries 398
Mean 43.3
Std Dev 12.16
Turn on : 24.9980
Width : 3.186
Height : 10.050
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ampl
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4
6
8
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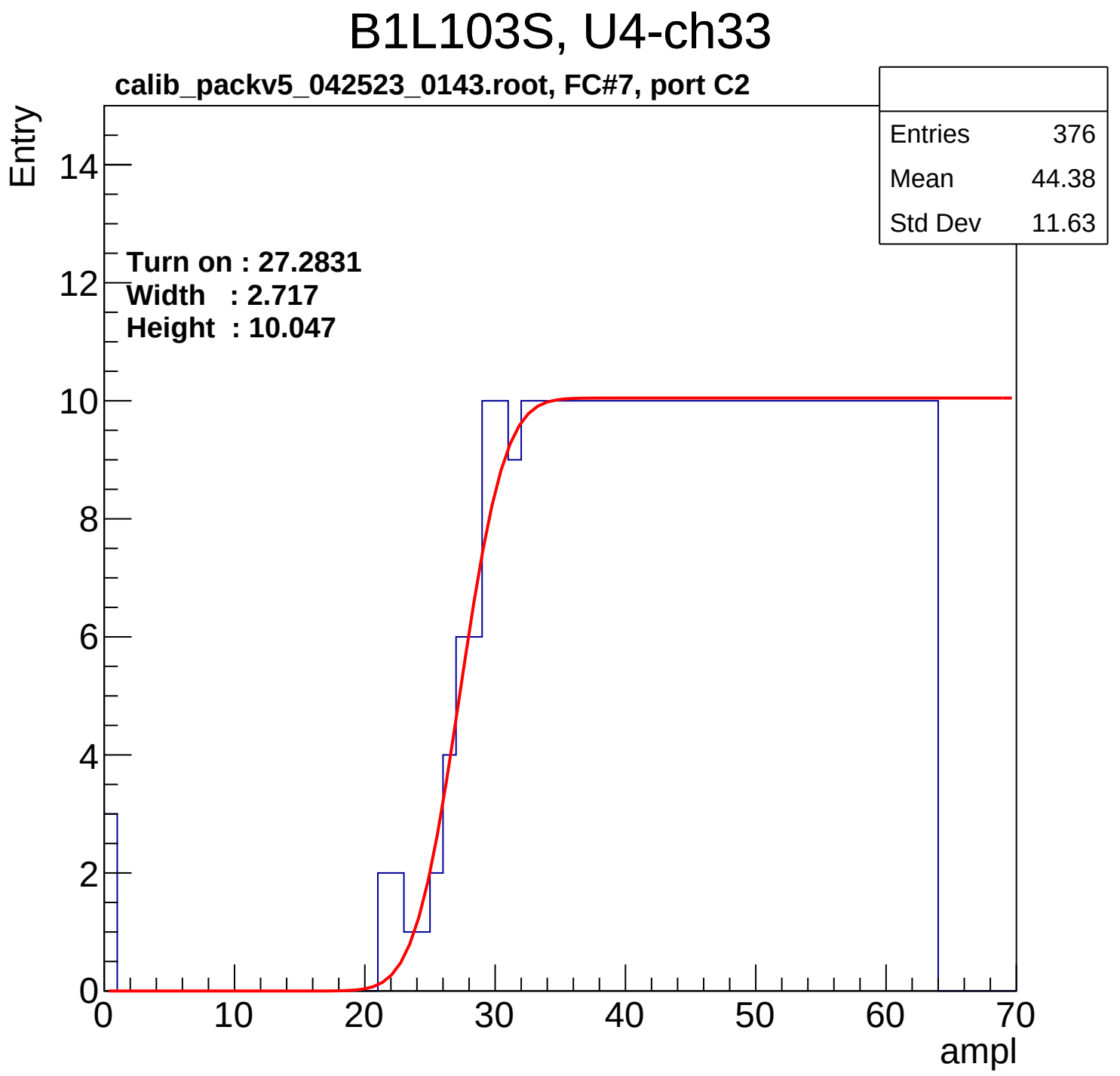
B1L103S, U4-ch33
calib_packv5_042523_0143.root, FC#7, port C2
Entries 376
Mean 44.38
Std Dev 11.63
Turn on : 27.2831
Width : 2.717
Height : 10.047
Entry
ampl
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6
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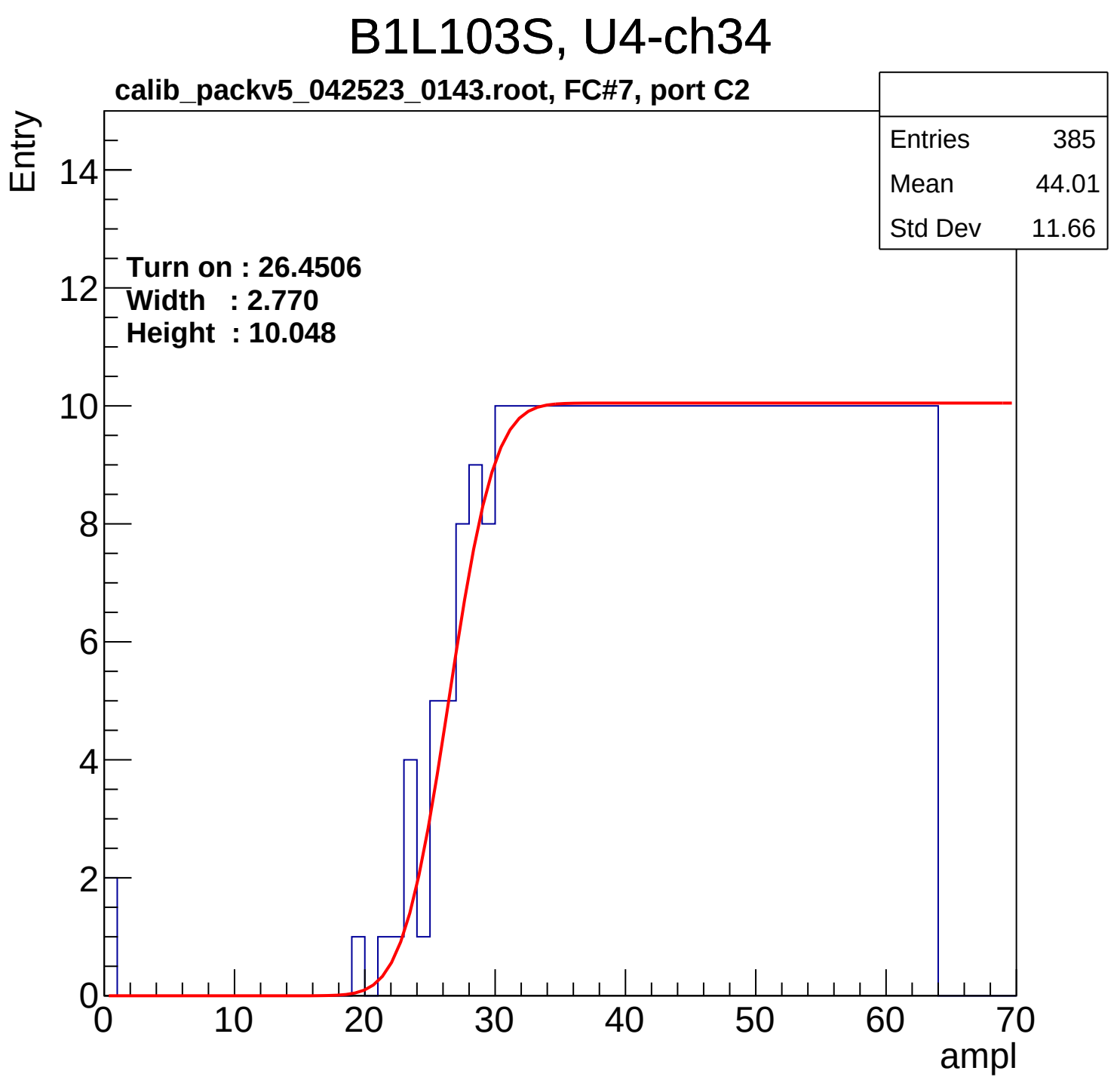
B1L103S, U4-ch34
calib_packv5_042523_0143.root, FC#7, port C2
Entries 385
Mean 44.01
Std Dev 11.66
Turn on : 26.4506
Width : 2.770
Height : 10.048
Entry
ampl
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6
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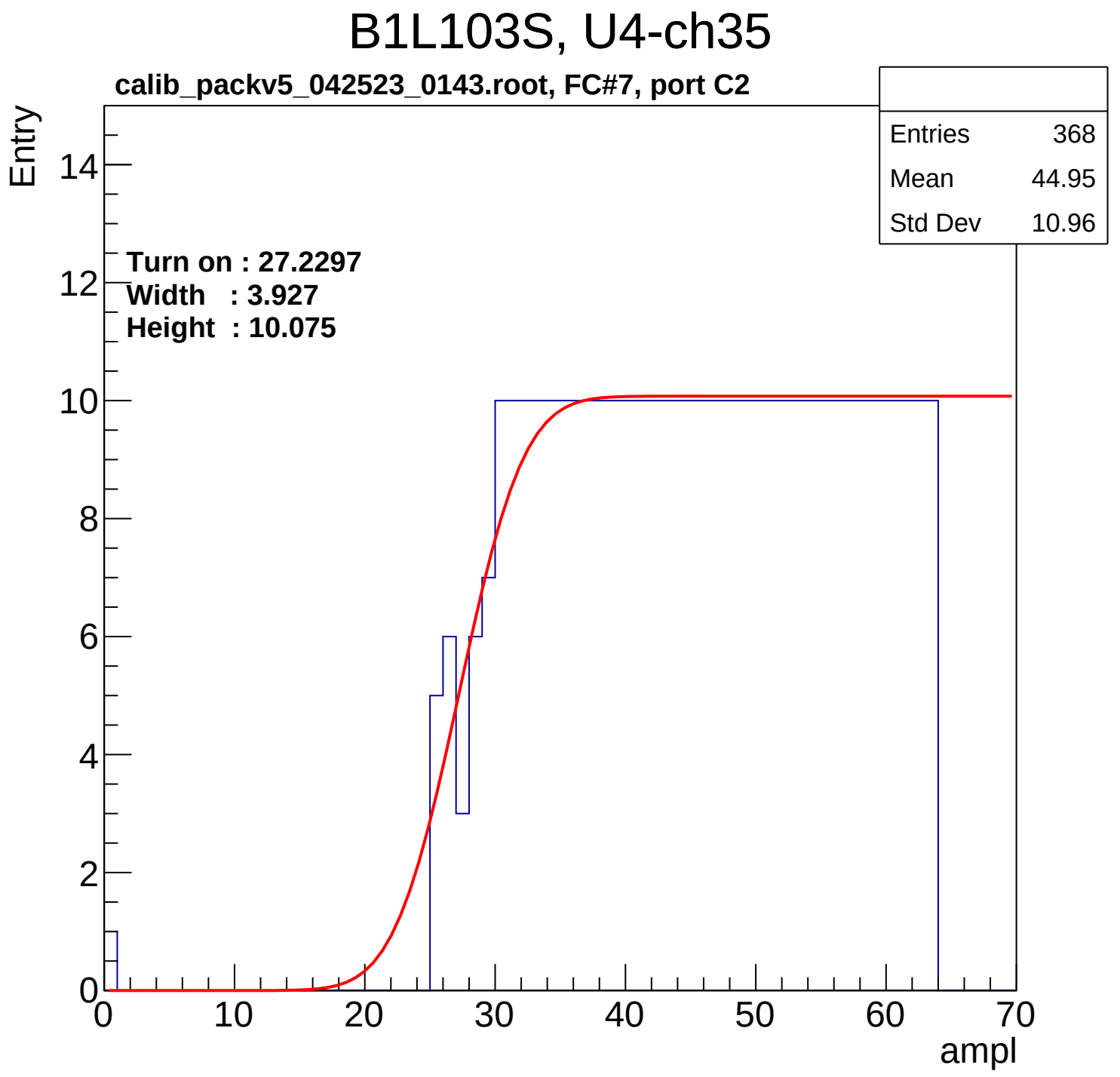
B1L103S, U4-ch35
calib_packv5_042523_0143.root, FC#7, port C2
Entries 368
Mean 44.95
Std Dev 10.96
Turn on : 27.2297
Width : 3.927
Height : 10.075
Entry
ampl
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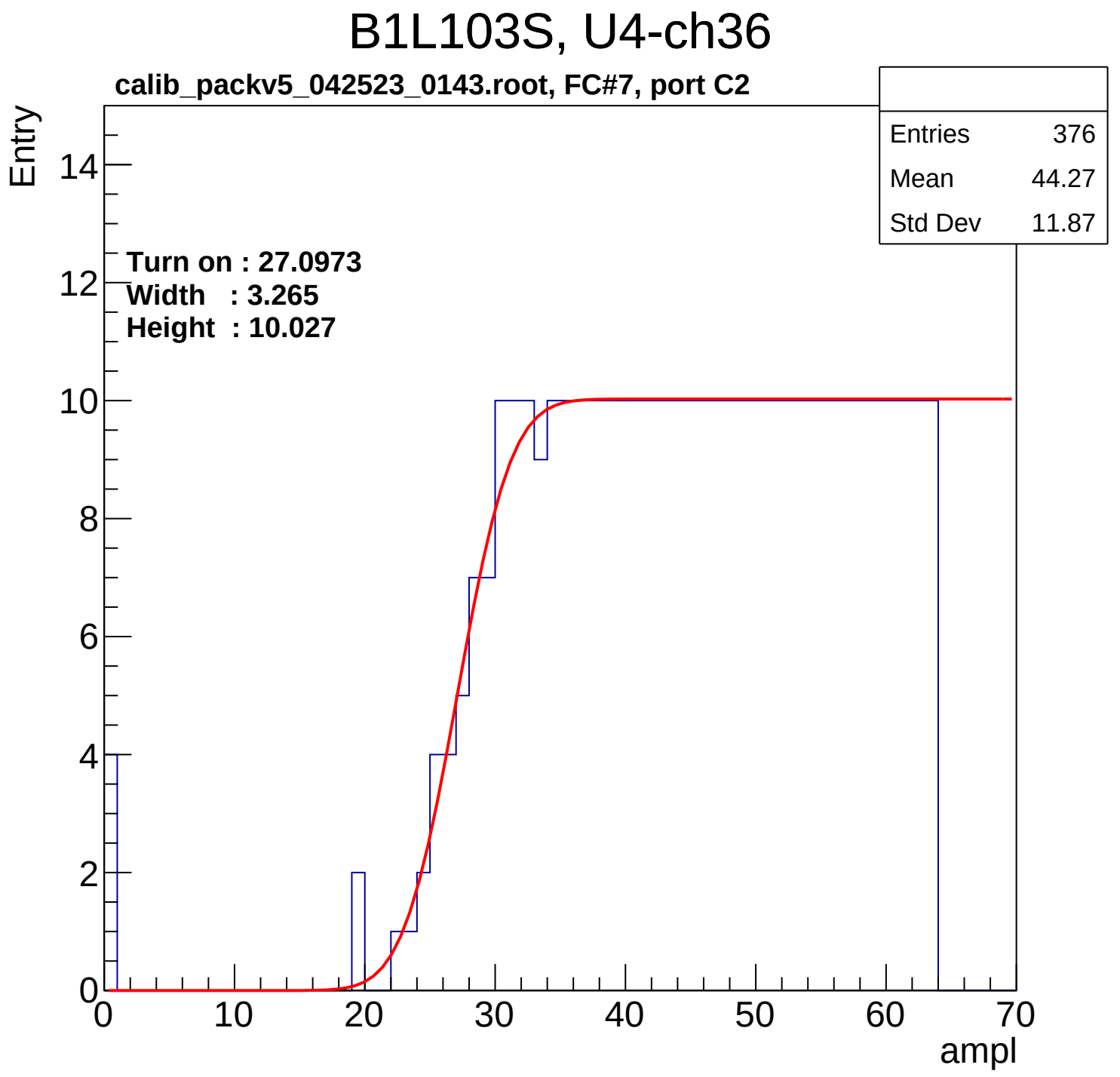
B1L103S, U4-ch36
calib_packv5_042523_0143.root, FC#7, port C2
Entries 376
Mean 44.27
Std Dev 11.87
Turn on : 27.0973
Width : 3.265
Height : 10.027
Entry
ampl
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6
8
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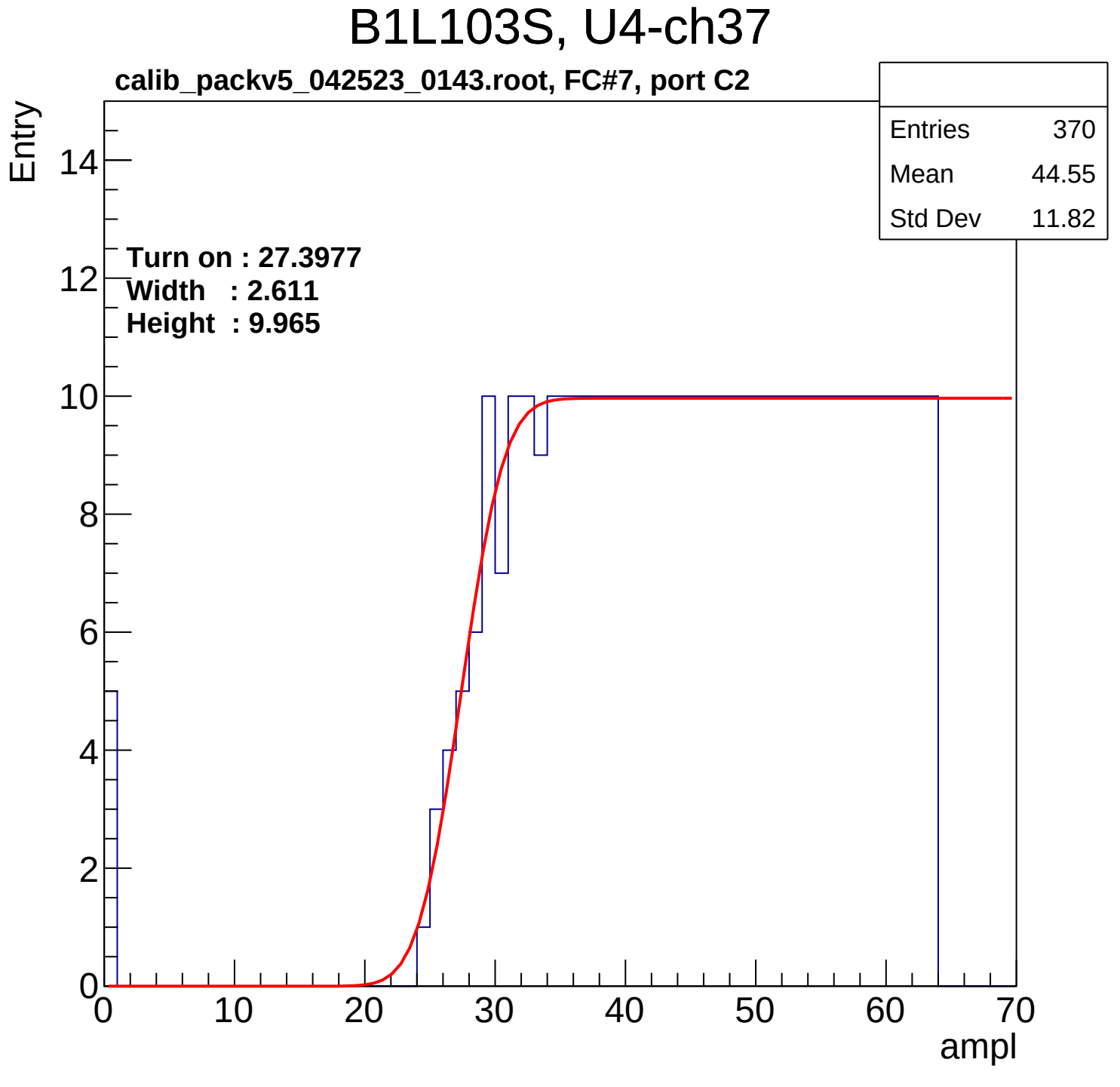
B1L103S, U4-ch37
calib_packv5_042523_0143.root, FC#7, port C2
Entries 370
Mean 44.55
Std Dev 11.82
Turn on : 27.3977
Width : 2.611
Height : 9.965
Entry
ampl
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6
8
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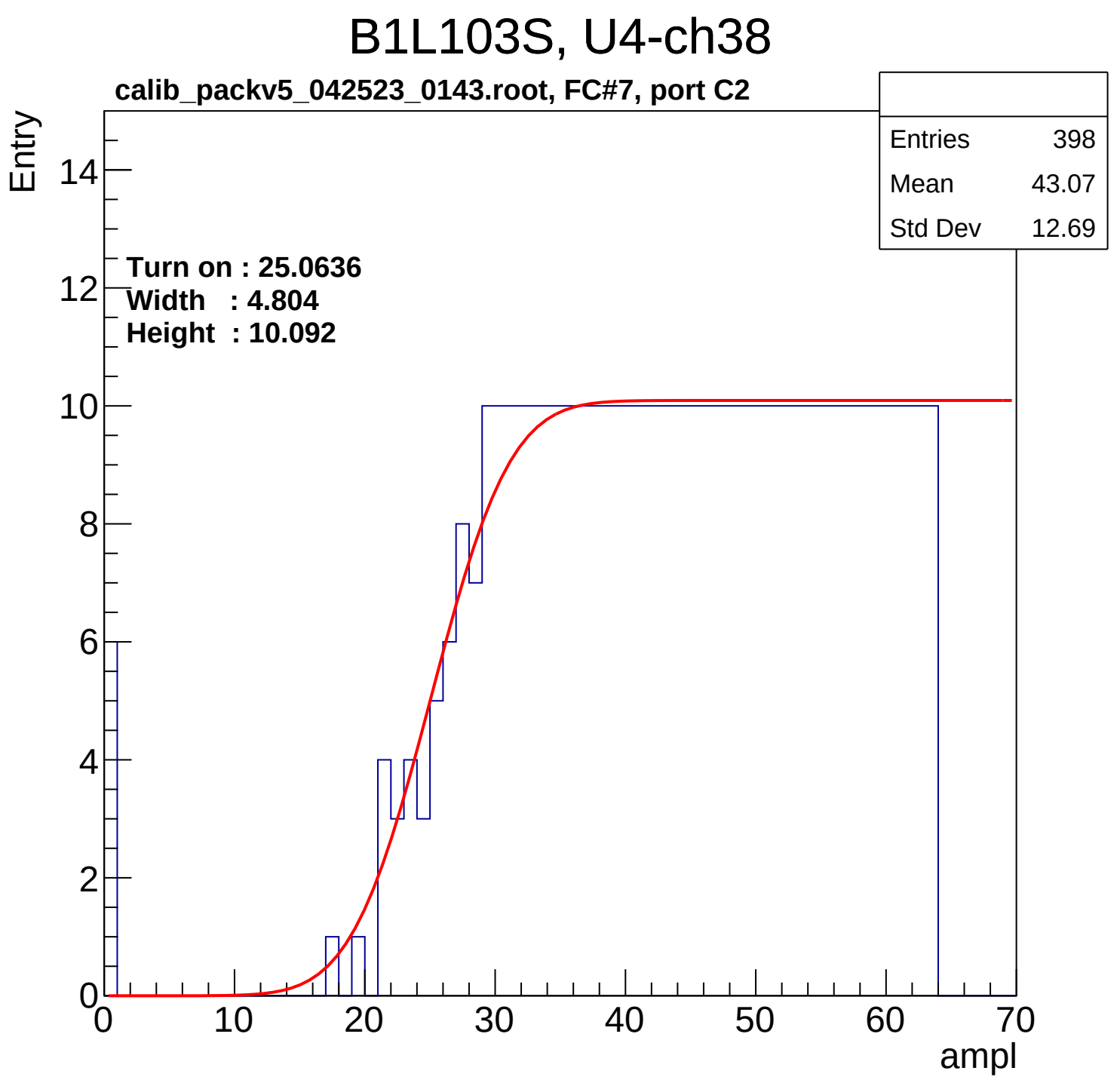
B1L103S, U4-ch38
calib_packv5_042523_0143.root, FC#7, port C2
Entries 398
Mean 43.07
Std Dev 12.69
Turn on : 25.0636
Width : 4.804
Height : 10.092
Entry
ampl
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6
8
10
12
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60
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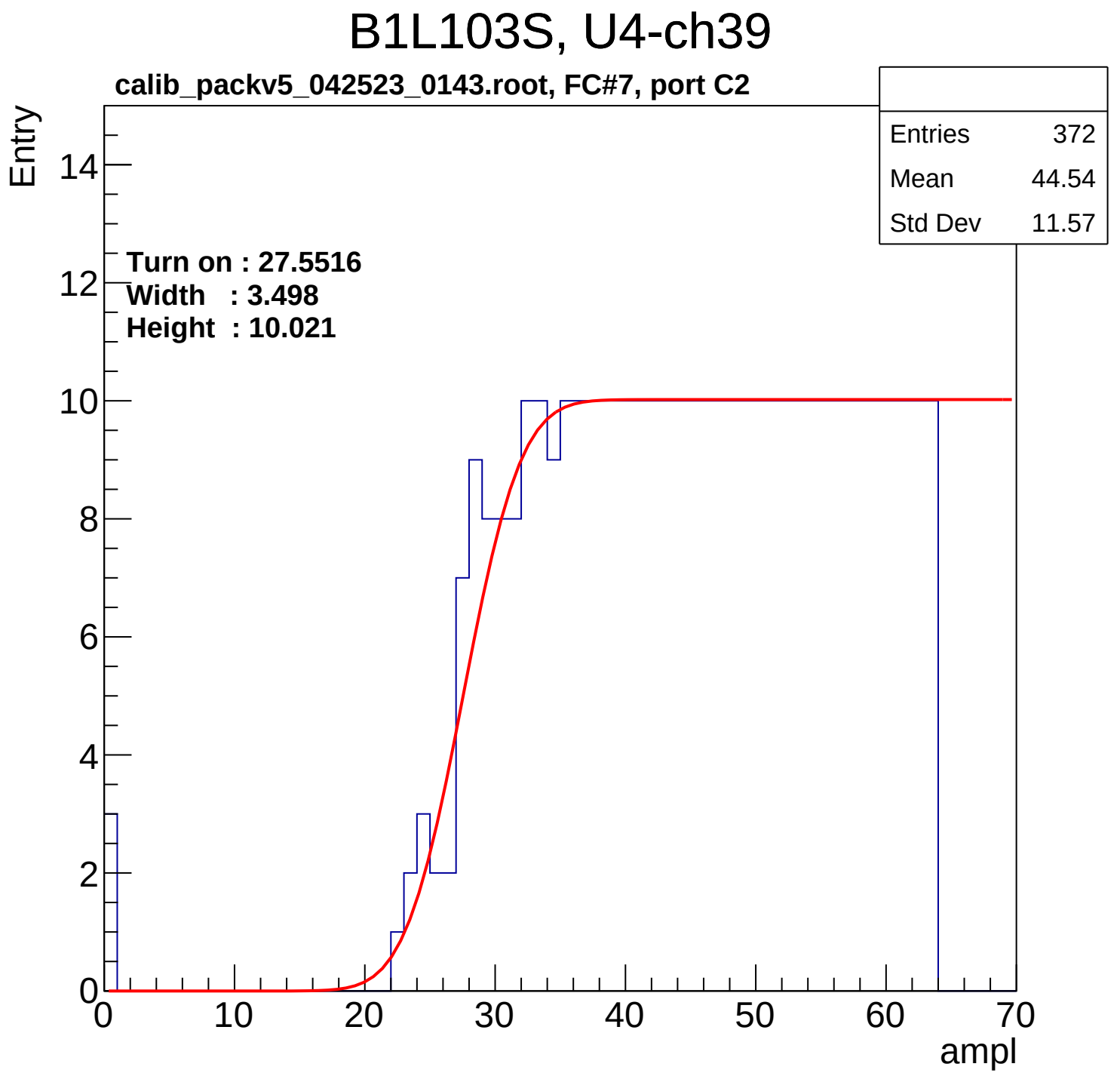
B1L103S, U4-ch39
calib_packv5_042523_0143.root, FC#7, port C2
Entries 372
Mean 44.54
Std Dev 11.57
Turn on : 27.5516
Width : 3.498
Height : 10.021
Entry
ampl
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6
8
10
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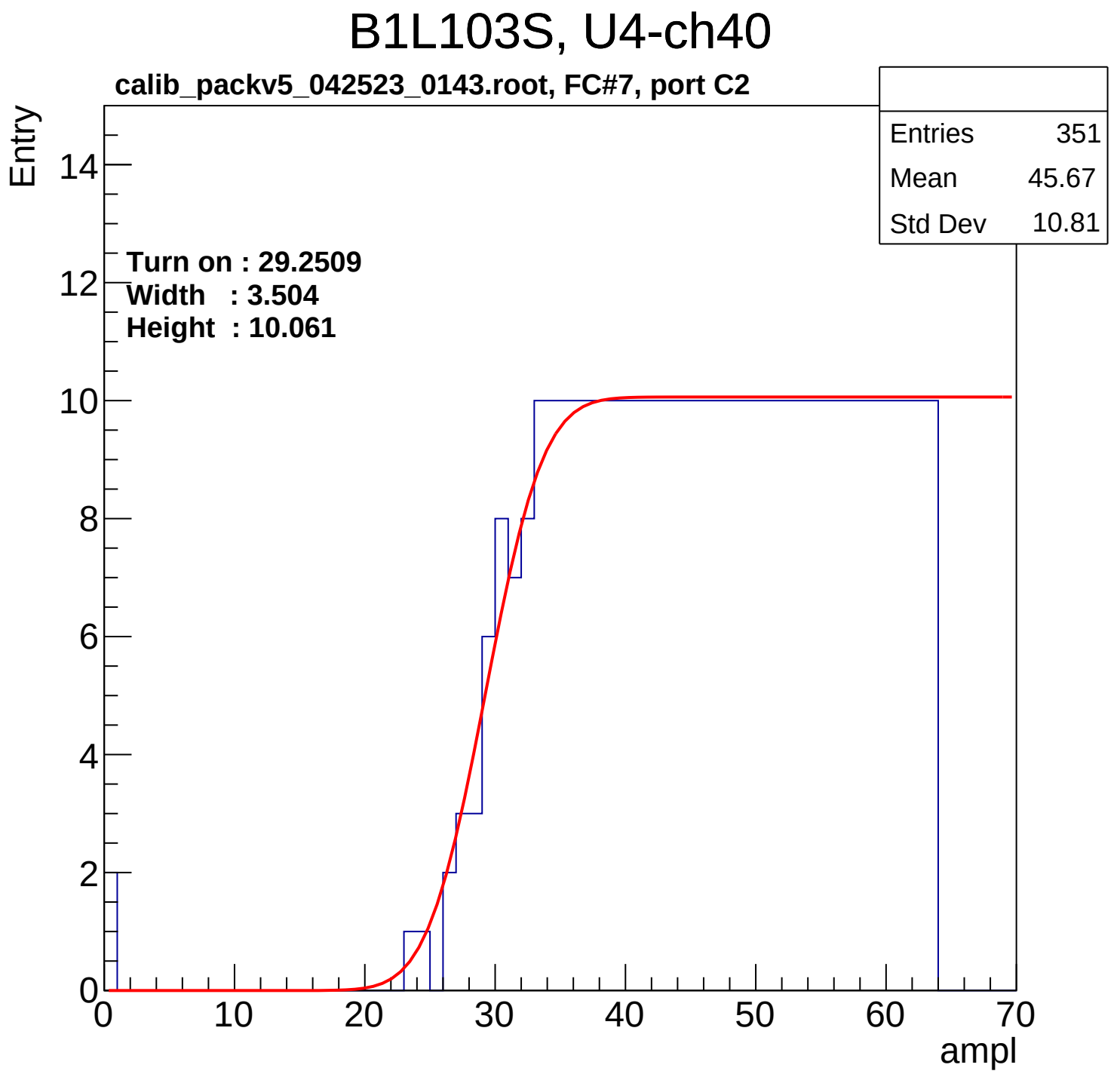
B1L103S, U4-ch40
calib_packv5_042523_0143.root, FC#7, port C2
Entries 351
Mean 45.67
Std Dev 10.81
Turn on : 29.2509
Width : 3.504
Height : 10.061
Entry
ampl
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6
8
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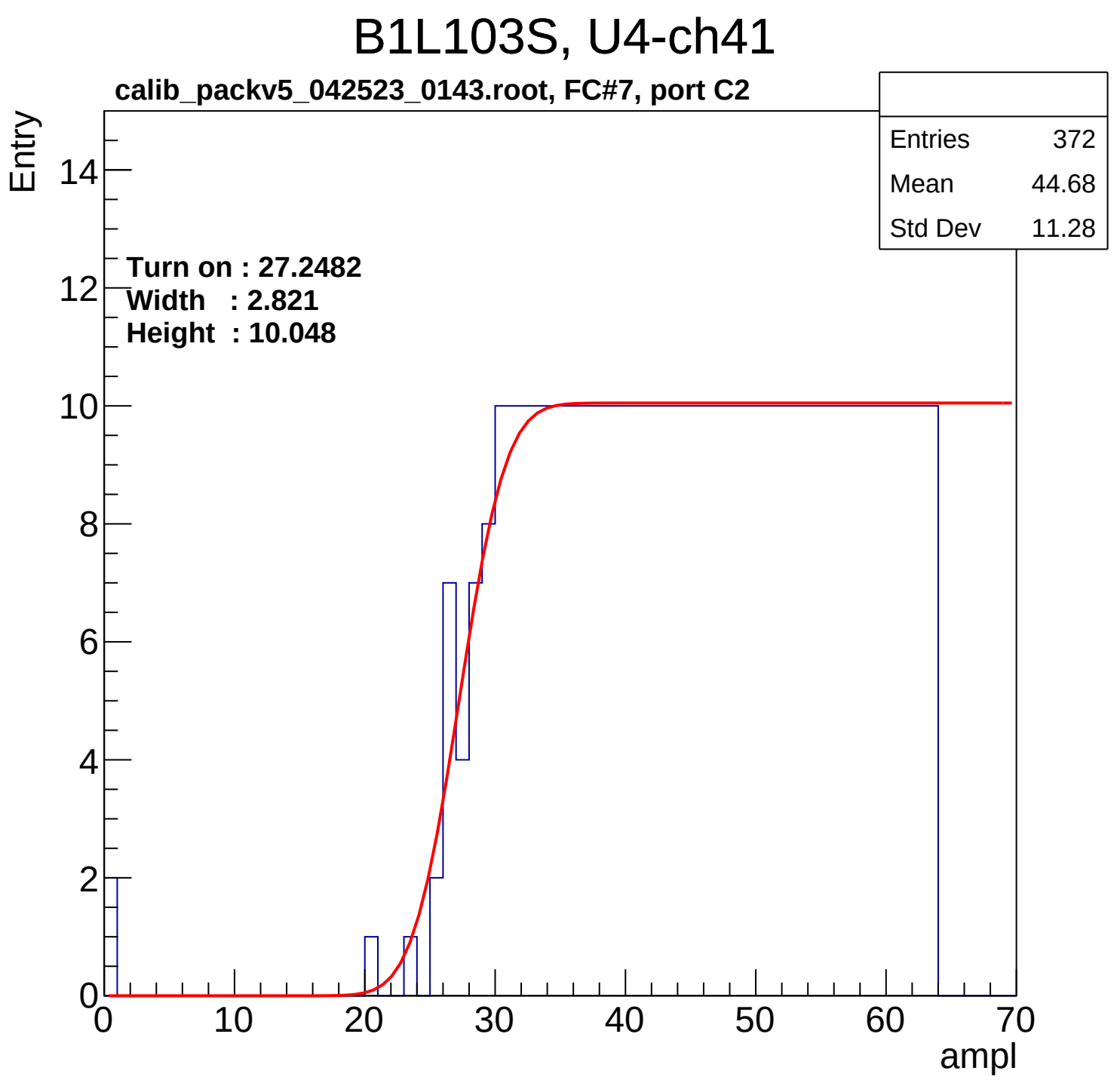
B1L103S, U4-ch41
calib_packv5_042523_0143.root, FC#7, port C2
Entries 372
Mean 44.68
Std Dev 11.28
Turn on : 27.2482
Width : 2.821
Height : 10.048
Entry
ampl
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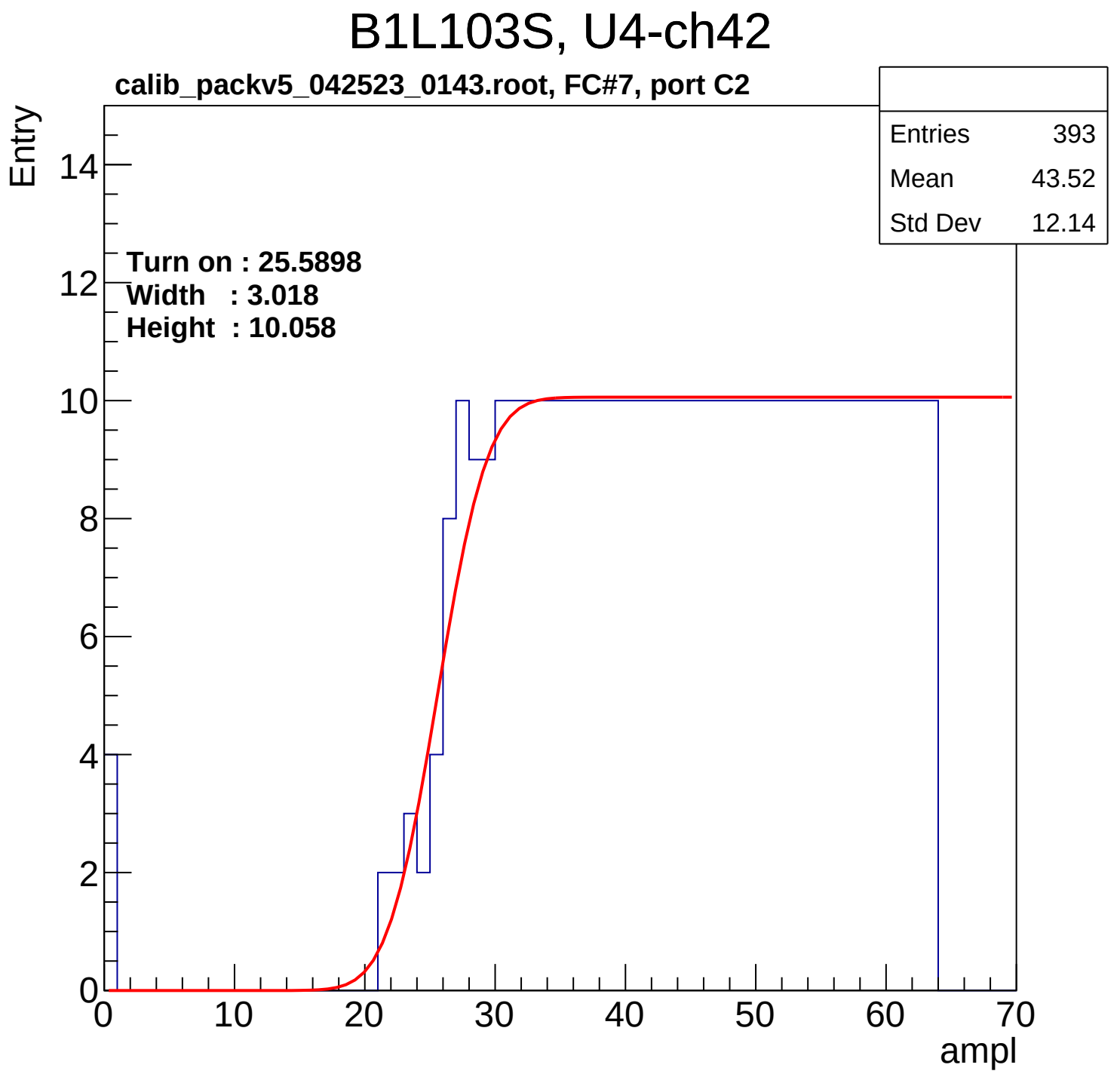
B1L103S, U4-ch42
calib_packv5_042523_0143.root, FC#7, port C2
Entries 393
Mean 43.52
Std Dev 12.14
Turn on : 25.5898
Width : 3.018
Height : 10.058
Entry
ampl
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6
8
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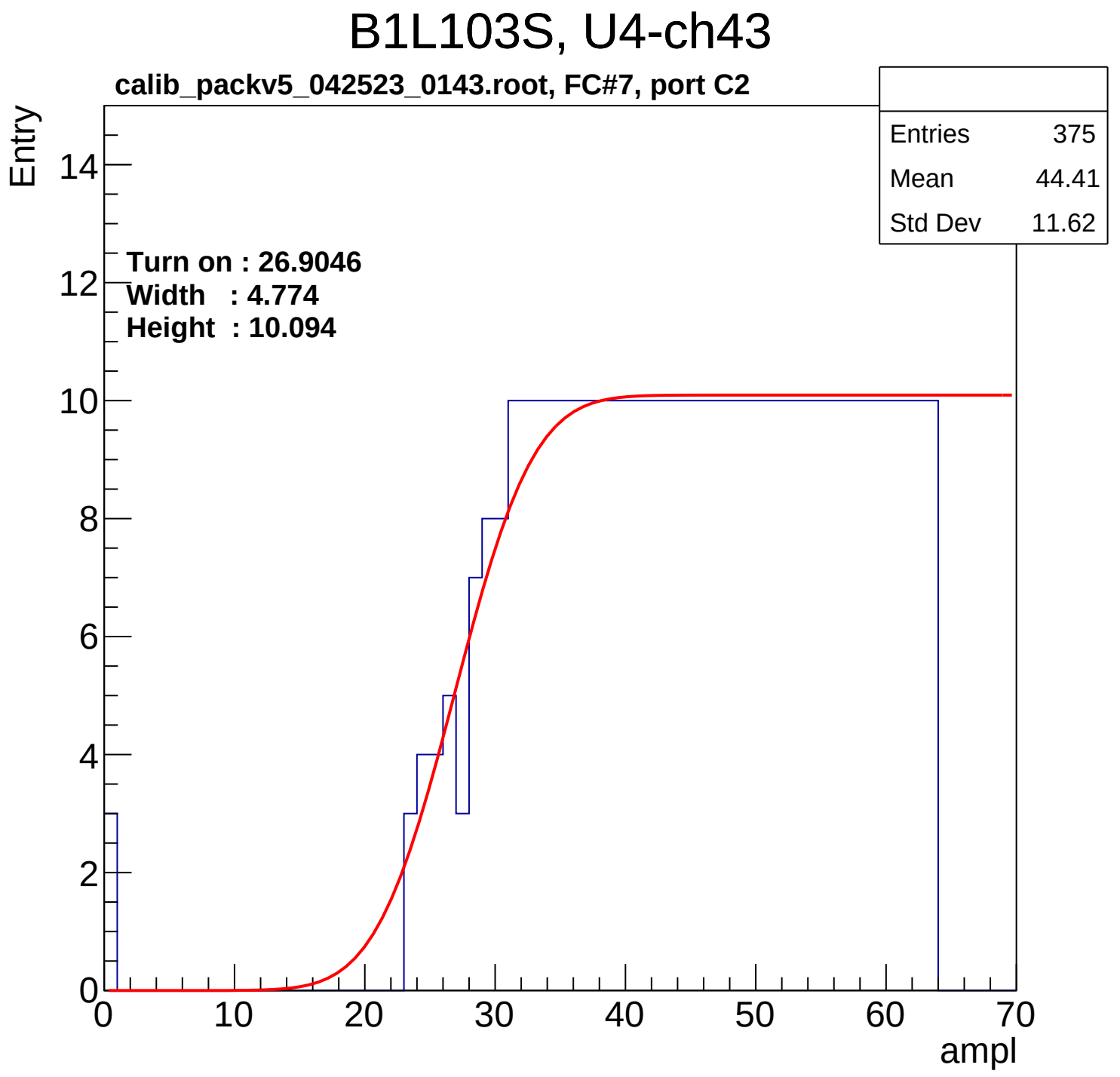
B1L103S, U4-ch43
calib_packv5_042523_0143.root, FC#7, port C2
Entries 375
Mean 44.41
Std Dev 11.62
Turn on : 26.9046
Width : 4.774
Height : 10.094
Entry
ampl
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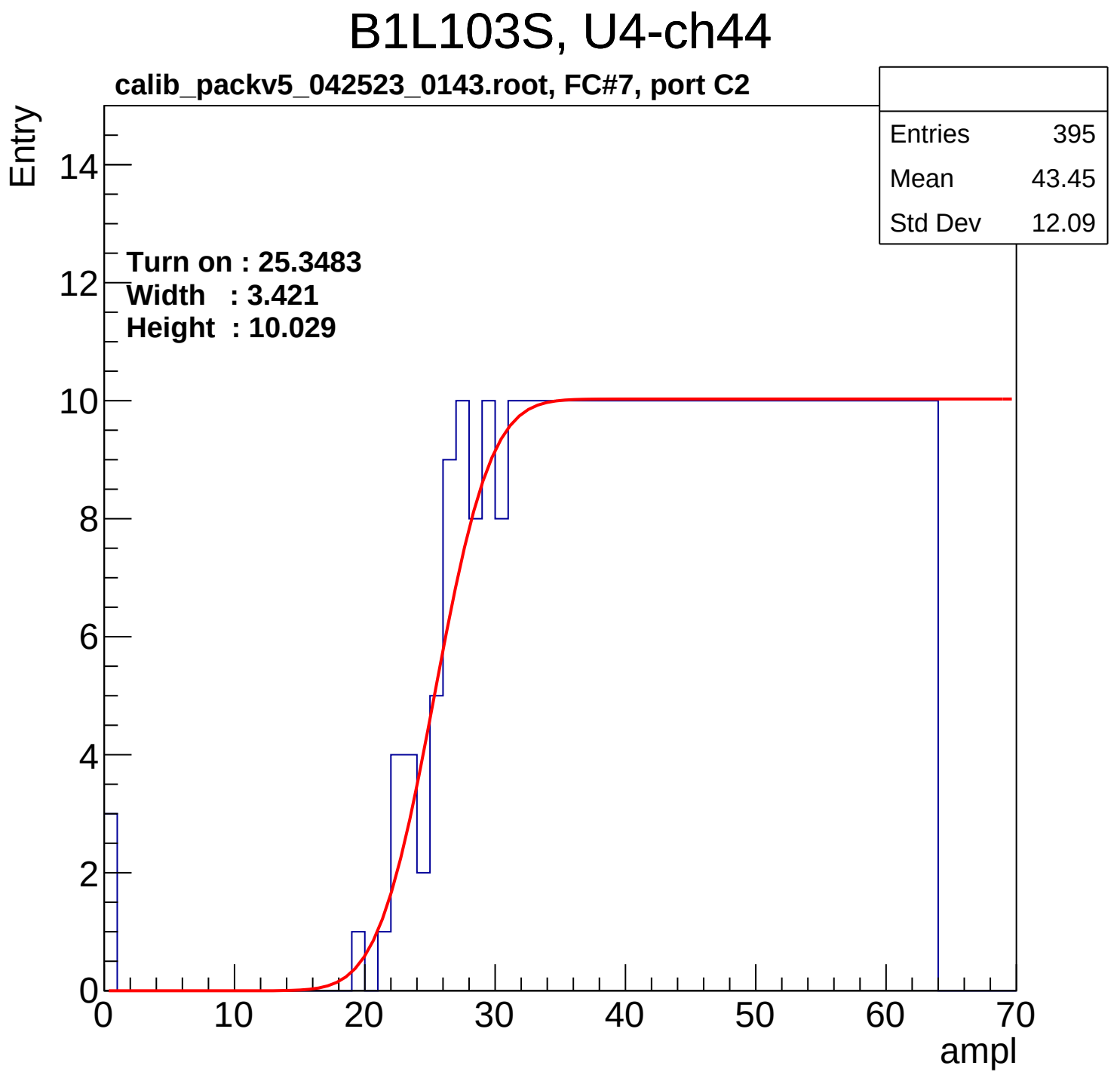
B1L103S, U4-ch44
calib_packv5_042523_0143.root, FC#7, port C2
Entries 395
Mean 43.45
Std Dev 12.09
Turn on : 25.3483
Width : 3.421
Height : 10.029
Entry
ampl
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8
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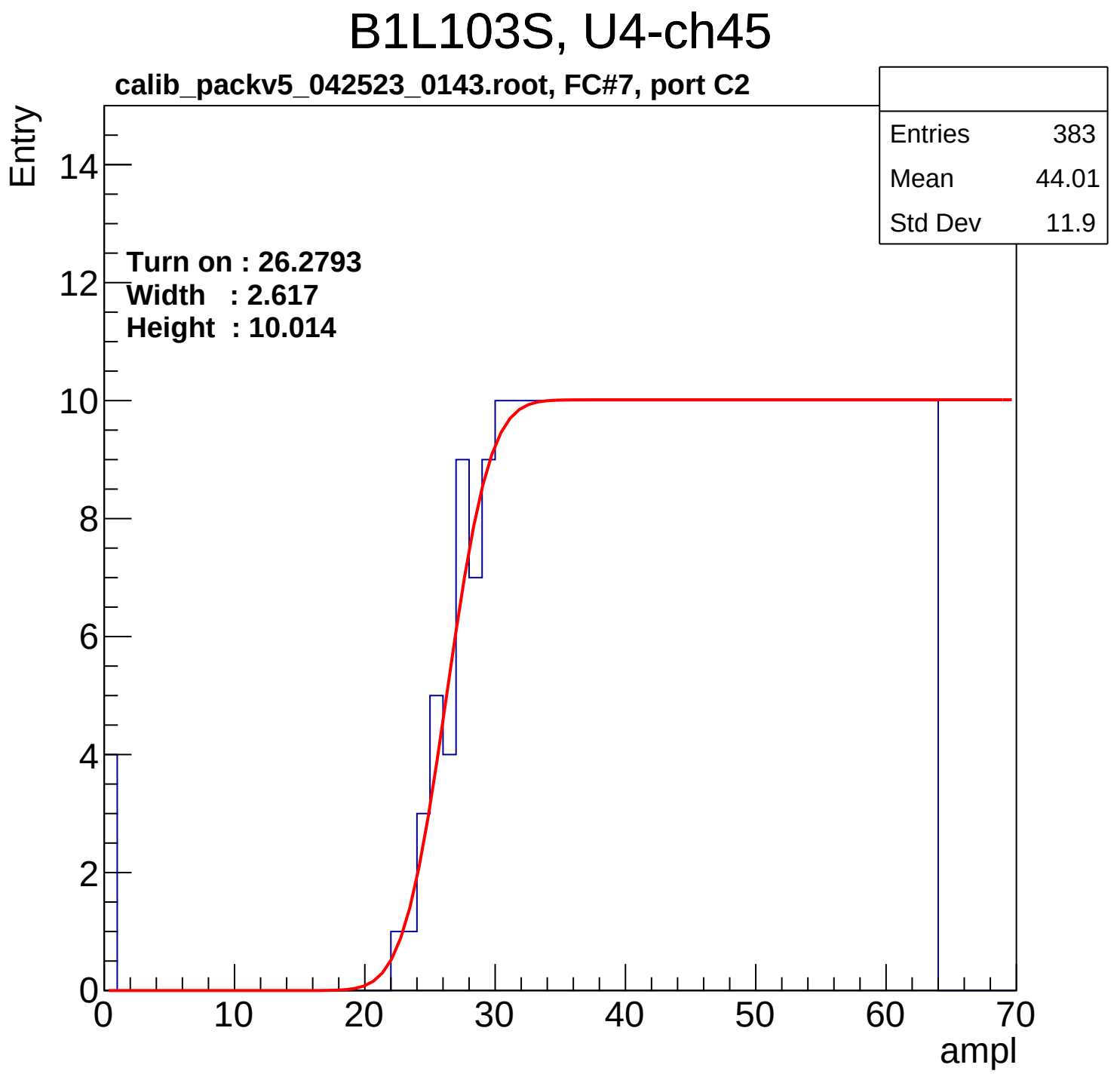
B1L103S, U4-ch45
calib_packv5_042523_0143.root, FC#7, port C2
Entries 383
Mean 44.01
Std Dev 11.9
Turn on : 26.2793
Width : 2.617
Height : 10.014
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ampl
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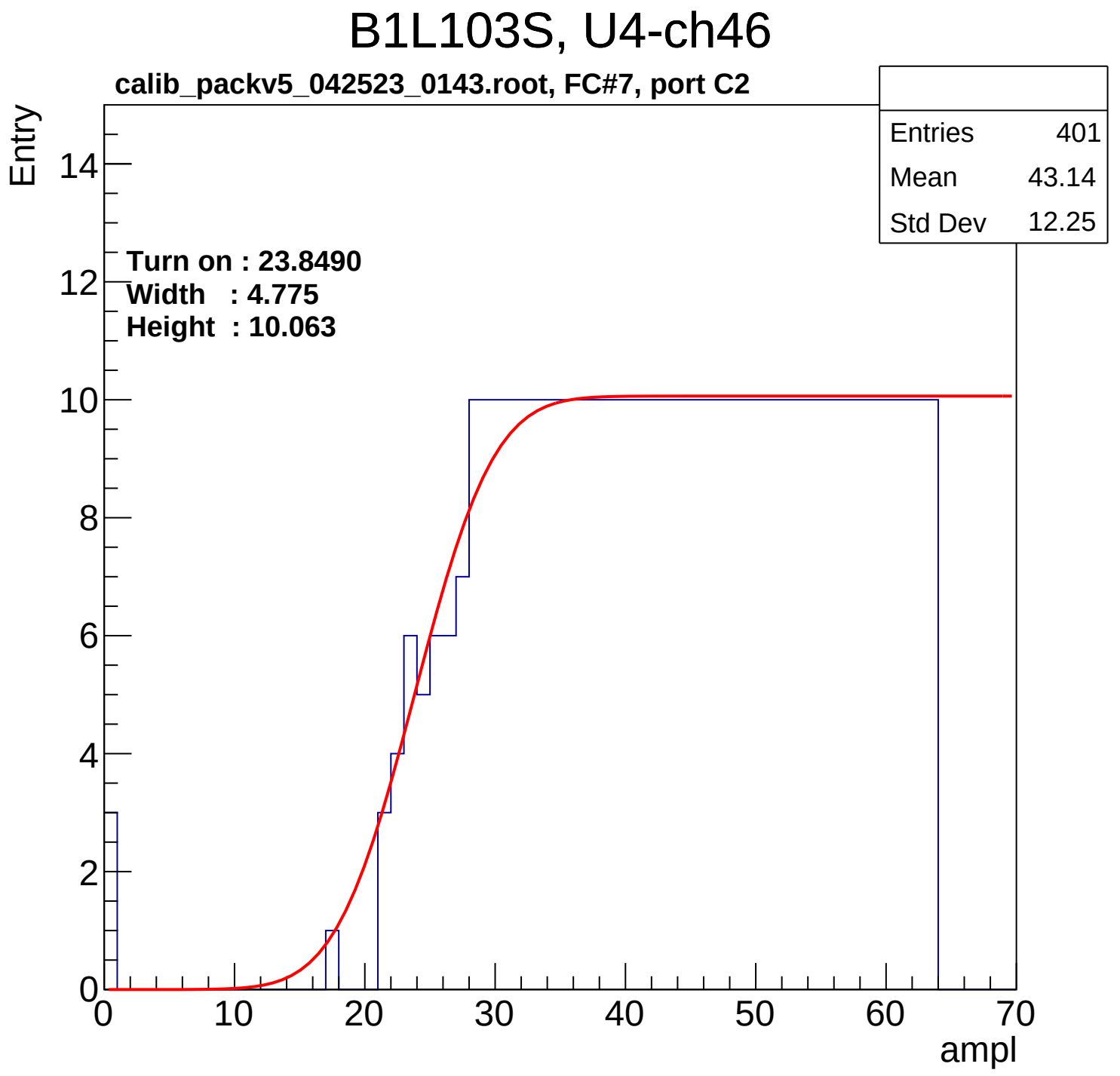
B1L103S, U4-ch46
calib_packv5_042523_0143.root, FC#7, port C2
Entries 401
Mean 43.14
Std Dev 12.25
Turn on : 23.8490
Width : 4.775
Height : 10.063
Entry
ampl
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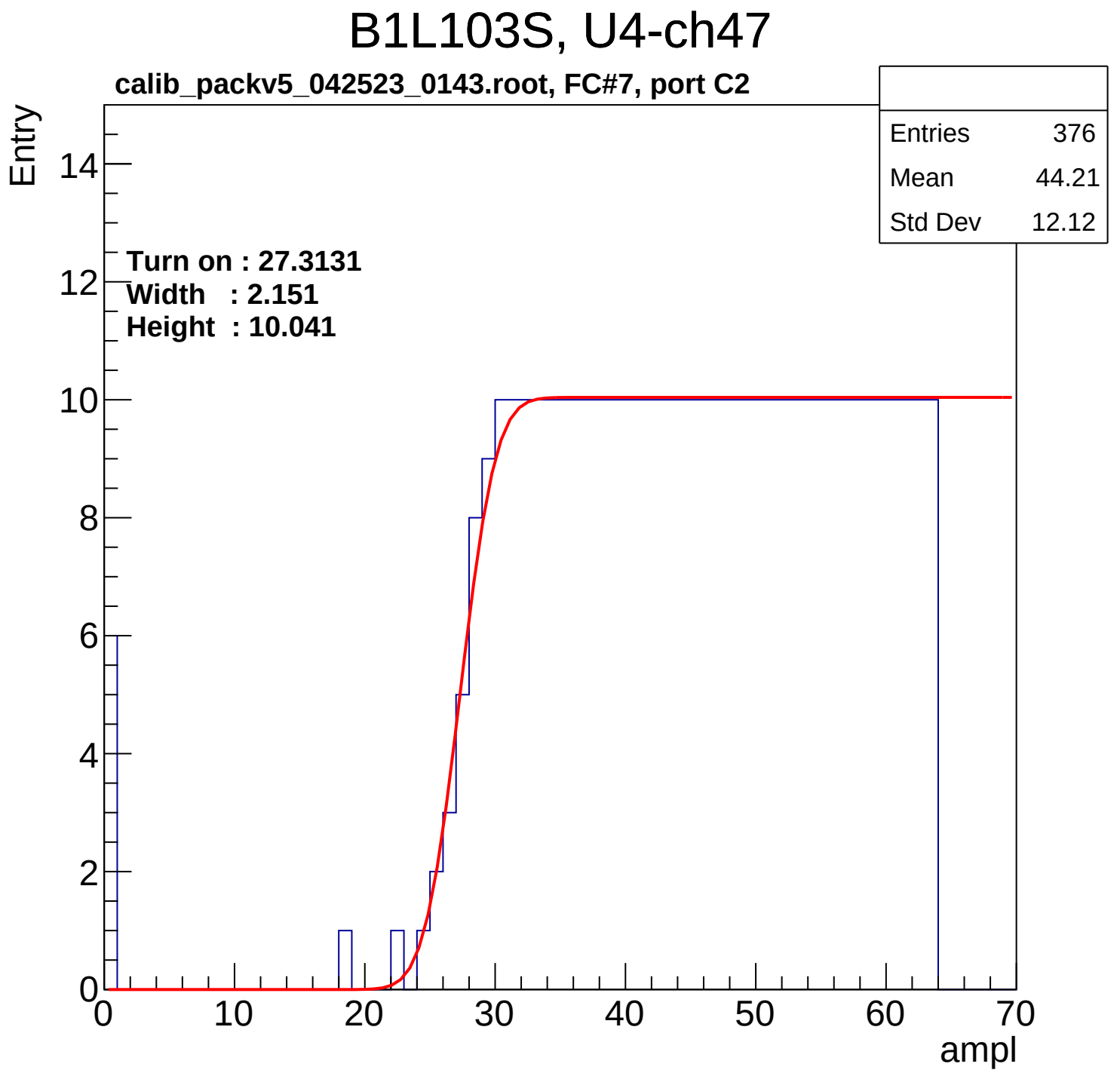
B1L103S, U4-ch47
calib_packv5_042523_0143.root, FC#7, port C2
Entries 376
Mean 44.21
Std Dev 12.12
Turn on : 27.3131
Width : 2.151
Height : 10.041
Entry
ampl
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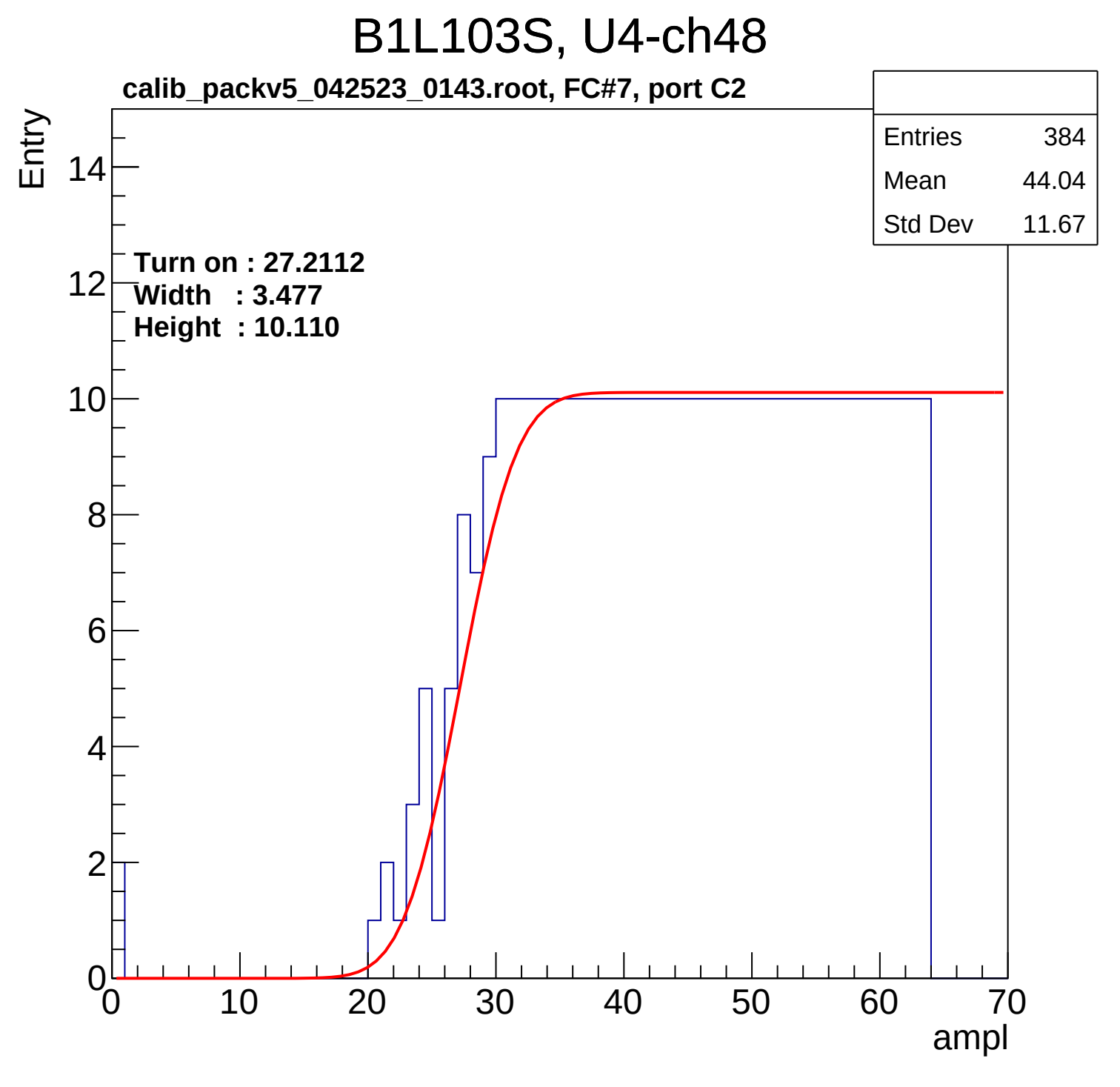
B1L103S, U4-ch48
calib_packv5_042523_0143.root, FC#7, port C2
Entries 384
Mean 44.04
Std Dev 11.67
Turn on : 27.2112
Width : 3.477
Height : 10.110
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ampl
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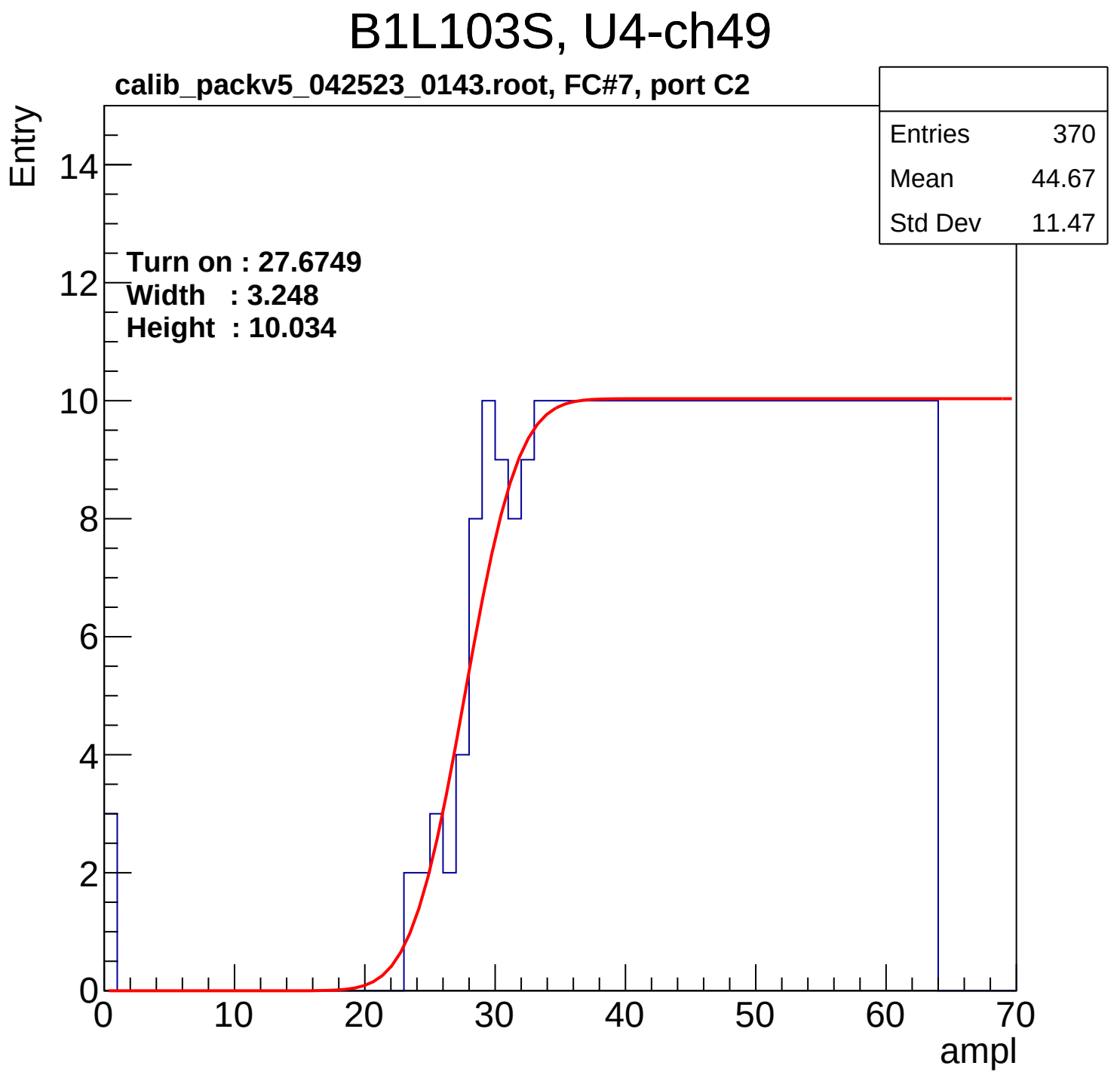
B1L103S, U4-ch49
calib_packv5_042523_0143.root, FC#7, port C2
Entries 370
Mean 44.67
Std Dev 11.47
Turn on : 27.6749
Width : 3.248
Height : 10.034
Entry
ampl
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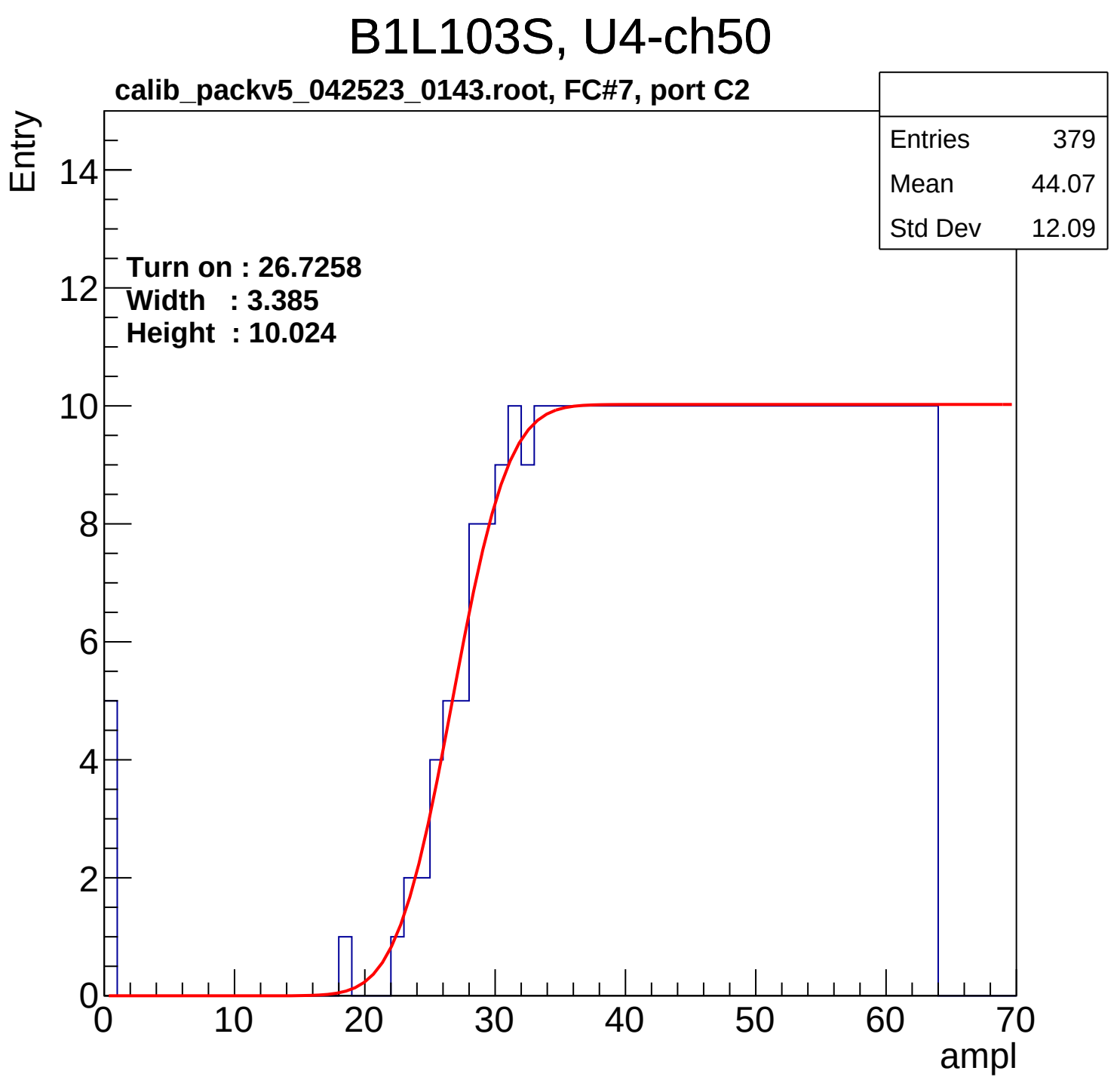
B1L103S, U4-ch50
calib_packv5_042523_0143.root, FC#7, port C2
Entries 379
Mean 44.07
Std Dev 12.09
Turn on : 26.7258
Width : 3.385
Height : 10.024
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ampl
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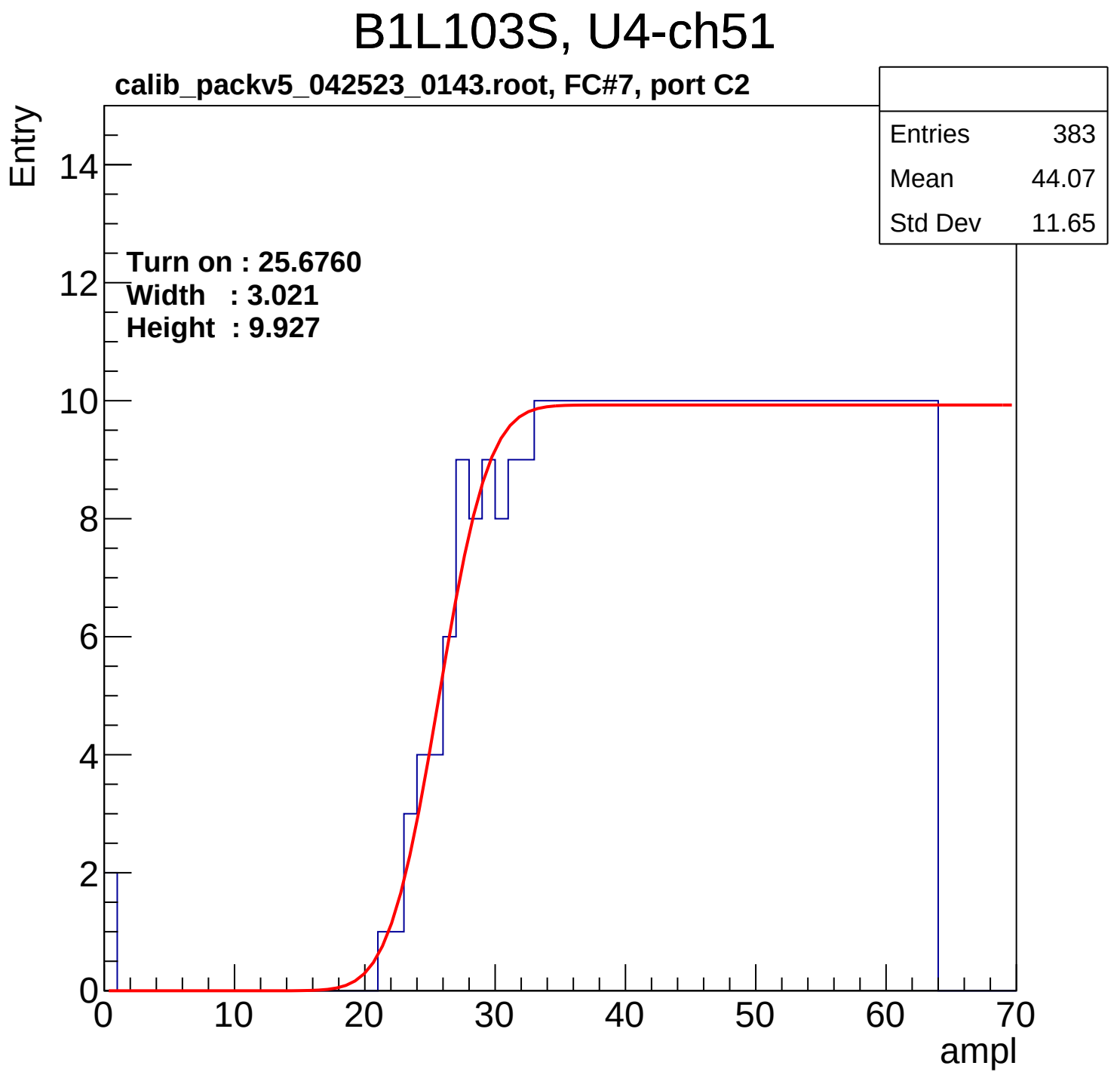
B1L103S, U4-ch51
calib_packv5_042523_0143.root, FC#7, port C2
Entries 383
Mean 44.07
Std Dev 11.65
Turn on : 25.6760
Width : 3.021
Height : 9.927
Entry
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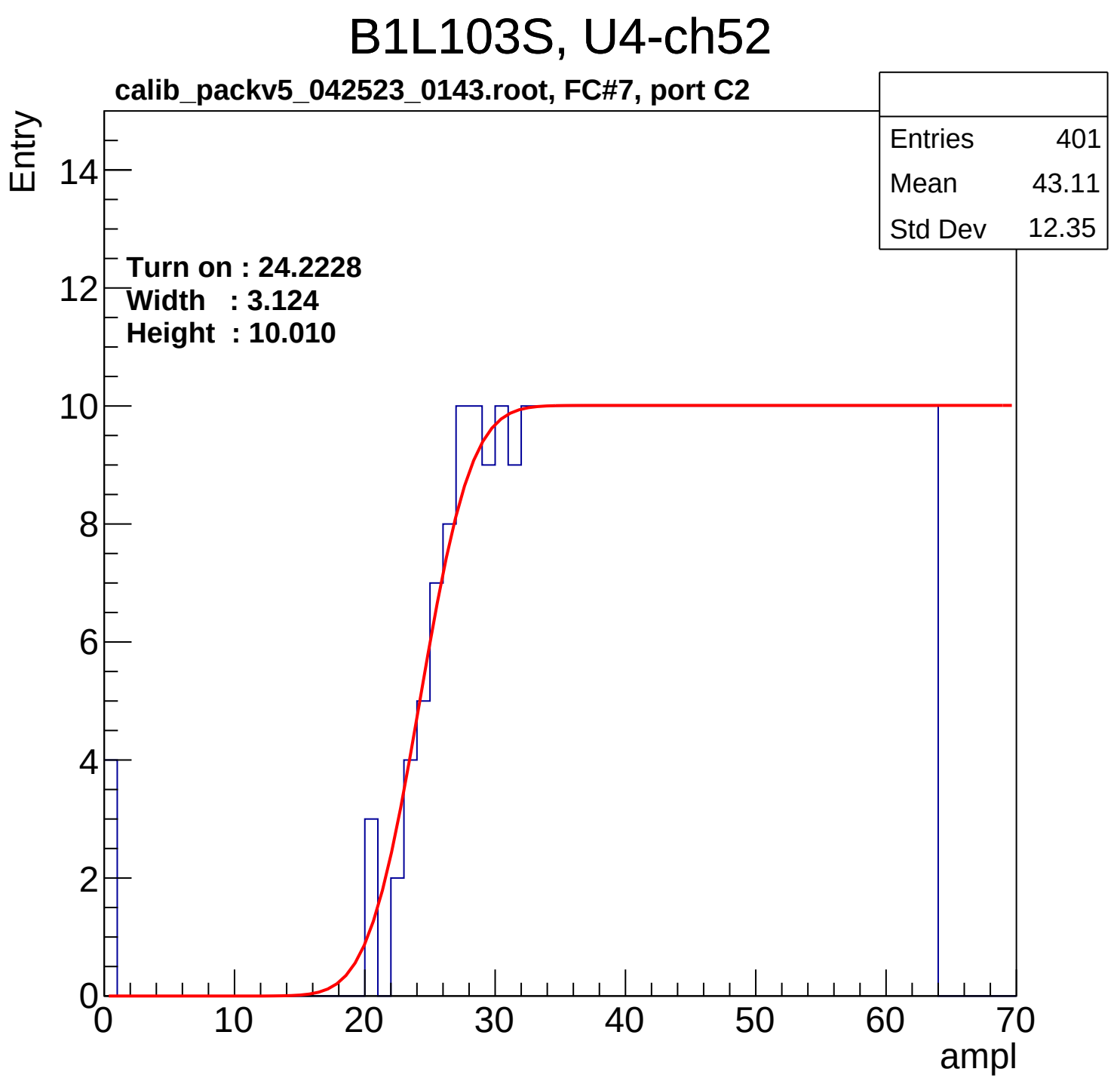
B1L103S, U4-ch52
calib_packv5_042523_0143.root, FC#7, port C2
Entries 401
Mean 43.11
Std Dev 12.35
Turn on : 24.2228
Width : 3.124
Height : 10.010
Entry
ampl
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6
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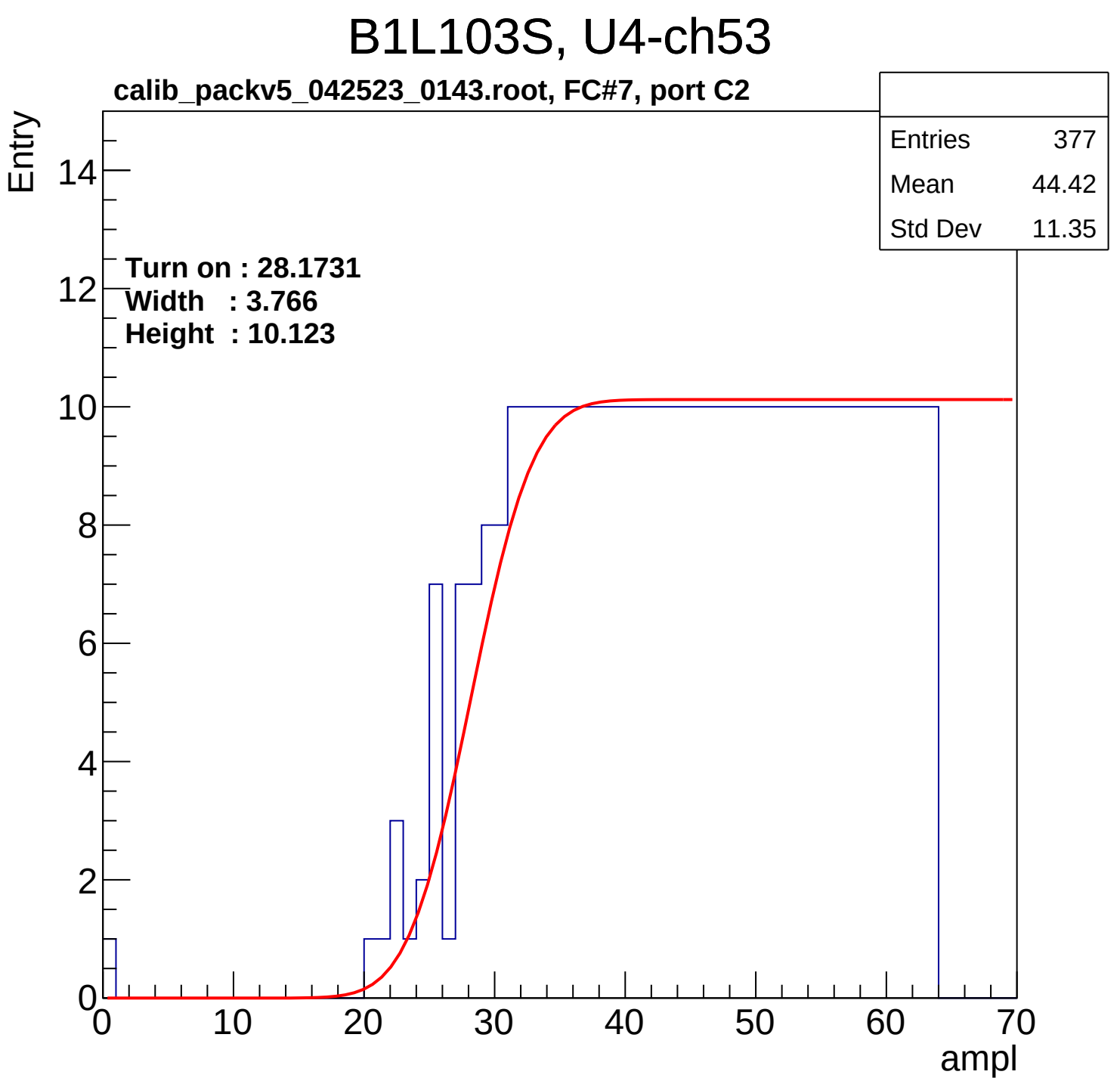
B1L103S, U4-ch53
calib_packv5_042523_0143.root, FC#7, port C2
Entries 377
Mean 44.42
Std Dev 11.35
Turn on : 28.1731
Width : 3.766
Height : 10.123
Entry
ampl
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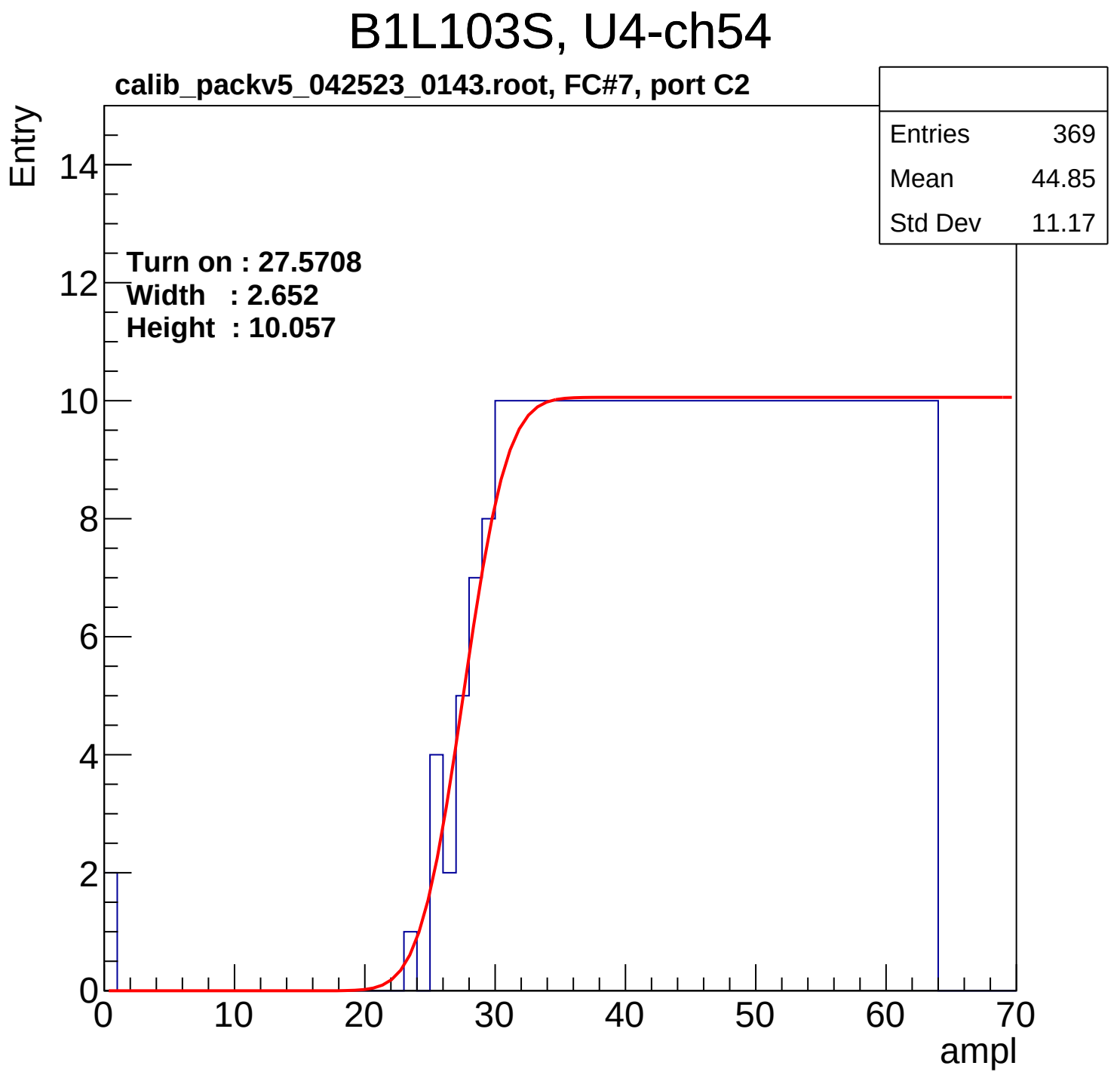
B1L103S, U4-ch54
calib_packv5_042523_0143.root, FC#7, port C2
Entries 369
Mean 44.85
Std Dev 11.17
Turn on : 27.5708
Width : 2.652
Height : 10.057
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ampl
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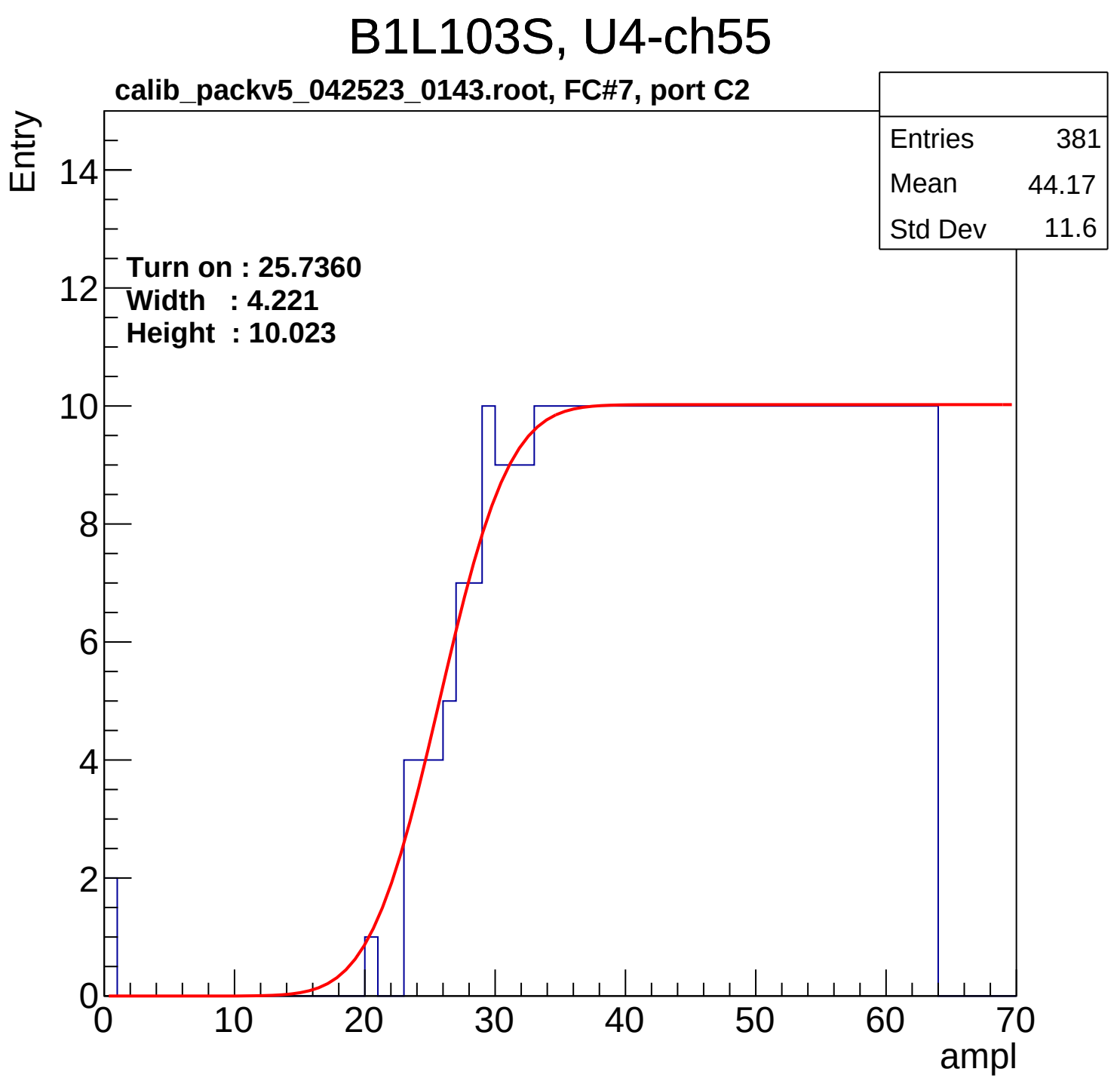
B1L103S, U4-ch55
calib_packv5_042523_0143.root, FC#7, port C2
Entries 381
Mean 44.17
Std Dev 11.6
Turn on : 25.7360
Width : 4.221
Height : 10.023
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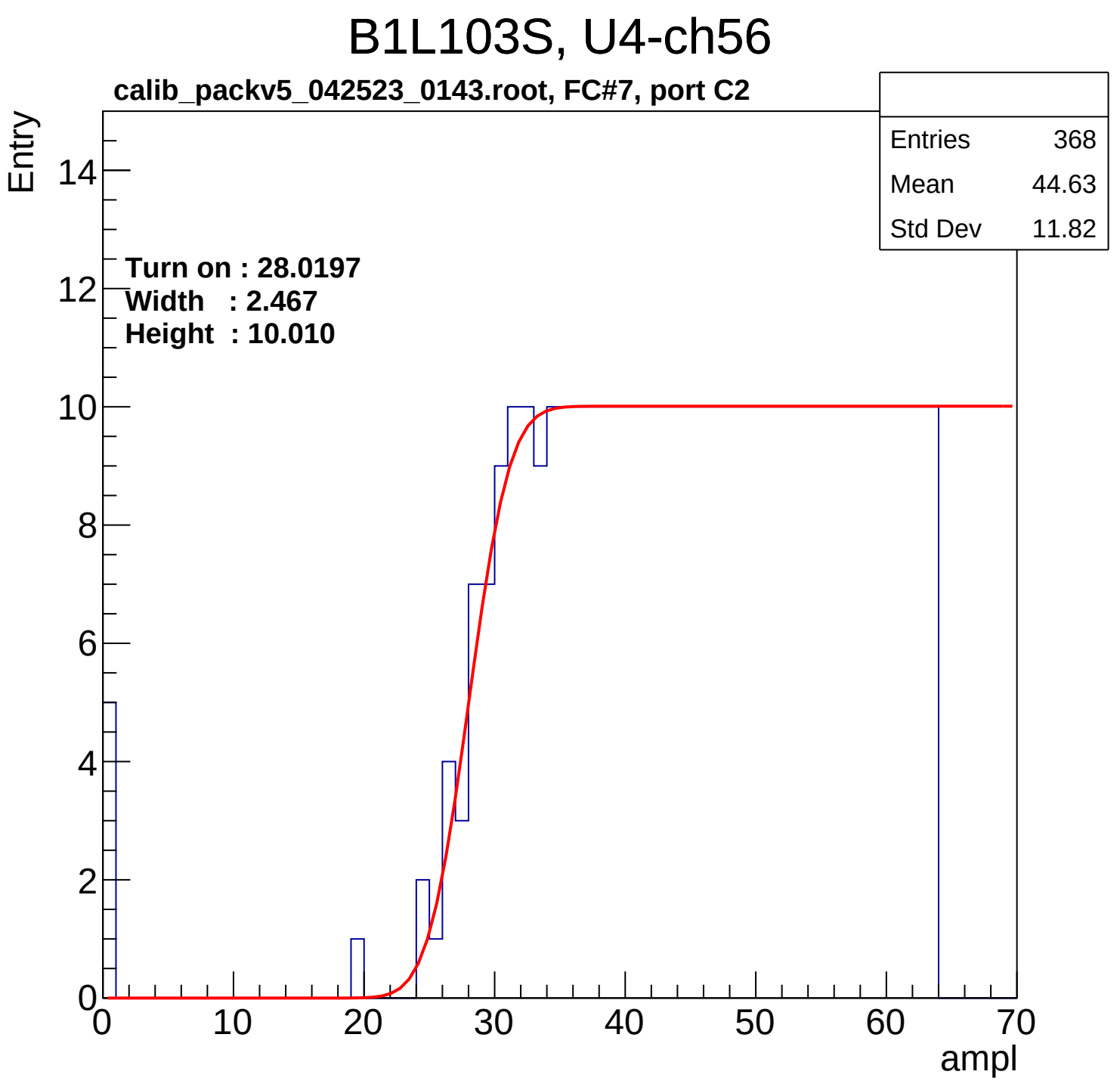
B1L103S, U4-ch56
calib_packv5_042523_0143.root, FC#7, port C2
Entries 368
Mean 44.63
Std Dev 11.82
Turn on : 28.0197
Width : 2.467
Height : 10.010
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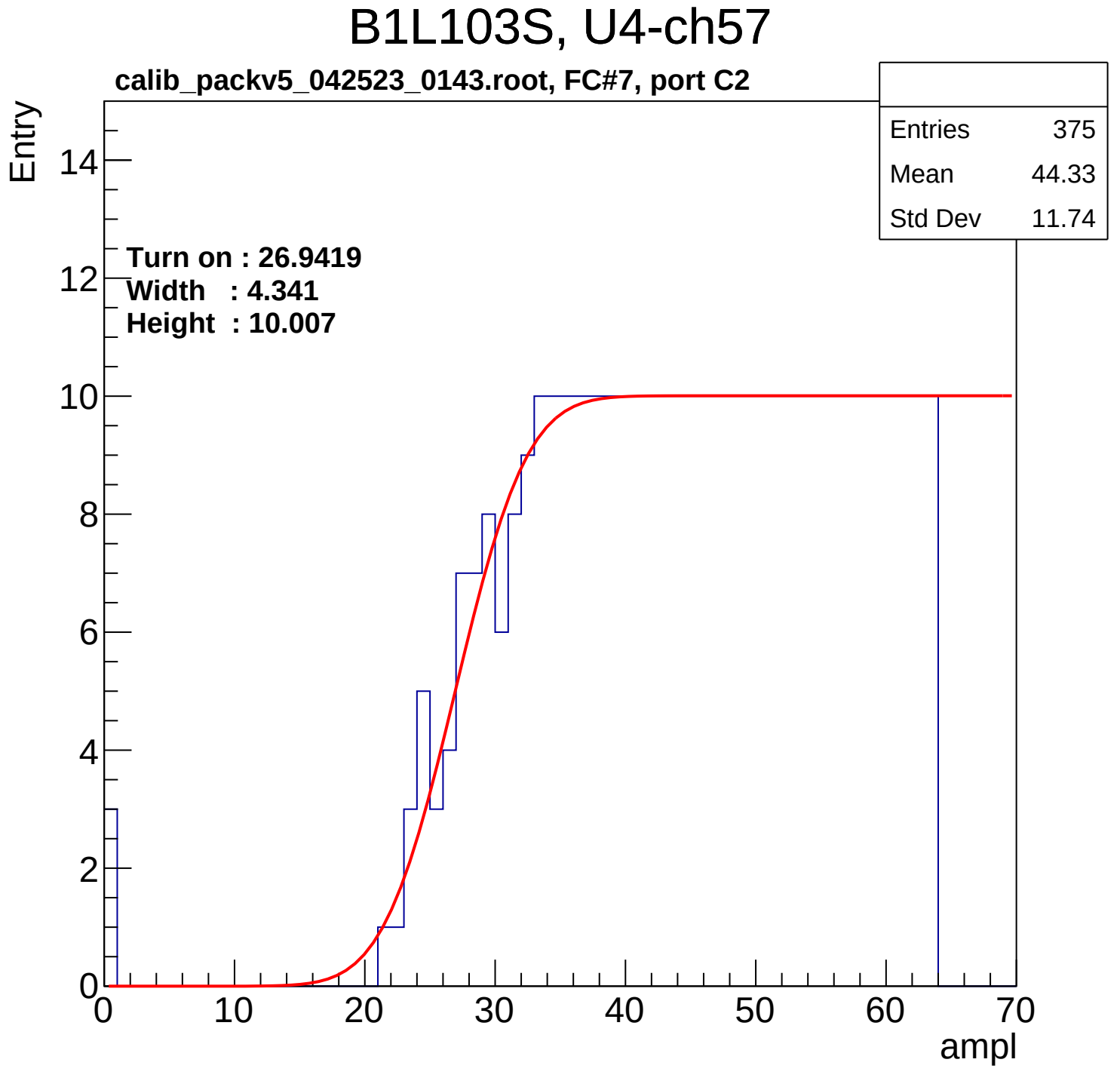
B1L103S, U4-ch57
calib_packv5_042523_0143.root, FC#7, port C2
Entries 375
Mean 44.33
Std Dev 11.74
Turn on : 26.9419
Width : 4.341
Height : 10.007
Entry
ampl
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4
6
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20
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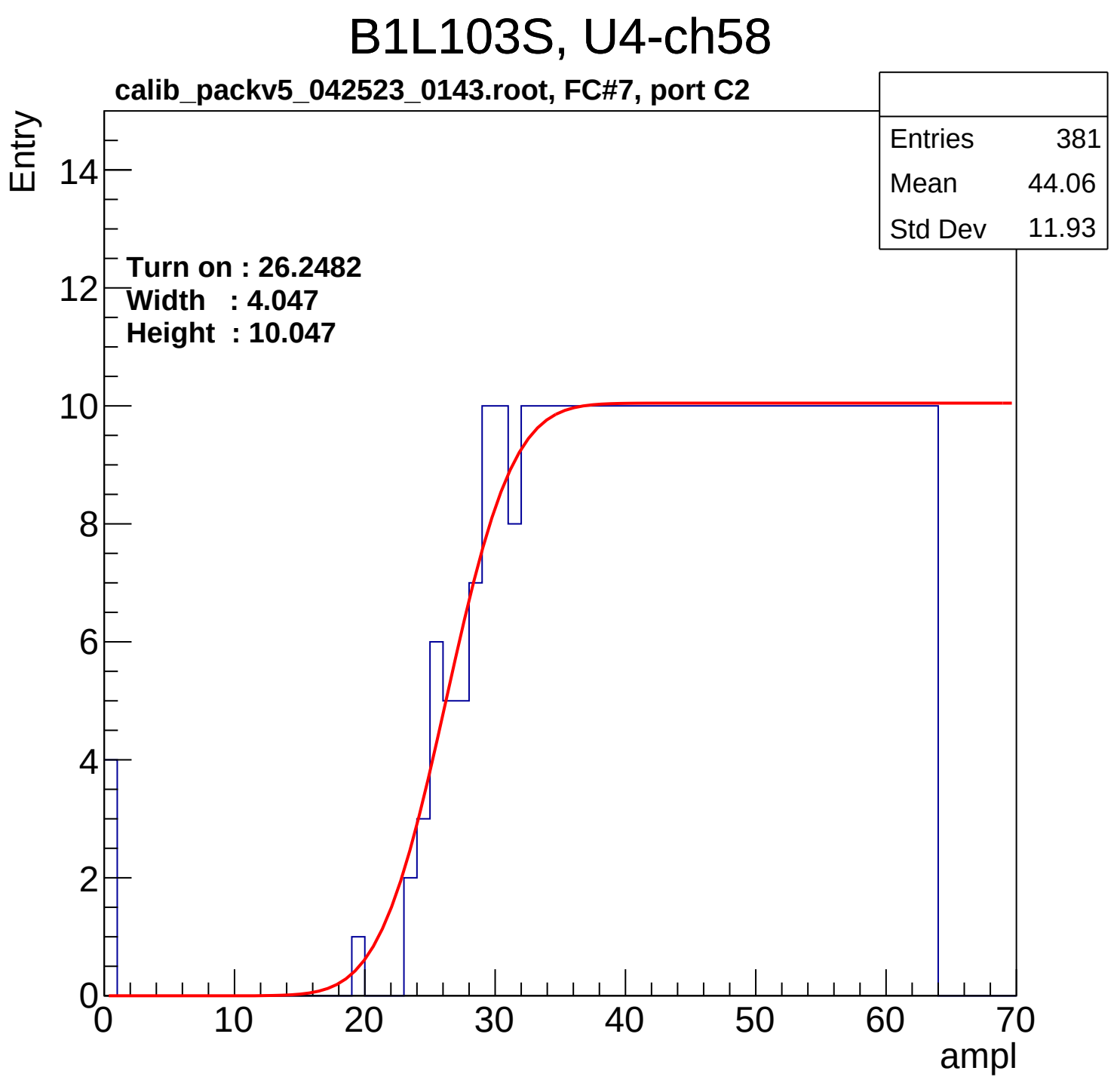
B1L103S, U4-ch58
calib_packv5_042523_0143.root, FC#7, port C2
Entries 381
Mean 44.06
Std Dev 11.93
Turn on : 26.2482
Width : 4.047
Height : 10.047
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ampl
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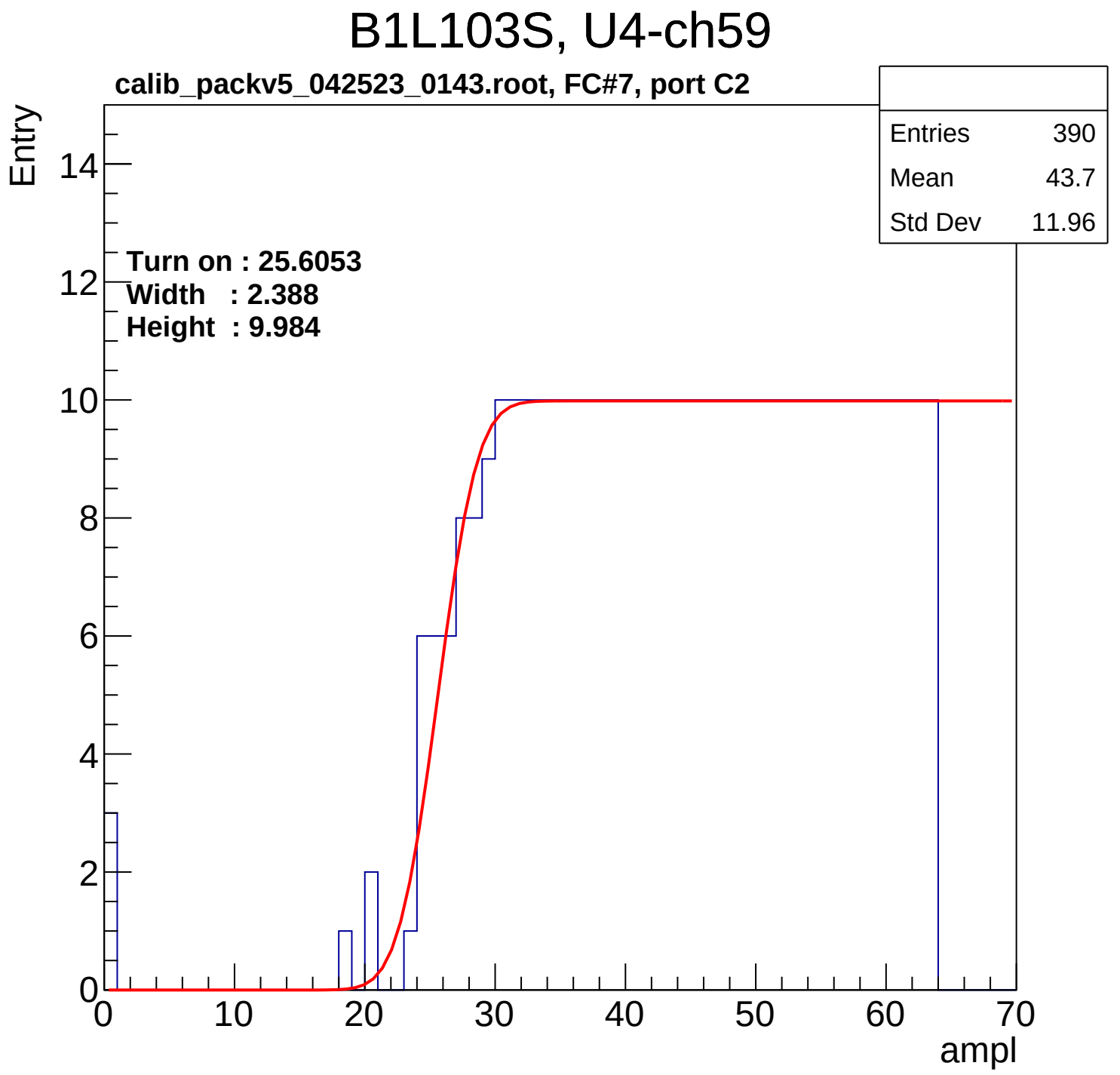
B1L103S, U4-ch59
calib_packv5_042523_0143.root, FC#7, port C2
Entries 390
Mean 43.7
Std Dev 11.96
Turn on : 25.6053
Width : 2.388
Height : 9.984
Entry
ampl
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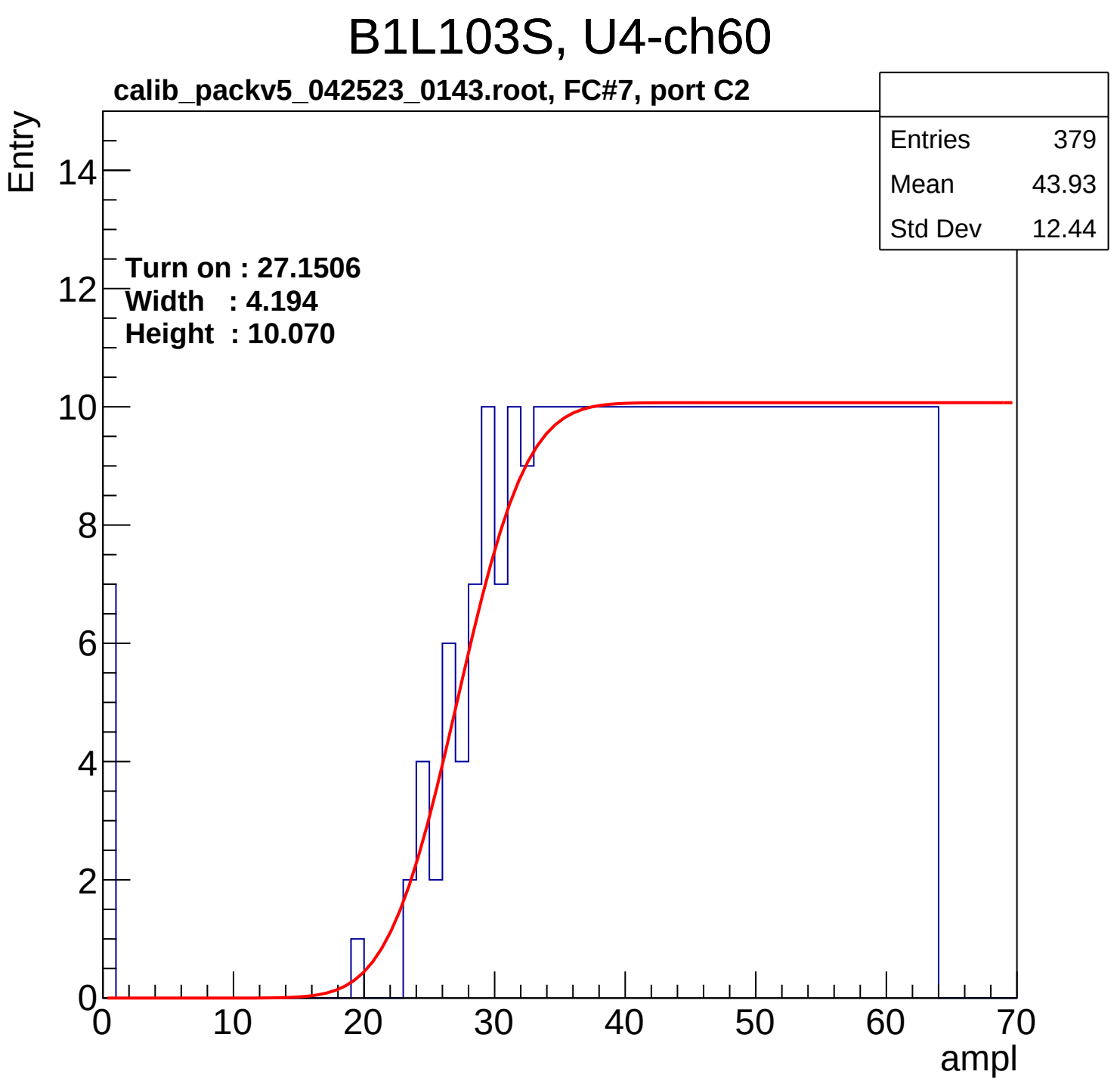
B1L103S, U4-ch60
calib_packv5_042523_0143.root, FC#7, port C2
Entries 379
Mean 43.93
Std Dev 12.44
Turn on : 27.1506
Width : 4.194
Height : 10.070
Entry
ampl
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2
4
6
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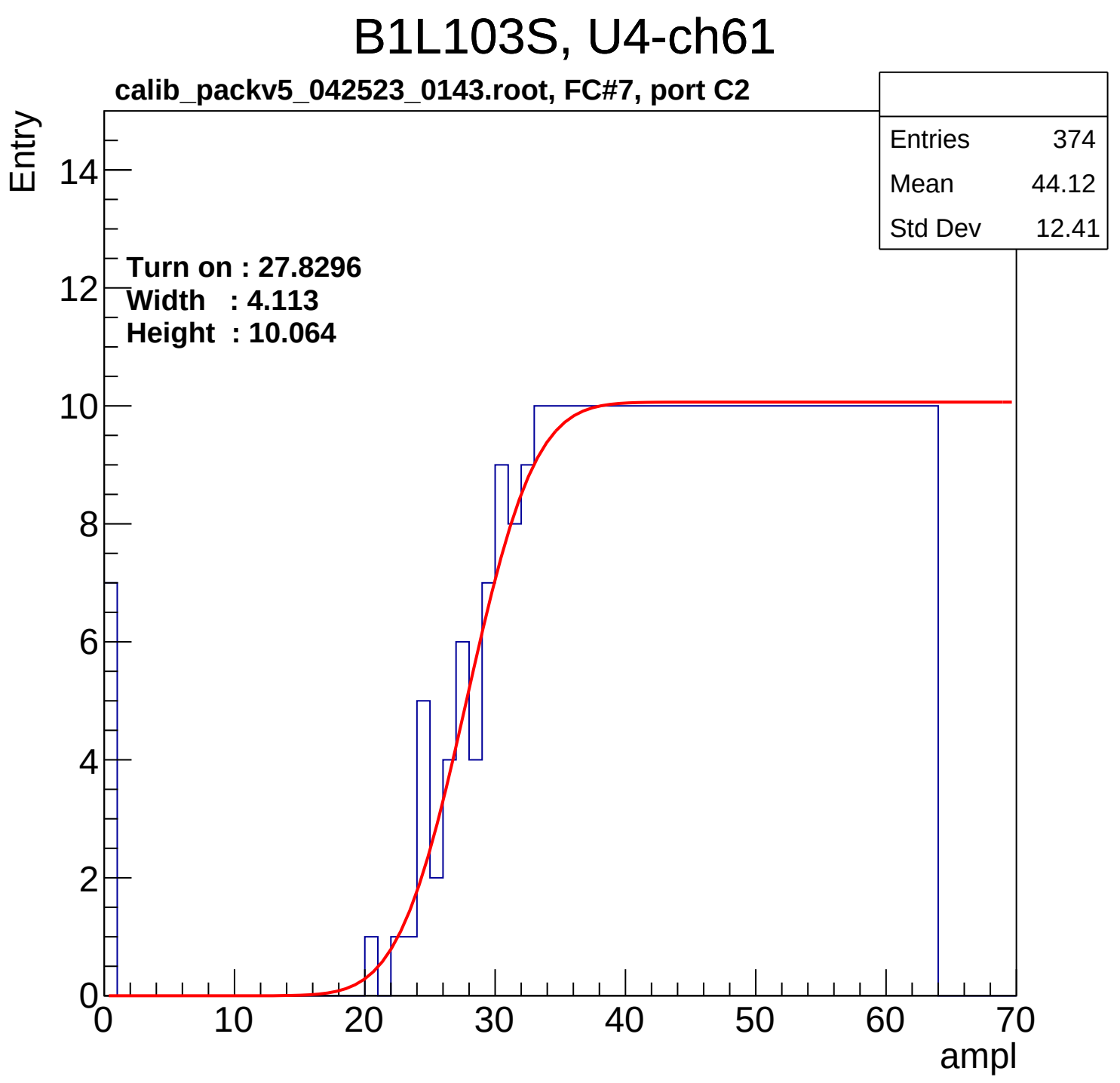
B1L103S, U4-ch61
calib_packv5_042523_0143.root, FC#7, port C2
Entries 374
Mean 44.12
Std Dev 12.41
Turn on : 27.8296
Width : 4.113
Height : 10.064
Entry
ampl
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4
6
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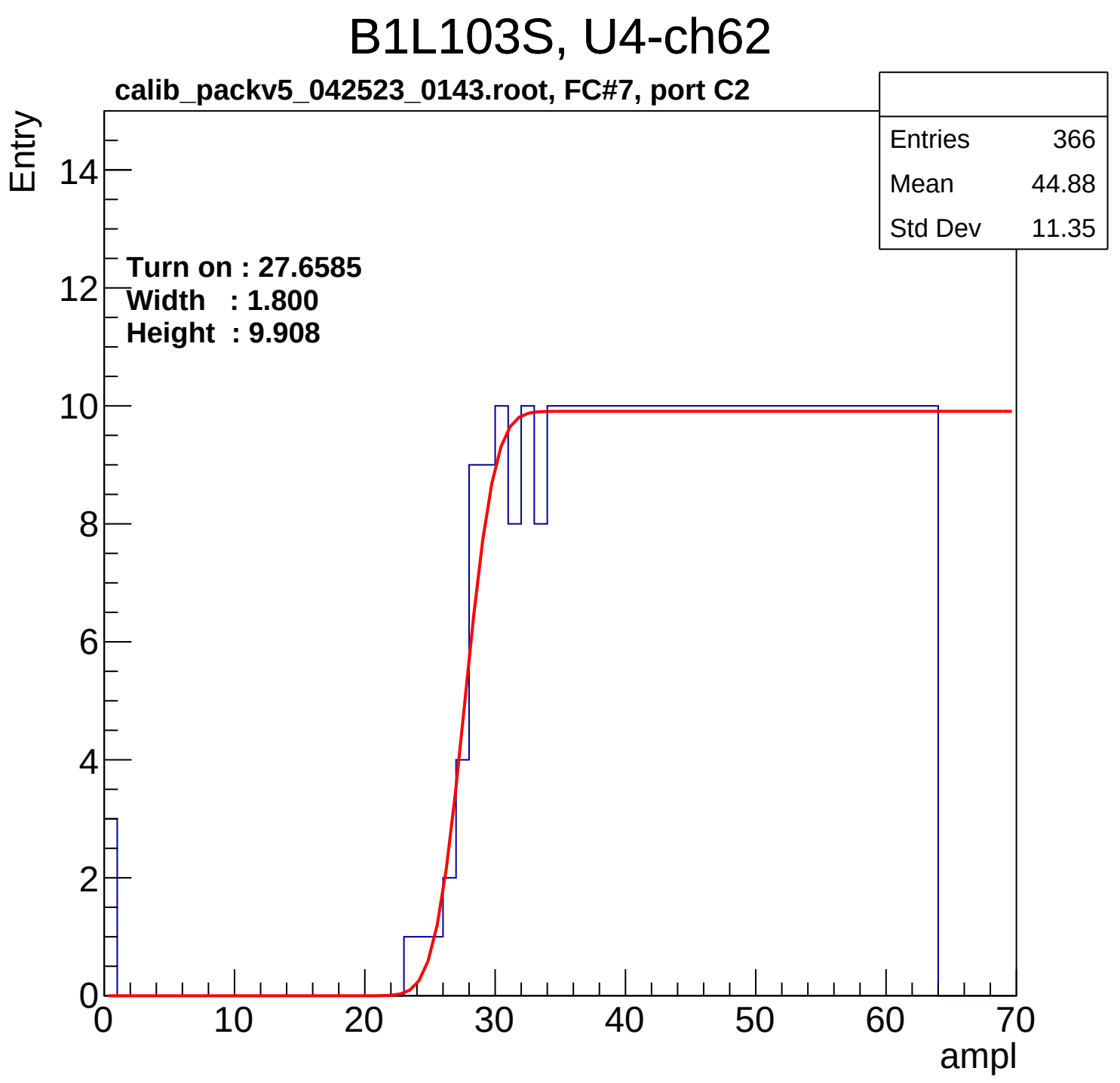
B1L103S, U4-ch62
calib_packv5_042523_0143.root, FC#7, port C2
Entries 366
Mean 44.88
Std Dev 11.35
Turn on : 27.6585
Width : 1.800
Height : 9.908
Entry
ampl
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2
4
6
8
10
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0
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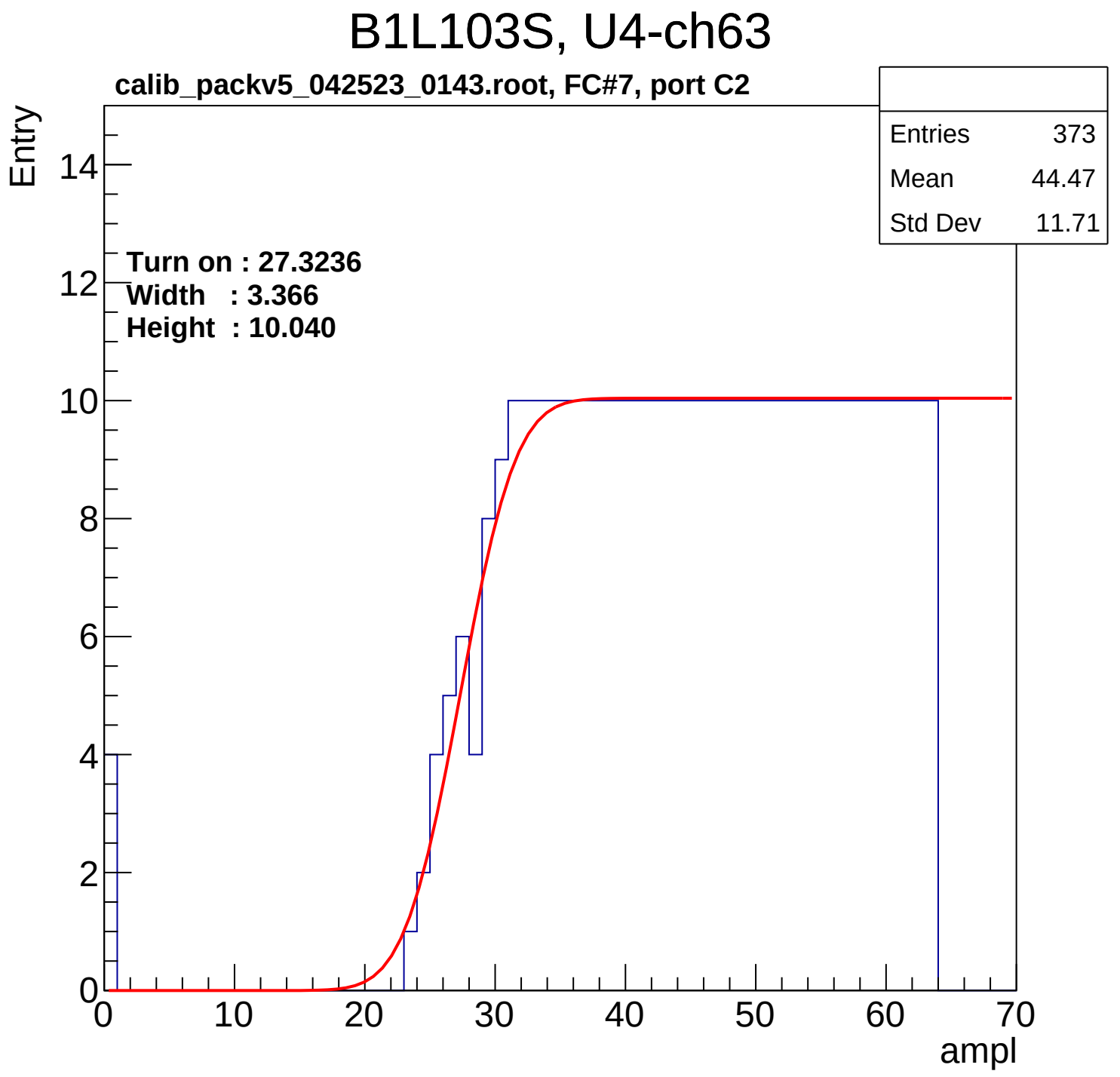
B1L103S, U4-ch63
calib_packv5_042523_0143.root, FC#7, port C2
Entries 373
Mean 44.47
Std Dev 11.71
Turn on : 27.3236
Width : 3.366
Height : 10.040
Entry
ampl
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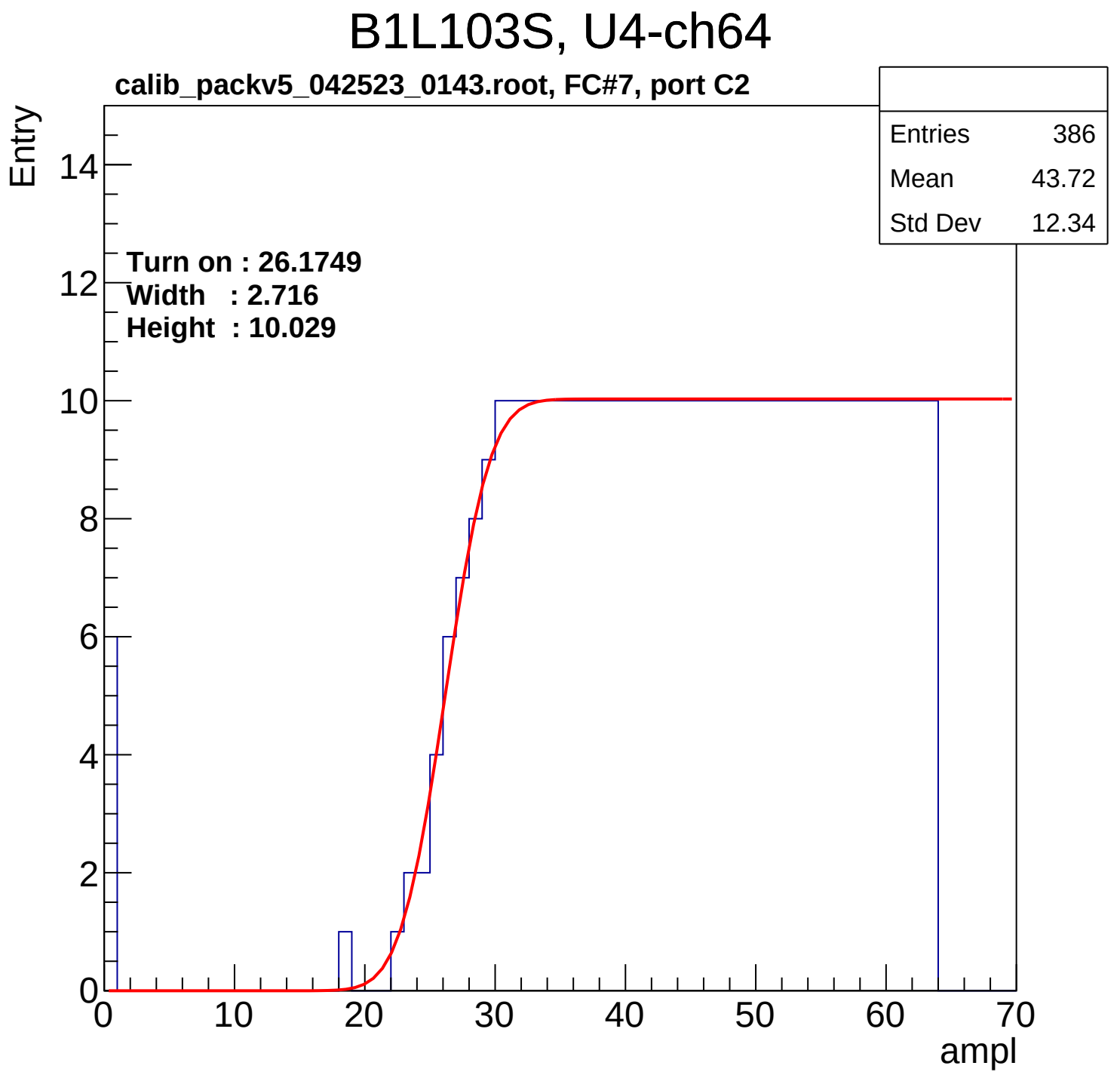
B1L103S, U4-ch64
calib_packv5_042523_0143.root, FC#7, port C2
Entries 386
Mean 43.72
Std Dev 12.34
Turn on : 26.1749
Width : 2.716
Height : 10.029
Entry
ampl
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6
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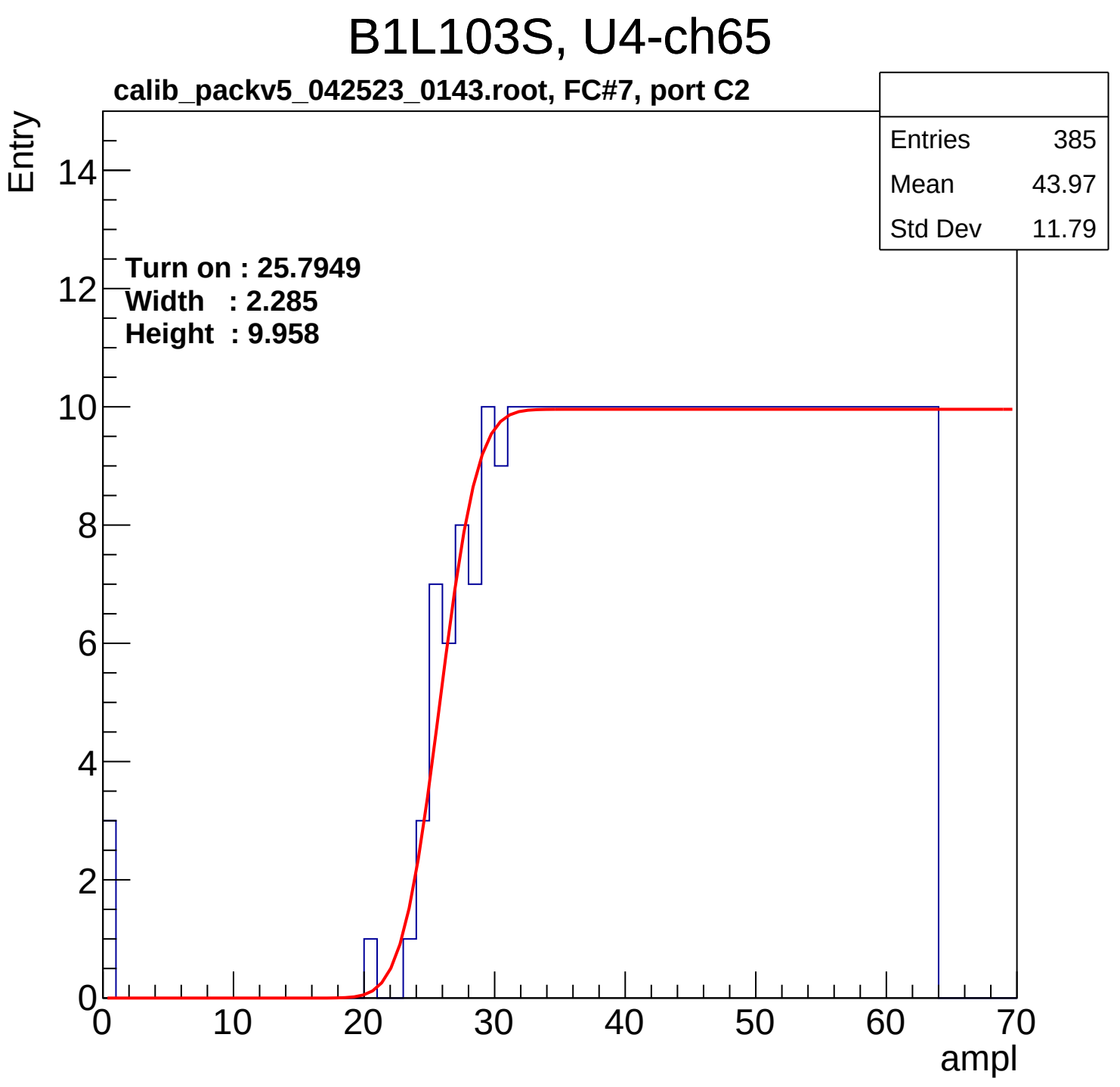
B1L103S, U4-ch65
calib_packv5_042523_0143.root, FC#7, port C2
Entries 385
Mean 43.97
Std Dev 11.79
Turn on : 25.7949
Width : 2.285
Height : 9.958
Entry
ampl
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2
4
6
8
10
12
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0
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60
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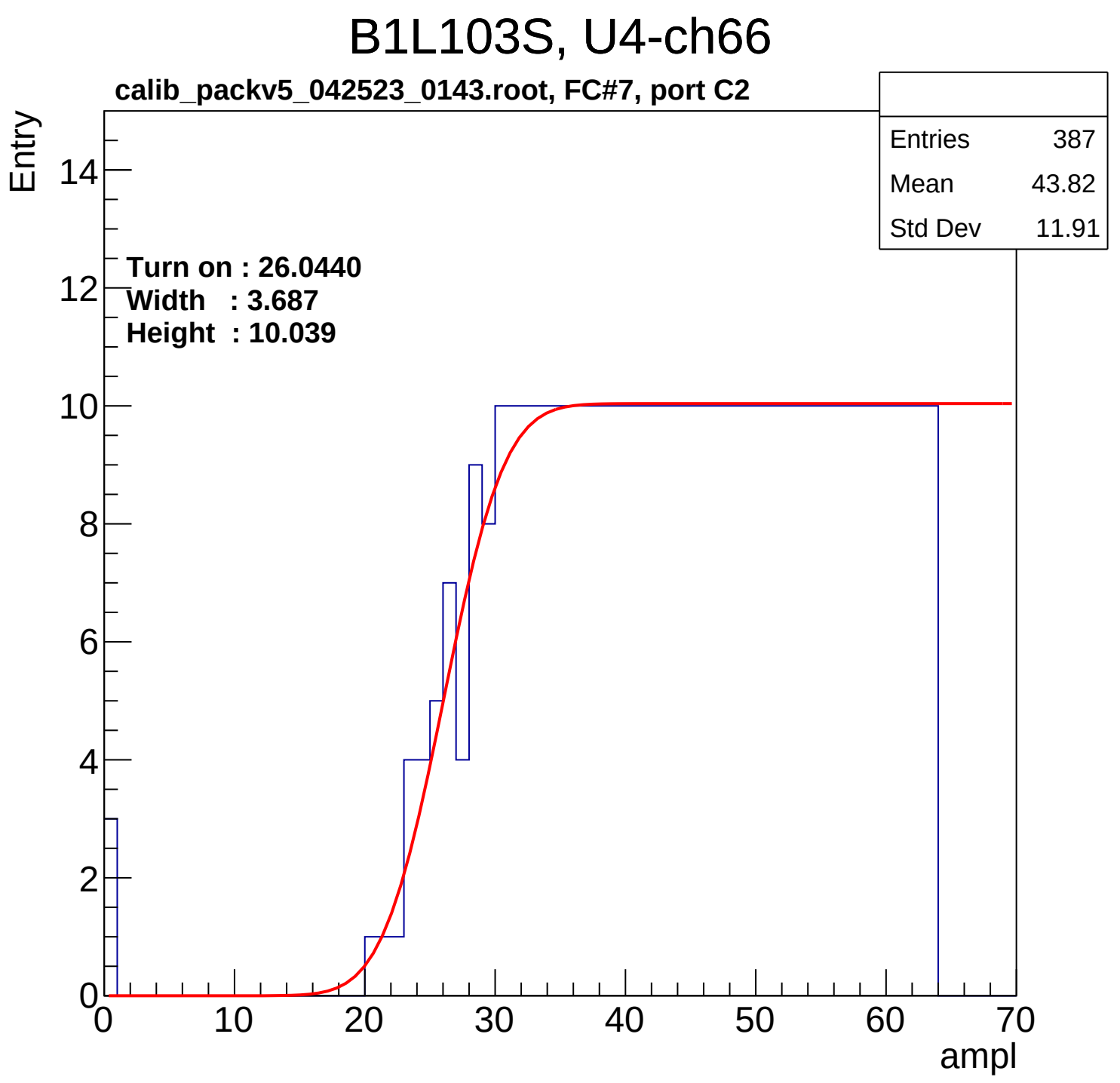
B1L103S, U4-ch66
calib_packv5_042523_0143.root, FC#7, port C2
Entries 387
Mean 43.82
Std Dev 11.91
Turn on : 26.0440
Width : 3.687
Height : 10.039
Entry
ampl
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4
6
8
10
12
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0
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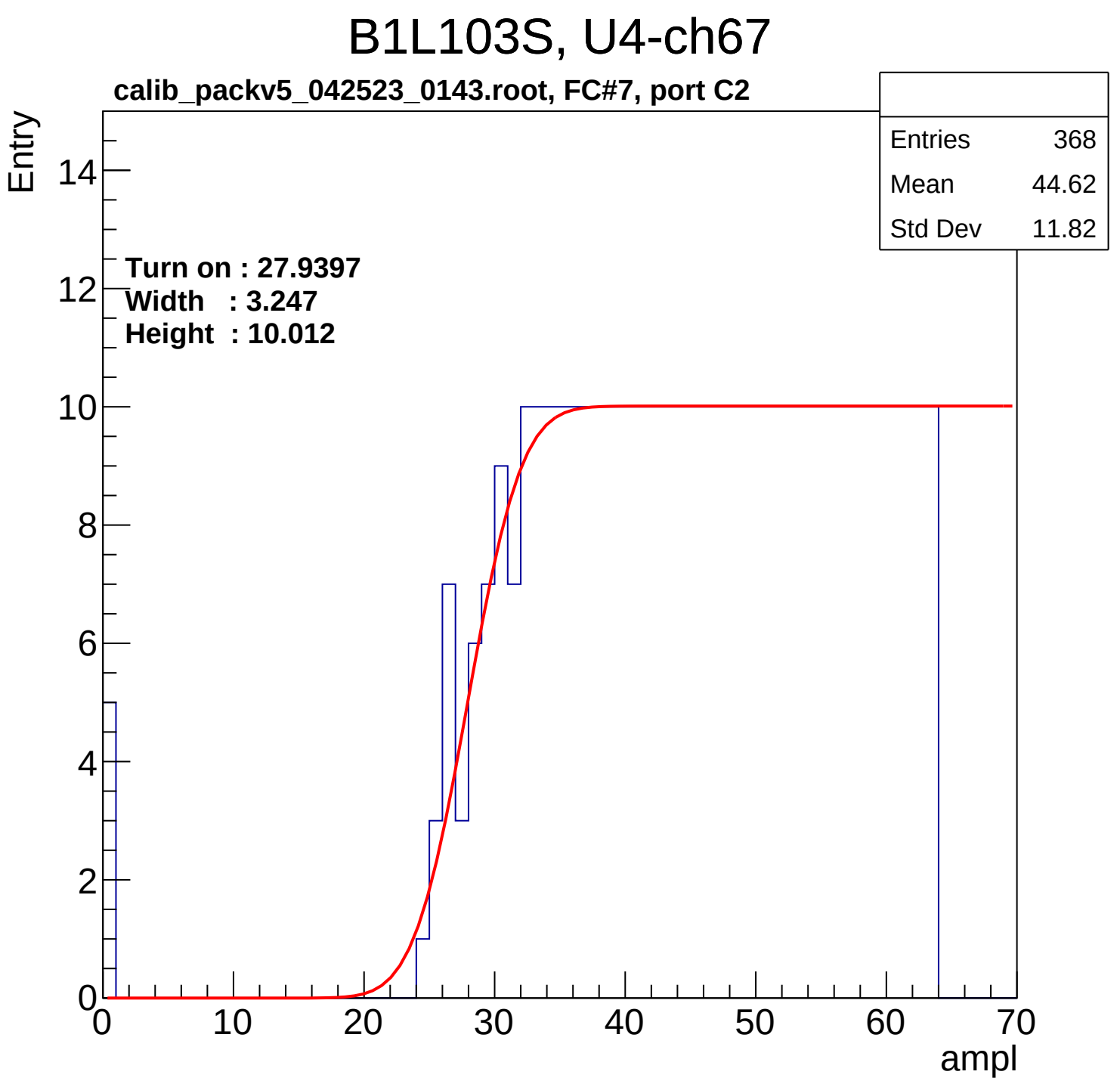
B1L103S, U4-ch67
calib_packv5_042523_0143.root, FC#7, port C2
Entries 368
Mean 44.62
Std Dev 11.82
Turn on : 27.9397
Width : 3.247
Height : 10.012
Entry
ampl
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2
4
6
8
10
12
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0
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60
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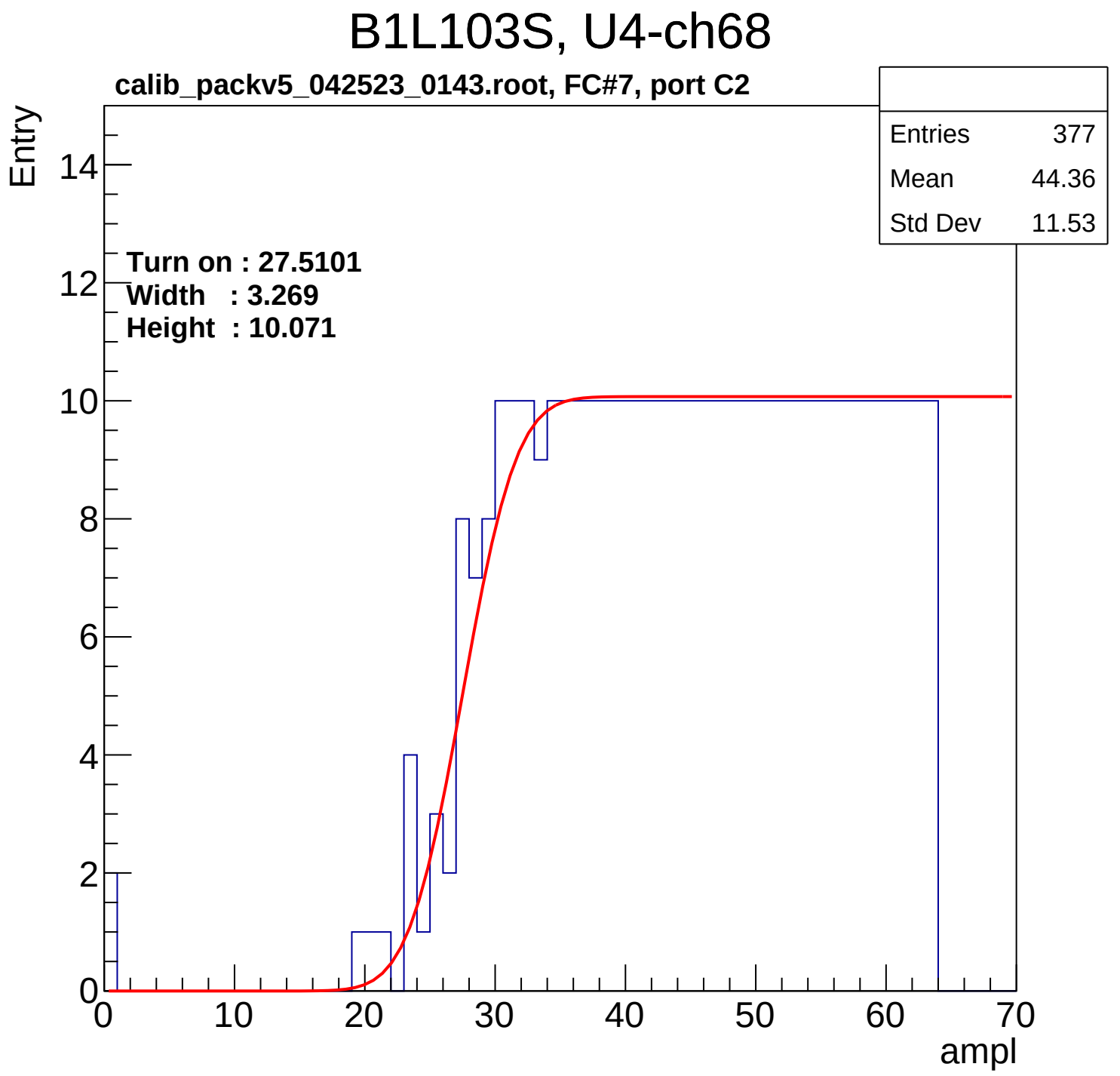
B1L103S, U4-ch68
calib_packv5_042523_0143.root, FC#7, port C2
Entries 377
Mean 44.36
Std Dev 11.53
Turn on : 27.5101
Width : 3.269
Height : 10.071
Entry
ampl
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8
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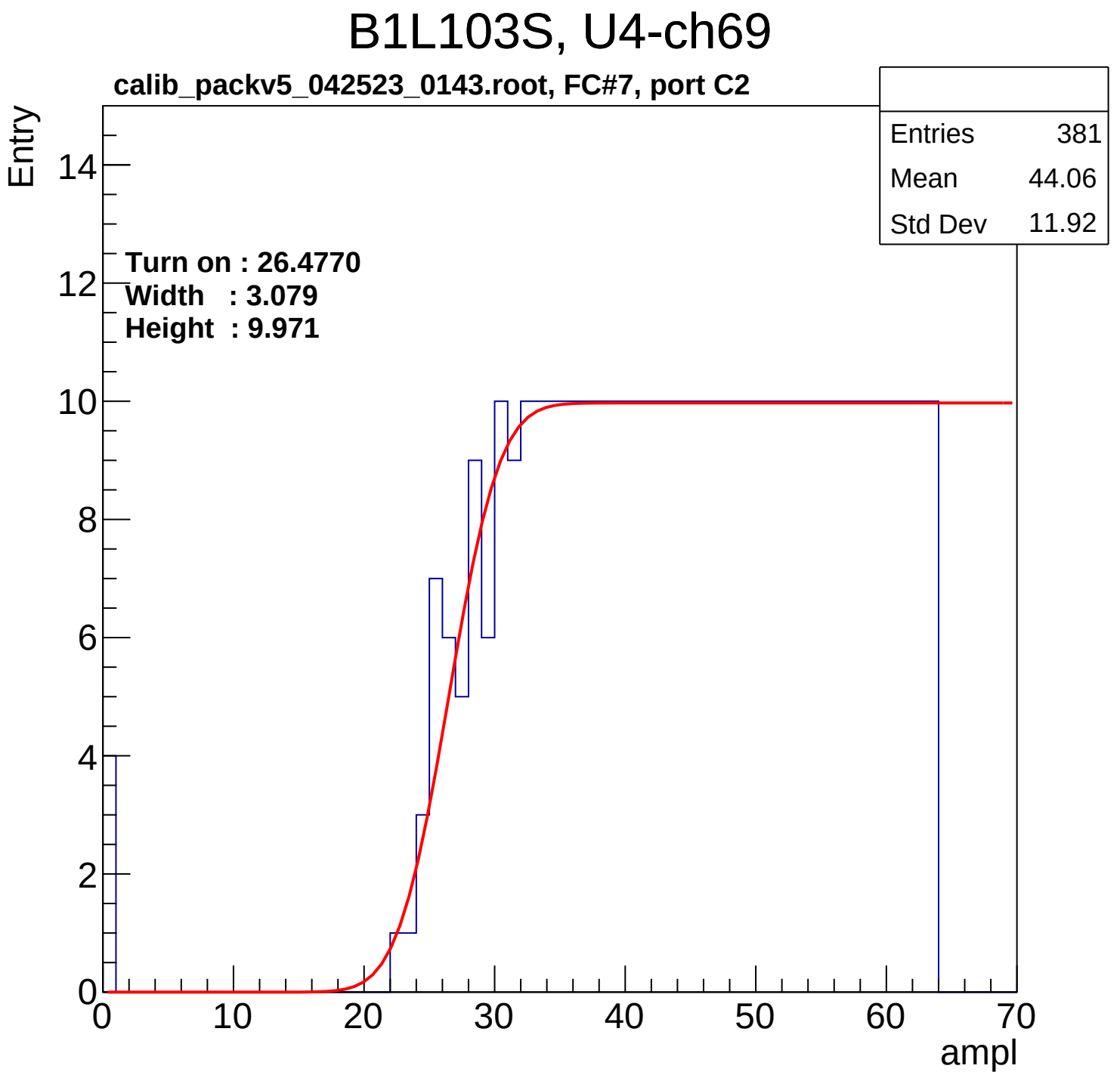
B1L103S, U4-ch69
calib_packv5_042523_0143.root, FC#7, port C2
Entries 381
Mean 44.06
Std Dev 11.92
Turn on : 26.4770
Width : 3.079
Height : 9.971
Entry
ampl
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6
8
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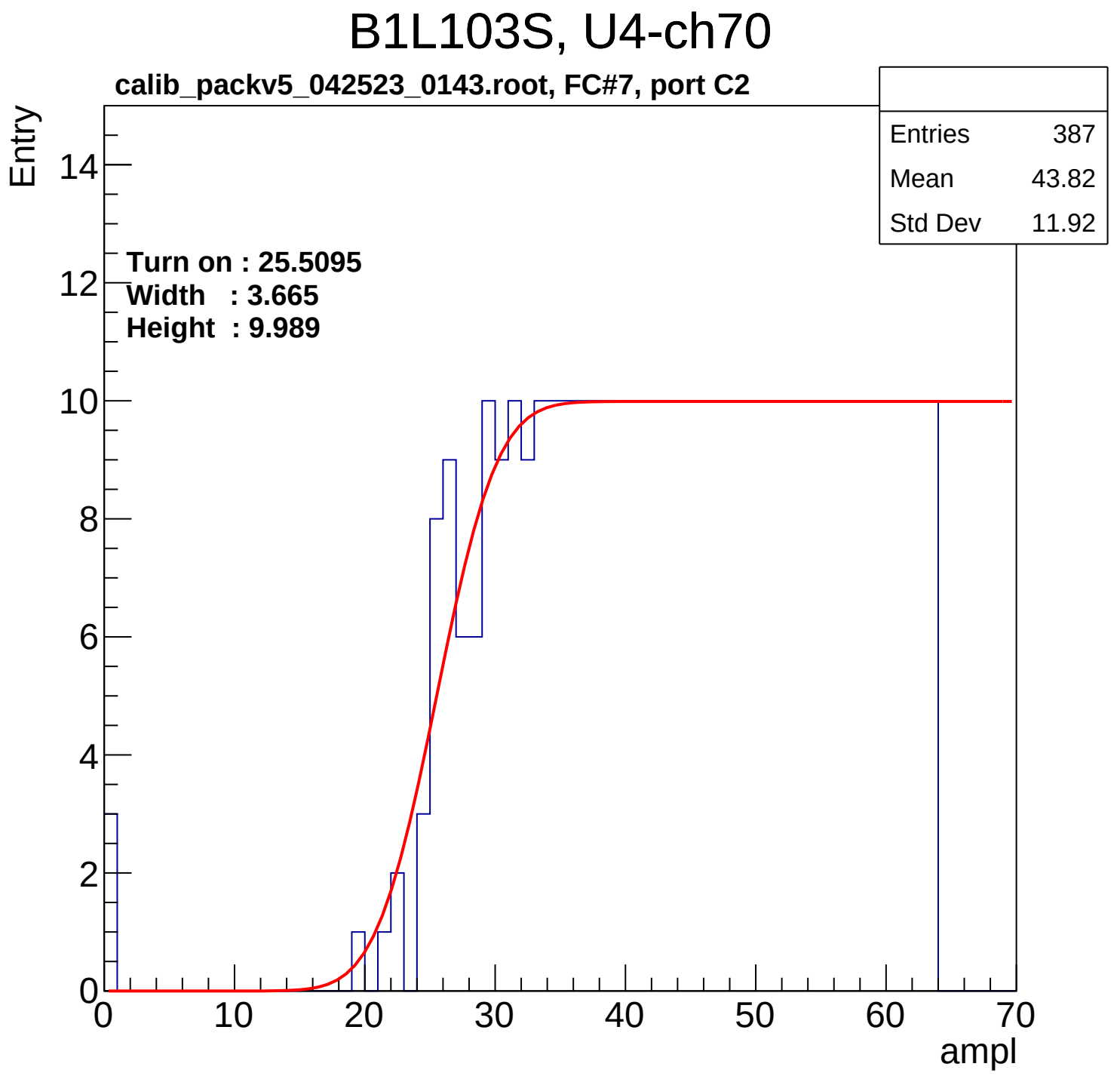
B1L103S, U4-ch70
calib_packv5_042523_0143.root, FC#7, port C2
Entries 387
Mean 43.82
Std Dev 11.92
Turn on : 25.5095
Width : 3.665
Height : 9.989
Entry
ampl
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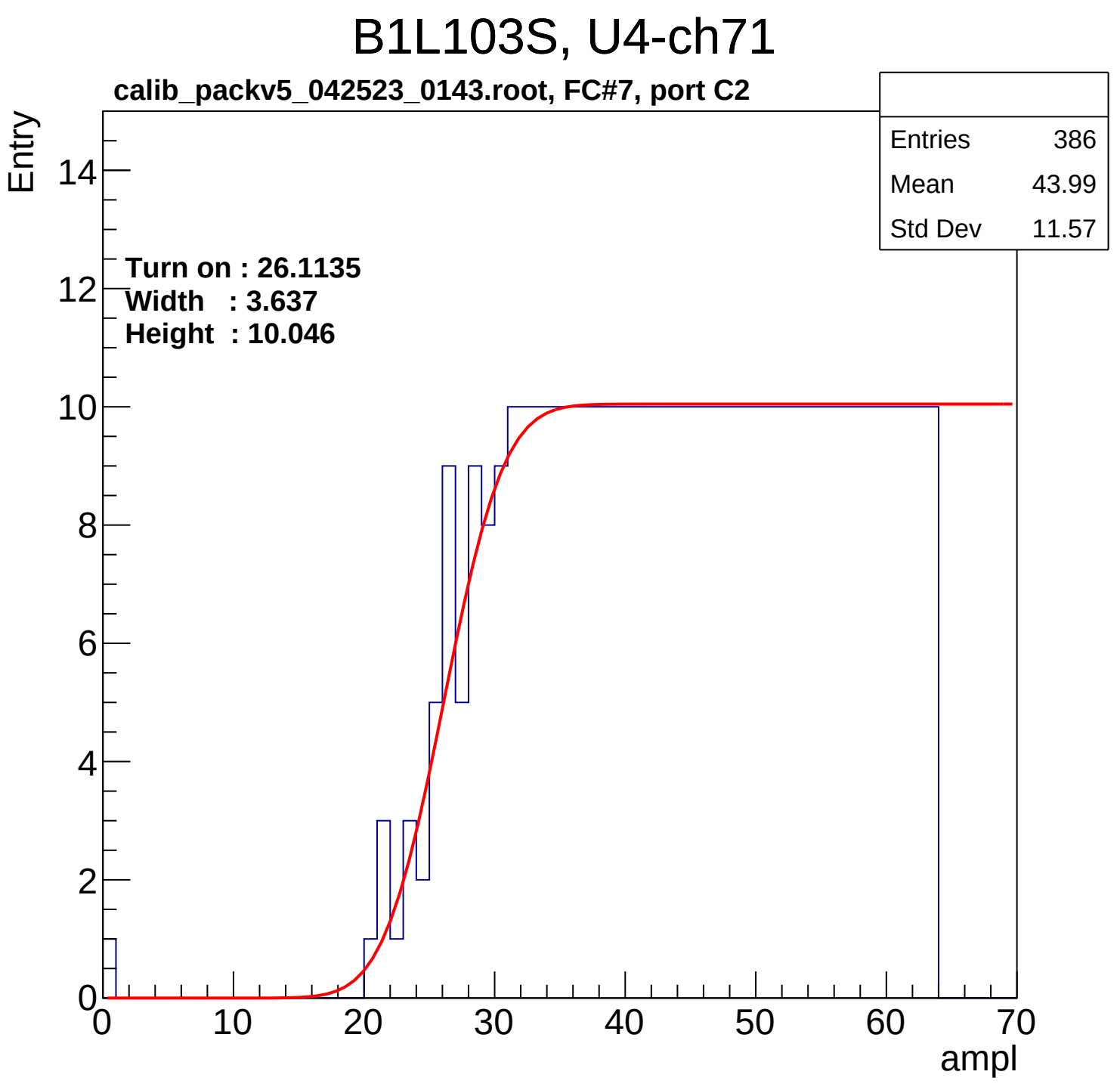
B1L103S, U4-ch71
calib_packv5_042523_0143.root, FC#7, port C2
Entries 386
Mean 43.99
Std Dev 11.57
Turn on : 26.1135
Width : 3.637
Height : 10.046
Entry
ampl
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6
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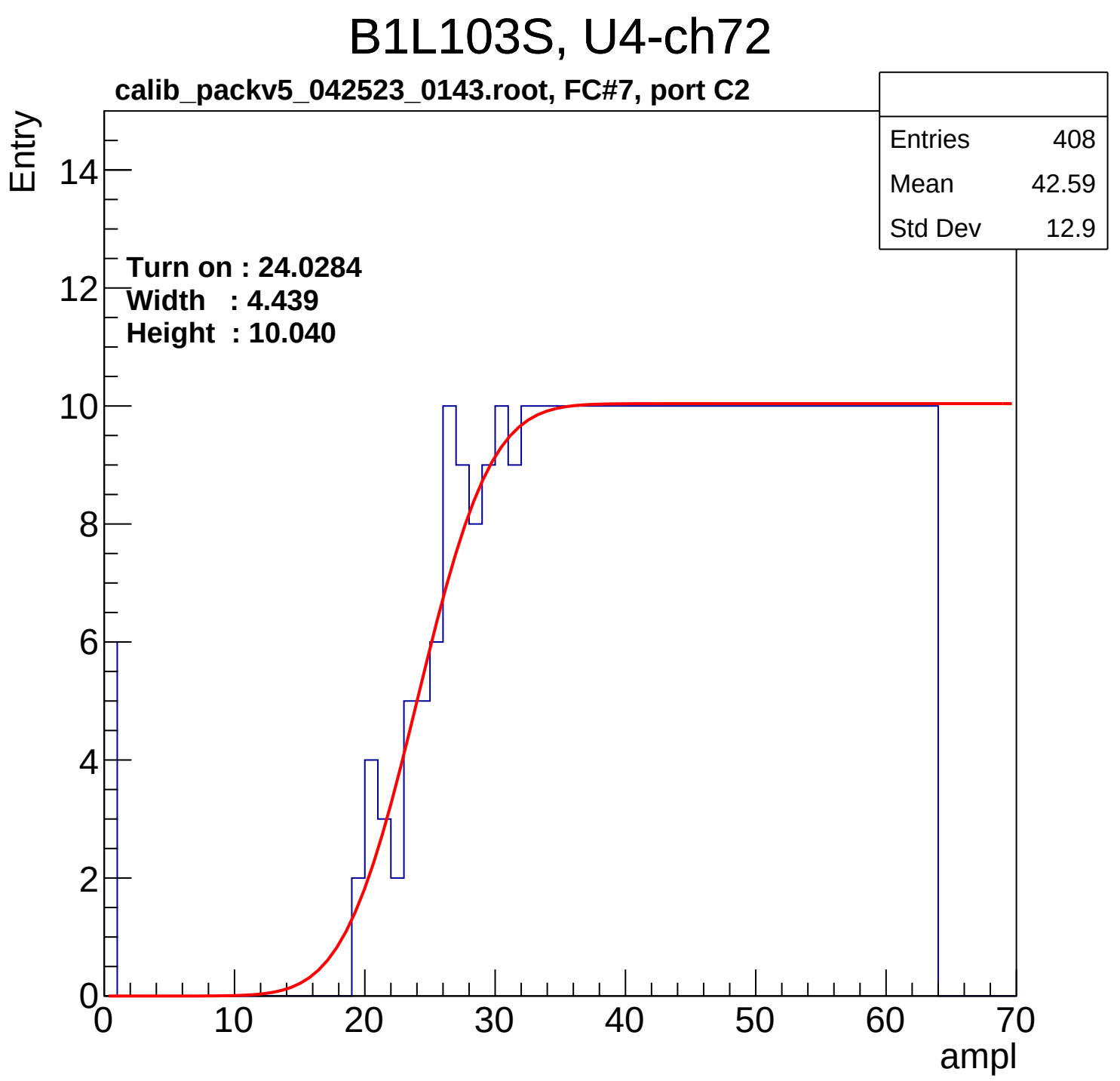
B1L103S, U4-ch72
calib_packv5_042523_0143.root, FC#7, port C2
Entries 408
Mean 42.59
Std Dev 12.9
Turn on : 24.0284
Width : 4.439
Height : 10.040
Entry
ampl
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6
8
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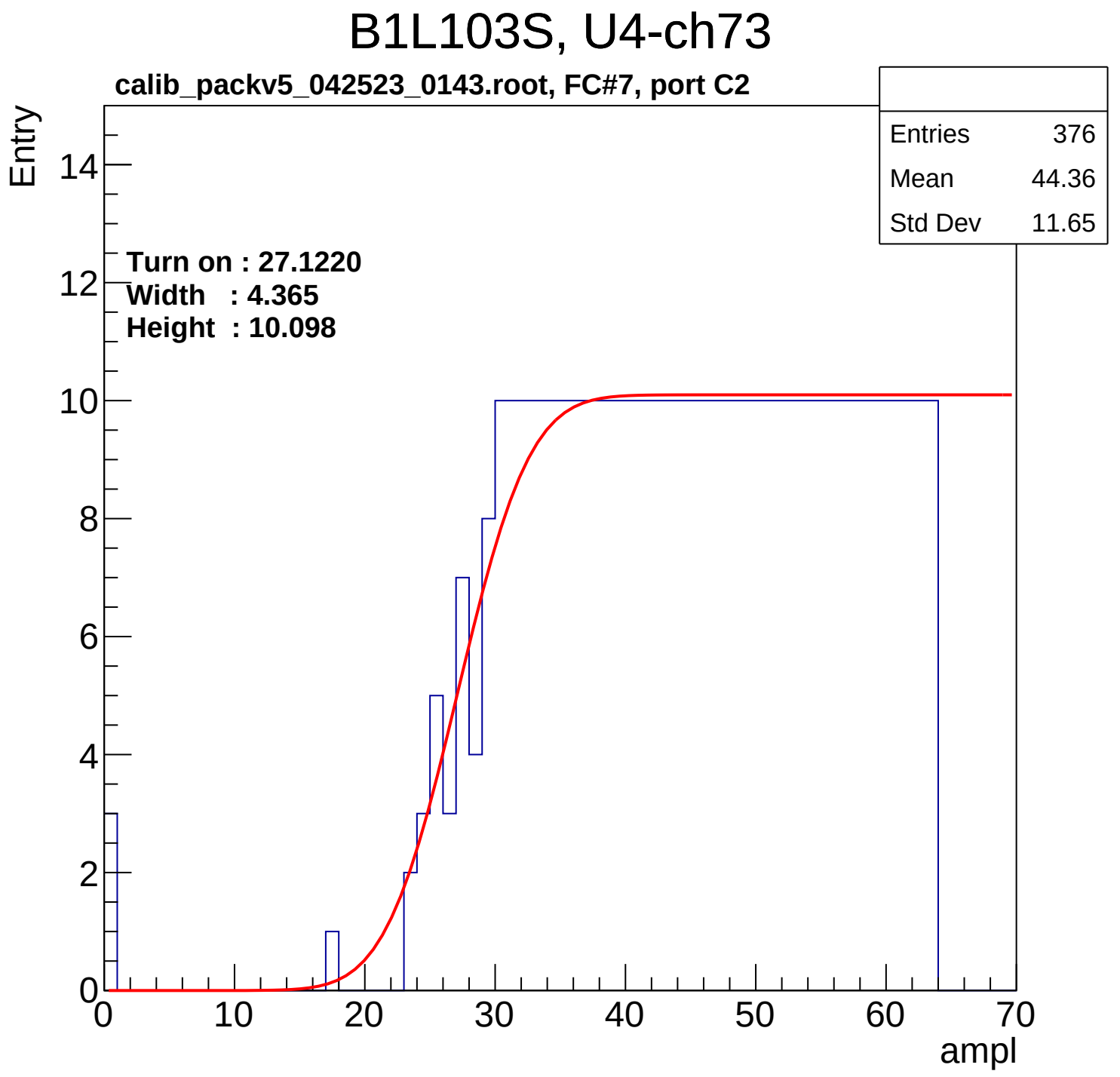
B1L103S, U4-ch73
calib_packv5_042523_0143.root, FC#7, port C2
Entries 376
Mean 44.36
Std Dev 11.65
Turn on : 27.1220
Width : 4.365
Height : 10.098
Entry
ampl
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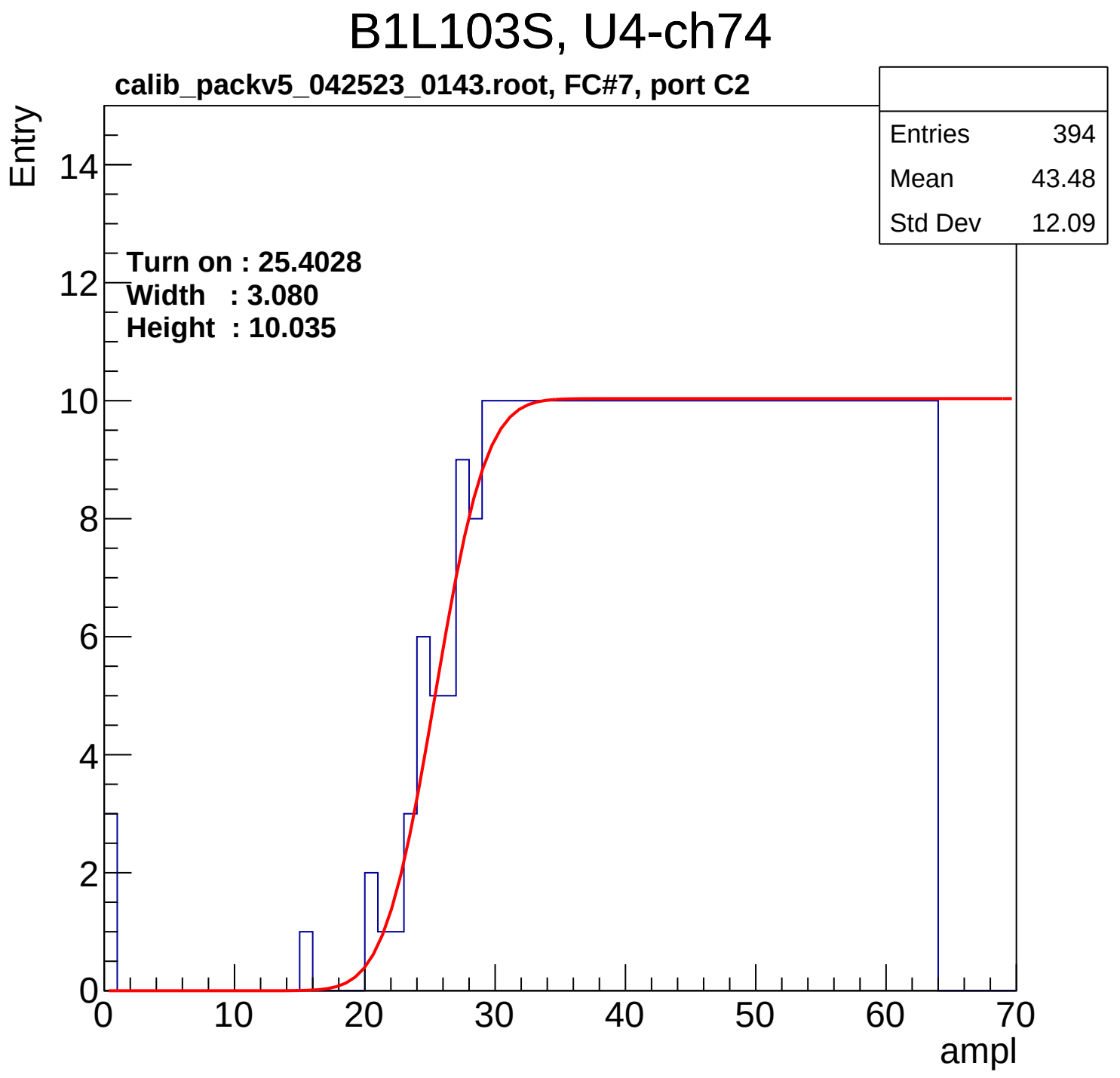
B1L103S, U4-ch74
calib_packv5_042523_0143.root, FC#7, port C2
Entries 394
Mean 43.48
Std Dev 12.09
Turn on : 25.4028
Width : 3.080
Height : 10.035
Entry
ampl
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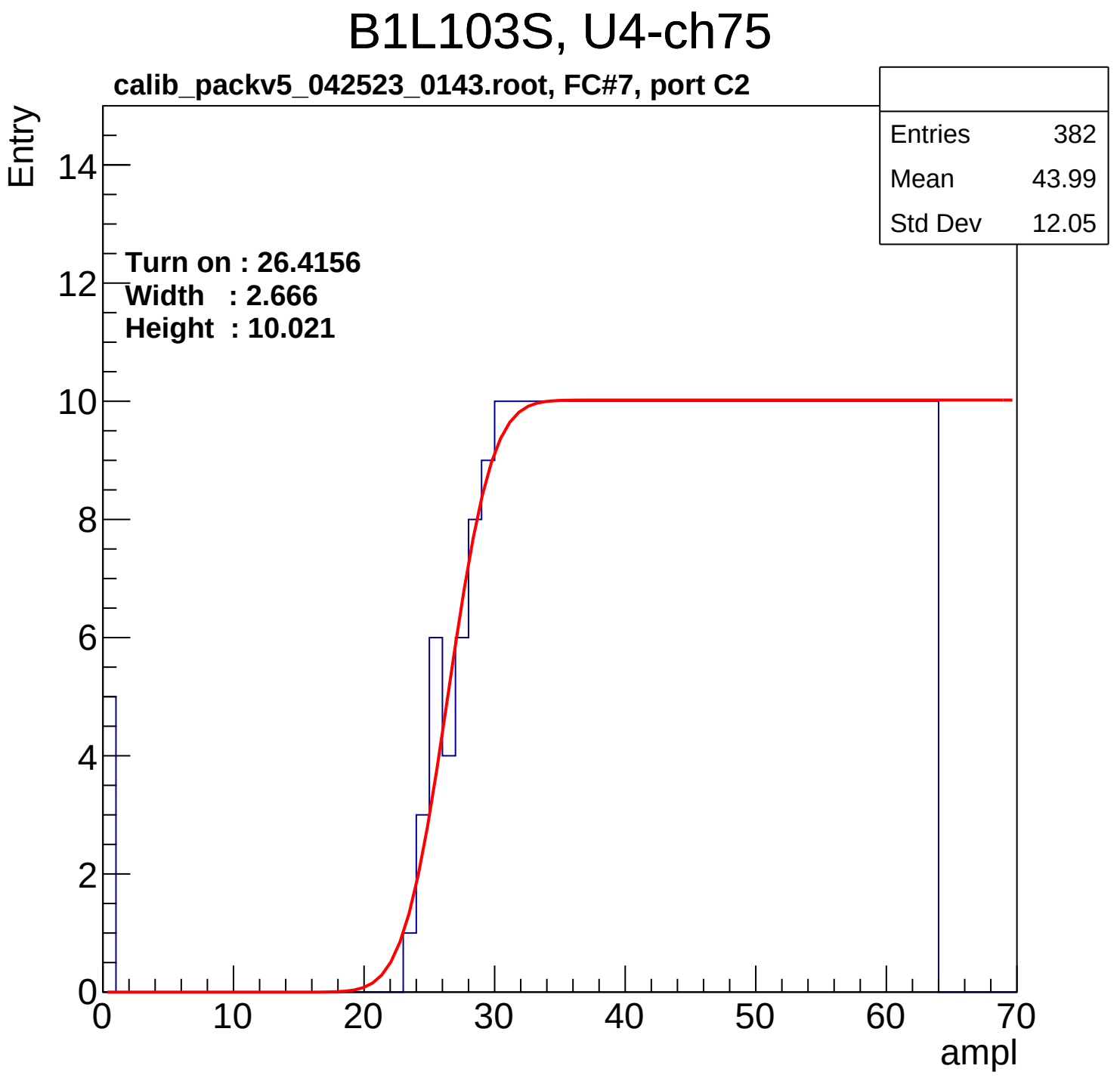
B1L103S, U4-ch75
calib_packv5_042523_0143.root, FC#7, port C2
Entries 382
Mean 43.99
Std Dev 12.05
Turn on : 26.4156
Width : 2.666
Height : 10.021
Entry
ampl
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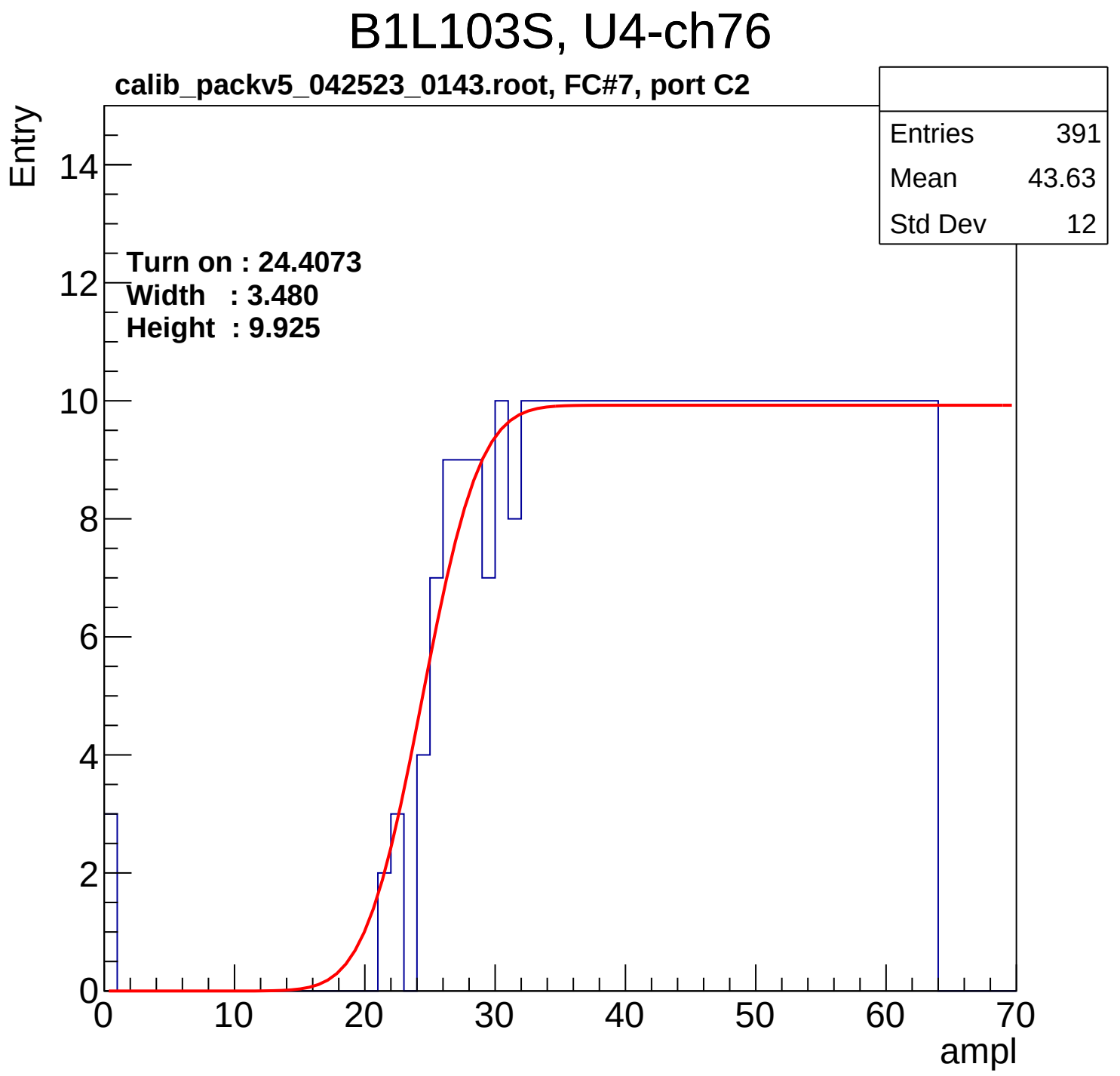
B1L103S, U4-ch76
calib_packv5_042523_0143.root, FC#7, port C2
Entries 391
Mean 43.63
Std Dev 12
Turn on : 24.4073
Width : 3.480
Height : 9.925
Entry
ampl
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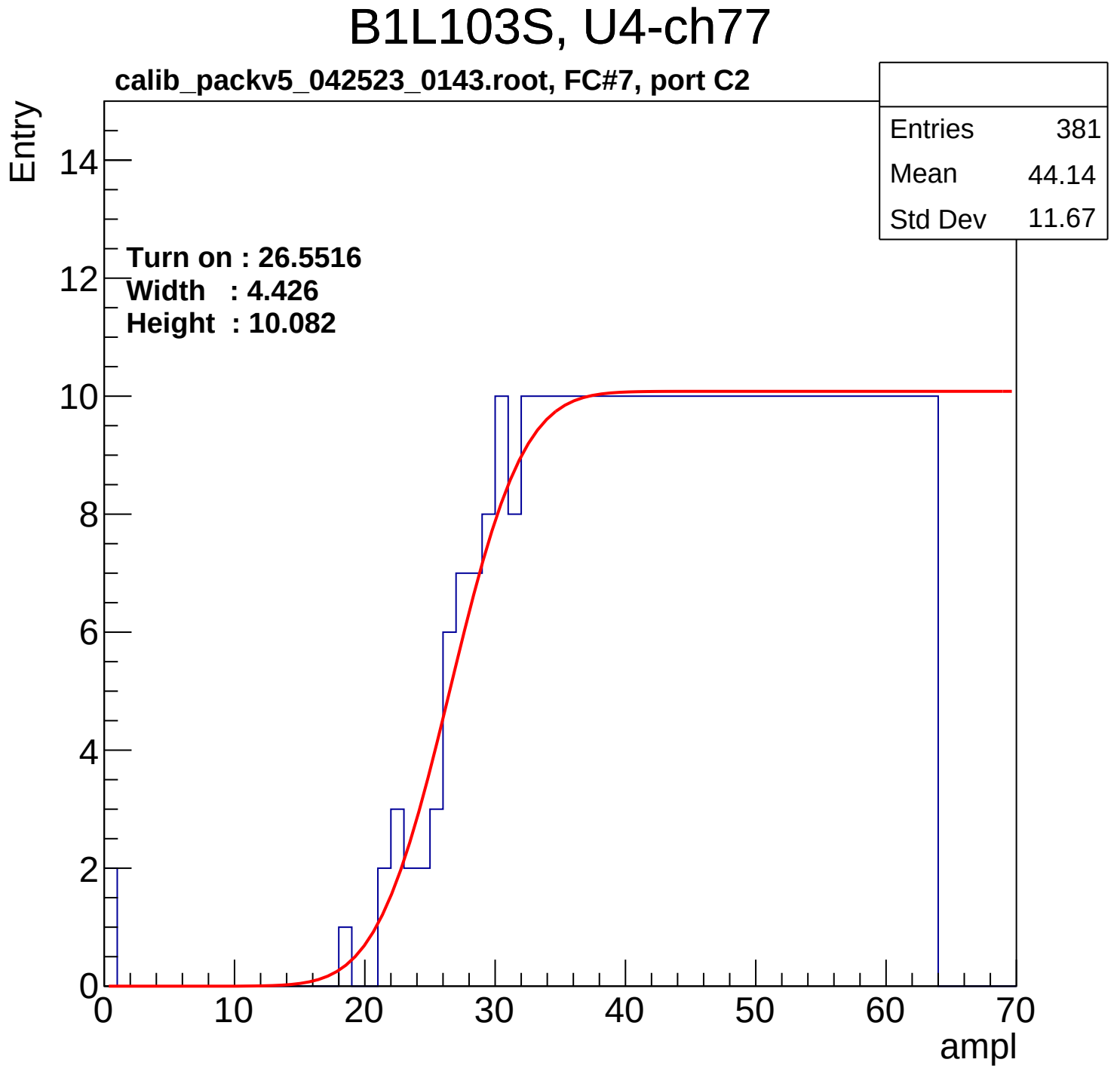
B1L103S, U4-ch77
calib_packv5_042523_0143.root, FC#7, port C2
Entries 381
Mean 44.14
Std Dev 11.67
Turn on : 26.5516
Width : 4.426
Height : 10.082
Entry
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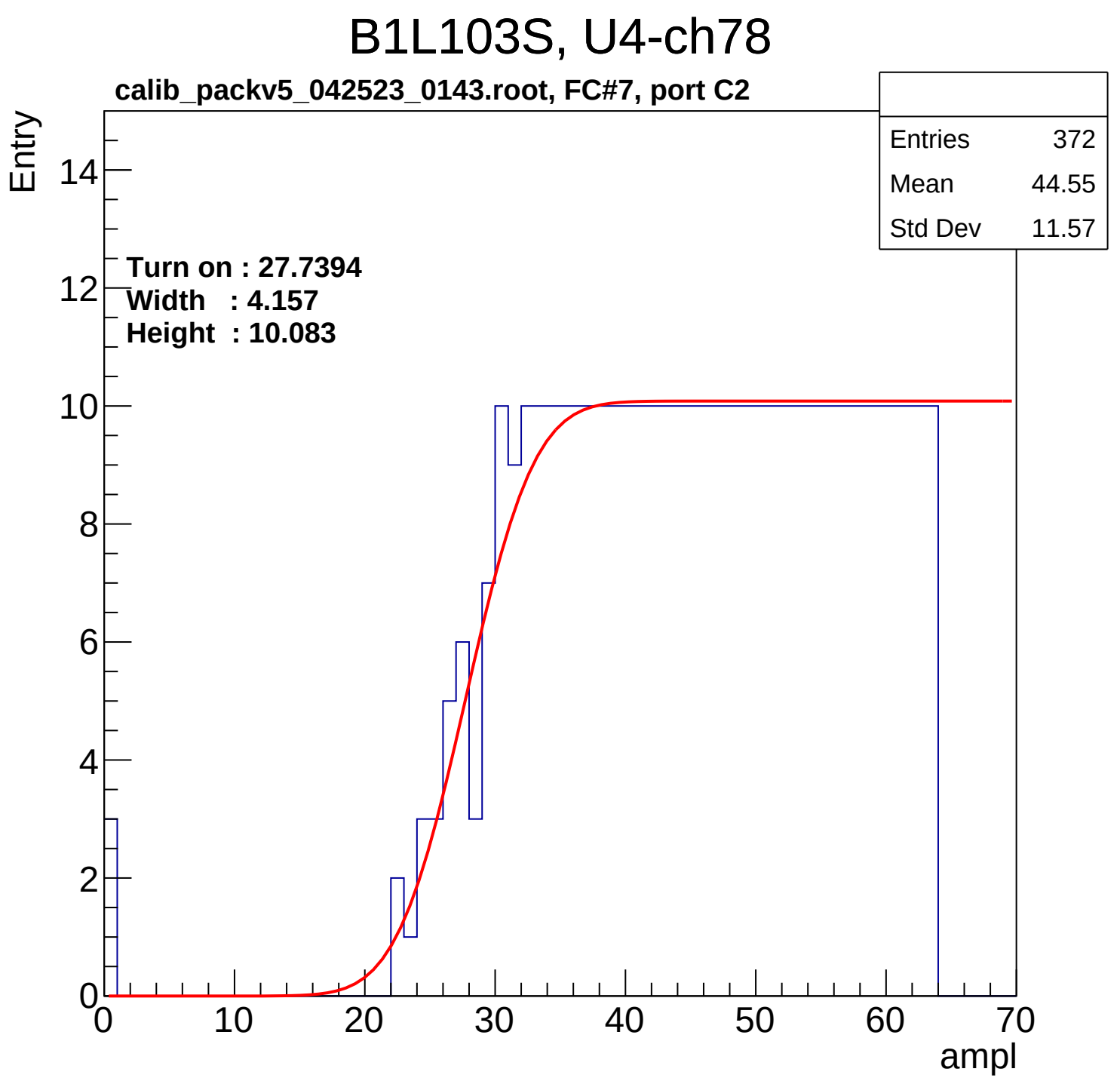
B1L103S, U4-ch78
calib_packv5_042523_0143.root, FC#7, port C2
Entries 372
Mean 44.55
Std Dev 11.57
Turn on : 27.7394
Width : 4.157
Height : 10.083
Entry
ampl
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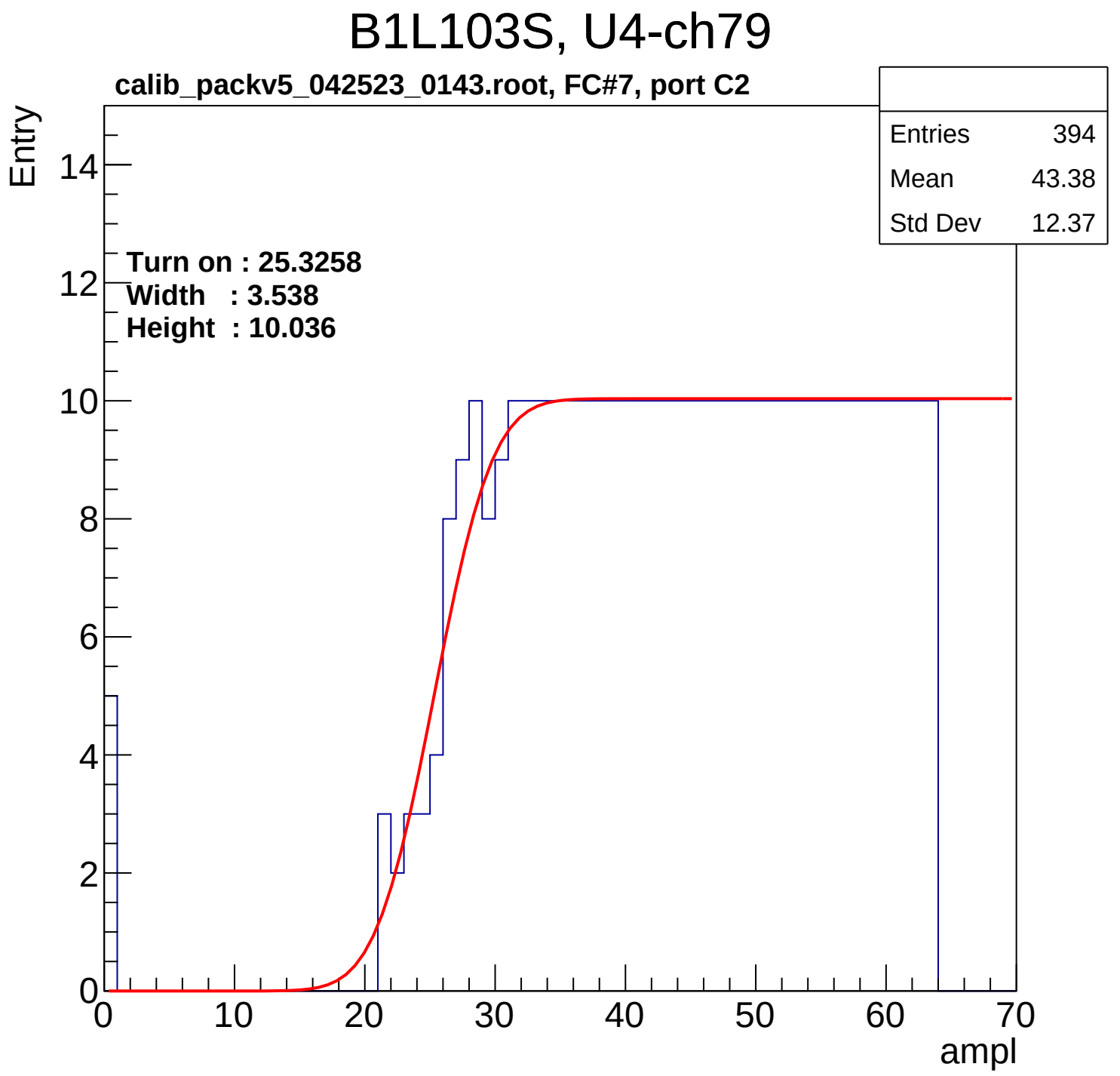
B1L103S, U4-ch79
calib_packv5_042523_0143.root, FC#7, port C2
Entries 394
Mean 43.38
Std Dev 12.37
Turn on : 25.3258
Width : 3.538
Height : 10.036
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ampl
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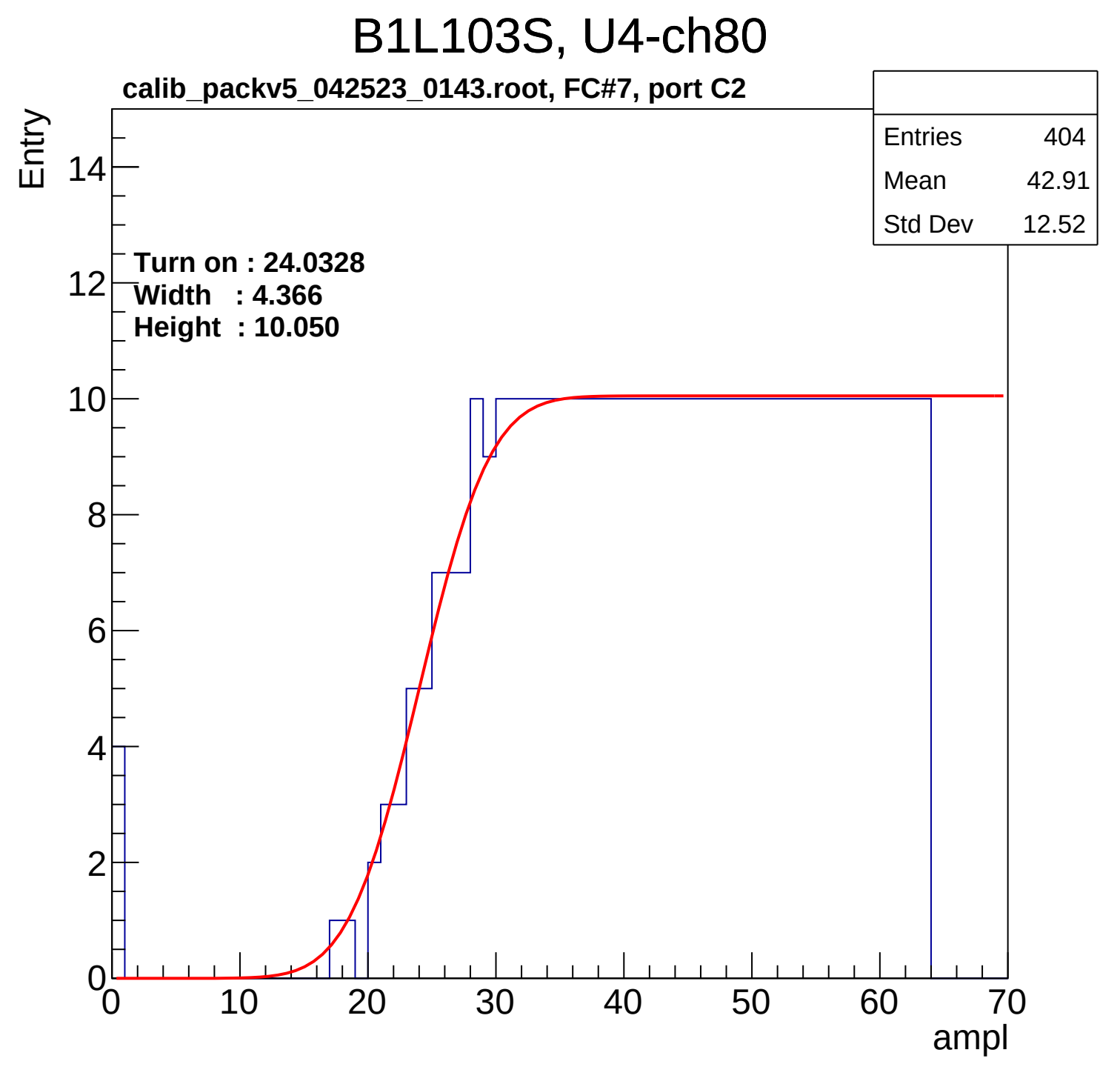
B1L103S, U4-ch80
calib_packv5_042523_0143.root, FC#7, port C2
Entries 404
Mean 42.91
Std Dev 12.52
Turn on : 24.0328
Width : 4.366
Height : 10.050
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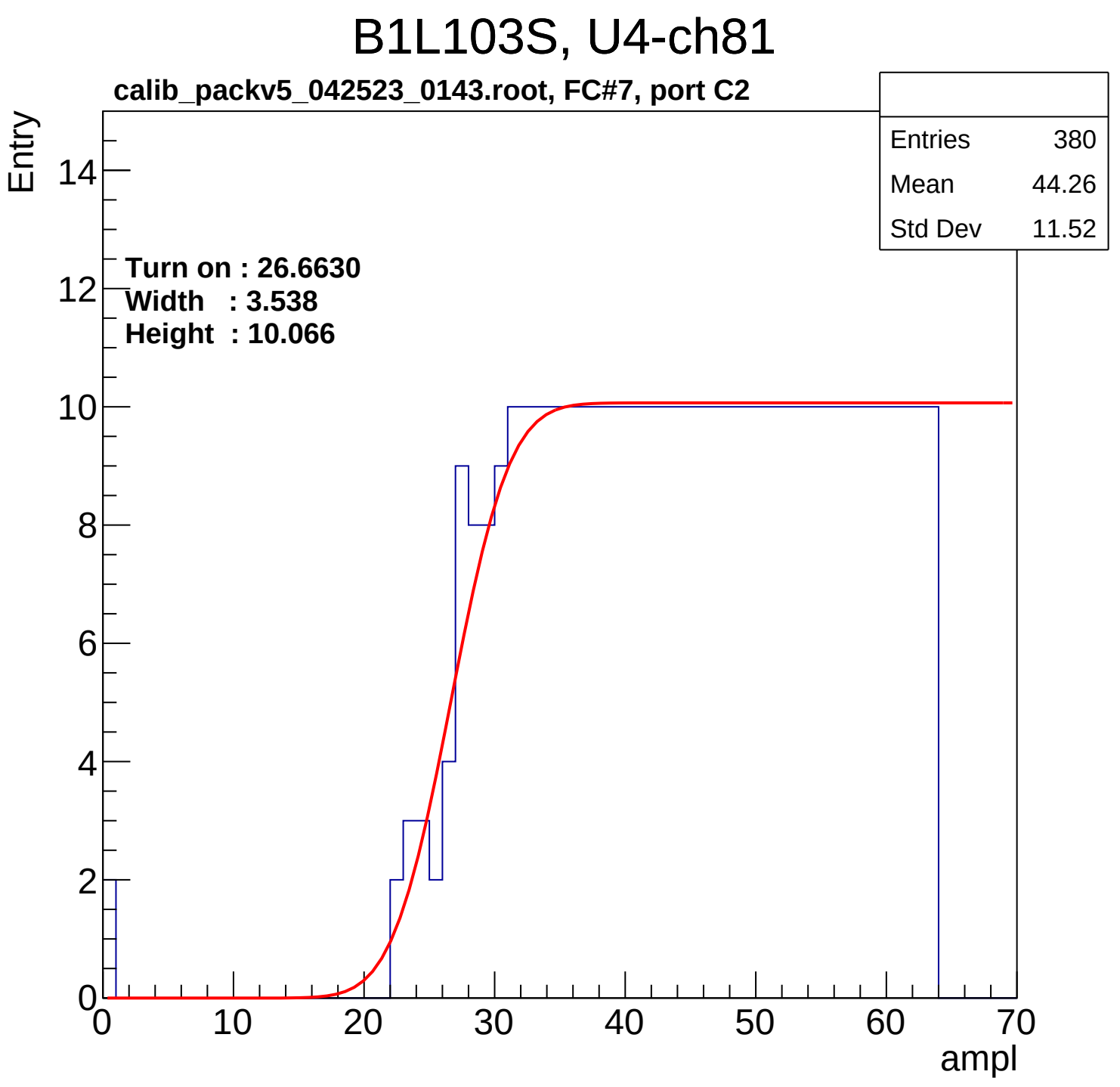
B1L103S, U4-ch81
calib_packv5_042523_0143.root, FC#7, port C2
Entries 380
Mean 44.26
Std Dev 11.52
Turn on : 26.6630
Width : 3.538
Height : 10.066
Entry
ampl
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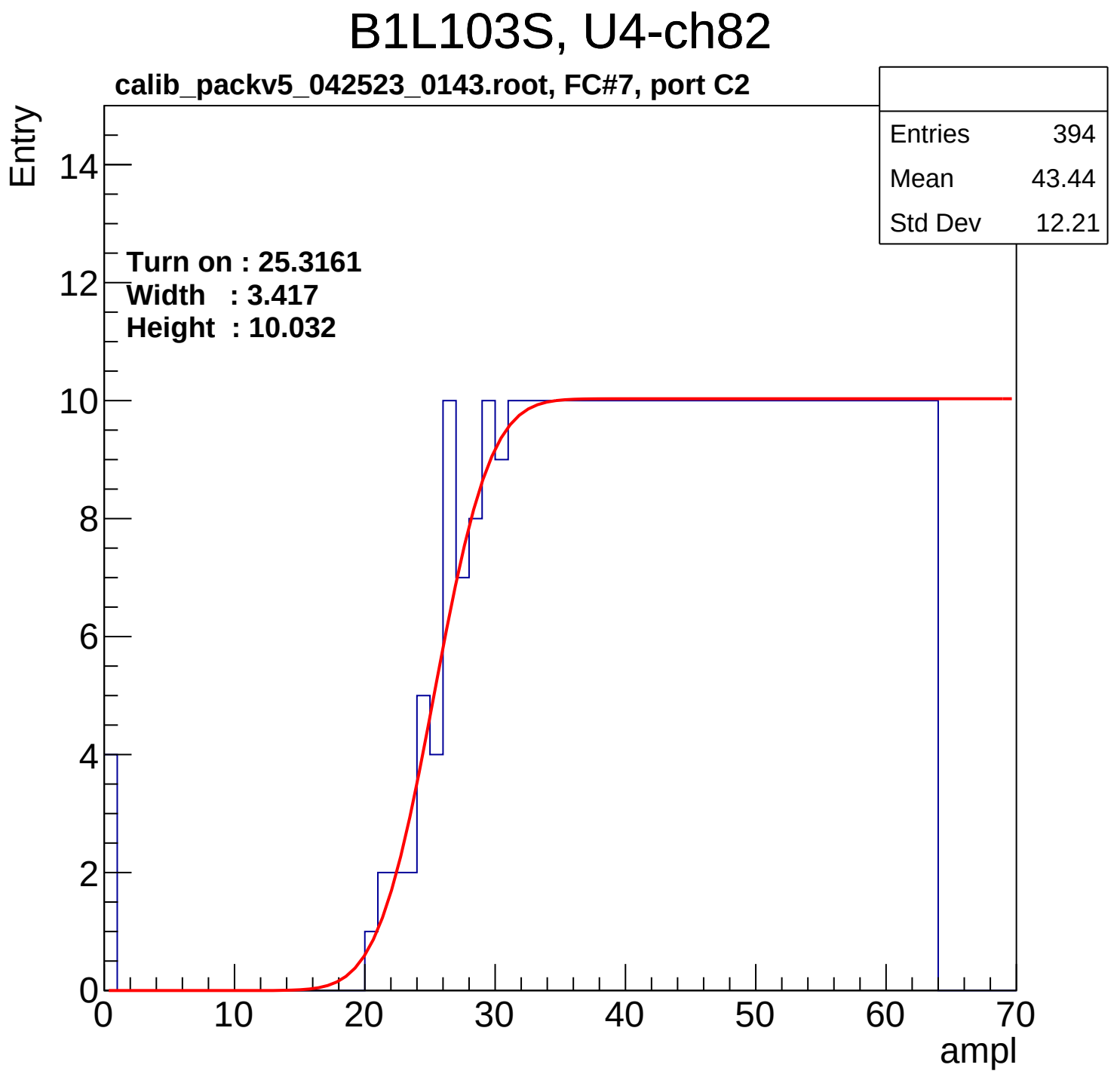
B1L103S, U4-ch82
calib_packv5_042523_0143.root, FC#7, port C2
Entries 394
Mean 43.44
Std Dev 12.21
Turn on : 25.3161
Width : 3.417
Height : 10.032
Entry
ampl
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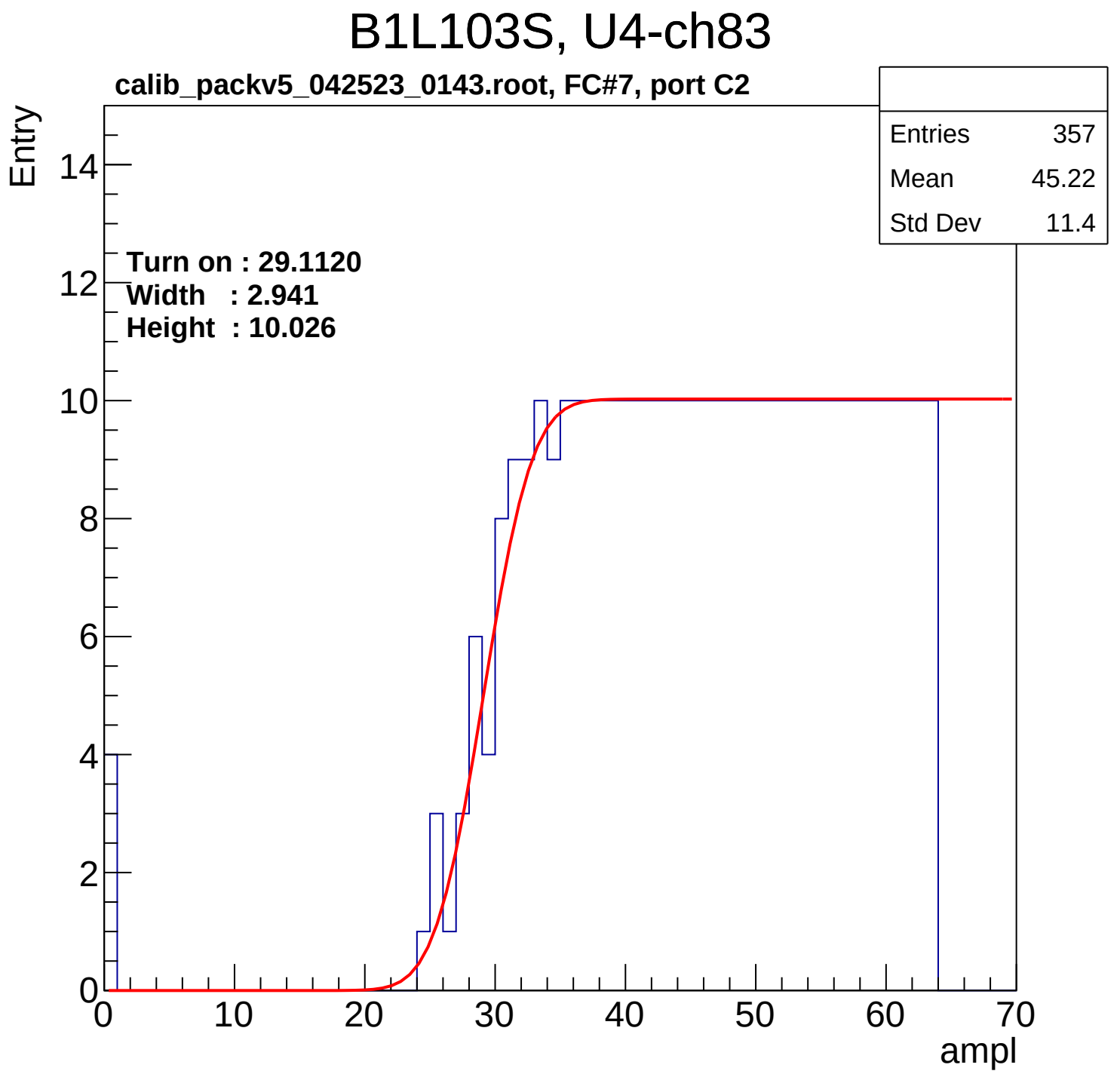
B1L103S, U4-ch83
calib_packv5_042523_0143.root, FC#7, port C2
Entries 357
Mean 45.22
Std Dev 11.4
Turn on : 29.1120
Width : 2.941
Height : 10.026
Entry
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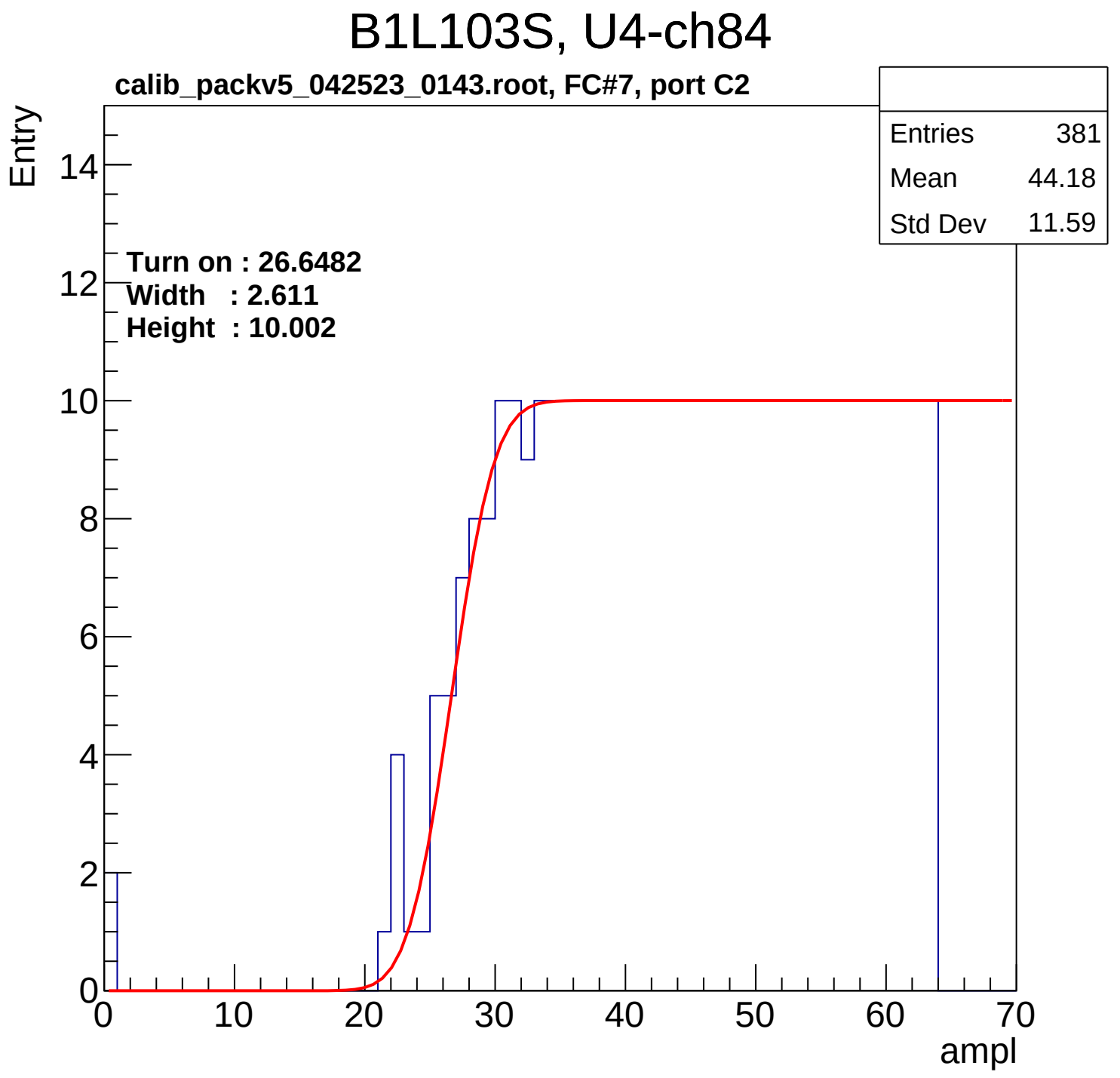
B1L103S, U4-ch84
calib_packv5_042523_0143.root, FC#7, port C2
Entries 381
Mean 44.18
Std Dev 11.59
Turn on : 26.6482
Width : 2.611
Height : 10.002
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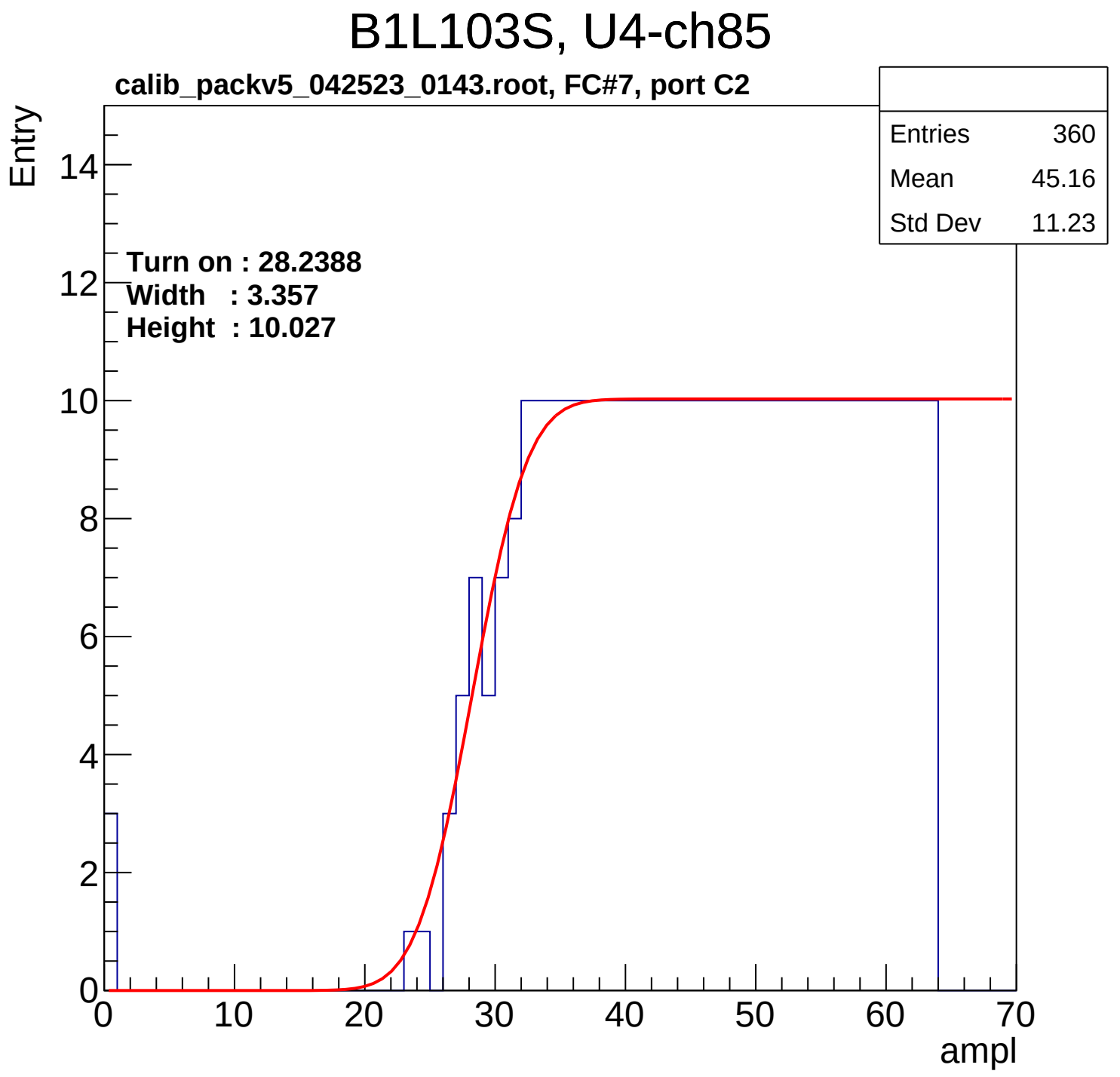
B1L103S, U4-ch85
calib_packv5_042523_0143.root, FC#7, port C2
Entries 360
Mean 45.16
Std Dev 11.23
Turn on : 28.2388
Width : 3.357
Height : 10.027
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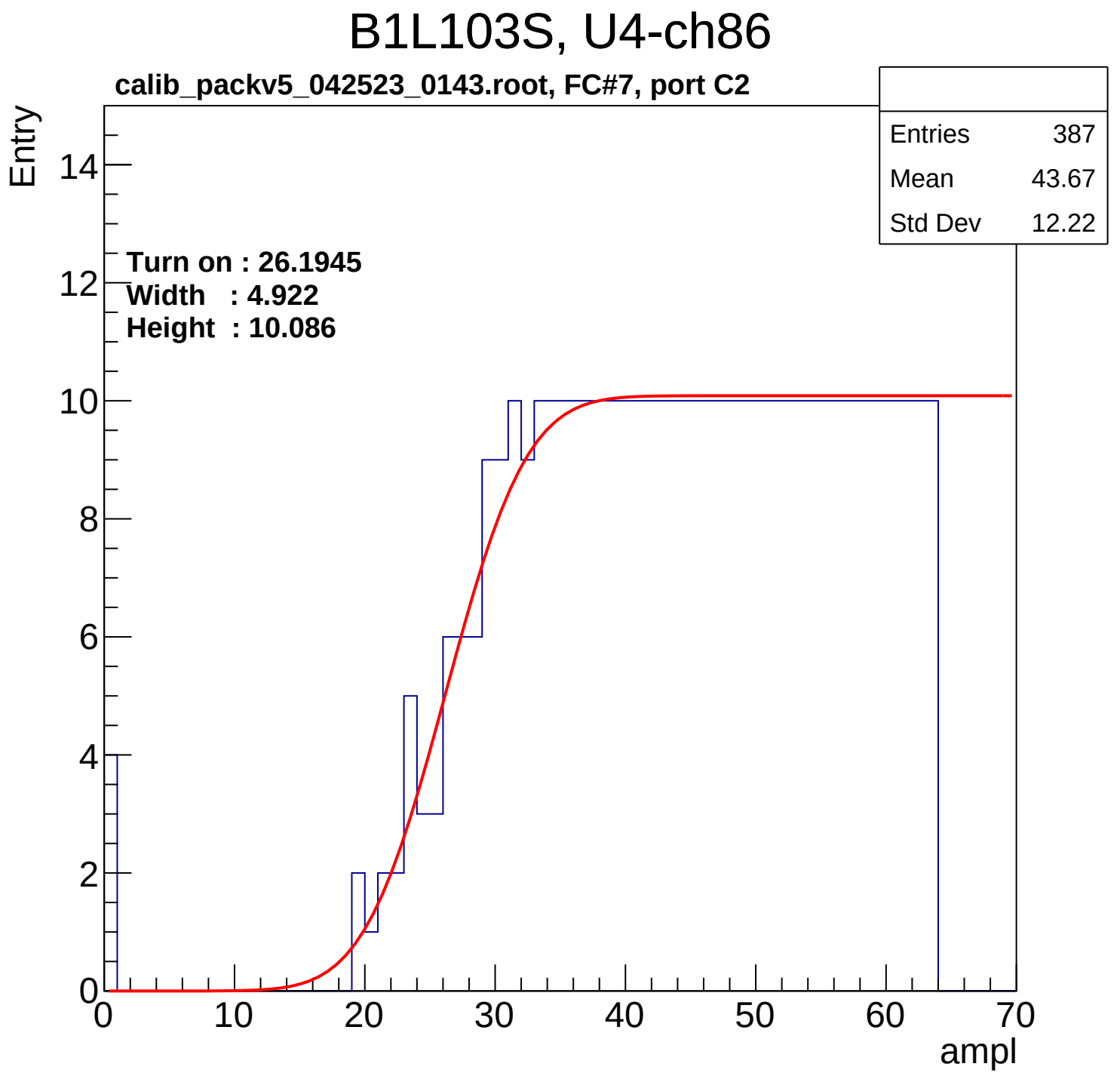
B1L103S, U4-ch86
calib_packv5_042523_0143.root, FC#7, port C2
Entries 387
Mean 43.67
Std Dev 12.22
Turn on : 26.1945
Width : 4.922
Height : 10.086
Entry
ampl
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6
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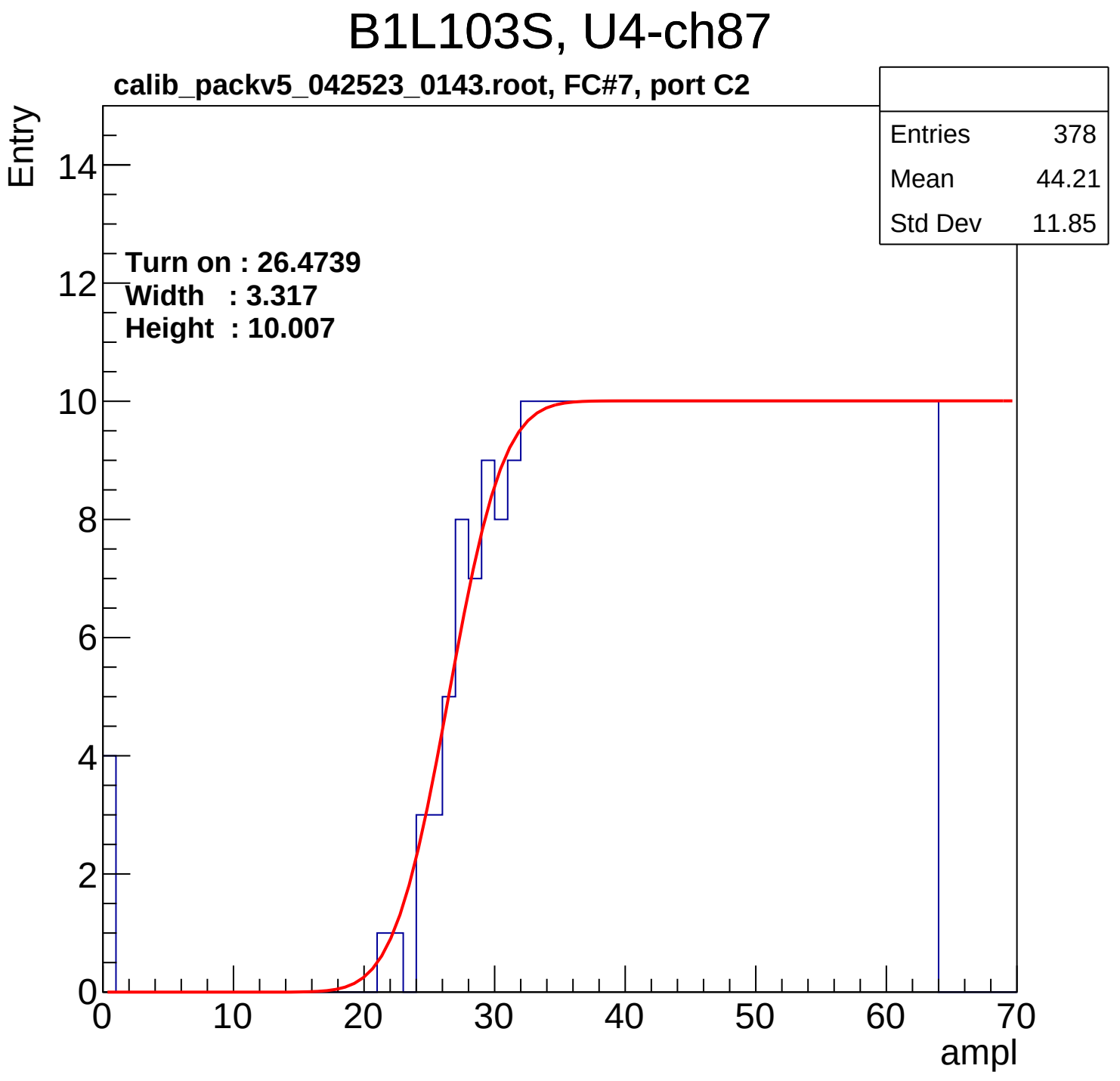
B1L103S, U4-ch87
calib_packv5_042523_0143.root, FC#7, port C2
Entries 378
Mean 44.21
Std Dev 11.85
Turn on : 26.4739
Width : 3.317
Height : 10.007
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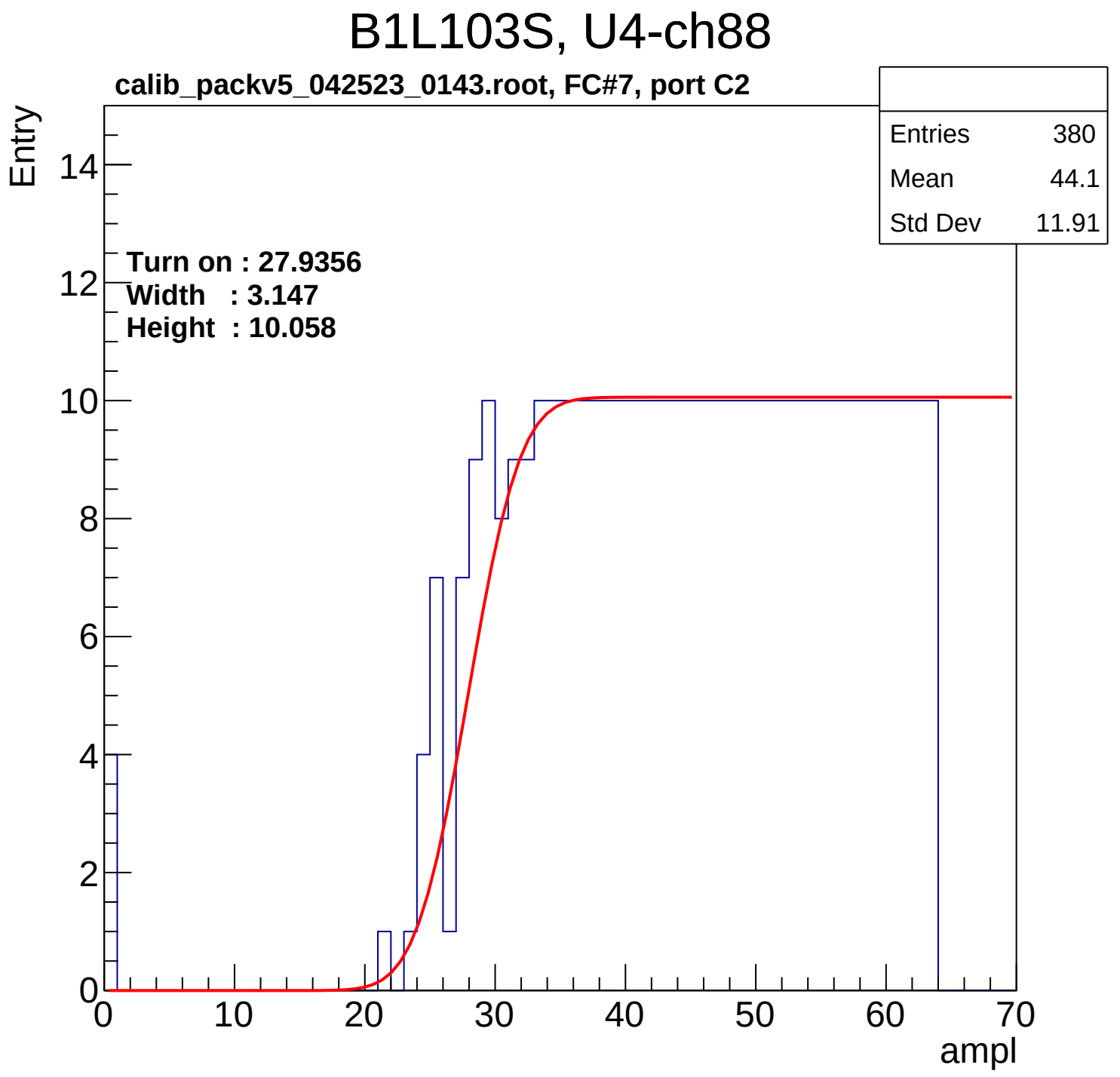
B1L103S, U4-ch88
calib_packv5_042523_0143.root, FC#7, port C2
Entries 380
Mean 44.1
Std Dev 11.91
Turn on : 27.9356
Width : 3.147
Height : 10.058
Entry
ampl
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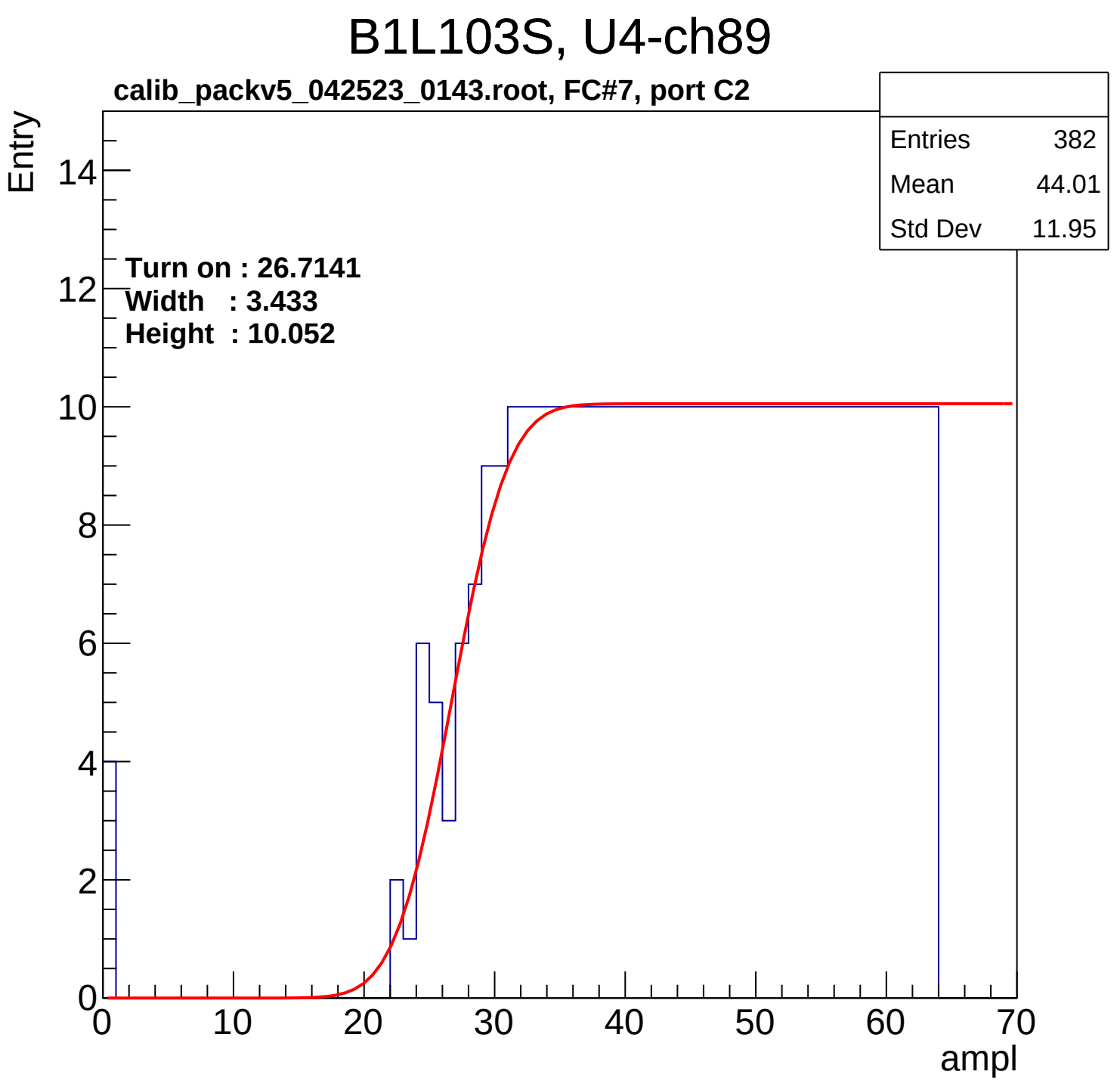
B1L103S, U4-ch89
calib_packv5_042523_0143.root, FC#7, port C2
Entries 382
Mean 44.01
Std Dev 11.95
Turn on : 26.7141
Width : 3.433
Height : 10.052
Entry
ampl
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4
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8
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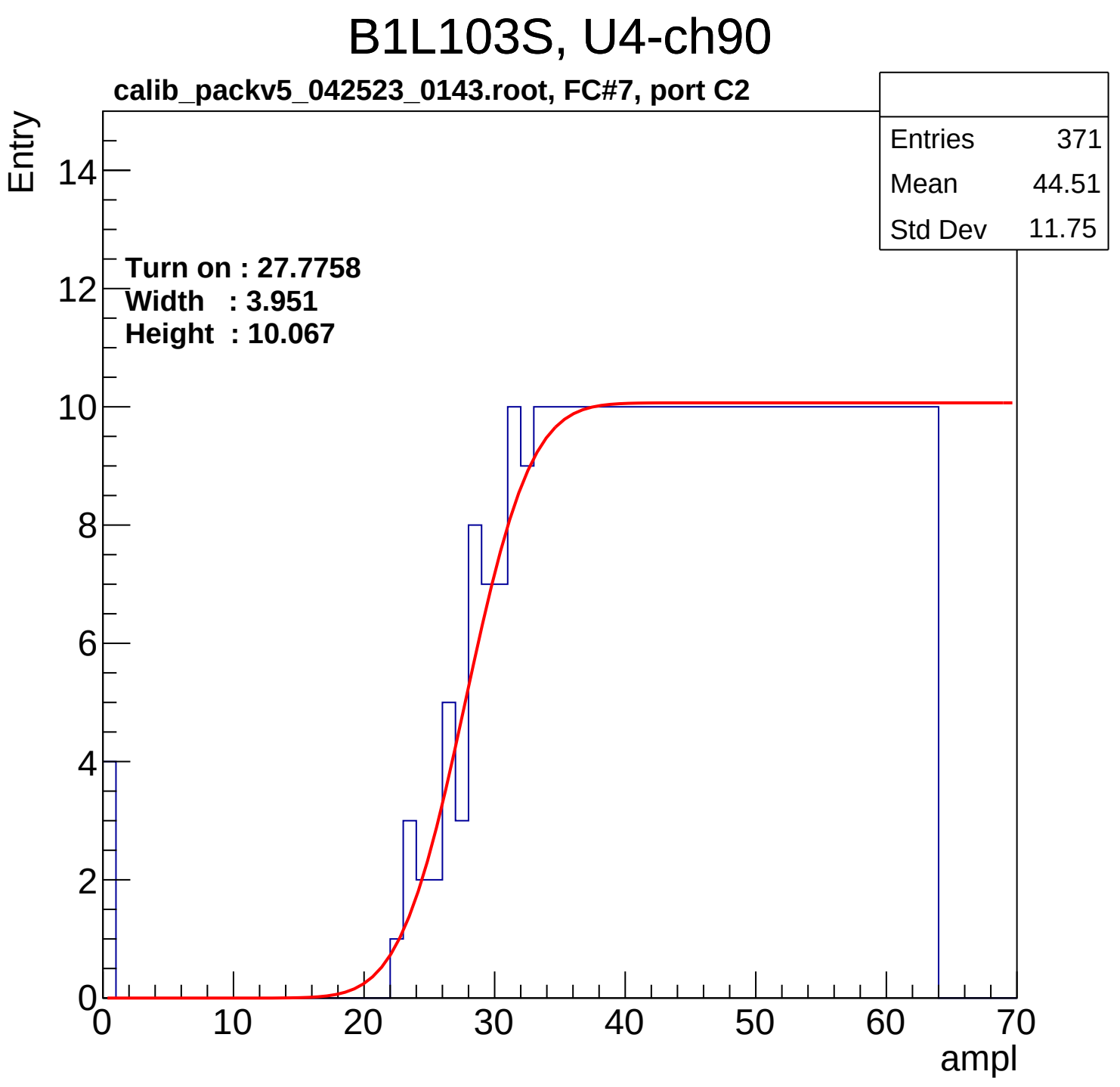
B1L103S, U4-ch90
calib_packv5_042523_0143.root, FC#7, port C2
Entries 371
Mean 44.51
Std Dev 11.75
Turn on : 27.7758
Width : 3.951
Height : 10.067
Entry
ampl
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6
8
10
12
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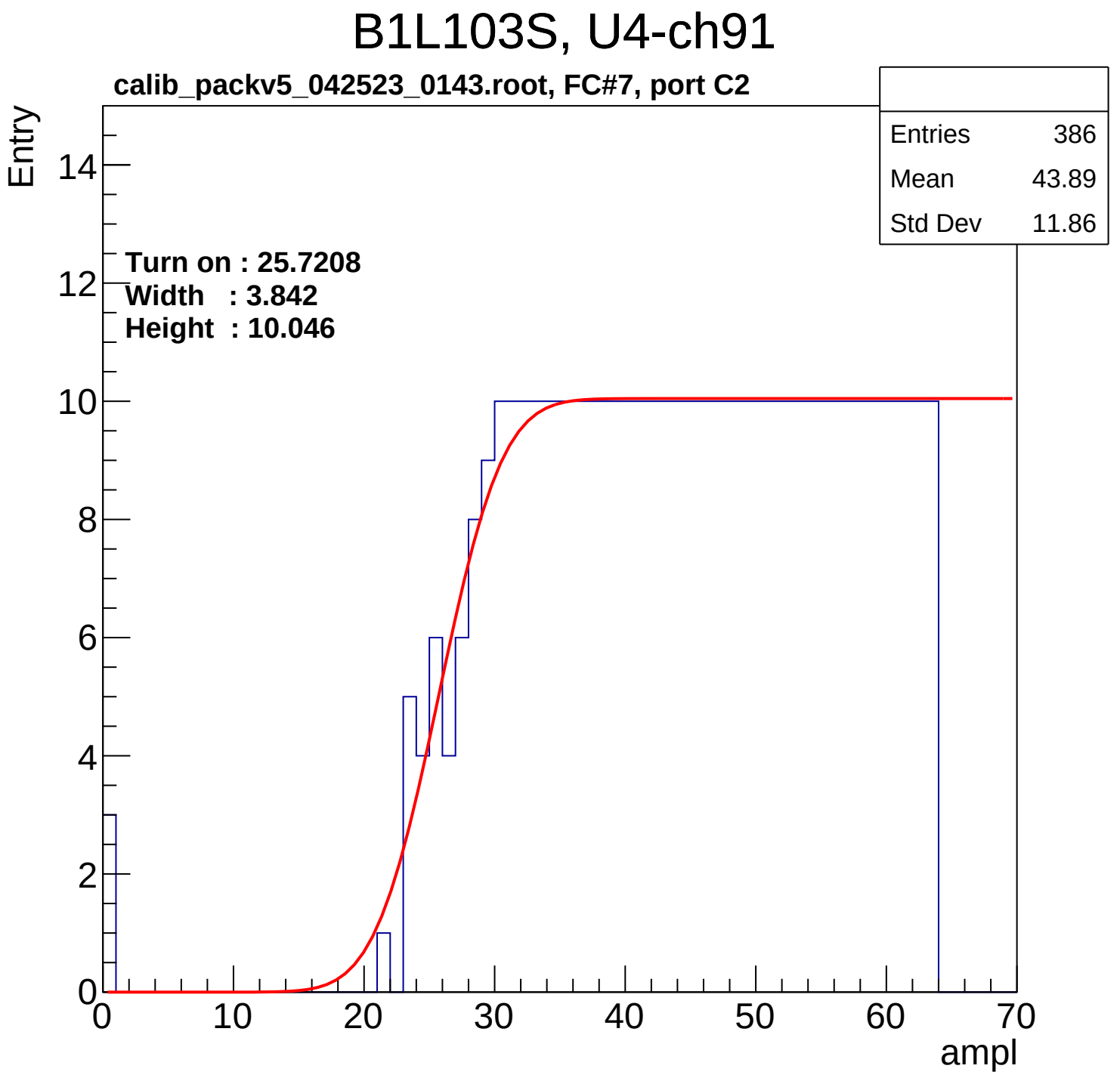
B1L103S, U4-ch91
calib_packv5_042523_0143.root, FC#7, port C2
Entries 386
Mean 43.89
Std Dev 11.86
Turn on : 25.7208
Width : 3.842
Height : 10.046
Entry
ampl
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6
8
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12
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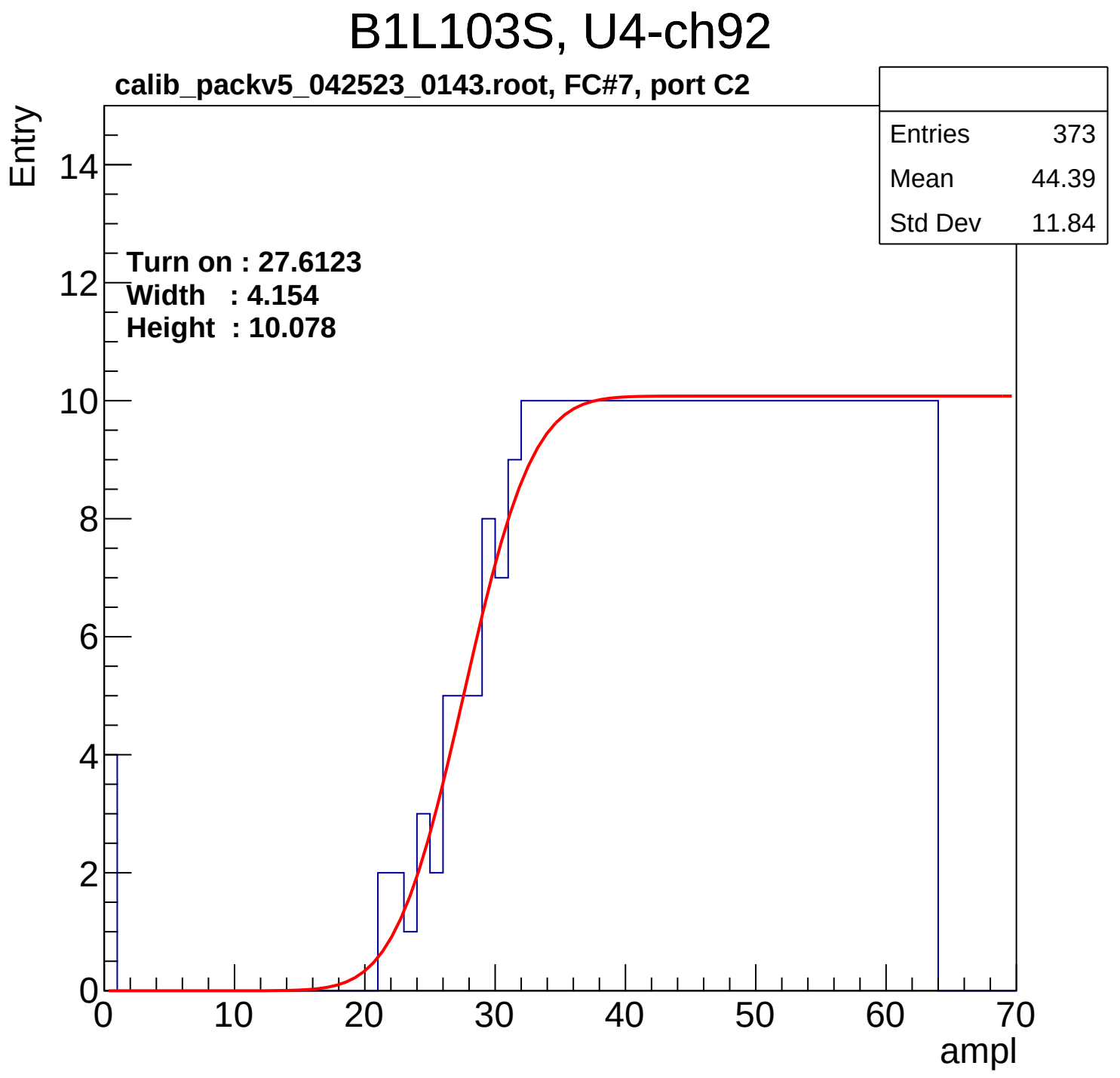
B1L103S, U4-ch92
calib_packv5_042523_0143.root, FC#7, port C2
Entries 373
Mean 44.39
Std Dev 11.84
Turn on : 27.6123
Width : 4.154
Height : 10.078
Entry
ampl
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4
6
8
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12
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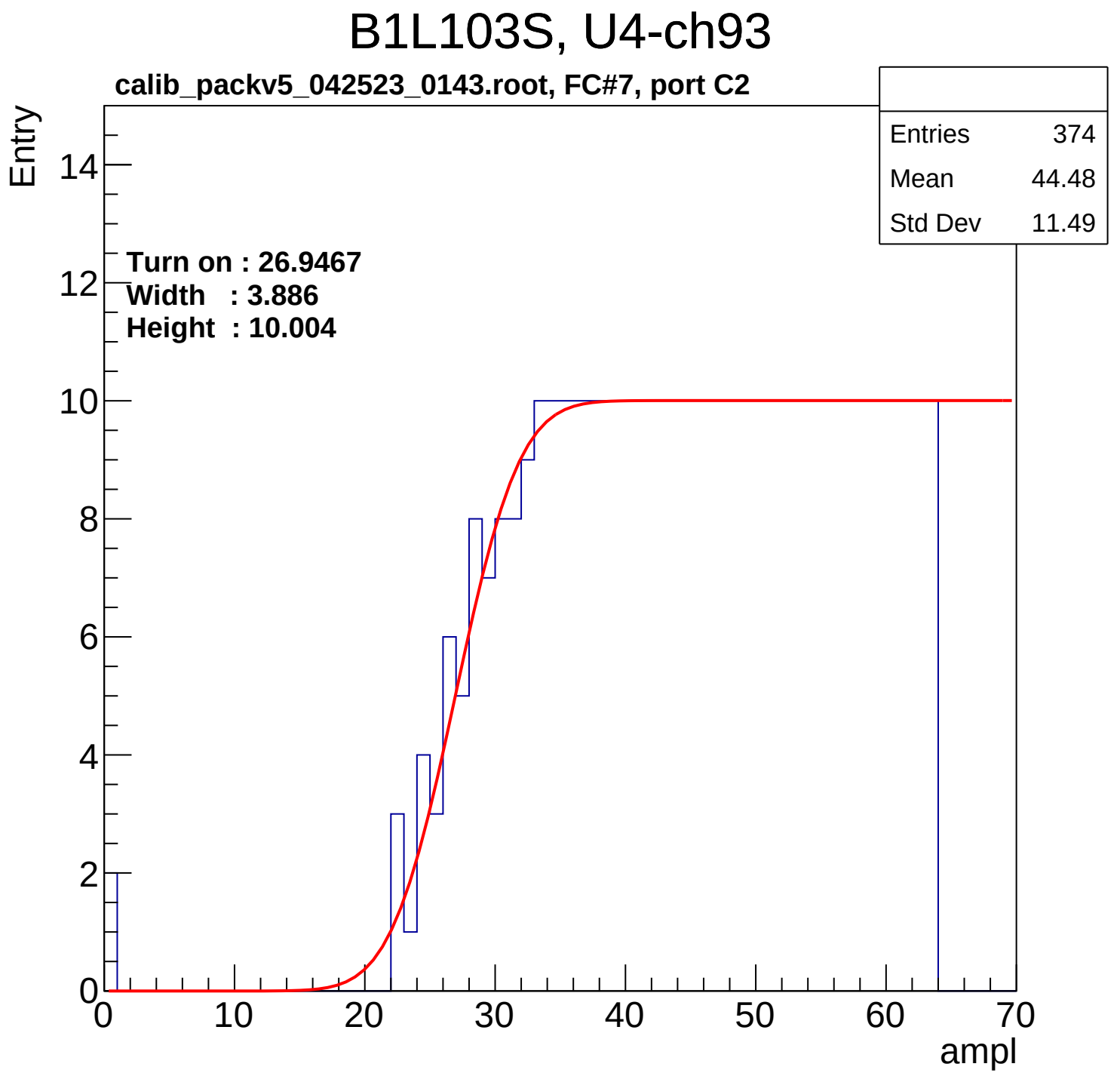
B1L103S, U4-ch93
calib_packv5_042523_0143.root, FC#7, port C2
Entries 374
Mean 44.48
Std Dev 11.49
Turn on : 26.9467
Width : 3.886
Height : 10.004
Entry
ampl
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6
8
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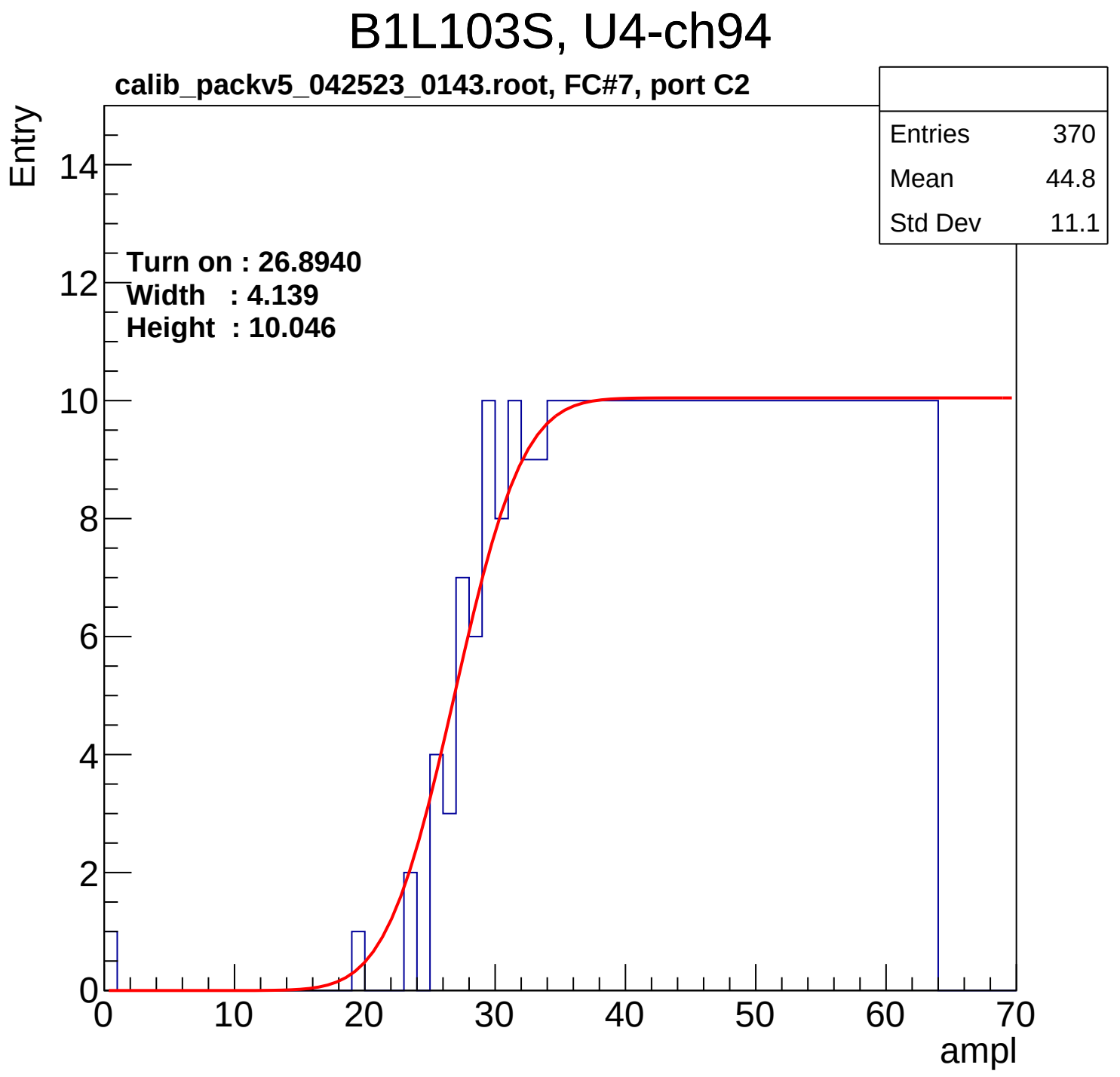
B1L103S, U4-ch94
calib_packv5_042523_0143.root, FC#7, port C2
Entries 370
Mean 44.8
Std Dev 11.1
Turn on : 26.8940
Width : 4.139
Height : 10.046
Entry
ampl
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2
4
6
8
10
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0
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60
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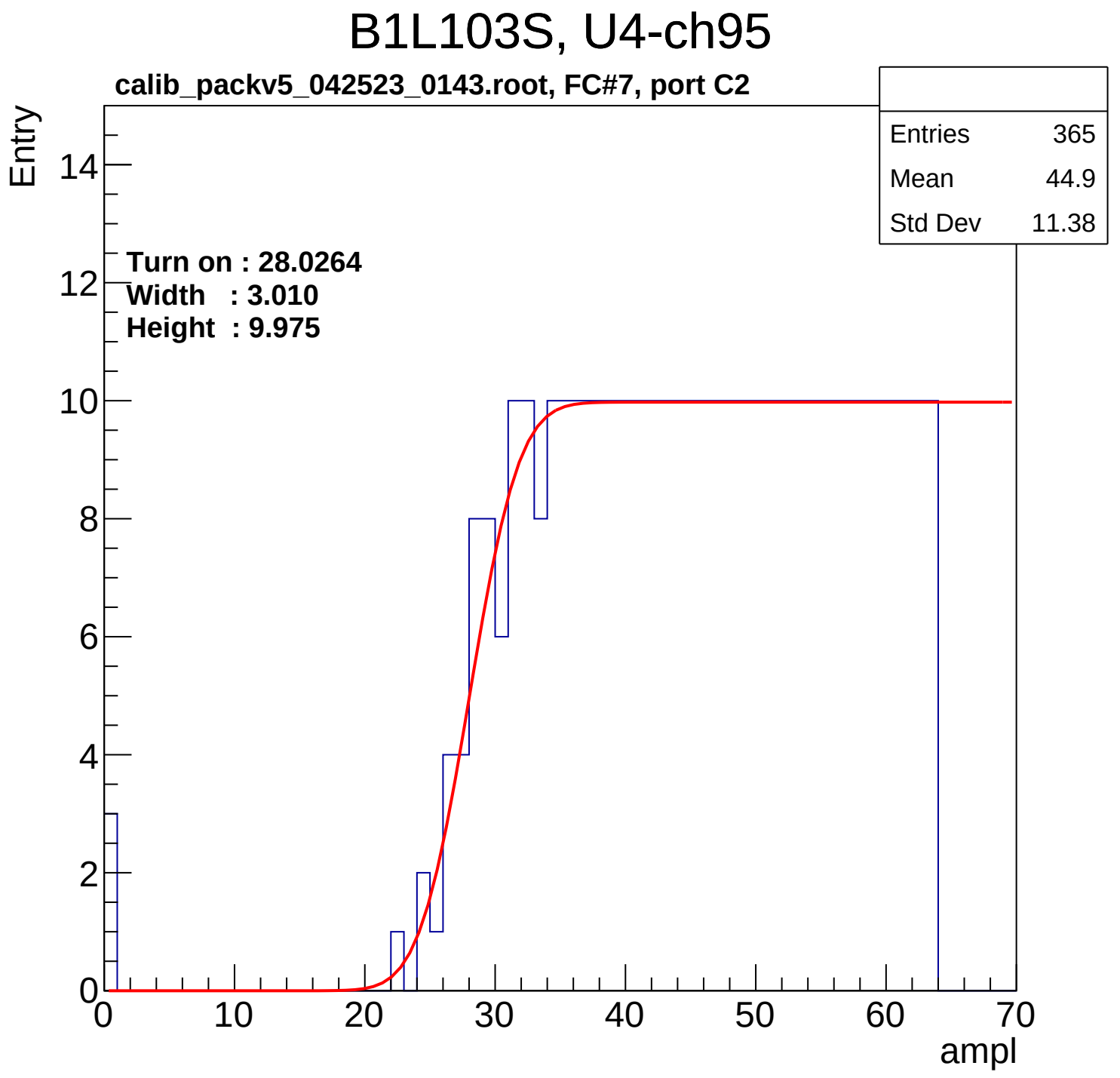
B1L103S, U4-ch95
calib_packv5_042523_0143.root, FC#7, port C2
Entries 365
Mean 44.9
Std Dev 11.38
Turn on : 28.0264
Width : 3.010
Height : 9.975
Entry
ampl
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4
6
8
10
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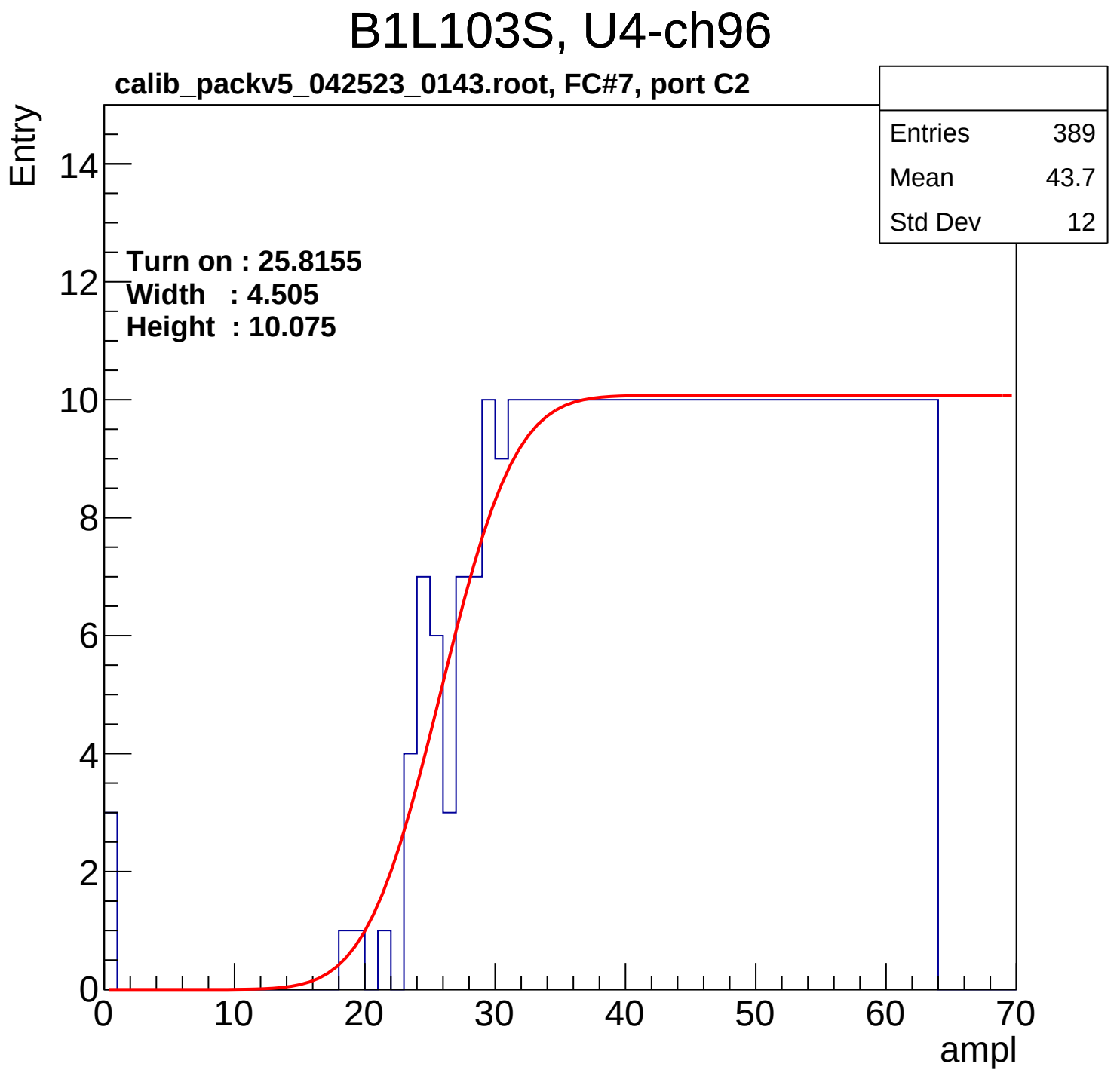
B1L103S, U4-ch96
calib_packv5_042523_0143.root, FC#7, port C2
Entries 389
Mean 43.7
Std Dev 12
Turn on : 25.8155
Width : 4.505
Height : 10.075
Entry
ampl
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2
4
6
8
10
12
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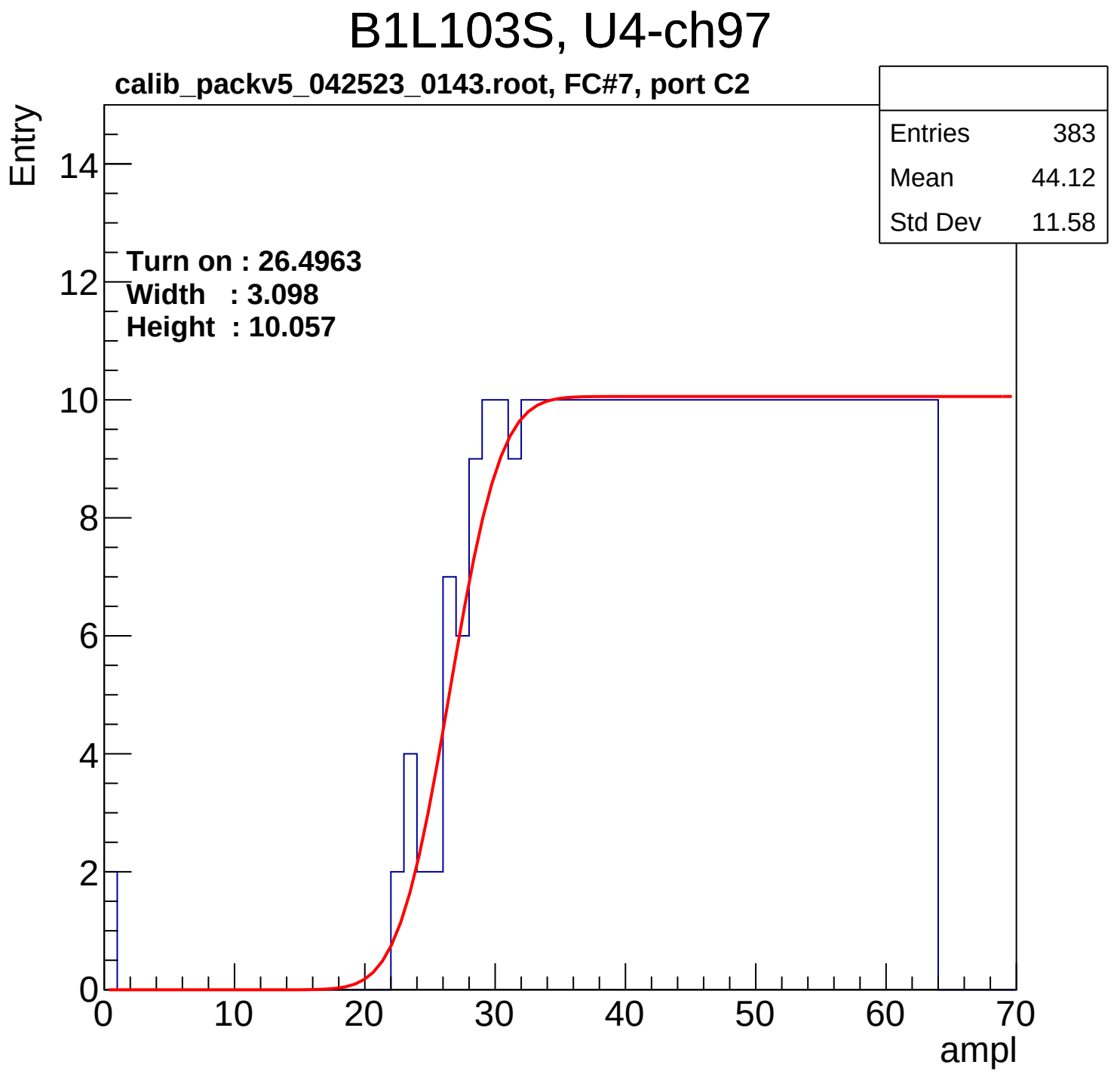
B1L103S, U4-ch97
calib_packv5_042523_0143.root, FC#7, port C2
Entries 383
Mean 44.12
Std Dev 11.58
Turn on : 26.4963
Width : 3.098
Height : 10.057
Entry
ampl
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2
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6
8
10
12
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0
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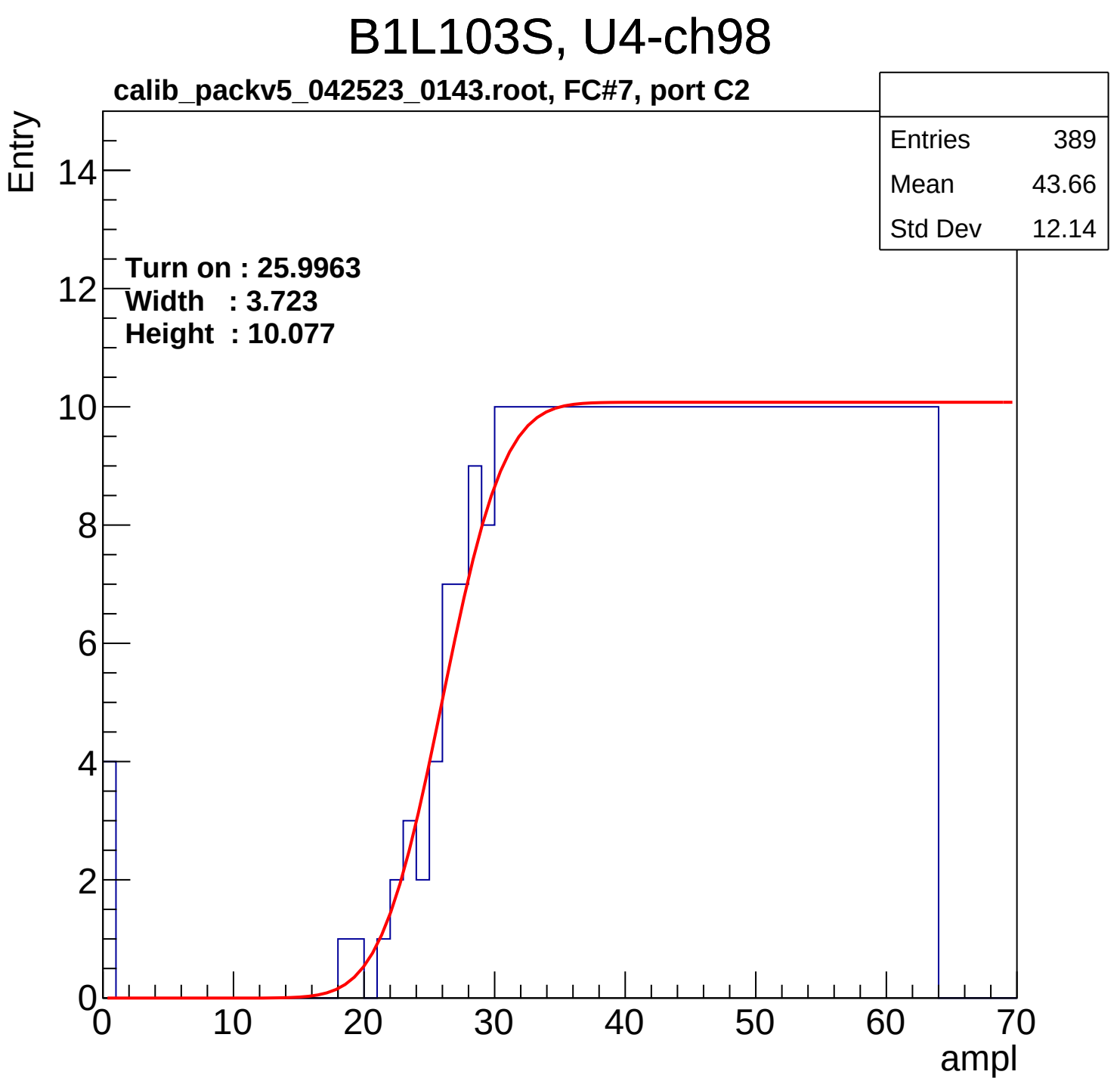
B1L103S, U4-ch98
calib_packv5_042523_0143.root, FC#7, port C2
Entries 389
Mean 43.66
Std Dev 12.14
Turn on : 25.9963
Width : 3.723
Height : 10.077
Entry
ampl
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2
4
6
8
10
12
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0
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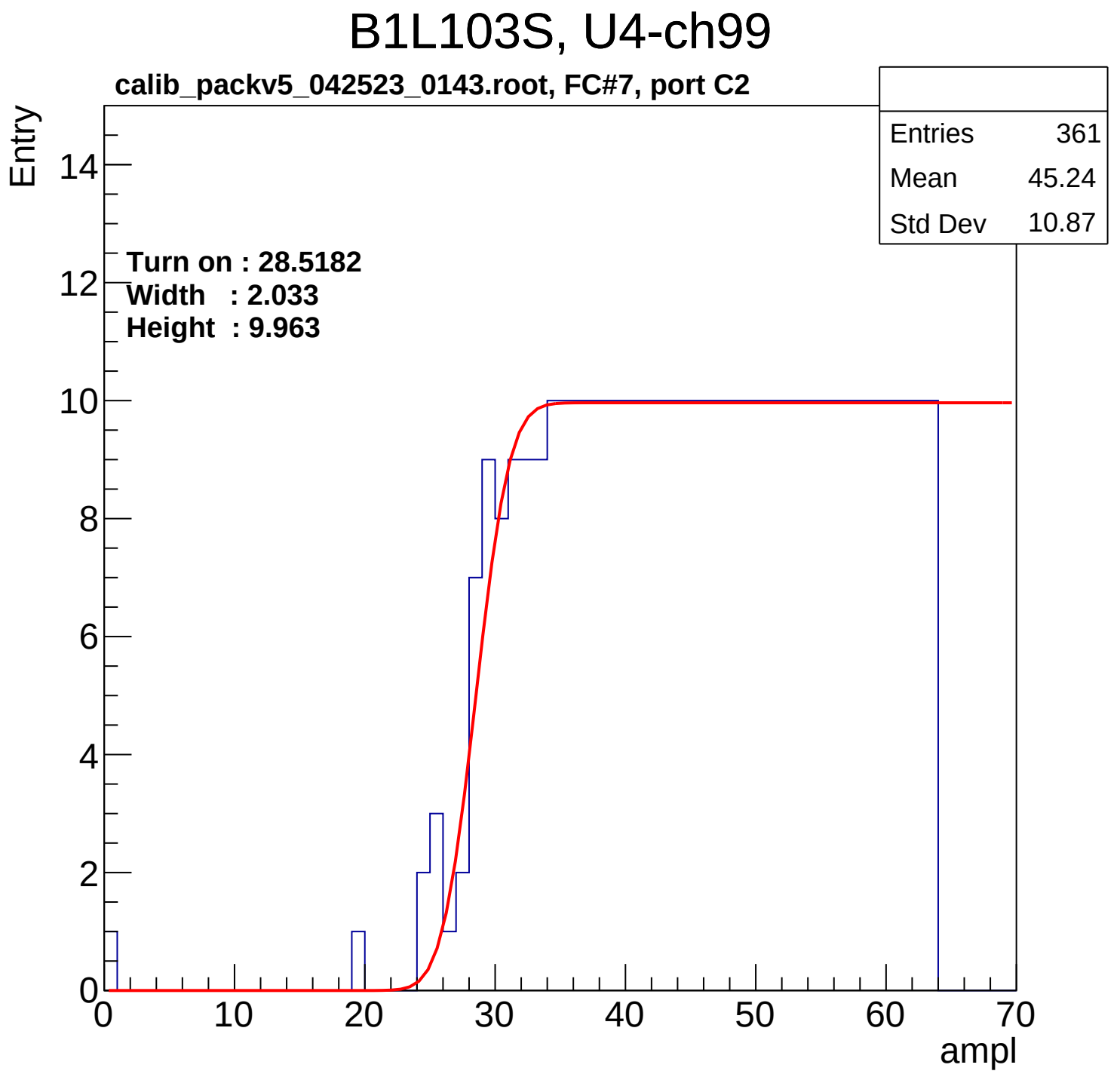
B1L103S, U4-ch99
calib_packv5_042523_0143.root, FC#7, port C2
Entries 361
Mean 45.24
Std Dev 10.87
Turn on : 28.5182
Width : 2.033
Height : 9.963
Entry
ampl
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6
8
10
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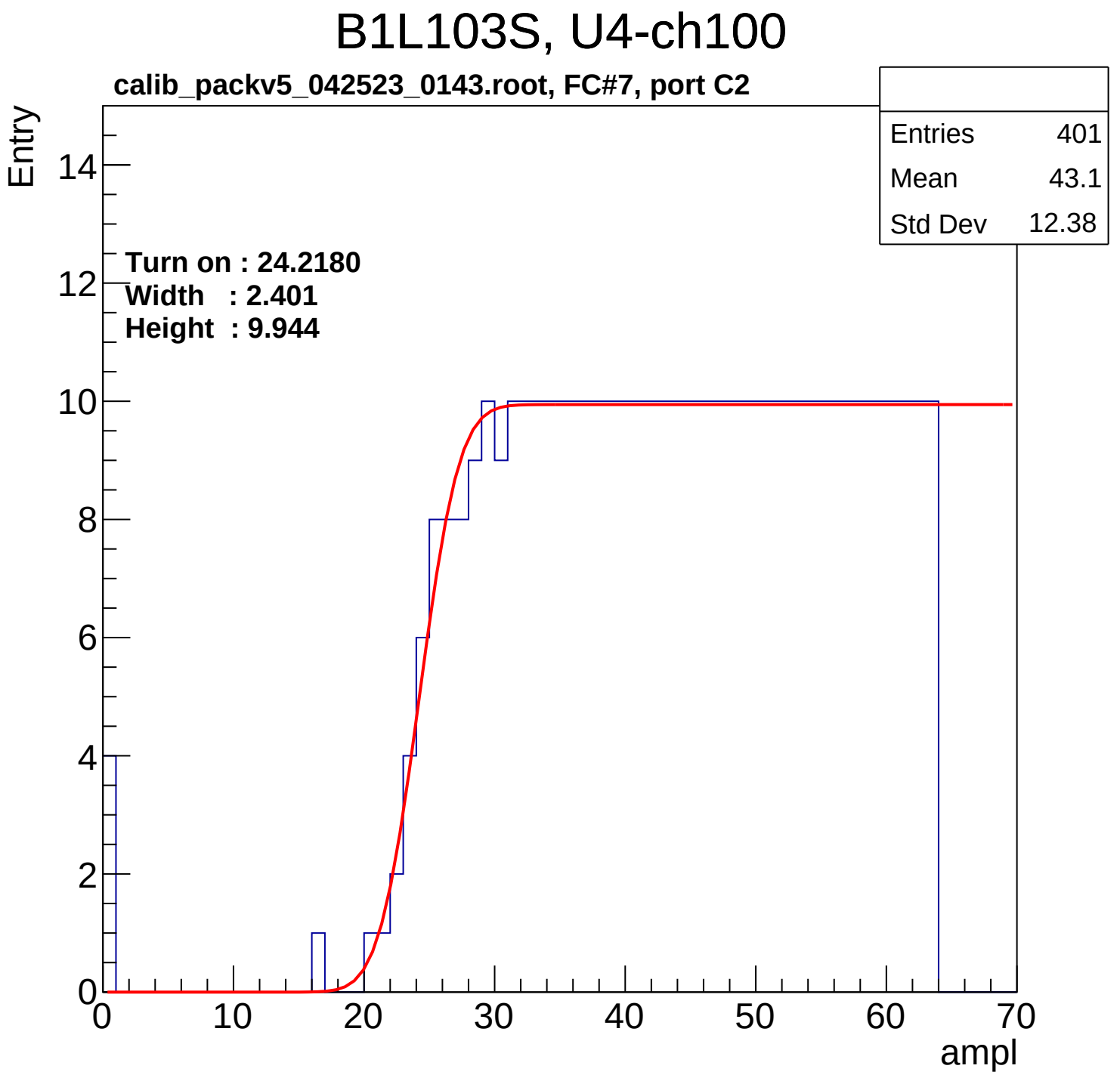
B1L103S, U4-ch100
calib_packv5_042523_0143.root, FC#7, port C2
Entries 401
Mean 43.1
Std Dev 12.38
Turn on : 24.2180
Width : 2.401
Height : 9.944
Entry
ampl
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2
4
6
8
10
12
14
0
10
20
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60
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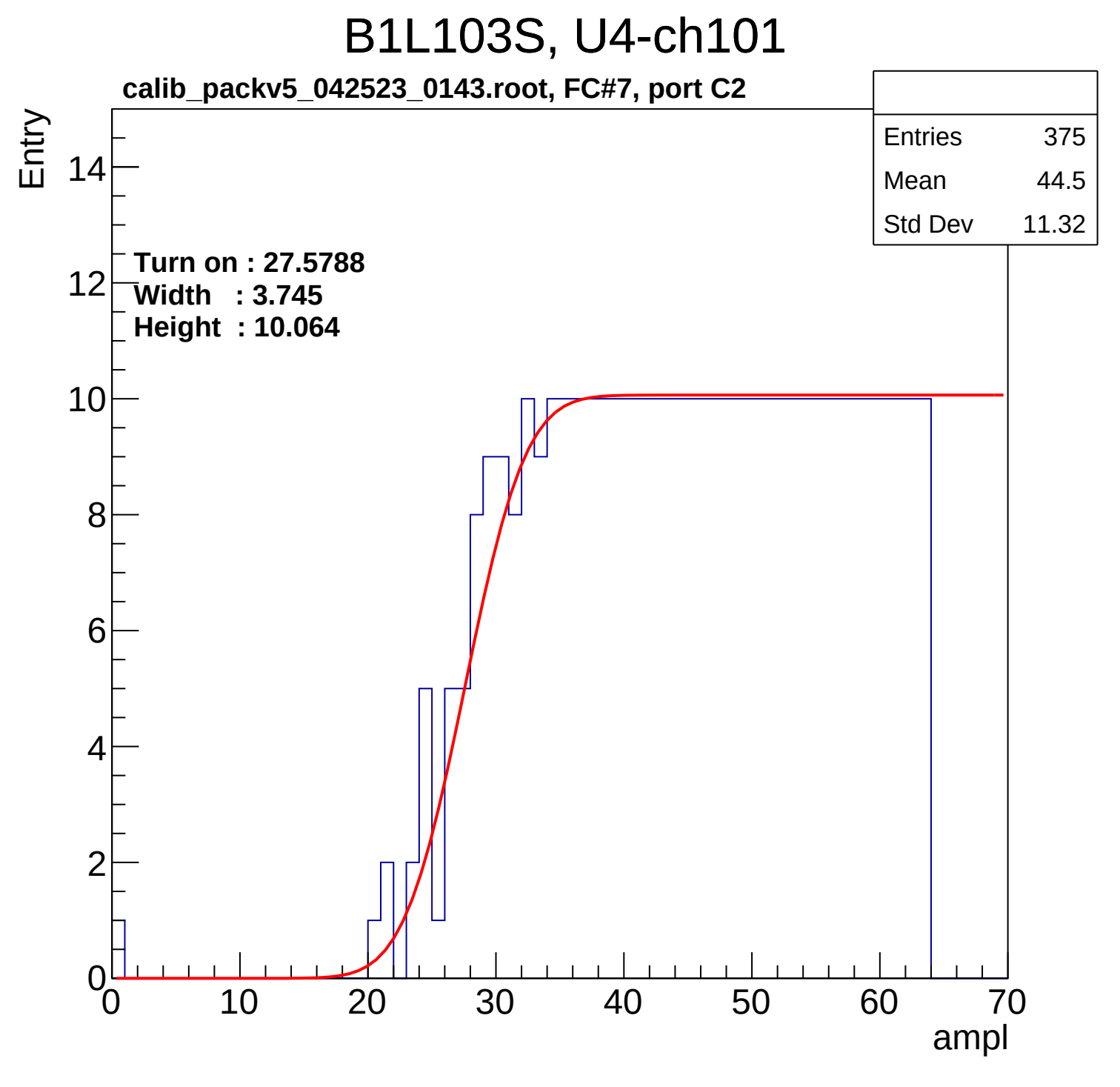
B1L103S, U4-ch101
calib_packv5_042523_0143.root, FC#7, port C2
Entries 375
Mean 44.5
Std Dev 11.32
Turn on : 27.5788
Width : 3.745
Height : 10.064
Entry
ampl
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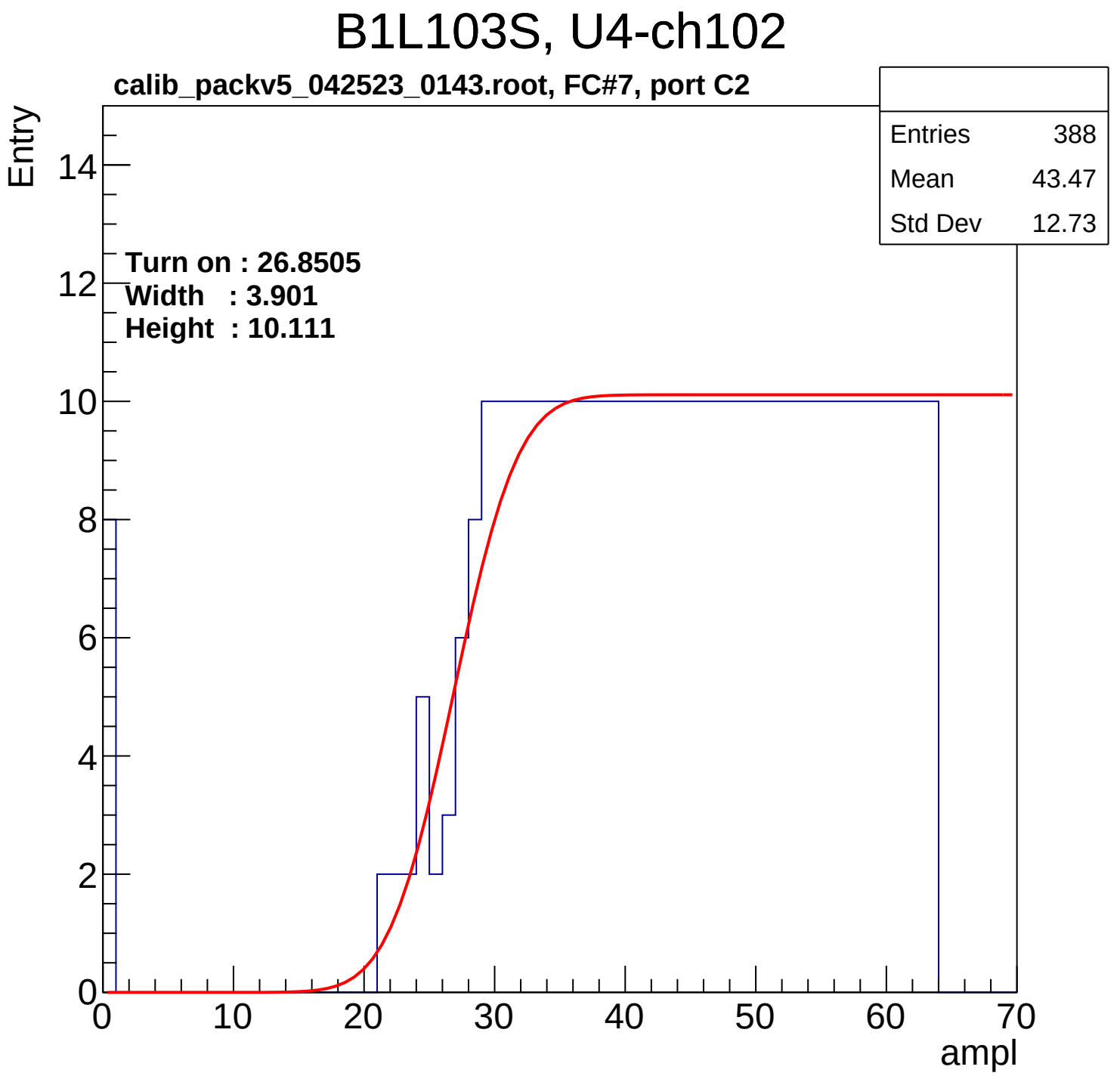
B1L103S, U4-ch102
calib_packv5_042523_0143.root, FC#7, port C2
Entries 388
Mean 43.47
Std Dev 12.73
Turn on : 26.8505
Width : 3.901
Height : 10.111
Entry
ampl
0
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6
8
10
12
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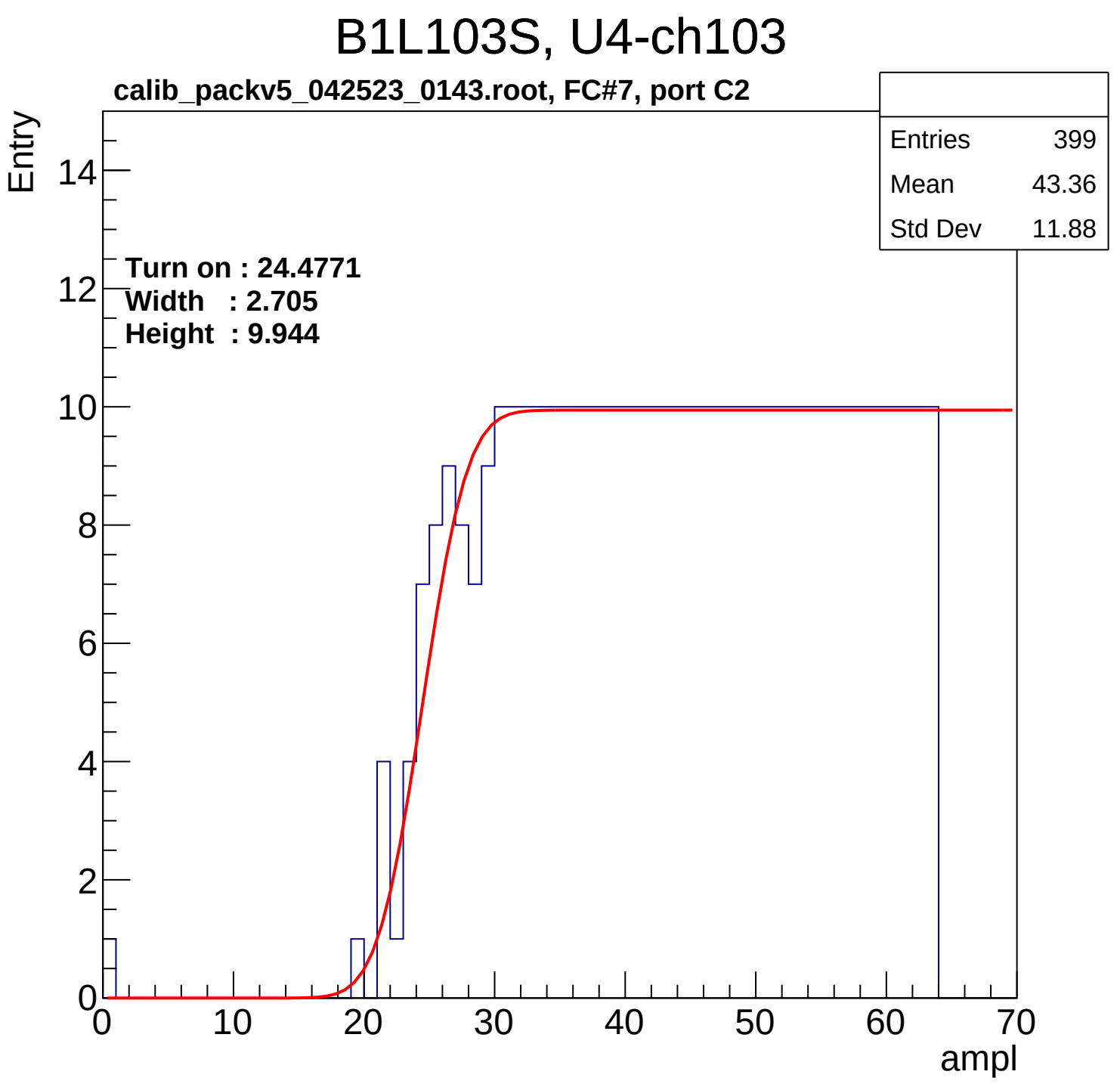
B1L103S, U4-ch103
calib_packv5_042523_0143.root, FC#7, port C2
Entries 399
Mean 43.36
Std Dev 11.88
Turn on : 24.4771
Width : 2.705
Height : 9.944
Entry
ampl
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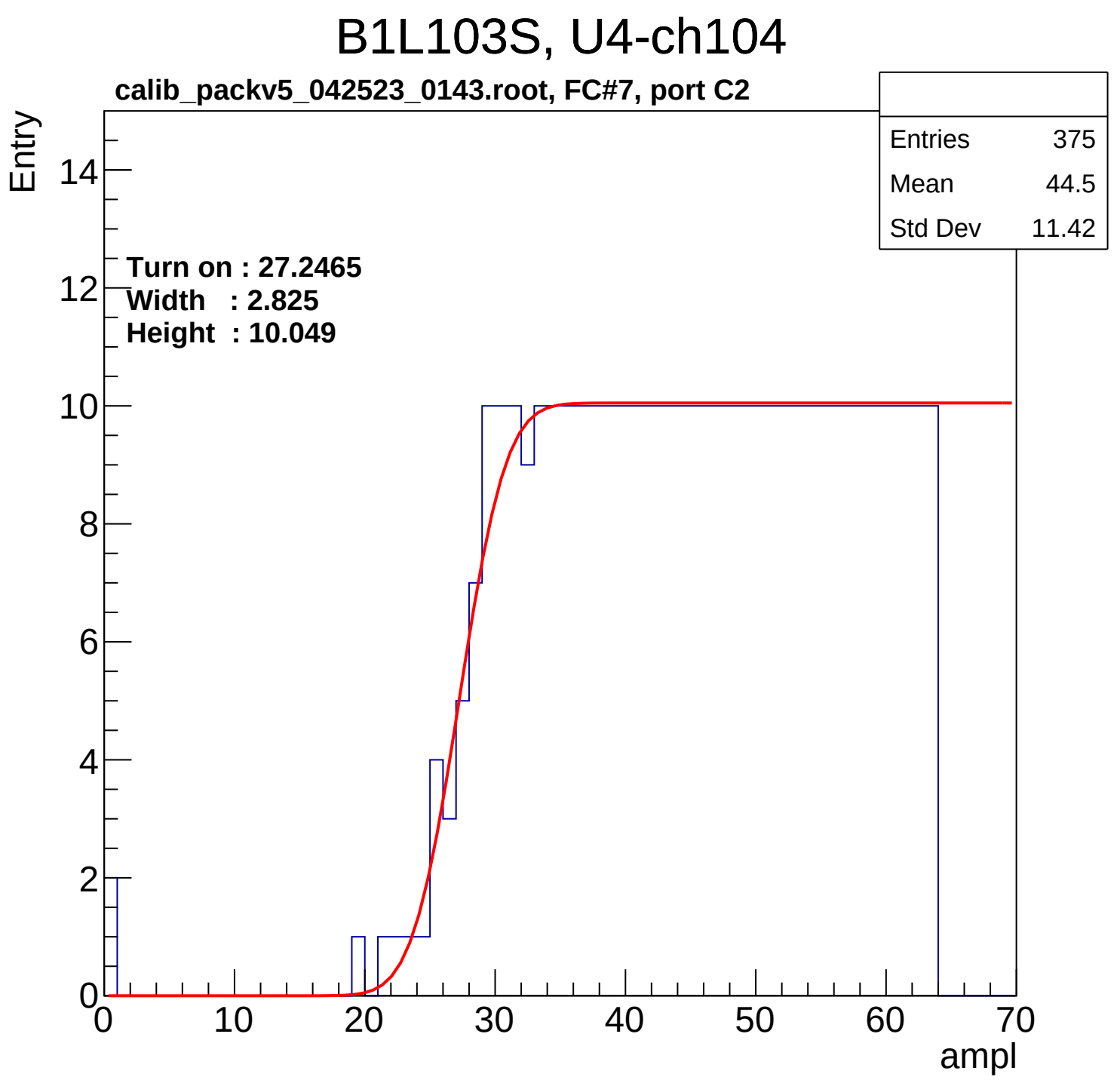
B1L103S, U4-ch104
calib_packv5_042523_0143.root, FC#7, port C2
Entries 375
Mean 44.5
Std Dev 11.42
Turn on : 27.2465
Width : 2.825
Height : 10.049
Entry
ampl
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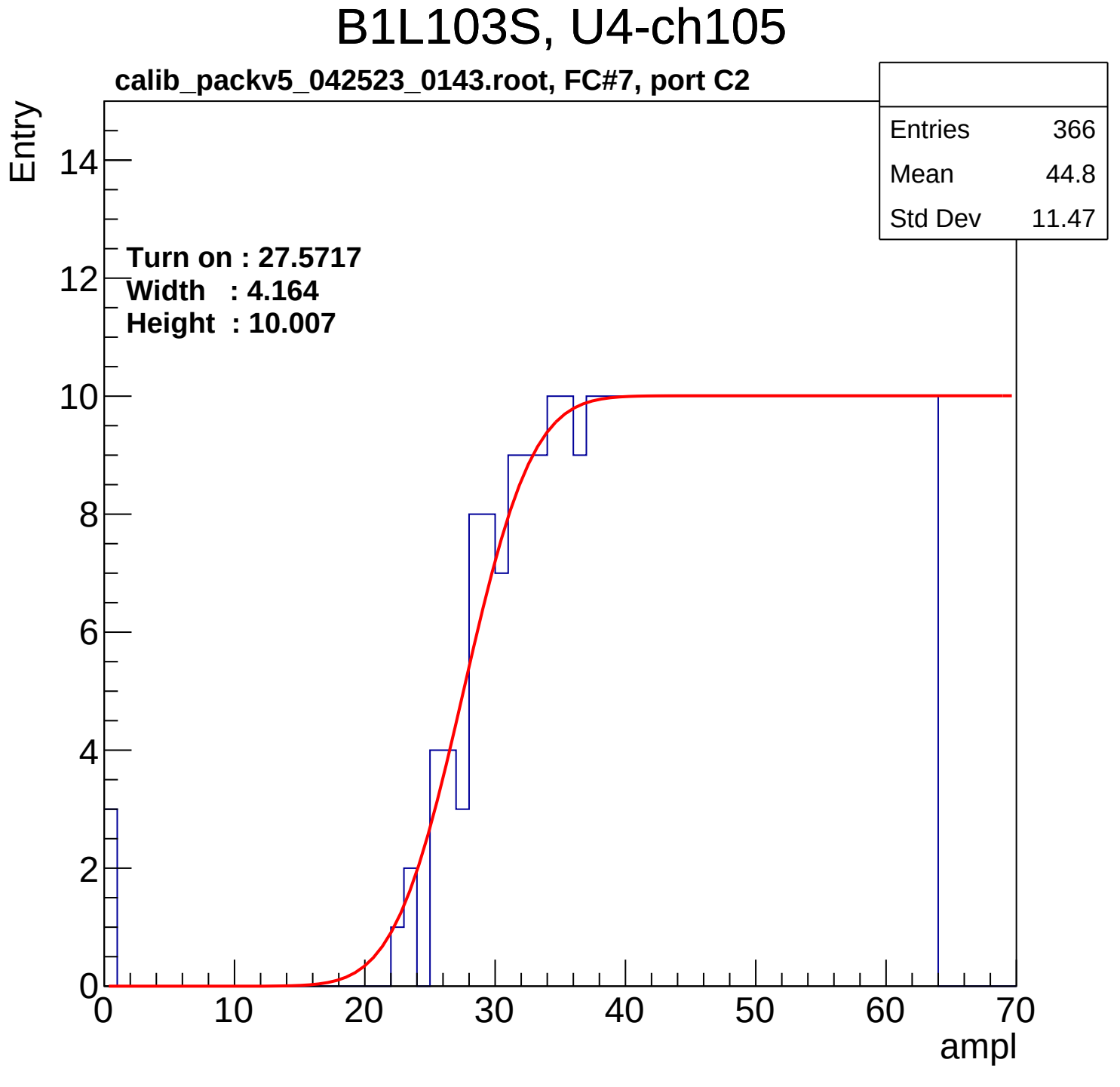
B1L103S, U4-ch105
calib_packv5_042523_0143.root, FC#7, port C2
Entries 366
Mean 44.8
Std Dev 11.47
Turn on : 27.5717
Width : 4.164
Height : 10.007
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ampl
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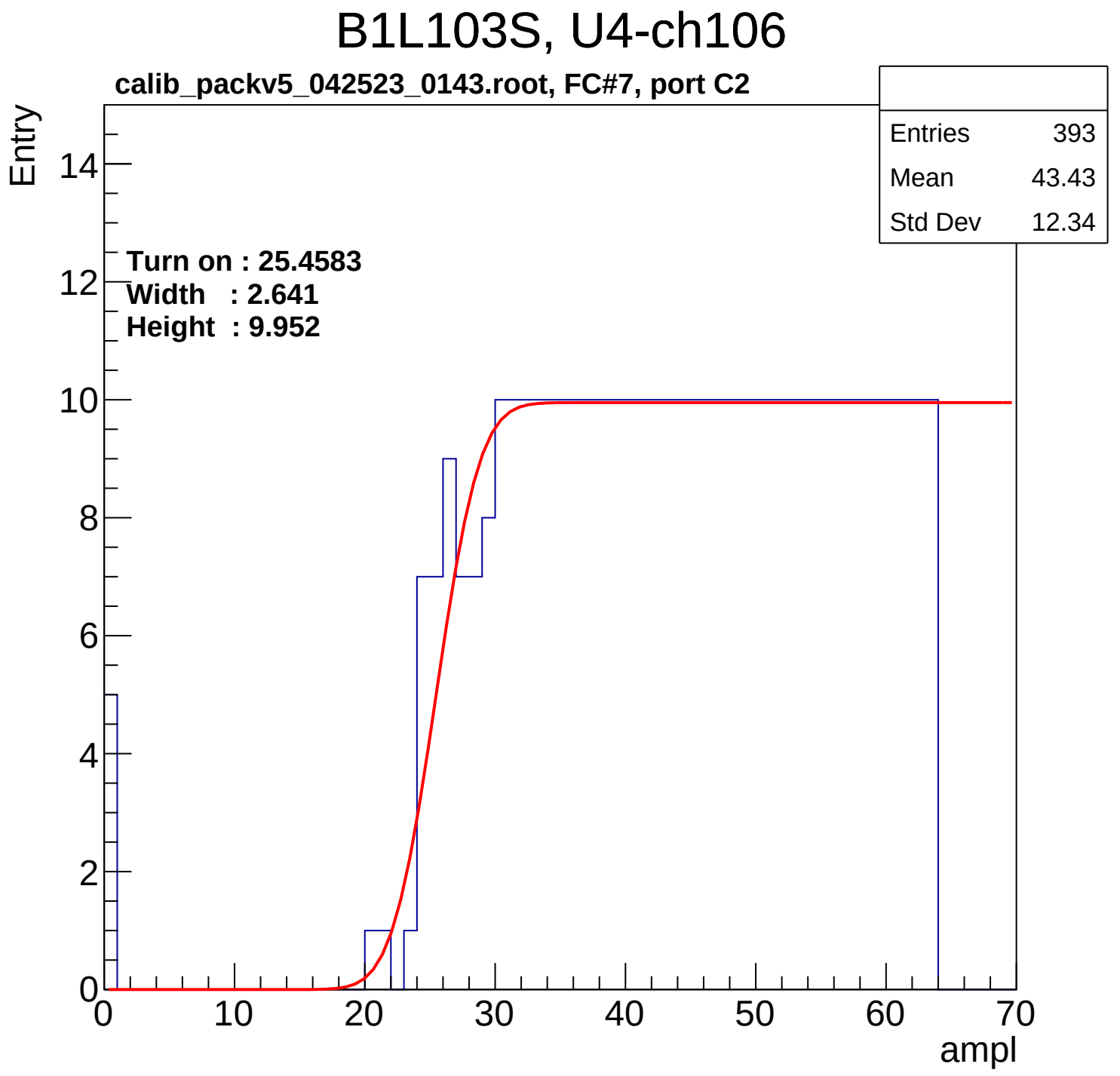
B1L103S, U4-ch106
calib_packv5_042523_0143.root, FC#7, port C2
Entries 393
Mean 43.43
Std Dev 12.34
Turn on : 25.4583
Width : 2.641
Height : 9.952
Entry
ampl
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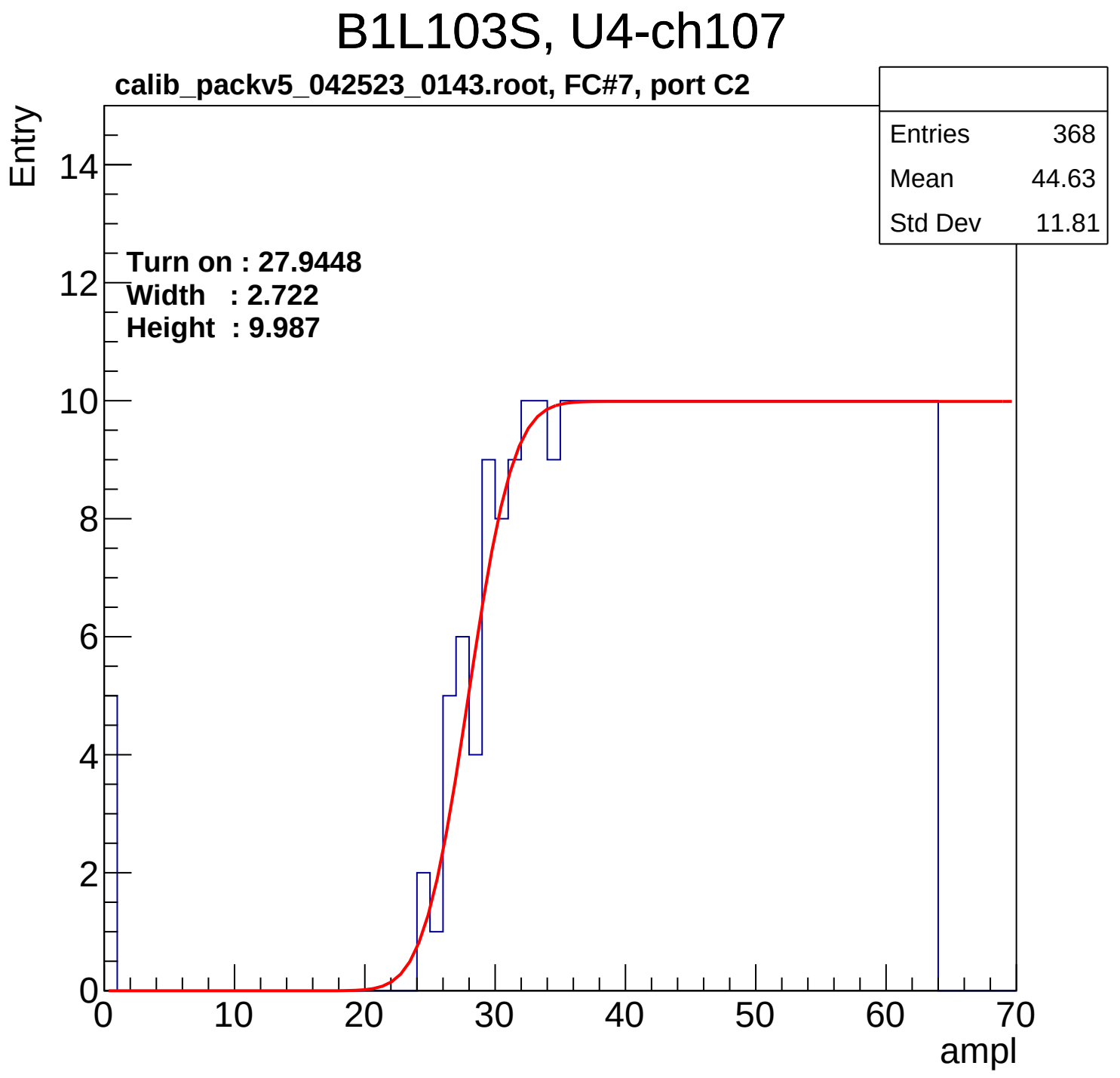
B1L103S, U4-ch107
calib_packv5_042523_0143.root, FC#7, port C2
Entries 368
Mean 44.63
Std Dev 11.81
Turn on : 27.9448
Width : 2.722
Height : 9.987
Entry
ampl
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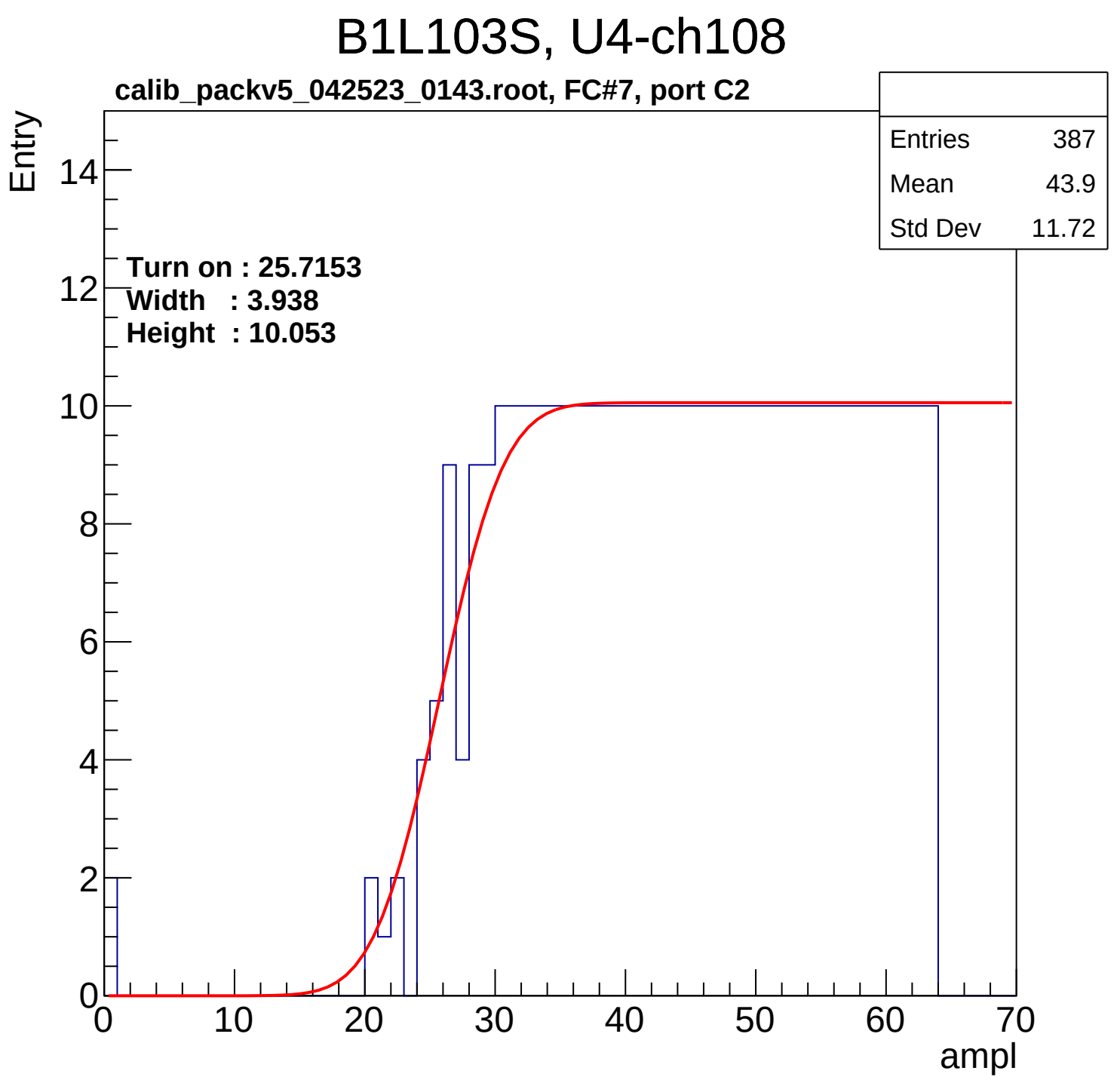
B1L103S, U4-ch108
calib_packv5_042523_0143.root, FC#7, port C2
Entries 387
Mean 43.9
Std Dev 11.72
Turn on : 25.7153
Width : 3.938
Height : 10.053
Entry
ampl
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6
8
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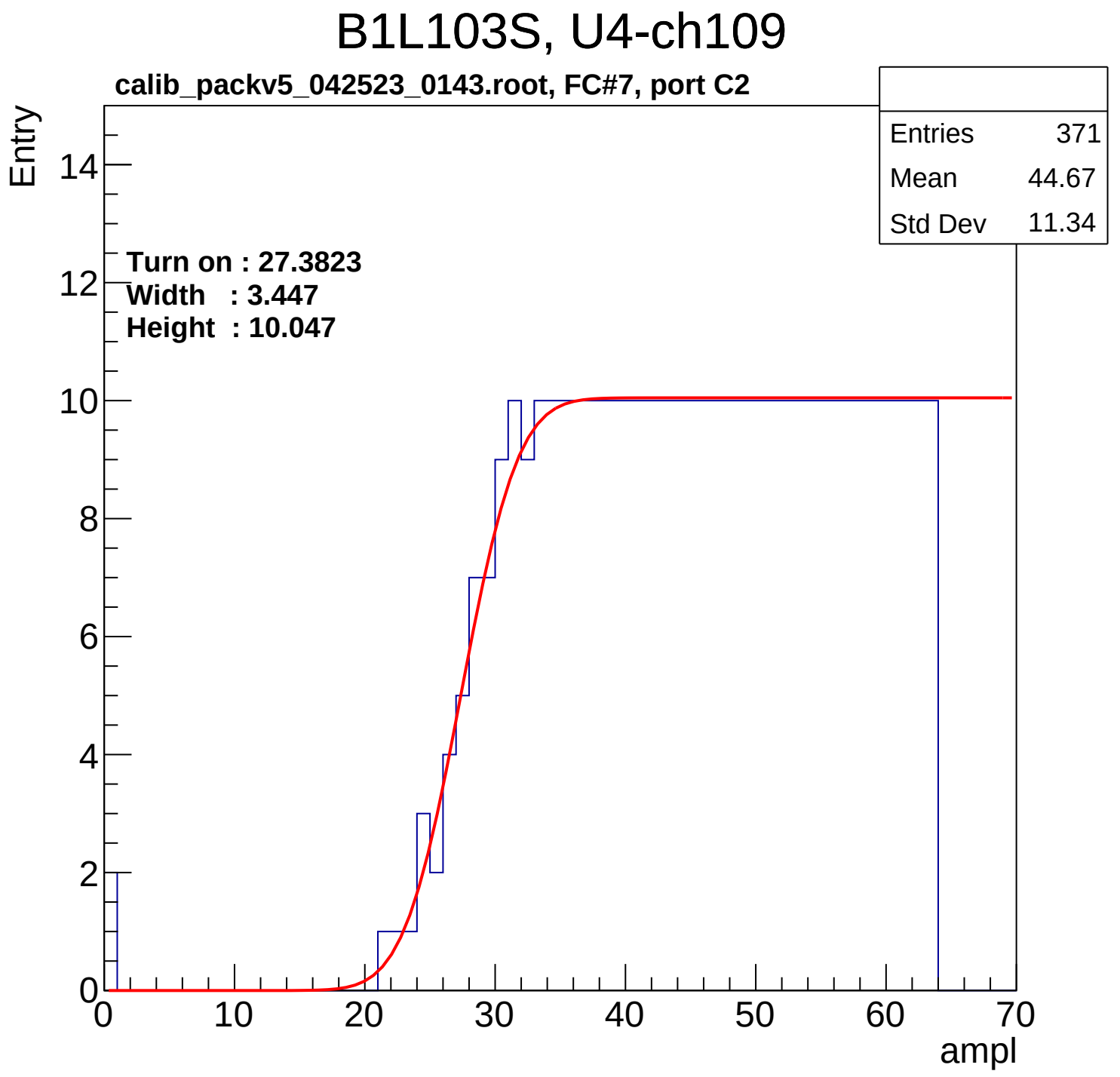
B1L103S, U4-ch109
calib_packv5_042523_0143.root, FC#7, port C2
Entries 371
Mean 44.67
Std Dev 11.34
Turn on : 27.3823
Width : 3.447
Height : 10.047
Entry
ampl
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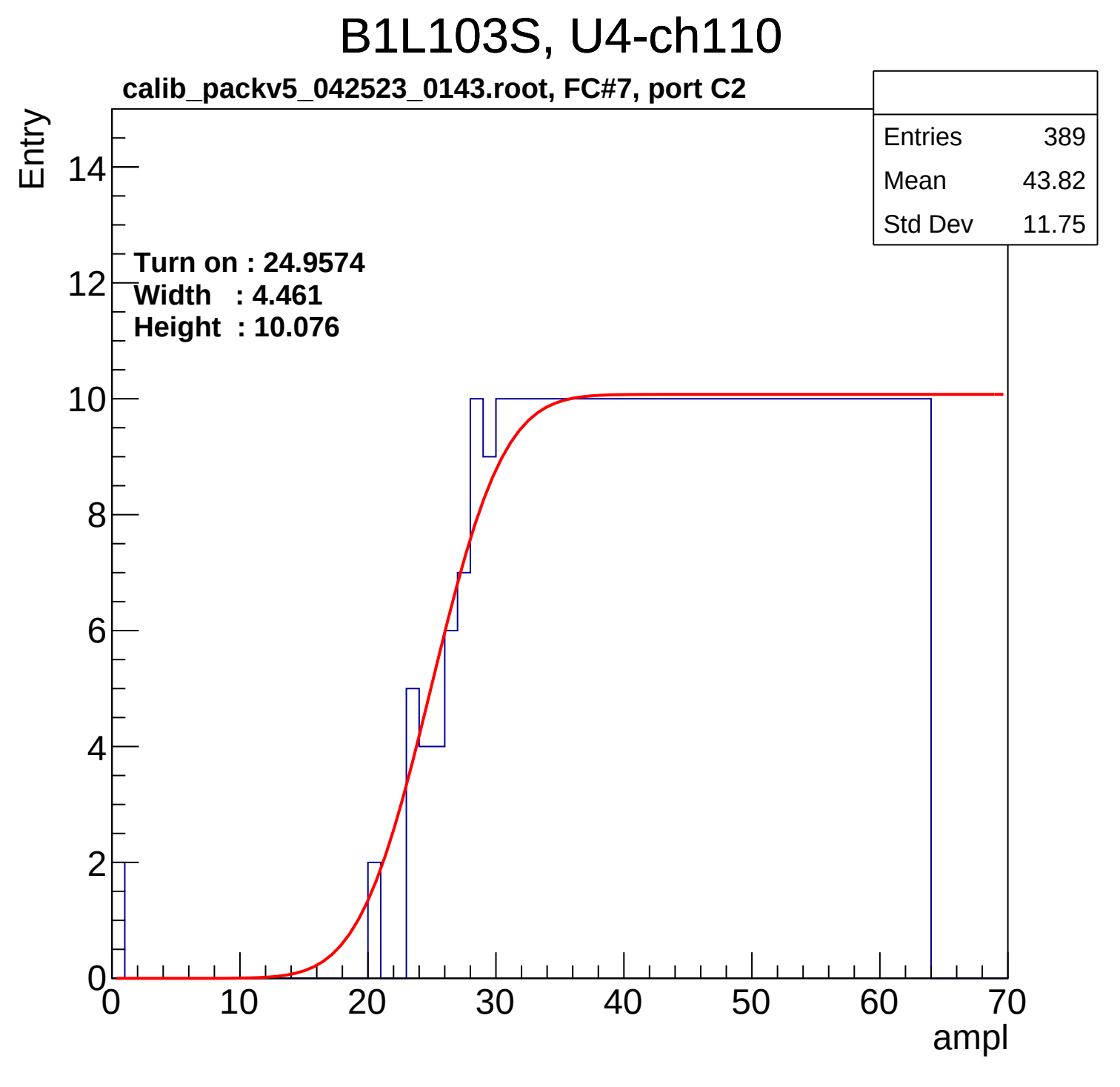
B1L103S, U4-ch110
calib_packv5_042523_0143.root, FC#7, port C2
Entries 389
Mean 43.82
Std Dev 11.75
Turn on : 24.9574
Width : 4.461
Height : 10.076
Entry
ampl
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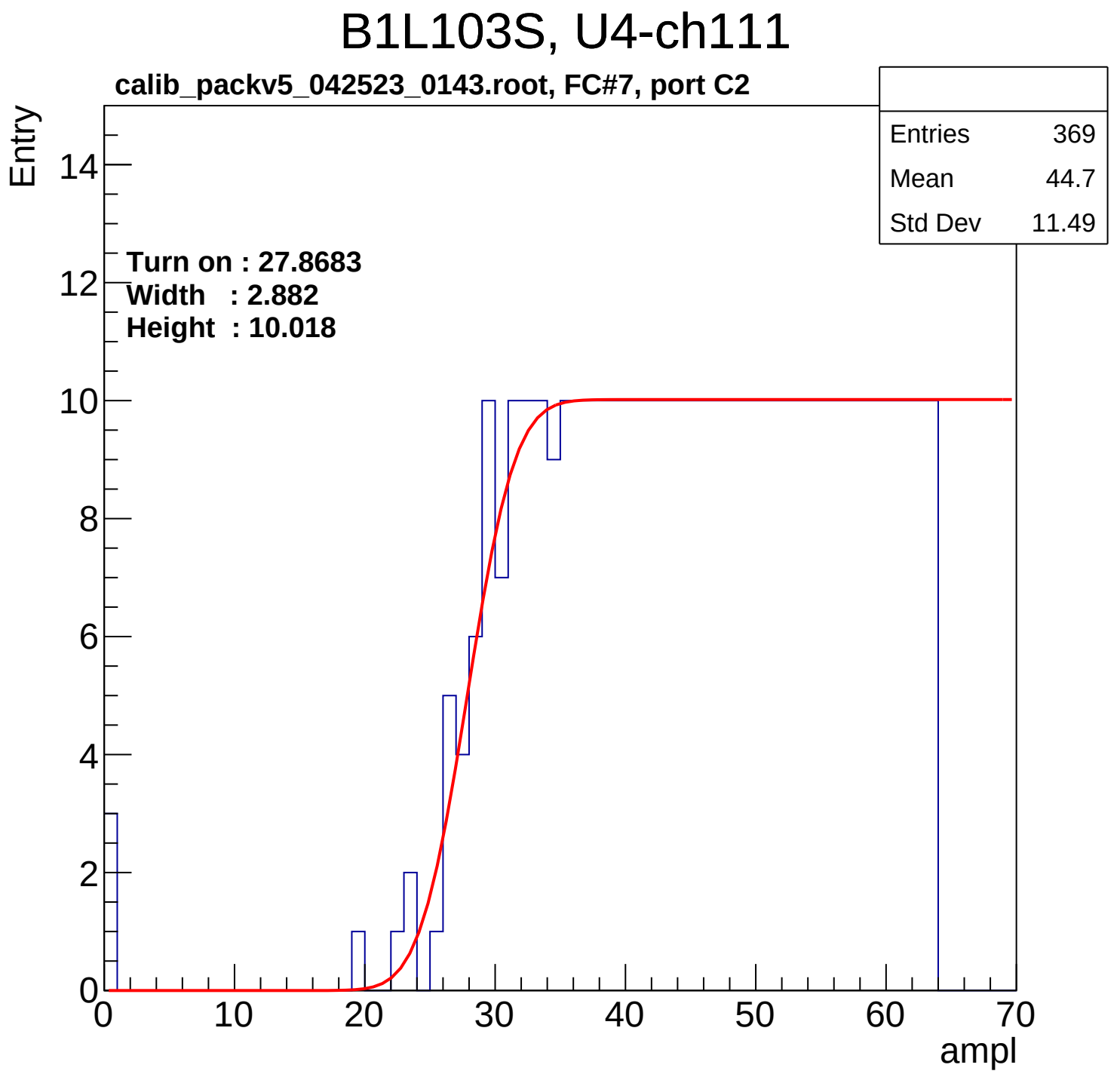
B1L103S, U4-ch111
calib_packv5_042523_0143.root, FC#7, port C2
Entries 369
Mean 44.7
Std Dev 11.49
Turn on : 27.8683
Width : 2.882
Height : 10.018
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ampl
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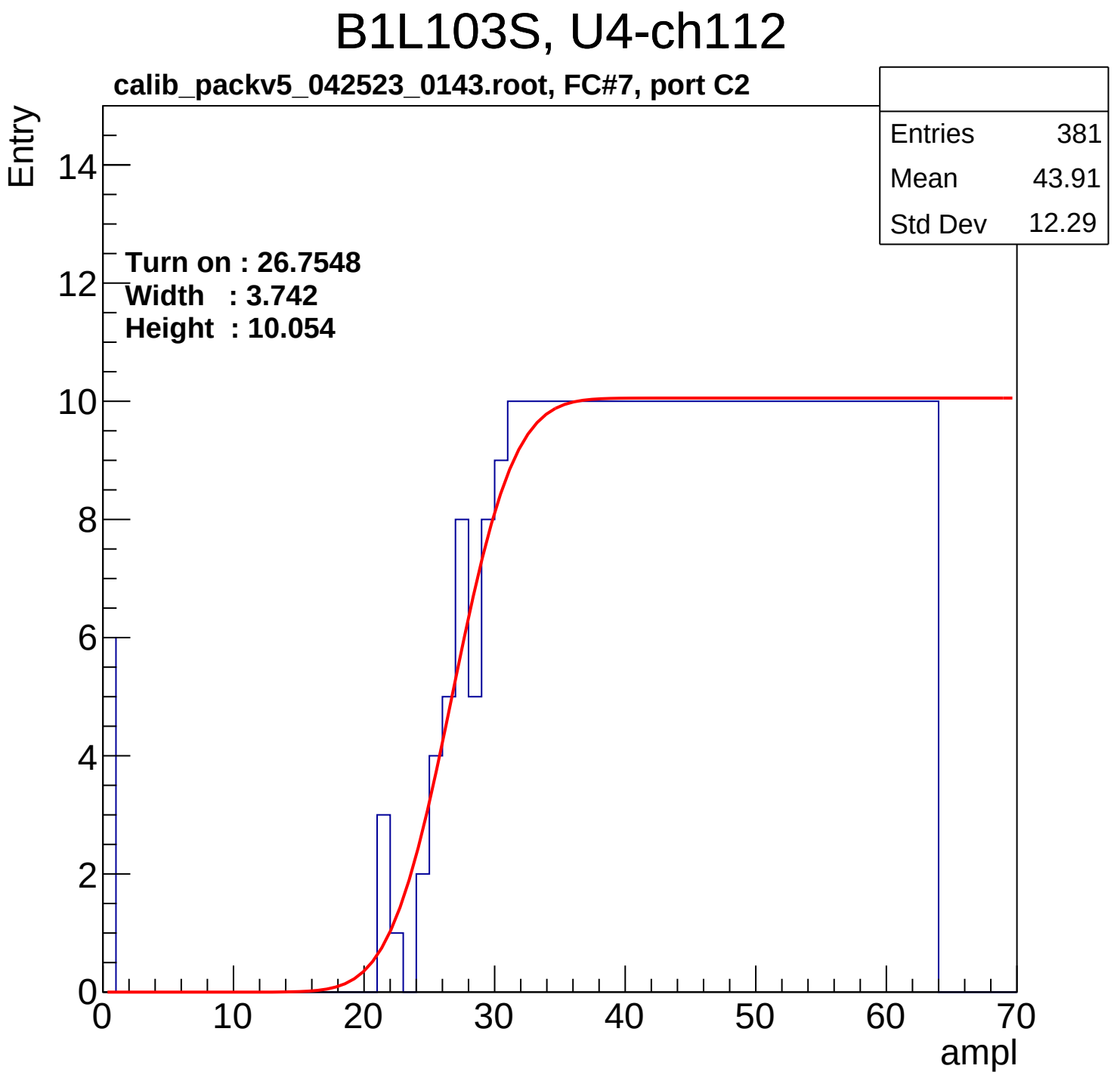
B1L103S, U4-ch112
calib_packv5_042523_0143.root, FC#7, port C2
Entries 381
Mean 43.91
Std Dev 12.29
Turn on : 26.7548
Width : 3.742
Height : 10.054
Entry
ampl
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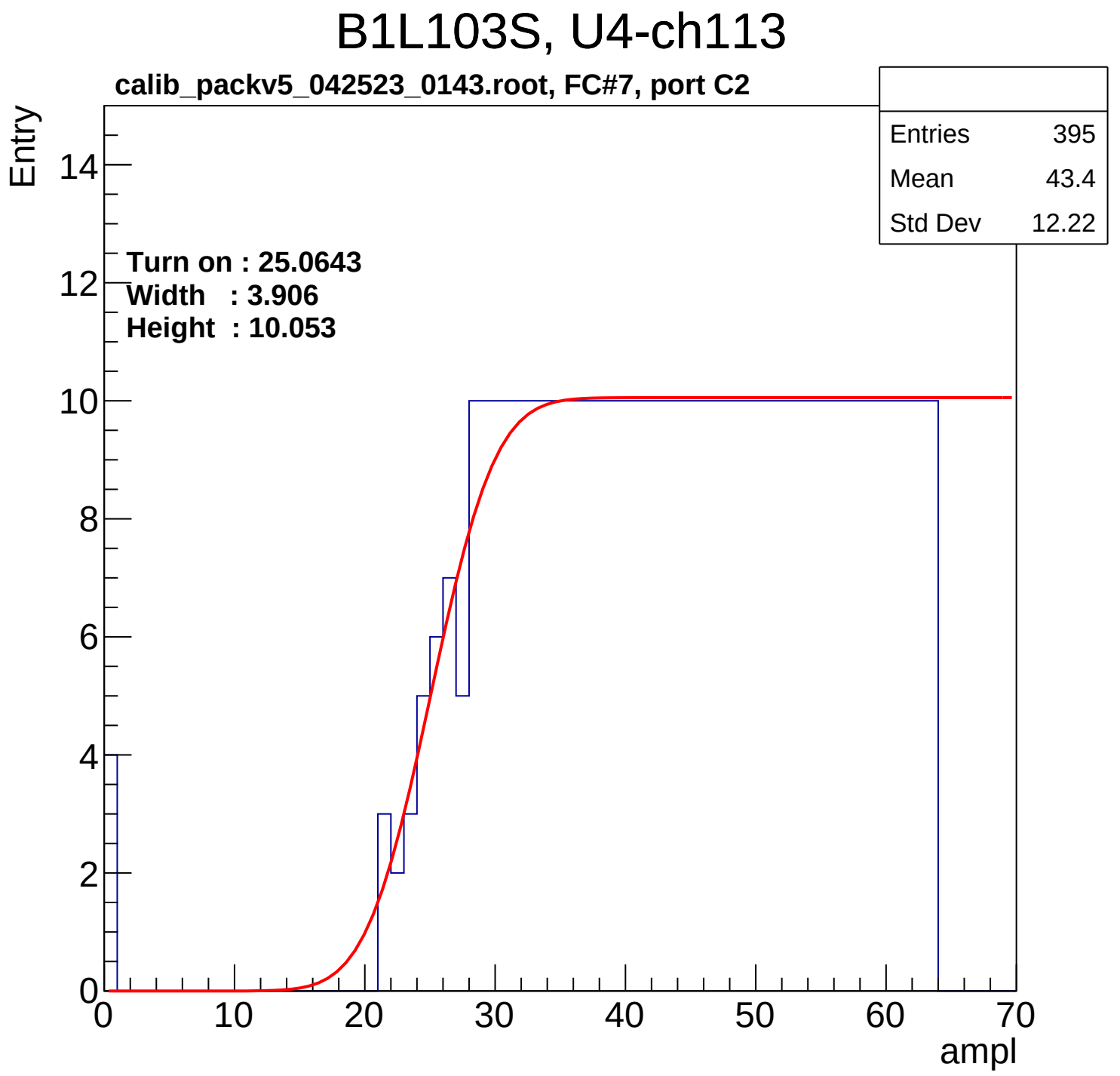
B1L103S, U4-ch113
calib_packv5_042523_0143.root, FC#7, port C2
Entries 395
Mean 43.4
Std Dev 12.22
Turn on : 25.0643
Width : 3.906
Height : 10.053
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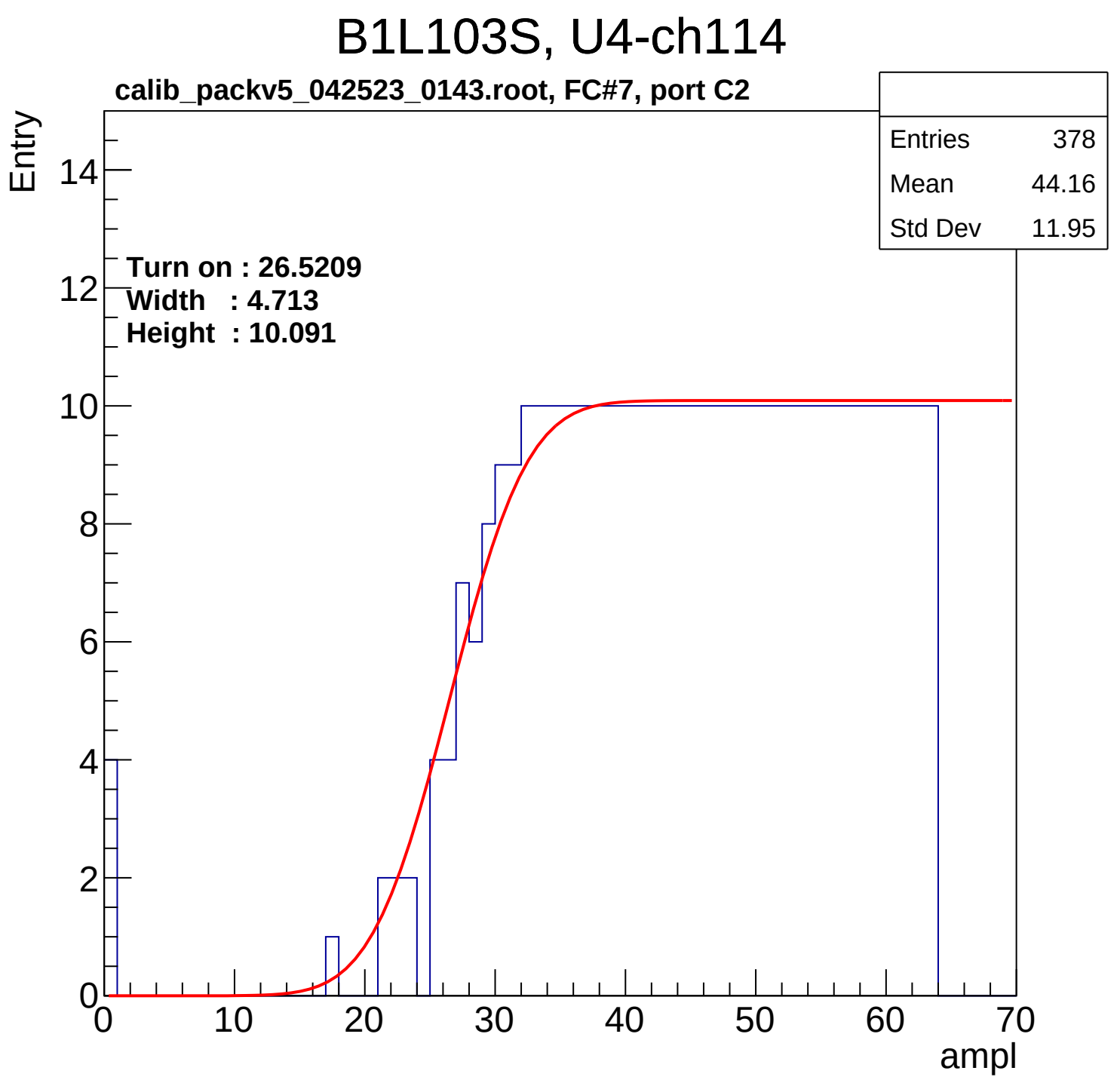
B1L103S, U4-ch114
calib_packv5_042523_0143.root, FC#7, port C2
Entries 378
Mean 44.16
Std Dev 11.95
Turn on : 26.5209
Width : 4.713
Height : 10.091
Entry
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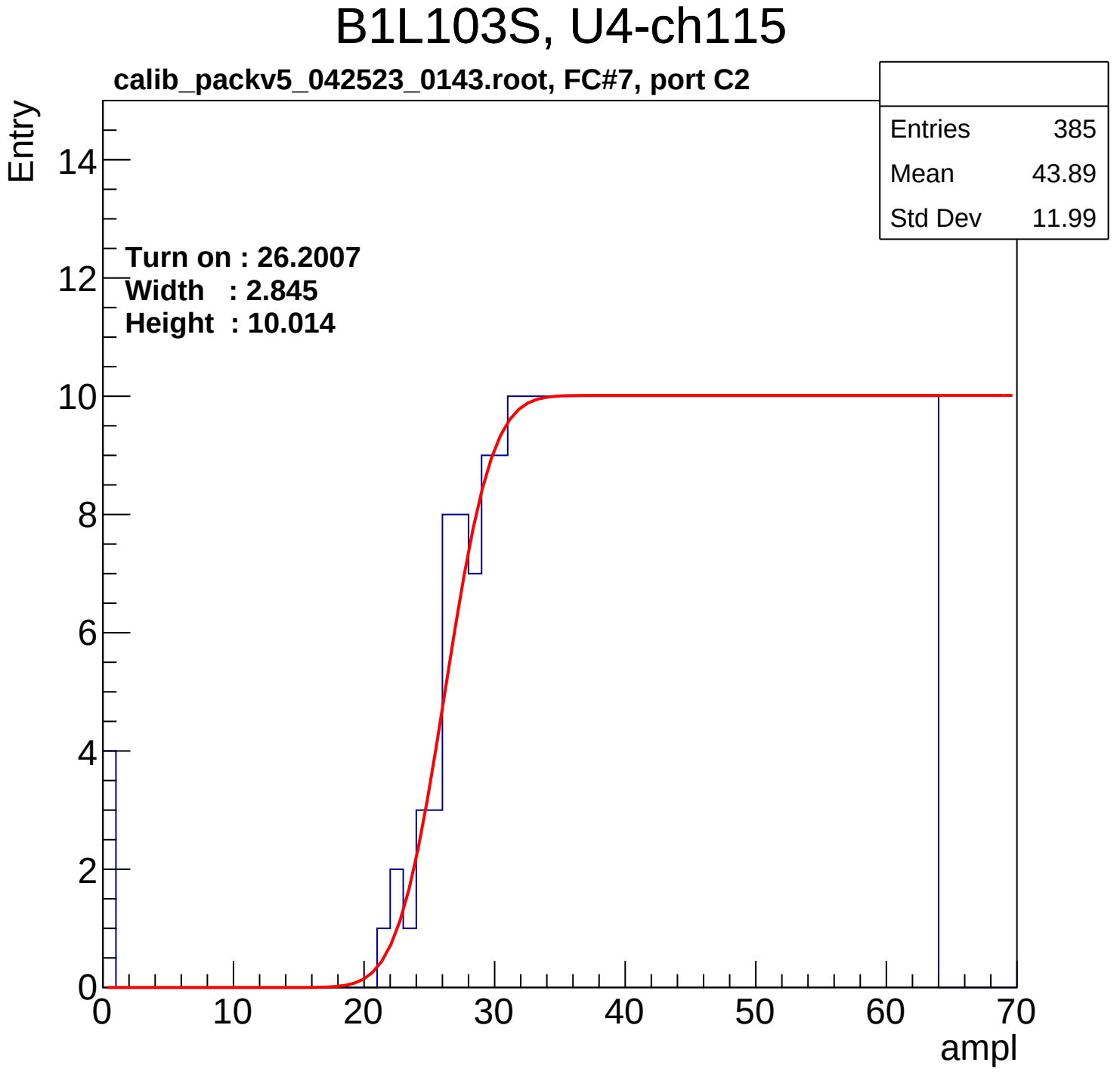
B1L103S, U4-ch115
calib_packv5_042523_0143.root, FC#7, port C2
Entries 385
Mean 43.89
Std Dev 11.99
Turn on : 26.2007
Width : 2.845
Height : 10.014
Entry
ampl
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6
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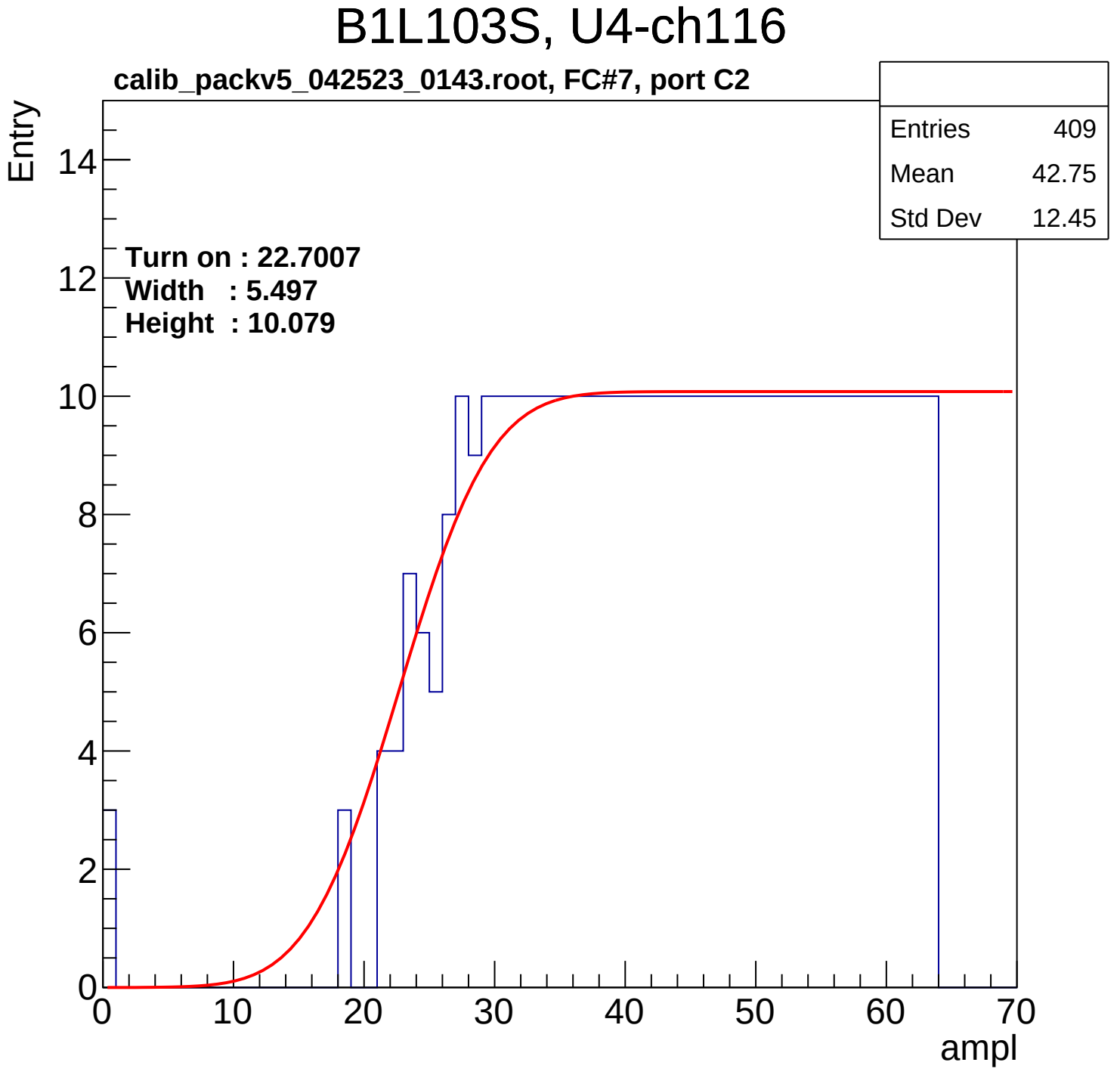
B1L103S, U4-ch116
calib_packv5_042523_0143.root, FC#7, port C2
Entries 409
Mean 42.75
Std Dev 12.45
Turn on : 22.7007
Width : 5.497
Height : 10.079
Entry
ampl
0
2
4
6
8
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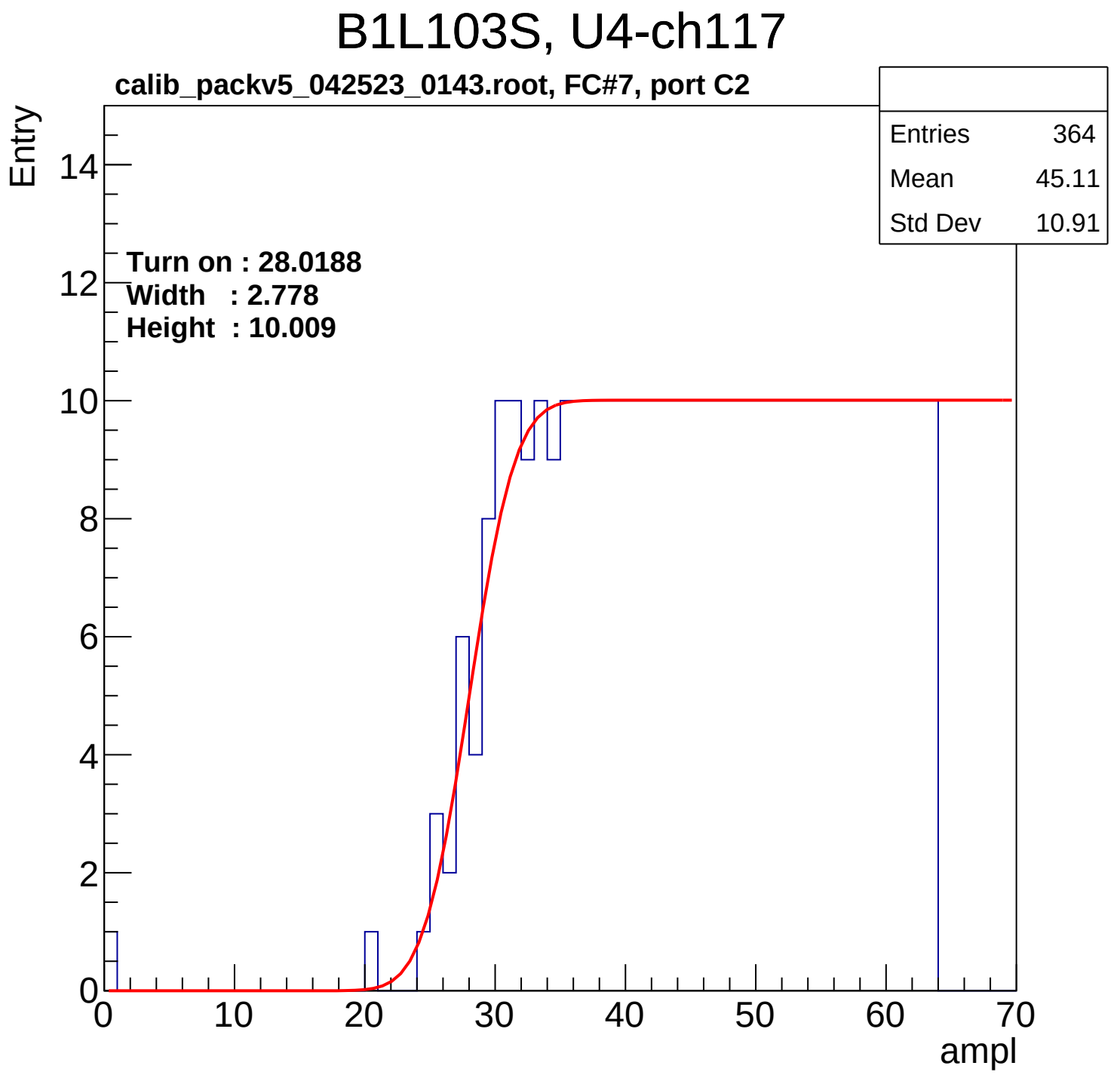
B1L103S, U4-ch117
calib_packv5_042523_0143.root, FC#7, port C2
Entries 364
Mean 45.11
Std Dev 10.91
Turn on : 28.0188
Width : 2.778
Height : 10.009
Entry
ampl
0
2
4
6
8
10
12
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0
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20
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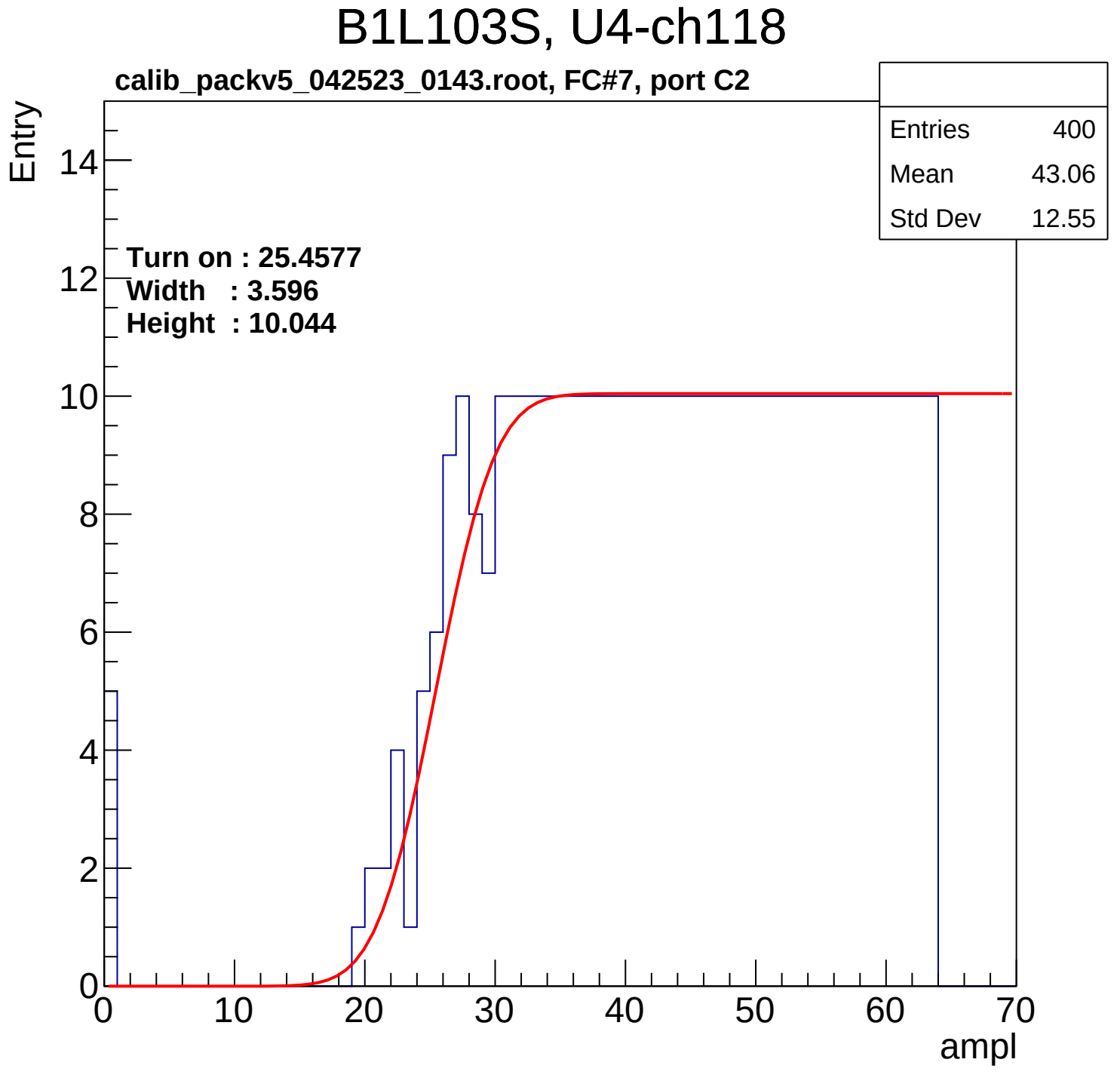
B1L103S, U4-ch118
calib_packv5_042523_0143.root, FC#7, port C2
Entries 400
Mean 43.06
Std Dev 12.55
Turn on : 25.4577
Width : 3.596
Height : 10.044
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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40
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60
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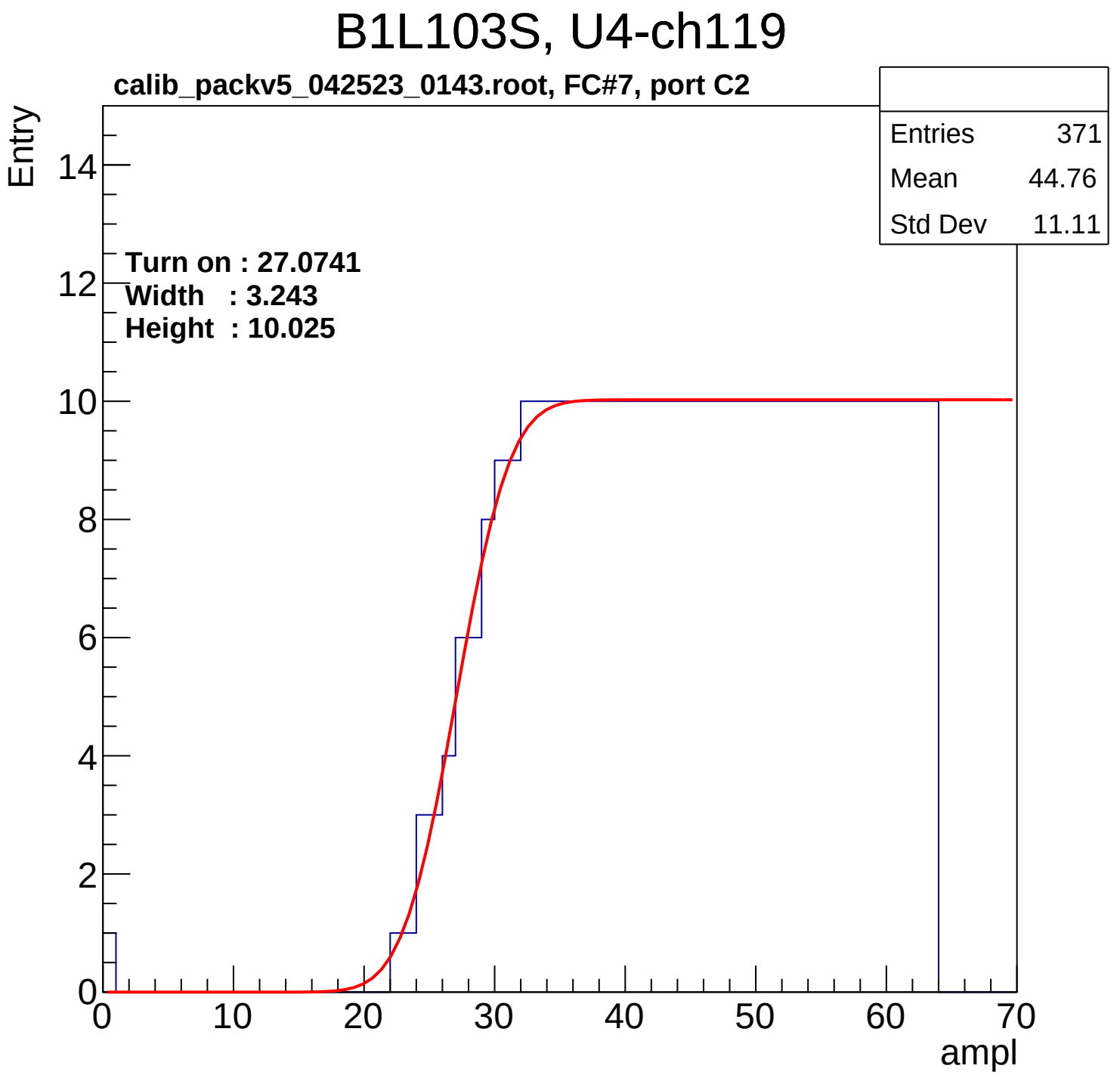
B1L103S, U4-ch119
calib_packv5_042523_0143.root, FC#7, port C2
Entries 371
Mean 44.76
Std Dev 11.11
Turn on : 27.0741
Width : 3.243
Height : 10.025
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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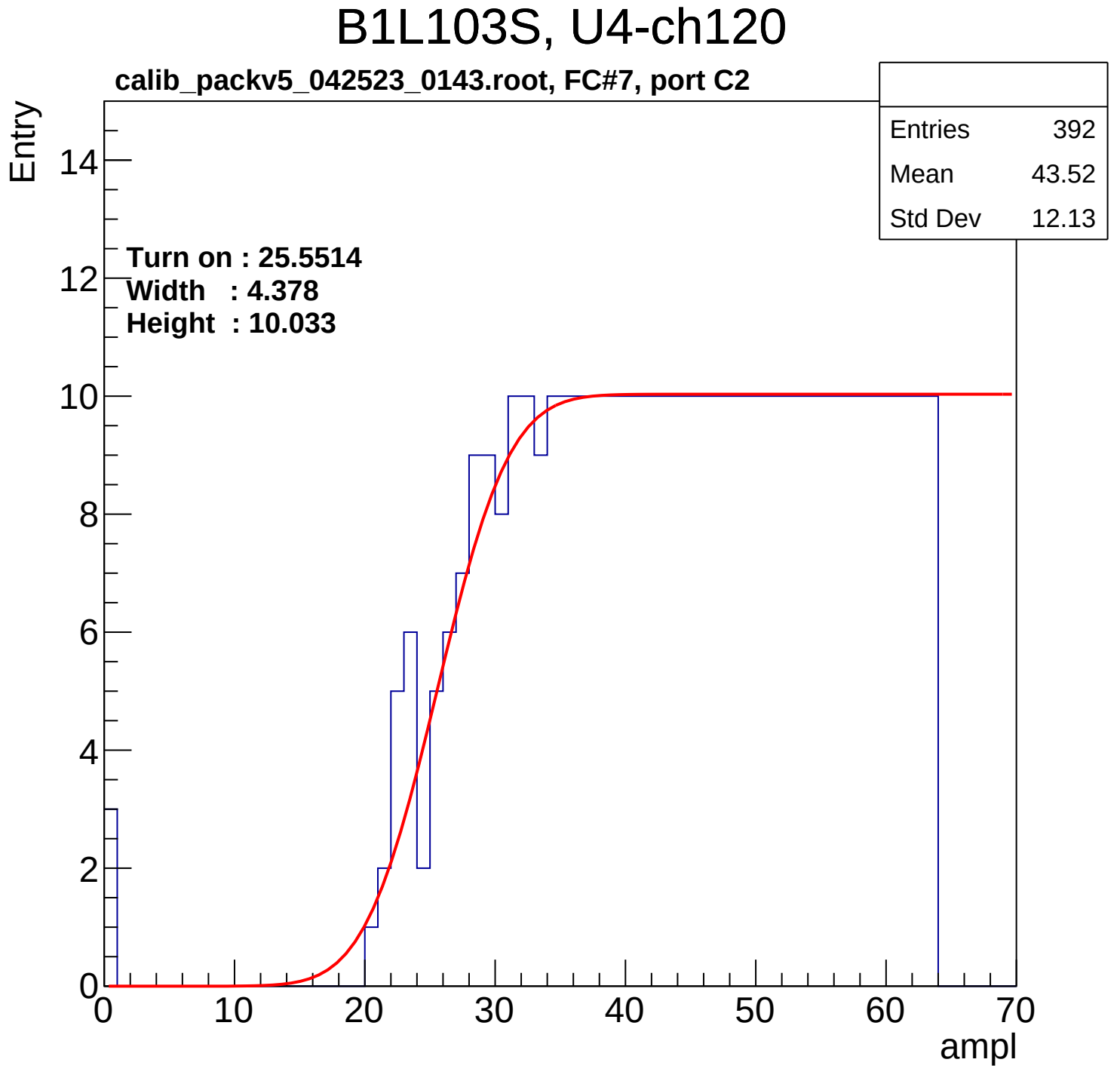
B1L103S, U4-ch120
calib_packv5_042523_0143.root, FC#7, port C2
Entries 392
Mean 43.52
Std Dev 12.13
Turn on : 25.5514
Width : 4.378
Height : 10.033
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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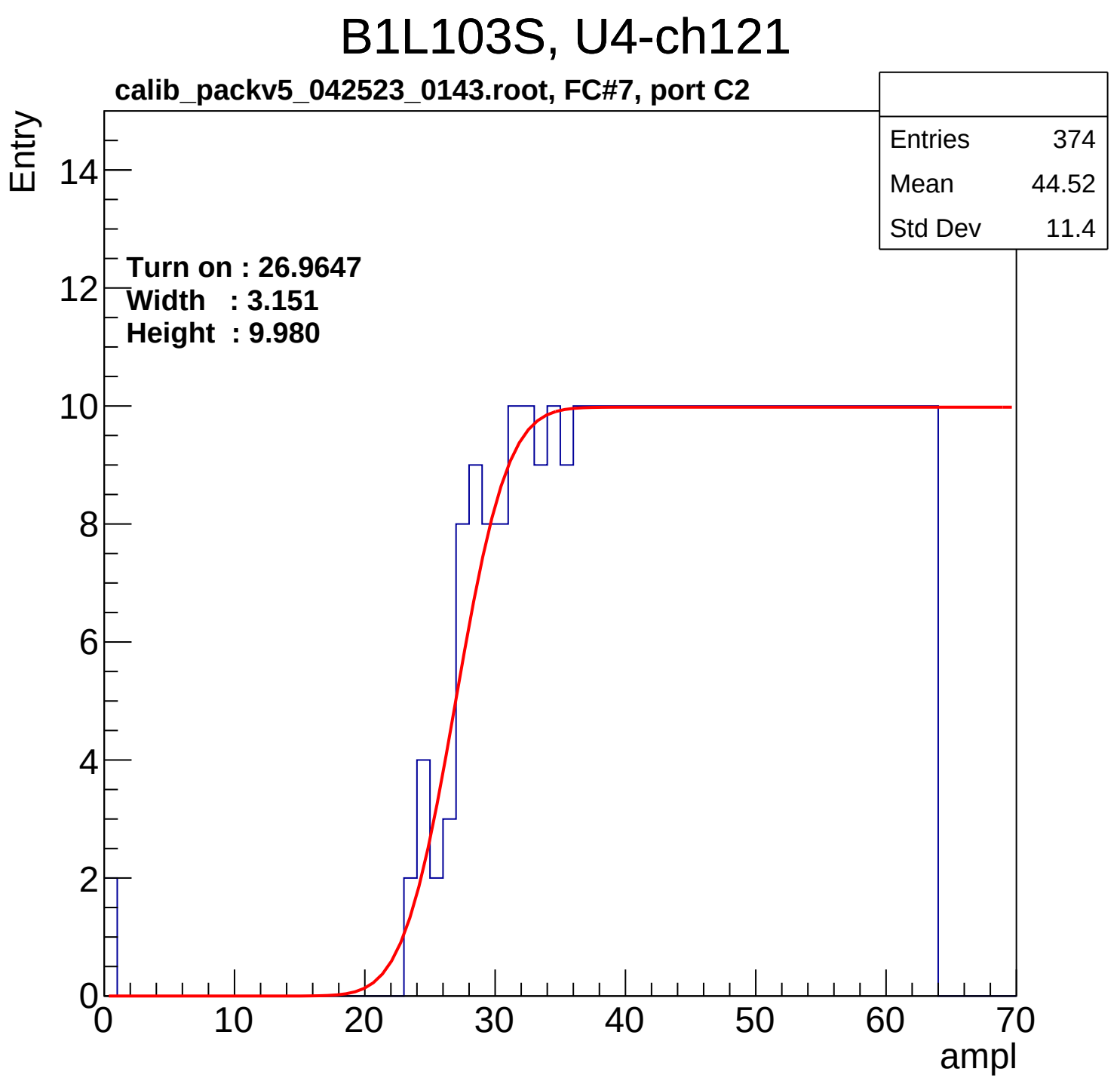
B1L103S, U4-ch121
calib_packv5_042523_0143.root, FC#7, port C2
Entries 374
Mean 44.52
Std Dev 11.4
Turn on : 26.9647
Width : 3.151
Height : 9.980
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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40
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60
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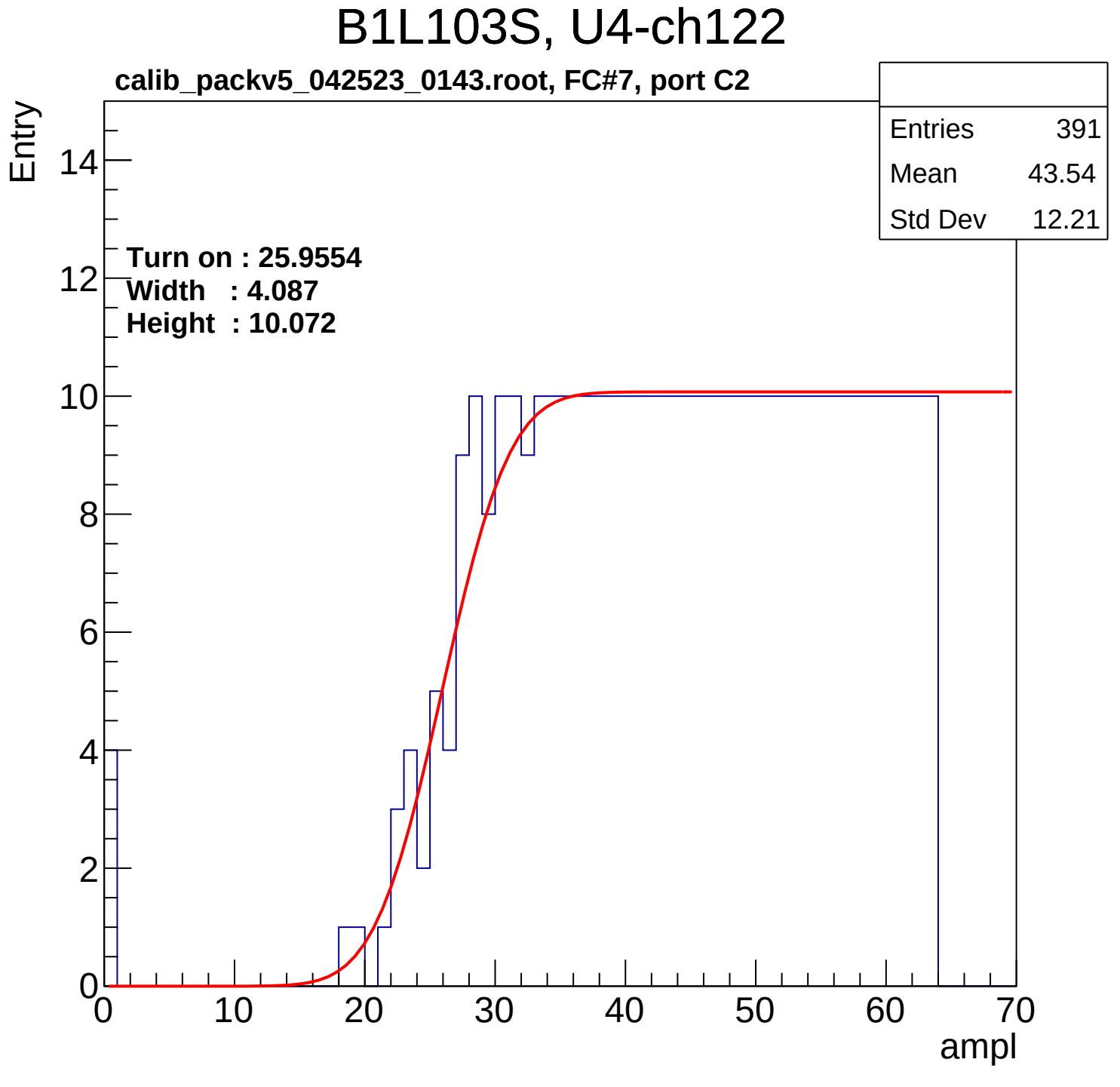
B1L103S, U4-ch122
calib_packv5_042523_0143.root, FC#7, port C2
Entries 391
Mean 43.54
Std Dev 12.21
Turn on : 25.9554
Width : 4.087
Height : 10.072
Entry
ampl
0
2
4
6
8
10
12
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0
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20
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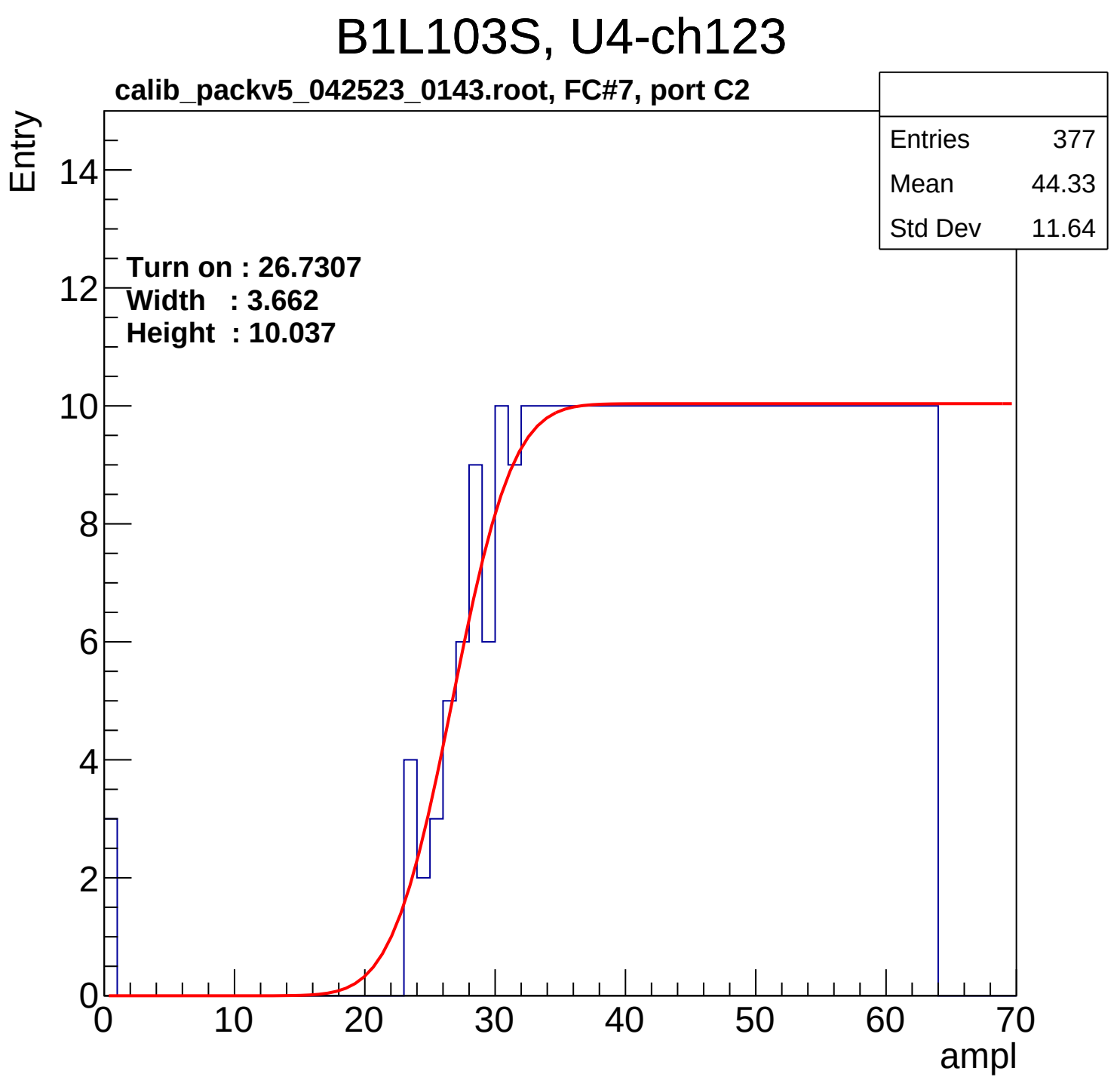
B1L103S, U4-ch123
calib_packv5_042523_0143.root, FC#7, port C2
Entries 377
Mean 44.33
Std Dev 11.64
Turn on : 26.7307
Width : 3.662
Height : 10.037
Entry
ampl
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6
8
10
12
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10
20
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40
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60
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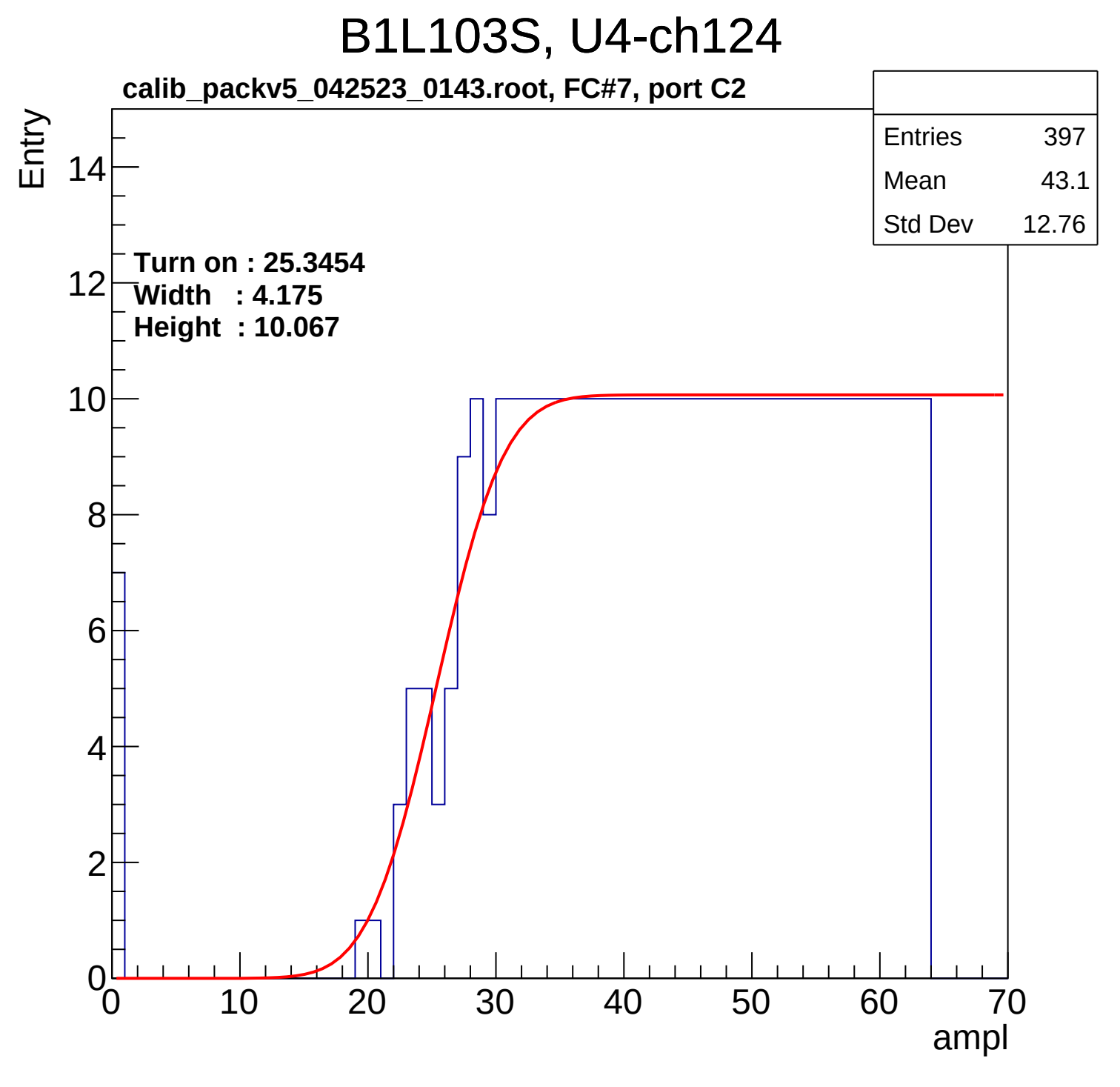
B1L103S, U4-ch124
calib_packv5_042523_0143.root, FC#7, port C2
Entries 397
Mean 43.1
Std Dev 12.76
Turn on : 25.3454
Width : 4.175
Height : 10.067
Entry
ampl
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4
6
8
10
12
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20
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40
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60
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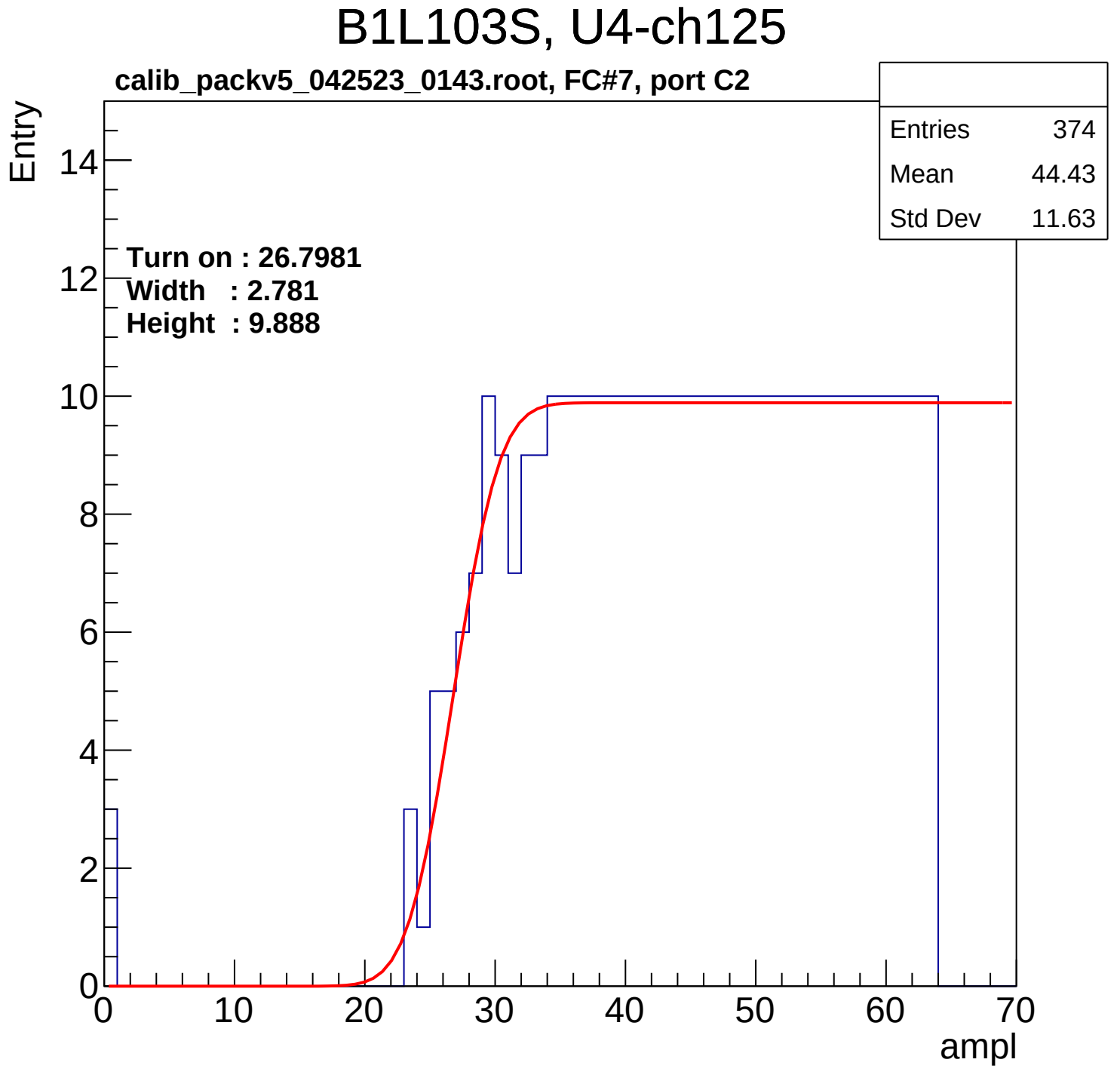
B1L103S, U4-ch125
calib_packv5_042523_0143.root, FC#7, port C2
Entries 374
Mean 44.43
Std Dev 11.63
Turn on : 26.7981
Width : 2.781
Height : 9.888
Entry
ampl
0
2
4
6
8
10
12
14
0
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20
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40
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60
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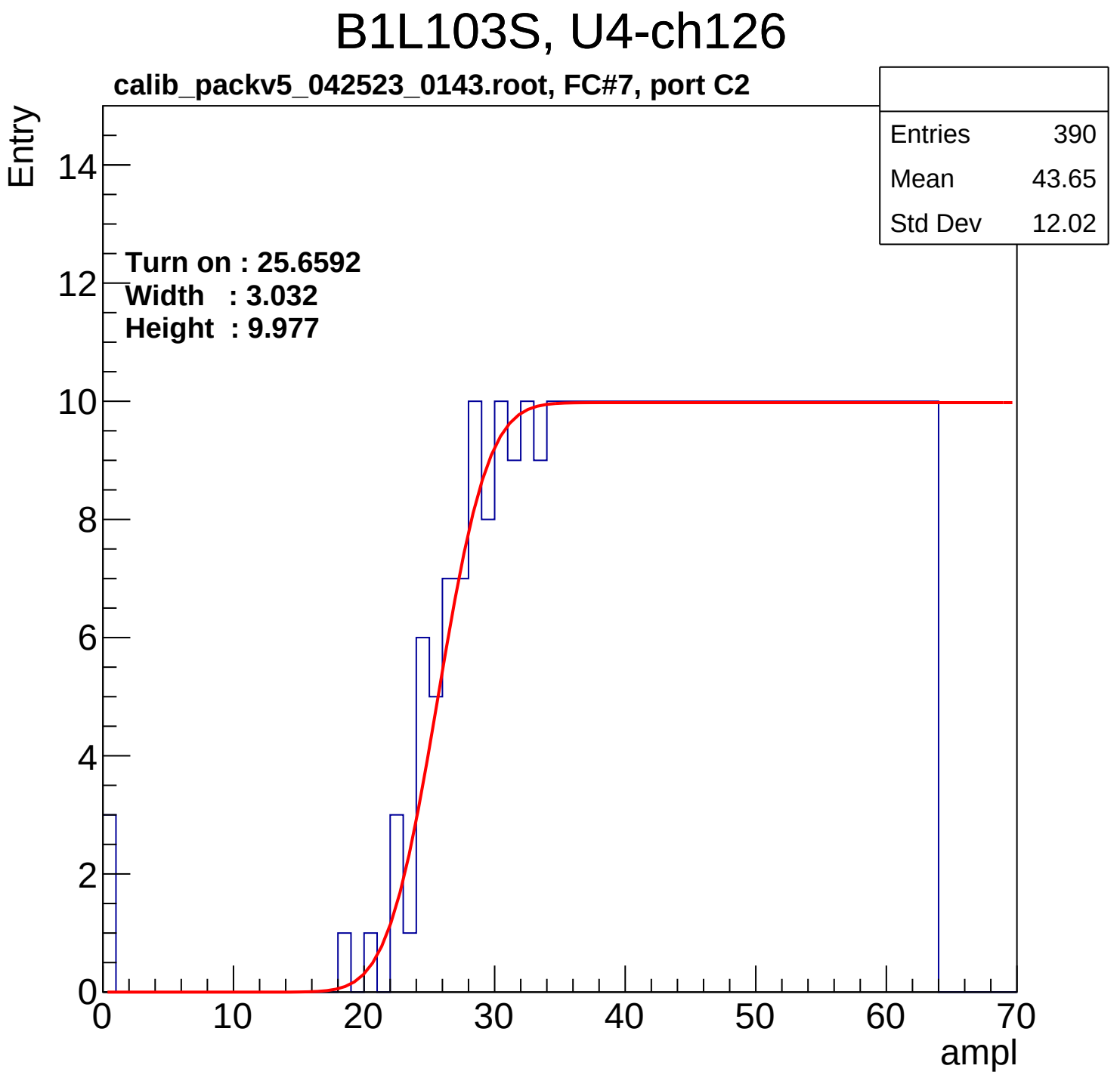
B1L103S, U4-ch126
calib_packv5_042523_0143.root, FC#7, port C2
Entries 390
Mean 43.65
Std Dev 12.02
Turn on : 25.6592
Width : 3.032
Height : 9.977
Entry
ampl
0
2
4
6
8
10
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14
0
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20
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40
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60
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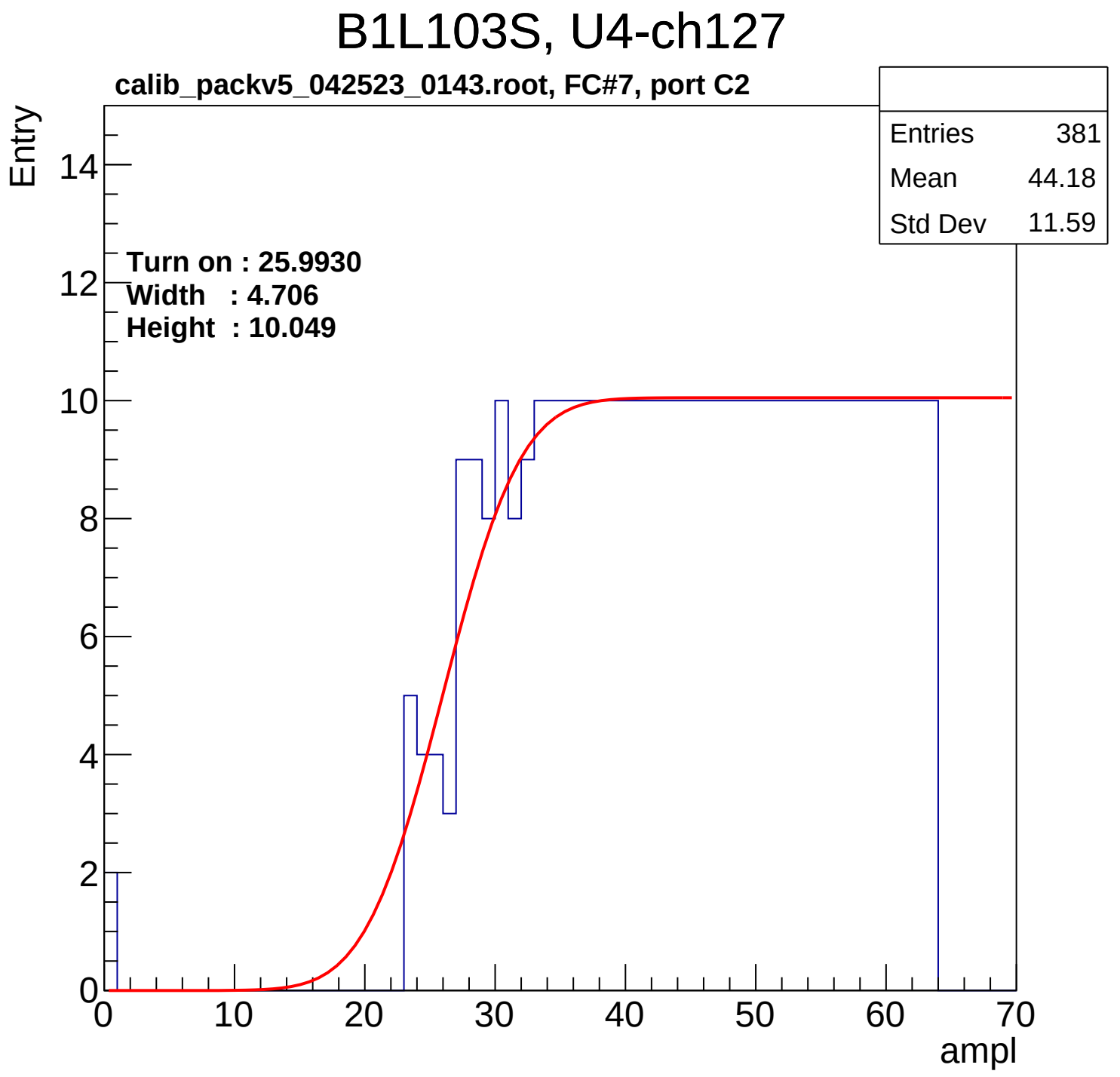
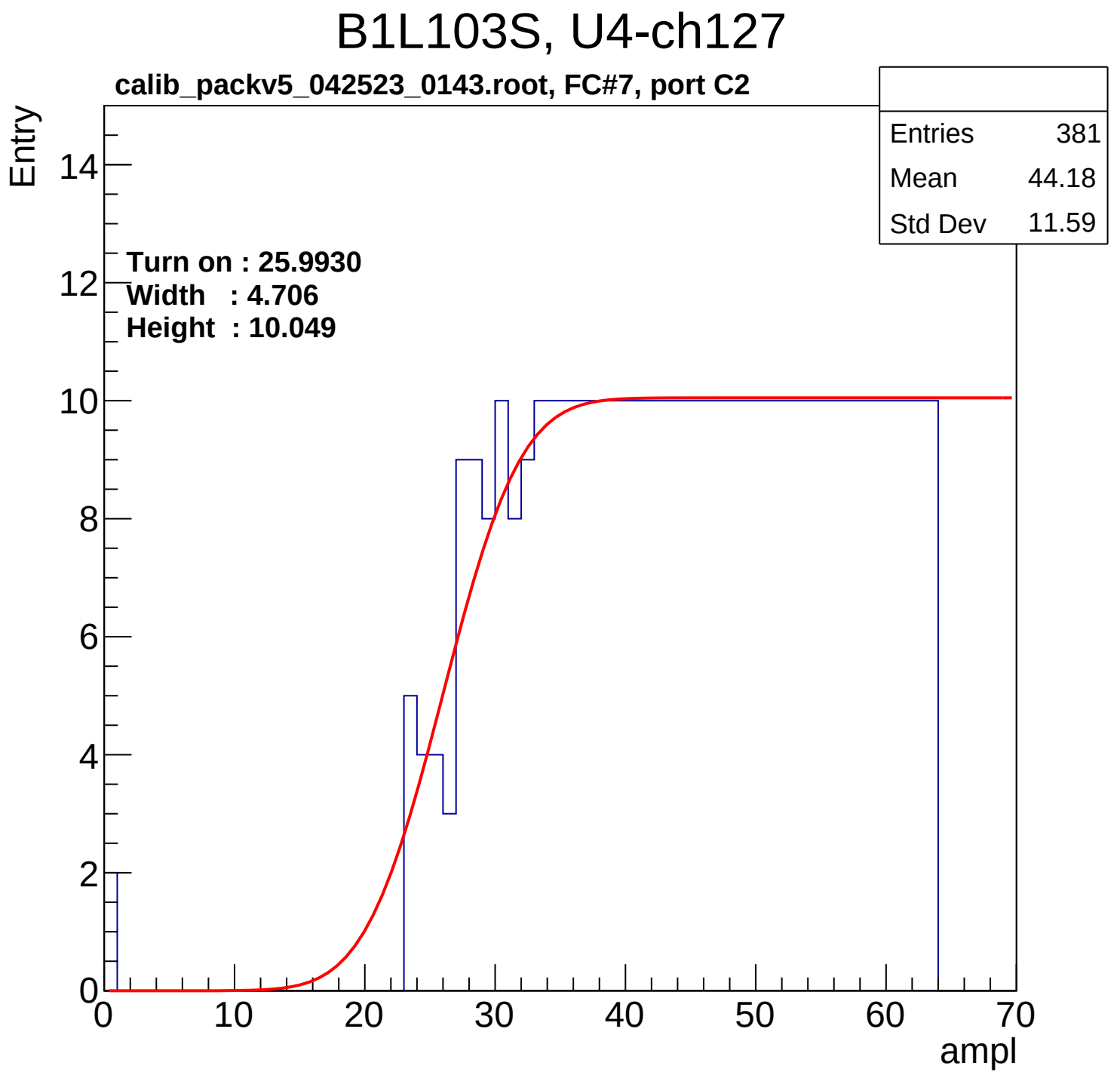

B1L103S, U4-ch127
calib_packv5_042523_0143.root, FC#7, port C2
Entries 381
Mean 44.18
Std Dev 11.59
Turn on : 25.9930
Width : 4.706
Height : 10.049
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L103S, U4-ch127
calib_packv5_042523_0143.root, FC#7, port C2
Entries 381
Mean 44.18
Std Dev 11.59
Turn on : 25.9930
Width : 4.706
Height : 10.049
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70