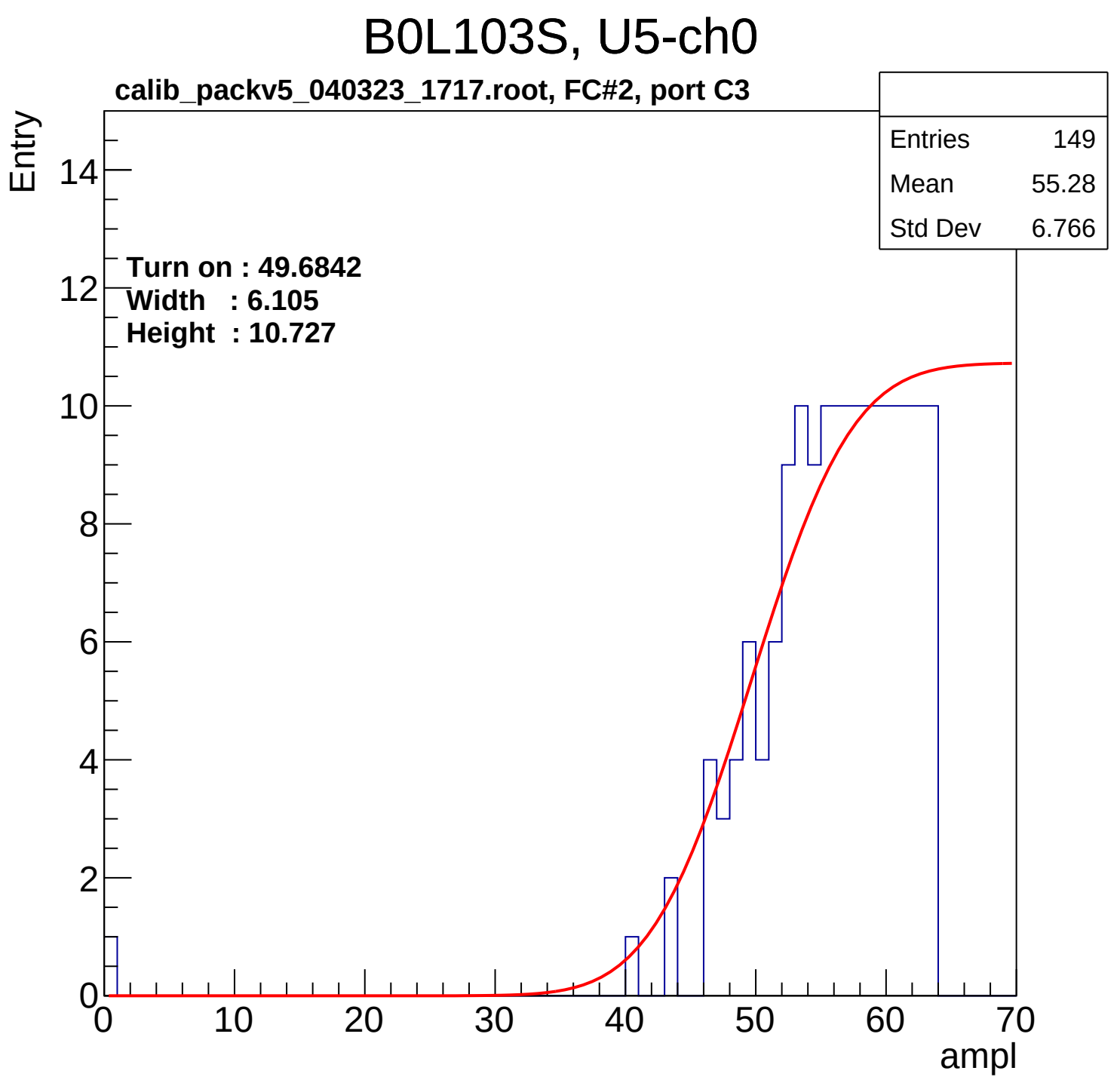
B0L103S, U5-ch0
calib_packv5_040323_1717.root, FC#2, port C3
Entries 149
Mean 55.28
Std Dev 6.766
Turn on : 49.6842
Width : 6.105
Height : 10.727
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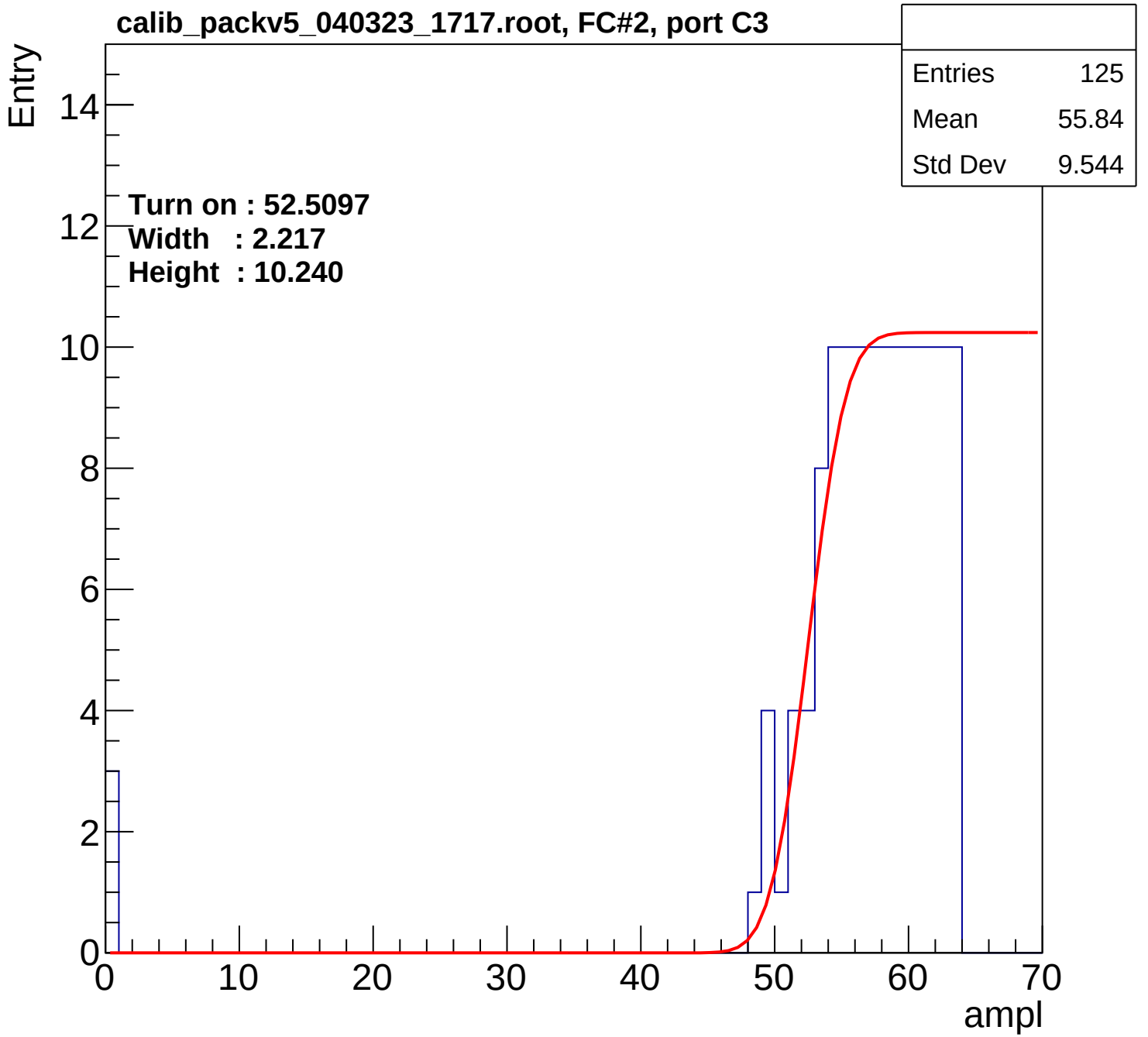
B0L103S, U5-ch1
calib_packv5_040323_1717.root, FC#2, port C3
Entries 125
Mean 55.84
Std Dev 9.544
Turn on : 52.5097
Width : 2.217
Height : 10.240
Entry
ampl
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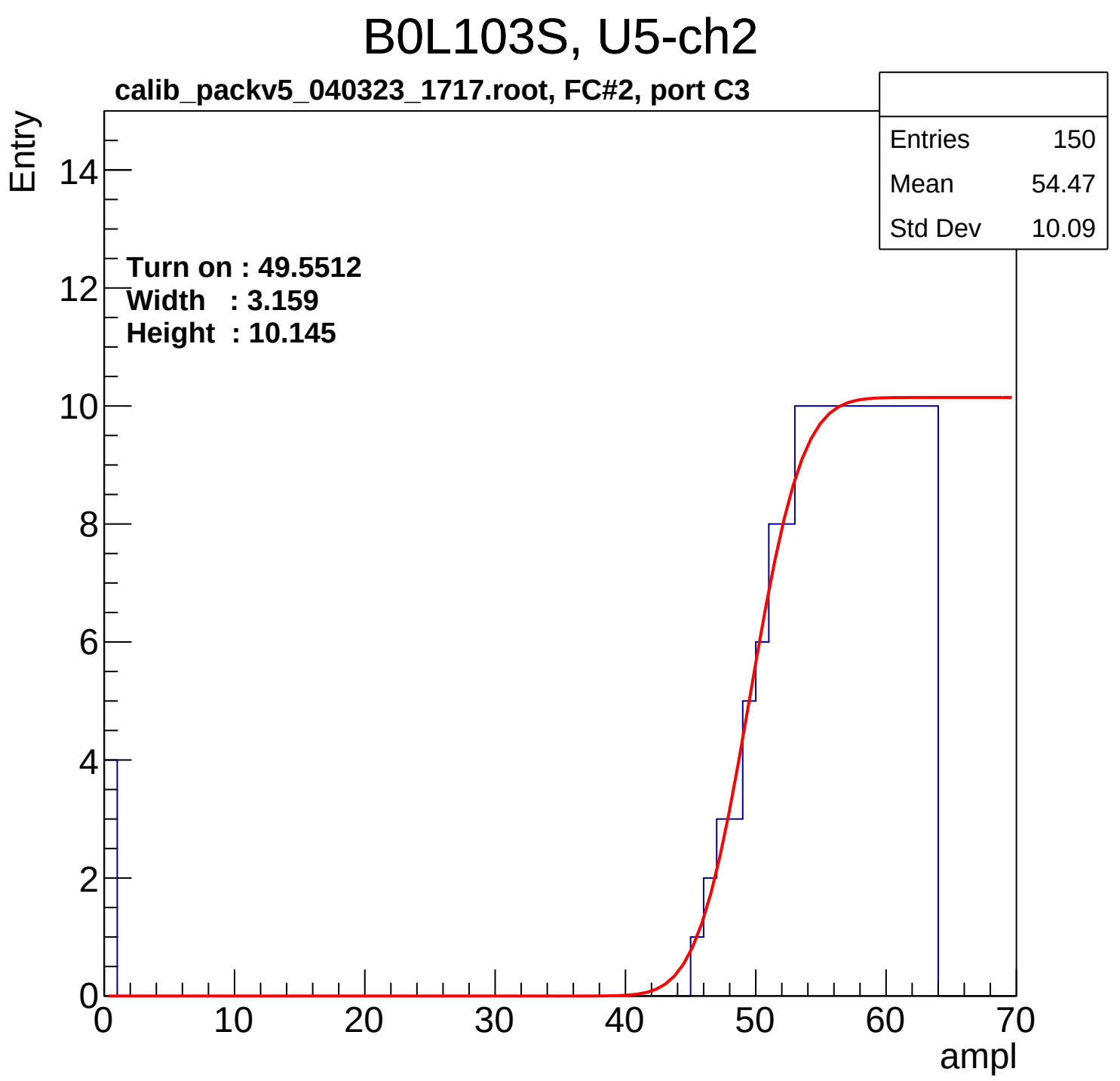
B0L103S, U5-ch2
calib_packv5_040323_1717.root, FC#2, port C3
Entries 150
Mean 54.47
Std Dev 10.09
Turn on : 49.5512
Width : 3.159
Height : 10.145
Entry
ampl
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2
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6
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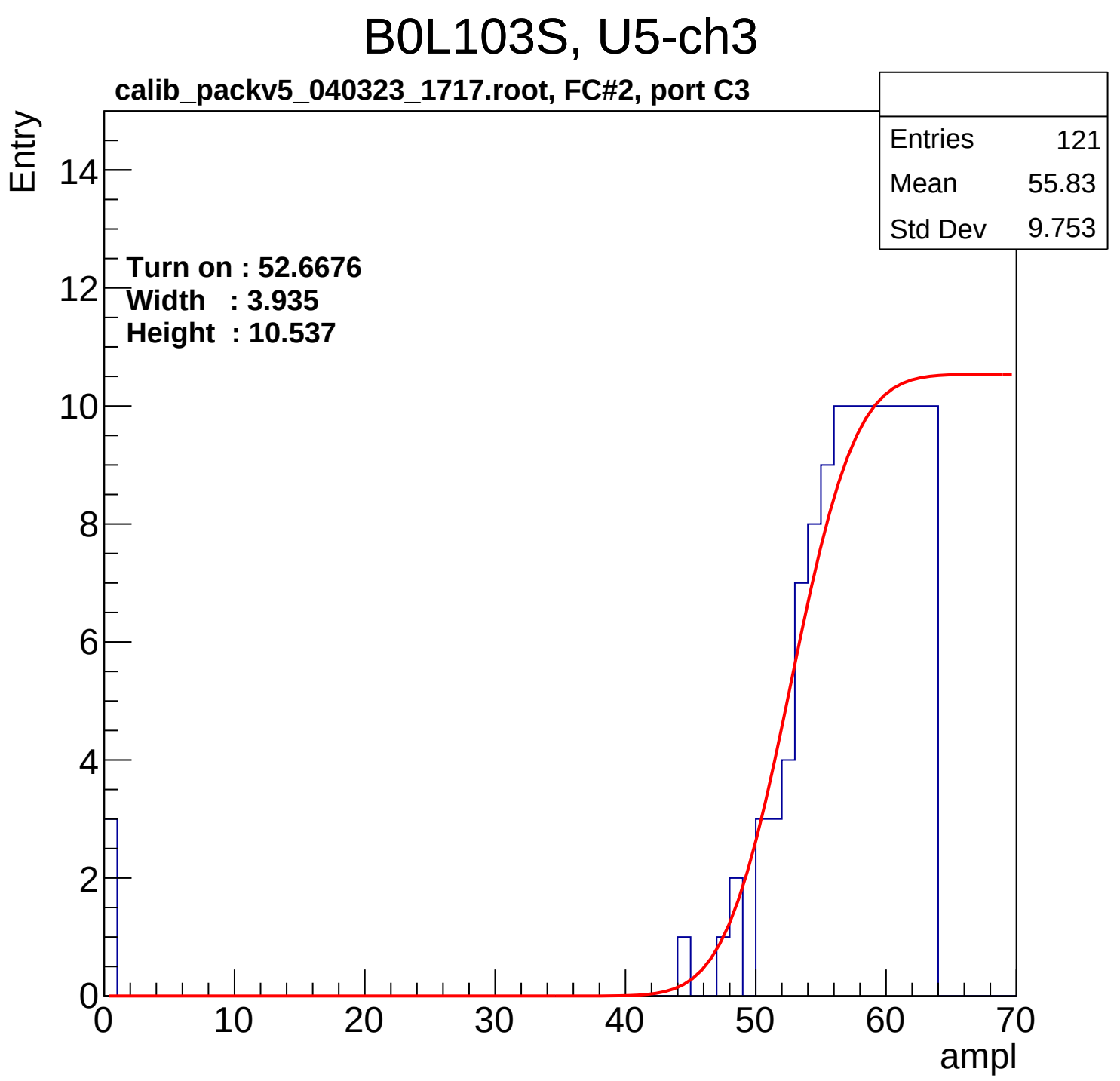
B0L103S, U5-ch3
calib_packv5_040323_1717.root, FC#2, port C3
Entries 121
Mean 55.83
Std Dev 9.753
Turn on : 52.6676
Width : 3.935
Height : 10.537
Entry
ampl
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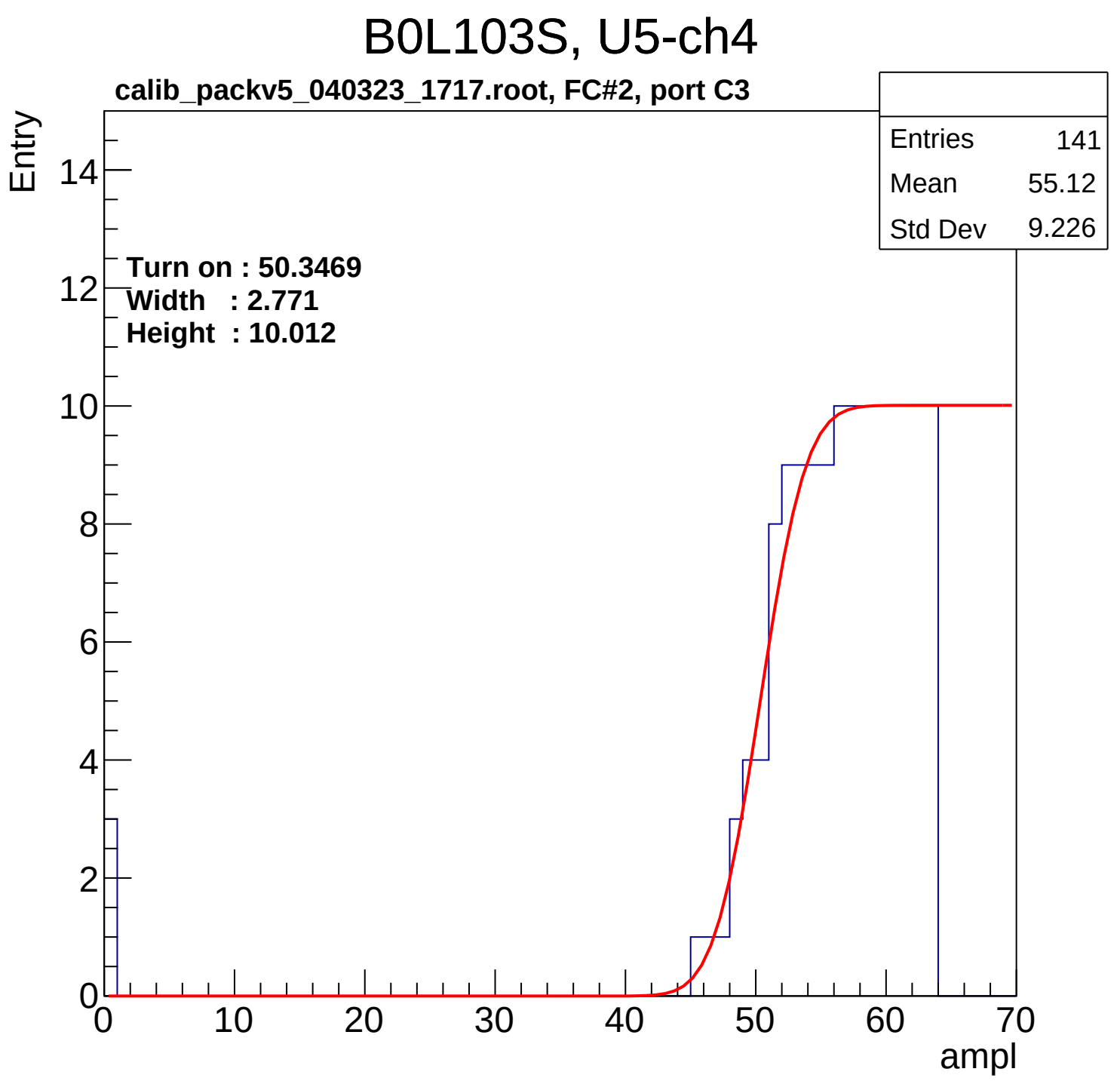
B0L103S, U5-ch4
calib_packv5_040323_1717.root, FC#2, port C3
Entries 141
Mean 55.12
Std Dev 9.226
Turn on : 50.3469
Width : 2.771
Height : 10.012
Entry
ampl
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2
4
6
8
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12
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0
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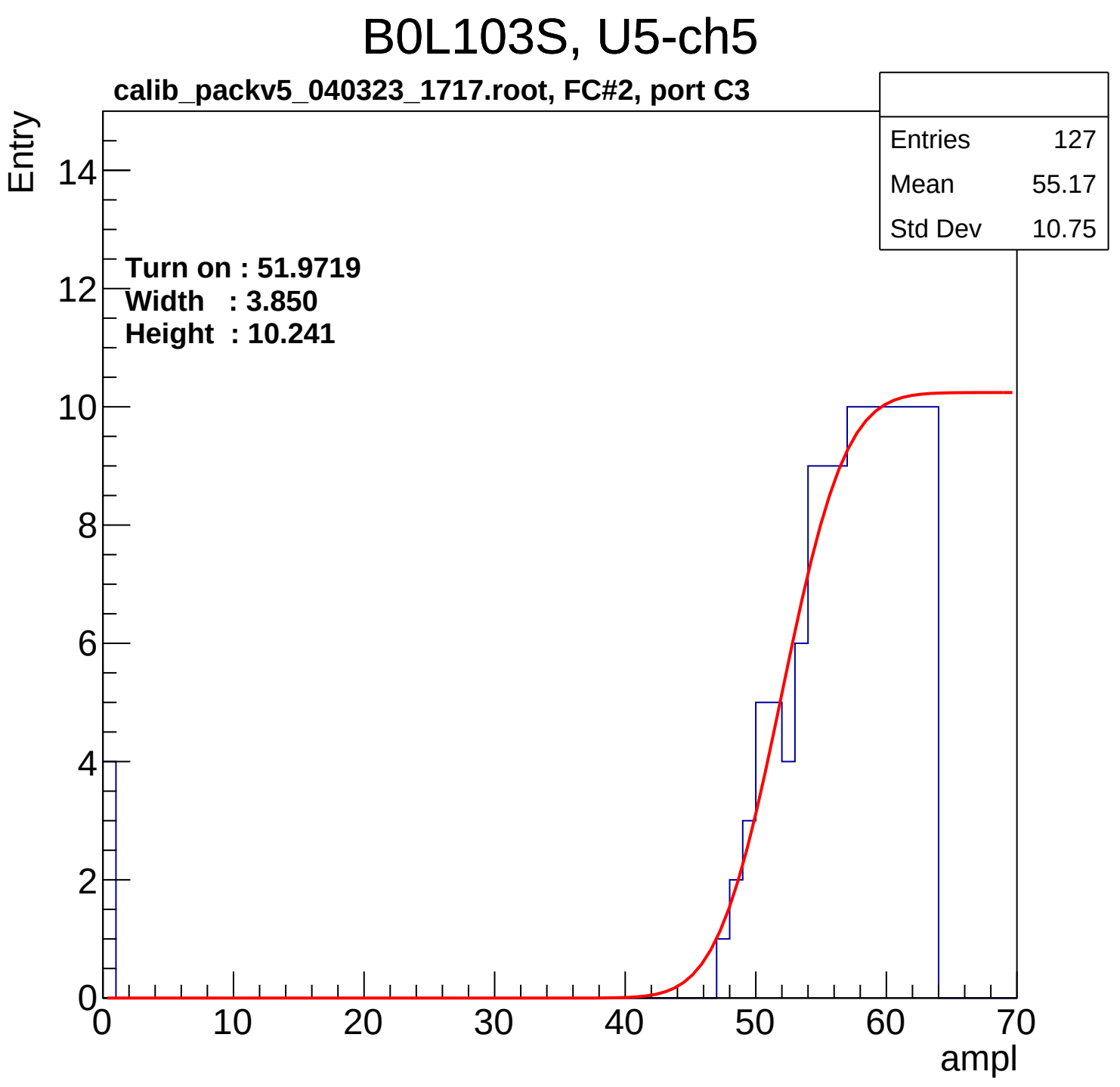
B0L103S, U5-ch5
calib_packv5_040323_1717.root, FC#2, port C3
Entries 127
Mean 55.17
Std Dev 10.75
Turn on : 51.9719
Width : 3.850
Height : 10.241
Entry
ampl
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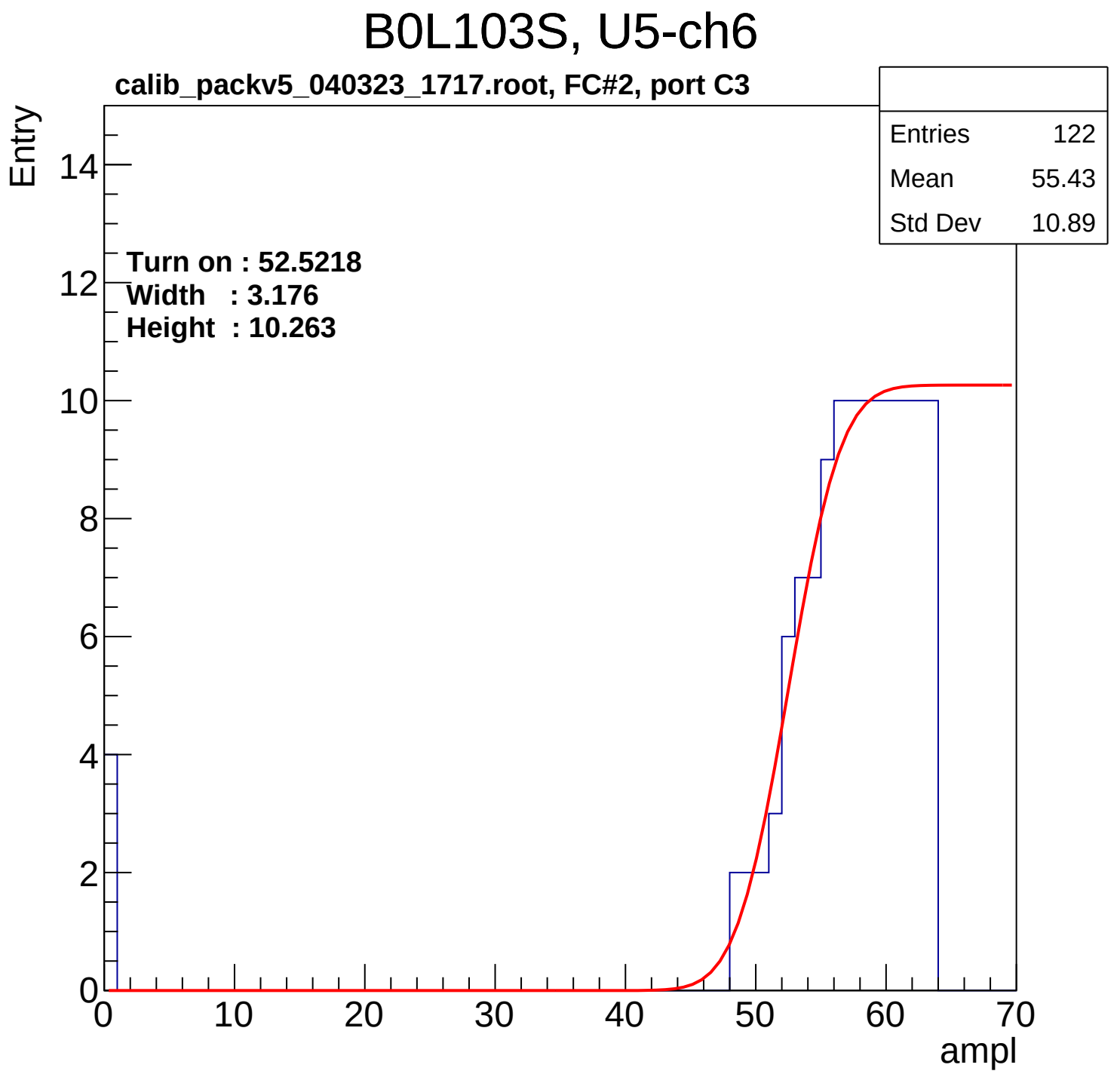
B0L103S, U5-ch6
calib_packv5_040323_1717.root, FC#2, port C3
Entries 122
Mean 55.43
Std Dev 10.89
Turn on : 52.5218
Width : 3.176
Height : 10.263
Entry
ampl
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6
8
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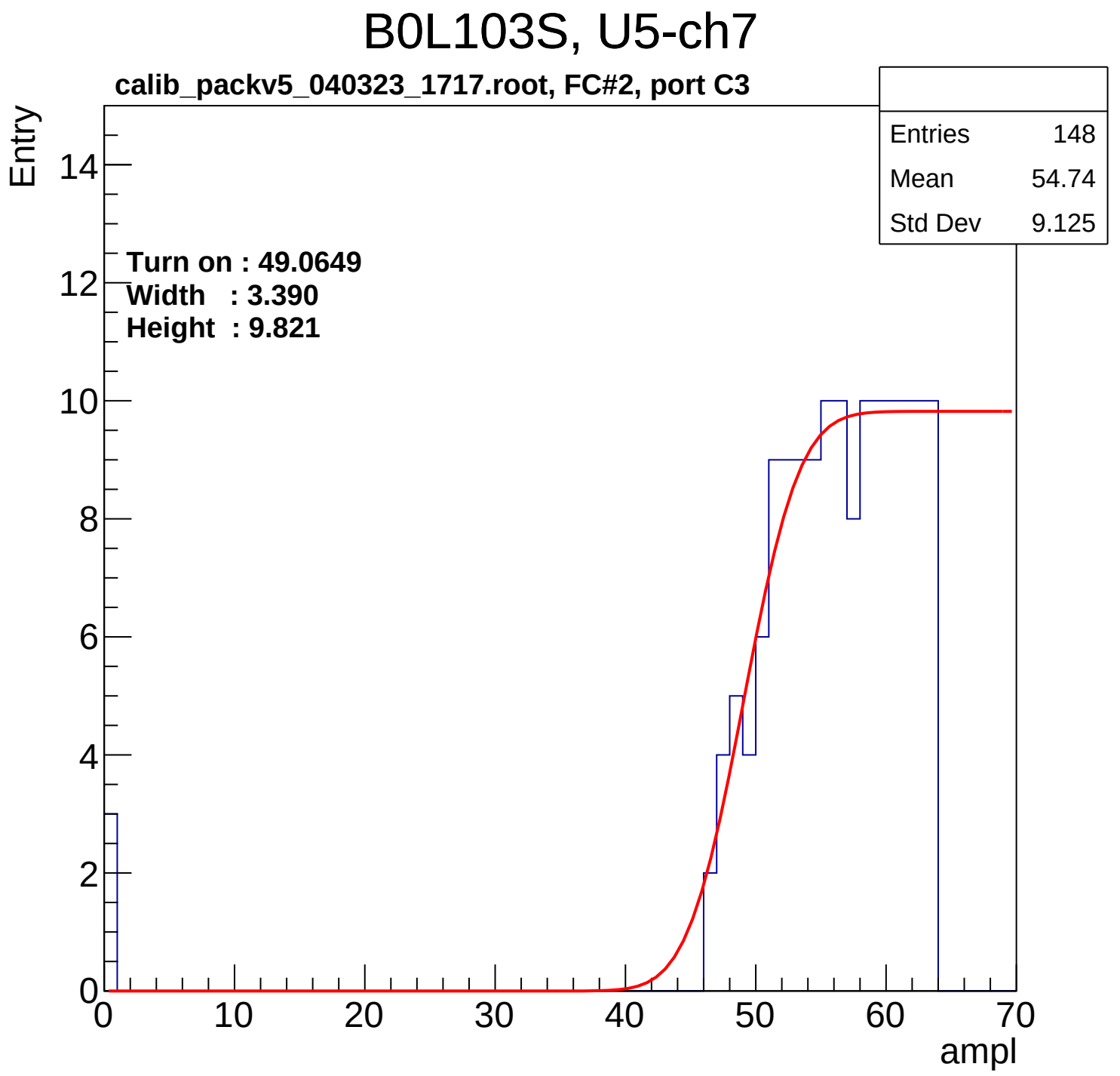
B0L103S, U5-ch7
calib_packv5_040323_1717.root, FC#2, port C3
Entries 148
Mean 54.74
Std Dev 9.125
Turn on : 49.0649
Width : 3.390
Height : 9.821
Entry
ampl
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6
8
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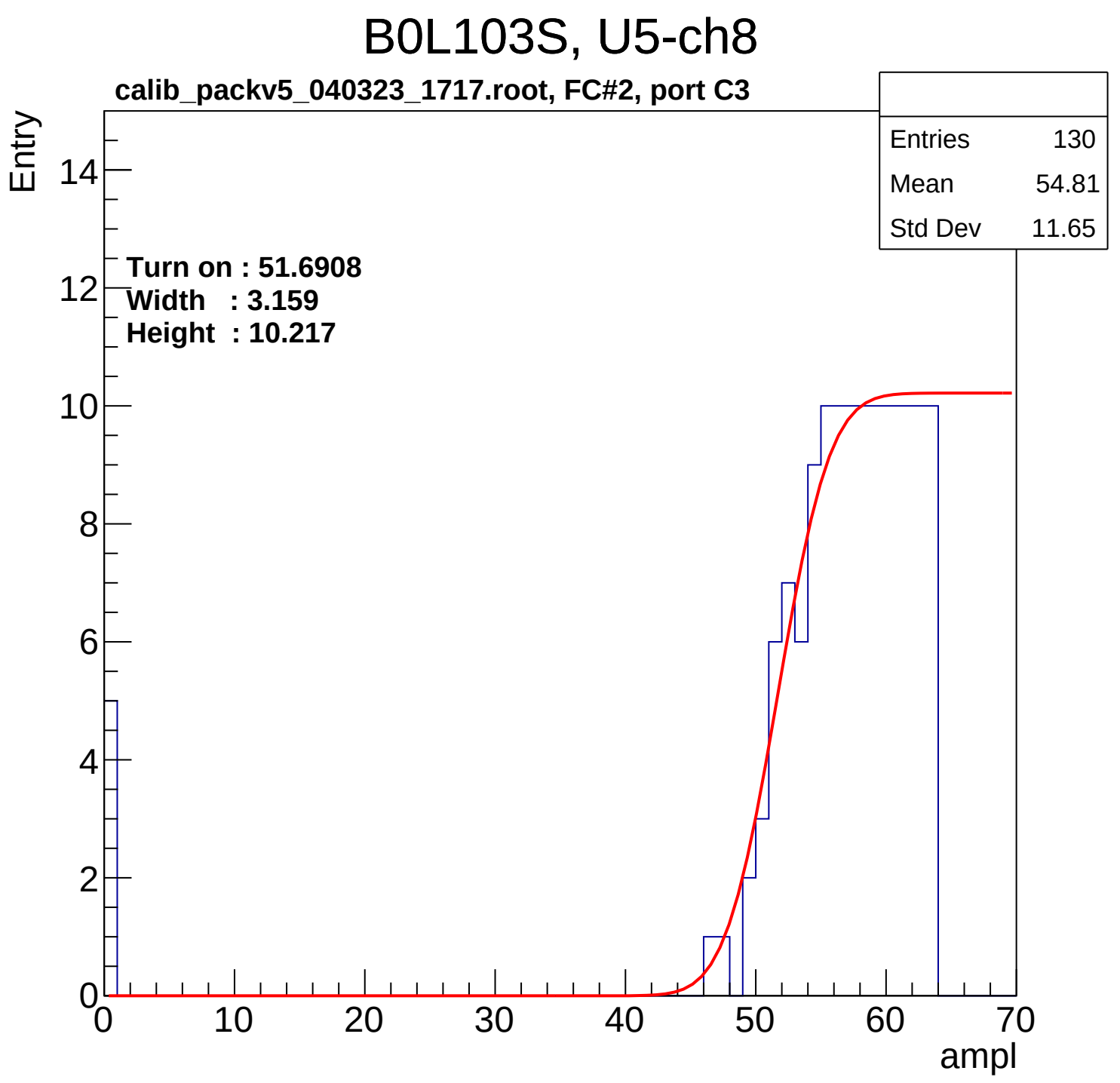
B0L103S, U5-ch8
calib_packv5_040323_1717.root, FC#2, port C3
Entries 130
Mean 54.81
Std Dev 11.65
Turn on : 51.6908
Width : 3.159
Height : 10.217
Entry
ampl
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8
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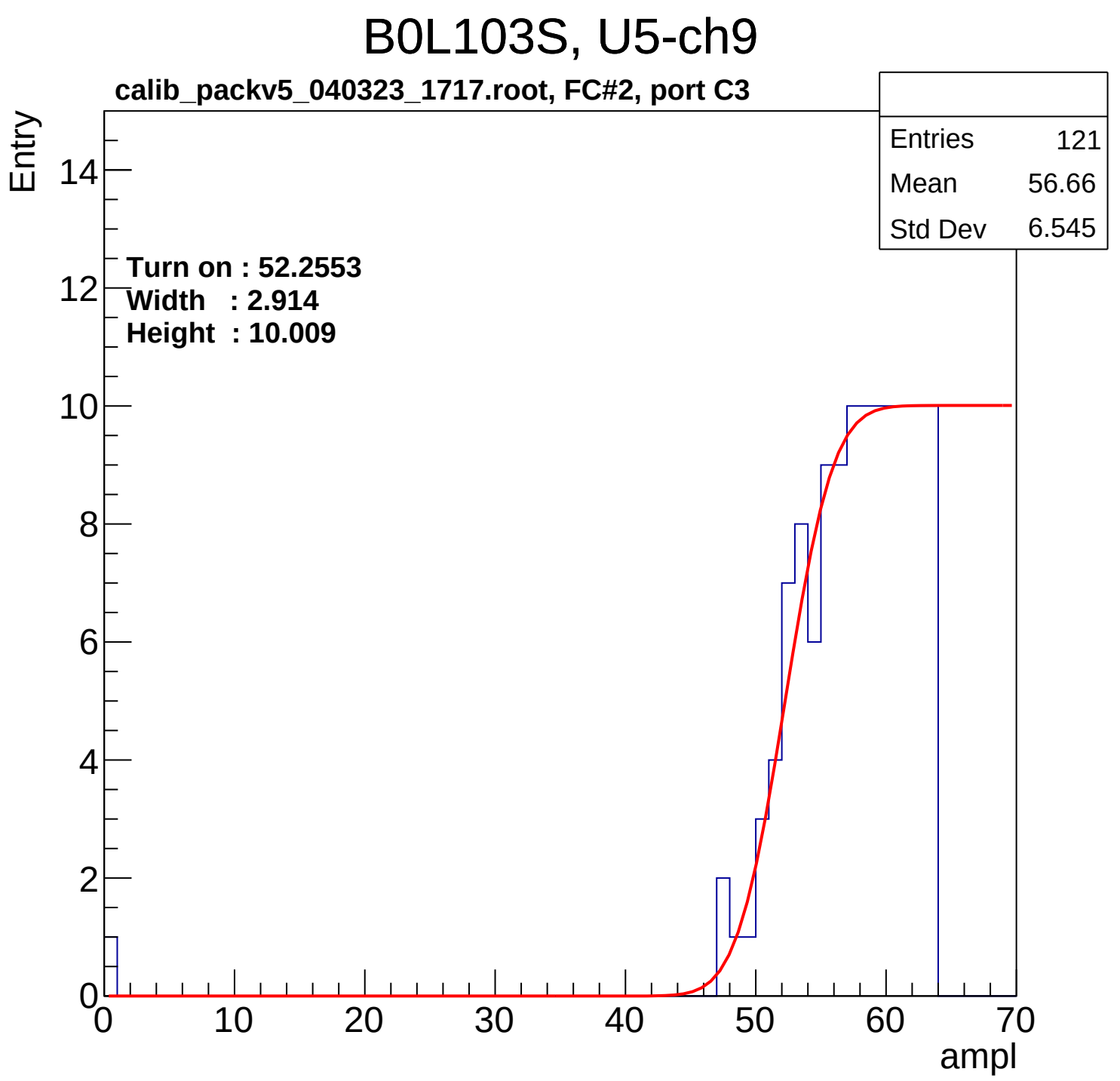
B0L103S, U5-ch9
calib_packv5_040323_1717.root, FC#2, port C3
Entries 121
Mean 56.66
Std Dev 6.545
Turn on : 52.2553
Width : 2.914
Height : 10.009
Entry
ampl
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6
8
10
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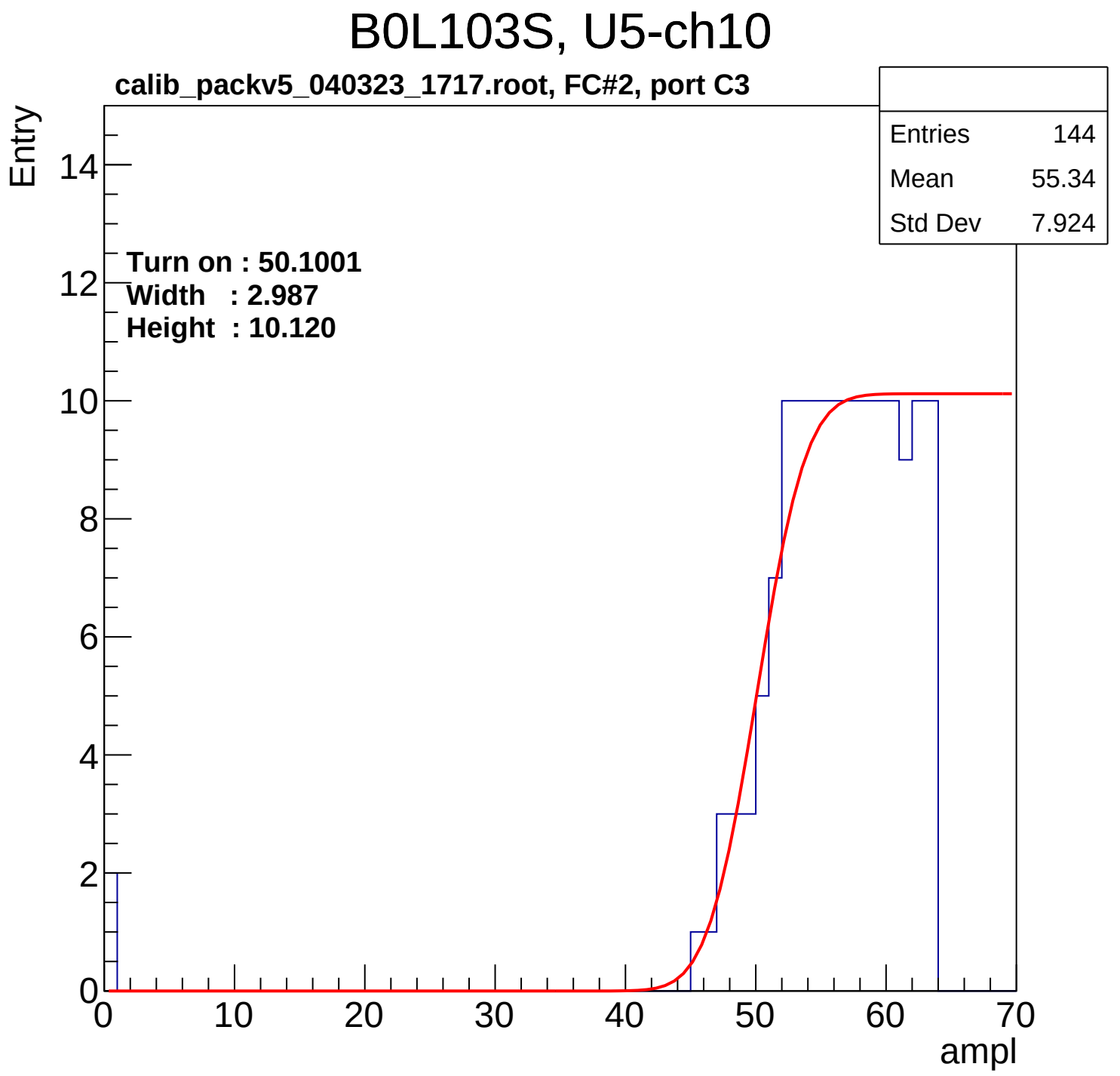
B0L103S, U5-ch10
calib_packv5_040323_1717.root, FC#2, port C3
Entries 144
Mean 55.34
Std Dev 7.924
Turn on : 50.1001
Width : 2.987
Height : 10.120
Entry
ampl
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6
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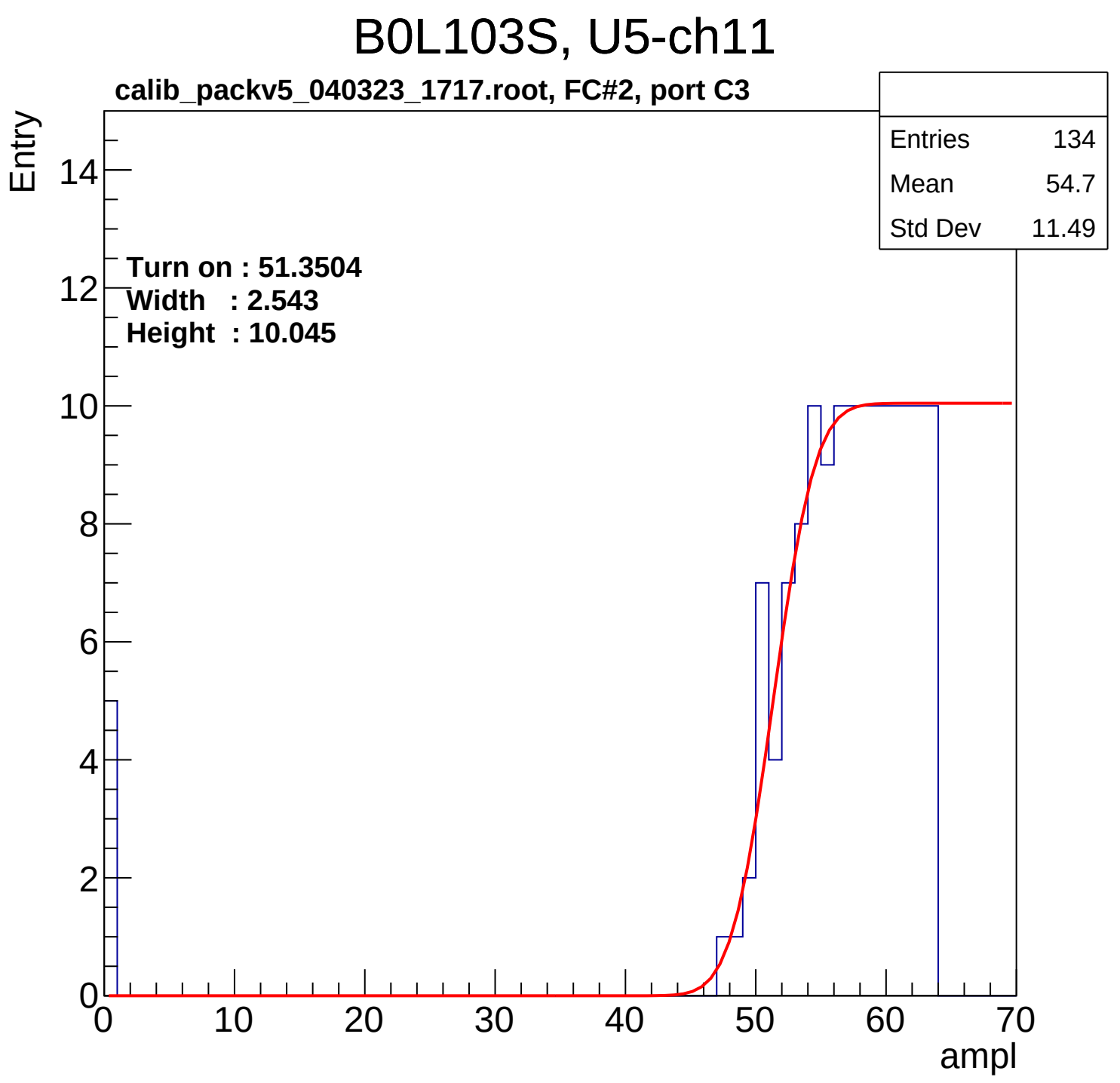
B0L103S, U5-ch11
calib_packv5_040323_1717.root, FC#2, port C3
Entries 134
Mean 54.7
Std Dev 11.49
Turn on : 51.3504
Width : 2.543
Height : 10.045
Entry
ampl
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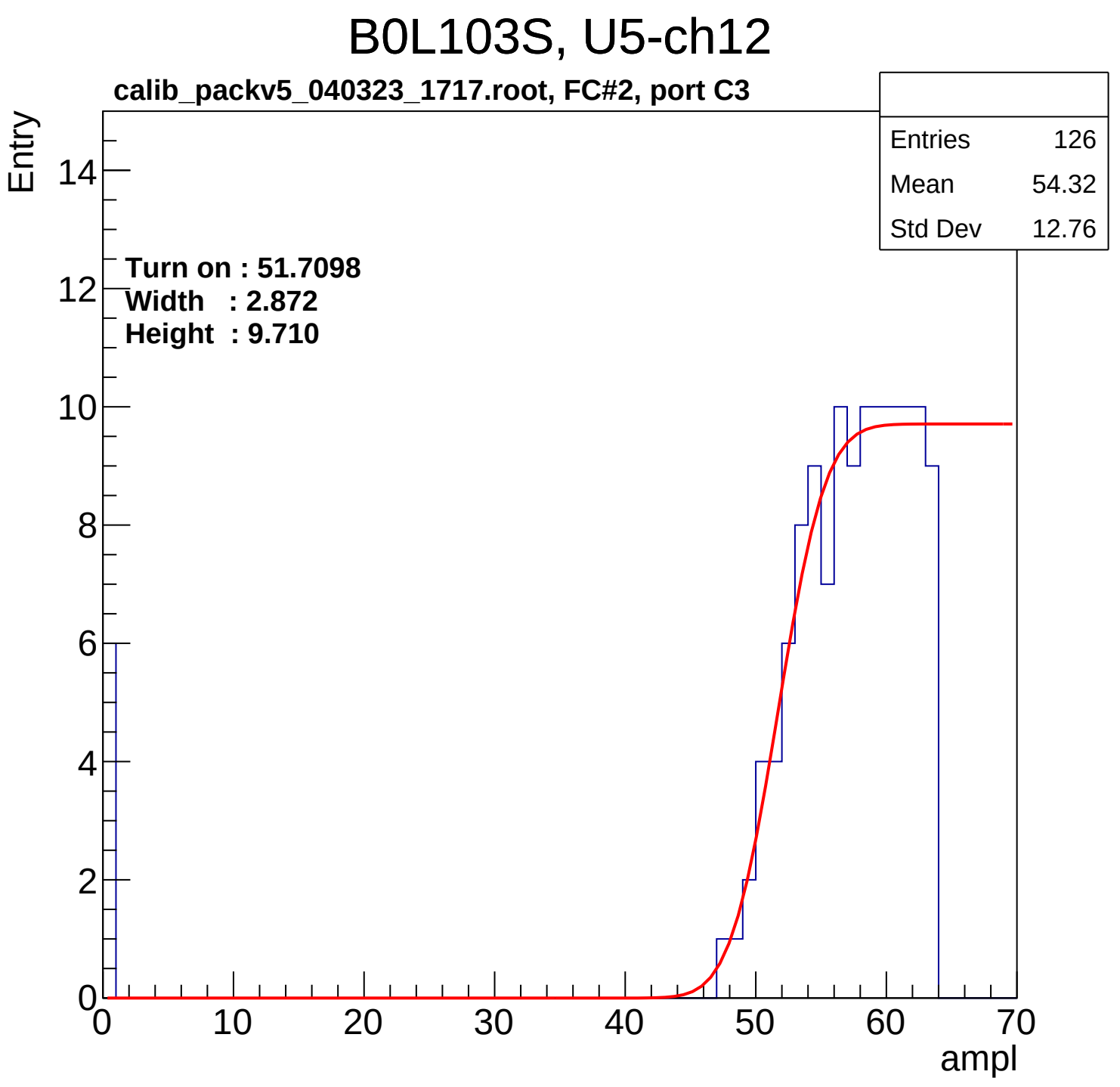
B0L103S, U5-ch12
calib_packv5_040323_1717.root, FC#2, port C3
Entries 126
Mean 54.32
Std Dev 12.76
Turn on : 51.7098
Width : 2.872
Height : 9.710
Entry
ampl
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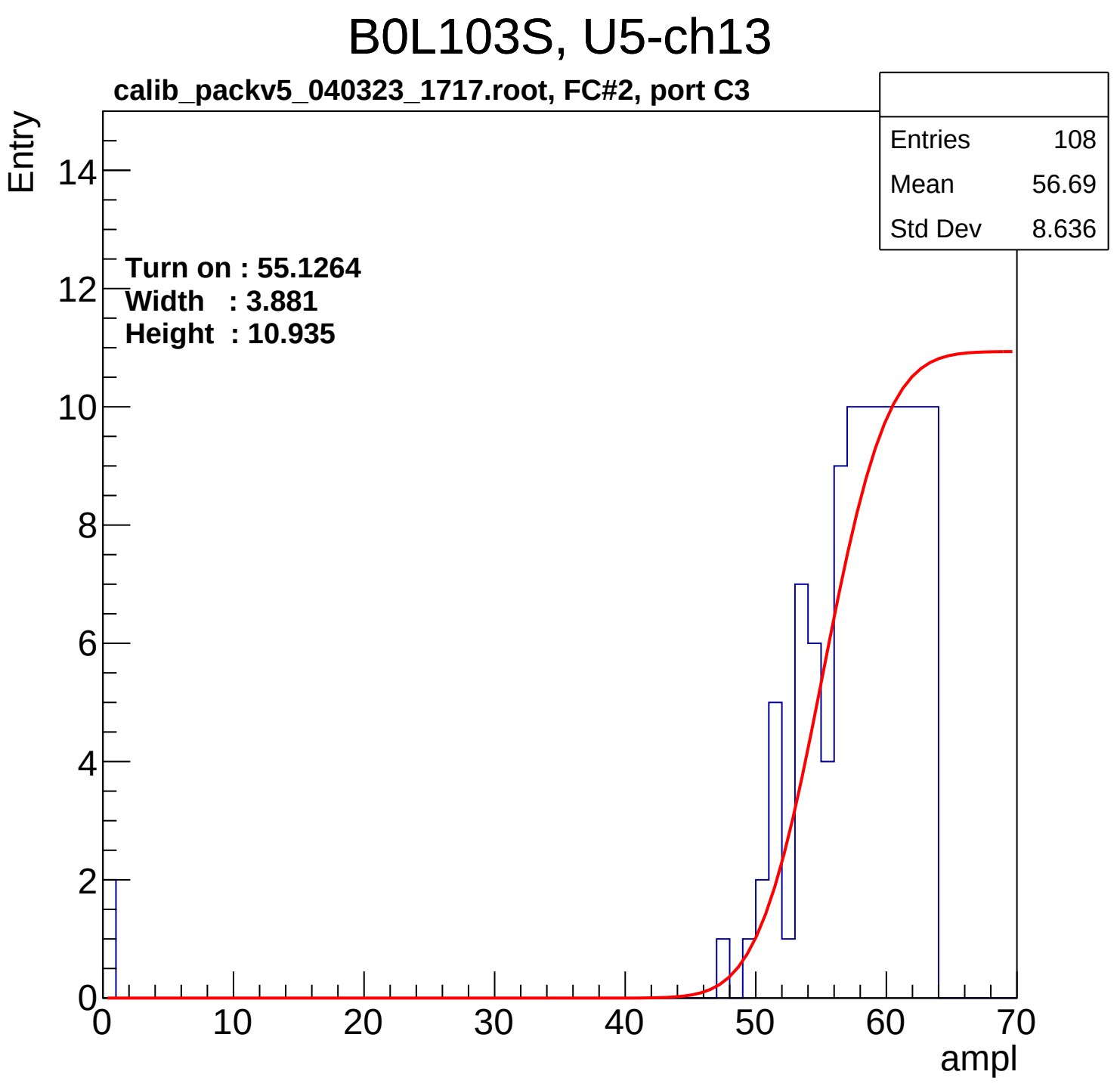
B0L103S, U5-ch13
calib_packv5_040323_1717.root, FC#2, port C3
Entries 108
Mean 56.69
Std Dev 8.636
Turn on : 55.1264
Width : 3.881
Height : 10.935
Entry
ampl
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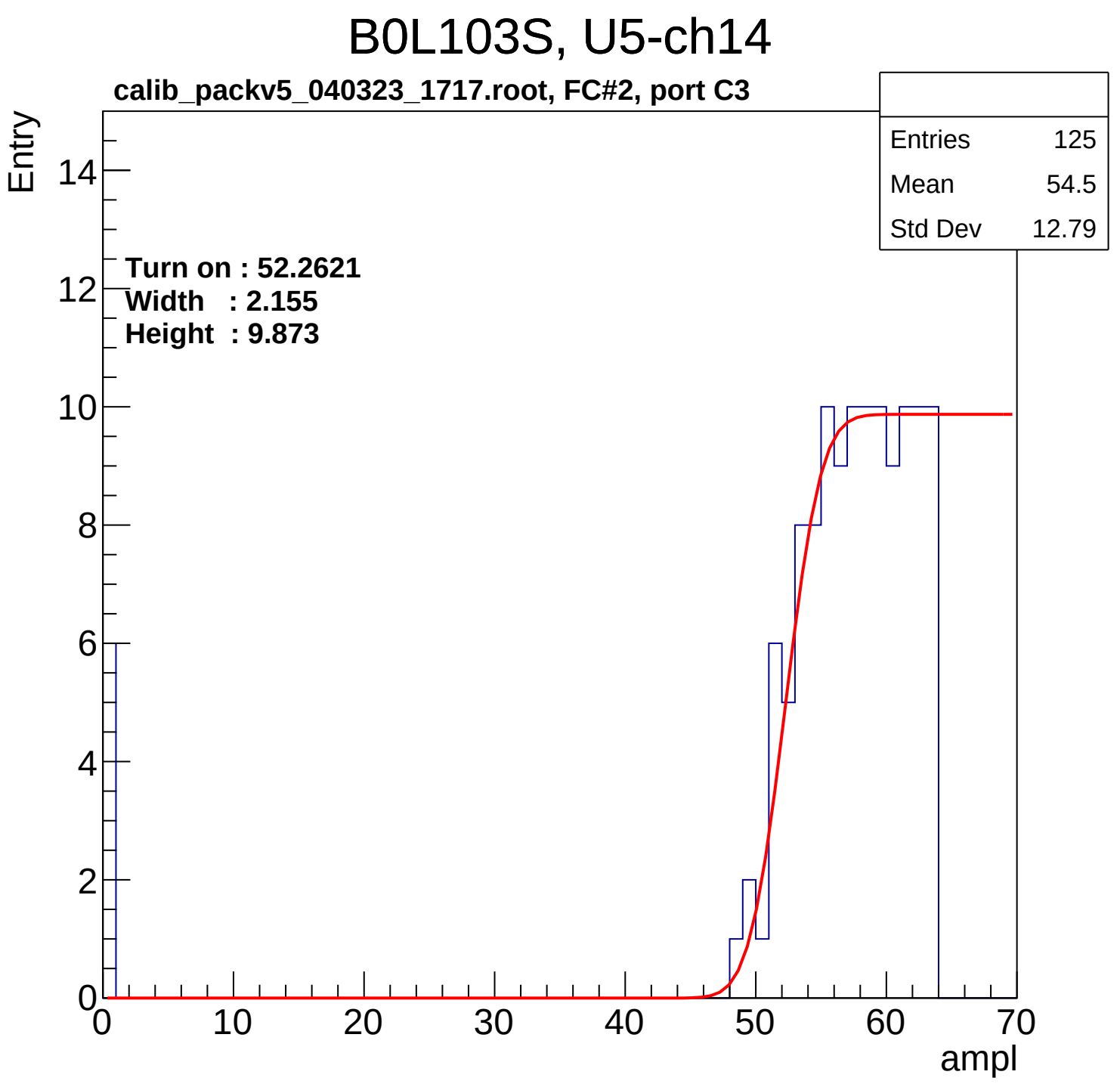
B0L103S, U5-ch14
calib_packv5_040323_1717.root, FC#2, port C3
Entries 125
Mean 54.5
Std Dev 12.79
Turn on : 52.2621
Width : 2.155
Height : 9.873
Entry
ampl
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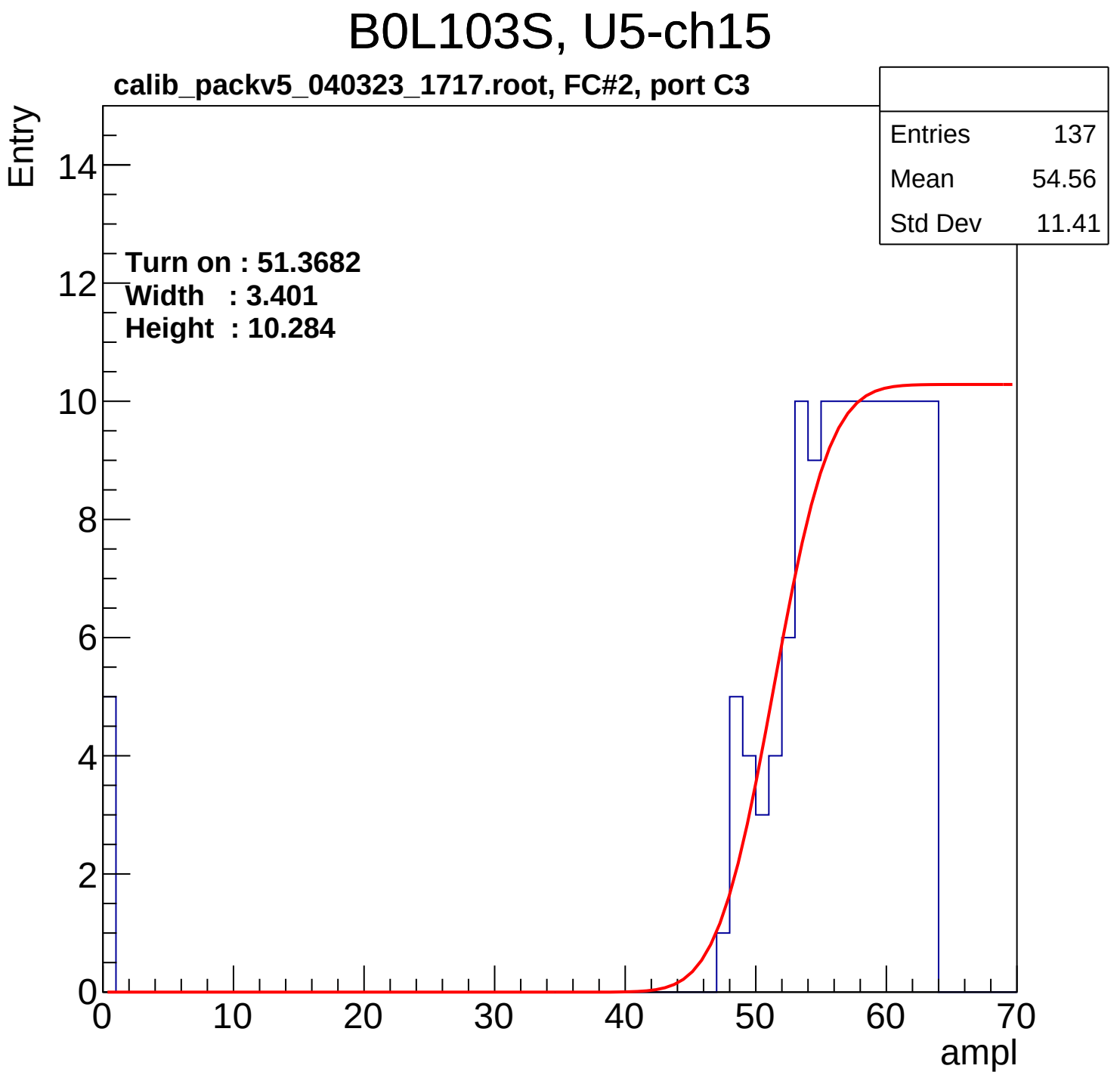
B0L103S, U5-ch15
calib_packv5_040323_1717.root, FC#2, port C3
Entries 137
Mean 54.56
Std Dev 11.41
Turn on : 51.3682
Width : 3.401
Height : 10.284
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ampl
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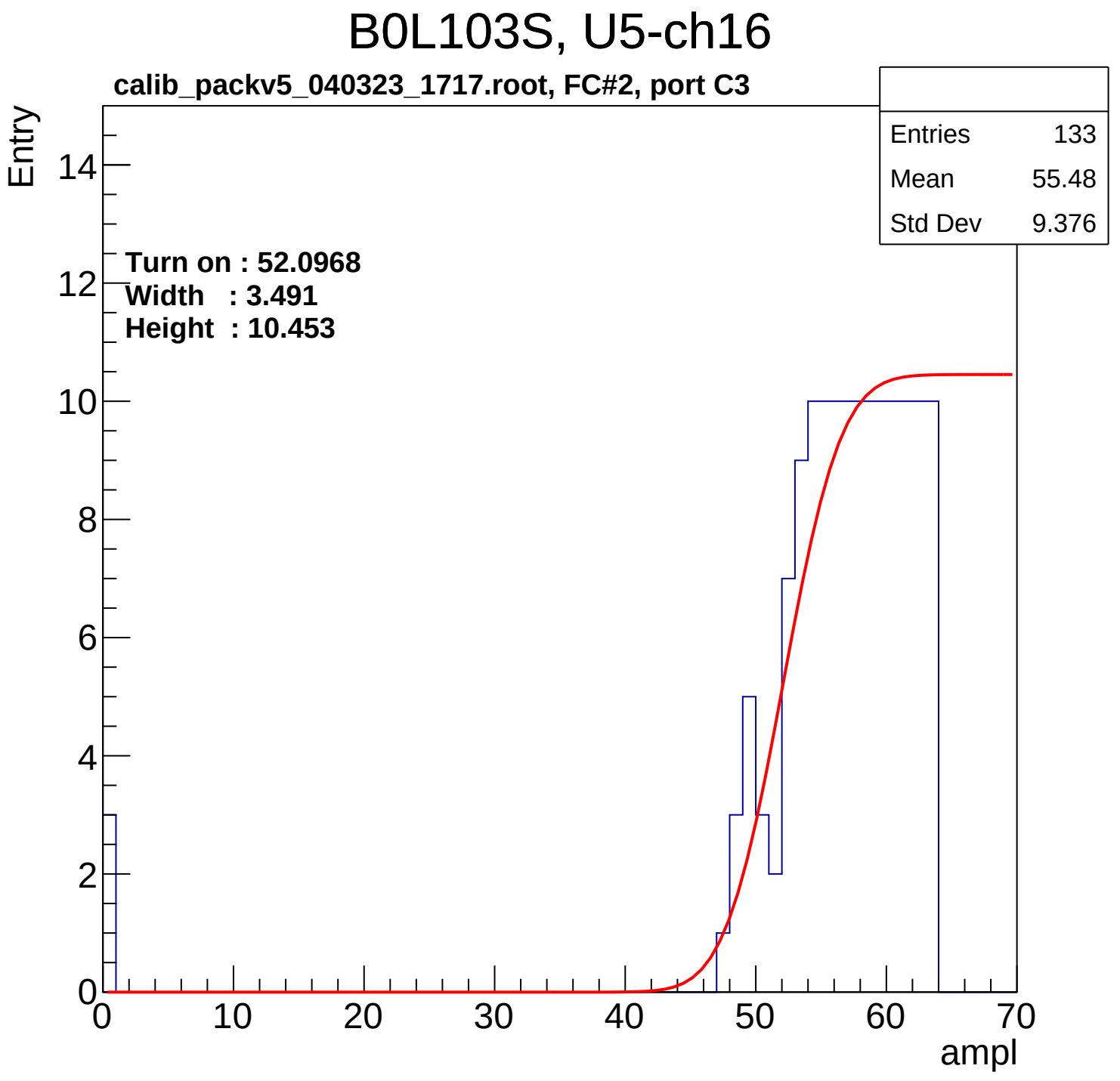
B0L103S, U5-ch16
calib_packv5_040323_1717.root, FC#2, port C3
Entries 133
Mean 55.48
Std Dev 9.376
Turn on : 52.0968
Width : 3.491
Height : 10.453
Entry
ampl
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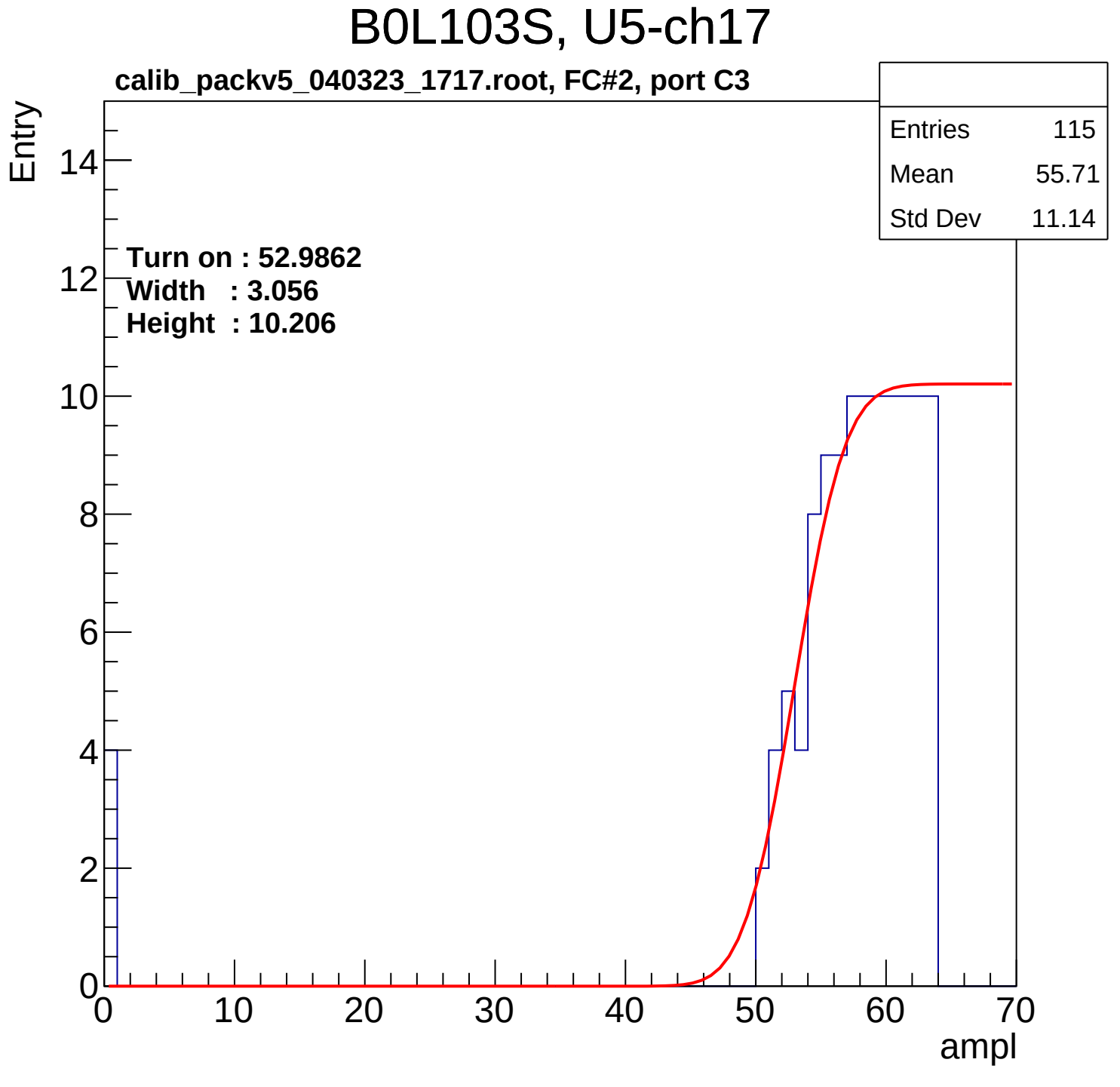
B0L103S, U5-ch17
calib_packv5_040323_1717.root, FC#2, port C3
Entries 115
Mean 55.71
Std Dev 11.14
Turn on : 52.9862
Width : 3.056
Height : 10.206
Entry
ampl
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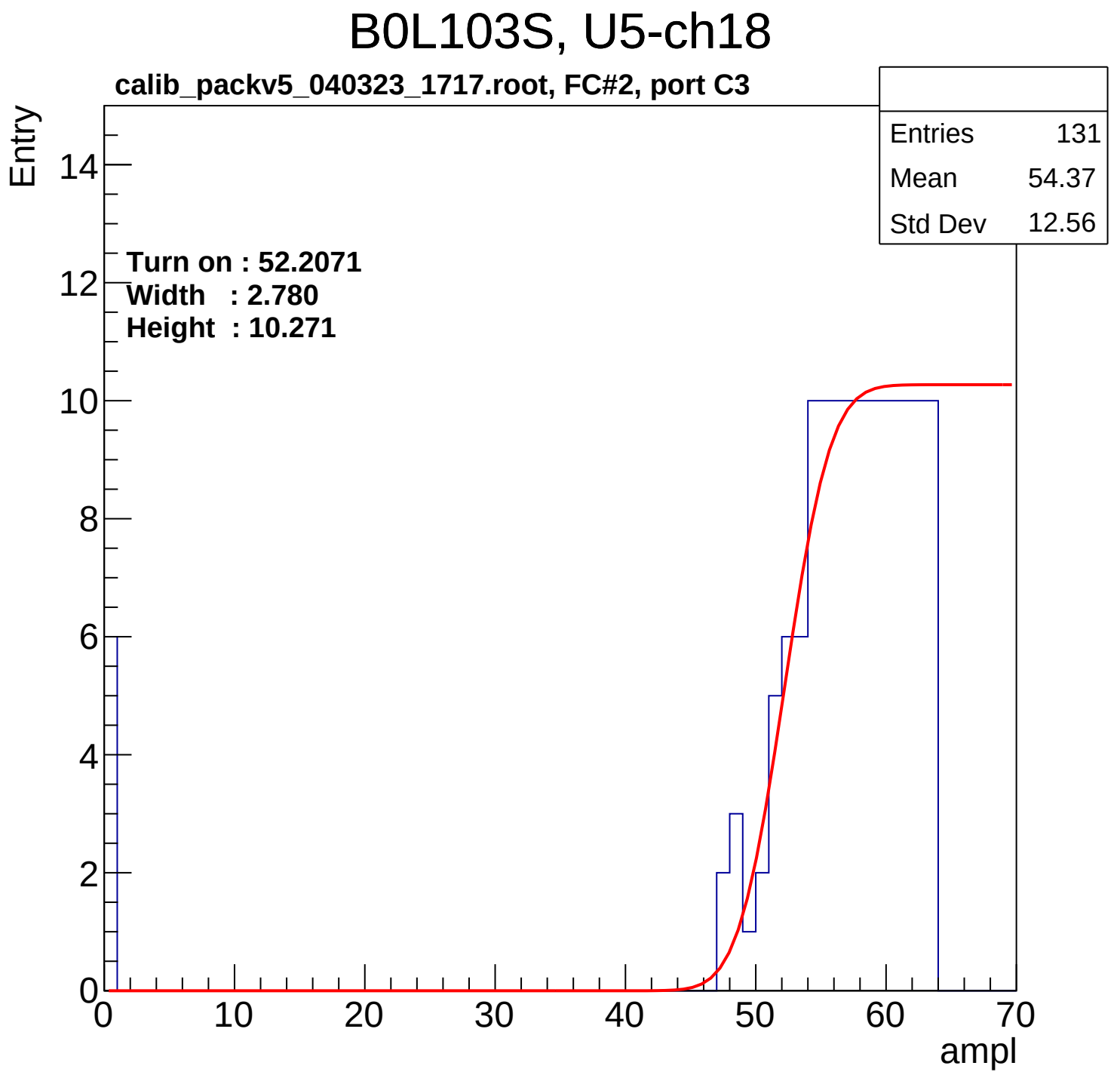
B0L103S, U5-ch18
calib_packv5_040323_1717.root, FC#2, port C3
Entries 131
Mean 54.37
Std Dev 12.56
Turn on : 52.2071
Width : 2.780
Height : 10.271
Entry
ampl
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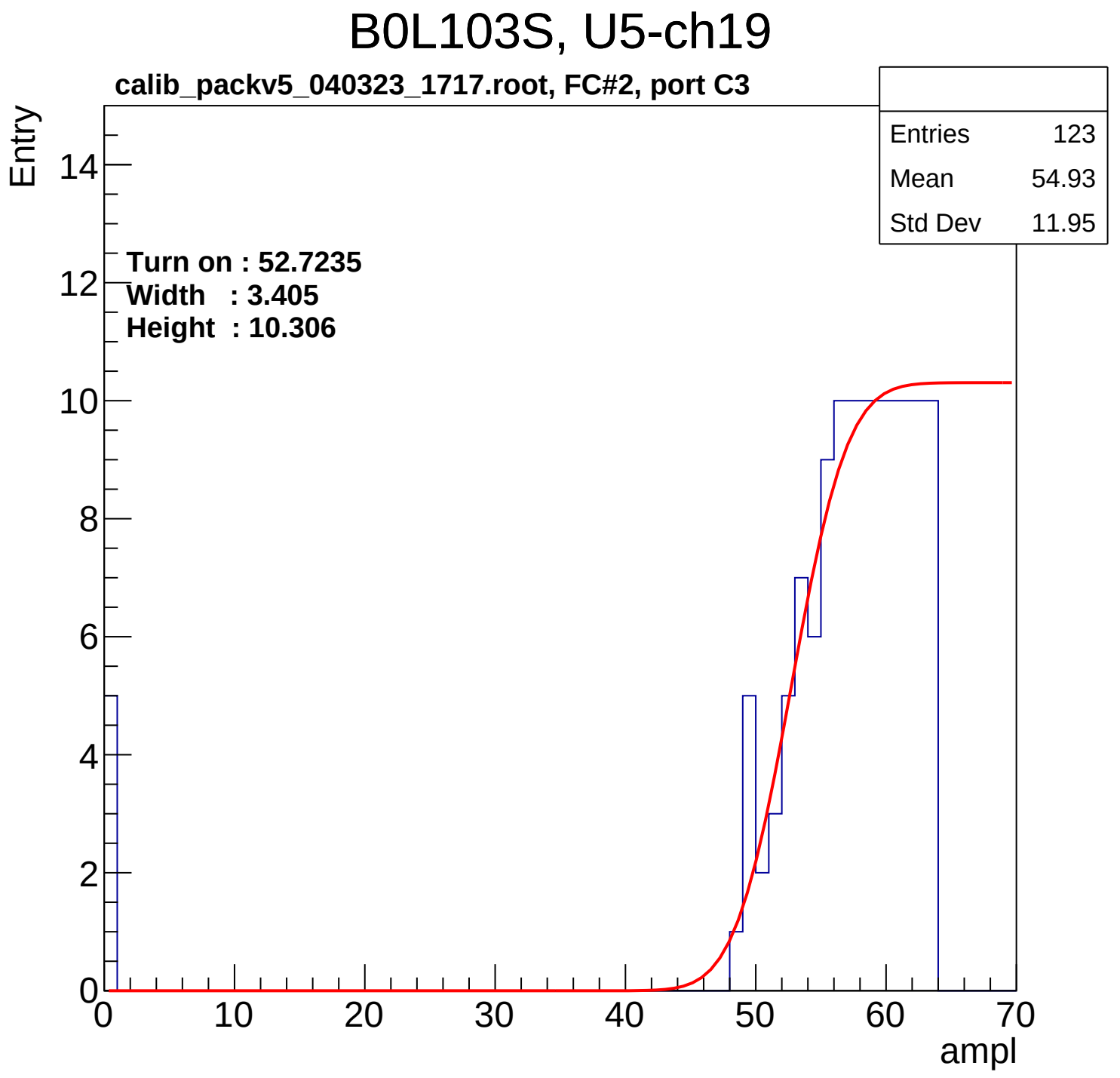
B0L103S, U5-ch19
calib_packv5_040323_1717.root, FC#2, port C3
Entries 123
Mean 54.93
Std Dev 11.95
Turn on : 52.7235
Width : 3.405
Height : 10.306
Entry
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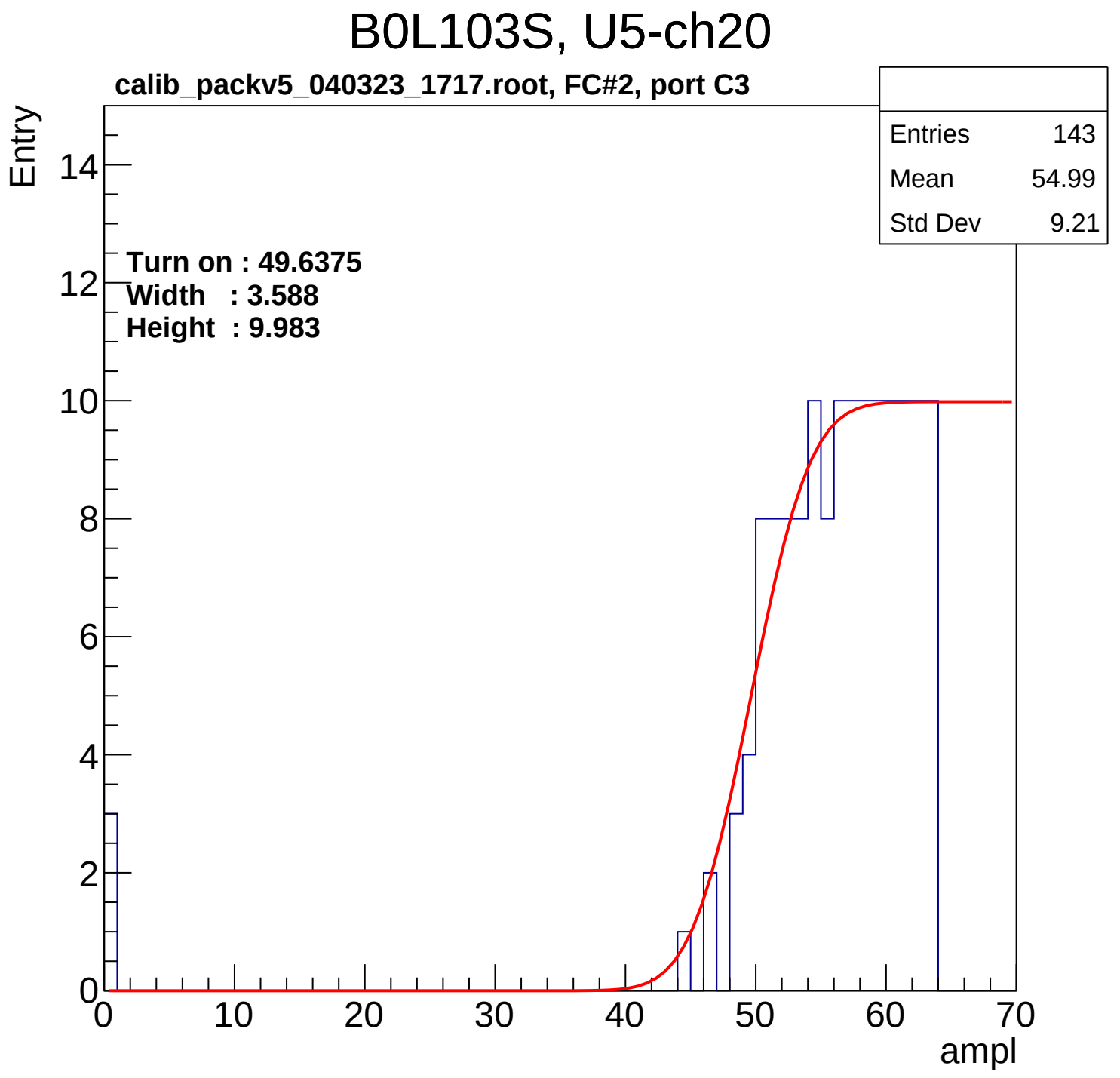
B0L103S, U5-ch20
calib_packv5_040323_1717.root, FC#2, port C3
Entries 143
Mean 54.99
Std Dev 9.21
Turn on : 49.6375
Width : 3.588
Height : 9.983
Entry
ampl
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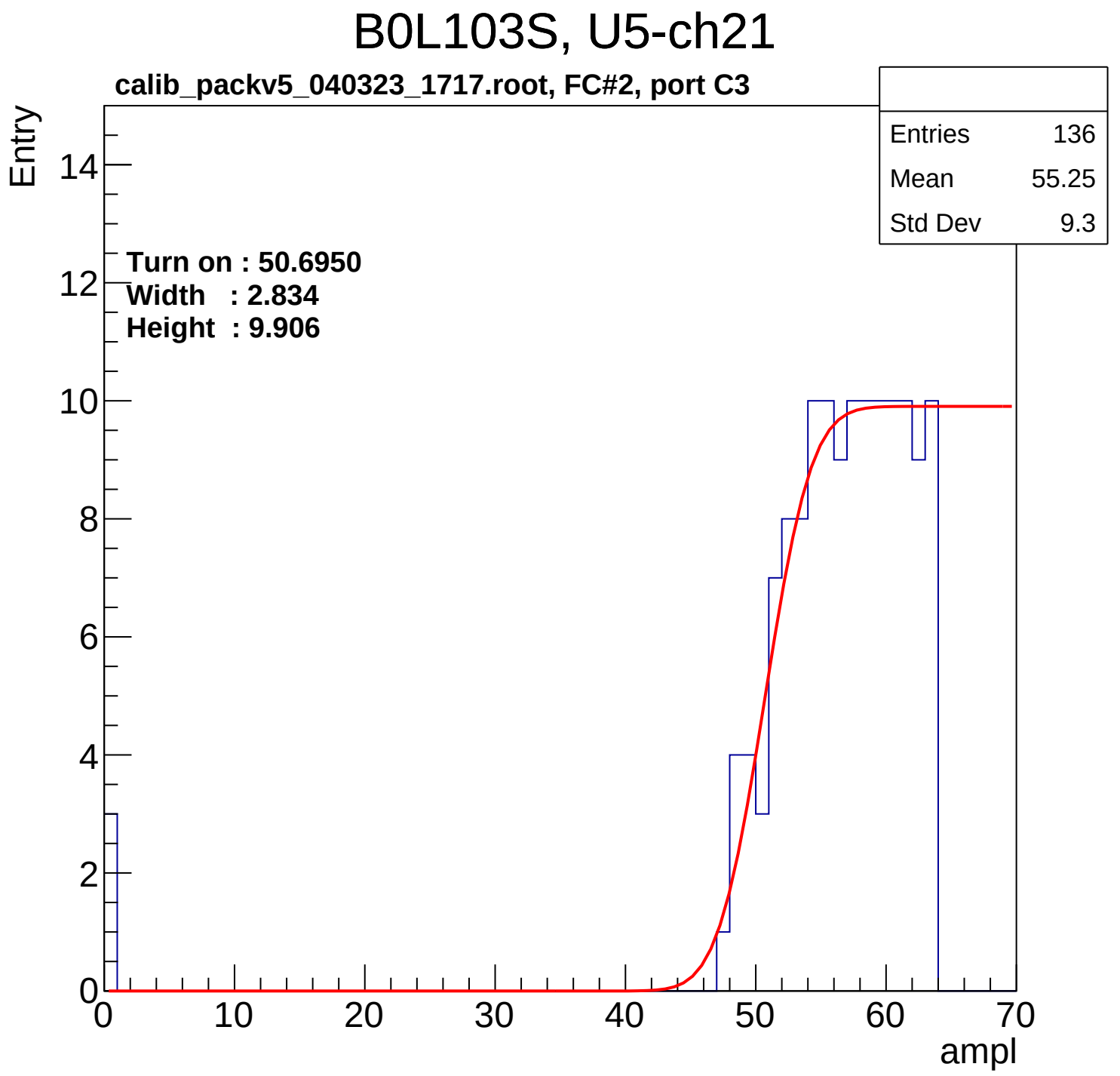
B0L103S, U5-ch21
calib_packv5_040323_1717.root, FC#2, port C3
Entries 136
Mean 55.25
Std Dev 9.3
Turn on : 50.6950
Width : 2.834
Height : 9.906
Entry
ampl
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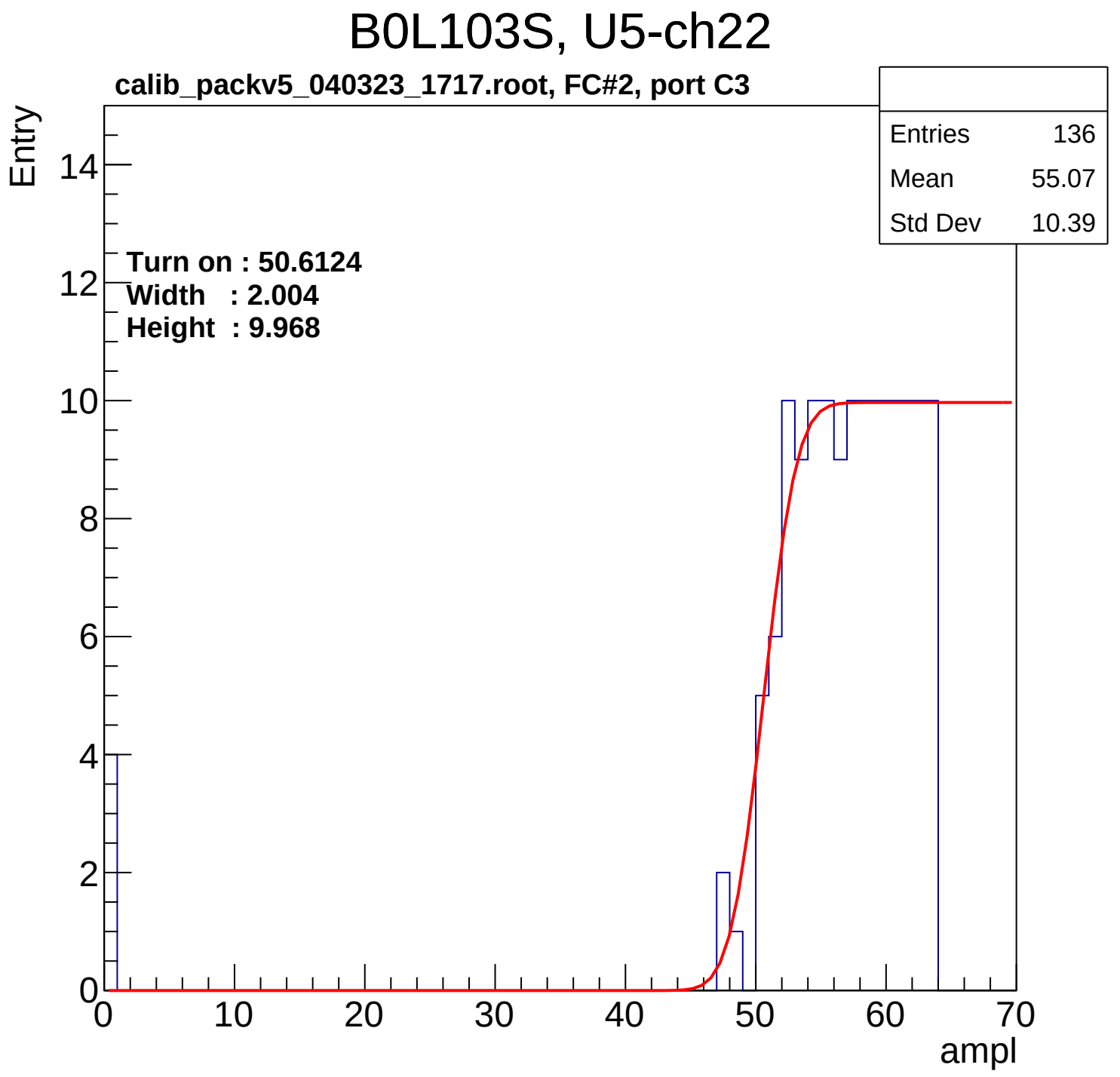
B0L103S, U5-ch22
calib_packv5_040323_1717.root, FC#2, port C3
Entries 136
Mean 55.07
Std Dev 10.39
Turn on : 50.6124
Width : 2.004
Height : 9.968
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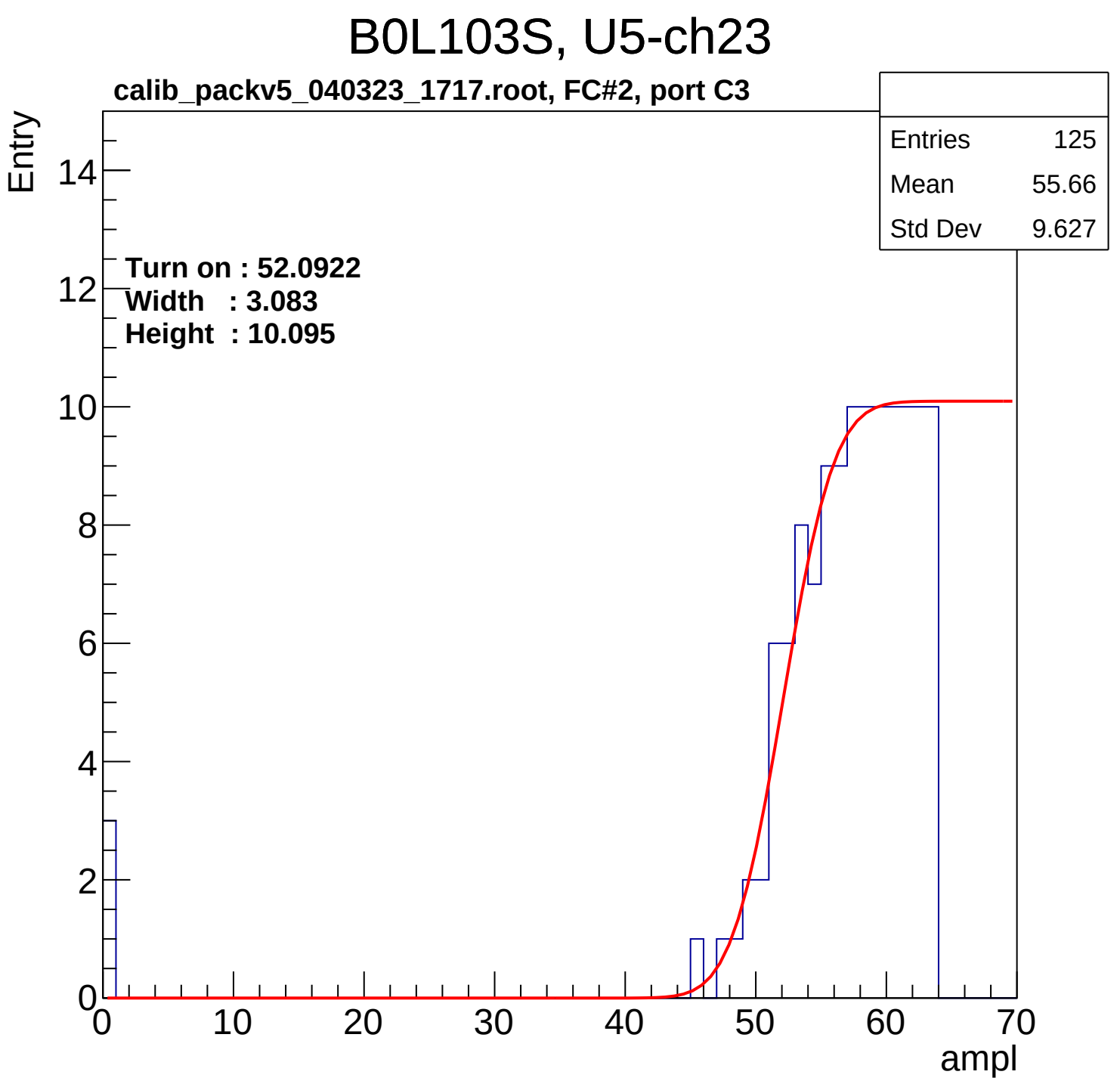
B0L103S, U5-ch23
calib_packv5_040323_1717.root, FC#2, port C3
Entries 125
Mean 55.66
Std Dev 9.627
Turn on : 52.0922
Width : 3.083
Height : 10.095
Entry
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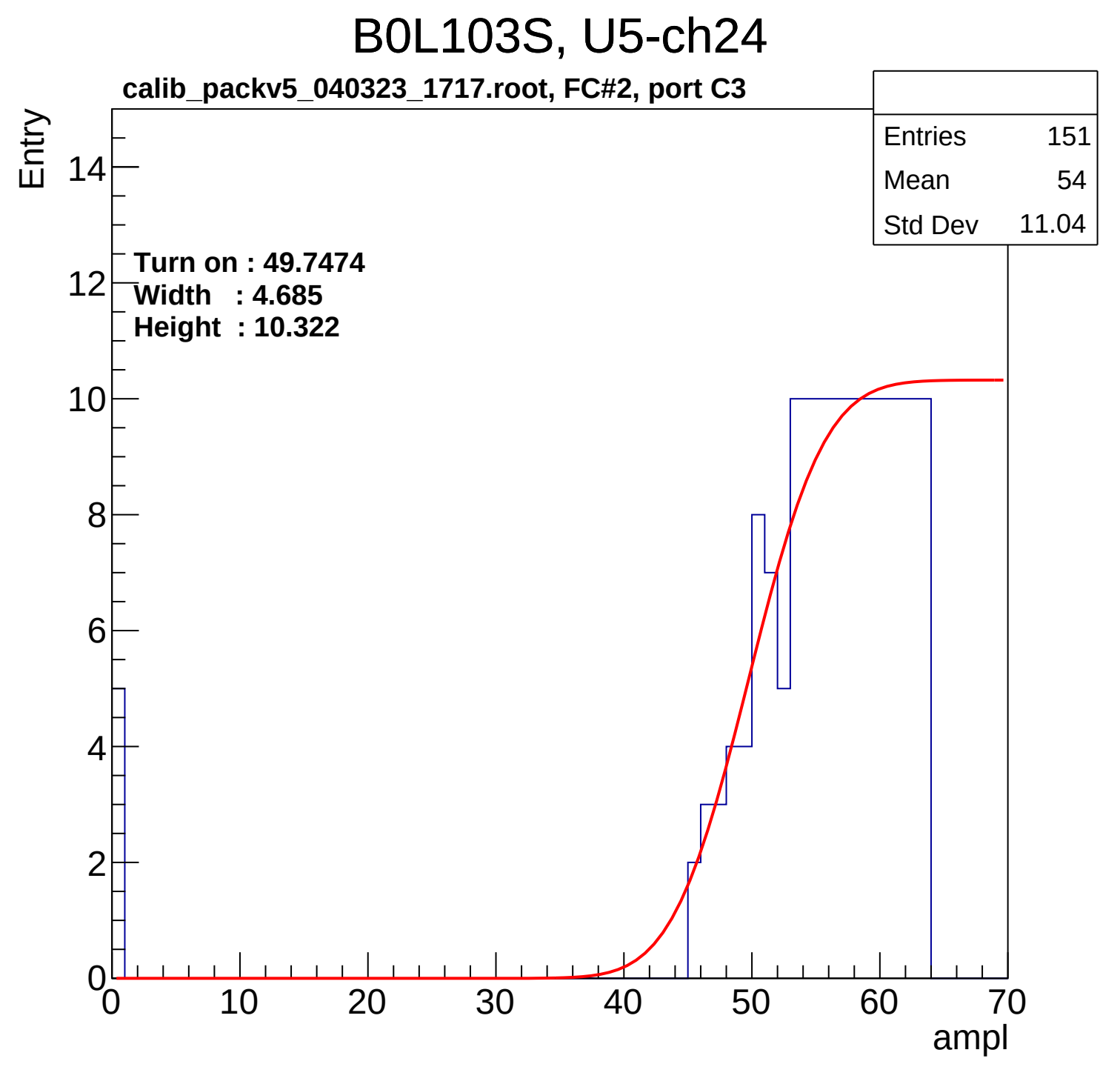
B0L103S, U5-ch24
calib_packv5_040323_1717.root, FC#2, port C3
Entries 151
Mean 54
Std Dev 11.04
Turn on : 49.7474
Width : 4.685
Height : 10.322
Entry
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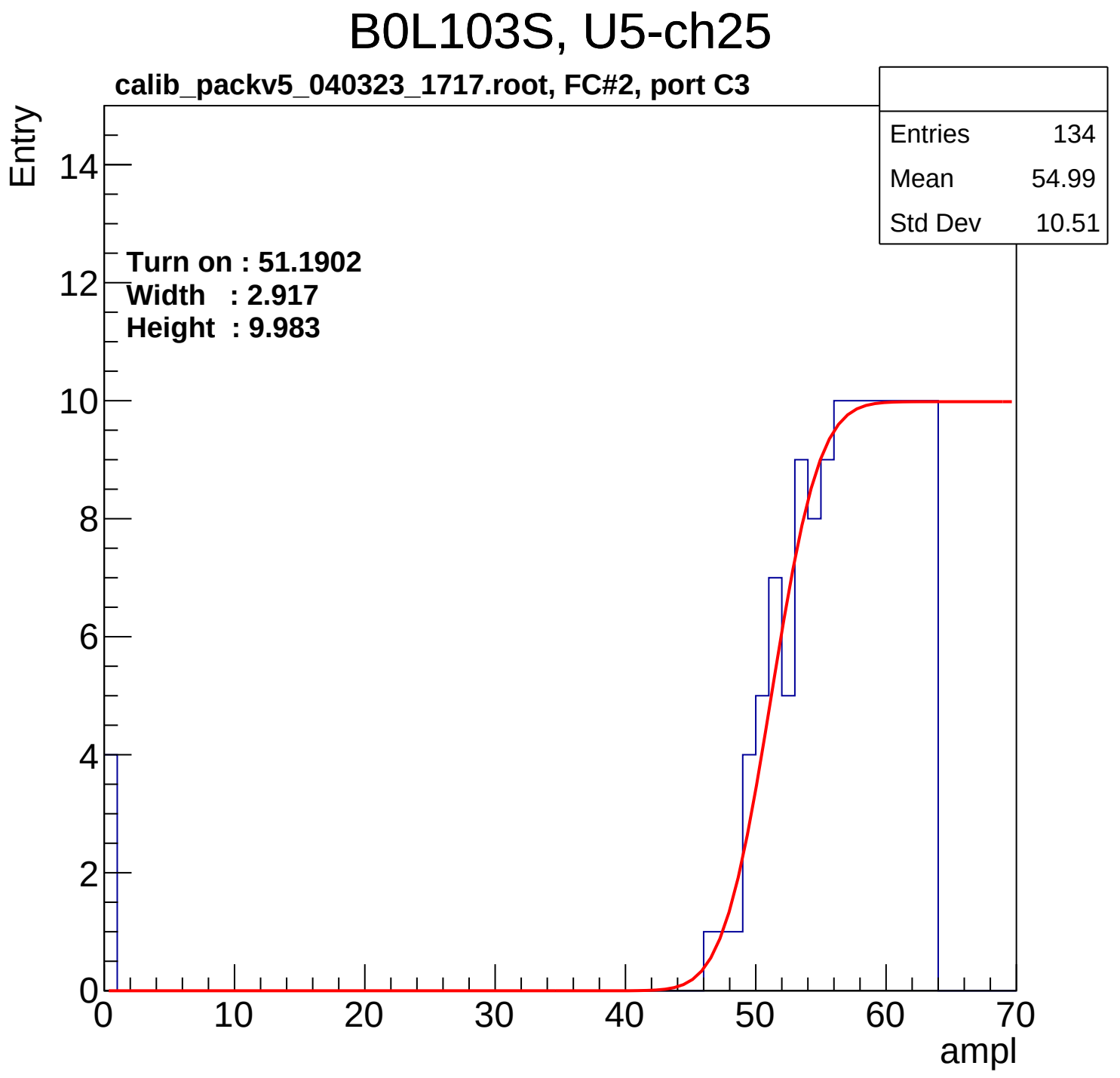
B0L103S, U5-ch25
calib_packv5_040323_1717.root, FC#2, port C3
Entries 134
Mean 54.99
Std Dev 10.51
Turn on : 51.1902
Width : 2.917
Height : 9.983
Entry
ampl
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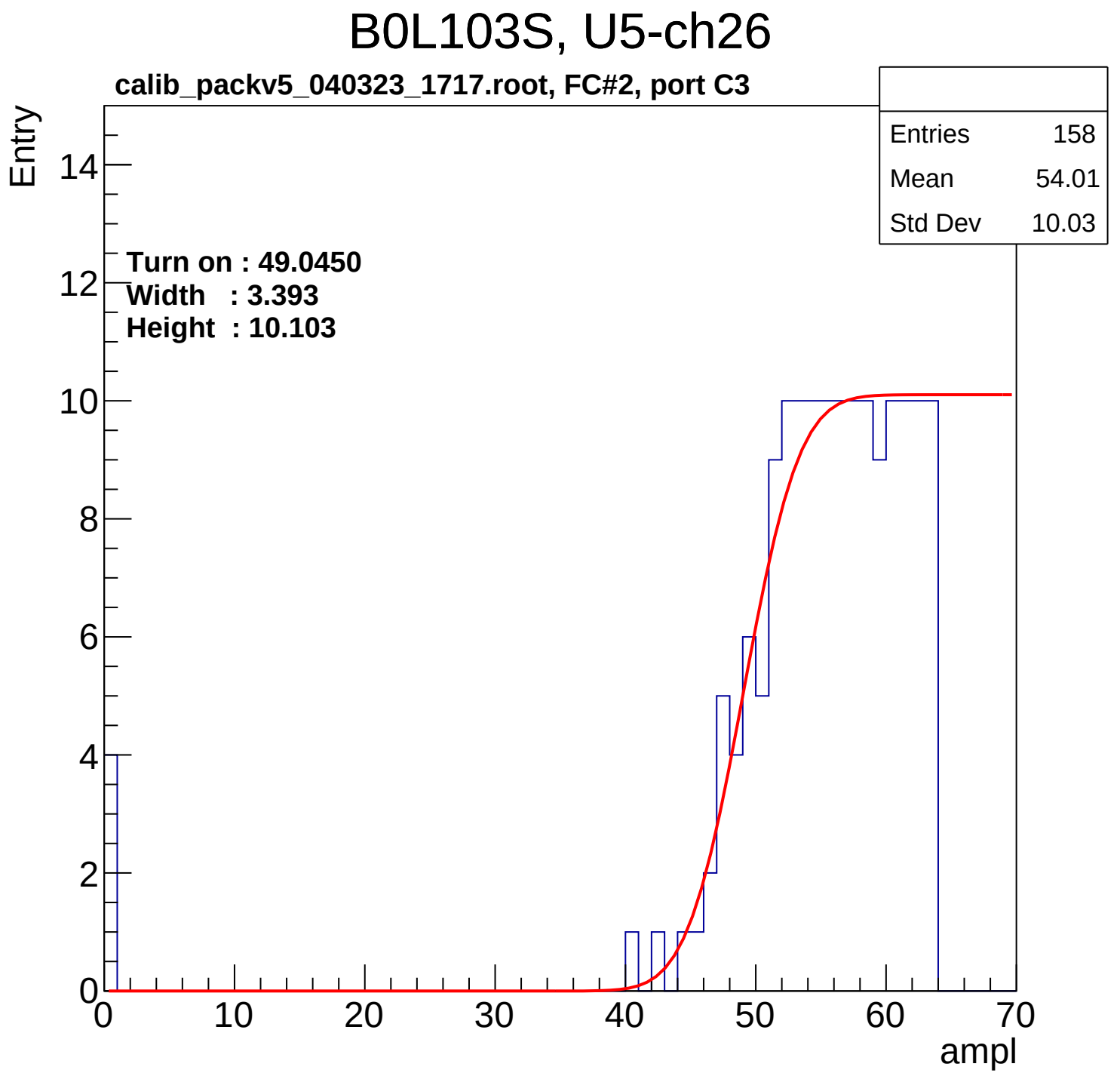
B0L103S, U5-ch26
calib_packv5_040323_1717.root, FC#2, port C3
Entries 158
Mean 54.01
Std Dev 10.03
Turn on : 49.0450
Width : 3.393
Height : 10.103
Entry
ampl
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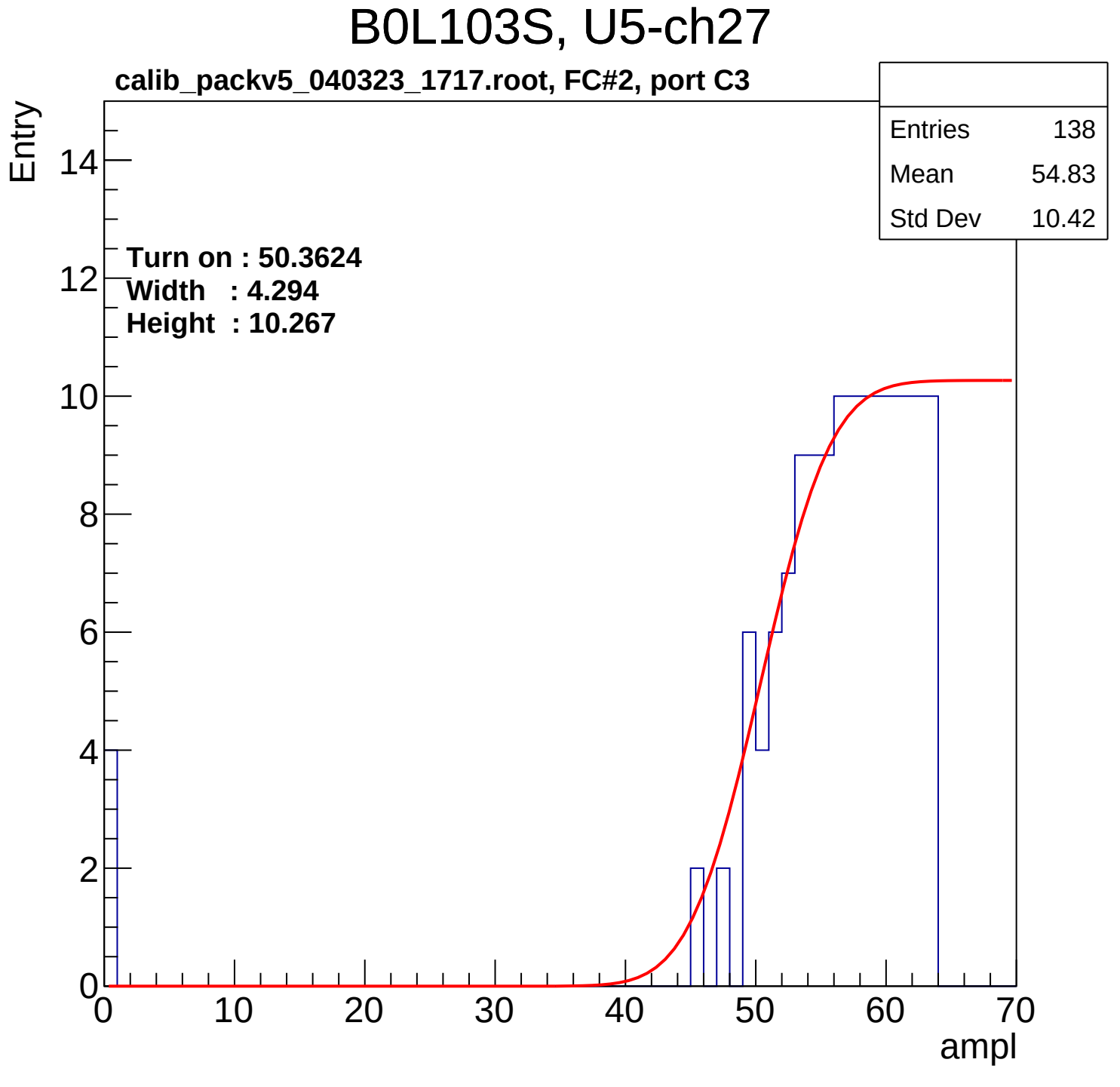
B0L103S, U5-ch27
calib_packv5_040323_1717.root, FC#2, port C3
Entries 138
Mean 54.83
Std Dev 10.42
Turn on : 50.3624
Width : 4.294
Height : 10.267
Entry
ampl
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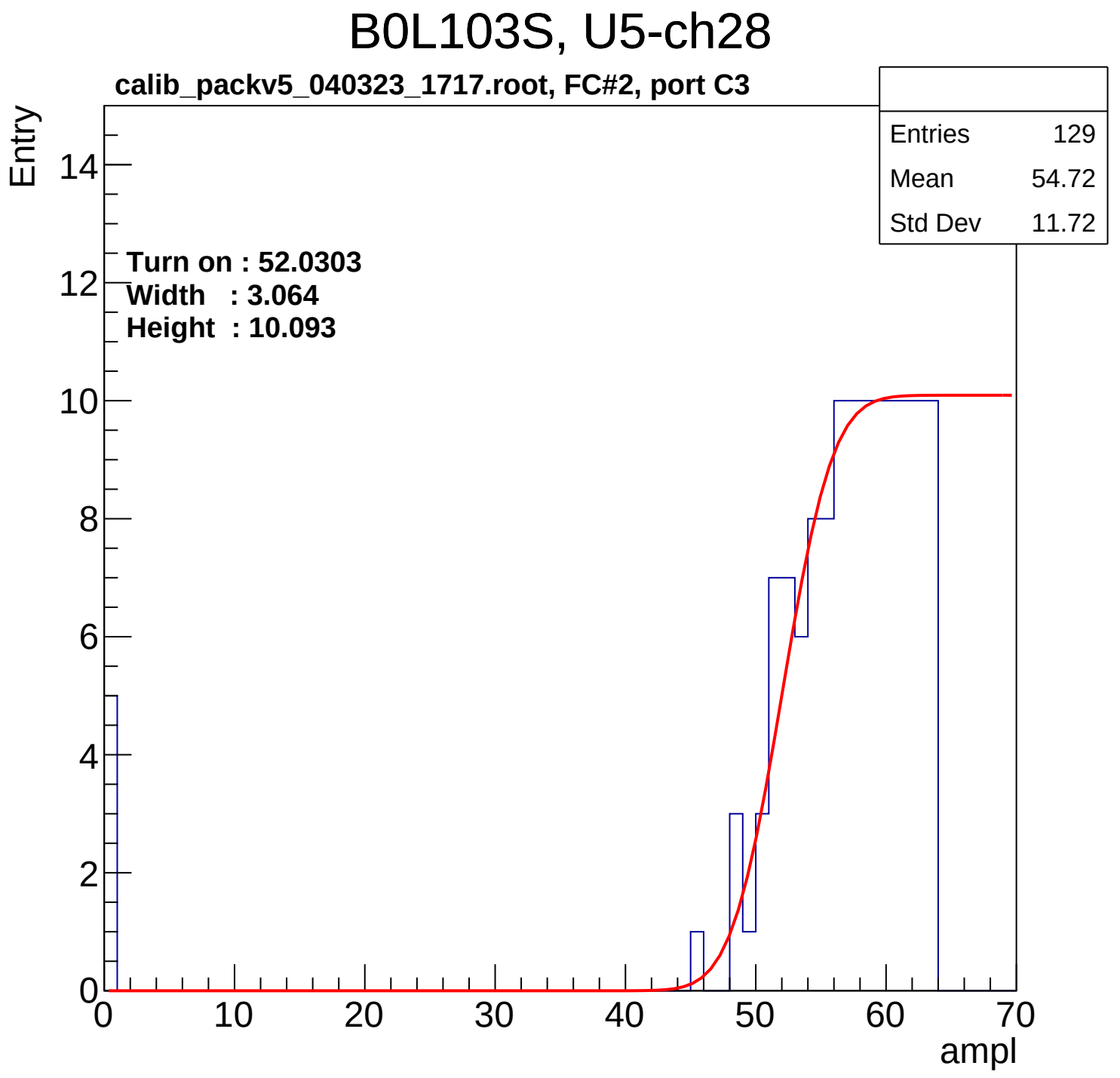
B0L103S, U5-ch28
calib_packv5_040323_1717.root, FC#2, port C3
Entries 129
Mean 54.72
Std Dev 11.72
Turn on : 52.0303
Width : 3.064
Height : 10.093
Entry
ampl
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20
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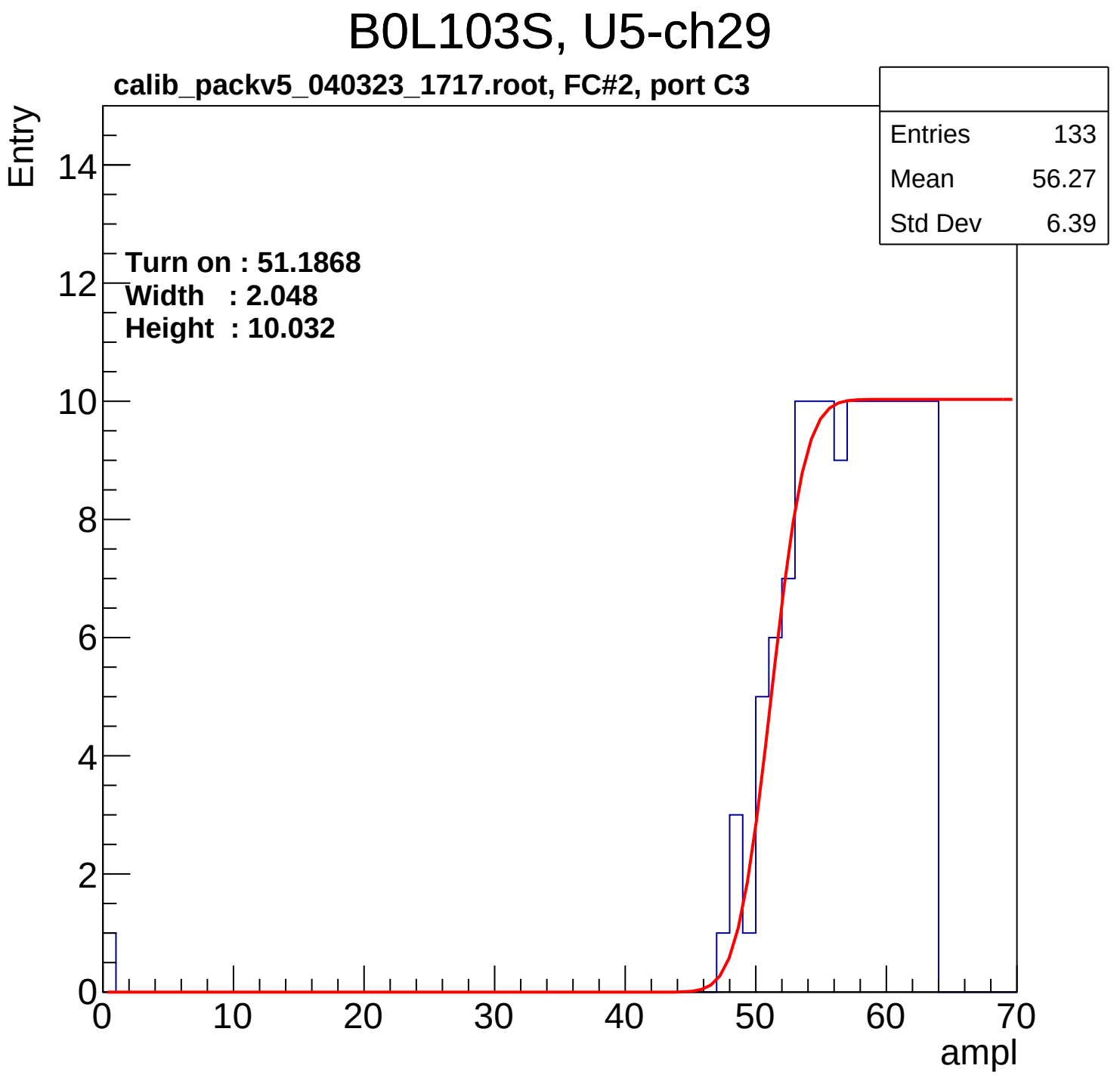
B0L103S, U5-ch29
calib_packv5_040323_1717.root, FC#2, port C3
Entries 133
Mean 56.27
Std Dev 6.39
Turn on : 51.1868
Width : 2.048
Height : 10.032
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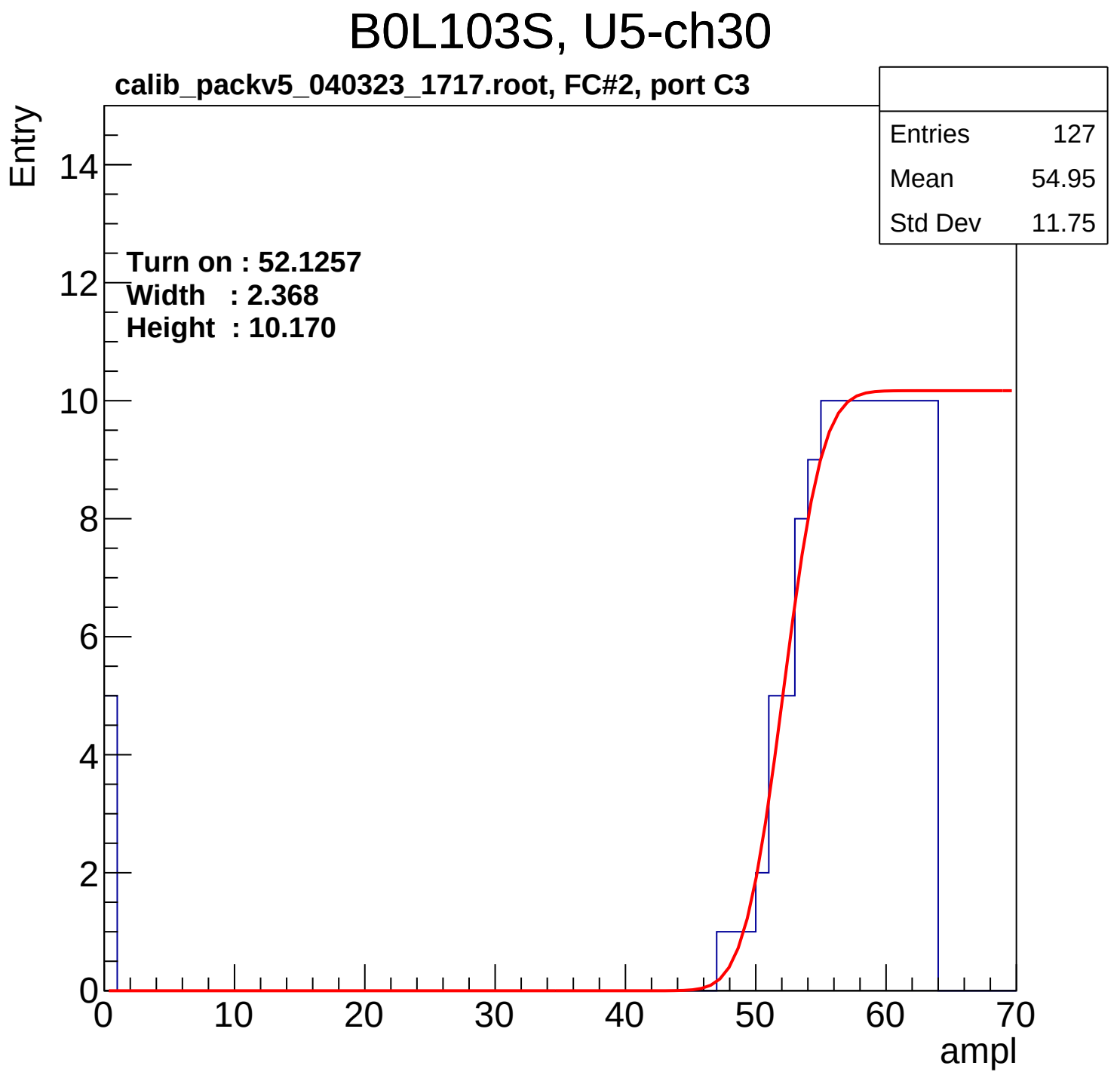
B0L103S, U5-ch30
calib_packv5_040323_1717.root, FC#2, port C3
Entries 127
Mean 54.95
Std Dev 11.75
Turn on : 52.1257
Width : 2.368
Height : 10.170
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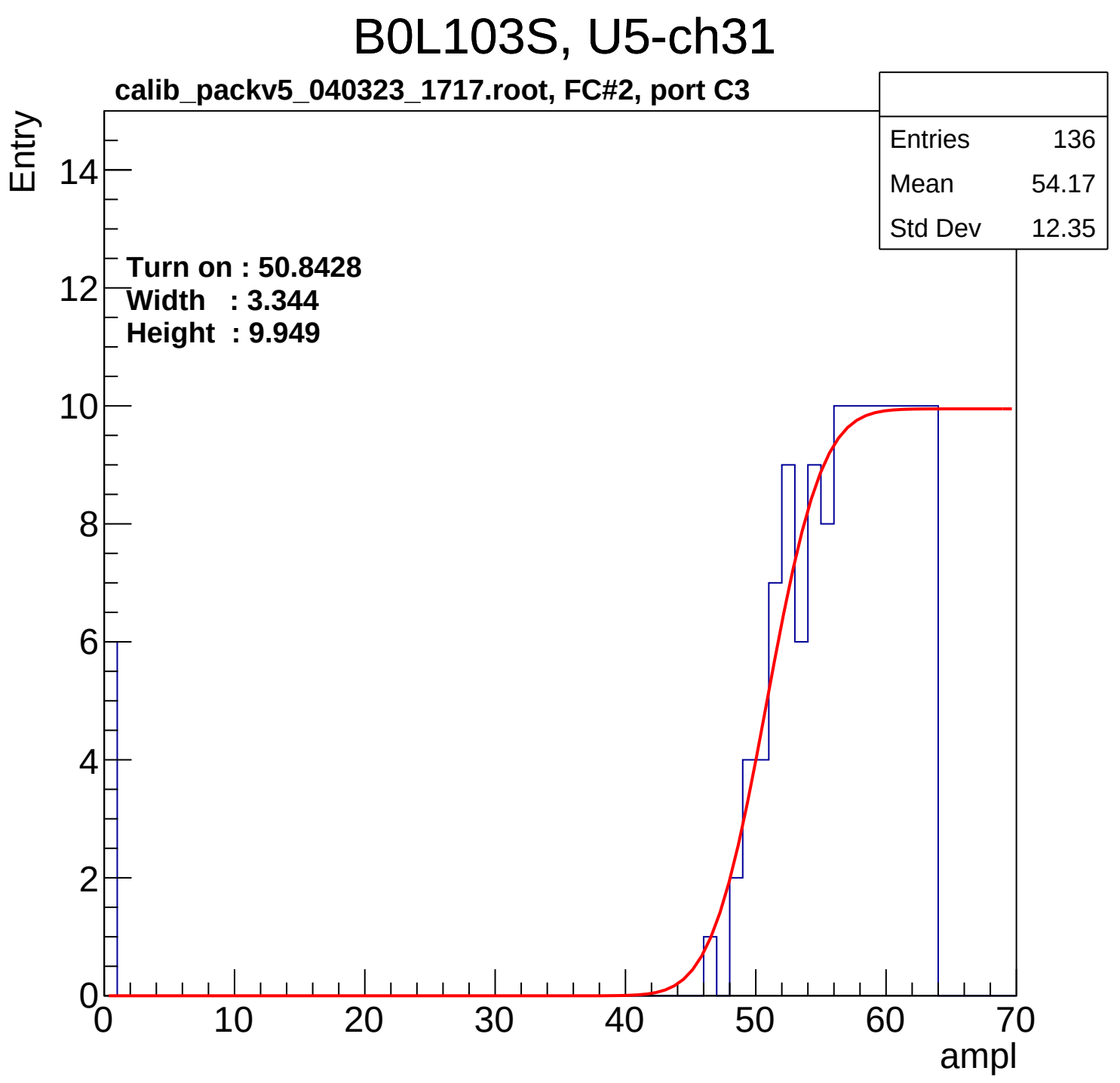
B0L103S, U5-ch31
calib_packv5_040323_1717.root, FC#2, port C3
Entries 136
Mean 54.17
Std Dev 12.35
Turn on : 50.8428
Width : 3.344
Height : 9.949
Entry
ampl
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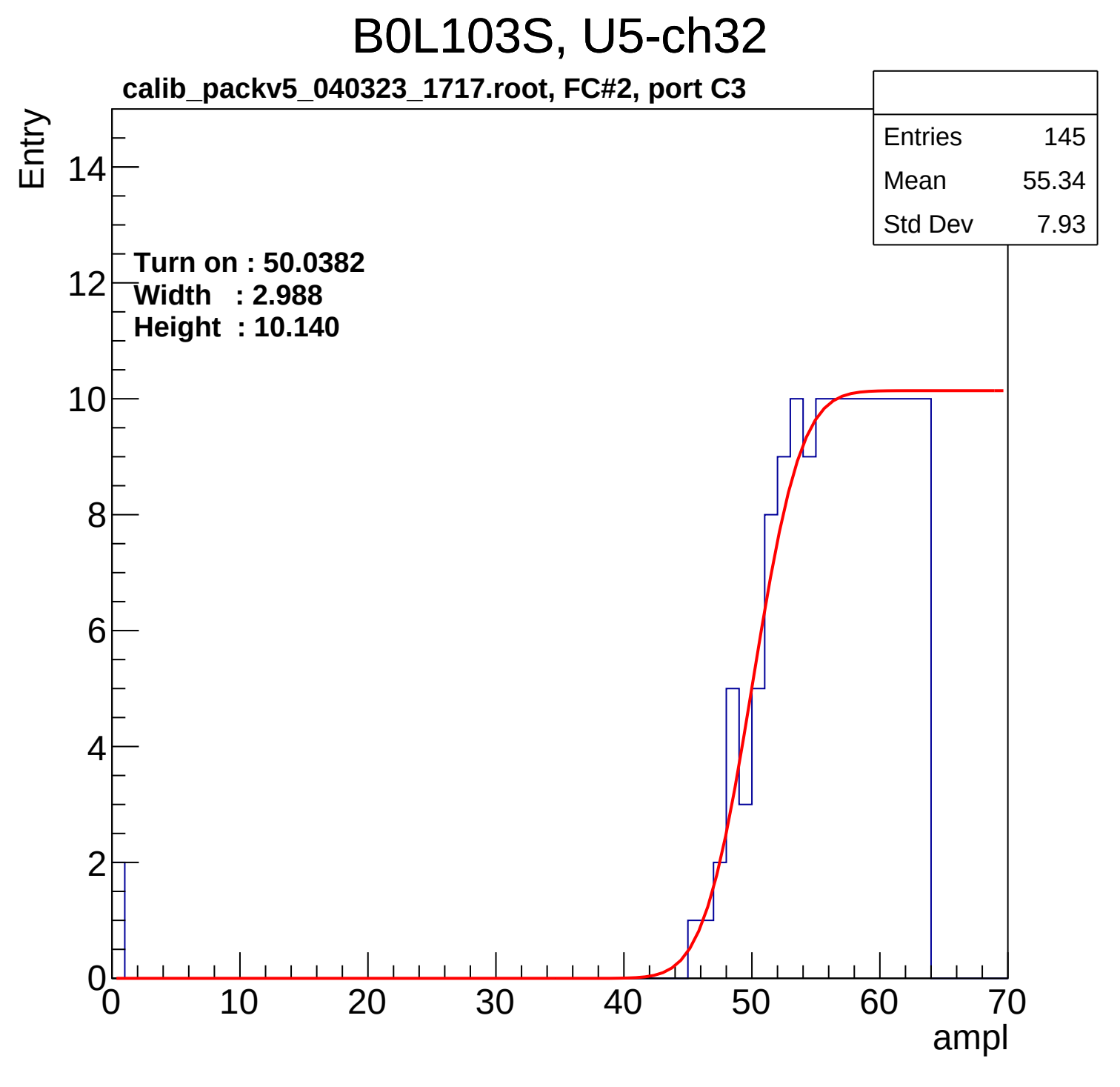
B0L103S, U5-ch32
calib_packv5_040323_1717.root, FC#2, port C3
Entries 145
Mean 55.34
Std Dev 7.93
Turn on : 50.0382
Width : 2.988
Height : 10.140
Entry
ampl
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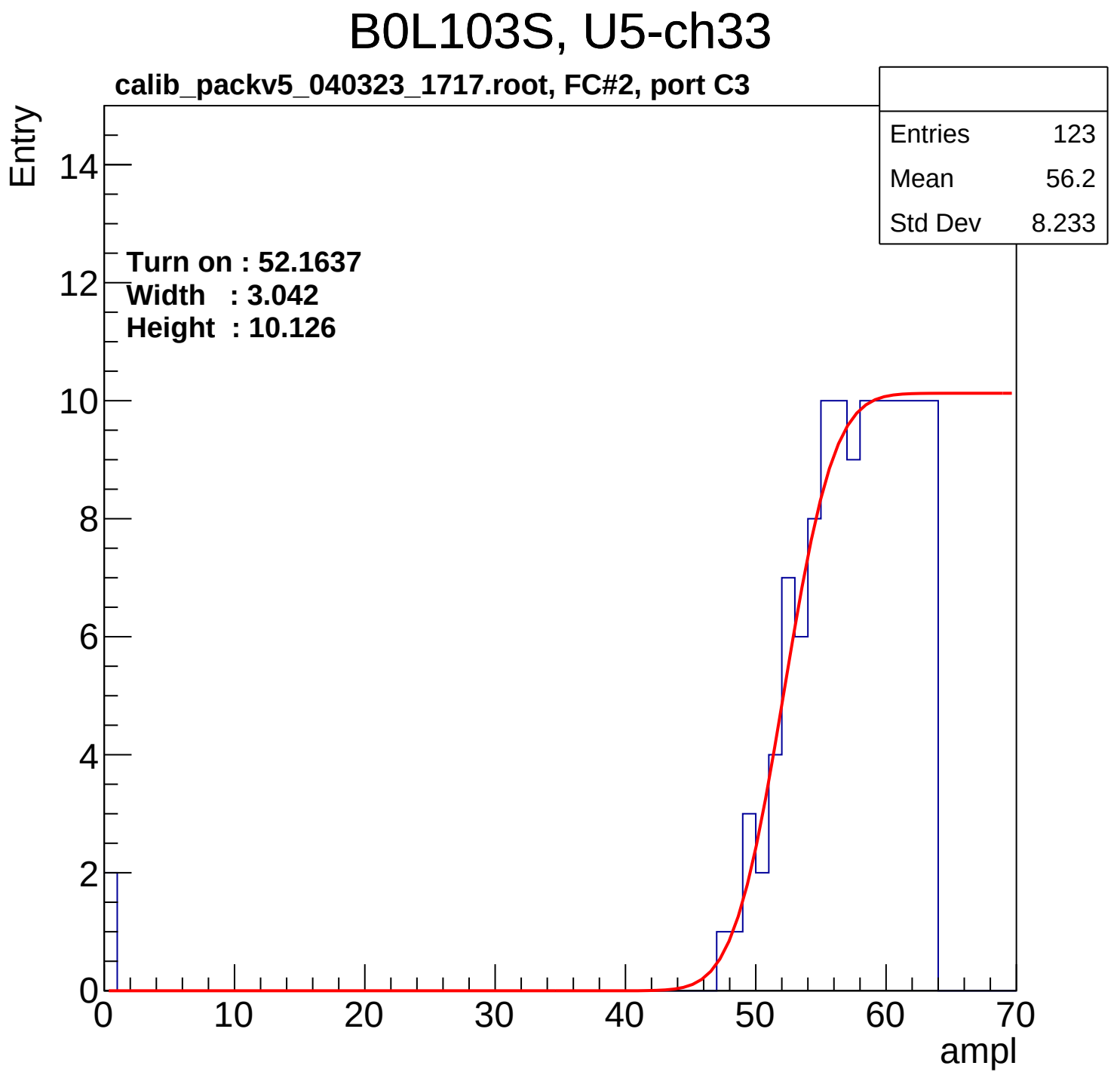
B0L103S, U5-ch33
calib_packv5_040323_1717.root, FC#2, port C3
Entries 123
Mean 56.2
Std Dev 8.233
Turn on : 52.1637
Width : 3.042
Height : 10.126
Entry
ampl
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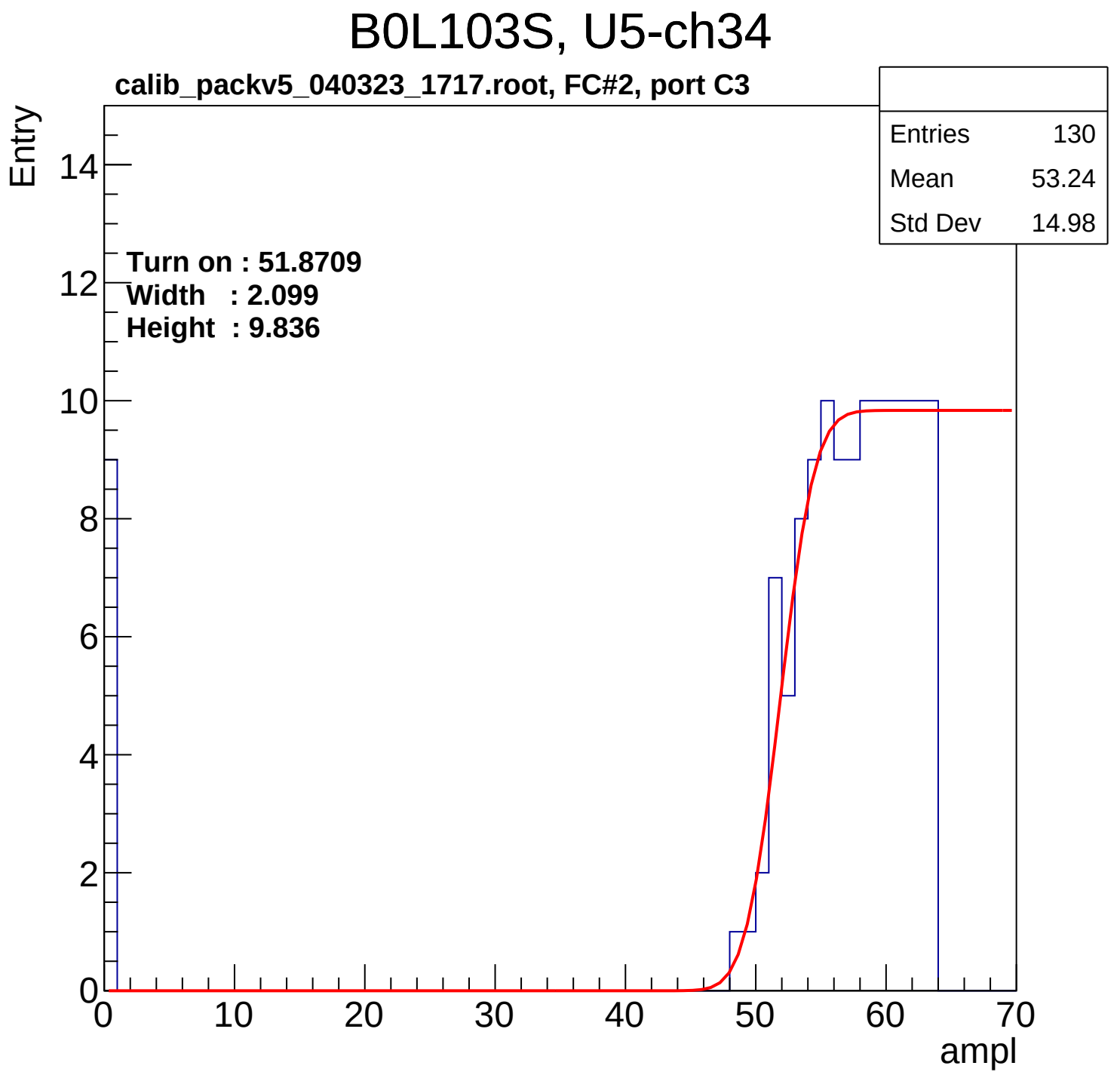
B0L103S, U5-ch34
calib_packv5_040323_1717.root, FC#2, port C3
Entries 130
Mean 53.24
Std Dev 14.98
Turn on : 51.8709
Width : 2.099
Height : 9.836
Entry
ampl
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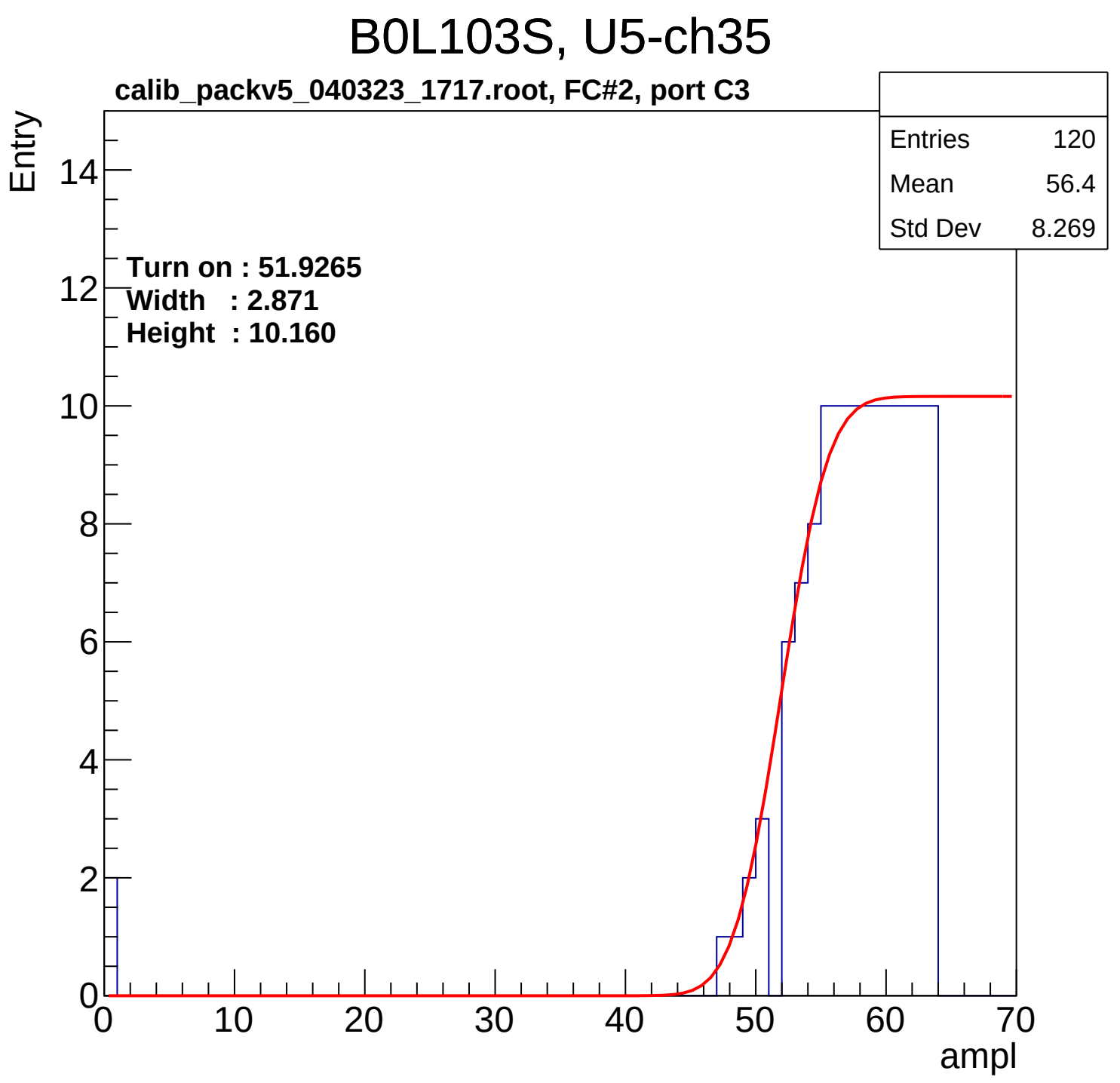
B0L103S, U5-ch35
calib_packv5_040323_1717.root, FC#2, port C3
Entries 120
Mean 56.4
Std Dev 8.269
Turn on : 51.9265
Width : 2.871
Height : 10.160
Entry
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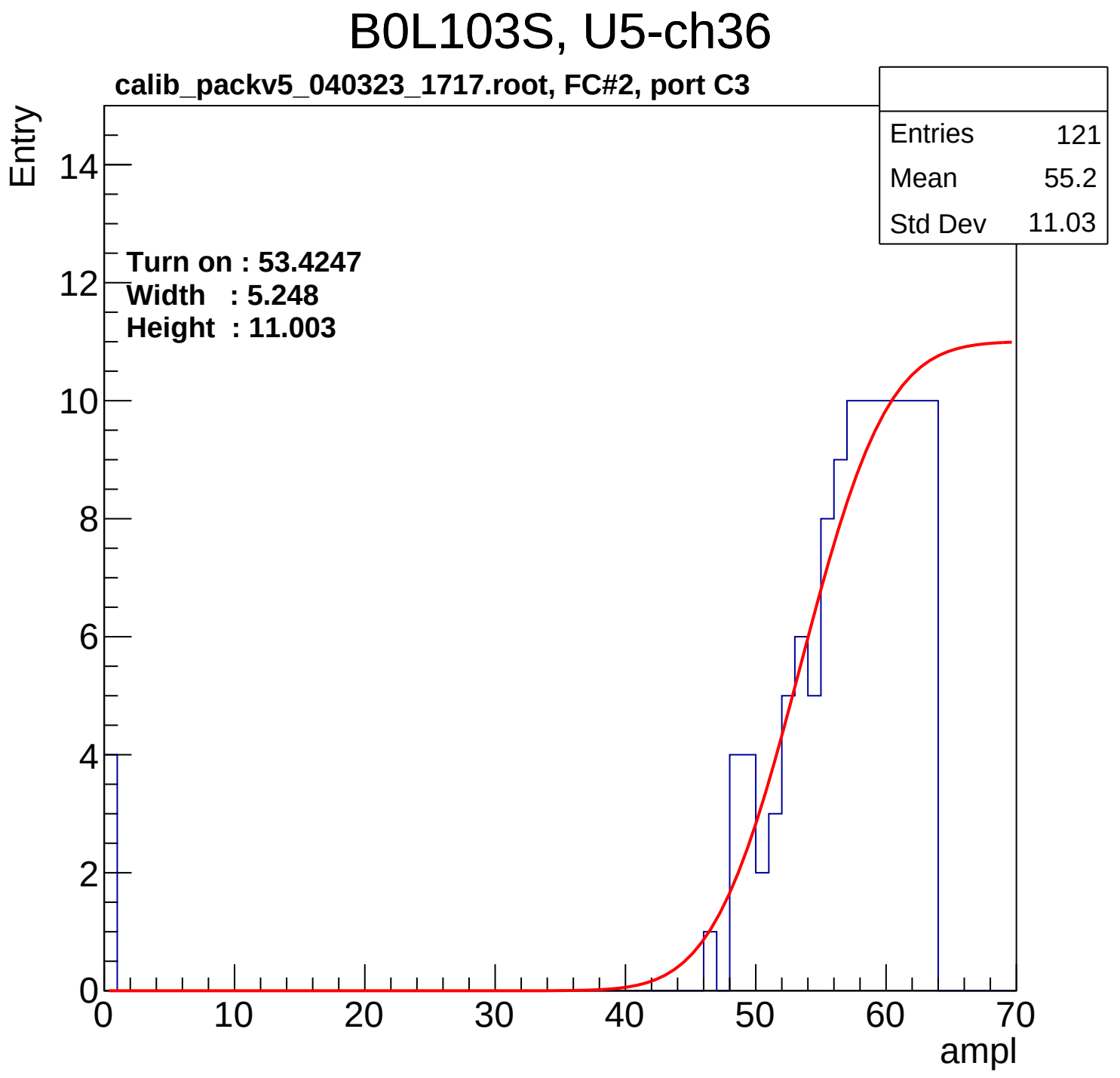
B0L103S, U5-ch36
calib_packv5_040323_1717.root, FC#2, port C3
Entries 121
Mean 55.2
Std Dev 11.03
Turn on : 53.4247
Width : 5.248
Height : 11.003
Entry
ampl
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6
8
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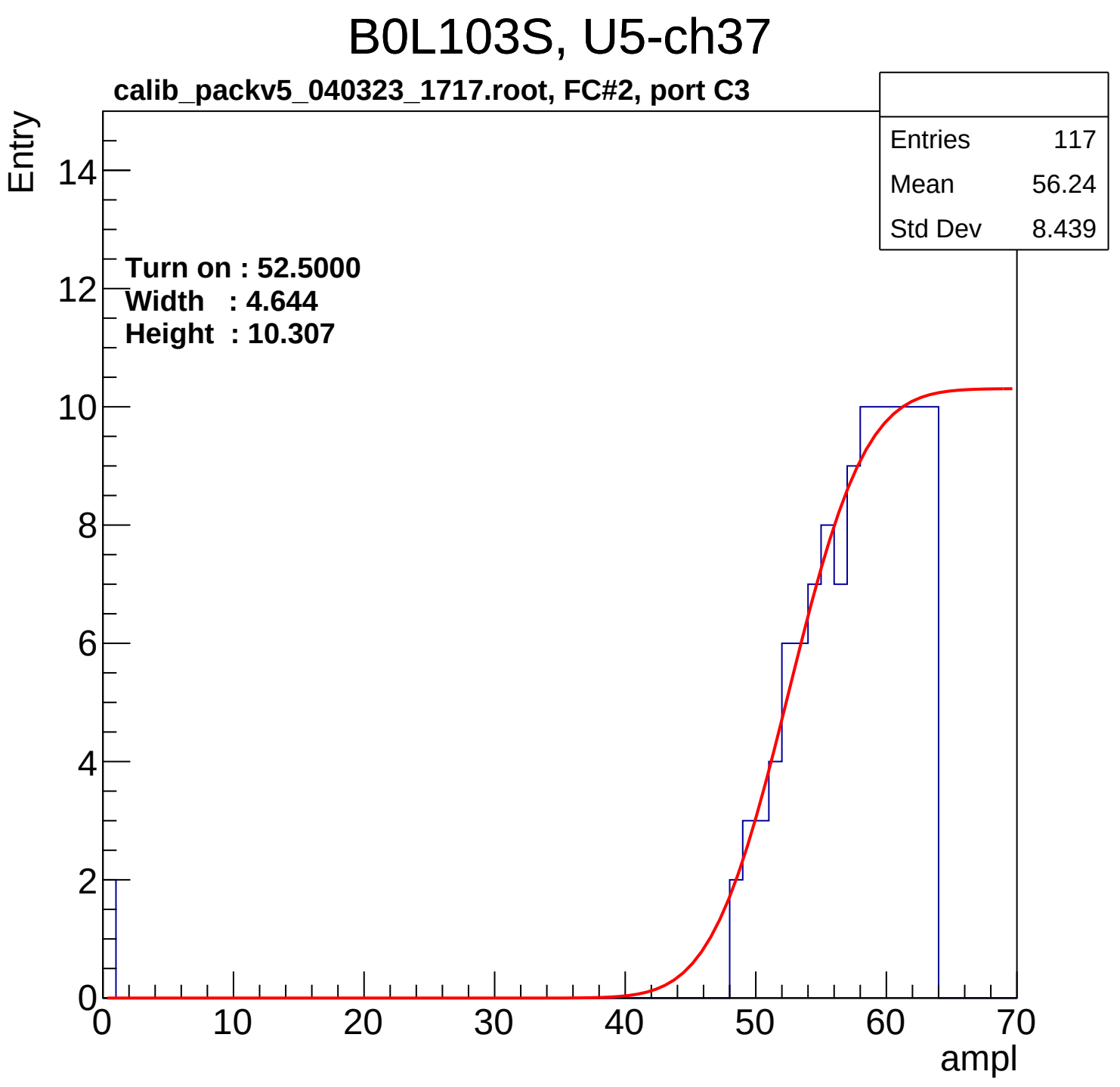
B0L103S, U5-ch37
calib_packv5_040323_1717.root, FC#2, port C3
Entries 117
Mean 56.24
Std Dev 8.439
Turn on : 52.5000
Width : 4.644
Height : 10.307
Entry
ampl
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8
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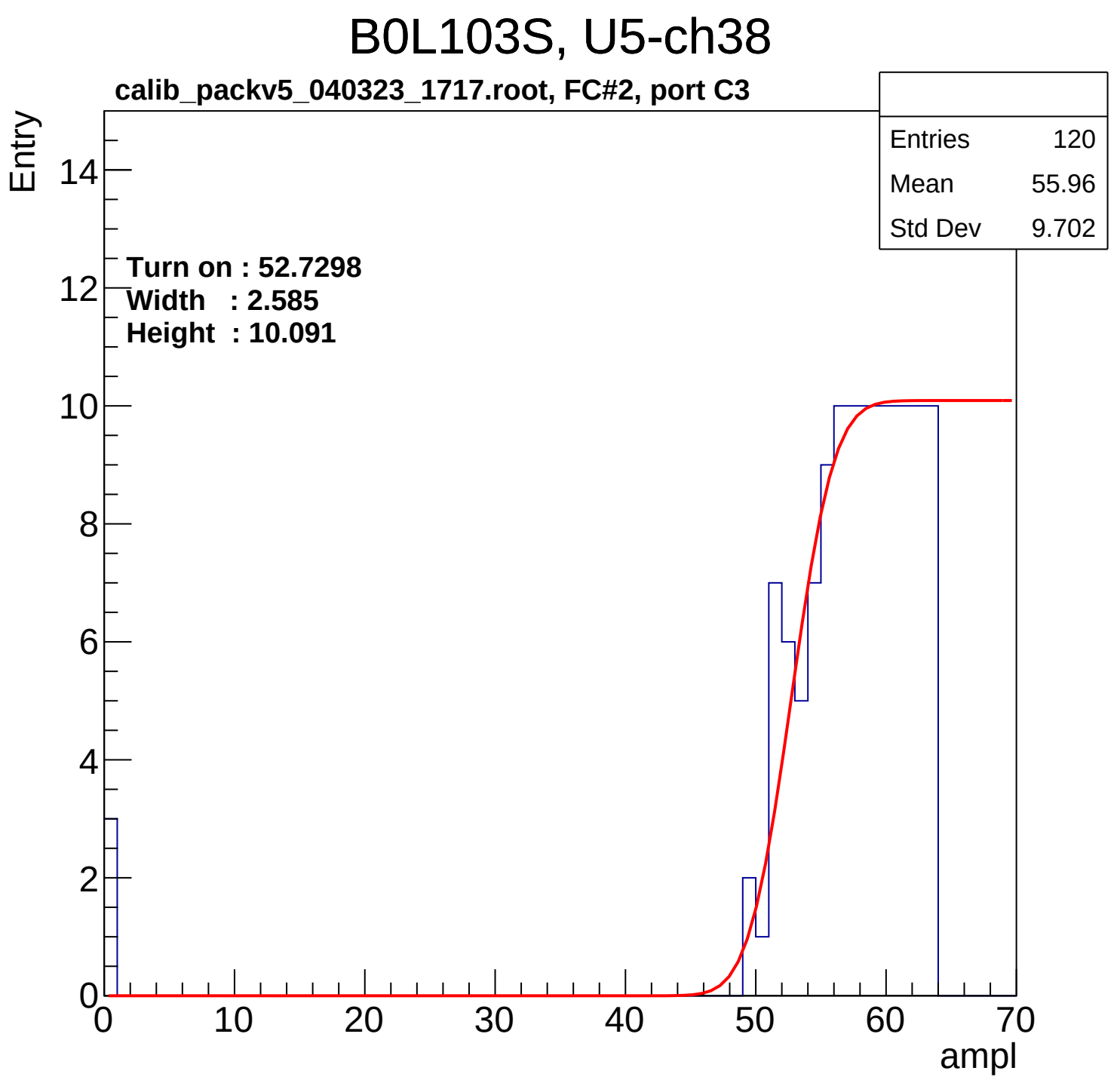
B0L103S, U5-ch38
calib_packv5_040323_1717.root, FC#2, port C3
Entries 120
Mean 55.96
Std Dev 9.702
Turn on : 52.7298
Width : 2.585
Height : 10.091
Entry
ampl
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8
10
12
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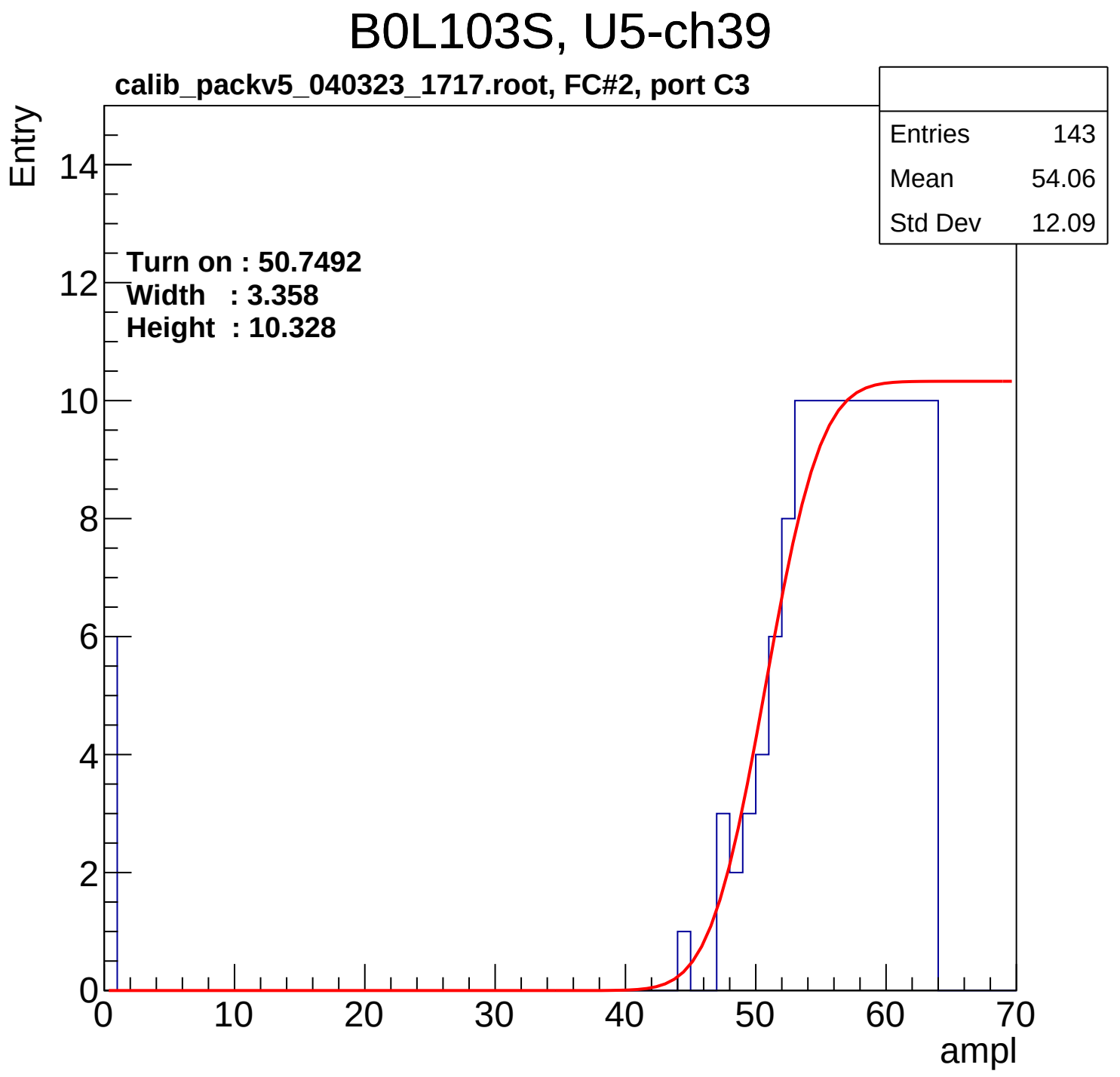
B0L103S, U5-ch39
calib_packv5_040323_1717.root, FC#2, port C3
Entries 143
Mean 54.06
Std Dev 12.09
Turn on : 50.7492
Width : 3.358
Height : 10.328
Entry
ampl
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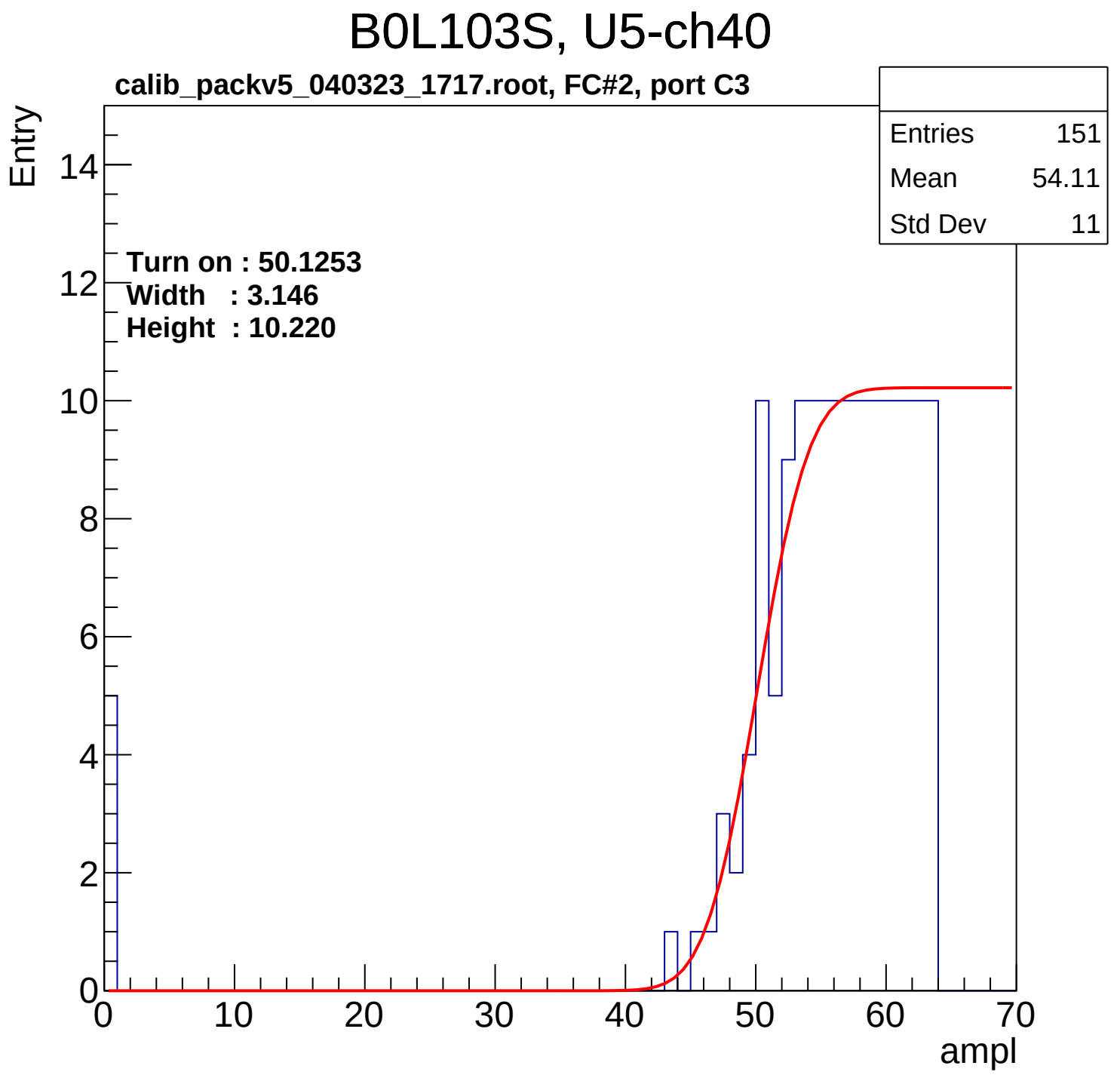
B0L103S, U5-ch40
calib_packv5_040323_1717.root, FC#2, port C3
Entries 151
Mean 54.11
Std Dev 11
Turn on : 50.1253
Width : 3.146
Height : 10.220
Entry
ampl
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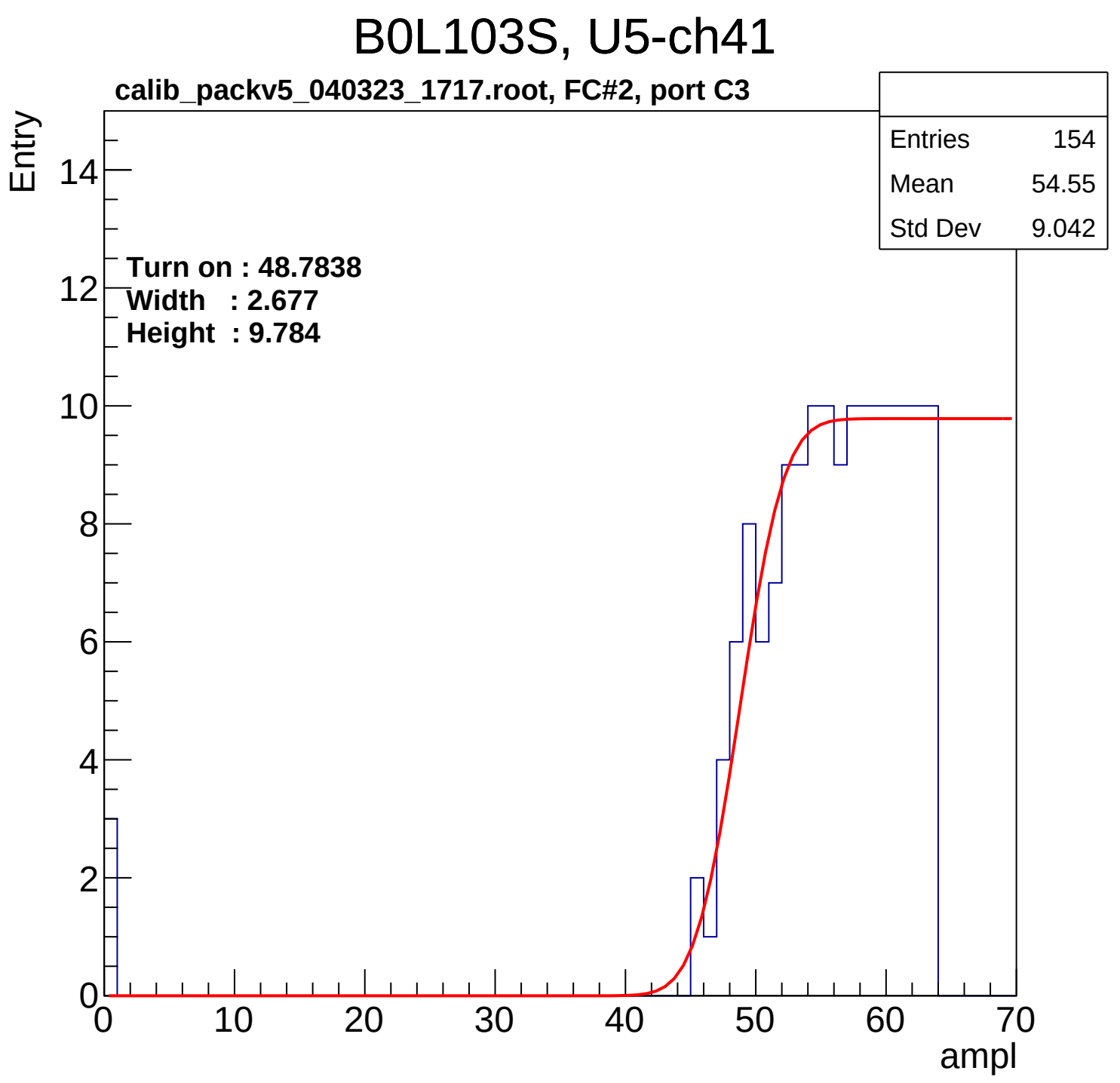
B0L103S, U5-ch41
calib_packv5_040323_1717.root, FC#2, port C3
Entries 154
Mean 54.55
Std Dev 9.042
Turn on : 48.7838
Width : 2.677
Height : 9.784
Entry
ampl
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8
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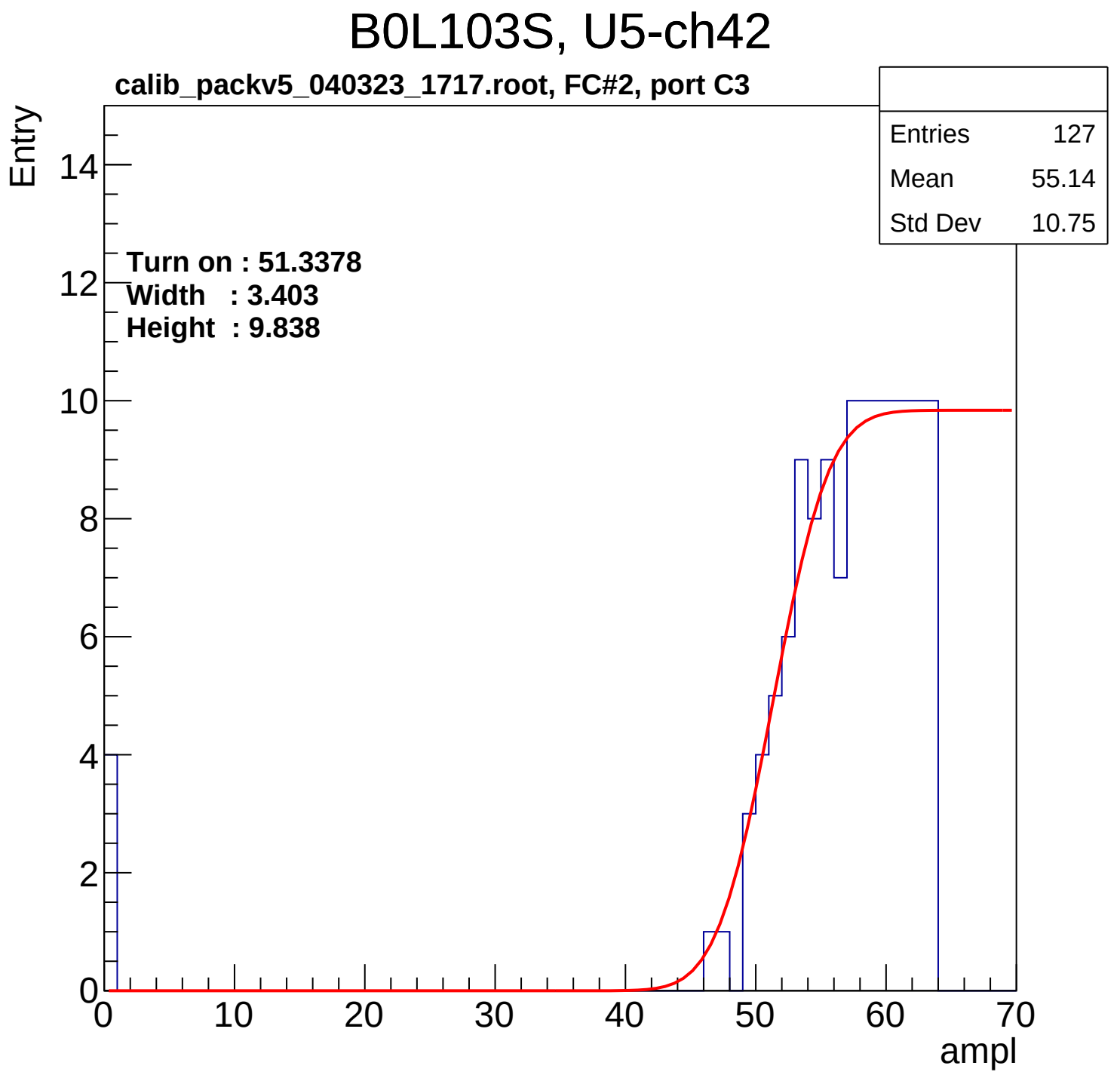
B0L103S, U5-ch42
calib_packv5_040323_1717.root, FC#2, port C3
Entries 127
Mean 55.14
Std Dev 10.75
Turn on : 51.3378
Width : 3.403
Height : 9.838
Entry
ampl
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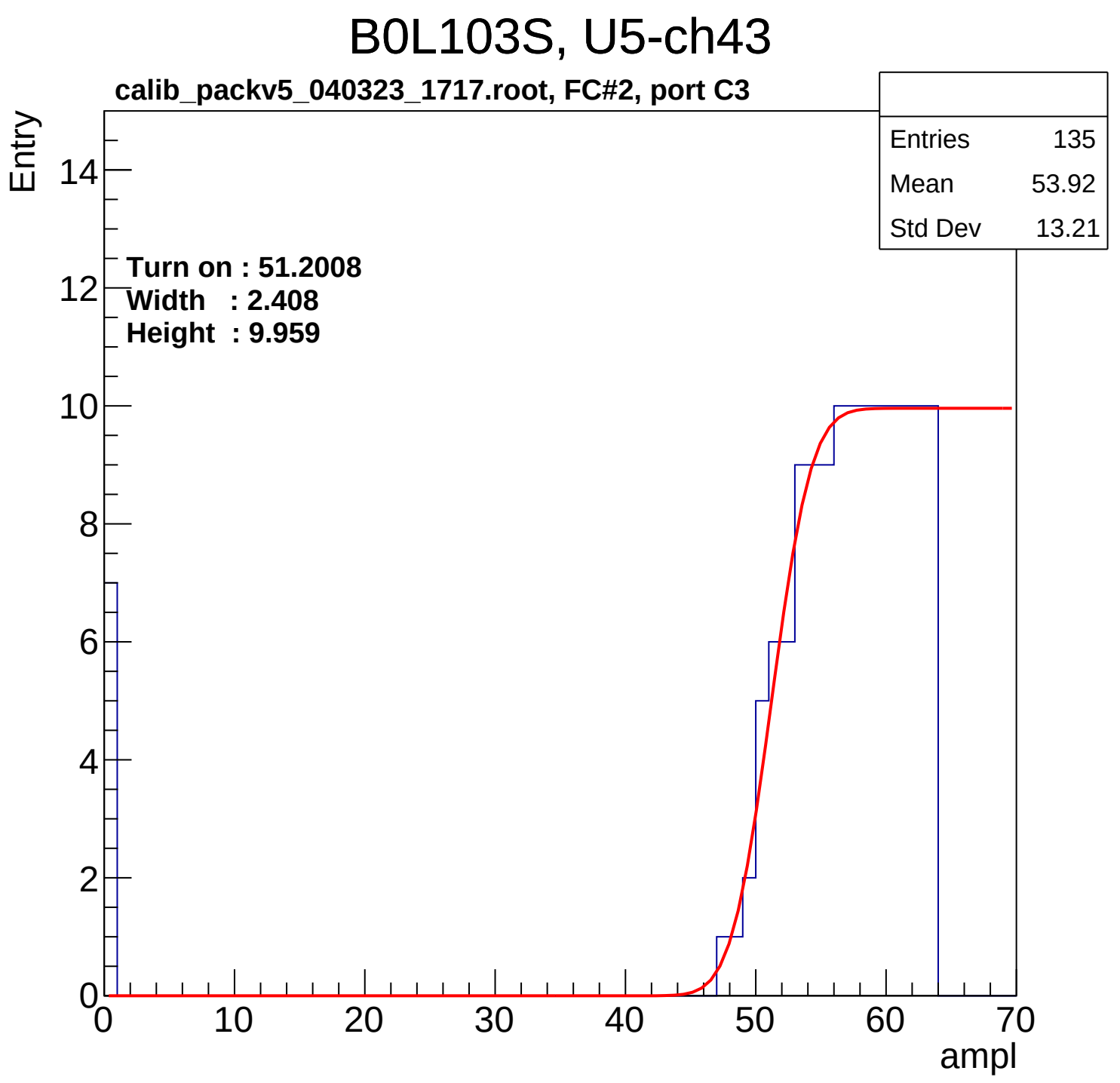
B0L103S, U5-ch43
calib_packv5_040323_1717.root, FC#2, port C3
Entries 135
Mean 53.92
Std Dev 13.21
Turn on : 51.2008
Width : 2.408
Height : 9.959
Entry
ampl
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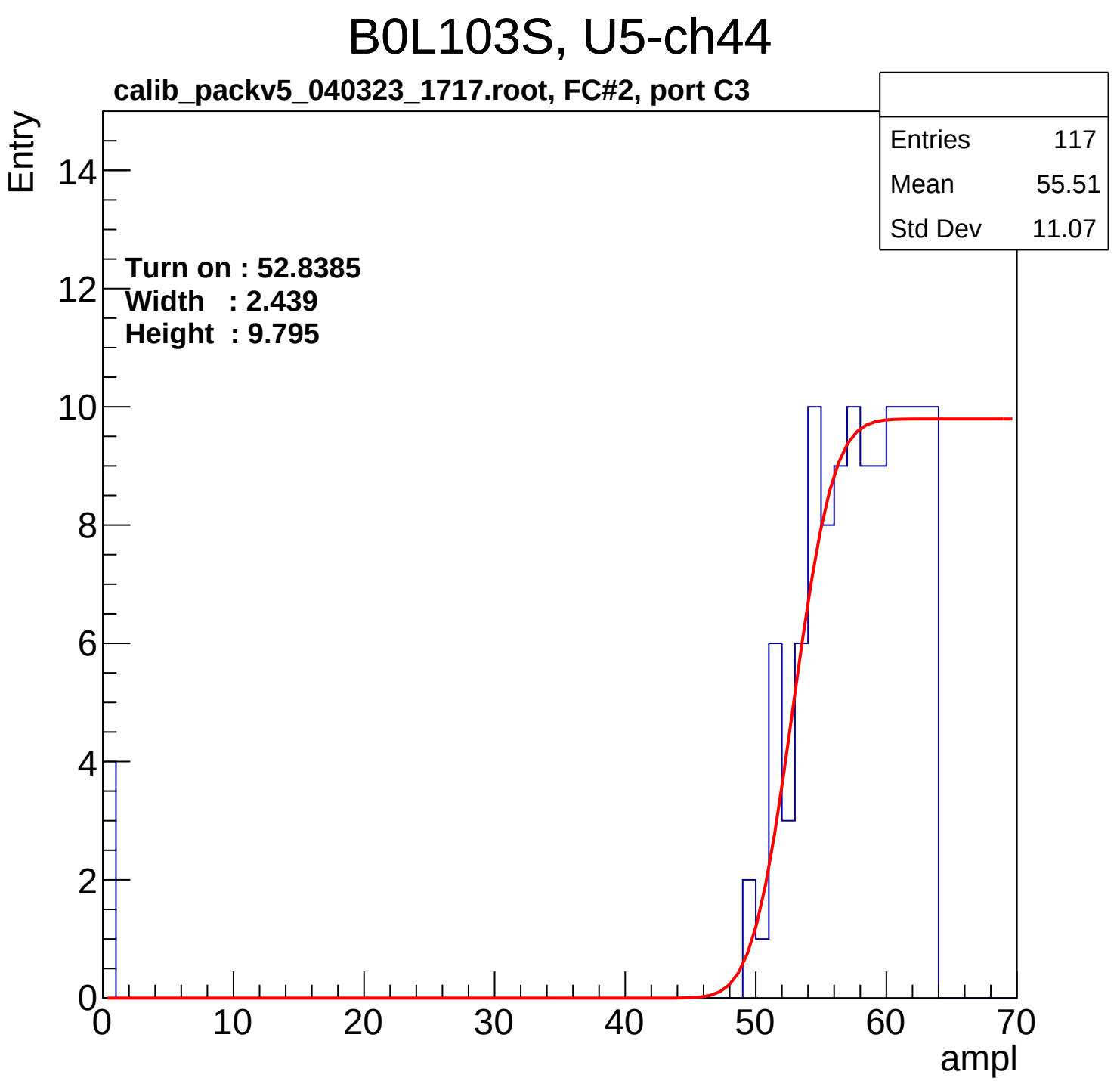
B0L103S, U5-ch44
calib_packv5_040323_1717.root, FC#2, port C3
Entries 117
Mean 55.51
Std Dev 11.07
Turn on : 52.8385
Width : 2.439
Height : 9.795
Entry
ampl
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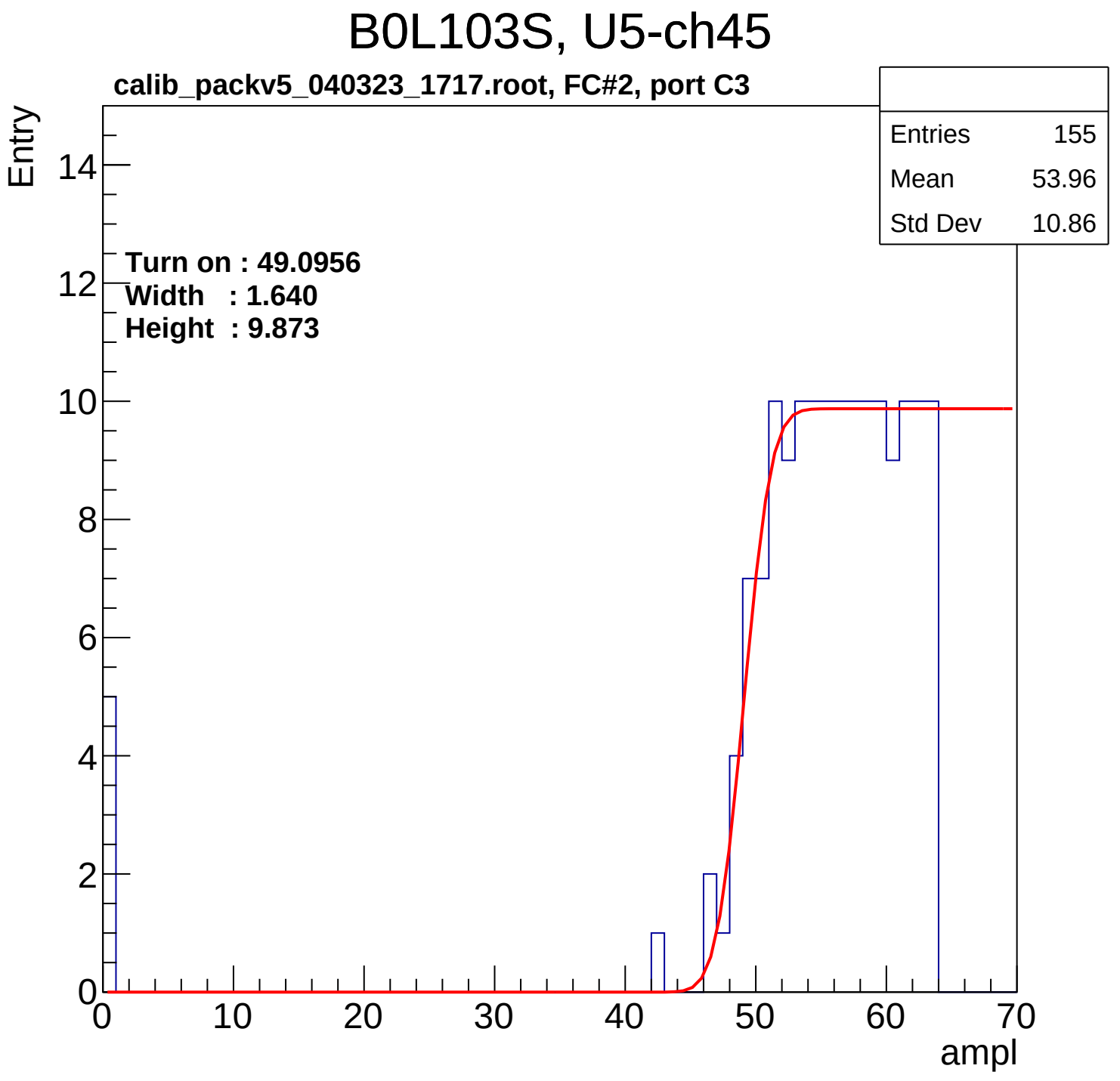
B0L103S, U5-ch45
calib_packv5_040323_1717.root, FC#2, port C3
Entries 155
Mean 53.96
Std Dev 10.86
Turn on : 49.0956
Width : 1.640
Height : 9.873
Entry
ampl
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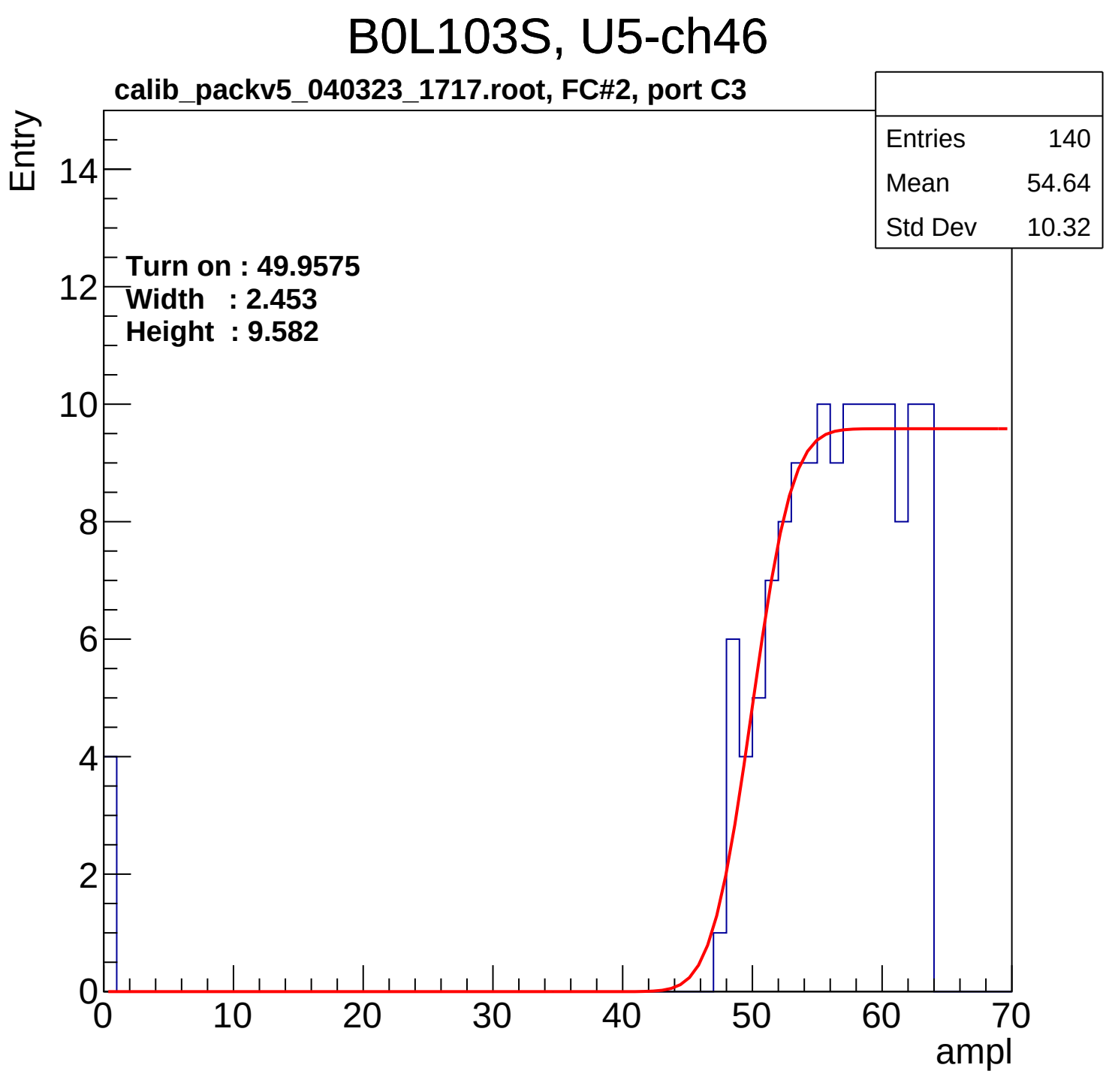
B0L103S, U5-ch46
calib_packv5_040323_1717.root, FC#2, port C3
Entries 140
Mean 54.64
Std Dev 10.32
Turn on : 49.9575
Width : 2.453
Height : 9.582
Entry
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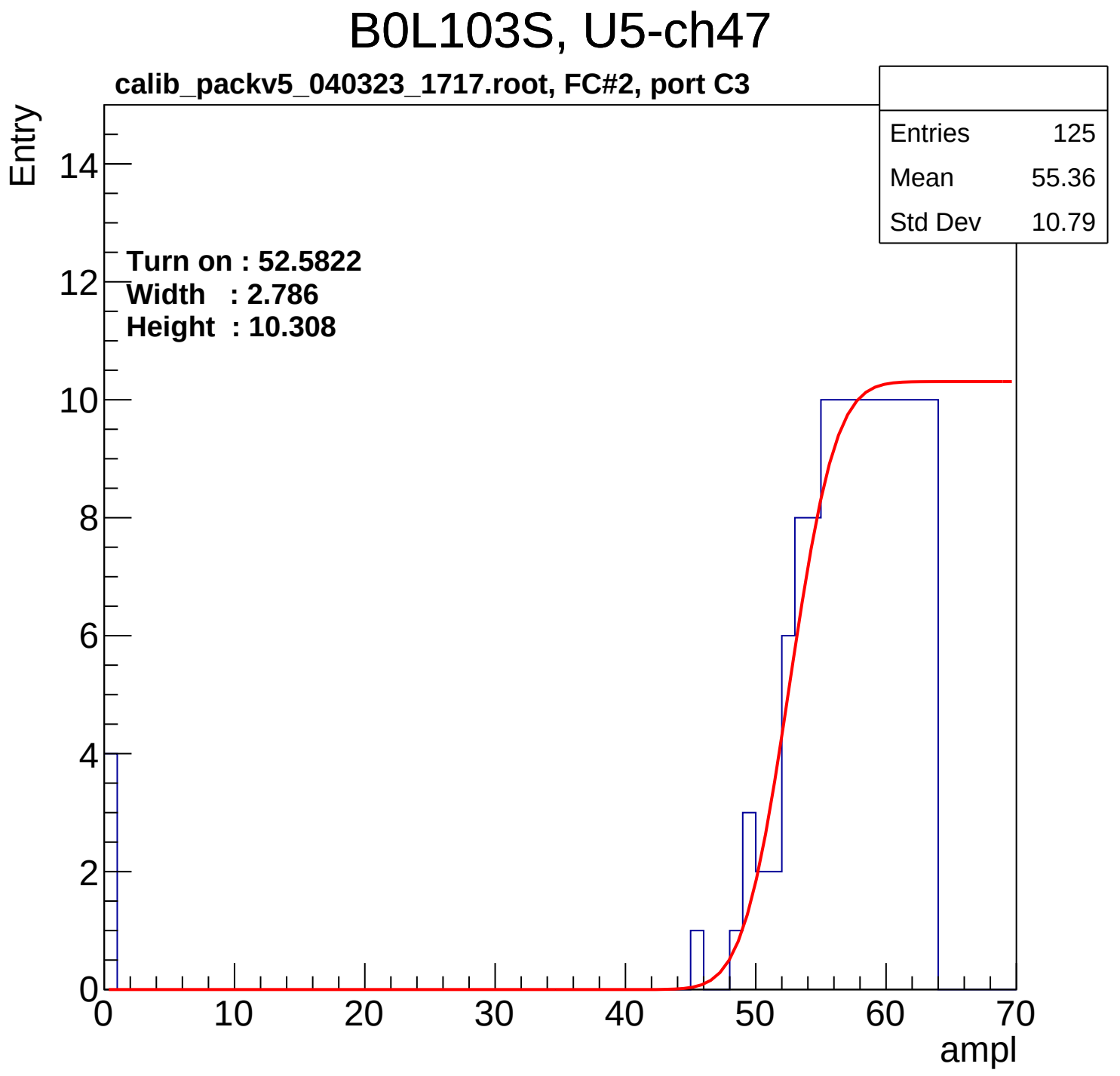
B0L103S, U5-ch47
calib_packv5_040323_1717.root, FC#2, port C3
Entries 125
Mean 55.36
Std Dev 10.79
Turn on : 52.5822
Width : 2.786
Height : 10.308
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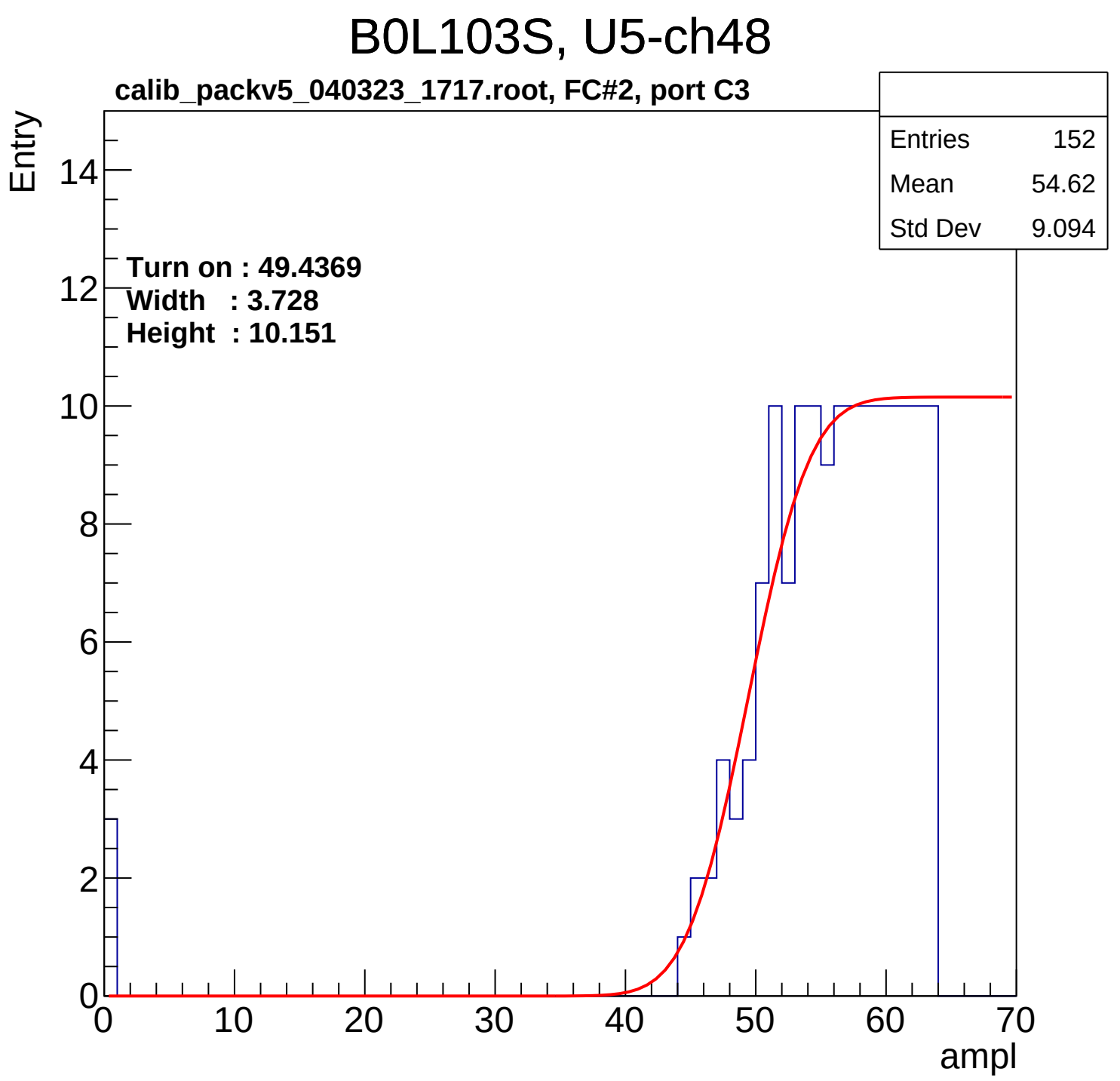
B0L103S, U5-ch48
calib_packv5_040323_1717.root, FC#2, port C3
Entries 152
Mean 54.62
Std Dev 9.094
Turn on : 49.4369
Width : 3.728
Height : 10.151
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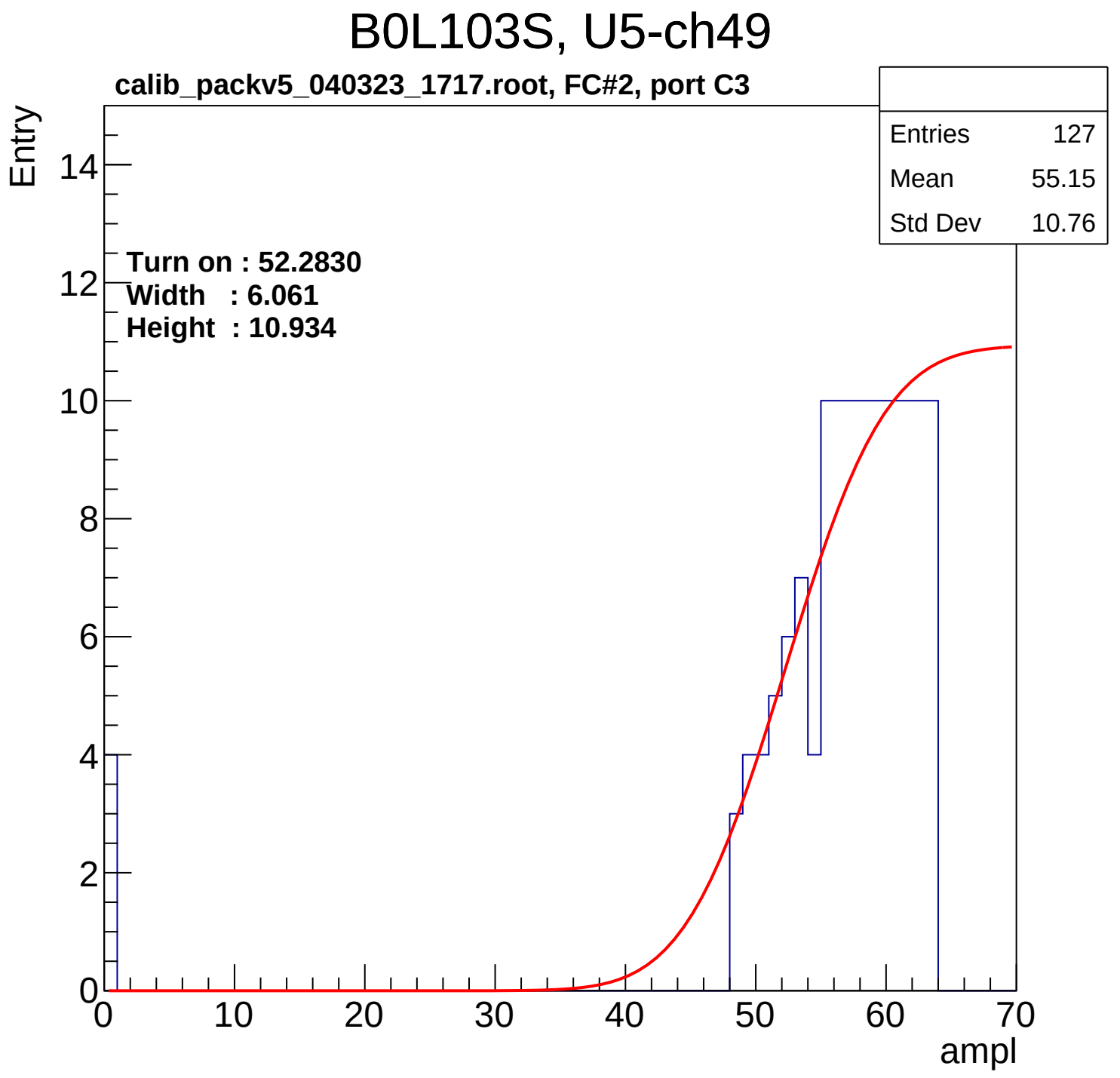
B0L103S, U5-ch49
calib_packv5_040323_1717.root, FC#2, port C3
Entries 127
Mean 55.15
Std Dev 10.76
Turn on : 52.2830
Width : 6.061
Height : 10.934
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ampl
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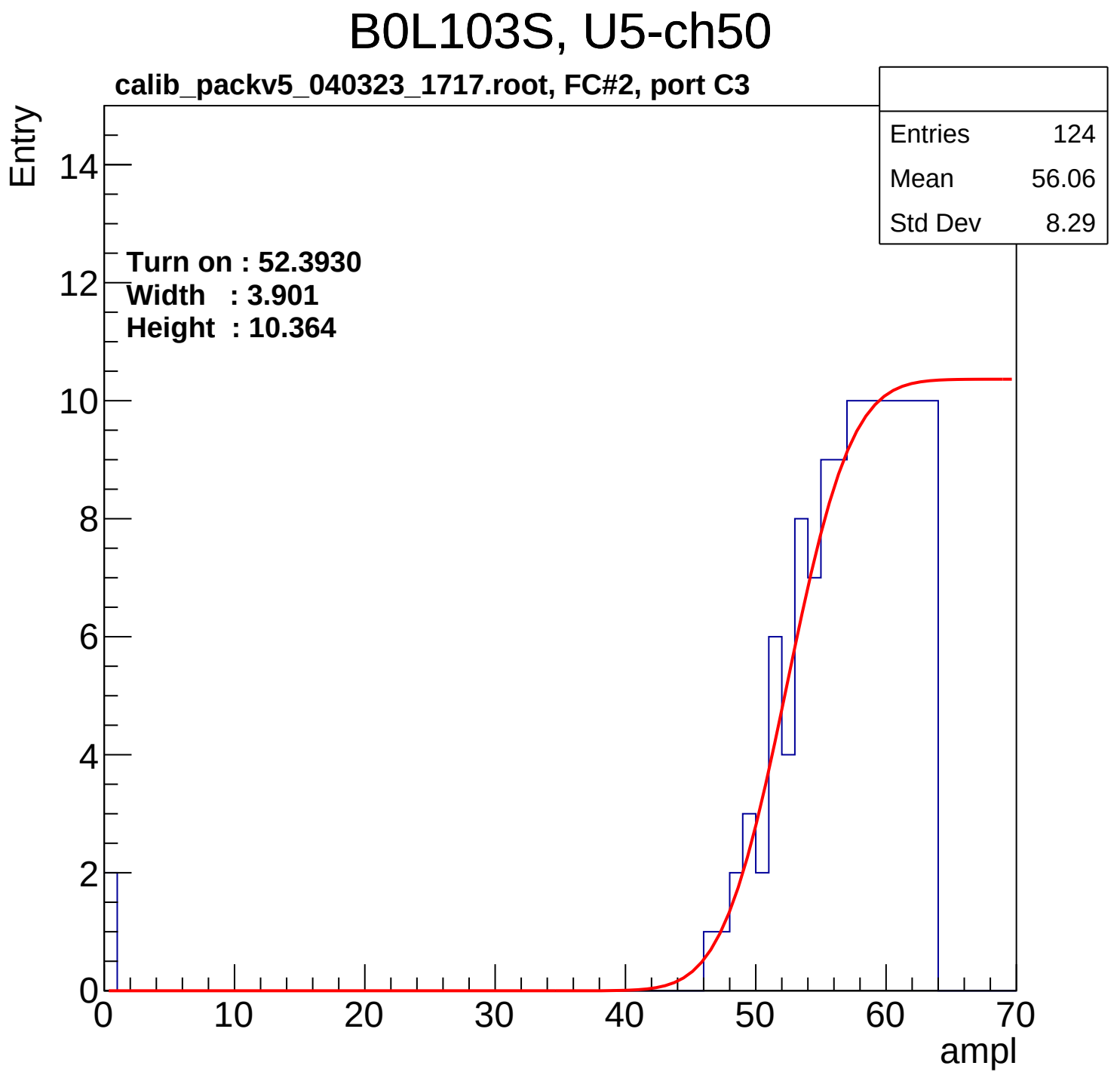
B0L103S, U5-ch50
calib_packv5_040323_1717.root, FC#2, port C3
Entries 124
Mean 56.06
Std Dev 8.29
Turn on : 52.3930
Width : 3.901
Height : 10.364
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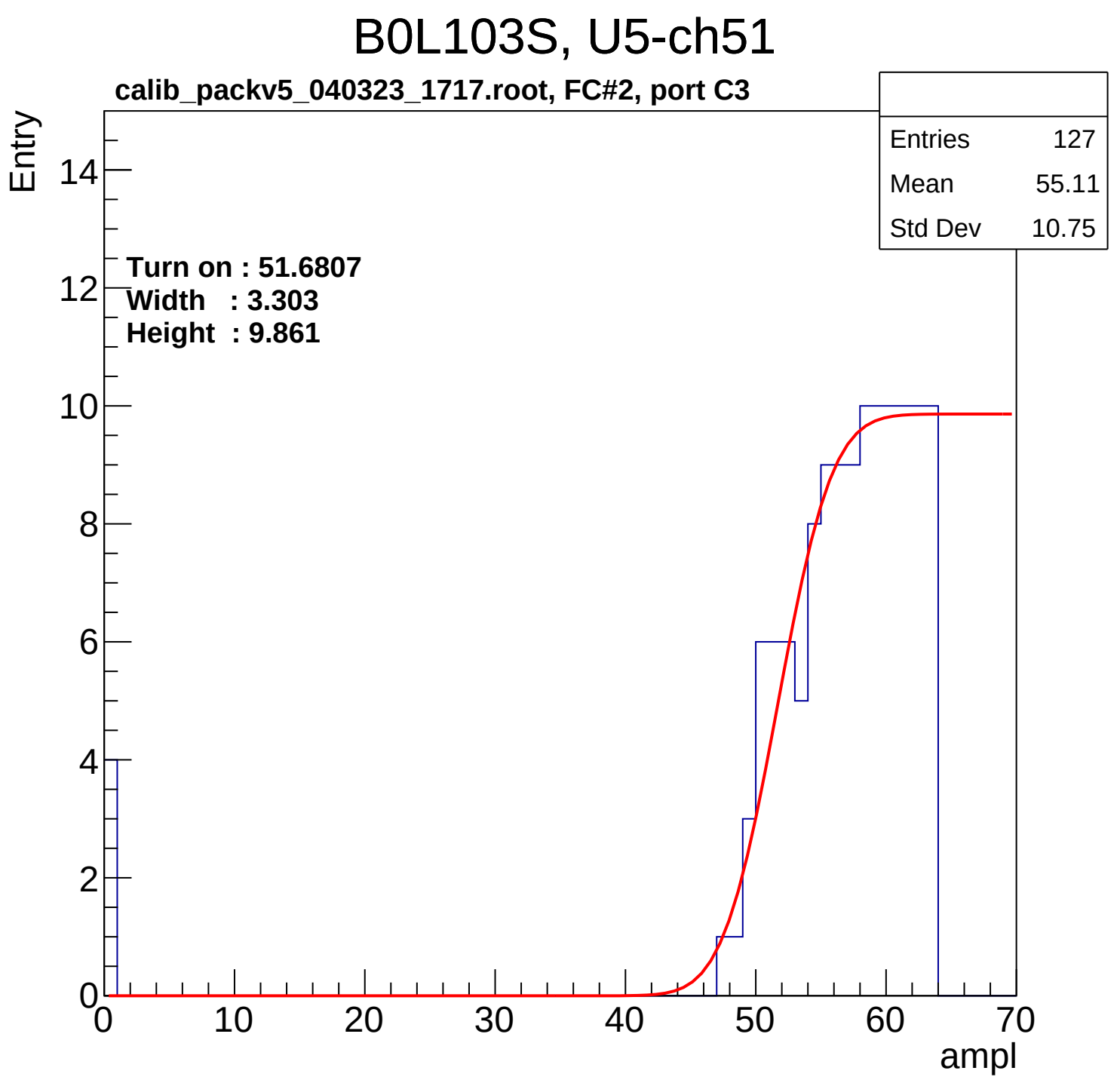
B0L103S, U5-ch51
calib_packv5_040323_1717.root, FC#2, port C3
Entries 127
Mean 55.11
Std Dev 10.75
Turn on : 51.6807
Width : 3.303
Height : 9.861
Entry
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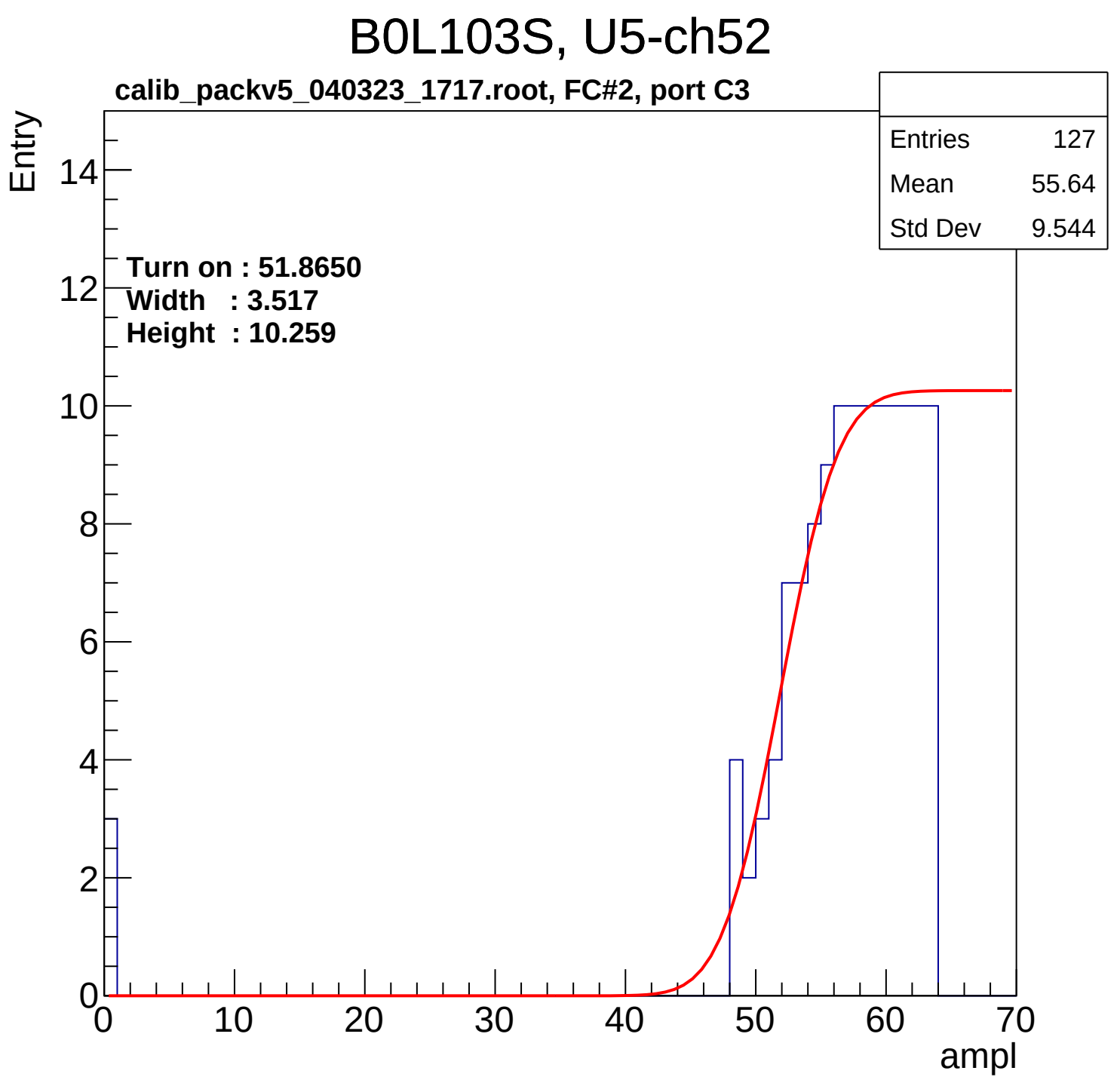
B0L103S, U5-ch52
calib_packv5_040323_1717.root, FC#2, port C3
Entries 127
Mean 55.64
Std Dev 9.544
Turn on : 51.8650
Width : 3.517
Height : 10.259
Entry
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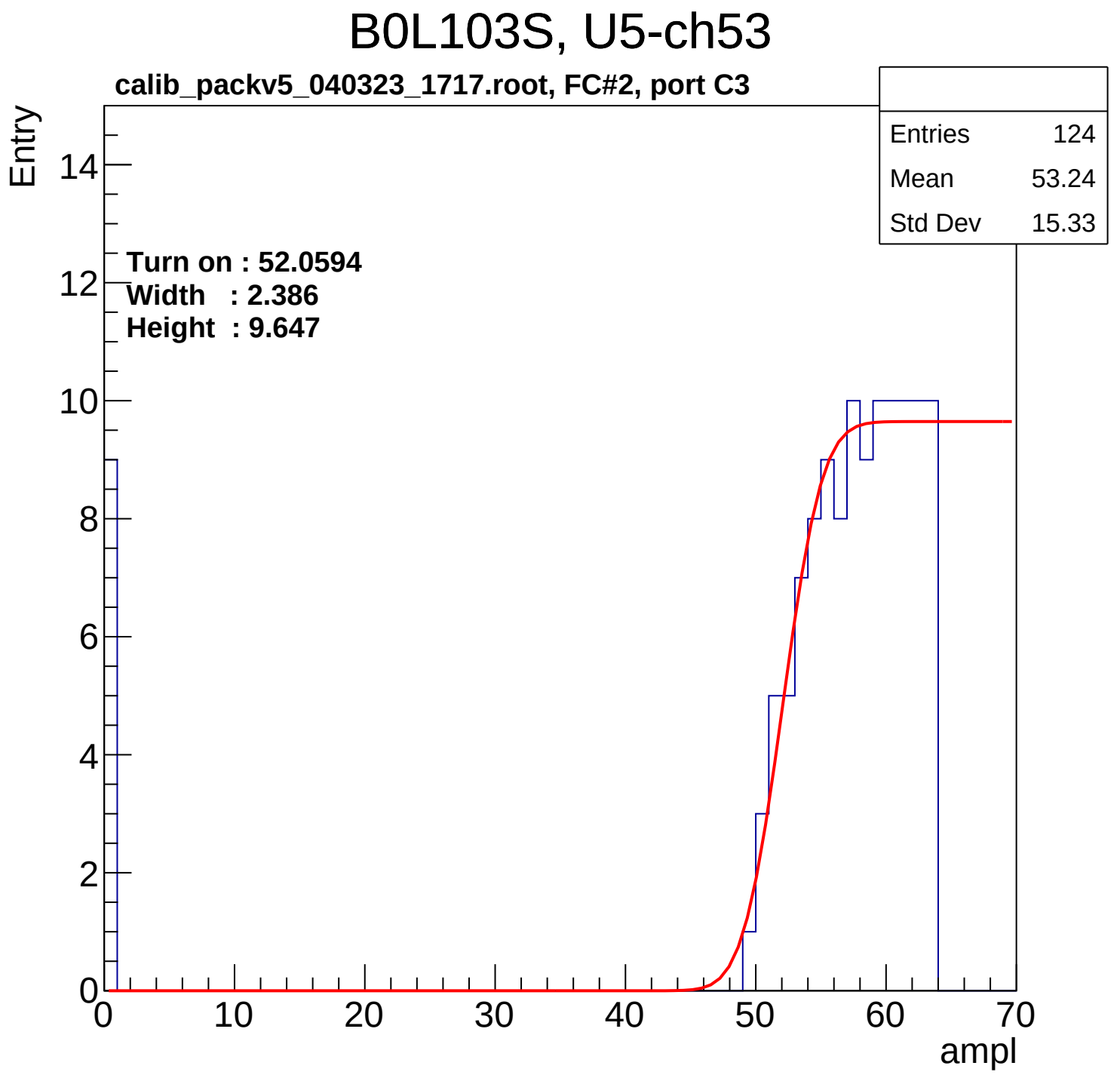
B0L103S, U5-ch53
calib_packv5_040323_1717.root, FC#2, port C3
Entries 124
Mean 53.24
Std Dev 15.33
Turn on : 52.0594
Width : 2.386
Height : 9.647
Entry
ampl
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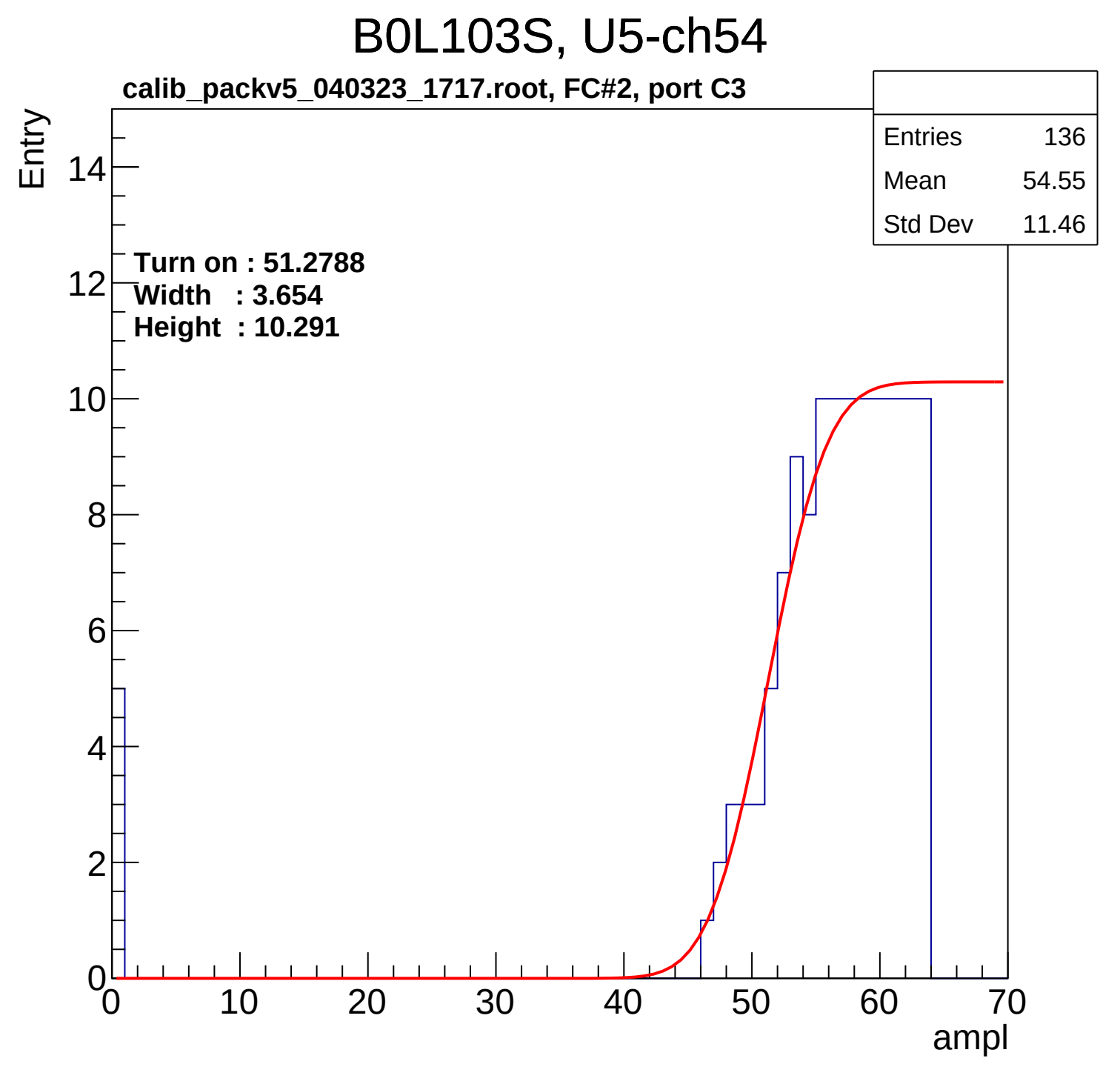
B0L103S, U5-ch54
calib_packv5_040323_1717.root, FC#2, port C3
Entries 136
Mean 54.55
Std Dev 11.46
Turn on : 51.2788
Width : 3.654
Height : 10.291
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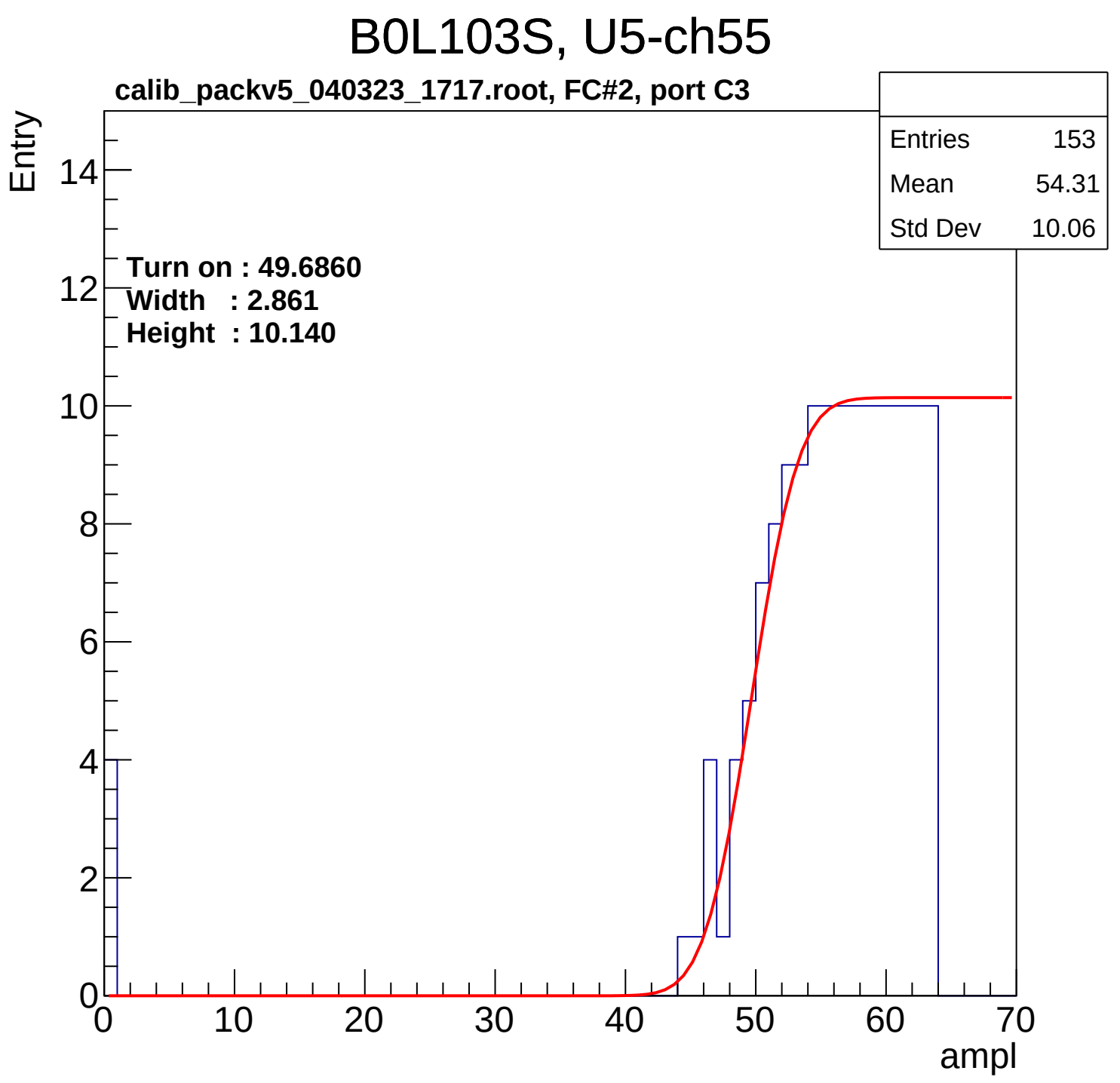
B0L103S, U5-ch55
calib_packv5_040323_1717.root, FC#2, port C3
Entries 153
Mean 54.31
Std Dev 10.06
Turn on : 49.6860
Width : 2.861
Height : 10.140
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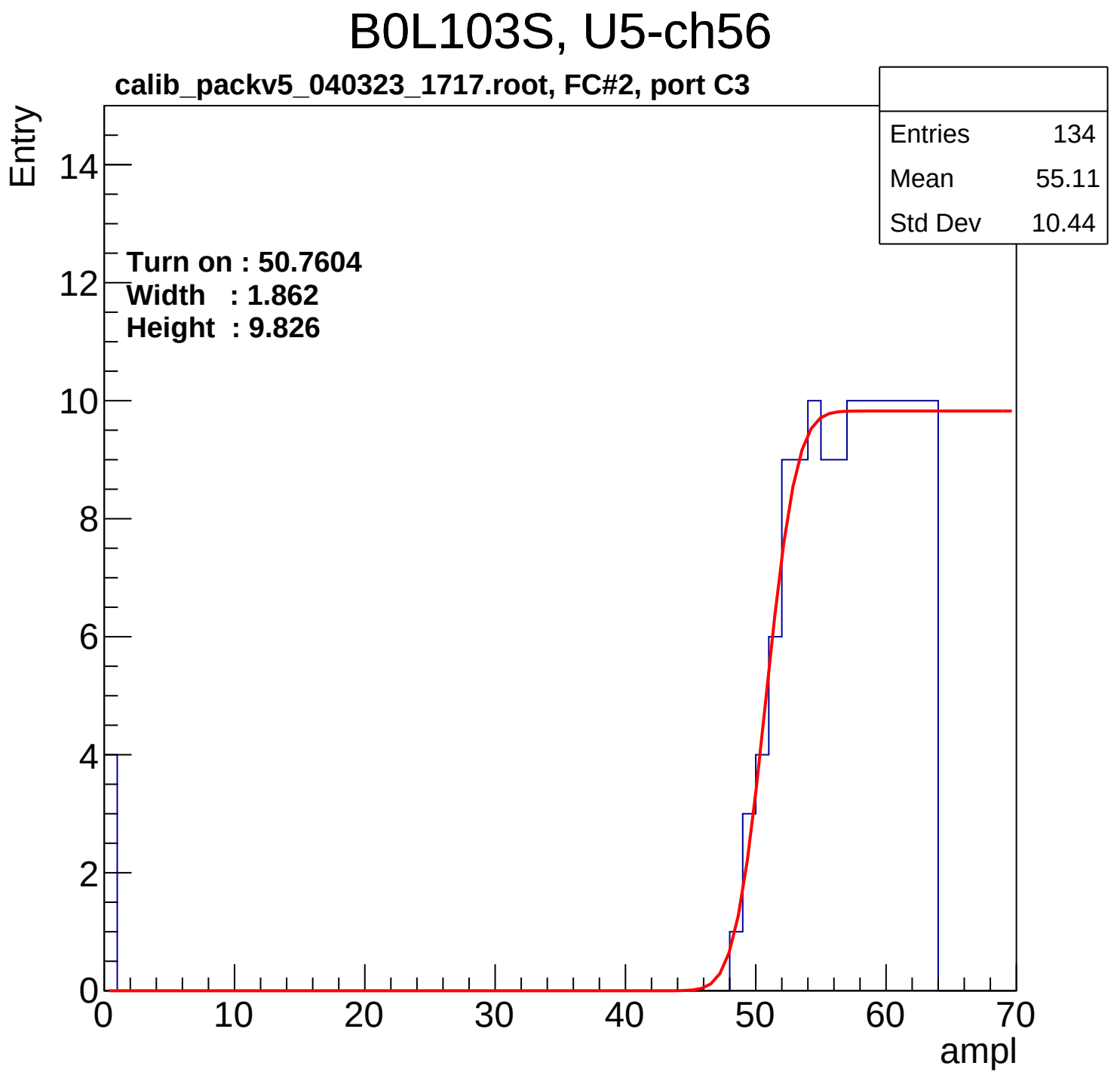
B0L103S, U5-ch56
calib_packv5_040323_1717.root, FC#2, port C3
Entries 134
Mean 55.11
Std Dev 10.44
Turn on : 50.7604
Width : 1.862
Height : 9.826
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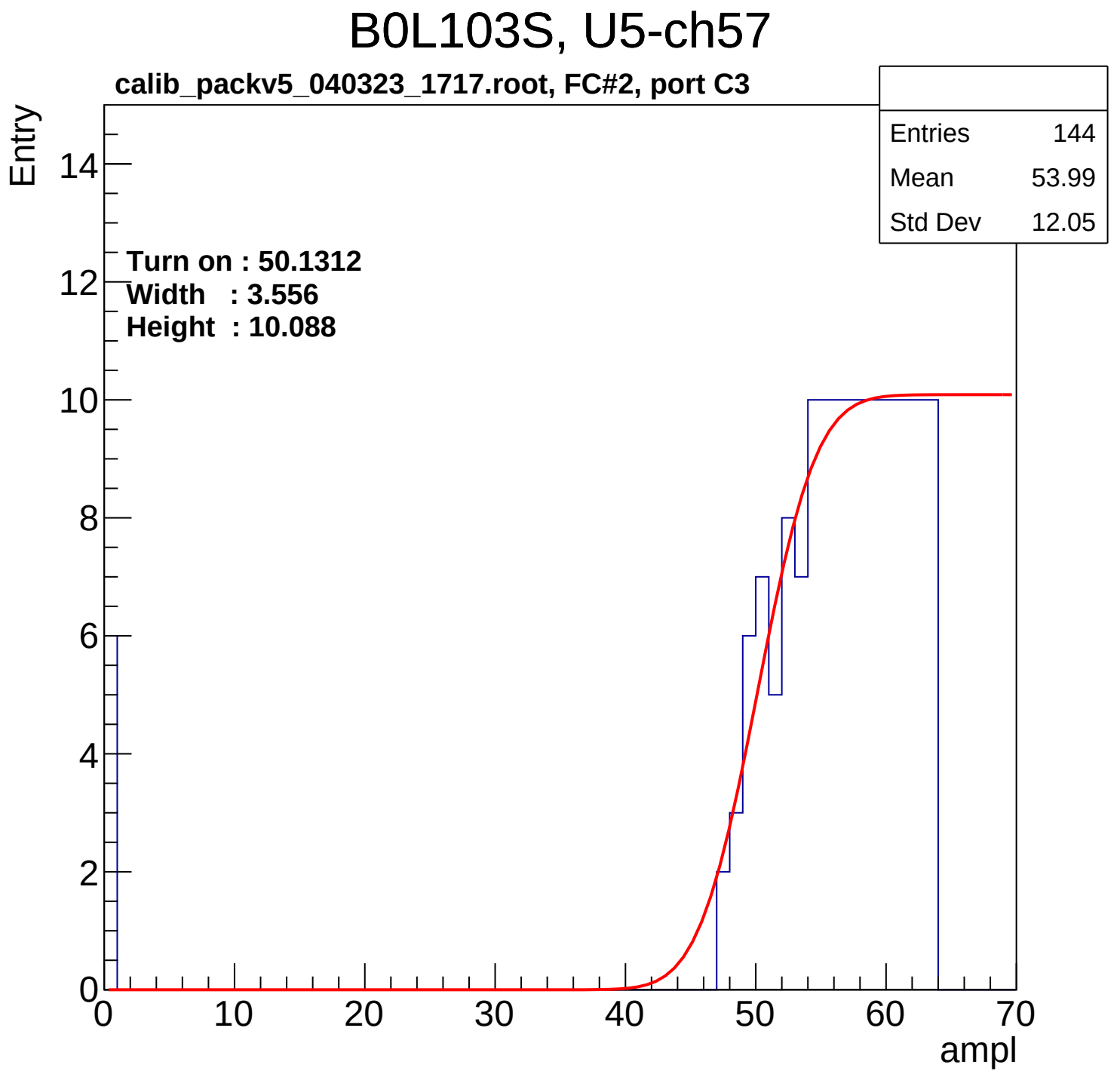
B0L103S, U5-ch57
calib_packv5_040323_1717.root, FC#2, port C3
Entries 144
Mean 53.99
Std Dev 12.05
Turn on : 50.1312
Width : 3.556
Height : 10.088
Entry
ampl
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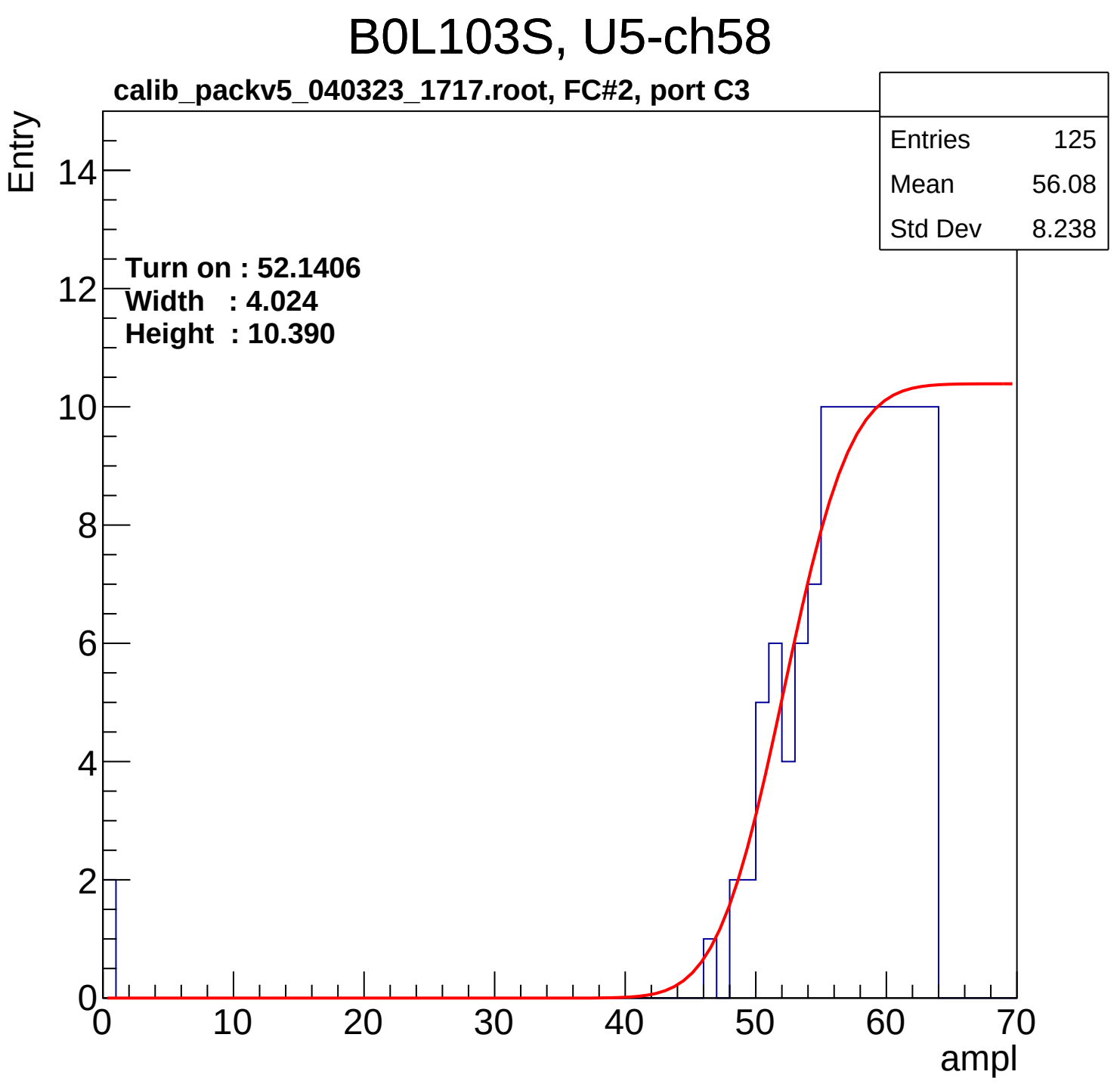
B0L103S, U5-ch58
calib_packv5_040323_1717.root, FC#2, port C3
Entries 125
Mean 56.08
Std Dev 8.238
Turn on : 52.1406
Width : 4.024
Height : 10.390
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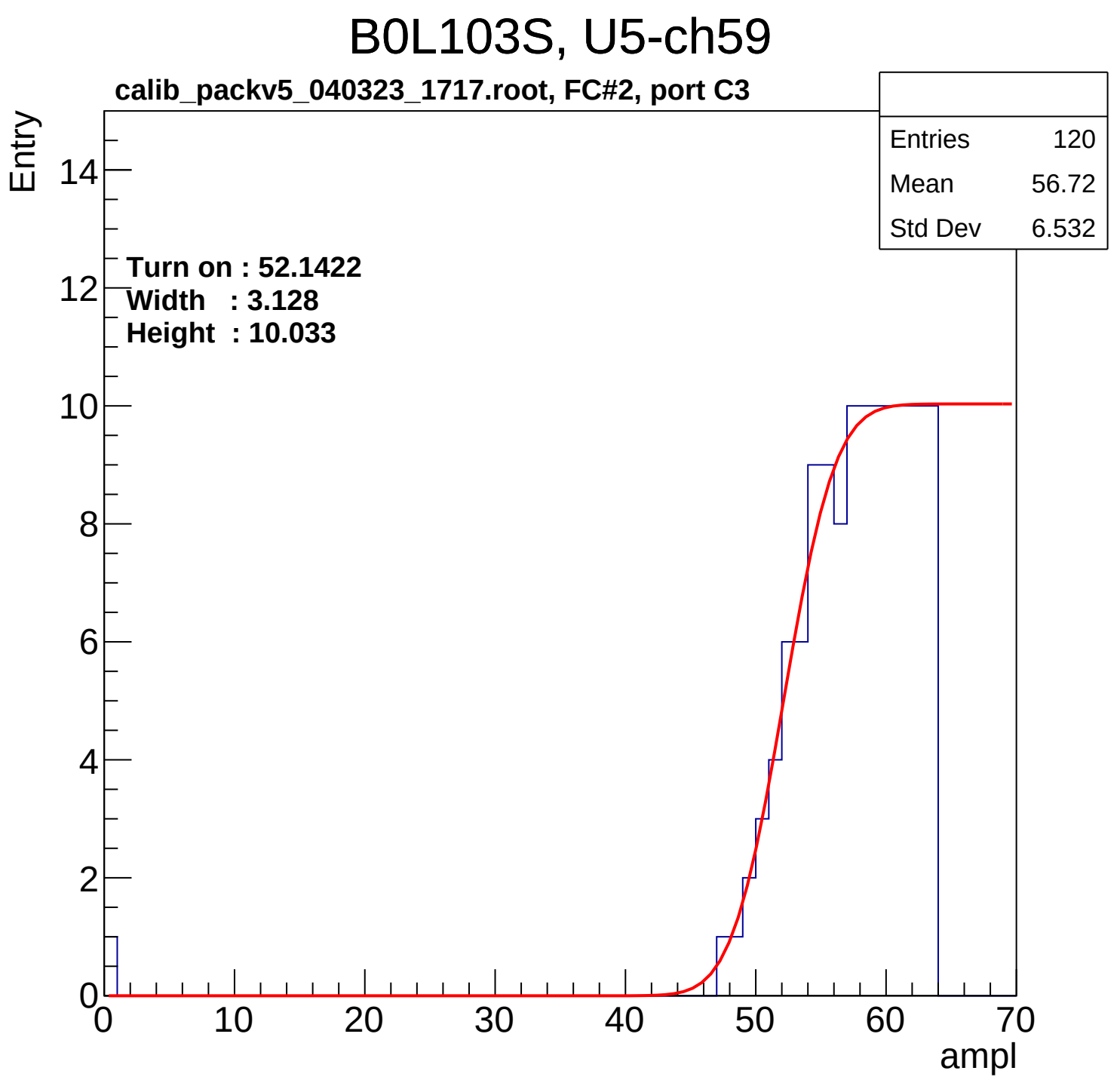
B0L103S, U5-ch59
calib_packv5_040323_1717.root, FC#2, port C3
Entries 120
Mean 56.72
Std Dev 6.532
Turn on : 52.1422
Width : 3.128
Height : 10.033
Entry
ampl
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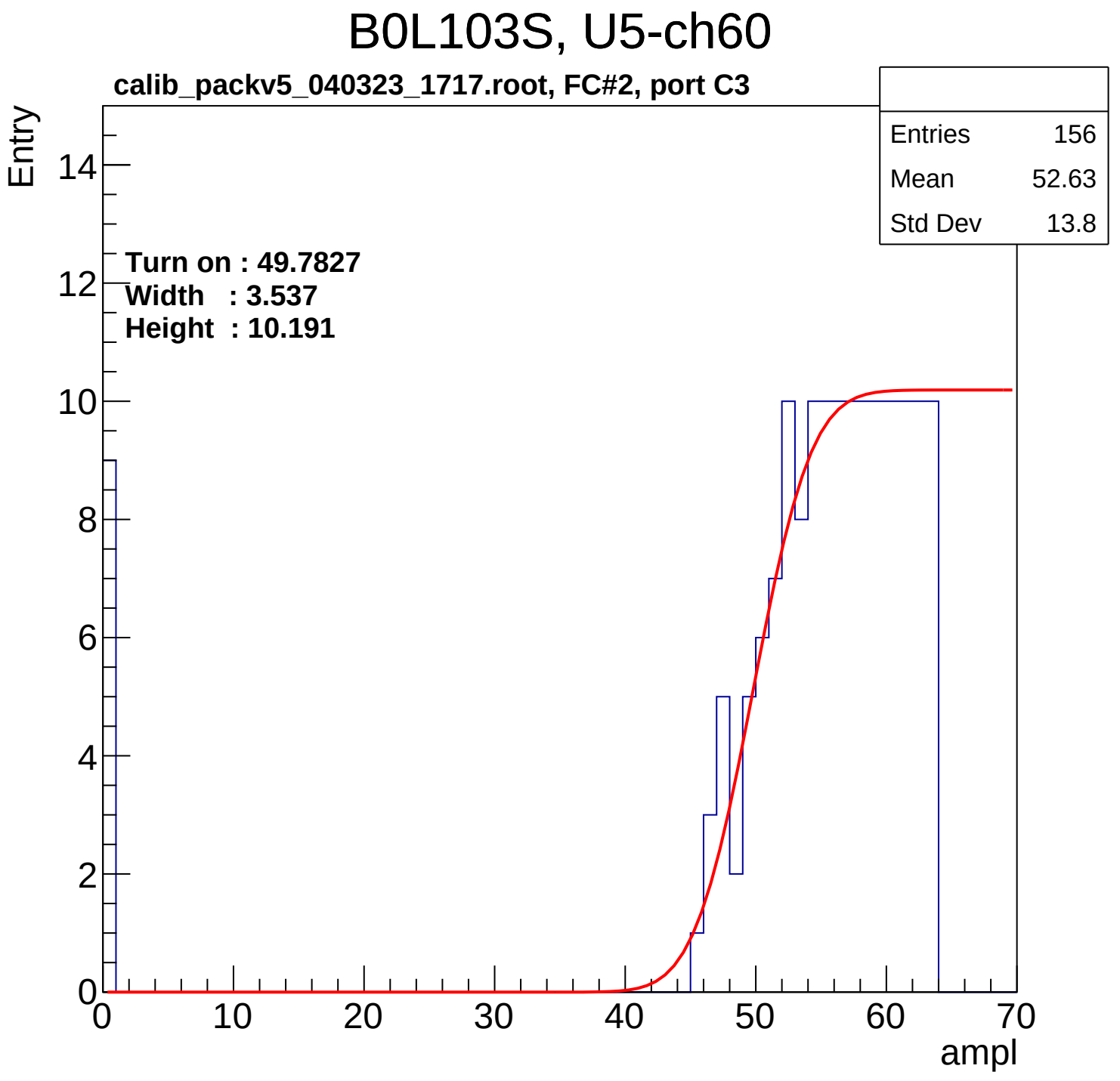
B0L103S, U5-ch60
calib_packv5_040323_1717.root, FC#2, port C3
Entries 156
Mean 52.63
Std Dev 13.8
Turn on : 49.7827
Width : 3.537
Height : 10.191
Entry
ampl
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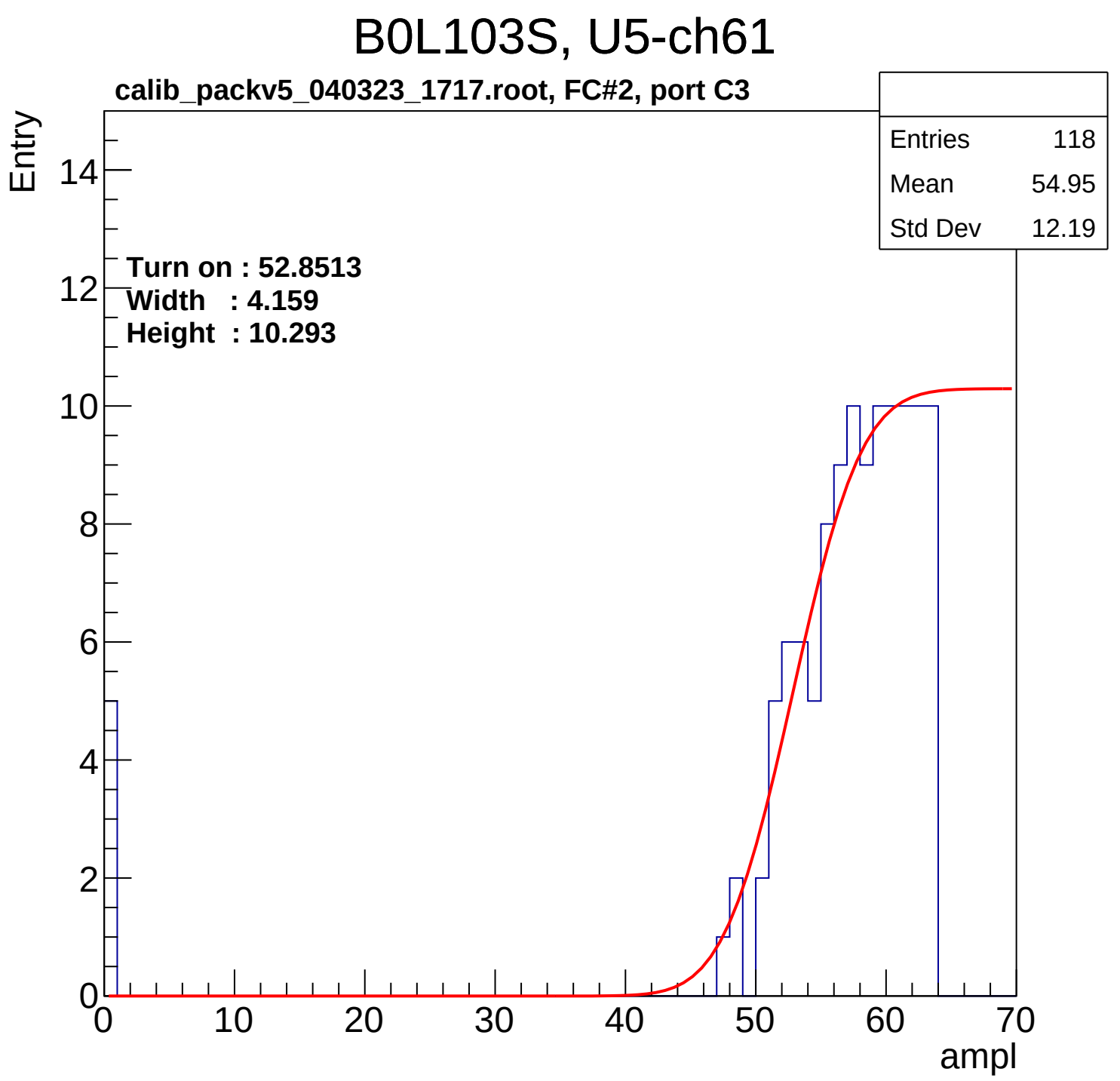
B0L103S, U5-ch61
calib_packv5_040323_1717.root, FC#2, port C3
Entries 118
Mean 54.95
Std Dev 12.19
Turn on : 52.8513
Width : 4.159
Height : 10.293
Entry
ampl
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2
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6
8
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0
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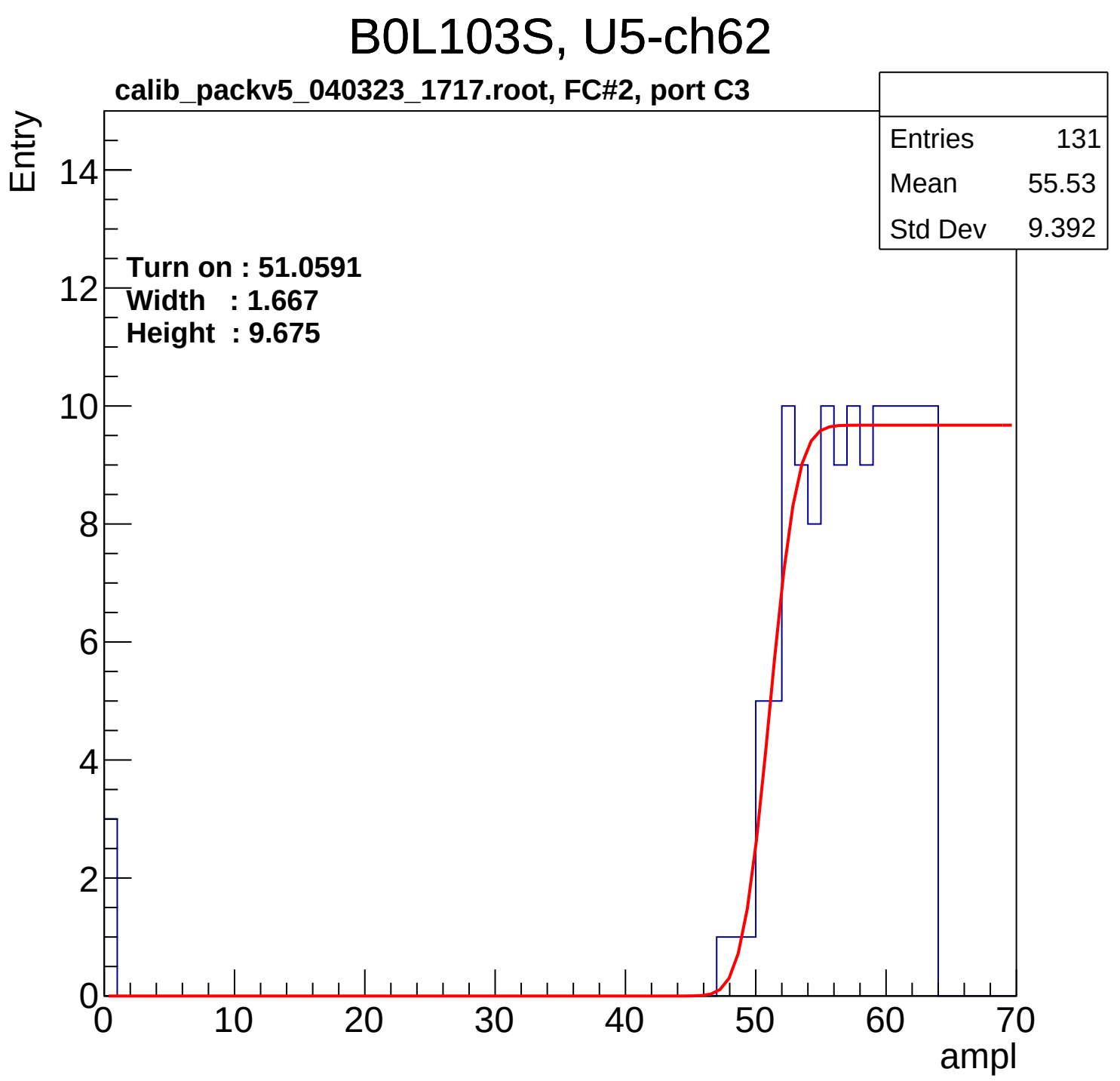
B0L103S, U5-ch62
calib_packv5_040323_1717.root, FC#2, port C3
Entries 131
Mean 55.53
Std Dev 9.392
Turn on : 51.0591
Width : 1.667
Height : 9.675
Entry
ampl
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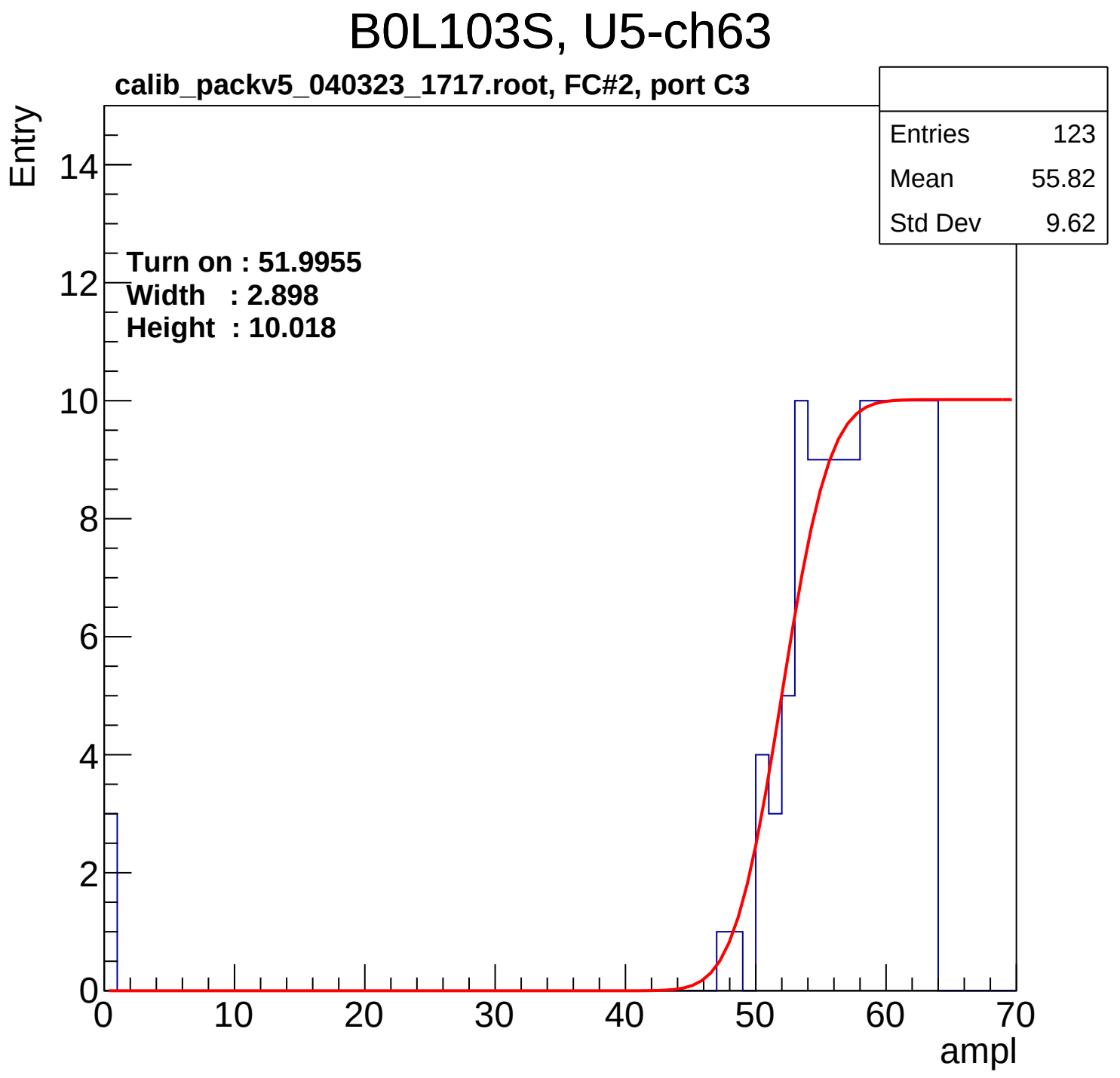
B0L103S, U5-ch63
calib_packv5_040323_1717.root, FC#2, port C3
Entries 123
Mean 55.82
Std Dev 9.62
Turn on : 51.9955
Width : 2.898
Height : 10.018
Entry
ampl
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2
4
6
8
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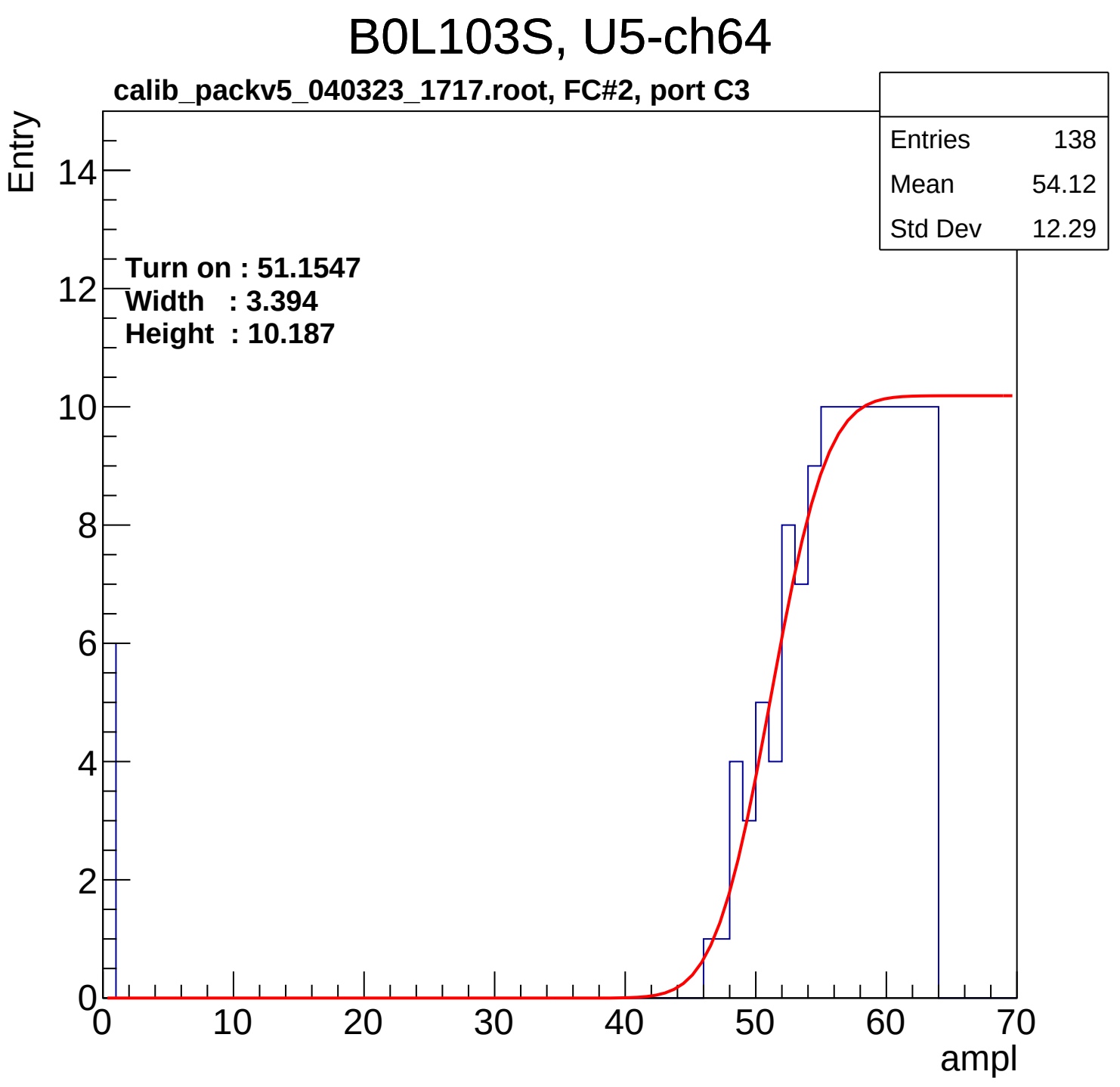
B0L103S, U5-ch64
calib_packv5_040323_1717.root, FC#2, port C3
Entries 138
Mean 54.12
Std Dev 12.29
Turn on : 51.1547
Width : 3.394
Height : 10.187
Entry
ampl
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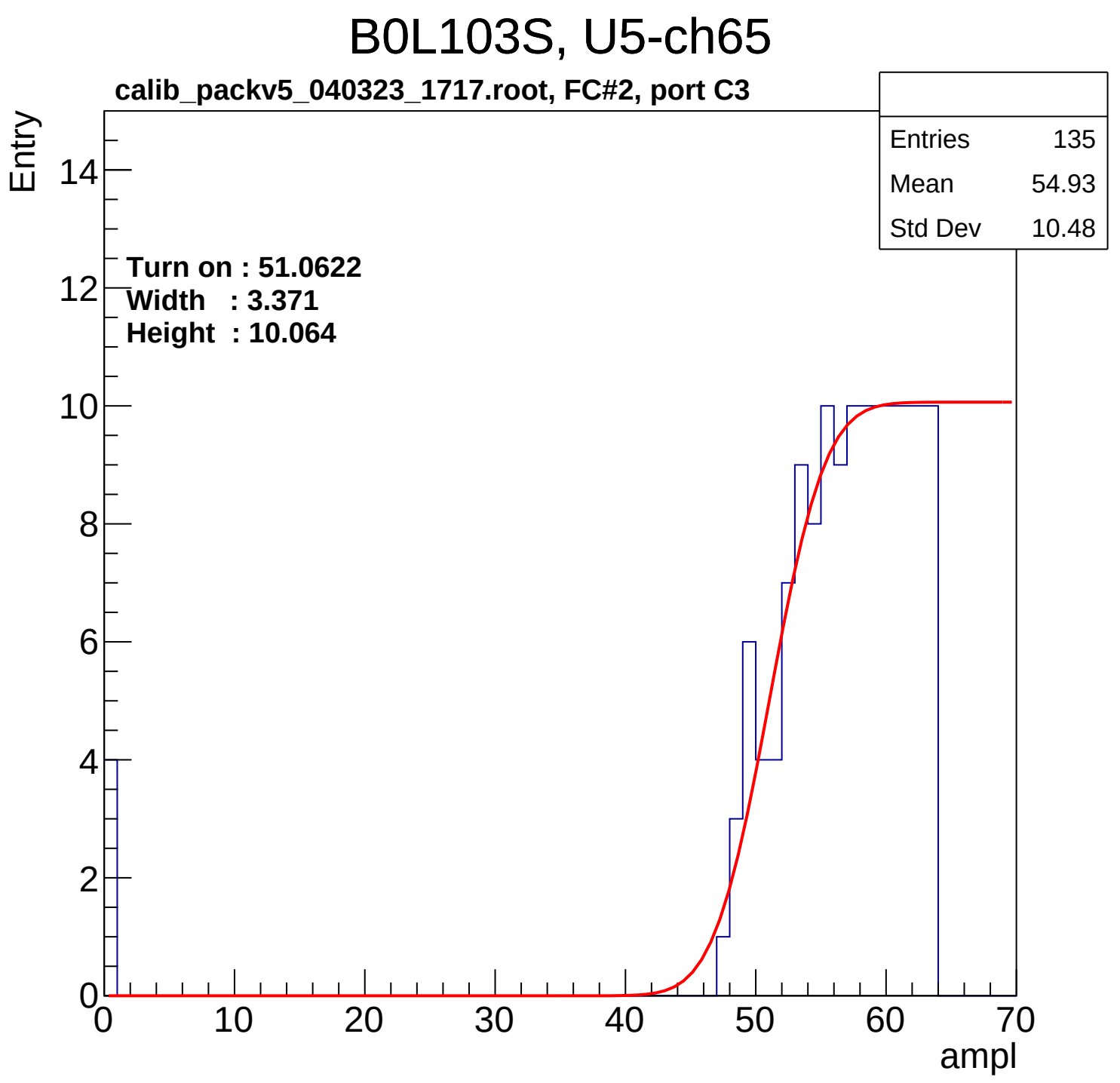
B0L103S, U5-ch65
calib_packv5_040323_1717.root, FC#2, port C3
Entries 135
Mean 54.93
Std Dev 10.48
Turn on : 51.0622
Width : 3.371
Height : 10.064
Entry
ampl
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6
8
10
12
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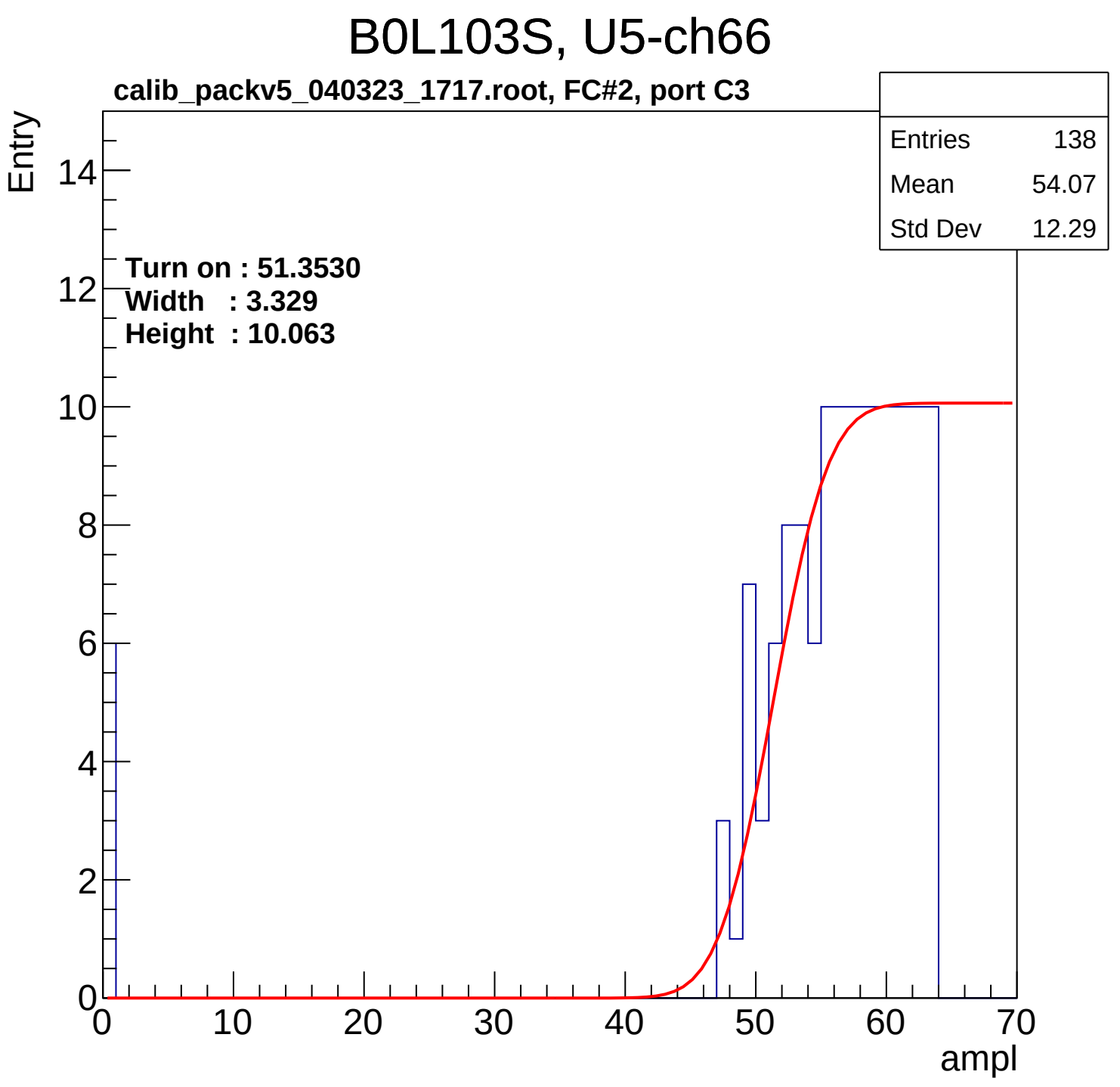
B0L103S, U5-ch66
calib_packv5_040323_1717.root, FC#2, port C3
Entries 138
Mean 54.07
Std Dev 12.29
Turn on : 51.3530
Width : 3.329
Height : 10.063
Entry
ampl
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8
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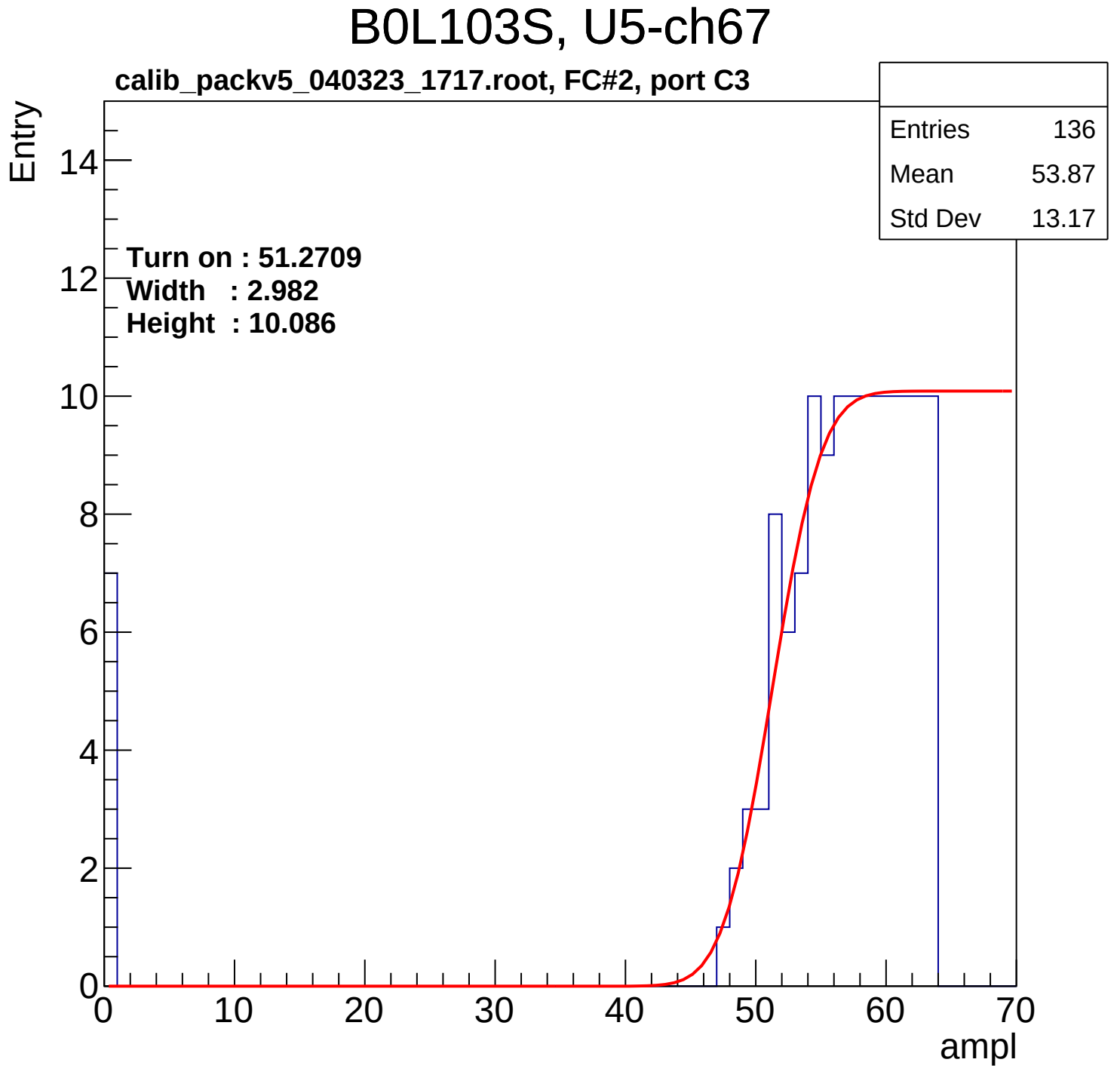
B0L103S, U5-ch67
calib_packv5_040323_1717.root, FC#2, port C3
Entries 136
Mean 53.87
Std Dev 13.17
Turn on : 51.2709
Width : 2.982
Height : 10.086
Entry
ampl
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6
8
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12
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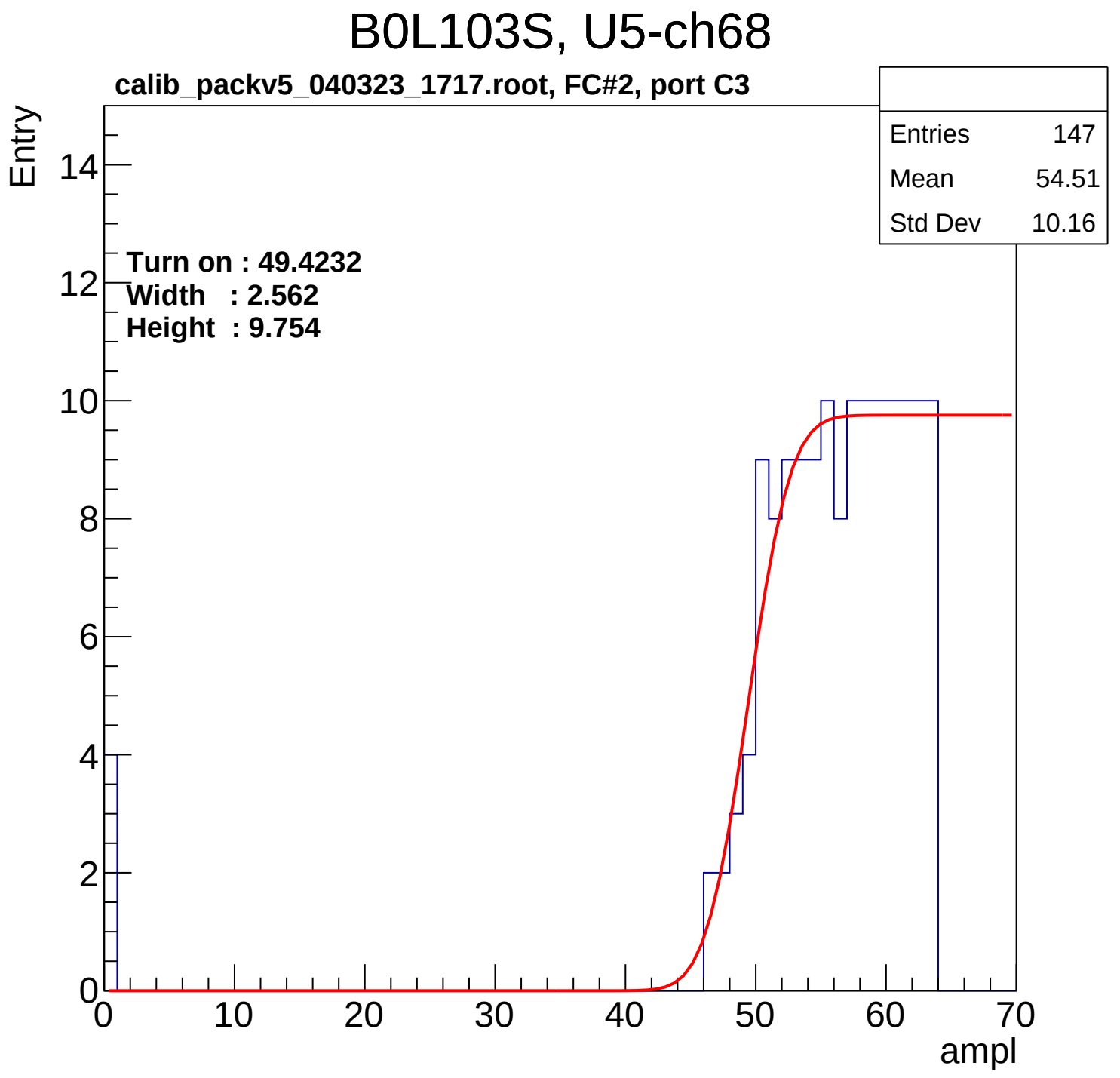
B0L103S, U5-ch68
calib_packv5_040323_1717.root, FC#2, port C3
Entries 147
Mean 54.51
Std Dev 10.16
Turn on : 49.4232
Width : 2.562
Height : 9.754
Entry
ampl
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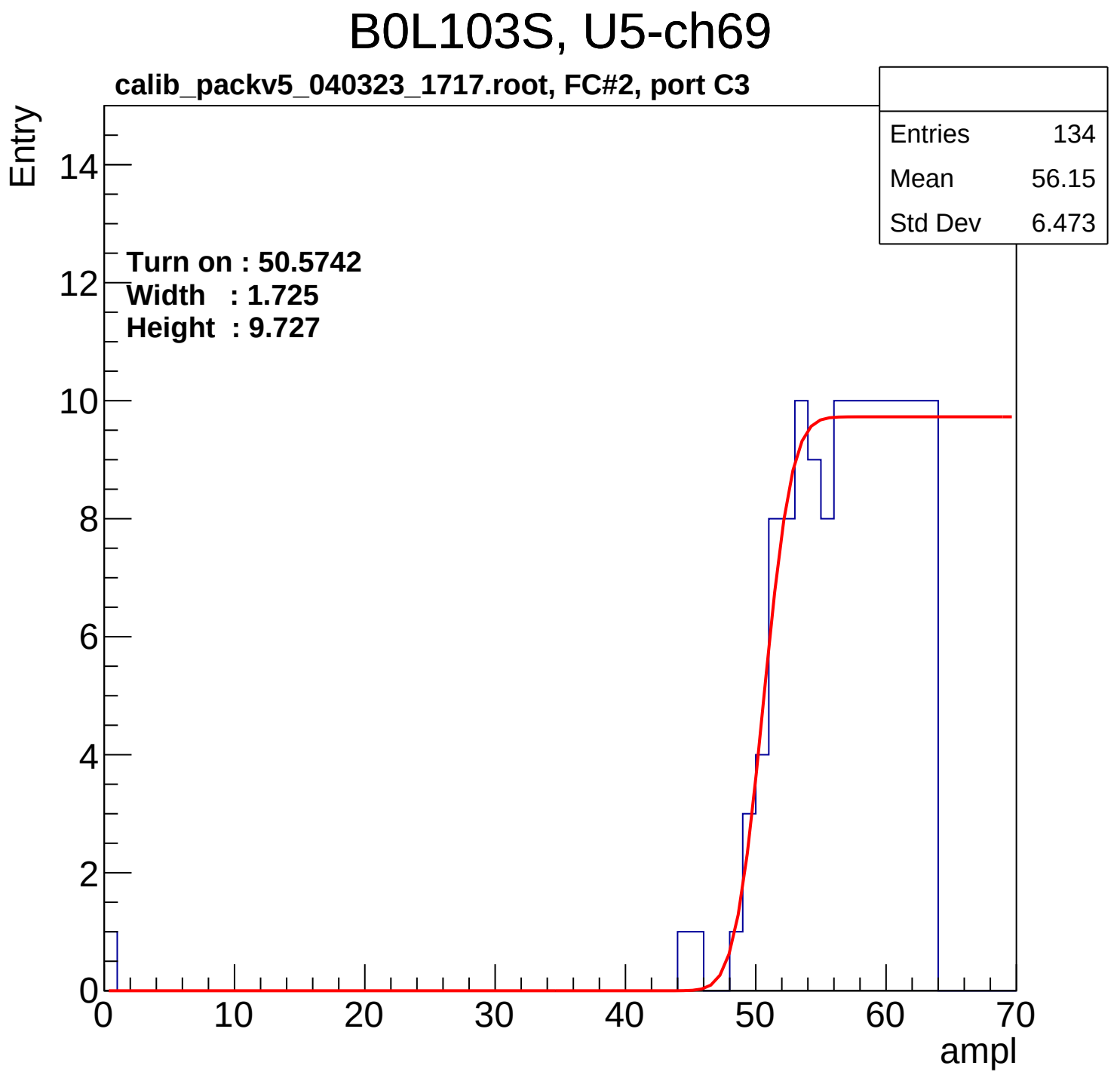
B0L103S, U5-ch69
calib_packv5_040323_1717.root, FC#2, port C3
Entries 134
Mean 56.15
Std Dev 6.473
Turn on : 50.5742
Width : 1.725
Height : 9.727
Entry
ampl
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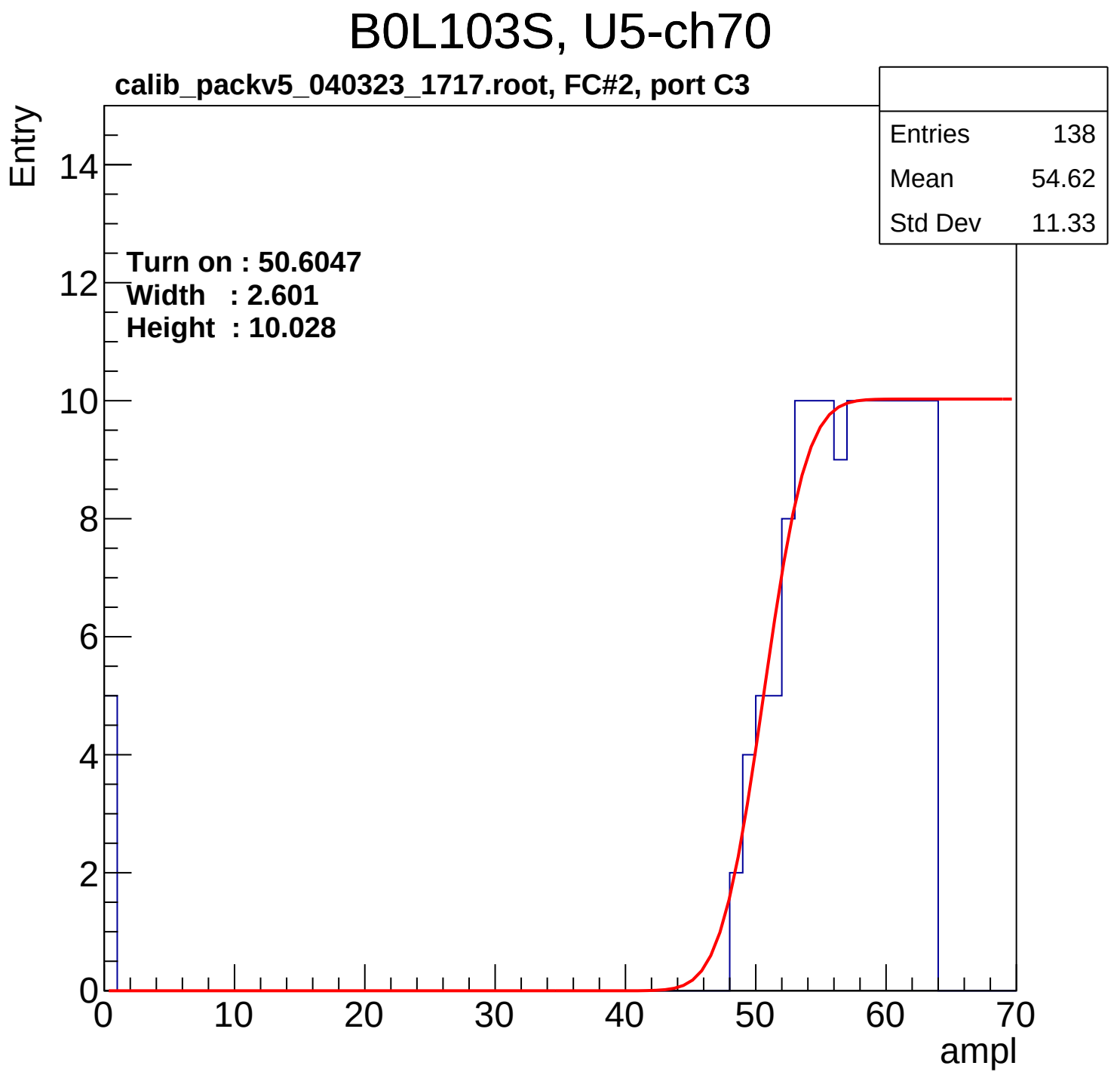
B0L103S, U5-ch70
calib_packv5_040323_1717.root, FC#2, port C3
Entries 138
Mean 54.62
Std Dev 11.33
Turn on : 50.6047
Width : 2.601
Height : 10.028
Entry
ampl
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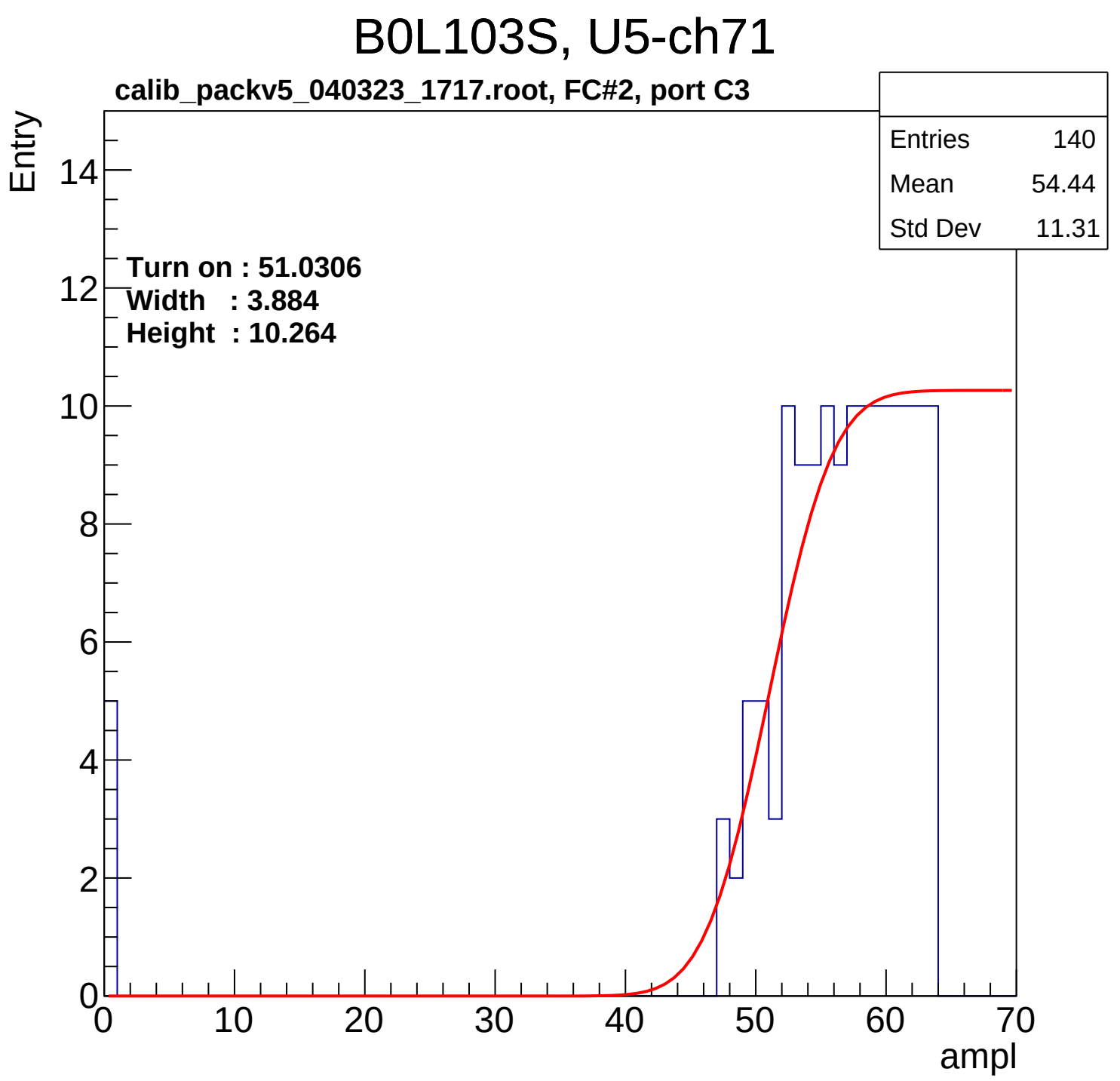
B0L103S, U5-ch71
calib_packv5_040323_1717.root, FC#2, port C3
Entries 140
Mean 54.44
Std Dev 11.31
Turn on : 51.0306
Width : 3.884
Height : 10.264
Entry
ampl
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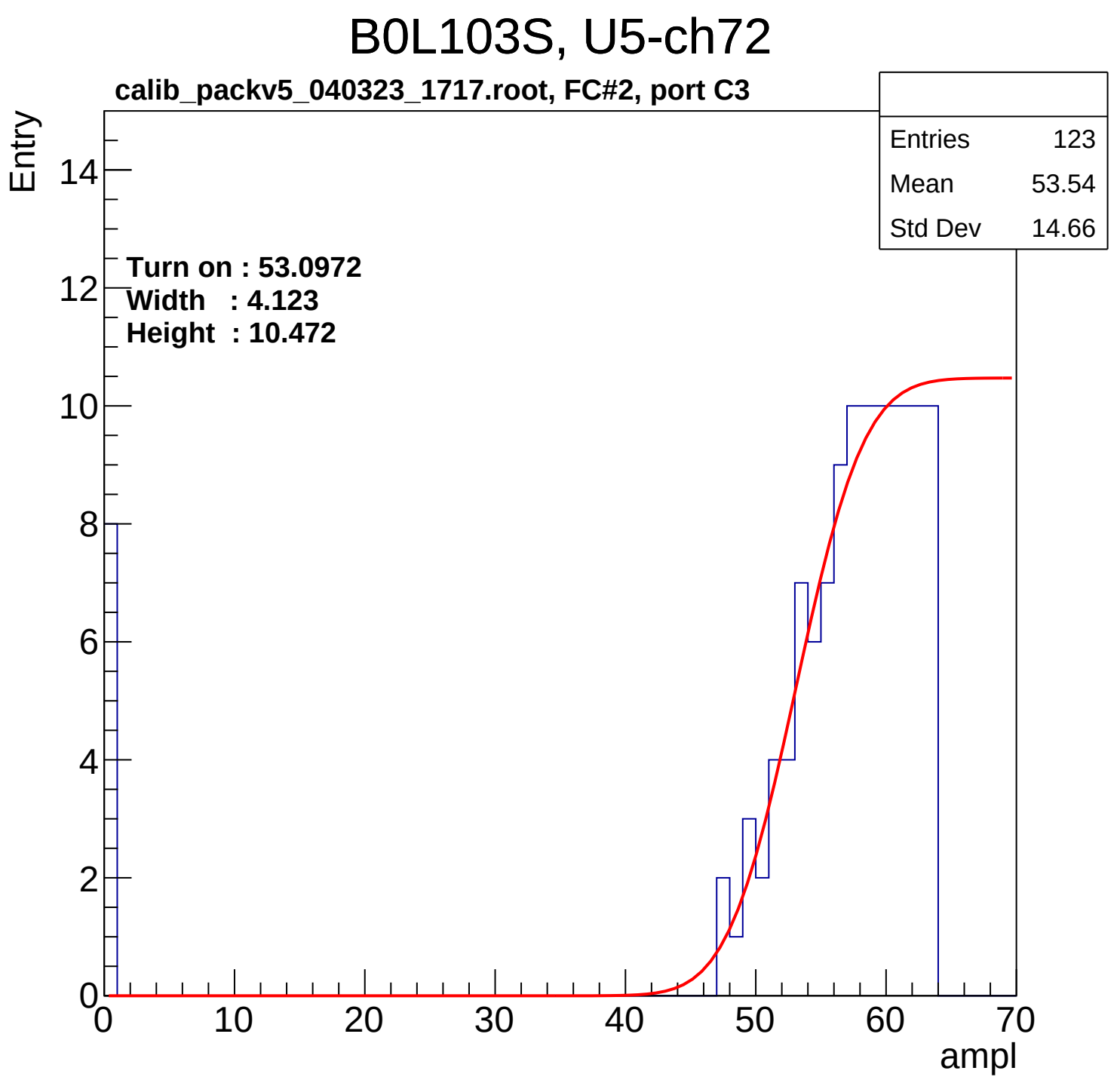
B0L103S, U5-ch72
calib_packv5_040323_1717.root, FC#2, port C3
Entries 123
Mean 53.54
Std Dev 14.66
Turn on : 53.0972
Width : 4.123
Height : 10.472
Entry
ampl
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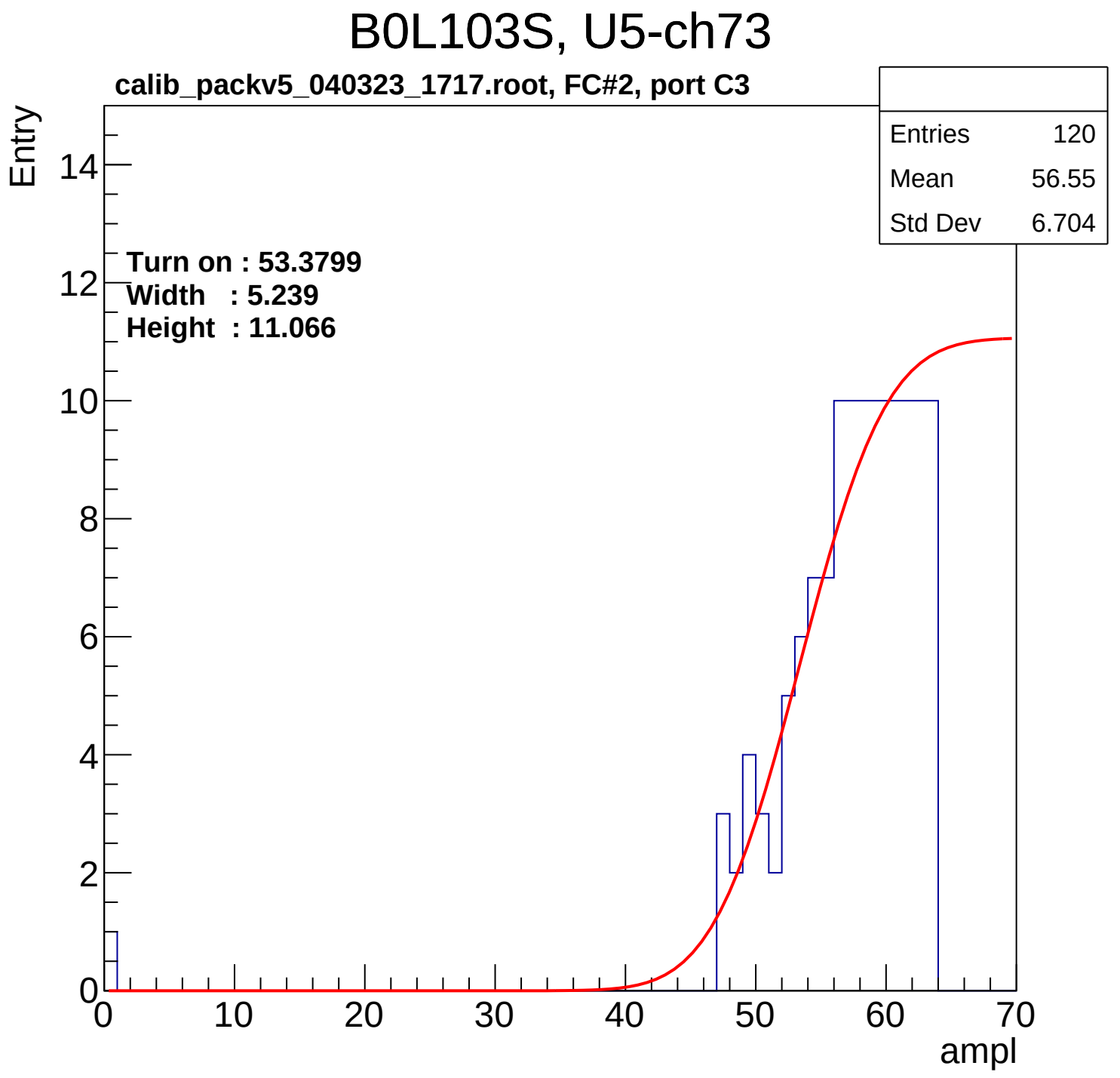
B0L103S, U5-ch73
calib_packv5_040323_1717.root, FC#2, port C3
Entries 120
Mean 56.55
Std Dev 6.704
Turn on : 53.3799
Width : 5.239
Height : 11.066
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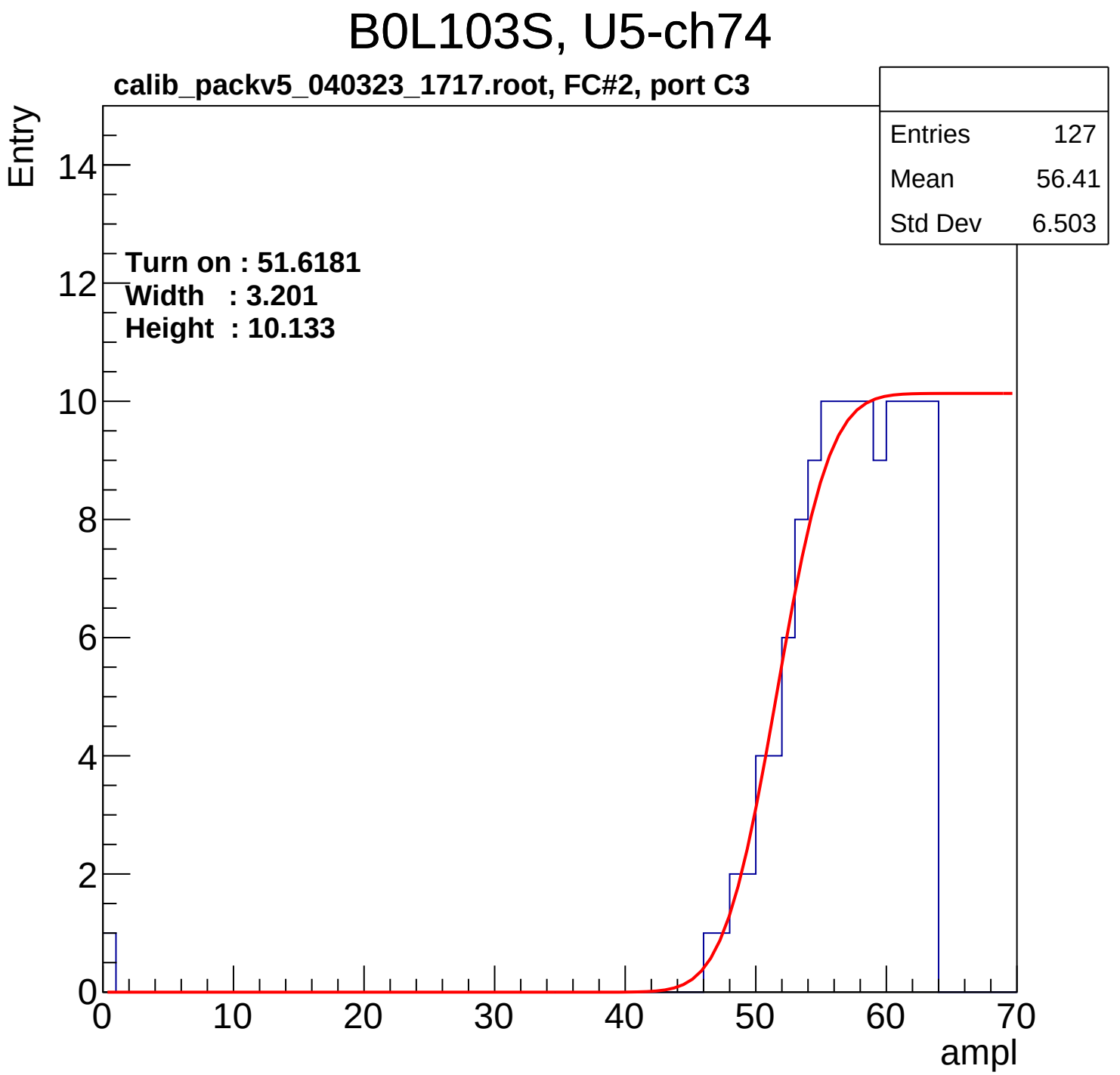
B0L103S, U5-ch74
calib_packv5_040323_1717.root, FC#2, port C3
Entries 127
Mean 56.41
Std Dev 6.503
Turn on : 51.6181
Width : 3.201
Height : 10.133
Entry
ampl
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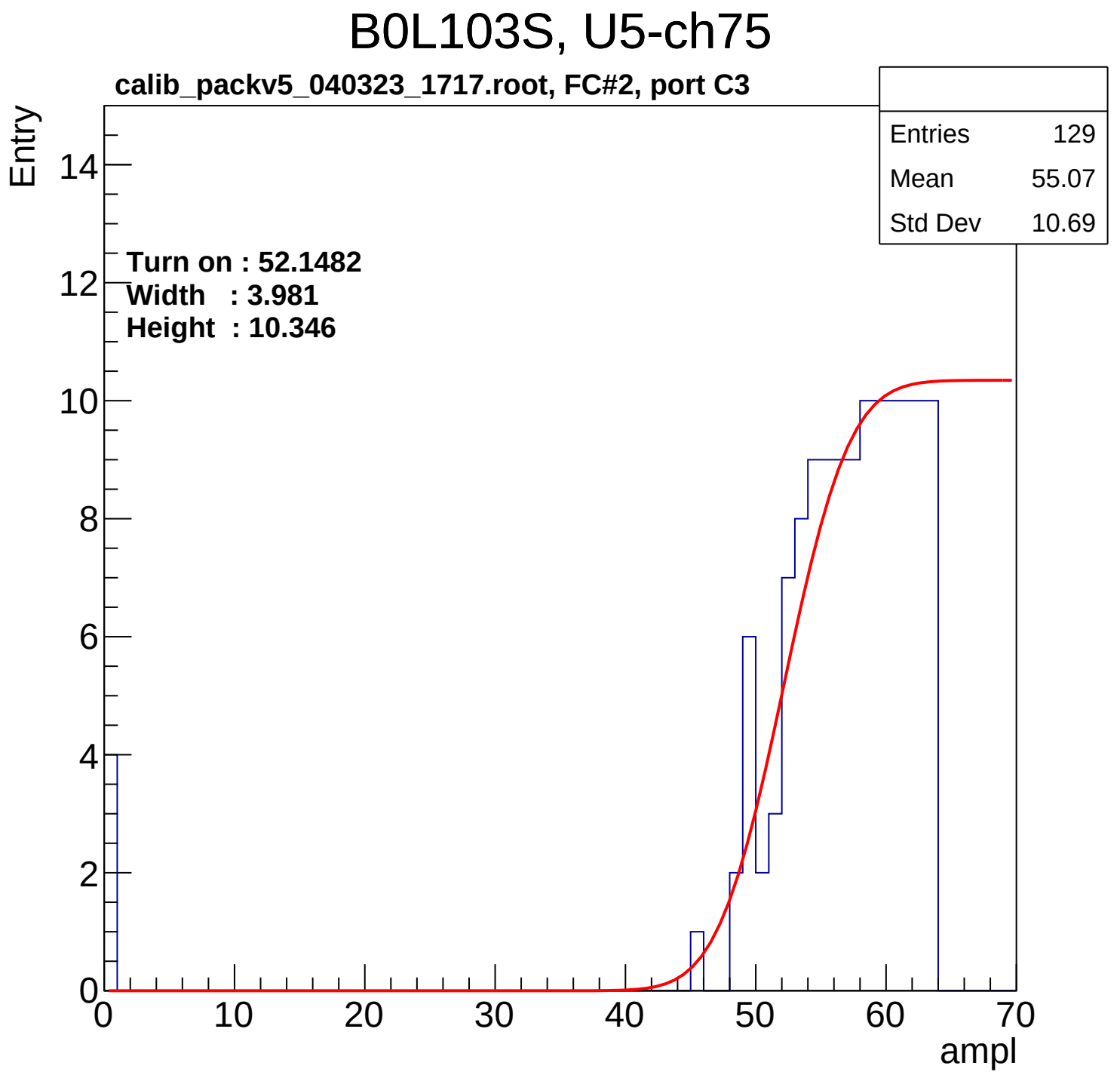
B0L103S, U5-ch75
calib_packv5_040323_1717.root, FC#2, port C3
Entries 129
Mean 55.07
Std Dev 10.69
Turn on : 52.1482
Width : 3.981
Height : 10.346
Entry
ampl
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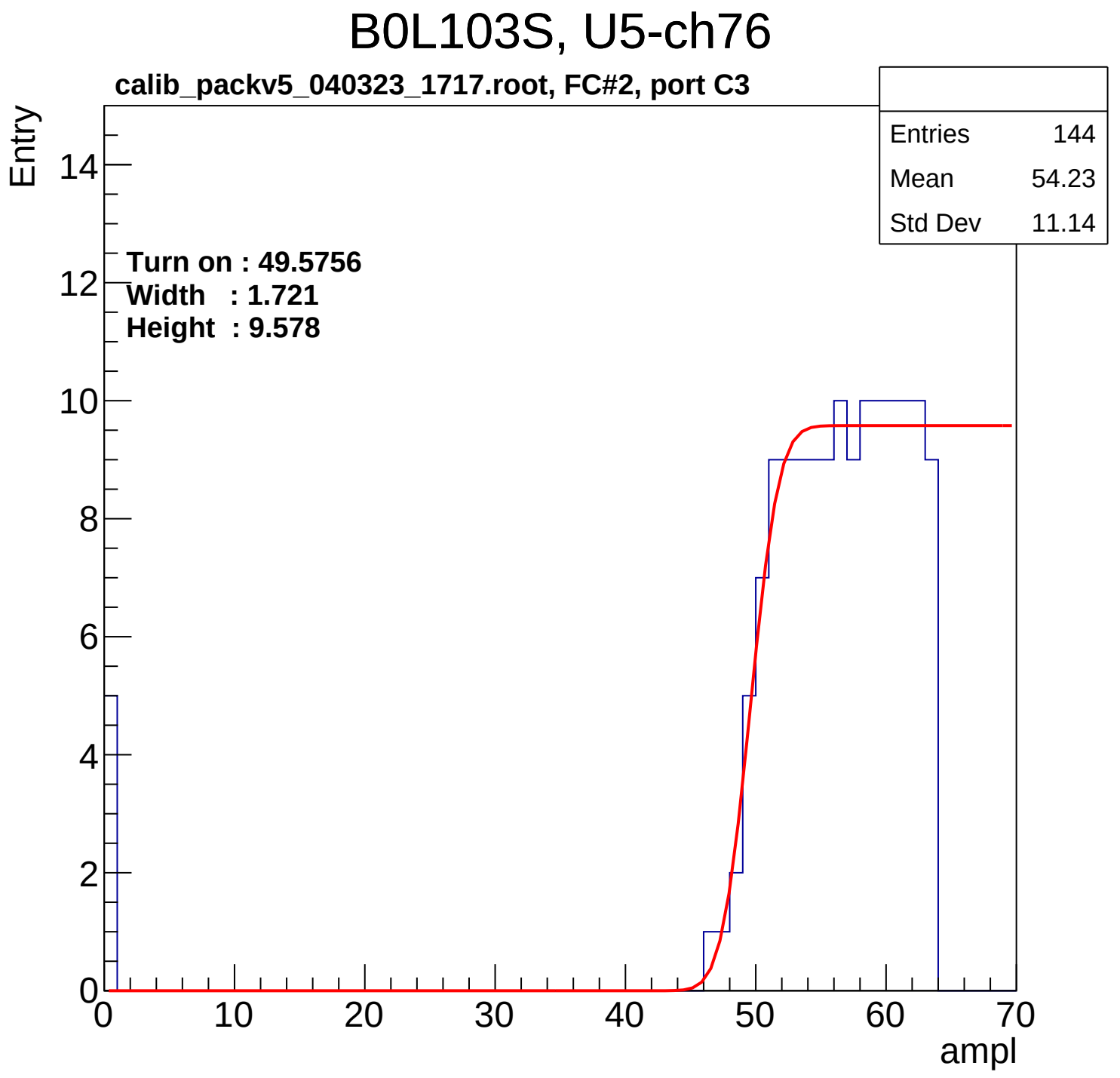
B0L103S, U5-ch76
calib_packv5_040323_1717.root, FC#2, port C3
Entries 144
Mean 54.23
Std Dev 11.14
Turn on : 49.5756
Width : 1.721
Height : 9.578
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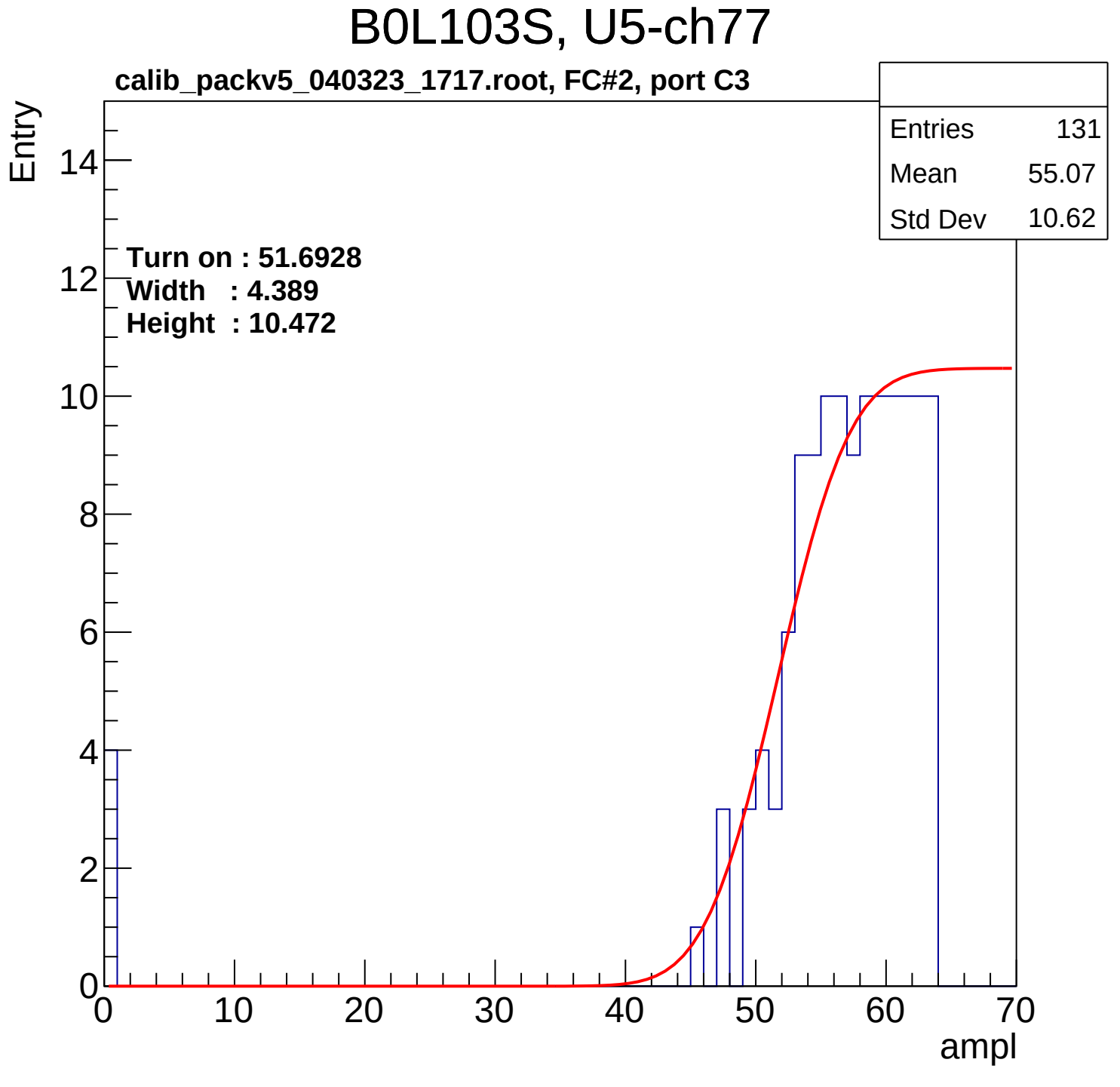
B0L103S, U5-ch77
calib_packv5_040323_1717.root, FC#2, port C3
Entries 131
Mean 55.07
Std Dev 10.62
Turn on : 51.6928
Width : 4.389
Height : 10.472
Entry
ampl
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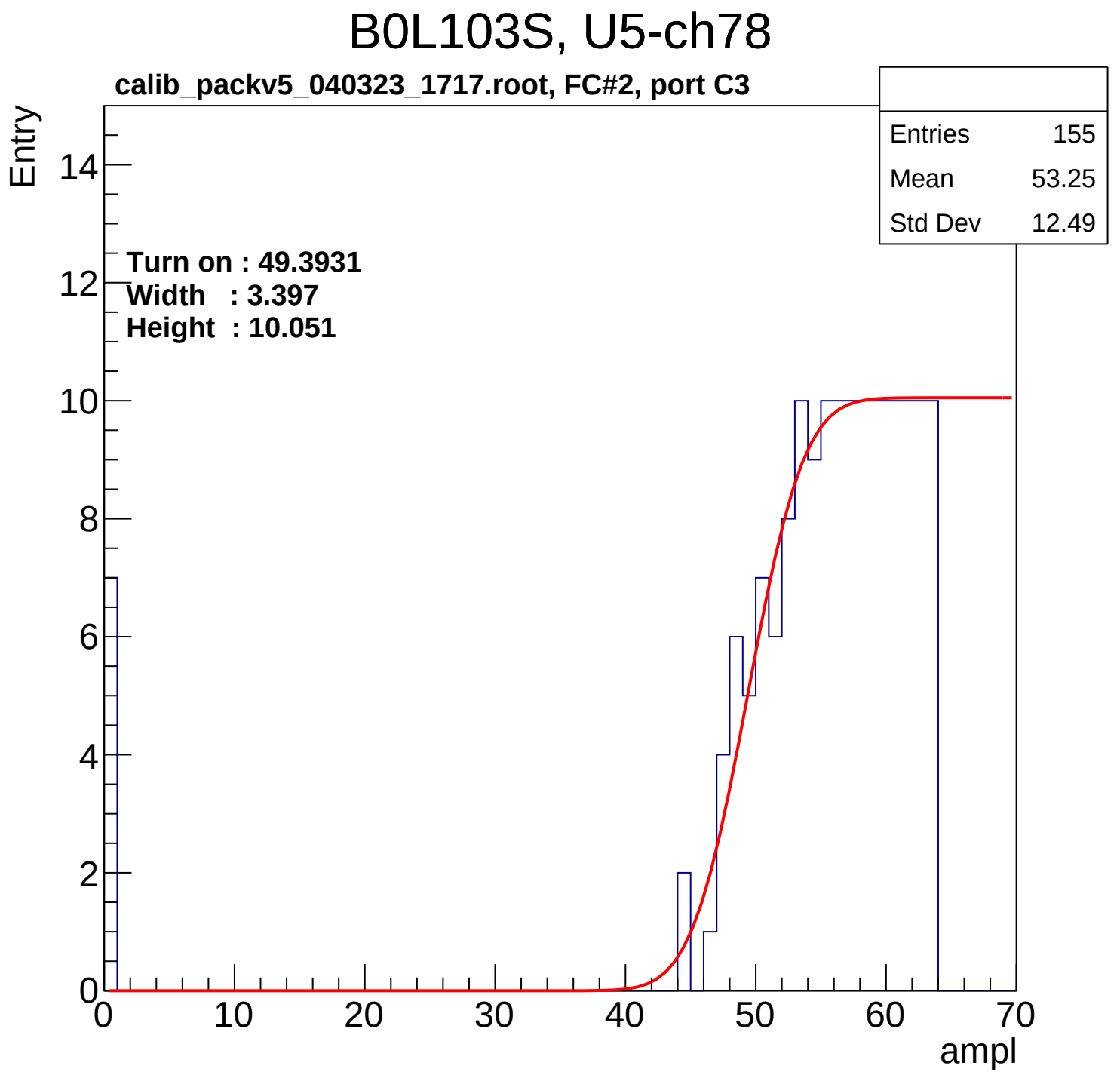
B0L103S, U5-ch78
calib_packv5_040323_1717.root, FC#2, port C3
Entries 155
Mean 53.25
Std Dev 12.49
Turn on : 49.3931
Width : 3.397
Height : 10.051
Entry
ampl
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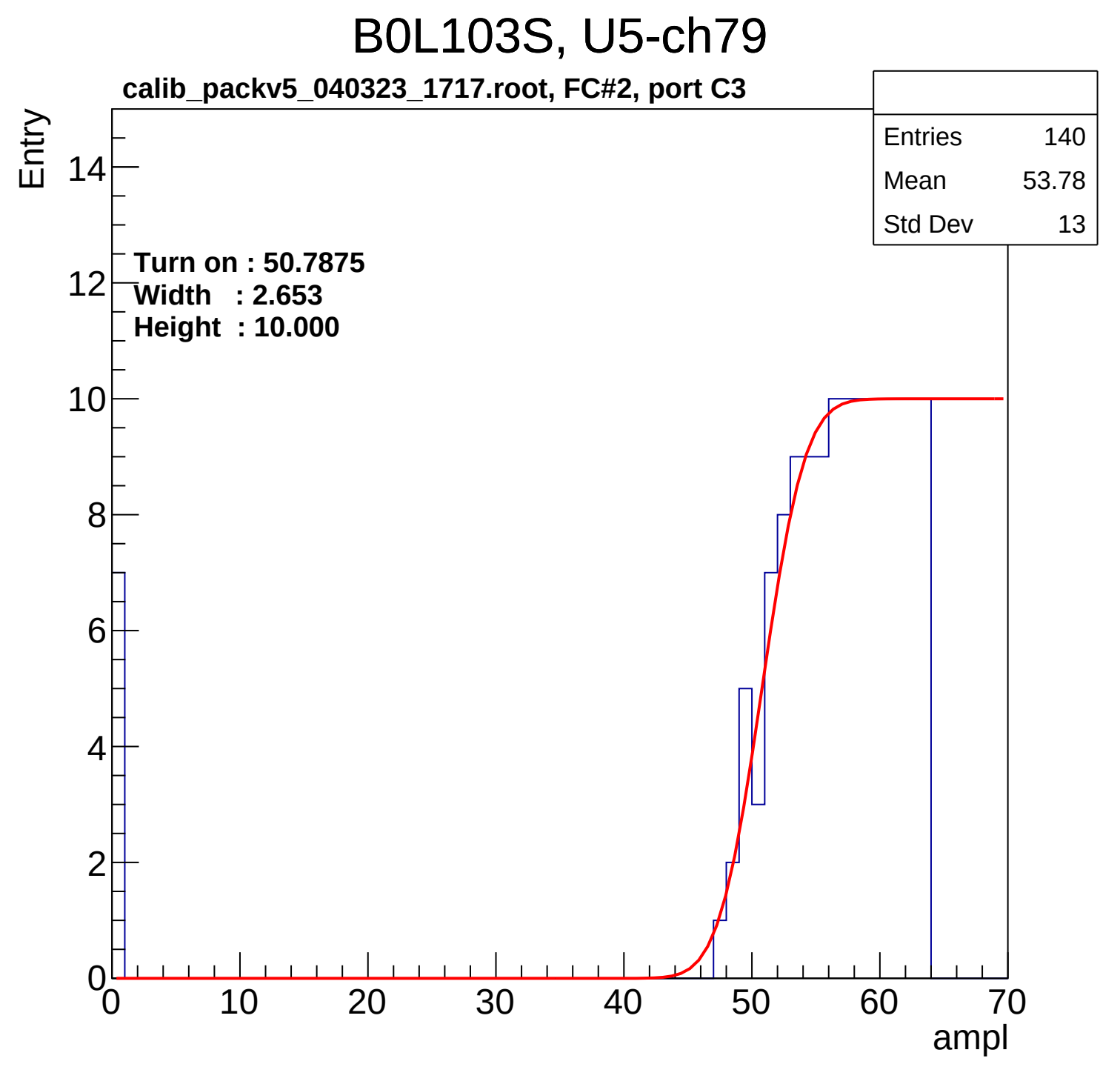
B0L103S, U5-ch79
calib_packv5_040323_1717.root, FC#2, port C3
Entries 140
Mean 53.78
Std Dev 13
Turn on : 50.7875
Width : 2.653
Height : 10.000
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ampl
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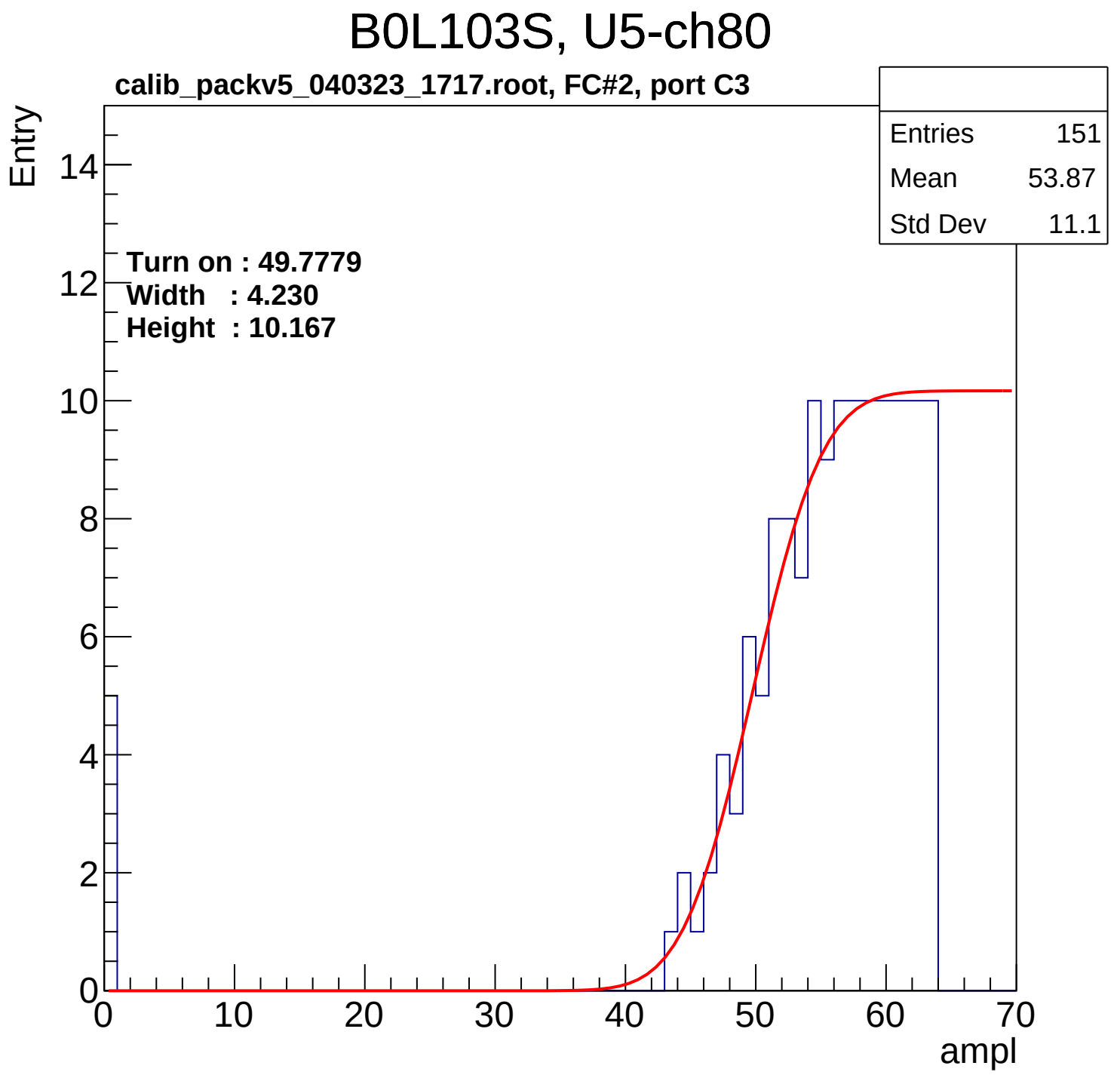
B0L103S, U5-ch80
calib_packv5_040323_1717.root, FC#2, port C3
Entries 151
Mean 53.87
Std Dev 11.1
Turn on : 49.7779
Width : 4.230
Height : 10.167
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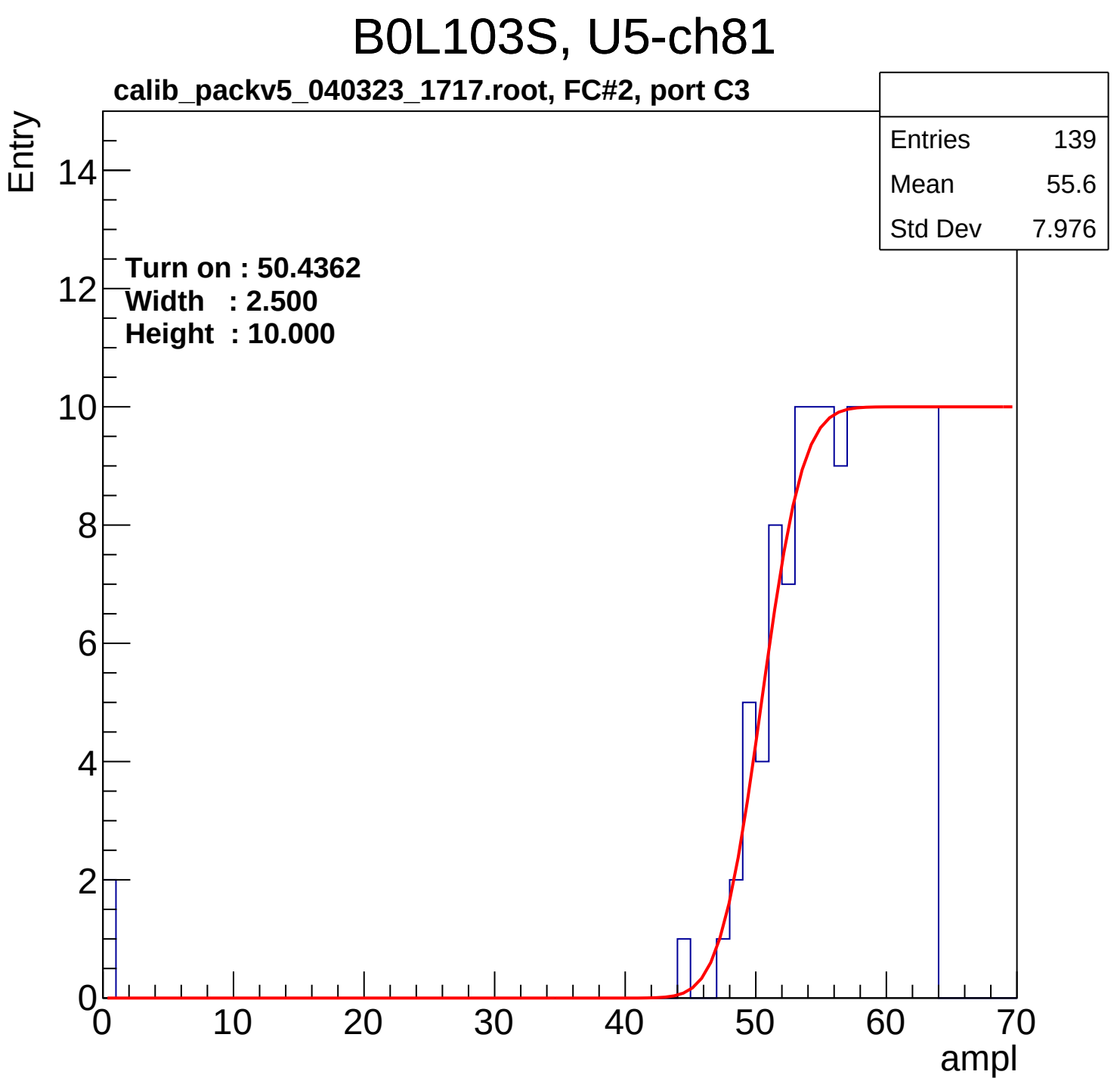
B0L103S, U5-ch81
calib_packv5_040323_1717.root, FC#2, port C3
Entries 139
Mean 55.6
Std Dev 7.976
Turn on : 50.4362
Width : 2.500
Height : 10.000
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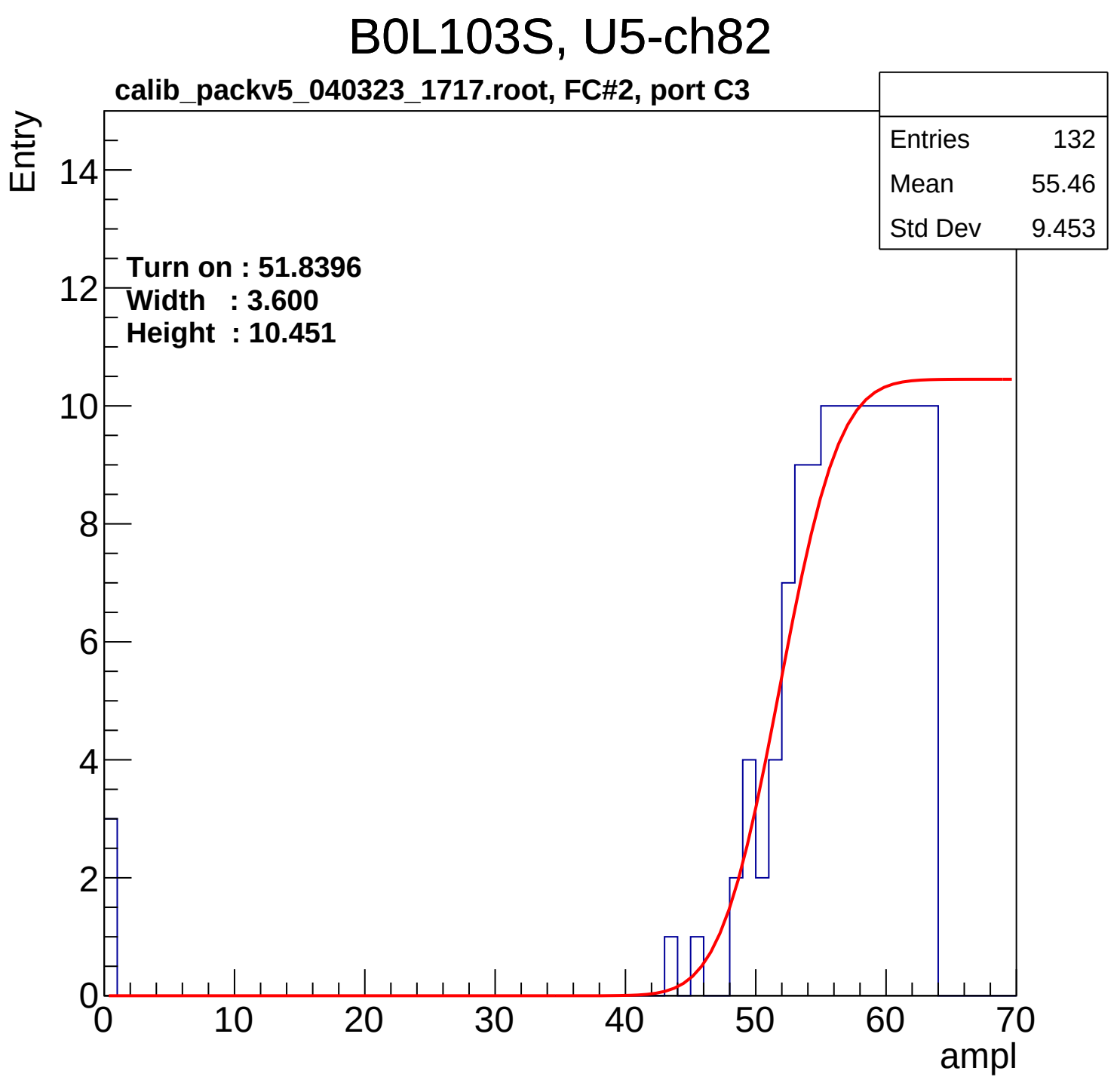
B0L103S, U5-ch82
calib_packv5_040323_1717.root, FC#2, port C3
Entries 132
Mean 55.46
Std Dev 9.453
Turn on : 51.8396
Width : 3.600
Height : 10.451
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ampl
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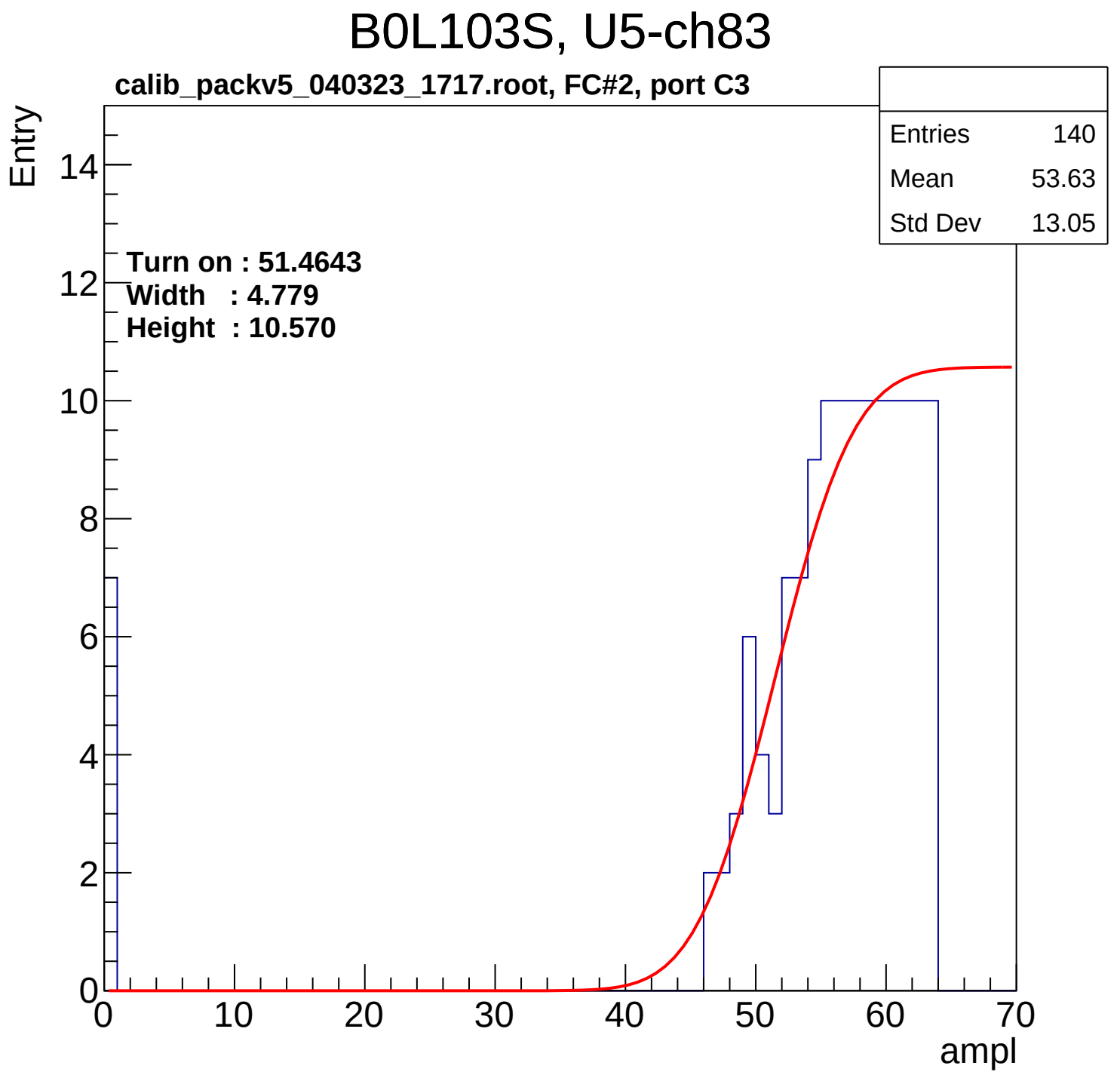
B0L103S, U5-ch83
calib_packv5_040323_1717.root, FC#2, port C3
Entries 140
Mean 53.63
Std Dev 13.05
Turn on : 51.4643
Width : 4.779
Height : 10.570
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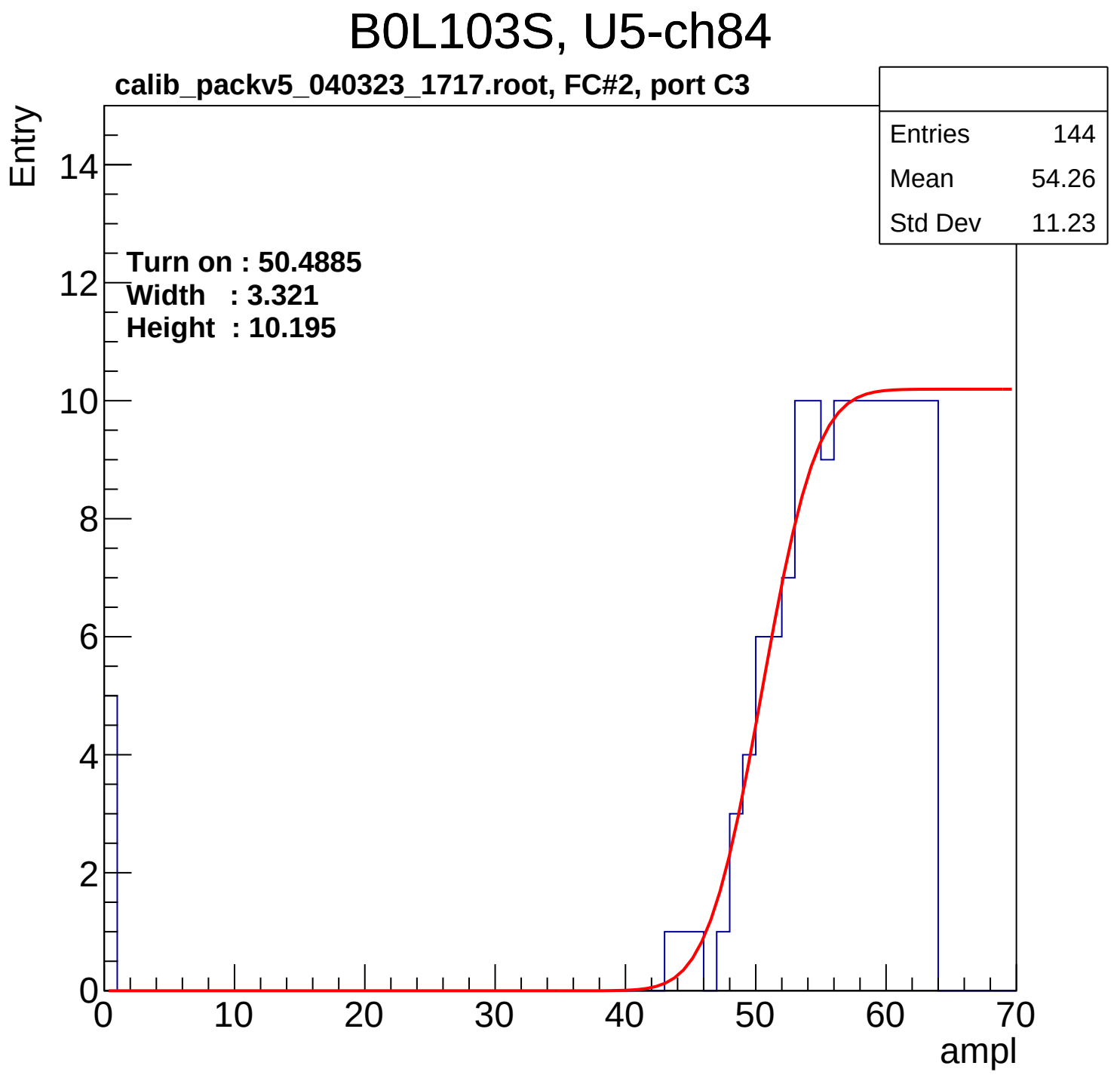
B0L103S, U5-ch84
calib_packv5_040323_1717.root, FC#2, port C3
Entries 144
Mean 54.26
Std Dev 11.23
Turn on : 50.4885
Width : 3.321
Height : 10.195
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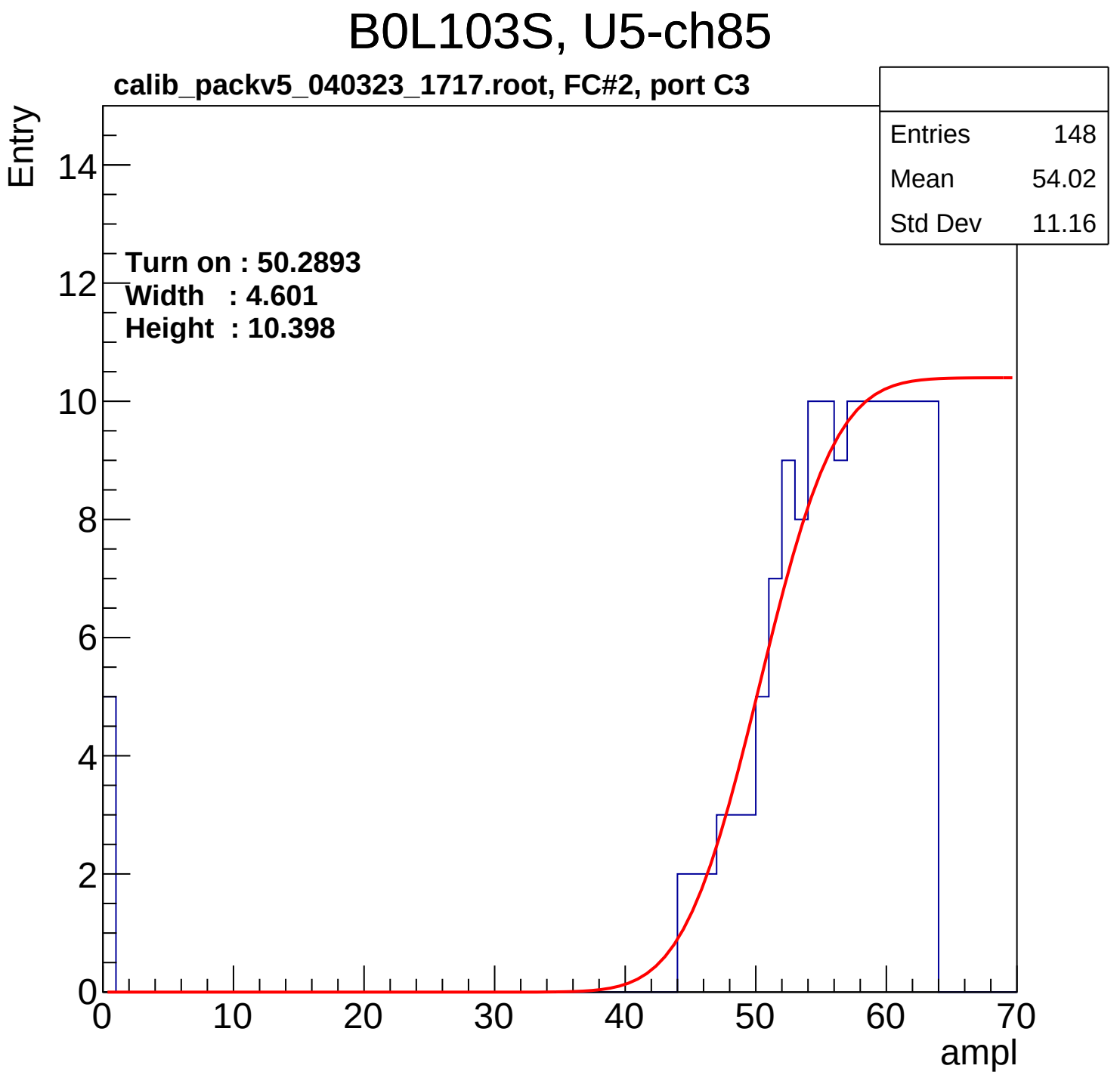
B0L103S, U5-ch85
calib_packv5_040323_1717.root, FC#2, port C3
Entries 148
Mean 54.02
Std Dev 11.16
Turn on : 50.2893
Width : 4.601
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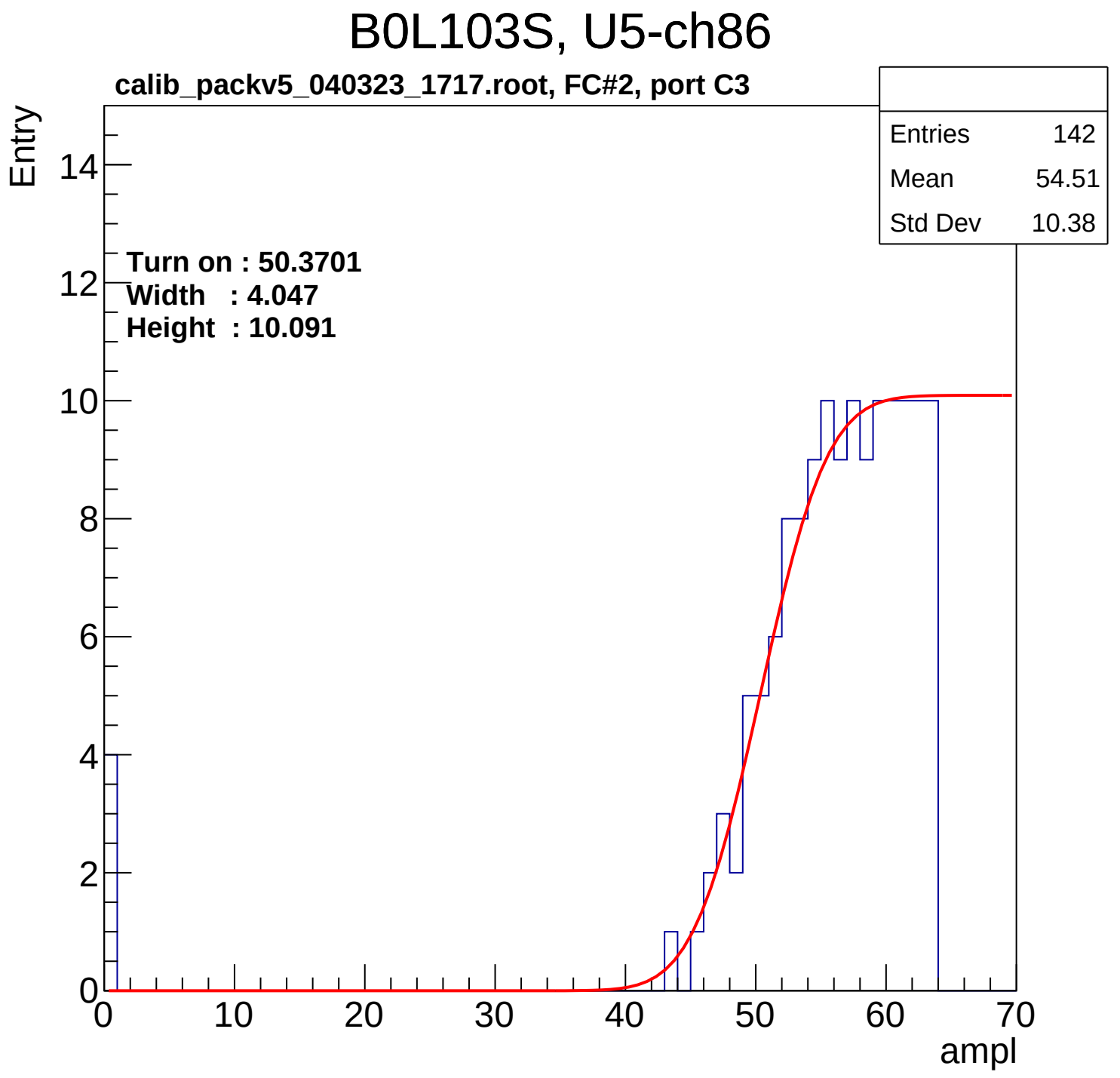
B0L103S, U5-ch86
calib_packv5_040323_1717.root, FC#2, port C3
Entries 142
Mean 54.51
Std Dev 10.38
Turn on : 50.3701
Width : 4.047
Height : 10.091
Entry
ampl
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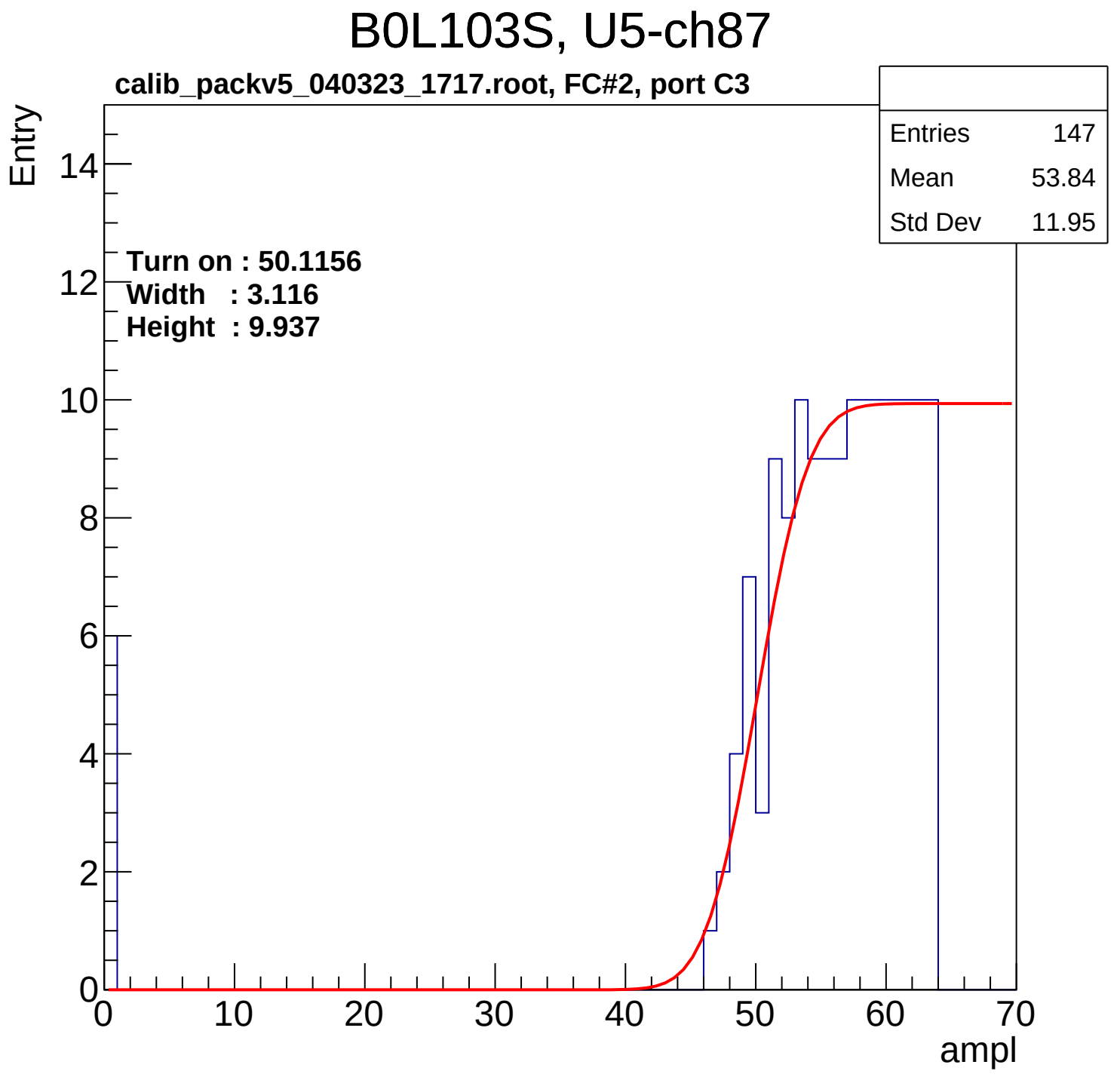
B0L103S, U5-ch87
calib_packv5_040323_1717.root, FC#2, port C3
Entries 147
Mean 53.84
Std Dev 11.95
Turn on : 50.1156
Width : 3.116
Height : 9.937
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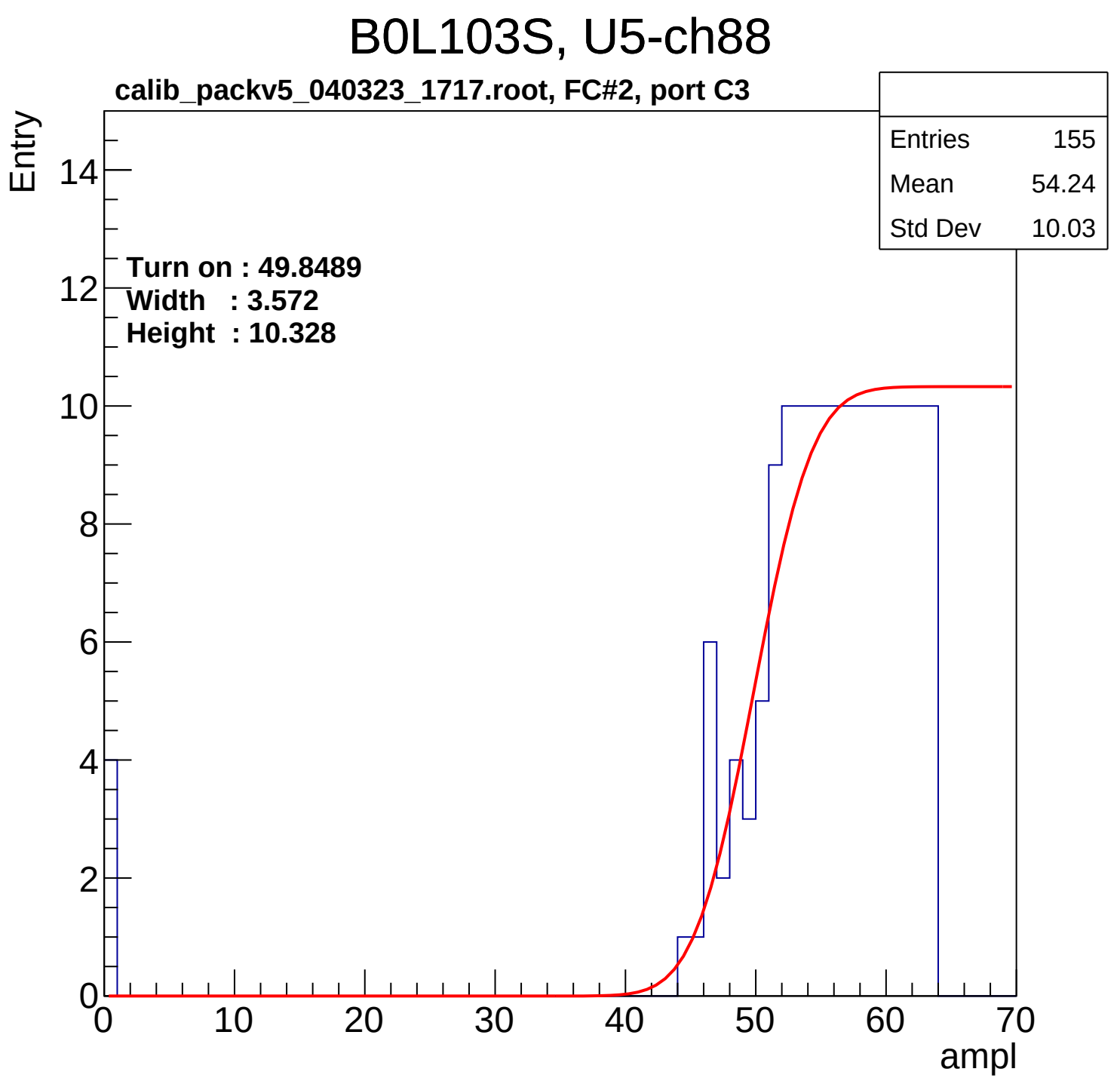
B0L103S, U5-ch88
calib_packv5_040323_1717.root, FC#2, port C3
Entries 155
Mean 54.24
Std Dev 10.03
Turn on : 49.8489
Width : 3.572
Height : 10.328
Entry
ampl
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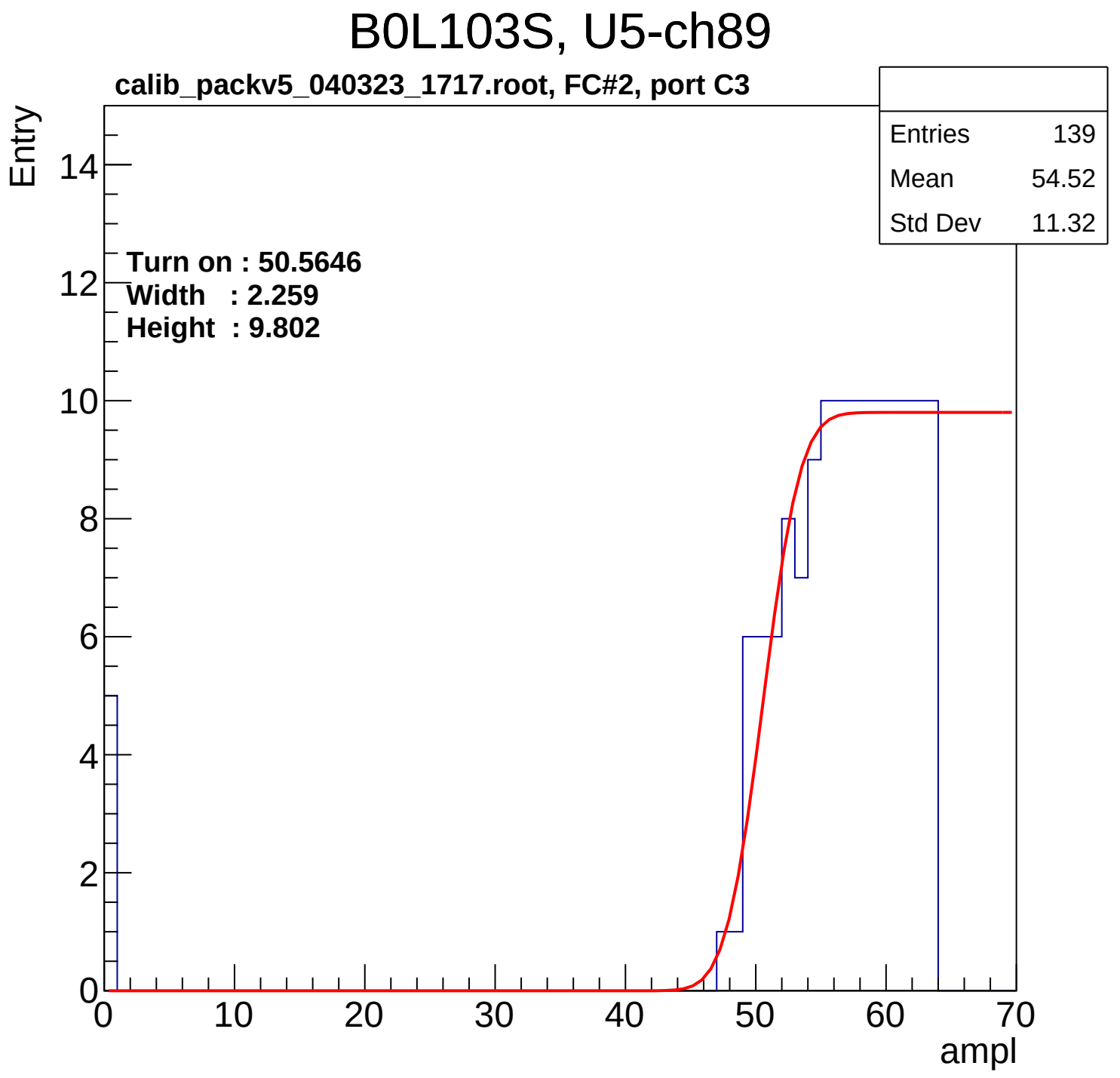
B0L103S, U5-ch89
calib_packv5_040323_1717.root, FC#2, port C3
Entries 139
Mean 54.52
Std Dev 11.32
Turn on : 50.5646
Width : 2.259
Height : 9.802
Entry
ampl
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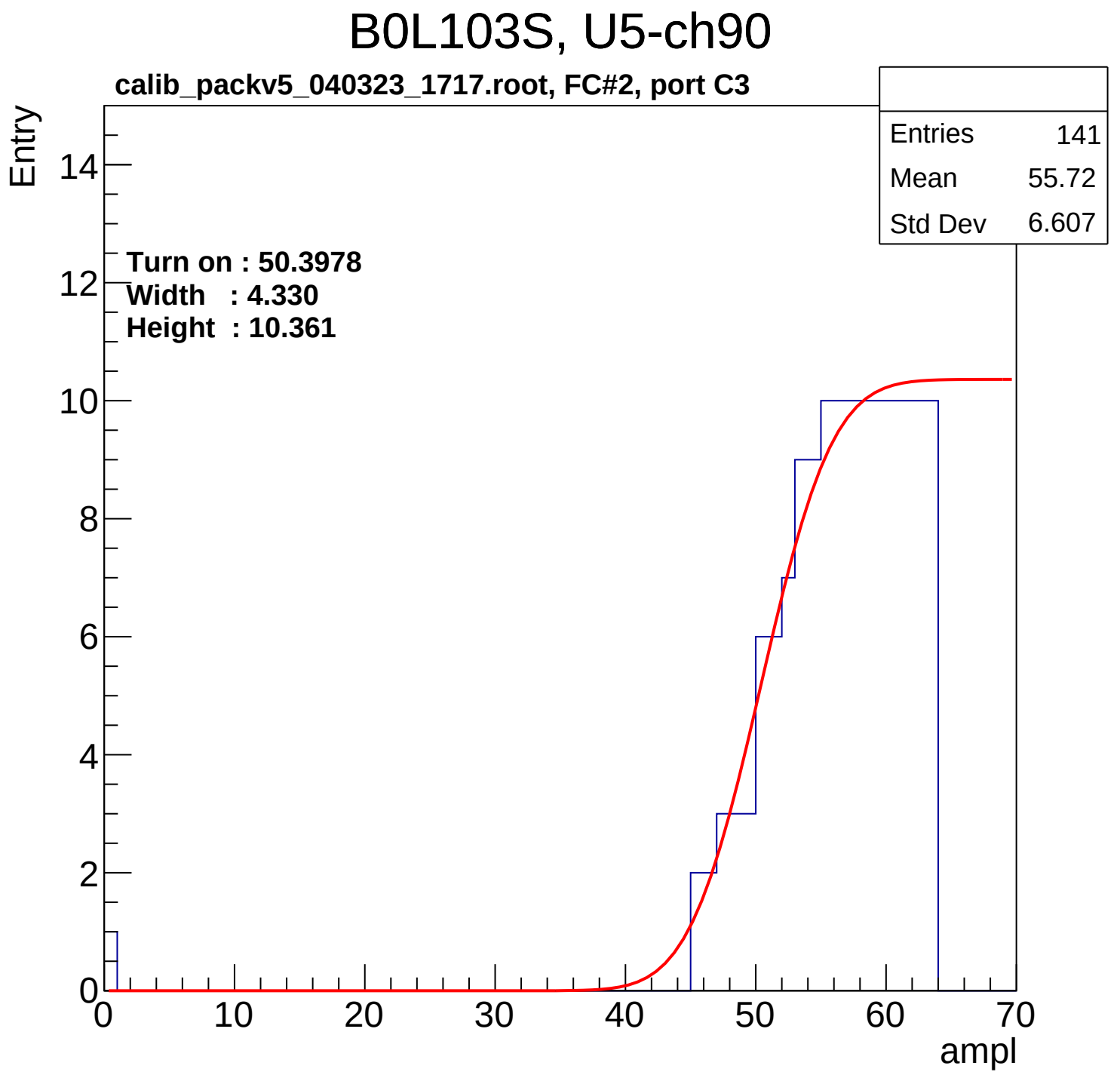
B0L103S, U5-ch90
calib_packv5_040323_1717.root, FC#2, port C3
Entries 141
Mean 55.72
Std Dev 6.607
Turn on : 50.3978
Width : 4.330
Height : 10.361
Entry
ampl
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2
4
6
8
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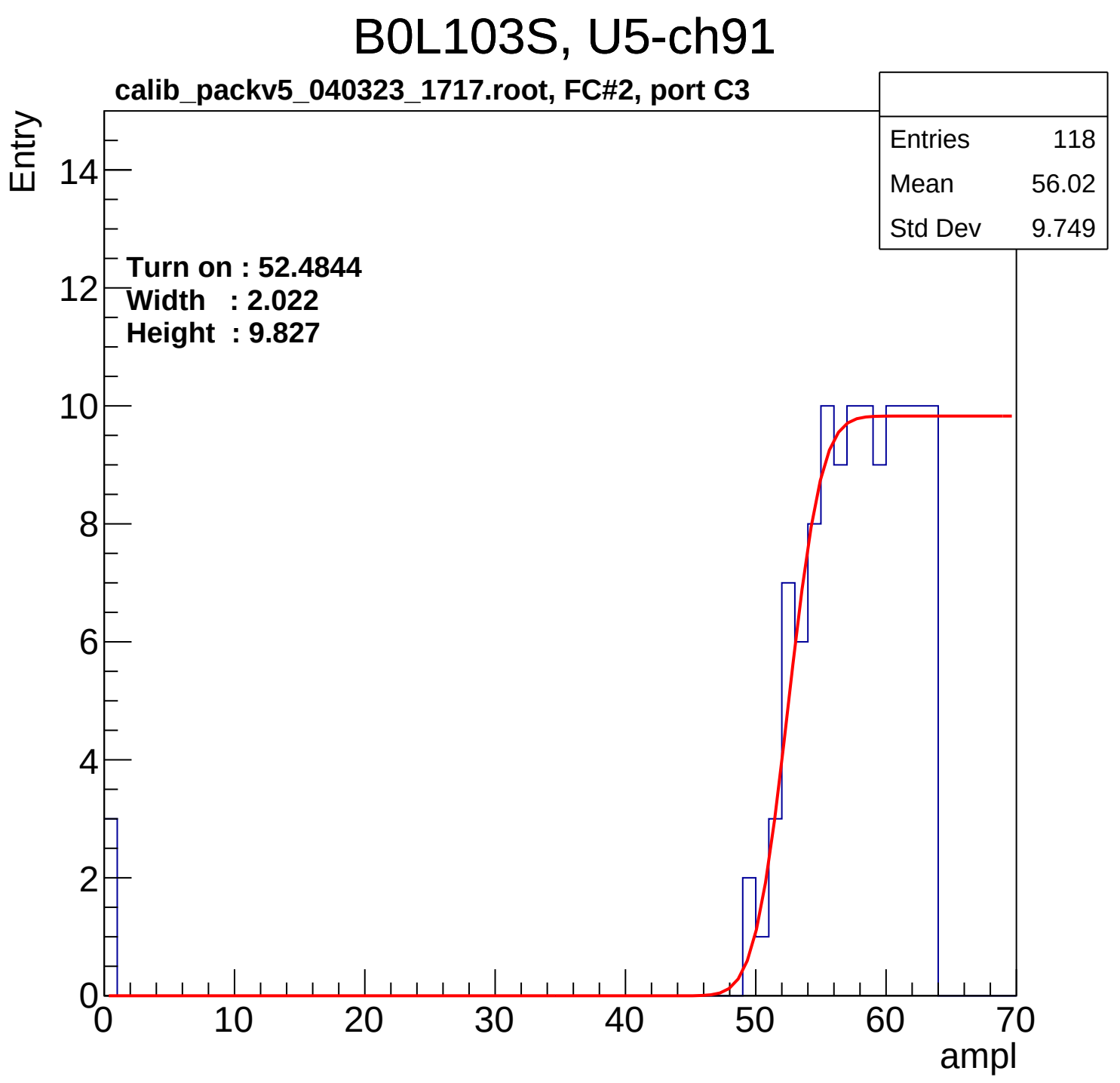
B0L103S, U5-ch91
calib_packv5_040323_1717.root, FC#2, port C3
Entries 118
Mean 56.02
Std Dev 9.749
Turn on : 52.4844
Width : 2.022
Height : 9.827
Entry
ampl
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2
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6
8
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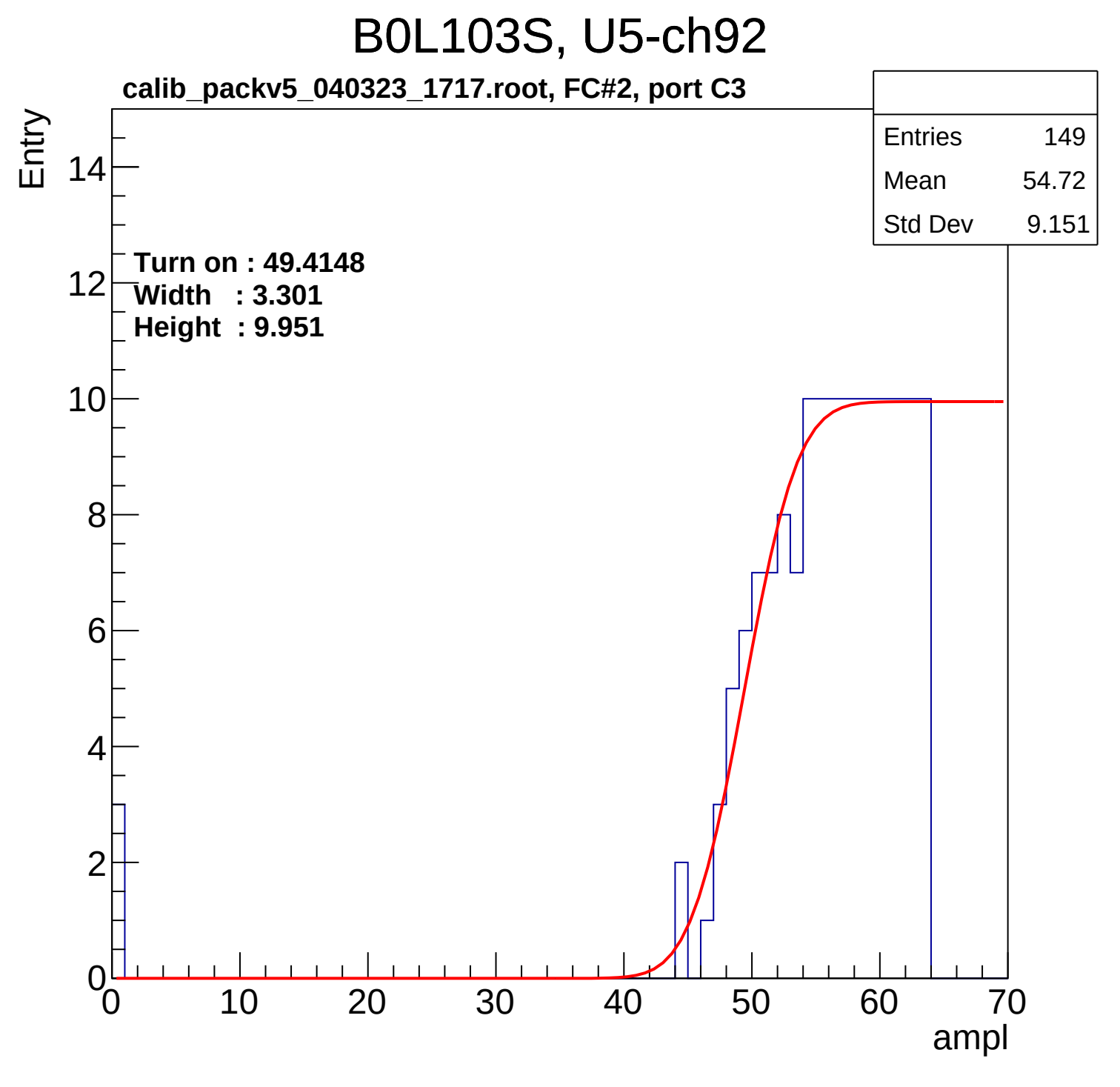
B0L103S, U5-ch92
calib_packv5_040323_1717.root, FC#2, port C3
Entries 149
Mean 54.72
Std Dev 9.151
Turn on : 49.4148
Width : 3.301
Height : 9.951
Entry
ampl
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2
4
6
8
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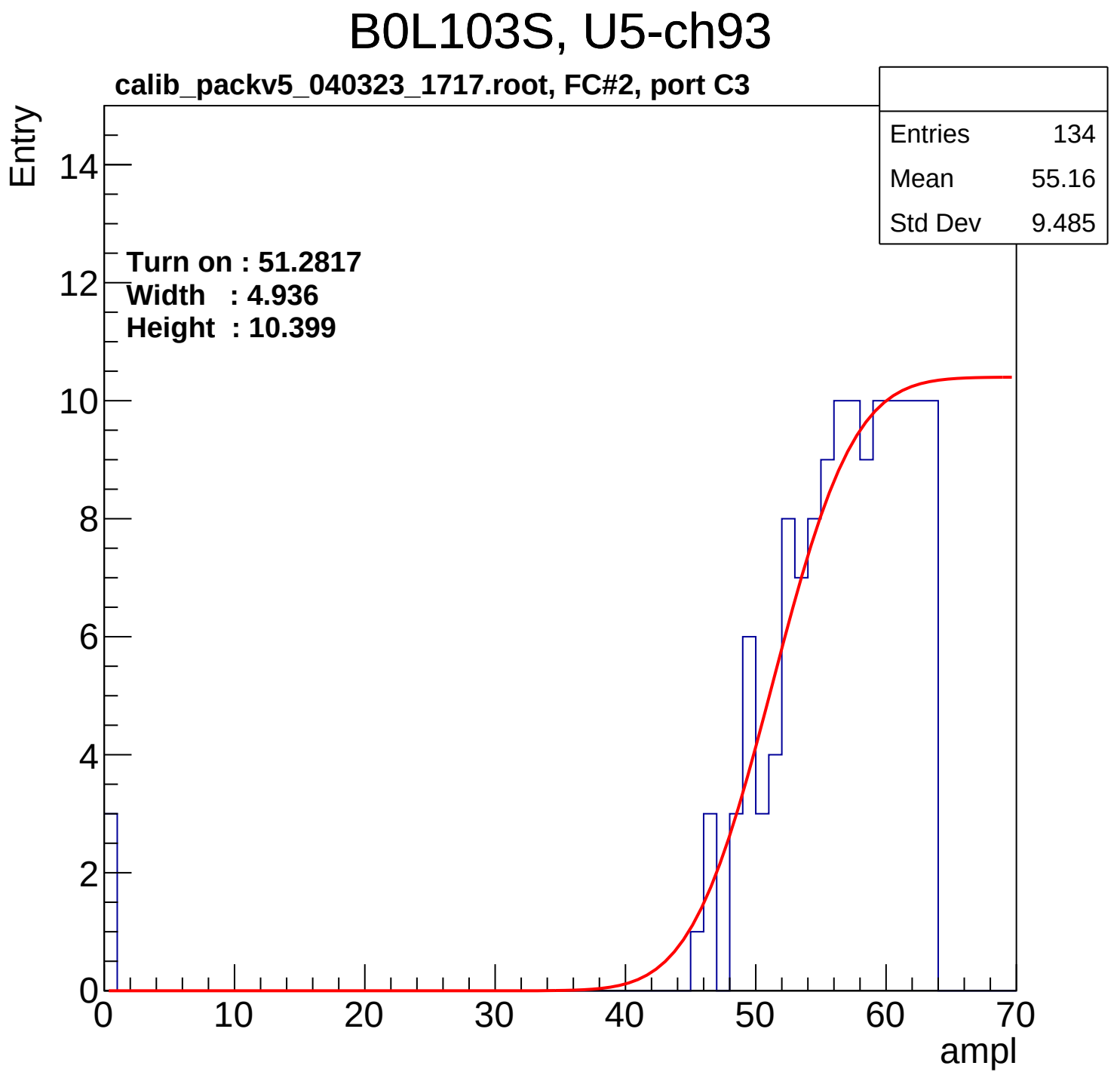
B0L103S, U5-ch93
calib_packv5_040323_1717.root, FC#2, port C3
Entries 134
Mean 55.16
Std Dev 9.485
Turn on : 51.2817
Width : 4.936
Height : 10.399
Entry
ampl
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6
8
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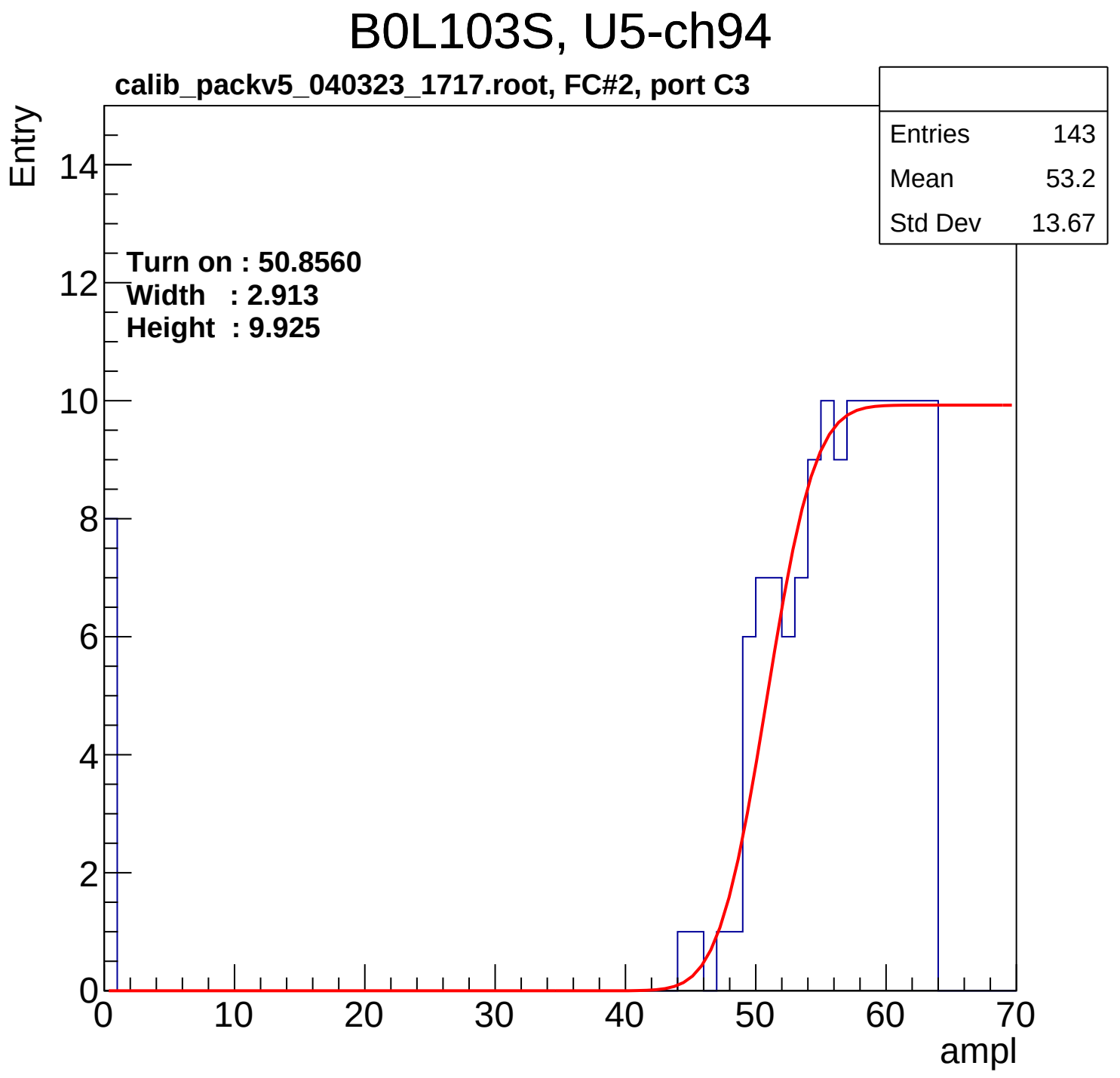
B0L103S, U5-ch94
calib_packv5_040323_1717.root, FC#2, port C3
Entries 143
Mean 53.2
Std Dev 13.67
Turn on : 50.8560
Width : 2.913
Height : 9.925
Entry
ampl
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2
4
6
8
10
12
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0
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20
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60
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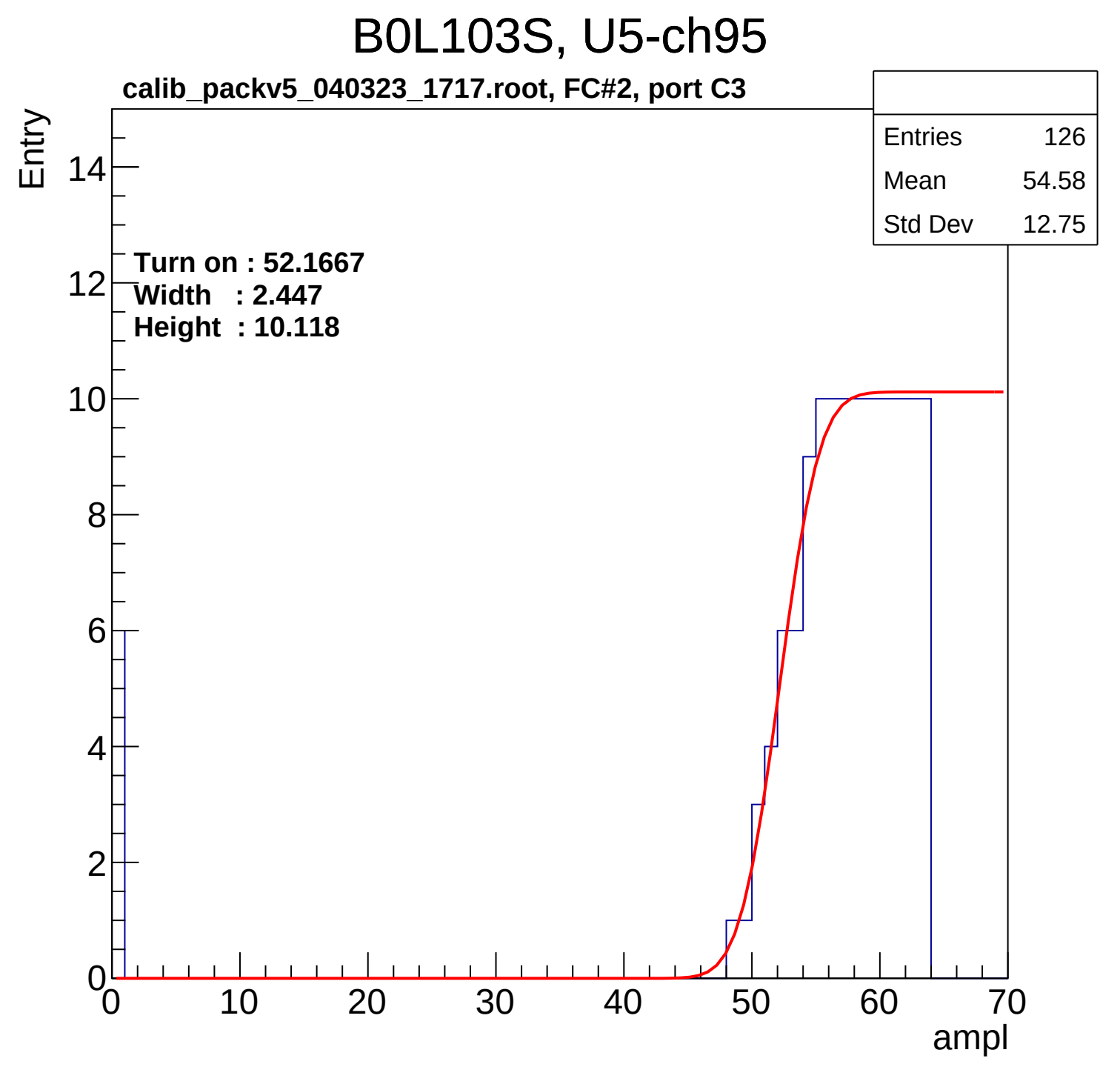
B0L103S, U5-ch95
calib_packv5_040323_1717.root, FC#2, port C3
Entries 126
Mean 54.58
Std Dev 12.75
Turn on : 52.1667
Width : 2.447
Height : 10.118
Entry
ampl
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6
8
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12
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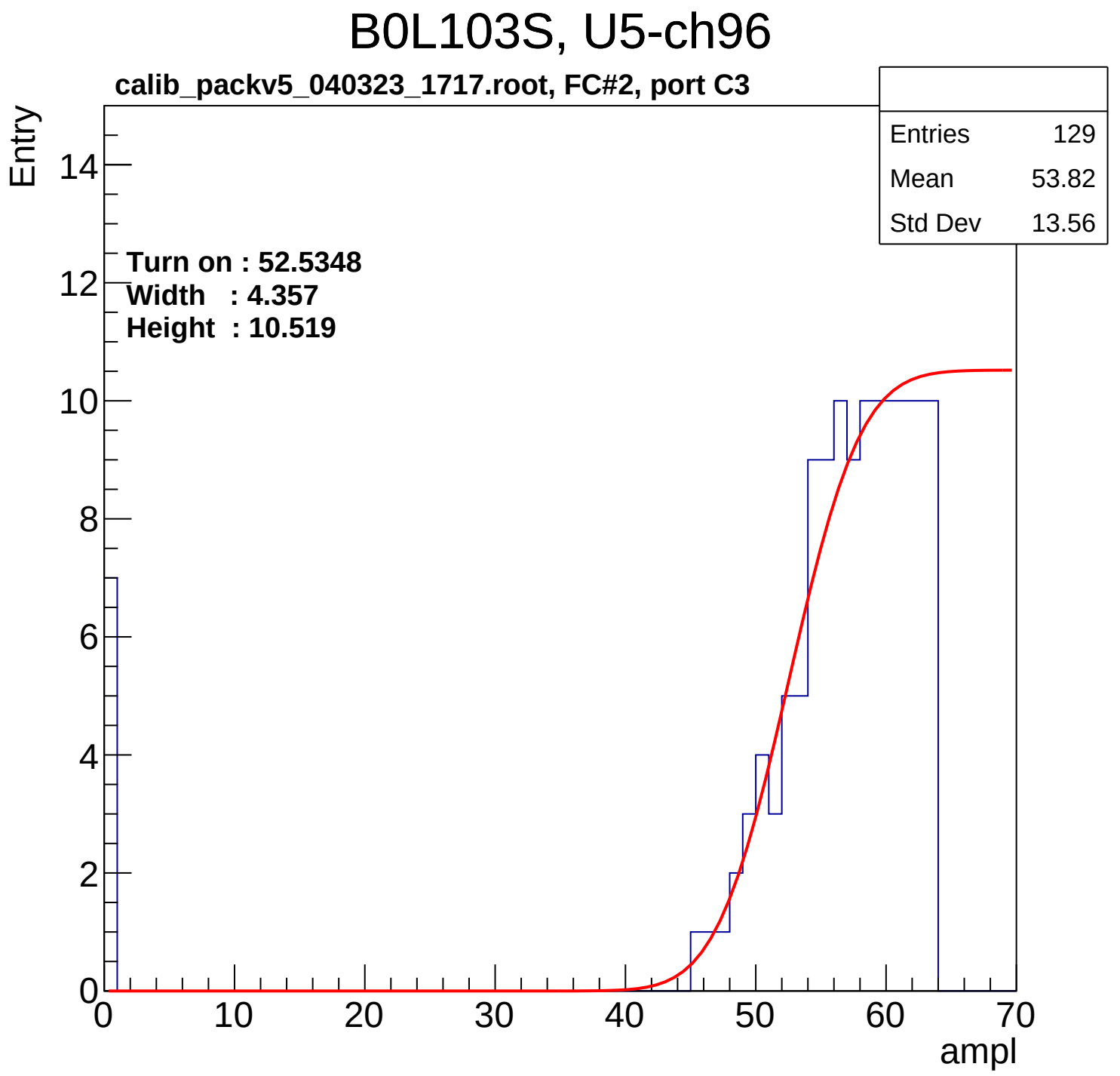
B0L103S, U5-ch96
calib_packv5_040323_1717.root, FC#2, port C3
Entries 129
Mean 53.82
Std Dev 13.56
Turn on : 52.5348
Width : 4.357
Height : 10.519
Entry
ampl
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6
8
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12
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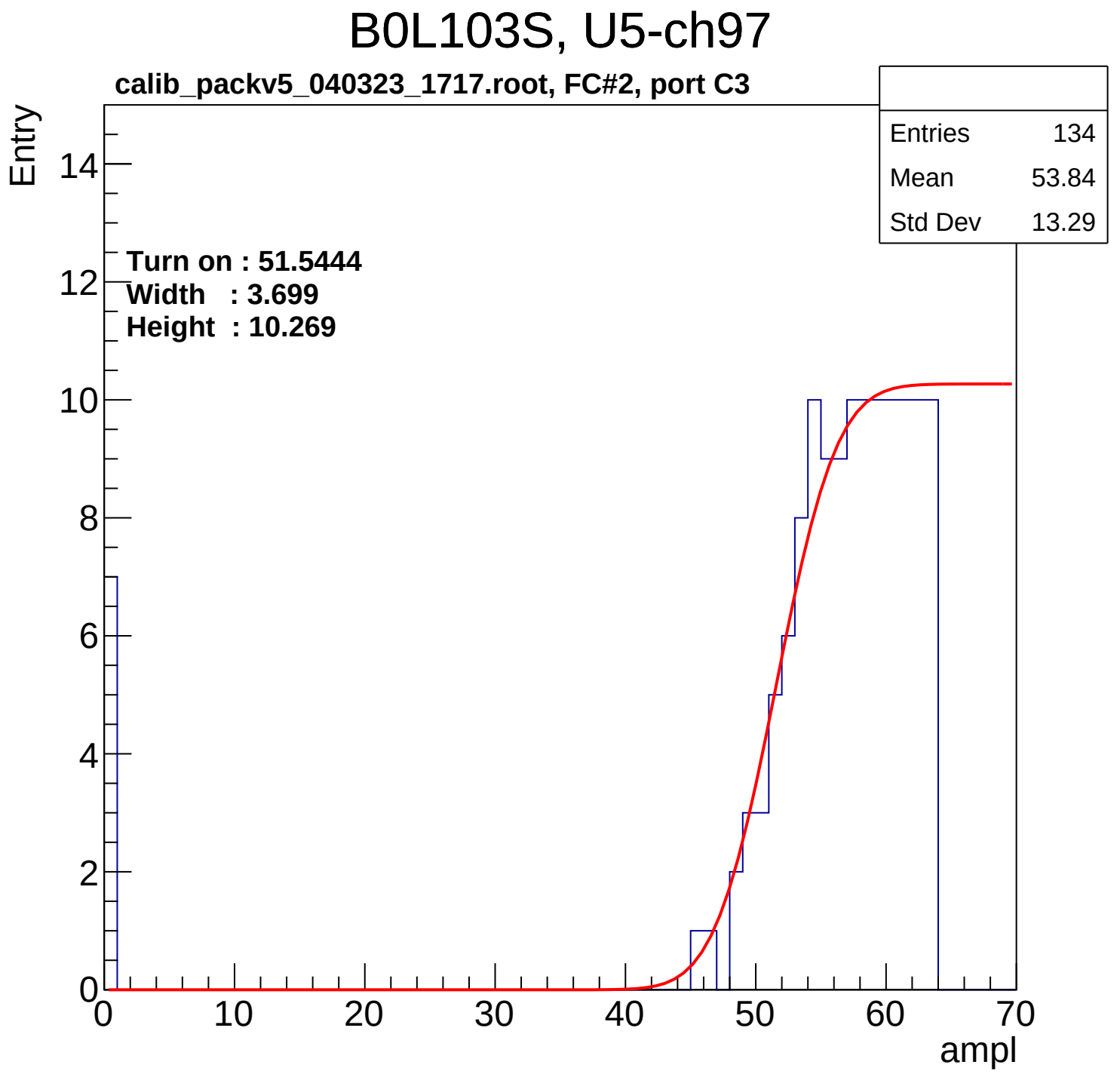
B0L103S, U5-ch97
calib_packv5_040323_1717.root, FC#2, port C3
Entries 134
Mean 53.84
Std Dev 13.29
Turn on : 51.5444
Width : 3.699
Height : 10.269
Entry
ampl
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6
8
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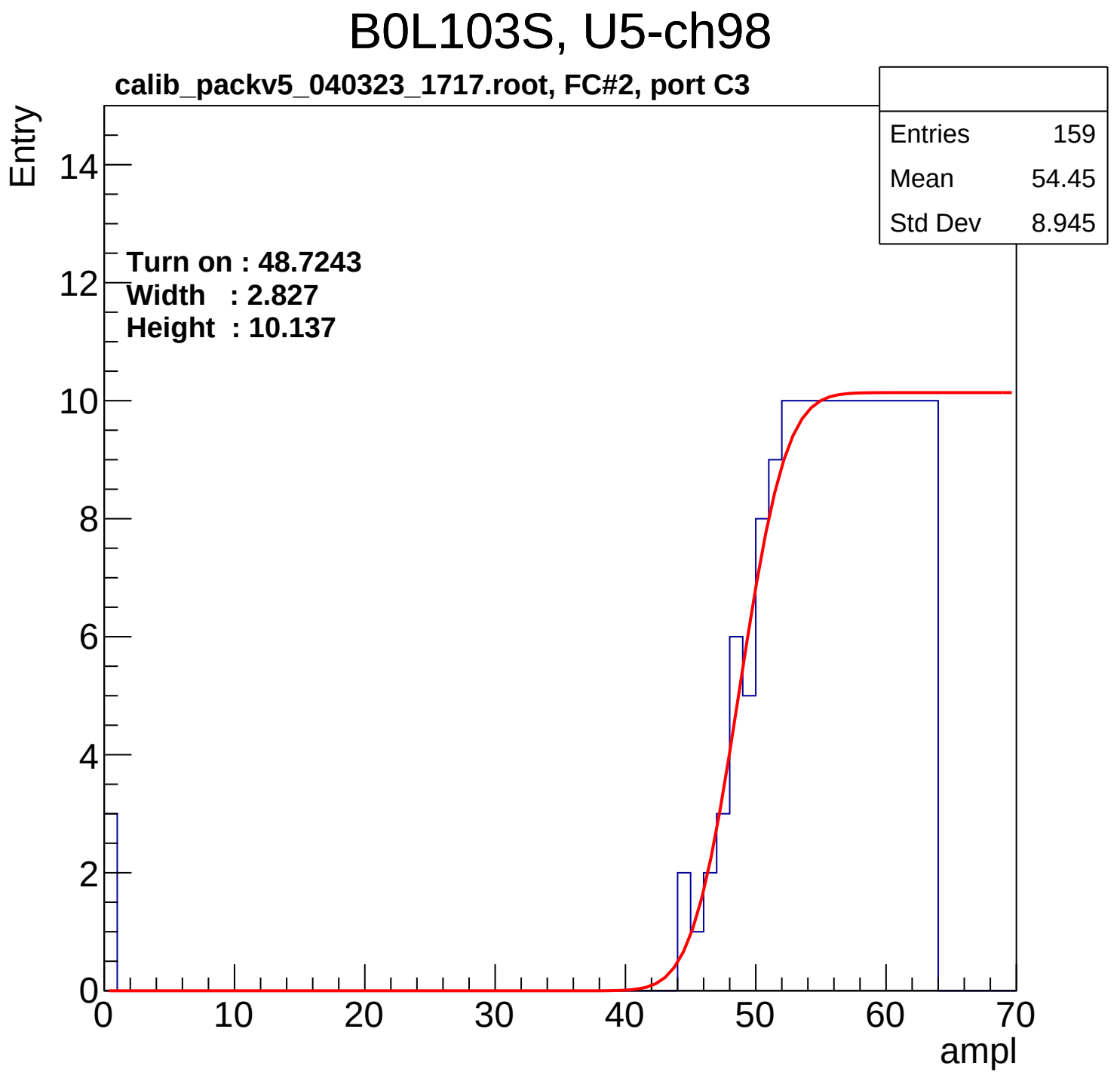
B0L103S, U5-ch98
calib_packv5_040323_1717.root, FC#2, port C3
Entries 159
Mean 54.45
Std Dev 8.945
Turn on : 48.7243
Width : 2.827
Height : 10.137
Entry
ampl
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8
10
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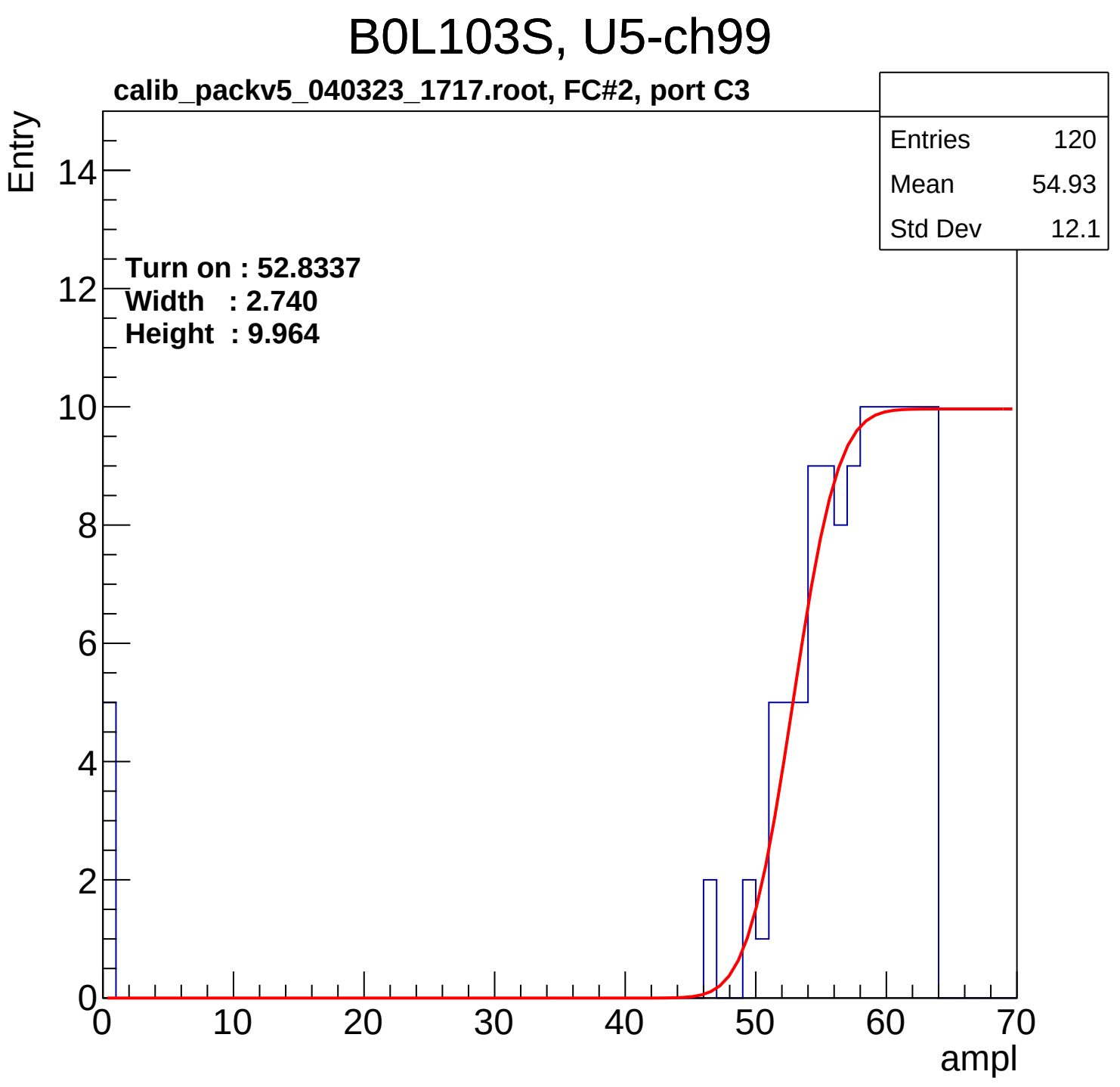
B0L103S, U5-ch99
calib_packv5_040323_1717.root, FC#2, port C3
Entries 120
Mean 54.93
Std Dev 12.1
Turn on : 52.8337
Width : 2.740
Height : 9.964
Entry
ampl
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6
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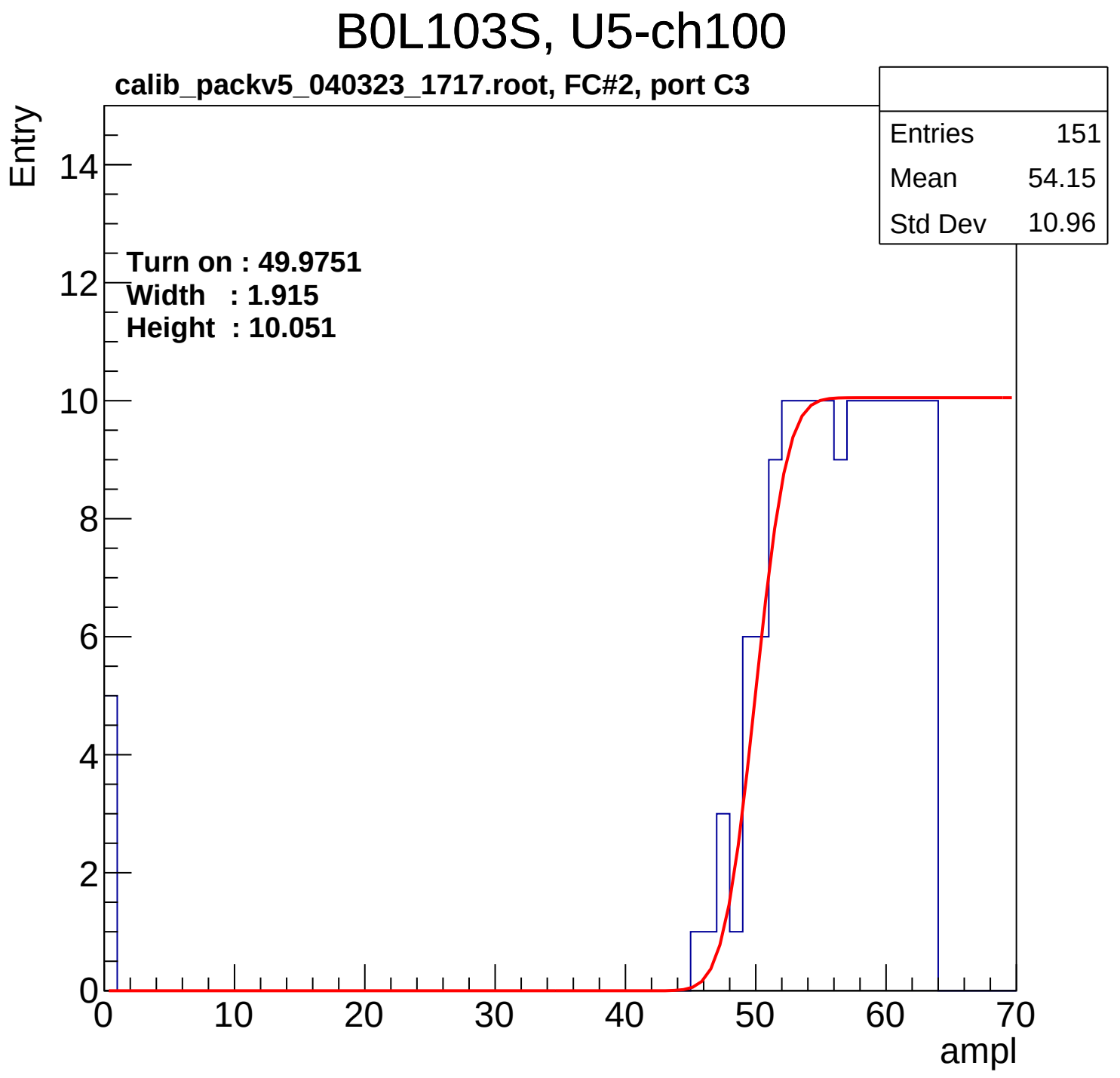
B0L103S, U5-ch100
calib_packv5_040323_1717.root, FC#2, port C3
Entries 151
Mean 54.15
Std Dev 10.96
Turn on : 49.9751
Width : 1.915
Height : 10.051
Entry
ampl
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8
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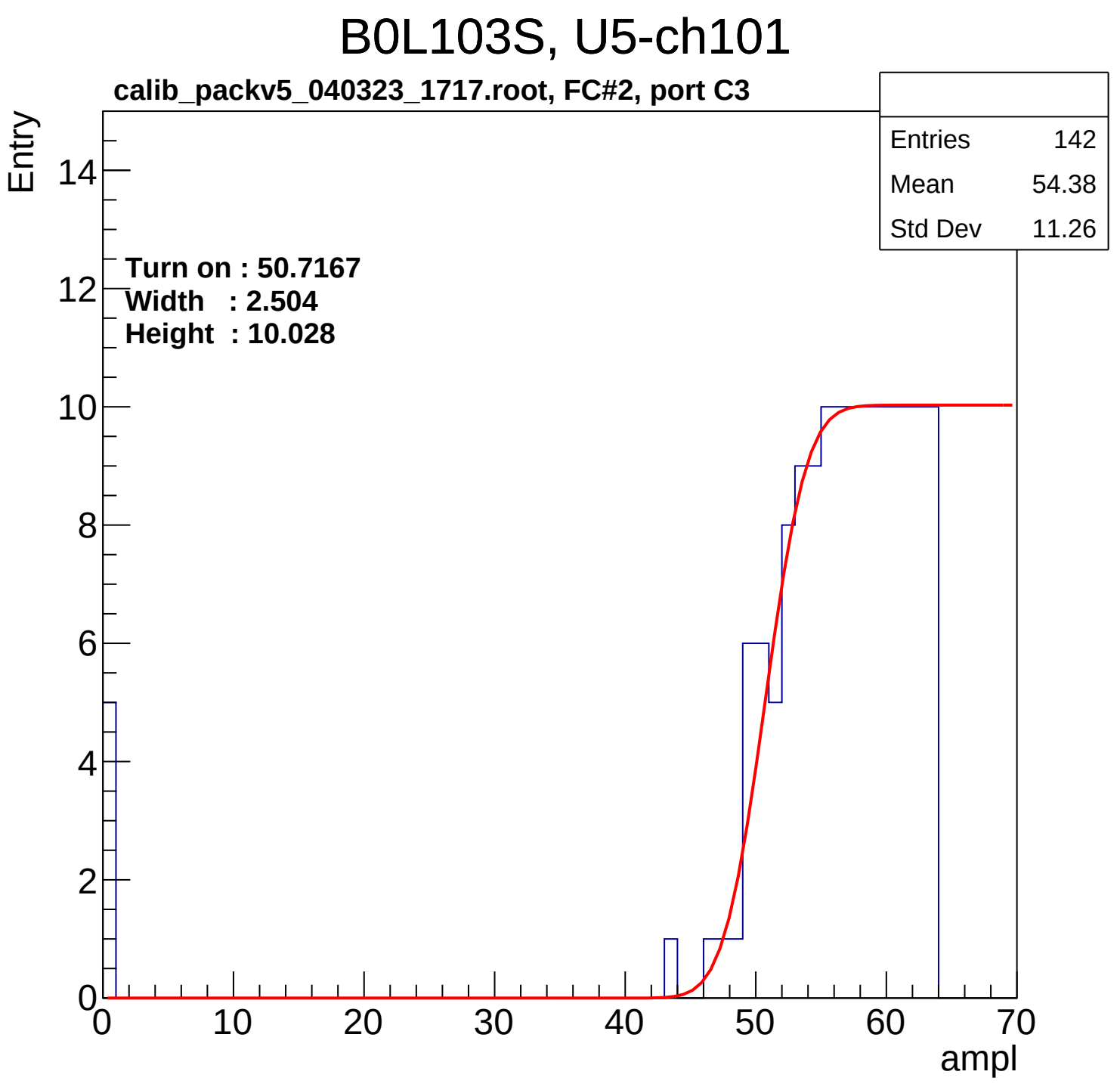
B0L103S, U5-ch101
calib_packv5_040323_1717.root, FC#2, port C3
Entries 142
Mean 54.38
Std Dev 11.26
Turn on : 50.7167
Width : 2.504
Height : 10.028
Entry
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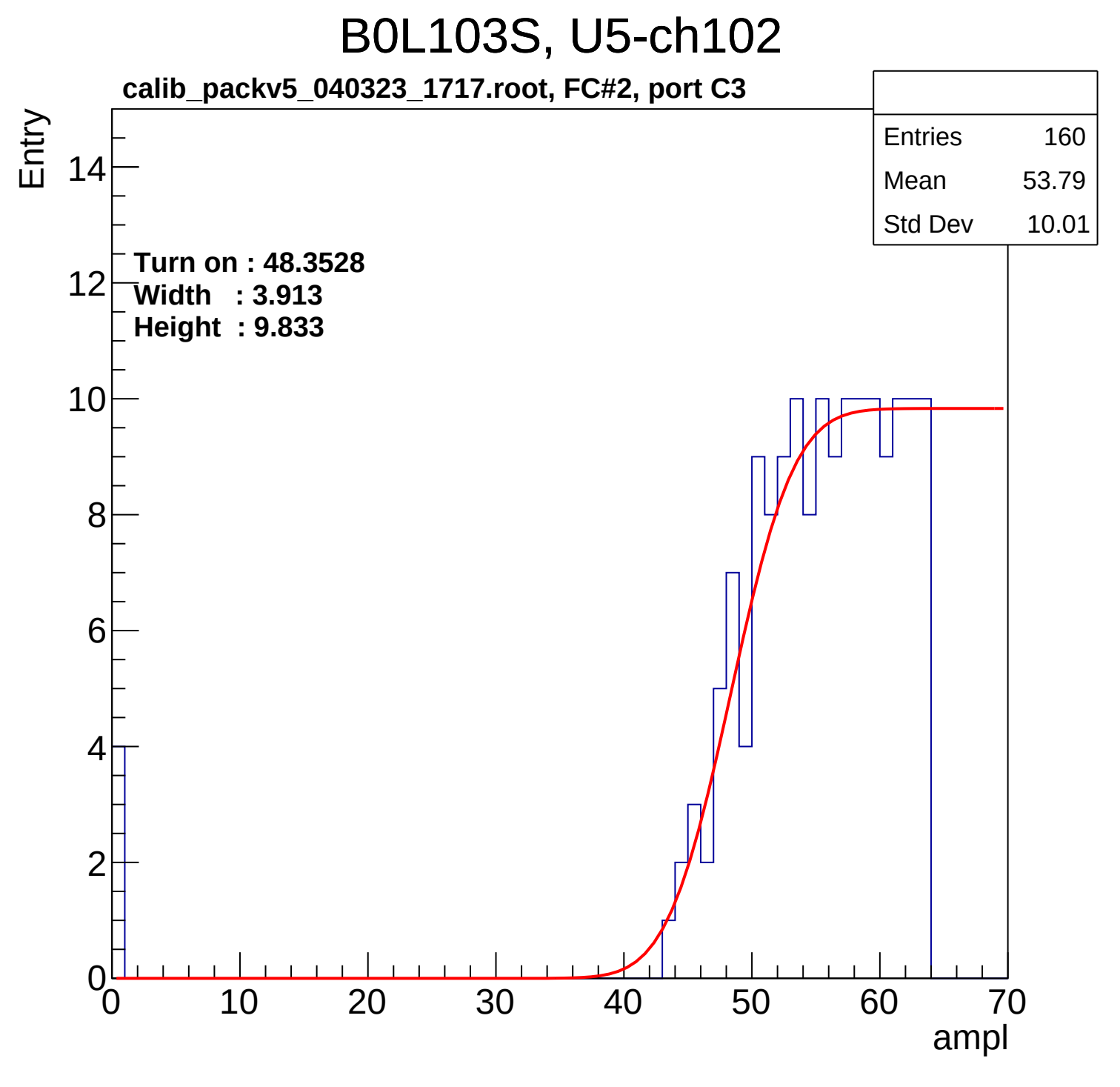
B0L103S, U5-ch102
calib_packv5_040323_1717.root, FC#2, port C3
Entries 160
Mean 53.79
Std Dev 10.01
Turn on : 48.3528
Width : 3.913
Height : 9.833
Entry
ampl
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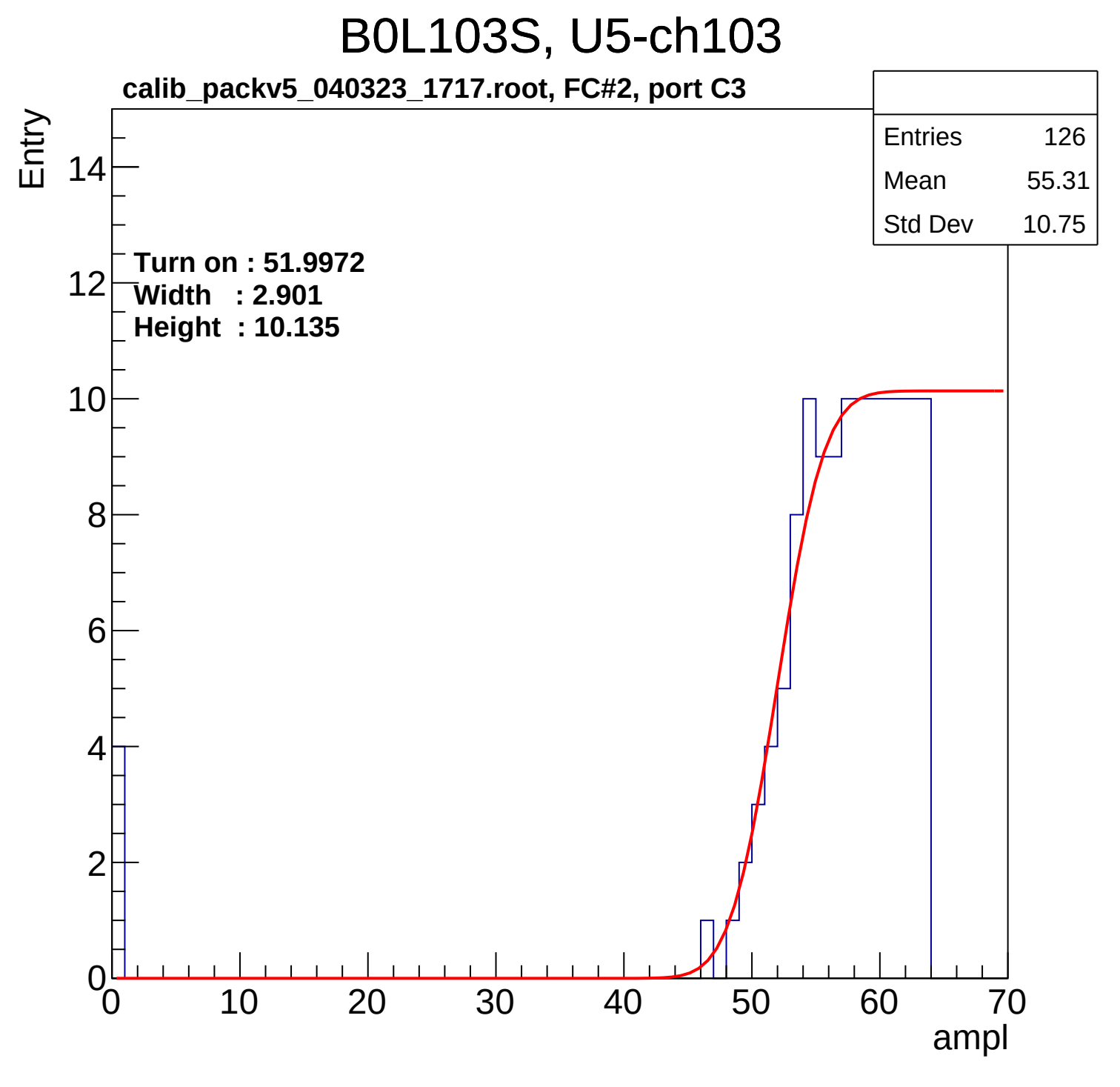
B0L103S, U5-ch103
calib_packv5_040323_1717.root, FC#2, port C3
Entries 126
Mean 55.31
Std Dev 10.75
Turn on : 51.9972
Width : 2.901
Height : 10.135
Entry
ampl
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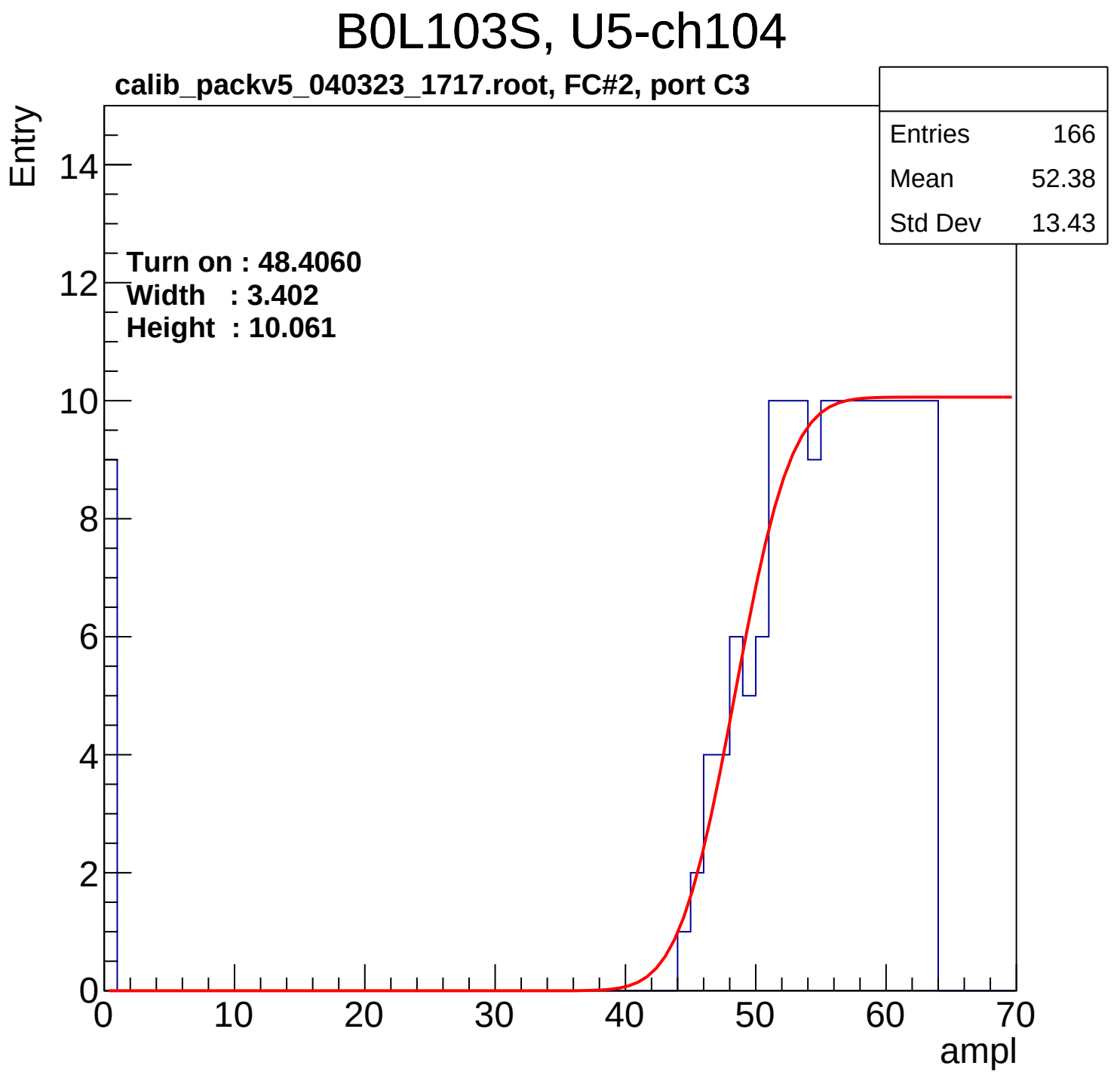
B0L103S, U5-ch104
calib_packv5_040323_1717.root, FC#2, port C3
Entries 166
Mean 52.38
Std Dev 13.43
Turn on : 48.4060
Width : 3.402
Height : 10.061
Entry
ampl
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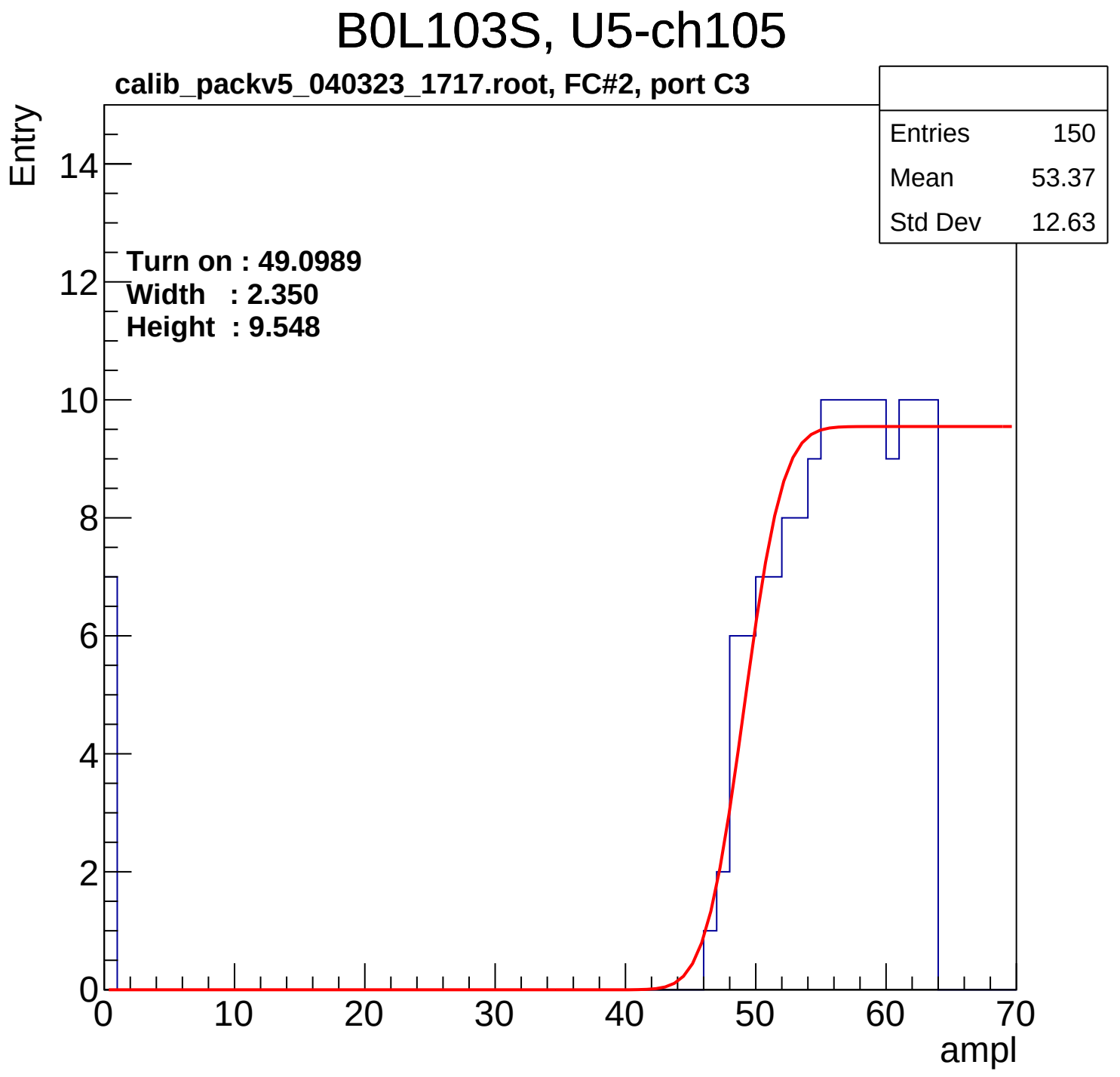
B0L103S, U5-ch105
calib_packv5_040323_1717.root, FC#2, port C3
Entries 150
Mean 53.37
Std Dev 12.63
Turn on : 49.0989
Width : 2.350
Height : 9.548
Entry
ampl
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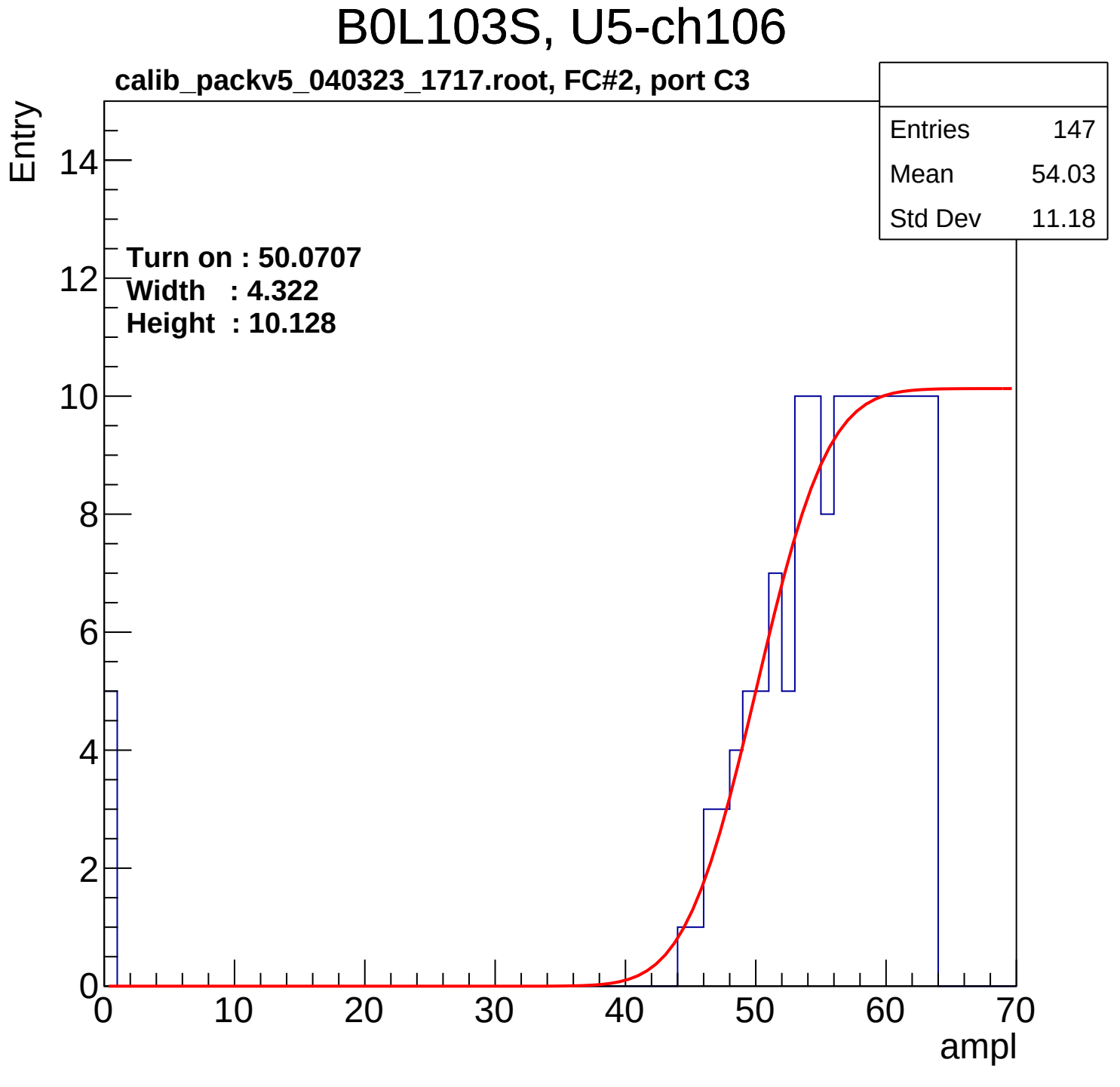
B0L103S, U5-ch106
calib_packv5_040323_1717.root, FC#2, port C3
Entries 147
Mean 54.03
Std Dev 11.18
Turn on : 50.0707
Width : 4.322
Height : 10.128
Entry
ampl
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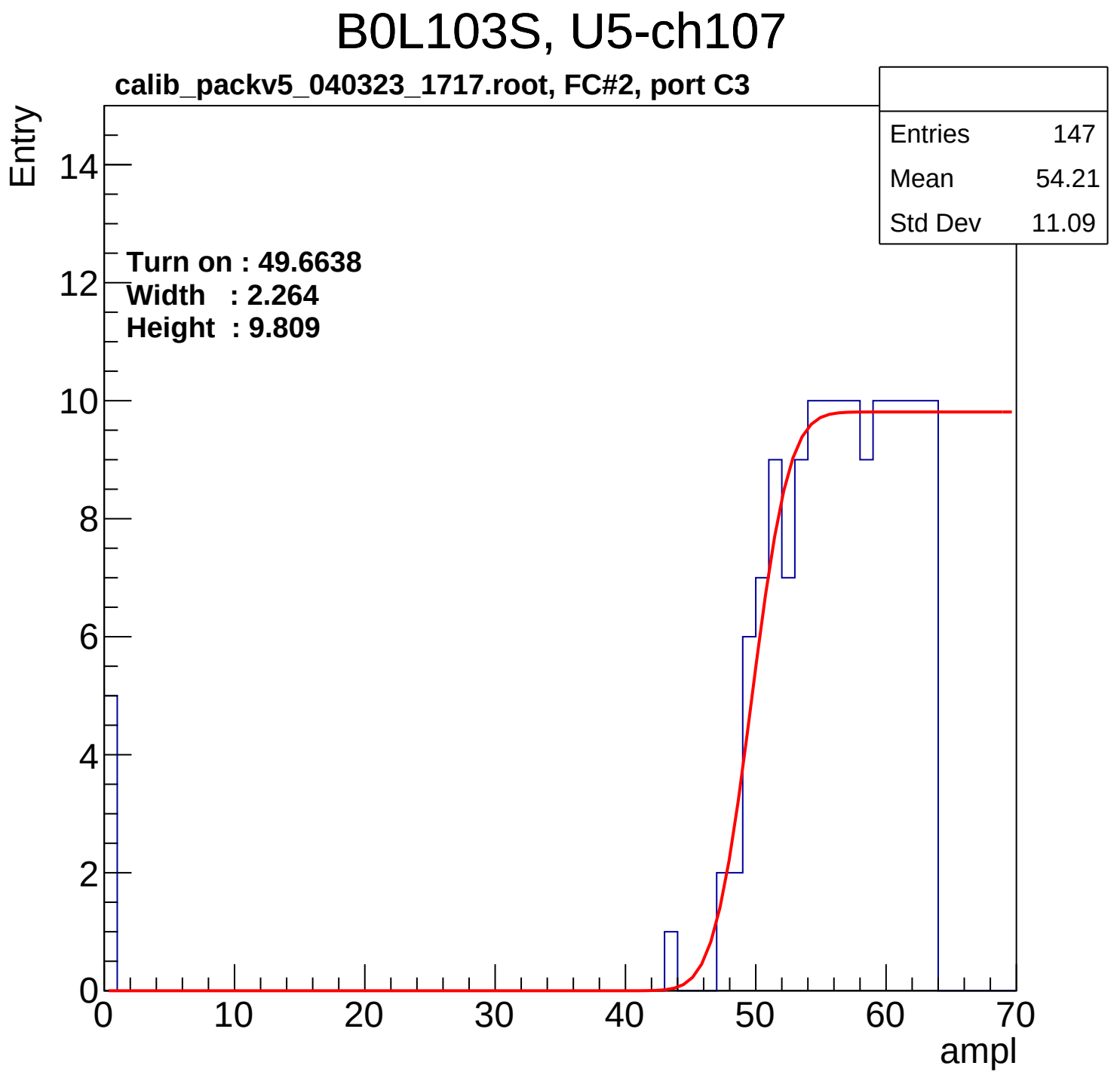
B0L103S, U5-ch107
calib_packv5_040323_1717.root, FC#2, port C3
Entries 147
Mean 54.21
Std Dev 11.09
Turn on : 49.6638
Width : 2.264
Height : 9.809
Entry
ampl
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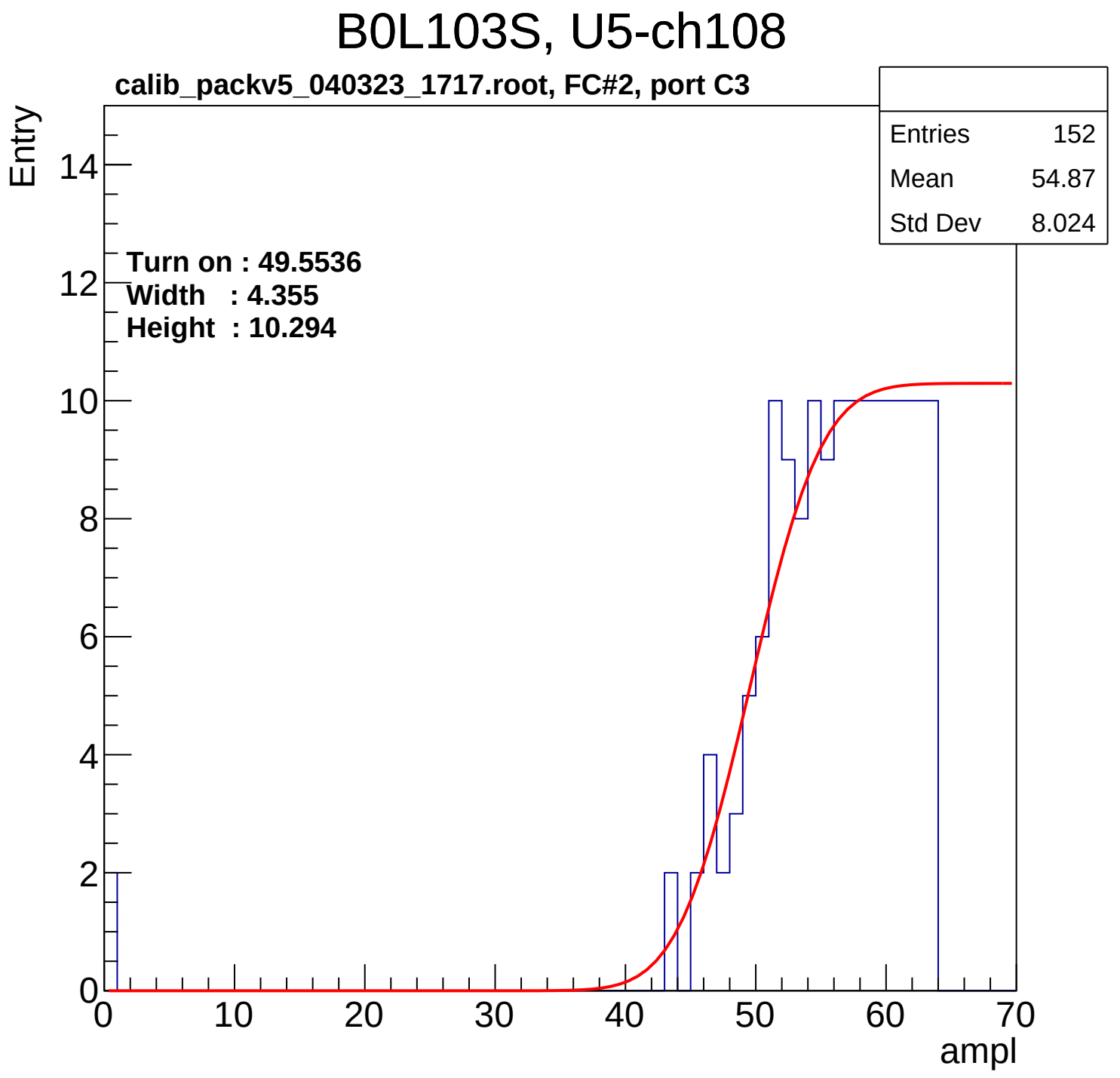
B0L103S, U5-ch108
calib_packv5_040323_1717.root, FC#2, port C3
Entries 152
Mean 54.87
Std Dev 8.024
Turn on : 49.5536
Width : 4.355
Height : 10.294
Entry
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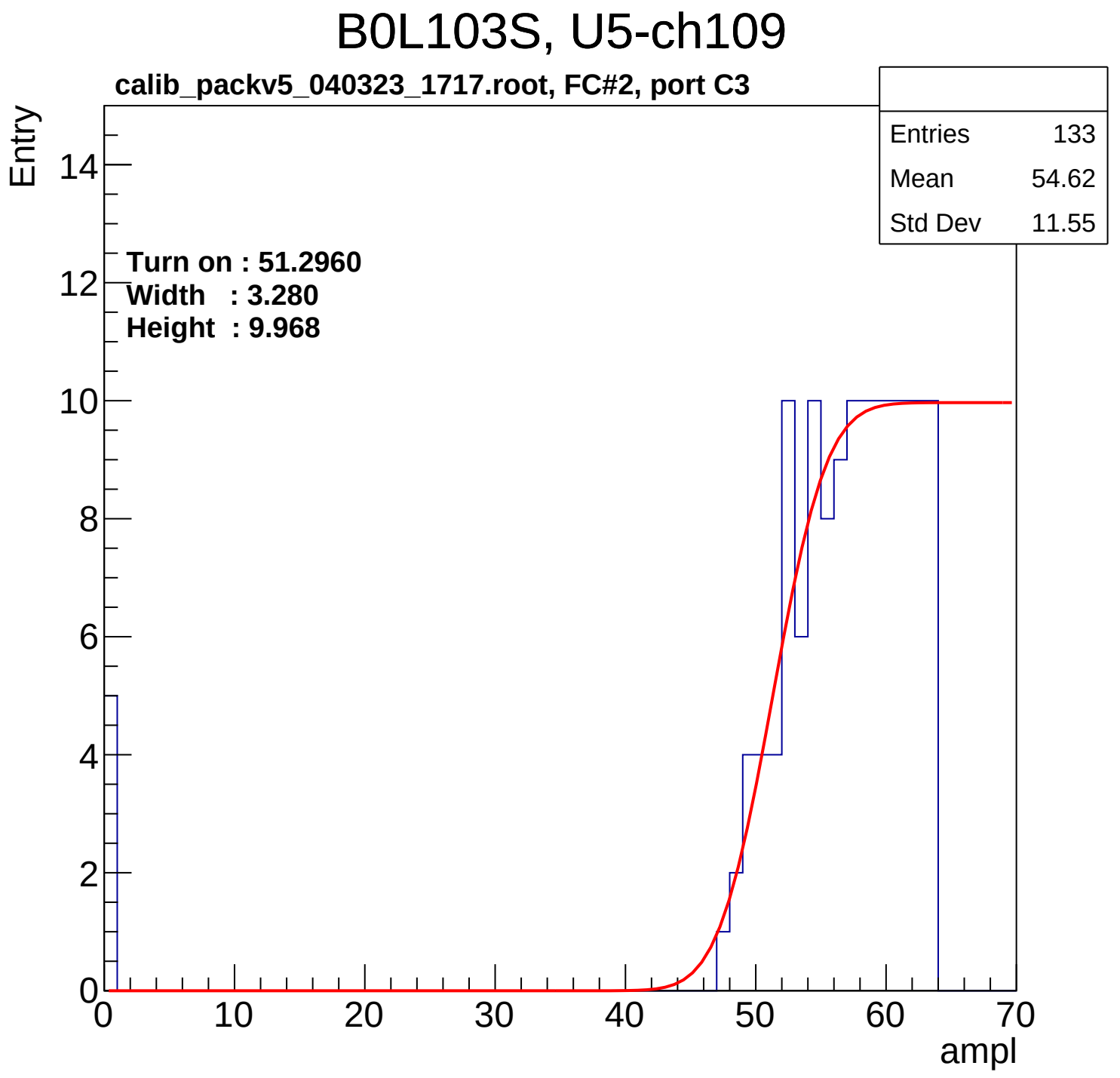
B0L103S, U5-ch109
calib_packv5_040323_1717.root, FC#2, port C3
Entries 133
Mean 54.62
Std Dev 11.55
Turn on : 51.2960
Width : 3.280
Height : 9.968
Entry
ampl
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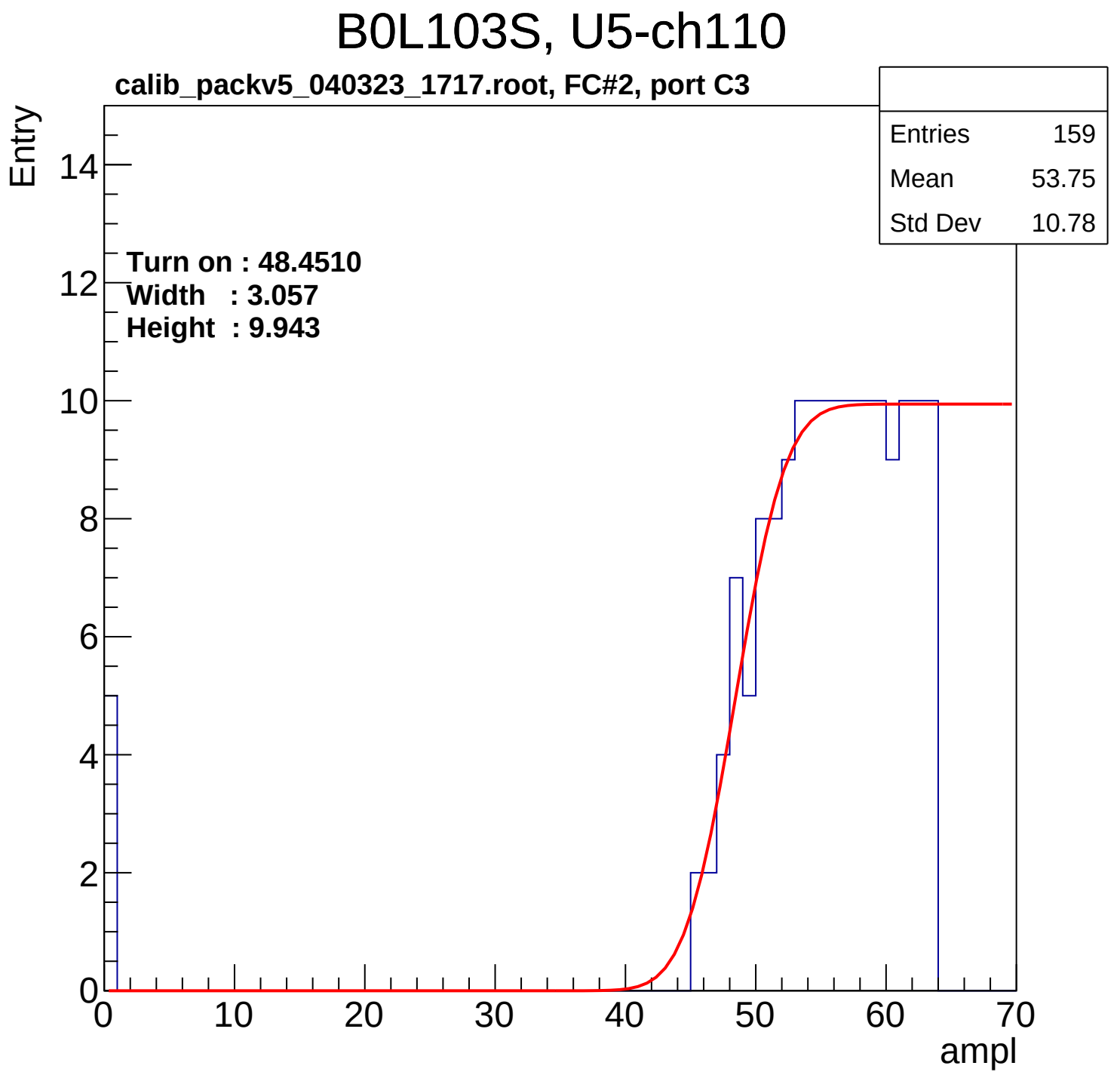
B0L103S, U5-ch110
calib_packv5_040323_1717.root, FC#2, port C3
Entries 159
Mean 53.75
Std Dev 10.78
Turn on : 48.4510
Width : 3.057
Height : 9.943
Entry
ampl
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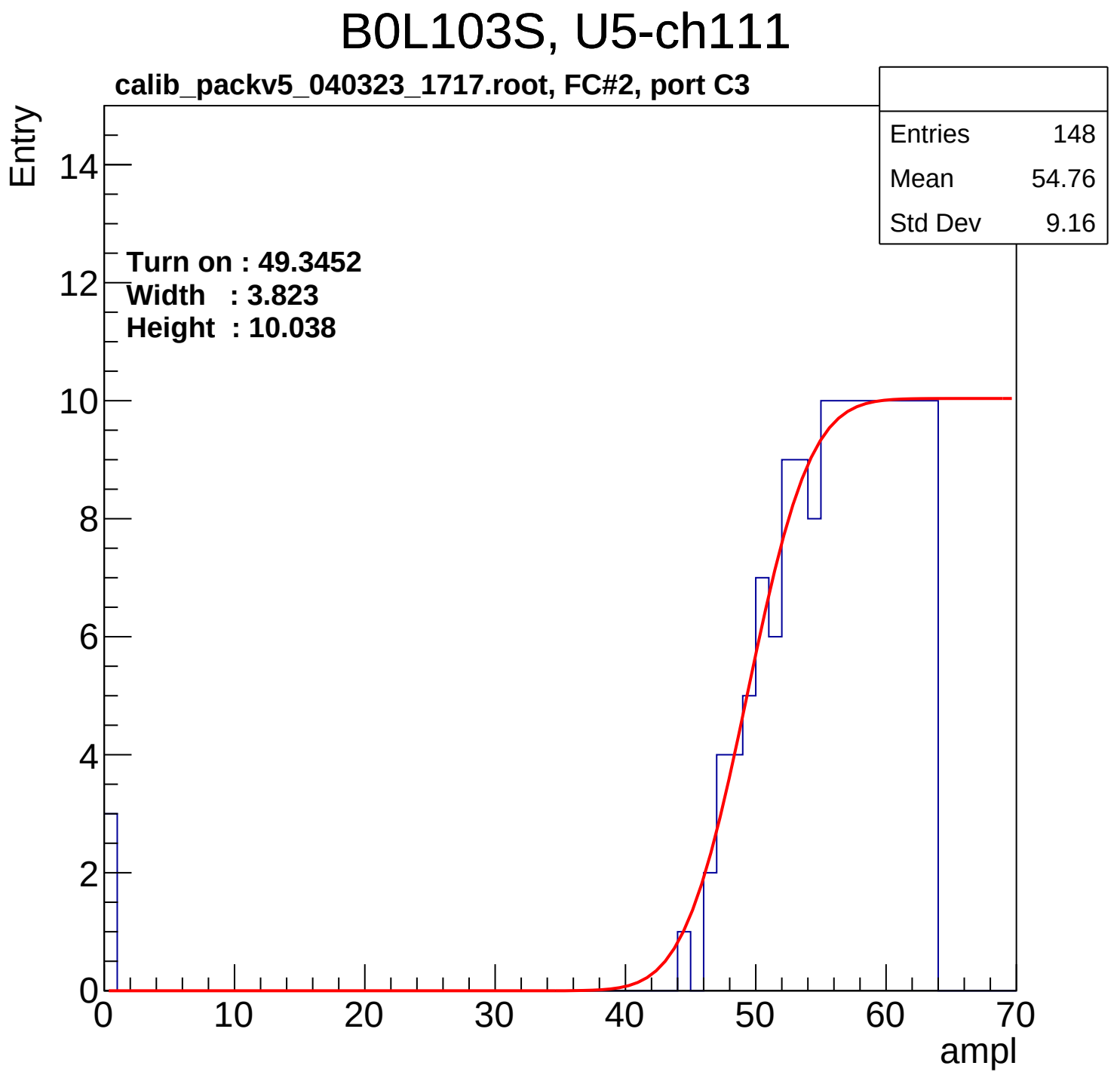
B0L103S, U5-ch111
calib_packv5_040323_1717.root, FC#2, port C3
Entries 148
Mean 54.76
Std Dev 9.16
Turn on : 49.3452
Width : 3.823
Height : 10.038
Entry
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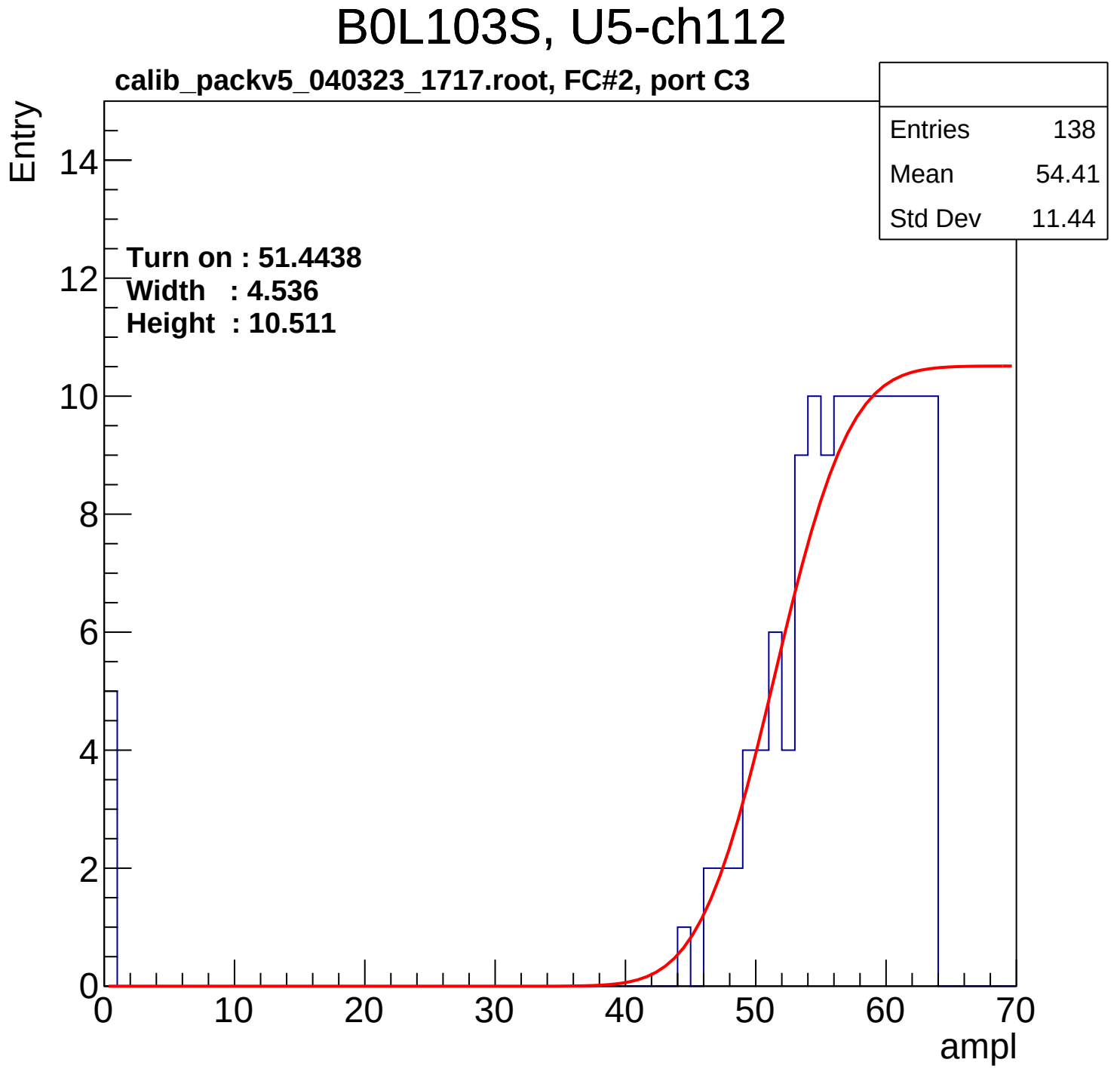
B0L103S, U5-ch112
calib_packv5_040323_1717.root, FC#2, port C3
Entries 138
Mean 54.41
Std Dev 11.44
Turn on : 51.4438
Width : 4.536
Height : 10.511
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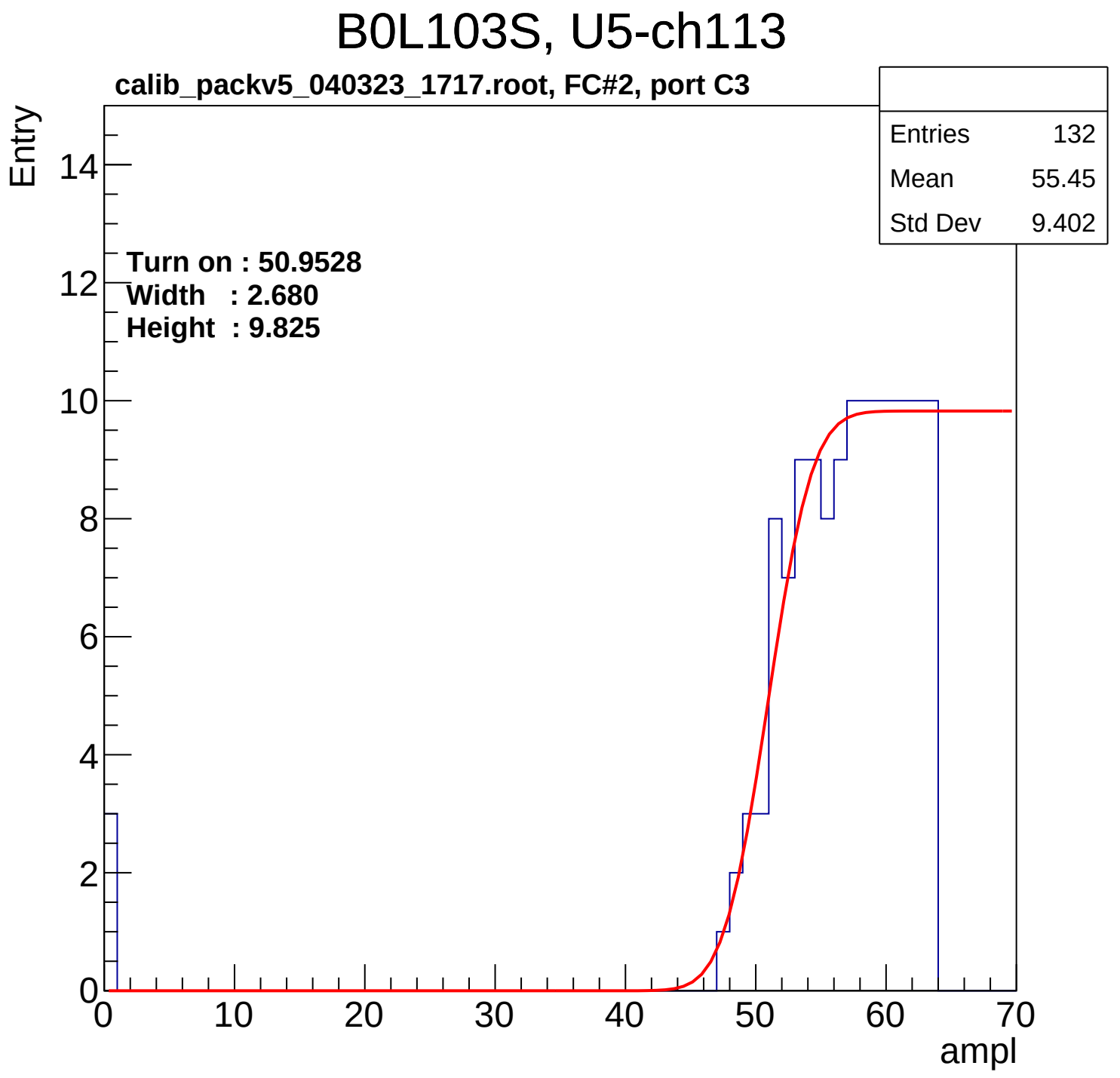
B0L103S, U5-ch113
calib_packv5_040323_1717.root, FC#2, port C3
Entries 132
Mean 55.45
Std Dev 9.402
Turn on : 50.9528
Width : 2.680
Height : 9.825
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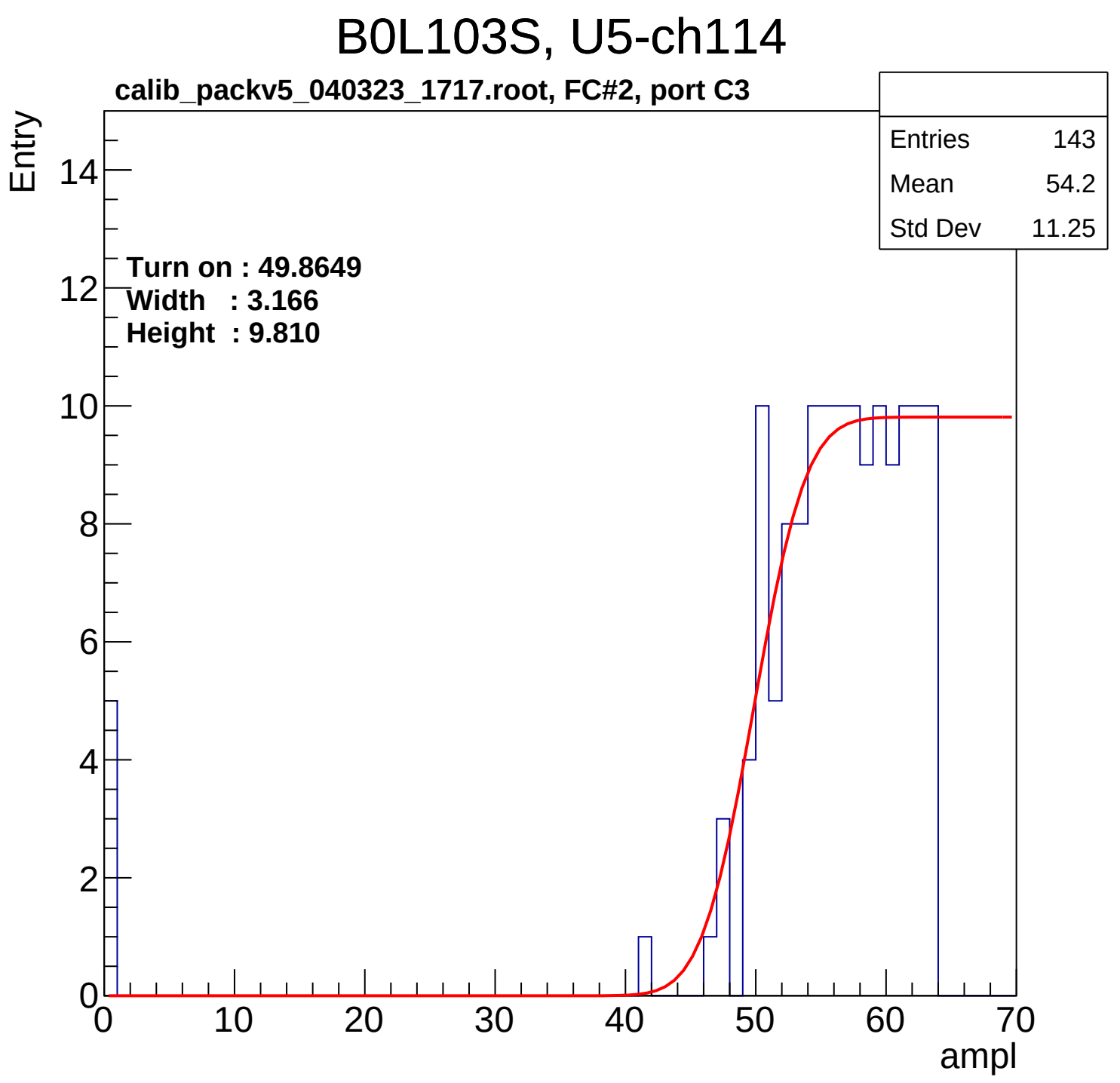
B0L103S, U5-ch114
calib_packv5_040323_1717.root, FC#2, port C3
Entries 143
Mean 54.2
Std Dev 11.25
Turn on : 49.8649
Width : 3.166
Height : 9.810
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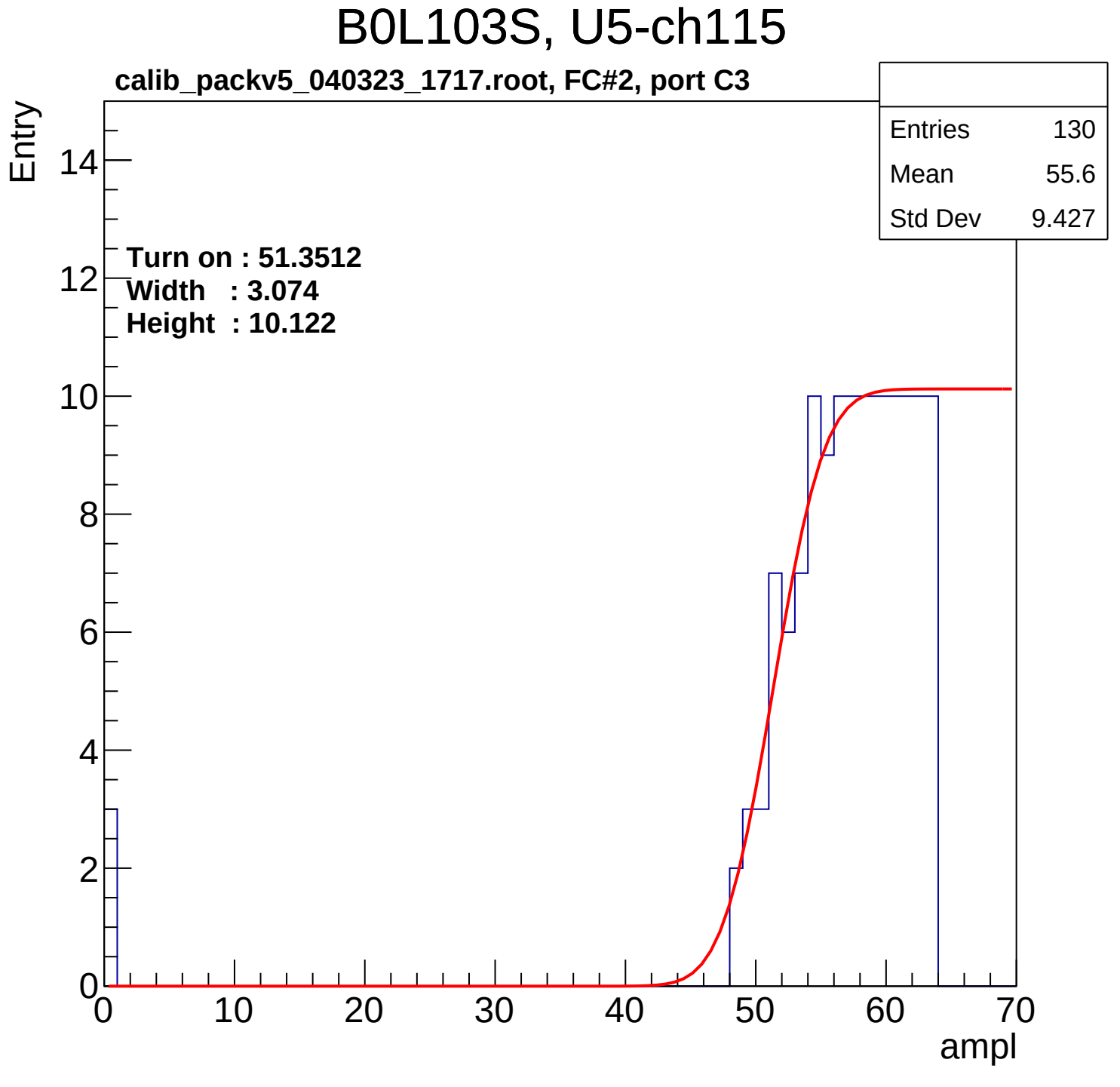
B0L103S, U5-ch115
calib_packv5_040323_1717.root, FC#2, port C3
Entries 130
Mean 55.6
Std Dev 9.427
Turn on : 51.3512
Width : 3.074
Height : 10.122
Entry
ampl
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4
6
8
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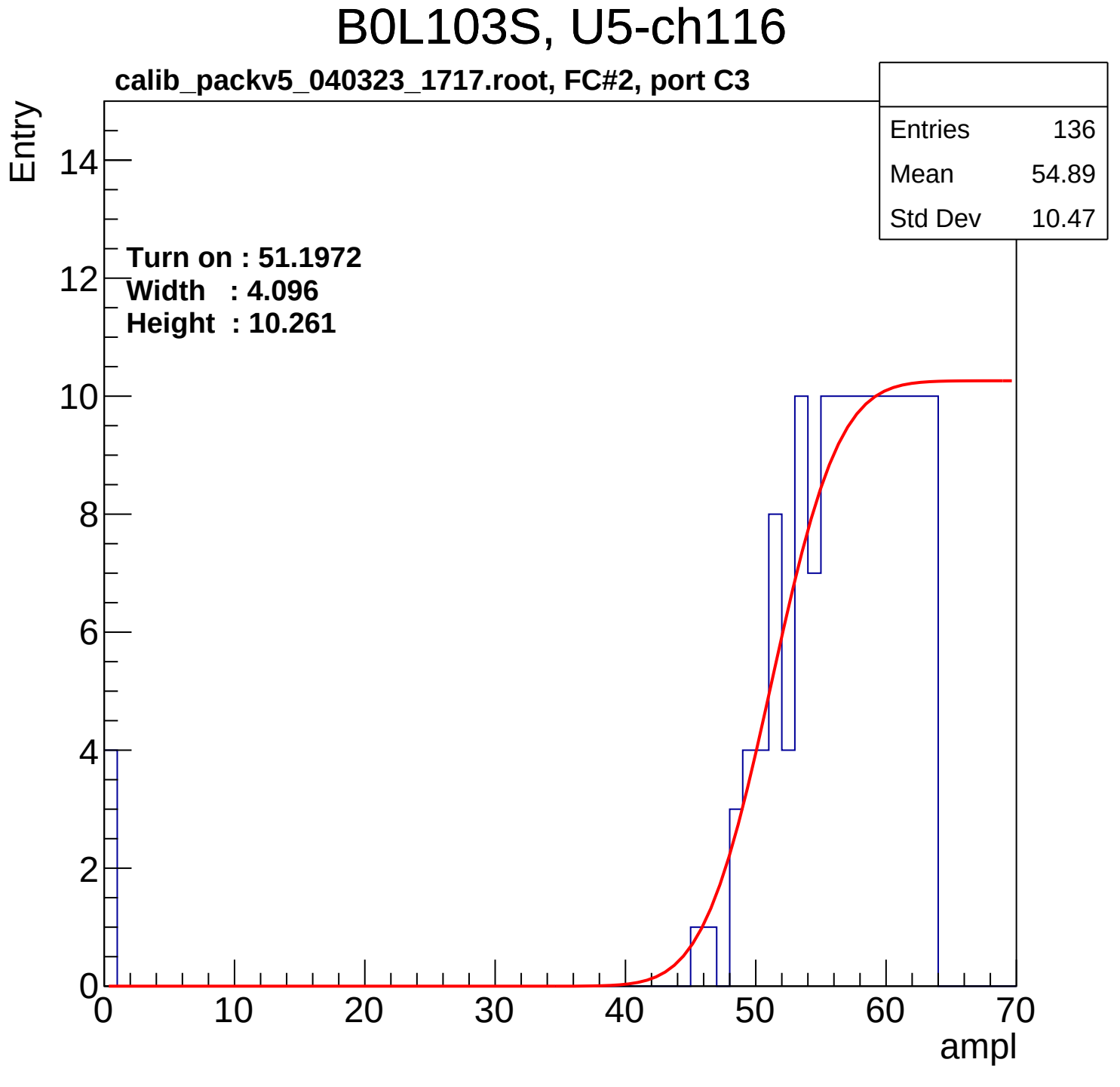
B0L103S, U5-ch116
calib_packv5_040323_1717.root, FC#2, port C3
Entries 136
Mean 54.89
Std Dev 10.47
Turn on : 51.1972
Width : 4.096
Height : 10.261
Entry
ampl
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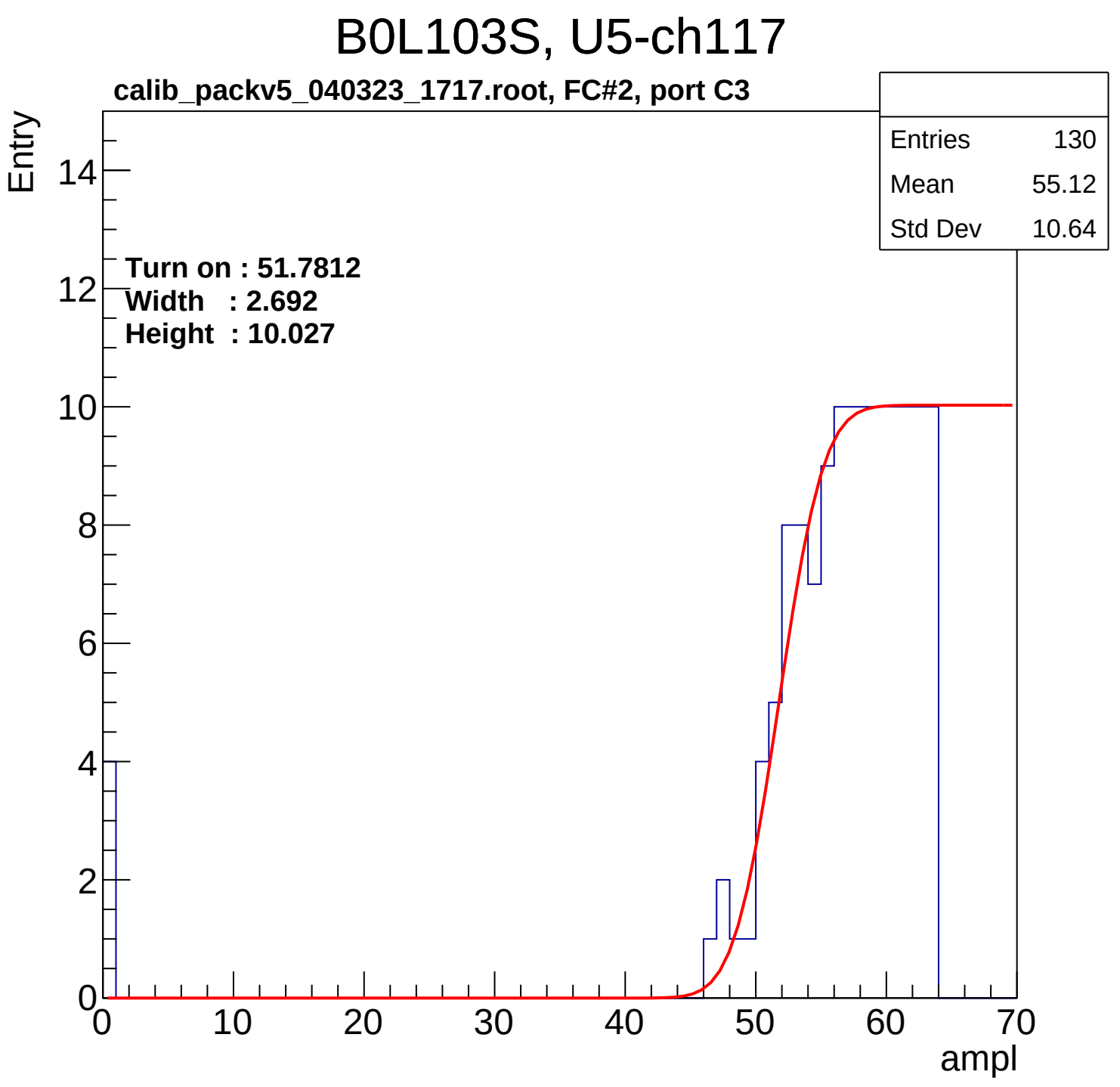
B0L103S, U5-ch117
calib_packv5_040323_1717.root, FC#2, port C3
Entries 130
Mean 55.12
Std Dev 10.64
Turn on : 51.7812
Width : 2.692
Height : 10.027
Entry
ampl
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2
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6
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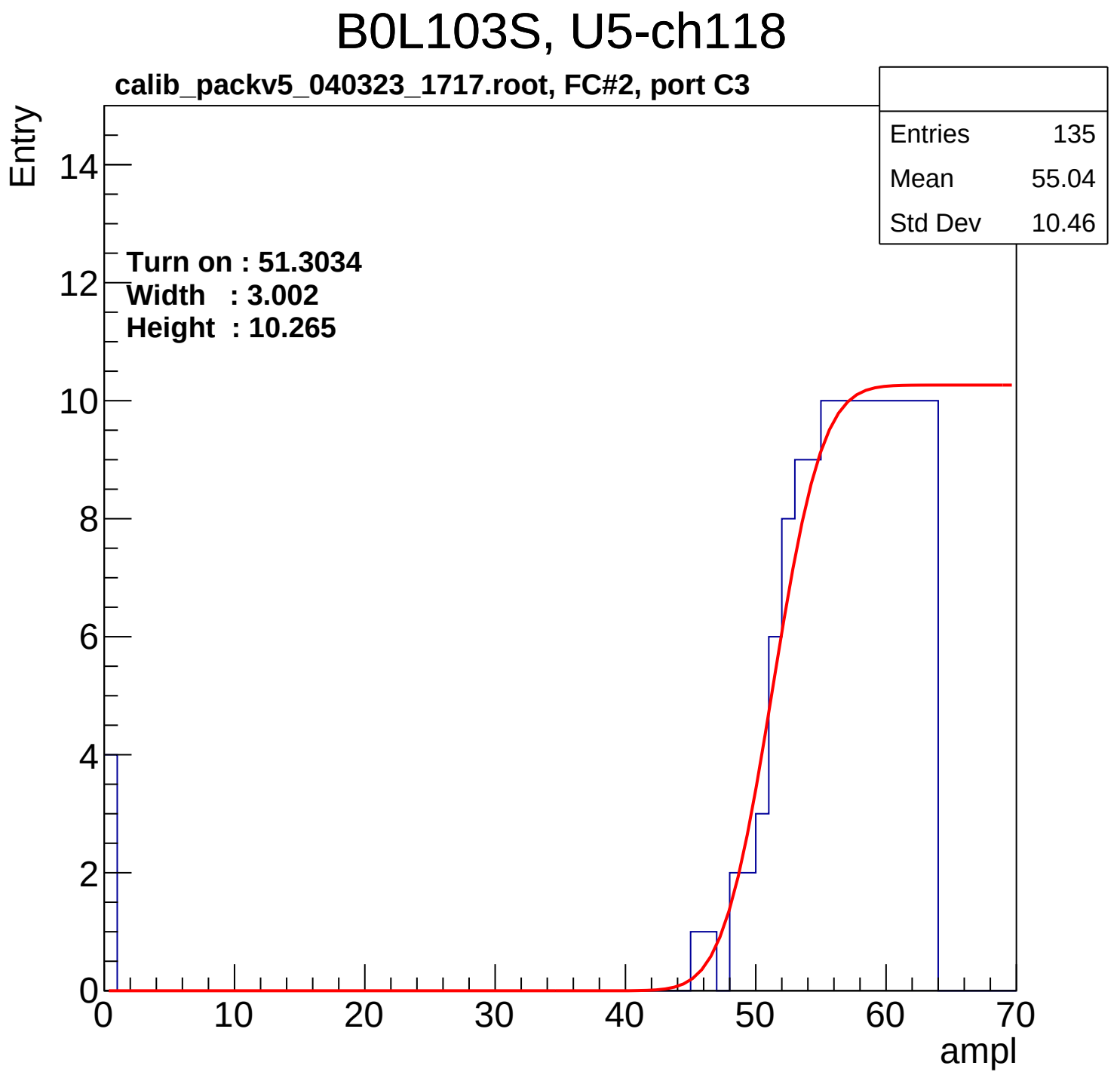
B0L103S, U5-ch118
calib_packv5_040323_1717.root, FC#2, port C3
Entries 135
Mean 55.04
Std Dev 10.46
Turn on : 51.3034
Width : 3.002
Height : 10.265
Entry
ampl
0
2
4
6
8
10
12
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20
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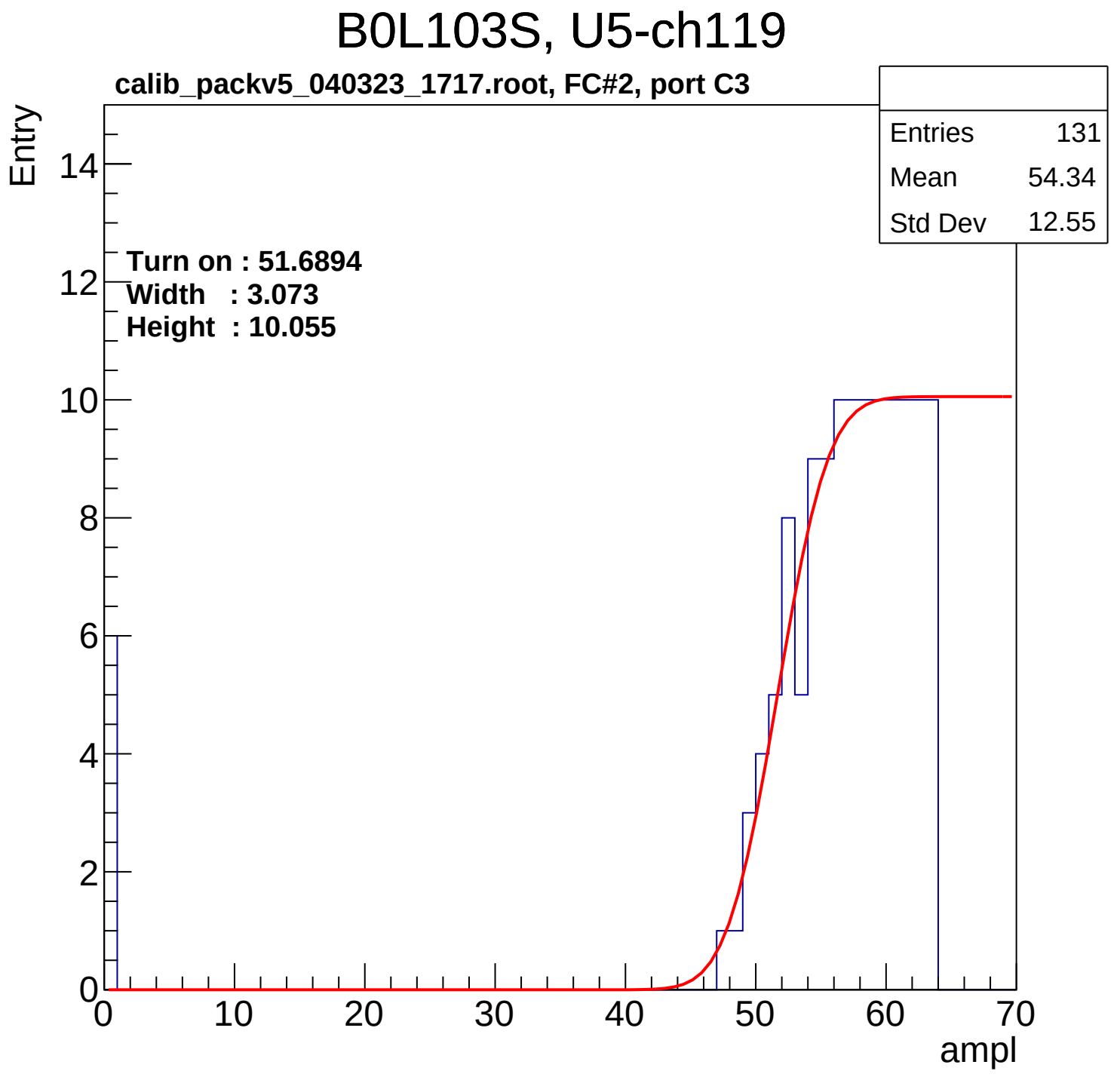
B0L103S, U5-ch119
calib_packv5_040323_1717.root, FC#2, port C3
Entries 131
Mean 54.34
Std Dev 12.55
Turn on : 51.6894
Width : 3.073
Height : 10.055
Entry
ampl
0
2
4
6
8
10
12
14
0
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20
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40
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60
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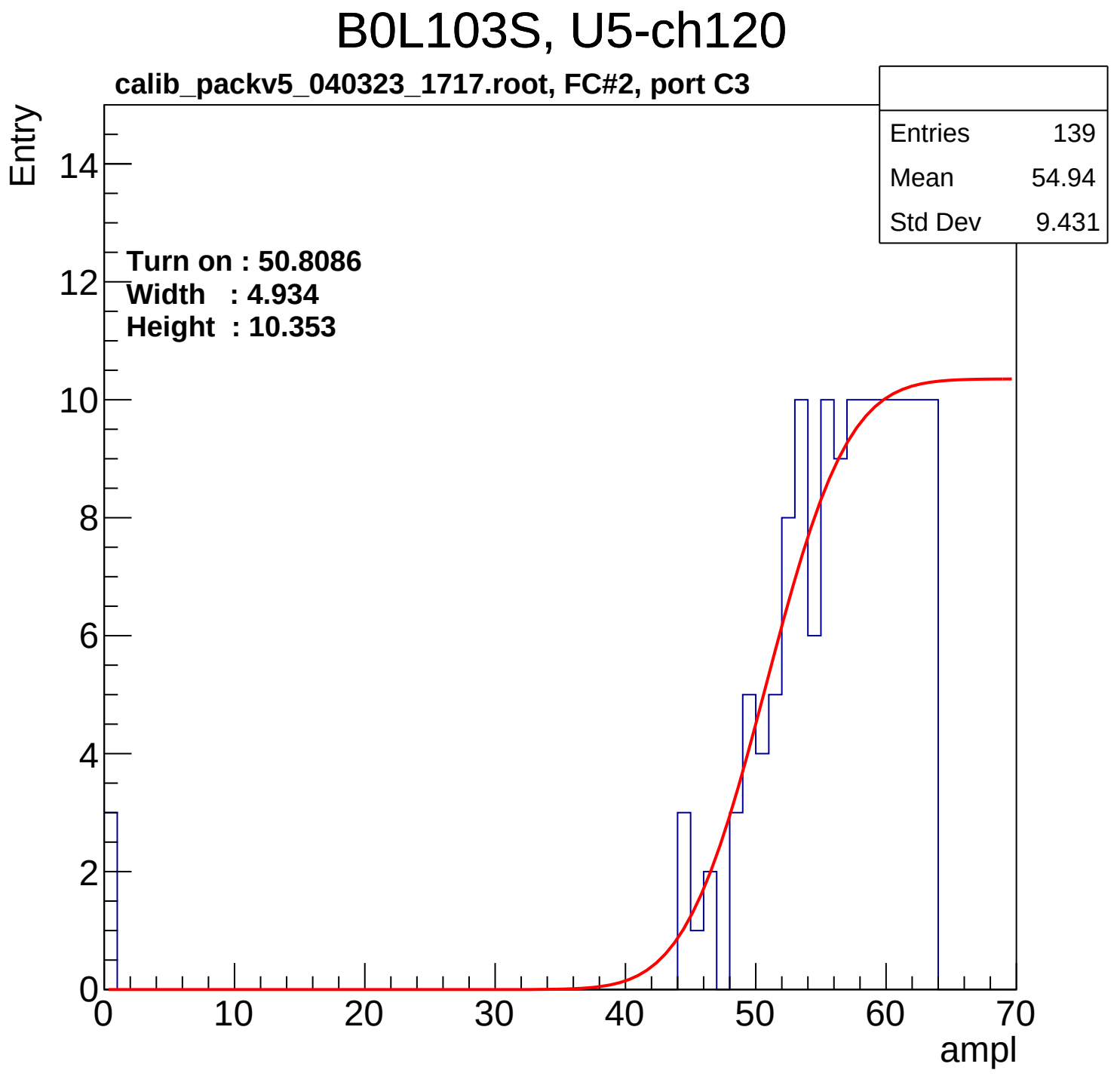
B0L103S, U5-ch120
calib_packv5_040323_1717.root, FC#2, port C3
Entries 139
Mean 54.94
Std Dev 9.431
Turn on : 50.8086
Width : 4.934
Height : 10.353
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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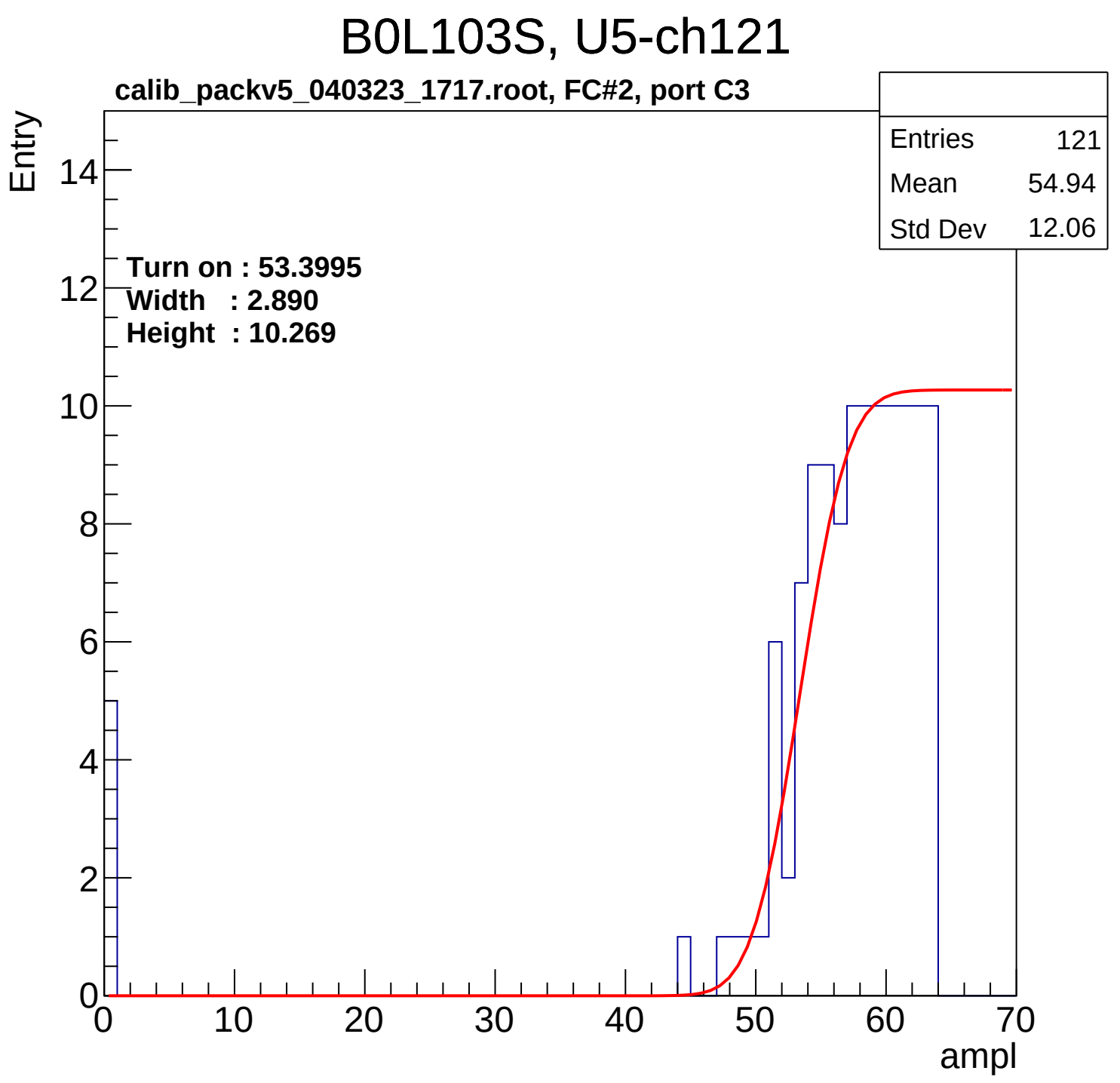
B0L103S, U5-ch121
calib_packv5_040323_1717.root, FC#2, port C3
Entries 121
Mean 54.94
Std Dev 12.06
Turn on : 53.3995
Width : 2.890
Height : 10.269
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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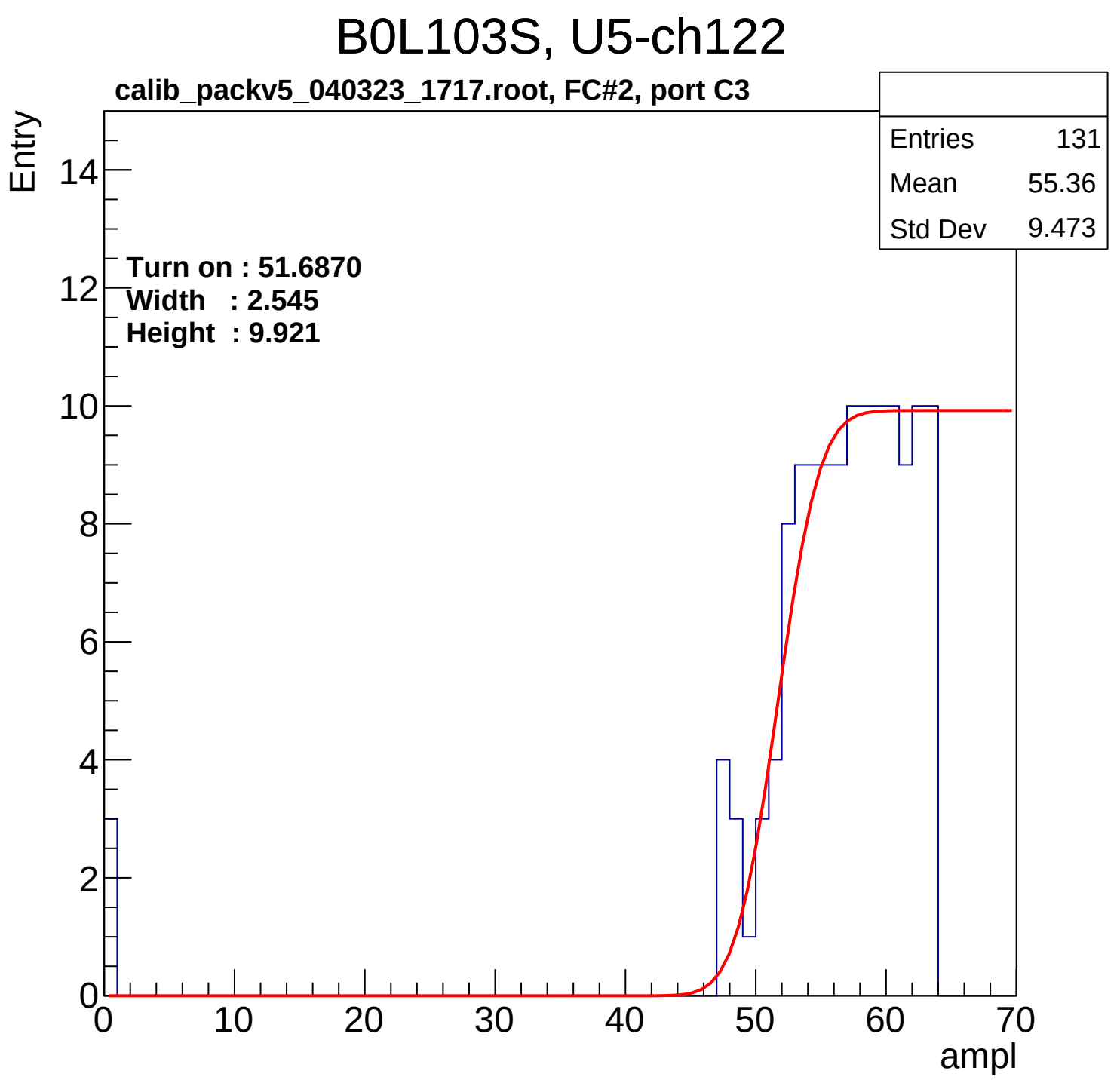
B0L103S, U5-ch122
calib_packv5_040323_1717.root, FC#2, port C3
Entries 131
Mean 55.36
Std Dev 9.473
Turn on : 51.6870
Width : 2.545
Height : 9.921
Entry
ampl
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4
6
8
10
12
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10
20
30
40
50
60
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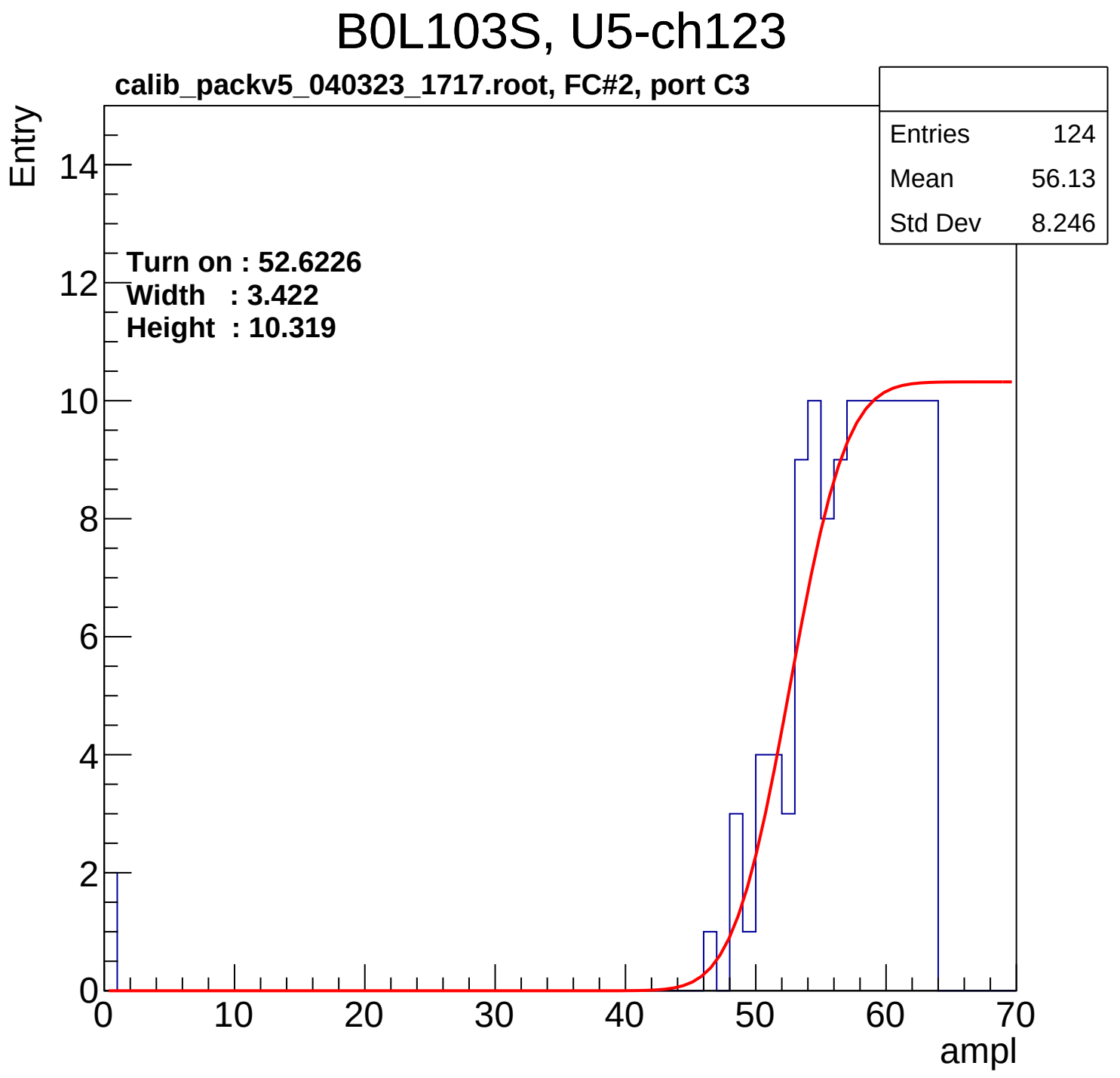
B0L103S, U5-ch123
calib_packv5_040323_1717.root, FC#2, port C3
Entries 124
Mean 56.13
Std Dev 8.246
Turn on : 52.6226
Width : 3.422
Height : 10.319
Entry
ampl
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2
4
6
8
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12
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0
10
20
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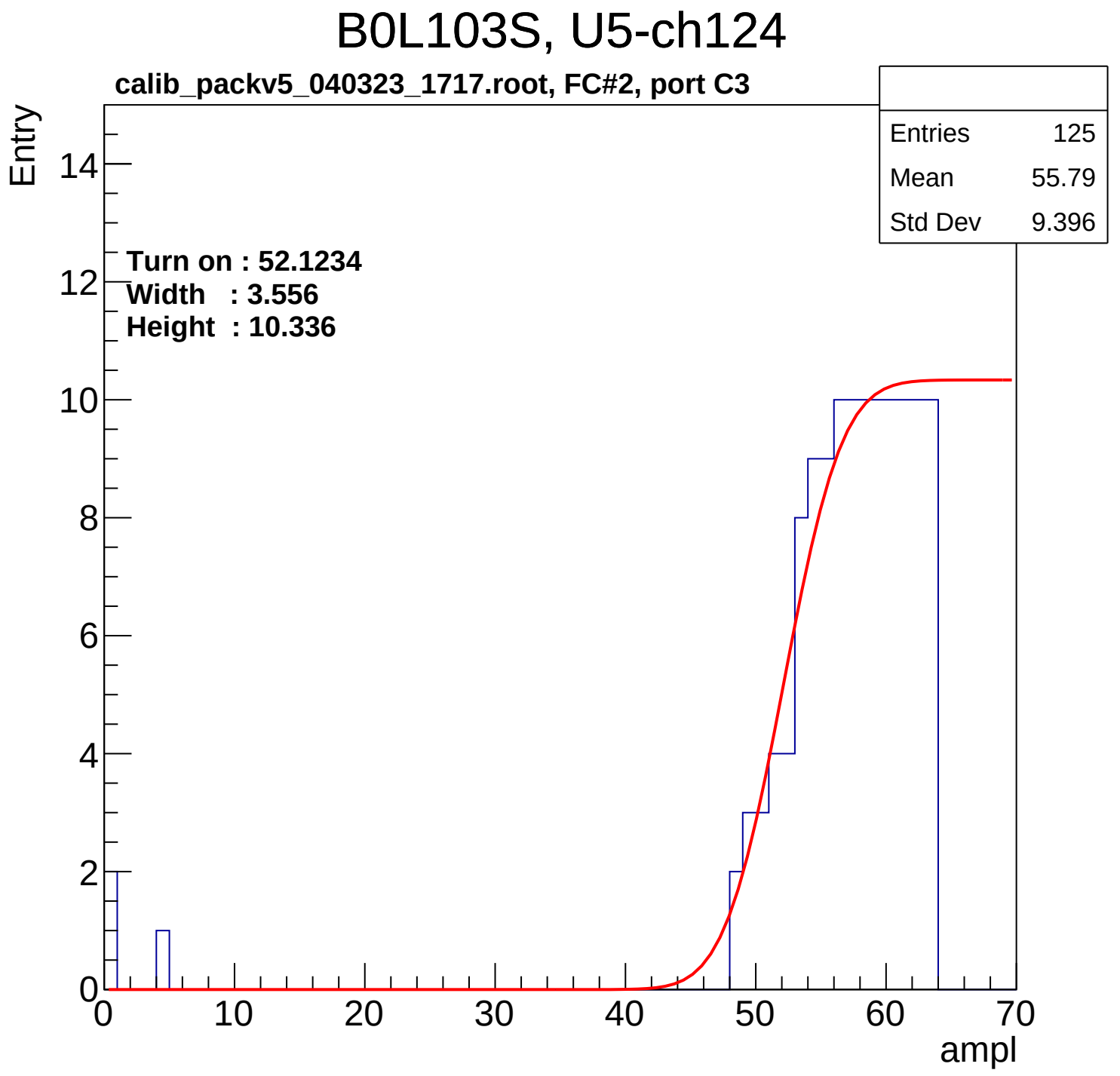
B0L103S, U5-ch124
calib_packv5_040323_1717.root, FC#2, port C3
Entries 125
Mean 55.79
Std Dev 9.396
Turn on : 52.1234
Width : 3.556
Height : 10.336
Entry
ampl
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2
4
6
8
10
12
14
0
10
20
30
40
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60
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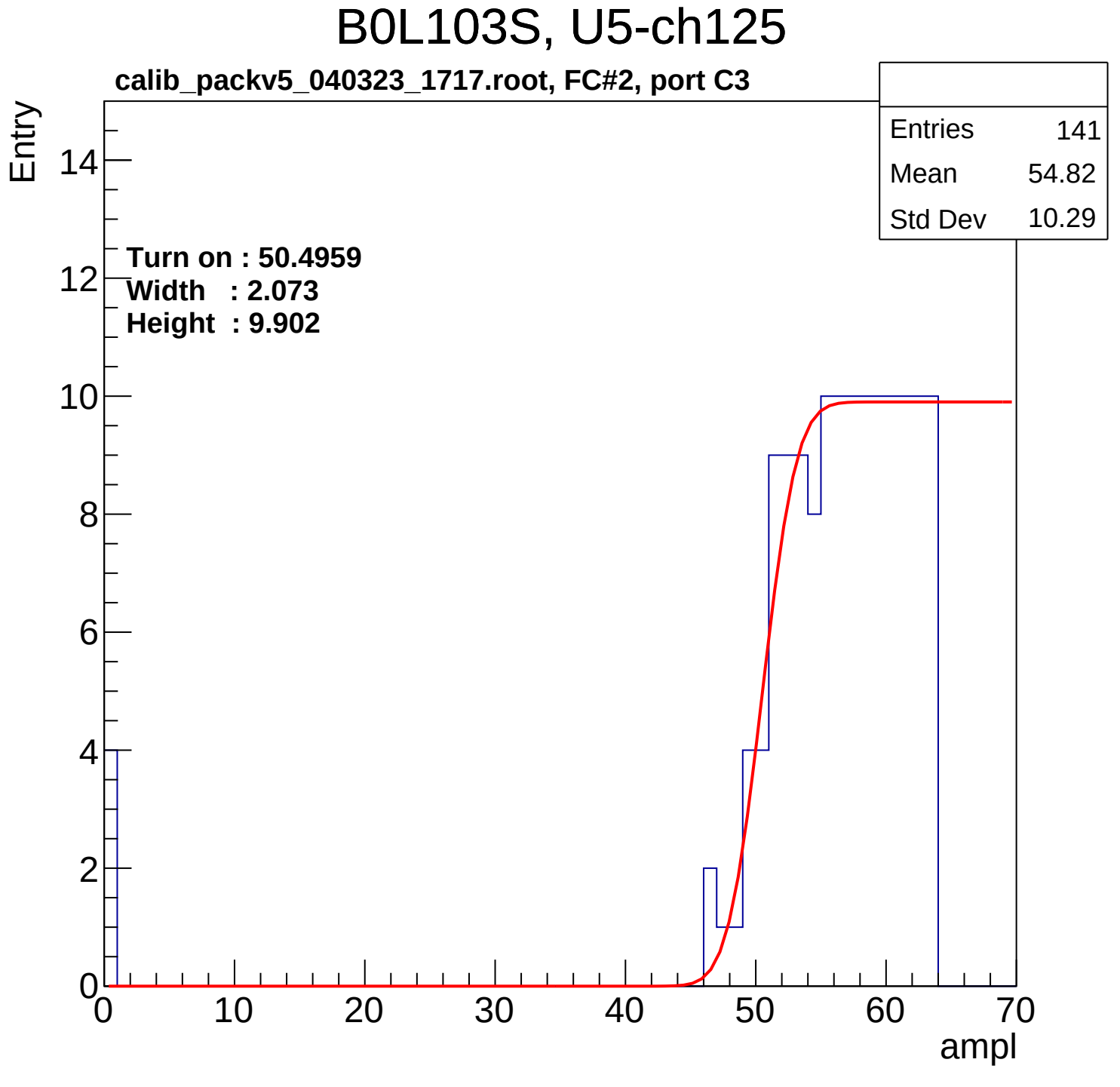
B0L103S, U5-ch125
calib_packv5_040323_1717.root, FC#2, port C3
Entries 141
Mean 54.82
Std Dev 10.29
Turn on : 50.4959
Width : 2.073
Height : 9.902
Entry
ampl
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4
6
8
10
12
14
0
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20
30
40
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60
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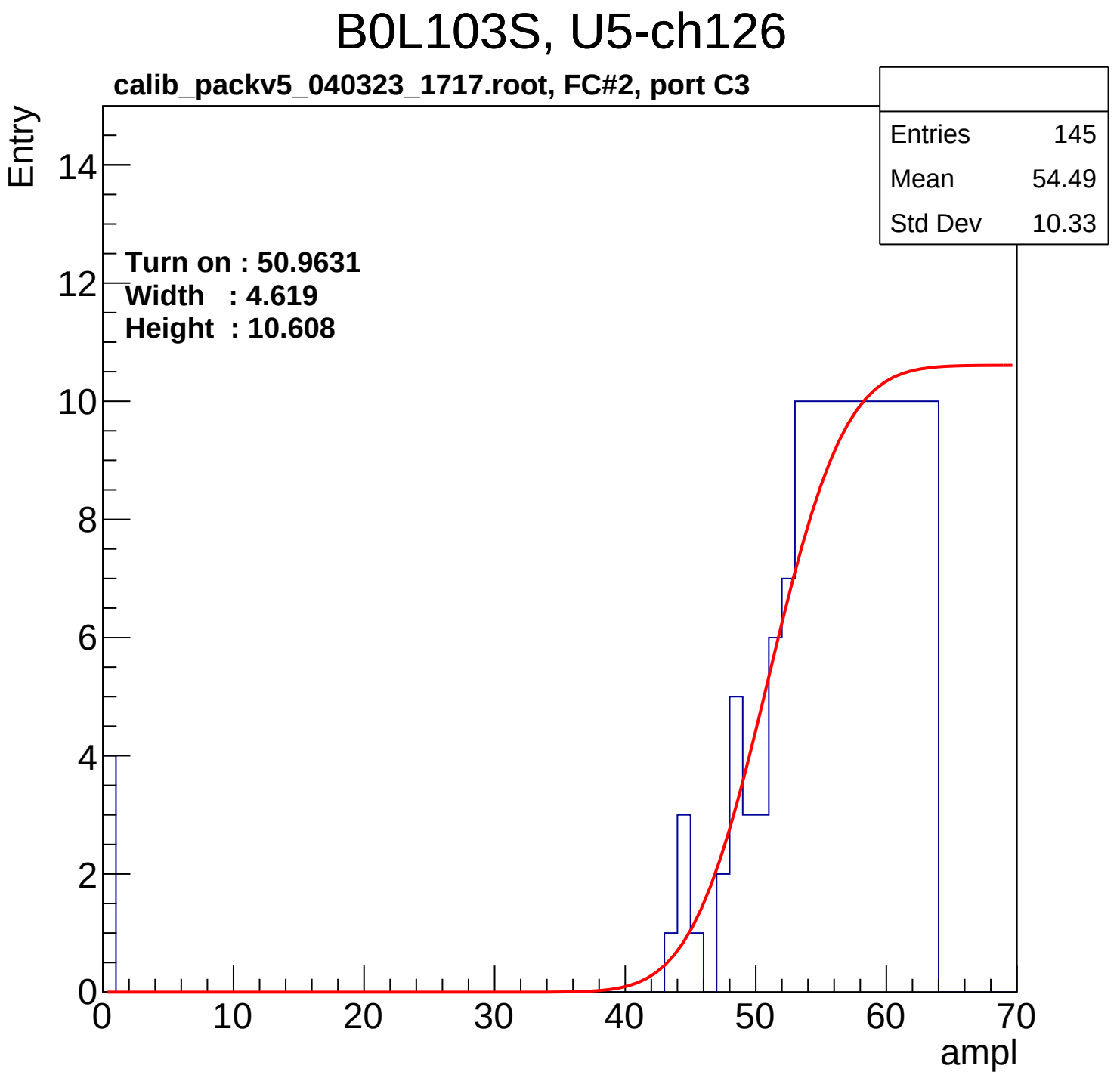
B0L103S, U5-ch126
calib_packv5_040323_1717.root, FC#2, port C3
Entries 145
Mean 54.49
Std Dev 10.33
Turn on : 50.9631
Width : 4.619
Height : 10.608
Entry
ampl
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4
6
8
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0
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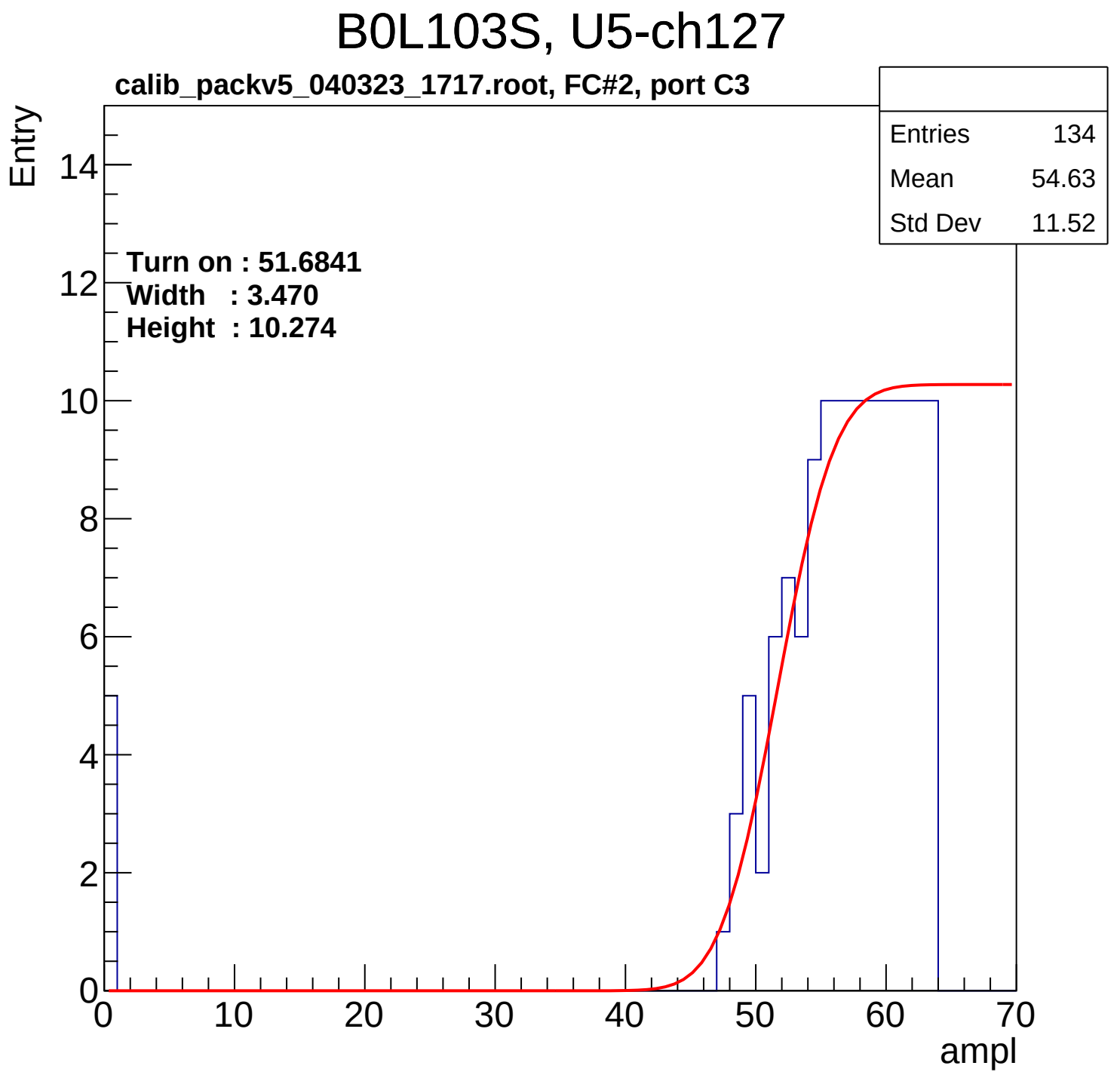
B0L103S, U5-ch127
calib_packv5_040323_1717.root, FC#2, port C3
Entries 134
Mean 54.63
Std Dev 11.52
Turn on : 51.6841
Width : 3.470
Height : 10.274
Entry
ampl
0
2
4
6
8
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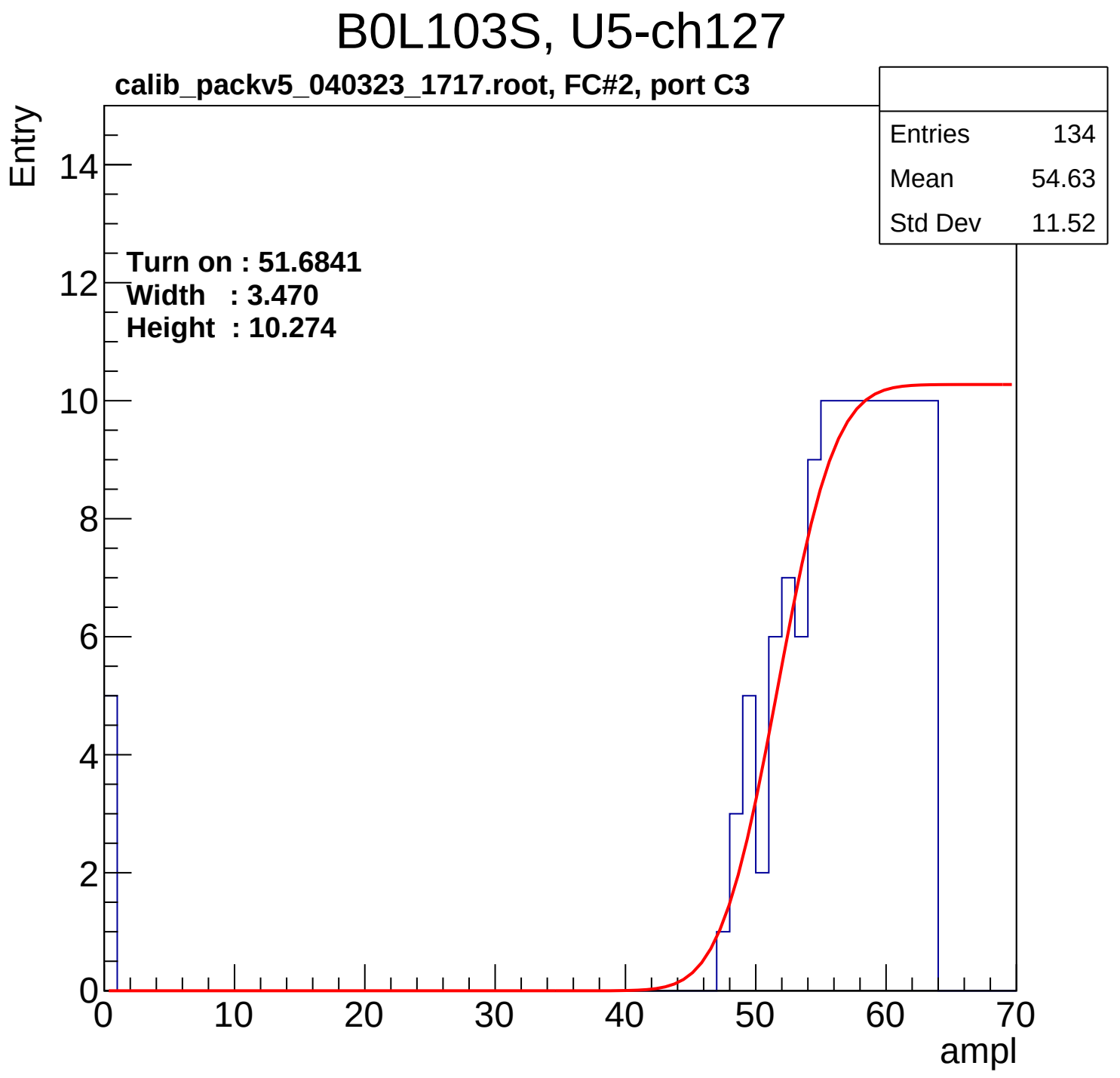
B0L103S, U5-ch127
calib_packv5_040323_1717.root, FC#2, port C3
Entries 134
Mean 54.63
Std Dev 11.52
Turn on : 51.6841
Width : 3.470
Height : 10.274
Entry
ampl
0
2
4
6
8
10
12
14
0
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