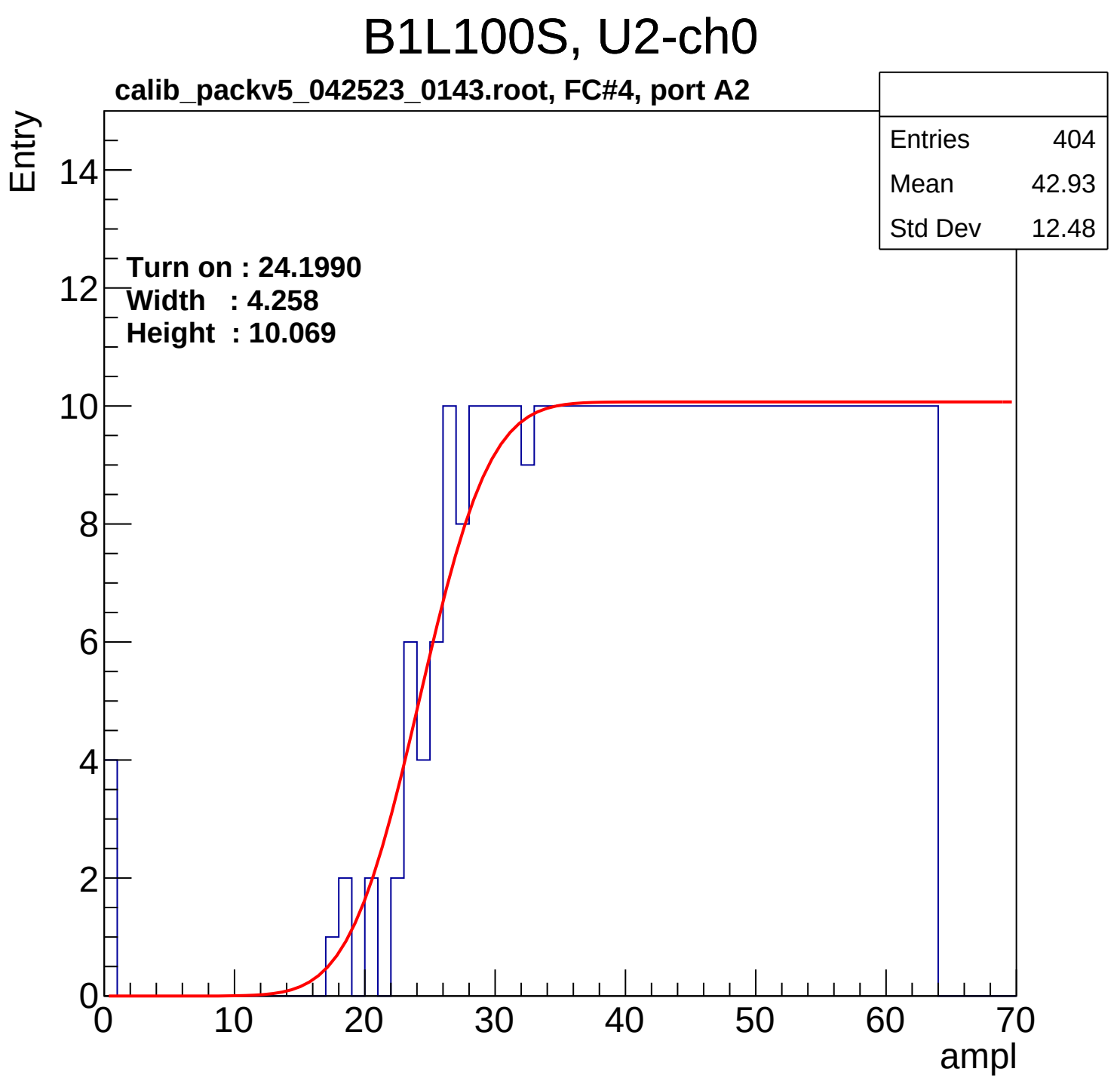
B1L100S, U2-ch0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 404
Mean 42.93
Std Dev 12.48
Turn on : 24.1990
Width : 4.258
Height : 10.069
Entry
ampl
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8
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0
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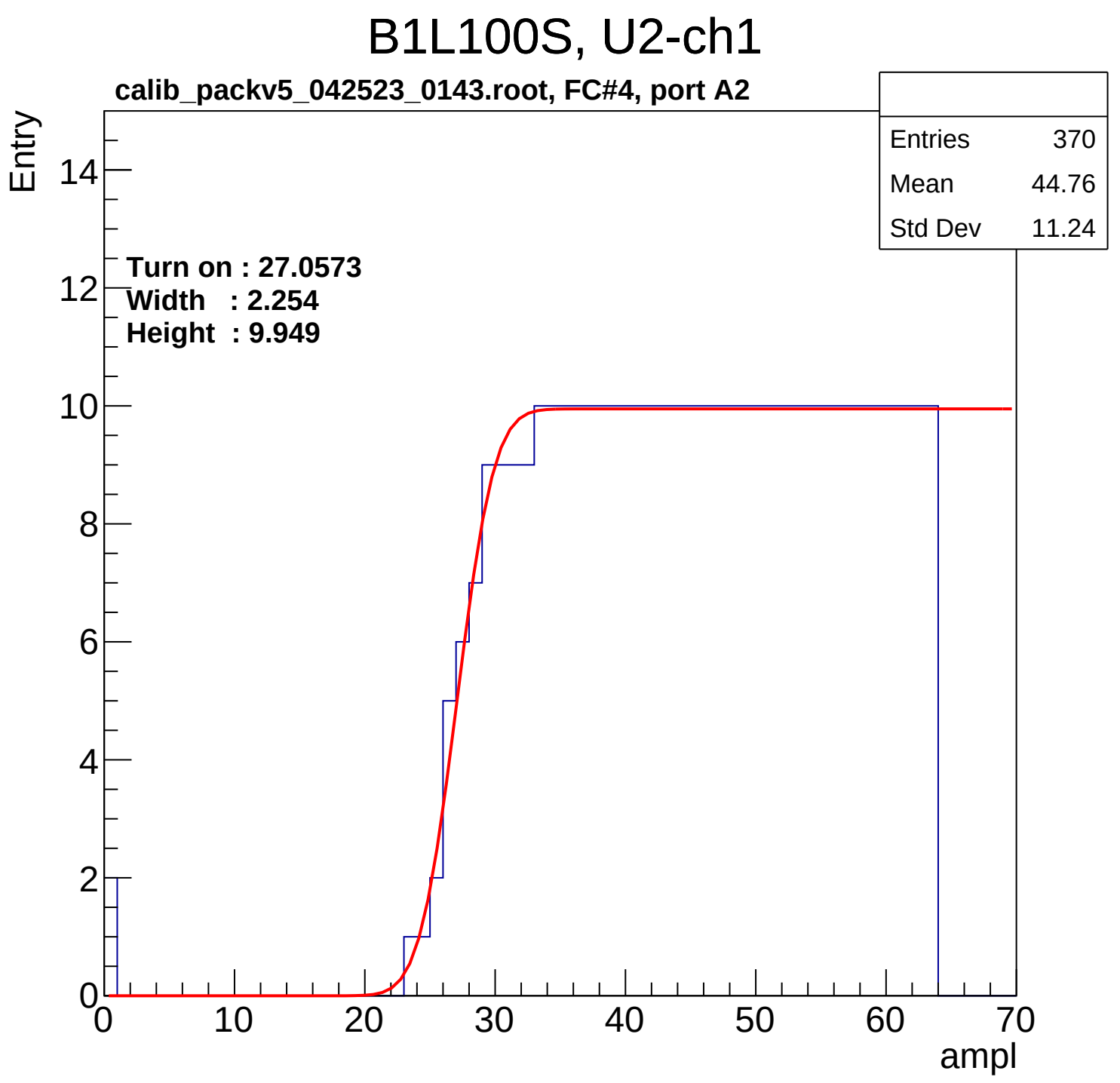
B1L100S, U2-ch1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 370
Mean 44.76
Std Dev 11.24
Turn on : 27.0573
Width : 2.254
Height : 9.949
Entry
ampl
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2
4
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8
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0
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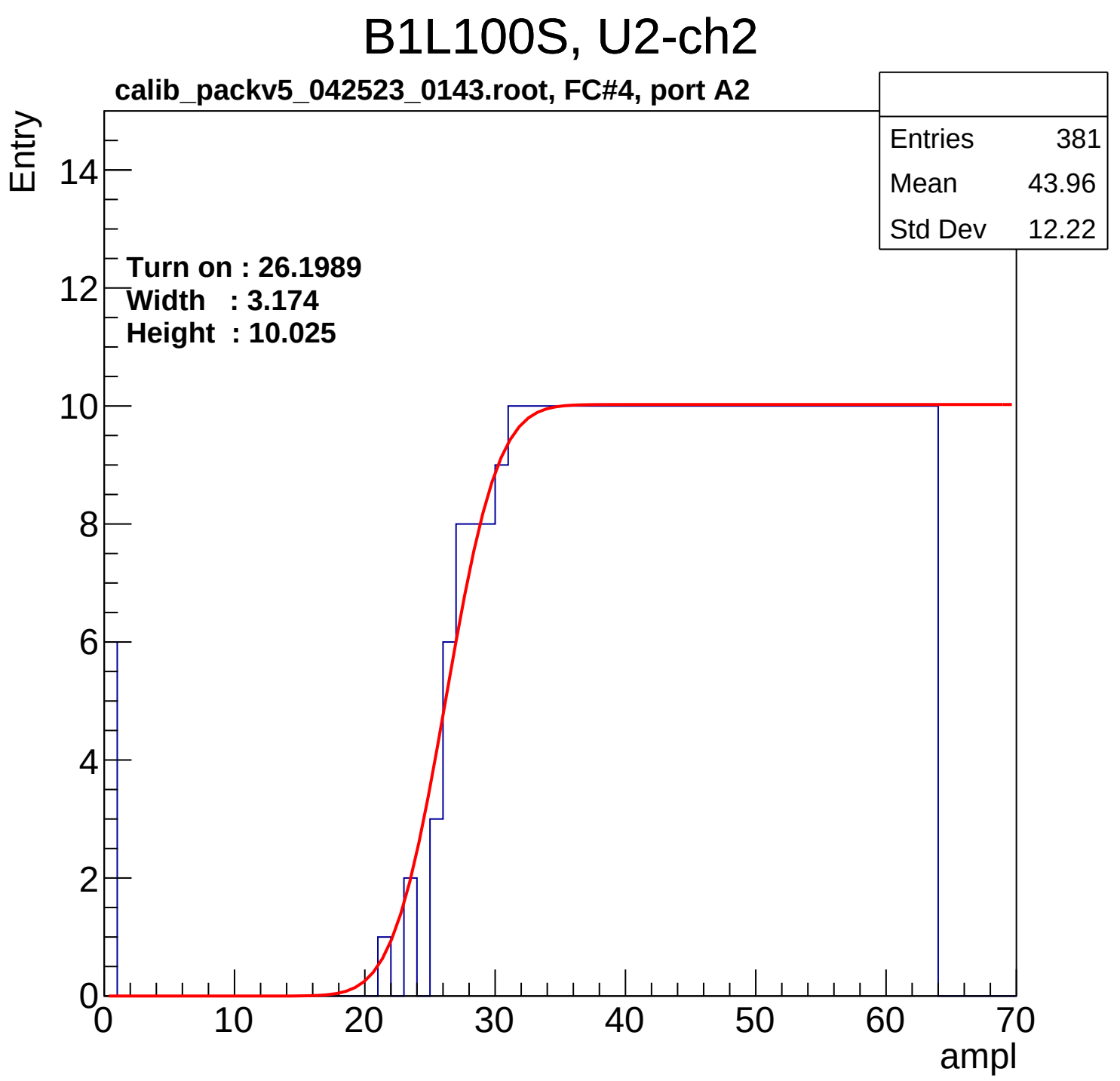
B1L100S, U2-ch2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 381
Mean 43.96
Std Dev 12.22
Turn on : 26.1989
Width : 3.174
Height : 10.025
Entry
ampl
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2
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6
8
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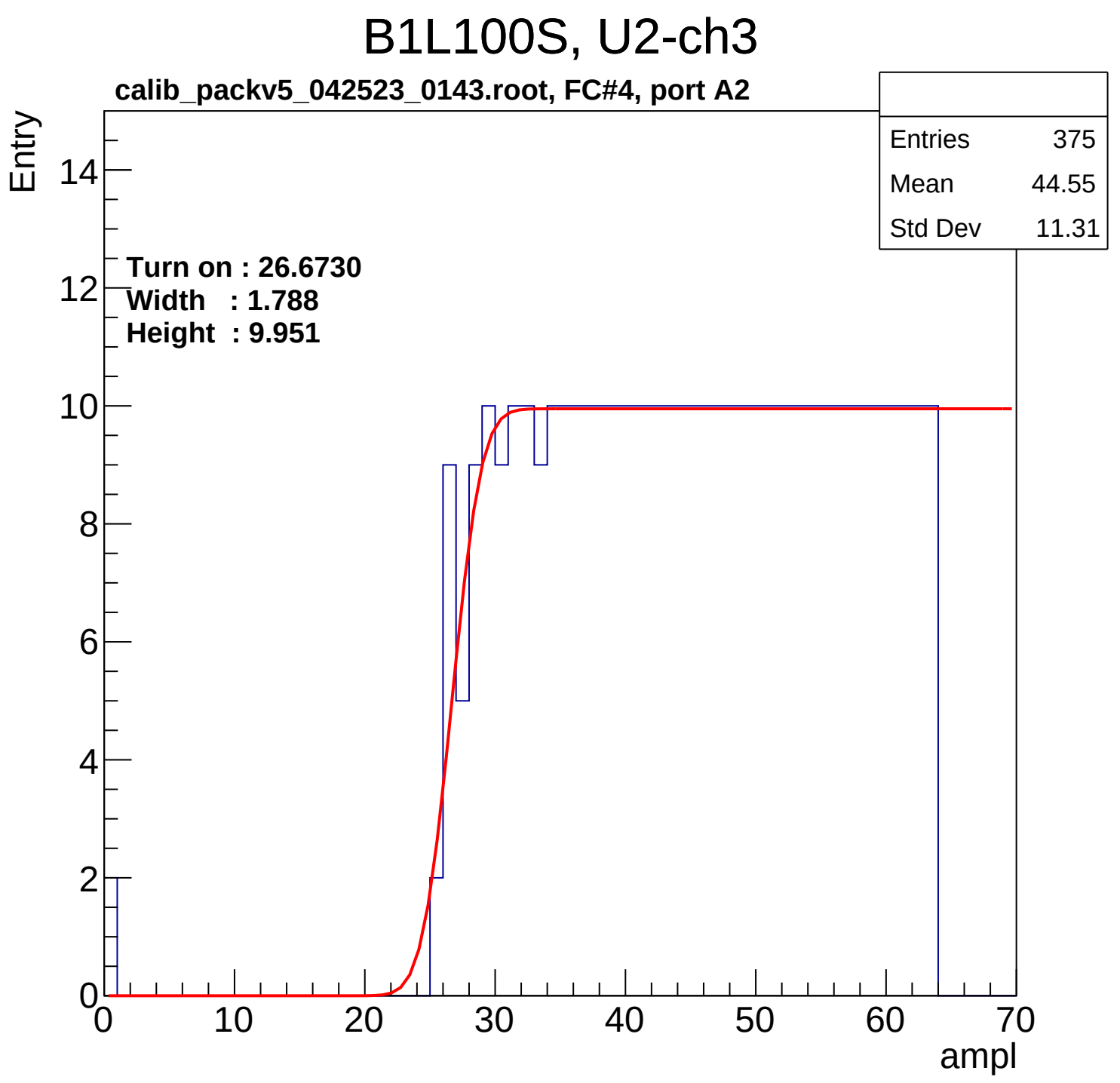
B1L100S, U2-ch3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 375
Mean 44.55
Std Dev 11.31
Turn on : 26.6730
Width : 1.788
Height : 9.951
Entry
ampl
0
2
4
6
8
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12
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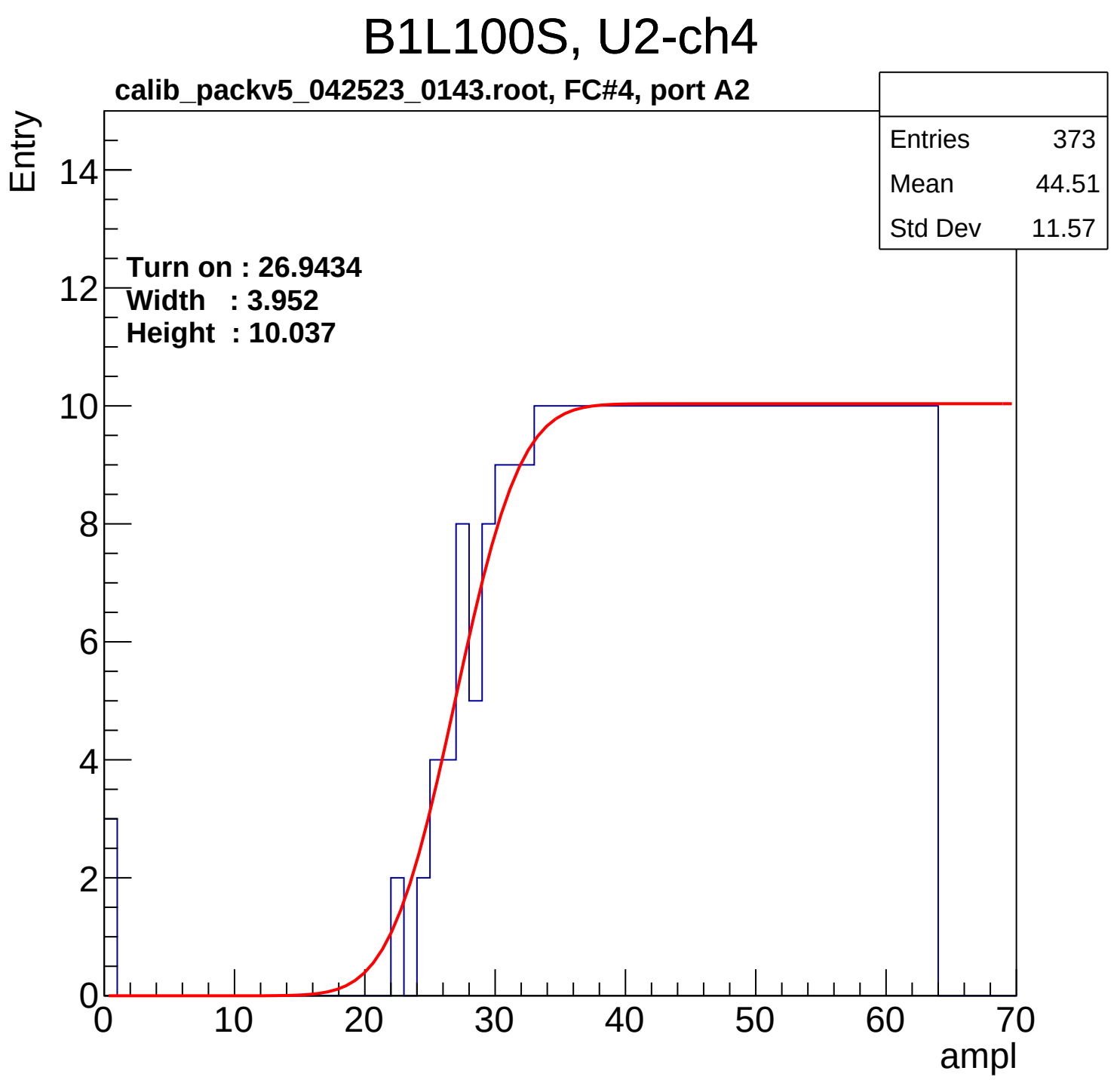
B1L100S, U2-ch4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 373
Mean 44.51
Std Dev 11.57
Turn on : 26.9434
Width : 3.952
Height : 10.037
Entry
ampl
0
2
4
6
8
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0
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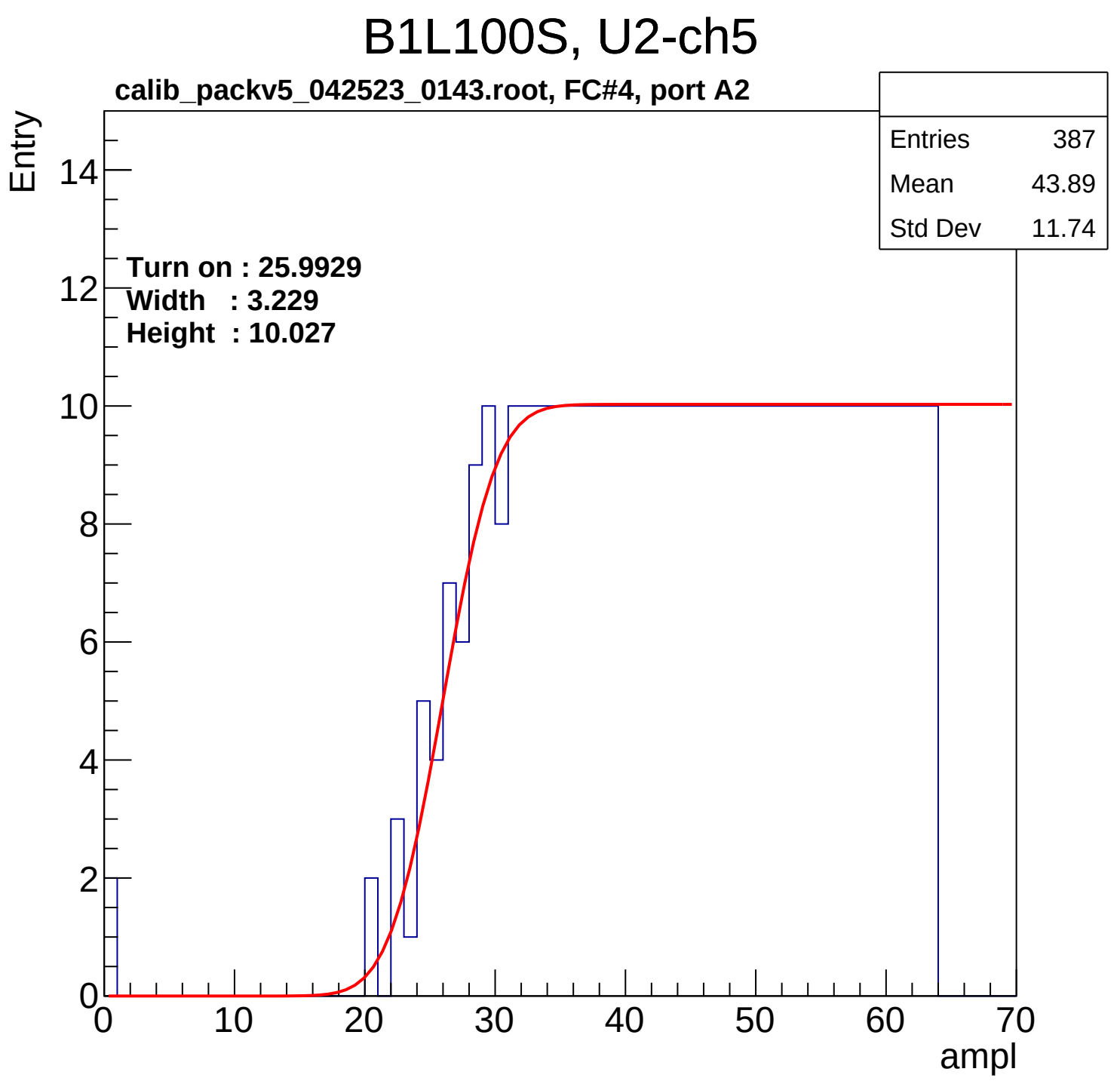
B1L100S, U2-ch5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 387
Mean 43.89
Std Dev 11.74
Turn on : 25.9929
Width : 3.229
Height : 10.027
Entry
ampl
0
2
4
6
8
10
12
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0
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60
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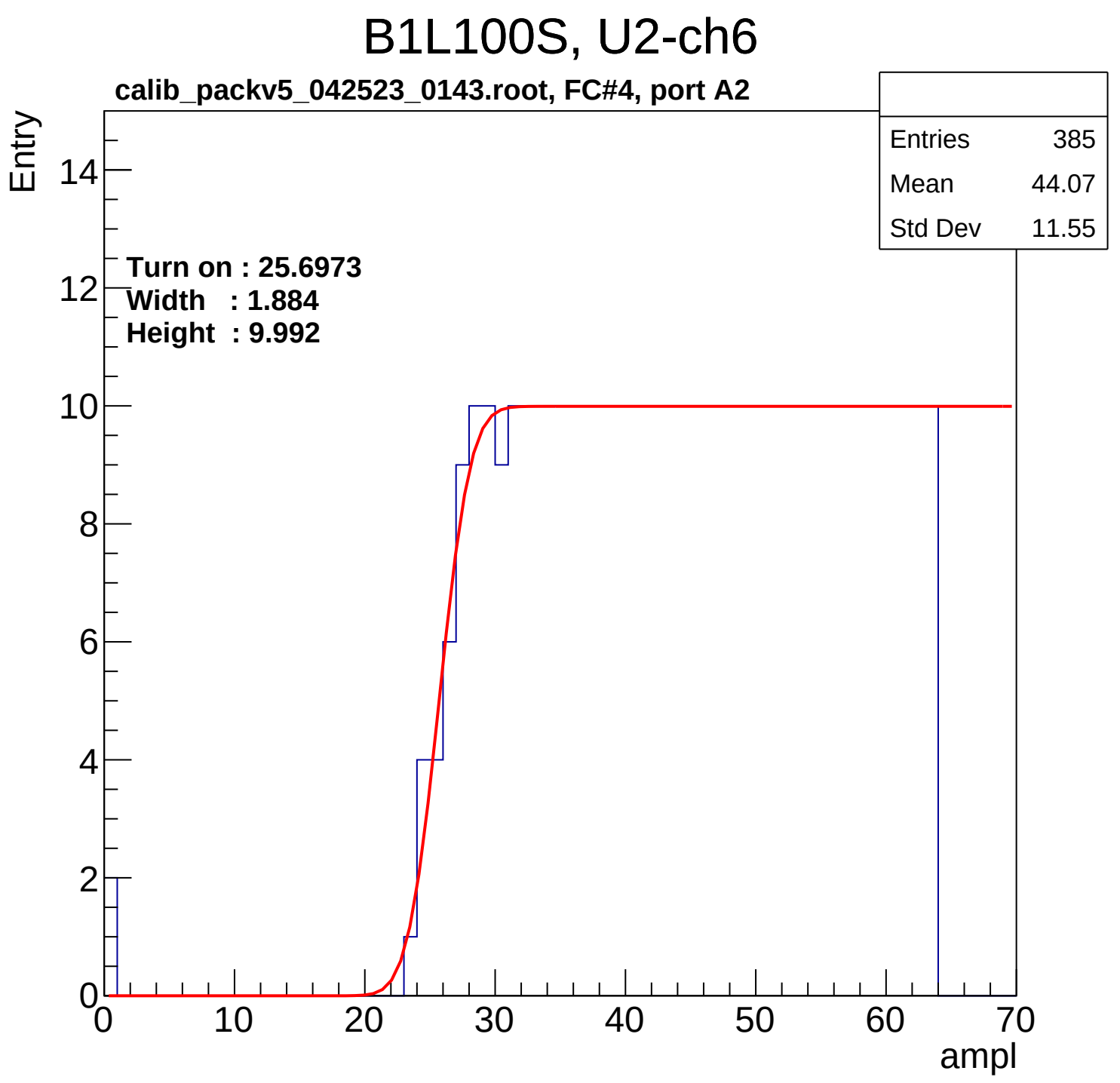
B1L100S, U2-ch6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 385
Mean 44.07
Std Dev 11.55
Turn on : 25.6973
Width : 1.884
Height : 9.992
Entry
ampl
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2
4
6
8
10
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0
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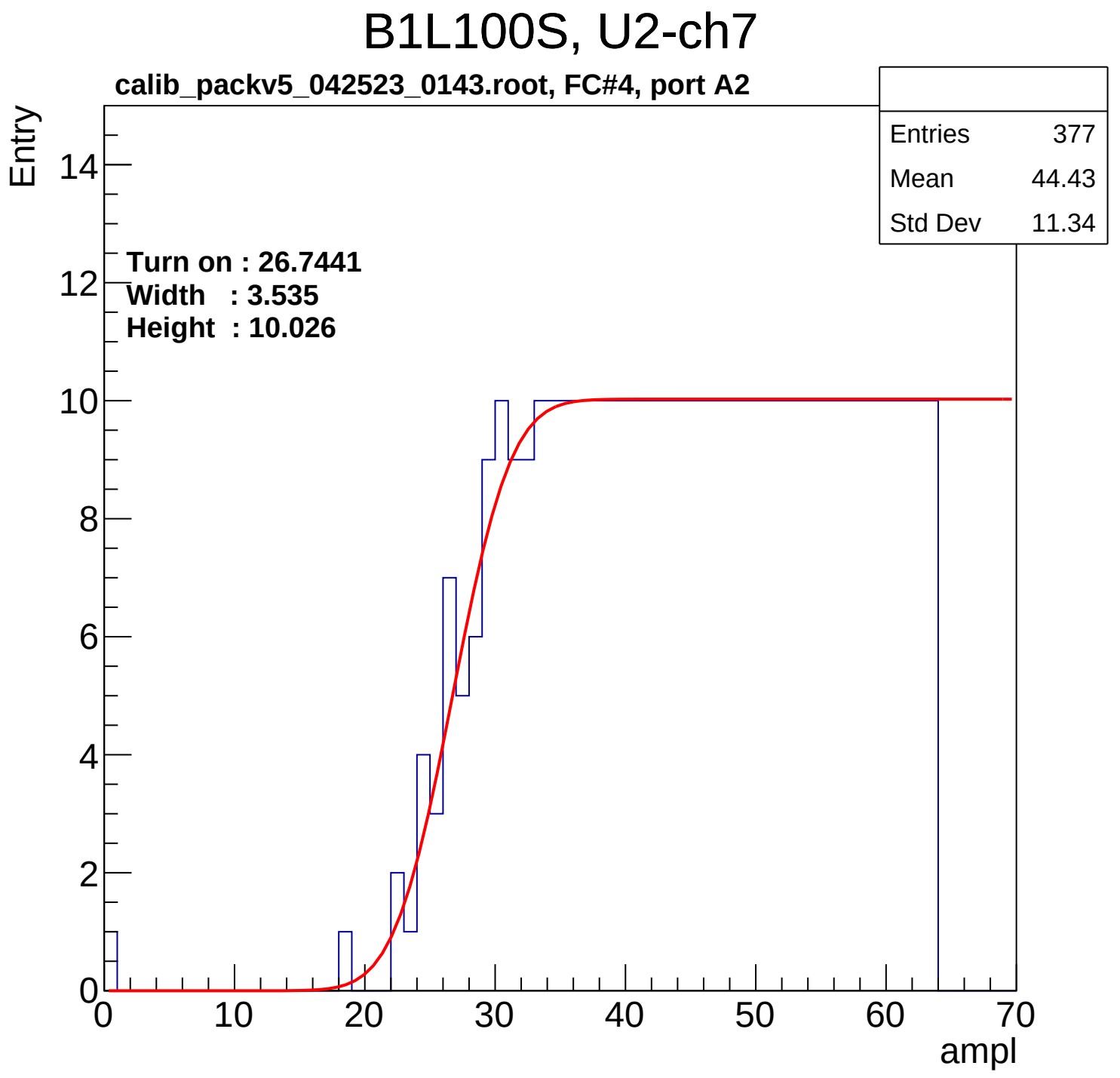
B1L100S, U2-ch7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 377
Mean 44.43
Std Dev 11.34
Turn on : 26.7441
Width : 3.535
Height : 10.026
Entry
ampl
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2
4
6
8
10
12
14
0
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20
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40
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60
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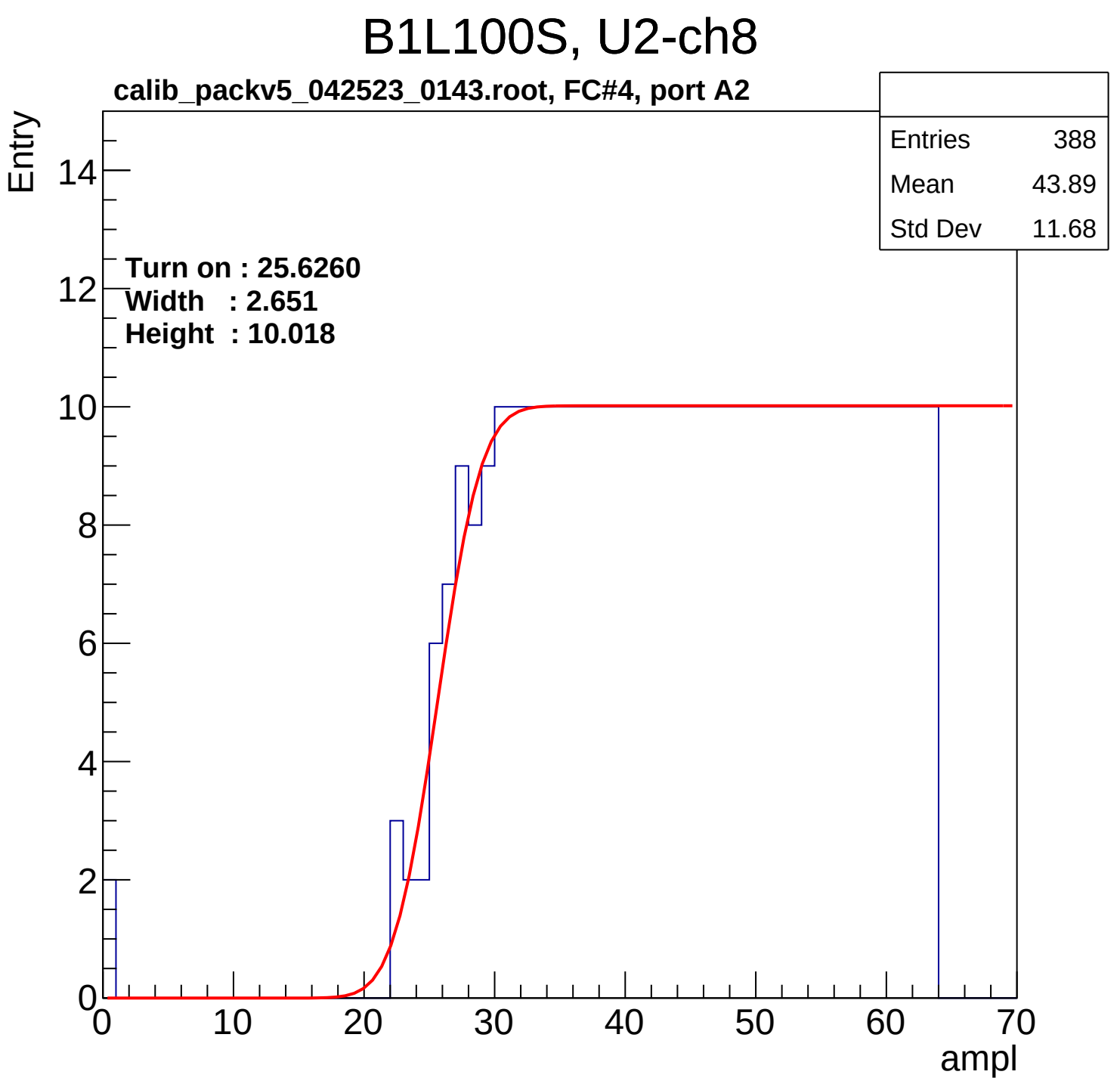
B1L100S, U2-ch8
calib_packv5_042523_0143.root, FC#4, port A2
Entries 388
Mean 43.89
Std Dev 11.68
Turn on : 25.6260
Width : 2.651
Height : 10.018
Entry
ampl
0
2
4
6
8
10
12
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0
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20
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40
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60
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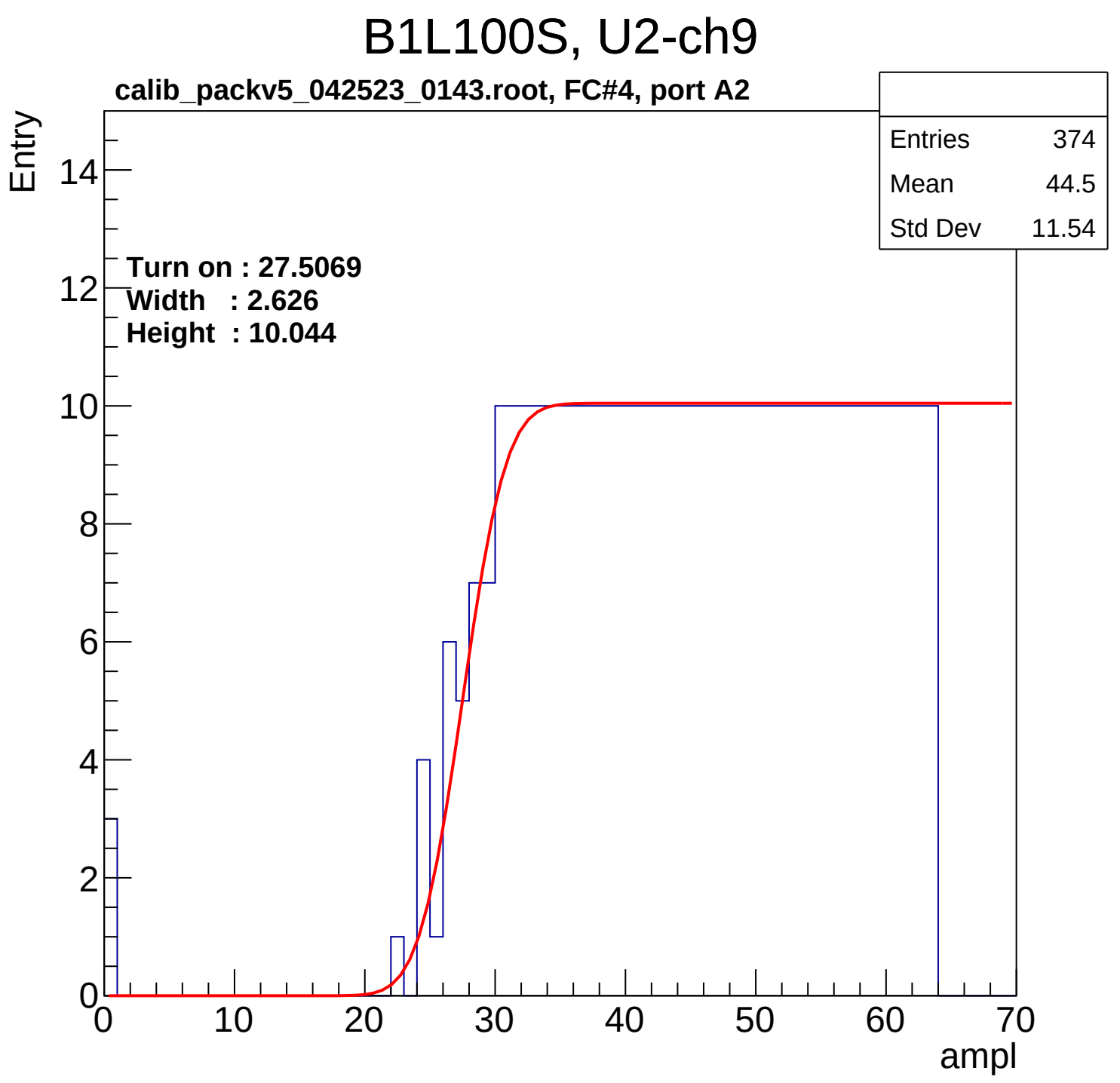
B1L100S, U2-ch9
calib_packv5_042523_0143.root, FC#4, port A2
Entries 374
Mean 44.5
Std Dev 11.54
Turn on : 27.5069
Width : 2.626
Height : 10.044
Entry
ampl
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2
4
6
8
10
12
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0
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20
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60
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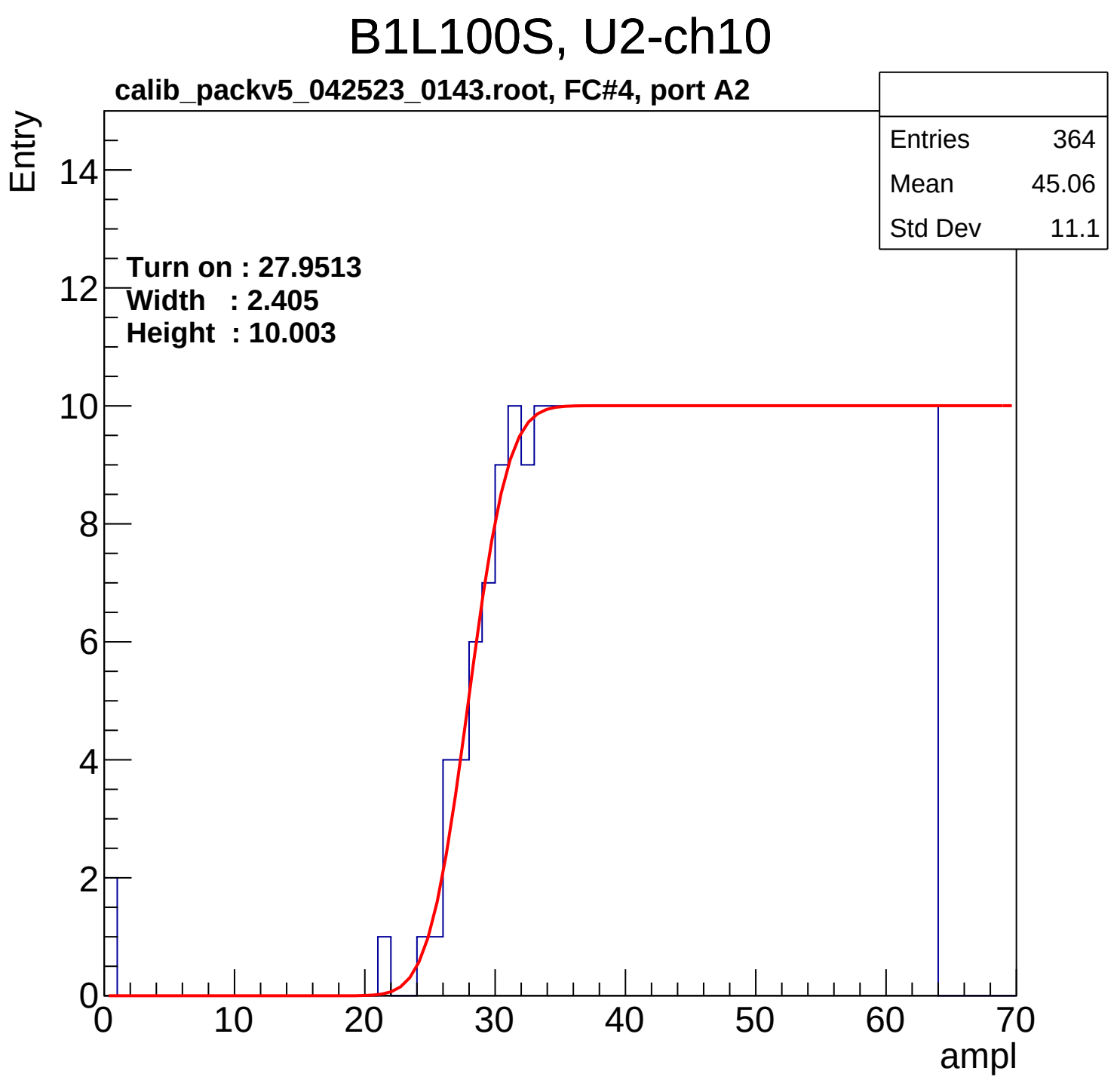
B1L100S, U2-ch10
calib_packv5_042523_0143.root, FC#4, port A2
Entries 364
Mean 45.06
Std Dev 11.1
Turn on : 27.9513
Width : 2.405
Height : 10.003
Entry
ampl
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4
6
8
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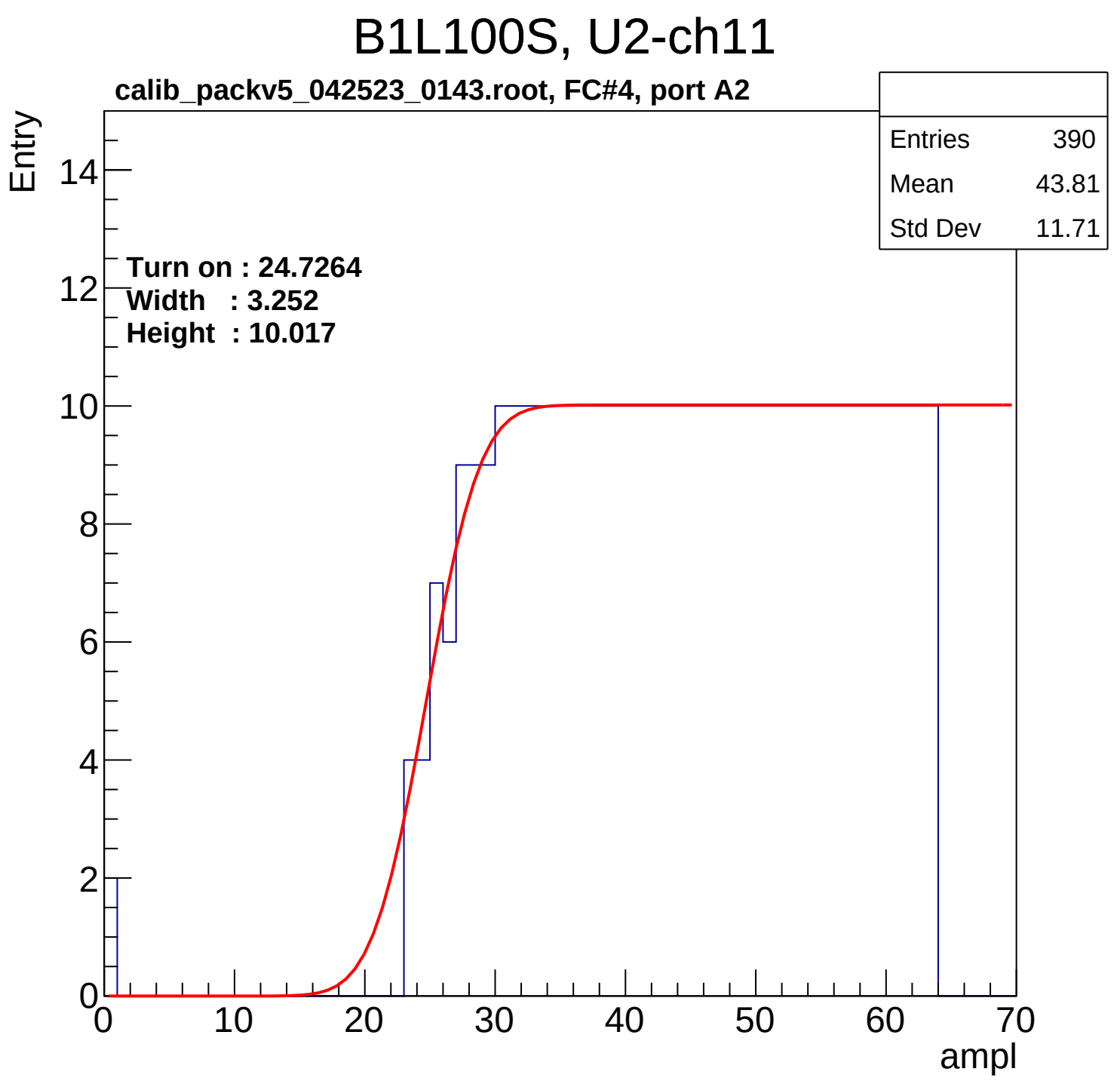
B1L100S, U2-ch11
calib_packv5_042523_0143.root, FC#4, port A2
Entries 390
Mean 43.81
Std Dev 11.71
Turn on : 24.7264
Width : 3.252
Height : 10.017
Entry
ampl
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6
8
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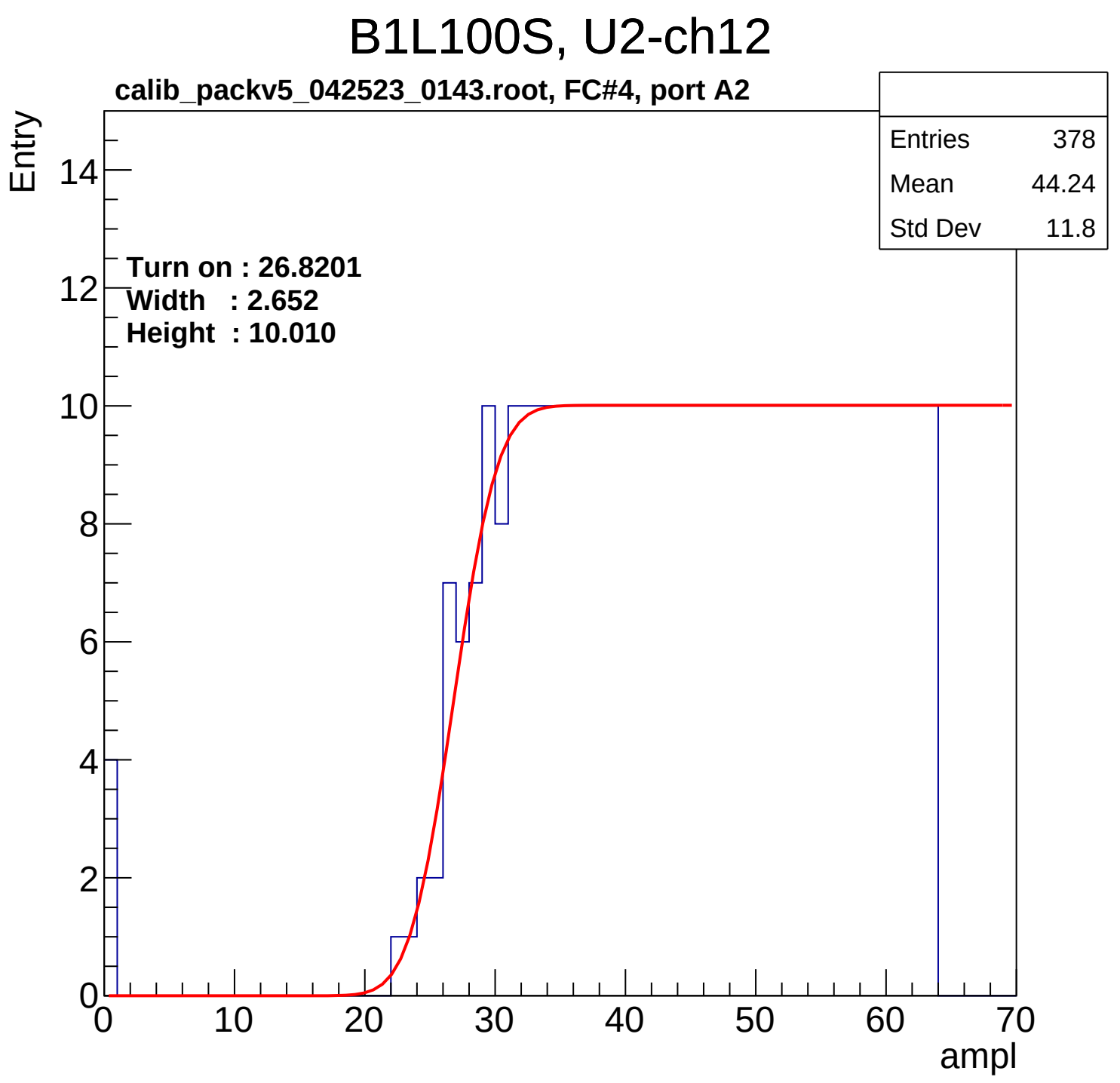
B1L100S, U2-ch12
calib_packv5_042523_0143.root, FC#4, port A2
Entries 378
Mean 44.24
Std Dev 11.8
Turn on : 26.8201
Width : 2.652
Height : 10.010
Entry
ampl
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4
6
8
10
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0
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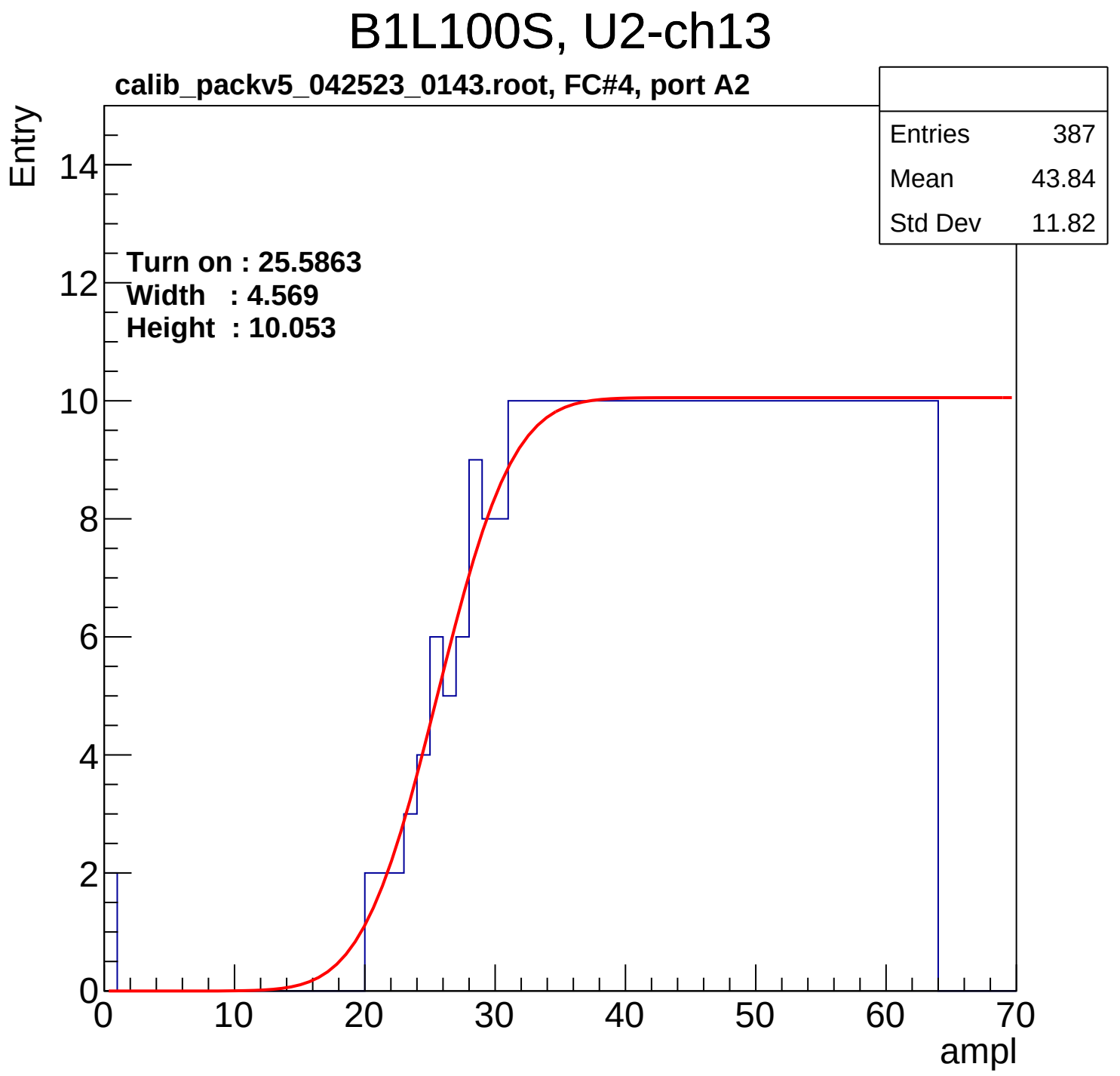
B1L100S, U2-ch13
calib_packv5_042523_0143.root, FC#4, port A2
Entries 387
Mean 43.84
Std Dev 11.82
Turn on : 25.5863
Width : 4.569
Height : 10.053
Entry
ampl
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6
8
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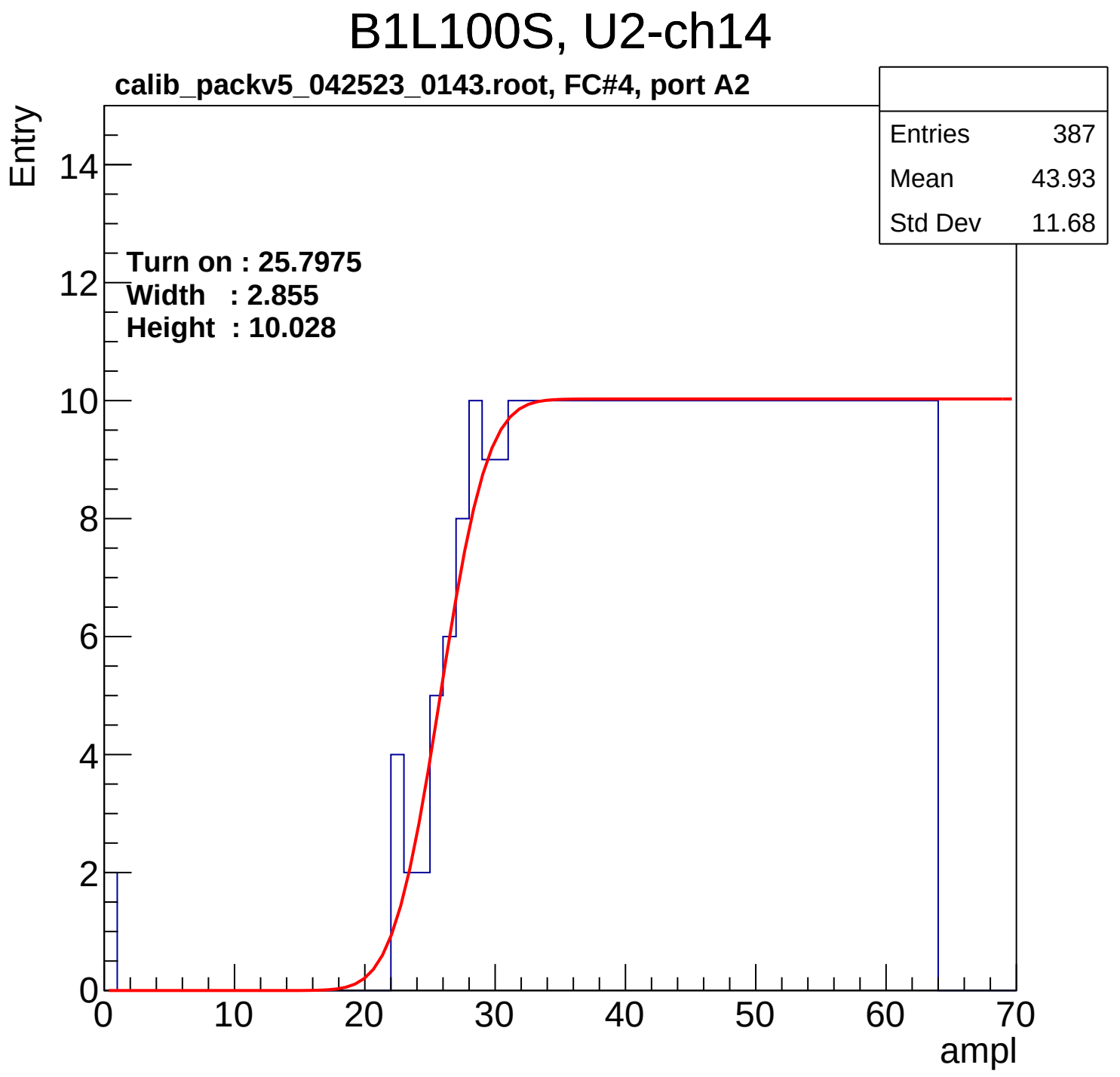
B1L100S, U2-ch14
calib_packv5_042523_0143.root, FC#4, port A2
Entries 387
Mean 43.93
Std Dev 11.68
Turn on : 25.7975
Width : 2.855
Height : 10.028
Entry
ampl
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4
6
8
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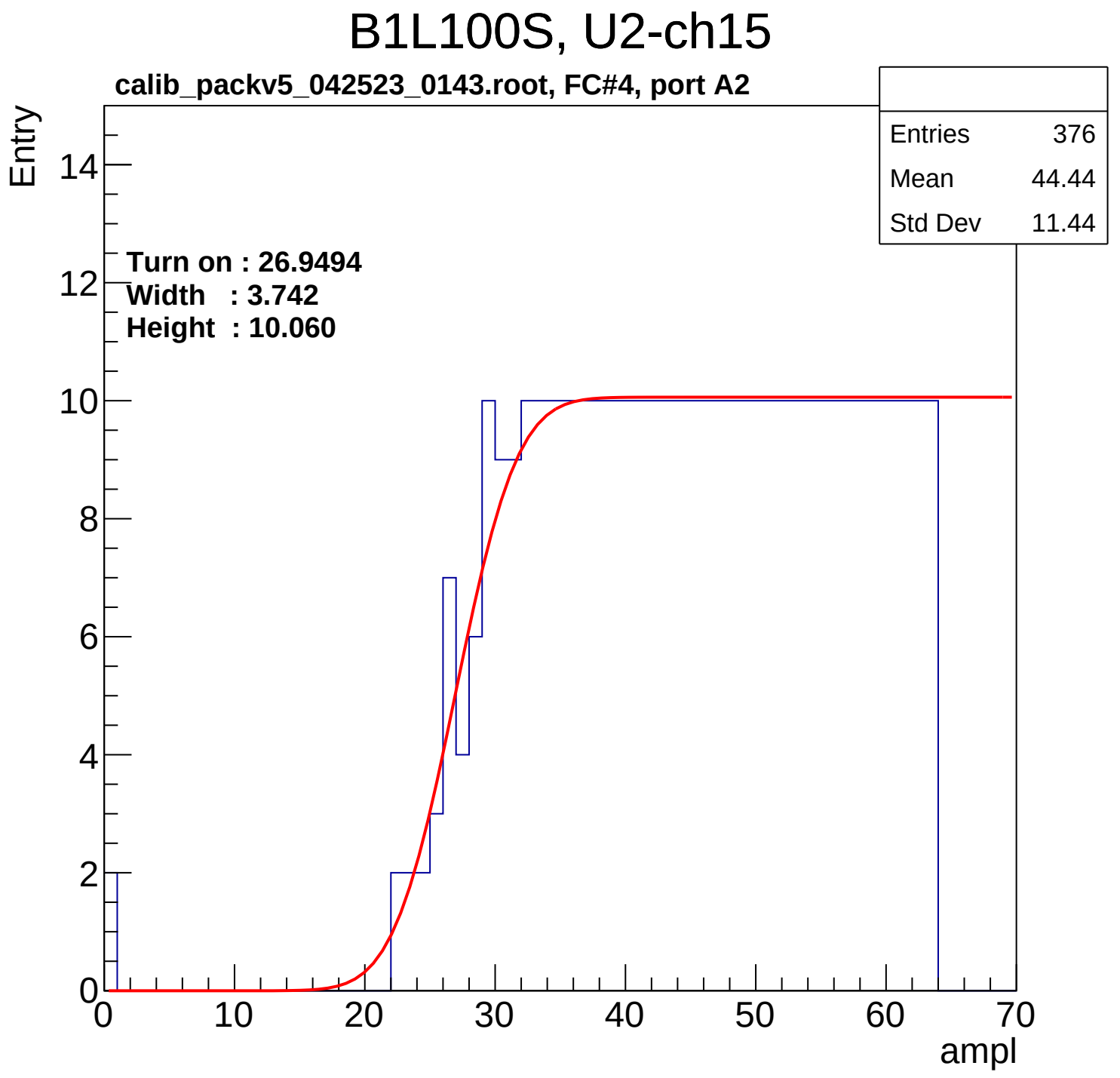
B1L100S, U2-ch15
calib_packv5_042523_0143.root, FC#4, port A2
Entries 376
Mean 44.44
Std Dev 11.44
Turn on : 26.9494
Width : 3.742
Height : 10.060
Entry
ampl
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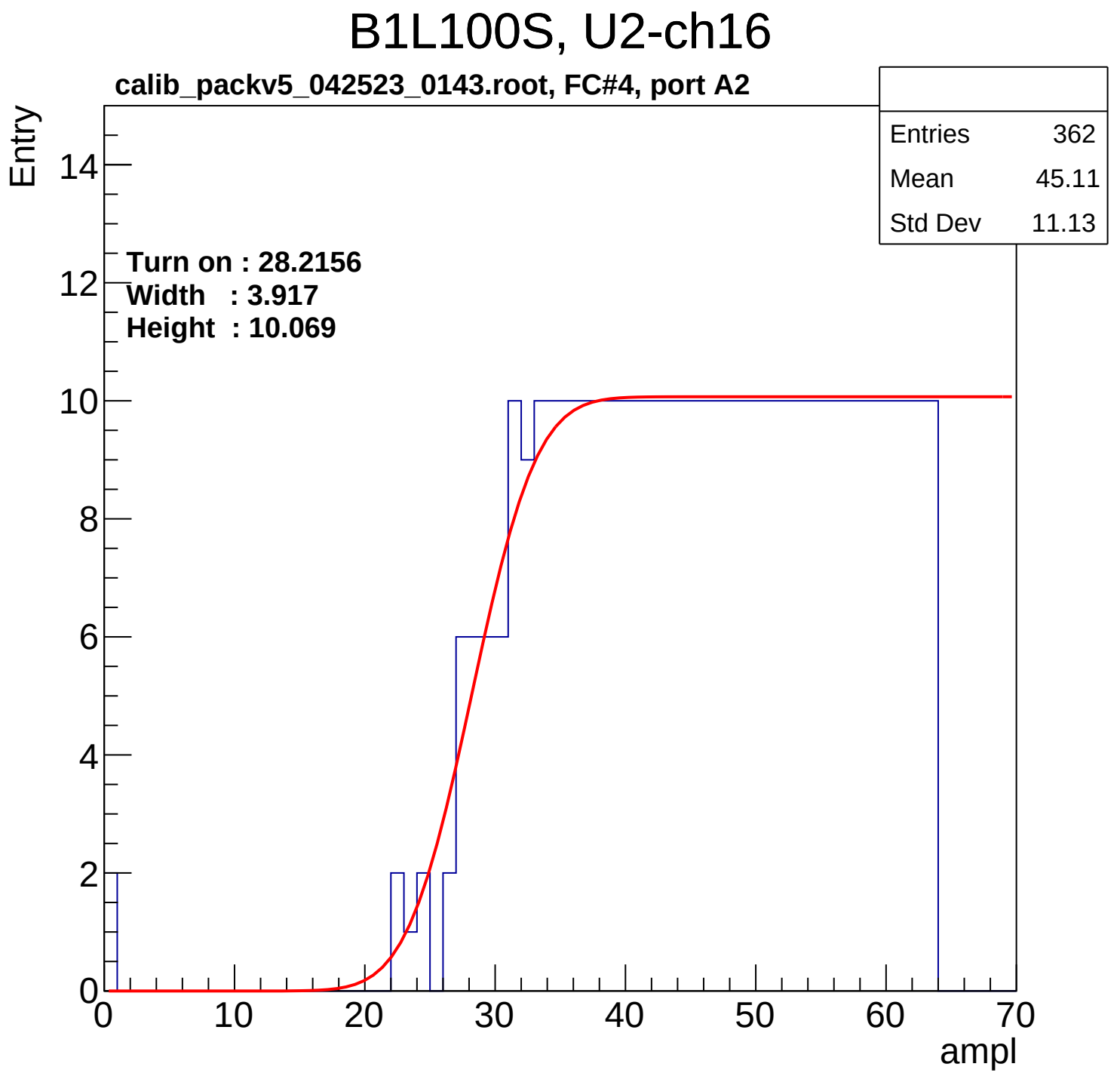
B1L100S, U2-ch16
calib_packv5_042523_0143.root, FC#4, port A2
Entries 362
Mean 45.11
Std Dev 11.13
Turn on : 28.2156
Width : 3.917
Height : 10.069
Entry
ampl
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4
6
8
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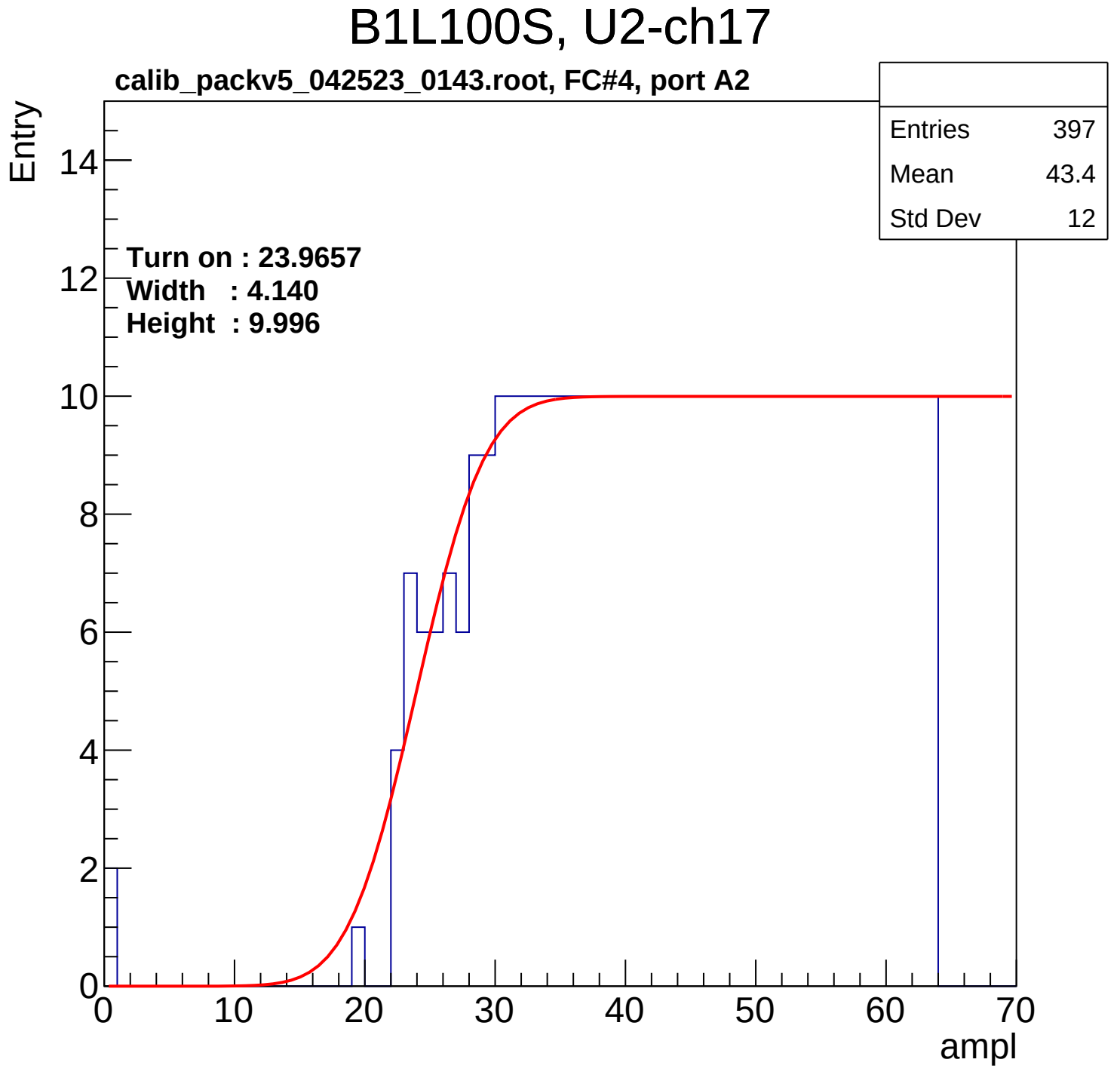
B1L100S, U2-ch17
calib_packv5_042523_0143.root, FC#4, port A2
Entries 397
Mean 43.4
Std Dev 12
Turn on : 23.9657
Width : 4.140
Height : 9.996
Entry
ampl
0
2
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6
8
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0
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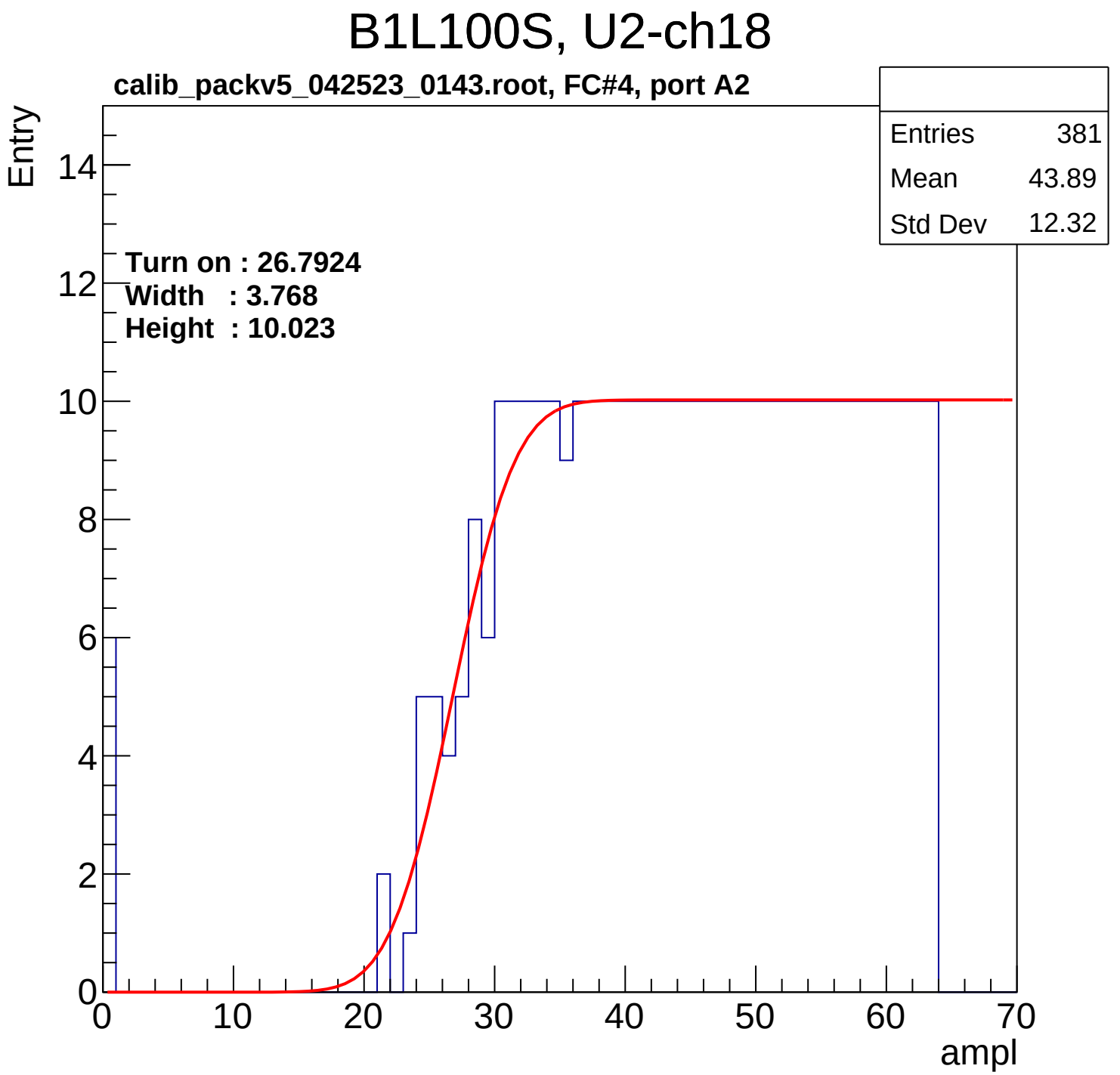
B1L100S, U2-ch18
calib_packv5_042523_0143.root, FC#4, port A2
Entries 381
Mean 43.89
Std Dev 12.32
Turn on : 26.7924
Width : 3.768
Height : 10.023
Entry
ampl
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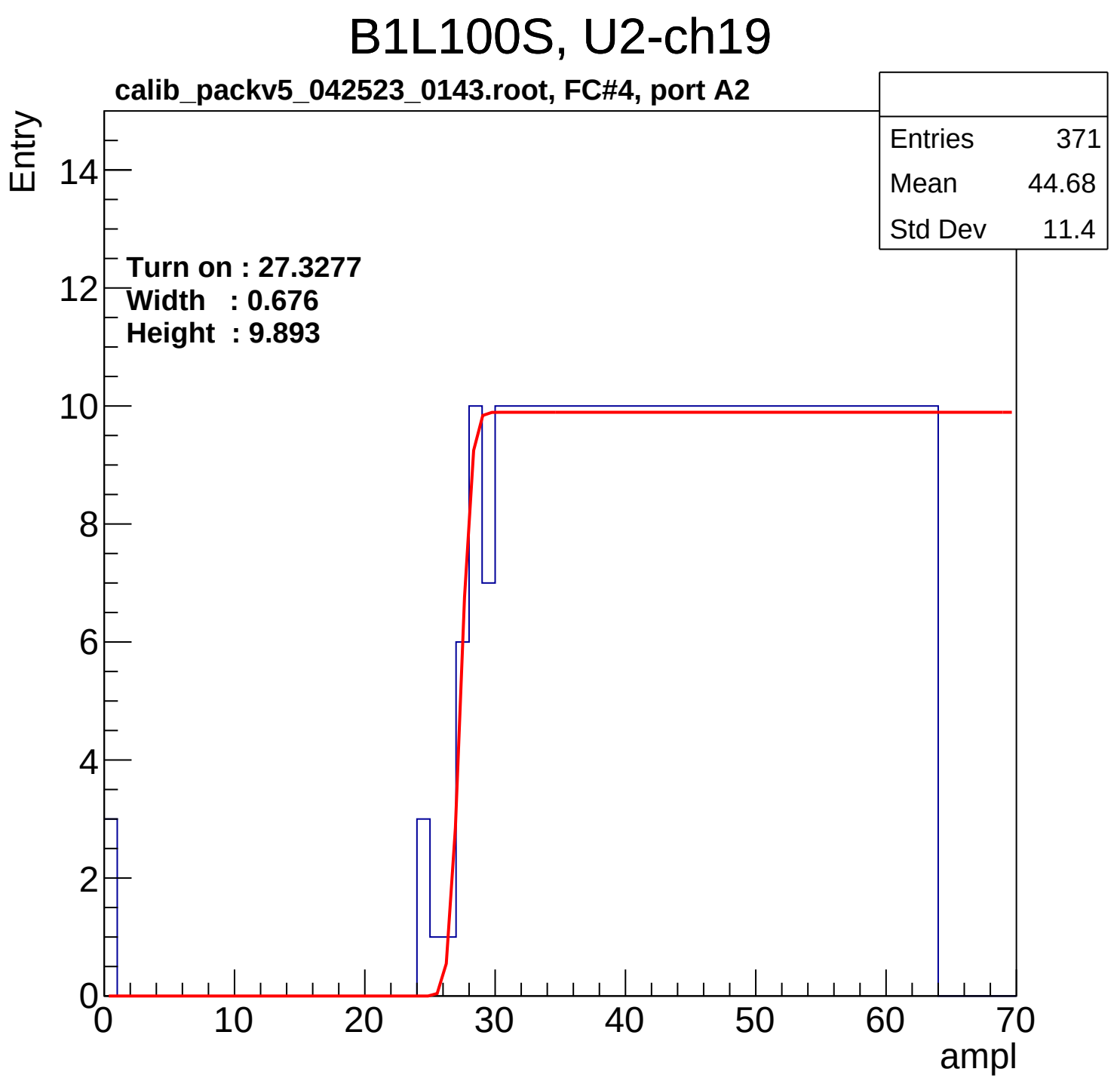
B1L100S, U2-ch19
calib_packv5_042523_0143.root, FC#4, port A2
Entries 371
Mean 44.68
Std Dev 11.4
Turn on : 27.3277
Width : 0.676
Height : 9.893
Entry
ampl
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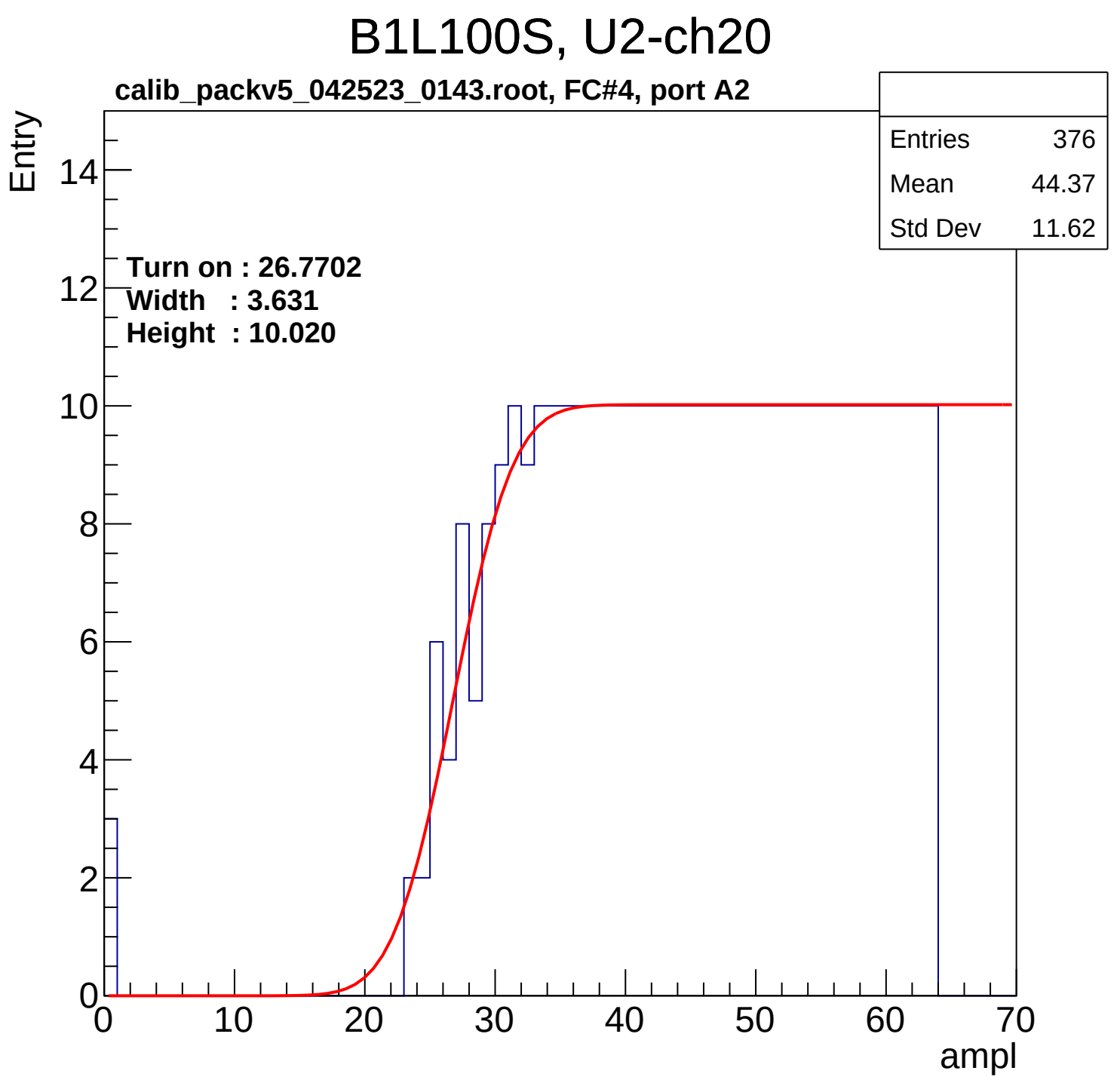
B1L100S, U2-ch20
calib_packv5_042523_0143.root, FC#4, port A2
Entries 376
Mean 44.37
Std Dev 11.62
Turn on : 26.7702
Width : 3.631
Height : 10.020
Entry
ampl
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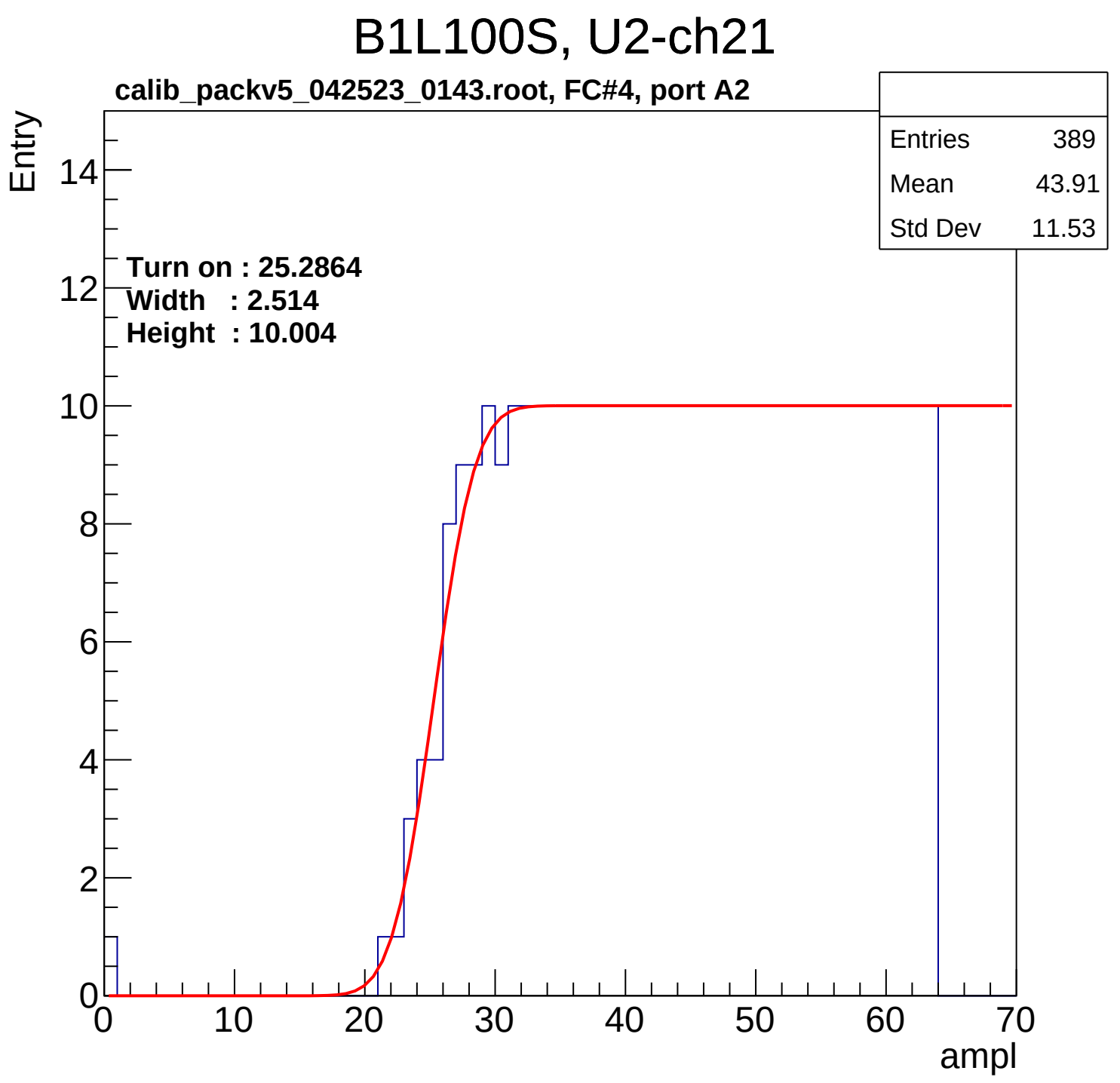
B1L100S, U2-ch21
calib_packv5_042523_0143.root, FC#4, port A2
Entries 389
Mean 43.91
Std Dev 11.53
Turn on : 25.2864
Width : 2.514
Height : 10.004
Entry
ampl
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2
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6
8
10
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0
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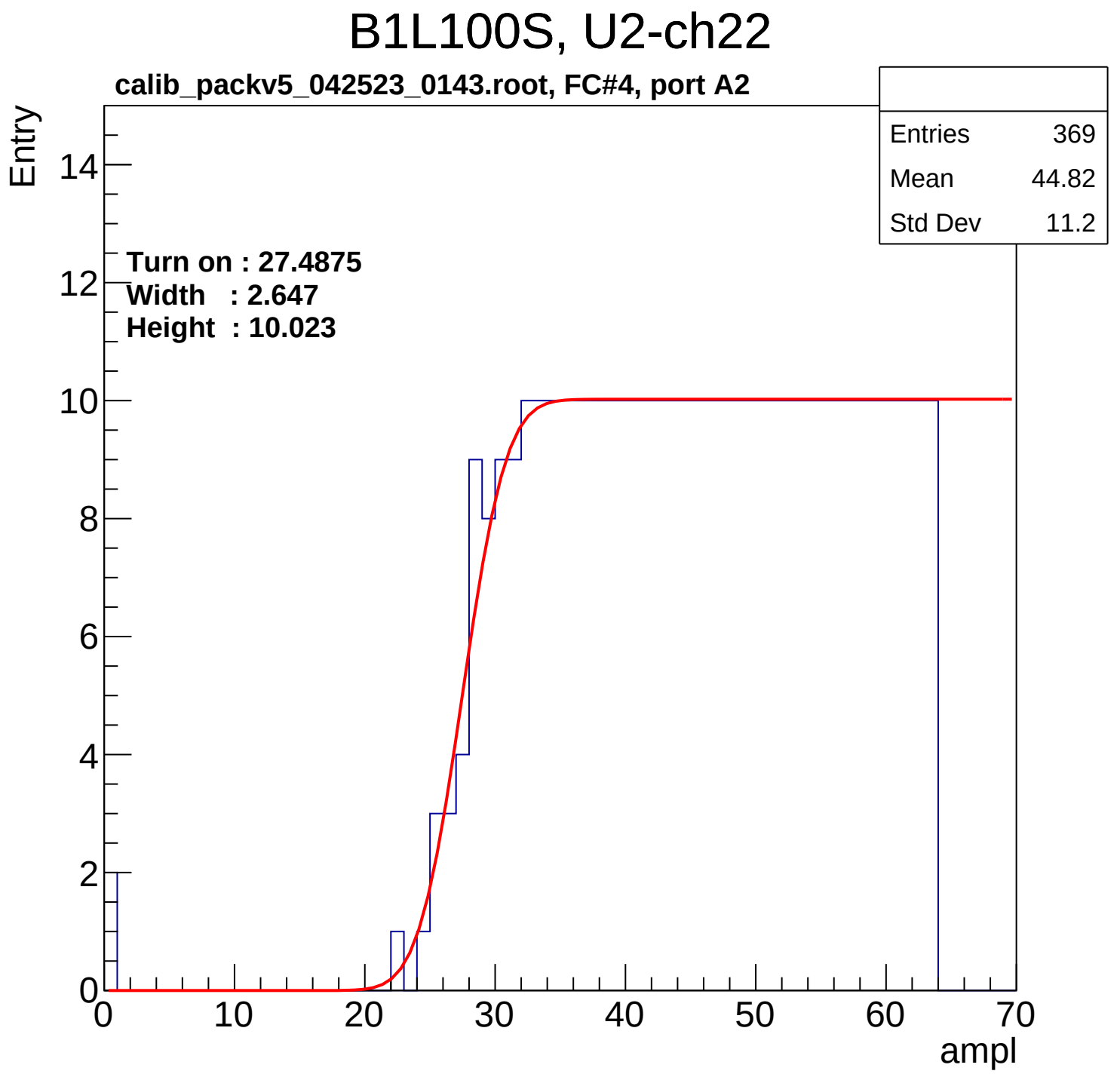
B1L100S, U2-ch22
calib_packv5_042523_0143.root, FC#4, port A2
Entries 369
Mean 44.82
Std Dev 11.2
Turn on : 27.4875
Width : 2.647
Height : 10.023
Entry
ampl
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6
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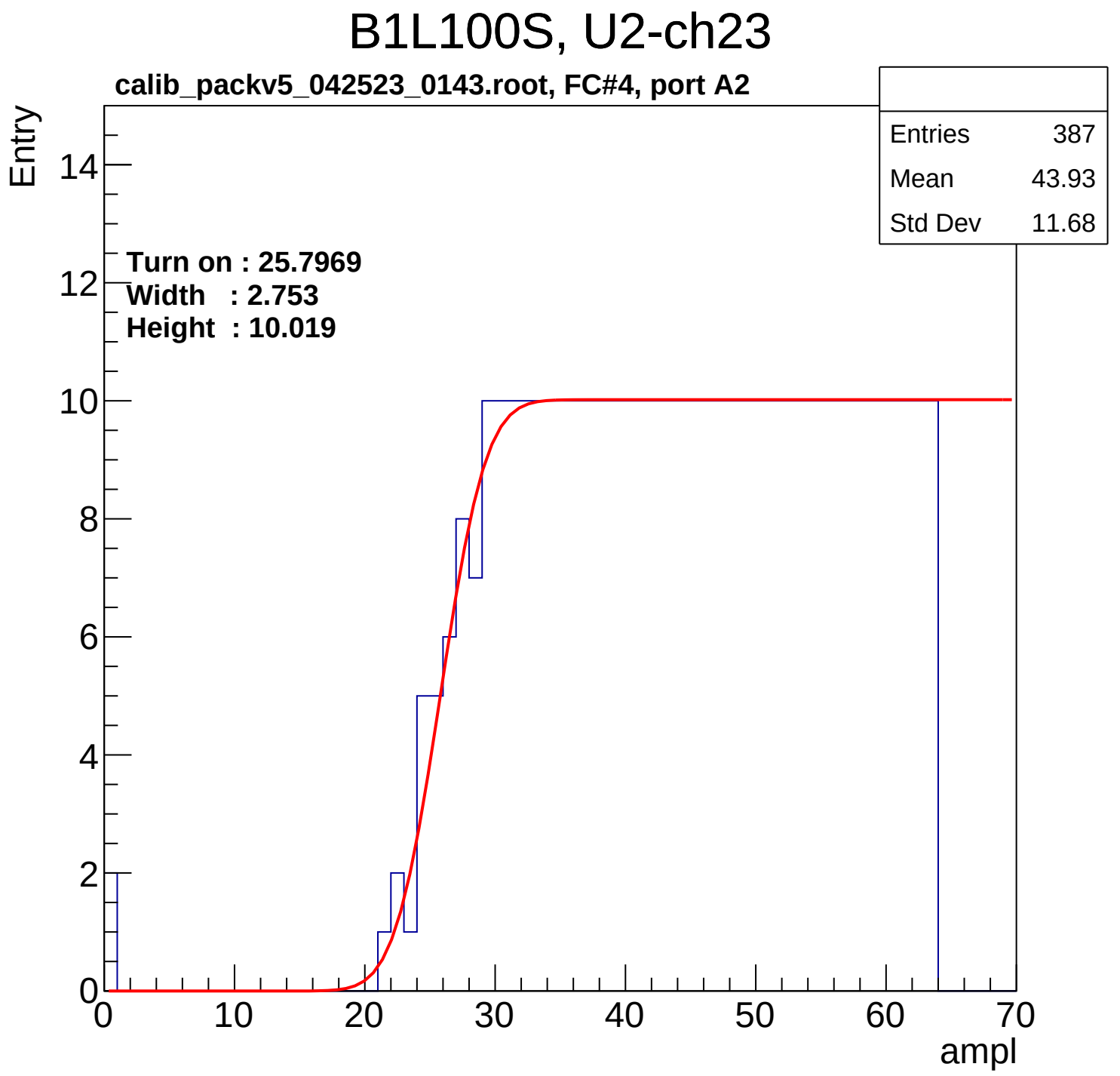
B1L100S, U2-ch23
calib_packv5_042523_0143.root, FC#4, port A2
Entries 387
Mean 43.93
Std Dev 11.68
Turn on : 25.7969
Width : 2.753
Height : 10.019
Entry
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4
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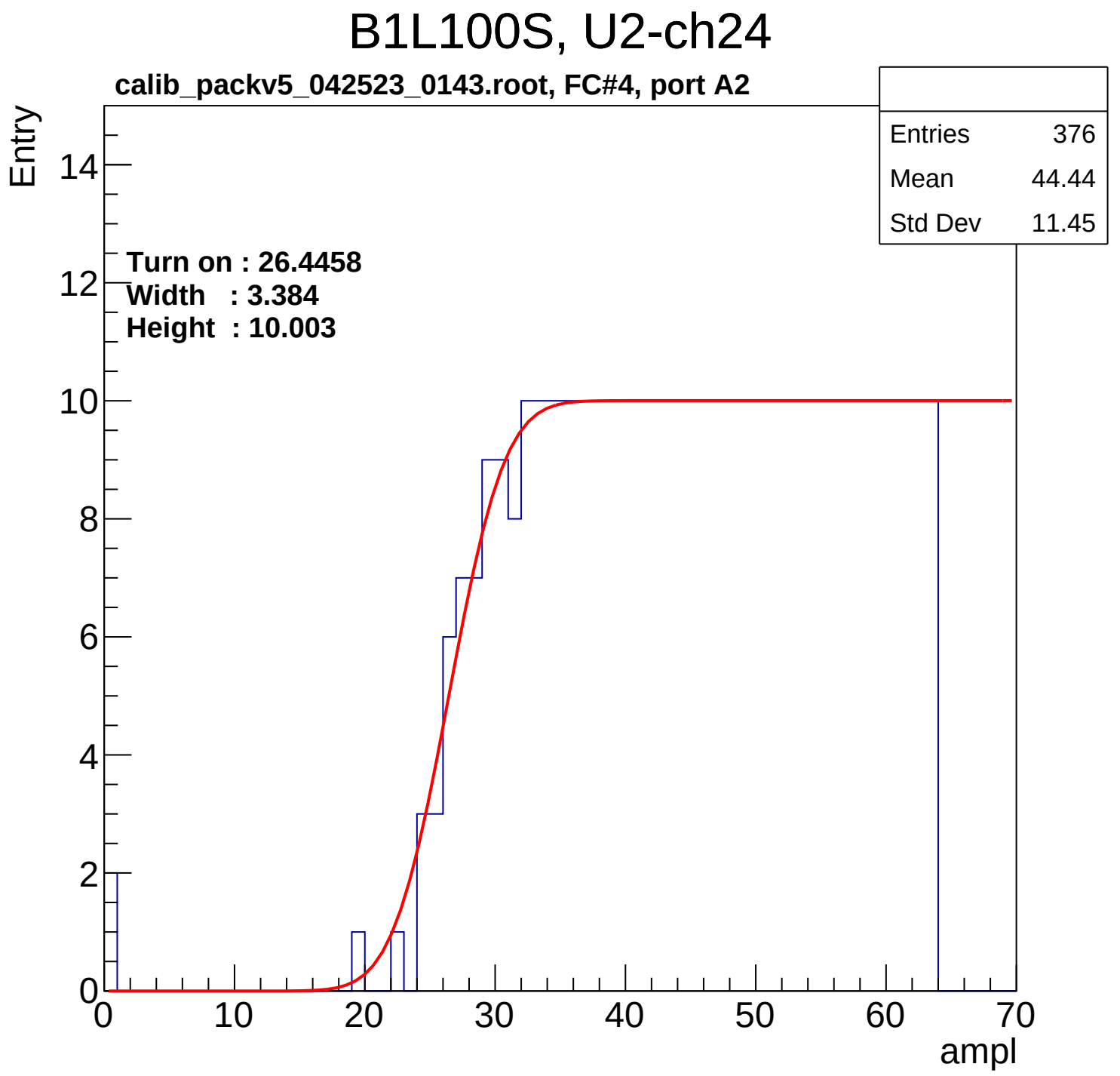
B1L100S, U2-ch24
calib_packv5_042523_0143.root, FC#4, port A2
Entries 376
Mean 44.44
Std Dev 11.45
Turn on : 26.4458
Width : 3.384
Height : 10.003
Entry
ampl
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8
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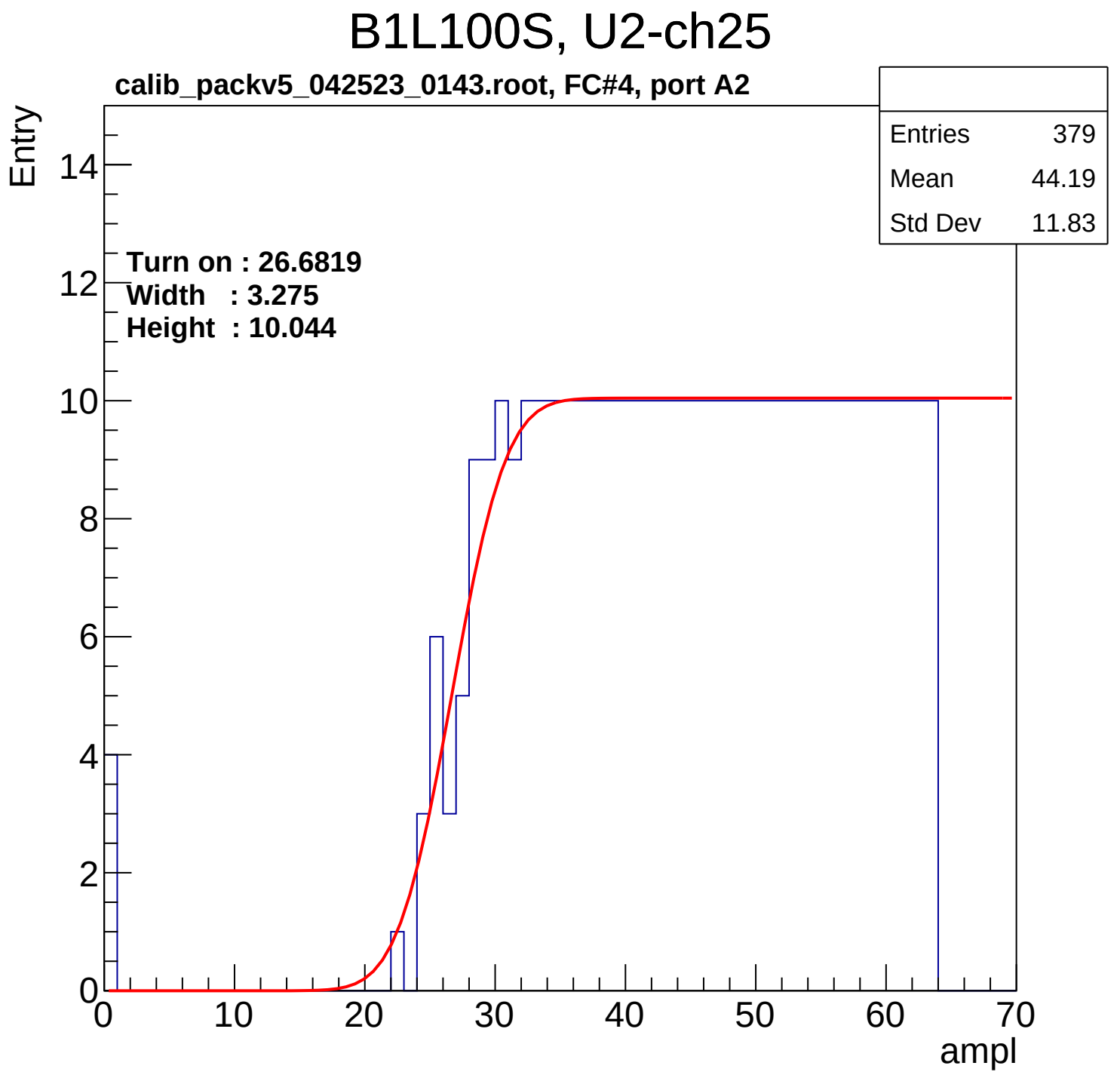
B1L100S, U2-ch25
calib_packv5_042523_0143.root, FC#4, port A2
Entries 379
Mean 44.19
Std Dev 11.83
Turn on : 26.6819
Width : 3.275
Height : 10.044
Entry
ampl
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6
8
10
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0
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60
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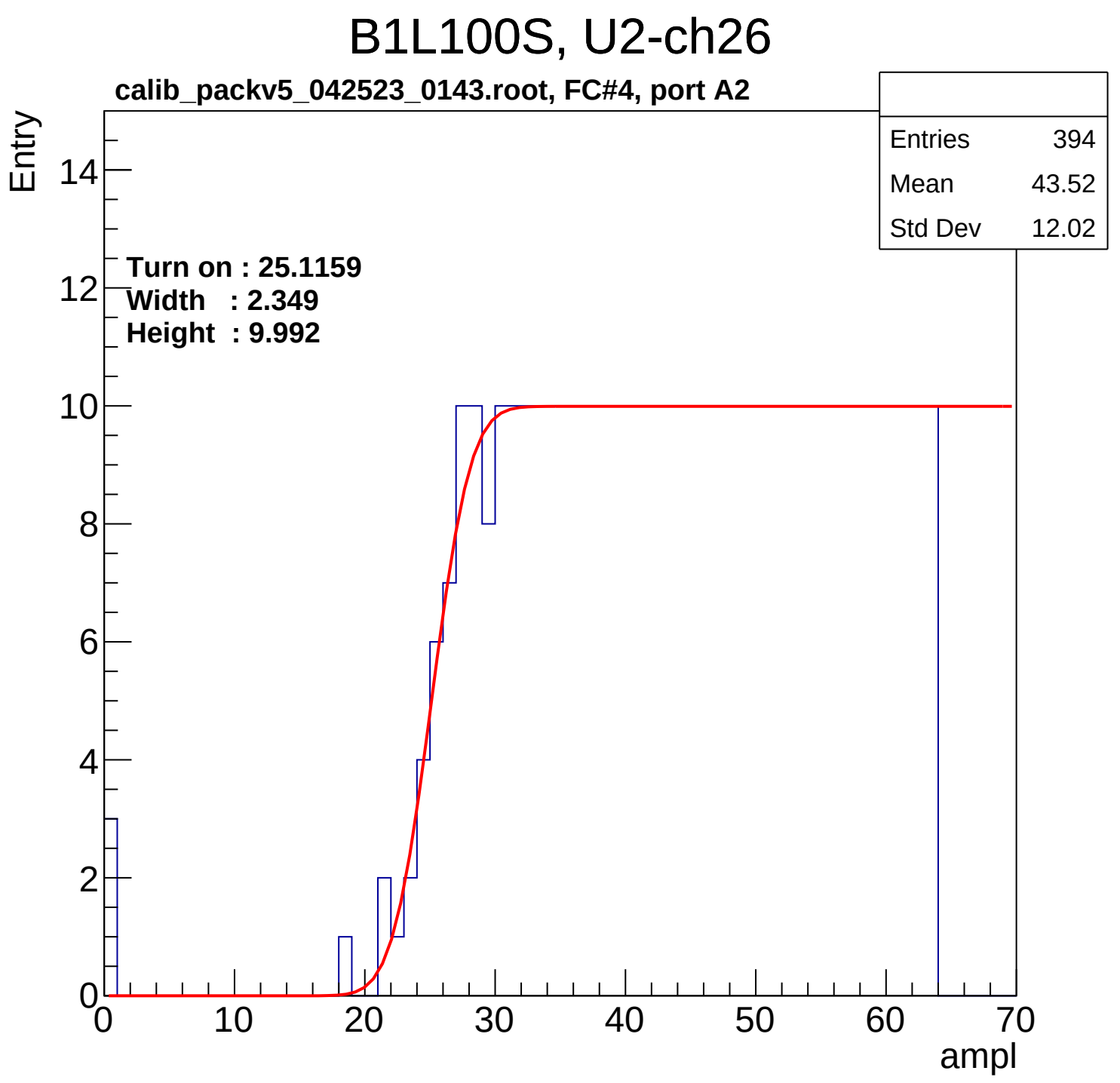
B1L100S, U2-ch26
calib_packv5_042523_0143.root, FC#4, port A2
Entries 394
Mean 43.52
Std Dev 12.02
Turn on : 25.1159
Width : 2.349
Height : 9.992
Entry
ampl
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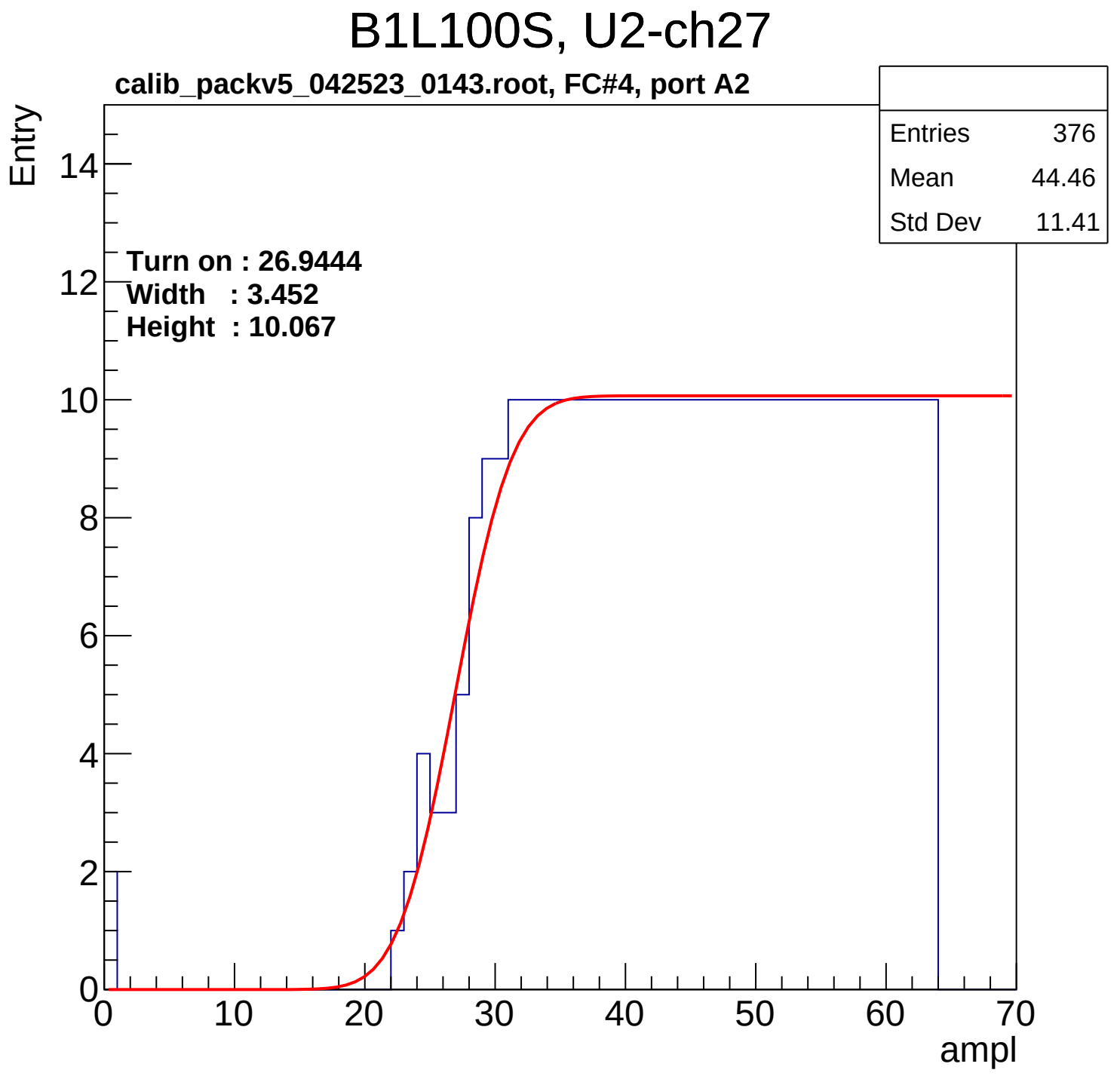
B1L100S, U2-ch27
calib_packv5_042523_0143.root, FC#4, port A2
Entries 376
Mean 44.46
Std Dev 11.41
Turn on : 26.9444
Width : 3.452
Height : 10.067
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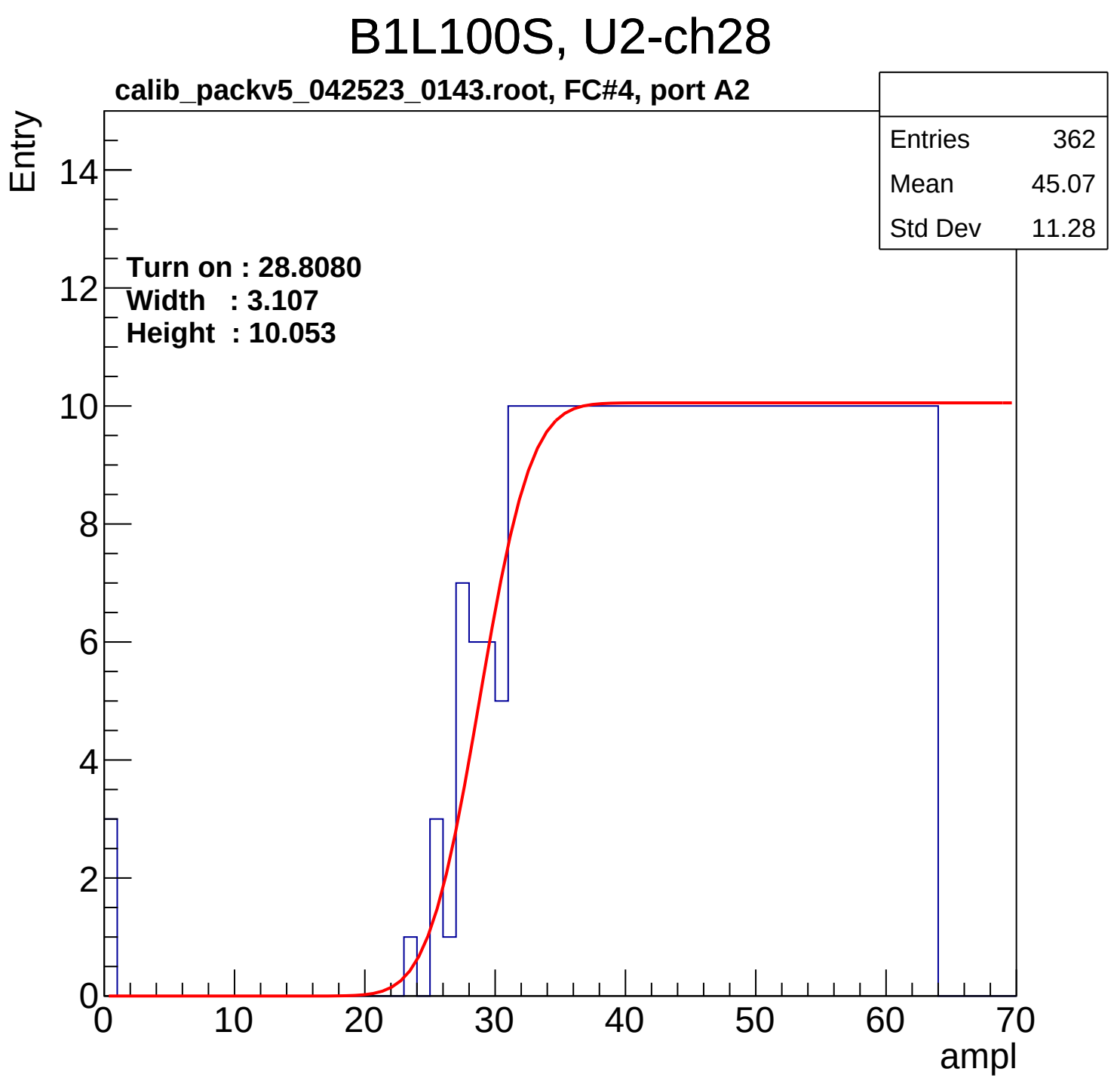
B1L100S, U2-ch28
calib_packv5_042523_0143.root, FC#4, port A2
Entries 362
Mean 45.07
Std Dev 11.28
Turn on : 28.8080
Width : 3.107
Height : 10.053
Entry
ampl
0
2
4
6
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12
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10
20
30
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50
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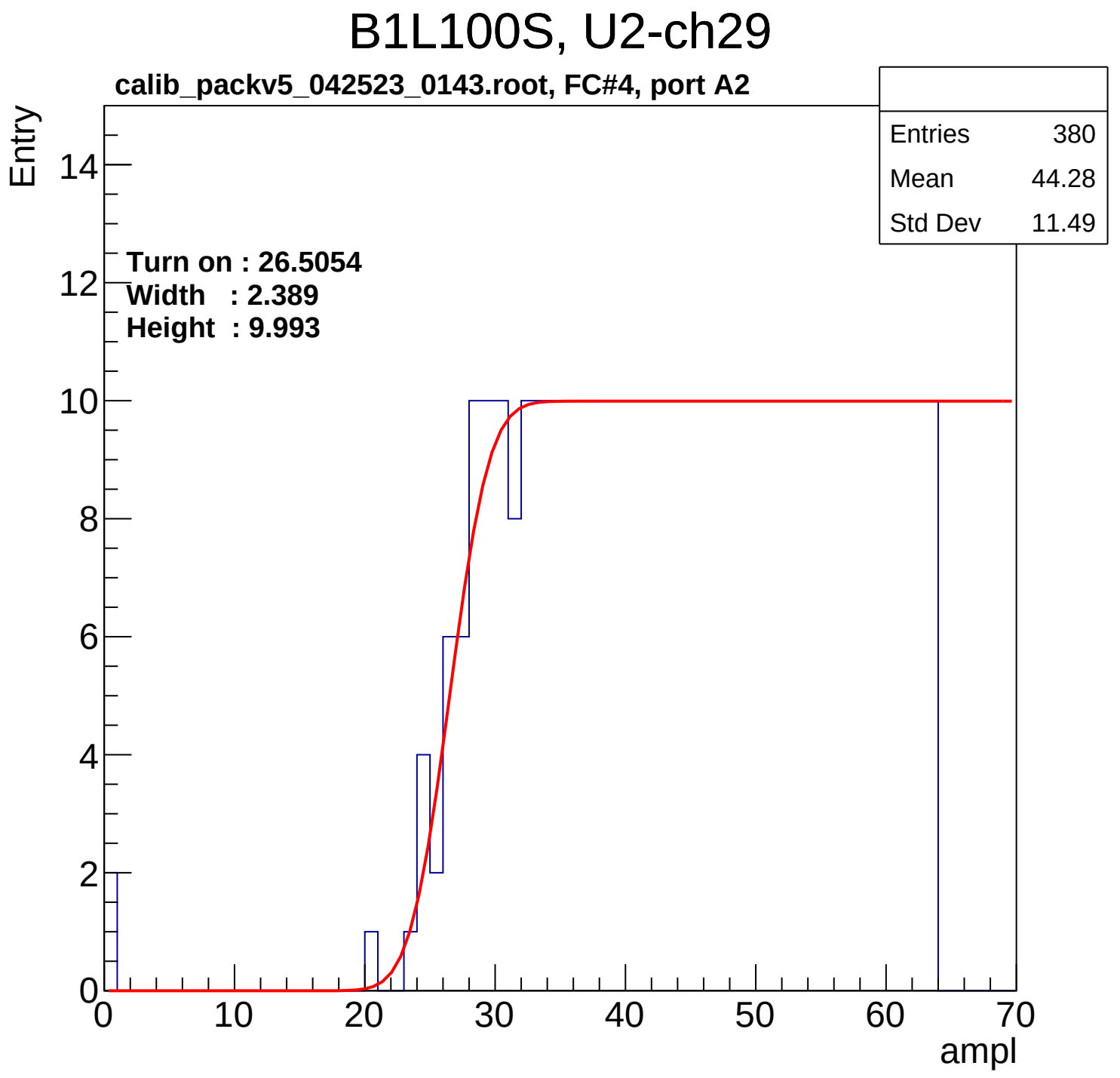
B1L100S, U2-ch29
calib_packv5_042523_0143.root, FC#4, port A2
Entries 380
Mean 44.28
Std Dev 11.49
Turn on : 26.5054
Width : 2.389
Height : 9.993
Entry
ampl
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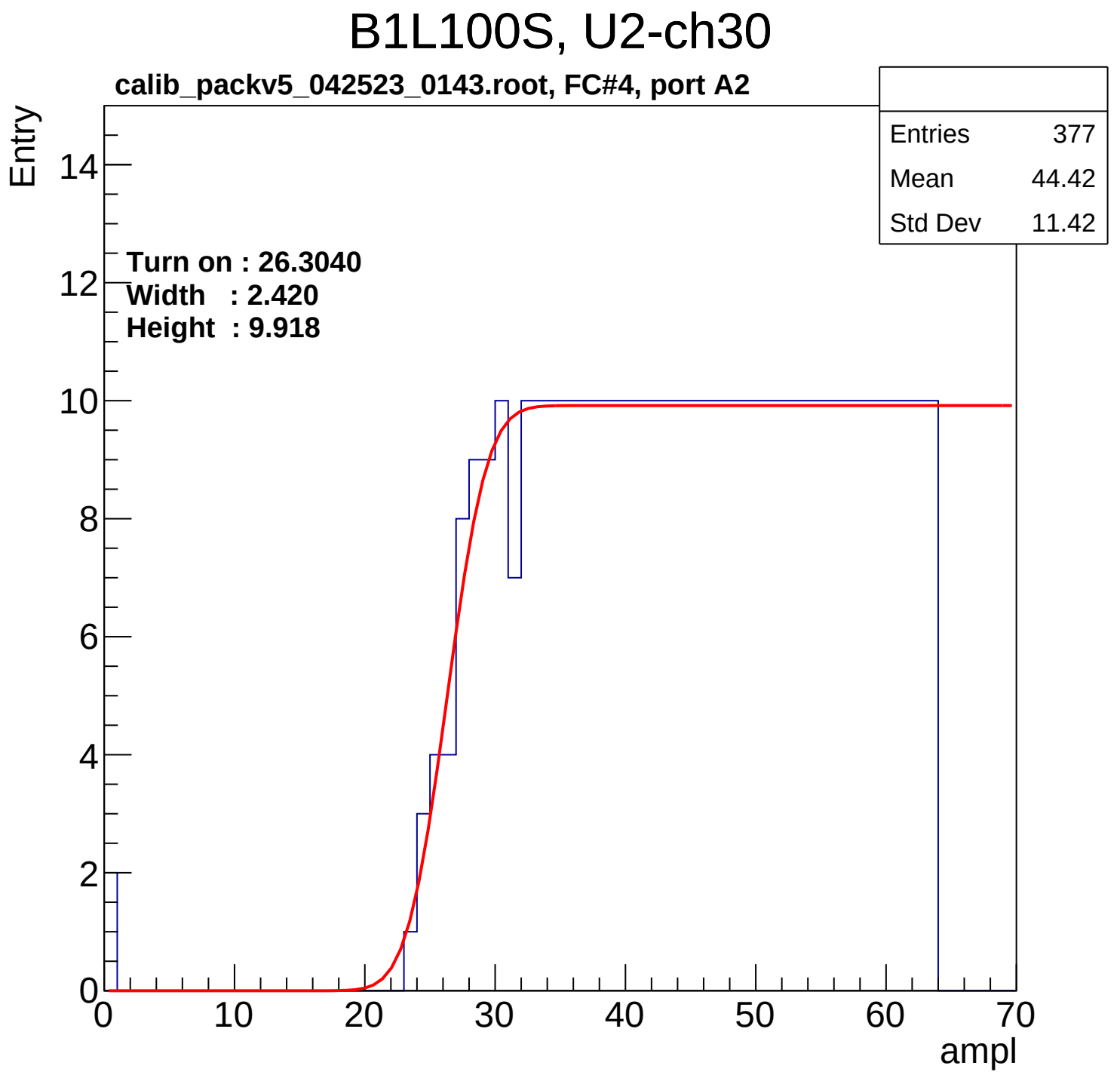
B1L100S, U2-ch30
calib_packv5_042523_0143.root, FC#4, port A2
Entries 377
Mean 44.42
Std Dev 11.42
Turn on : 26.3040
Width : 2.420
Height : 9.918
Entry
ampl
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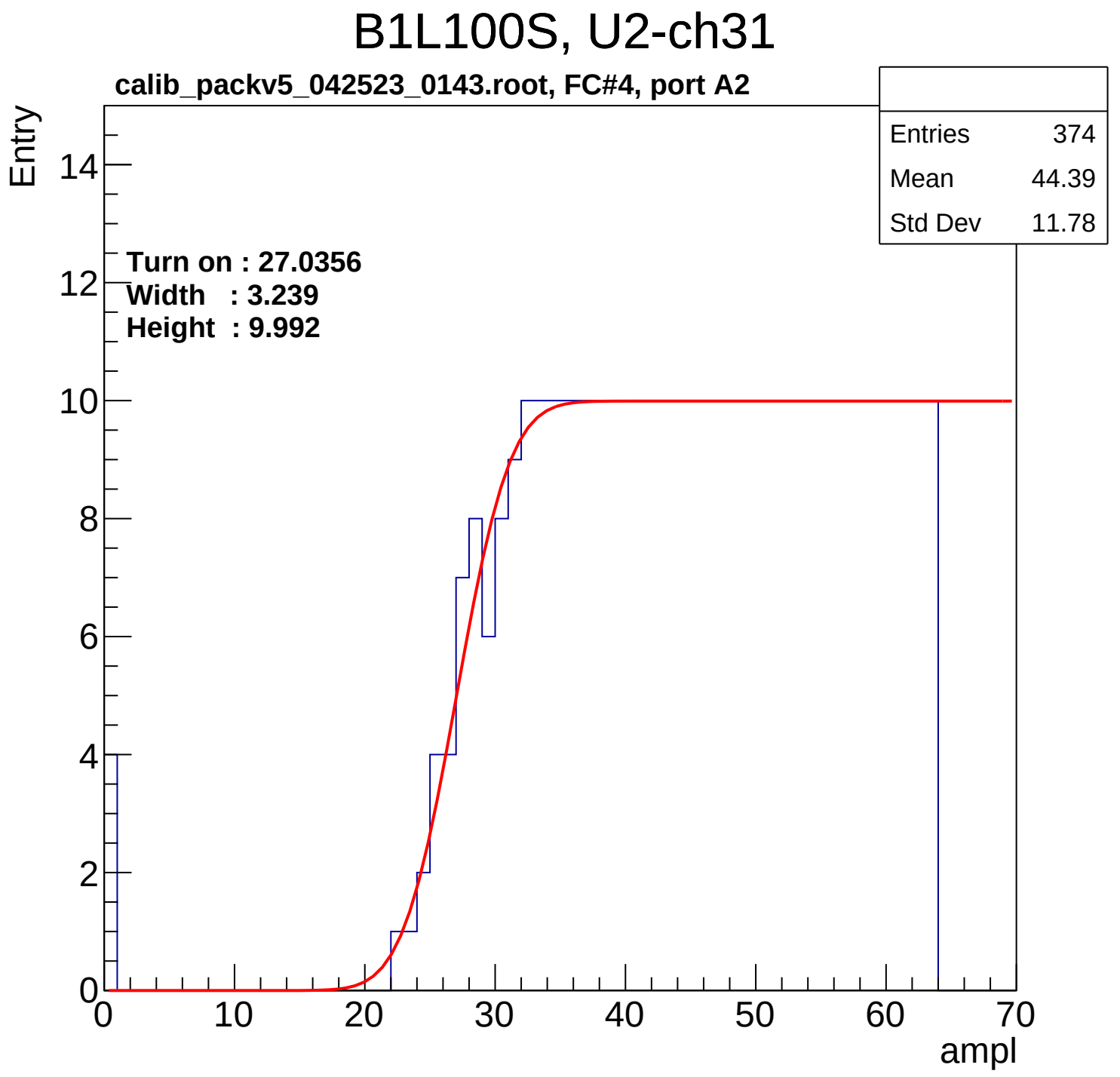
B1L100S, U2-ch31
calib_packv5_042523_0143.root, FC#4, port A2
Entries 374
Mean 44.39
Std Dev 11.78
Turn on : 27.0356
Width : 3.239
Height : 9.992
Entry
ampl
0
2
4
6
8
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0
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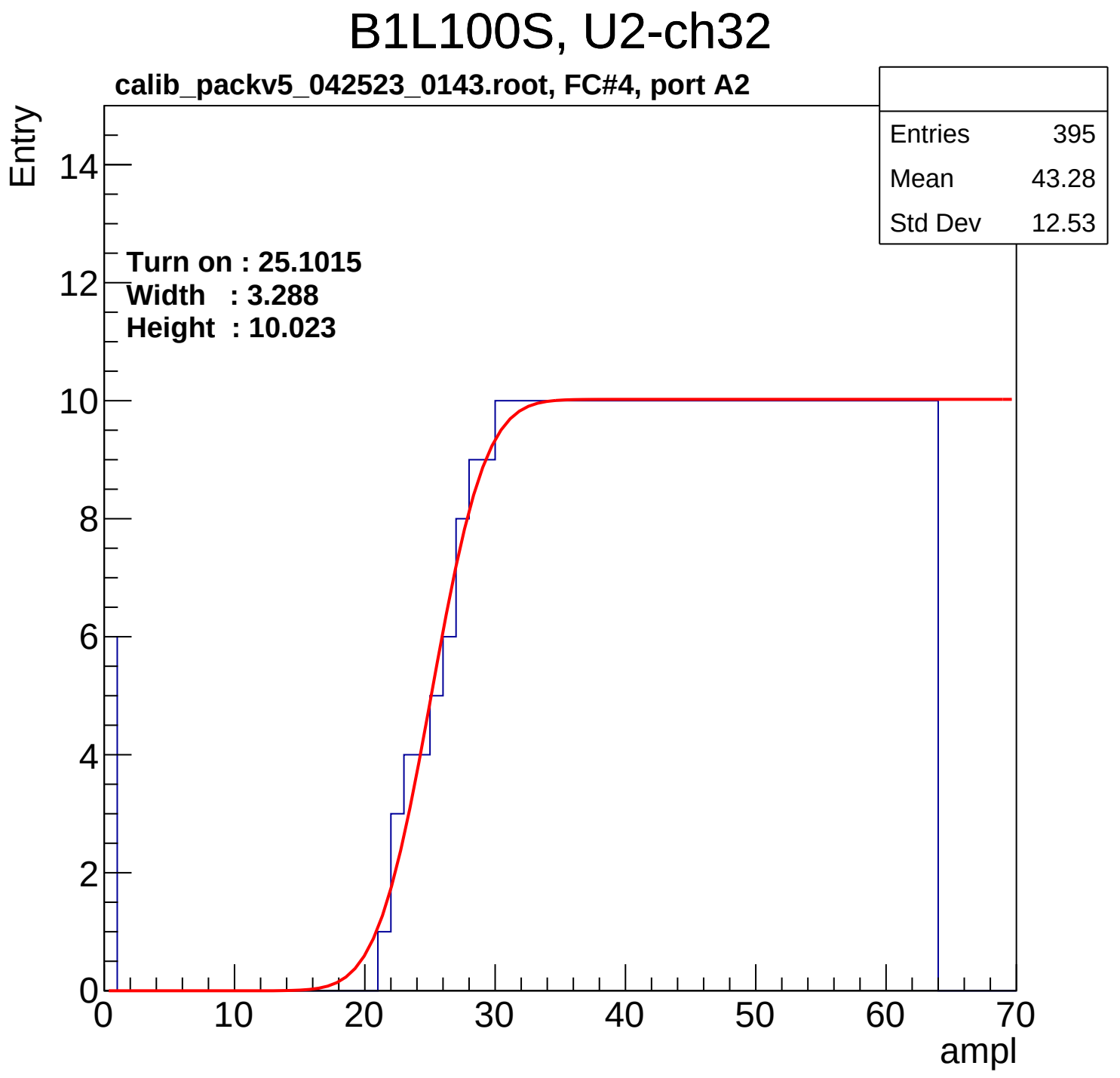
B1L100S, U2-ch32
calib_packv5_042523_0143.root, FC#4, port A2
Entries 395
Mean 43.28
Std Dev 12.53
Turn on : 25.1015
Width : 3.288
Height : 10.023
Entry
ampl
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6
8
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12
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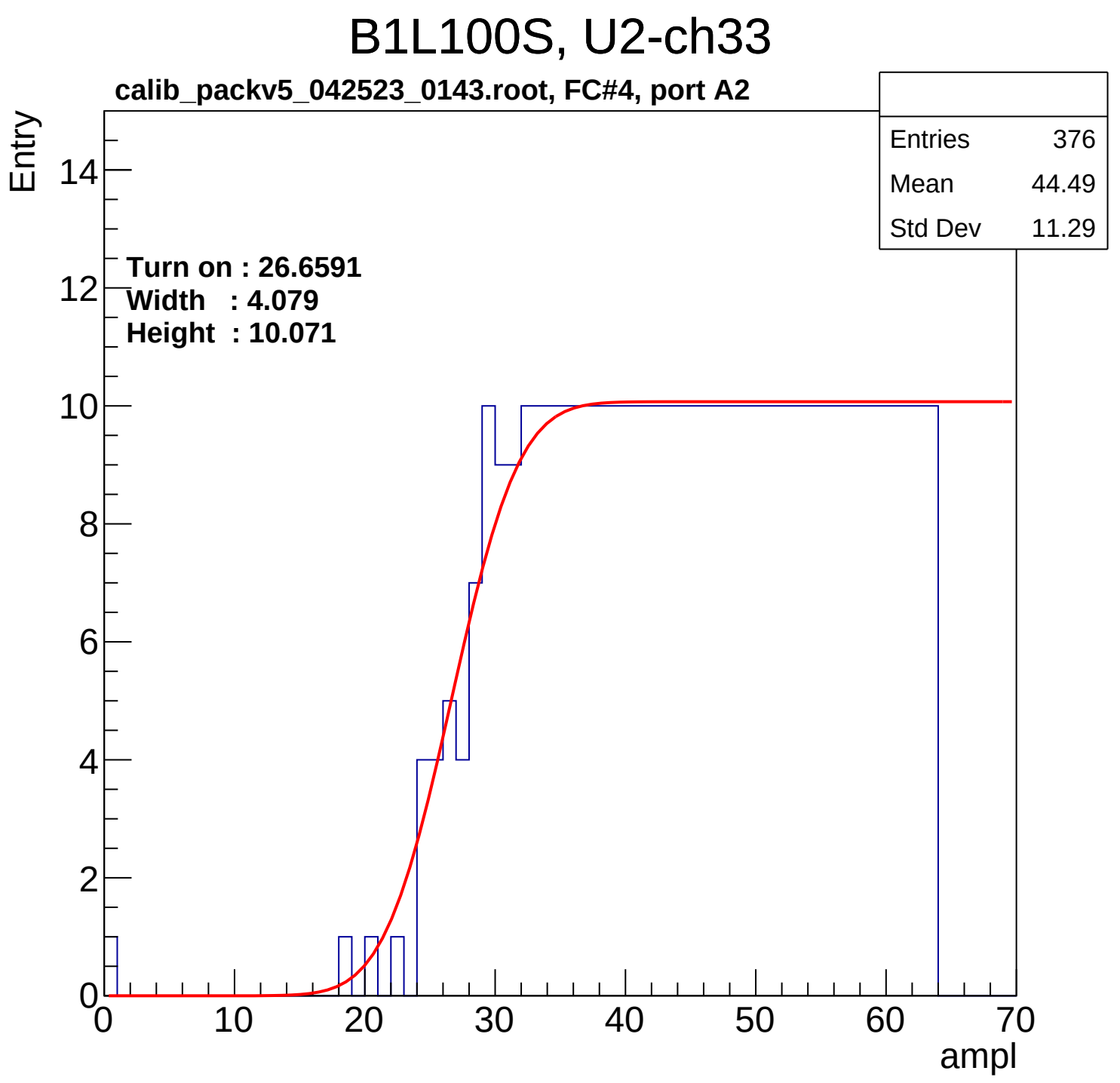
B1L100S, U2-ch33
calib_packv5_042523_0143.root, FC#4, port A2
Entries 376
Mean 44.49
Std Dev 11.29
Turn on : 26.6591
Width : 4.079
Height : 10.071
Entry
ampl
0
2
4
6
8
10
12
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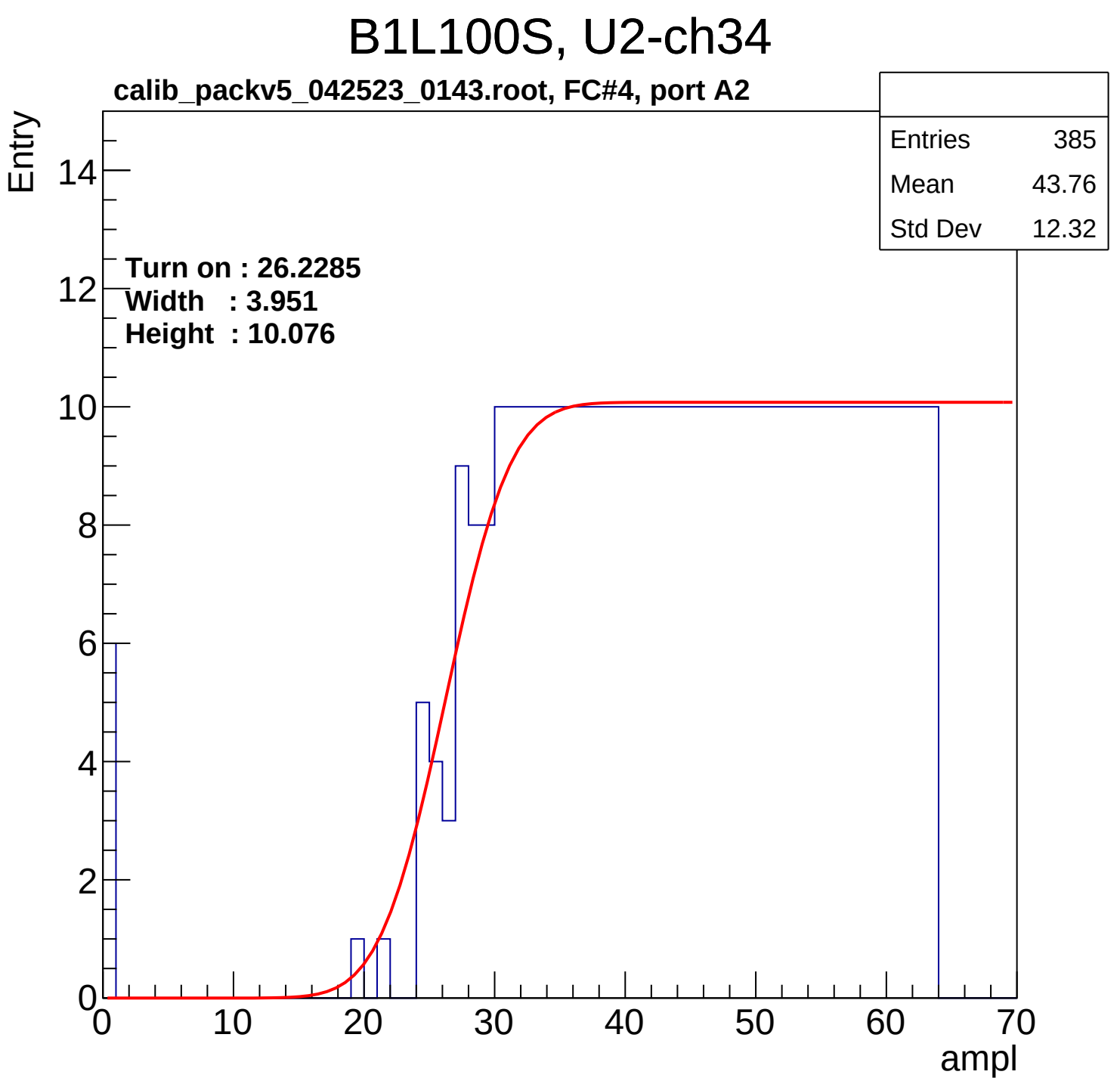
B1L100S, U2-ch34
calib_packv5_042523_0143.root, FC#4, port A2
Entries 385
Mean 43.76
Std Dev 12.32
Turn on : 26.2285
Width : 3.951
Height : 10.076
Entry
ampl
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2
4
6
8
10
12
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0
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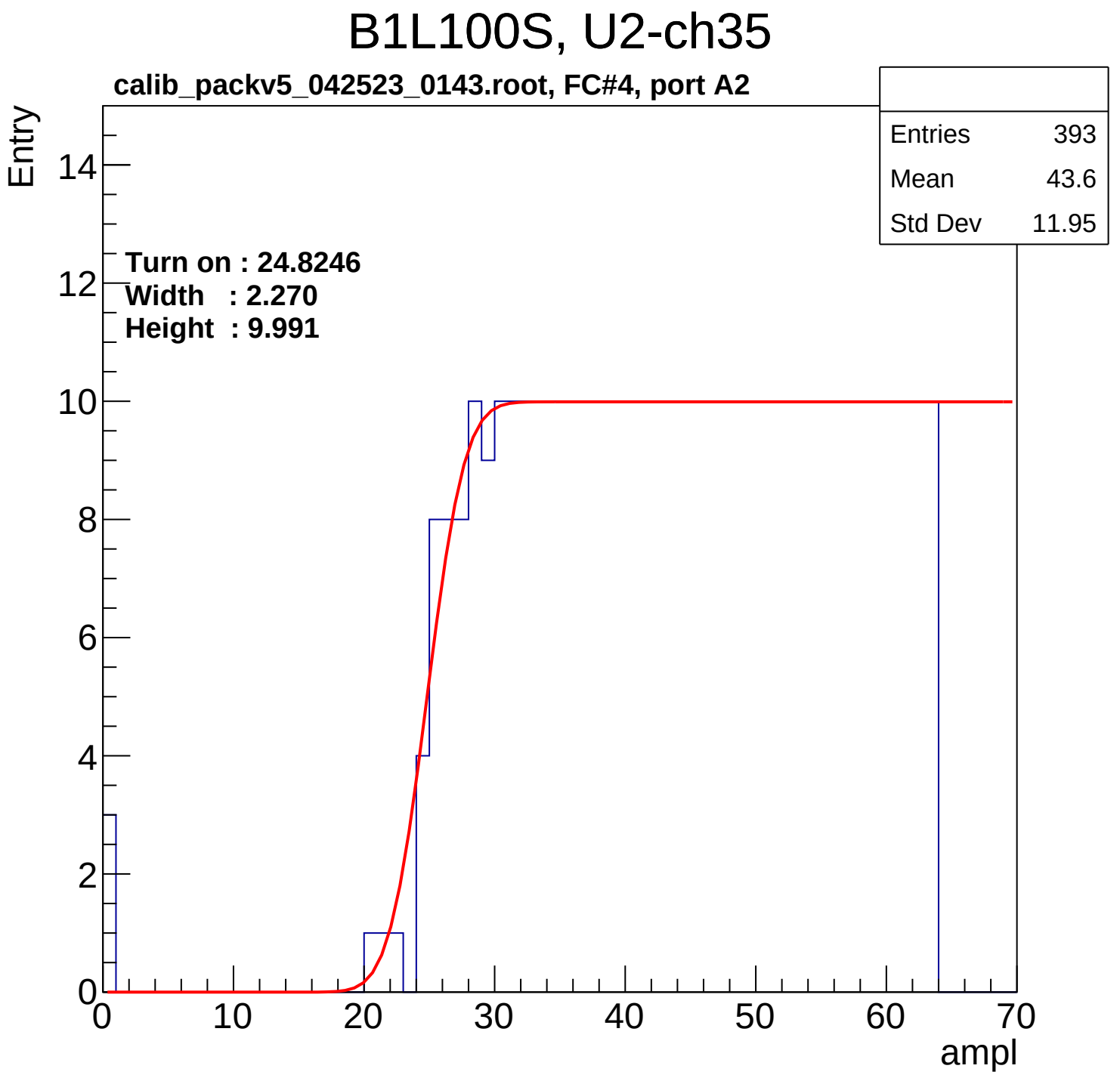
B1L100S, U2-ch35
calib_packv5_042523_0143.root, FC#4, port A2
Entries 393
Mean 43.6
Std Dev 11.95
Turn on : 24.8246
Width : 2.270
Height : 9.991
Entry
ampl
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2
4
6
8
10
12
14
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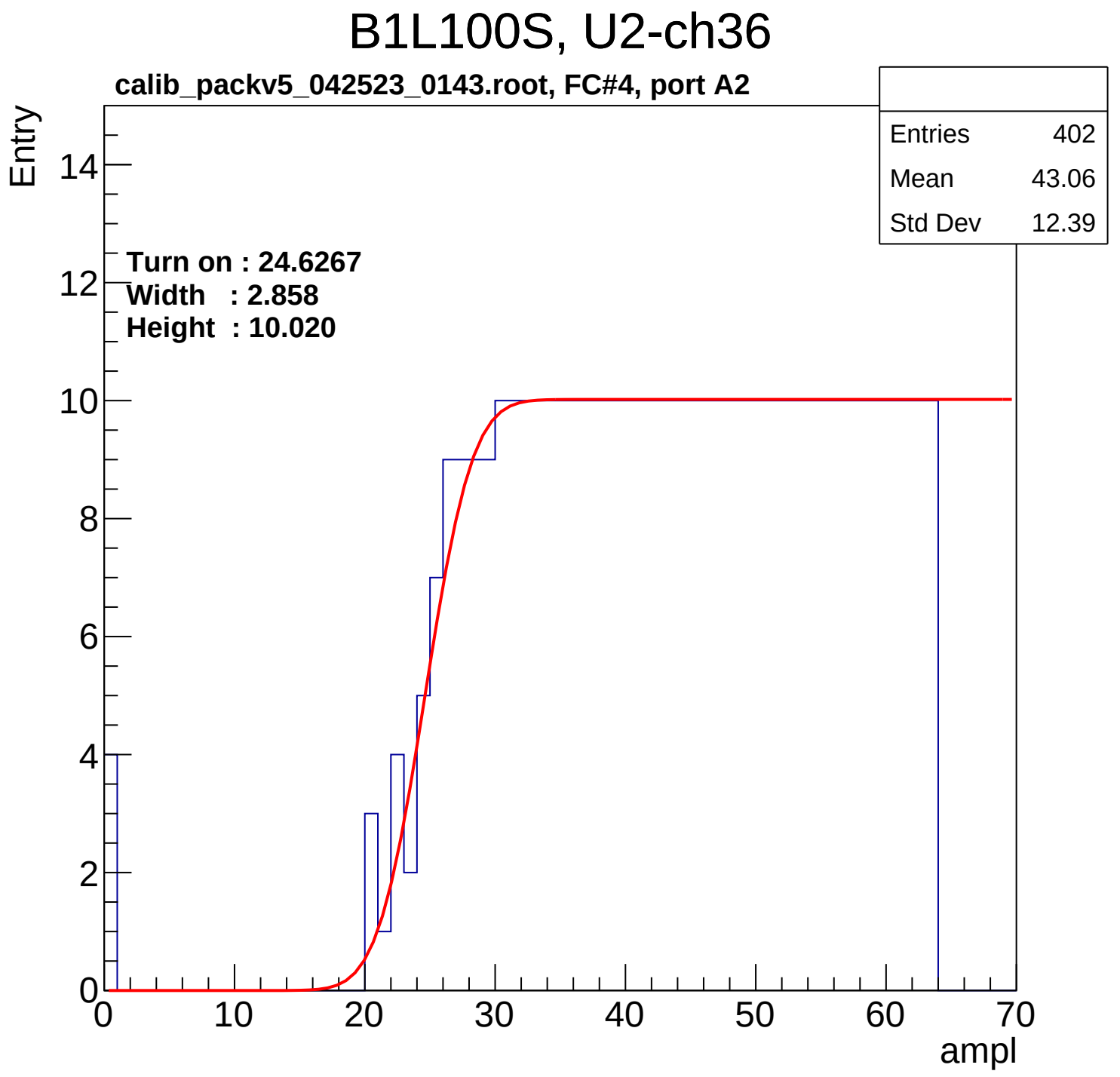
B1L100S, U2-ch36
calib_packv5_042523_0143.root, FC#4, port A2
Entries 402
Mean 43.06
Std Dev 12.39
Turn on : 24.6267
Width : 2.858
Height : 10.020
Entry
ampl
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2
4
6
8
10
12
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0
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20
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40
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60
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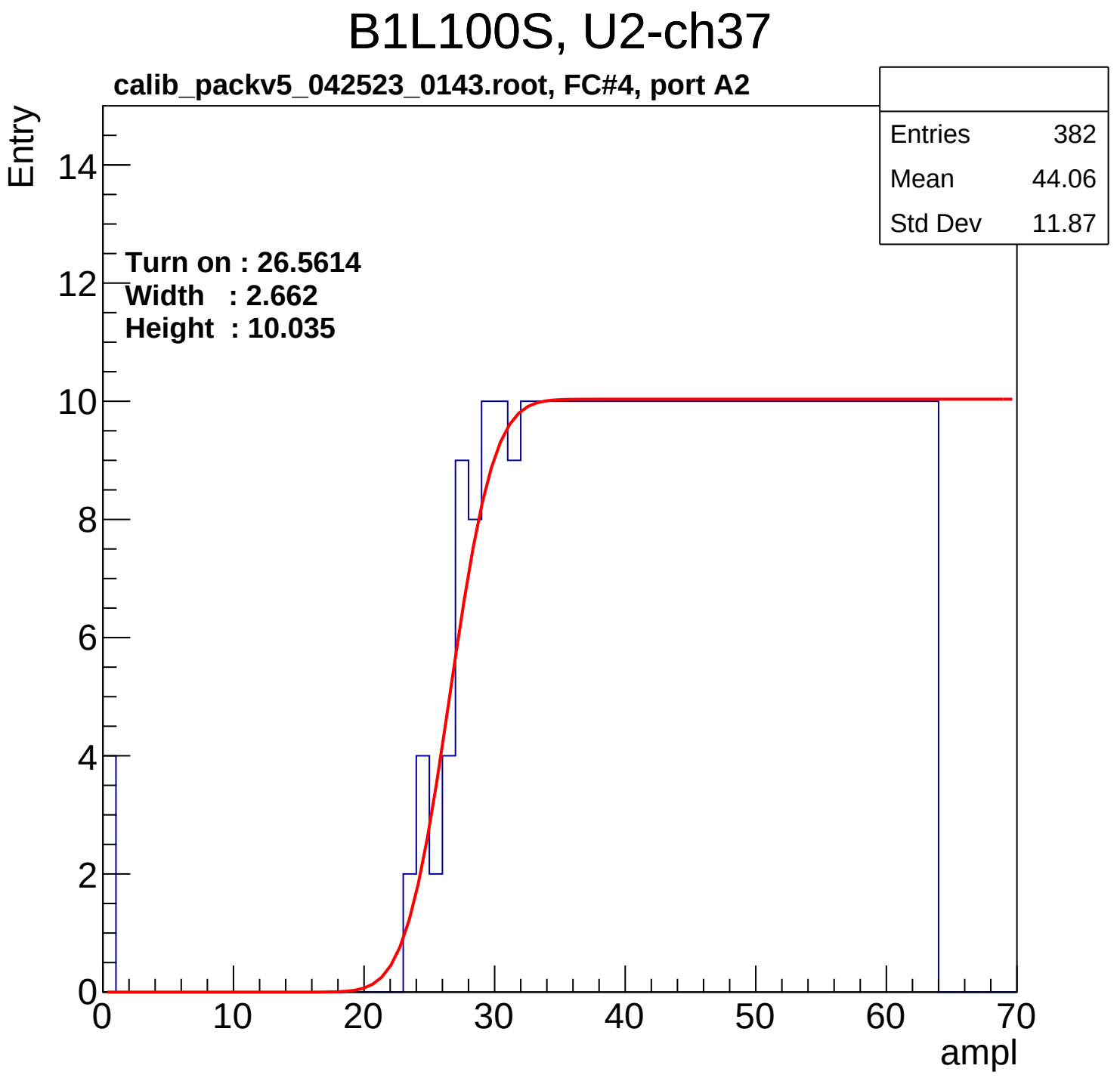
B1L100S, U2-ch37
calib_packv5_042523_0143.root, FC#4, port A2
Entries 382
Mean 44.06
Std Dev 11.87
Turn on : 26.5614
Width : 2.662
Height : 10.035
Entry
ampl
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6
8
10
12
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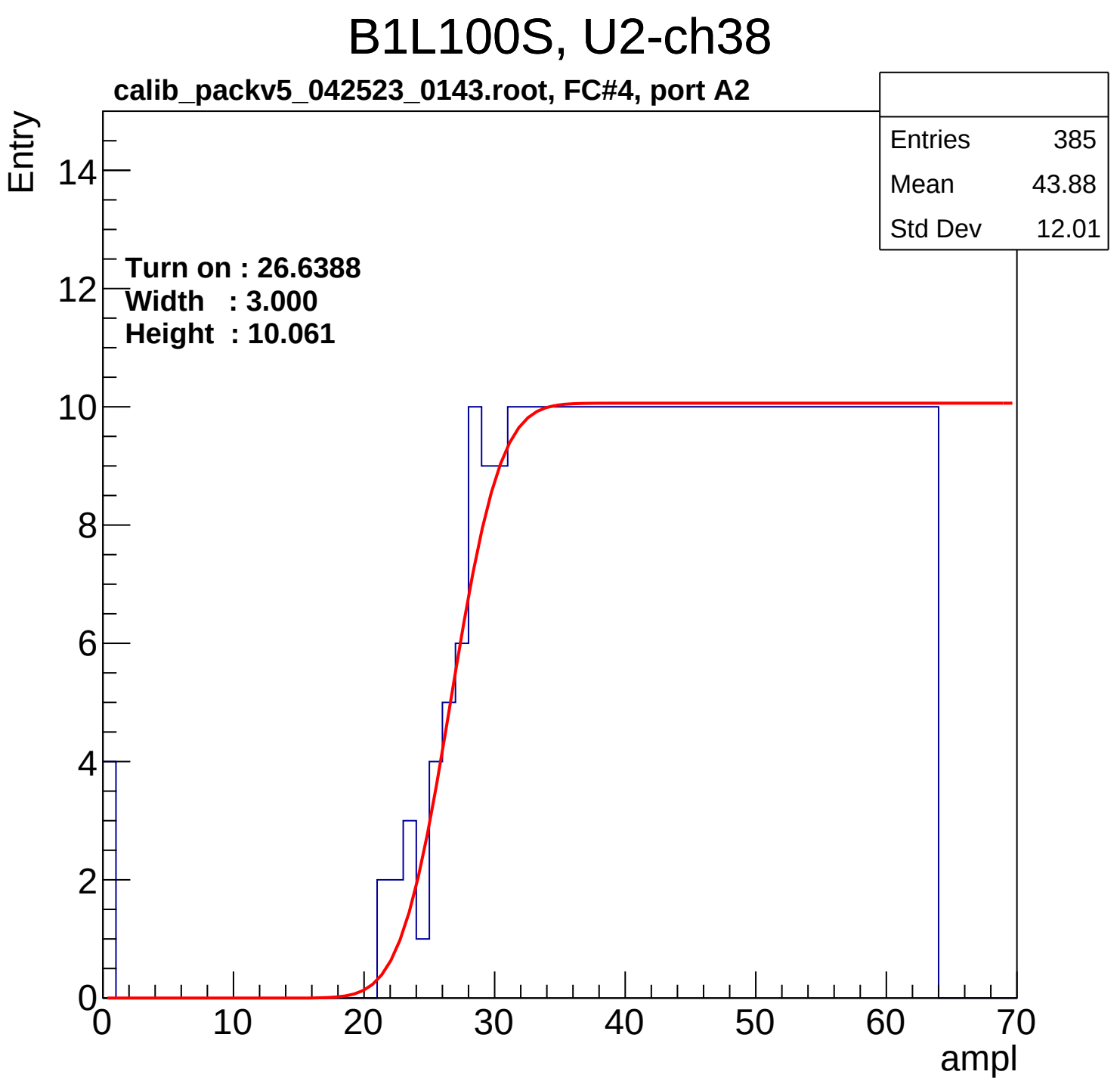
B1L100S, U2-ch38
calib_packv5_042523_0143.root, FC#4, port A2
Entries 385
Mean 43.88
Std Dev 12.01
Turn on : 26.6388
Width : 3.000
Height : 10.061
Entry
ampl
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2
4
6
8
10
12
14
0
10
20
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60
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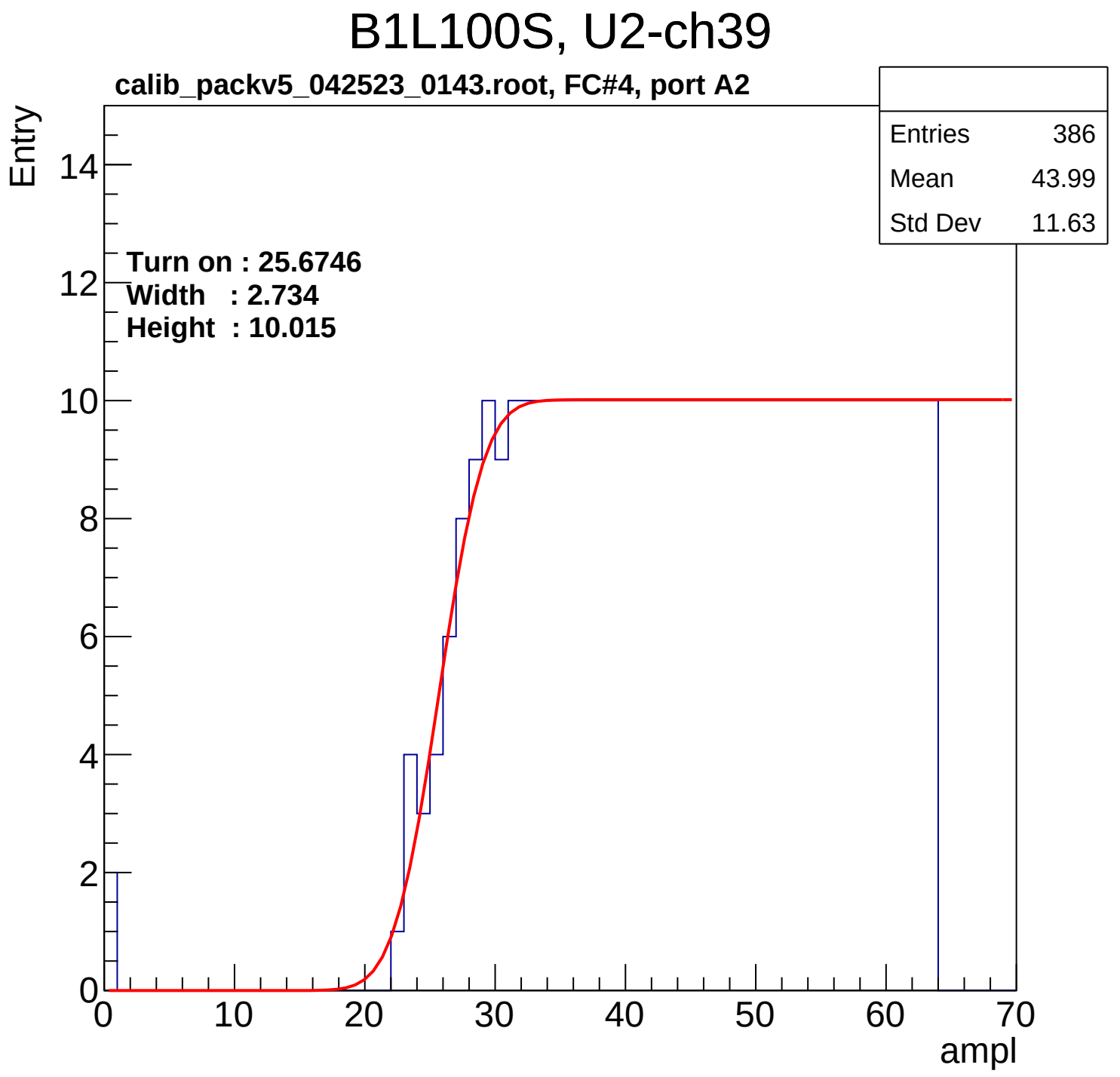
B1L100S, U2-ch39
calib_packv5_042523_0143.root, FC#4, port A2
Entries 386
Mean 43.99
Std Dev 11.63
Turn on : 25.6746
Width : 2.734
Height : 10.015
Entry
ampl
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2
4
6
8
10
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0
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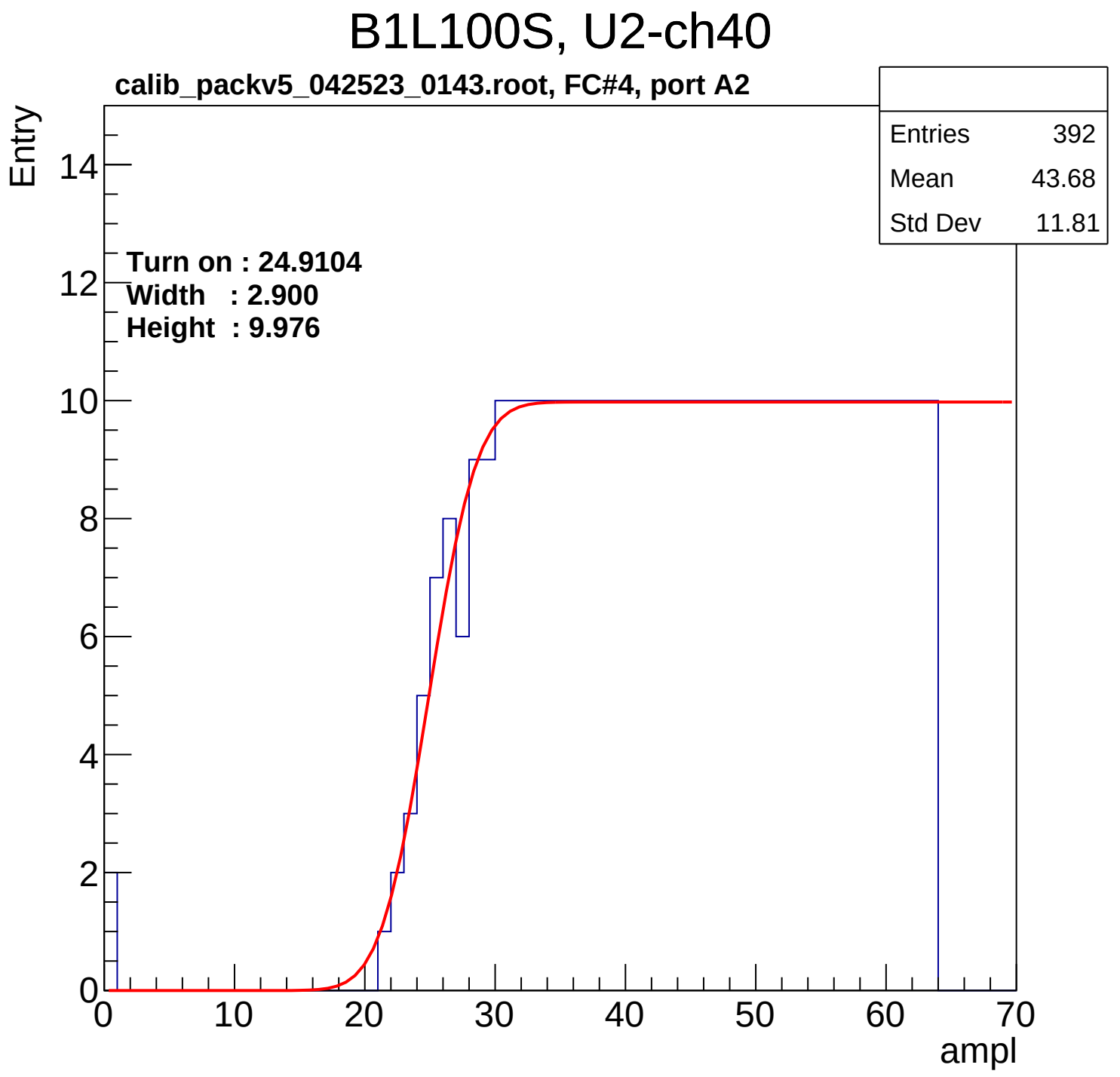
B1L100S, U2-ch40
calib_packv5_042523_0143.root, FC#4, port A2
Entries 392
Mean 43.68
Std Dev 11.81
Turn on : 24.9104
Width : 2.900
Height : 9.976
Entry
ampl
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2
4
6
8
10
12
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0
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20
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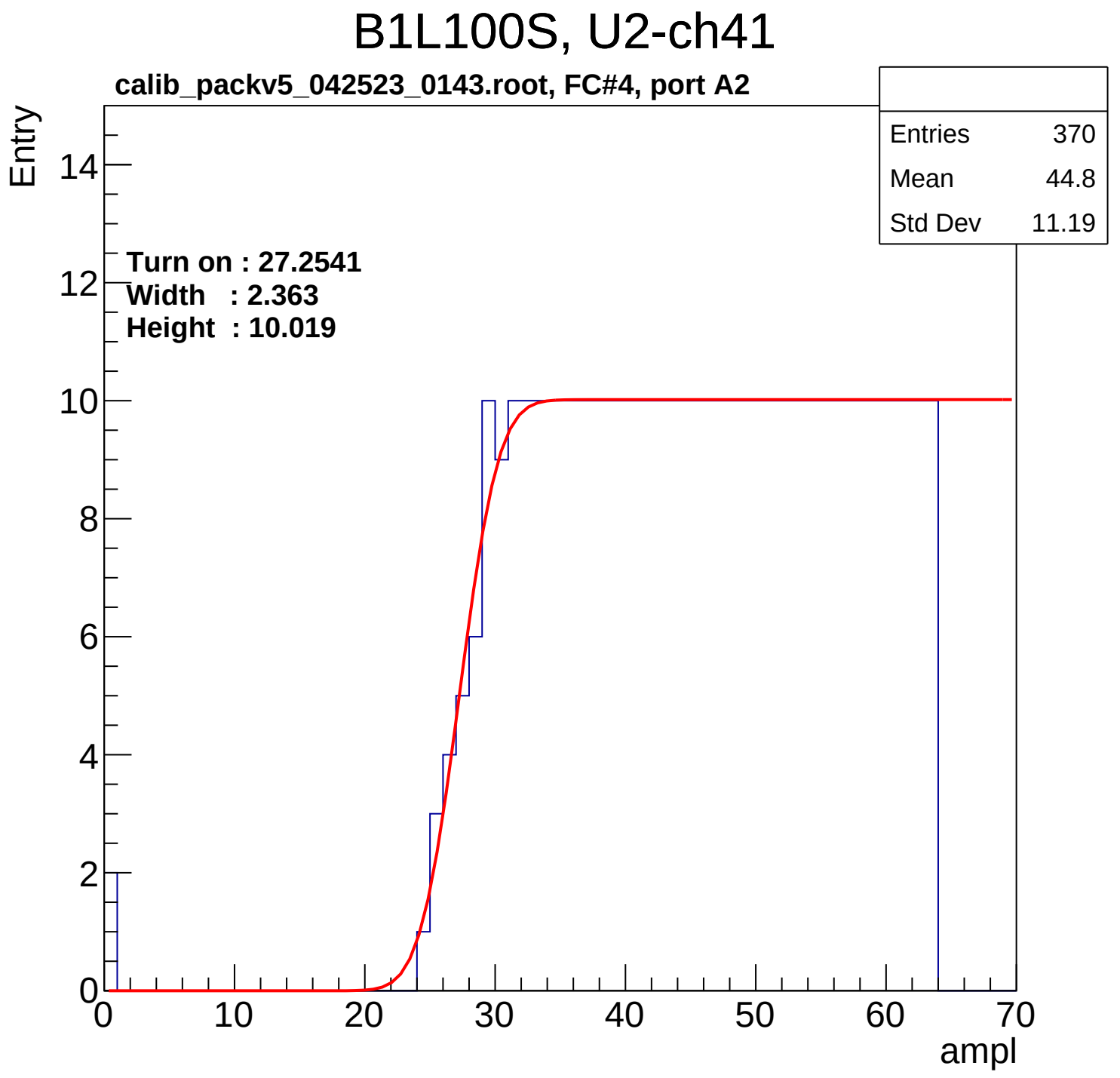
B1L100S, U2-ch41
calib_packv5_042523_0143.root, FC#4, port A2
Entries 370
Mean 44.8
Std Dev 11.19
Turn on : 27.2541
Width : 2.363
Height : 10.019
Entry
ampl
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8
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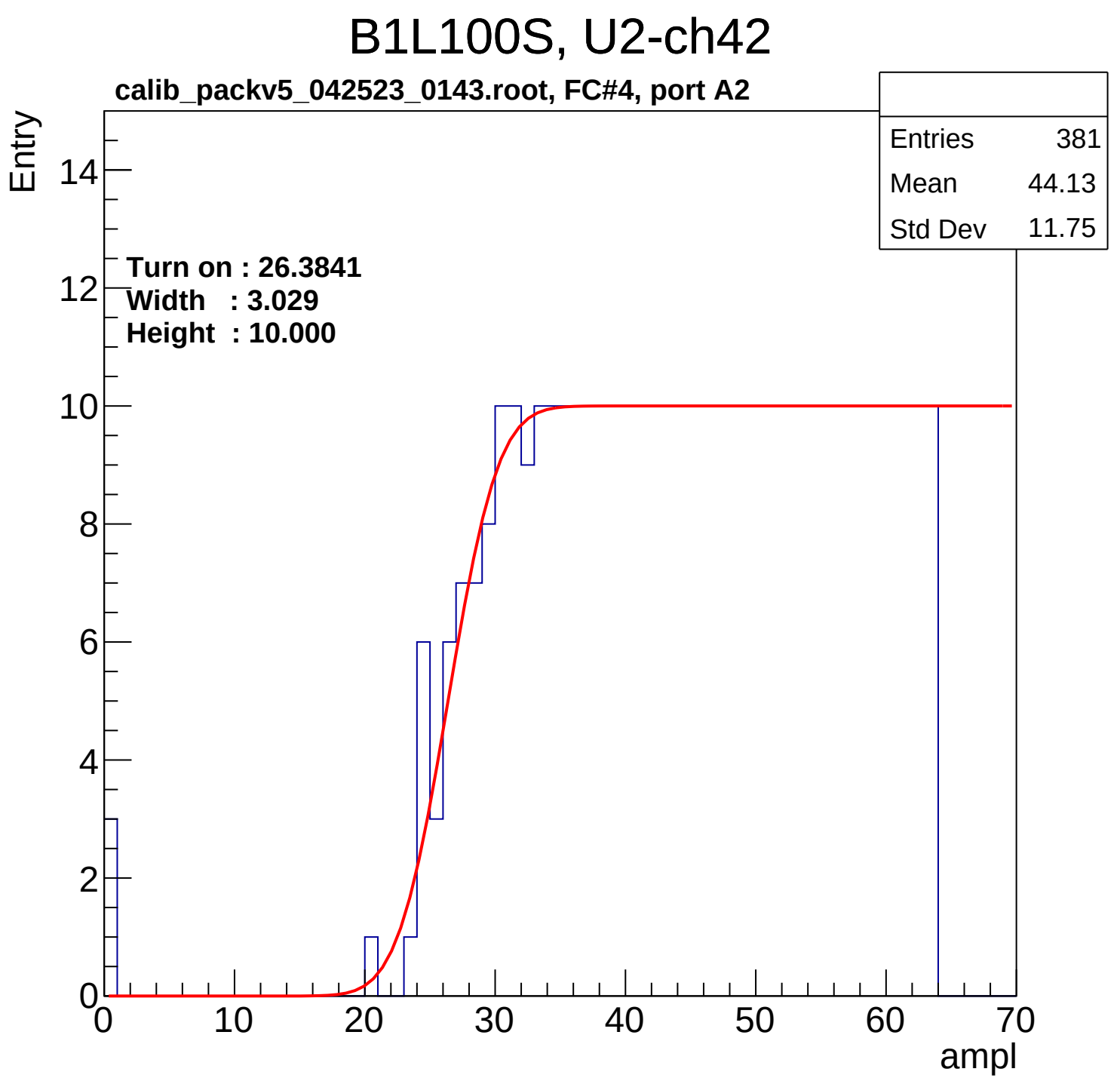
B1L100S, U2-ch42
calib_packv5_042523_0143.root, FC#4, port A2
Entries 381
Mean 44.13
Std Dev 11.75
Turn on : 26.3841
Width : 3.029
Height : 10.000
Entry
ampl
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4
6
8
10
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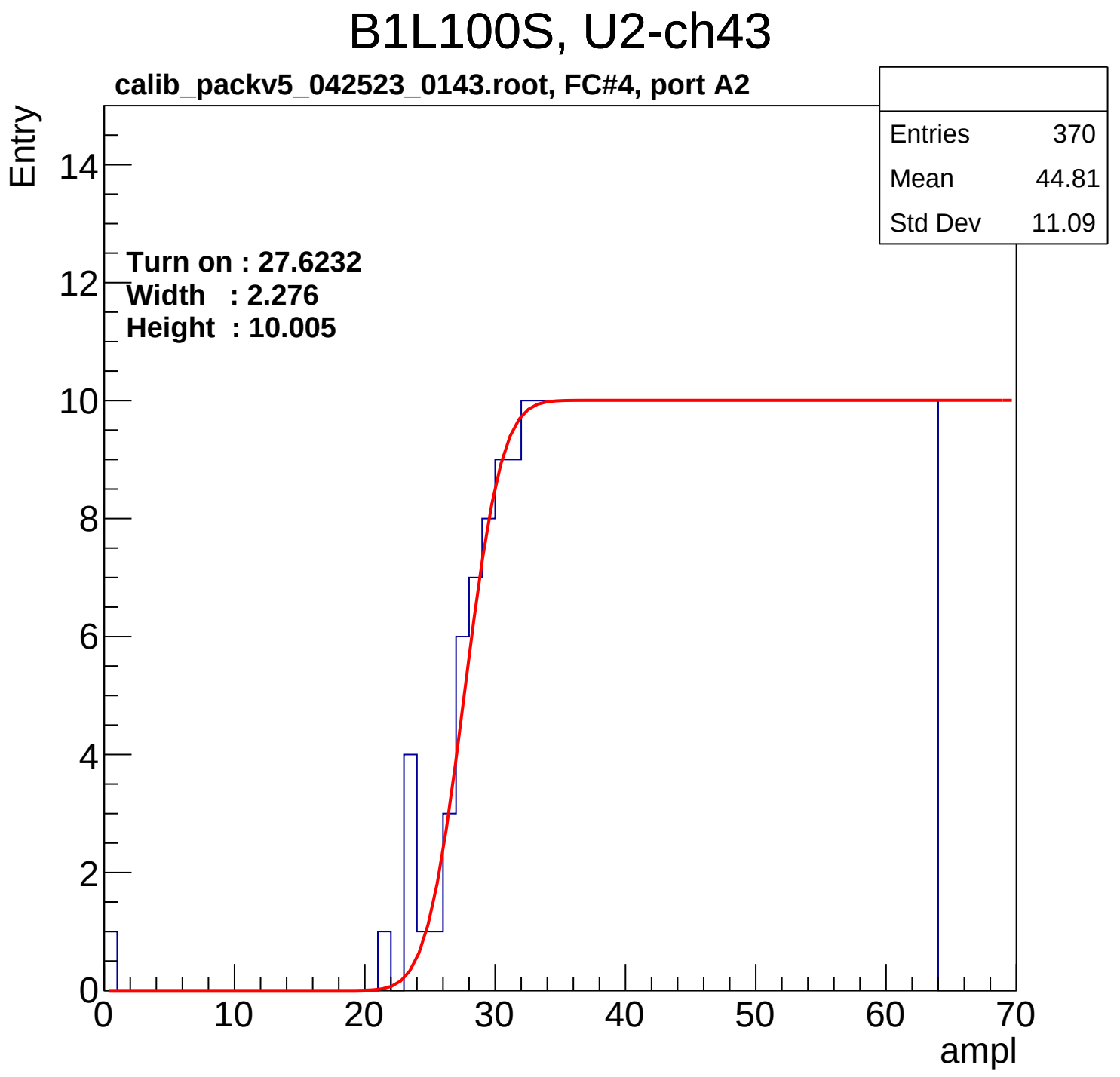
B1L100S, U2-ch43
calib_packv5_042523_0143.root, FC#4, port A2
Entries 370
Mean 44.81
Std Dev 11.09
Turn on : 27.6232
Width : 2.276
Height : 10.005
Entry
ampl
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6
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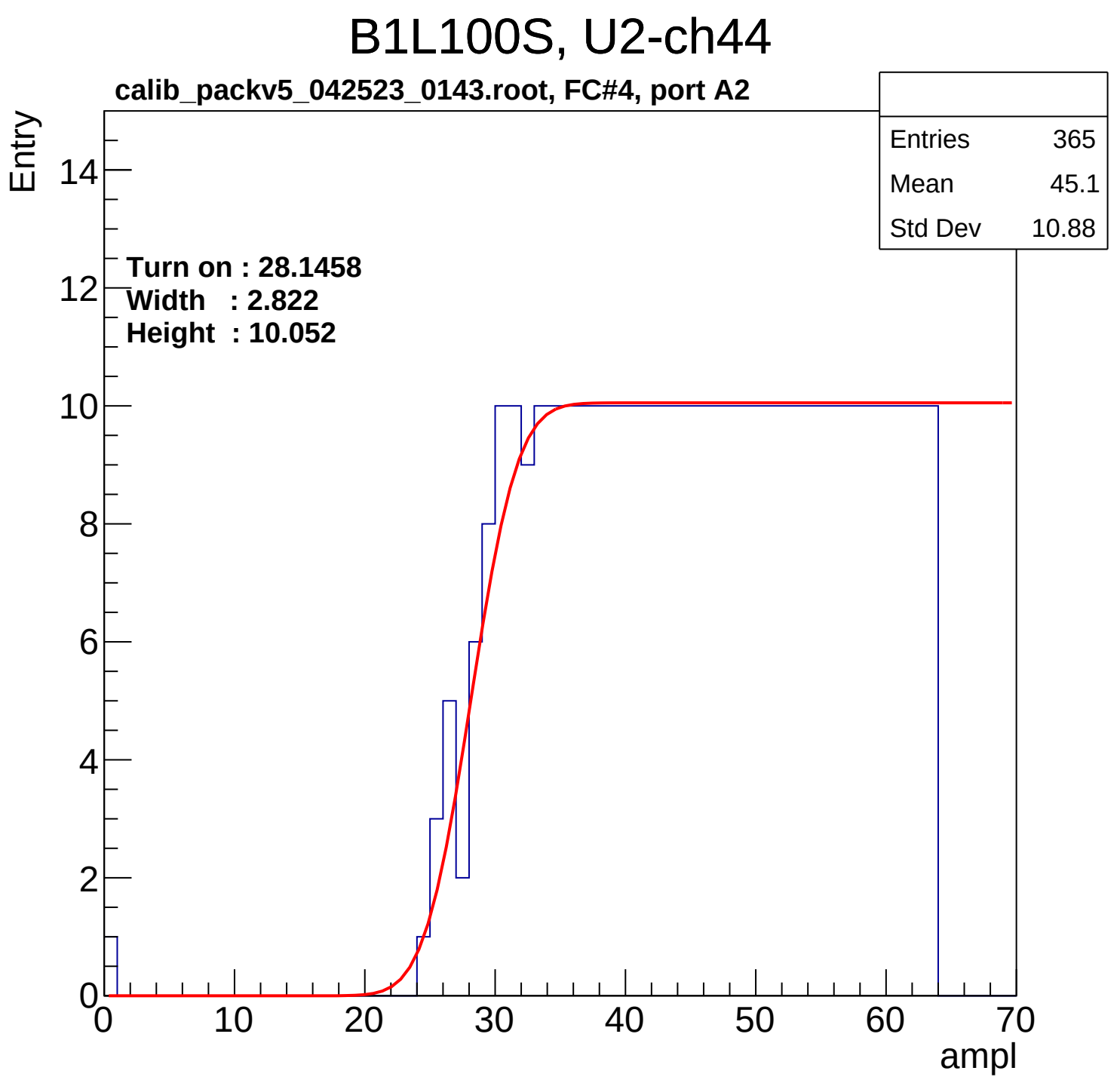
B1L100S, U2-ch44
calib_packv5_042523_0143.root, FC#4, port A2
Entries 365
Mean 45.1
Std Dev 10.88
Turn on : 28.1458
Width : 2.822
Height : 10.052
Entry
ampl
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2
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8
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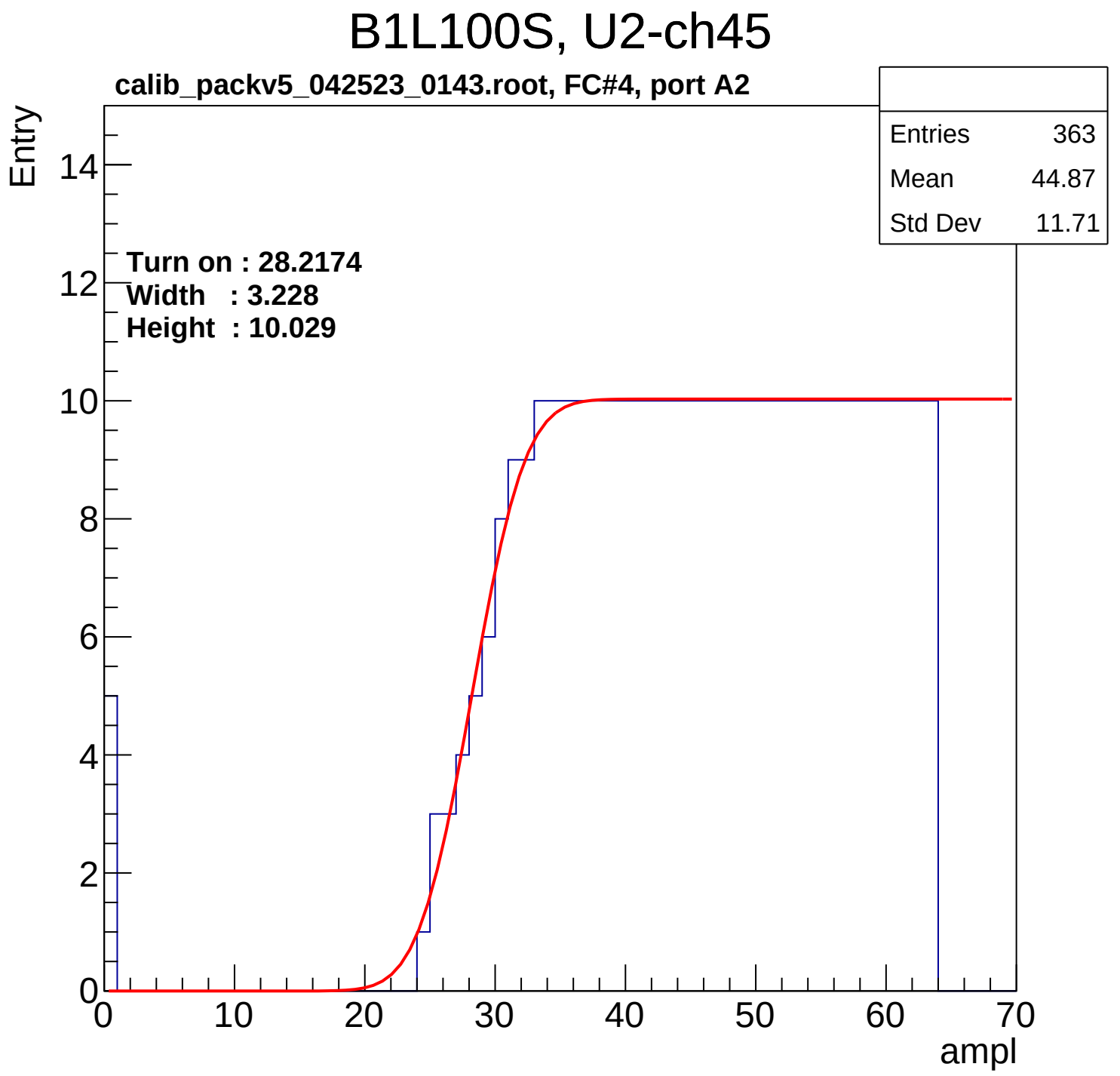
B1L100S, U2-ch45
calib_packv5_042523_0143.root, FC#4, port A2
Entries 363
Mean 44.87
Std Dev 11.71
Turn on : 28.2174
Width : 3.228
Height : 10.029
Entry
ampl
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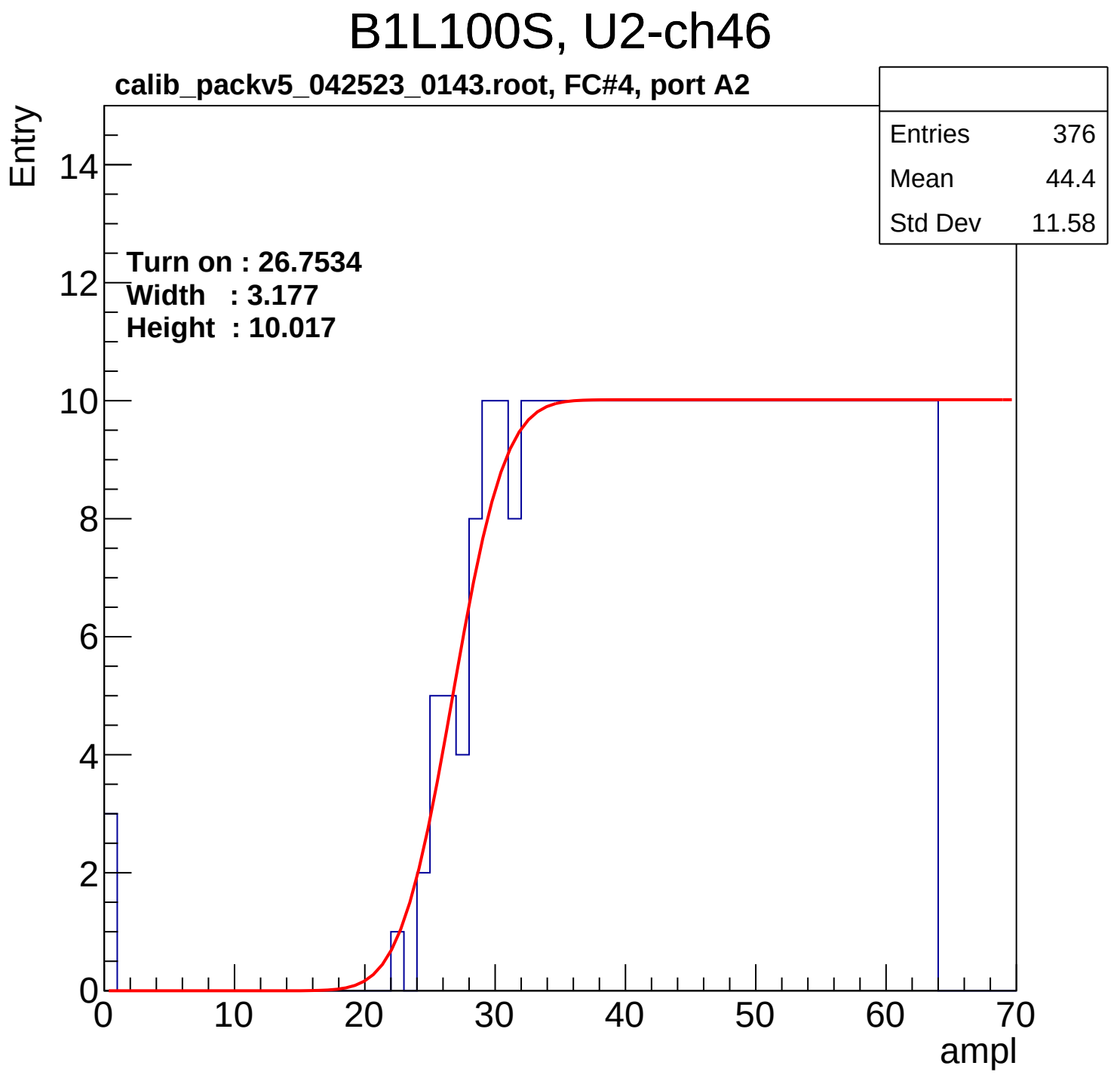
B1L100S, U2-ch46
calib_packv5_042523_0143.root, FC#4, port A2
Entries 376
Mean 44.4
Std Dev 11.58
Turn on : 26.7534
Width : 3.177
Height : 10.017
Entry
ampl
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6
8
10
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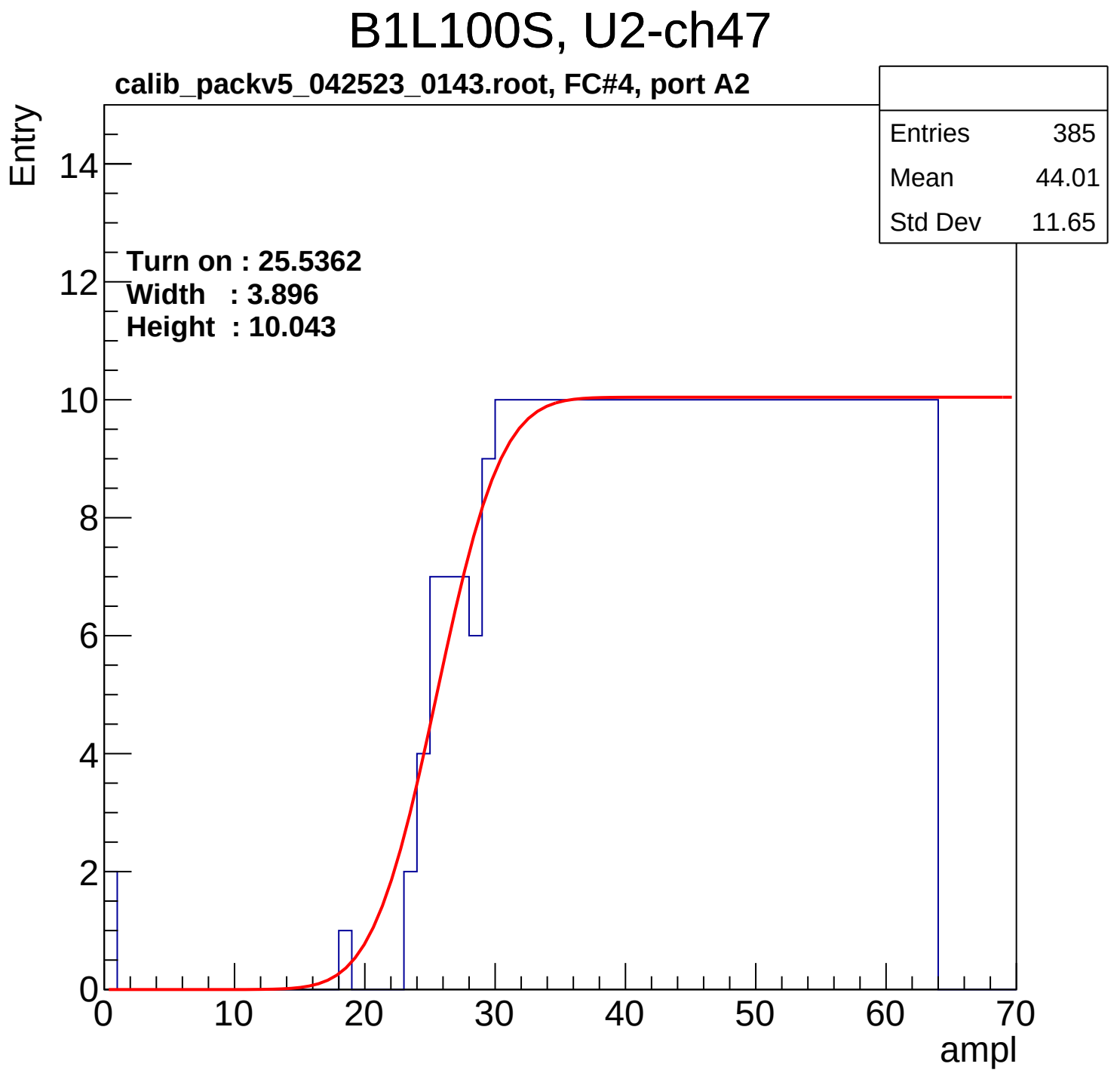
B1L100S, U2-ch47
calib_packv5_042523_0143.root, FC#4, port A2
Entries 385
Mean 44.01
Std Dev 11.65
Turn on : 25.5362
Width : 3.896
Height : 10.043
Entry
ampl
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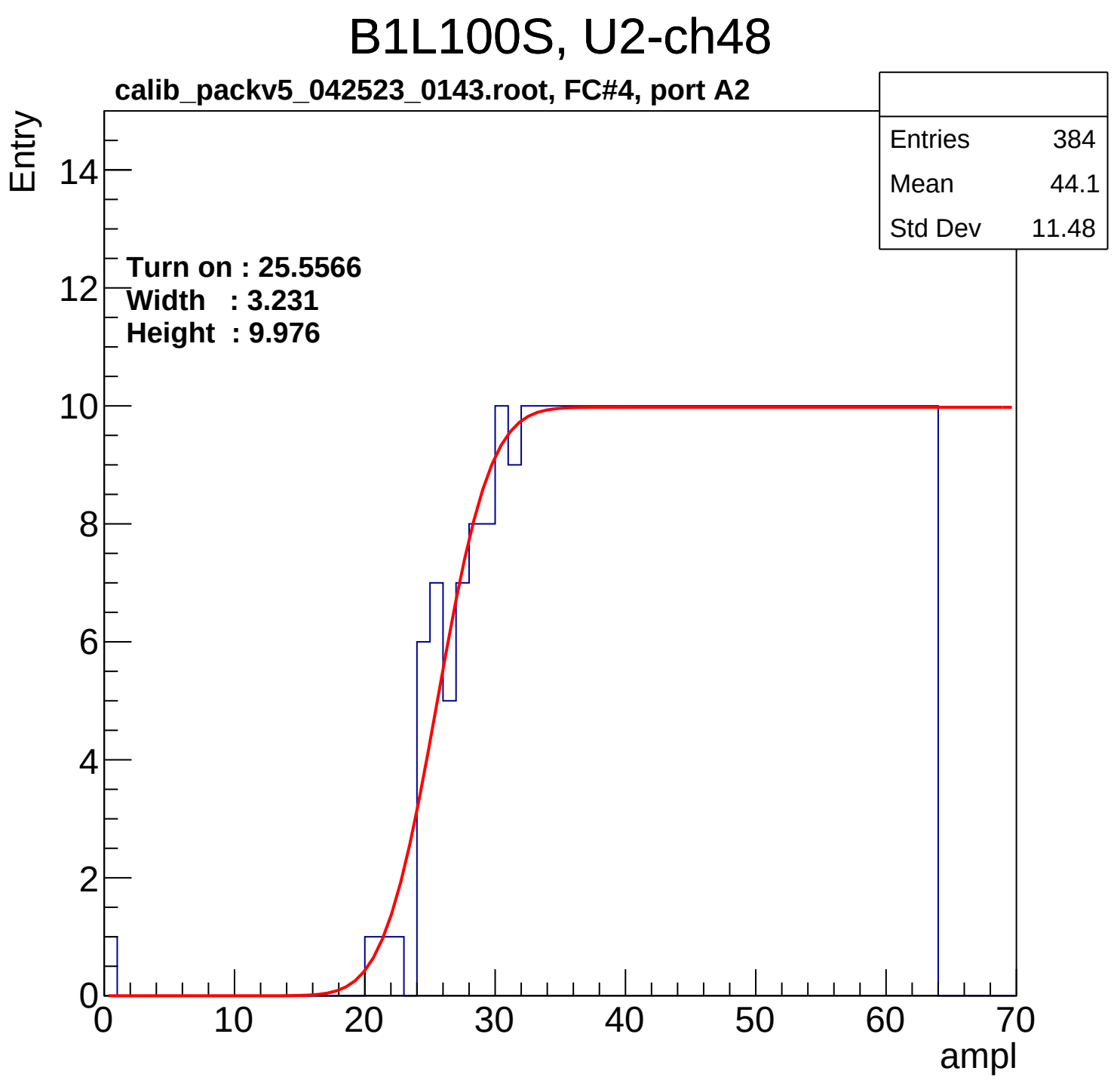
B1L100S, U2-ch48
calib_packv5_042523_0143.root, FC#4, port A2
Entries 384
Mean 44.1
Std Dev 11.48
Turn on : 25.5566
Width : 3.231
Height : 9.976
Entry
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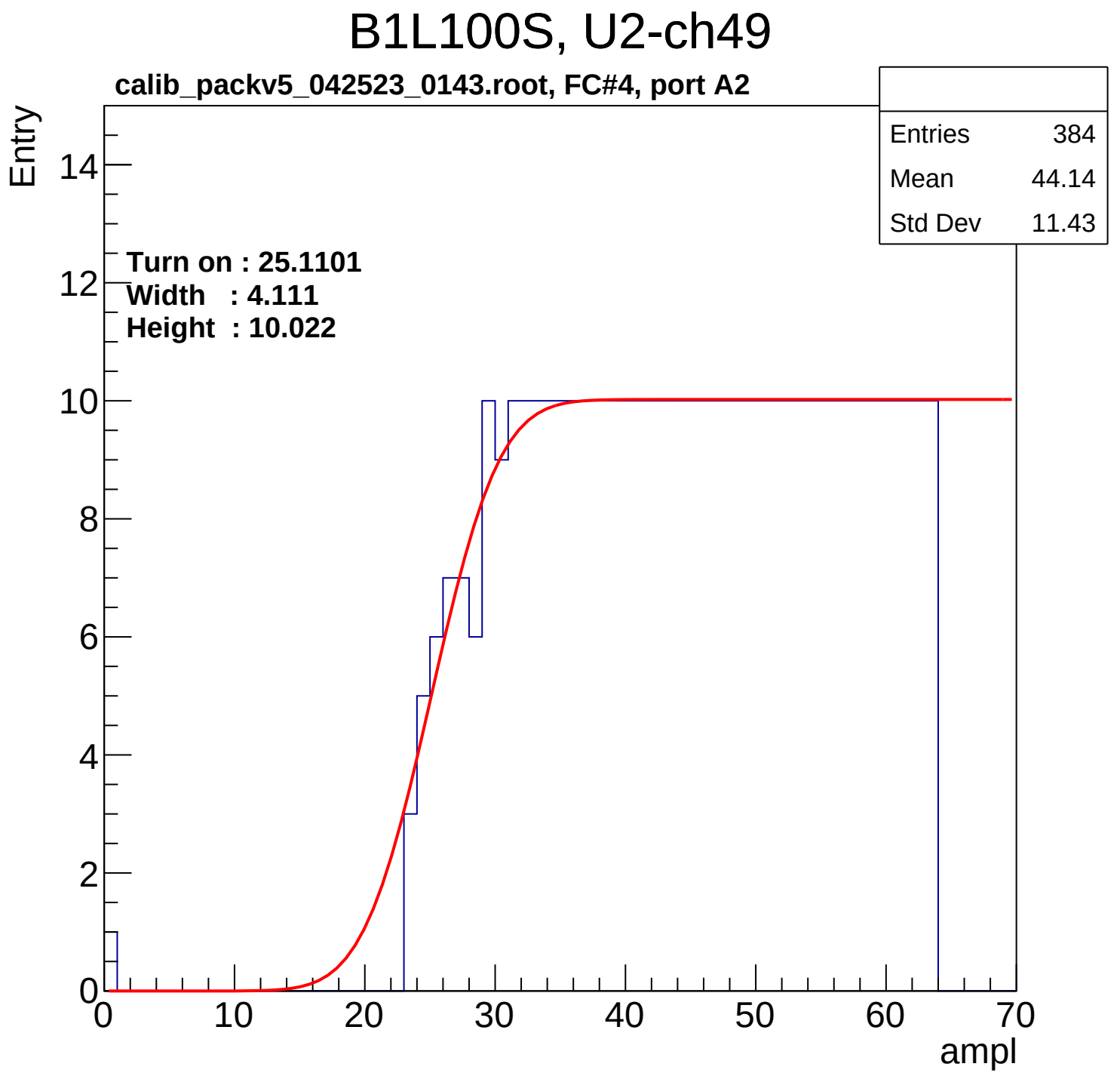
B1L100S, U2-ch49
calib_packv5_042523_0143.root, FC#4, port A2
Entries 384
Mean 44.14
Std Dev 11.43
Turn on : 25.1101
Width : 4.111
Height : 10.022
Entry
ampl
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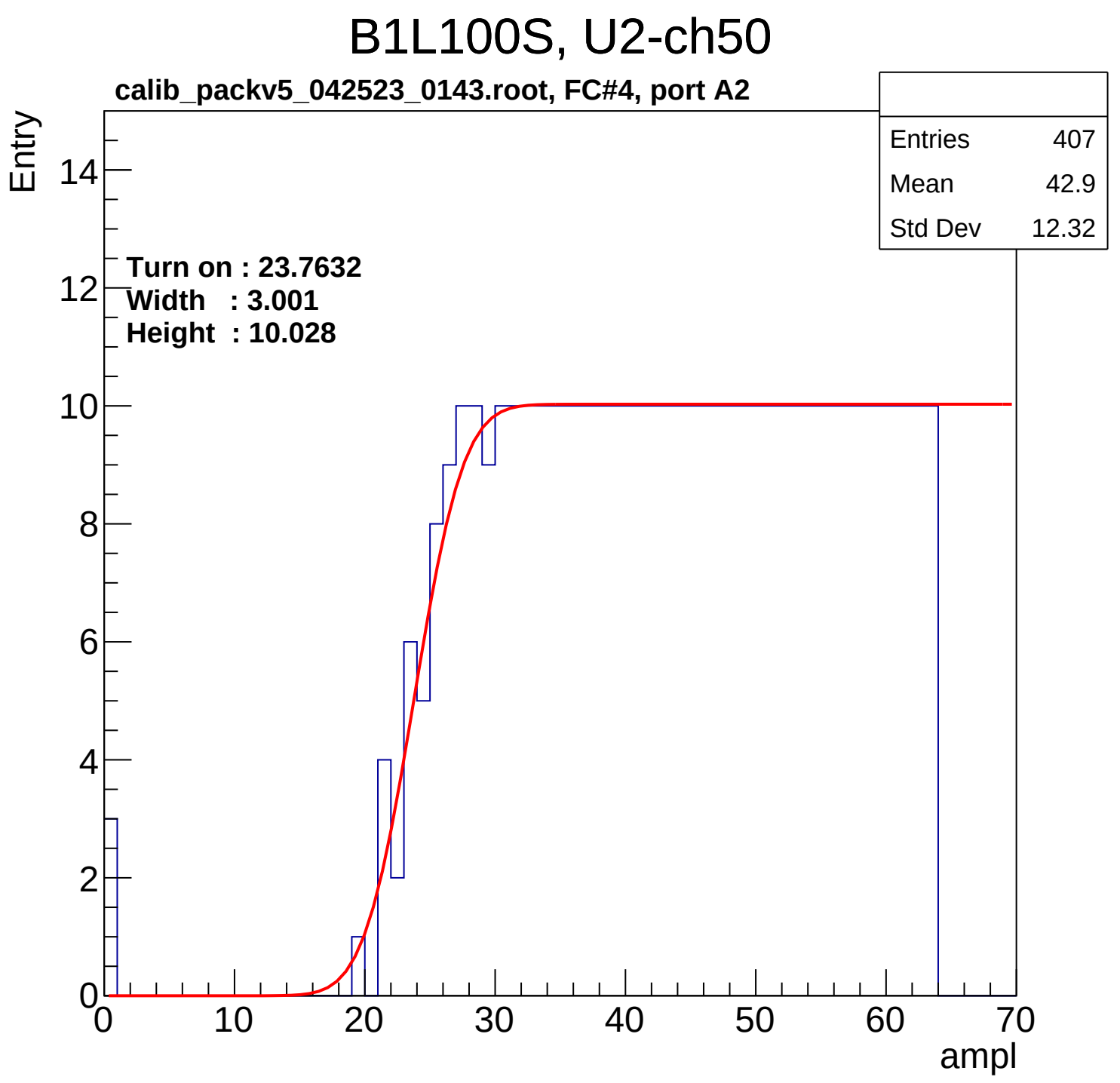
B1L100S, U2-ch50
calib_packv5_042523_0143.root, FC#4, port A2
Entries 407
Mean 42.9
Std Dev 12.32
Turn on : 23.7632
Width : 3.001
Height : 10.028
Entry
ampl
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8
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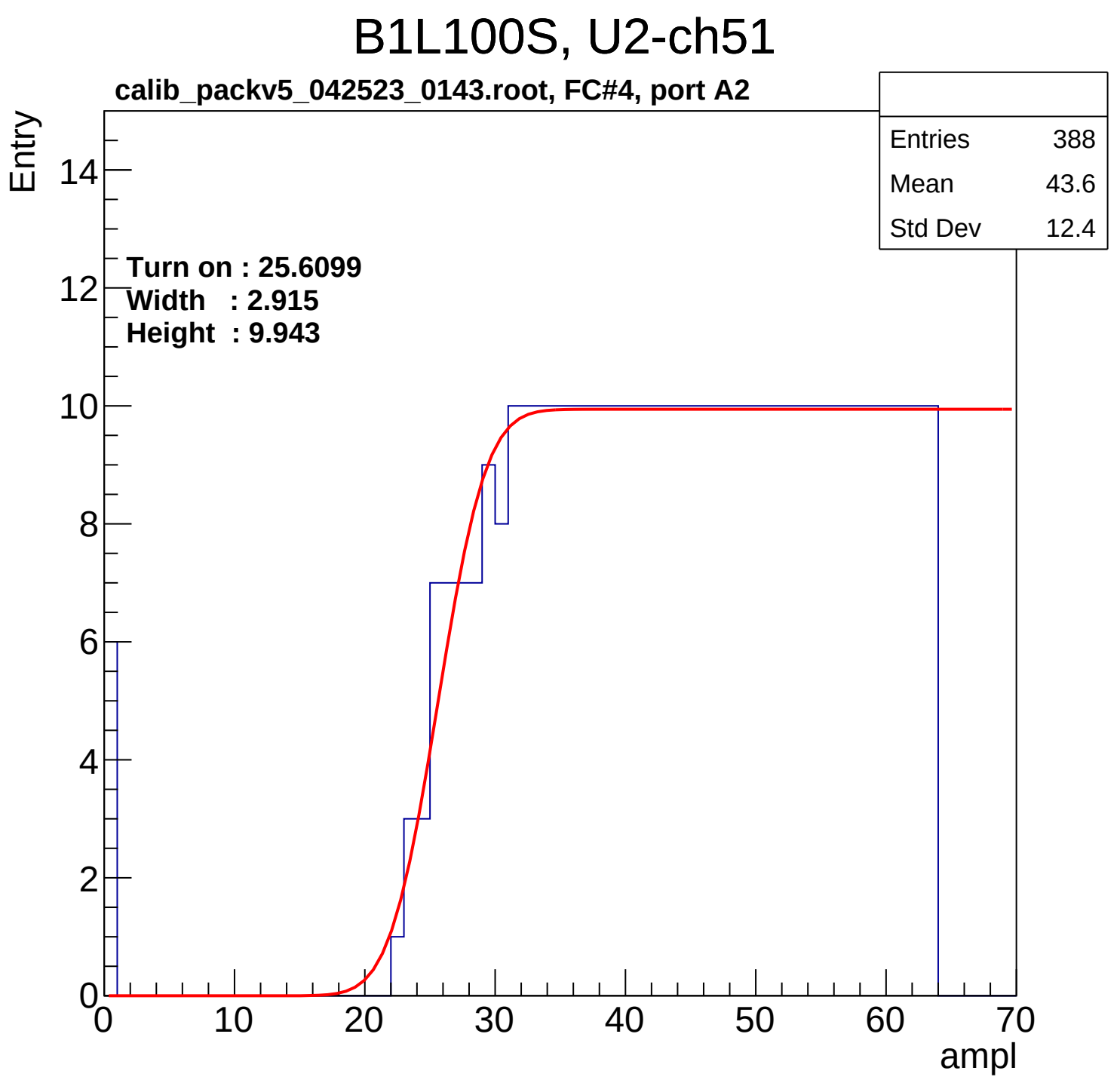
B1L100S, U2-ch51
calib_packv5_042523_0143.root, FC#4, port A2
Entries 388
Mean 43.6
Std Dev 12.4
Turn on : 25.6099
Width : 2.915
Height : 9.943
Entry
ampl
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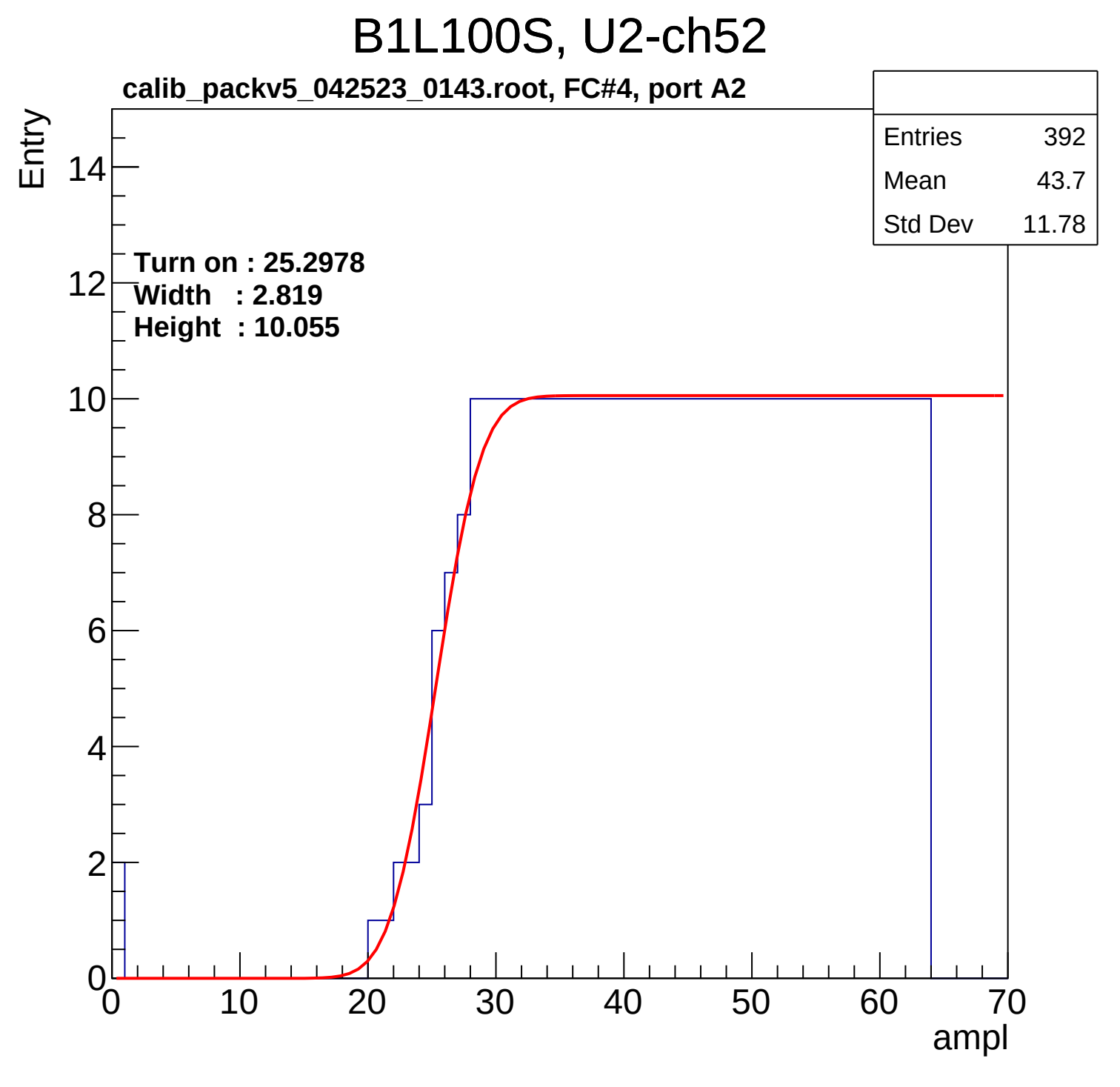
B1L100S, U2-ch52
calib_packv5_042523_0143.root, FC#4, port A2
Entries 392
Mean 43.7
Std Dev 11.78
Turn on : 25.2978
Width : 2.819
Height : 10.055
Entry
ampl
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6
8
10
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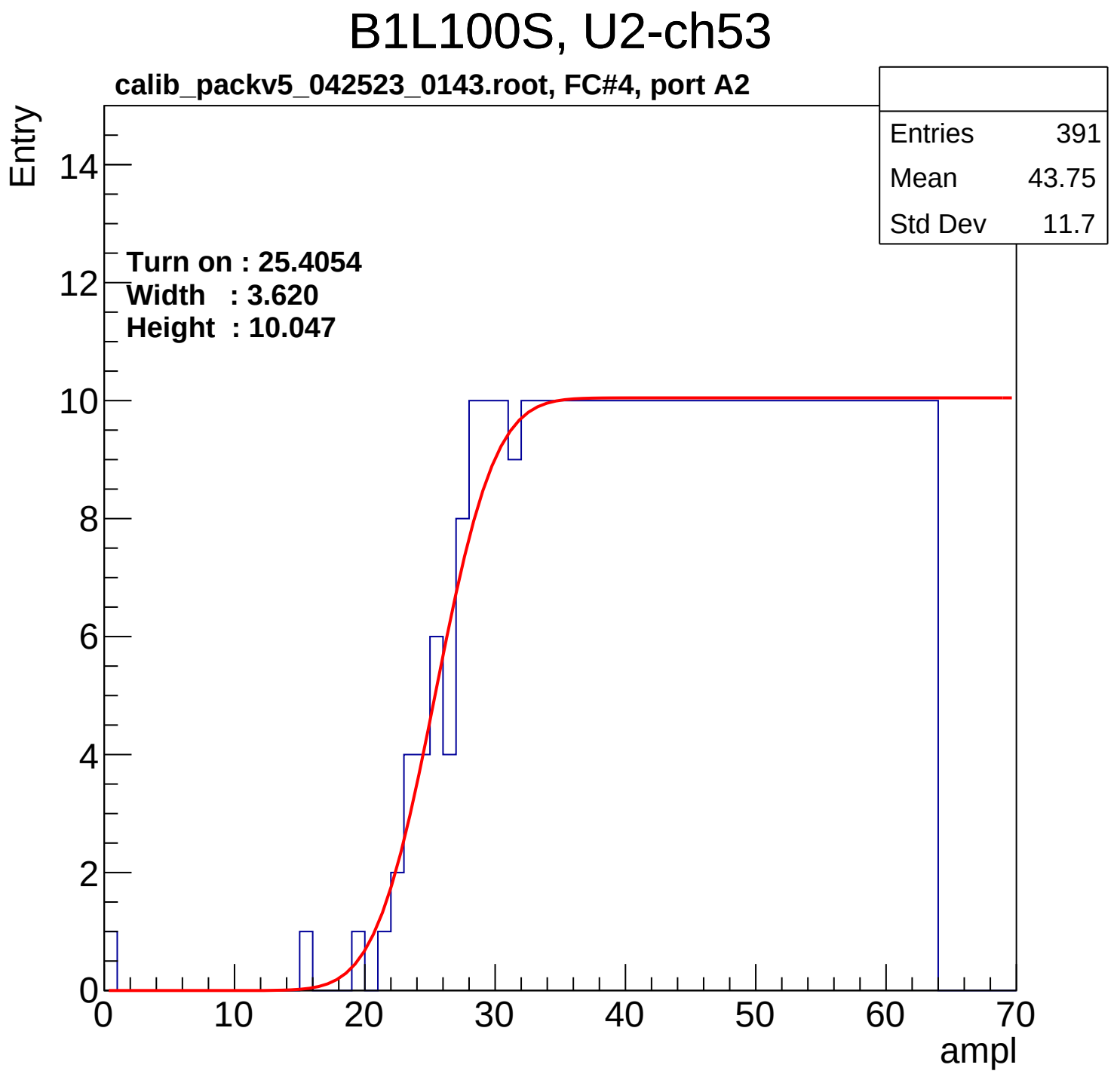
B1L100S, U2-ch53
calib_packv5_042523_0143.root, FC#4, port A2
Entries 391
Mean 43.75
Std Dev 11.7
Turn on : 25.4054
Width : 3.620
Height : 10.047
Entry
ampl
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6
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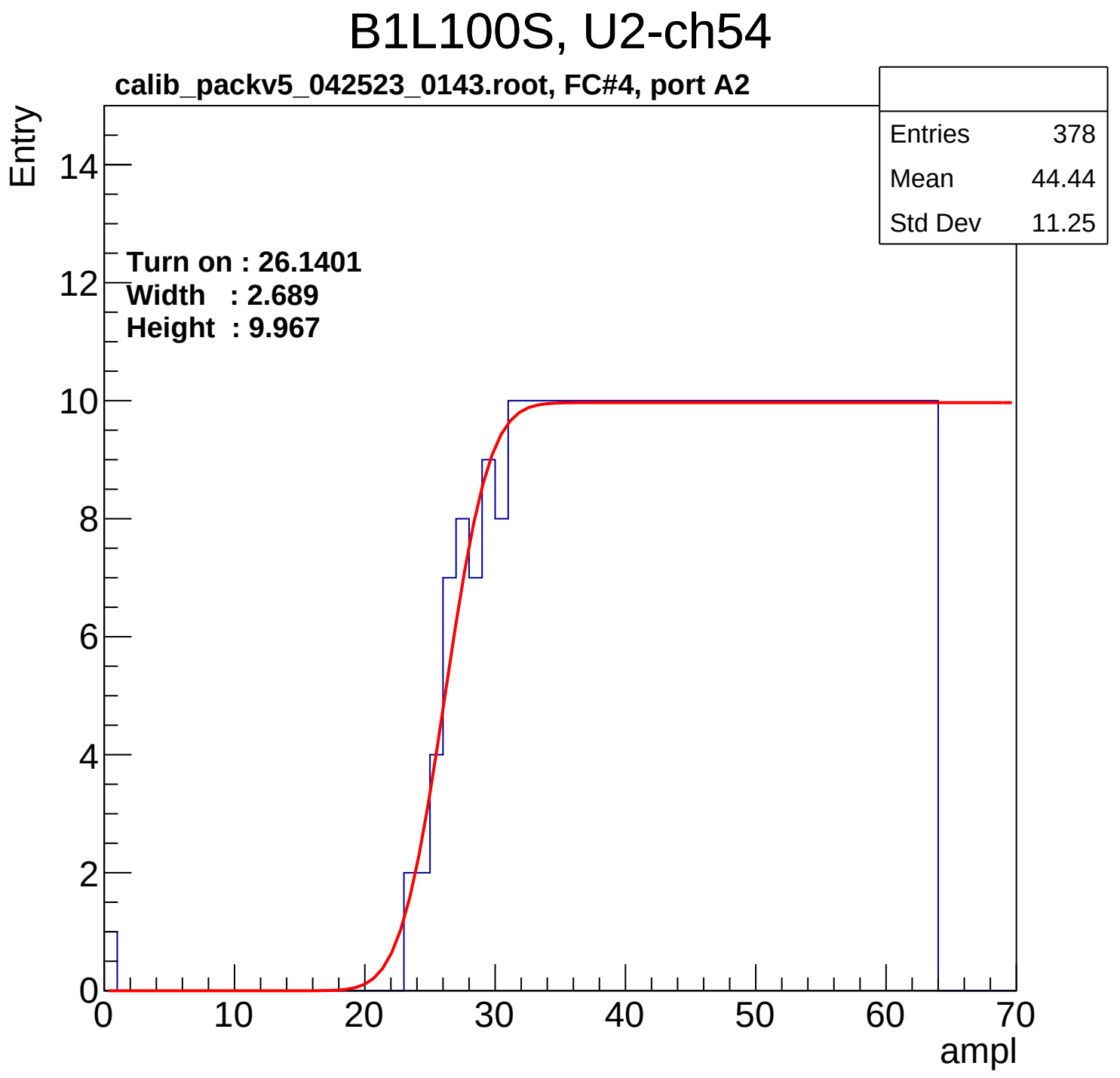
B1L100S, U2-ch54
calib_packv5_042523_0143.root, FC#4, port A2
Entries 378
Mean 44.44
Std Dev 11.25
Turn on : 26.1401
Width : 2.689
Height : 9.967
Entry
ampl
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6
8
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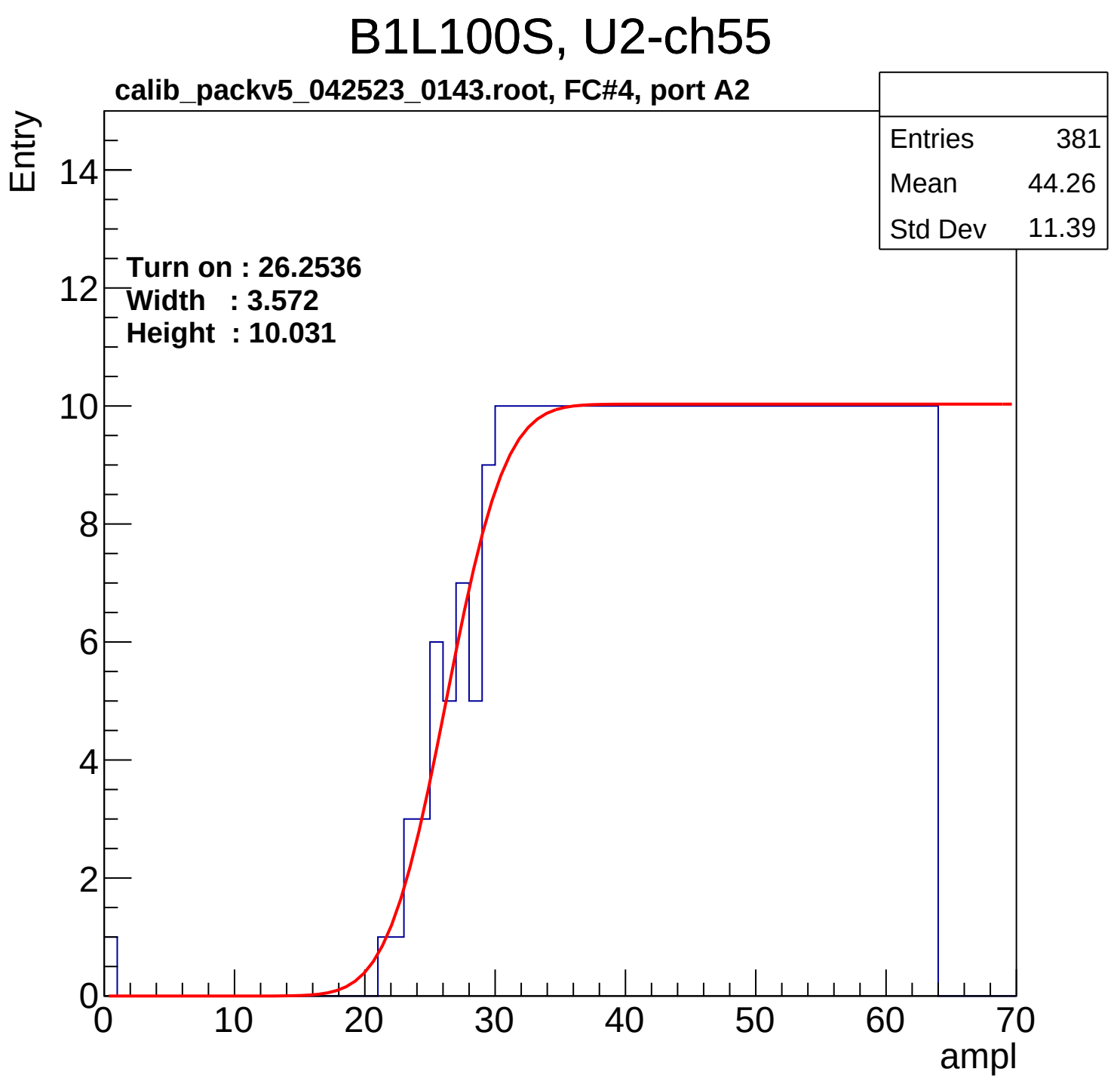
B1L100S, U2-ch55
calib_packv5_042523_0143.root, FC#4, port A2
Entries 381
Mean 44.26
Std Dev 11.39
Turn on : 26.2536
Width : 3.572
Height : 10.031
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ampl
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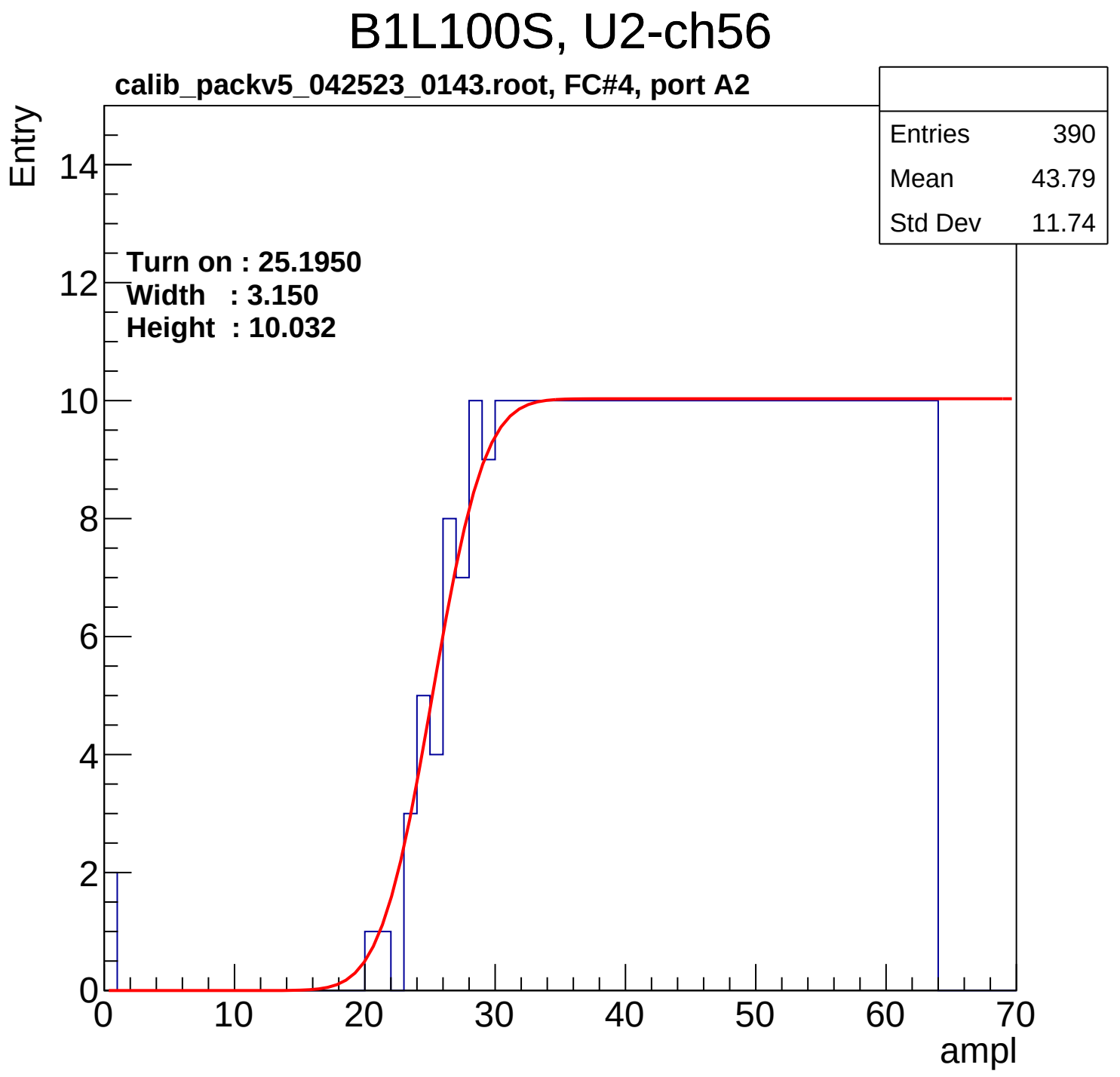
B1L100S, U2-ch56
calib_packv5_042523_0143.root, FC#4, port A2
Entries 390
Mean 43.79
Std Dev 11.74
Turn on : 25.1950
Width : 3.150
Height : 10.032
Entry
ampl
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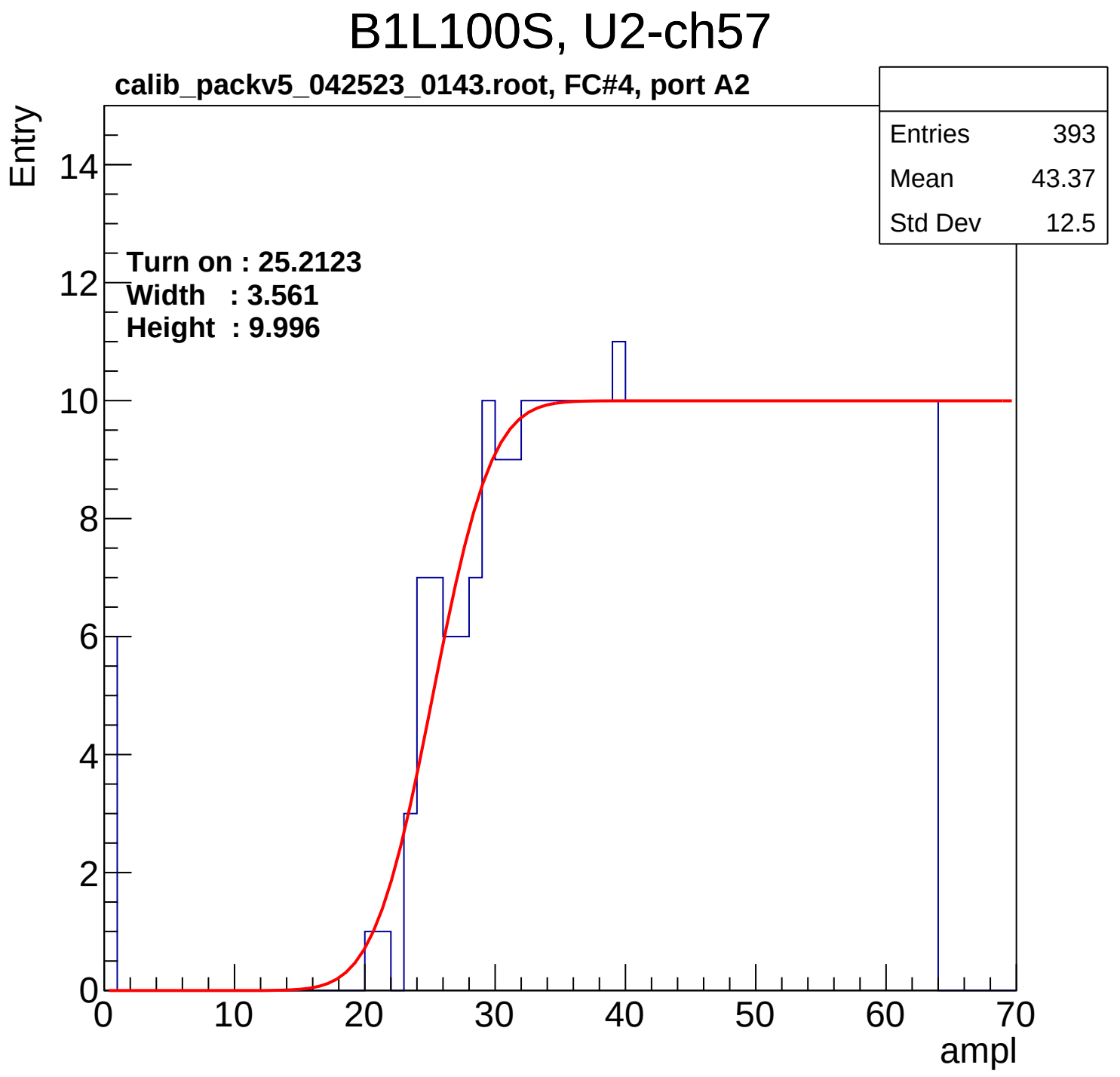
B1L100S, U2-ch57
calib_packv5_042523_0143.root, FC#4, port A2
Entries 393
Mean 43.37
Std Dev 12.5
Turn on : 25.2123
Width : 3.561
Height : 9.996
Entry
ampl
0
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4
6
8
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12
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10
20
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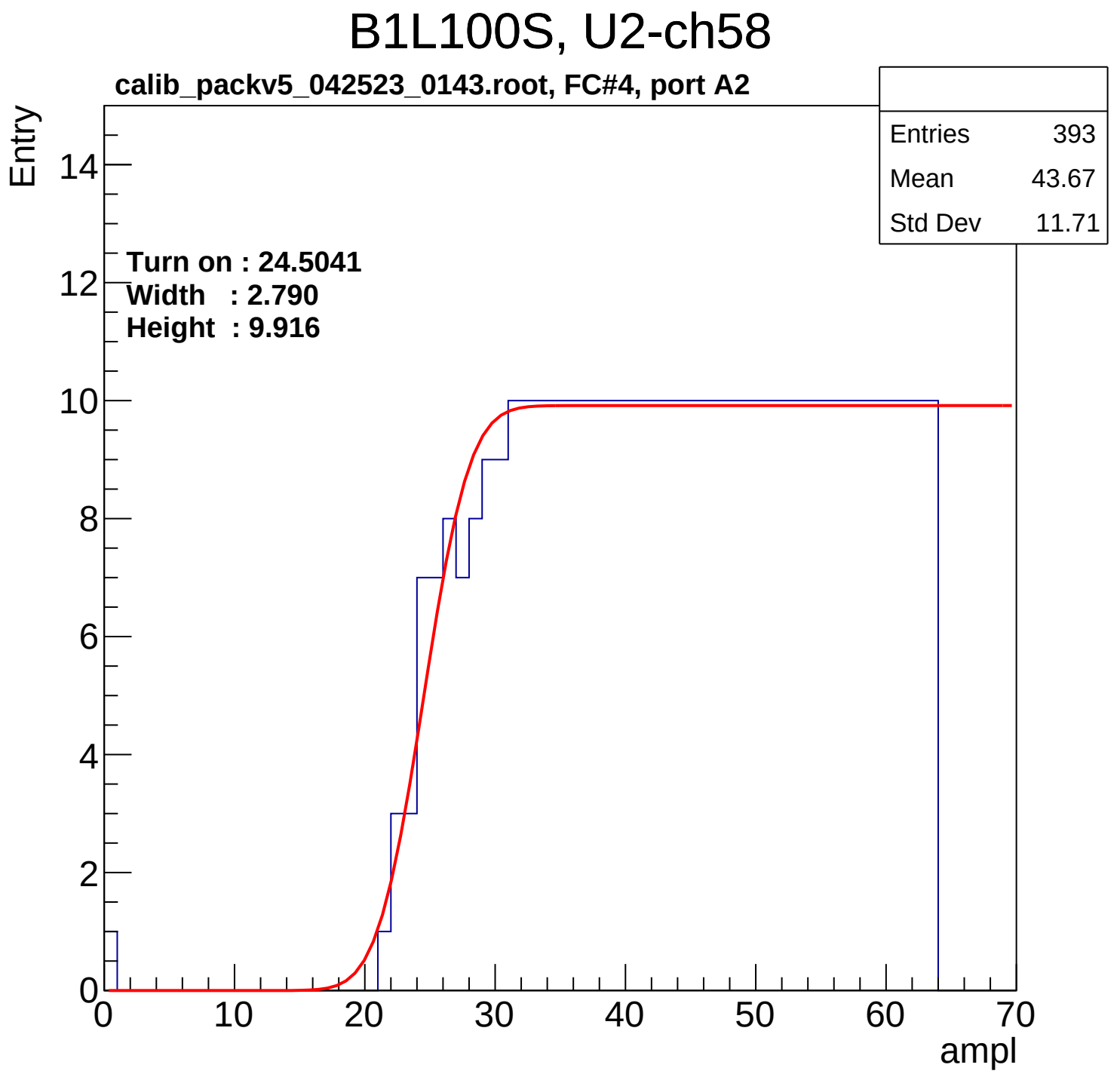
B1L100S, U2-ch58
calib_packv5_042523_0143.root, FC#4, port A2
Entries 393
Mean 43.67
Std Dev 11.71
Turn on : 24.5041
Width : 2.790
Height : 9.916
Entry
ampl
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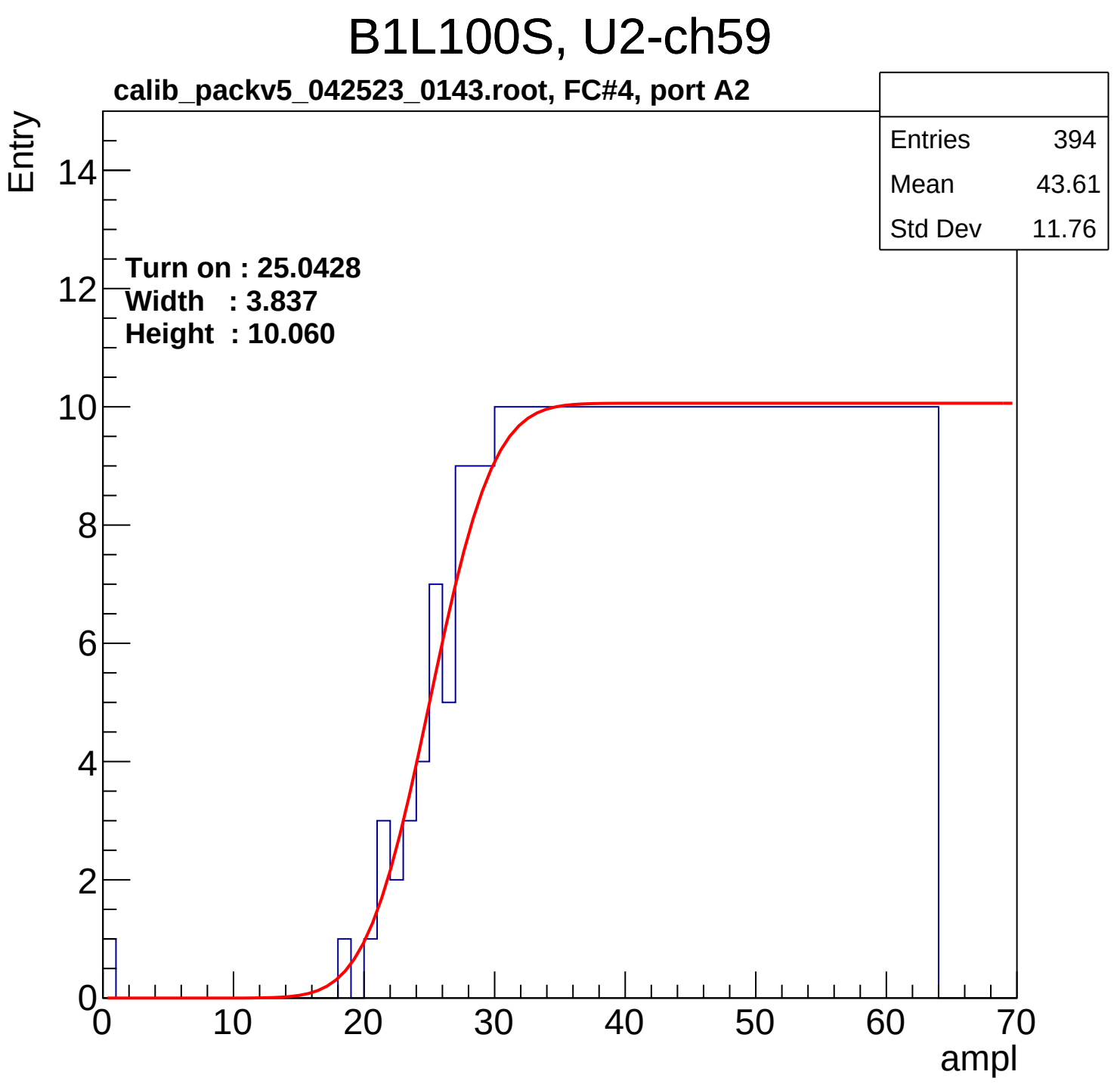
B1L100S, U2-ch59
calib_packv5_042523_0143.root, FC#4, port A2
Entries 394
Mean 43.61
Std Dev 11.76
Turn on : 25.0428
Width : 3.837
Height : 10.060
Entry
ampl
0
2
4
6
8
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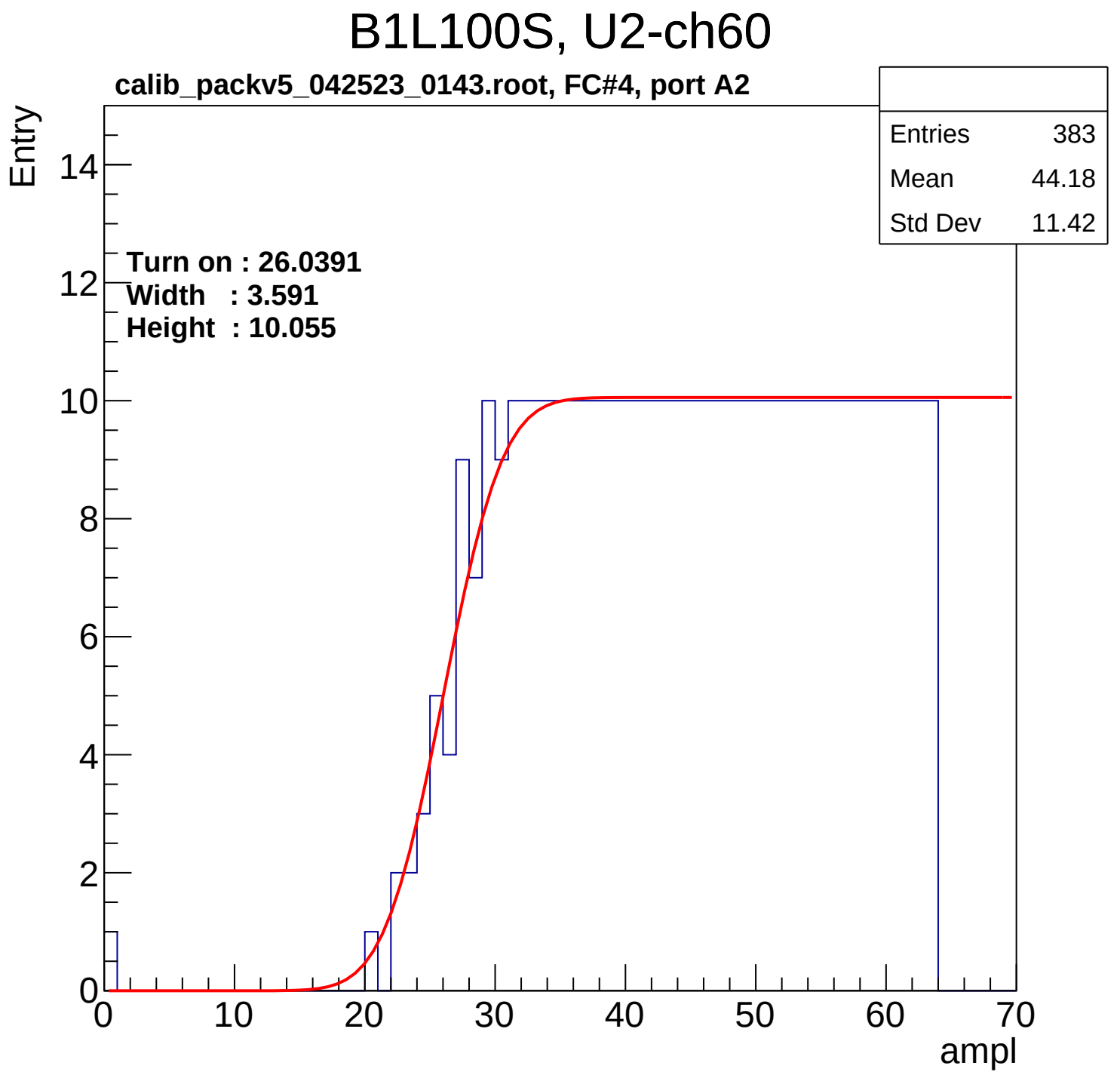
B1L100S, U2-ch60
calib_packv5_042523_0143.root, FC#4, port A2
Entries 383
Mean 44.18
Std Dev 11.42
Turn on : 26.0391
Width : 3.591
Height : 10.055
Entry
ampl
0
2
4
6
8
10
12
14
0
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40
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60
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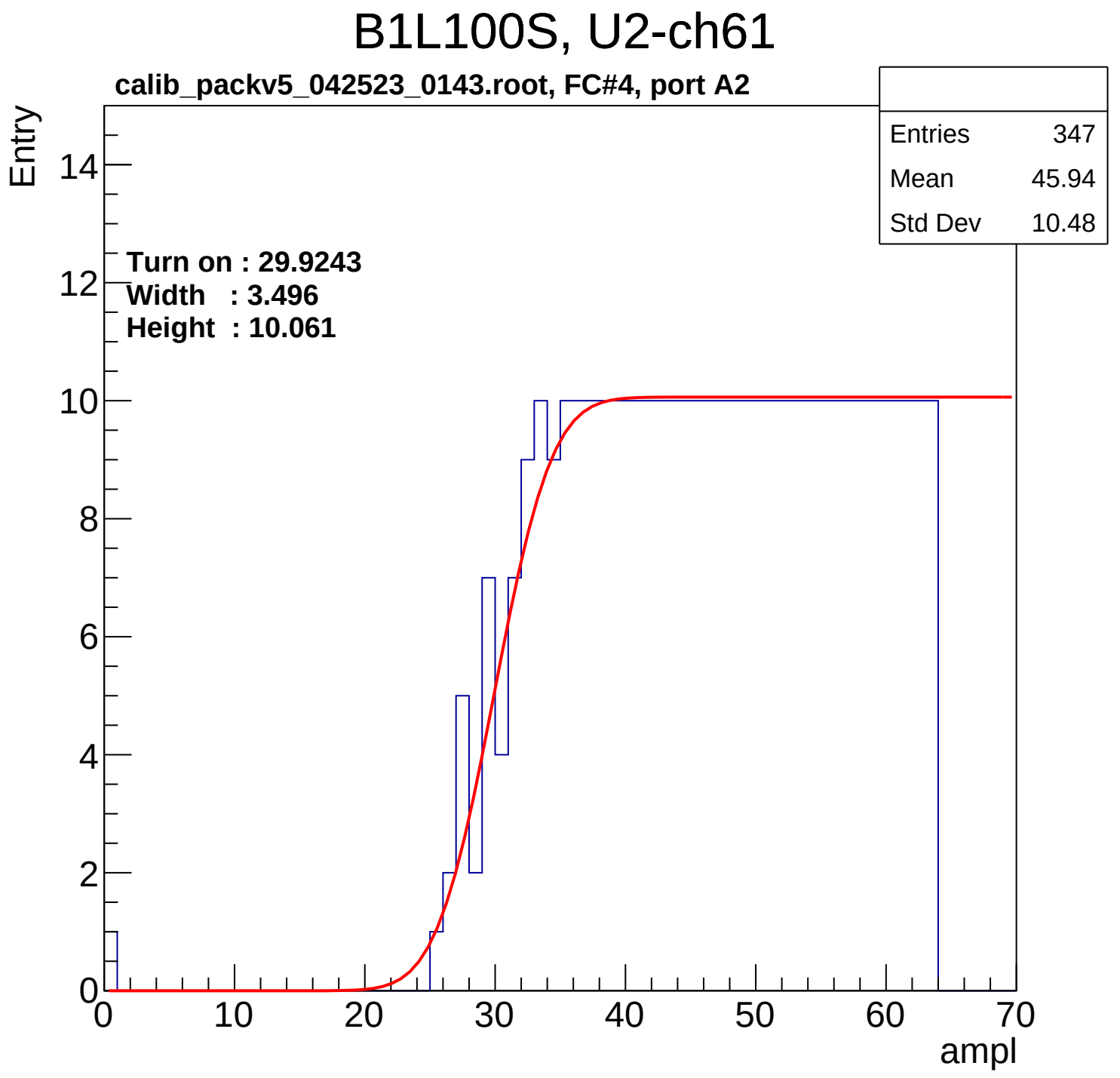
B1L100S, U2-ch61
calib_packv5_042523_0143.root, FC#4, port A2
Entries 347
Mean 45.94
Std Dev 10.48
Turn on : 29.9243
Width : 3.496
Height : 10.061
Entry
ampl
0
2
4
6
8
10
12
14
0
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60
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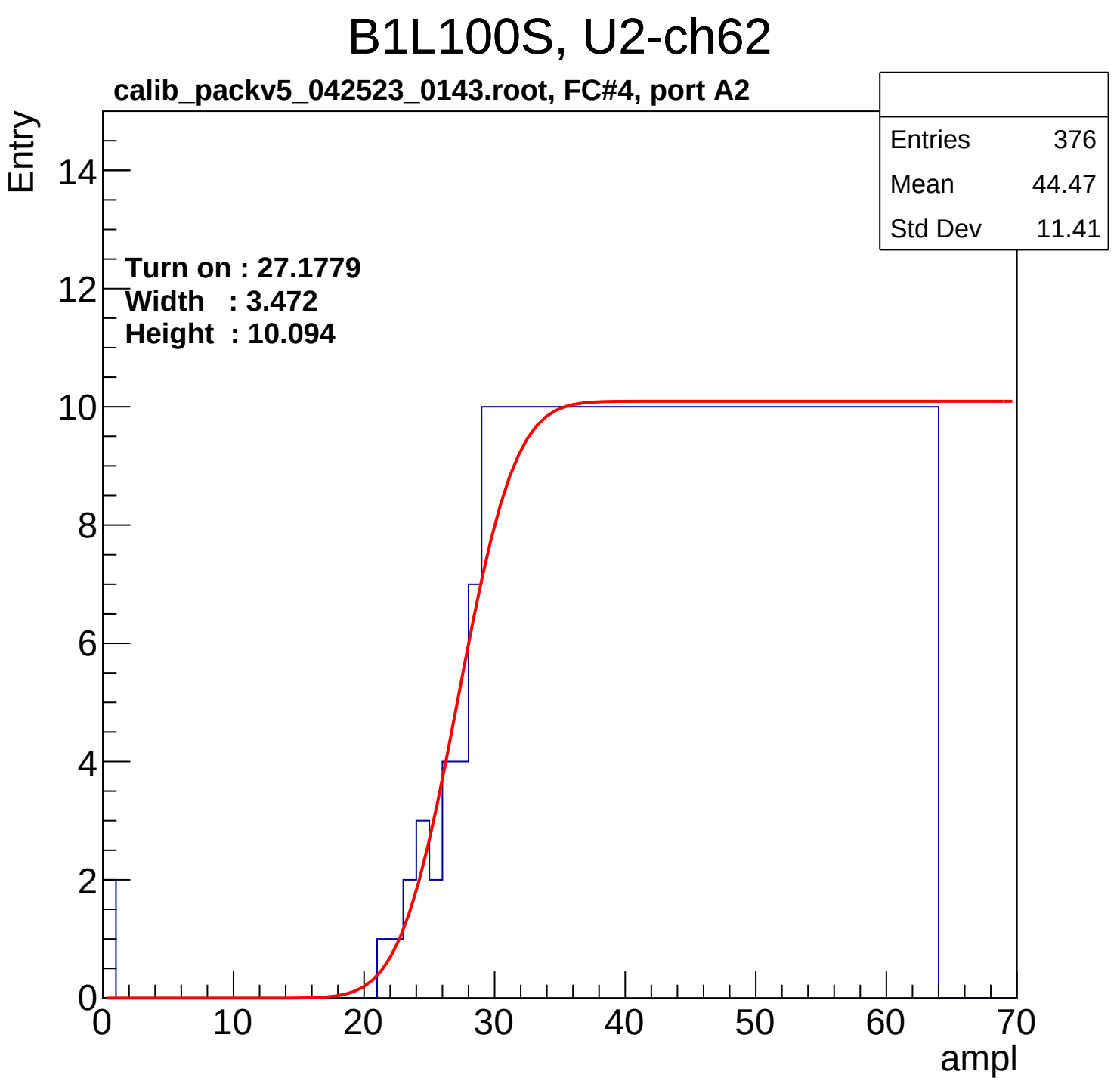
B1L100S, U2-ch62
calib_packv5_042523_0143.root, FC#4, port A2
Entries 376
Mean 44.47
Std Dev 11.41
Turn on : 27.1779
Width : 3.472
Height : 10.094
Entry
ampl
0
2
4
6
8
10
12
14
0
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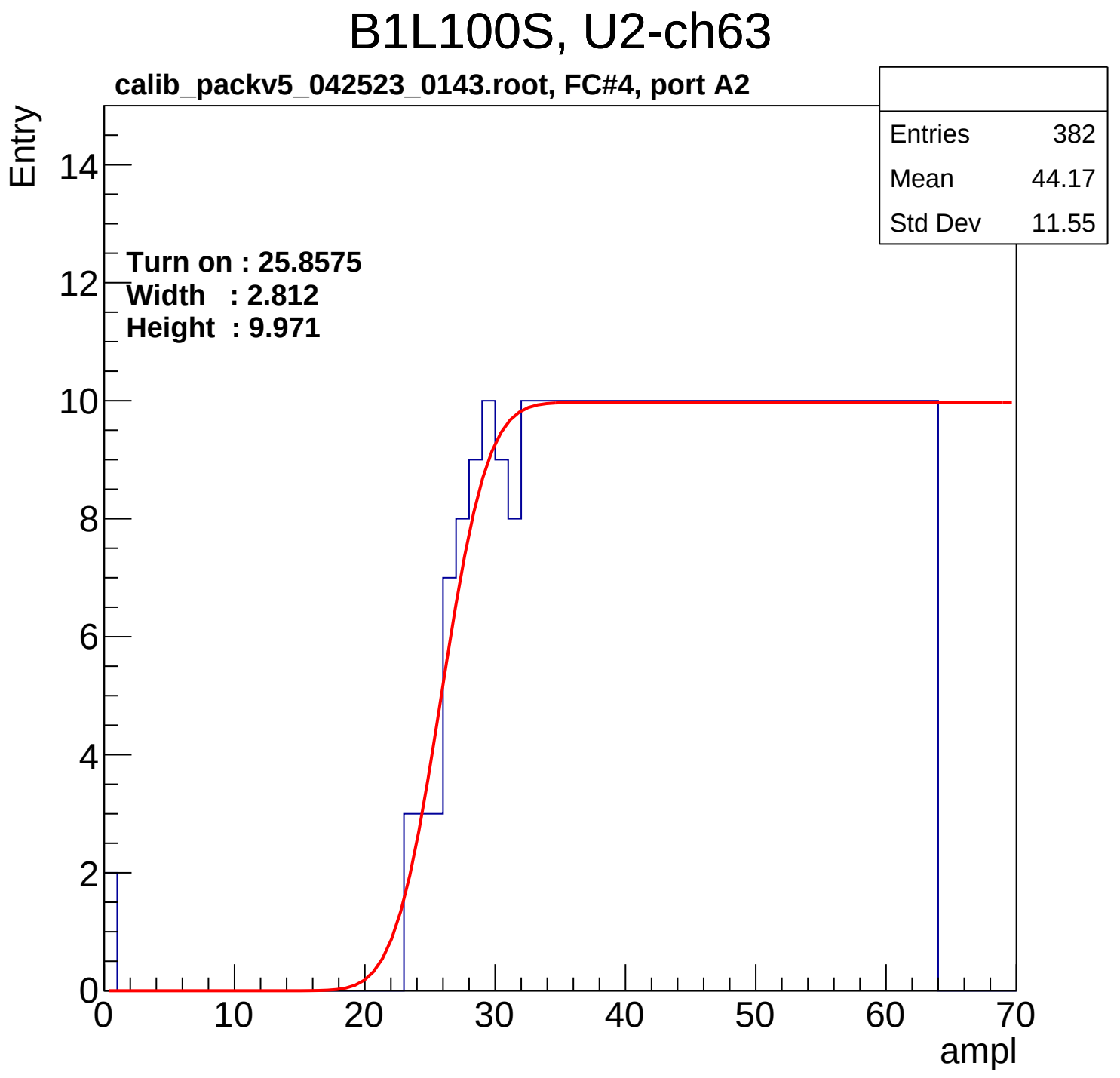
B1L100S, U2-ch63
calib_packv5_042523_0143.root, FC#4, port A2
Entries 382
Mean 44.17
Std Dev 11.55
Turn on : 25.8575
Width : 2.812
Height : 9.971
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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60
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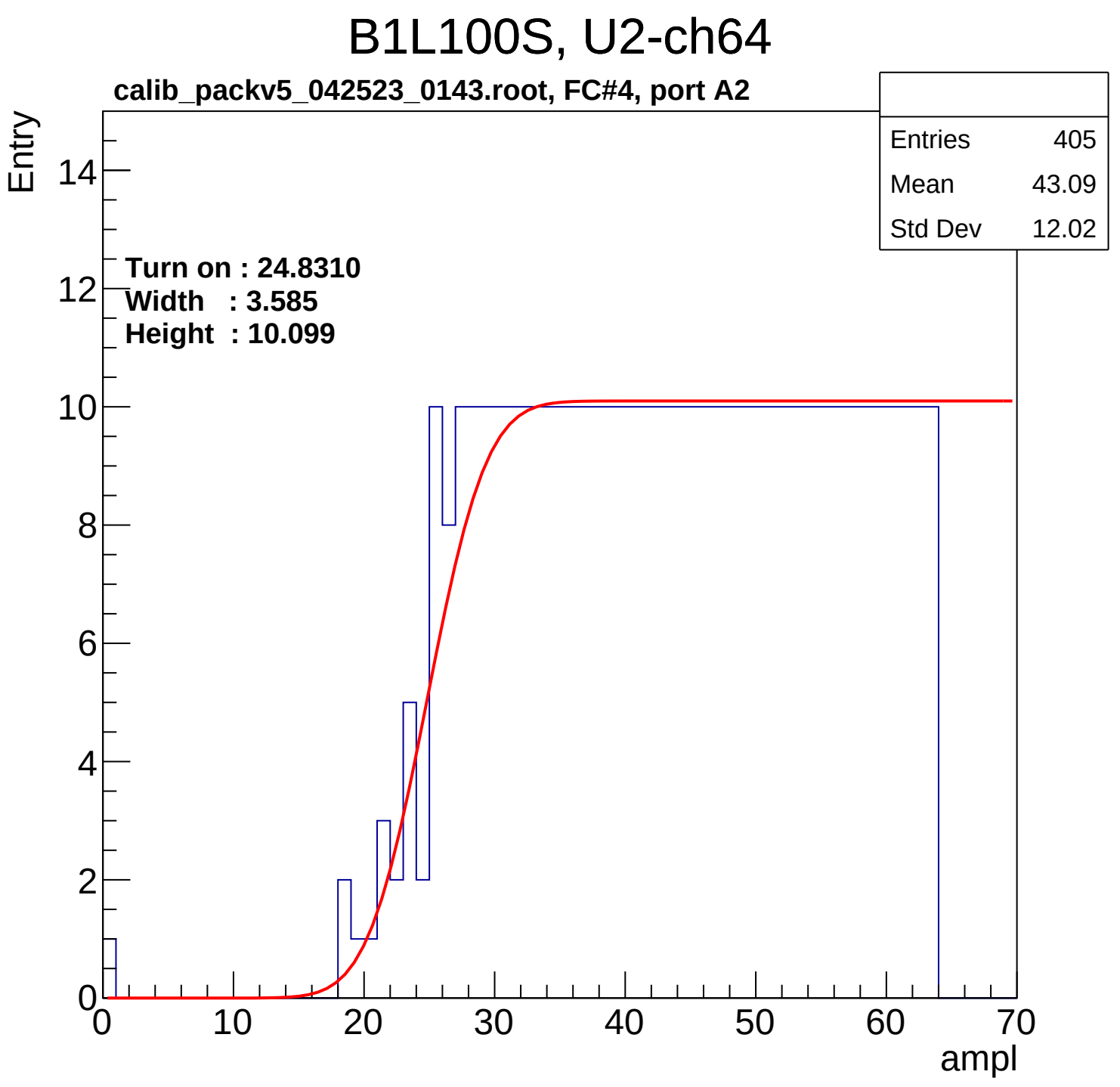
B1L100S, U2-ch64
calib_packv5_042523_0143.root, FC#4, port A2
Entries 405
Mean 43.09
Std Dev 12.02
Turn on : 24.8310
Width : 3.585
Height : 10.099
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
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60
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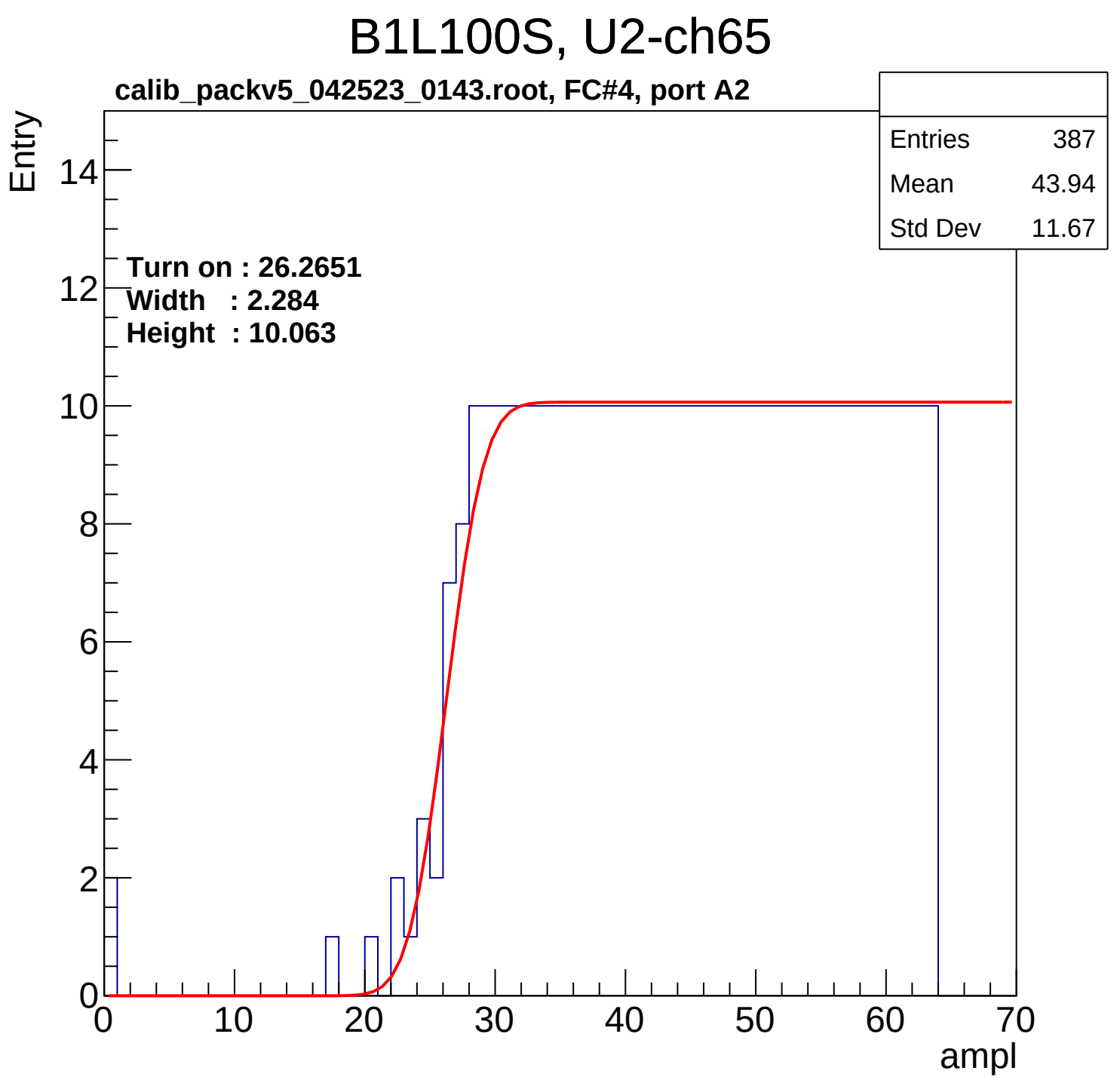
B1L100S, U2-ch65
calib_packv5_042523_0143.root, FC#4, port A2
Entries 387
Mean 43.94
Std Dev 11.67
Turn on : 26.2651
Width : 2.284
Height : 10.063
Entry
ampl
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2
4
6
8
10
12
14
0
10
20
30
40
50
60
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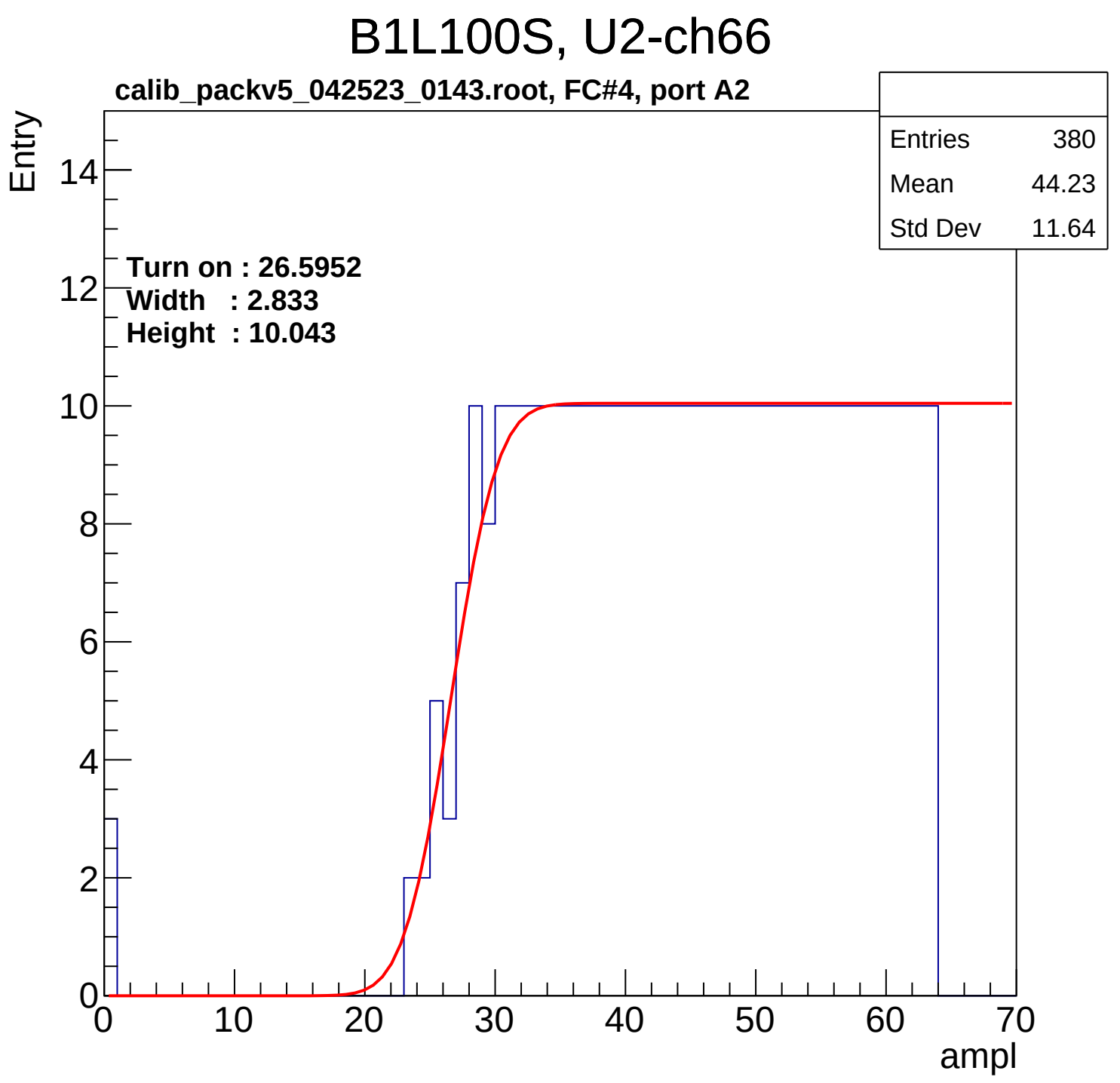
B1L100S, U2-ch66
calib_packv5_042523_0143.root, FC#4, port A2
Entries 380
Mean 44.23
Std Dev 11.64
Turn on : 26.5952
Width : 2.833
Height : 10.043
Entry
ampl
0
2
4
6
8
10
12
14
0
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40
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60
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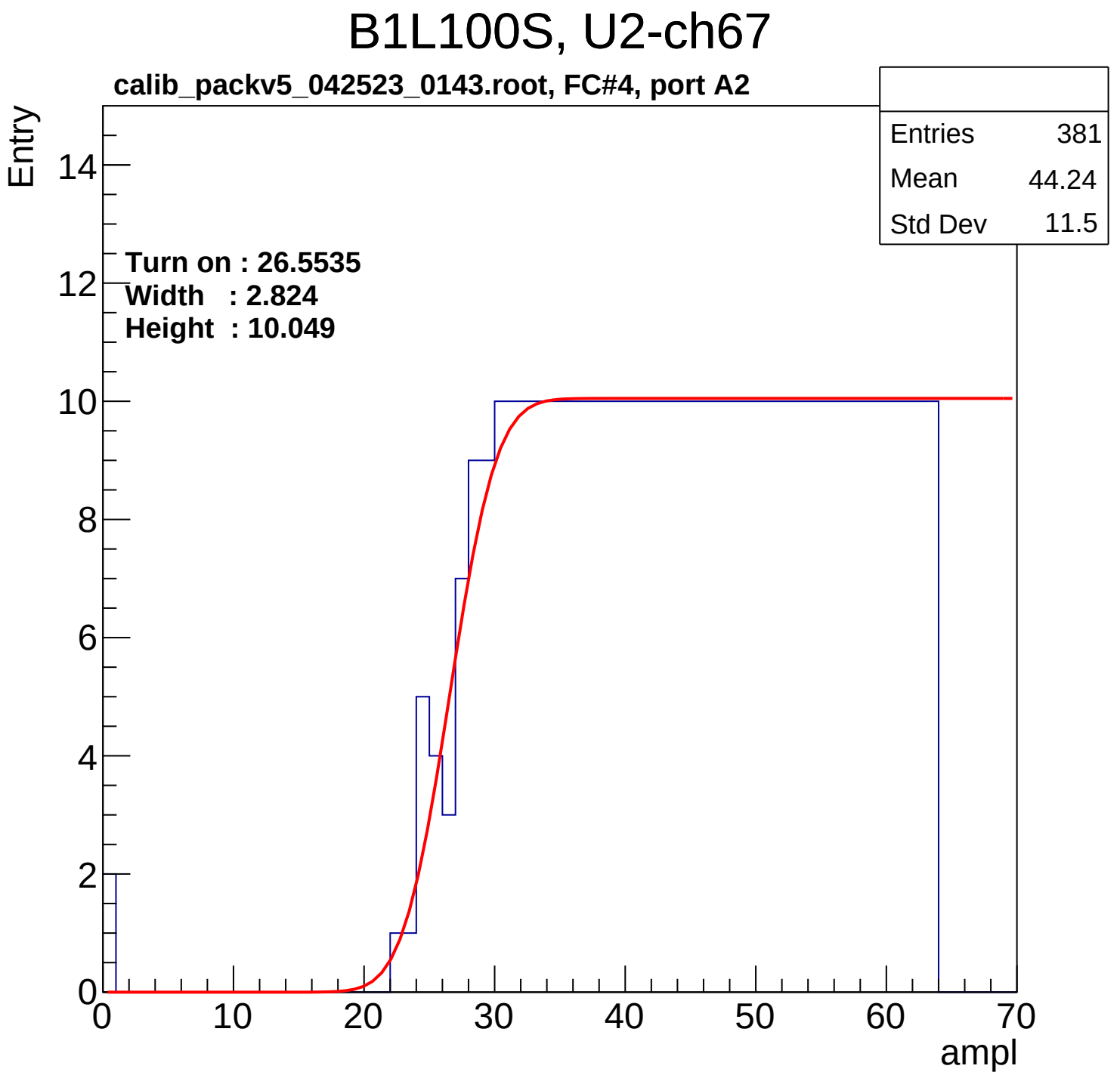
B1L100S, U2-ch67
calib_packv5_042523_0143.root, FC#4, port A2
Entries 381
Mean 44.24
Std Dev 11.5
Turn on : 26.5535
Width : 2.824
Height : 10.049
Entry
ampl
0
2
4
6
8
10
12
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0
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20
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40
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60
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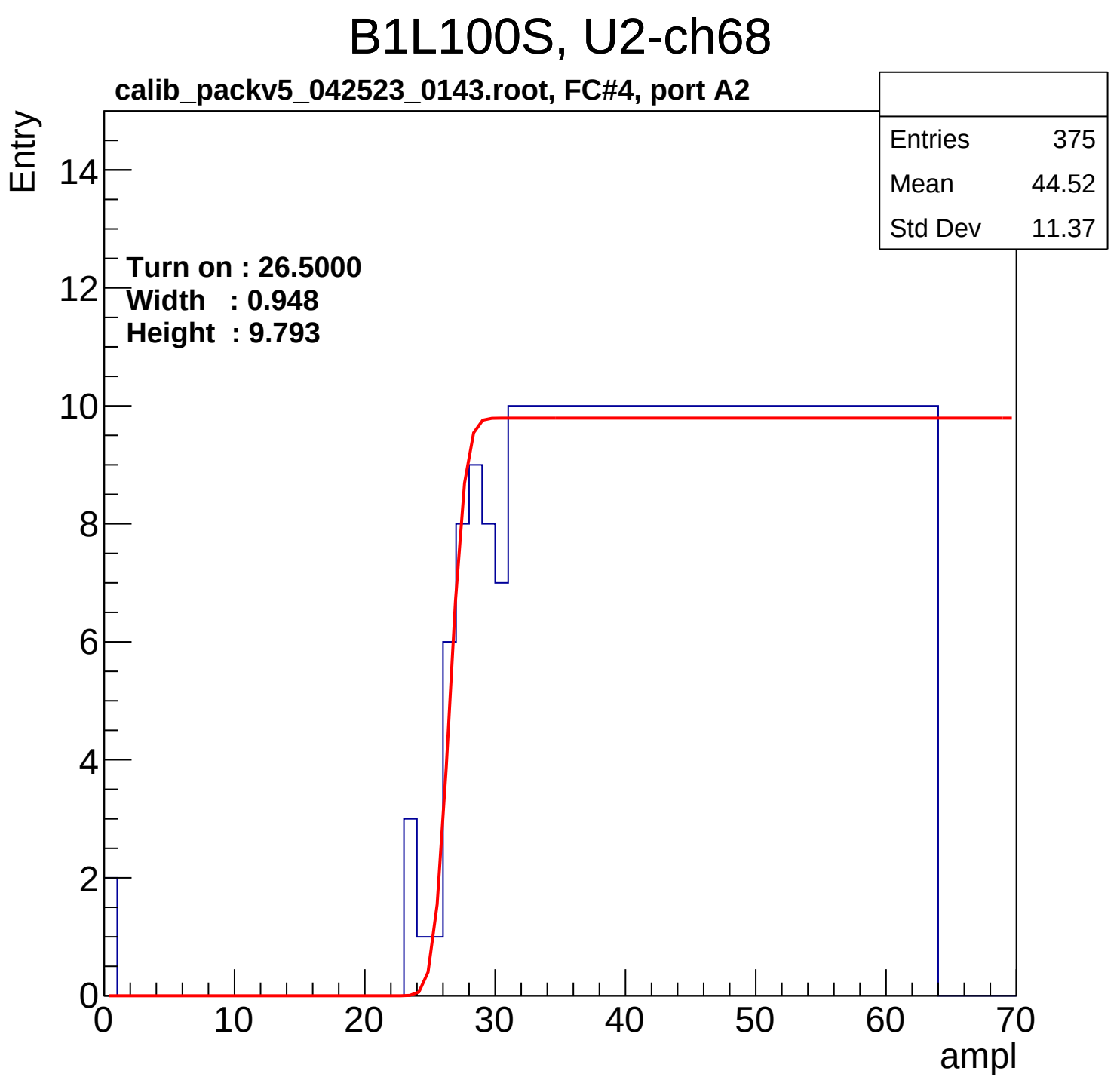
B1L100S, U2-ch68
calib_packv5_042523_0143.root, FC#4, port A2
Entries 375
Mean 44.52
Std Dev 11.37
Turn on : 26.5000
Width : 0.948
Height : 9.793
Entry
ampl
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2
4
6
8
10
12
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0
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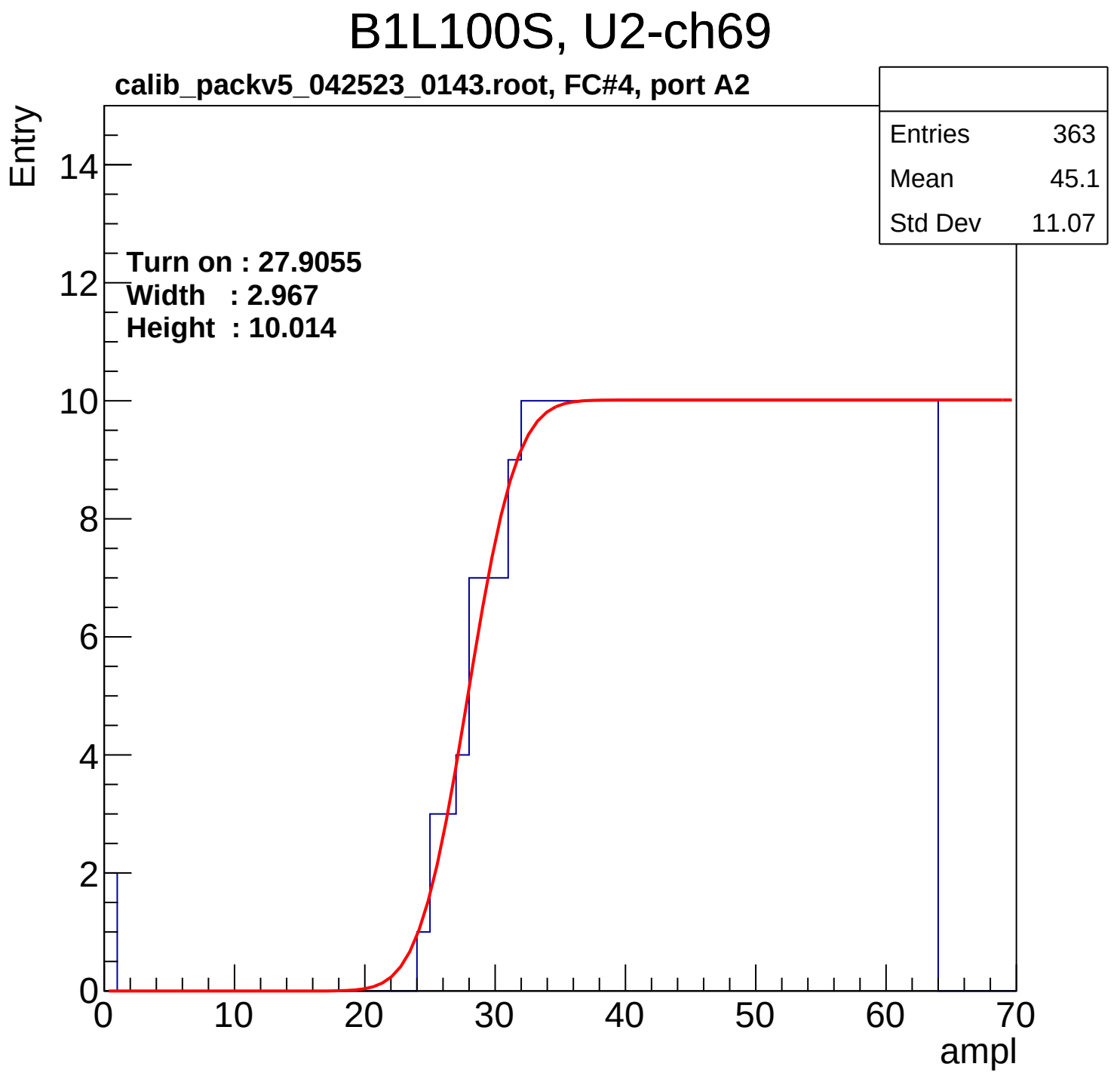
B1L100S, U2-ch69
calib_packv5_042523_0143.root, FC#4, port A2
Entries 363
Mean 45.1
Std Dev 11.07
Turn on : 27.9055
Width : 2.967
Height : 10.014
Entry
ampl
0
2
4
6
8
10
12
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0
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60
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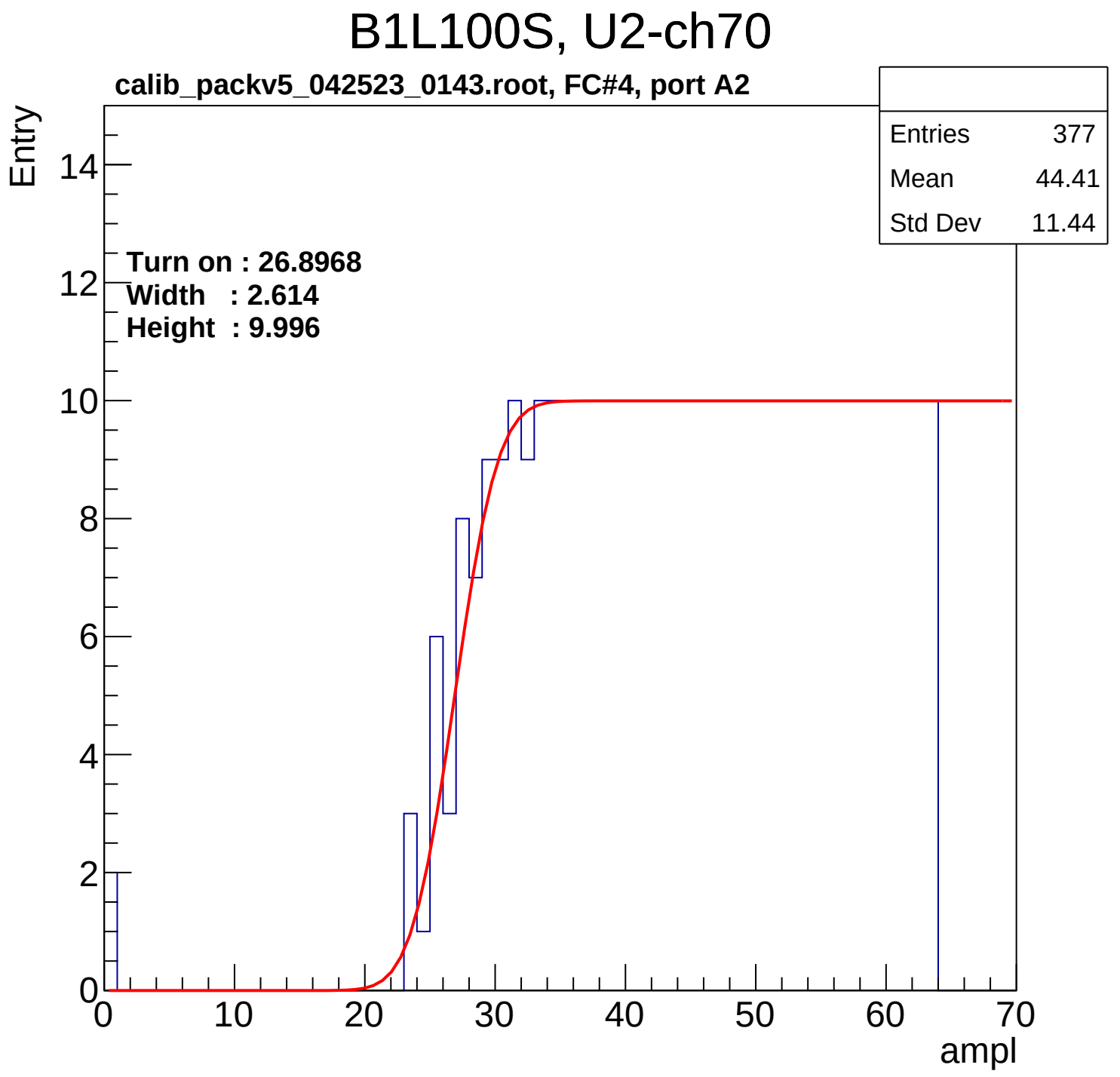
B1L100S, U2-ch70
calib_packv5_042523_0143.root, FC#4, port A2
Entries 377
Mean 44.41
Std Dev 11.44
Turn on : 26.8968
Width : 2.614
Height : 9.996
Entry
ampl
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2
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6
8
10
12
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0
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20
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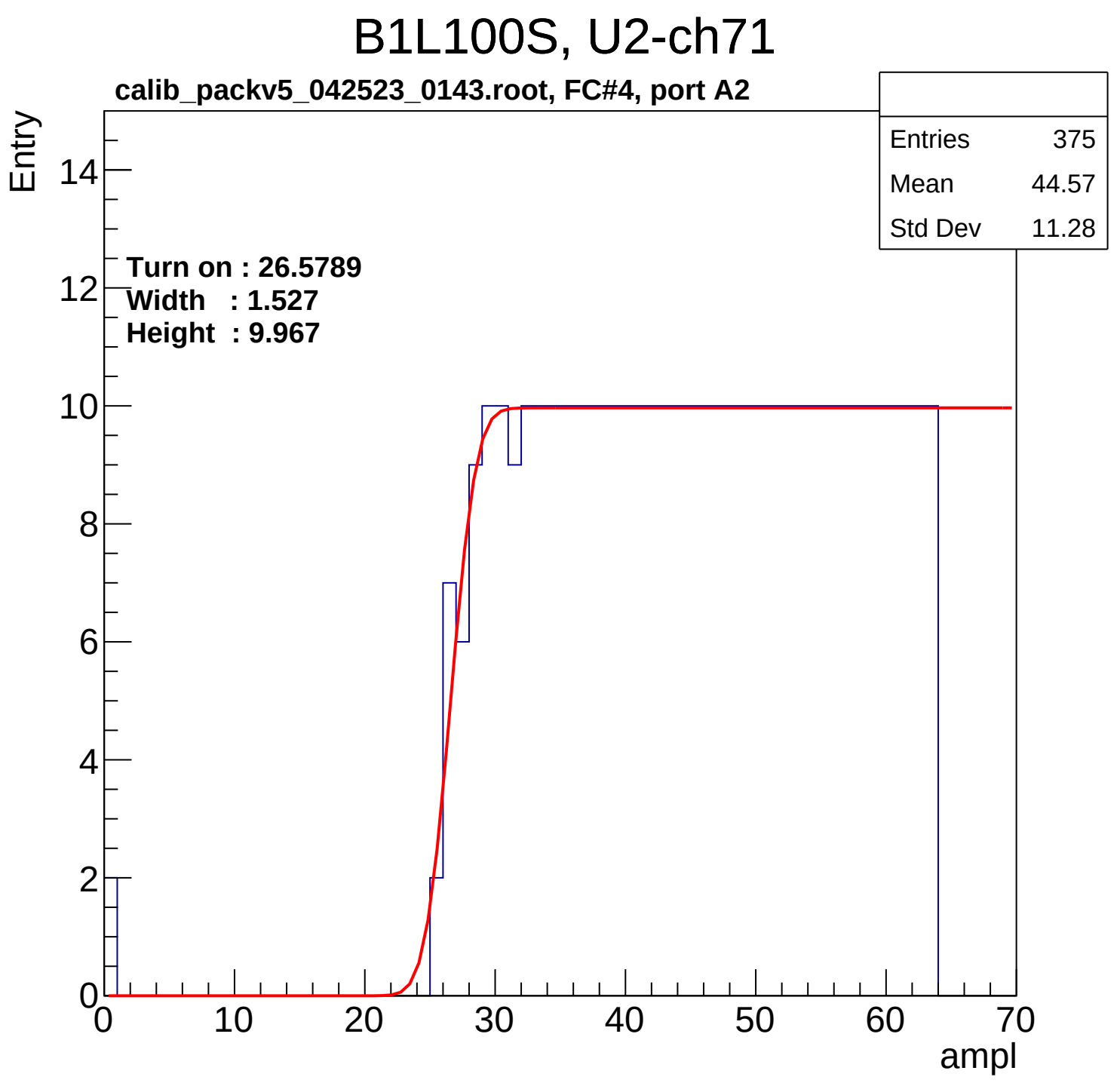
B1L100S, U2-ch71
calib_packv5_042523_0143.root, FC#4, port A2
Entries 375
Mean 44.57
Std Dev 11.28
Turn on : 26.5789
Width : 1.527
Height : 9.967
Entry
ampl
0
2
4
6
8
10
12
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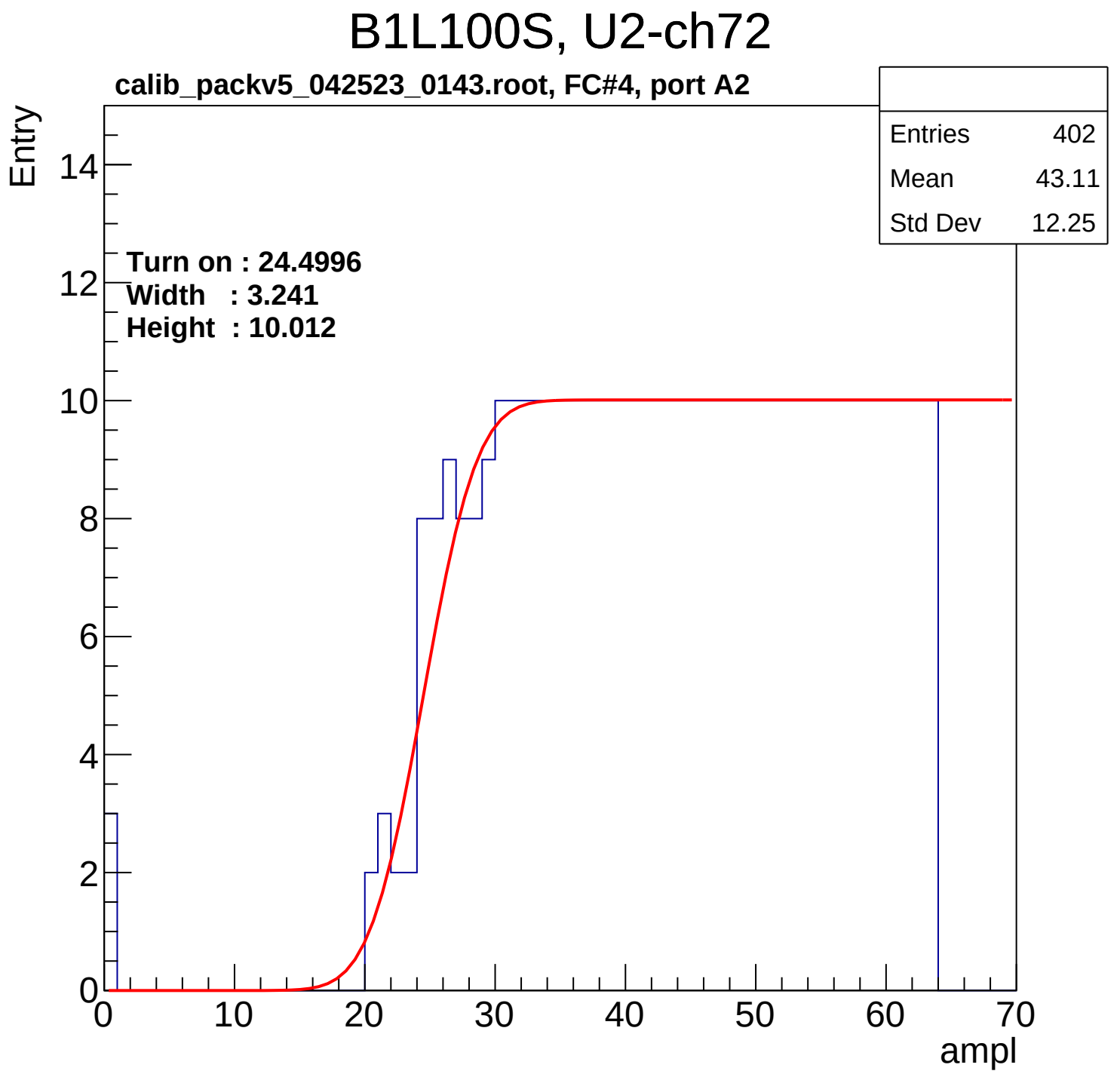
B1L100S, U2-ch72
calib_packv5_042523_0143.root, FC#4, port A2
Entries 402
Mean 43.11
Std Dev 12.25
Turn on : 24.4996
Width : 3.241
Height : 10.012
Entry
ampl
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6
8
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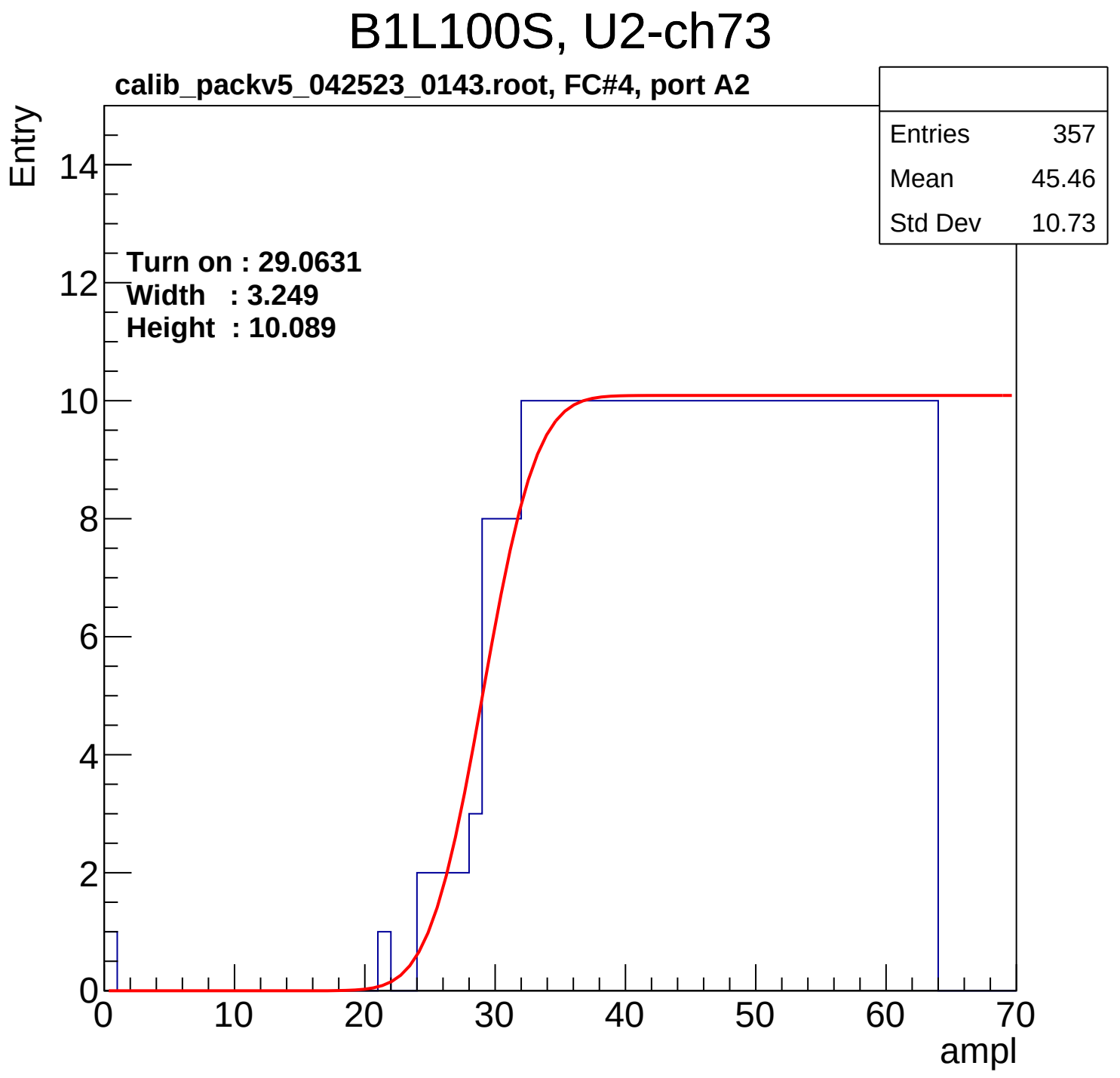
B1L100S, U2-ch73
calib_packv5_042523_0143.root, FC#4, port A2
Entries 357
Mean 45.46
Std Dev 10.73
Turn on : 29.0631
Width : 3.249
Height : 10.089
Entry
ampl
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6
8
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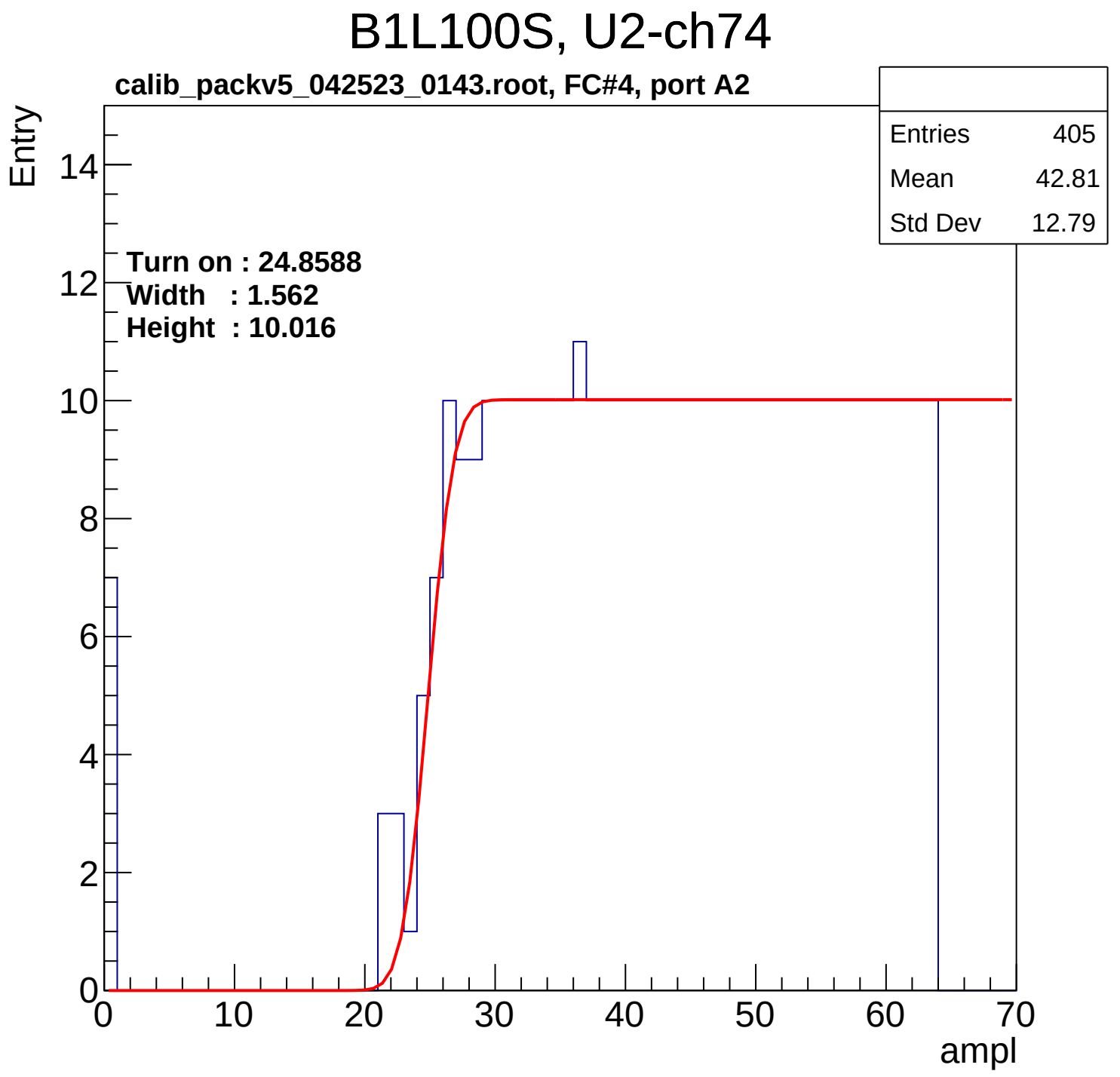
B1L100S, U2-ch74
calib_packv5_042523_0143.root, FC#4, port A2
Entries 405
Mean 42.81
Std Dev 12.79
Turn on : 24.8588
Width : 1.562
Height : 10.016
Entry
ampl
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8
10
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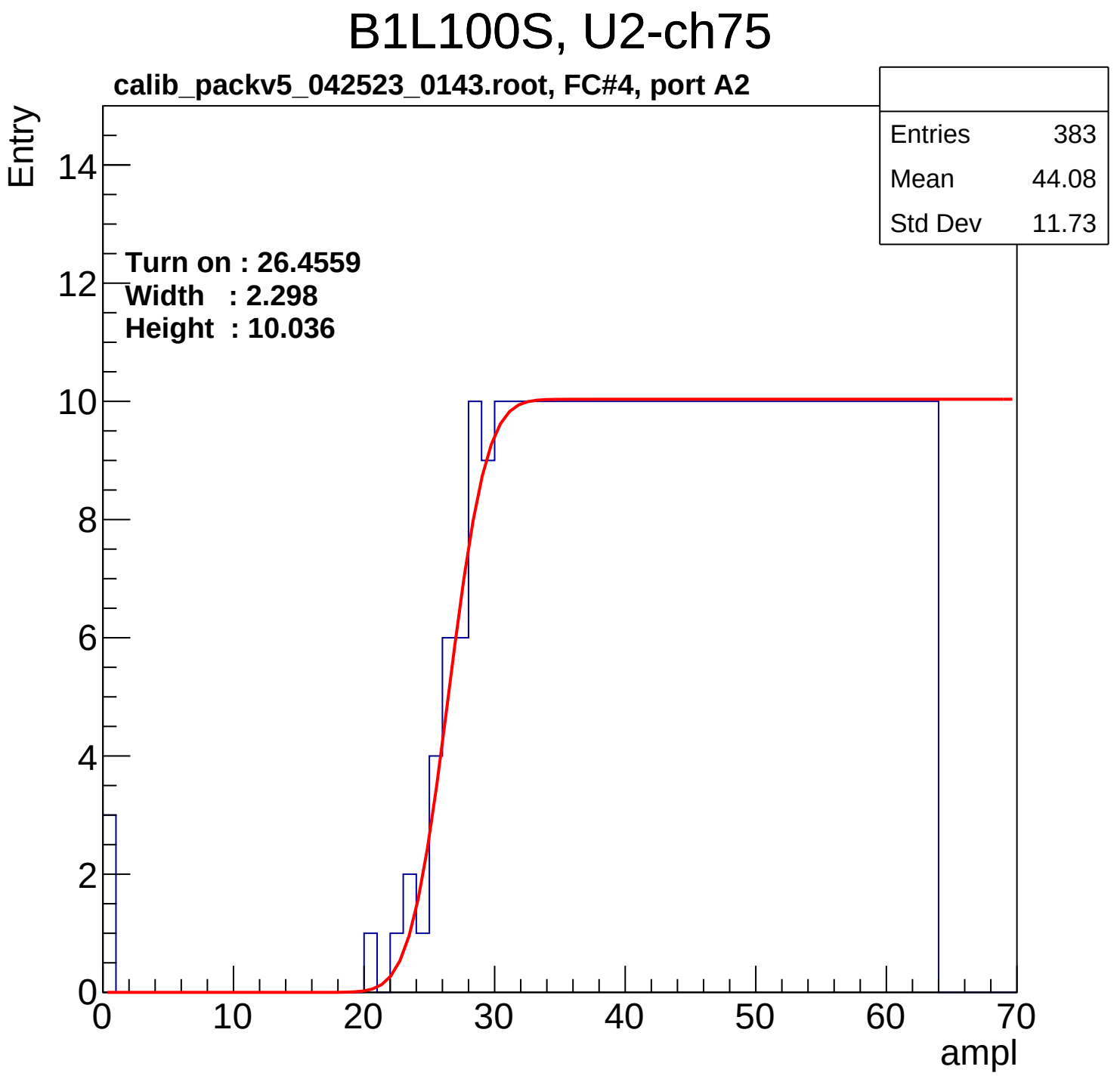
B1L100S, U2-ch75
calib_packv5_042523_0143.root, FC#4, port A2
Entries 383
Mean 44.08
Std Dev 11.73
Turn on : 26.4559
Width : 2.298
Height : 10.036
Entry
ampl
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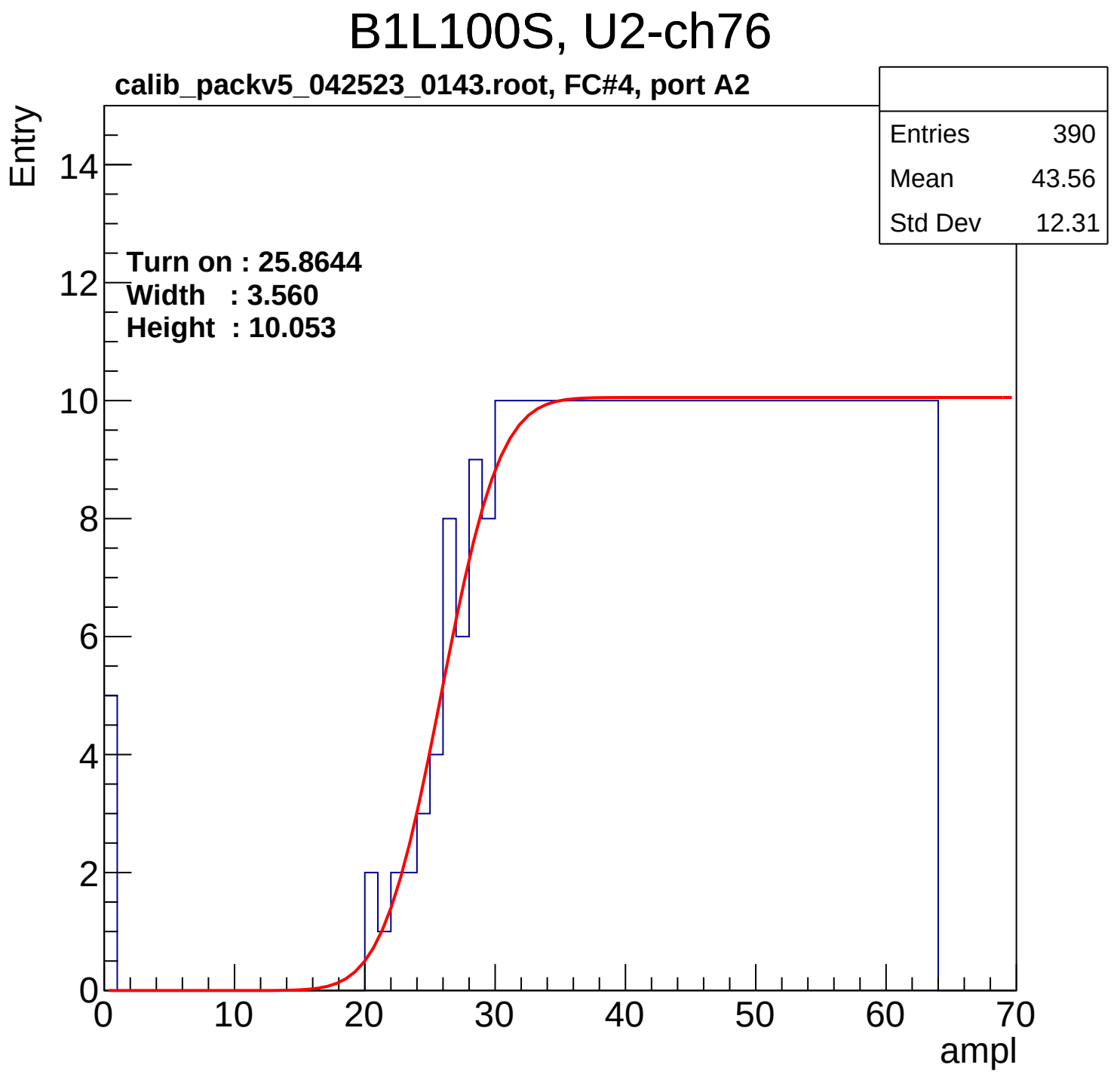
B1L100S, U2-ch76
calib_packv5_042523_0143.root, FC#4, port A2
Entries 390
Mean 43.56
Std Dev 12.31
Turn on : 25.8644
Width : 3.560
Height : 10.053
Entry
ampl
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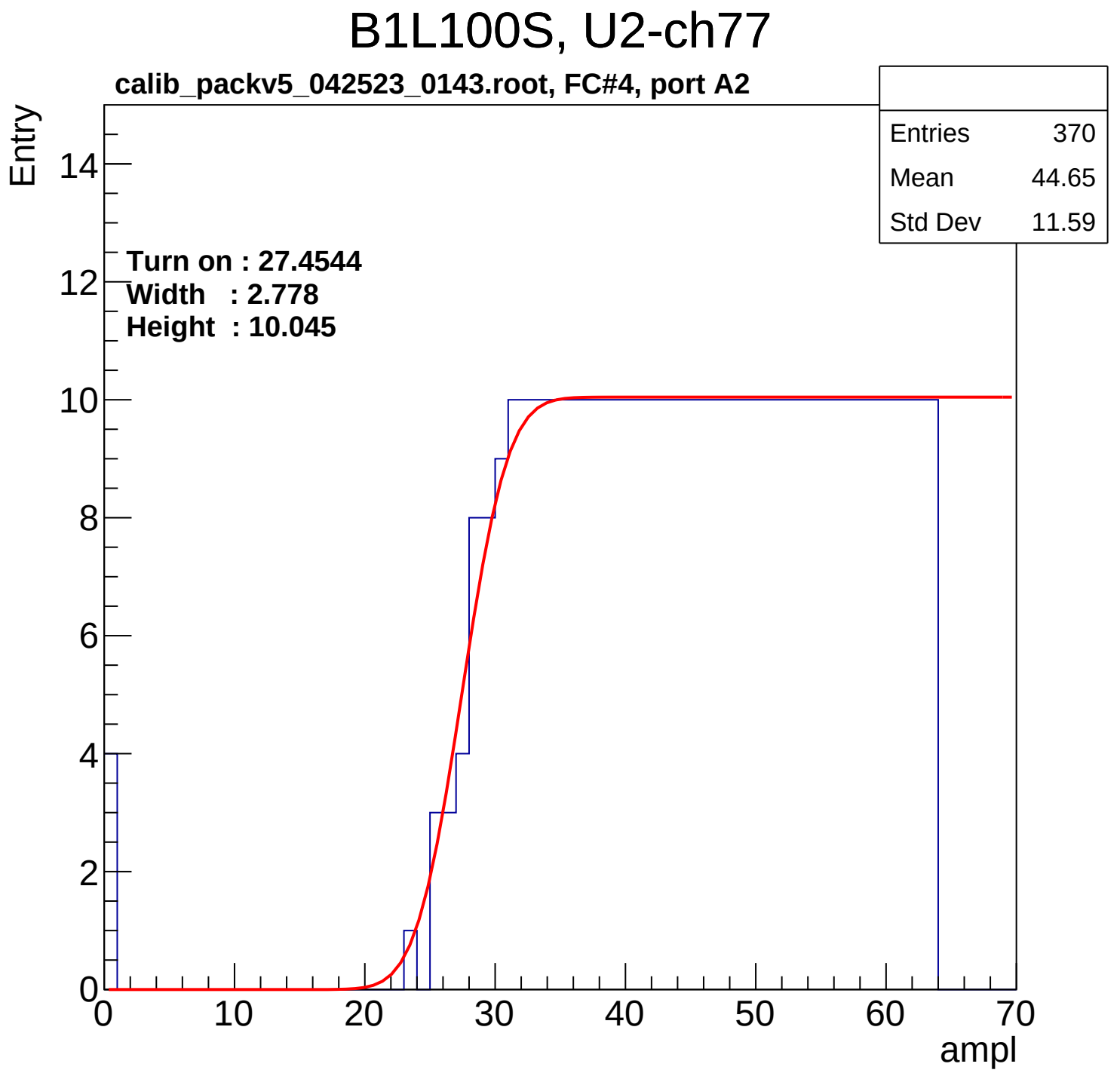
B1L100S, U2-ch77
calib_packv5_042523_0143.root, FC#4, port A2
Entries 370
Mean 44.65
Std Dev 11.59
Turn on : 27.4544
Width : 2.778
Height : 10.045
Entry
ampl
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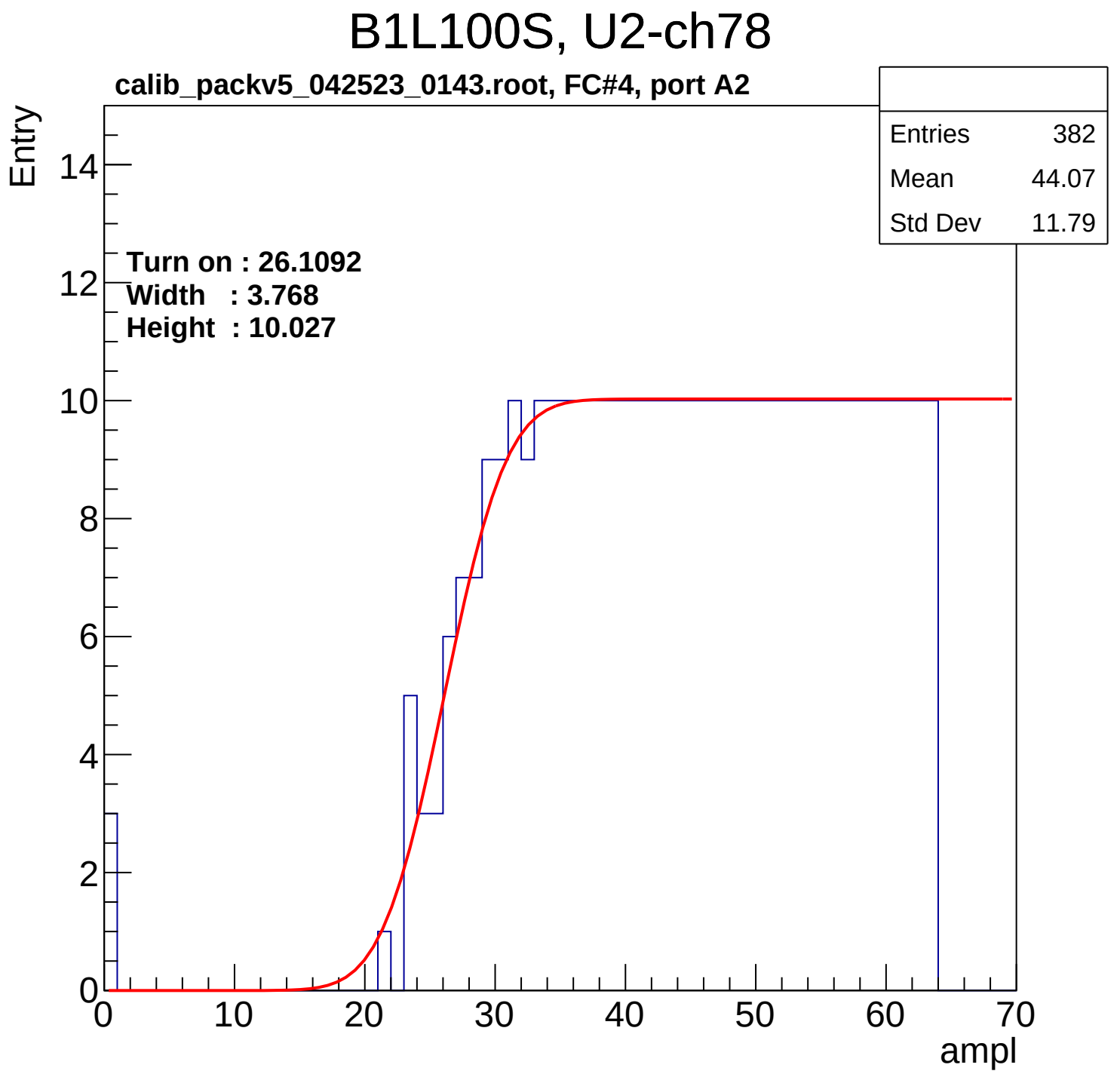
B1L100S, U2-ch78
calib_packv5_042523_0143.root, FC#4, port A2
Entries 382
Mean 44.07
Std Dev 11.79
Turn on : 26.1092
Width : 3.768
Height : 10.027
Entry
ampl
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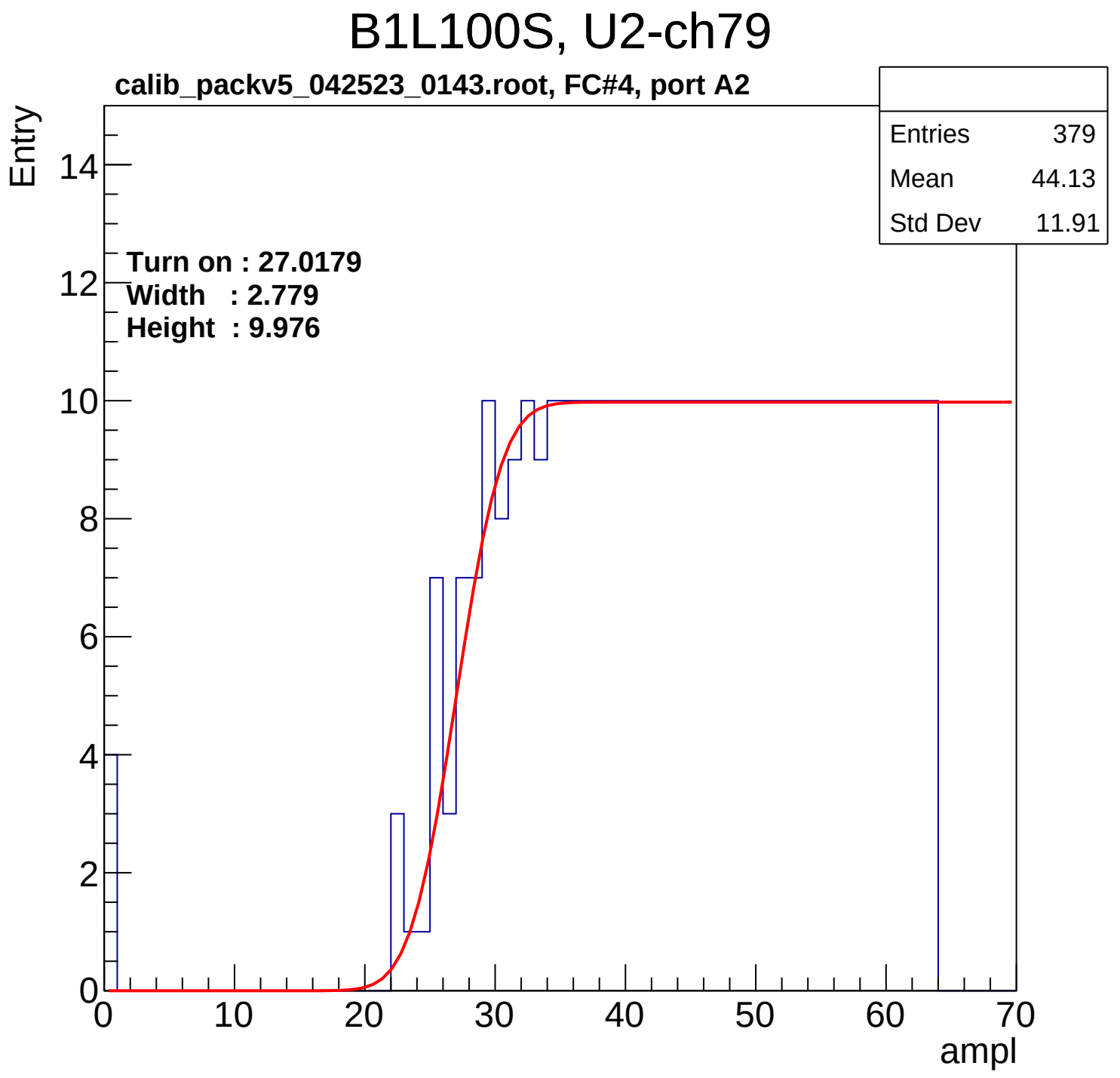
B1L100S, U2-ch79
calib_packv5_042523_0143.root, FC#4, port A2
Entries 379
Mean 44.13
Std Dev 11.91
Turn on : 27.0179
Width : 2.779
Height : 9.976
Entry
ampl
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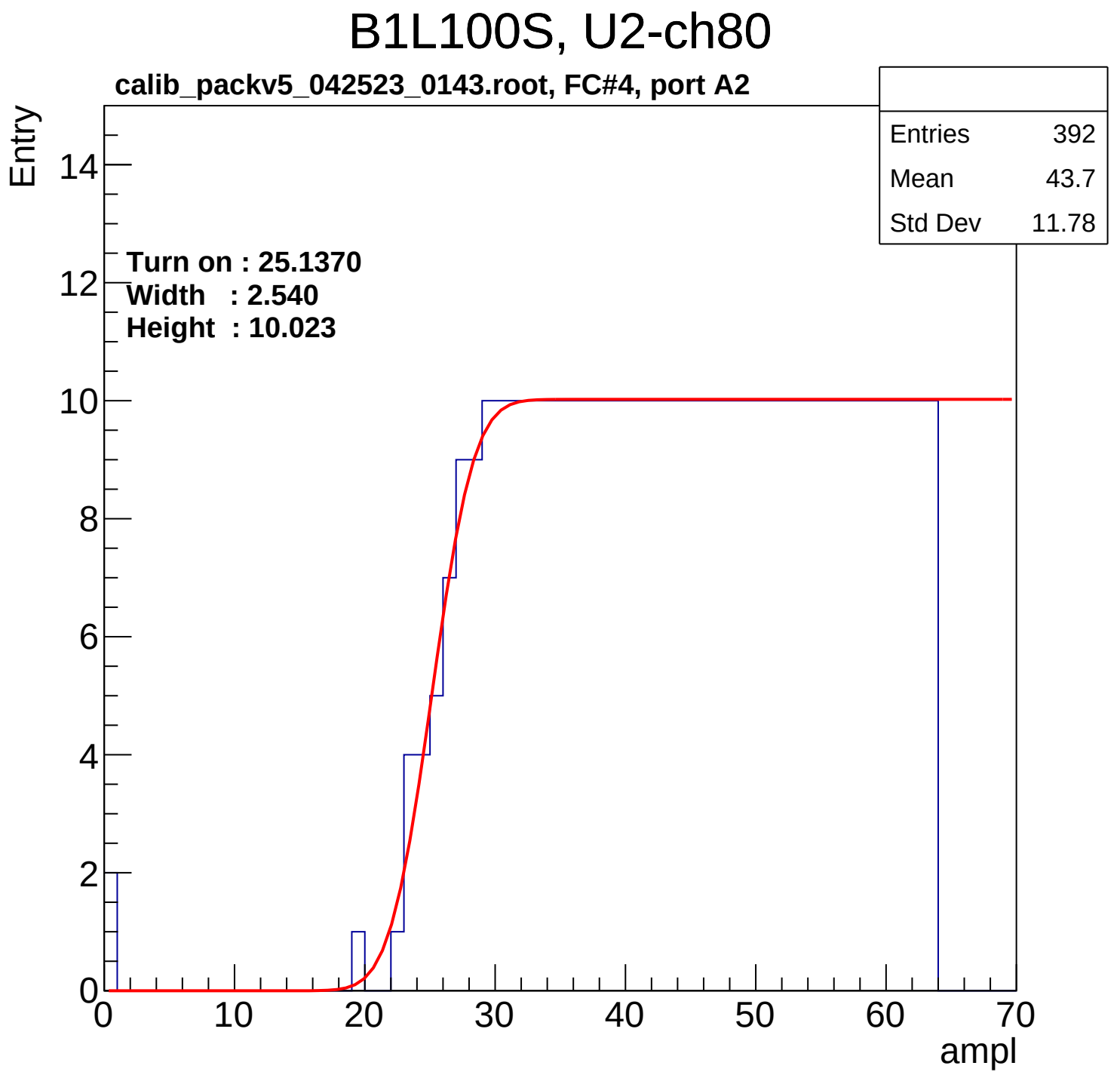
B1L100S, U2-ch80
calib_packv5_042523_0143.root, FC#4, port A2
Entries 392
Mean 43.7
Std Dev 11.78
Turn on : 25.1370
Width : 2.540
Height : 10.023
Entry
ampl
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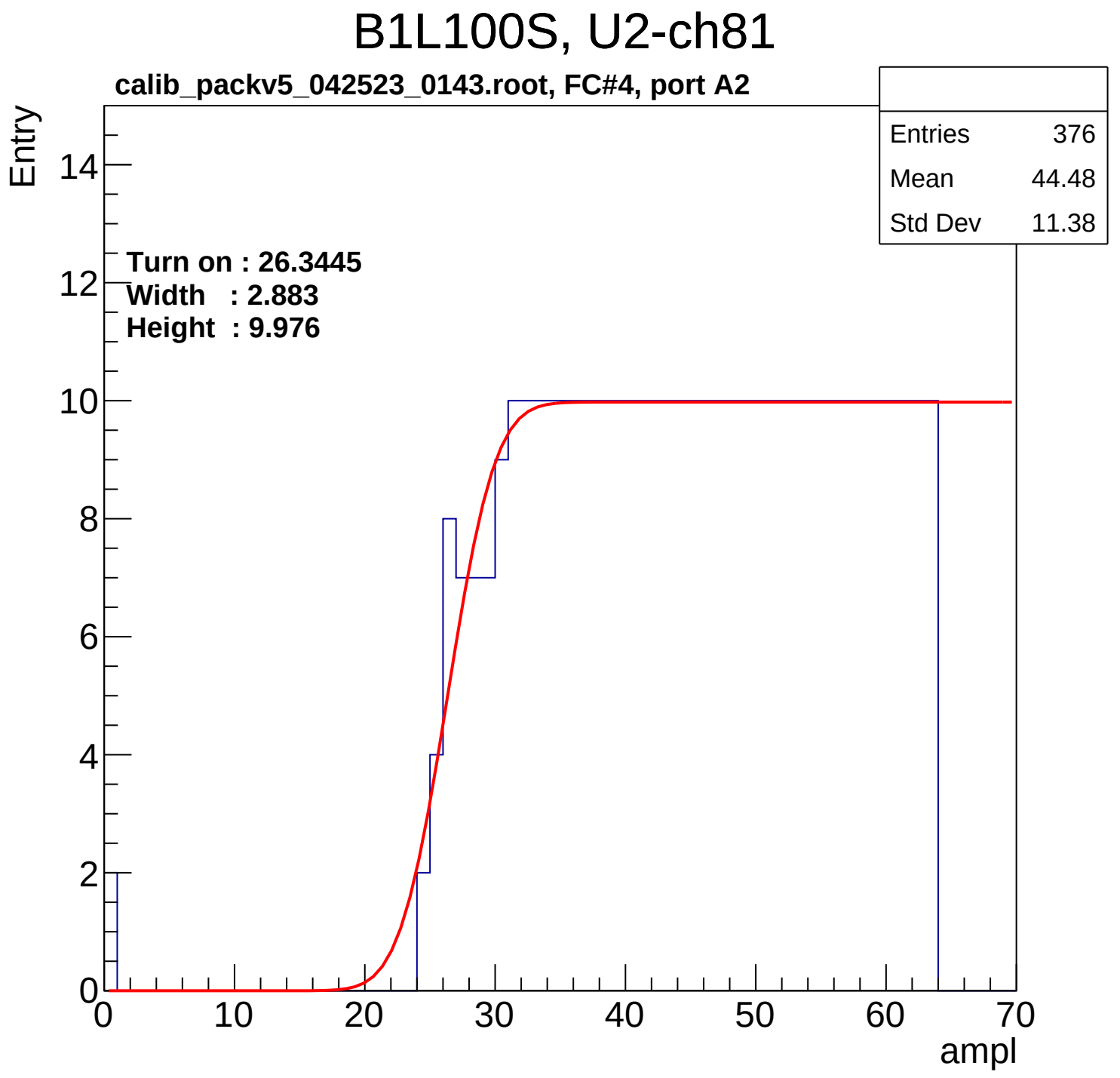
B1L100S, U2-ch81
calib_packv5_042523_0143.root, FC#4, port A2
Entries 376
Mean 44.48
Std Dev 11.38
Turn on : 26.3445
Width : 2.883
Height : 9.976
Entry
ampl
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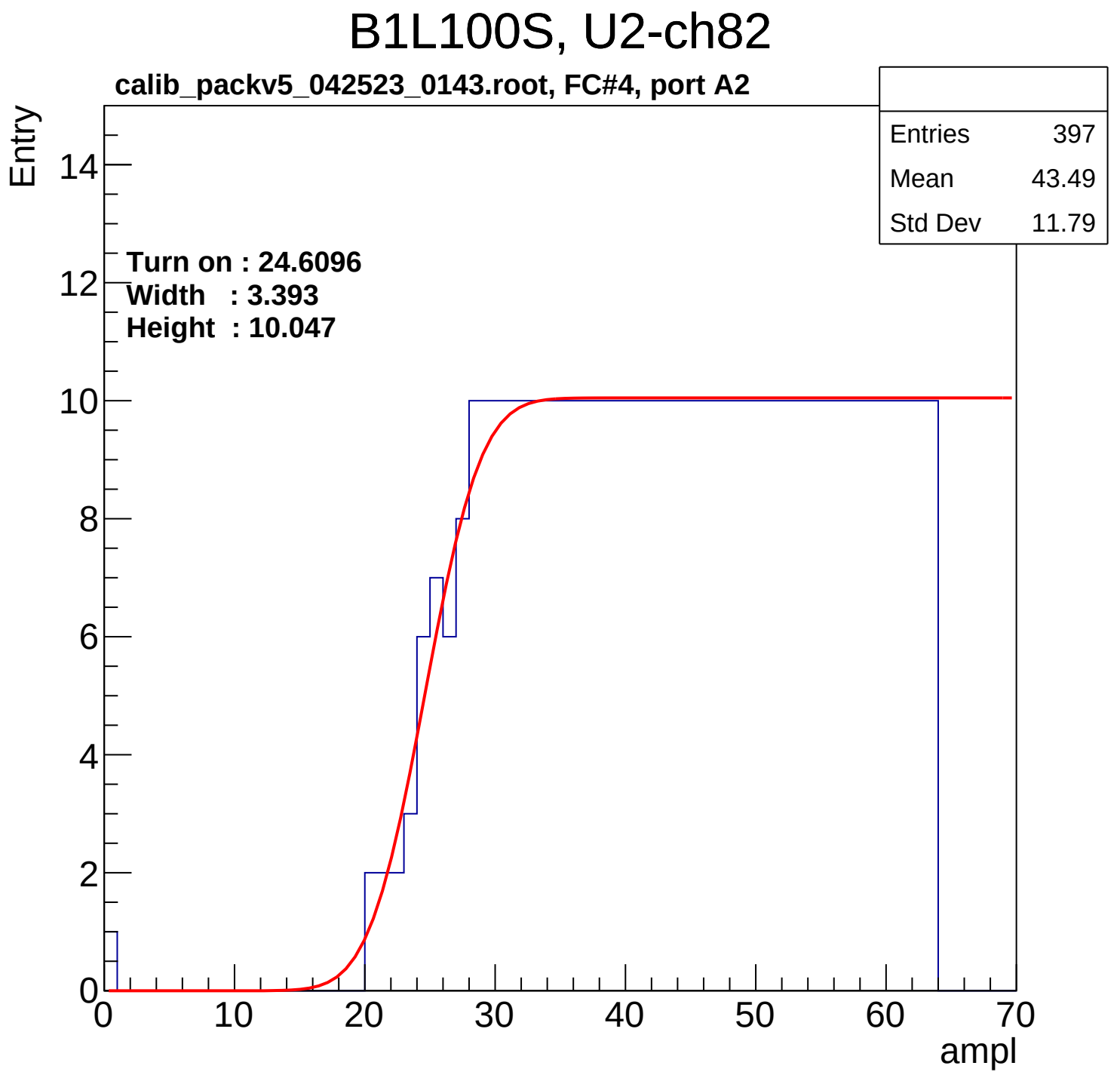
B1L100S, U2-ch82
calib_packv5_042523_0143.root, FC#4, port A2
Entries 397
Mean 43.49
Std Dev 11.79
Turn on : 24.6096
Width : 3.393
Height : 10.047
Entry
ampl
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6
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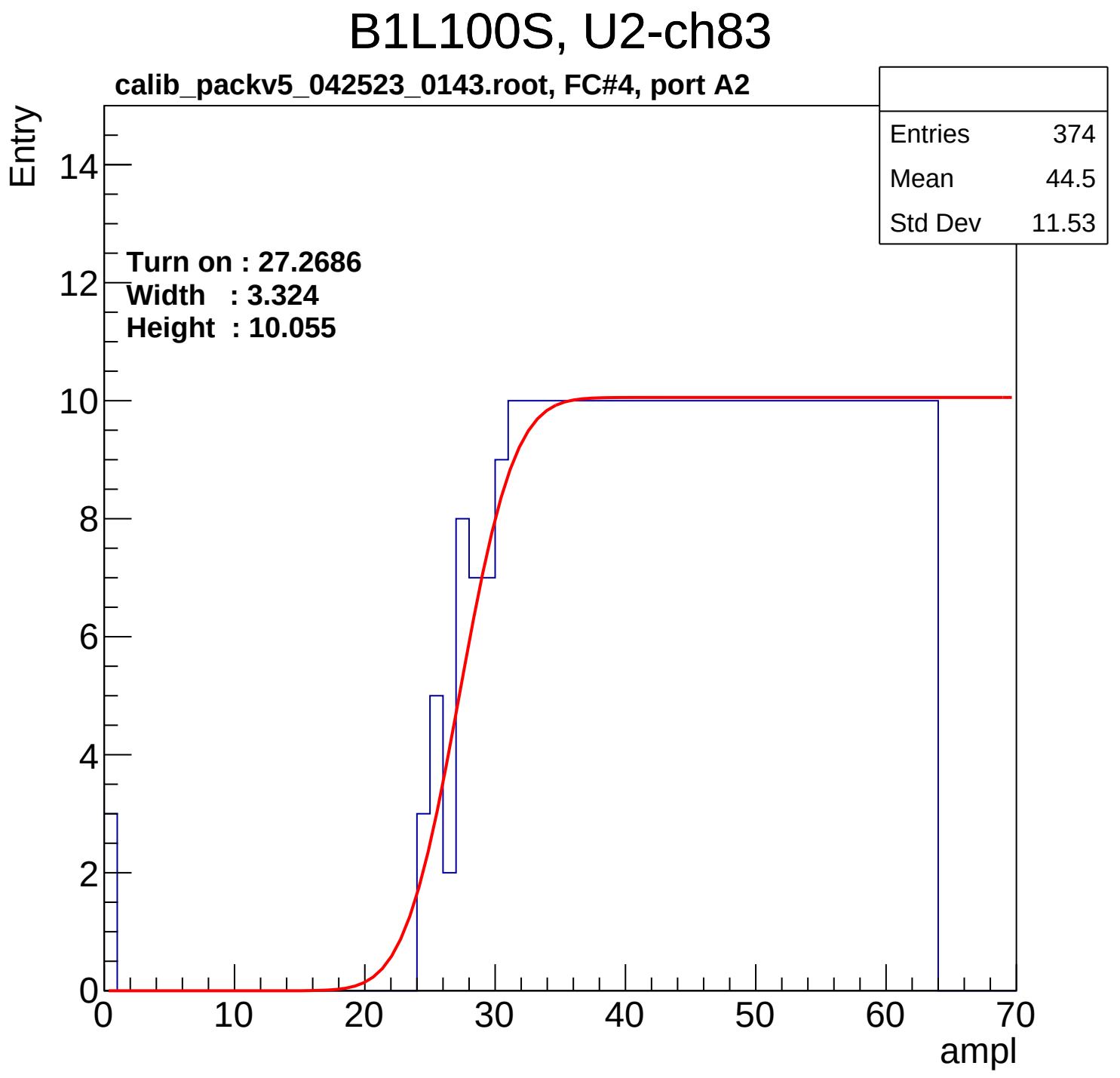
B1L100S, U2-ch83
calib_packv5_042523_0143.root, FC#4, port A2
Entries 374
Mean 44.5
Std Dev 11.53
Turn on : 27.2686
Width : 3.324
Height : 10.055
Entry
ampl
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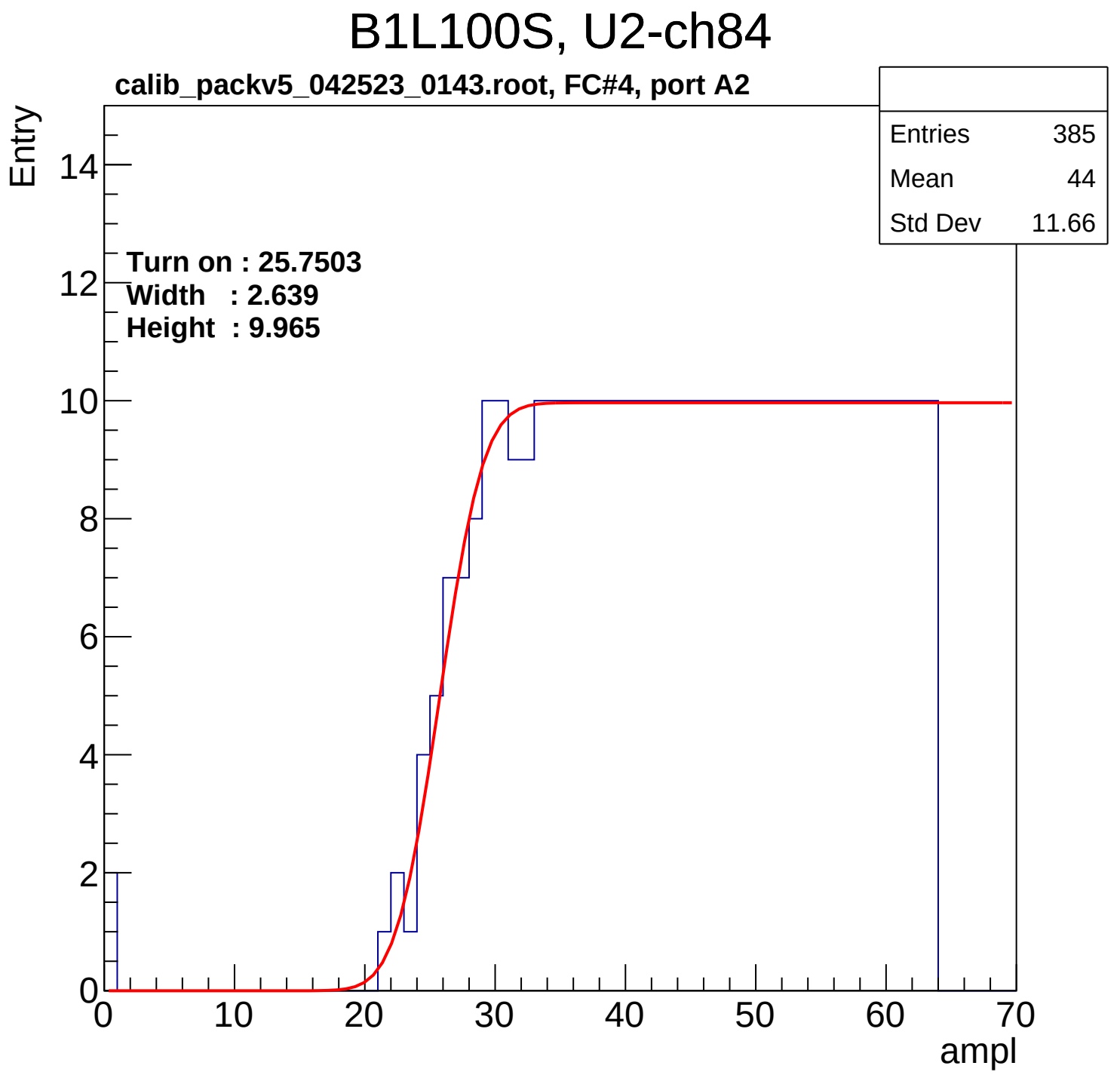
B1L100S, U2-ch84
calib_packv5_042523_0143.root, FC#4, port A2
Entries 385
Mean 44
Std Dev 11.66
Turn on : 25.7503
Width : 2.639
Height : 9.965
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ampl
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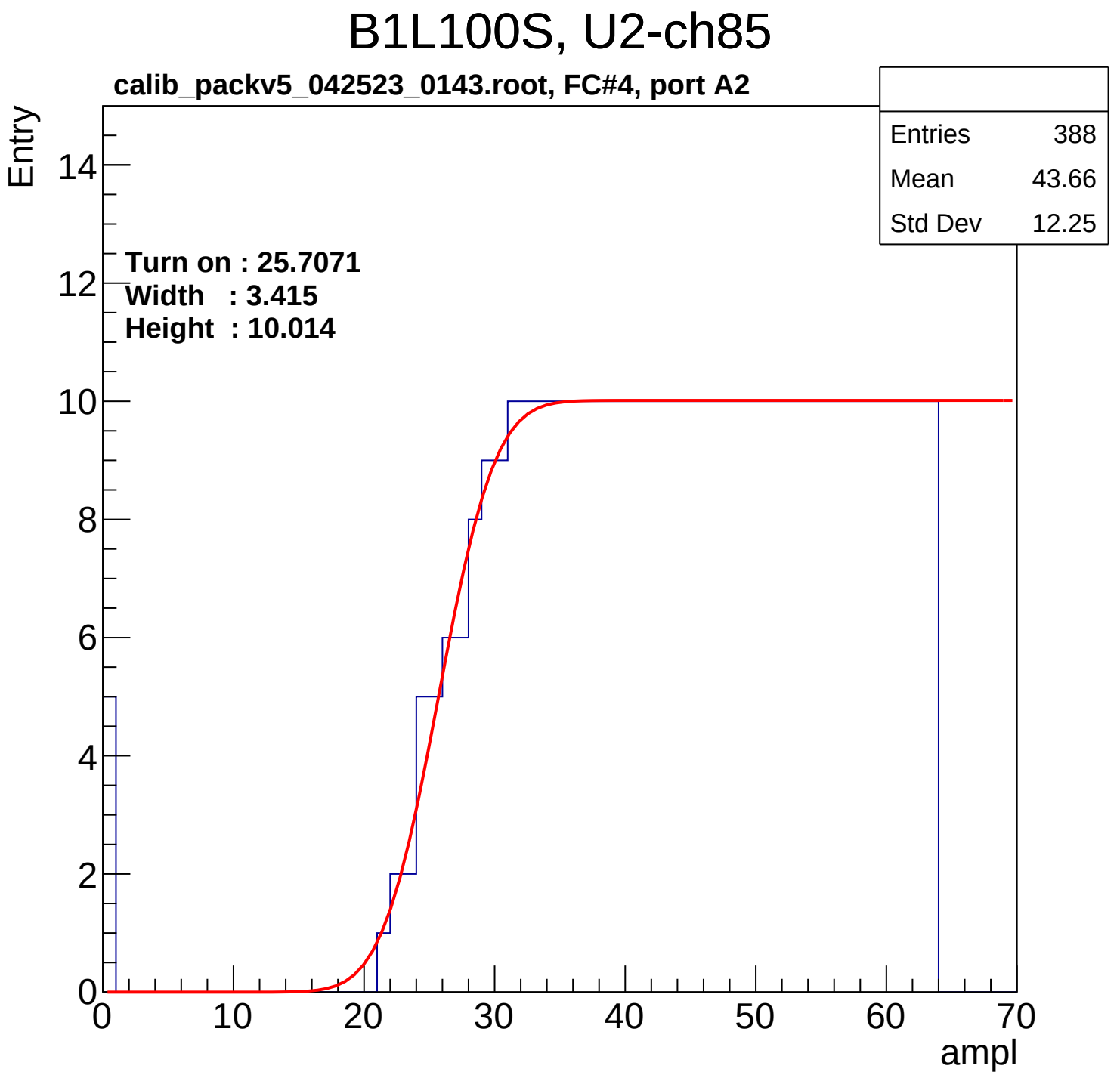
B1L100S, U2-ch85
calib_packv5_042523_0143.root, FC#4, port A2
Entries 388
Mean 43.66
Std Dev 12.25
Turn on : 25.7071
Width : 3.415
Height : 10.014
Entry
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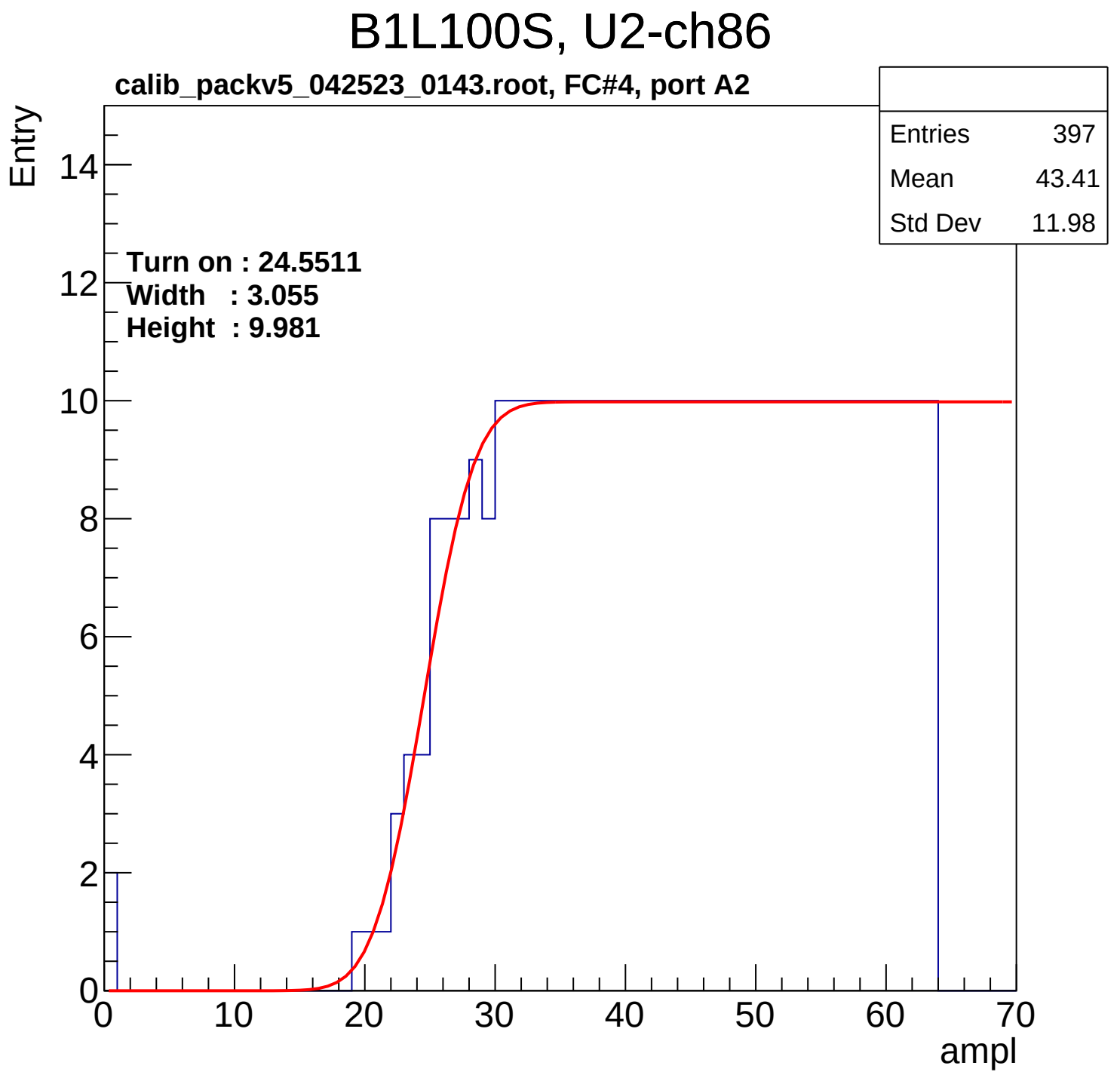
B1L100S, U2-ch86
calib_packv5_042523_0143.root, FC#4, port A2
Entries 397
Mean 43.41
Std Dev 11.98
Turn on : 24.5511
Width : 3.055
Height : 9.981
Entry
ampl
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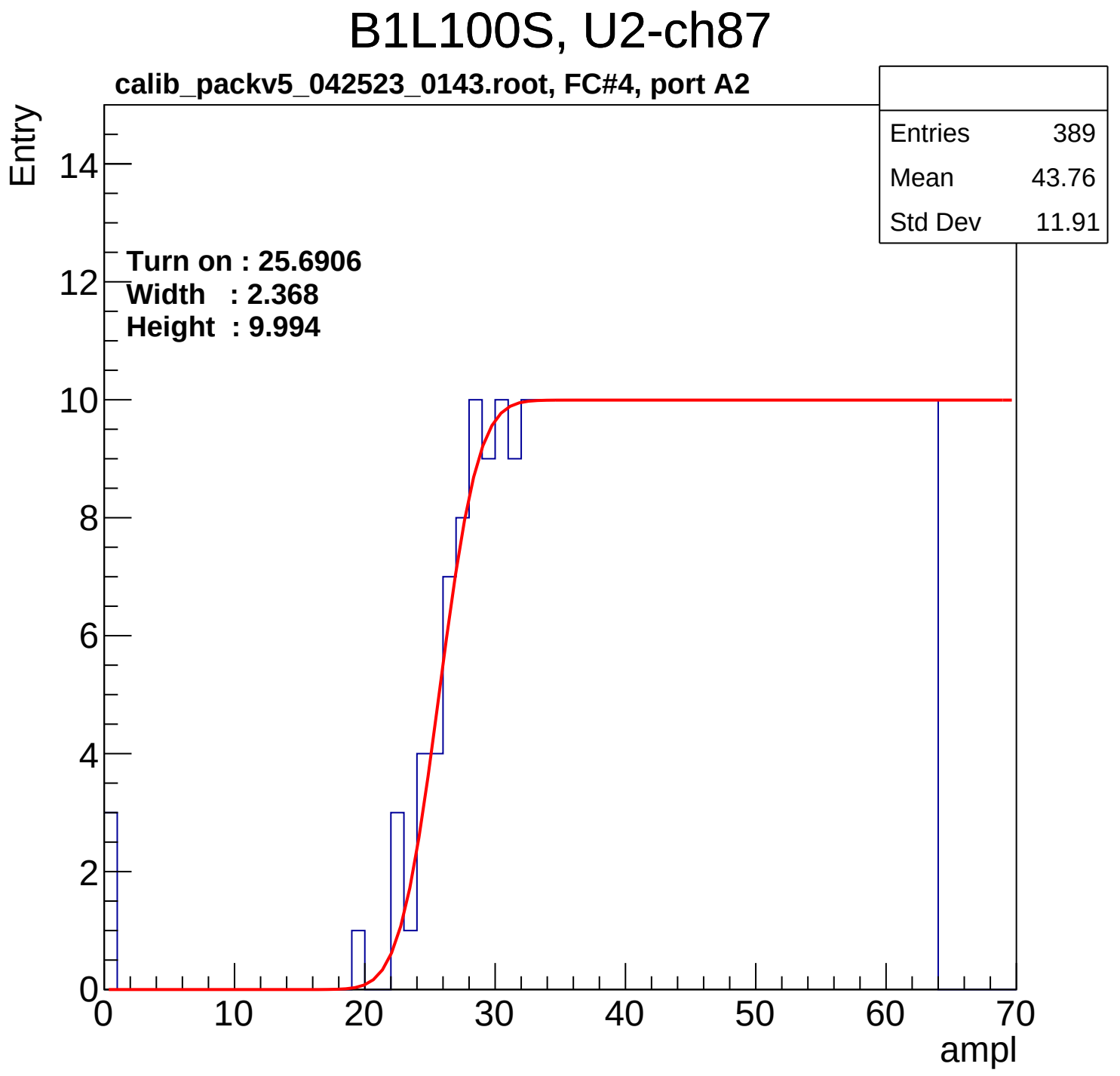
B1L100S, U2-ch87
calib_packv5_042523_0143.root, FC#4, port A2
Entries 389
Mean 43.76
Std Dev 11.91
Turn on : 25.6906
Width : 2.368
Height : 9.994
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ampl
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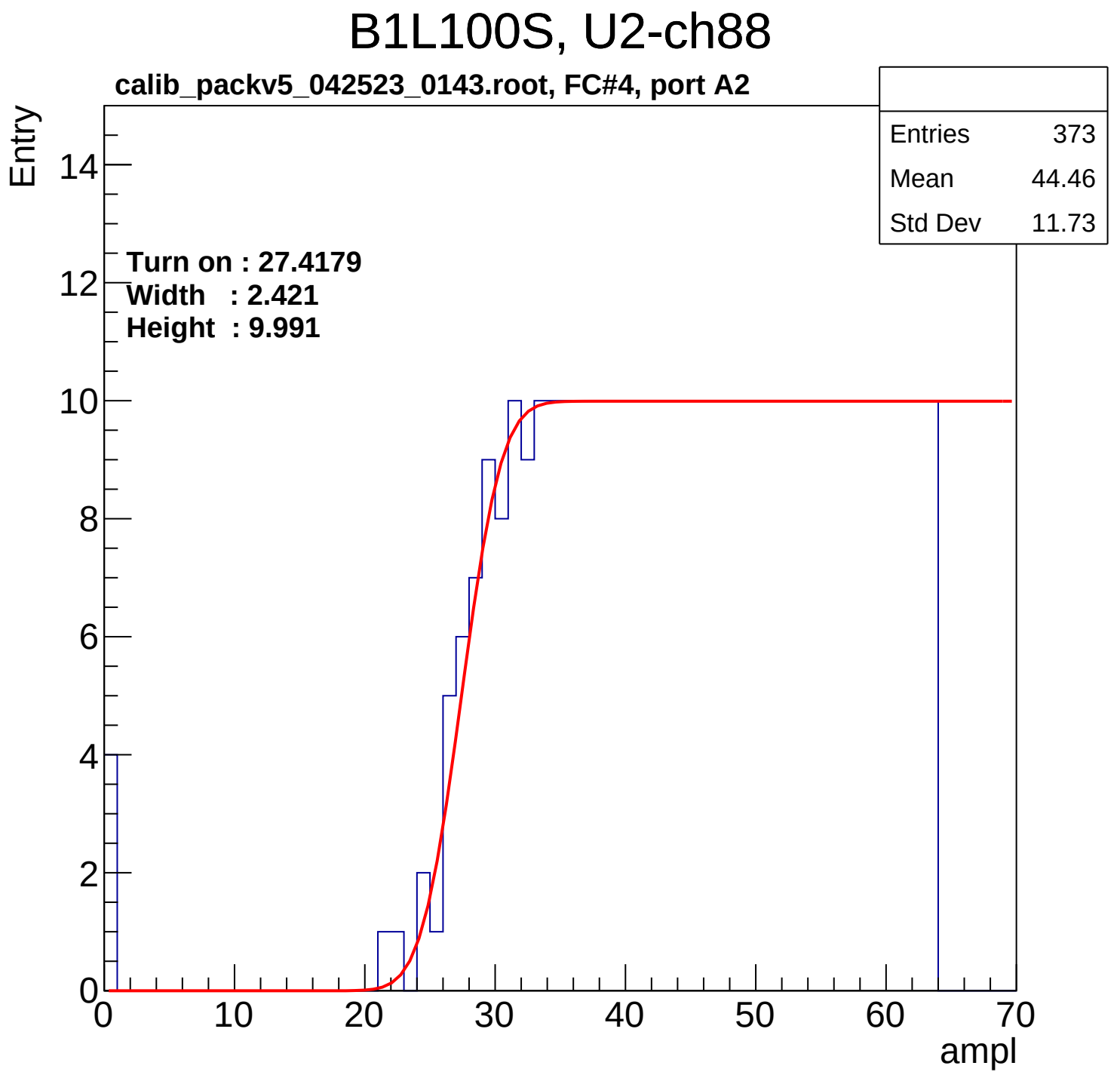
B1L100S, U2-ch88
calib_packv5_042523_0143.root, FC#4, port A2
Entries 373
Mean 44.46
Std Dev 11.73
Turn on : 27.4179
Width : 2.421
Height : 9.991
Entry
ampl
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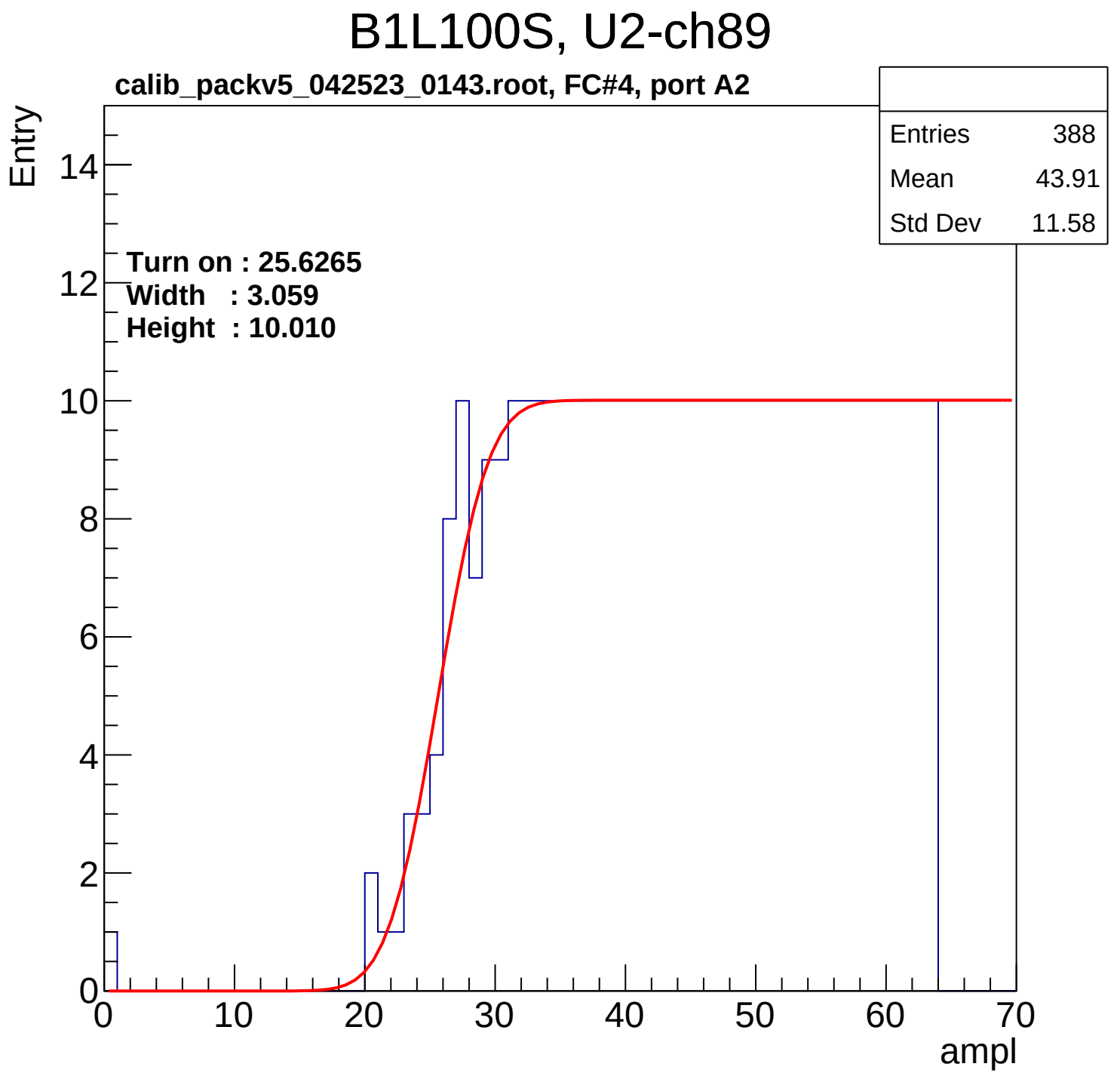
B1L100S, U2-ch89
calib_packv5_042523_0143.root, FC#4, port A2
Entries 388
Mean 43.91
Std Dev 11.58
Turn on : 25.6265
Width : 3.059
Height : 10.010
Entry
ampl
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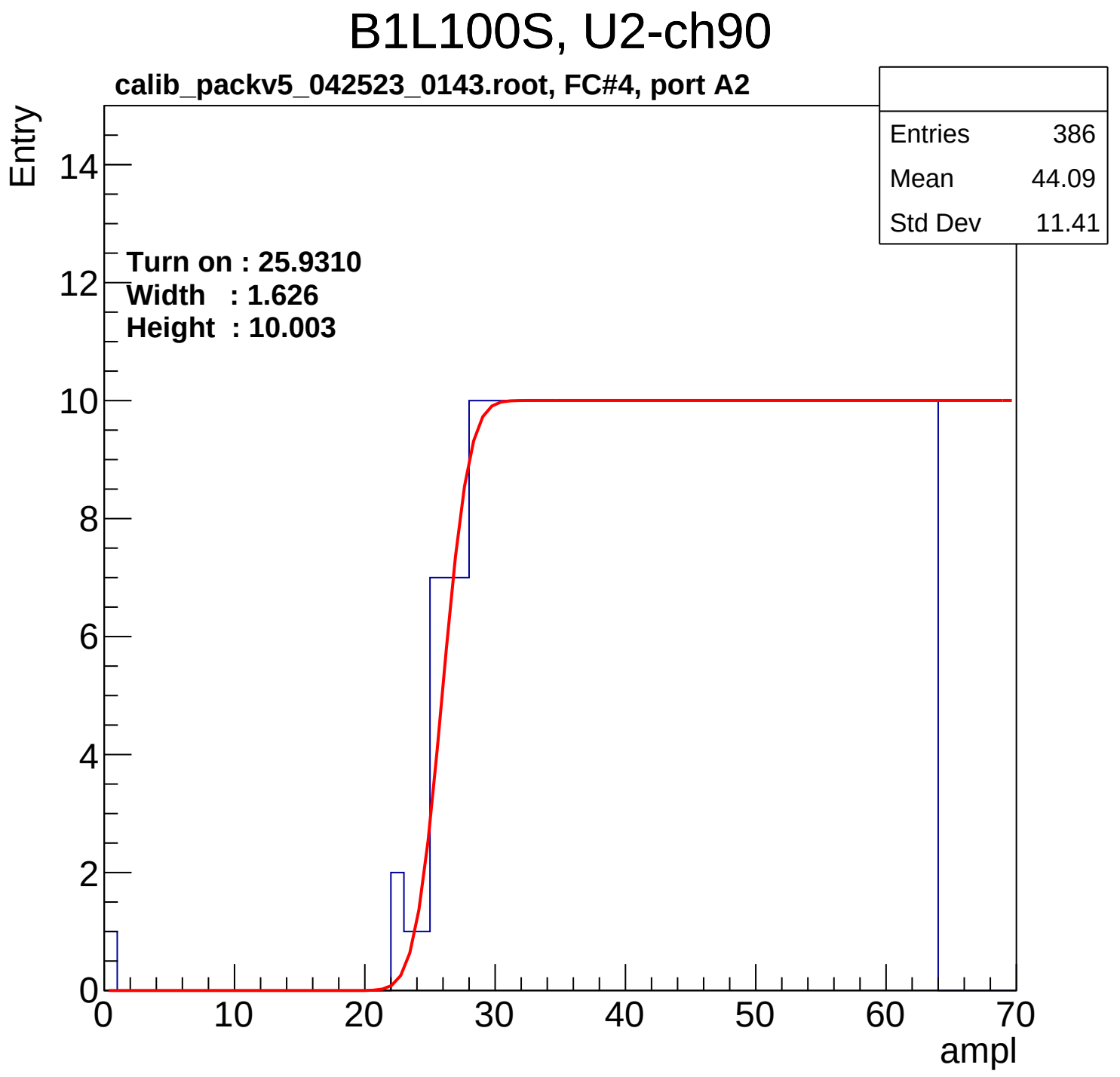
B1L100S, U2-ch90
calib_packv5_042523_0143.root, FC#4, port A2
Entries 386
Mean 44.09
Std Dev 11.41
Turn on : 25.9310
Width : 1.626
Height : 10.003
Entry
ampl
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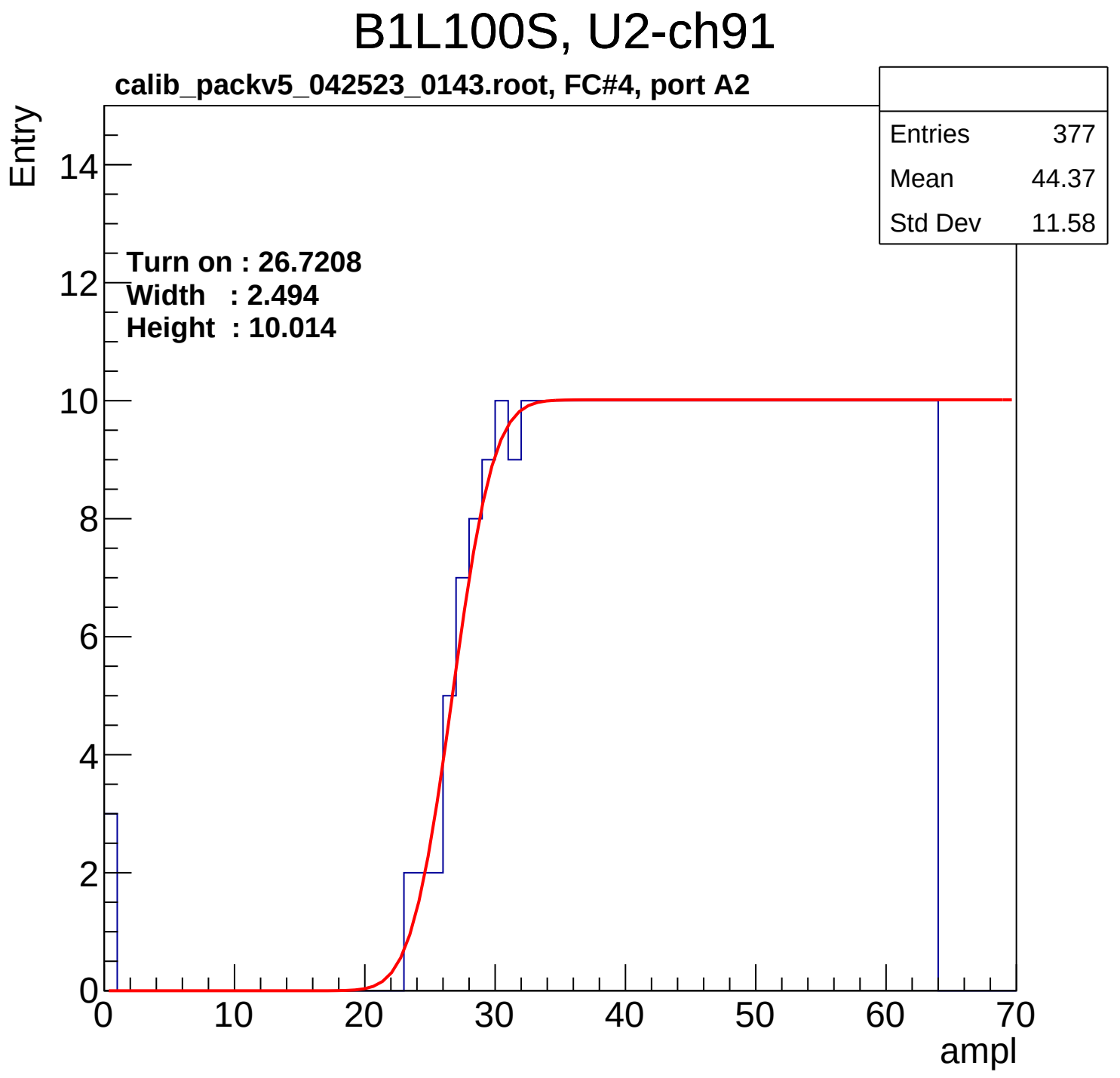
B1L100S, U2-ch91
calib_packv5_042523_0143.root, FC#4, port A2
Entries 377
Mean 44.37
Std Dev 11.58
Turn on : 26.7208
Width : 2.494
Height : 10.014
Entry
ampl
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2
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6
8
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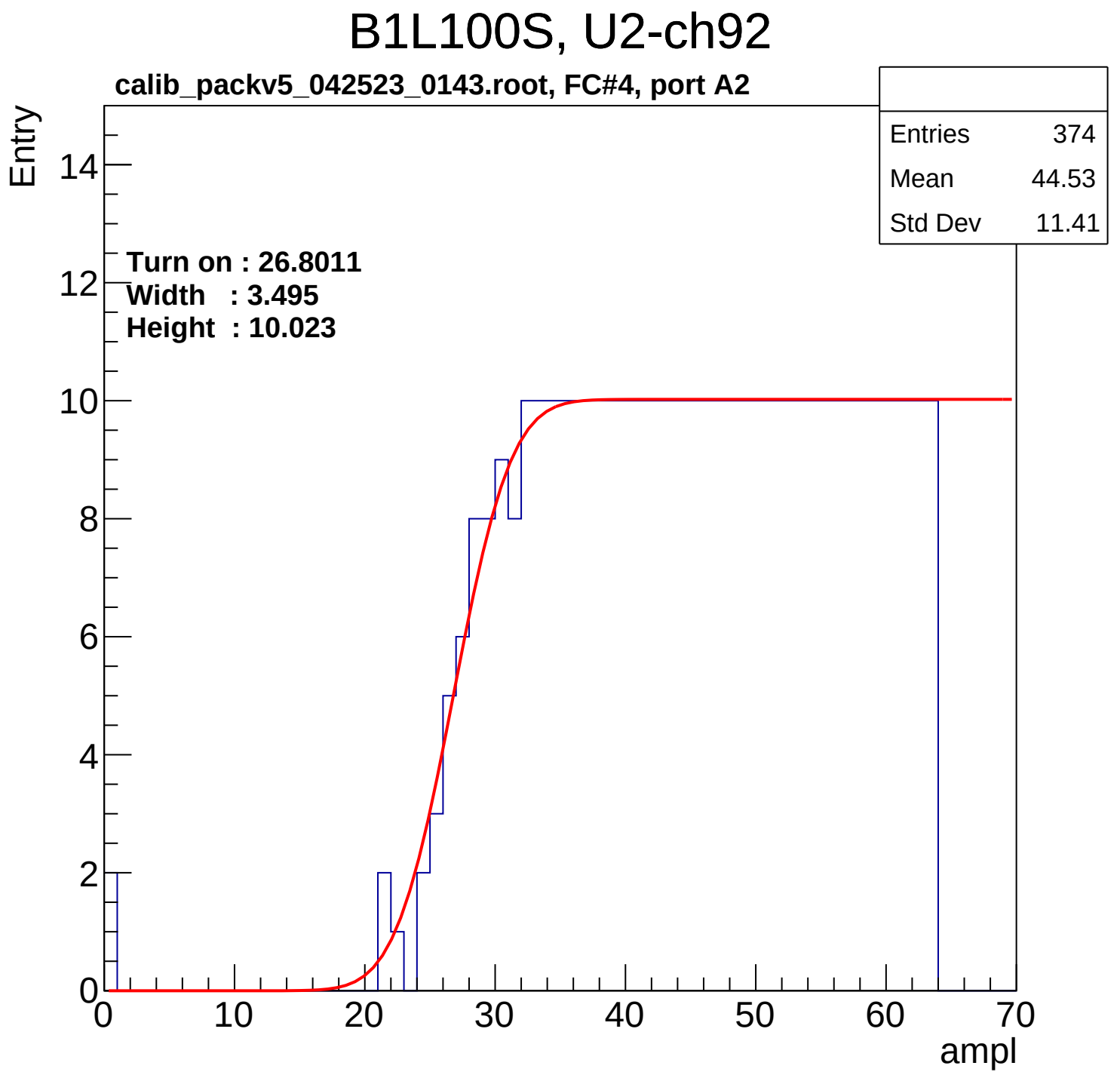
B1L100S, U2-ch92
calib_packv5_042523_0143.root, FC#4, port A2
Entries 374
Mean 44.53
Std Dev 11.41
Turn on : 26.8011
Width : 3.495
Height : 10.023
Entry
ampl
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8
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0
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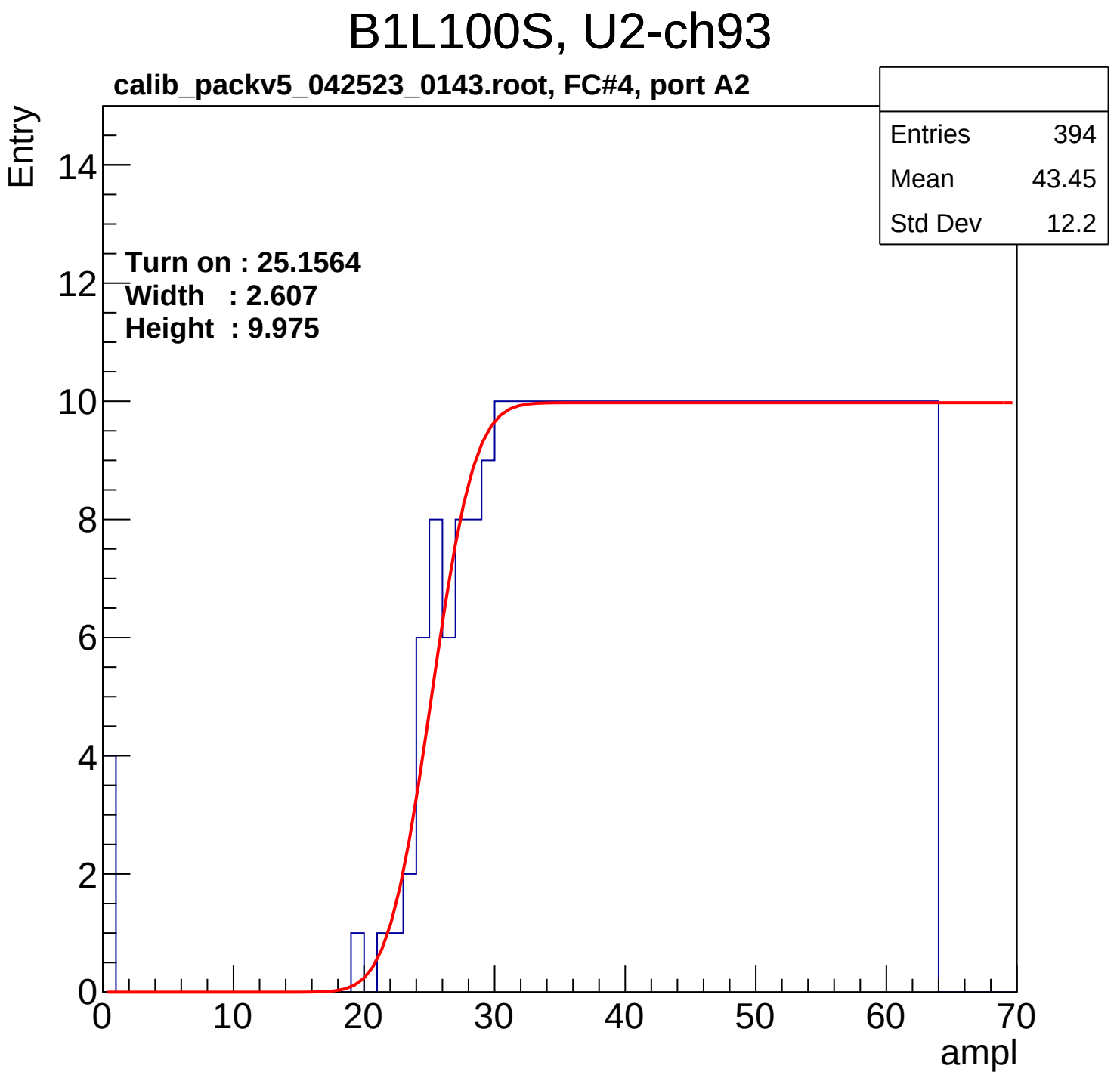
B1L100S, U2-ch93
calib_packv5_042523_0143.root, FC#4, port A2
Entries 394
Mean 43.45
Std Dev 12.2
Turn on : 25.1564
Width : 2.607
Height : 9.975
Entry
ampl
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6
8
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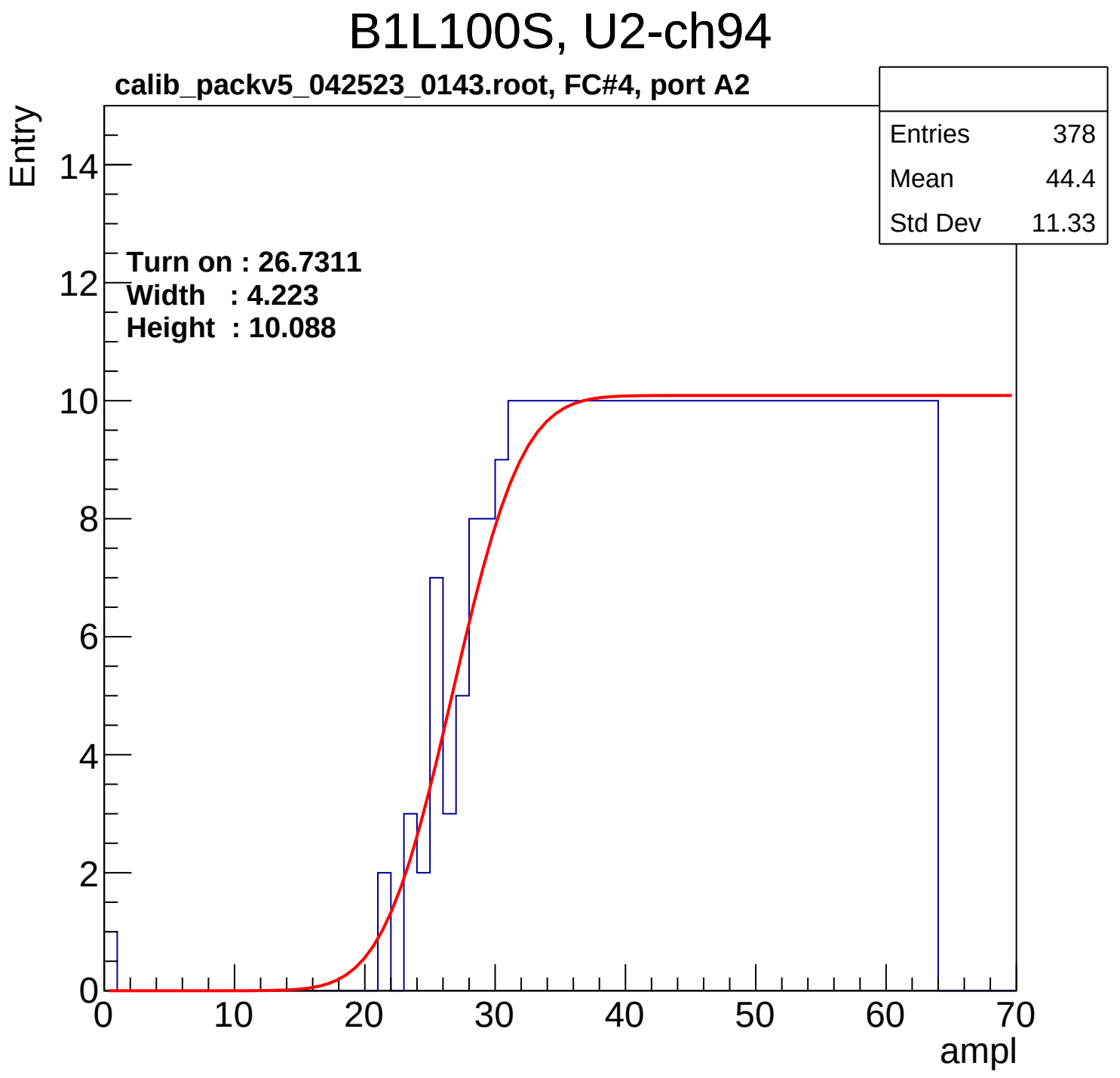
B1L100S, U2-ch94
calib_packv5_042523_0143.root, FC#4, port A2
Entries 378
Mean 44.4
Std Dev 11.33
Turn on : 26.7311
Width : 4.223
Height : 10.088
Entry
ampl
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6
8
10
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0
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60
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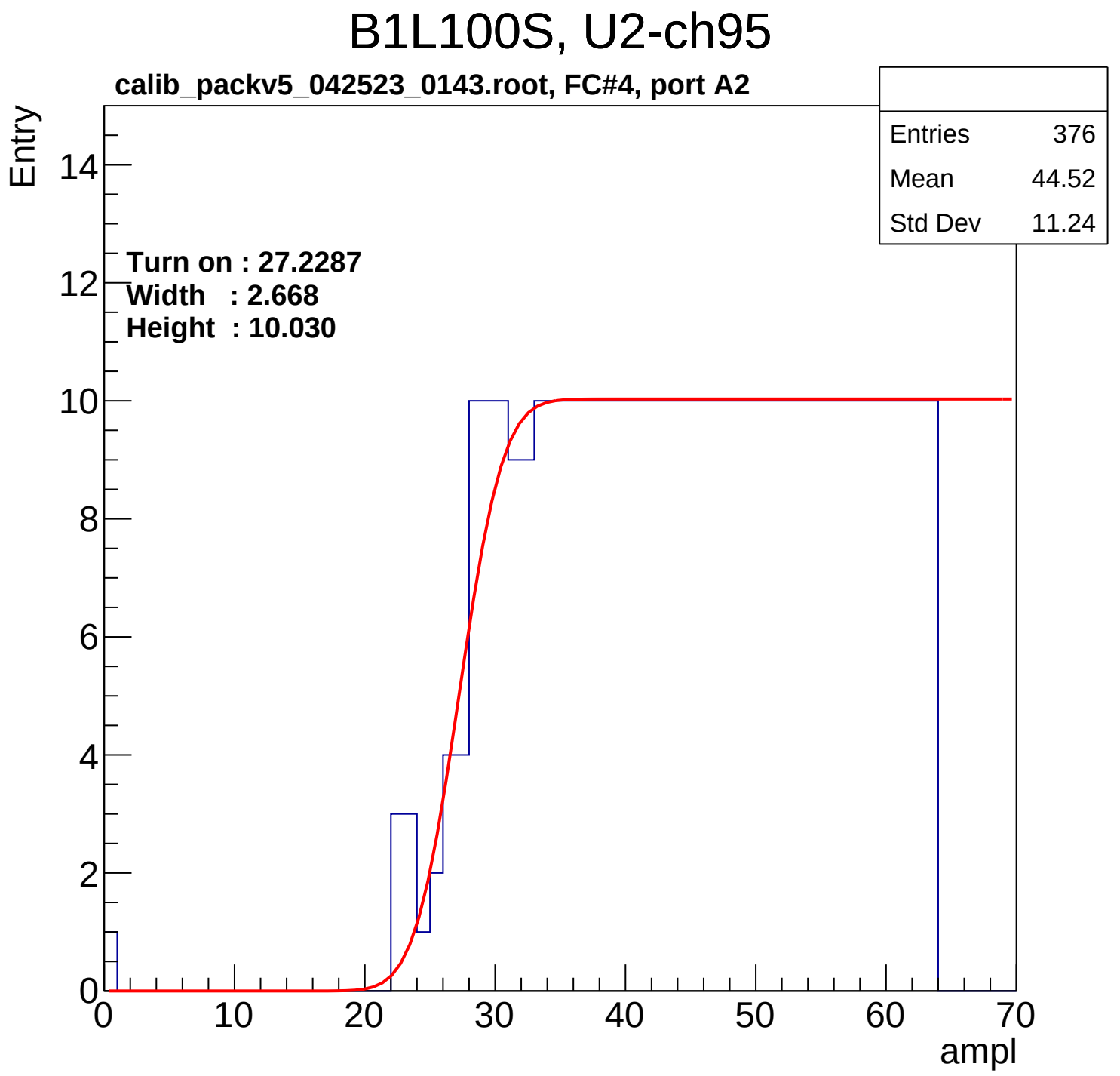
B1L100S, U2-ch95
calib_packv5_042523_0143.root, FC#4, port A2
Entries 376
Mean 44.52
Std Dev 11.24
Turn on : 27.2287
Width : 2.668
Height : 10.030
Entry
ampl
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2
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6
8
10
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0
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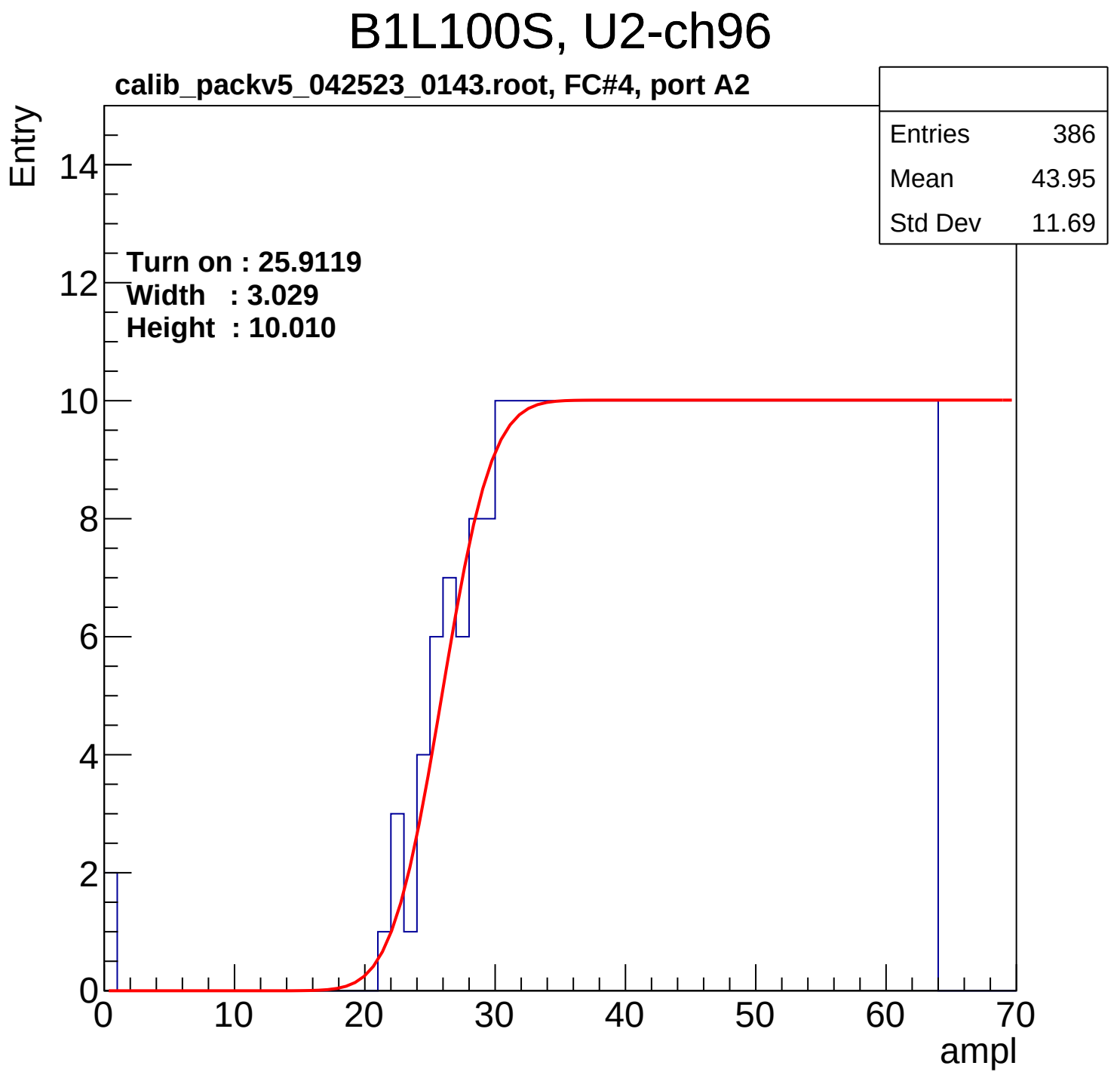
B1L100S, U2-ch96
calib_packv5_042523_0143.root, FC#4, port A2
Entries 386
Mean 43.95
Std Dev 11.69
Turn on : 25.9119
Width : 3.029
Height : 10.010
Entry
ampl
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6
8
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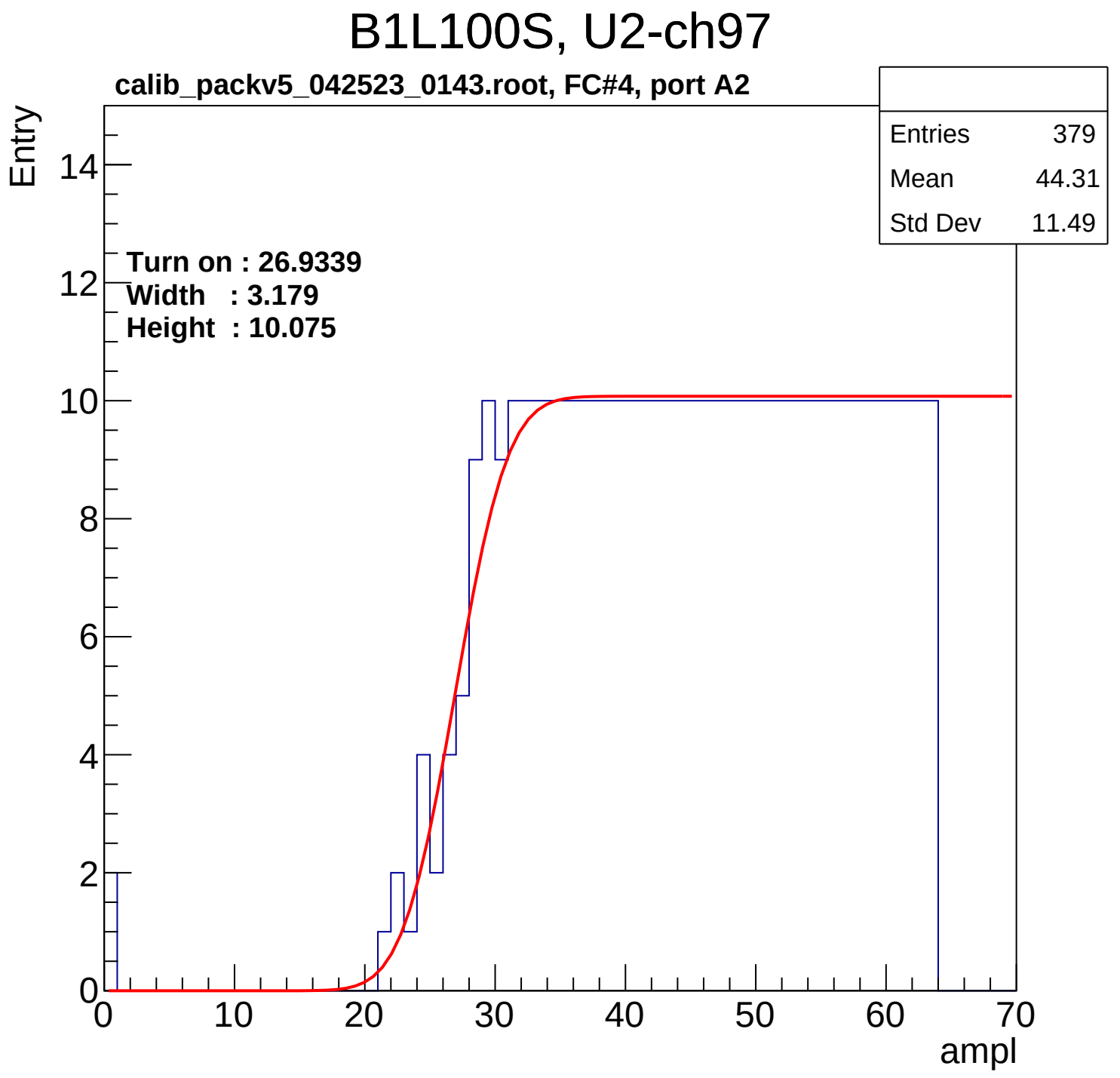
B1L100S, U2-ch97
calib_packv5_042523_0143.root, FC#4, port A2
Entries 379
Mean 44.31
Std Dev 11.49
Turn on : 26.9339
Width : 3.179
Height : 10.075
Entry
ampl
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6
8
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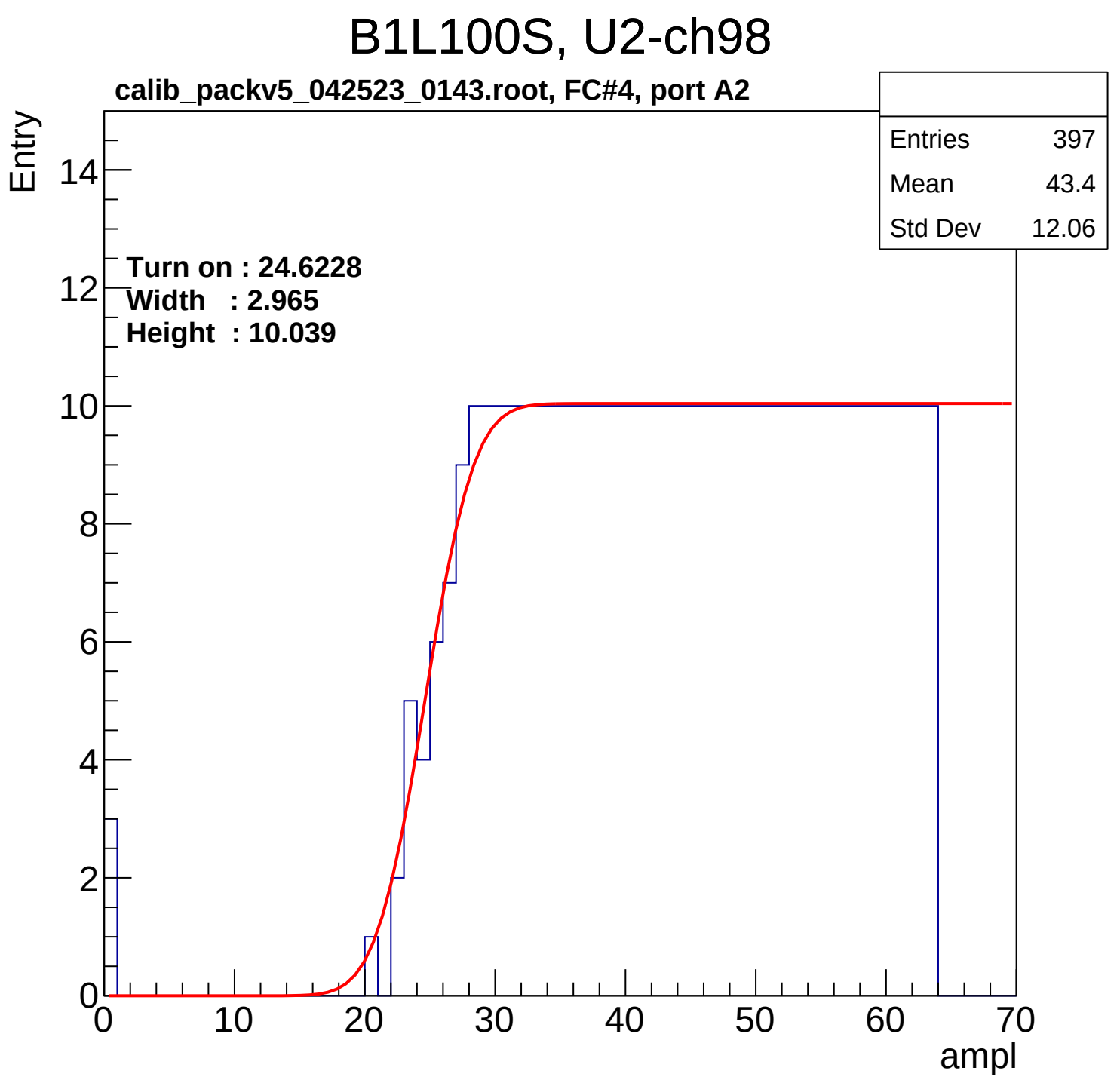
B1L100S, U2-ch98
calib_packv5_042523_0143.root, FC#4, port A2
Entries 397
Mean 43.4
Std Dev 12.06
Turn on : 24.6228
Width : 2.965
Height : 10.039
Entry
ampl
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2
4
6
8
10
12
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0
10
20
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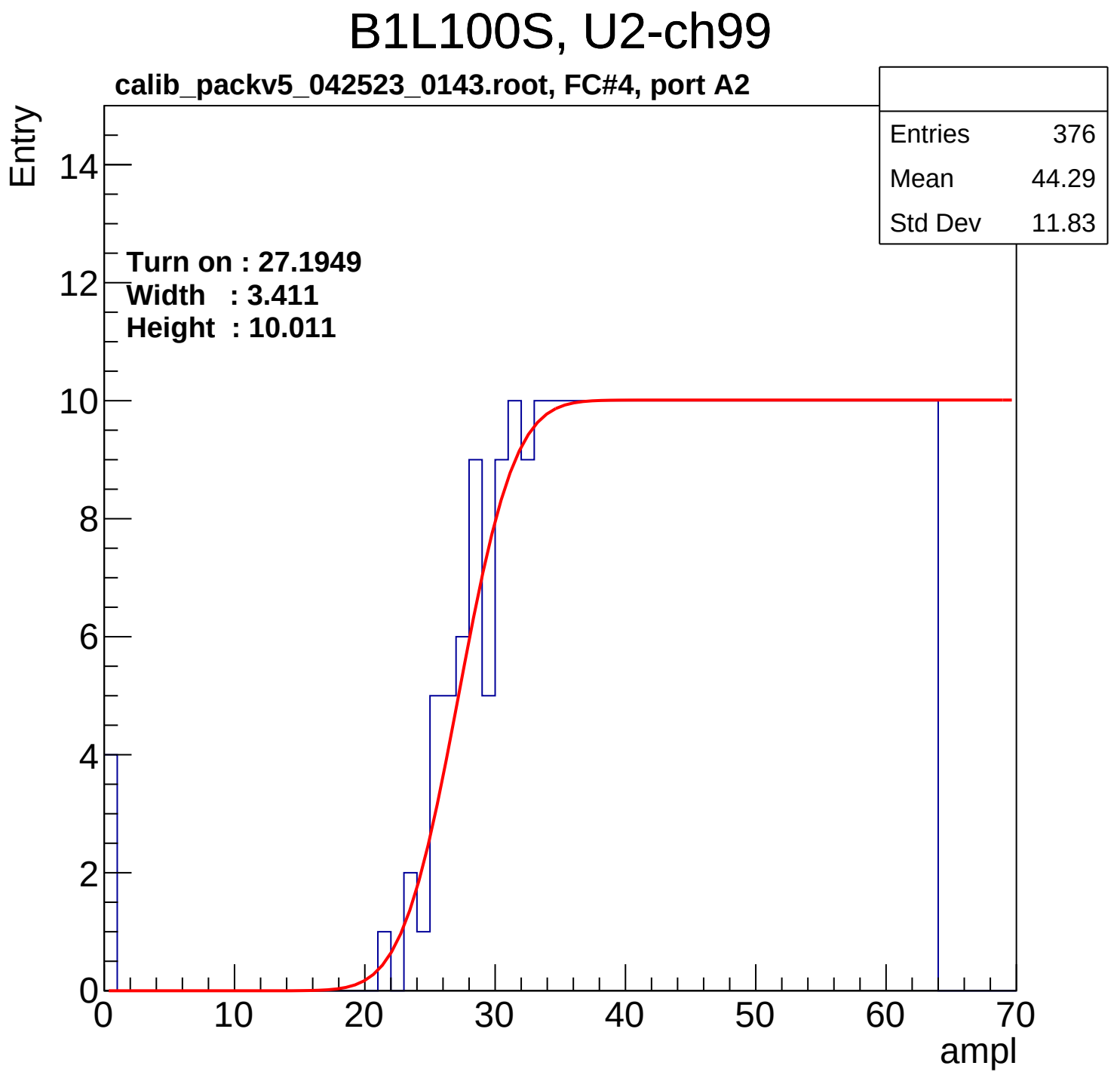
B1L100S, U2-ch99
calib_packv5_042523_0143.root, FC#4, port A2
Entries 376
Mean 44.29
Std Dev 11.83
Turn on : 27.1949
Width : 3.411
Height : 10.011
Entry
ampl
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6
8
10
12
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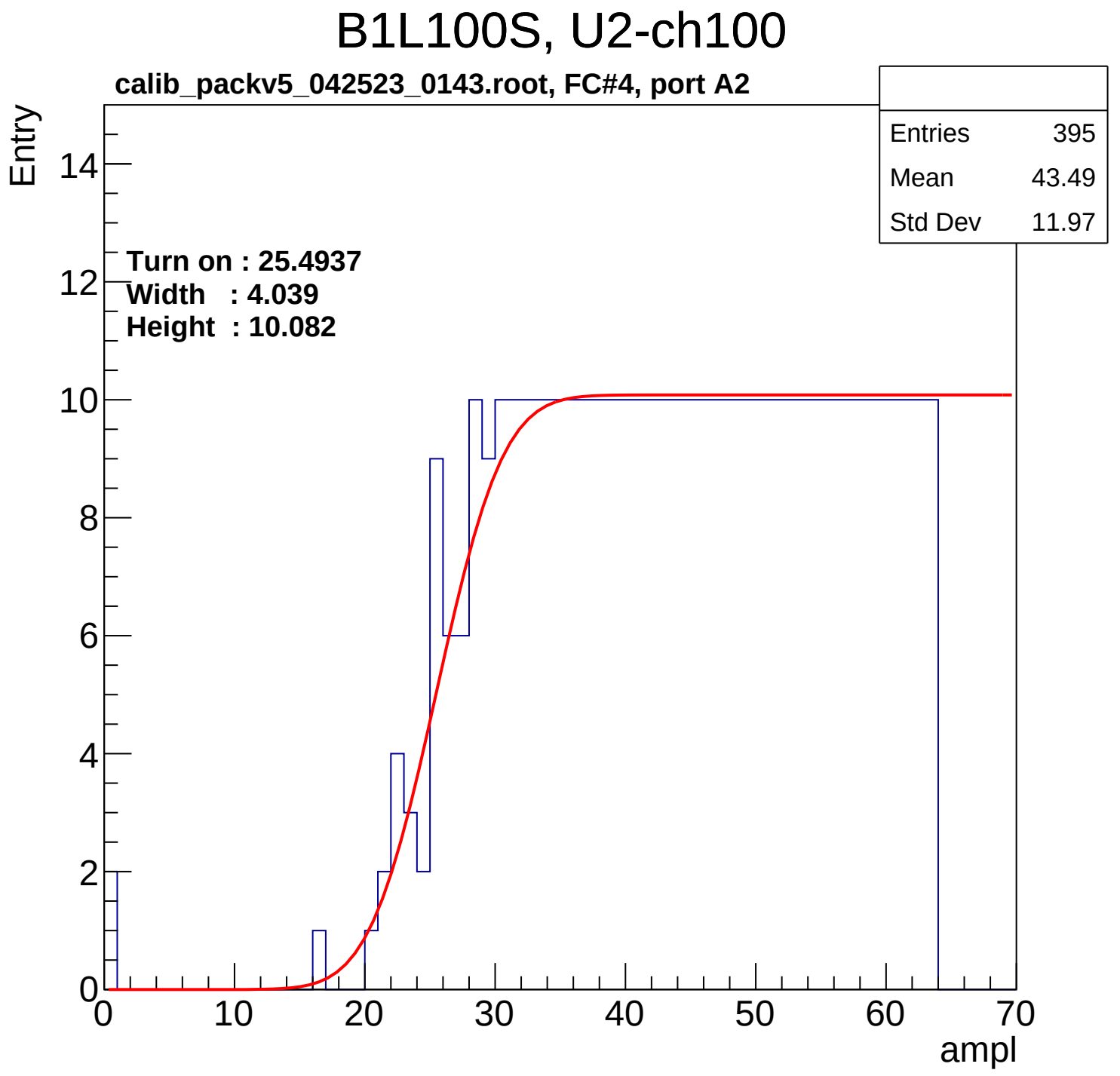
B1L100S, U2-ch100
calib_packv5_042523_0143.root, FC#4, port A2
Entries 395
Mean 43.49
Std Dev 11.97
Turn on : 25.4937
Width : 4.039
Height : 10.082
Entry
ampl
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6
8
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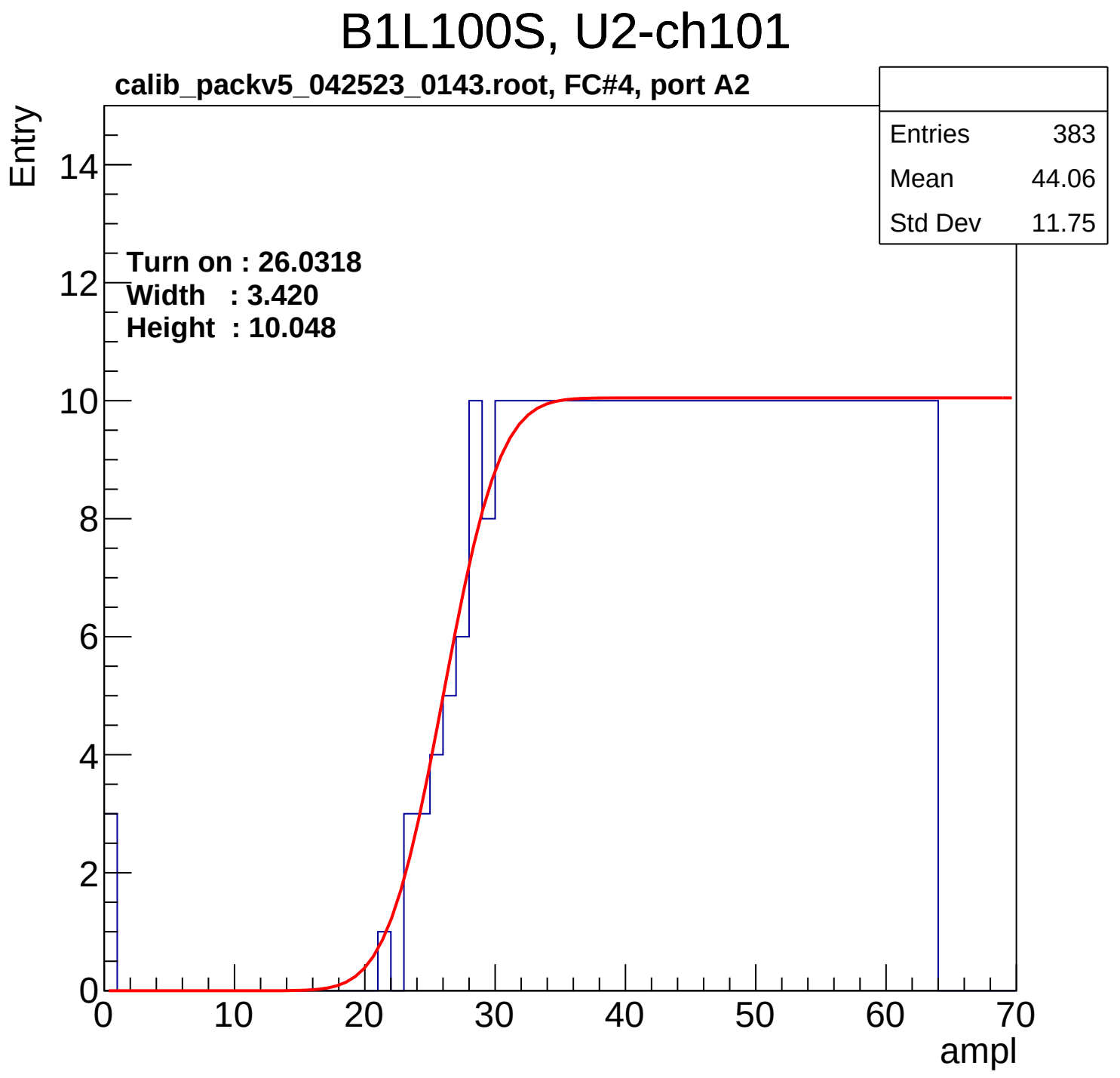
B1L100S, U2-ch101
calib_packv5_042523_0143.root, FC#4, port A2
Entries 383
Mean 44.06
Std Dev 11.75
Turn on : 26.0318
Width : 3.420
Height : 10.048
Entry
ampl
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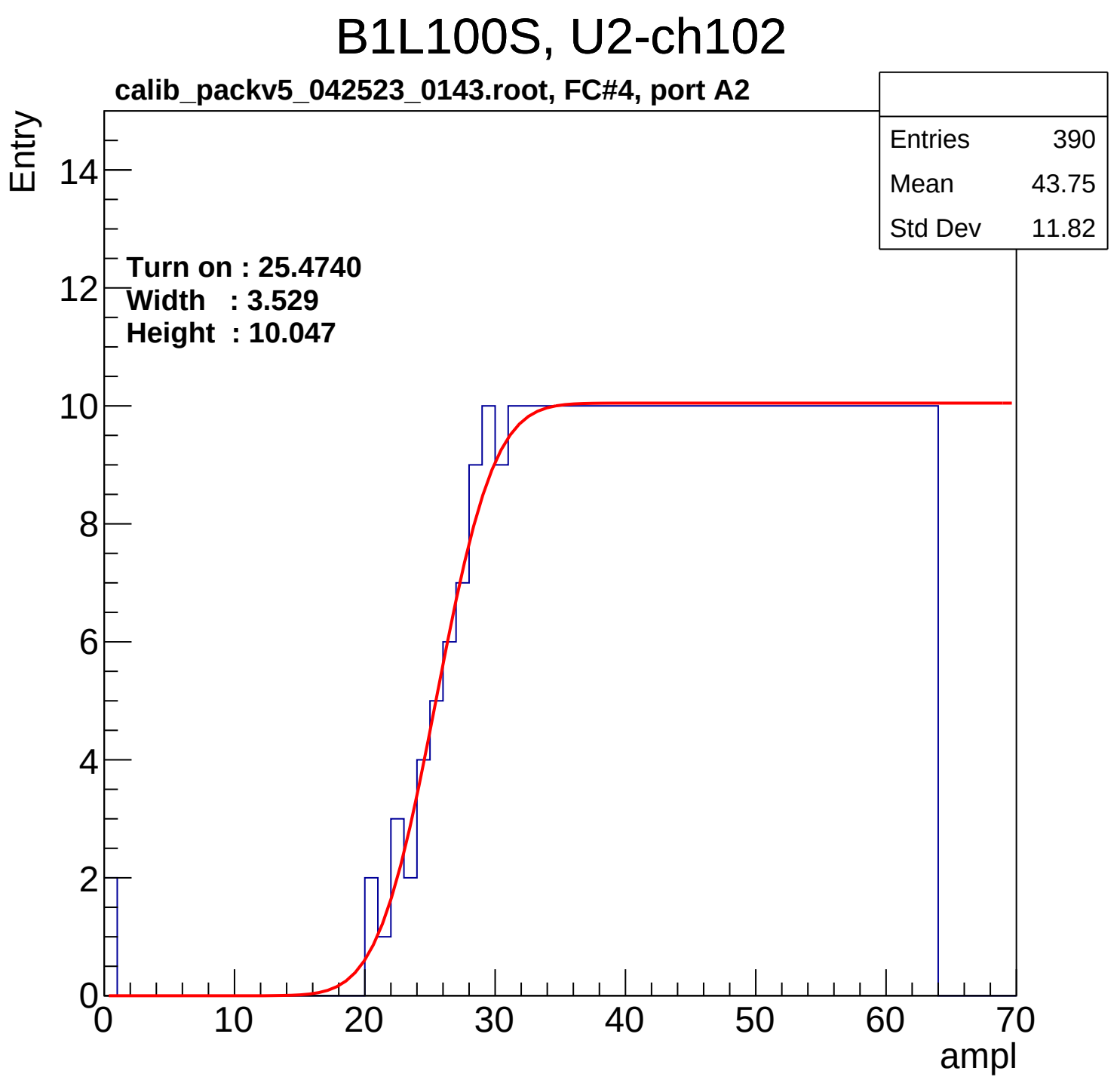
B1L100S, U2-ch102
calib_packv5_042523_0143.root, FC#4, port A2
Entries 390
Mean 43.75
Std Dev 11.82
Turn on : 25.4740
Width : 3.529
Height : 10.047
Entry
ampl
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6
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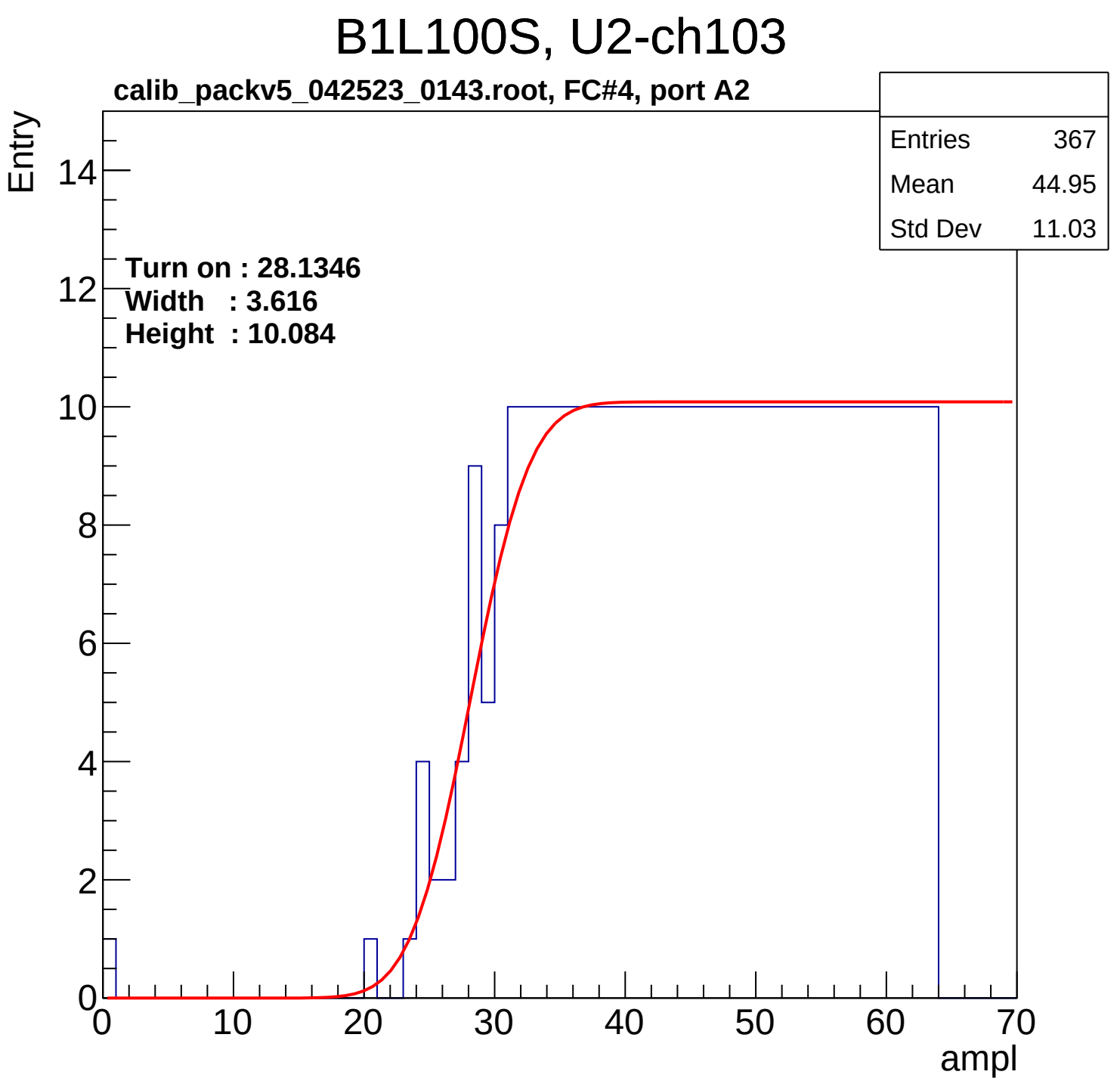
B1L100S, U2-ch103
calib_packv5_042523_0143.root, FC#4, port A2
Entries 367
Mean 44.95
Std Dev 11.03
Turn on : 28.1346
Width : 3.616
Height : 10.084
Entry
ampl
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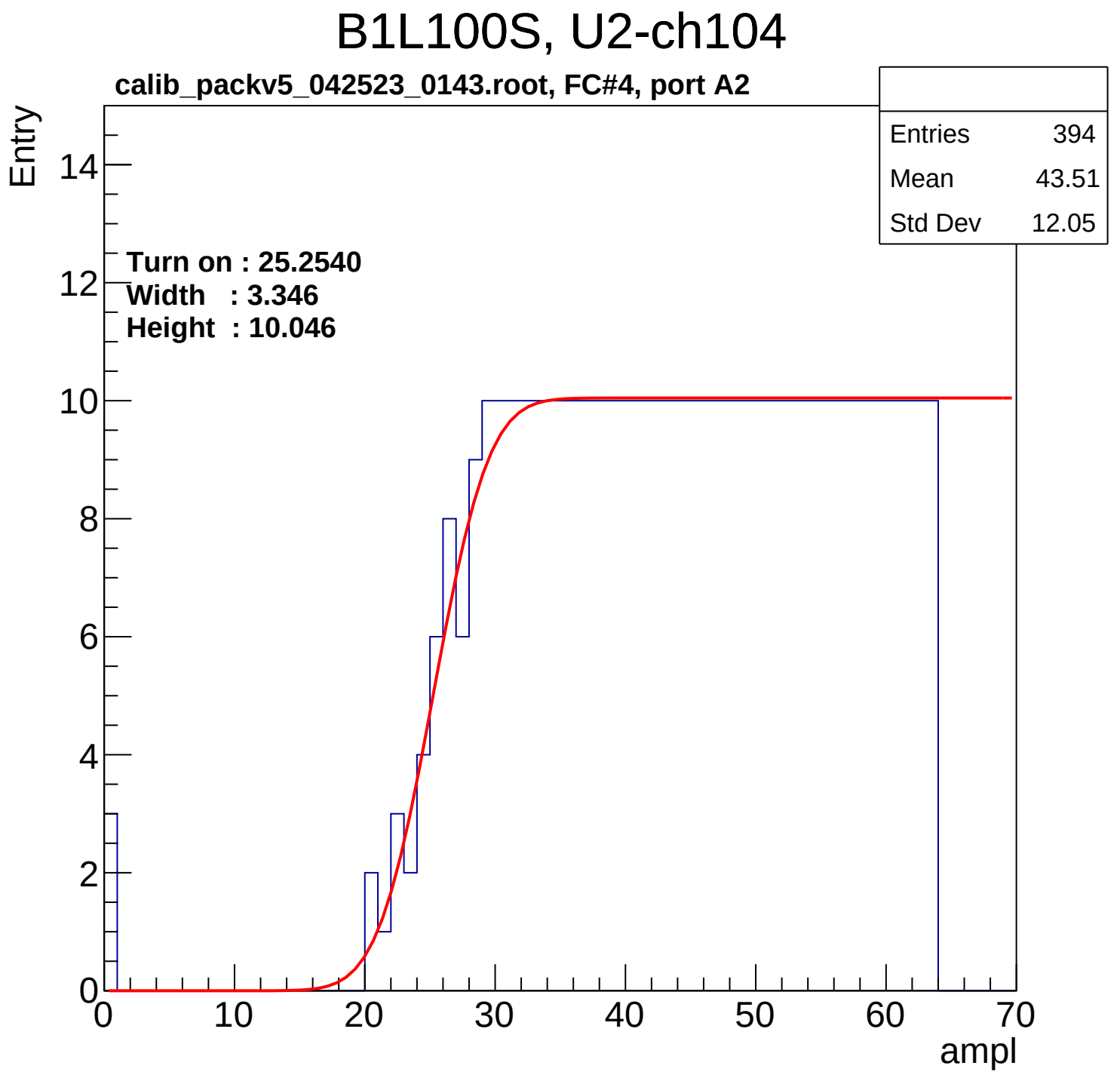
B1L100S, U2-ch104
calib_packv5_042523_0143.root, FC#4, port A2
Entries 394
Mean 43.51
Std Dev 12.05
Turn on : 25.2540
Width : 3.346
Height : 10.046
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ampl
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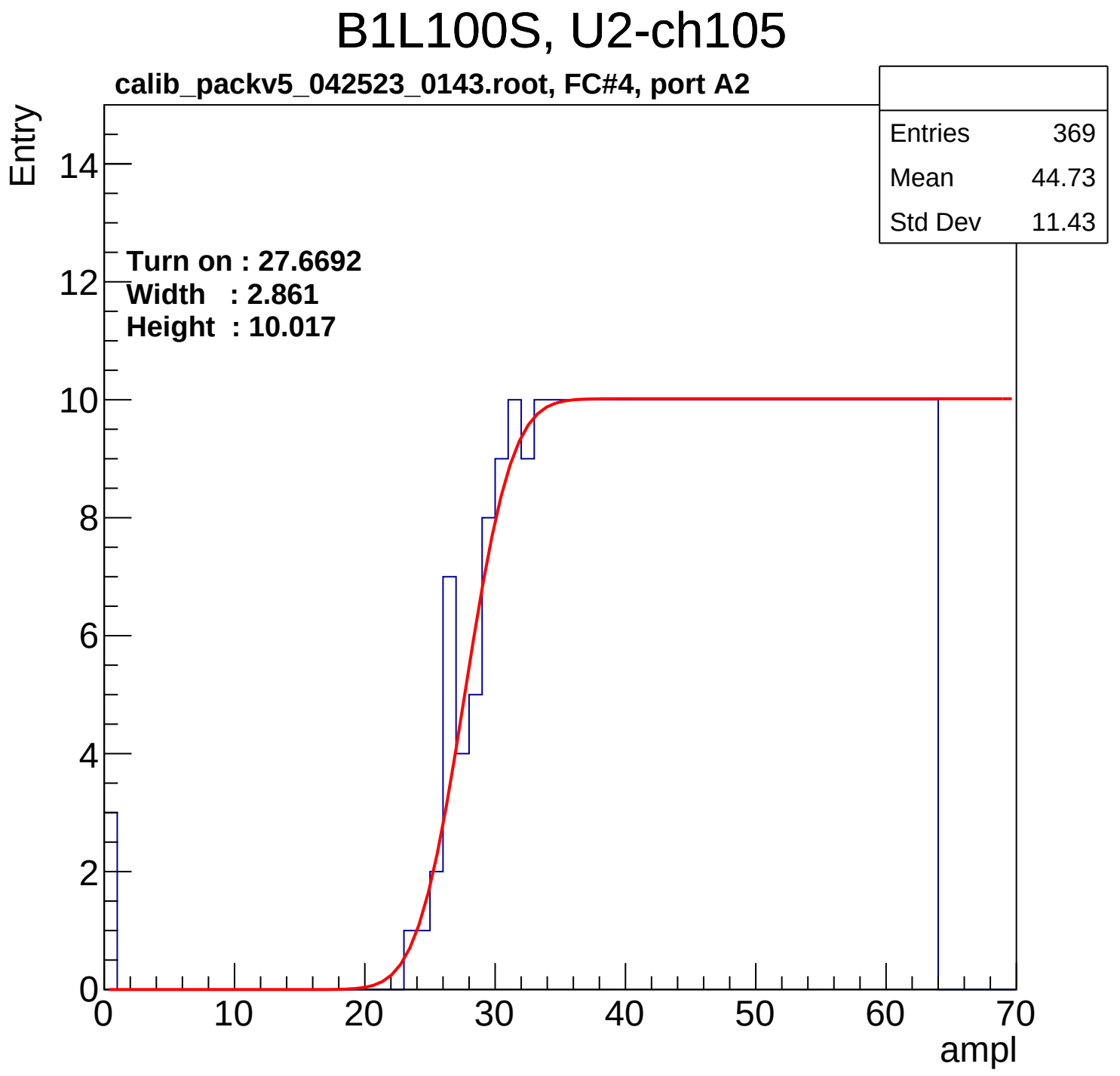
B1L100S, U2-ch105
calib_packv5_042523_0143.root, FC#4, port A2
Entries 369
Mean 44.73
Std Dev 11.43
Turn on : 27.6692
Width : 2.861
Height : 10.017
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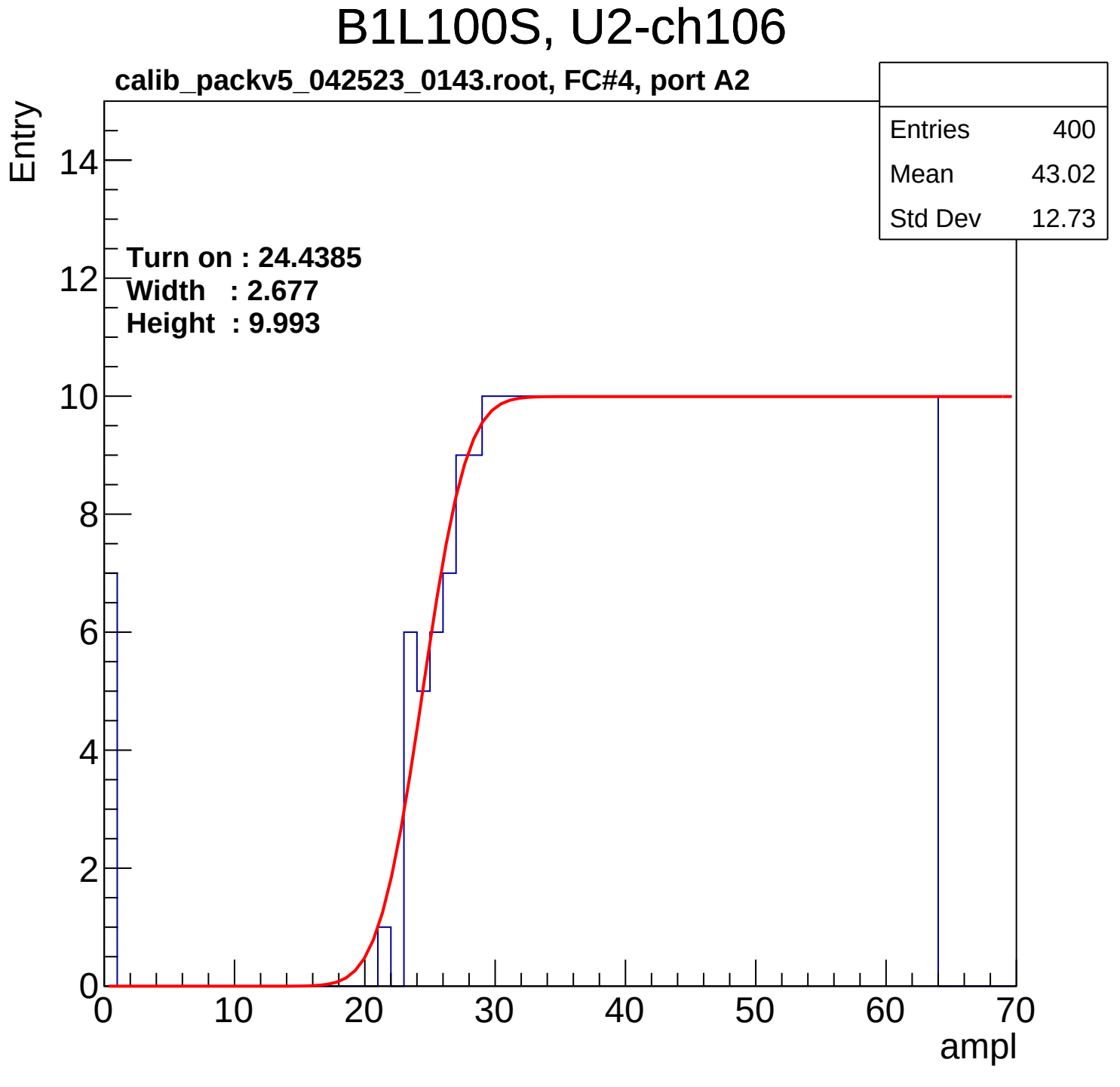
B1L100S, U2-ch106
calib_packv5_042523_0143.root, FC#4, port A2
Entries 400
Mean 43.02
Std Dev 12.73
Turn on : 24.4385
Width : 2.677
Height : 9.993
Entry
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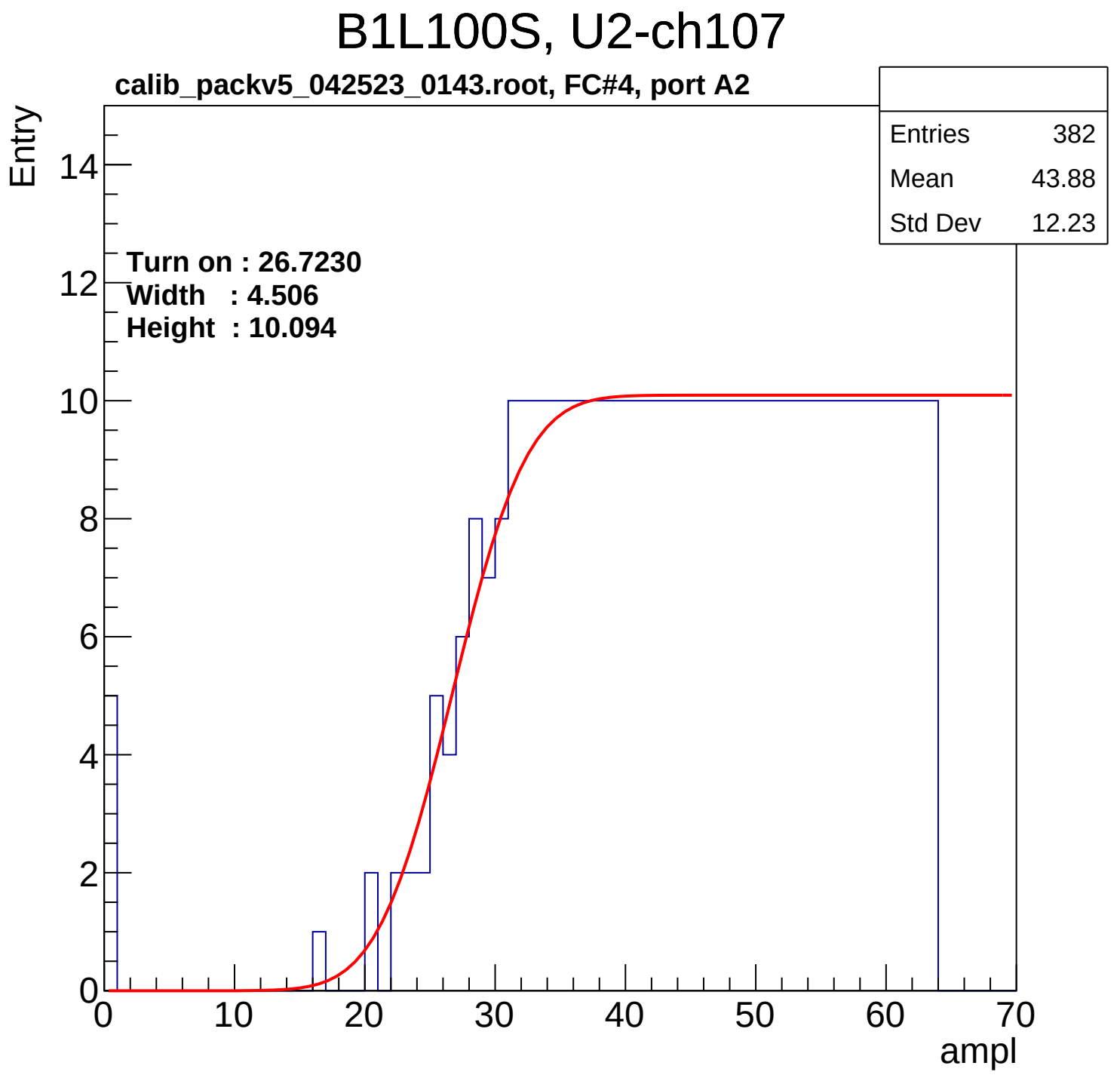
B1L100S, U2-ch107
calib_packv5_042523_0143.root, FC#4, port A2
Entries 382
Mean 43.88
Std Dev 12.23
Turn on : 26.7230
Width : 4.506
Height : 10.094
Entry
ampl
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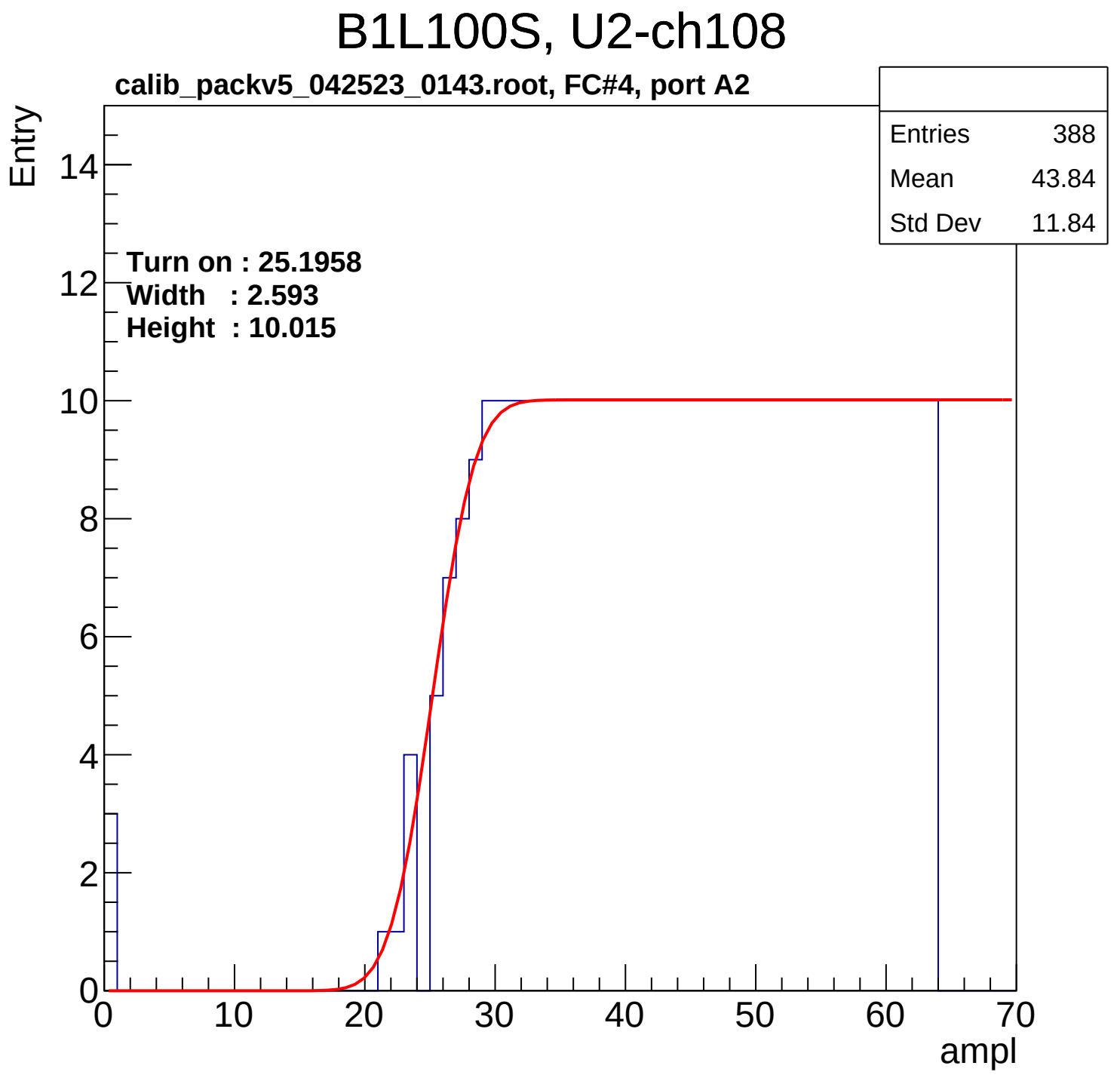
B1L100S, U2-ch108
calib_packv5_042523_0143.root, FC#4, port A2
Entries 388
Mean 43.84
Std Dev 11.84
Turn on : 25.1958
Width : 2.593
Height : 10.015
Entry
ampl
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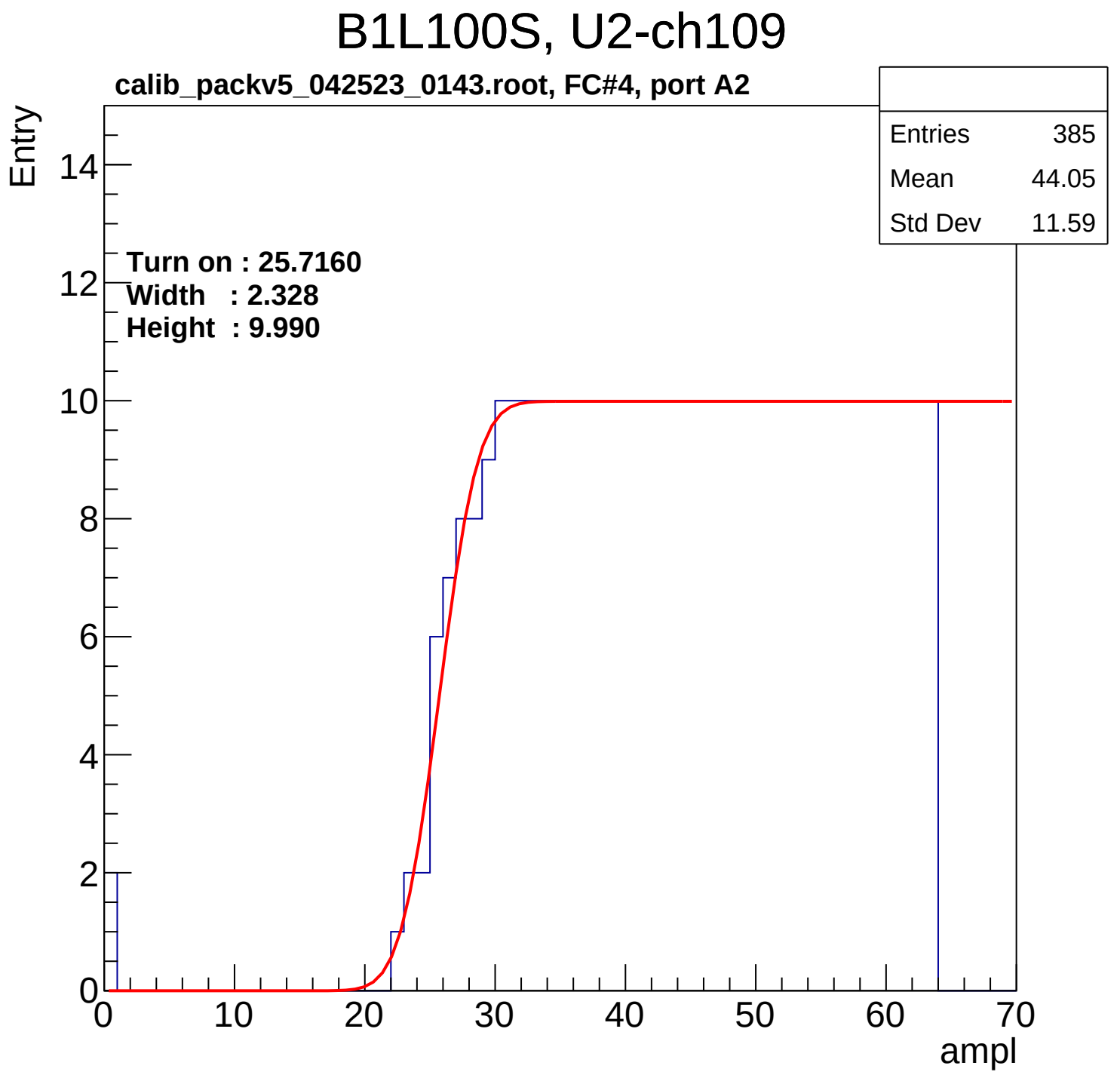
B1L100S, U2-ch109
calib_packv5_042523_0143.root, FC#4, port A2
Entries 385
Mean 44.05
Std Dev 11.59
Turn on : 25.7160
Width : 2.328
Height : 9.990
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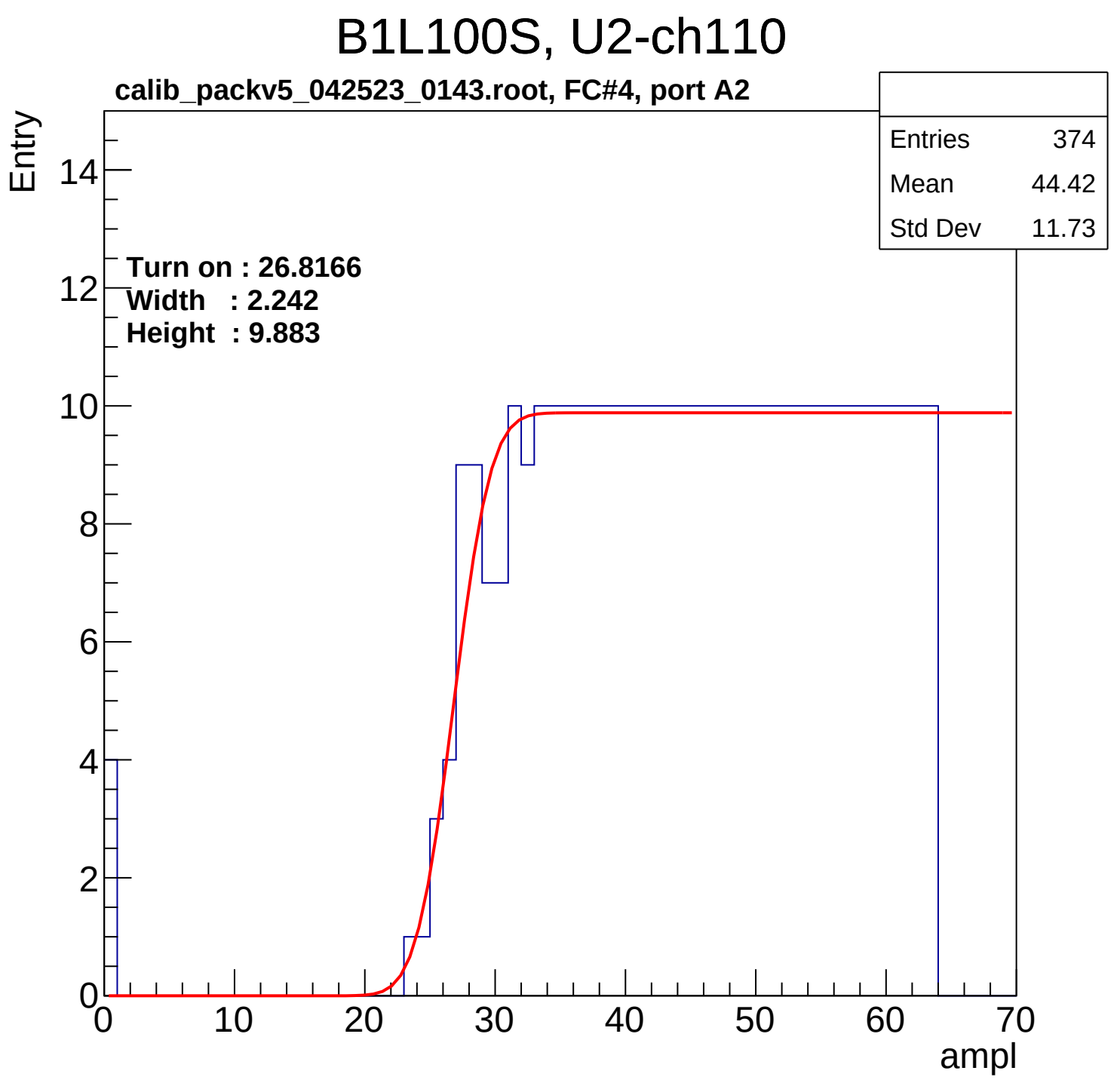
B1L100S, U2-ch110
calib_packv5_042523_0143.root, FC#4, port A2
Entries 374
Mean 44.42
Std Dev 11.73
Turn on : 26.8166
Width : 2.242
Height : 9.883
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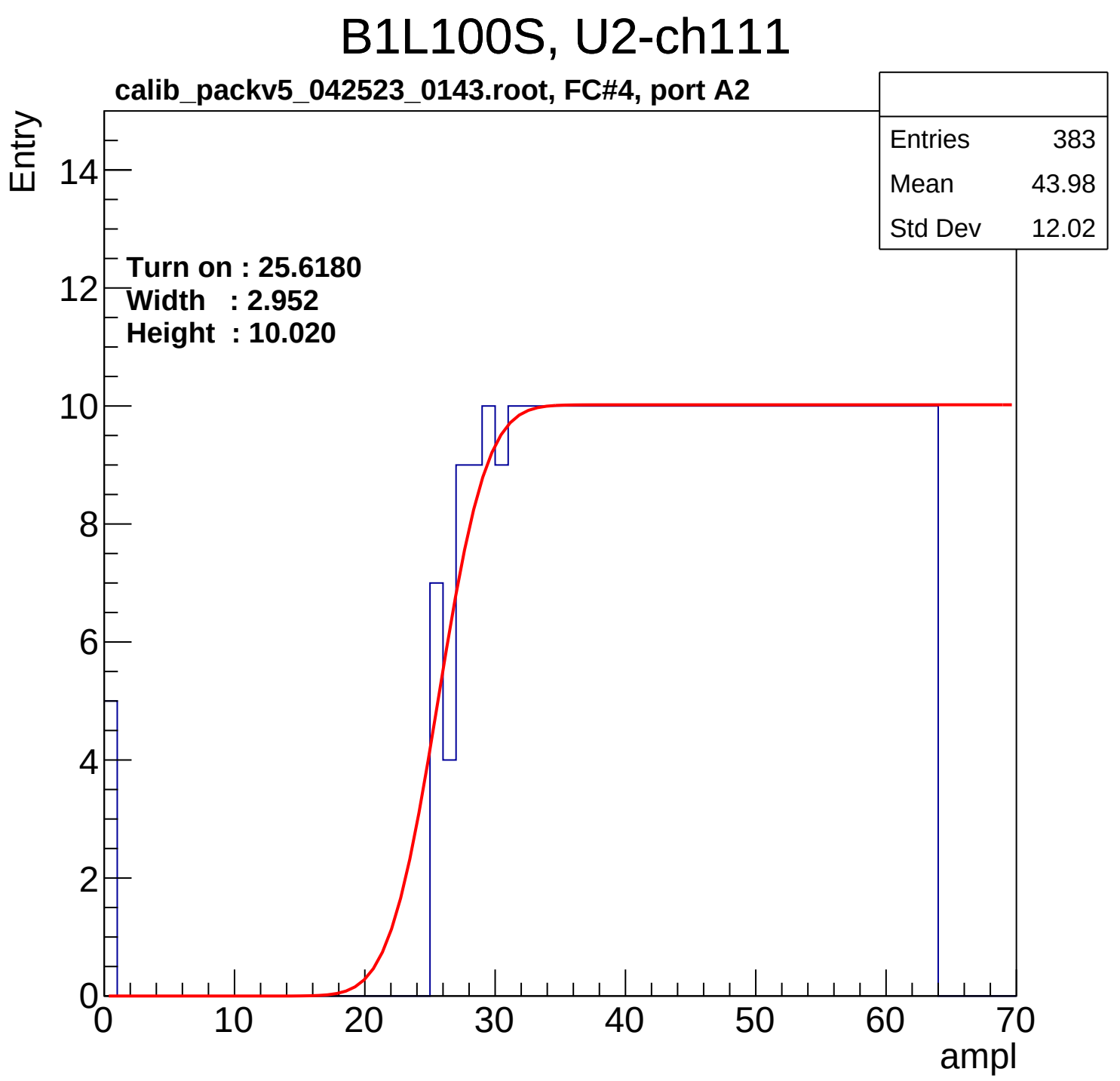
B1L100S, U2-ch111
calib_packv5_042523_0143.root, FC#4, port A2
Entries 383
Mean 43.98
Std Dev 12.02
Turn on : 25.6180
Width : 2.952
Height : 10.020
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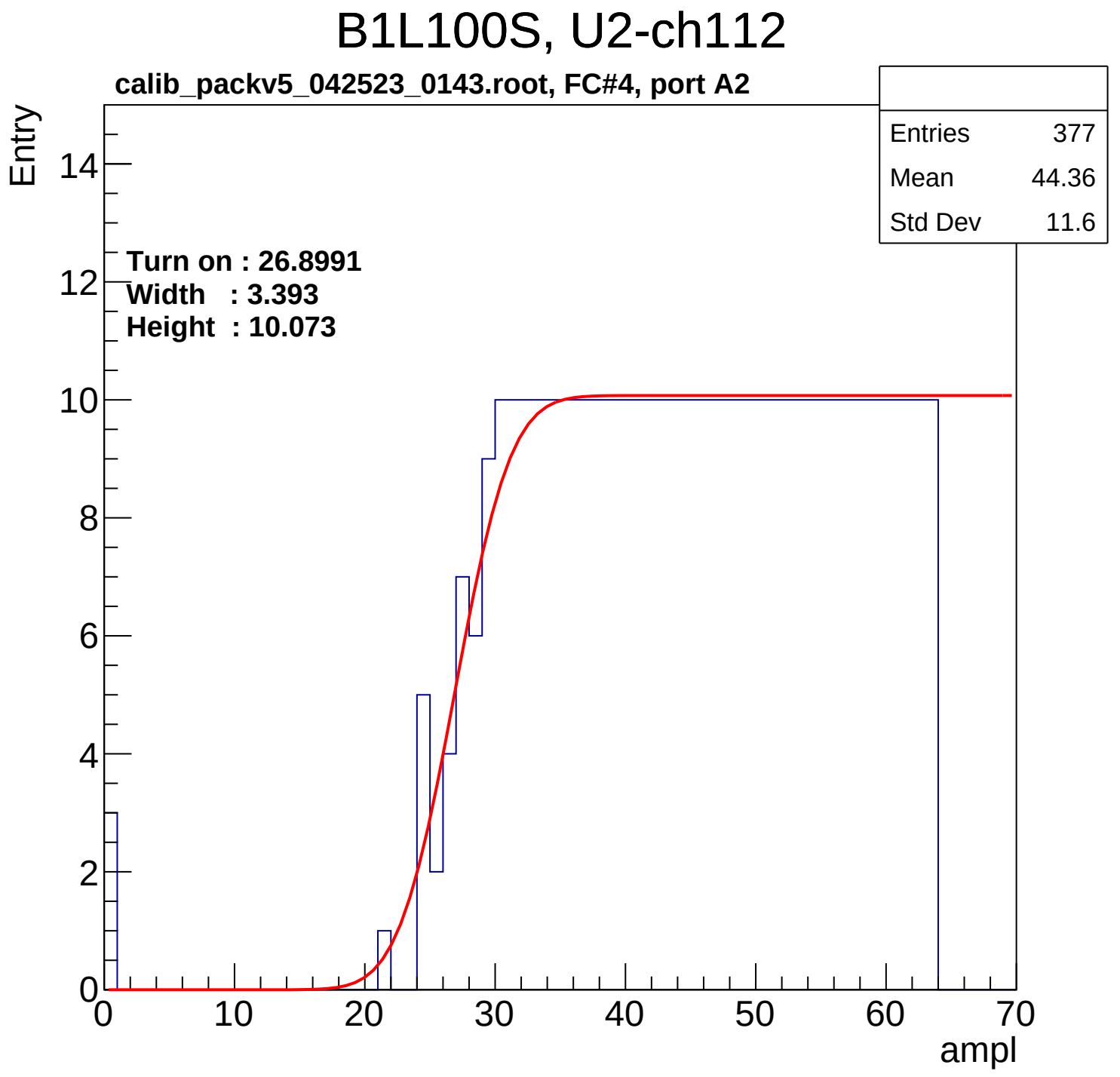
B1L100S, U2-ch112
calib_packv5_042523_0143.root, FC#4, port A2
Entries 377
Mean 44.36
Std Dev 11.6
Turn on : 26.8991
Width : 3.393
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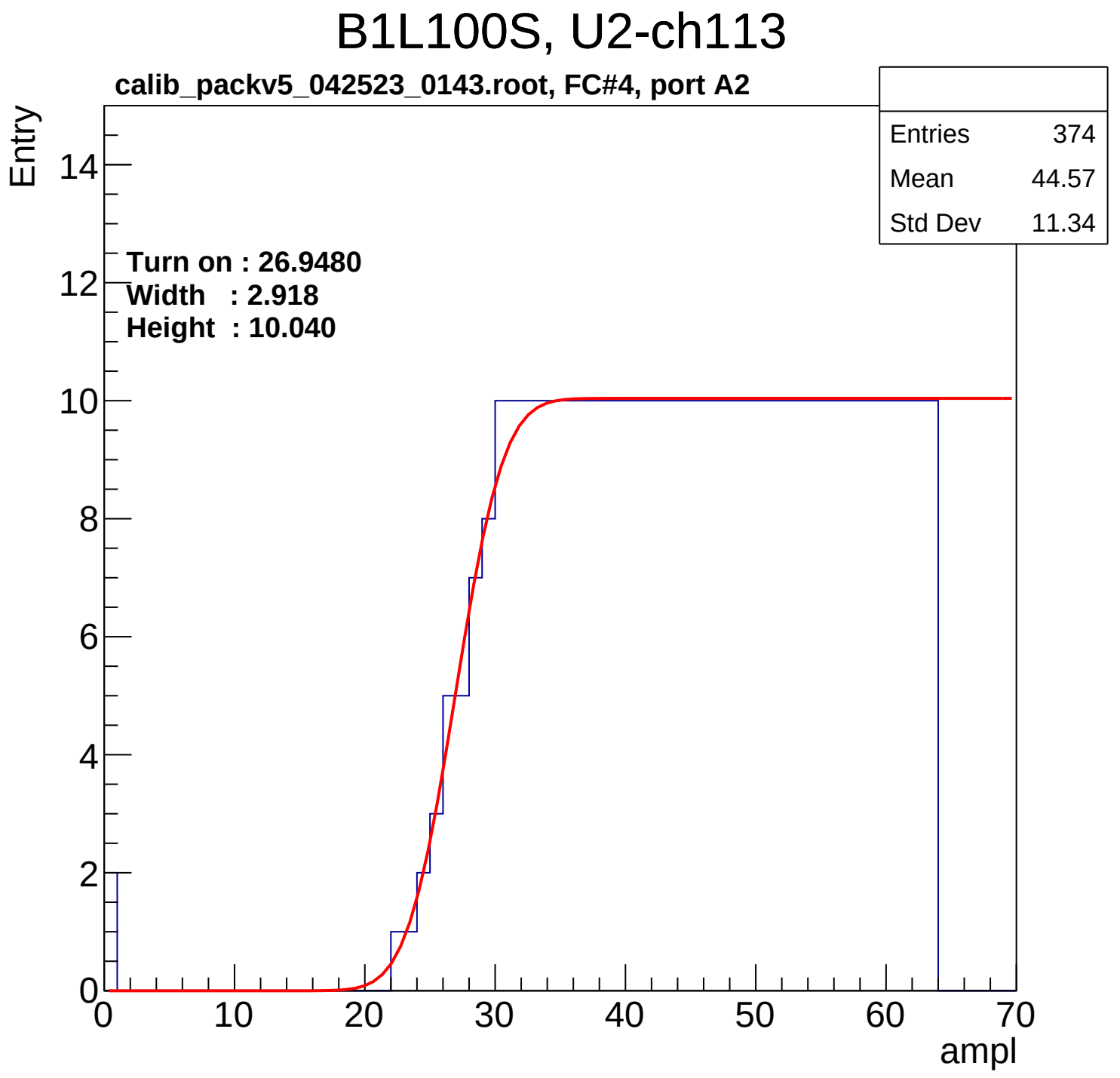
B1L100S, U2-ch113
calib_packv5_042523_0143.root, FC#4, port A2
Entries 374
Mean 44.57
Std Dev 11.34
Turn on : 26.9480
Width : 2.918
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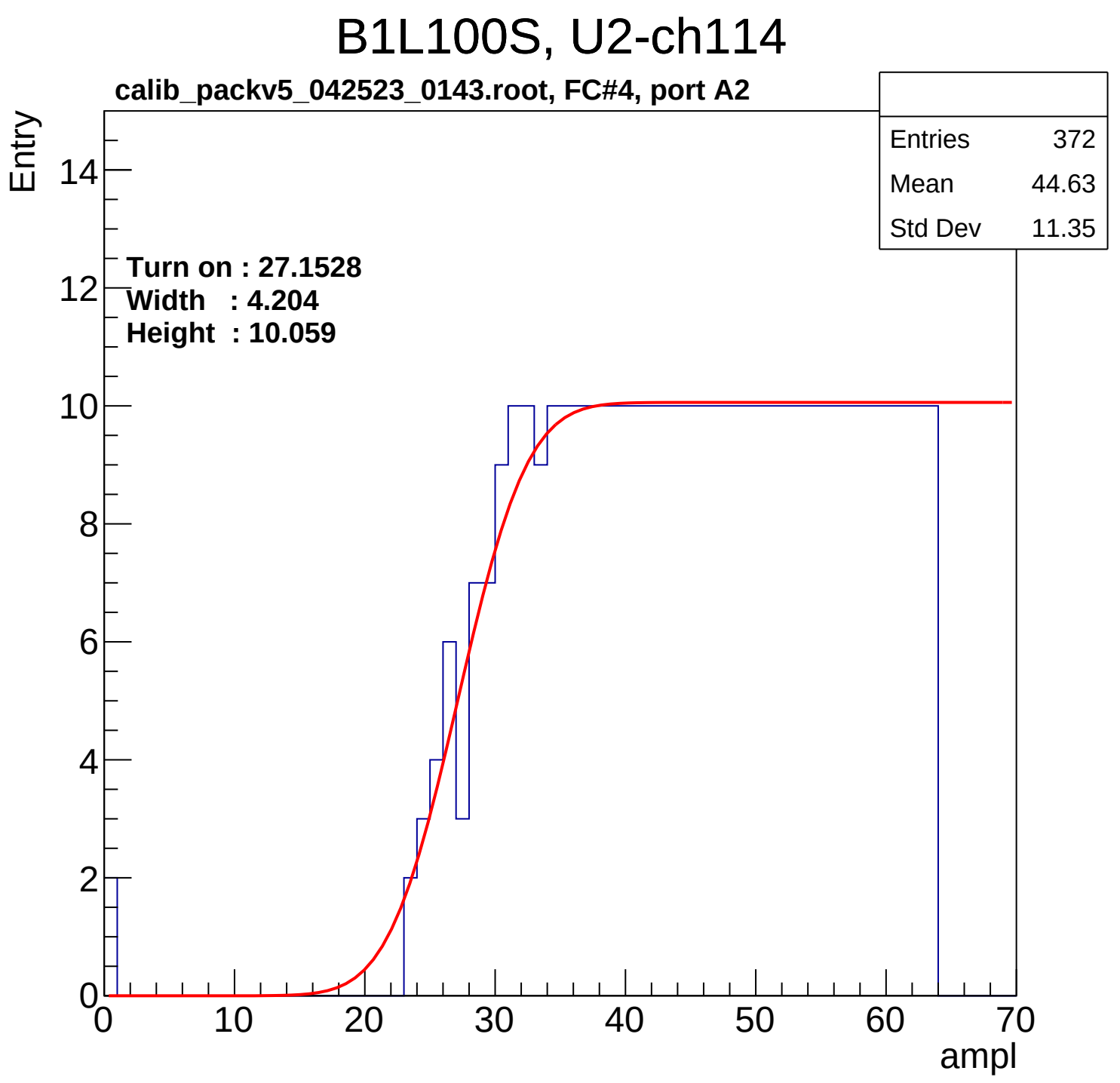
B1L100S, U2-ch114
calib_packv5_042523_0143.root, FC#4, port A2
Entries 372
Mean 44.63
Std Dev 11.35
Turn on : 27.1528
Width : 4.204
Height : 10.059
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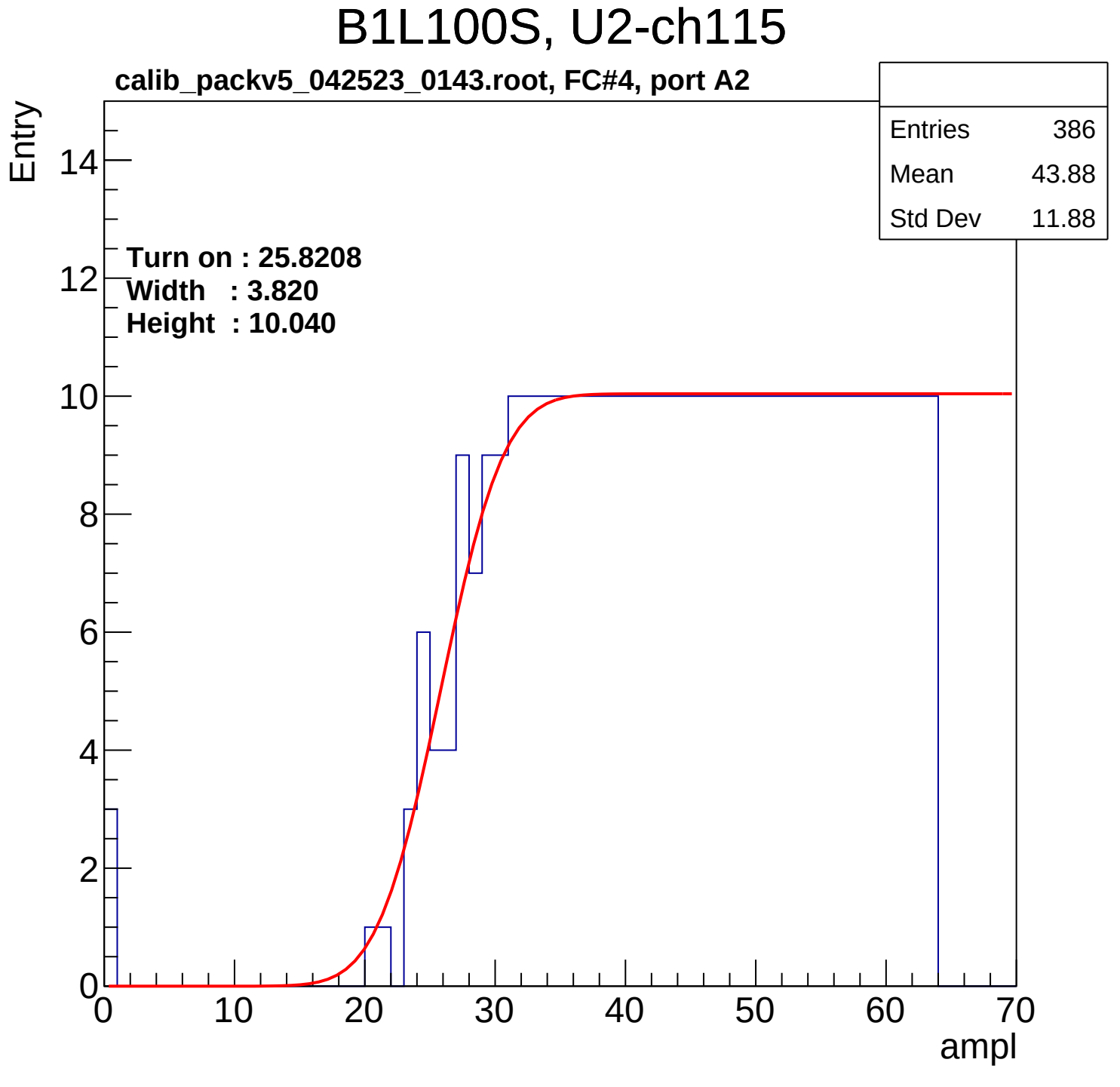
B1L100S, U2-ch115
calib_packv5_042523_0143.root, FC#4, port A2
Entries 386
Mean 43.88
Std Dev 11.88
Turn on : 25.8208
Width : 3.820
Height : 10.040
Entry
ampl
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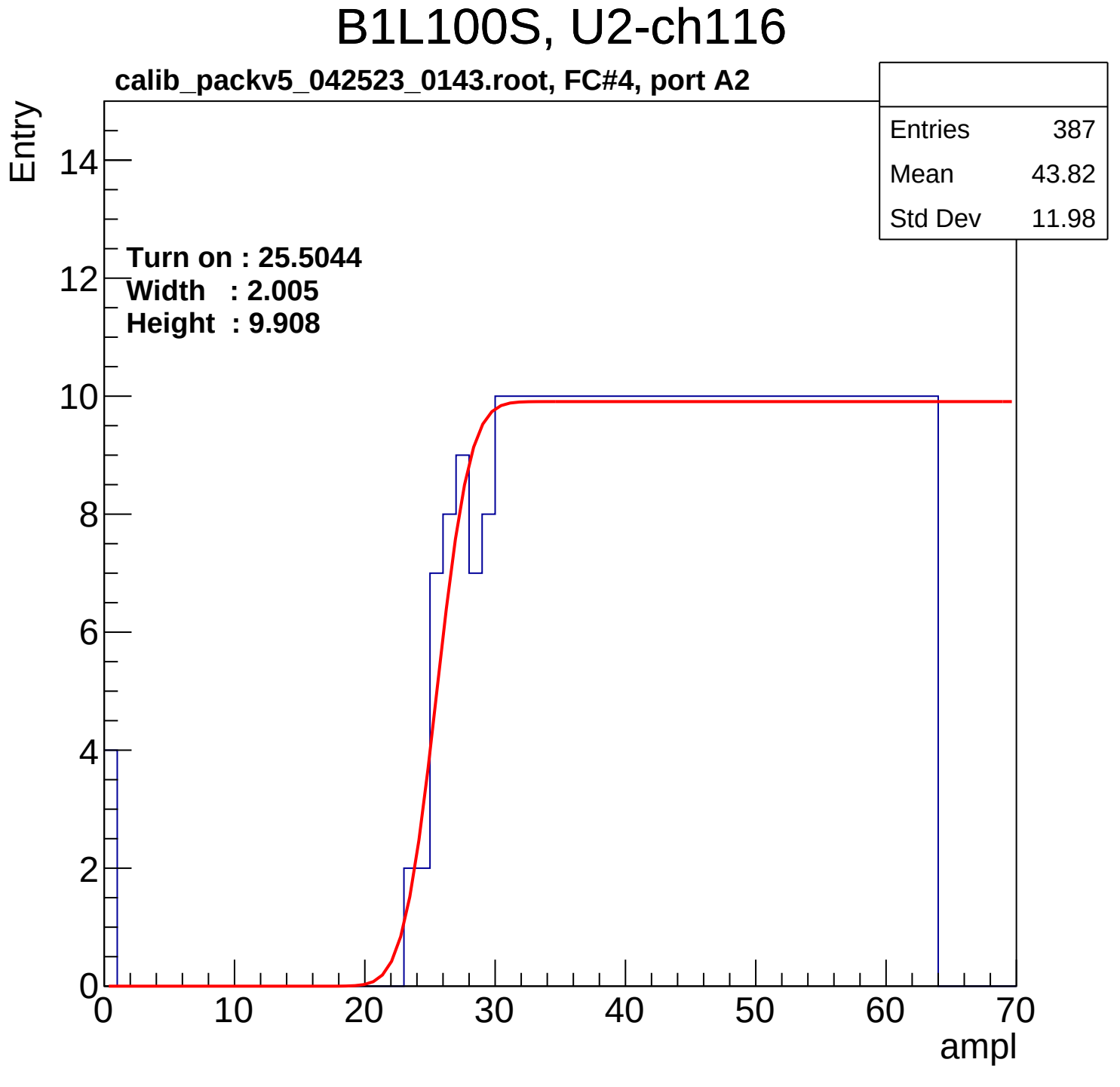
B1L100S, U2-ch116
calib_packv5_042523_0143.root, FC#4, port A2
Entries 387
Mean 43.82
Std Dev 11.98
Turn on : 25.5044
Width : 2.005
Height : 9.908
Entry
ampl
0
2
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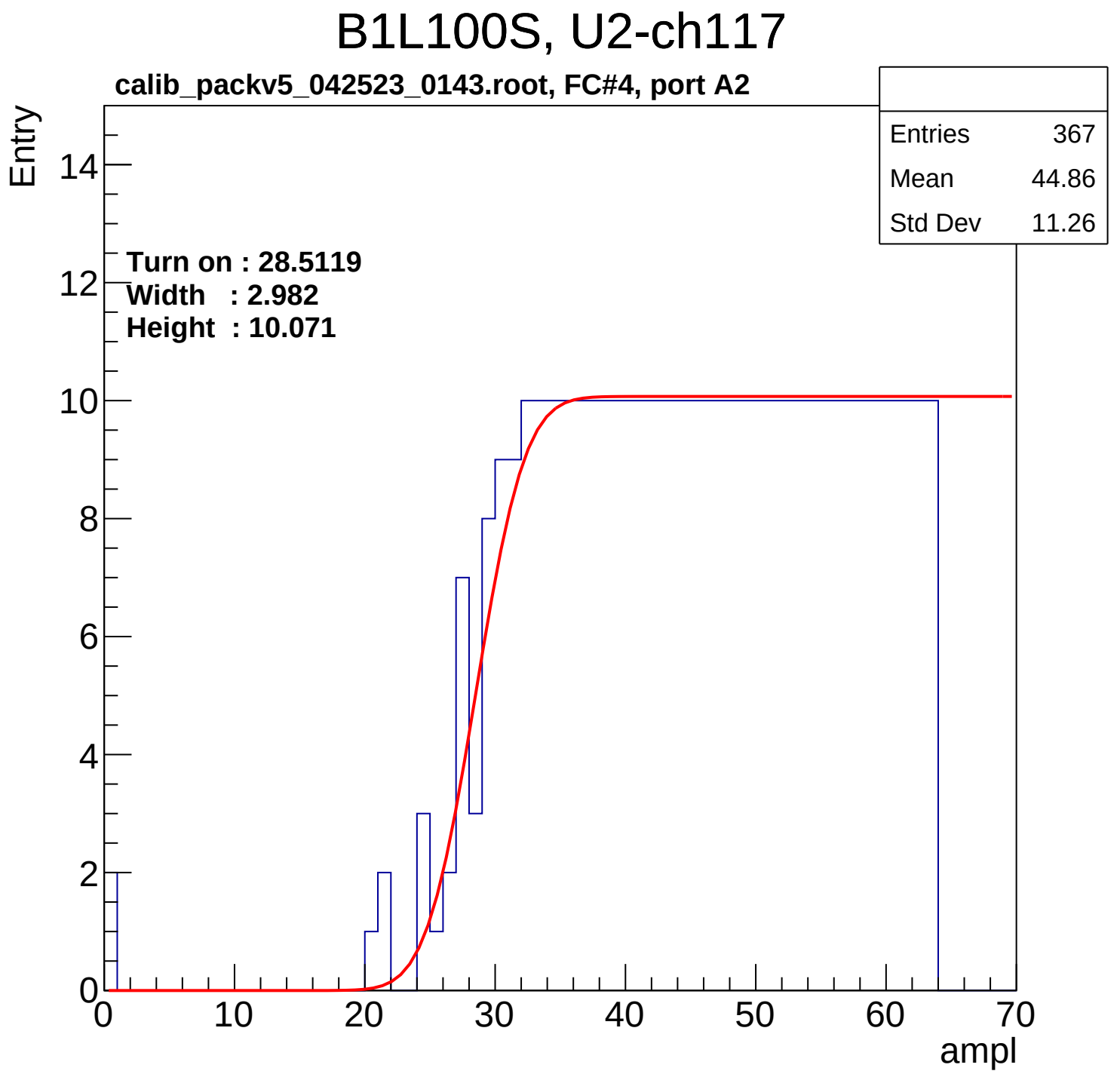
B1L100S, U2-ch117
calib_packv5_042523_0143.root, FC#4, port A2
Entries 367
Mean 44.86
Std Dev 11.26
Turn on : 28.5119
Width : 2.982
Height : 10.071
Entry
ampl
0
2
4
6
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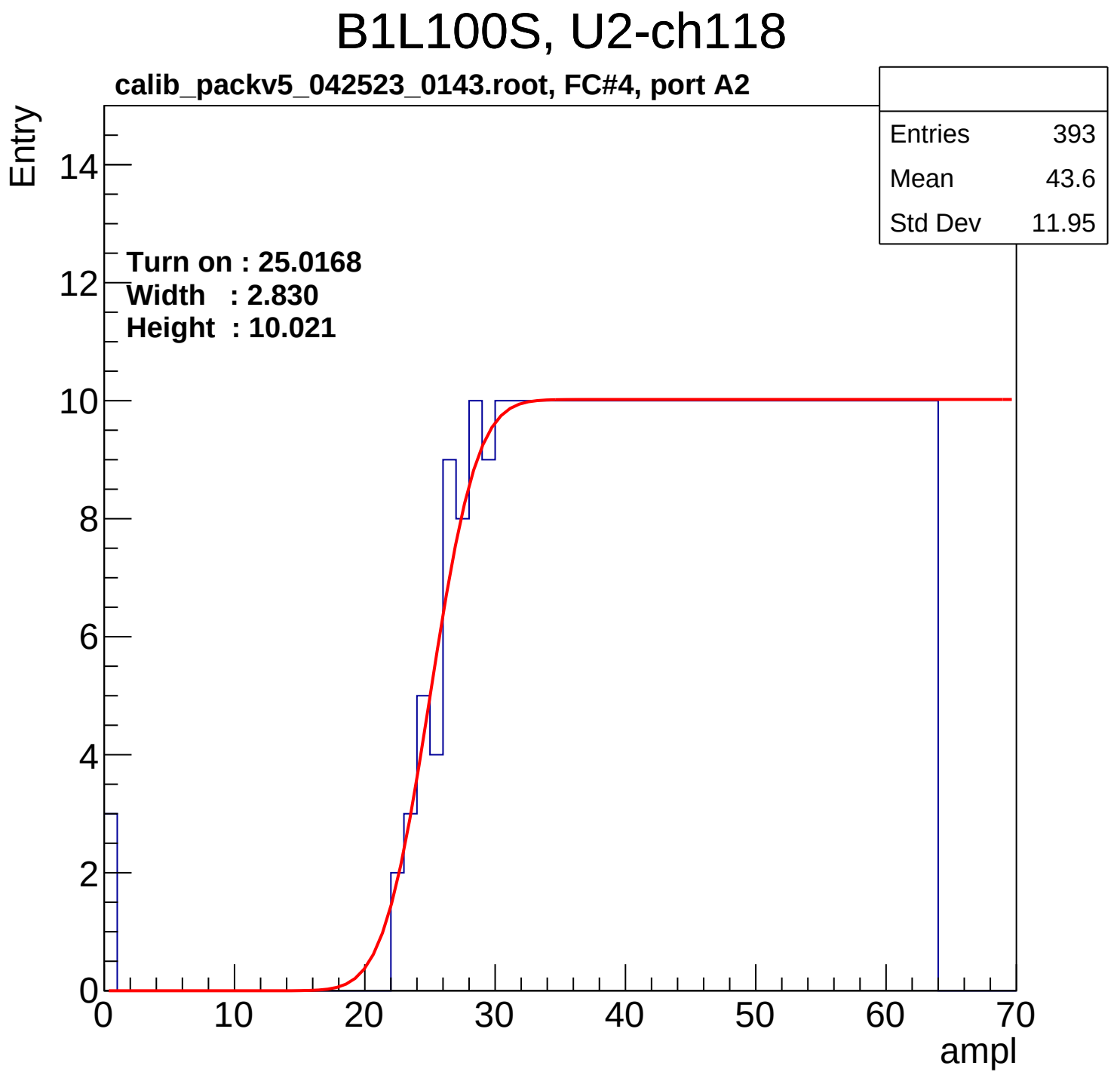
B1L100S, U2-ch118
calib_packv5_042523_0143.root, FC#4, port A2
Entries 393
Mean 43.6
Std Dev 11.95
Turn on : 25.0168
Width : 2.830
Height : 10.021
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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40
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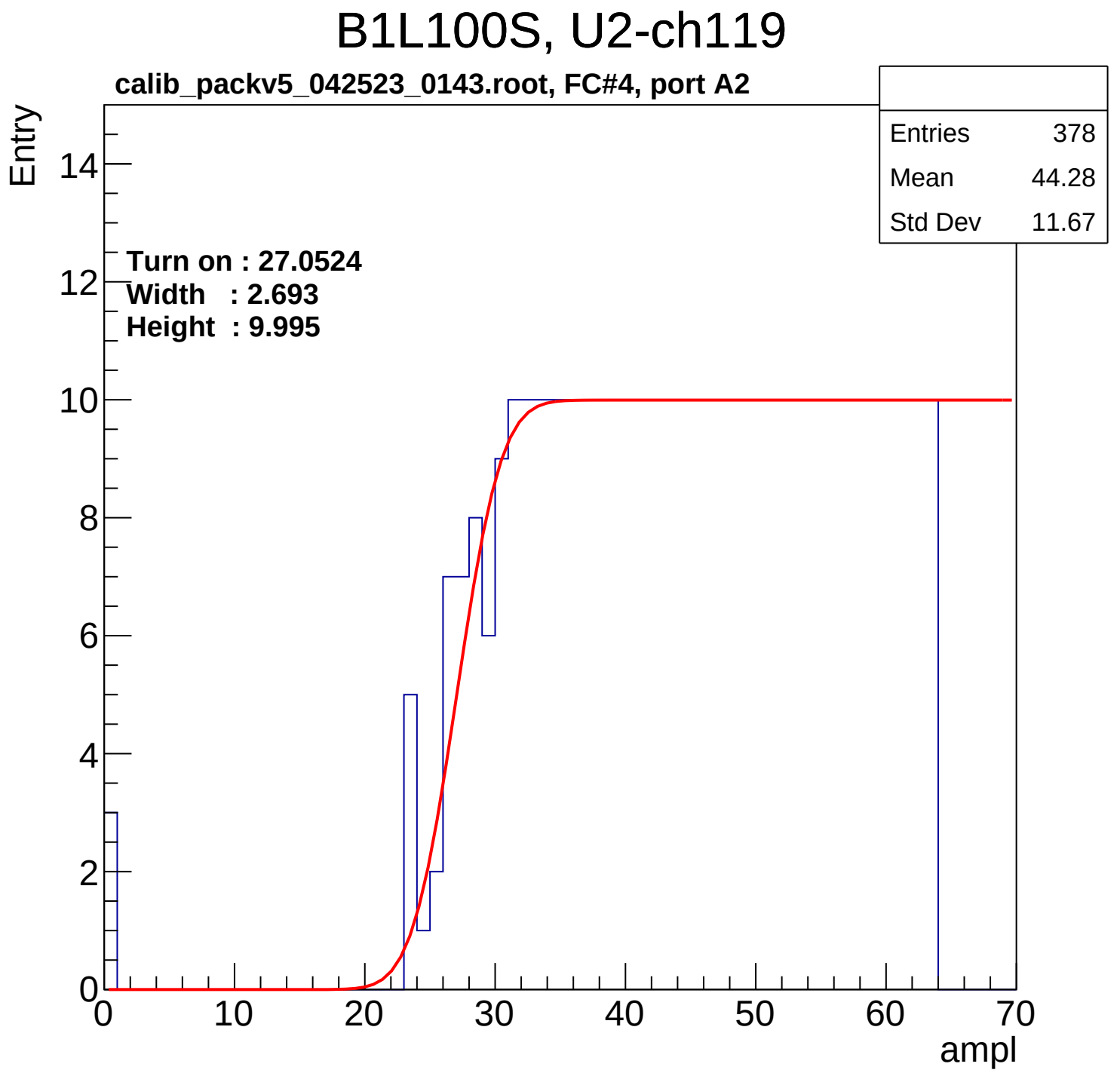
B1L100S, U2-ch119
calib_packv5_042523_0143.root, FC#4, port A2
Entries 378
Mean 44.28
Std Dev 11.67
Turn on : 27.0524
Width : 2.693
Height : 9.995
Entry
ampl
0
2
4
6
8
10
12
14
0
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20
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40
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60
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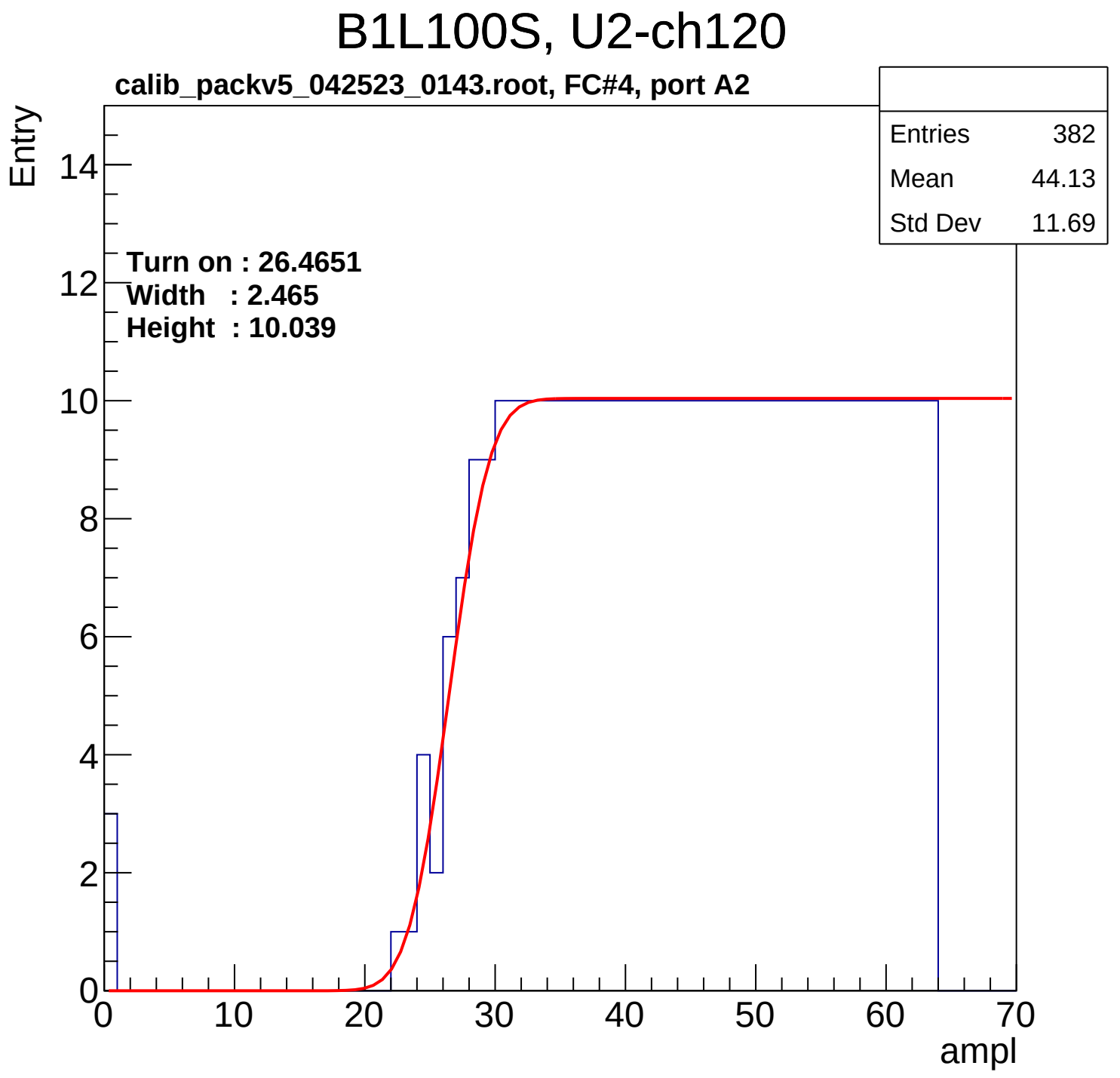
B1L100S, U2-ch120
calib_packv5_042523_0143.root, FC#4, port A2
Entries 382
Mean 44.13
Std Dev 11.69
Turn on : 26.4651
Width : 2.465
Height : 10.039
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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40
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60
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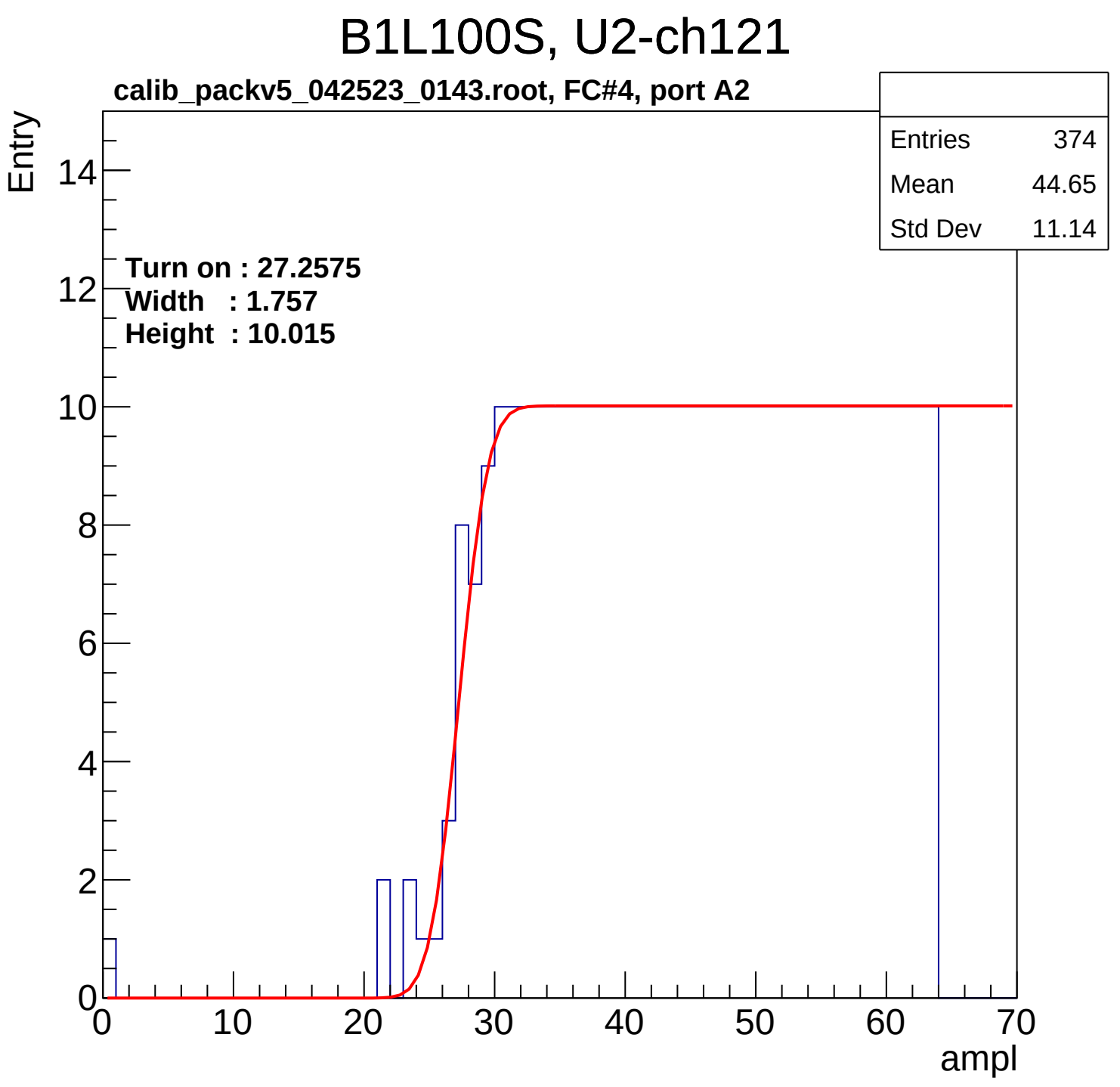
B1L100S, U2-ch121
calib_packv5_042523_0143.root, FC#4, port A2
Entries 374
Mean 44.65
Std Dev 11.14
Turn on : 27.2575
Width : 1.757
Height : 10.015
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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40
50
60
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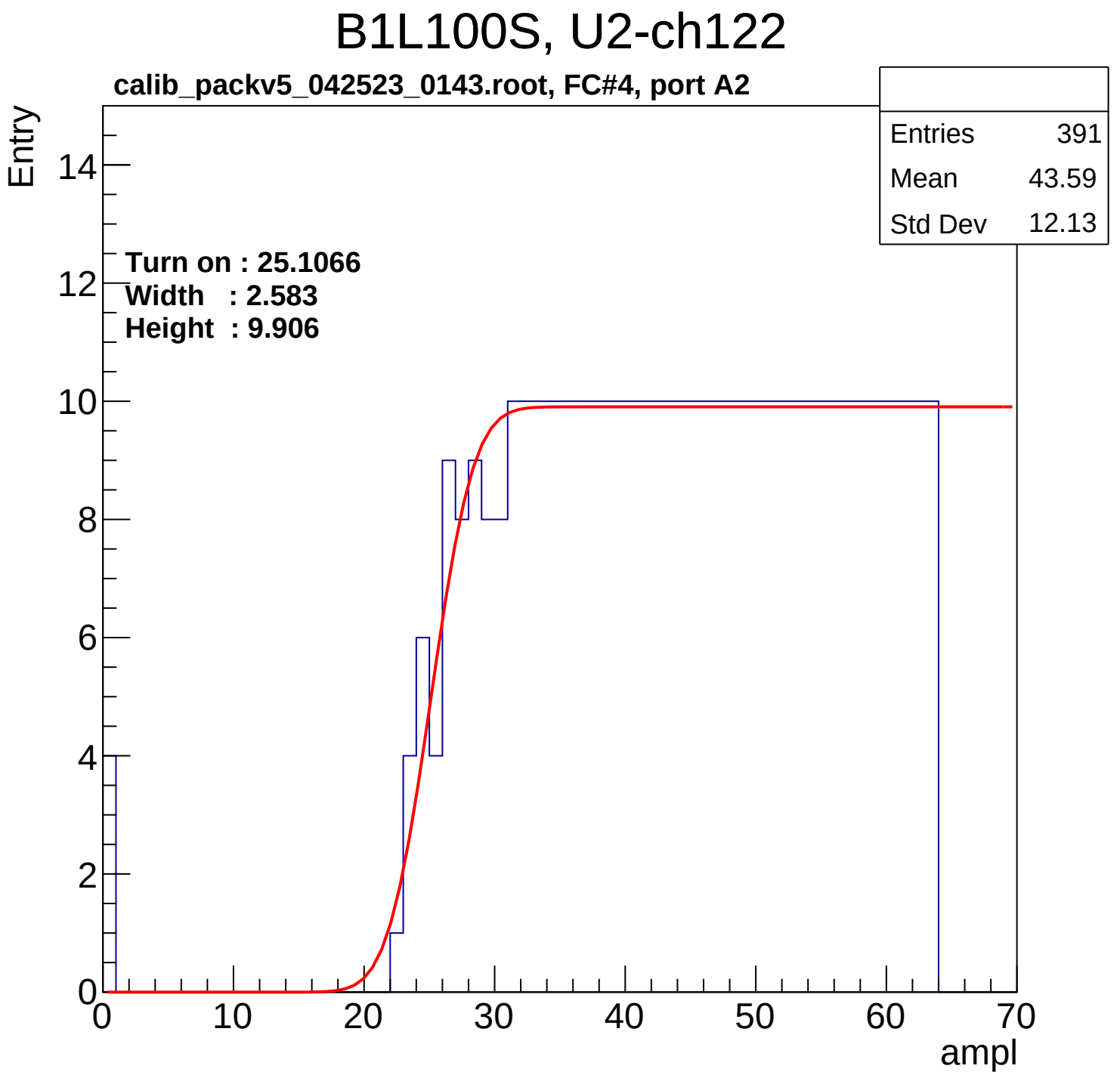
B1L100S, U2-ch122
calib_packv5_042523_0143.root, FC#4, port A2
Entries 391
Mean 43.59
Std Dev 12.13
Turn on : 25.1066
Width : 2.583
Height : 9.906
Entry
ampl
0
2
4
6
8
10
12
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10
20
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40
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60
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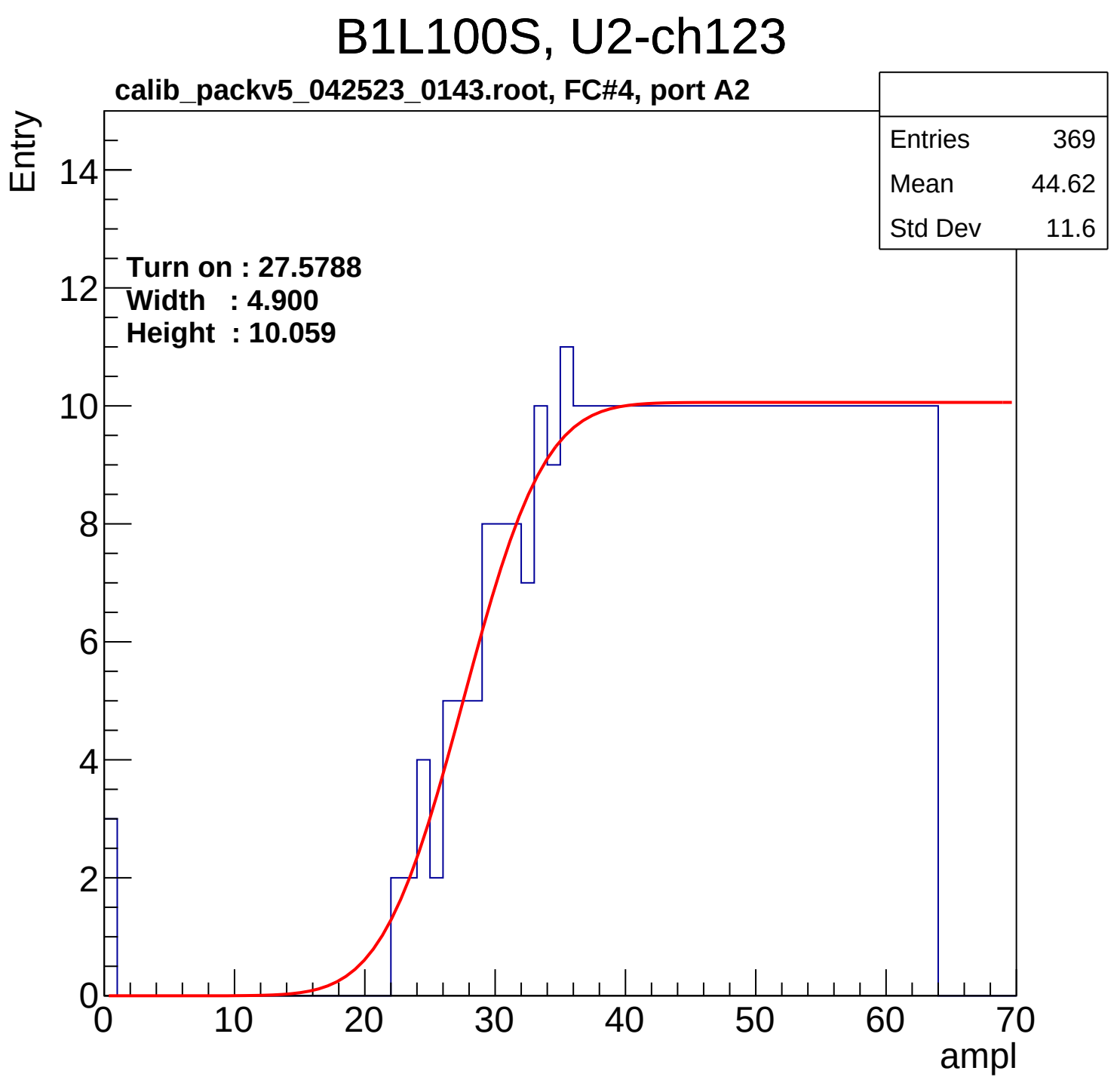
B1L100S, U2-ch123
calib_packv5_042523_0143.root, FC#4, port A2
Entries 369
Mean 44.62
Std Dev 11.6
Turn on : 27.5788
Width : 4.900
Height : 10.059
Entry
ampl
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2
4
6
8
10
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0
10
20
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40
50
60
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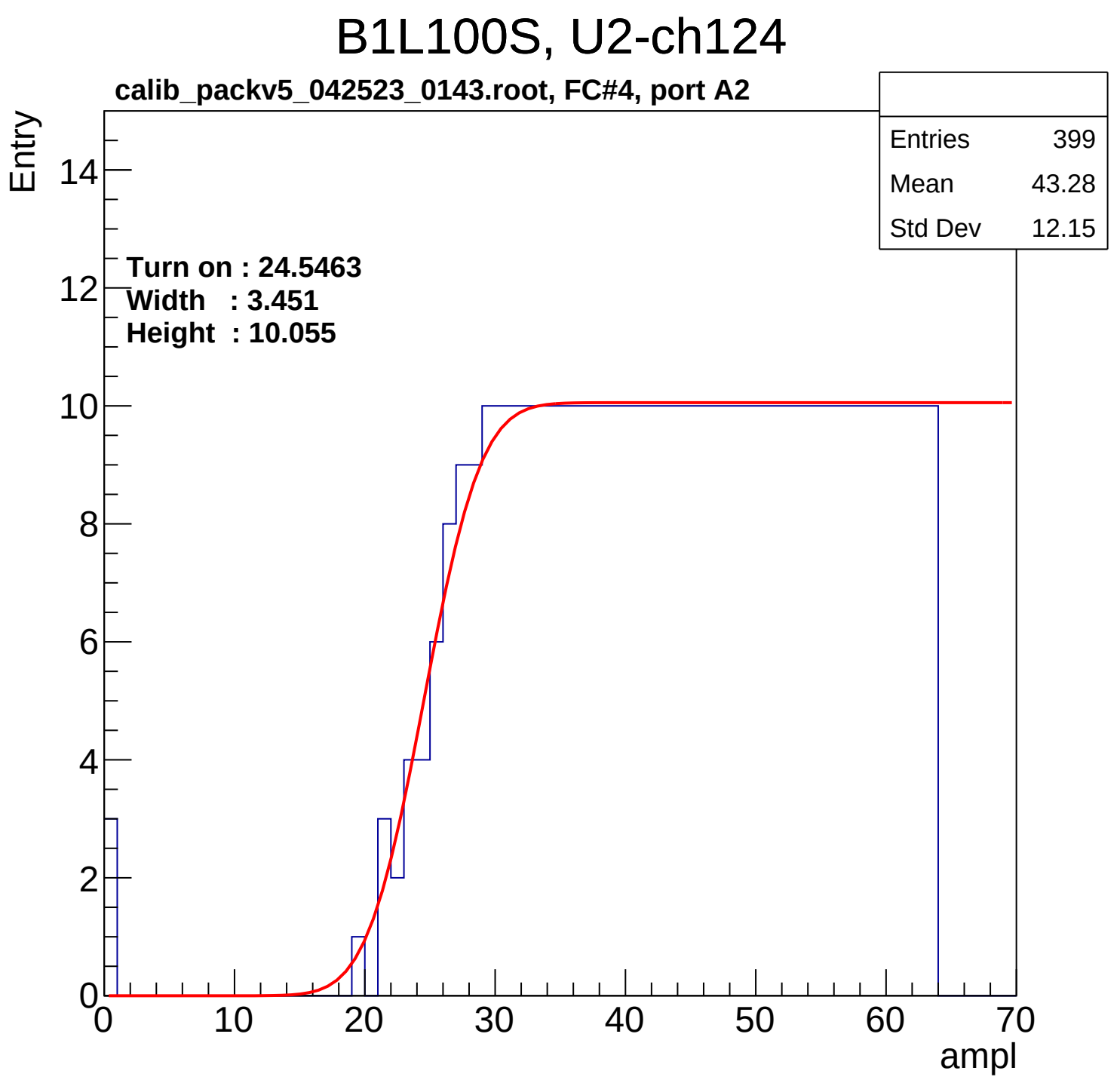
B1L100S, U2-ch124
calib_packv5_042523_0143.root, FC#4, port A2
Entries 399
Mean 43.28
Std Dev 12.15
Turn on : 24.5463
Width : 3.451
Height : 10.055
Entry
ampl
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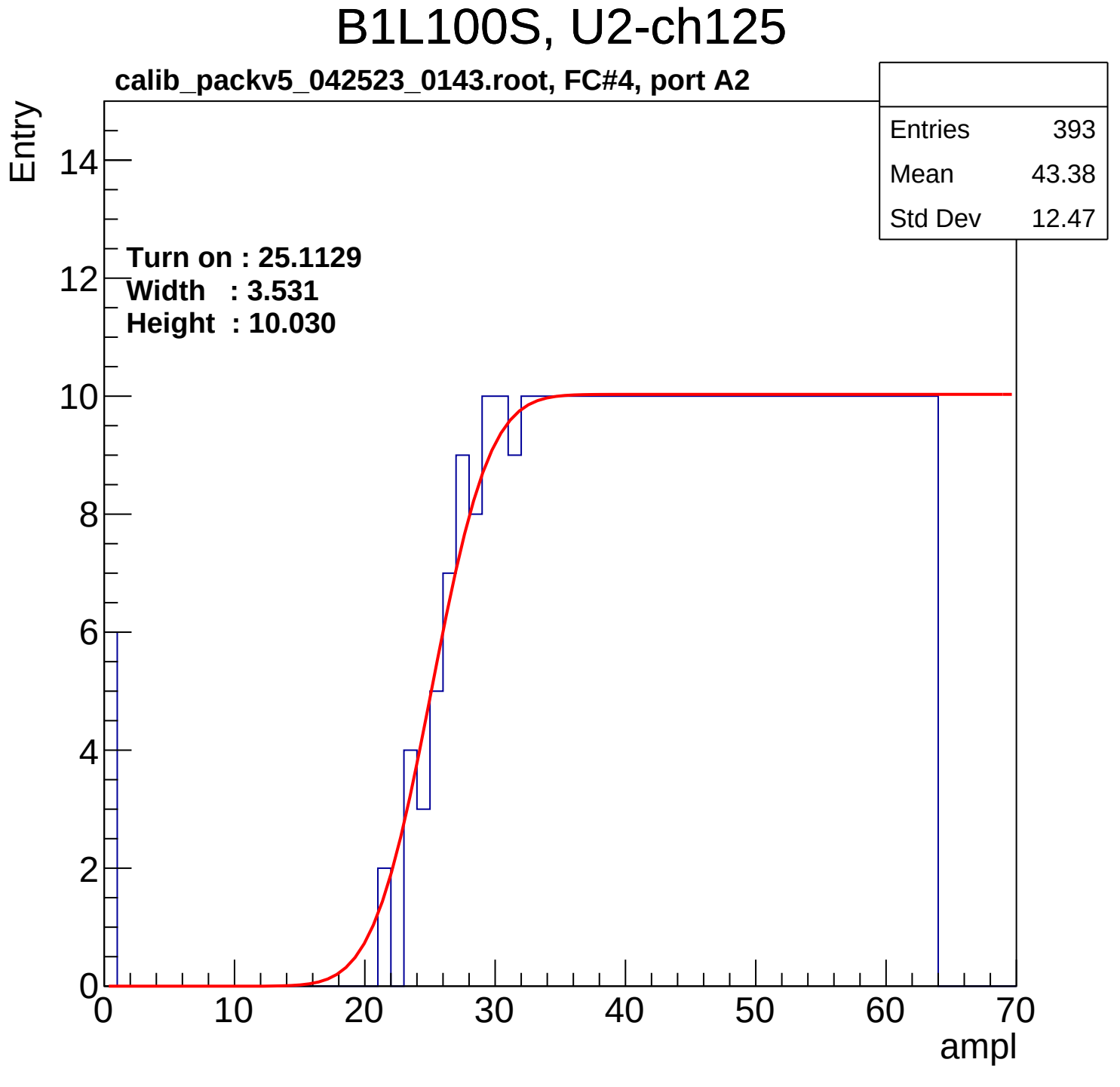
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L100S, U2-ch125
calib_packv5_042523_0143.root, FC#4, port A2
Entries 393
Mean 43.38
Std Dev 12.47
Turn on : 25.1129
Width : 3.531
Height : 10.030
Entry
ampl
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2
4
6
8
10
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60
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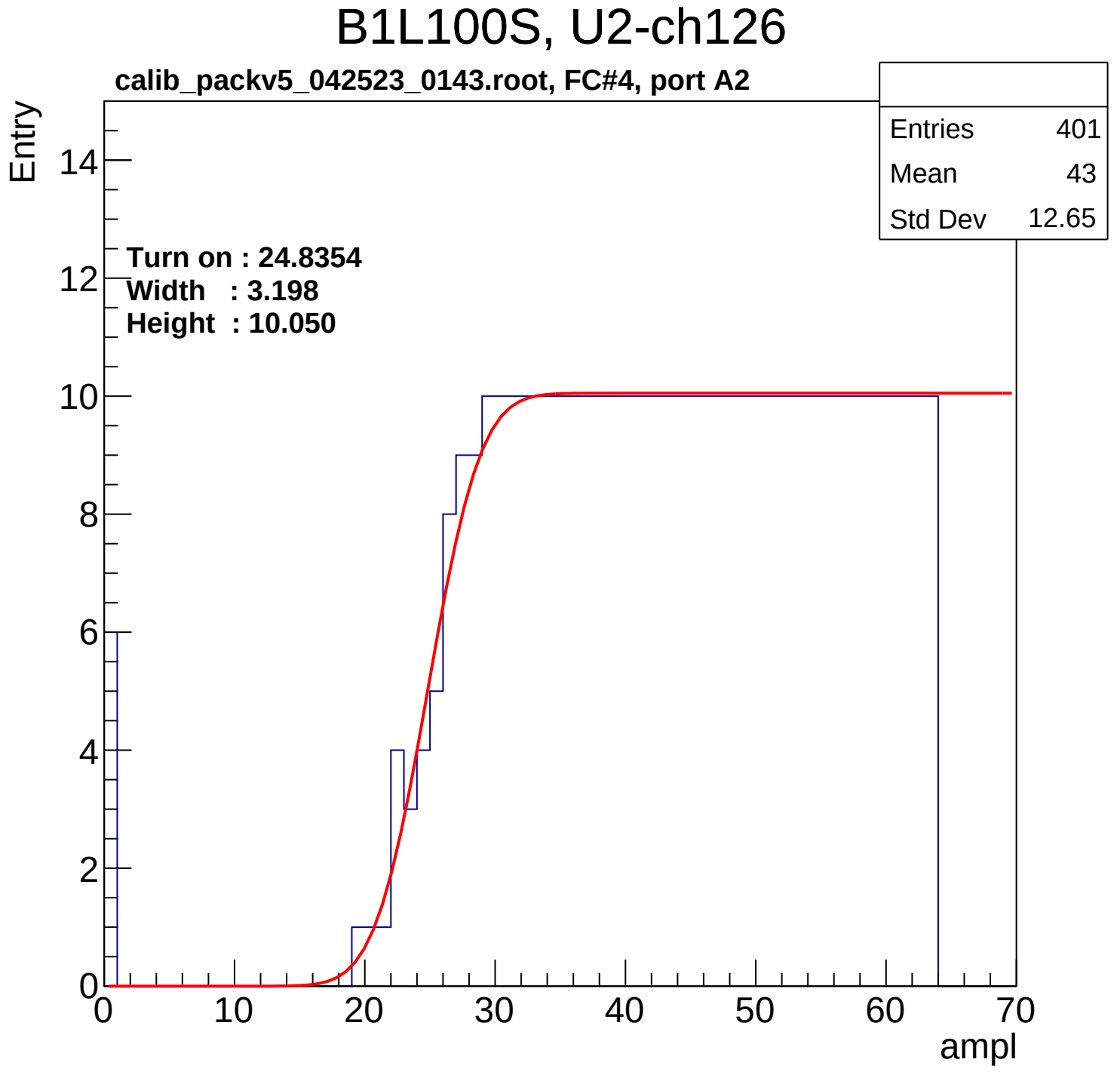
B1L100S, U2-ch126
calib_packv5_042523_0143.root, FC#4, port A2
Entries 401
Mean 43
Std Dev 12.65
Turn on : 24.8354
Width : 3.198
Height : 10.050
Entry
ampl
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4
6
8
10
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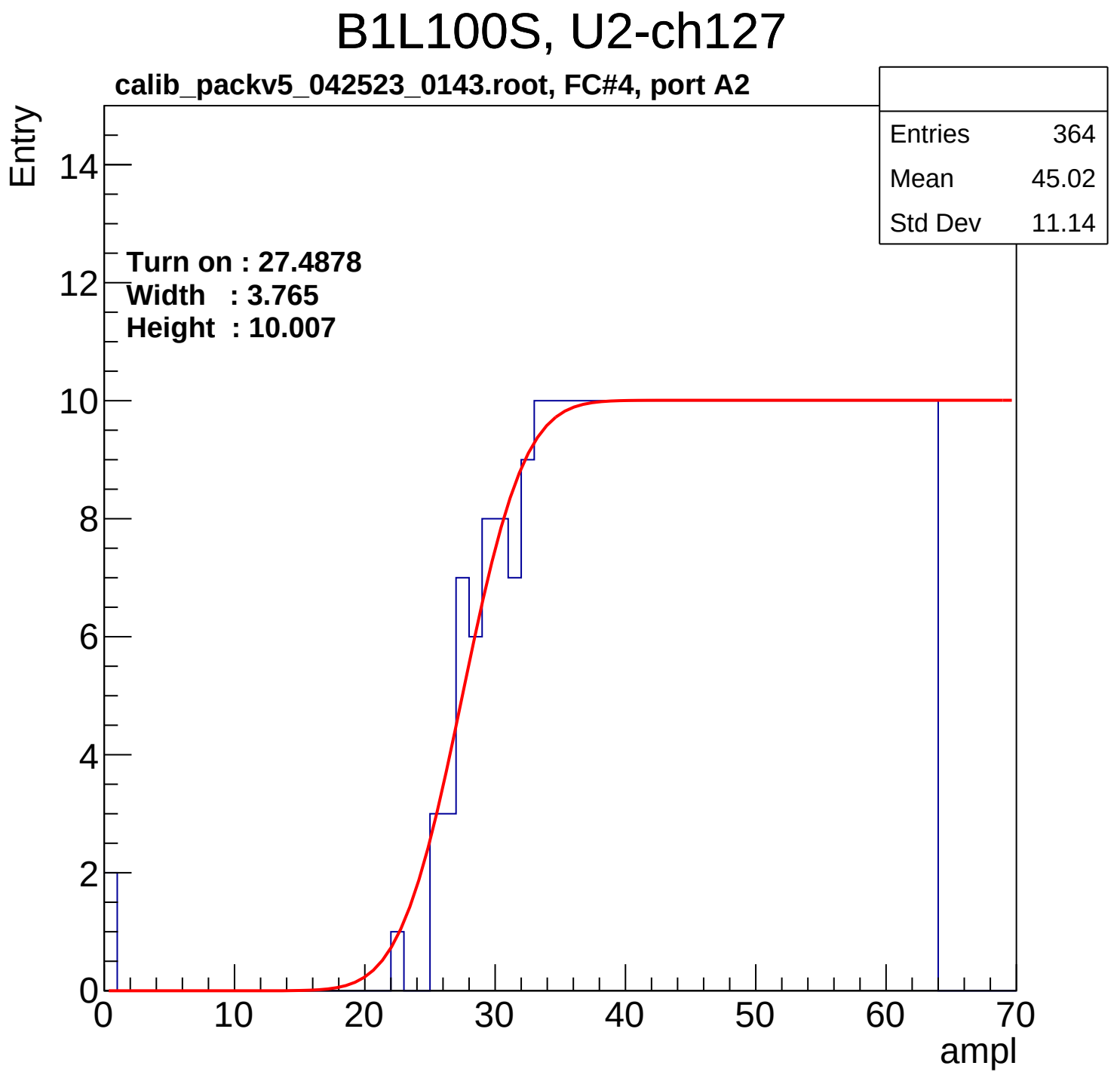
B1L100S, U2-ch127
calib_packv5_042523_0143.root, FC#4, port A2
Entries 364
Mean 45.02
Std Dev 11.14
Turn on : 27.4878
Width : 3.765
Height : 10.007
Entry
ampl
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4
6
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10
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0
10
20
30
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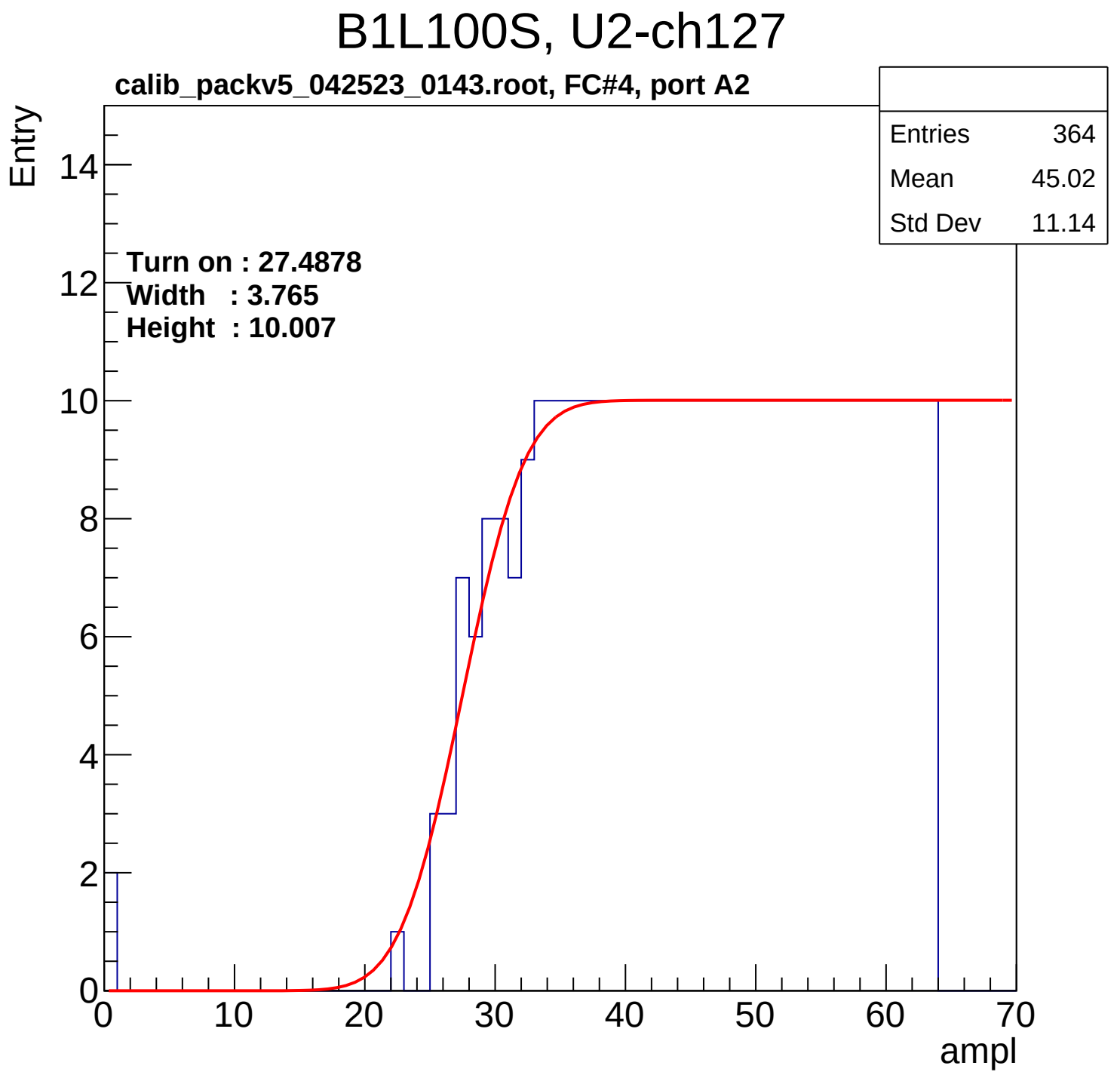
B1L100S, U2-ch127
calib_packv5_042523_0143.root, FC#4, port A2
Entries 364
Mean 45.02
Std Dev 11.14
Turn on : 27.4878
Width : 3.765
Height : 10.007
Entry
ampl
0
2
4
6
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20
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