



# B1L101S, U22-ch0, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	93
Mean	31.92
Std Dev	3.771

**Gaus mean : 32.6909**

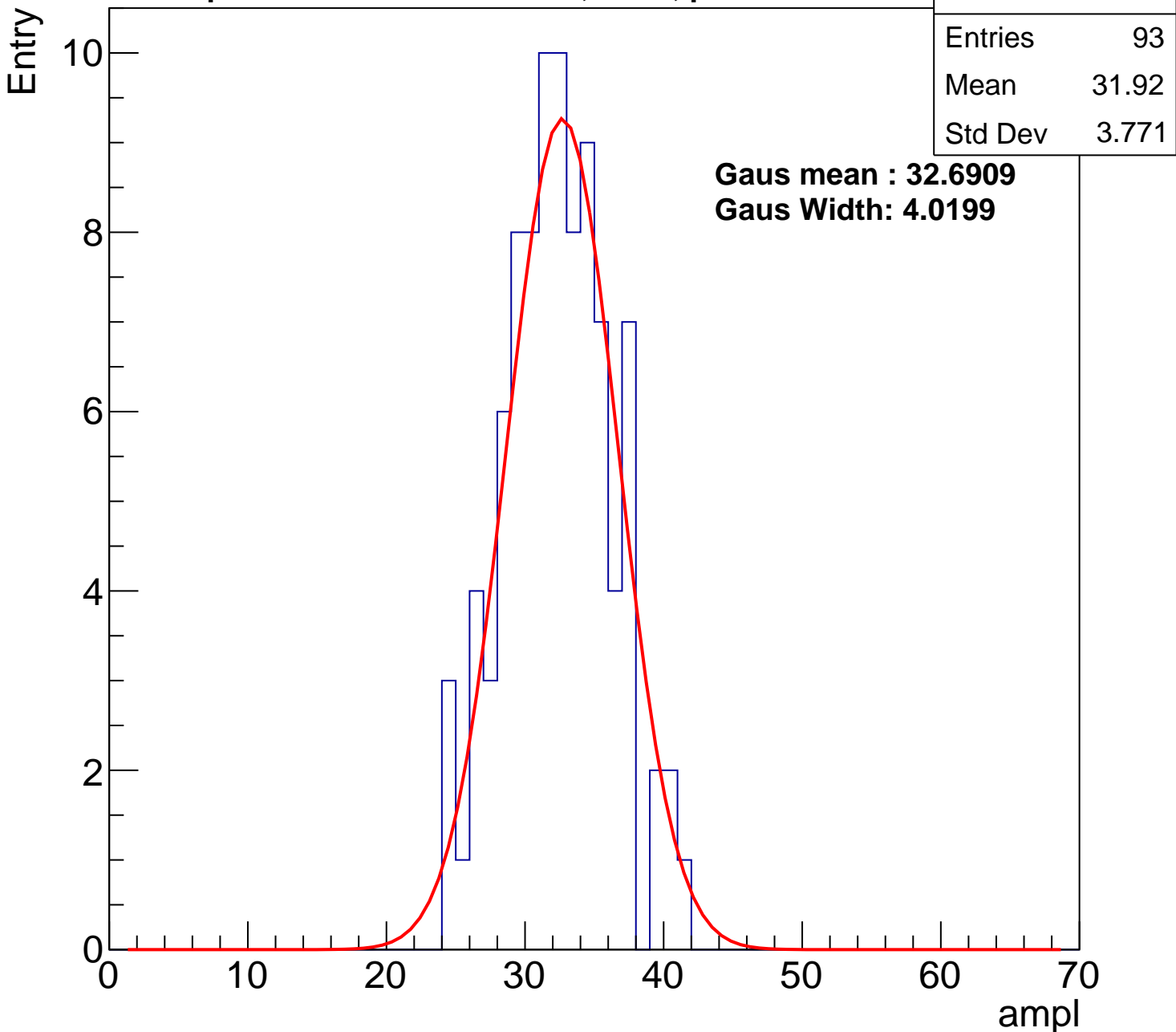
**Gaus Width: 4.0199**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U22-ch0, adc1

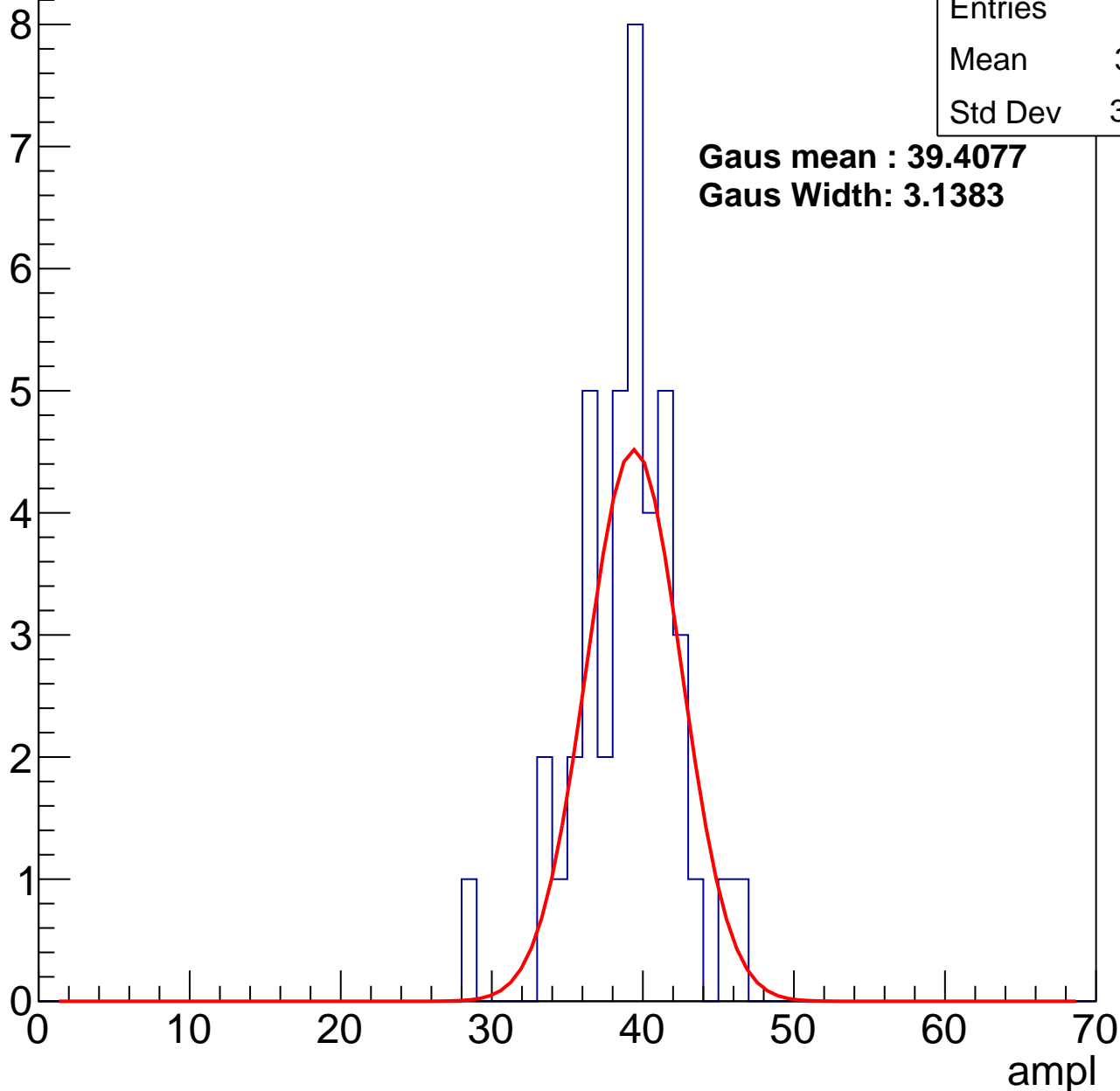
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	41
Mean	38.51
Std Dev	3.314

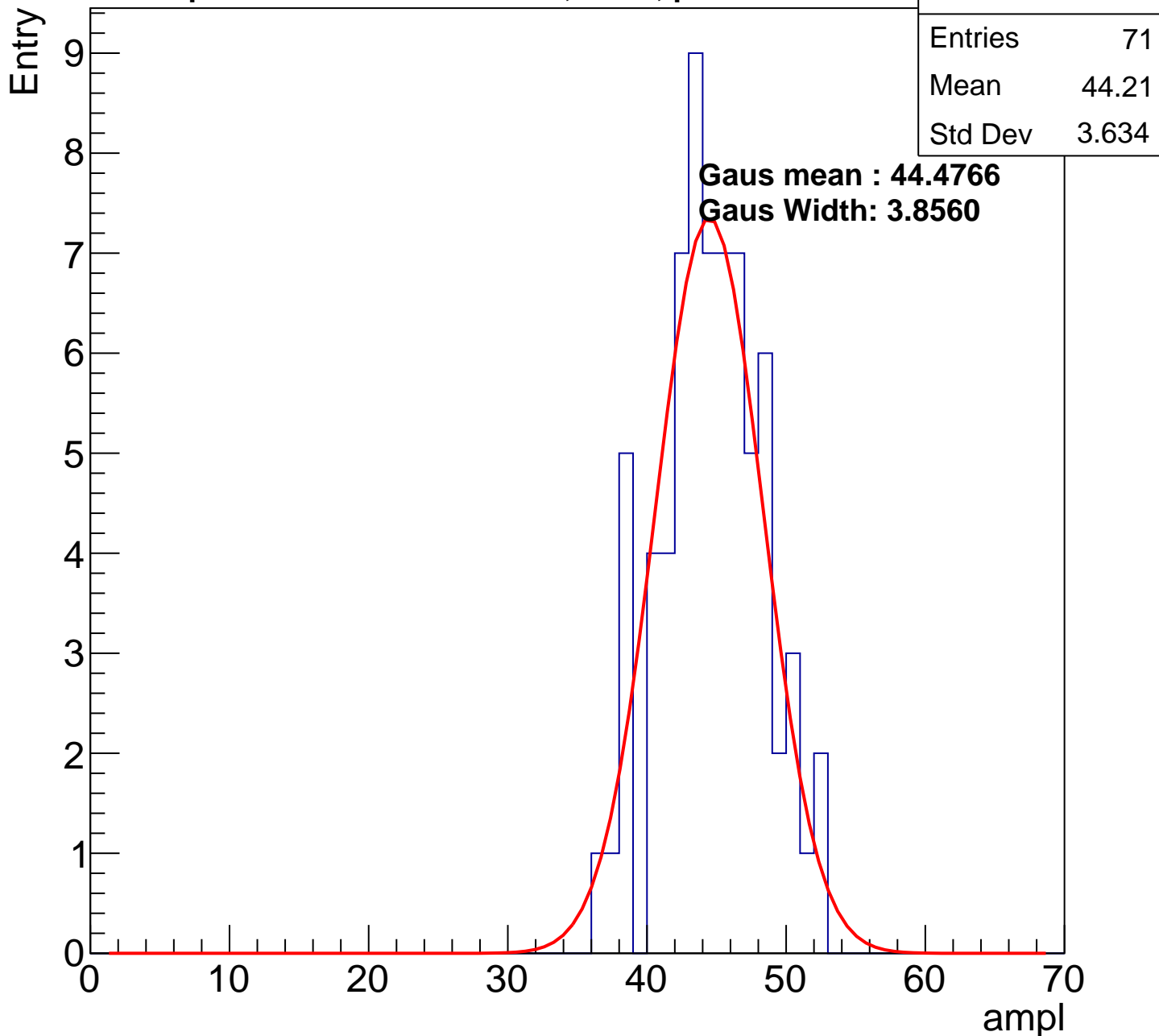
**Gaus mean : 39.4077**

**Gaus Width: 3.1383**



# B1L101S, U22-ch0, adc2

calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U22-ch0, adc3

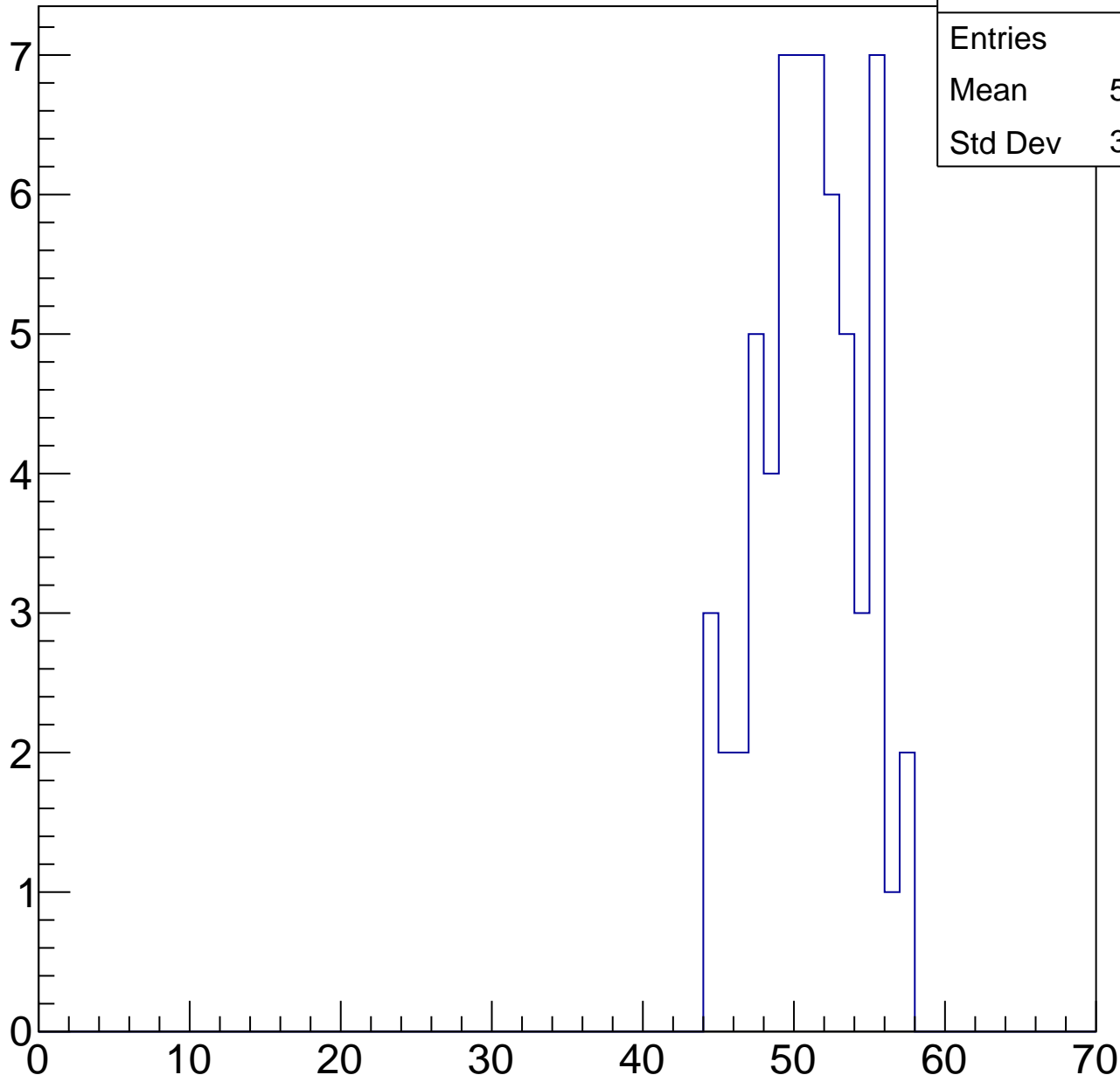
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

7  
6  
5  
4  
3  
2  
1  
0

Entries	61
Mean	50.57
Std Dev	3.316

ampl



# B1L101S, U22-ch0, adc4

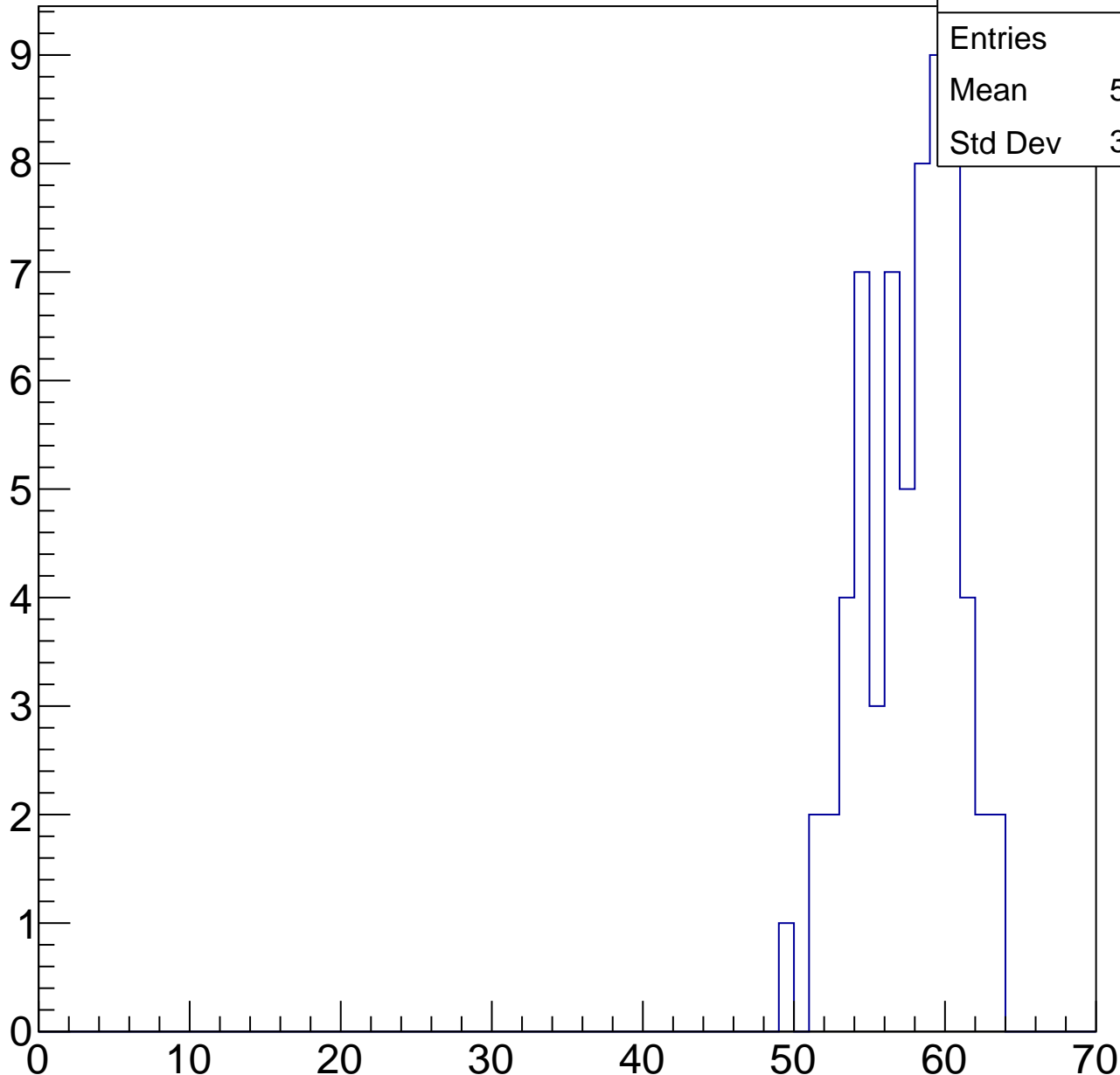
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	64
Mean	57.12
Std Dev	3.145

ampl

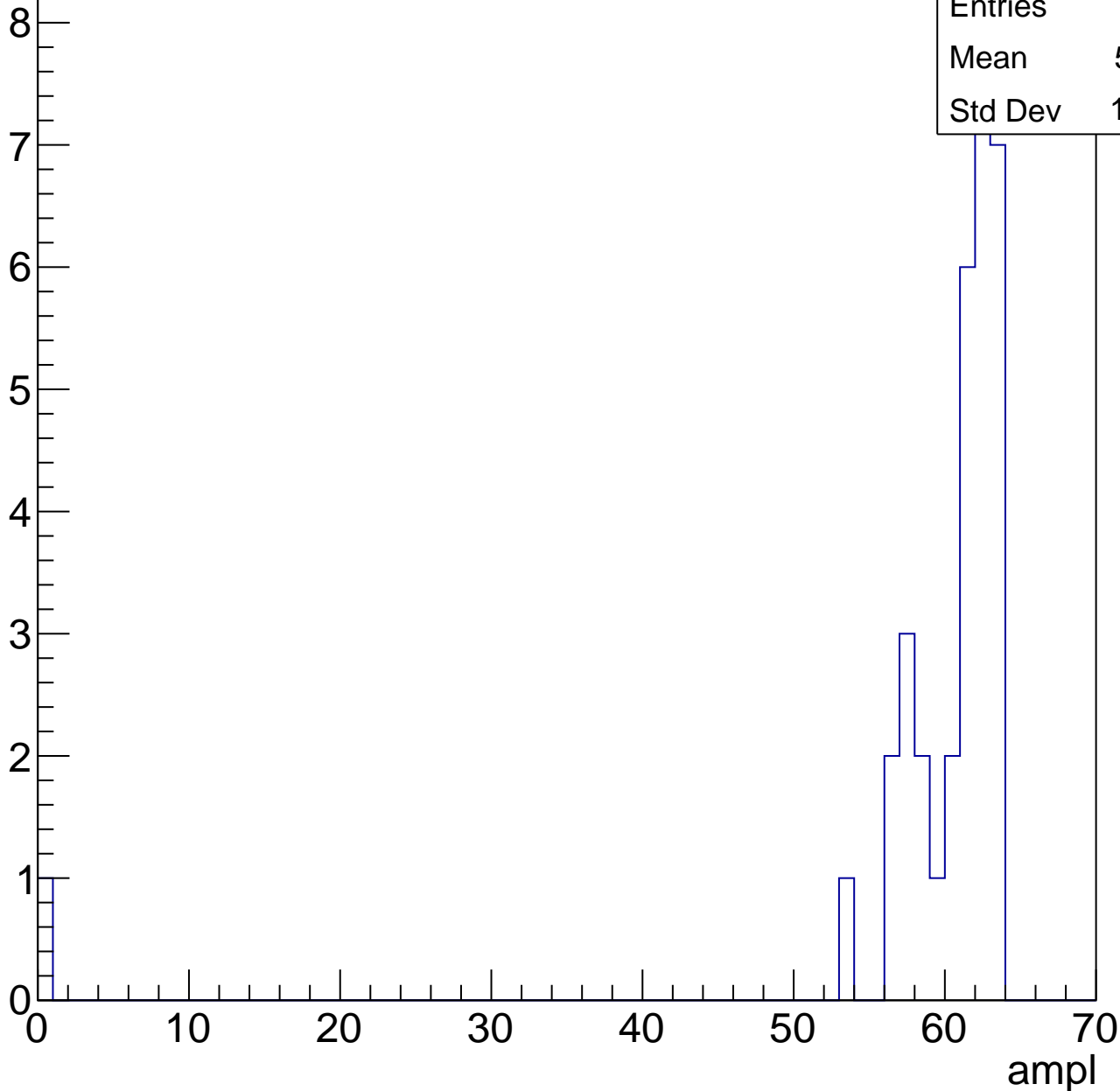


# B1L101S, U22-ch0, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	33
Mean	58.61
Std Dev	10.67



# B1L101S, U22-ch0, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U22-ch0, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	2
Mean	11.5
Std Dev	11.5

# B1L101S, U22-ch1, adc0

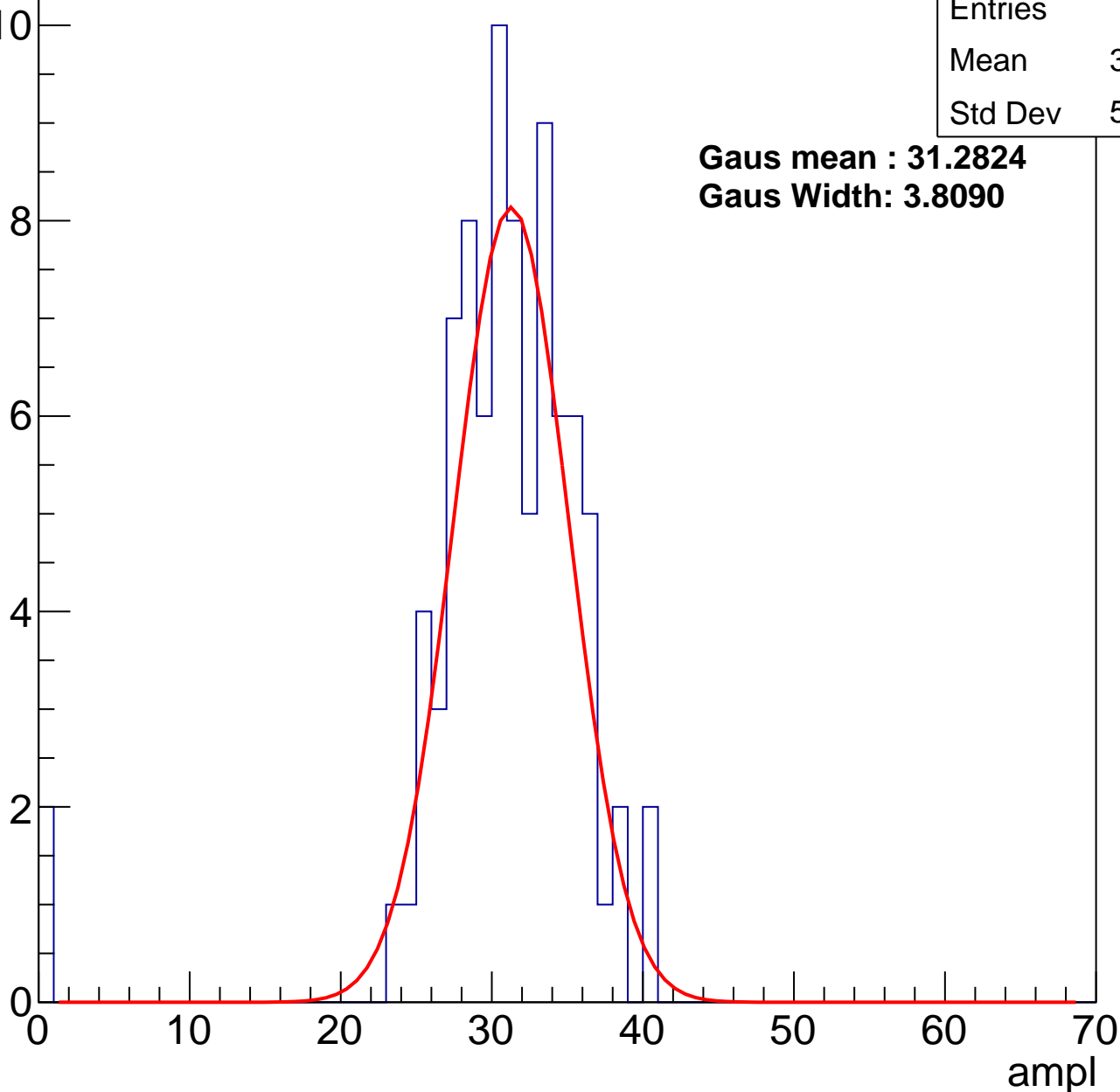
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	86
Mean	30.28
Std Dev	5.945

**Gaus mean : 31.2824**

**Gaus Width: 3.8090**



# B1L101S, U22-ch1, adc1

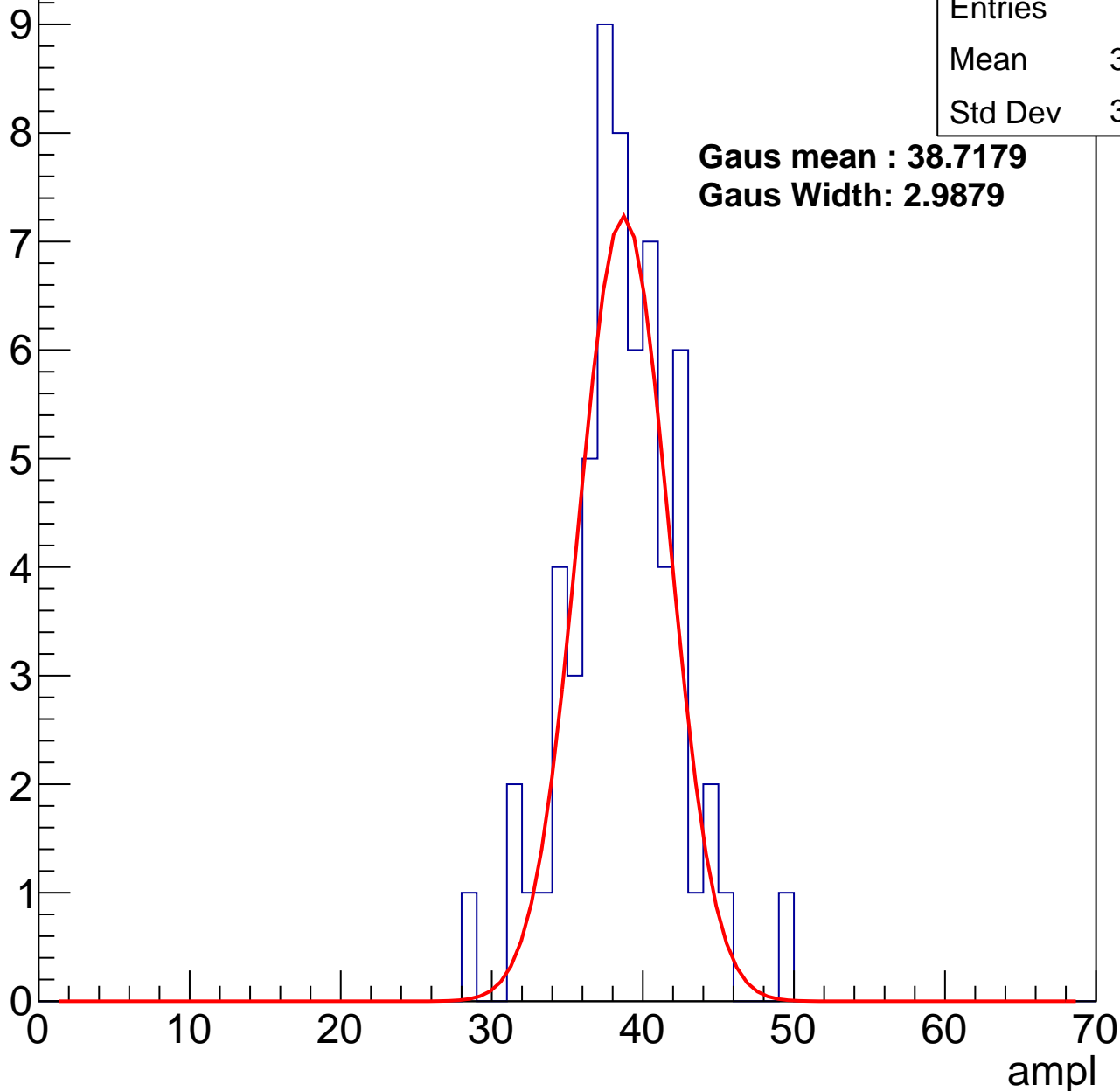
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	38.19
Std Dev	3.614

**Gaus mean : 38.7179**

**Gaus Width: 2.9879**



# B1L101S, U22-ch1, adc2

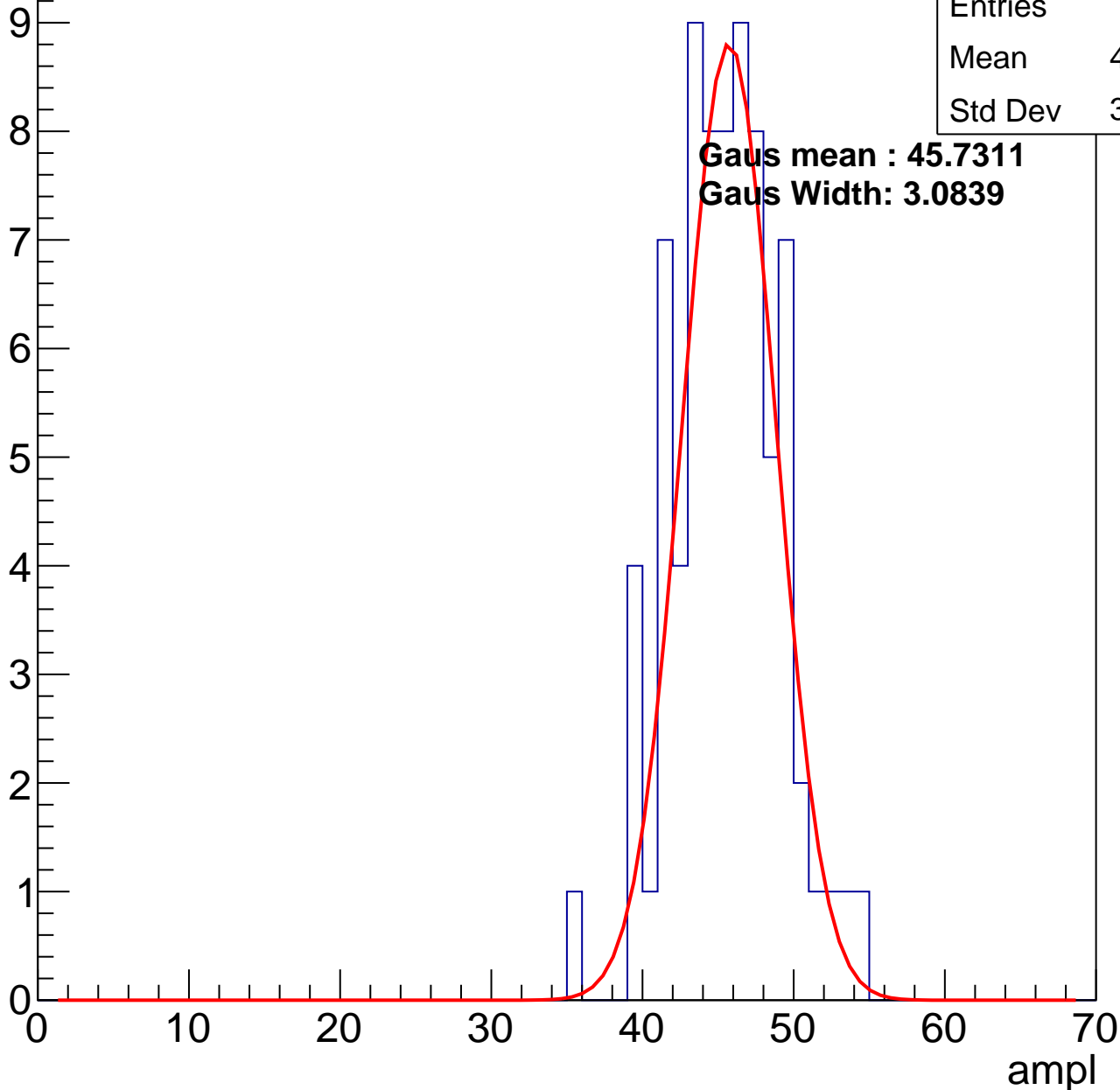
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	77
Mean	45.04
Std Dev	3.492

**Gaus mean : 45.7311**

**Gaus Width: 3.0839**

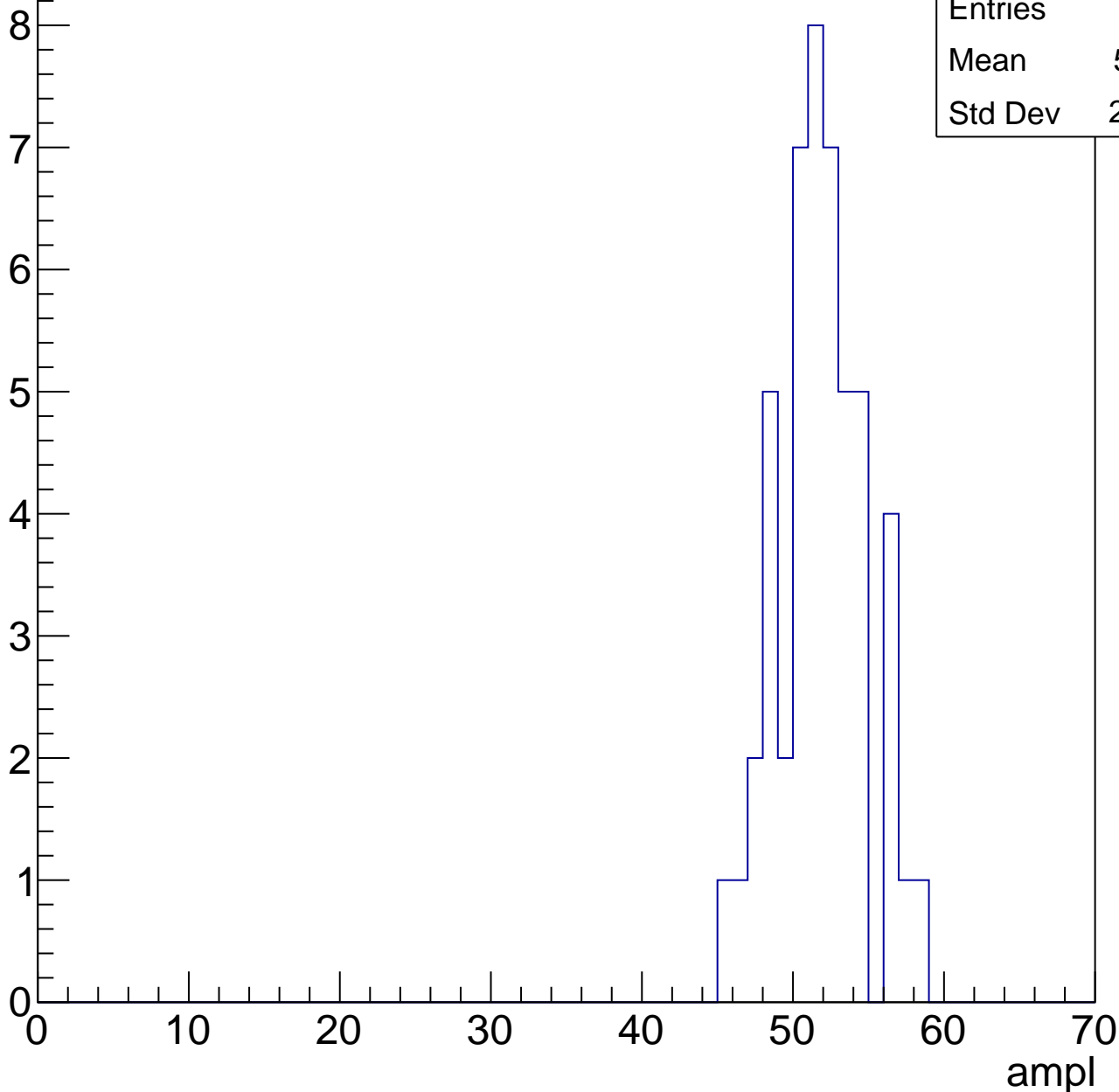


# B1L101S, U22-ch1, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	49
Mean	51.41
Std Dev	2.864

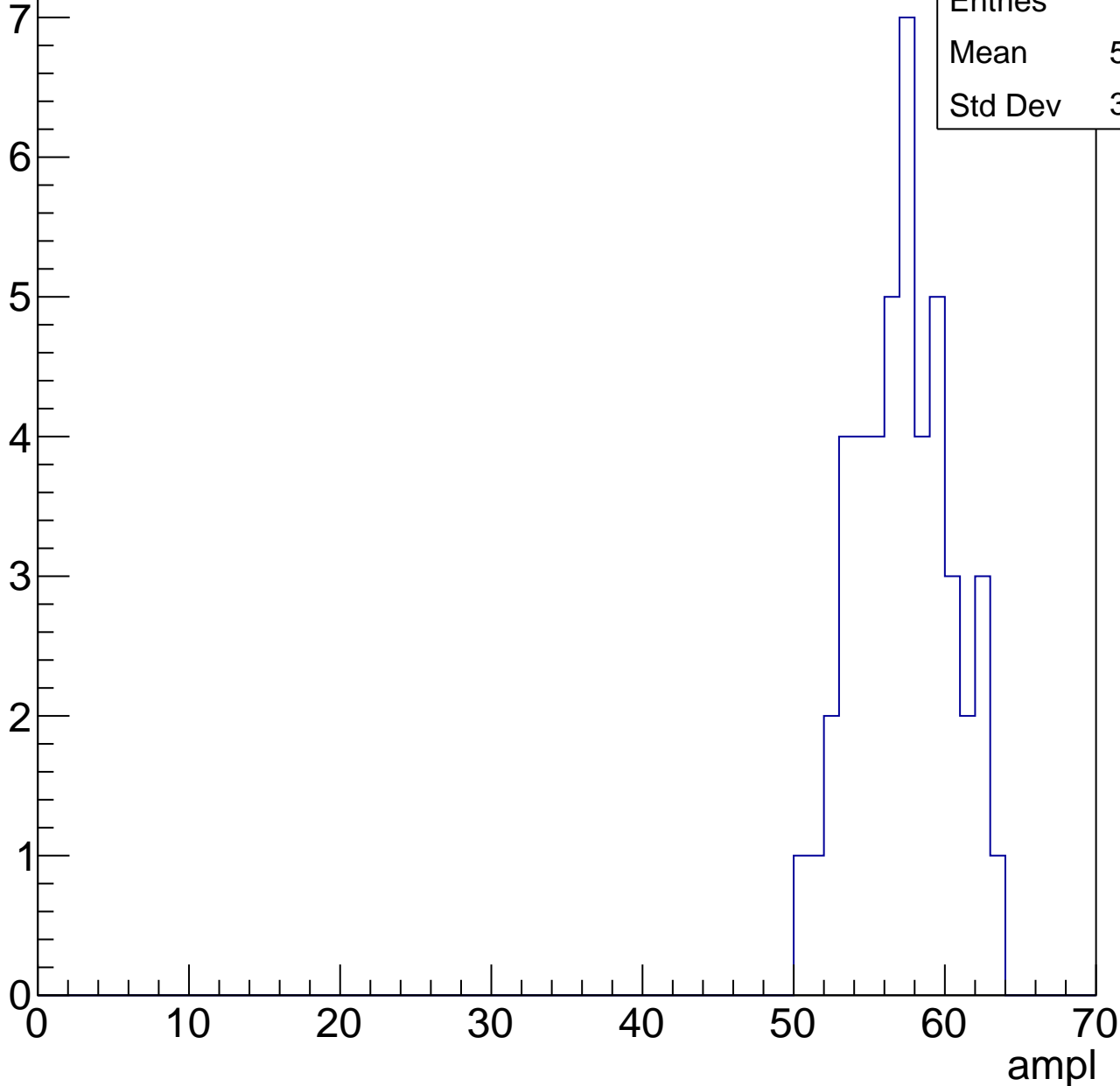


# B1L101S, U22-ch1, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	46
Mean	56.74
Std Dev	3.117

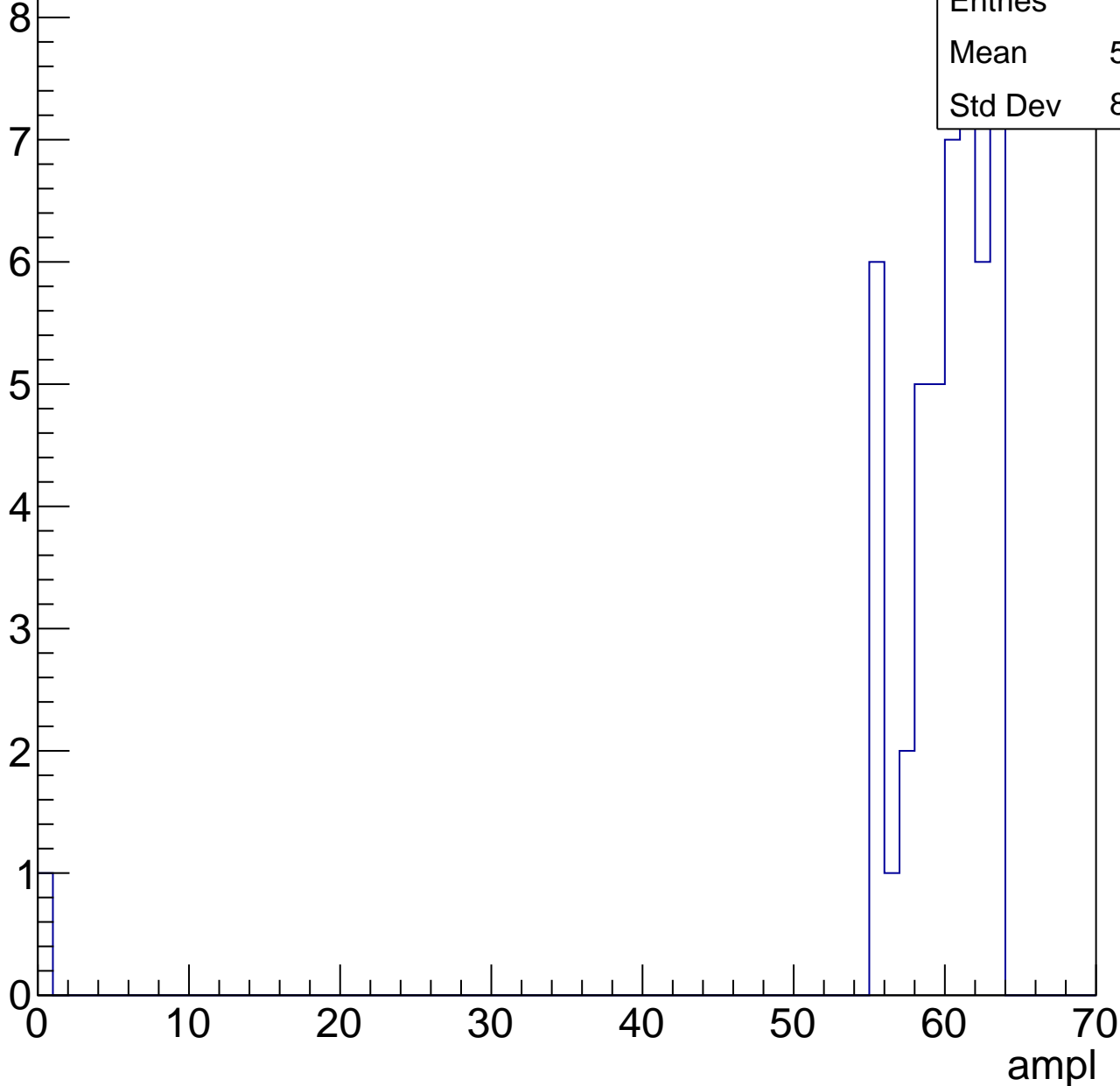


# B1L101S, U22-ch1, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	49
Mean	58.55
Std Dev	8.818



# B1L101S, U22-ch1, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U22-ch1, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L101S, U22-ch2, adc0

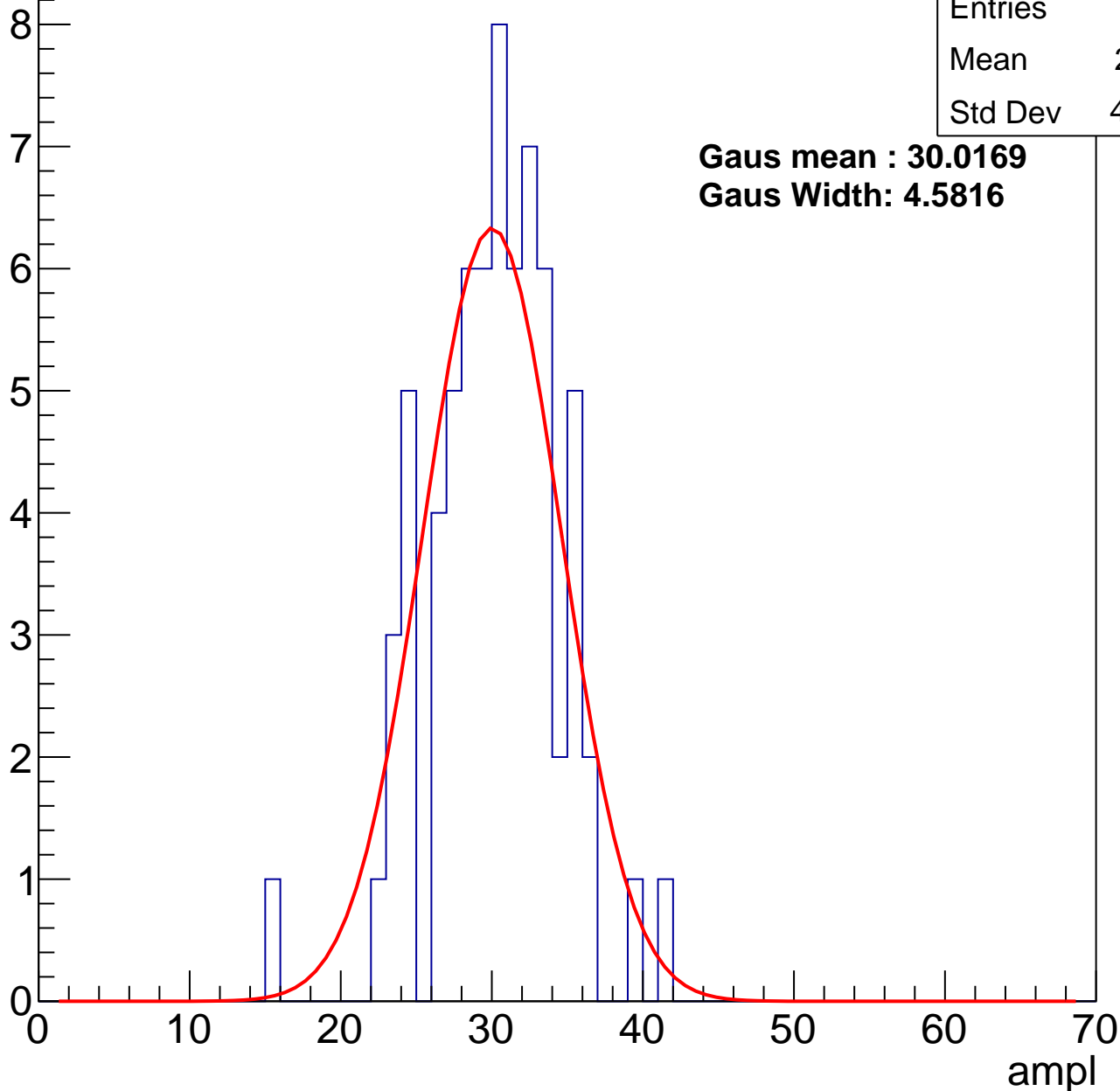
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	29.71
Std Dev	4.287

**Gaus mean : 30.0169**

**Gaus Width: 4.5816**



# B1L101S, U22-ch2, adc1

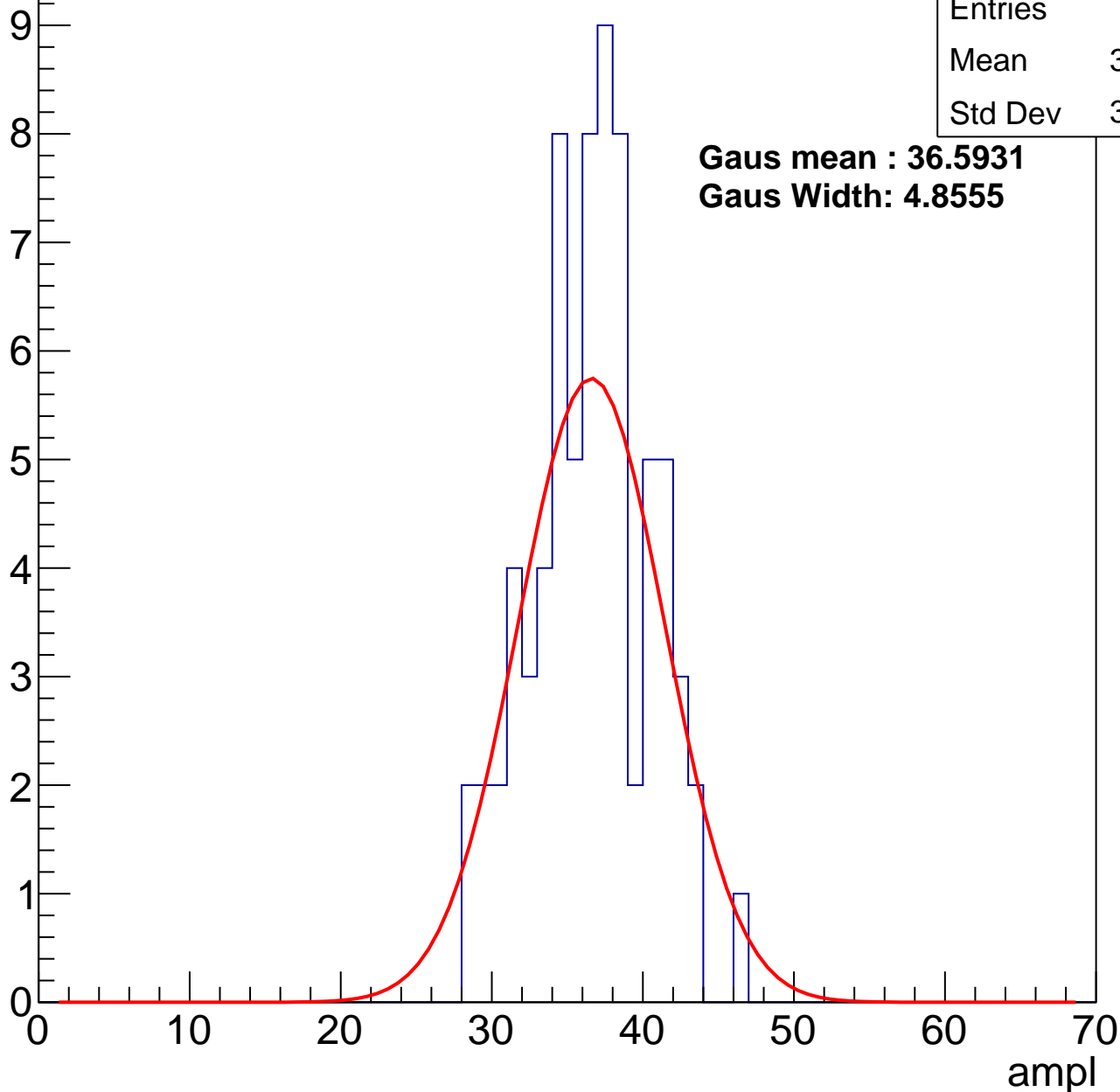
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	73
Mean	36.15
Std Dev	3.859

**Gaus mean : 36.5931**

**Gaus Width: 4.8555**



# B1L101S, U22-ch2, adc2

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	80
Mean	44.26
Std Dev	3.622

**Gaus mean : 44.7900**

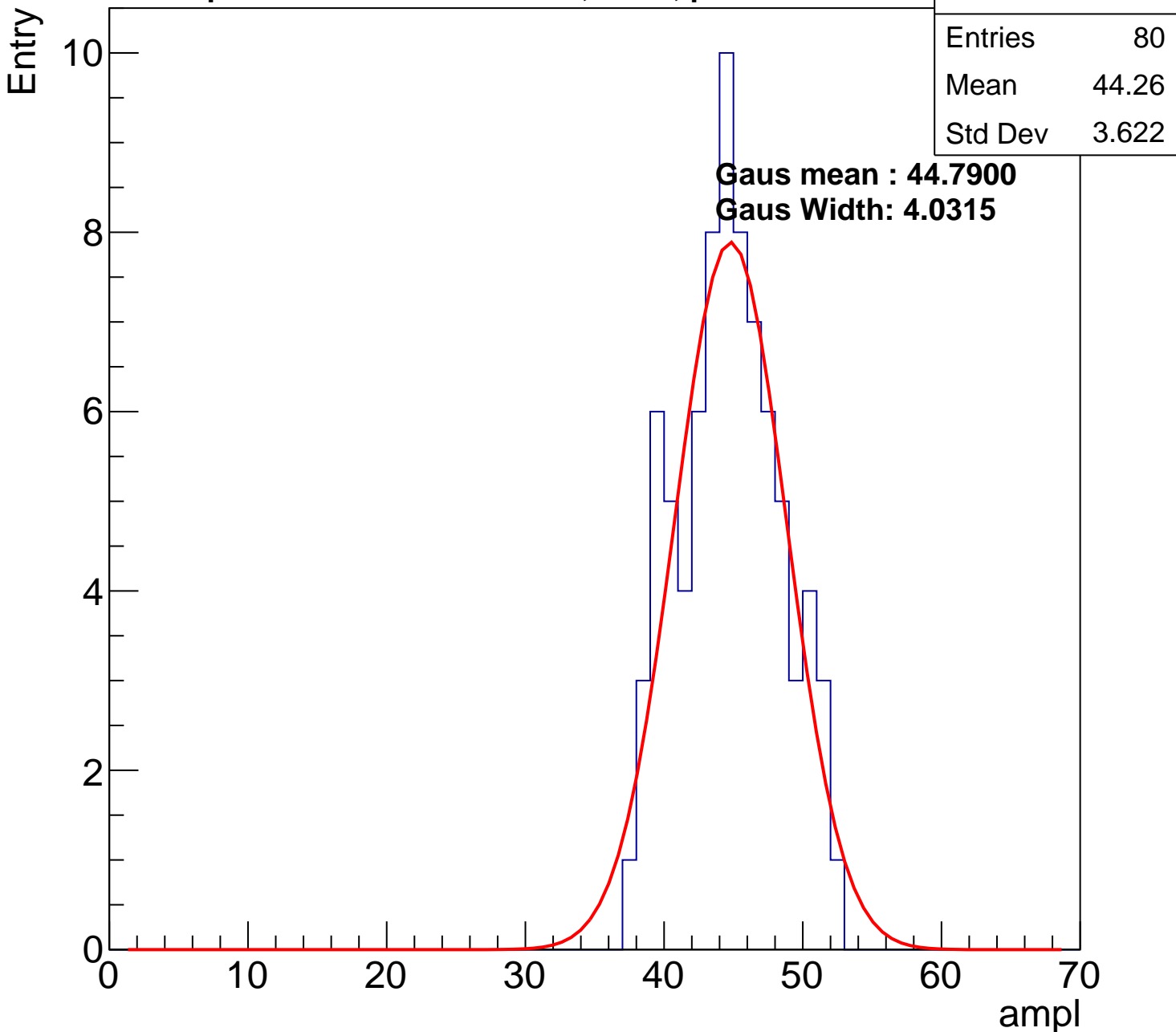
**Gaus Width: 4.0315**

Entry

10  
8  
6  
4  
2  
0

ampl

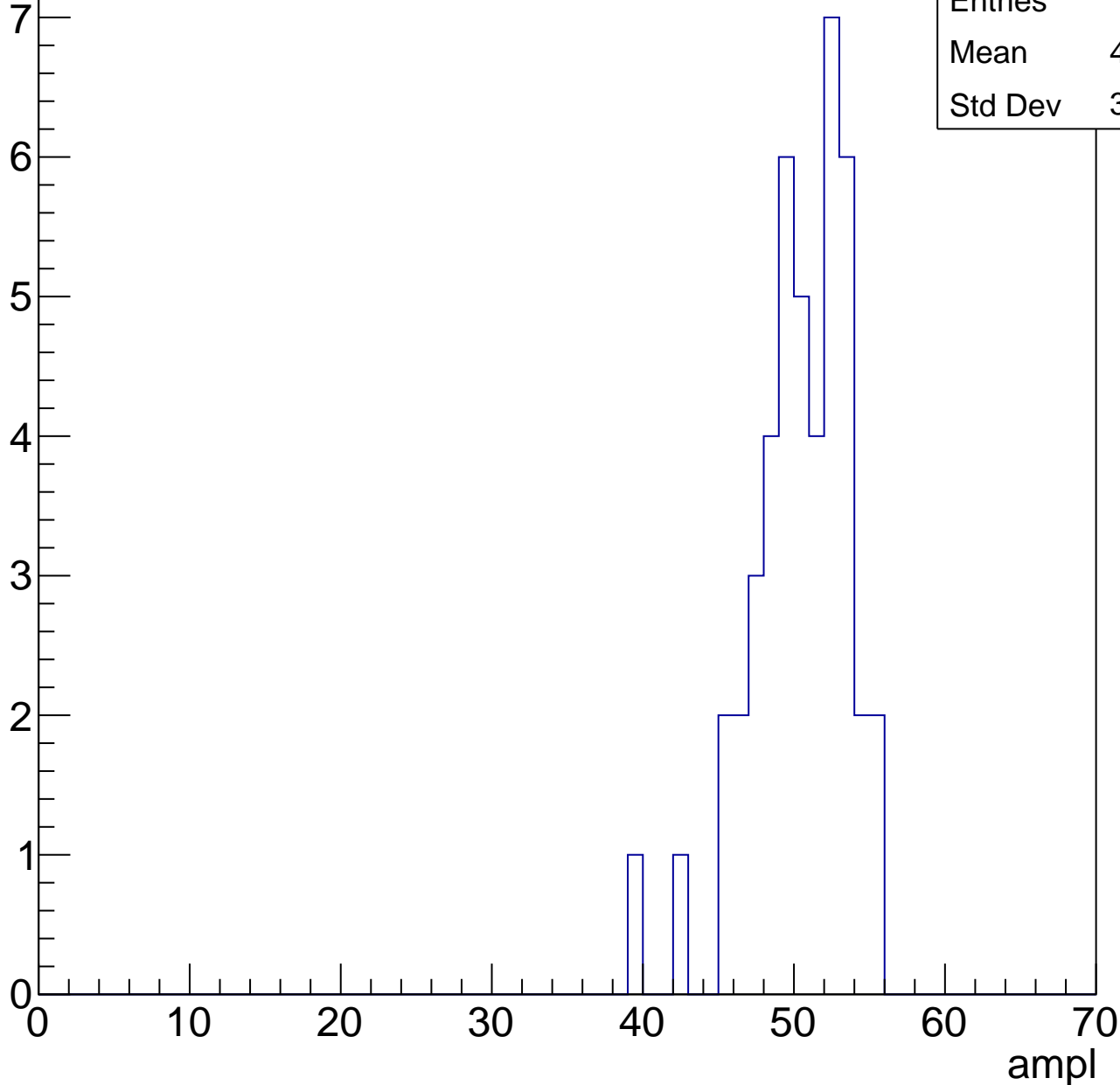
0 10 20 30 40 50 60 70



# B1L101S, U22-ch2, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

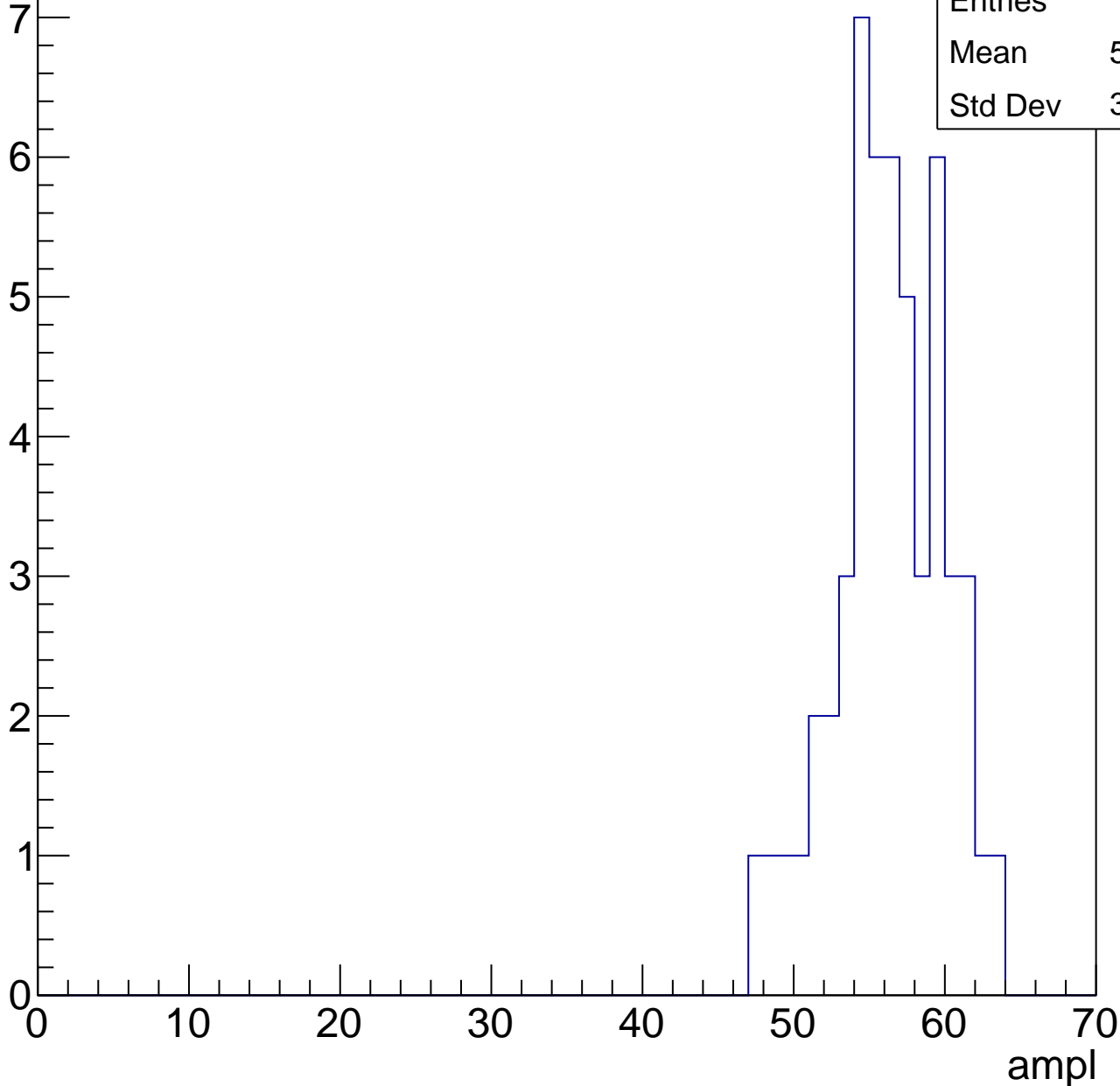


# B1L101S, U22-ch2, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	52
Mean	55.85
Std Dev	3.538

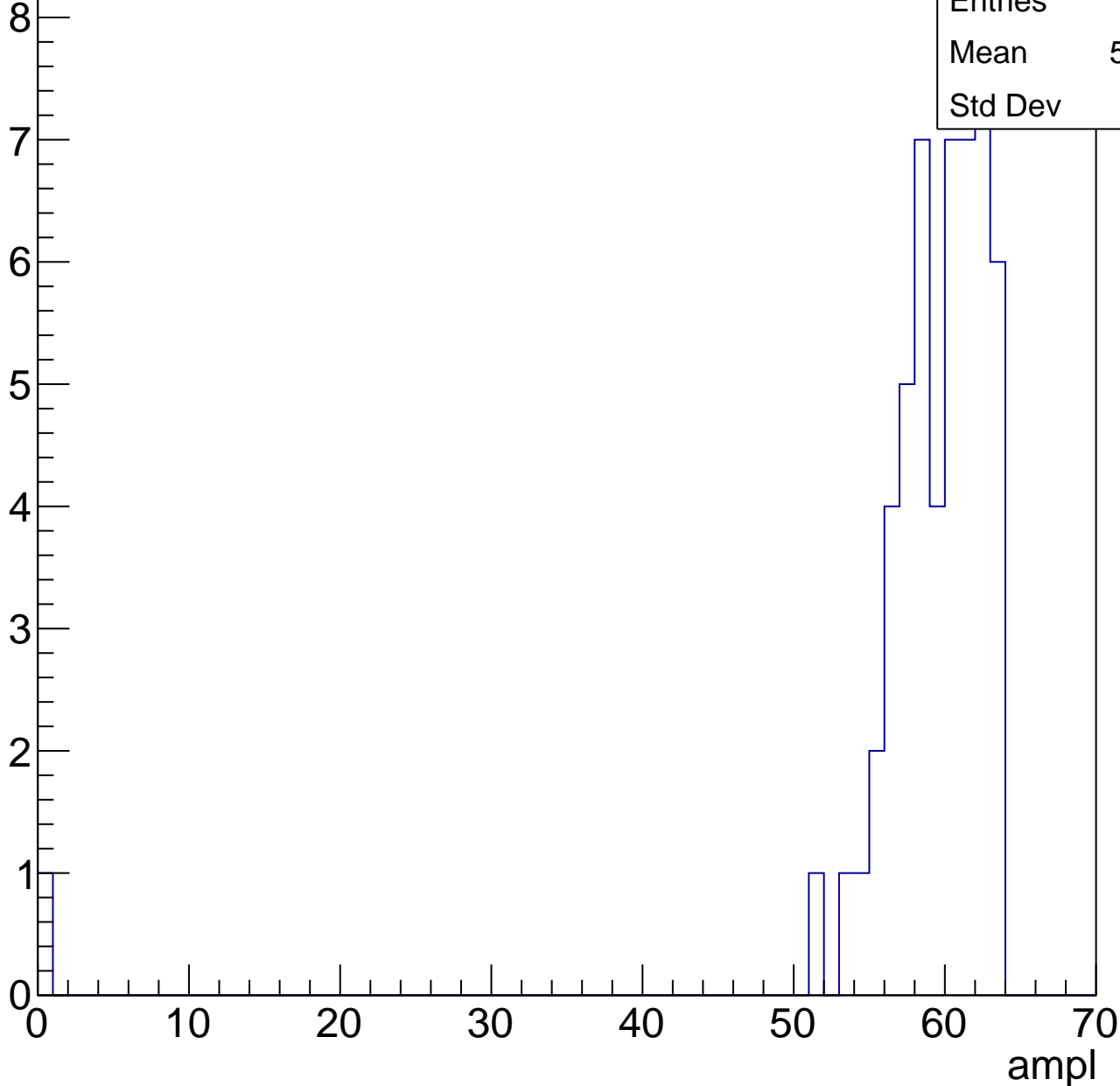


# B1L101S, U22-ch2, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	54
Mean	58.15
Std Dev	8.46



# B1L101S, U22-ch2, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U22-ch2, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U22-ch3, adc0

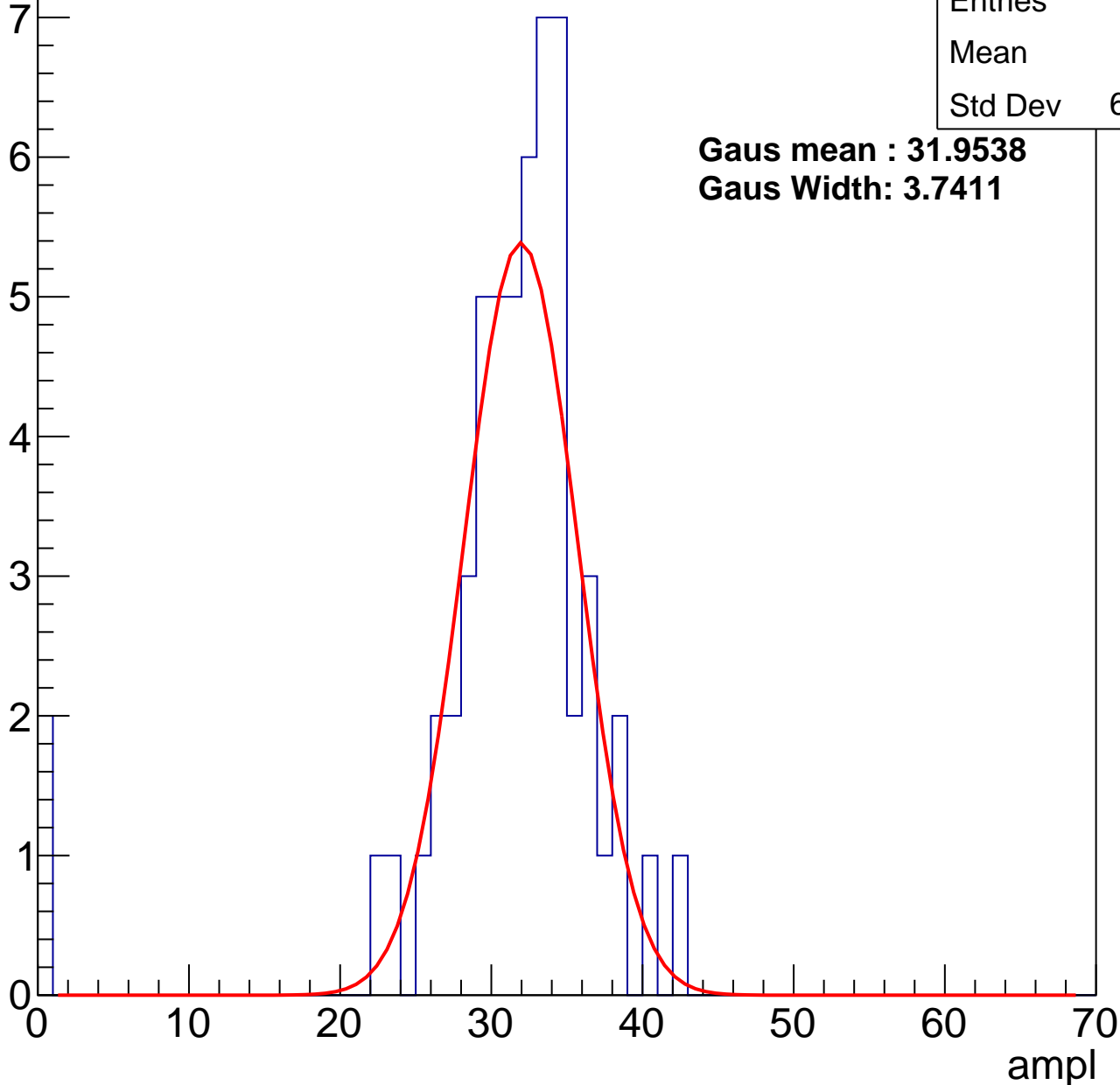
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	57
Mean	30.6
Std Dev	6.968

**Gaus mean : 31.9538**

**Gaus Width: 3.7411**



# B1L101S, U22-ch3, adc1

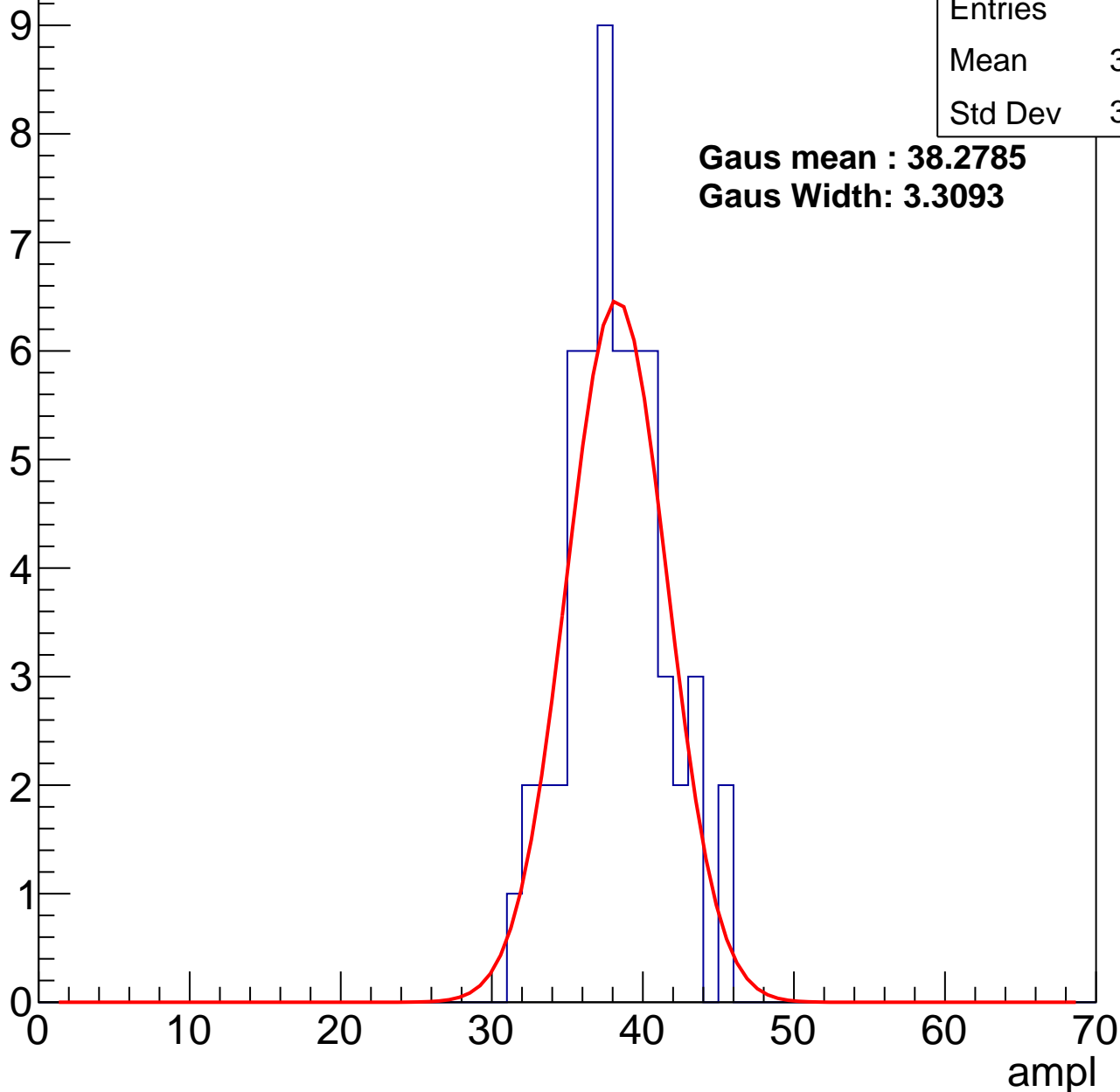
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	56
Mean	37.79
Std Dev	3.132

**Gaus mean : 38.2785**

**Gaus Width: 3.3093**



# B1L101S, U22-ch3, adc2

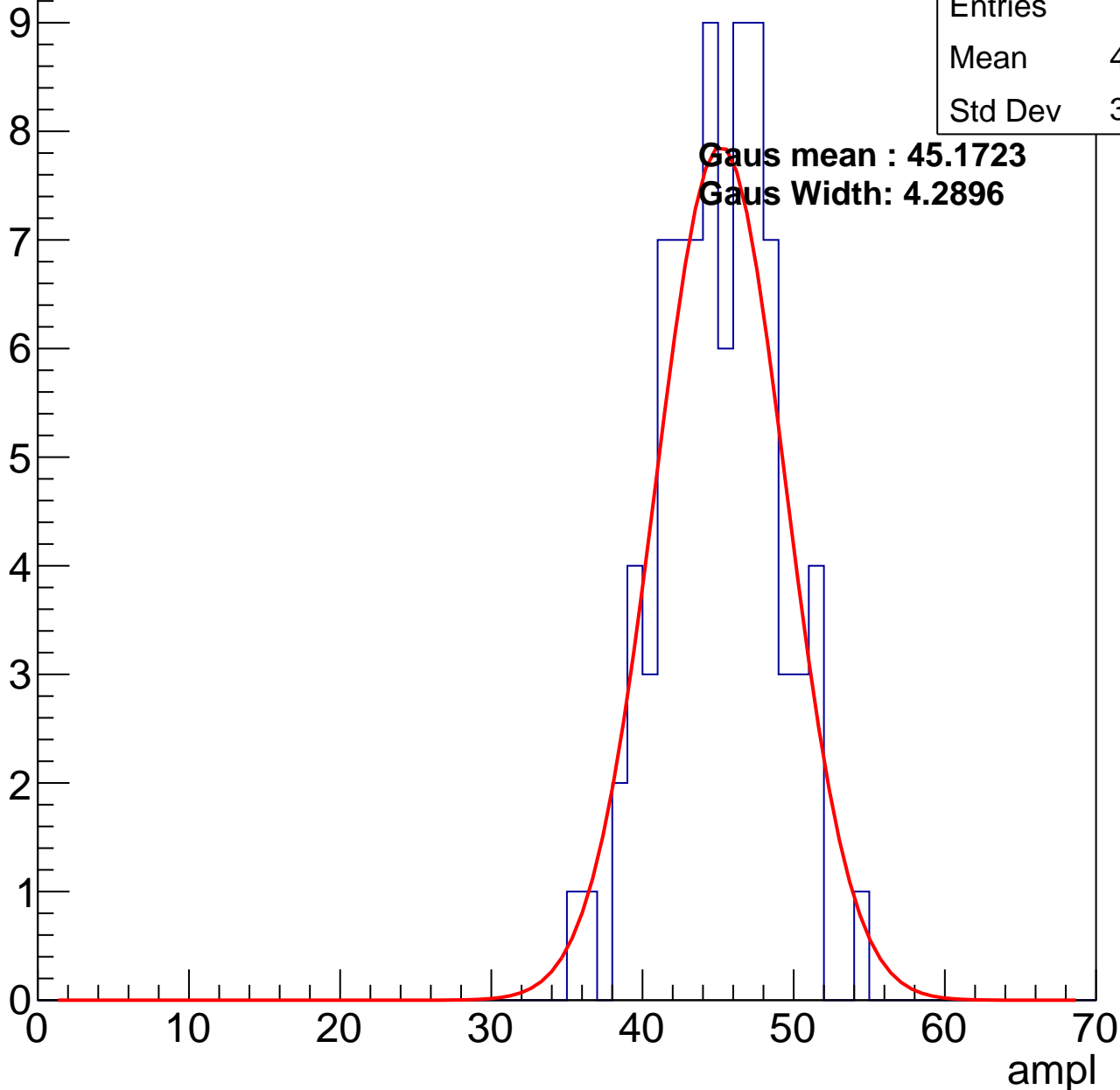
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	83
Mean	44.57
Std Dev	3.723

**Gaus mean : 45.1723**

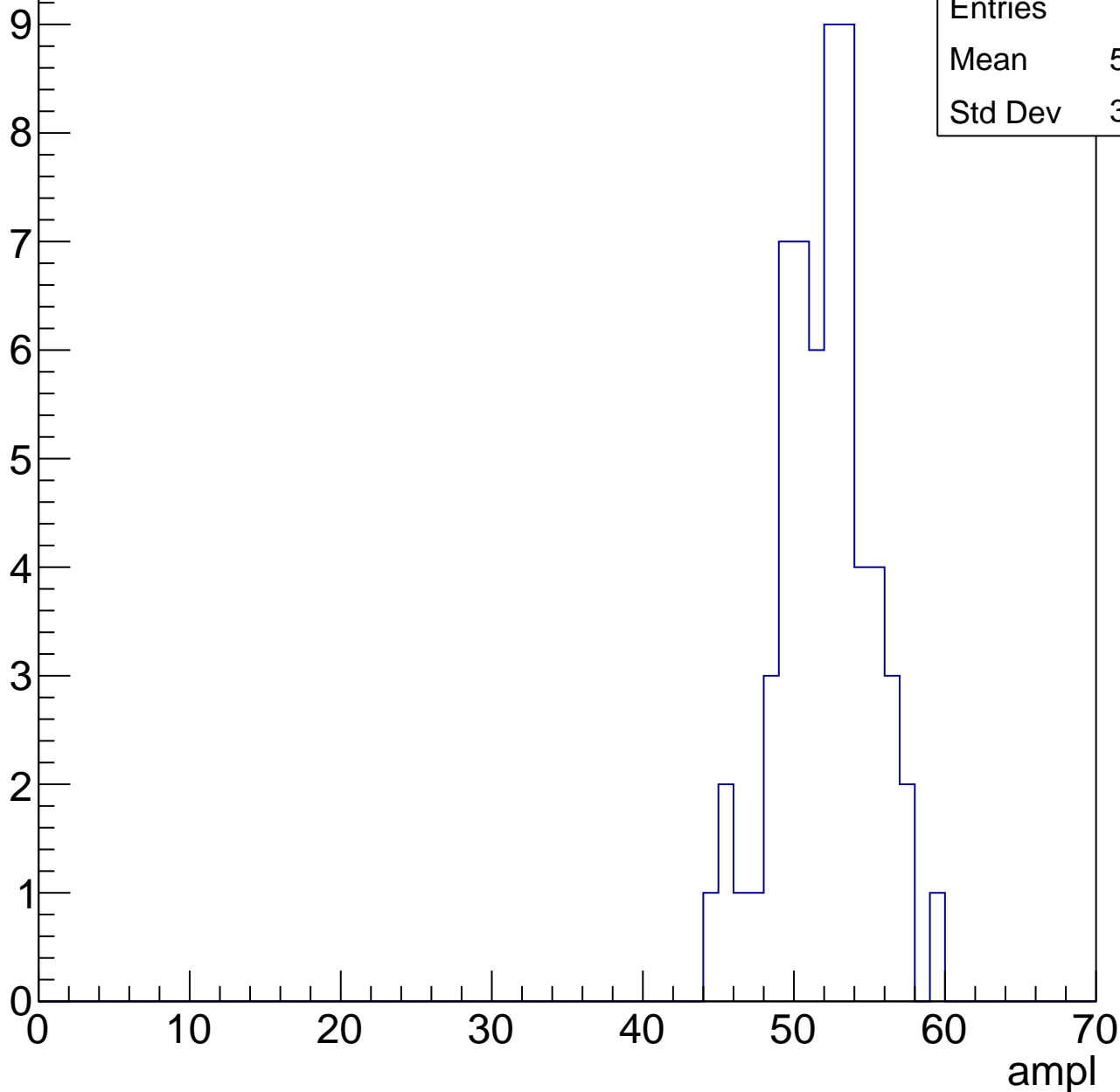
**Gaus Width: 4.2896**



# B1L101S, U22-ch3, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

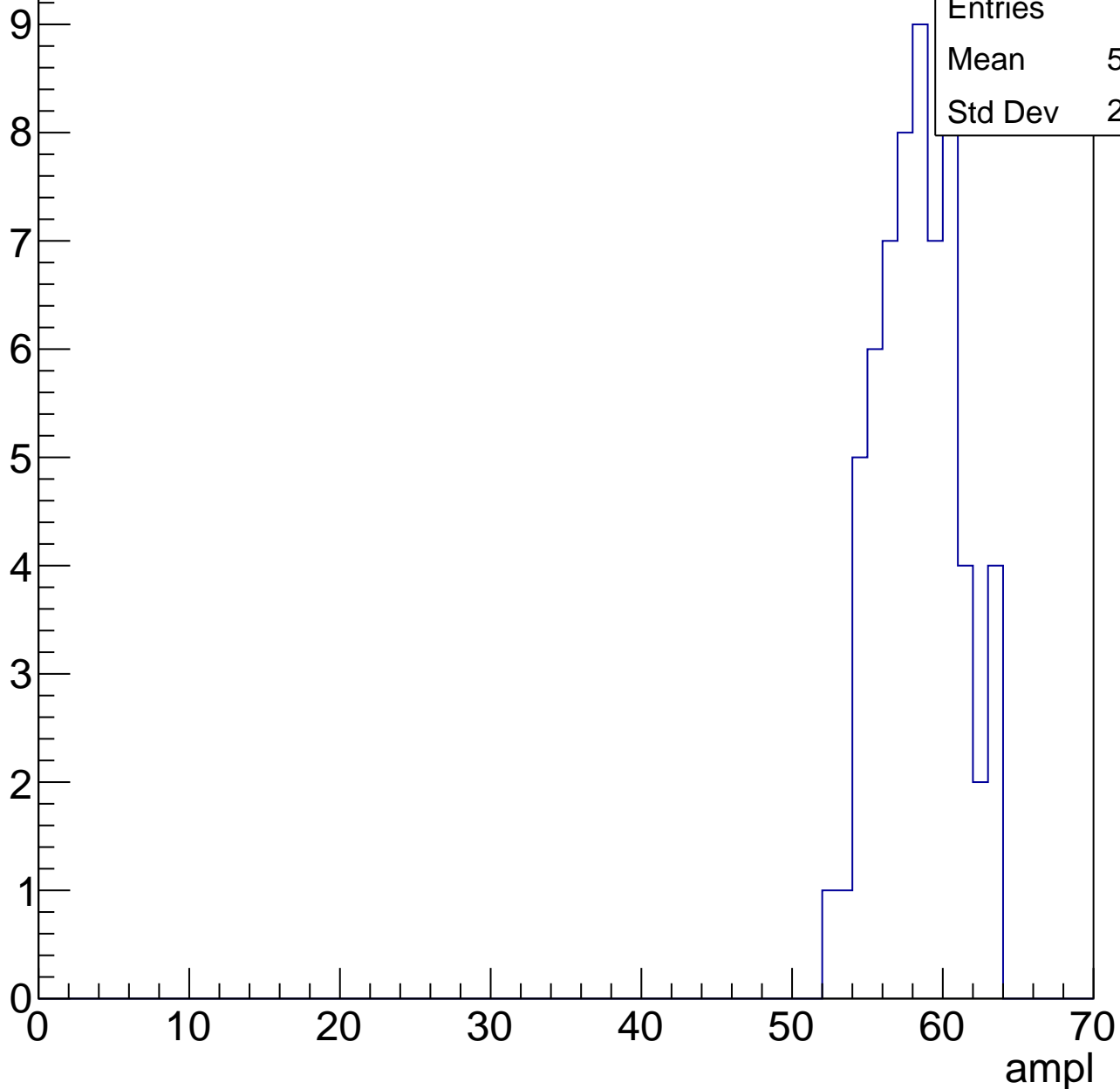
Entry



# B1L101S, U22-ch3, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

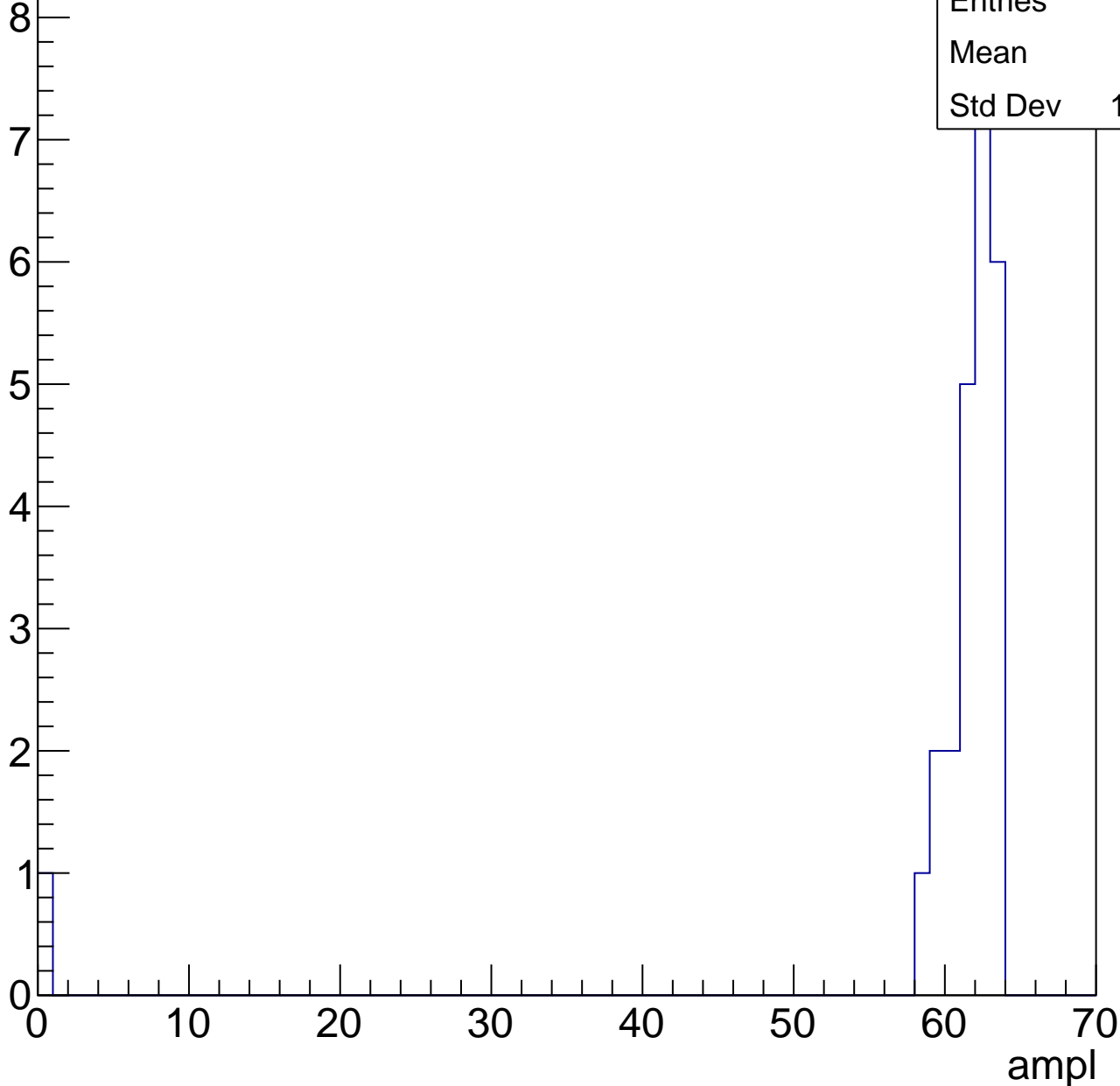


# B1L101S, U22-ch3, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

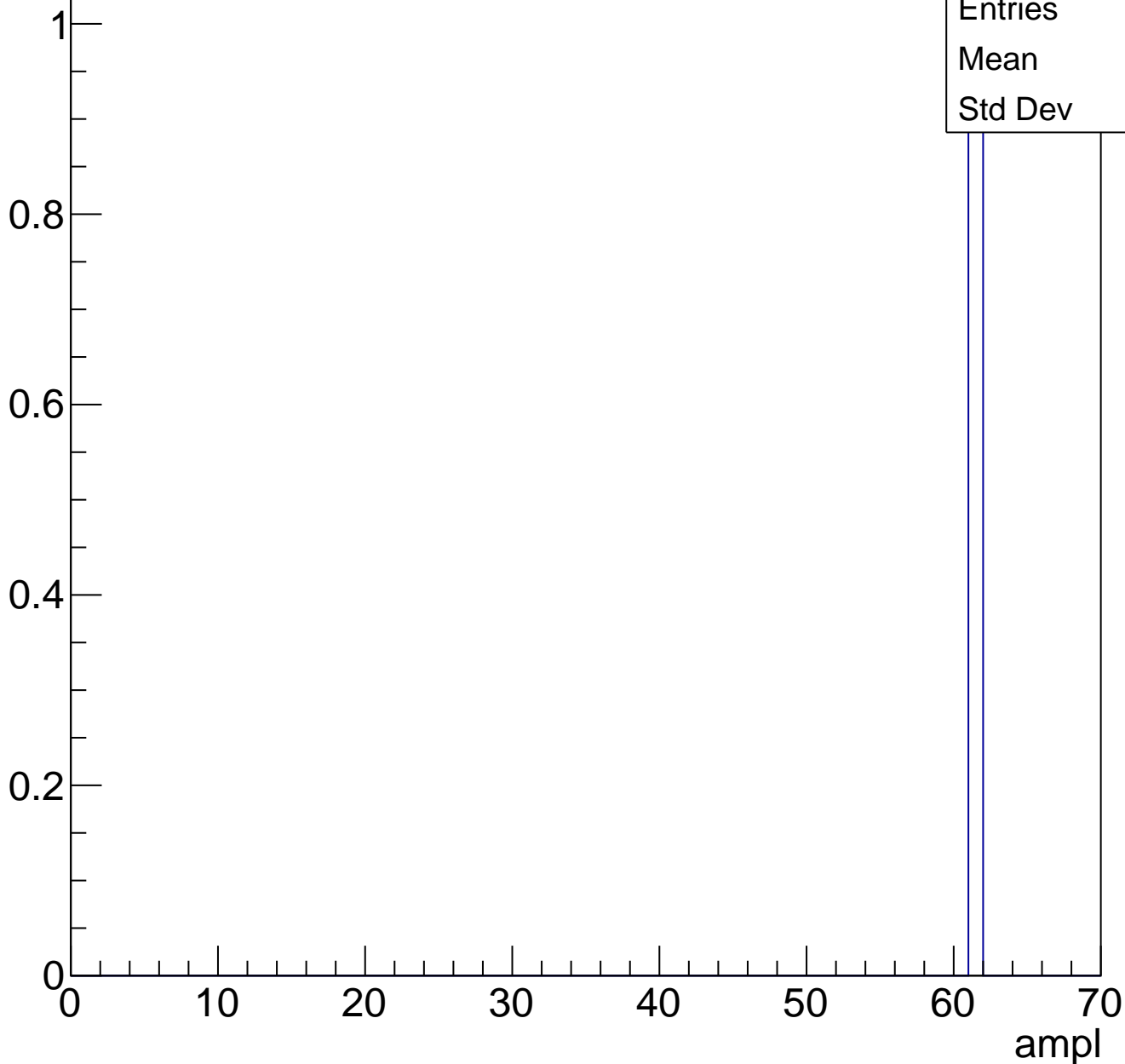
Entries	25
Mean	59
Std Dev	12.12



# B1L101S, U22-ch3, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U22-ch3, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L101S, U22-ch4, adc0

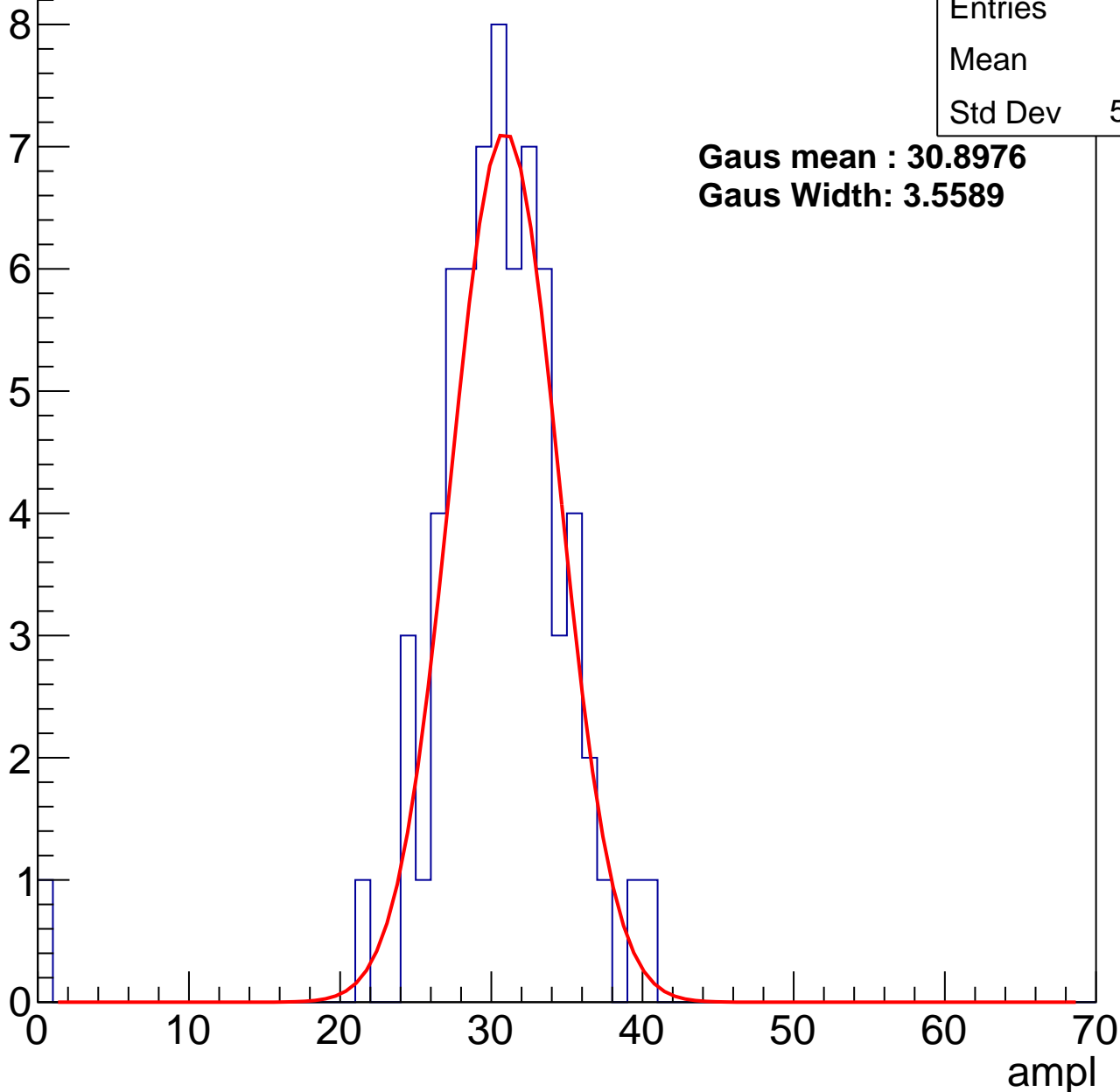
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	29.9
Std Dev	5.145

**Gaus mean : 30.8976**

**Gaus Width: 3.5589**



# B1L101S, U22-ch4, adc1

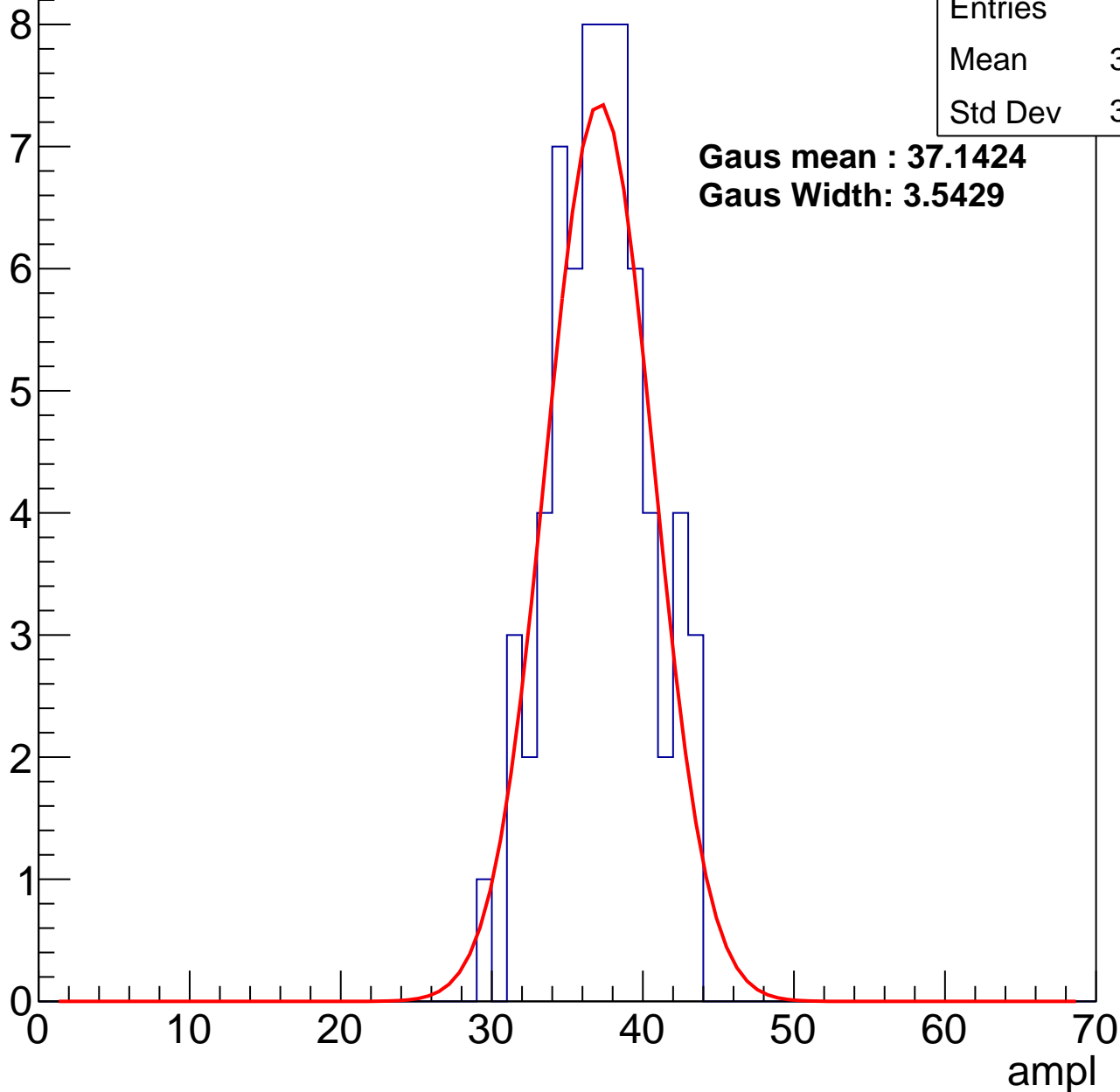
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	66
Mean	36.77
Std Dev	3.223

**Gaus mean : 37.1424**

**Gaus Width: 3.5429**



# B1L101S, U22-ch4, adc2

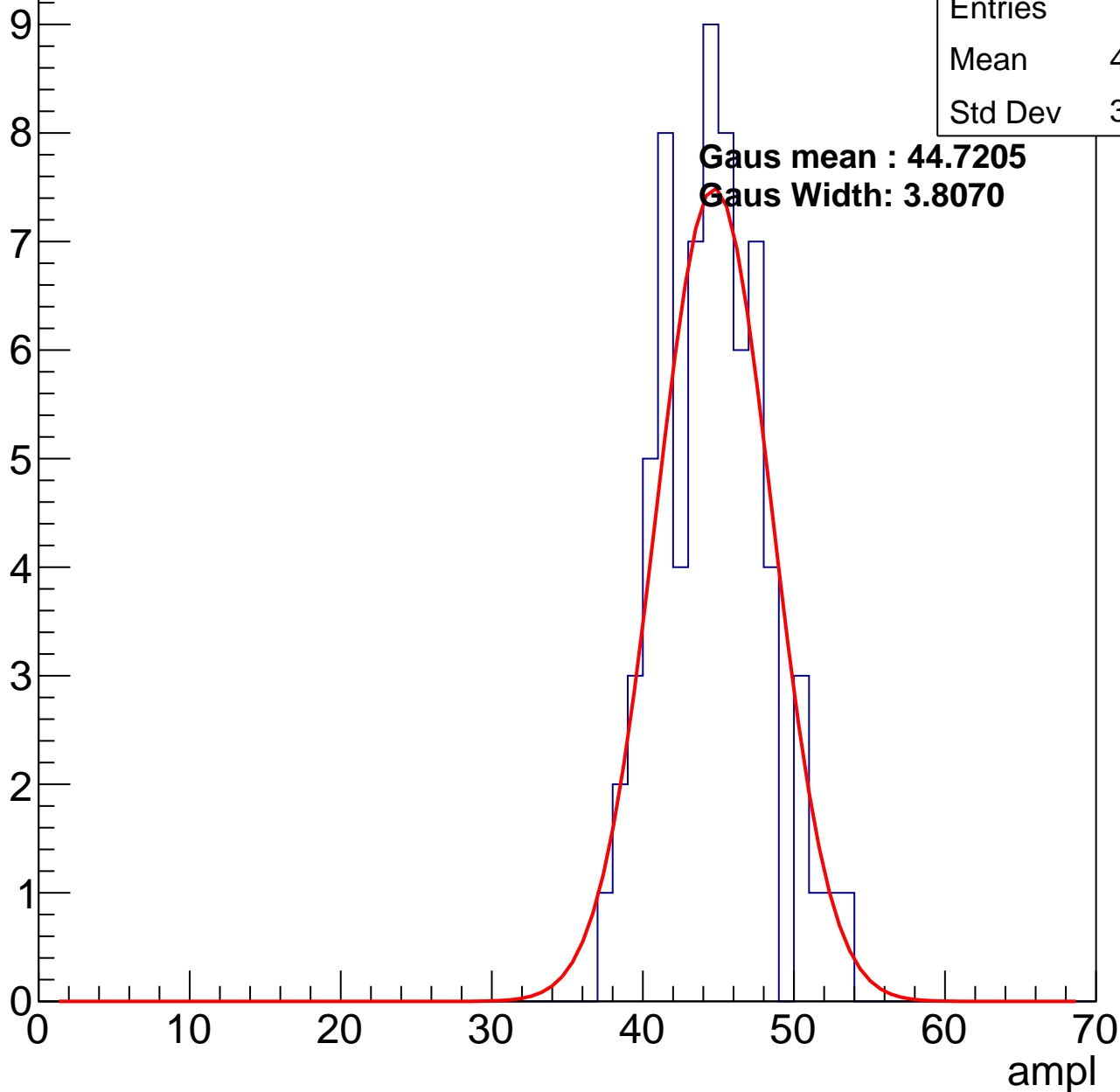
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	44.09
Std Dev	3.447

**Gaus mean : 44.7205**

**Gaus Width: 3.8070**

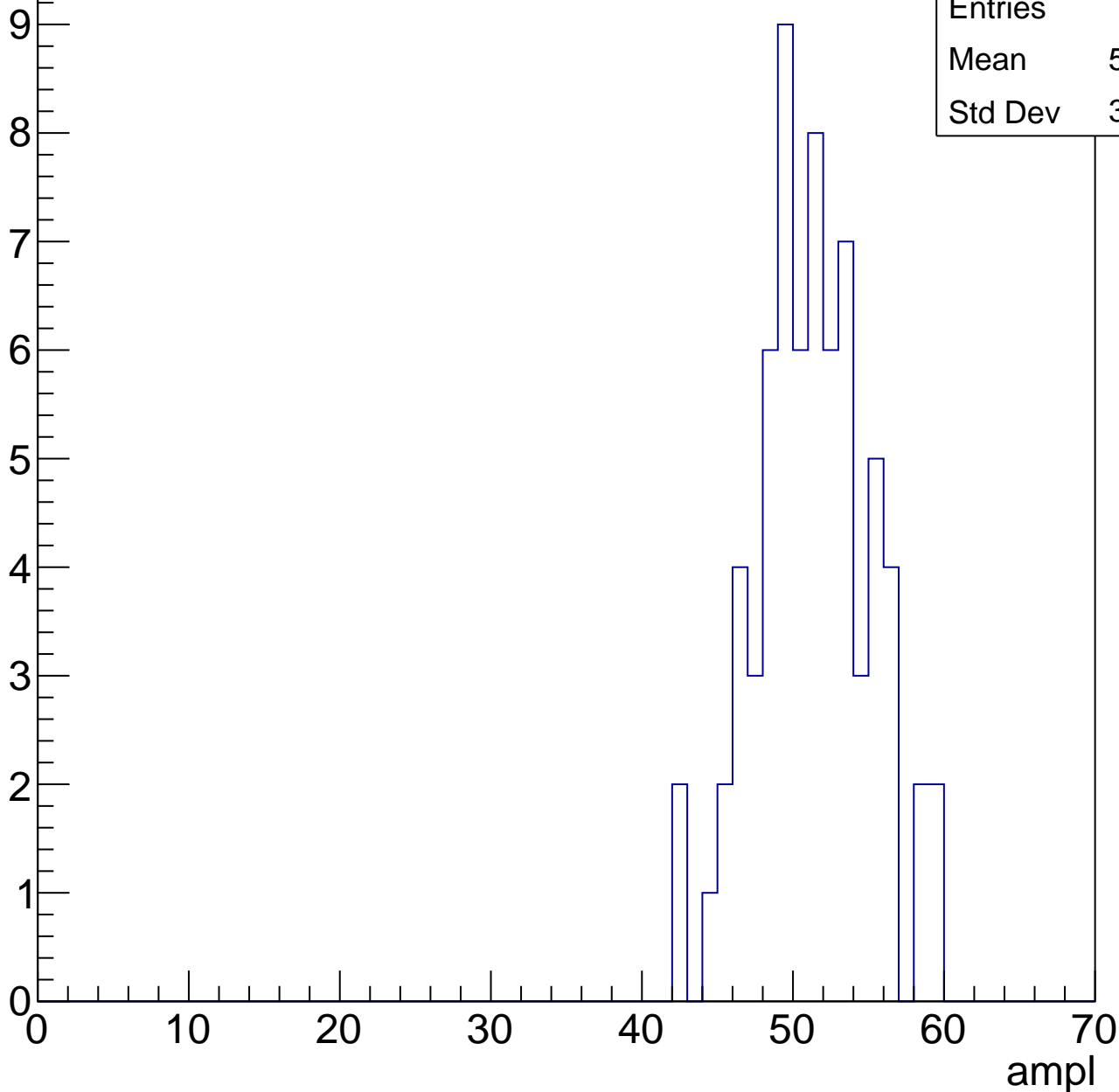


# B1L101S, U22-ch4, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

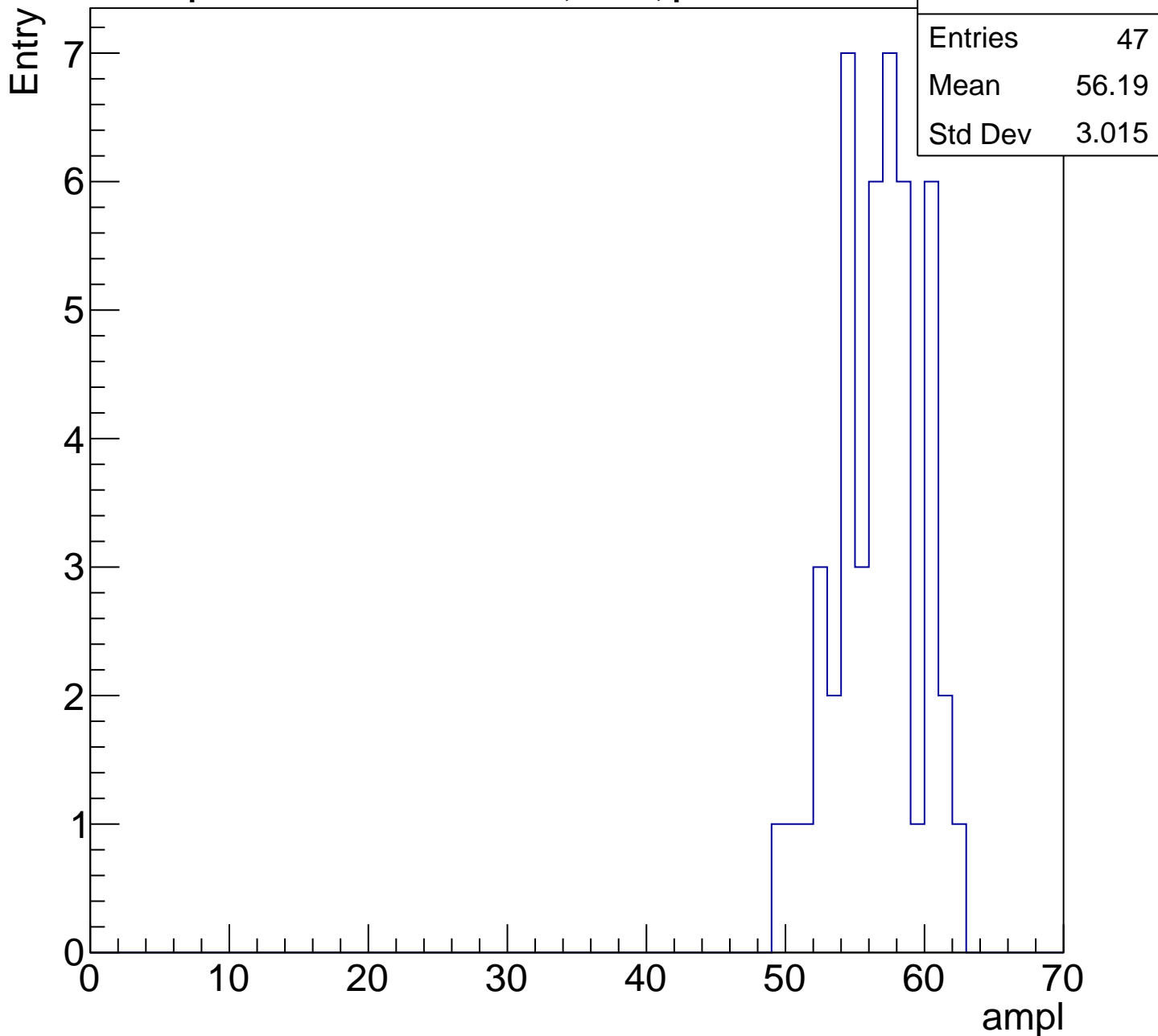
Entry

Entries	70
Mean	50.83
Std Dev	3.764



# B1L101S, U22-ch4, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

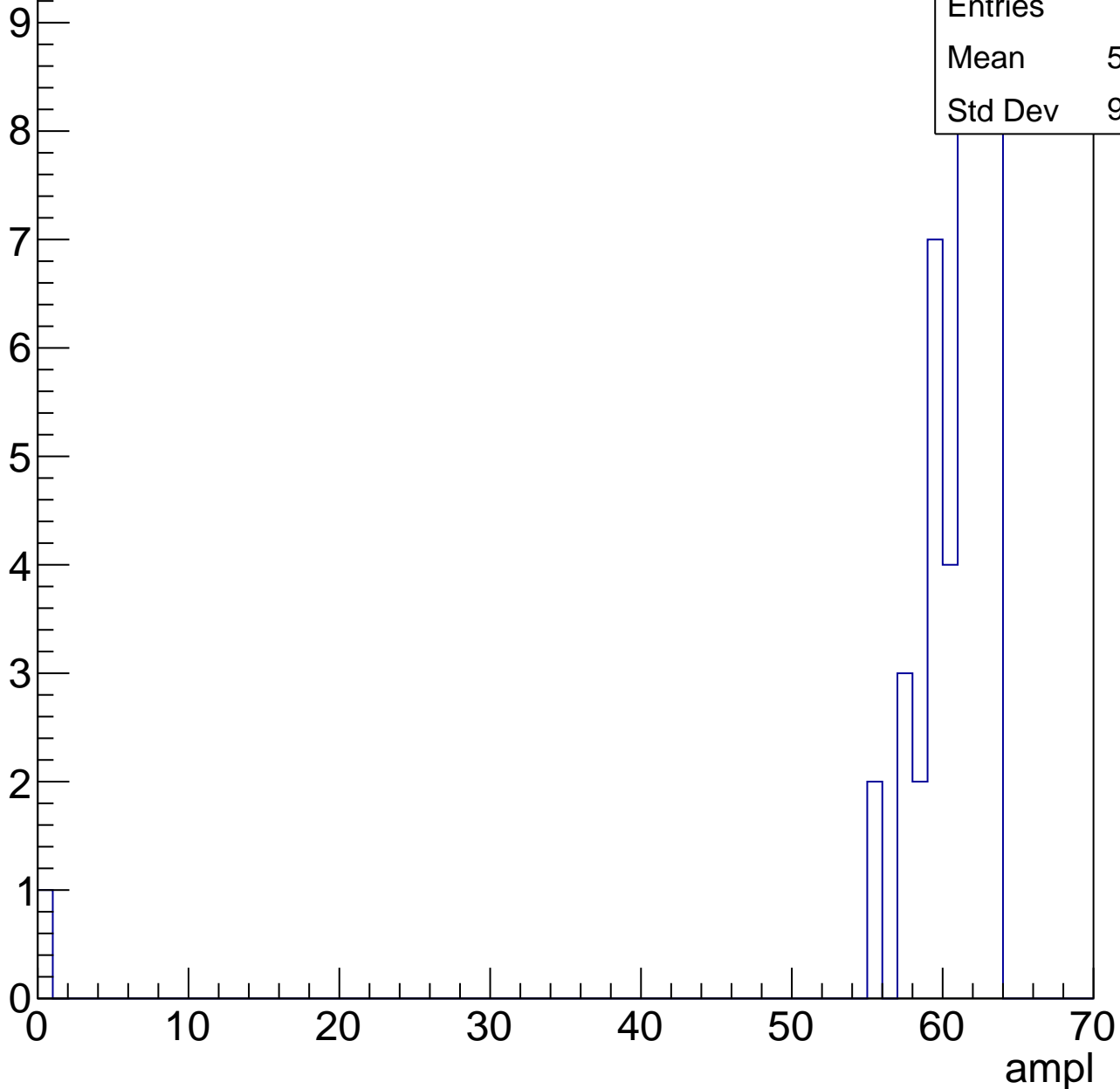


# B1L101S, U22-ch4, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	45
Mean	59.13
Std Dev	9.159



# B1L101S, U22-ch4, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U22-ch4, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L101S, U22-ch5, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	87
Mean	31.31
Std Dev	5.059

**Gaus mean : 32.5332**

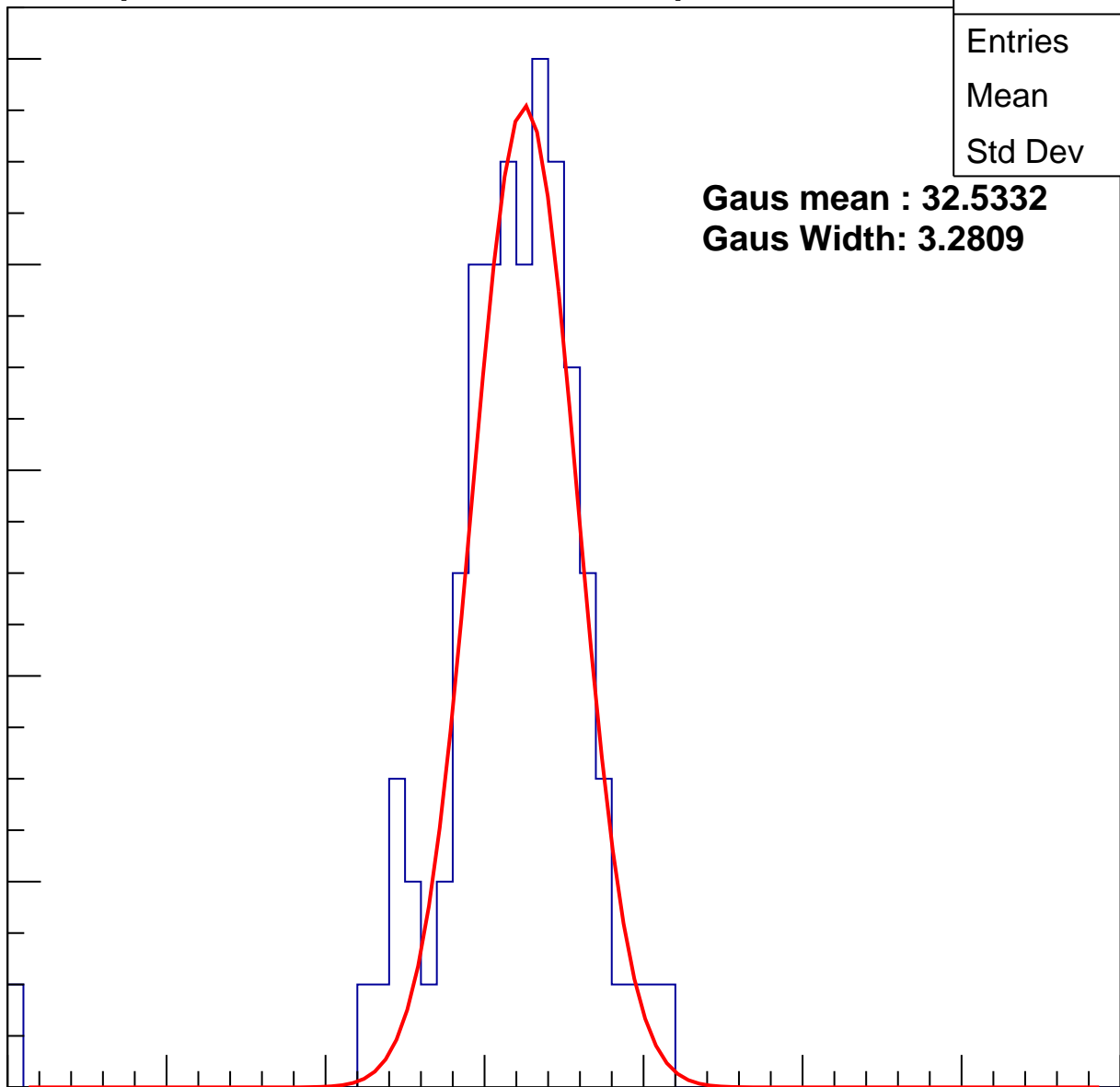
**Gaus Width: 3.2809**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U22-ch5, adc1

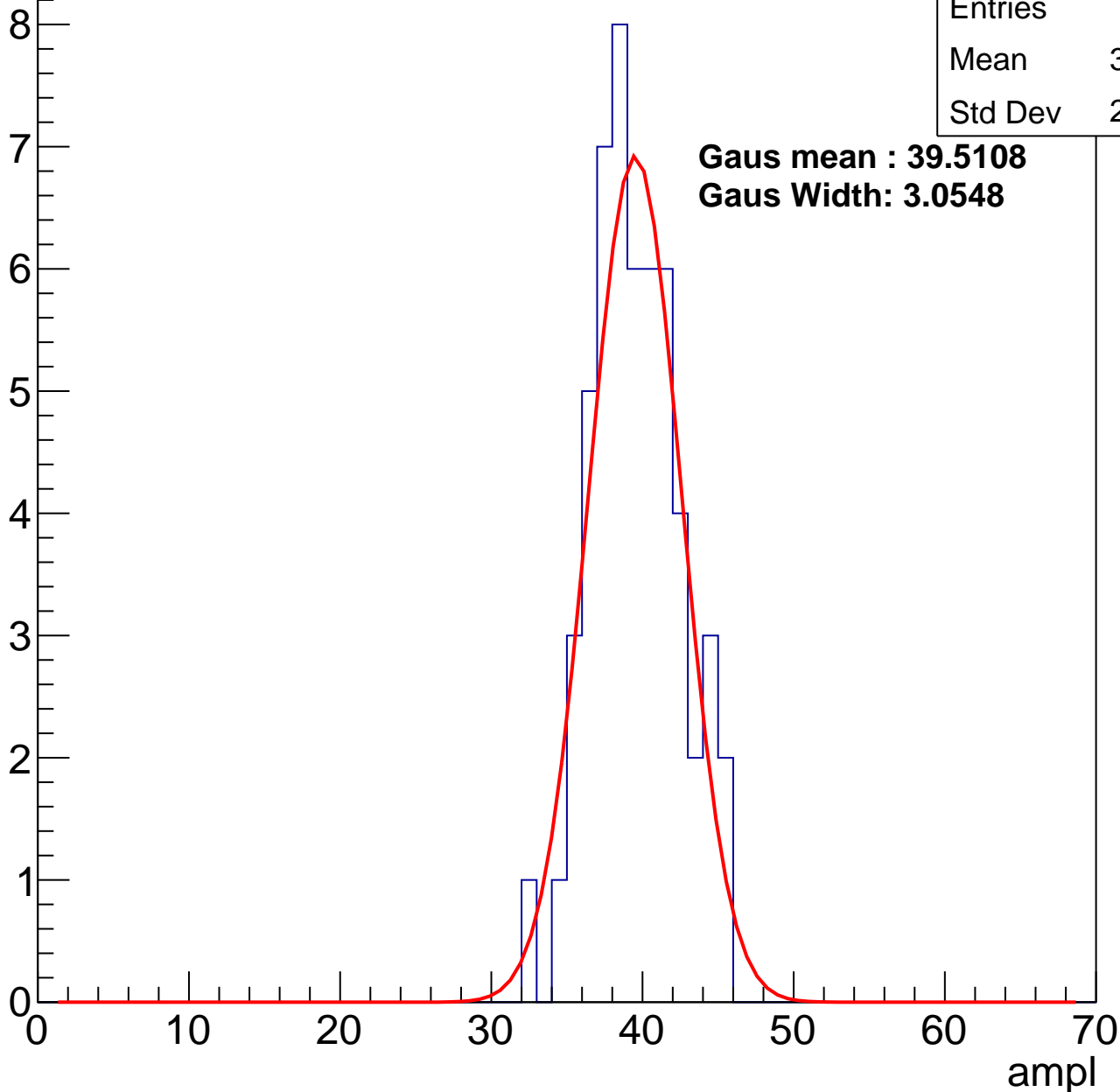
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	54
Mean	39.07
Std Dev	2.879

**Gaus mean : 39.5108**

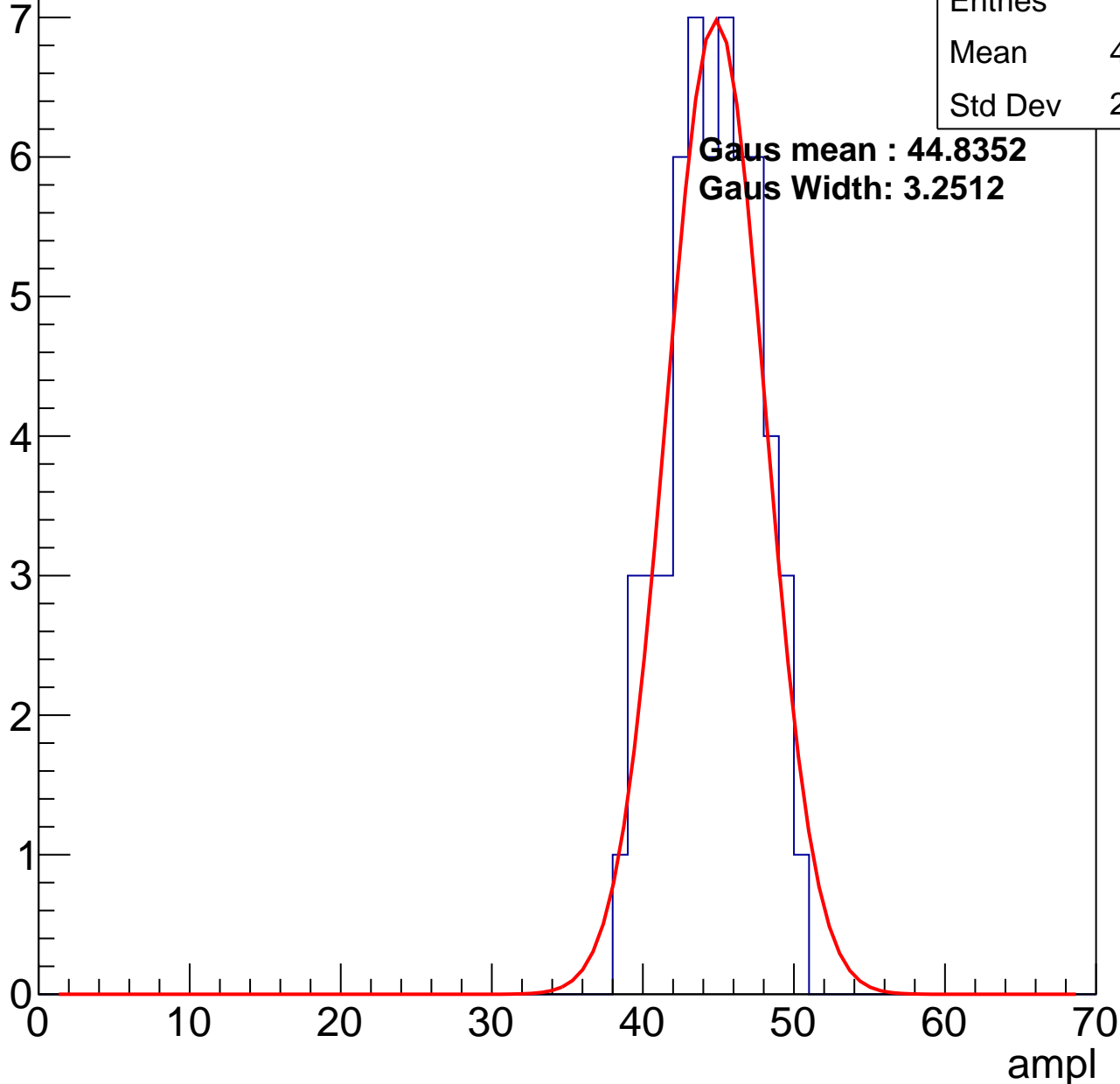
**Gaus Width: 3.0548**



# B1L101S, U22-ch5, adc2

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	56
Mean	44.23
Std Dev	2.909

# B1L101S, U22-ch5, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

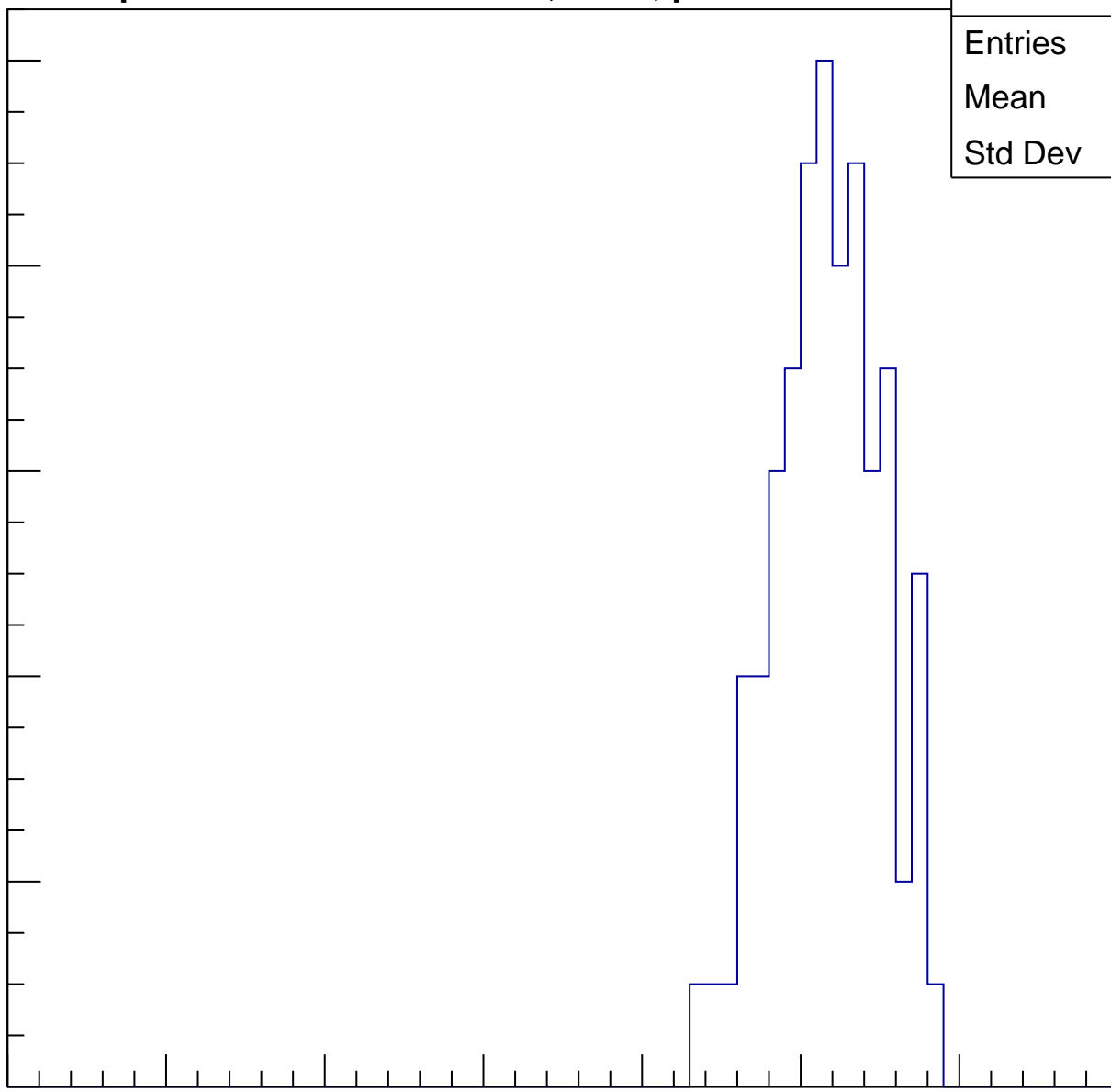
Entries	81
Mean	51.26
Std Dev	3.31

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

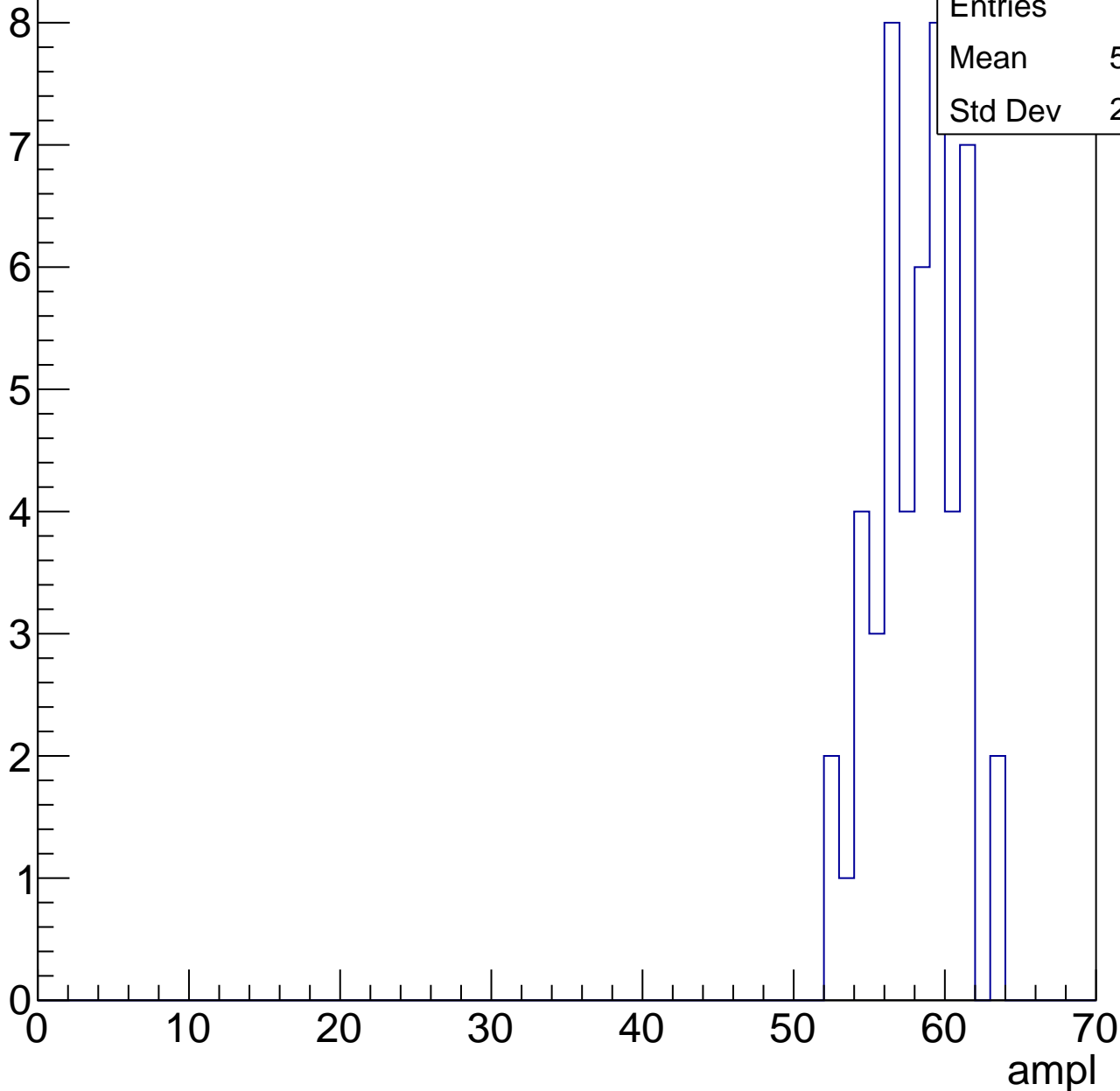


# B1L101S, U22-ch5, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	49
Mean	57.69
Std Dev	2.697

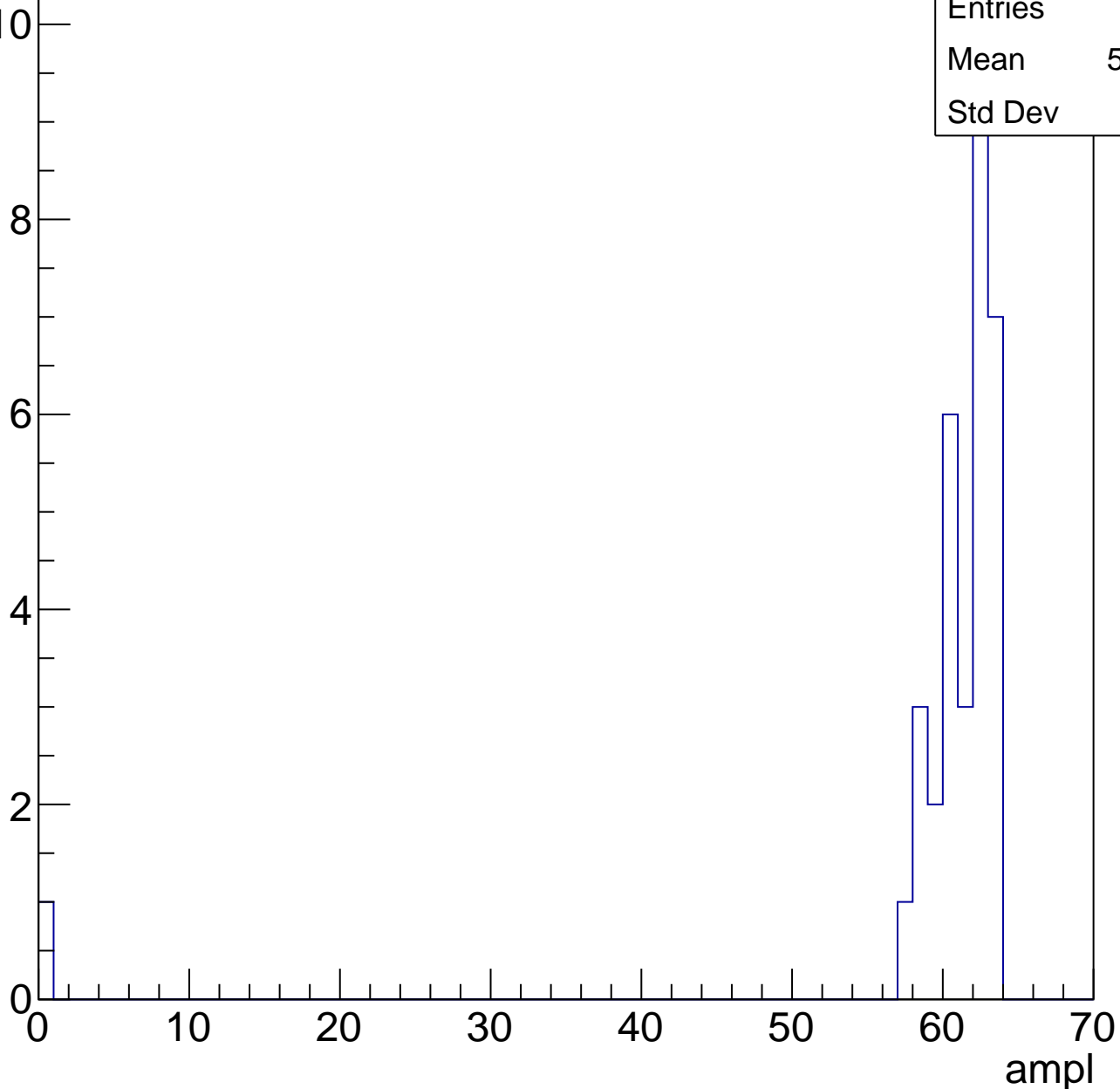


# B1L101S, U22-ch5, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	33
Mean	59.18
Std Dev	10.6



# B1L101S, U22-ch5, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U22-ch5, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U22-ch6, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	85
Mean	29.96
Std Dev	3.73

**Gaus mean : 29.8394**

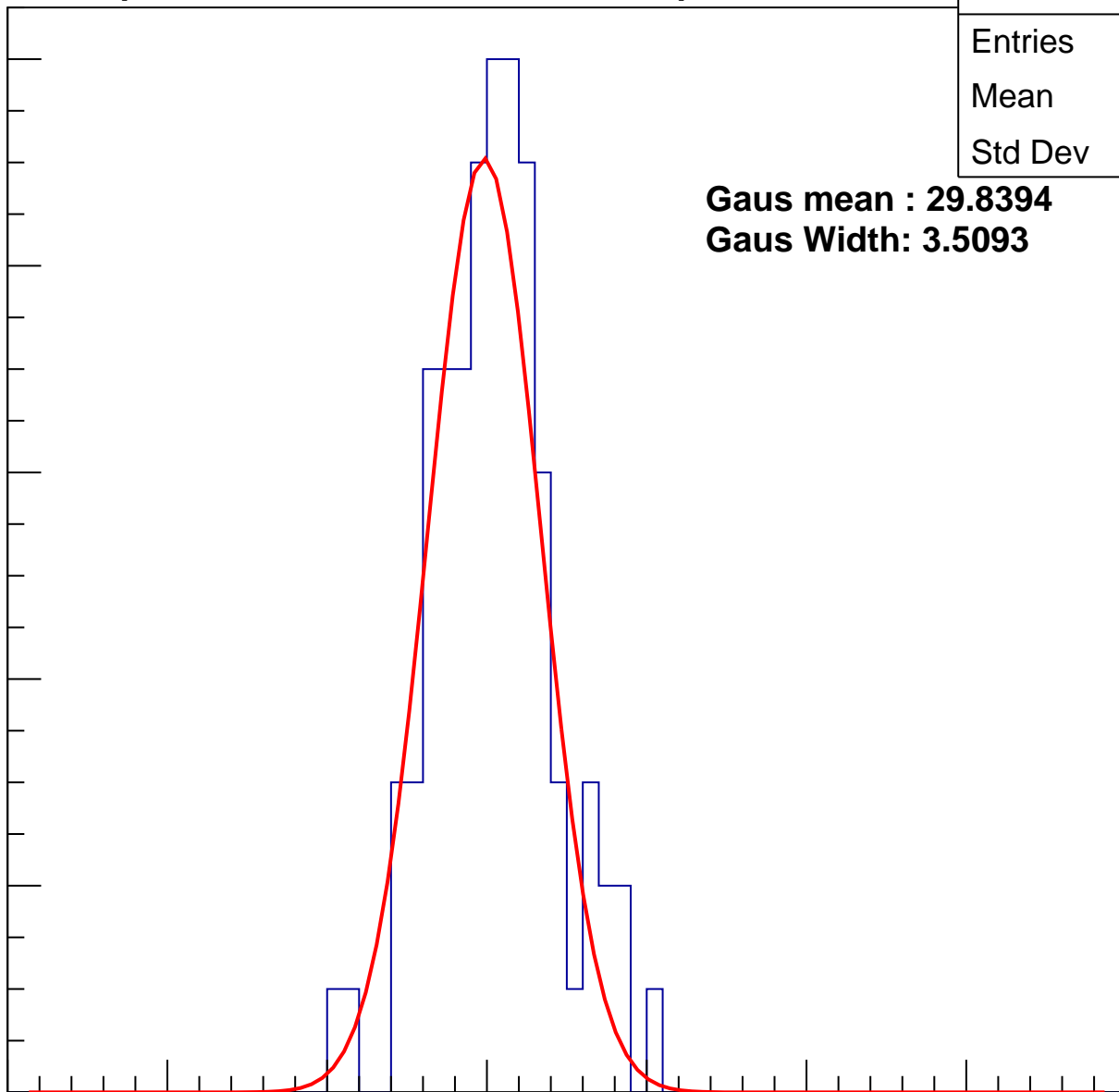
**Gaus Width: 3.5093**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B1L101S, U22-ch6, adc1

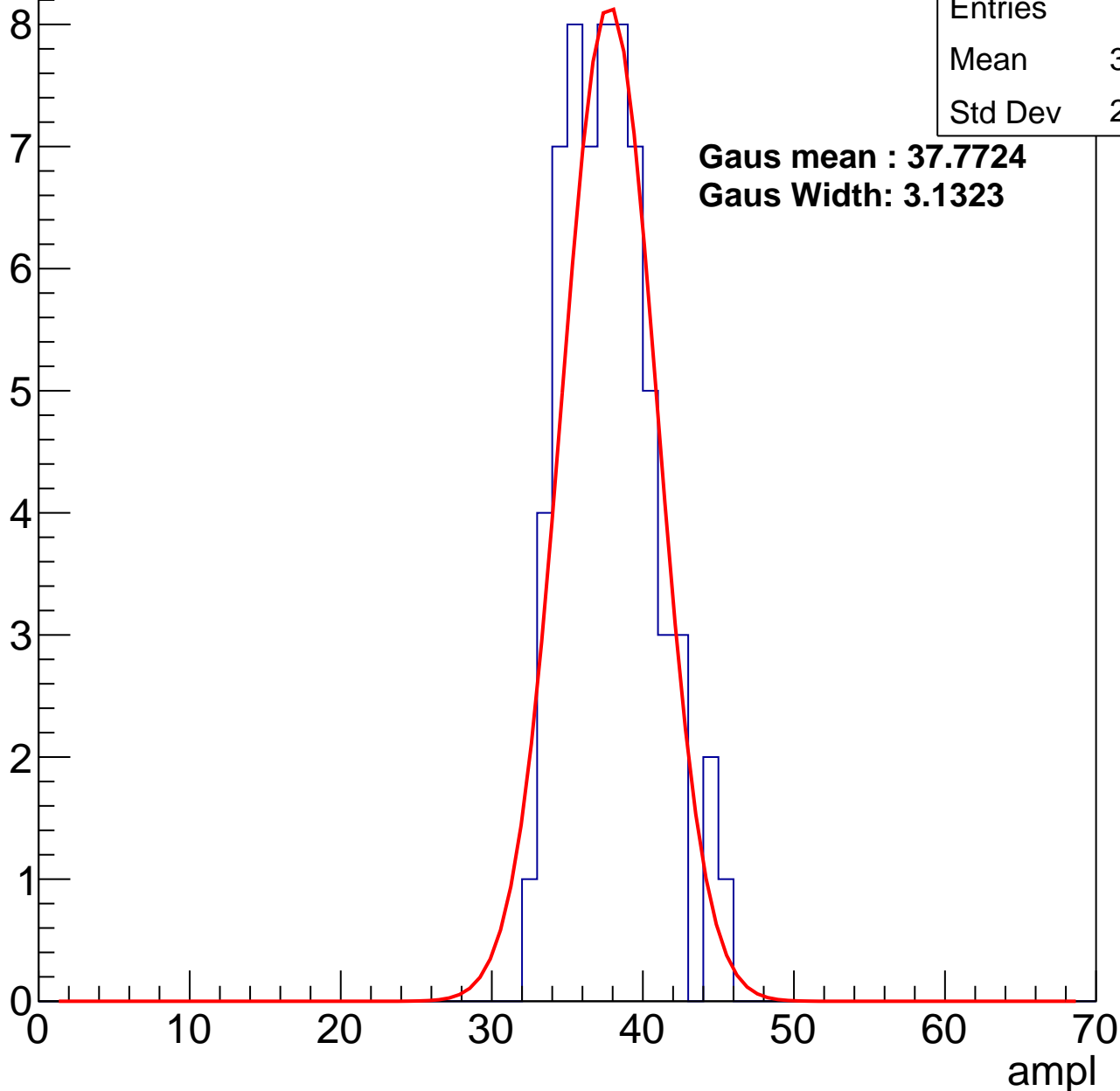
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	37.33
Std Dev	2.932

**Gaus mean : 37.7724**

**Gaus Width: 3.1323**



# B1L101S, U22-ch6, adc2

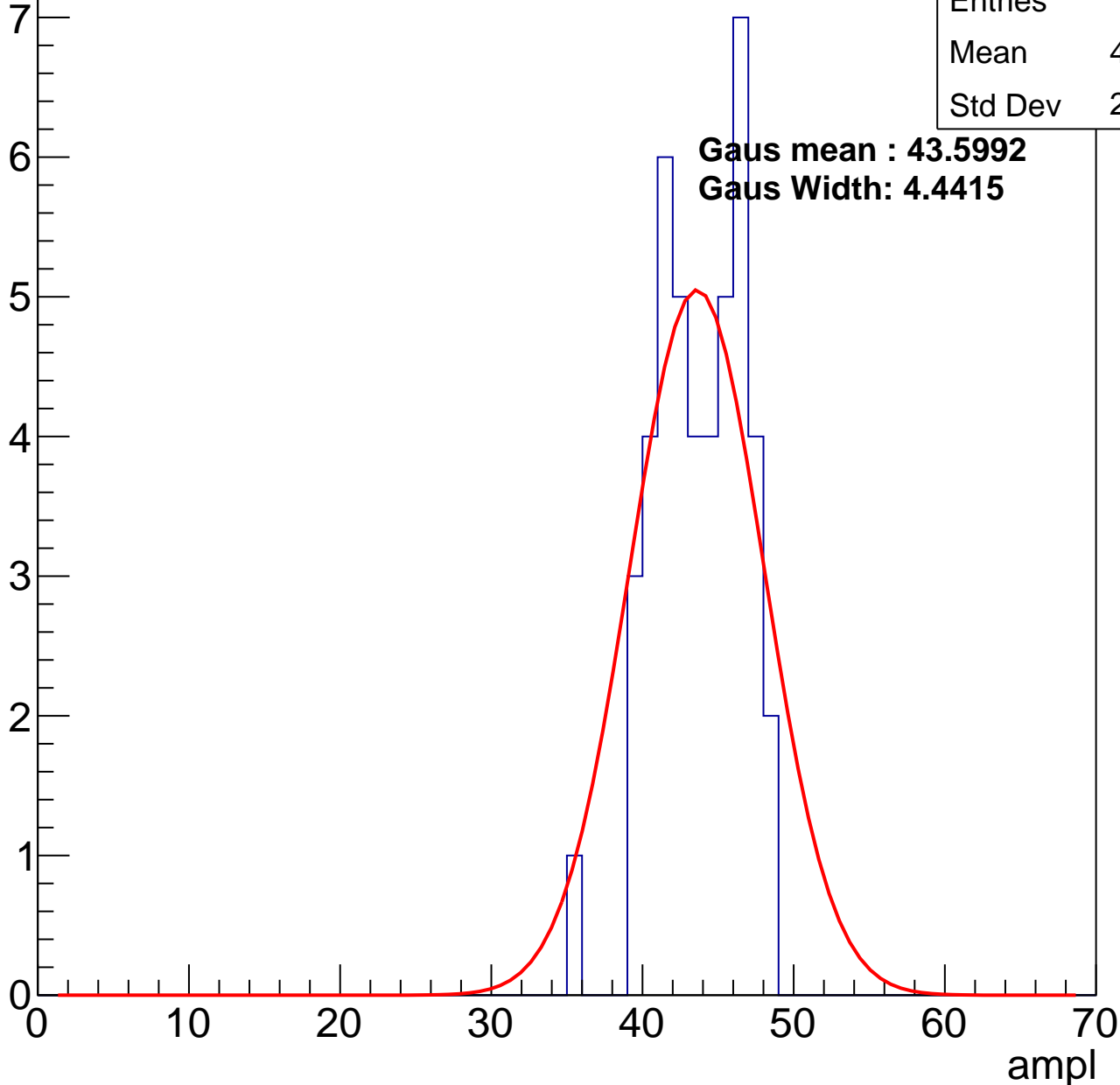
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	45
Mean	43.27
Std Dev	2.886

**Gaus mean : 43.5992**

**Gaus Width: 4.4415**



# B1L101S, U22-ch6, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	86
Mean	49.4
Std Dev	3.986

Entry

10

8

6

4

2

0

0

10

20

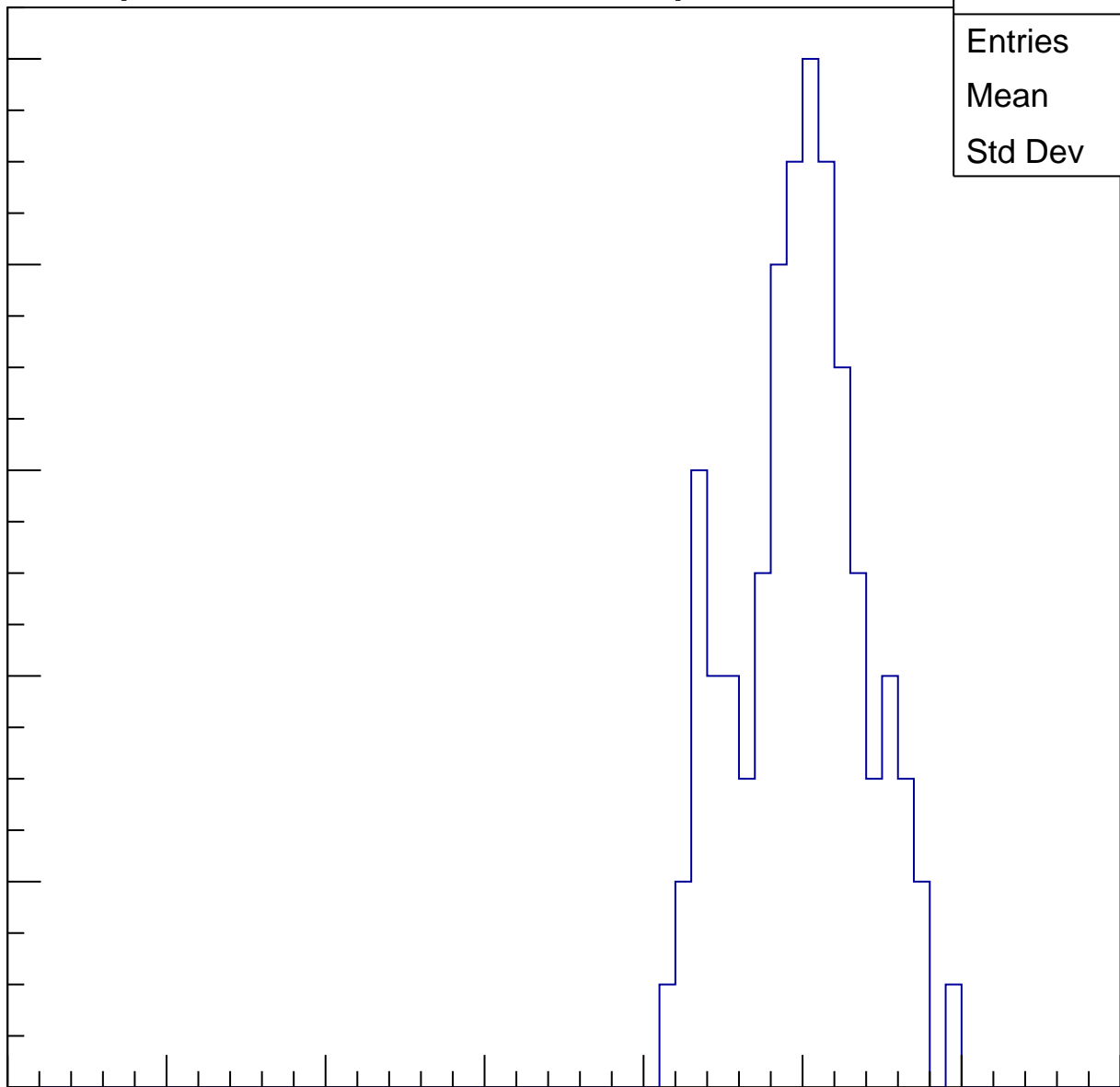
30

40

50

60

ampl

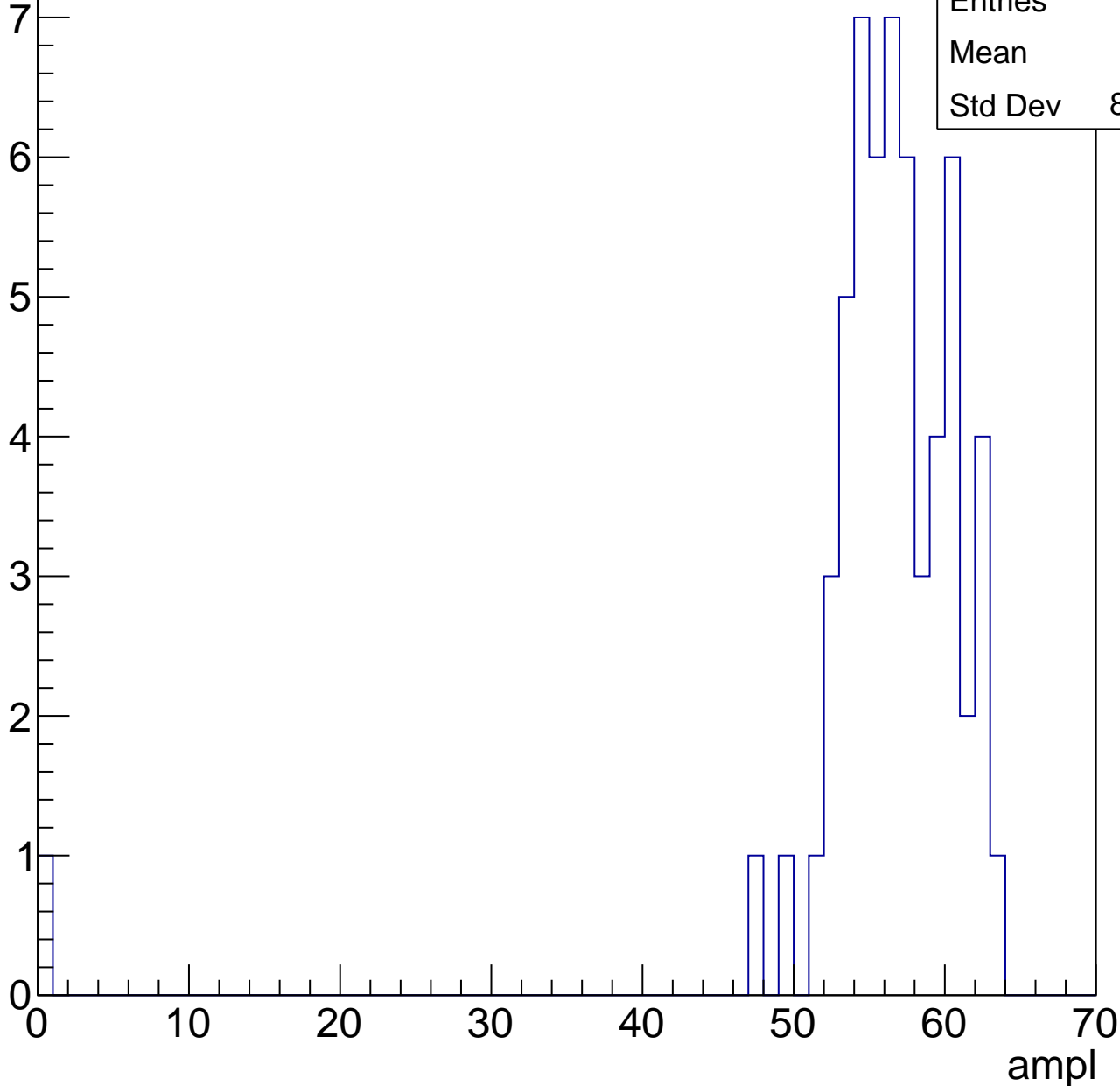


# B1L101S, U22-ch6, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	58
Mean	55.4
Std Dev	8.083



# B1L101S, U22-ch6, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

7

6

5

4

3

2

1

0

Entries	36
Mean	60.36
Std Dev	1.946

0 10 20 30 40 50 60 70

ampl

# B1L101S, U22-ch6, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

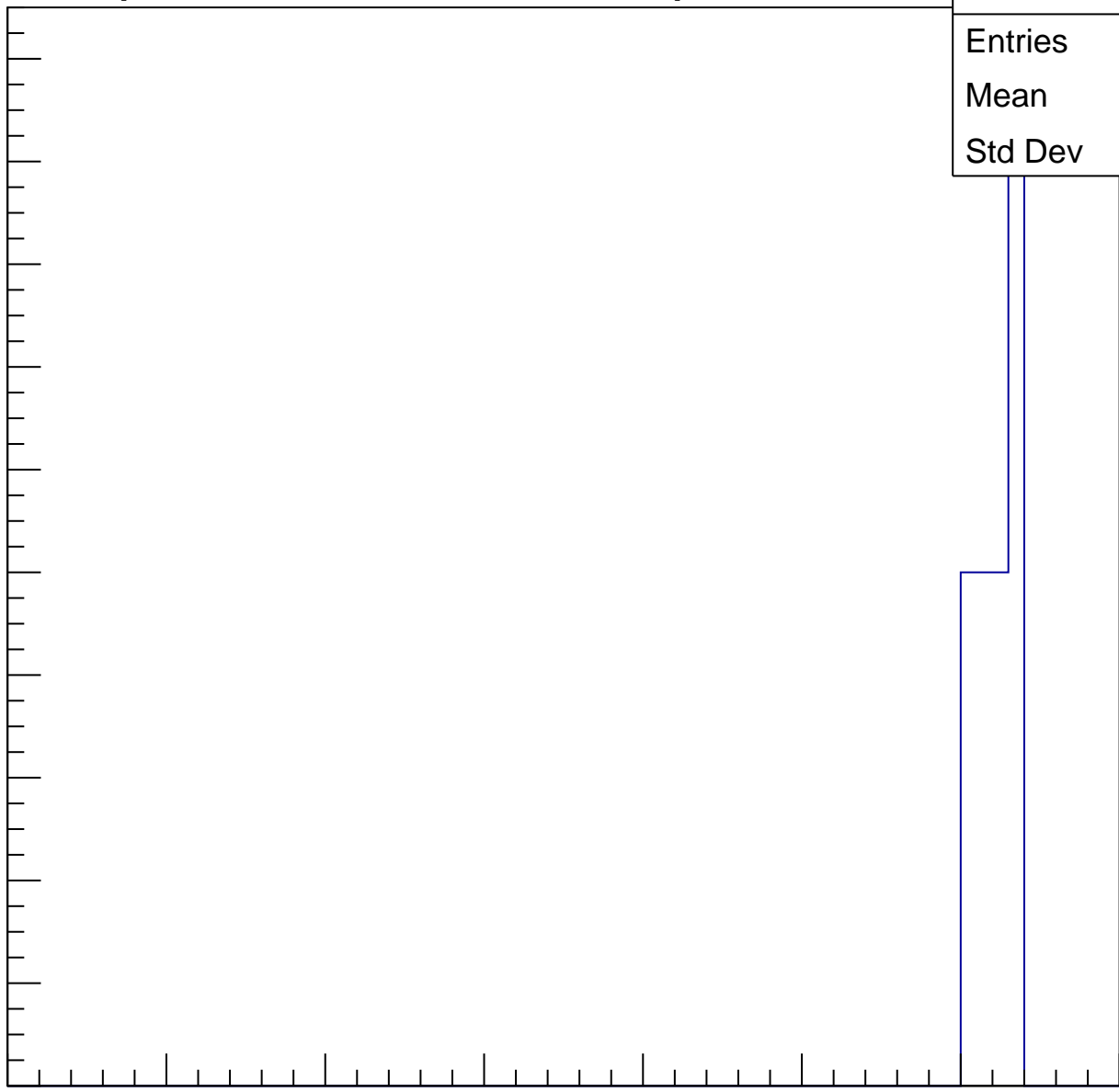
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	5
Mean	61.8
Std Dev	1.166

ampl

0 10 20 30 40 50 60 70





# B1L101S, U22-ch6, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L101S, U22-ch7, adc0

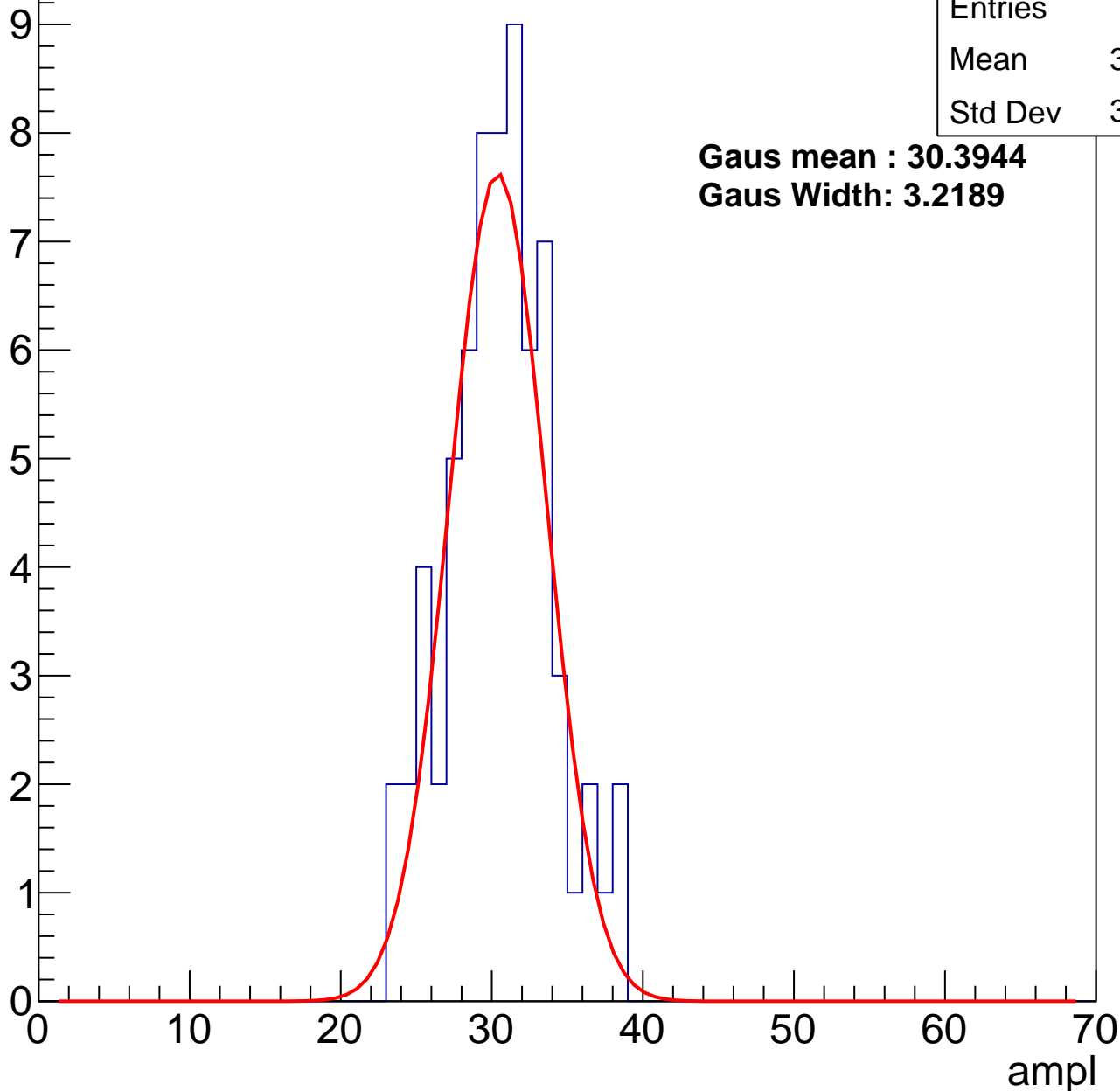
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	30.07
Std Dev	3.423

**Gaus mean : 30.3944**

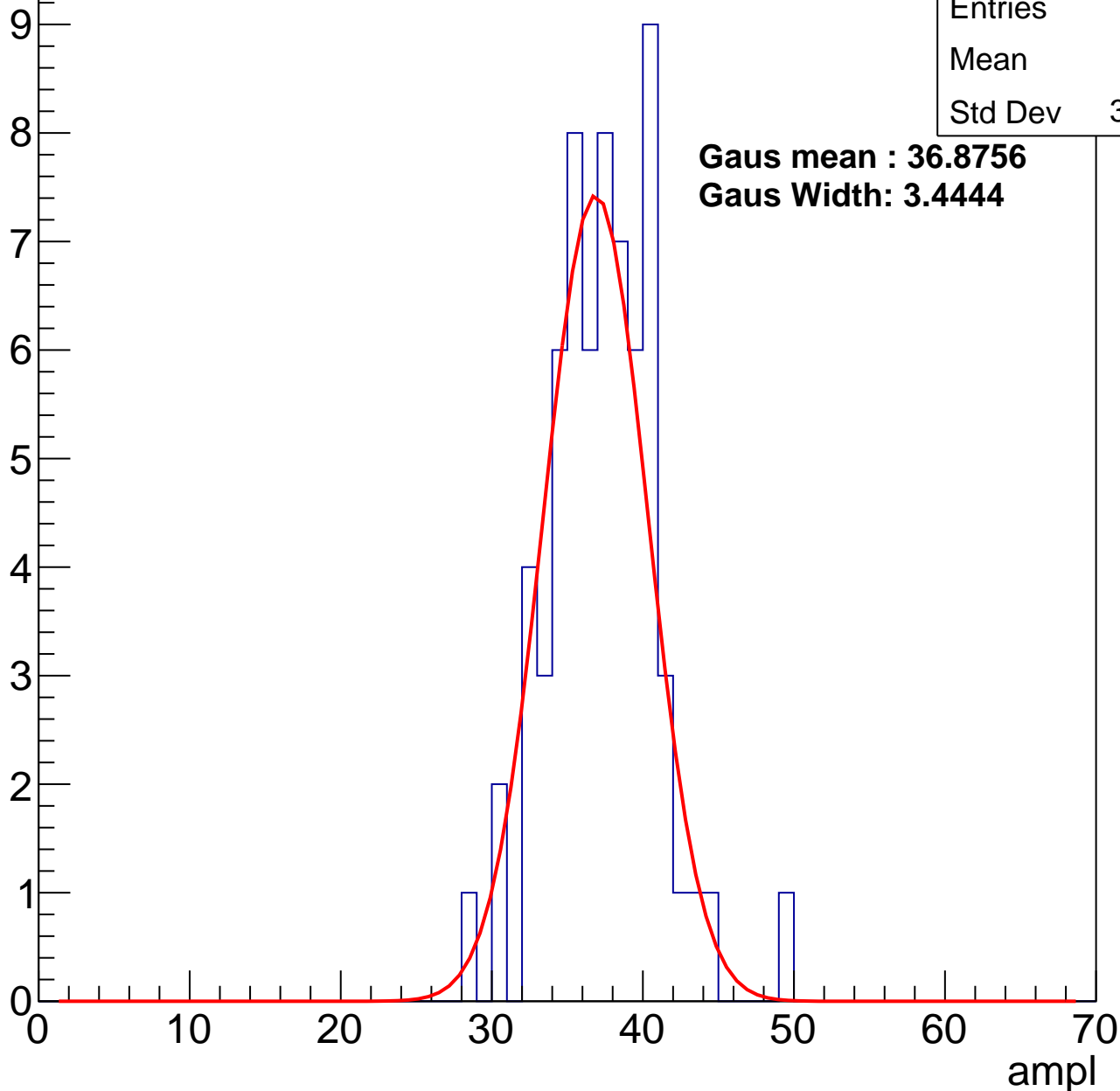
**Gaus Width: 3.2189**



# B1L101S, U22-ch7, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U22-ch7, adc2

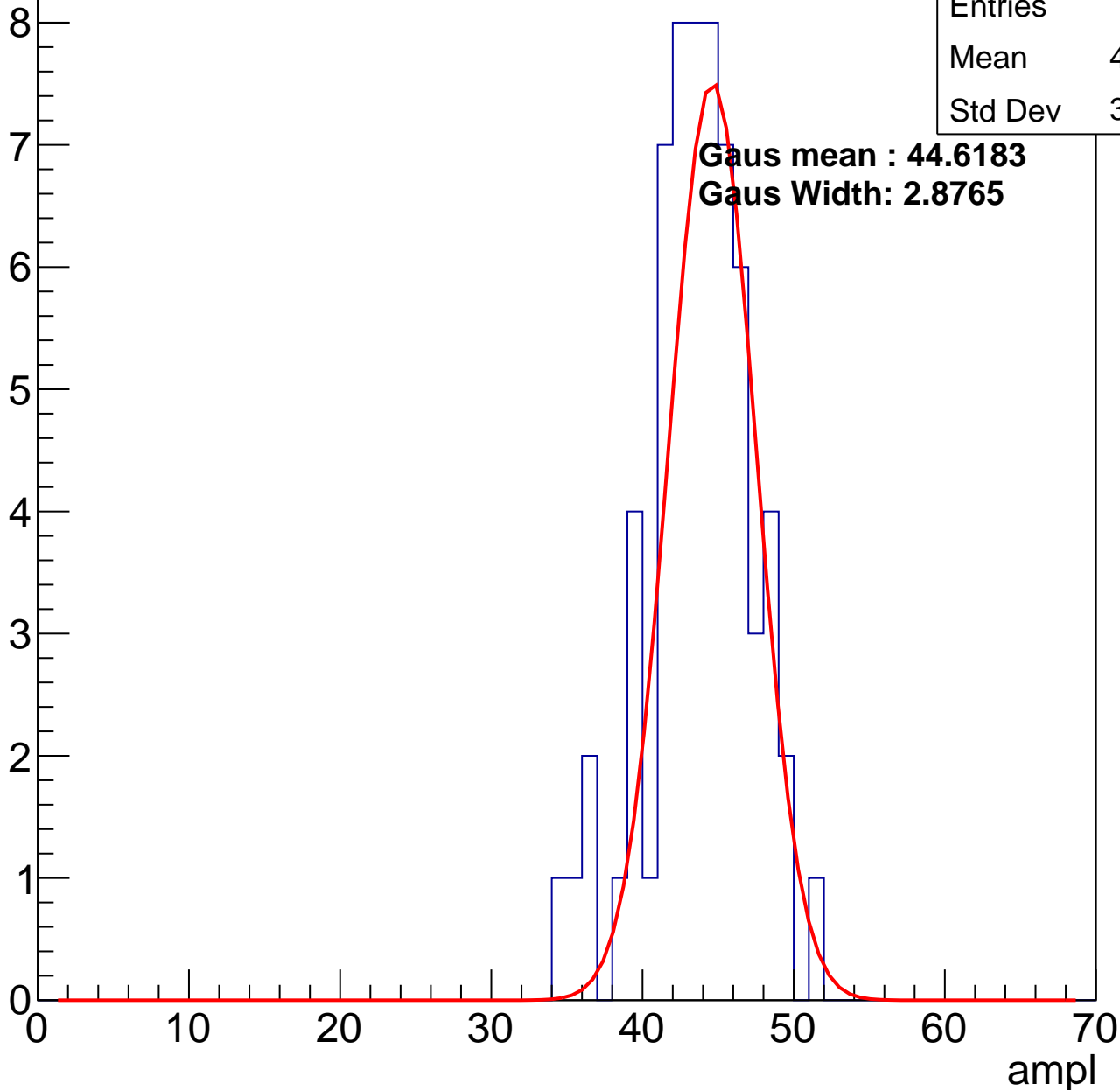
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	43.23
Std Dev	3.418

**Gaus mean : 44.6183**

**Gaus Width: 2.8765**

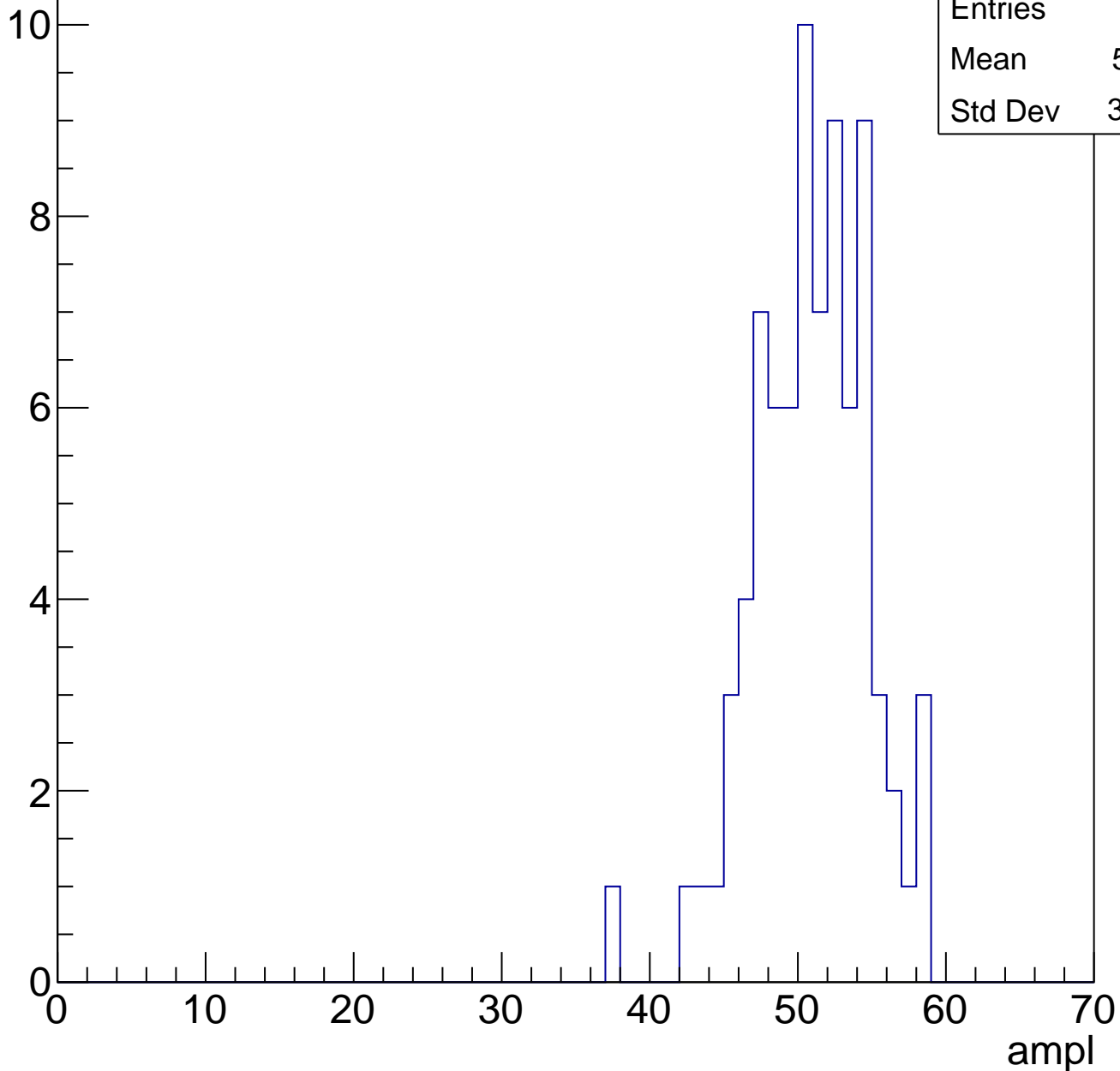


# B1L101S, U22-ch7, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

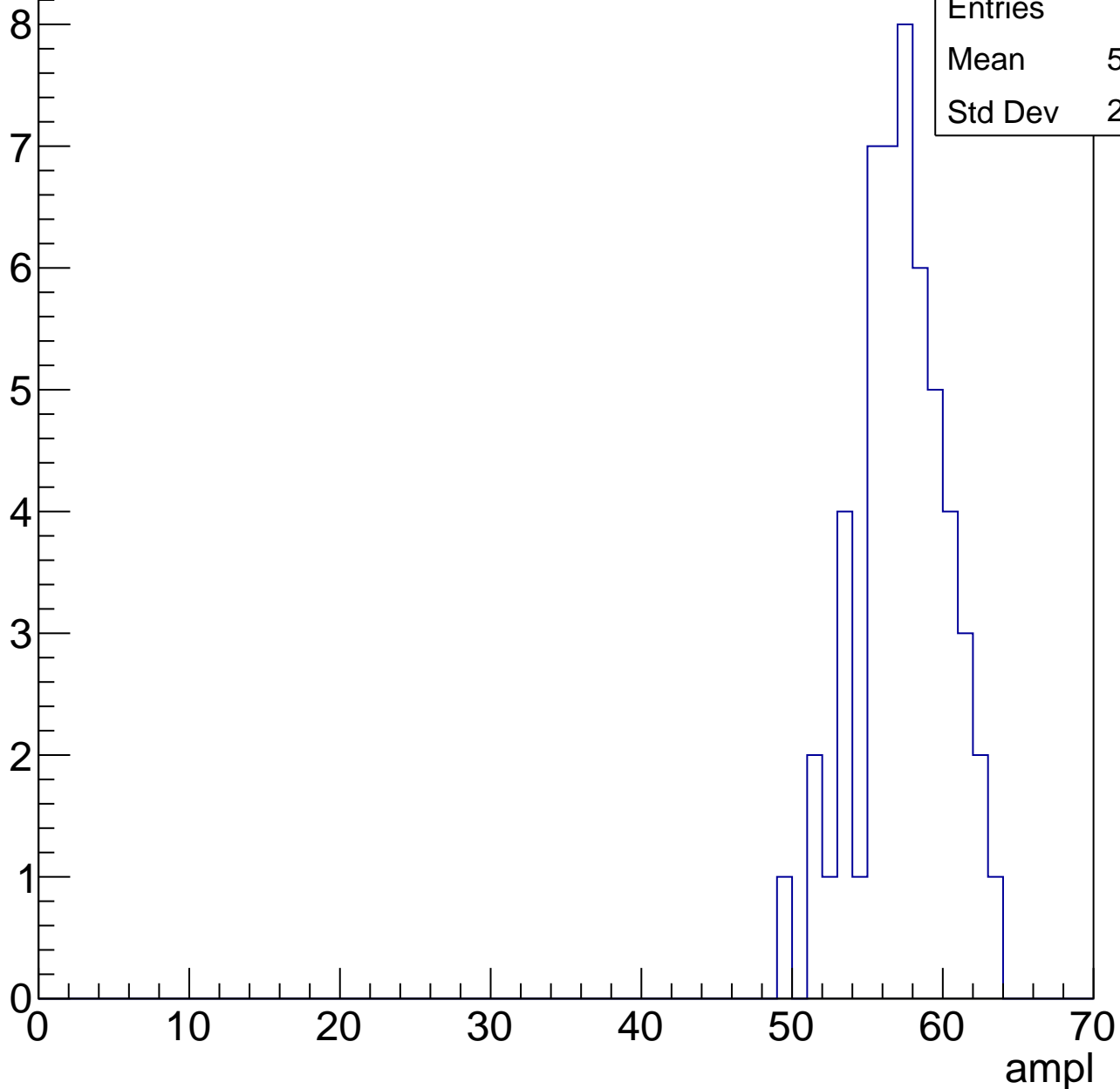
Entries	80
Mean	50.41
Std Dev	3.817



# B1L101S, U22-ch7, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

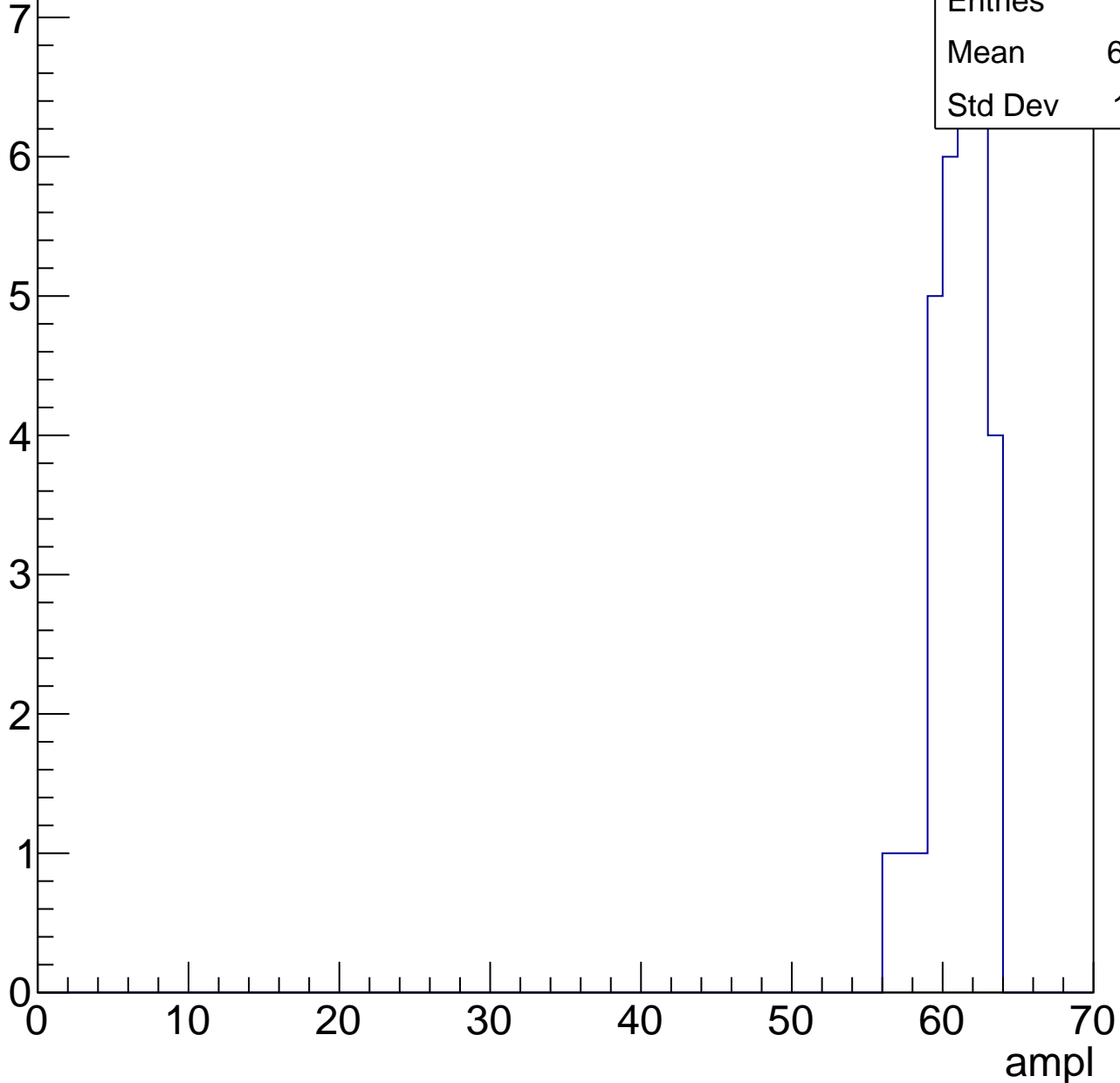


# B1L101S, U22-ch7, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	32
Mean	60.59
Std Dev	1.711

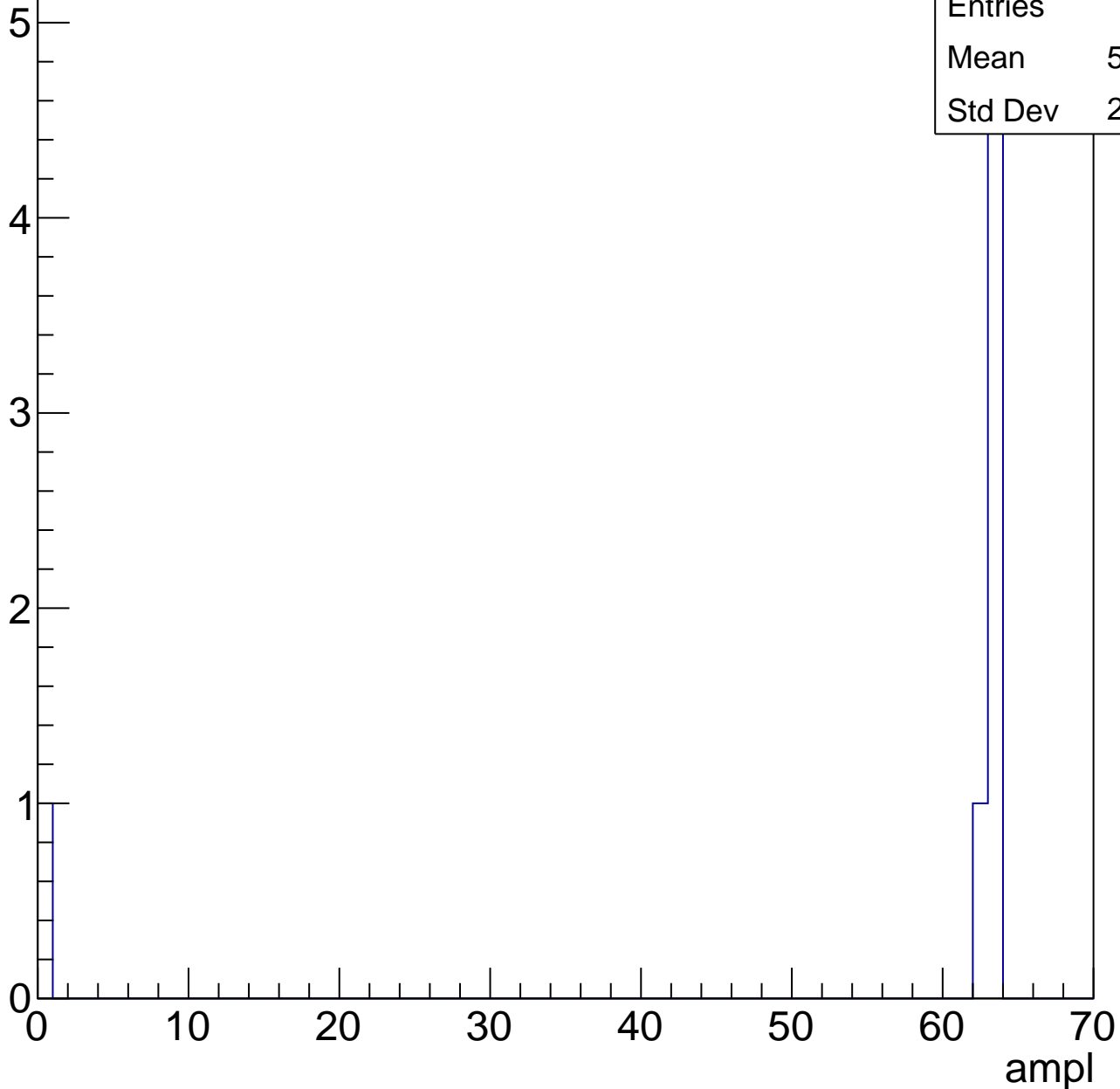


# B1L101S, U22-ch7, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	7
Mean	53.86
Std Dev	21.99





# B1L101S, U22-ch7, adc7

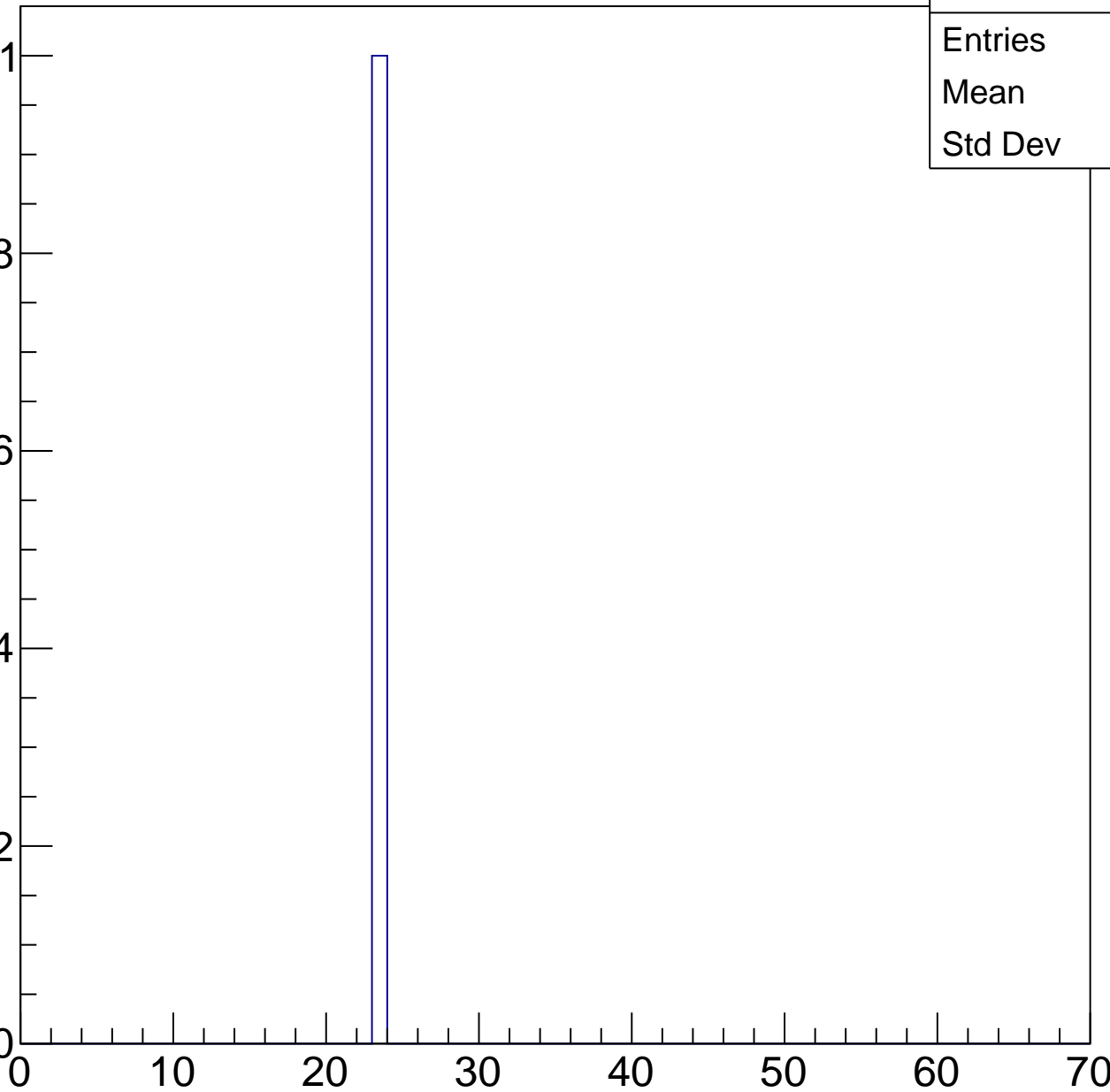
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

1  
0.8  
0.6  
0.4  
0.2  
0

Entries	1
Mean	23
Std Dev	0

ampl



# B1L101S, U22-ch8, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	86
Mean	29.92
Std Dev	4.859

**Gaus mean : 31.2035**

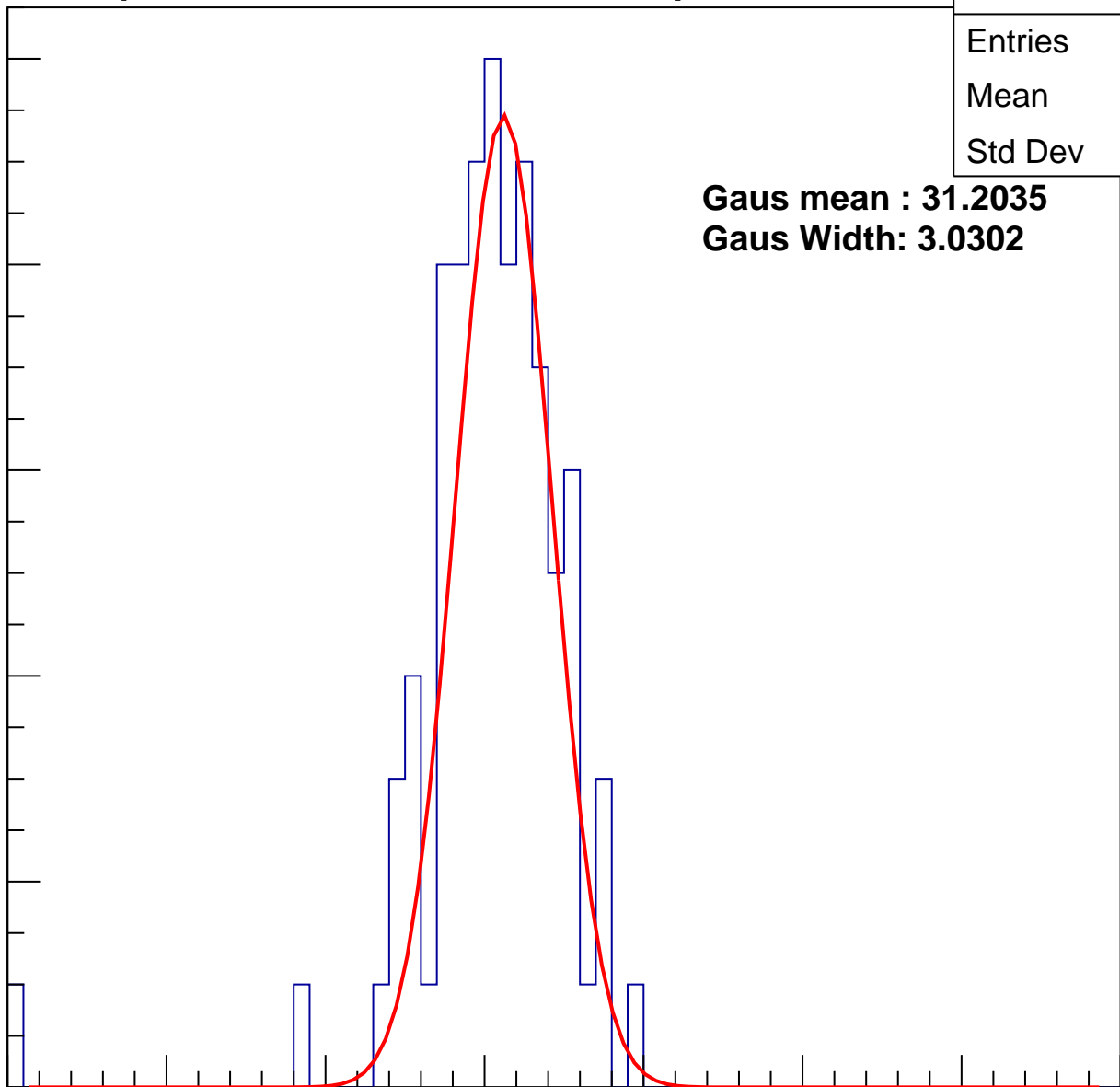
**Gaus Width: 3.0302**

Entry

10  
8  
6  
4  
2  
0

ampl

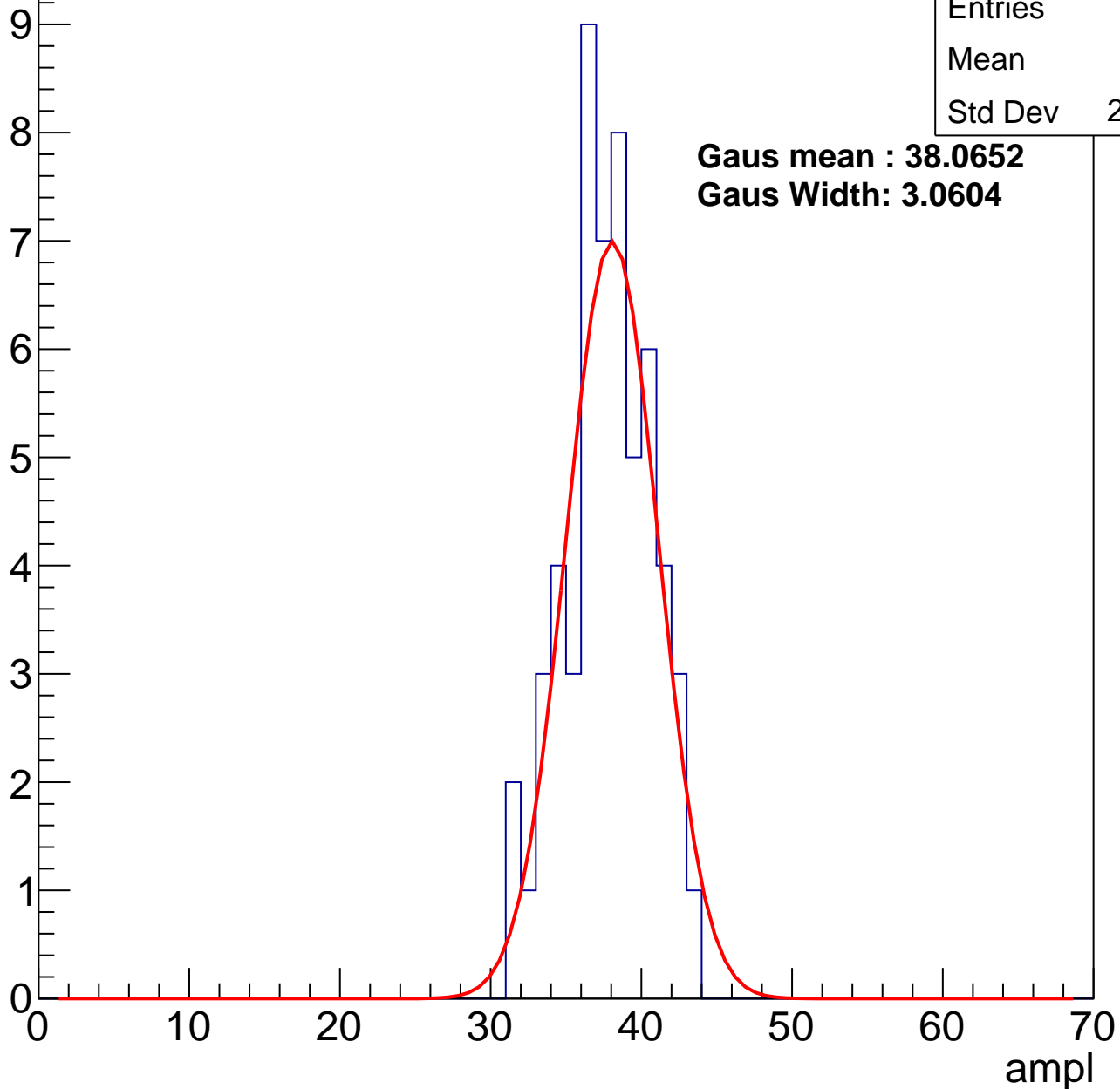
0 10 20 30 40 50 60 70



# B1L101S, U22-ch8, adc1

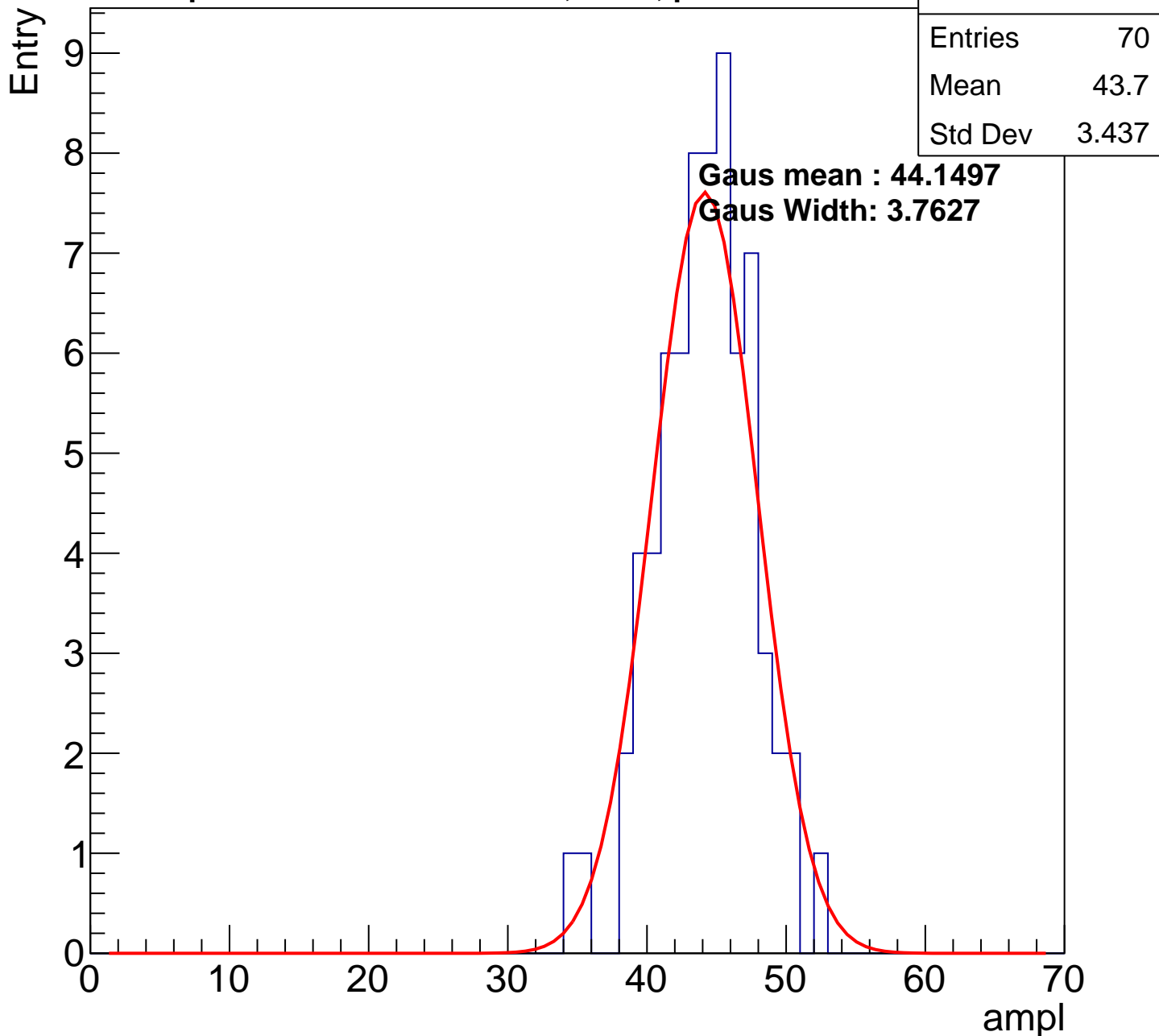
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U22-ch8, adc2

calib\_packv5\_042523\_0143.root, FC#0, port D2

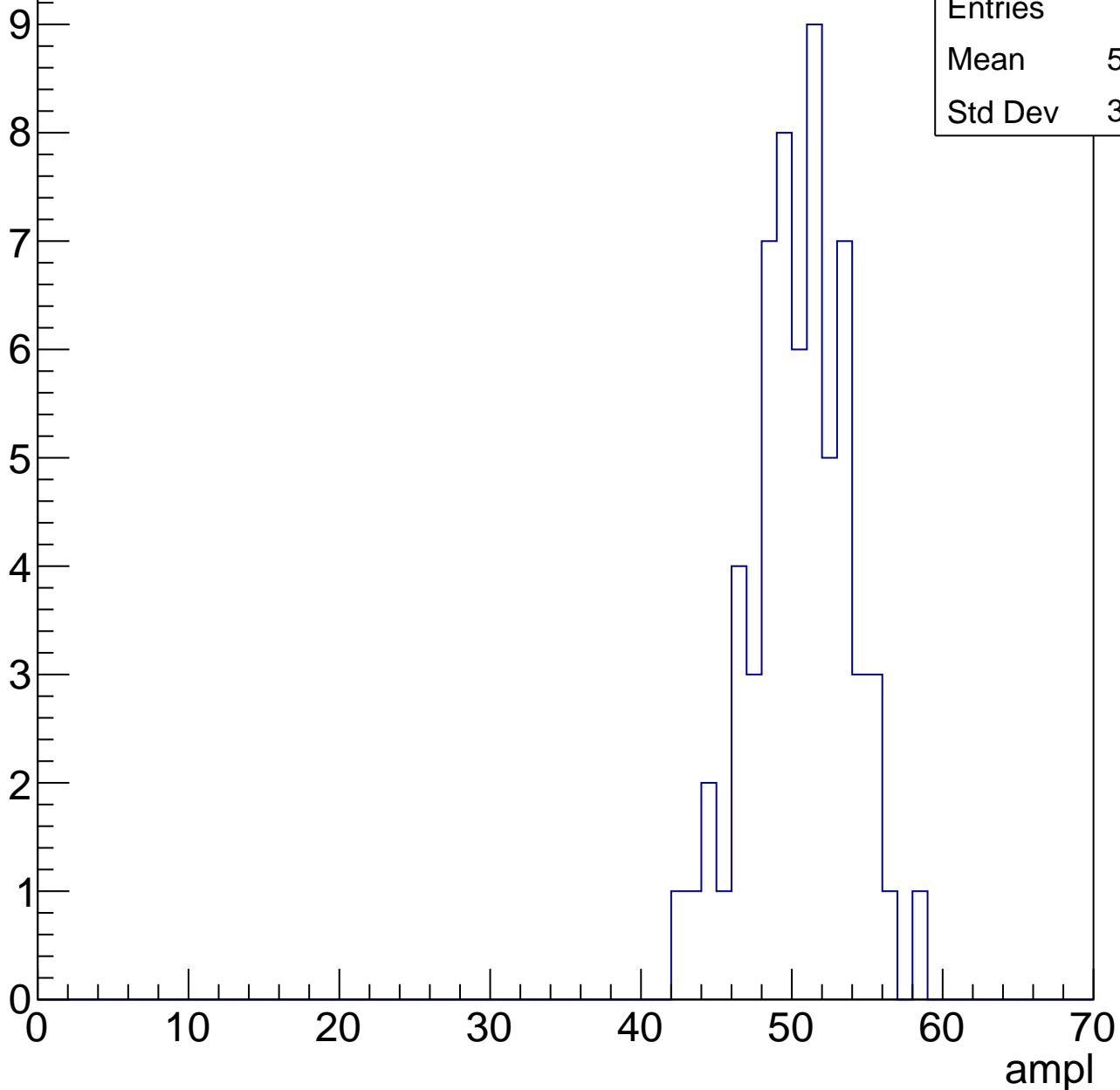


# B1L101S, U22-ch8, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

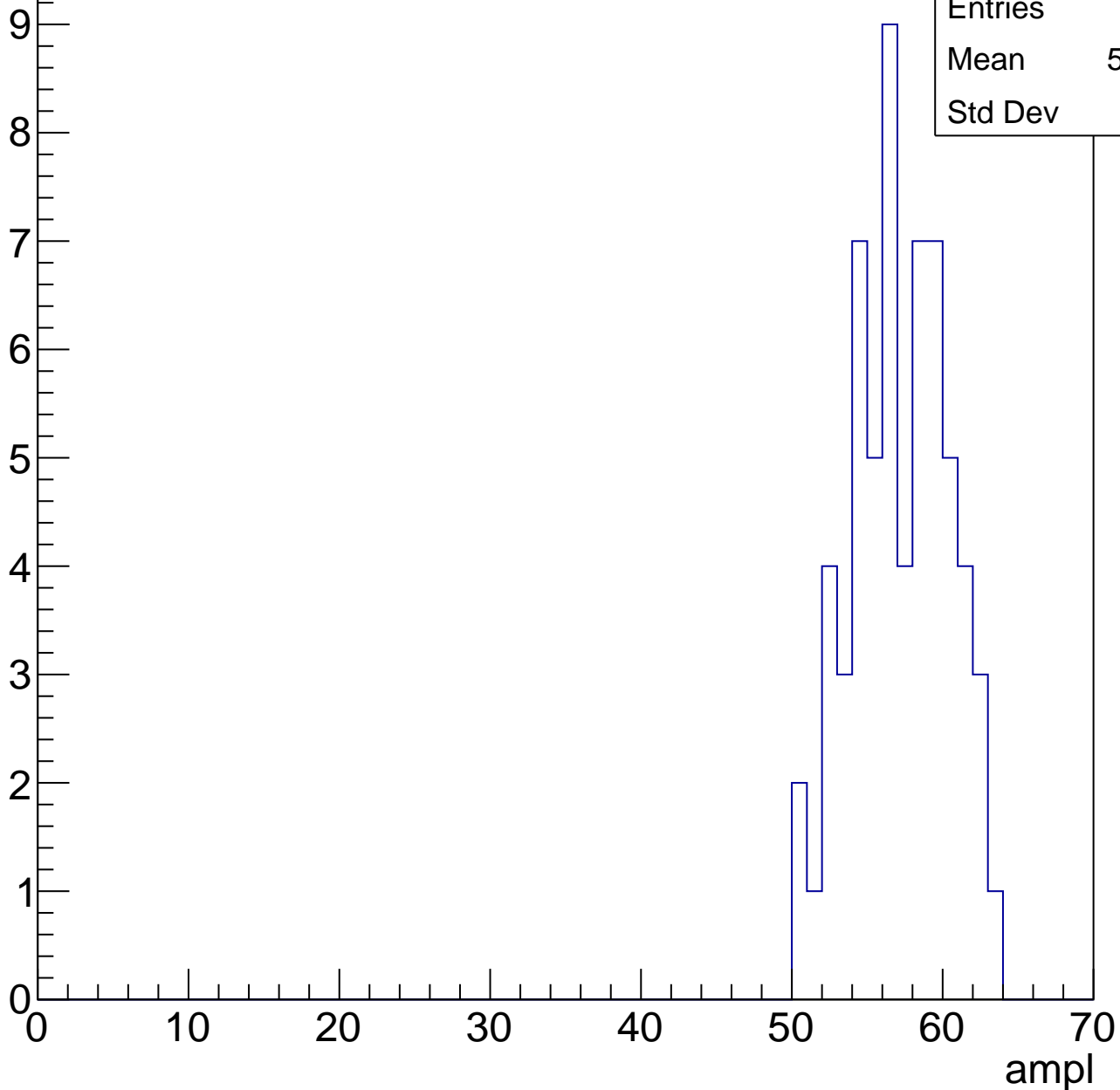
Entries	62
Mean	50.03
Std Dev	3.243



# B1L101S, U22-ch8, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



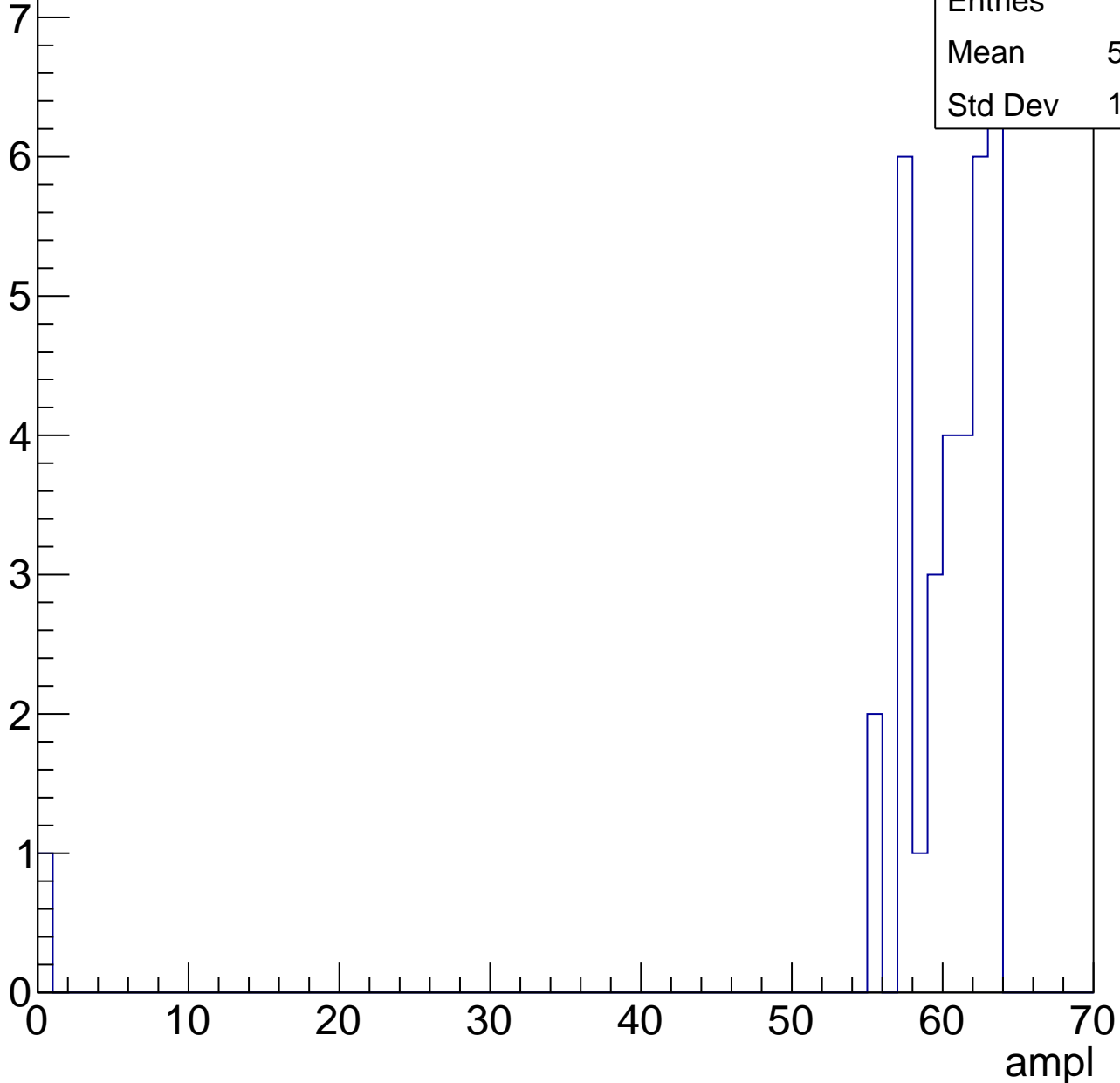
Entries	62
Mean	56.69
Std Dev	3.17

# B1L101S, U22-ch8, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

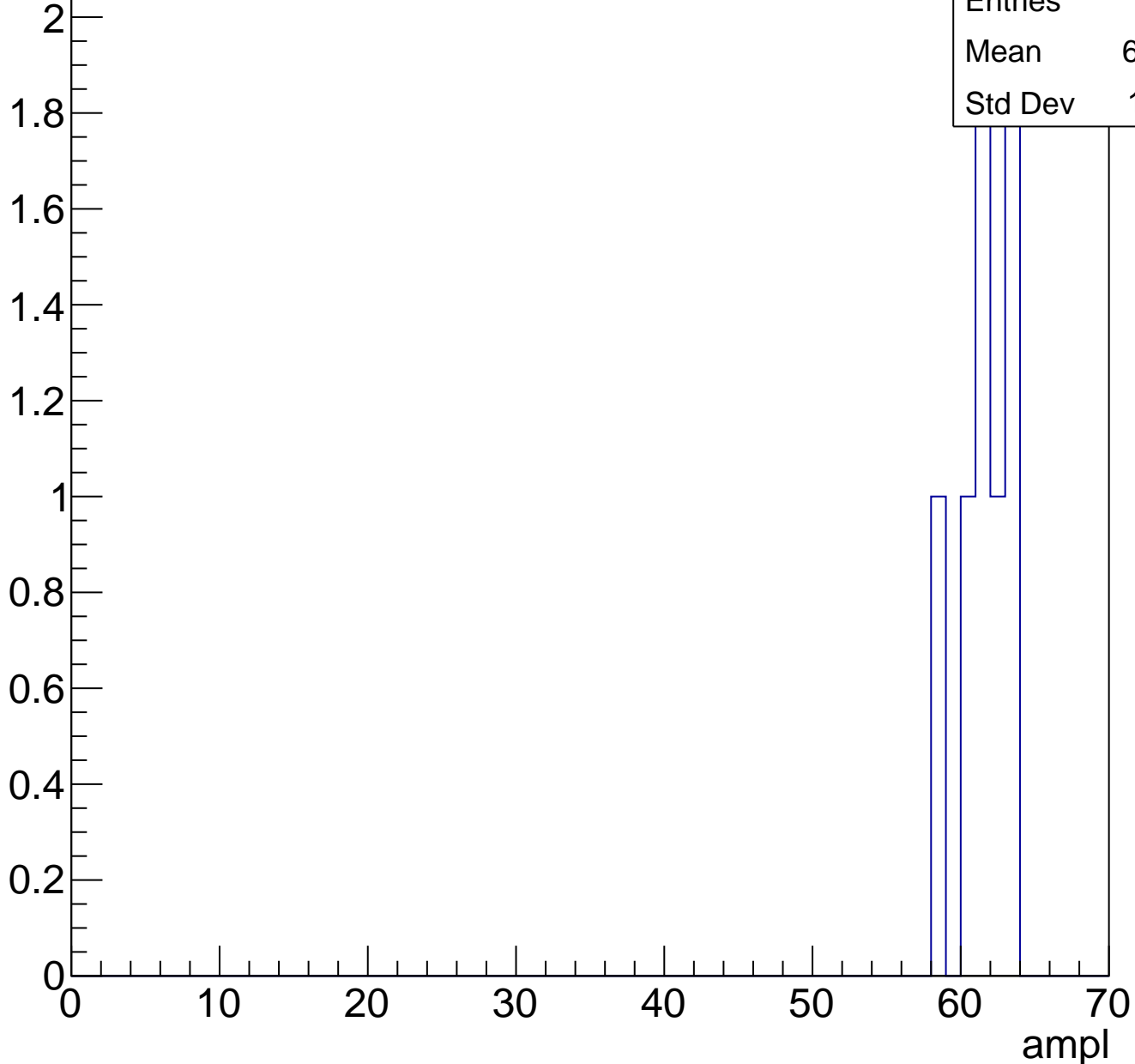
Entries	34
Mean	58.35
Std Dev	10.45



# B1L101S, U22-ch8, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U22-ch8, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L101S, U22-ch9, adc0

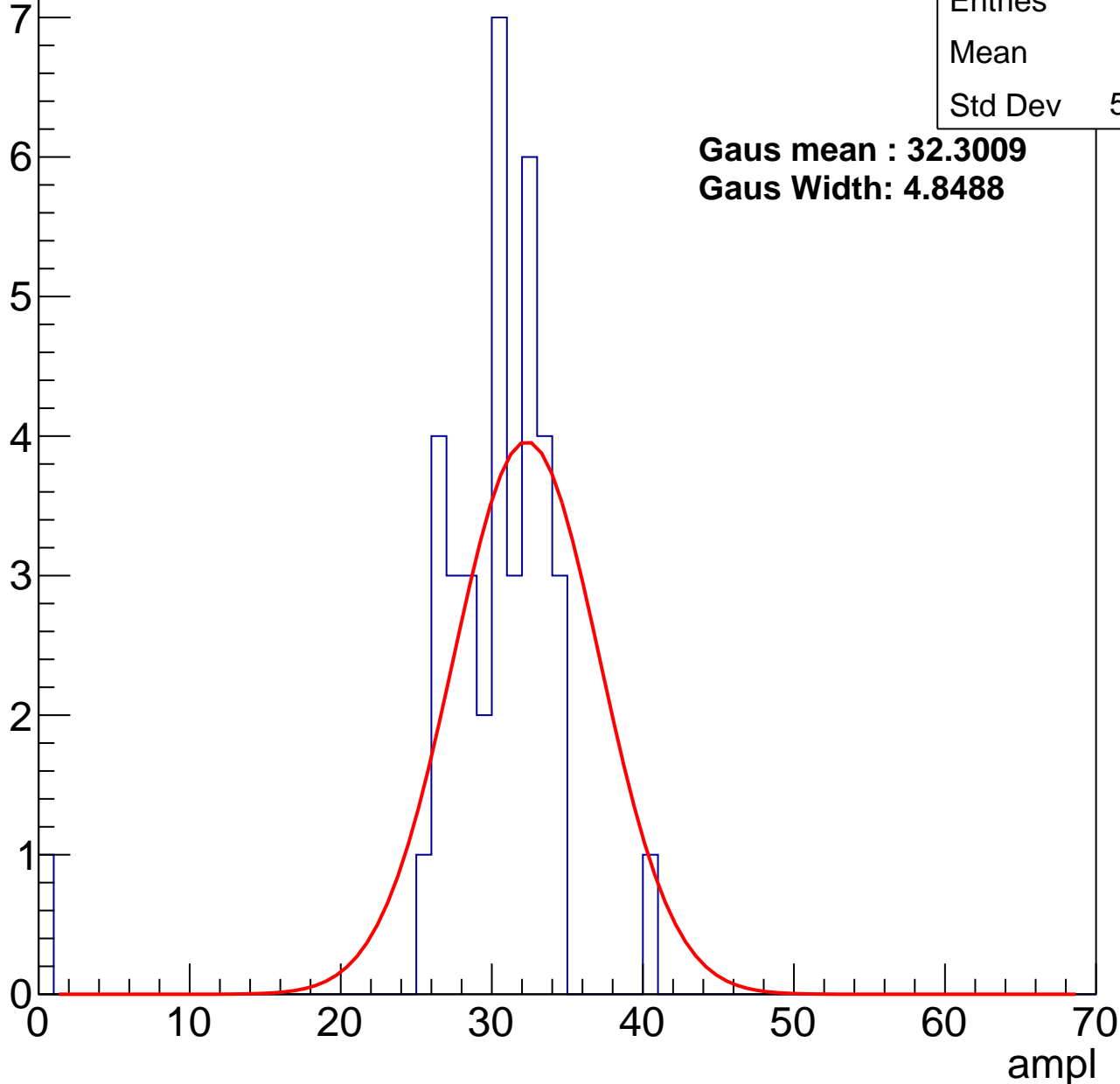
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	38
Mean	29.5
Std Dev	5.693

**Gaus mean : 32.3009**

**Gaus Width: 4.8488**



# B1L101S, U22-ch9, adc1

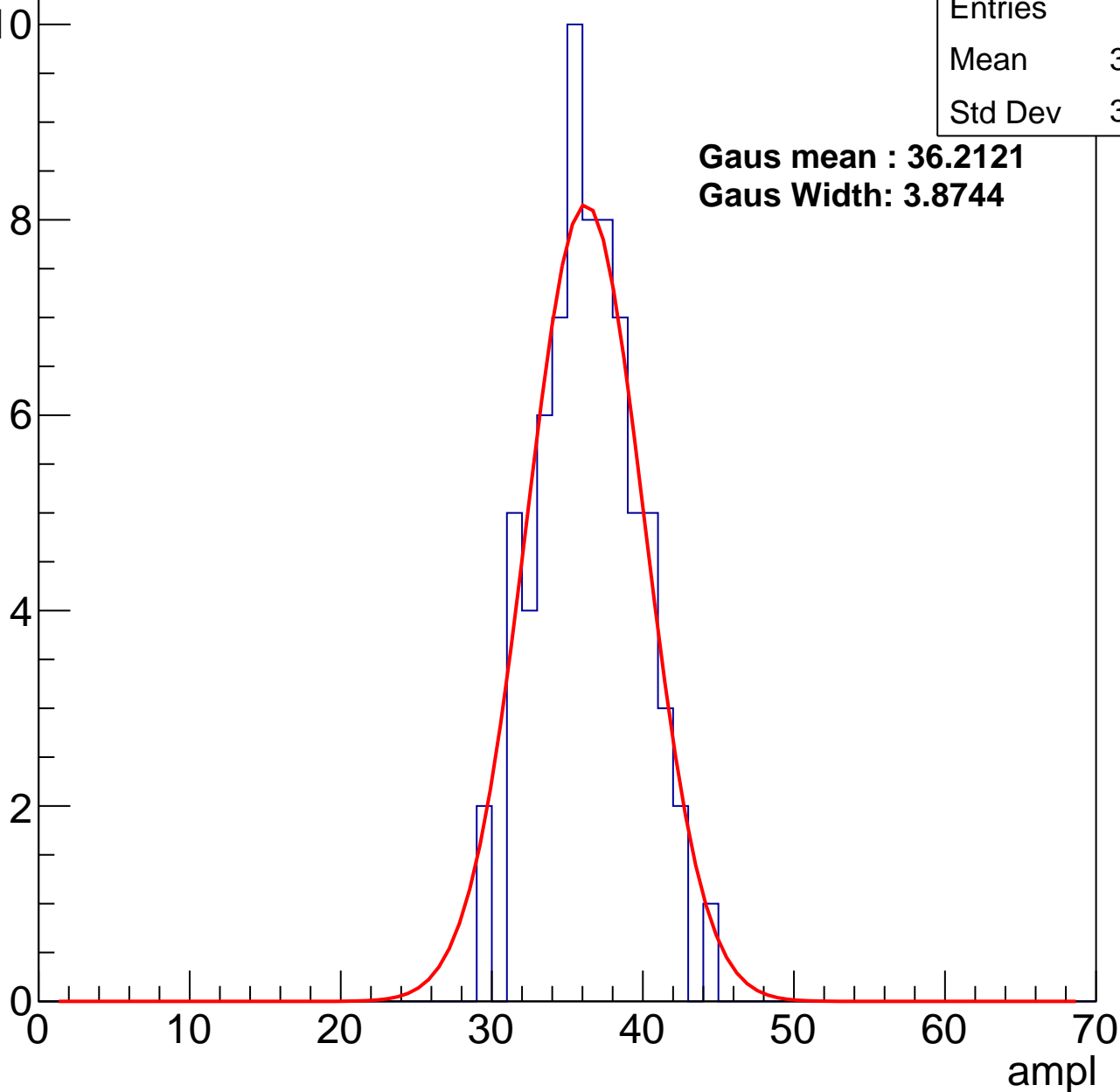
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	73
Mean	35.93
Std Dev	3.207

**Gaus mean : 36.2121**

**Gaus Width: 3.8744**



# B1L101S, U22-ch9, adc2

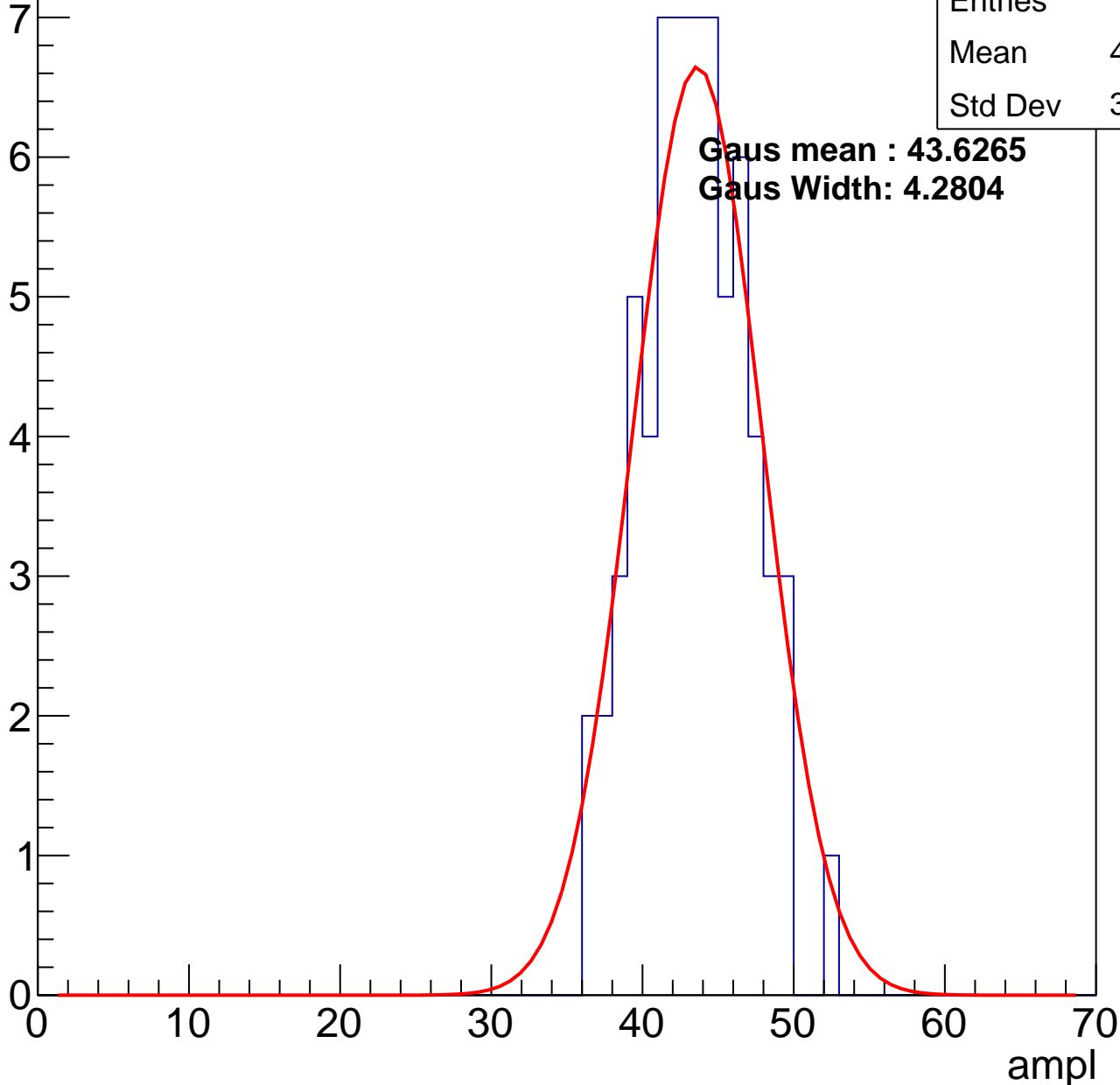
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	66
Mean	42.98
Std Dev	3.492

**Gaus mean : 43.6265**

**Gaus Width: 4.2804**



# B1L101S, U22-ch9, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	72
Mean	49.5
Std Dev	3.508

Entry

10

8

6

4

2

0

0

10

20

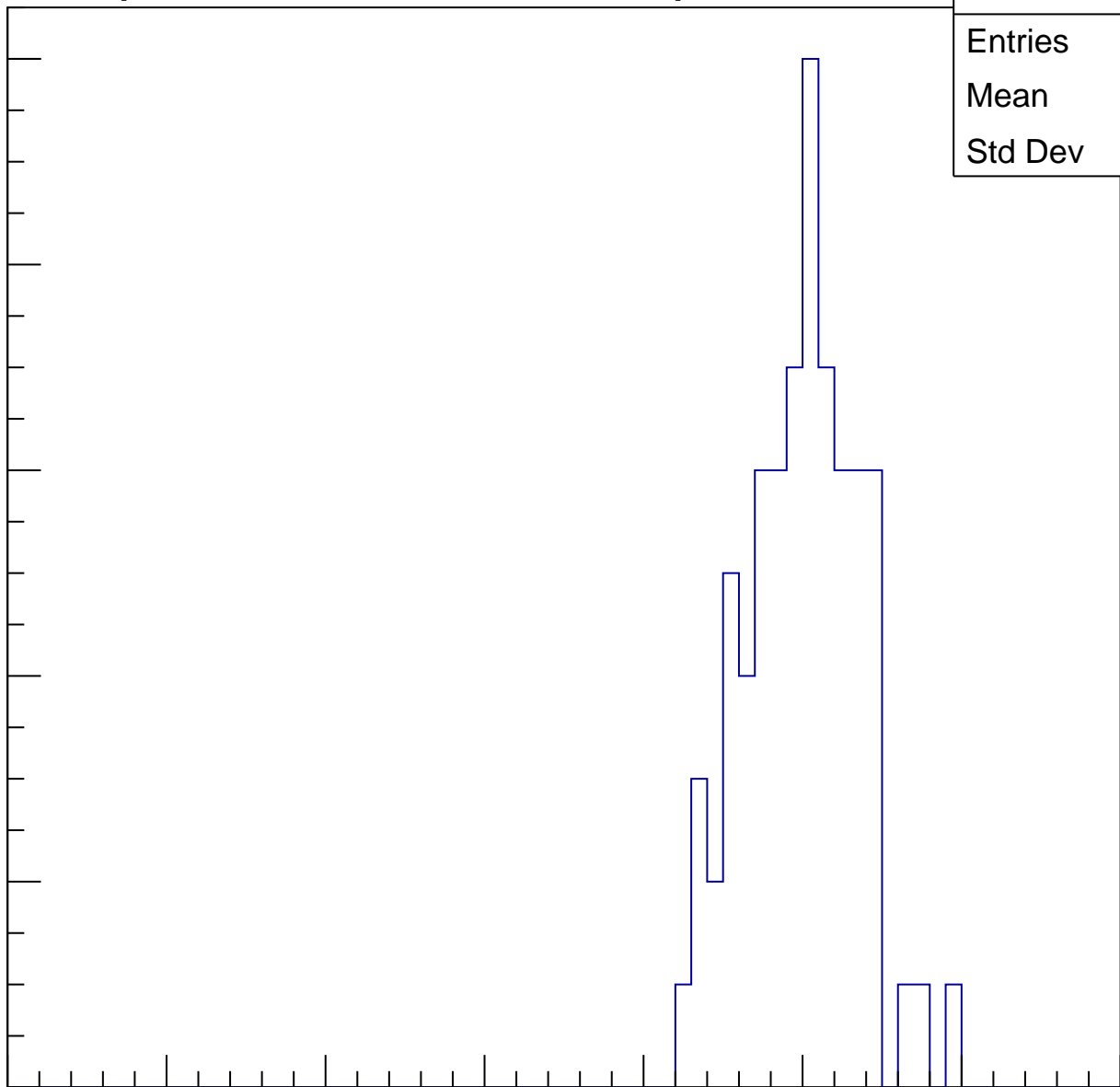
30

40

50

60

ampl

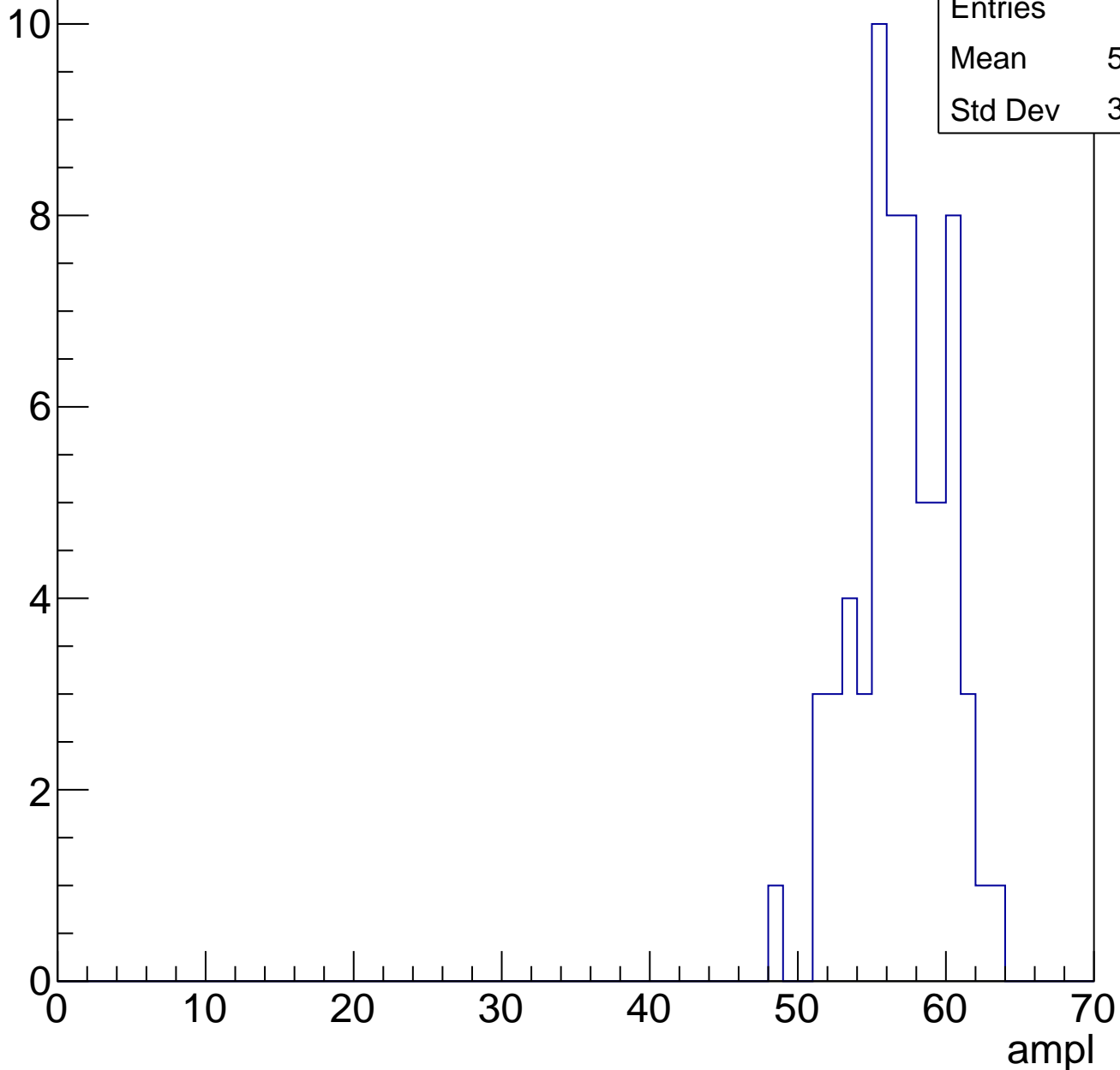


# B1L101S, U22-ch9, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	63
Mean	56.48
Std Dev	3.065

Entry

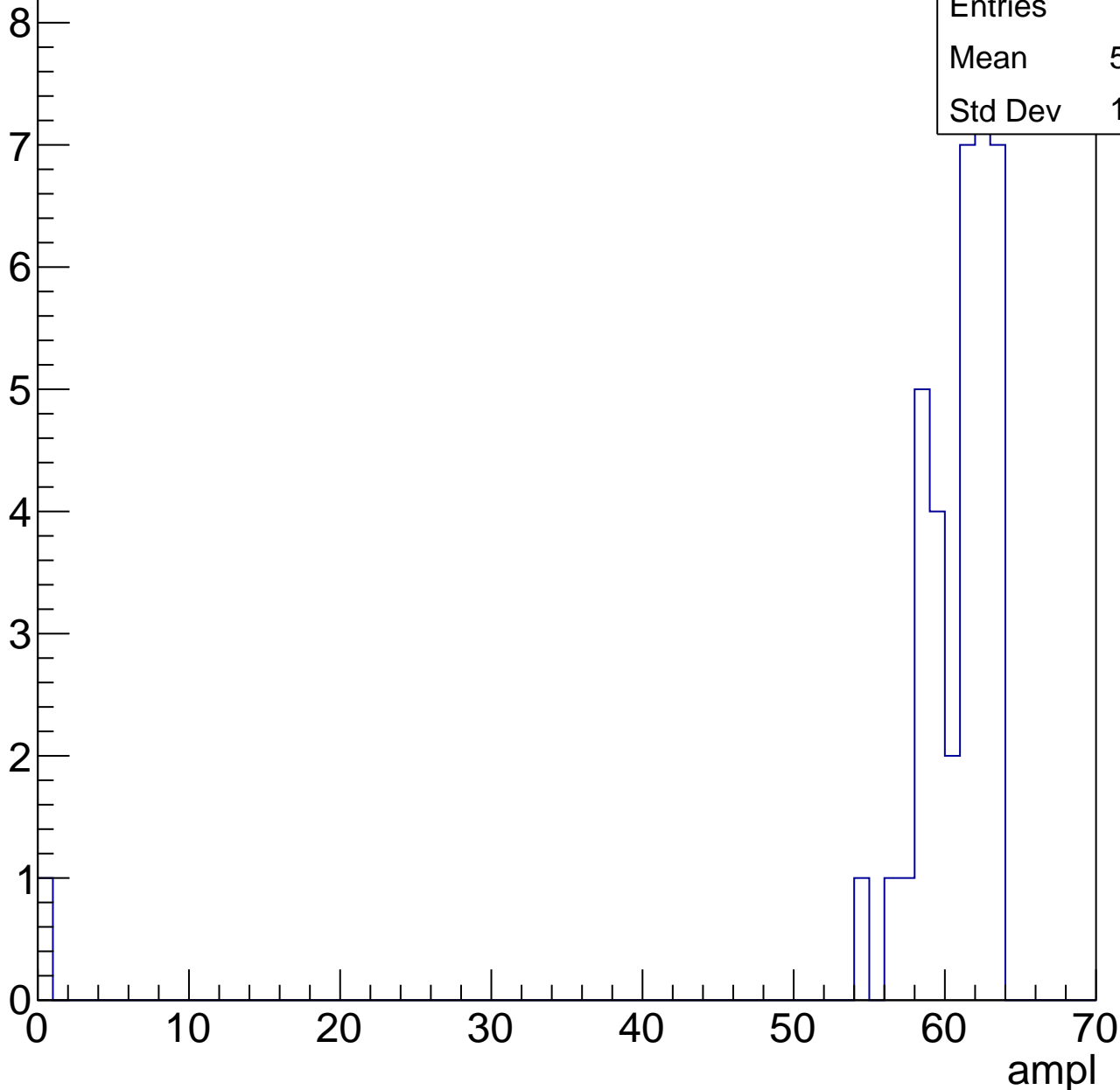


# B1L101S, U22-ch9, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	37
Mean	58.84
Std Dev	10.05



# B1L101S, U22-ch9, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U22-ch9, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U22-ch10, adc0

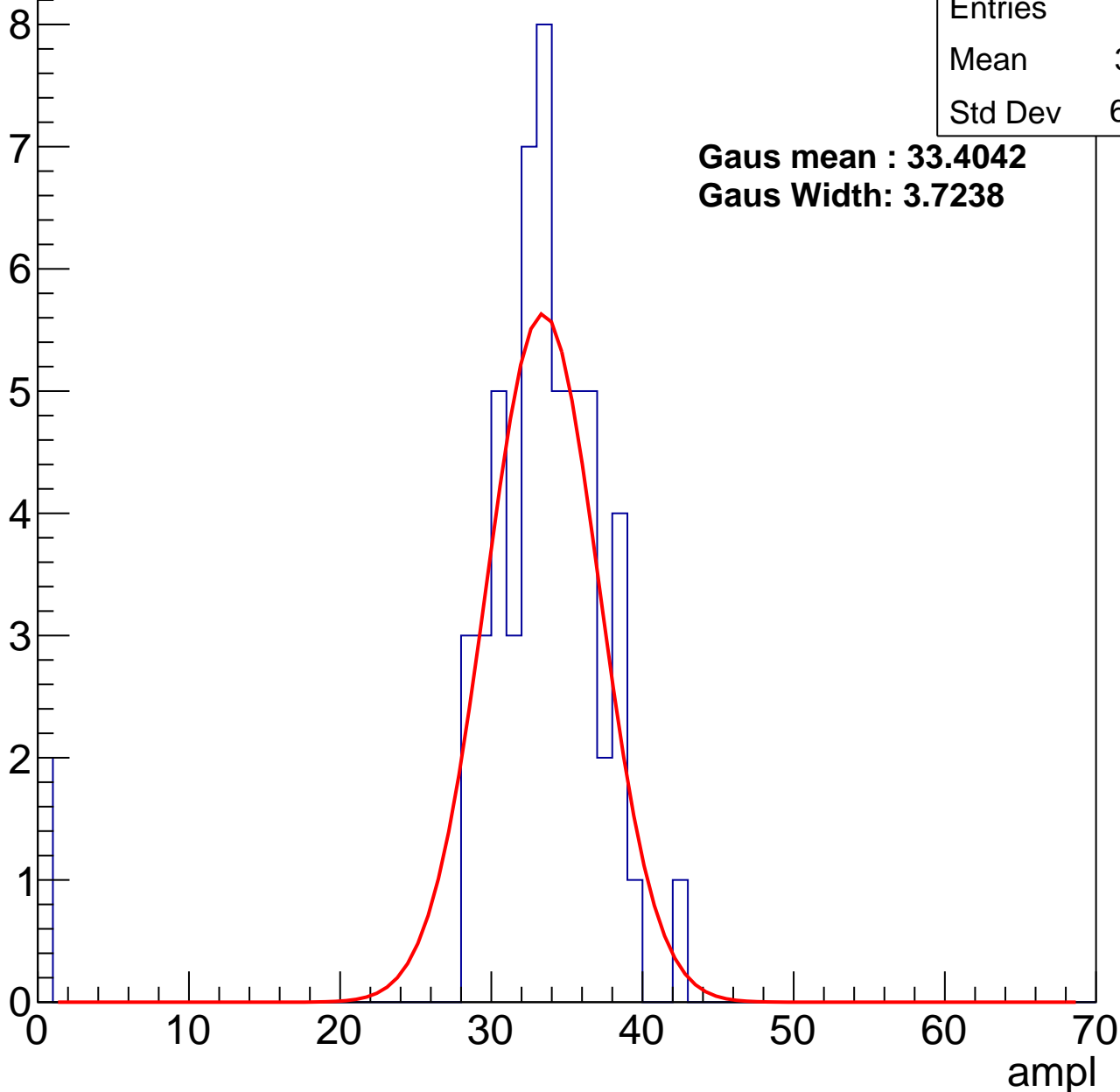
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	54
Mean	32.11
Std Dev	6.994

**Gaus mean : 33.4042**

**Gaus Width: 3.7238**



# B1L101S, U22-ch10, adc1

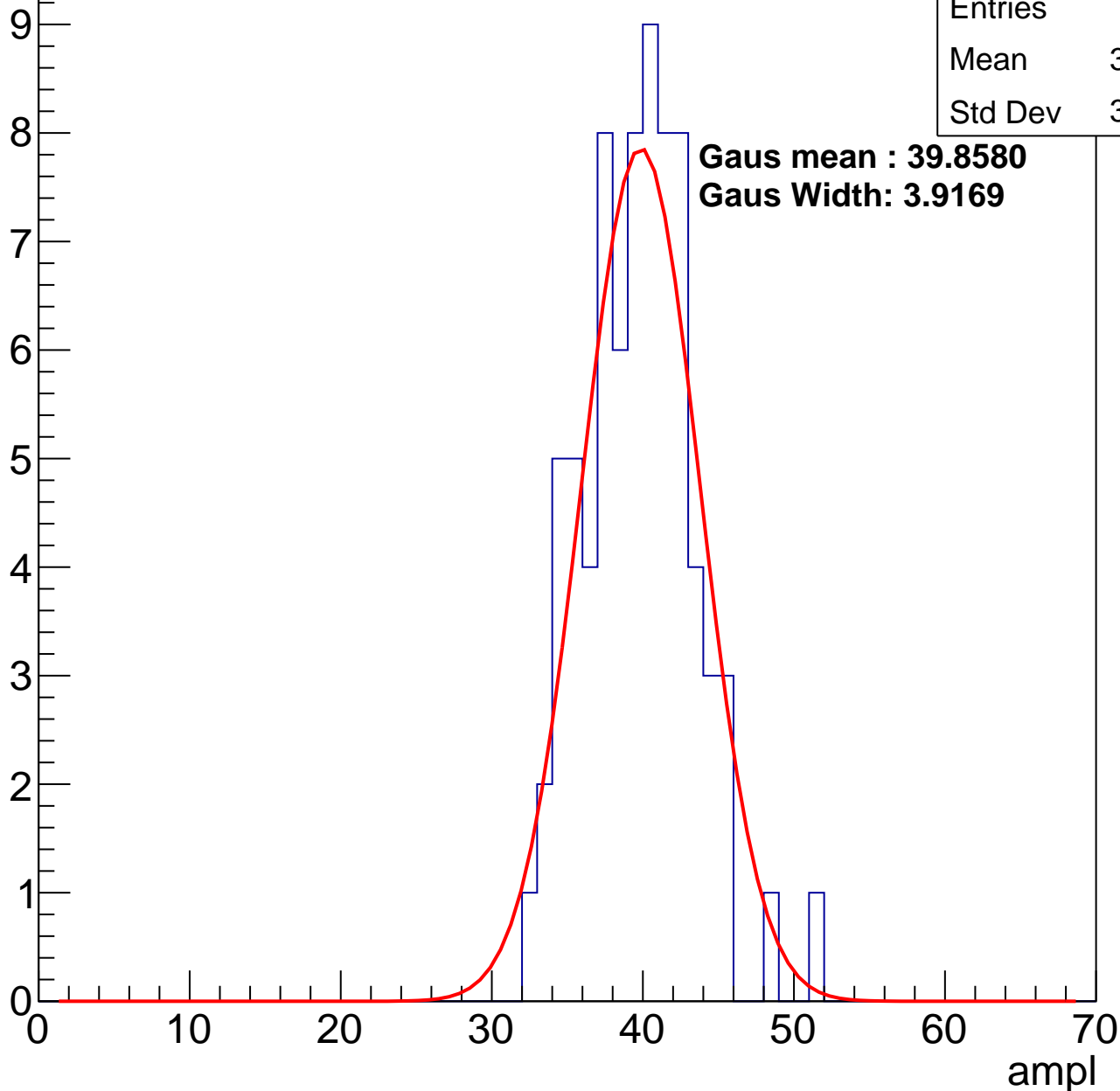
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	76
Mean	39.28
Std Dev	3.589

**Gaus mean : 39.8580**

**Gaus Width: 3.9169**



# B1L101S, U22-ch10, adc2

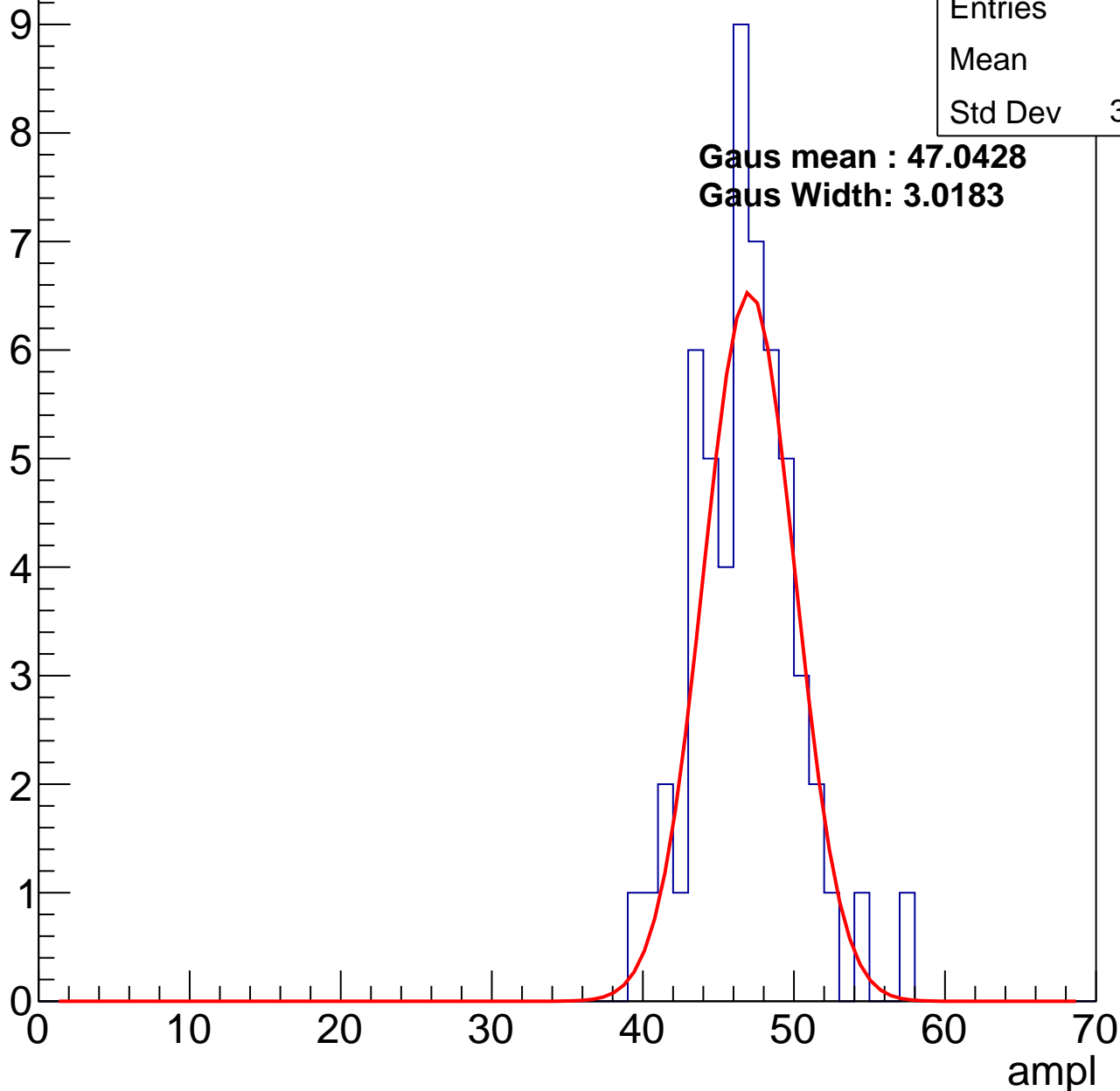
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	55
Mean	46.4
Std Dev	3.344

**Gaus mean : 47.0428**

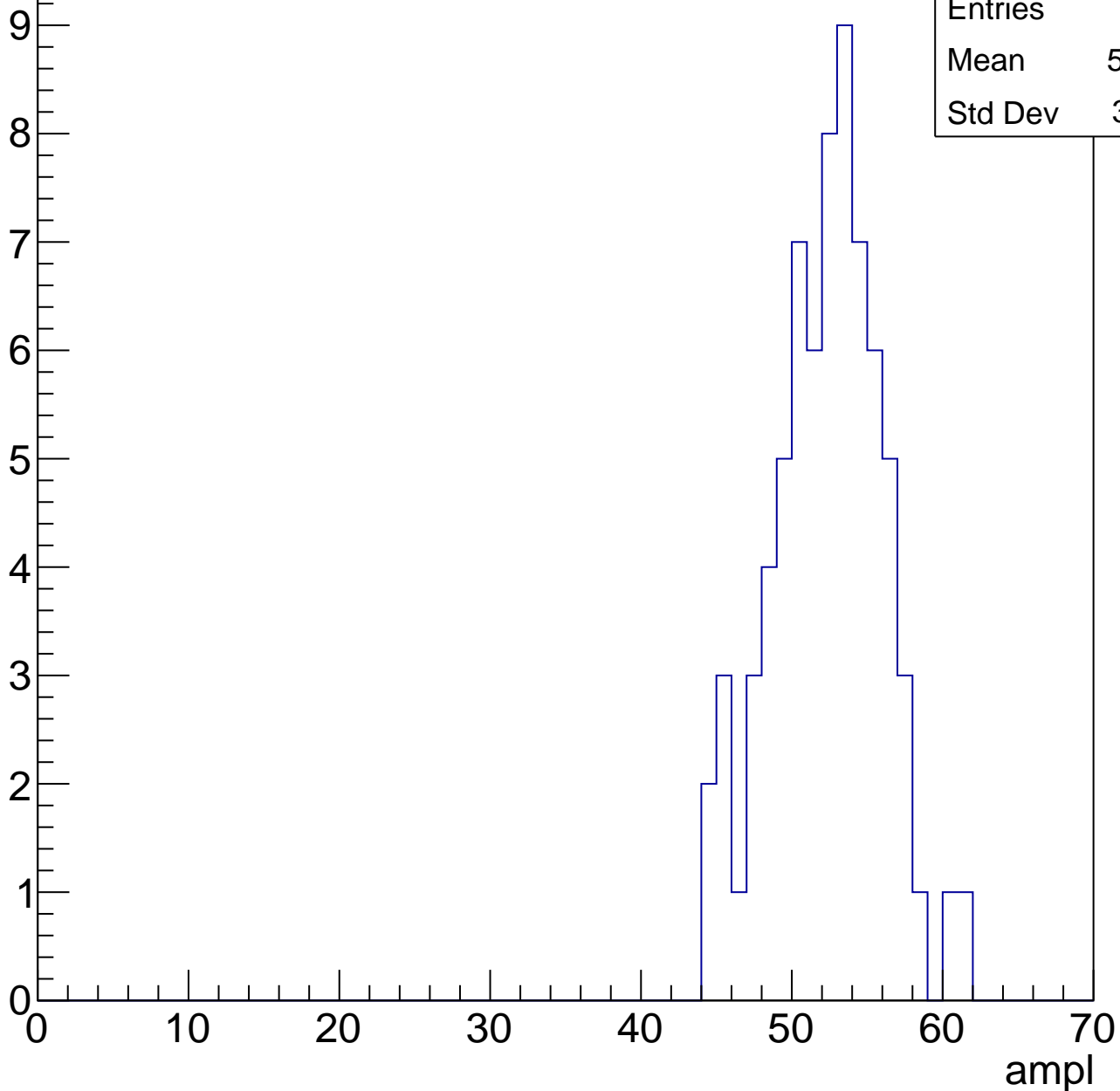
**Gaus Width: 3.0183**



# B1L101S, U22-ch10, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

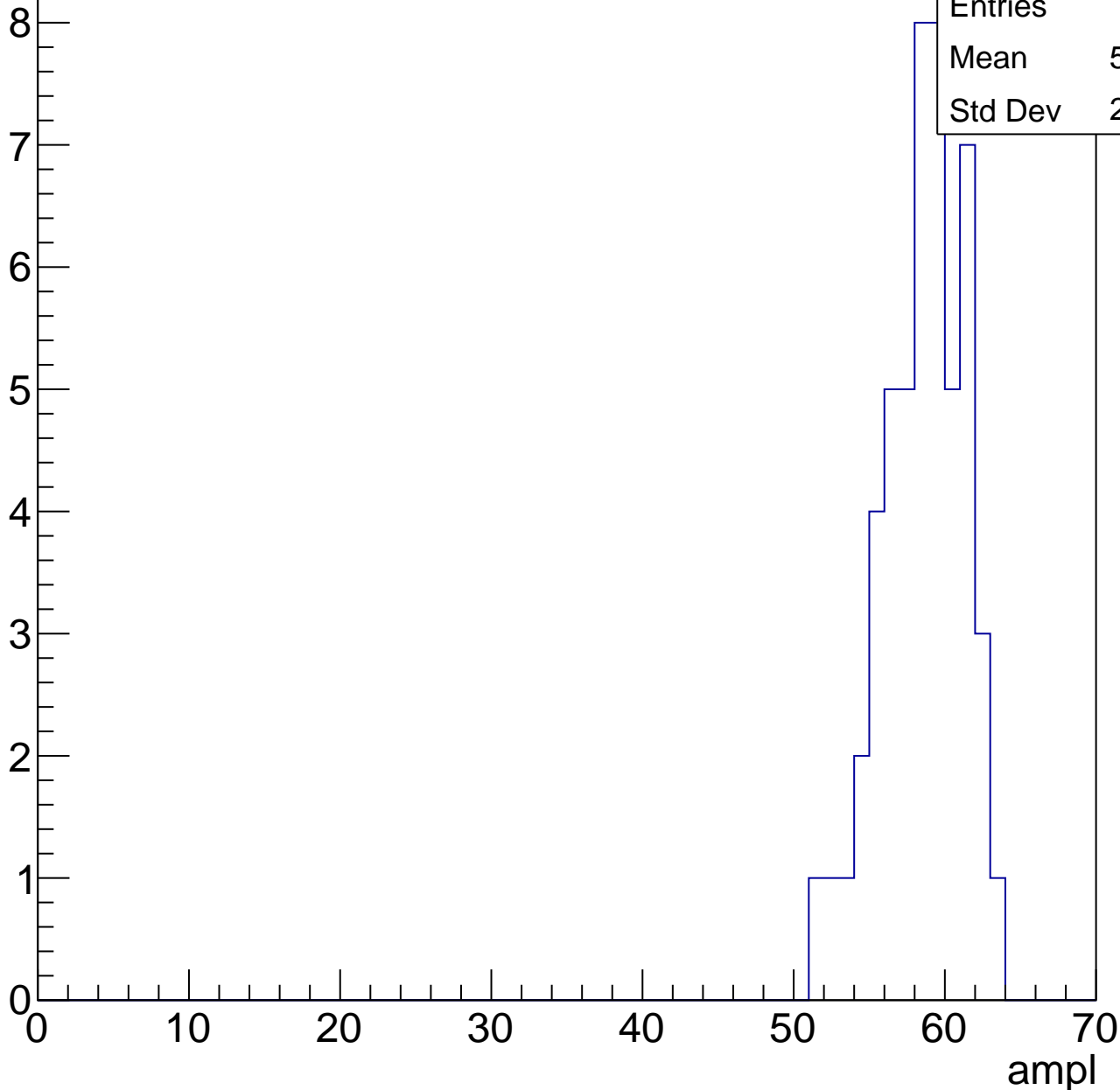


# B1L101S, U22-ch10, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	51
Mean	58.06
Std Dev	2.682

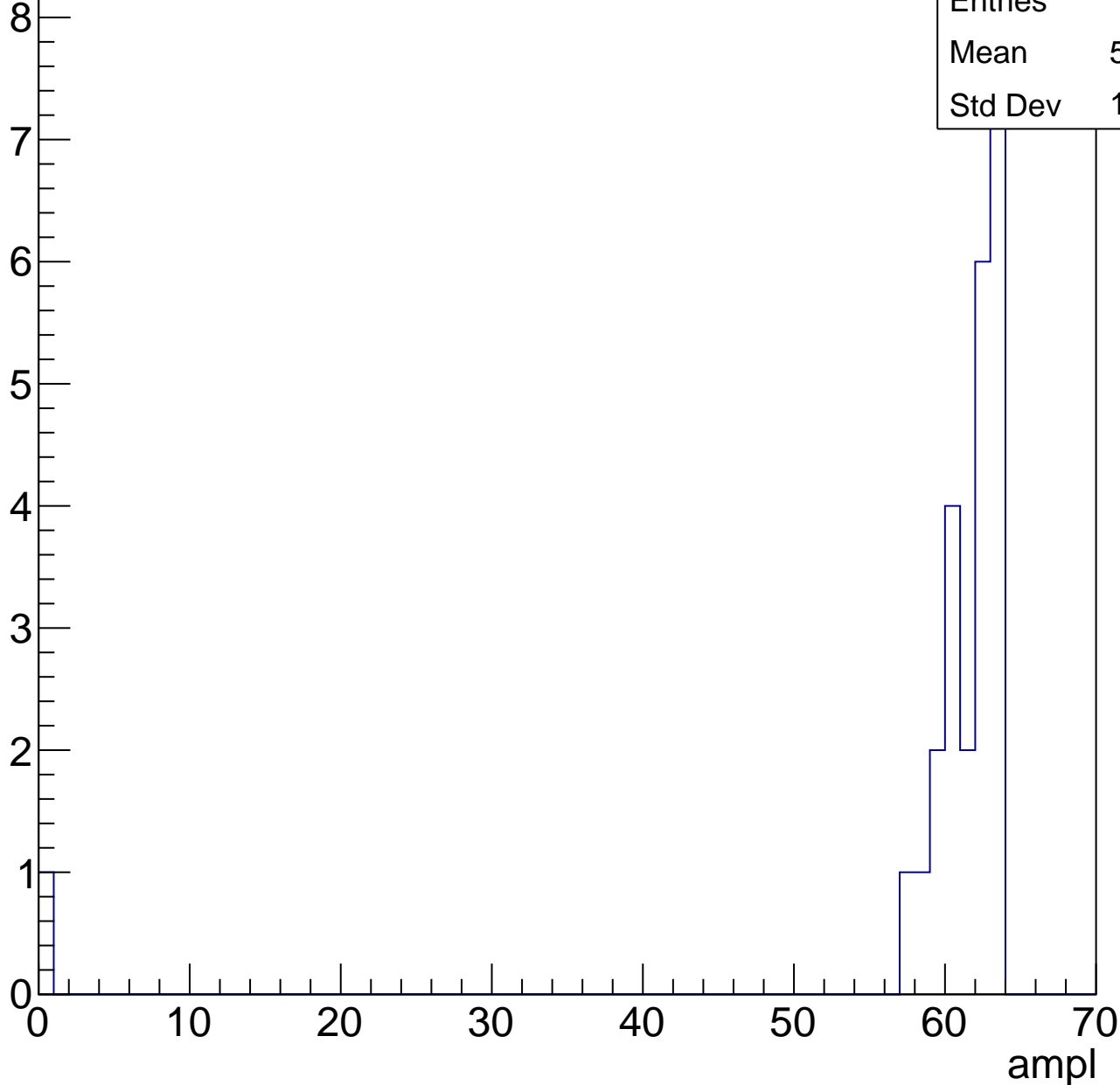


# B1L101S, U22-ch10, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	25
Mean	58.84
Std Dev	12.13



# B1L101S, U22-ch10, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

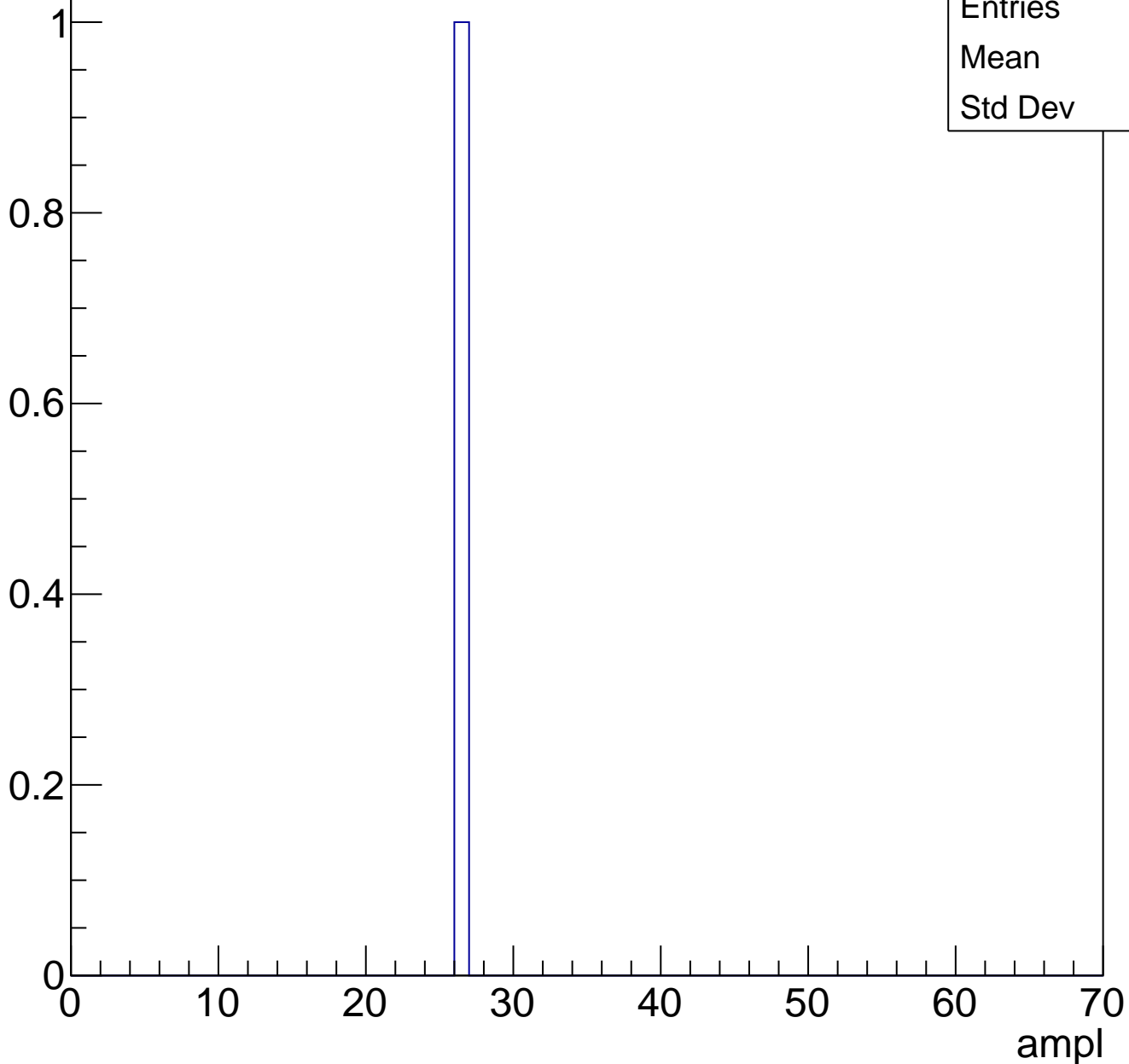




# B1L101S, U22-ch10, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



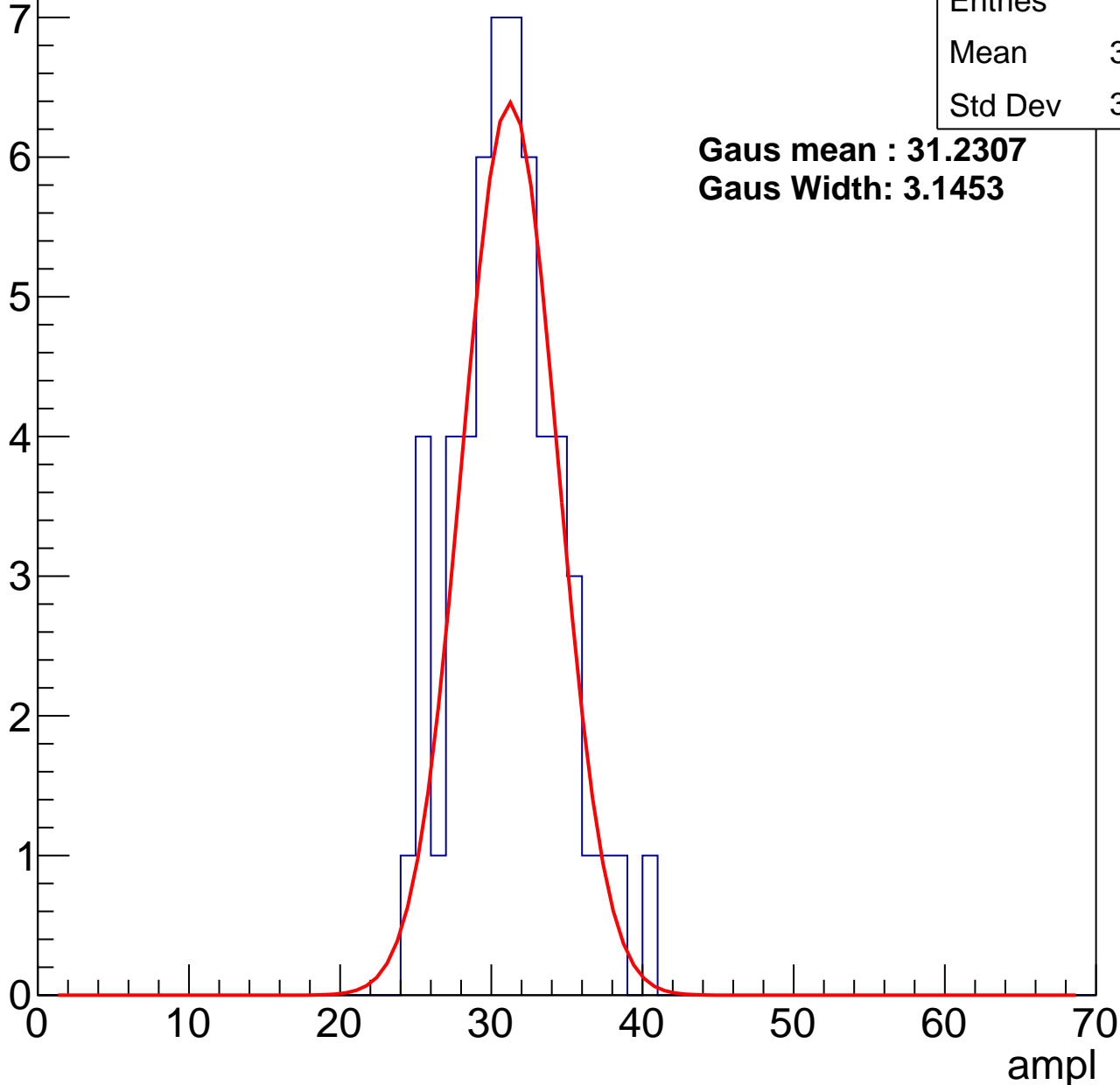
# B1L101S, U22-ch11, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	55
Mean	30.67
Std Dev	3.412

**Gaus mean : 31.2307**  
**Gaus Width: 3.1453**



# B1L101S, U22-ch11, adc1

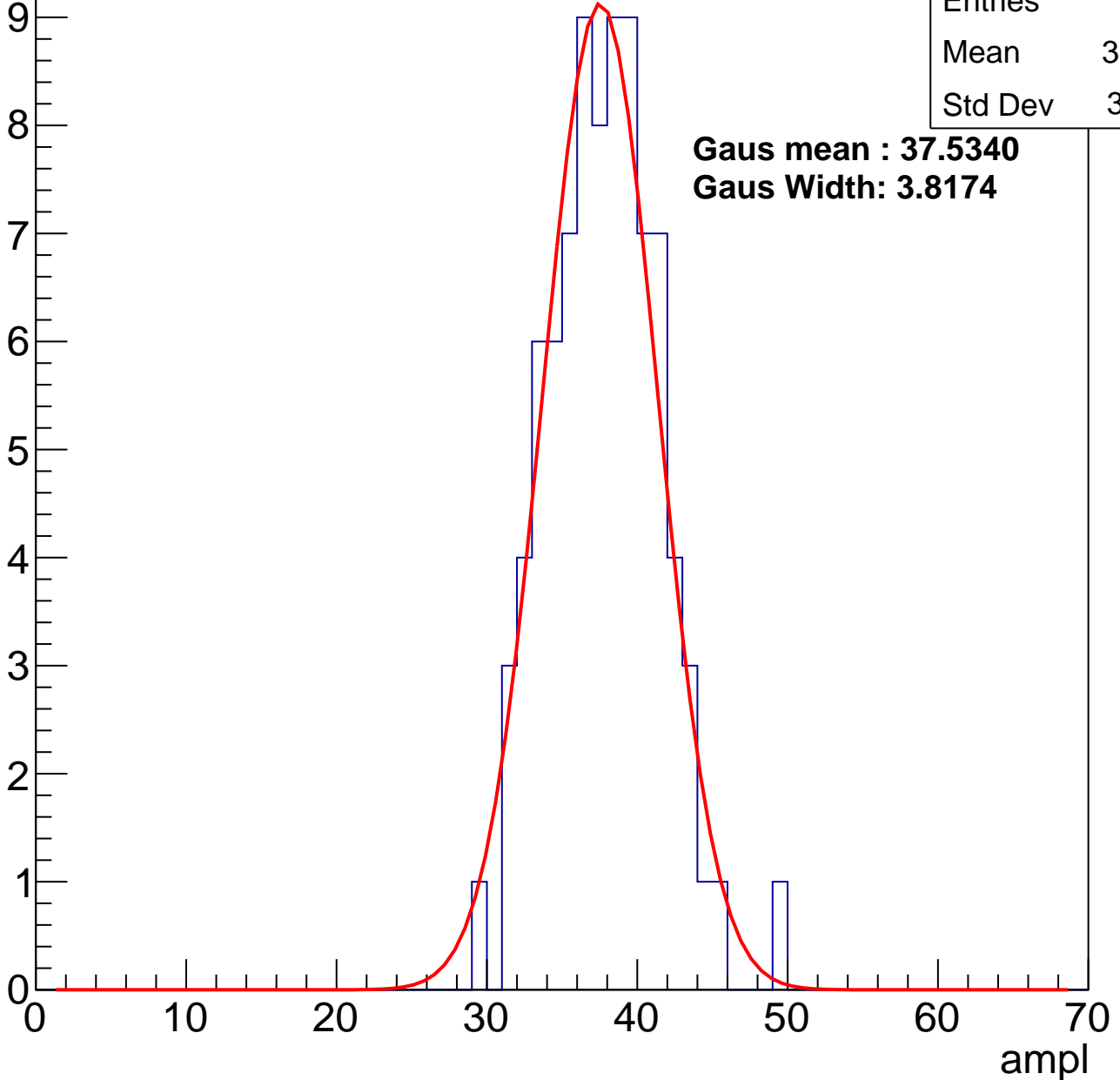
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	86
Mean	37.35
Std Dev	3.631

**Gaus mean : 37.5340**

**Gaus Width: 3.8174**



# B1L101S, U22-ch11, adc2

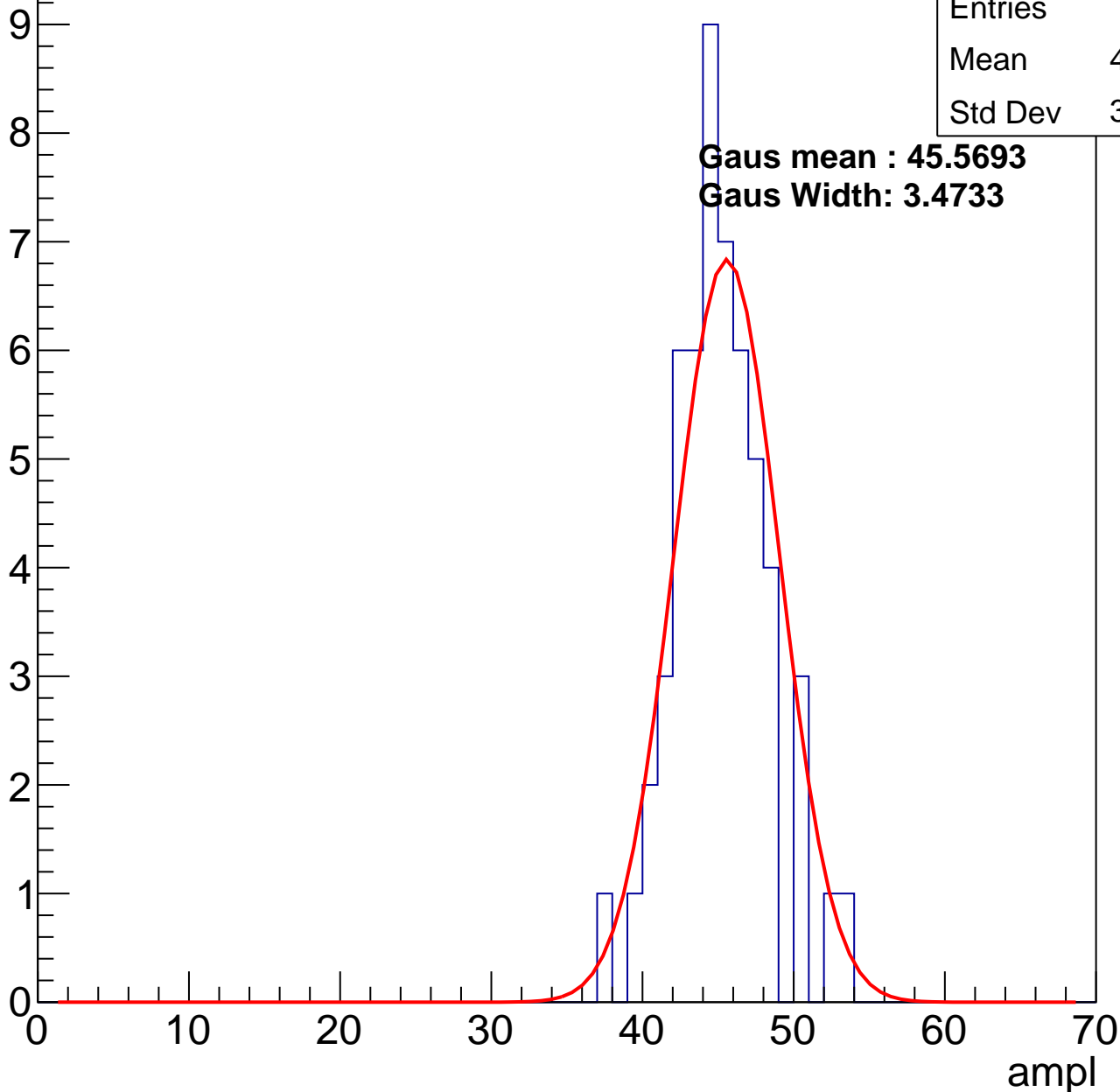
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	55
Mean	44.69
Std Dev	3.104

**Gaus mean : 45.5693**

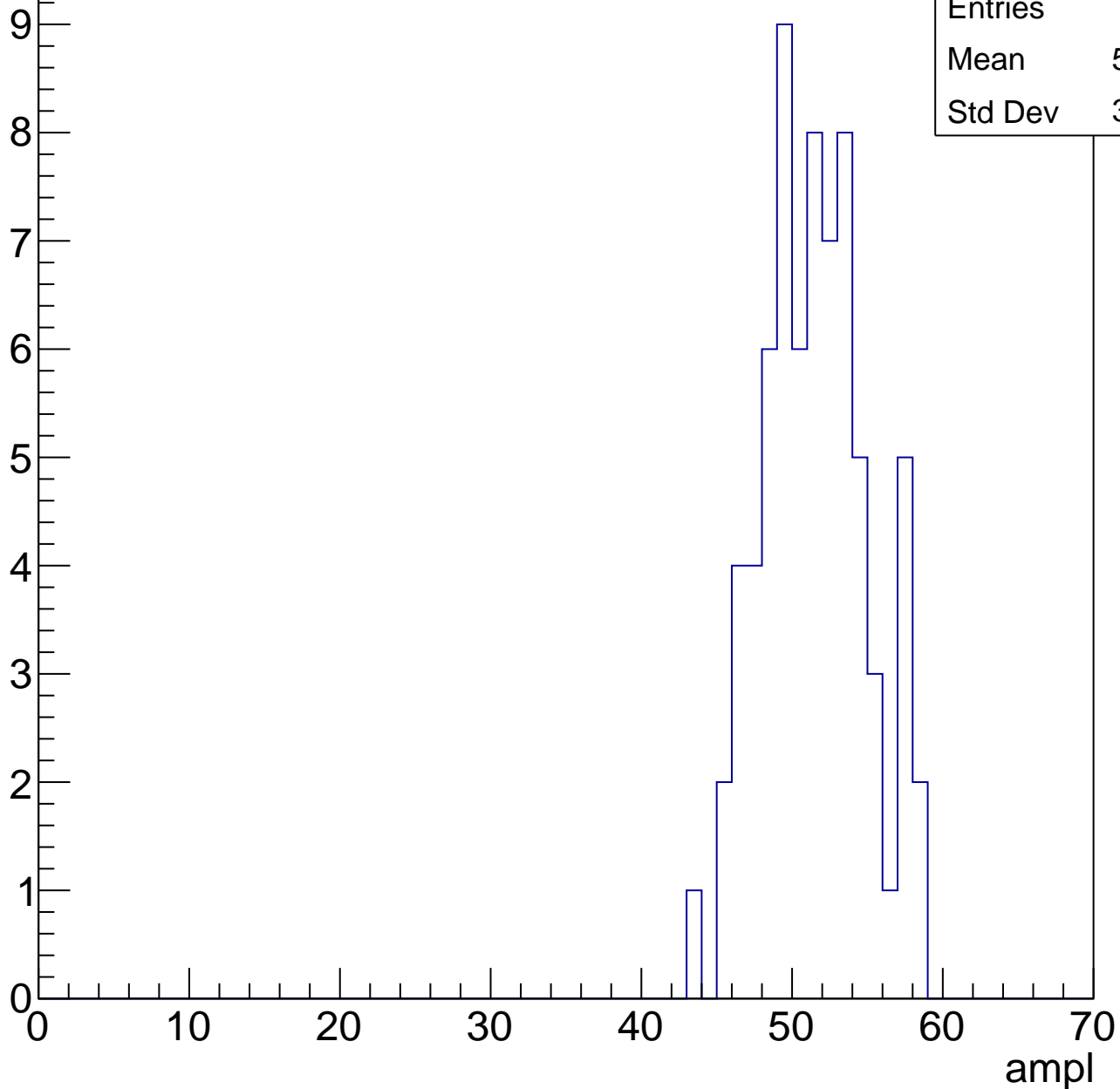
**Gaus Width: 3.4733**



# B1L101S, U22-ch11, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

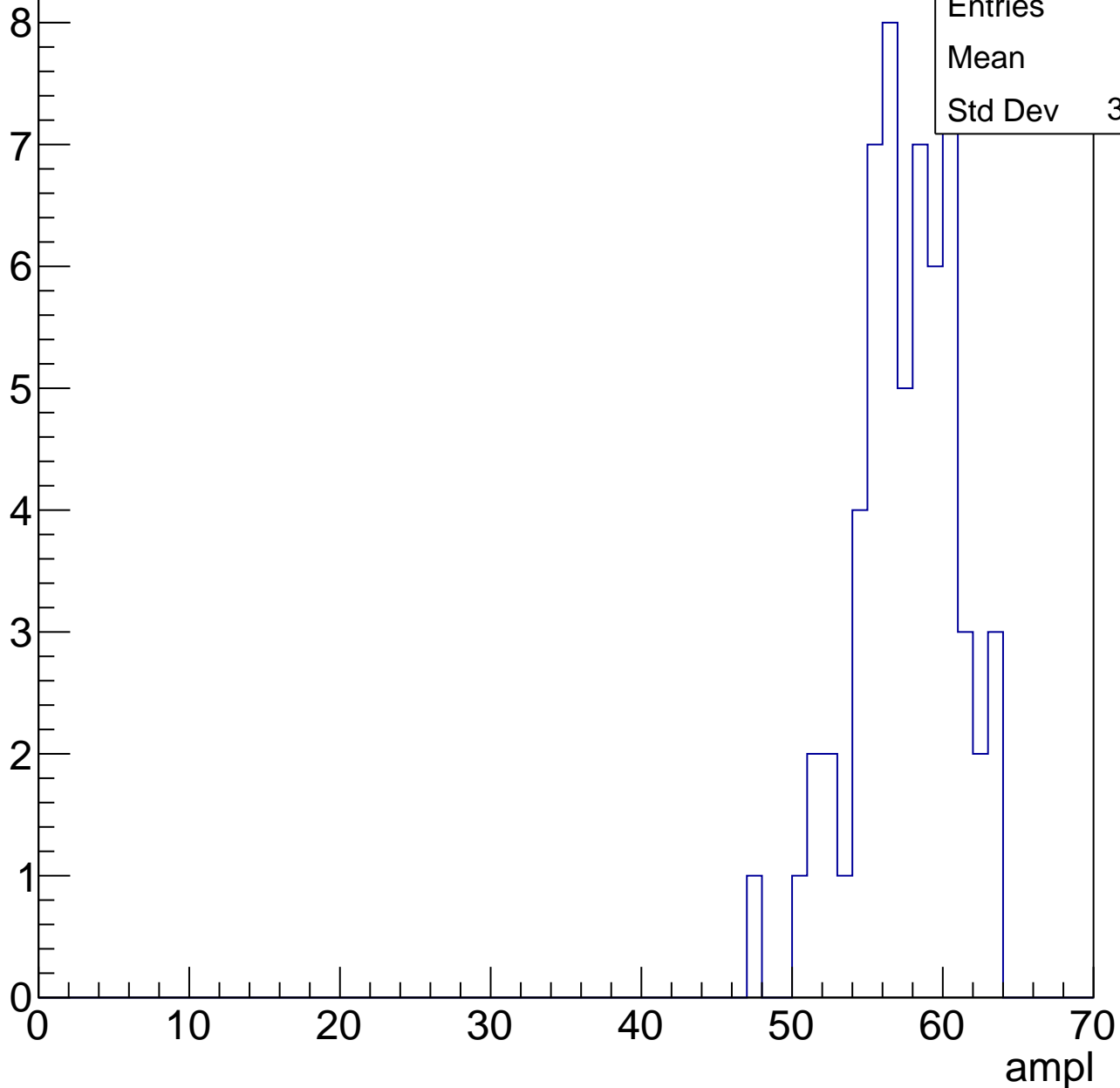
Entry



# B1L101S, U22-ch11, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

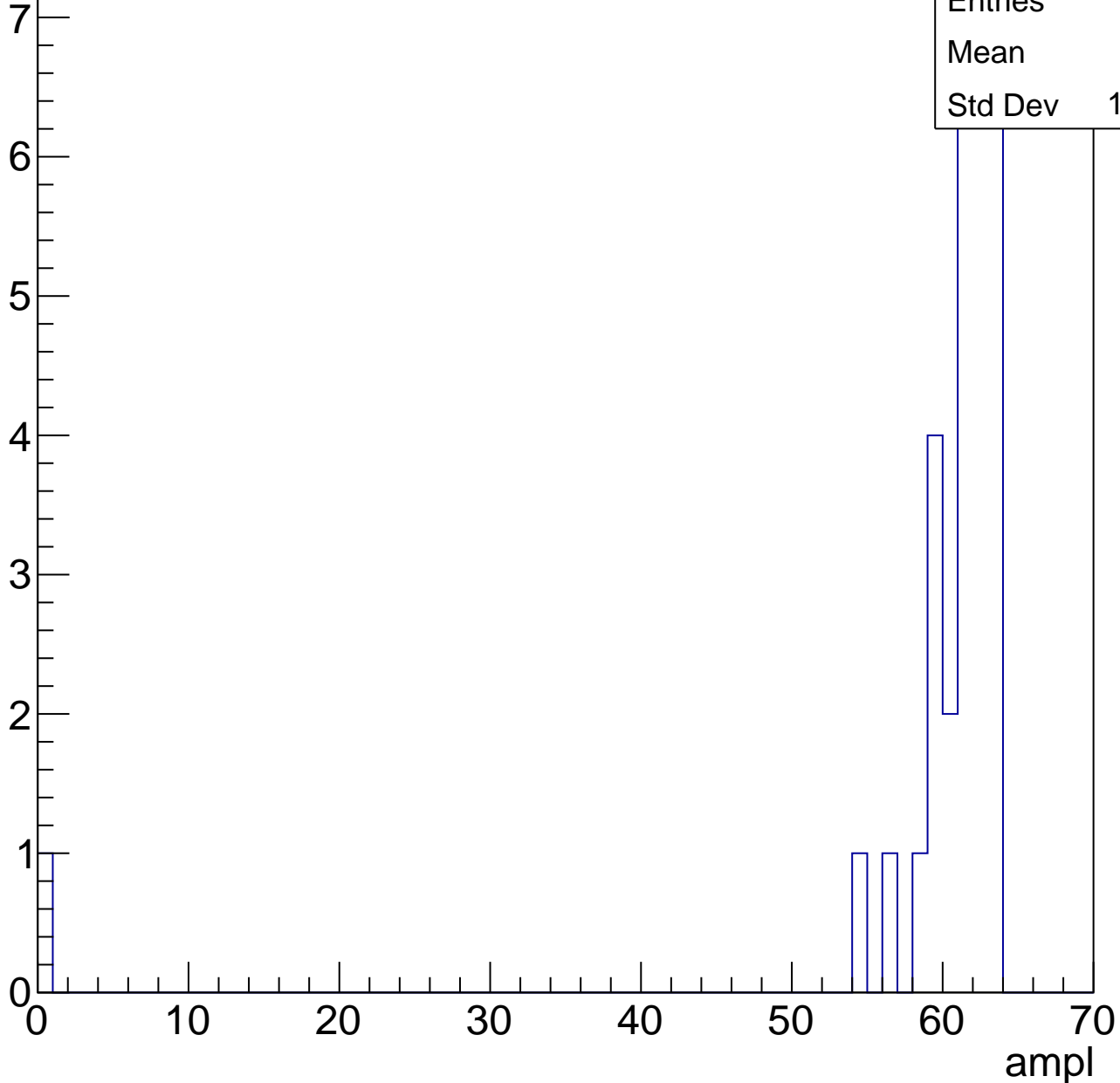


# B1L101S, U22-ch11, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	31
Mean	58.9
Std Dev	10.96



# B1L101S, U22-ch11, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U22-ch11, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

1  
0.8  
0.6  
0.4  
0.2  
0

0

10

20

30

40

50

60

70

ampl

Entries	1
Mean	24
Std Dev	0

# B1L101S, U22-ch12, adc0

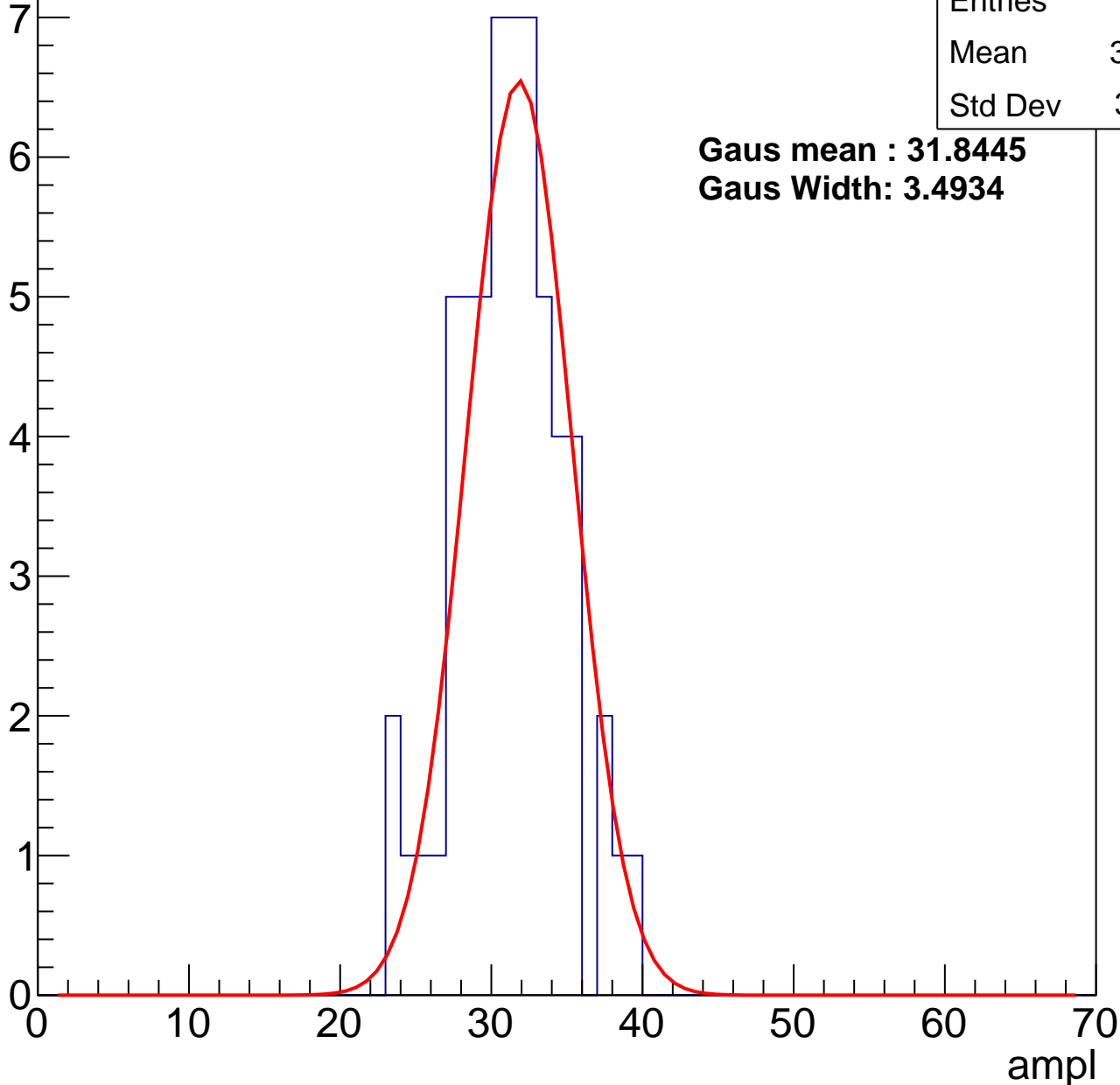
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	58
Mean	30.76
Std Dev	3.471

**Gaus mean : 31.8445**

**Gaus Width: 3.4934**



# B1L101S, U22-ch12, adc1

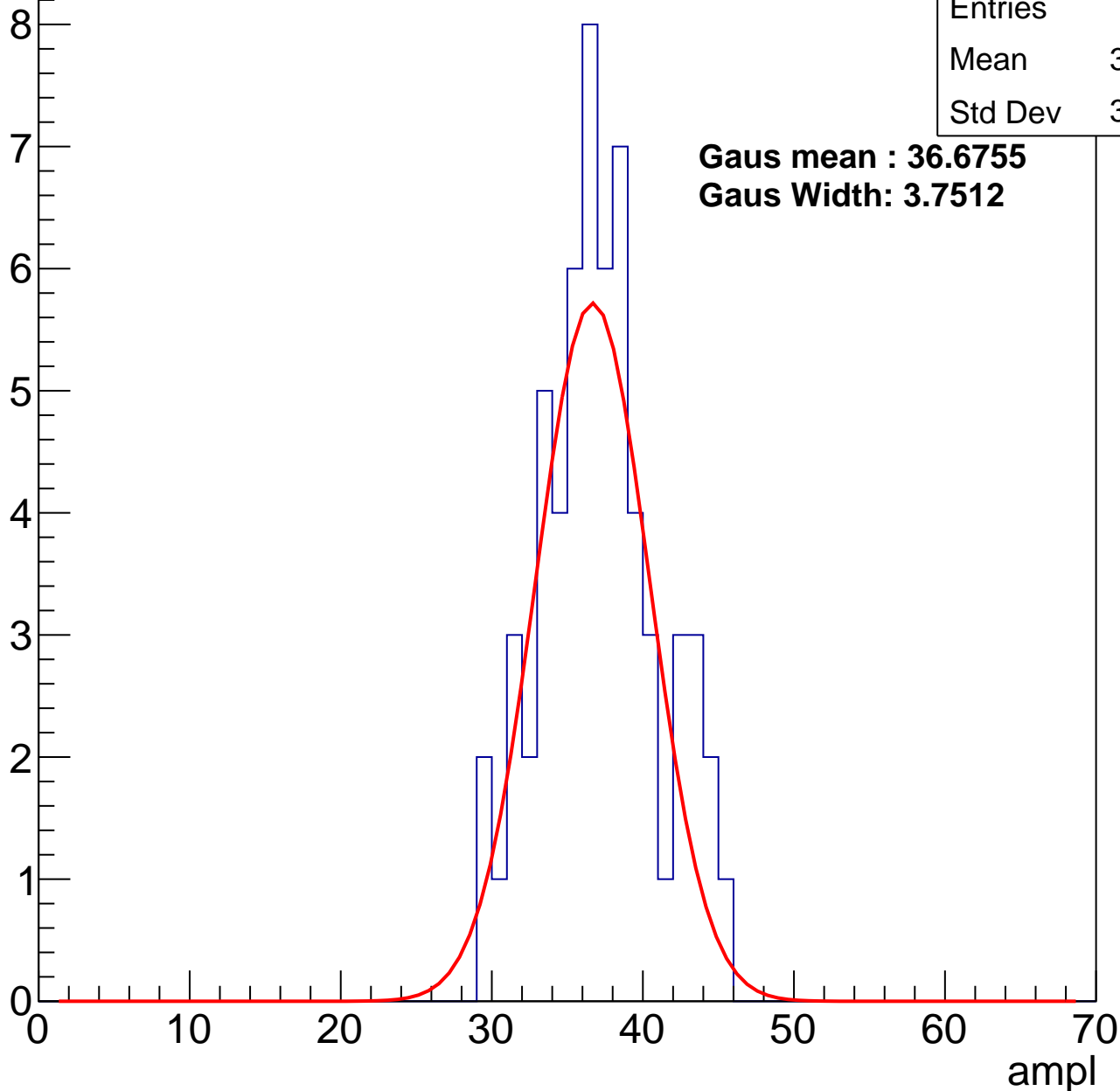
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	36.67
Std Dev	3.814

**Gaus mean : 36.6755**

**Gaus Width: 3.7512**



# B1L101S, U22-ch12, adc2

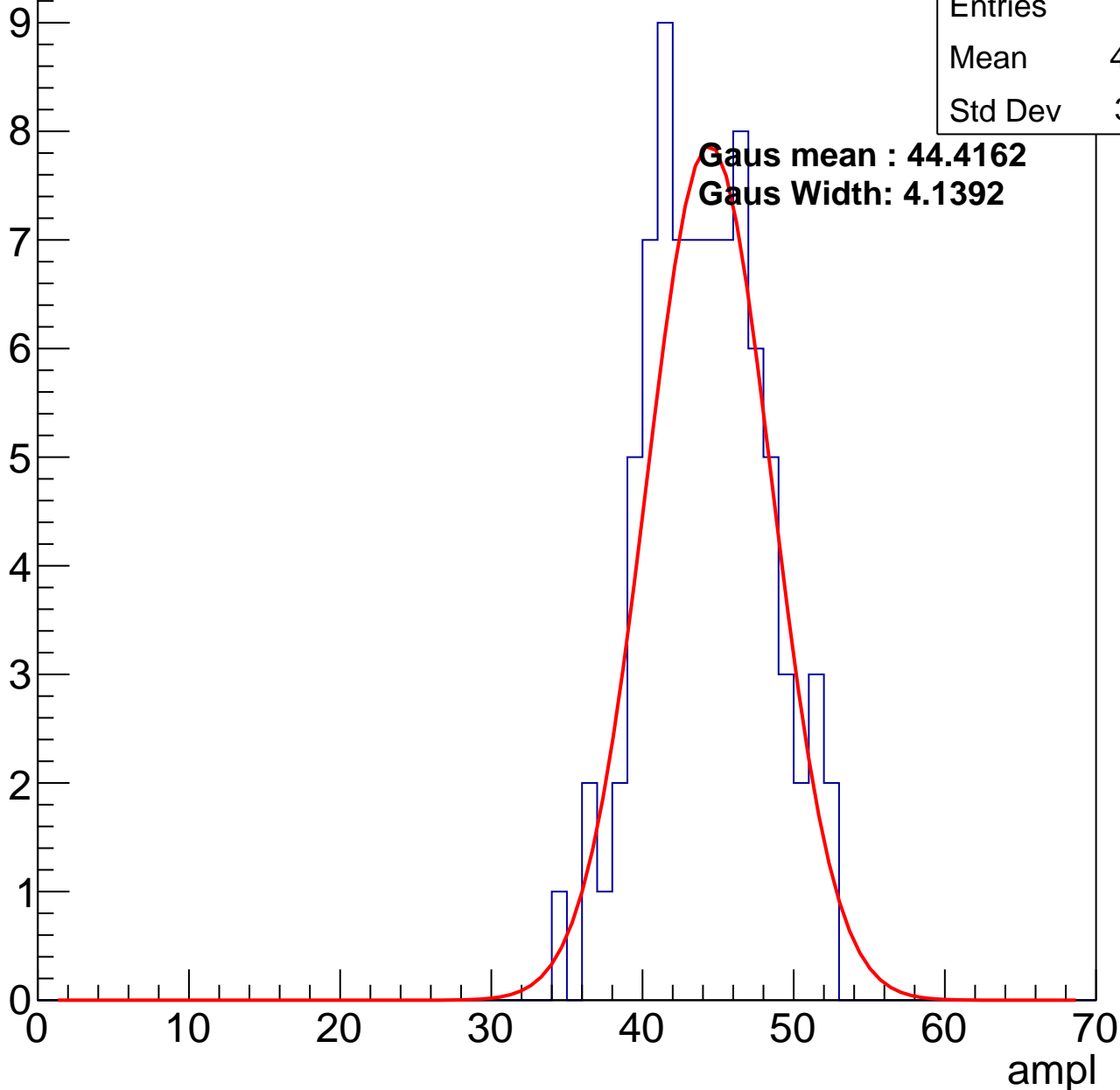
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	84
Mean	43.75
Std Dev	3.921

**Gaus mean : 44.4162**

**Gaus Width: 4.1392**

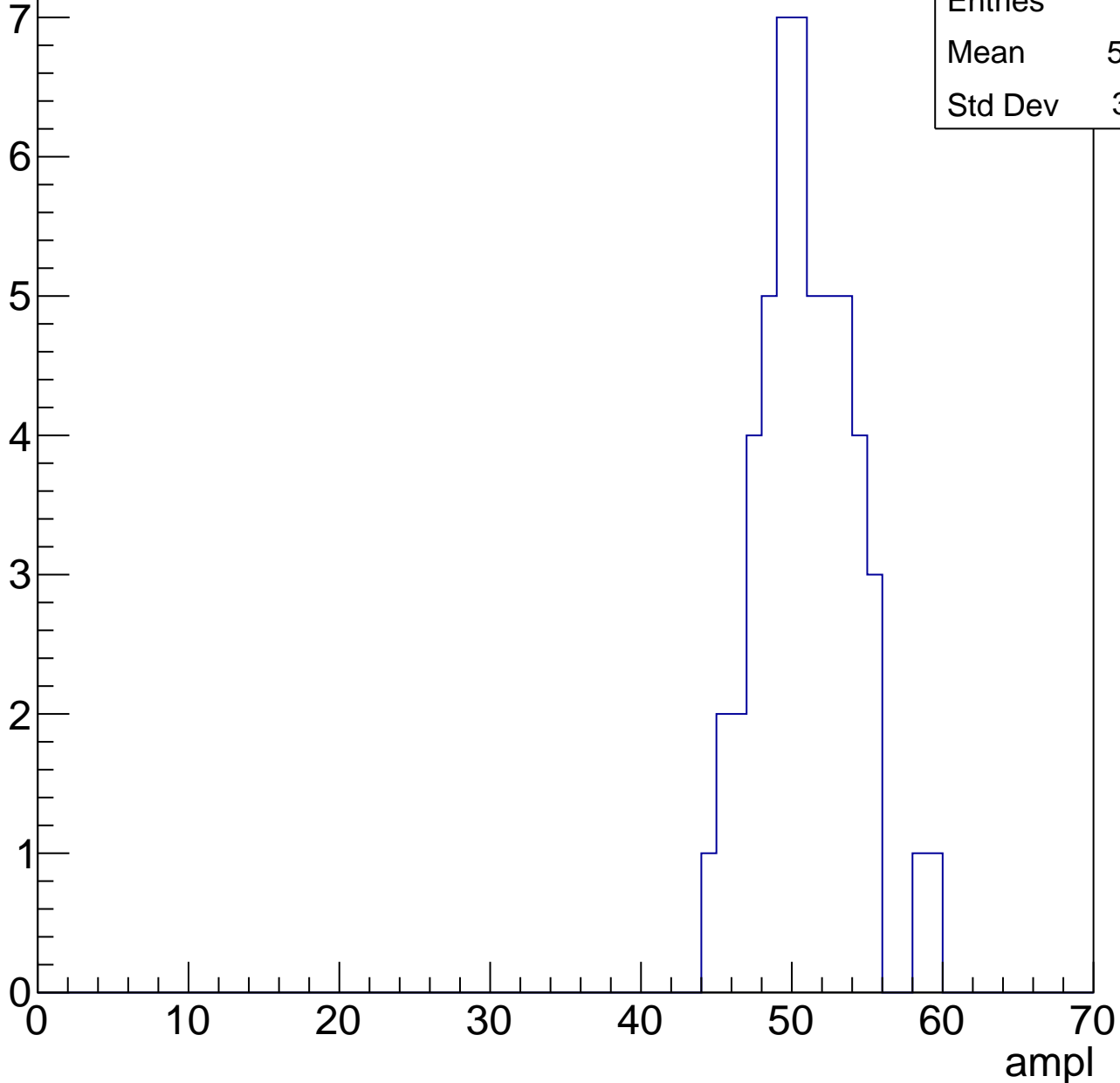


# B1L101S, U22-ch12, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	52
Mean	50.48
Std Dev	3.171

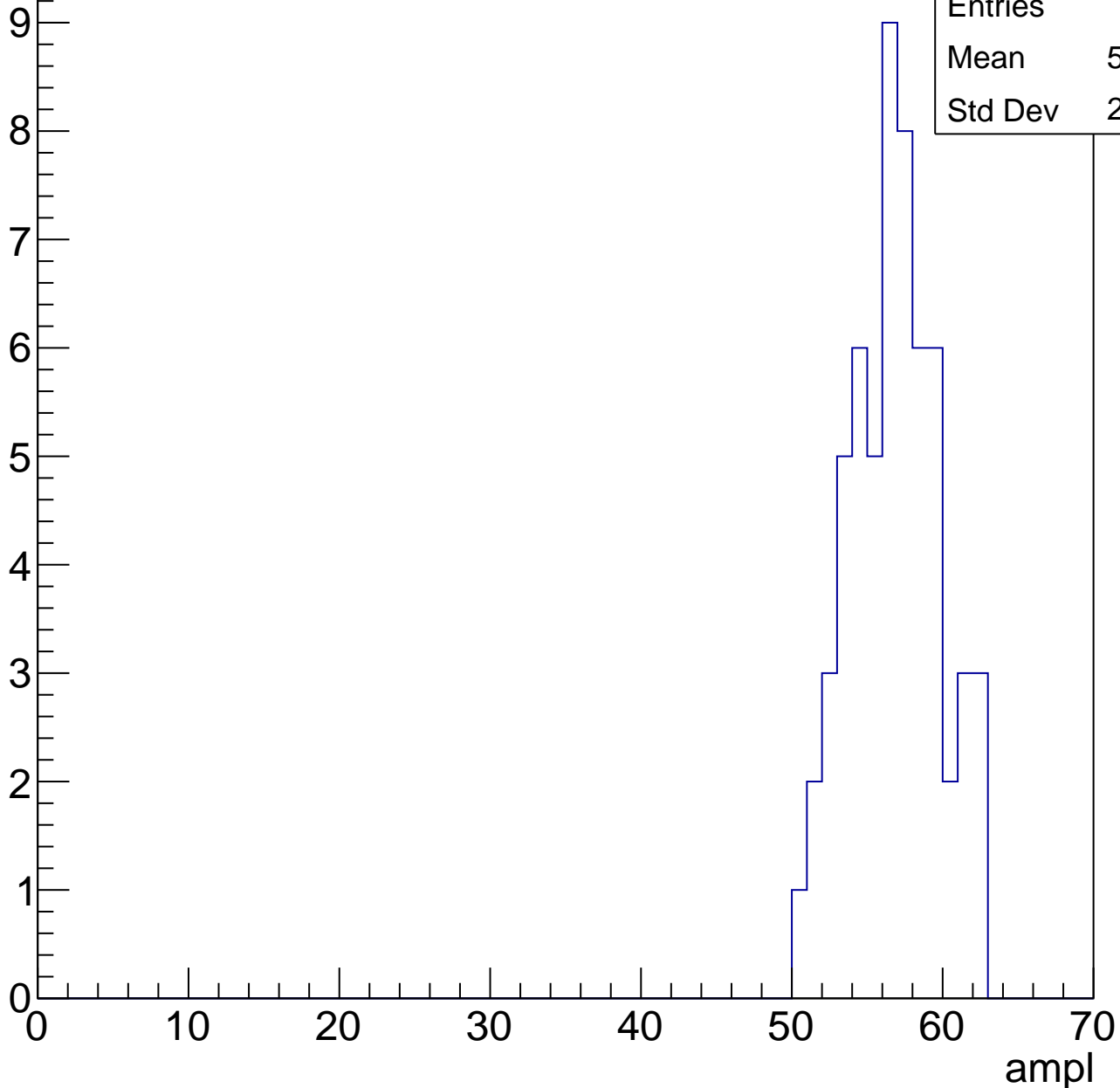


# B1L101S, U22-ch12, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	59
Mean	56.32
Std Dev	2.919

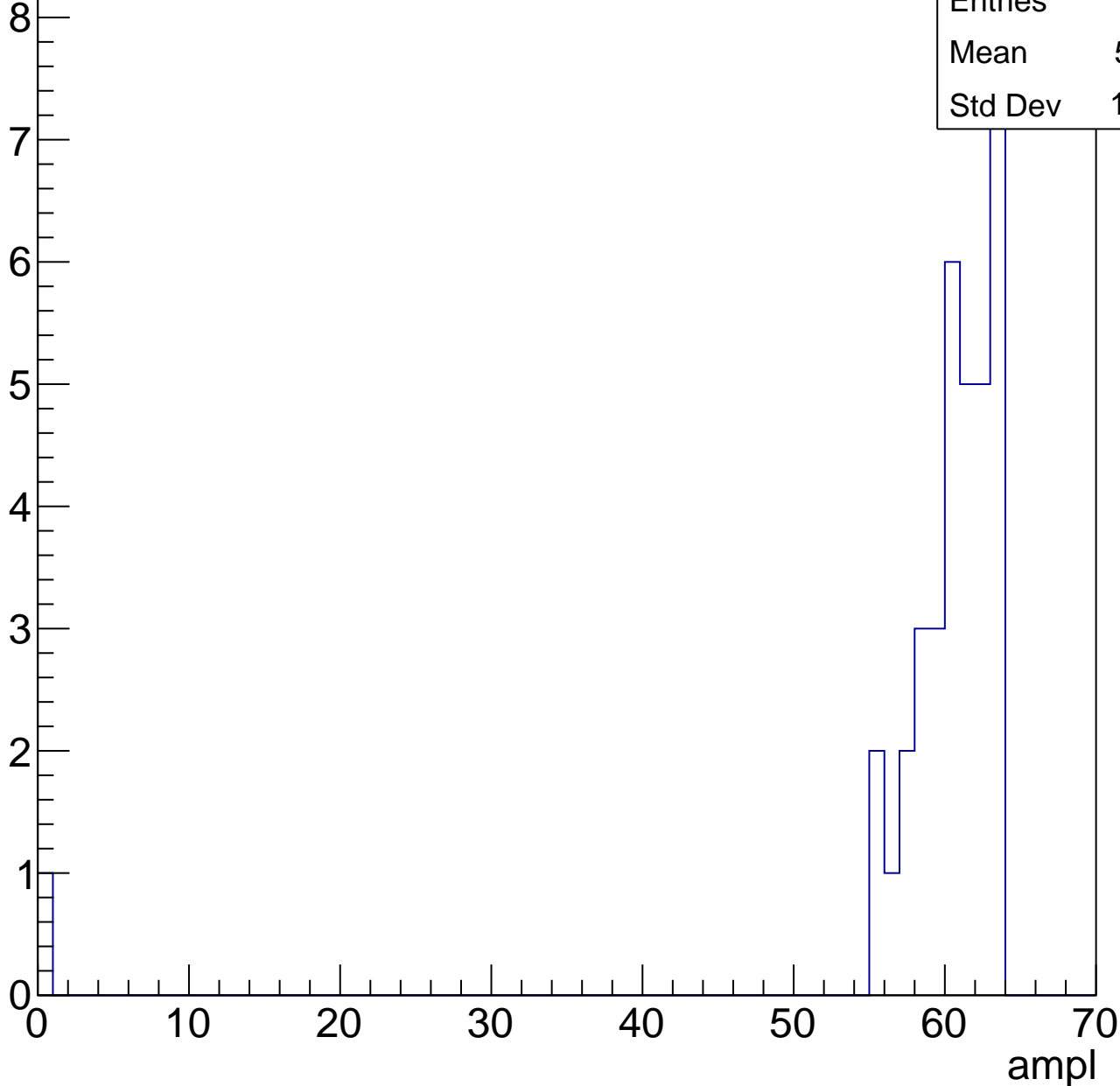


# B1L101S, U22-ch12, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	36
Mean	58.61
Std Dev	10.17



# B1L101S, U22-ch12, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

0

10

20

30

40

50

60

70

ampl

Entries	8
Mean	61.5
Std Dev	1.118



# B1L101S, U22-ch12, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	3
Mean	7.667
Std Dev	10.84

# B1L101S, U22-ch13, adc0

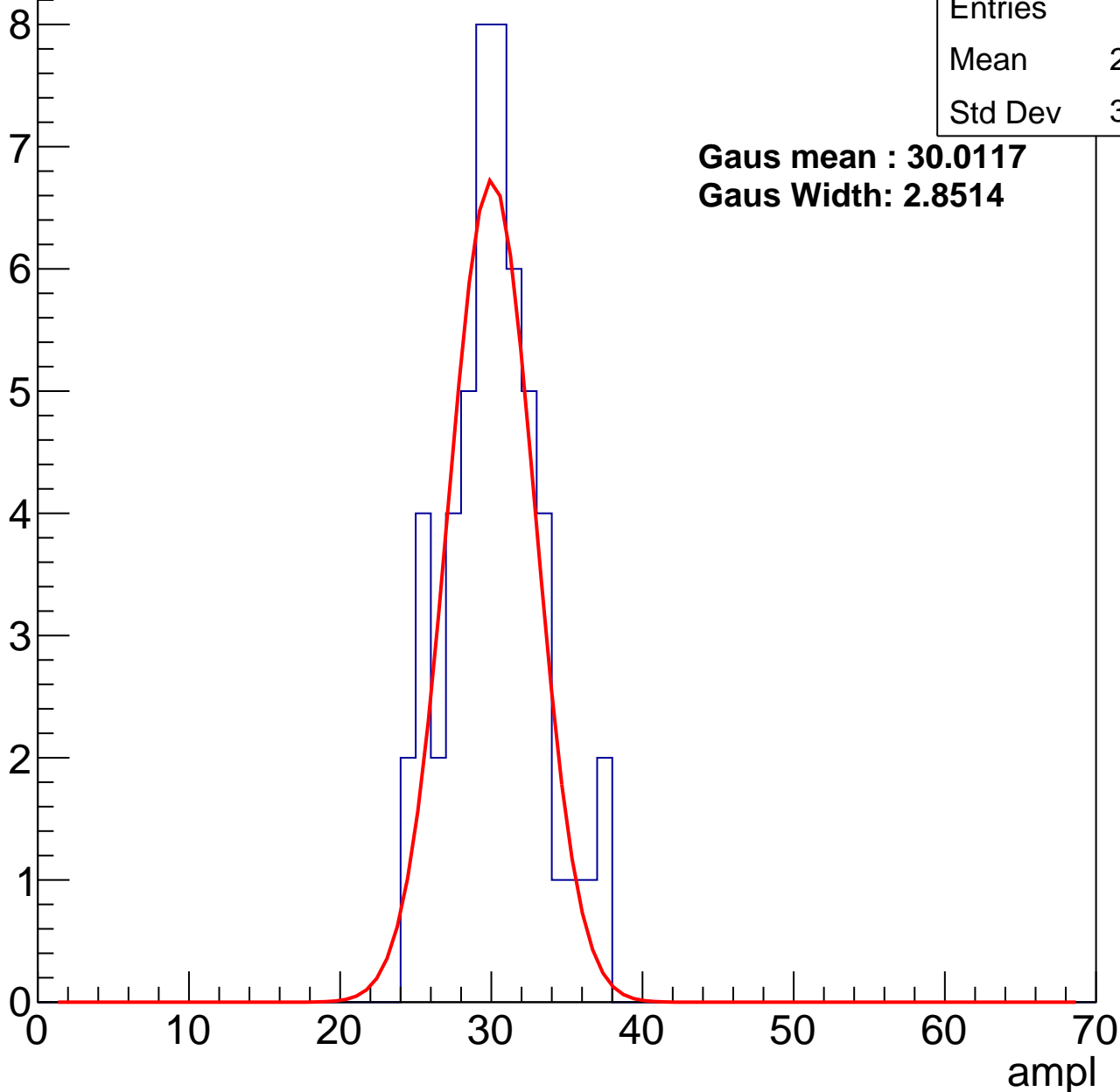
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	53
Mean	29.75
Std Dev	3.077

**Gaus mean : 30.0117**

**Gaus Width: 2.8514**



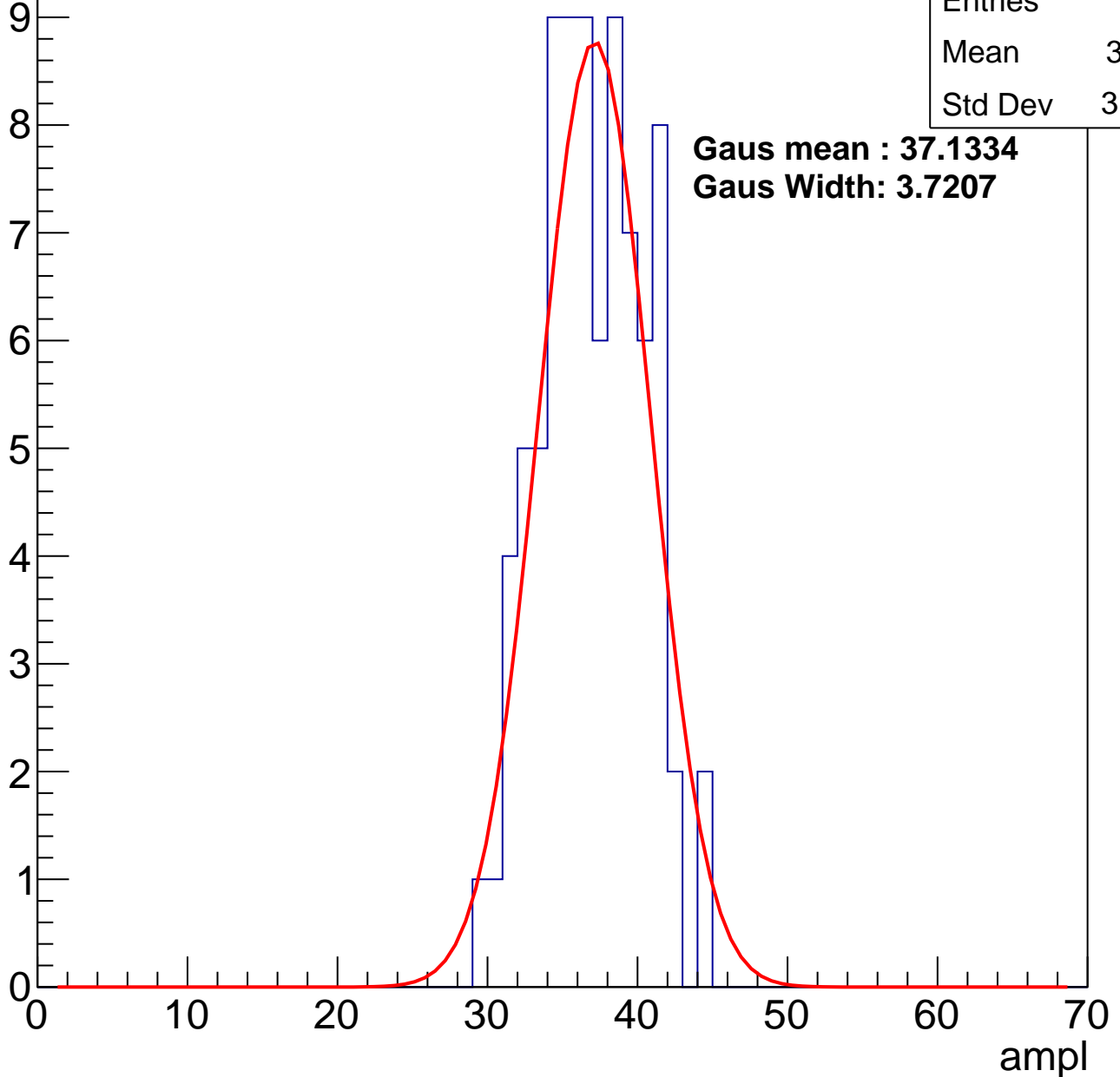
# B1L101S, U22-ch13, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	83
Mean	36.51
Std Dev	3.356

**Gaus mean : 37.1334**  
**Gaus Width: 3.7207**



# B1L101S, U22-ch13, adc2

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	72
Mean	44.4
Std Dev	3.239

**Gaus mean : 45.1975**

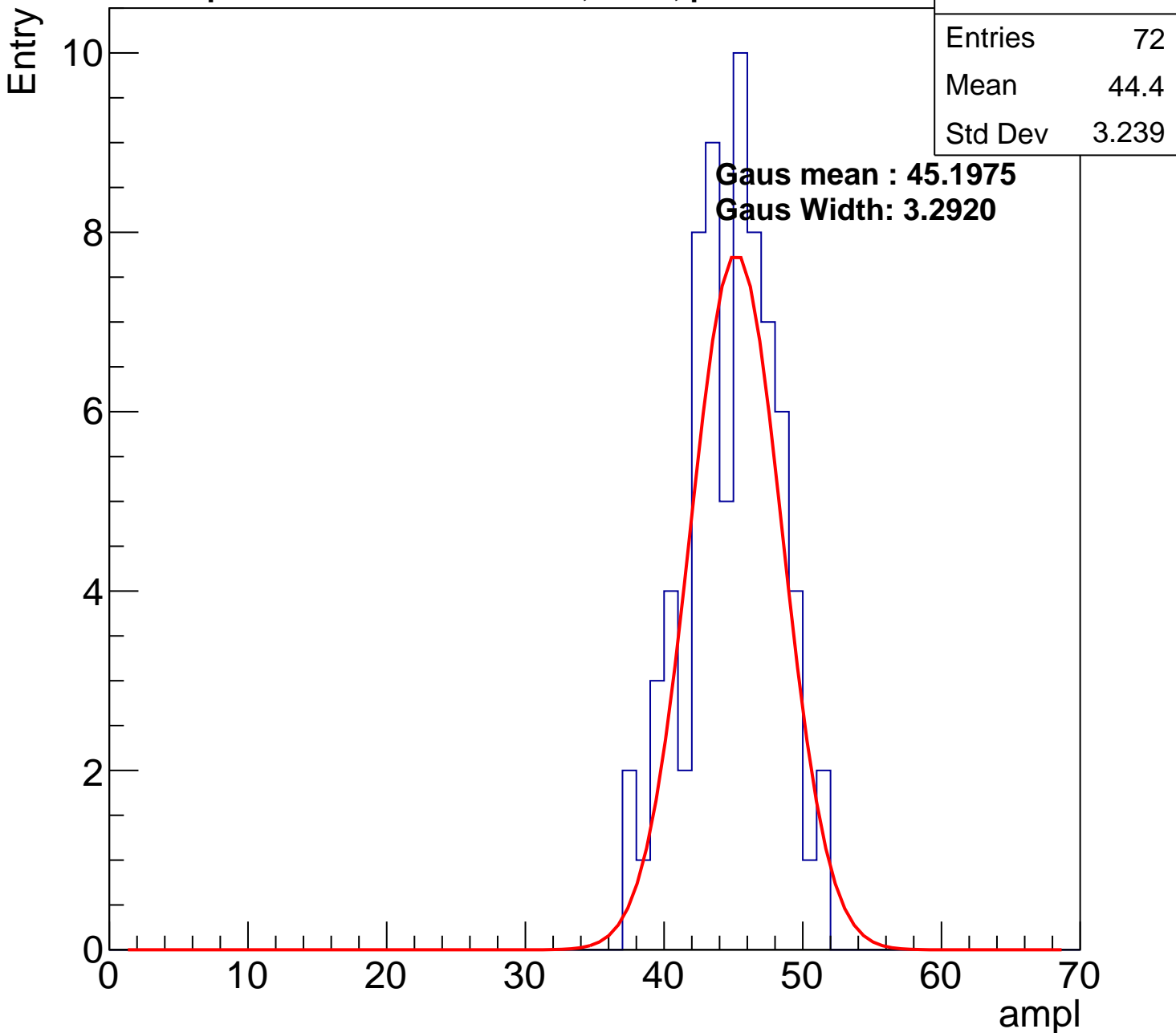
**Gaus Width: 3.2920**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

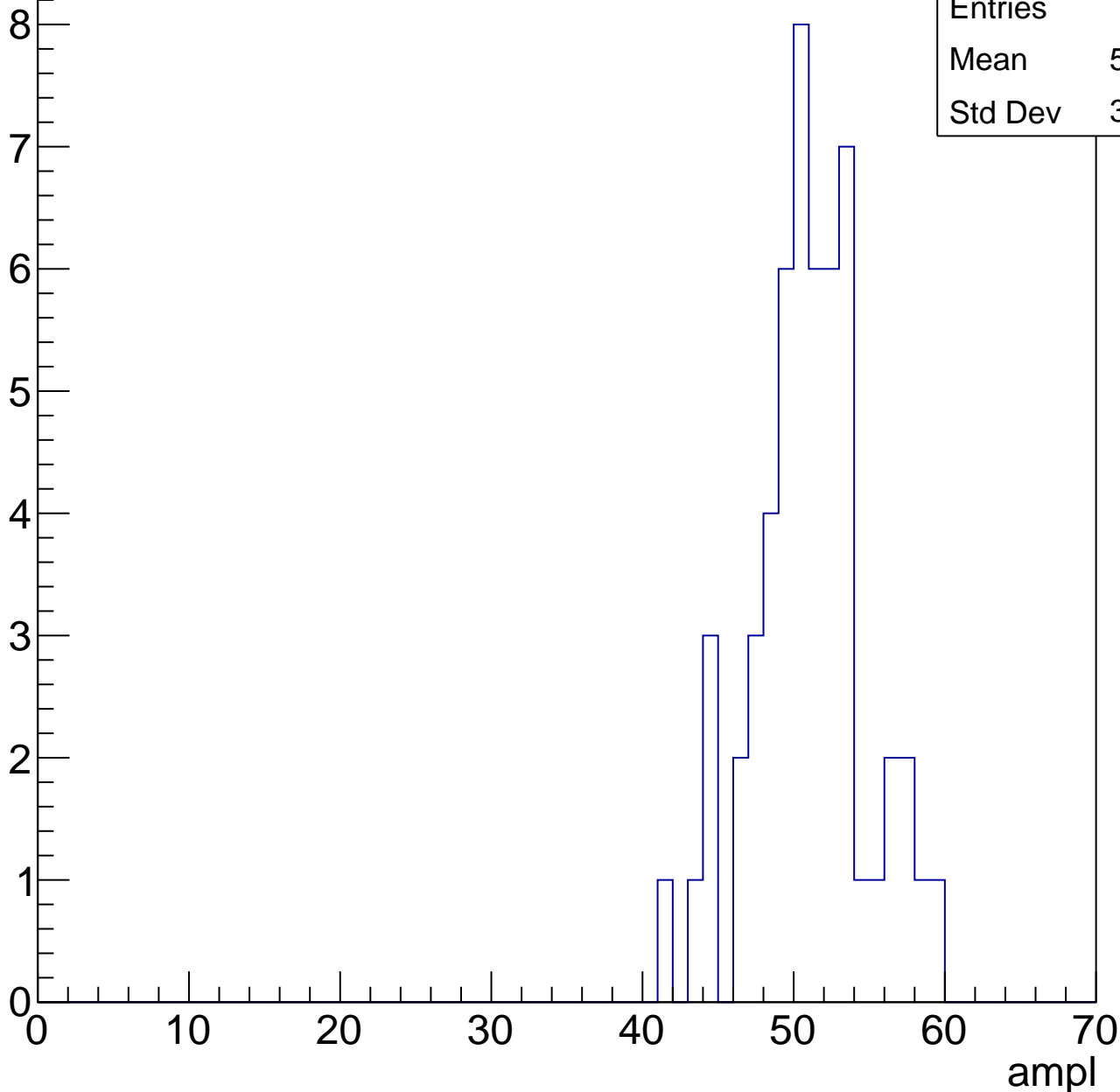


# B1L101S, U22-ch13, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	55
Mean	50.47
Std Dev	3.707

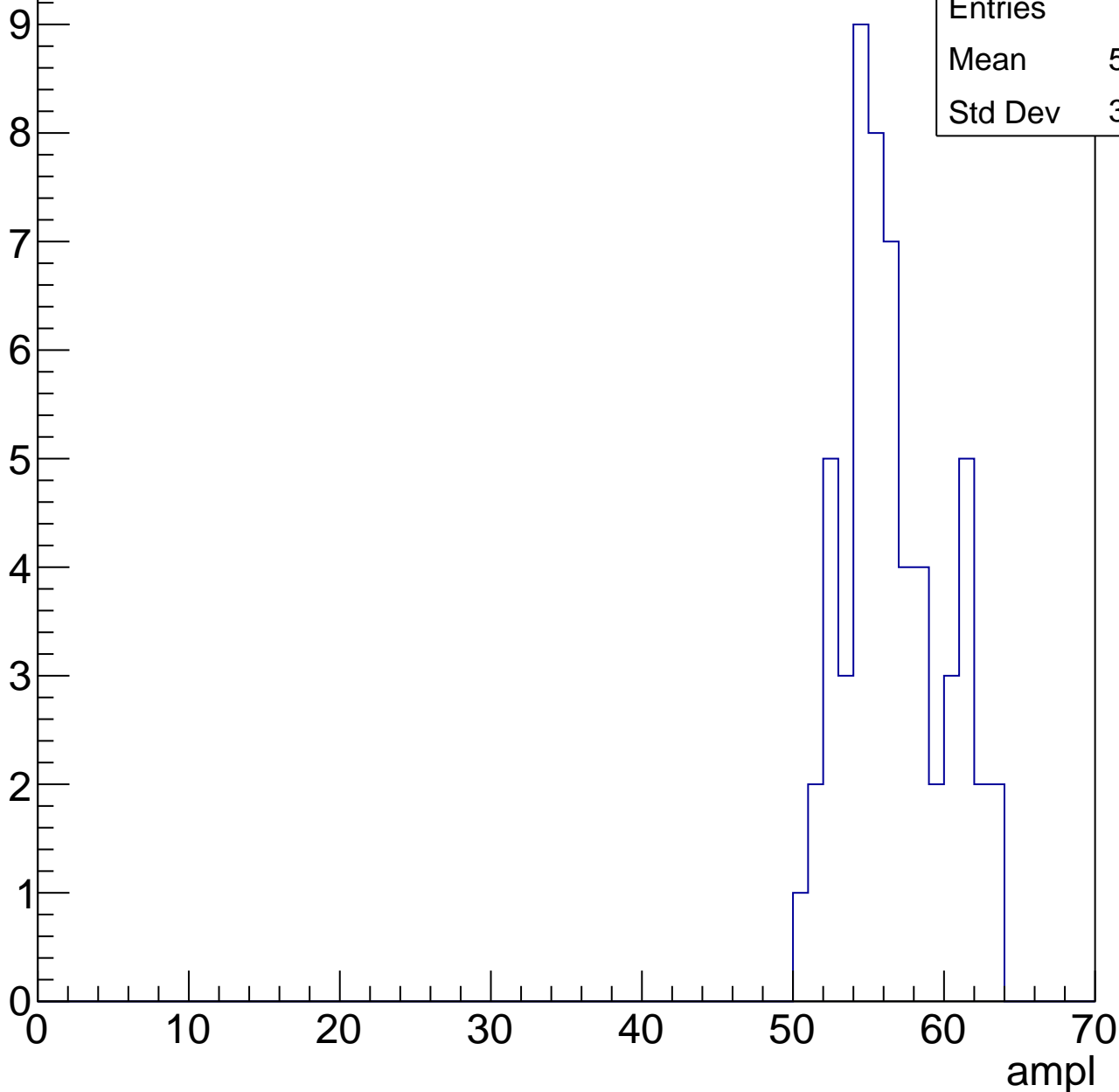


# B1L101S, U22-ch13, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	57
Mean	56.18
Std Dev	3.288

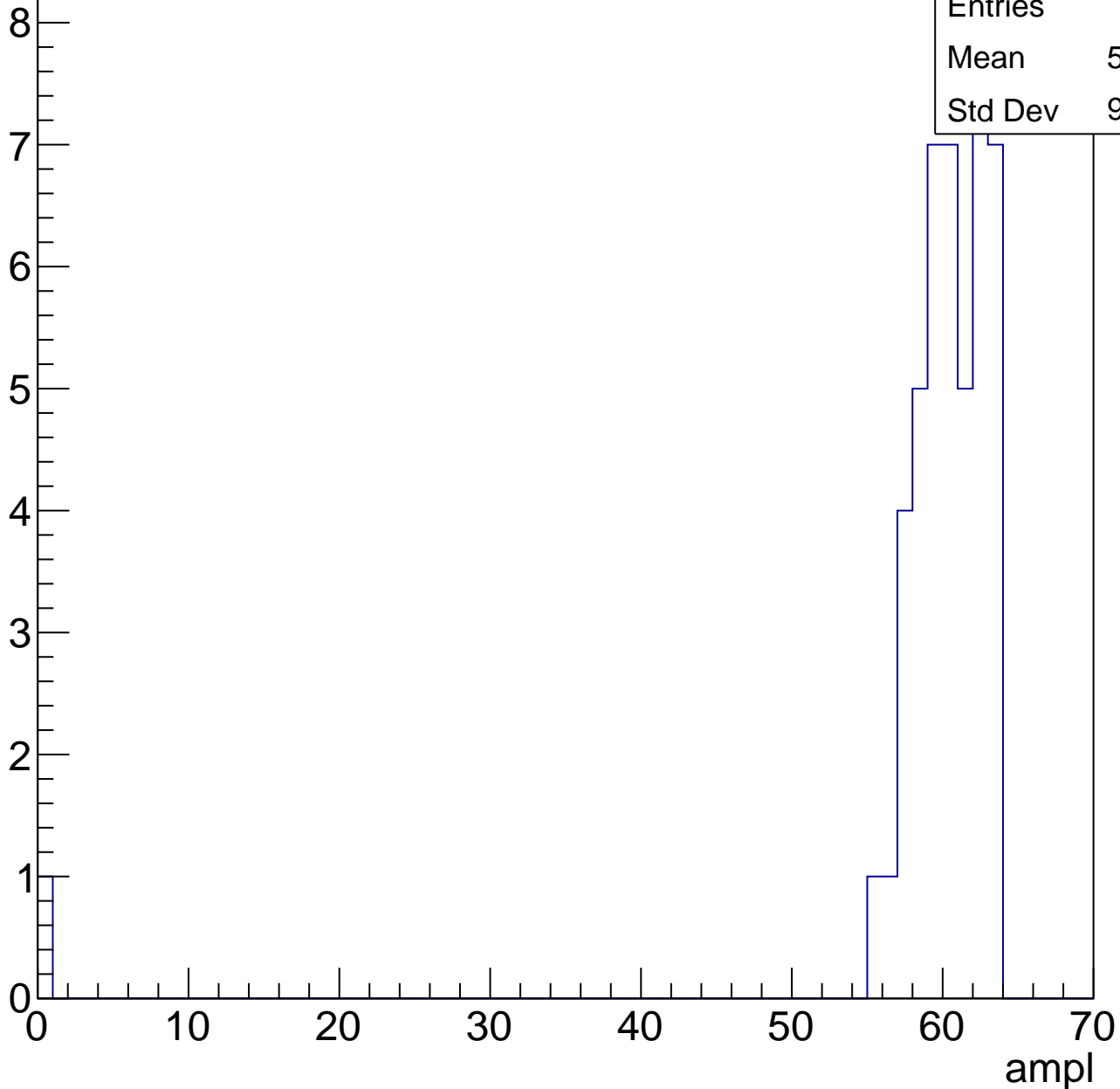


# B1L101S, U22-ch13, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

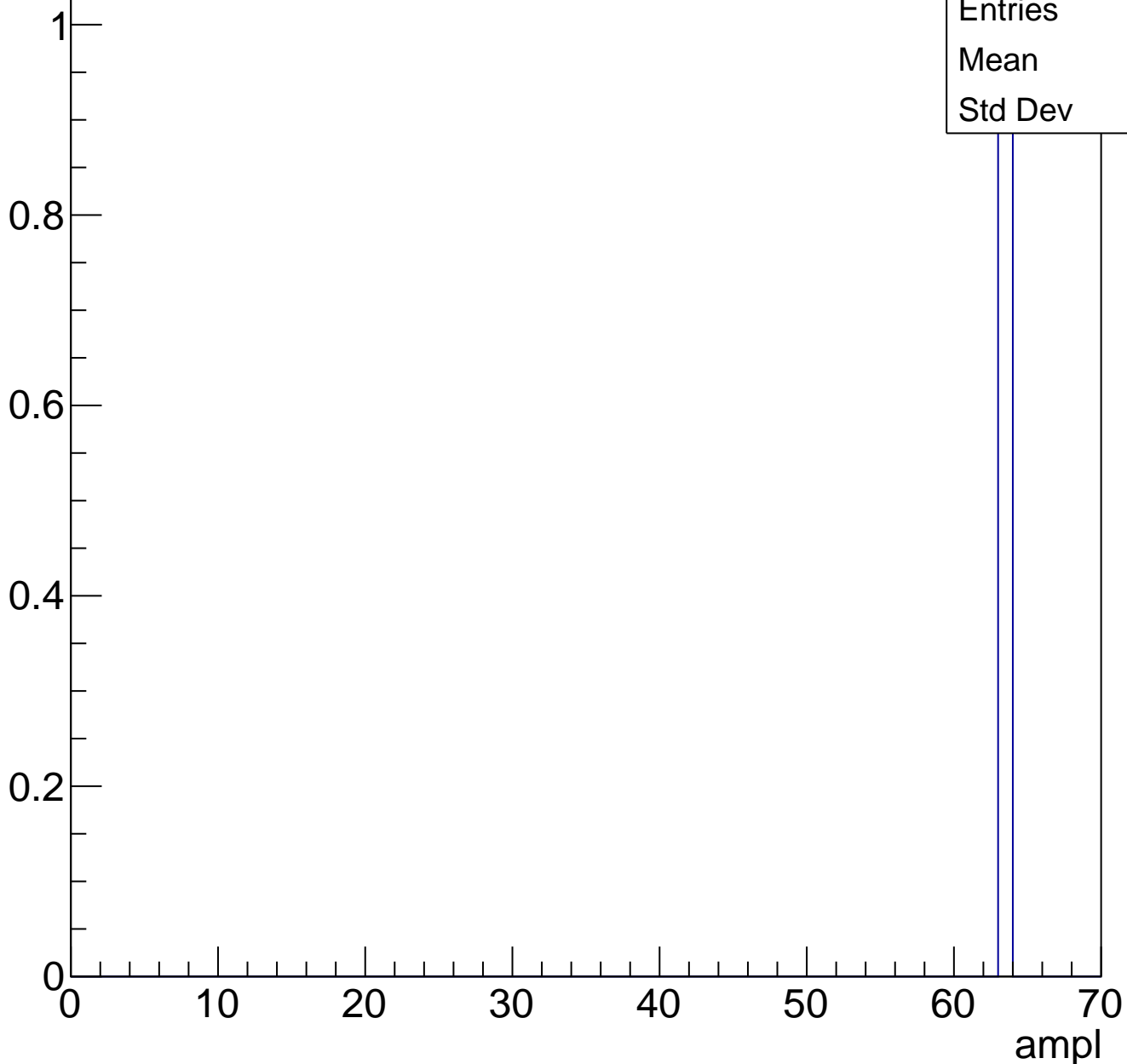
Entries	46
Mean	58.78
Std Dev	9.012



# B1L101S, U22-ch13, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U22-ch13, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L101S, U22-ch14, adc0

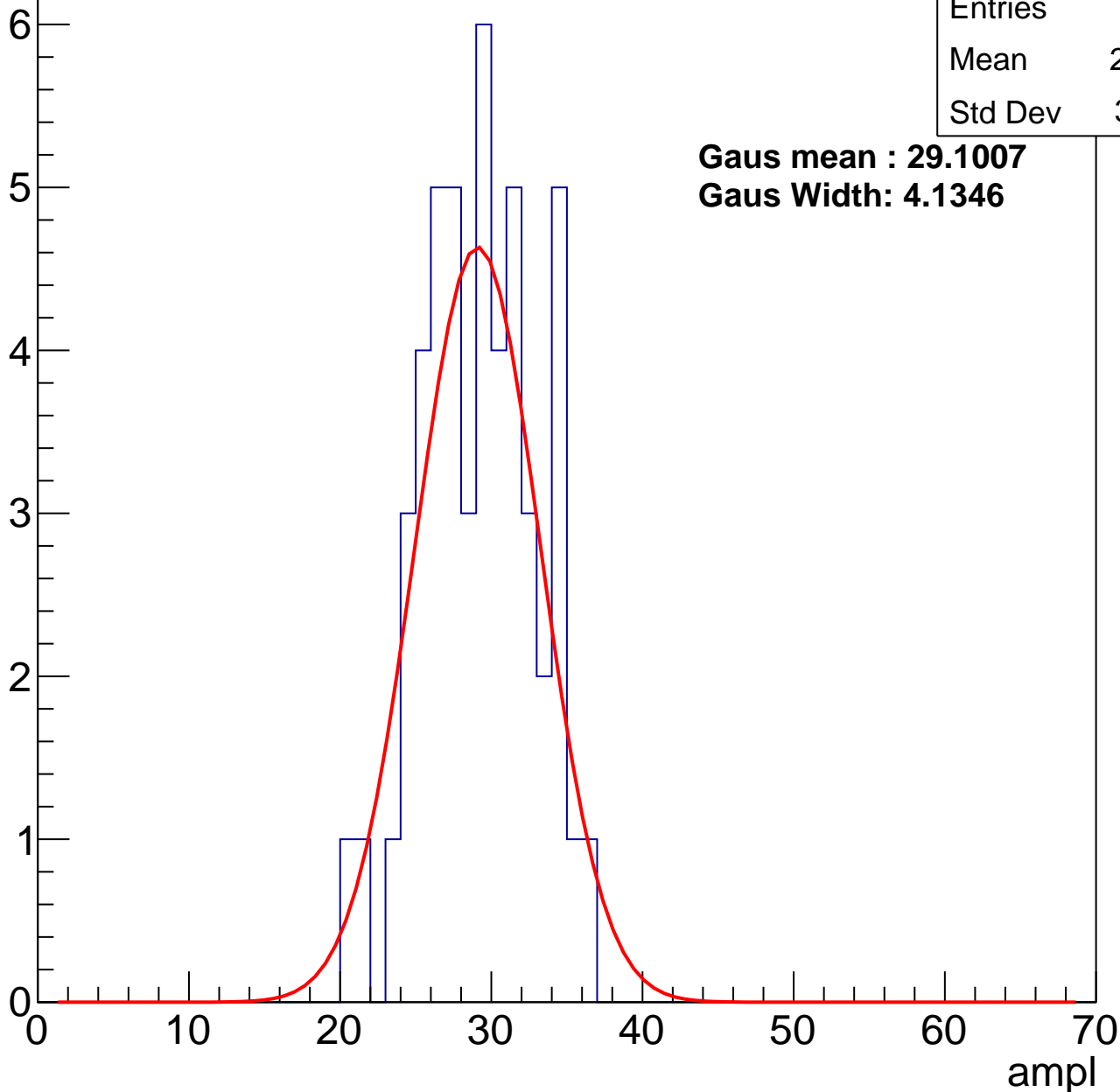
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	50
Mean	28.74
Std Dev	3.681

**Gaus mean : 29.1007**

**Gaus Width: 4.1346**



# B1L101S, U22-ch14, adc1

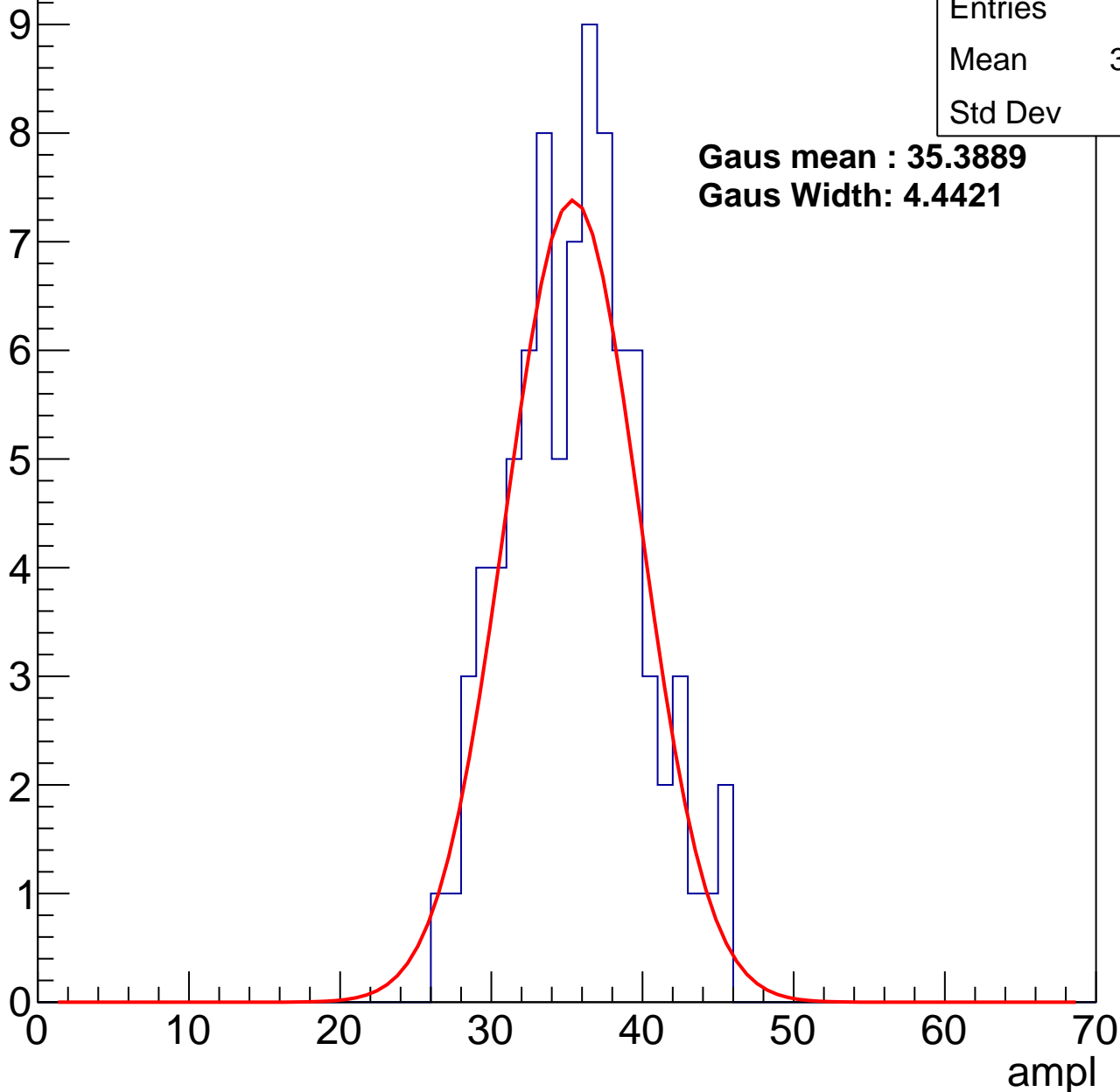
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	85
Mean	35.13
Std Dev	4.25

**Gaus mean : 35.3889**

**Gaus Width: 4.4421**



# B1L101S, U22-ch14, adc2

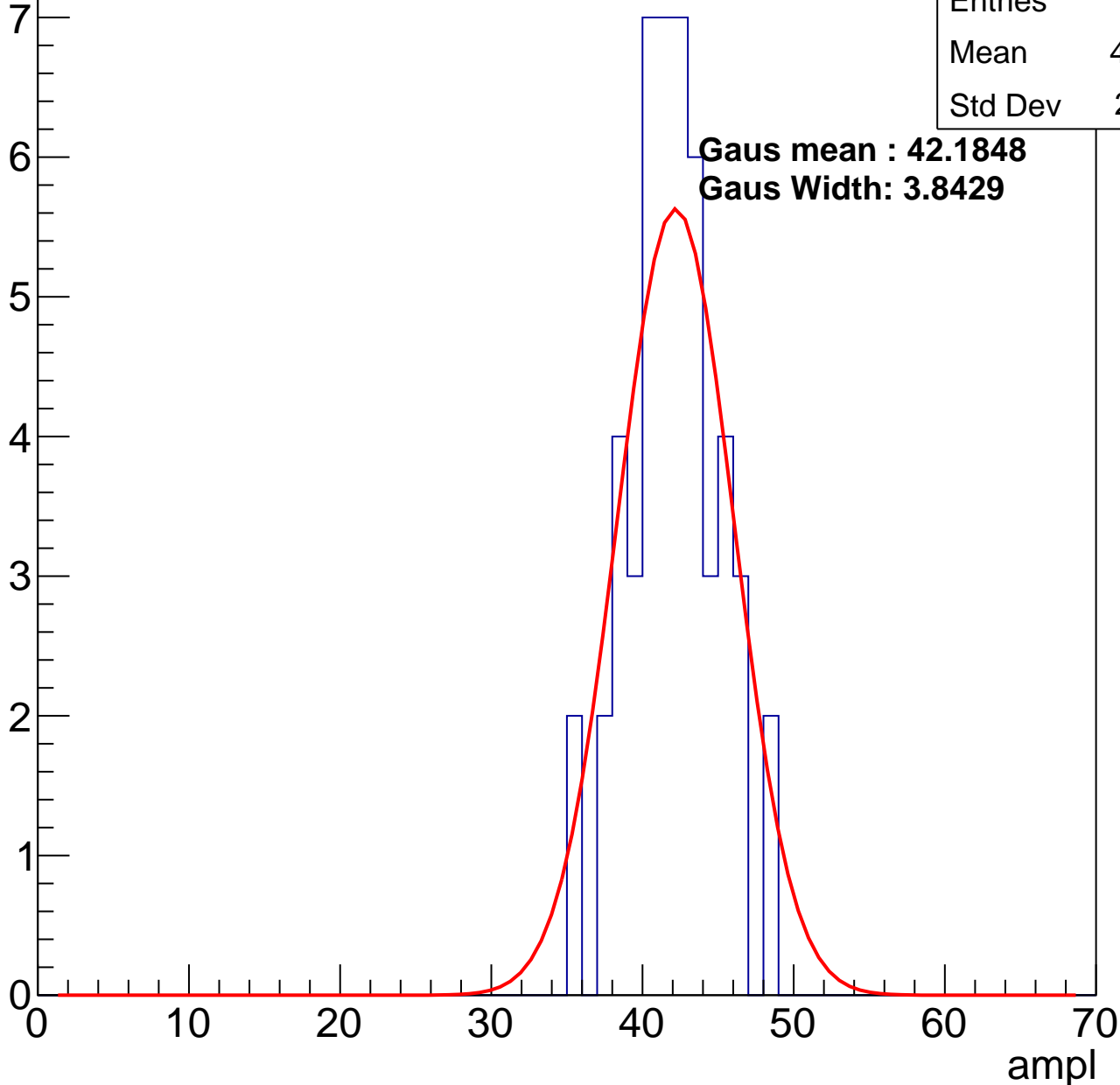
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	50
Mean	41.56
Std Dev	2.961

**Gaus mean : 42.1848**

**Gaus Width: 3.8429**

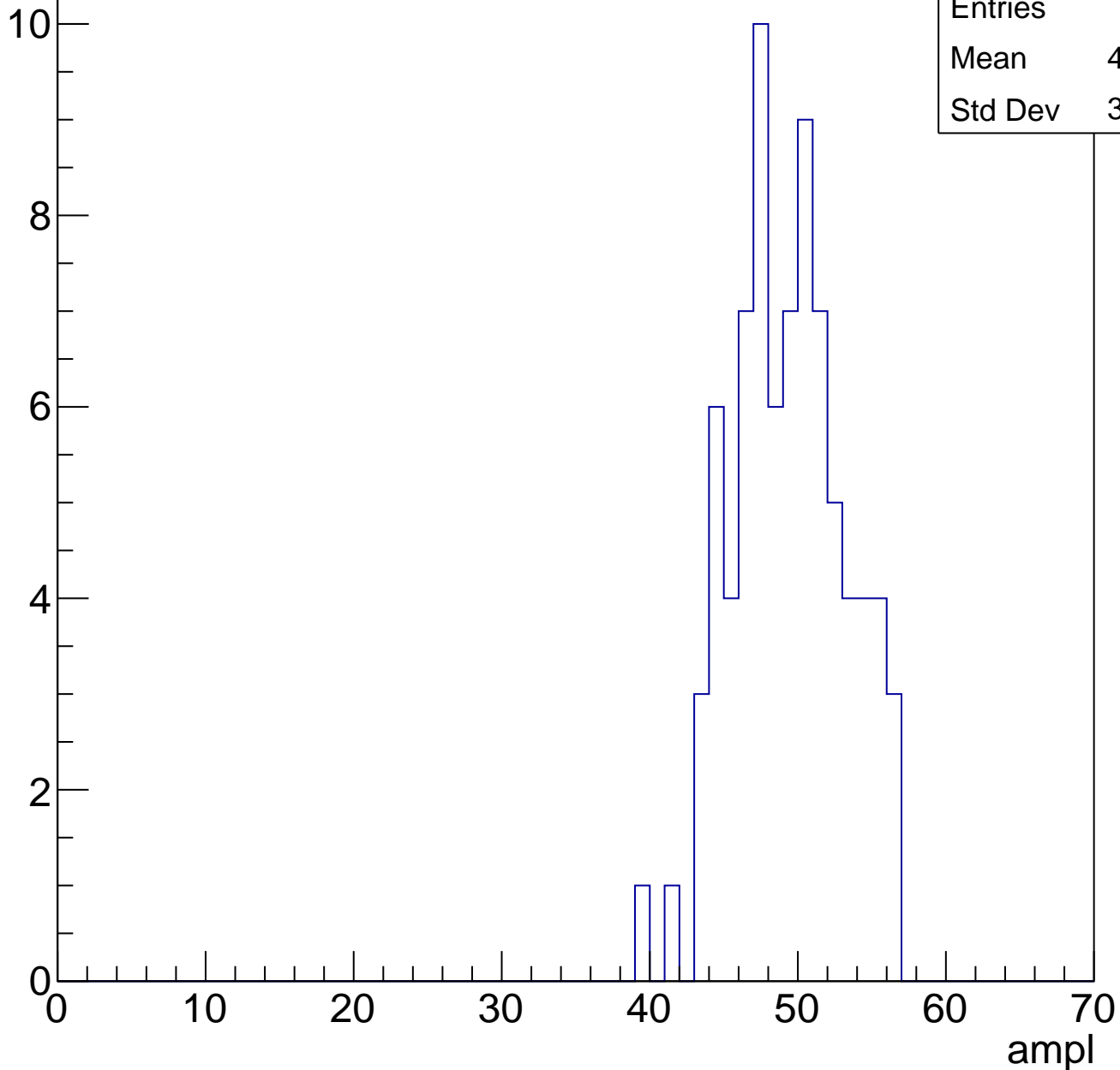


# B1L101S, U22-ch14, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	81
Mean	48.88
Std Dev	3.736

Entry

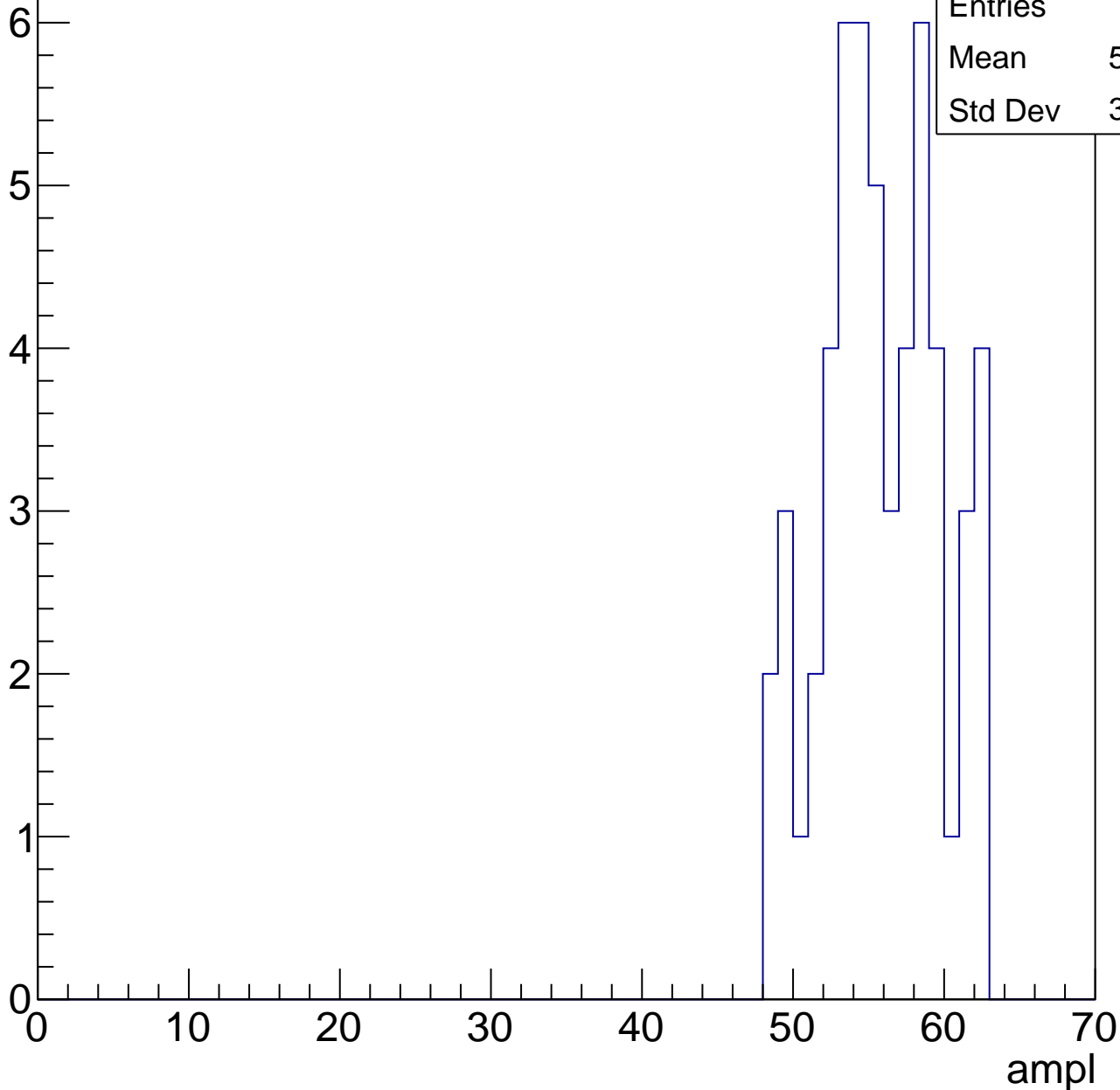


# B1L101S, U22-ch14, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

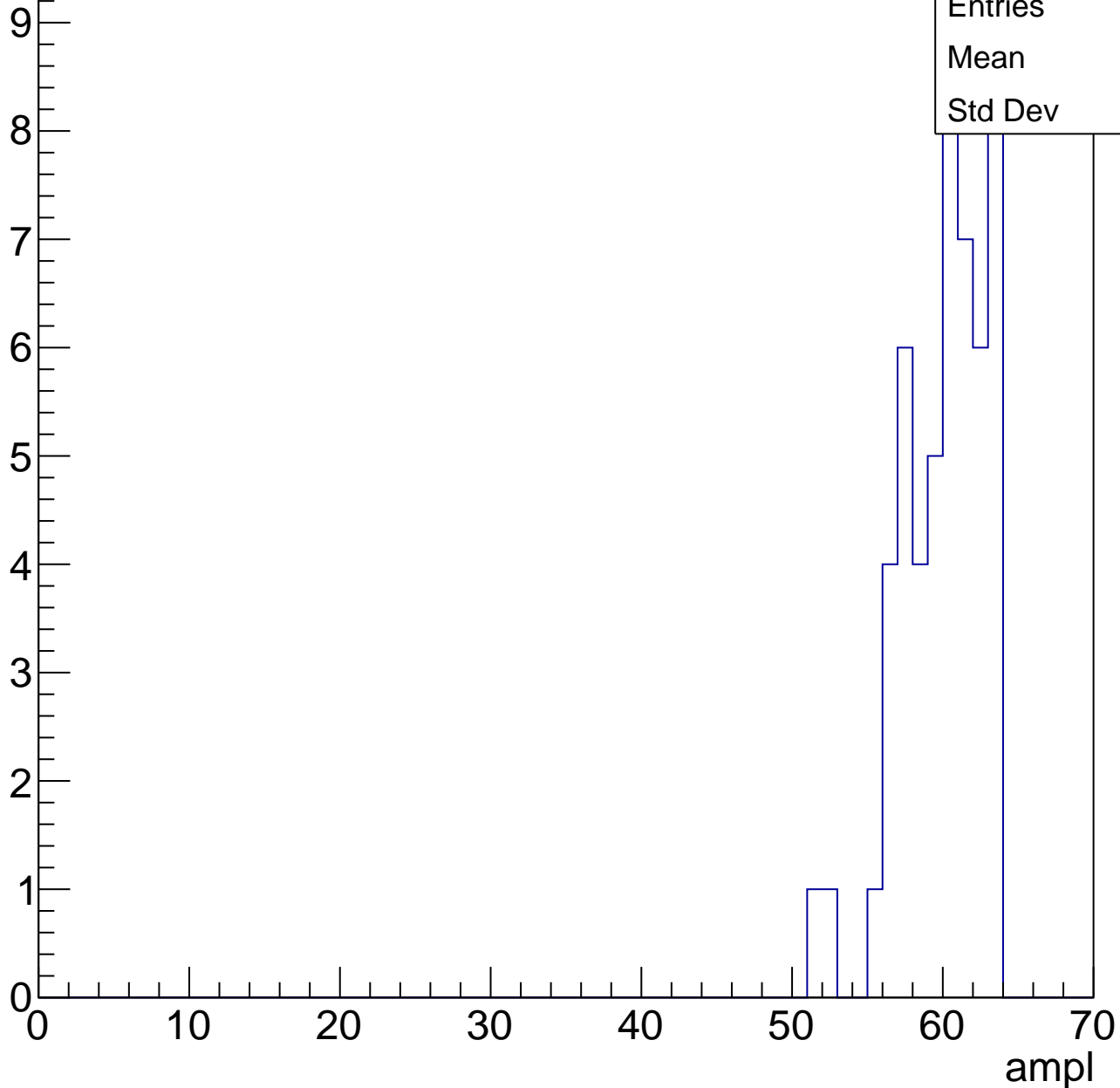
Entries	54
Mean	55.39
Std Dev	3.817



# B1L101S, U22-ch14, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

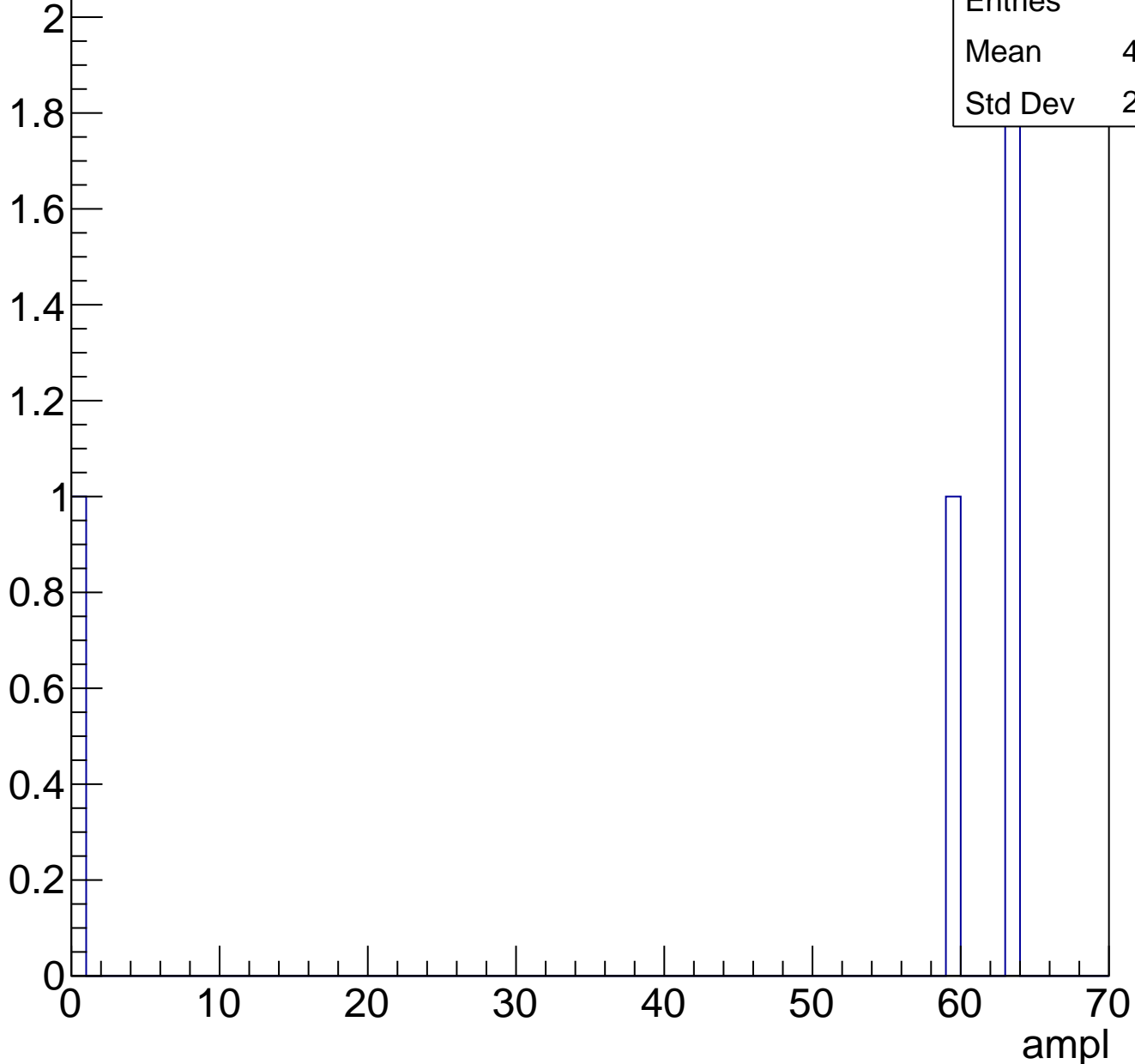
Entry



# B1L101S, U22-ch14, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U22-ch14, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	3
Mean	6.667
Std Dev	9.428

# B1L101S, U22-ch15, adc0

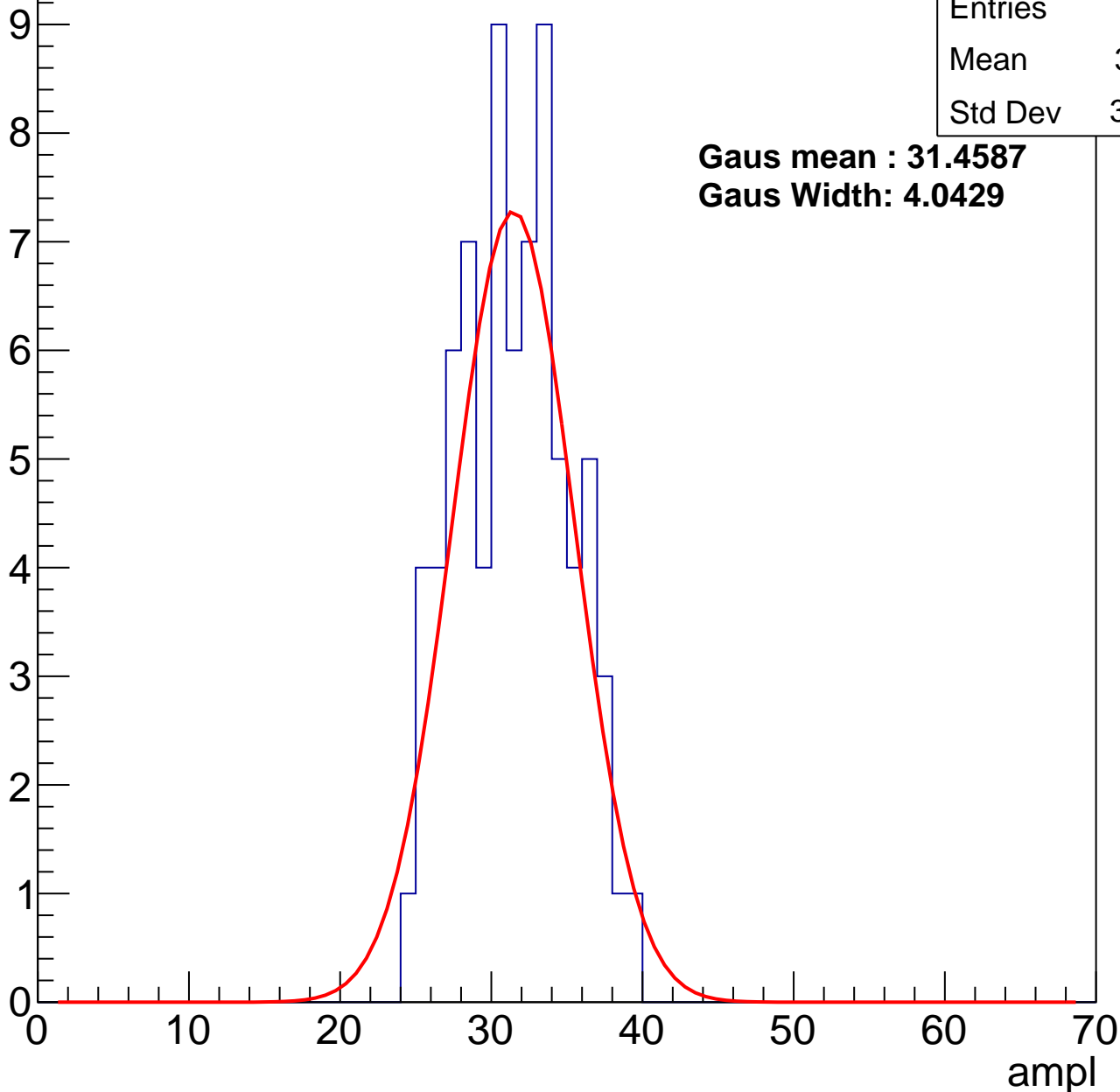
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	76
Mean	31.01
Std Dev	3.582

**Gaus mean : 31.4587**

**Gaus Width: 4.0429**



# B1L101S, U22-ch15, adc1

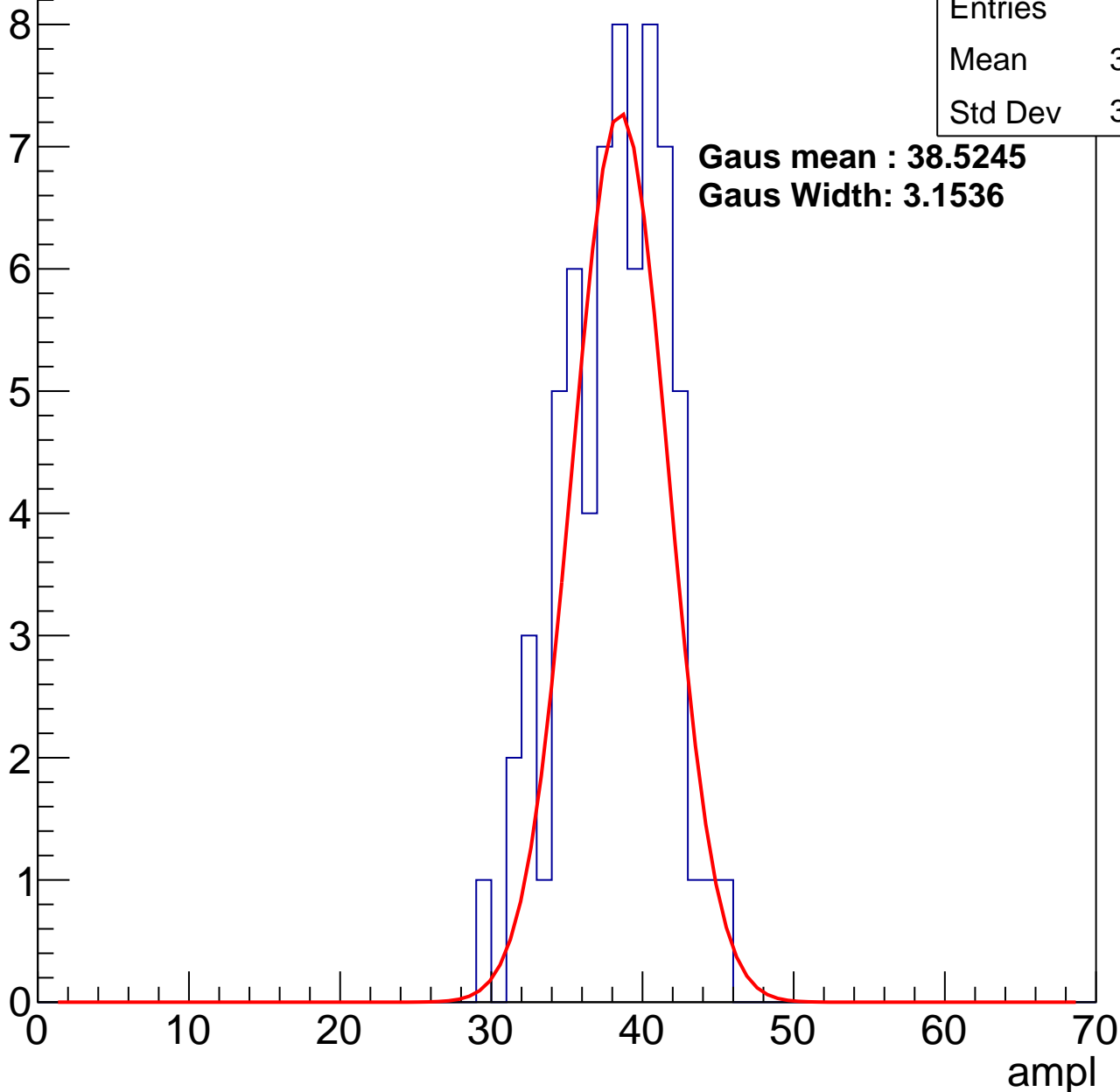
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	66
Mean	37.73
Std Dev	3.382

**Gaus mean : 38.5245**

**Gaus Width: 3.1536**



# B1L101S, U22-ch15, adc2

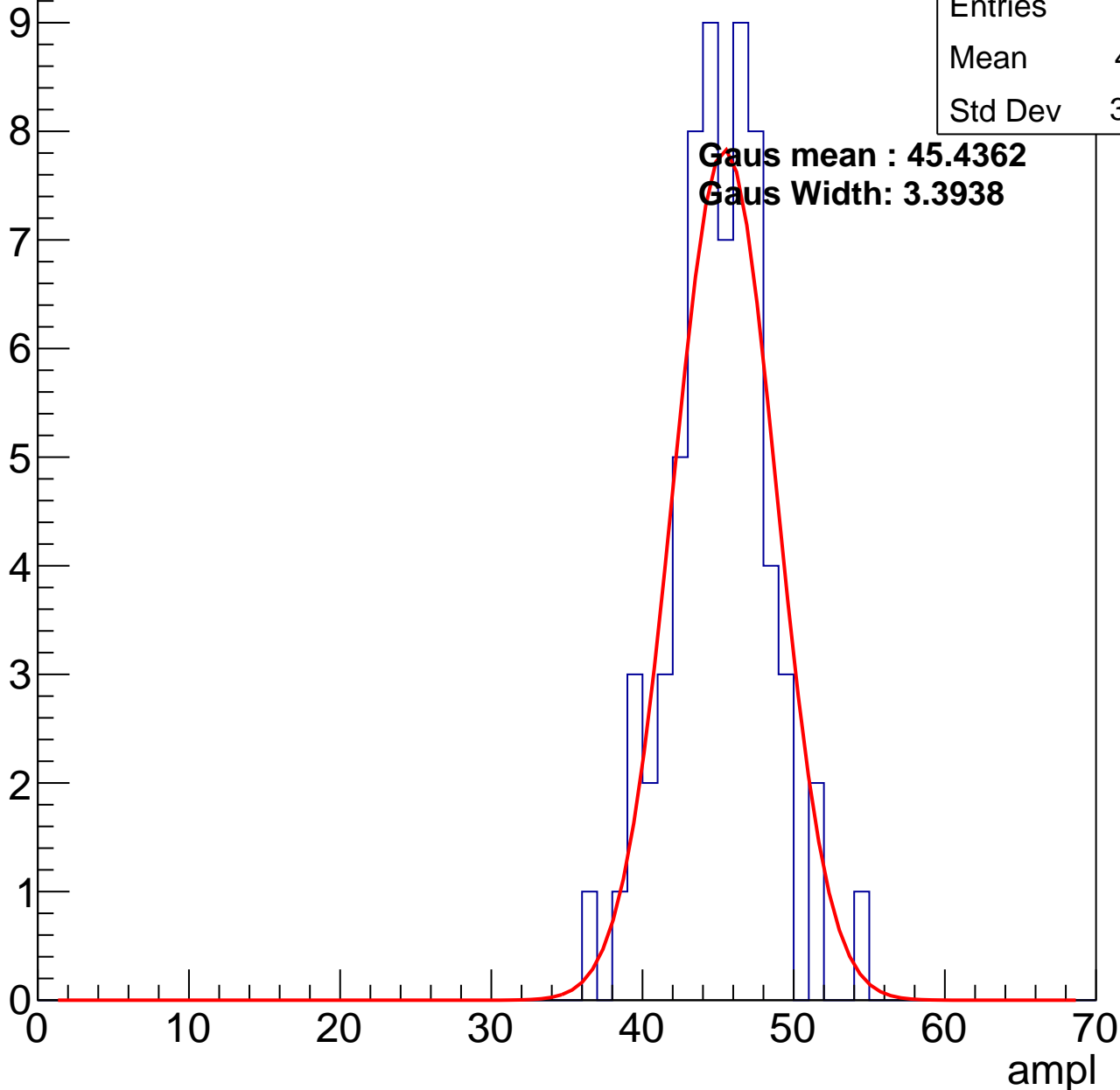
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	66
Mean	44.61
Std Dev	3.233

**Gaus mean : 45.4362**

**Gaus Width: 3.3938**

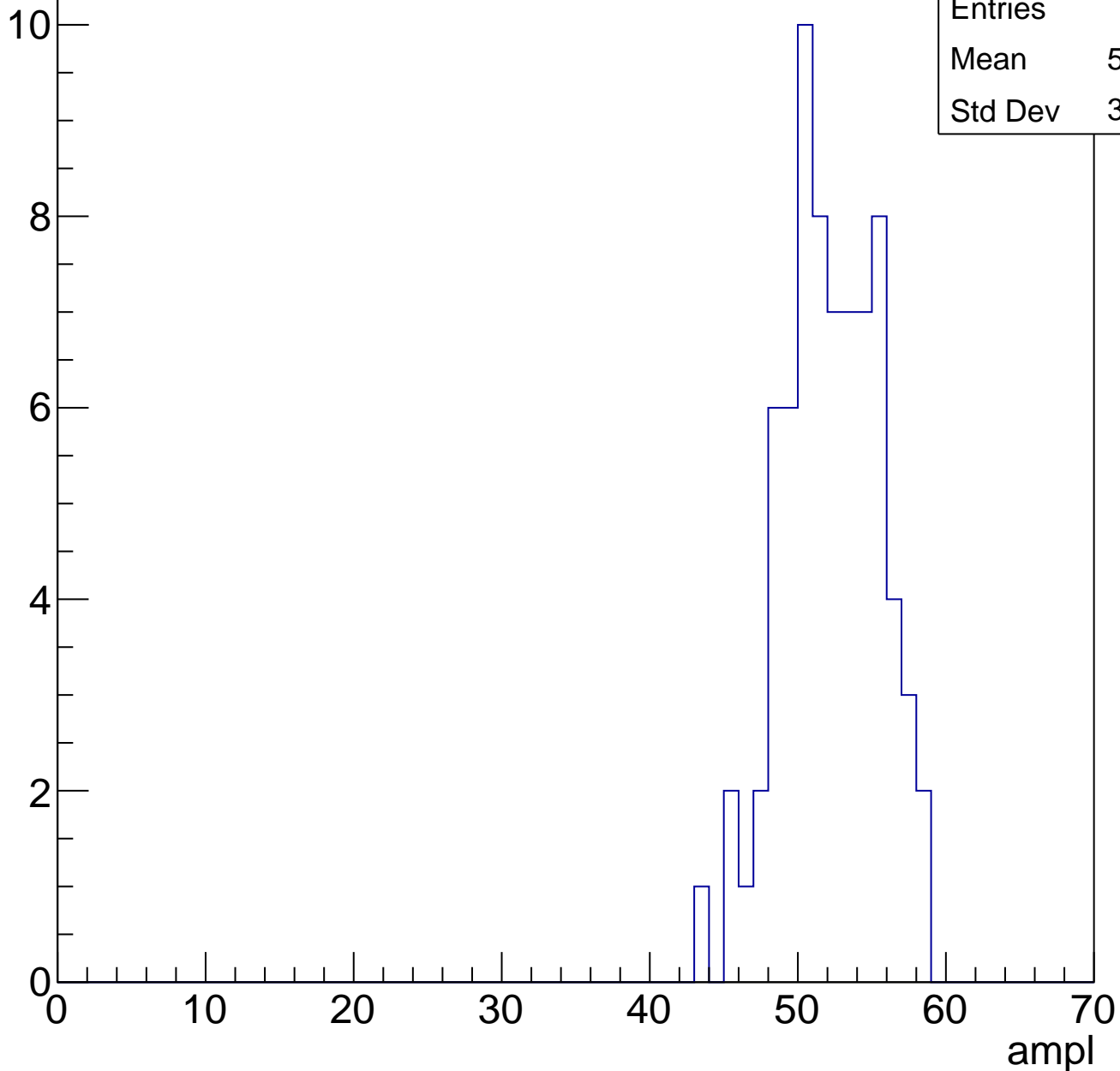


# B1L101S, U22-ch15, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	74
Mean	51.72
Std Dev	3.236

Entry

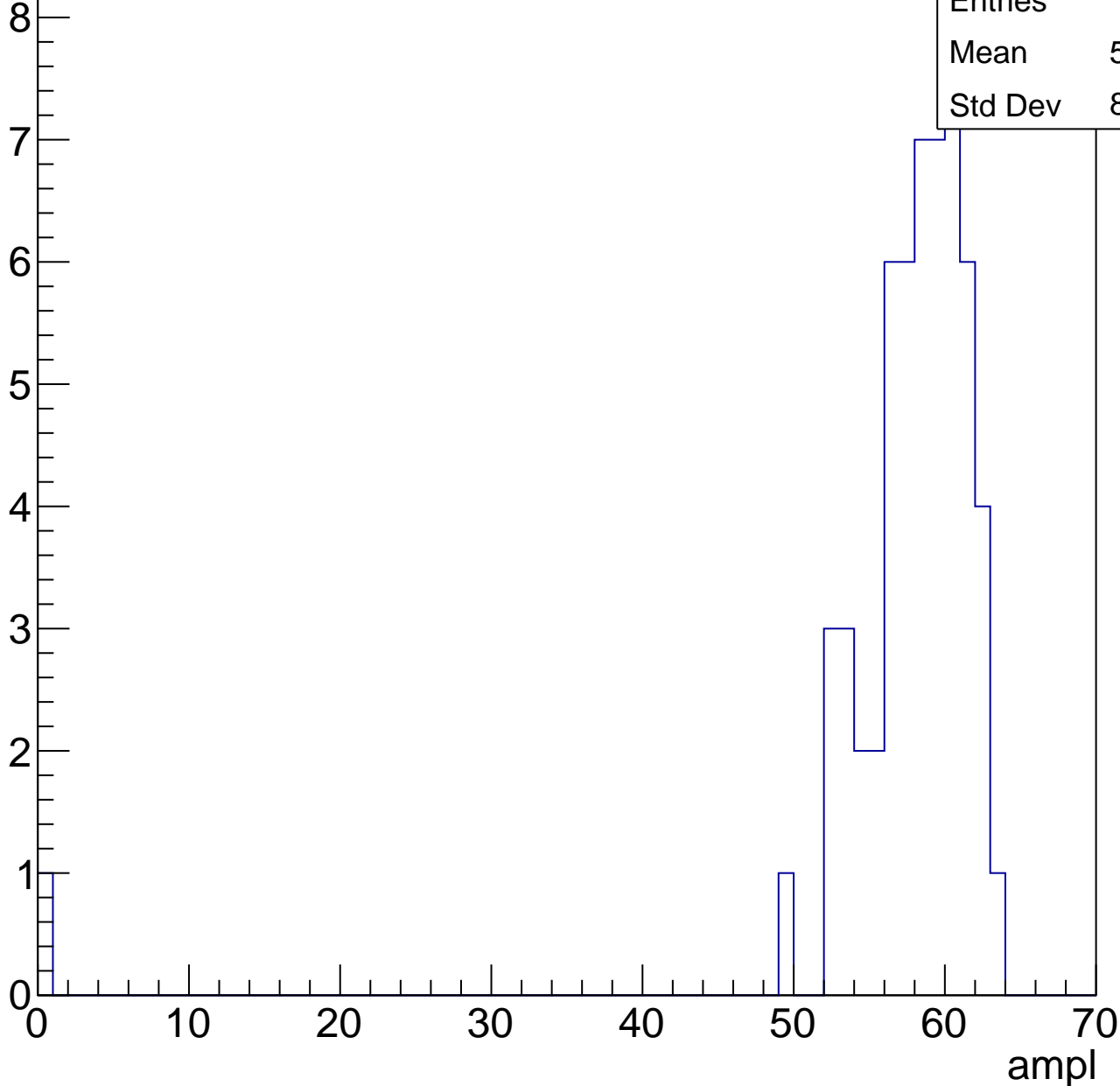


# B1L101S, U22-ch15, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

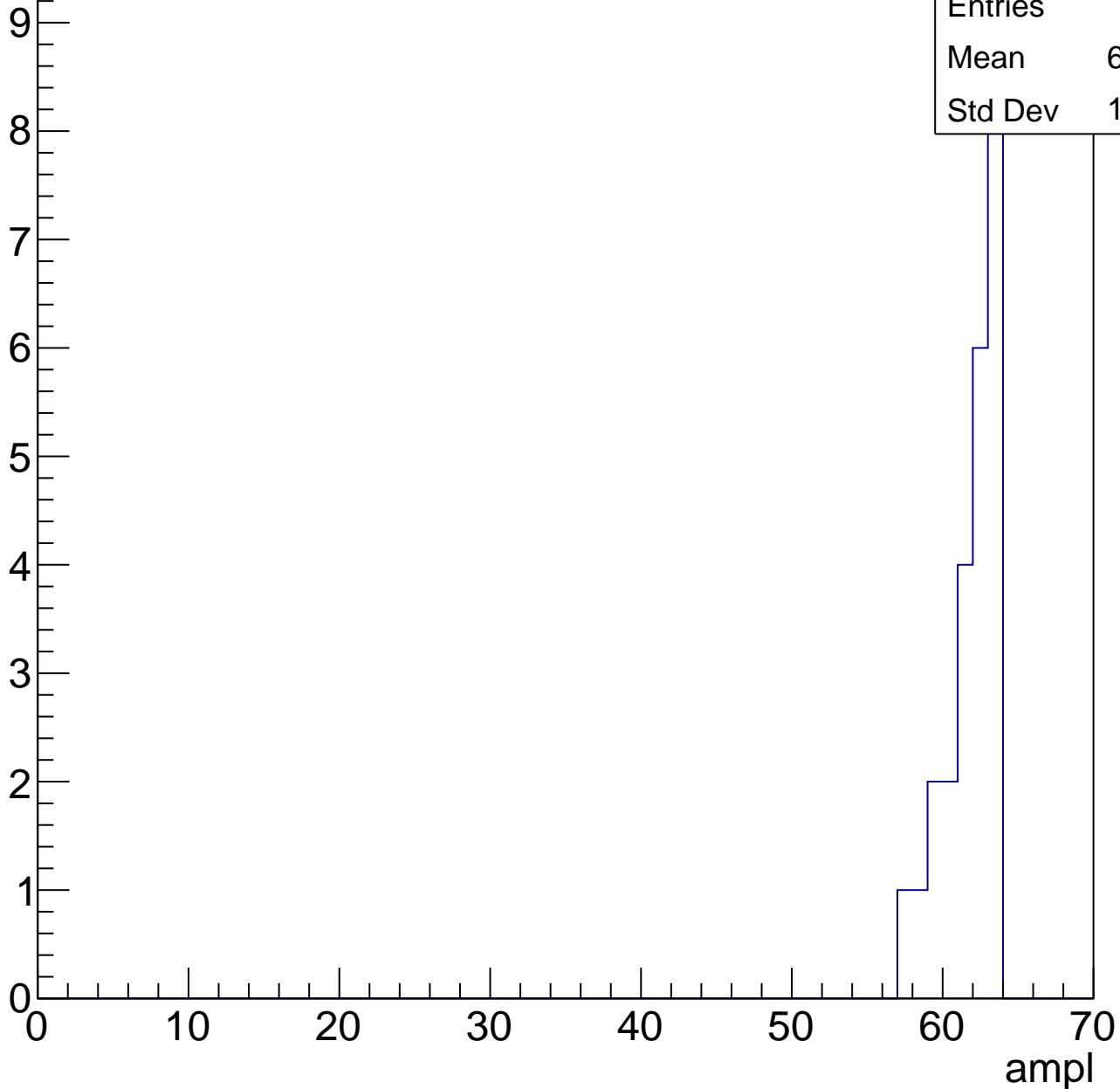
Entries	57
Mean	56.77
Std Dev	8.169



# B1L101S, U22-ch15, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U22-ch15, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U22-ch15, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U22-ch16, adc0

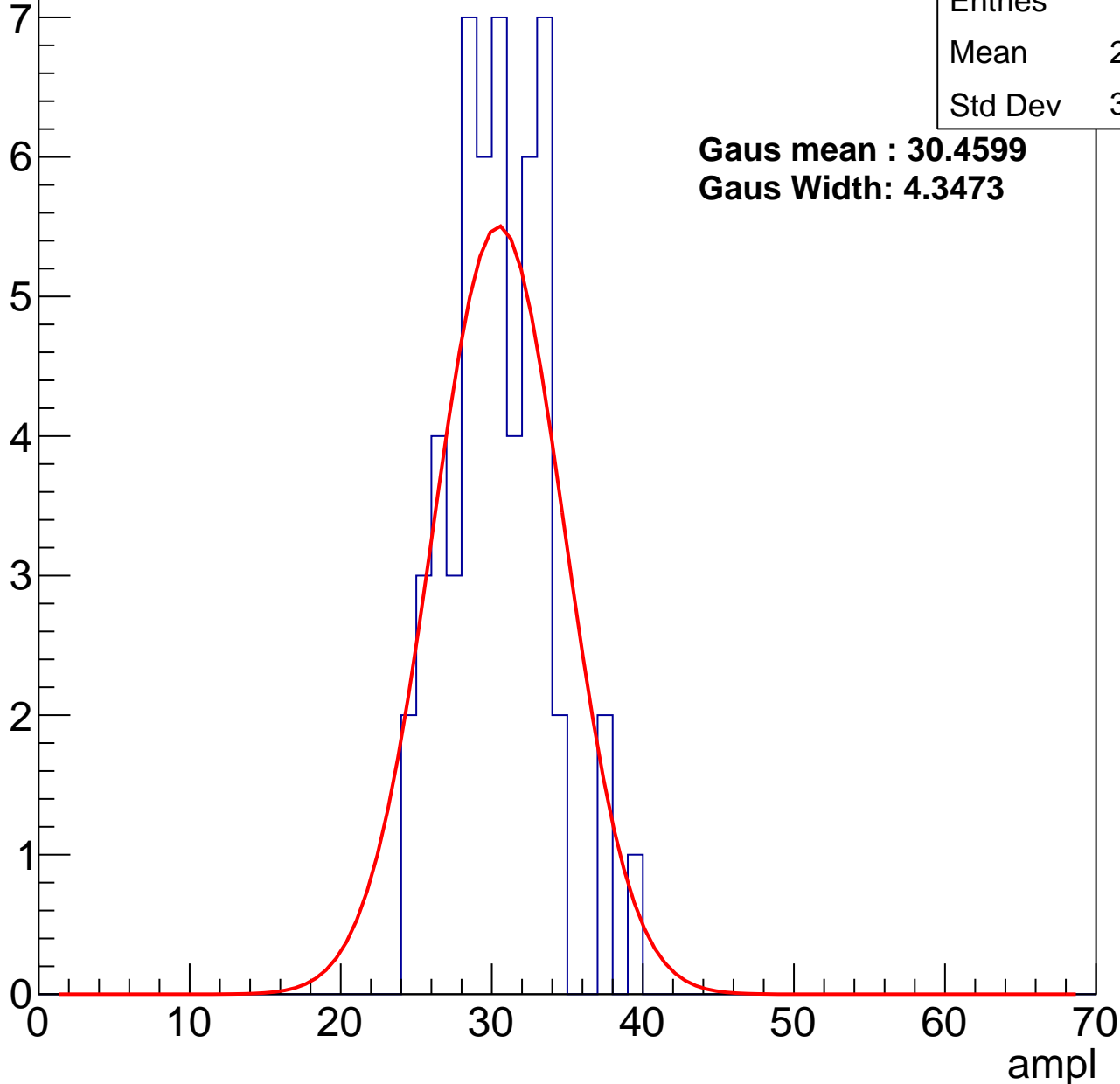
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	54
Mean	29.93
Std Dev	3.259

**Gaus mean : 30.4599**

**Gaus Width: 4.3473**



# B1L101S, U22-ch16, adc1

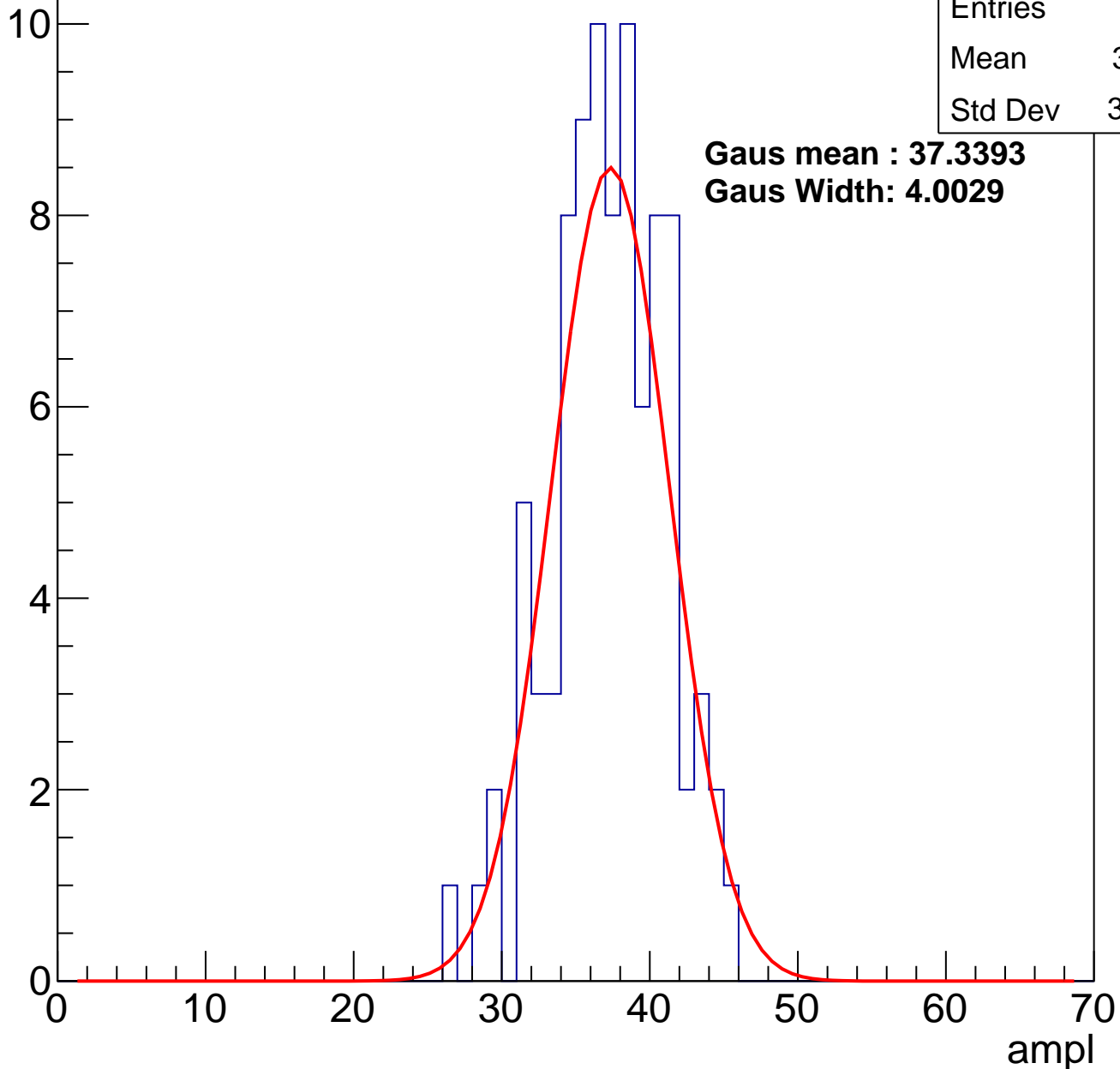
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	90
Mean	36.81
Std Dev	3.803

**Gaus mean : 37.3393**

**Gaus Width: 4.0029**

Entry



# B1L101S, U22-ch16, adc2

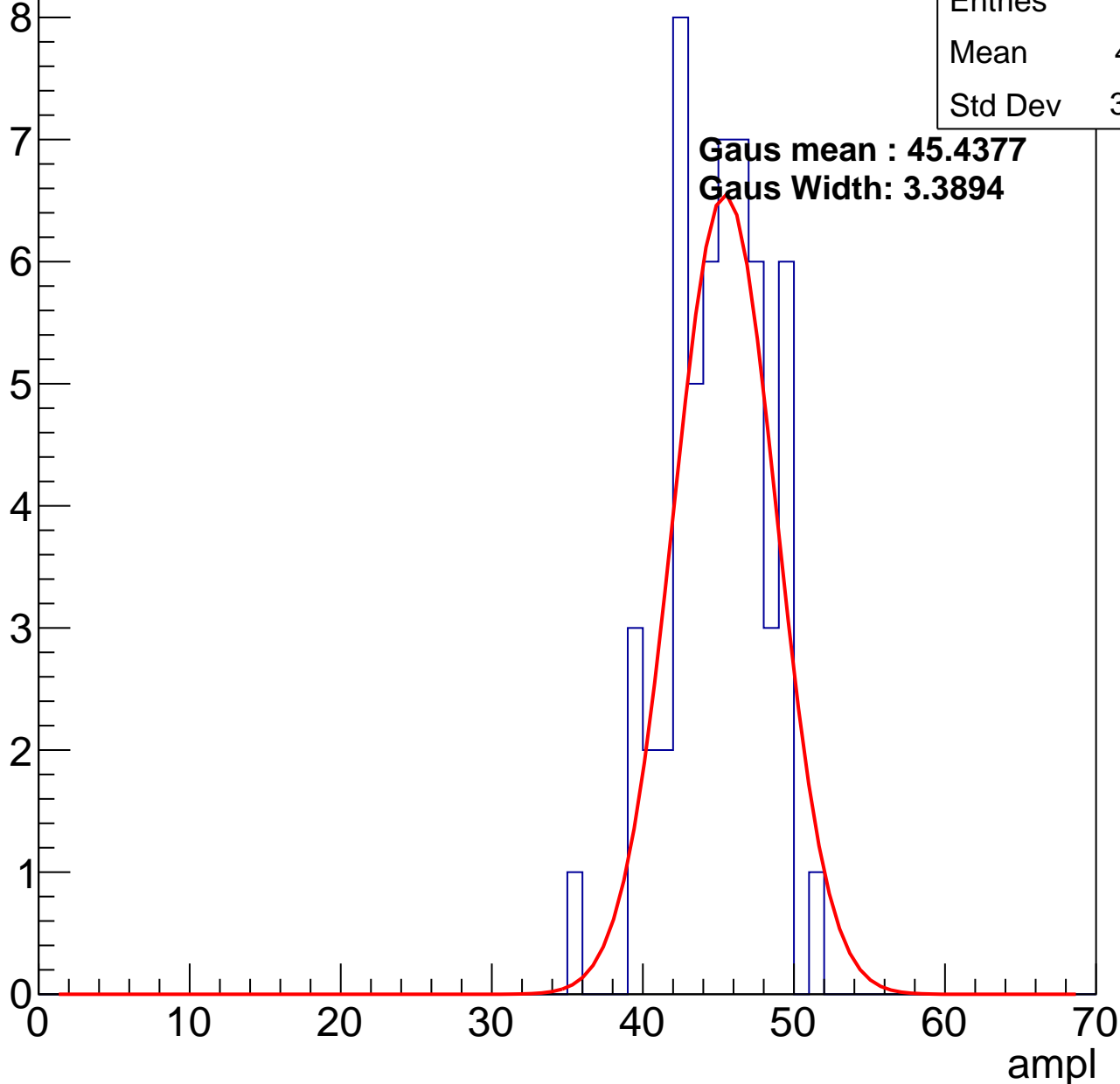
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	57
Mean	44.51
Std Dev	3.146

**Gaus mean : 45.4377**

**Gaus Width: 3.3894**

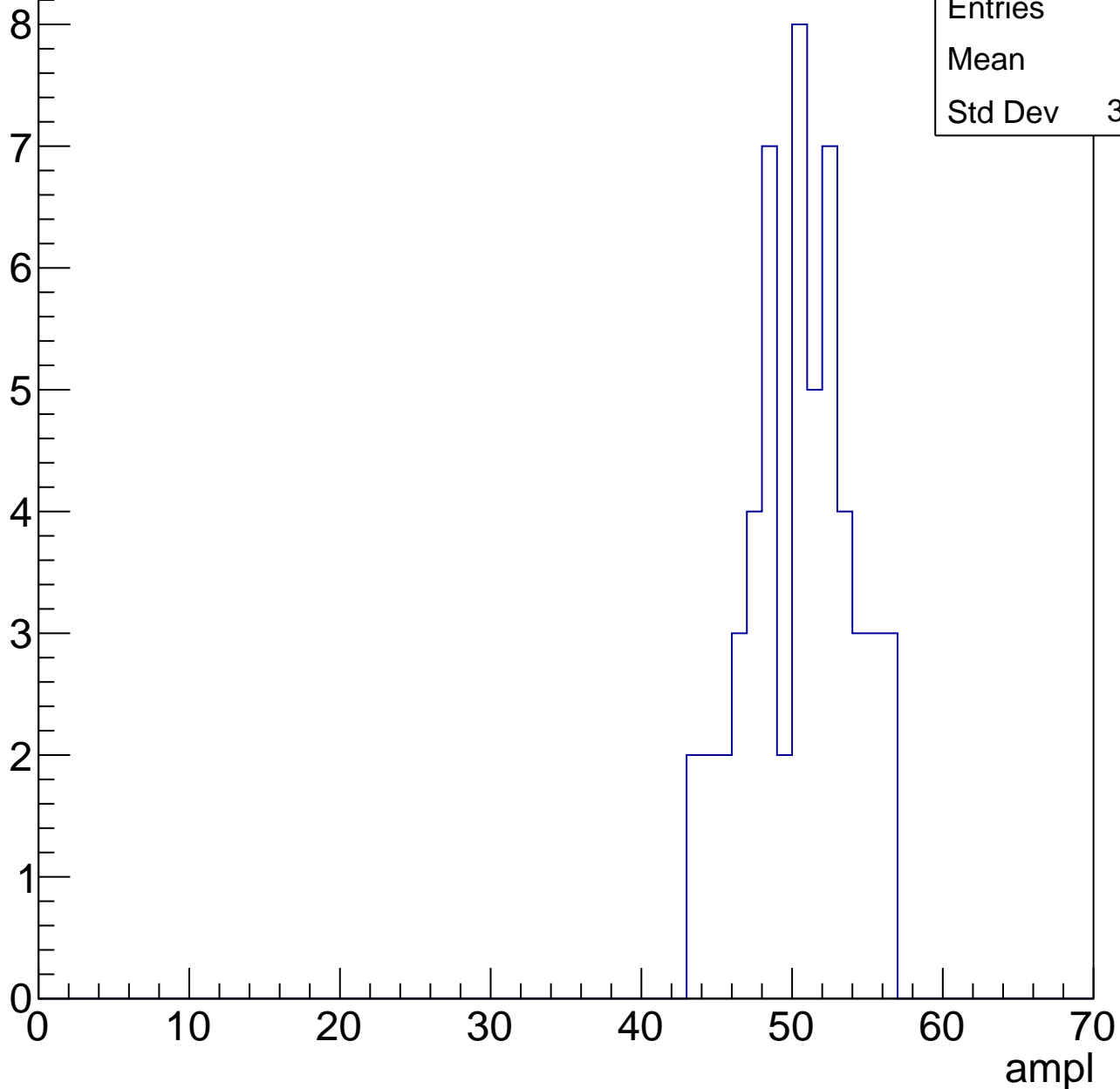


# B1L101S, U22-ch16, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	55
Mean	50
Std Dev	3.395

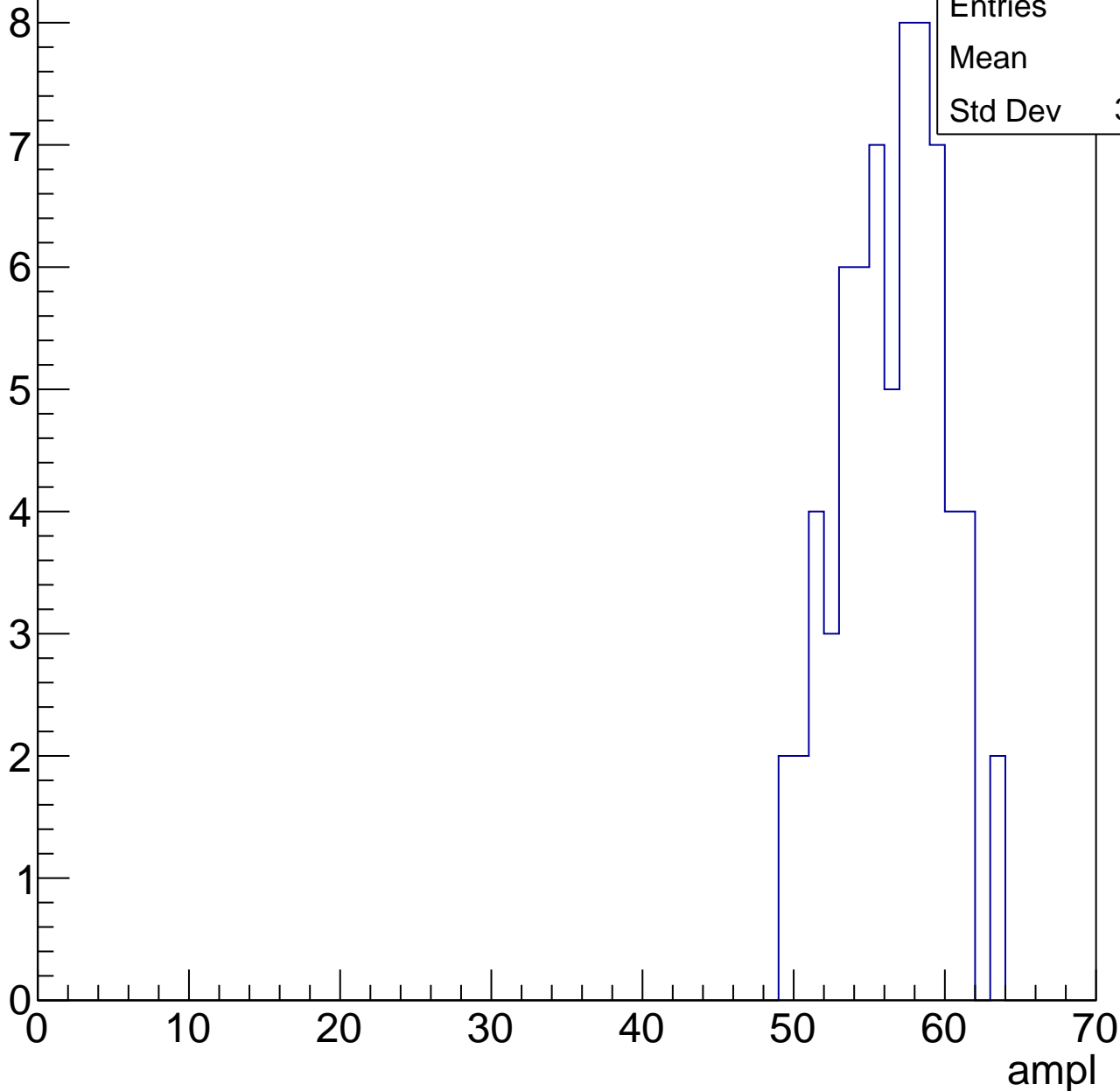


# B1L101S, U22-ch16, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	56
Std Dev	3.361

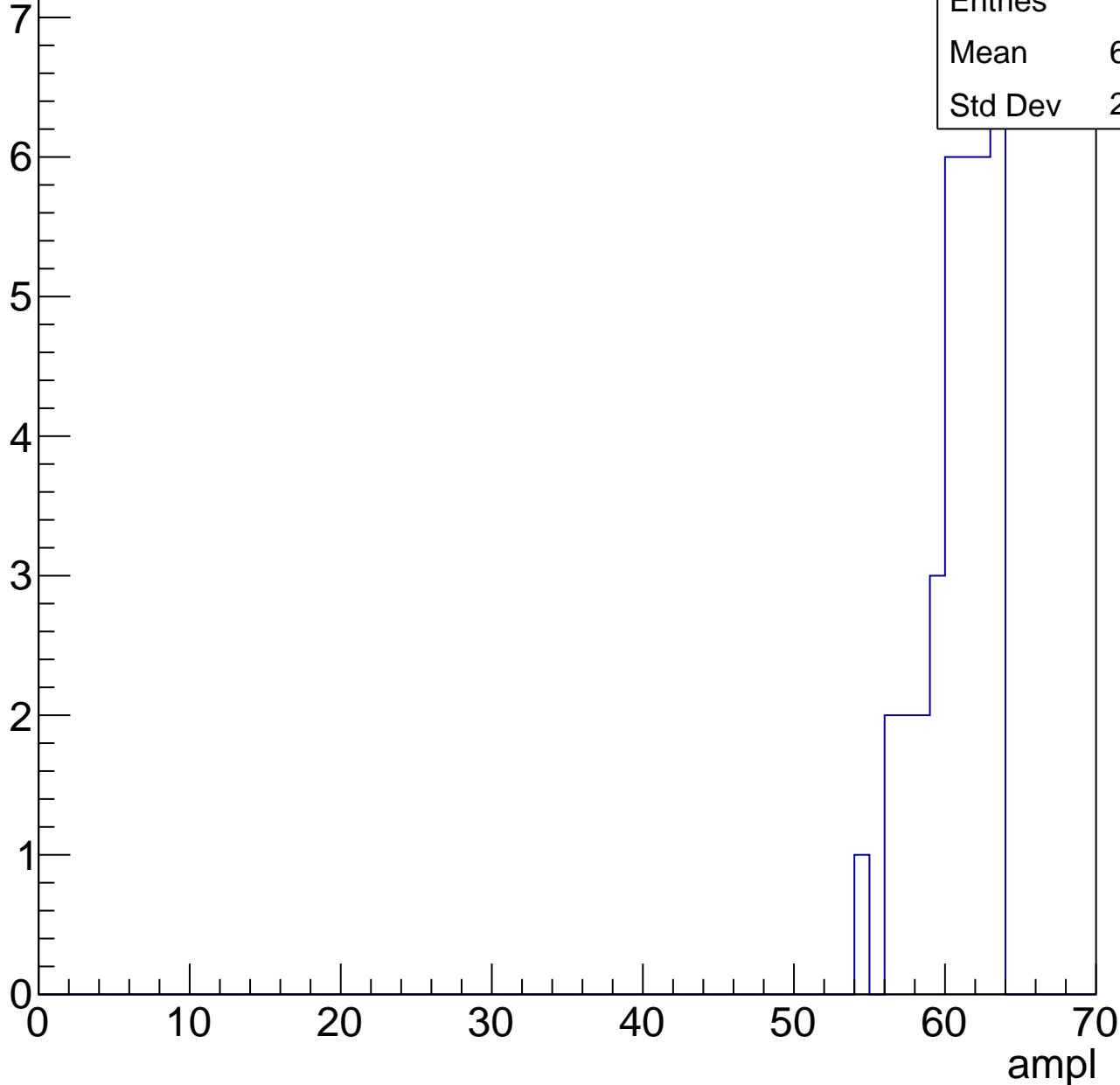


# B1L101S, U22-ch16, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

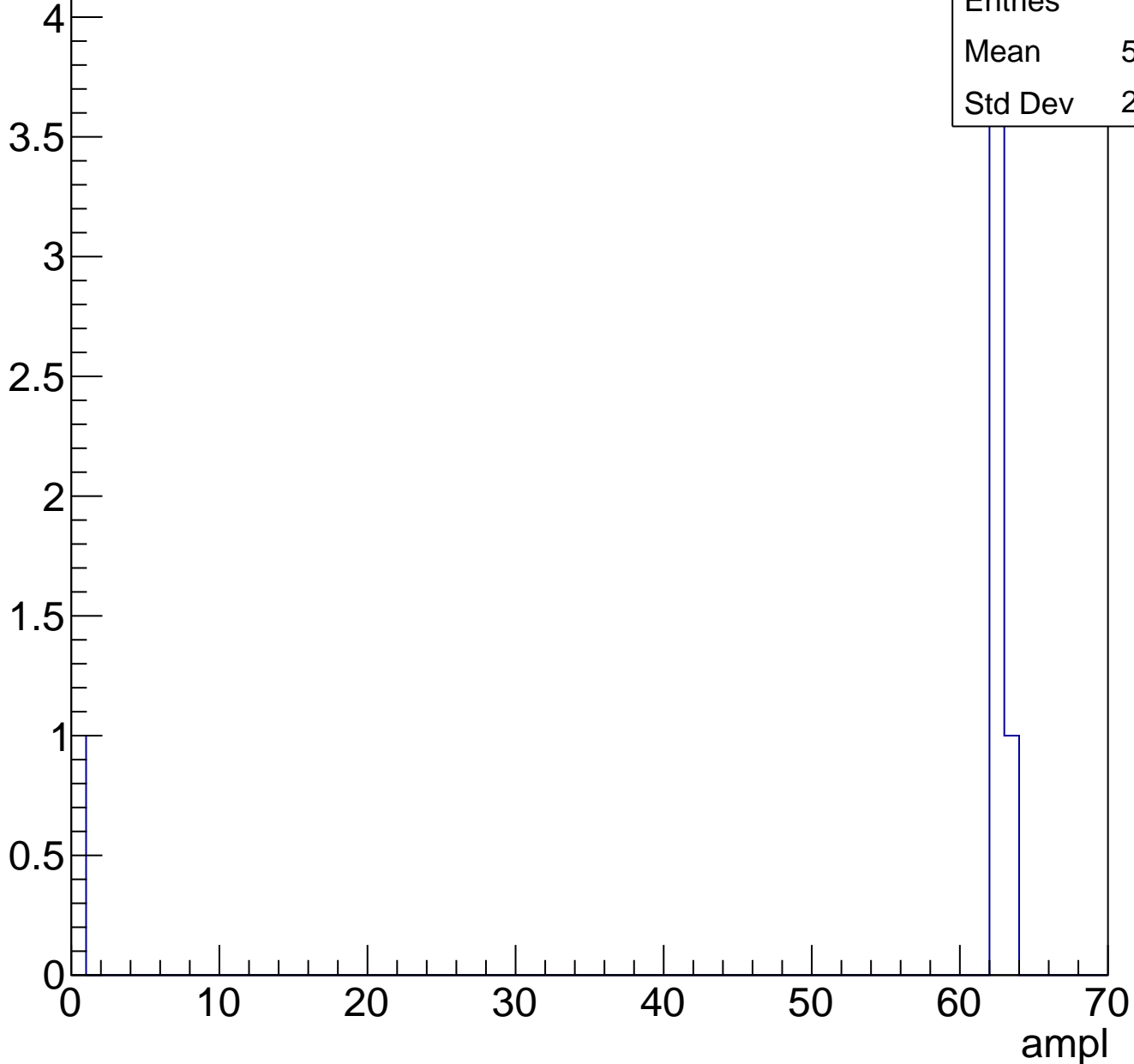
Entries	35
Mean	60.34
Std Dev	2.305



# B1L101S, U22-ch16, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U22-ch16, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L101S, U22-ch17, adc0

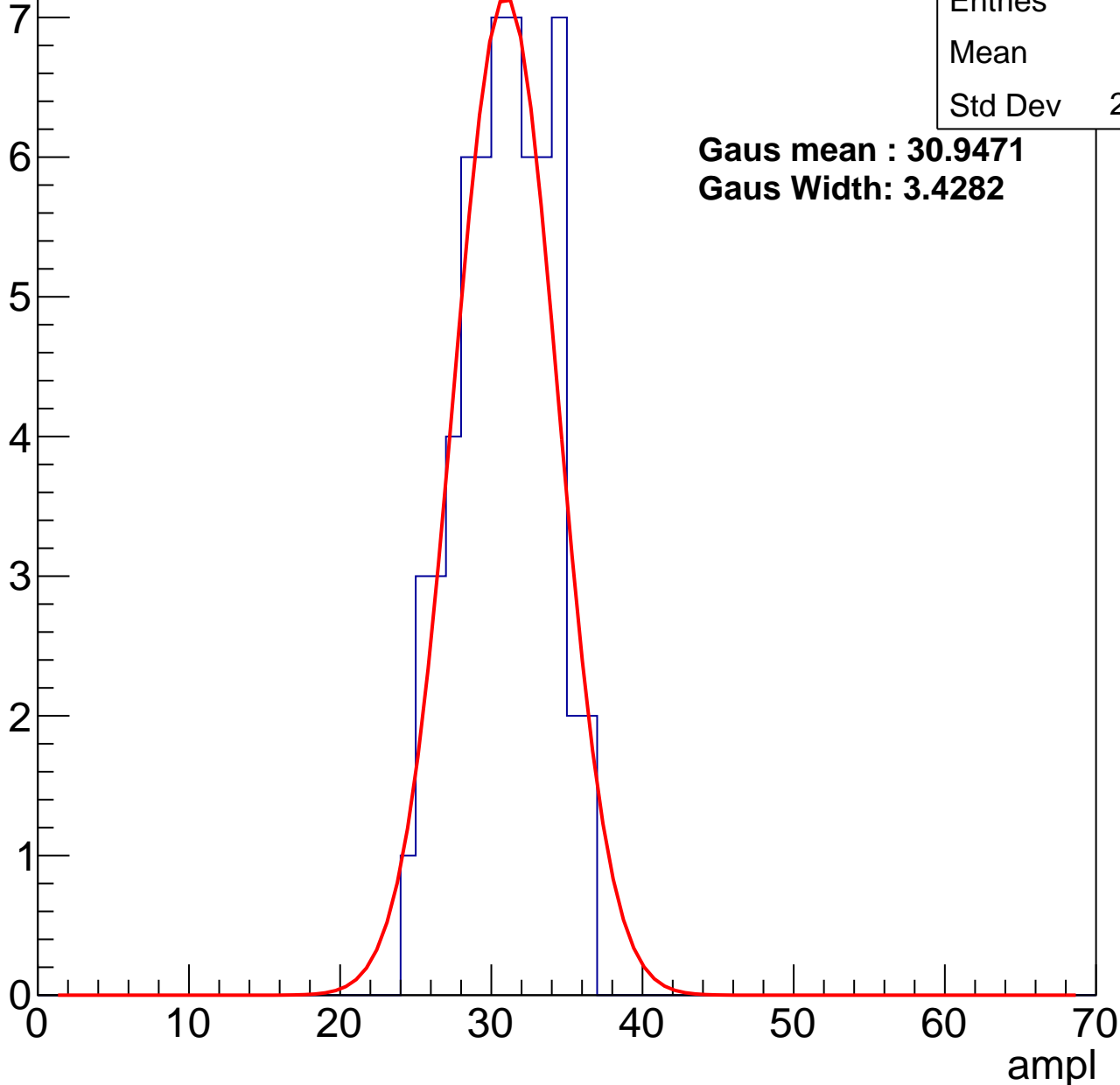
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	60
Mean	30.4
Std Dev	2.984

**Gaus mean : 30.9471**

**Gaus Width: 3.4282**



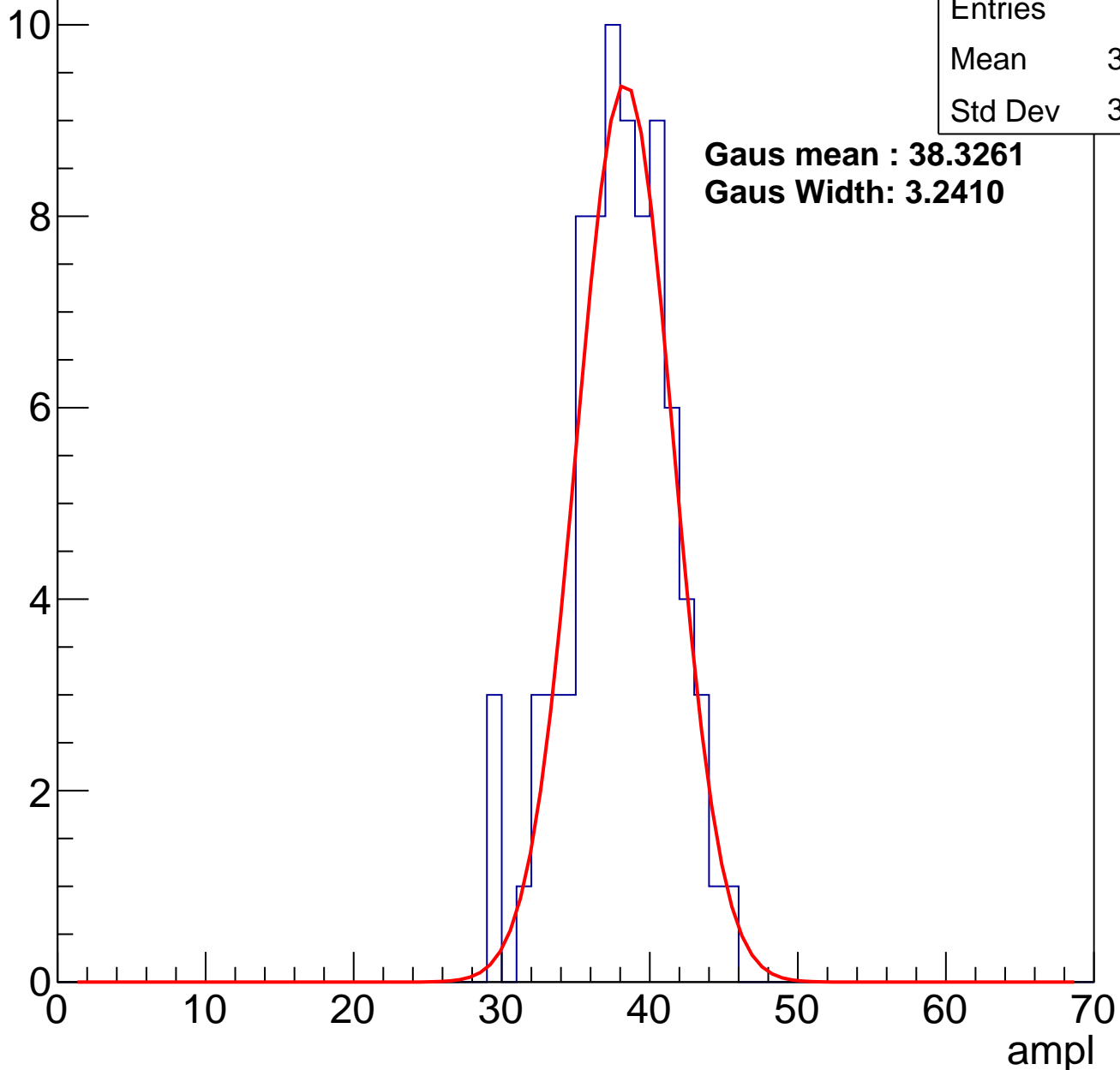
# B1L101S, U22-ch17, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	80
Mean	37.49
Std Dev	3.424

**Gaus mean : 38.3261**  
**Gaus Width: 3.2410**

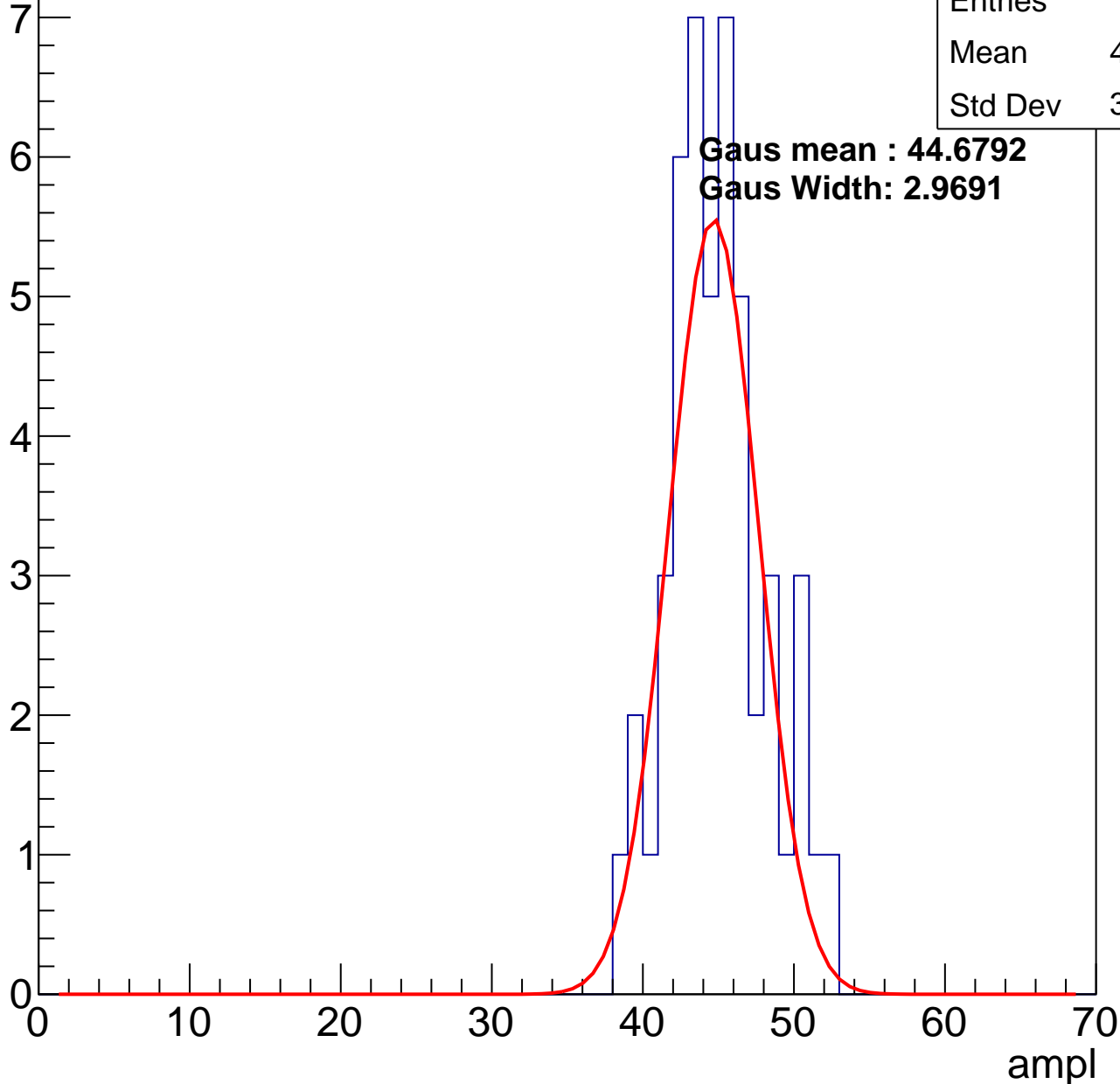
Entry



# B1L101S, U22-ch17, adc2

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

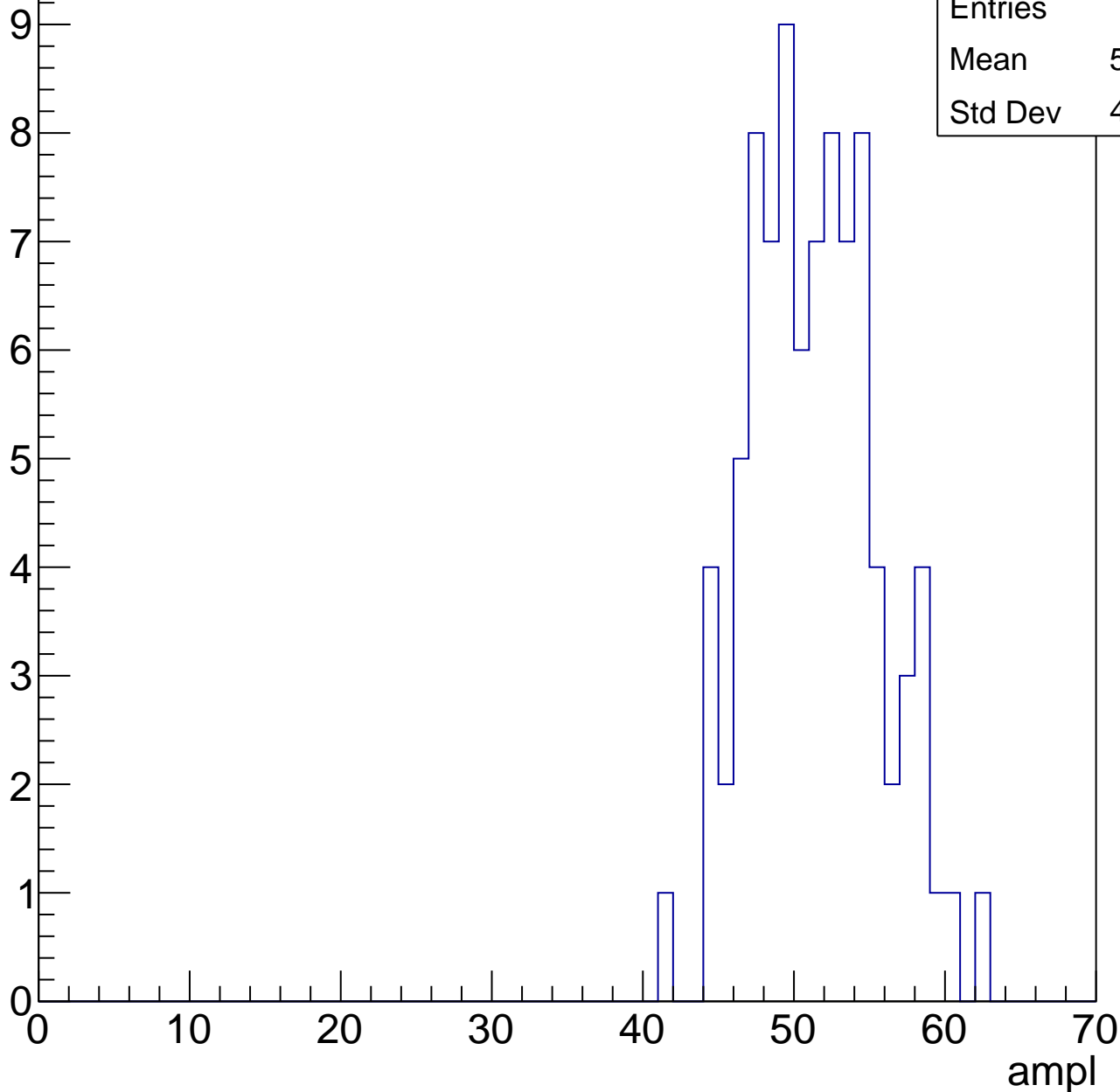


# B1L101S, U22-ch17, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

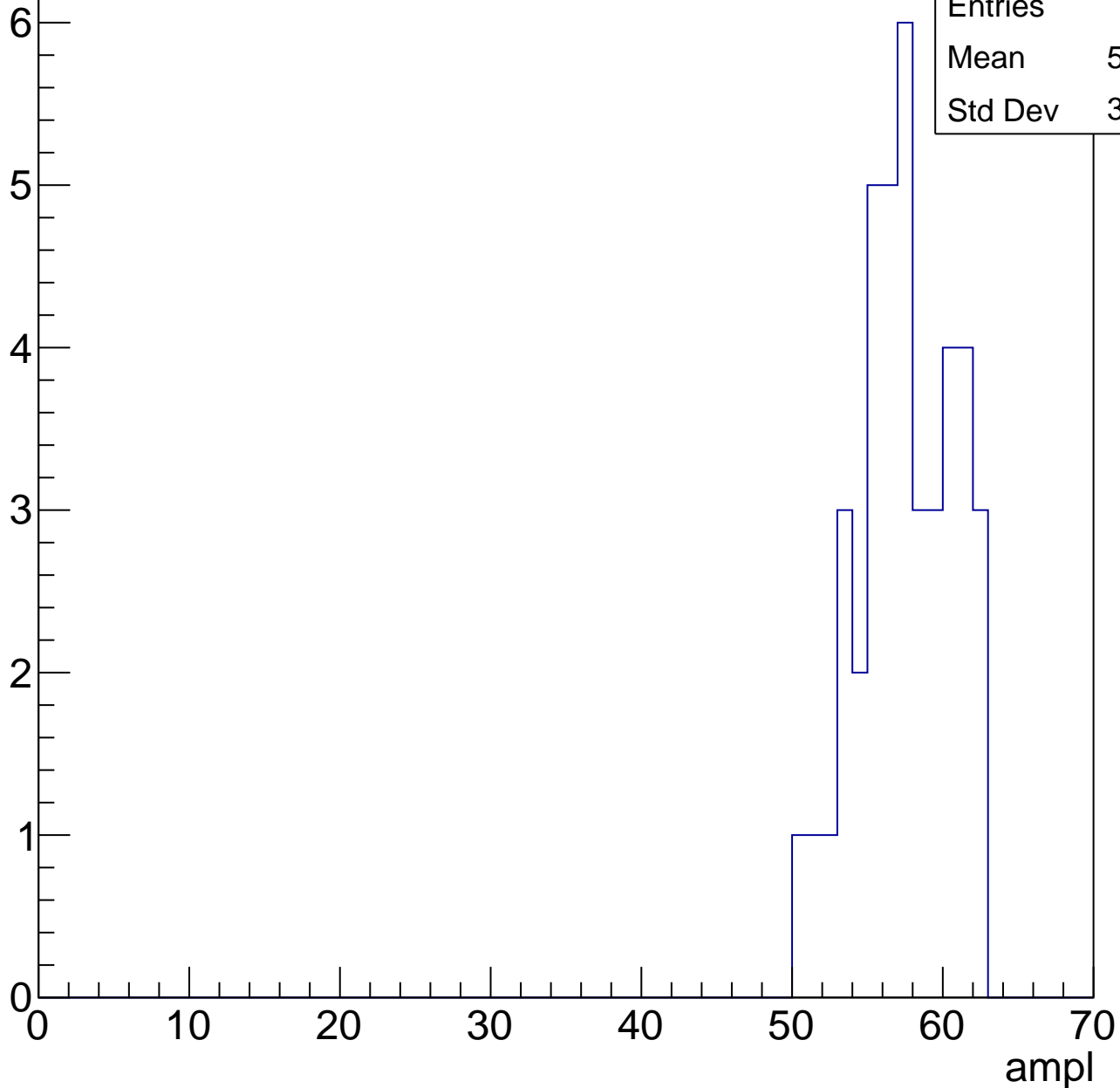
Entries	88
Mean	50.93
Std Dev	4.153



# B1L101S, U22-ch17, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



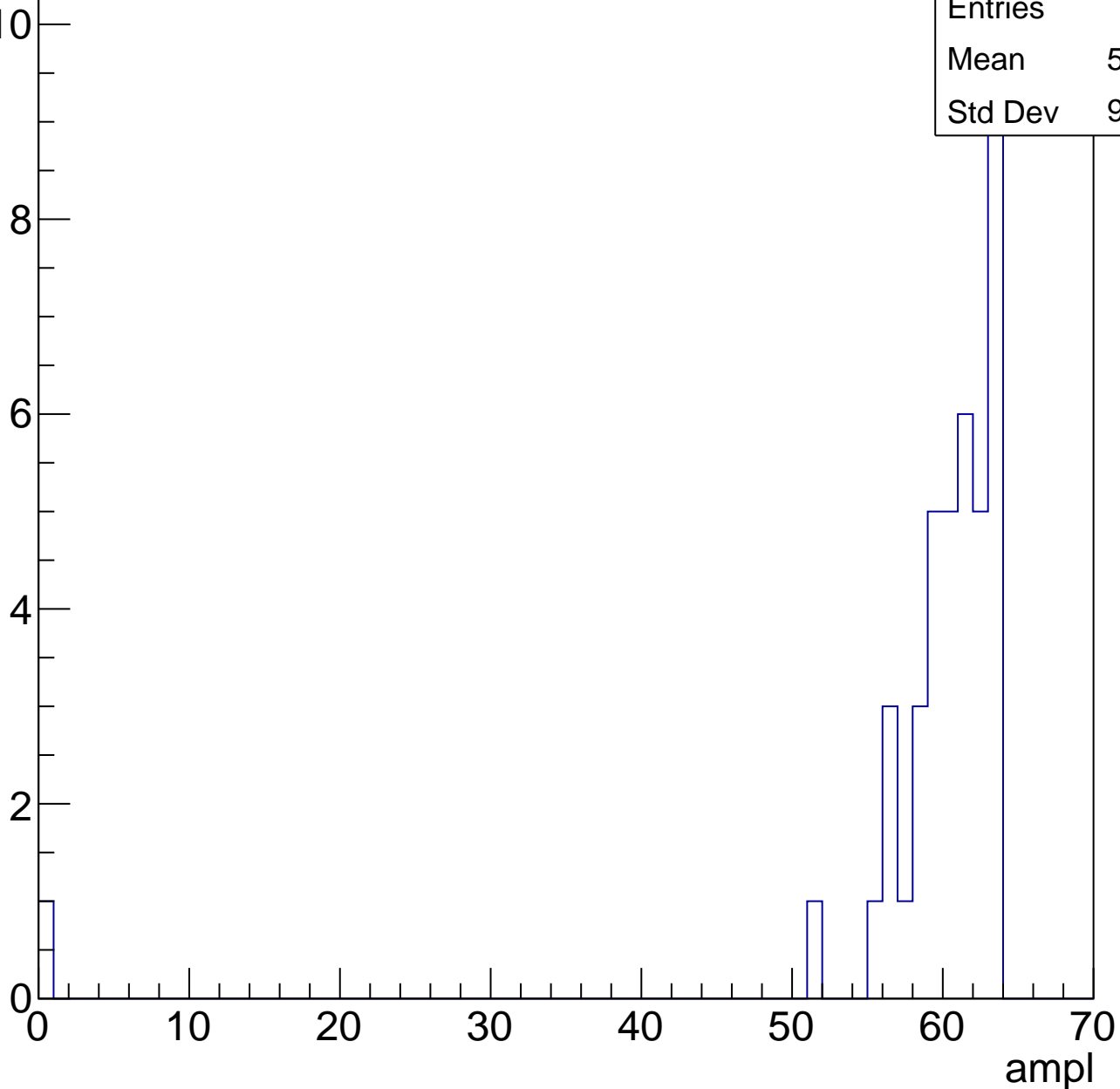
Entries	41
Mean	57.02
Std Dev	3.088

# B1L101S, U22-ch17, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

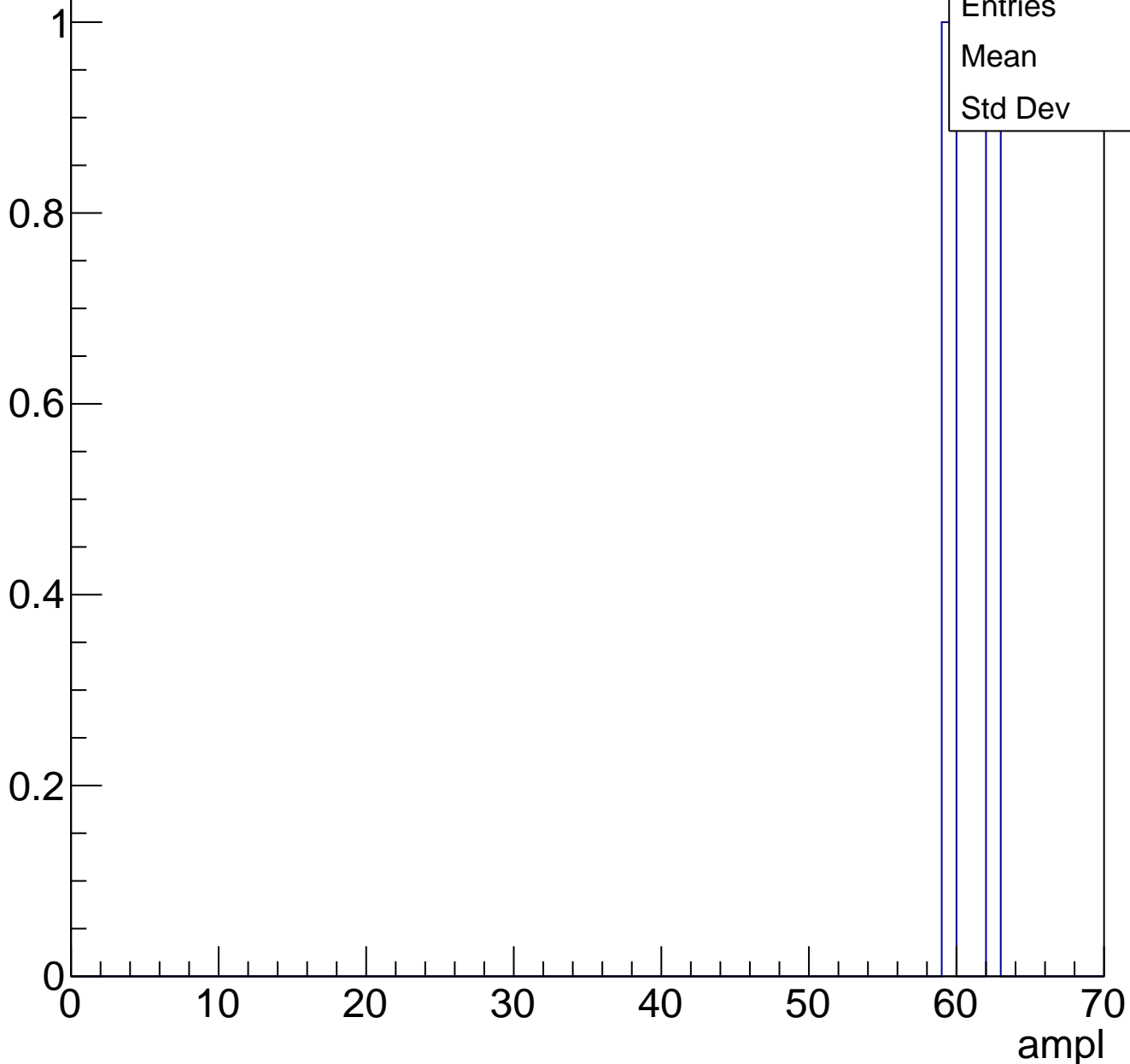
Entries	41
Mean	58.68
Std Dev	9.659



# B1L101S, U22-ch17, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U22-ch17, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U22-ch18, adc0

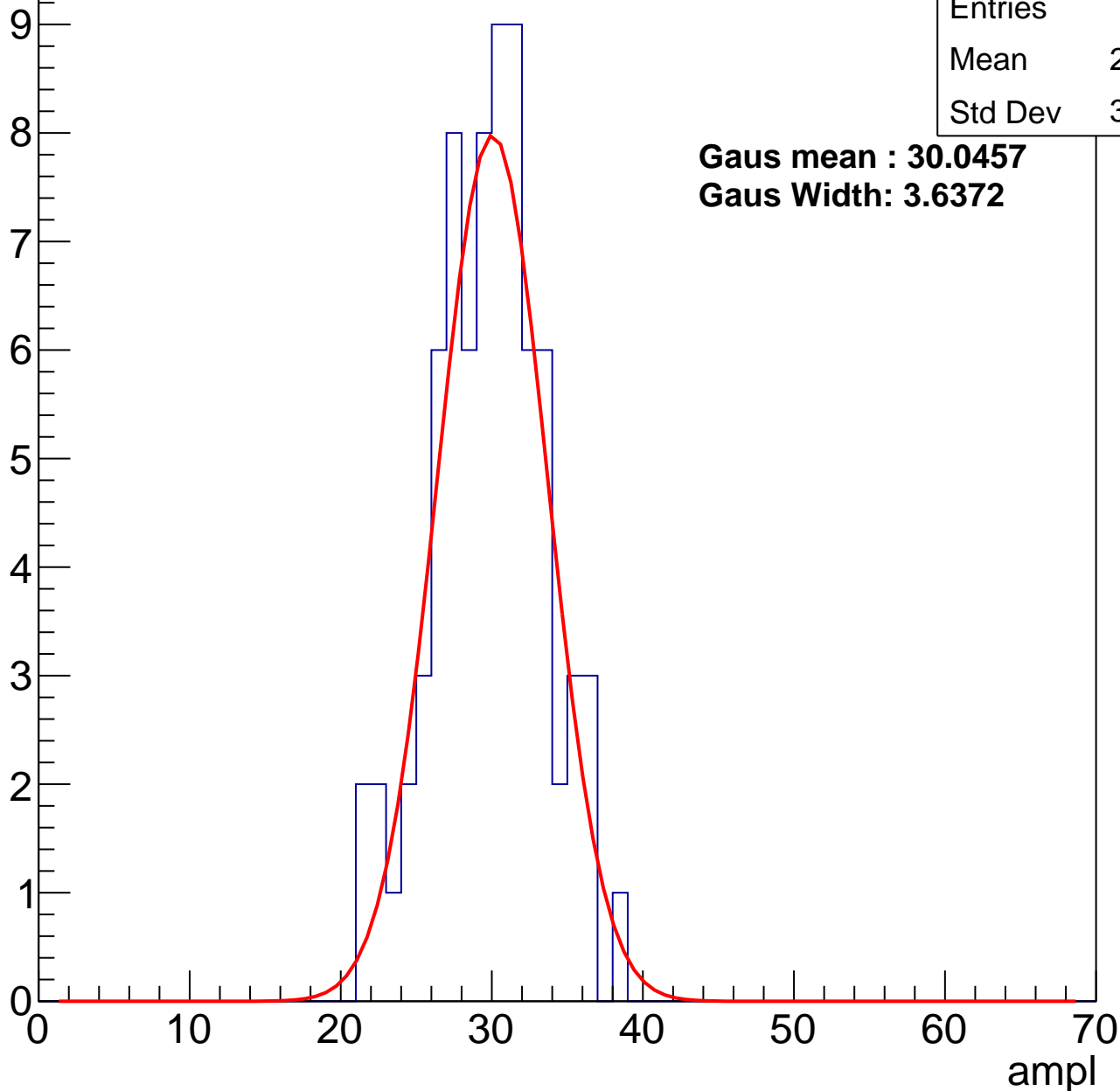
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	77
Mean	29.38
Std Dev	3.643

**Gaus mean : 30.0457**

**Gaus Width: 3.6372**



# B1L101S, U22-ch18, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	69
Mean	37.03
Std Dev	3.514

**Gaus mean : 37.5143**

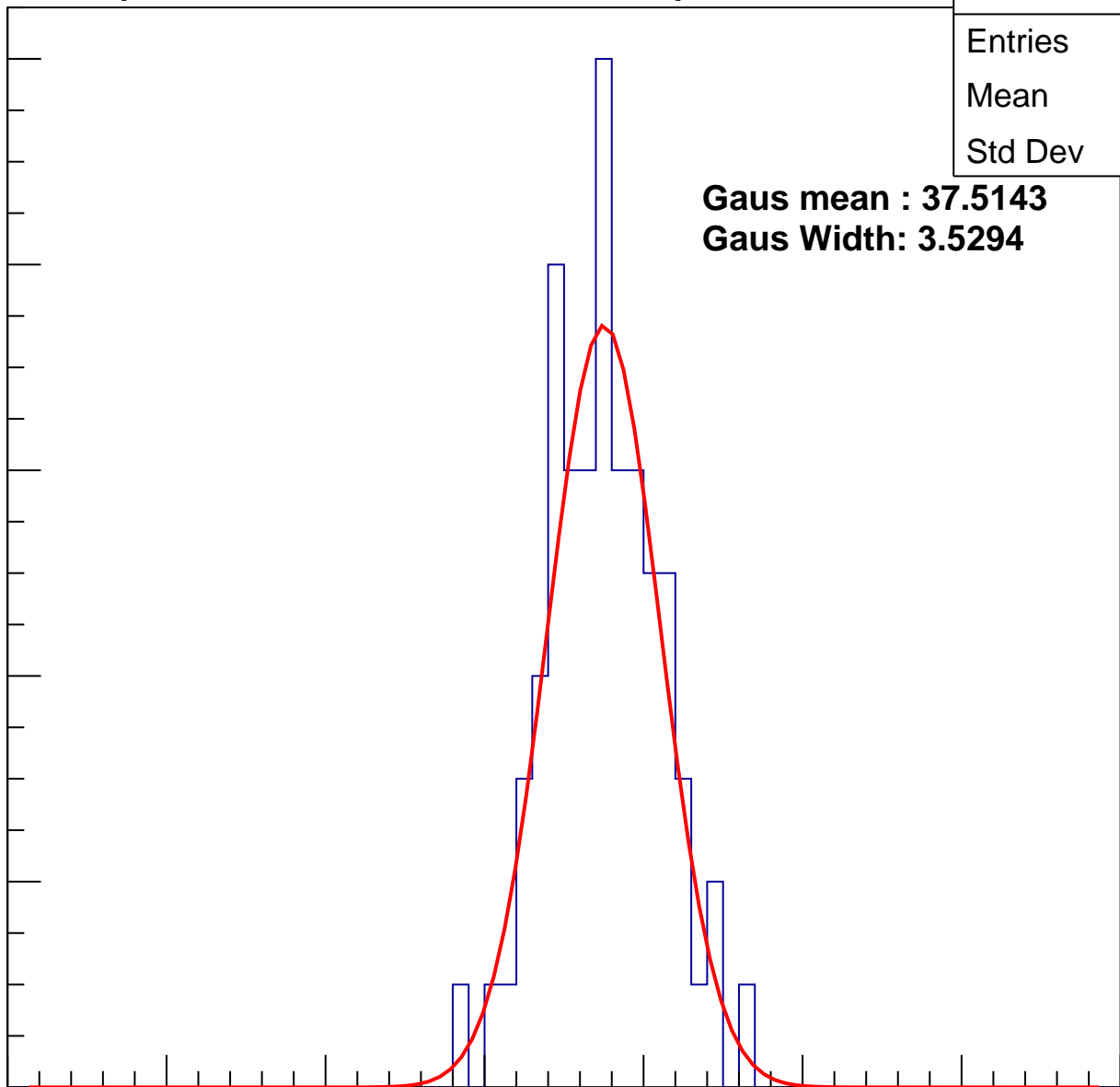
**Gaus Width: 3.5294**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U22-ch18, adc2

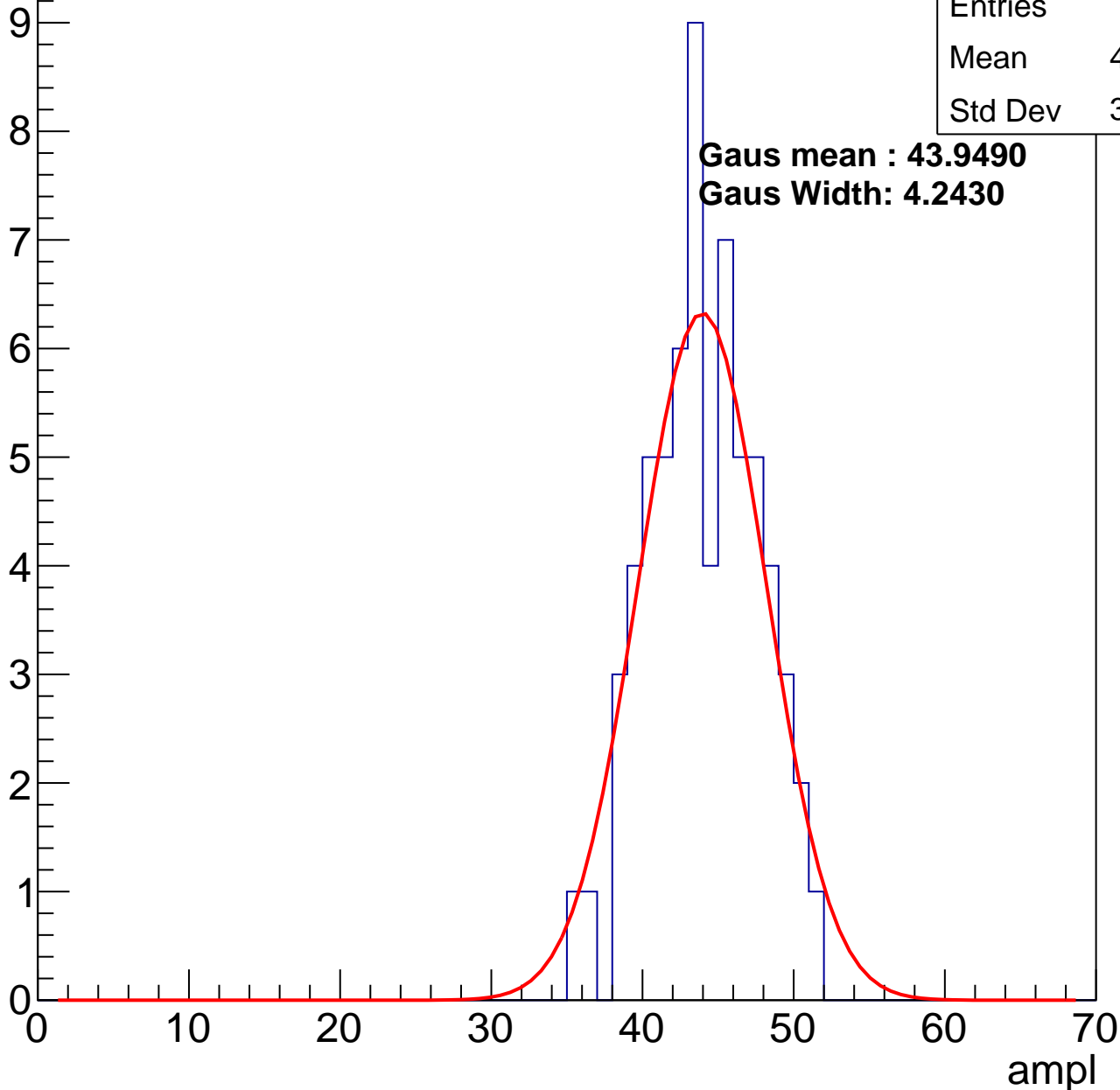
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	43.55
Std Dev	3.574

**Gaus mean : 43.9490**

**Gaus Width: 4.2430**

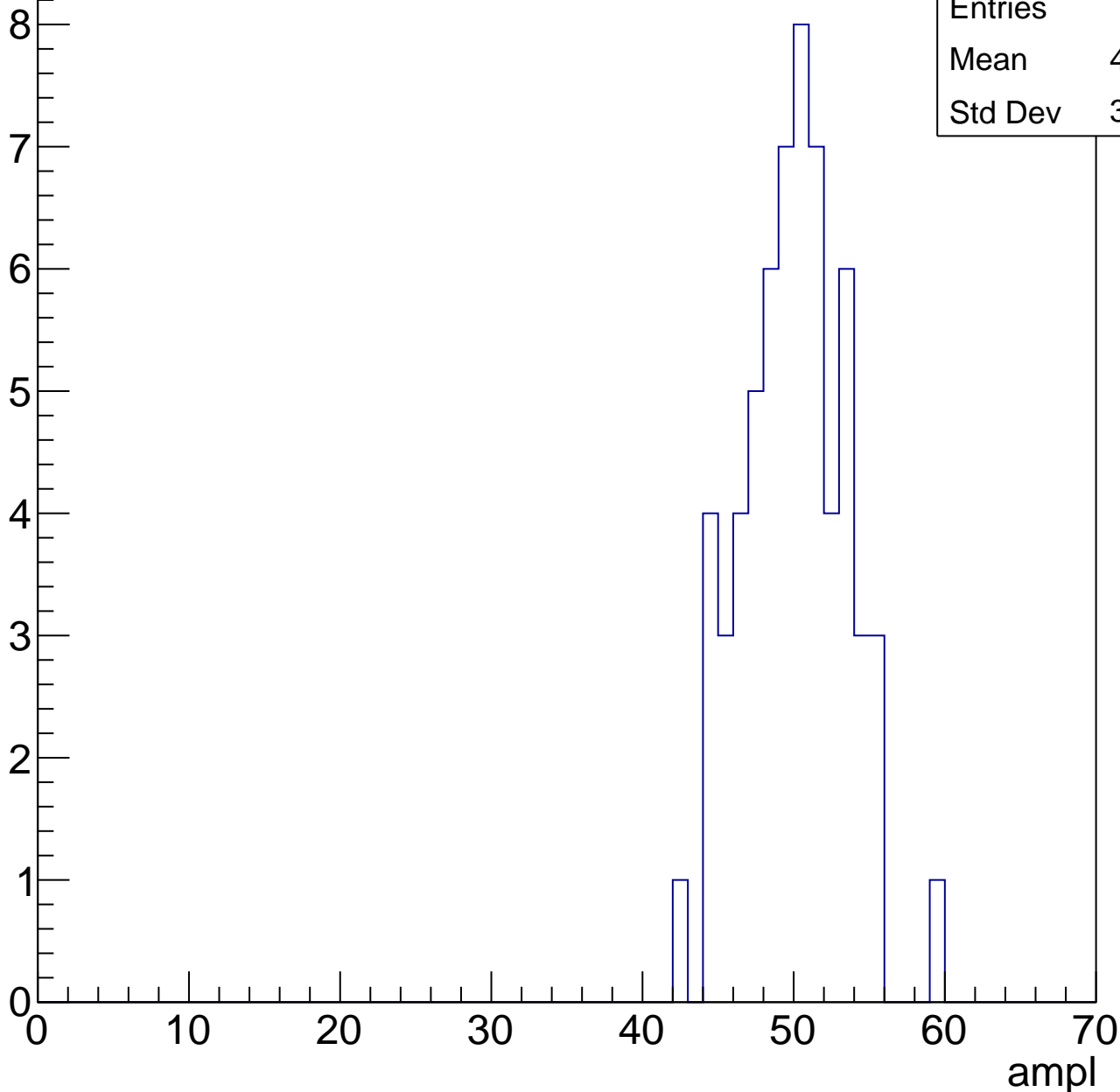


# B1L101S, U22-ch18, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

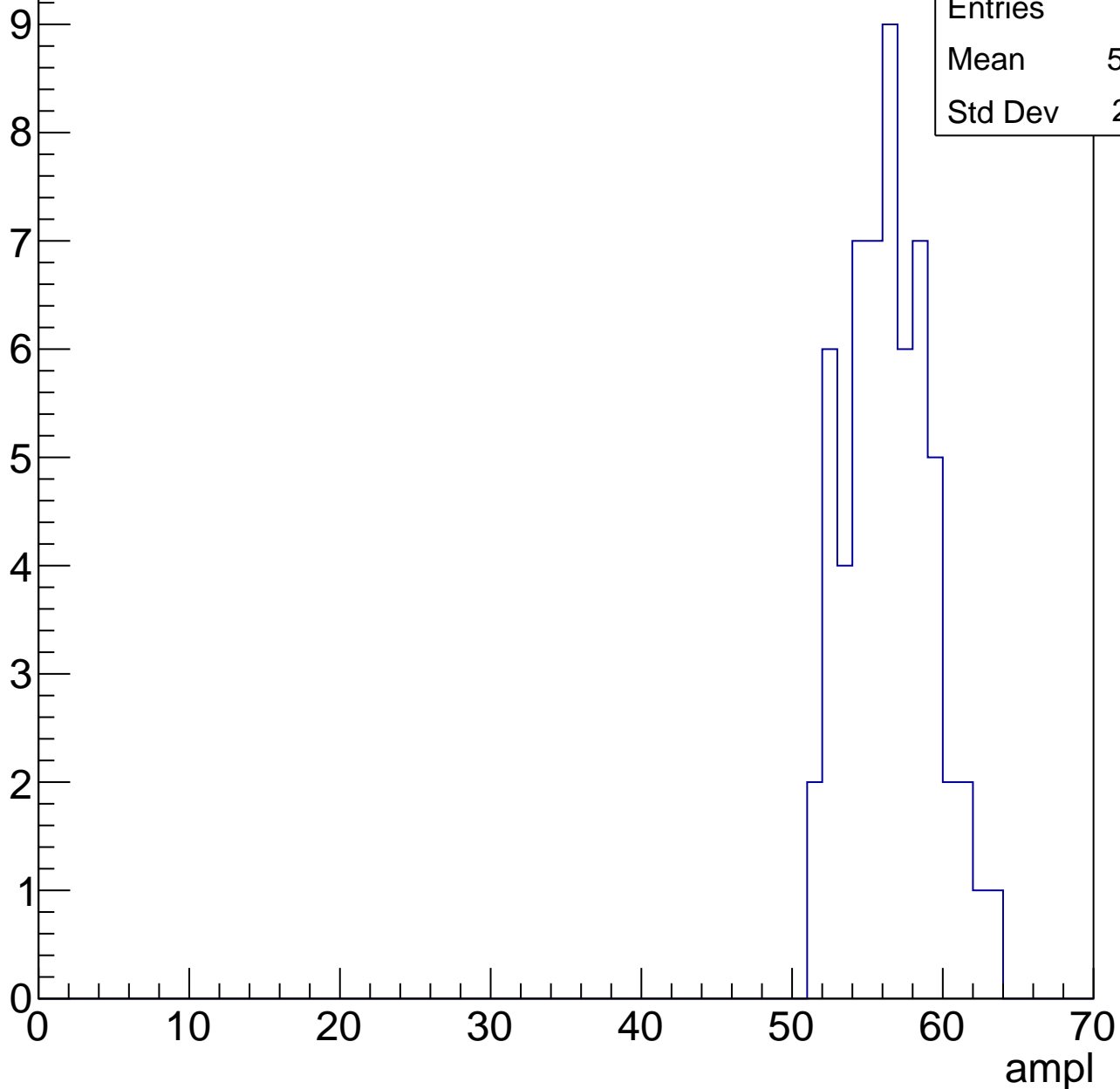
Entries	62
Mean	49.55
Std Dev	3.339



# B1L101S, U22-ch18, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

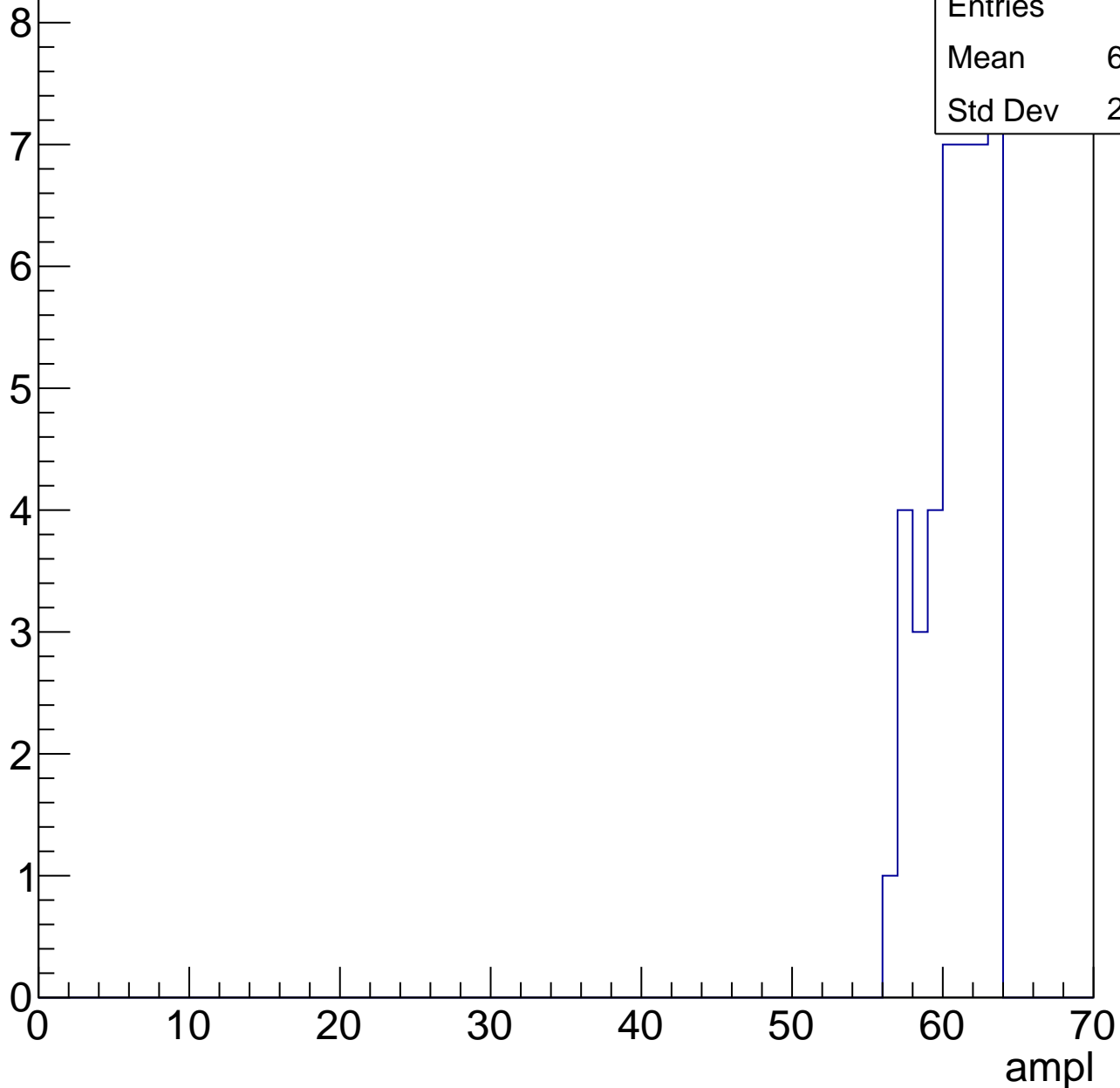
Entry



# B1L101S, U22-ch18, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	41
Mean	60.46
Std Dev	2.013

# B1L101S, U22-ch18, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

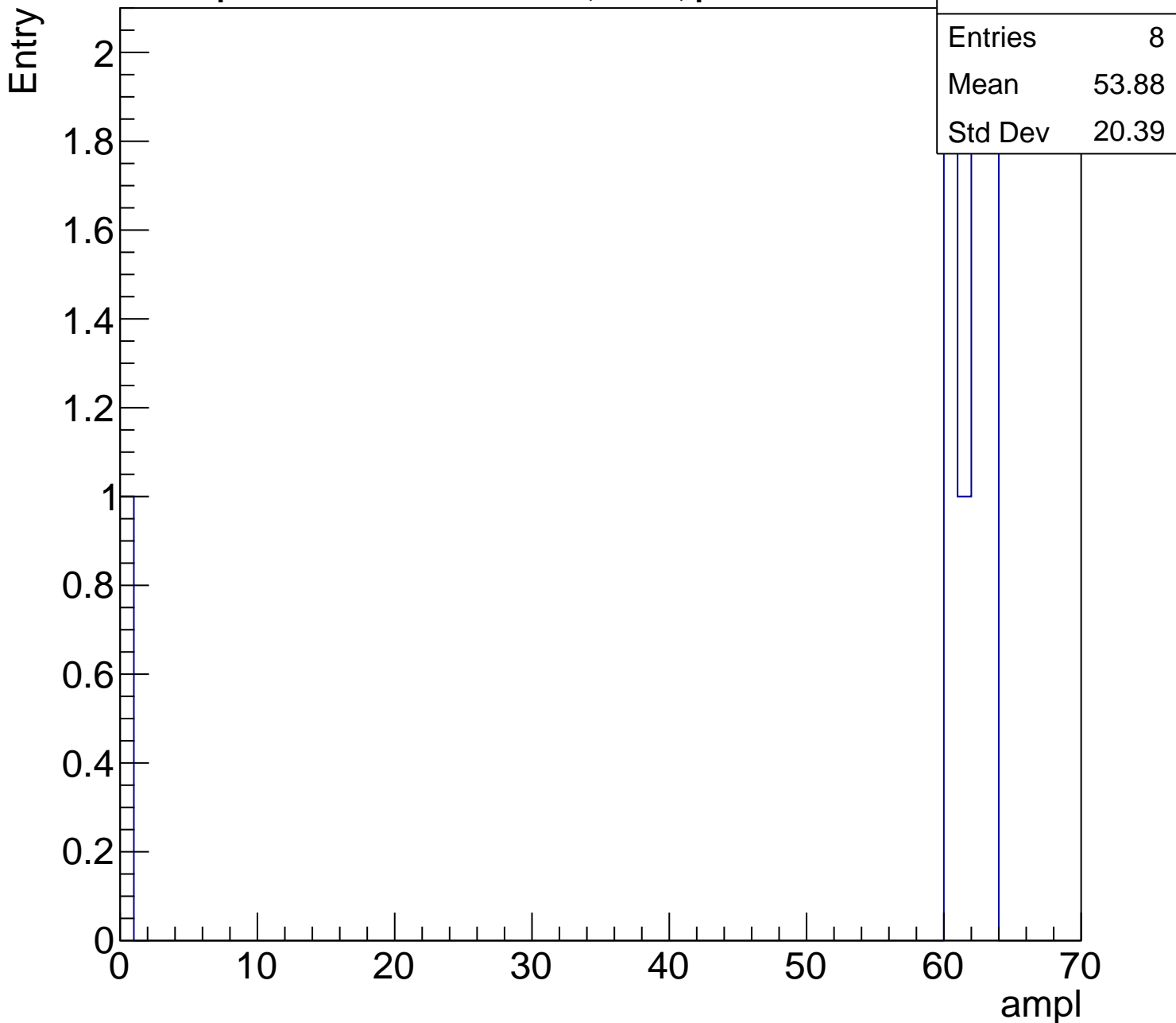
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	8
Mean	53.88
Std Dev	20.39

0 10 20 30 40 50 60 70

ampl





# B1L101S, U22-ch18, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U22-ch19, adc0

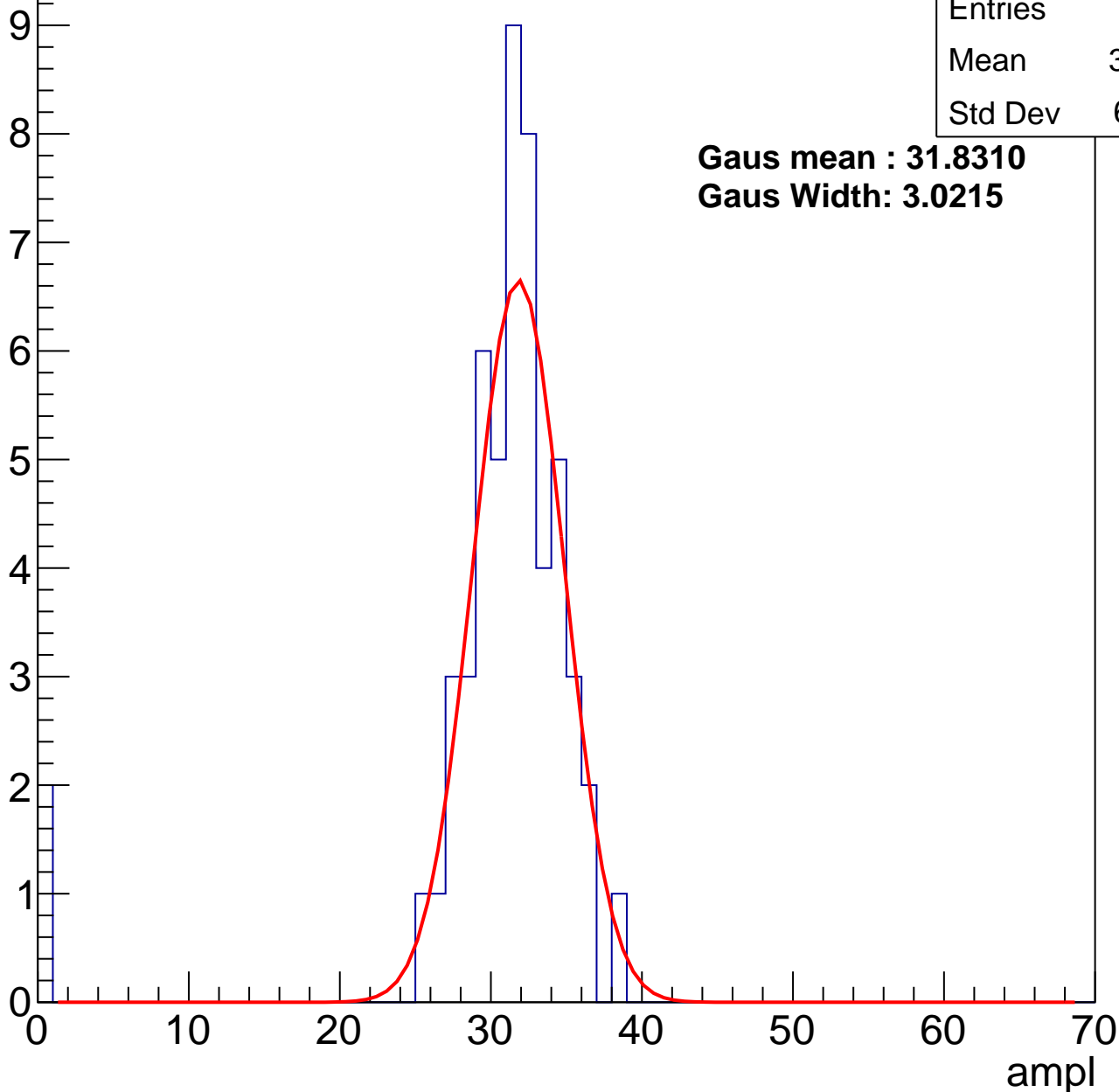
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	53
Mean	30.04
Std Dev	6.521

**Gaus mean : 31.8310**

**Gaus Width: 3.0215**



# B1L101S, U22-ch19, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	84
Mean	37.8
Std Dev	3.696

**Gaus mean : 37.8519**

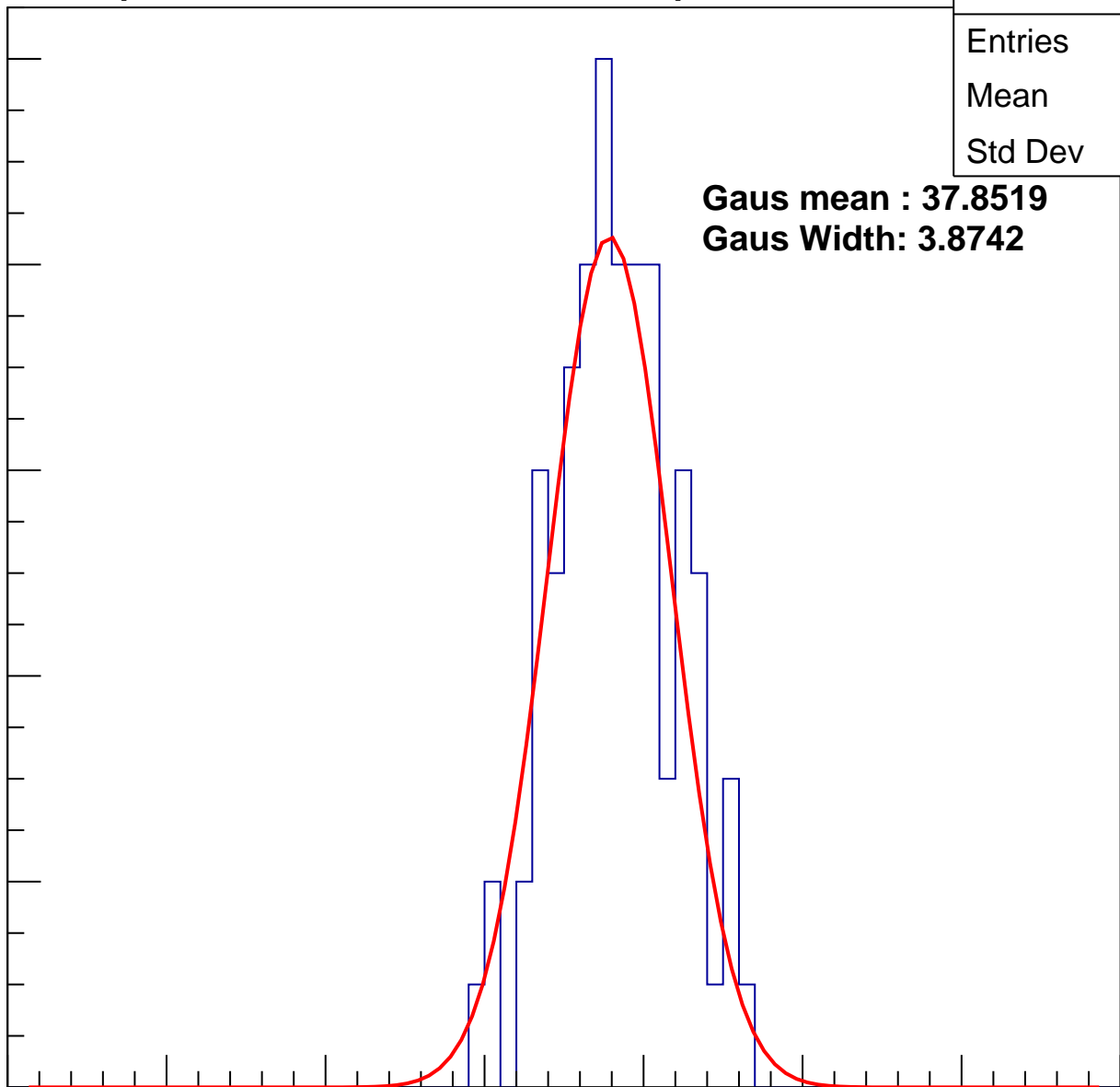
**Gaus Width: 3.8742**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B1L101S, U22-ch19, adc2

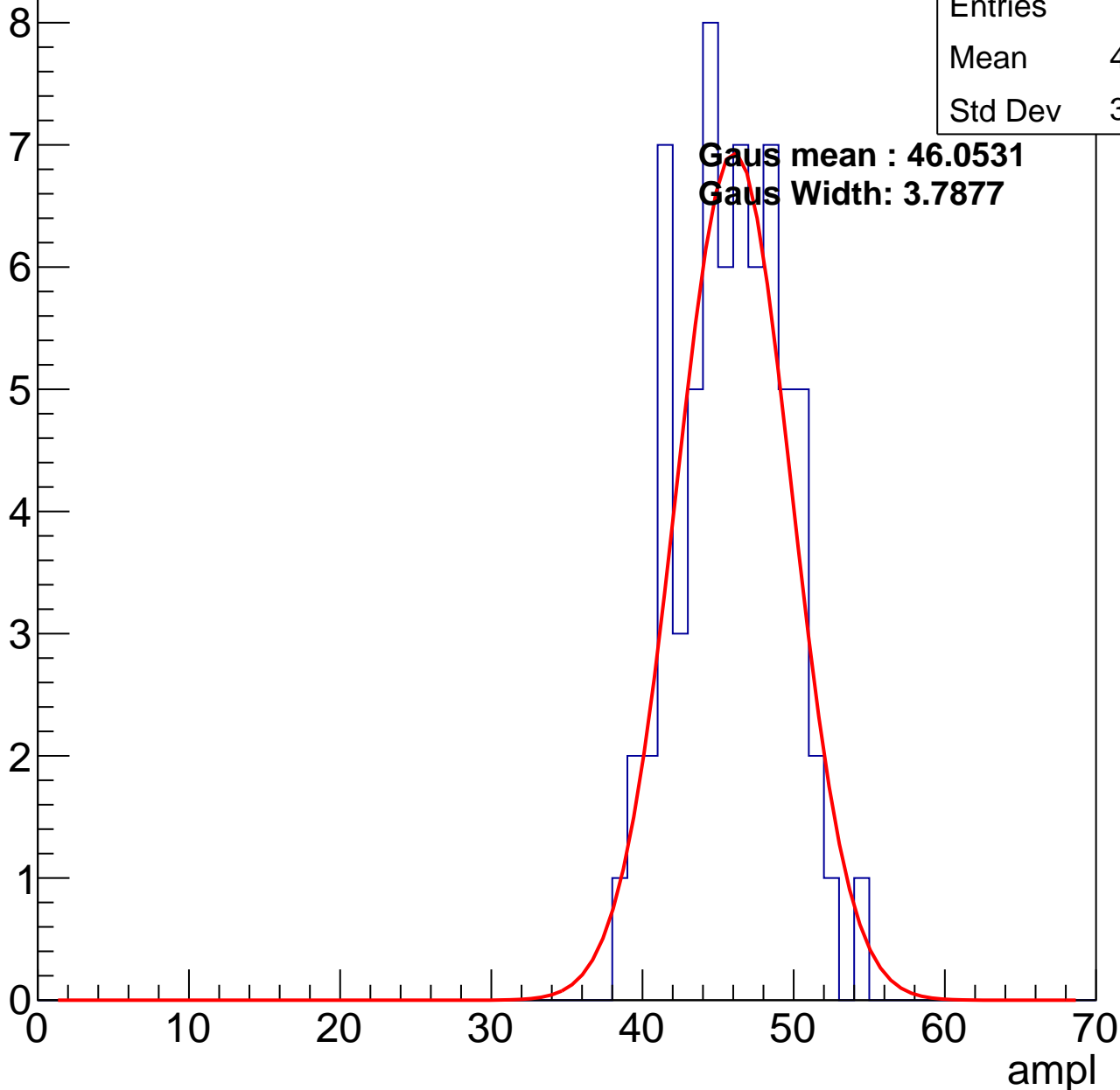
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	45.43
Std Dev	3.487

Gaus mean : 46.0531

Gaus Width: 3.7877

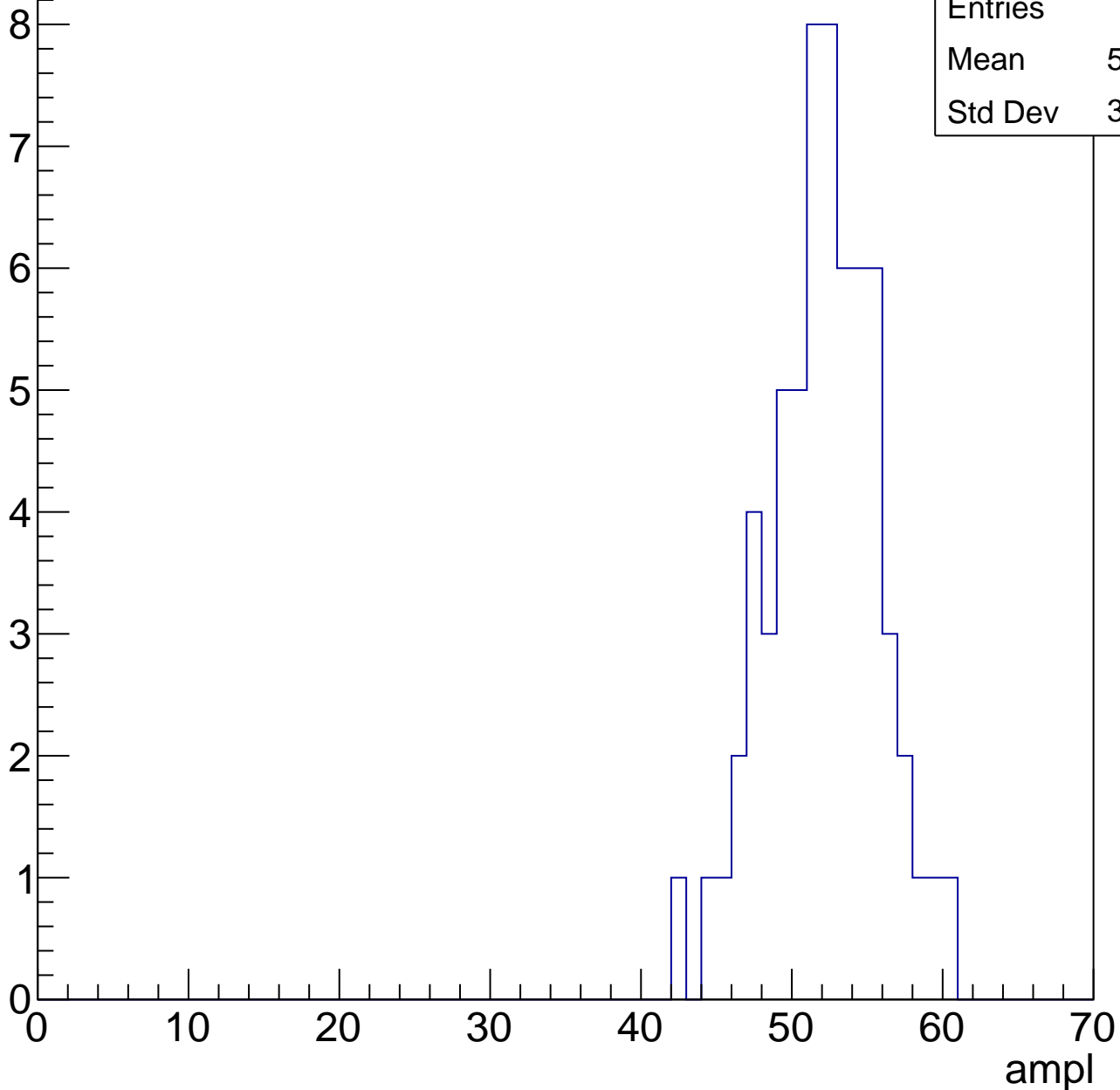


# B1L101S, U22-ch19, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	51.64
Std Dev	3.598

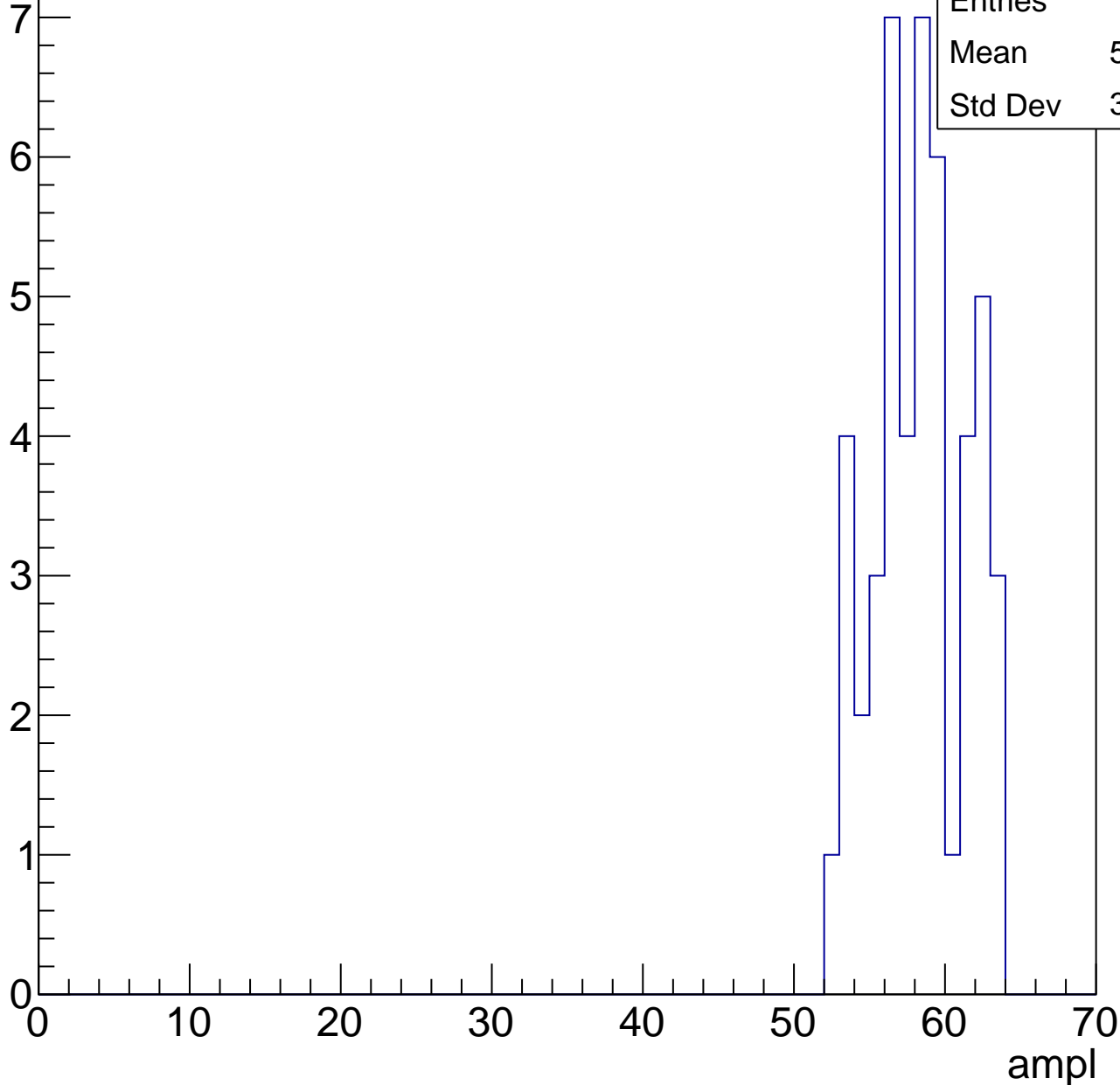


# B1L101S, U22-ch19, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	47
Mean	57.87
Std Dev	3.015

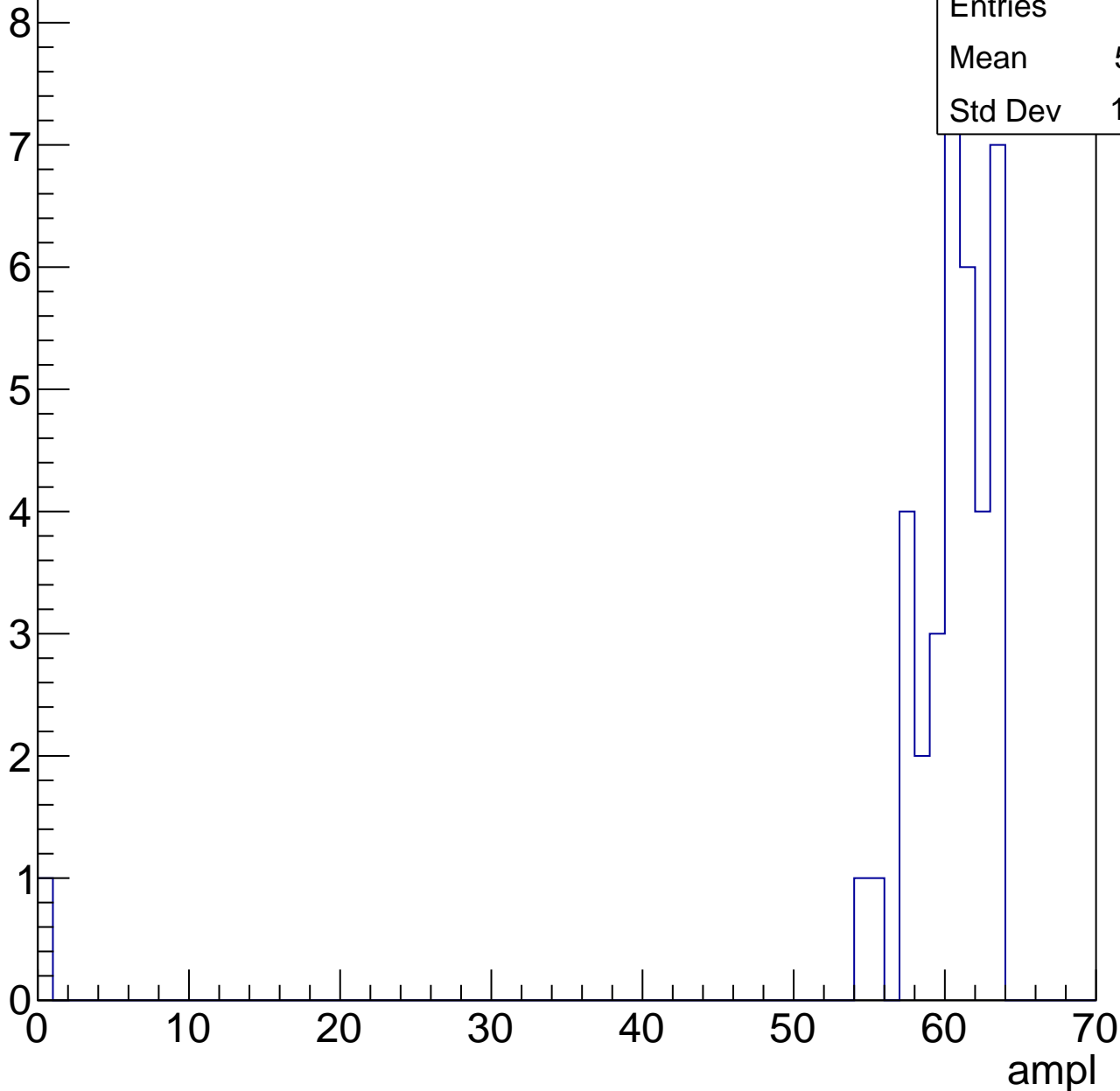


# B1L101S, U22-ch19, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	37
Mean	58.51
Std Dev	10.02



# B1L101S, U22-ch19, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U22-ch19, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U22-ch20, adc0

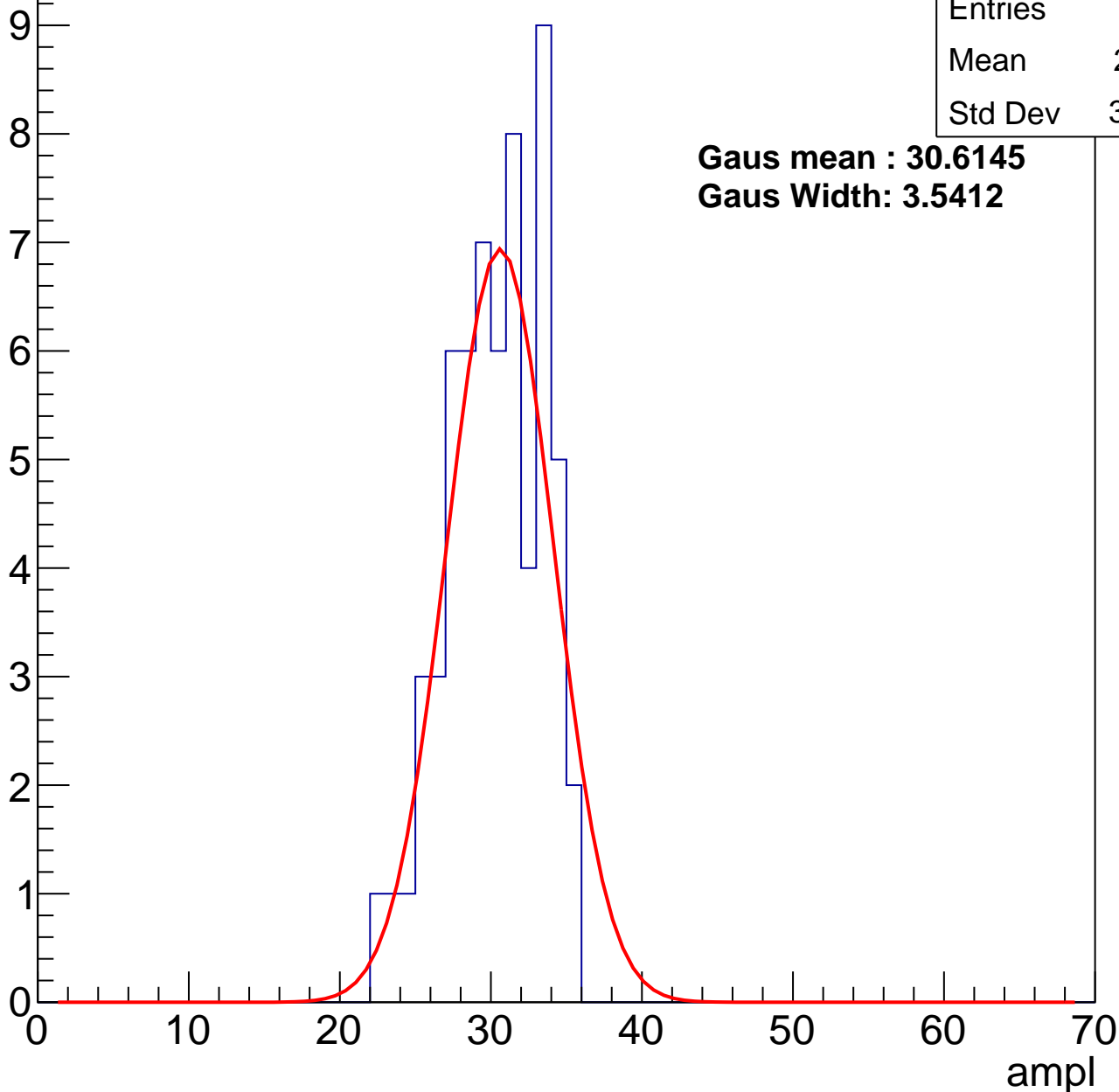
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	29.81
Std Dev	3.084

**Gaus mean : 30.6145**

**Gaus Width: 3.5412**



# B1L101S, U22-ch20, adc1

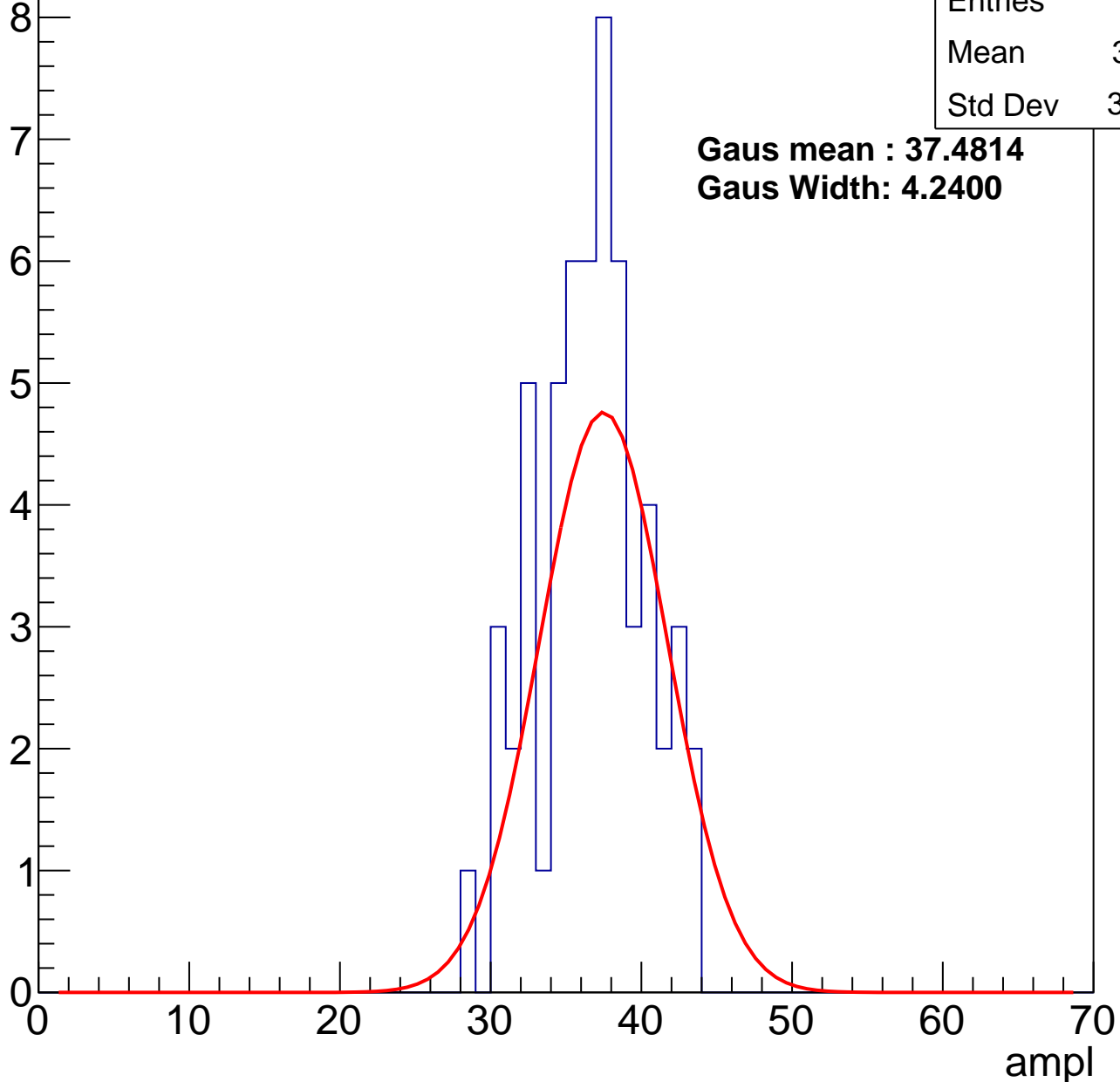
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	57
Mean	36.21
Std Dev	3.538

**Gaus mean : 37.4814**

**Gaus Width: 4.2400**



# B1L101S, U22-ch20, adc2

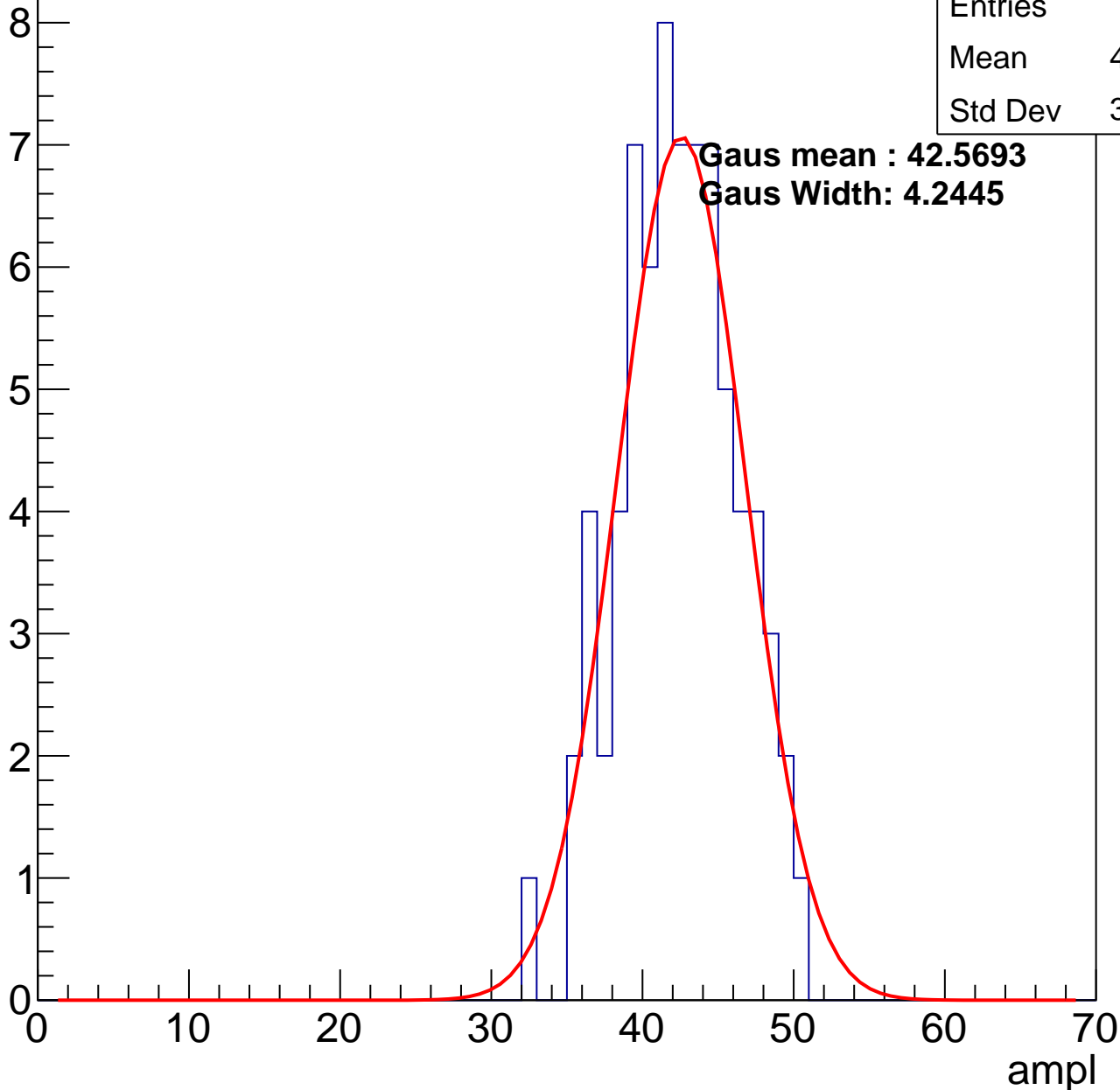
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	74
Mean	41.96
Std Dev	3.793

**Gaus mean : 42.5693**

**Gaus Width: 4.2445**

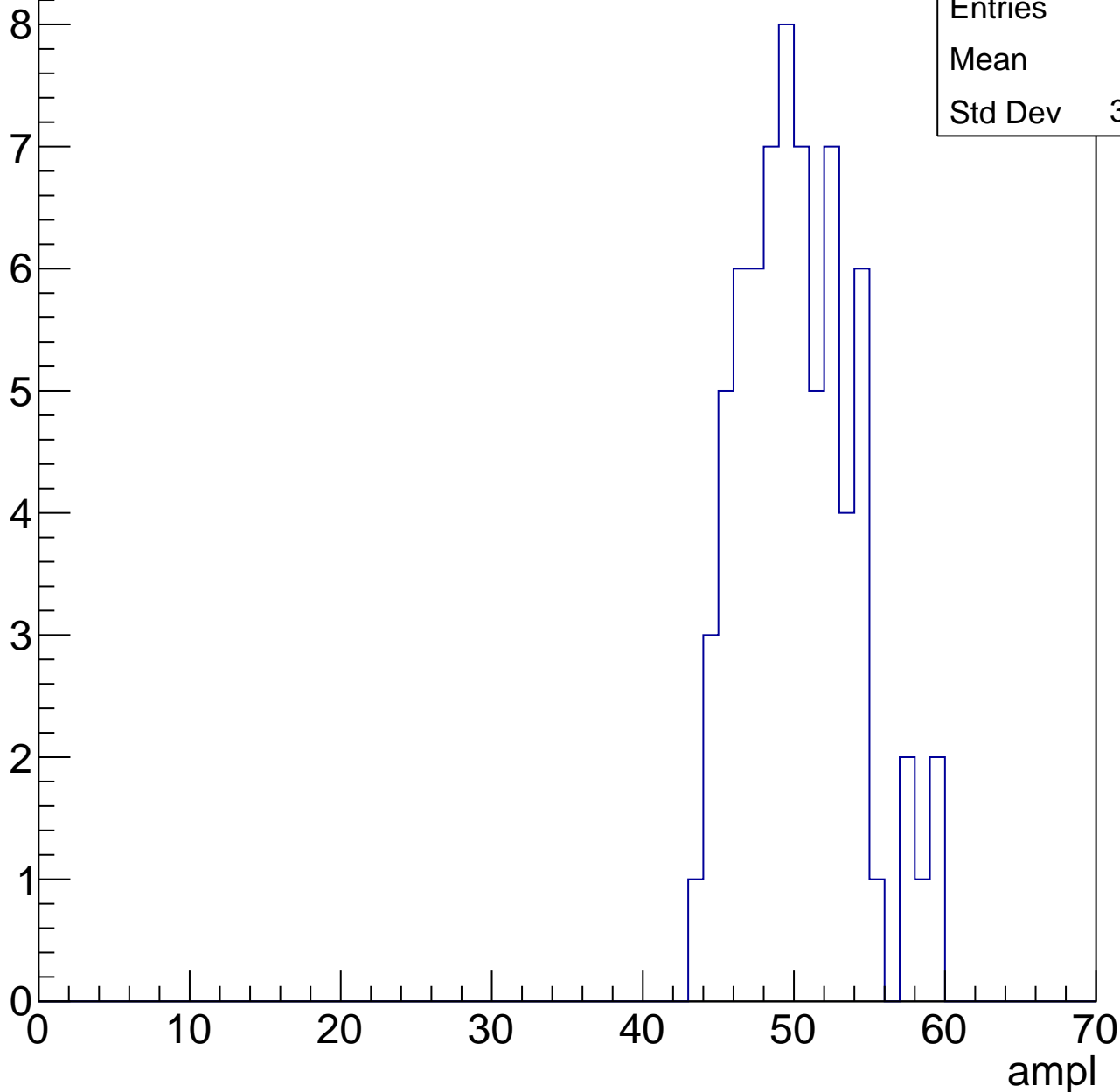


# B1L101S, U22-ch20, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	71
Mean	49.8
Std Dev	3.714

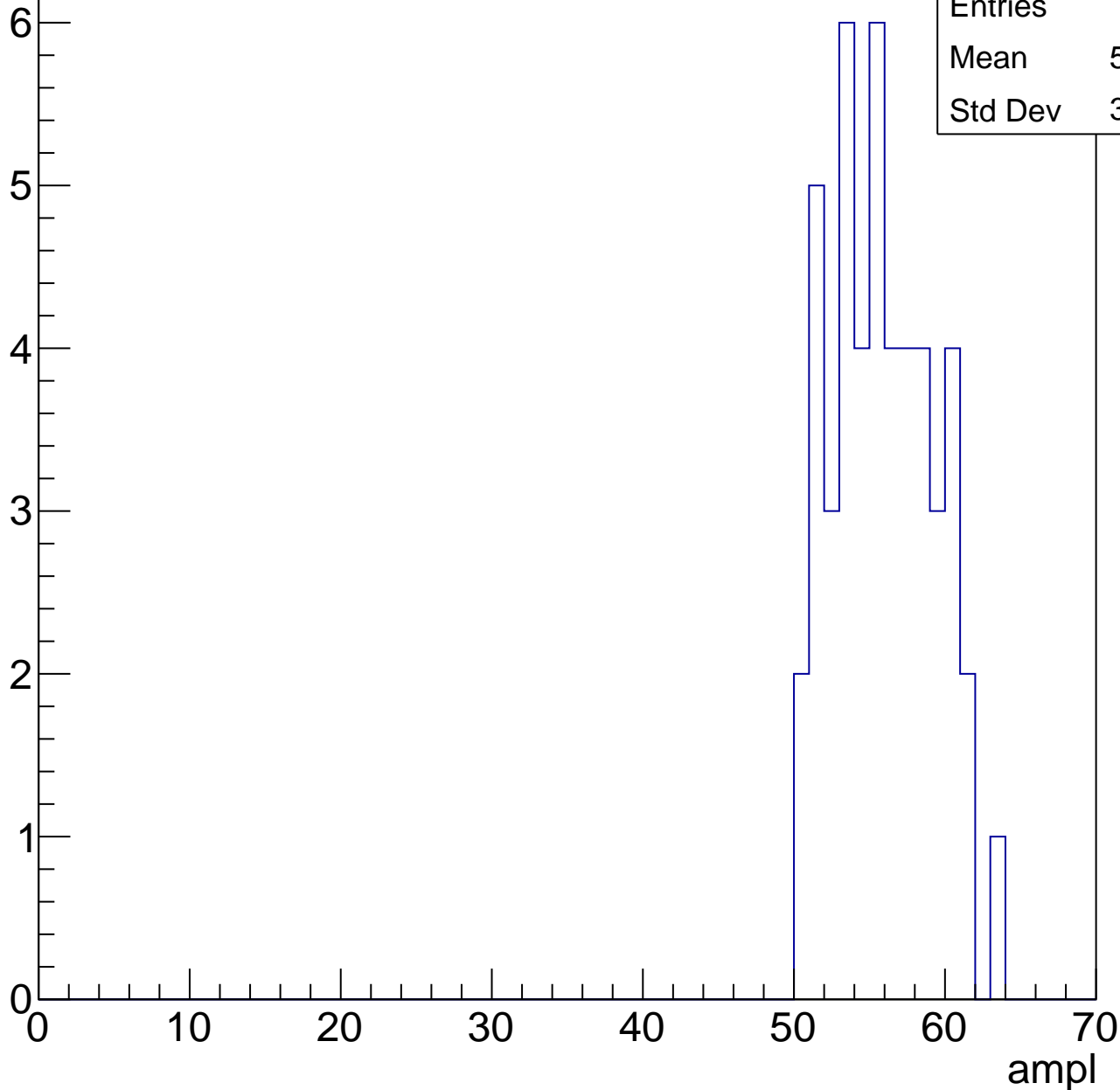


# B1L101S, U22-ch20, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	48
Mean	55.44
Std Dev	3.278

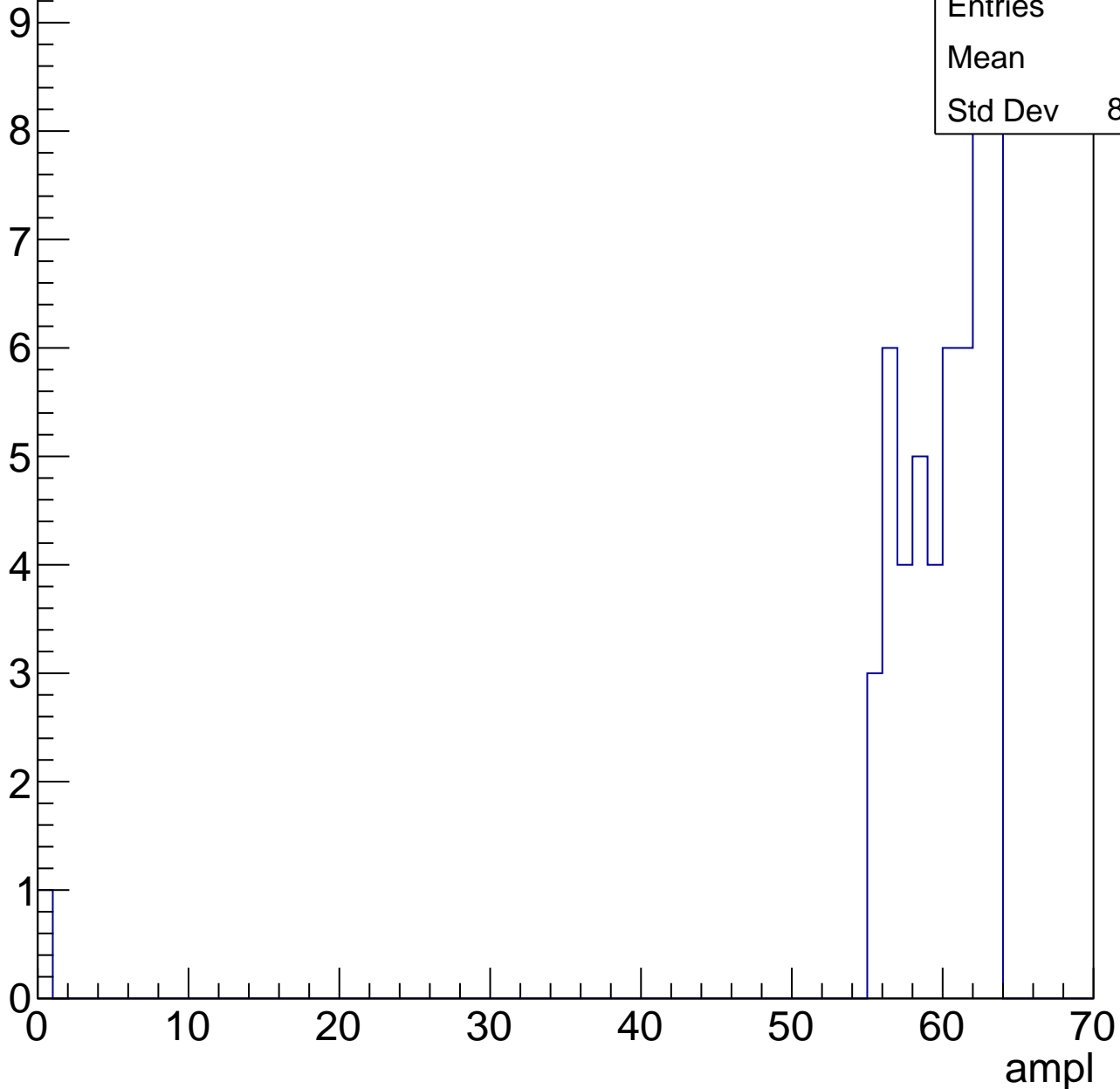


# B1L101S, U22-ch20, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

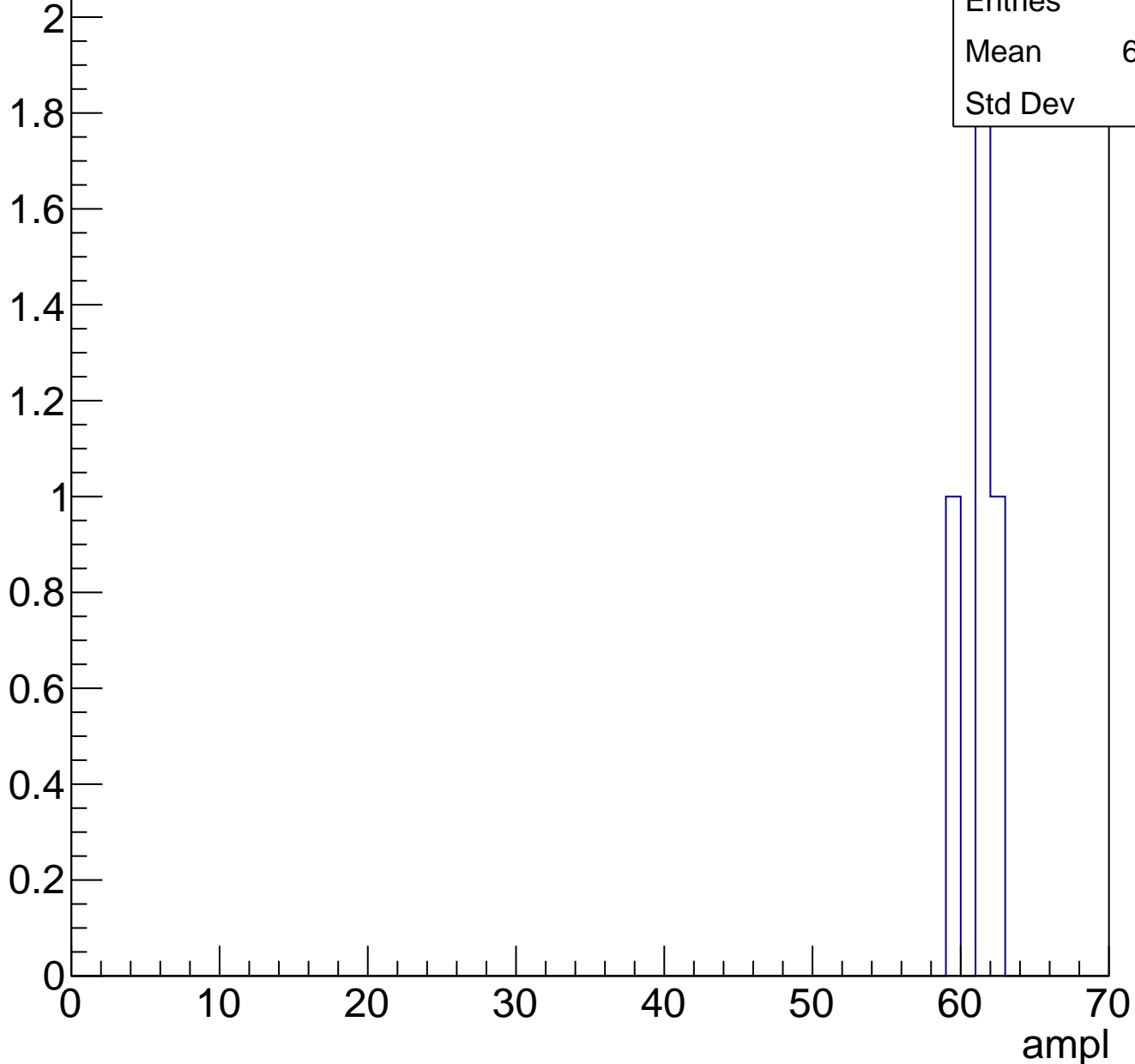
Entries	53
Mean	58.6
Std Dev	8.524



# B1L101S, U22-ch20, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U22-ch20, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U22-ch21, adc0

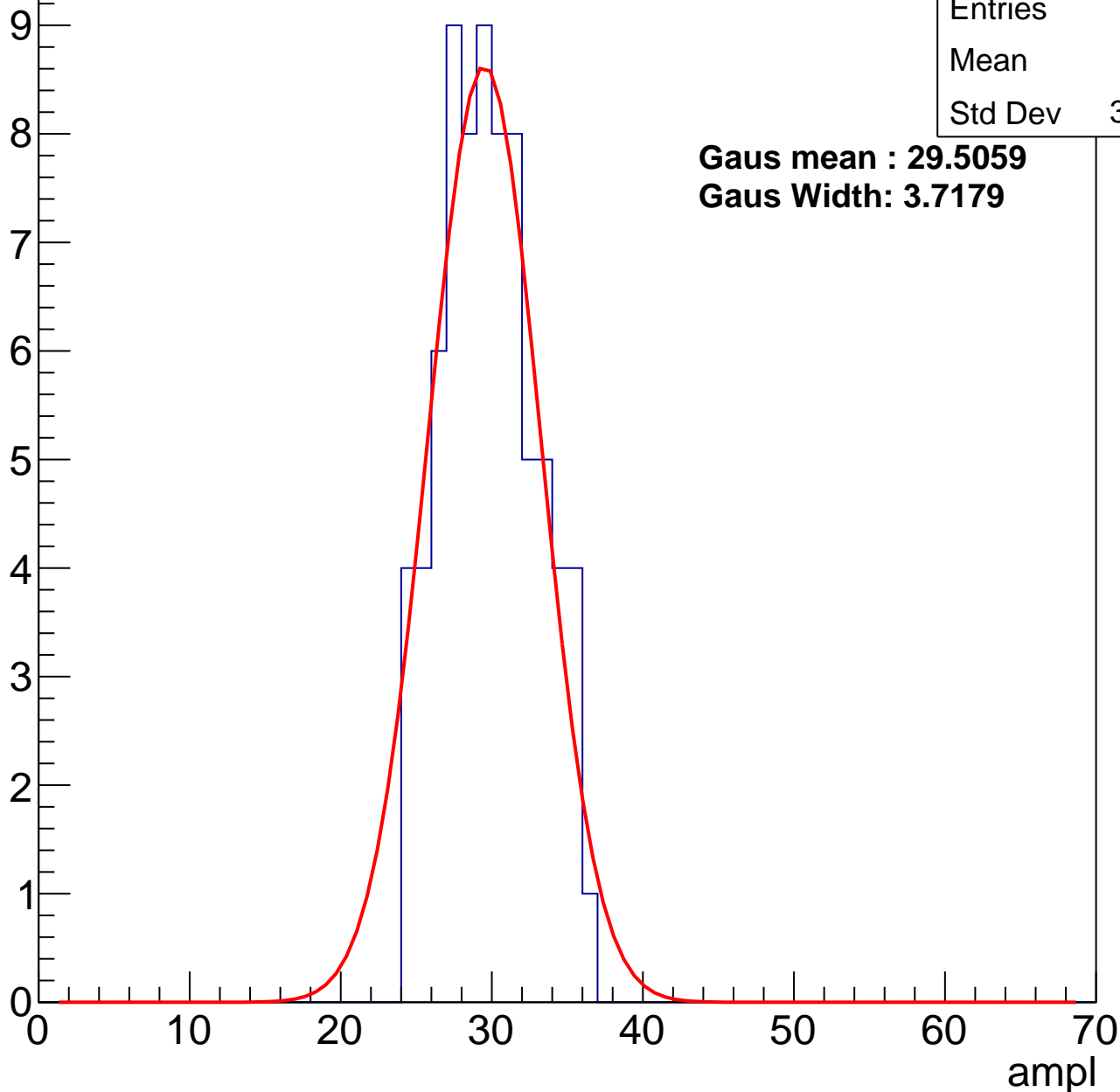
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	75
Mean	29.4
Std Dev	3.072

**Gaus mean : 29.5059**

**Gaus Width: 3.7179**



# B1L101S, U22-ch21, adc1

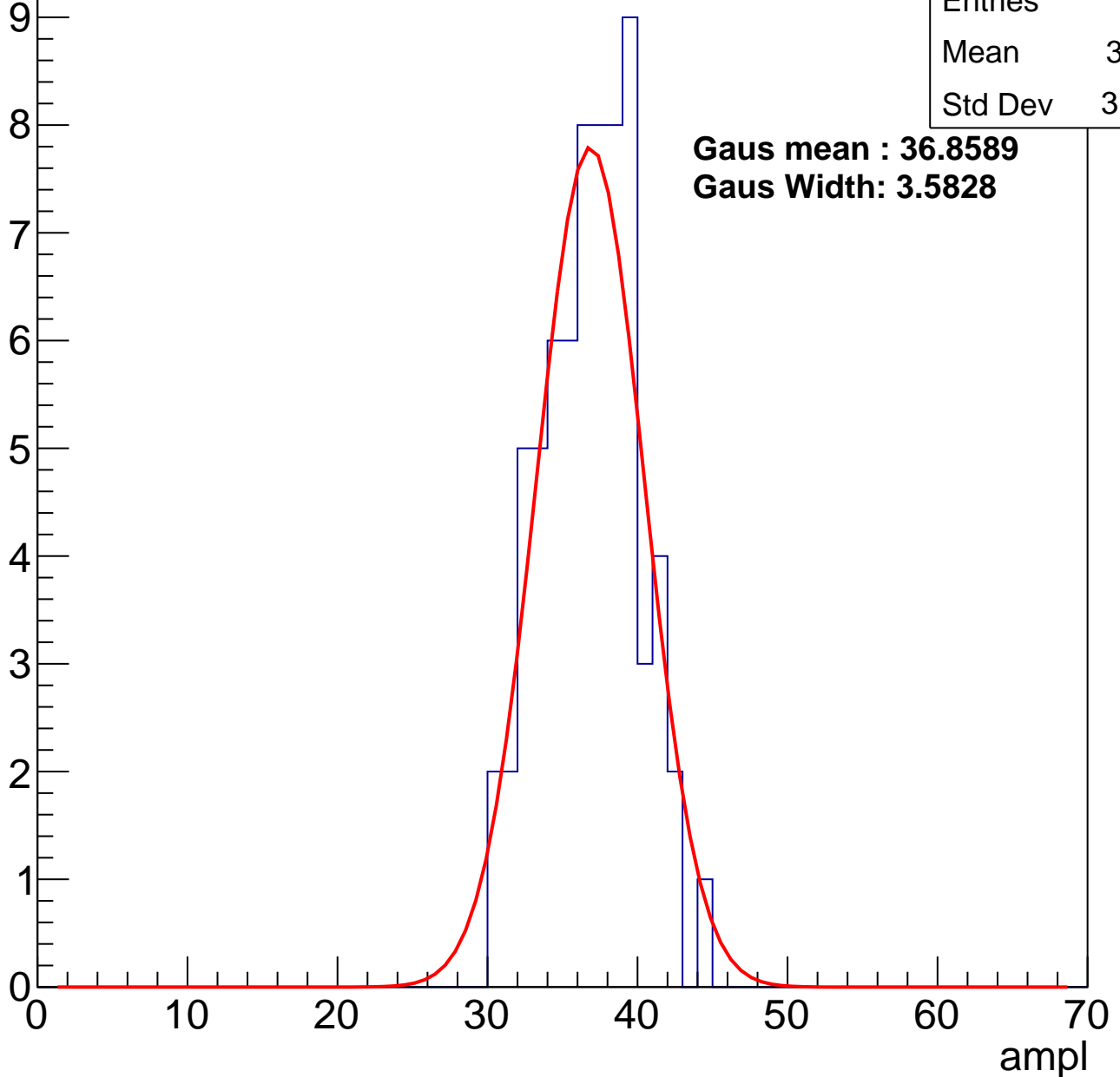
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	36.41
Std Dev	3.118

**Gaus mean : 36.8589**

**Gaus Width: 3.5828**



# B1L101S, U22-ch21, adc2

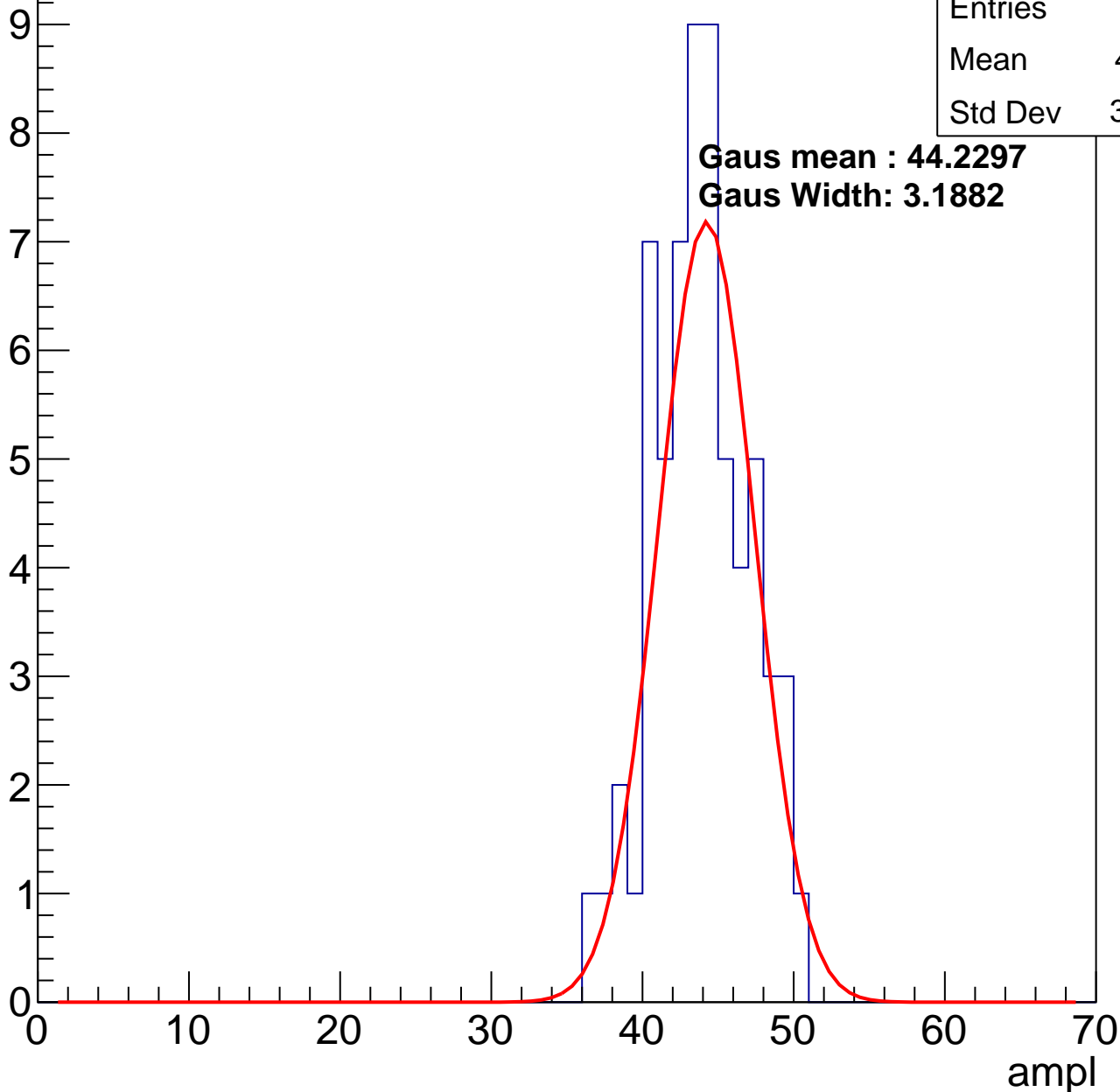
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	43.41
Std Dev	3.105

**Gaus mean : 44.2297**

**Gaus Width: 3.1882**

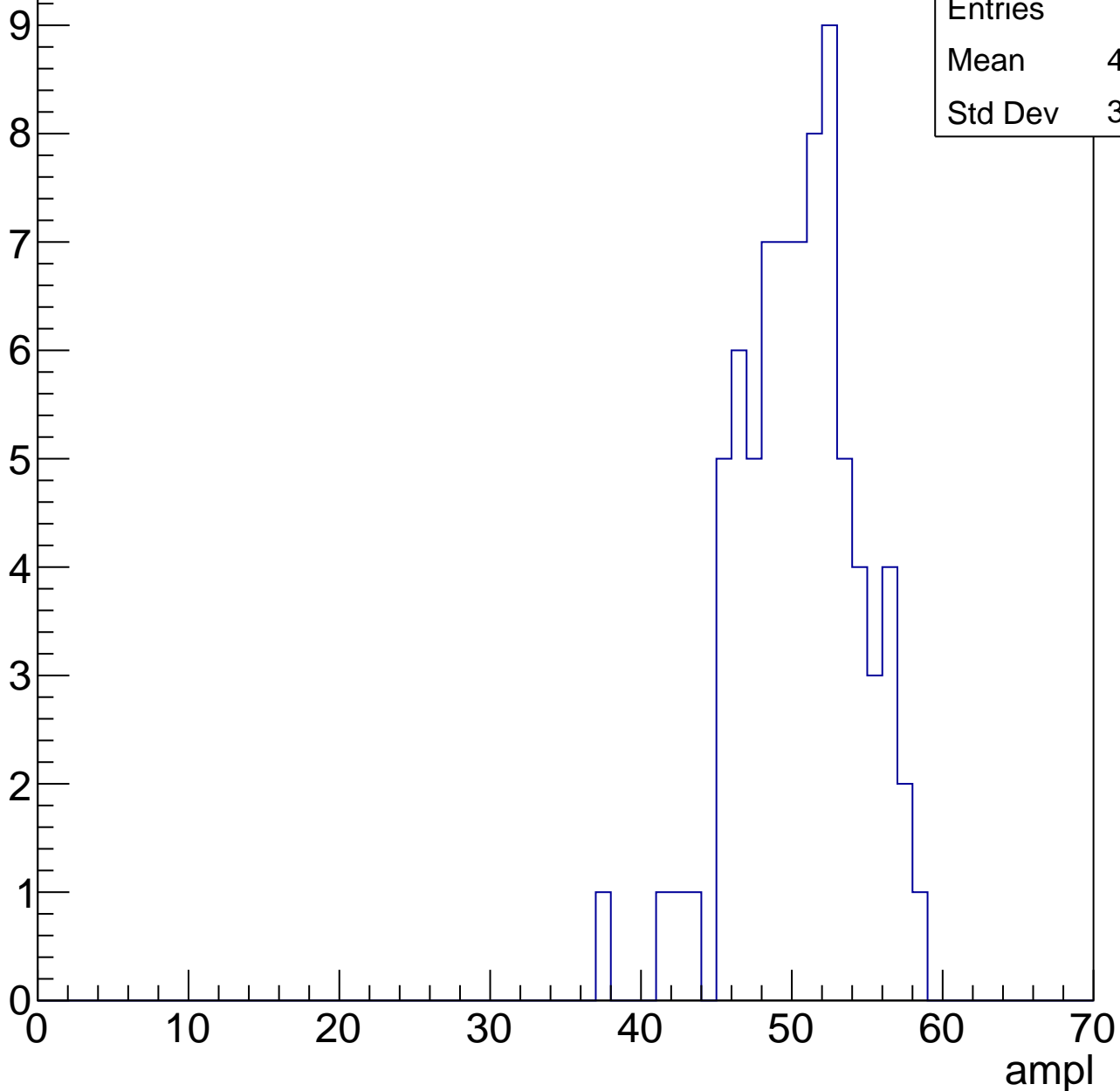


# B1L101S, U22-ch21, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	77
Mean	49.95
Std Dev	3.944



# B1L101S, U22-ch21, adc4

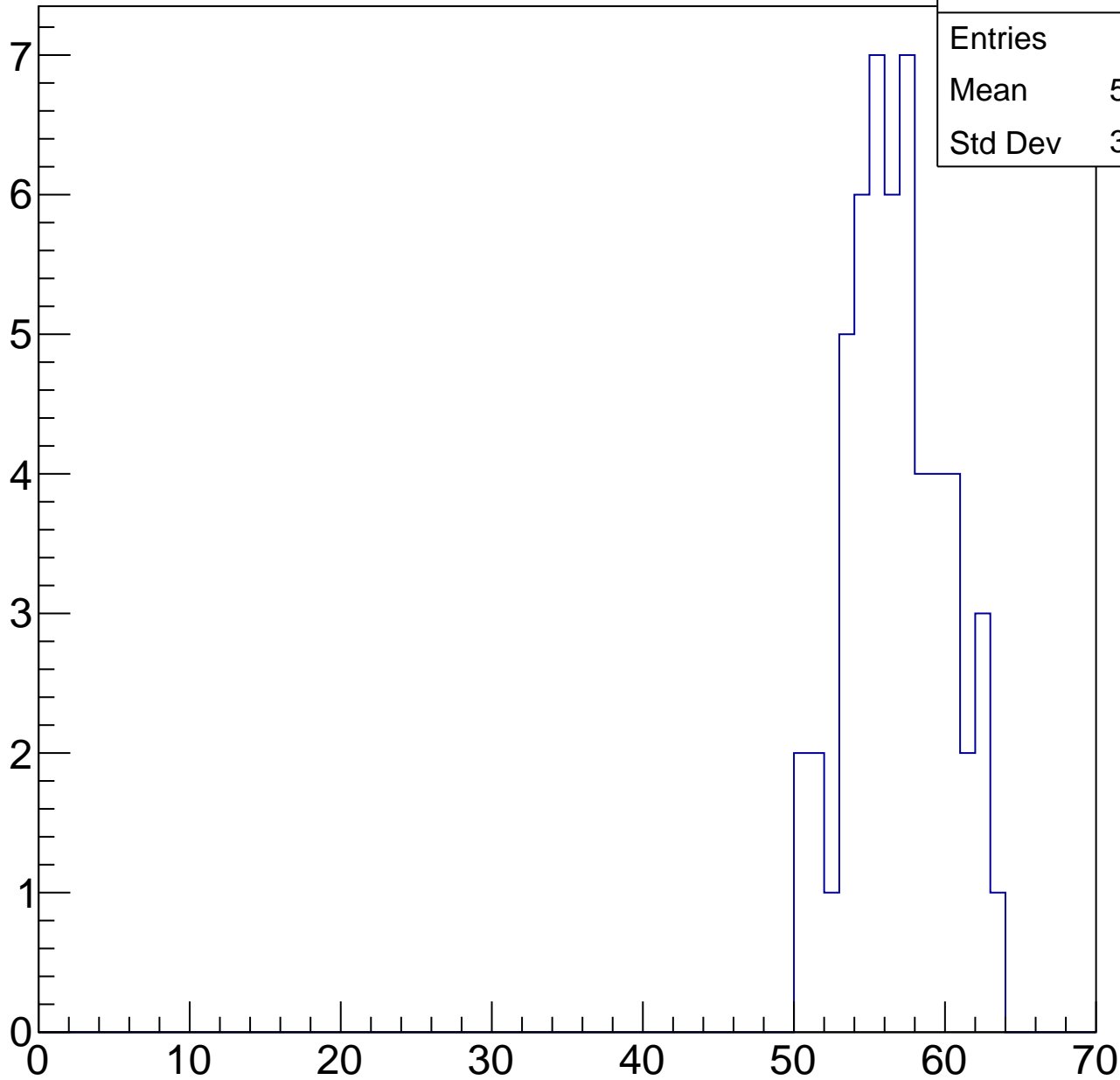
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

7  
6  
5  
4  
3  
2  
1  
0

Entries	54
Mean	56.33
Std Dev	3.156

ampl

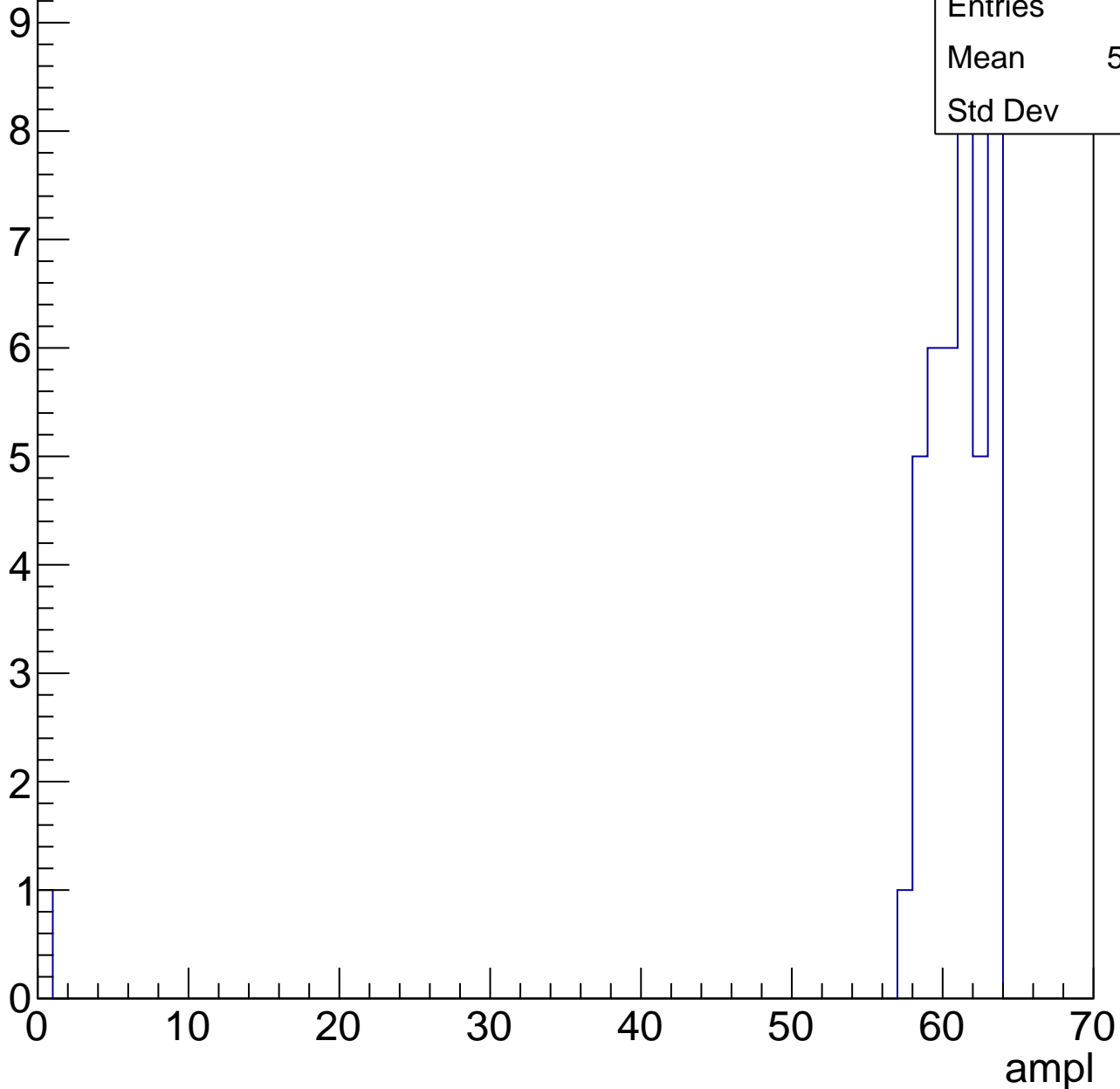


# B1L101S, U22-ch21, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	41
Mean	59.17
Std Dev	9.52



# B1L101S, U22-ch21, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U22-ch21, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	3
Mean	7
Std Dev	9.899

# B1L101S, U22-ch22, adc0

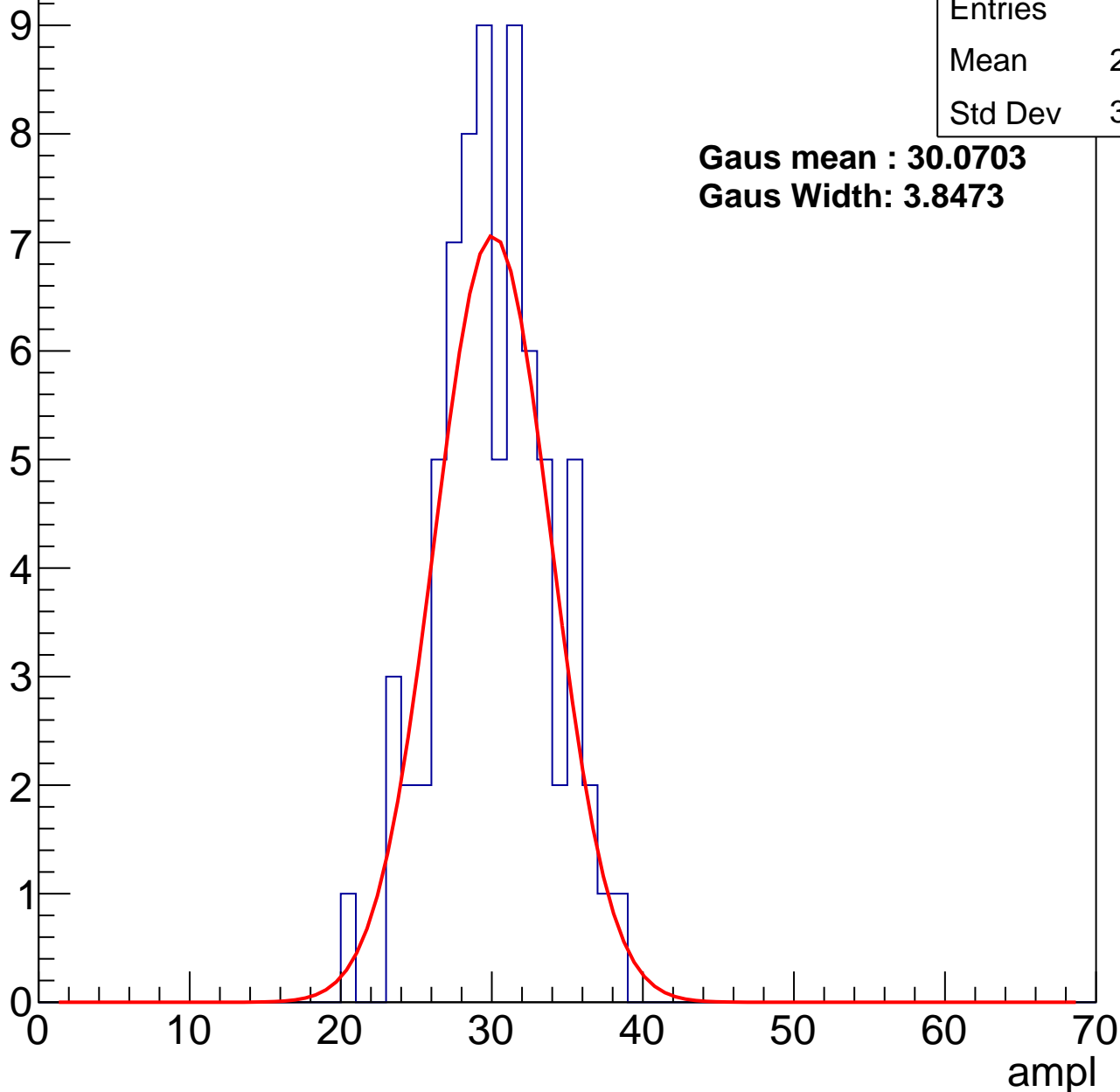
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	73
Mean	29.68
Std Dev	3.637

**Gaus mean : 30.0703**

**Gaus Width: 3.8473**



# B1L101S, U22-ch22, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	74
Mean	36.65
Std Dev	5.544

**Gaus mean : 37.2297**

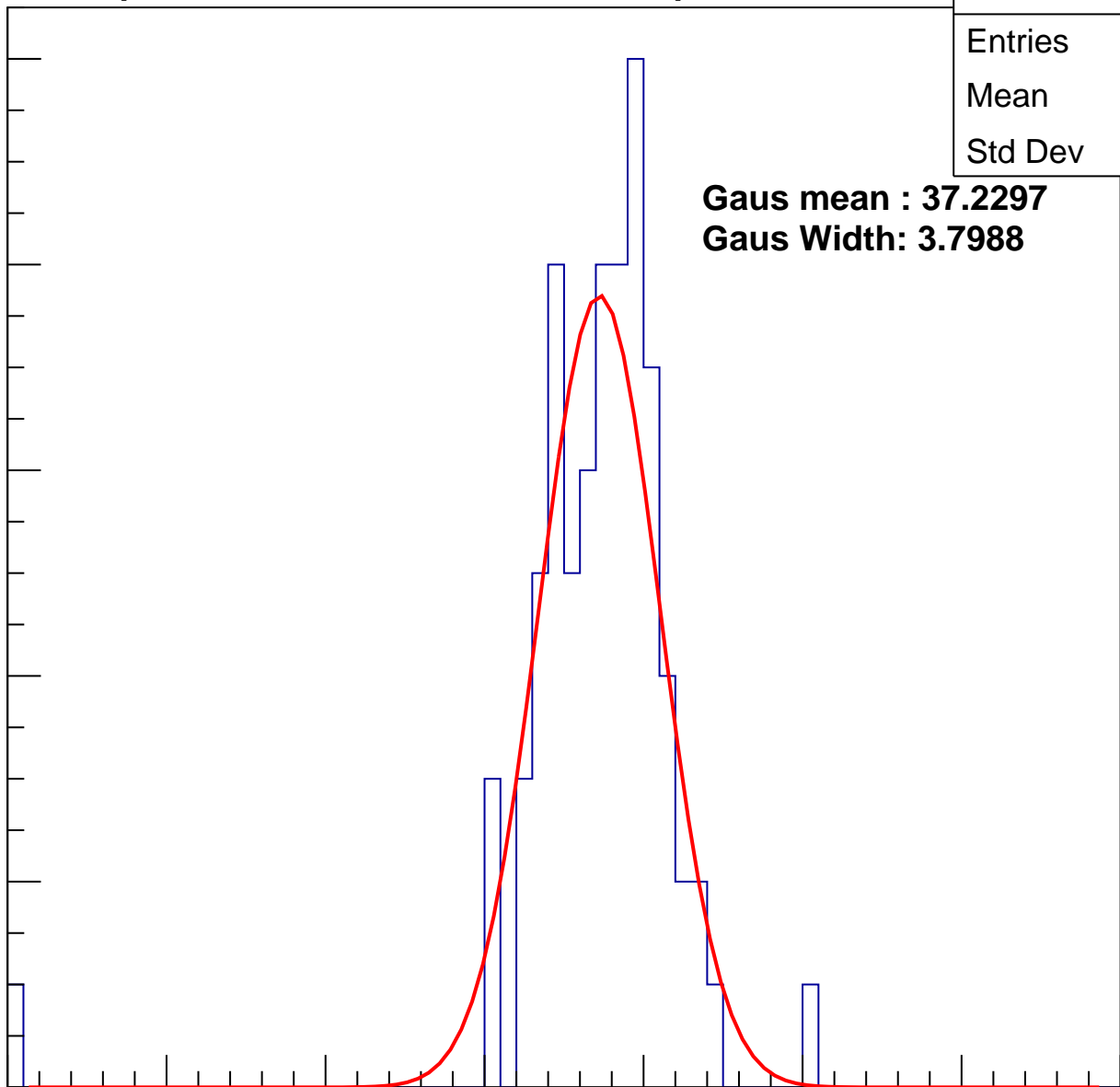
**Gaus Width: 3.7988**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U22-ch22, adc2

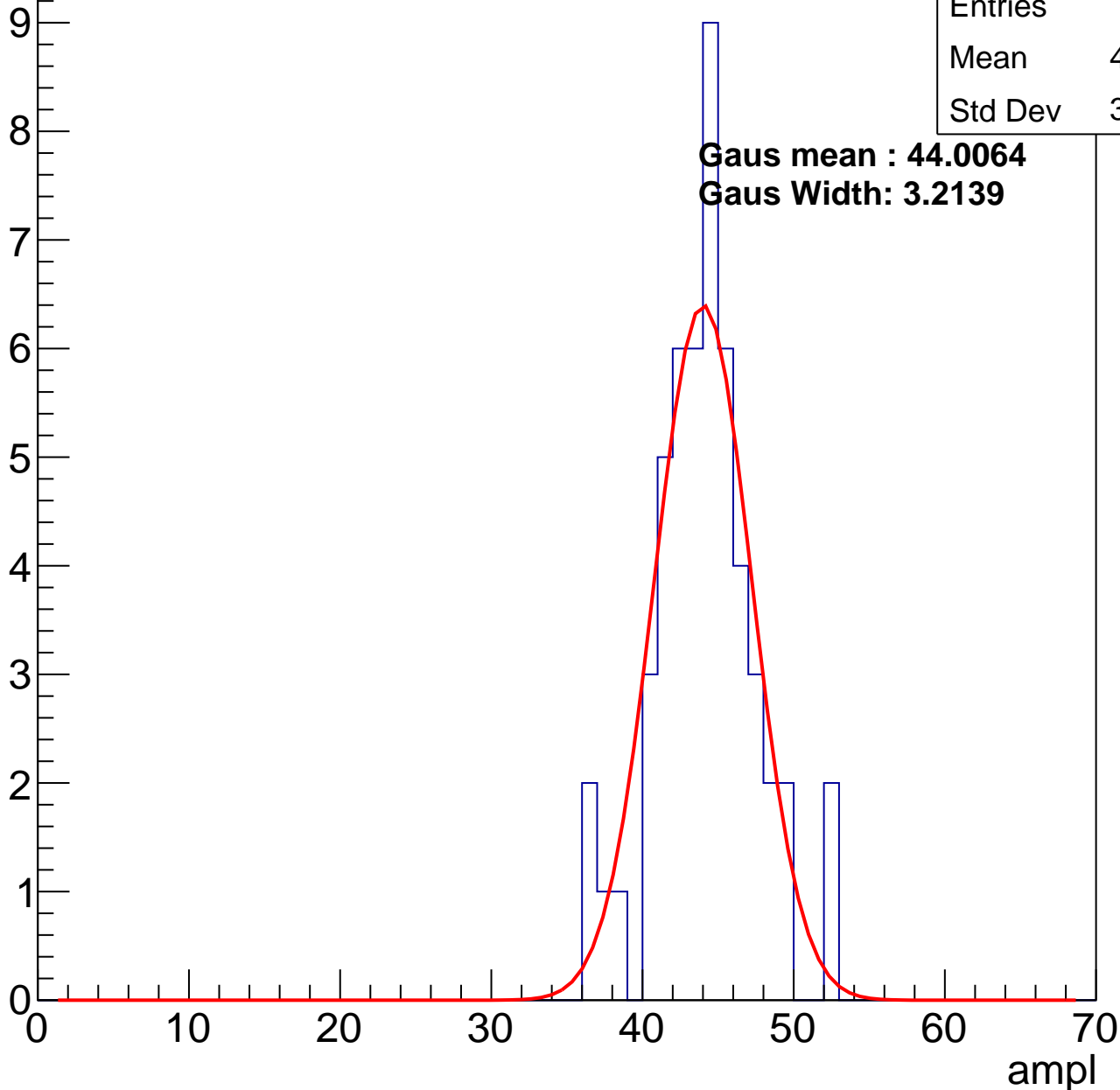
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	52
Mean	43.67
Std Dev	3.367

**Gaus mean : 44.0064**

**Gaus Width: 3.2139**

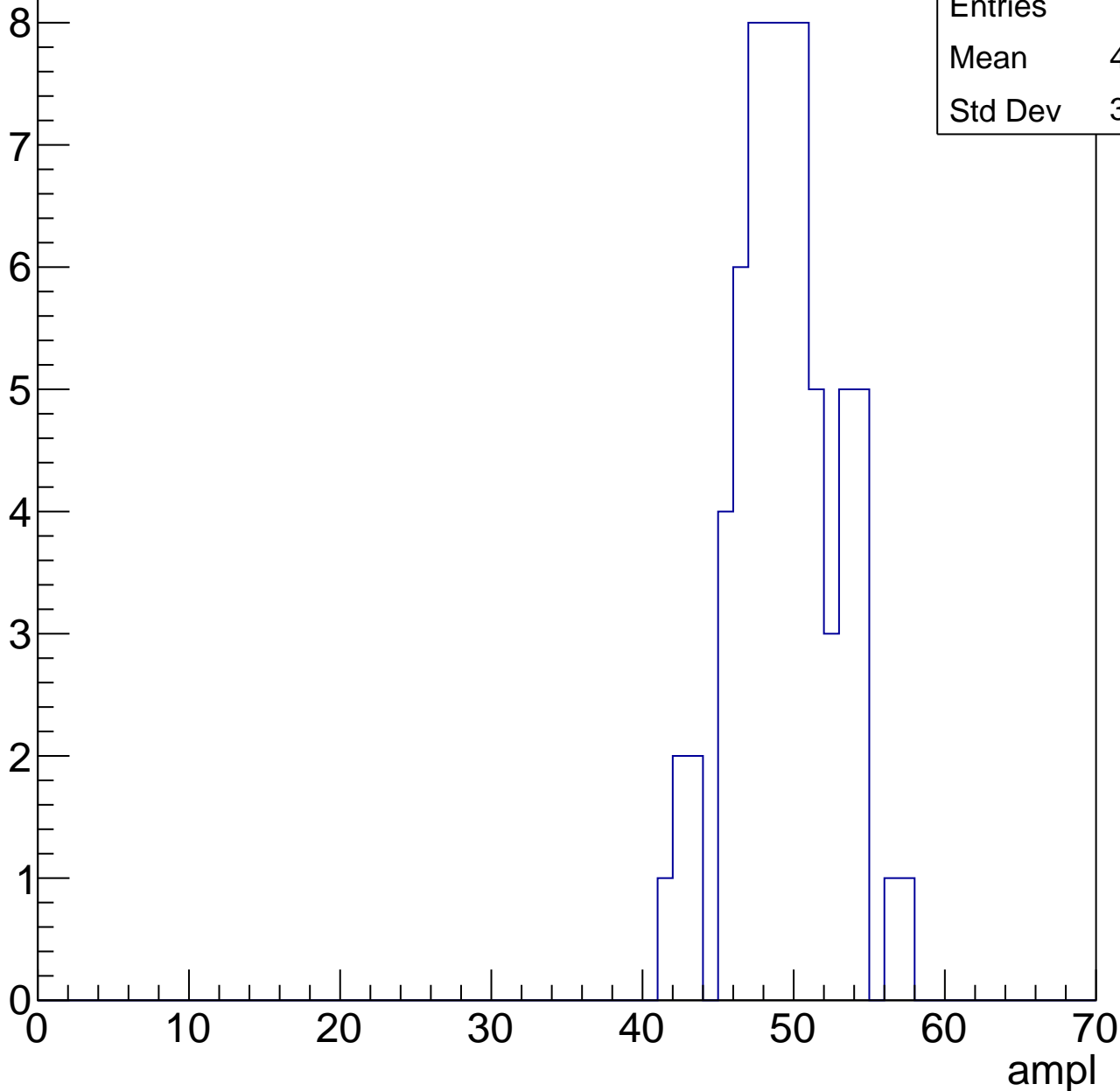


# B1L101S, U22-ch22, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	67
Mean	48.93
Std Dev	3.378

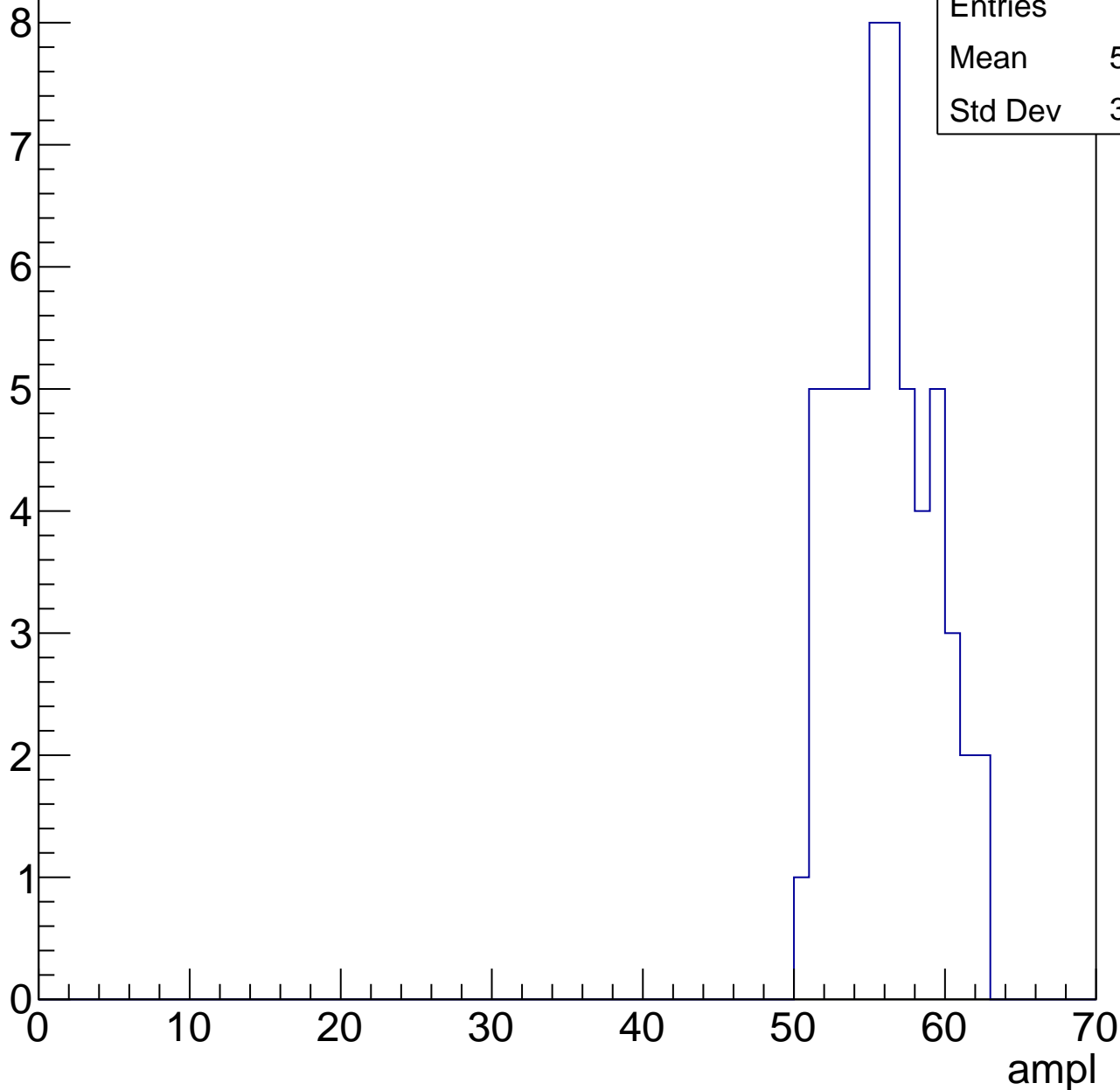


# B1L101S, U22-ch22, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	58
Mean	55.62
Std Dev	3.056

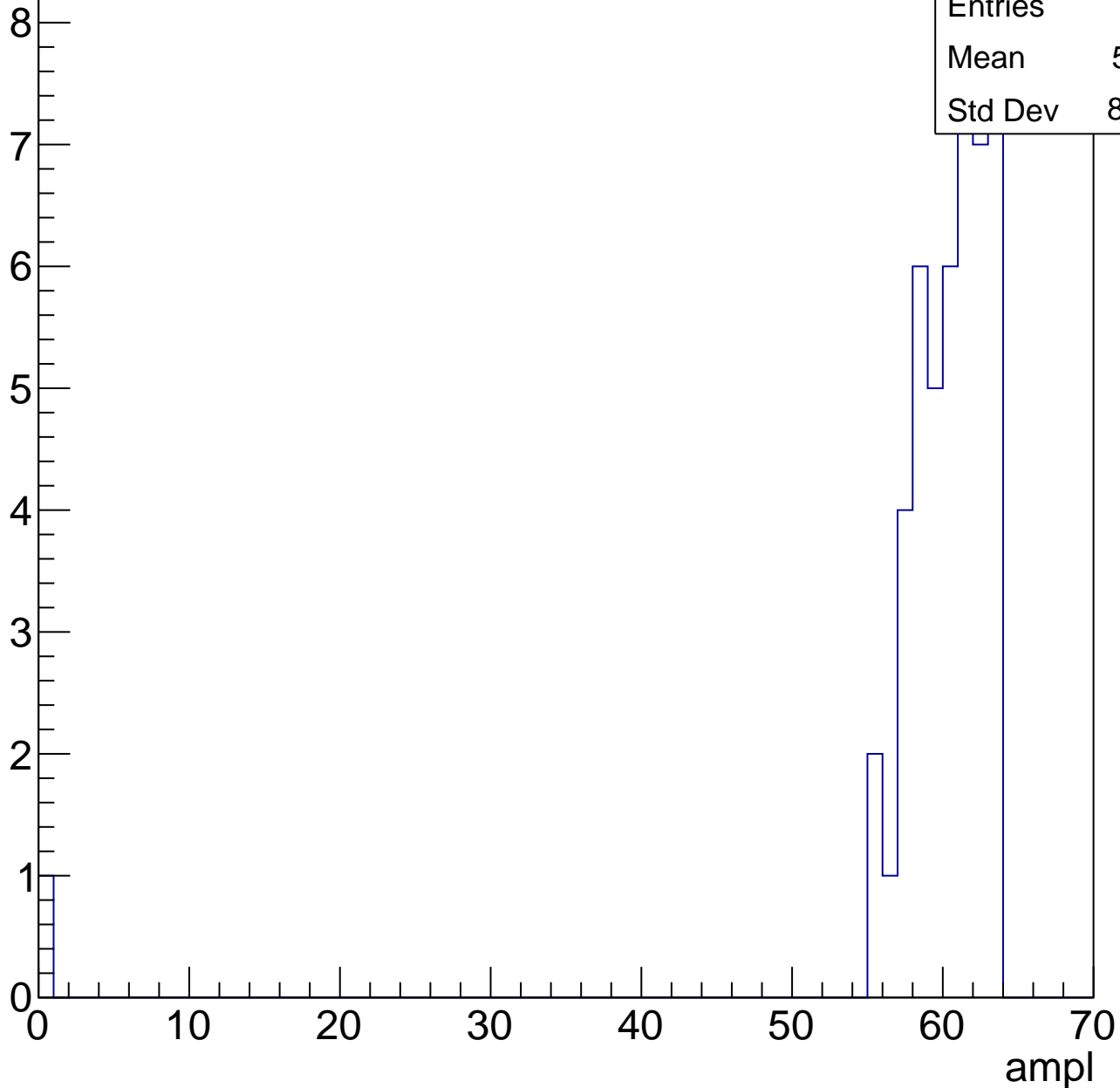


# B1L101S, U22-ch22, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	48
Mean	58.81
Std Dev	8.864



# B1L101S, U22-ch22, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

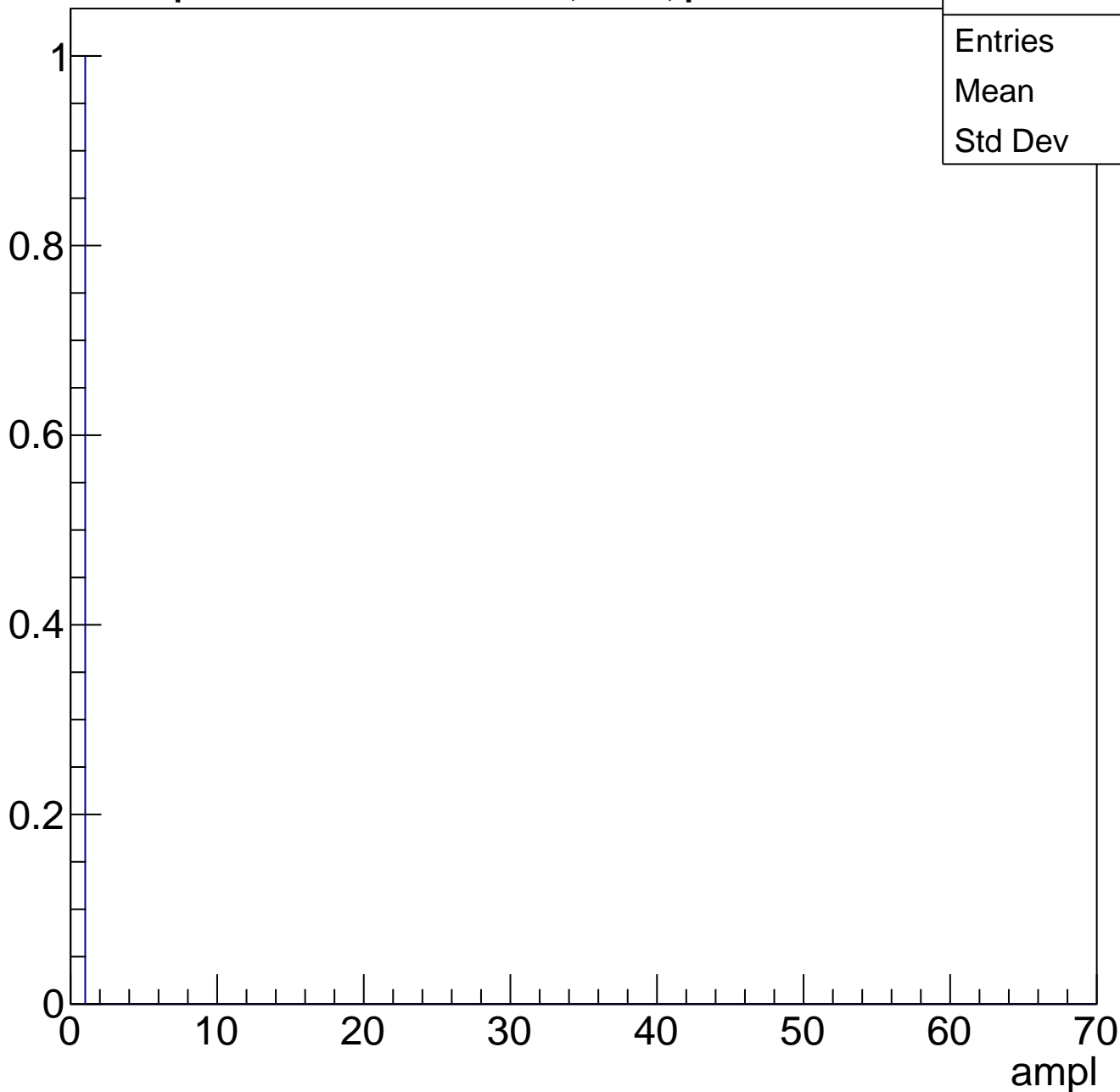




# B1L101S, U22-ch22, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L101S, U22-ch23, adc0

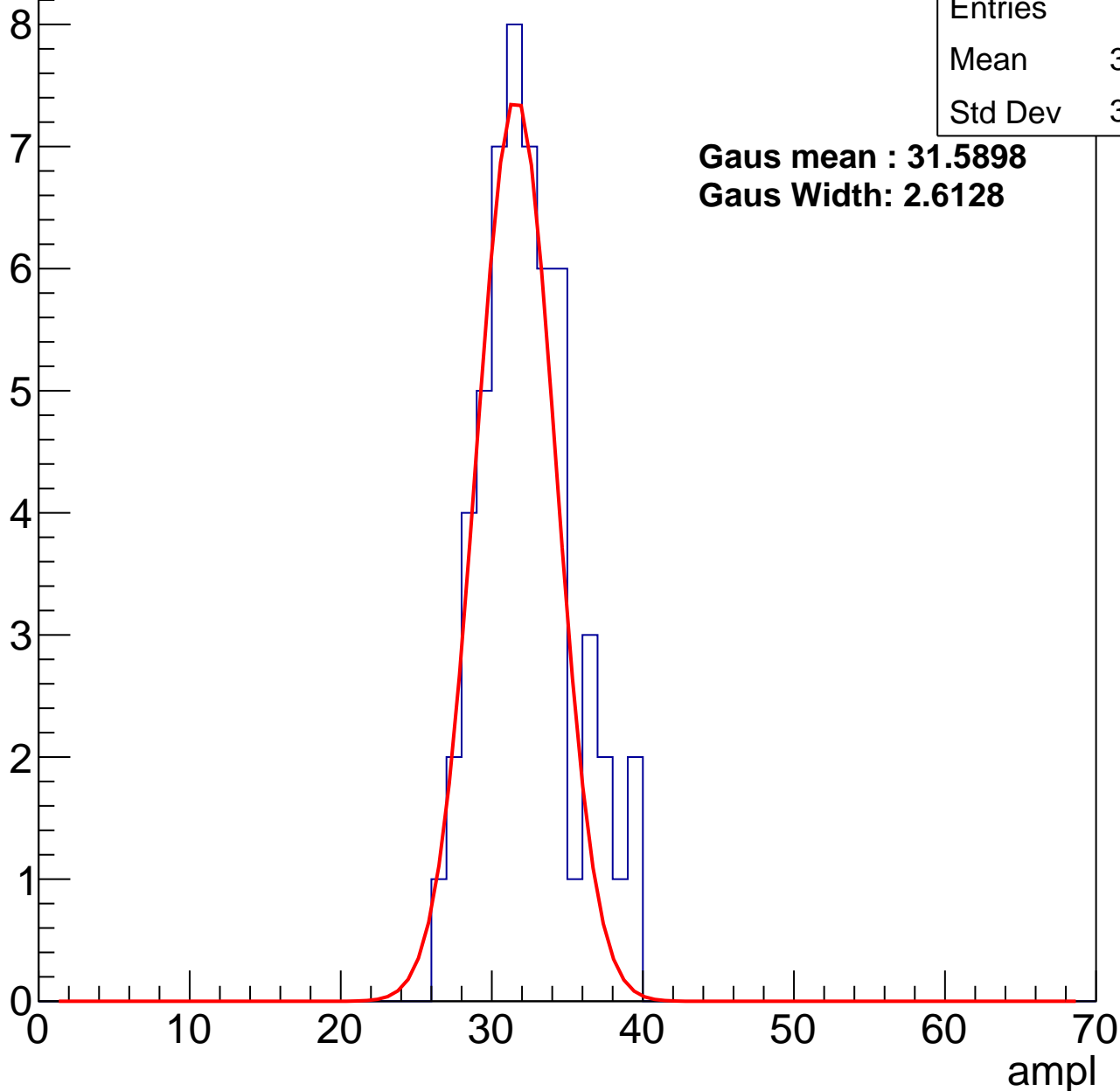
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	55
Mean	31.89
Std Dev	3.019

**Gaus mean : 31.5898**

**Gaus Width: 2.6128**



# B1L101S, U22-ch23, adc1

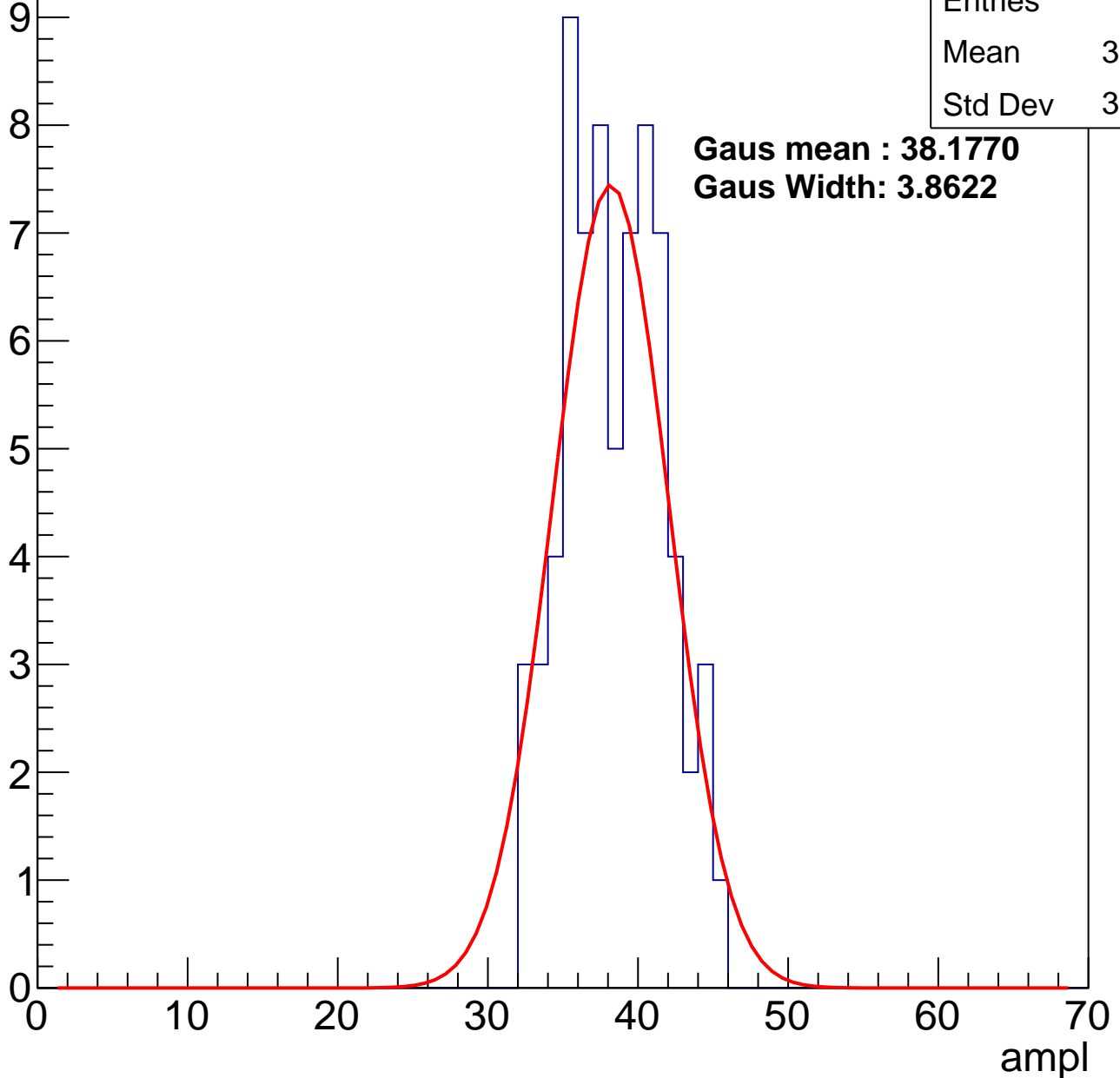
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	71
Mean	37.96
Std Dev	3.222

**Gaus mean : 38.1770**

**Gaus Width: 3.8622**



# B1L101S, U22-ch23, adc2

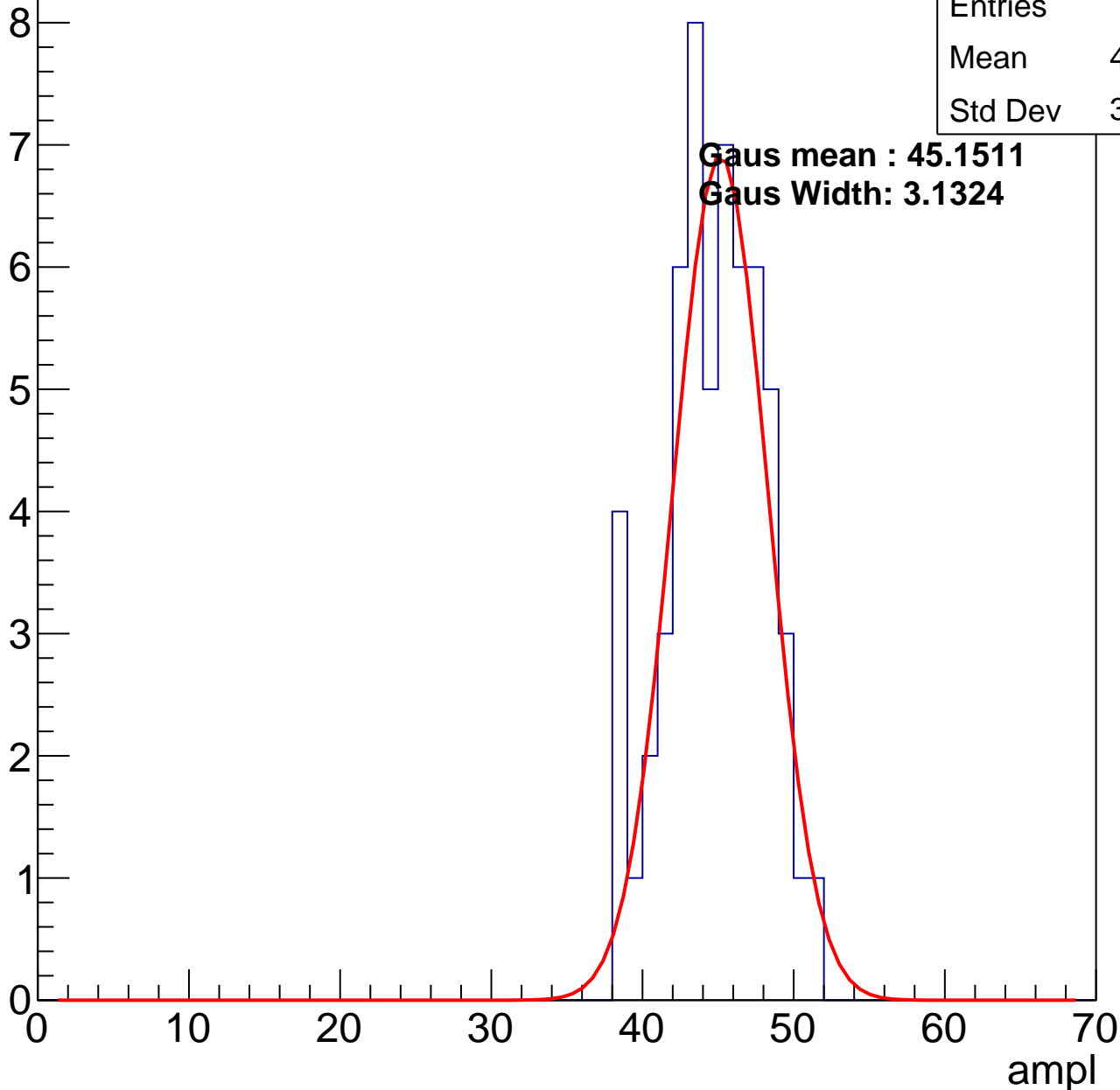
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	58
Mean	44.33
Std Dev	3.159

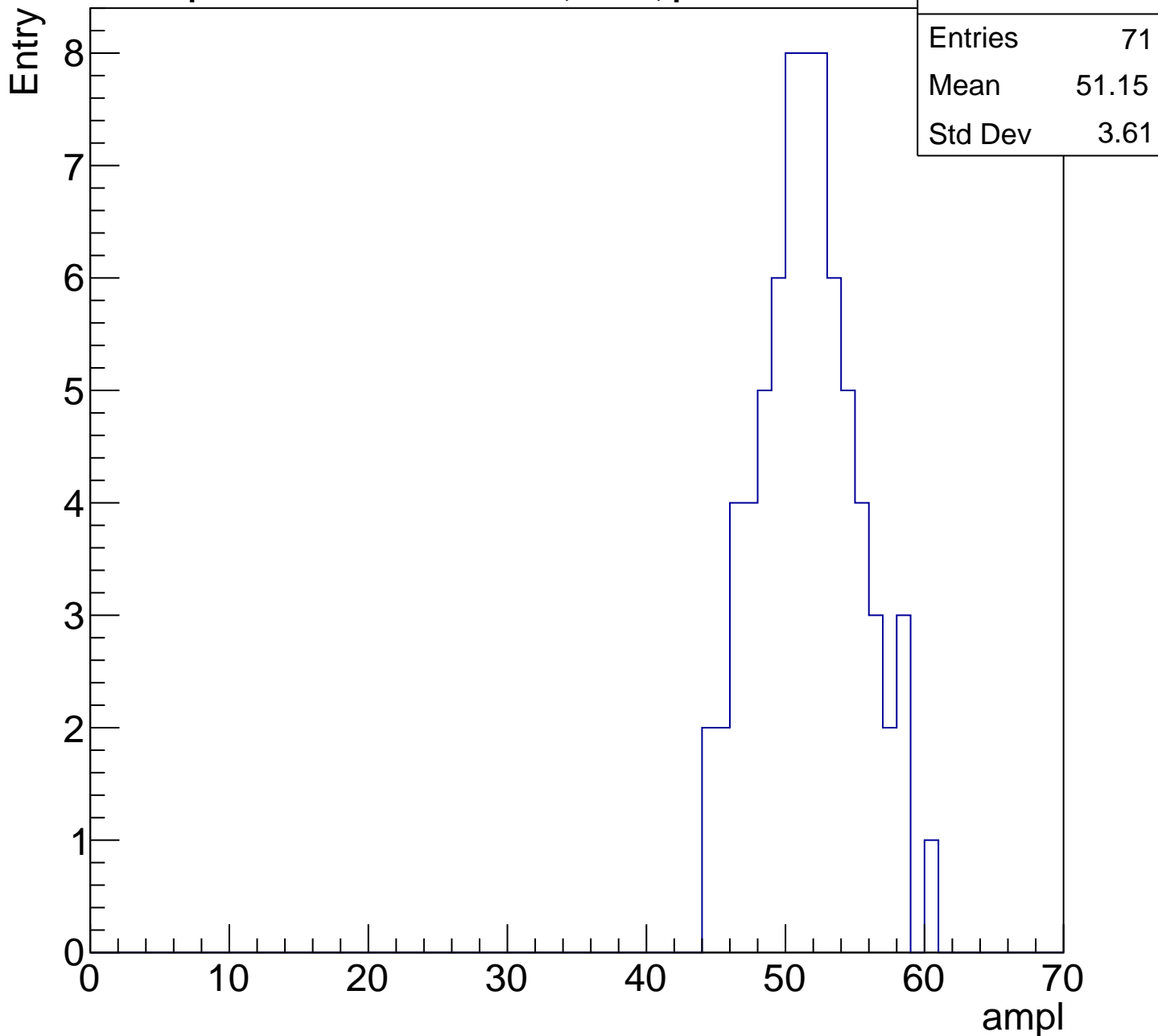
**Gaus mean : 45.1511**

**Gaus Width: 3.1324**



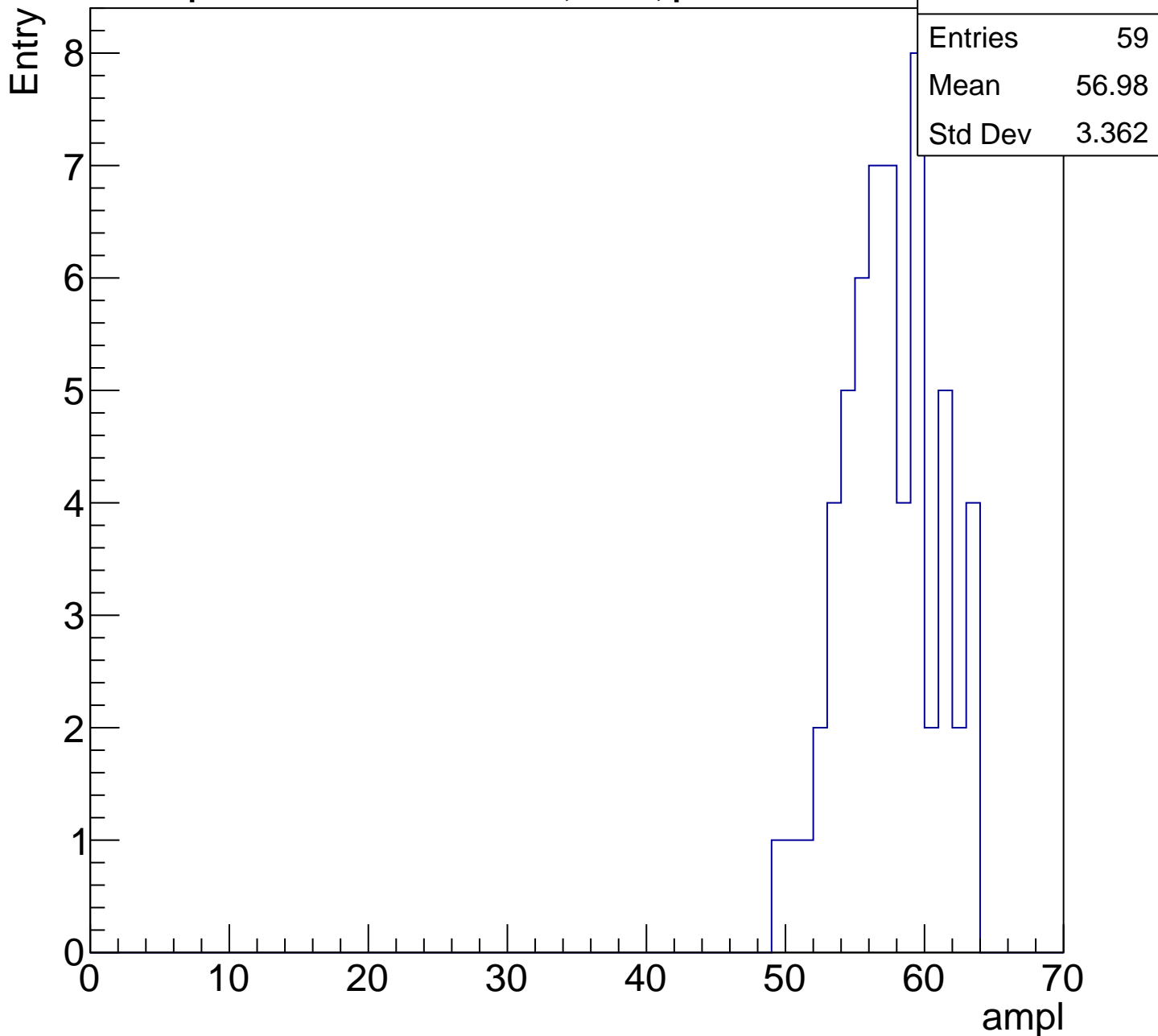
# B1L101S, U22-ch23, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2



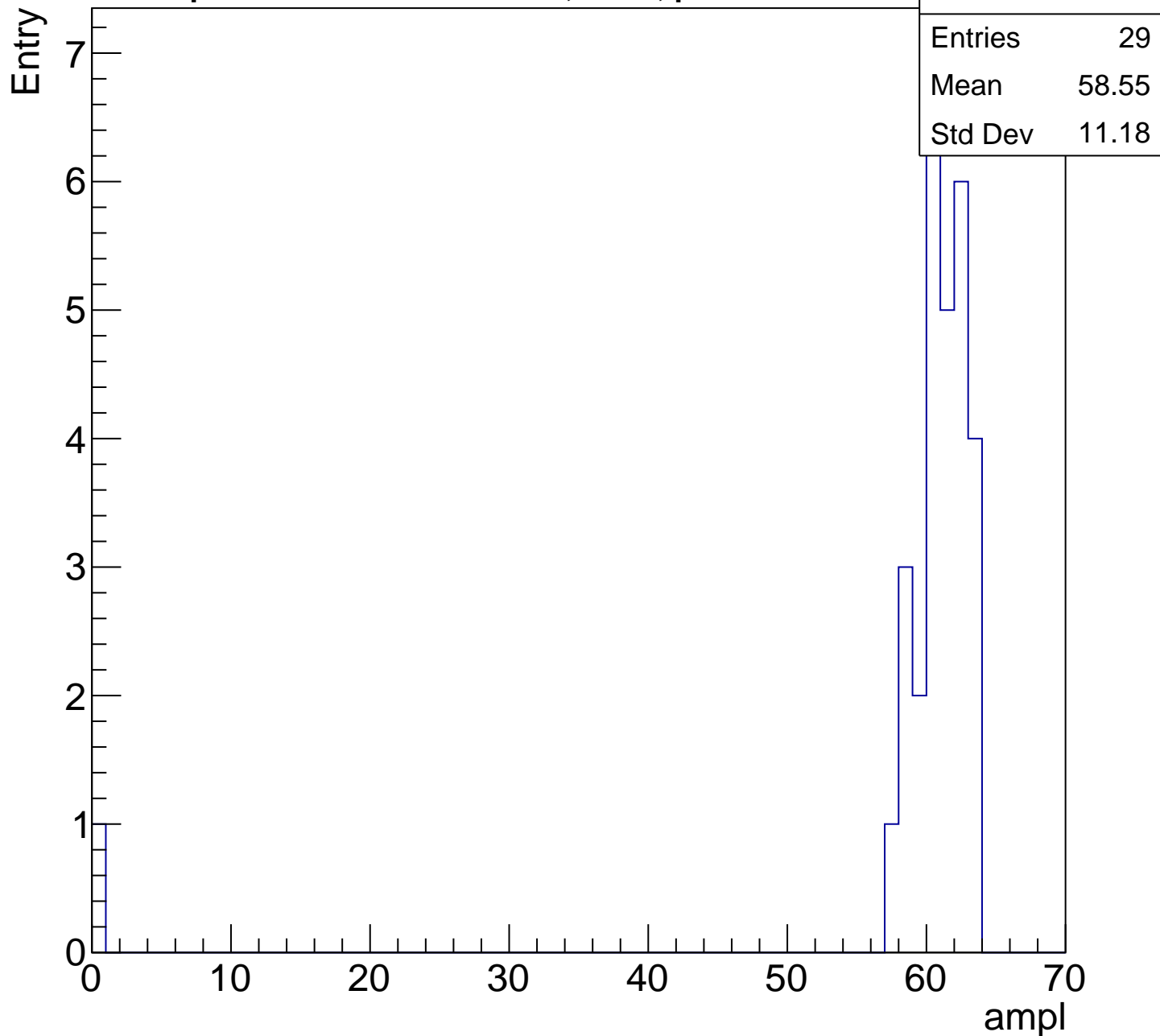
# B1L101S, U22-ch23, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U22-ch23, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U22-ch23, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

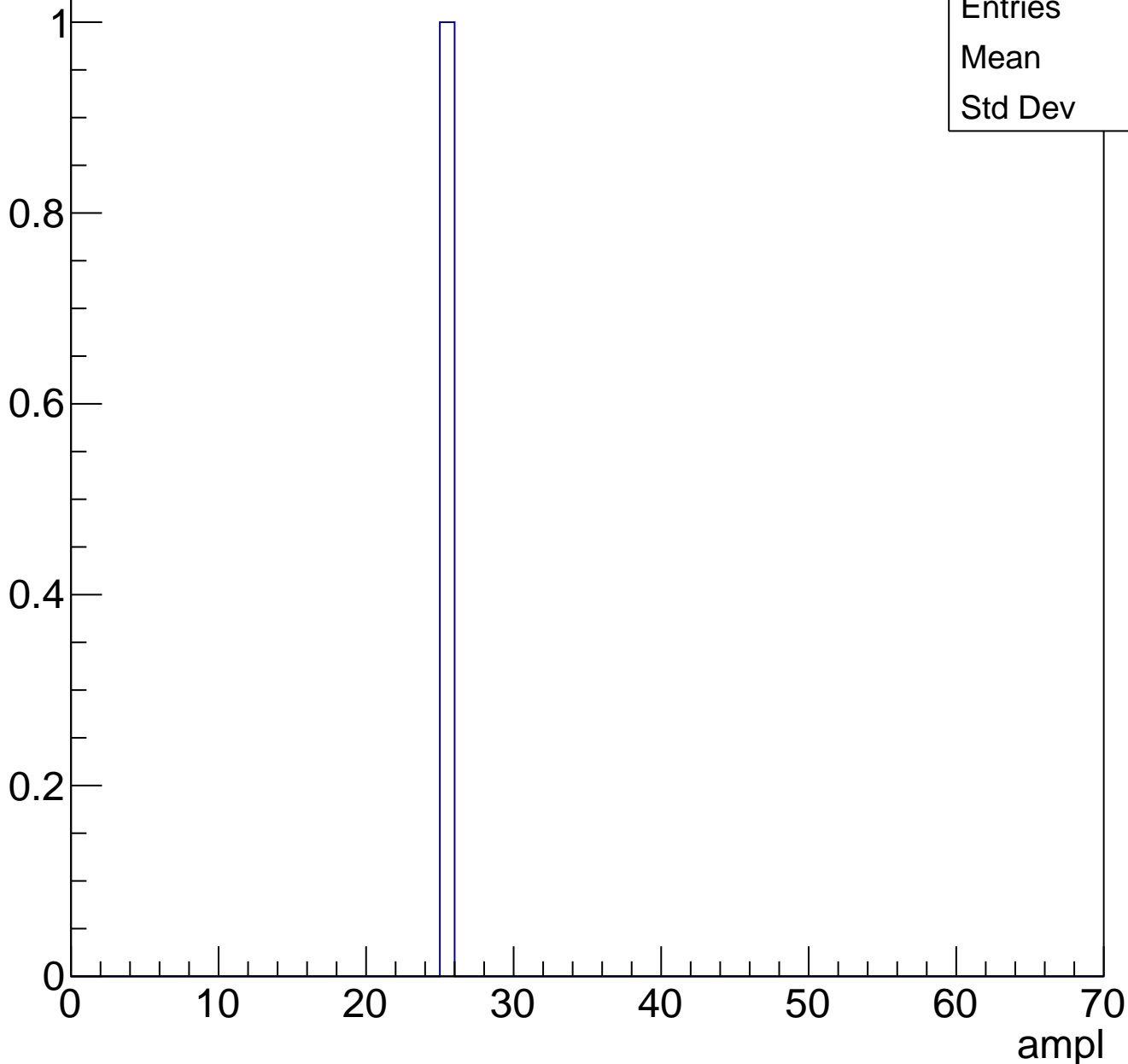




# B1L101S, U22-ch23, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U22-ch24, adc0

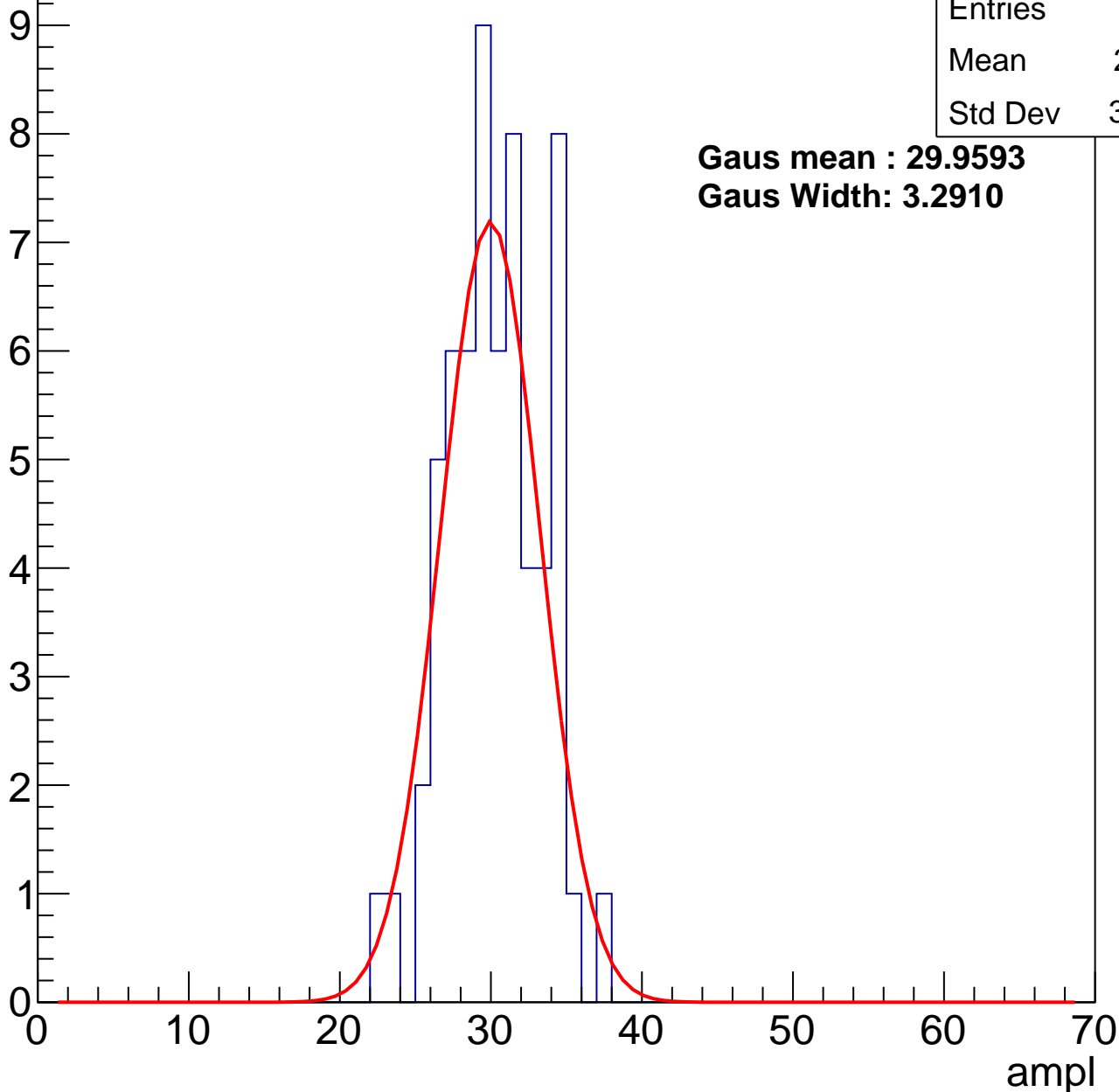
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	29.81
Std Dev	3.084

**Gaus mean : 29.9593**

**Gaus Width: 3.2910**



# B1L101S, U22-ch24, adc1

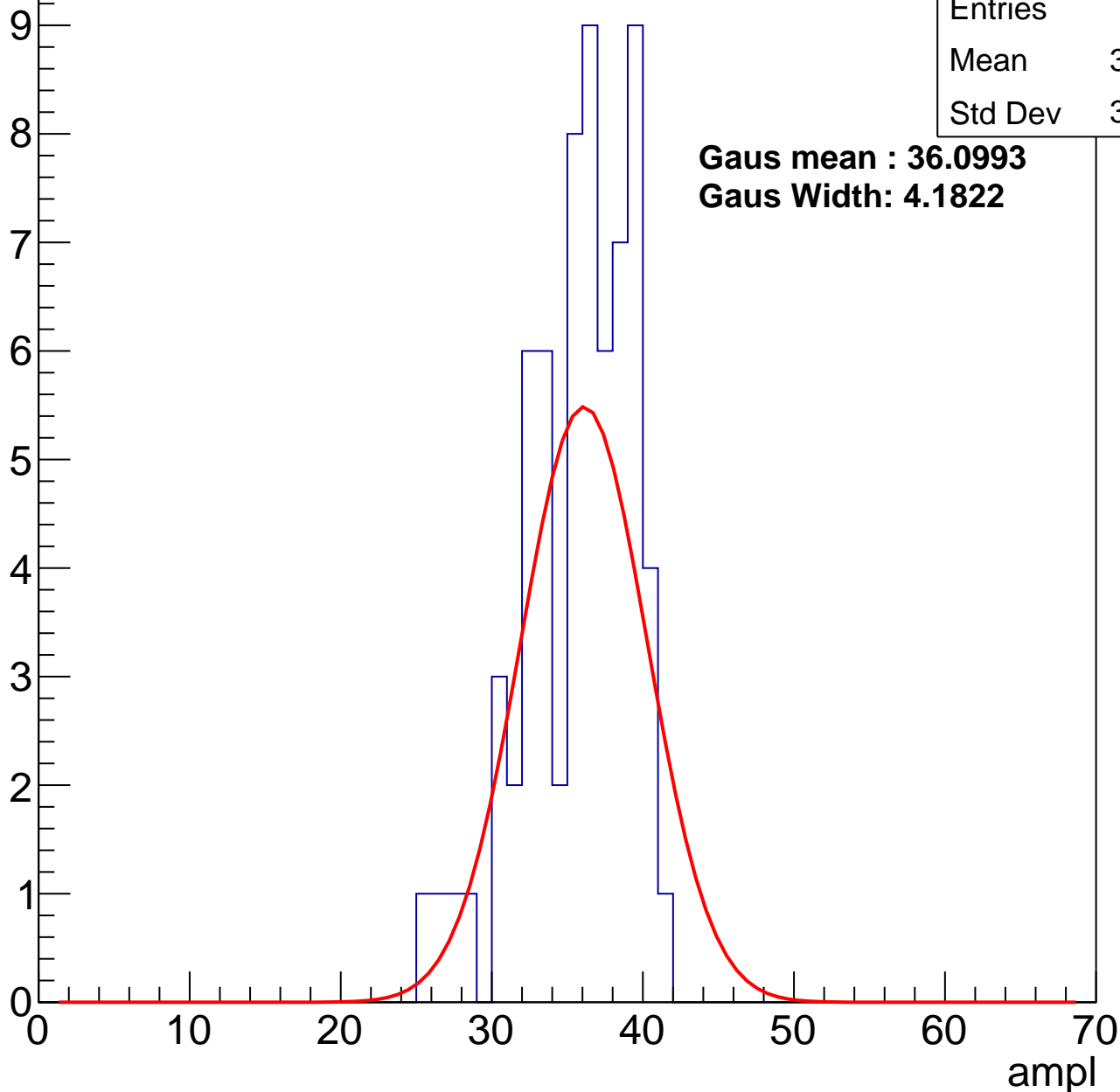
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	67
Mean	35.22
Std Dev	3.569

**Gaus mean : 36.0993**

**Gaus Width: 4.1822**



# B1L101S, U22-ch24, adc2

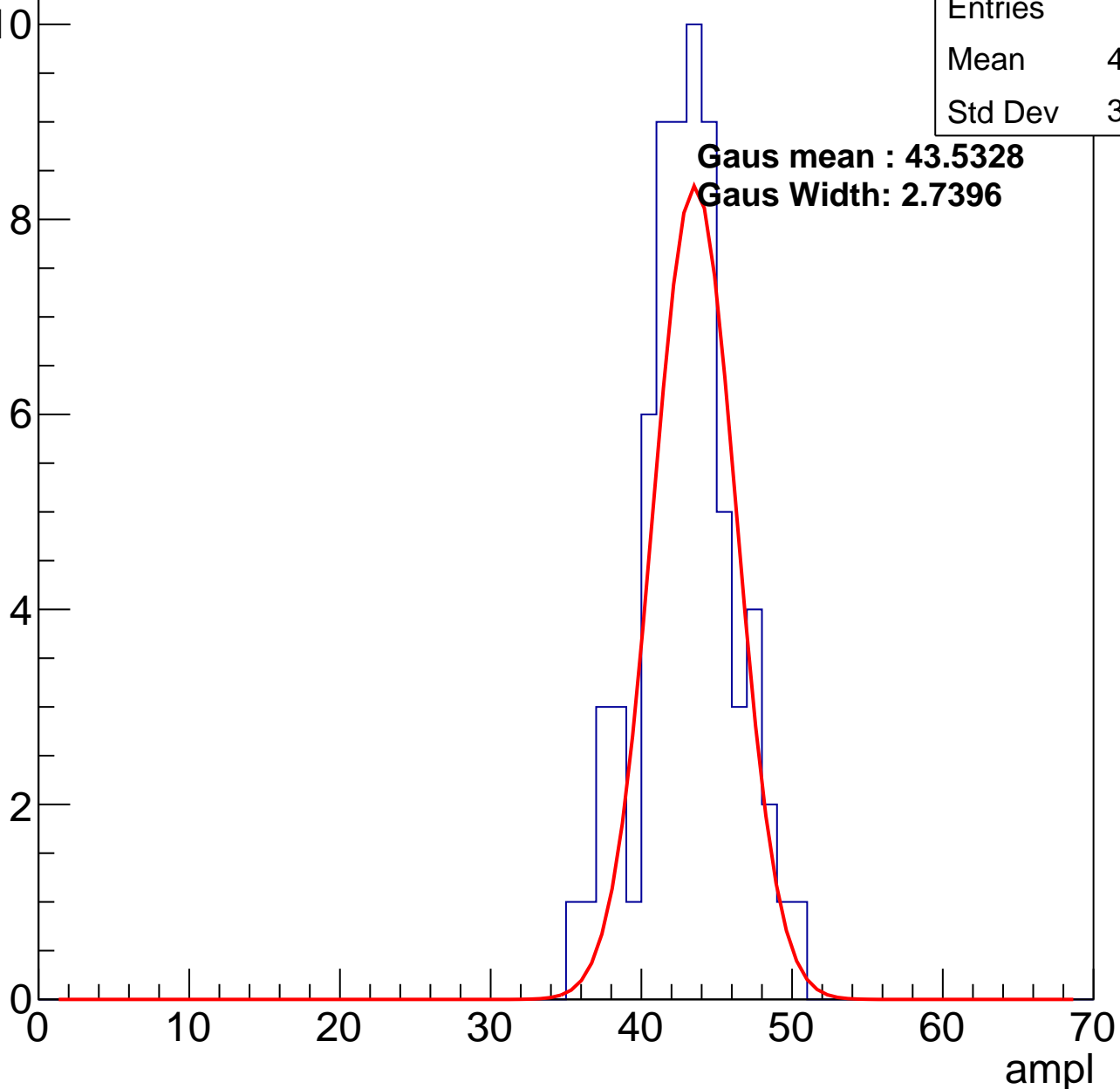
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	42.56
Std Dev	3.098

**Gaus mean : 43.5328**

**Gaus Width: 2.7396**

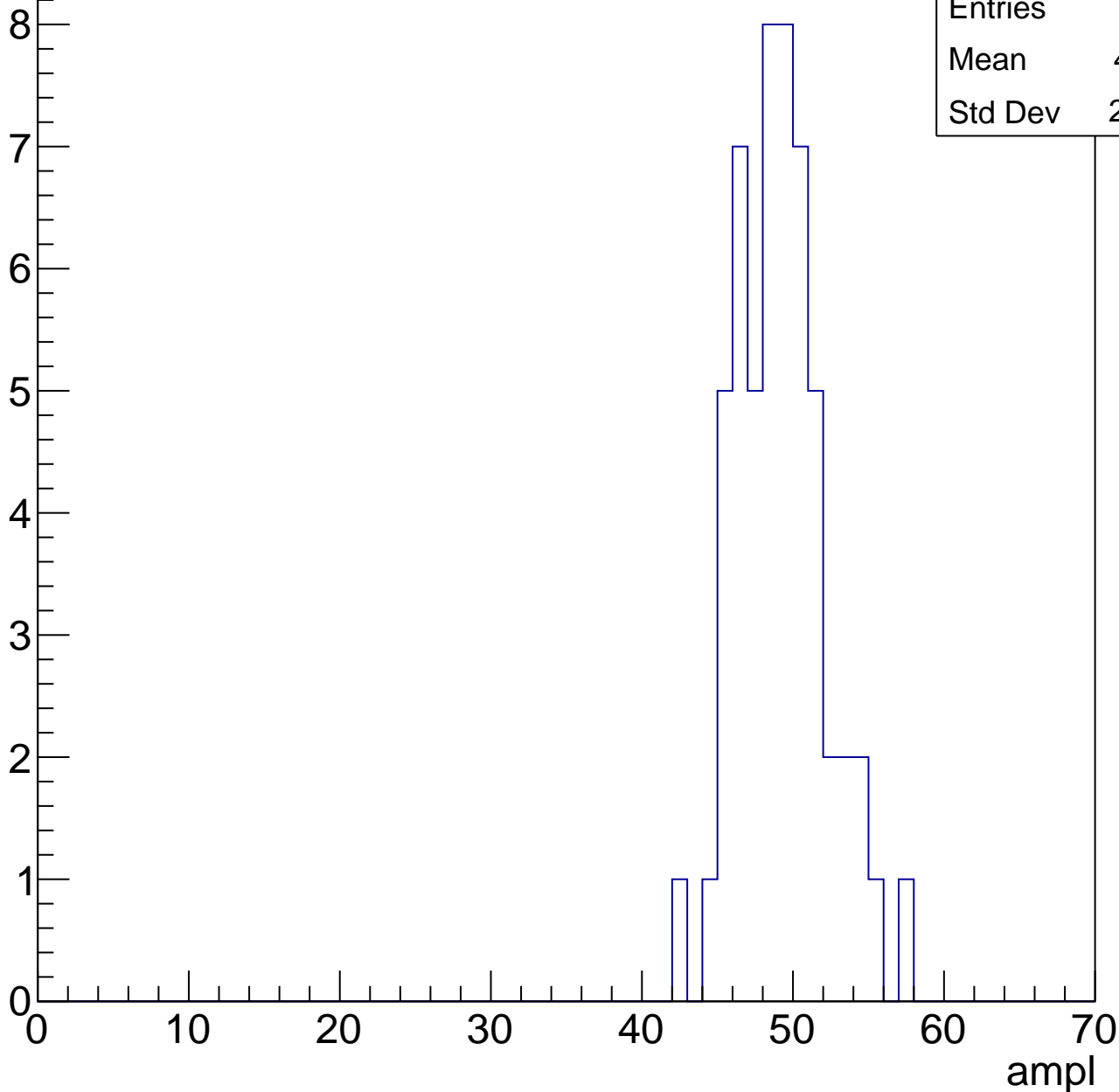


# B1L101S, U22-ch24, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	55
Mean	48.71
Std Dev	2.915

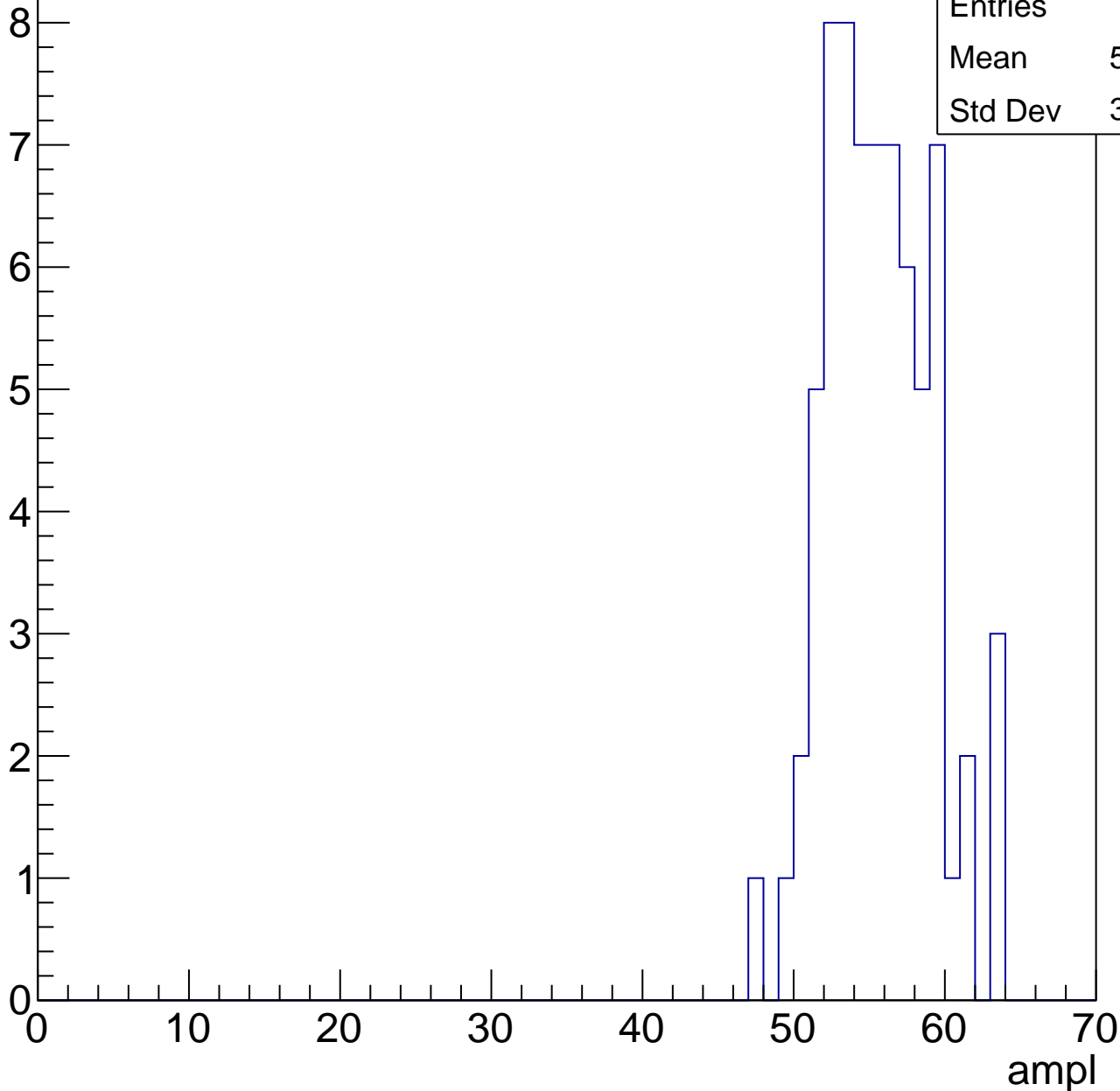


# B1L101S, U22-ch24, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	55.17
Std Dev	3.414

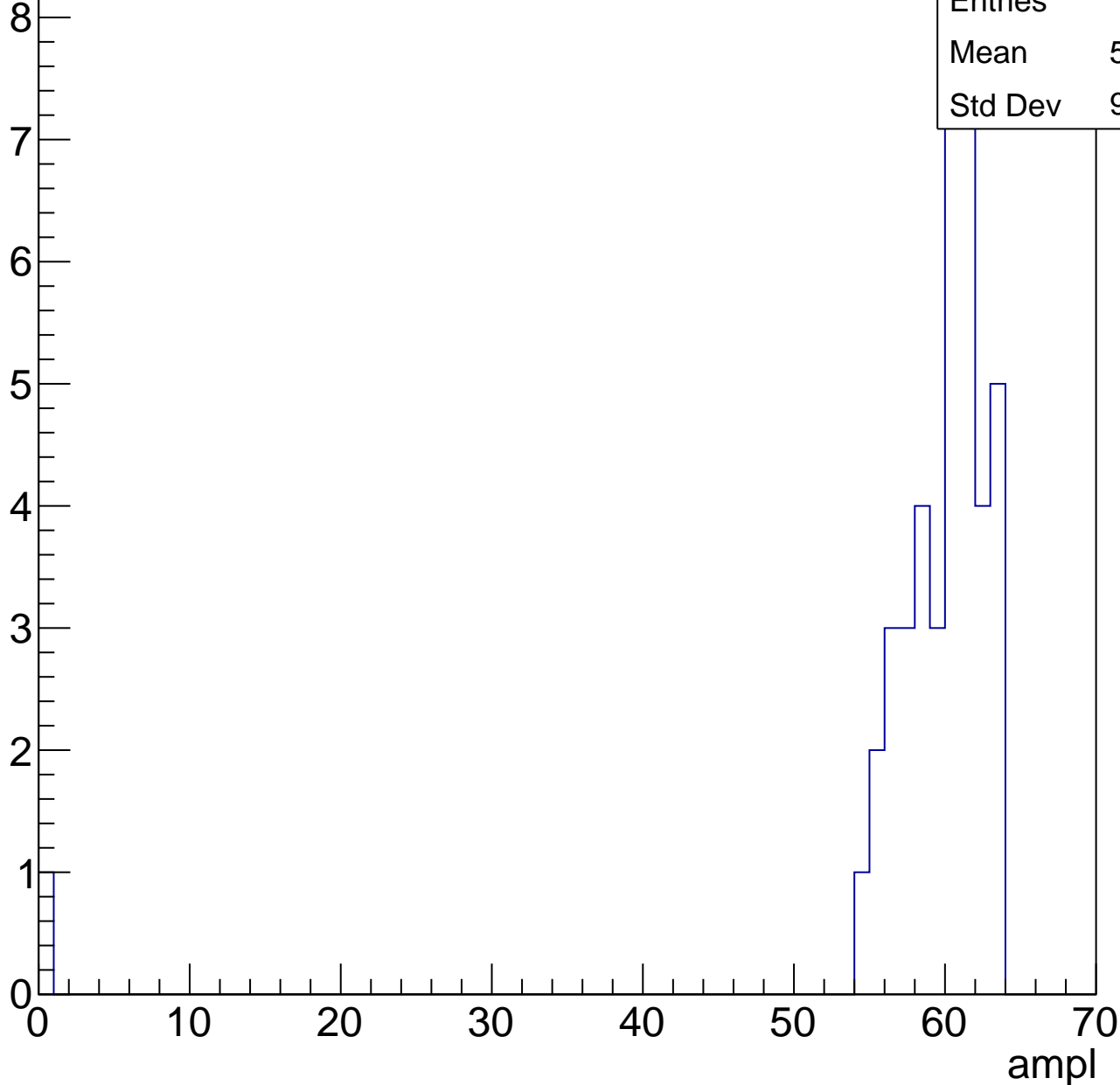


# B1L101S, U22-ch24, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	42
Mean	58.17
Std Dev	9.396

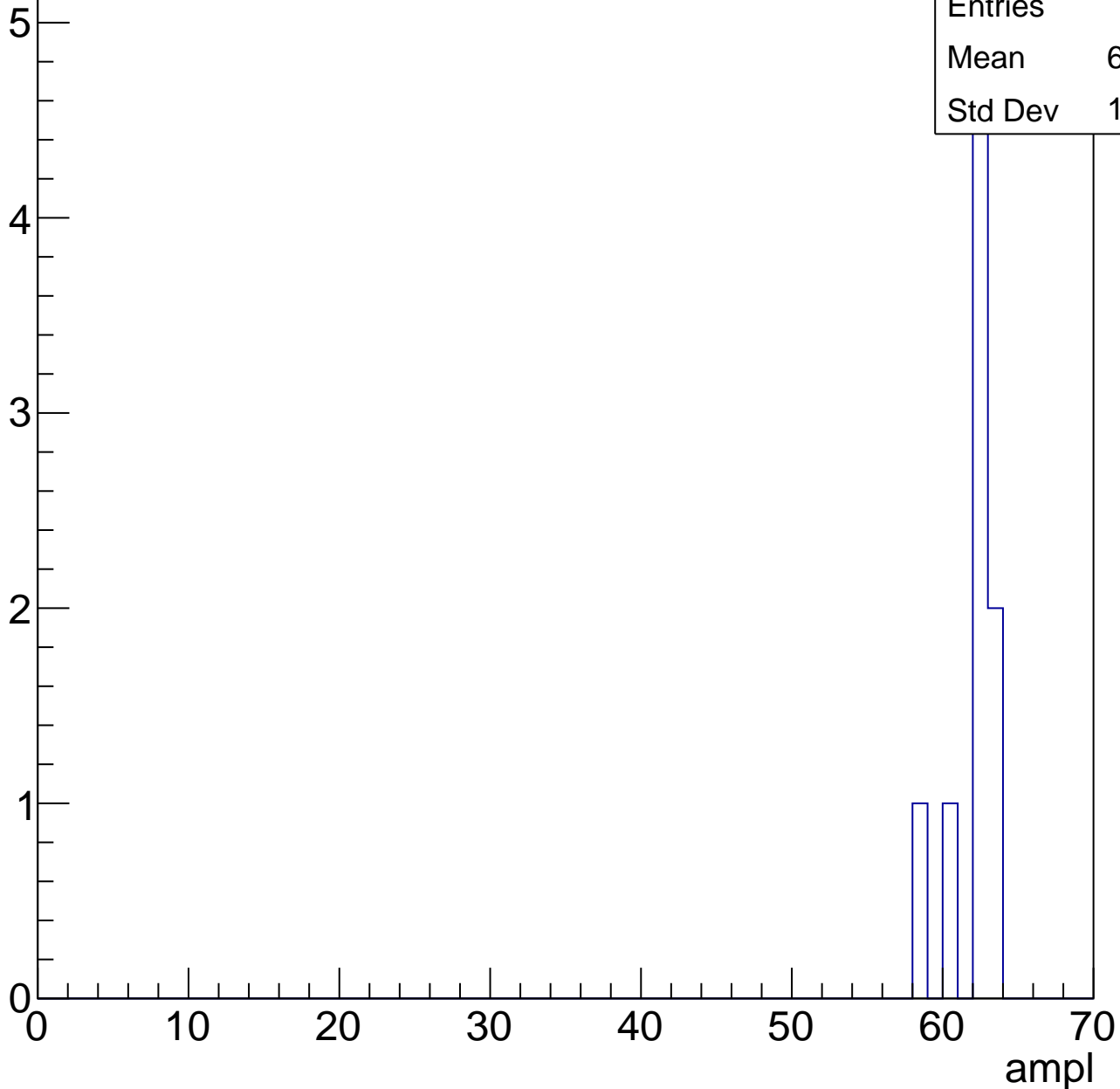


# B1L101S, U22-ch24, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	9
Mean	61.56
Std Dev	1.499





# B1L101S, U22-ch24, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U22-ch25, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	70
Mean	30.56
Std Dev	3.022

**Gaus mean : 30.7392**

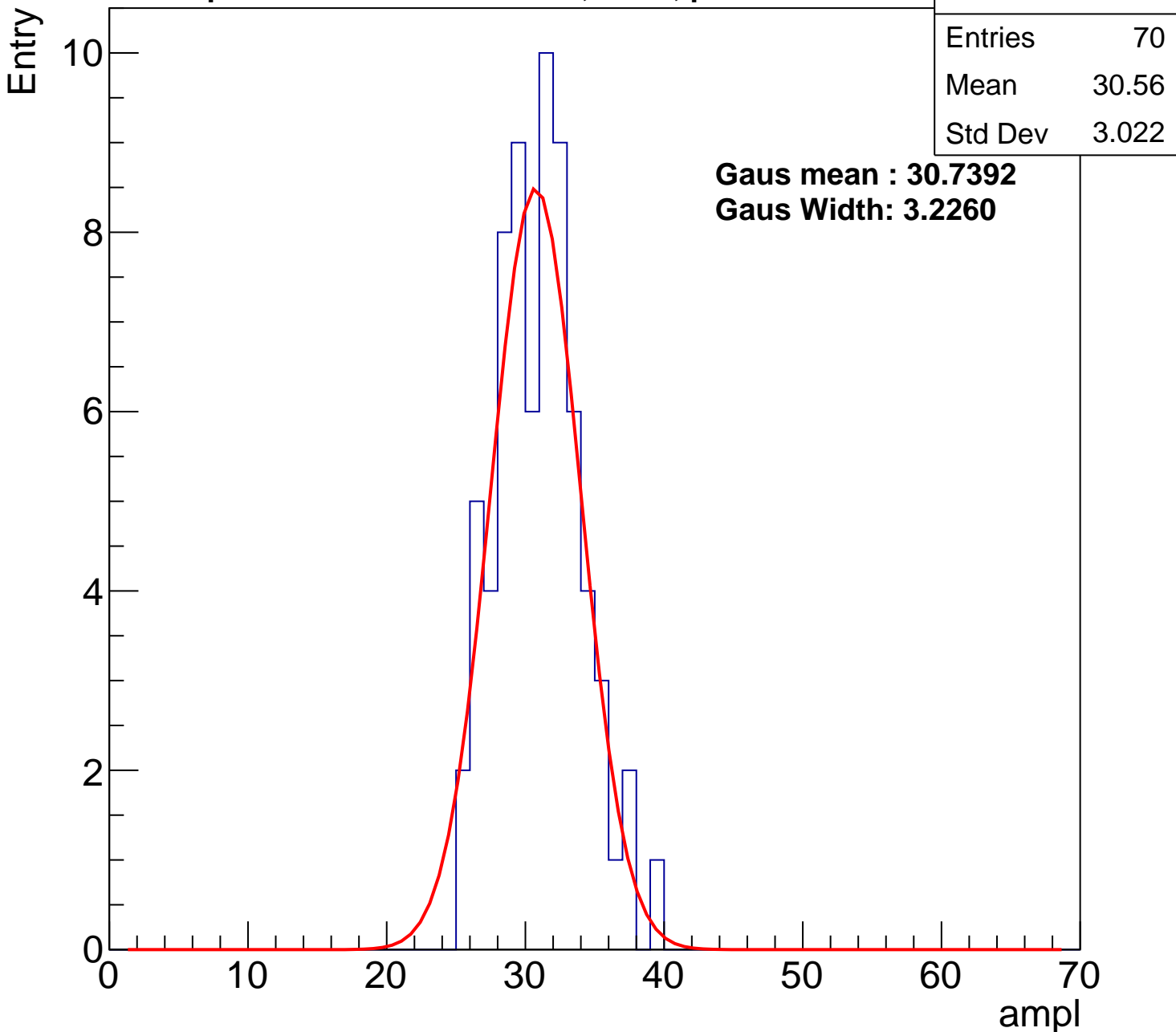
**Gaus Width: 3.2260**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U22-ch25, adc1

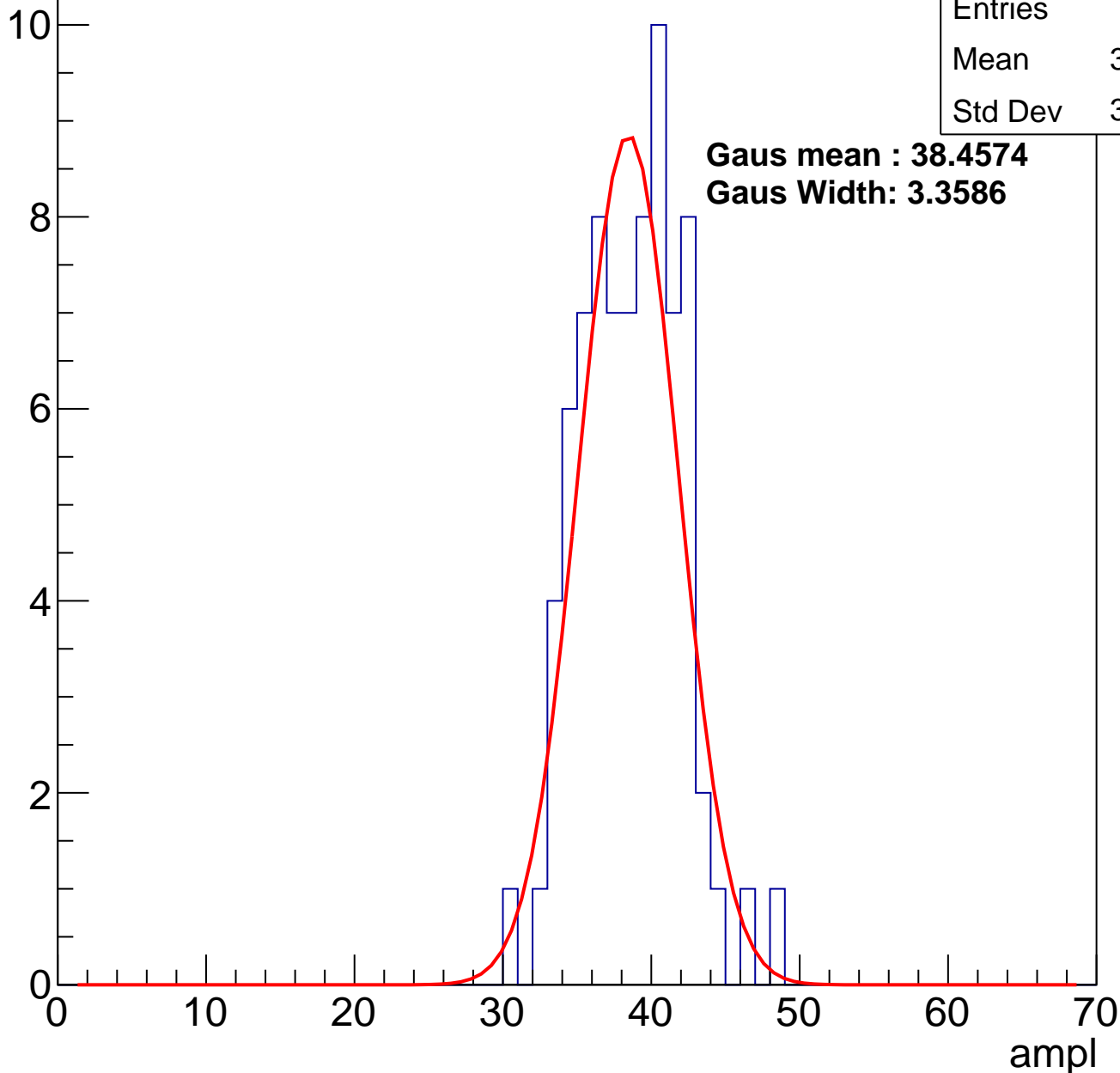
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	79
Mean	38.16
Std Dev	3.347

**Gaus mean : 38.4574**

**Gaus Width: 3.3586**

Entry



# B1L101S, U22-ch25, adc2

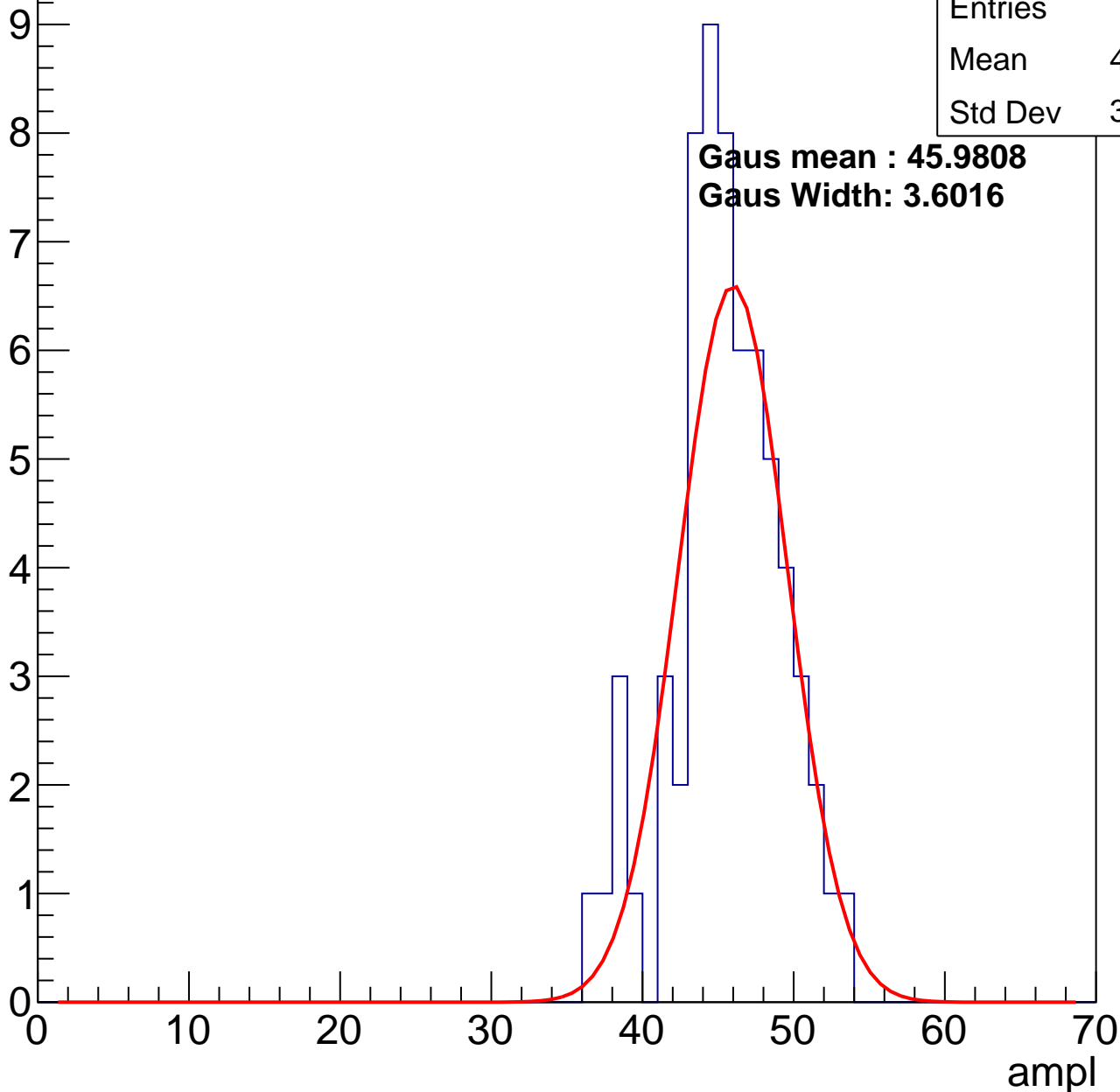
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	45.06
Std Dev	3.609

**Gaus mean : 45.9808**

**Gaus Width: 3.6016**

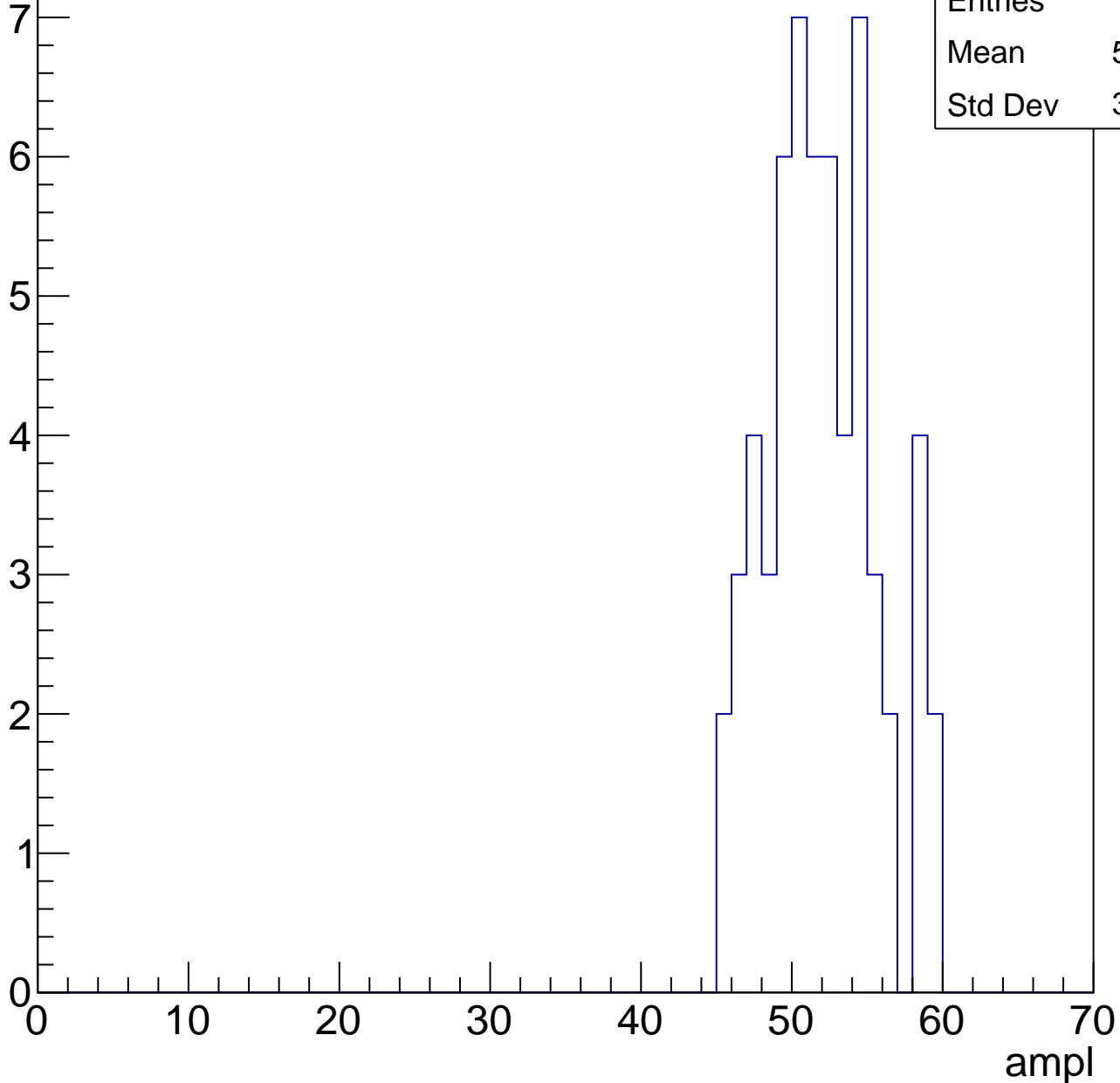


# B1L101S, U22-ch25, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	59
Mean	51.51
Std Dev	3.591

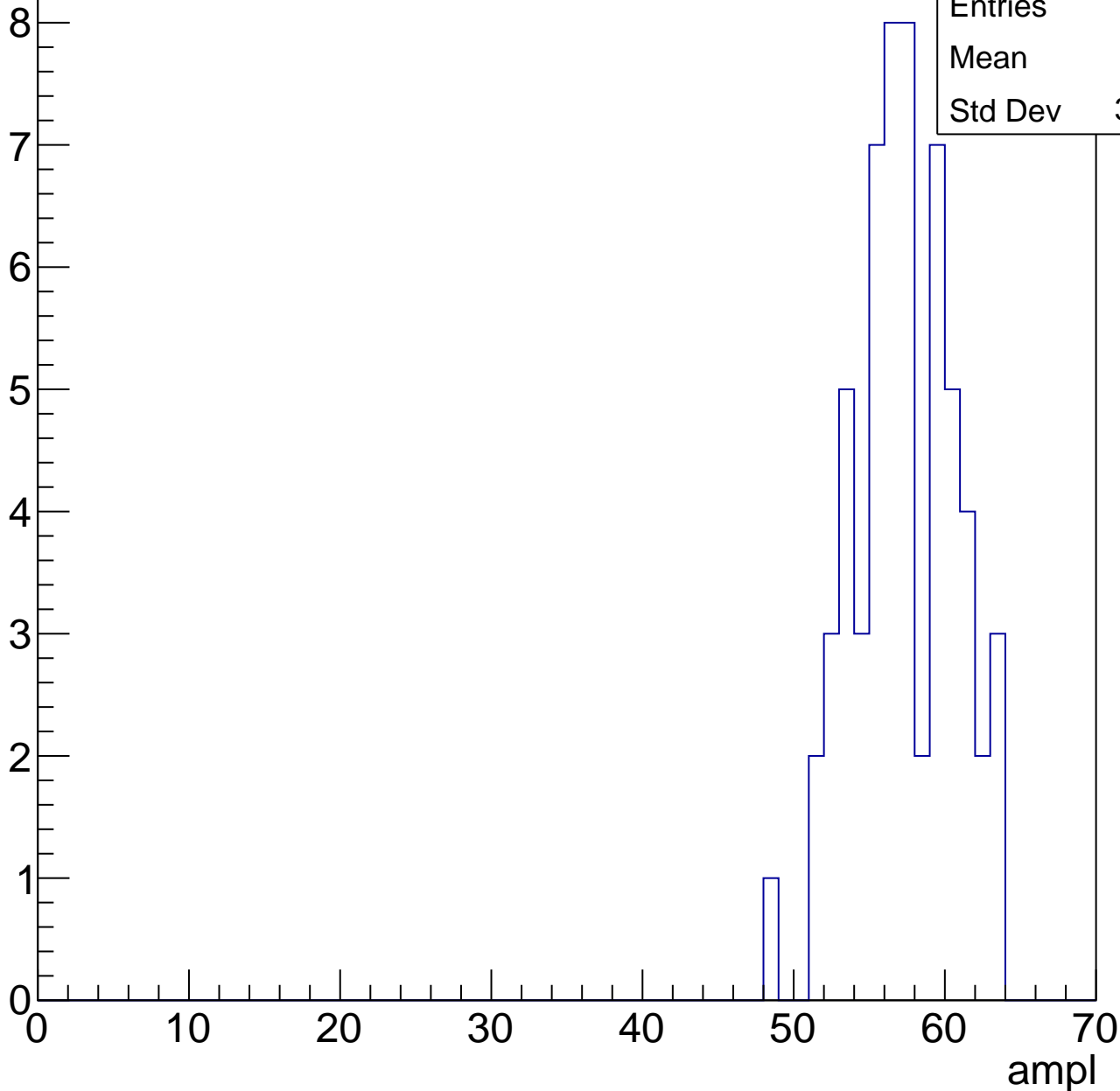


# B1L101S, U22-ch25, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	60
Mean	56.8
Std Dev	3.331

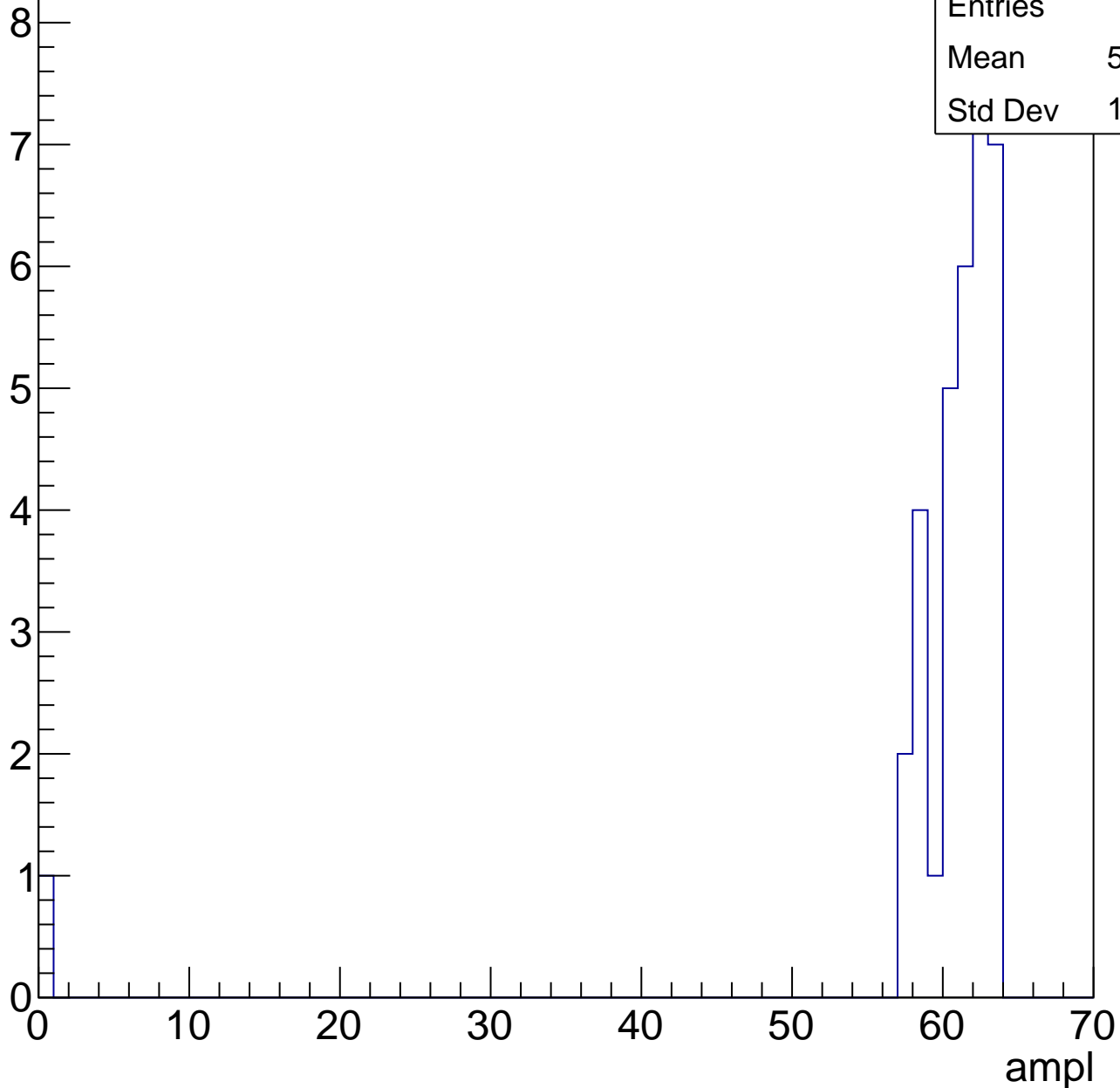


# B1L101S, U22-ch25, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	34
Mean	59.06
Std Dev	10.44



# B1L101S, U22-ch25, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0



# B1L101S, U22-ch25, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U22-ch26, adc0

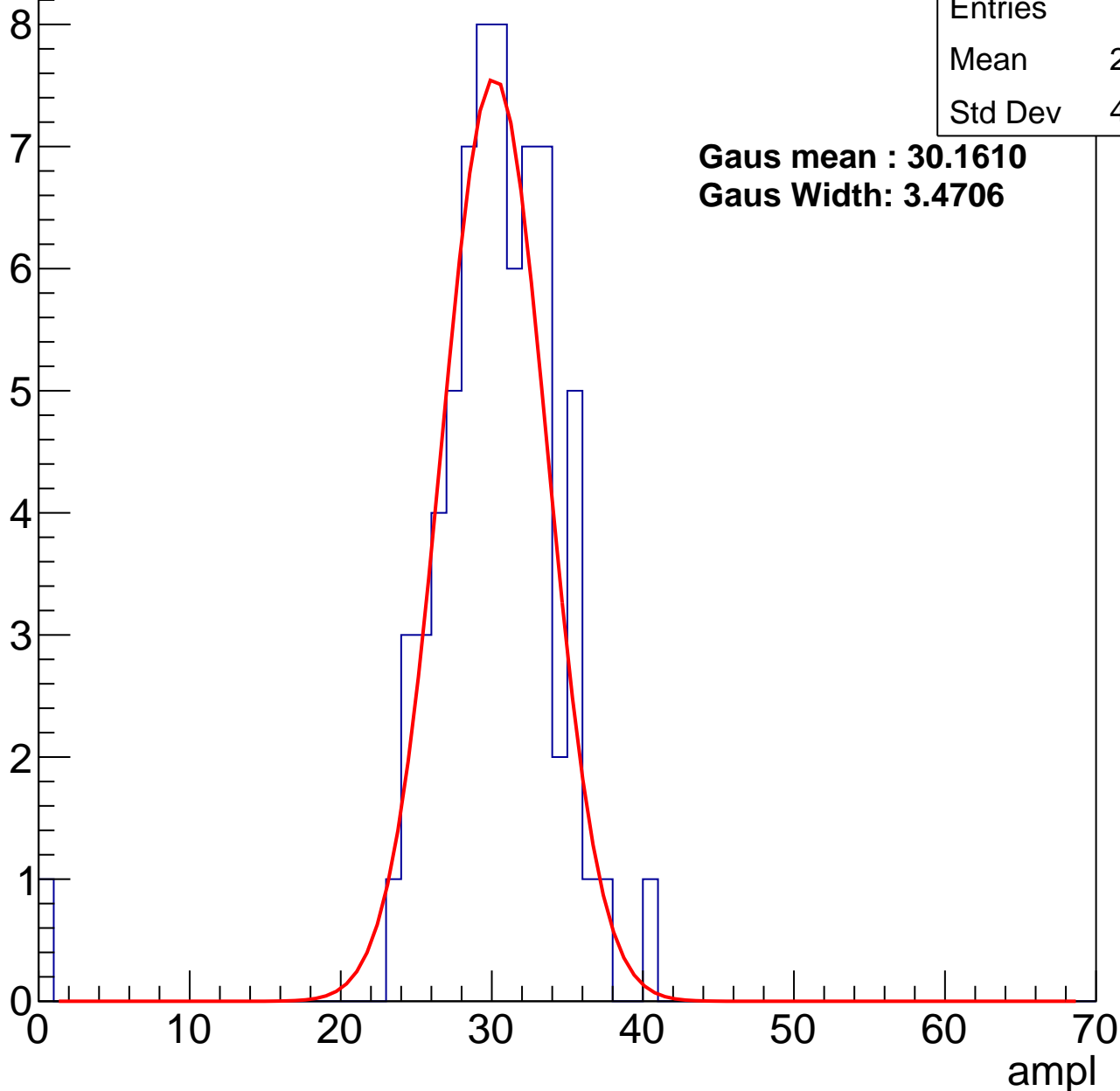
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	29.63
Std Dev	4.937

**Gaus mean : 30.1610**

**Gaus Width: 3.4706**

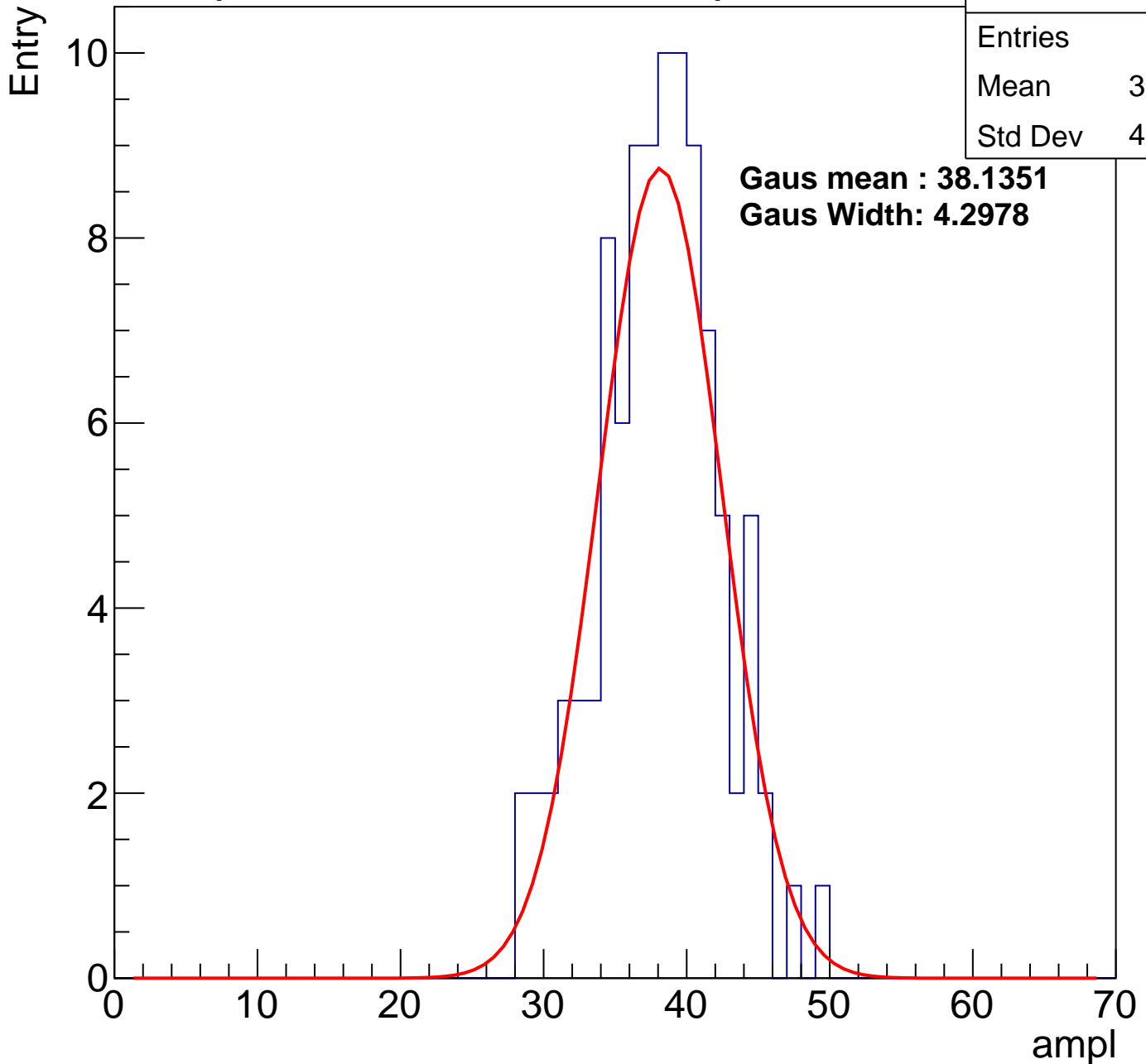


# B1L101S, U22-ch26, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	99
Mean	37.58
Std Dev	4.202

**Gaus mean : 38.1351**  
**Gaus Width: 4.2978**



# B1L101S, U22-ch26, adc2

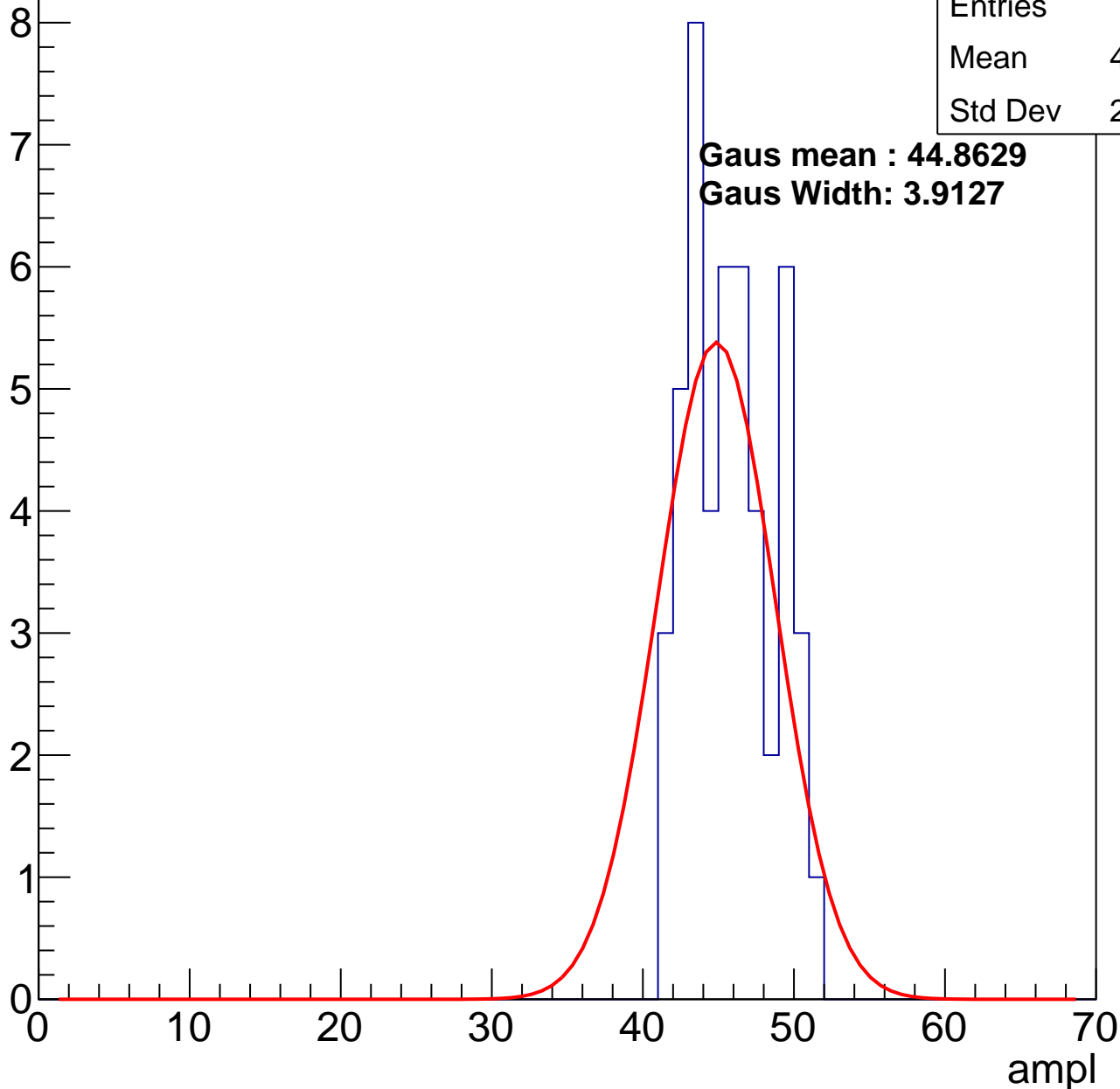
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	48
Mean	45.38
Std Dev	2.774

**Gaus mean : 44.8629**

**Gaus Width: 3.9127**

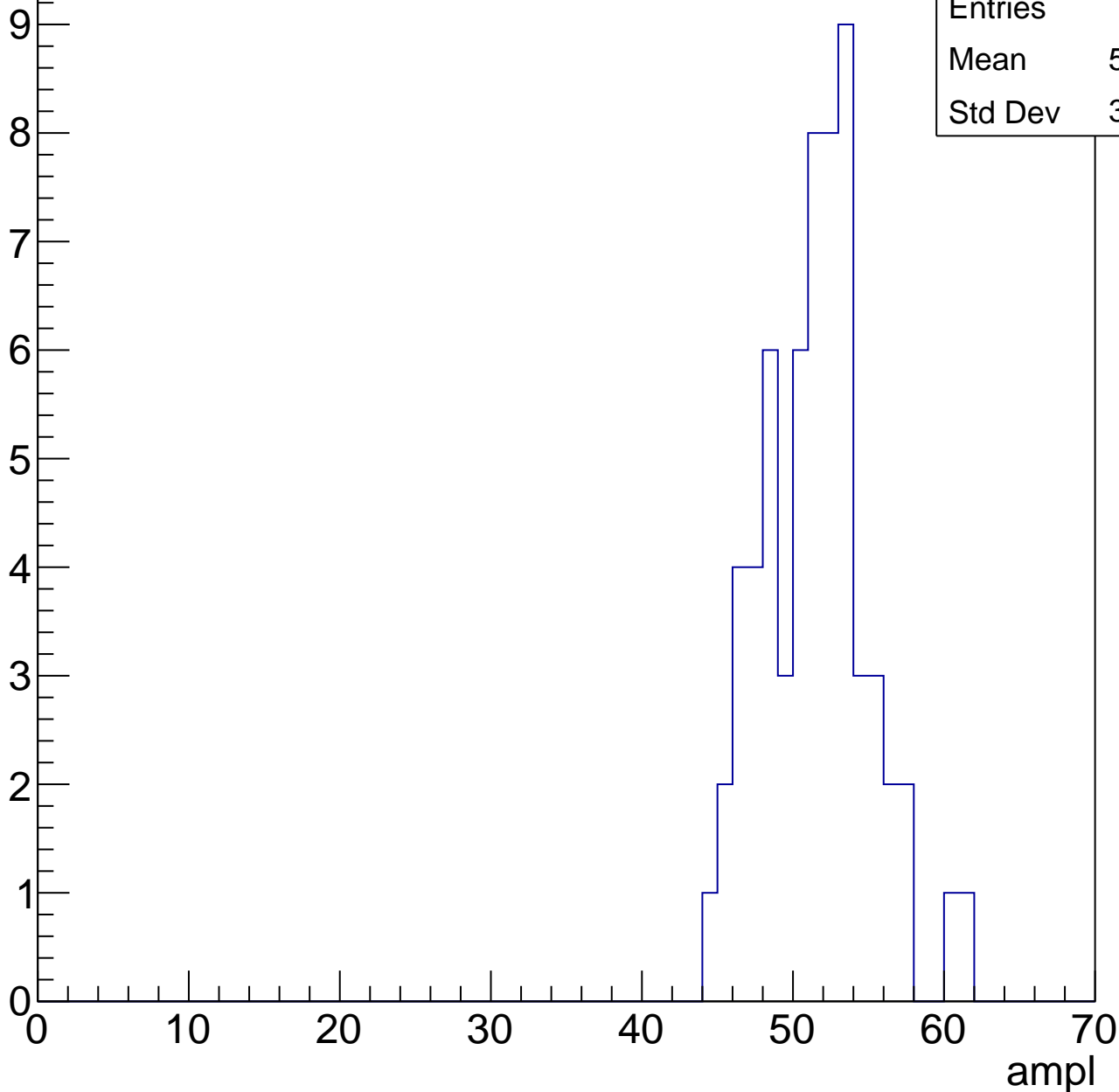


# B1L101S, U22-ch26, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

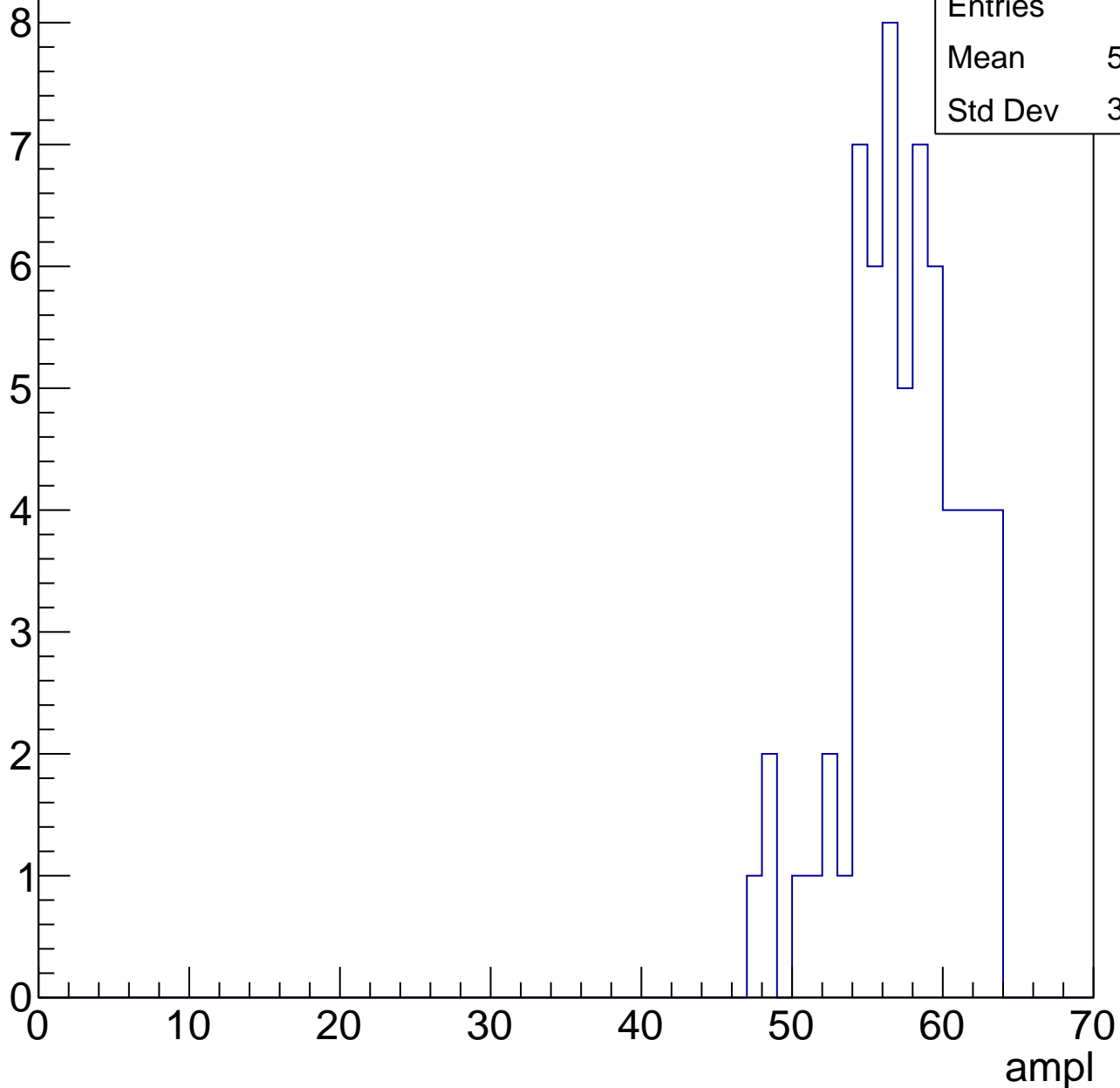
Entries	63
Mean	51.05
Std Dev	3.516



# B1L101S, U22-ch26, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

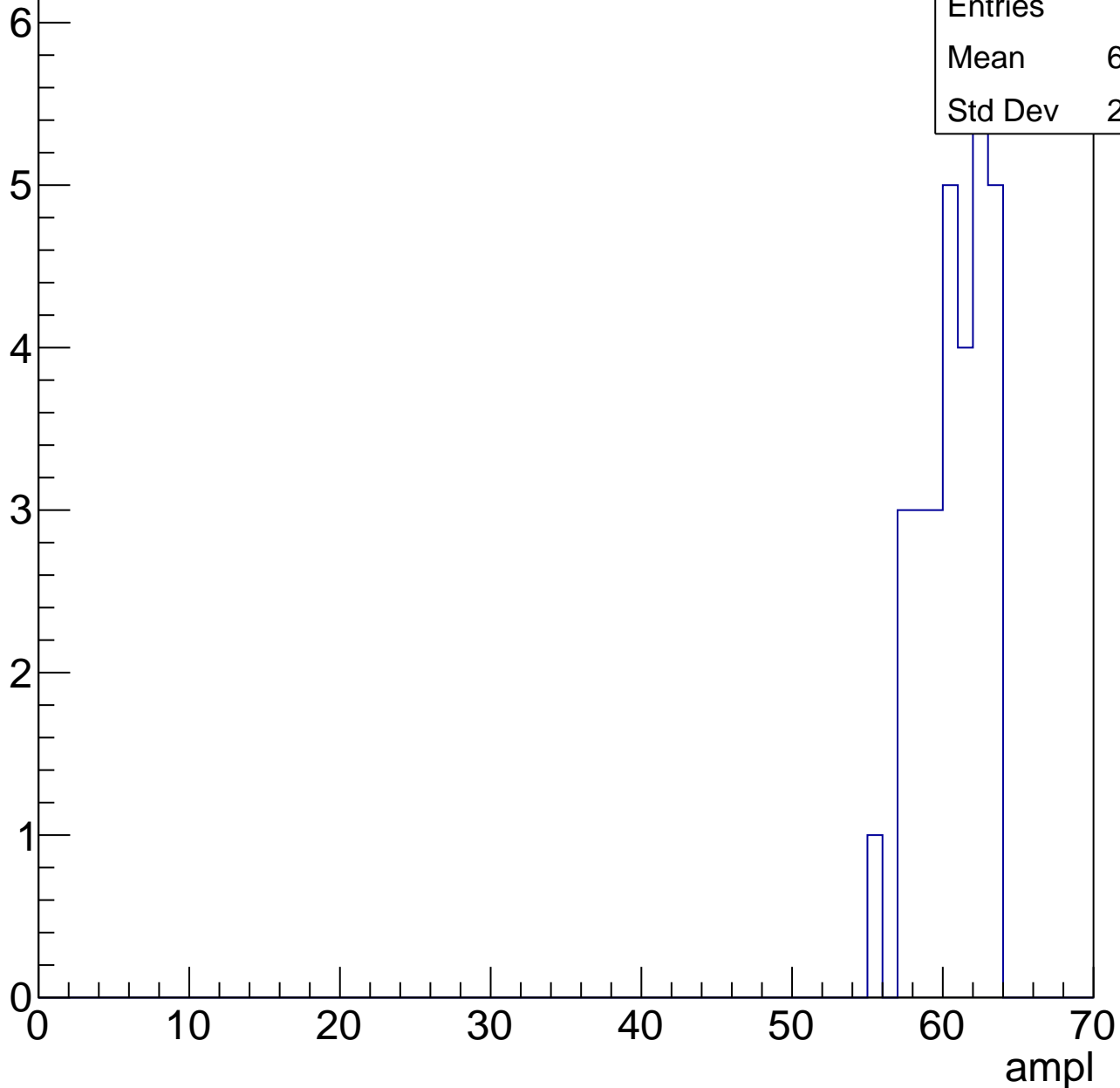


# B1L101S, U22-ch26, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

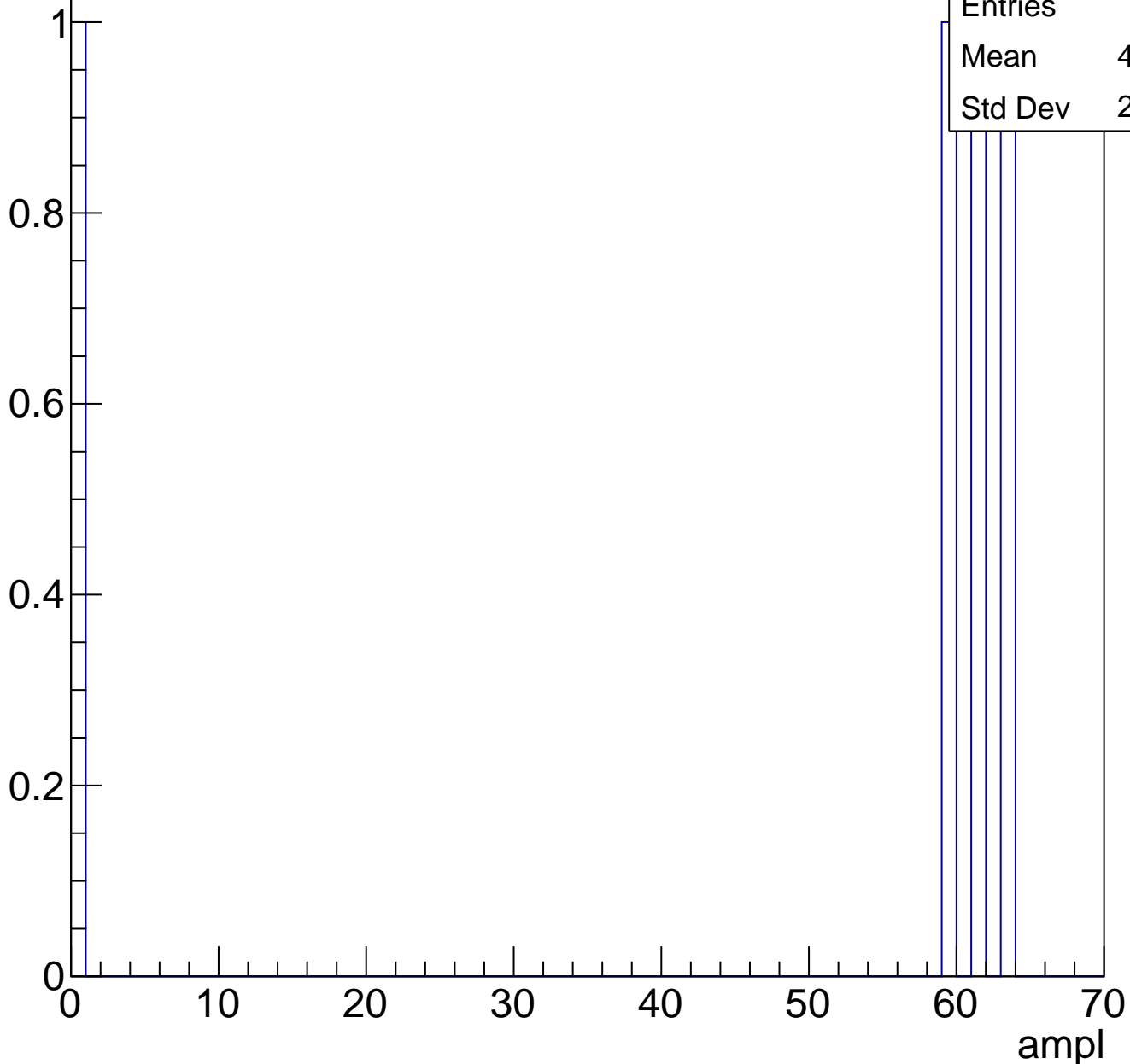
Entries	30
Mean	60.27
Std Dev	2.144



# B1L101S, U22-ch26, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	4
Mean	45.75
Std Dev	26.45



# B1L101S, U22-ch26, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U22-ch27, adc0

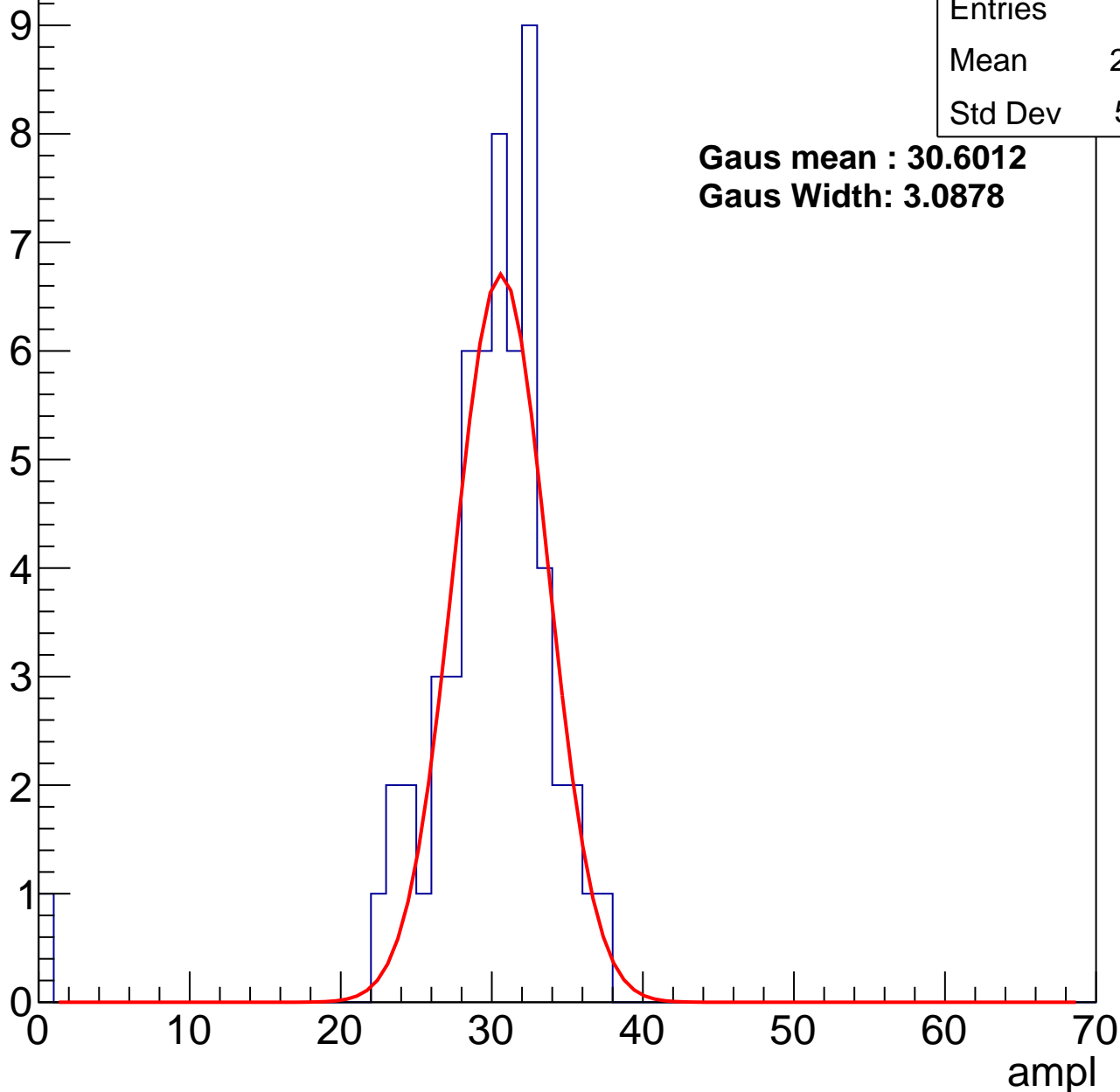
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	58
Mean	29.29
Std Dev	5.051

**Gaus mean : 30.6012**

**Gaus Width: 3.0878**



# B1L101S, U22-ch27, adc1

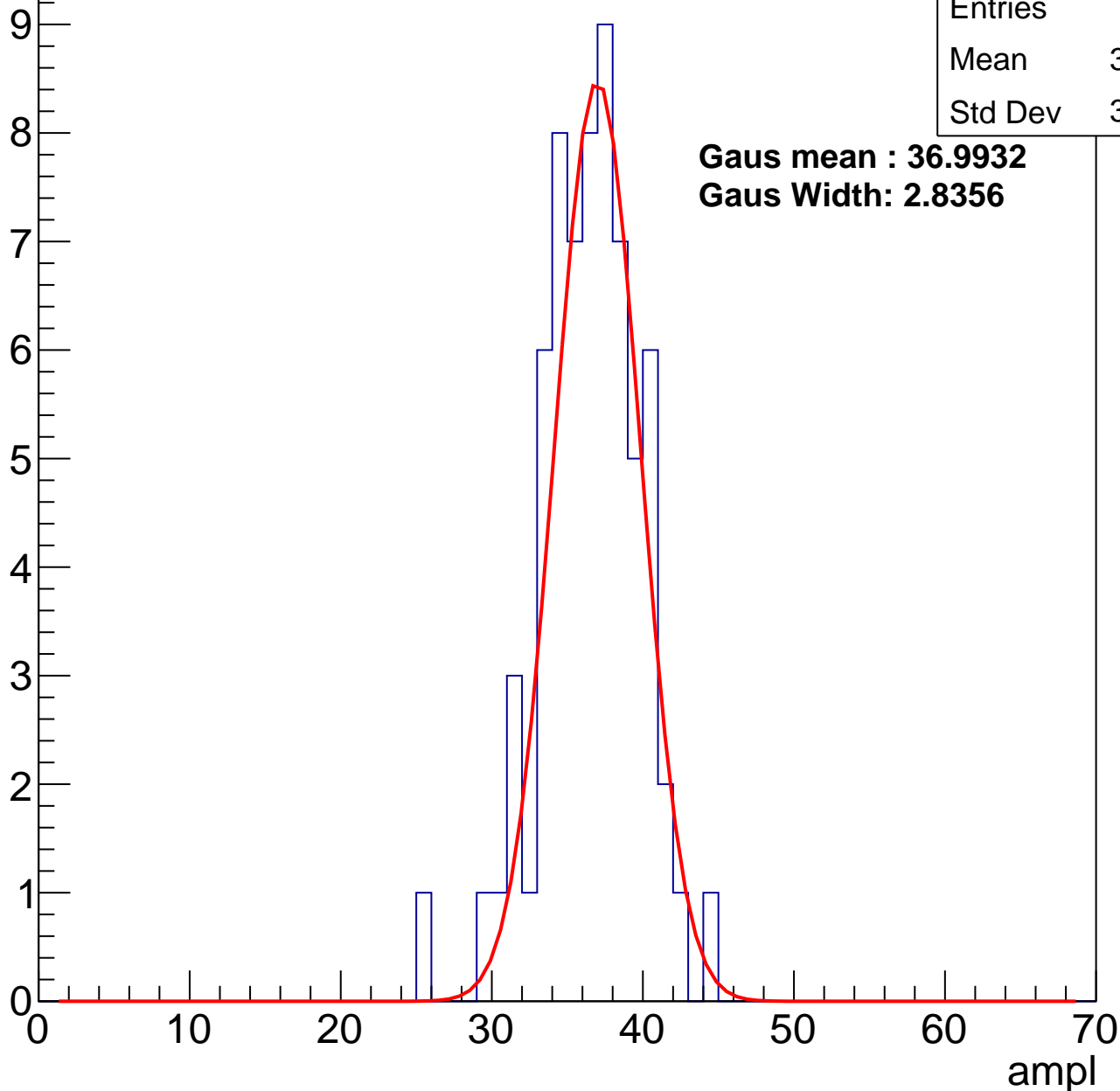
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	67
Mean	36.03
Std Dev	3.273

**Gaus mean : 36.9932**

**Gaus Width: 2.8356**



# B1L101S, U22-ch27, adc2

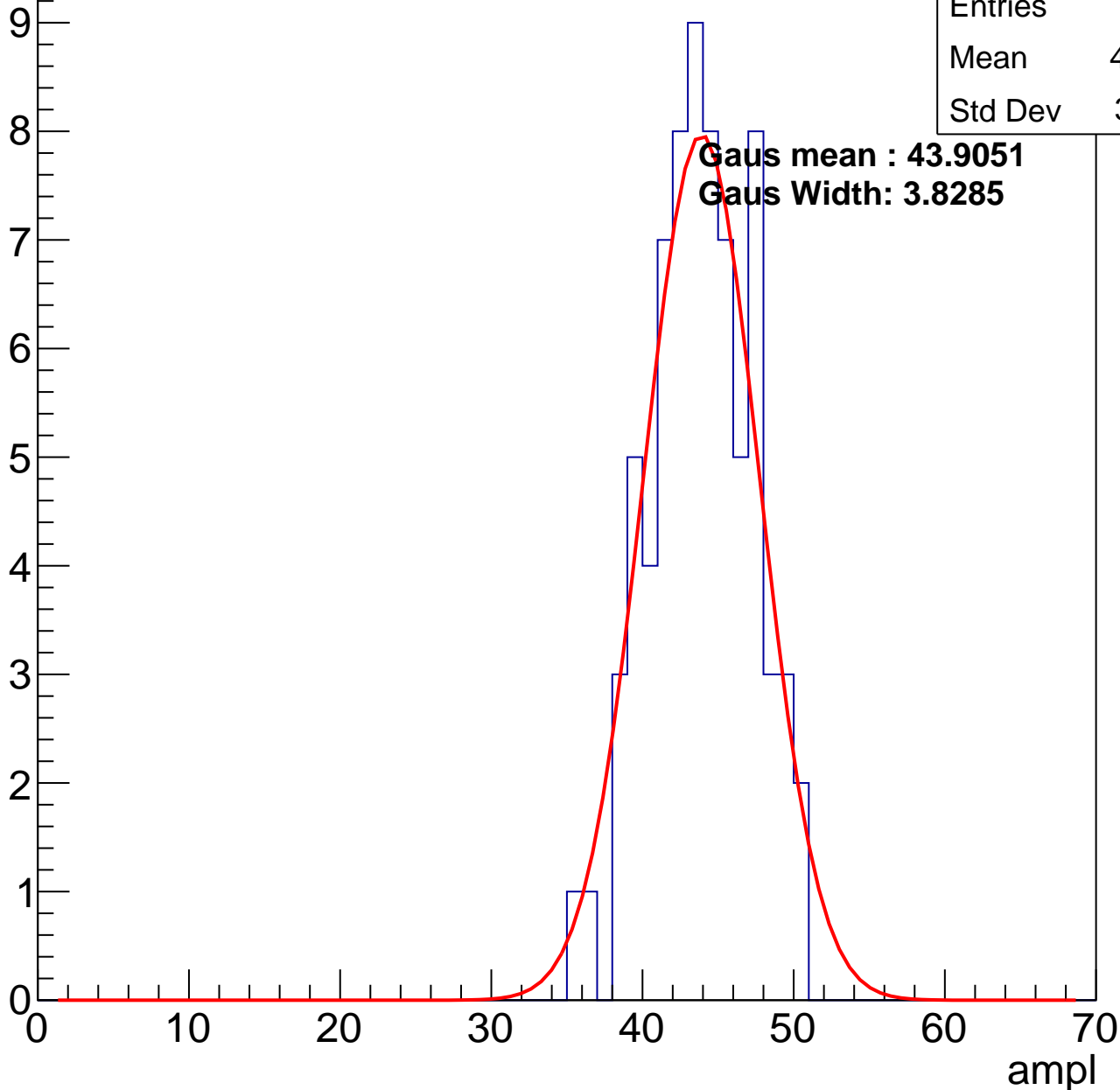
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	74
Mean	43.43
Std Dev	3.321

**Gaus mean : 43.9051**

**Gaus Width: 3.8285**

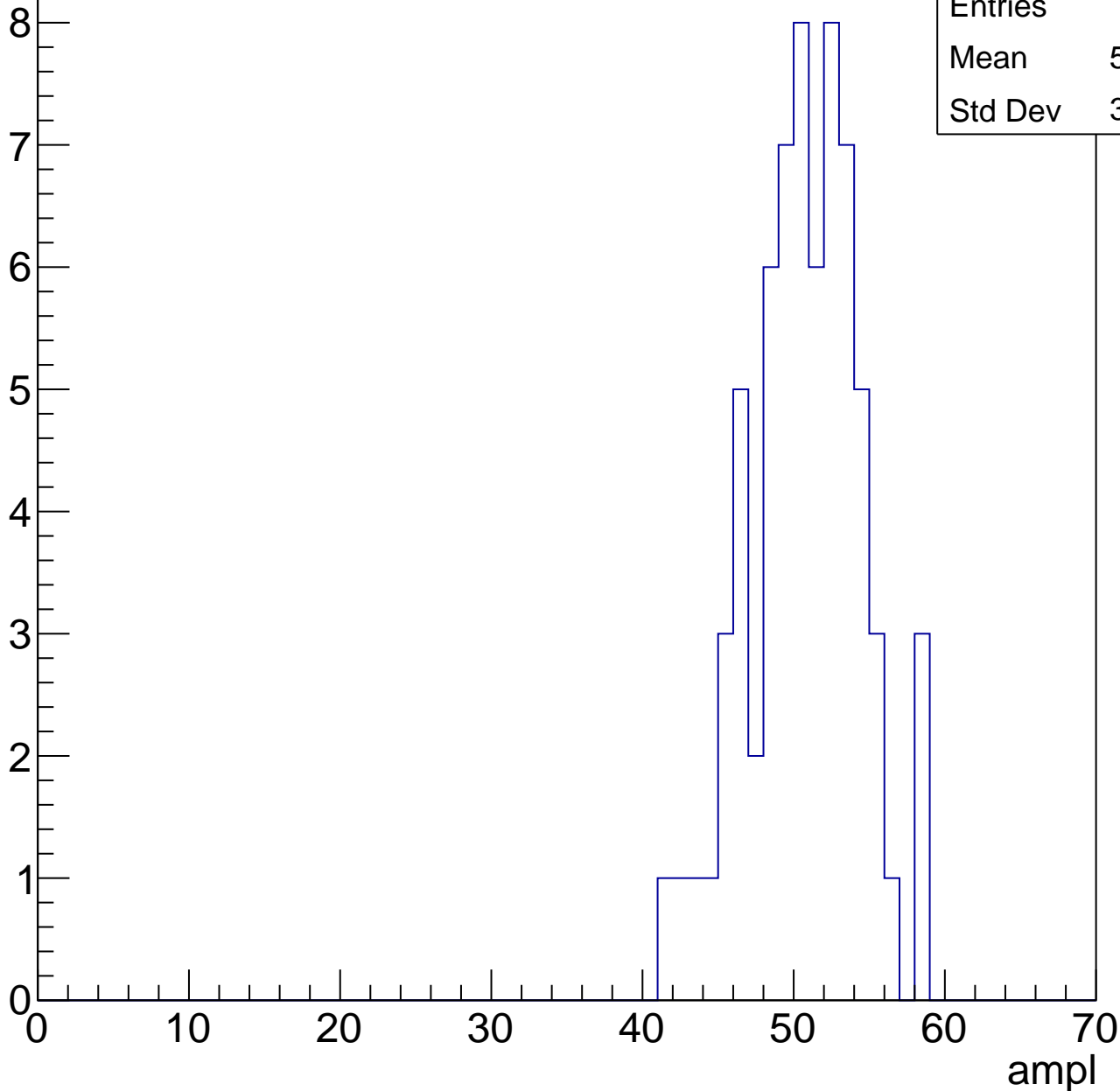


# B1L101S, U22-ch27, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	50.26
Std Dev	3.665

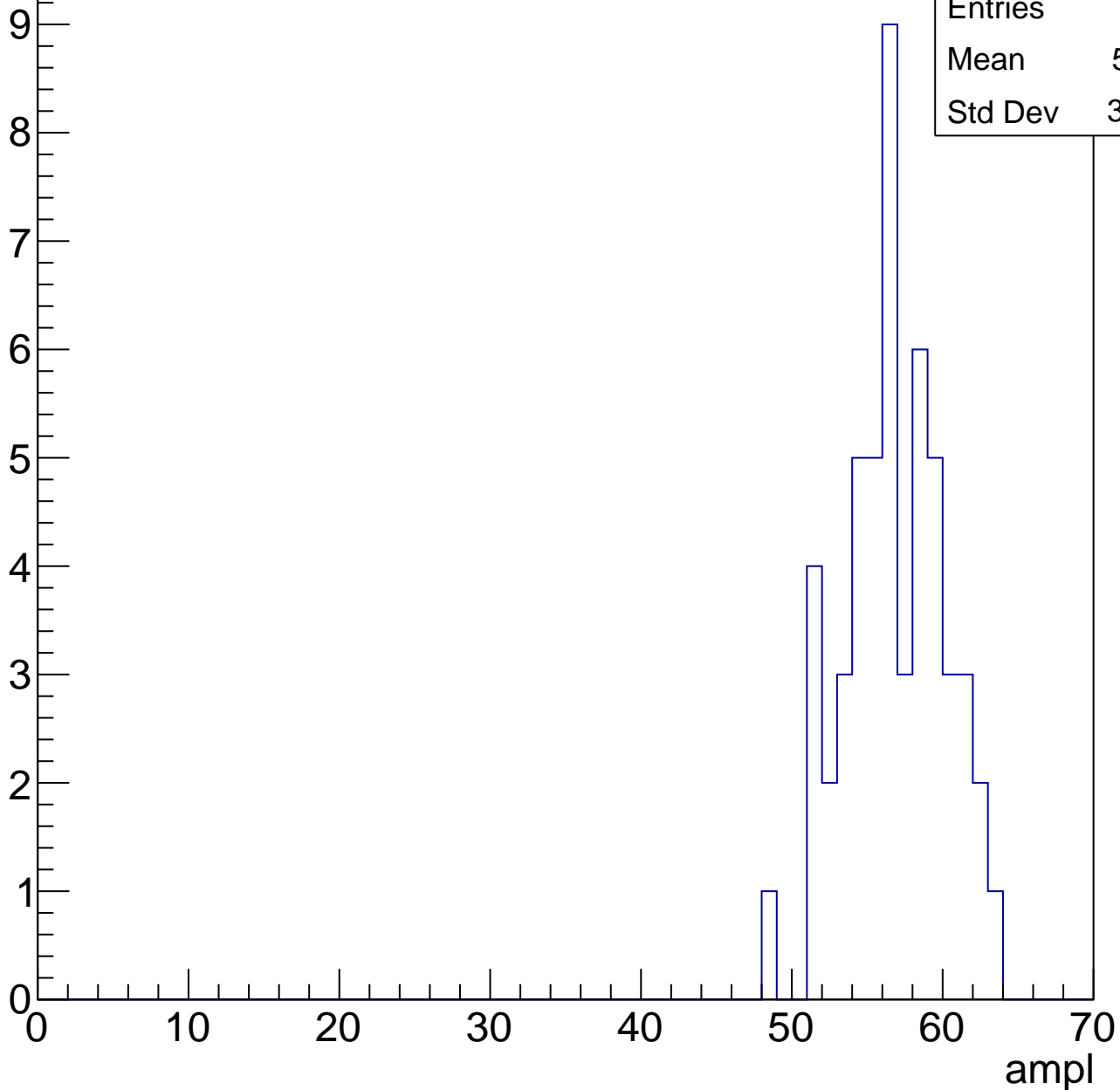


# B1L101S, U22-ch27, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	52
Mean	56.31
Std Dev	3.279



# B1L101S, U22-ch27, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

7

6

5

4

3

2

1

0

Entries 43

Mean 58.63

Std Dev 9.314

ampl

0

10

20

30

40

50

60

70

# B1L101S, U22-ch27, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U22-ch27, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L101S, U22-ch28, adc0

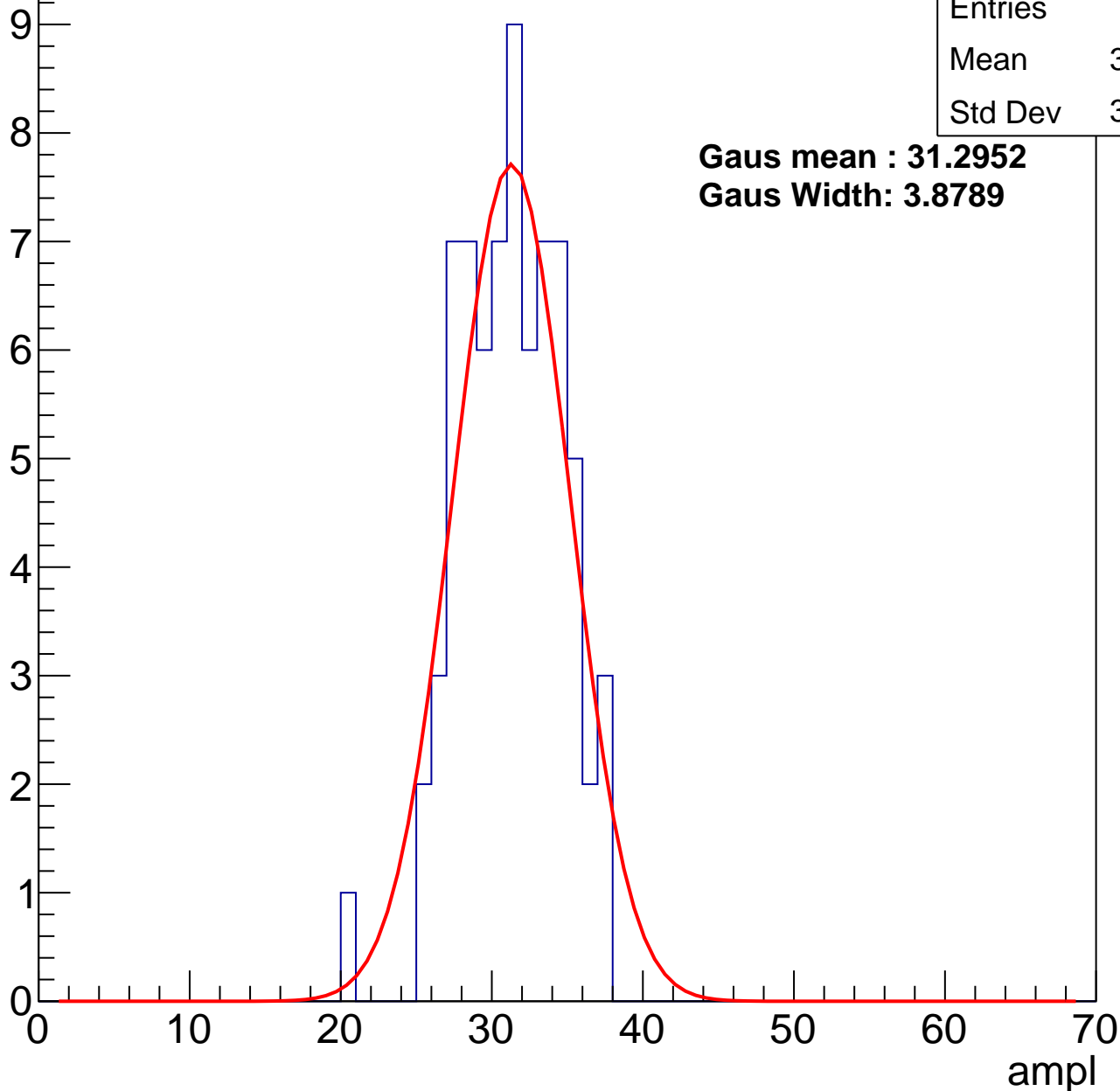
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	72
Mean	30.76
Std Dev	3.344

**Gaus mean : 31.2952**

**Gaus Width: 3.8789**



# B1L101S, U22-ch28, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	81
Mean	37.95
Std Dev	4.024

**Gaus mean : 38.3690**

**Gaus Width: 3.8942**

10

8

6

4

2

0

0

10

20

30

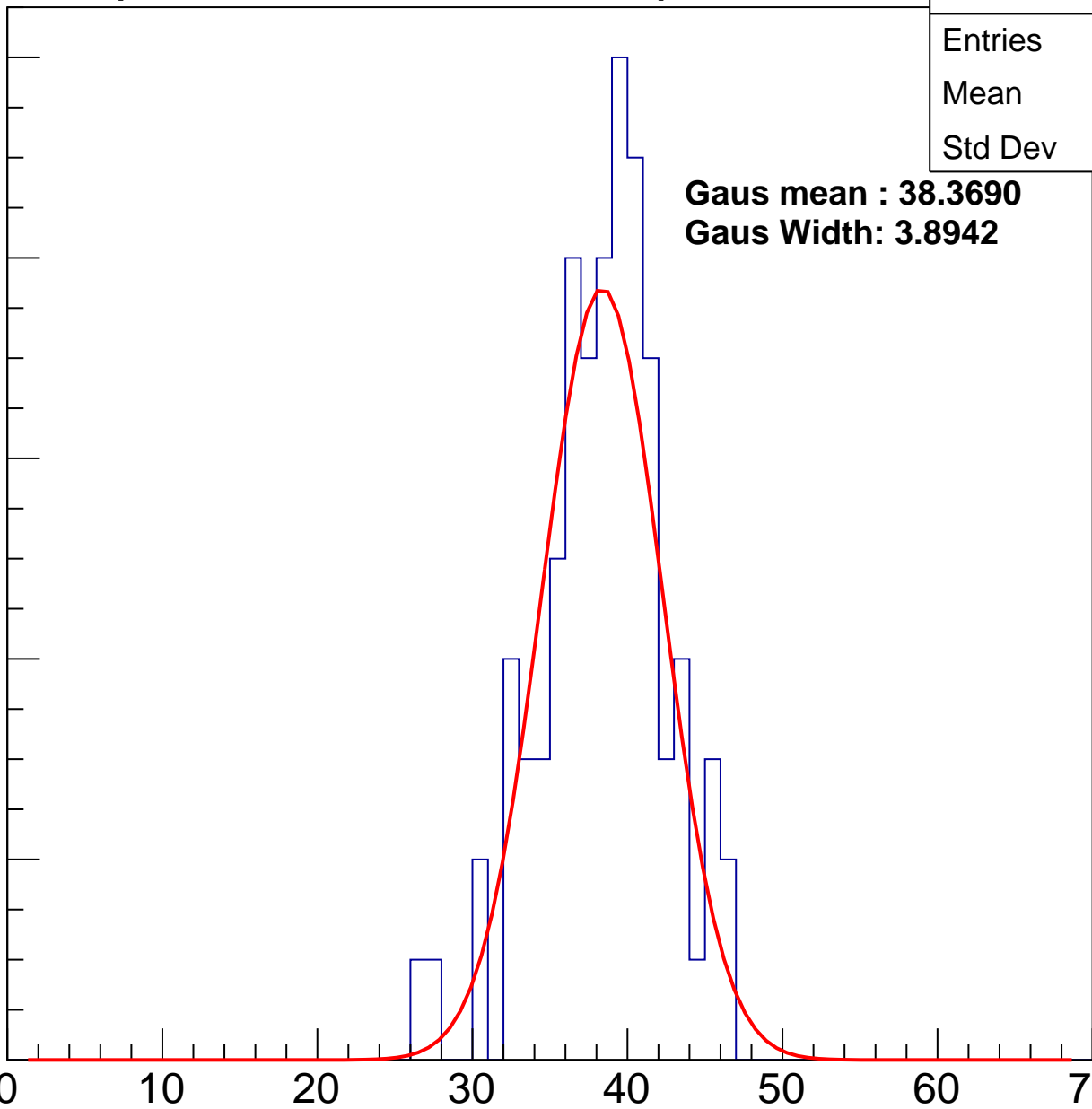
40

50

60

70

ampl



# B1L101S, U22-ch28, adc2

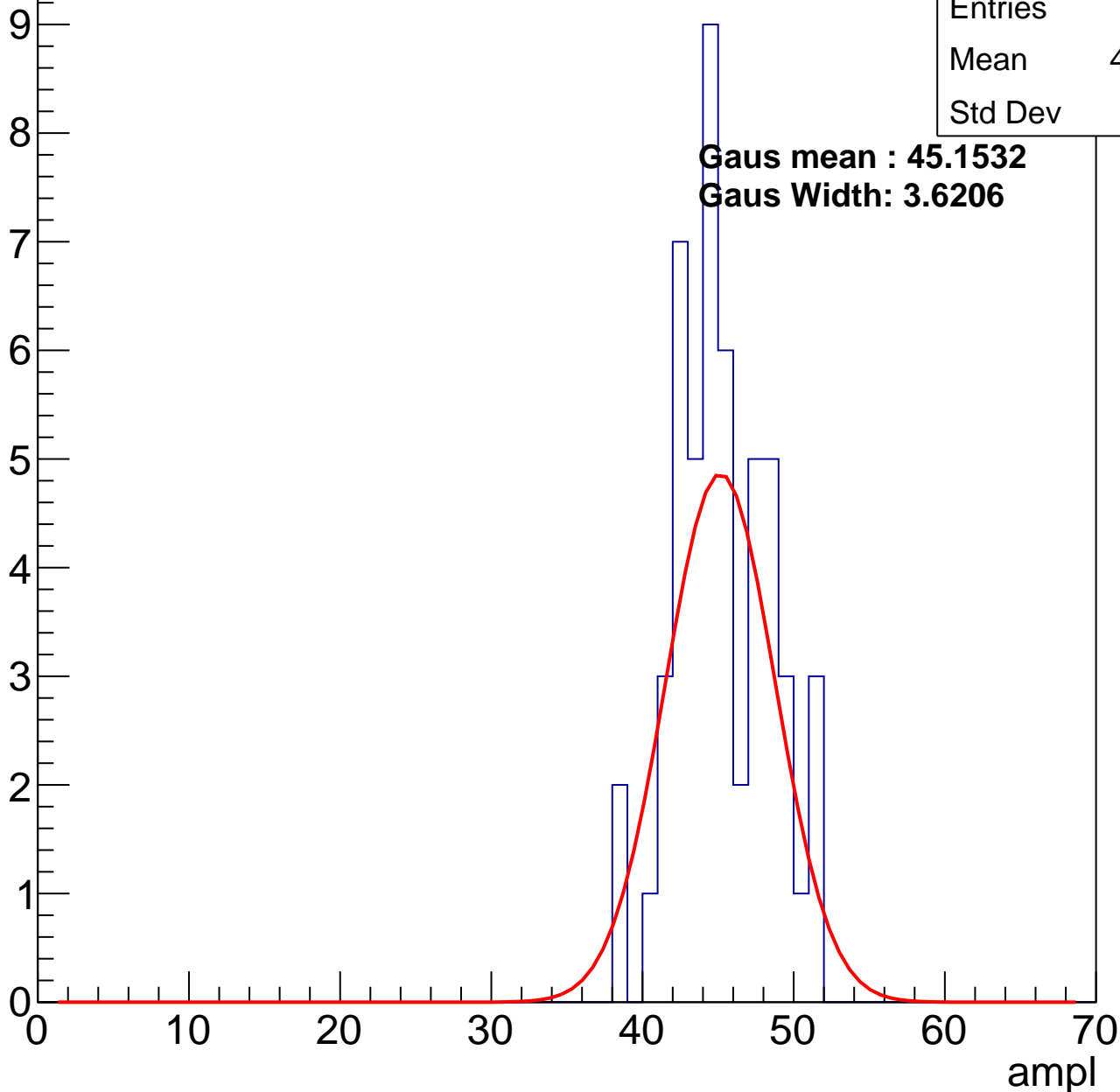
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	52
Mean	44.83
Std Dev	3.13

**Gaus mean : 45.1532**

**Gaus Width: 3.6206**



# B1L101S, U22-ch28, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	63
Mean	50.68
Std Dev	3.504

Entry

10

8

6

4

2

0

0

10

20

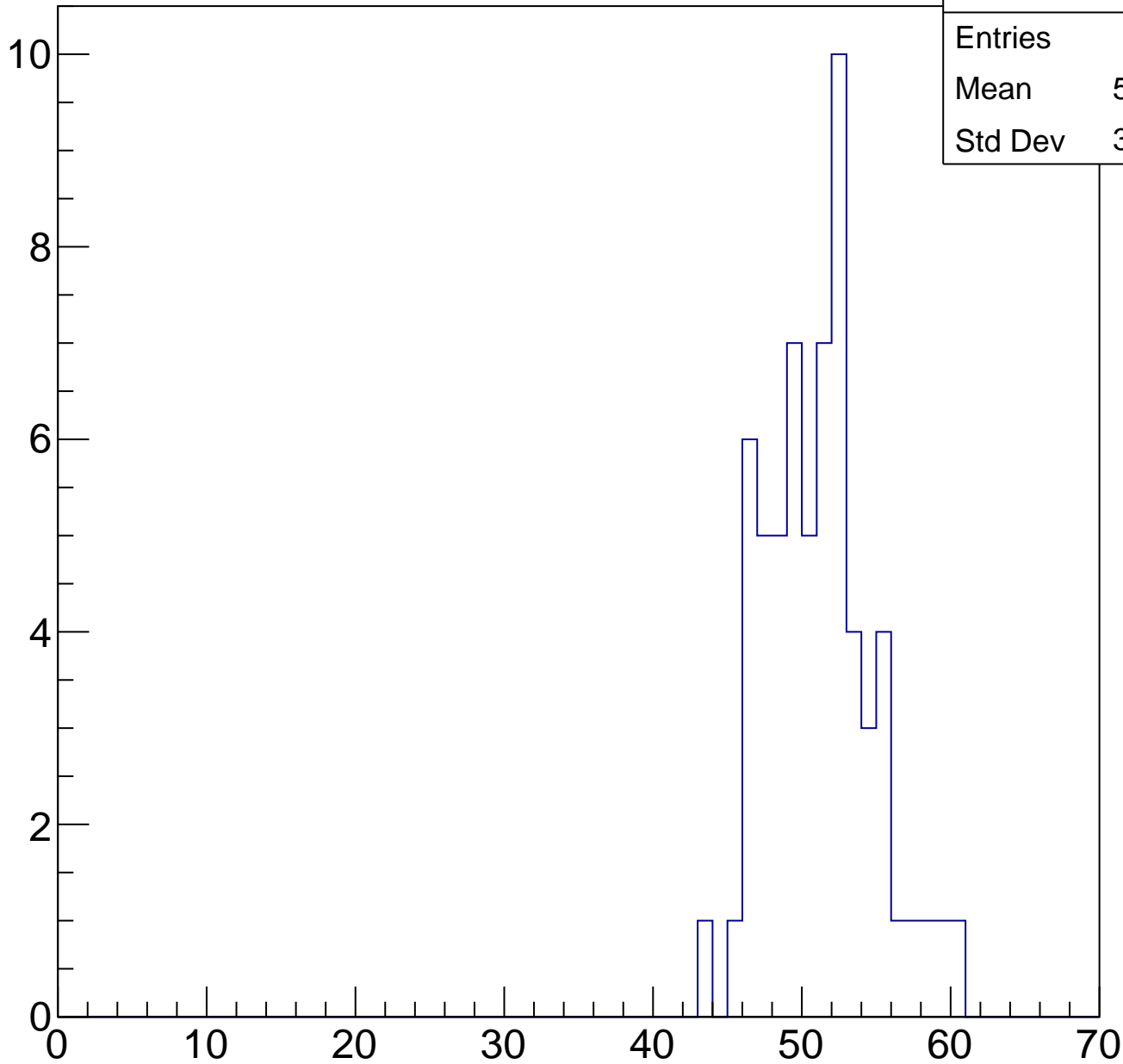
30

40

50

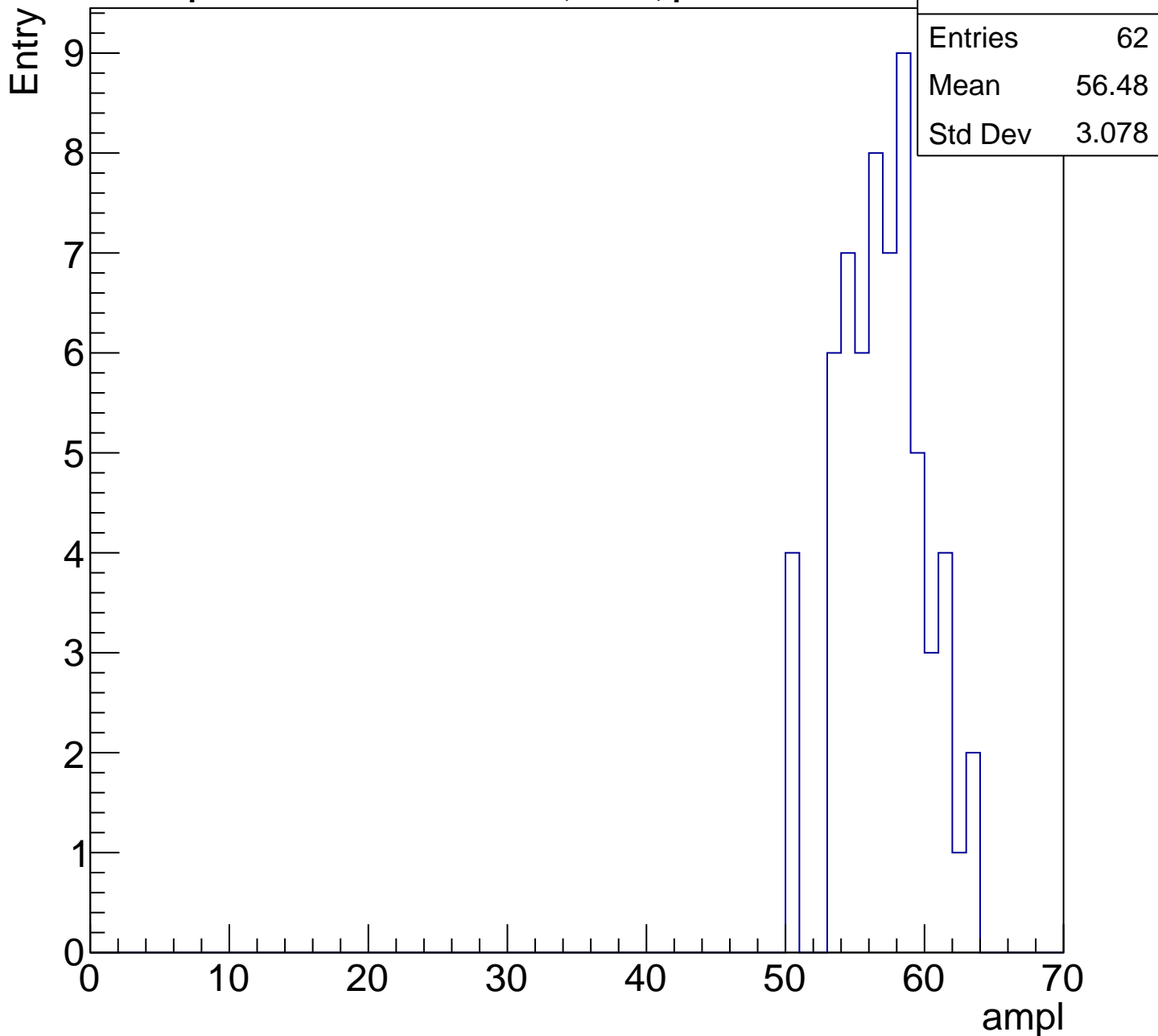
60

ampl



# B1L101S, U22-ch28, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

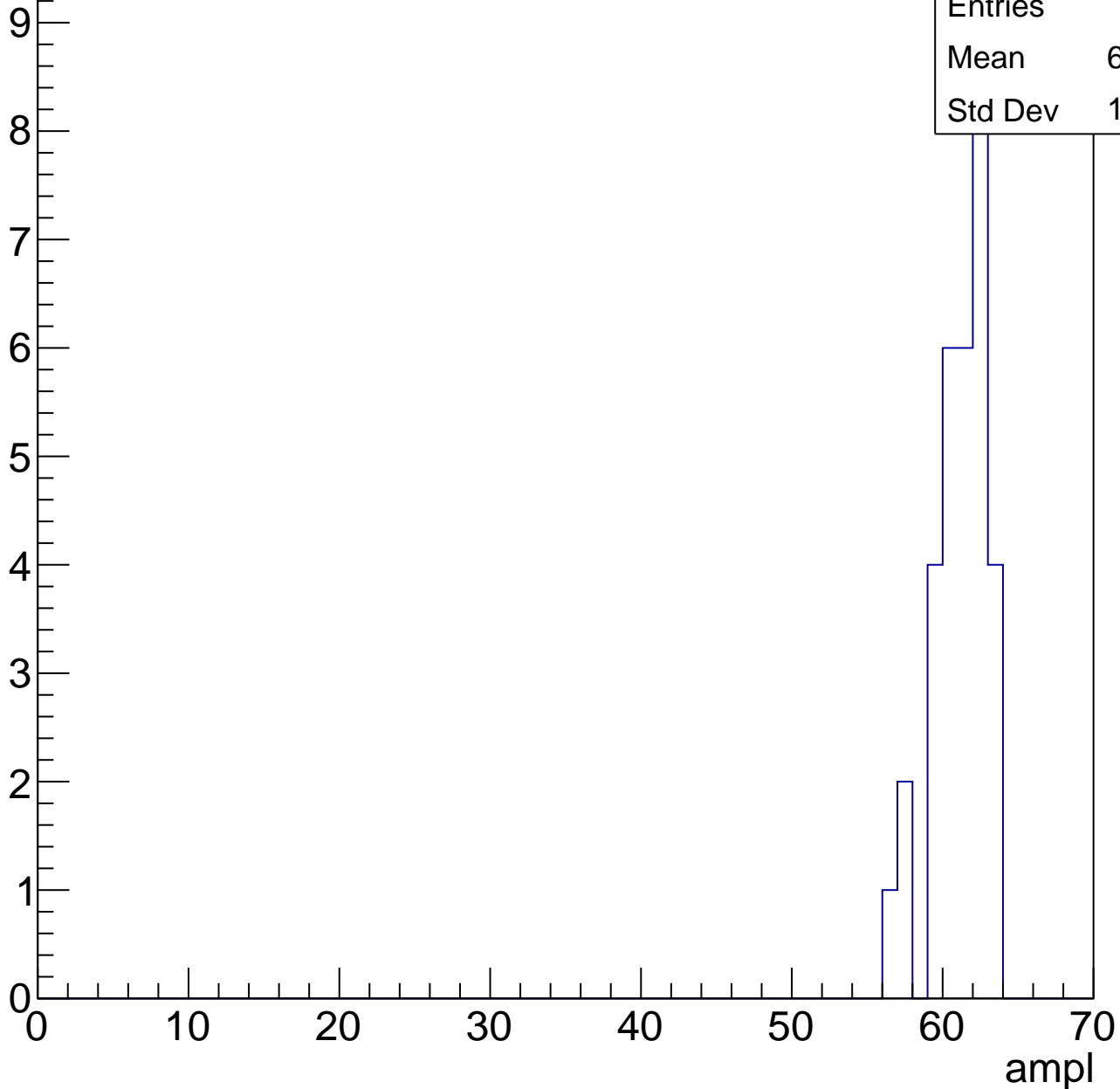


# B1L101S, U22-ch28, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

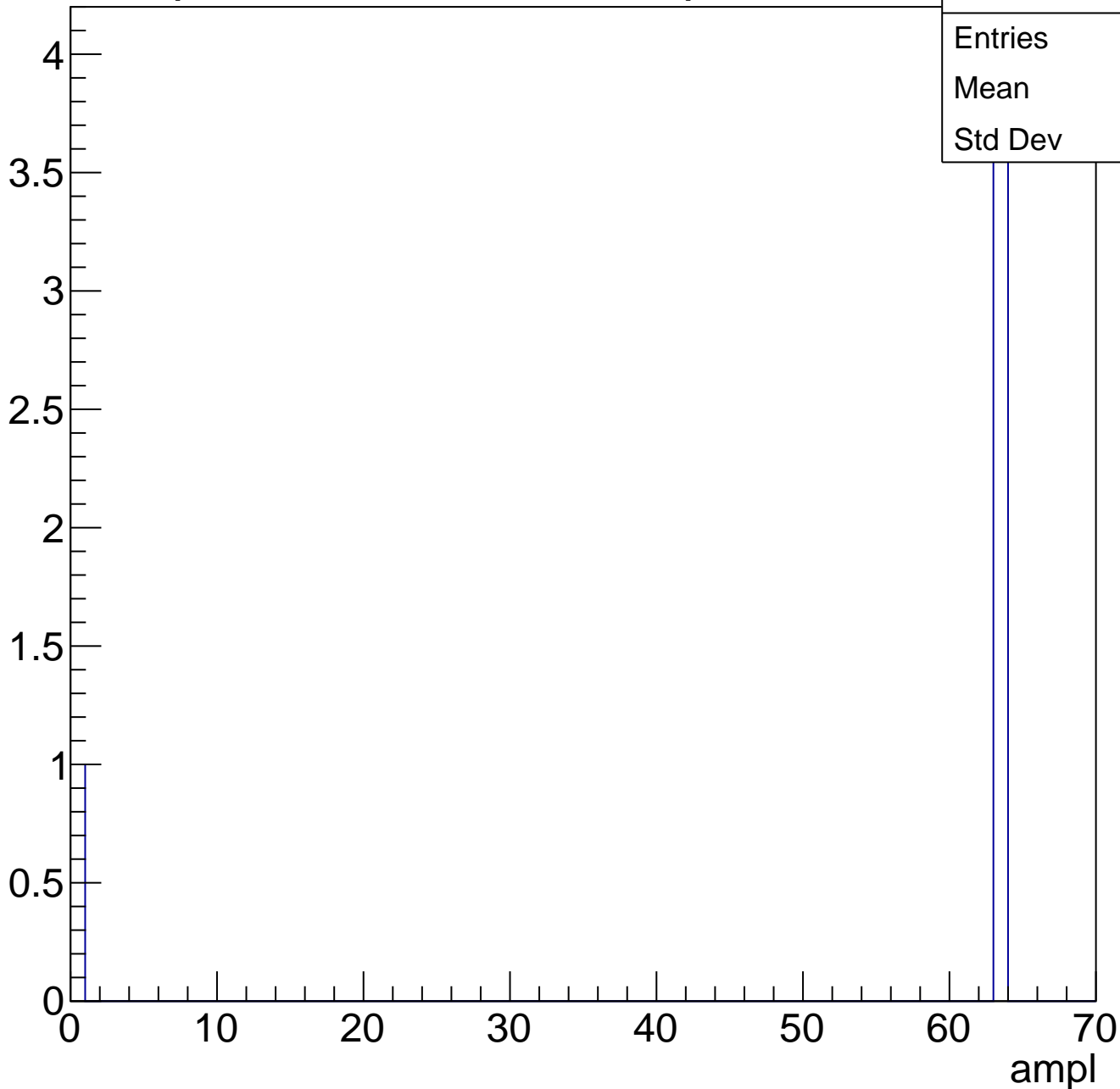
Entries	32
Mean	60.69
Std Dev	1.775



# B1L101S, U22-ch28, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U22-ch28, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U22-ch29, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	80
Mean	30.56
Std Dev	5.869

**Gaus mean : 31.9740**

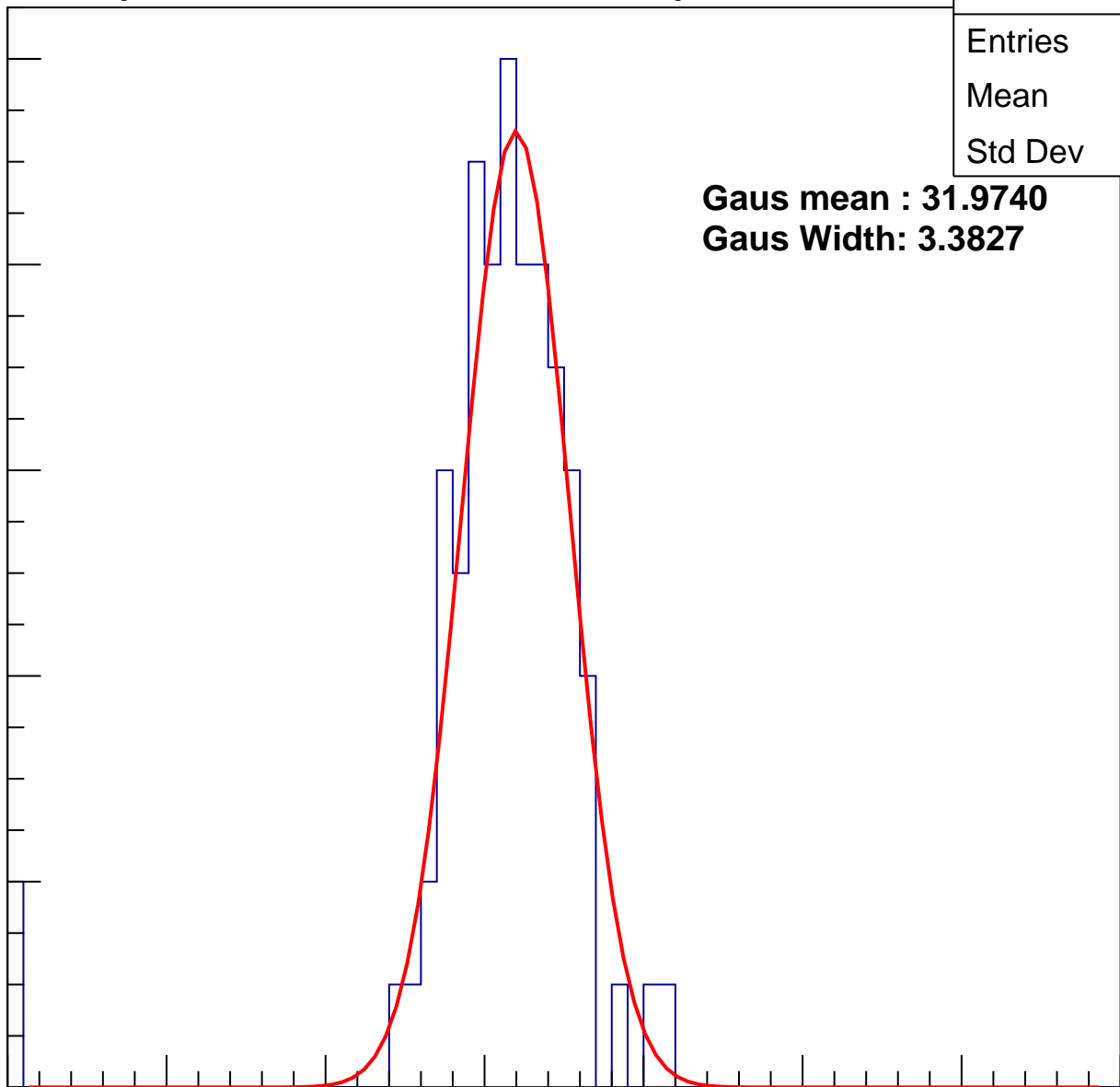
**Gaus Width: 3.3827**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U22-ch29, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	60
Mean	38.13
Std Dev	3.149

**Gaus mean : 38.6204**

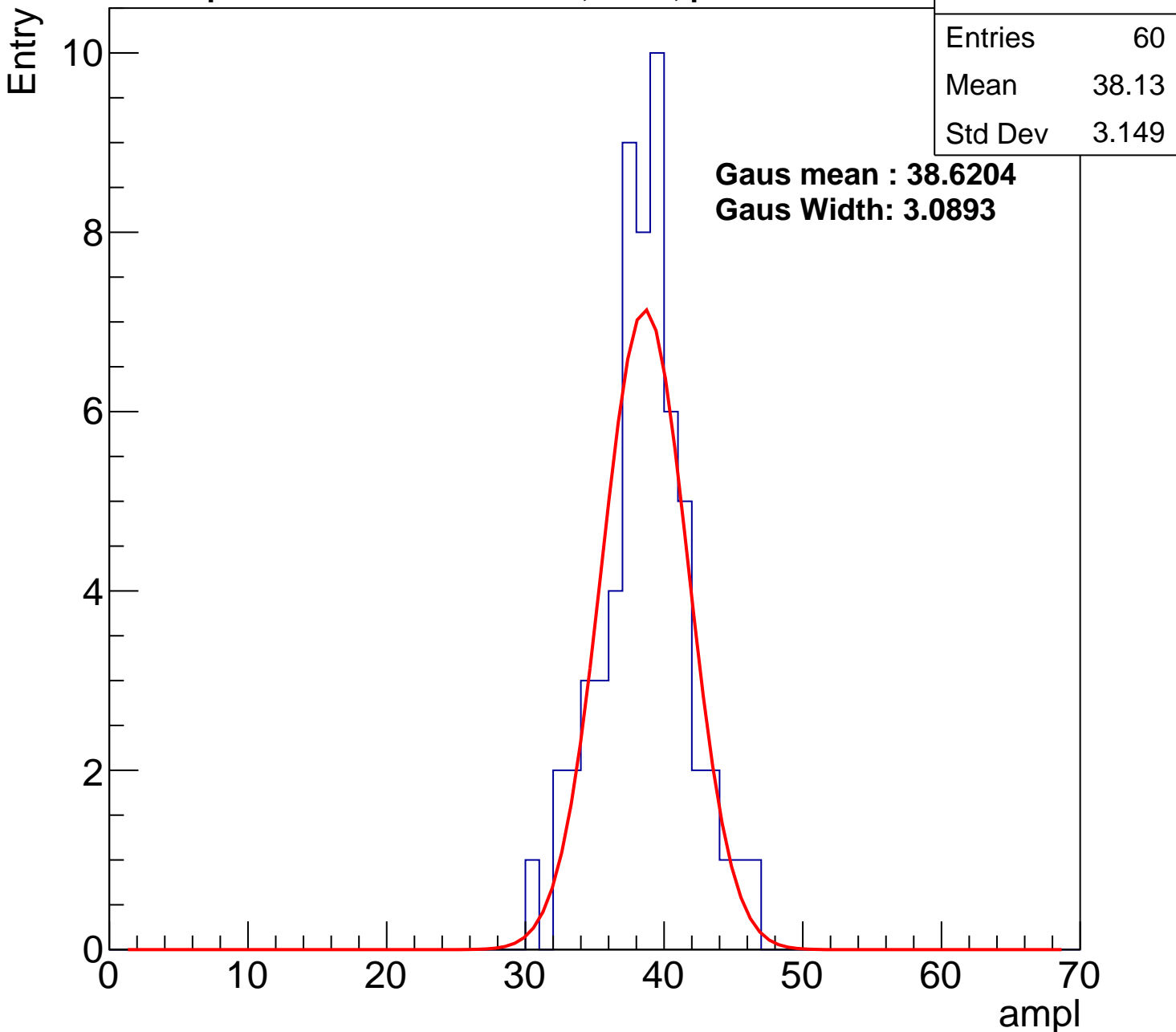
**Gaus Width: 3.0893**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U22-ch29, adc2

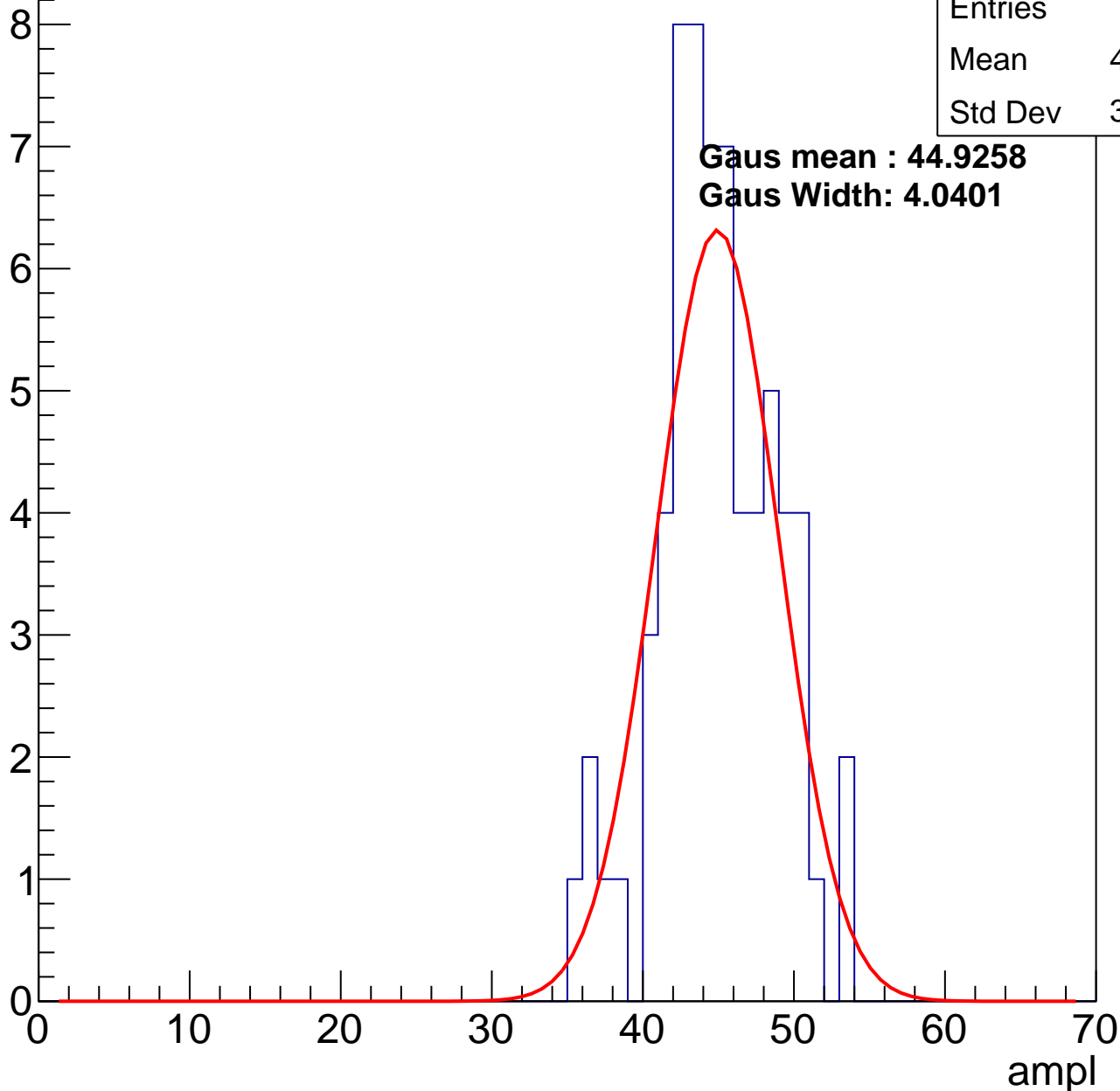
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	66
Mean	44.45
Std Dev	3.889

**Gaus mean : 44.9258**

**Gaus Width: 4.0401**



# B1L101S, U22-ch29, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

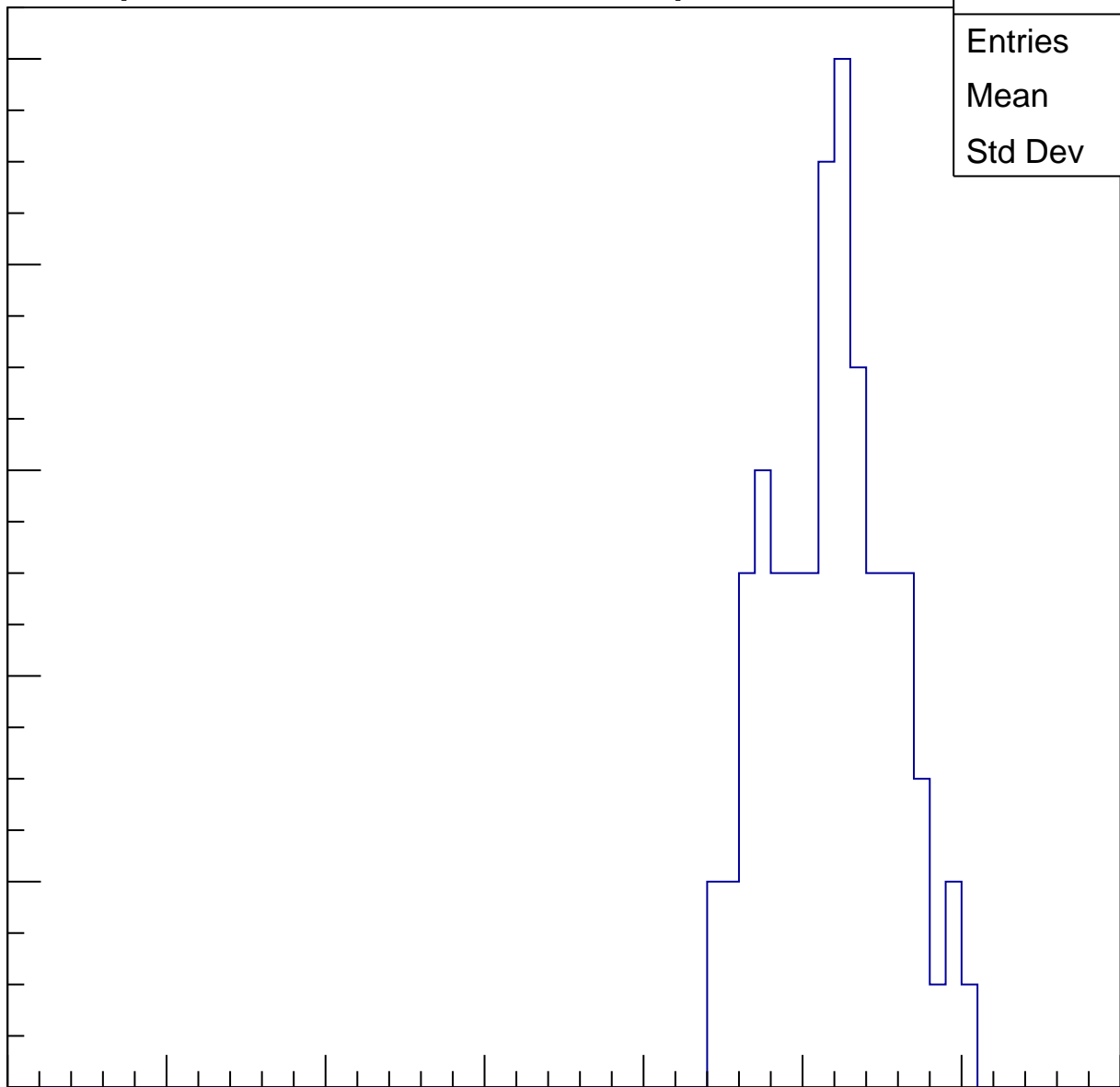
Entries	78
Mean	51.37
Std Dev	3.763

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

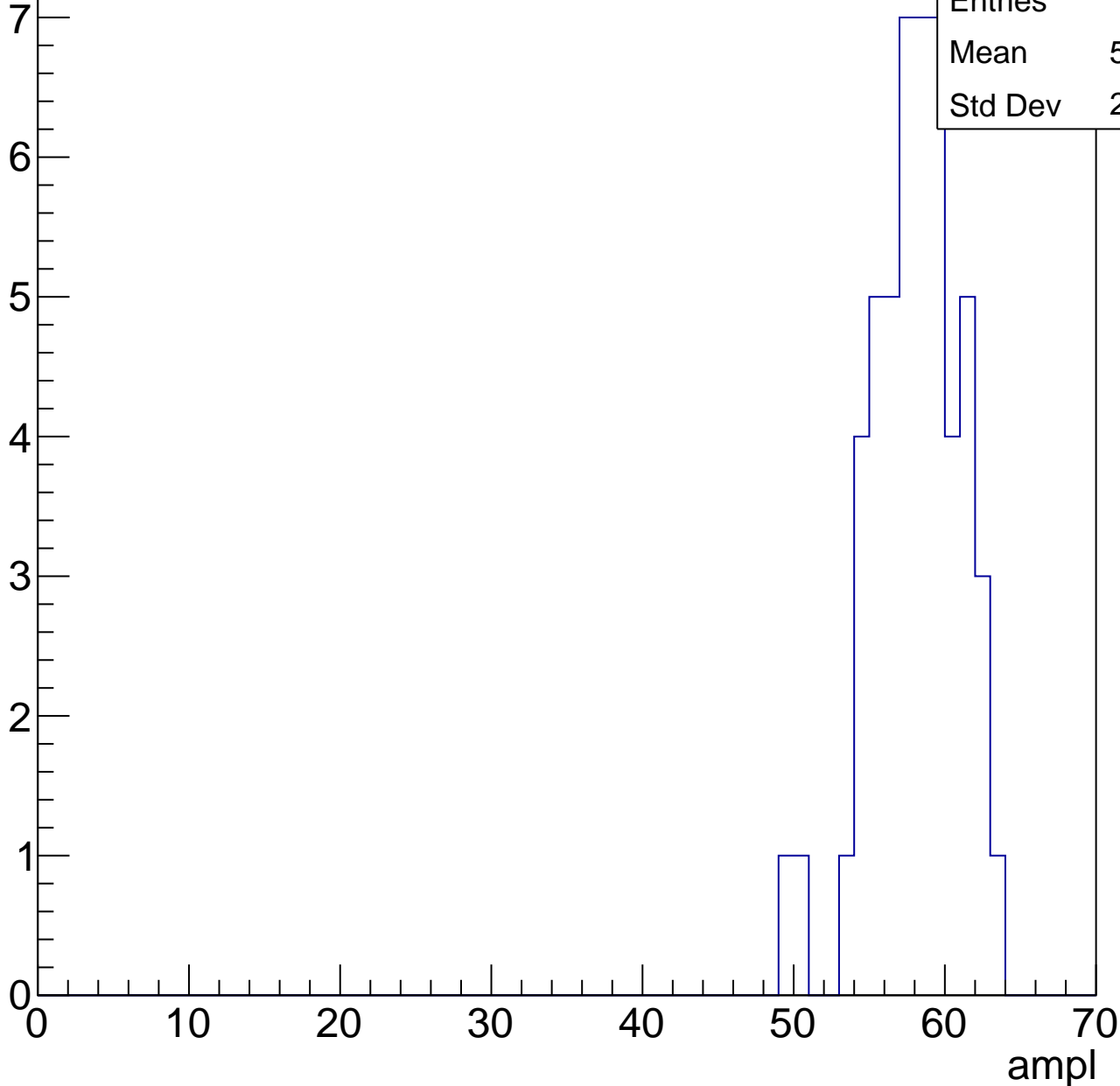


# B1L101S, U22-ch29, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	51
Mean	57.55
Std Dev	2.926

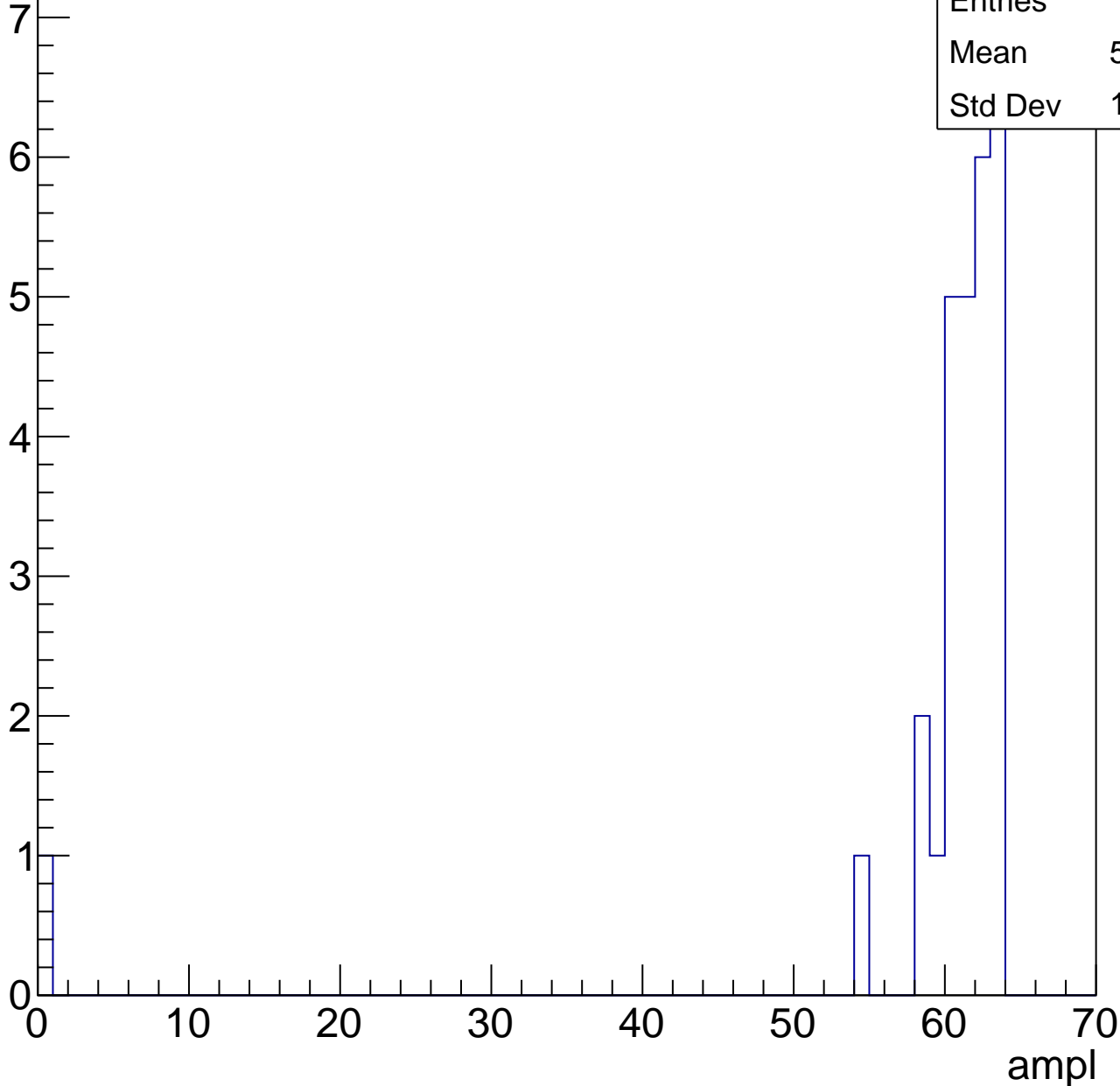


# B1L101S, U22-ch29, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	28
Mean	58.82
Std Dev	11.49



# B1L101S, U22-ch29, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U22-ch29, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U22-ch30, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	96
Mean	30.43
Std Dev	3.793

**Gaus mean : 31.0214**

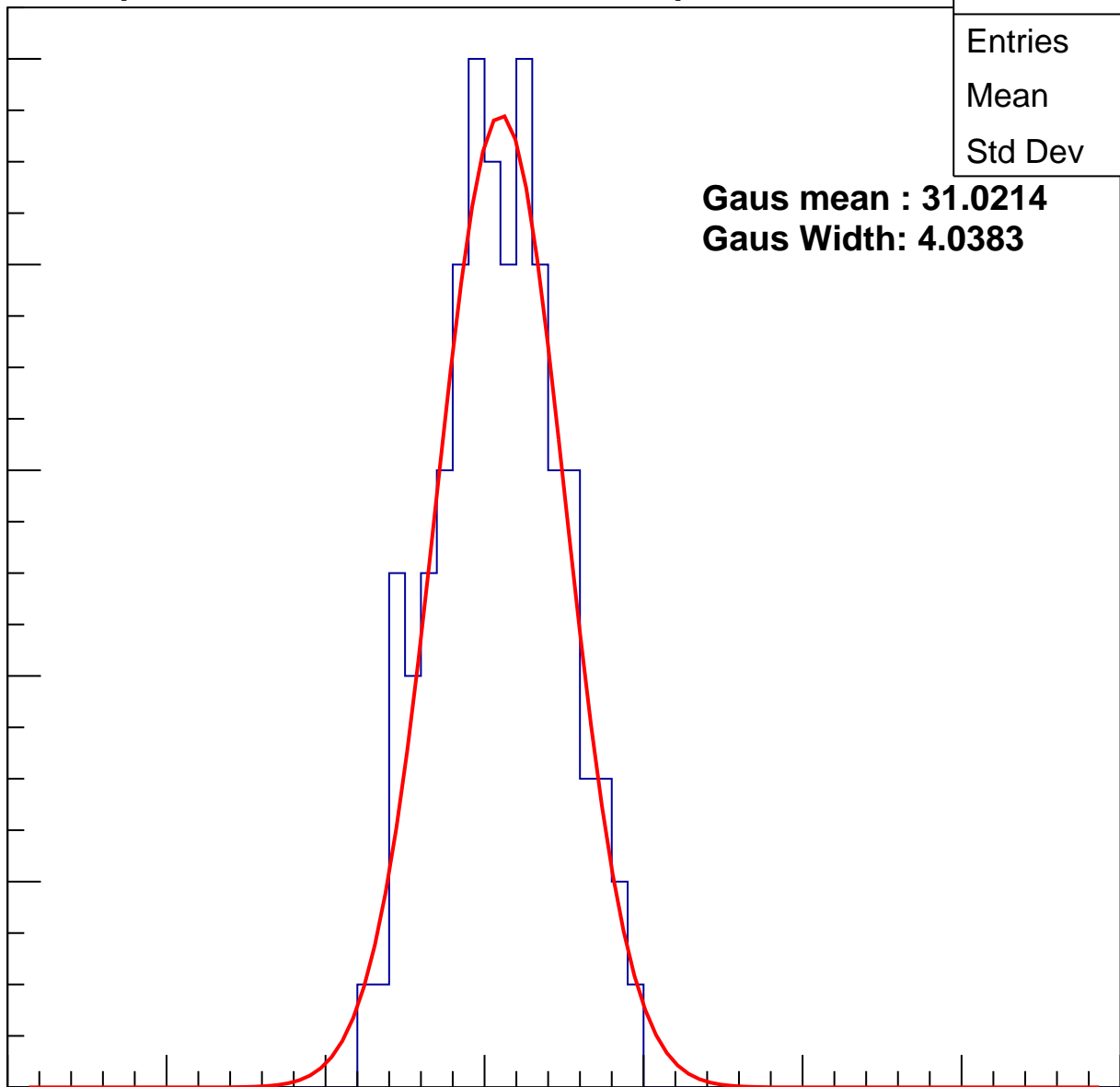
**Gaus Width: 4.0383**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U22-ch30, adc1

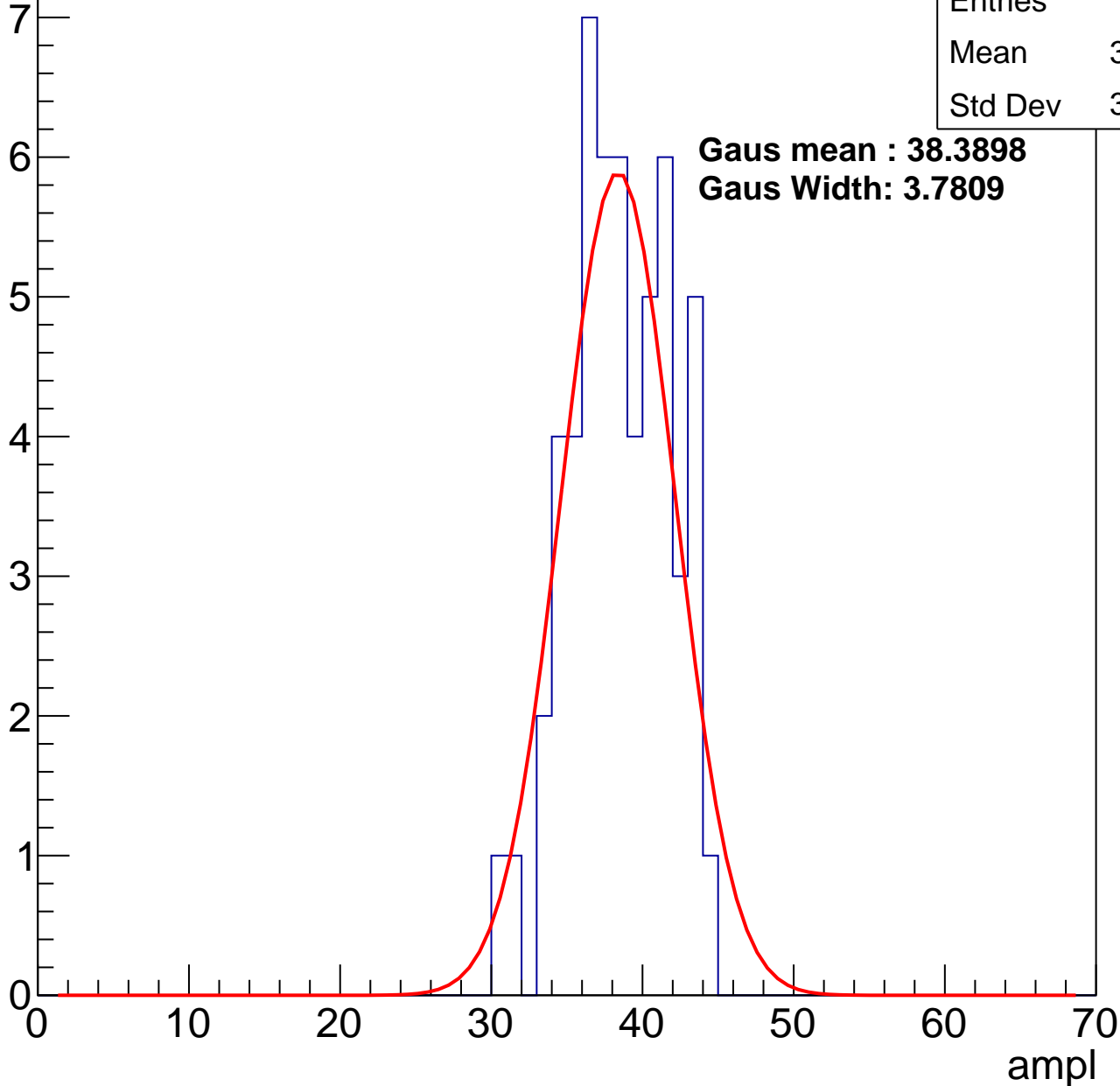
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	55
Mean	38.04
Std Dev	3.258

**Gaus mean : 38.3898**

**Gaus Width: 3.7809**



# B1L101S, U22-ch30, adc2

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	79
Mean	44.7
Std Dev	3.705

**Gaus mean : 45.2089**

**Gaus Width: 4.1713**

10

8

6

4

2

0

0

10

20

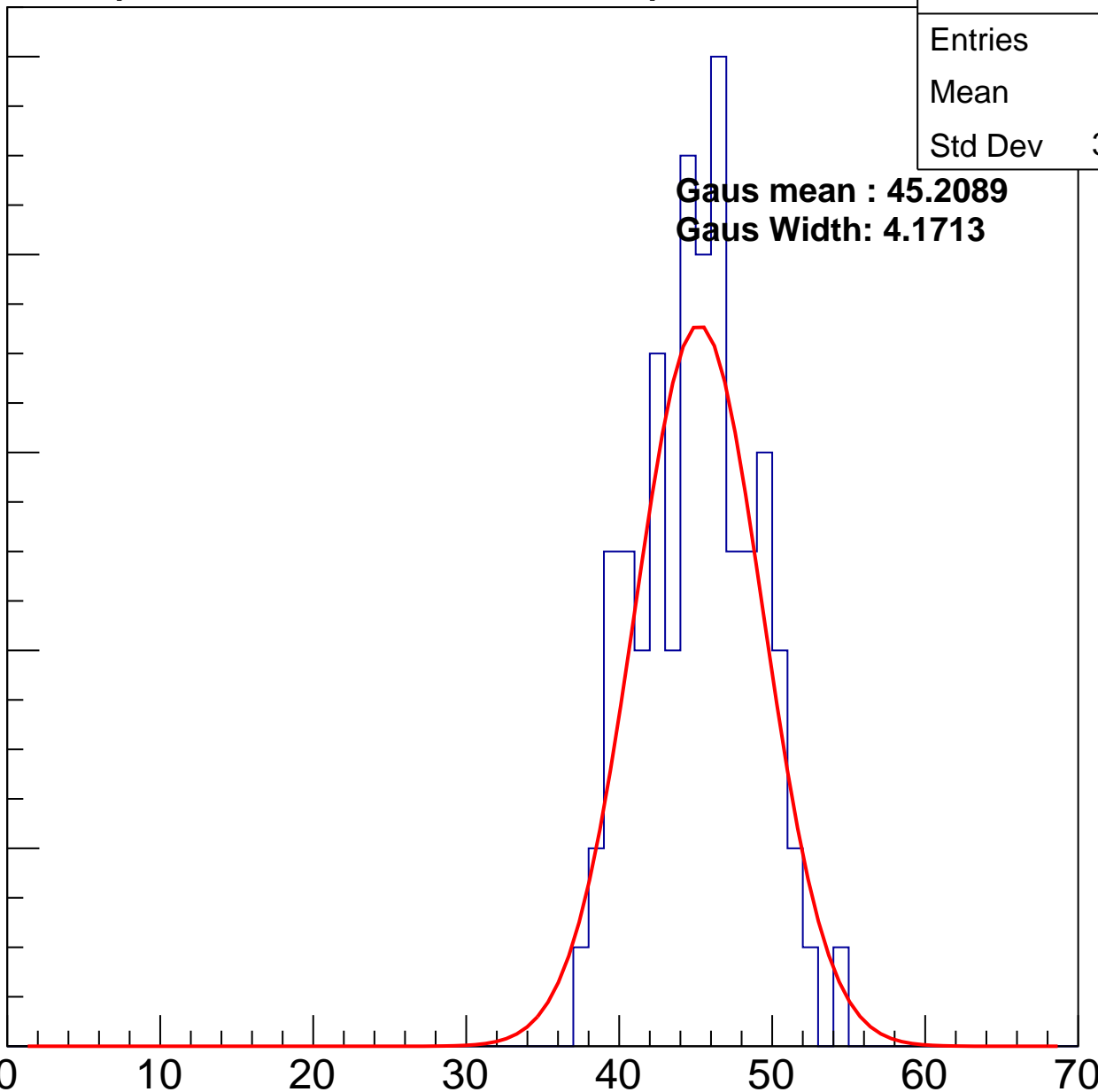
30

40

50

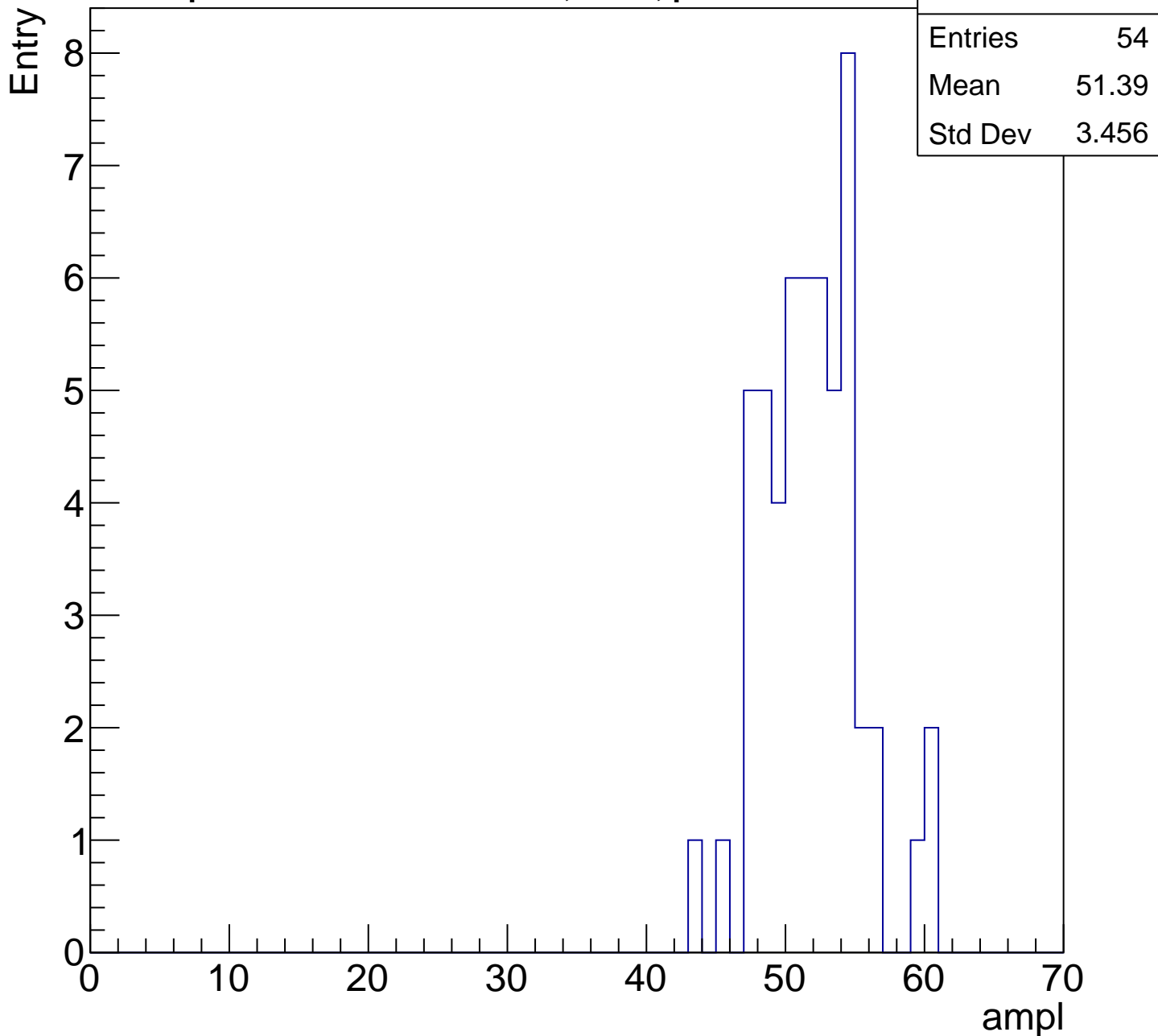
60

ampl



# B1L101S, U22-ch30, adc3

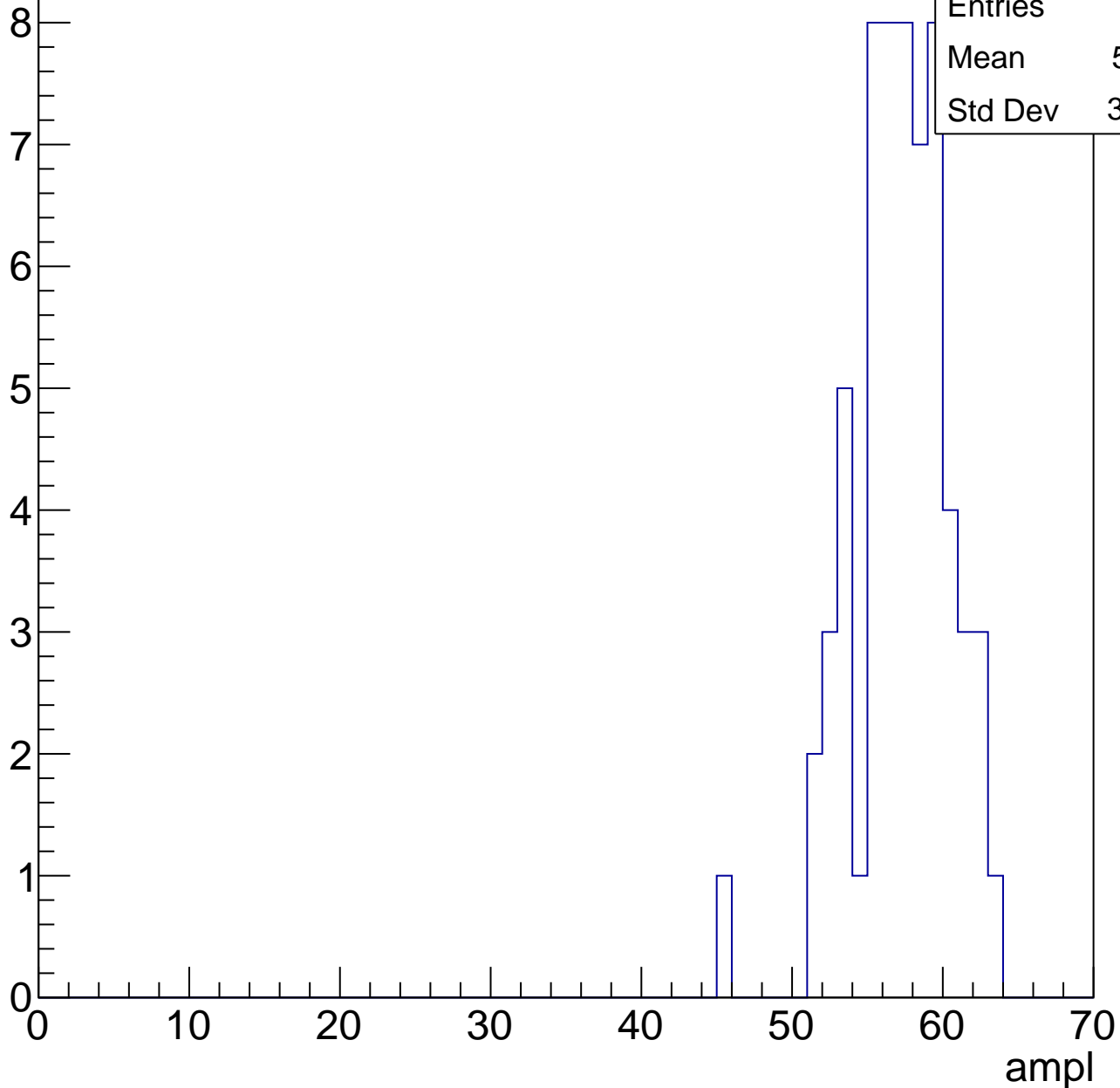
calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U22-ch30, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

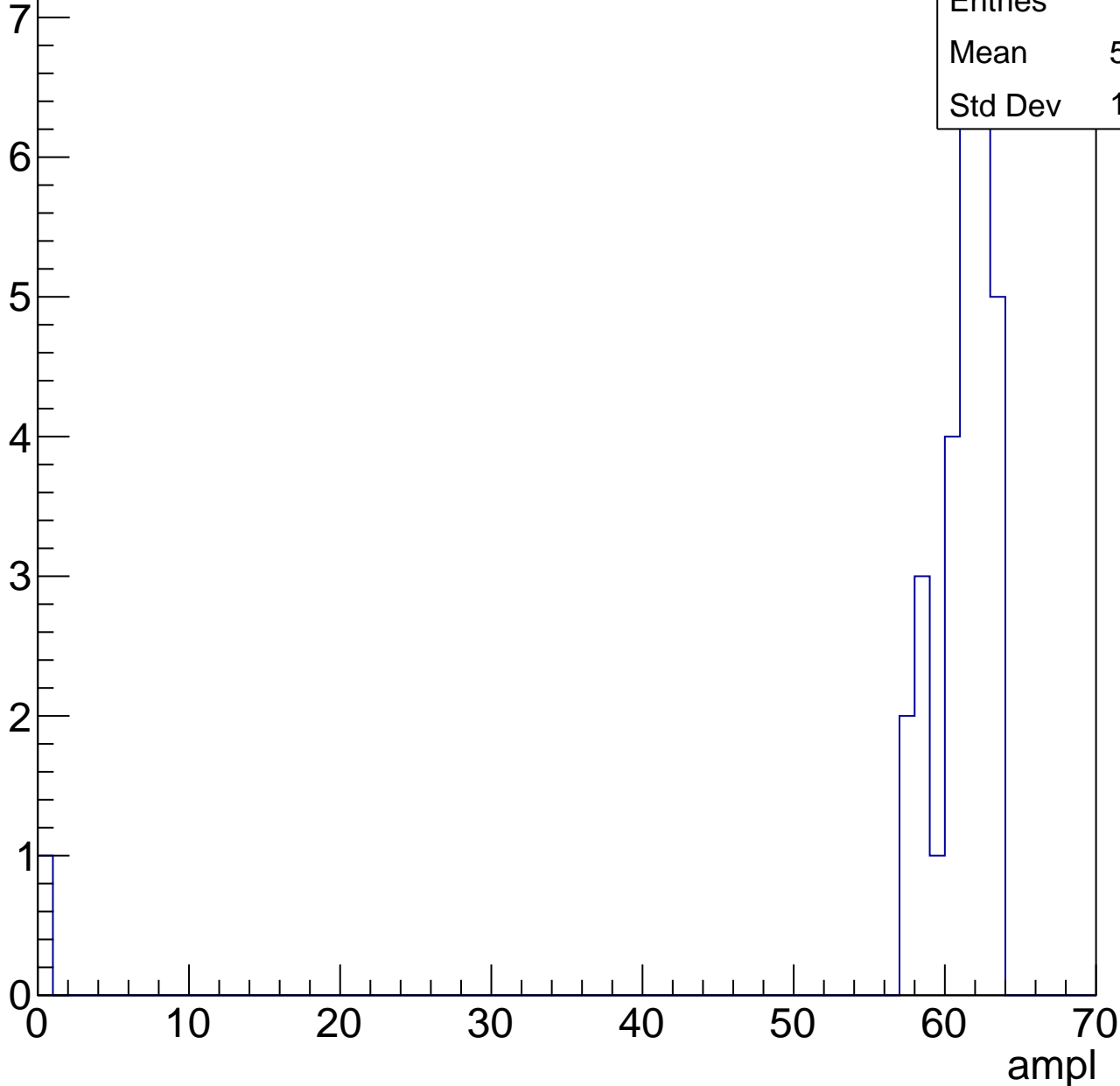


# B1L101S, U22-ch30, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

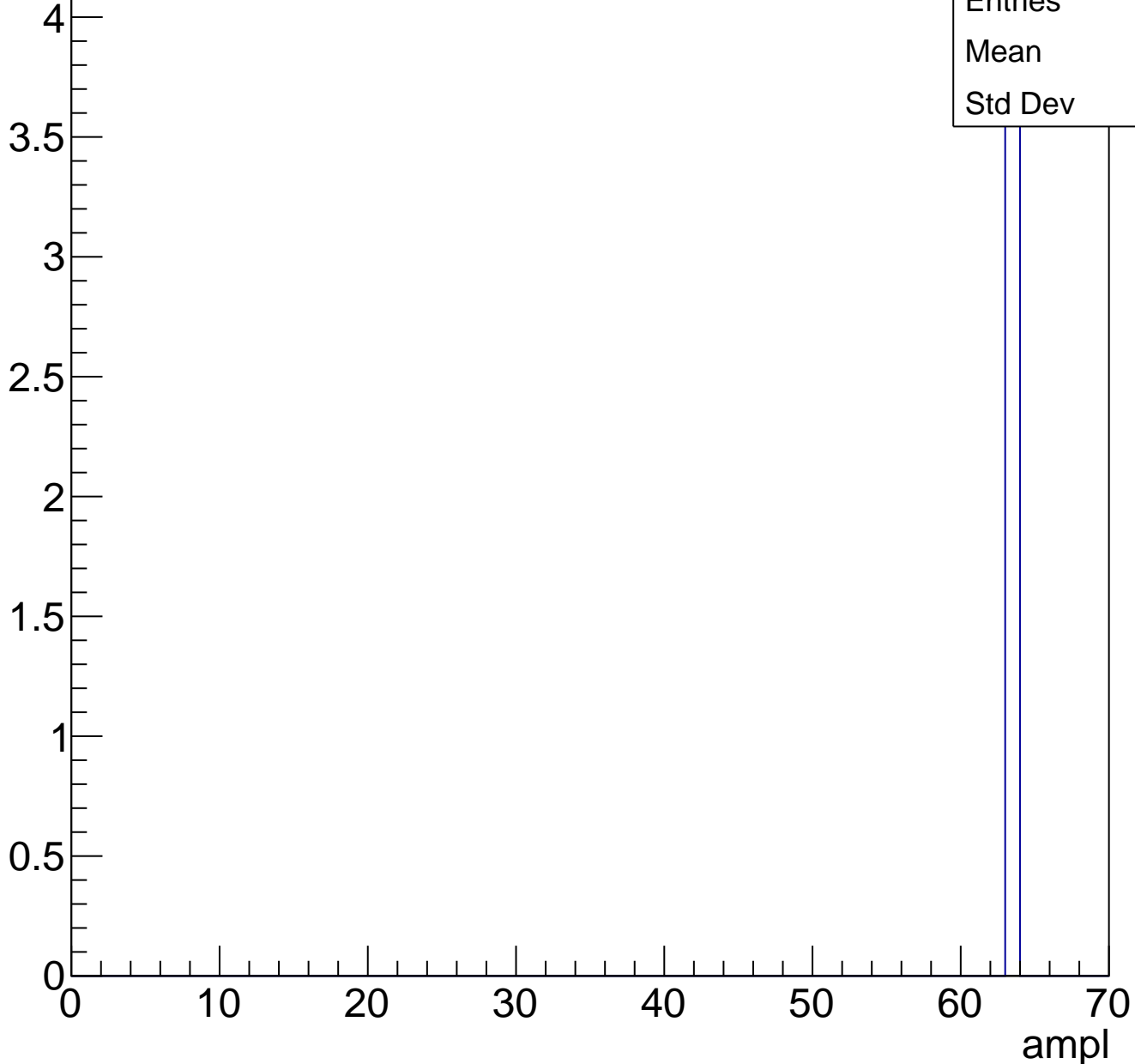
Entries	30
Mean	58.77
Std Dev	11.05



# B1L101S, U22-ch30, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U22-ch30, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	3
Mean	7
Std Dev	9.899

# B1L101S, U22-ch31, adc0

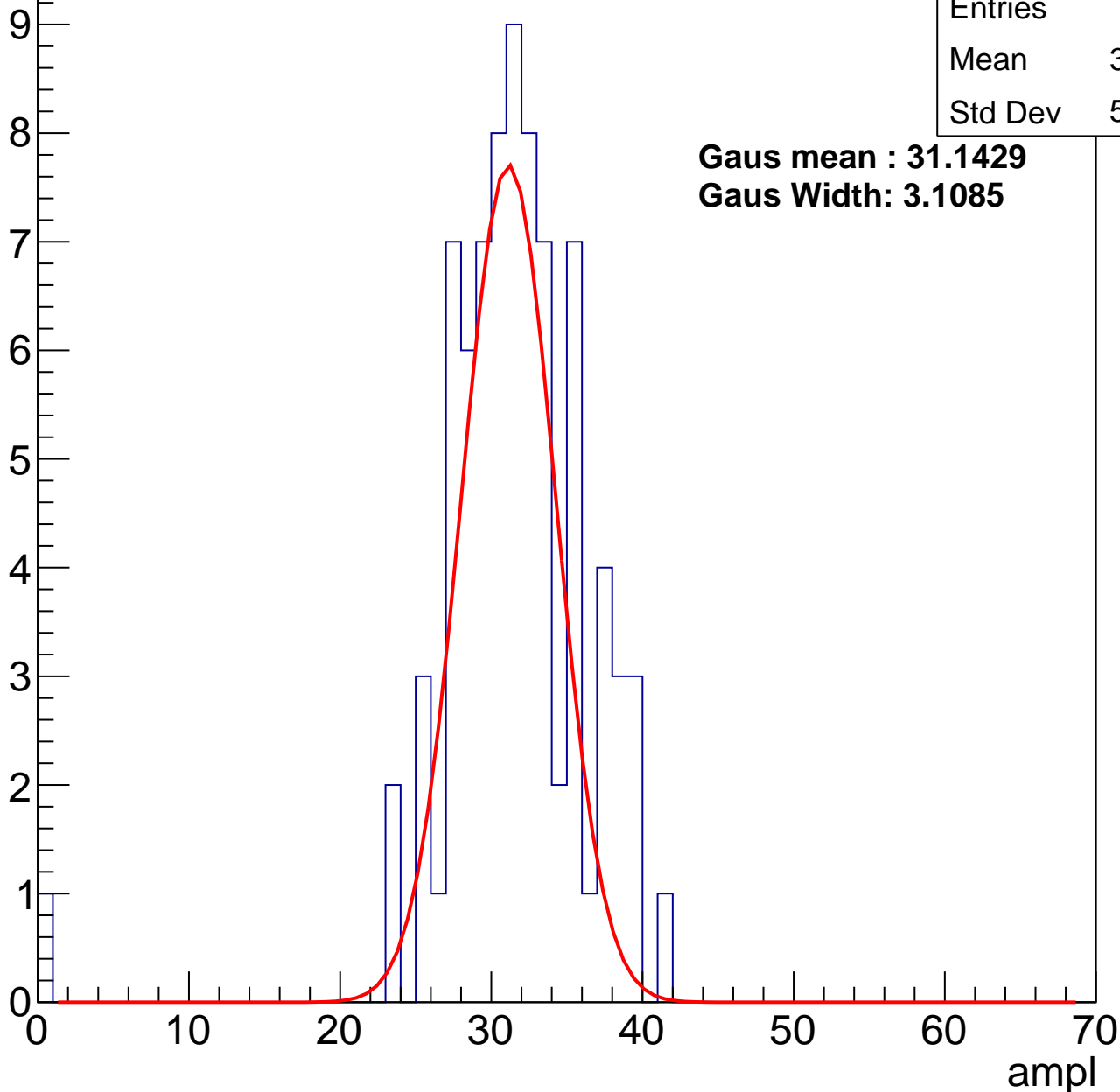
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	80
Mean	31.02
Std Dev	5.242

**Gaus mean : 31.1429**

**Gaus Width: 3.1085**



# B1L101S, U22-ch31, adc1

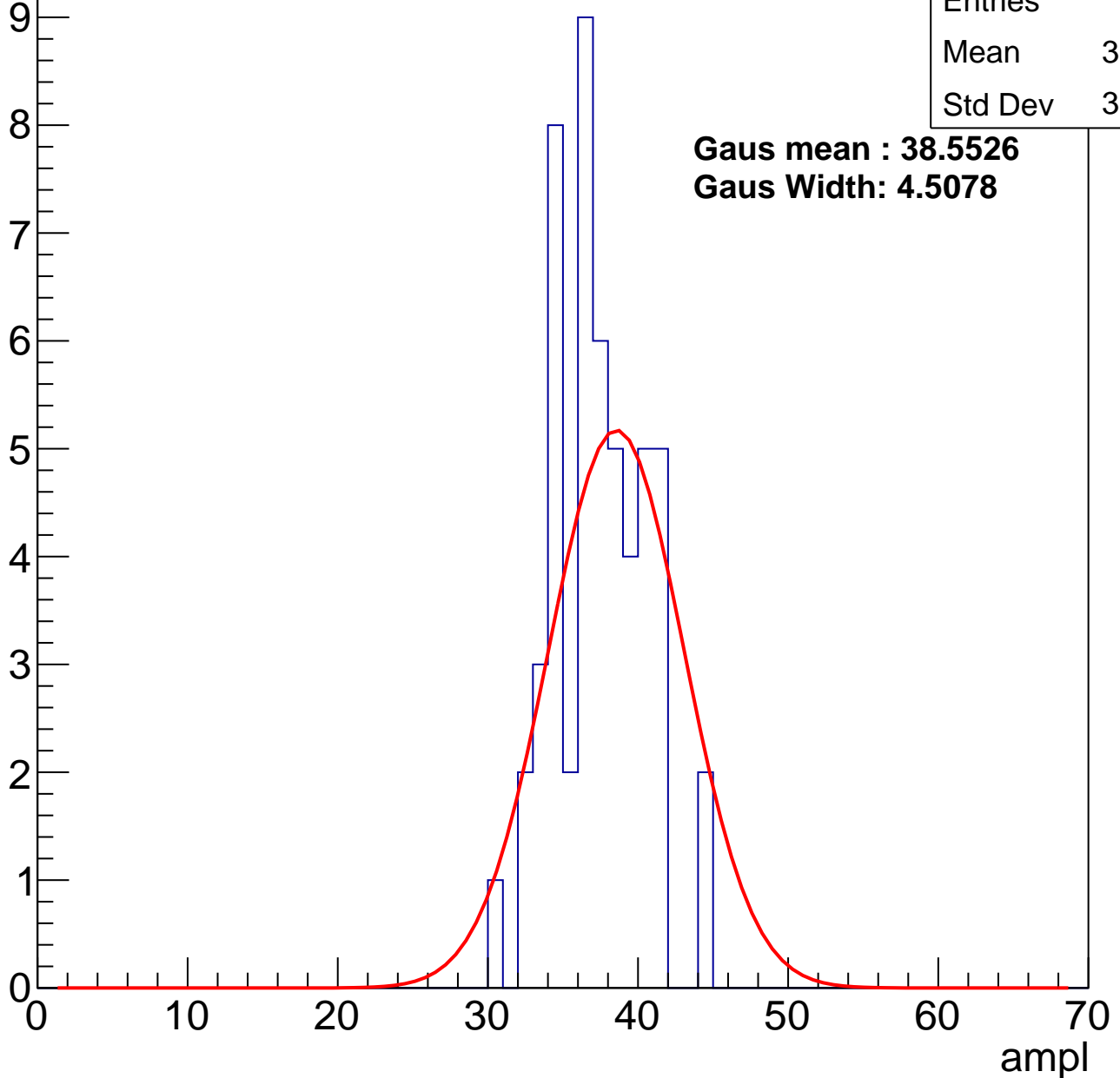
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	52
Mean	36.92
Std Dev	3.037

**Gaus mean : 38.5526**

**Gaus Width: 4.5078**



# B1L101S, U22-ch31, adc2

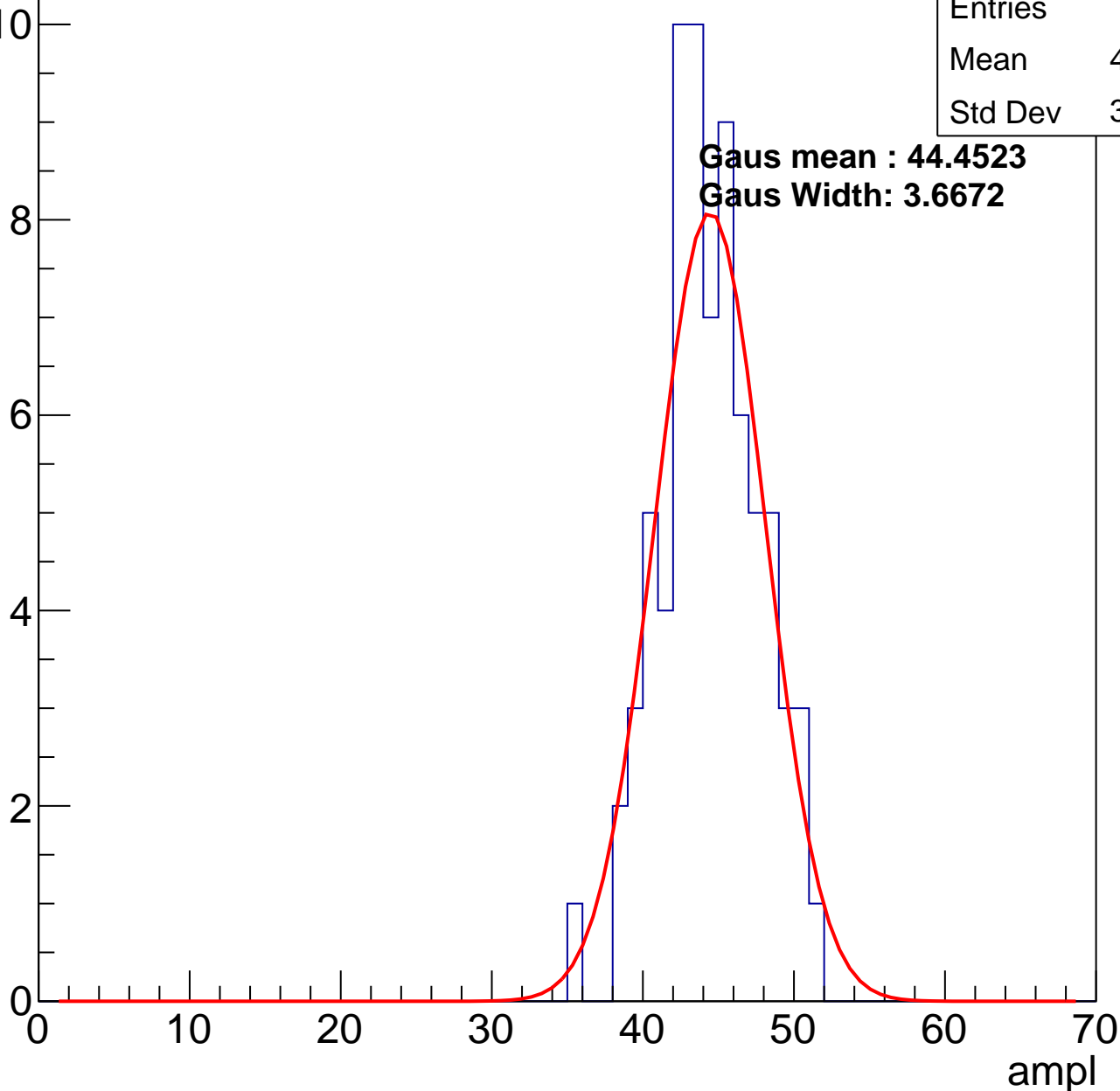
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	74
Mean	43.97
Std Dev	3.255

**Gaus mean : 44.4523**

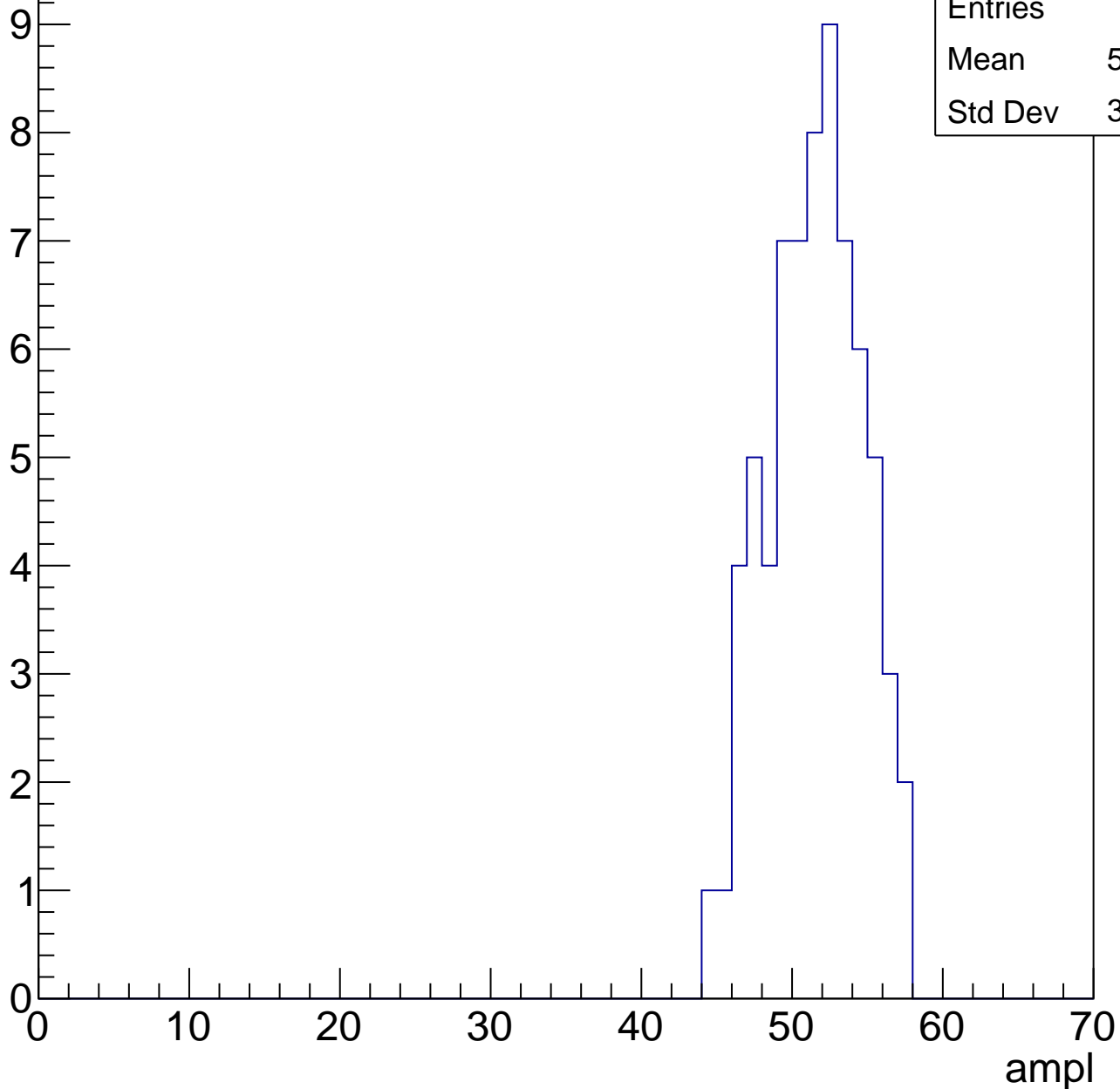
**Gaus Width: 3.6672**



# B1L101S, U22-ch31, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

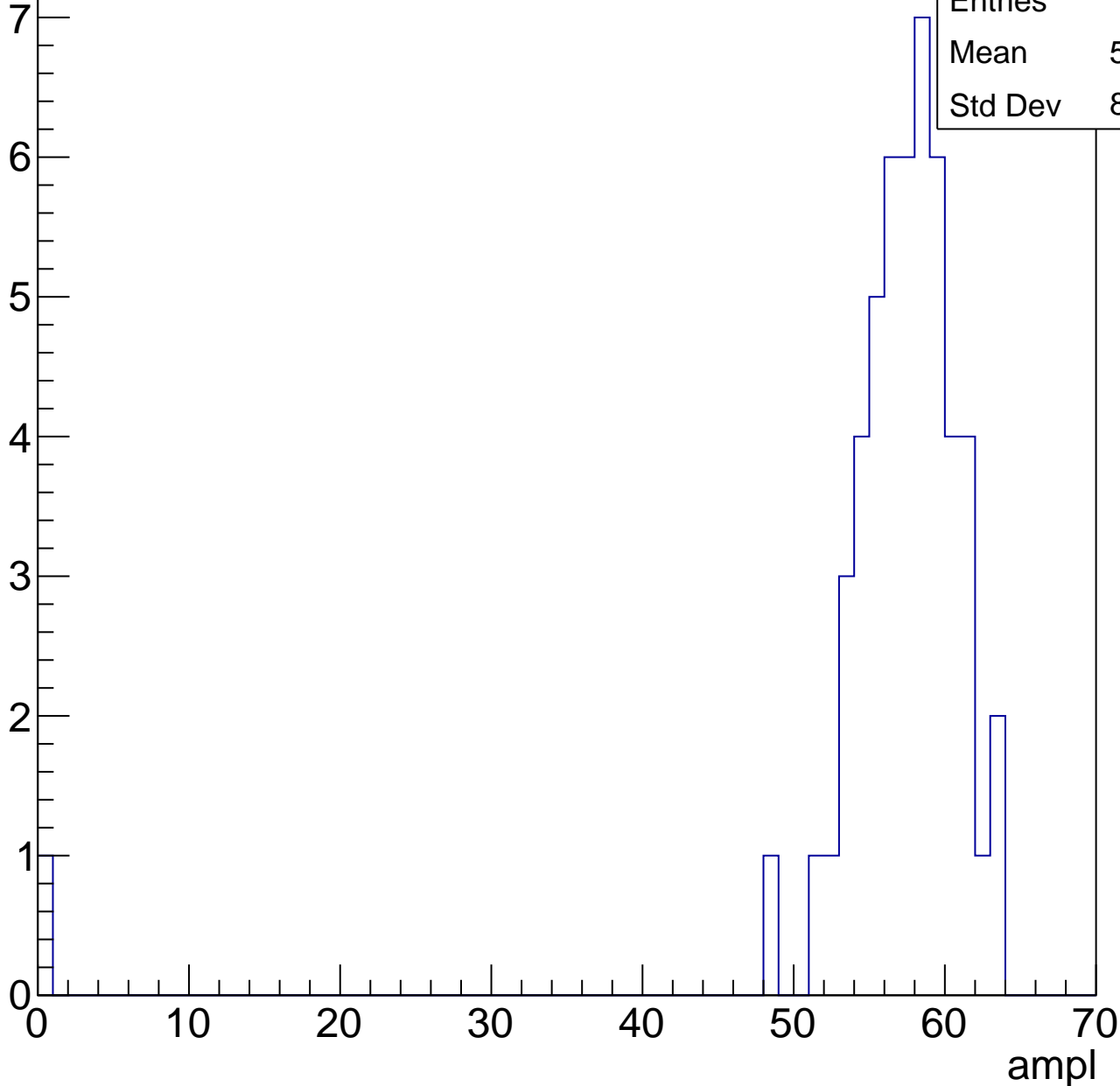


# B1L101S, U22-ch31, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	52
Mean	55.98
Std Dev	8.407

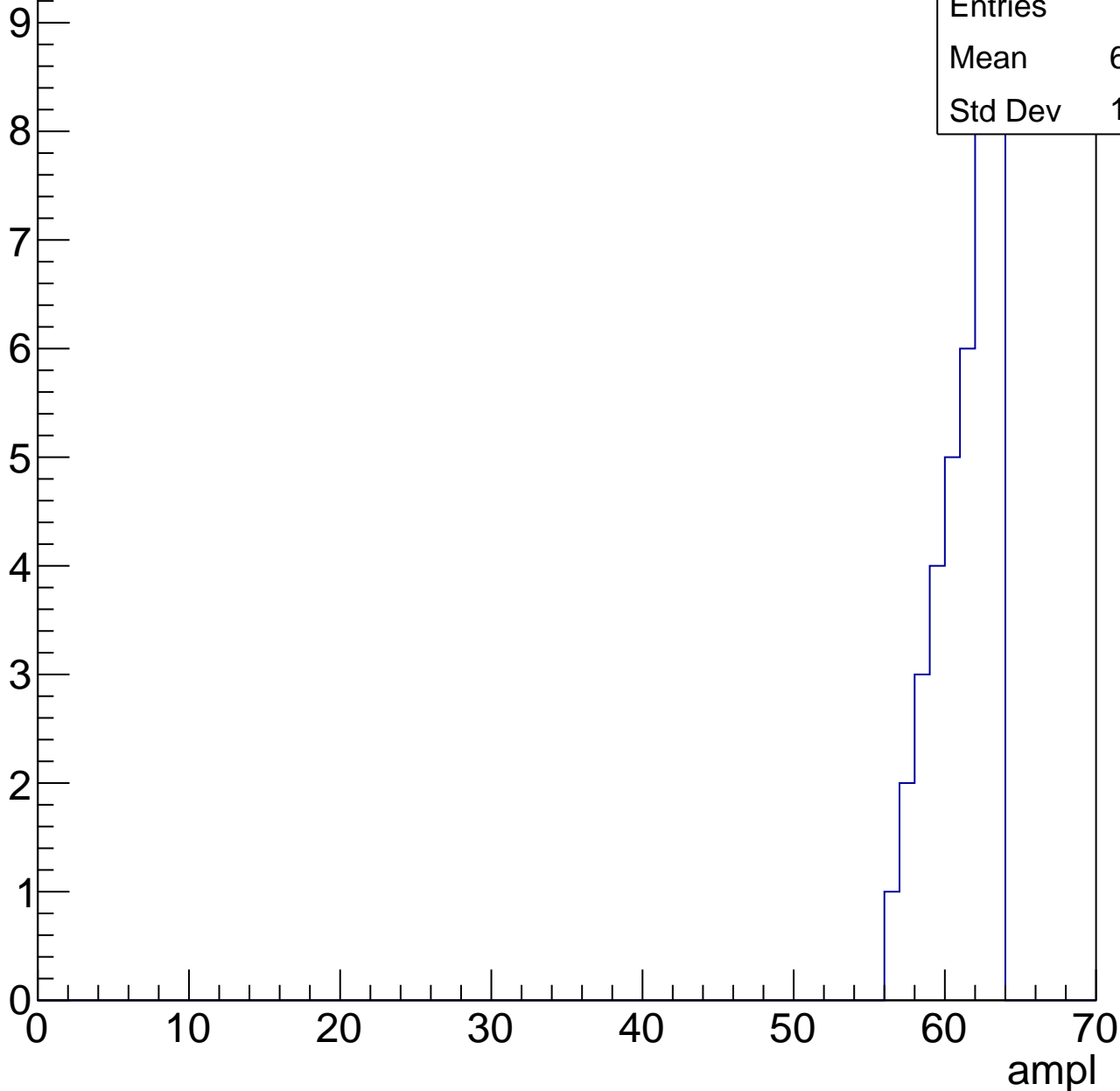


# B1L101S, U22-ch31, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	38
Mean	60.74
Std Dev	1.942



# B1L101S, U22-ch31, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

1

0.8

0.6

0.4

0.2

0

0

10

20

30

40

50

60

70

ampl

Entries

1

Mean

60

Std Dev

0



# B1L101S, U22-ch31, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U22-ch32, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	74
Mean	28.7
Std Dev	5.007

**Gaus mean : 30.0030**

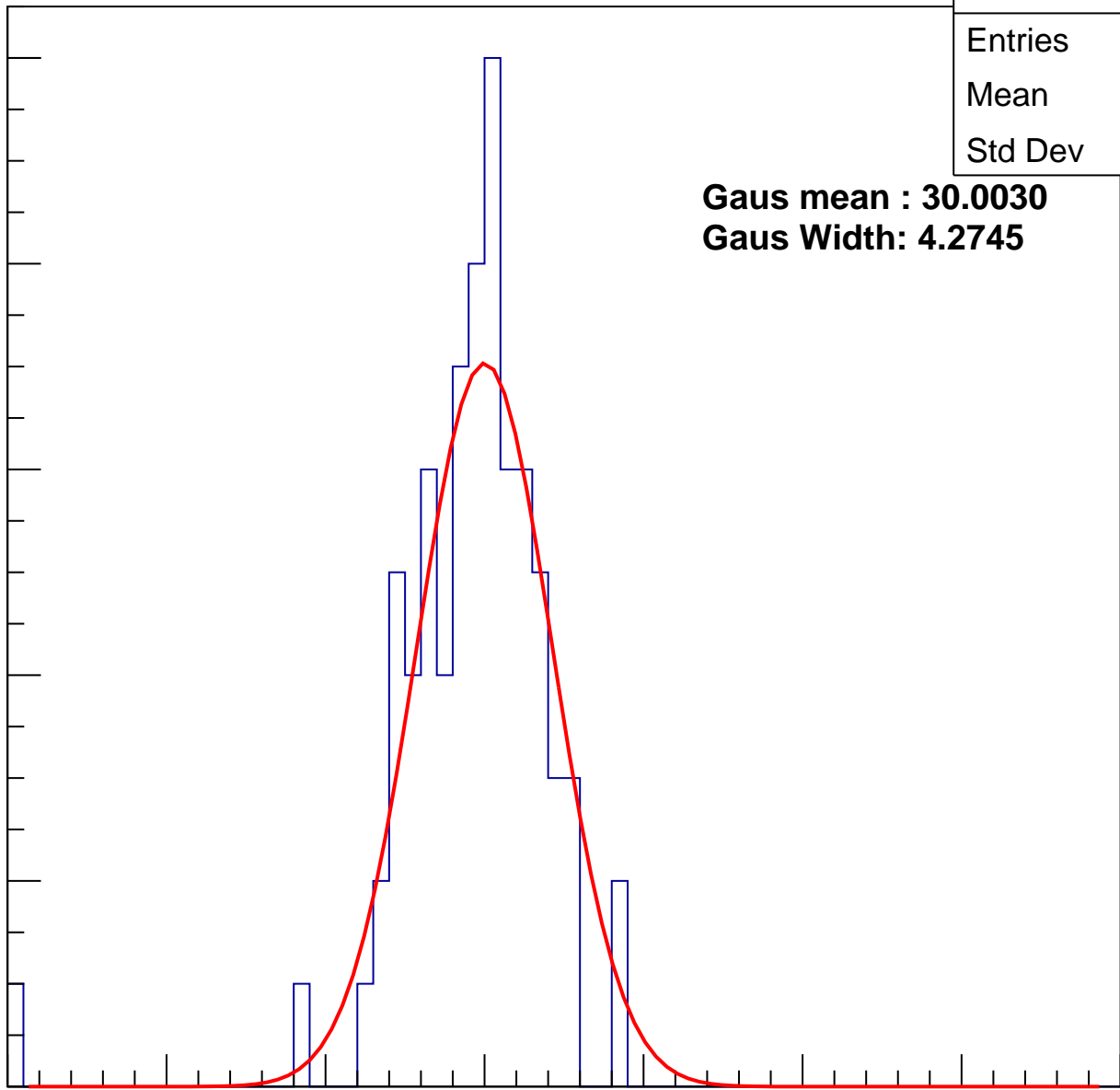
**Gaus Width: 4.2745**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U22-ch32, adc1

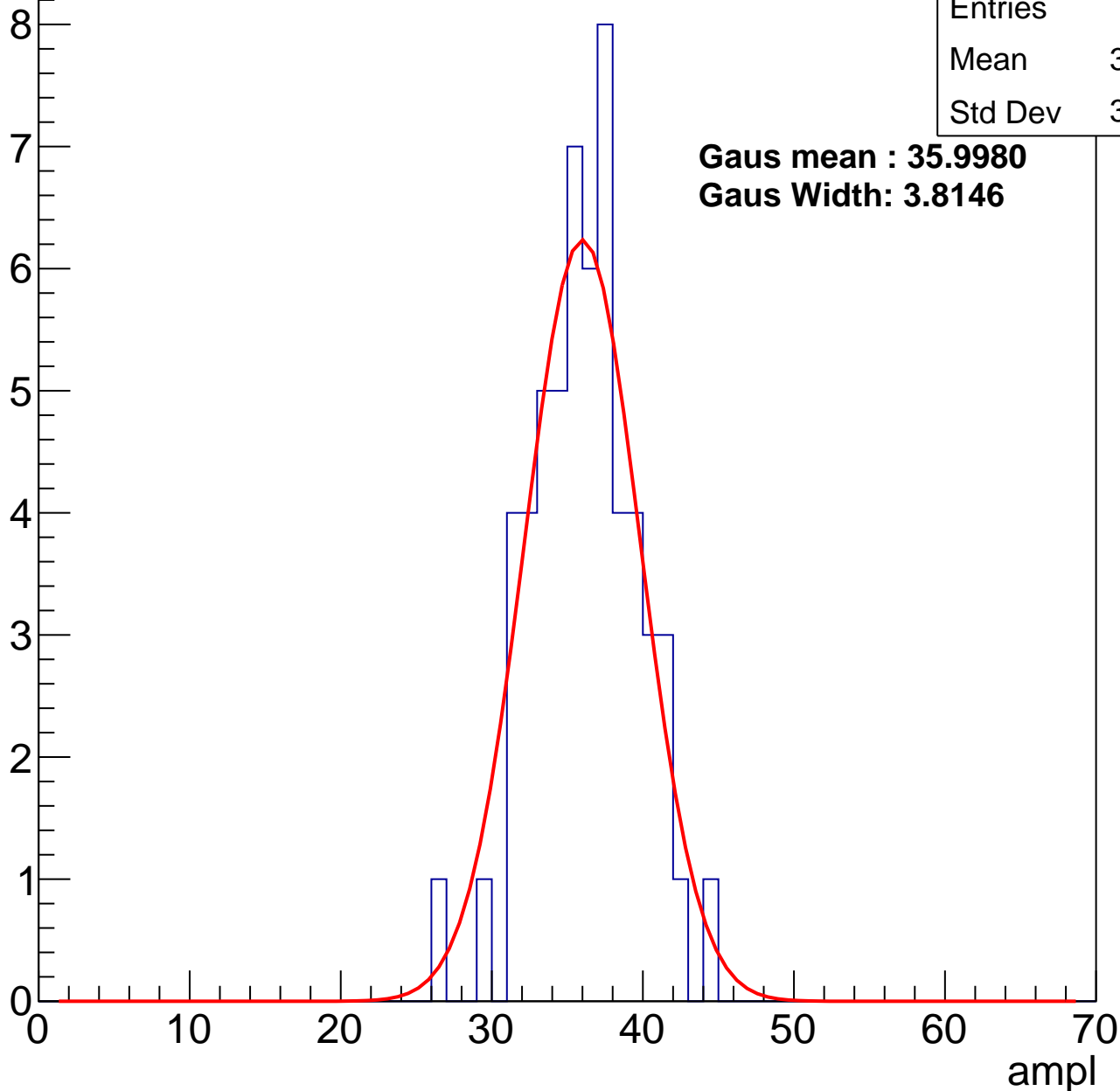
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	57
Mean	35.72
Std Dev	3.412

**Gaus mean : 35.9980**

**Gaus Width: 3.8146**



# B1L101S, U22-ch32, adc2

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	75
Mean	42.32
Std Dev	3.827

**Gaus mean : 42.5319**

**Gaus Width: 3.9769**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

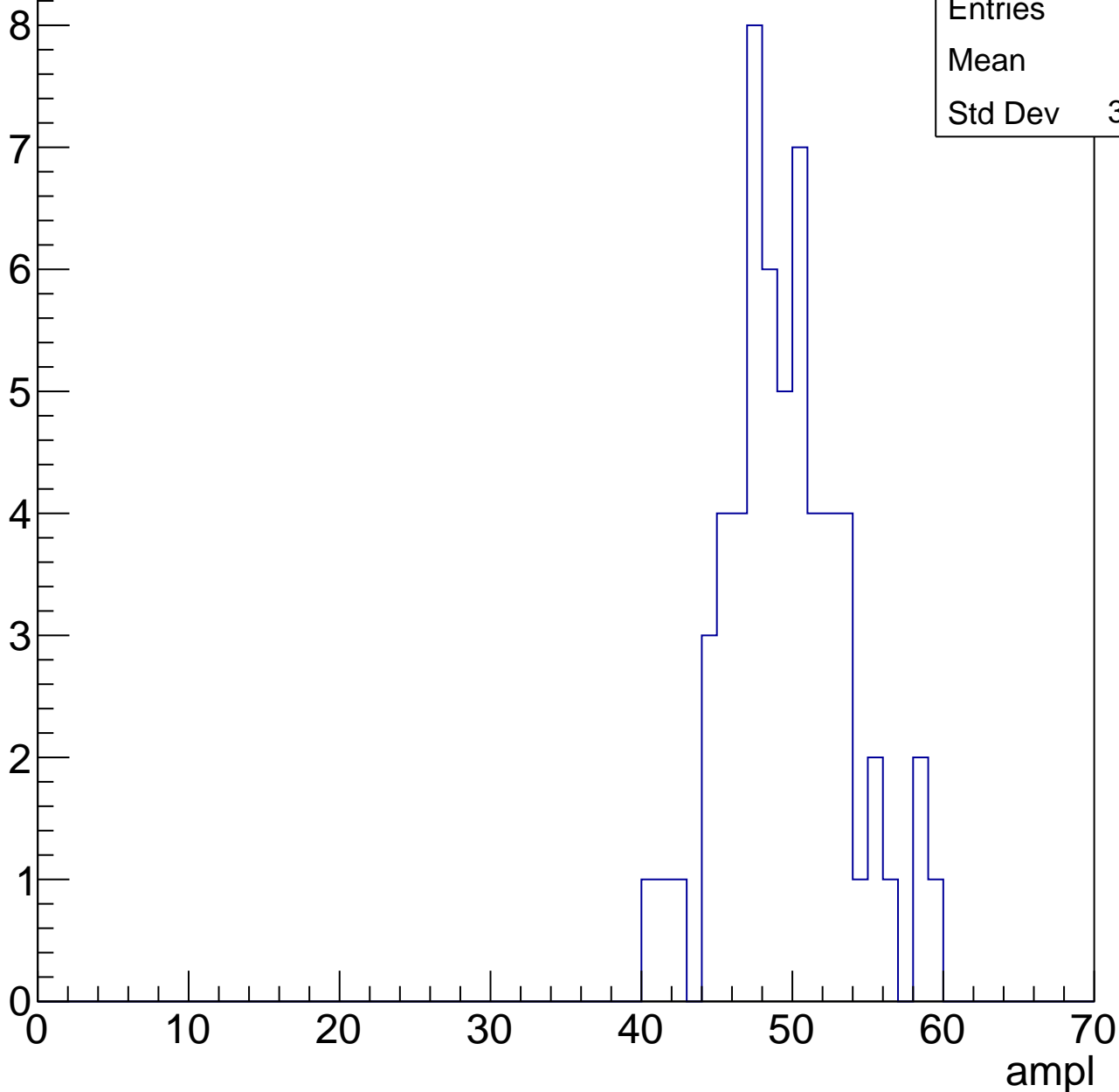


# B1L101S, U22-ch32, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

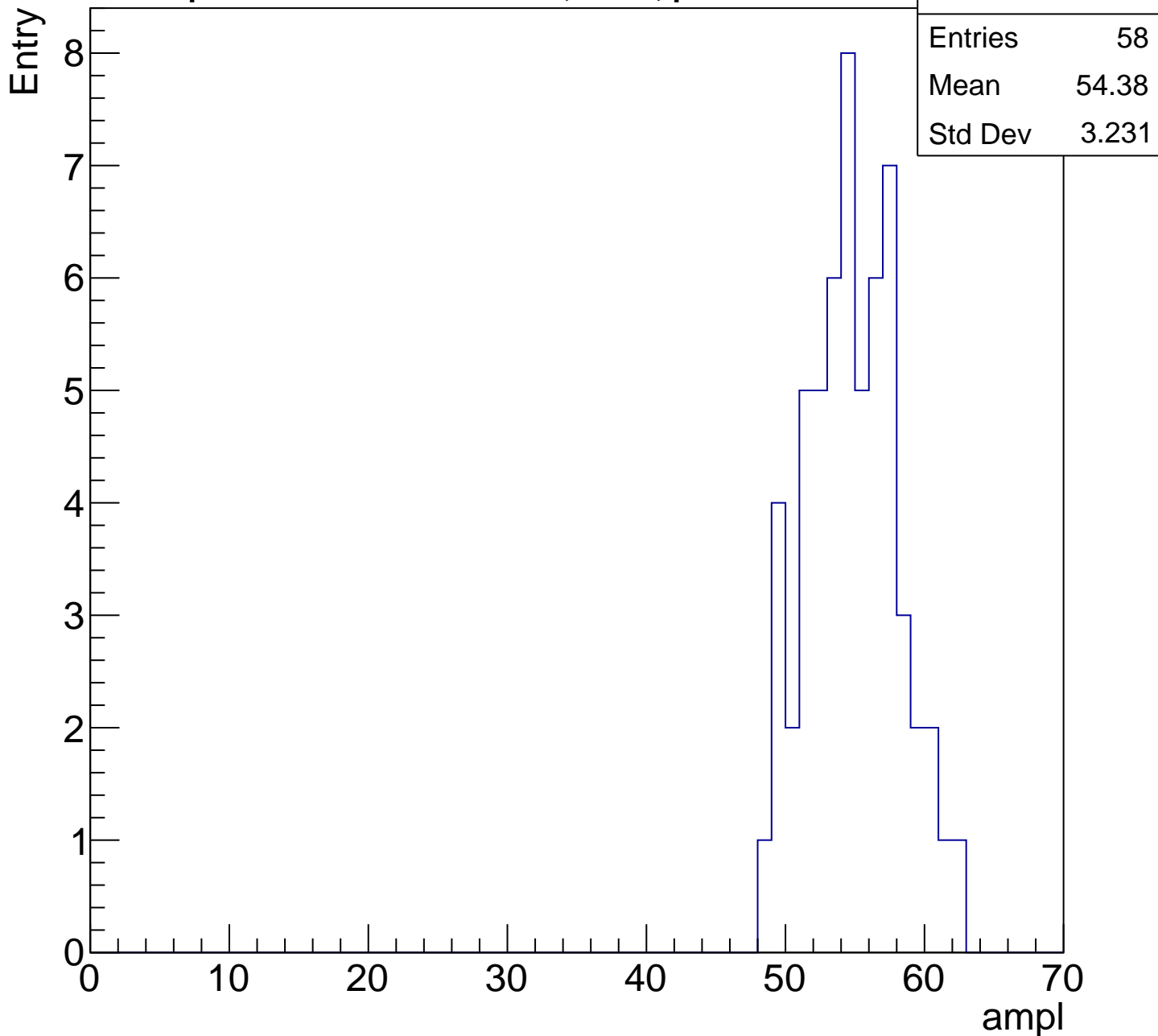
Entry

Entries	59
Mean	49.1
Std Dev	3.986



# B1L101S, U22-ch32, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U22-ch32, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	52
Mean	58.6
Std Dev	8.572

ampl

0 10 20 30 40 50 60 70

1

2

3

4

5

6

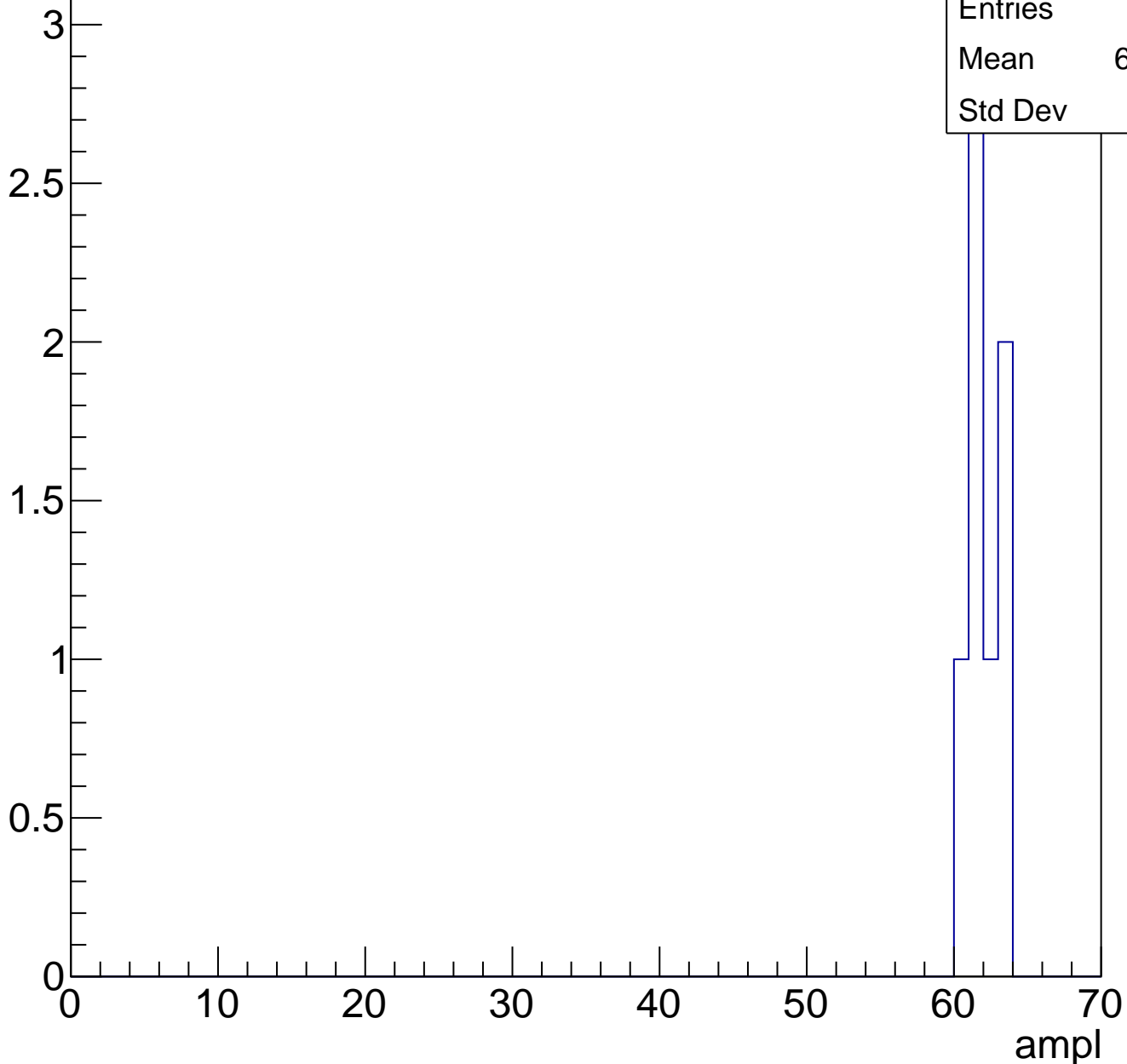
7

8

# B1L101S, U22-ch32, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	7
Mean	61.57
Std Dev	1.05



# B1L101S, U22-ch32, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U22-ch33, adc0

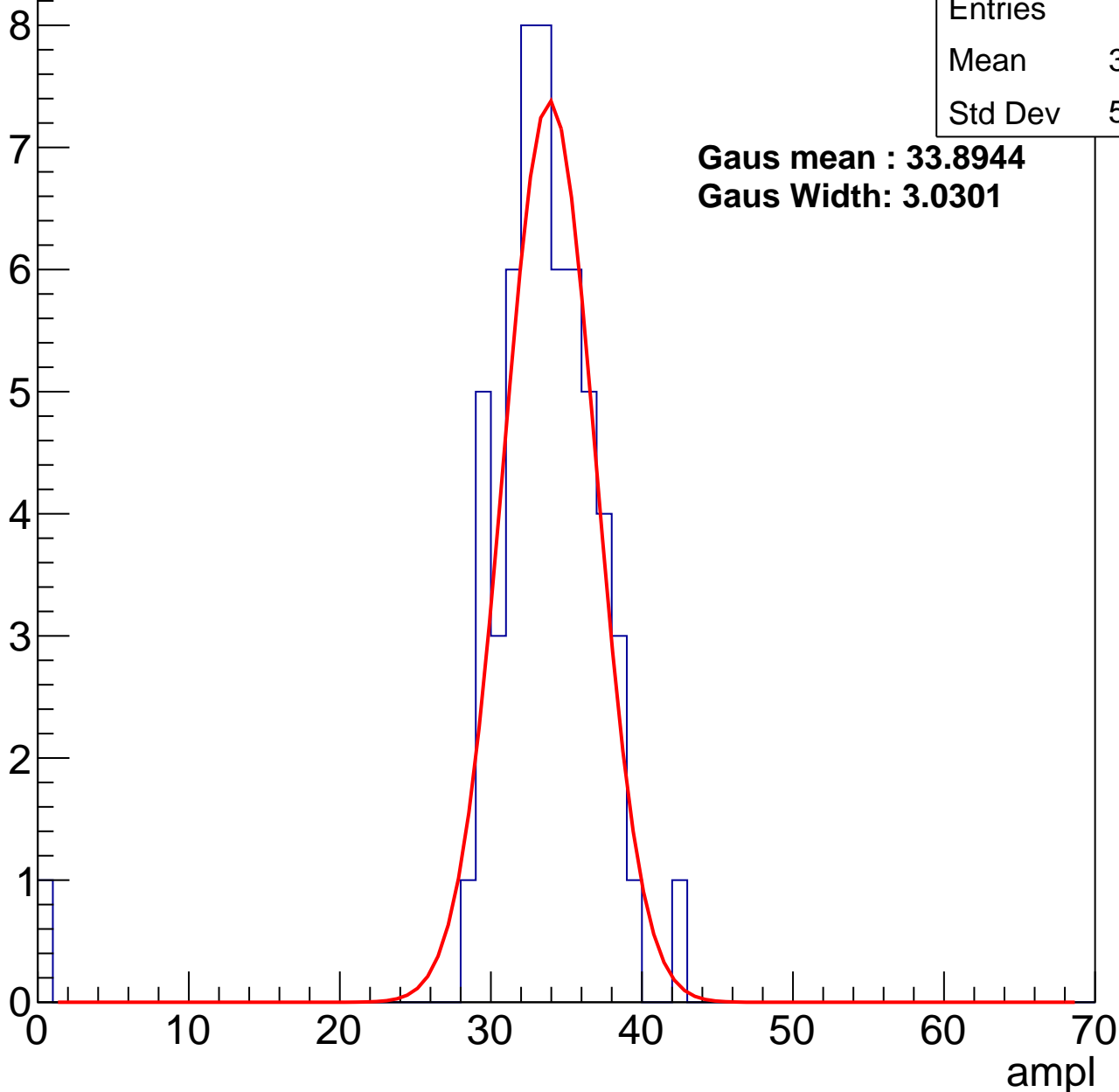
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	58
Mean	32.86
Std Dev	5.224

**Gaus mean : 33.8944**

**Gaus Width: 3.0301**



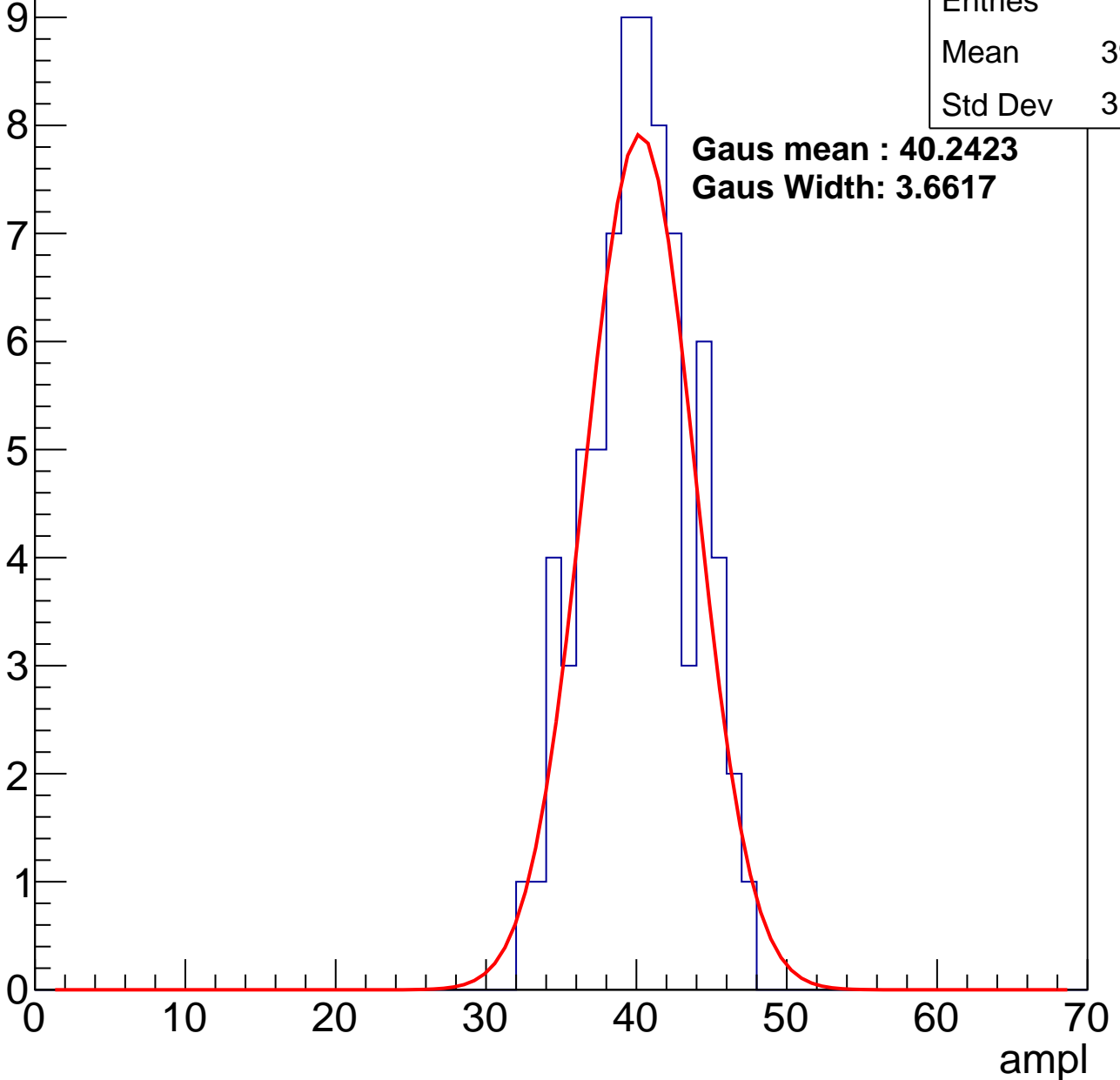
# B1L101S, U22-ch33, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	75
Mean	39.76
Std Dev	3.405

**Gaus mean : 40.2423**  
**Gaus Width: 3.6617**



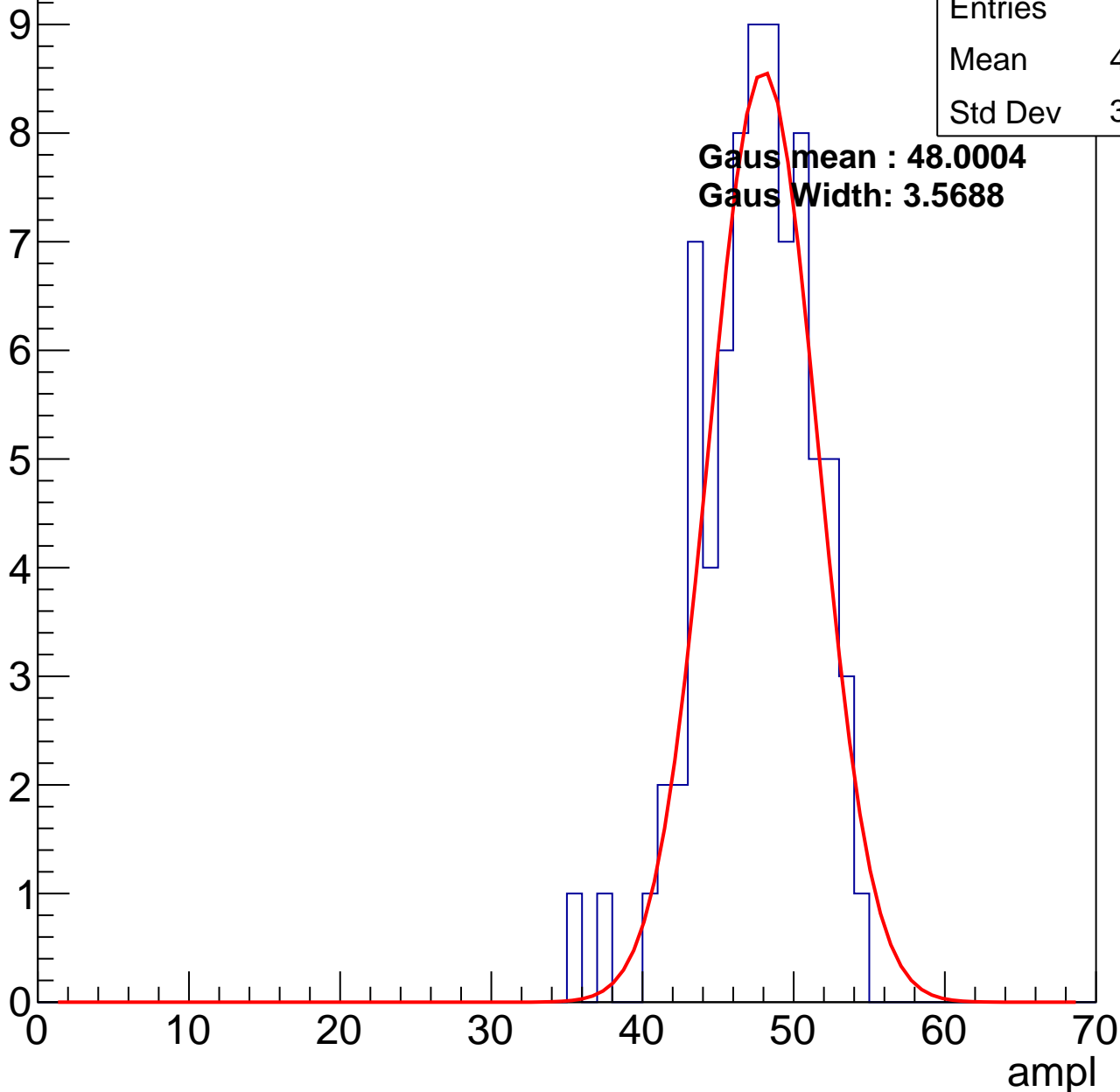
# B1L101S, U22-ch33, adc2

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	79
Mean	47.08
Std Dev	3.673

**Gaus mean : 48.0004**  
**Gaus Width: 3.5688**

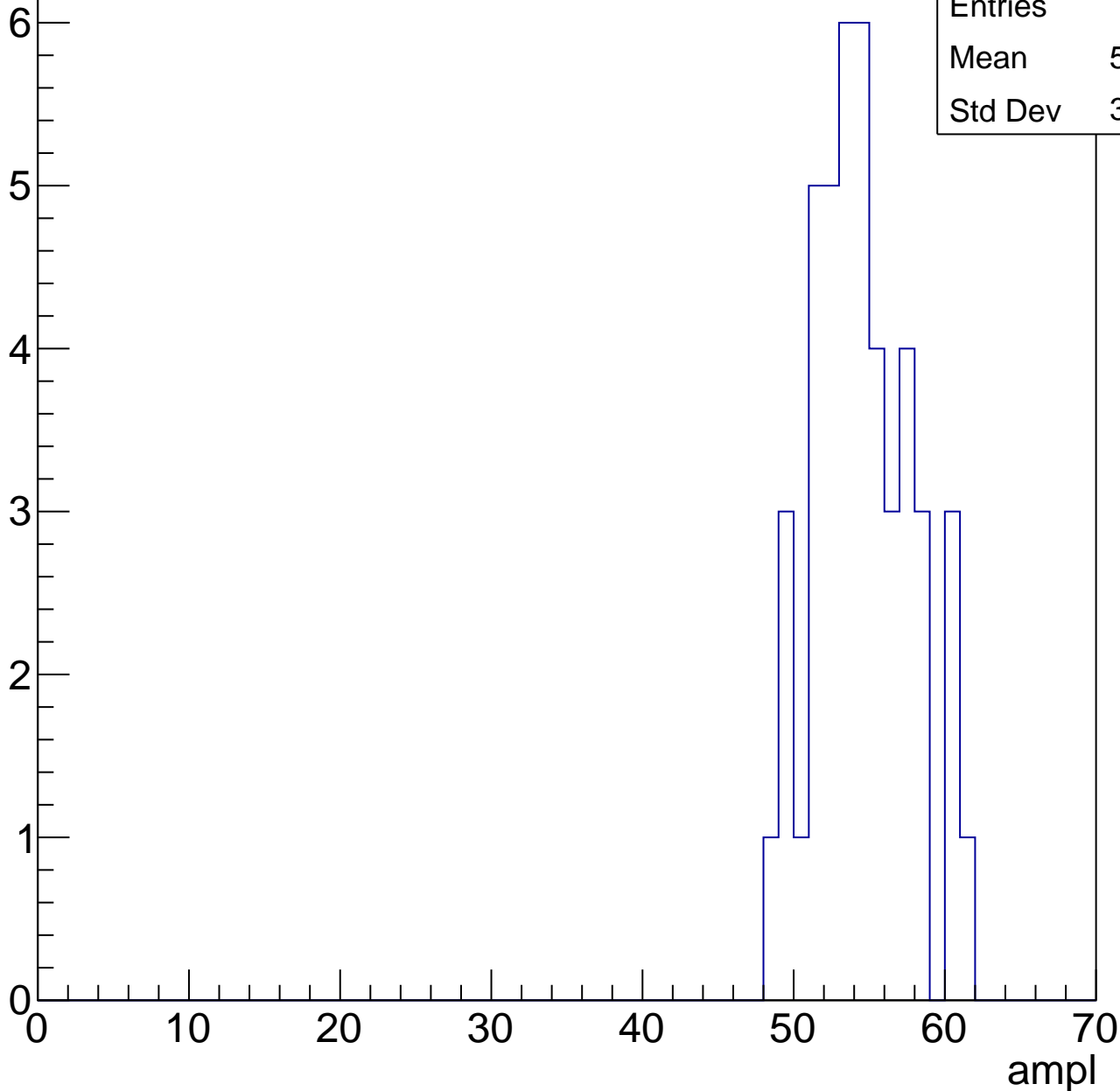


# B1L101S, U22-ch33, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	45
Mean	54.07
Std Dev	3.179



# B1L101S, U22-ch33, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	64
Mean	58.34
Std Dev	2.785

Entry

10

8

6

4

2

0

0

10

20

30

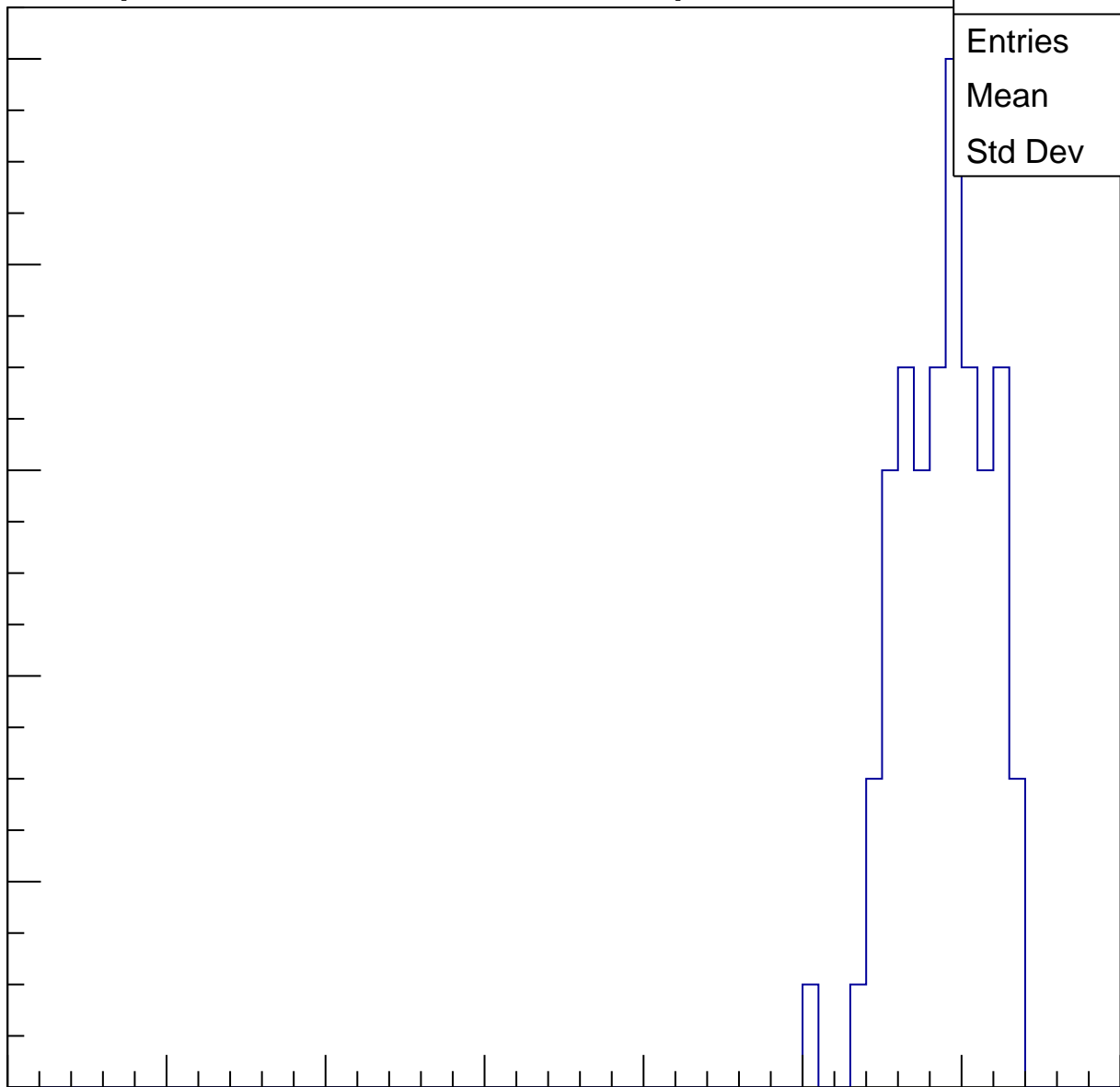
40

50

60

70

ampl

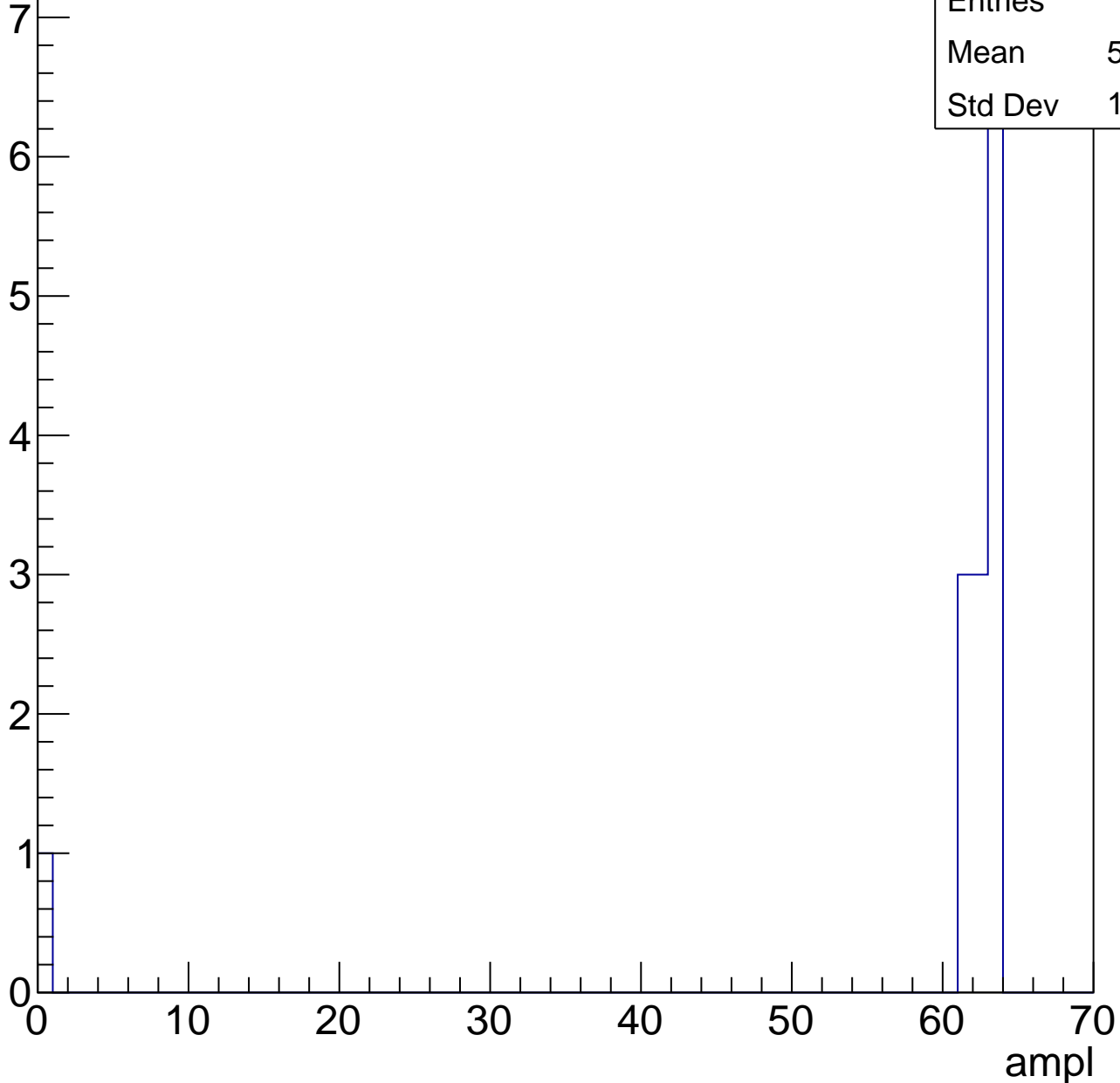


# B1L101S, U22-ch33, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	14
Mean	57.86
Std Dev	16.07



# B1L101S, U22-ch33, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



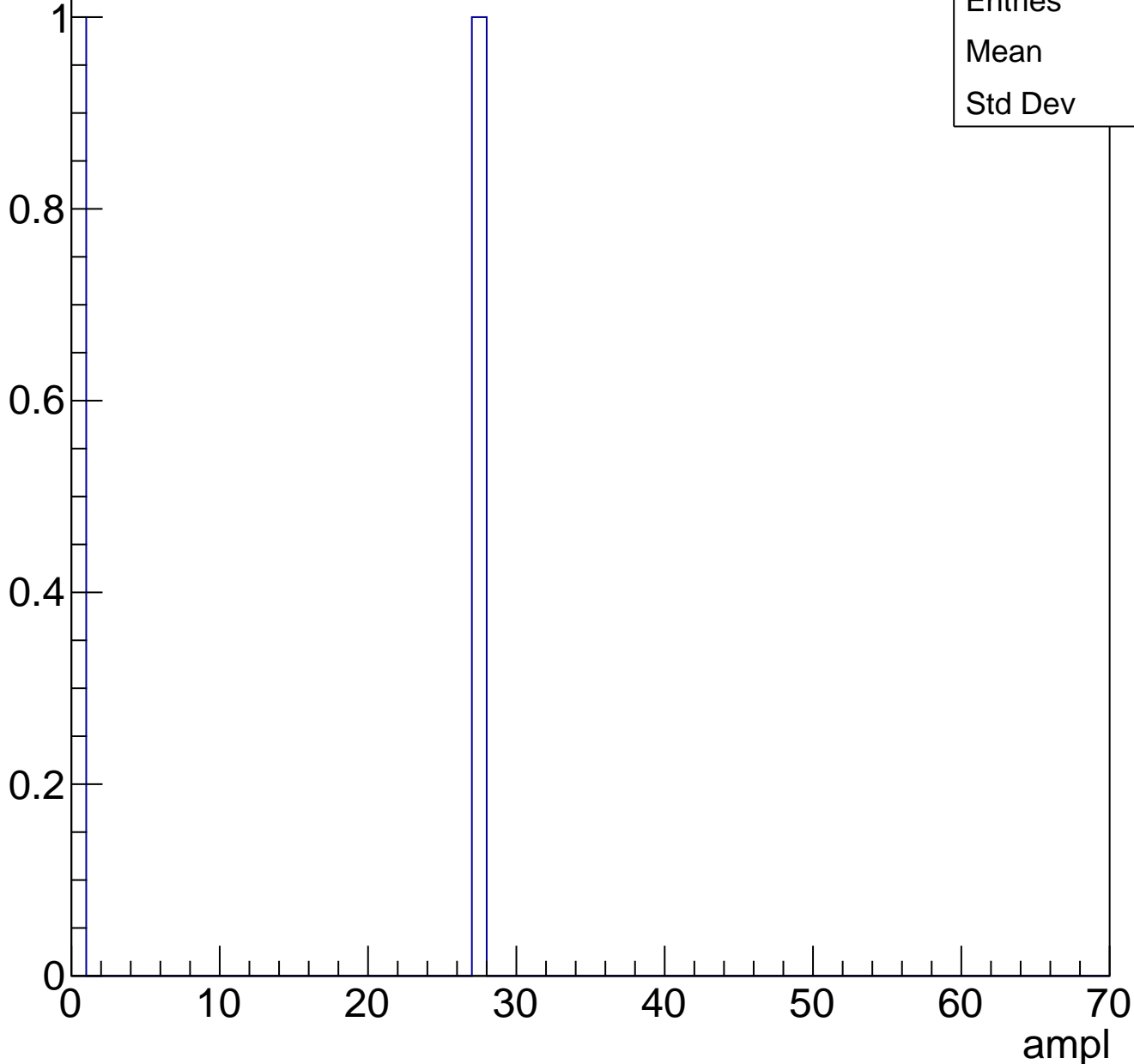
Entries	0
Mean	0
Std Dev	0



# B1L101S, U22-ch33, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U22-ch34, adc0

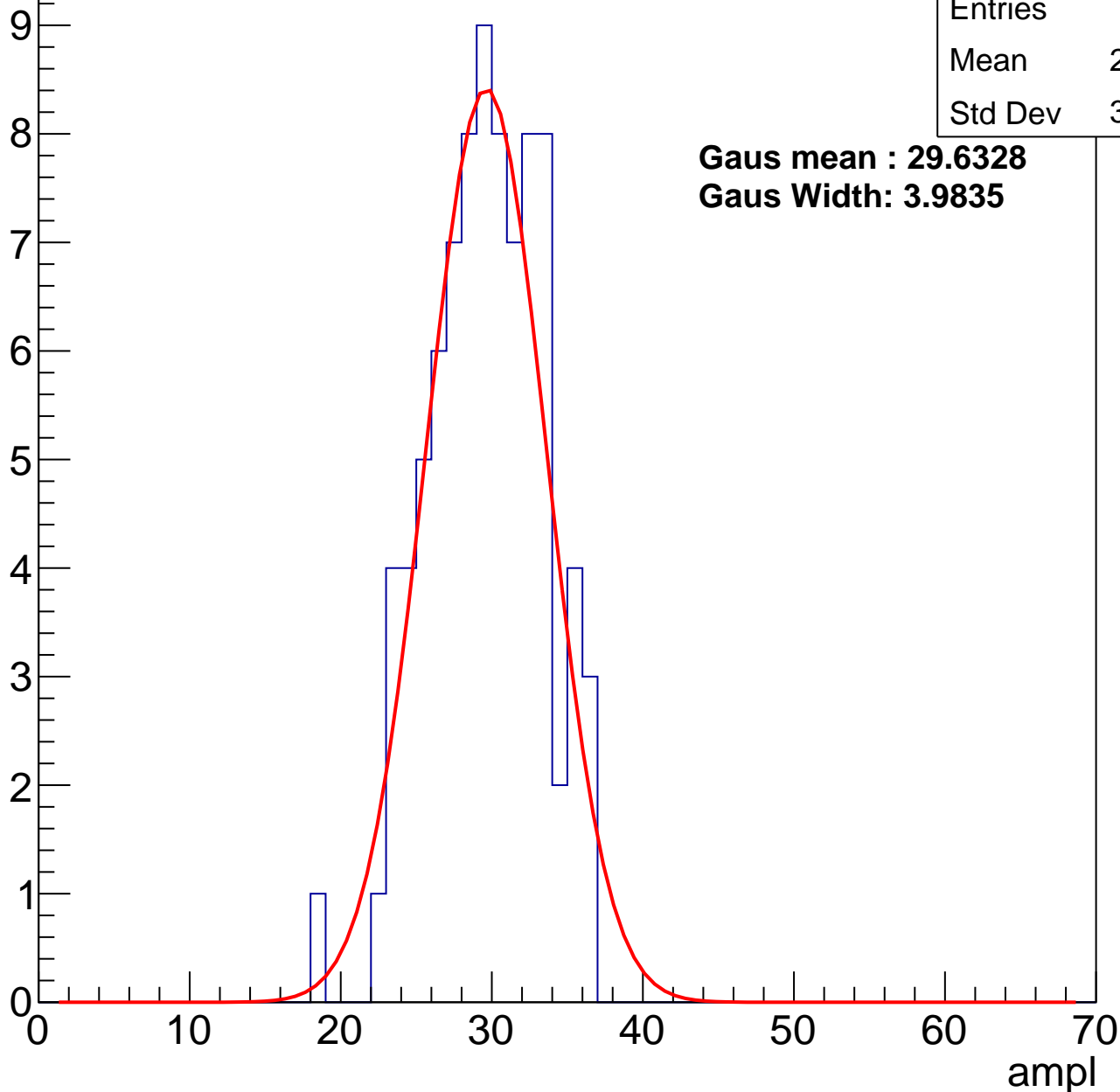
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	85
Mean	29.13
Std Dev	3.694

**Gaus mean : 29.6328**

**Gaus Width: 3.9835**



# B1L101S, U22-ch34, adc1

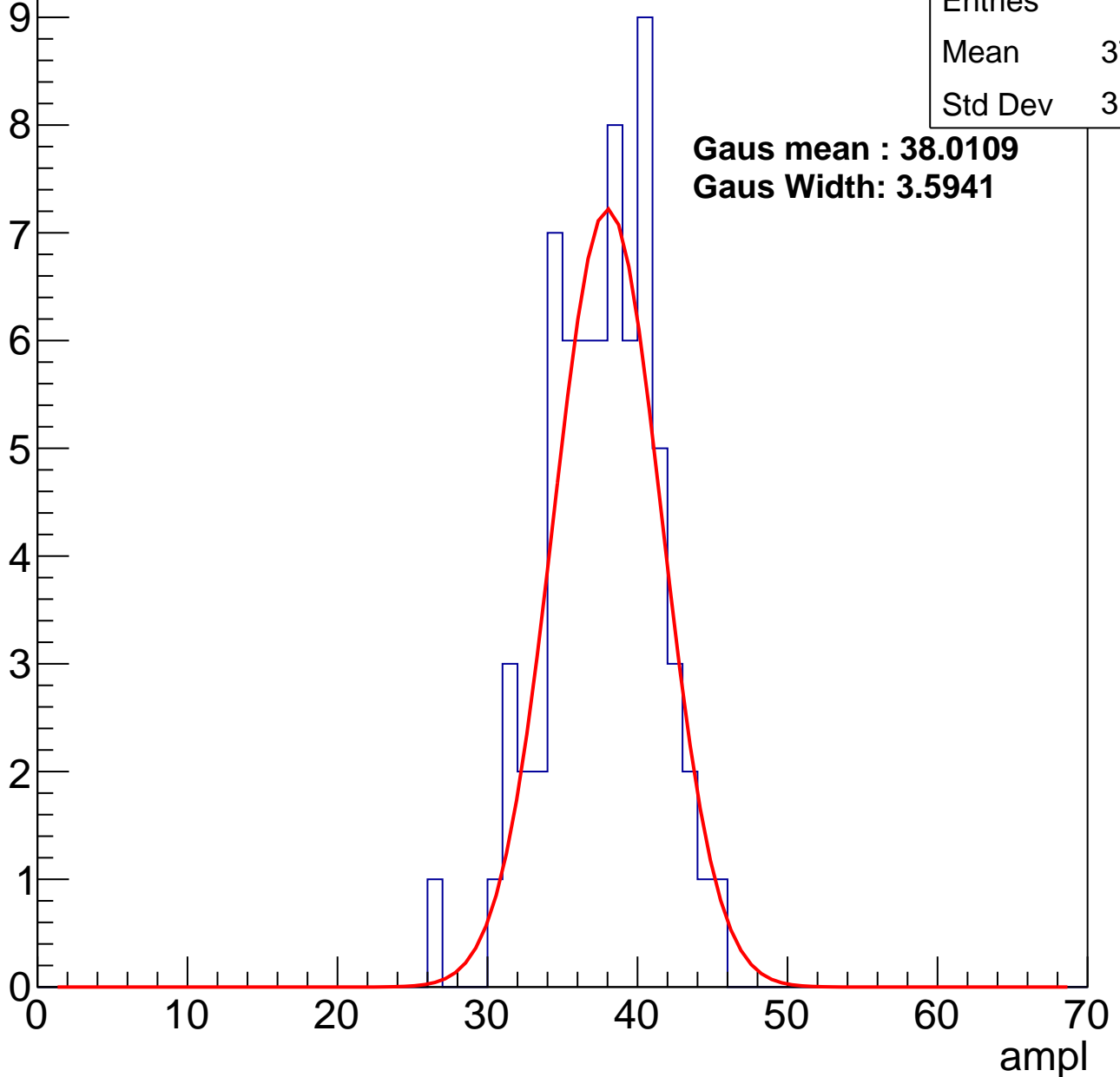
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	37.23
Std Dev	3.616

**Gaus mean : 38.0109**

**Gaus Width: 3.5941**



# B1L101S, U22-ch34, adc2

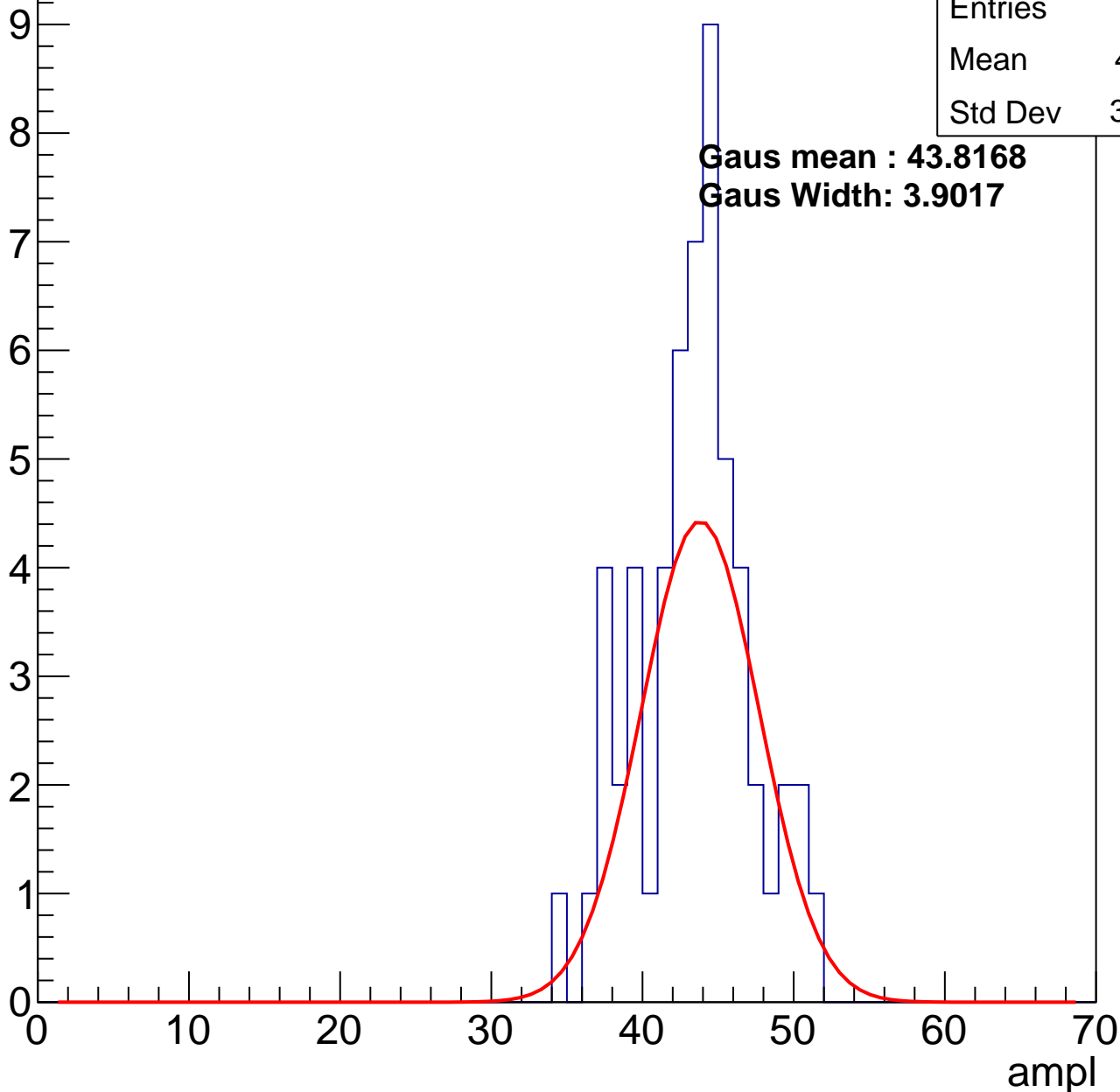
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	56
Mean	42.91
Std Dev	3.719

**Gaus mean : 43.8168**

**Gaus Width: 3.9017**

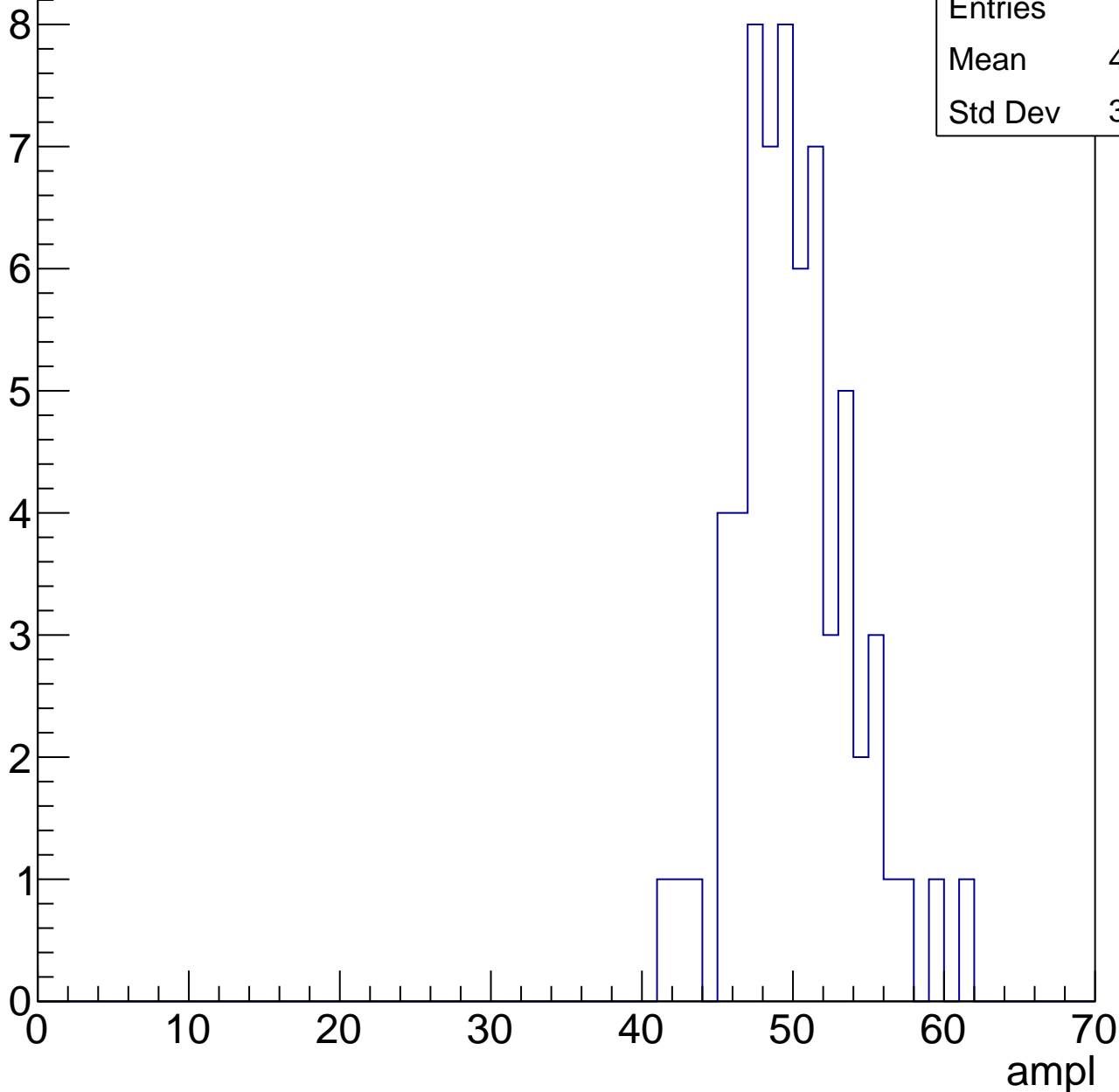


# B1L101S, U22-ch34, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

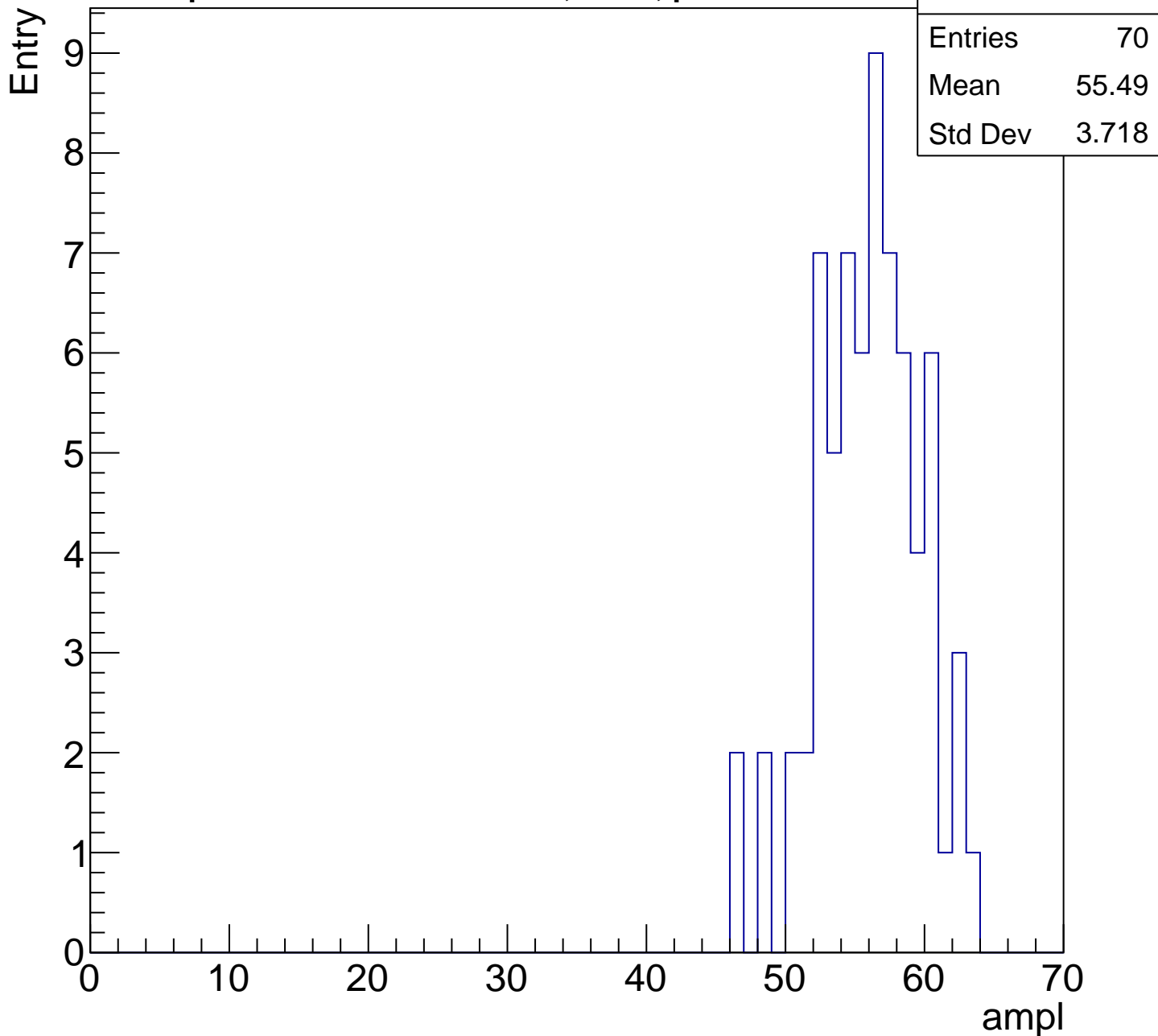
Entry

Entries	64
Mean	49.66
Std Dev	3.784



# B1L101S, U22-ch34, adc4

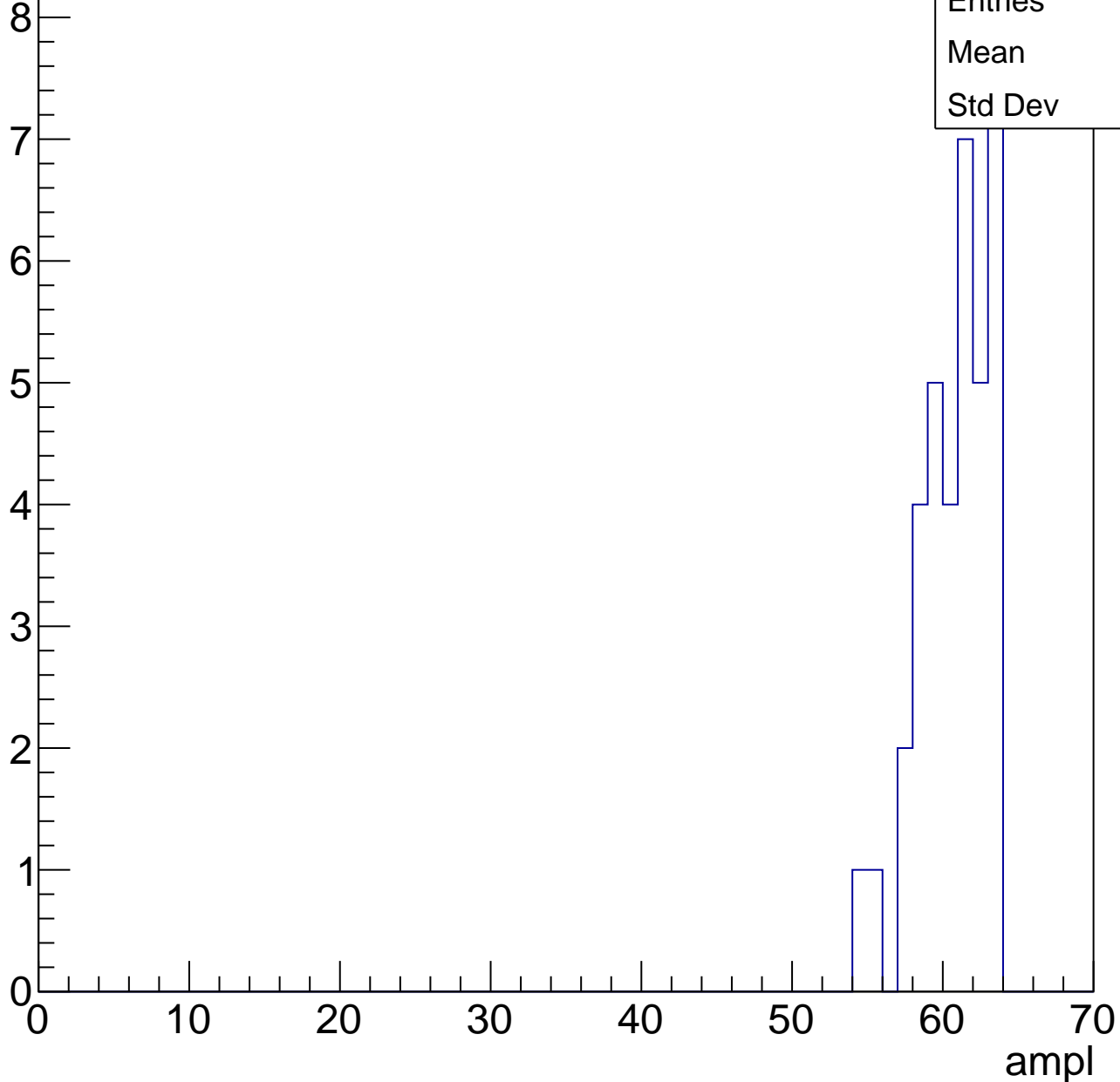
calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U22-ch34, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U22-ch34, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U22-ch34, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U22-ch35, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	69
Mean	31.58
Std Dev	4.988

**Gaus mean : 32.1746**

**Gaus Width: 3.4412**

Entry

10  
8  
6  
4  
2  
0

ampl

0

10

20

30

40

50

60

70

# B1L101S, U22-ch35, adc1

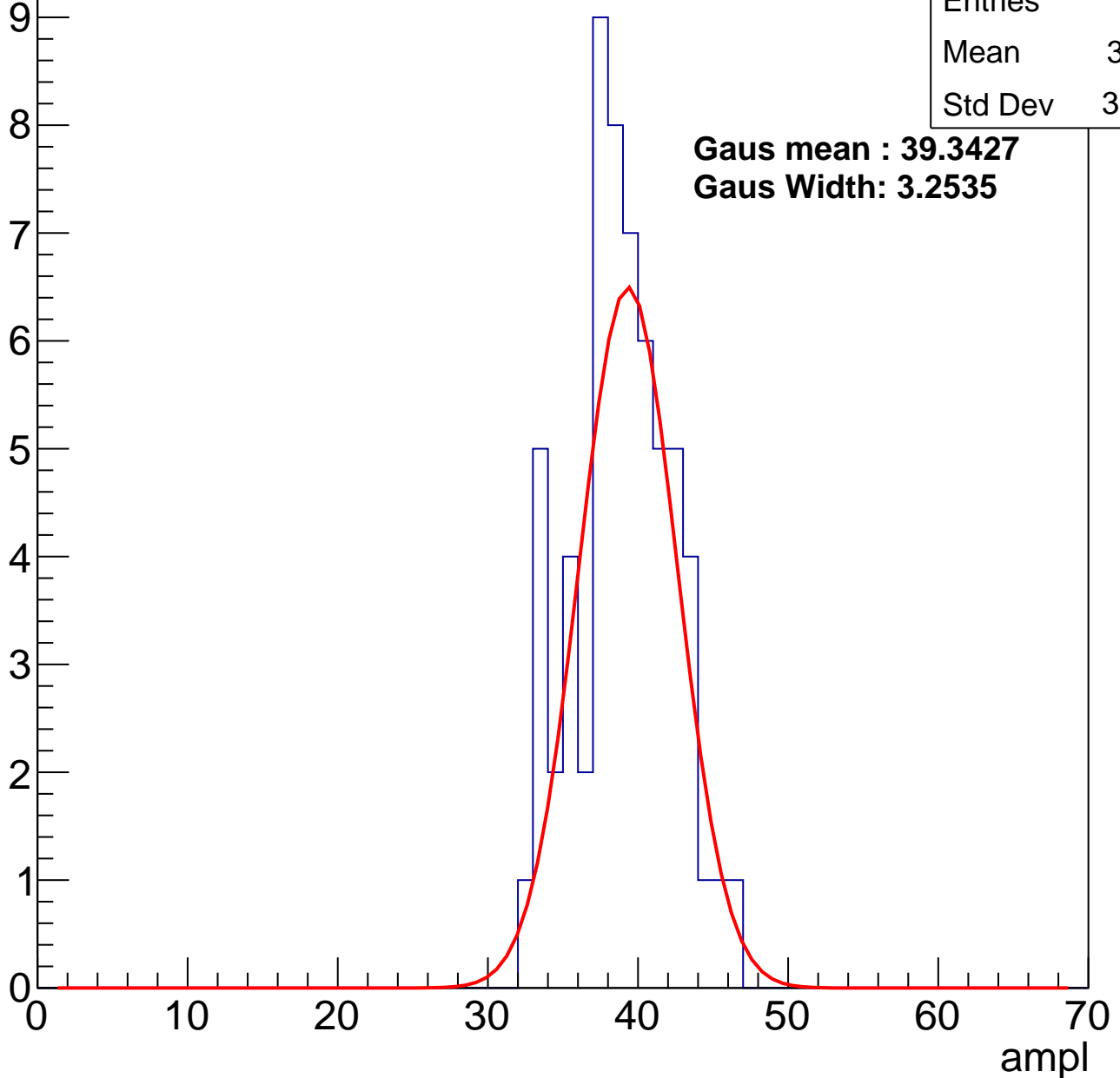
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	38.51
Std Dev	3.227

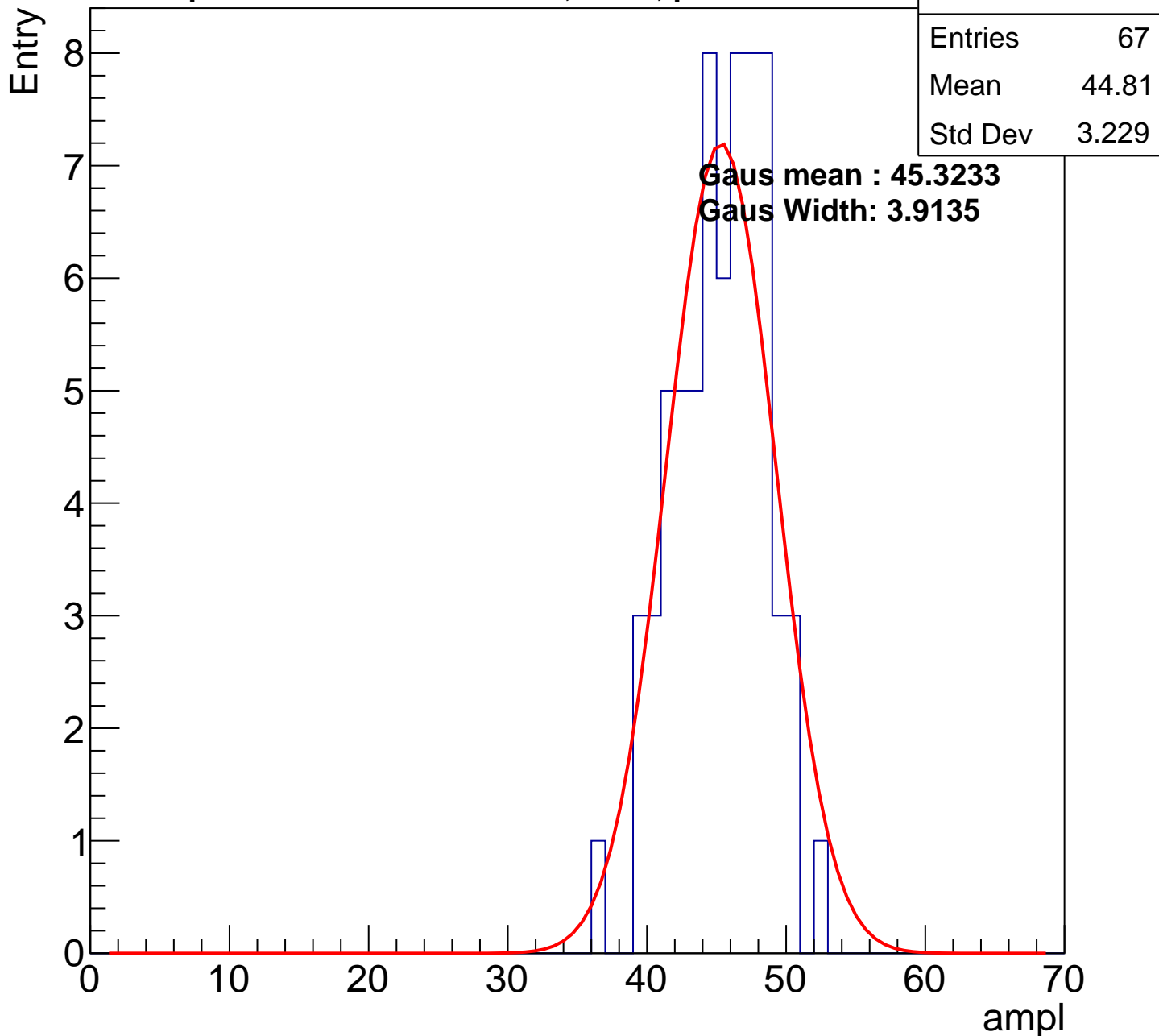
**Gaus mean : 39.3427**

**Gaus Width: 3.2535**



# B1L101S, U22-ch35, adc2

calib\_packv5\_042523\_0143.root, FC#0, port D2

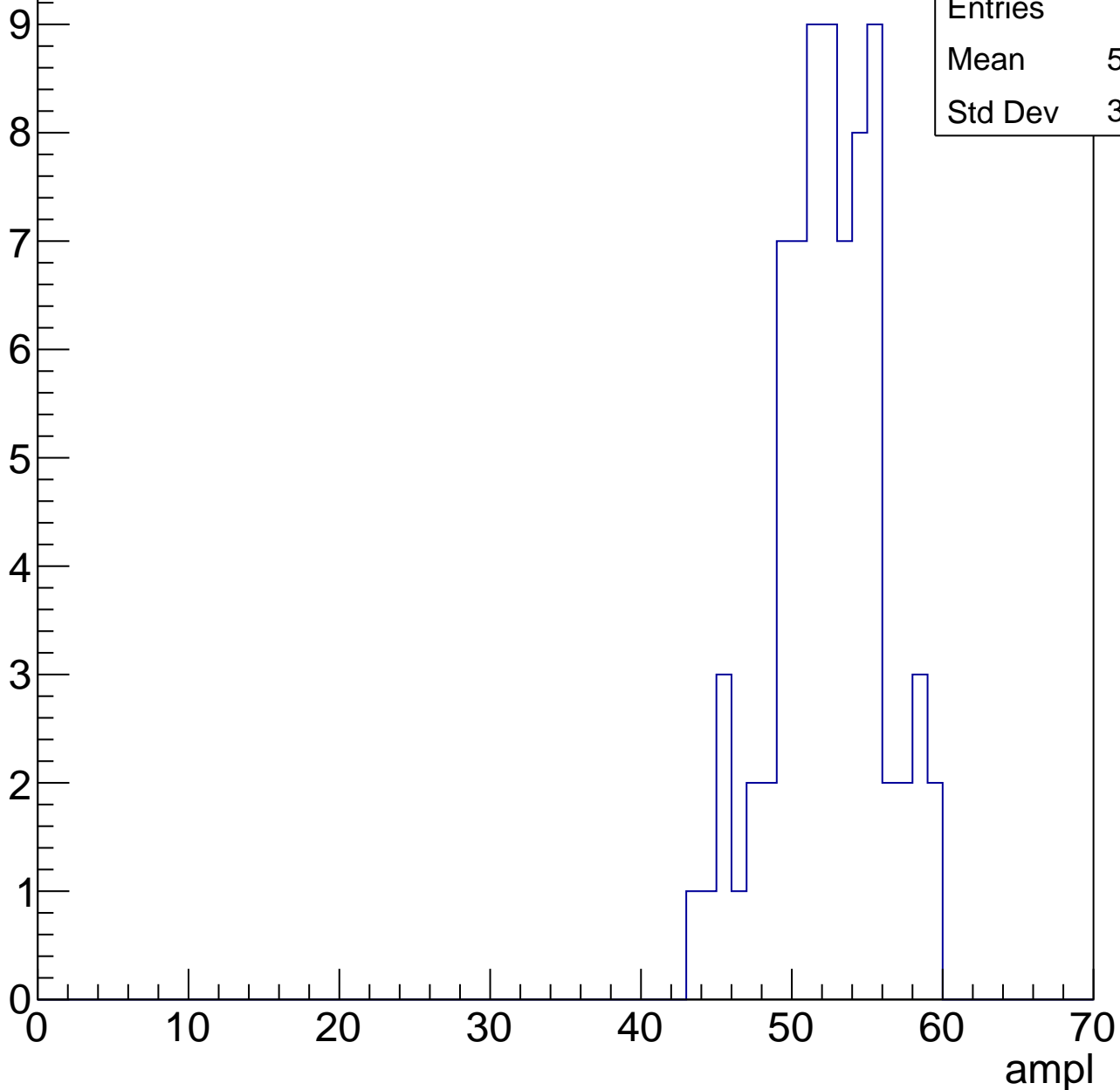


# B1L101S, U22-ch35, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	75
Mean	51.92
Std Dev	3.498

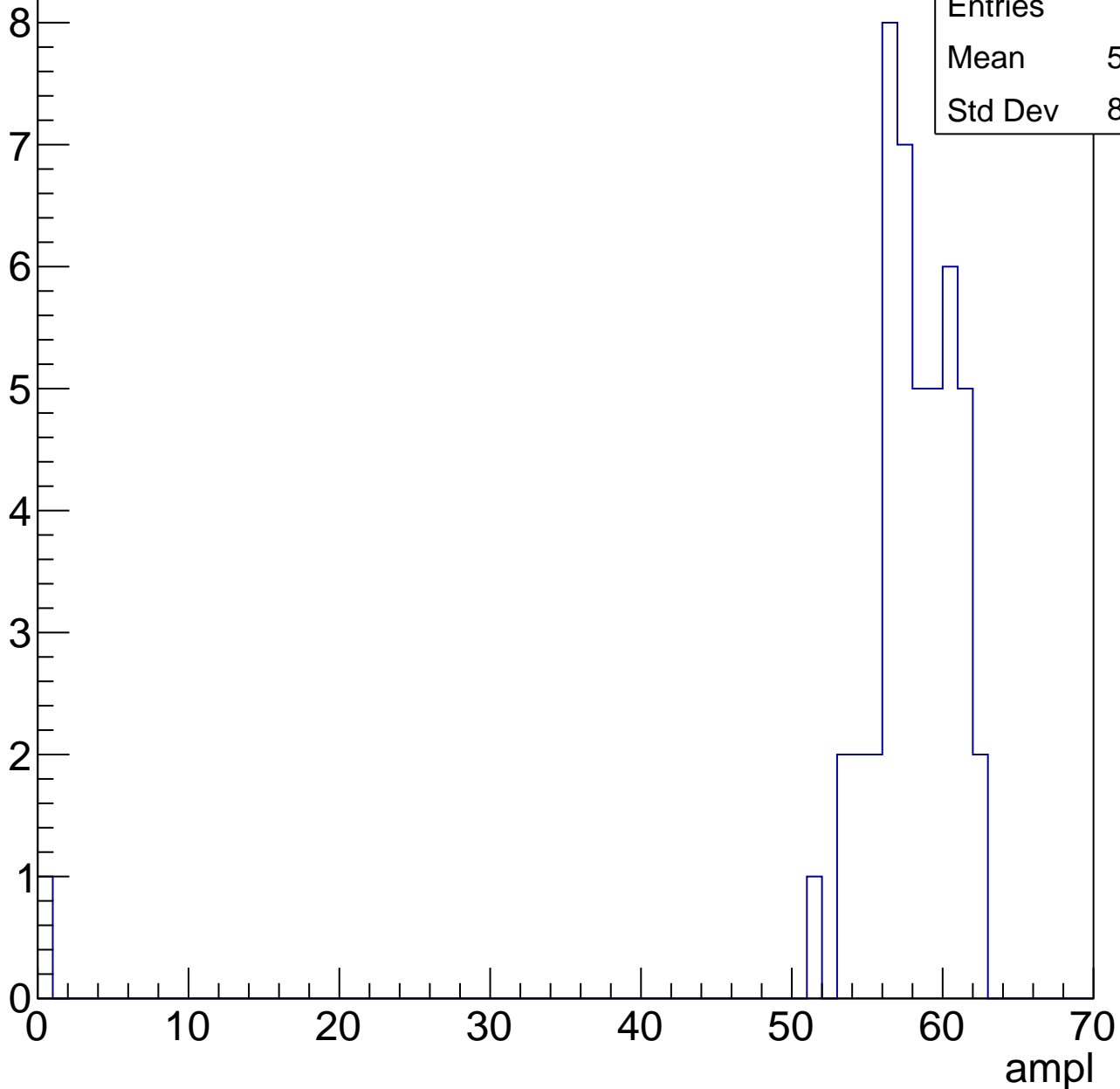


# B1L101S, U22-ch35, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	46
Mean	56.43
Std Dev	8.779

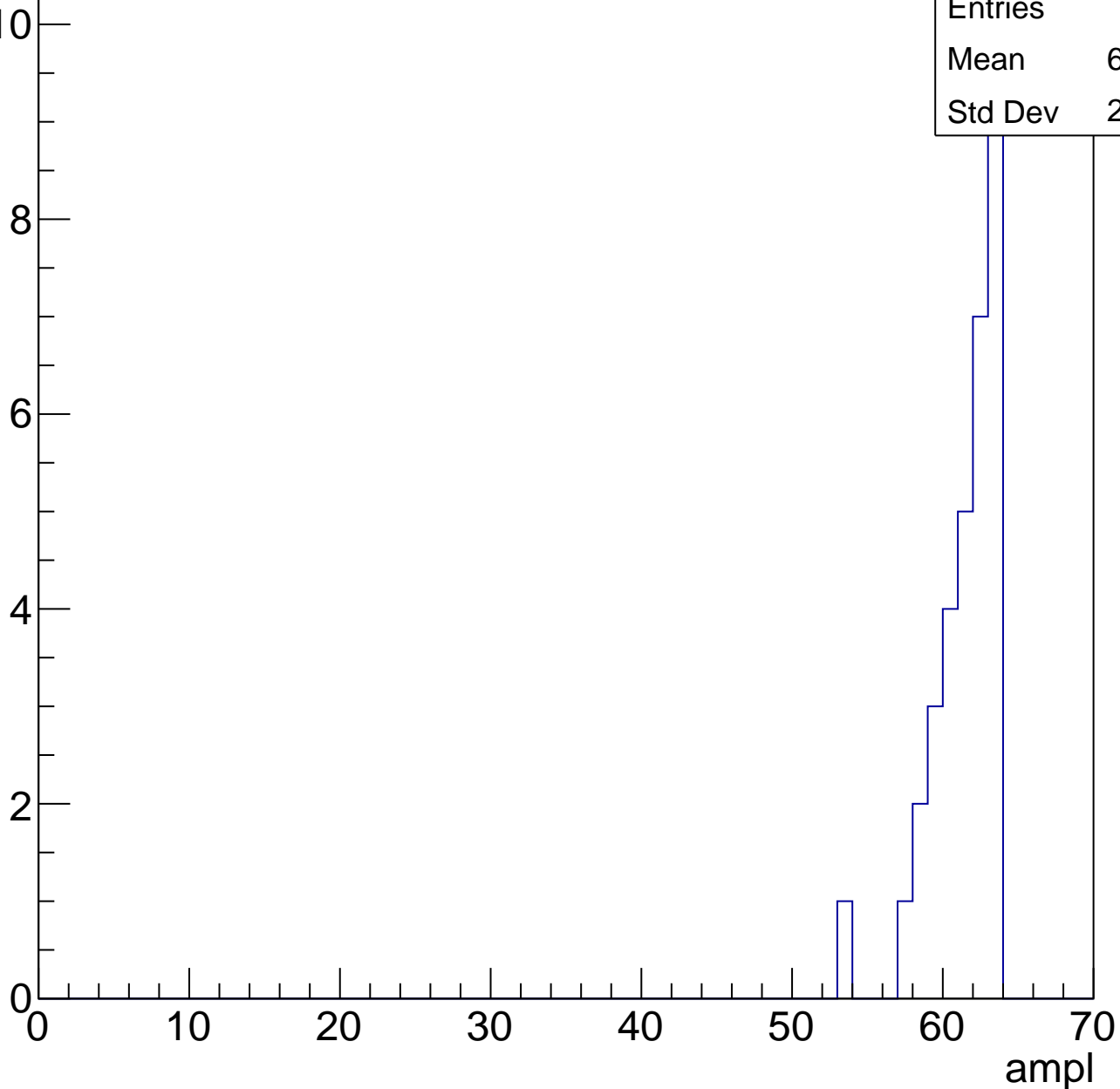


# B1L101S, U22-ch35, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	33
Mean	60.97
Std Dev	2.209



# B1L101S, U22-ch35, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U22-ch35, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U22-ch36, adc0

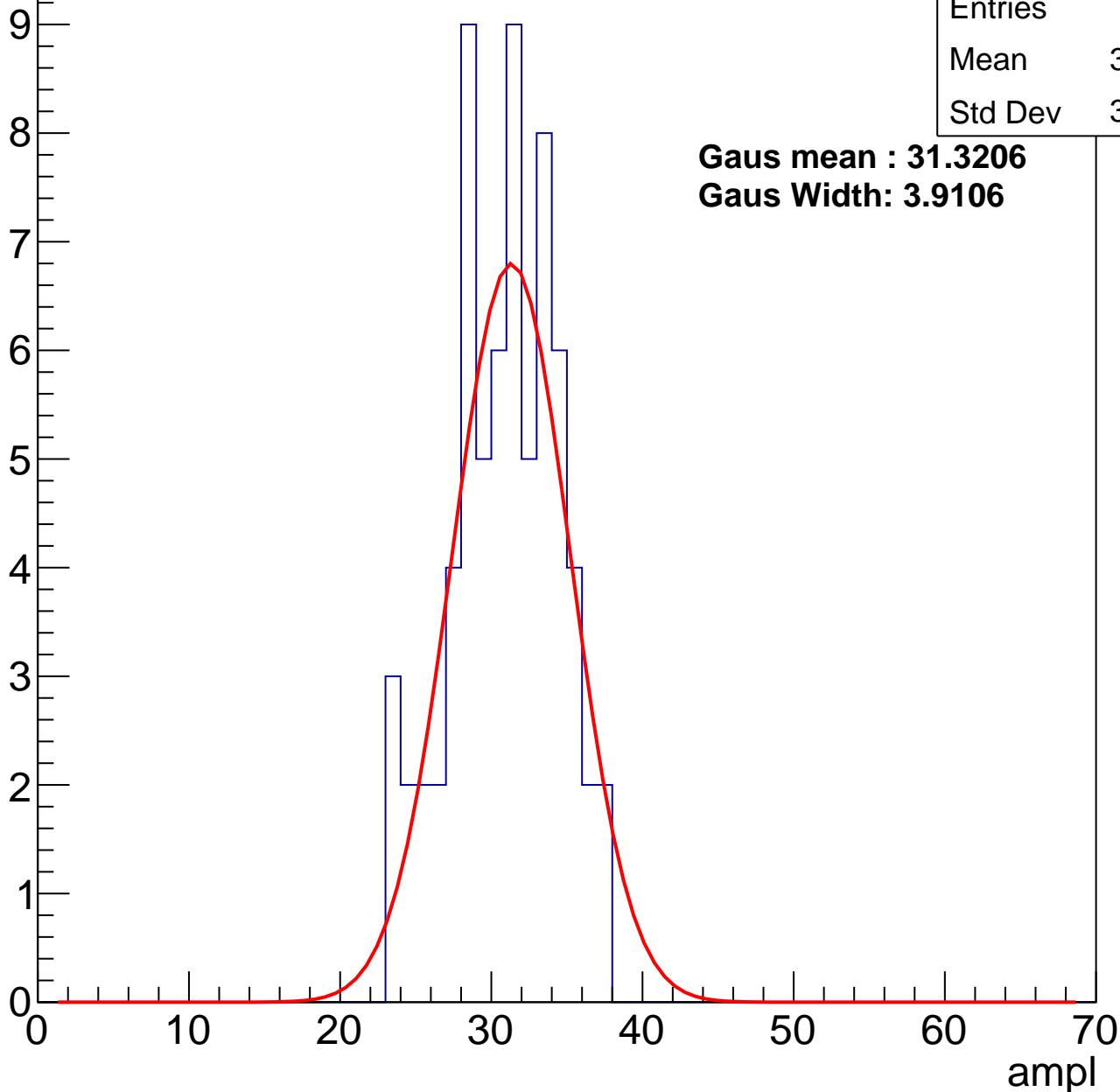
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	30.39
Std Dev	3.478

**Gaus mean : 31.3206**

**Gaus Width: 3.9106**



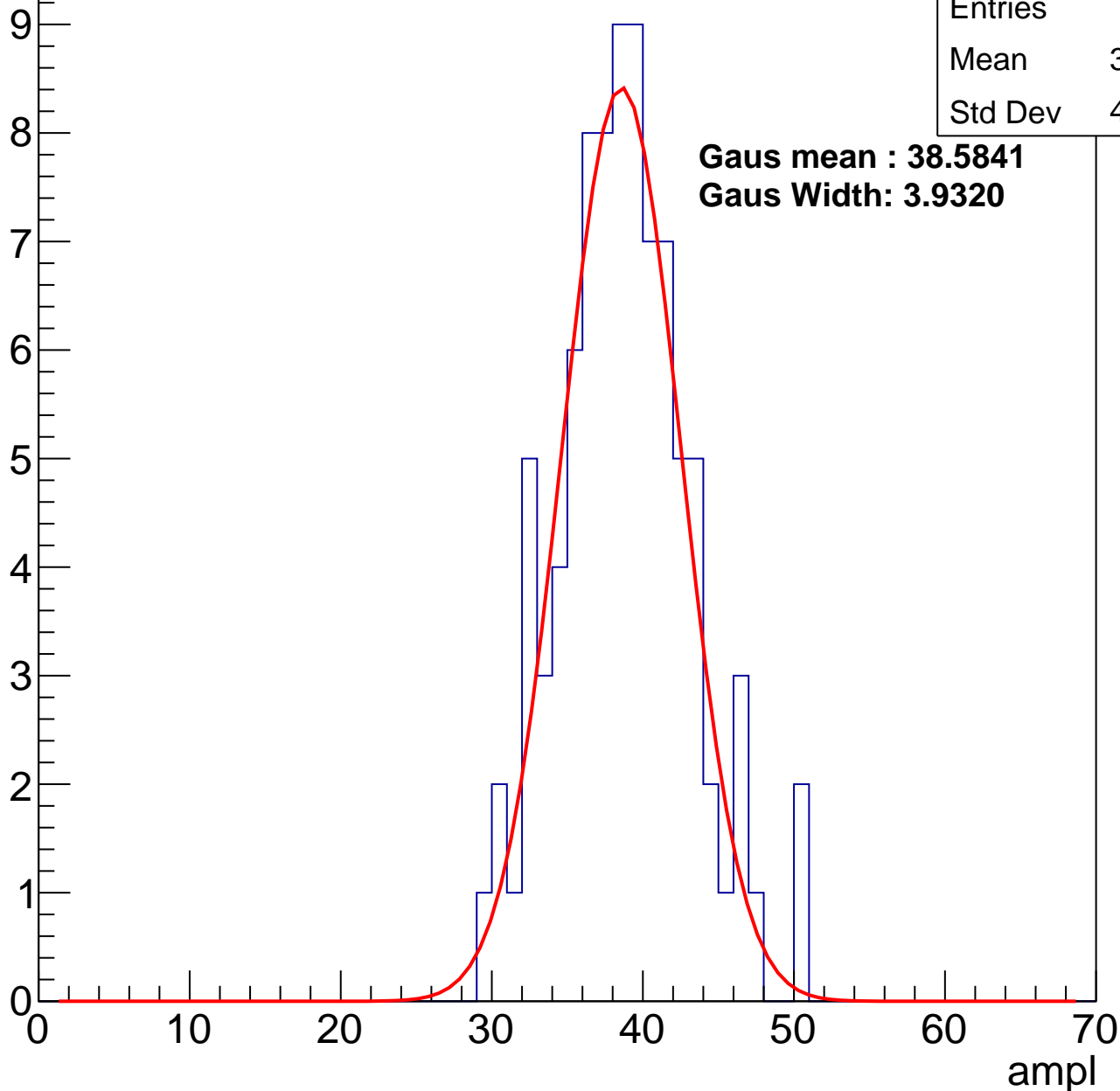
# B1L101S, U22-ch36, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	89
Mean	38.34
Std Dev	4.303

**Gaus mean : 38.5841**  
**Gaus Width: 3.9320**



# B1L101S, U22-ch36, adc2

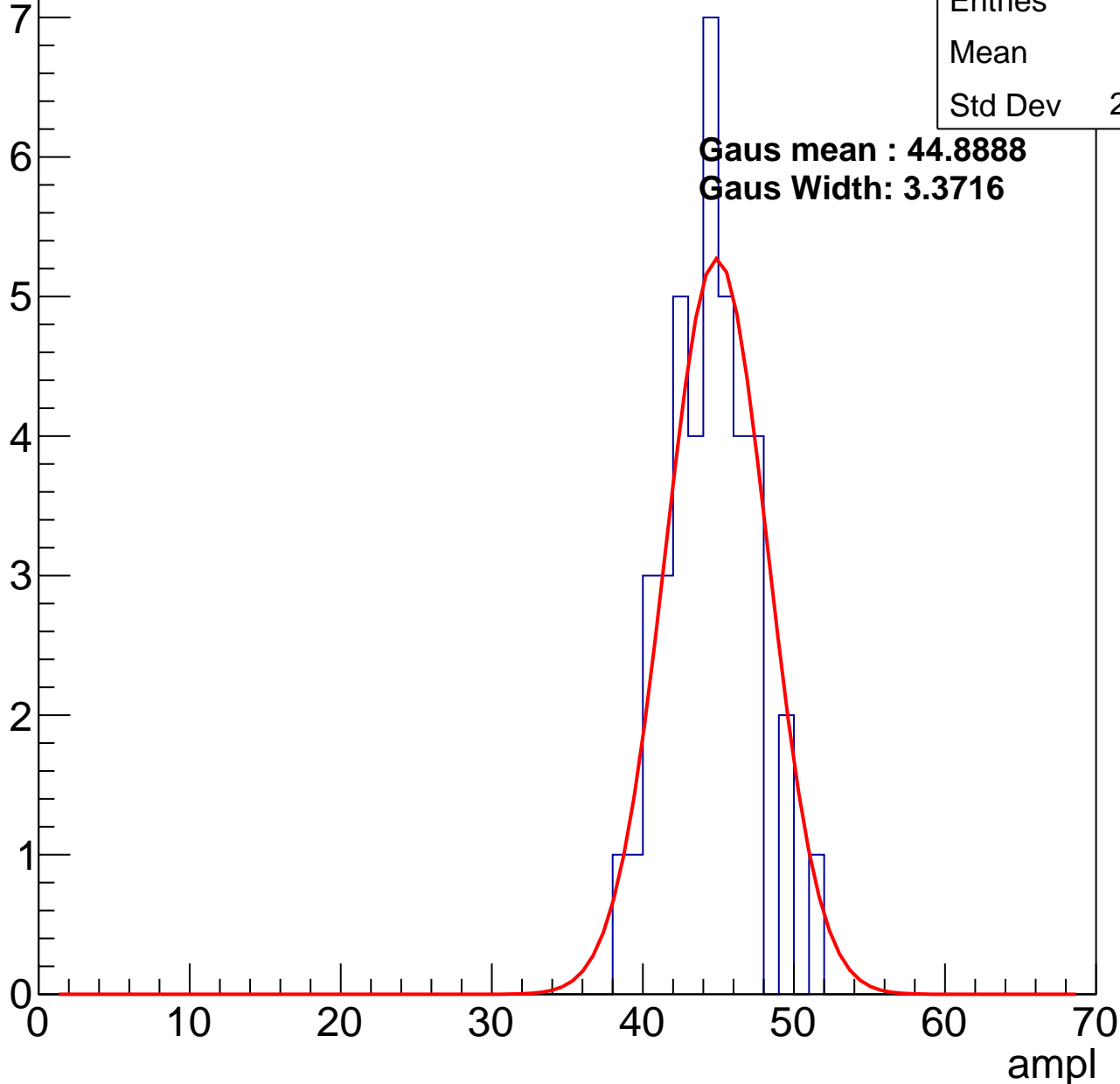
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	40
Mean	43.9
Std Dev	2.809

**Gaus mean : 44.8888**

**Gaus Width: 3.3716**

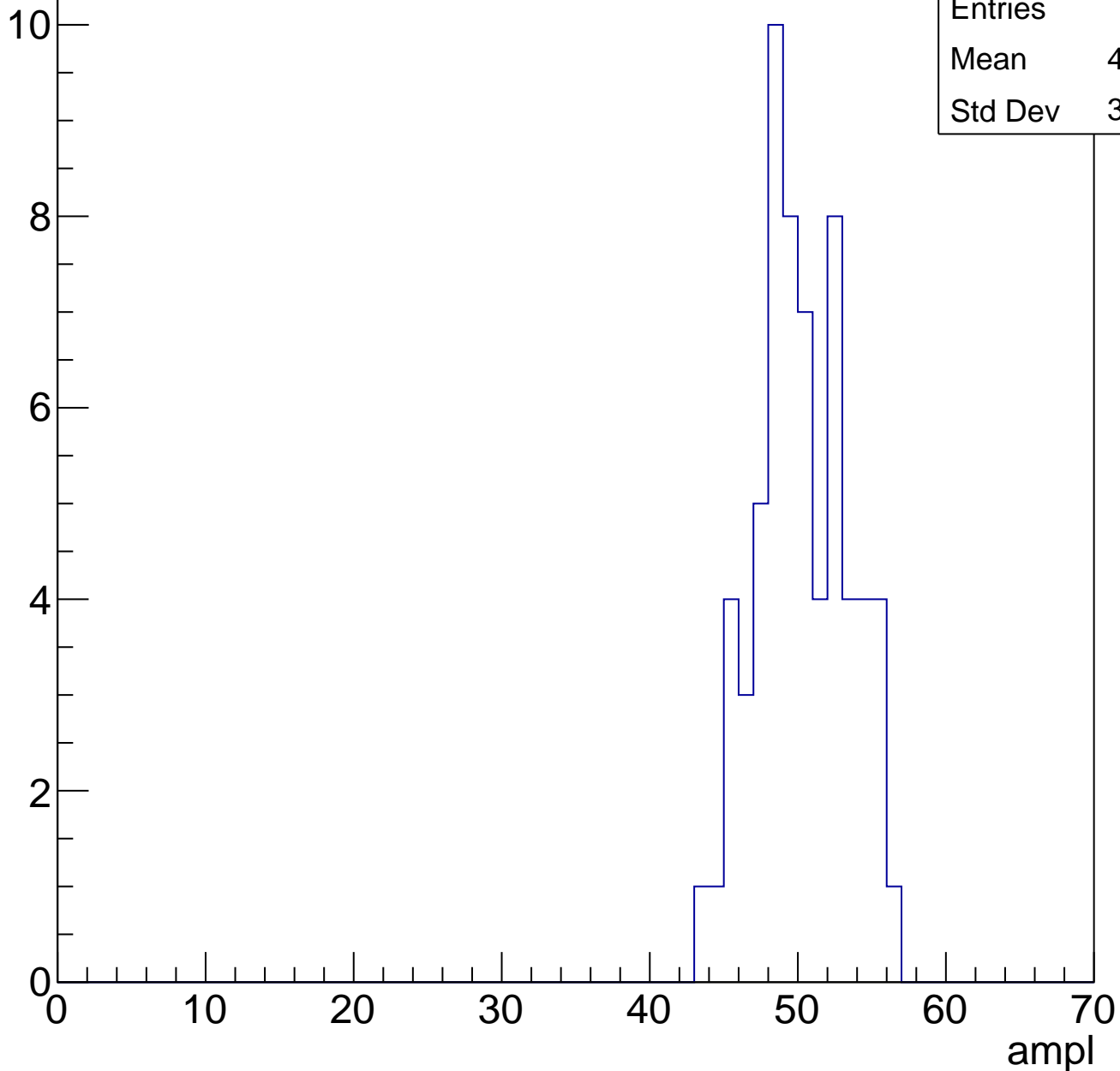


# B1L101S, U22-ch36, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

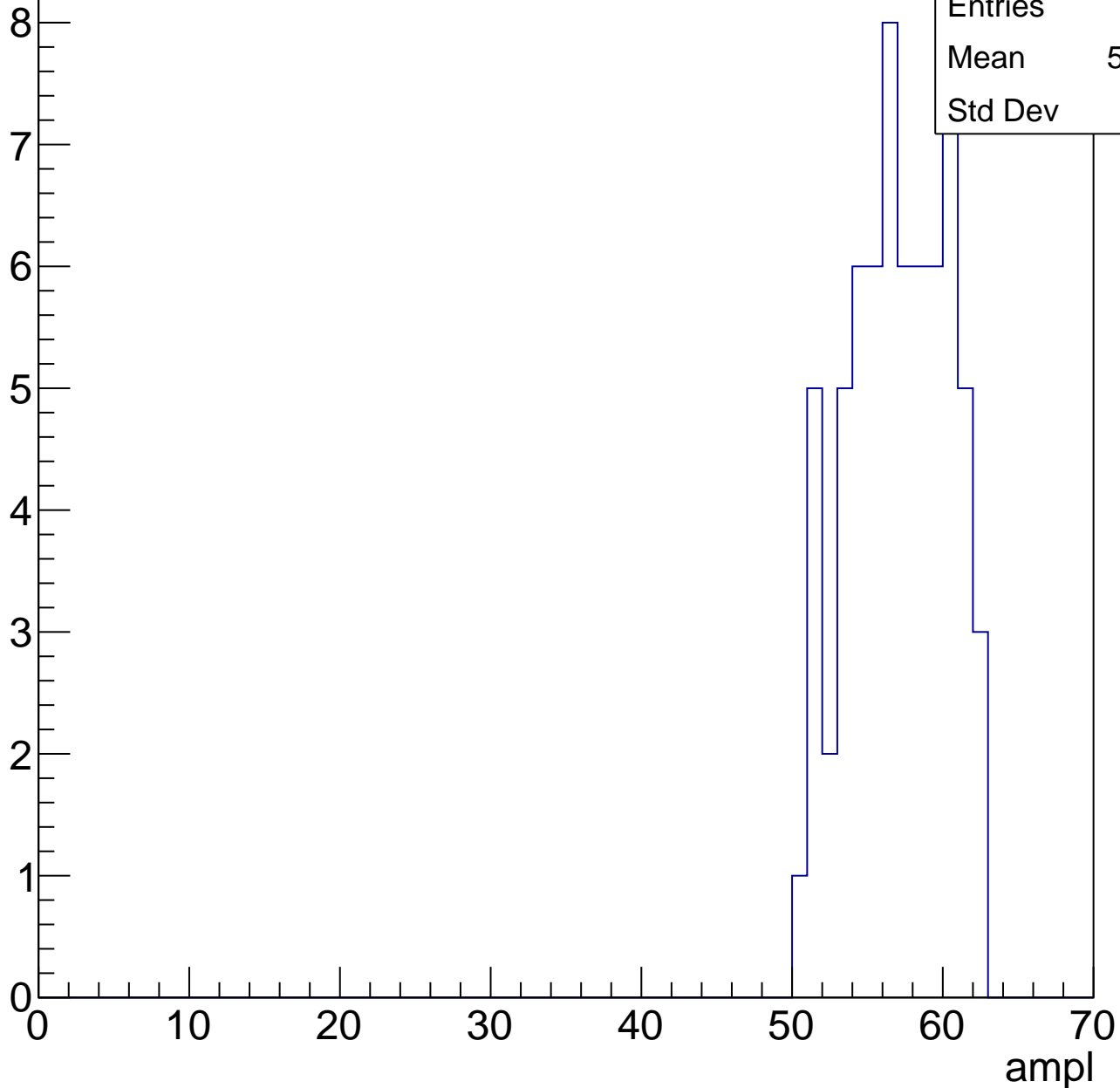
Entries	64
Mean	49.78
Std Dev	3.049



# B1L101S, U22-ch36, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

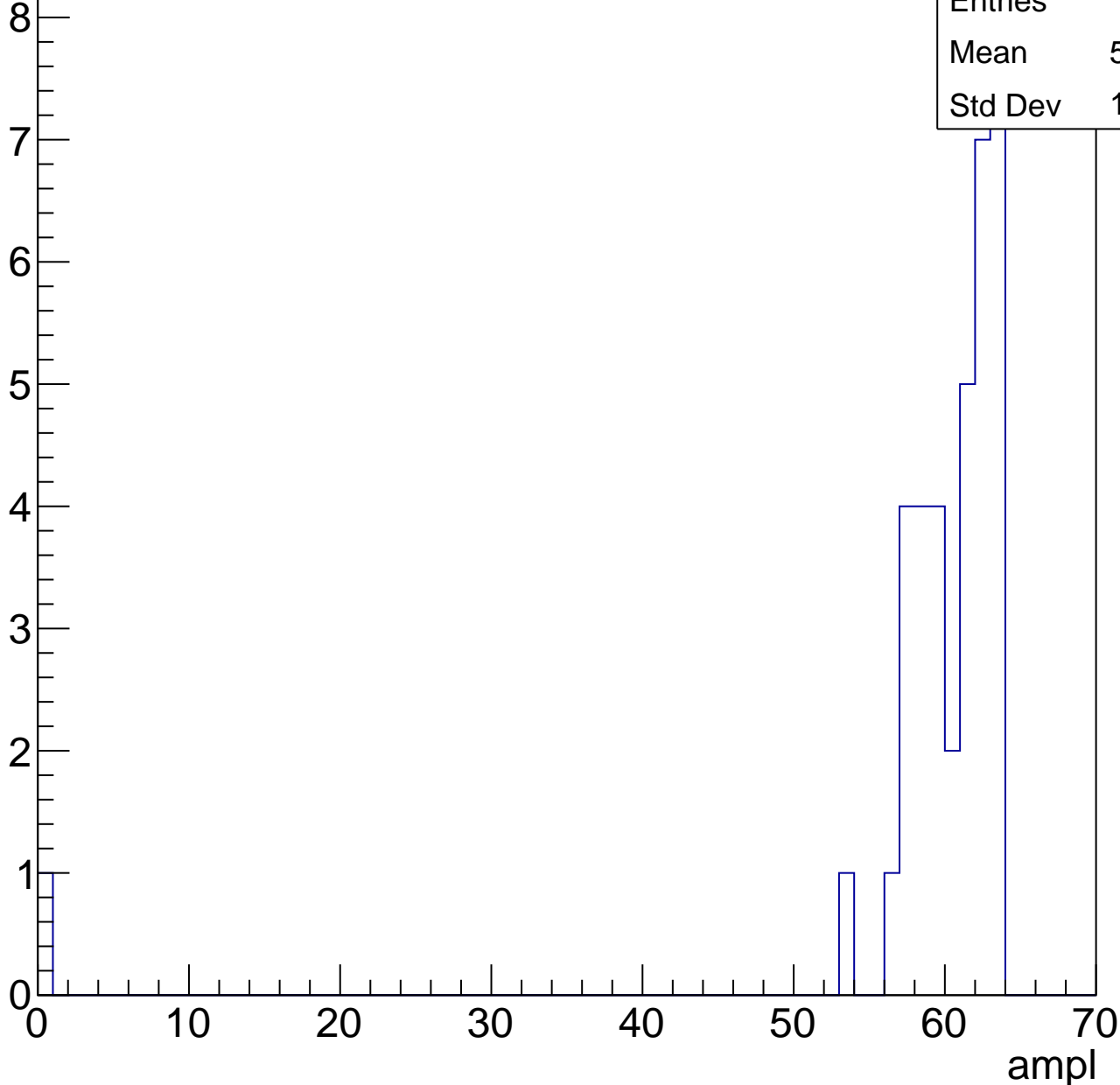


# B1L101S, U22-ch36, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	37
Mean	58.59
Std Dev	10.07



# B1L101S, U22-ch36, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U22-ch36, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U22-ch37, adc0

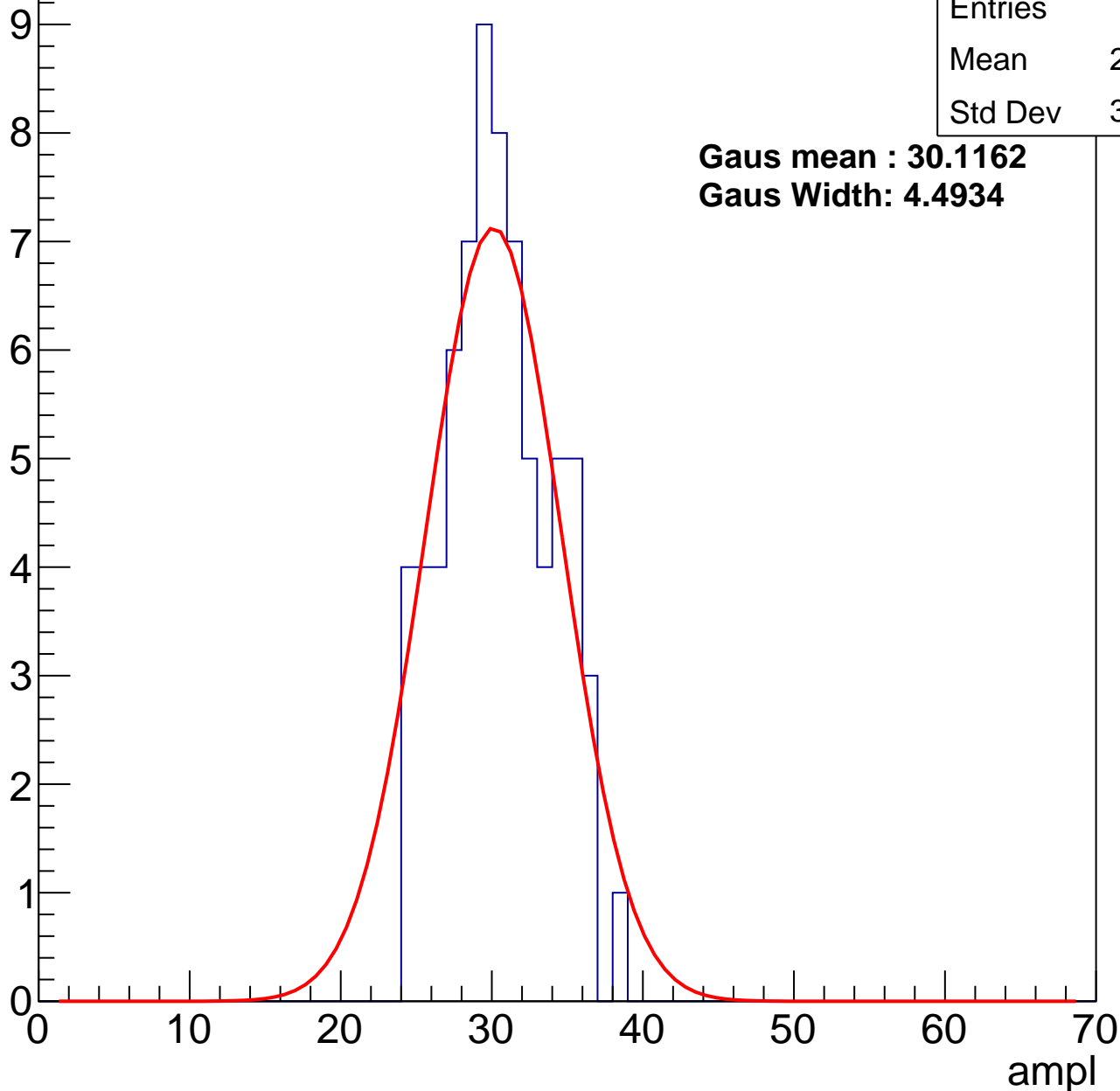
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	72
Mean	29.99
Std Dev	3.414

**Gaus mean : 30.1162**

**Gaus Width: 4.4934**



# B1L101S, U22-ch37, adc1

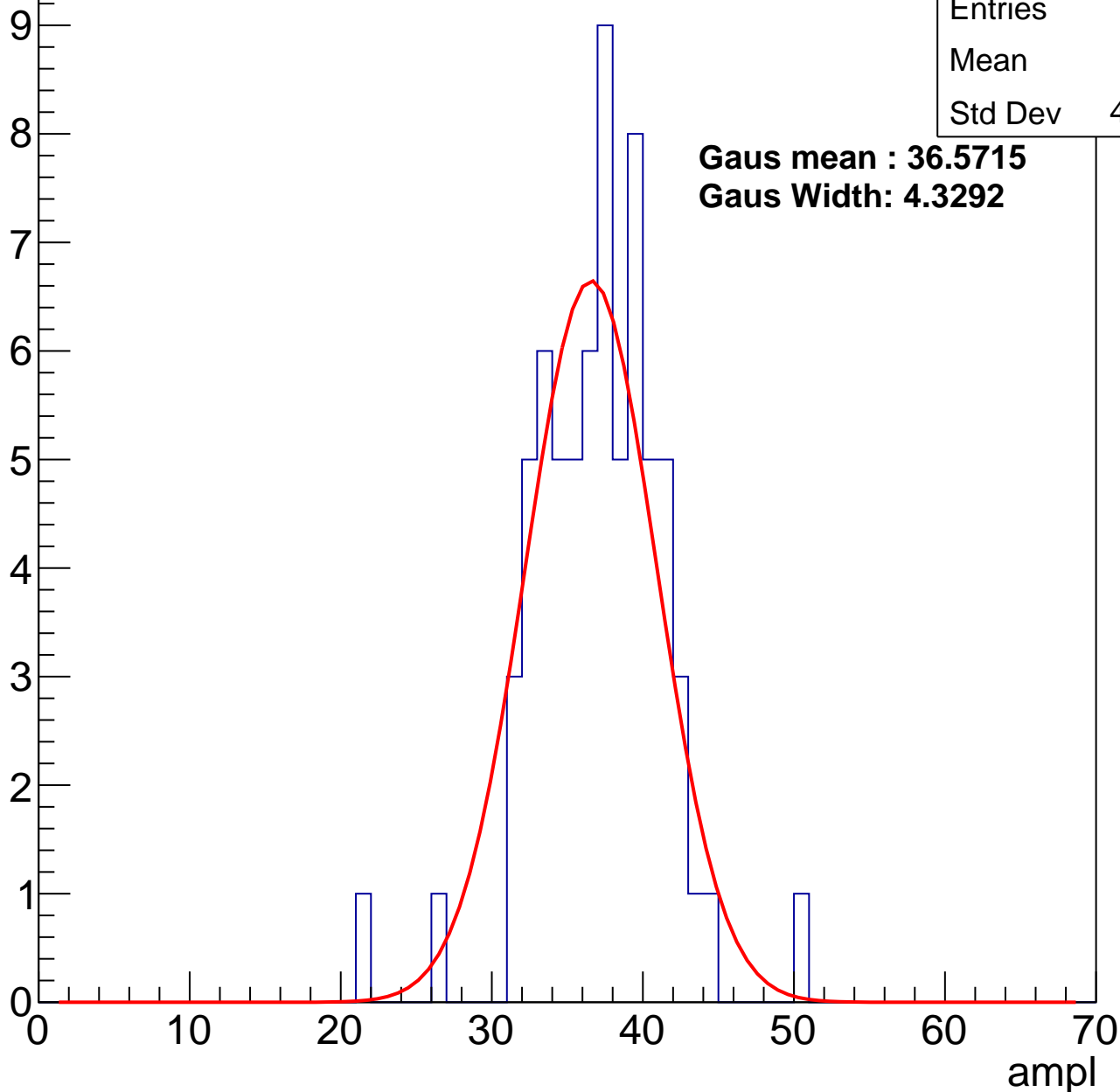
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	36.6
Std Dev	4.237

**Gaus mean : 36.5715**

**Gaus Width: 4.3292**



# B1L101S, U22-ch37, adc2

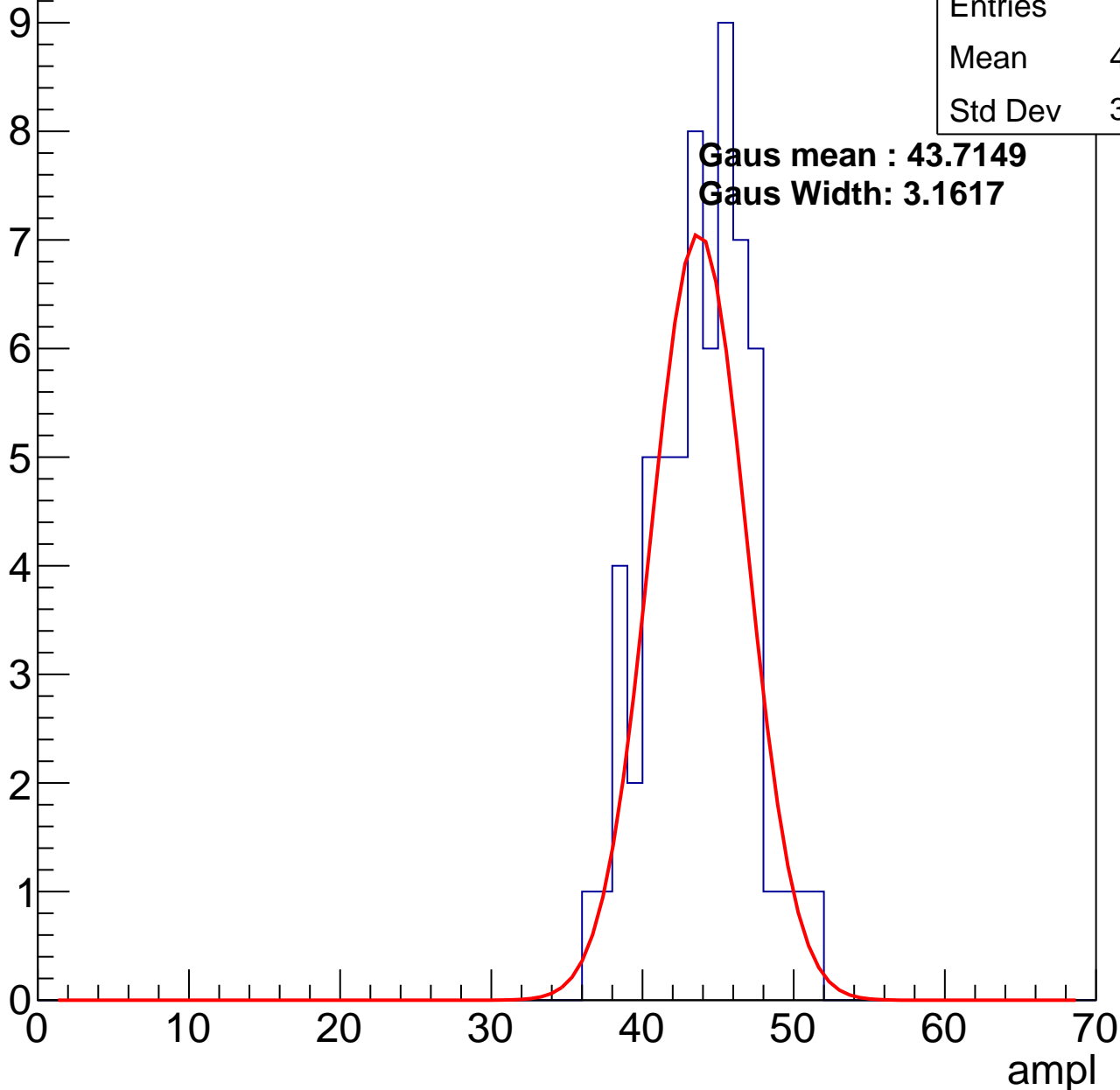
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	43.38
Std Dev	3.219

**Gaus mean : 43.7149**

**Gaus Width: 3.1617**

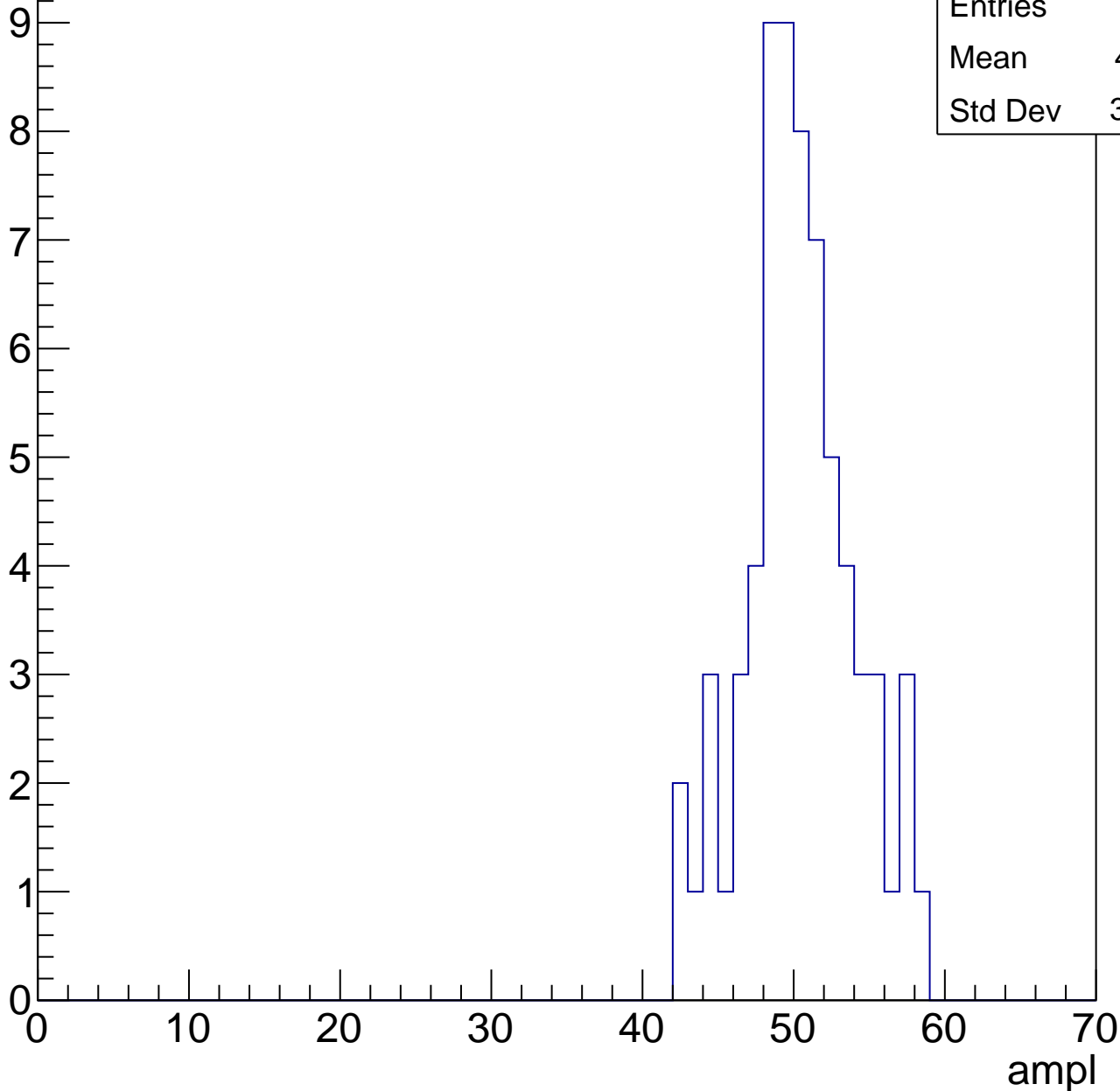


# B1L101S, U22-ch37, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	67
Mean	49.91
Std Dev	3.607

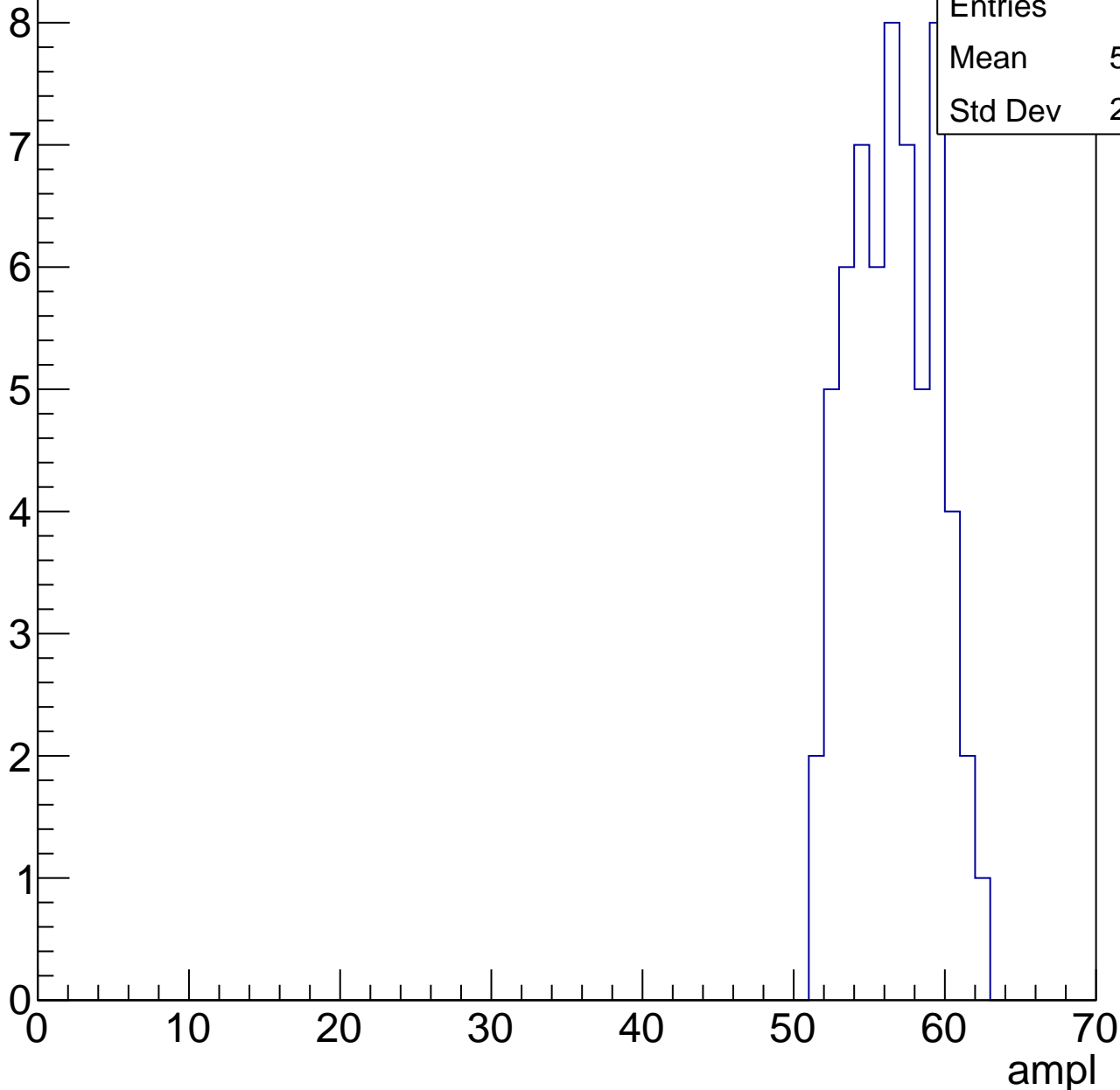


# B1L101S, U22-ch37, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	56.08
Std Dev	2.766

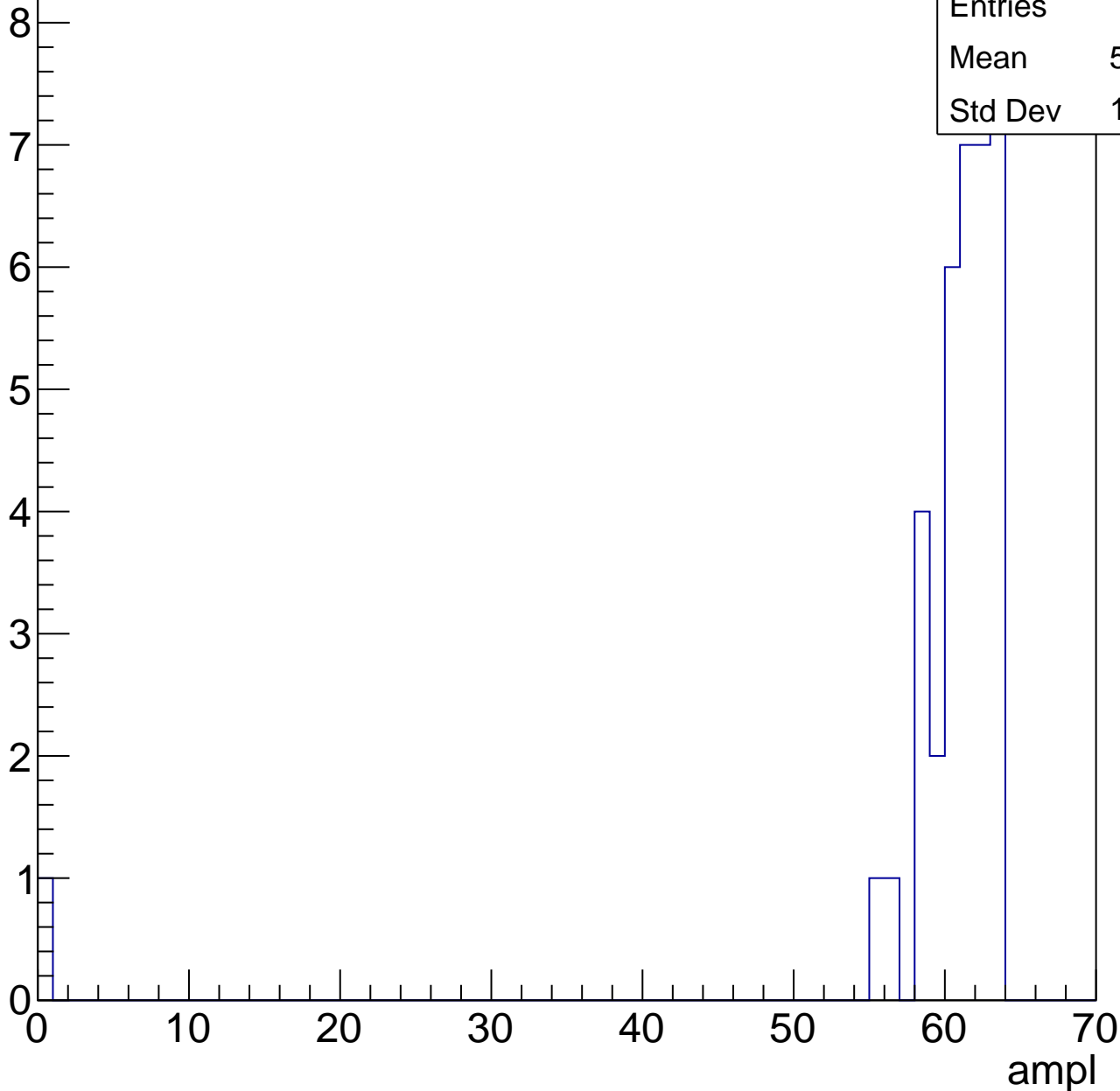


# B1L101S, U22-ch37, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	37
Mean	59.08
Std Dev	10.05



# B1L101S, U22-ch37, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	5
Mean	62.2
Std Dev	0.7483

ampl

0 10 20 30 40 50 60 70



# B1L101S, U22-ch37, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

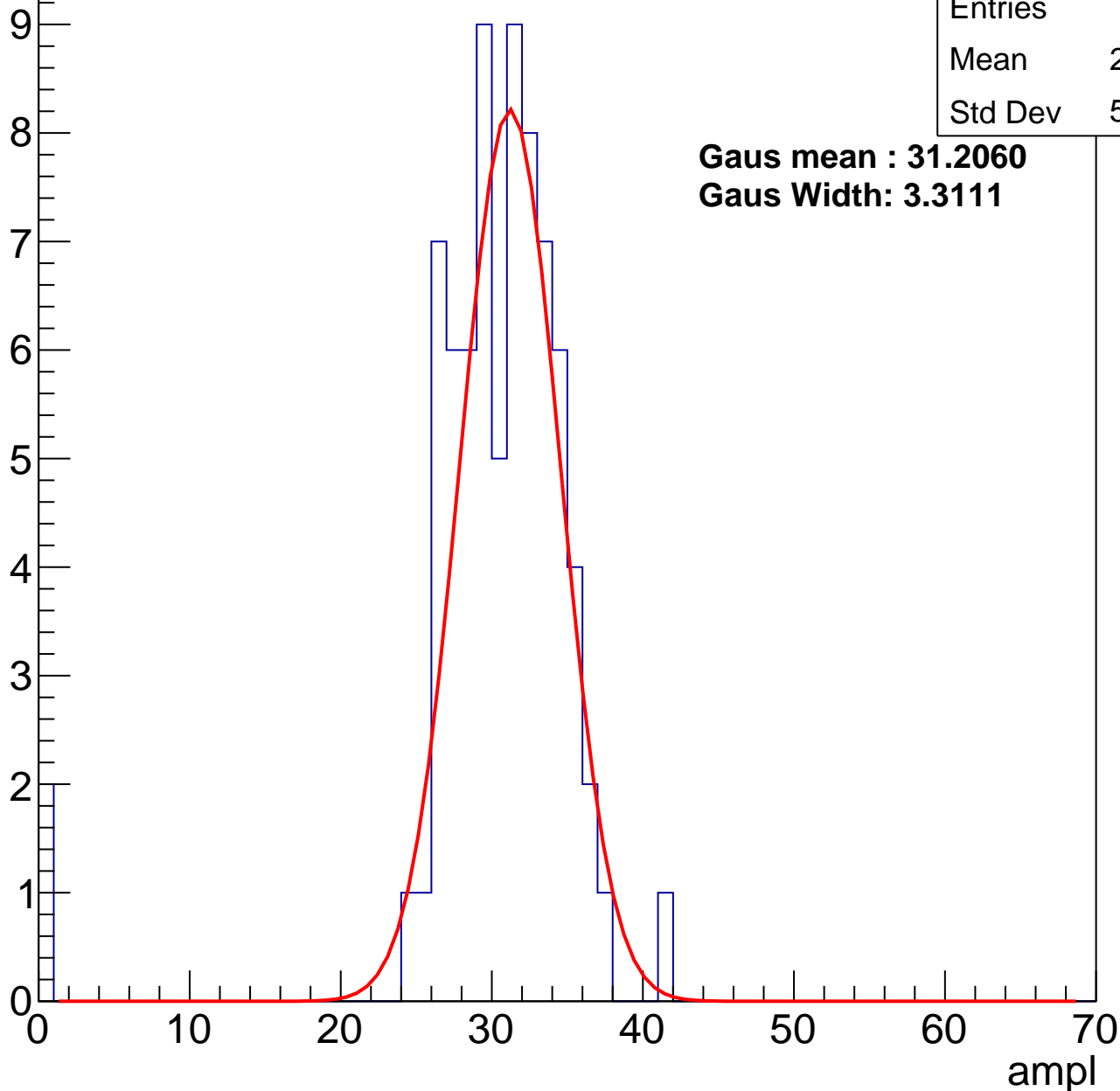


Entries	0
Mean	0
Std Dev	0

# B1L101S, U22-ch38, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U22-ch38, adc1

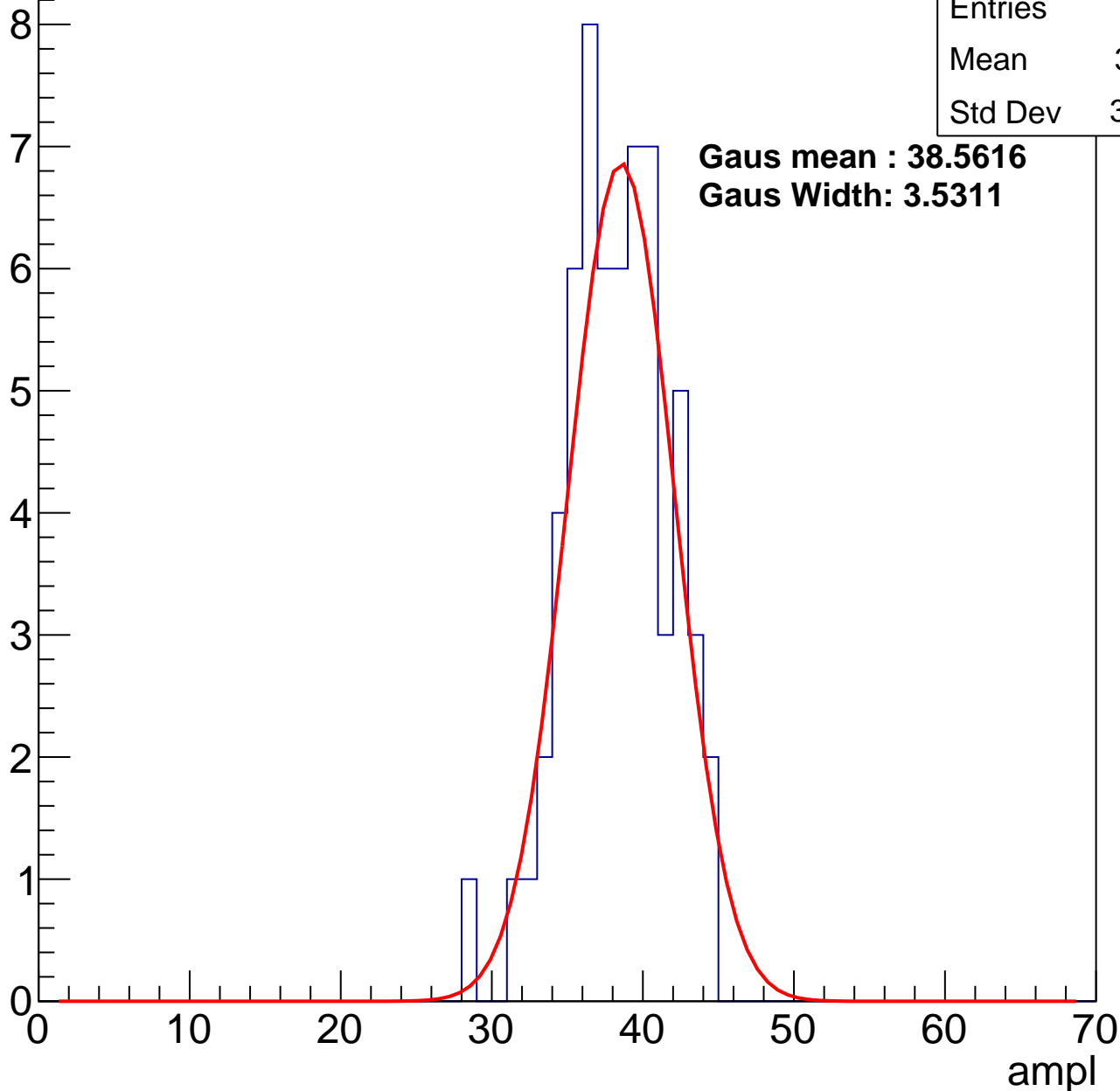
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	37.81
Std Dev	3.306

**Gaus mean : 38.5616**

**Gaus Width: 3.5311**



# B1L101S, U22-ch38, adc2

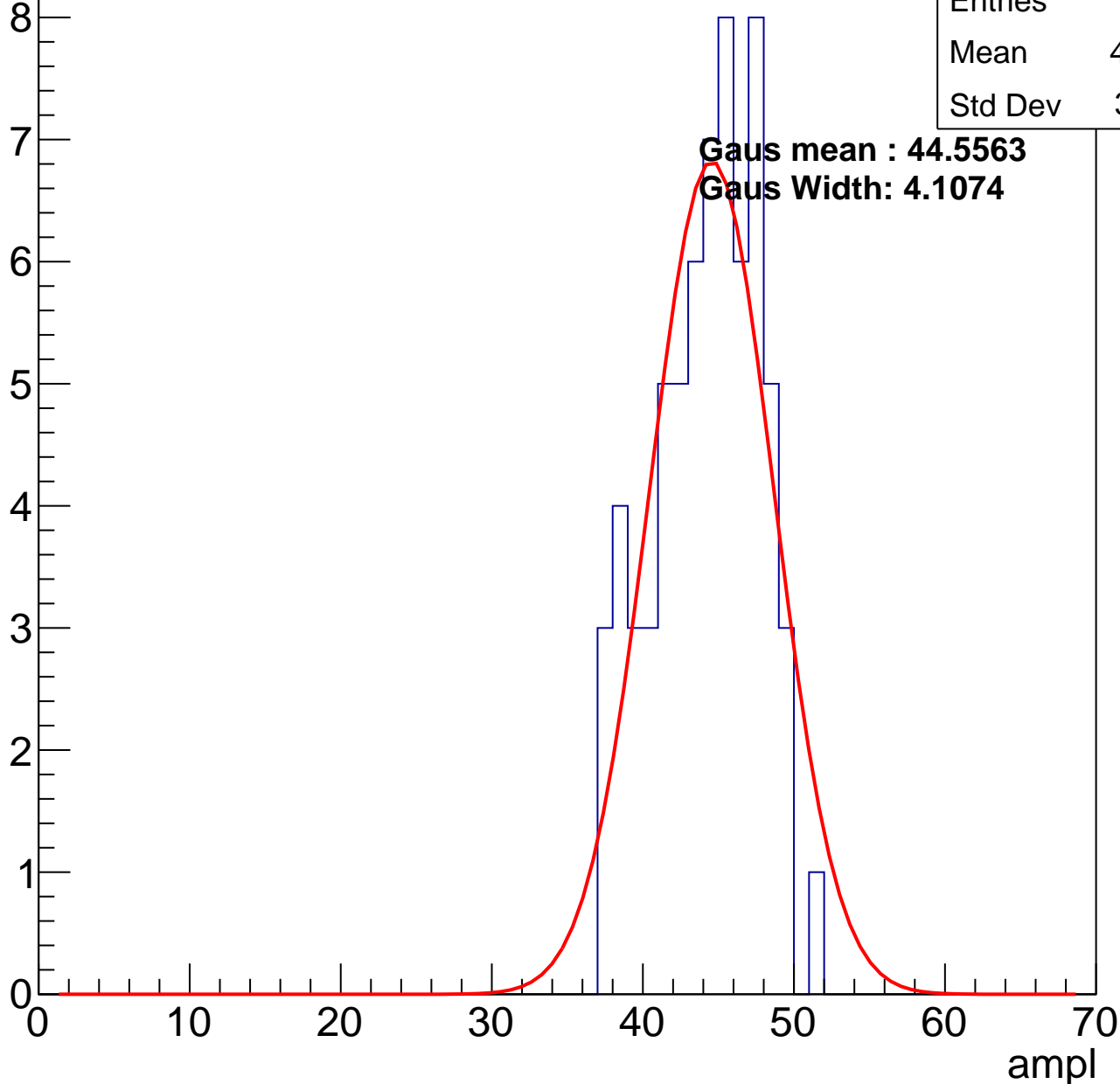
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	67
Mean	43.75
Std Dev	3.431

**Gaus mean : 44.5563**

**Gaus Width: 4.1074**

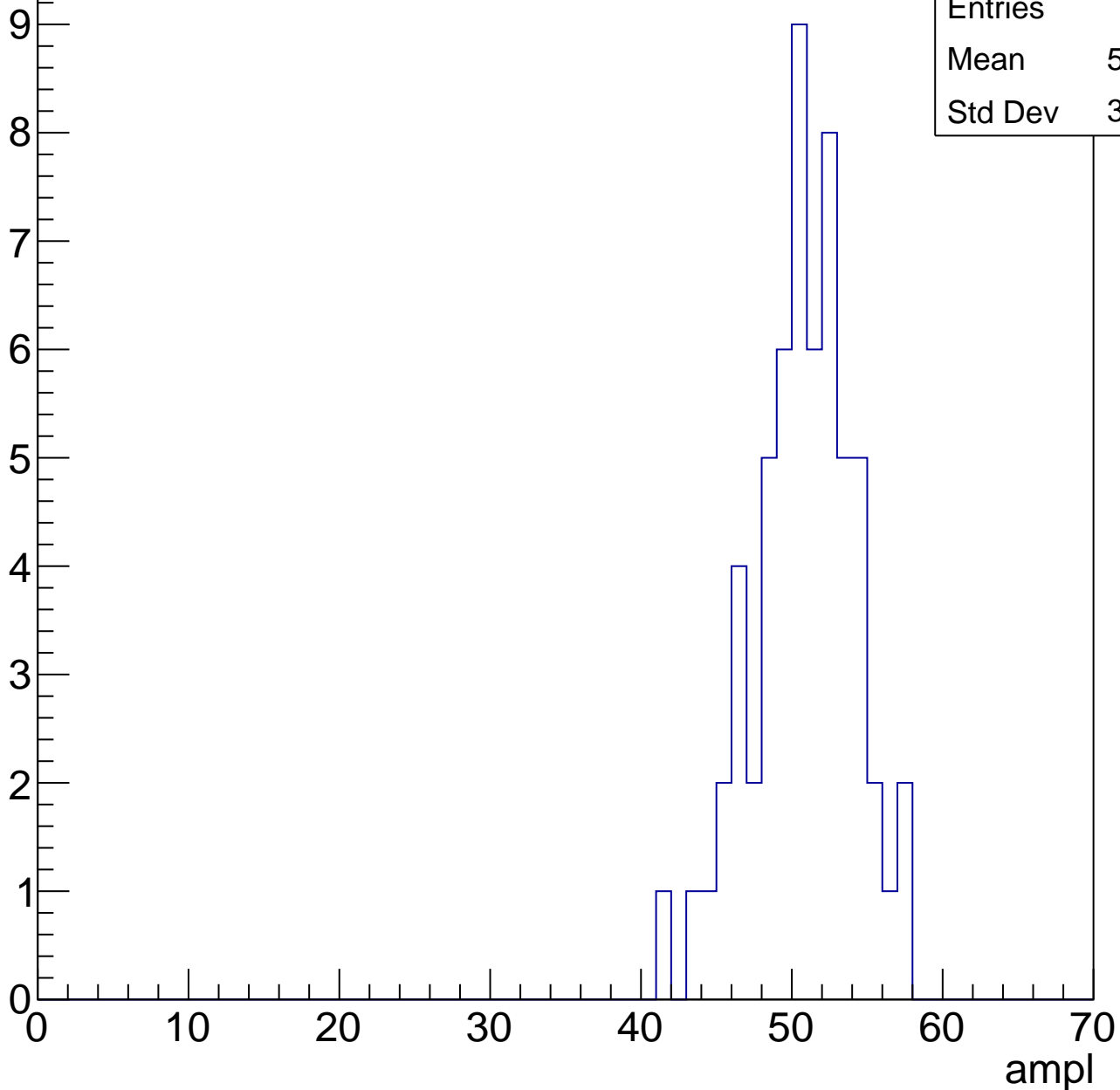


# B1L101S, U22-ch38, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

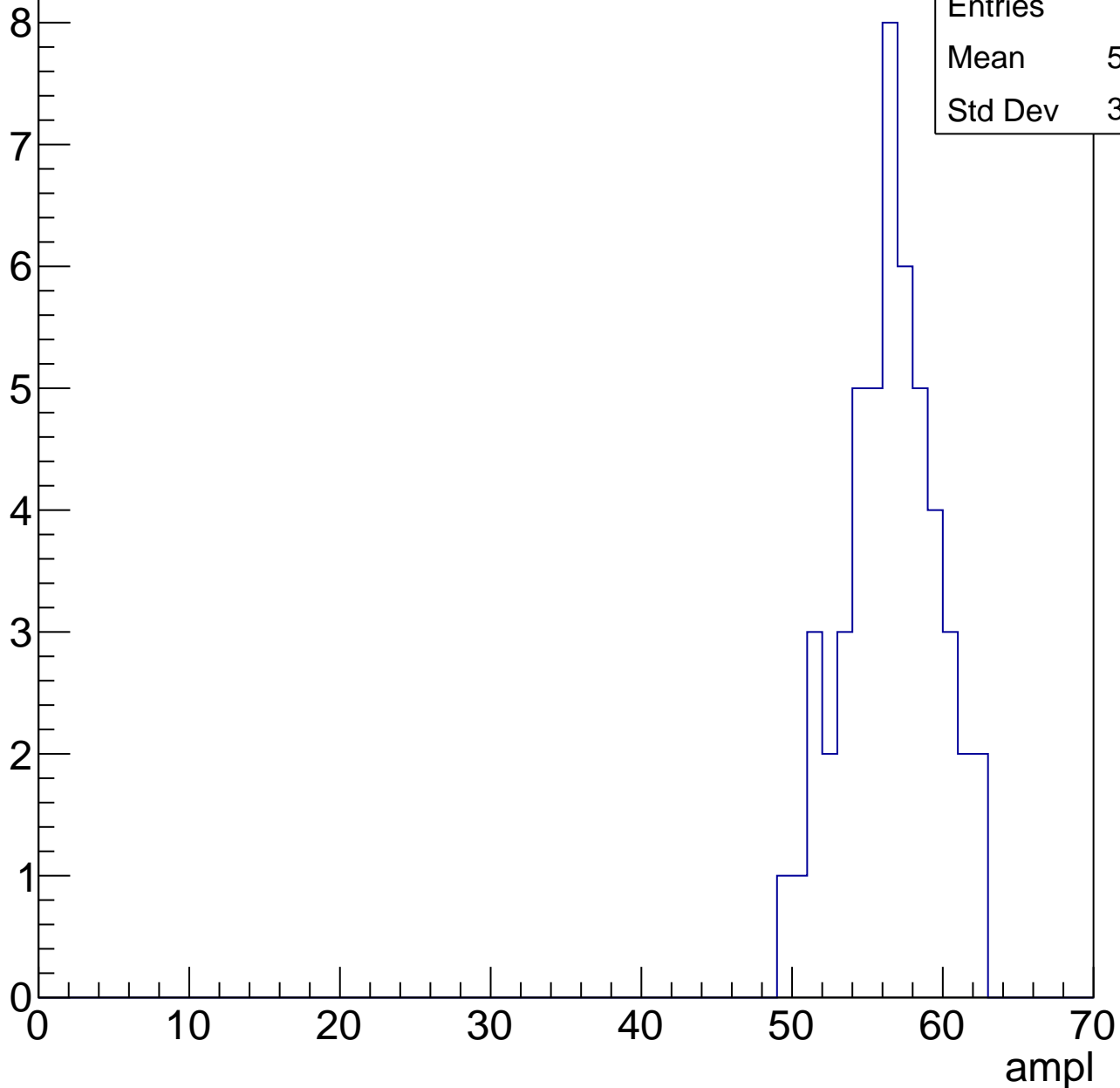
Entries	60
Mean	50.28
Std Dev	3.332



# B1L101S, U22-ch38, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

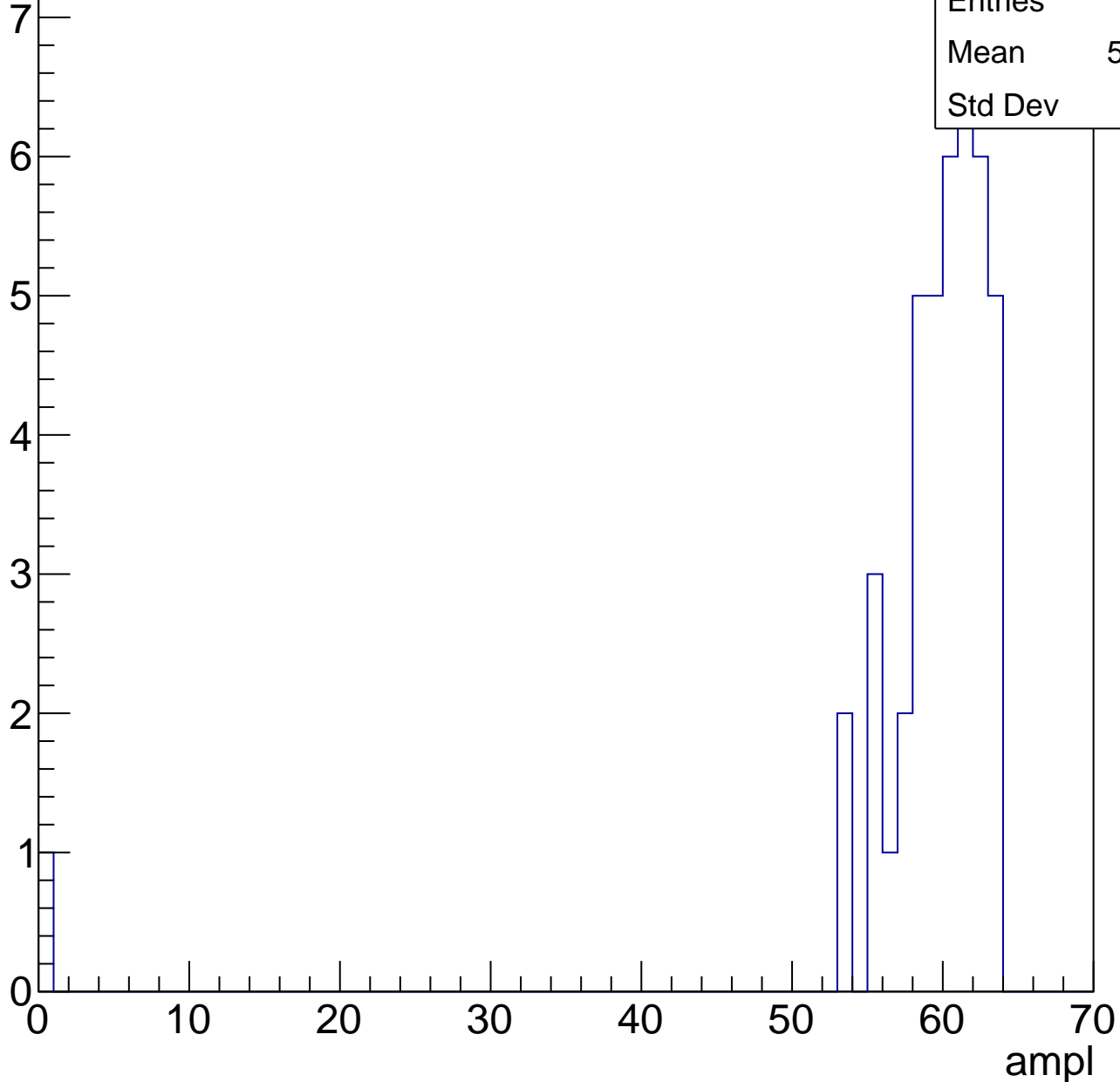
Entry



# B1L101S, U22-ch38, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

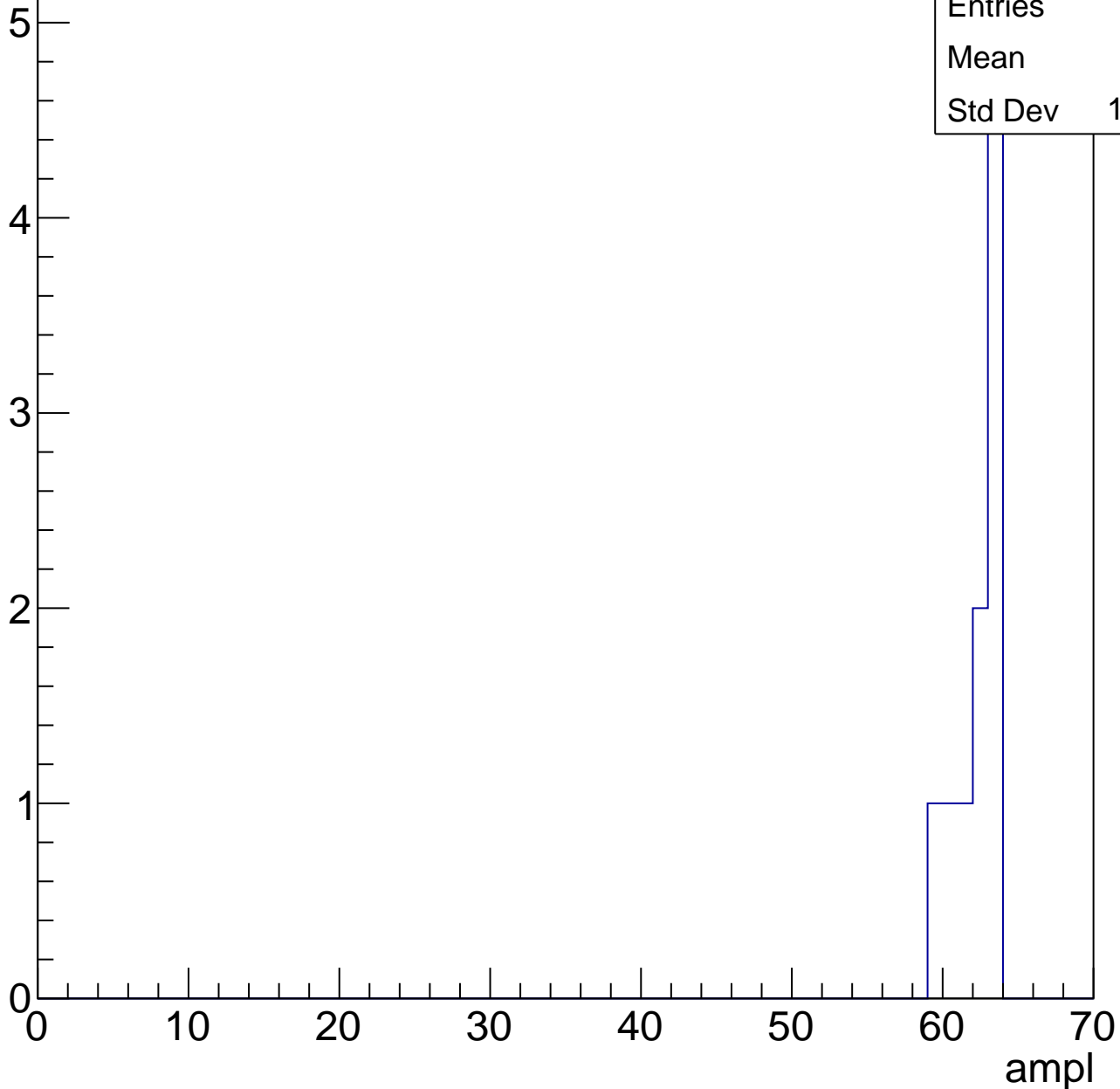


# B1L101S, U22-ch38, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	10
Mean	61.9
Std Dev	1.375





# B1L101S, U22-ch38, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U22-ch39, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	86
Mean	30.24
Std Dev	4.93

**Gaus mean : 30.7764**

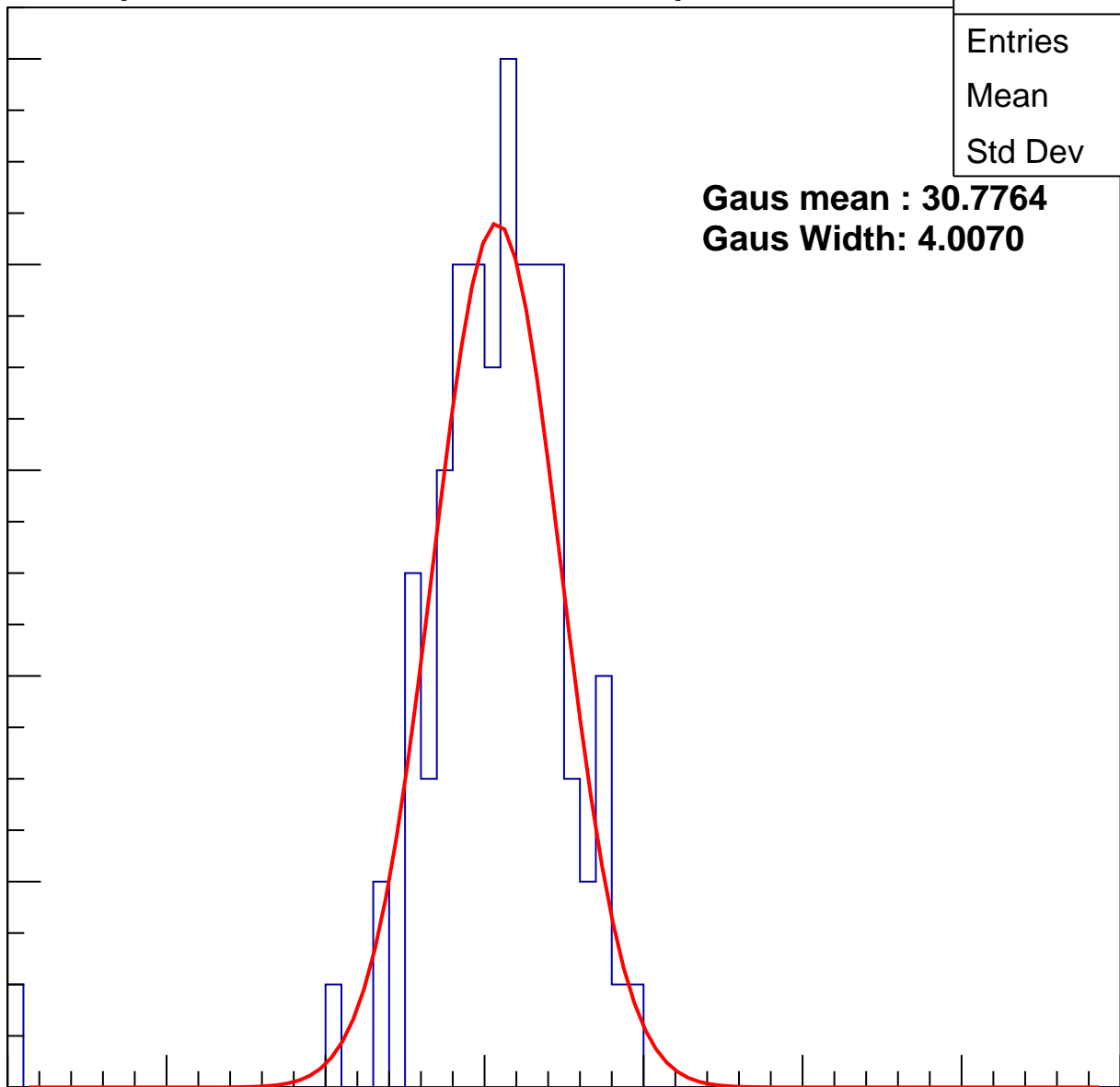
**Gaus Width: 4.0070**

Entry

10  
8  
6  
4  
2  
0

ampl

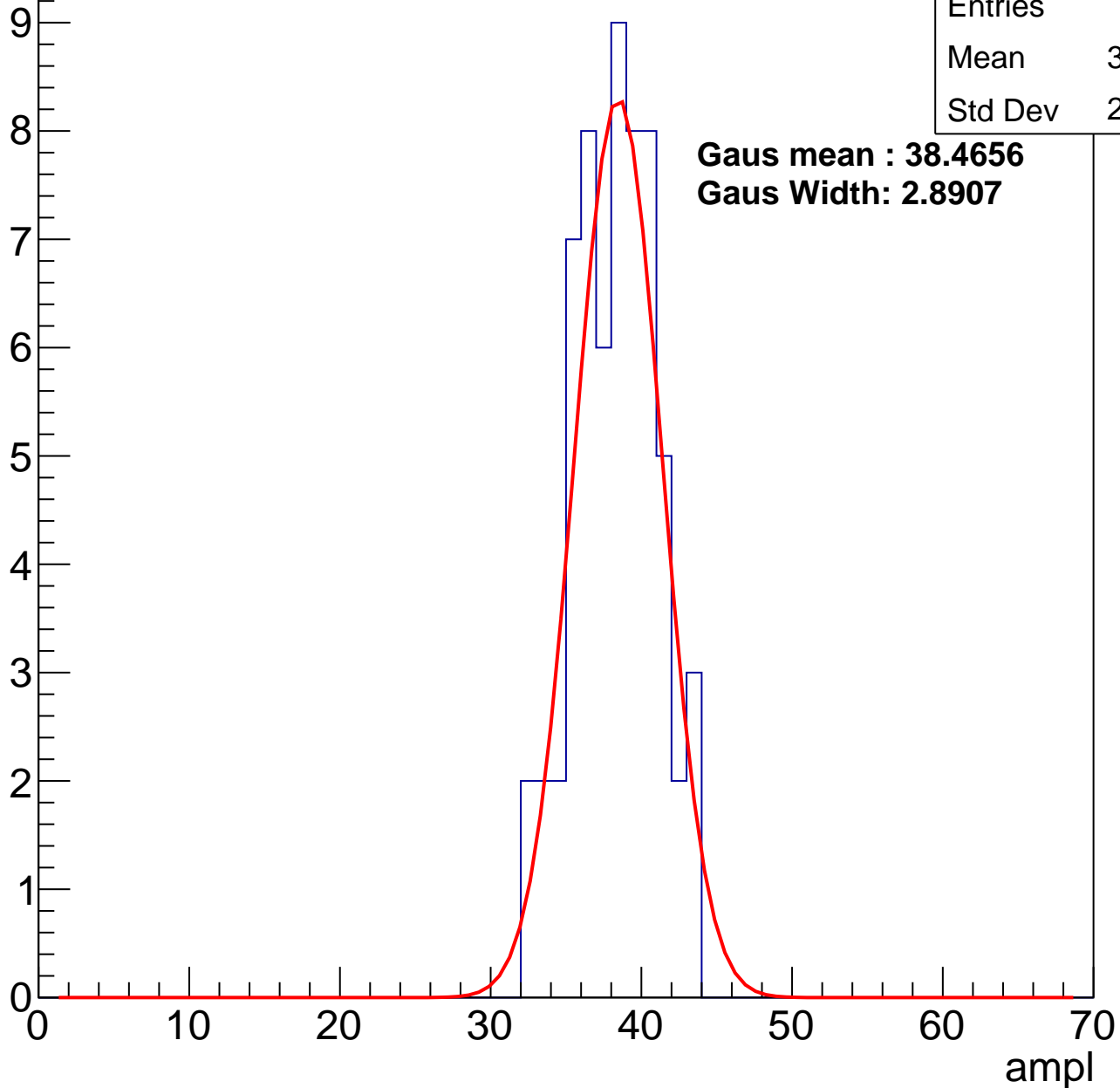
0 10 20 30 40 50 60 70



# B1L101S, U22-ch39, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U22-ch39, adc2

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	44.99
Std Dev	3.014

**Gaus mean : 45.3341**

**Gaus Width: 3.1088**

10

8

6

4

2

0

0

10

20

30

40

50

60

70

ampl

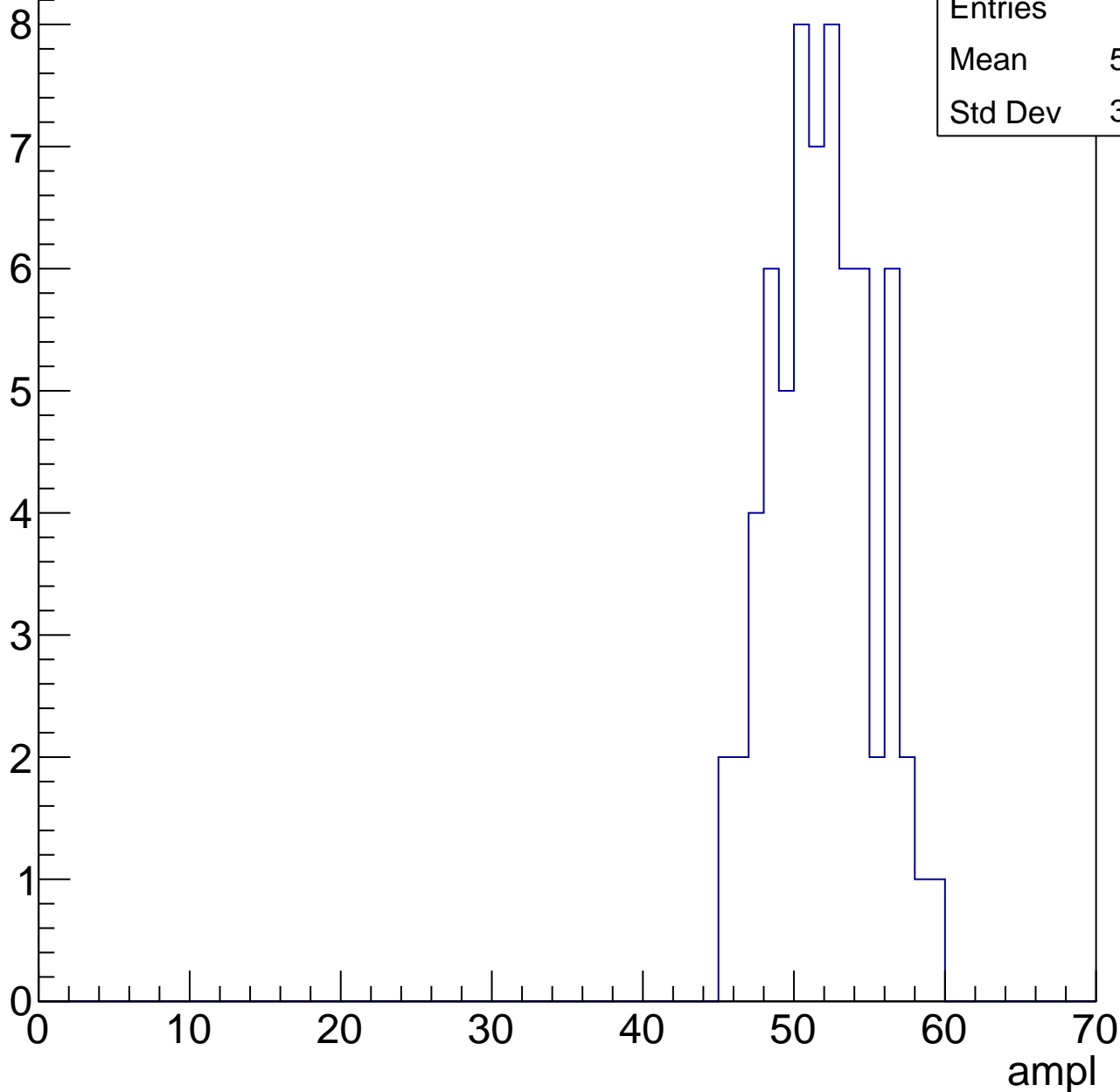
0 10 20 30 40 50 60 70

# B1L101S, U22-ch39, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

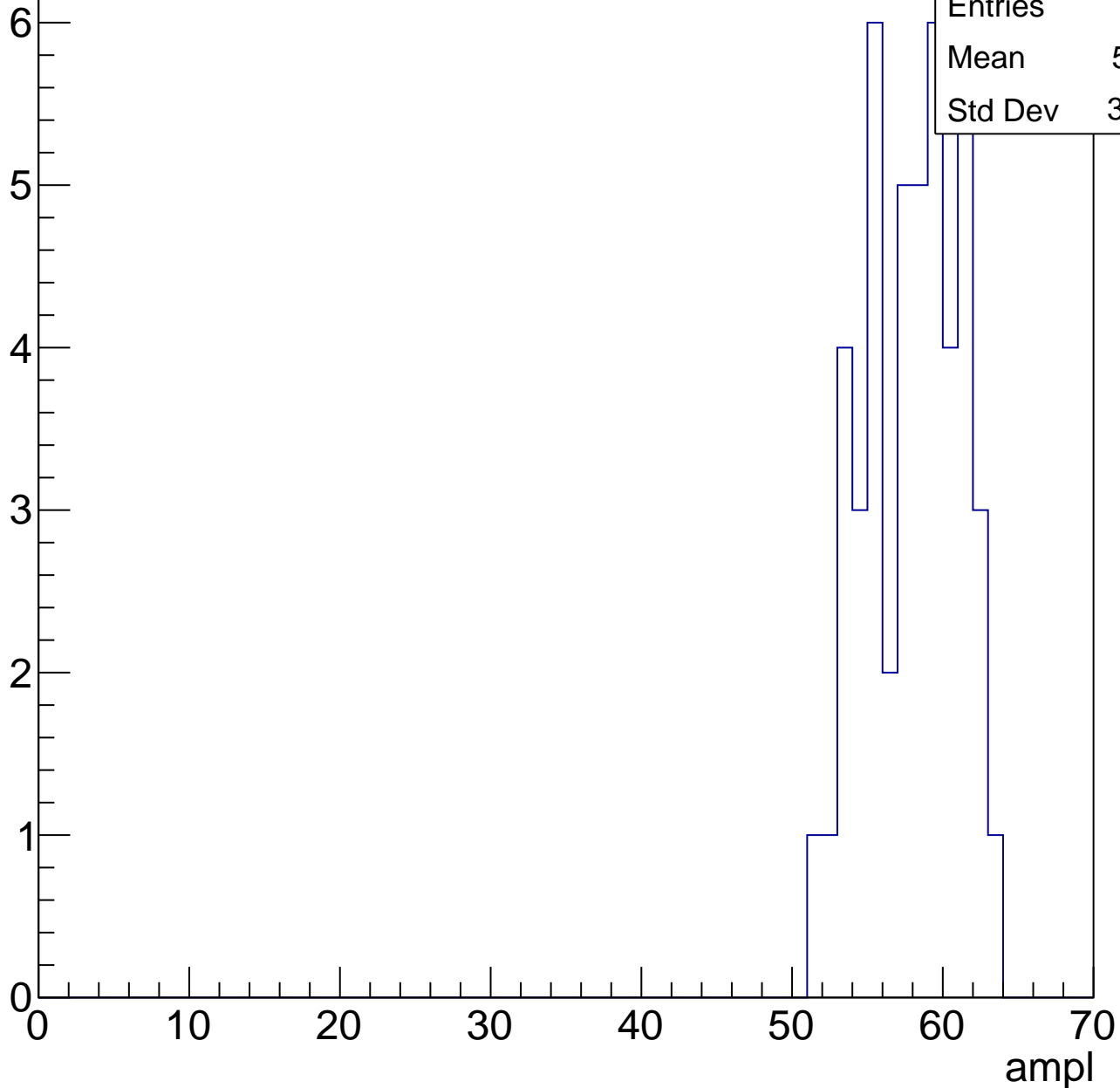
Entries	66
Mean	51.44
Std Dev	3.276



# B1L101S, U22-ch39, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

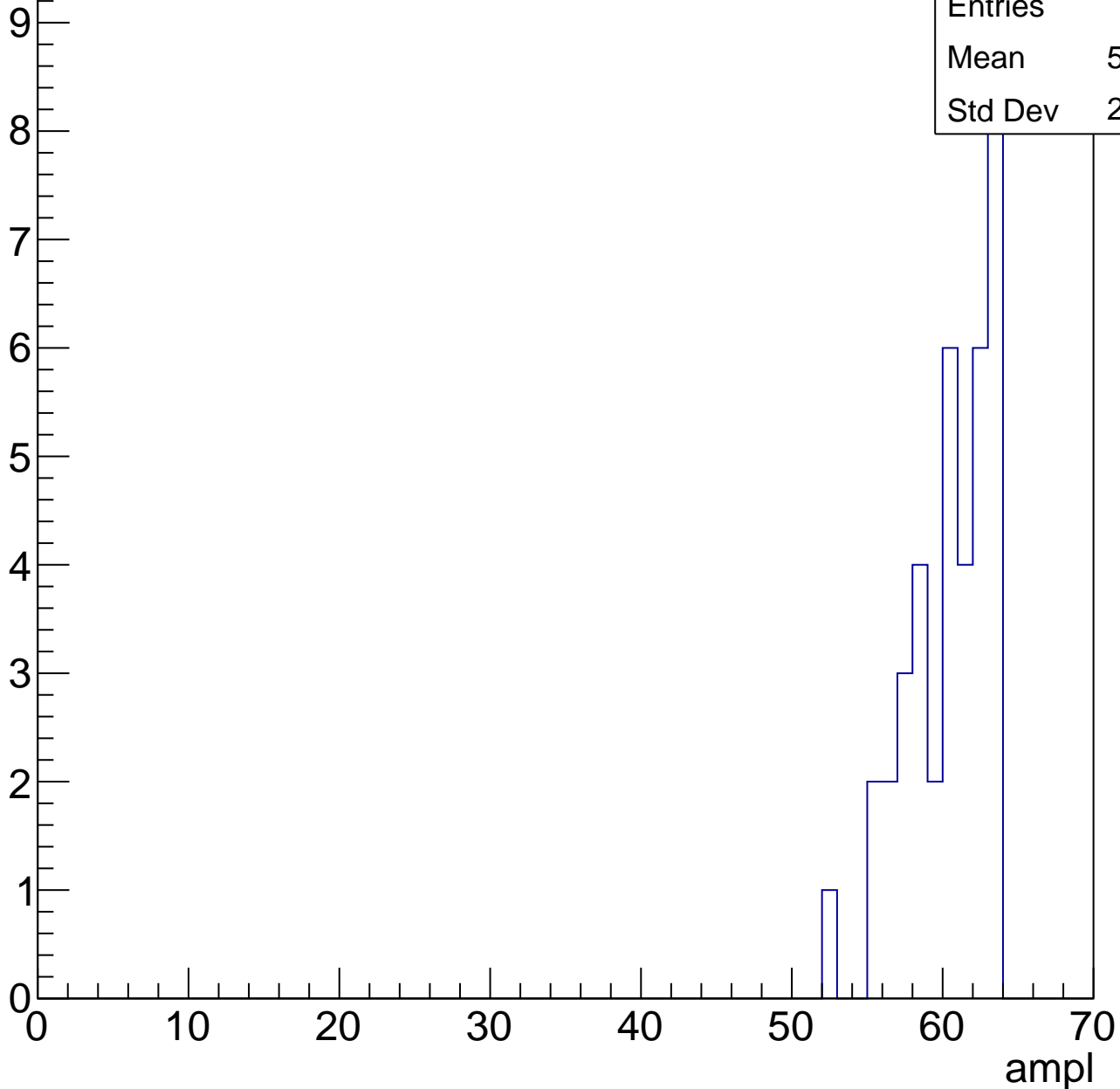


# B1L101S, U22-ch39, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

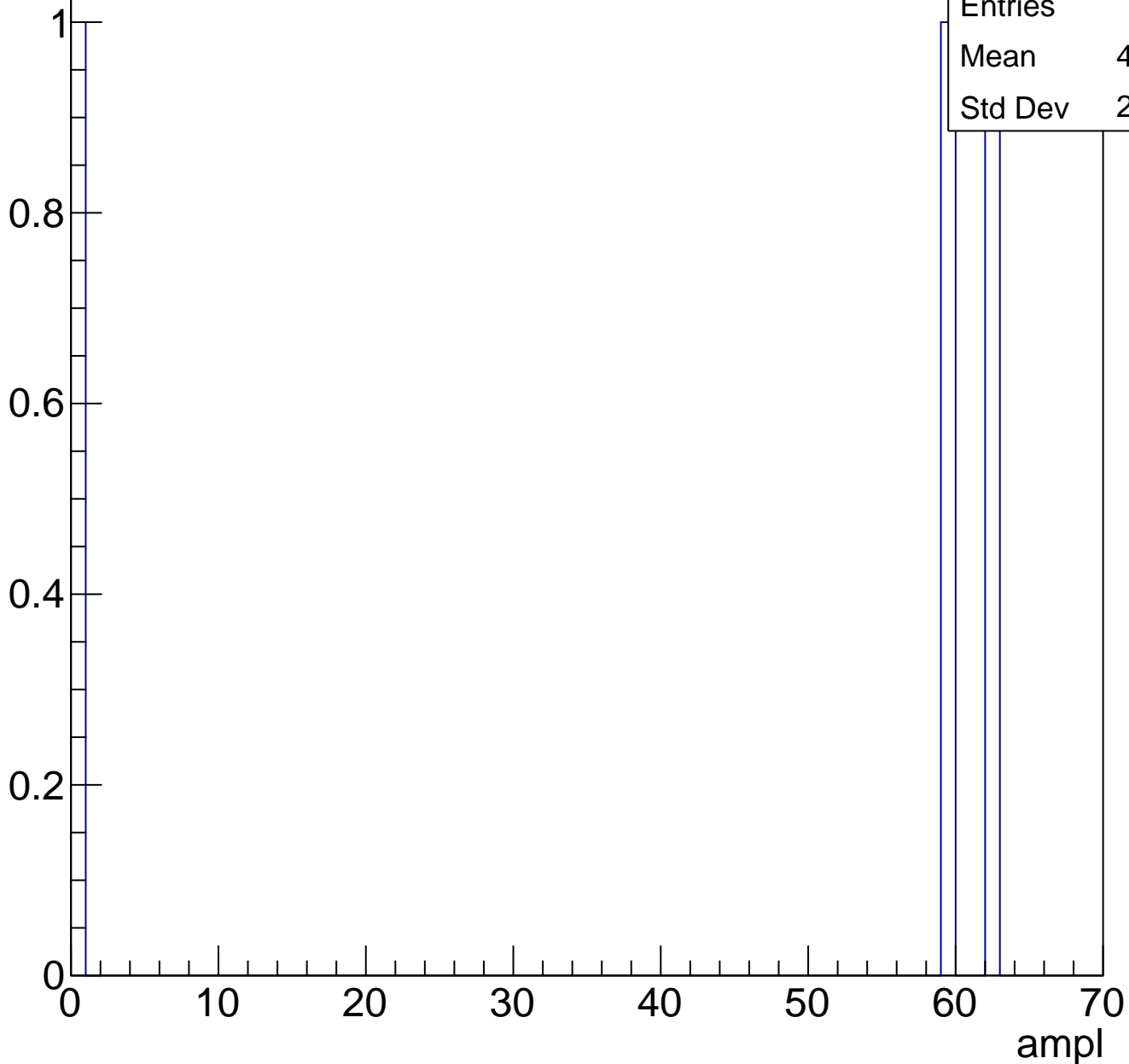
Entries	39
Mean	59.95
Std Dev	2.773



# B1L101S, U22-ch39, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U22-ch39, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U22-ch40, adc0

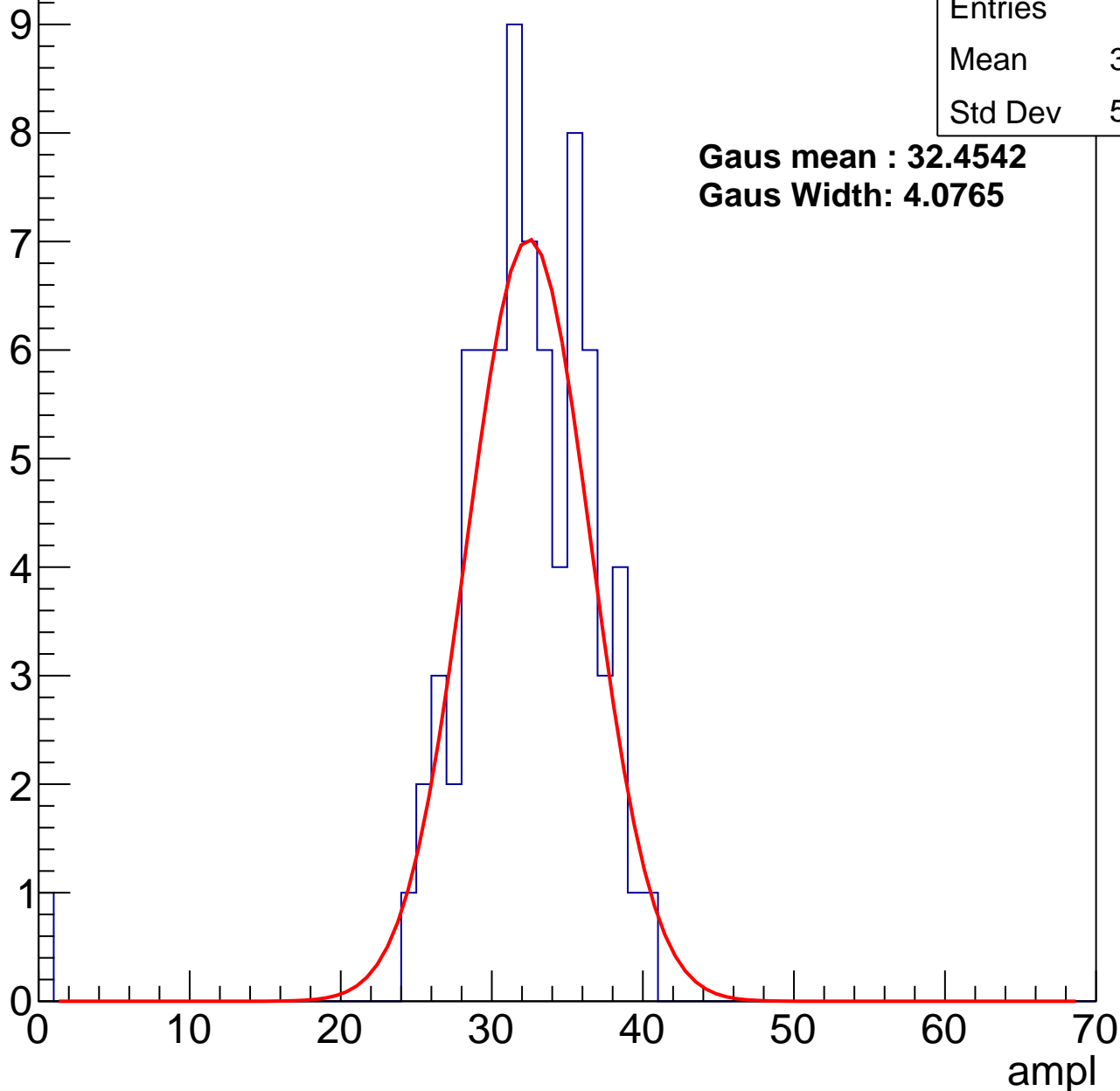
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	76
Mean	31.62
Std Dev	5.178

**Gaus mean : 32.4542**

**Gaus Width: 4.0765**



# B1L101S, U22-ch40, adc1

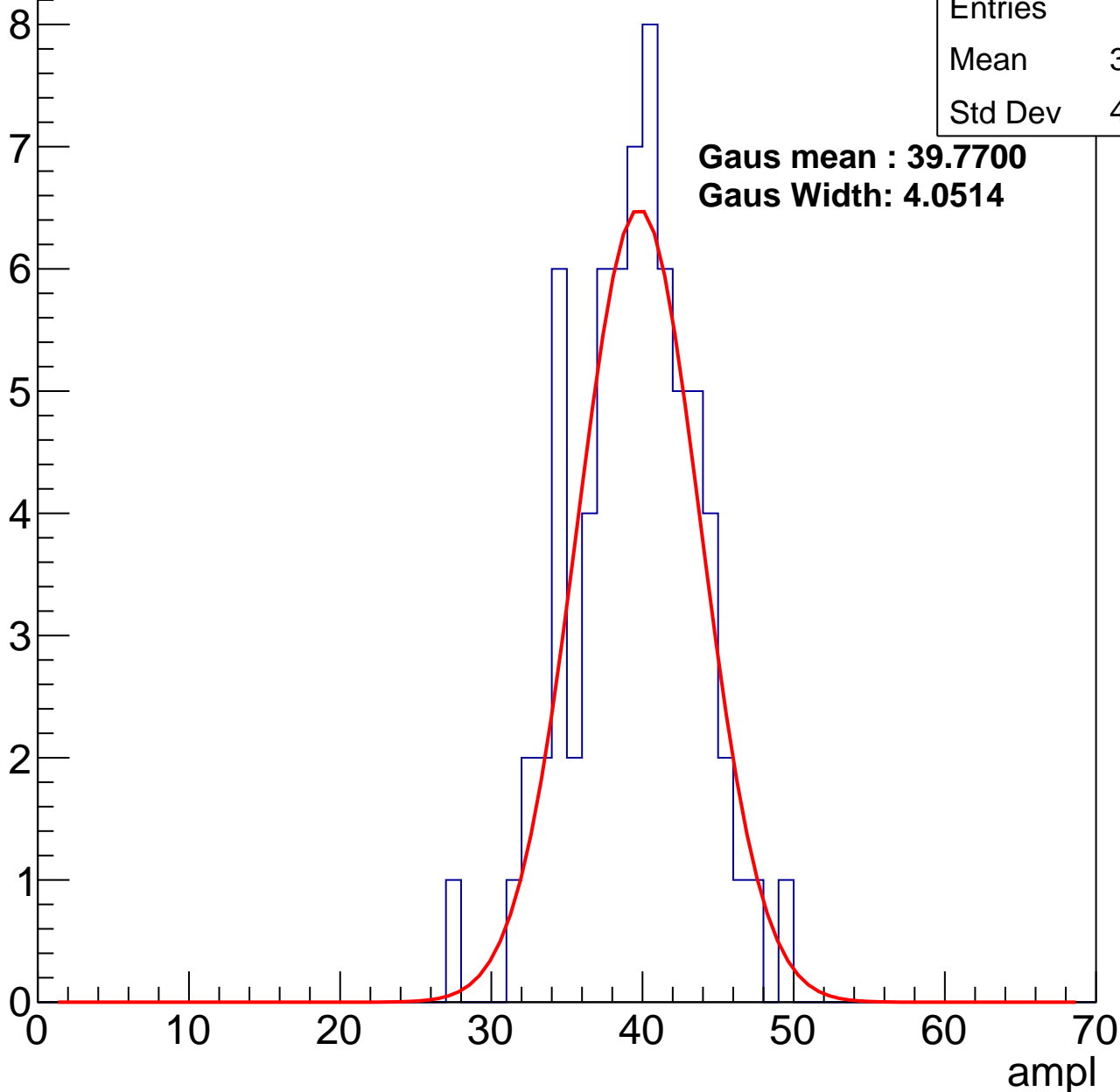
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	38.97
Std Dev	4.085

**Gaus mean : 39.7700**

**Gaus Width: 4.0514**



# B1L101S, U22-ch40, adc2

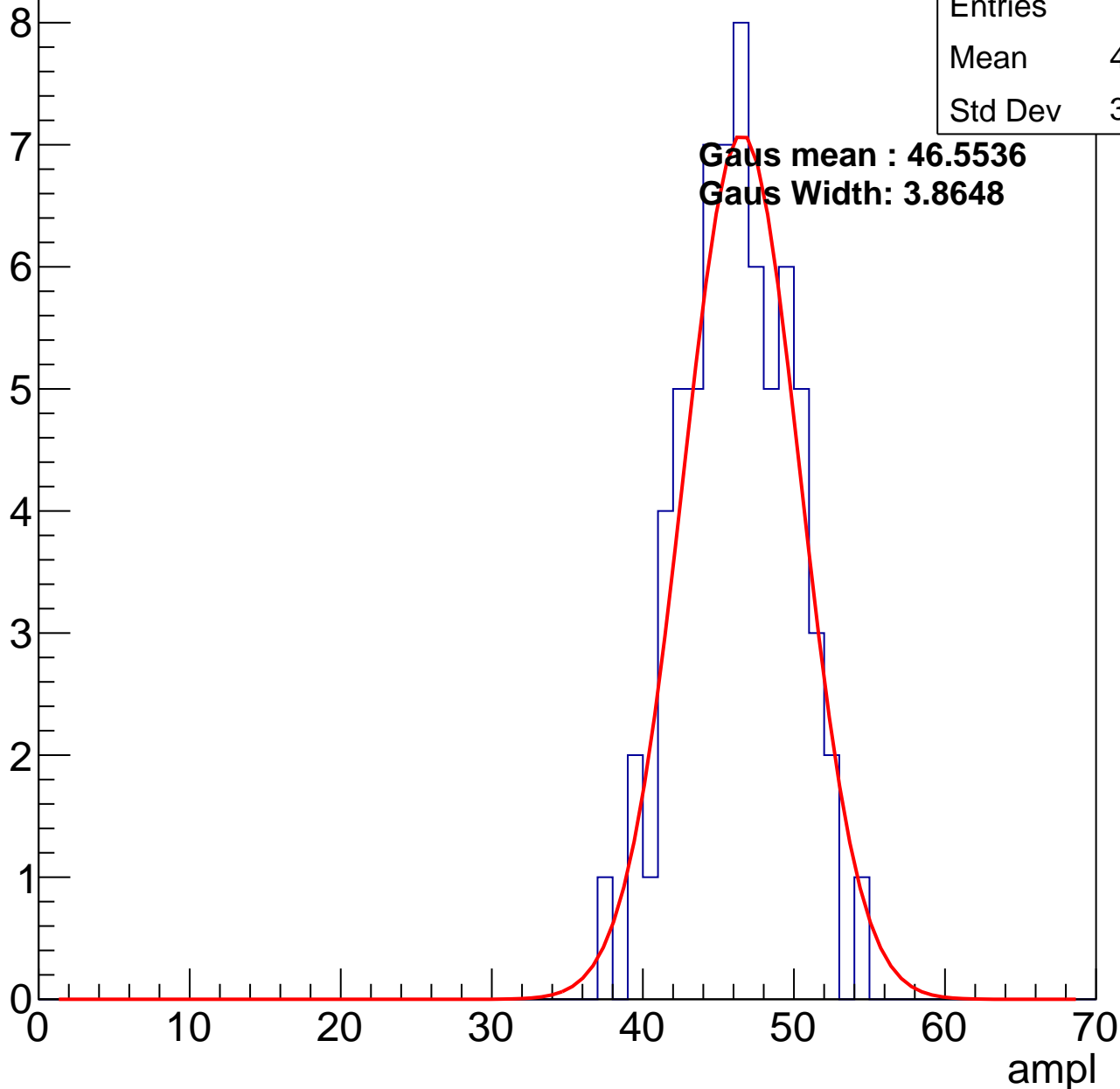
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	45.76
Std Dev	3.519

**Gaus mean : 46.5536**

**Gaus Width: 3.8648**

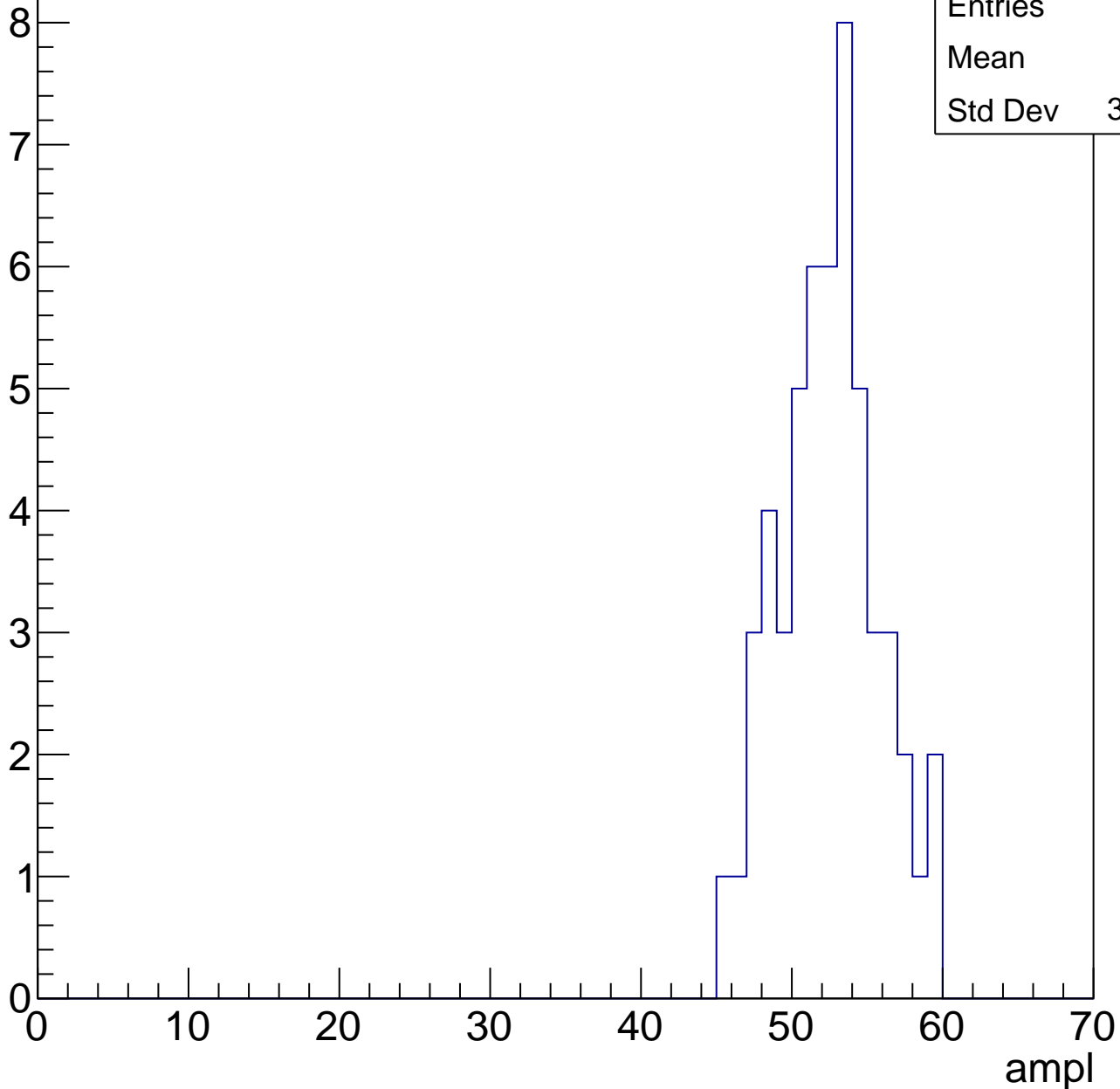


# B1L101S, U22-ch40, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	53
Mean	52
Std Dev	3.262

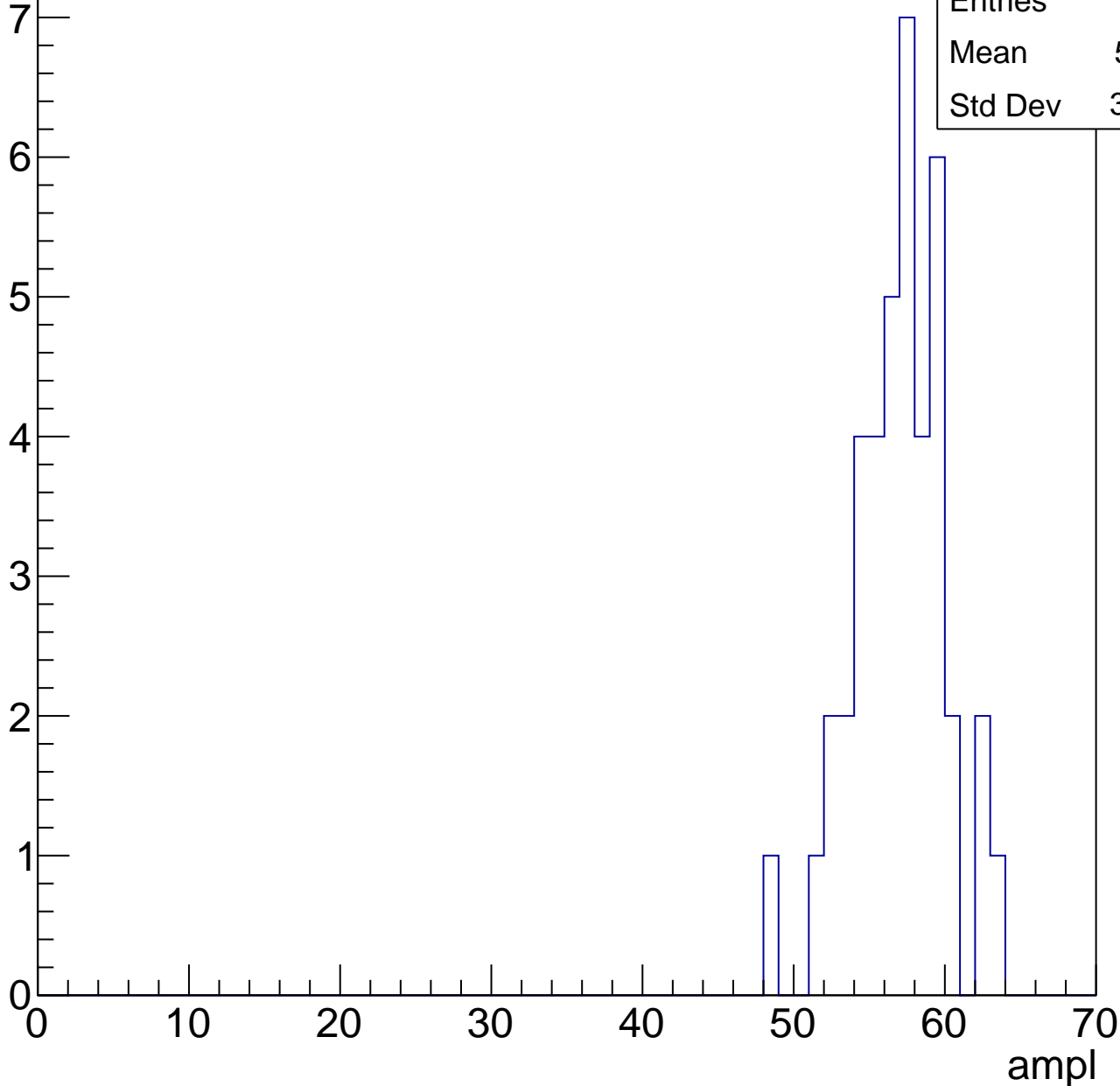


# B1L101S, U22-ch40, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

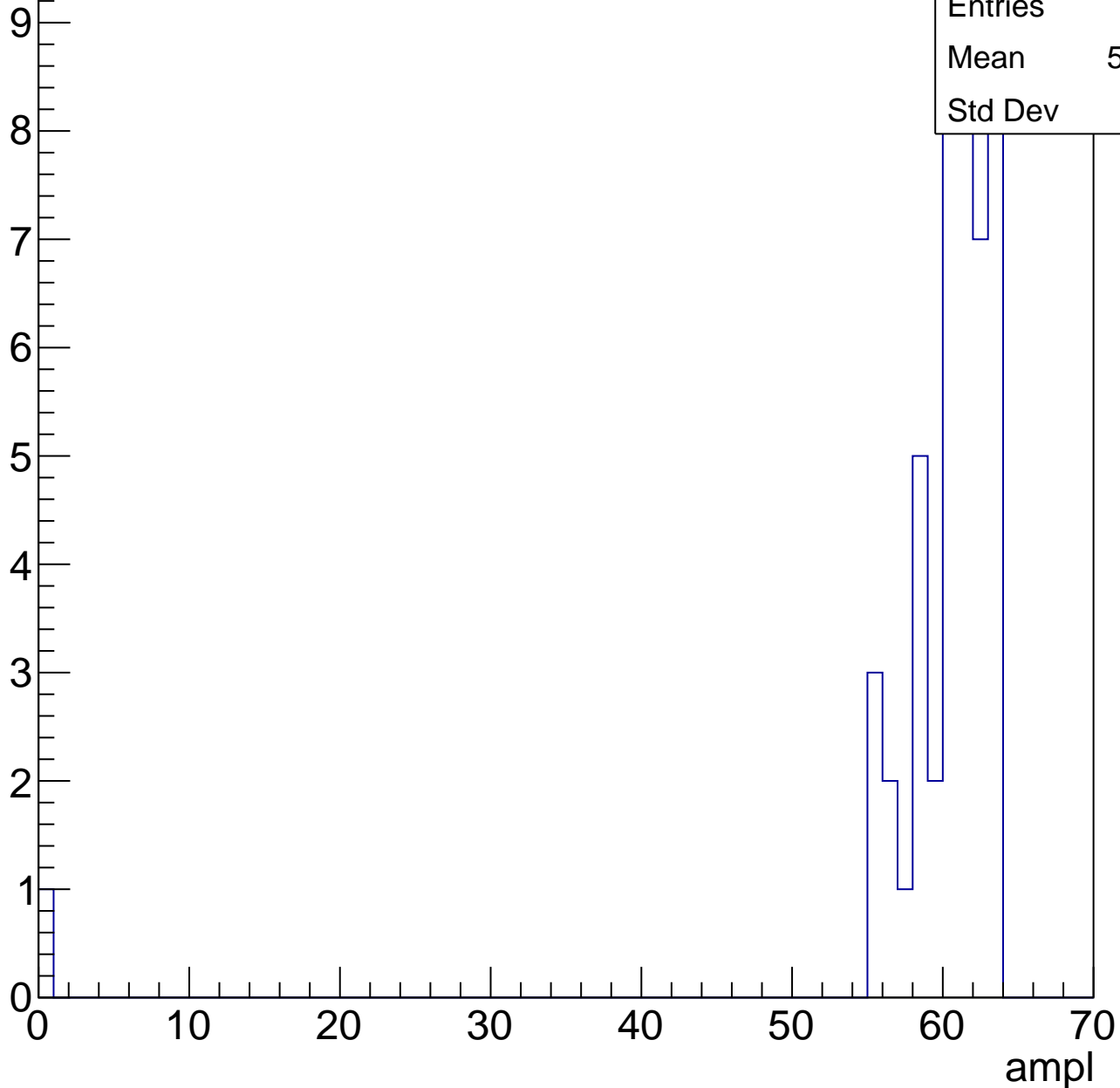
Entries	41
Mean	56.51
Std Dev	3.037



# B1L101S, U22-ch40, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U22-ch40, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U22-ch40, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U22-ch41, adc0

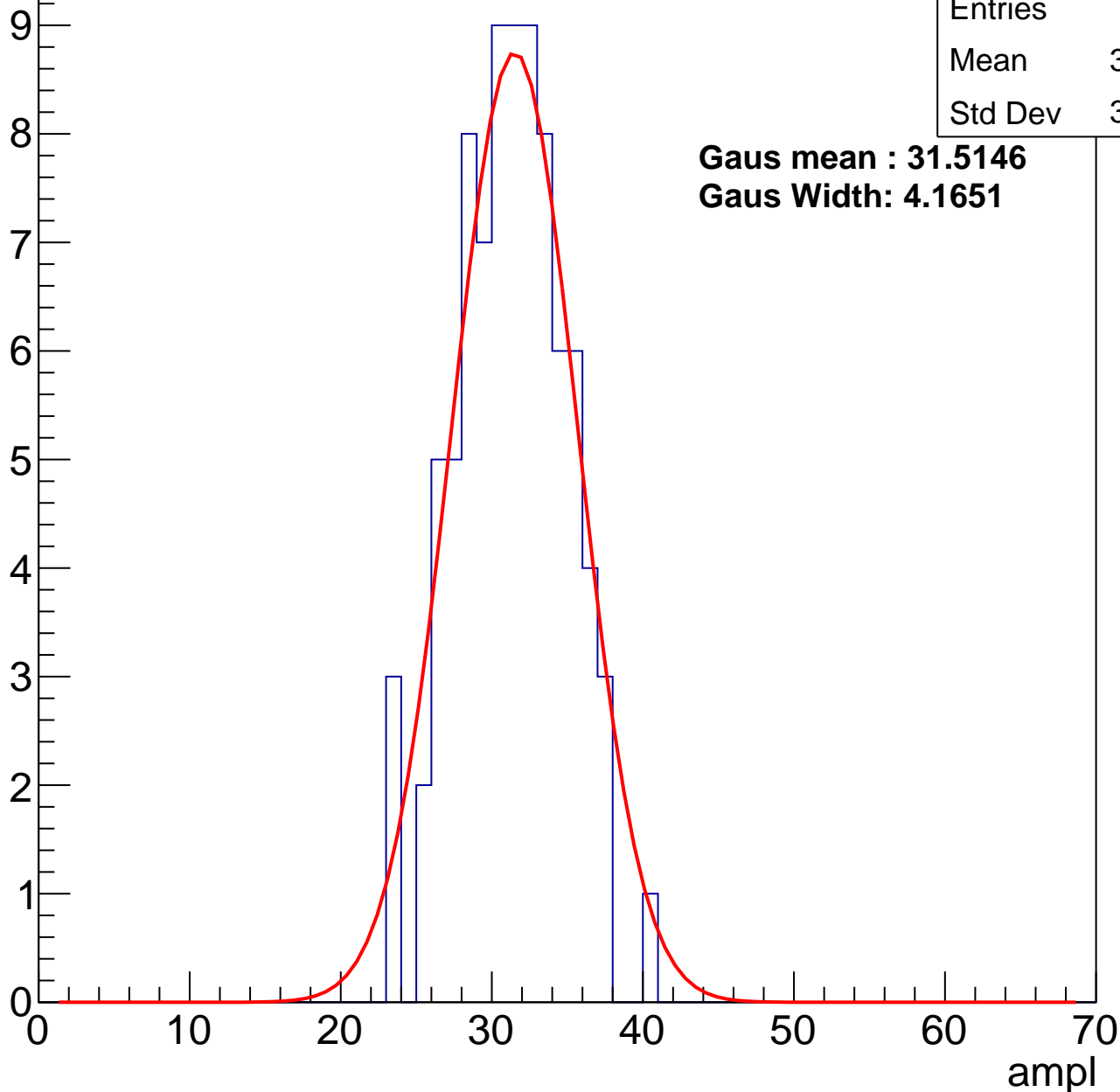
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	85
Mean	30.84
Std Dev	3.524

**Gaus mean : 31.5146**

**Gaus Width: 4.1651**



# B1L101S, U22-ch41, adc1

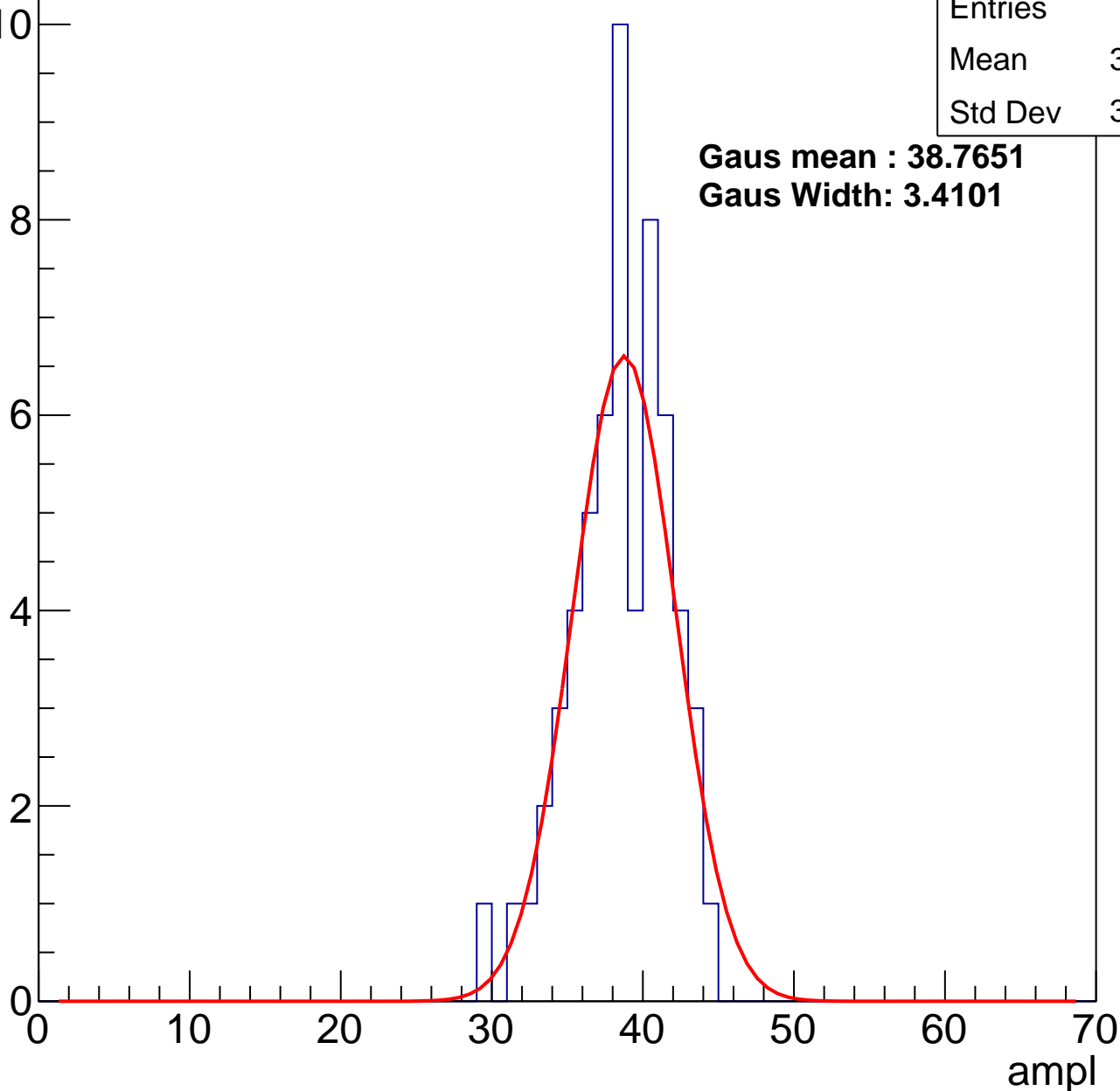
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	59
Mean	38.05
Std Dev	3.165

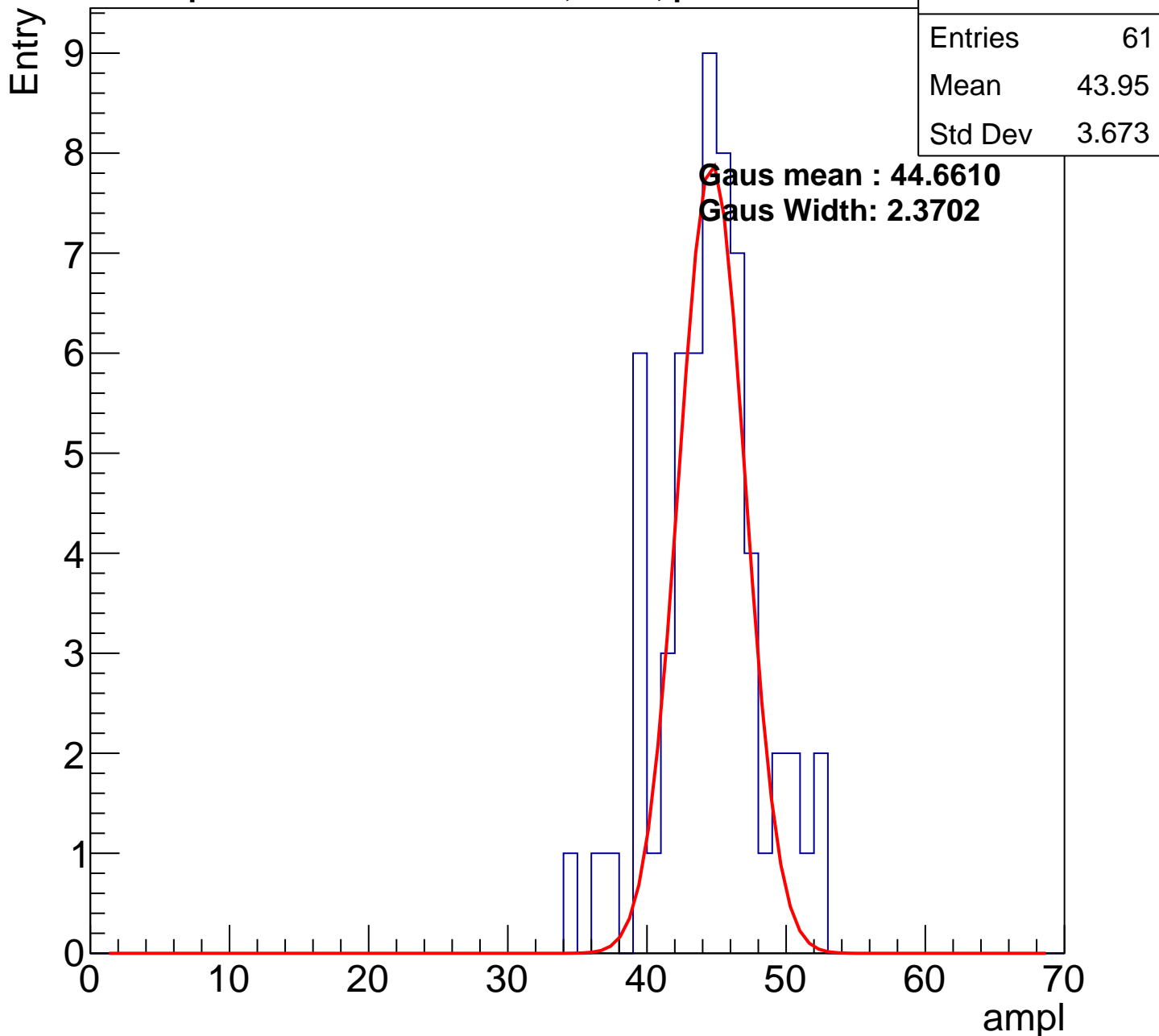
**Gaus mean : 38.7651**

**Gaus Width: 3.4101**



# B1L101S, U22-ch41, adc2

calib\_packv5\_042523\_0143.root, FC#0, port D2

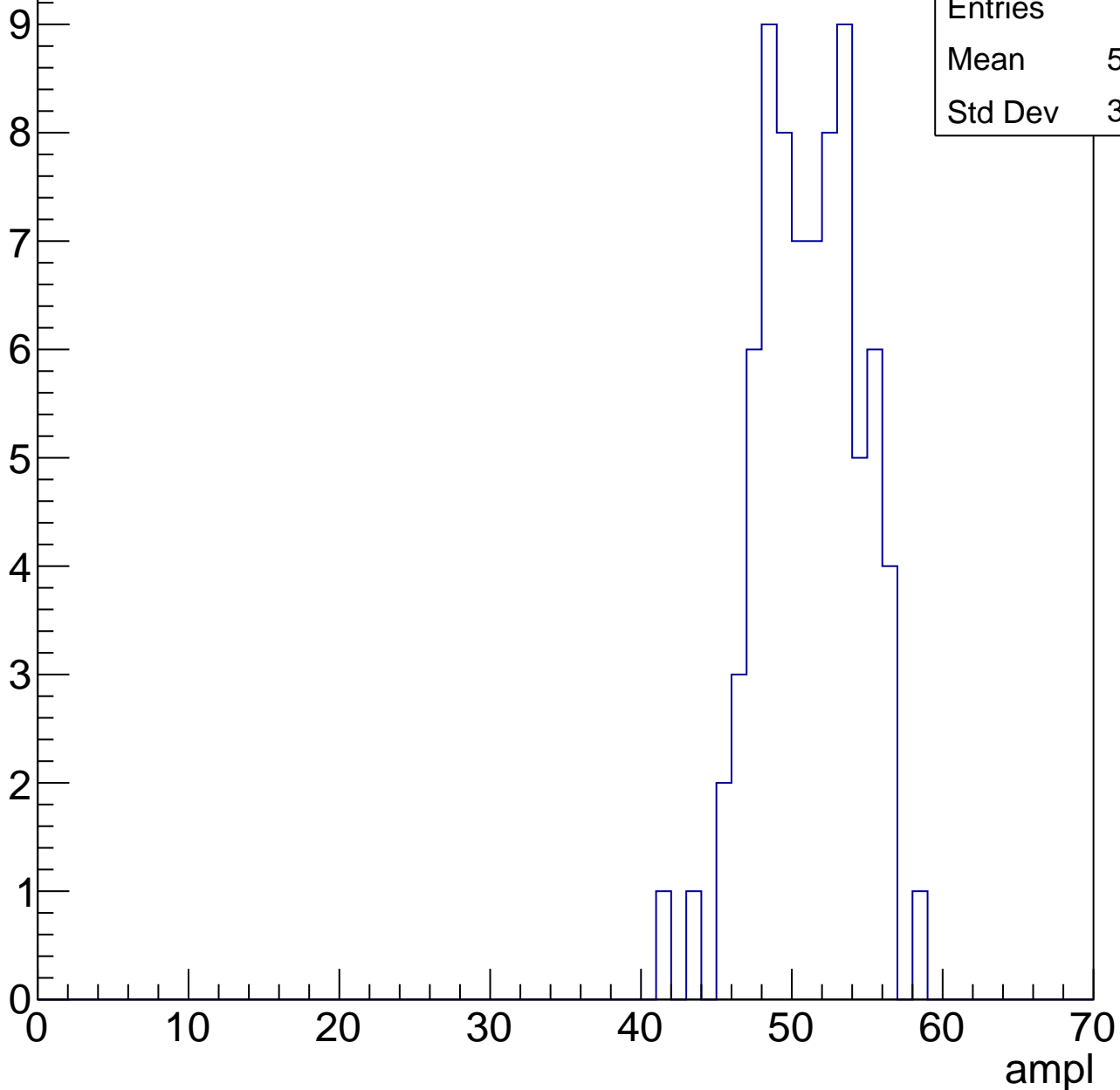


# B1L101S, U22-ch41, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	77
Mean	50.65
Std Dev	3.325

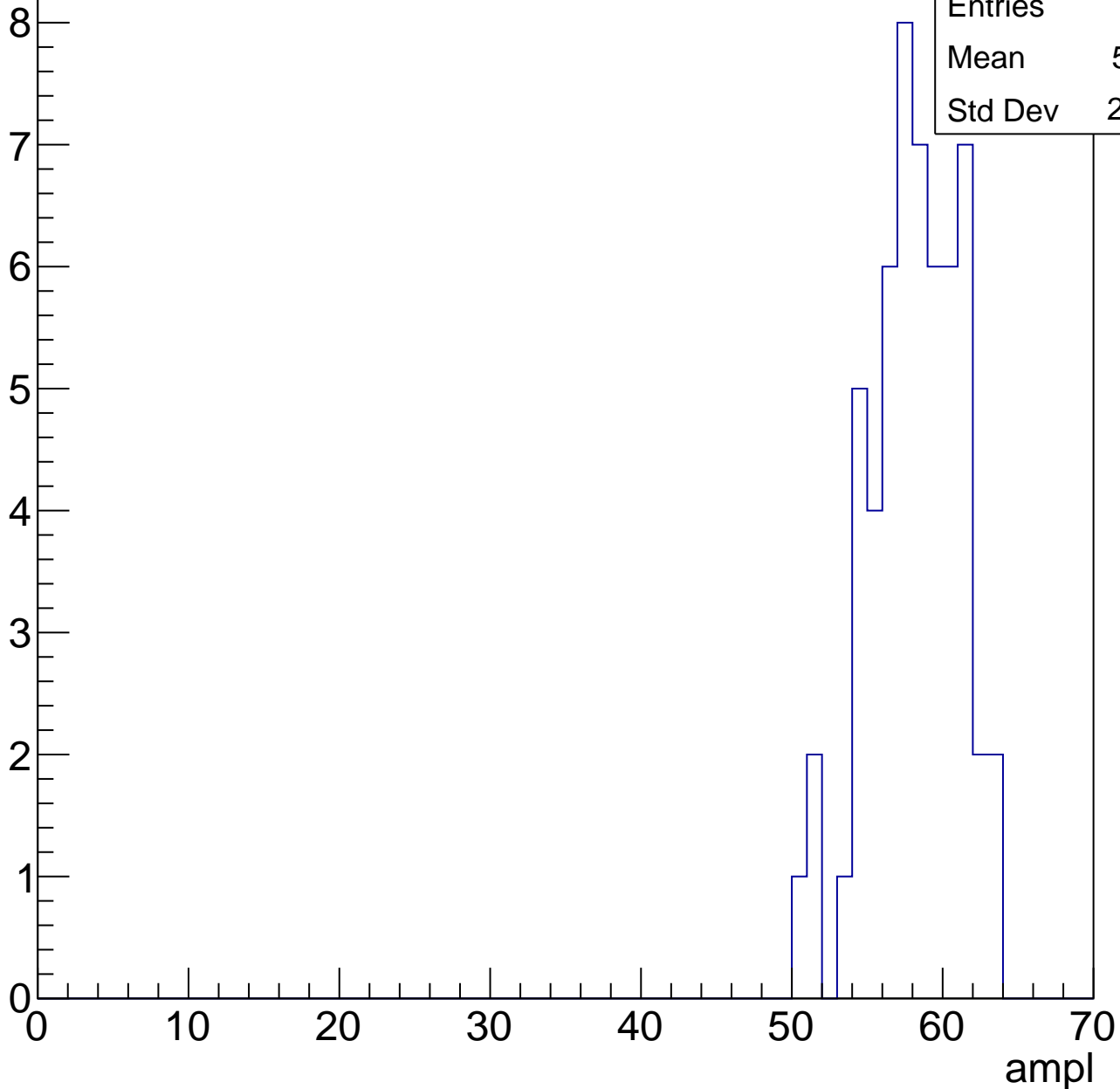


# B1L101S, U22-ch41, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	57
Mean	57.61
Std Dev	2.966

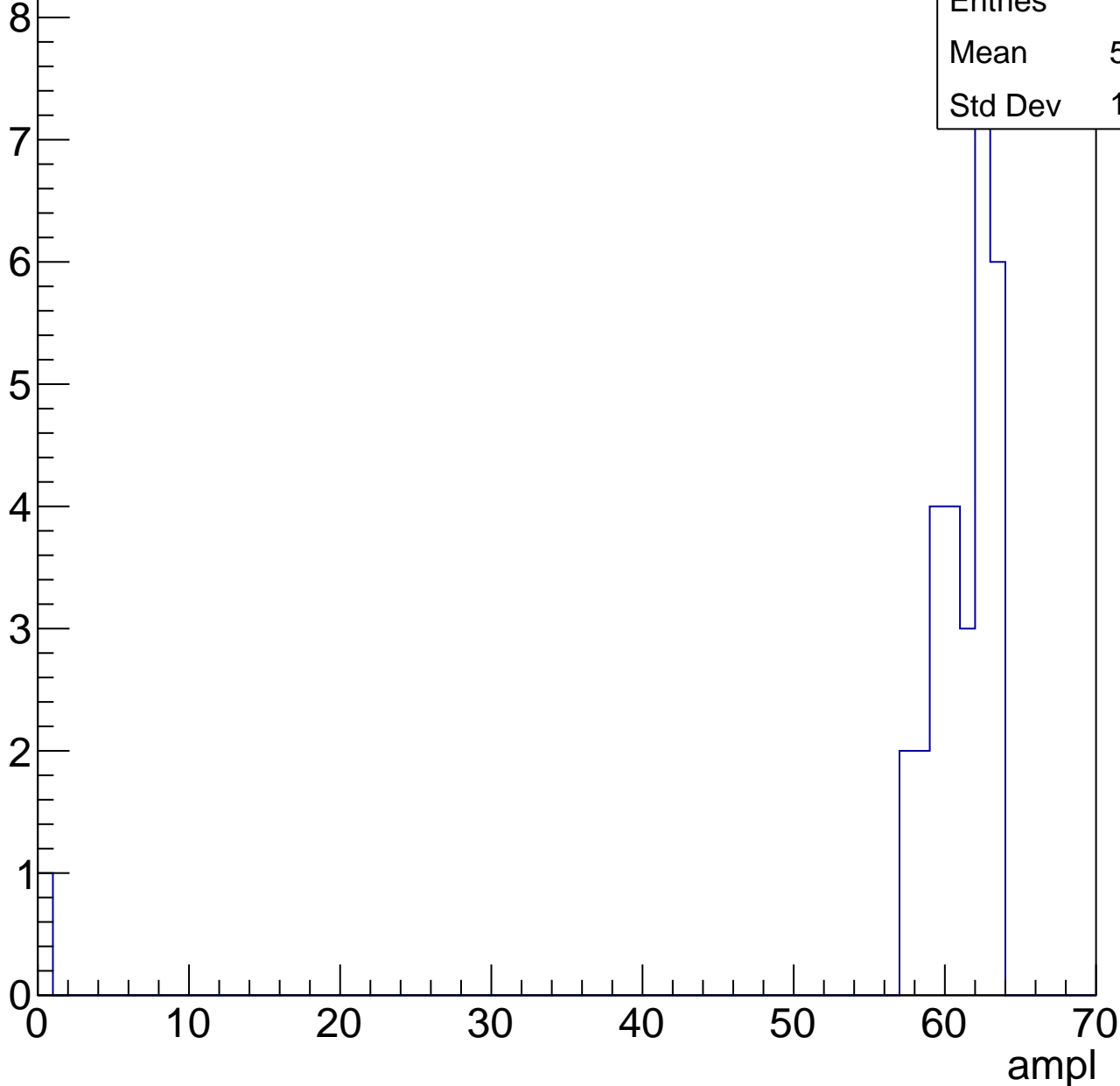


# B1L101S, U22-ch41, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	30
Mean	58.77
Std Dev	11.07



# B1L101S, U22-ch41, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	2
Mean	63
Std Dev	0

0 10 20 30 40 50 60 70

ampl



# B1L101S, U22-ch41, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U22-ch42, adc0

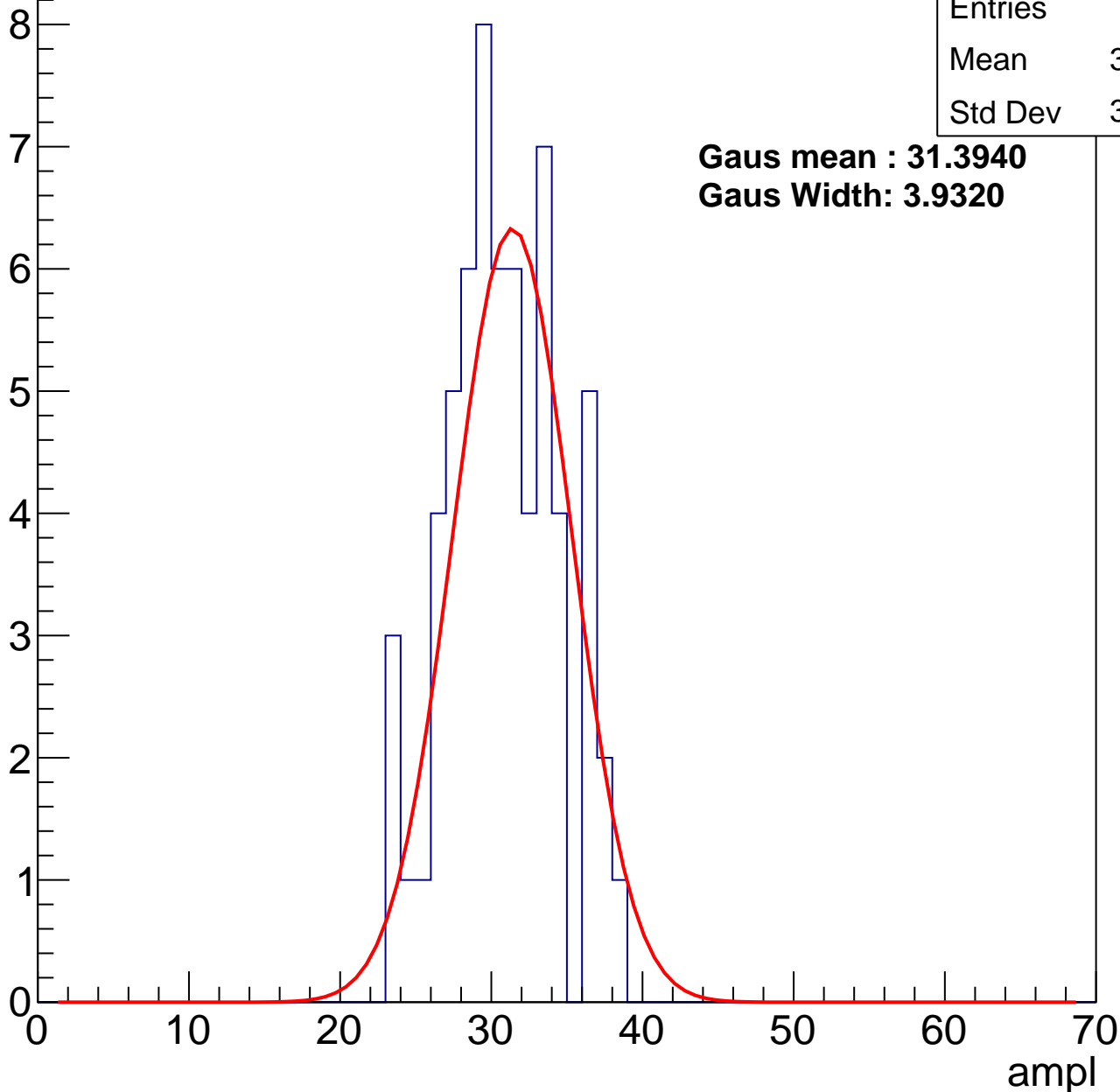
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	30.32
Std Dev	3.638

**Gaus mean : 31.3940**

**Gaus Width: 3.9320**



# B1L101S, U22-ch42, adc1

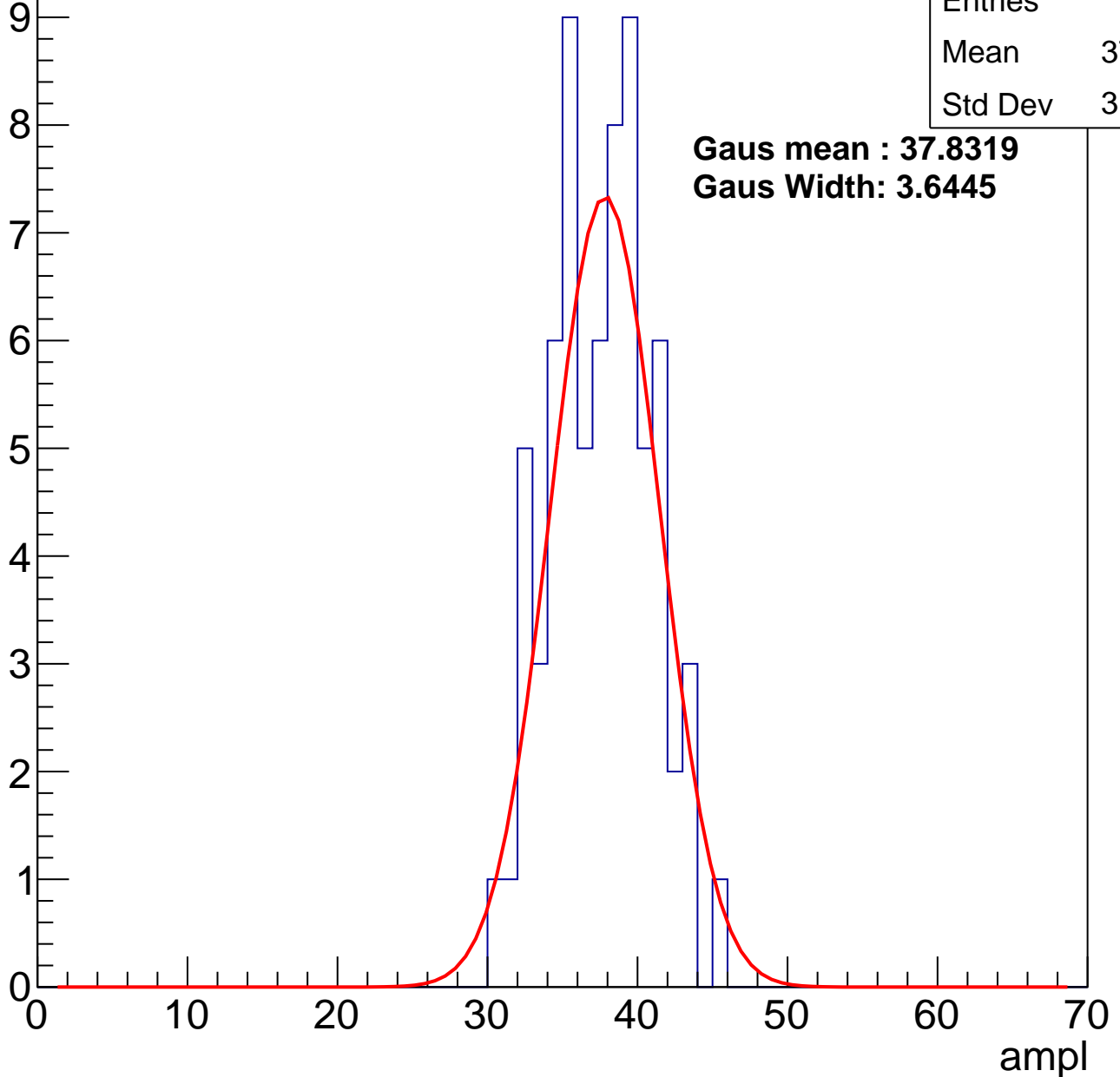
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	37.14
Std Dev	3.292

**Gaus mean : 37.8319**

**Gaus Width: 3.6445**



# B1L101S, U22-ch42, adc2

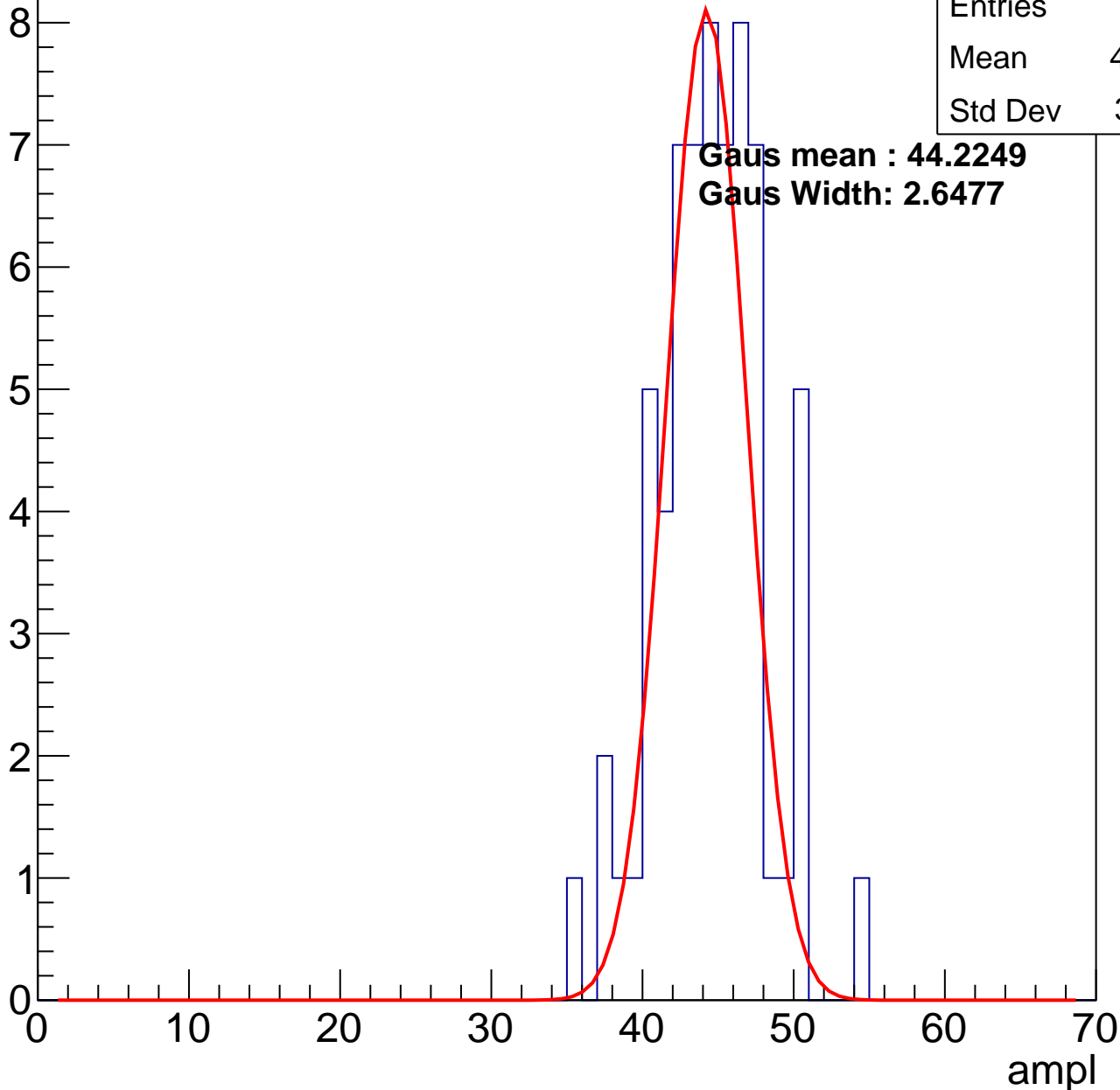
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	66
Mean	44.09
Std Dev	3.511

**Gaus mean : 44.2249**

**Gaus Width: 2.6477**



# B1L101S, U22-ch42, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

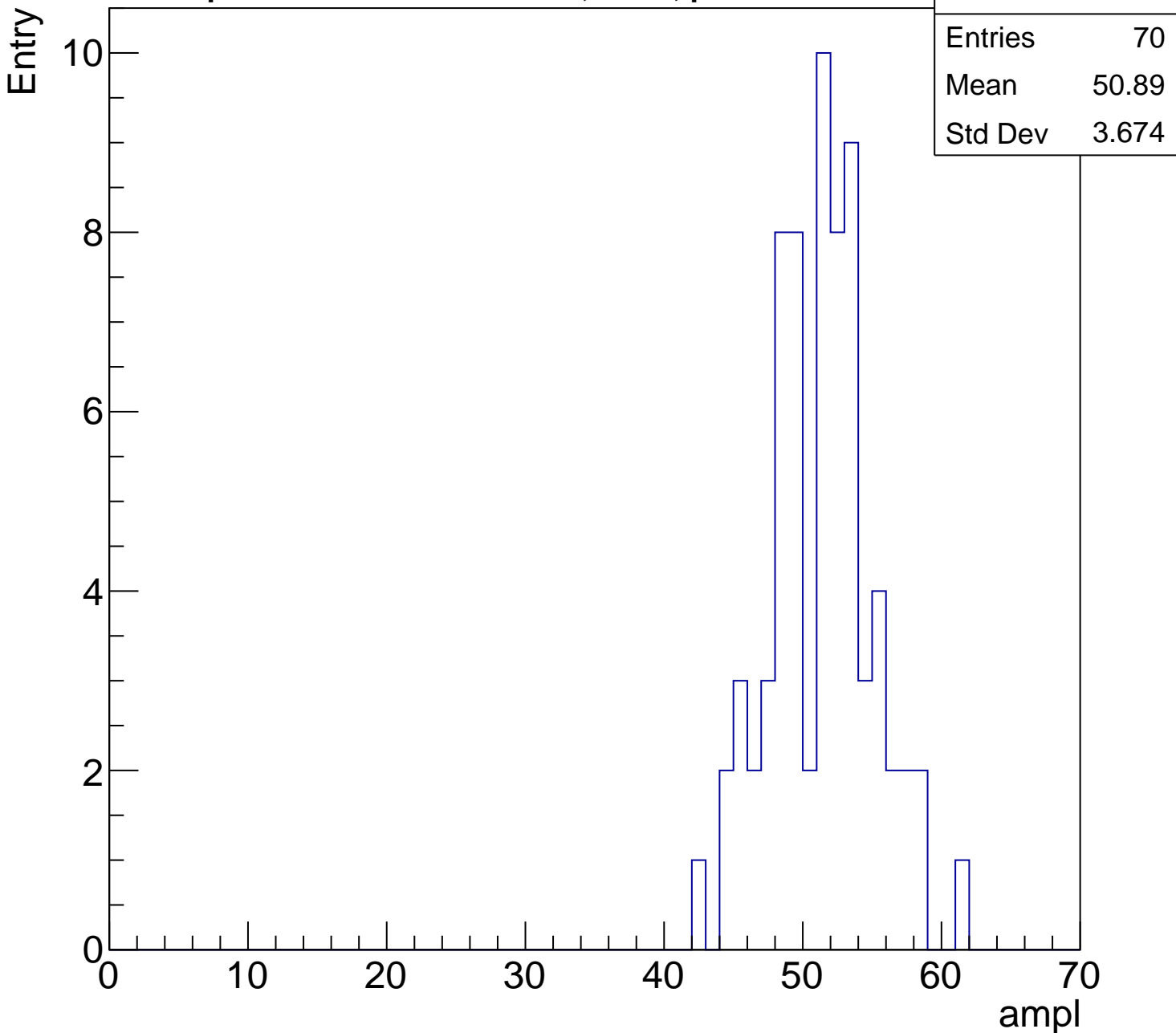
Entries	70
Mean	50.89
Std Dev	3.674

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B1L101S, U22-ch42, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

6

5

4

3

2

1

0

Entries 50

Mean 56.34

Std Dev 3.35

0

10

20

30

40

50

60

70

ampl

0

10

20

30

40

50

60

70

0

10

20

30

40

50

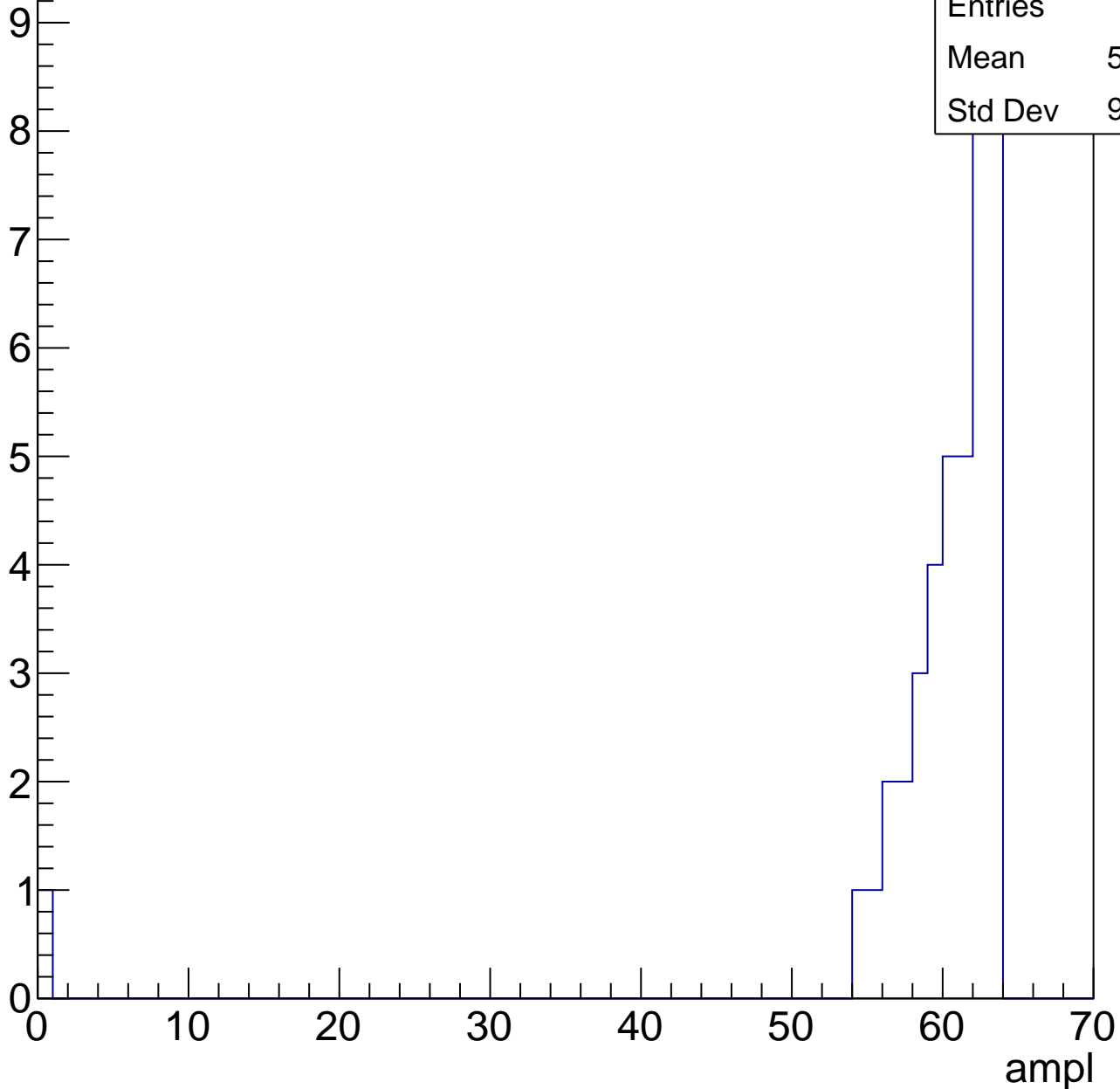
60

70

# B1L101S, U22-ch42, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

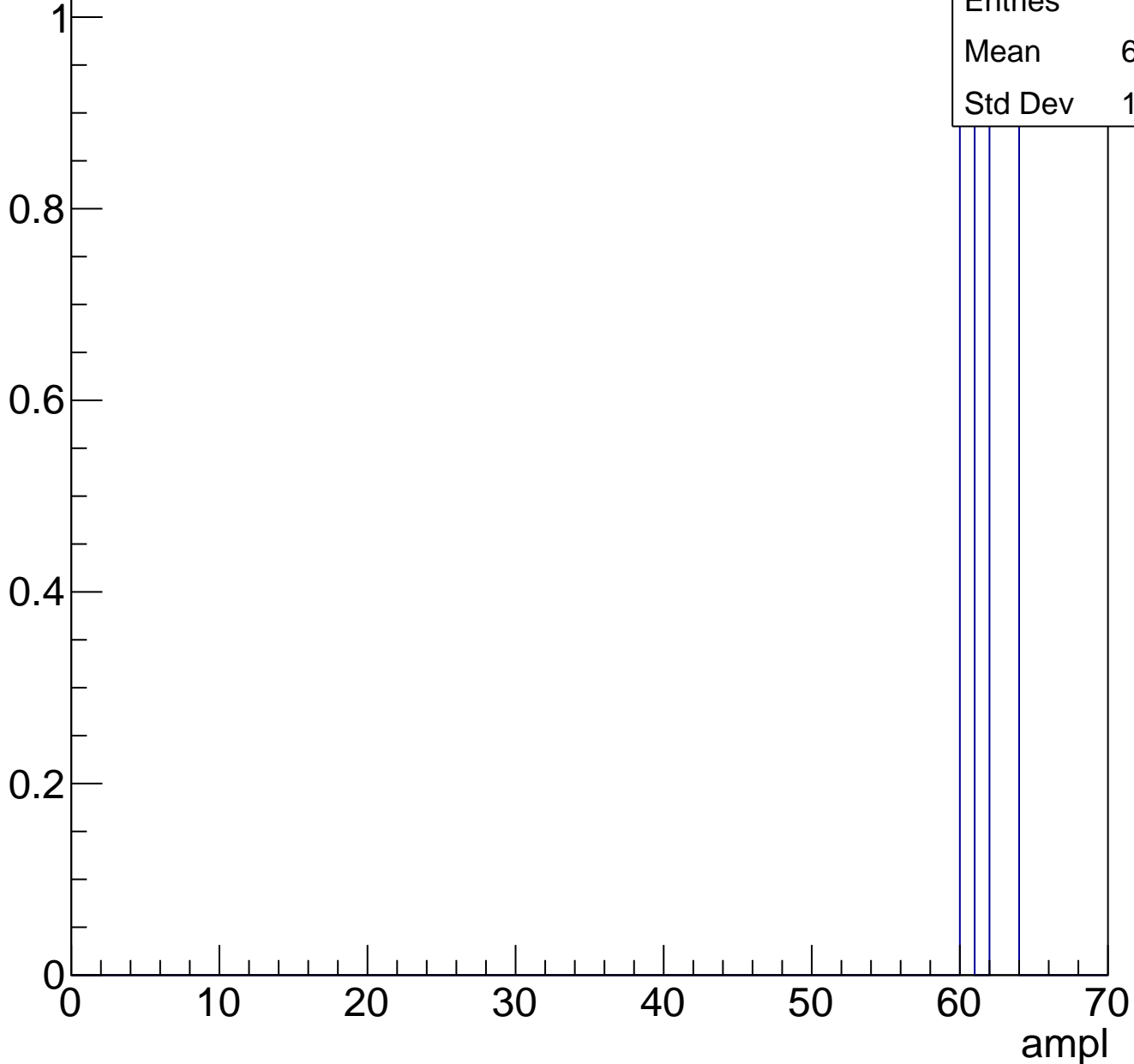
Entry



# B1L101S, U22-ch42, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U22-ch42, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U22-ch43, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	76
Mean	29.41
Std Dev	3.213

**Gaus mean : 29.9743**

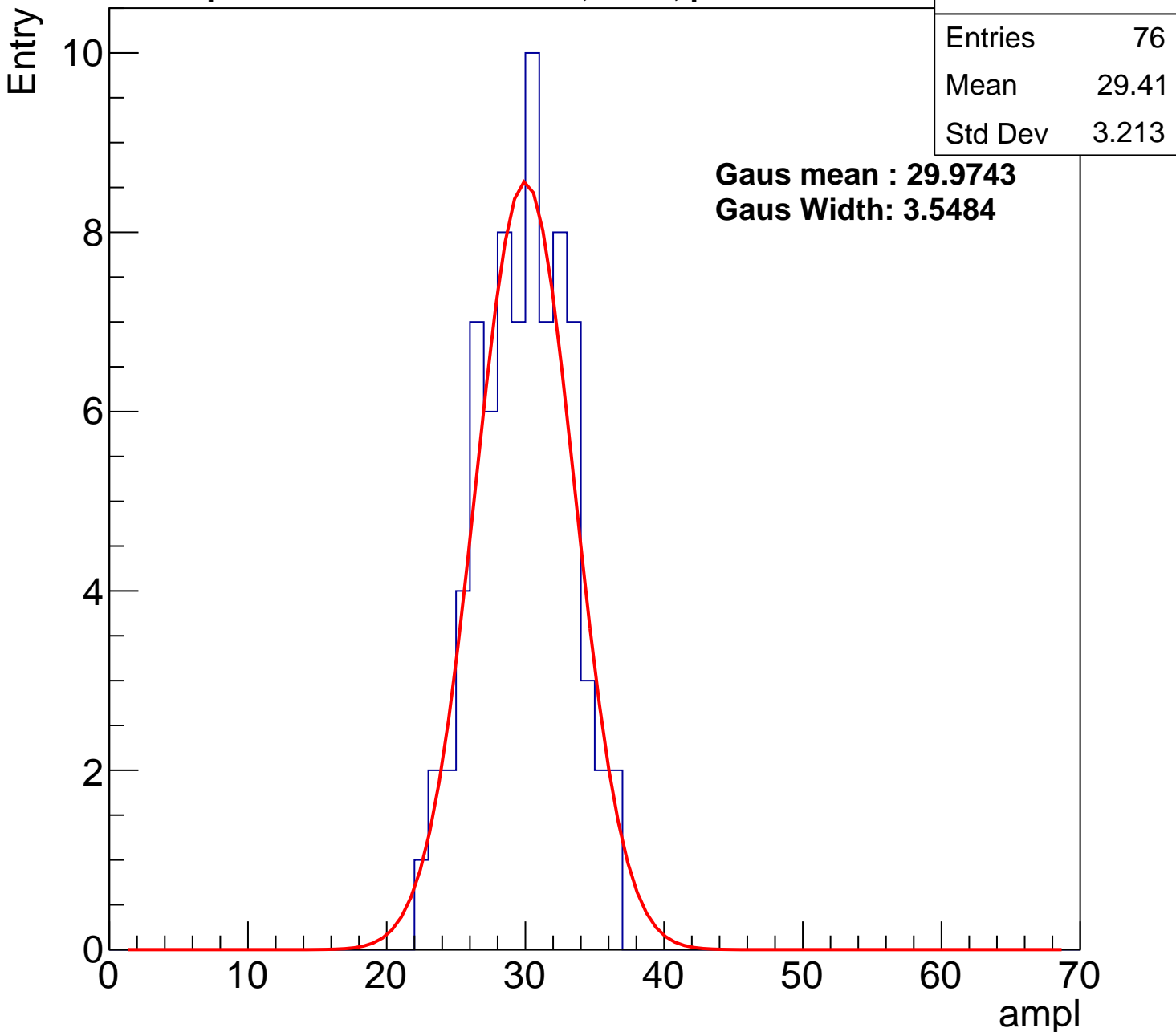
**Gaus Width: 3.5484**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U22-ch43, adc1

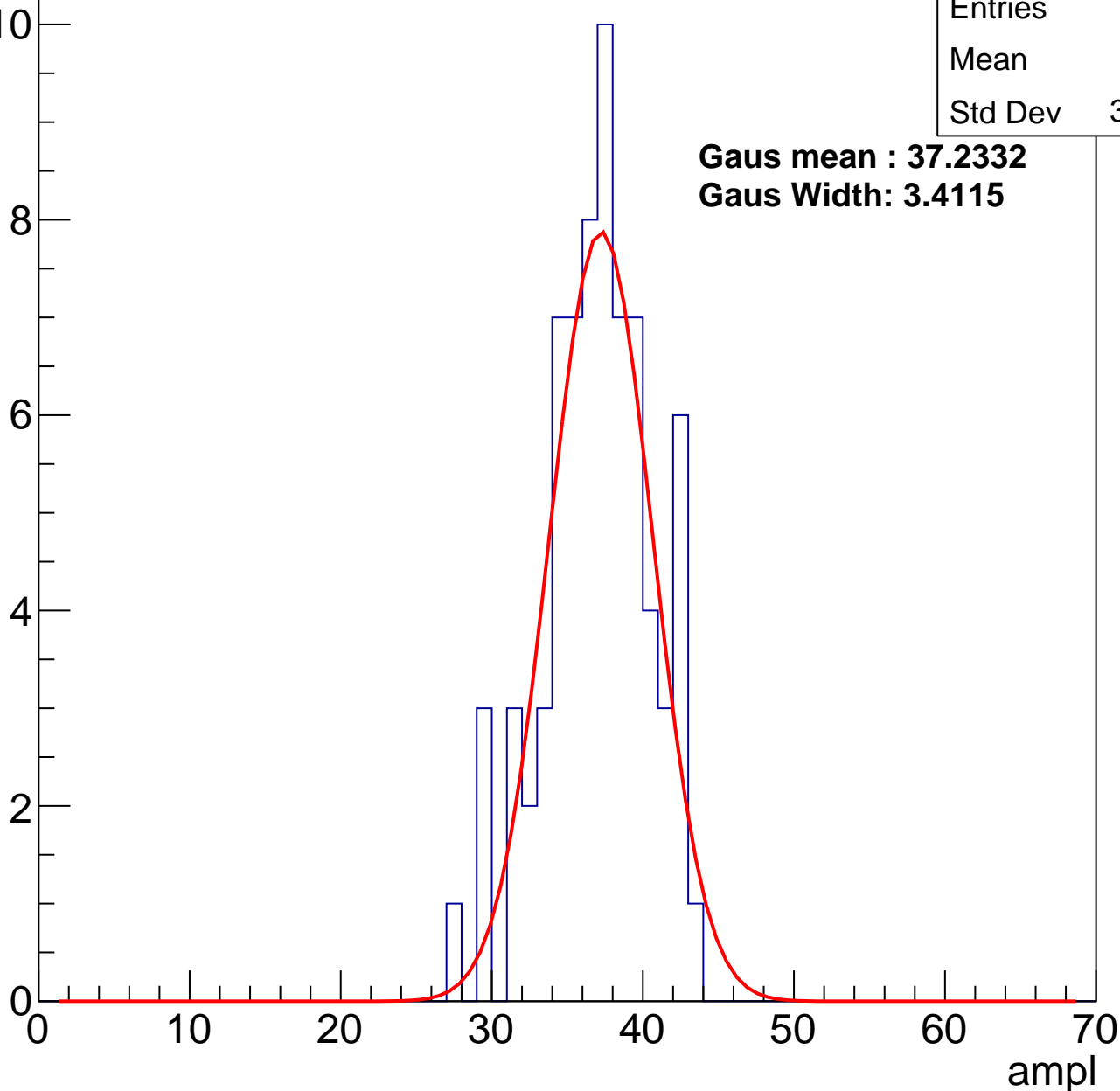
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	72
Mean	36.5
Std Dev	3.504

**Gaus mean : 37.2332**

**Gaus Width: 3.4115**



# B1L101S, U22-ch43, adc2

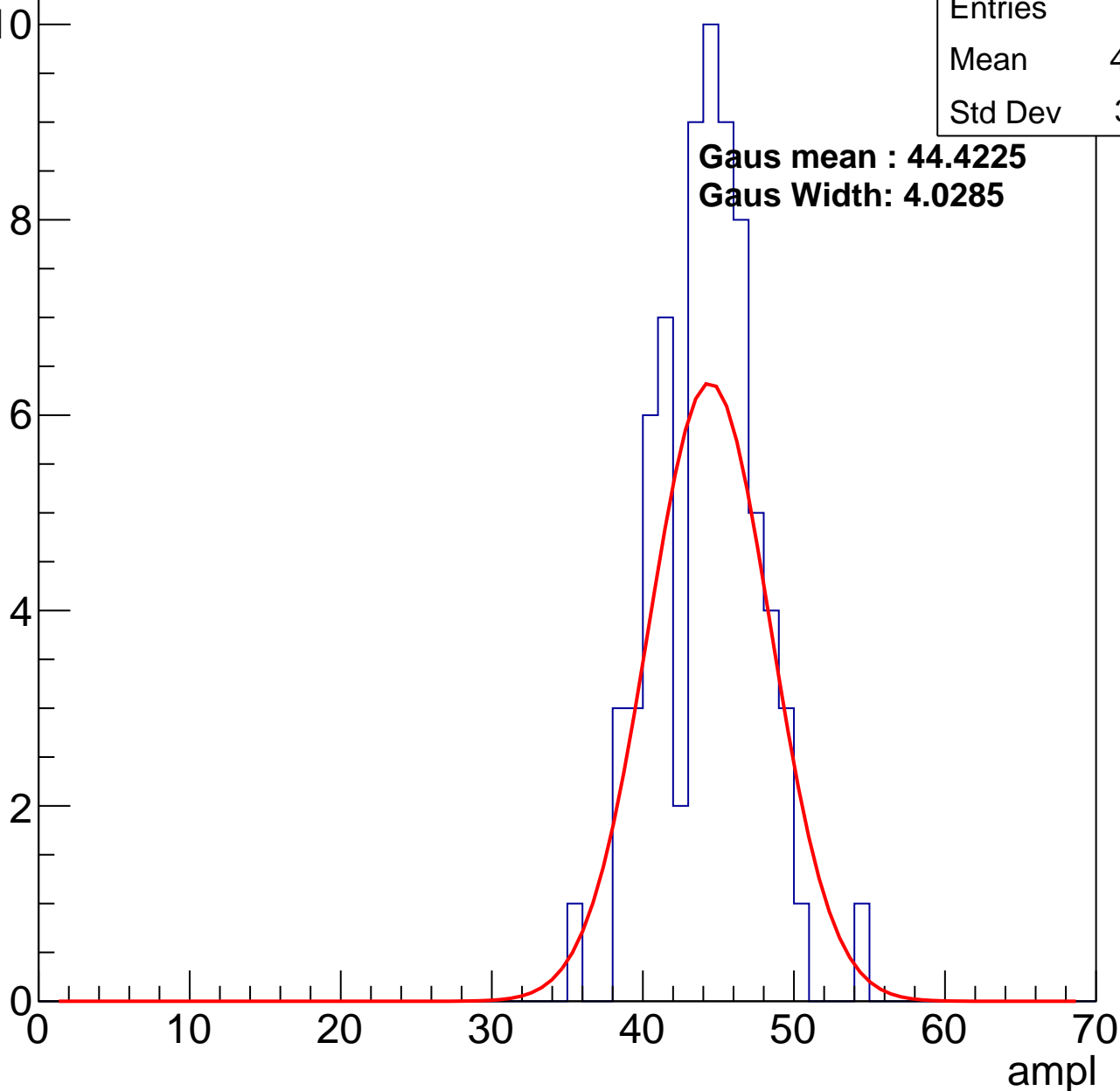
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	72
Mean	43.82
Std Dev	3.331

**Gaus mean : 44.4225**

**Gaus Width: 4.0285**

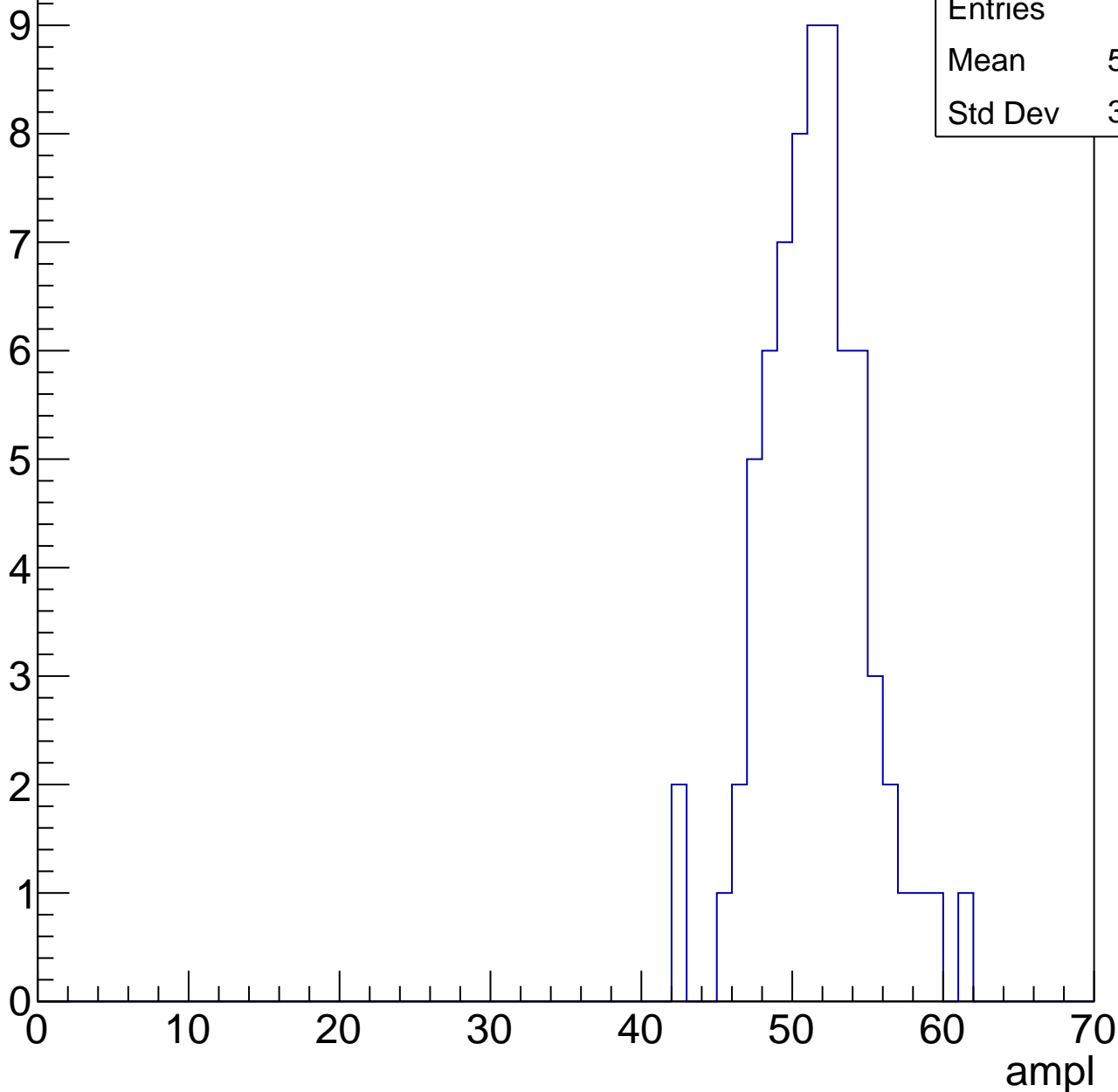


# B1L101S, U22-ch43, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	50.97
Std Dev	3.489

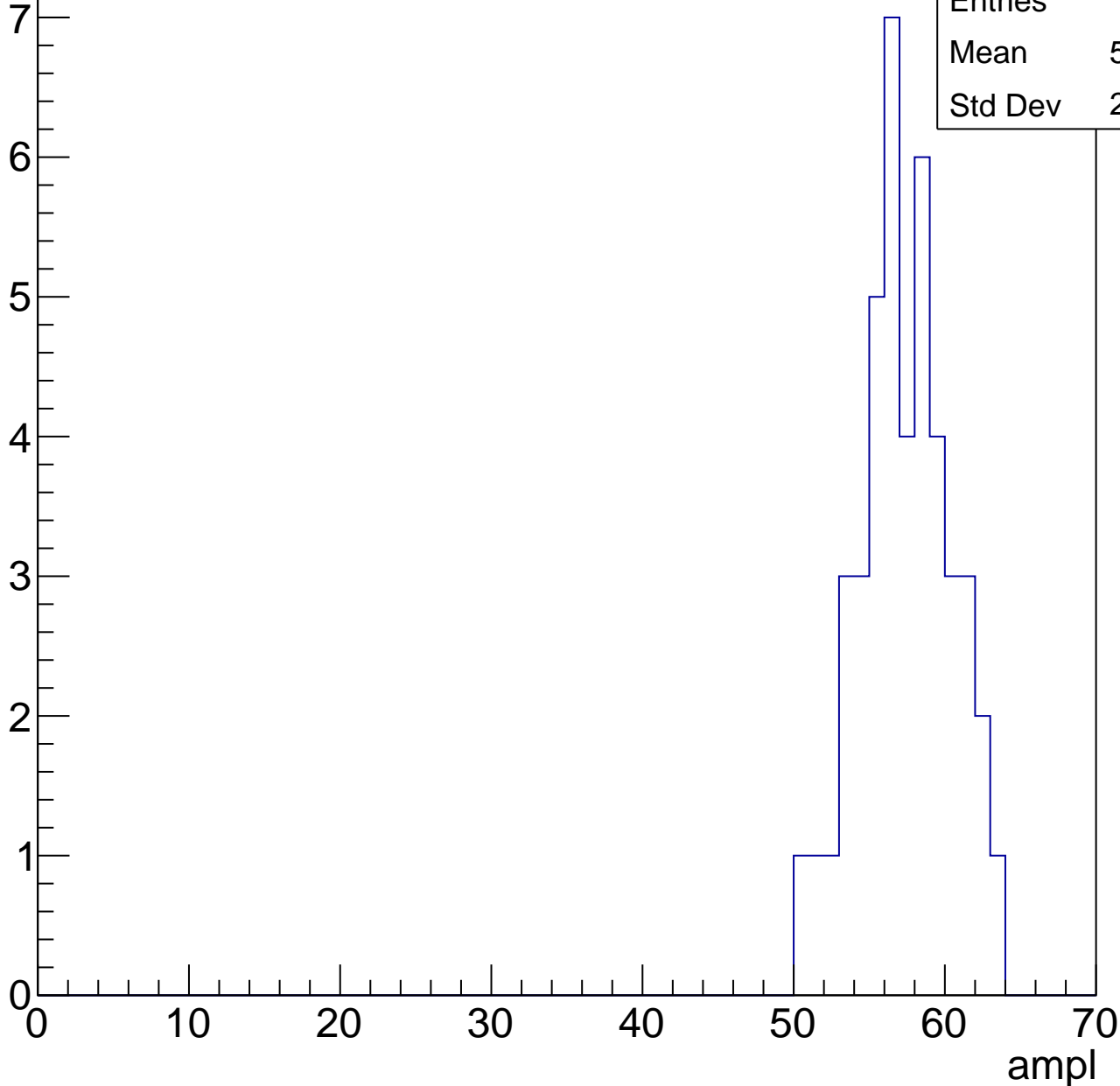


# B1L101S, U22-ch43, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	44
Mean	56.89
Std Dev	2.994



# B1L101S, U22-ch43, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

7

6

5

4

3

2

1

0

Entries	43
Mean	58.35
Std Dev	9.331

ampl

# B1L101S, U22-ch43, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

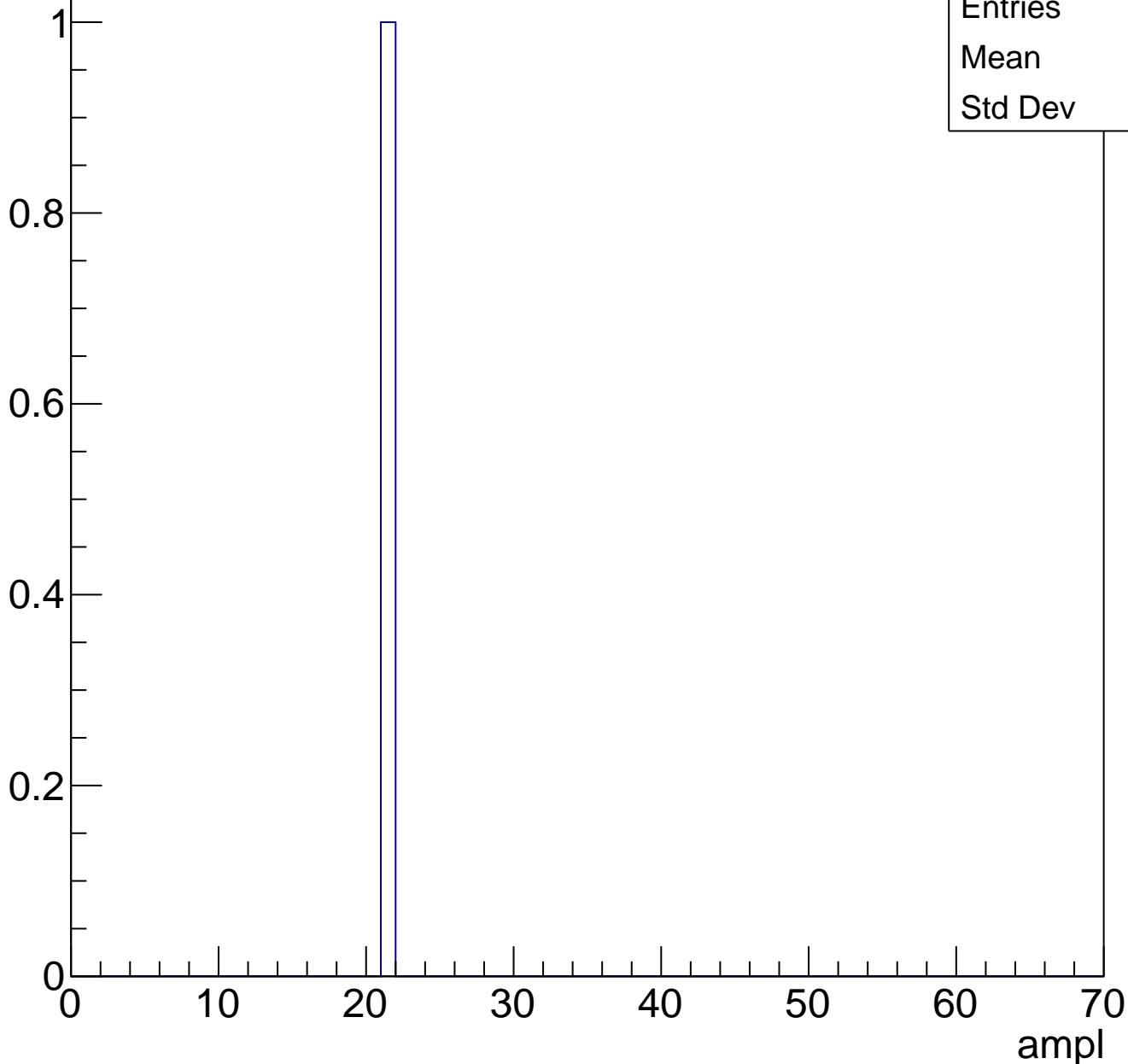




# B1L101S, U22-ch43, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U22-ch44, adc0

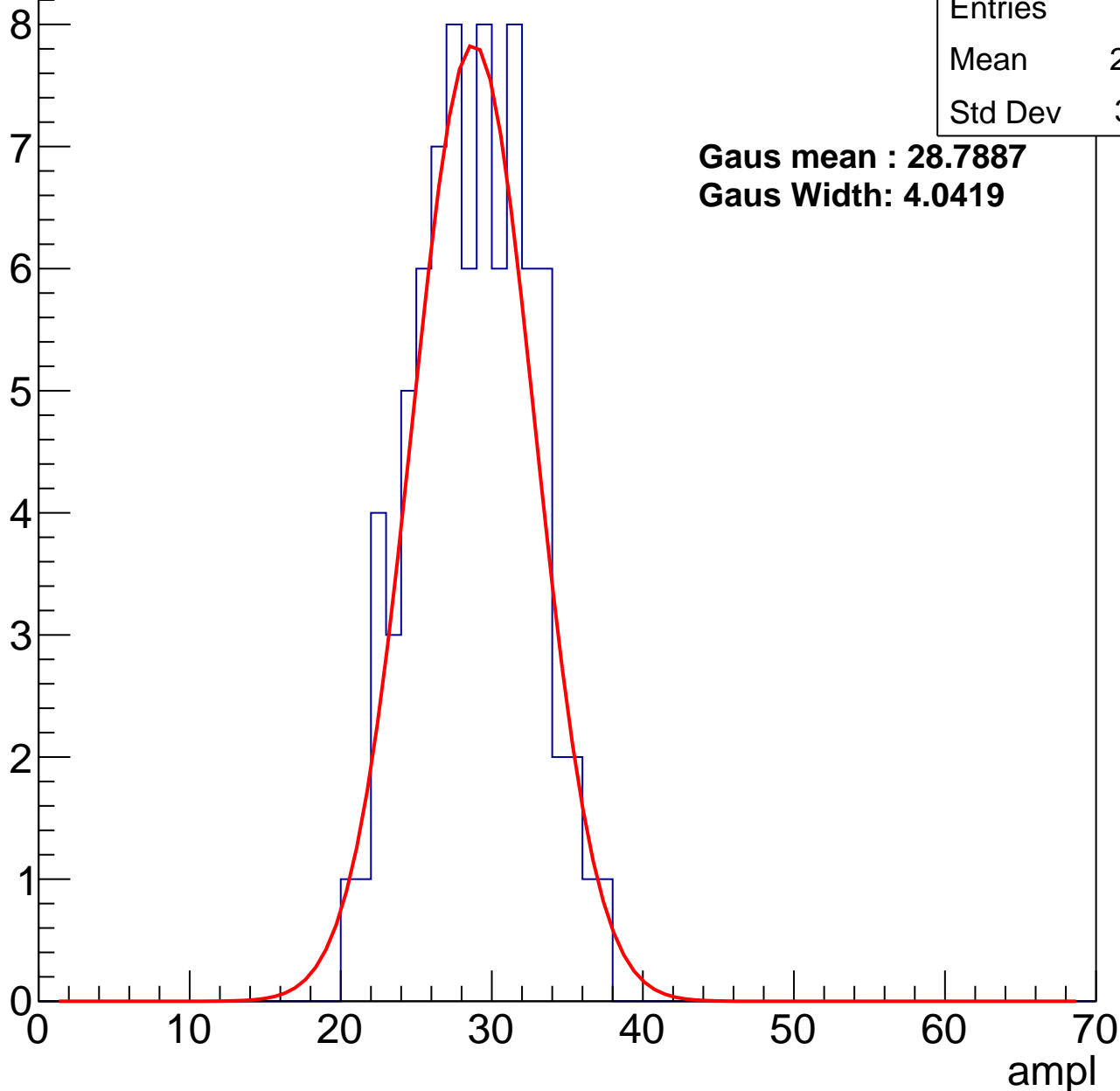
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	81
Mean	28.33
Std Dev	3.781

**Gaus mean : 28.7887**

**Gaus Width: 4.0419**



# B1L101S, U22-ch44, adc1

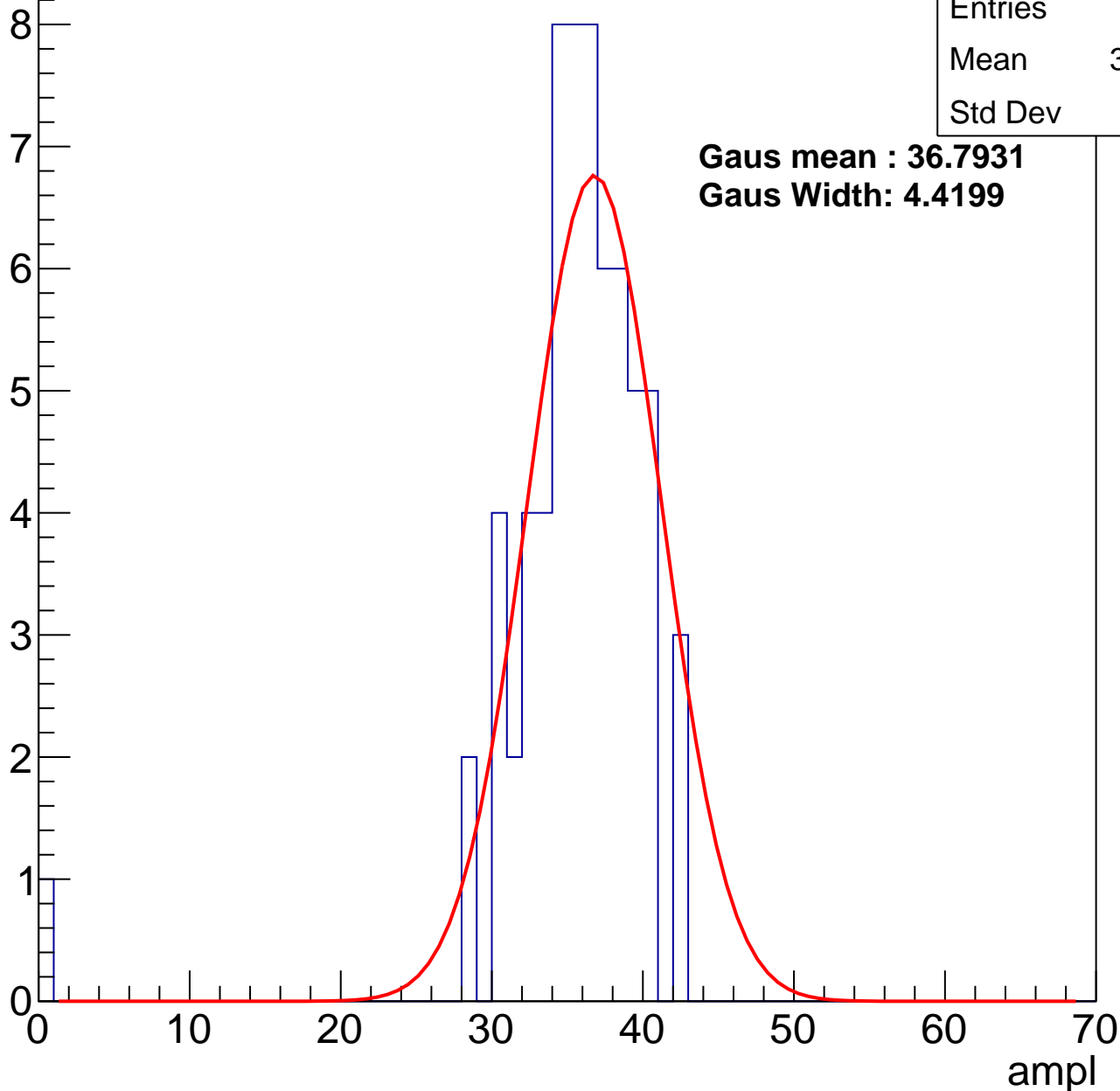
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	66
Mean	34.98
Std Dev	5.44

**Gaus mean : 36.7931**

**Gaus Width: 4.4199**



# B1L101S, U22-ch44, adc2

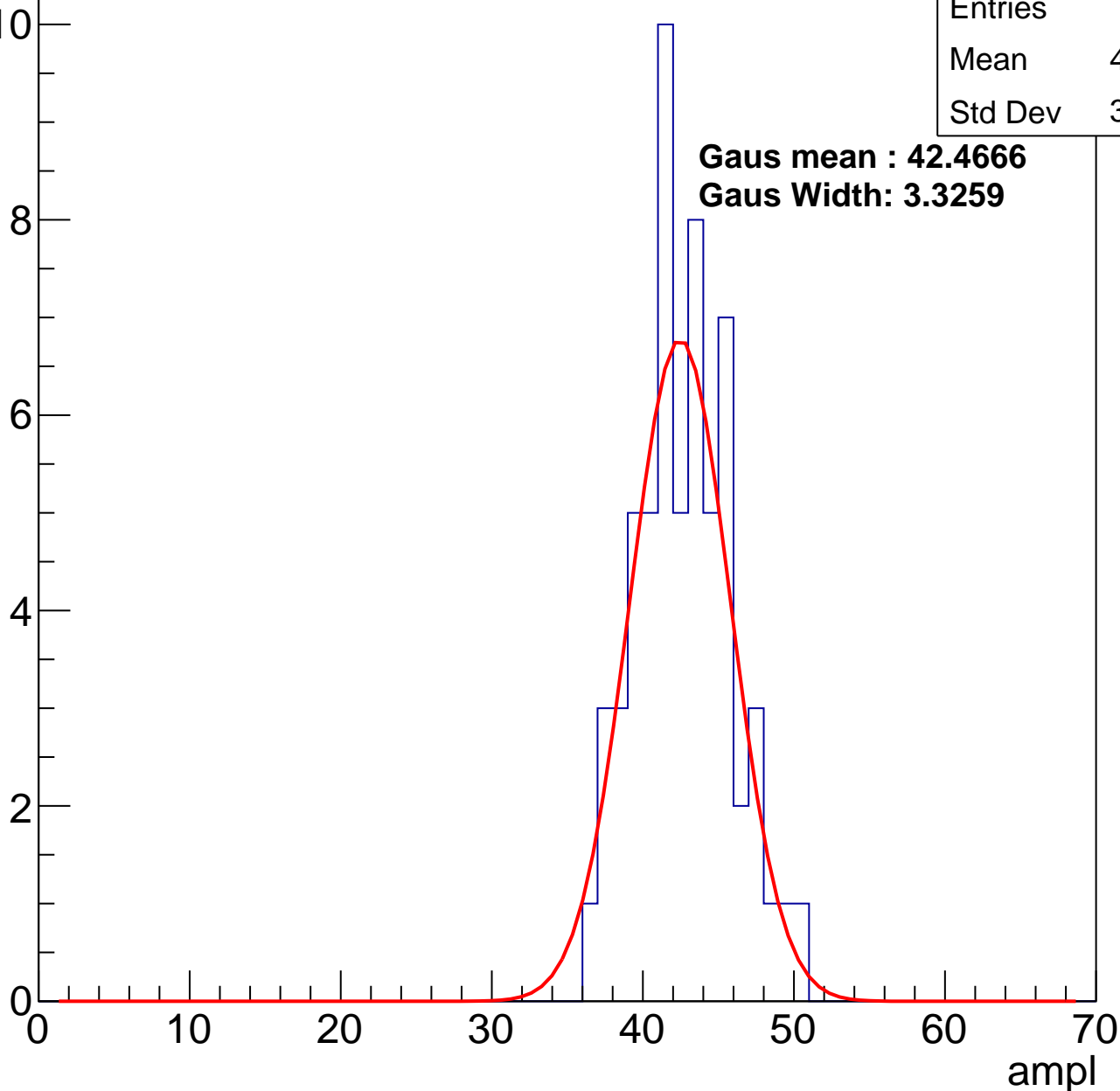
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	60
Mean	42.25
Std Dev	3.102

**Gaus mean : 42.4666**

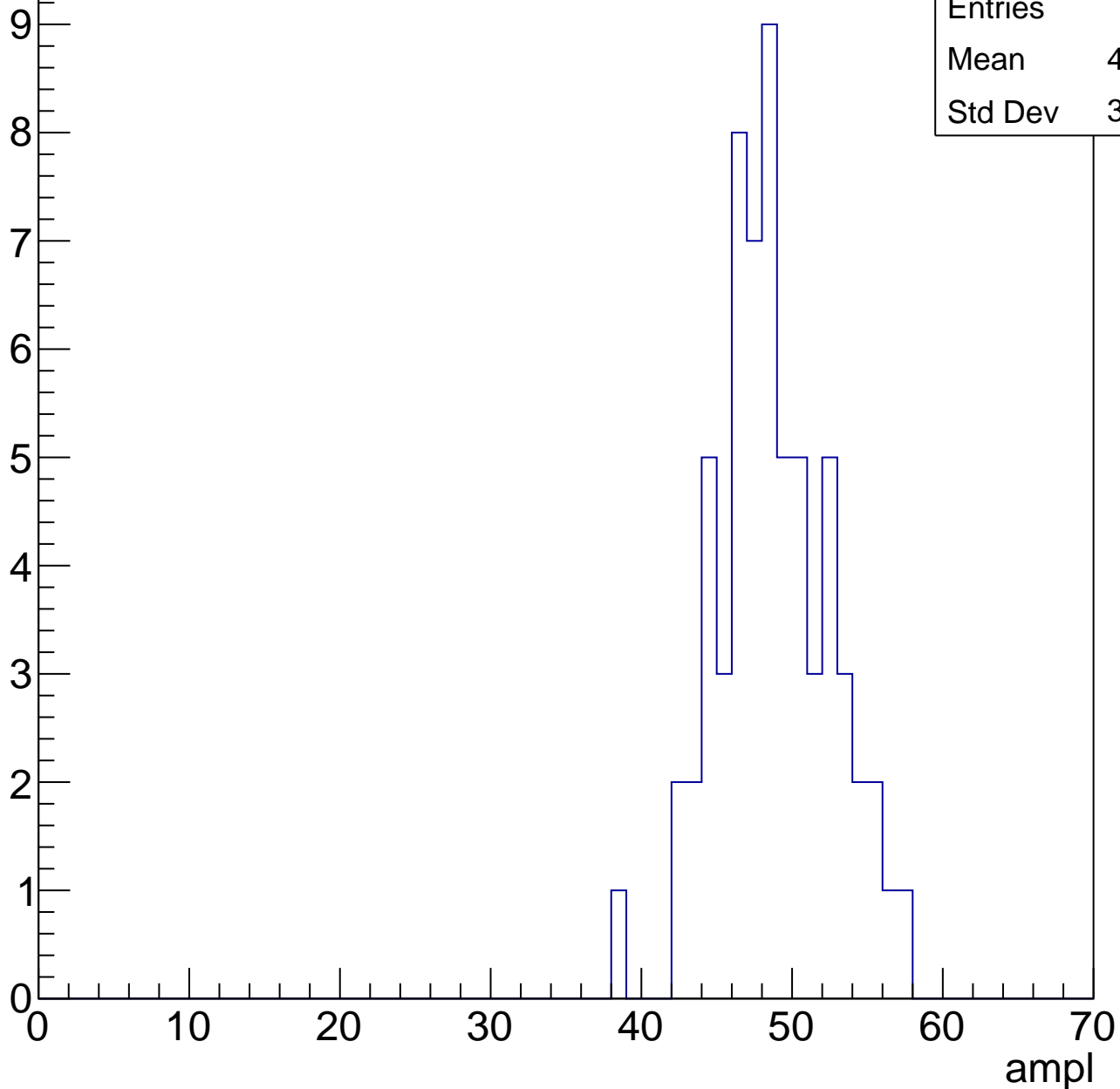
**Gaus Width: 3.3259**



# B1L101S, U22-ch44, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	64
Mean	48.28
Std Dev	3.718

# B1L101S, U22-ch44, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

7

6

5

4

3

2

1

0

Entries

64

Mean

54.31

Std Dev

3.142

0

10

20

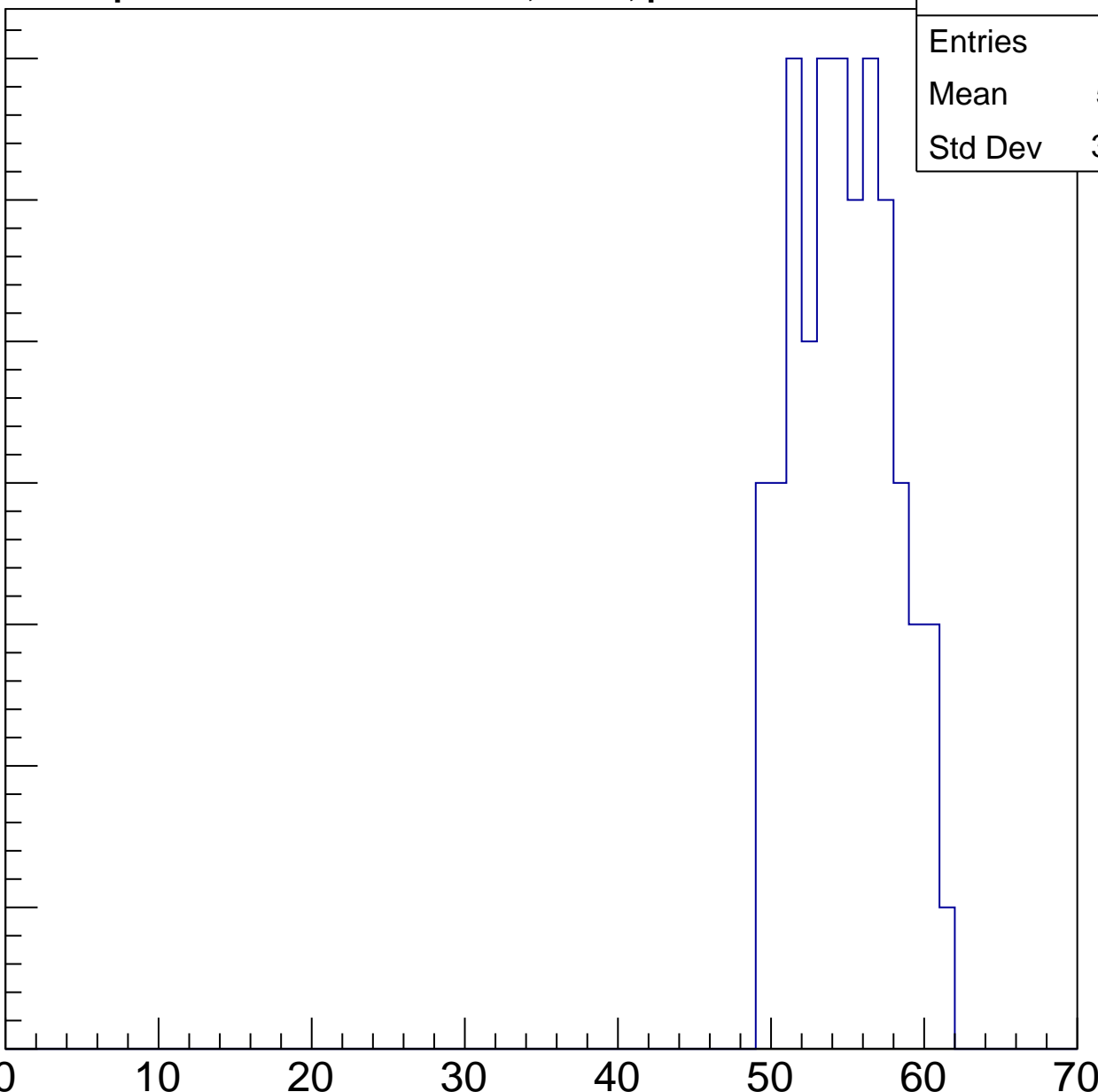
30

40

50

60

ampl

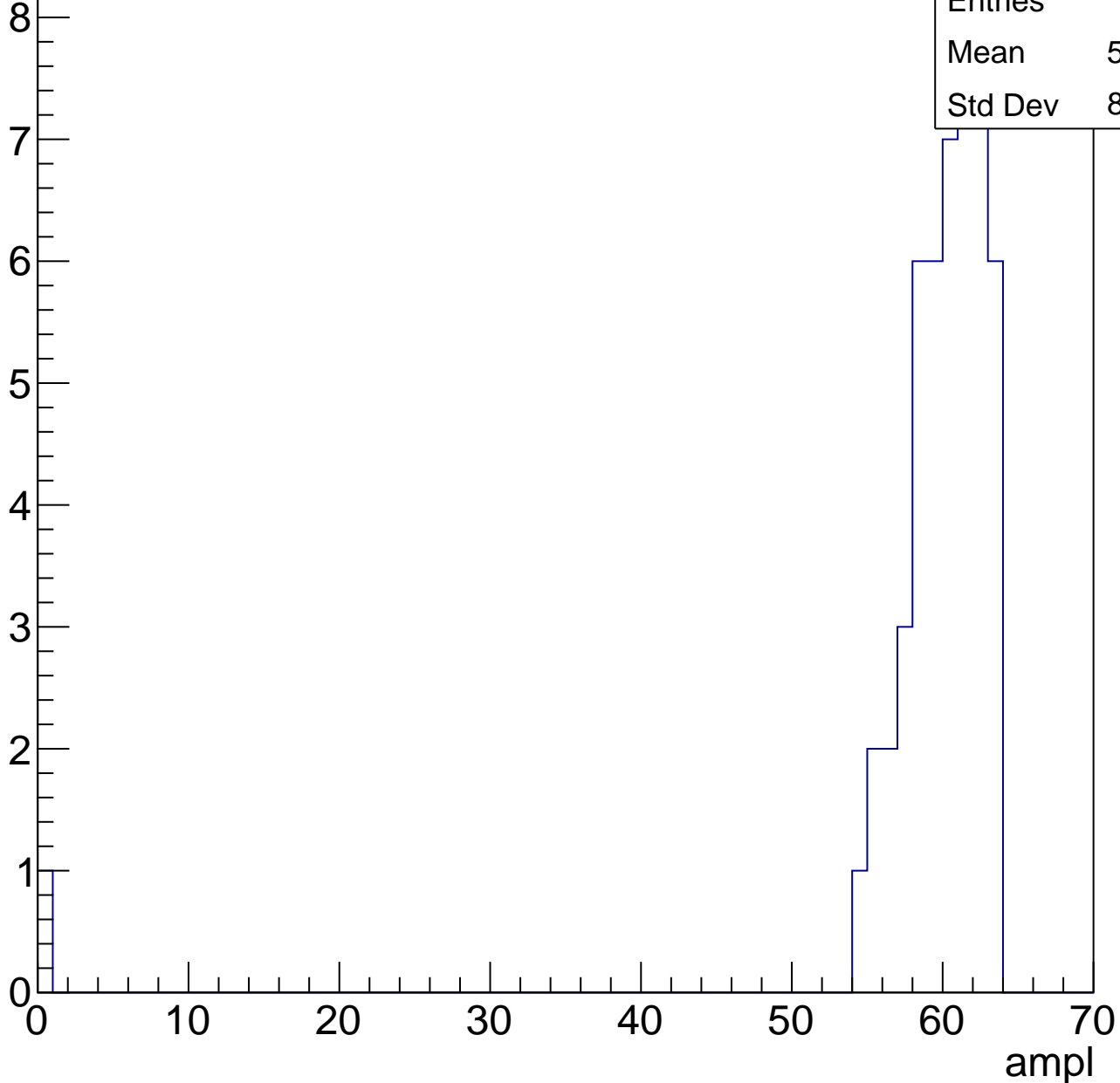


# B1L101S, U22-ch44, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

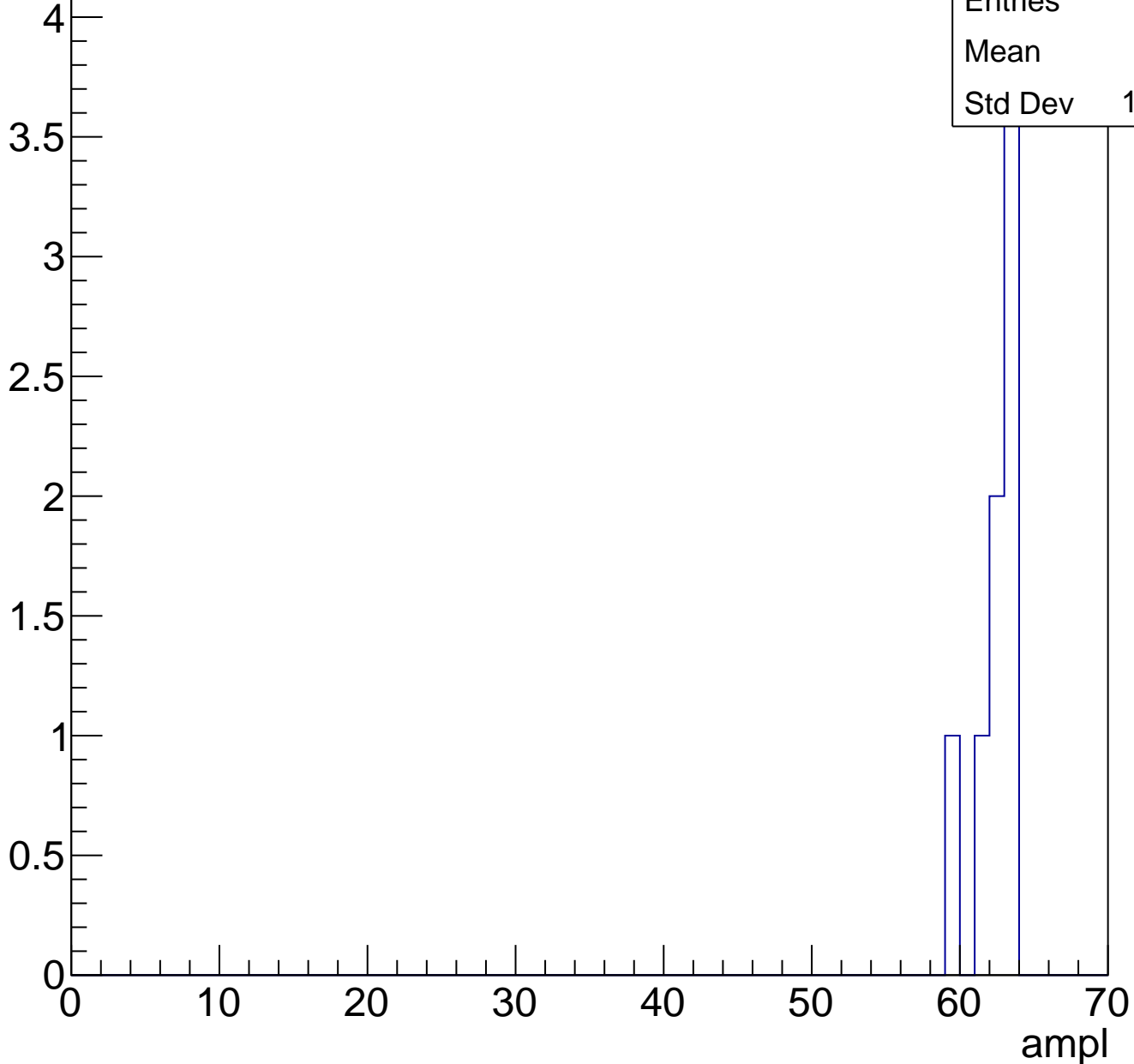
Entries	50
Mean	58.62
Std Dev	8.688



# B1L101S, U22-ch44, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U22-ch44, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U22-ch45, adc0

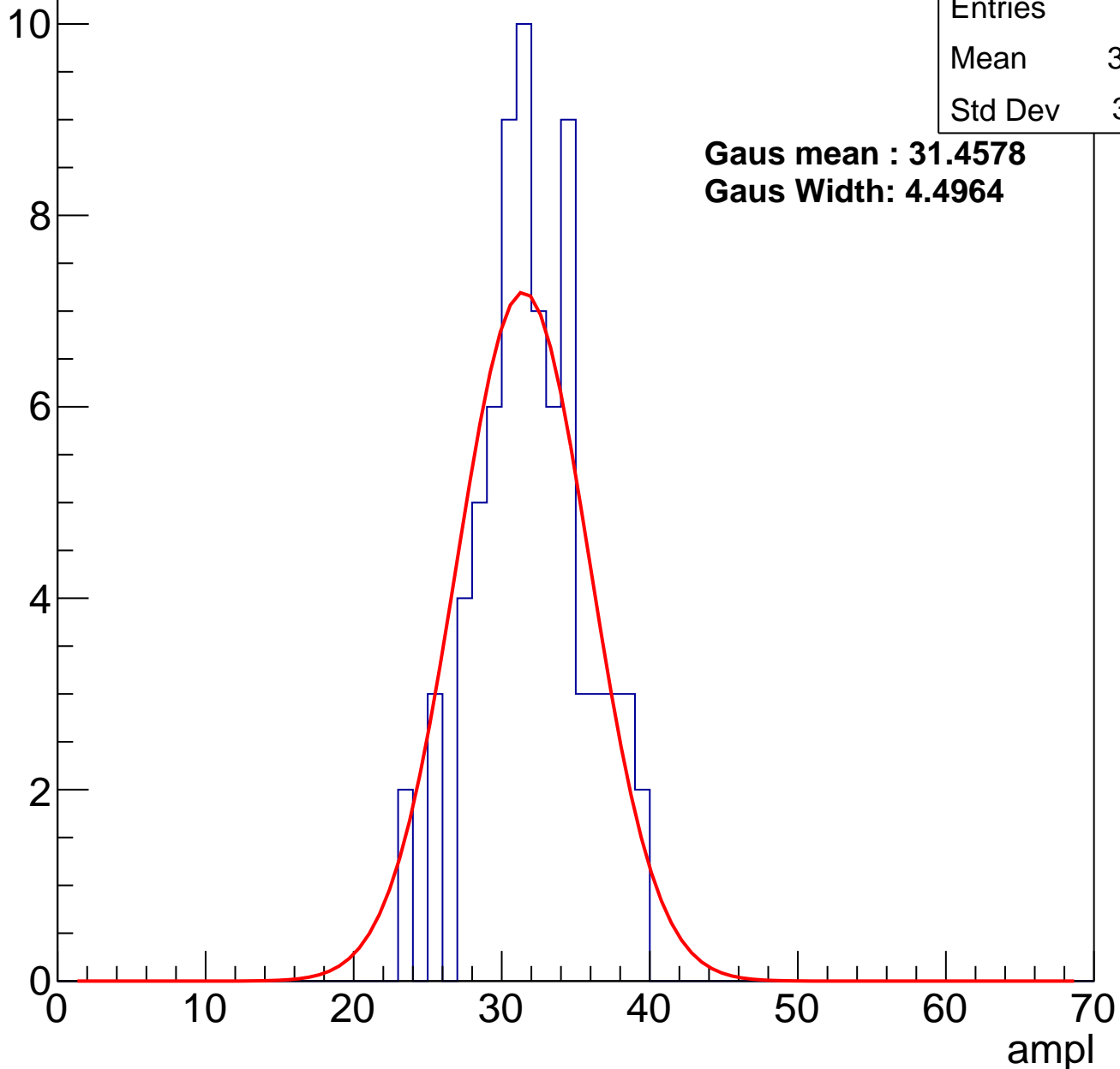
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	75
Mean	31.56
Std Dev	3.601

**Gaus mean : 31.4578**

**Gaus Width: 4.4964**

Entry



# B1L101S, U22-ch45, adc1

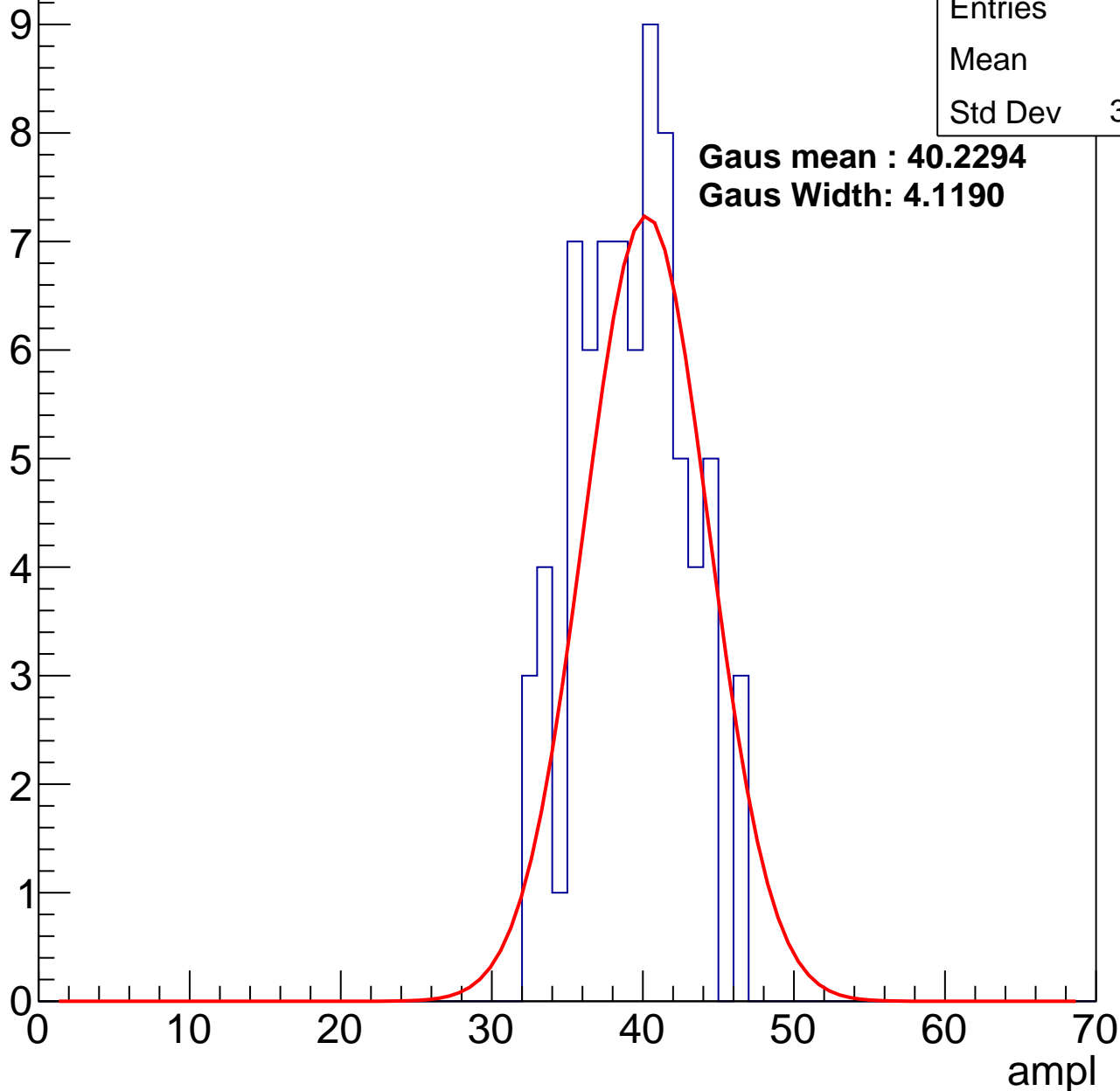
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	75
Mean	38.8
Std Dev	3.533

**Gaus mean : 40.2294**

**Gaus Width: 4.1190**



# B1L101S, U22-ch45, adc2

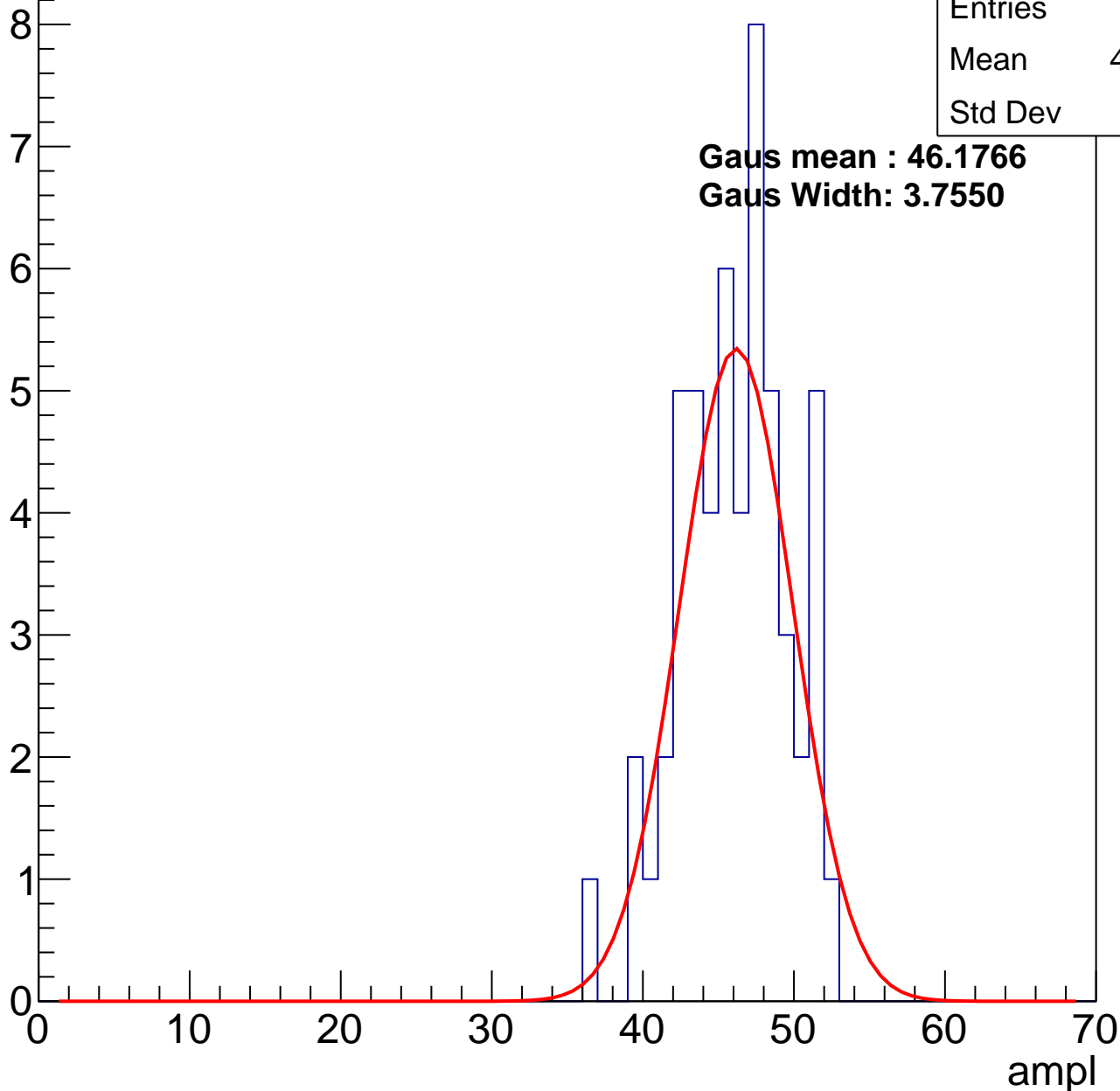
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	54
Mean	45.57
Std Dev	3.52

**Gaus mean : 46.1766**

**Gaus Width: 3.7550**

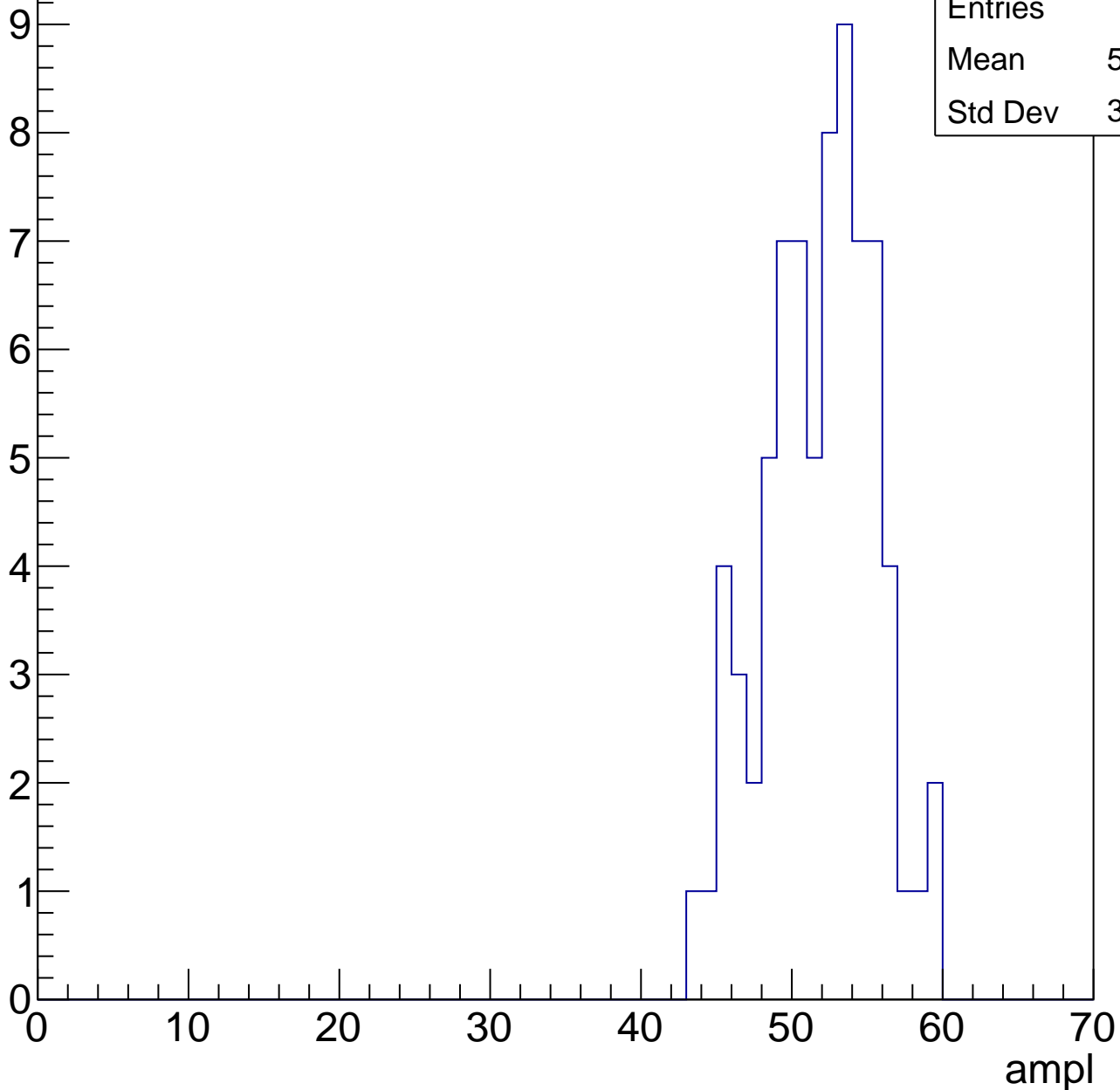


# B1L101S, U22-ch45, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	74
Mean	51.35
Std Dev	3.615

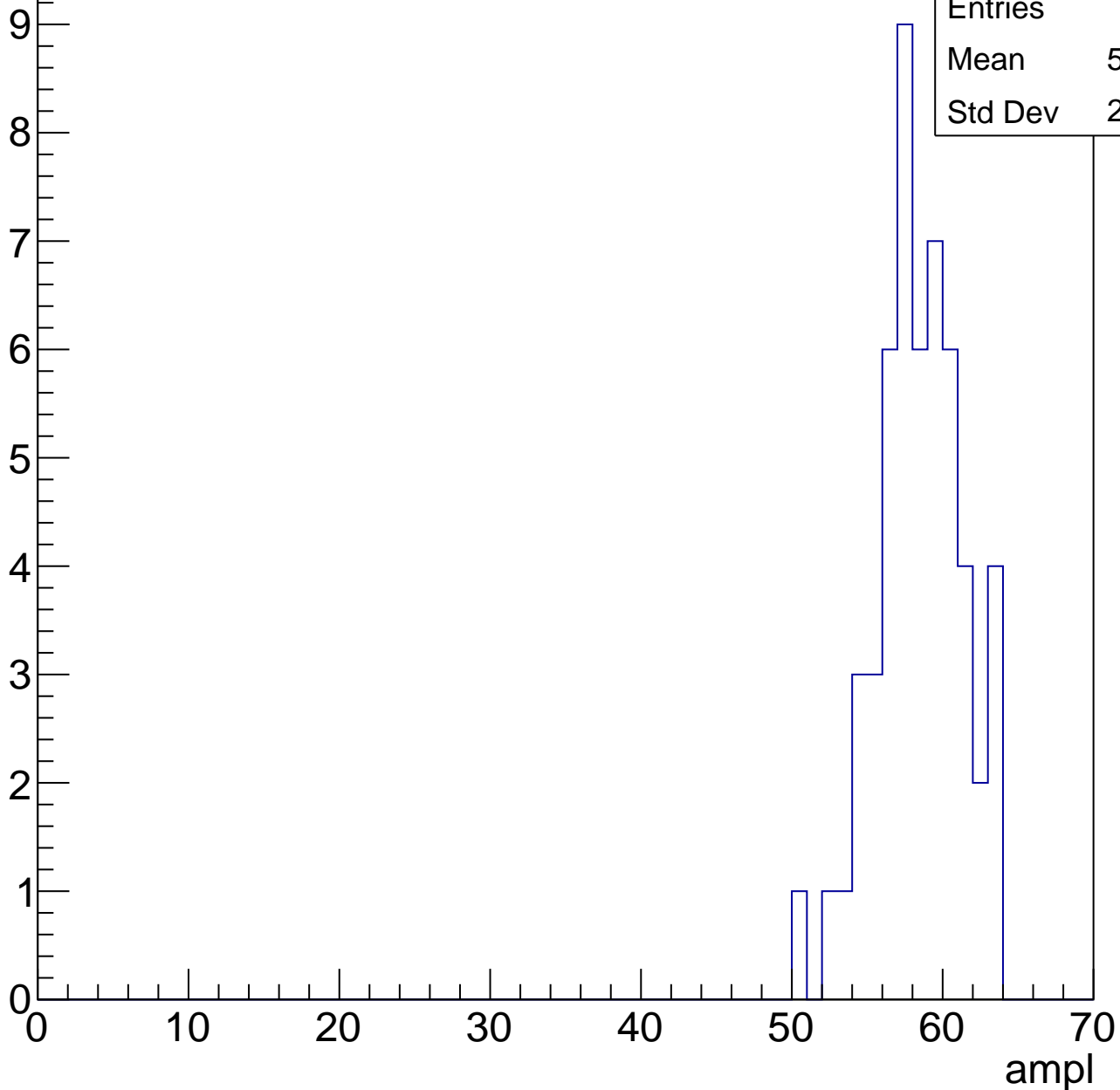


# B1L101S, U22-ch45, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	53
Mean	57.96
Std Dev	2.855

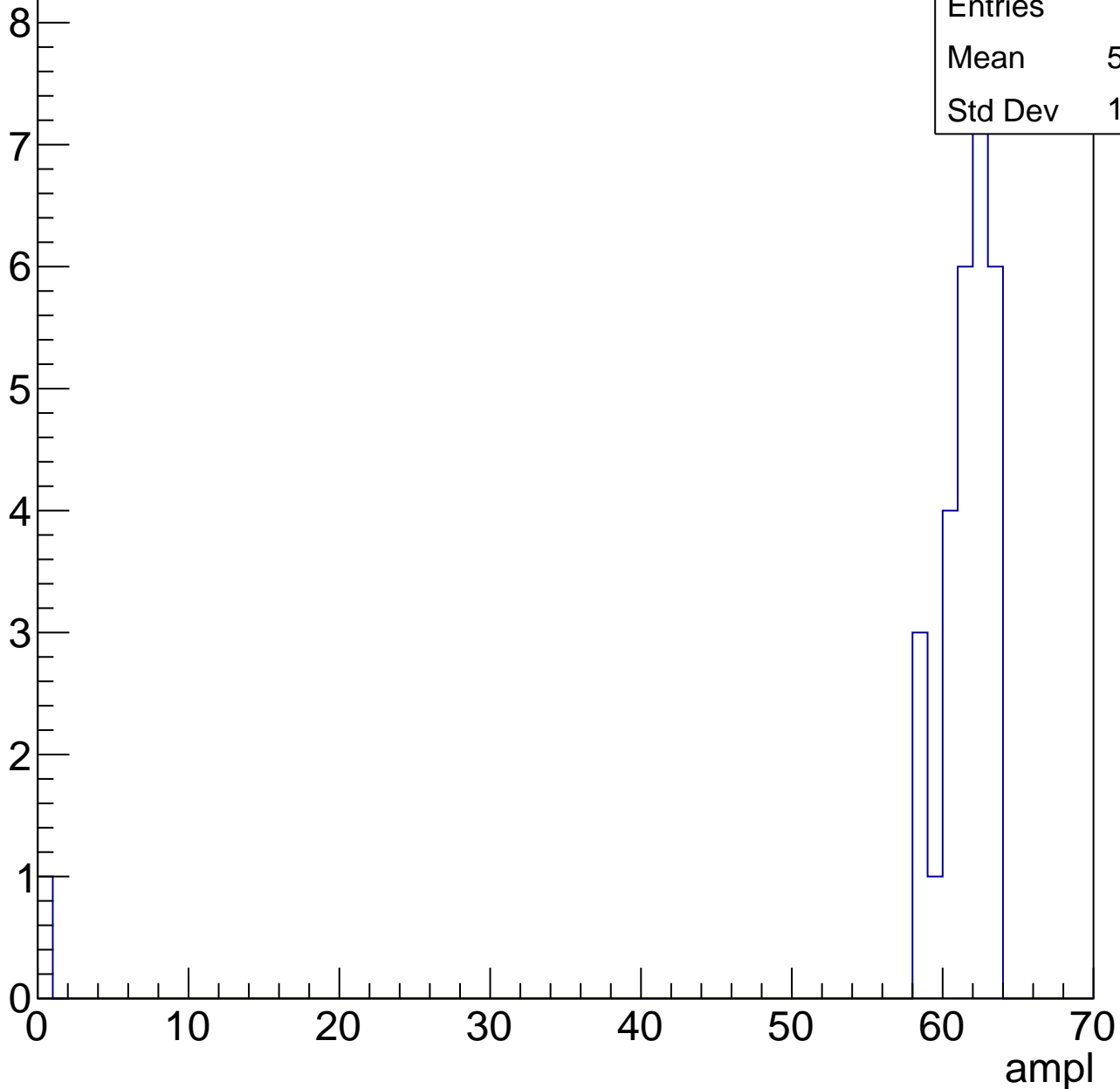


# B1L101S, U22-ch45, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	29
Mean	59.07
Std Dev	11.26



# B1L101S, U22-ch45, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U22-ch45, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U22-ch46, adc0

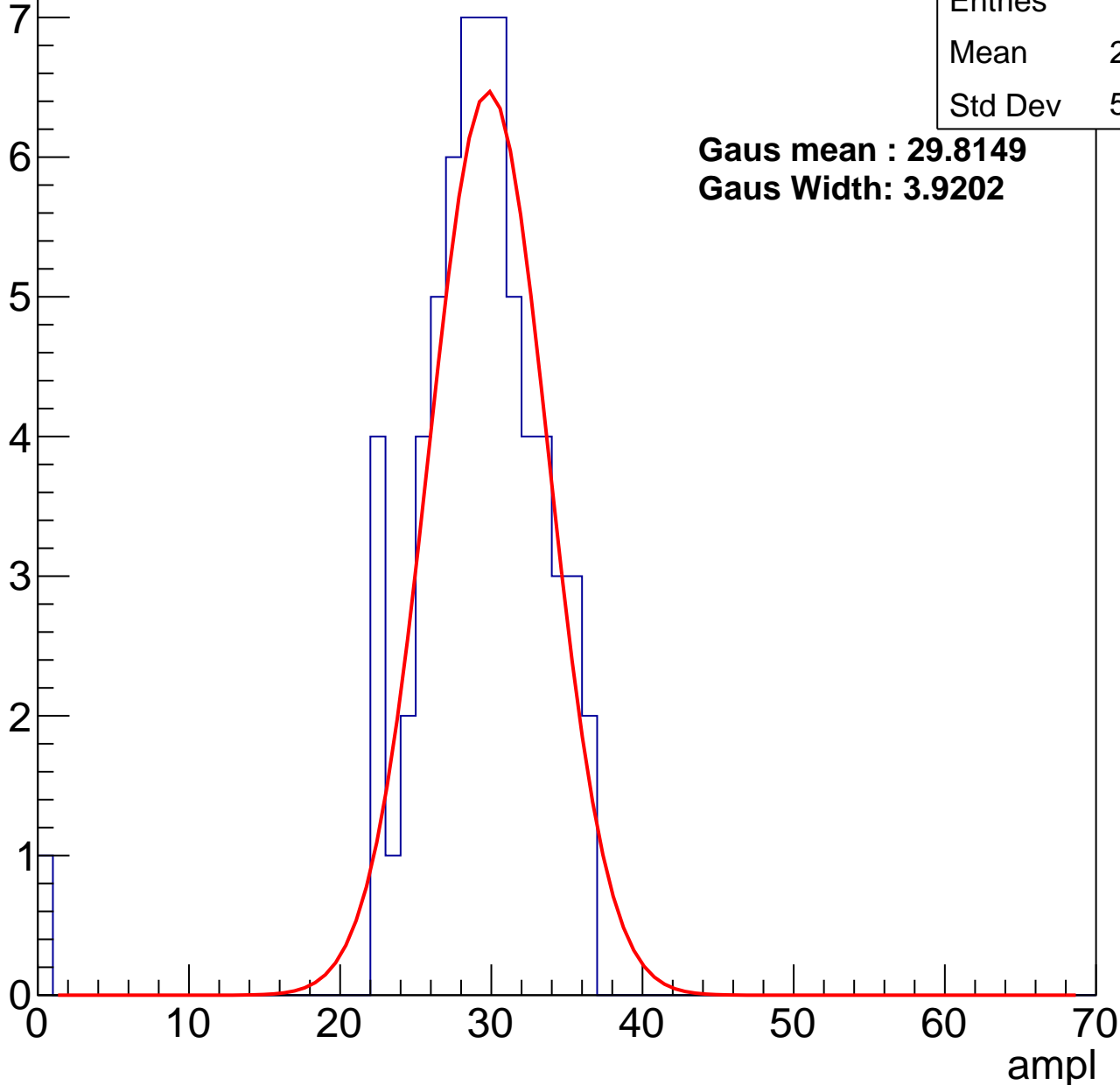
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	28.52
Std Dev	5.048

**Gaus mean : 29.8149**

**Gaus Width: 3.9202**



# B1L101S, U22-ch46, adc1

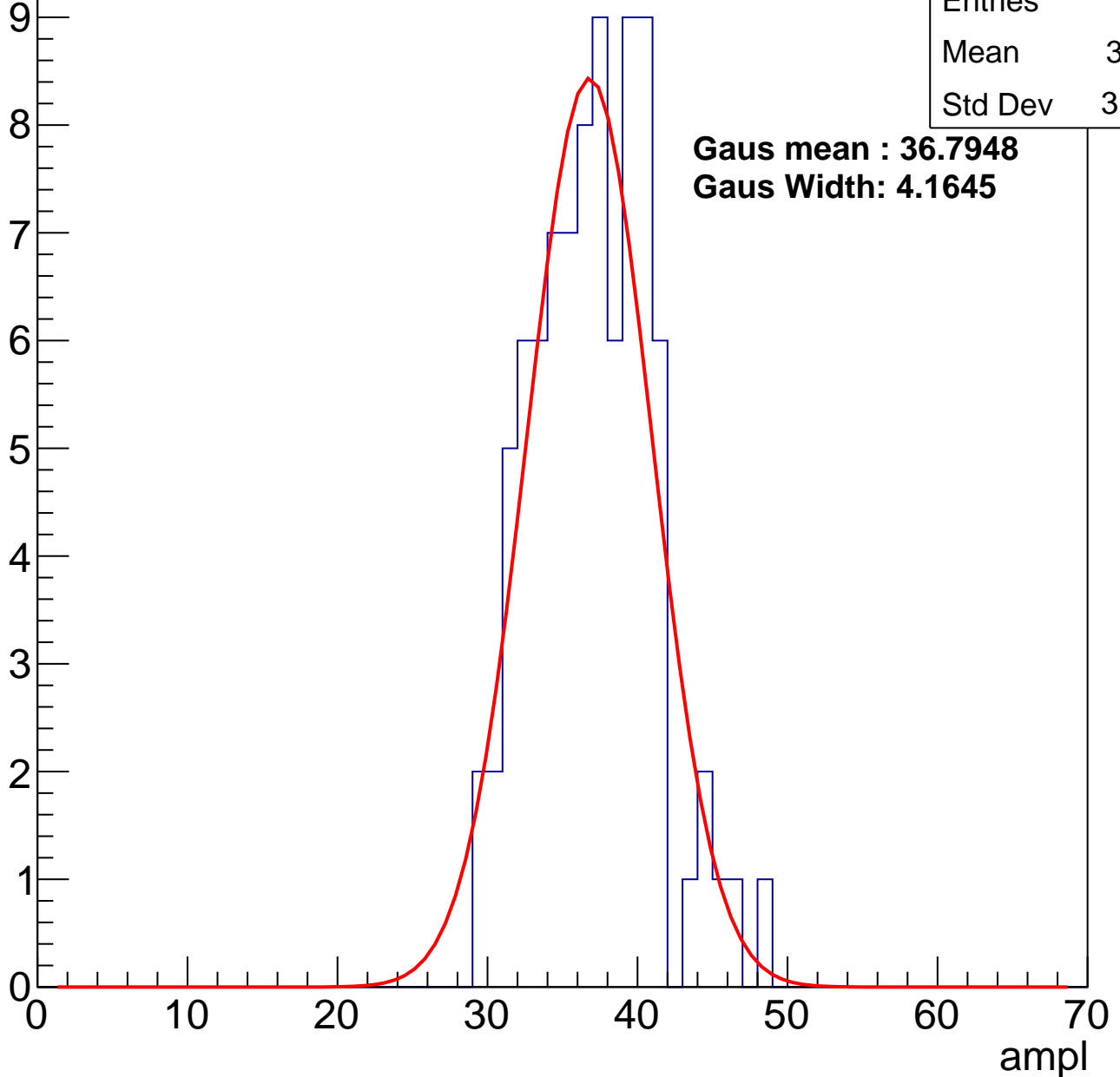
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	88
Mean	36.61
Std Dev	3.927

**Gaus mean : 36.7948**

**Gaus Width: 4.1645**



# B1L101S, U22-ch46, adc2

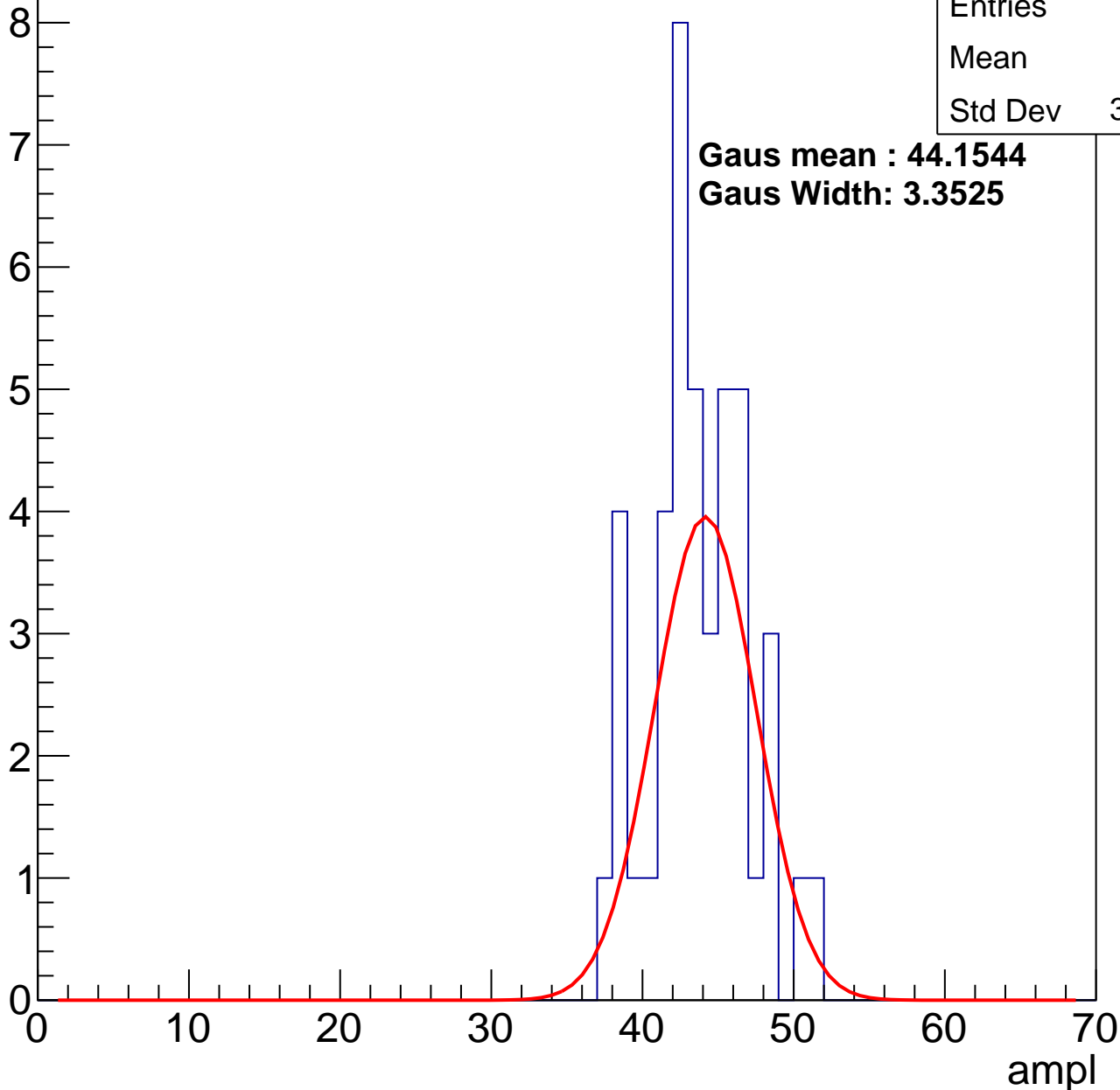
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	43
Mean	43.3
Std Dev	3.246

**Gaus mean : 44.1544**

**Gaus Width: 3.3525**

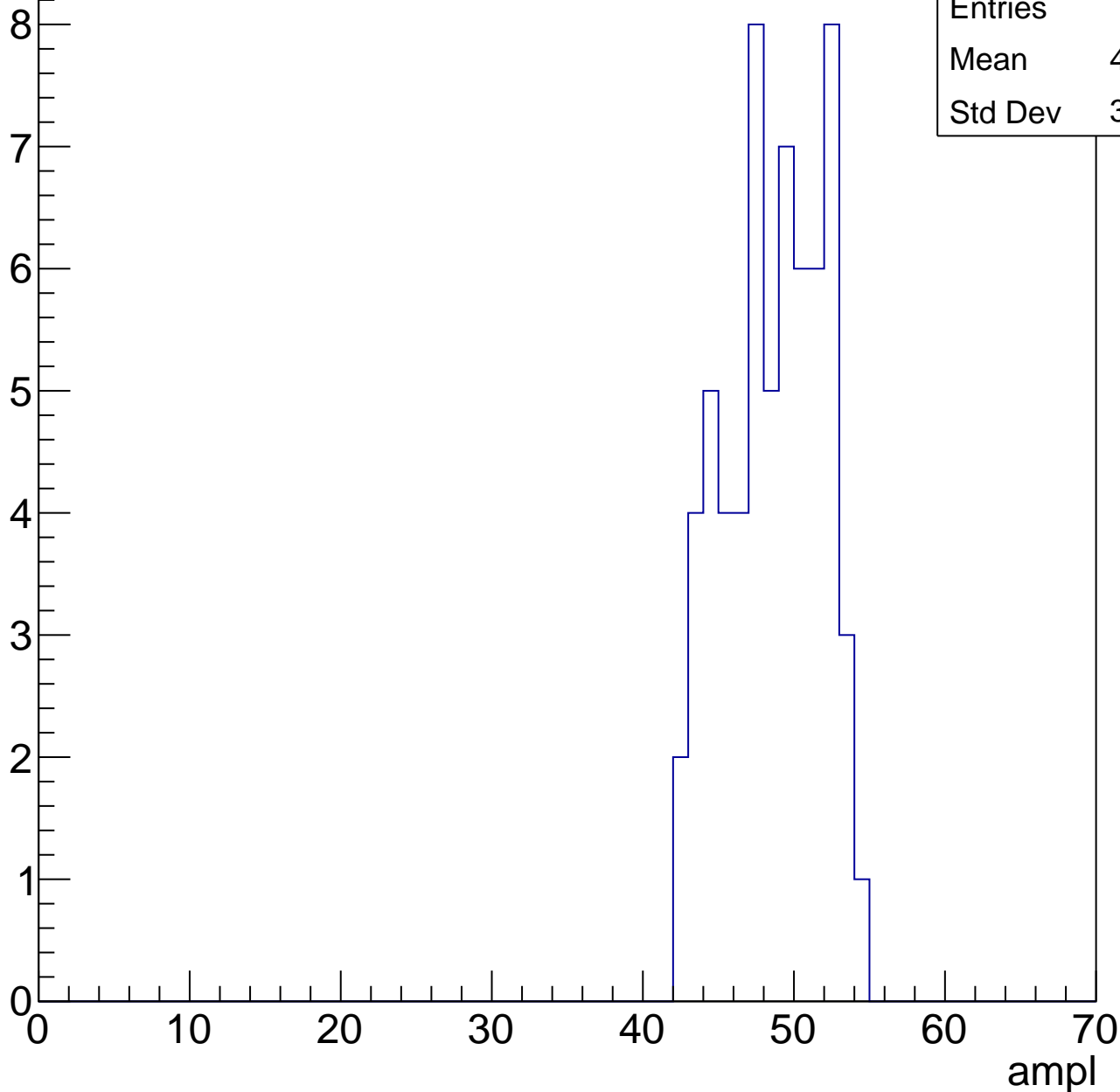


# B1L101S, U22-ch46, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	48.16
Std Dev	3.173

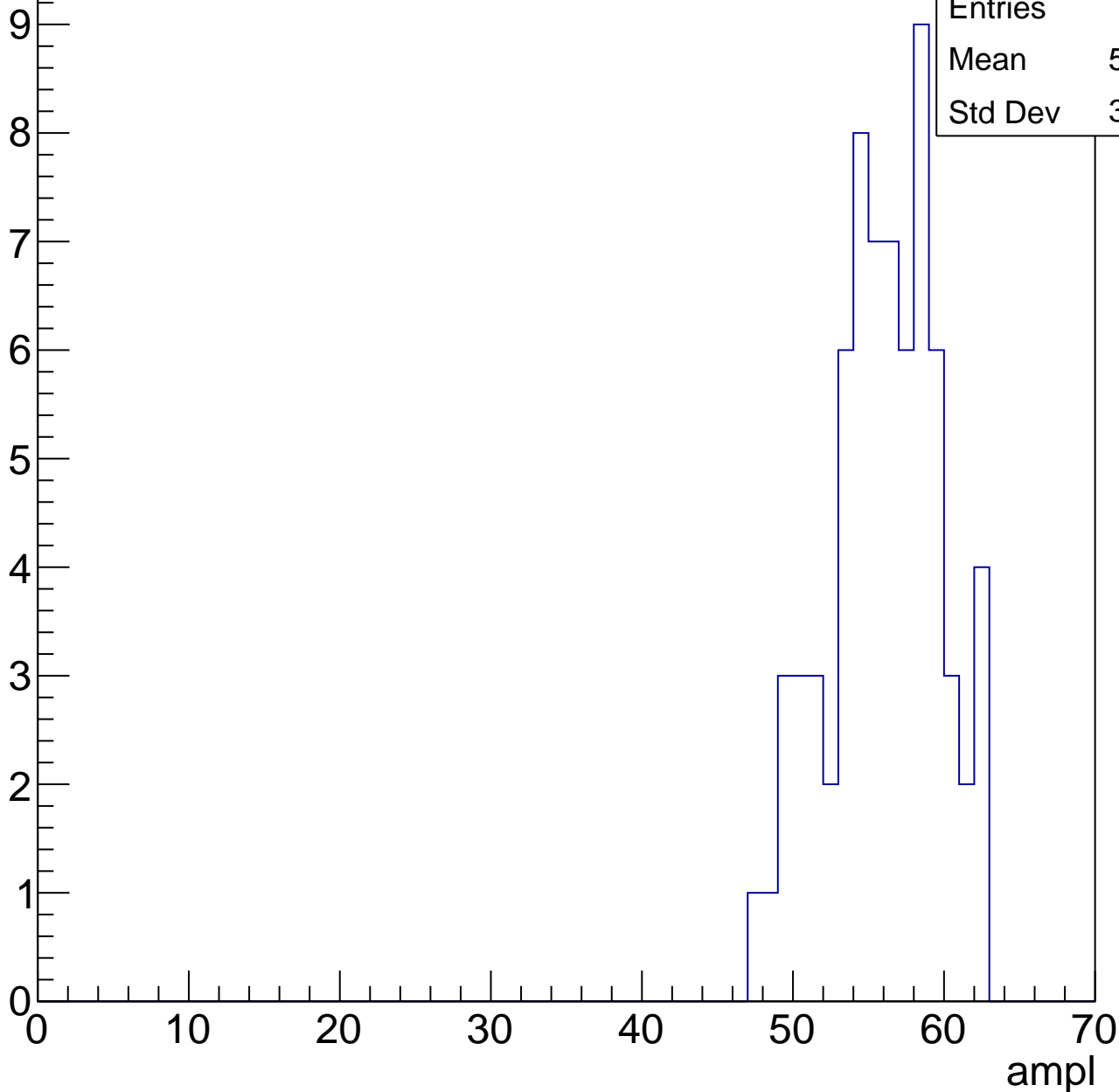


# B1L101S, U22-ch46, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	71
Mean	55.55
Std Dev	3.607

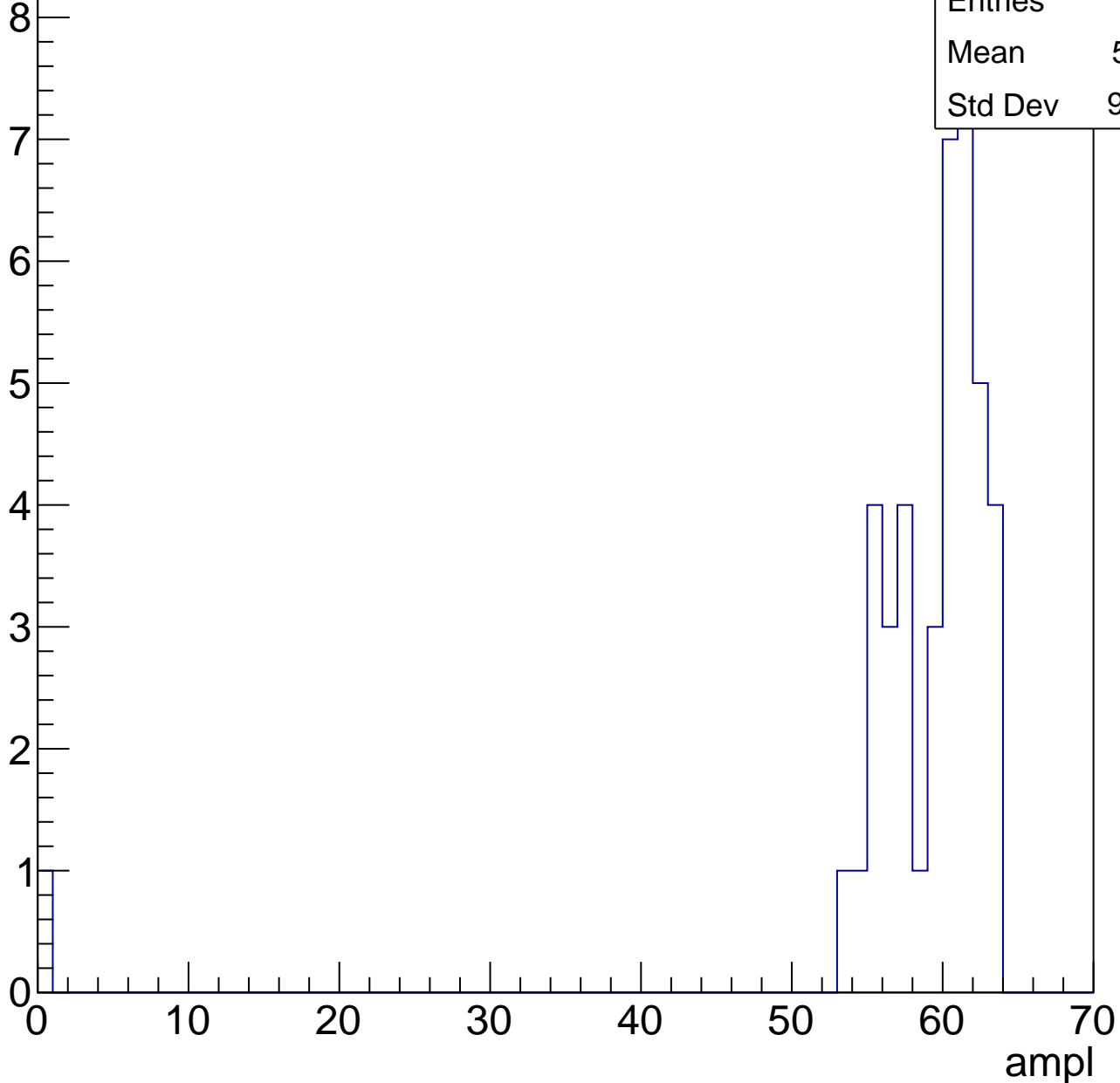


# B1L101S, U22-ch46, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	42
Mean	57.81
Std Dev	9.435

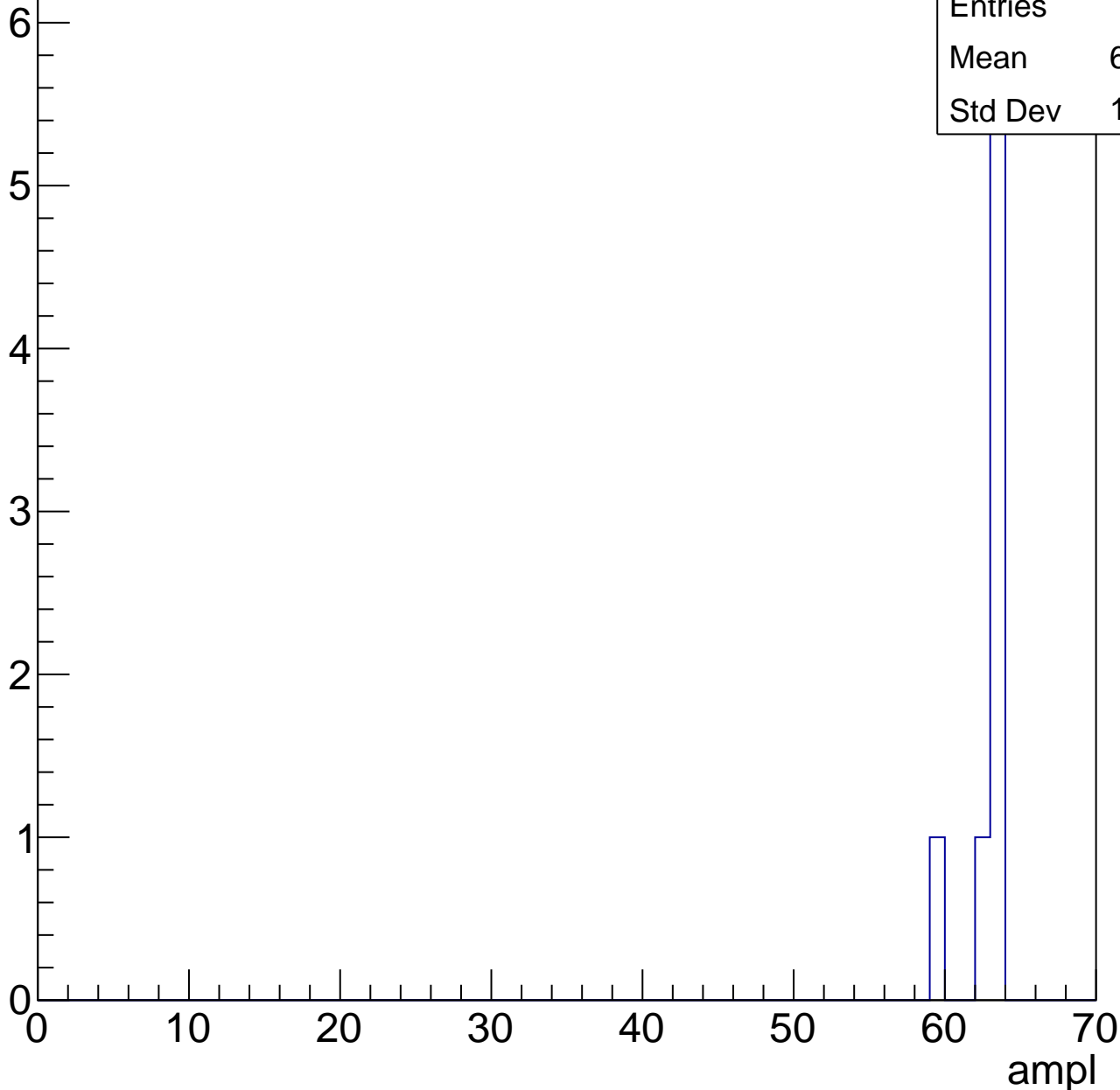


# B1L101S, U22-ch46, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	8
Mean	62.38
Std Dev	1.317





# B1L101S, U22-ch46, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L101S, U22-ch47, adc0

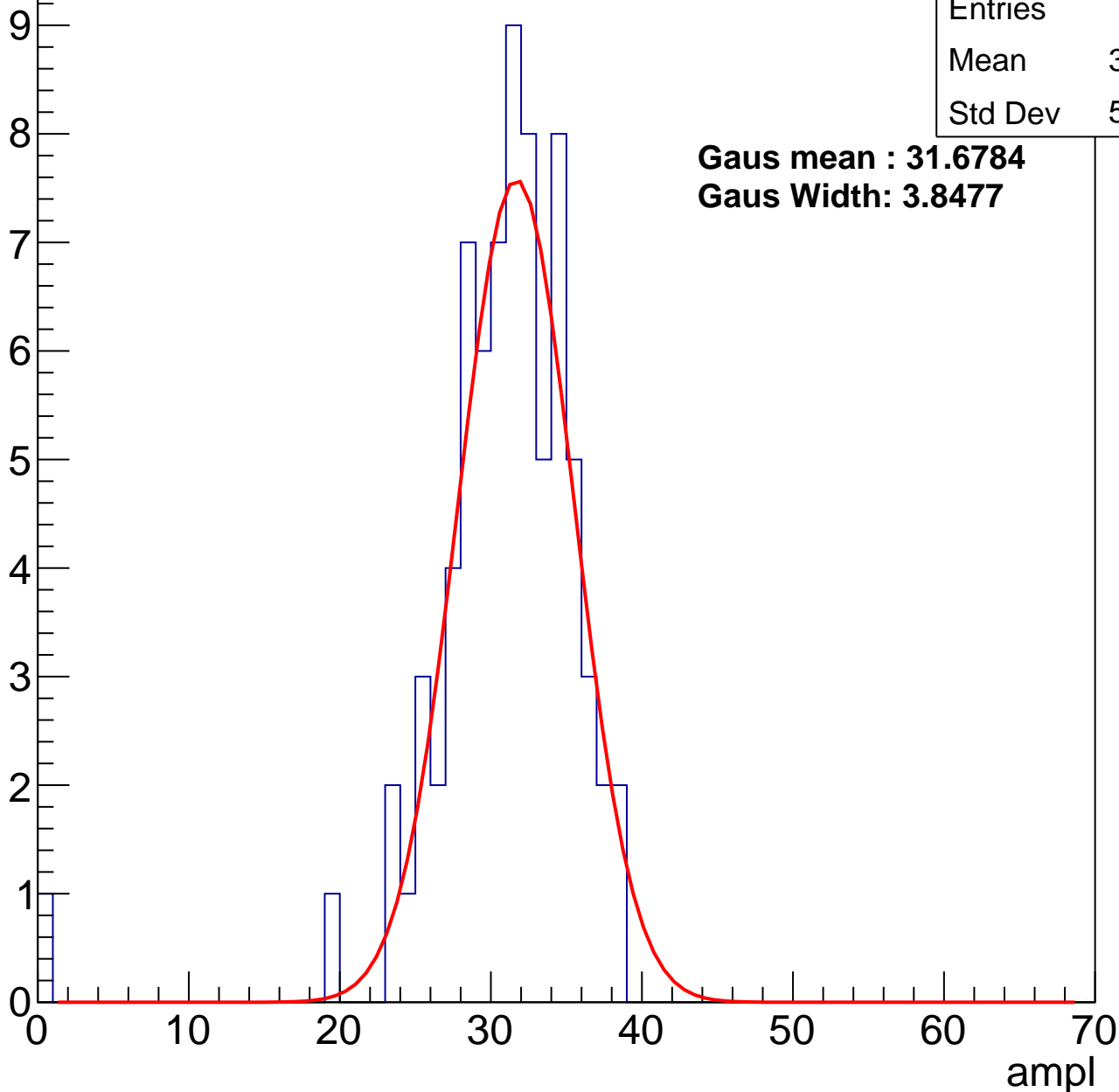
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	76
Mean	30.38
Std Dev	5.122

**Gaus mean : 31.6784**

**Gaus Width: 3.8477**



# B1L101S, U22-ch47, adc1

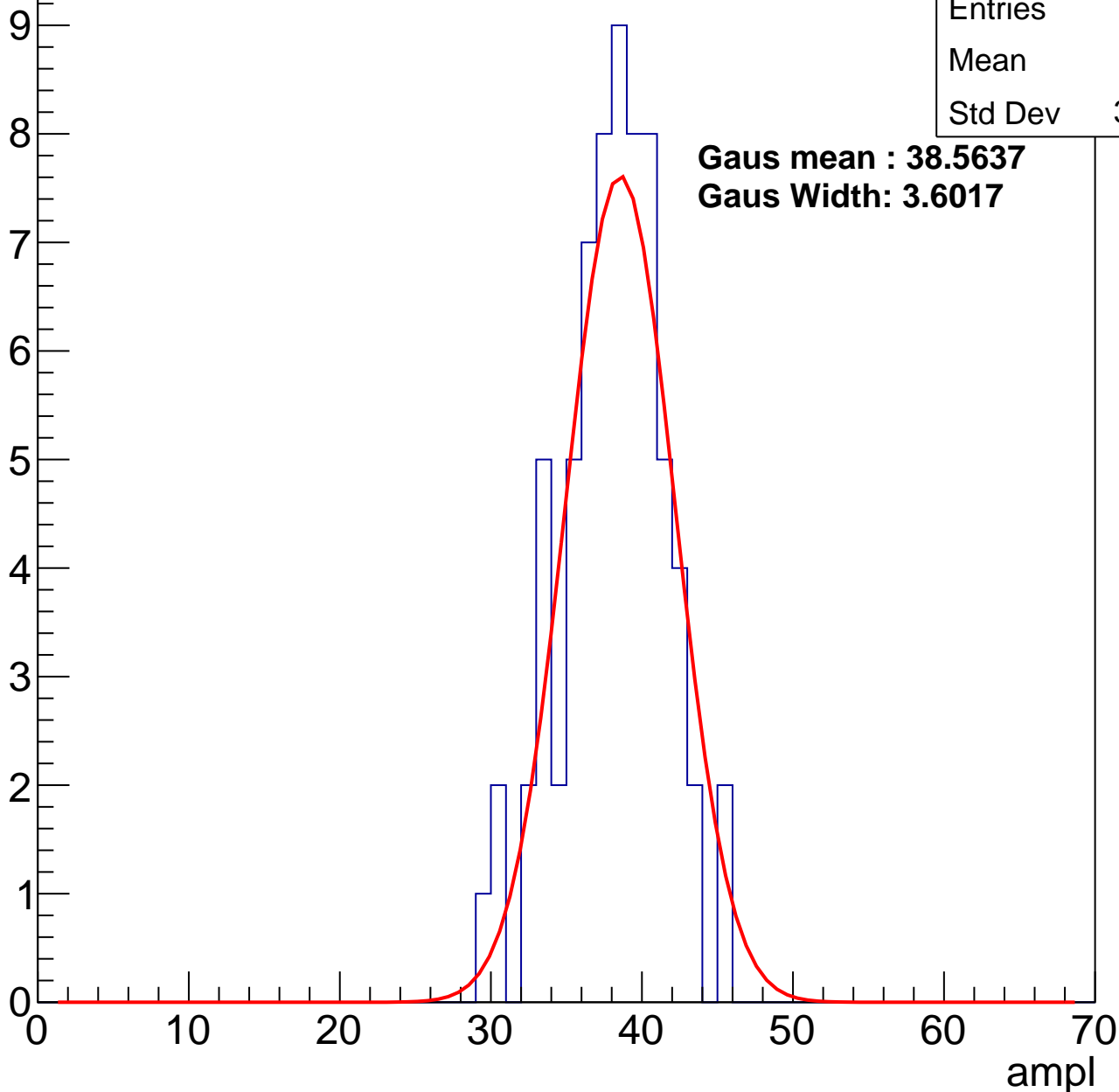
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	37.6
Std Dev	3.391

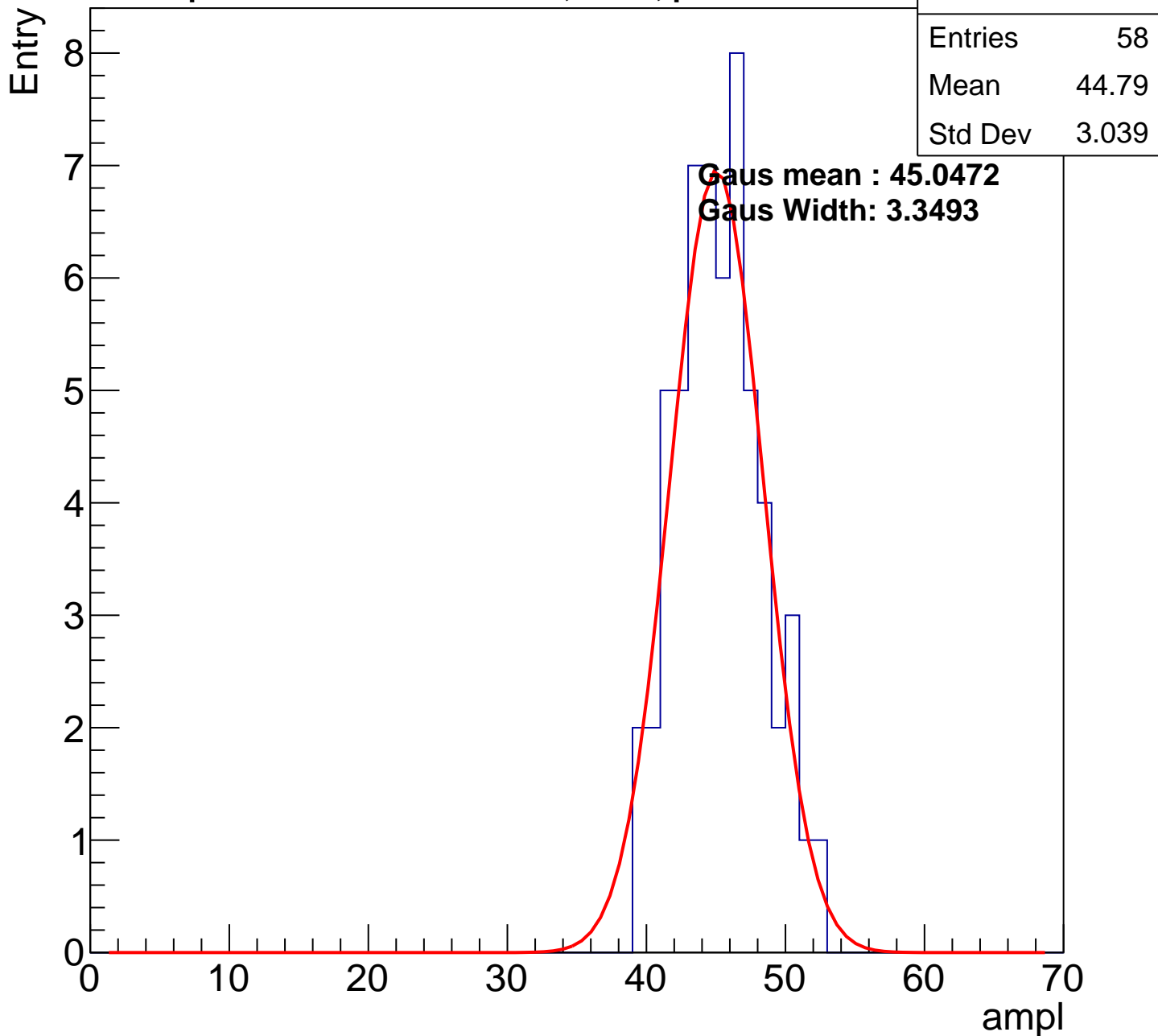
**Gaus mean : 38.5637**

**Gaus Width: 3.6017**



# B1L101S, U22-ch47, adc2

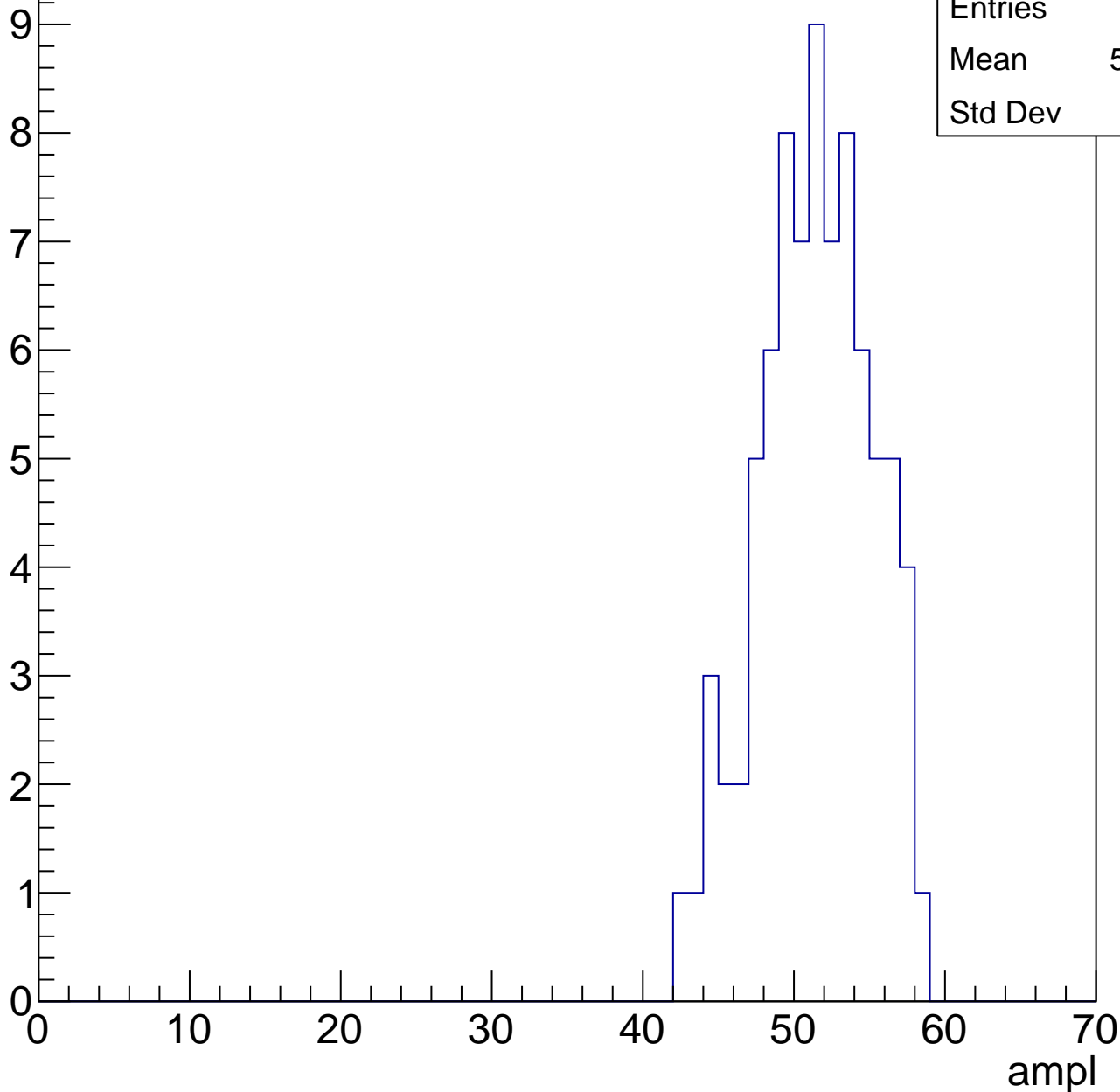
calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U22-ch47, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U22-ch47, adc4

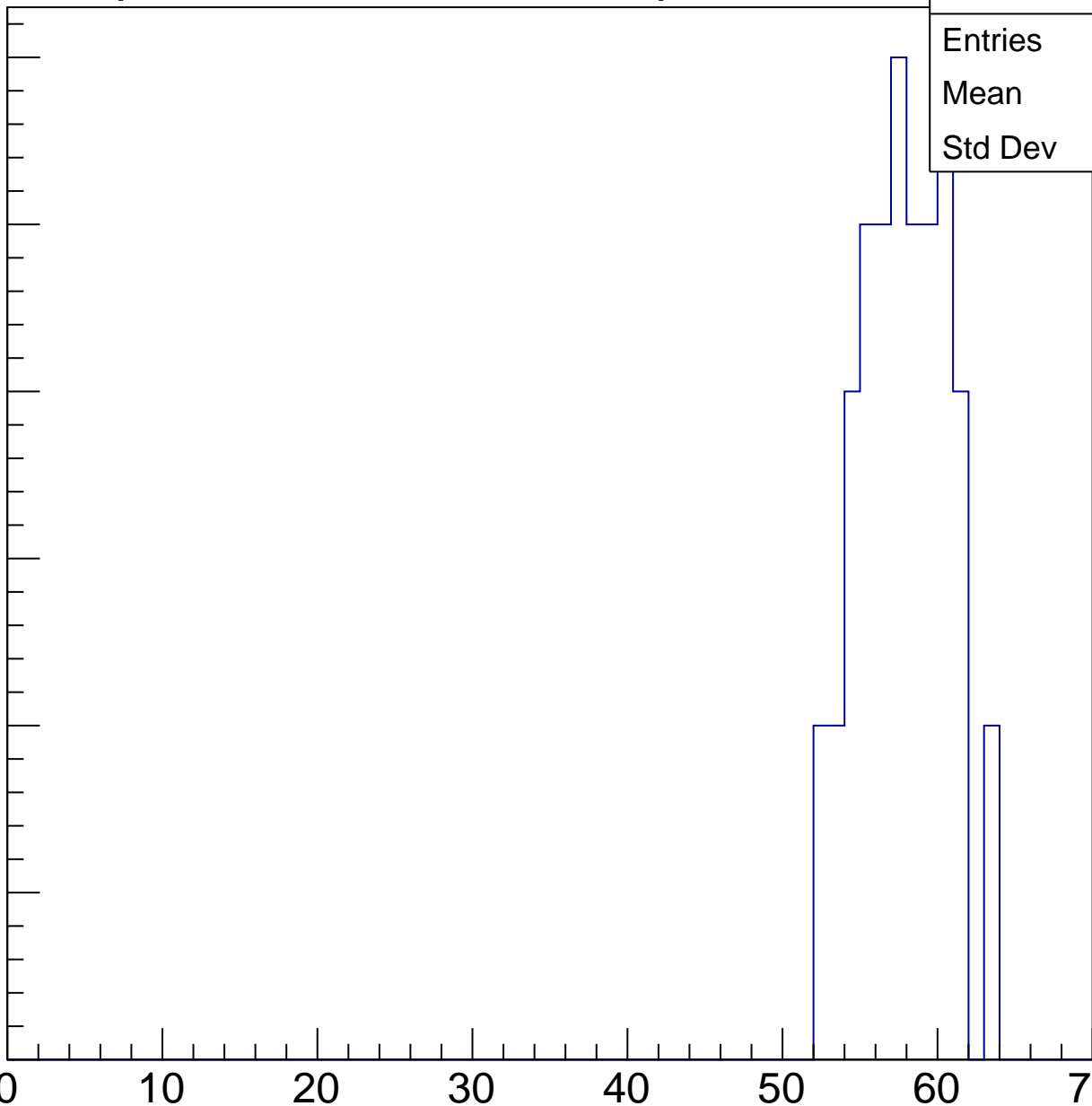
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

6  
5  
4  
3  
2  
1  
0

Entries	46
Mean	57.35
Std Dev	2.768

ampl



# B1L101S, U22-ch47, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	36
Mean	59.19
Std Dev	10.13

Entry

10

8

6

4

2

0

0

10

20

30

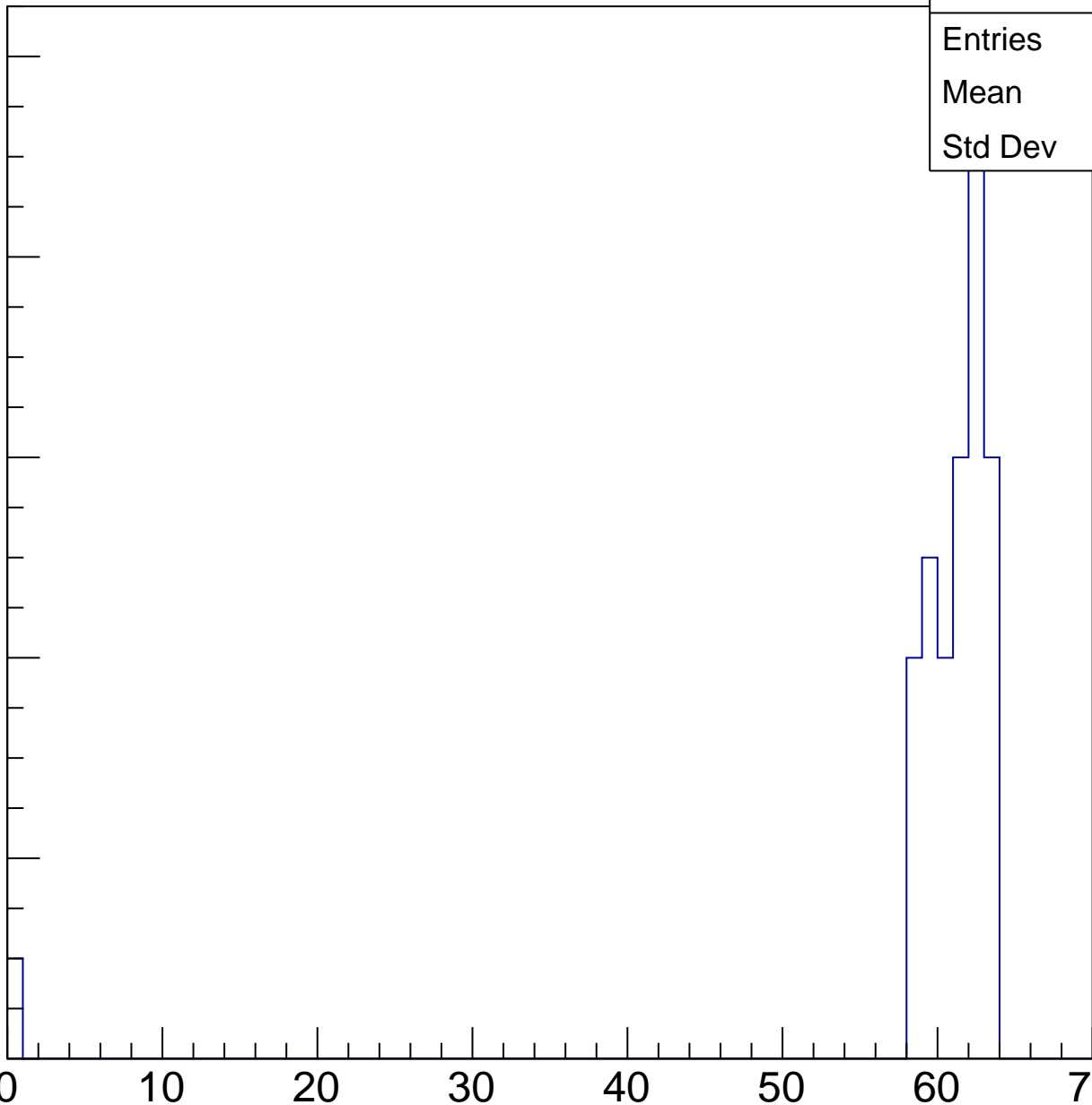
40

50

60

70

ampl



# B1L101S, U22-ch47, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	2
Mean	63
Std Dev	0

0 10 20 30 40 50 60 70

ampl



# B1L101S, U22-ch47, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L101S, U22-ch48, adc0

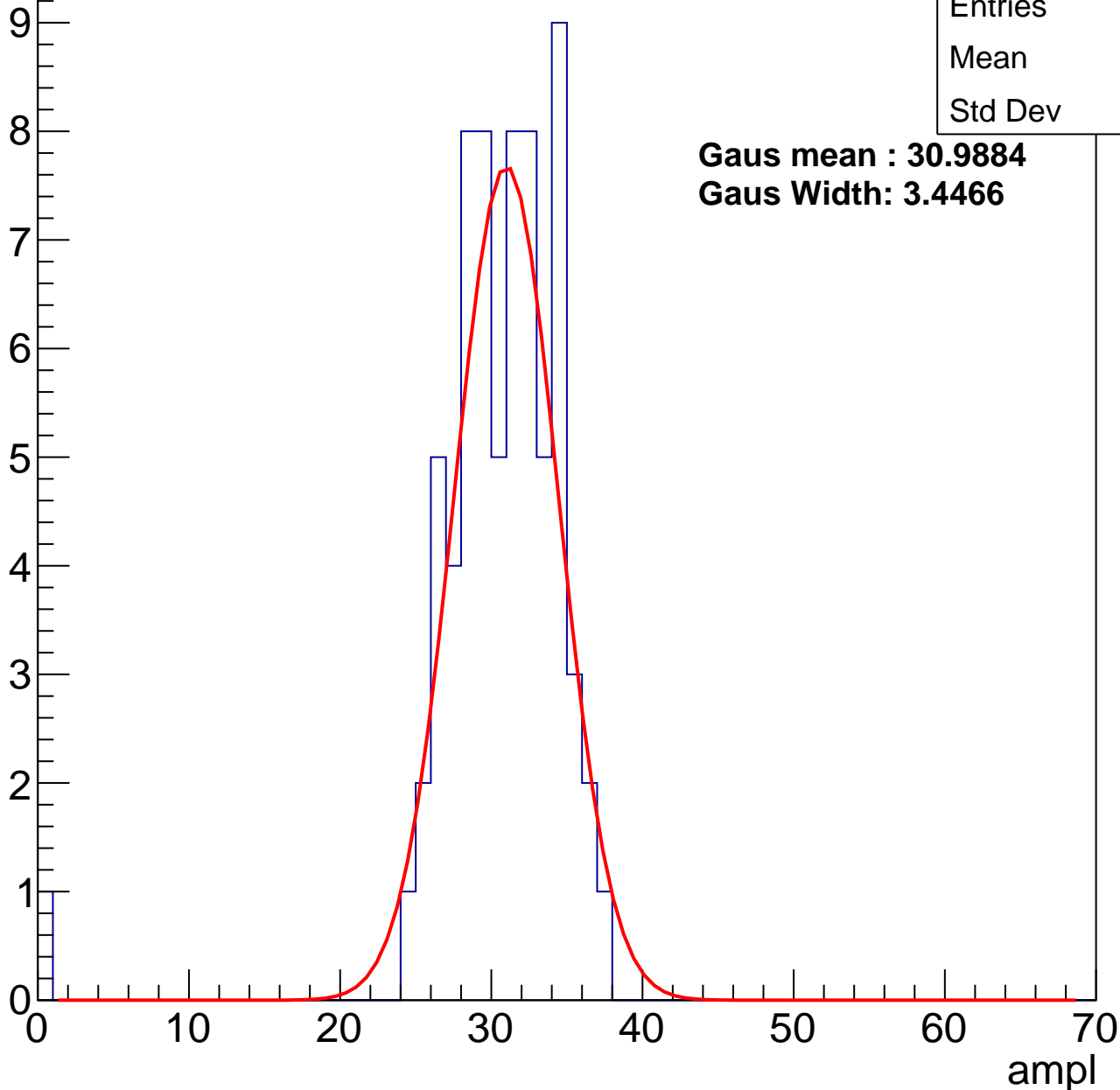
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	30.1
Std Dev	4.73

**Gaus mean : 30.9884**

**Gaus Width: 3.4466**



# B1L101S, U22-ch48, adc1

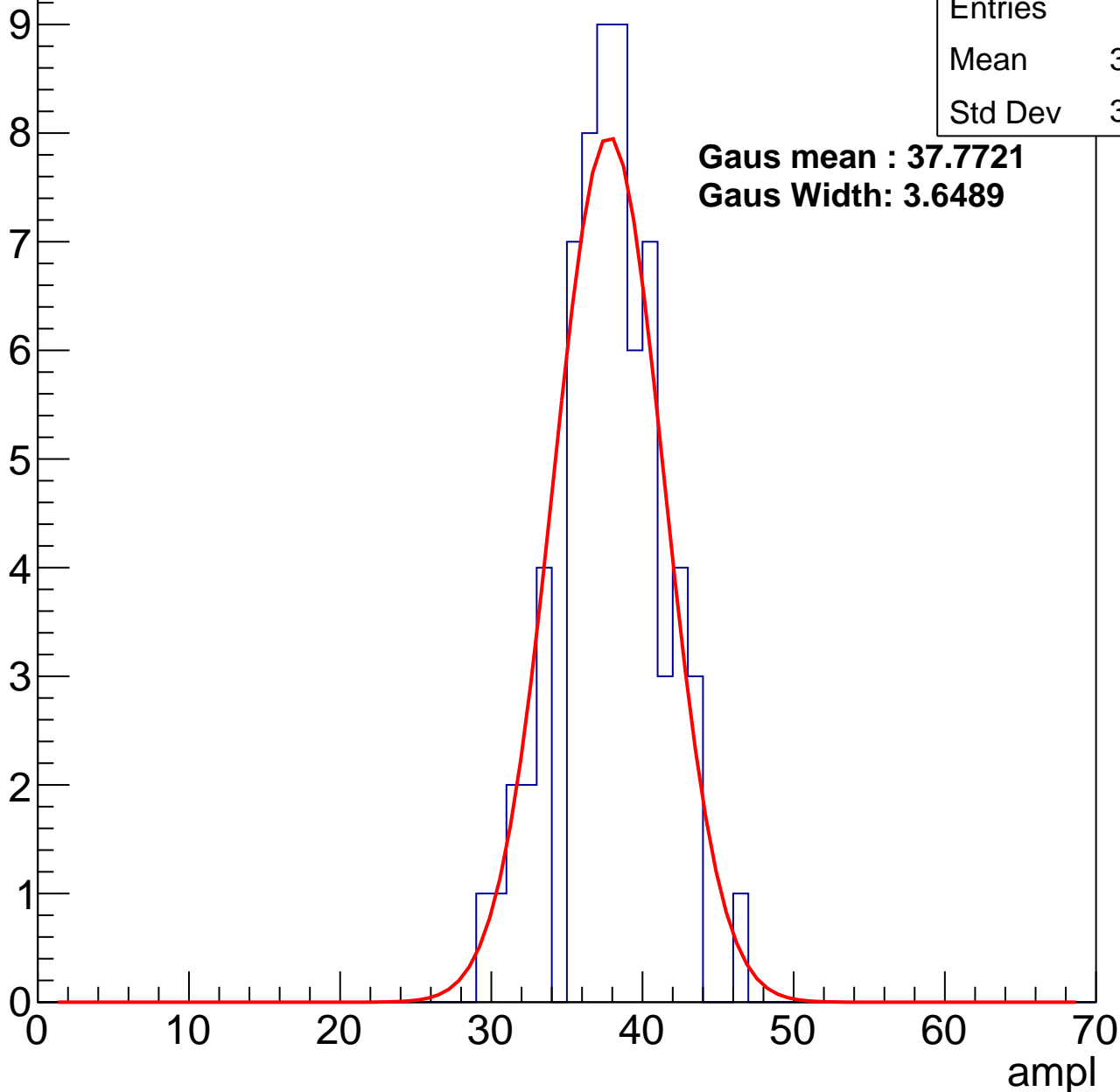
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	67
Mean	37.39
Std Dev	3.363

**Gaus mean : 37.7721**

**Gaus Width: 3.6489**



# B1L101S, U22-ch48, adc2

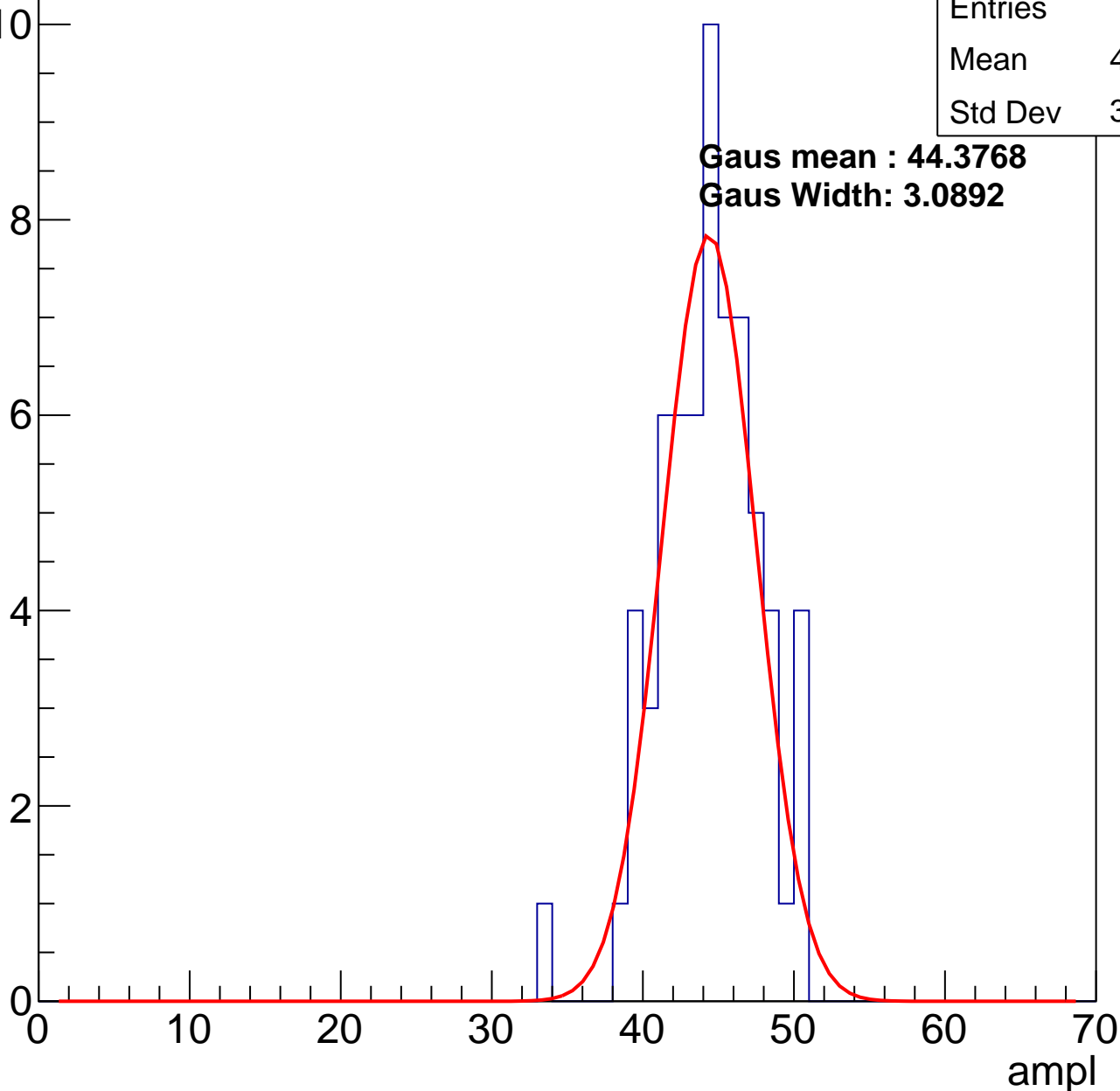
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	43.94
Std Dev	3.286

**Gaus mean : 44.3768**

**Gaus Width: 3.0892**

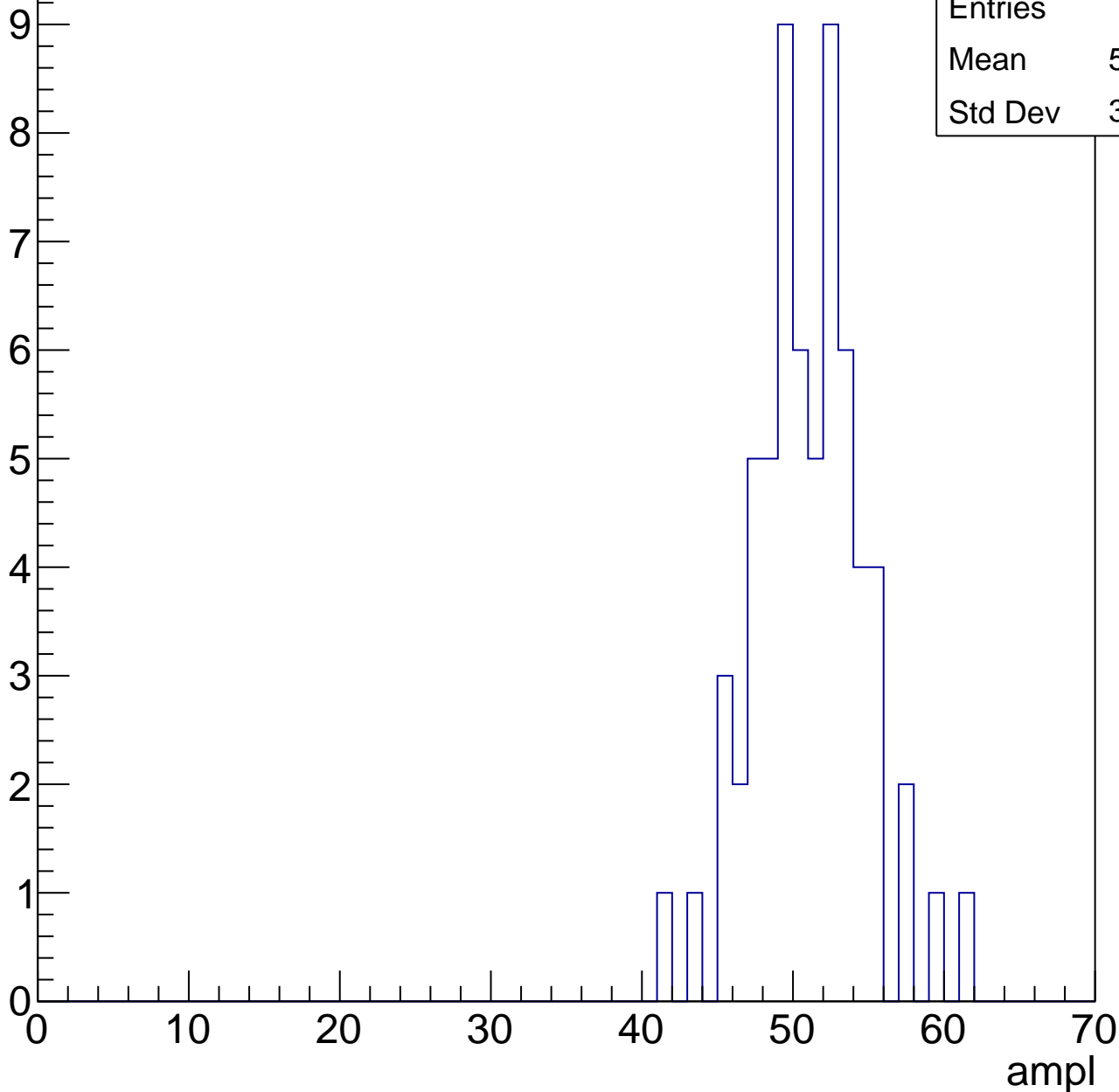


# B1L101S, U22-ch48, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

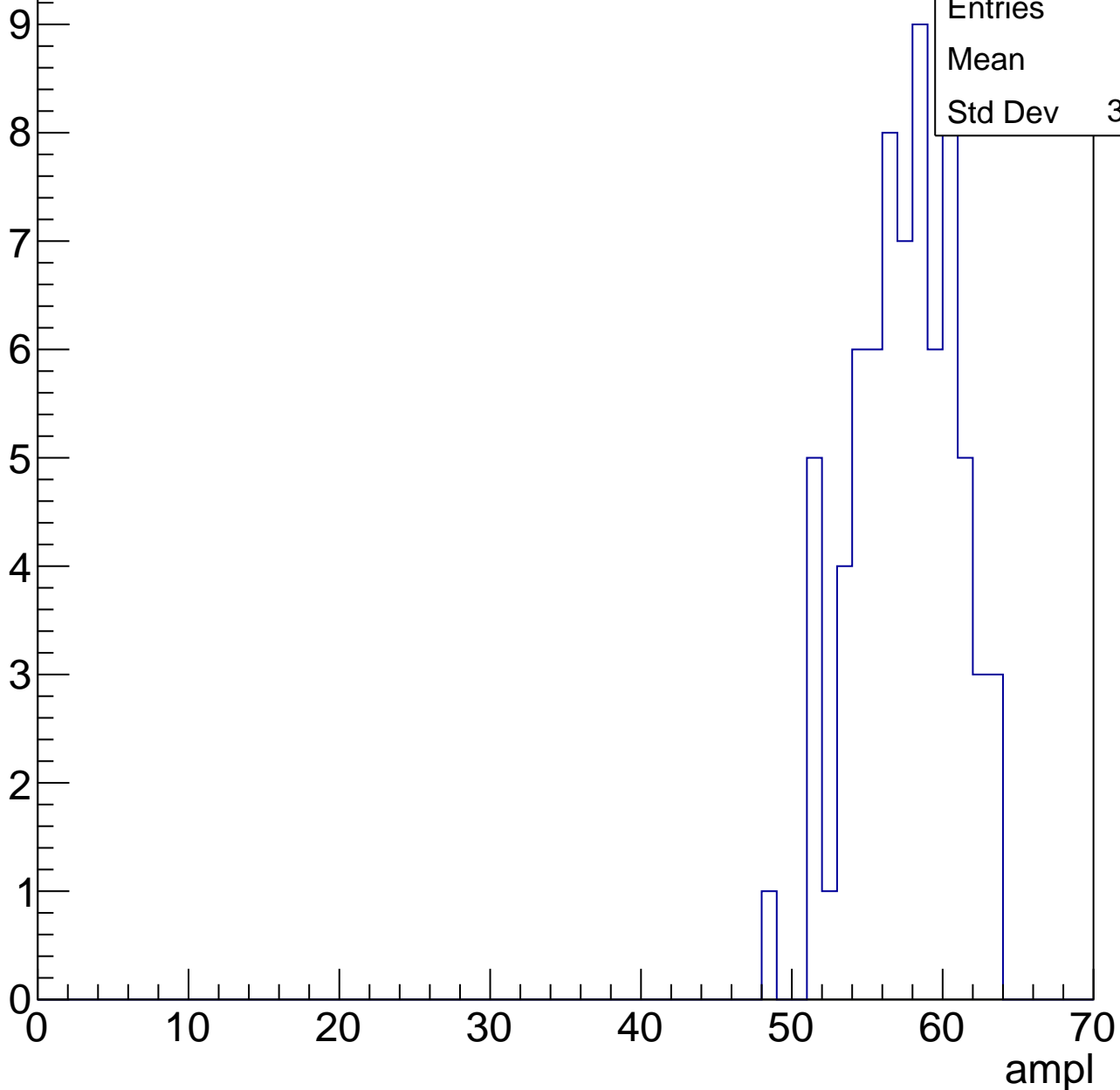
Entries	64
Mean	50.59
Std Dev	3.639



# B1L101S, U22-ch48, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

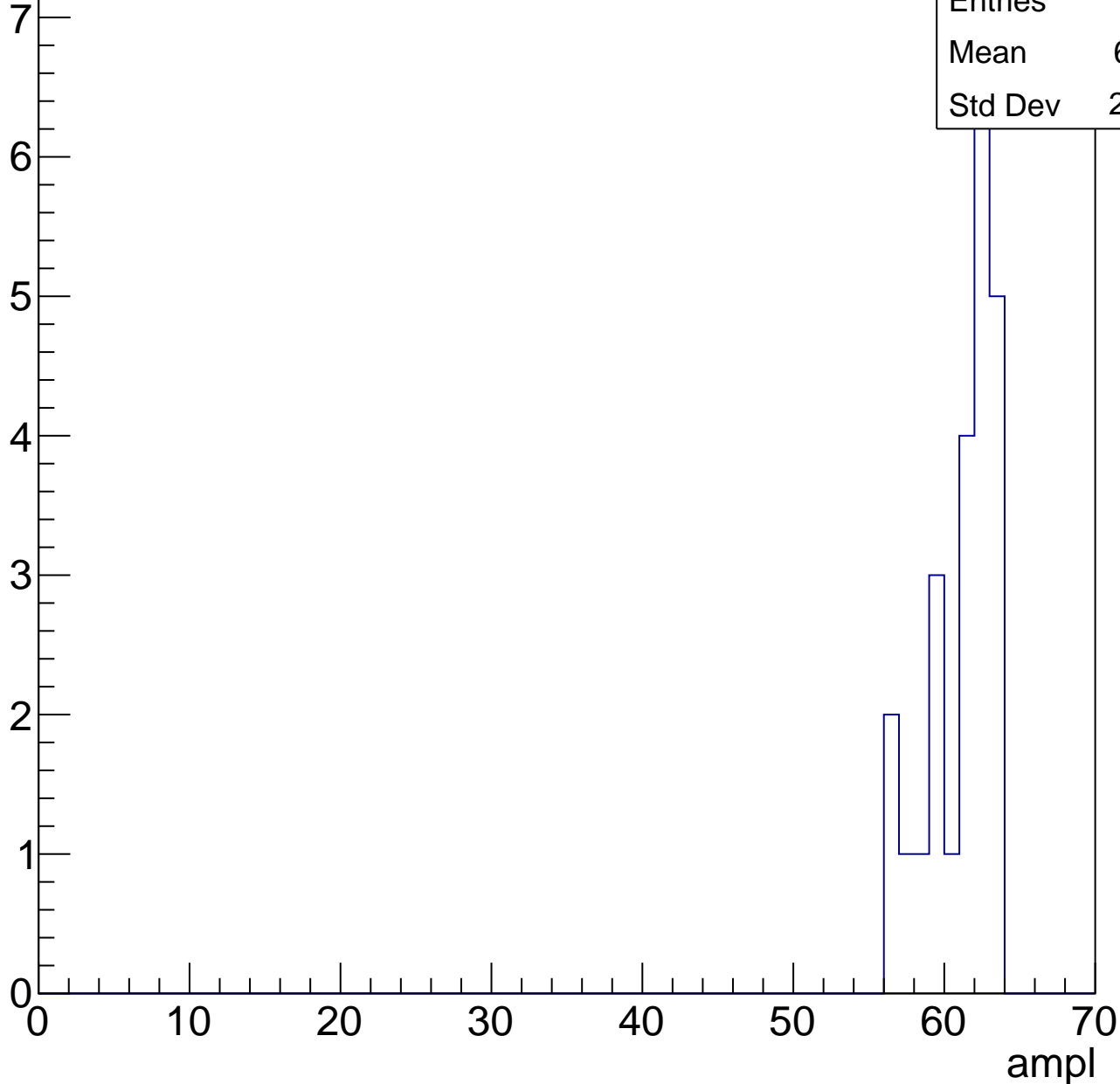


# B1L101S, U22-ch48, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

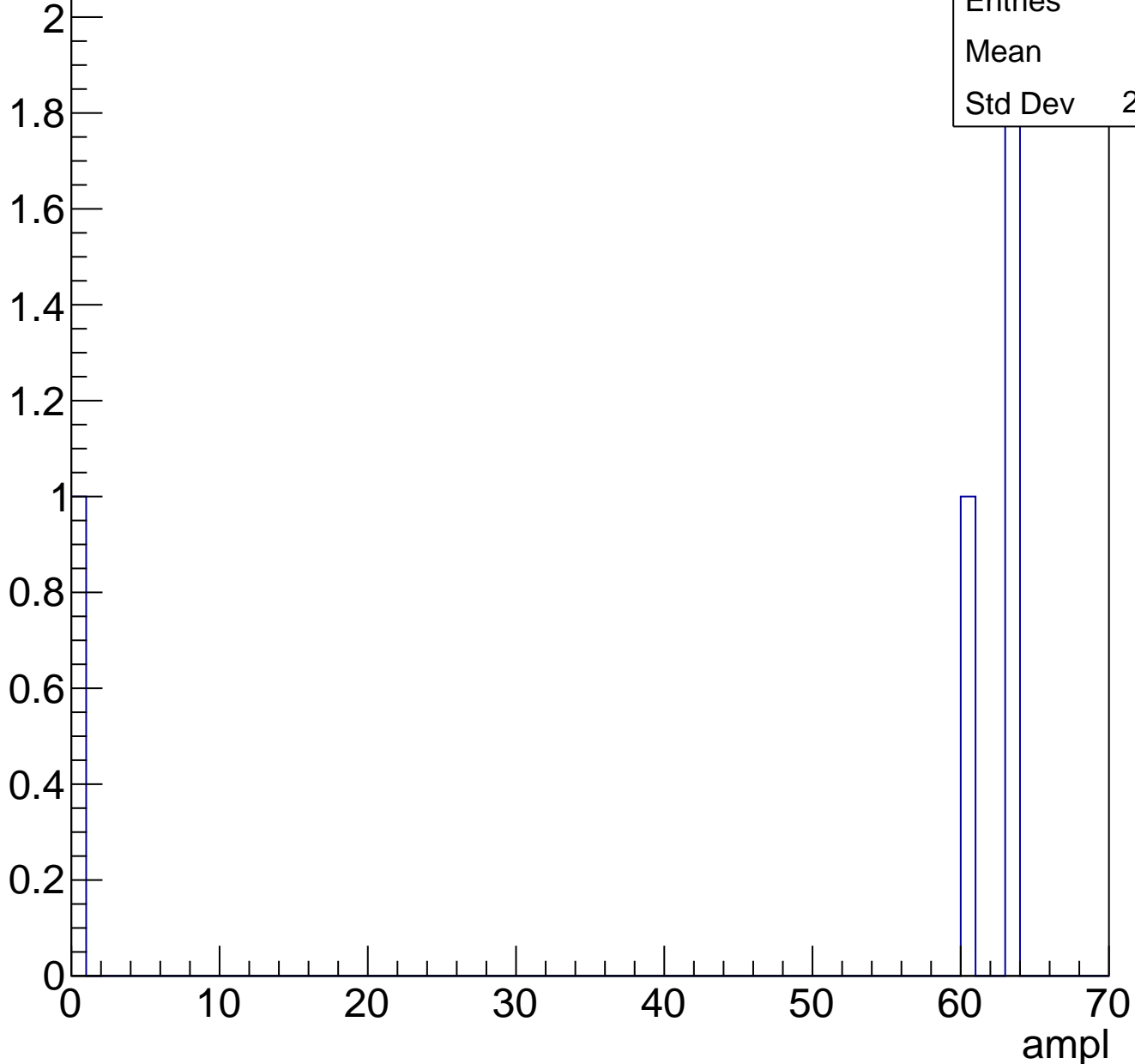
Entries	24
Mean	60.71
Std Dev	2.169



# B1L101S, U22-ch48, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U22-ch48, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U22-ch49, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	99
Mean	28.77
Std Dev	3.318

**Gaus mean : 29.3883**

**Gaus Width: 3.9245**

Entry

10

8

6

4

2

0

0

10

20

30

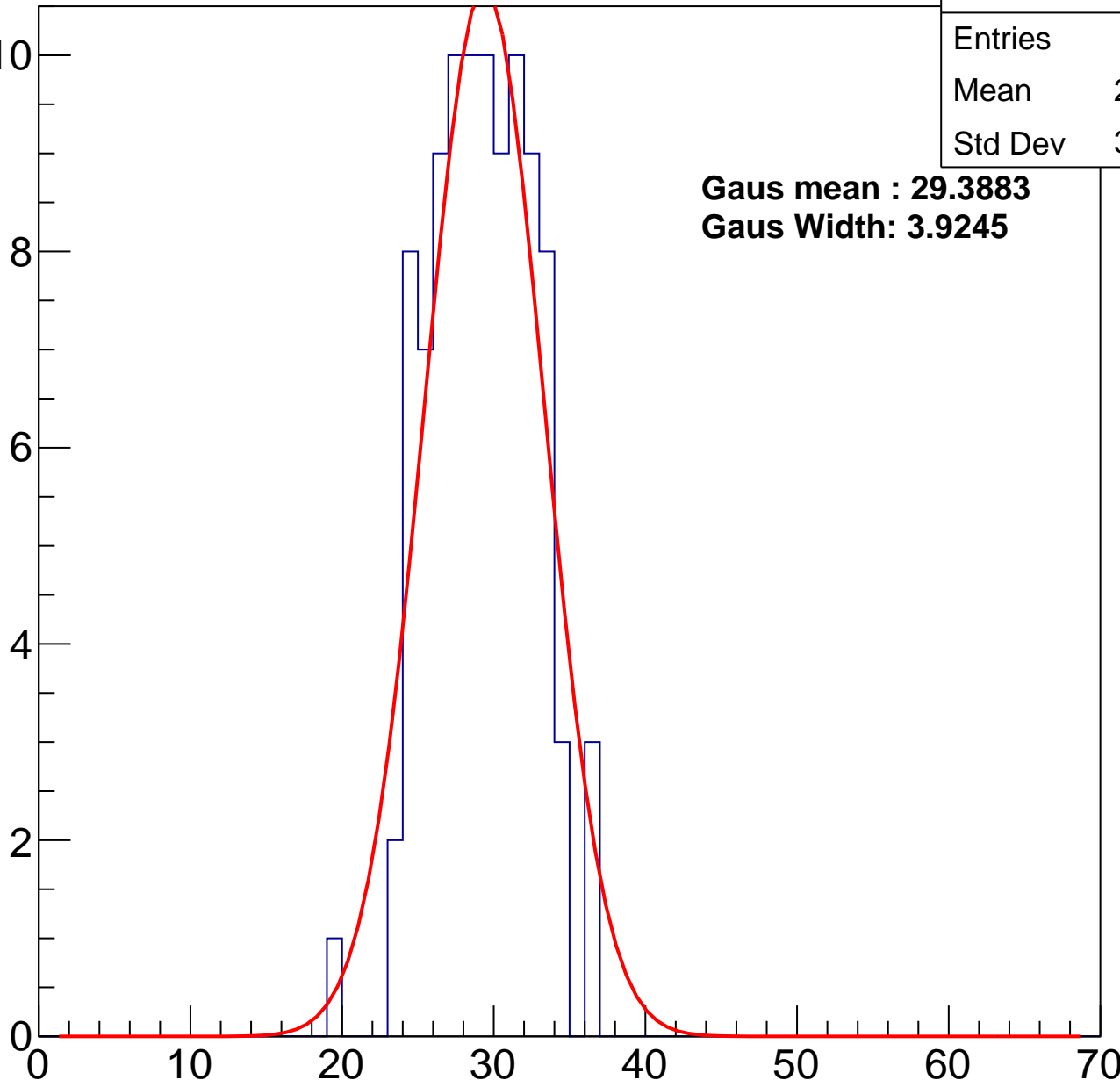
40

50

60

70

ampl



# B1L101S, U22-ch49, adc1

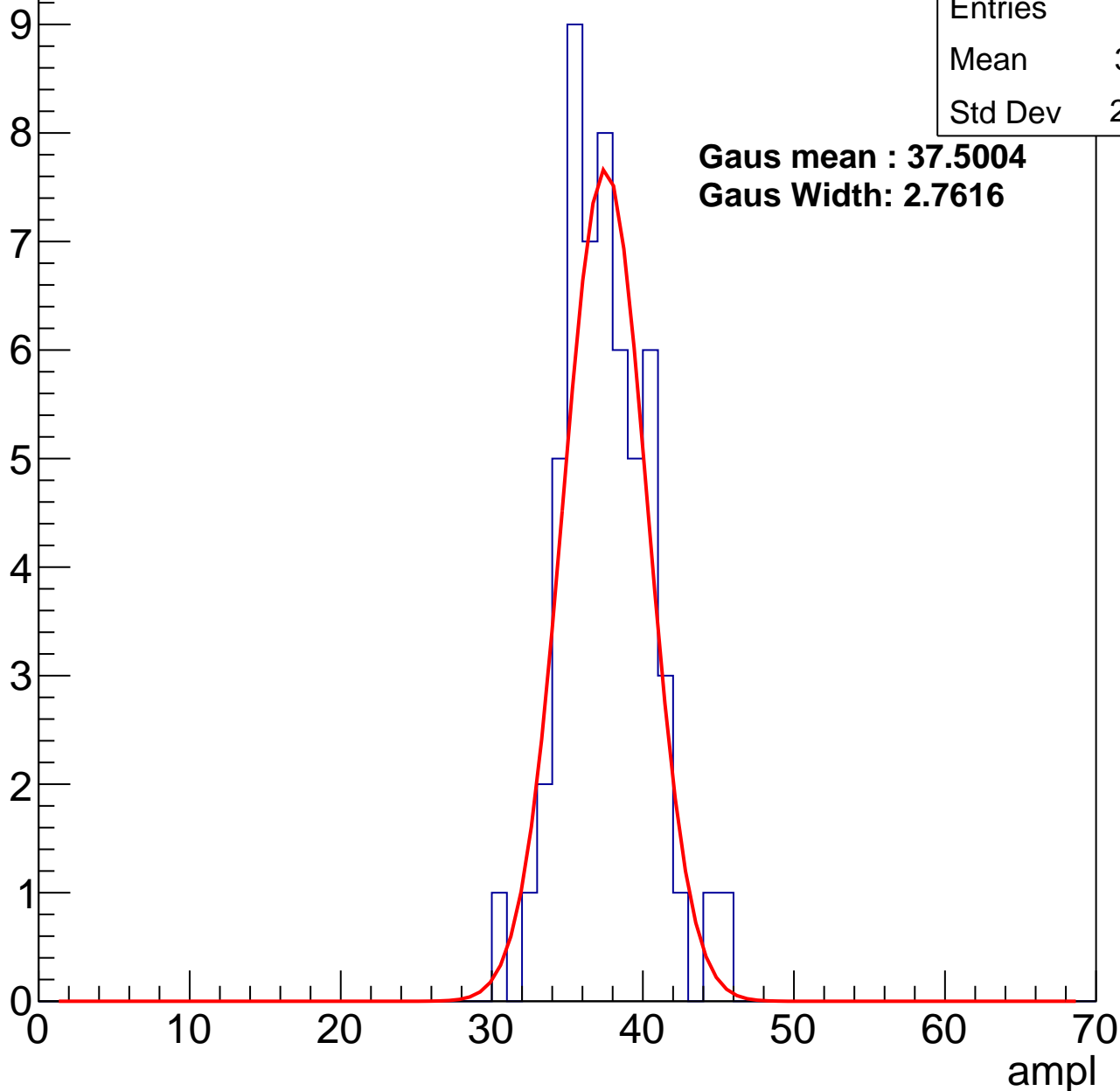
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	56
Mean	37.11
Std Dev	2.864

**Gaus mean : 37.5004**

**Gaus Width: 2.7616**



# B1L101S, U22-ch49, adc2

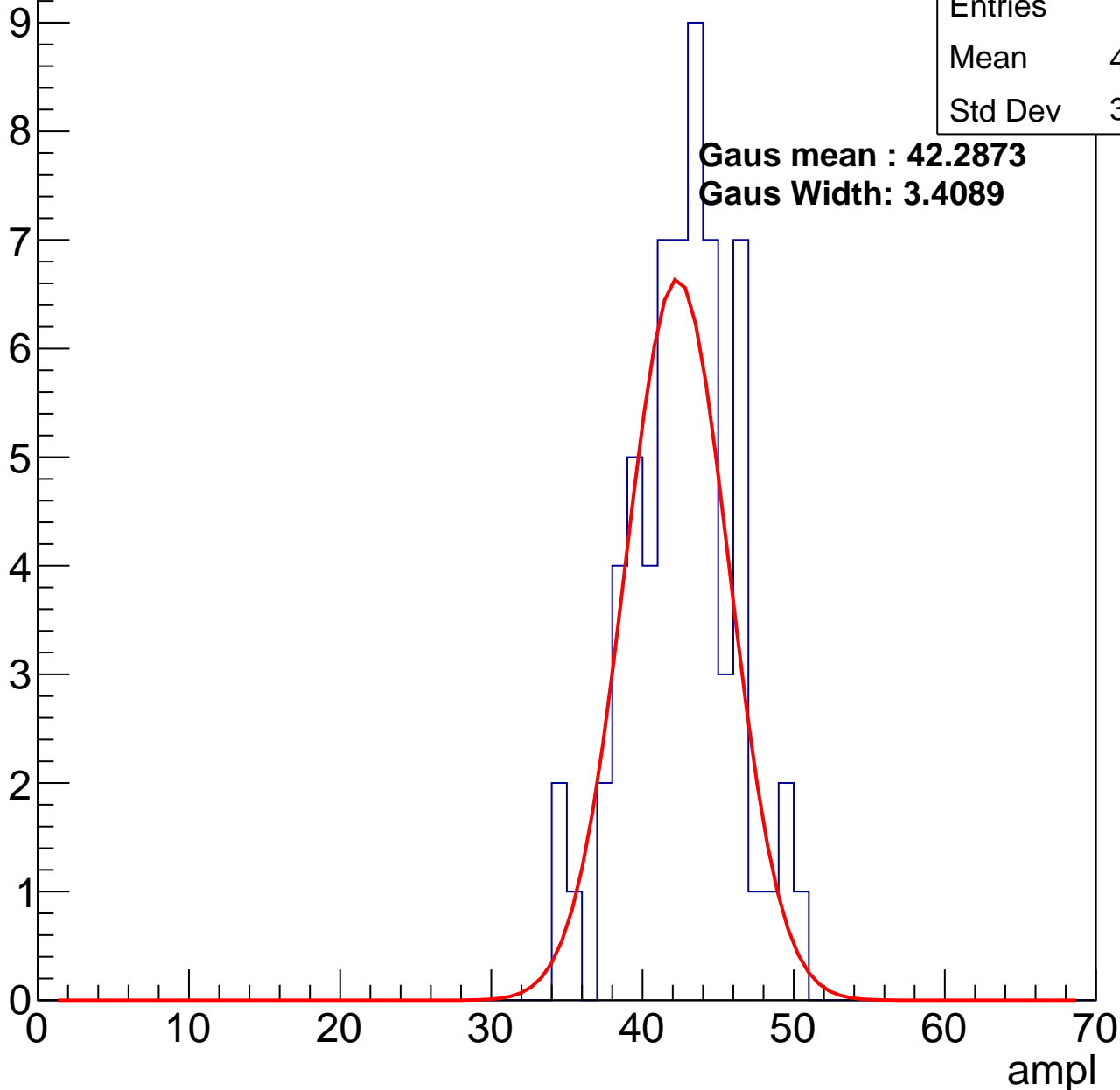
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	42.22
Std Dev	3.462

**Gaus mean : 42.2873**

**Gaus Width: 3.4089**

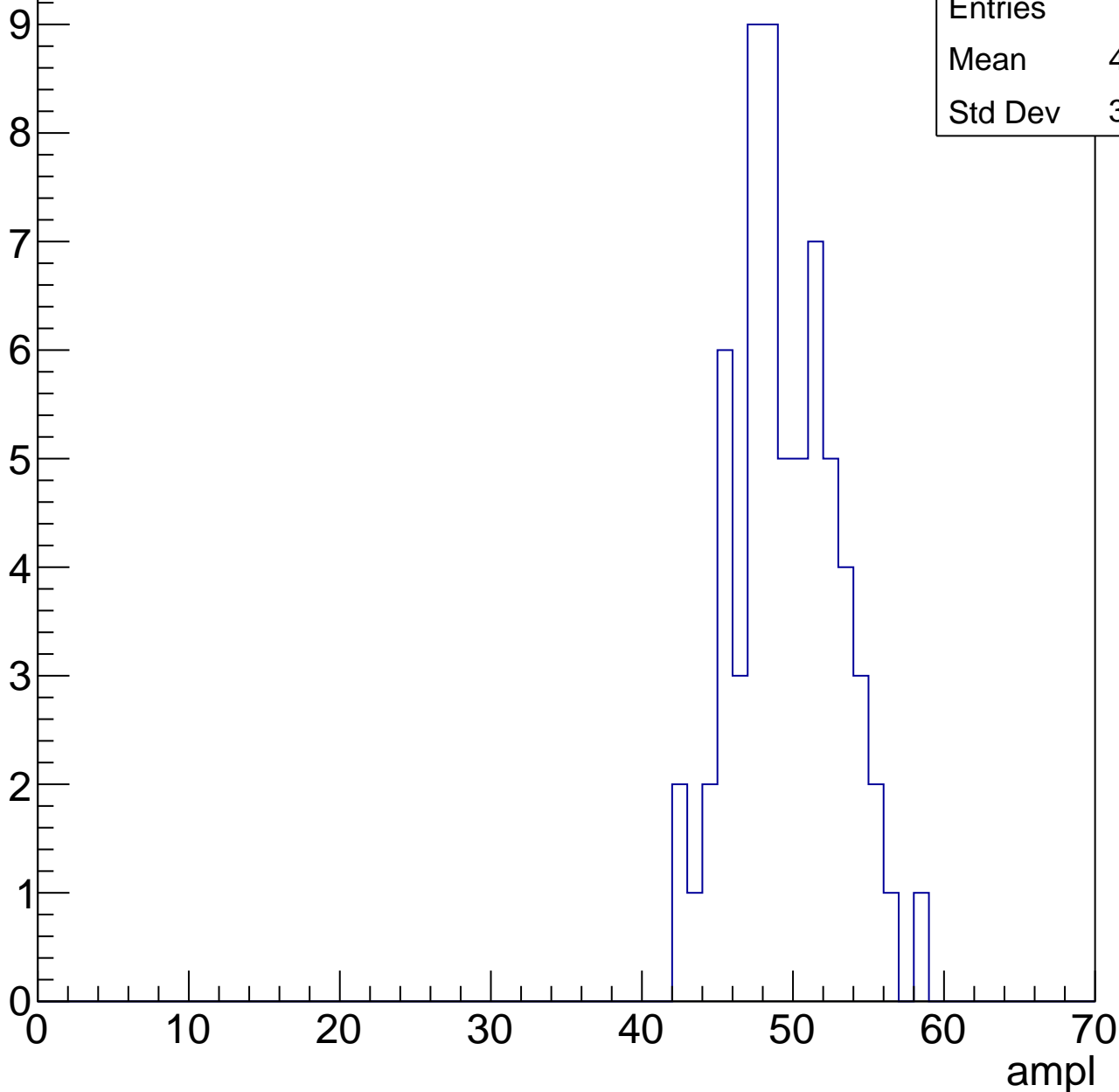


# B1L101S, U22-ch49, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	49.05
Std Dev	3.444

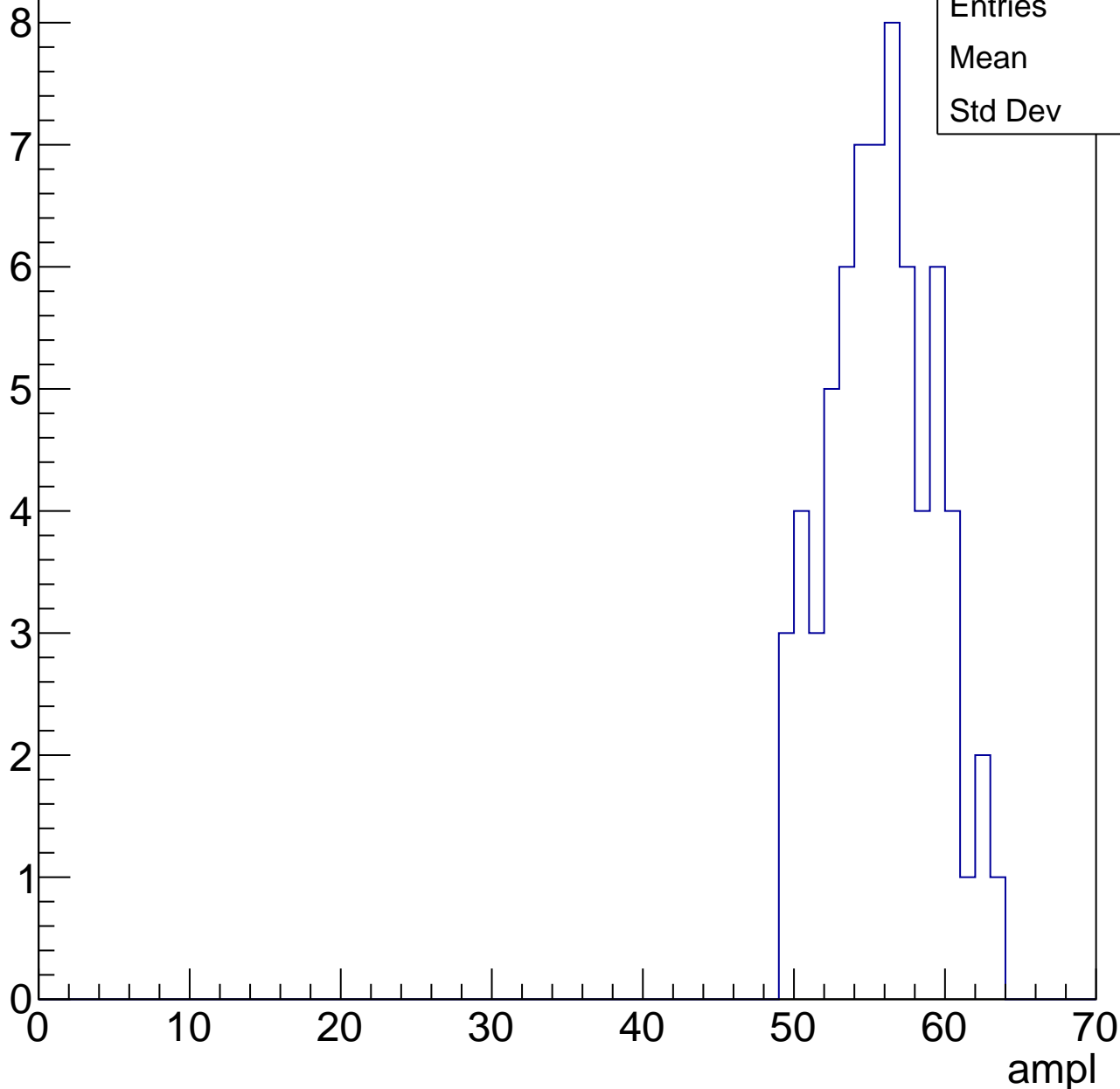


# B1L101S, U22-ch49, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	67
Mean	55.3
Std Dev	3.43



# B1L101S, U22-ch49, adc5

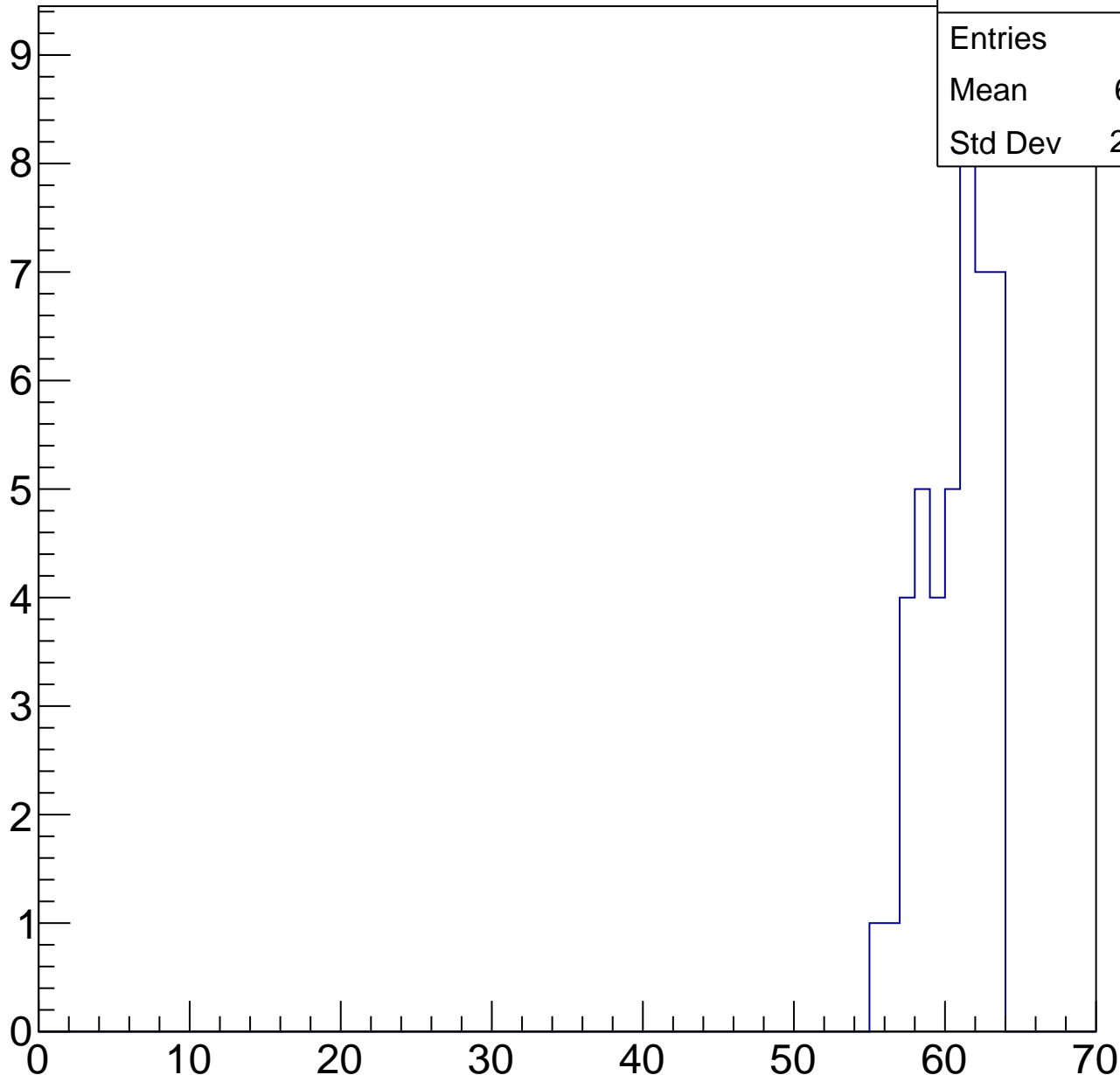
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	43
Mean	60.21
Std Dev	2.152

ampl



# B1L101S, U22-ch49, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

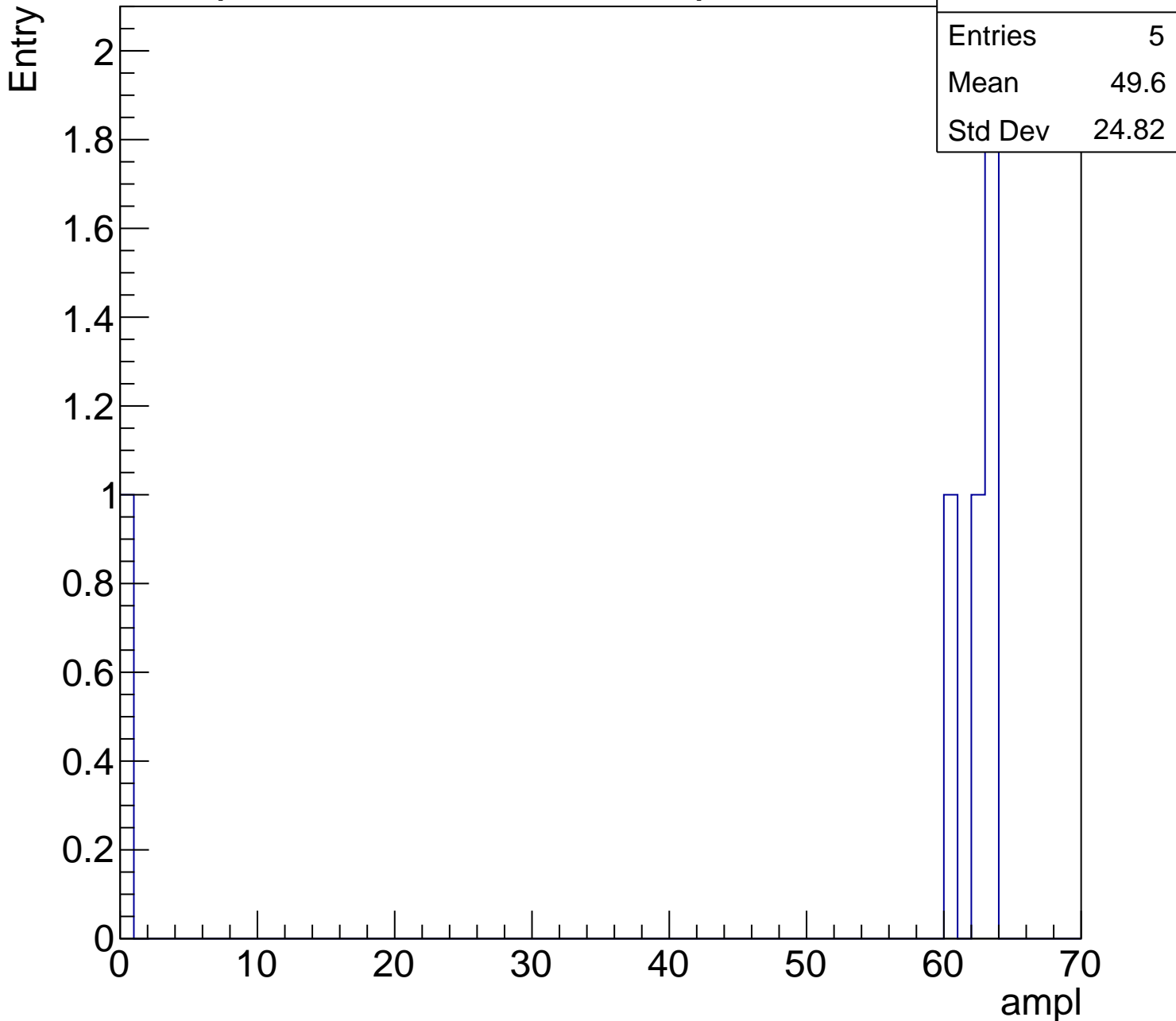
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	5
Mean	49.6
Std Dev	24.82

0 10 20 30 40 50 60 70

ampl





# B1L101S, U22-ch49, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L101S, U22-ch50, adc0

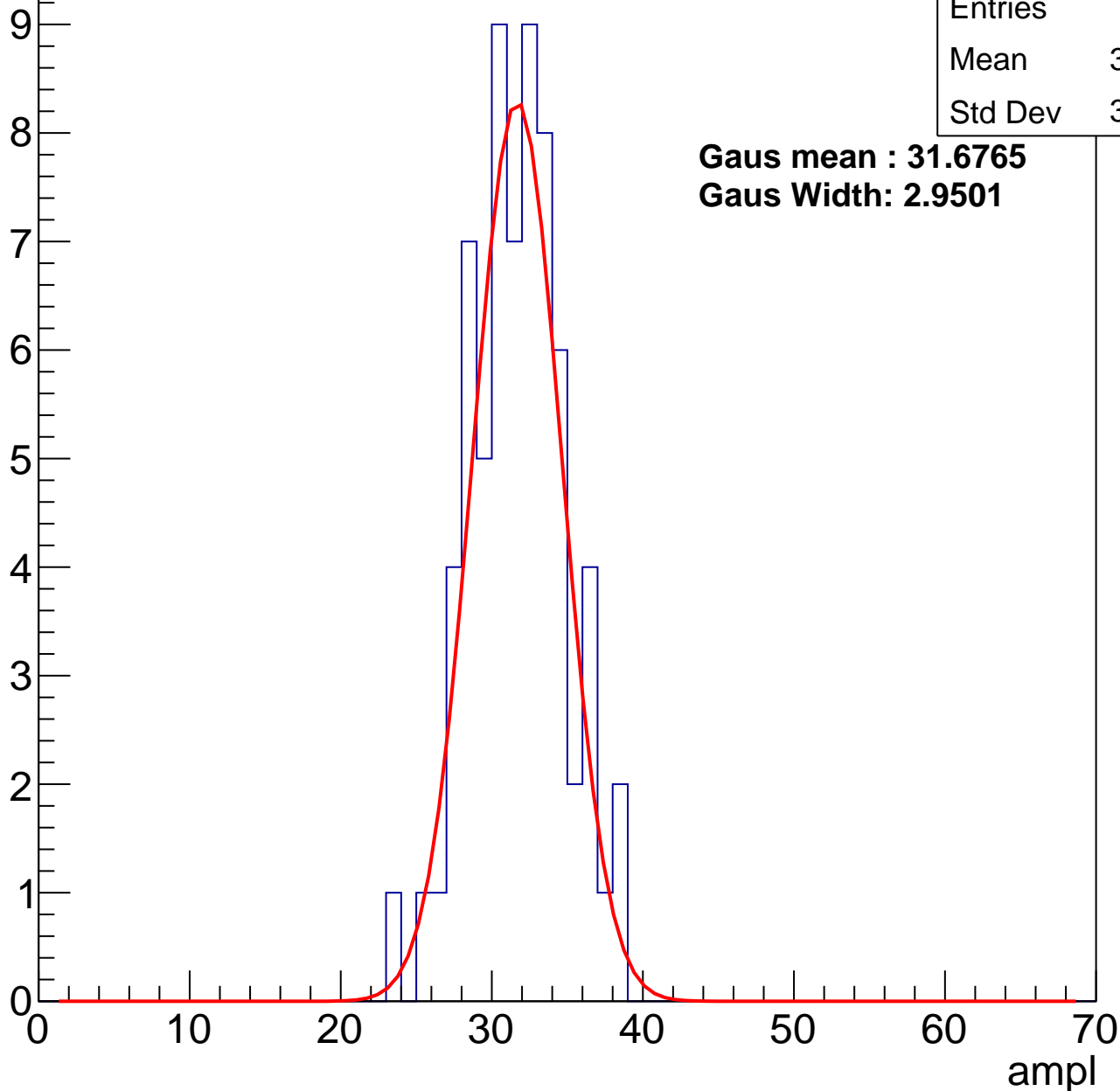
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	67
Mean	31.24
Std Dev	3.086

**Gaus mean : 31.6765**

**Gaus Width: 2.9501**



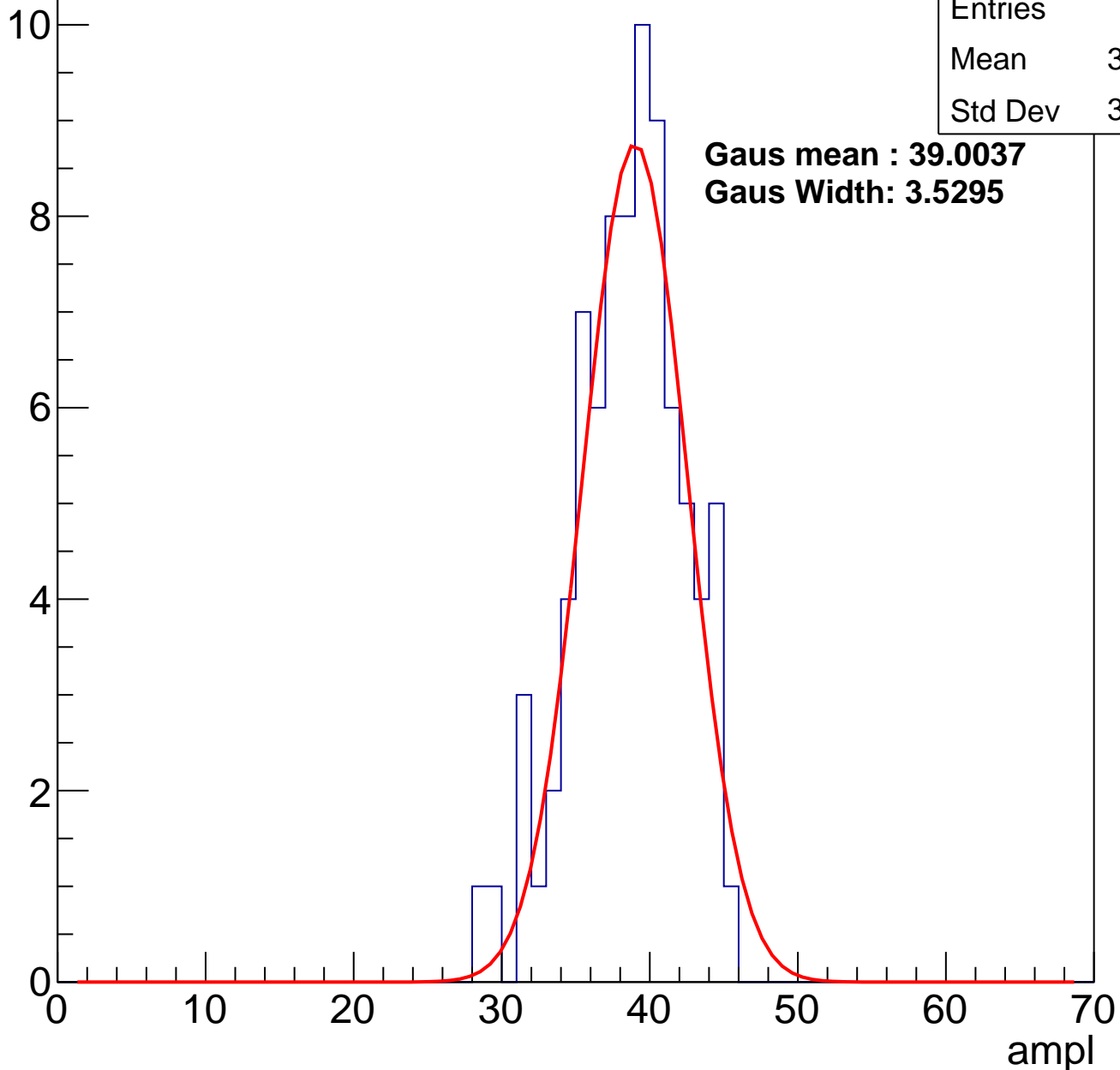
# B1L101S, U22-ch50, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	81
Mean	38.12
Std Dev	3.653

**Gaus mean : 39.0037**  
**Gaus Width: 3.5295**

Entry



# B1L101S, U22-ch50, adc2

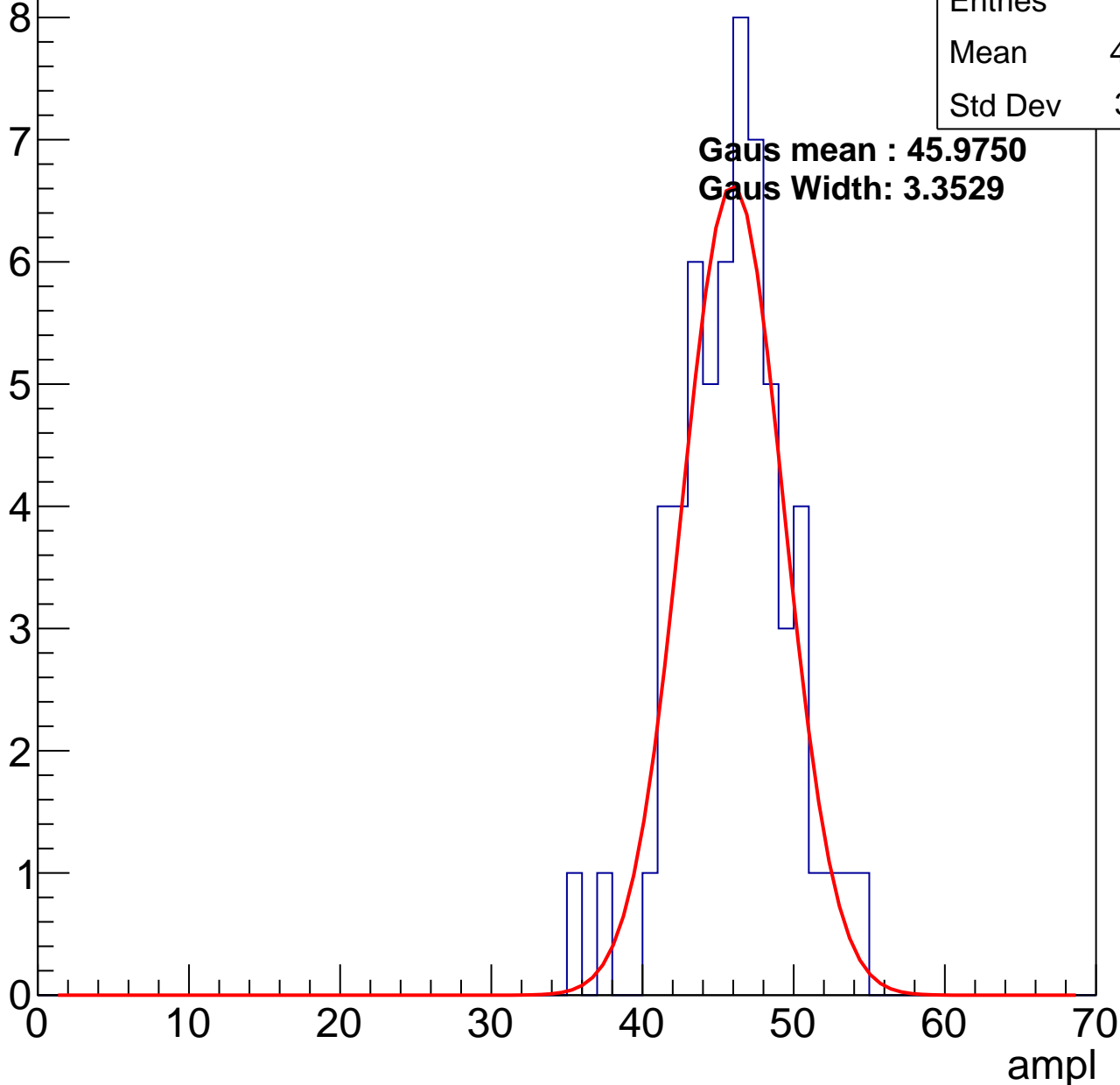
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	59
Mean	45.53
Std Dev	3.591

**Gaus mean : 45.9750**

**Gaus Width: 3.3529**

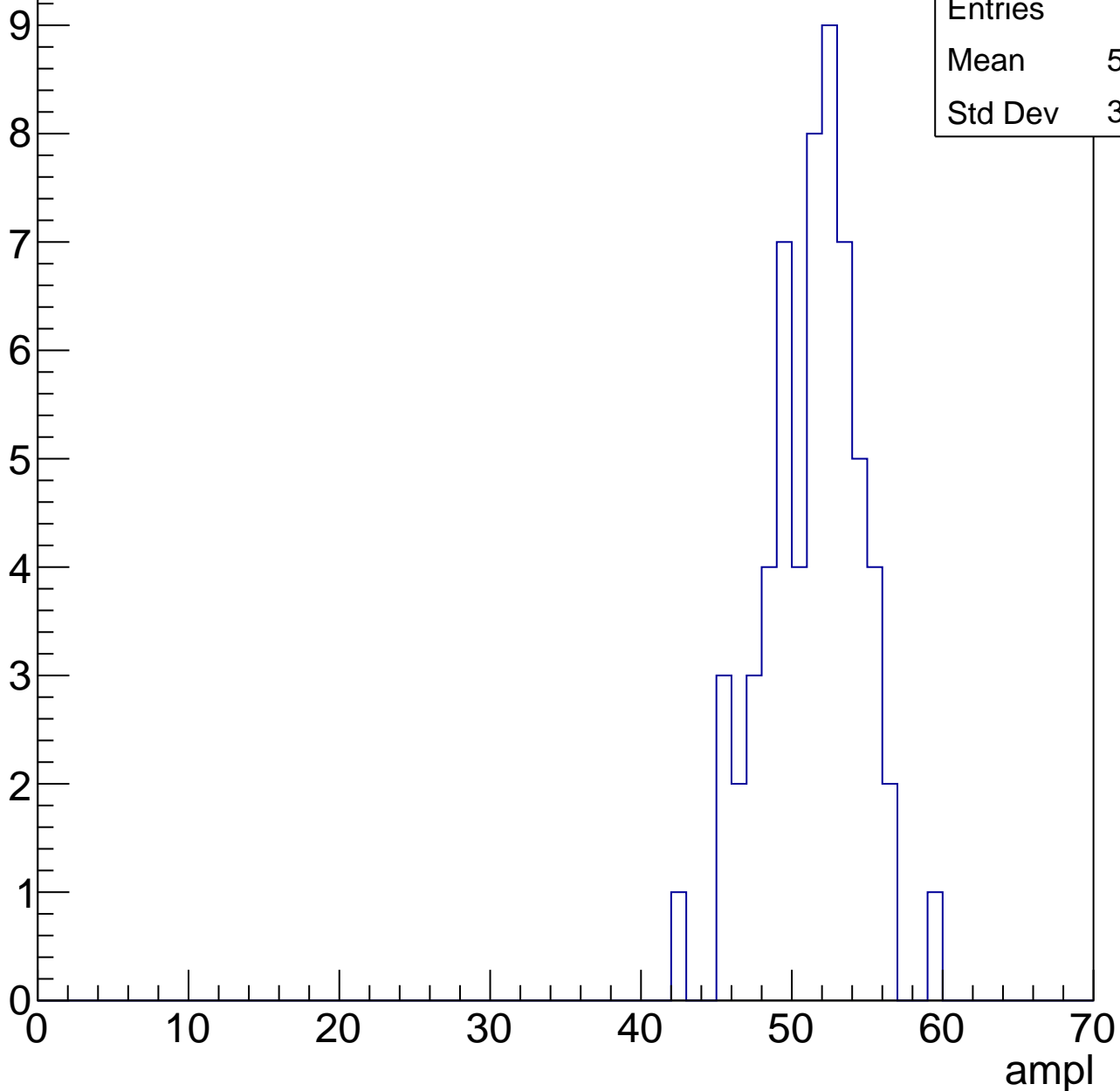


# B1L101S, U22-ch50, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

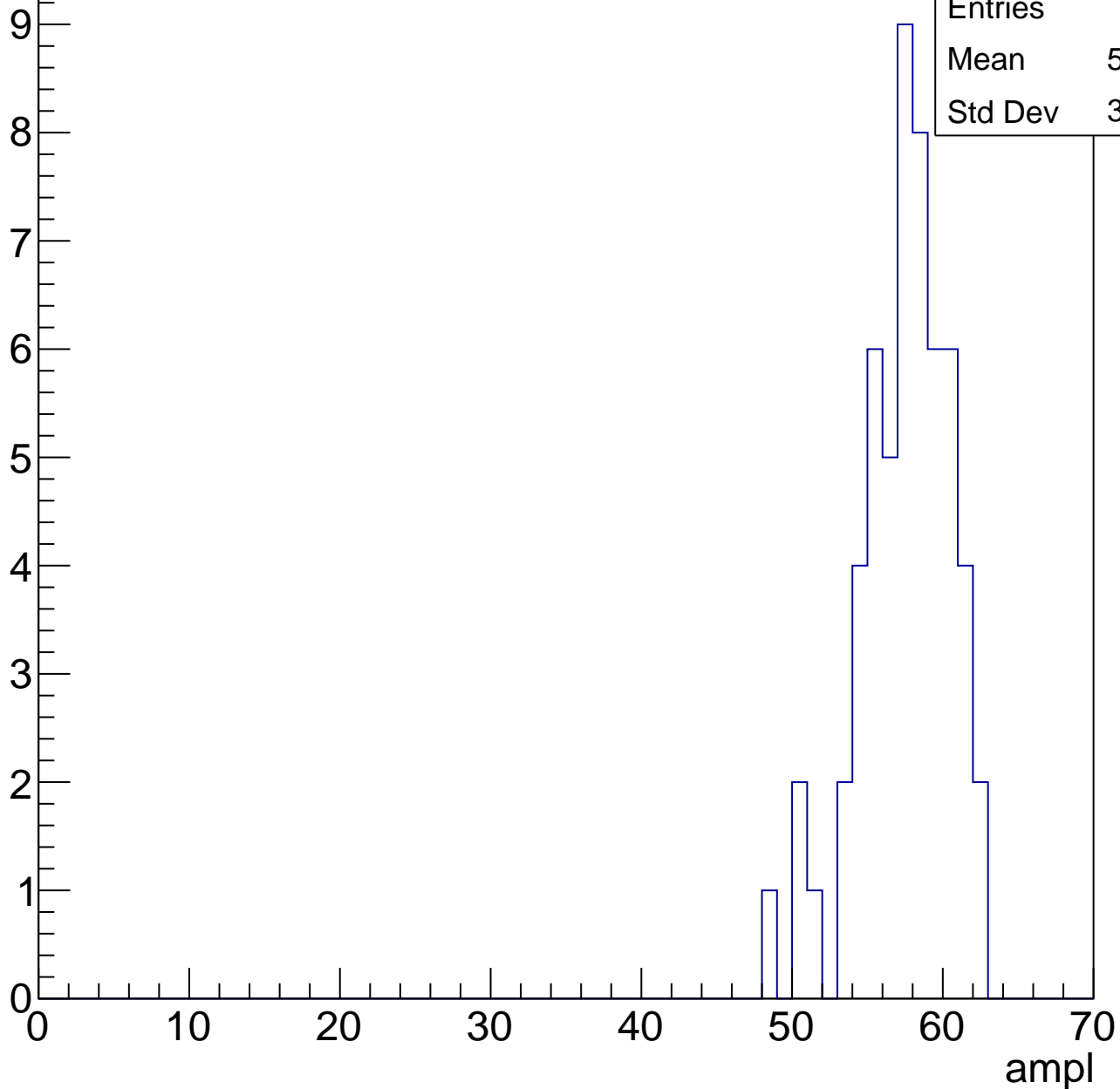
Entries	60
Mean	50.88
Std Dev	3.199



# B1L101S, U22-ch50, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

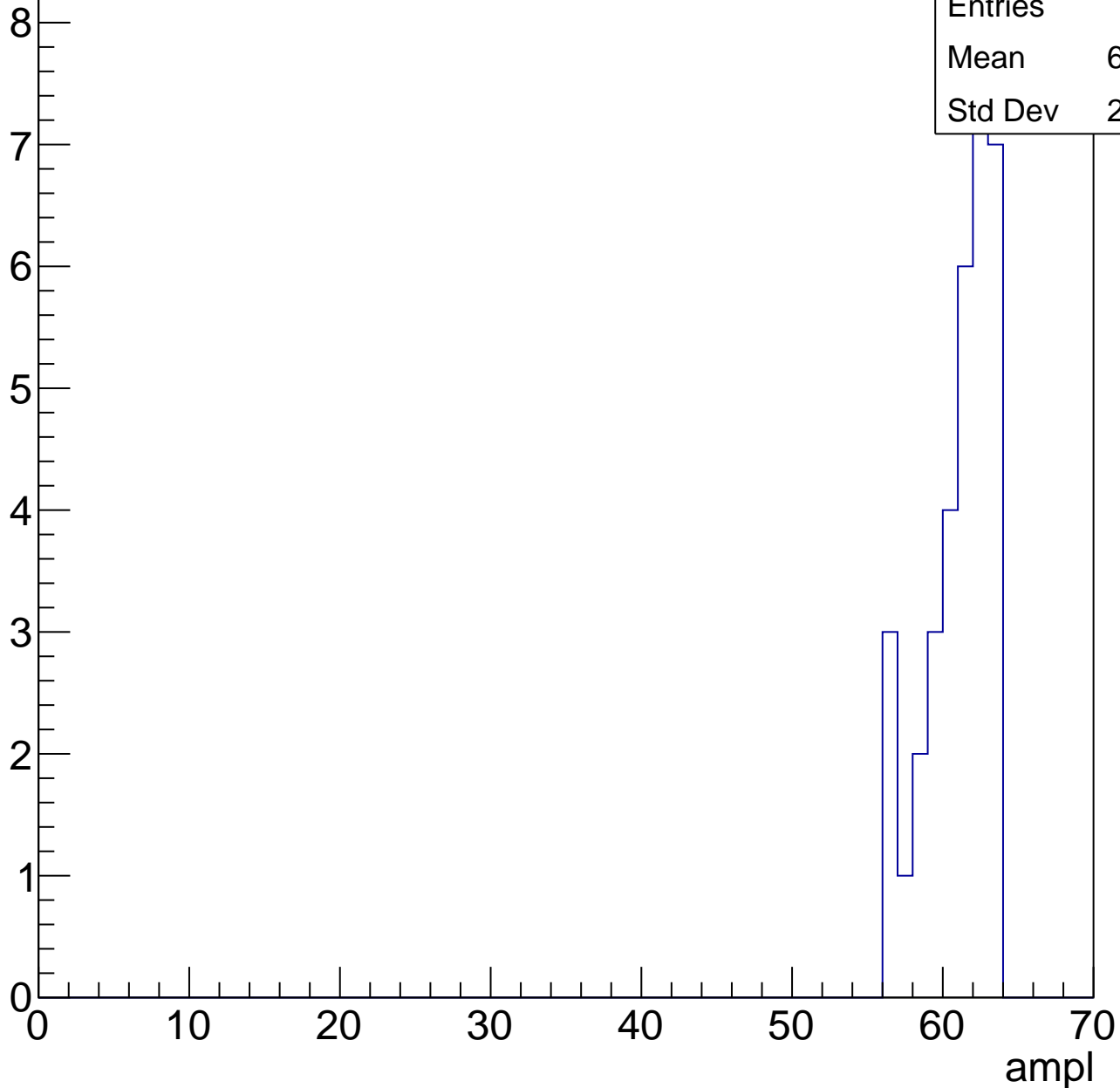


# B1L101S, U22-ch50, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

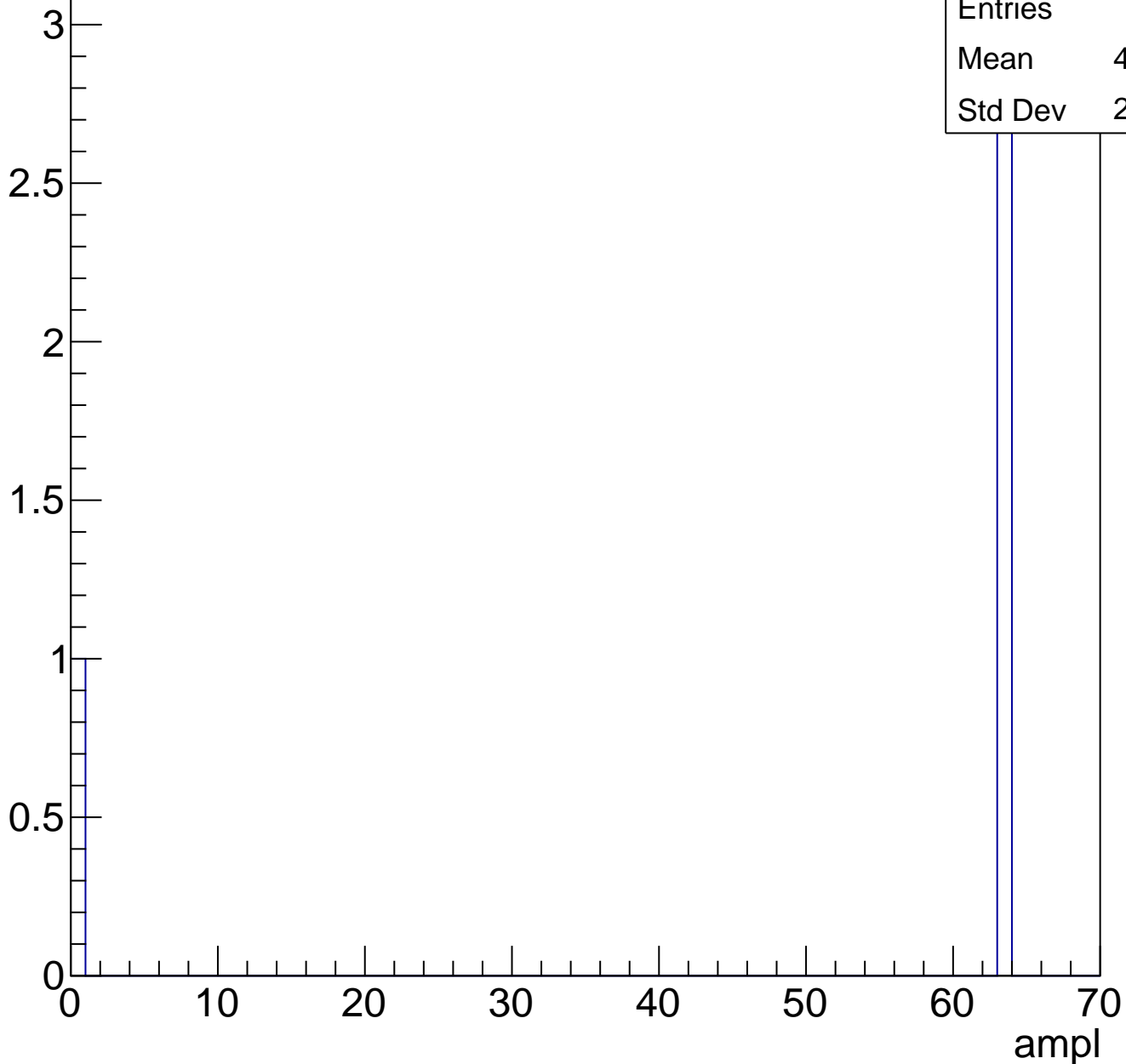
Entries	34
Mean	60.62
Std Dev	2.142



# B1L101S, U22-ch50, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U22-ch50, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L101S, U22-ch51, adc0

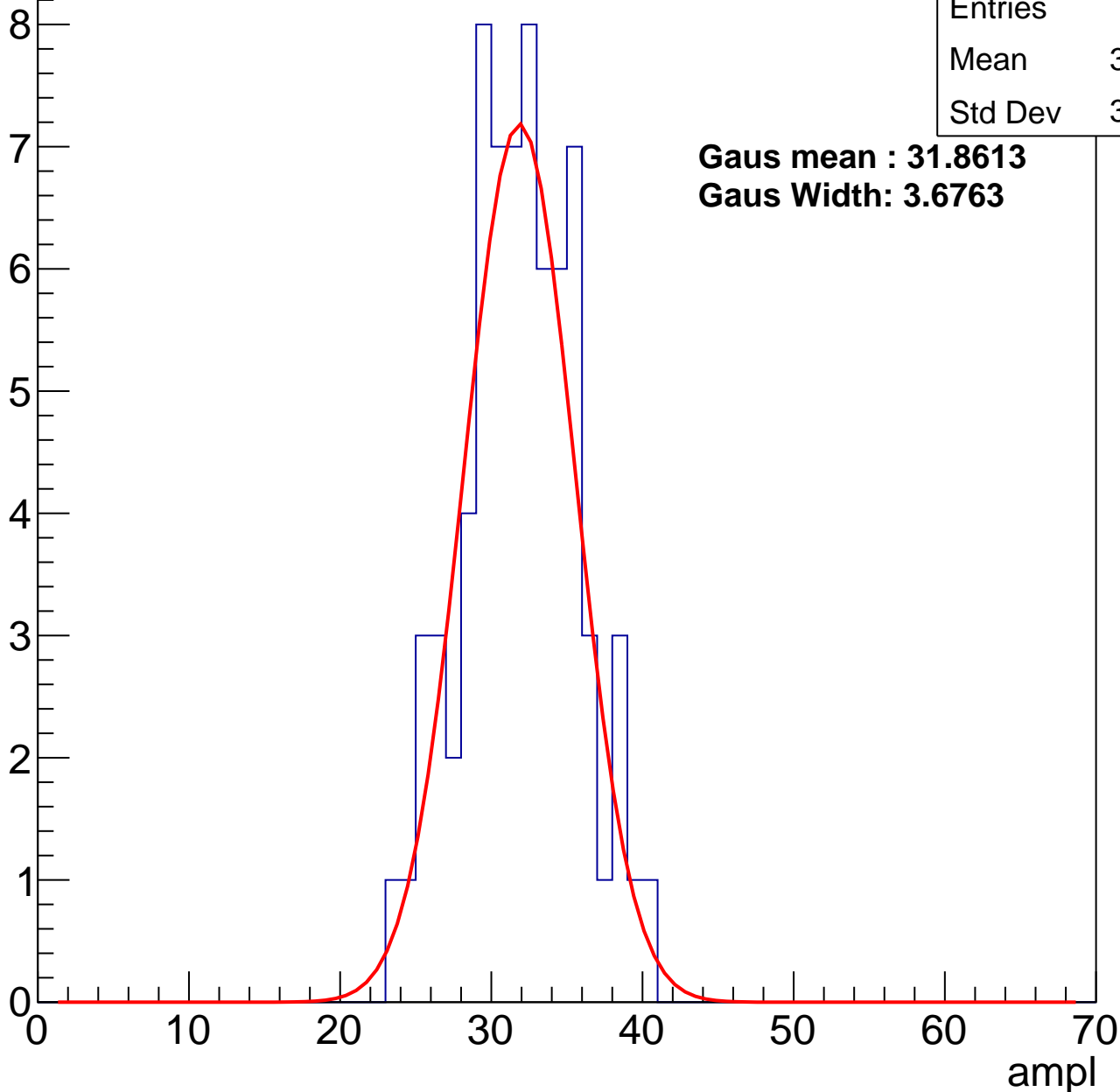
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	72
Mean	31.47
Std Dev	3.704

**Gaus mean : 31.8613**

**Gaus Width: 3.6763**



# B1L101S, U22-ch51, adc1

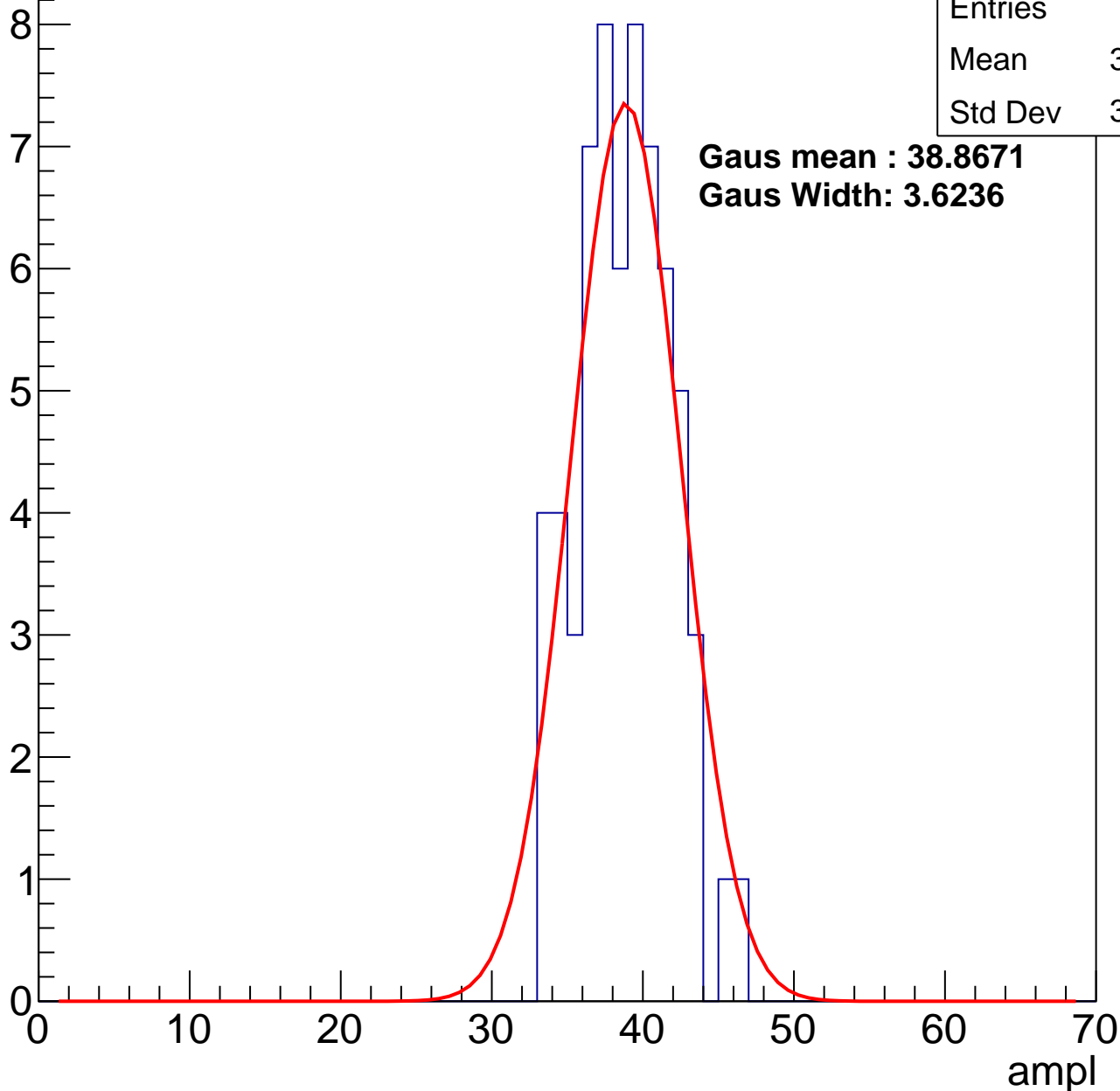
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	38.37
Std Dev	3.025

**Gaus mean : 38.8671**

**Gaus Width: 3.6236**



# B1L101S, U22-ch51, adc2

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	44.65
Std Dev	3.009

**Gaus mean : 45.4405**

**Gaus Width: 3.1592**

10

8

6

4

2

0

0

2

4

6

8

10

ampl

0

10

20

30

40

50

60

70

# B1L101S, U22-ch51, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	57
Mean	50.84
Std Dev	2.943

Entry

10

8

6

4

2

0

0

10

20

30

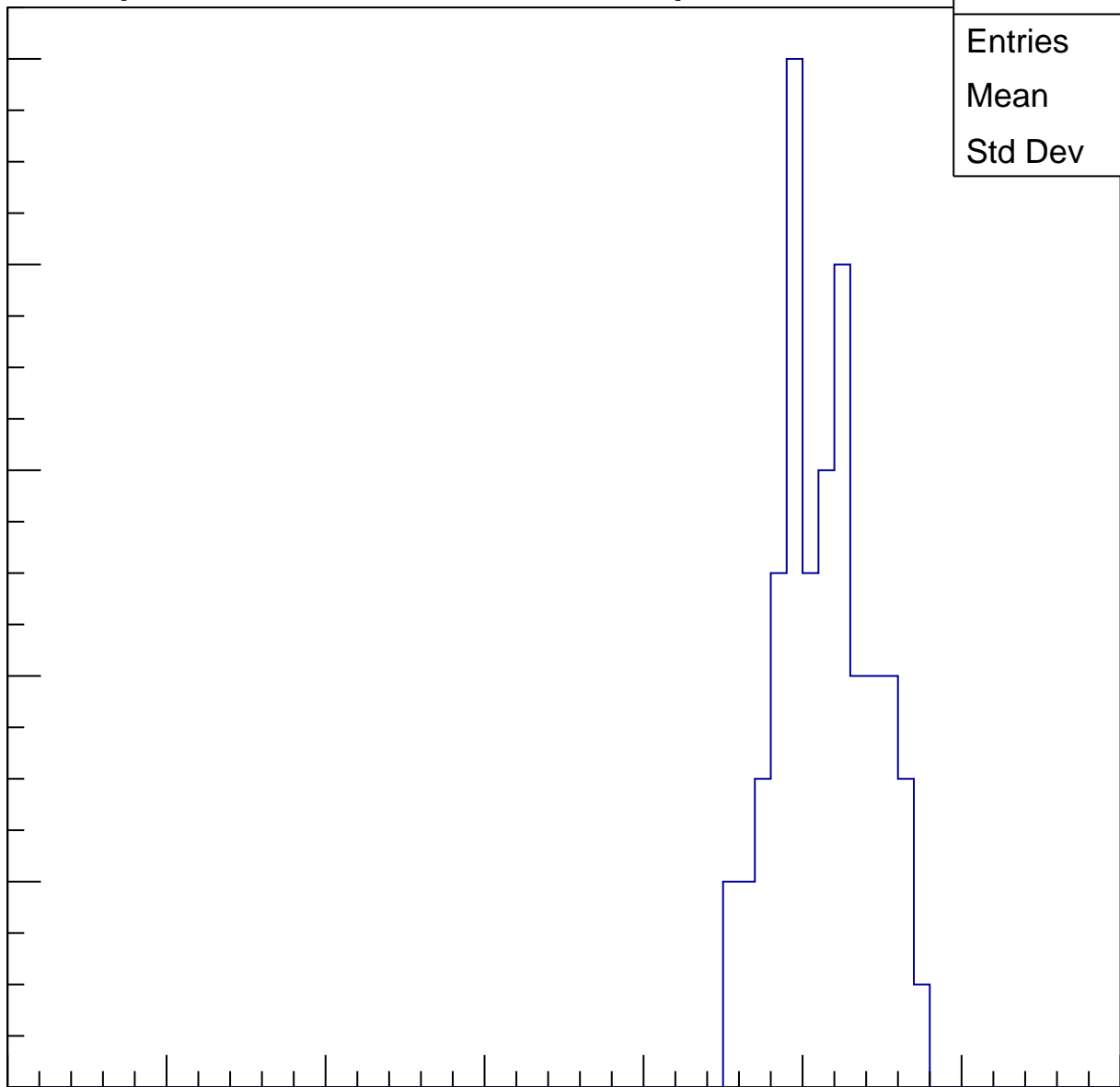
40

50

60

70

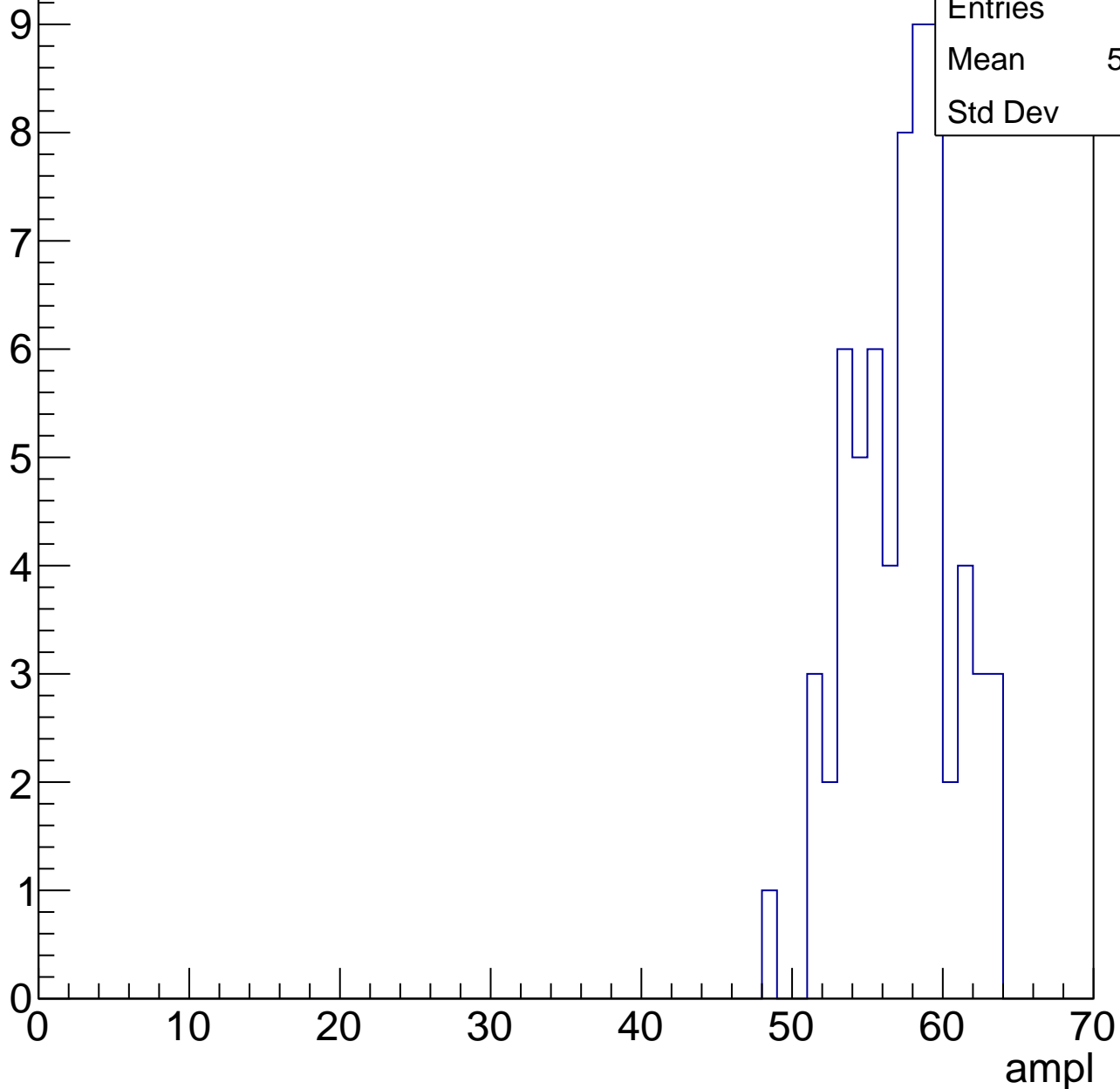
ampl



# B1L101S, U22-ch51, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

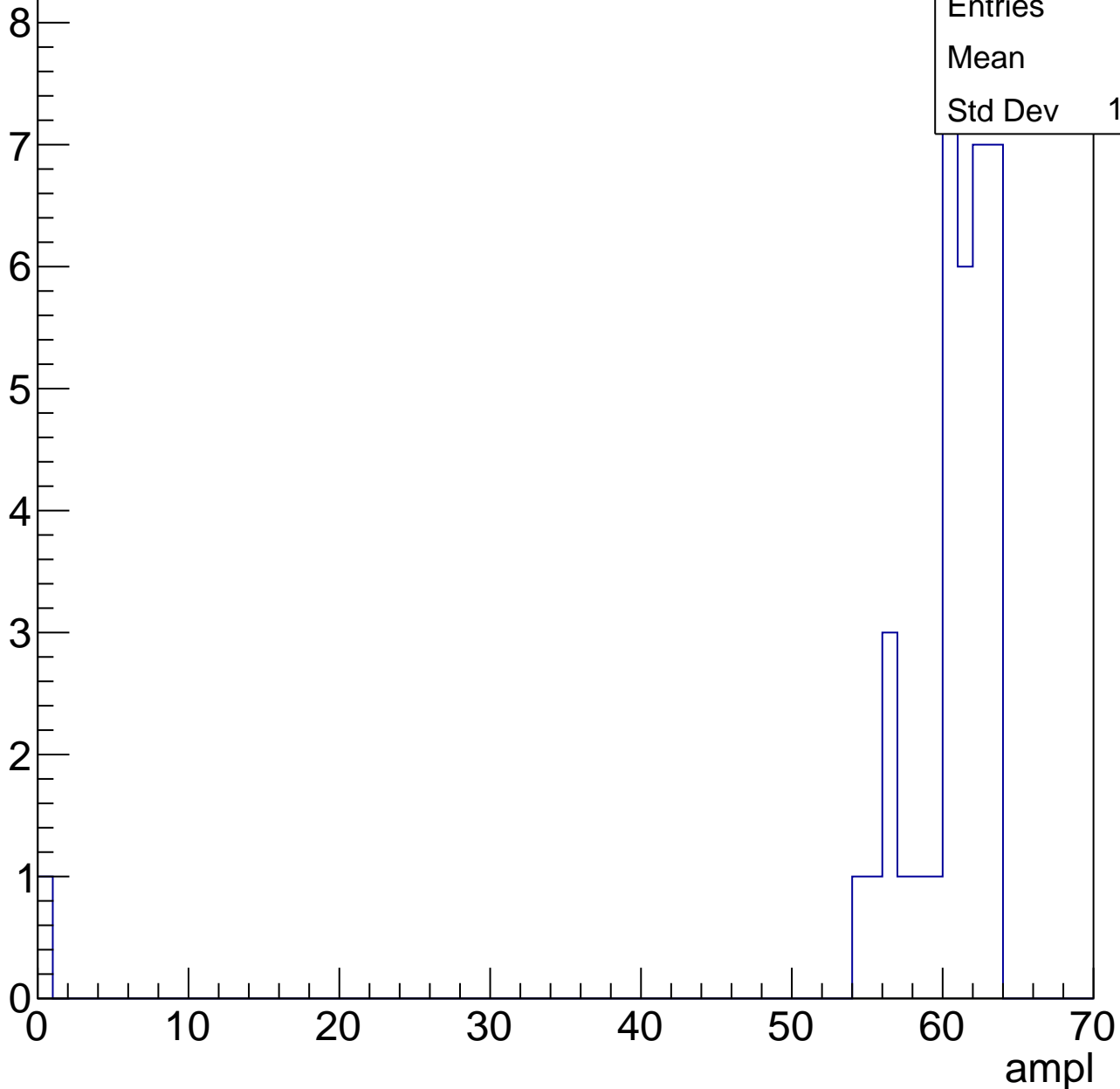


# B1L101S, U22-ch51, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	37
Mean	58.7
Std Dev	10.08



# B1L101S, U22-ch51, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0



# B1L101S, U22-ch51, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U22-ch52, adc0

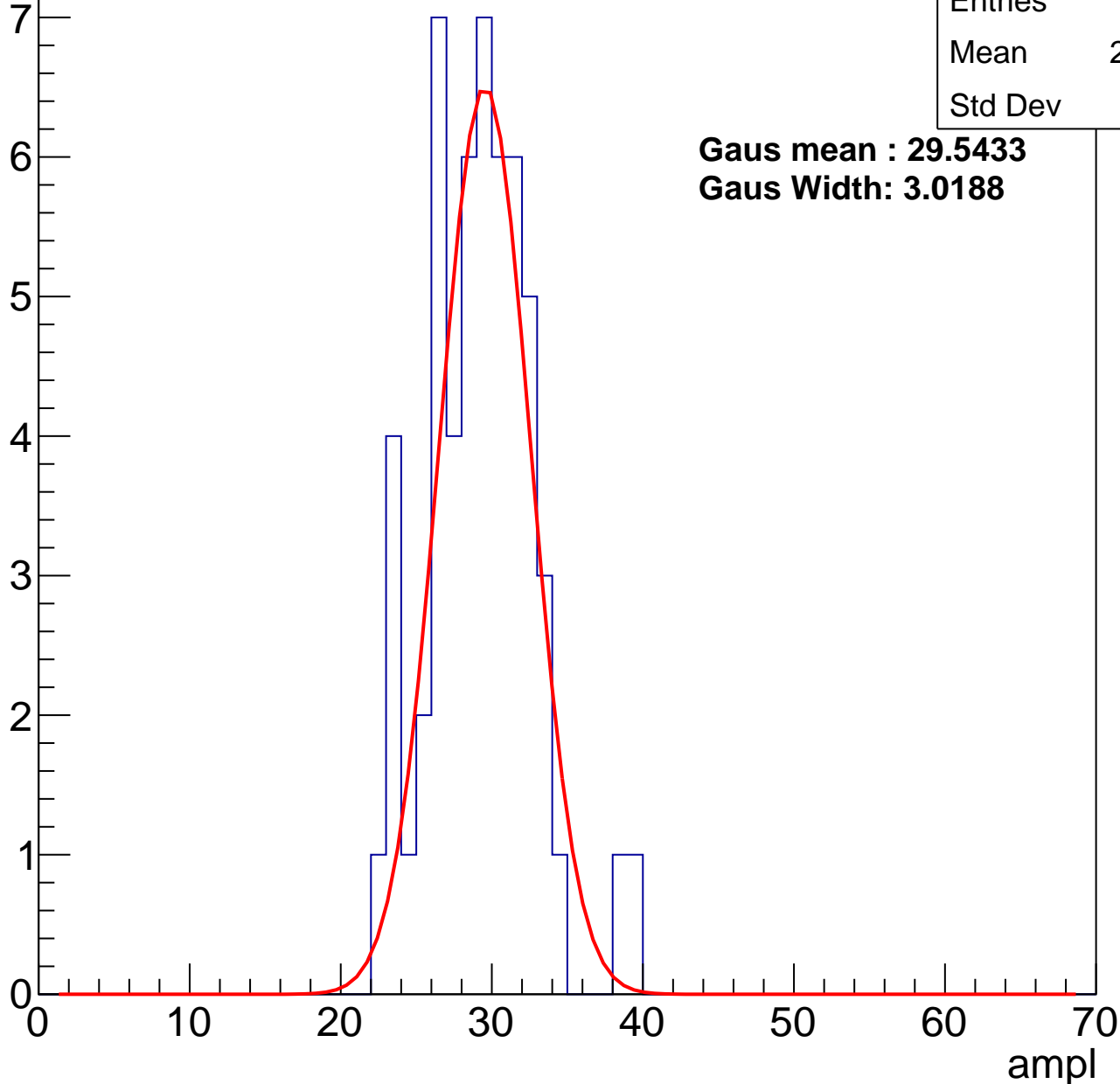
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	55
Mean	28.82
Std Dev	3.47

**Gaus mean : 29.5433**

**Gaus Width: 3.0188**



# B1L101S, U22-ch52, adc1

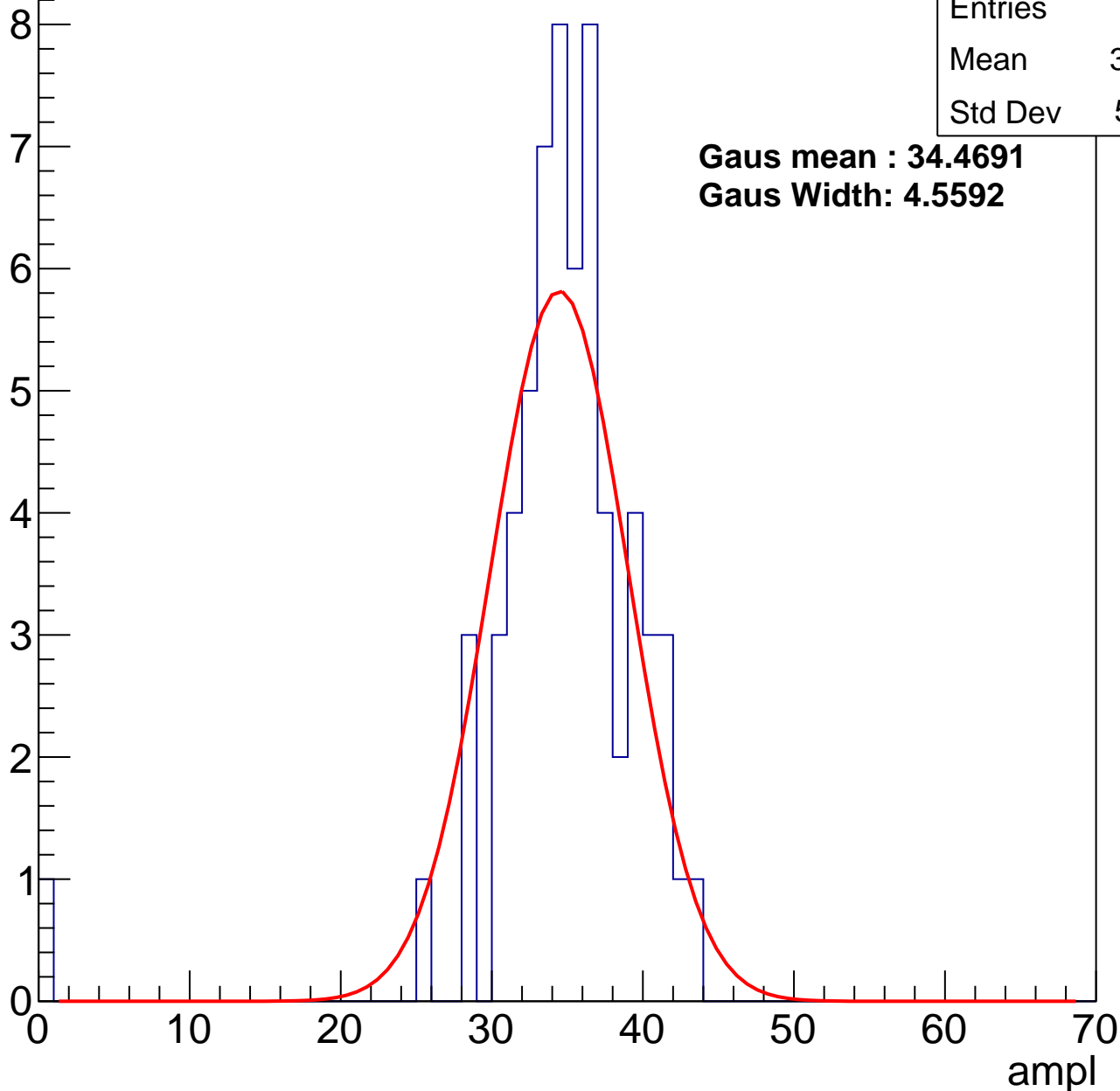
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	34.25
Std Dev	5.671

**Gaus mean : 34.4691**

**Gaus Width: 4.5592**



# B1L101S, U22-ch52, adc2

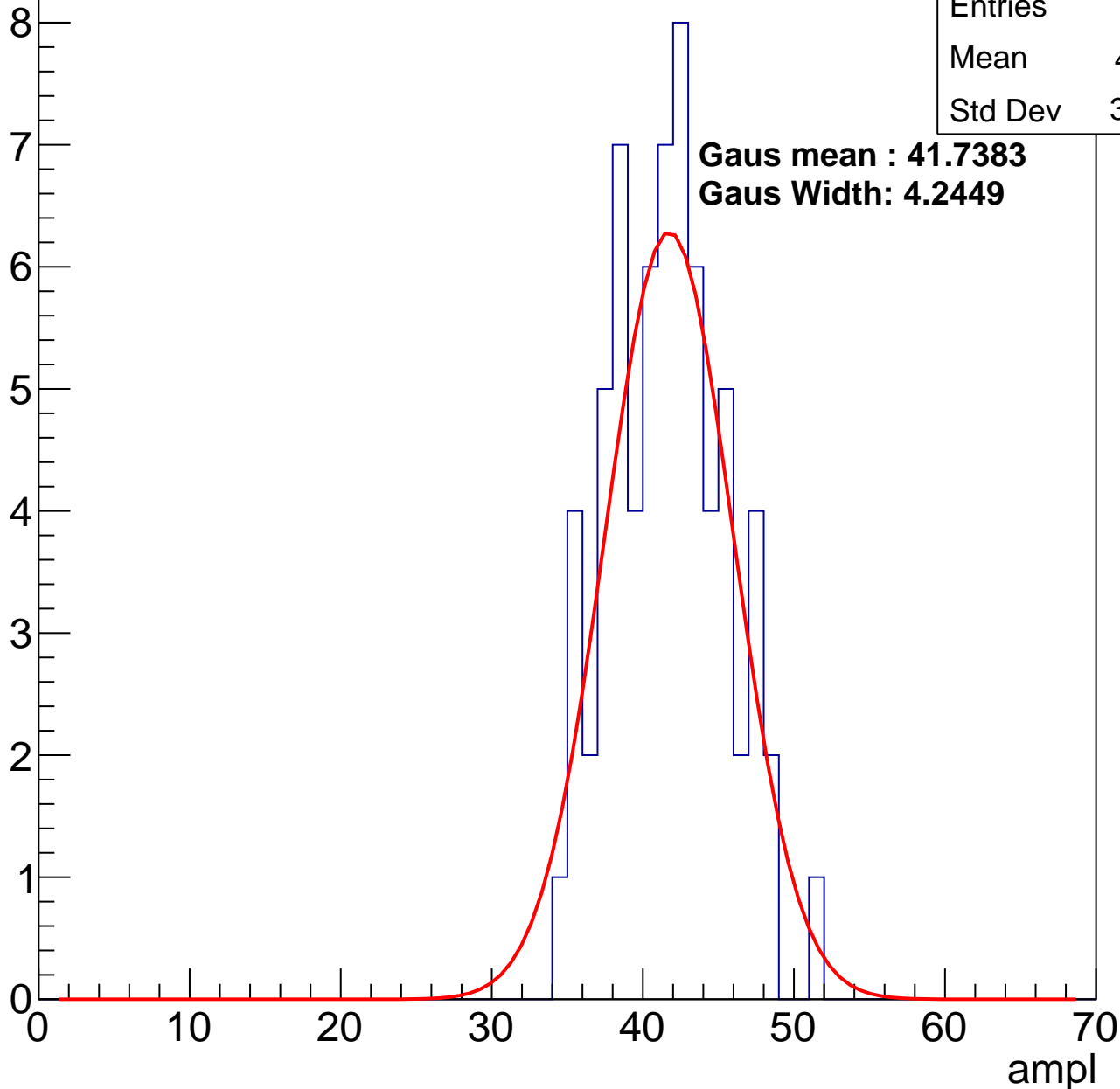
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	41.21
Std Dev	3.728

**Gaus mean : 41.7383**

**Gaus Width: 4.2449**

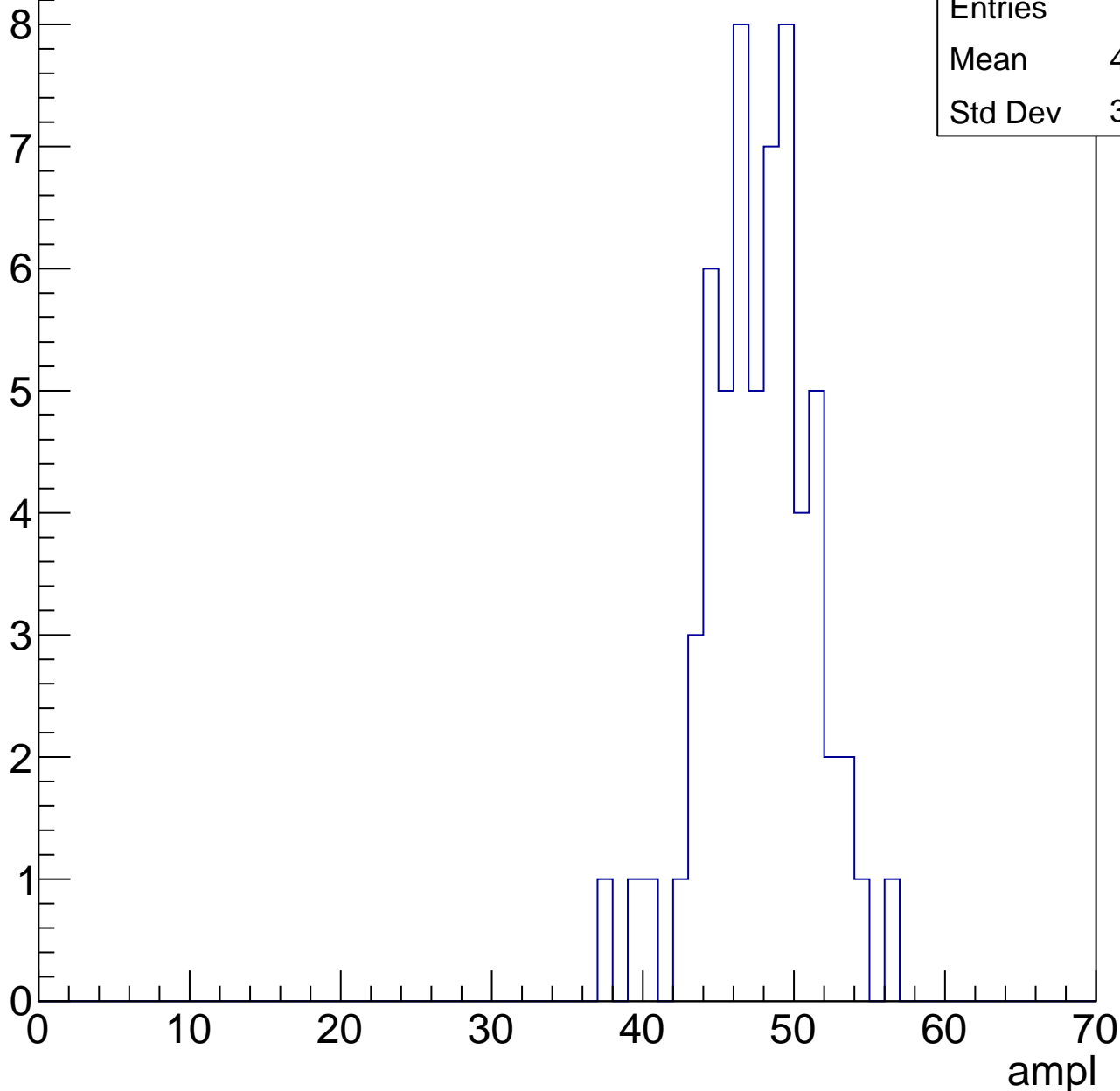


# B1L101S, U22-ch52, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	47.25
Std Dev	3.556

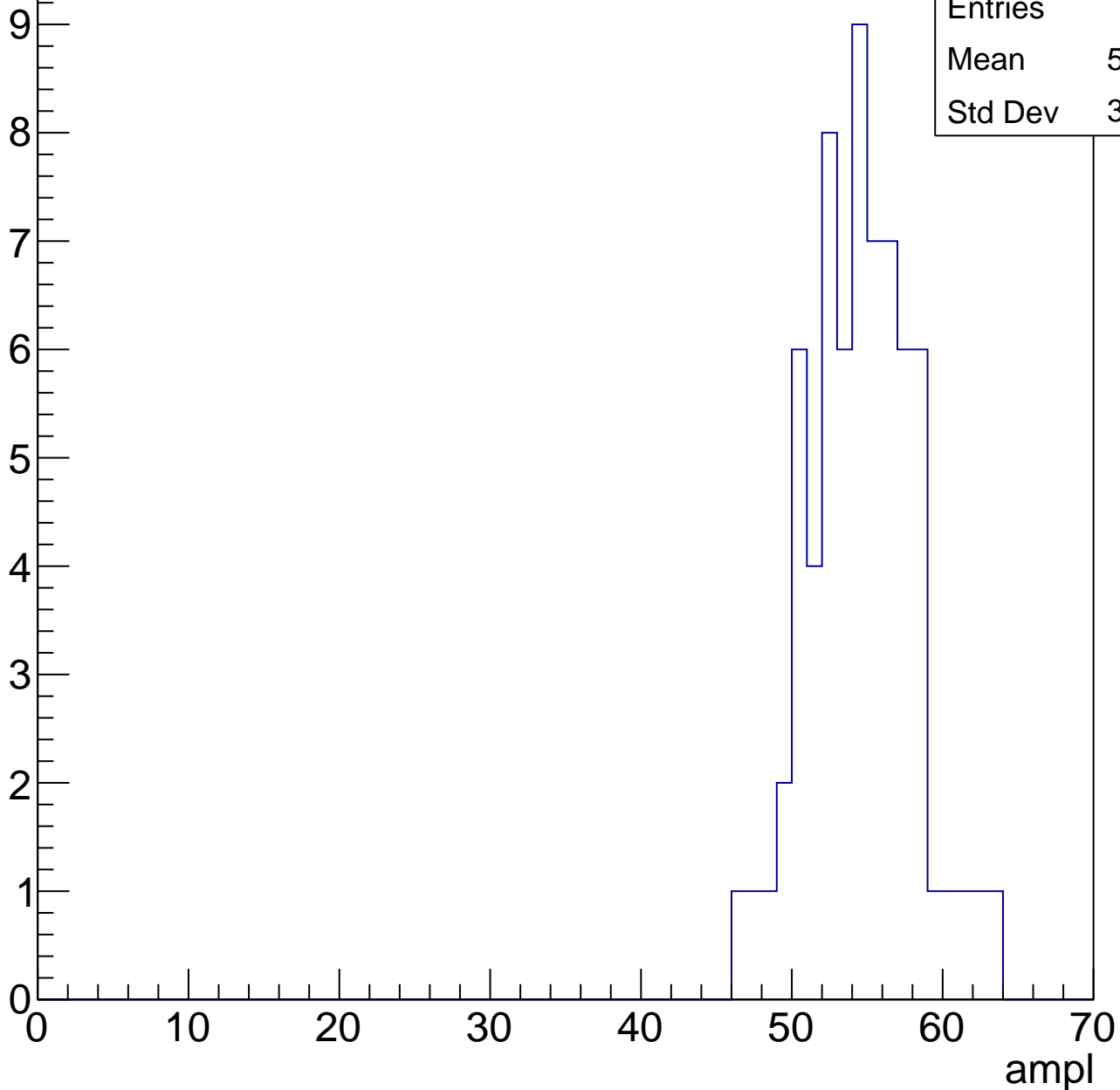


# B1L101S, U22-ch52, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	54.13
Std Dev	3.422



# B1L101S, U22-ch52, adc5

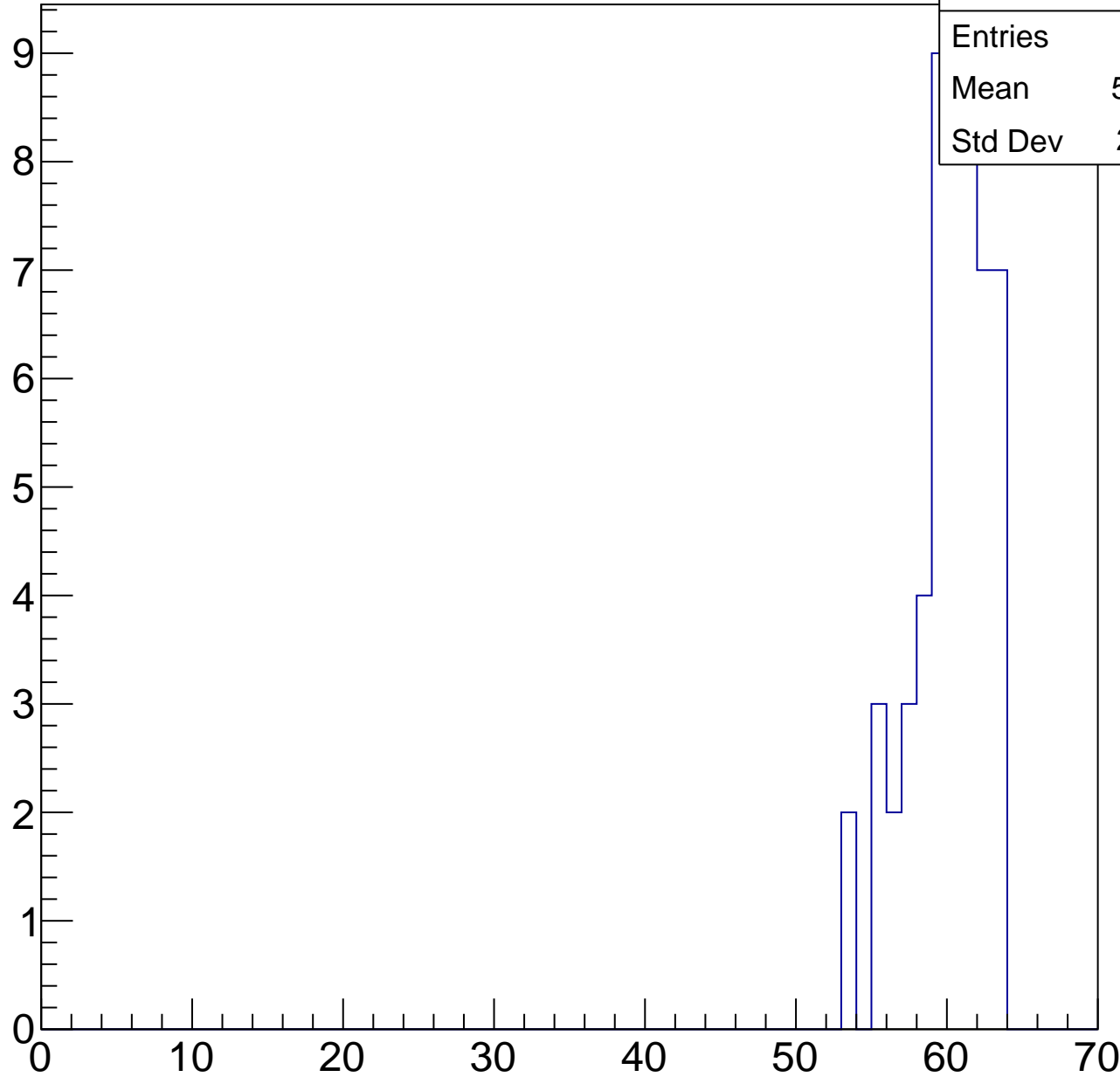
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	54
Mean	59.63
Std Dev	2.541

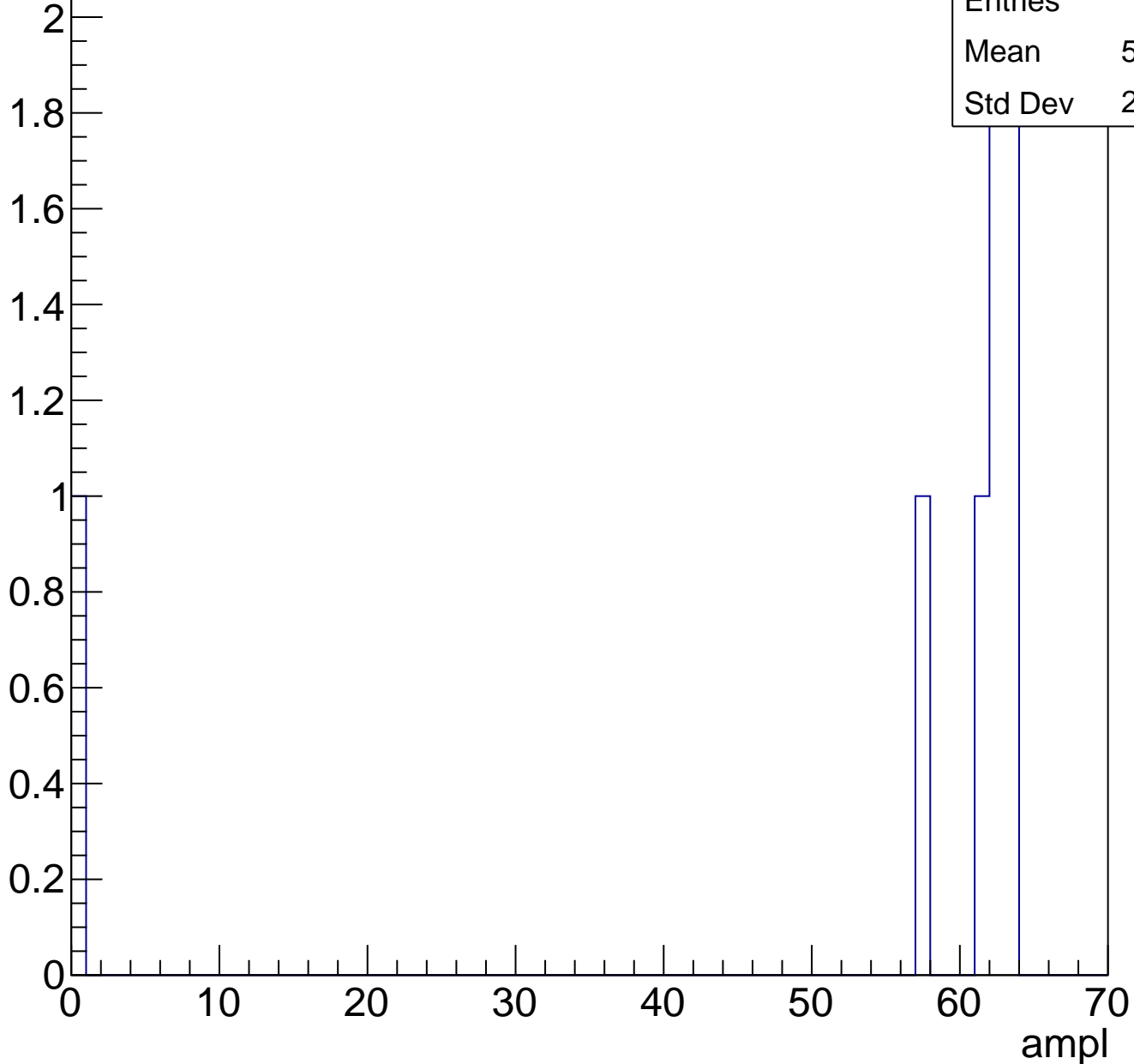
ampl



# B1L101S, U22-ch52, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U22-ch52, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U22-ch53, adc0

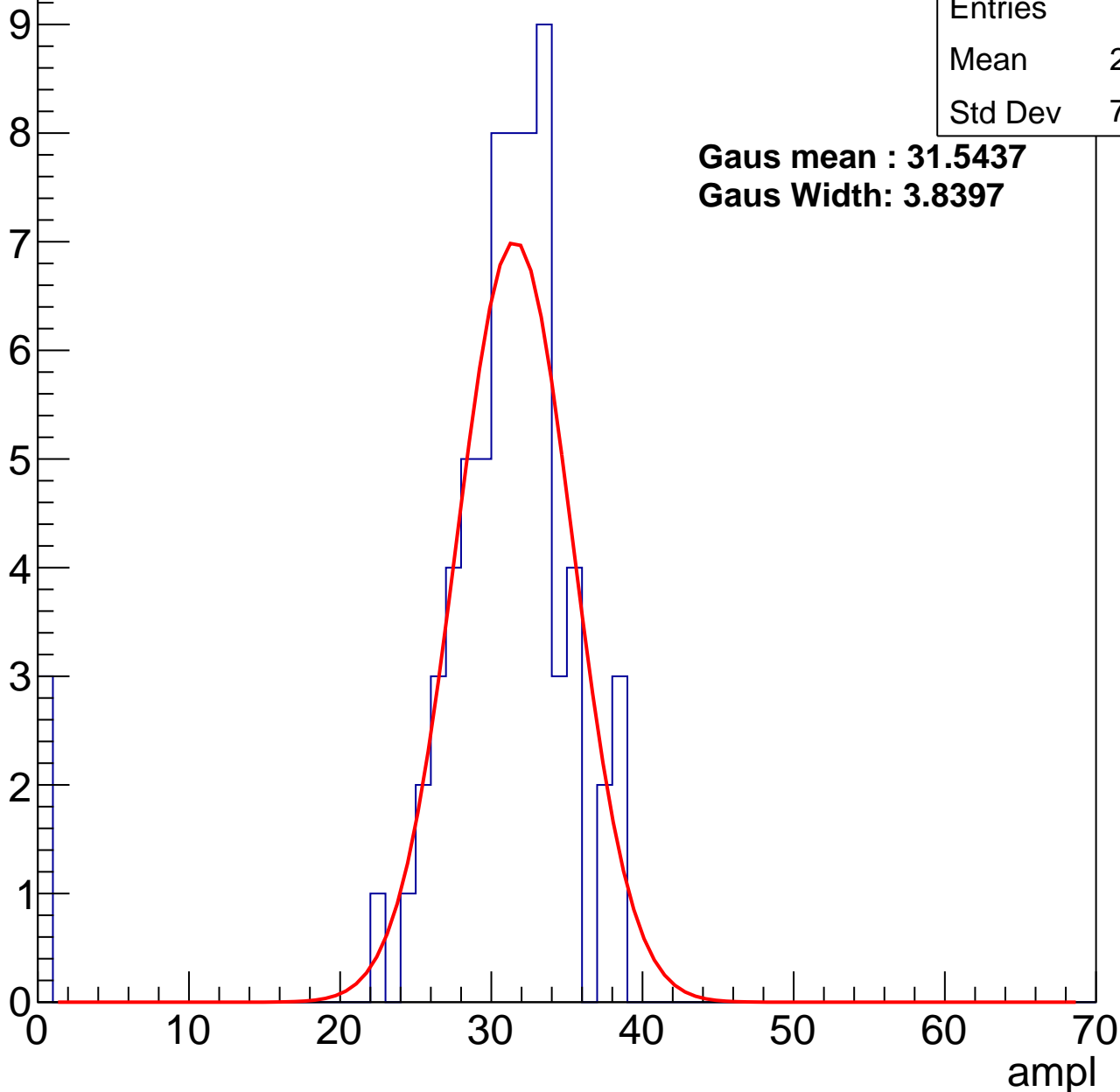
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	29.54
Std Dev	7.125

**Gaus mean : 31.5437**

**Gaus Width: 3.8397**



# B1L101S, U22-ch53, adc1

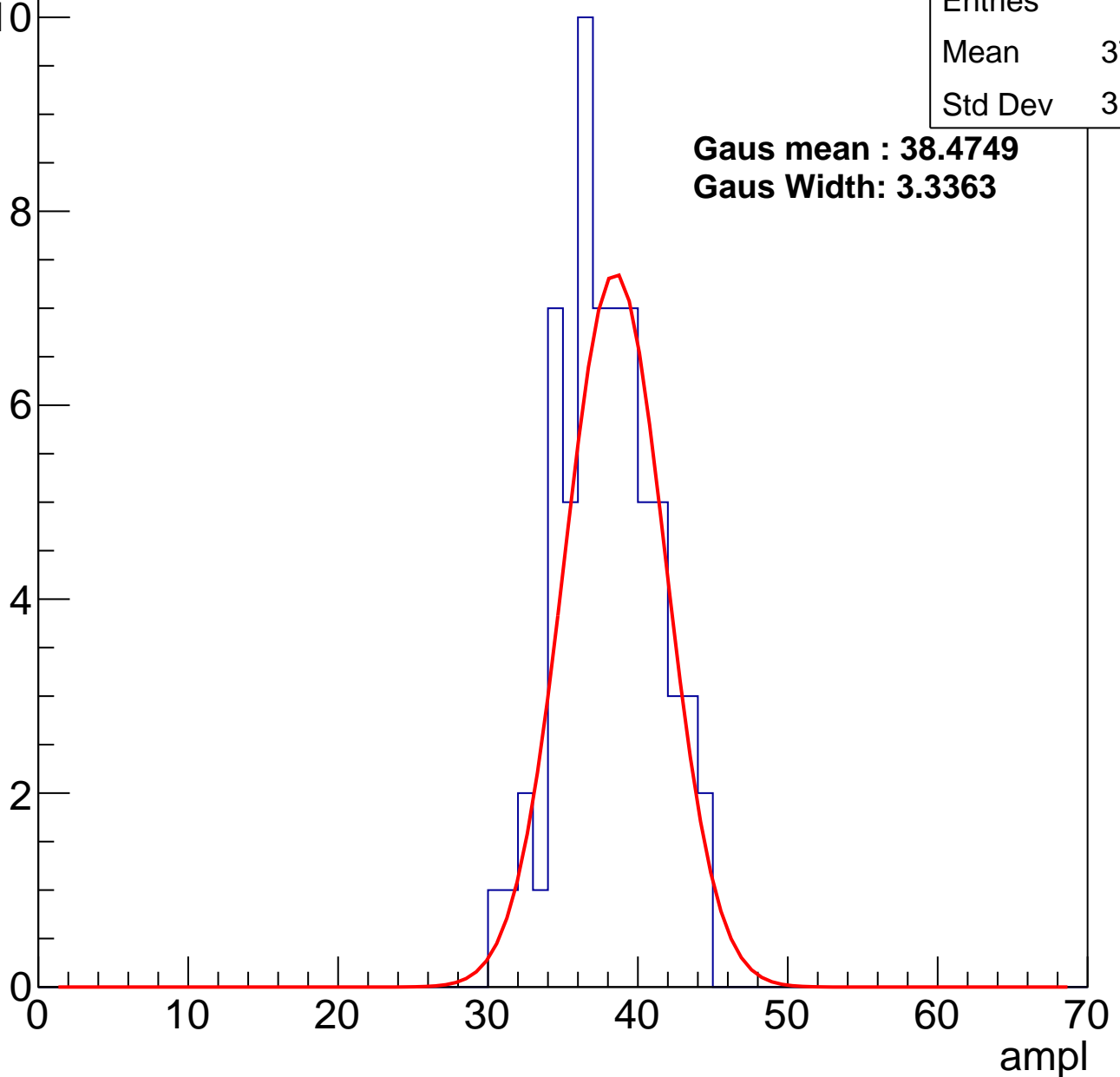
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	66
Mean	37.53
Std Dev	3.178

**Gaus mean : 38.4749**

**Gaus Width: 3.3363**



# B1L101S, U22-ch53, adc2

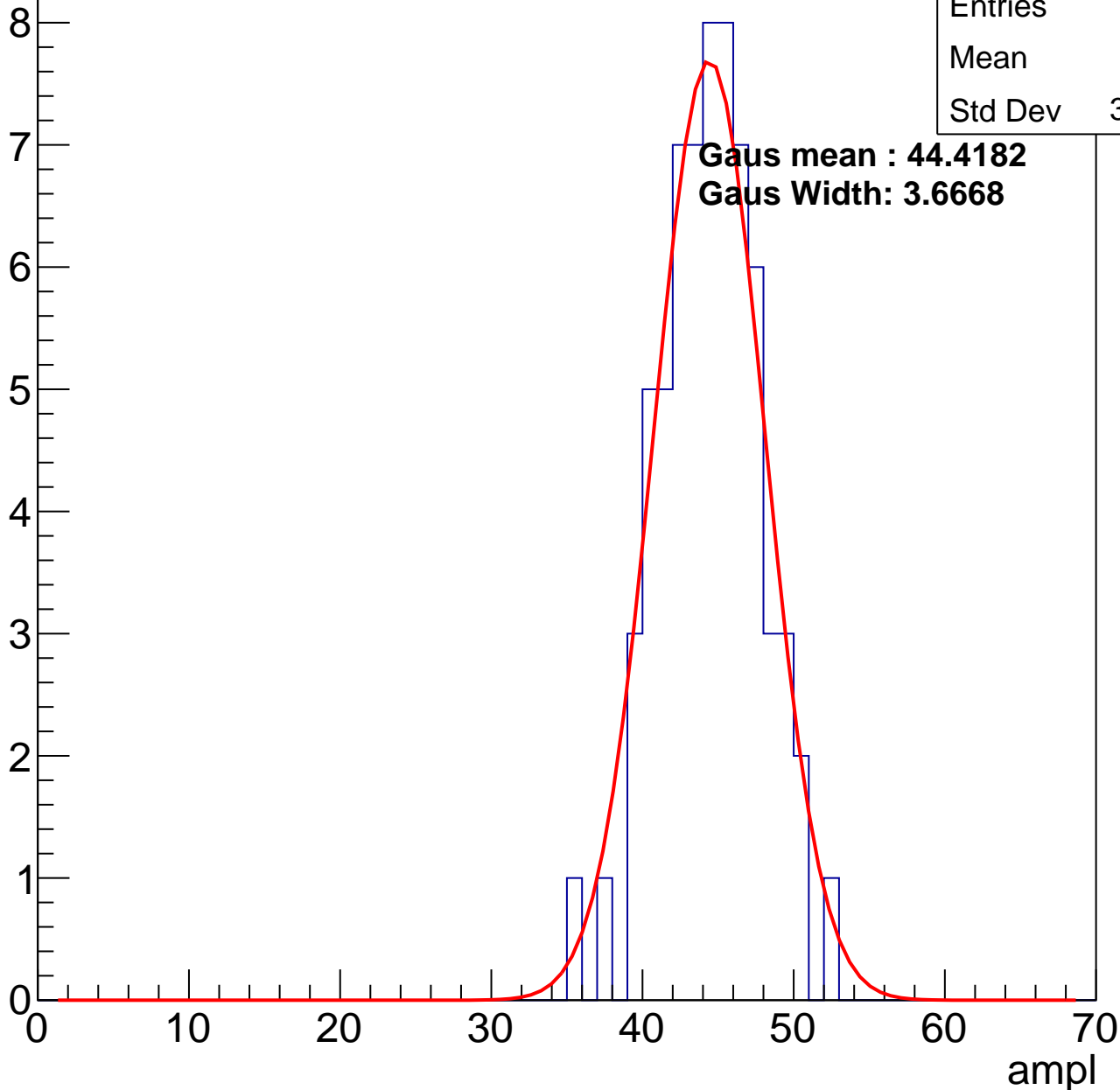
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	67
Mean	44
Std Dev	3.264

**Gaus mean : 44.4182**

**Gaus Width: 3.6668**

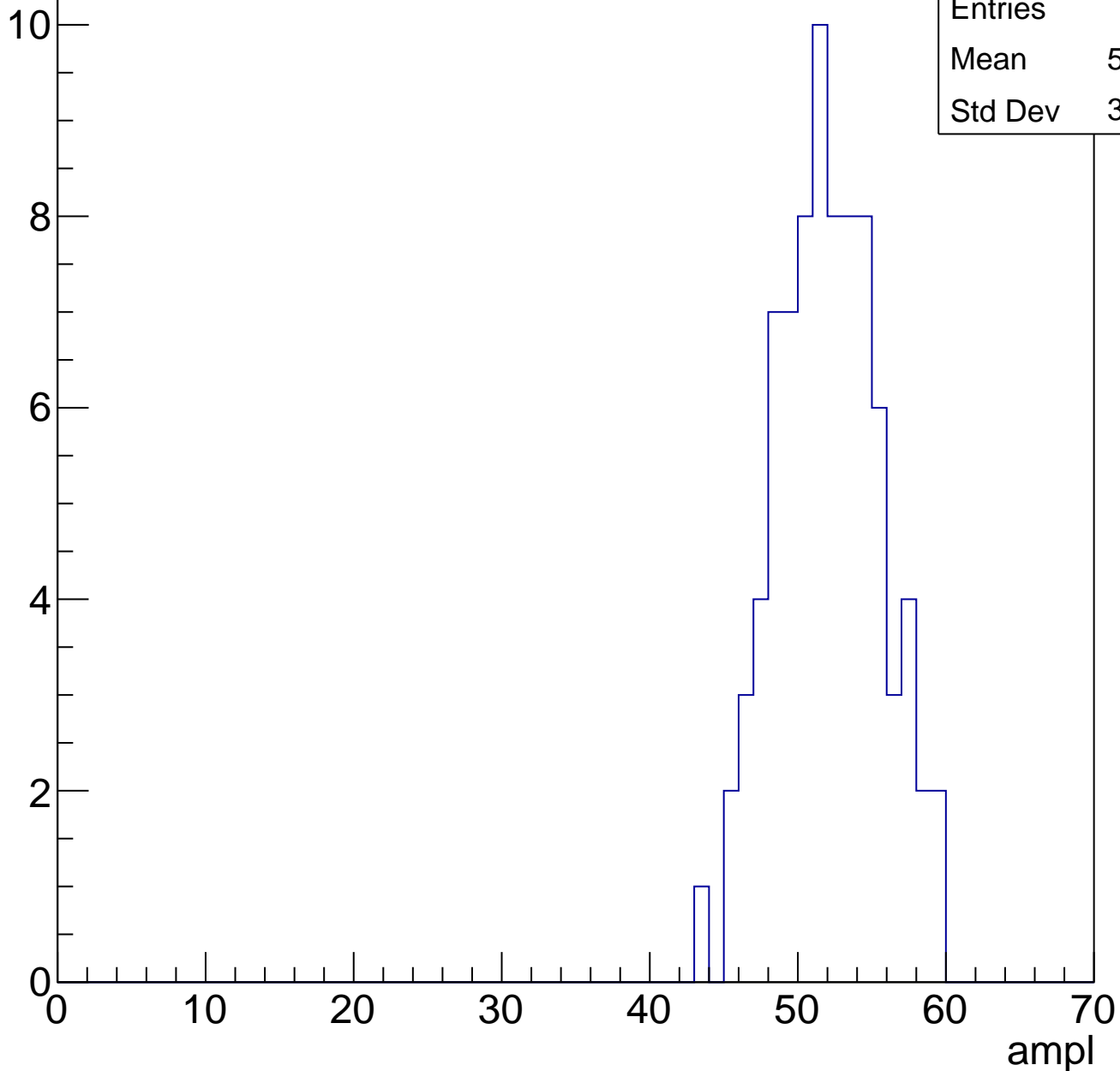


# B1L101S, U22-ch53, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

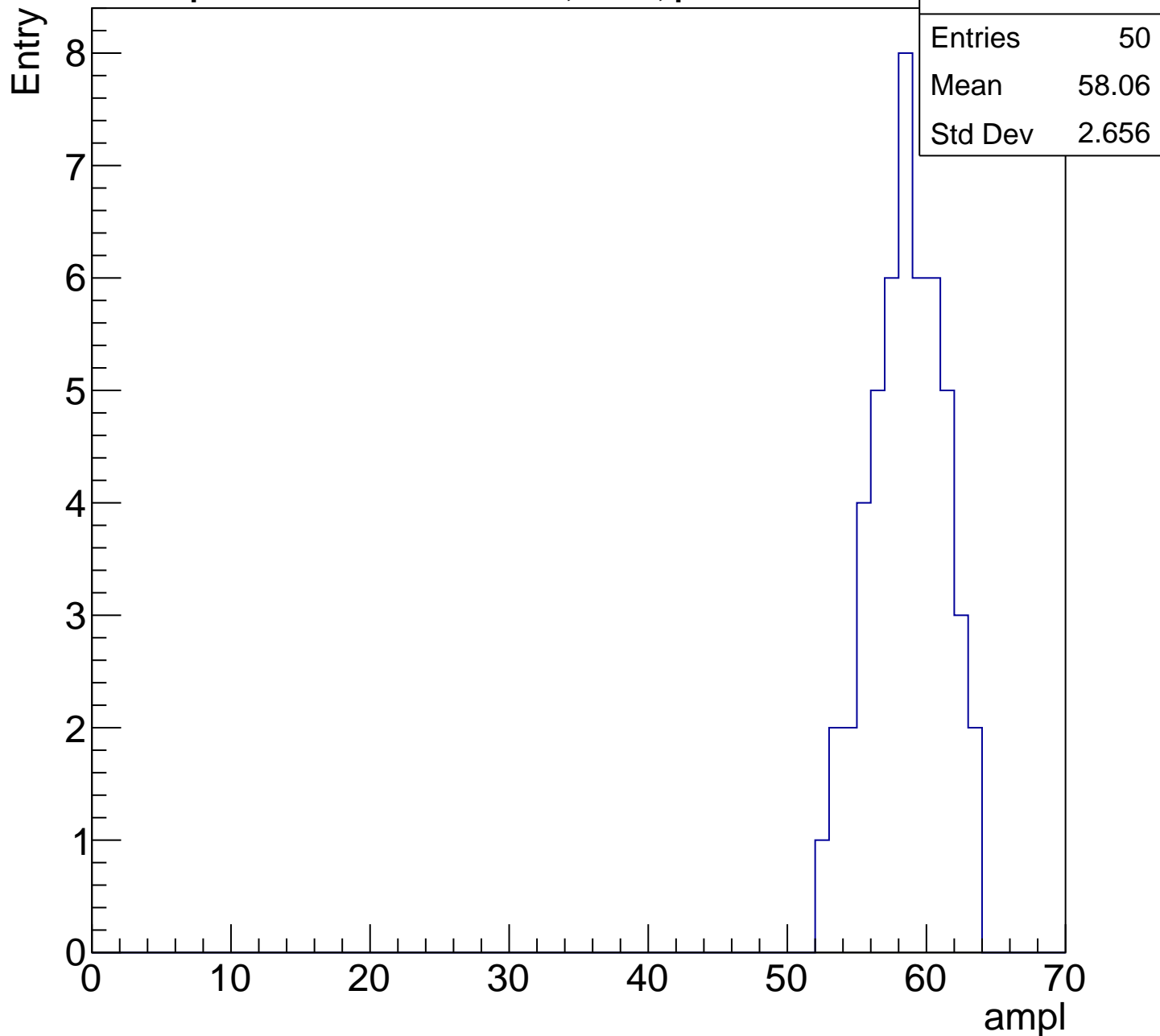
Entry

Entries	83
Mean	51.57
Std Dev	3.472



# B1L101S, U22-ch53, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

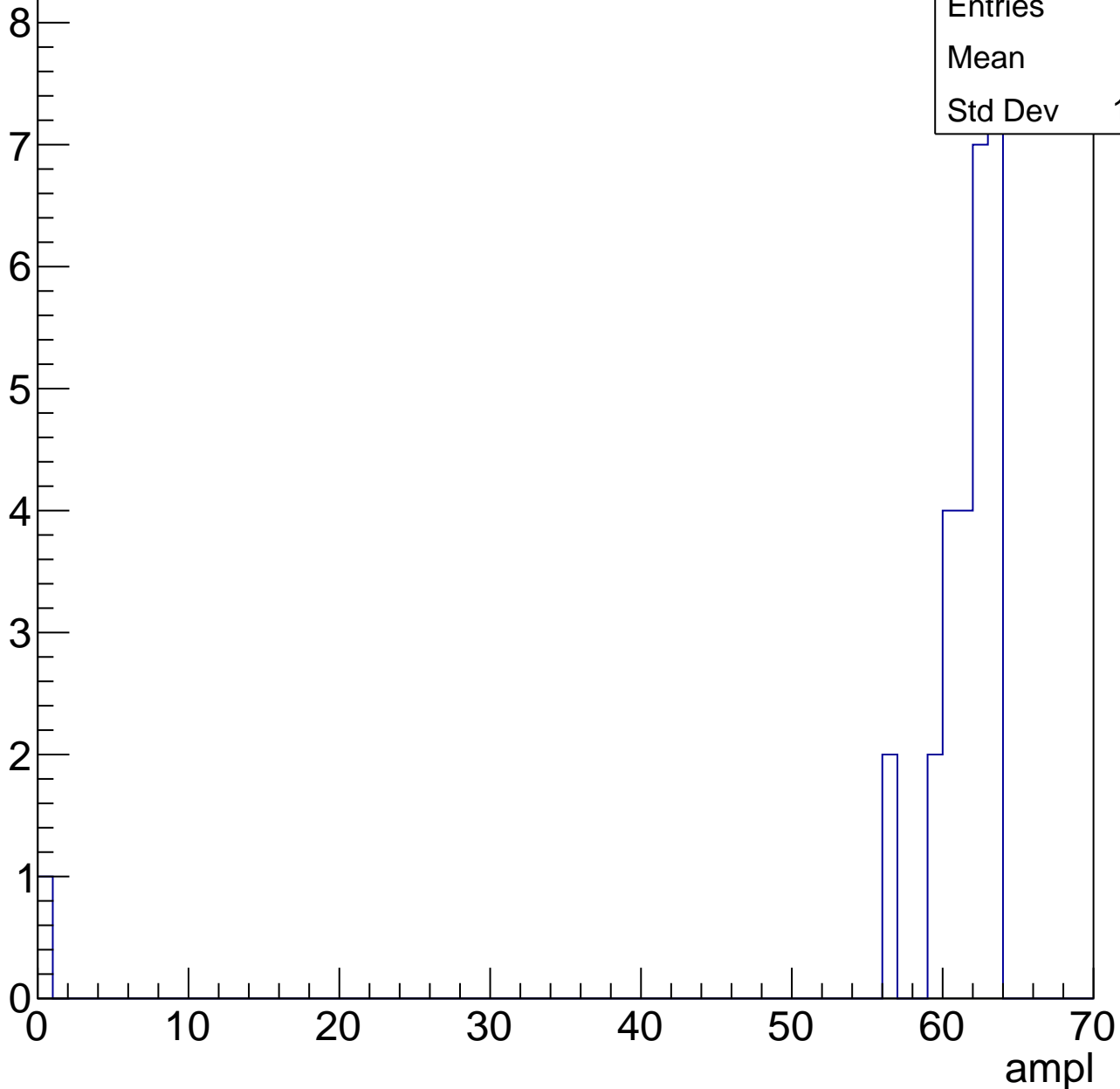


# B1L101S, U22-ch53, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	28
Mean	59
Std Dev	11.51



# B1L101S, U22-ch53, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U22-ch53, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L101S, U22-ch54, adc0

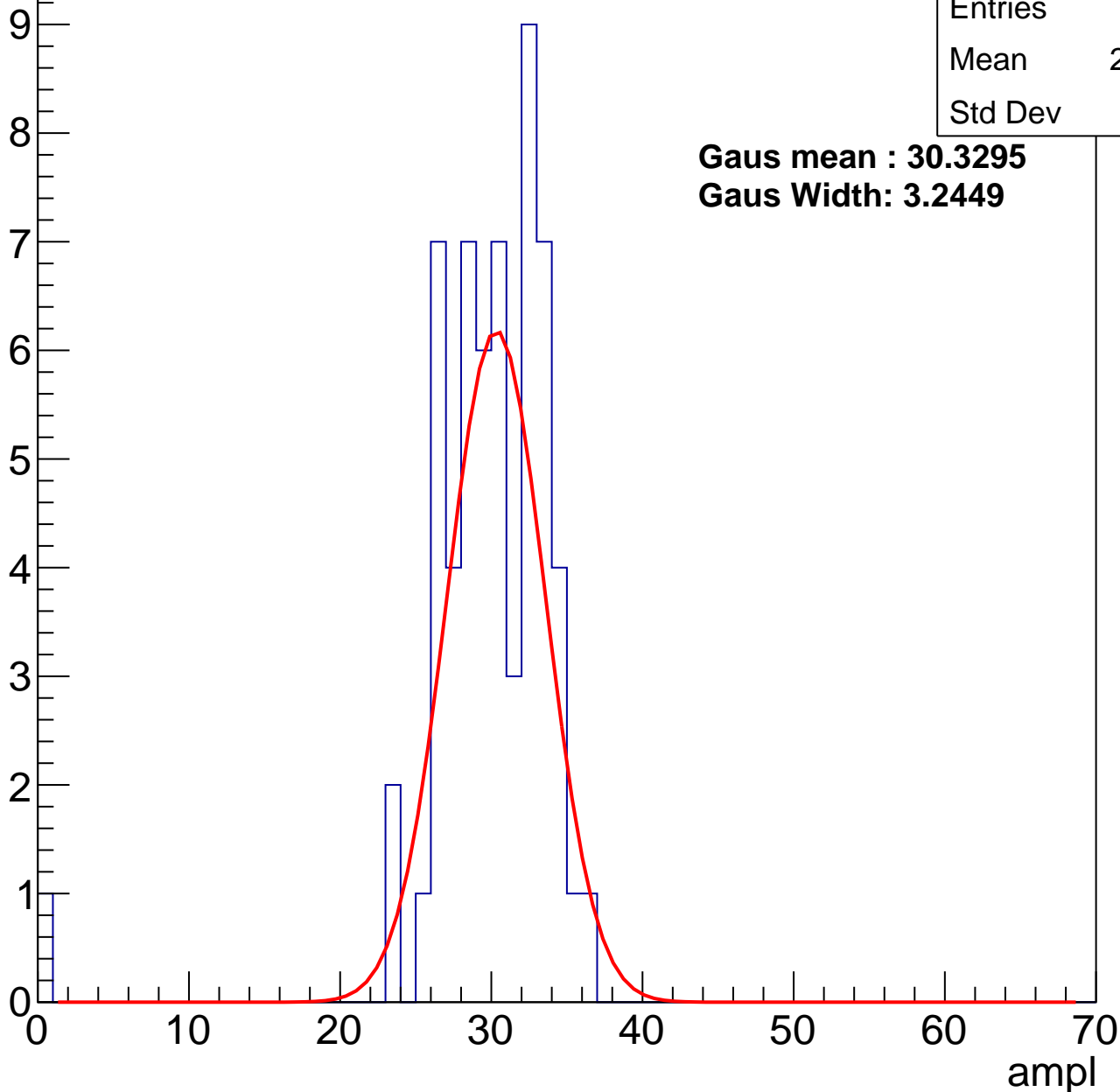
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	60
Mean	29.33
Std Dev	4.84

**Gaus mean : 30.3295**

**Gaus Width: 3.2449**



# B1L101S, U22-ch54, adc1

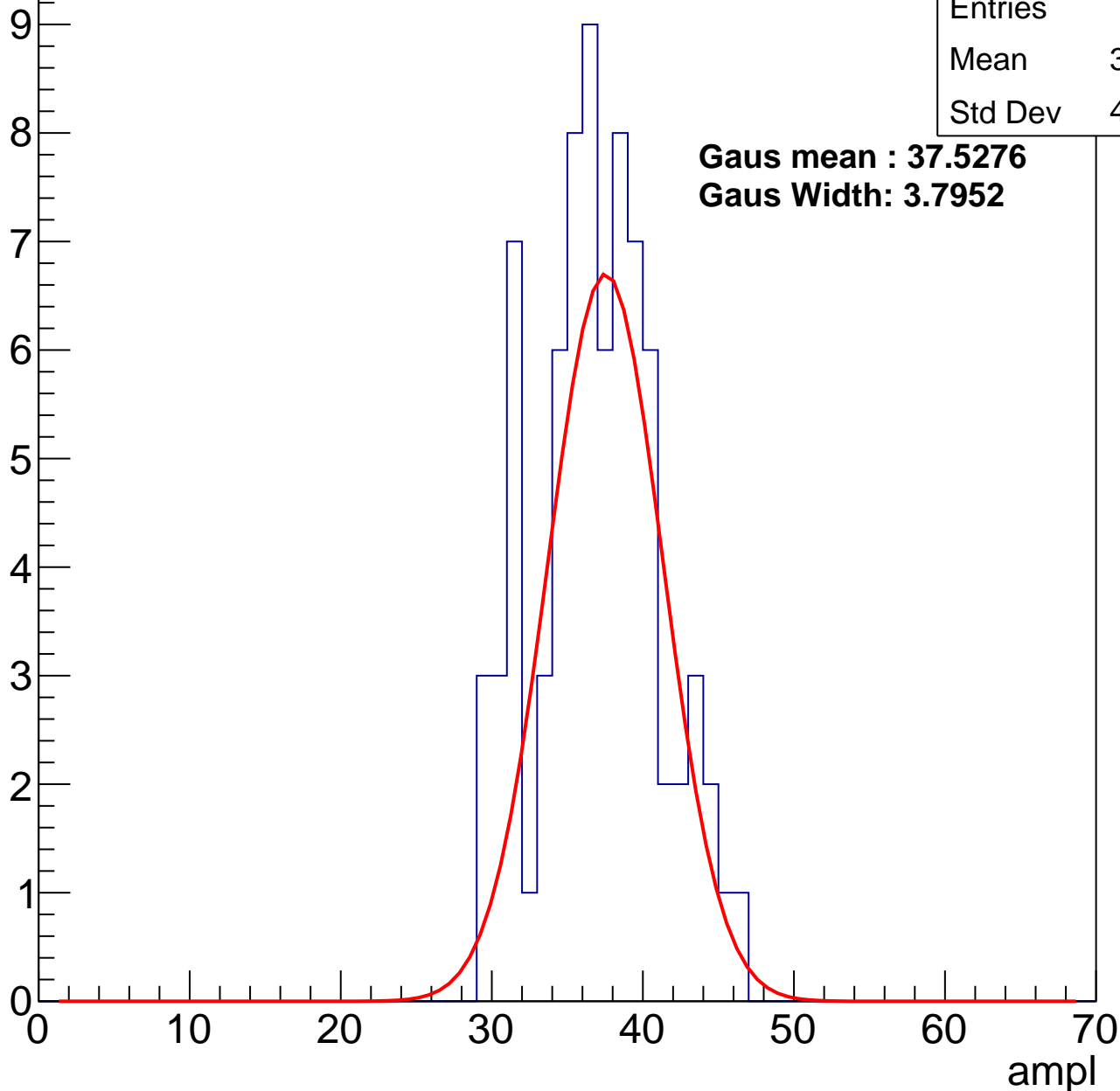
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	78
Mean	36.49
Std Dev	4.022

**Gaus mean : 37.5276**

**Gaus Width: 3.7952**



# B1L101S, U22-ch54, adc2

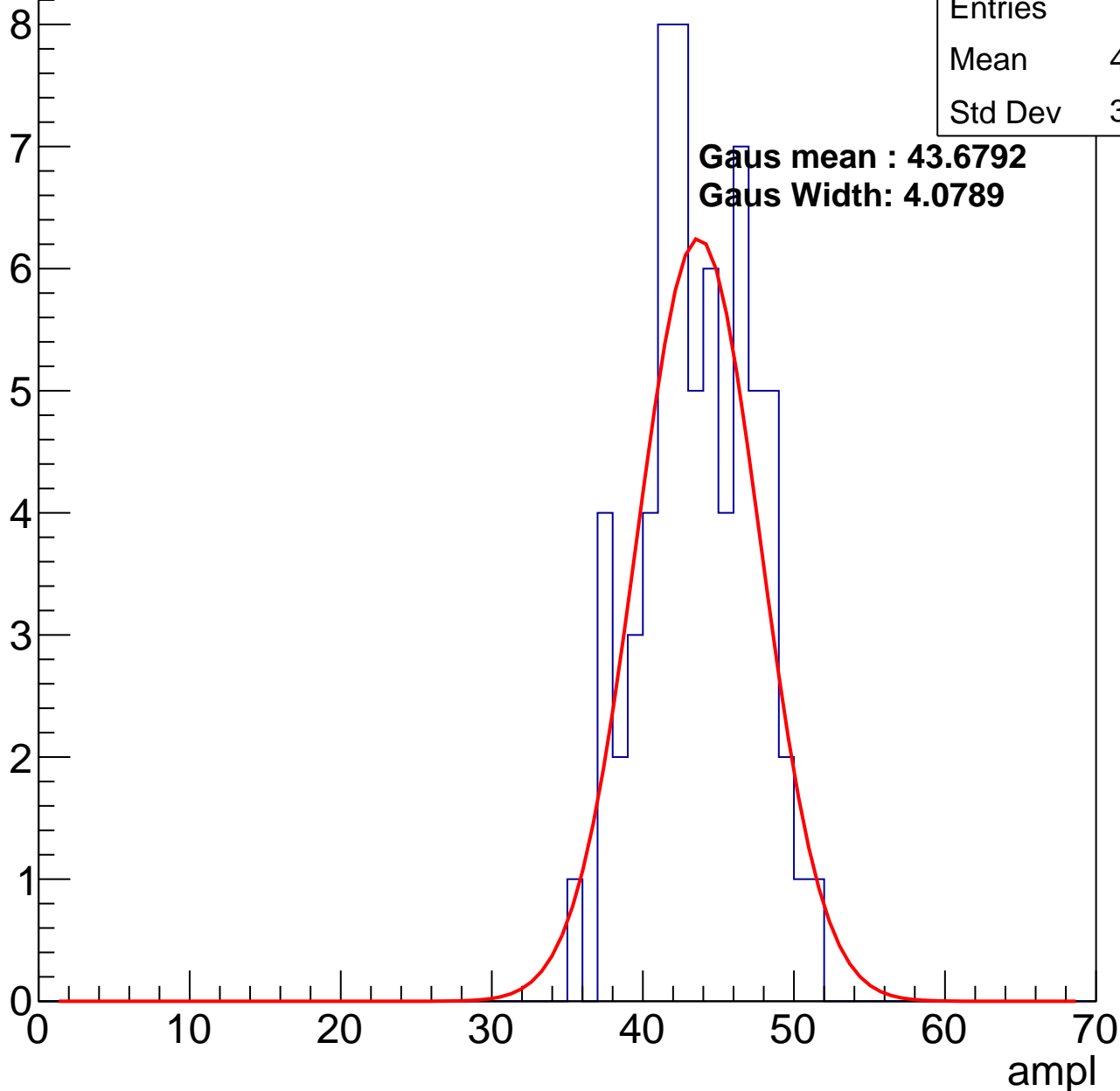
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	66
Mean	43.26
Std Dev	3.594

**Gaus mean : 43.6792**

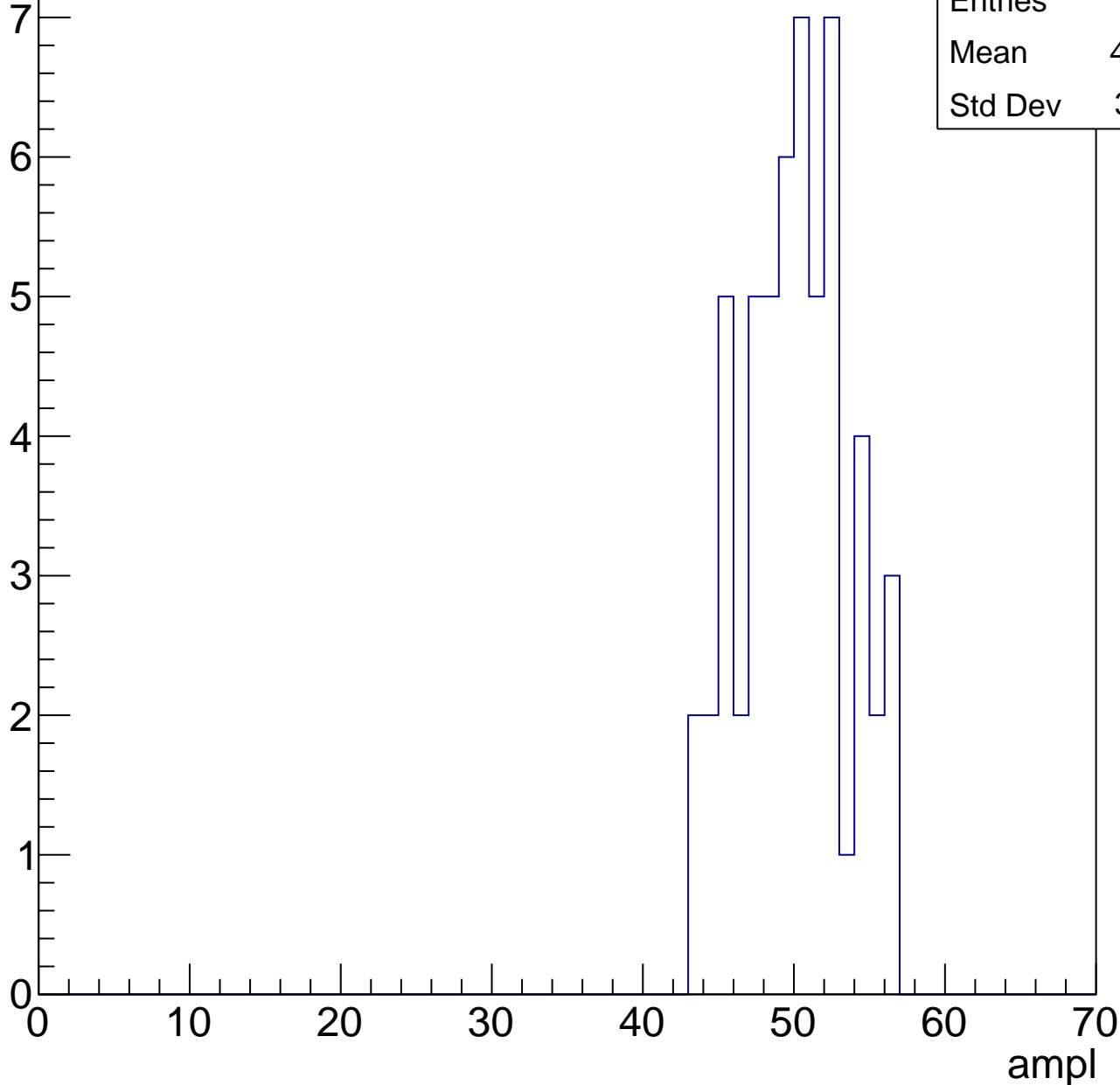
**Gaus Width: 4.0789**



# B1L101S, U22-ch54, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

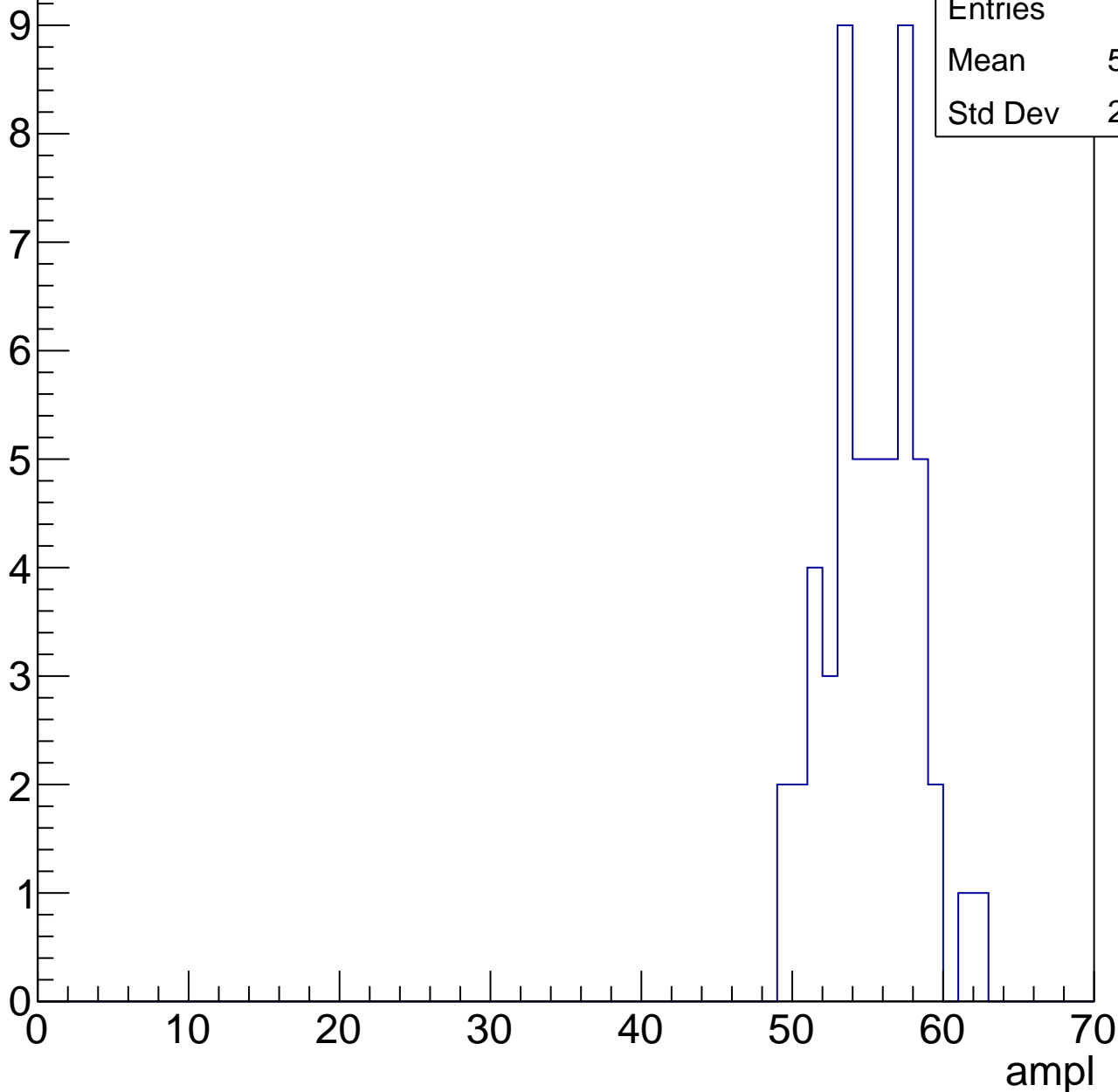


# B1L101S, U22-ch54, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	53
Mean	54.79
Std Dev	2.929



# B1L101S, U22-ch54, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

10

Entries 47

Mean 58.4

Std Dev 8.908

8

6

4

2

0

0

10

20

30

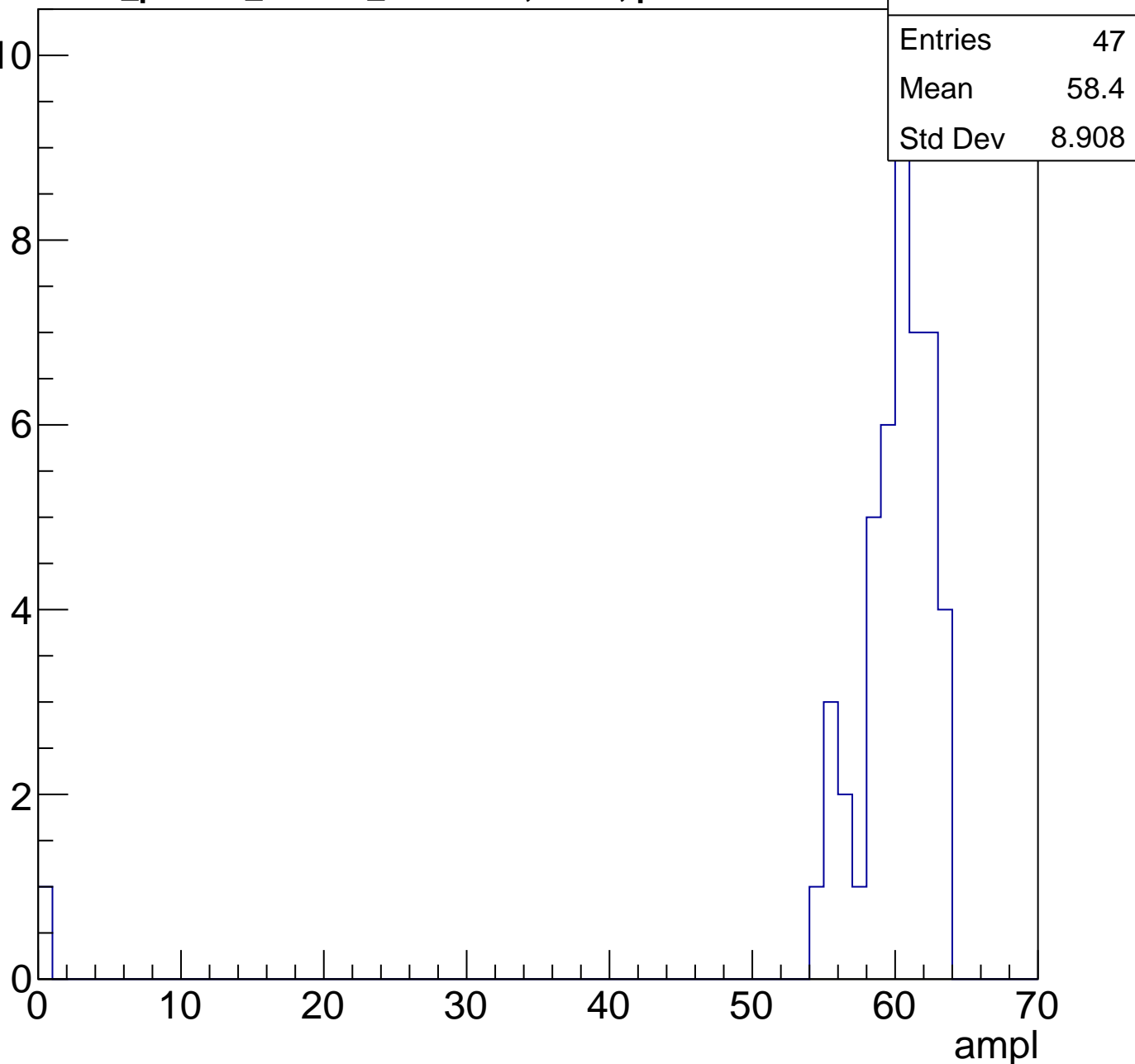
40

50

60

70

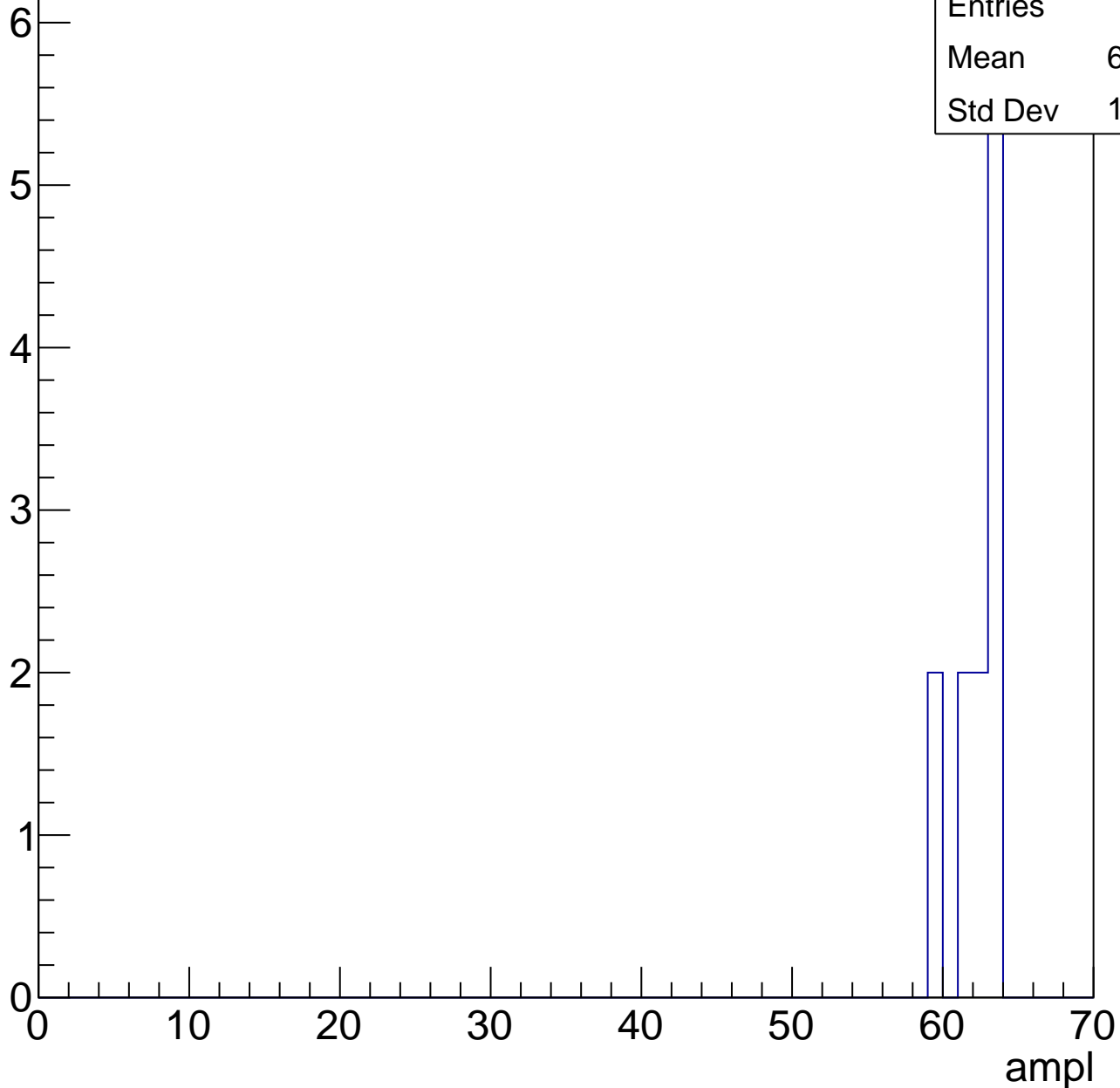
ampl



# B1L101S, U22-ch54, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	12
Mean	61.83
Std Dev	1.462



# B1L101S, U22-ch54, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L101S, U22-ch55, adc0

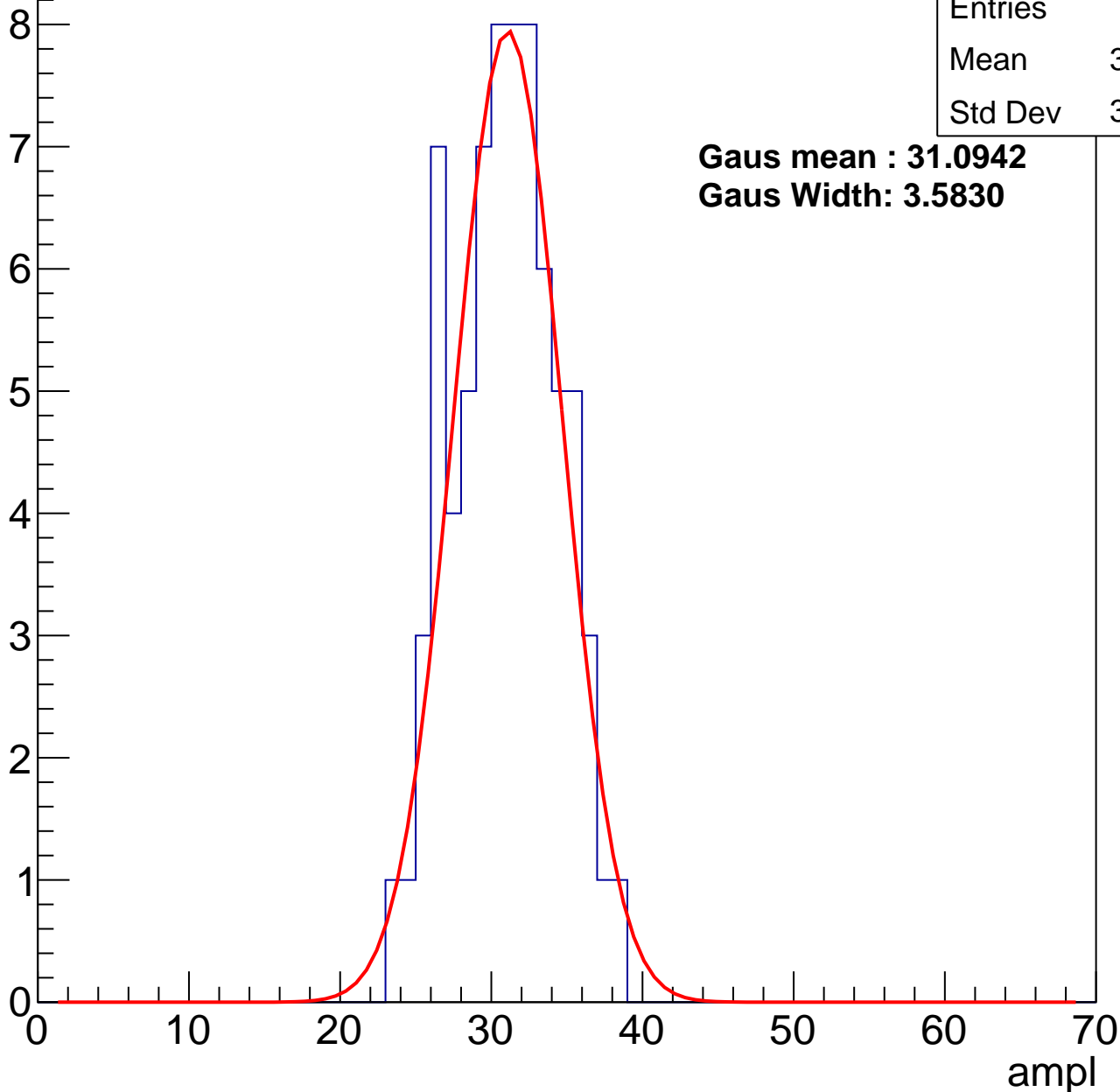
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	73
Mean	30.48
Std Dev	3.389

**Gaus mean : 31.0942**

**Gaus Width: 3.5830**



# B1L101S, U22-ch55, adc1

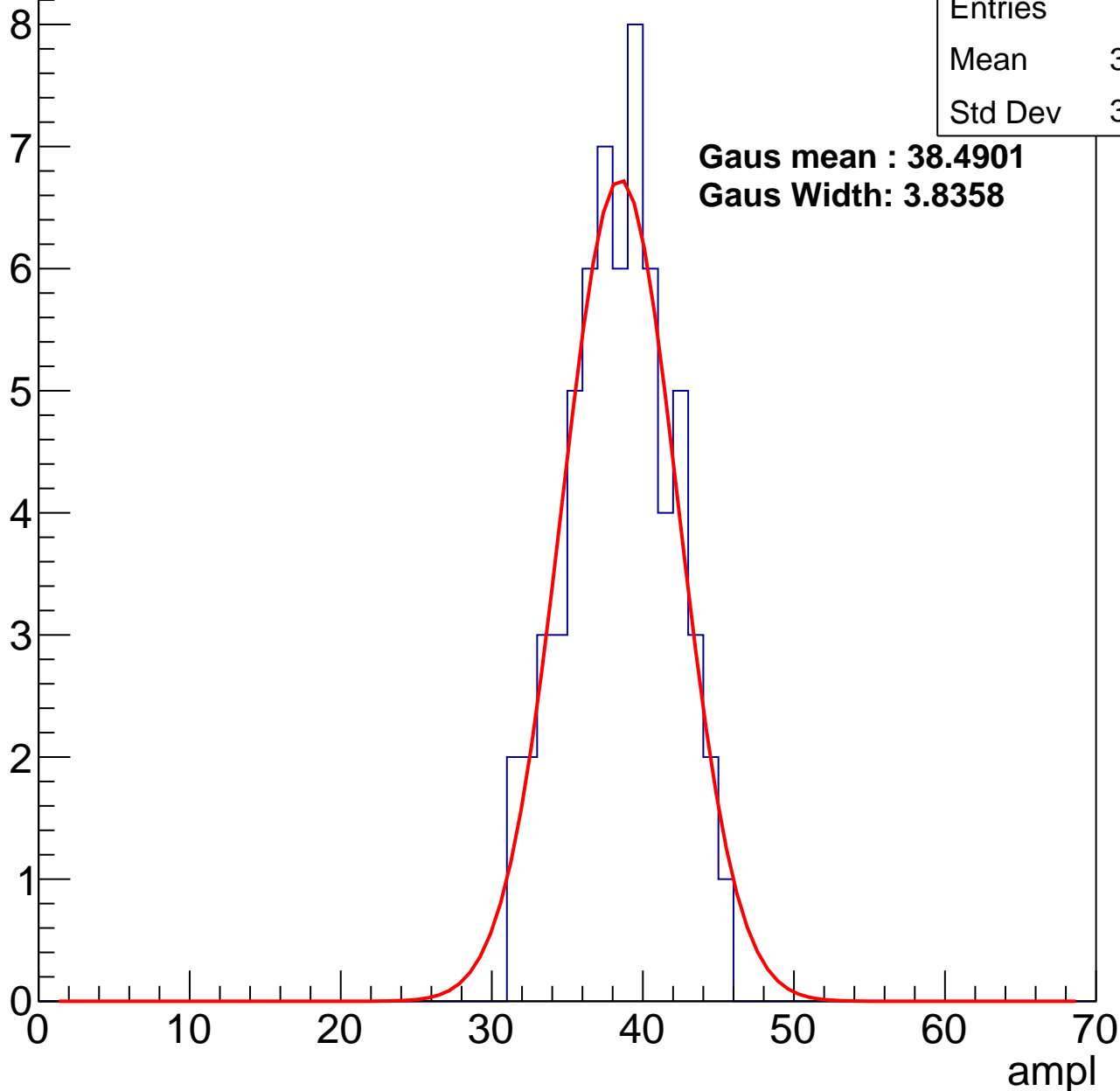
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	37.98
Std Dev	3.364

**Gaus mean : 38.4901**

**Gaus Width: 3.8358**



# B1L101S, U22-ch55, adc2

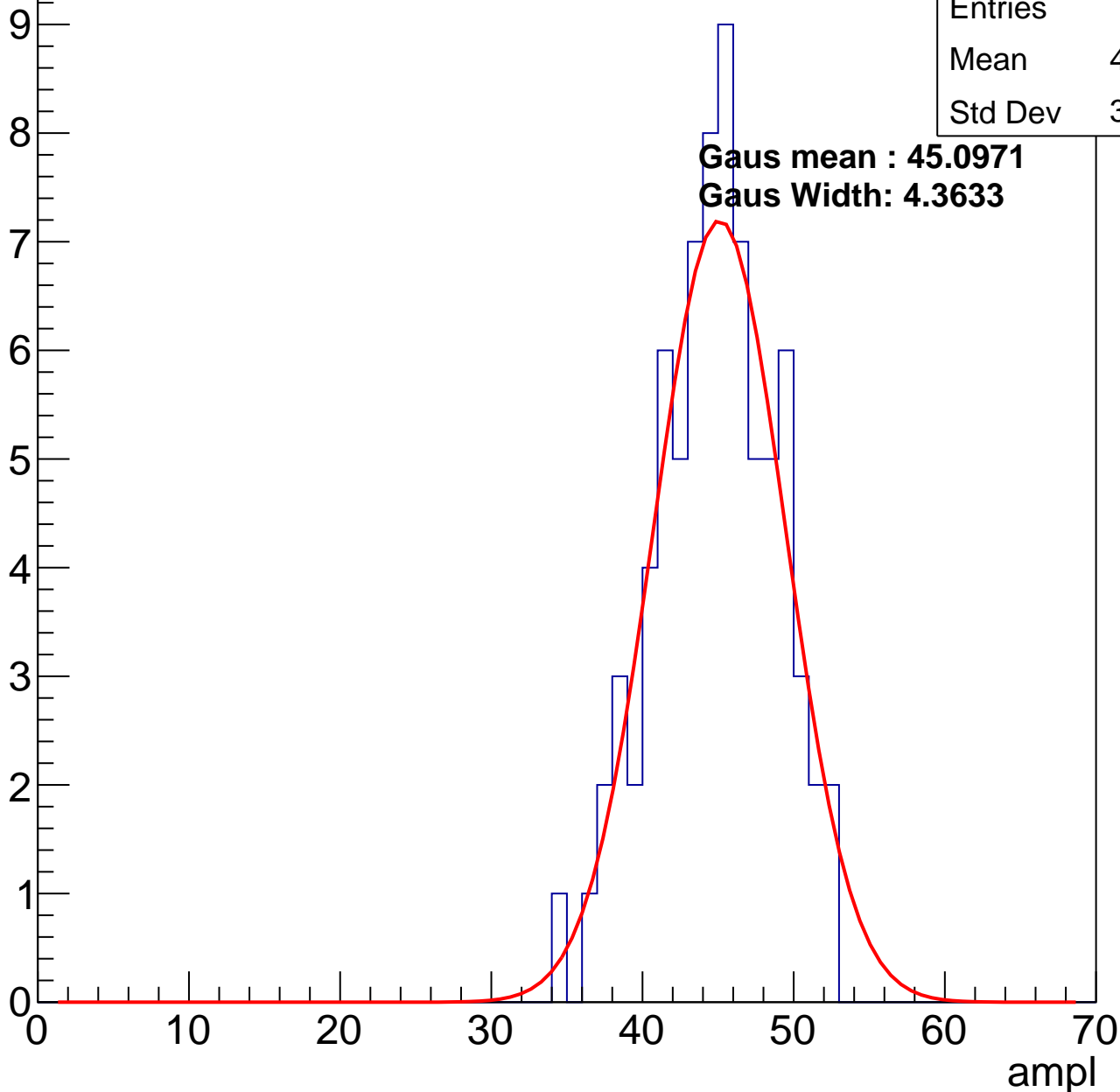
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	78
Mean	44.32
Std Dev	3.927

**Gaus mean : 45.0971**

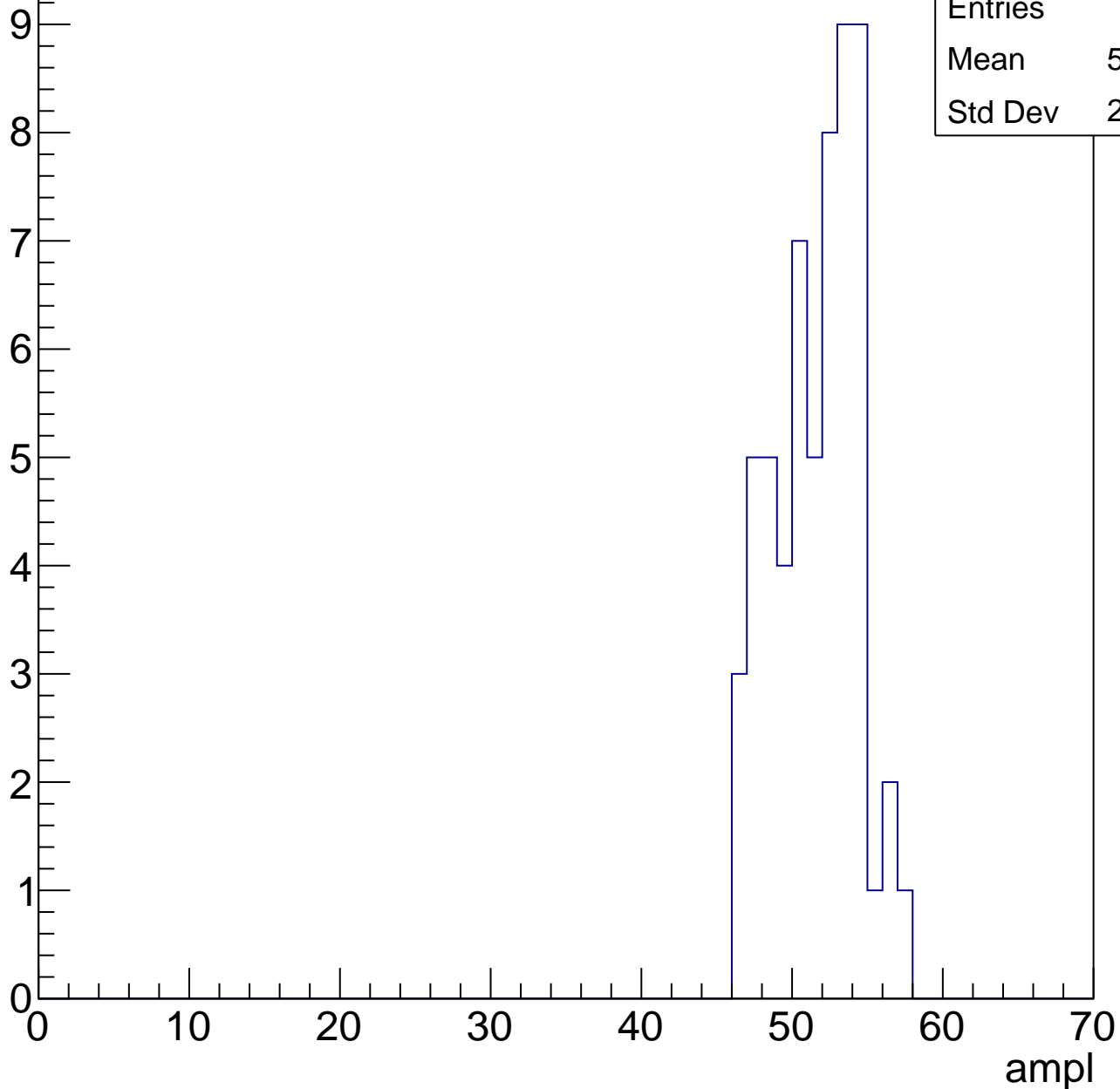
**Gaus Width: 4.3633**



# B1L101S, U22-ch55, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

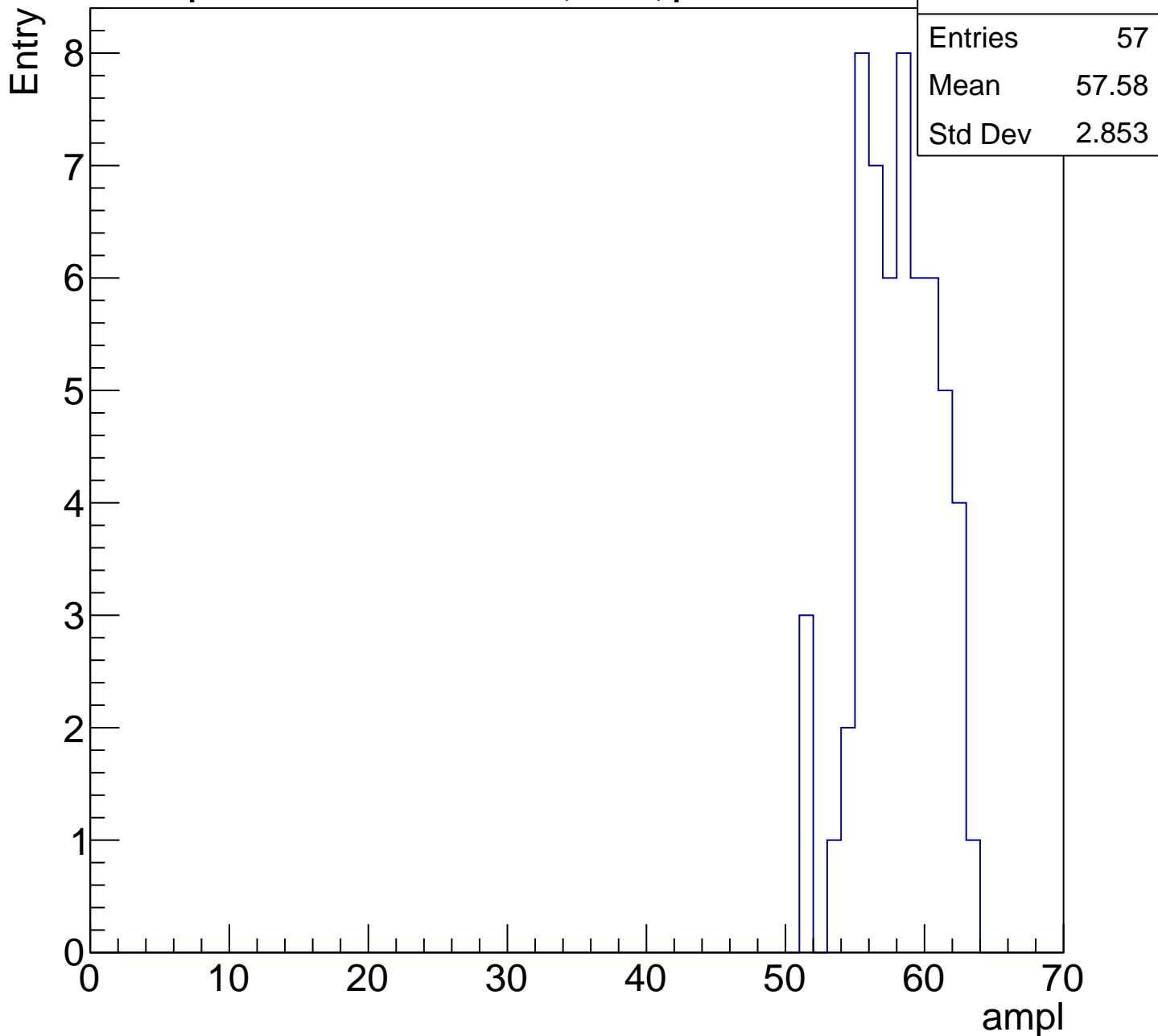
Entry



Entries	59
Mean	51.14
Std Dev	2.758

# B1L101S, U22-ch55, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

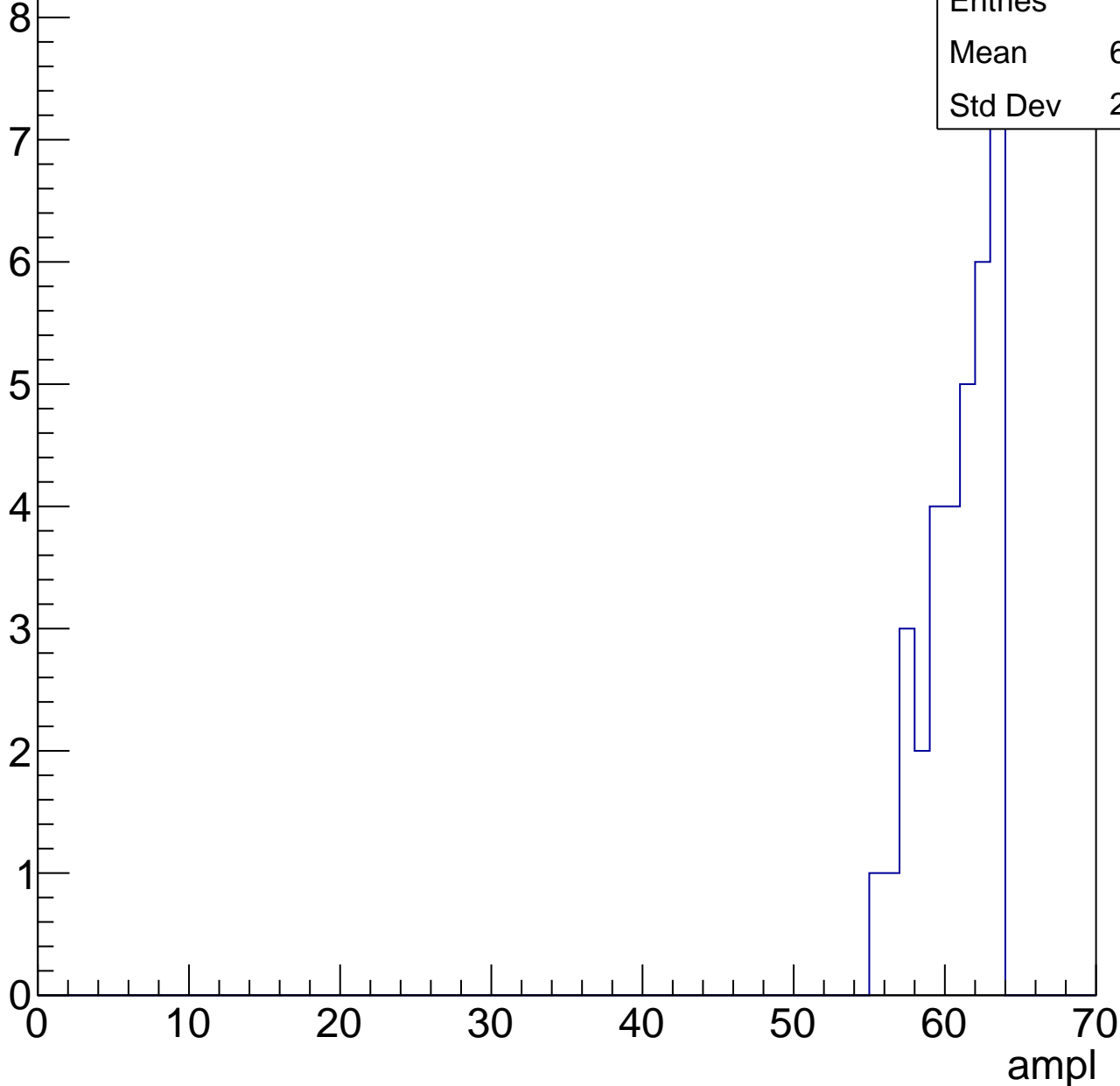


# B1L101S, U22-ch55, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	34
Mean	60.44
Std Dev	2.265



# B1L101S, U22-ch55, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U22-ch55, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U22-ch56, adc0

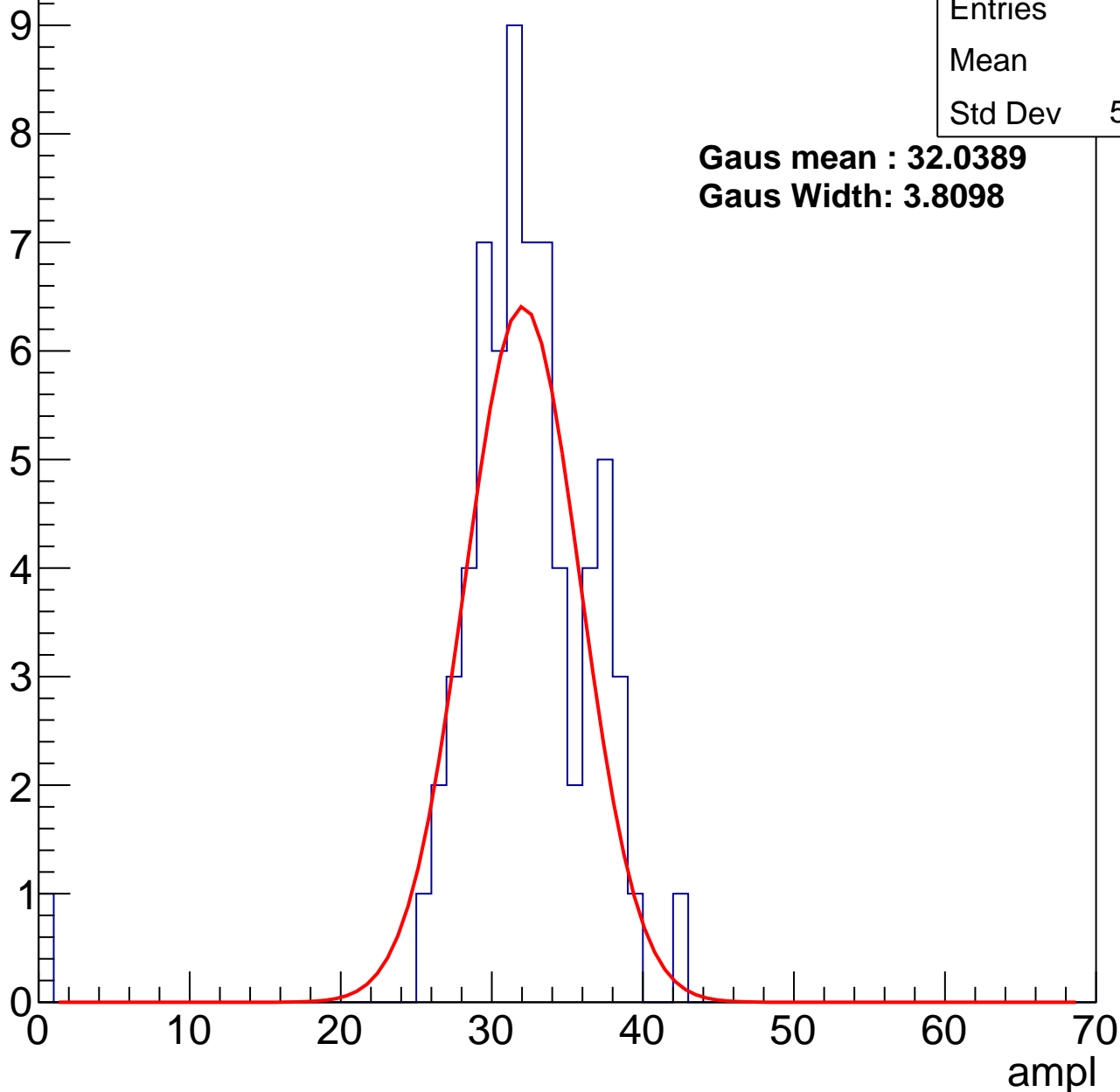
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	67
Mean	31.6
Std Dev	5.263

**Gaus mean : 32.0389**

**Gaus Width: 3.8098**



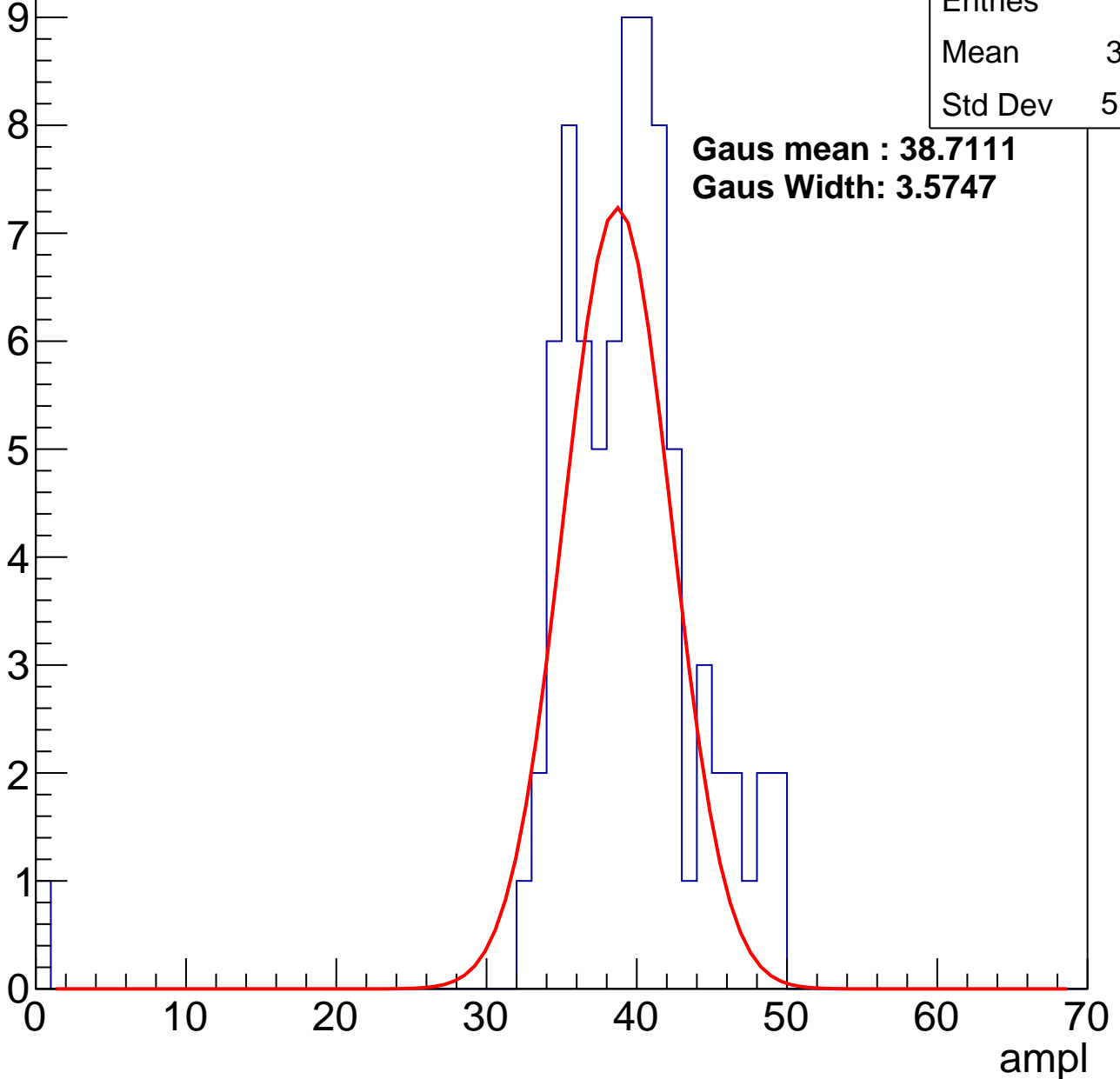
# B1L101S, U22-ch56, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	79
Mean	38.71
Std Dev	5.917

**Gaus mean : 38.7111**  
**Gaus Width: 3.5747**



# B1L101S, U22-ch56, adc2

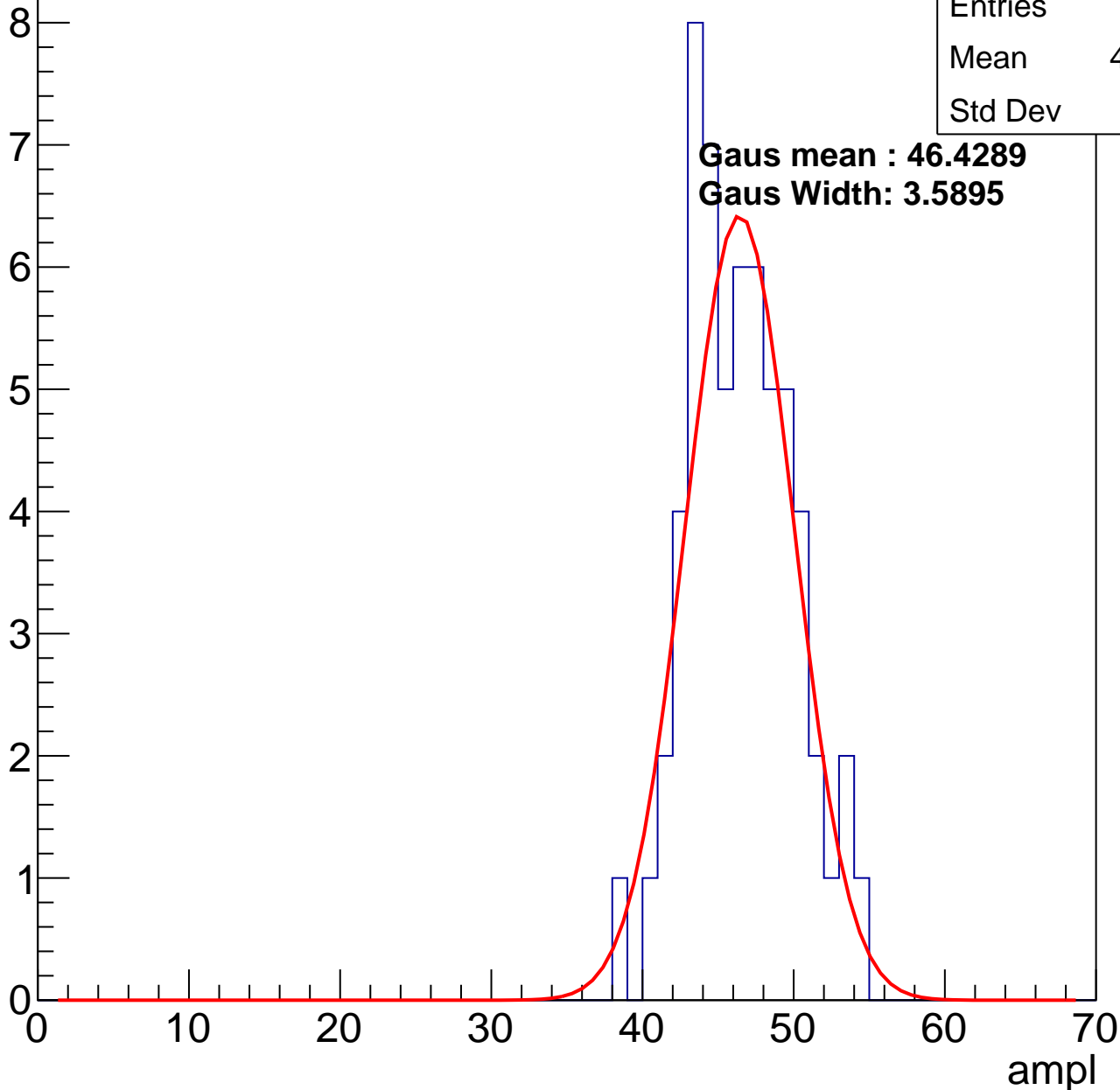
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	60
Mean	46.03
Std Dev	3.42

**Gaus mean : 46.4289**

**Gaus Width: 3.5895**



# B1L101S, U22-ch56, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	90
Mean	52.79
Std Dev	5.478

Entry

10

8

6

4

2

0

0

10

20

30

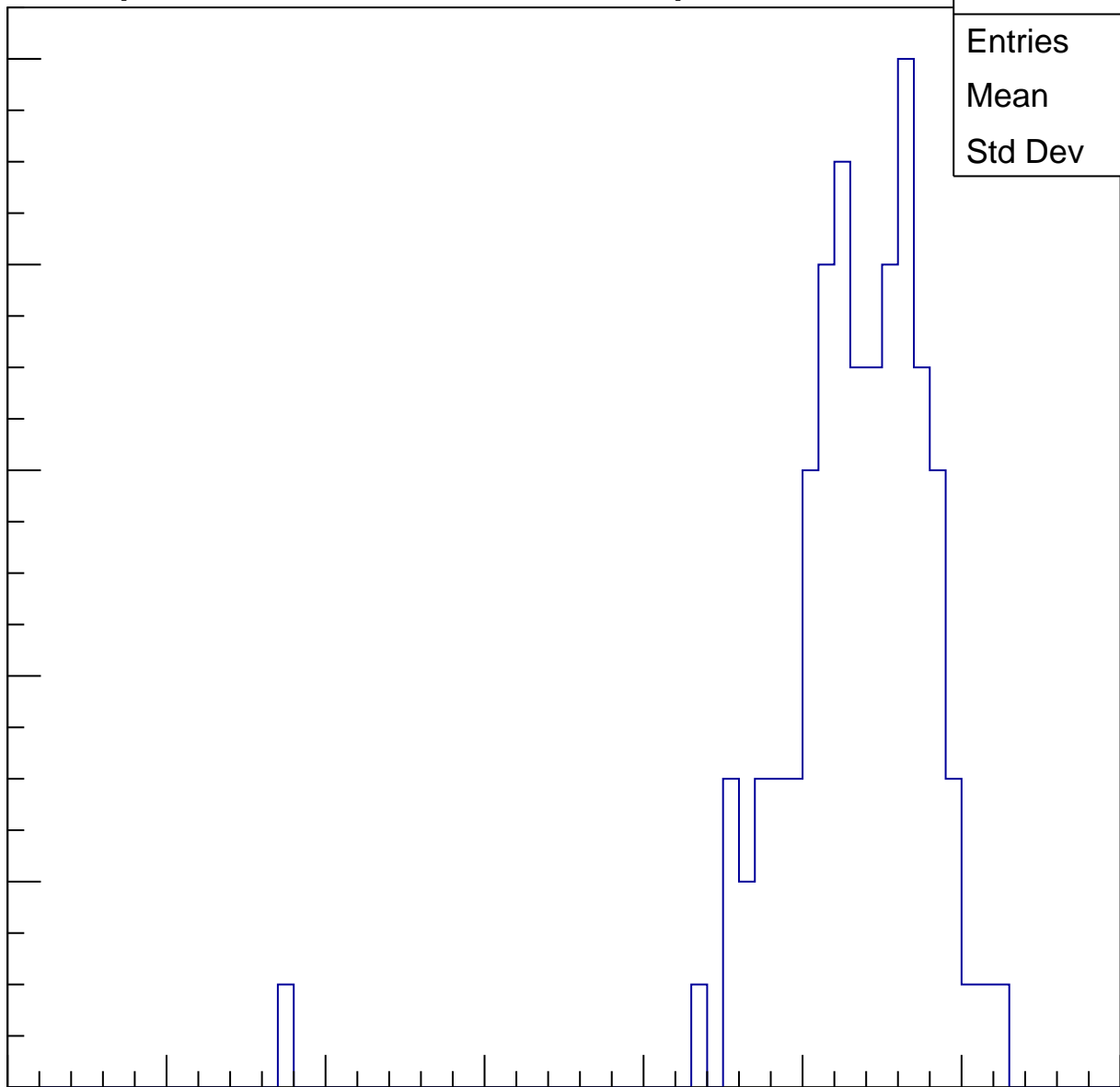
40

50

60

70

ampl

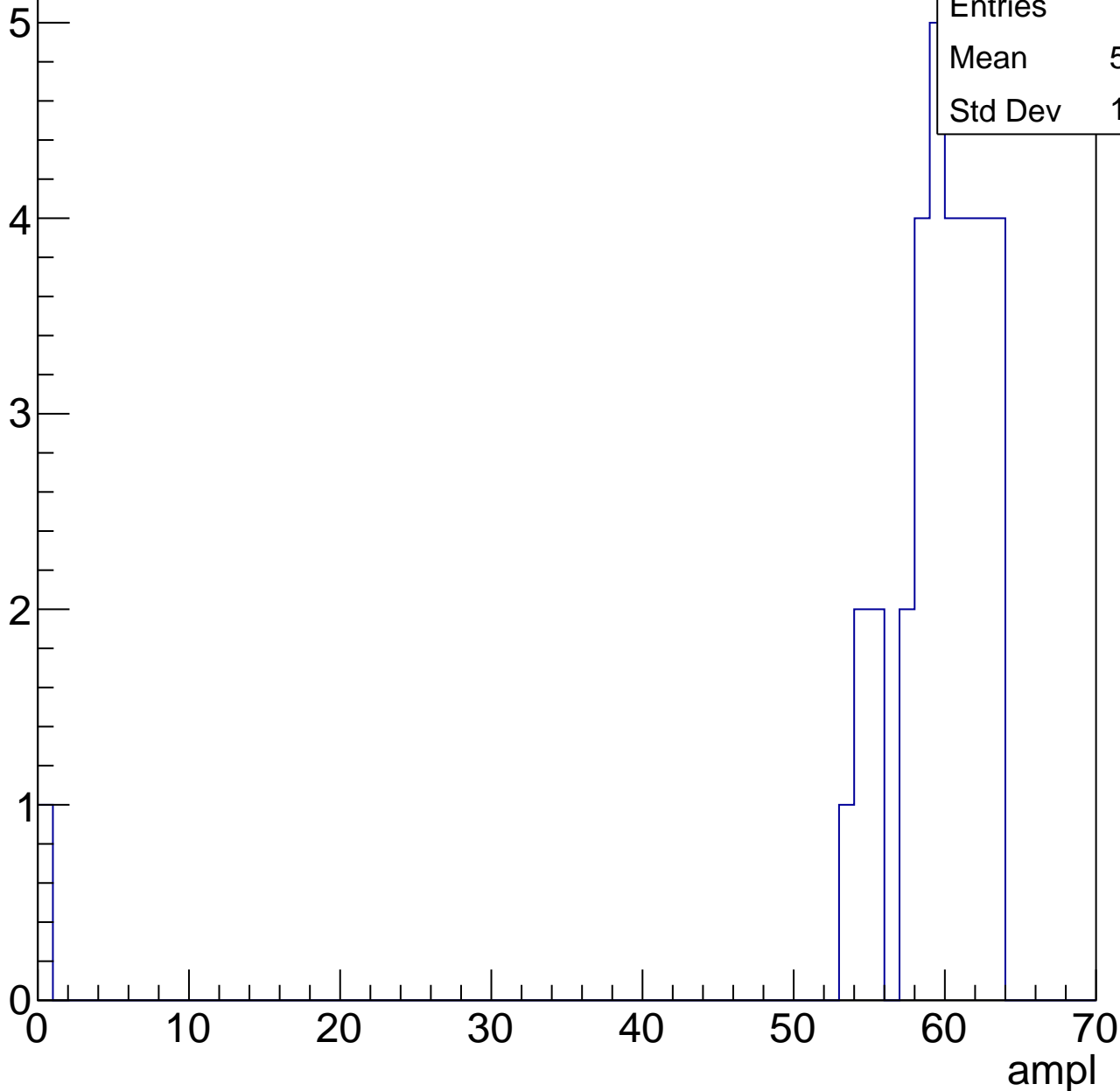


# B1L101S, U22-ch56, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	33
Mean	57.45
Std Dev	10.52

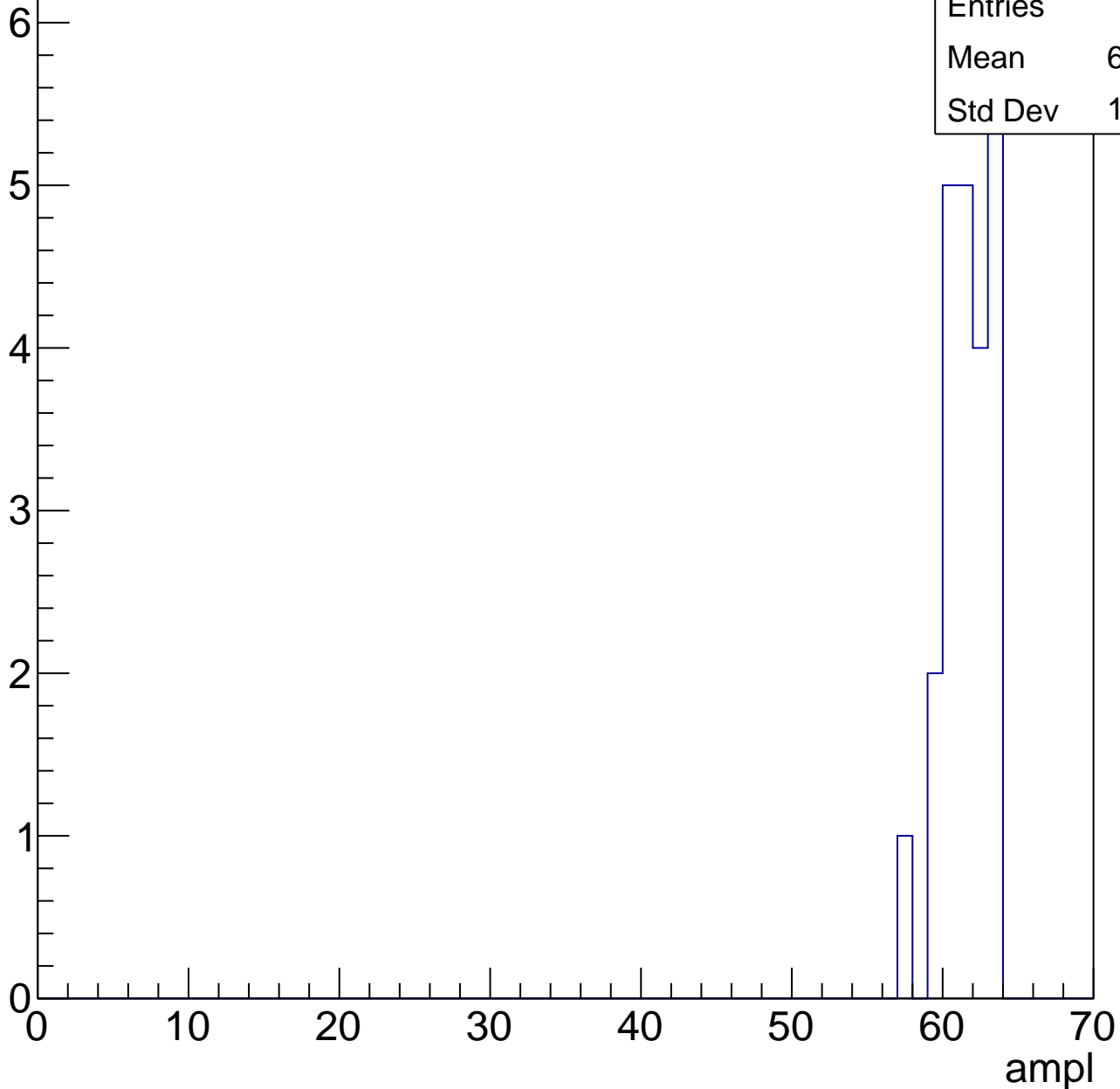


# B1L101S, U22-ch56, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	23
Mean	61.13
Std Dev	1.569



# B1L101S, U22-ch56, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	62
Std Dev	0



# B1L101S, U22-ch56, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



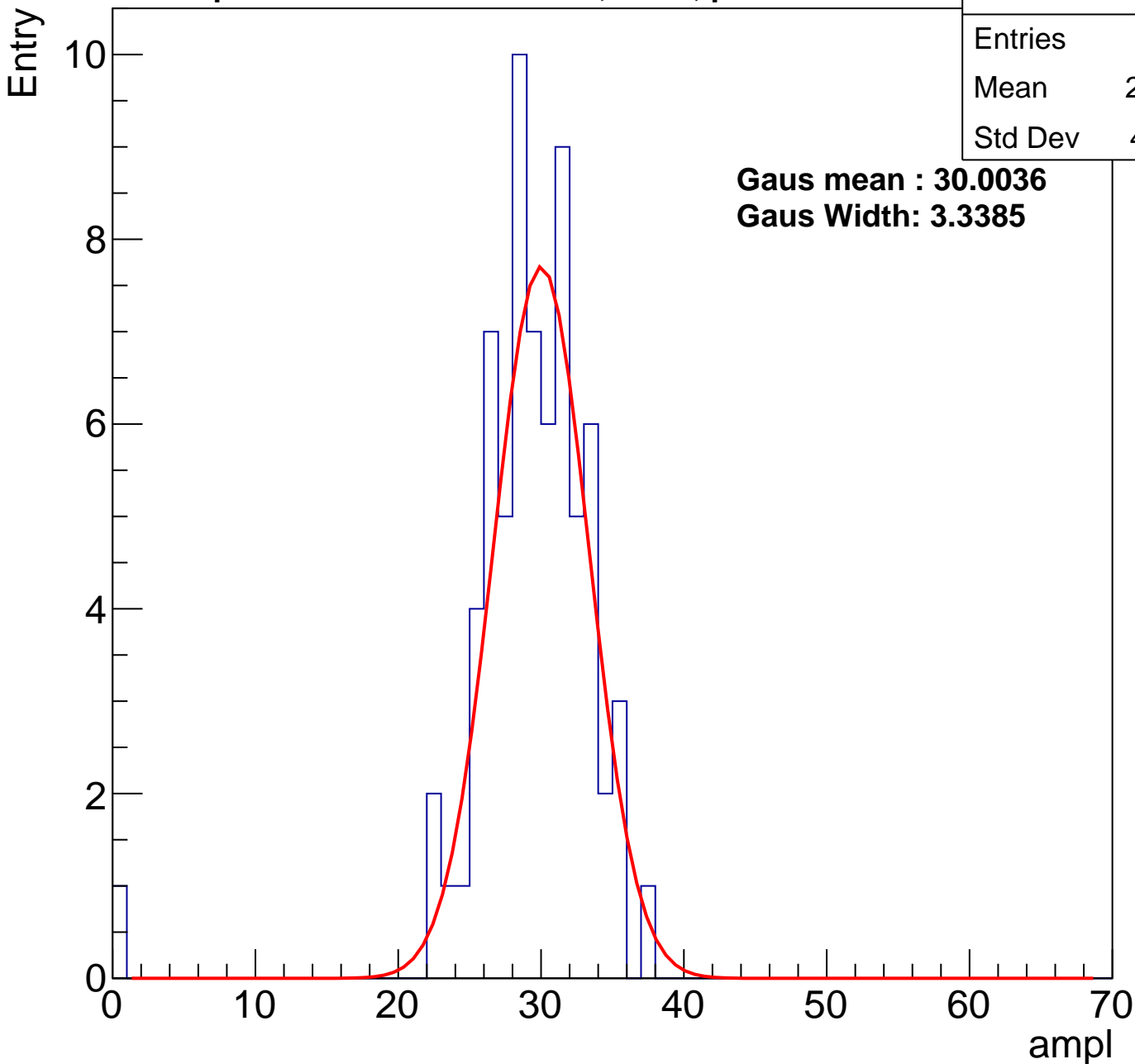
# B1L101S, U22-ch57, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	70
Mean	28.83
Std Dev	4.721

**Gaus mean : 30.0036**

**Gaus Width: 3.3385**



# B1L101S, U22-ch57, adc1

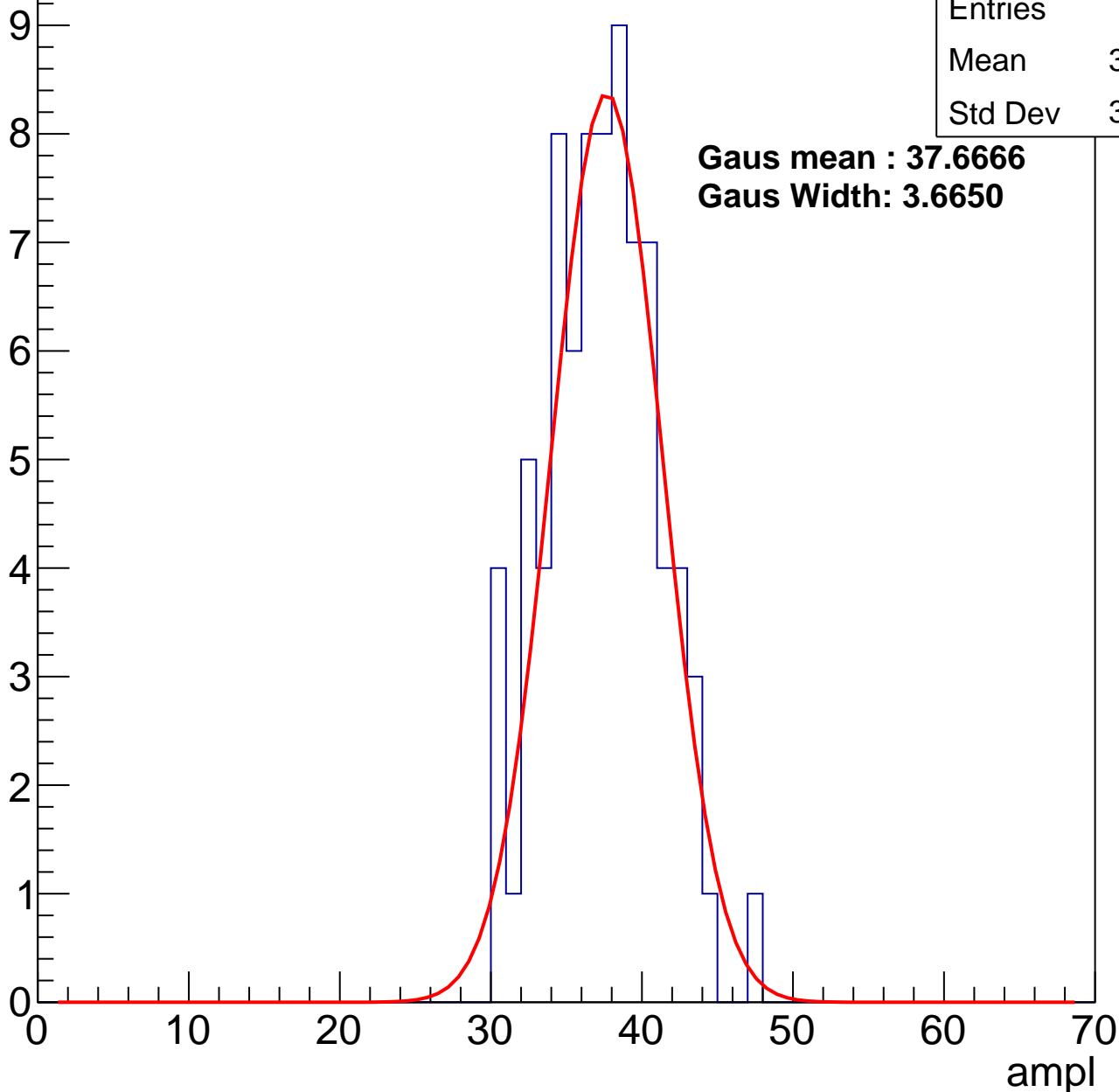
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	80
Mean	36.95
Std Dev	3.616

**Gaus mean : 37.6666**

**Gaus Width: 3.6650**



# B1L101S, U22-ch57, adc2

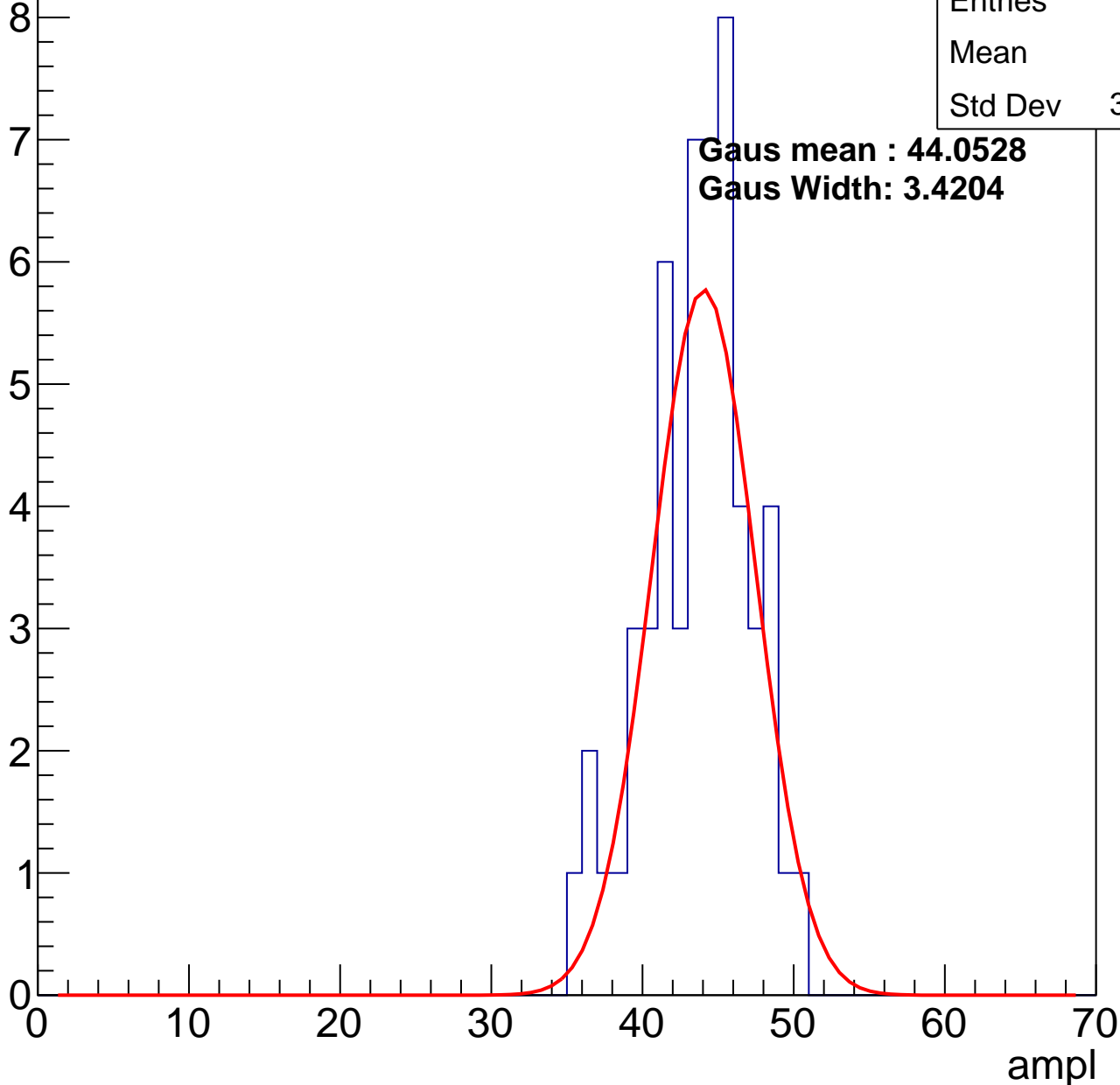
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	55
Mean	43.2
Std Dev	3.387

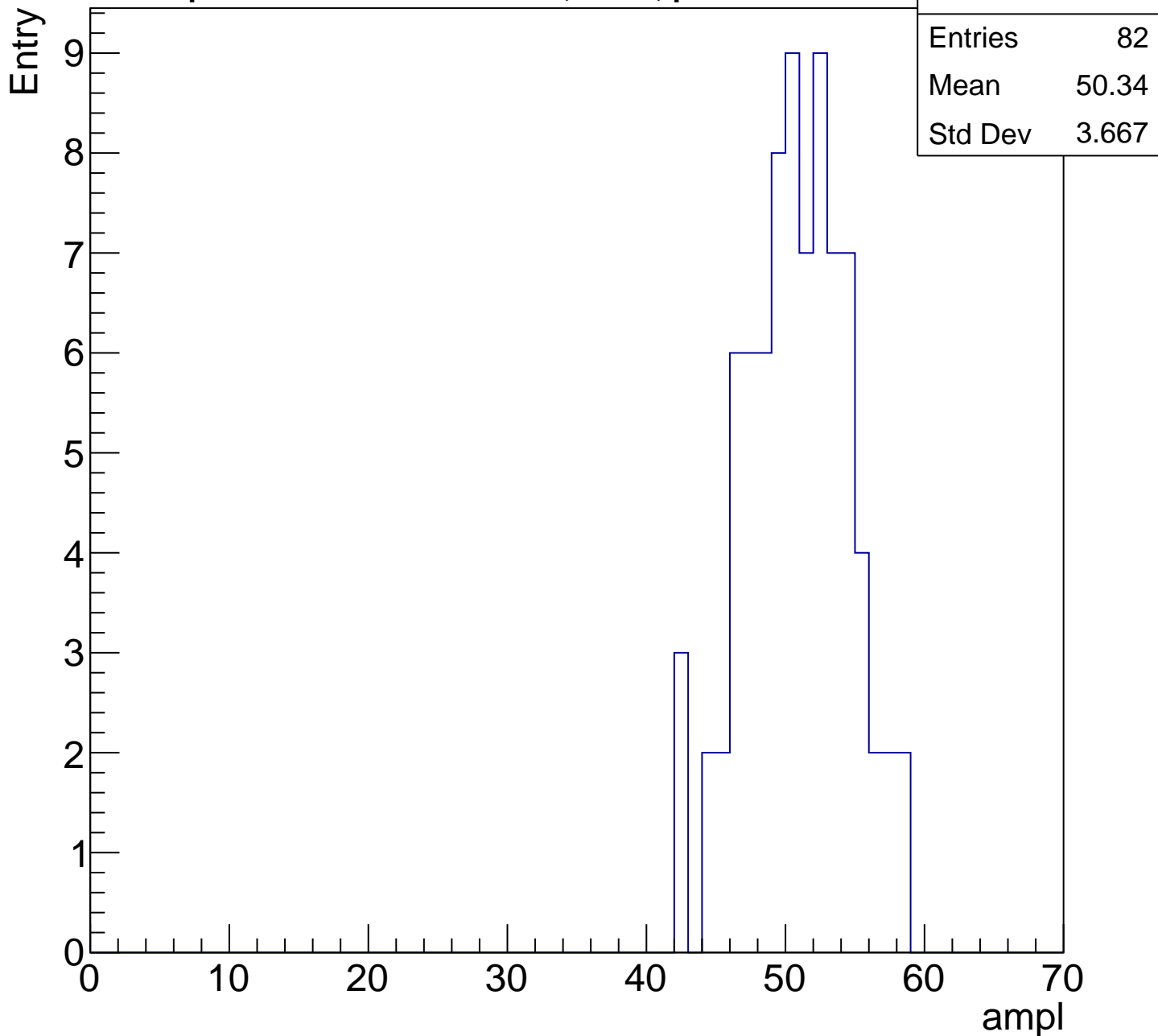
**Gaus mean : 44.0528**

**Gaus Width: 3.4204**



# B1L101S, U22-ch57, adc3

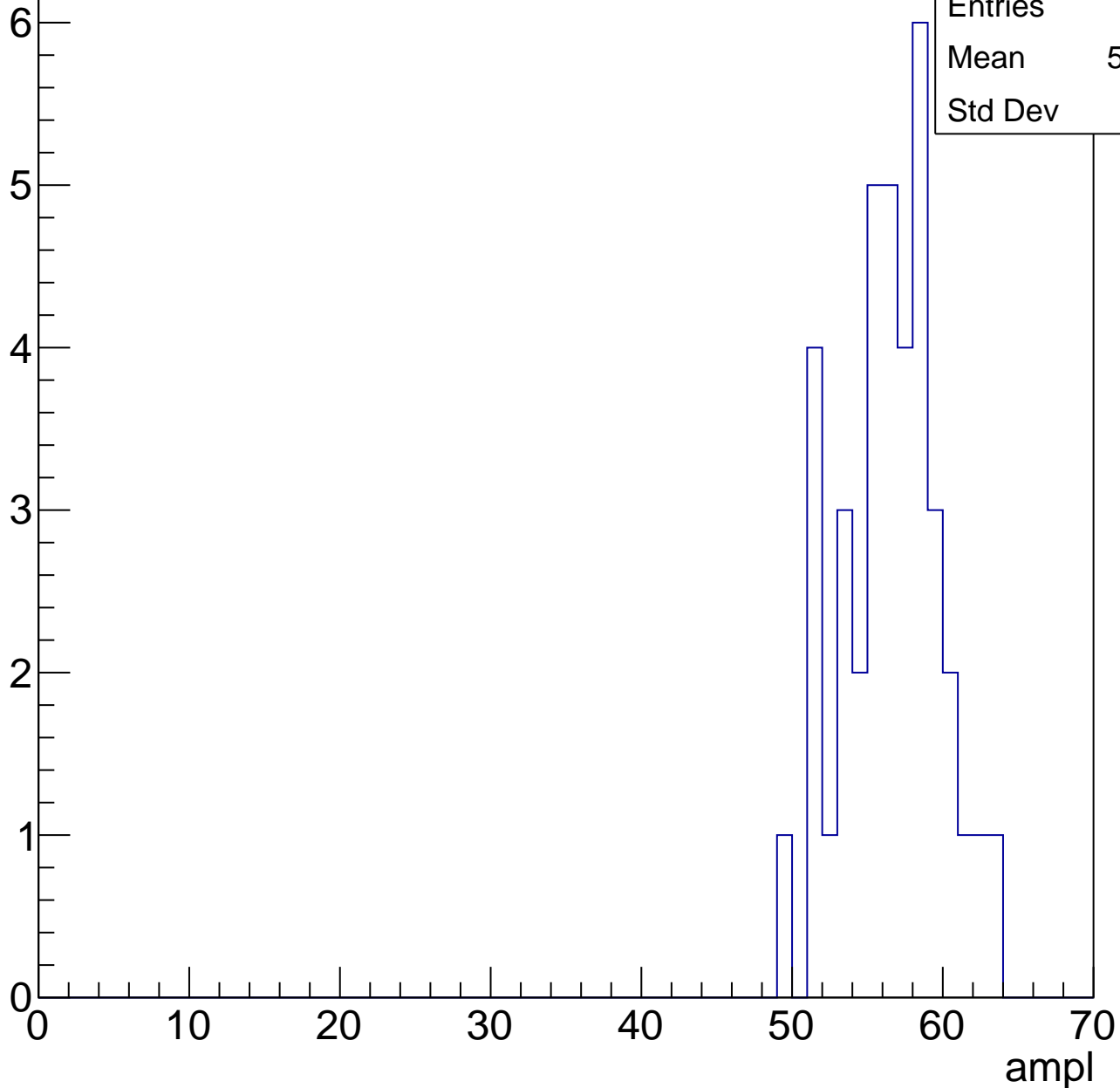
calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U22-ch57, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	39
Mean	56.05
Std Dev	3.21

# B1L101S, U22-ch57, adc5

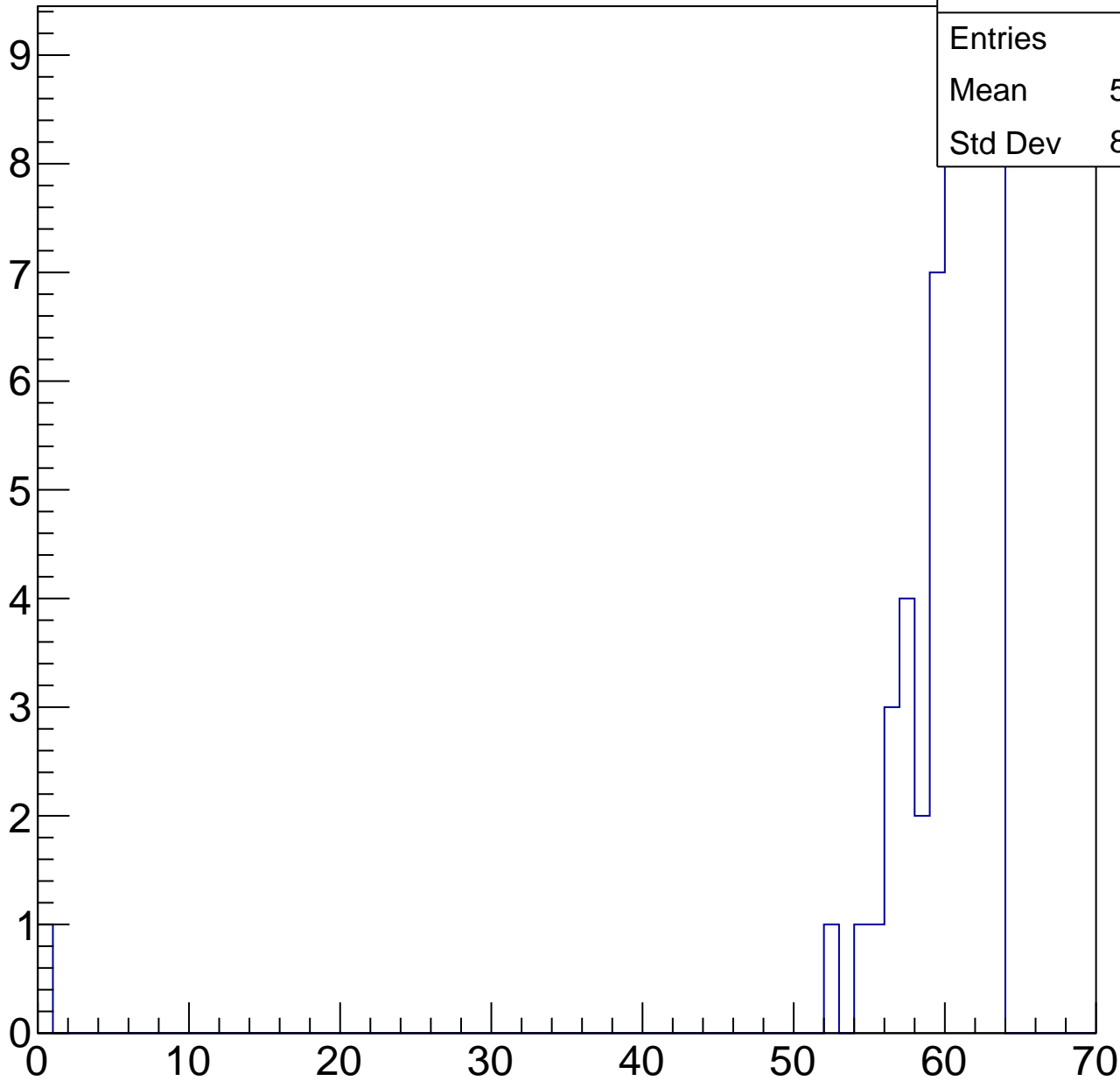
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	54
Mean	58.83
Std Dev	8.463

ampl



# B1L101S, U22-ch57, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U22-ch57, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U22-ch58, adc0

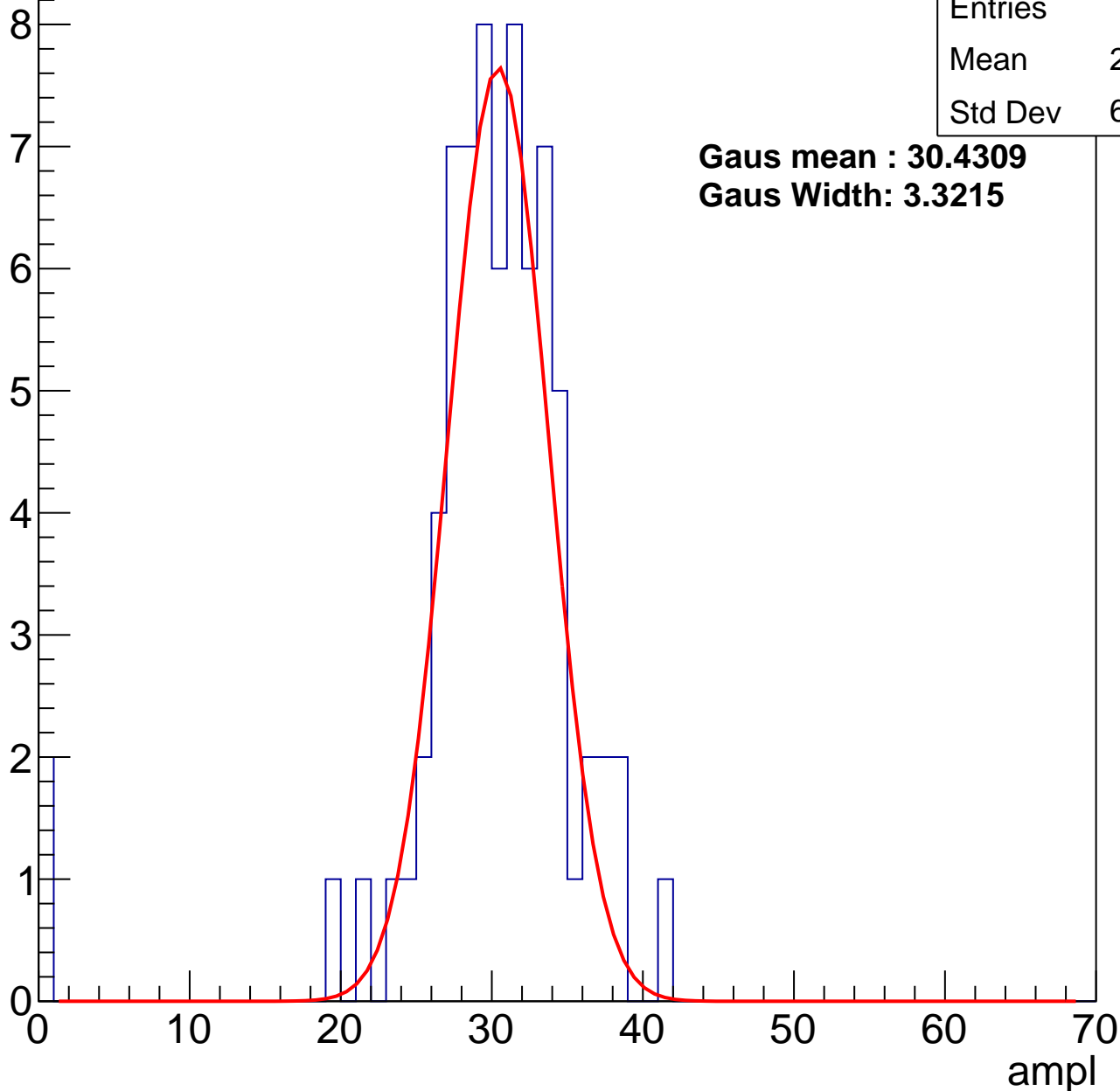
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	74
Mean	29.42
Std Dev	6.254

**Gaus mean : 30.4309**

**Gaus Width: 3.3215**



# B1L101S, U22-ch58, adc1

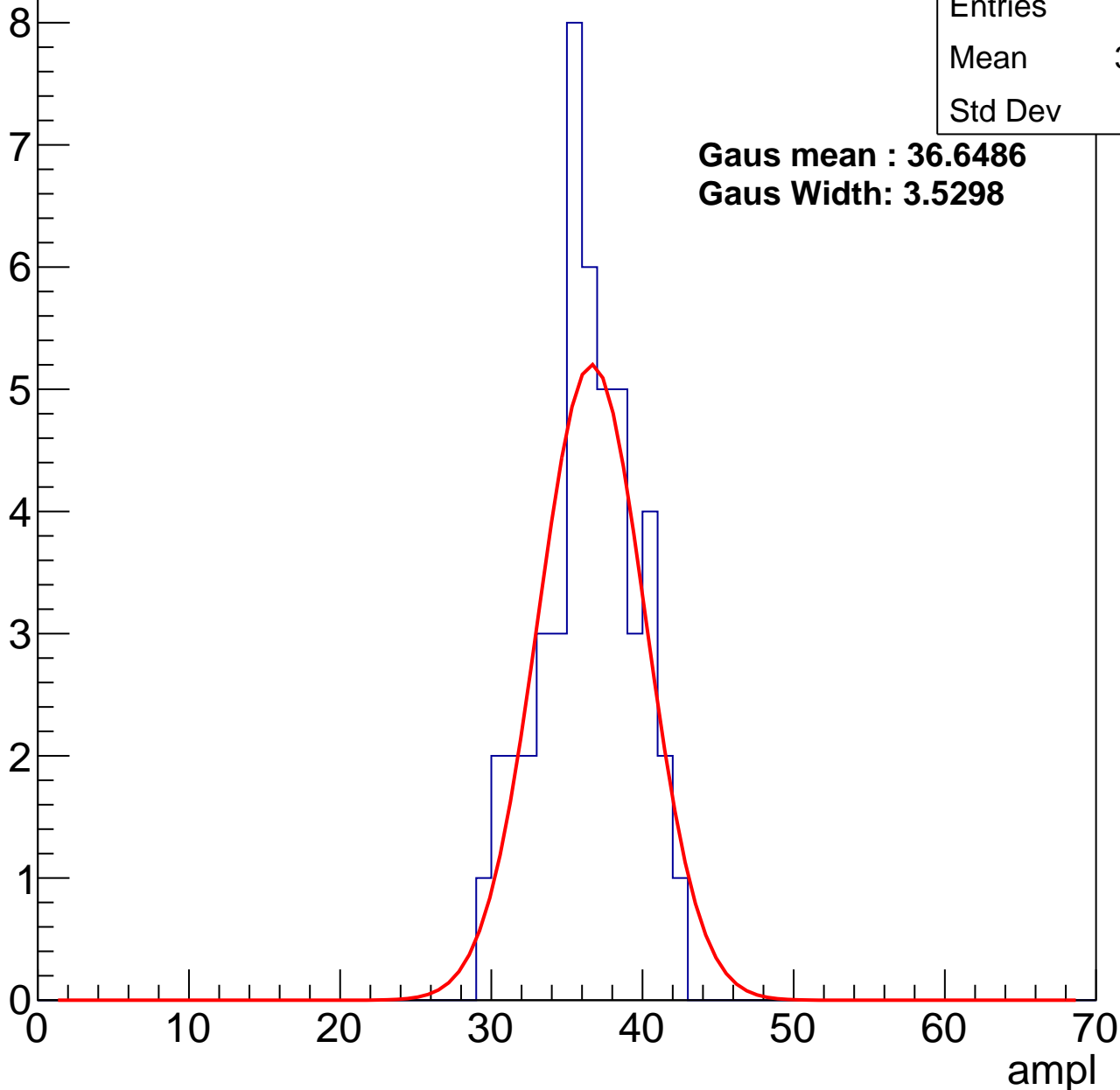
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	47
Mean	35.91
Std Dev	3.1

**Gaus mean : 36.6486**

**Gaus Width: 3.5298**



# B1L101S, U22-ch58, adc2

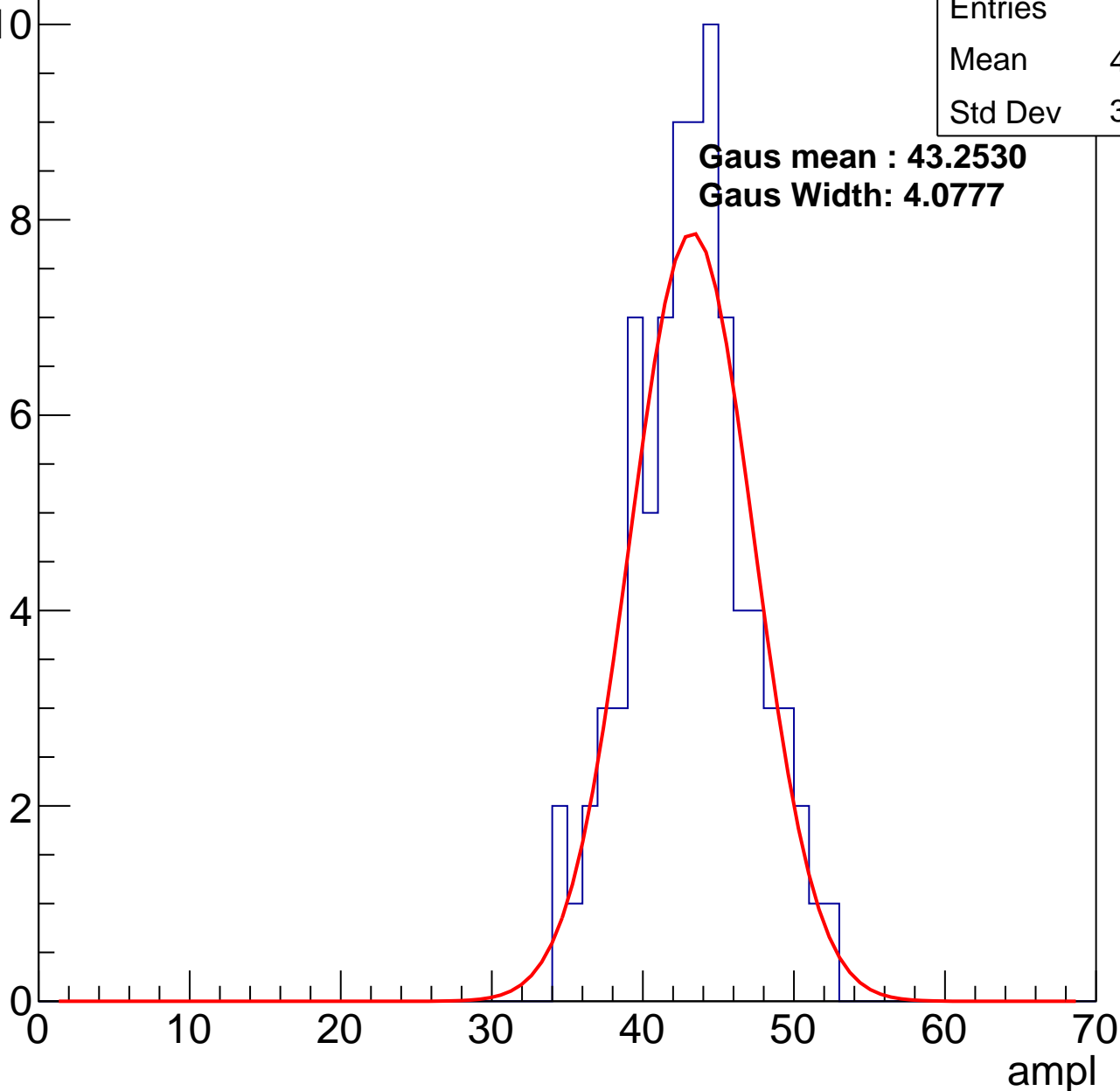
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	83
Mean	42.72
Std Dev	3.894

**Gaus mean : 43.2530**

**Gaus Width: 4.0777**

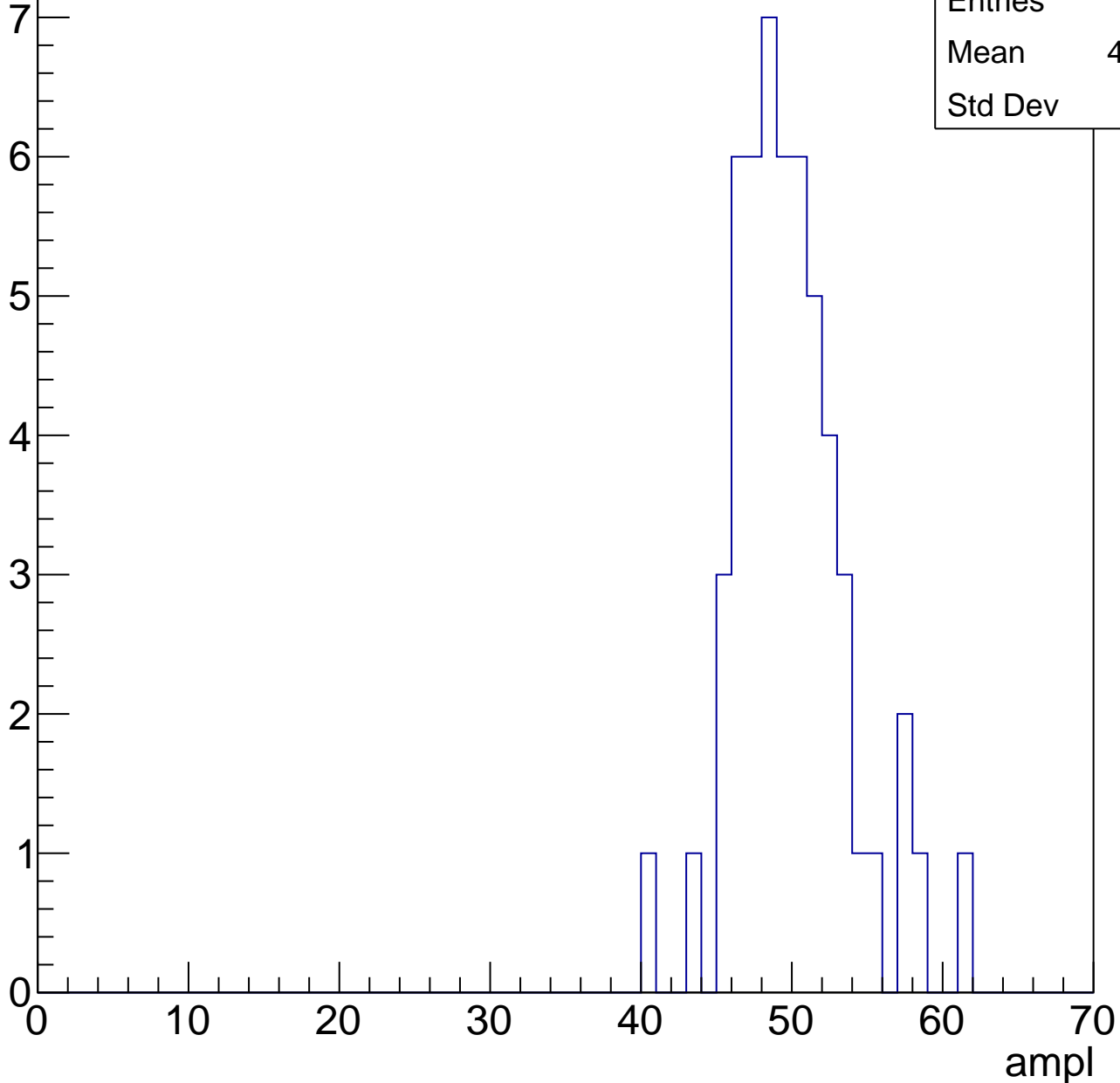


# B1L101S, U22-ch58, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	54
Mean	49.44
Std Dev	3.76



# B1L101S, U22-ch58, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	80
Mean	56.02
Std Dev	3.305

Entry

10

8

6

4

2

0

0

10

20

30

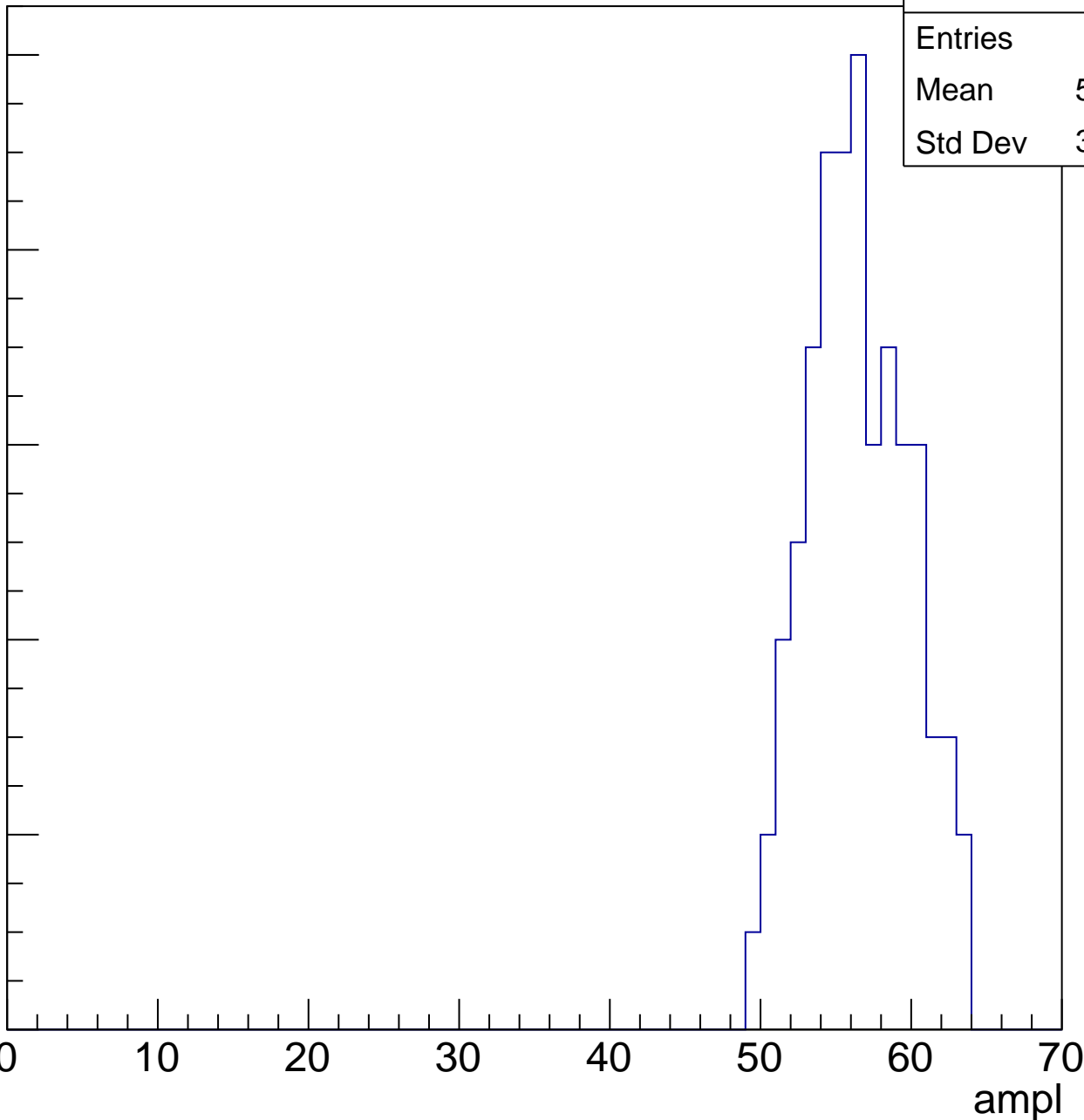
40

50

60

70

ampl



# B1L101S, U22-ch58, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

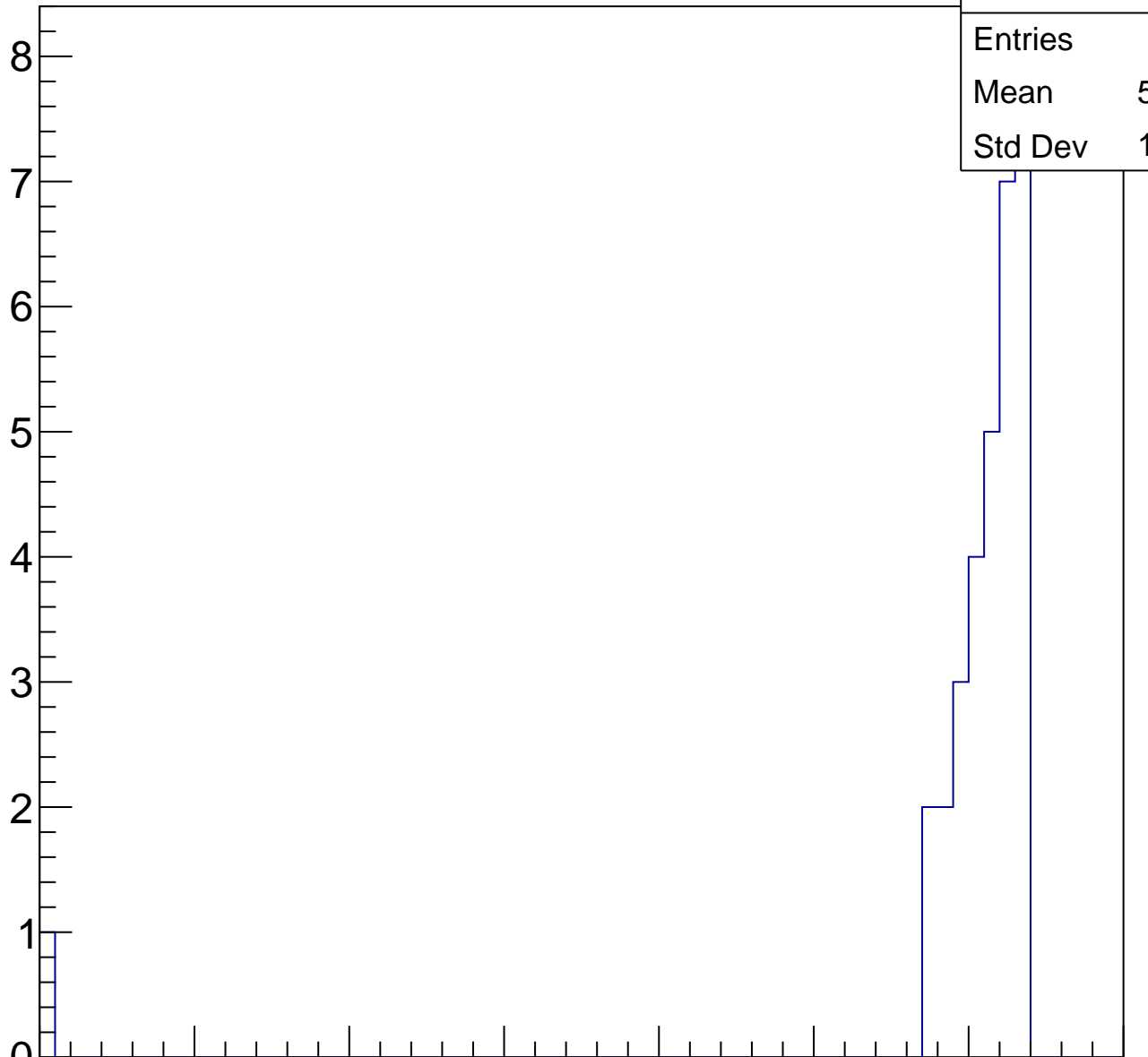
Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	32
Mean	59.06
Std Dev	10.76

ampl

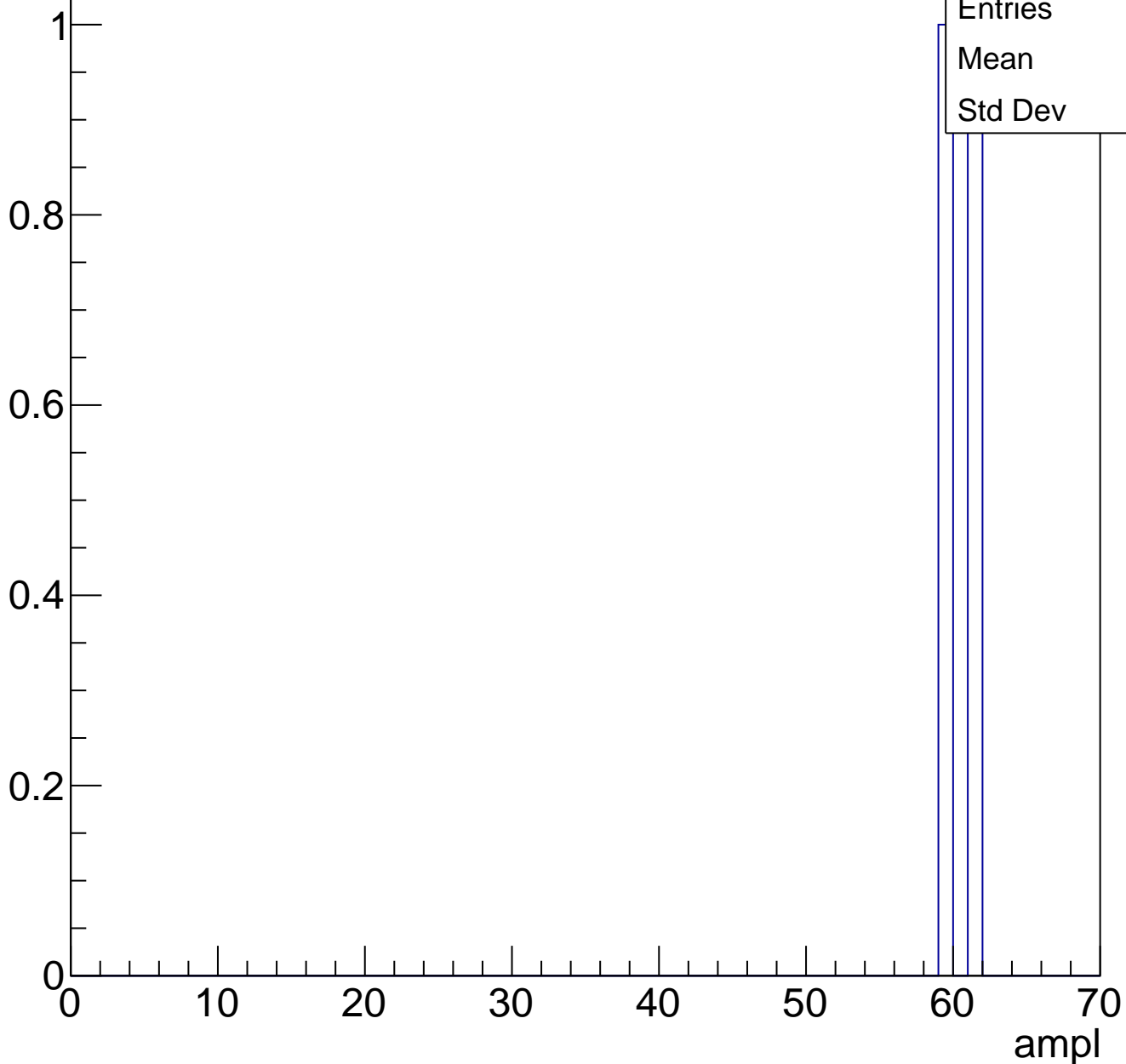
0 10 20 30 40 50 60 70



# B1L101S, U22-ch58, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U22-ch58, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U22-ch59, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	83
Mean	31.63
Std Dev	3.795

**Gaus mean : 32.0065**

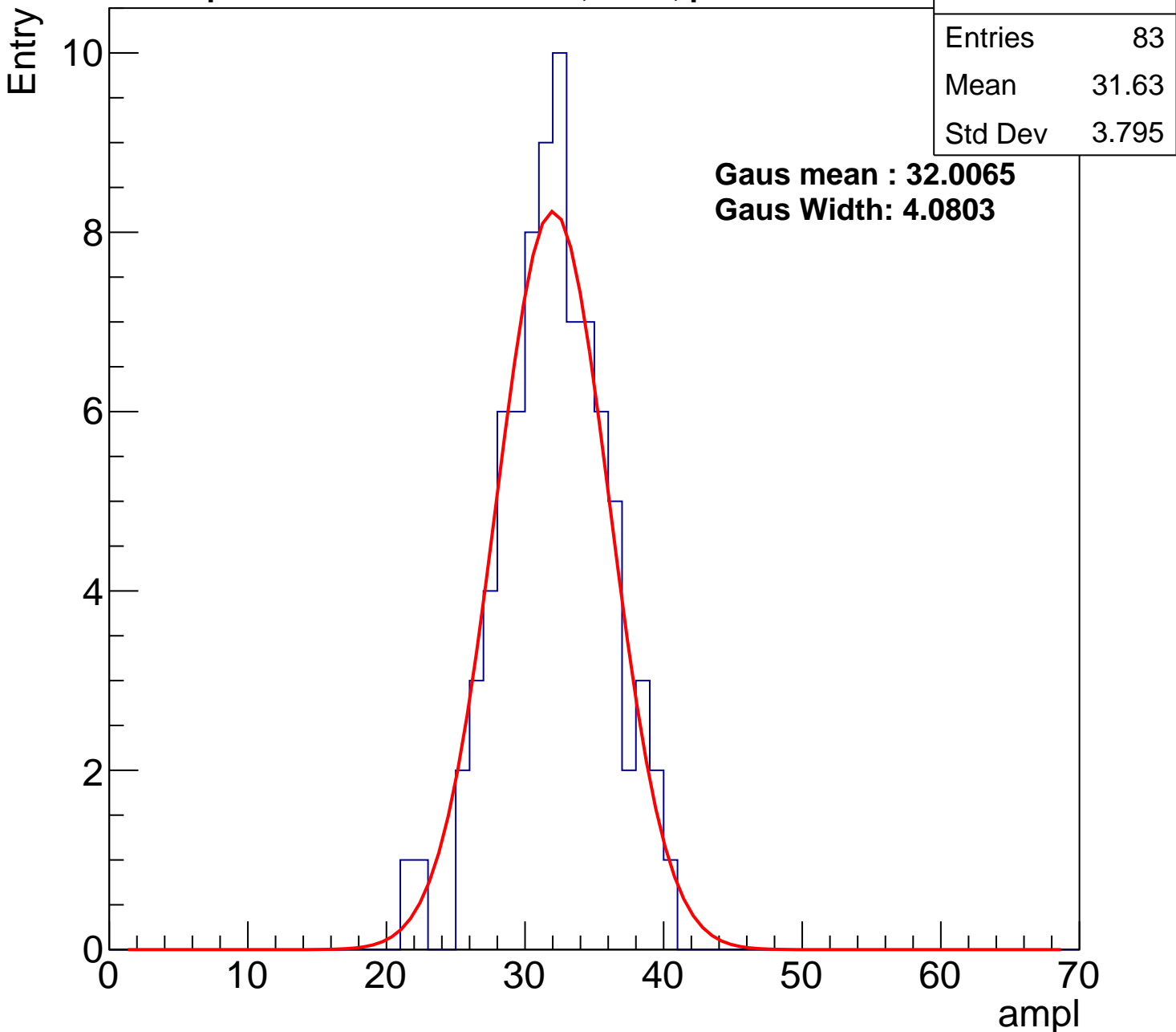
**Gaus Width: 4.0803**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U22-ch59, adc1

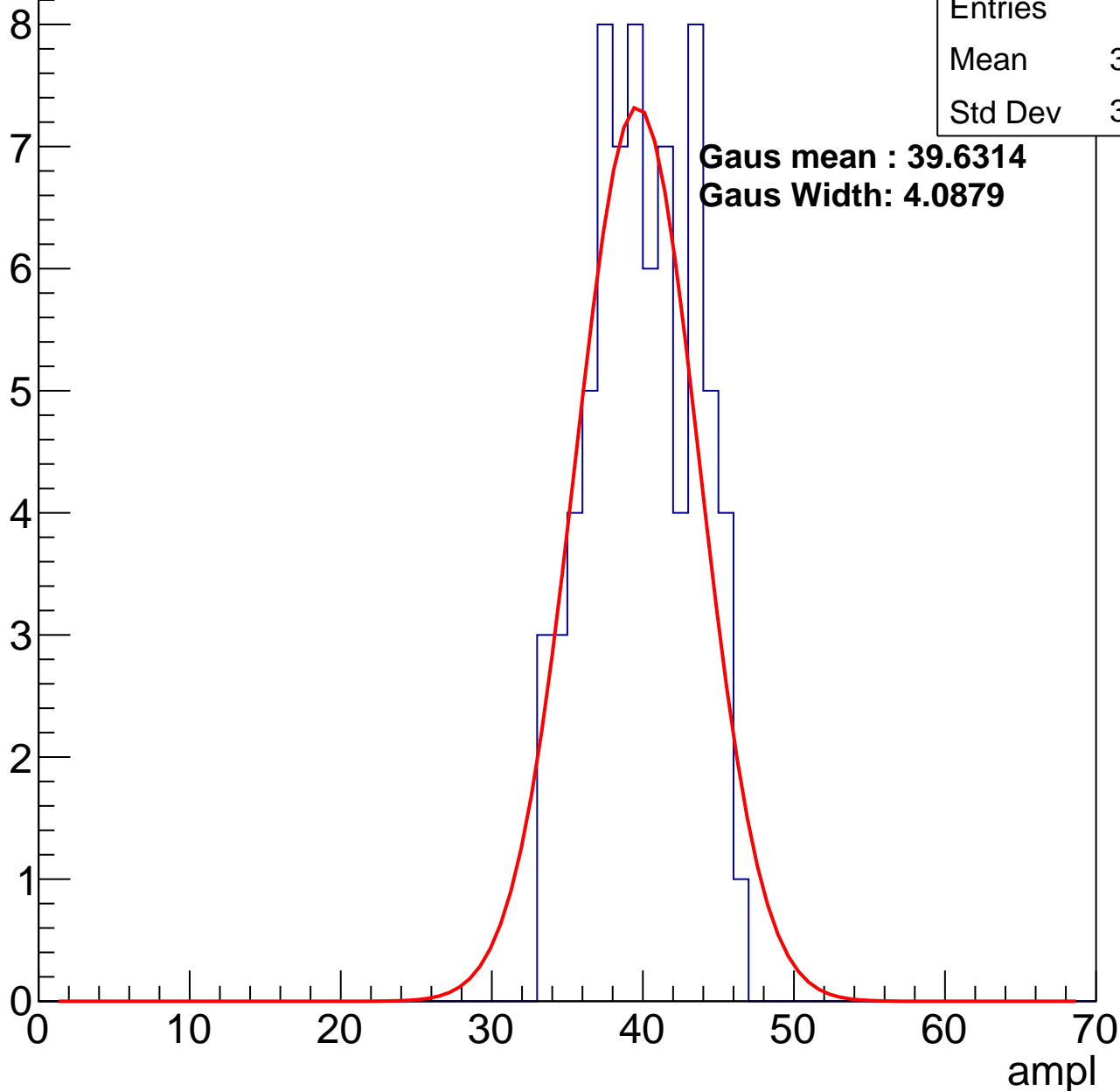
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	73
Mean	39.45
Std Dev	3.376

**Gaus mean : 39.6314**

**Gaus Width: 4.0879**



# B1L101S, U22-ch59, adc2

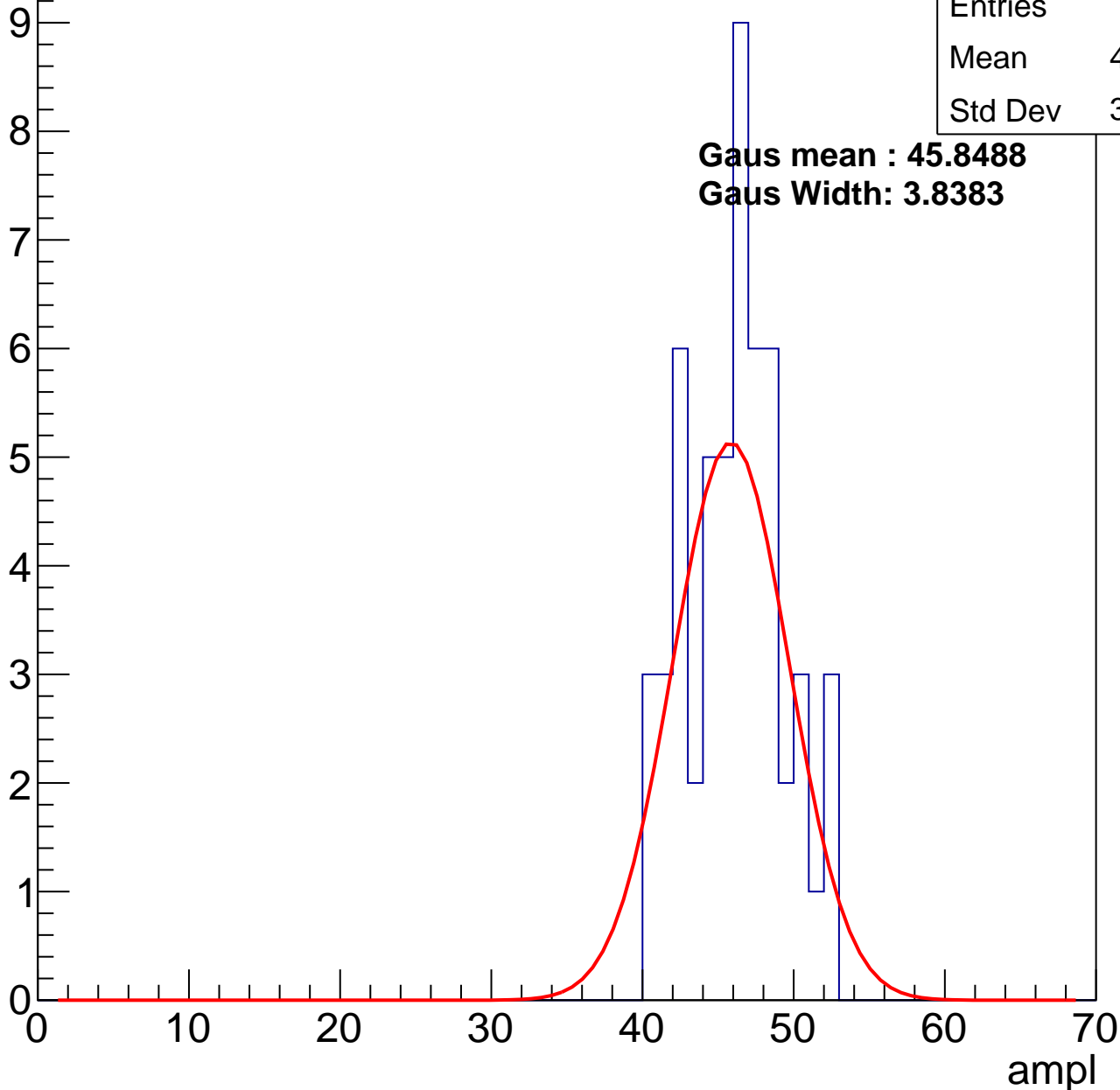
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	54
Mean	45.65
Std Dev	3.175

**Gaus mean : 45.8488**

**Gaus Width: 3.8383**

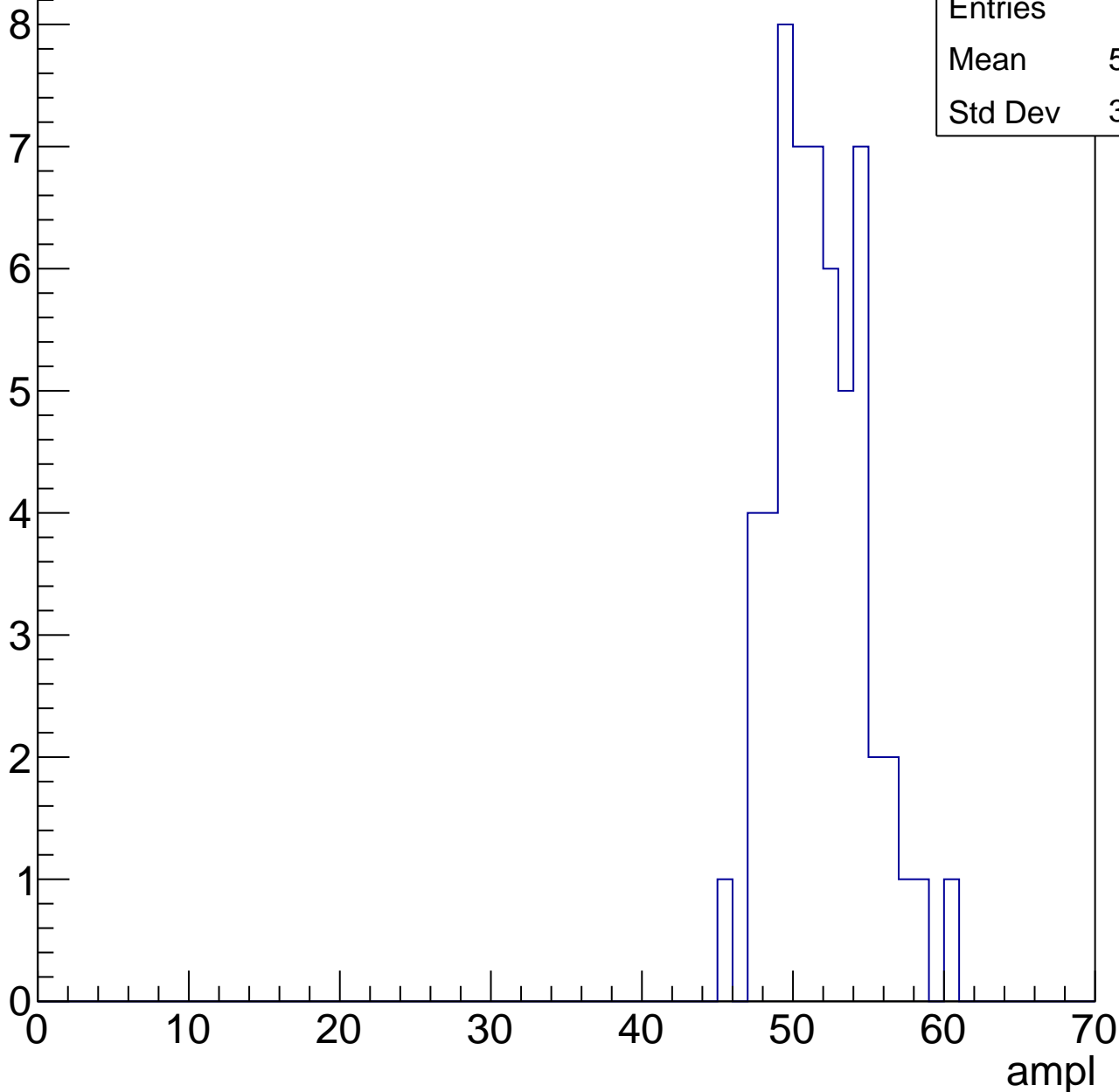


# B1L101S, U22-ch59, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

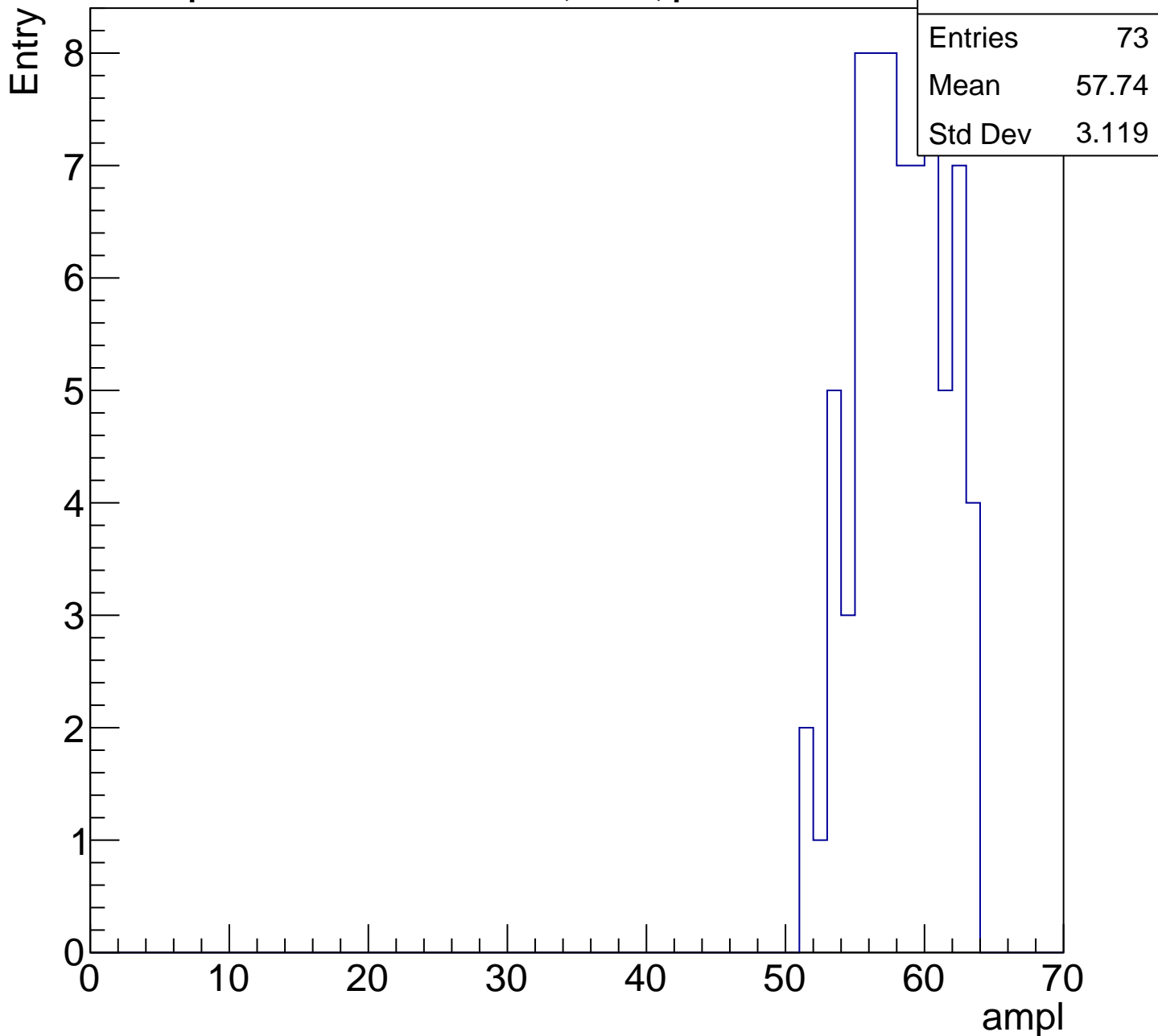
Entry

Entries	56
Mean	51.36
Std Dev	3.003



# B1L101S, U22-ch59, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

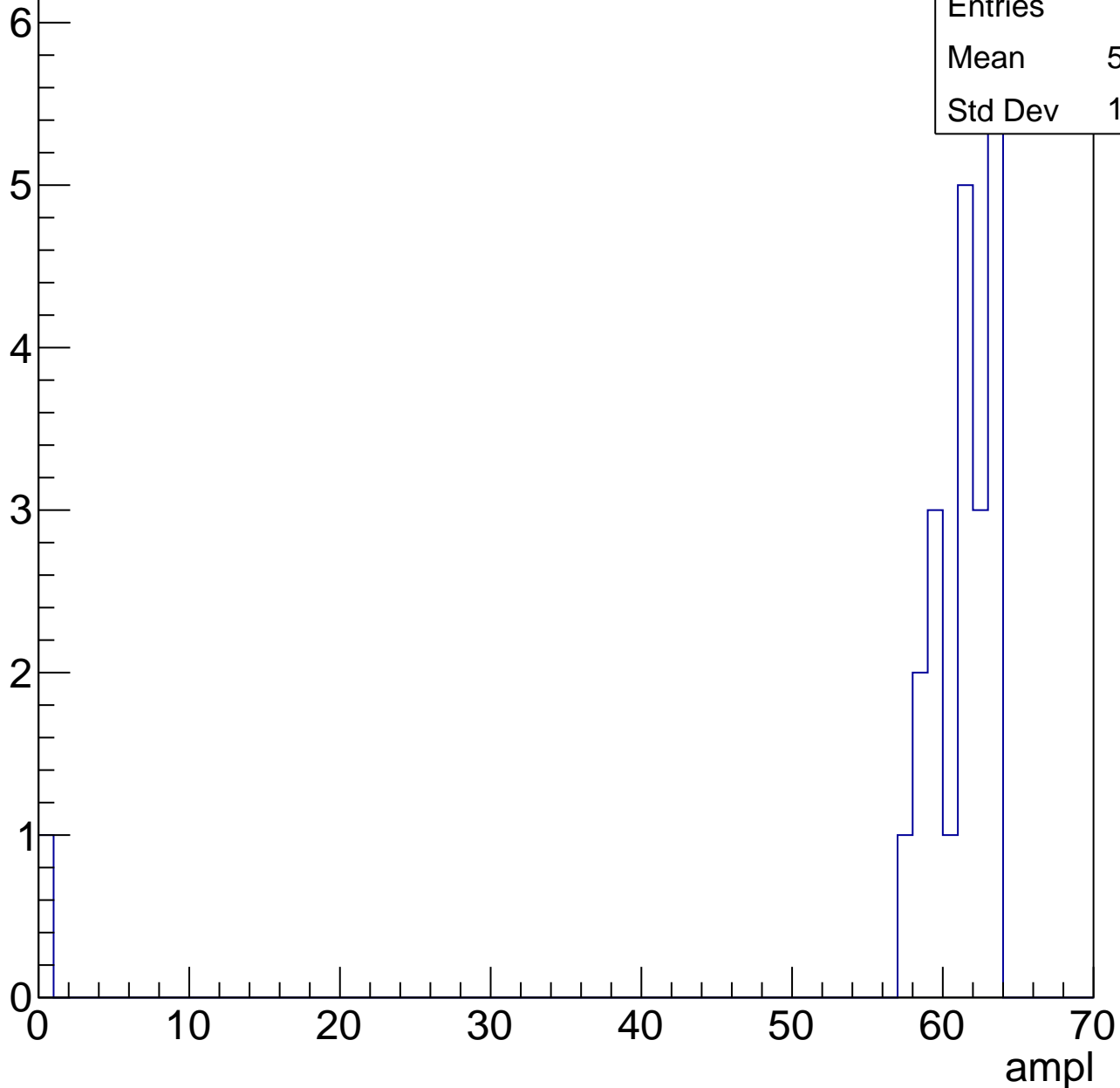


# B1L101S, U22-ch59, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	22
Mean	58.14
Std Dev	12.82



# B1L101S, U22-ch59, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0



# B1L101S, U22-ch59, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U22-ch60, adc0

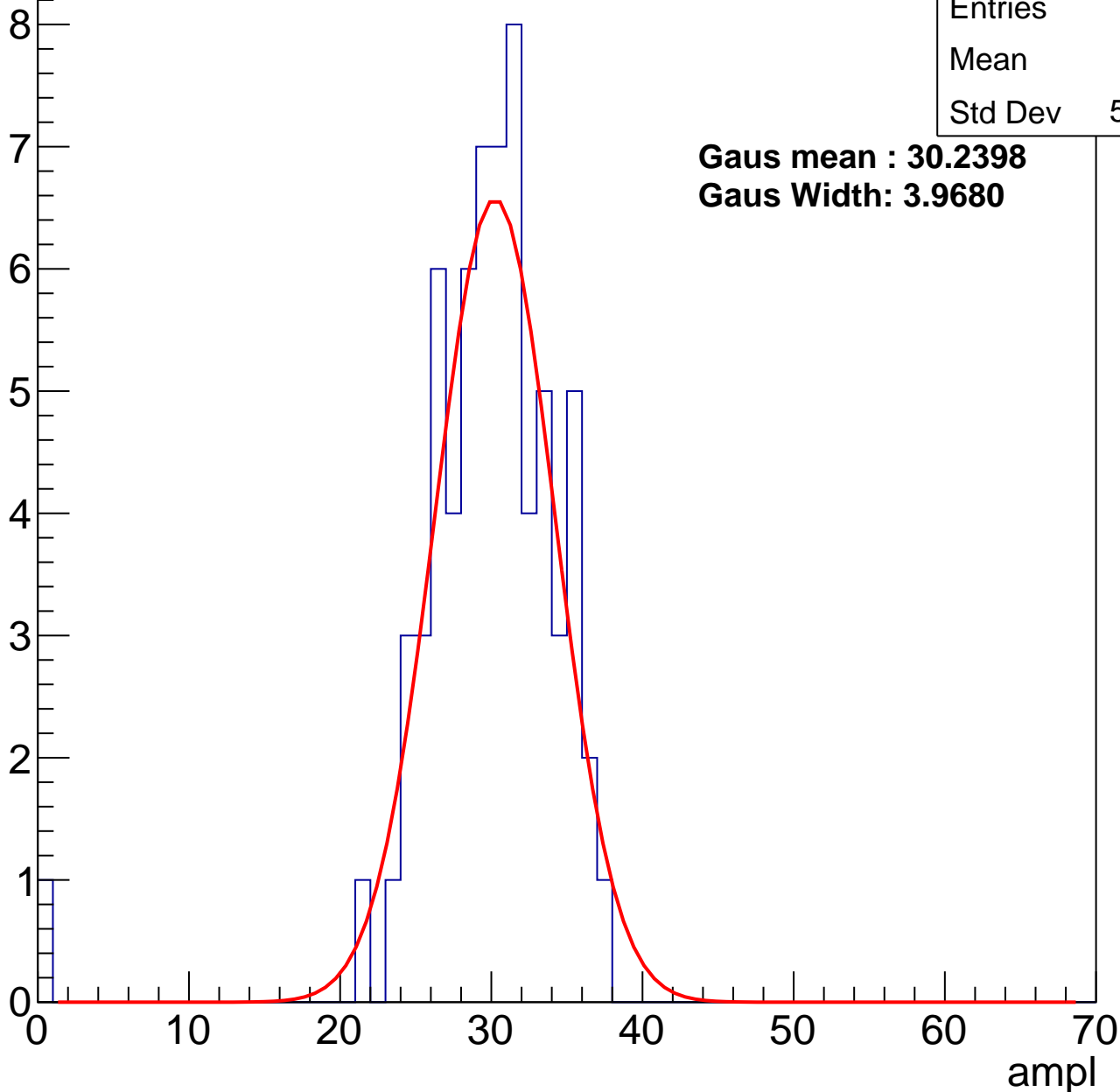
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	67
Mean	29.3
Std Dev	5.046

**Gaus mean : 30.2398**

**Gaus Width: 3.9680**



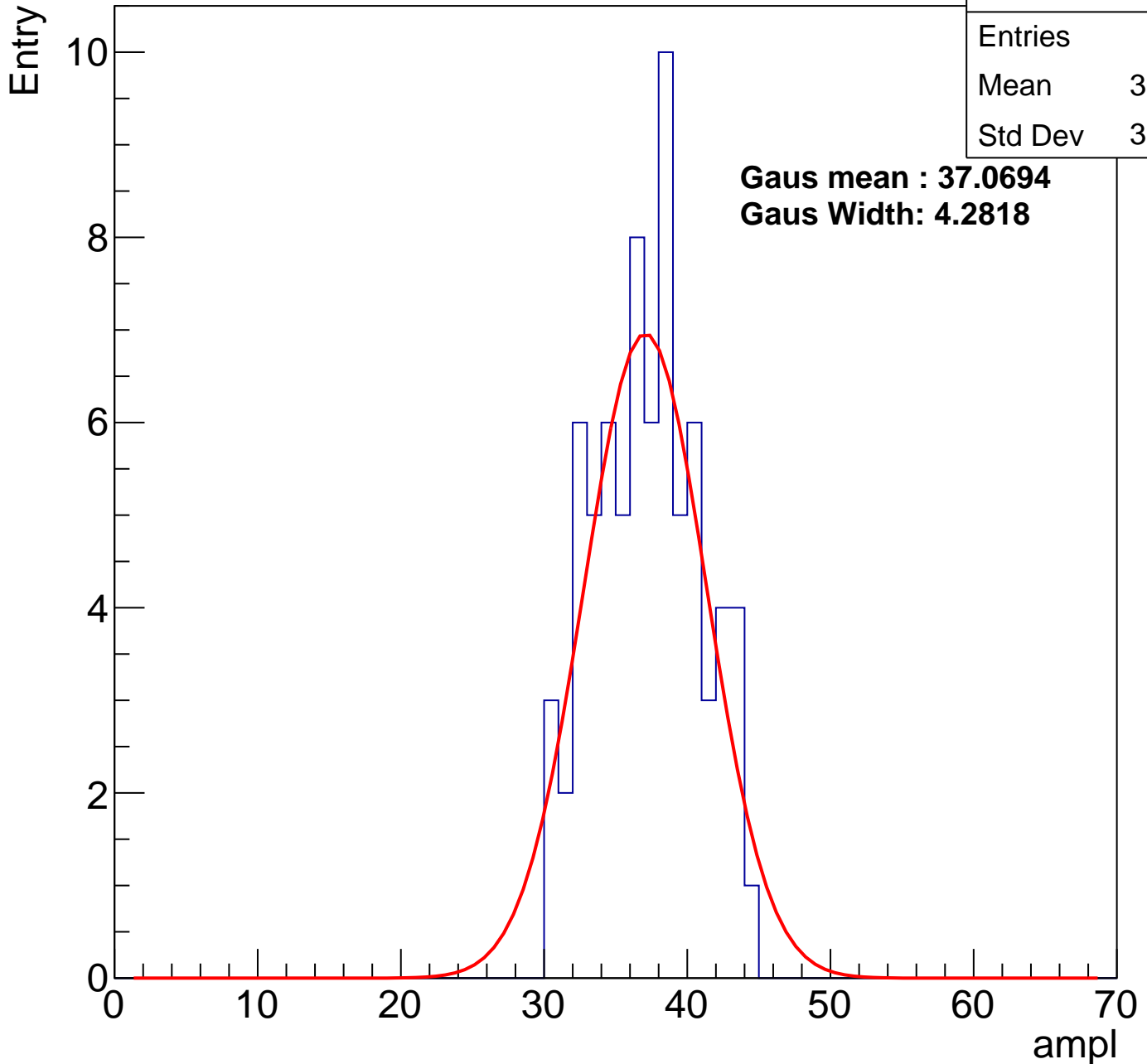
# B1L101S, U22-ch60, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	74
Mean	36.76
Std Dev	3.586

**Gaus mean : 37.0694**

**Gaus Width: 4.2818**



# B1L101S, U22-ch60, adc2

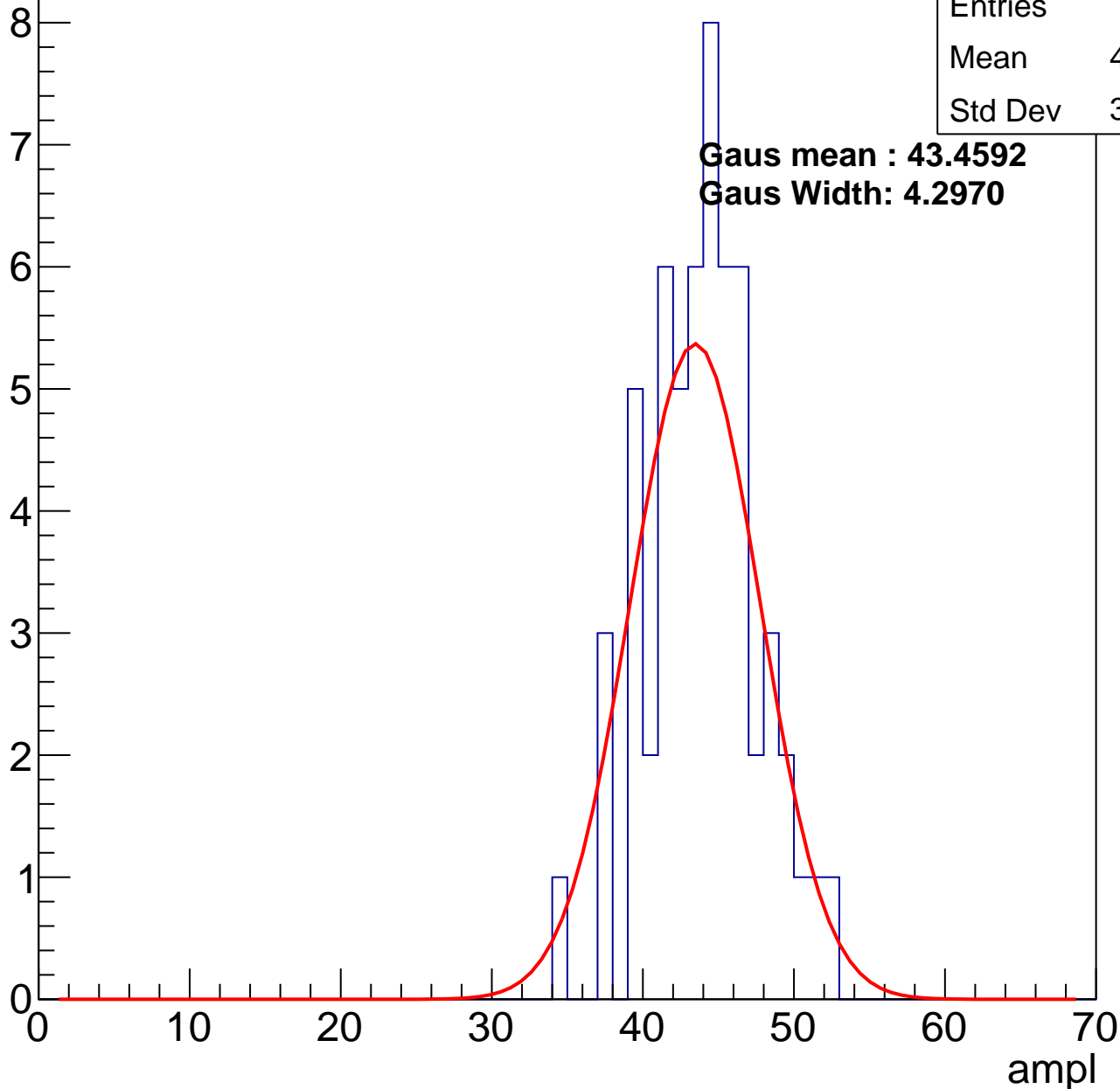
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	58
Mean	43.47
Std Dev	3.626

**Gaus mean : 43.4592**

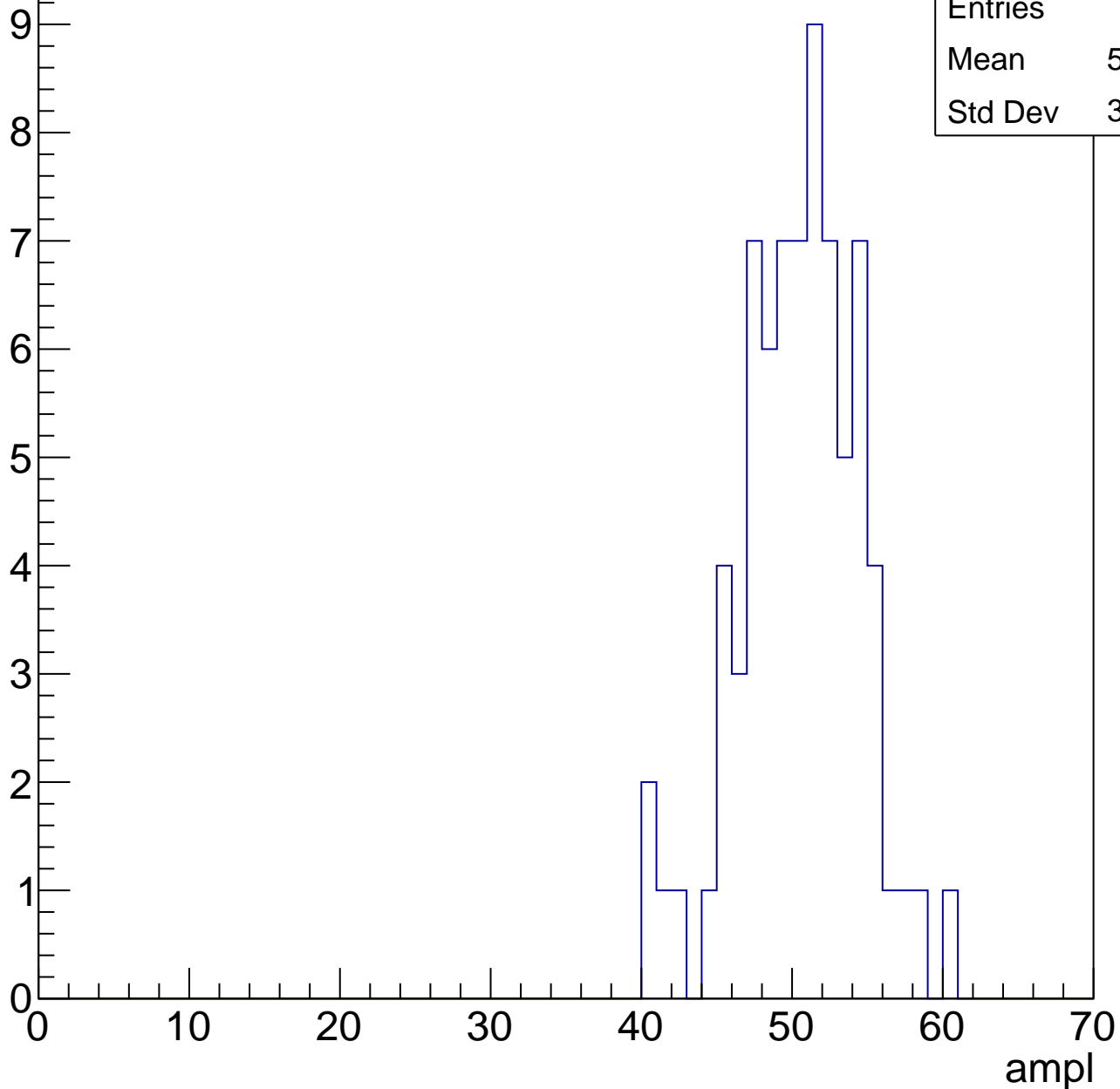
**Gaus Width: 4.2970**



# B1L101S, U22-ch60, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

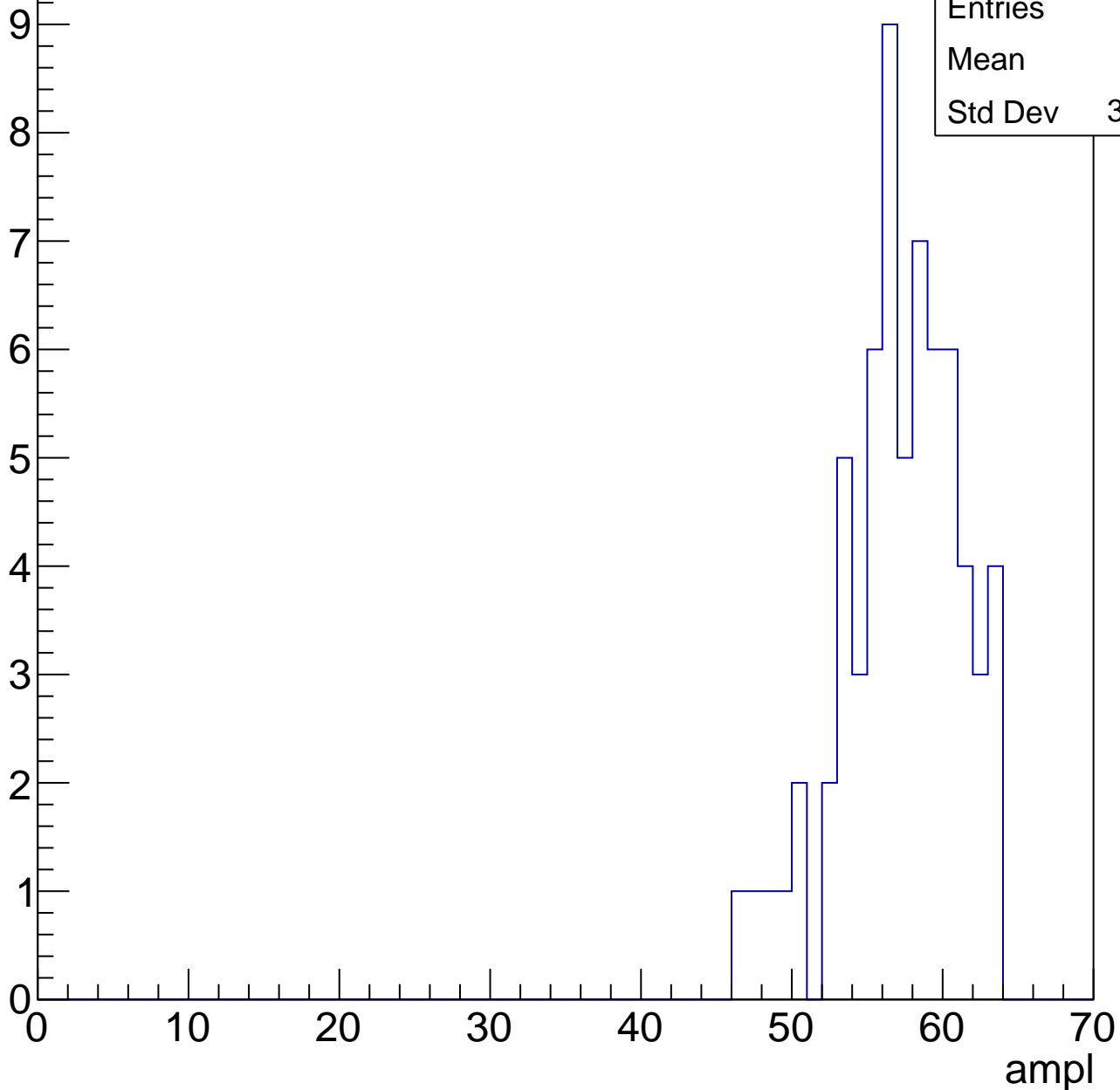


# B1L101S, U22-ch60, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	66
Mean	56.7
Std Dev	3.923

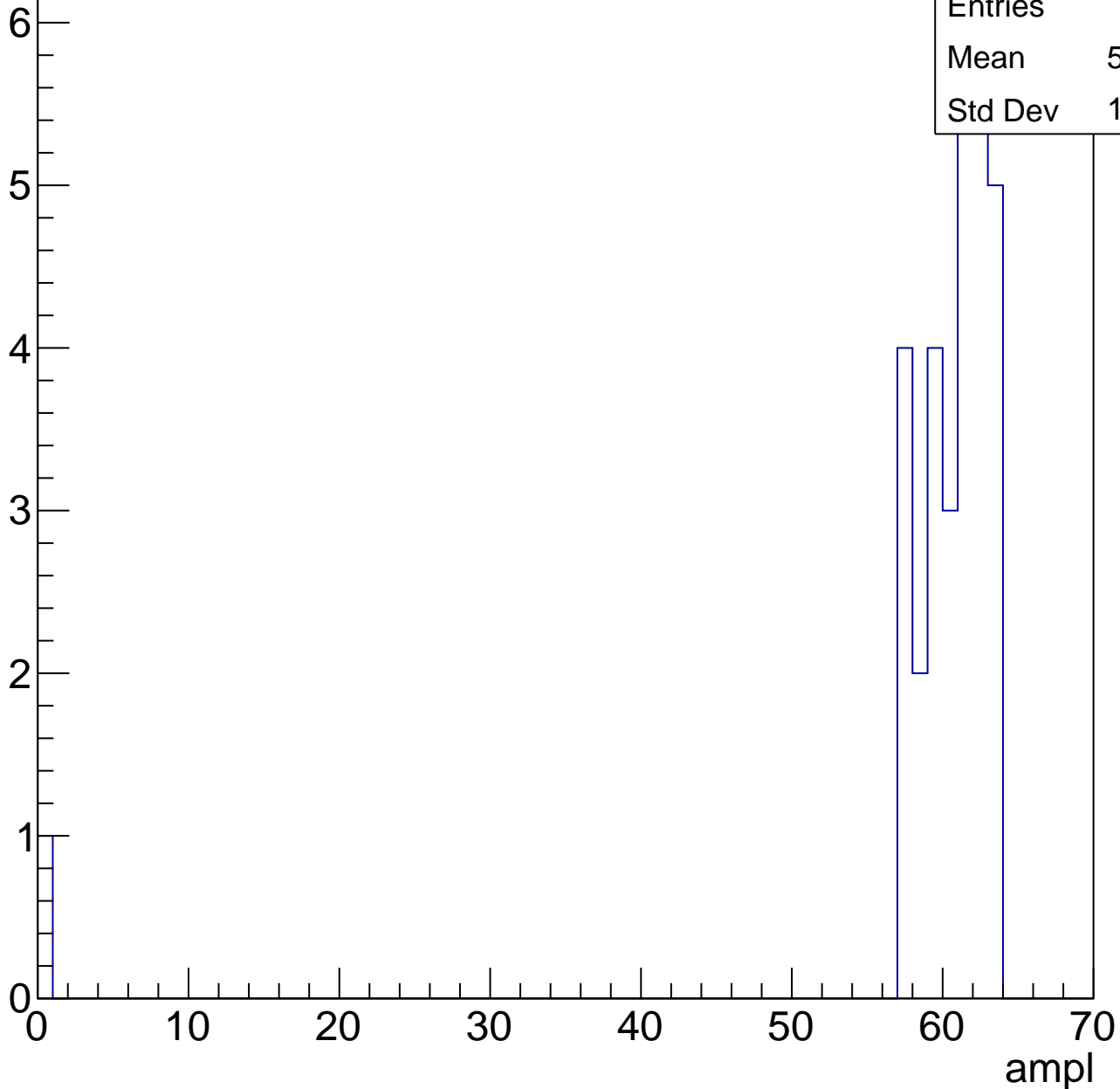


# B1L101S, U22-ch60, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	31
Mean	58.48
Std Dev	10.85



# B1L101S, U22-ch60, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U22-ch60, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U22-ch61, adc0

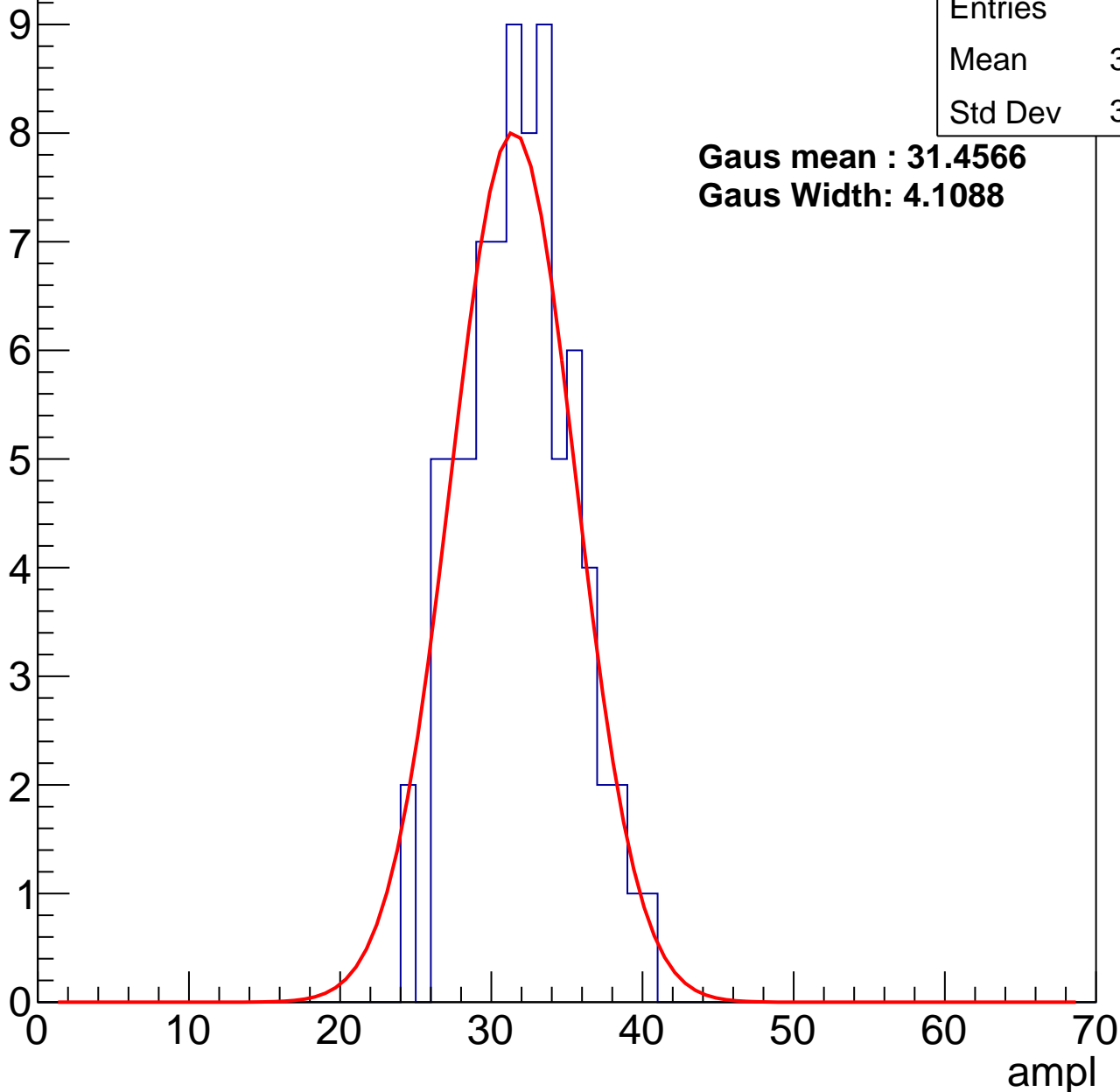
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	78
Mean	31.42
Std Dev	3.525

**Gaus mean : 31.4566**

**Gaus Width: 4.1088**



# B1L101S, U22-ch61, adc1

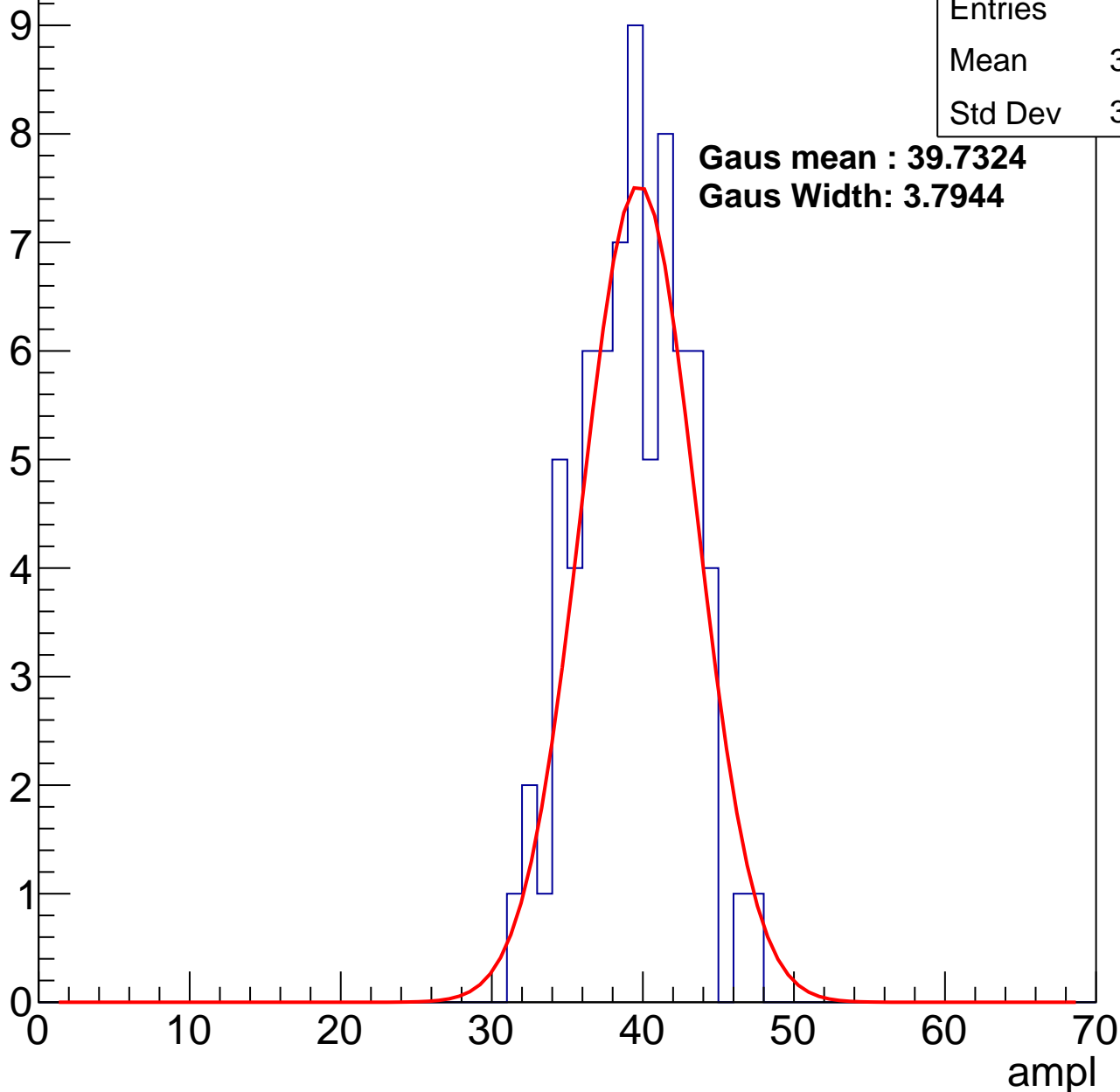
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	72
Mean	38.89
Std Dev	3.478

**Gaus mean : 39.7324**

**Gaus Width: 3.7944**



# B1L101S, U22-ch61, adc2

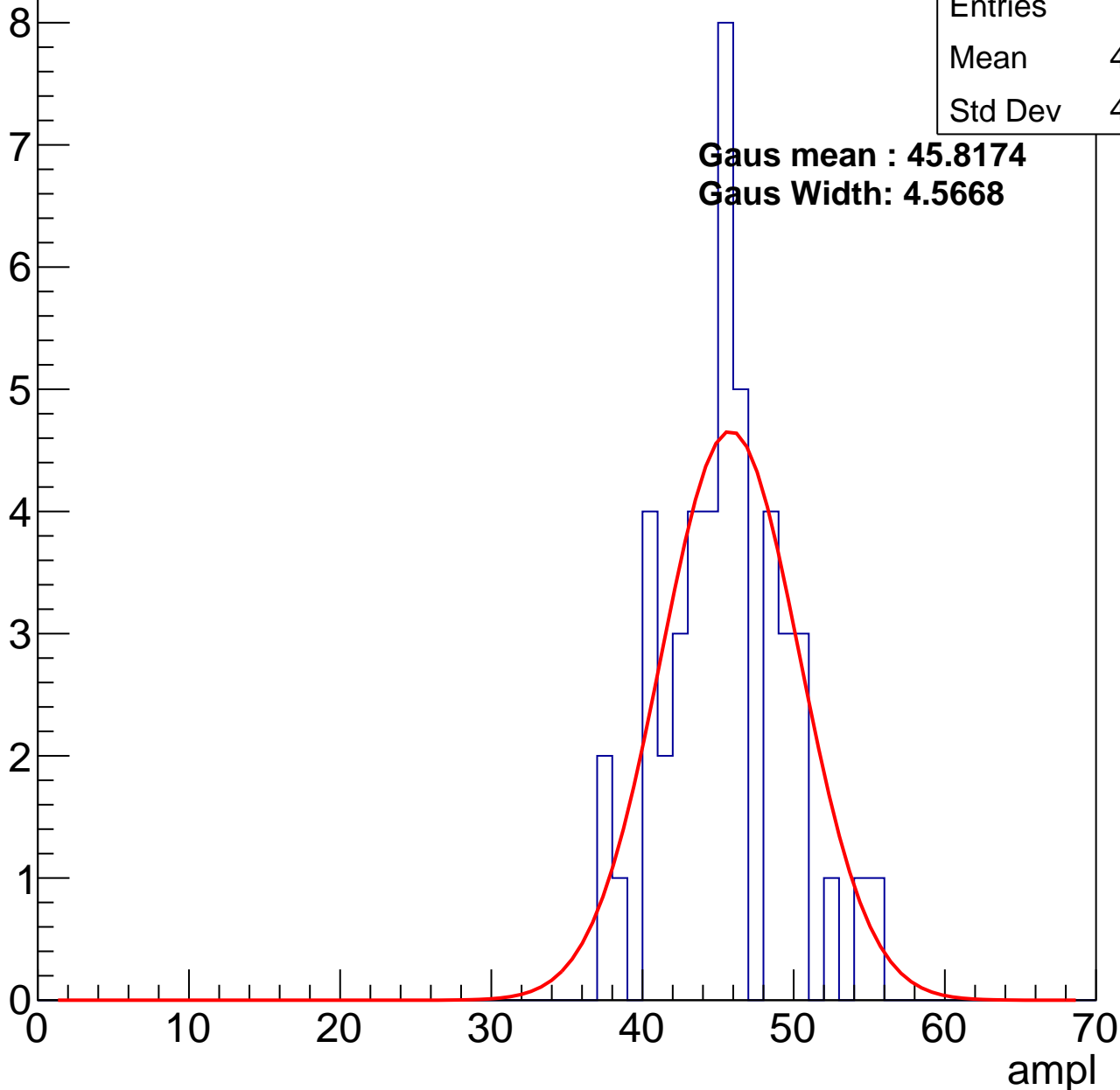
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	46
Mean	44.96
Std Dev	4.038

**Gaus mean : 45.8174**

**Gaus Width: 4.5668**



# B1L101S, U22-ch61, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	80
Mean	50.7
Std Dev	3.61

Entry

10

8

6

4

2

0

0

10

20

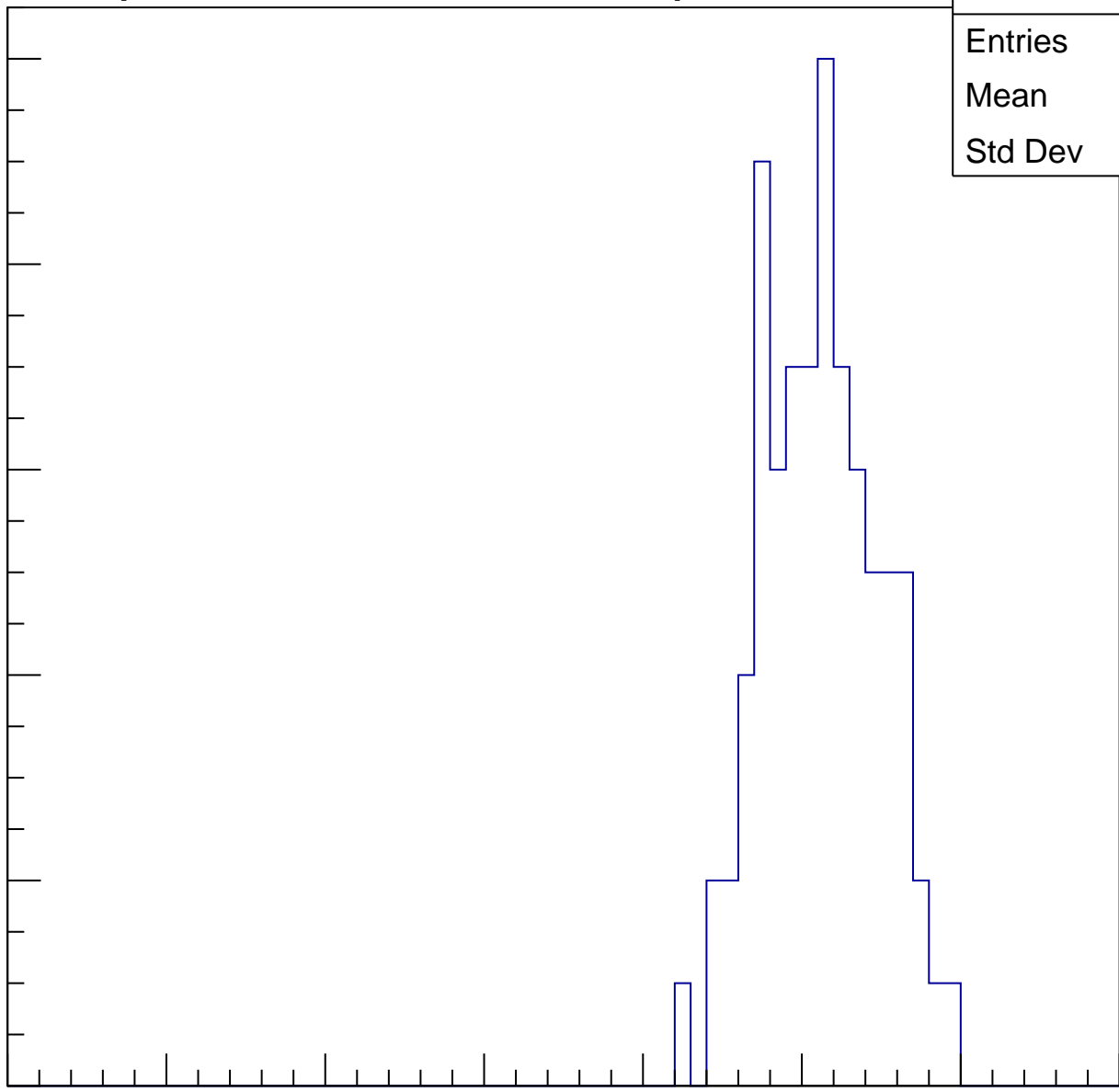
30

40

50

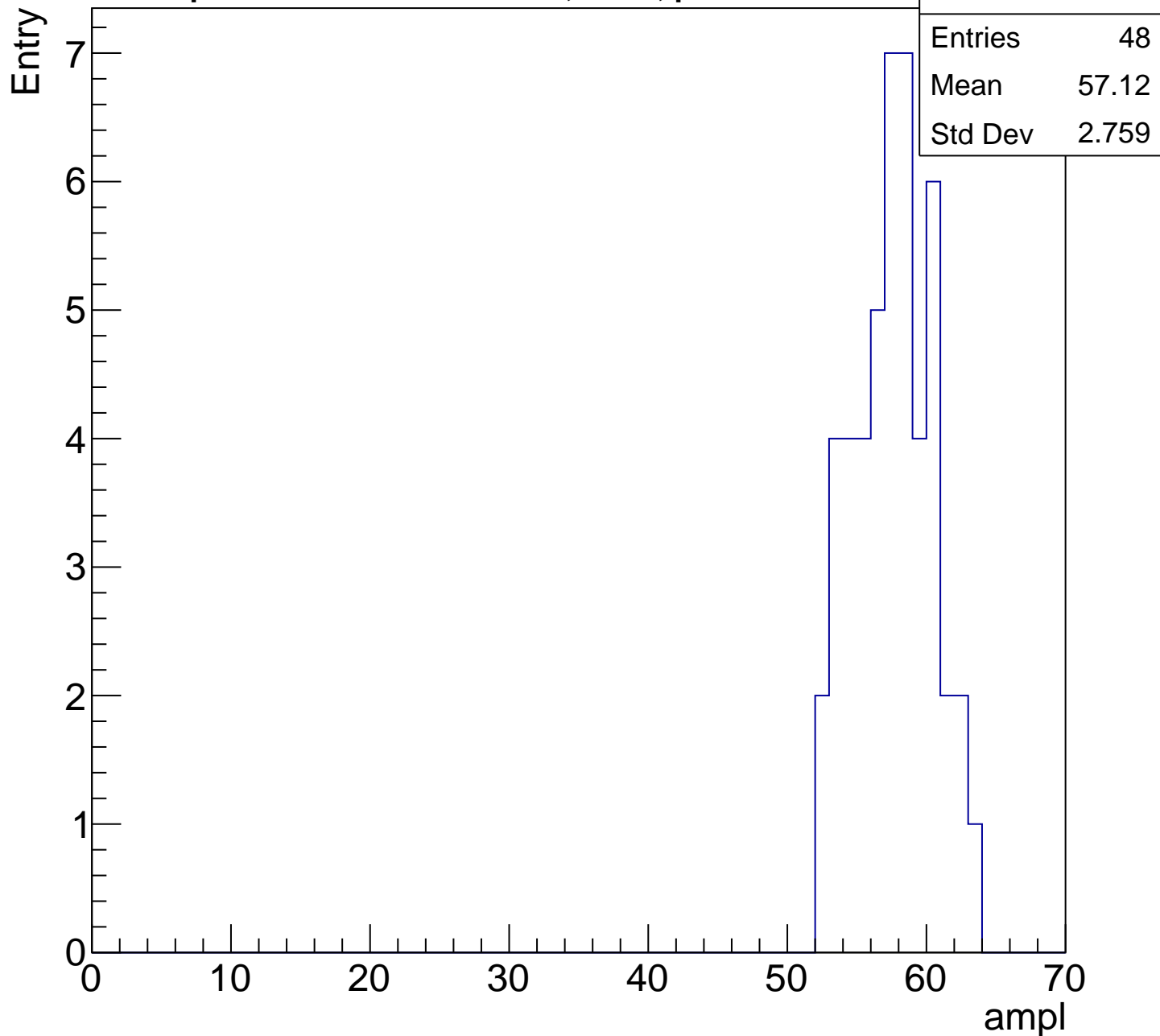
60

ampl



# B1L101S, U22-ch61, adc4

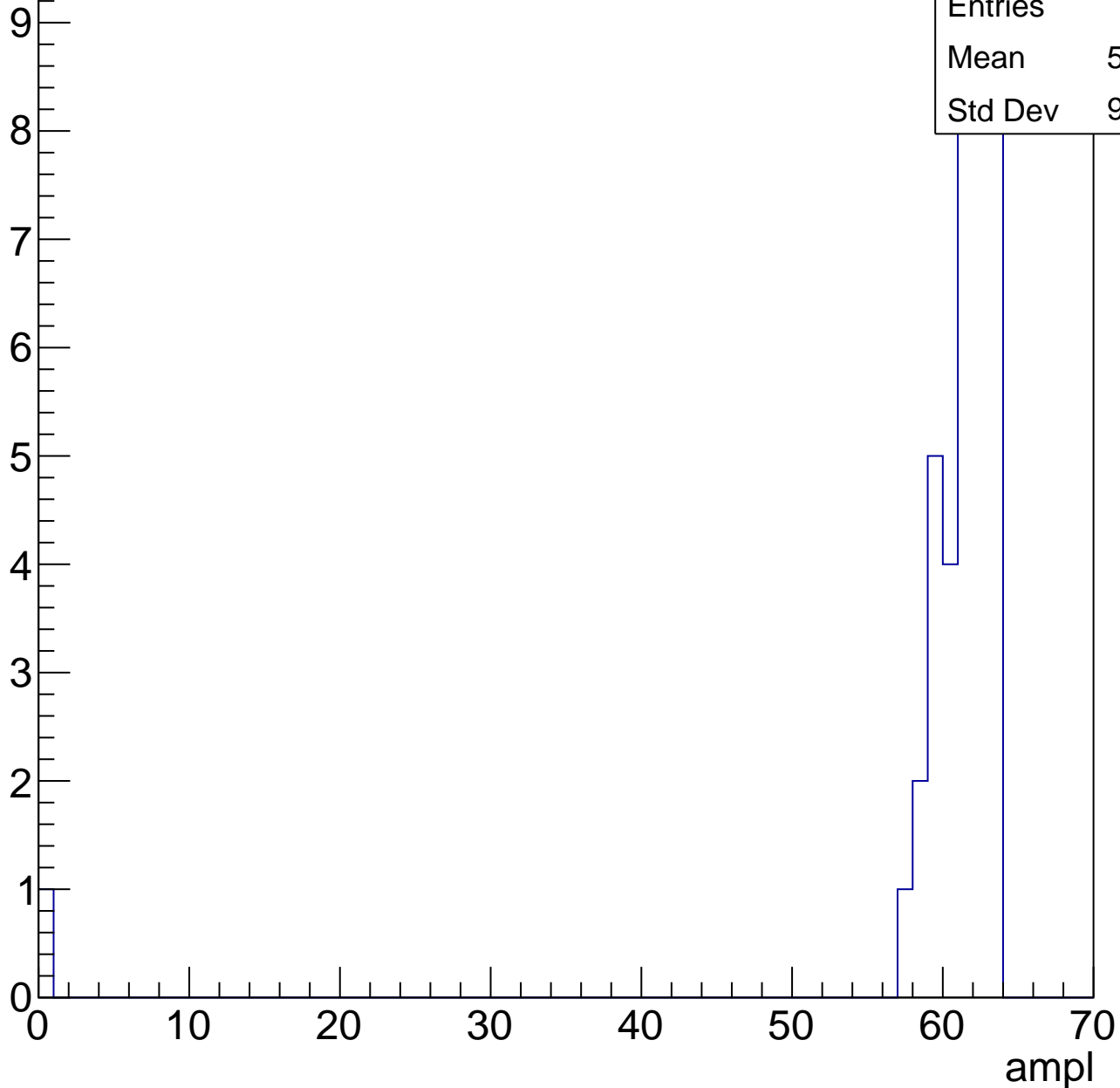
calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U22-ch61, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U22-ch61, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



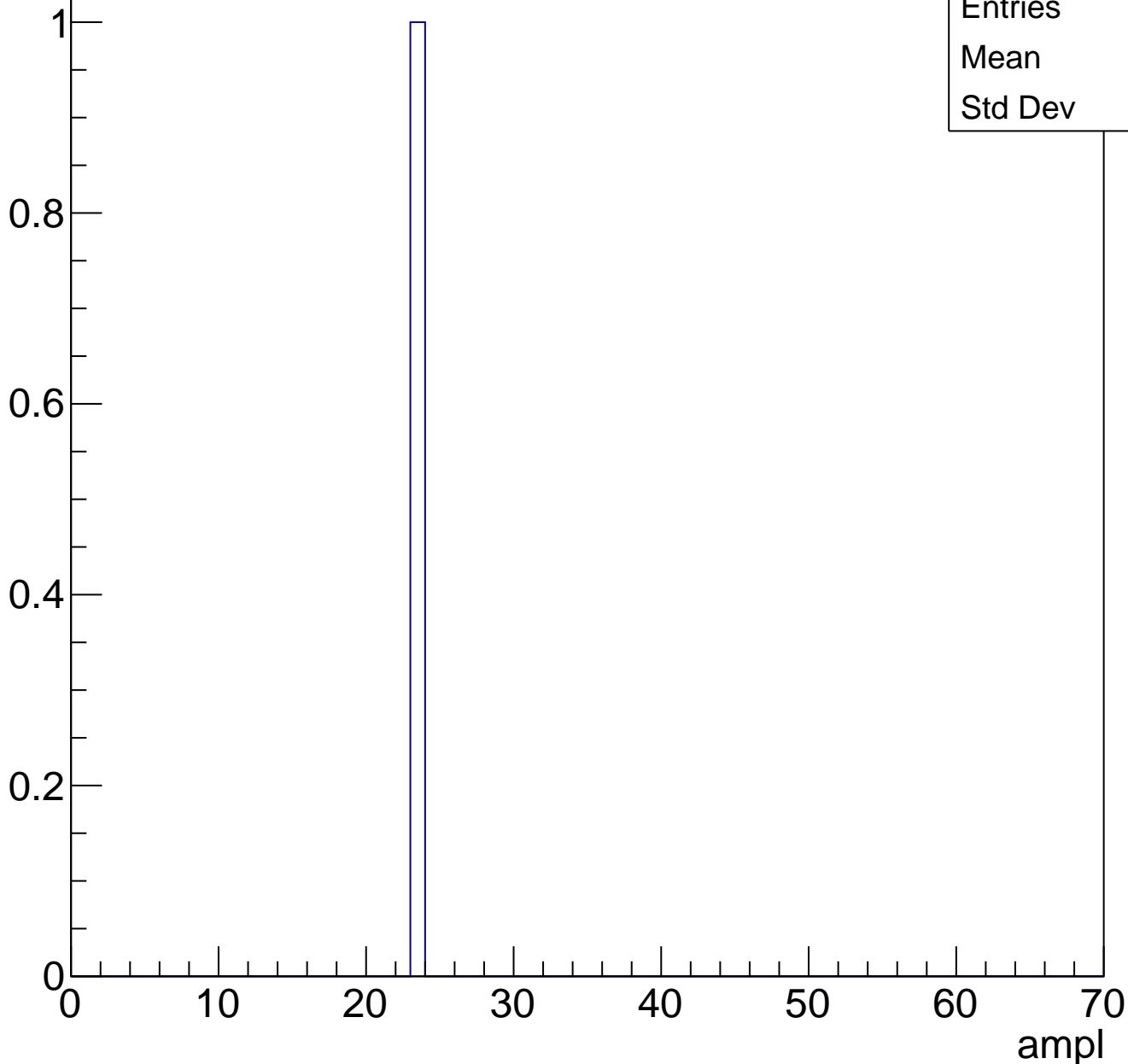
Entries	0
Mean	0
Std Dev	0



# B1L101S, U22-ch61, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U22-ch62, adc0

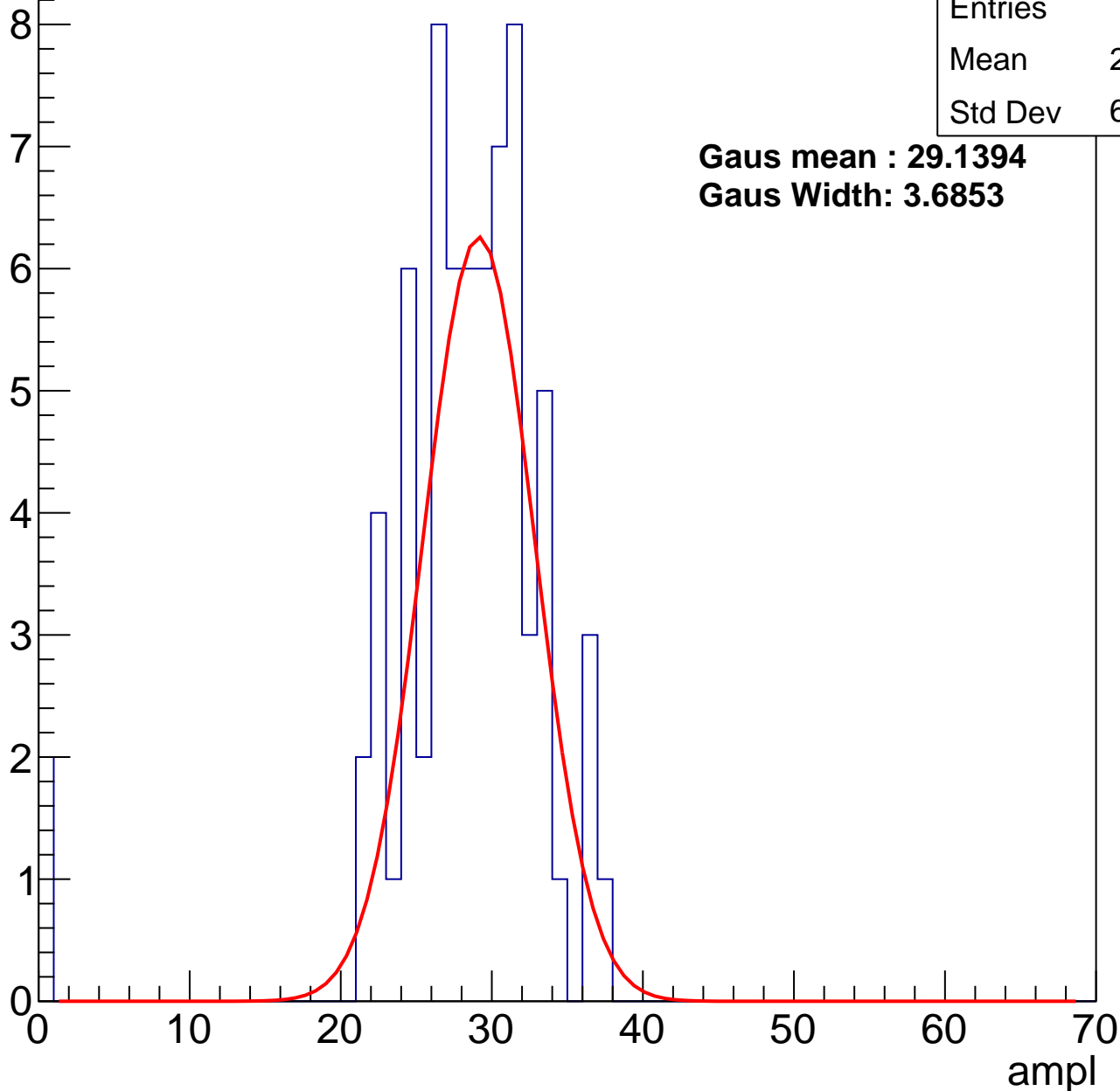
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	71
Mean	27.56
Std Dev	6.006

**Gaus mean : 29.1394**

**Gaus Width: 3.6853**



# B1L101S, U22-ch62, adc1

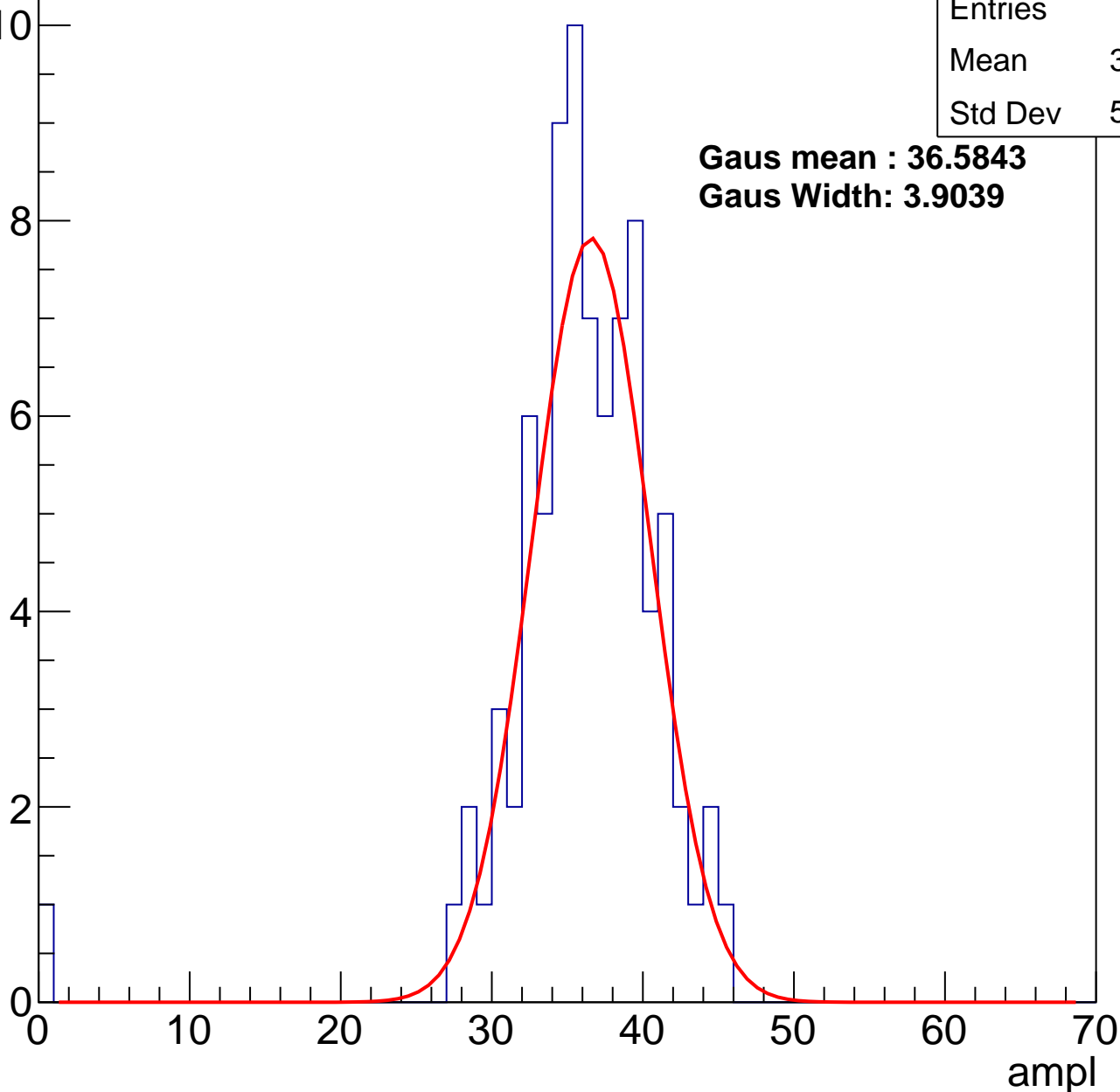
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	83
Mean	35.59
Std Dev	5.499

**Gaus mean : 36.5843**

**Gaus Width: 3.9039**



# B1L101S, U22-ch62, adc2

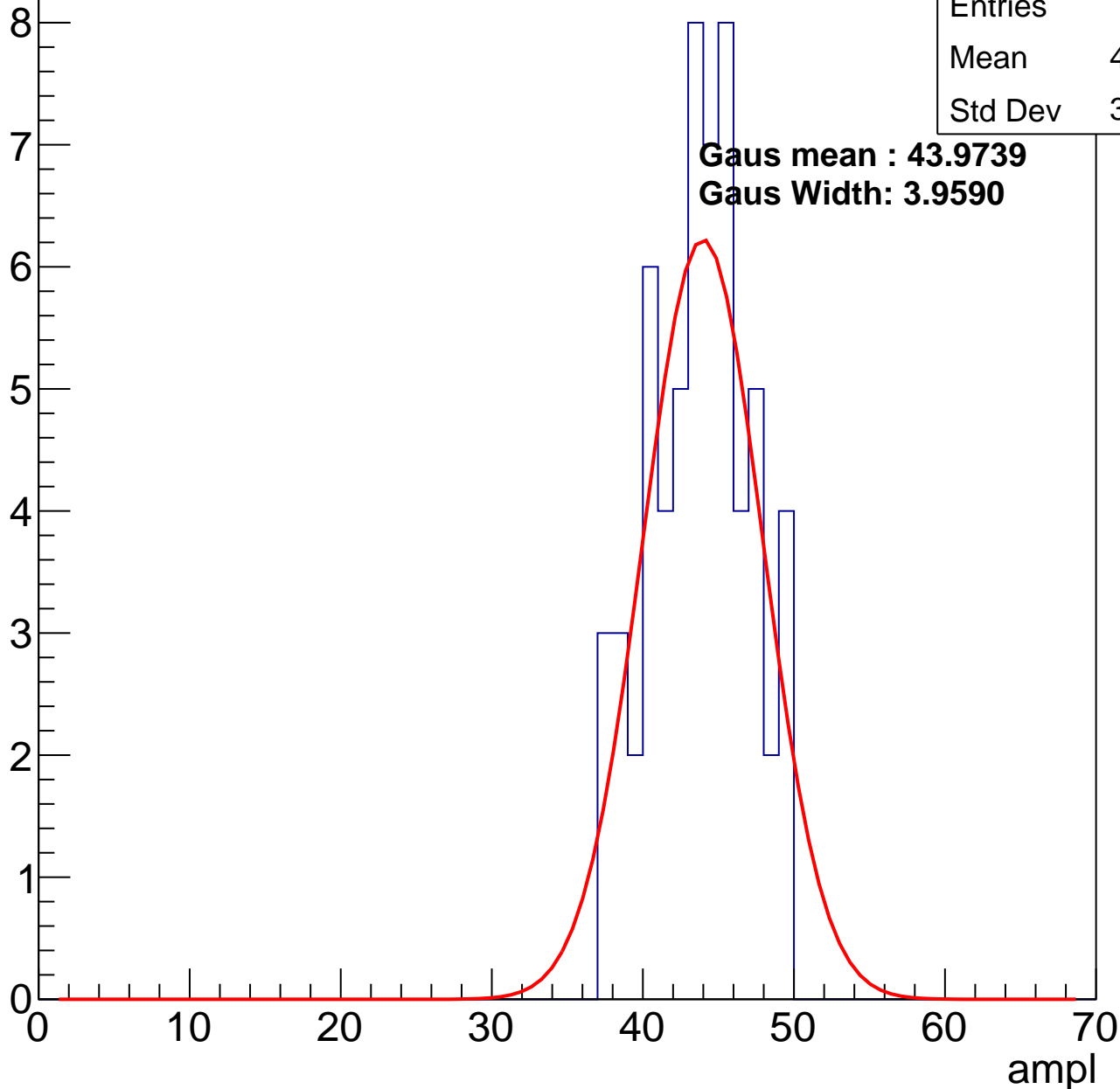
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	43.28
Std Dev	3.225

**Gaus mean : 43.9739**

**Gaus Width: 3.9590**

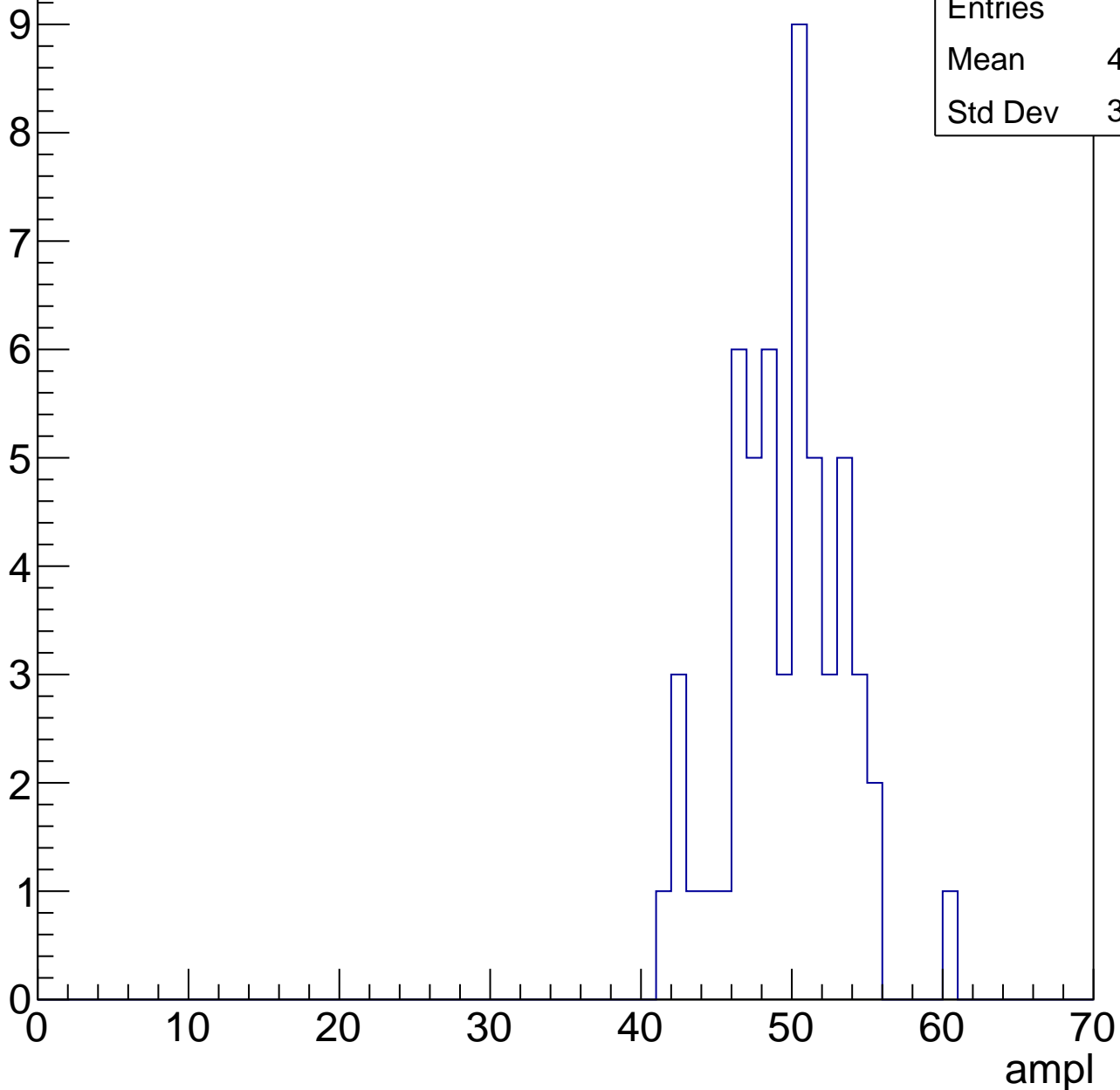


# B1L101S, U22-ch62, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

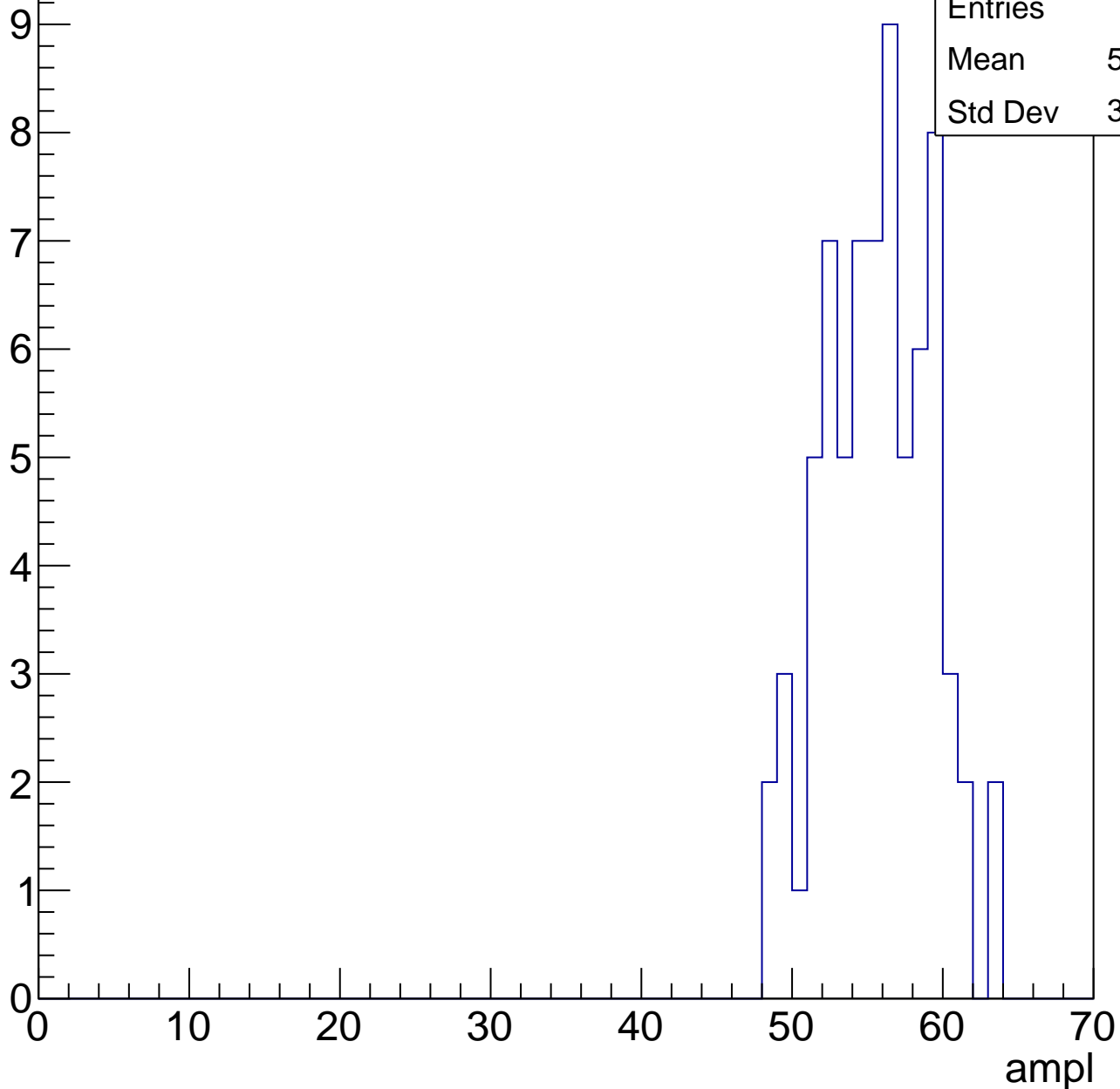
Entries	55
Mean	49.15
Std Dev	3.744



# B1L101S, U22-ch62, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



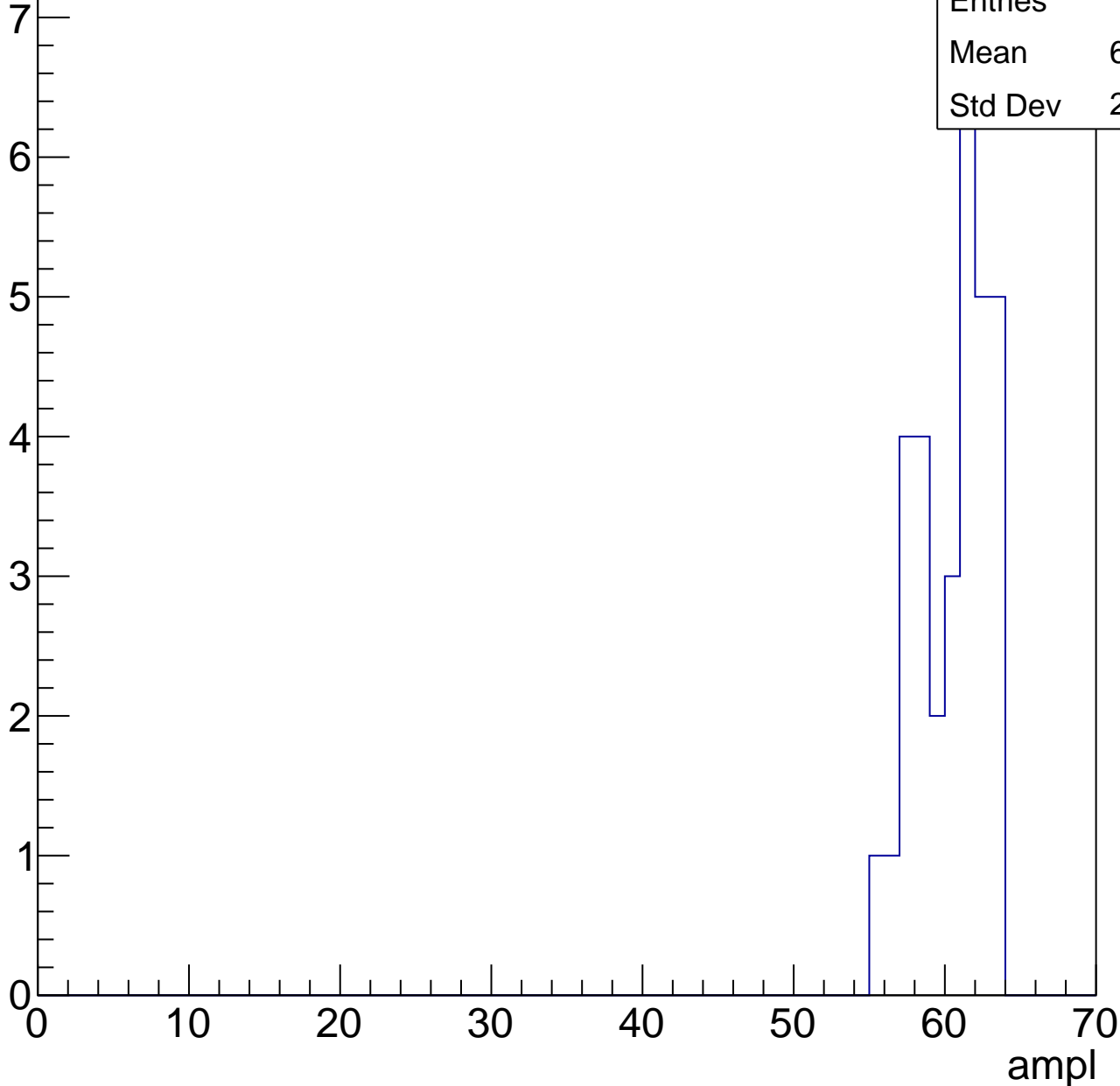
Entries	72
Mean	55.24
Std Dev	3.502

# B1L101S, U22-ch62, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	32
Mean	60.03
Std Dev	2.284

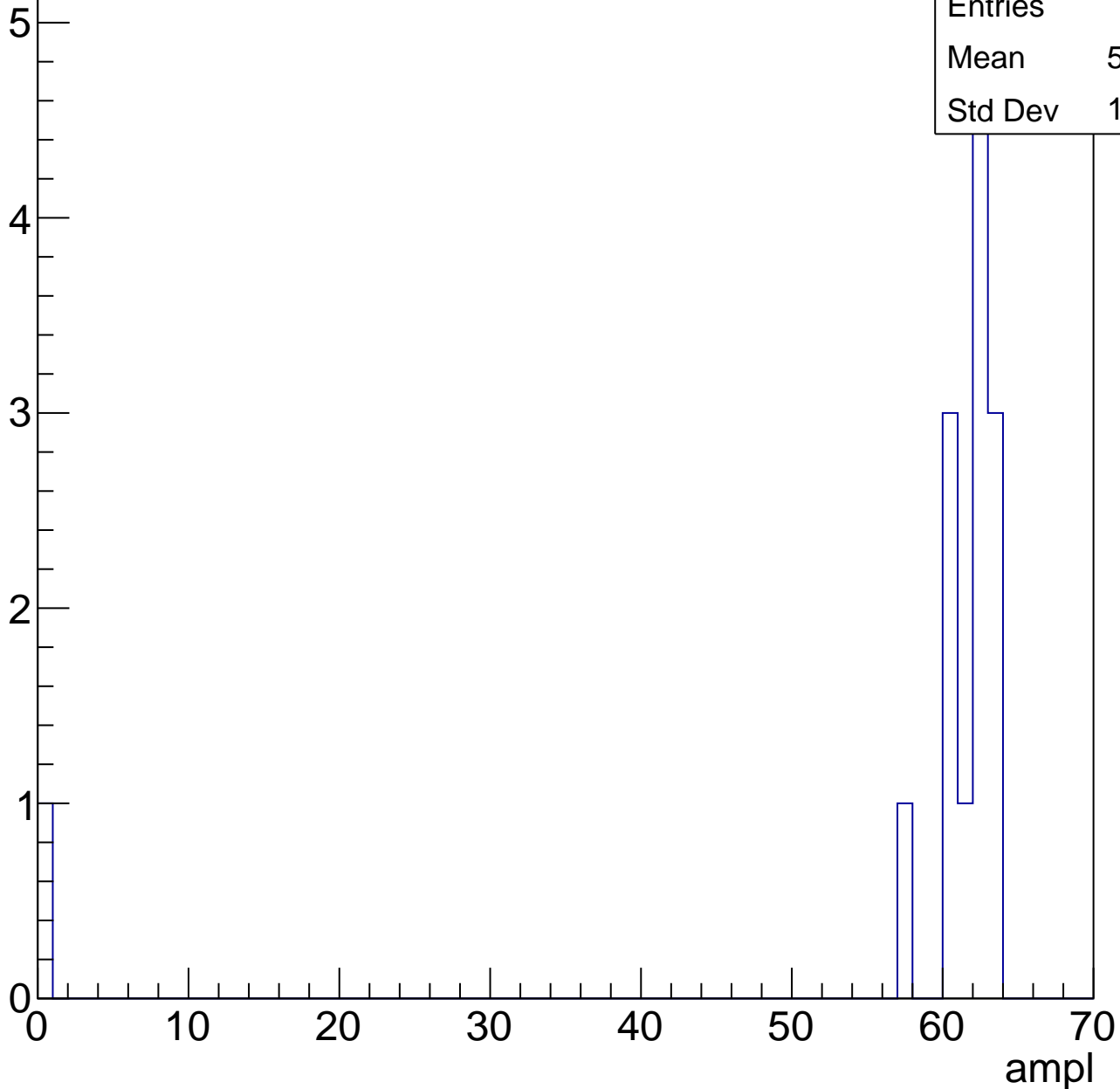


# B1L101S, U22-ch62, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	14
Mean	56.93
Std Dev	15.87





# B1L101S, U22-ch62, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L101S, U22-ch63, adc0

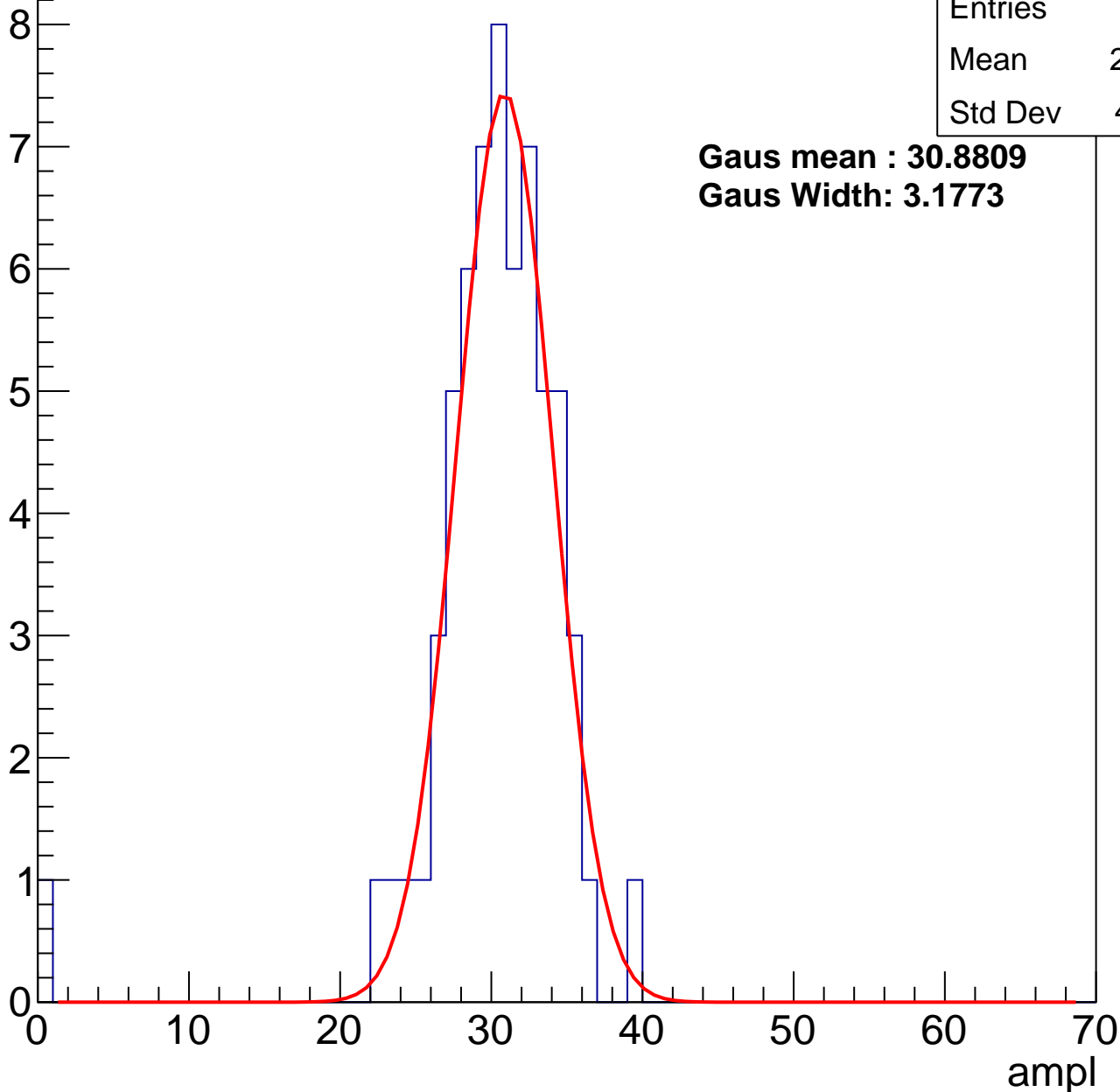
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	29.73
Std Dev	4.991

**Gaus mean : 30.8809**

**Gaus Width: 3.1773**

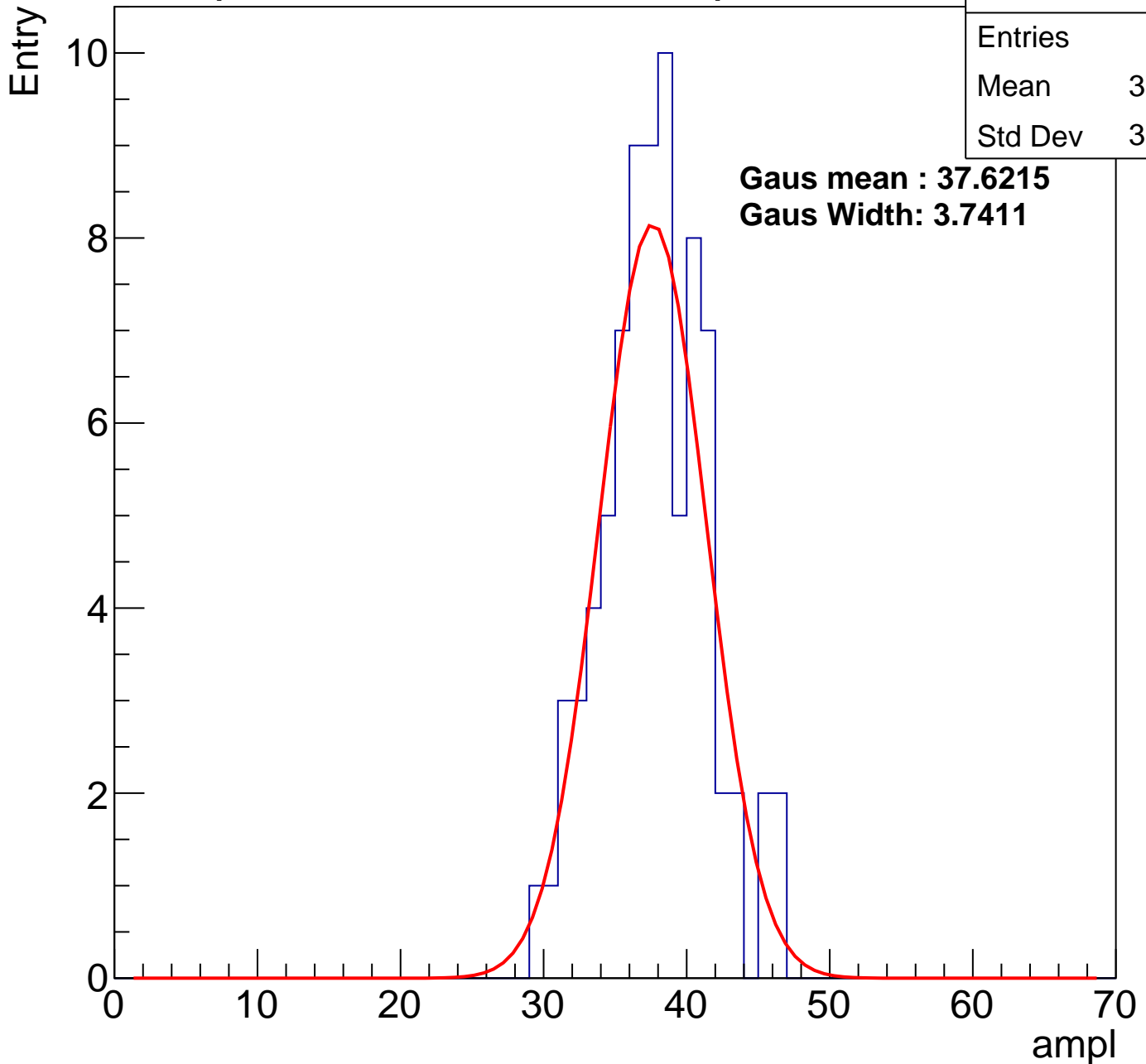


# B1L101S, U22-ch63, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	80
Mean	37.33
Std Dev	3.639

**Gaus mean : 37.6215**  
**Gaus Width: 3.7411**



# B1L101S, U22-ch63, adc2

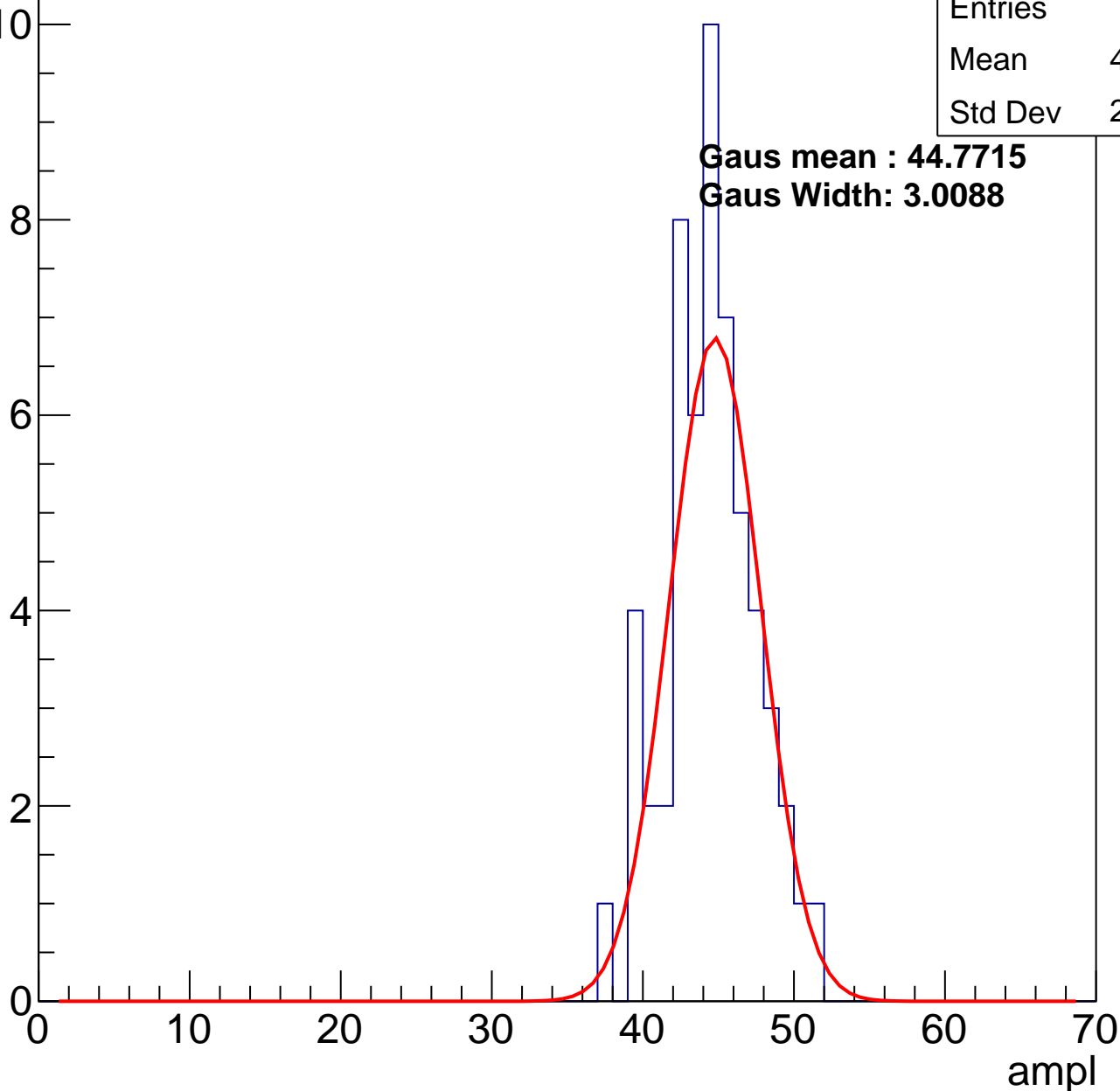
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	56
Mean	44.02
Std Dev	2.937

**Gaus mean : 44.7715**

**Gaus Width: 3.0088**

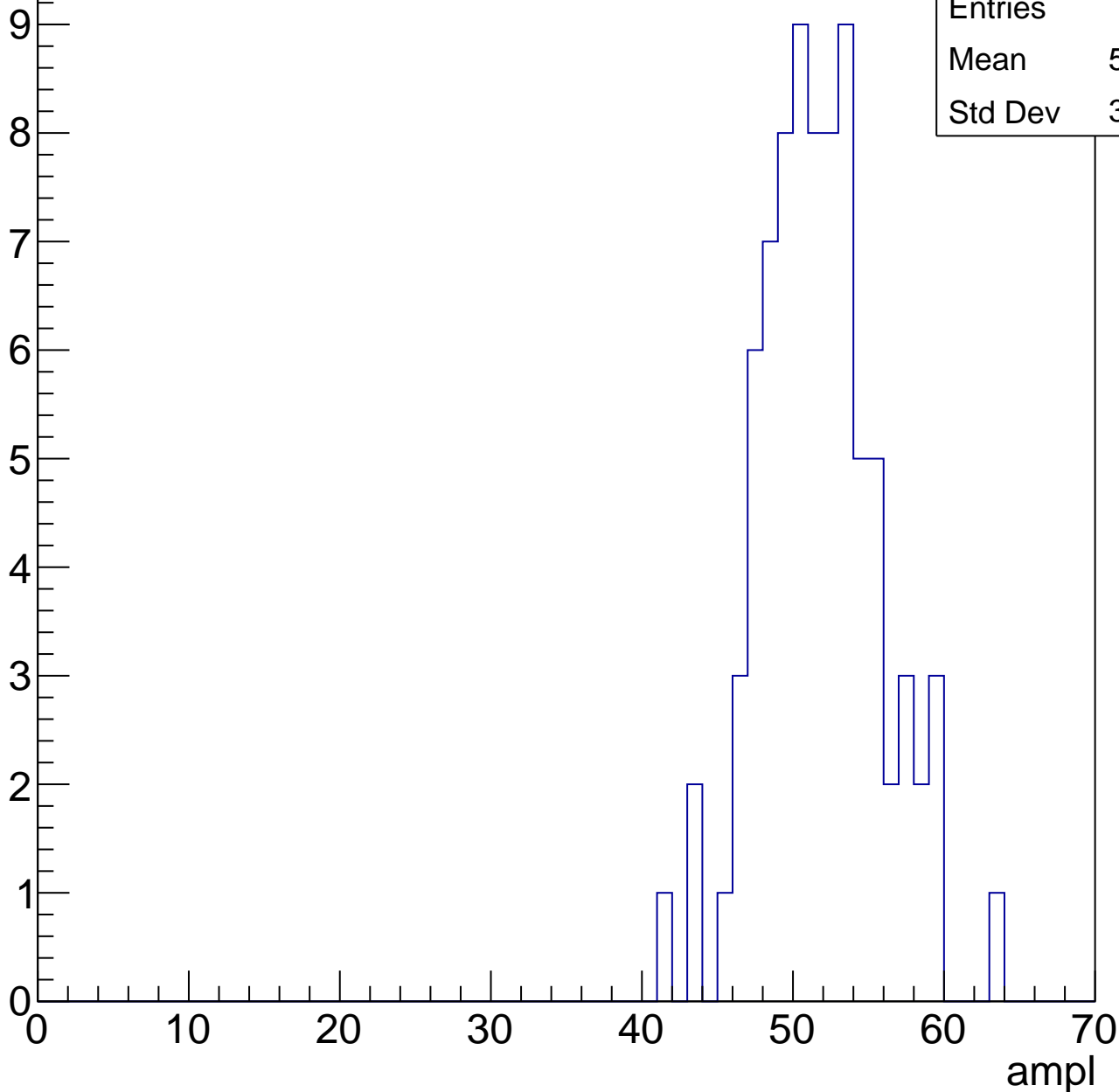


# B1L101S, U22-ch63, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	83
Mean	51.27
Std Dev	3.949

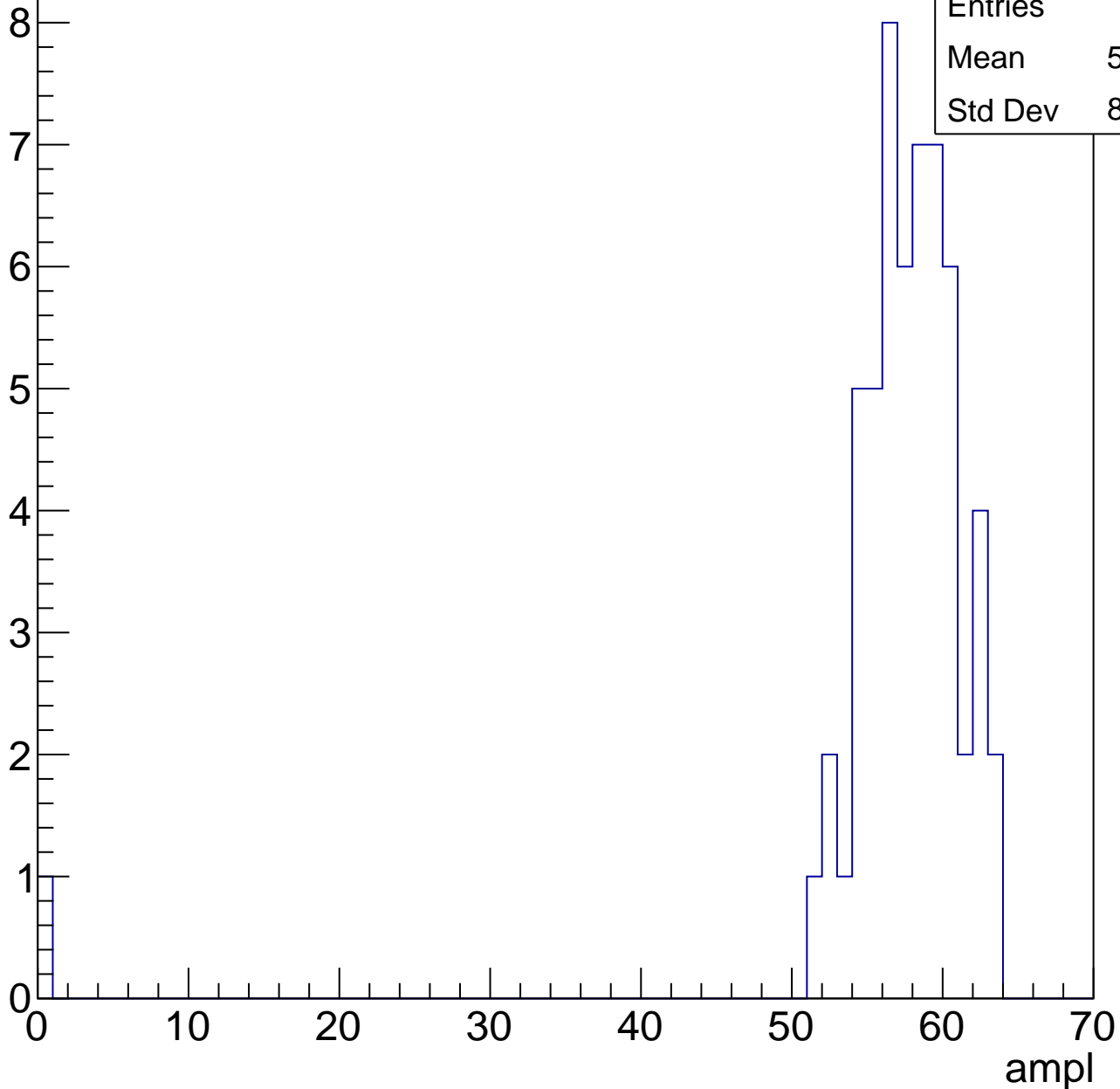


# B1L101S, U22-ch63, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	57
Mean	56.46
Std Dev	8.057

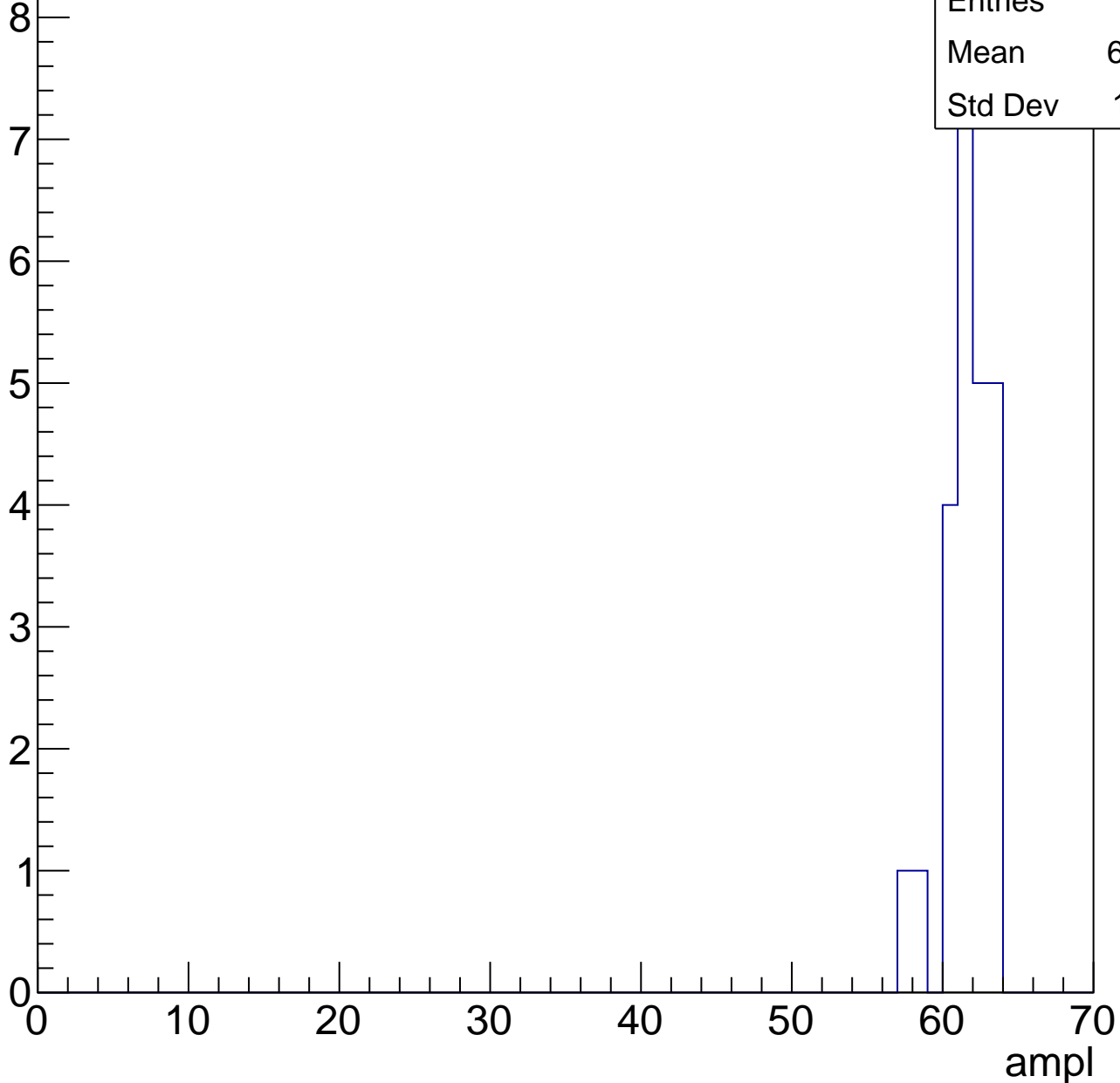


# B1L101S, U22-ch63, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	24
Mean	61.17
Std Dev	1.491



# B1L101S, U22-ch63, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	3
Mean	62.67
Std Dev	0.4714

ampl

0 10 20 30 40 50 60 70



# B1L101S, U22-ch63, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U22-ch64, adc0

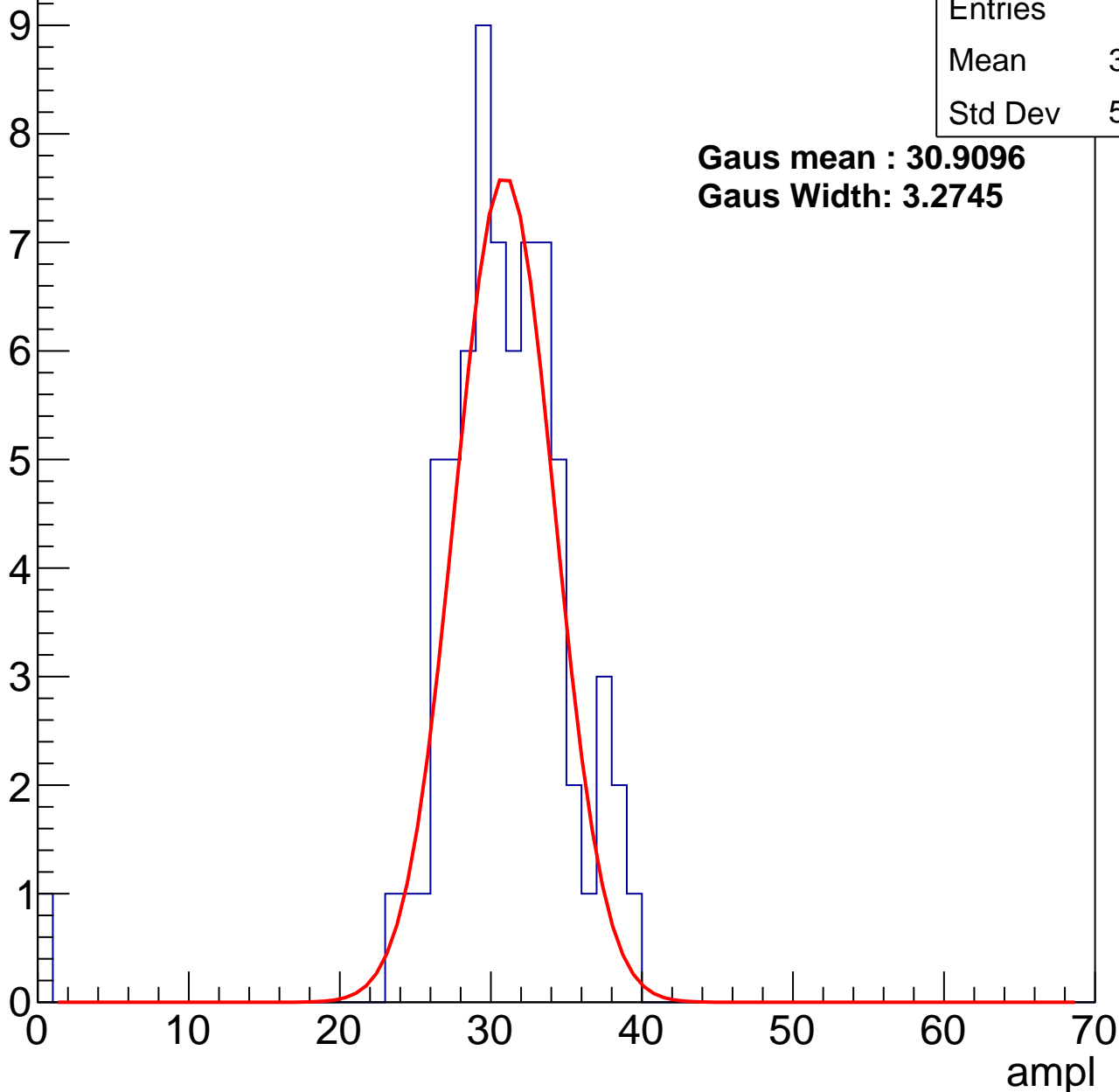
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	30.27
Std Dev	5.045

**Gaus mean : 30.9096**

**Gaus Width: 3.2745**



# B1L101S, U22-ch64, adc1

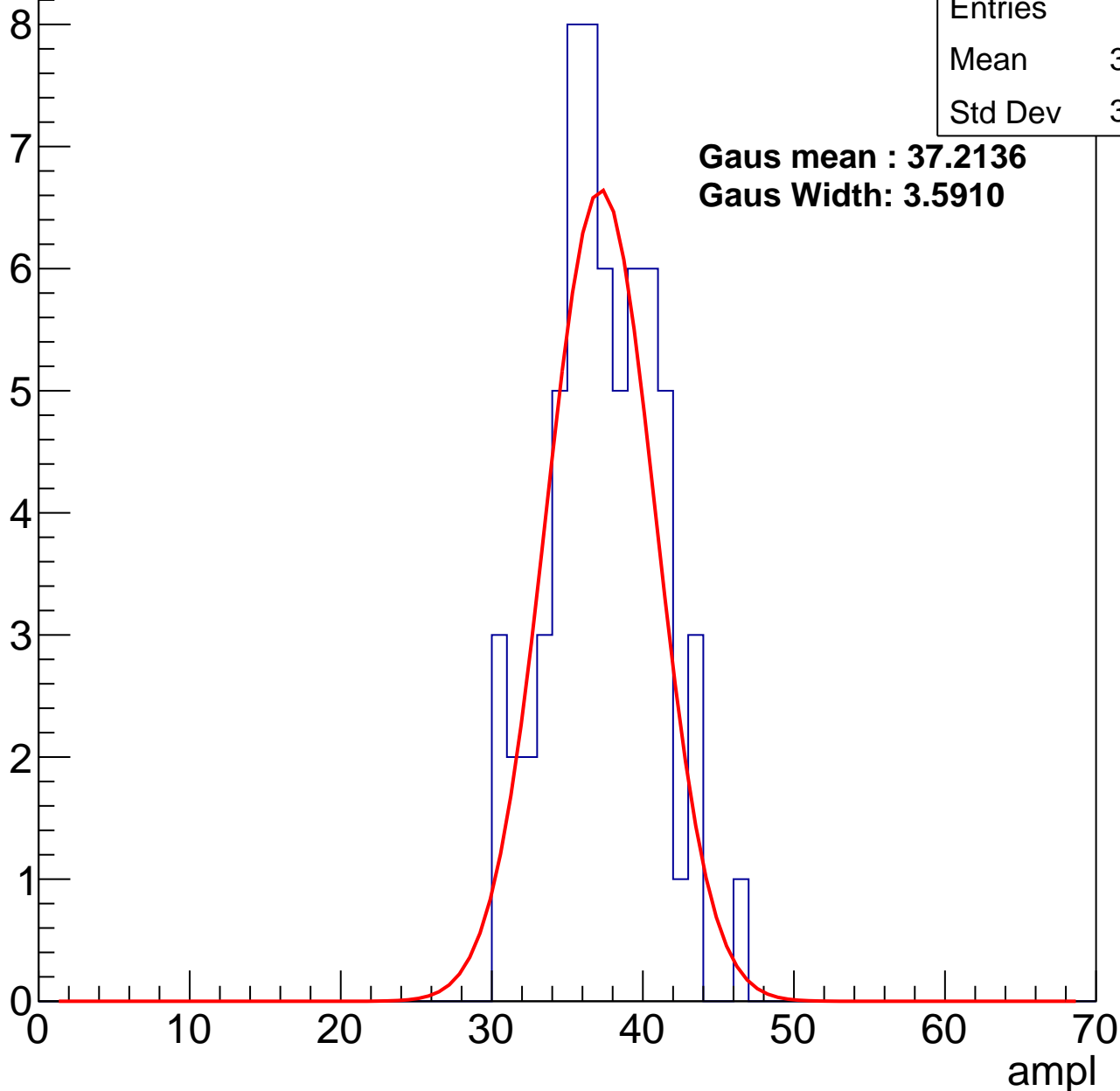
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	36.89
Std Dev	3.487

**Gaus mean : 37.2136**

**Gaus Width: 3.5910**



# B1L101S, U22-ch64, adc2

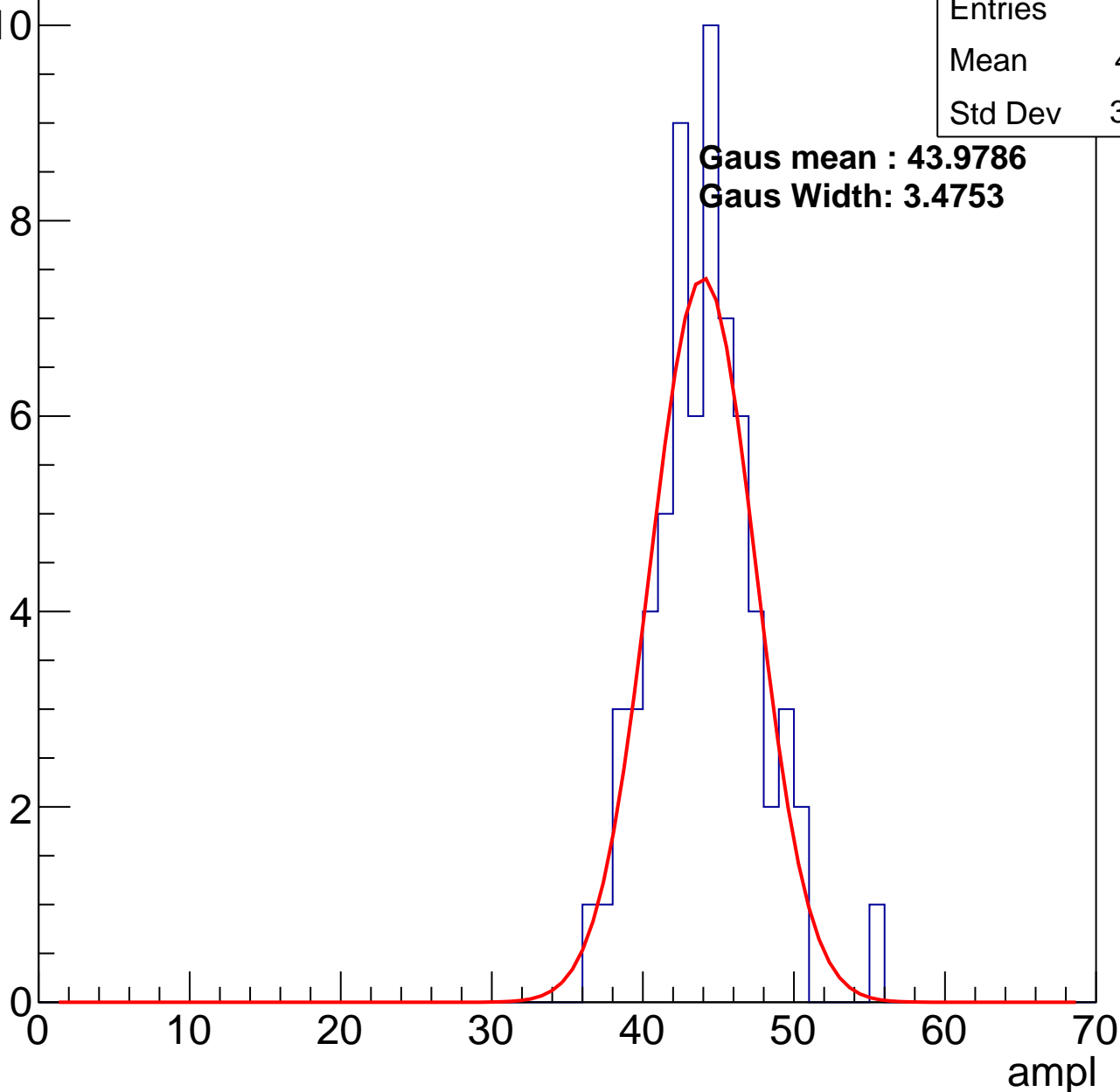
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	67
Mean	43.61
Std Dev	3.464

**Gaus mean : 43.9786**

**Gaus Width: 3.4753**



# B1L101S, U22-ch64, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	87
Mean	51.34
Std Dev	3.434

Entry

10

8

6

4

2

0

0

10

20

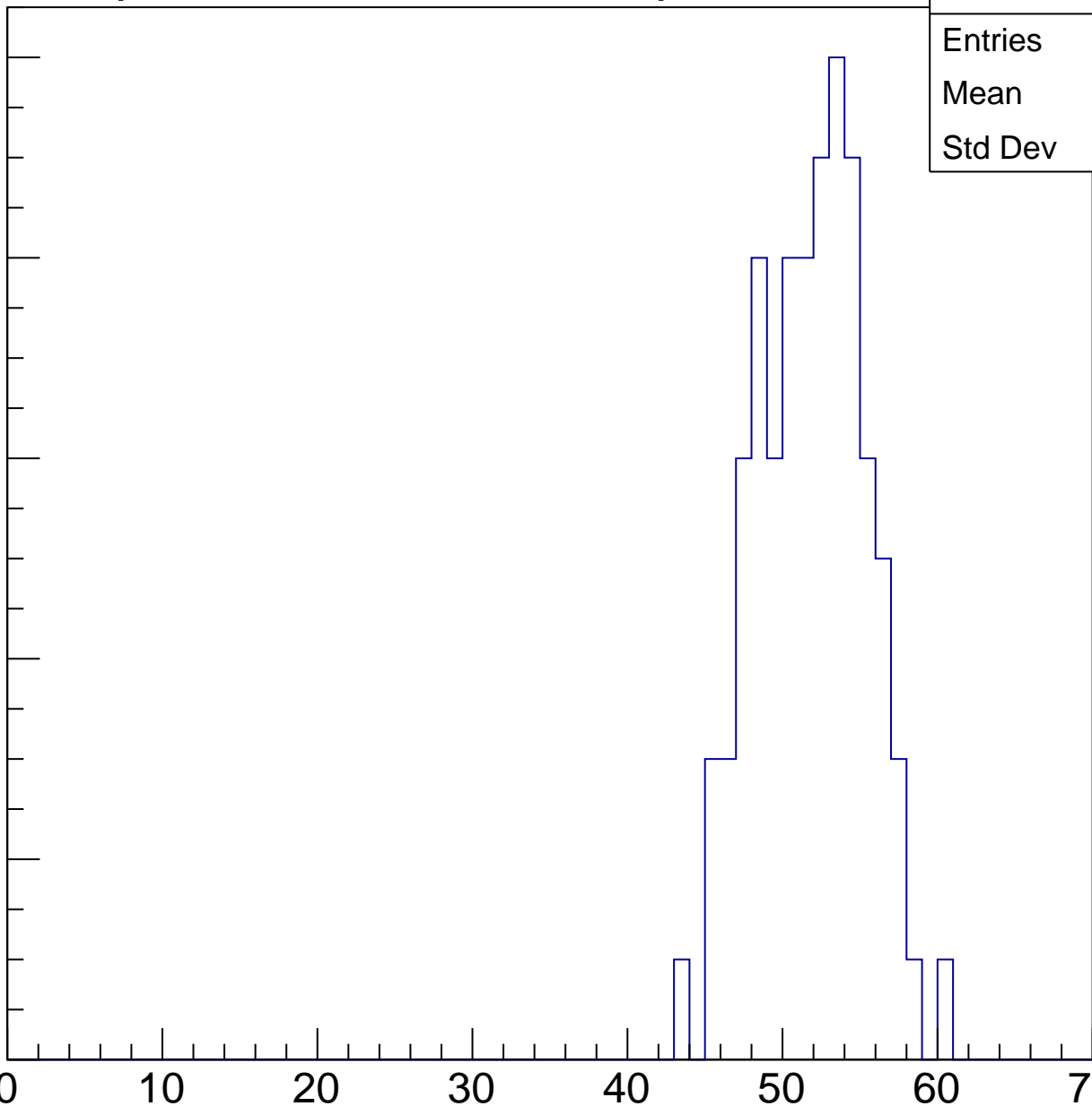
30

40

50

60

ampl

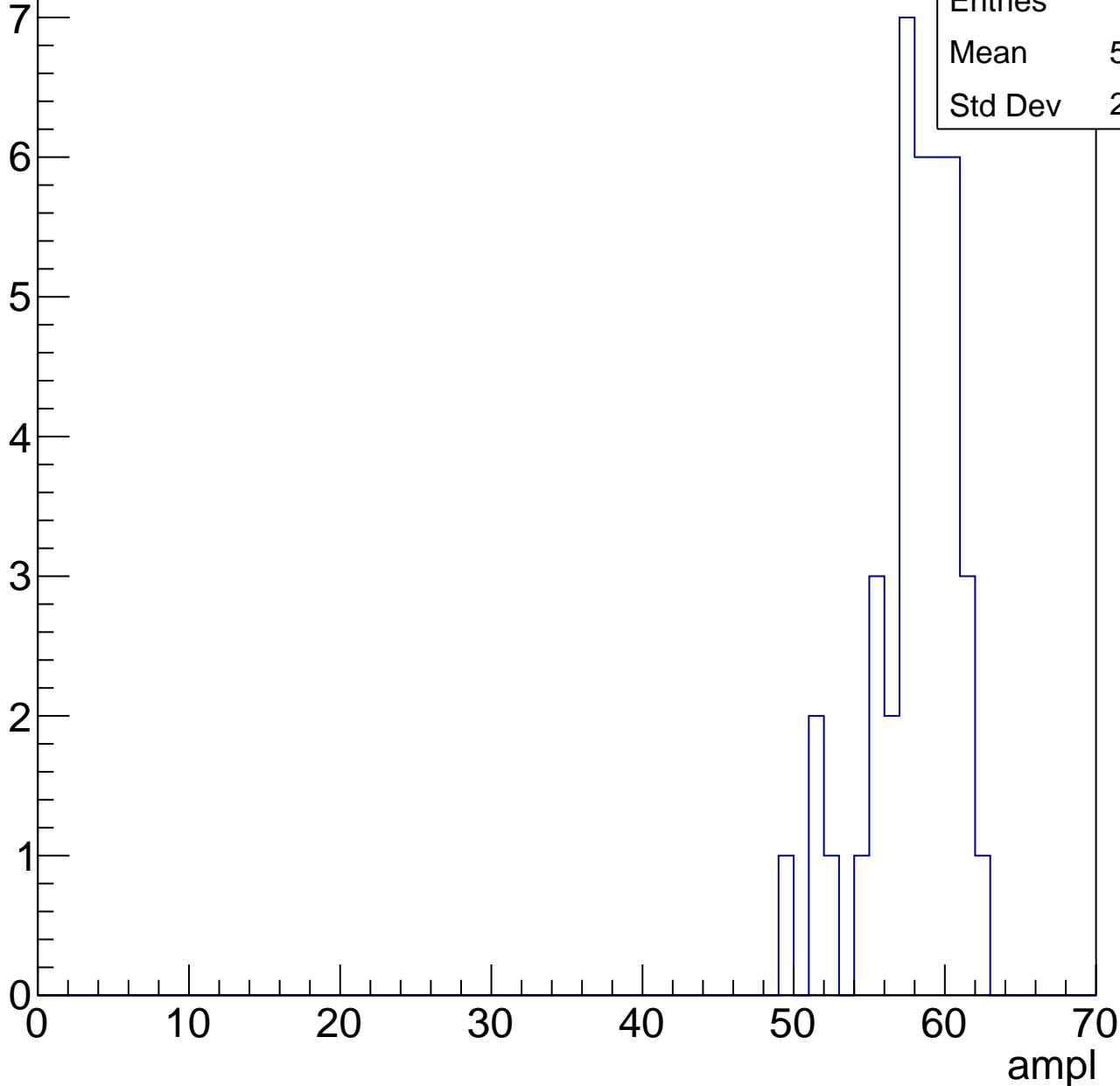


# B1L101S, U22-ch64, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	39
Mean	57.44
Std Dev	2.925



# B1L101S, U22-ch64, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	39
Mean	59.28
Std Dev	9.84

Entry

10

8

6

4

2

0

0

10

20

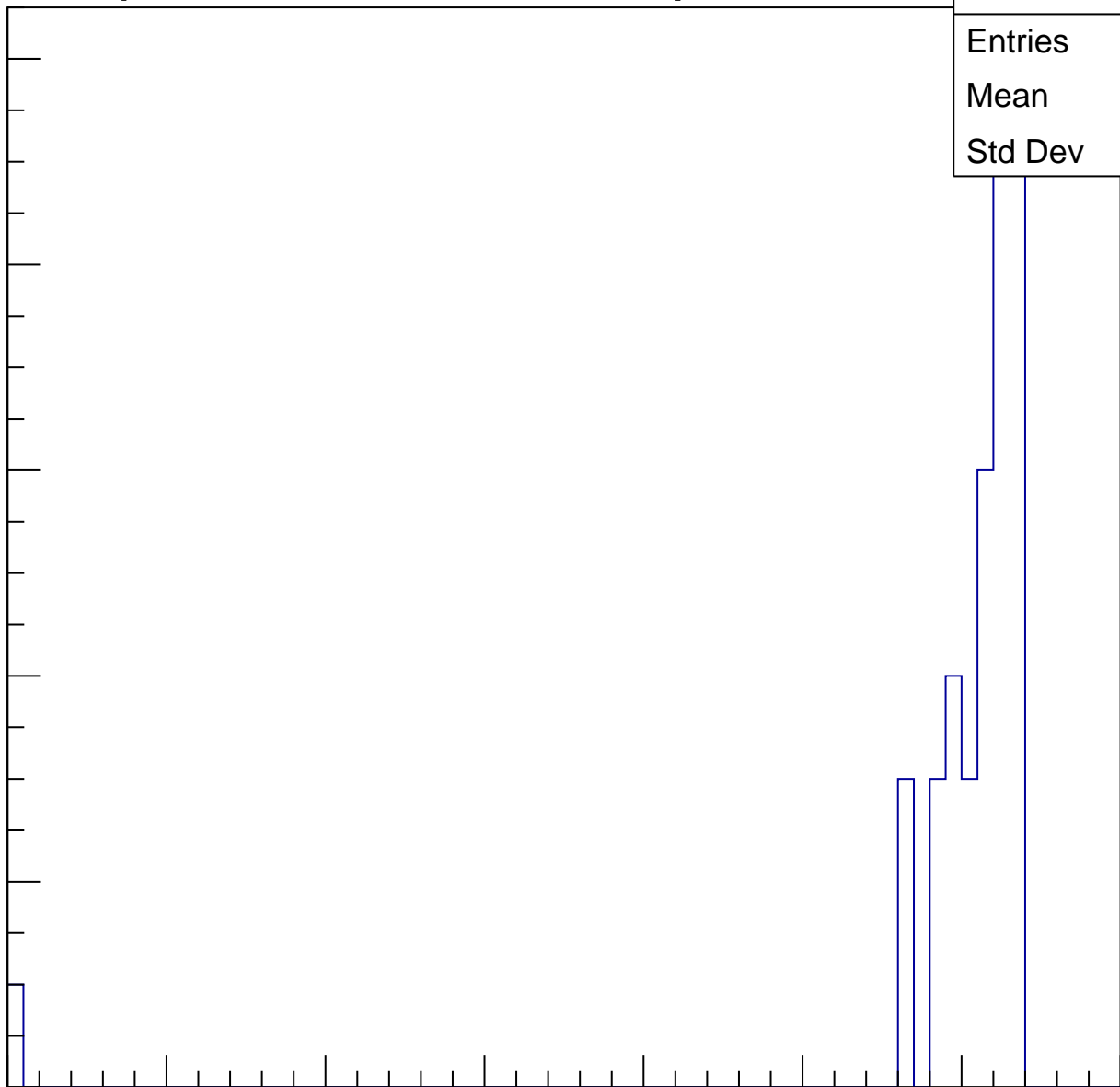
30

40

50

60

ampl



# B1L101S, U22-ch64, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U22-ch64, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	3
Mean	7.333
Std Dev	10.37

# B1L101S, U22-ch65, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	71
Mean	32.03
Std Dev	3.319

**Gaus mean : 32.1406**

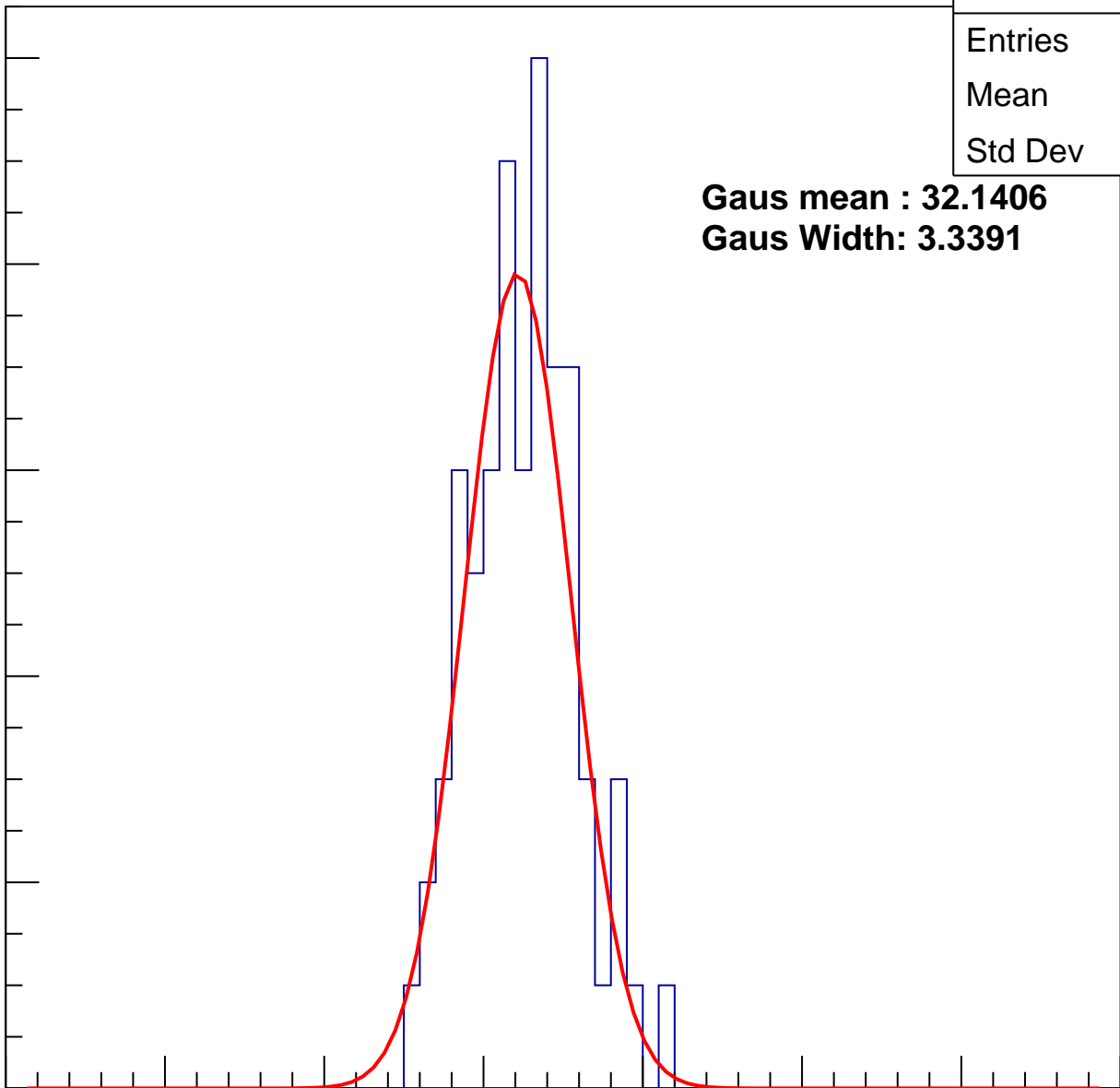
**Gaus Width: 3.3391**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U22-ch65, adc1

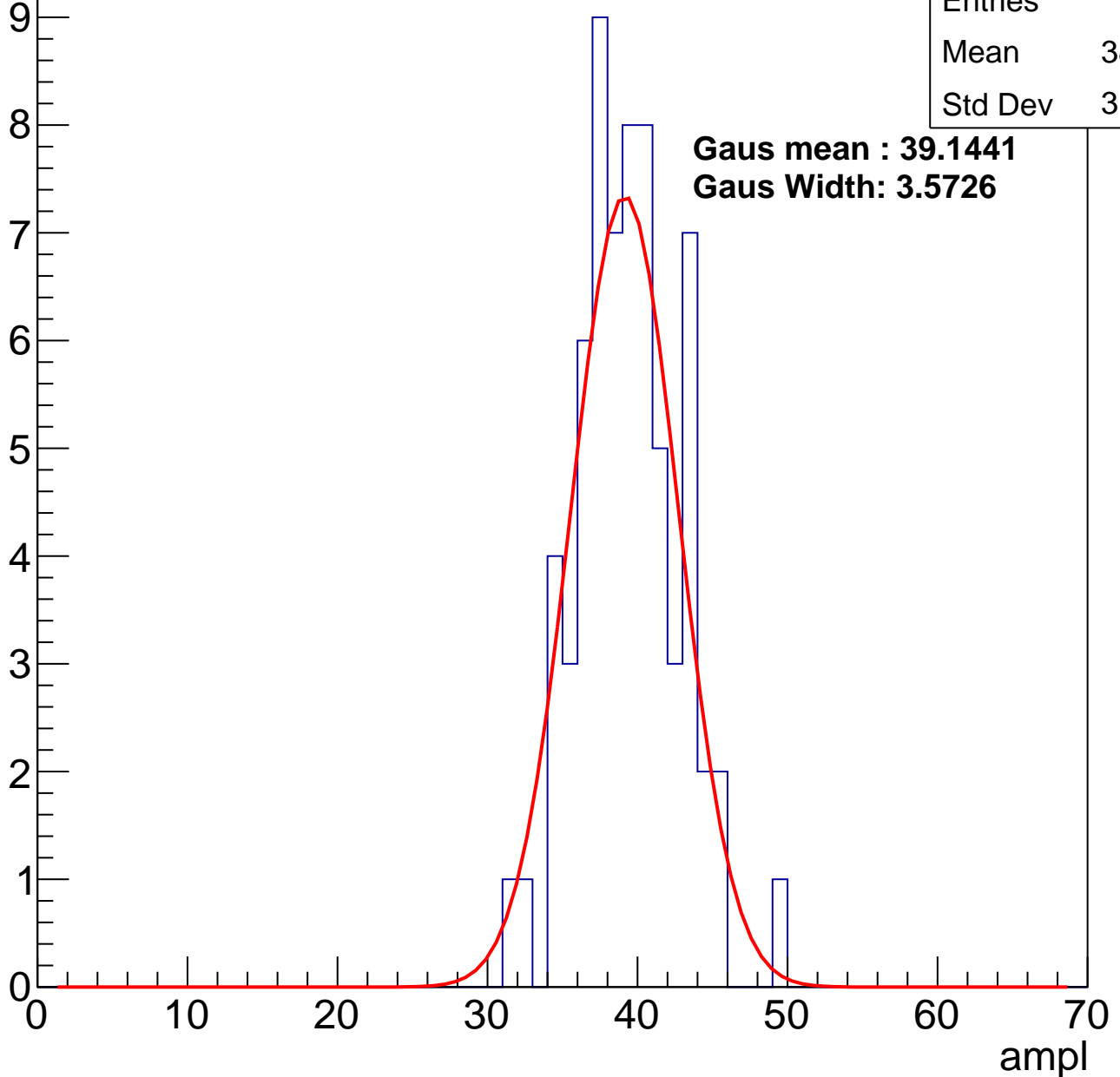
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	67
Mean	38.96
Std Dev	3.339

**Gaus mean : 39.1441**

**Gaus Width: 3.5726**



# B1L101S, U22-ch65, adc2

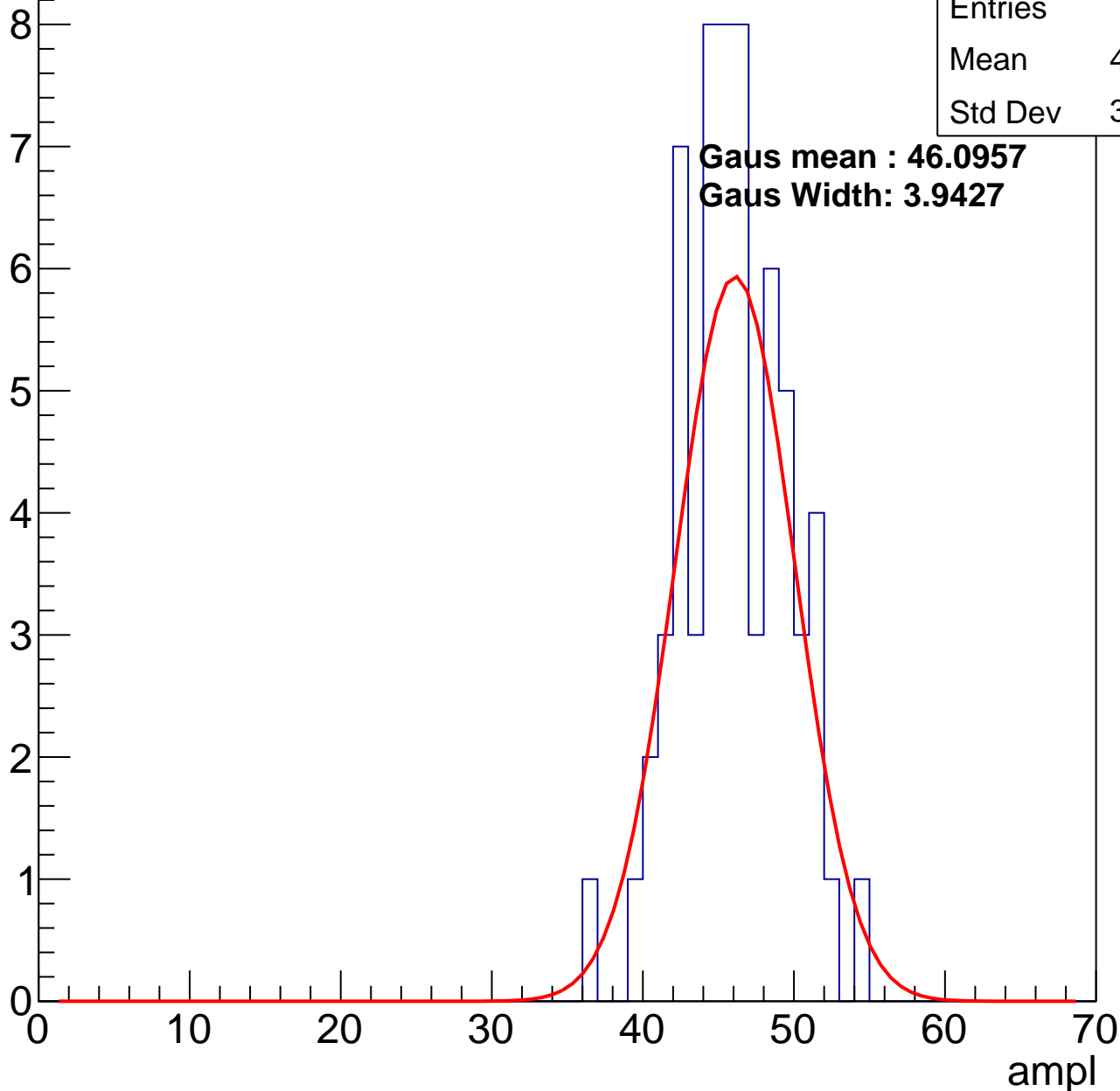
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	45.55
Std Dev	3.495

**Gaus mean : 46.0957**

**Gaus Width: 3.9427**

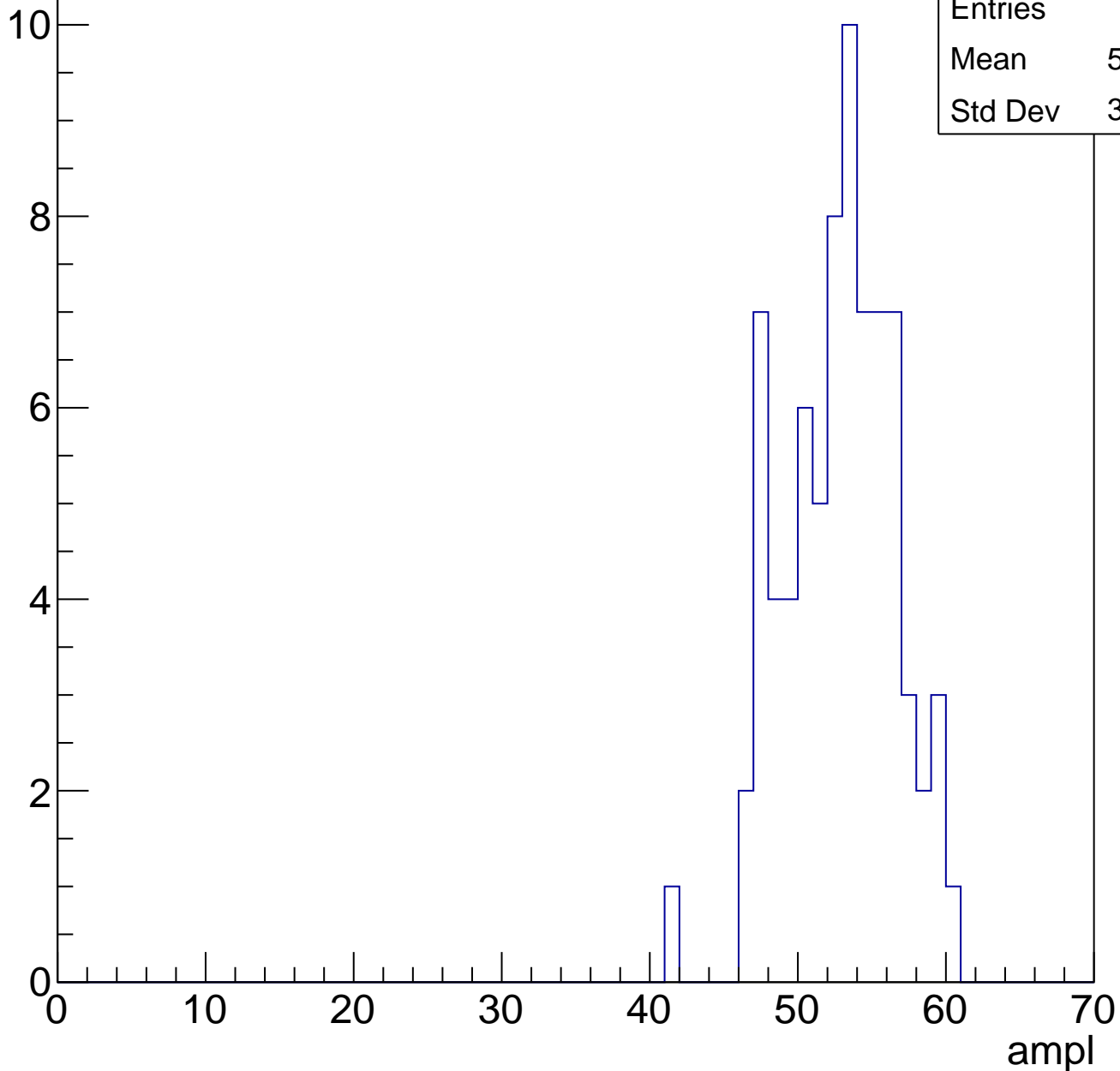


# B1L101S, U22-ch65, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

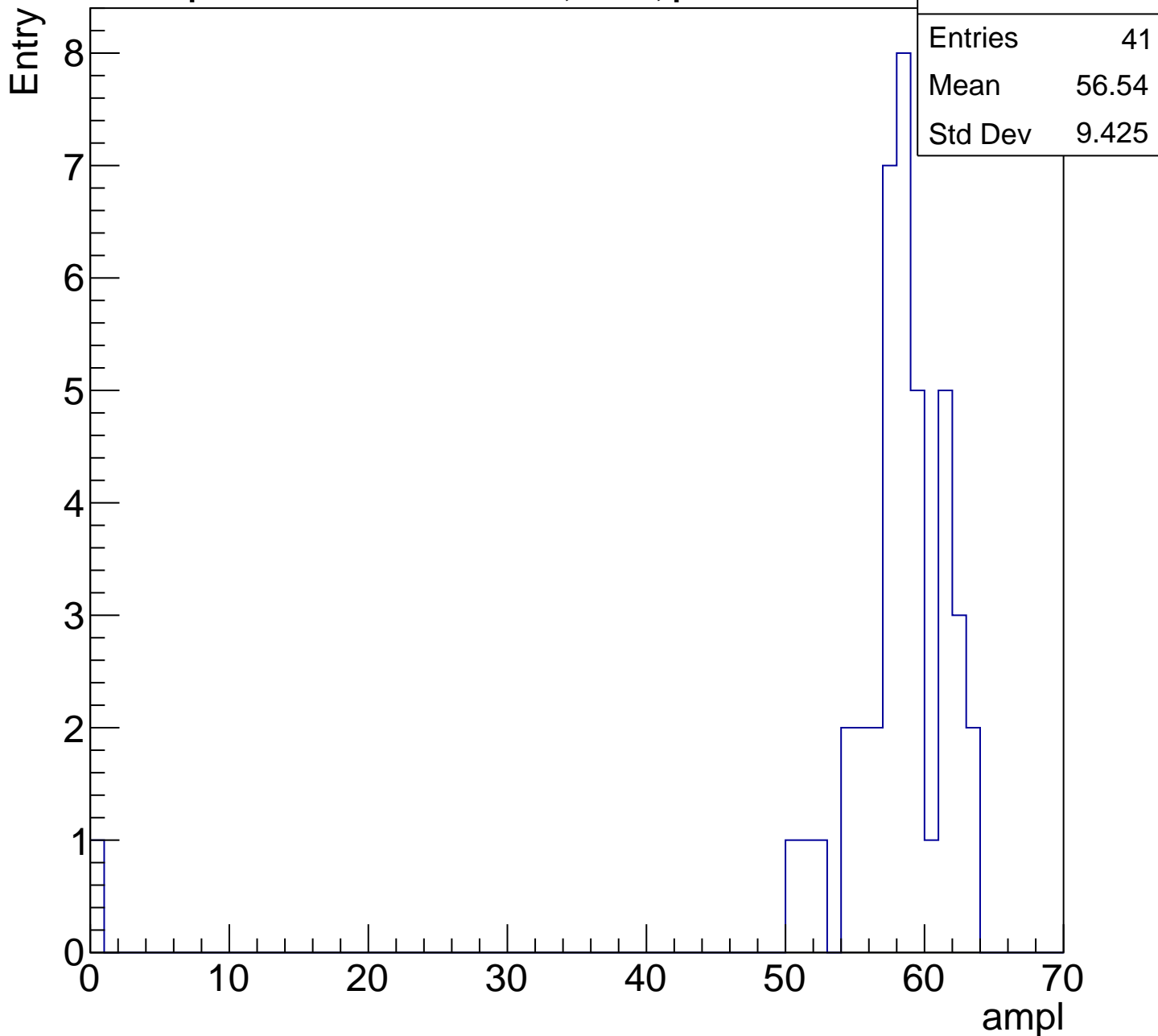
Entries	77
Mean	52.34
Std Dev	3.709

Entry



# B1L101S, U22-ch65, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

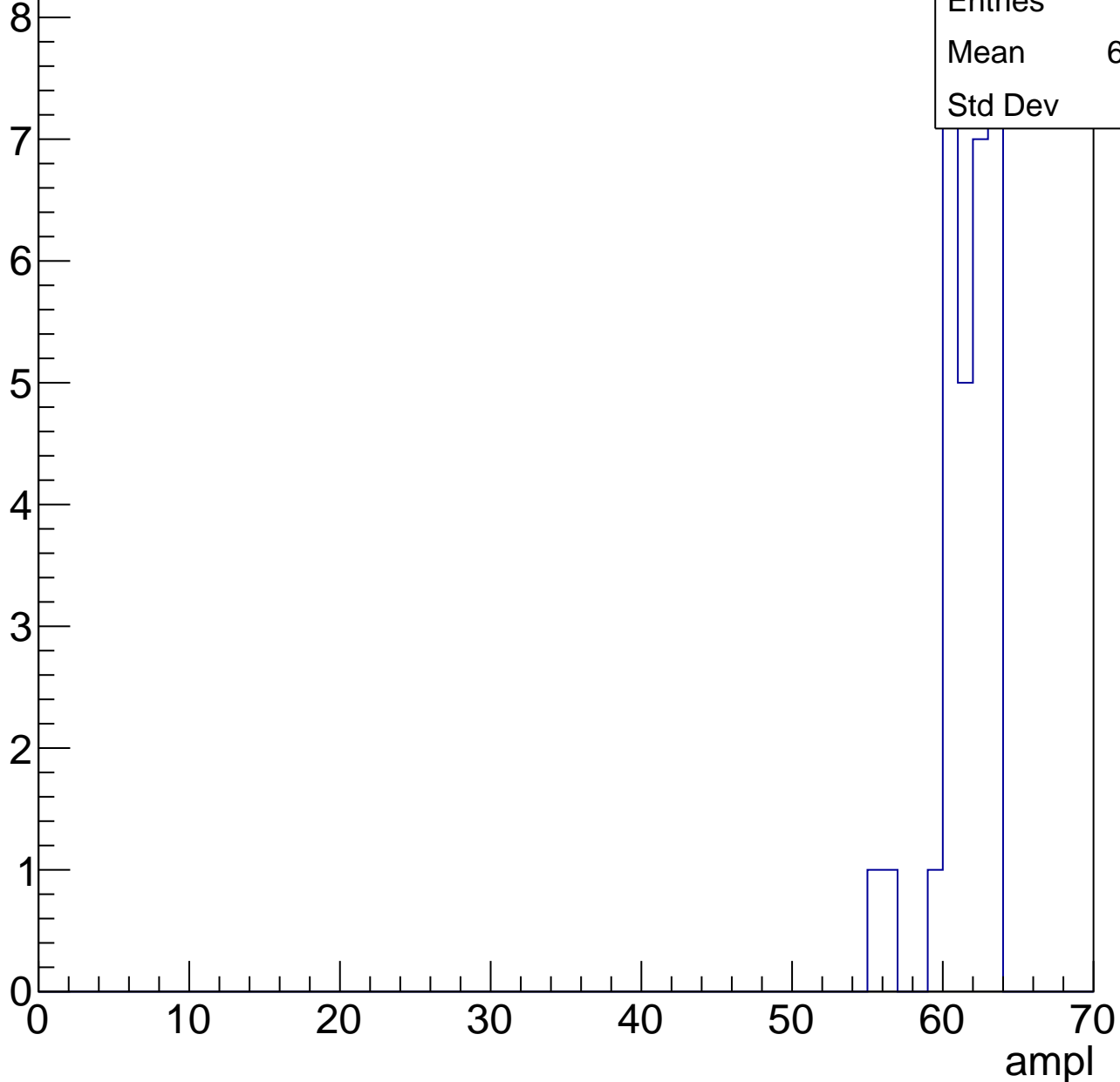


# B1L101S, U22-ch65, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

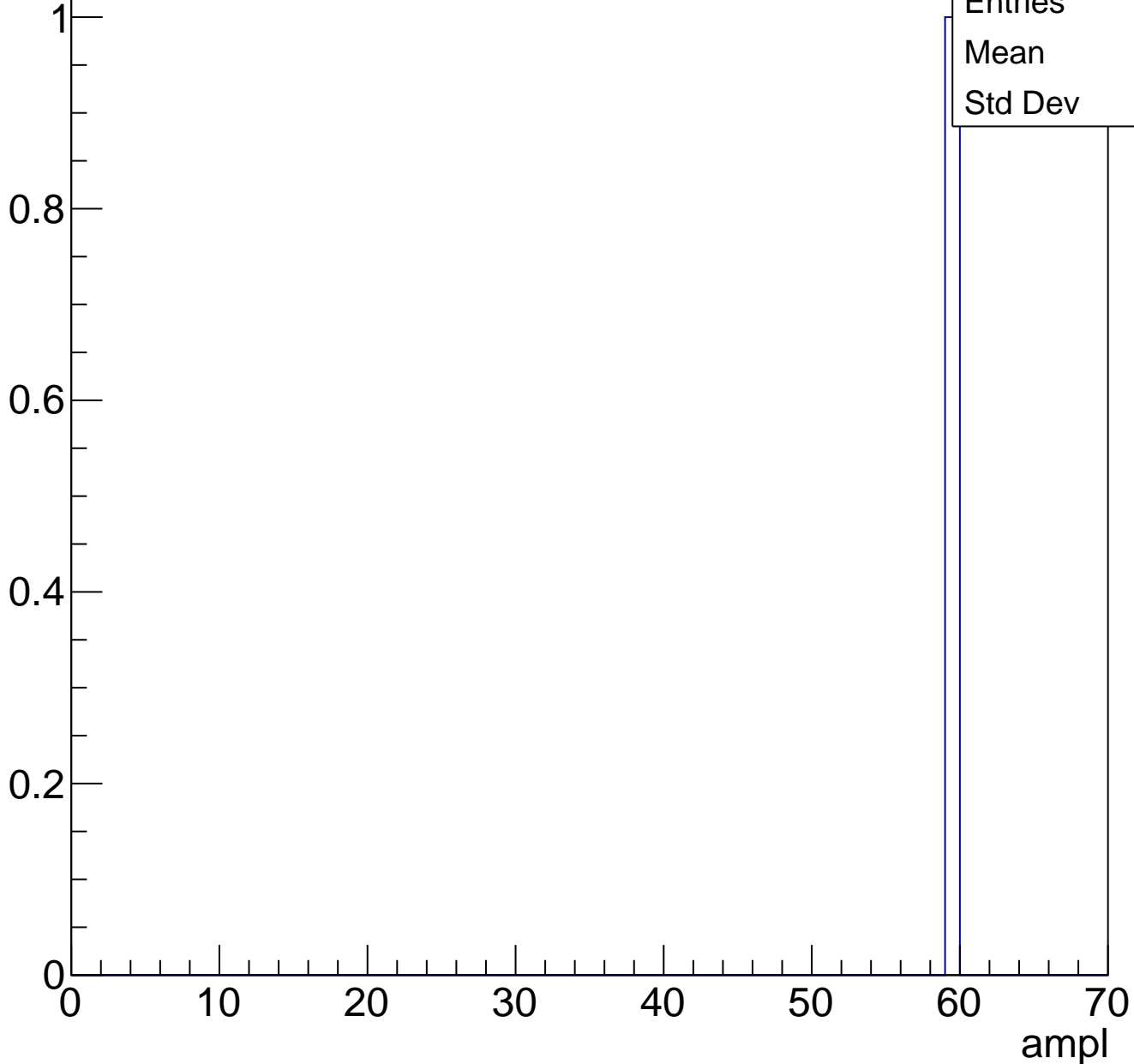
Entries	31
Mean	61.06
Std Dev	1.9



# B1L101S, U22-ch65, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U22-ch65, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U22-ch66, adc0

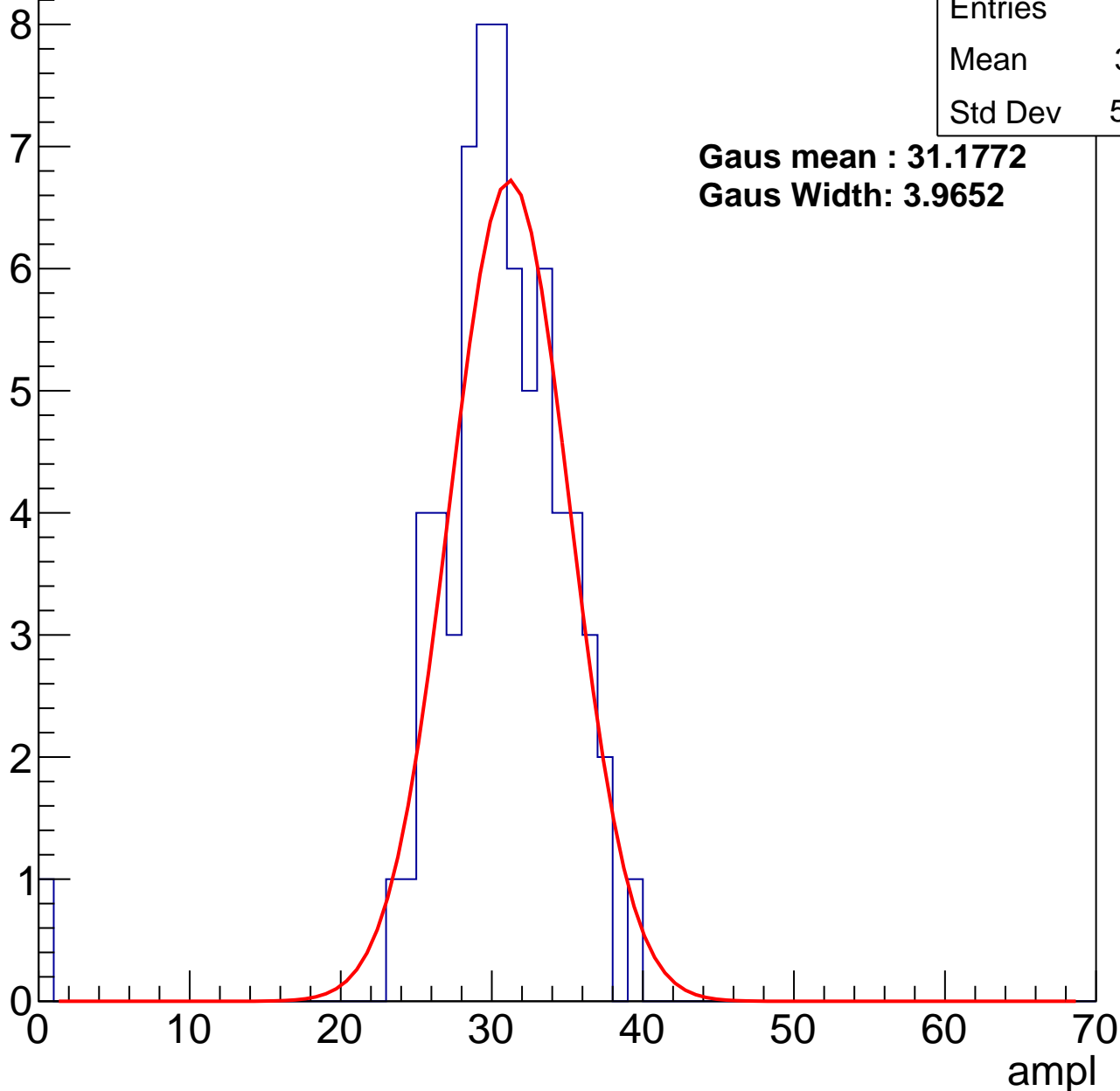
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	30.01
Std Dev	5.063

**Gaus mean : 31.1772**

**Gaus Width: 3.9652**



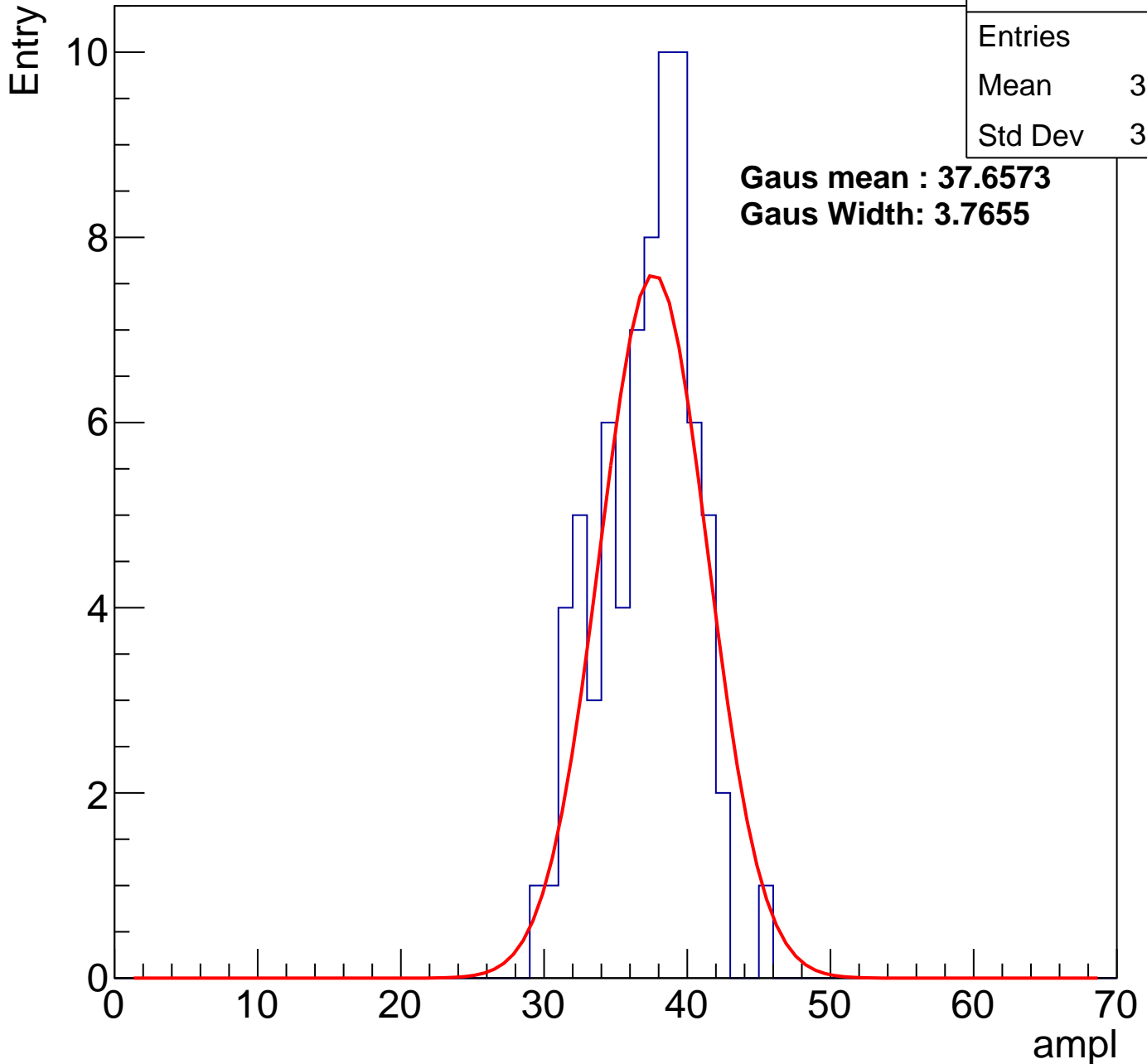
# B1L101S, U22-ch66, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	73
Mean	36.68
Std Dev	3.306

**Gaus mean : 37.6573**

**Gaus Width: 3.7655**



# B1L101S, U22-ch66, adc2

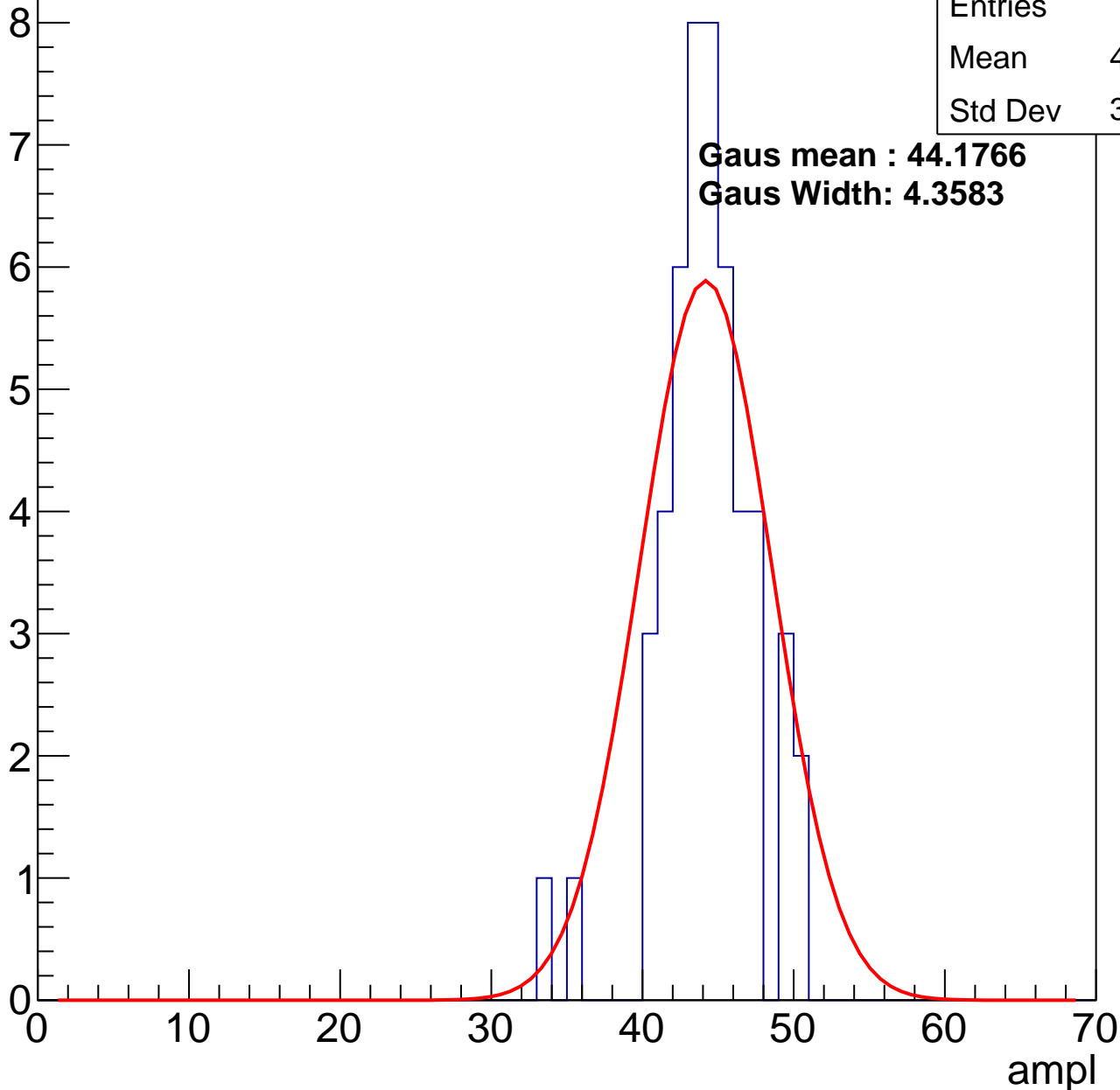
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	50
Mean	43.78
Std Dev	3.227

**Gaus mean : 44.1766**

**Gaus Width: 4.3583**



# B1L101S, U22-ch66, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	84
Mean	49.83
Std Dev	4.079

Entry

10

8

6

4

2

0

0

10

20

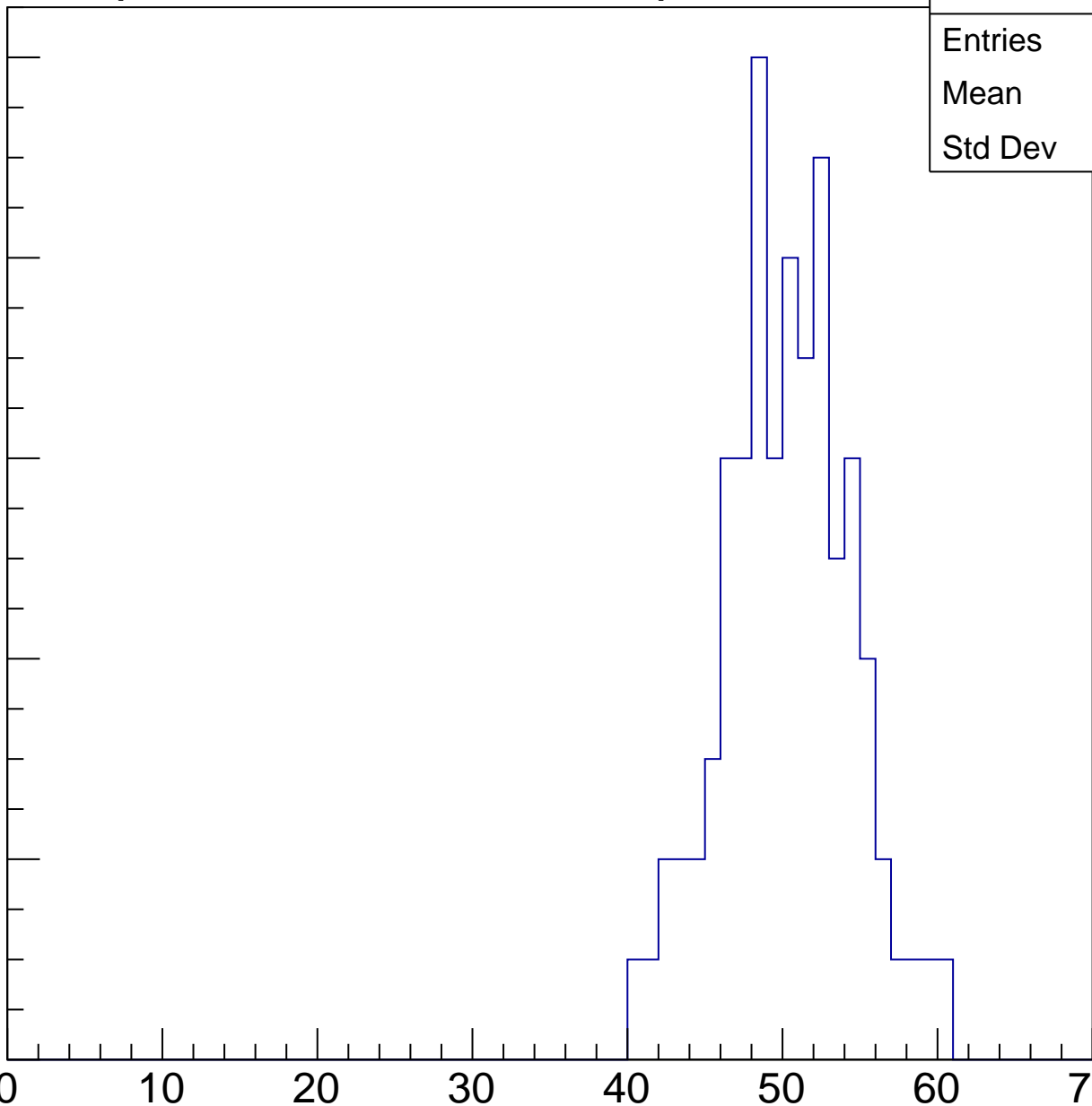
30

40

50

60

ampl

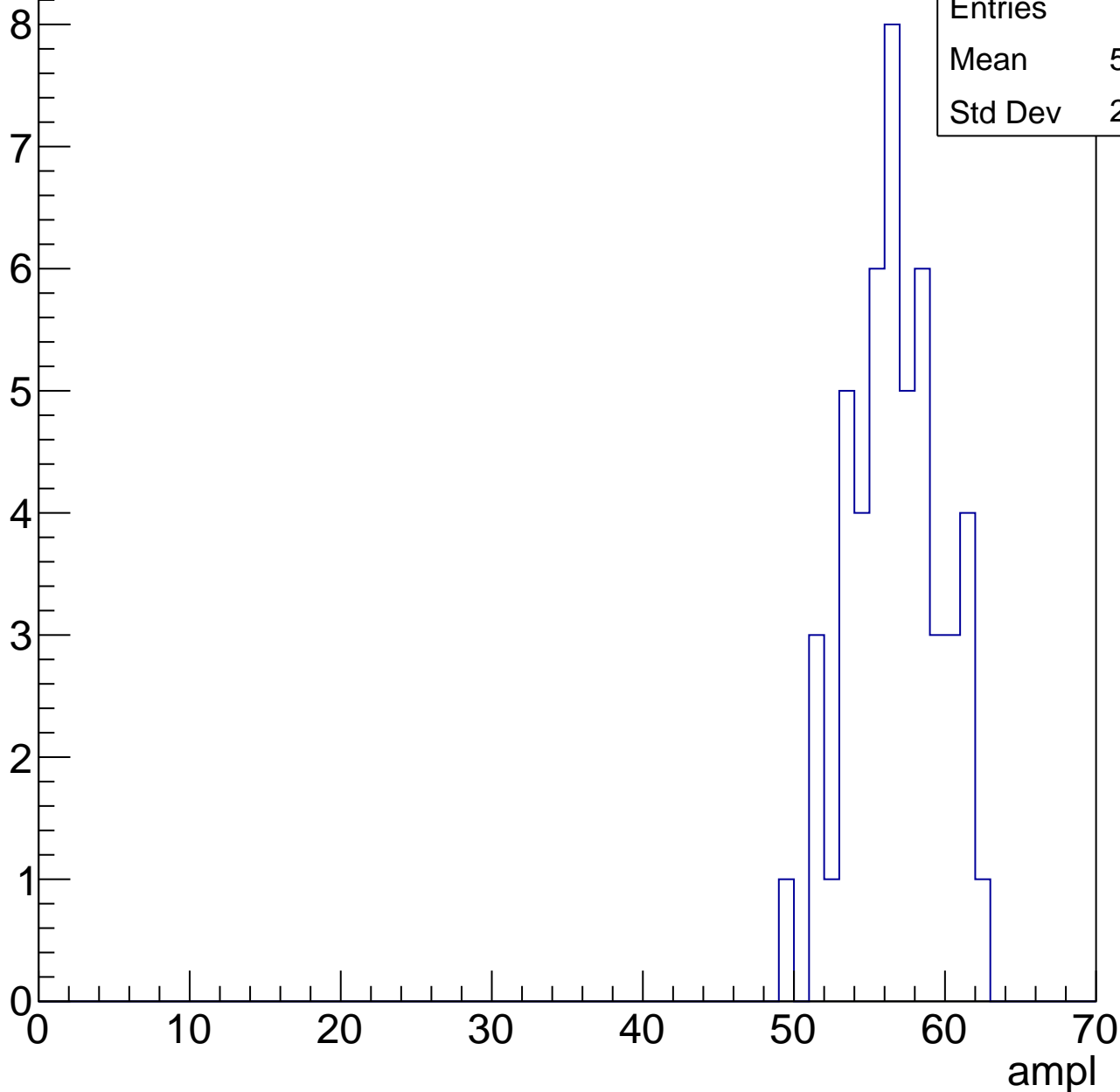


# B1L101S, U22-ch66, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	50
Mean	56.18
Std Dev	2.985

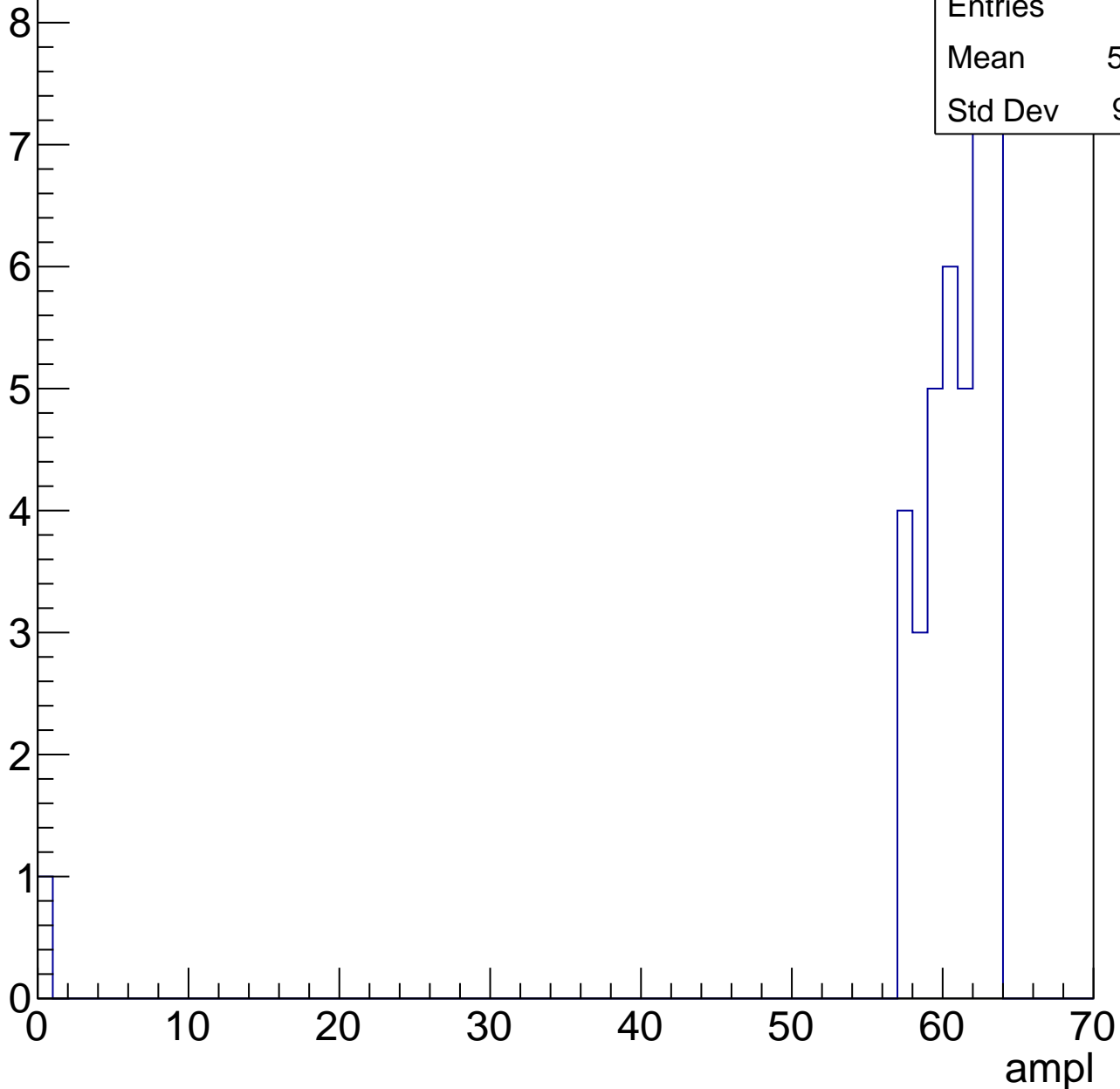


# B1L101S, U22-ch66, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

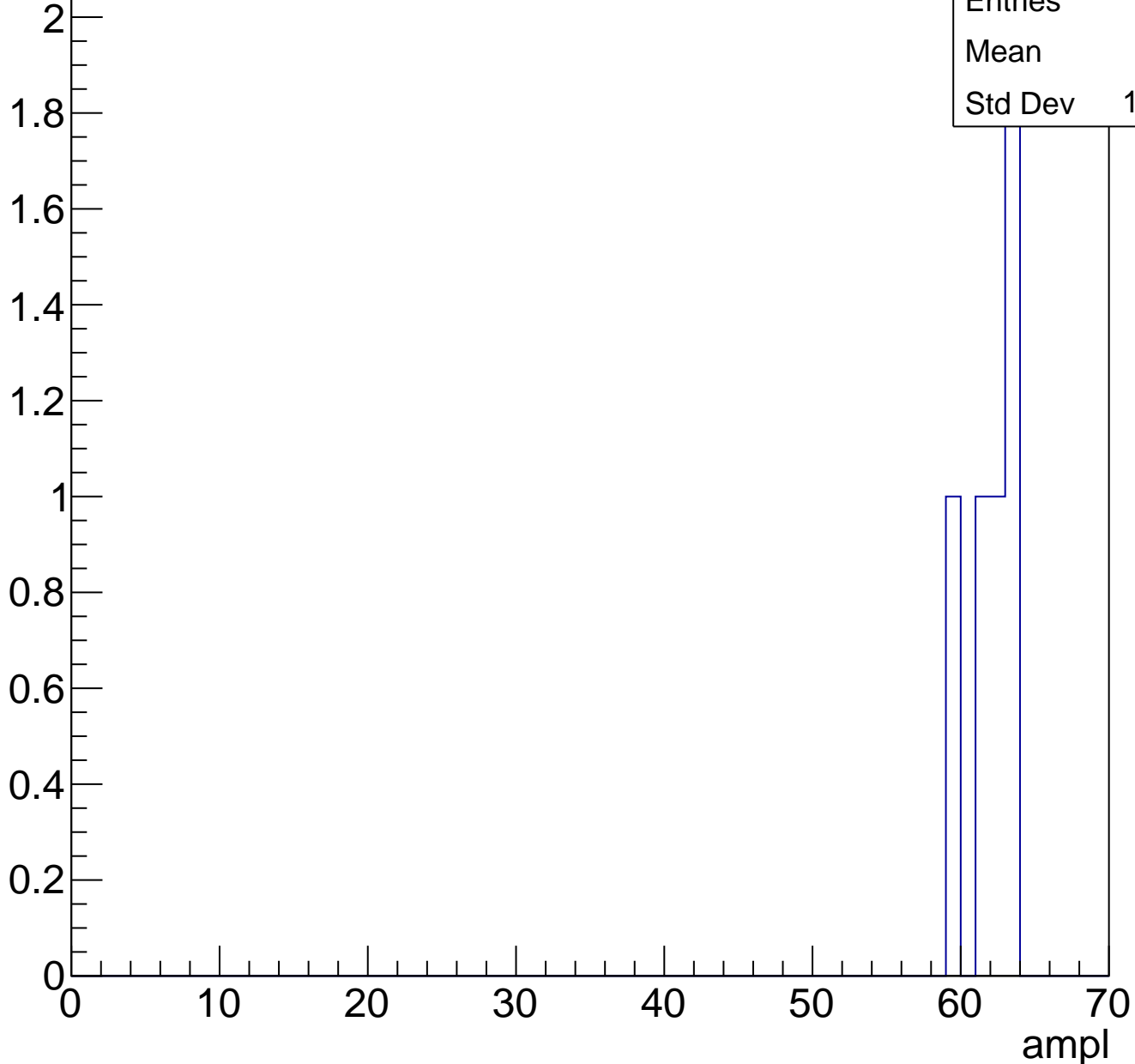
Entries	40
Mean	59.05
Std Dev	9.651



# B1L101S, U22-ch66, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U22-ch66, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L101S, U22-ch67, adc0

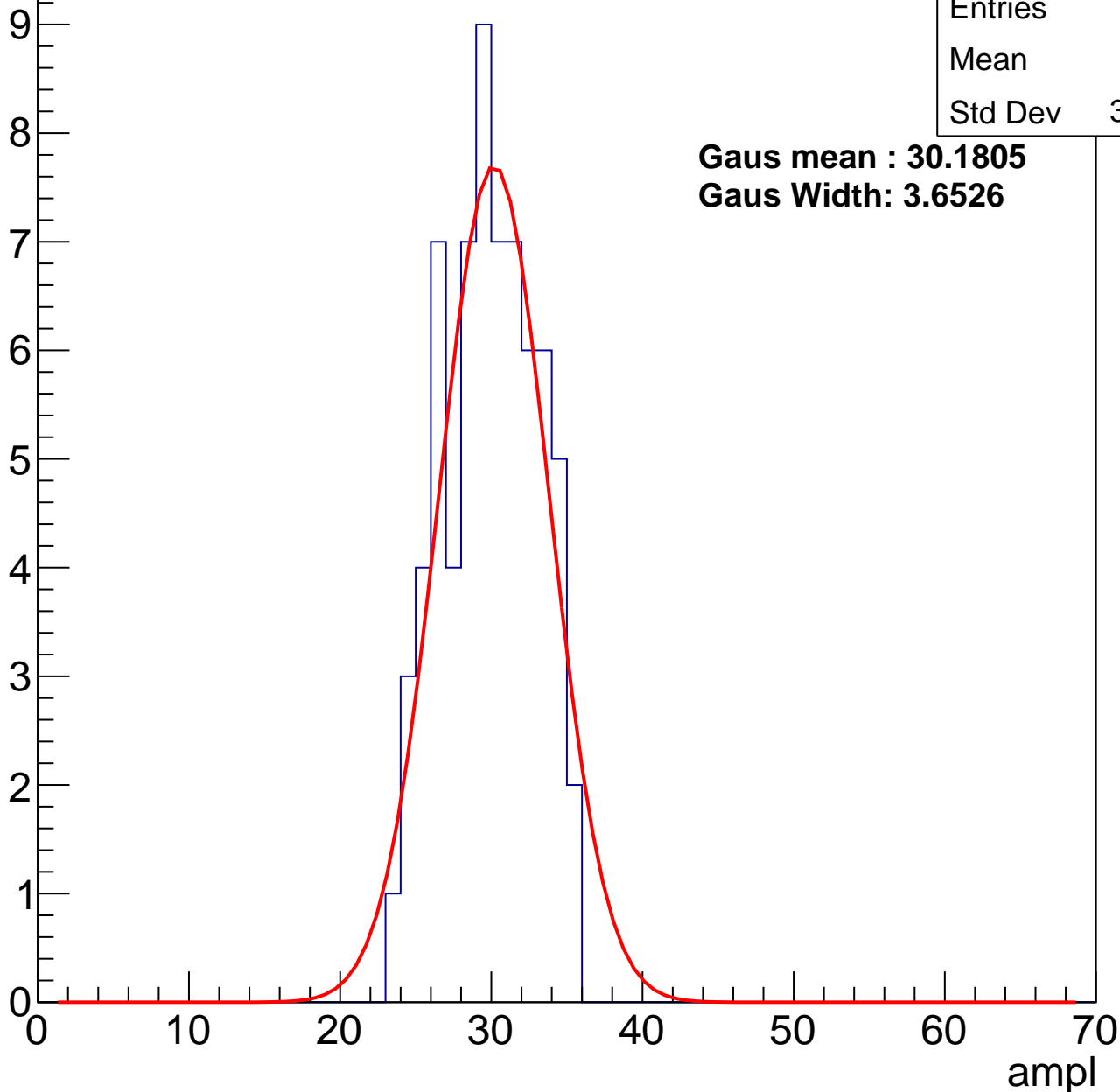
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	29.4
Std Dev	3.049

**Gaus mean : 30.1805**

**Gaus Width: 3.6526**



# B1L101S, U22-ch67, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

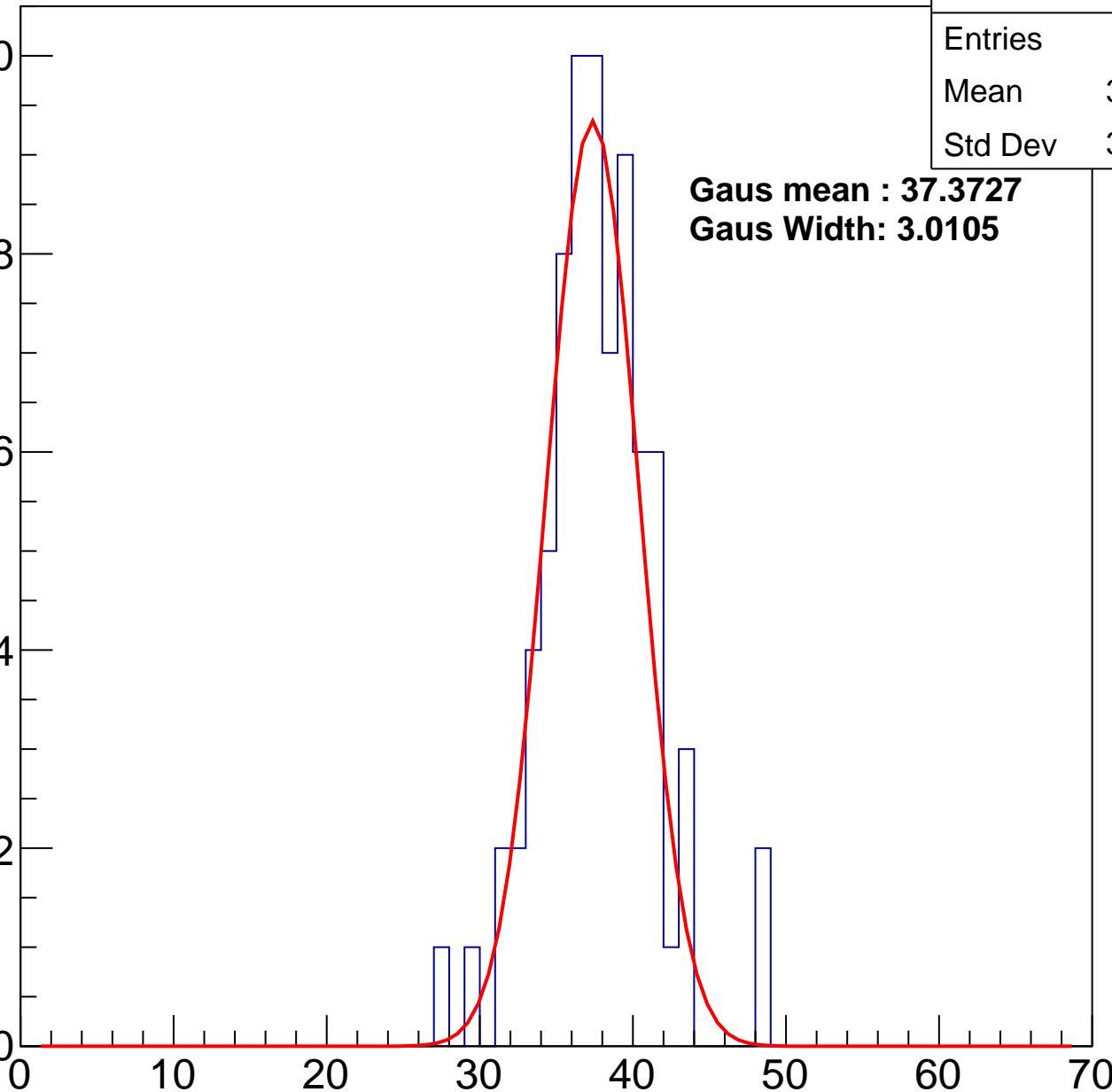
Entries	77
Mean	37.19
Std Dev	3.607

**Gaus mean : 37.3727**

**Gaus Width: 3.0105**

10  
8  
6  
4  
2  
0

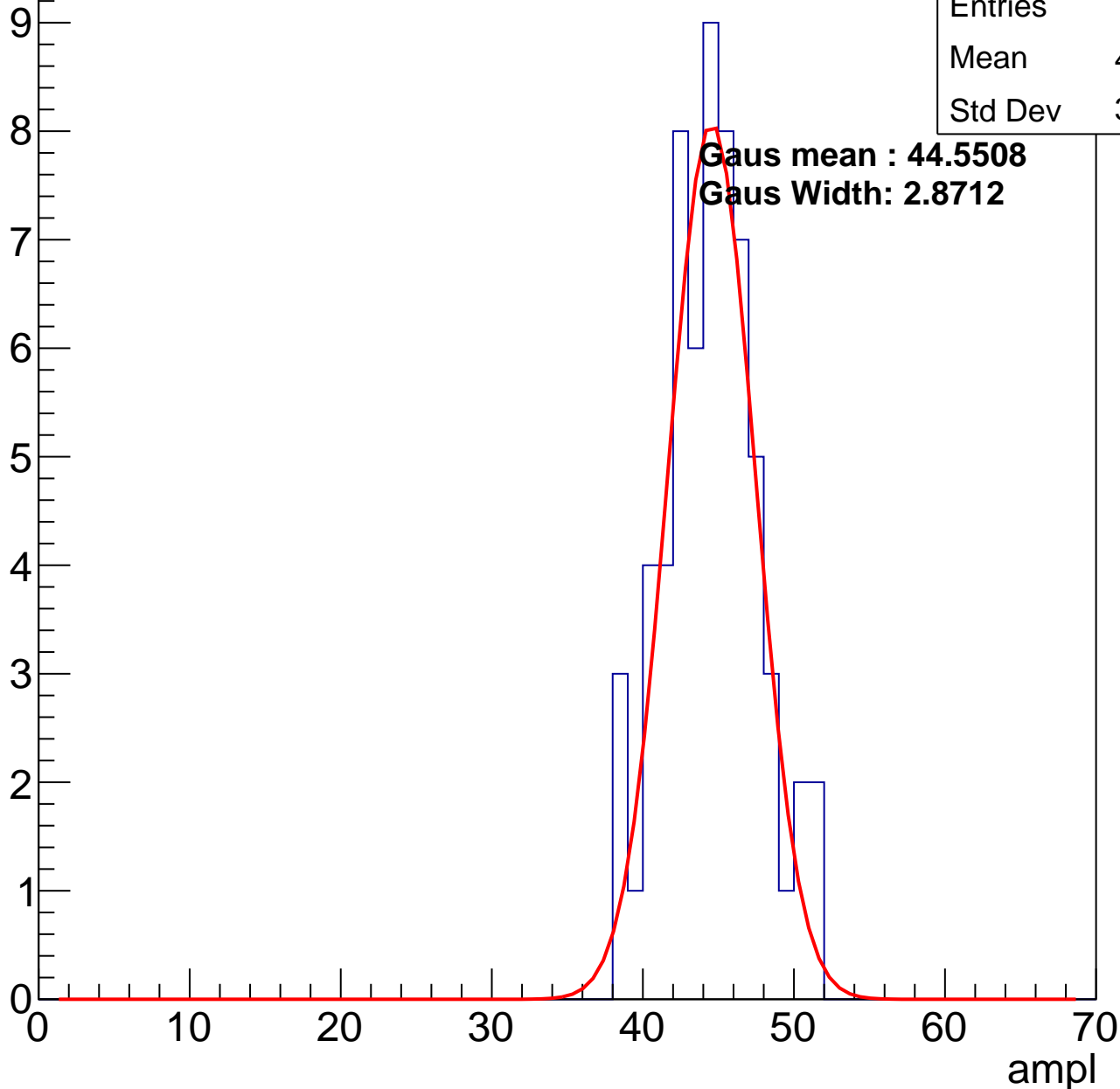
ampl



# B1L101S, U22-ch67, adc2

calib\_packv5\_042523\_0143.root, FC#0, port D2

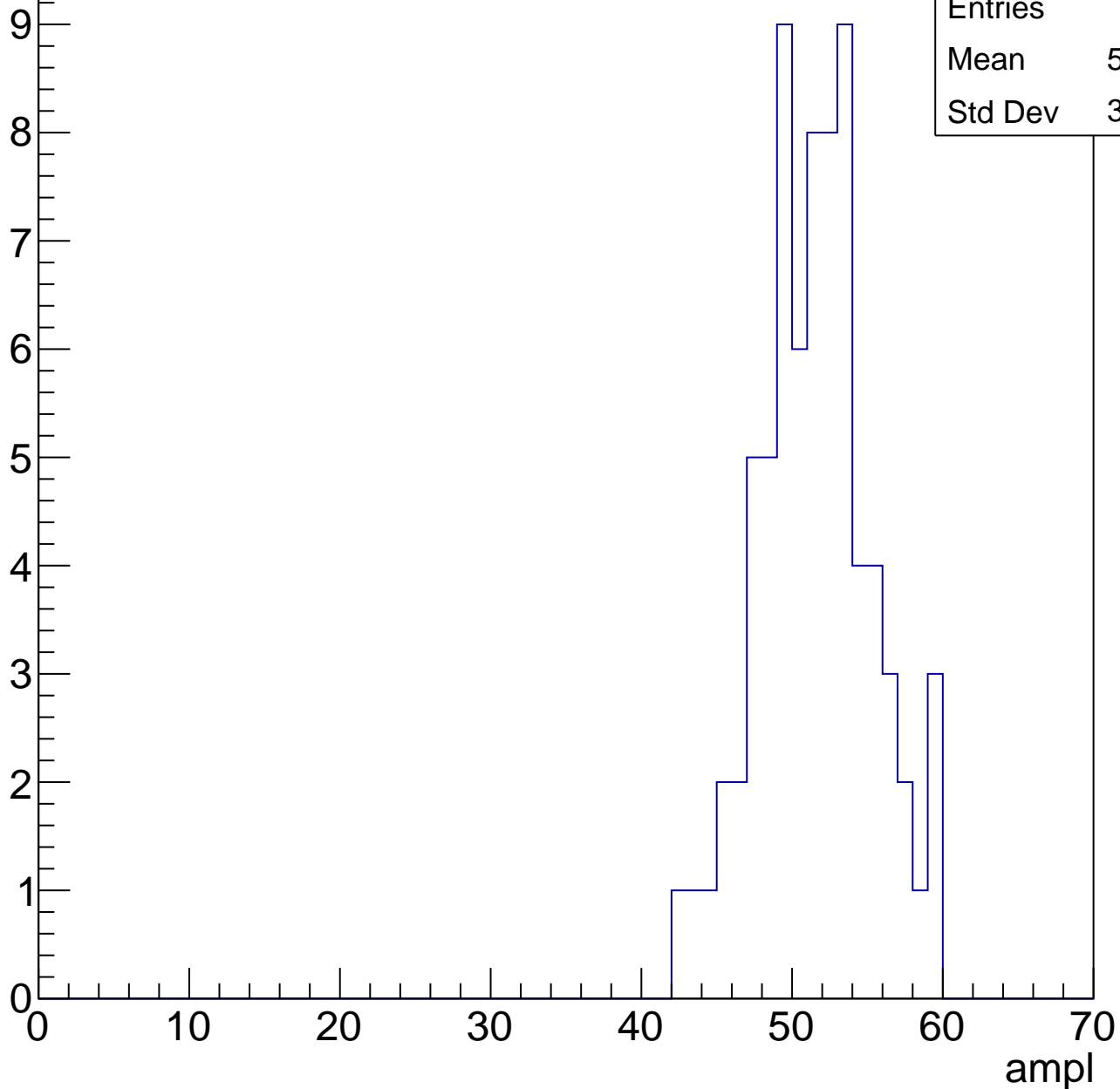
Entry



# B1L101S, U22-ch67, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



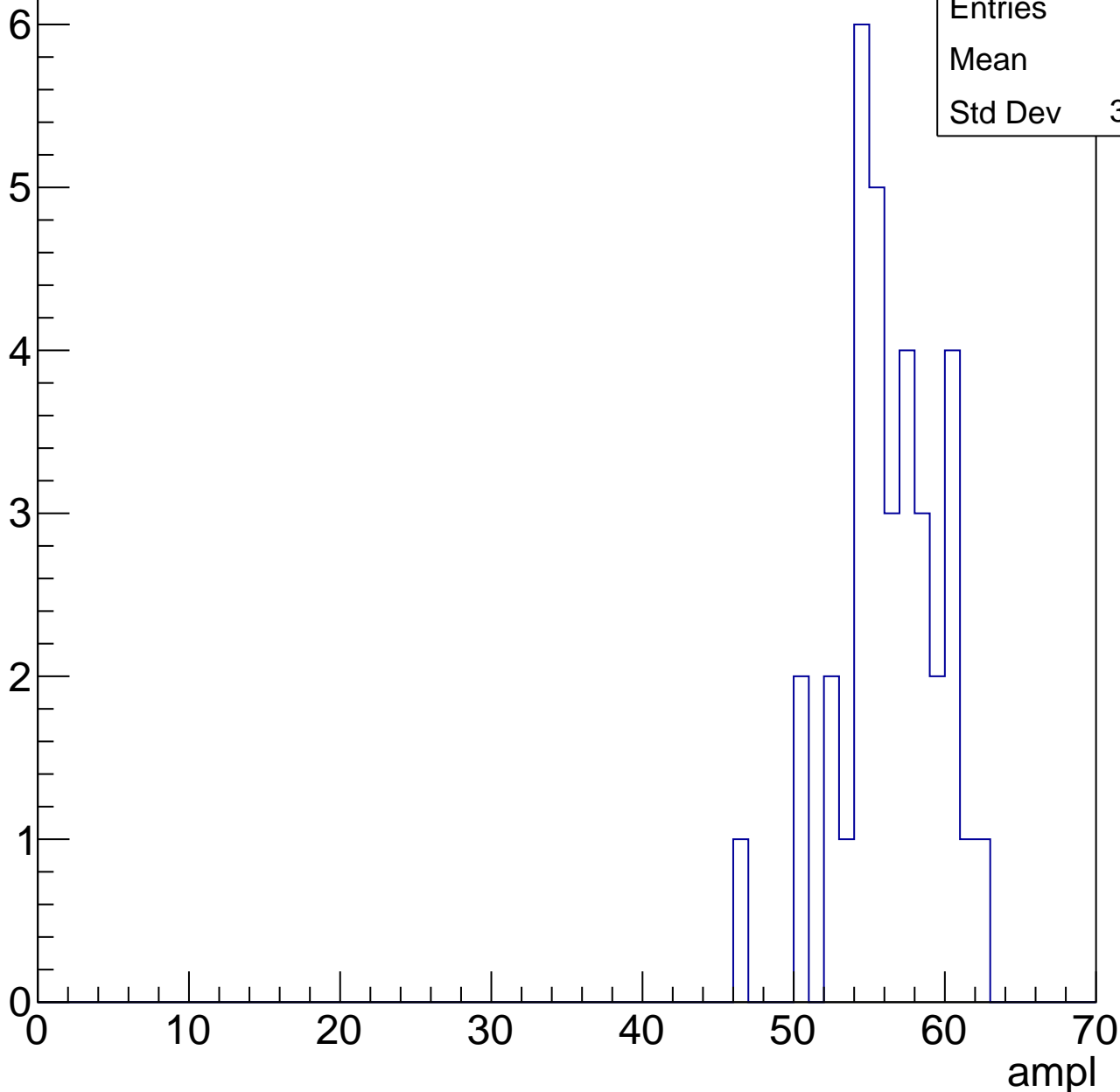
Entries	74
Mean	51.09
Std Dev	3.702

# B1L101S, U22-ch67, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

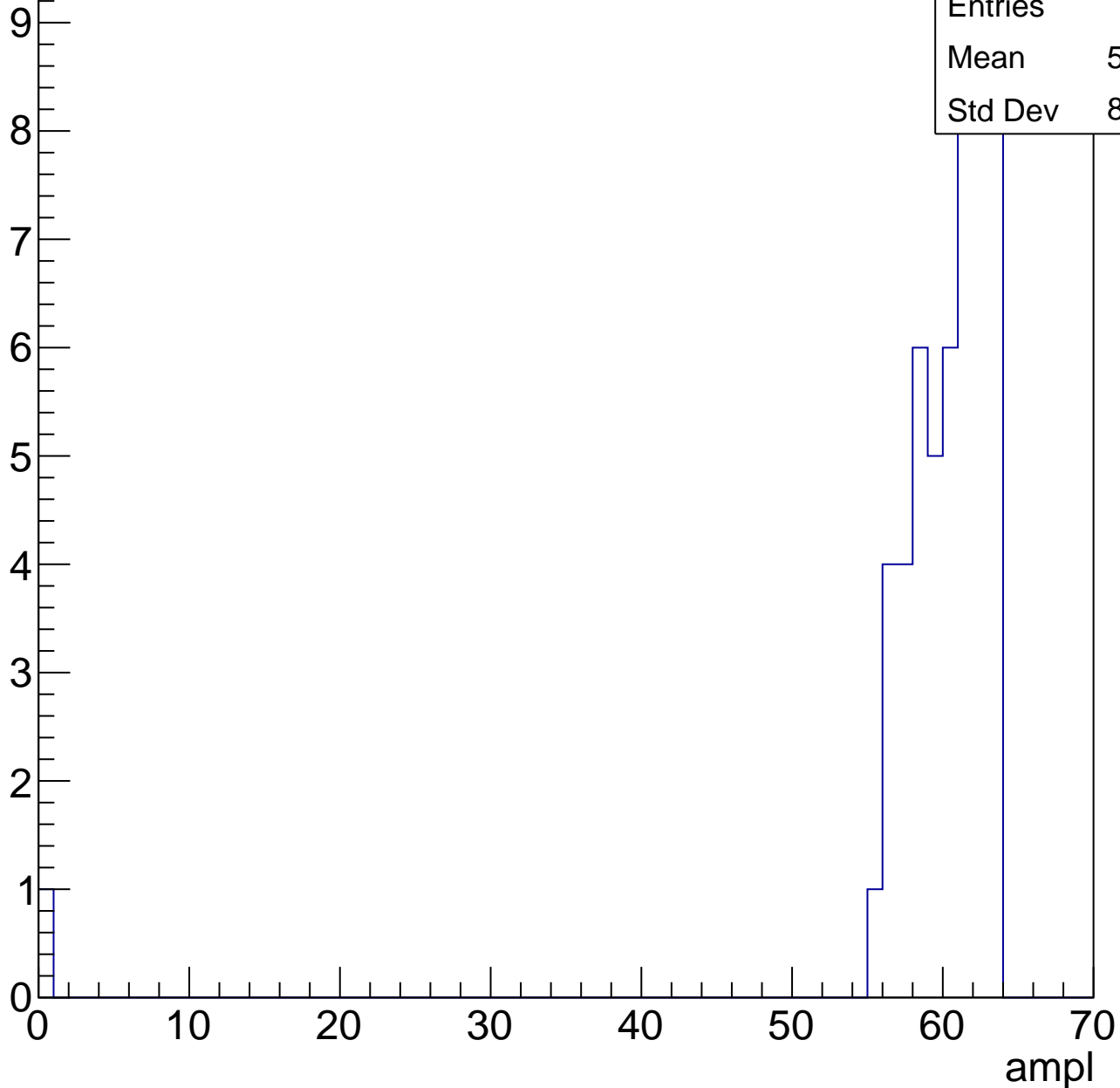
Entries	35
Mean	55.8
Std Dev	3.379



# B1L101S, U22-ch67, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U22-ch67, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	3
Mean	62.67
Std Dev	0.4714

ampl

0 10 20 30 40 50 60 70



# B1L101S, U22-ch67, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L101S, U22-ch68, adc0

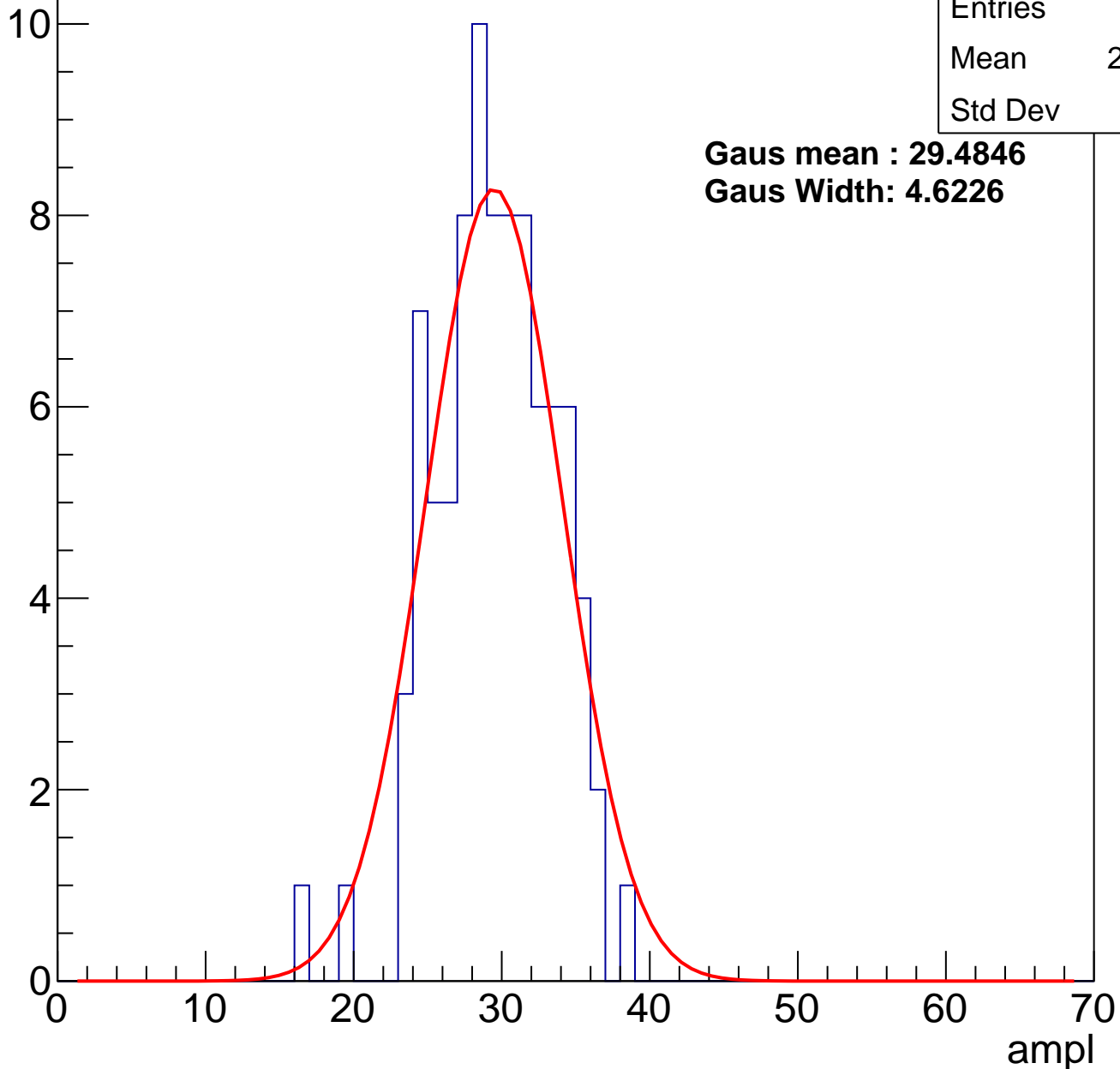
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	89
Mean	29.07
Std Dev	3.94

**Gaus mean : 29.4846**

**Gaus Width: 4.6226**

Entry



# B1L101S, U22-ch68, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	72
Mean	37.57
Std Dev	3.933

**Gaus mean : 37.6422**

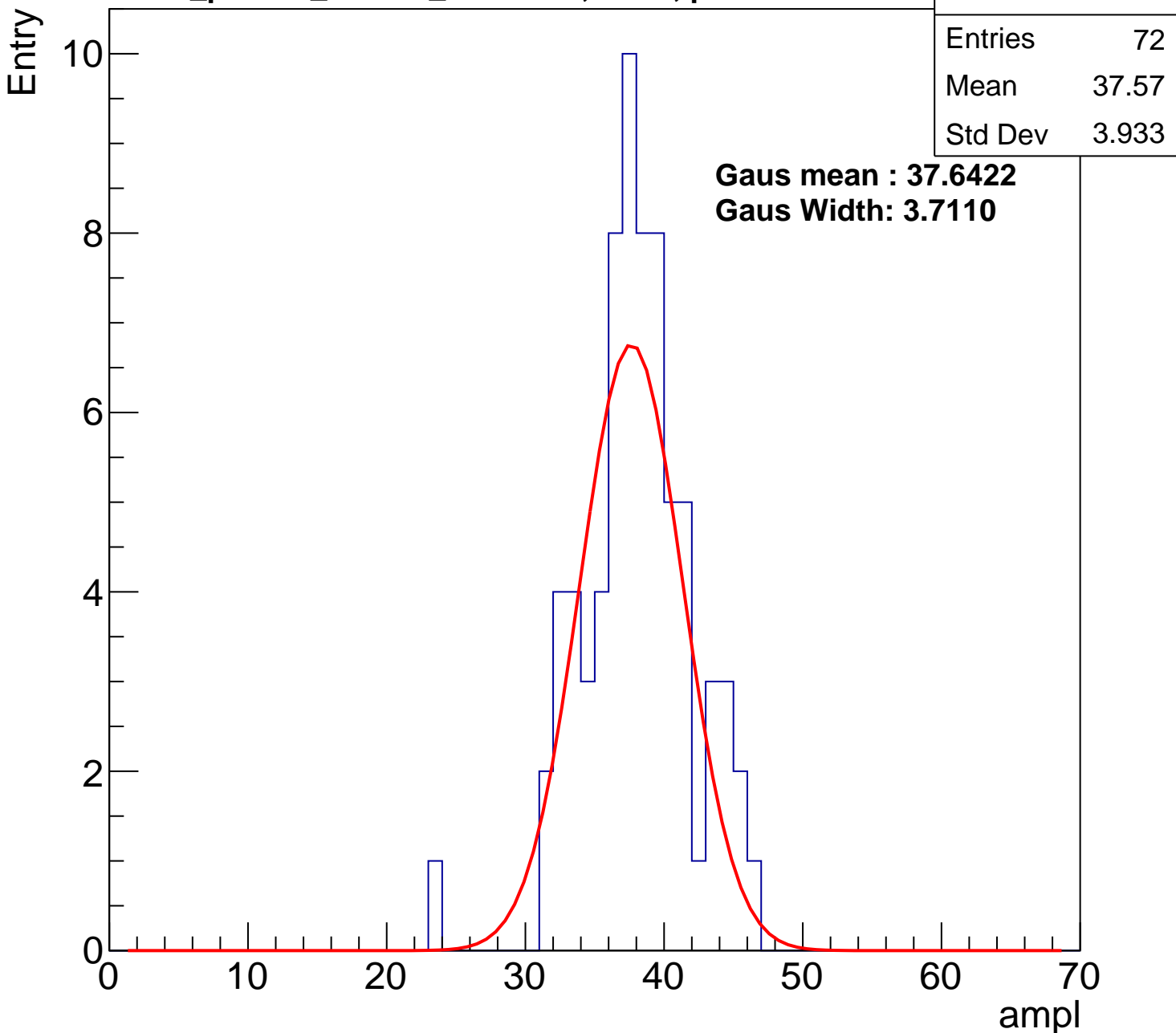
**Gaus Width: 3.7110**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U22-ch68, adc2

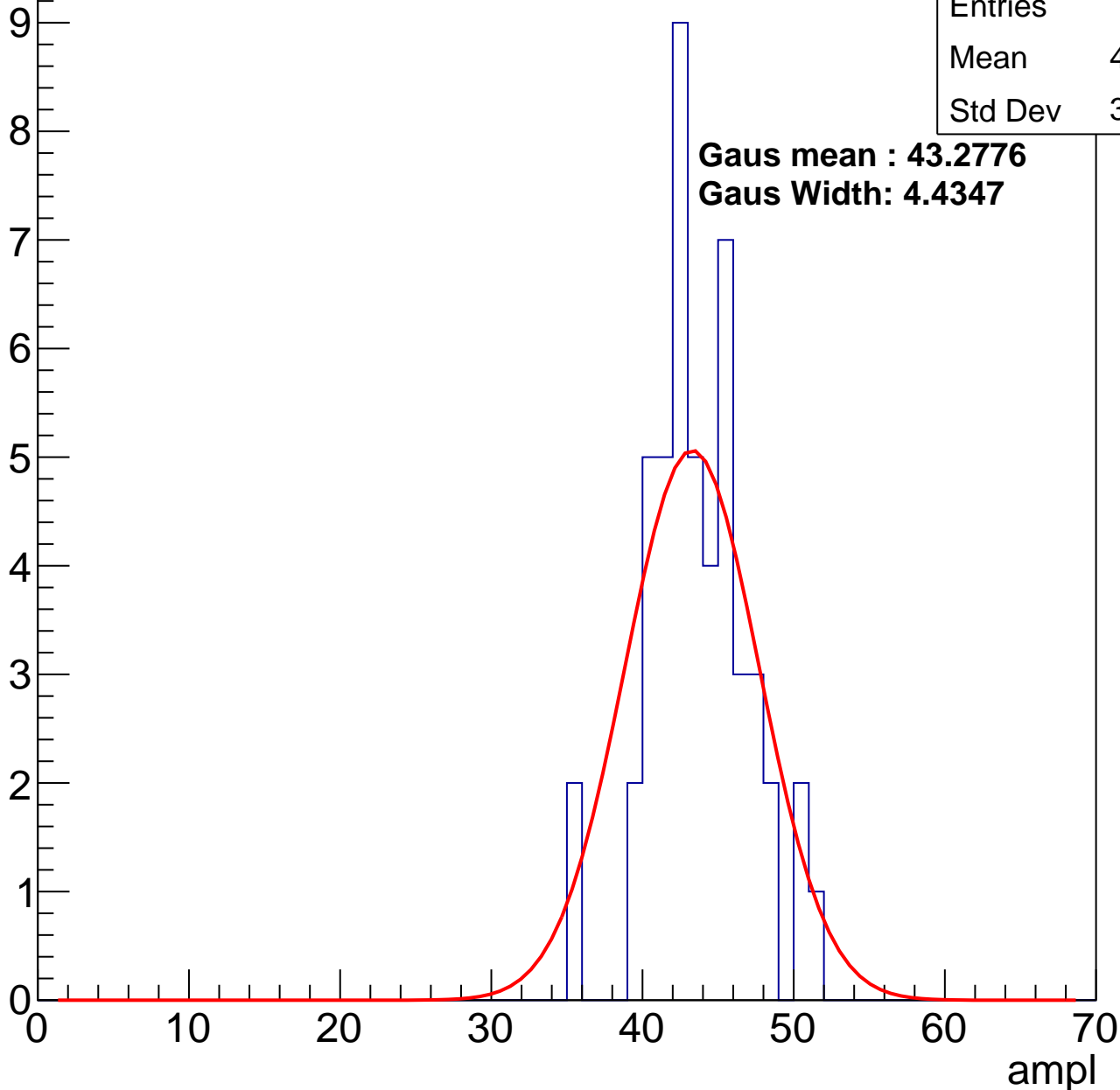
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	50
Mean	43.26
Std Dev	3.315

**Gaus mean : 43.2776**

**Gaus Width: 4.4347**

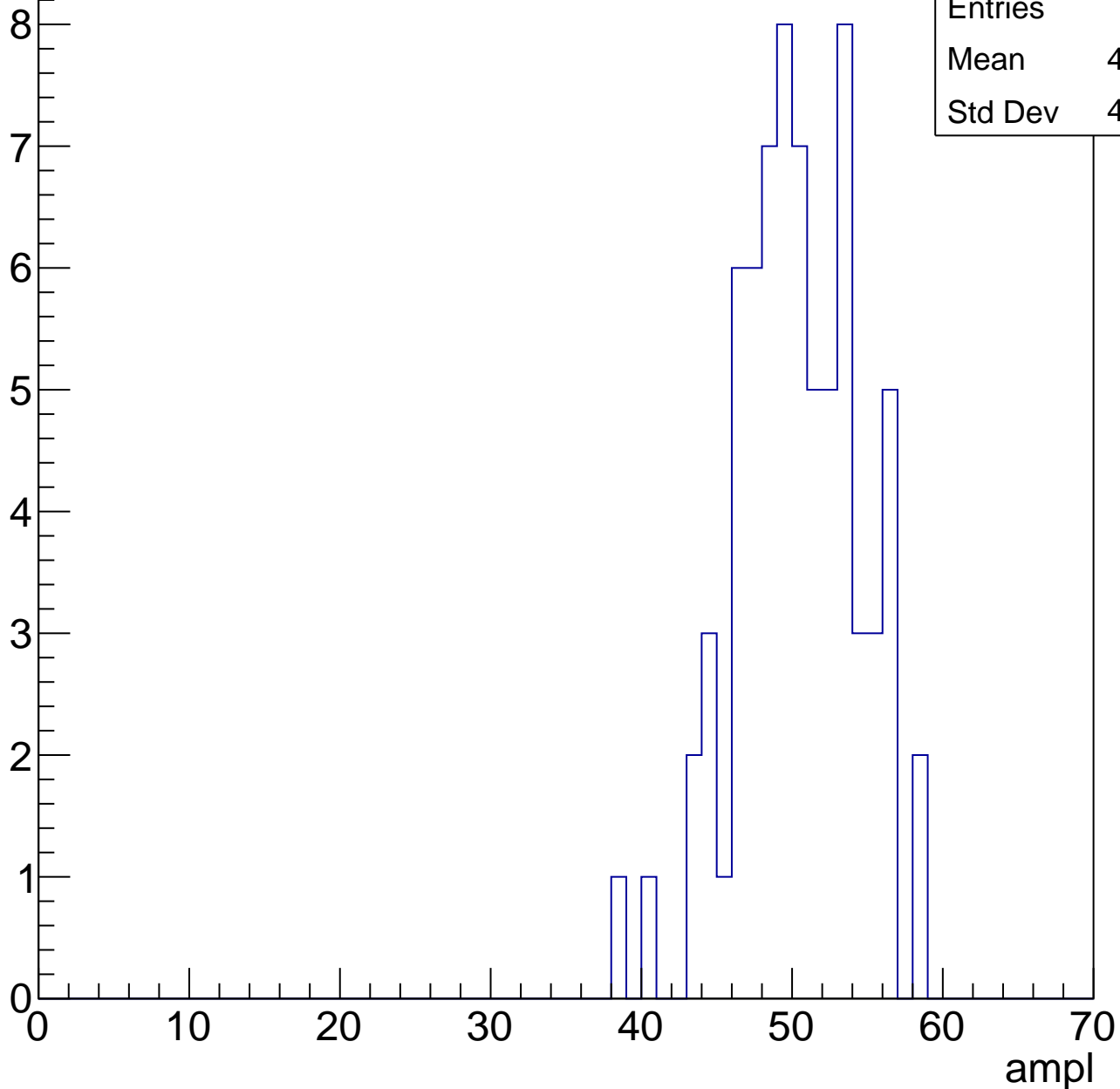


# B1L101S, U22-ch68, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

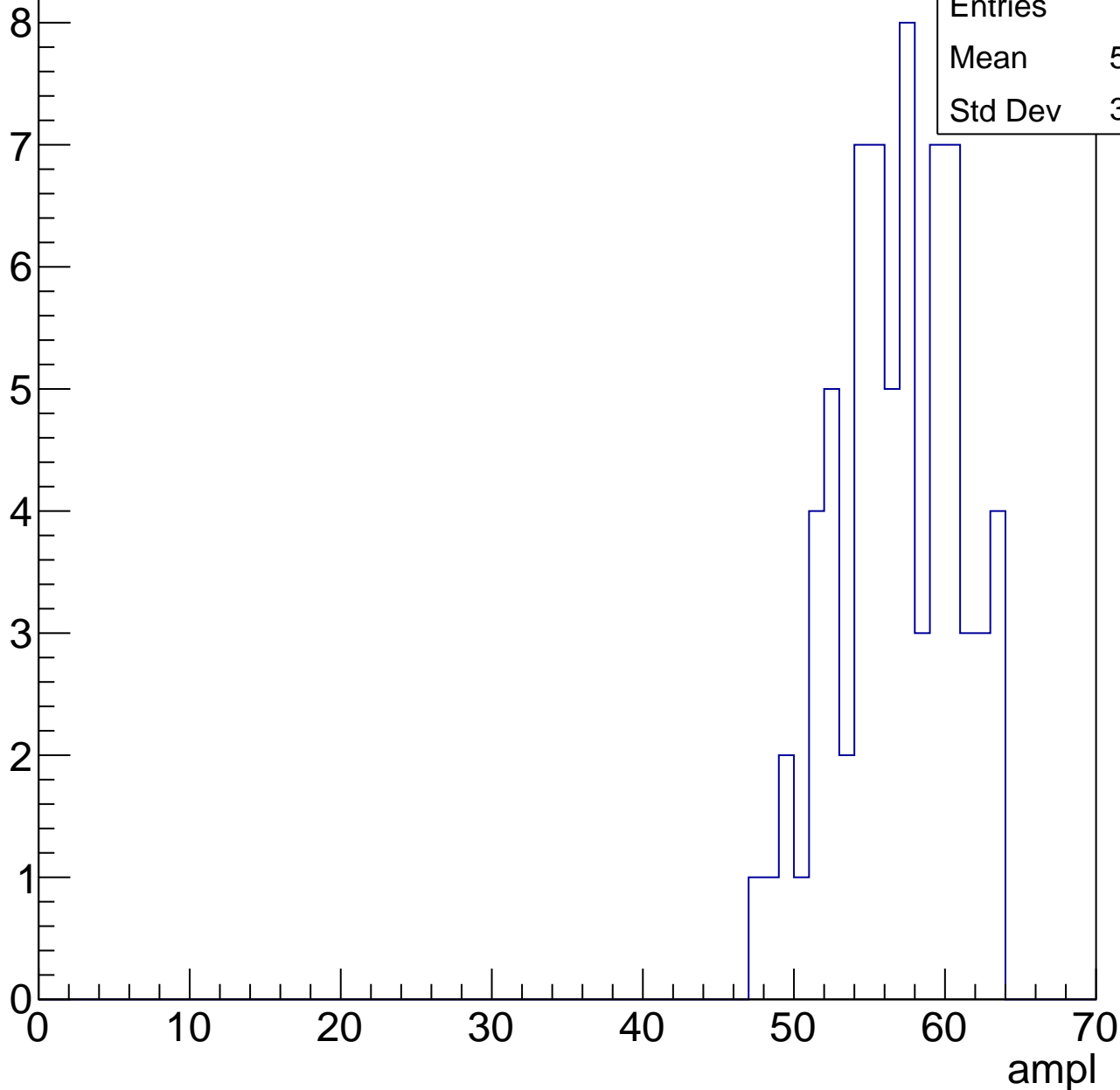
Entries	73
Mean	49.85
Std Dev	4.033



# B1L101S, U22-ch68, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

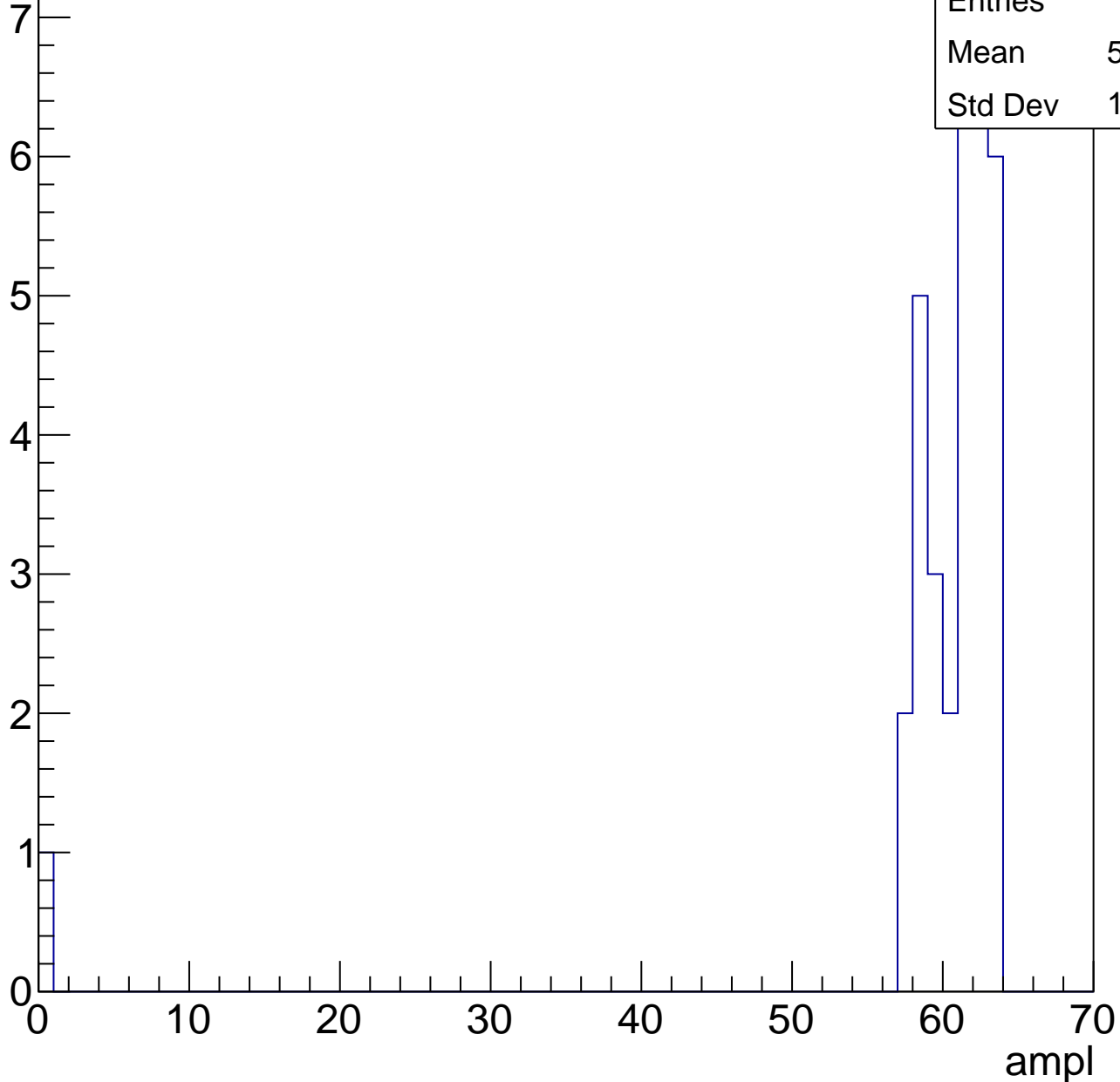


Entries	70
Mean	56.29
Std Dev	3.928

# B1L101S, U22-ch68, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U22-ch68, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U22-ch68, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U22-ch69, adc0

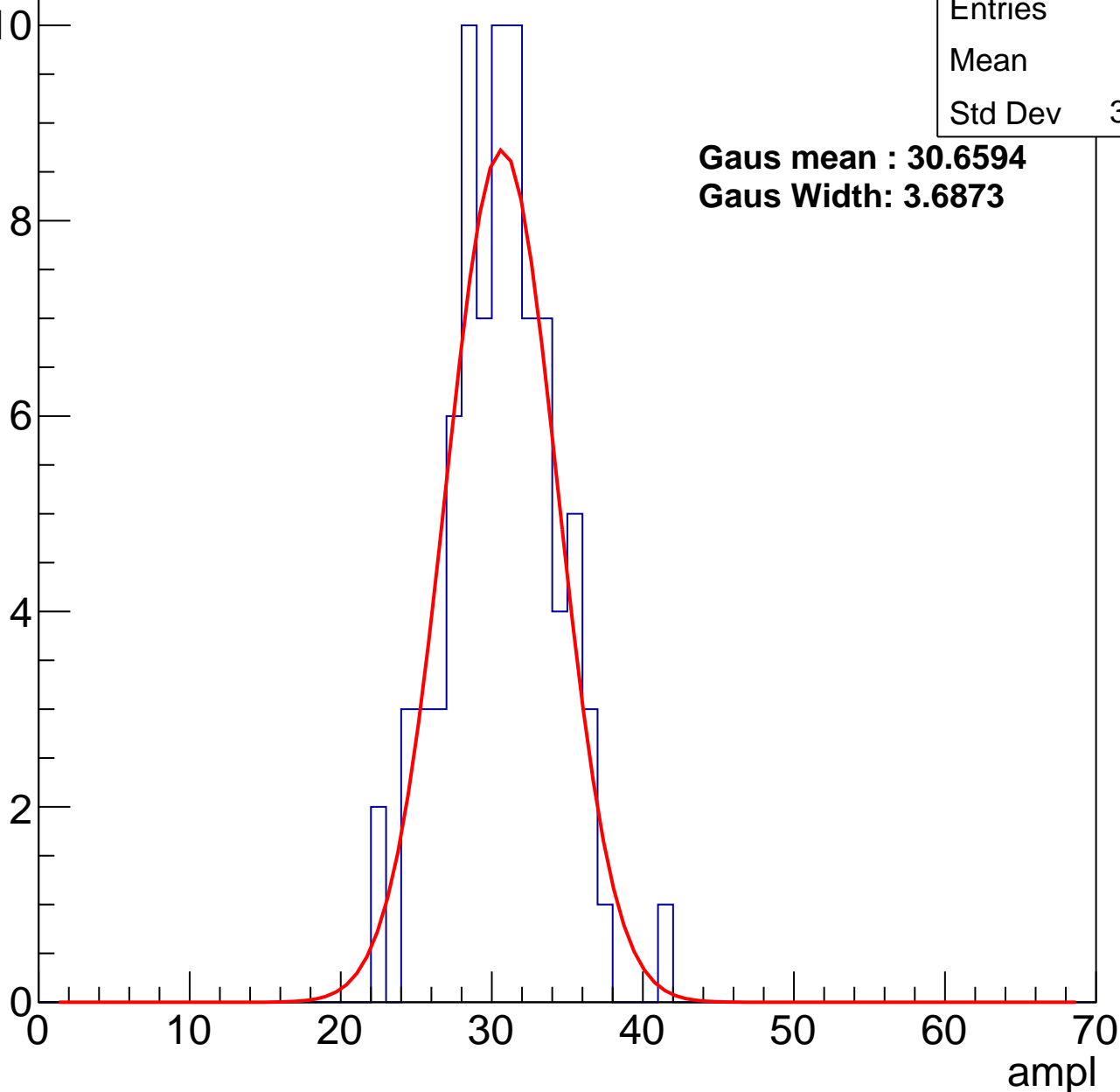
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	82
Mean	30.2
Std Dev	3.535

**Gaus mean : 30.6594**

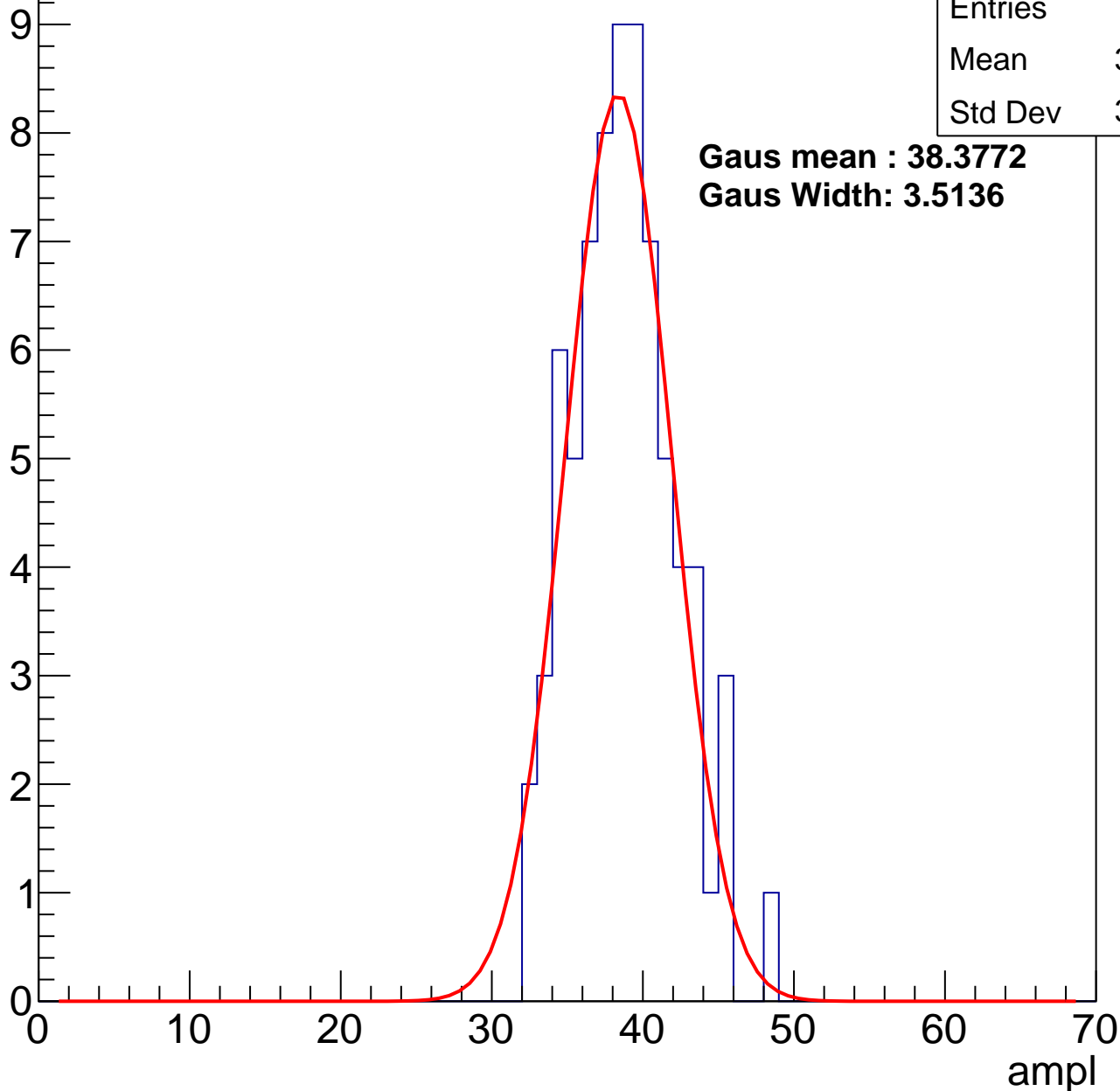
**Gaus Width: 3.6873**



# B1L101S, U22-ch69, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U22-ch69, adc2

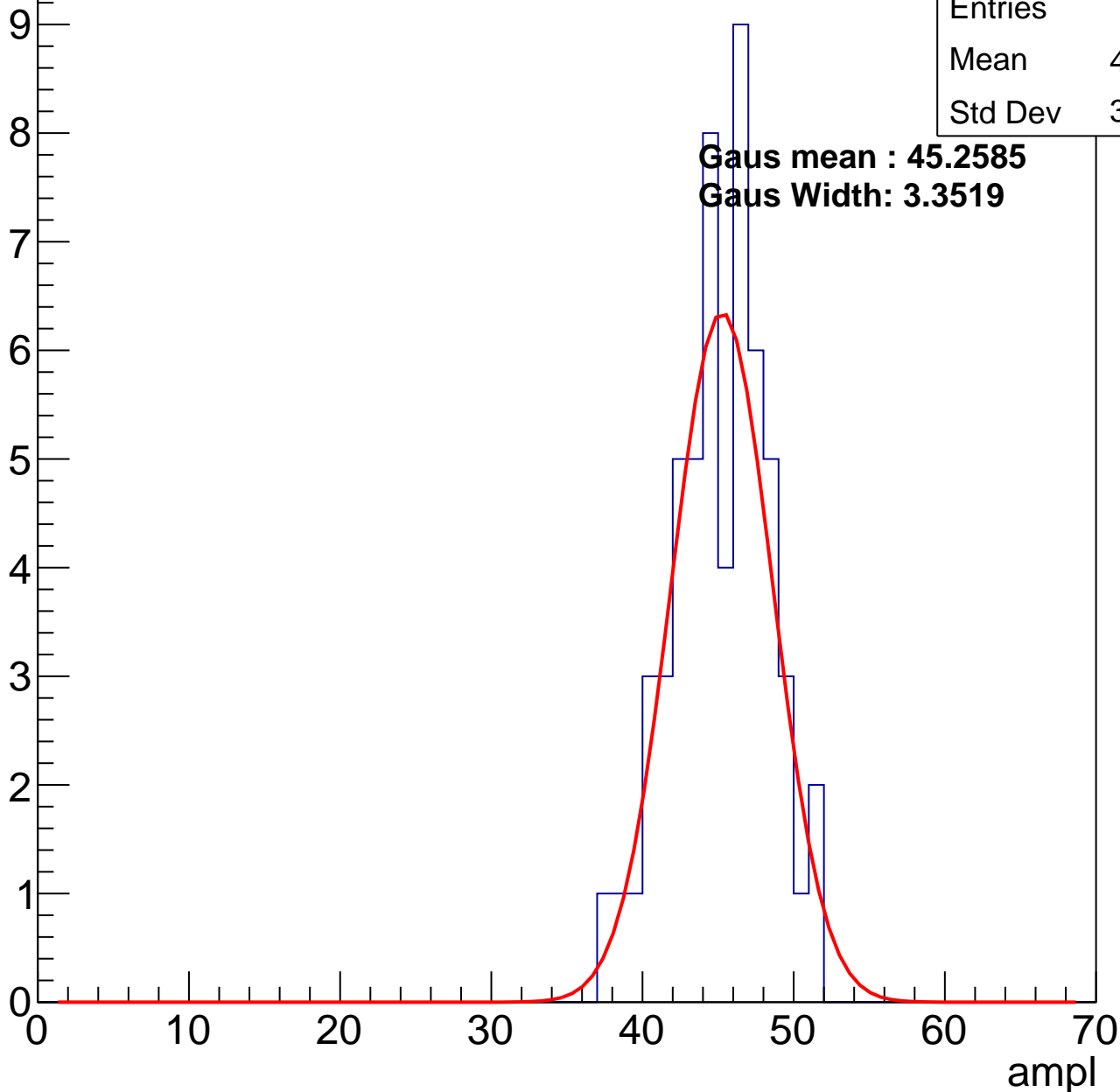
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	57
Mean	44.72
Std Dev	3.144

**Gaus mean : 45.2585**

**Gaus Width: 3.3519**

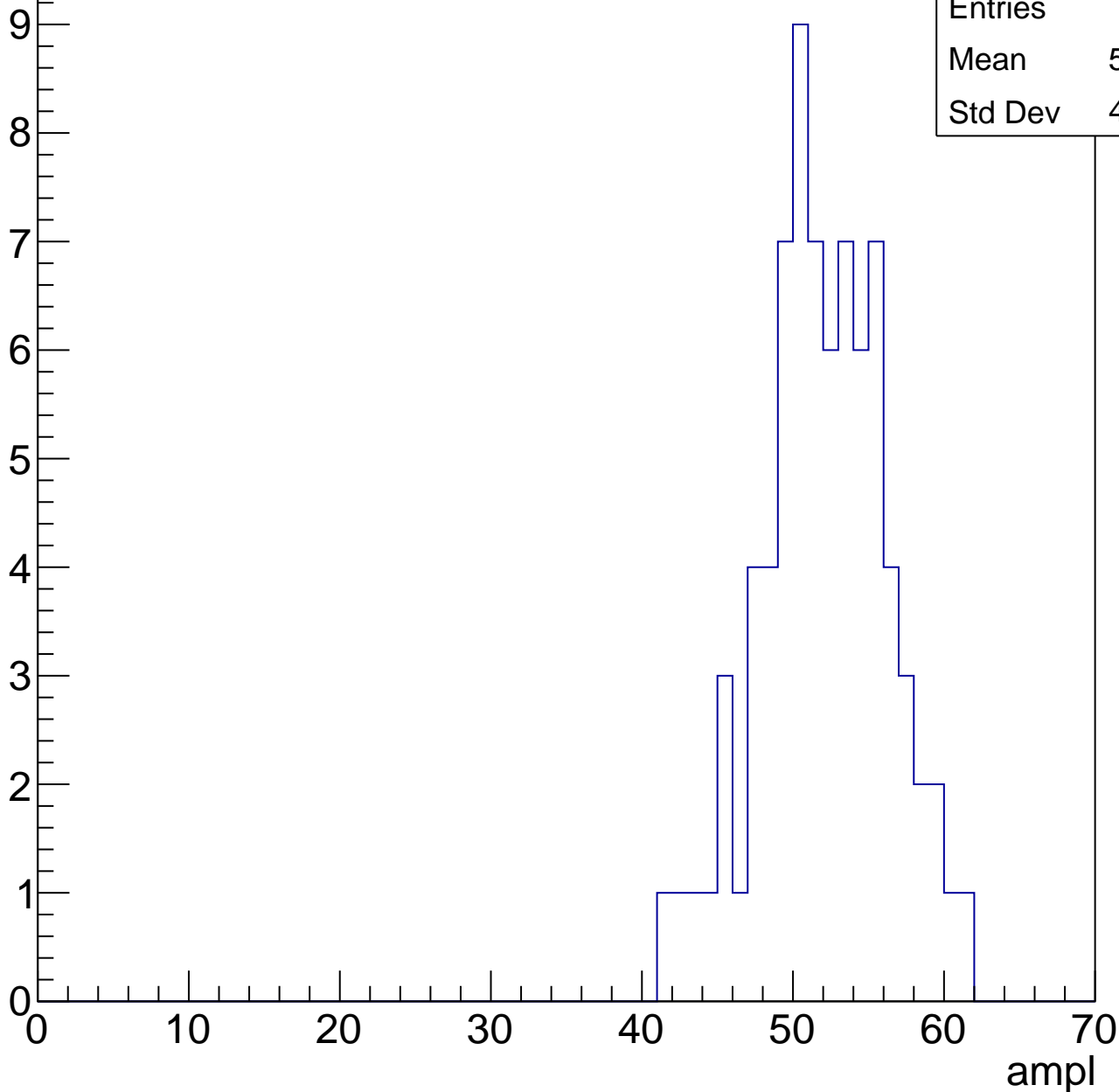


# B1L101S, U22-ch69, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

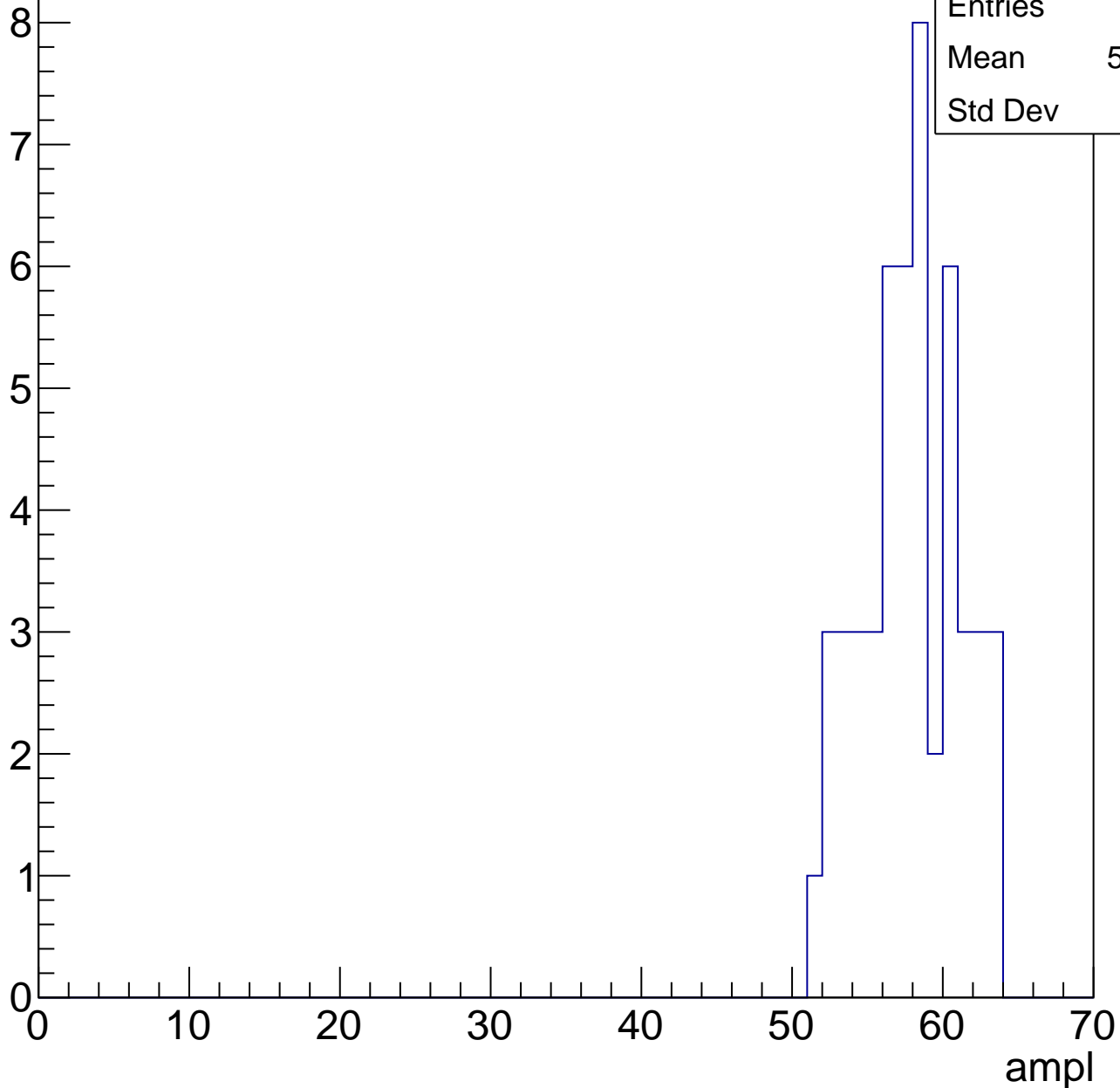
Entries	78
Mean	51.58
Std Dev	4.165



# B1L101S, U22-ch69, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

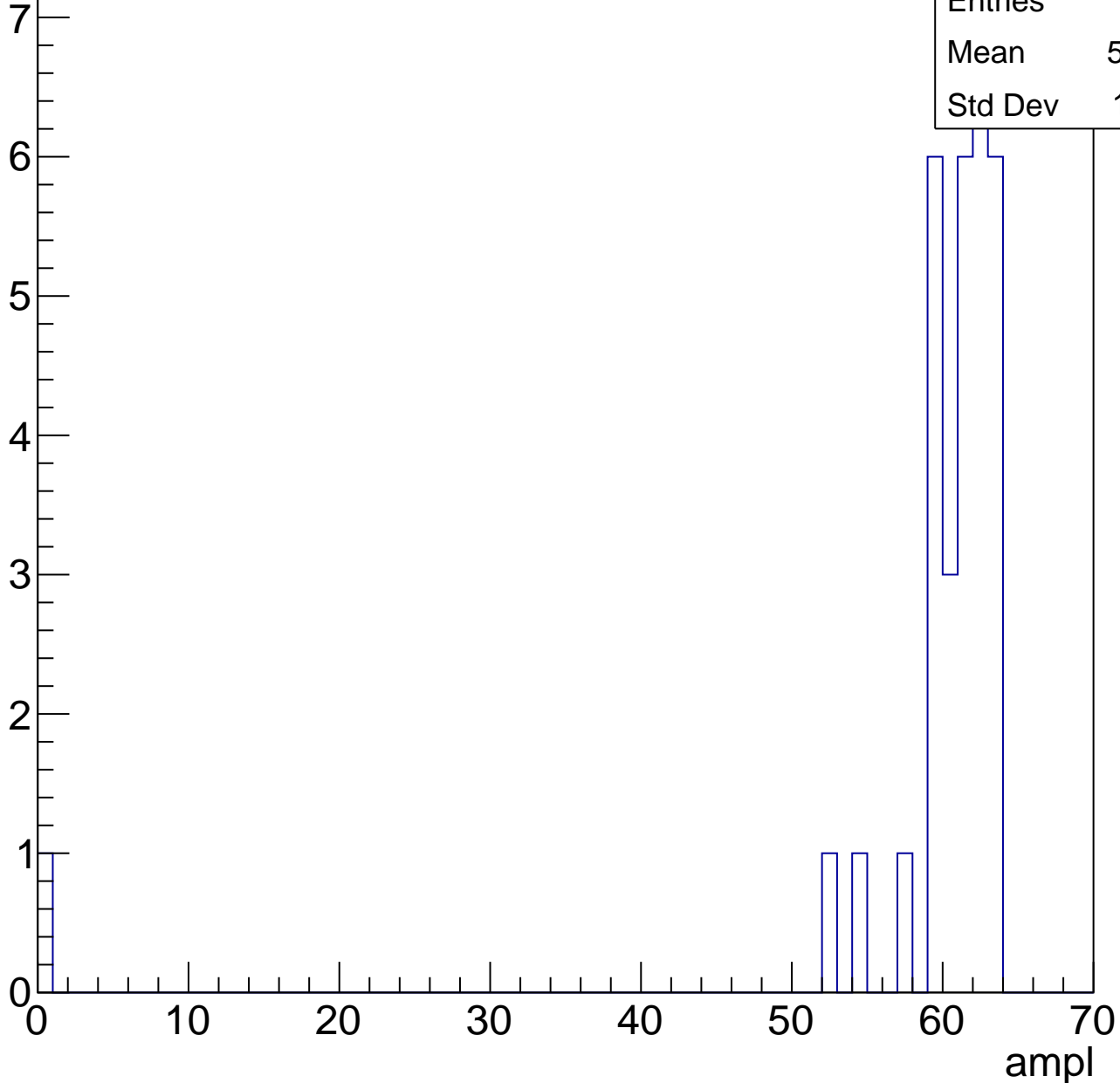


# B1L101S, U22-ch69, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	32
Mean	58.59
Std Dev	10.81



# B1L101S, U22-ch69, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

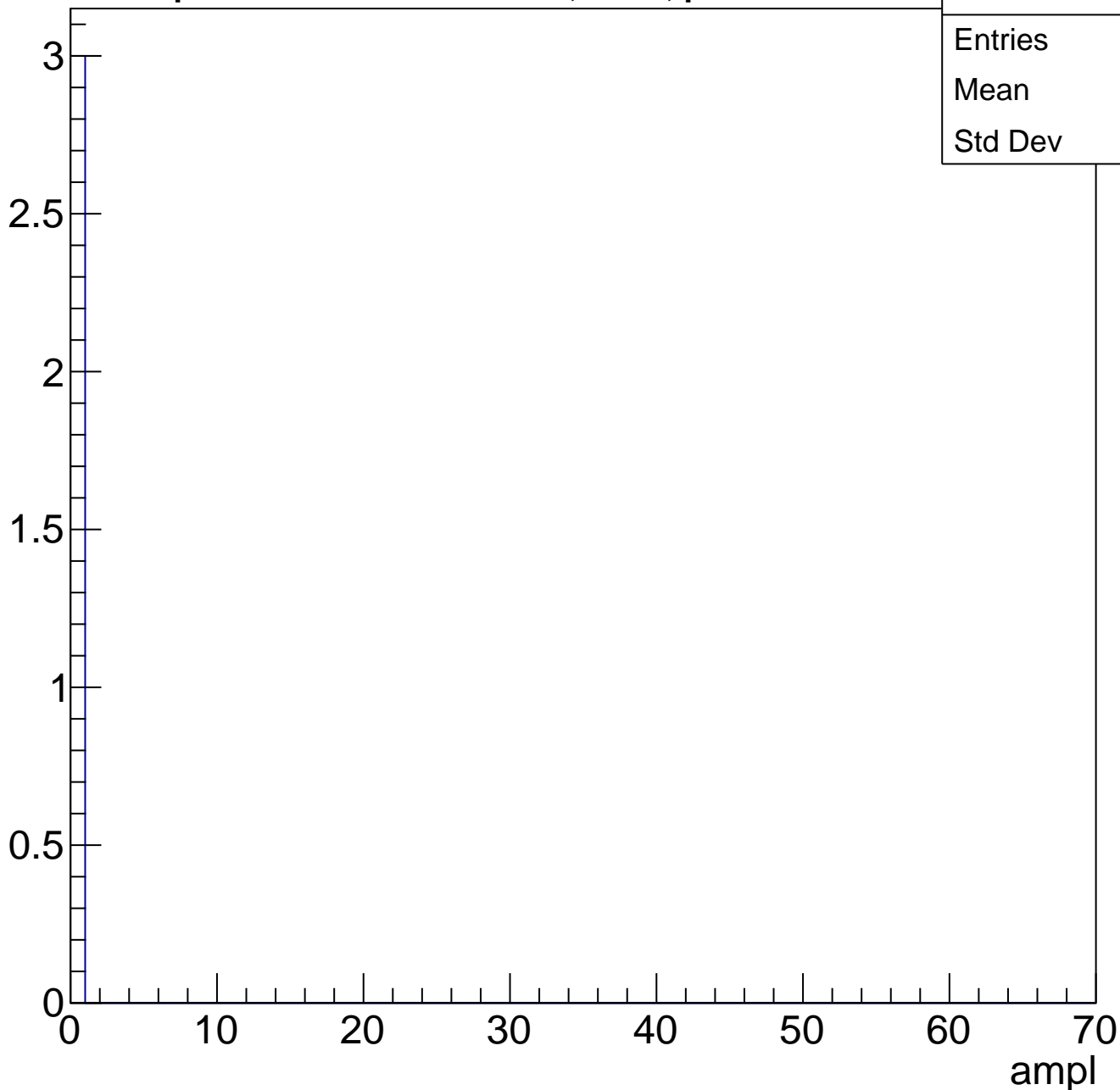




# B1L101S, U22-ch69, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	3
Mean	0
Std Dev	0

# B1L101S, U22-ch70, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	84
Mean	29.43
Std Dev	3.793

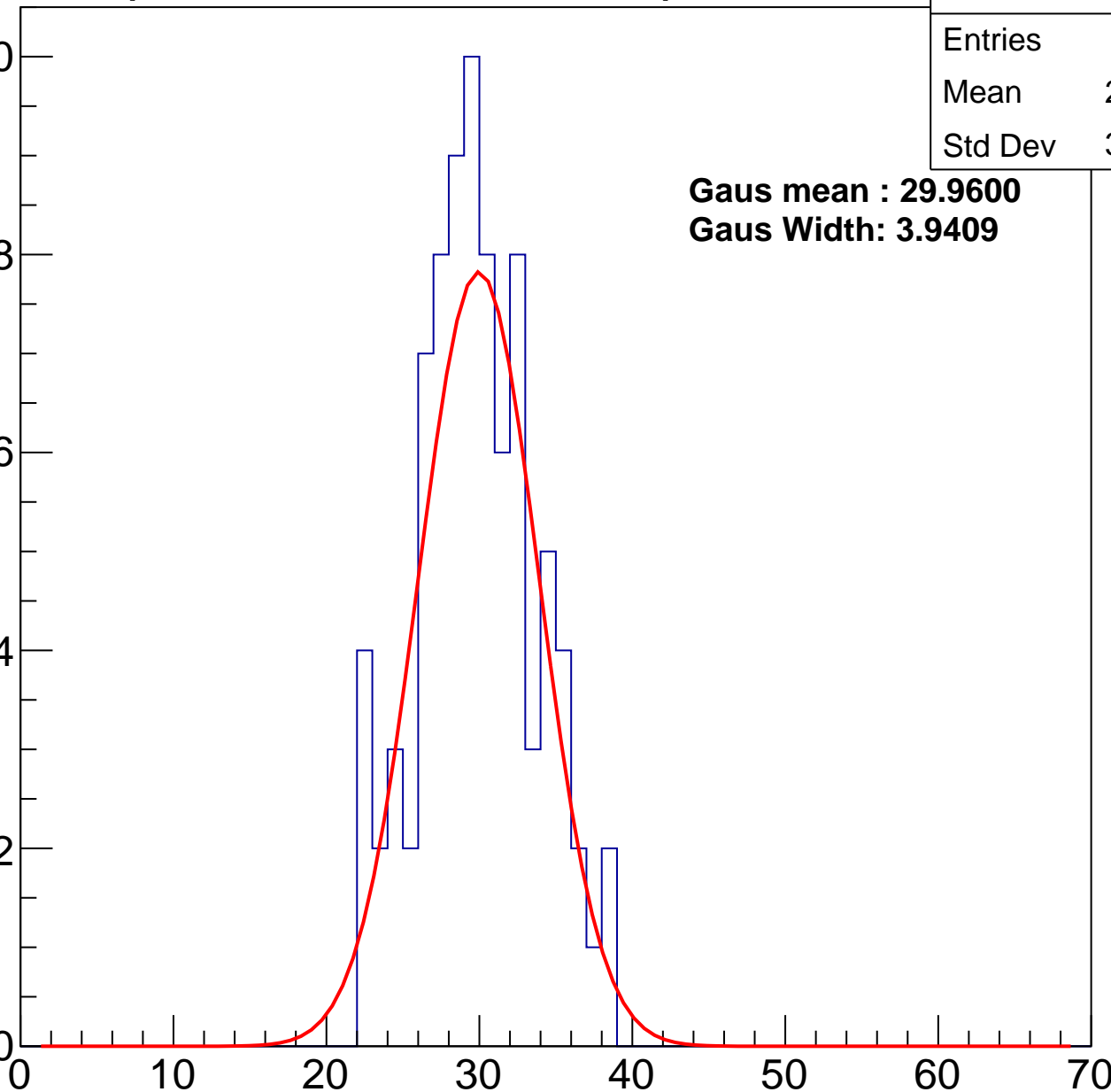
**Gaus mean : 29.9600**

**Gaus Width: 3.9409**

Entry

10  
8  
6  
4  
2  
0

ampl



# B1L101S, U22-ch70, adc1

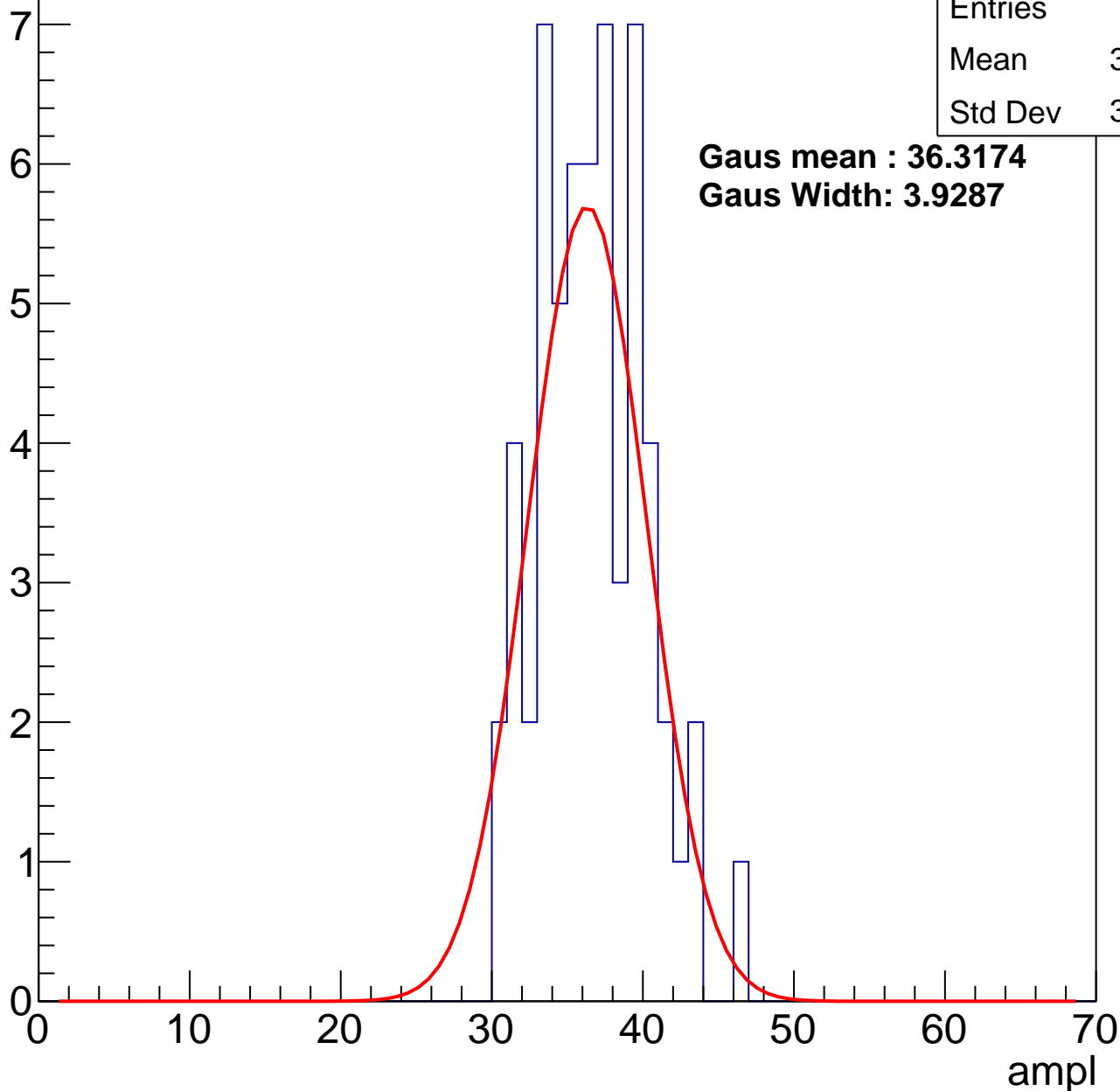
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	59
Mean	36.22
Std Dev	3.494

**Gaus mean : 36.3174**

**Gaus Width: 3.9287**



# B1L101S, U22-ch70, adc2

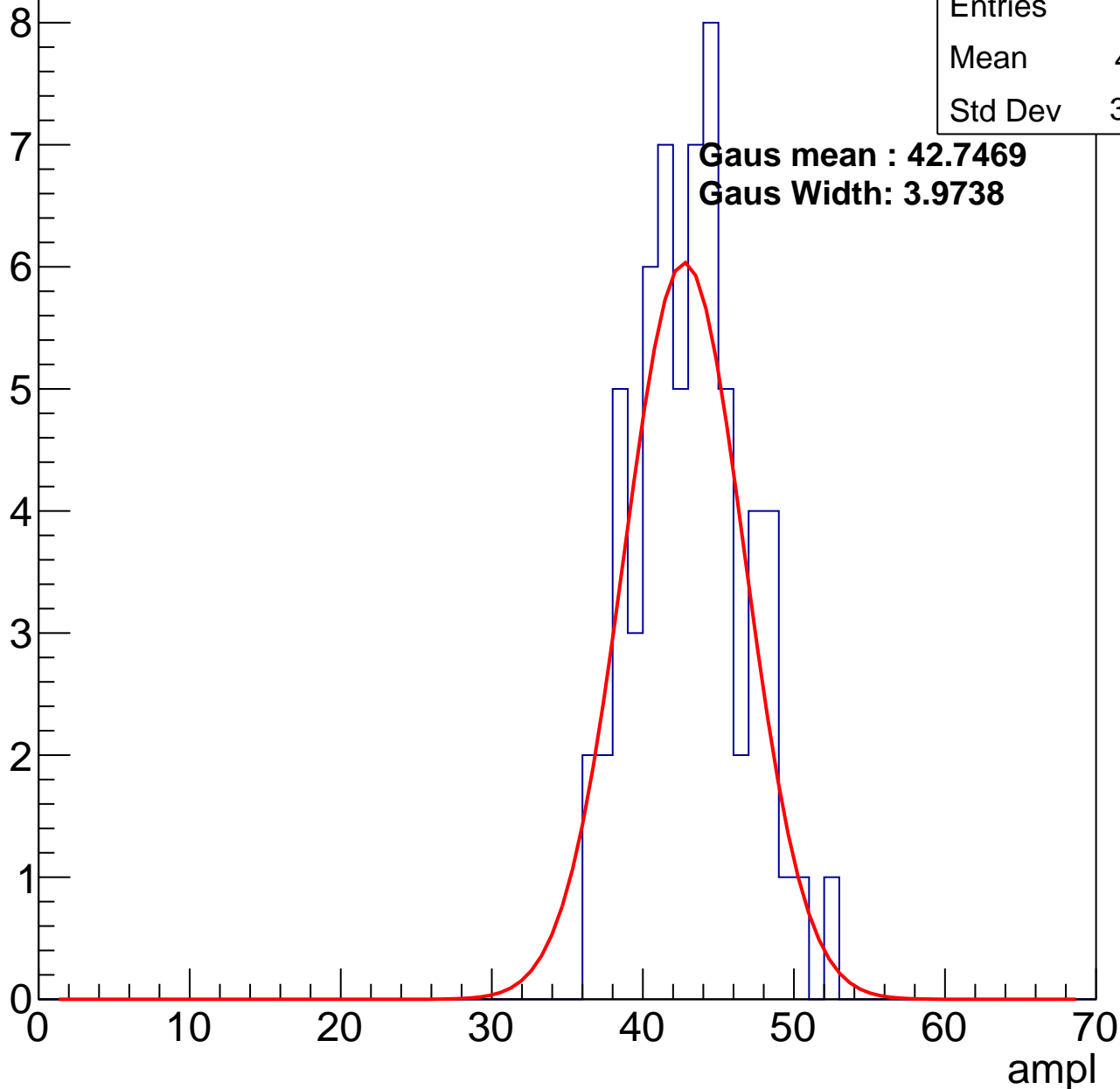
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	42.71
Std Dev	3.565

**Gaus mean : 42.7469**

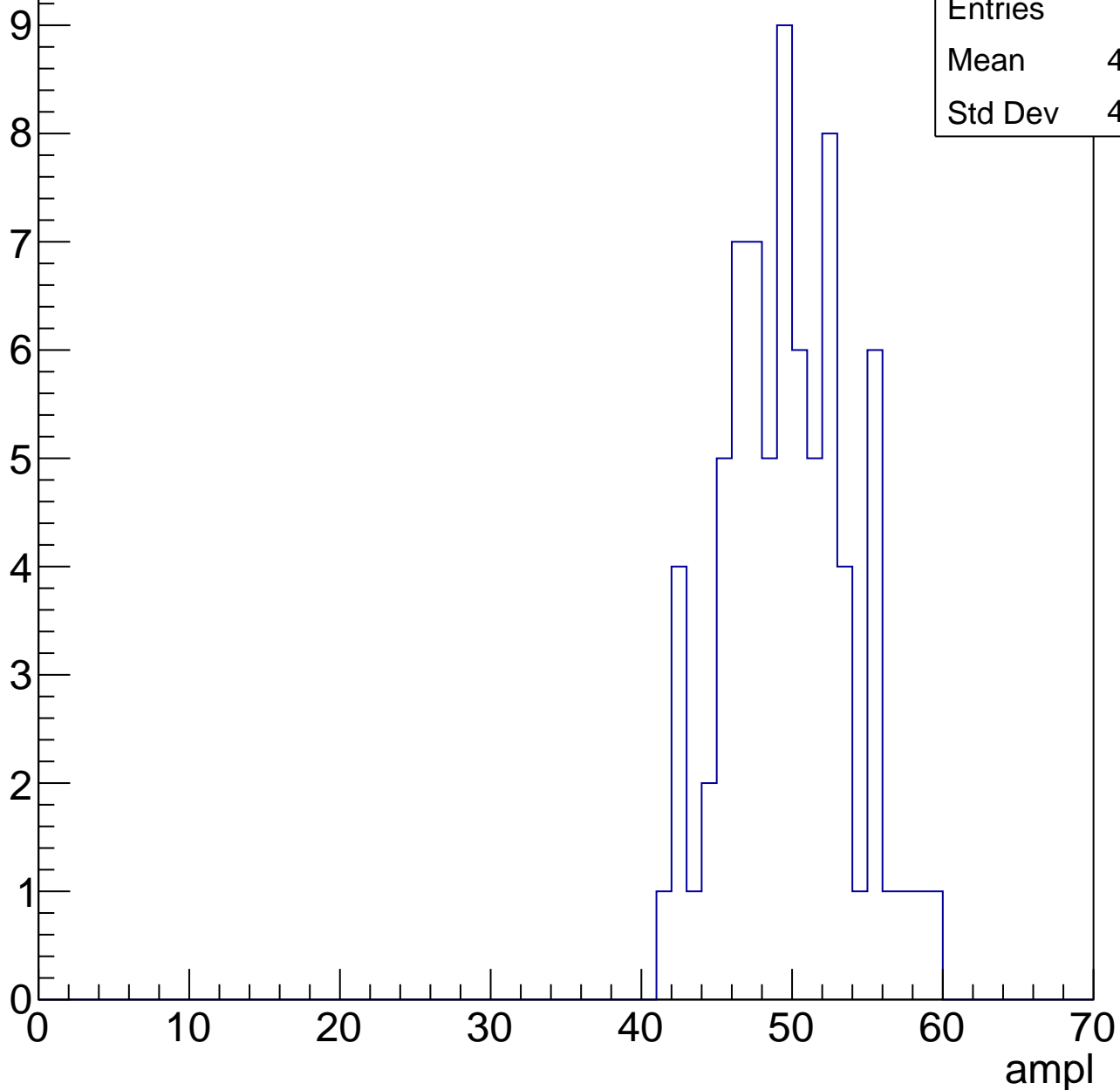
**Gaus Width: 3.9738**



# B1L101S, U22-ch70, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



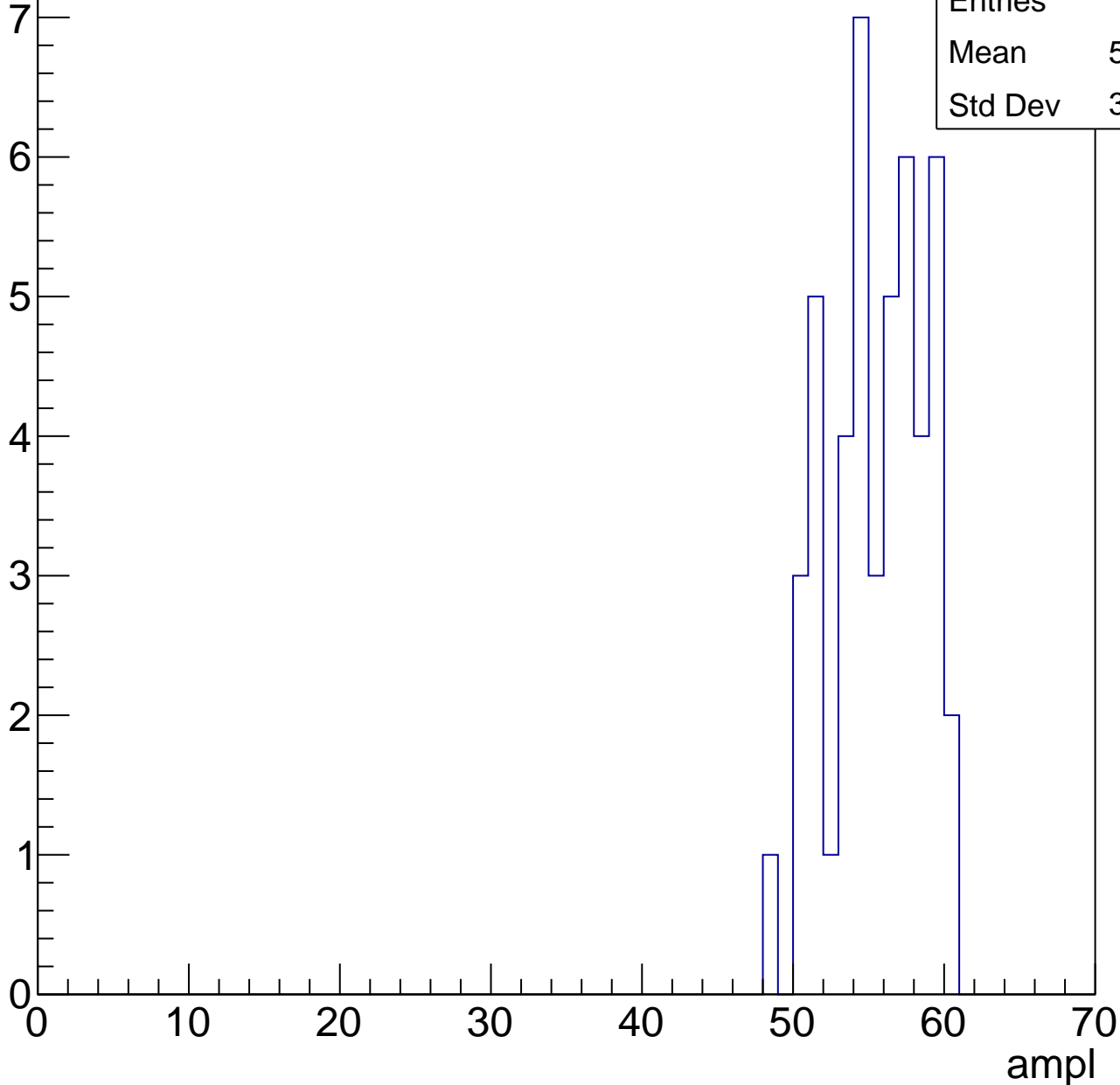
Entries	75
Mean	49.25
Std Dev	4.024

# B1L101S, U22-ch70, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	47
Mean	55.06
Std Dev	3.083



# B1L101S, U22-ch70, adc5

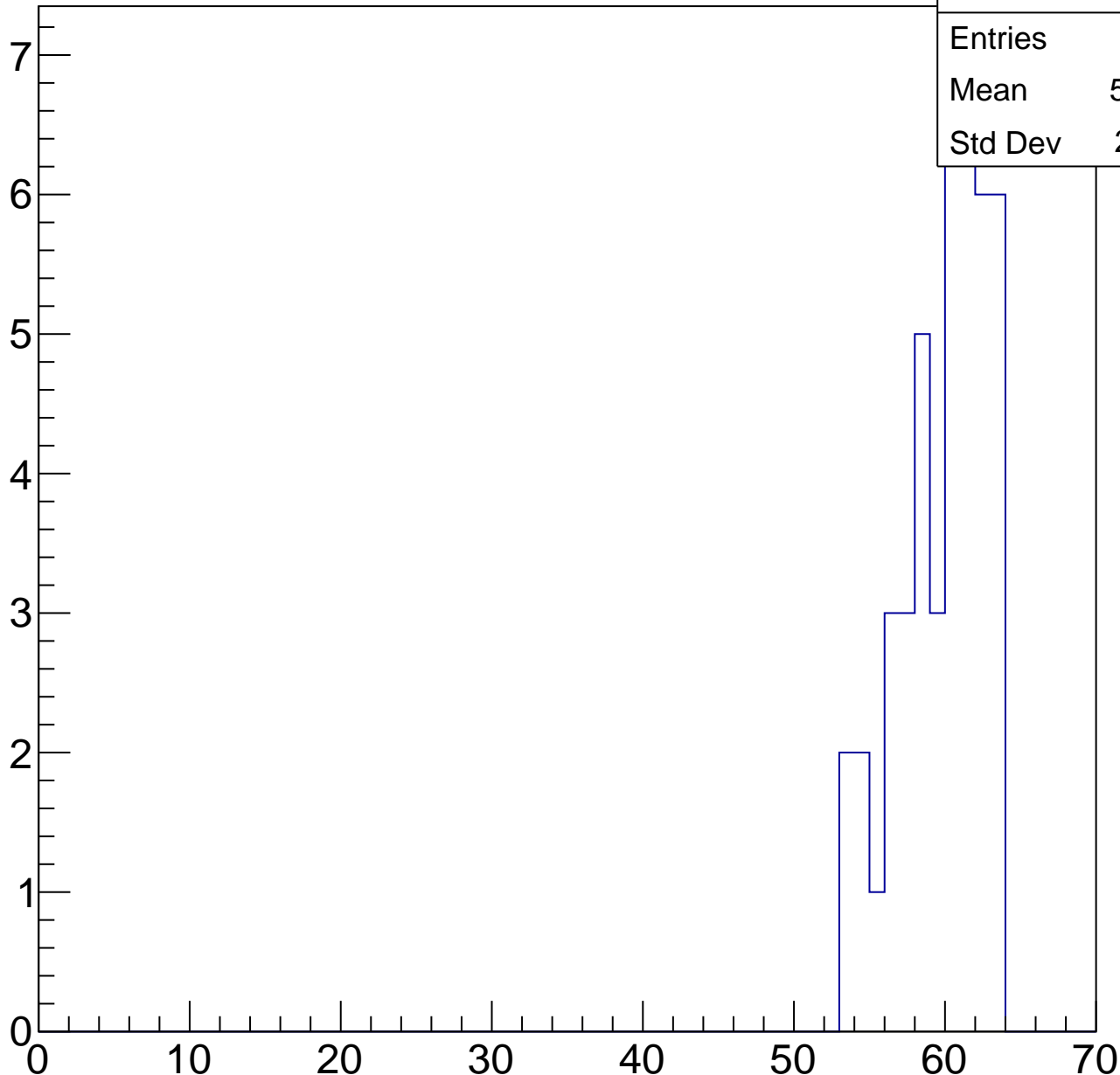
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

7  
6  
5  
4  
3  
2  
1  
0

Entries	45
Mean	59.38
Std Dev	2.831

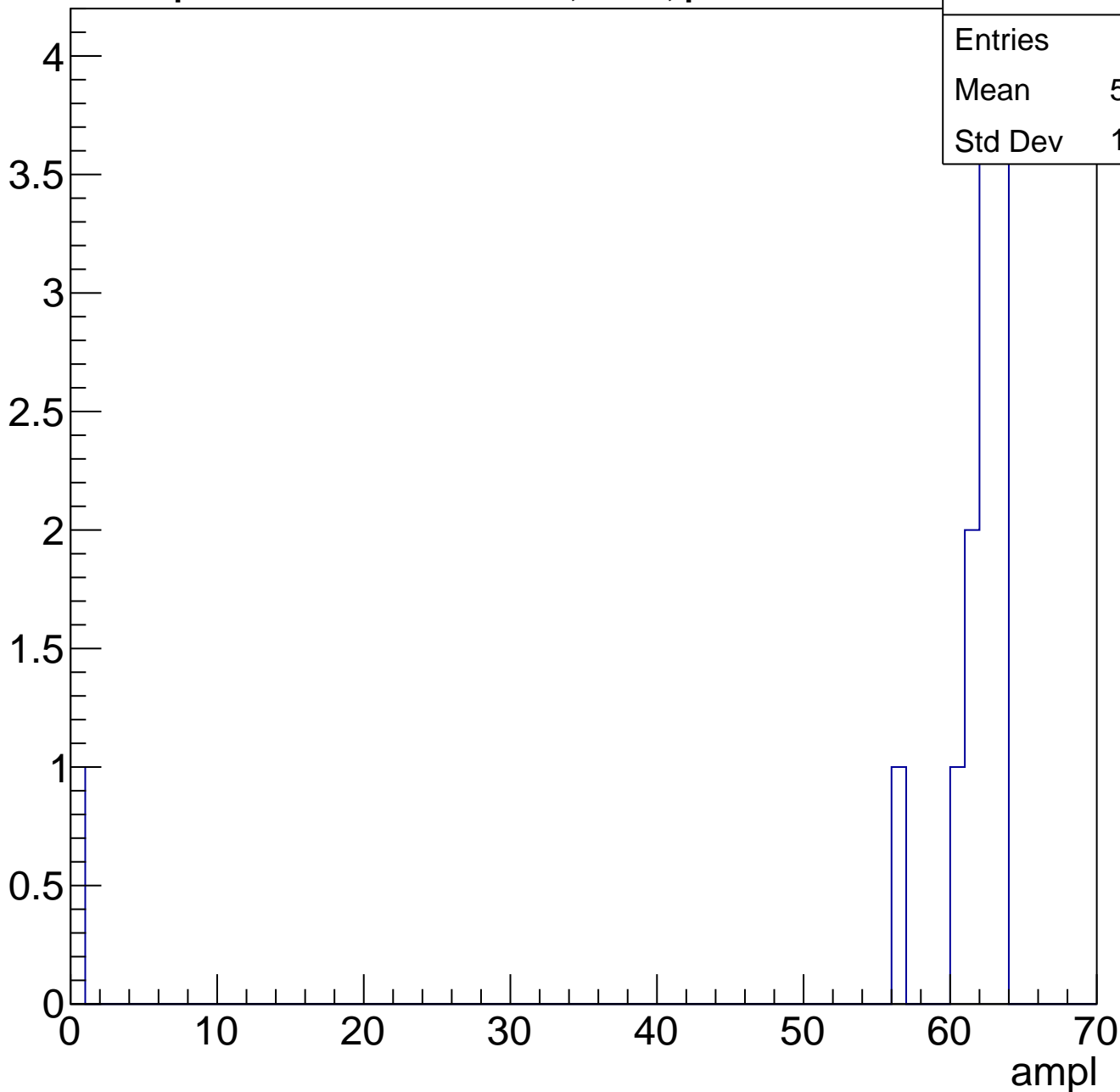
ampl



# B1L101S, U22-ch70, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

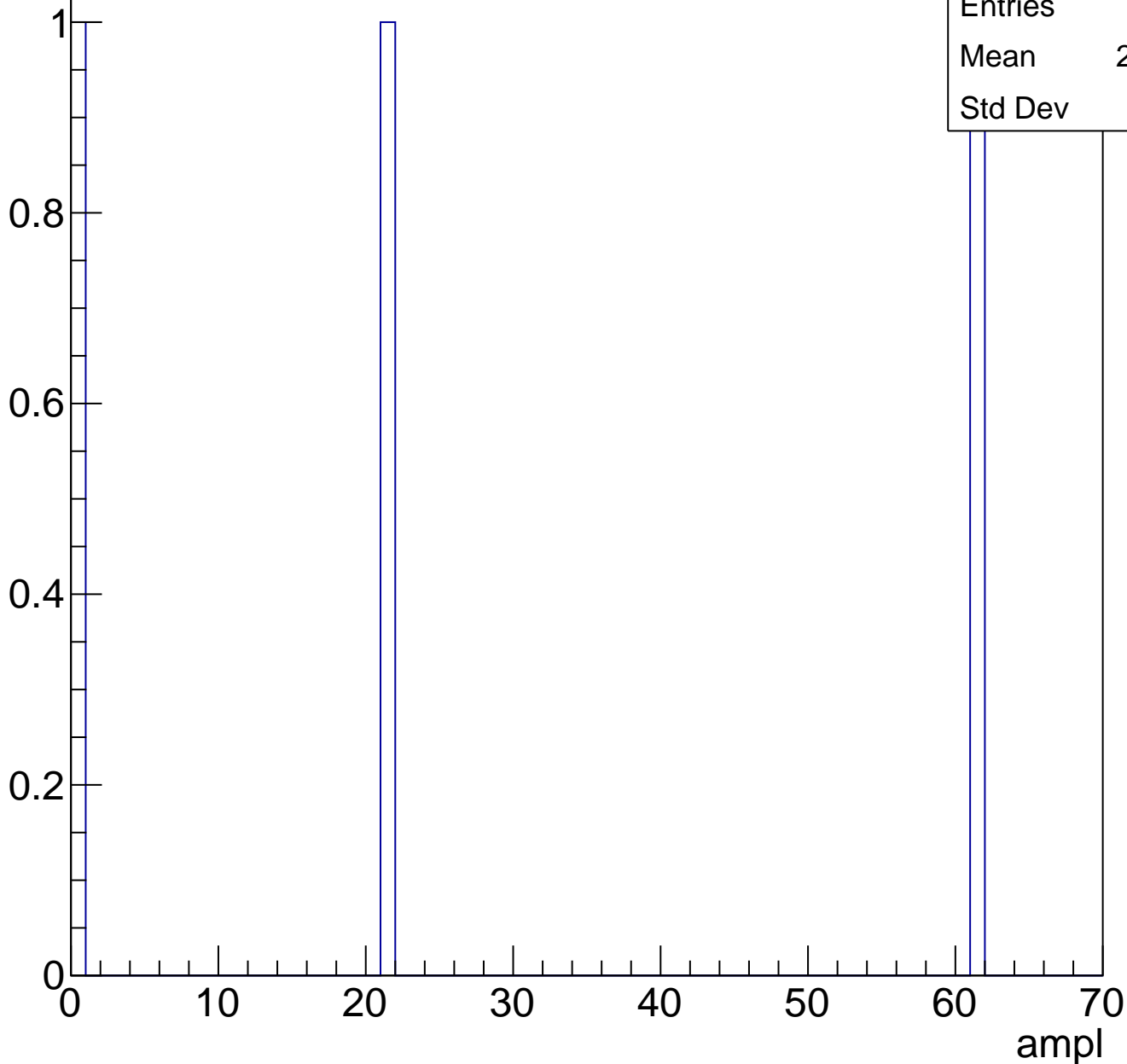




# B1L101S, U22-ch70, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U22-ch71, adc0

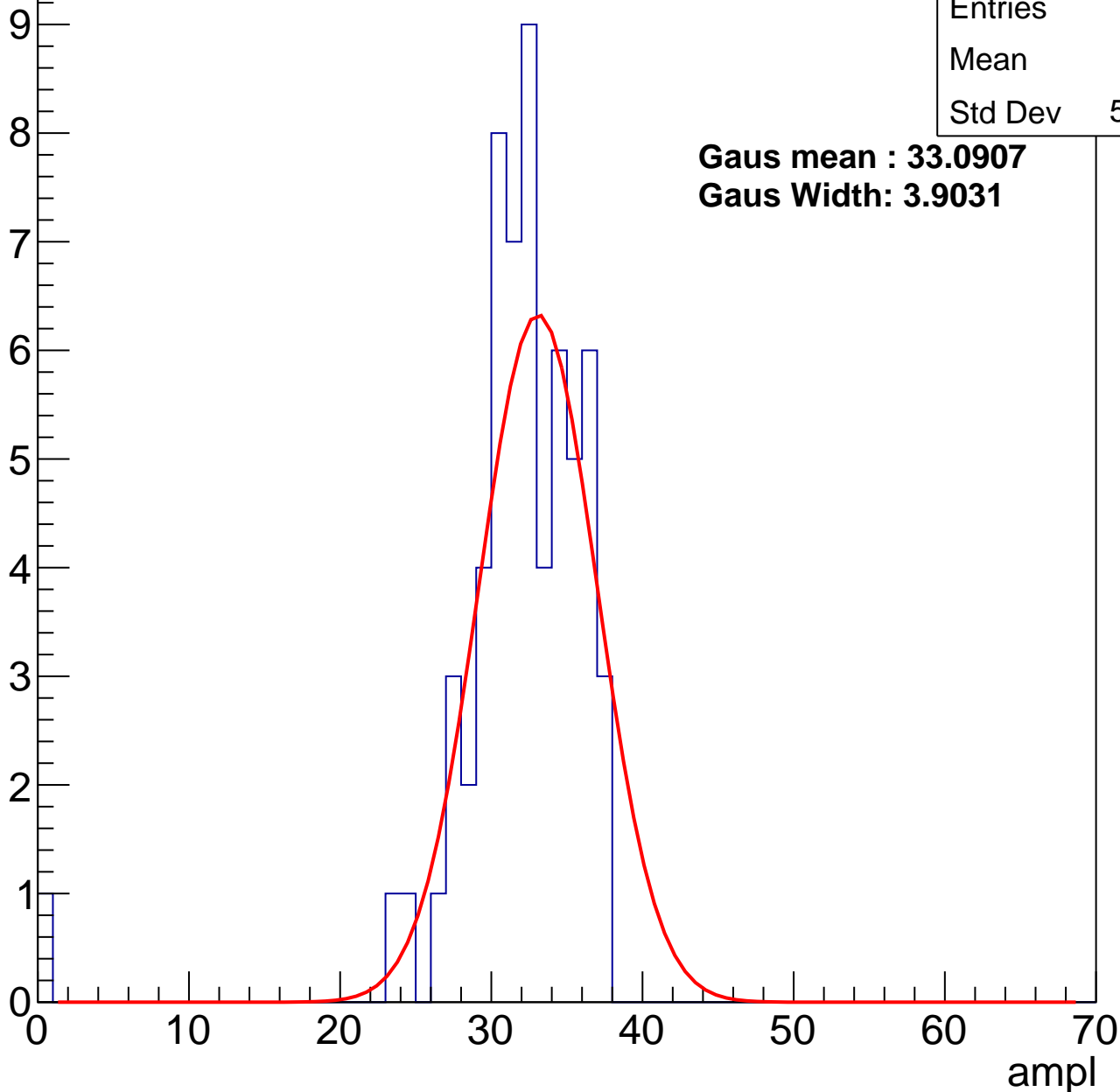
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	31.3
Std Dev	5.123

**Gaus mean : 33.0907**

**Gaus Width: 3.9031**



# B1L101S, U22-ch71, adc1

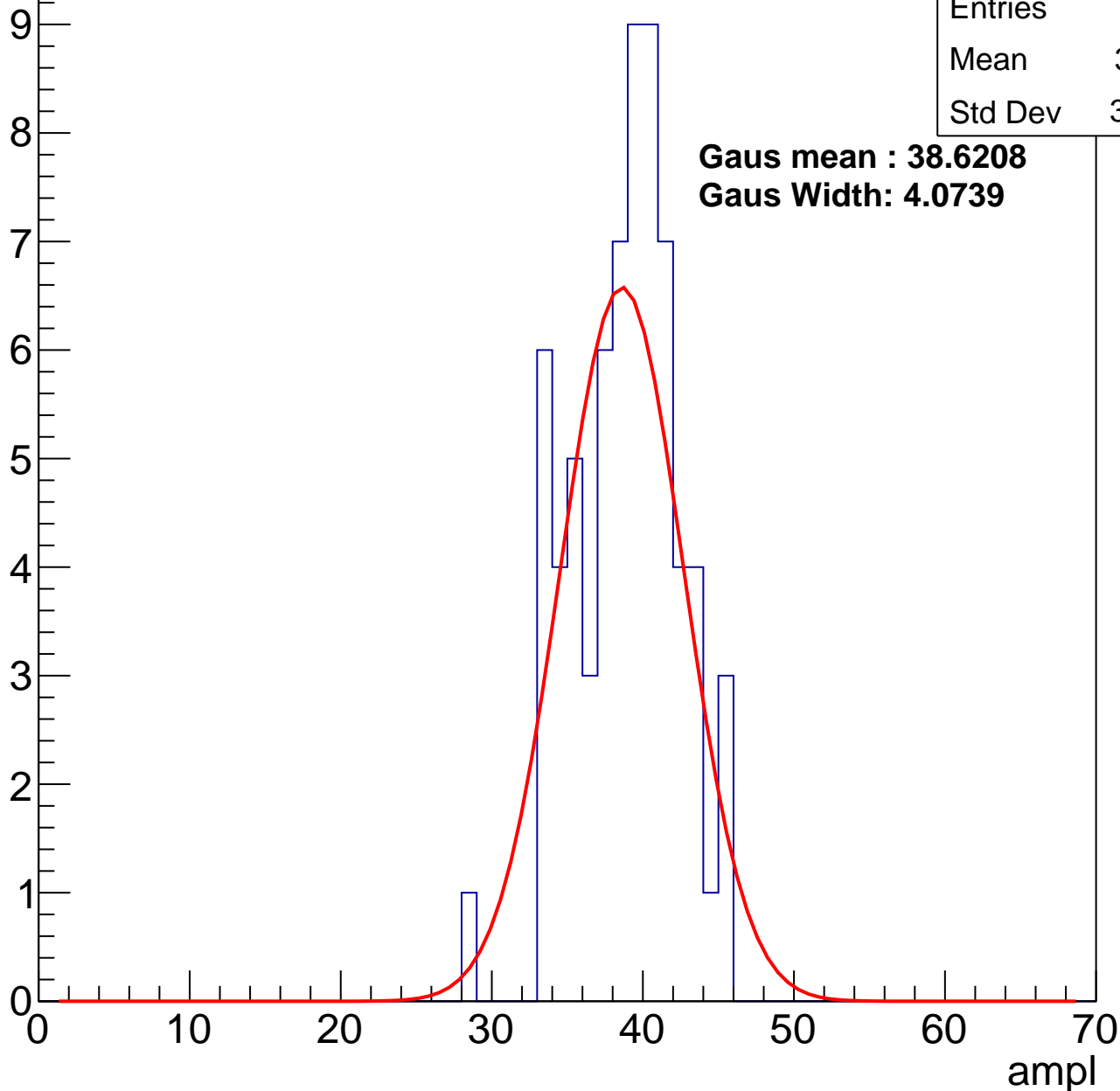
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	38.41
Std Dev	3.449

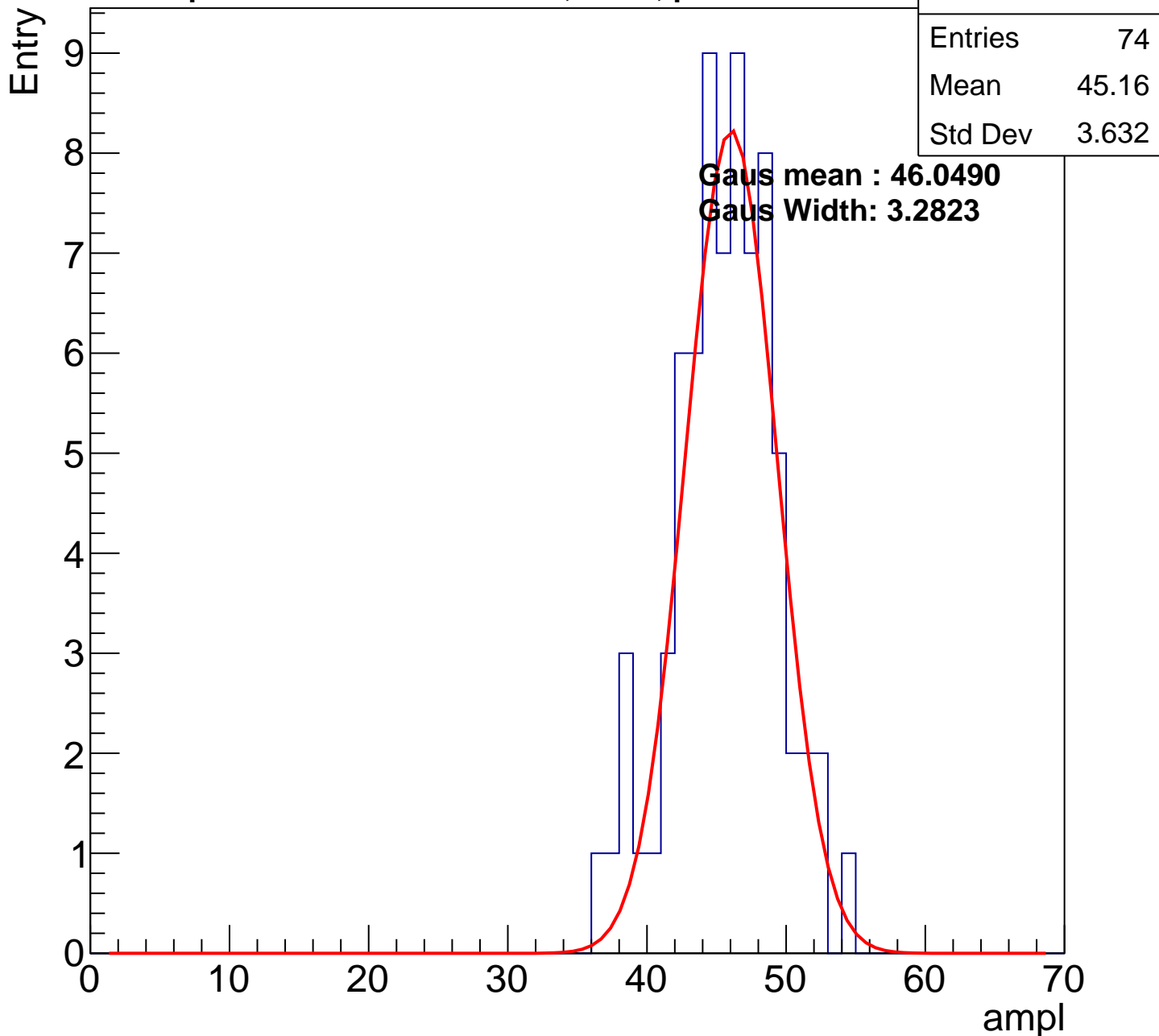
**Gaus mean : 38.6208**

**Gaus Width: 4.0739**



# B1L101S, U22-ch71, adc2

calib\_packv5\_042523\_0143.root, FC#0, port D2

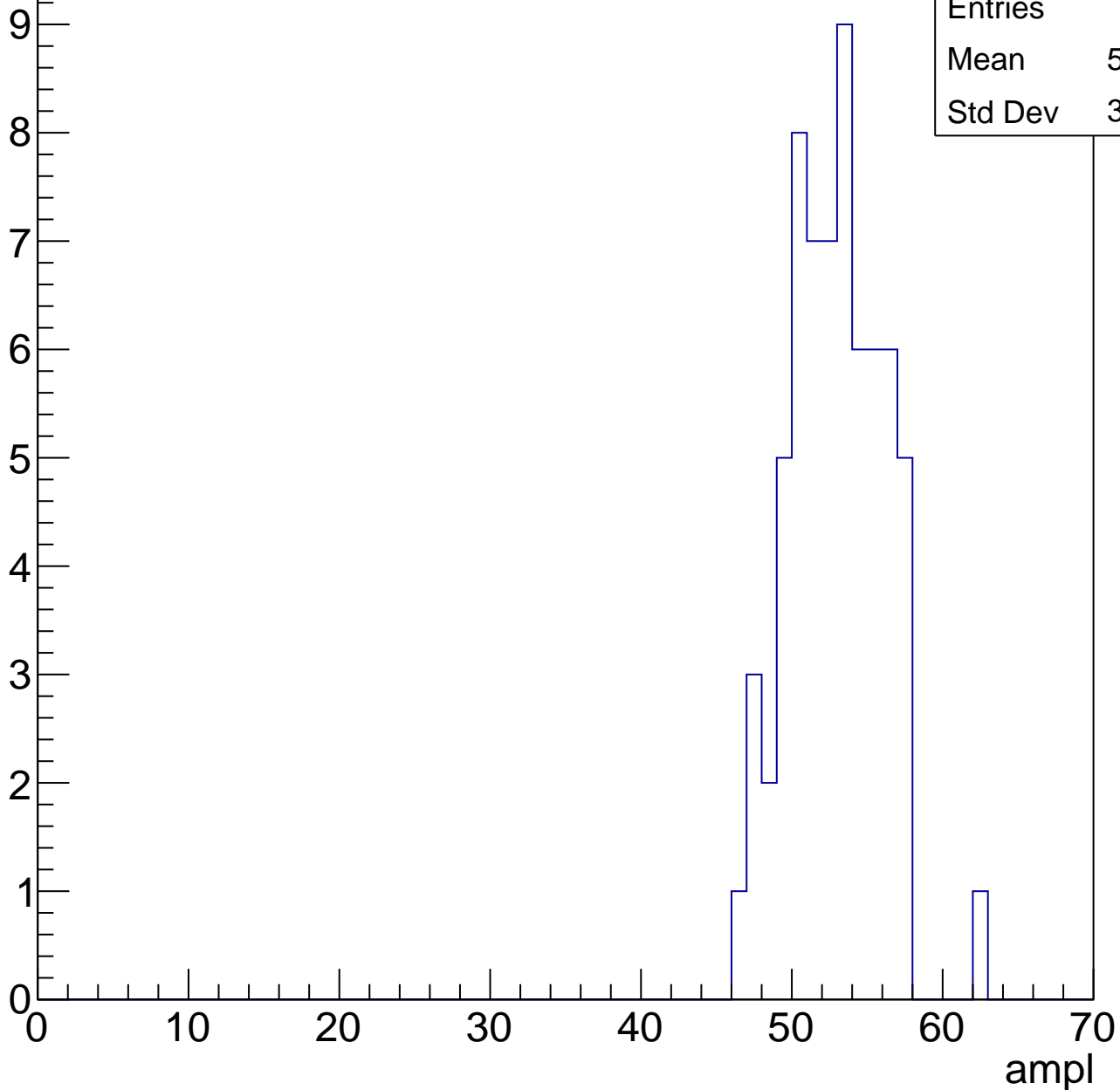


# B1L101S, U22-ch71, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	66
Mean	52.47
Std Dev	3.066

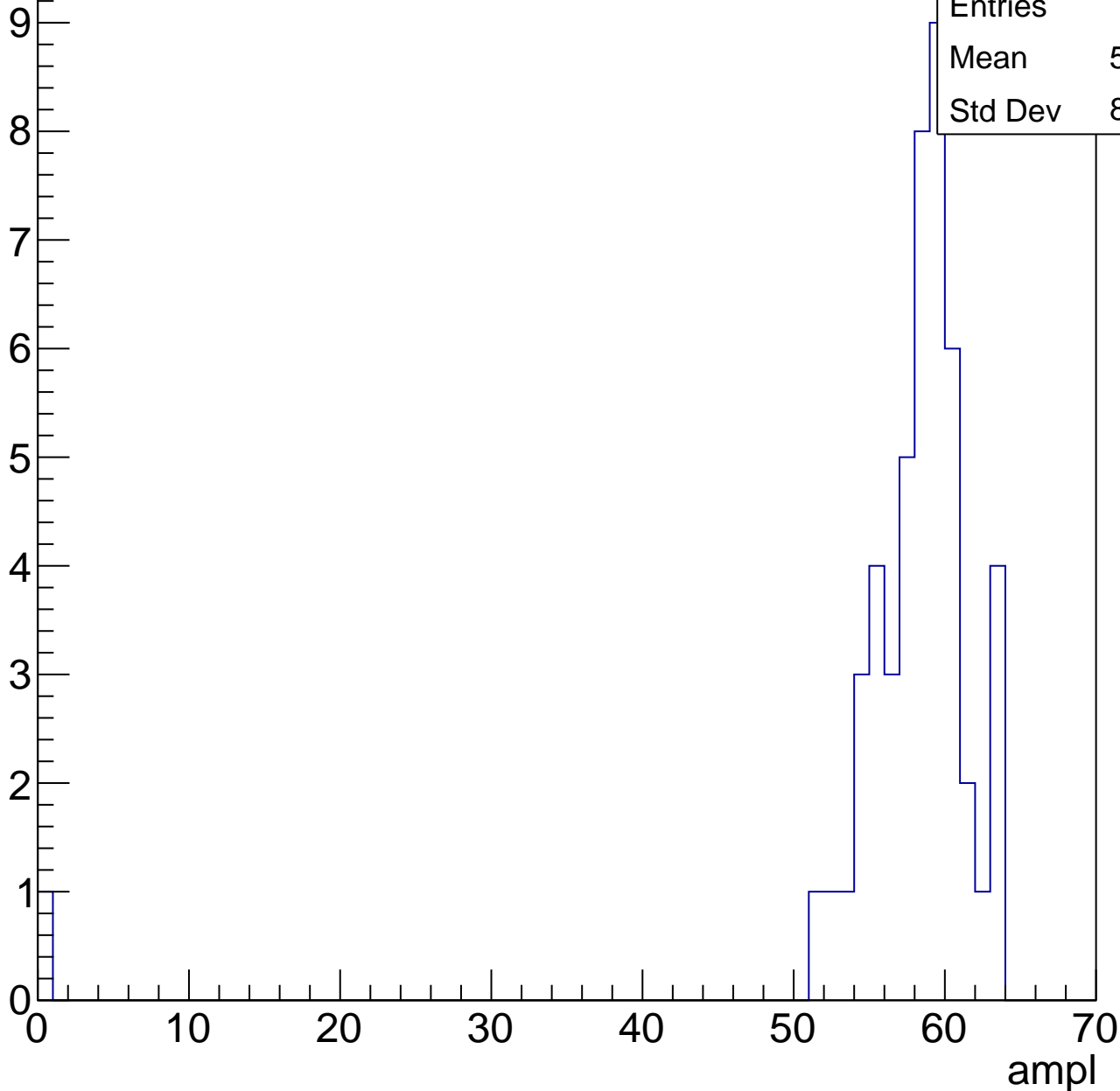


# B1L101S, U22-ch71, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	49
Mean	56.78
Std Dev	8.653

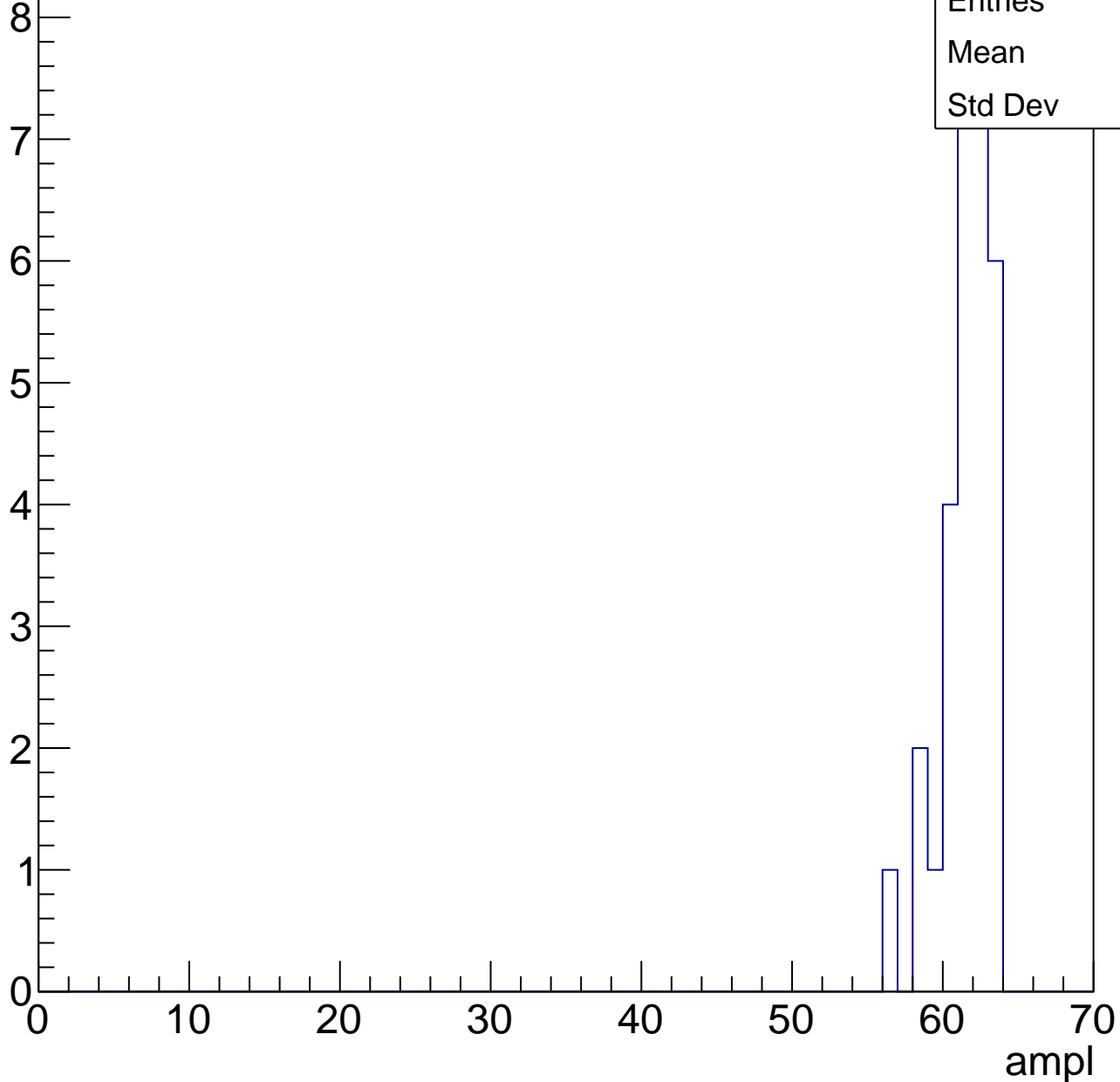


# B1L101S, U22-ch71, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	30
Mean	61.1
Std Dev	1.66



# B1L101S, U22-ch71, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U22-ch71, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U22-ch72, adc0

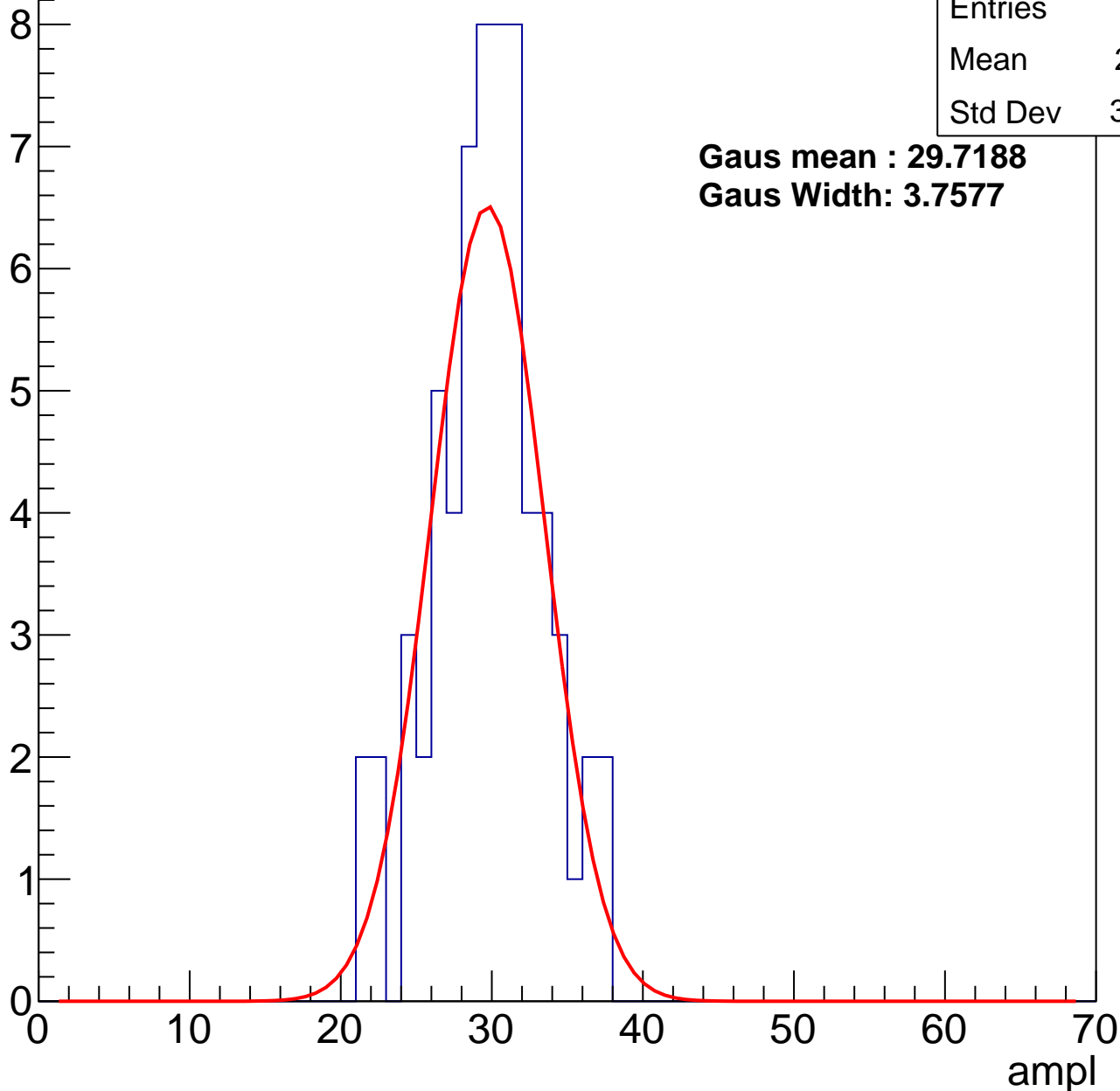
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	29.31
Std Dev	3.662

**Gaus mean : 29.7188**

**Gaus Width: 3.7577**



# B1L101S, U22-ch72, adc1

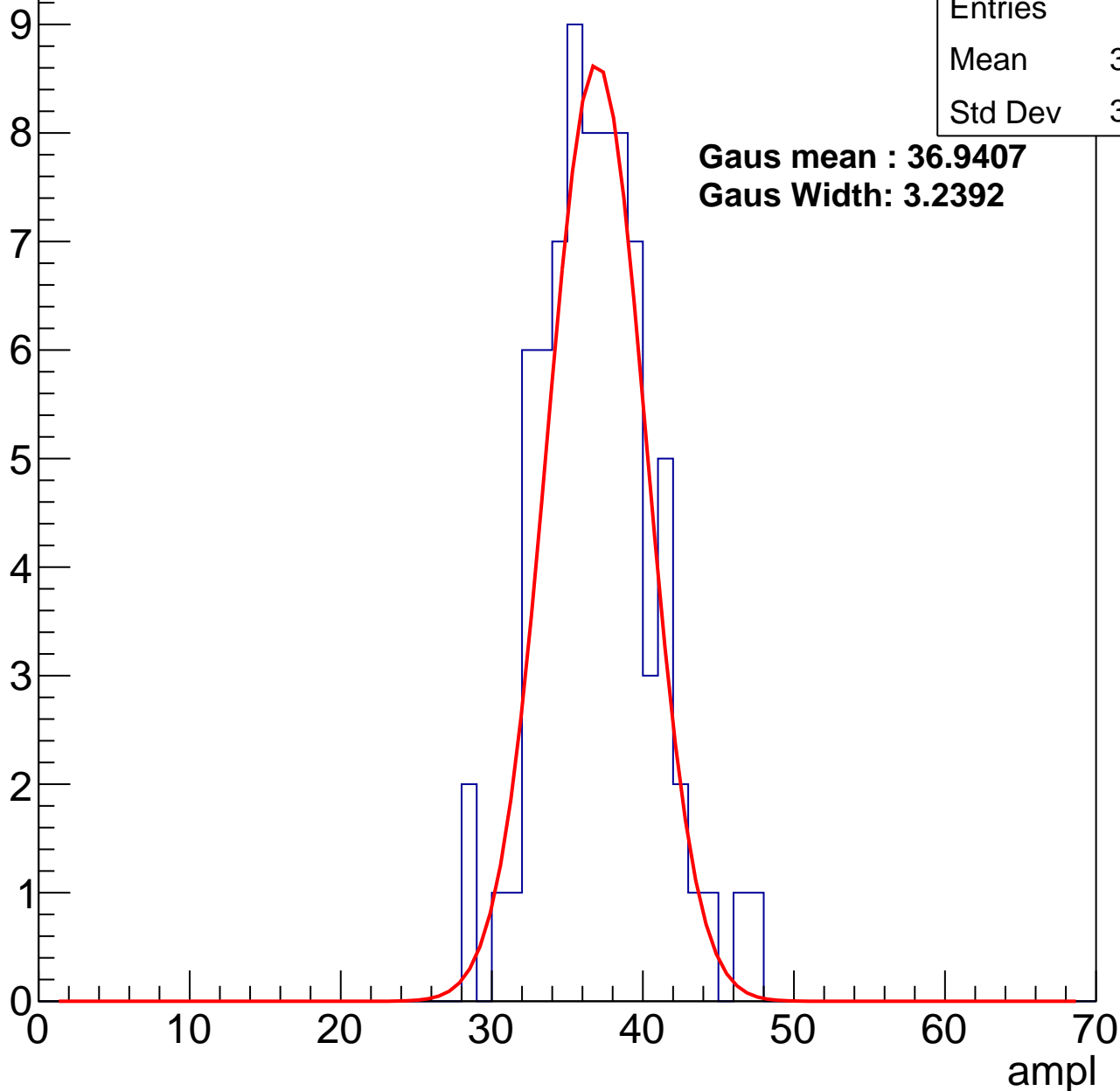
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	77
Mean	36.49
Std Dev	3.674

**Gaus mean : 36.9407**

**Gaus Width: 3.2392**



# B1L101S, U22-ch72, adc2

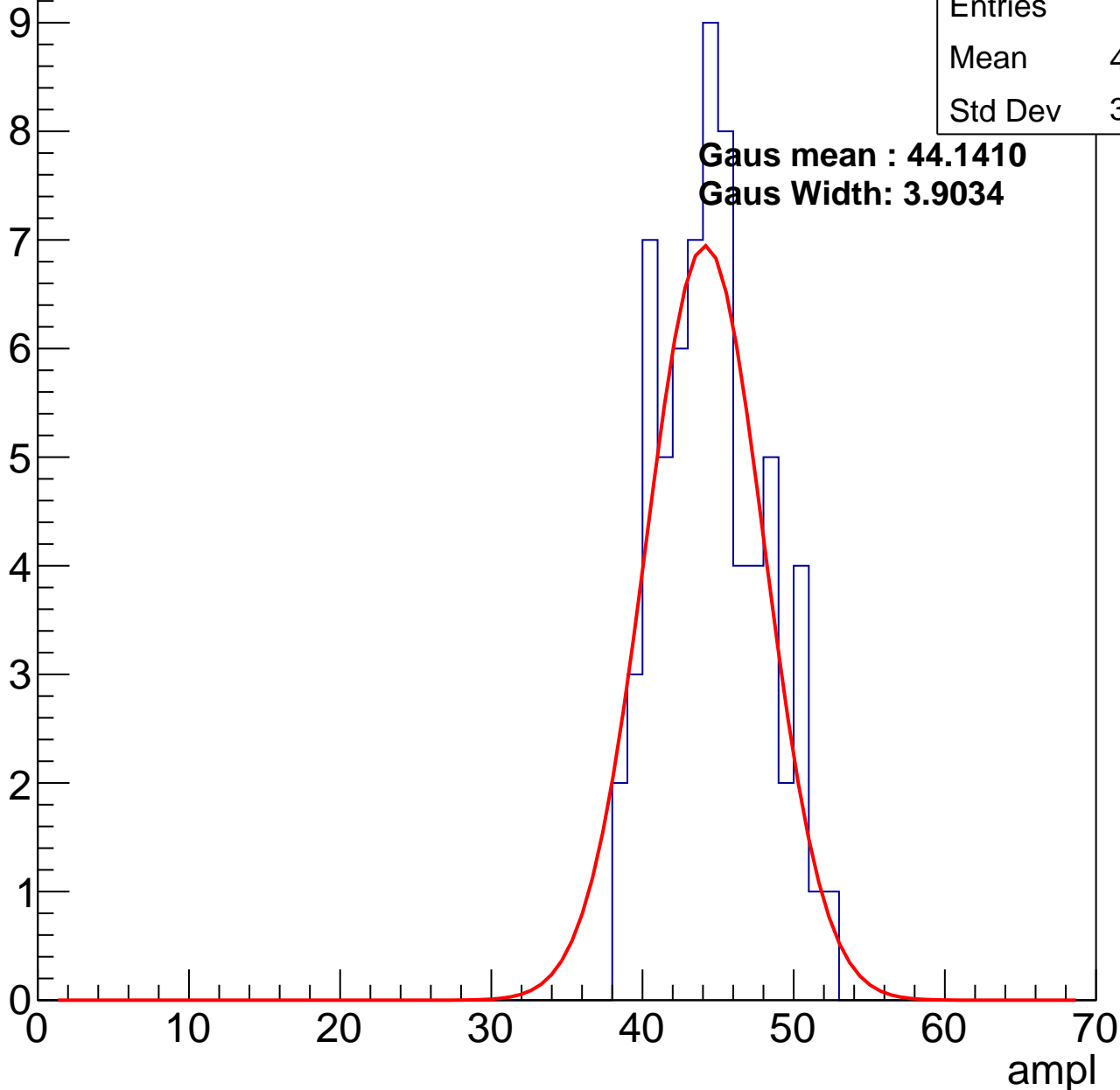
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	44.12
Std Dev	3.389

**Gaus mean : 44.1410**

**Gaus Width: 3.9034**

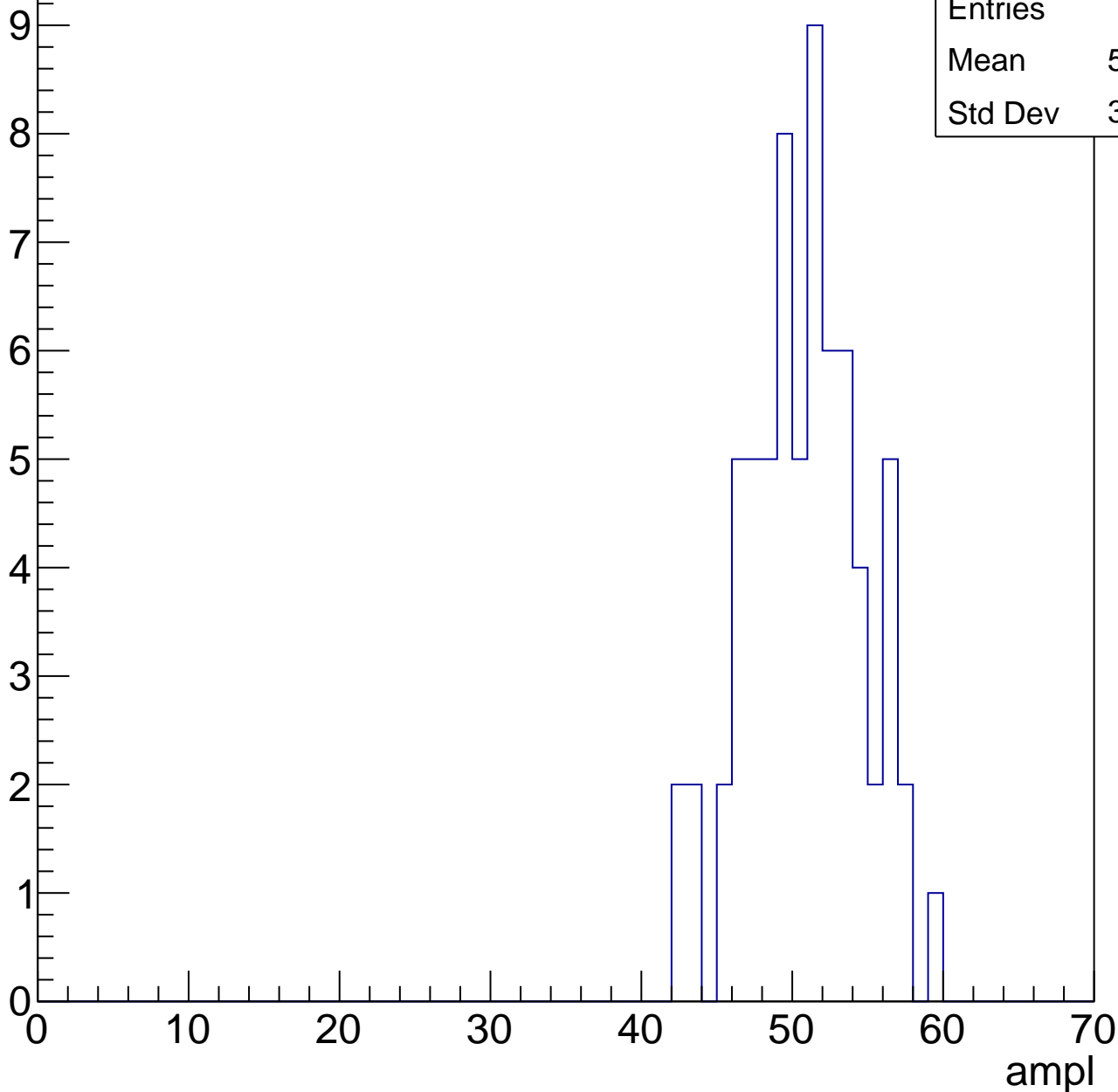


# B1L101S, U22-ch72, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	50.36
Std Dev	3.769



# B1L101S, U22-ch72, adc4

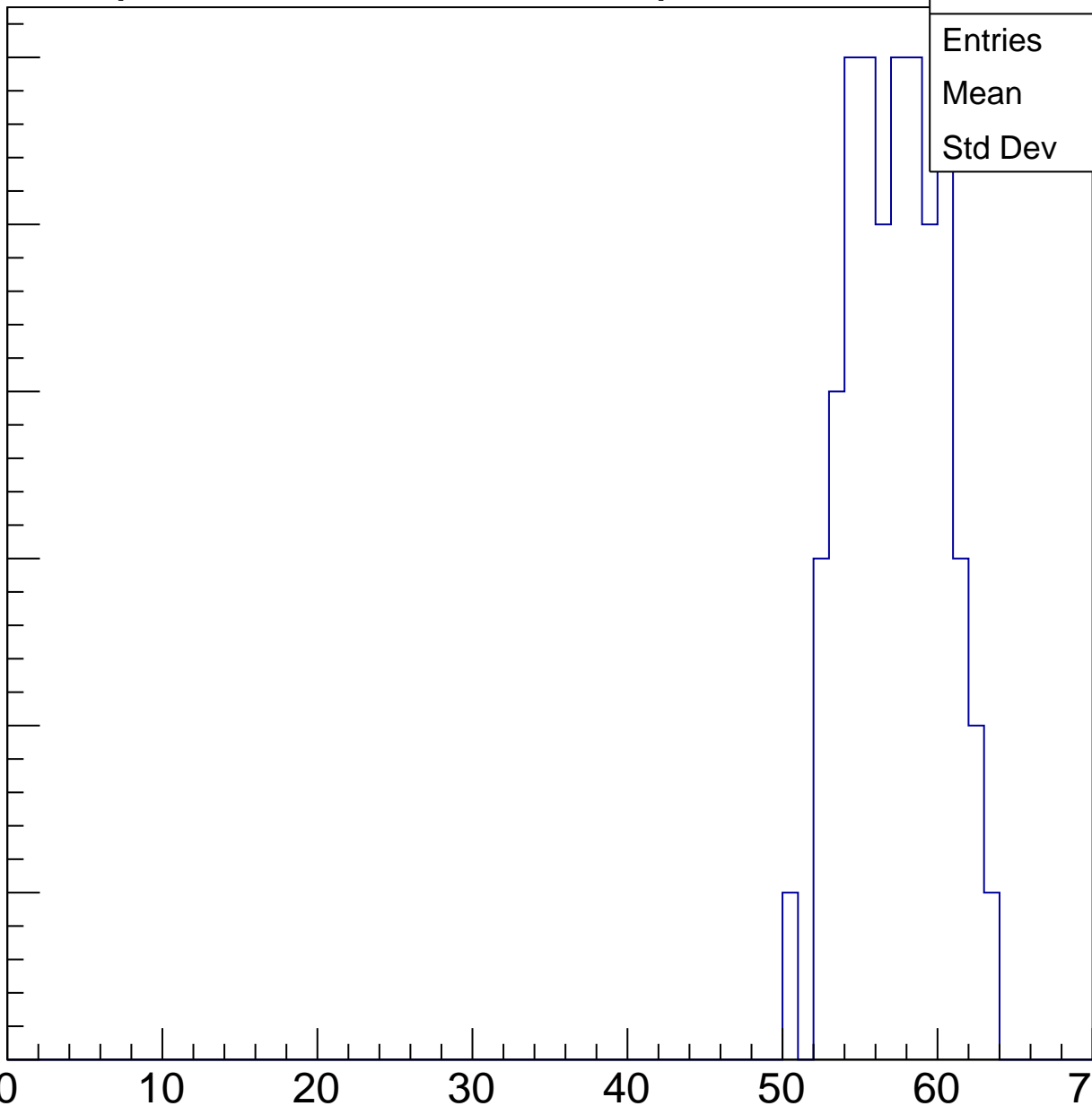
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

6  
5  
4  
3  
2  
1  
0

Entries	54
Mean	56.8
Std Dev	2.99

ampl

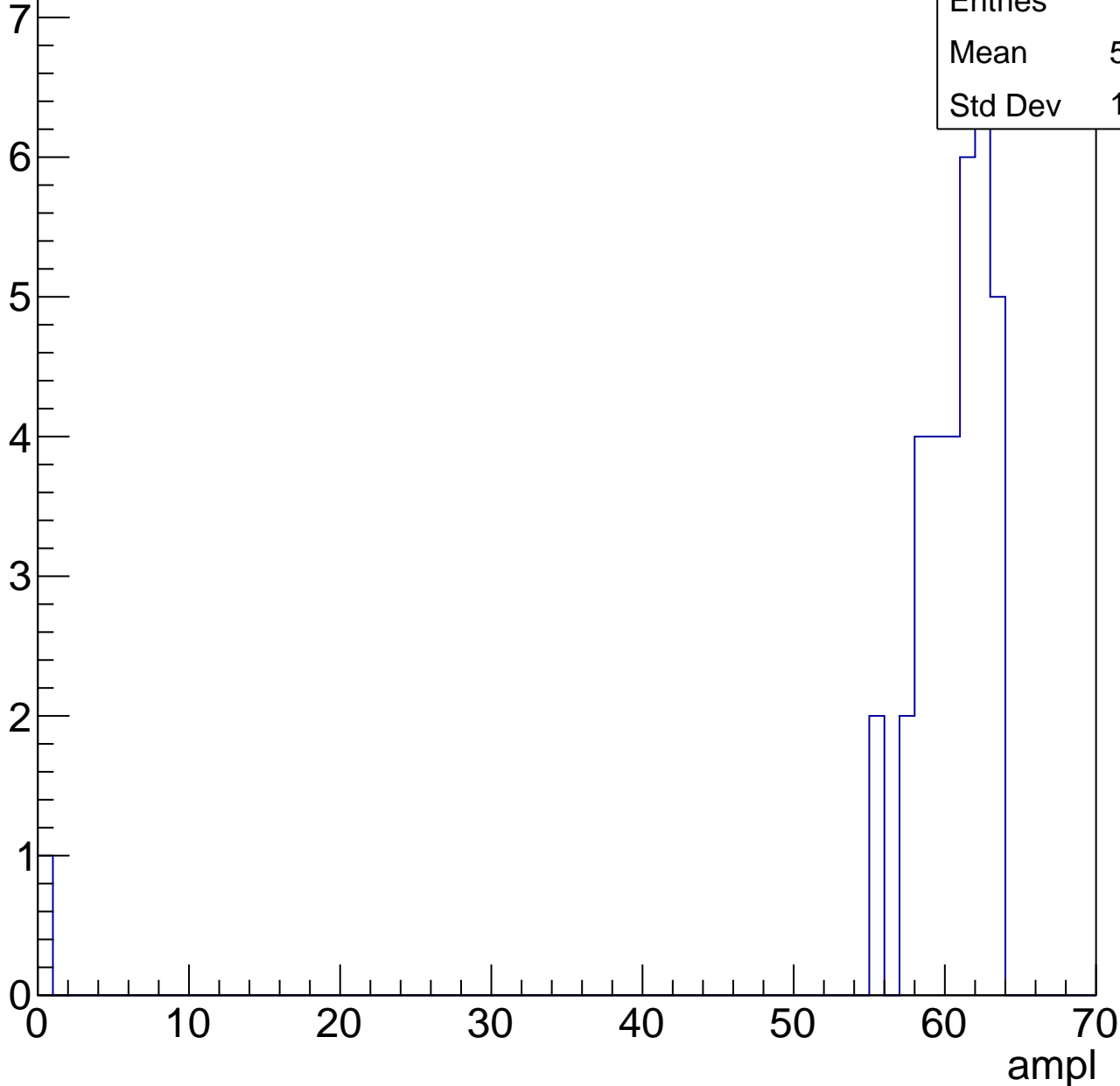


# B1L101S, U22-ch72, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	35
Mean	58.49
Std Dev	10.26



# B1L101S, U22-ch72, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	6
Mean	62.5
Std Dev	0.7638



# B1L101S, U22-ch72, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L101S, U22-ch73, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	70
Mean	30.29
Std Dev	3.352

**Gaus mean : 30.7572**

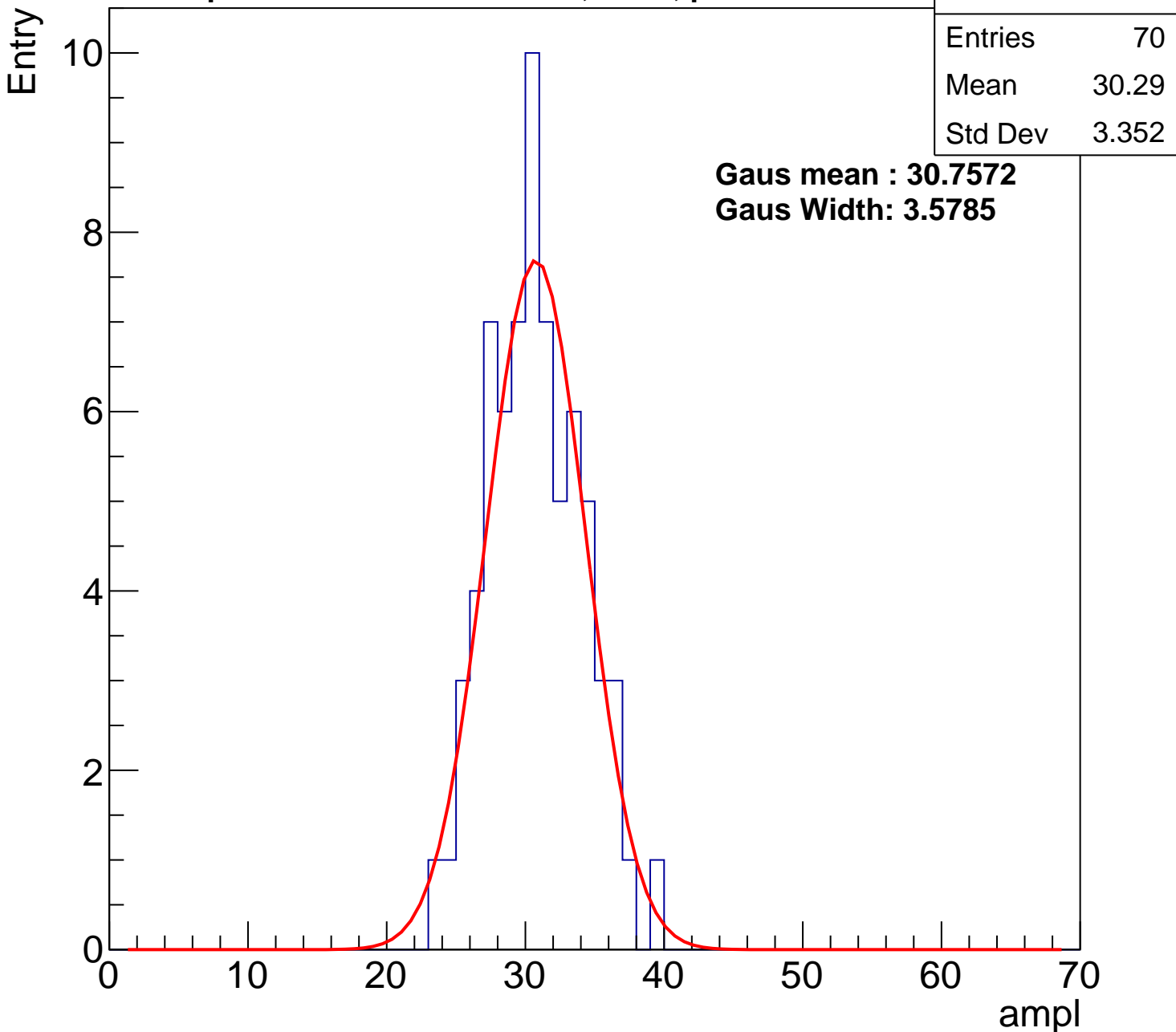
**Gaus Width: 3.5785**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U22-ch73, adc1

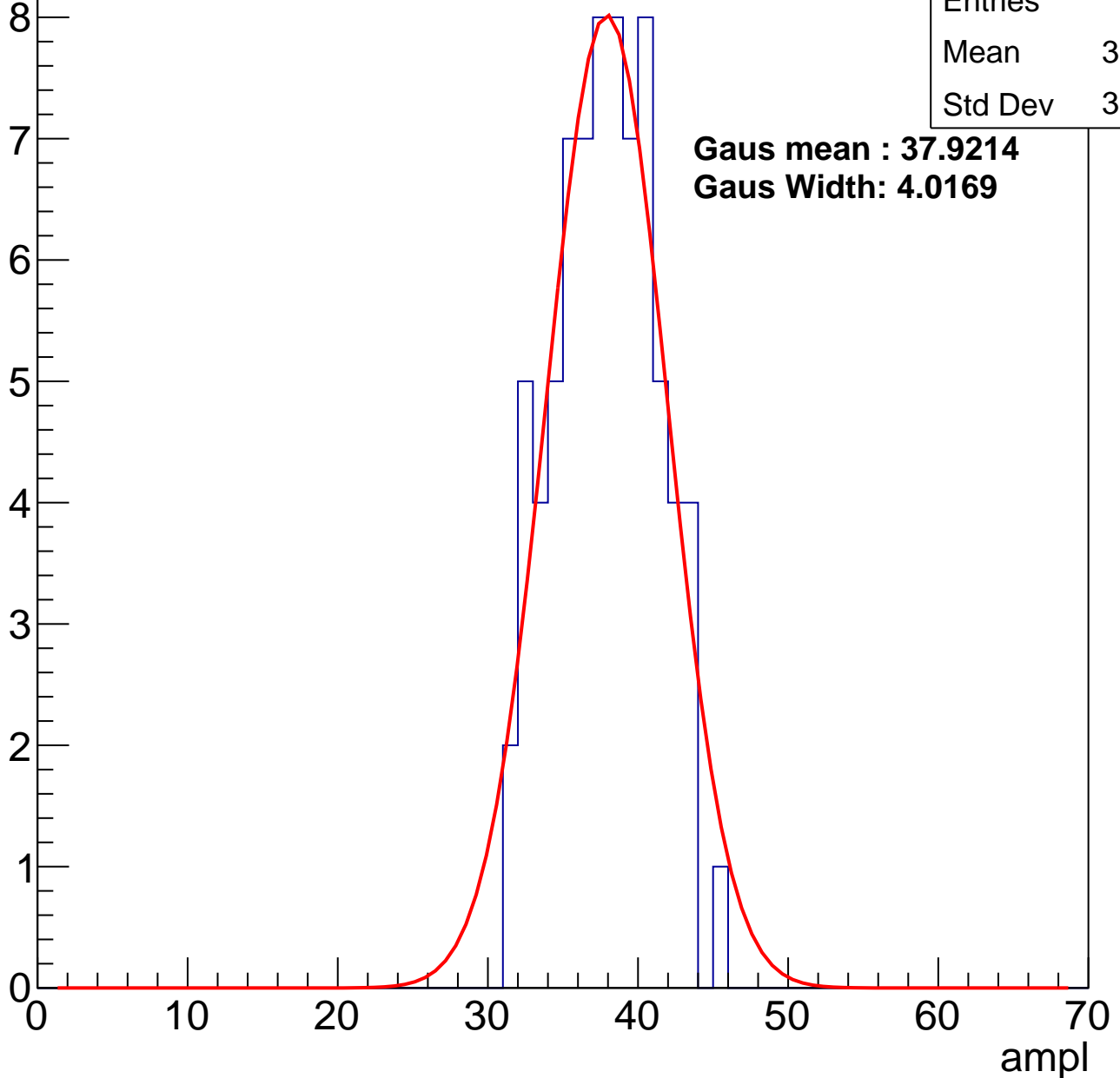
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	75
Mean	37.39
Std Dev	3.318

**Gaus mean : 37.9214**

**Gaus Width: 4.0169**



# B1L101S, U22-ch73, adc2

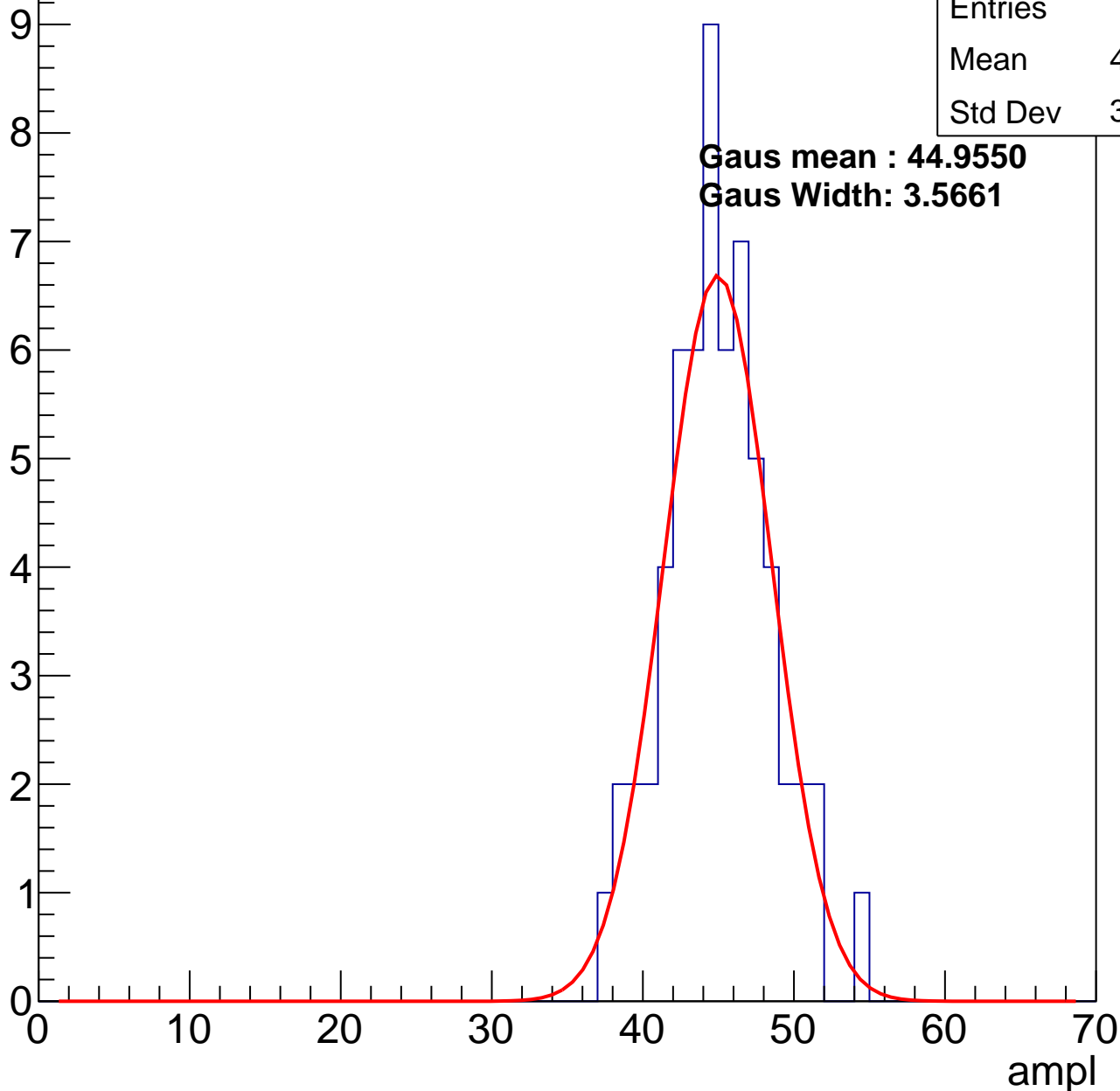
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	44.49
Std Dev	3.429

**Gaus mean : 44.9550**

**Gaus Width: 3.5661**

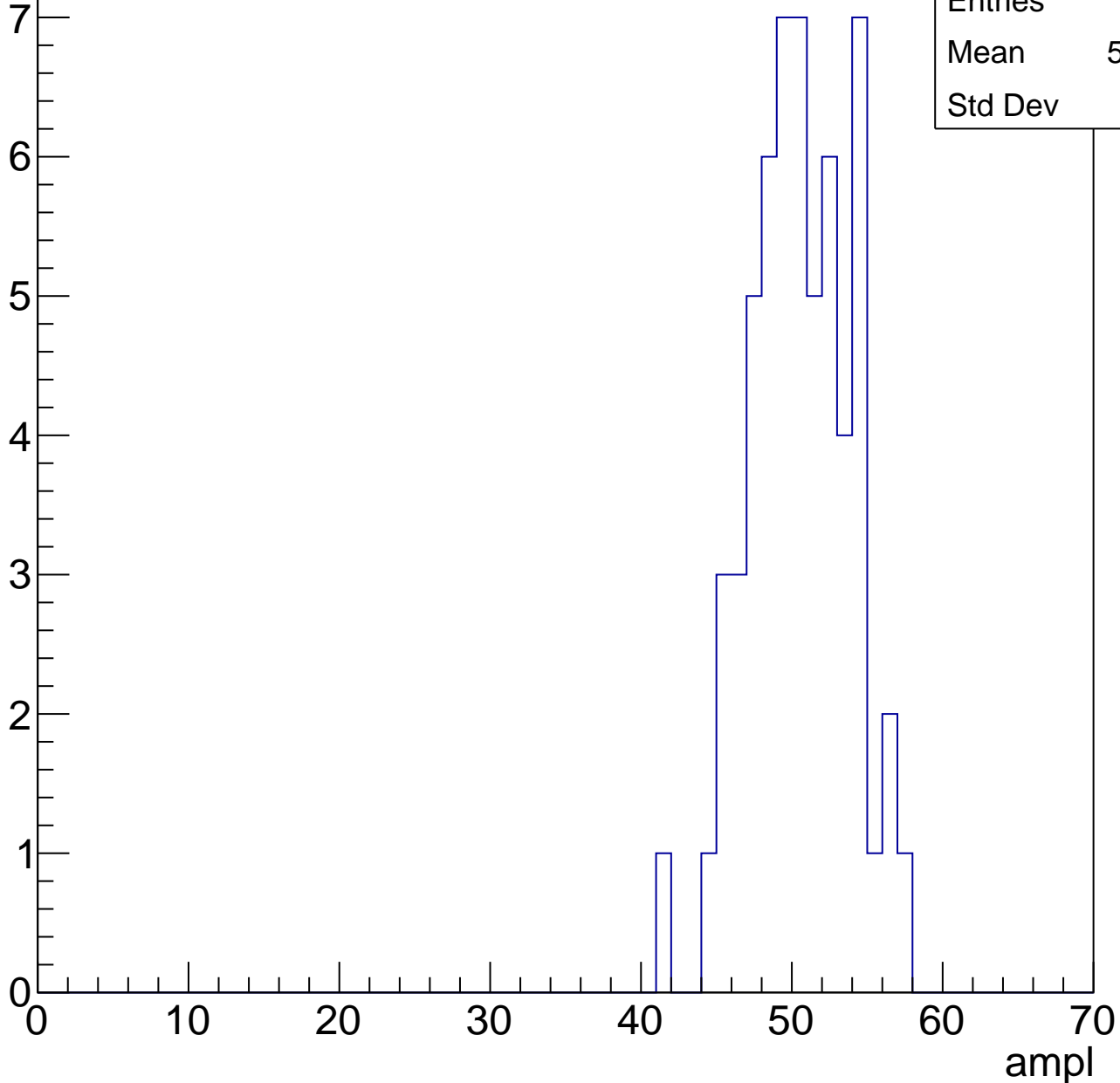


# B1L101S, U22-ch73, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

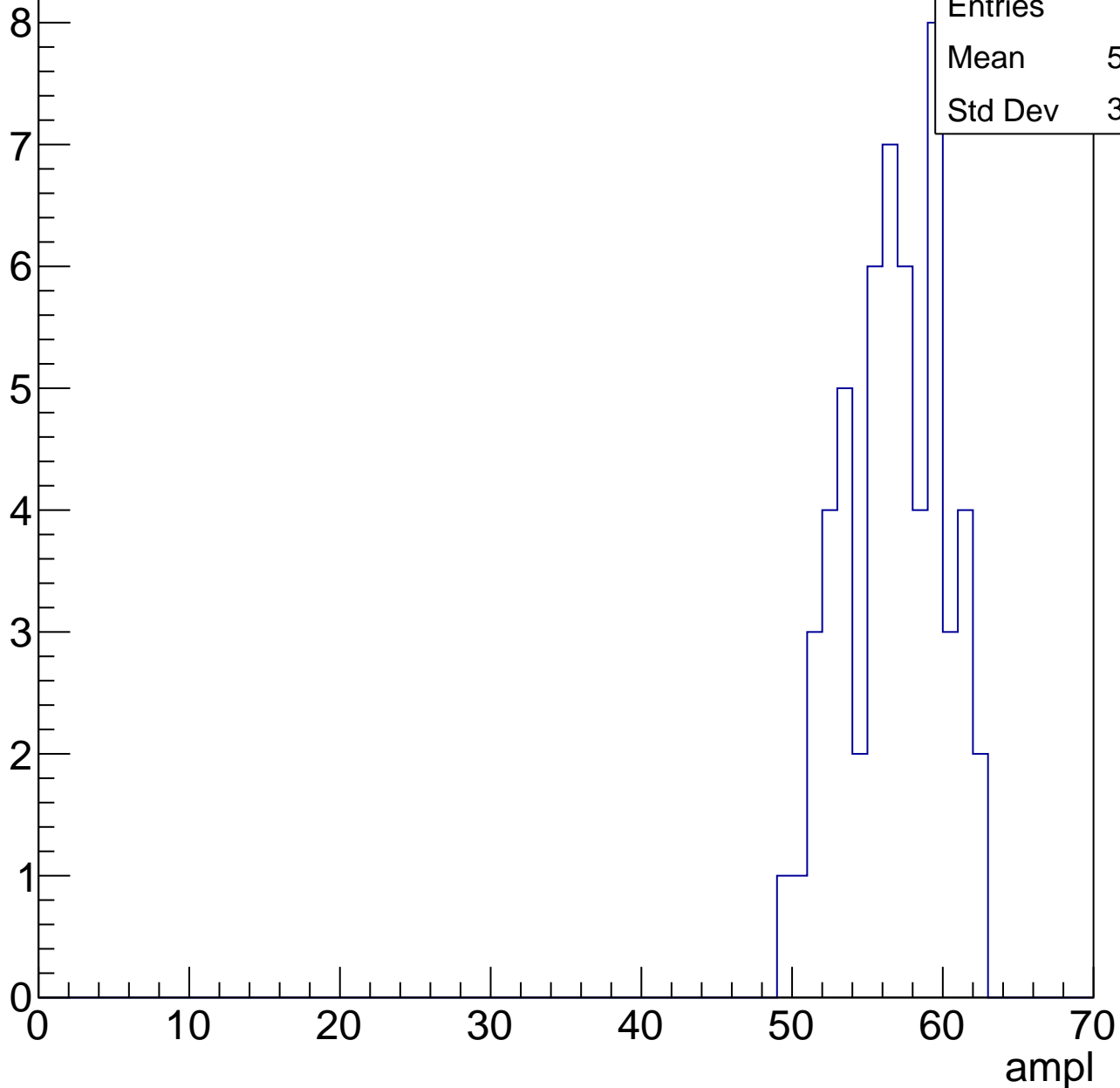
Entries	59
Mean	50.08
Std Dev	3.29



# B1L101S, U22-ch73, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

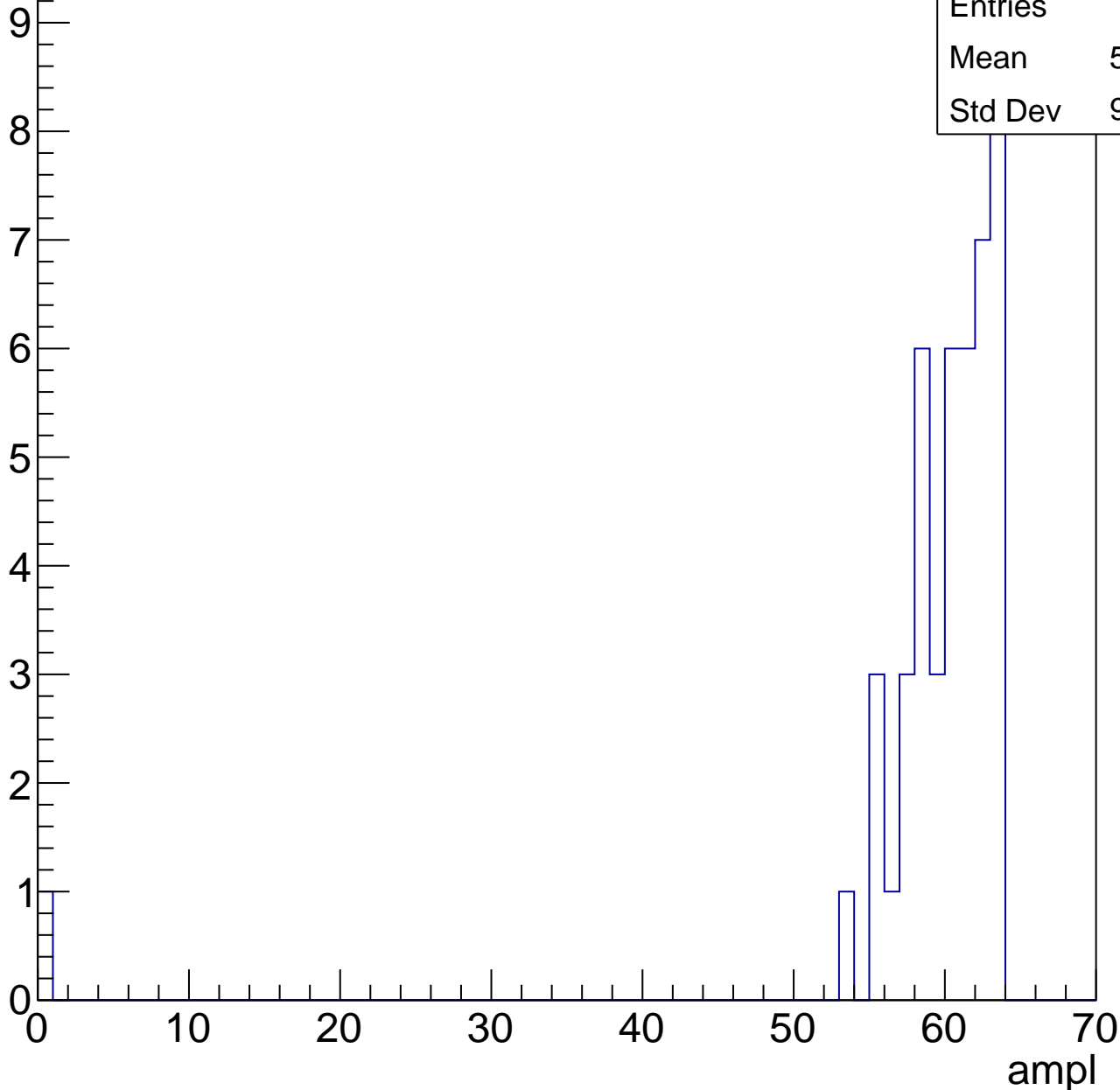


# B1L101S, U22-ch73, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

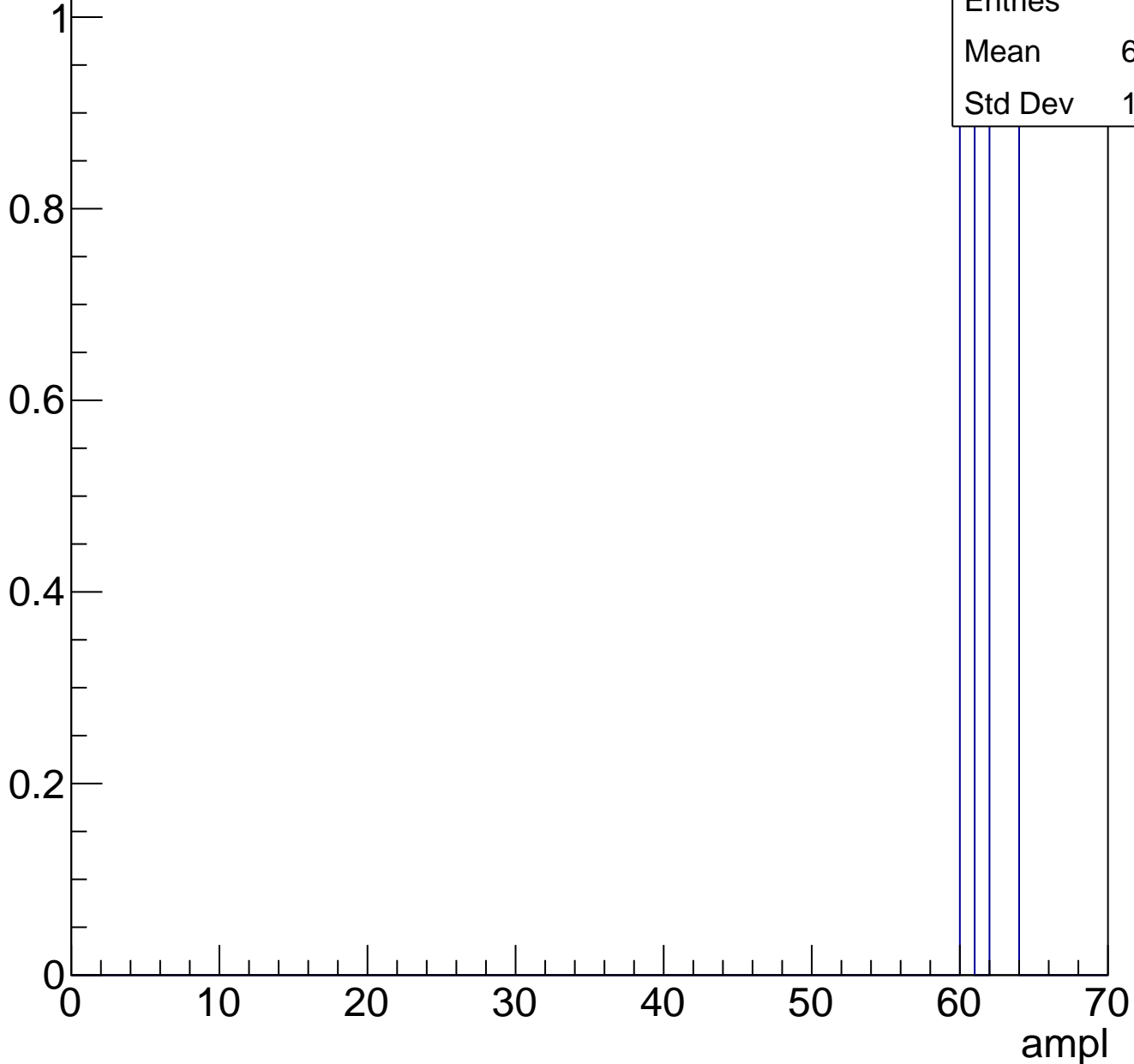
Entries	46
Mean	58.63
Std Dev	9.116



# B1L101S, U22-ch73, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U22-ch73, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U22-ch74, adc0

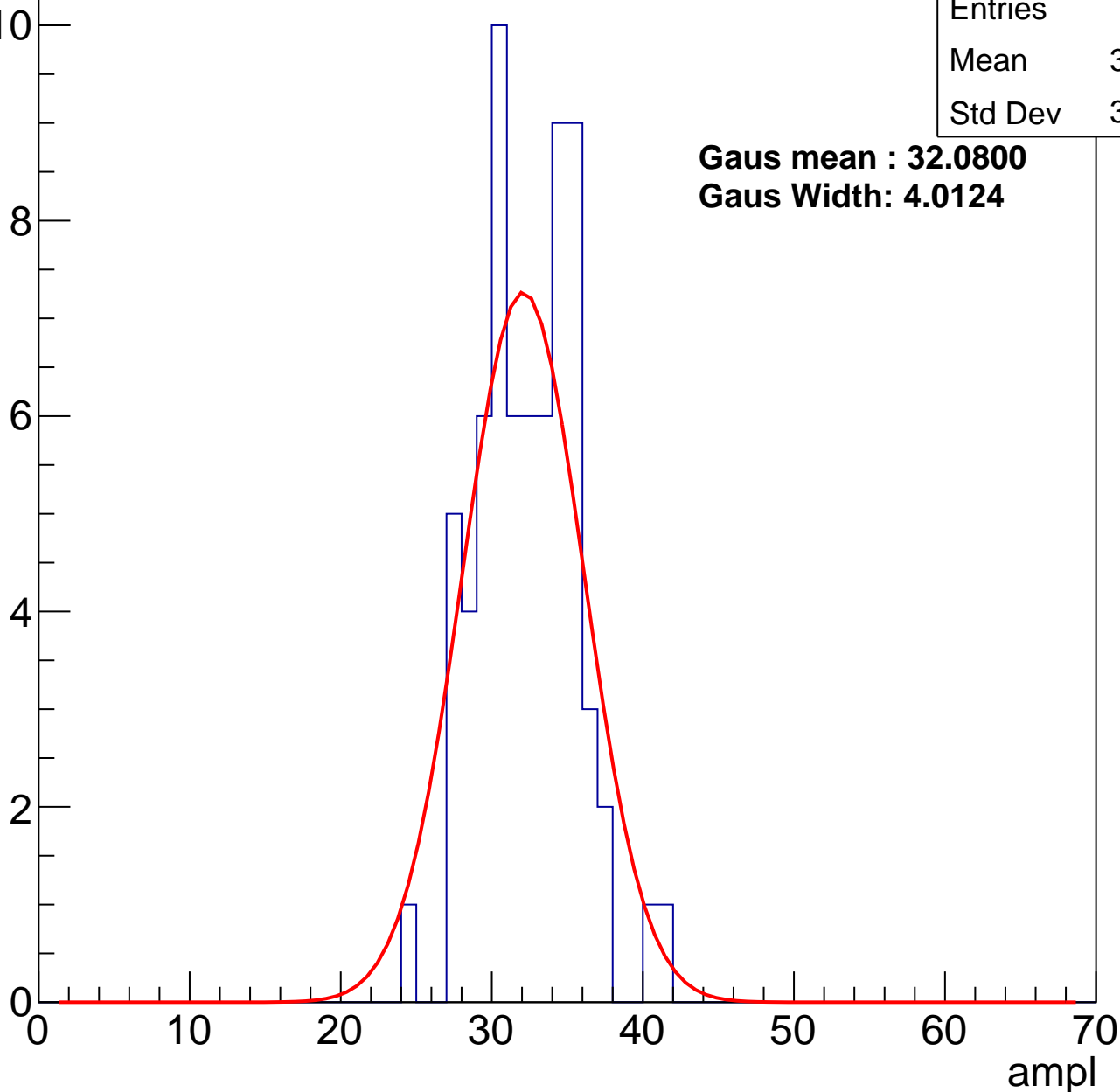
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	31.96
Std Dev	3.228

**Gaus mean : 32.0800**

**Gaus Width: 4.0124**



# B1L101S, U22-ch74, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	69
Mean	38.7
Std Dev	3.621

**Gaus mean : 40.0430**

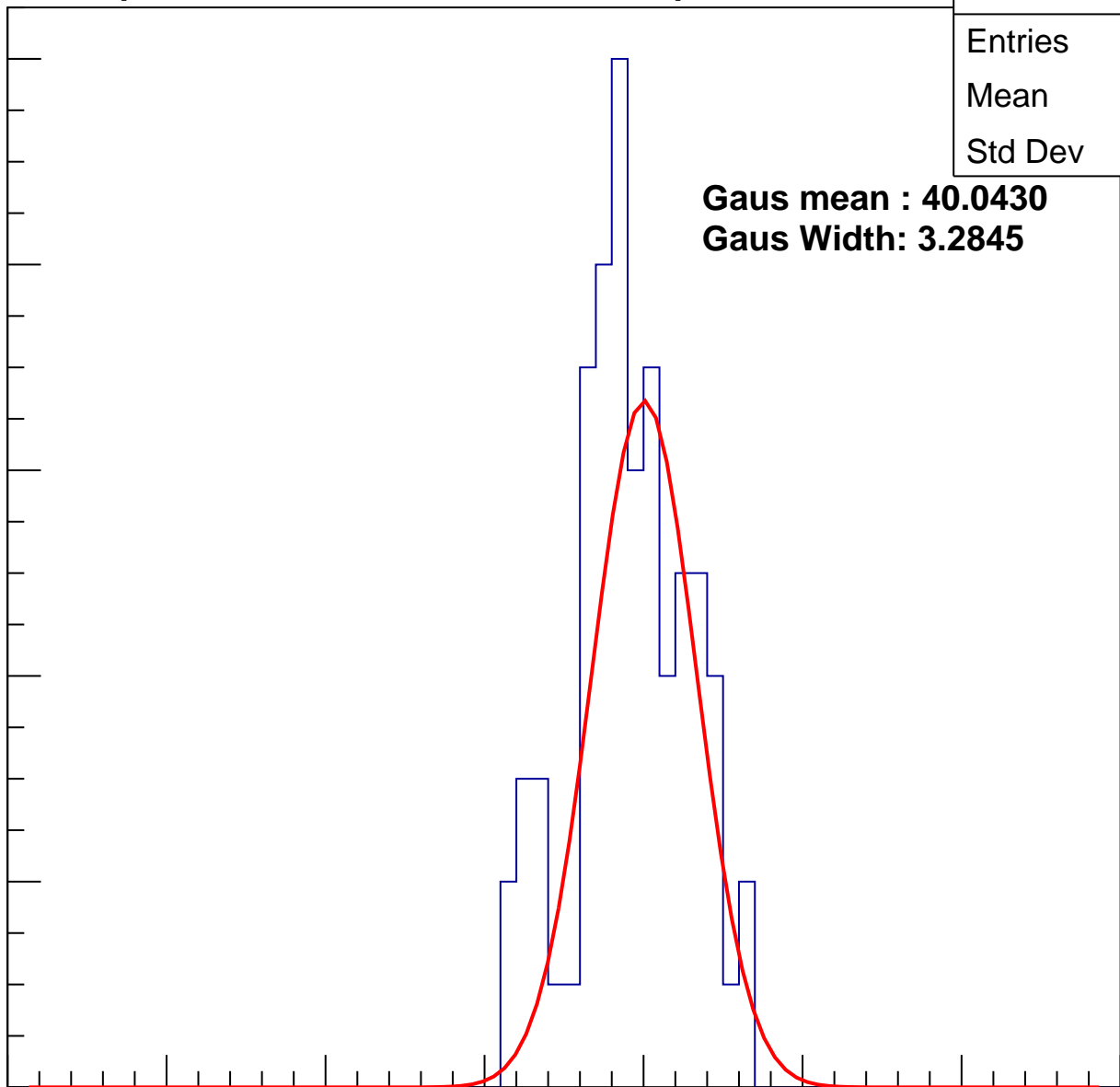
**Gaus Width: 3.2845**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U22-ch74, adc2

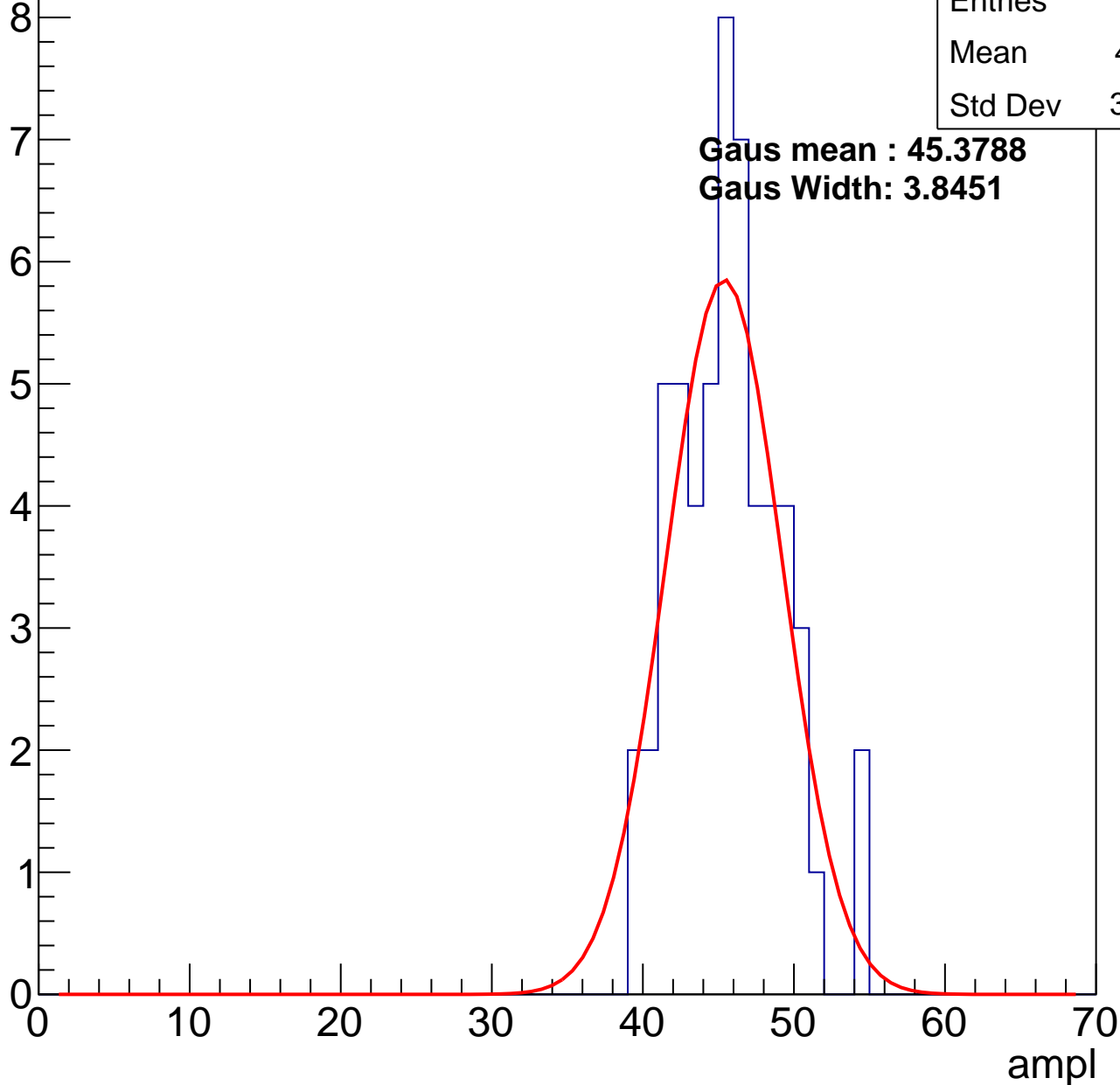
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	56
Mean	45.21
Std Dev	3.437

**Gaus mean : 45.3788**

**Gaus Width: 3.8451**

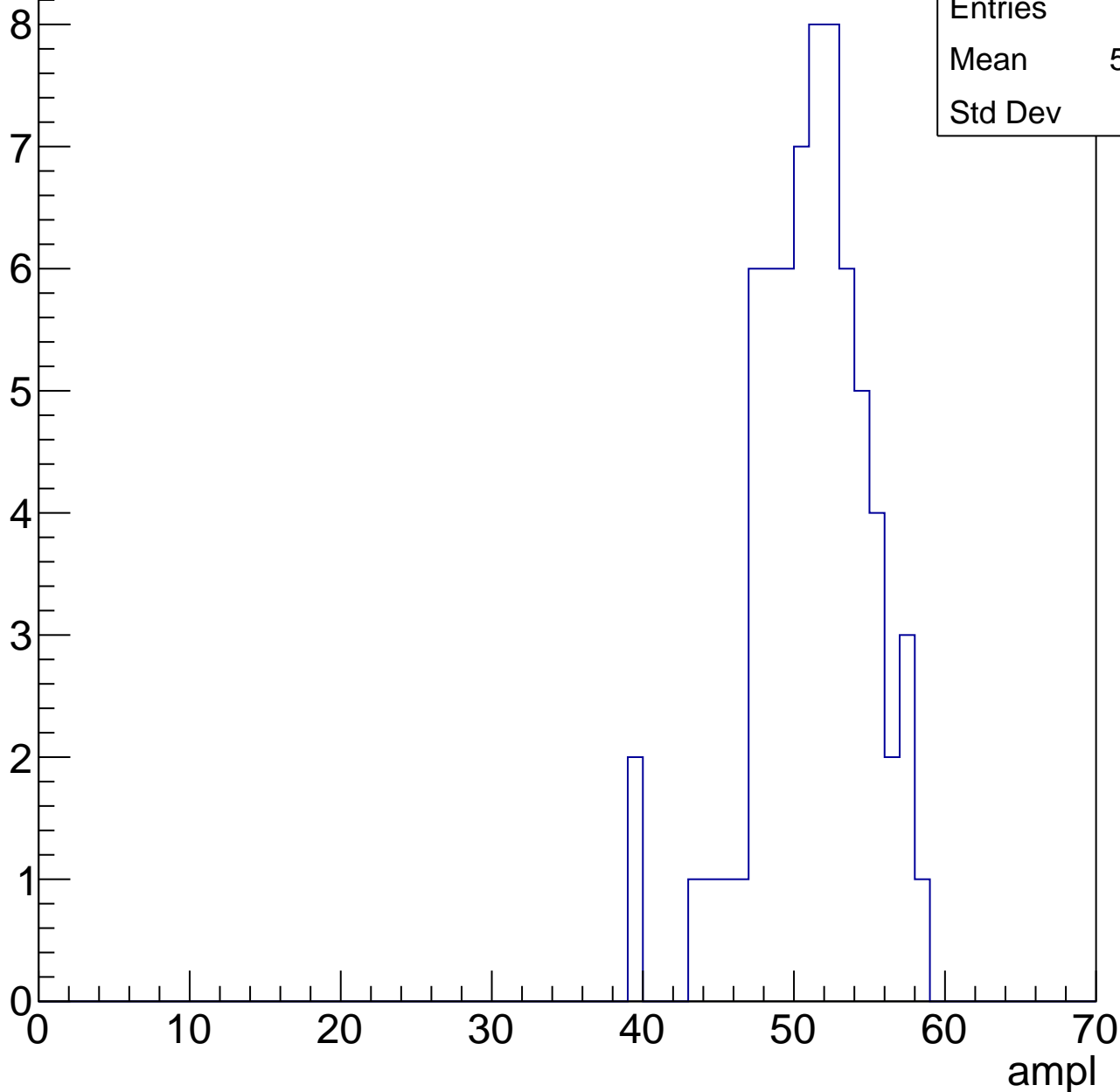


# B1L101S, U22-ch74, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	50.63
Std Dev	3.8

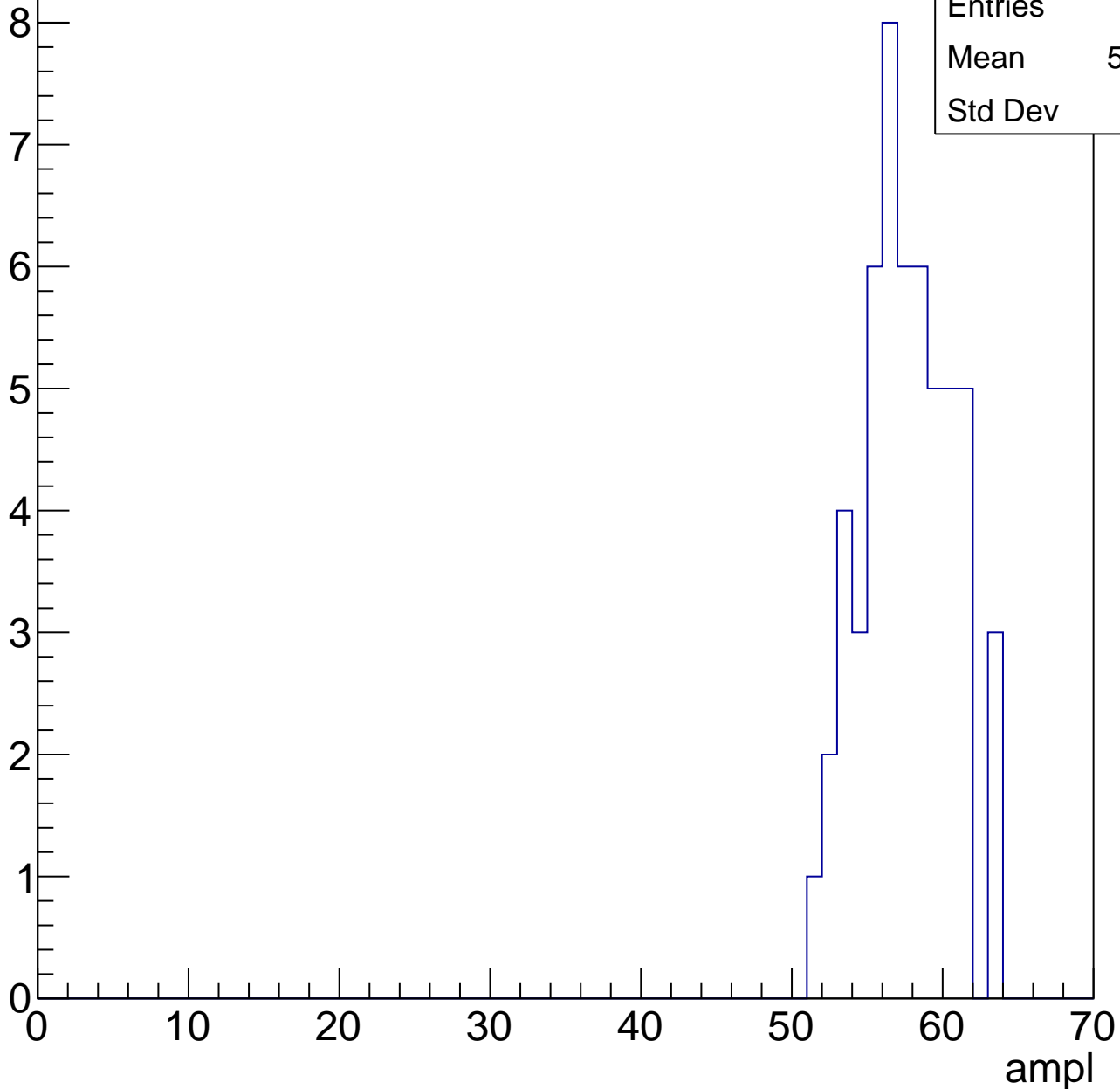


# B1L101S, U22-ch74, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	54
Mean	57.15
Std Dev	2.94

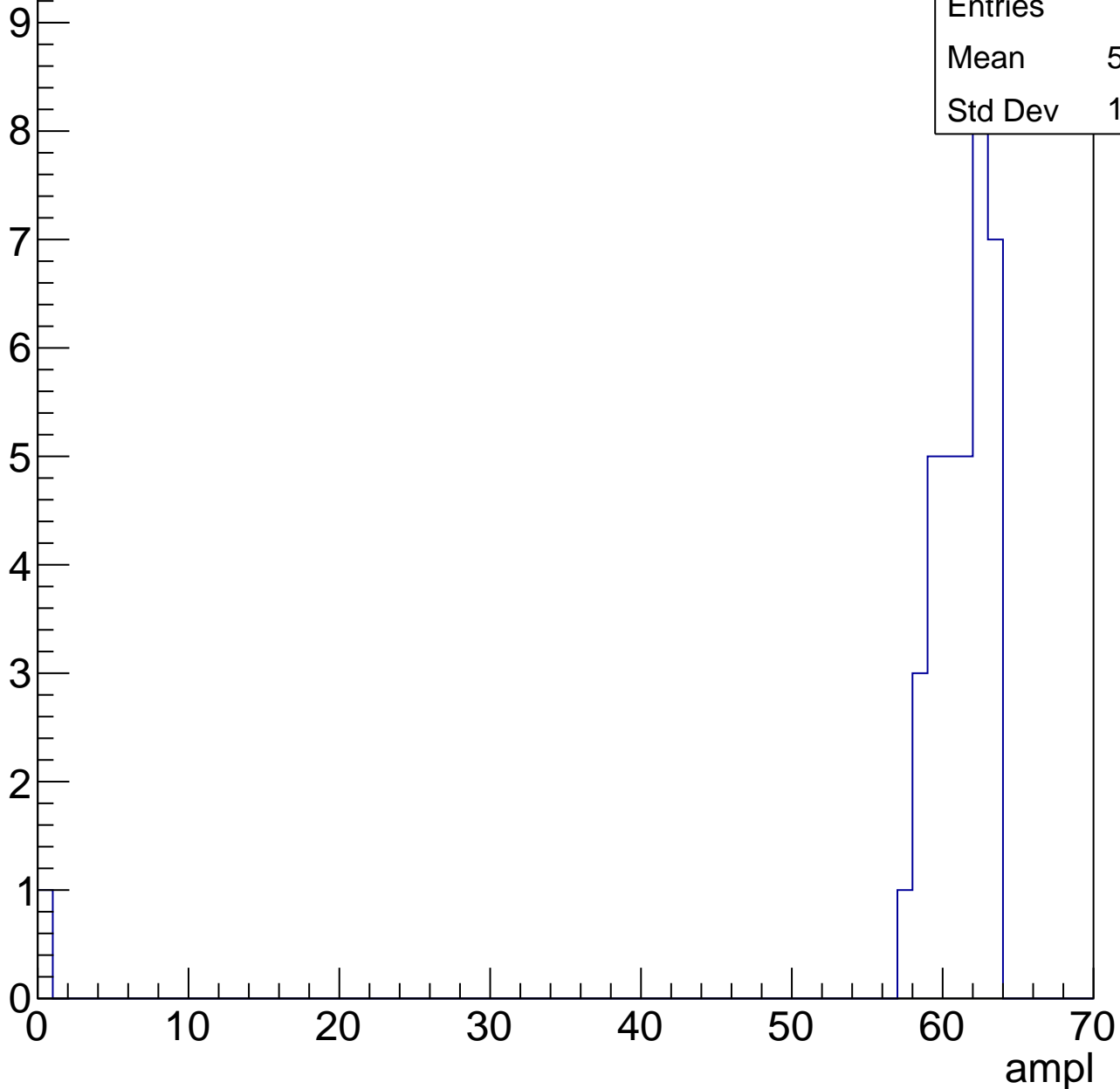


# B1L101S, U22-ch74, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	36
Mean	59.17
Std Dev	10.14



# B1L101S, U22-ch74, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U22-ch74, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U22-ch75, adc0

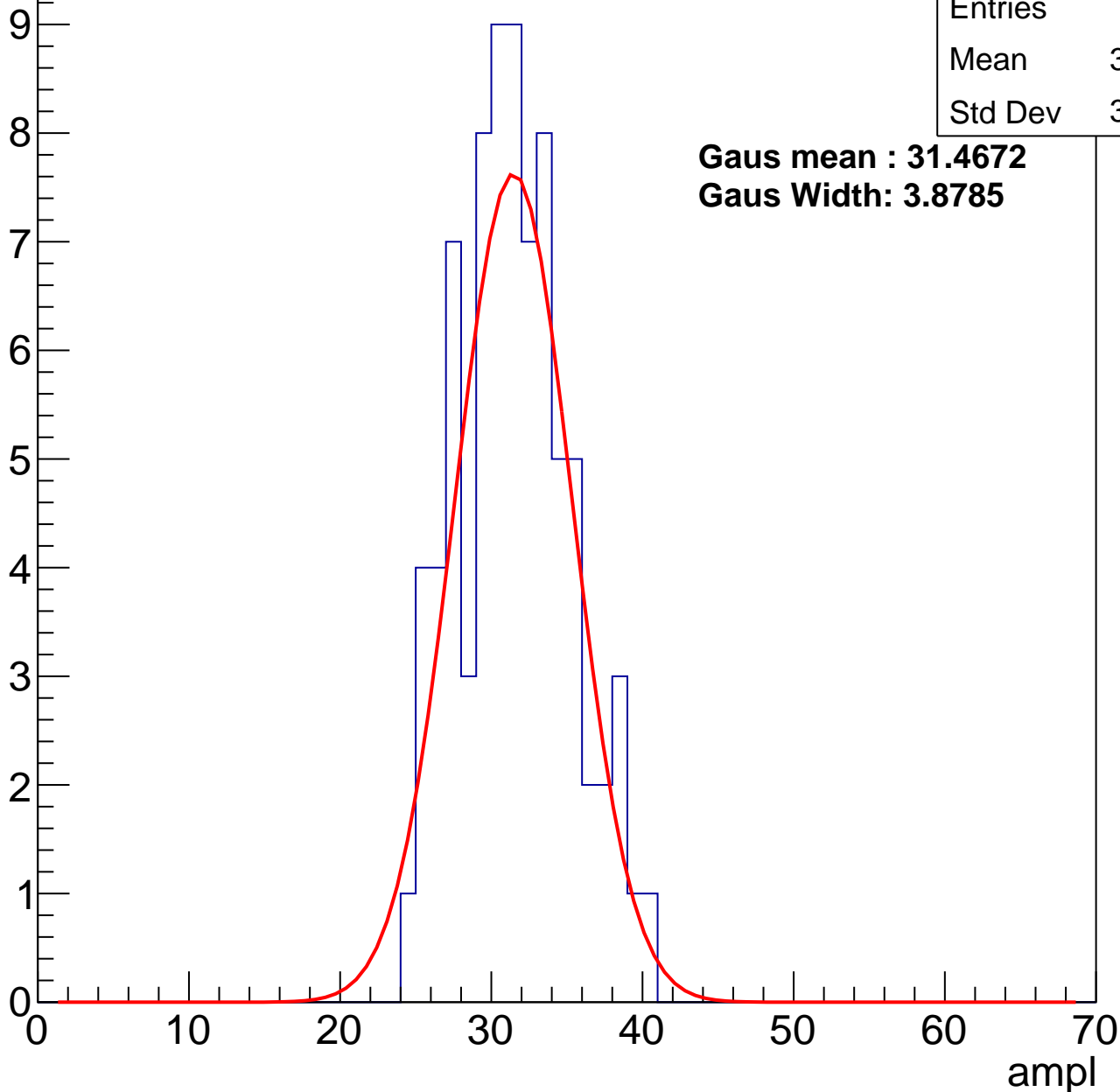
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	79
Mean	31.06
Std Dev	3.647

**Gaus mean : 31.4672**

**Gaus Width: 3.8785**



# B1L101S, U22-ch75, adc1

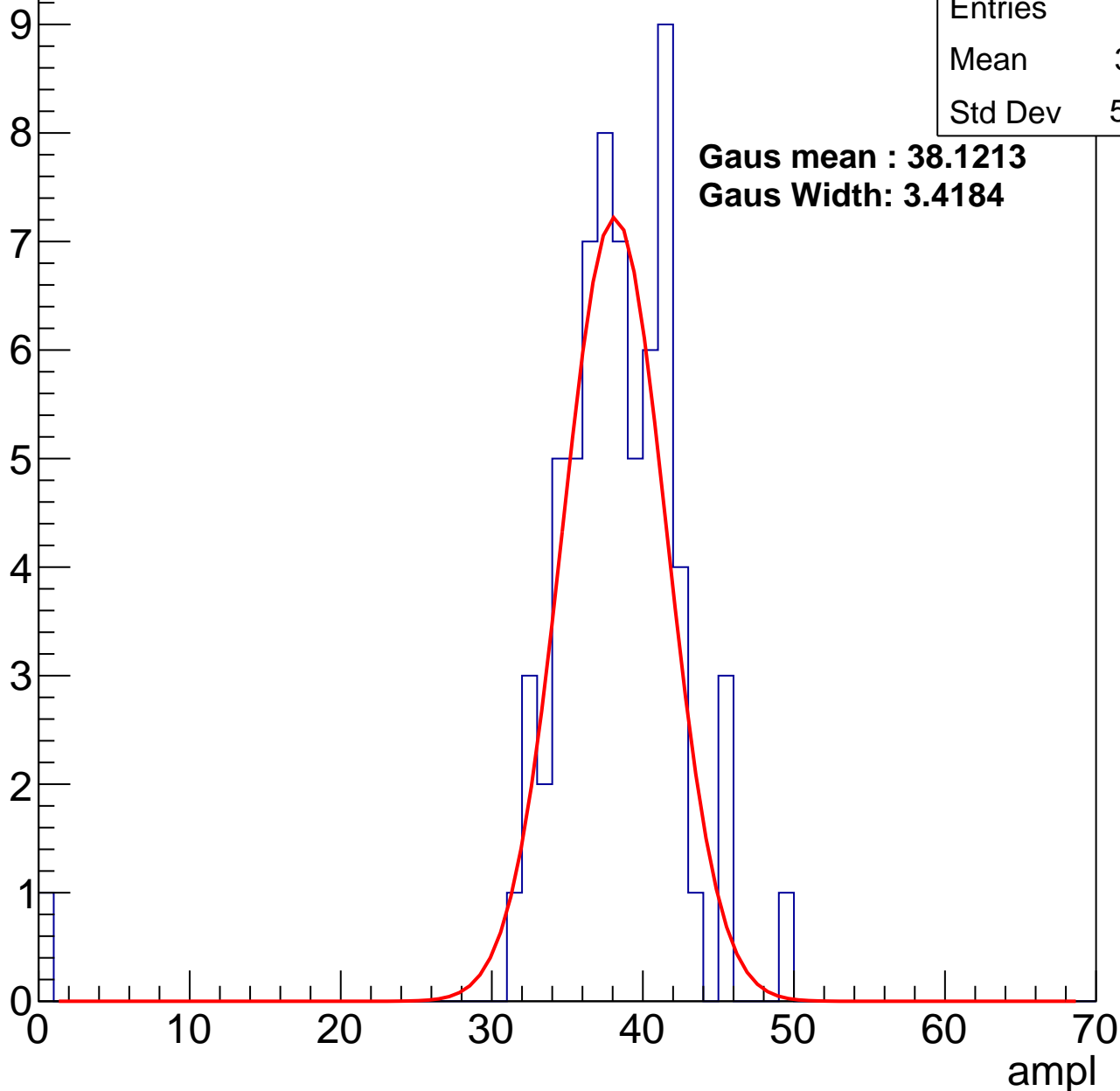
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	37.51
Std Dev	5.769

**Gaus mean : 38.1213**

**Gaus Width: 3.4184**



# B1L101S, U22-ch75, adc2

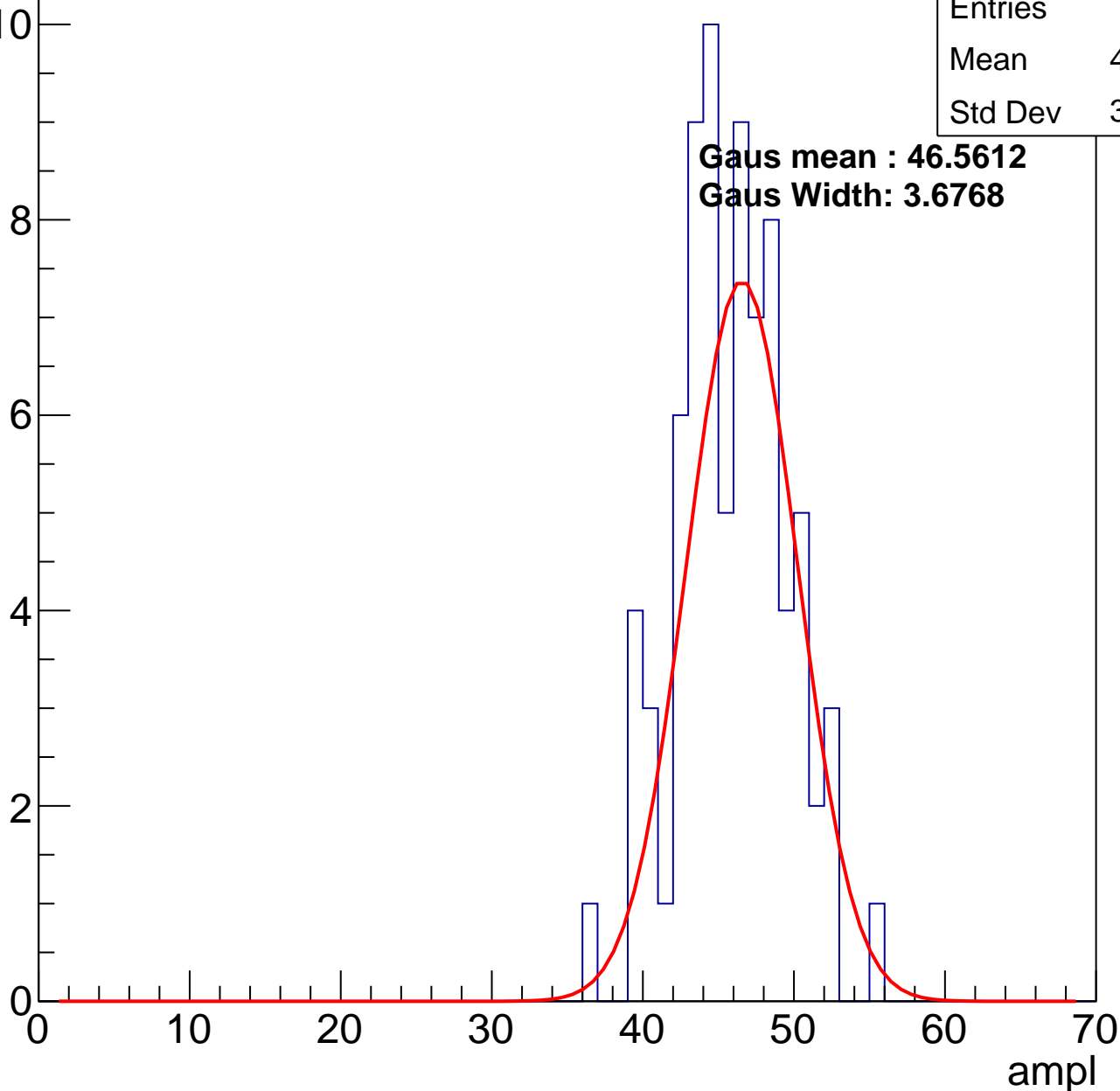
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	78
Mean	45.42
Std Dev	3.614

**Gaus mean : 46.5612**

**Gaus Width: 3.6768**



# B1L101S, U22-ch75, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

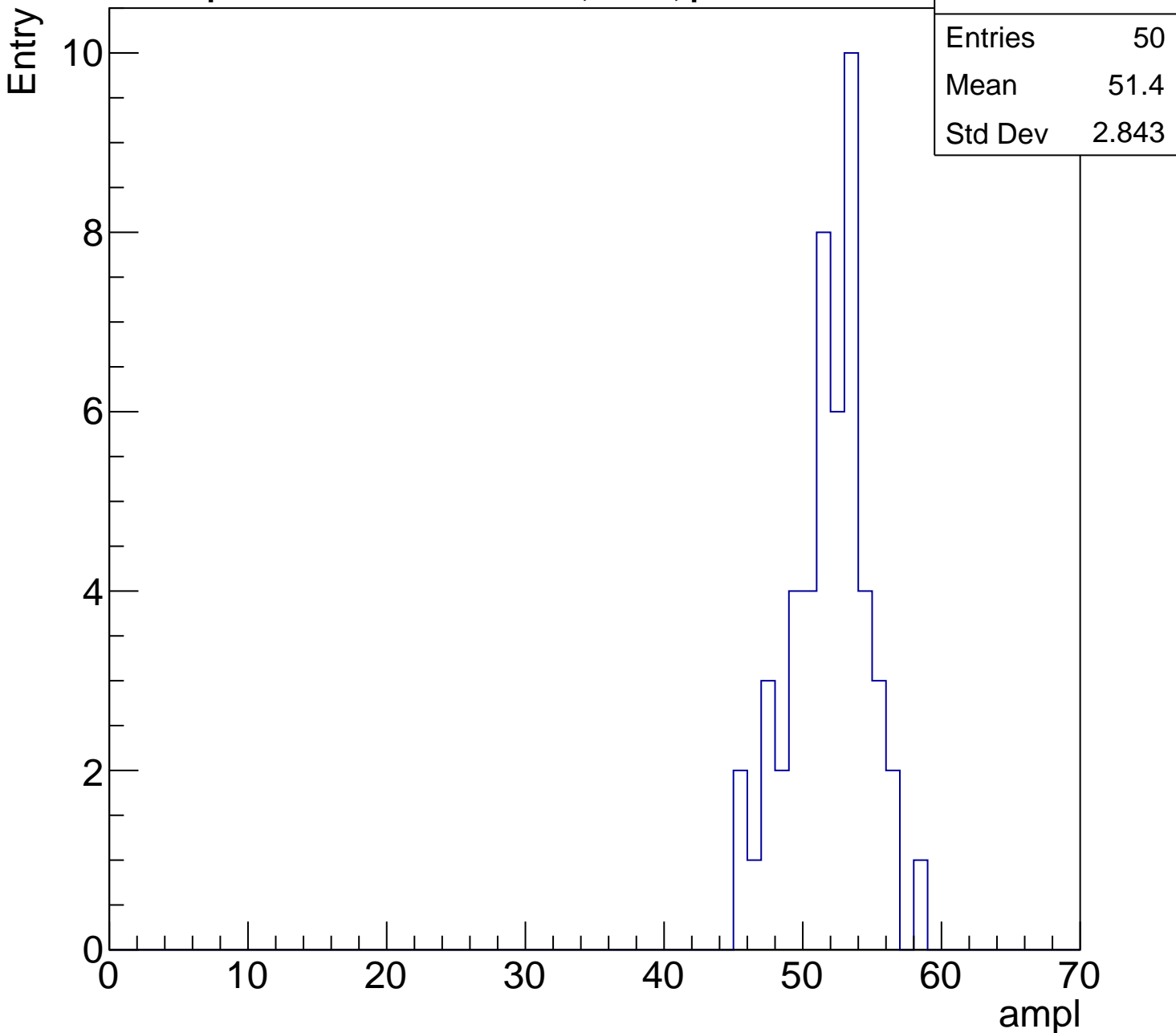
Entries	50
Mean	51.4
Std Dev	2.843

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

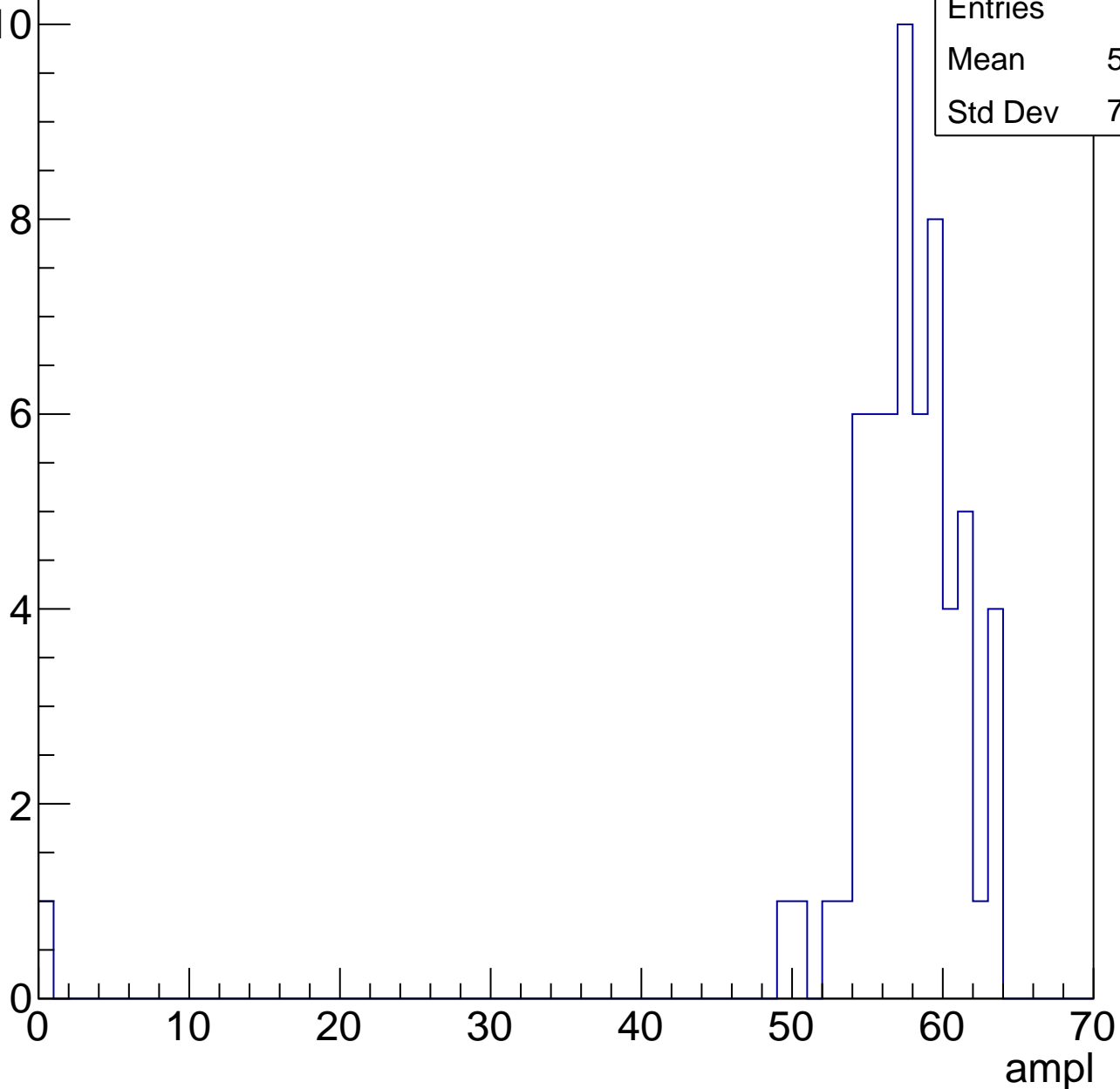


# B1L101S, U22-ch75, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	56.44
Std Dev	7.883



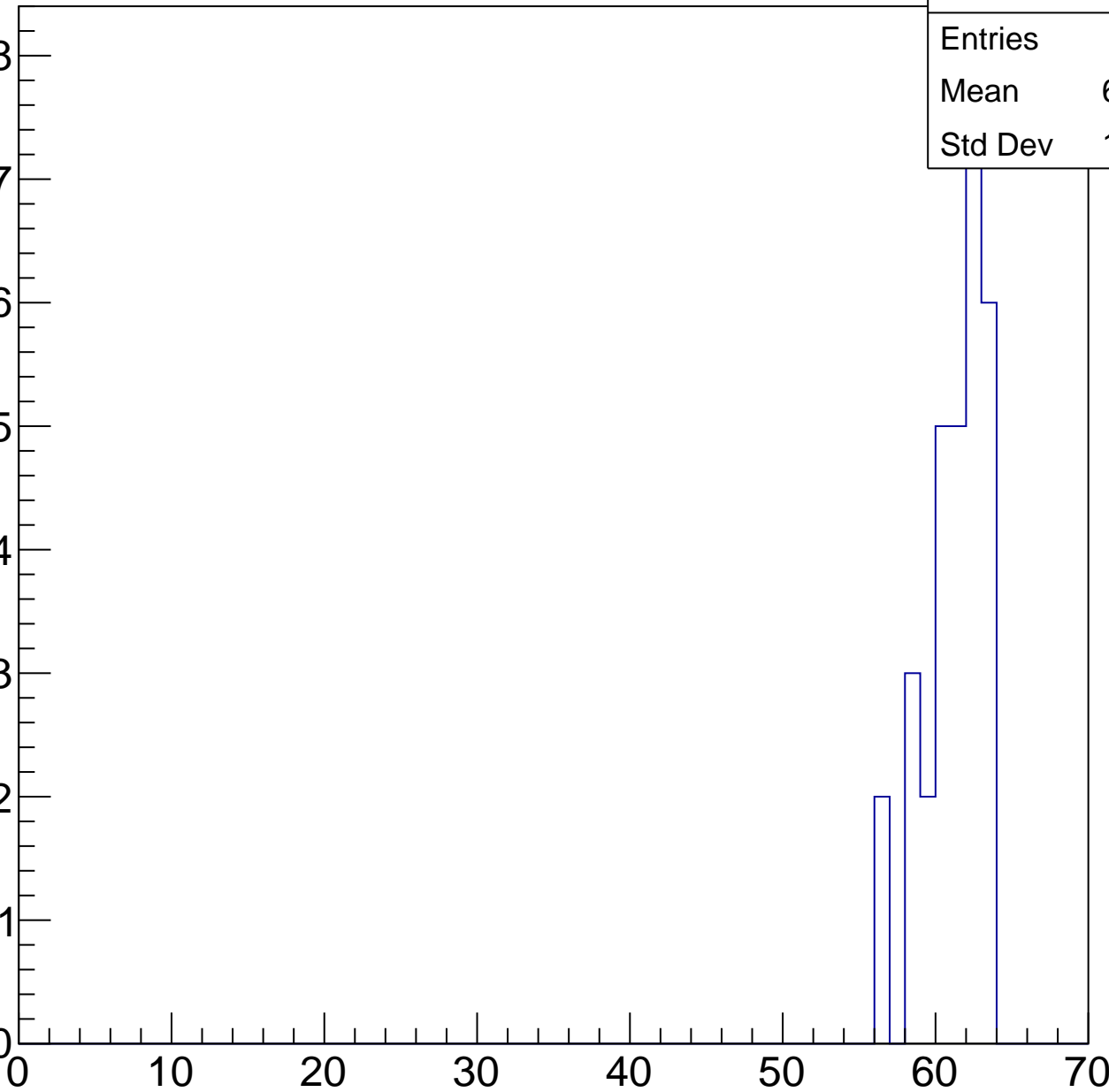
# B1L101S, U22-ch75, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	31
Mean	60.74
Std Dev	1.967

8  
7  
6  
5  
4  
3  
2  
1  
0



ampl

# B1L101S, U22-ch75, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U22-ch75, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U22-ch76, adc0

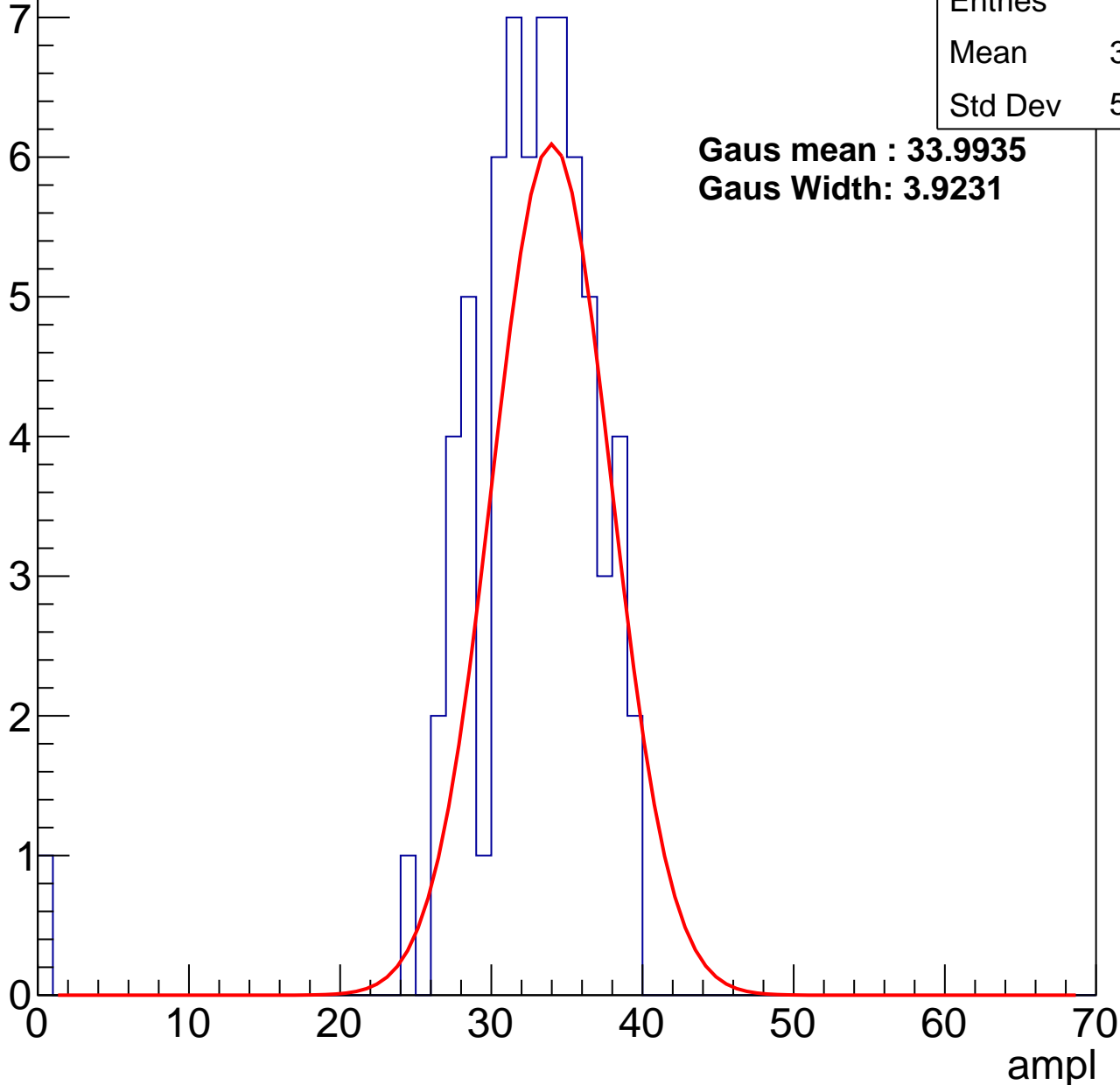
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	67
Mean	31.97
Std Dev	5.277

**Gaus mean : 33.9935**

**Gaus Width: 3.9231**



# B1L101S, U22-ch76, adc1

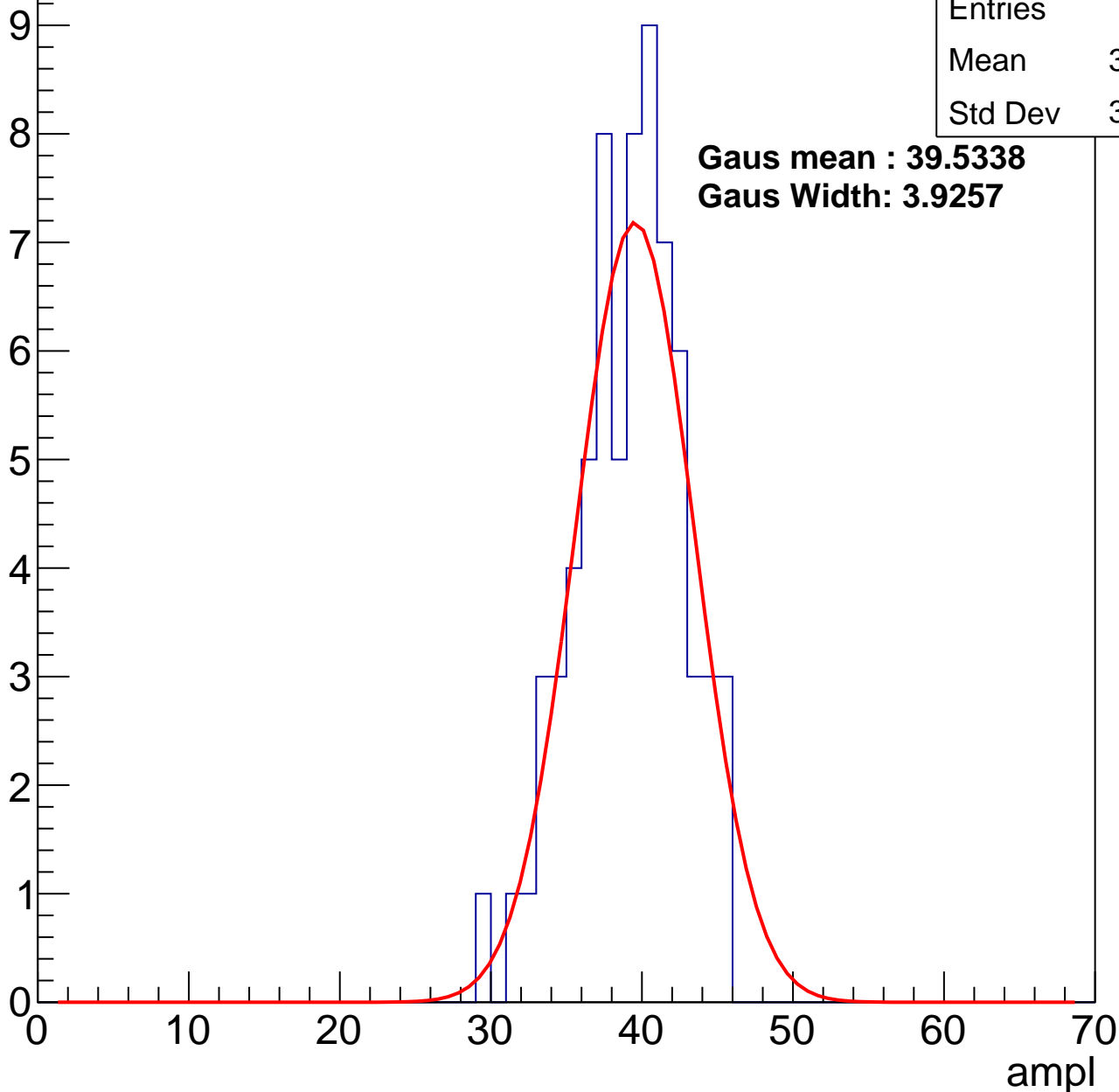
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	38.66
Std Dev	3.496

**Gaus mean : 39.5338**

**Gaus Width: 3.9257**



# B1L101S, U22-ch76, adc2

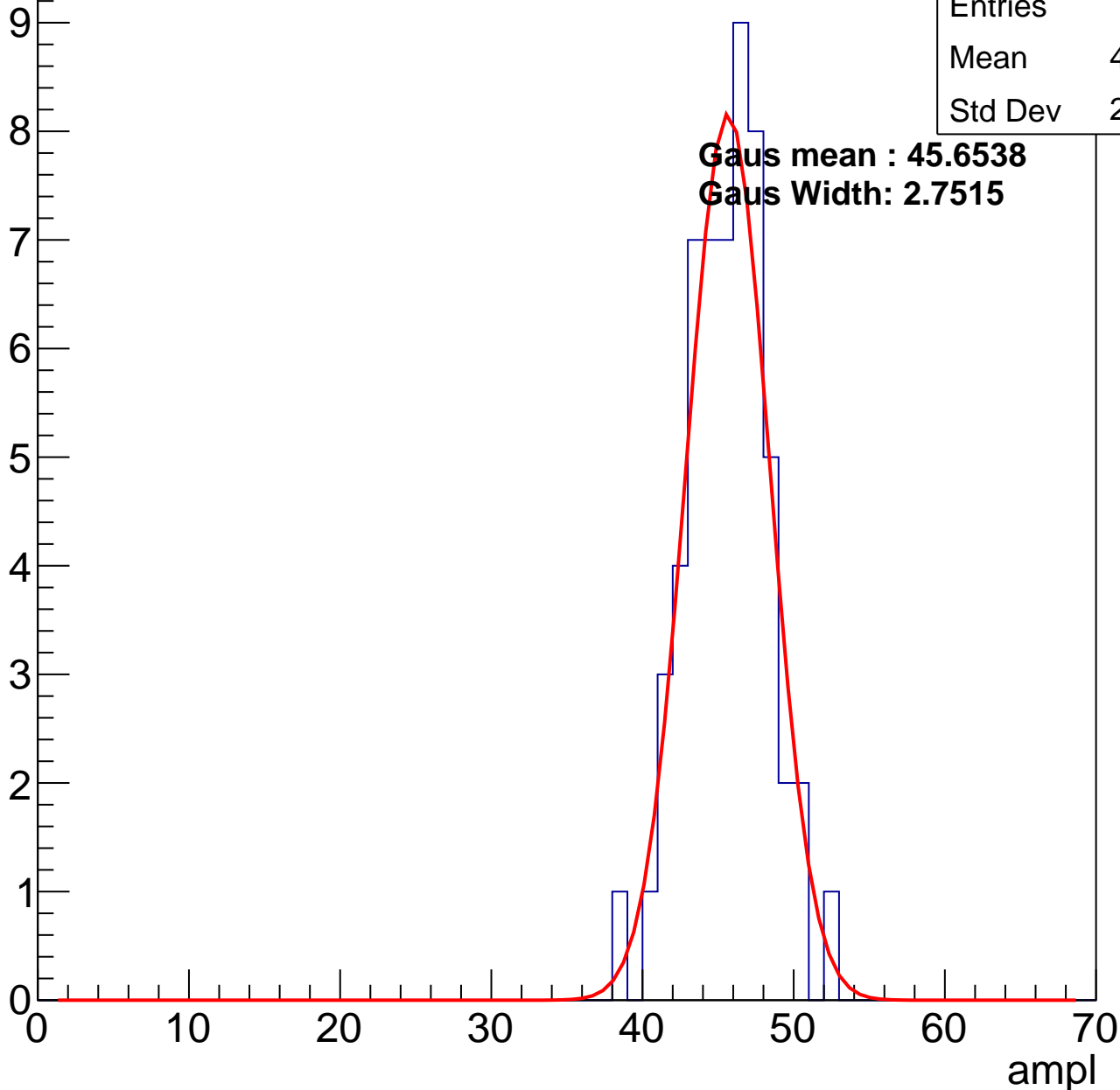
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	57
Mean	45.14
Std Dev	2.678

**Gaus mean : 45.6538**

**Gaus Width: 2.7515**

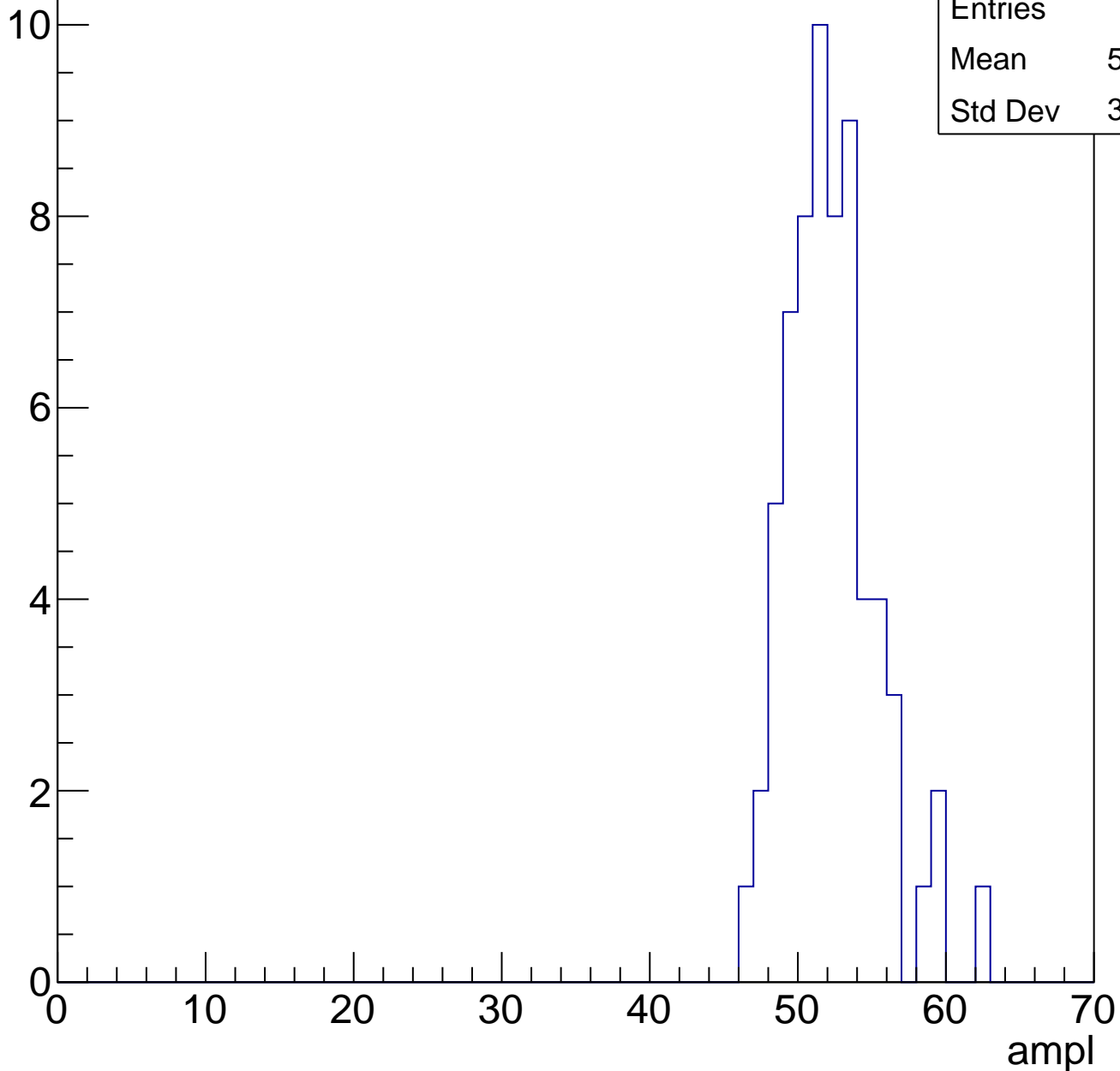


# B1L101S, U22-ch76, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

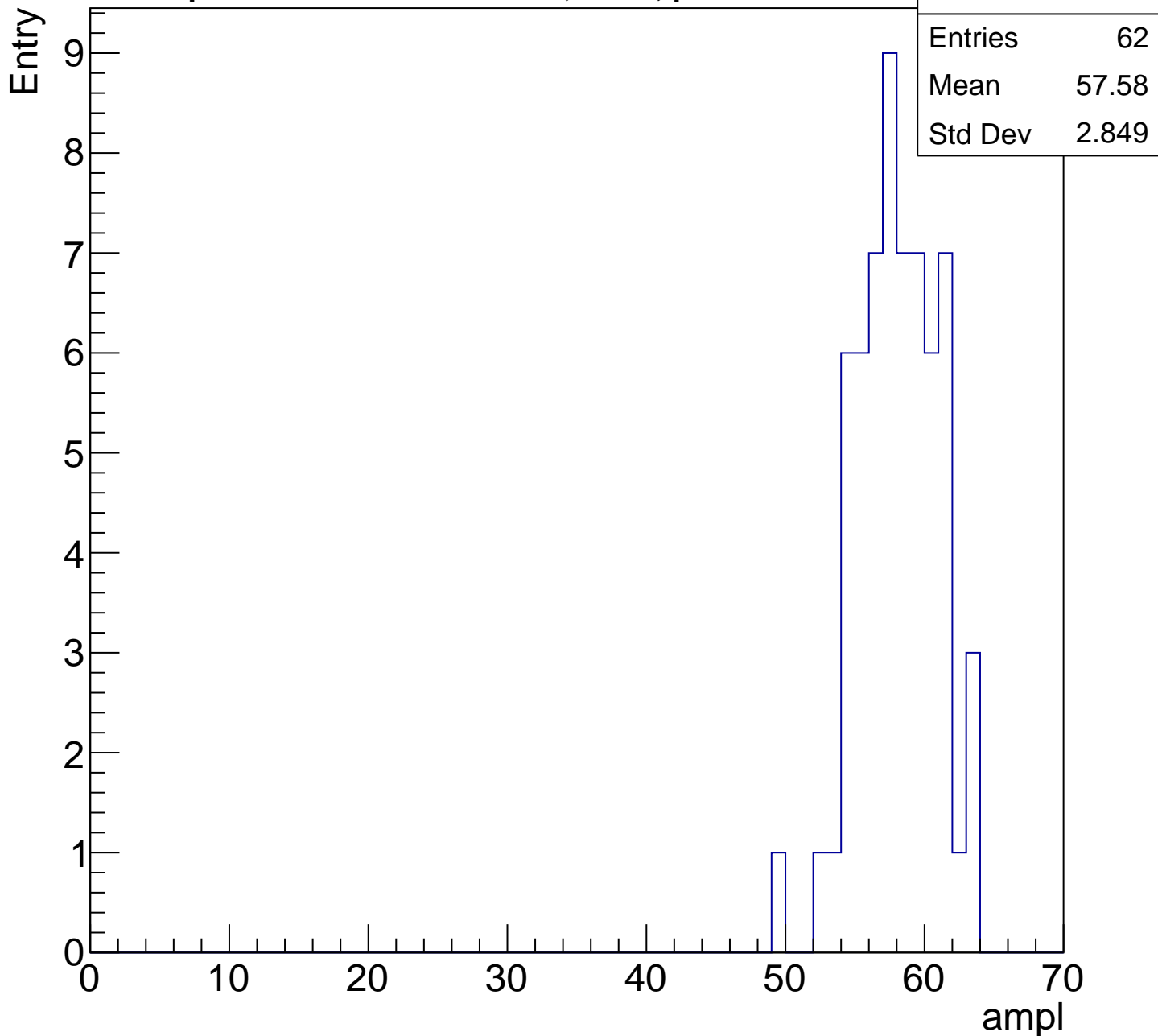
Entries	65
Mean	51.82
Std Dev	3.068

Entry



# B1L101S, U22-ch76, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

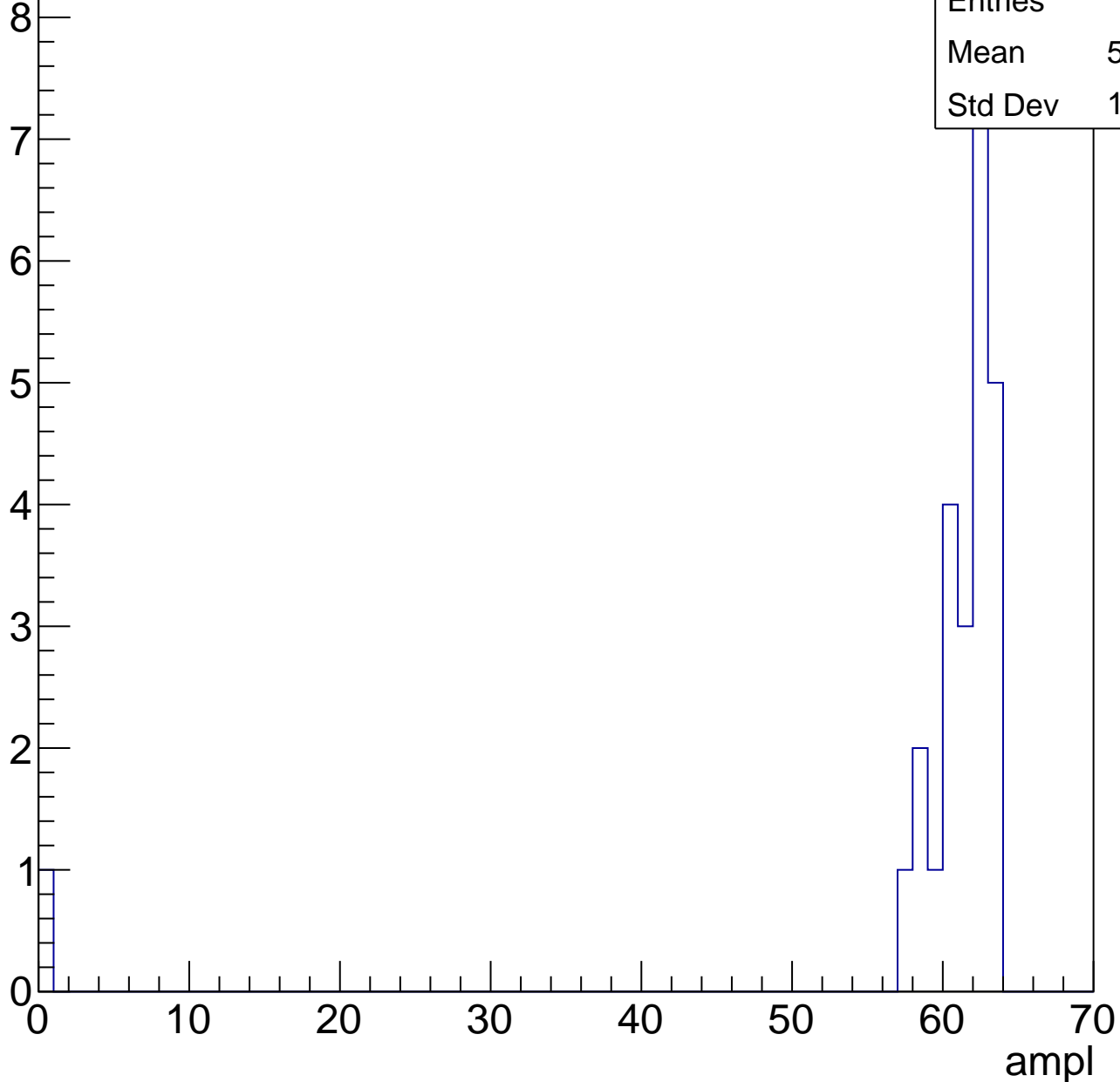


# B1L101S, U22-ch76, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	25
Mean	58.64
Std Dev	12.09



# B1L101S, U22-ch76, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	2
Mean	63
Std Dev	0

ampl



# B1L101S, U22-ch76, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U22-ch77, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	65
Mean	30.63
Std Dev	2.933

**Gaus mean : 31.3360**

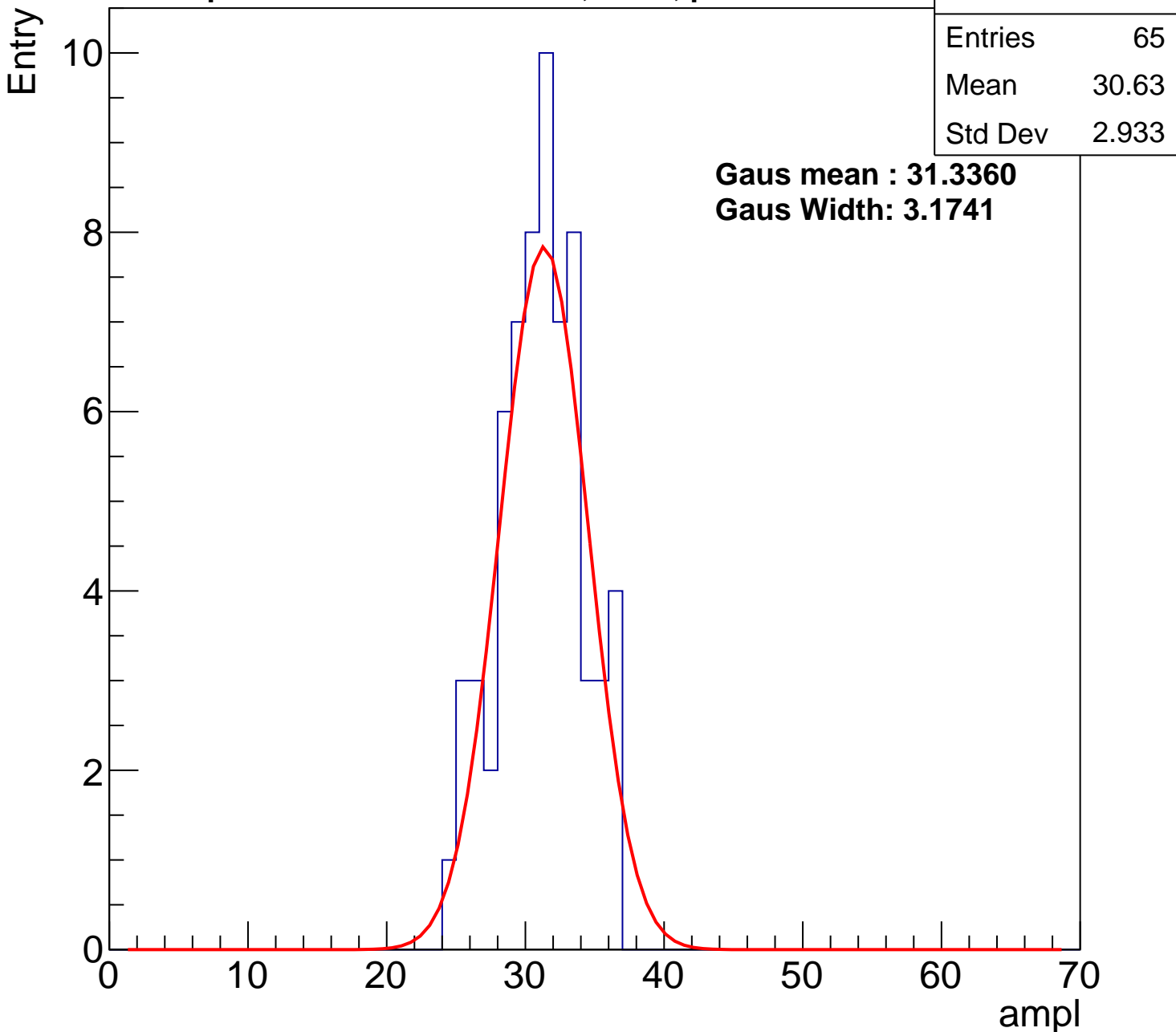
**Gaus Width: 3.1741**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U22-ch77, adc1

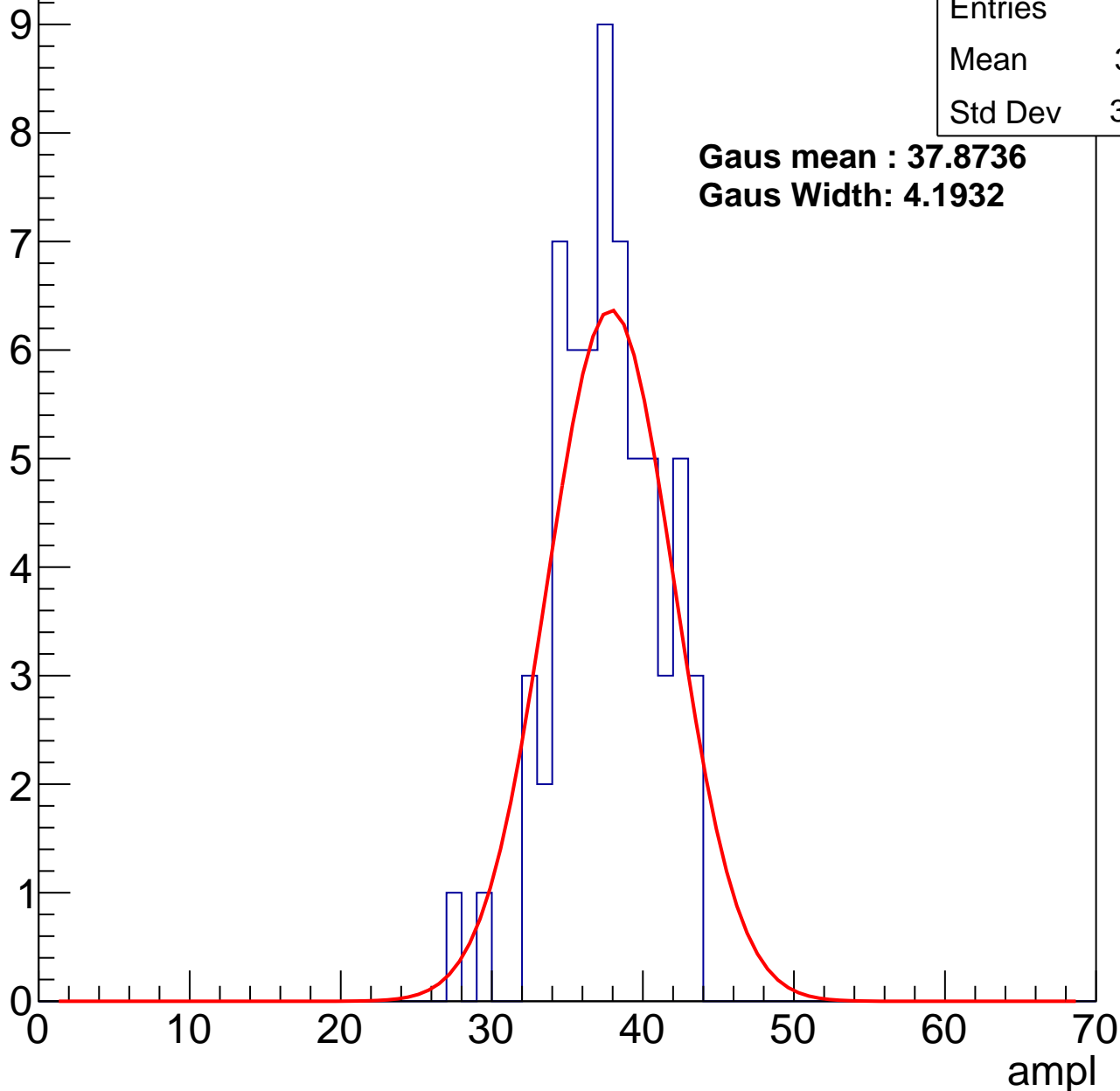
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	37.11
Std Dev	3.372

**Gaus mean : 37.8736**

**Gaus Width: 4.1932**



# B1L101S, U22-ch77, adc2

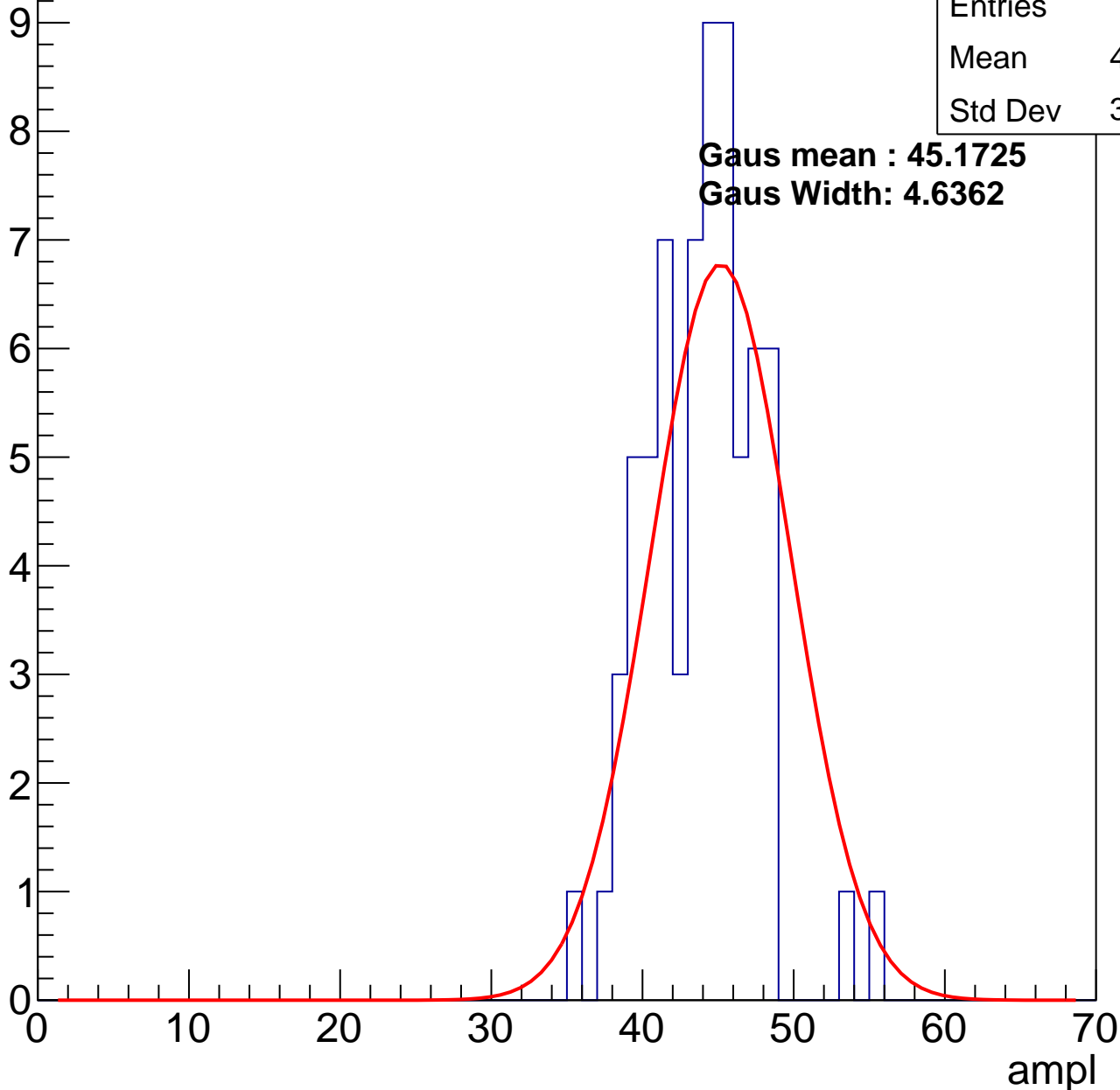
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	43.54
Std Dev	3.594

**Gaus mean : 45.1725**

**Gaus Width: 4.6362**

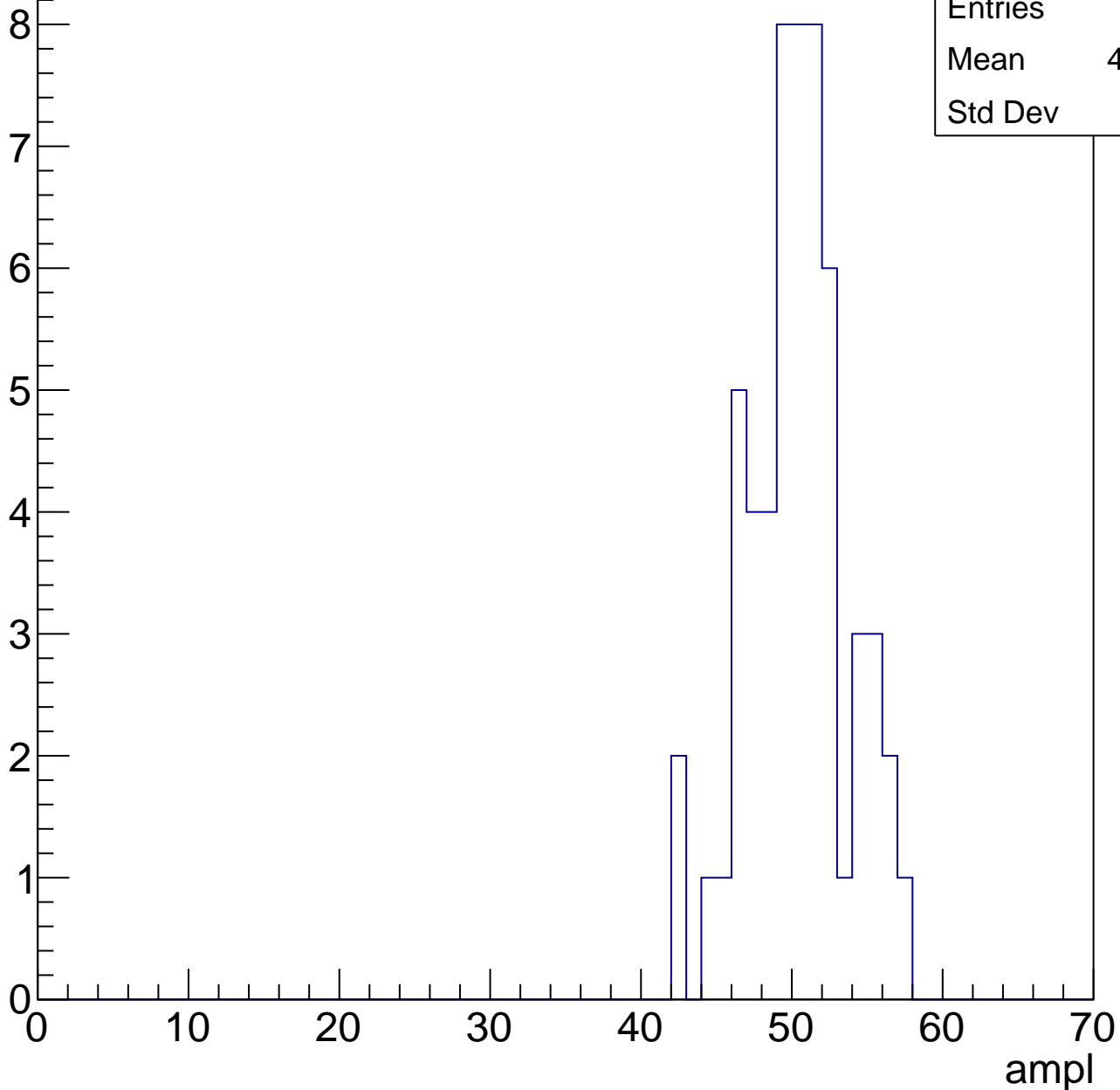


# B1L101S, U22-ch77, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	57
Mean	49.89
Std Dev	3.28

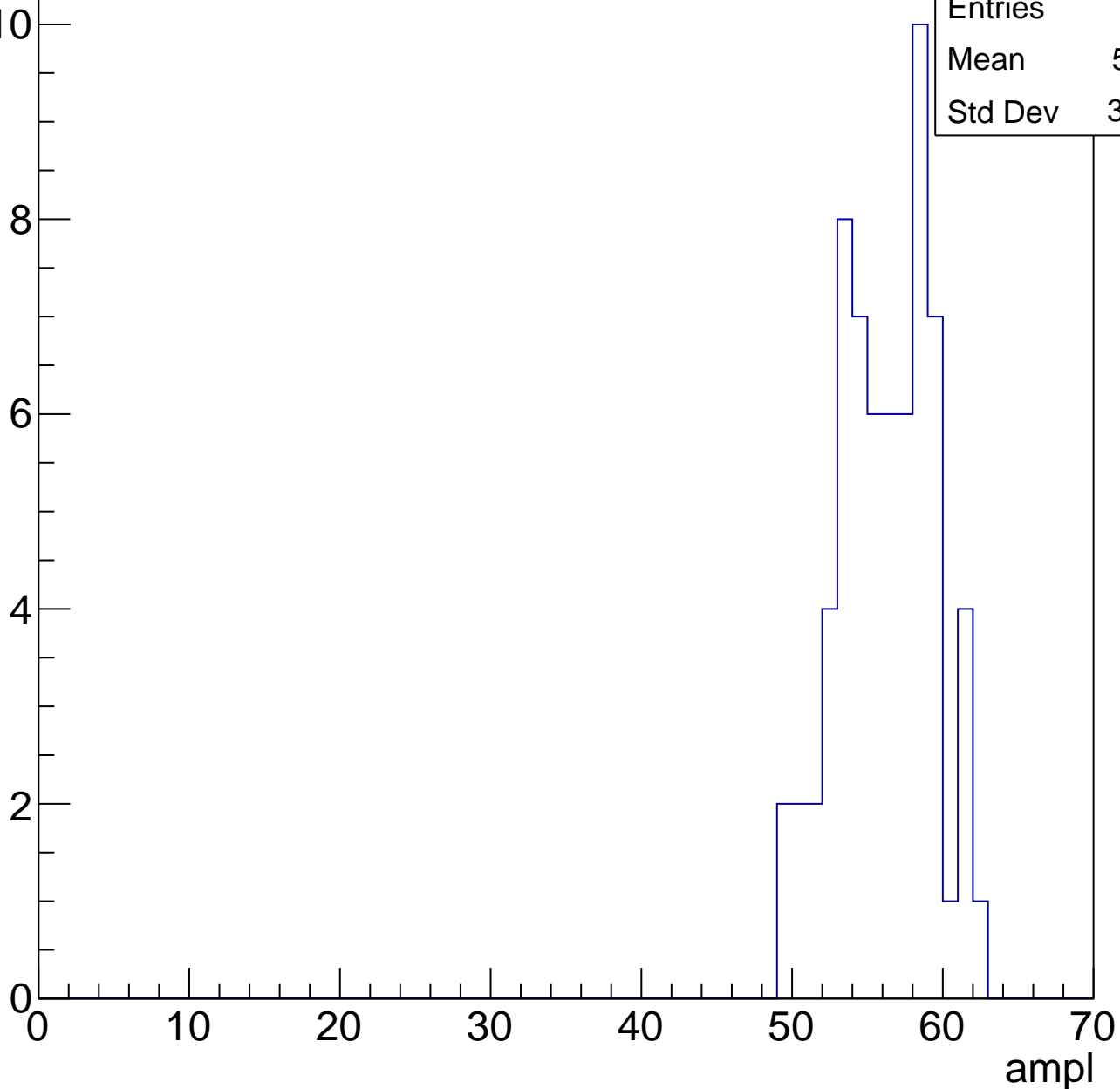


# B1L101S, U22-ch77, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	66
Mean	55.71
Std Dev	3.127



# B1L101S, U22-ch77, adc5

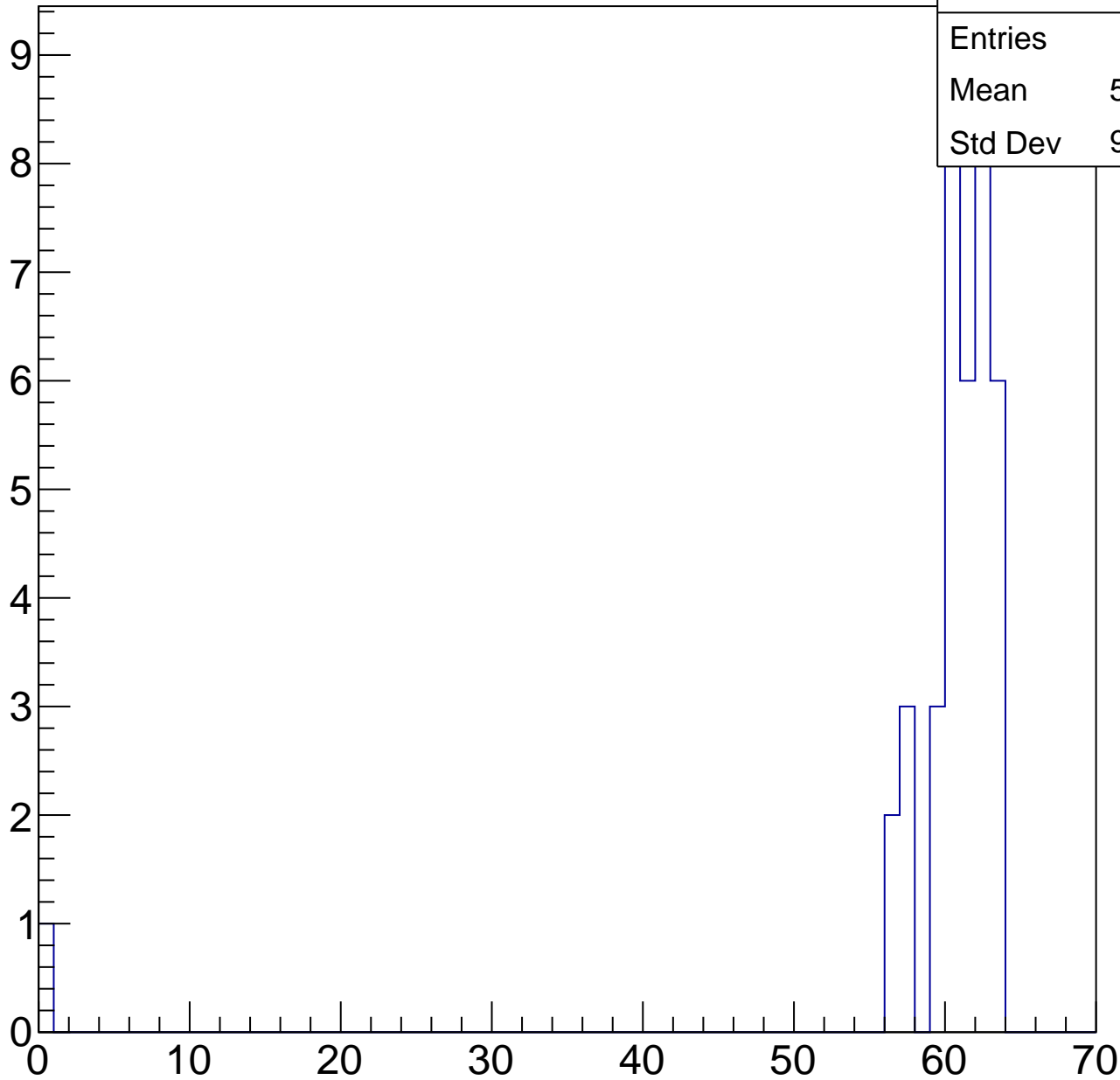
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	39
Mean	59.03
Std Dev	9.768

ampl



# B1L101S, U22-ch77, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	2
Mean	63
Std Dev	0

0 10 20 30 40 50 60 70

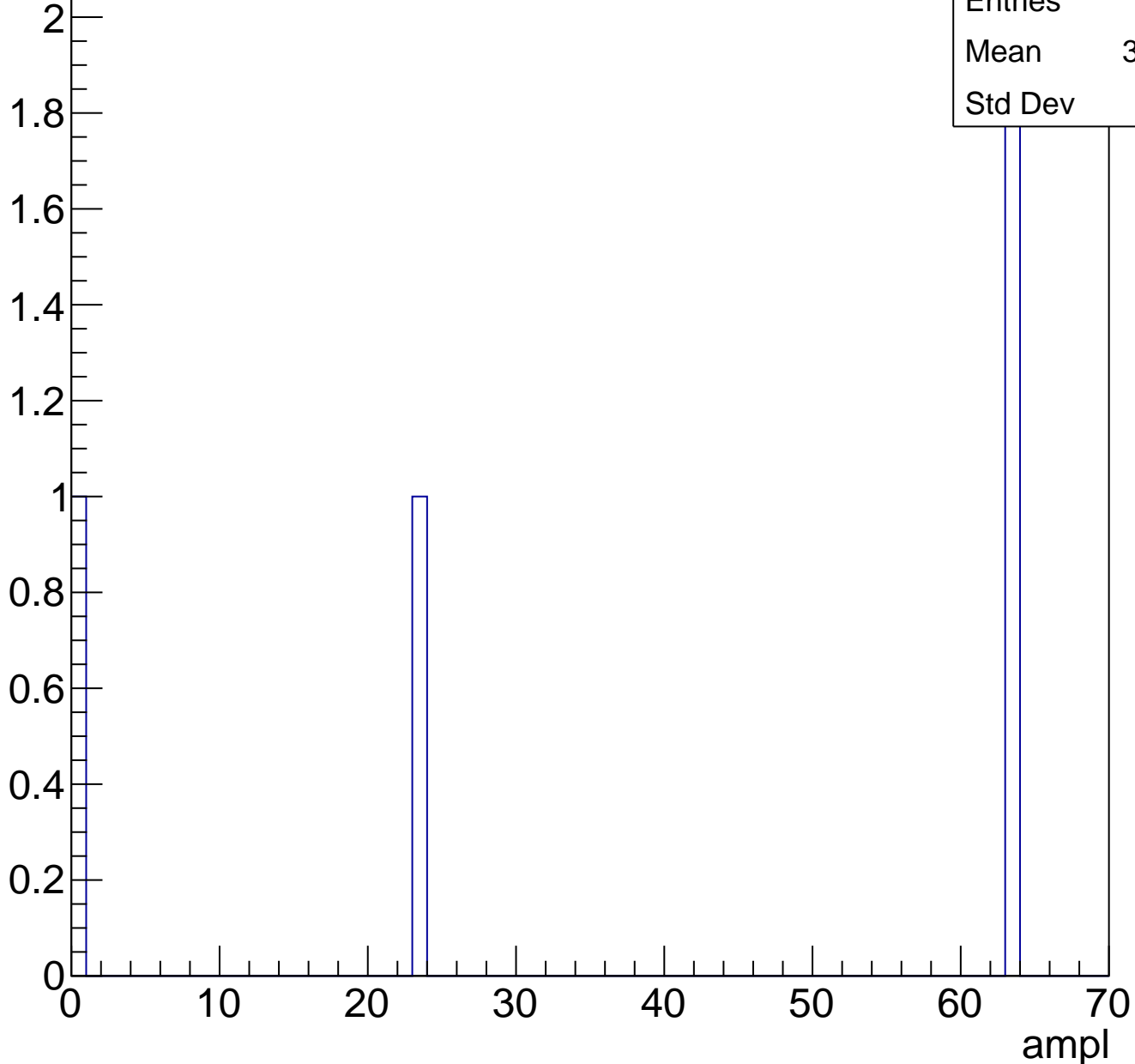
ampl



# B1L101S, U22-ch77, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U22-ch78, adc0

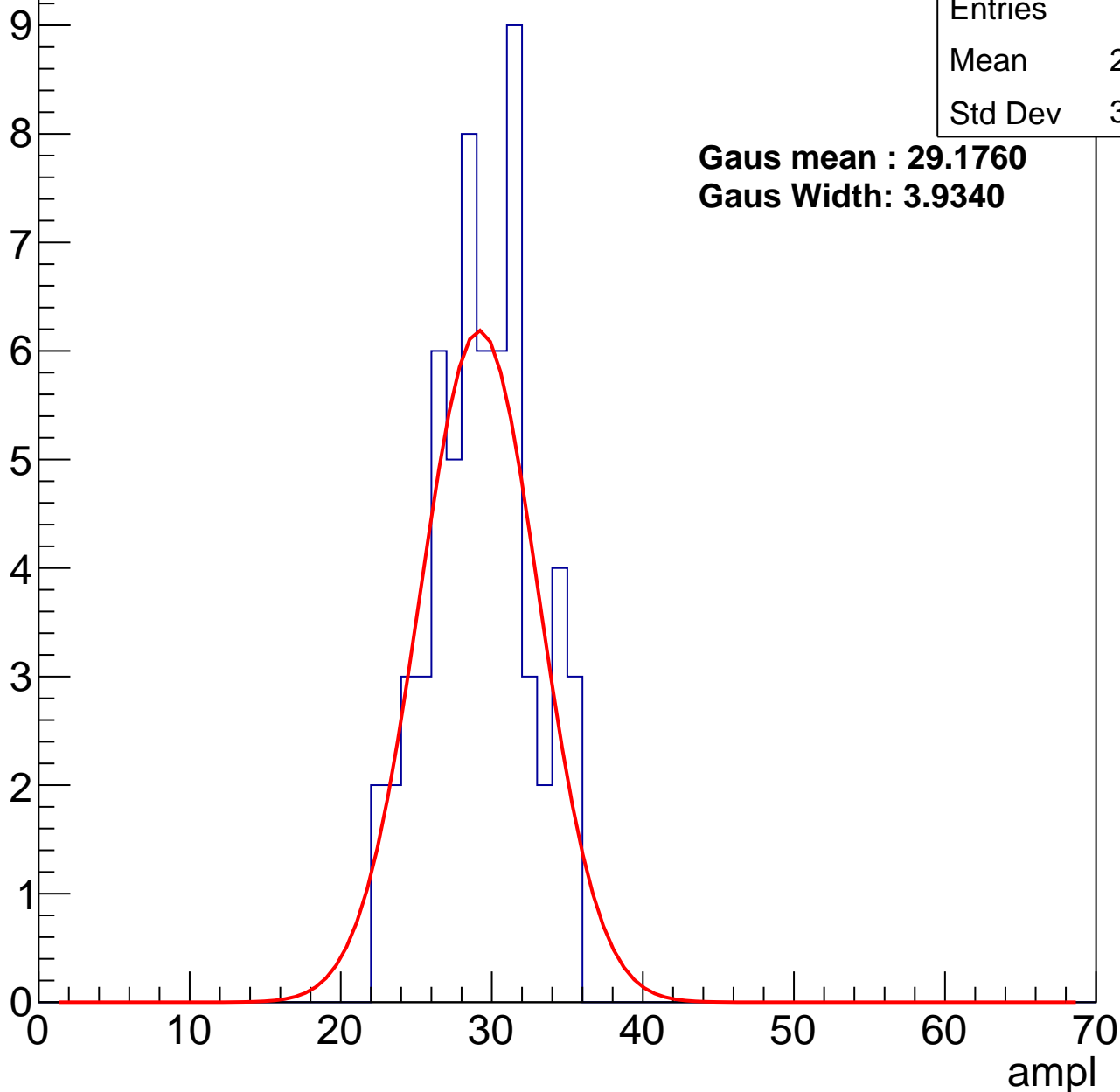
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	28.84
Std Dev	3.318

**Gaus mean : 29.1760**

**Gaus Width: 3.9340**

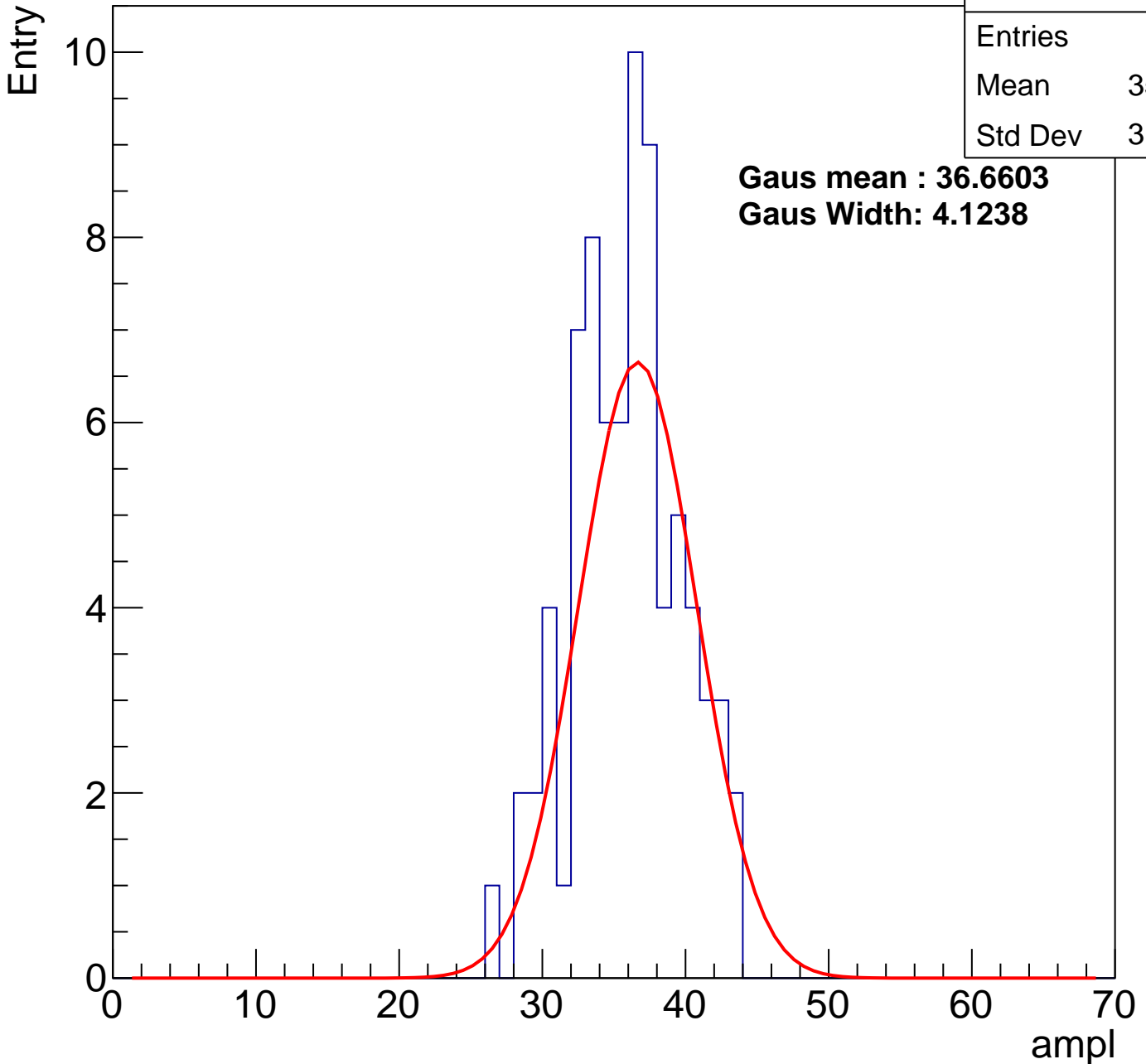


# B1L101S, U22-ch78, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	77
Mean	35.43
Std Dev	3.778

**Gaus mean : 36.6603**  
**Gaus Width: 4.1238**



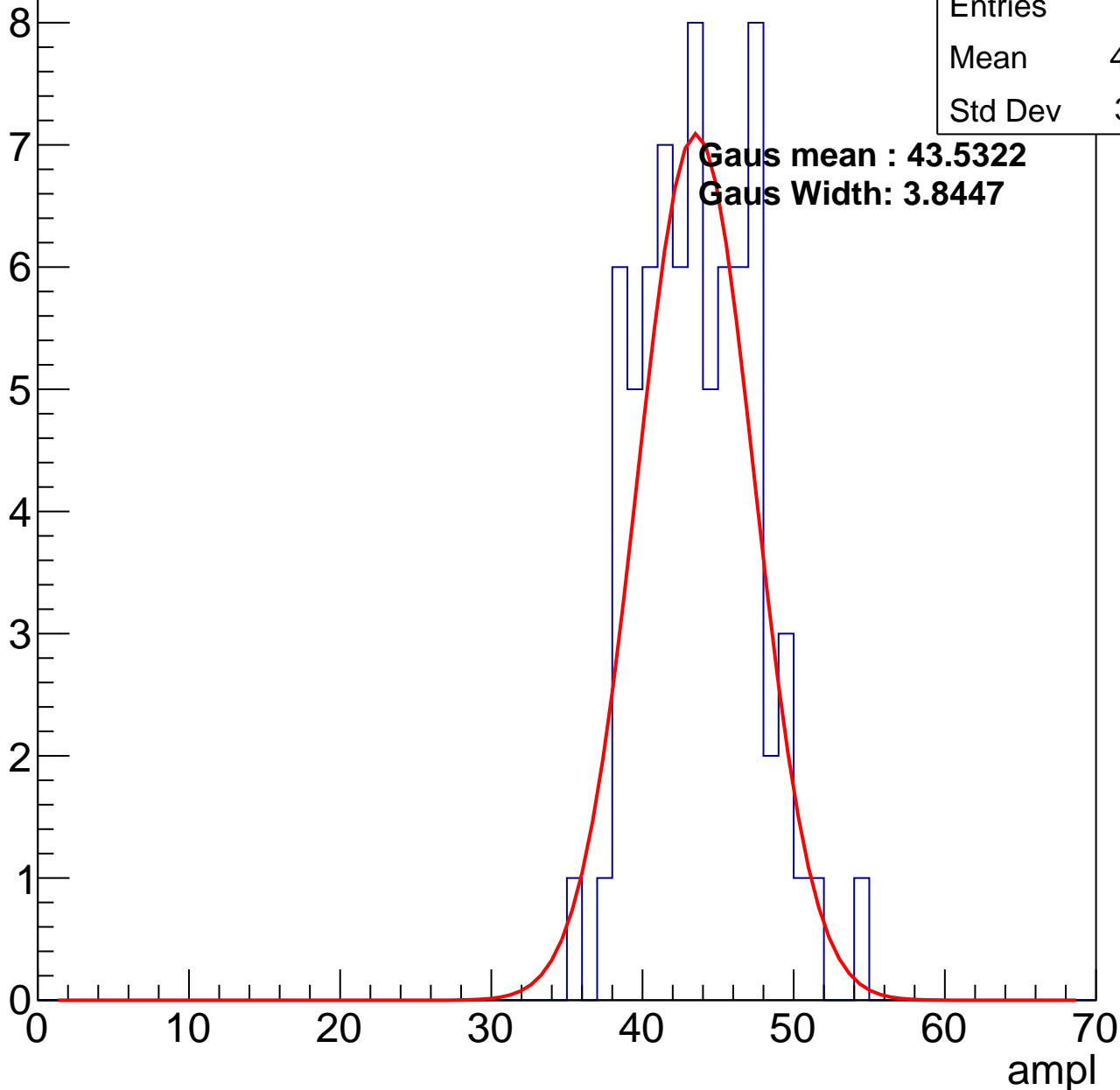
# B1L101S, U22-ch78, adc2

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	73
Mean	43.26
Std Dev	3.731

**Gaus mean : 43.5322**  
**Gaus Width: 3.8447**

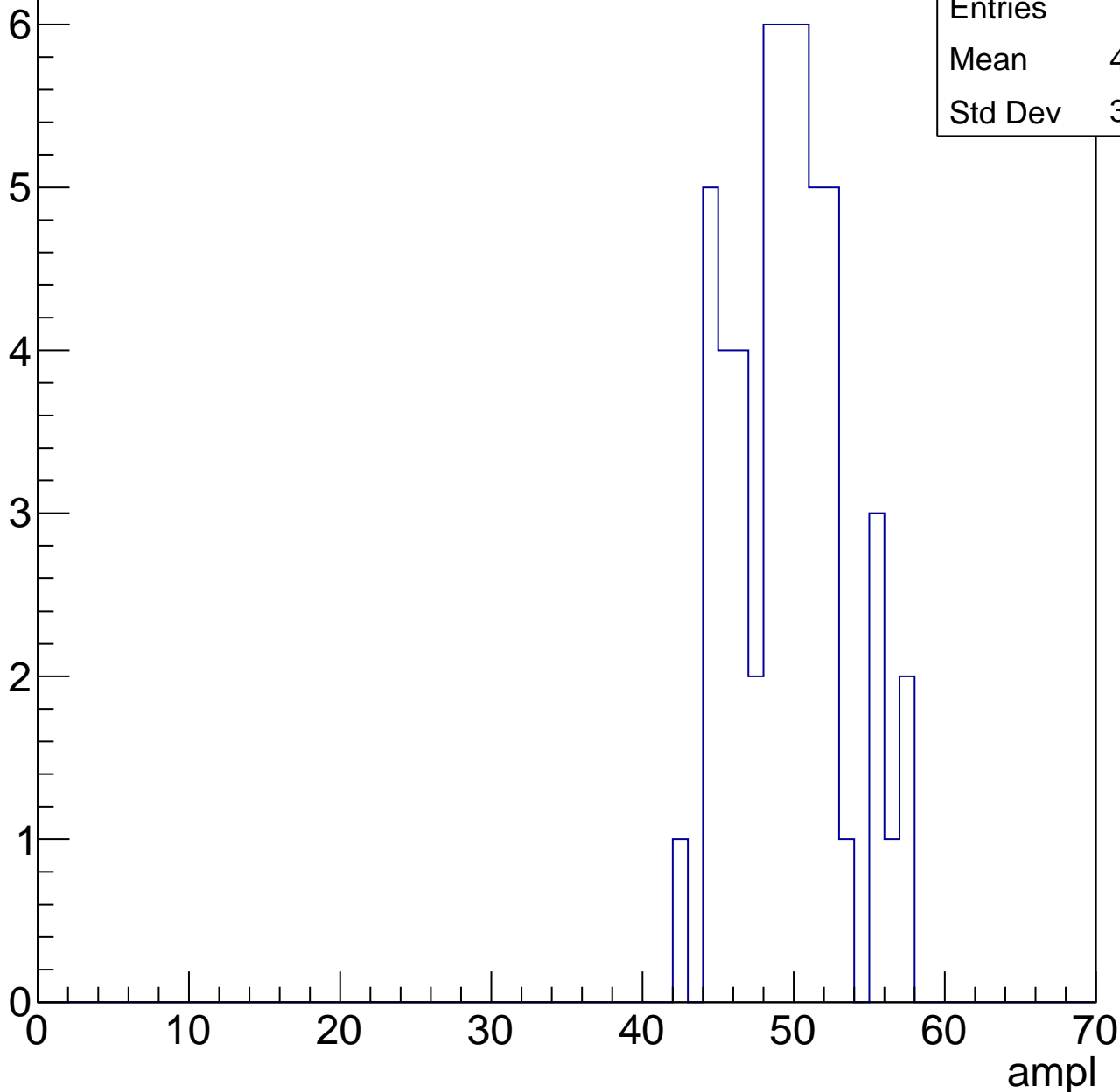


# B1L101S, U22-ch78, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	51
Mean	49.12
Std Dev	3.595

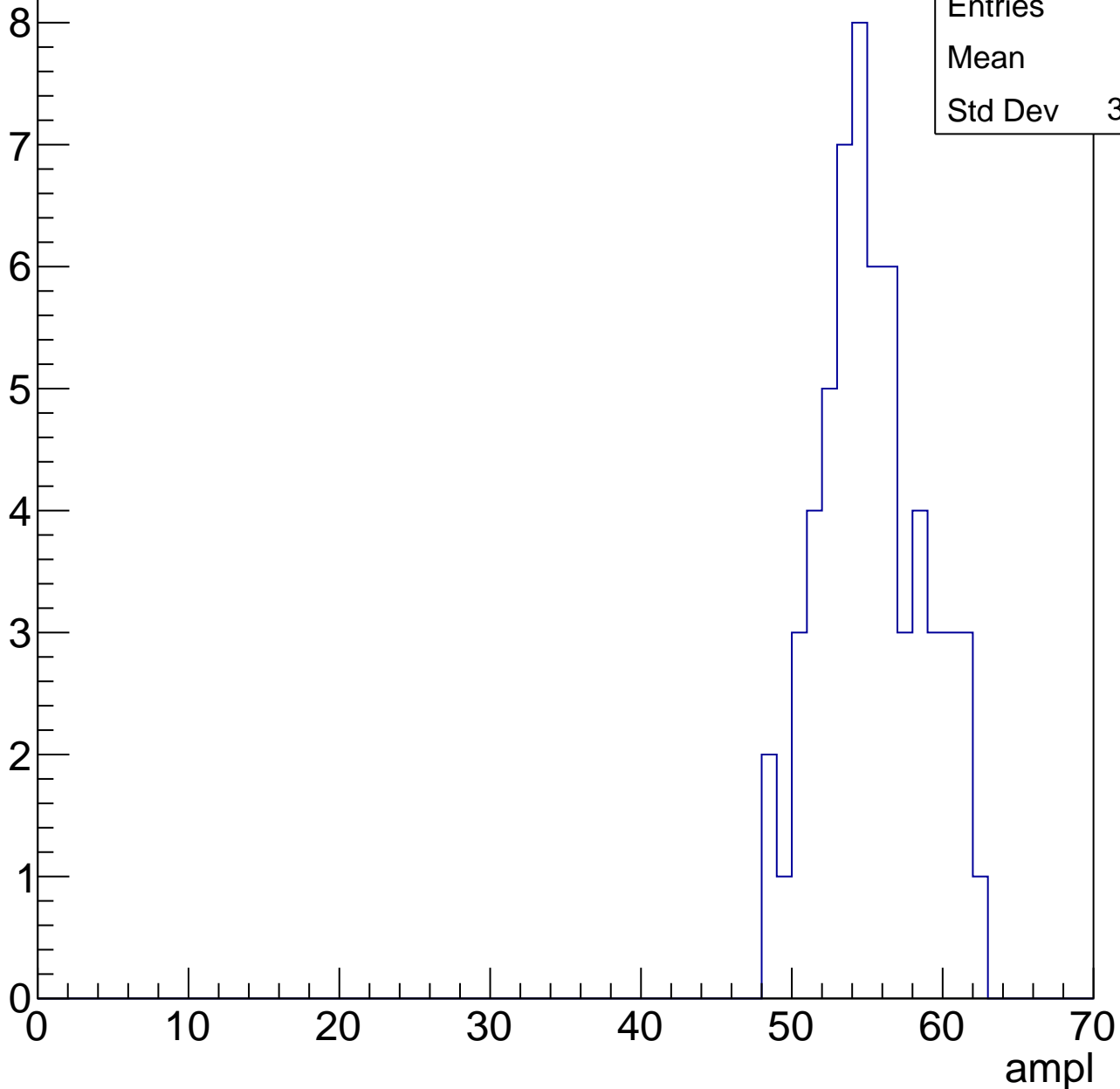


# B1L101S, U22-ch78, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	59
Mean	54.8
Std Dev	3.409

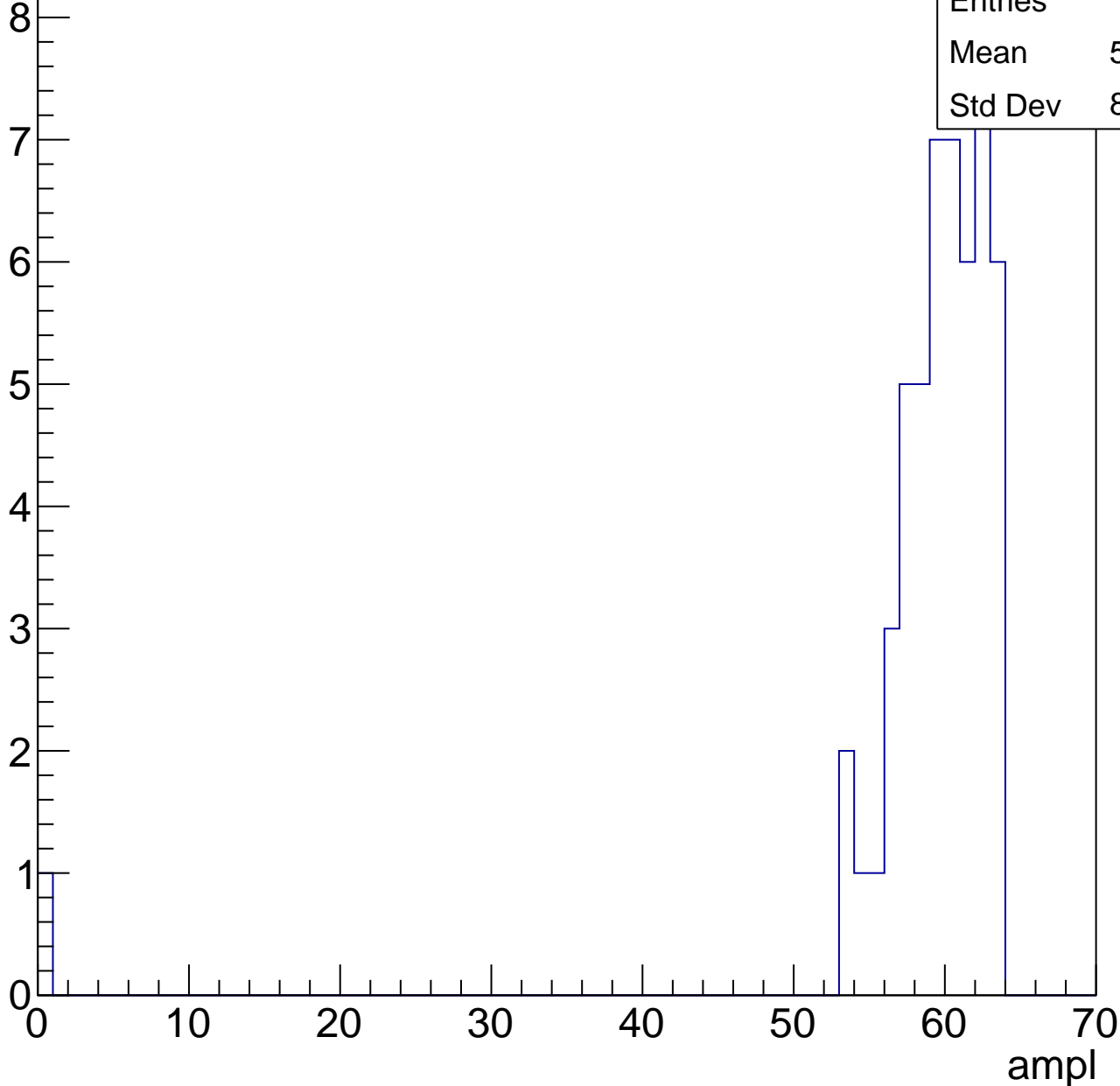


# B1L101S, U22-ch78, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

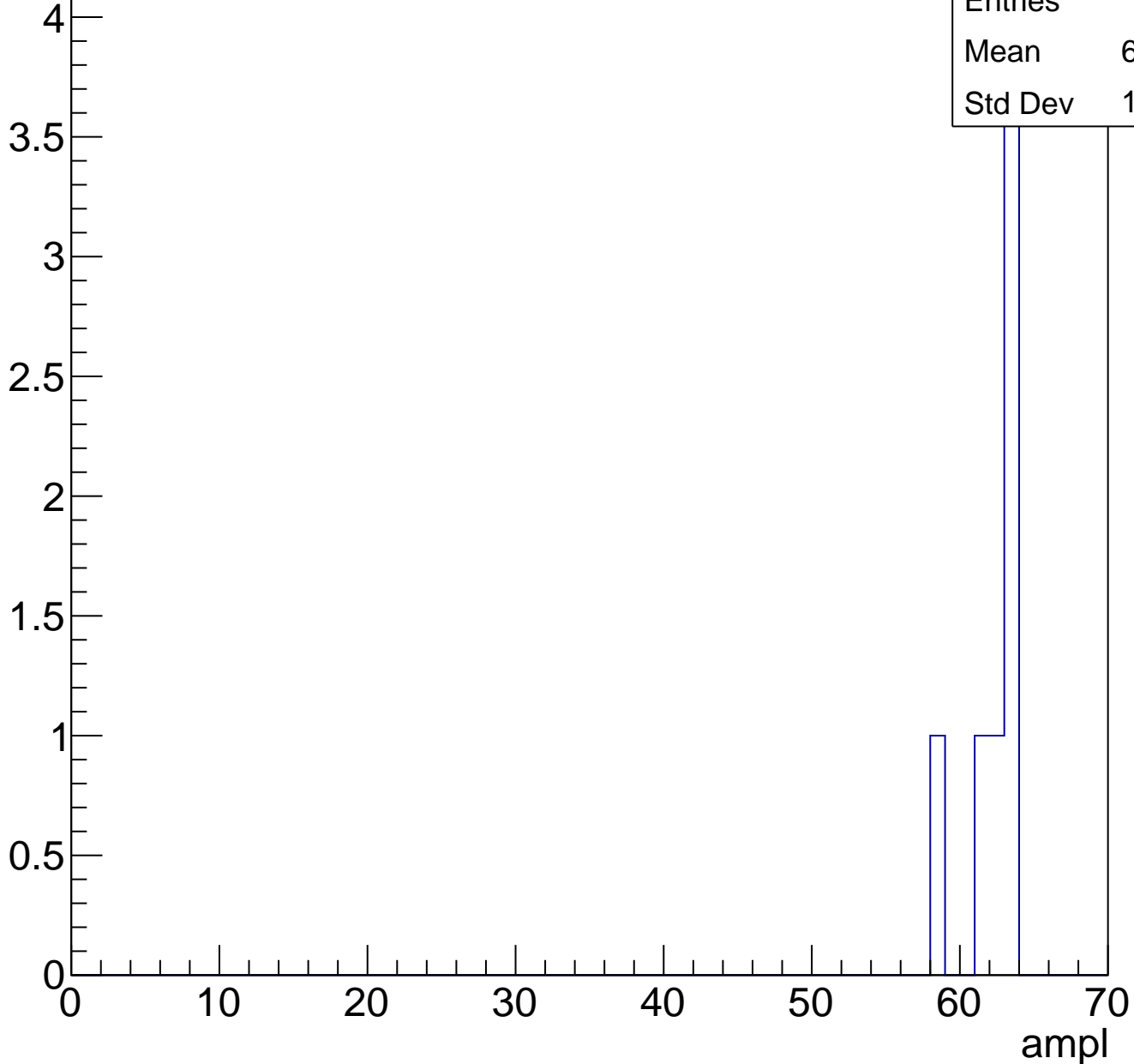
Entries	52
Mean	58.29
Std Dev	8.569



# B1L101S, U22-ch78, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U22-ch78, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U22-ch79, adc0

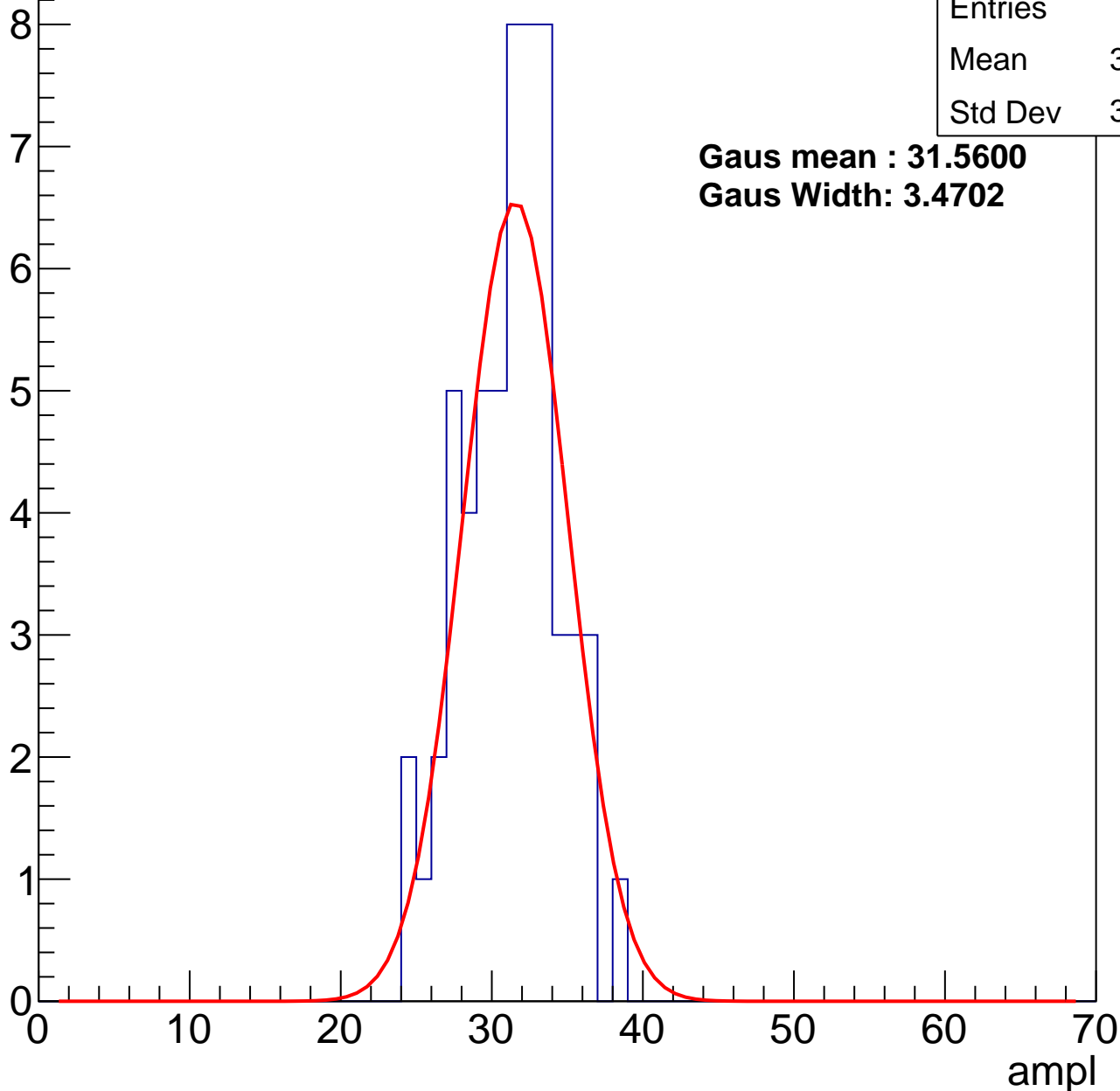
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	58
Mean	30.83
Std Dev	3.114

**Gaus mean : 31.5600**

**Gaus Width: 3.4702**



# B1L101S, U22-ch79, adc1

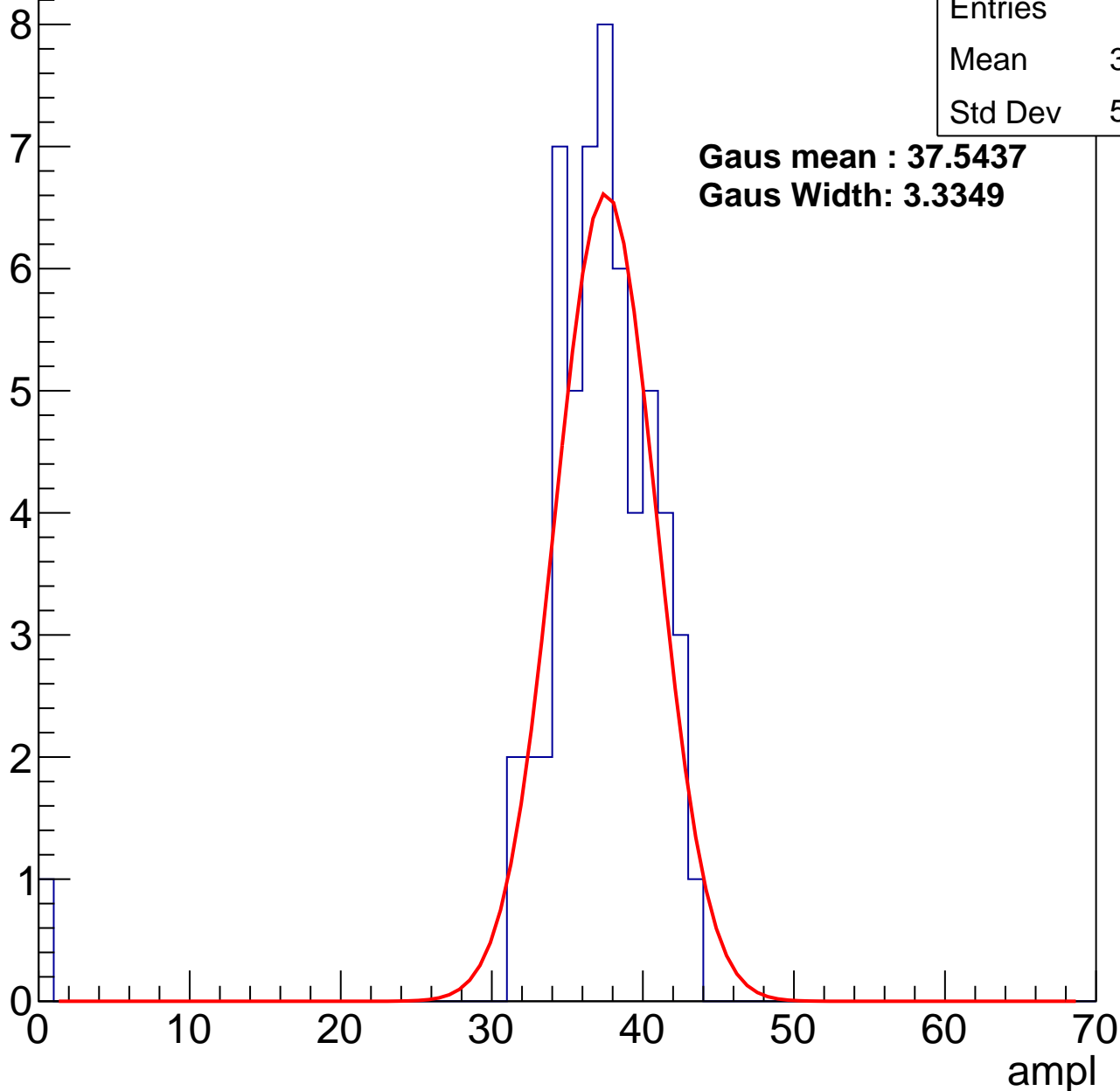
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	57
Mean	36.32
Std Dev	5.664

**Gaus mean : 37.5437**

**Gaus Width: 3.3349**



# B1L101S, U22-ch79, adc2

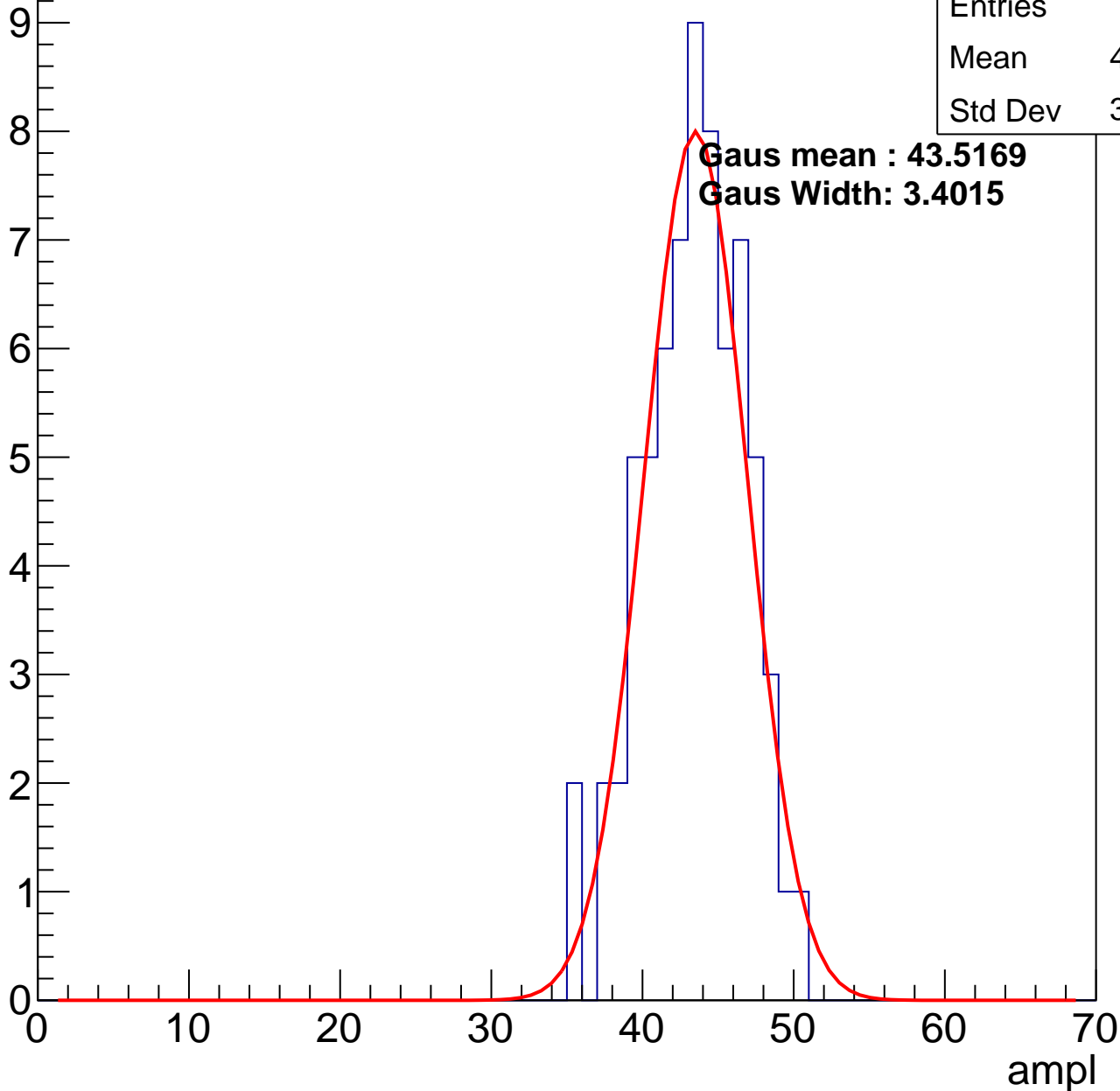
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	42.96
Std Dev	3.277

**Gaus mean : 43.5169**

**Gaus Width: 3.4015**

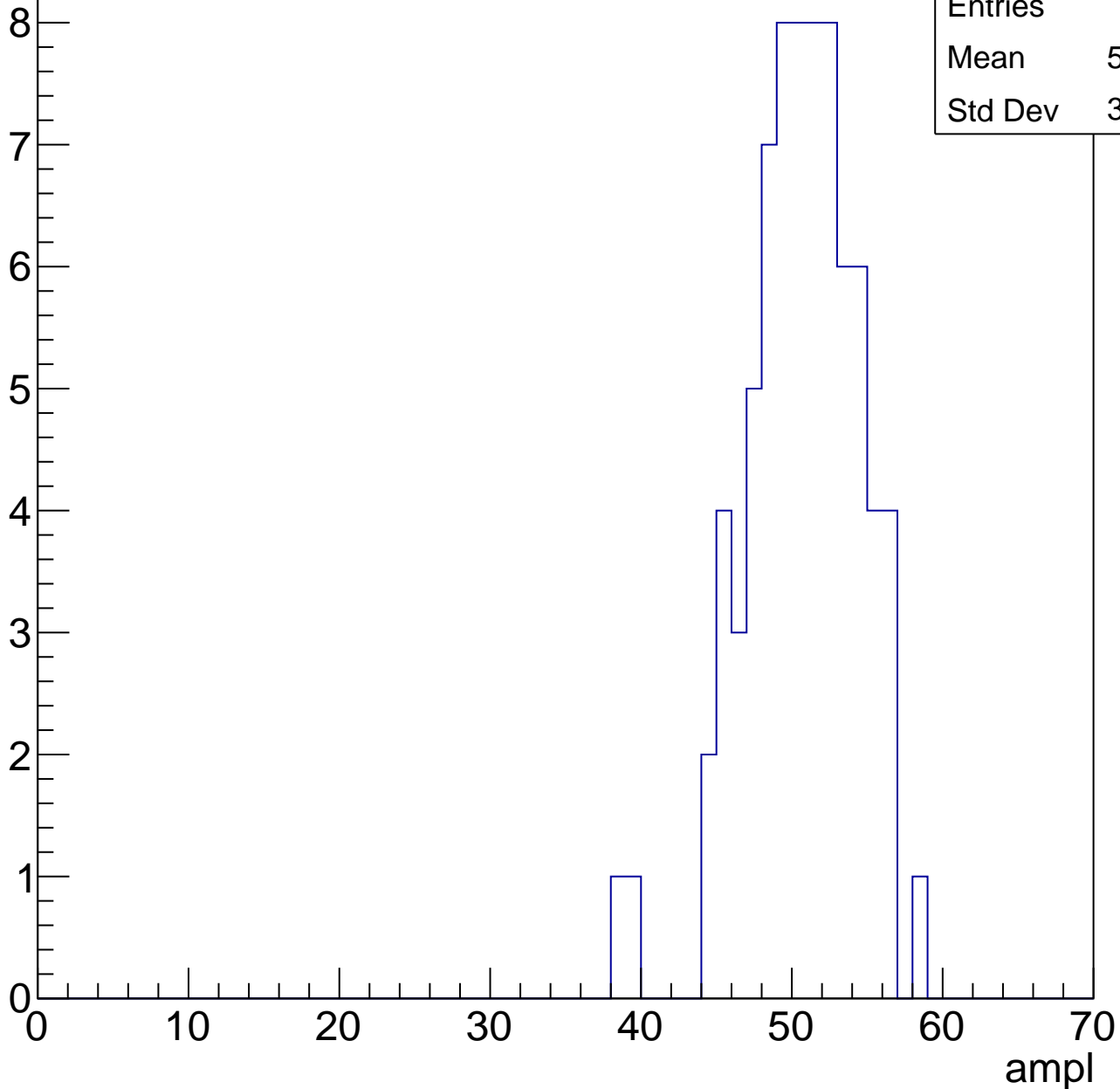


# B1L101S, U22-ch79, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	76
Mean	50.18
Std Dev	3.737

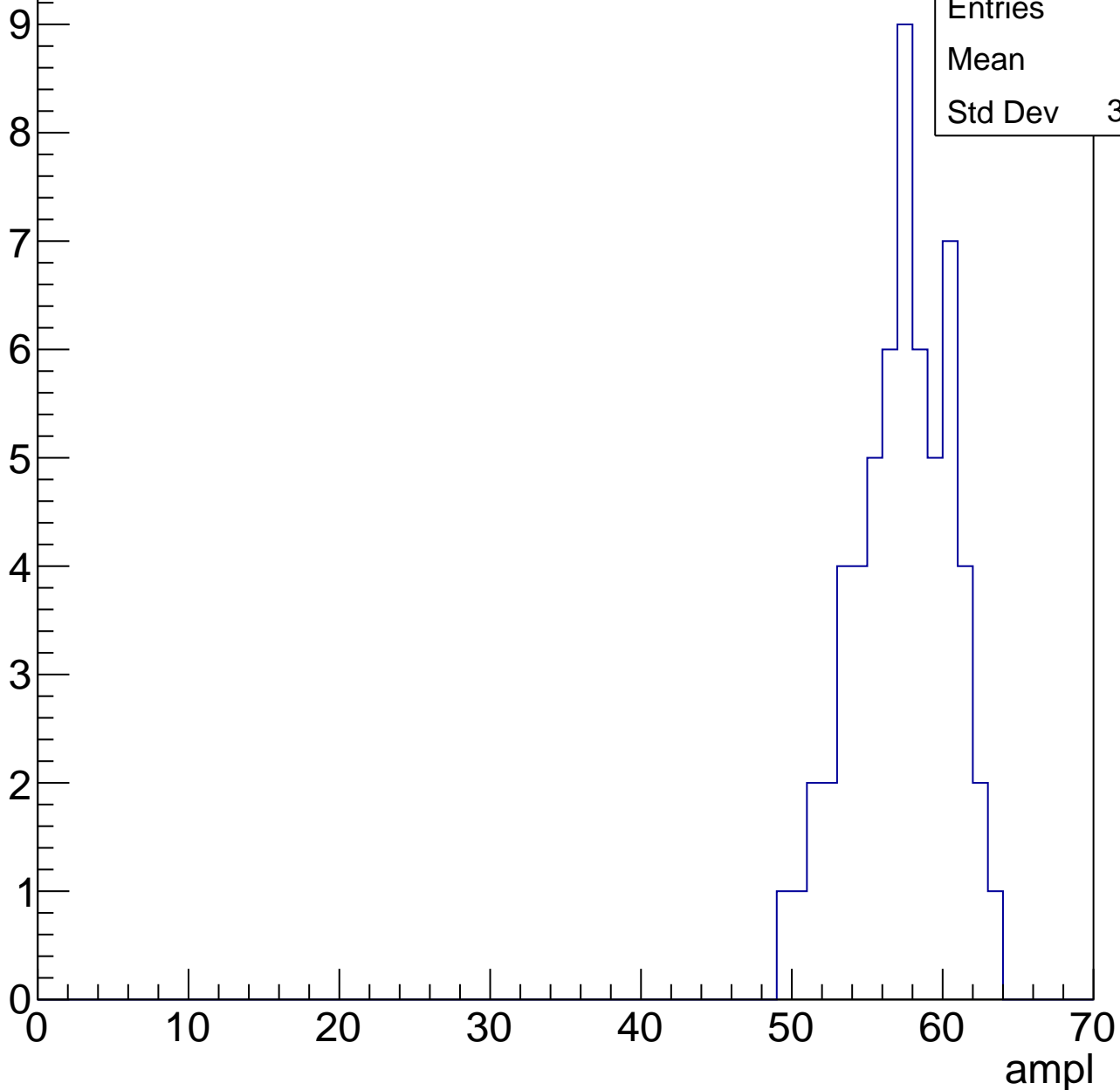


# B1L101S, U22-ch79, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	59
Mean	56.8
Std Dev	3.182

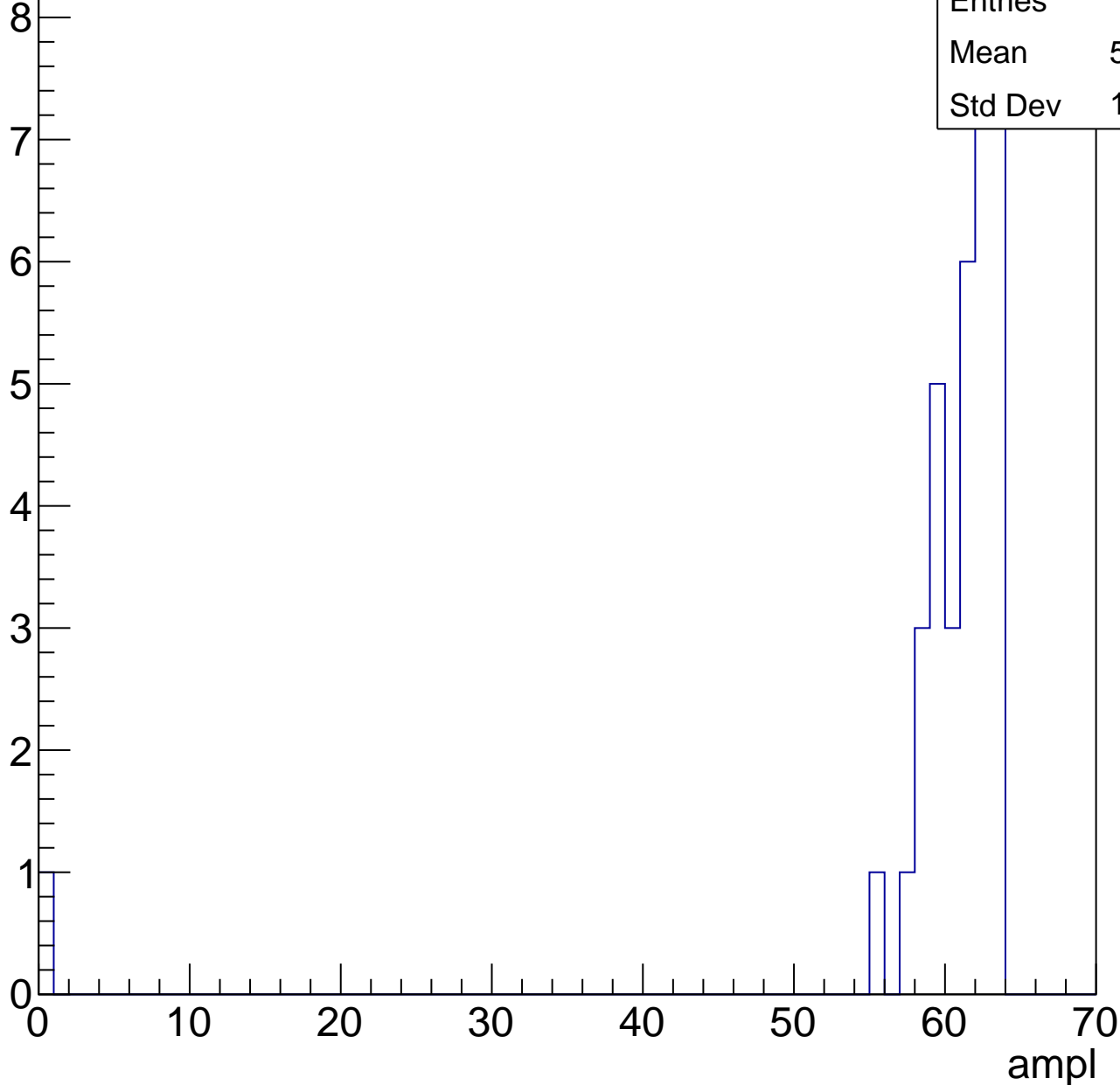


# B1L101S, U22-ch79, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	36
Mean	59.08
Std Dev	10.18



# B1L101S, U22-ch79, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U22-ch79, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U22-ch80, adc0

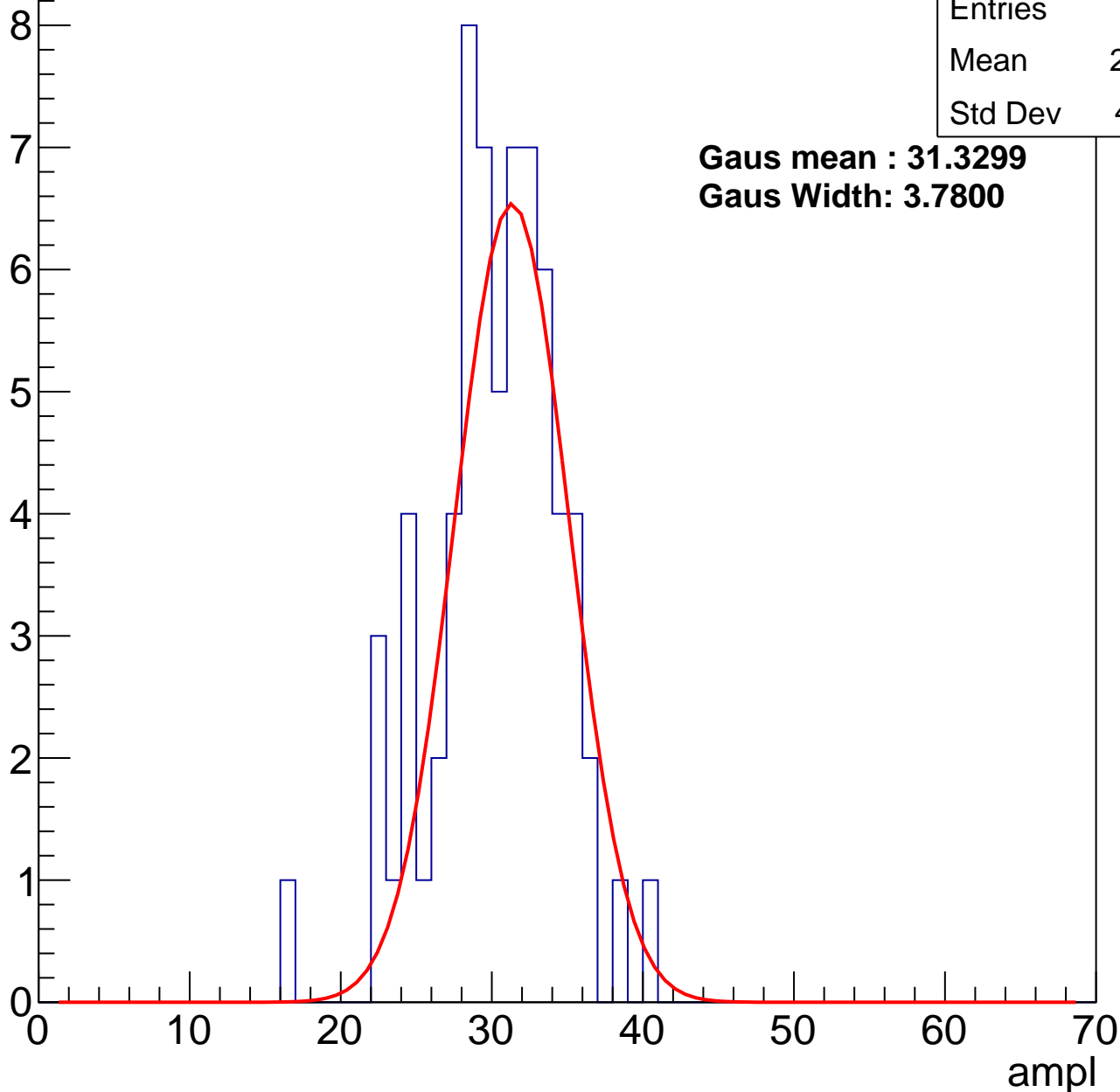
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	29.82
Std Dev	4.201

**Gaus mean : 31.3299**

**Gaus Width: 3.7800**



# B1L101S, U22-ch80, adc1

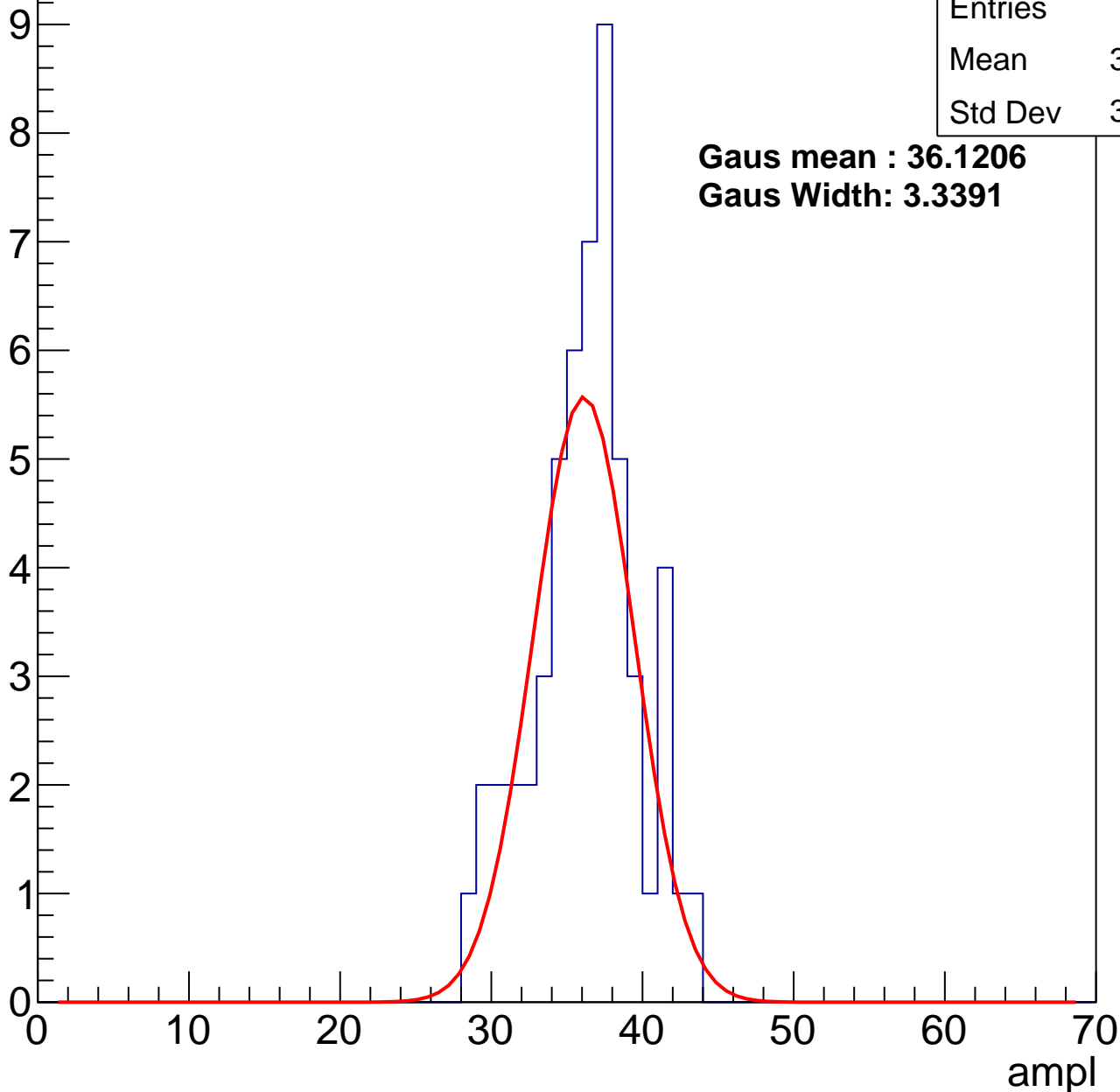
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	54
Mean	35.78
Std Dev	3.398

**Gaus mean : 36.1206**

**Gaus Width: 3.3391**



# B1L101S, U22-ch80, adc2

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	78
Mean	42.4
Std Dev	3.603

**Gaus mean : 43.0604**

**Gaus Width: 3.1638**

10

8

6

4

2

0

ampl

0

10

20

30

40

50

60

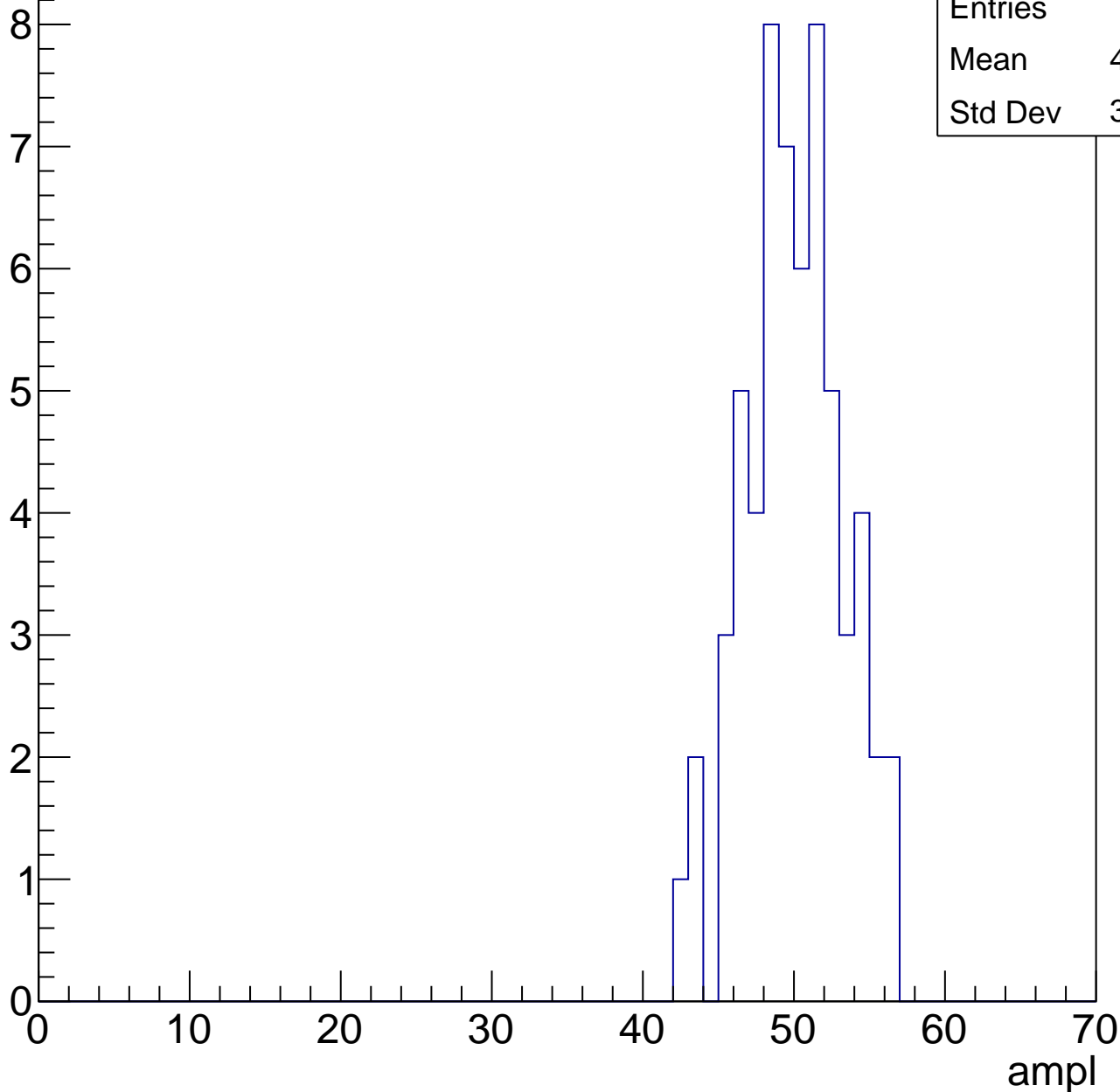
70

# B1L101S, U22-ch80, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

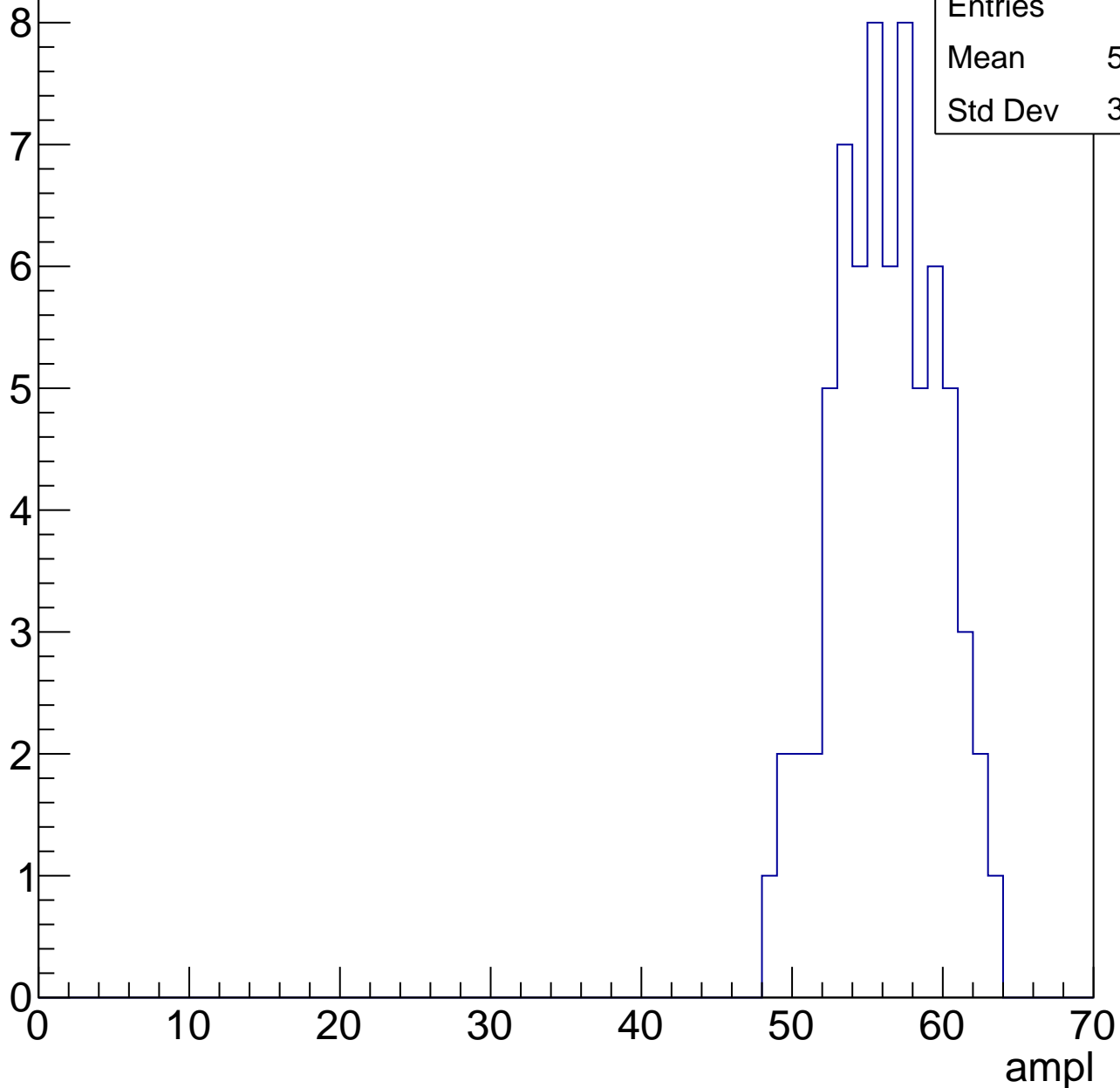
Entries	60
Mean	49.55
Std Dev	3.217



# B1L101S, U22-ch80, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

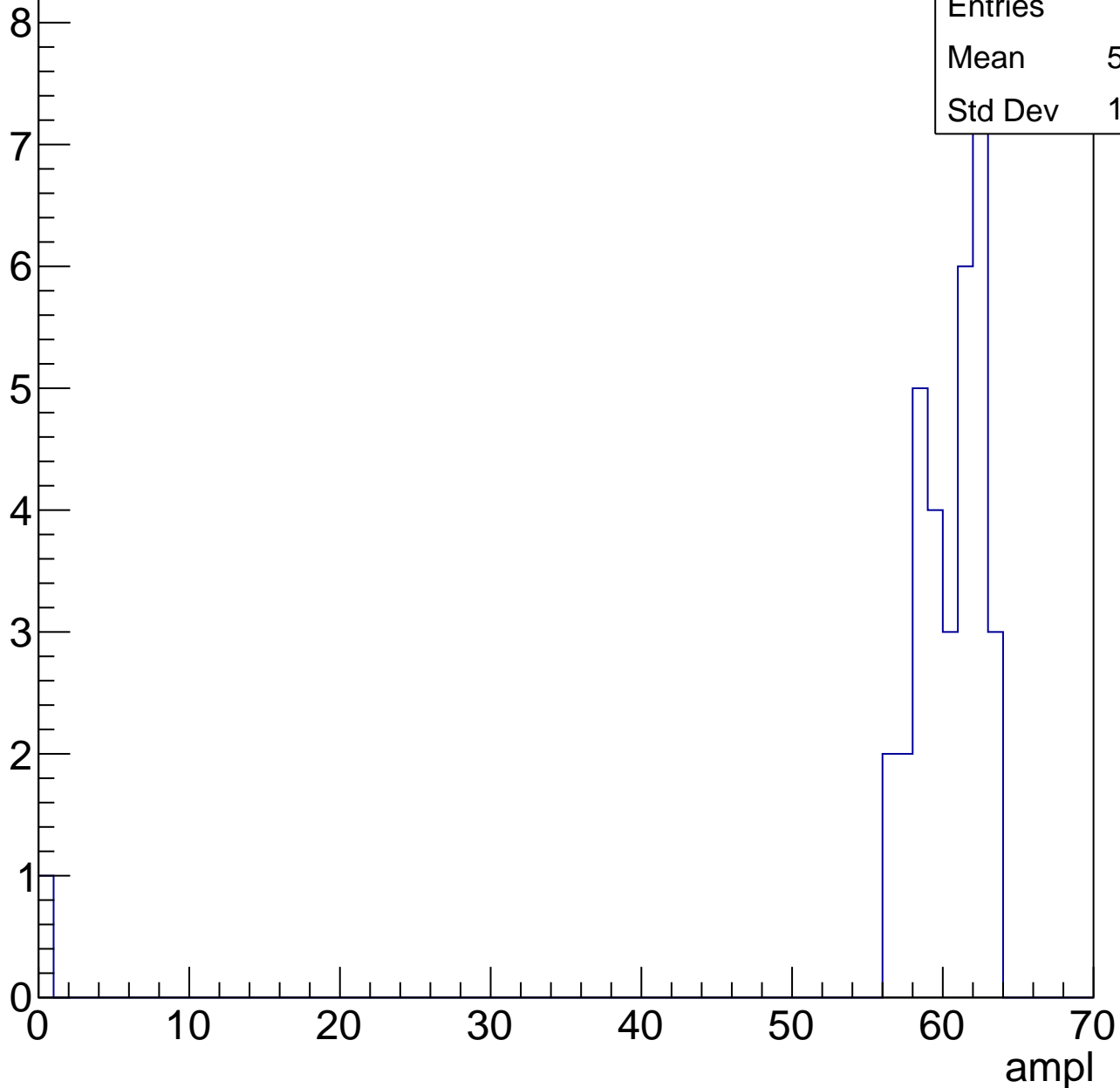


# B1L101S, U22-ch80, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	34
Mean	58.32
Std Dev	10.35



# B1L101S, U22-ch80, adc6

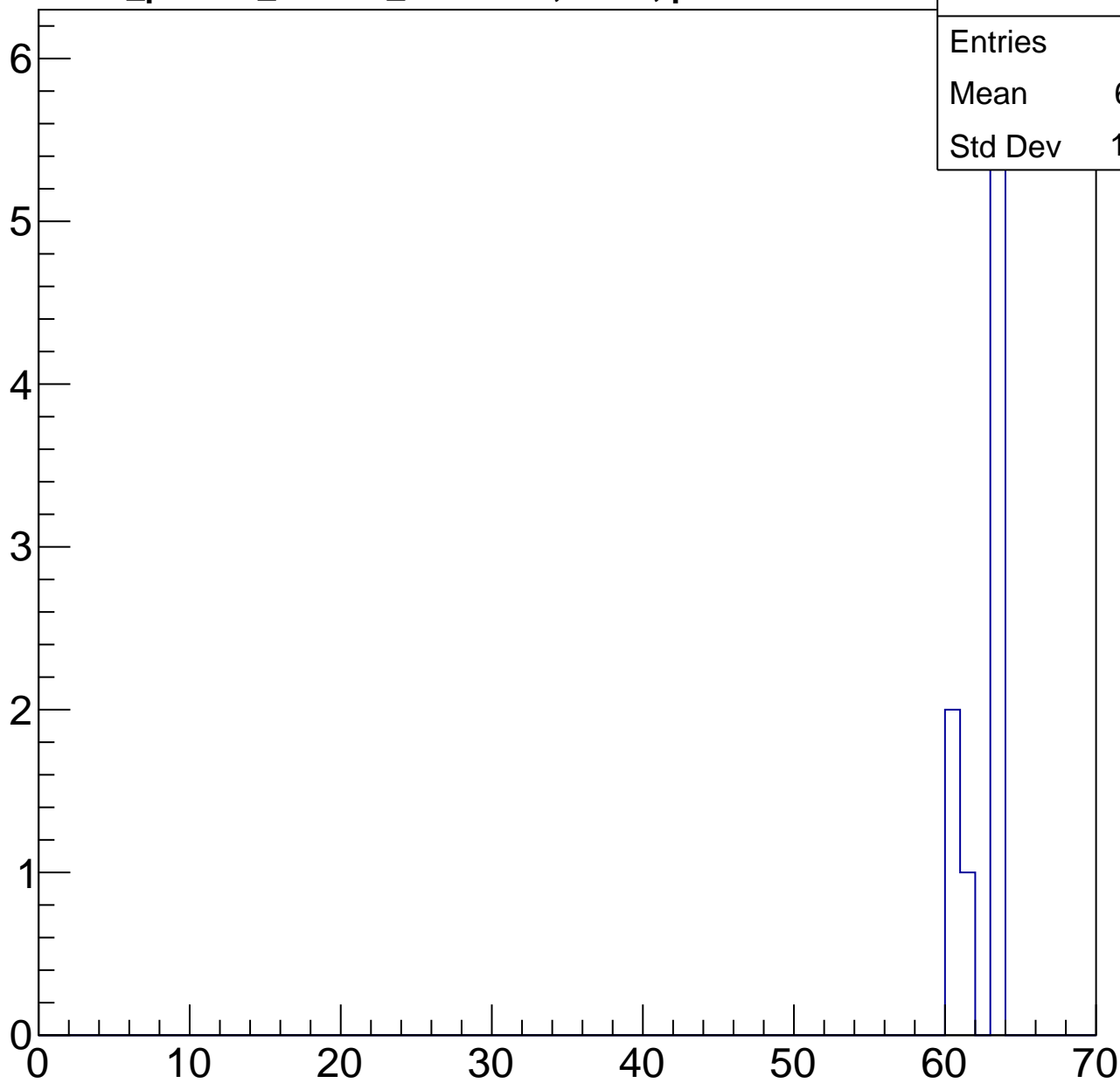
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

6  
5  
4  
3  
2  
1  
0

Entries	9
Mean	62.11
Std Dev	1.286

ampl





# B1L101S, U22-ch80, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U22-ch81, adc0

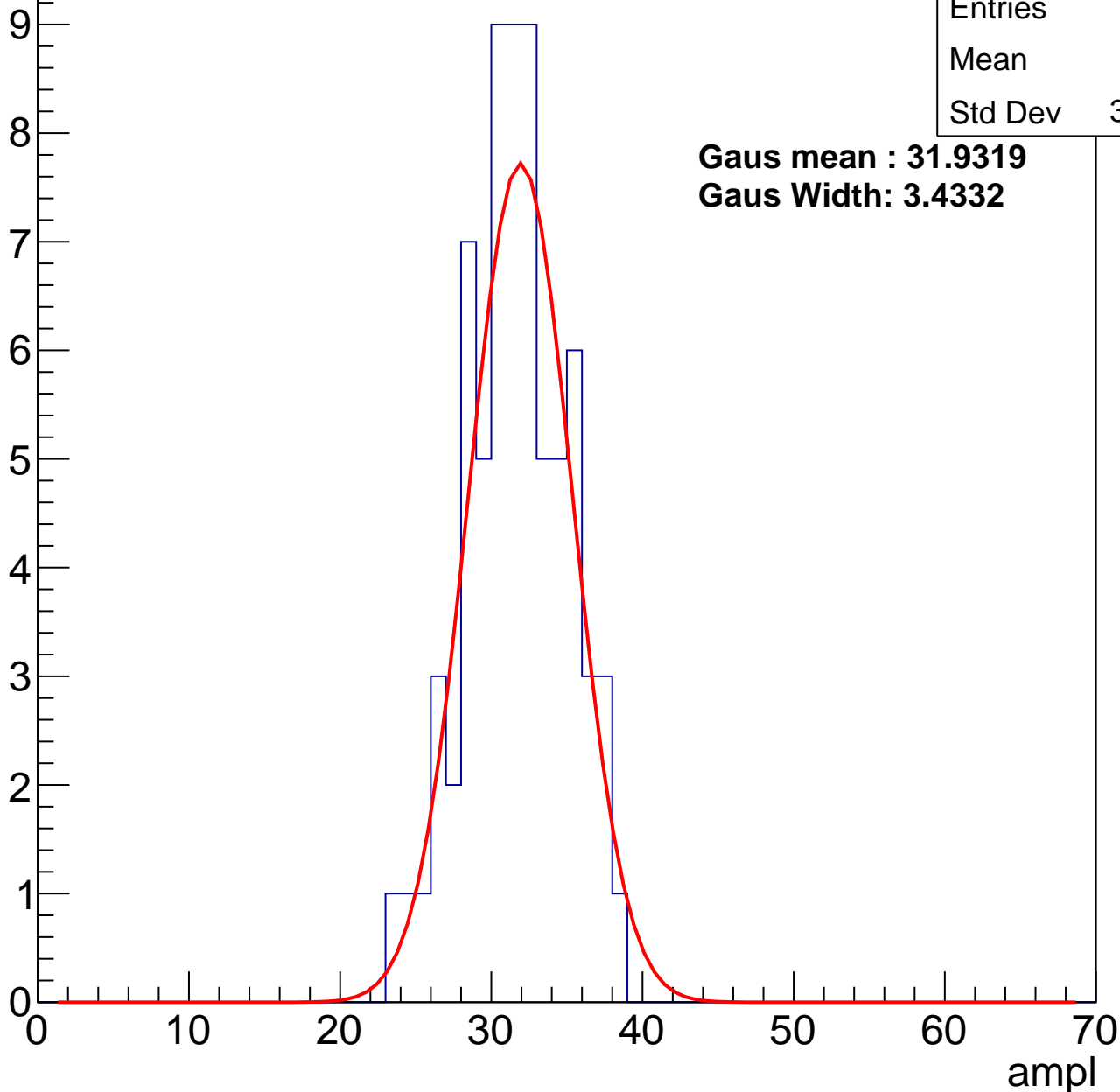
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	31.2
Std Dev	3.267

**Gaus mean : 31.9319**

**Gaus Width: 3.4332**



# B1L101S, U22-ch81, adc1

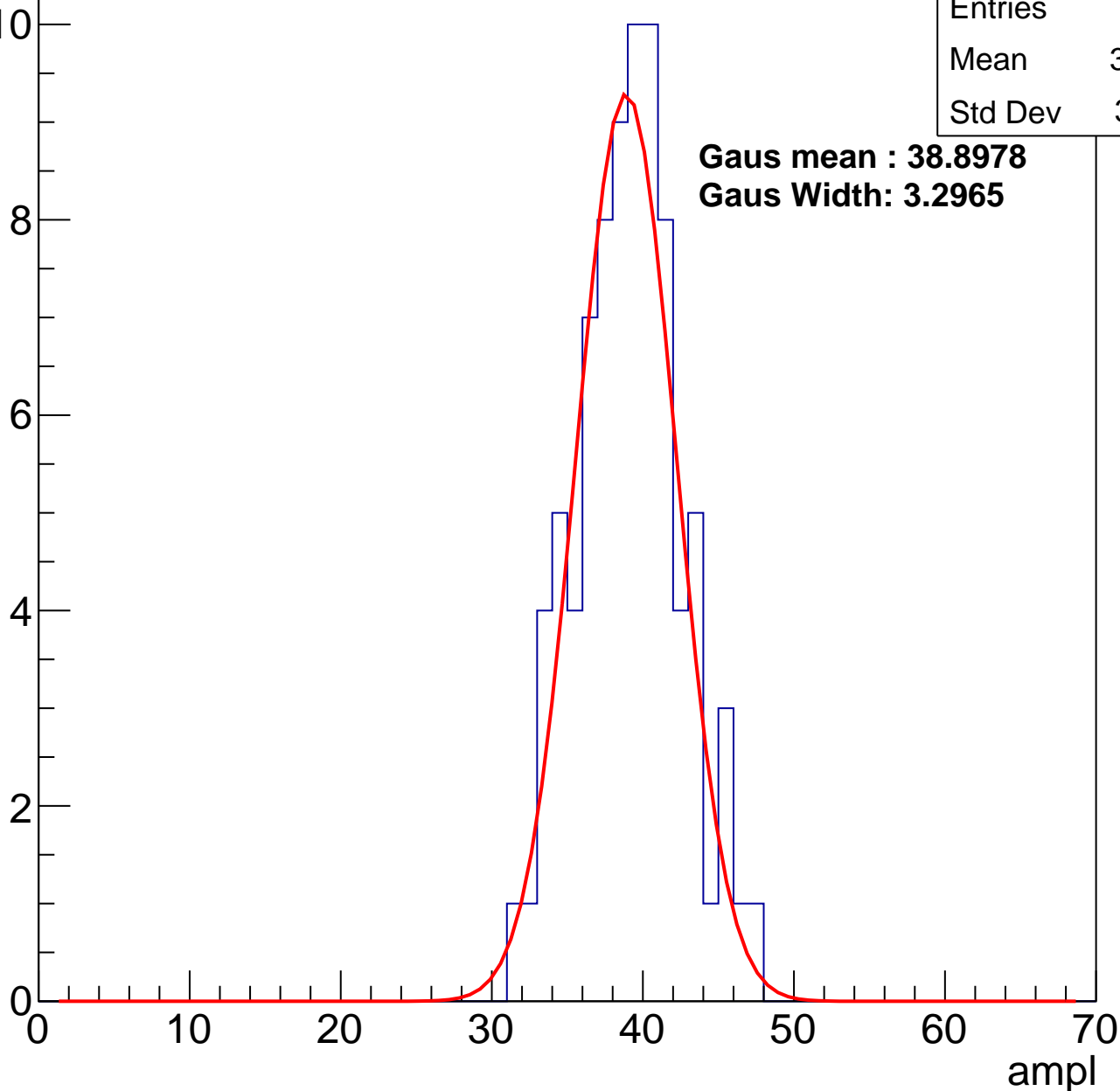
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	82
Mean	38.63
Std Dev	3.391

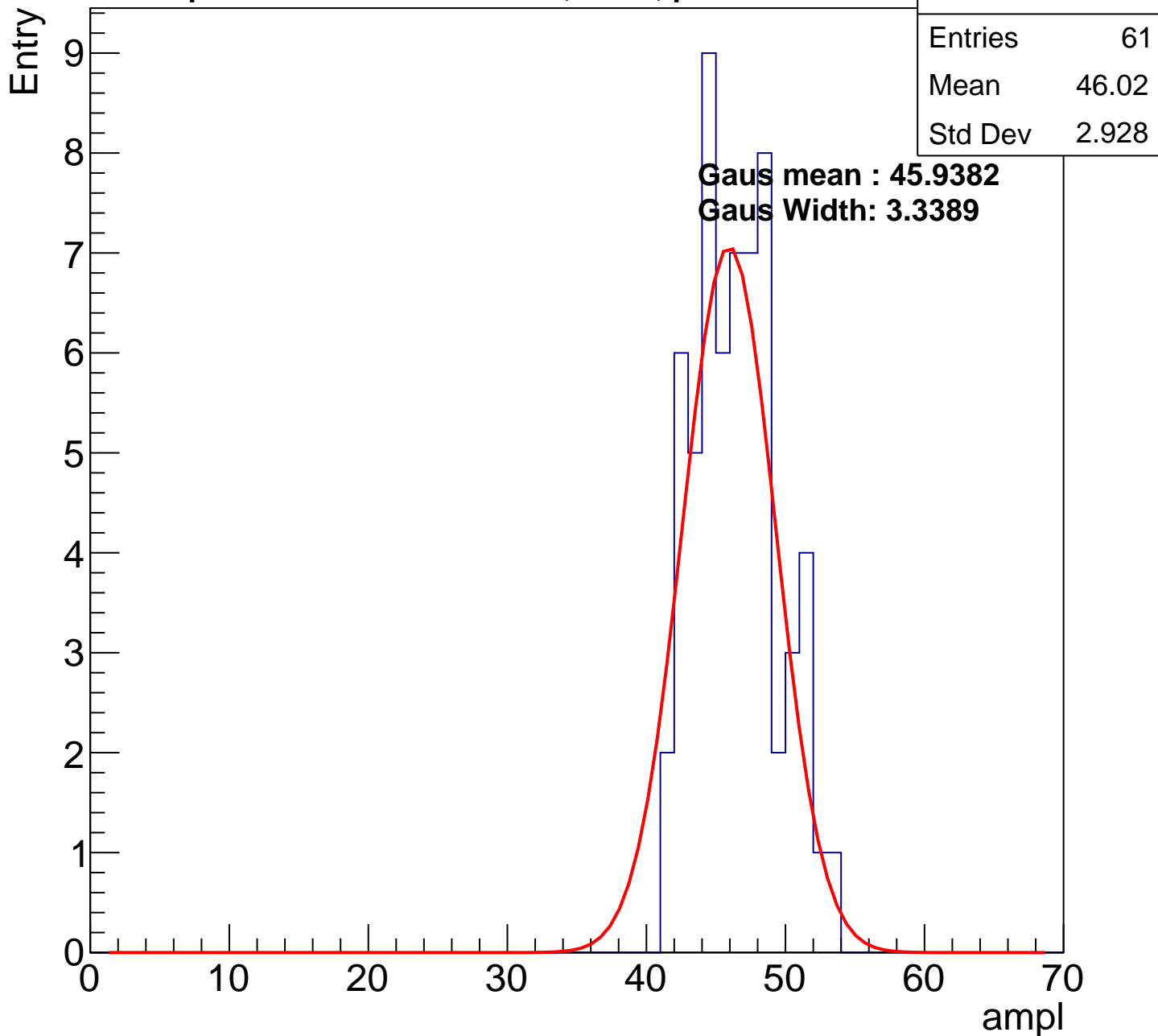
**Gaus mean : 38.8978**

**Gaus Width: 3.2965**



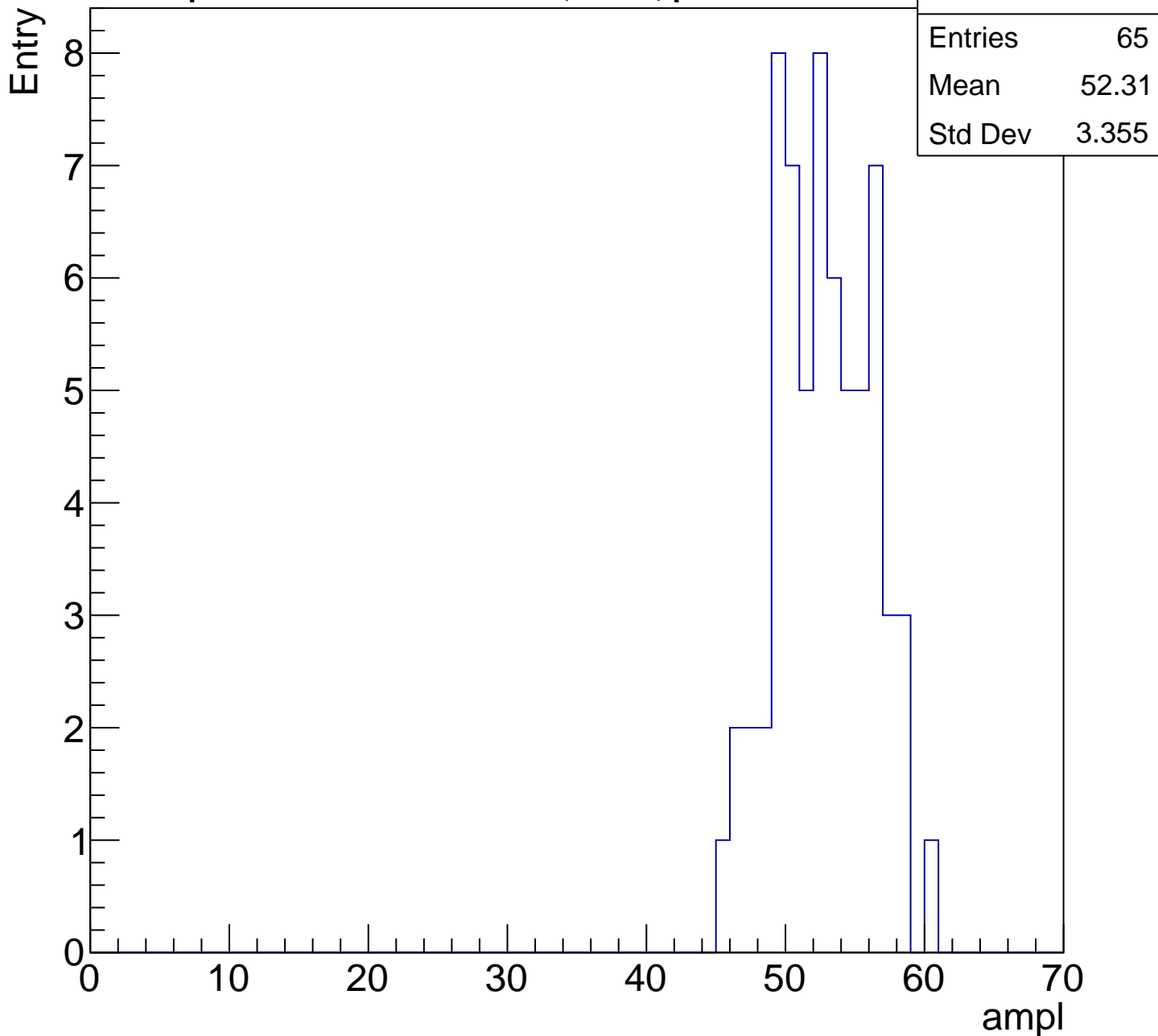
# B1L101S, U22-ch81, adc2

calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U22-ch81, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

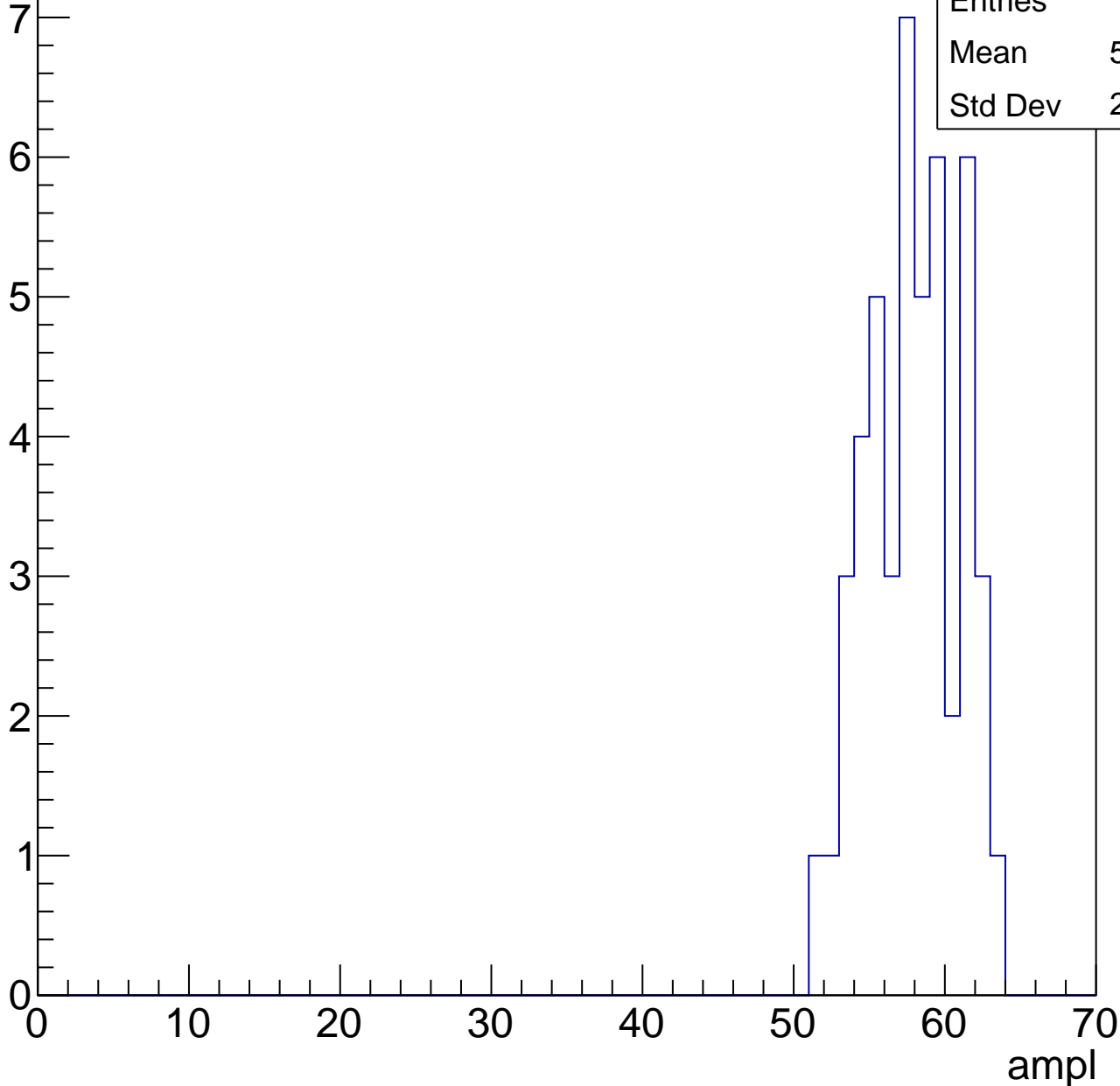


# B1L101S, U22-ch81, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	47
Mean	57.43
Std Dev	2.966

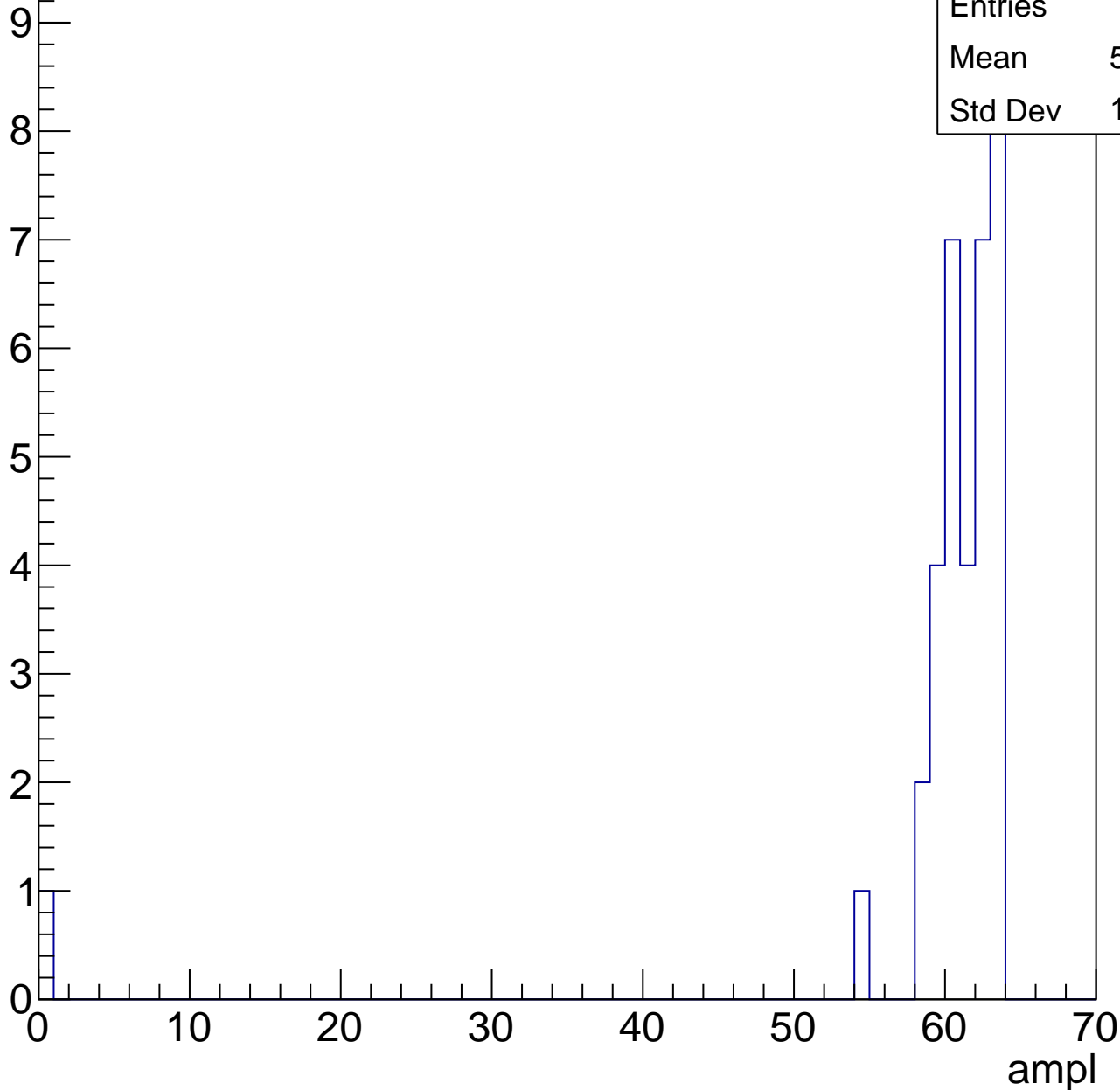


# B1L101S, U22-ch81, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	35
Mean	59.17
Std Dev	10.33



# B1L101S, U22-ch81, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0



# B1L101S, U22-ch81, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U22-ch82, adc0

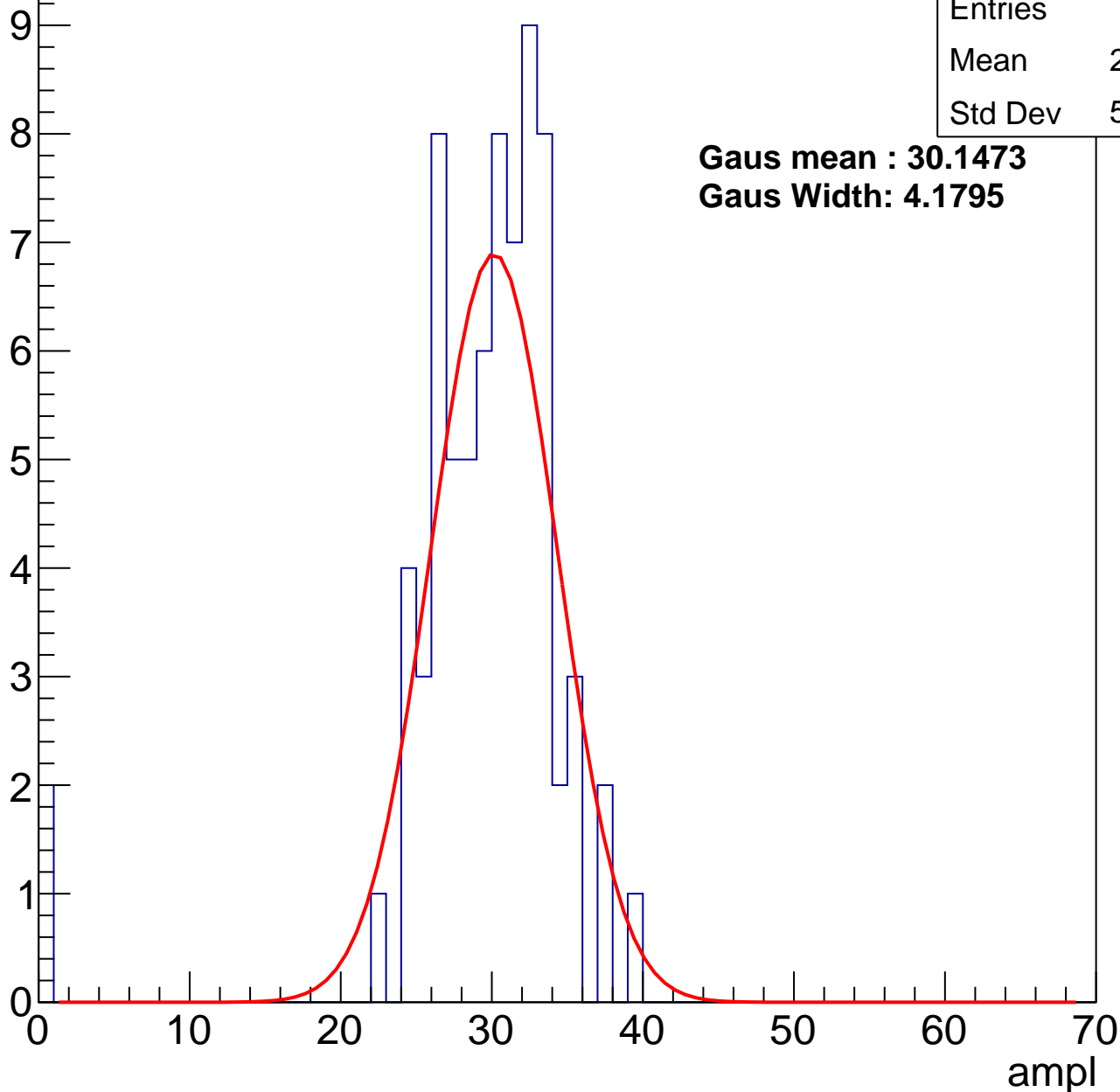
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	74
Mean	28.99
Std Dev	5.935

**Gaus mean : 30.1473**

**Gaus Width: 4.1795**



# B1L101S, U22-ch82, adc1

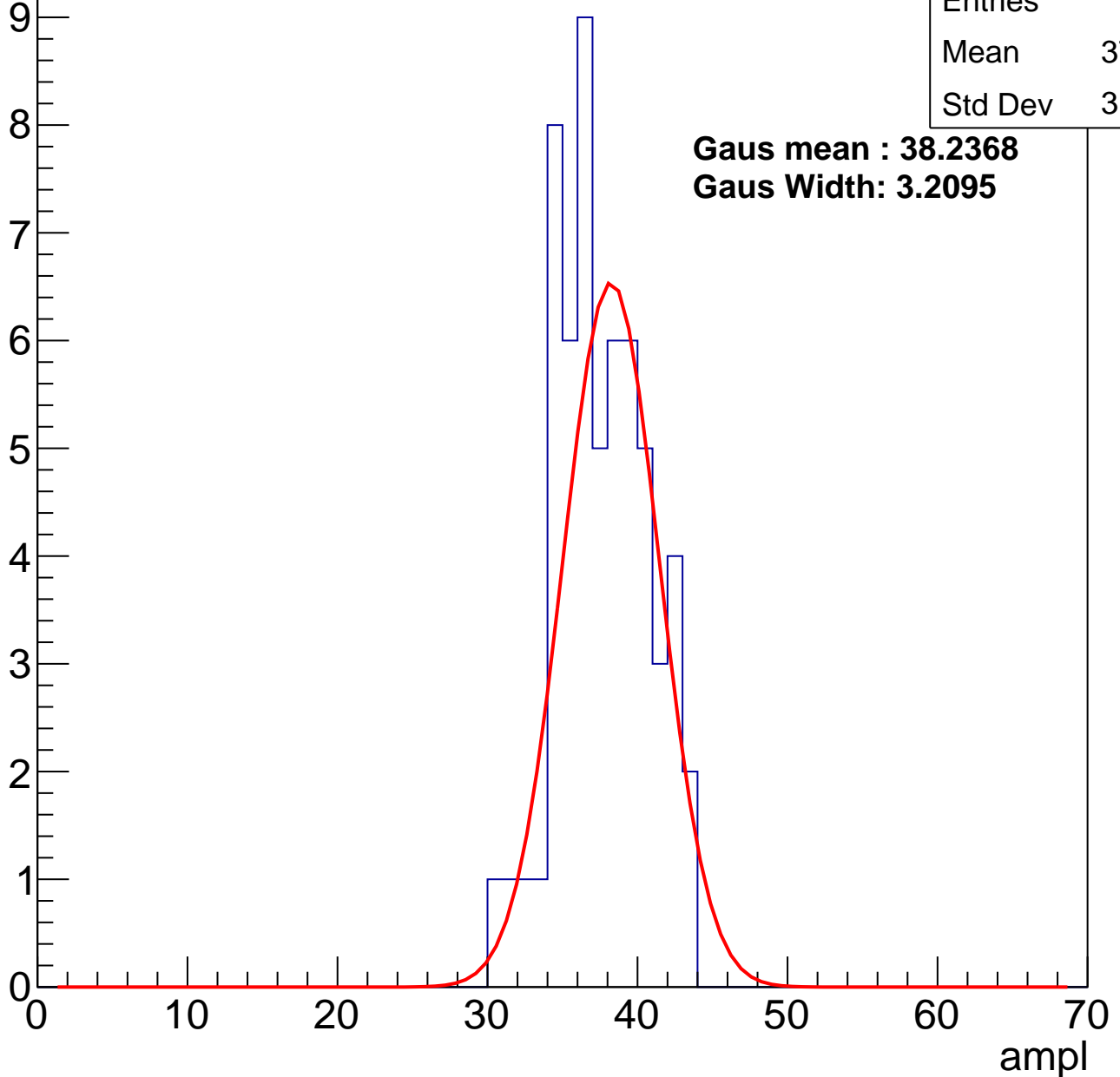
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	58
Mean	37.17
Std Dev	3.007

**Gaus mean : 38.2368**

**Gaus Width: 3.2095**



# B1L101S, U22-ch82, adc2

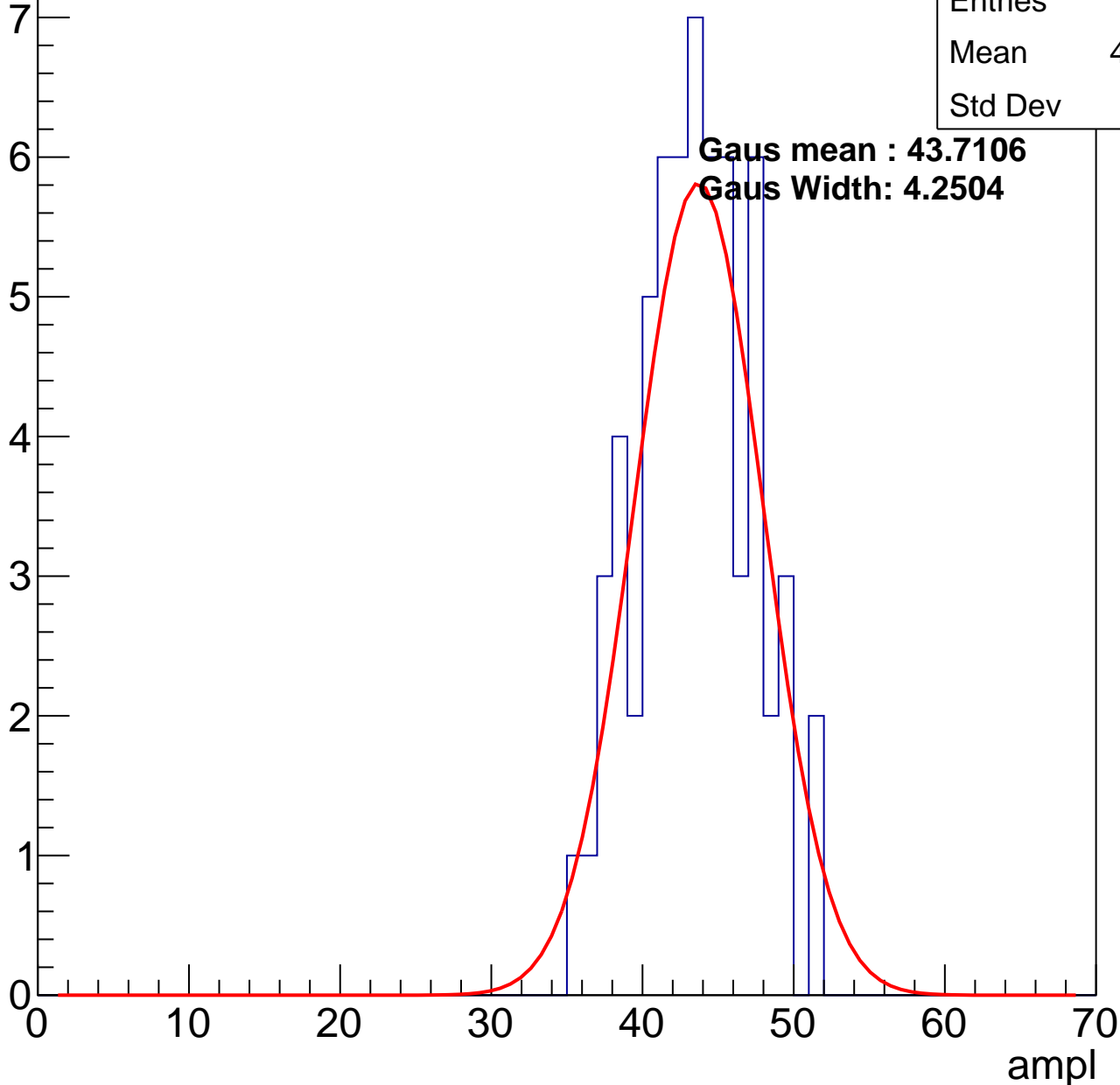
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	43.02
Std Dev	3.71

**Gaus mean : 43.7106**

**Gaus Width: 4.2504**

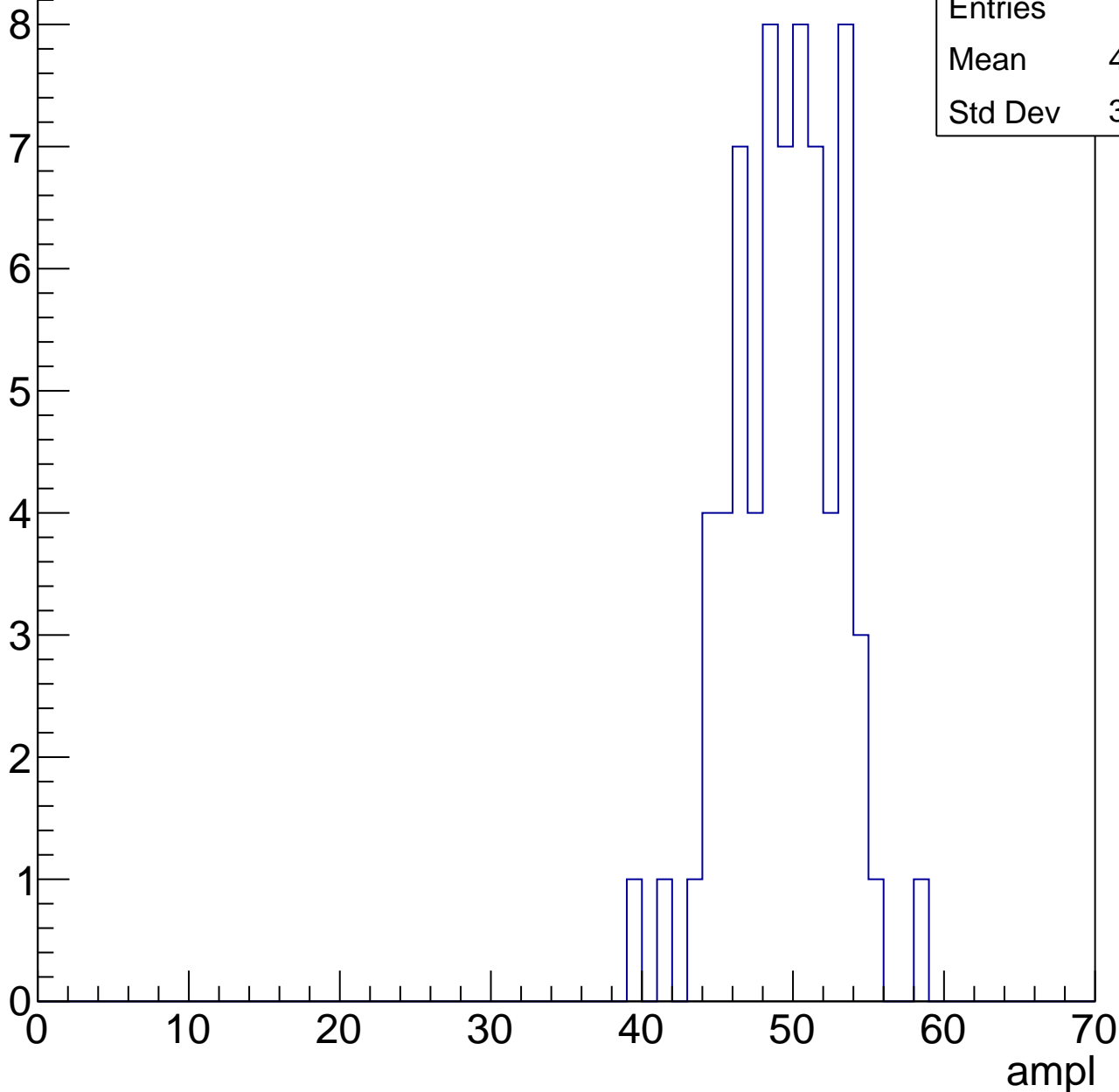


# B1L101S, U22-ch82, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	48.99
Std Dev	3.495



# B1L101S, U22-ch82, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

10

8

6

4

2

0

0

10

20

30

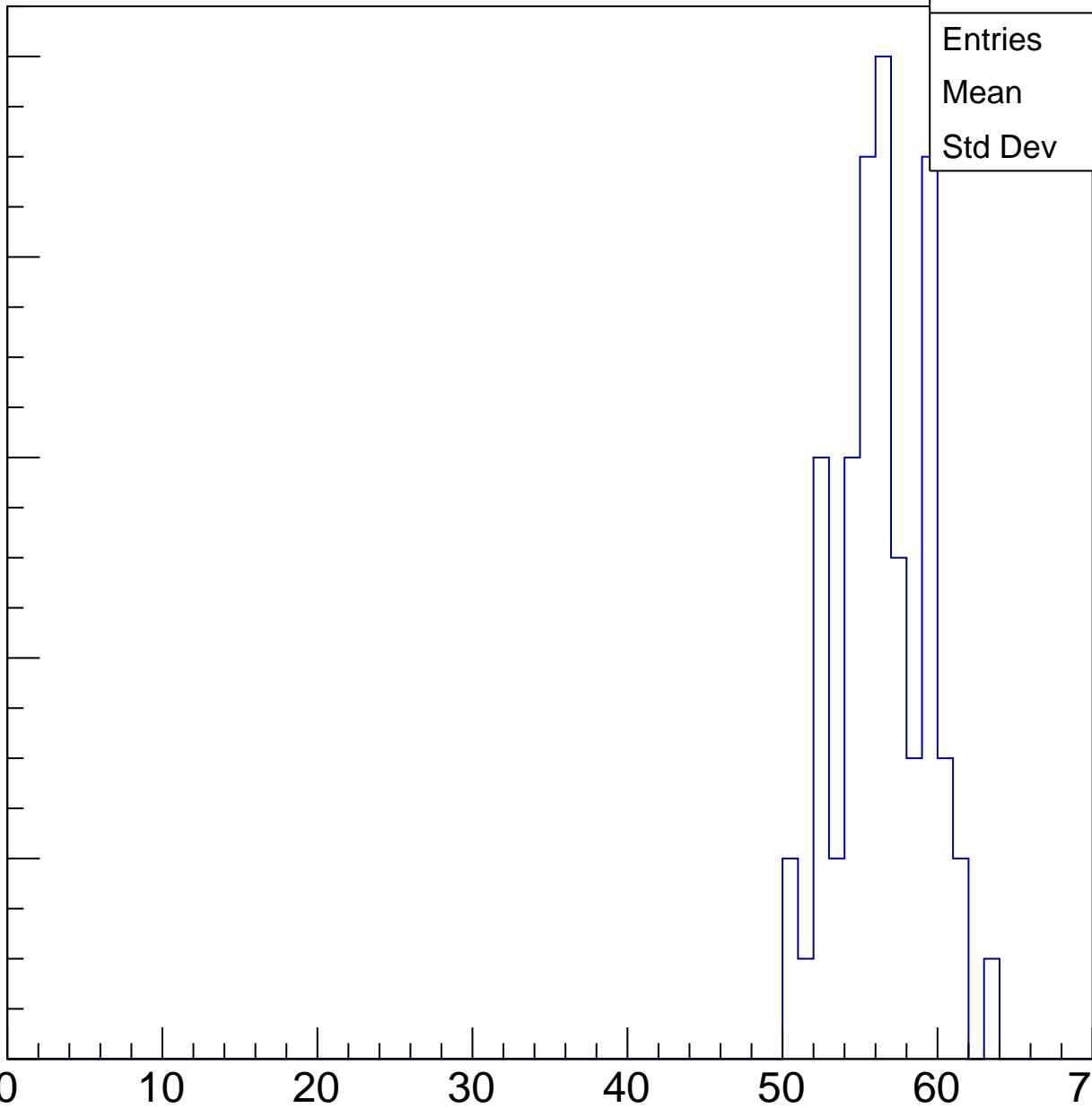
40

50

60

ampl

Entries	59
Mean	55.98
Std Dev	2.879



# B1L101S, U22-ch82, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

10

8

6

4

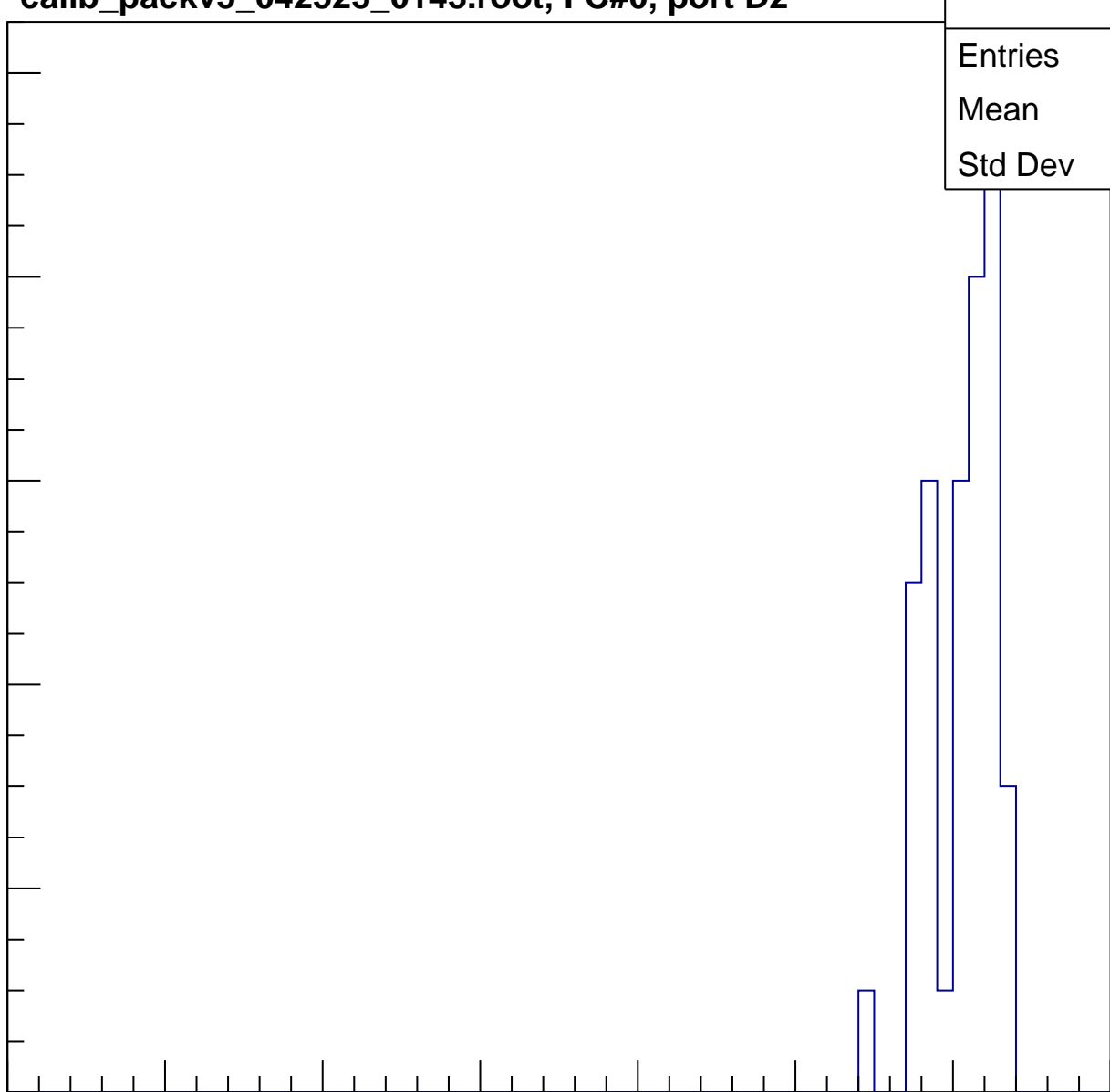
2

0

Entries	40
Mean	60.08
Std Dev	2.126

ampl

0 10 20 30 40 50 60 70

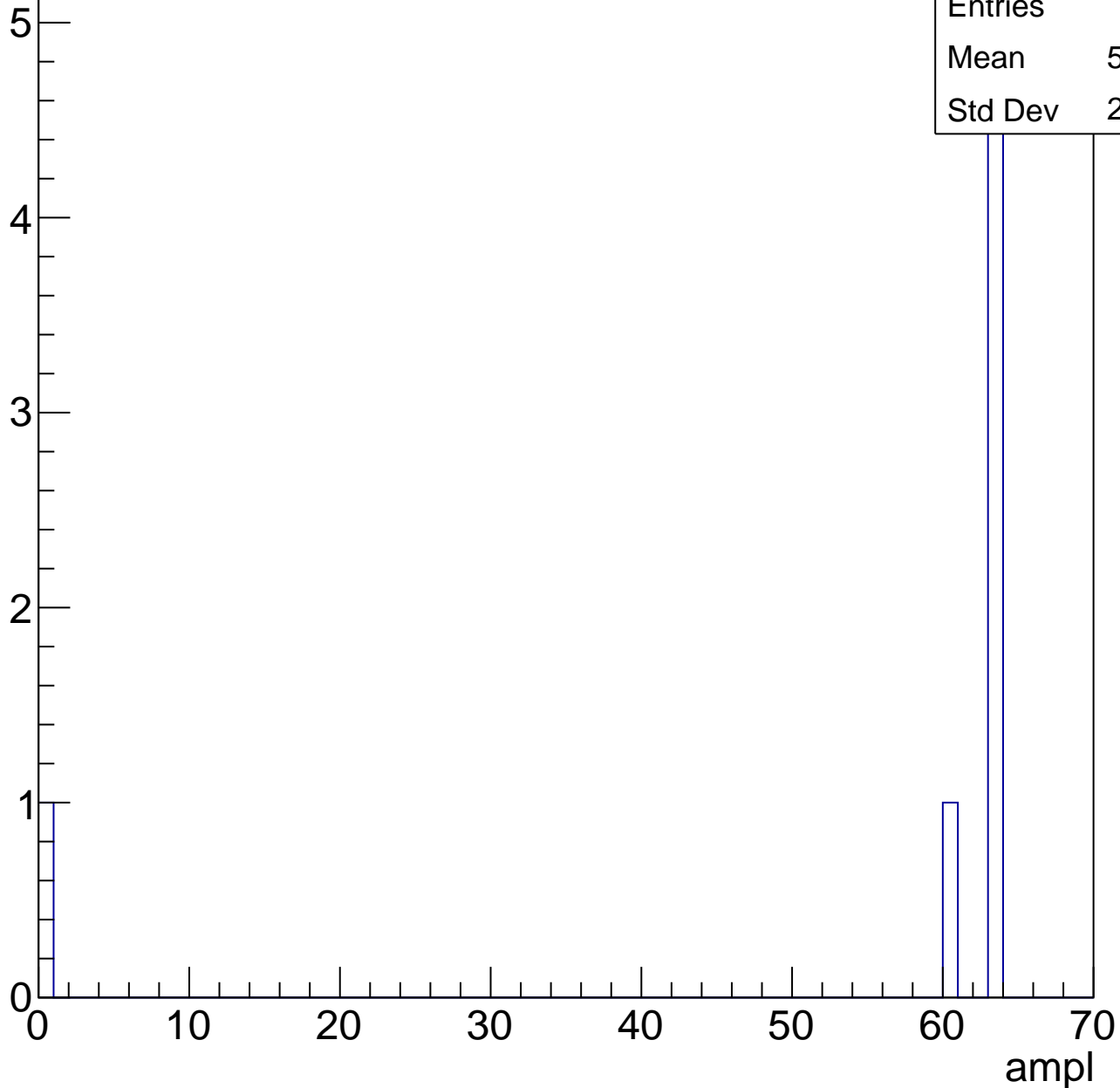


# B1L101S, U22-ch82, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	7
Mean	53.57
Std Dev	21.89

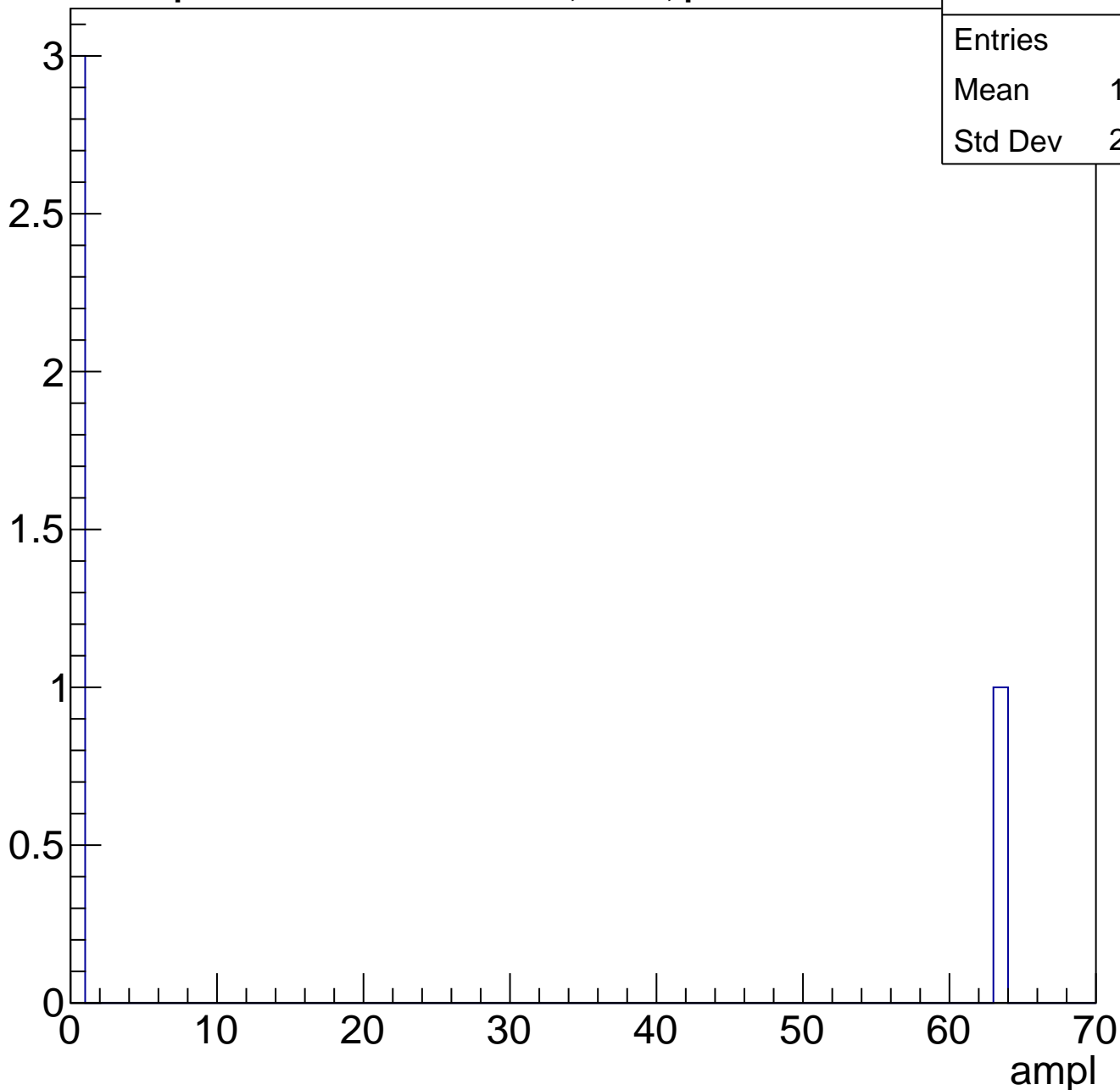




# B1L101S, U22-ch82, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	4
Mean	15.75
Std Dev	27.28

# B1L101S, U22-ch83, adc0

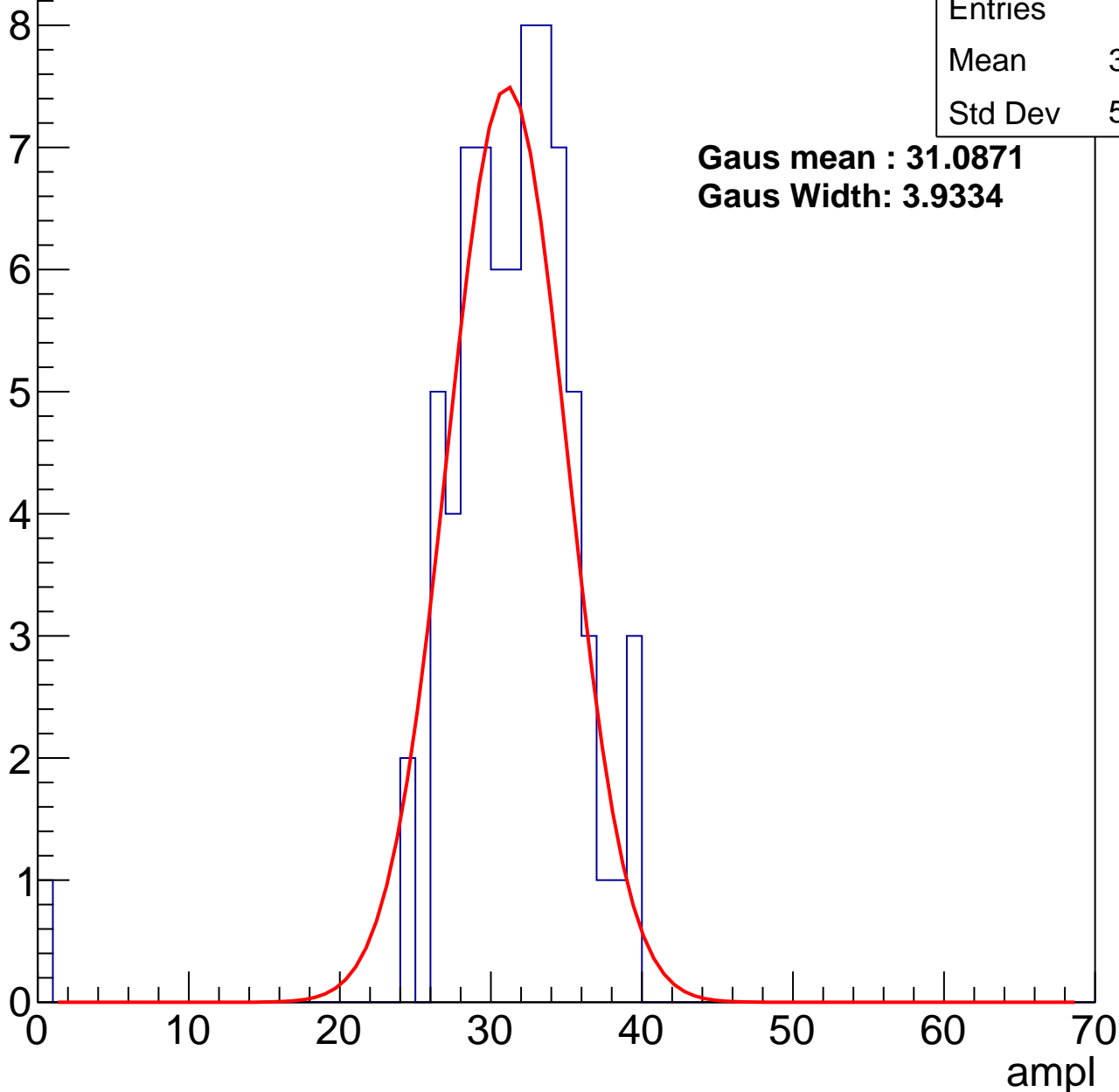
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	74
Mean	30.86
Std Dev	5.039

**Gaus mean : 31.0871**

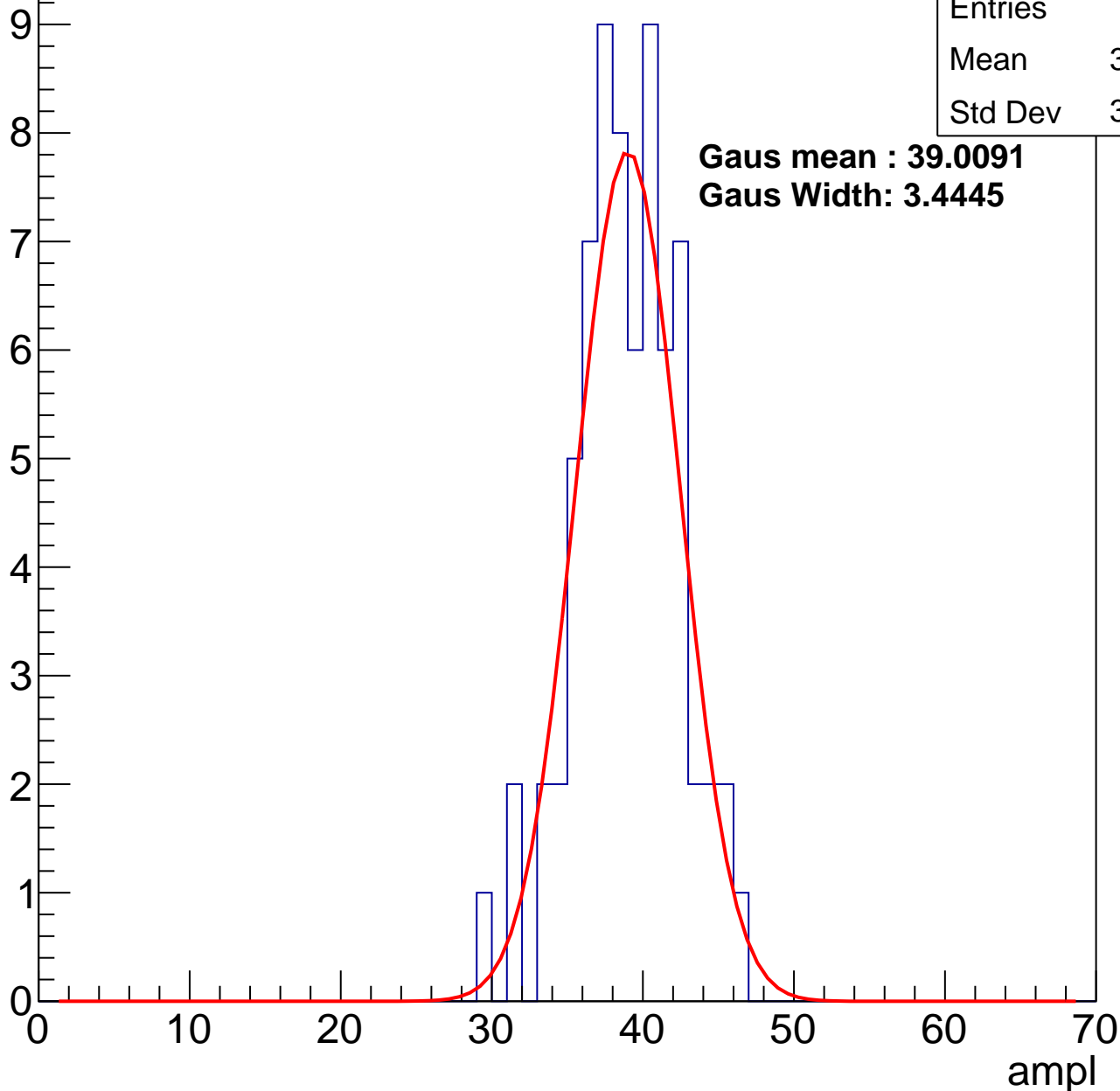
**Gaus Width: 3.9334**



# B1L101S, U22-ch83, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U22-ch83, adc2

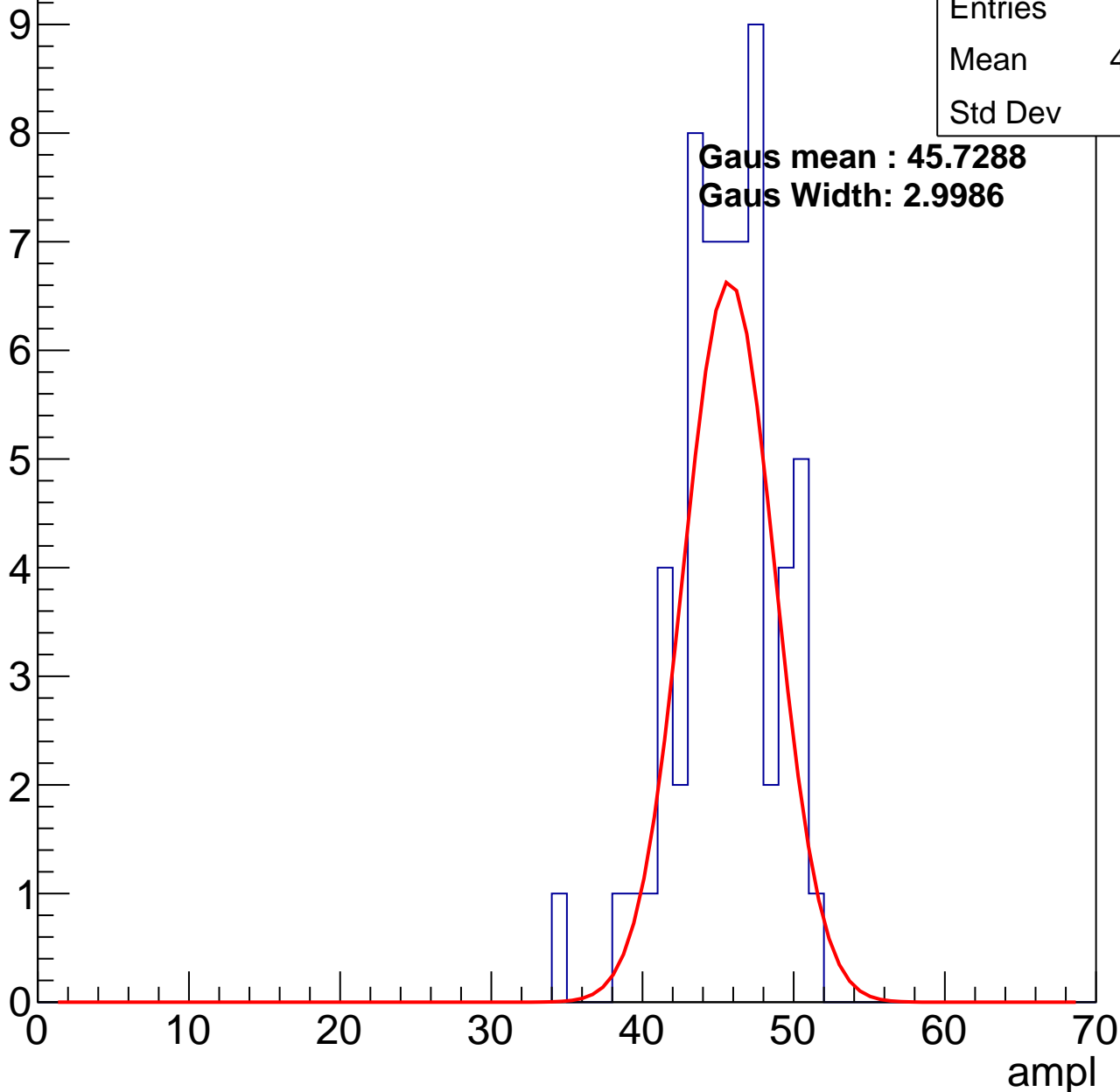
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	60
Mean	45.07
Std Dev	3.26

**Gaus mean : 45.7288**

**Gaus Width: 2.9986**

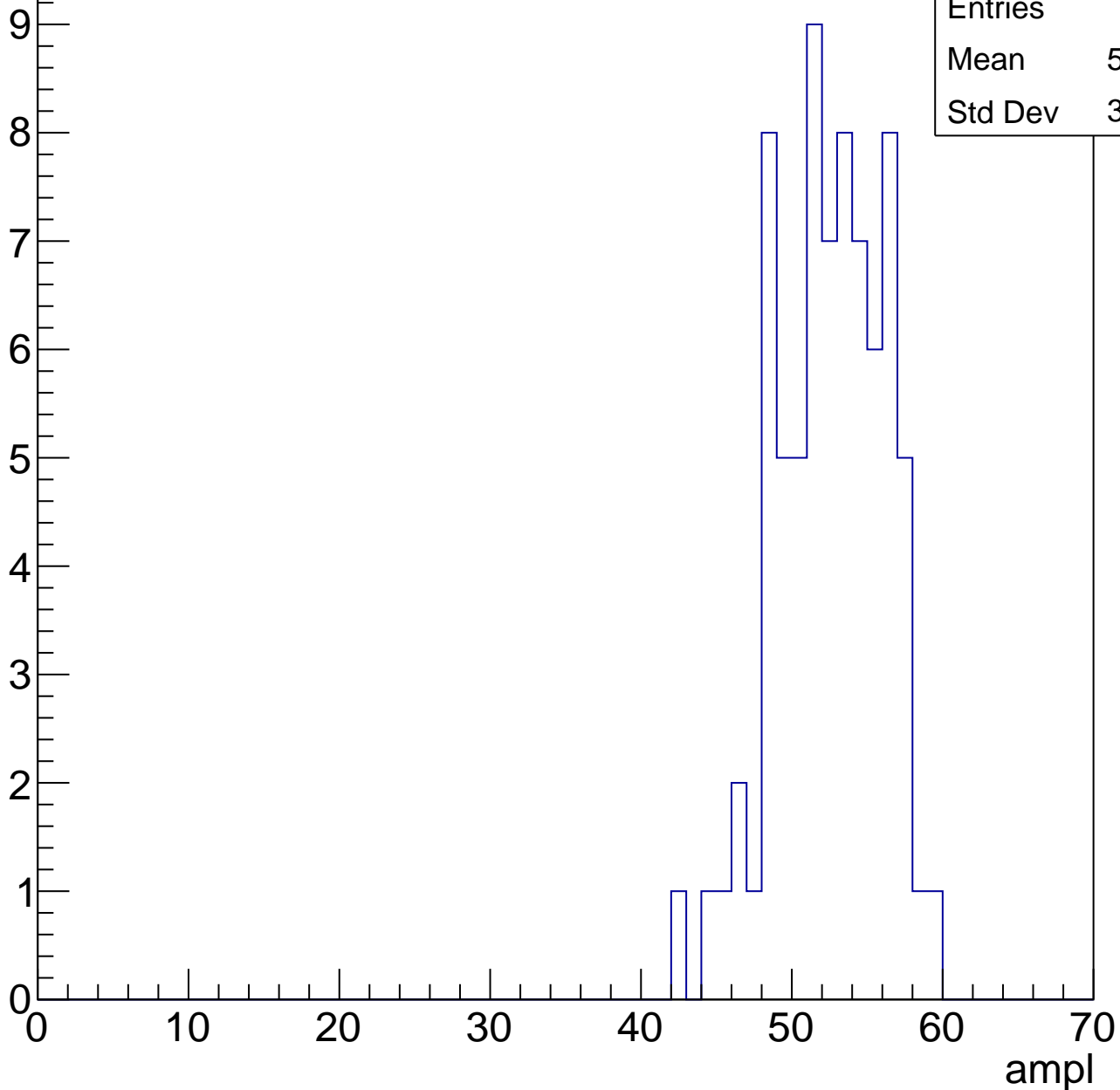


# B1L101S, U22-ch83, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	76
Mean	52.03
Std Dev	3.517

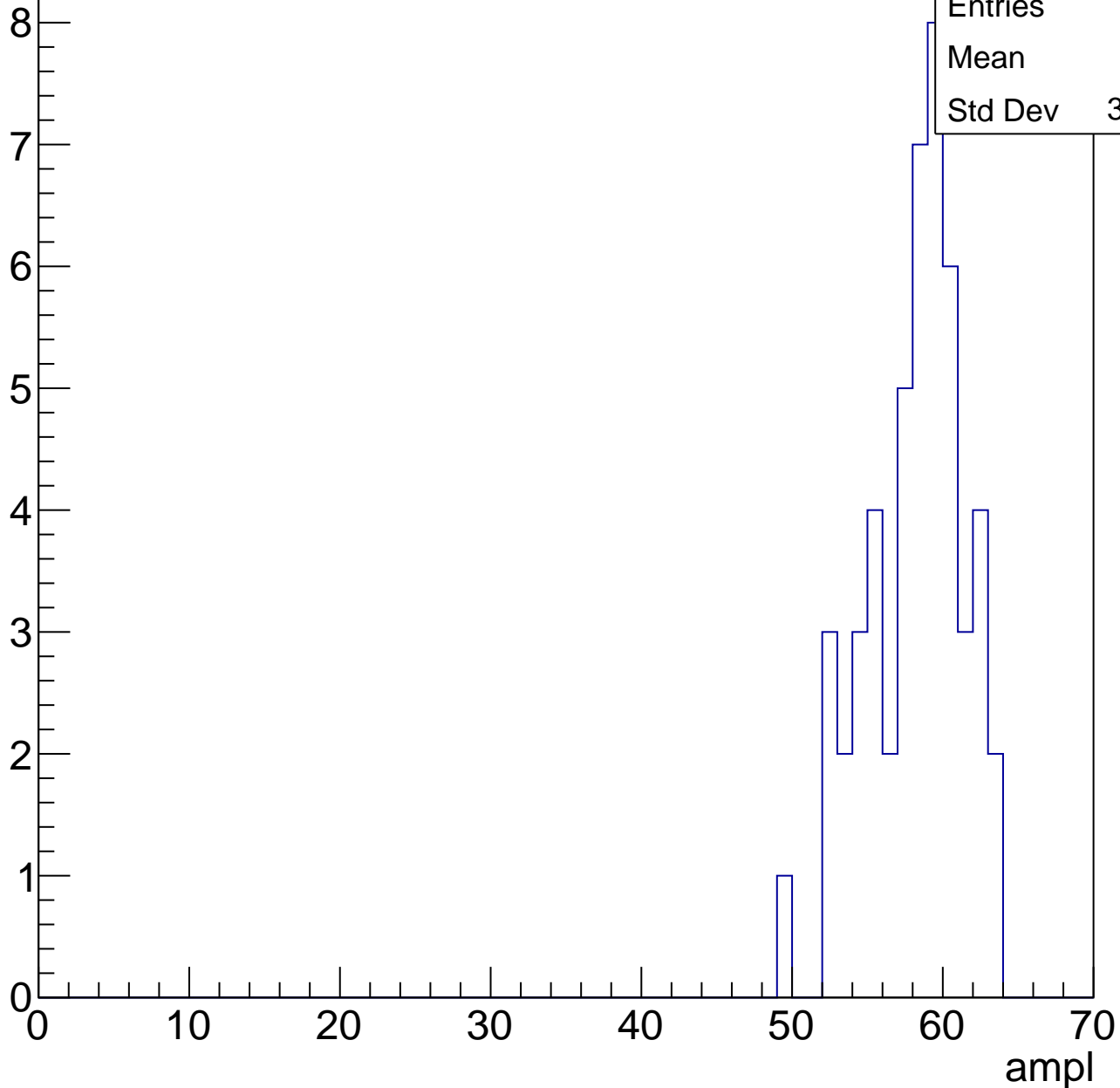


# B1L101S, U22-ch83, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	50
Mean	57.7
Std Dev	3.176

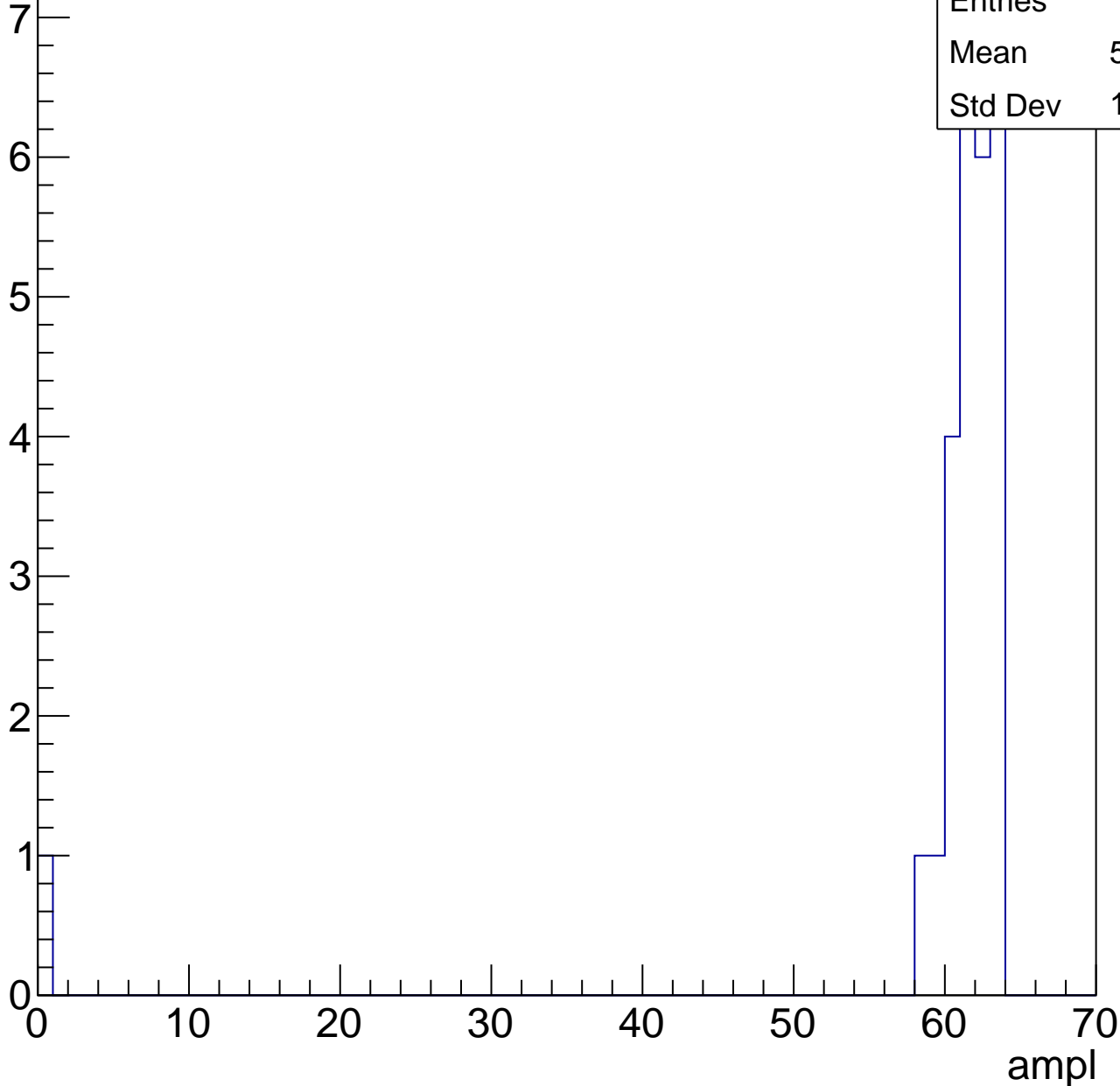


# B1L101S, U22-ch83, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

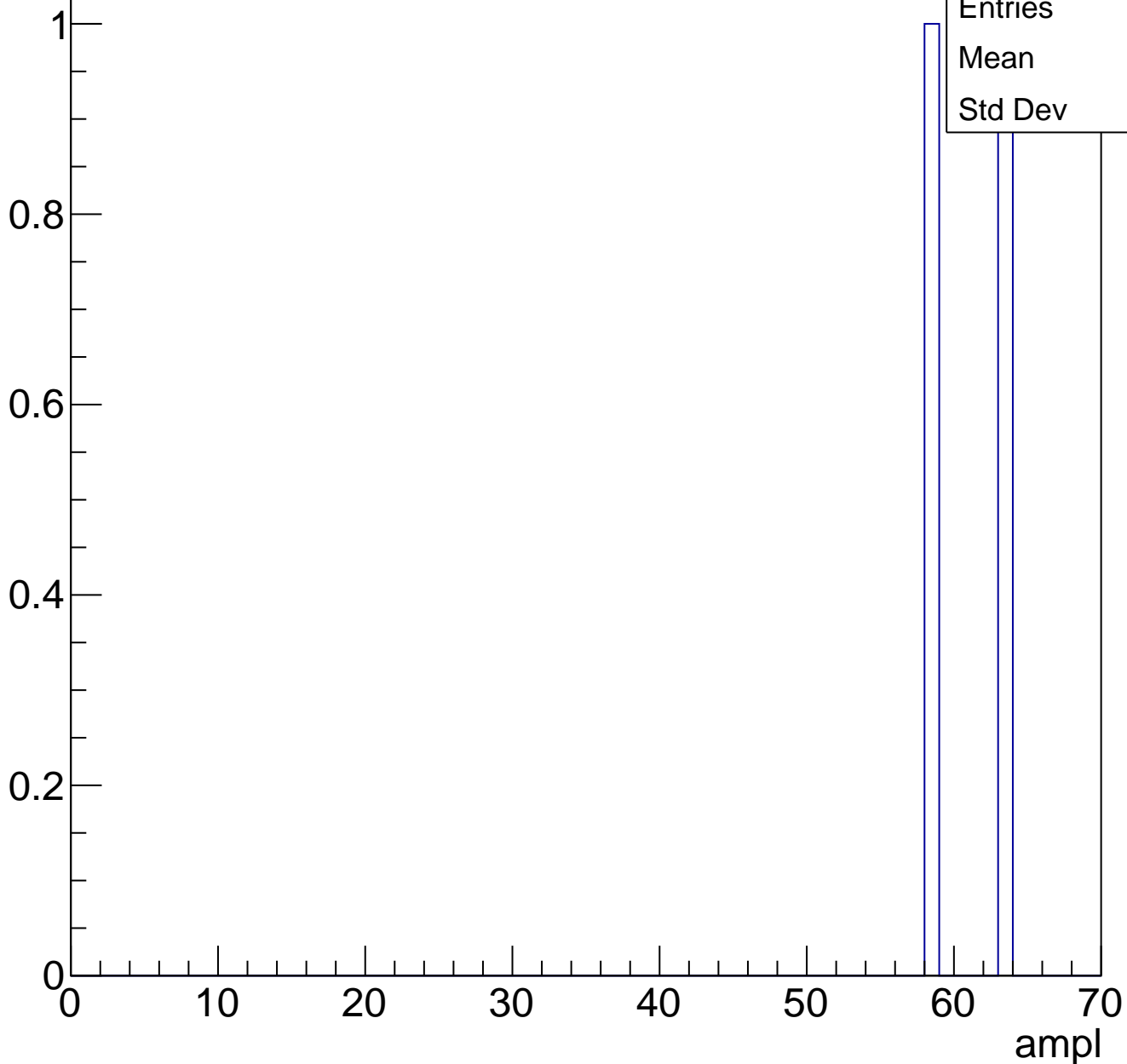
Entries	27
Mean	59.15
Std Dev	11.67



# B1L101S, U22-ch83, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U22-ch83, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

1  
0.8  
0.6  
0.4  
0.2  
0

Entries	1
Mean	24
Std Dev	0

ampl

# B1L101S, U22-ch84, adc0

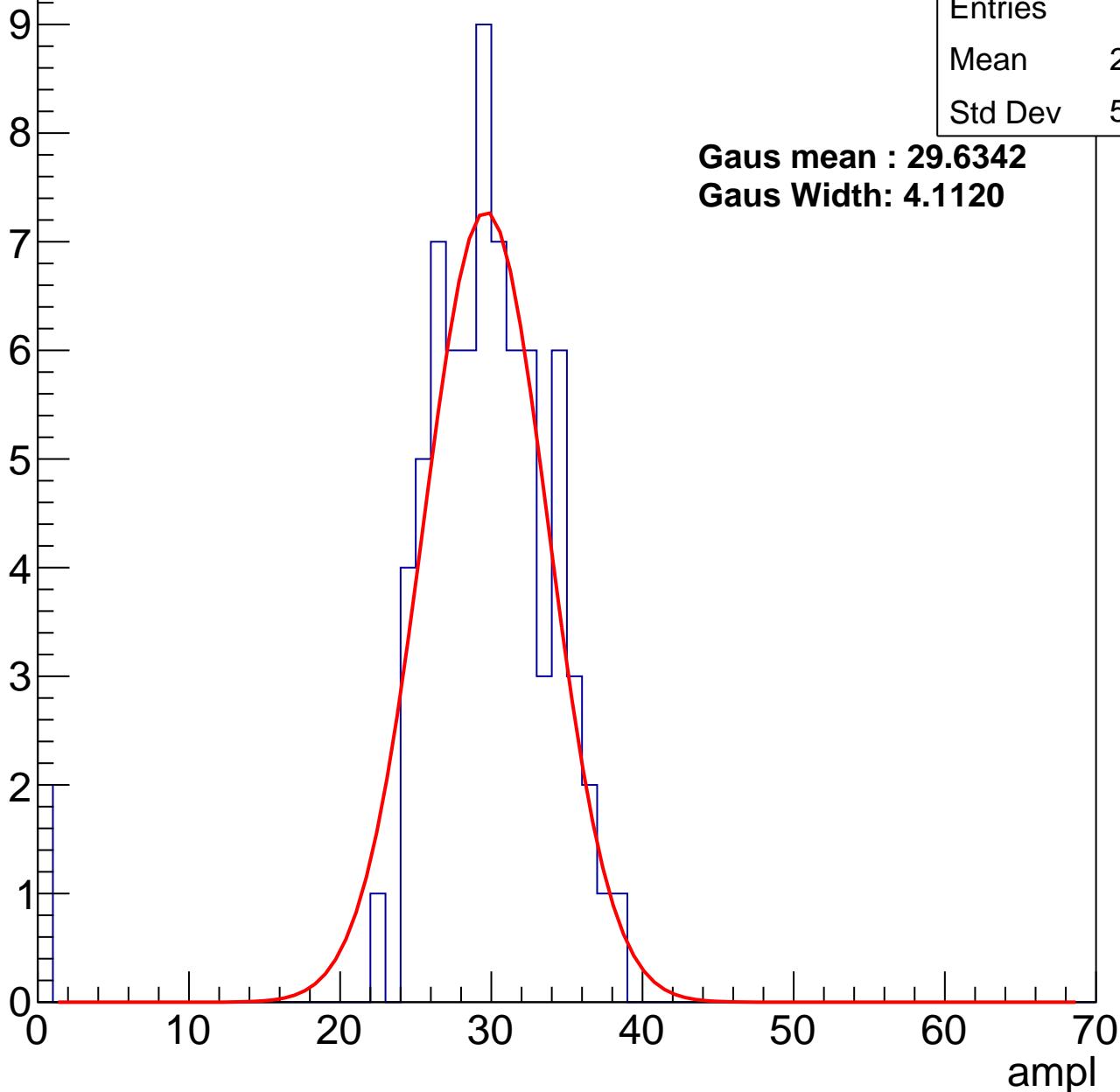
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	75
Mean	28.79
Std Dev	5.927

**Gaus mean : 29.6342**

**Gaus Width: 4.1120**



# B1L101S, U22-ch84, adc1

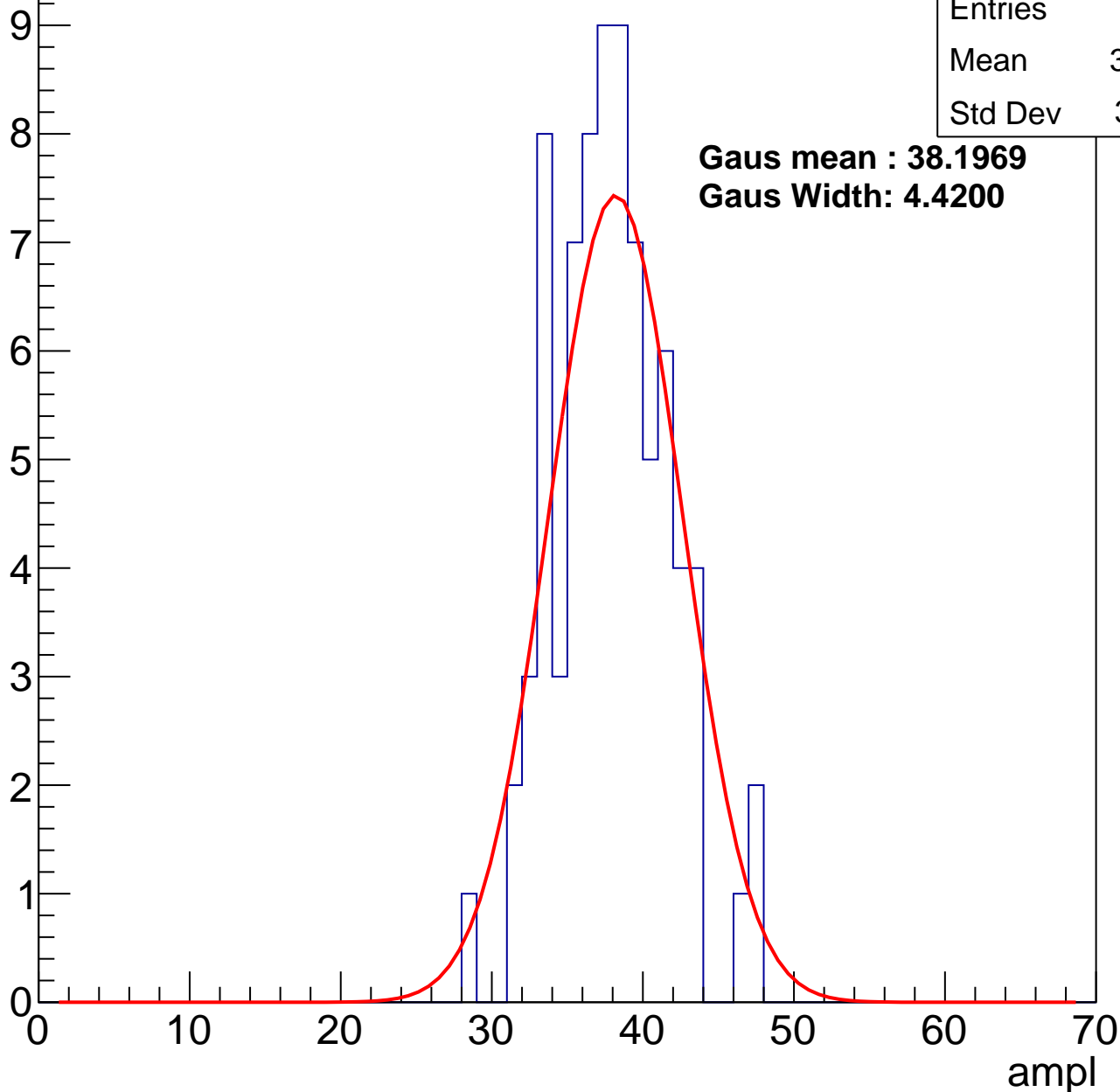
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	79
Mean	37.46
Std Dev	3.741

**Gaus mean : 38.1969**

**Gaus Width: 4.4200**



# B1L101S, U22-ch84, adc2

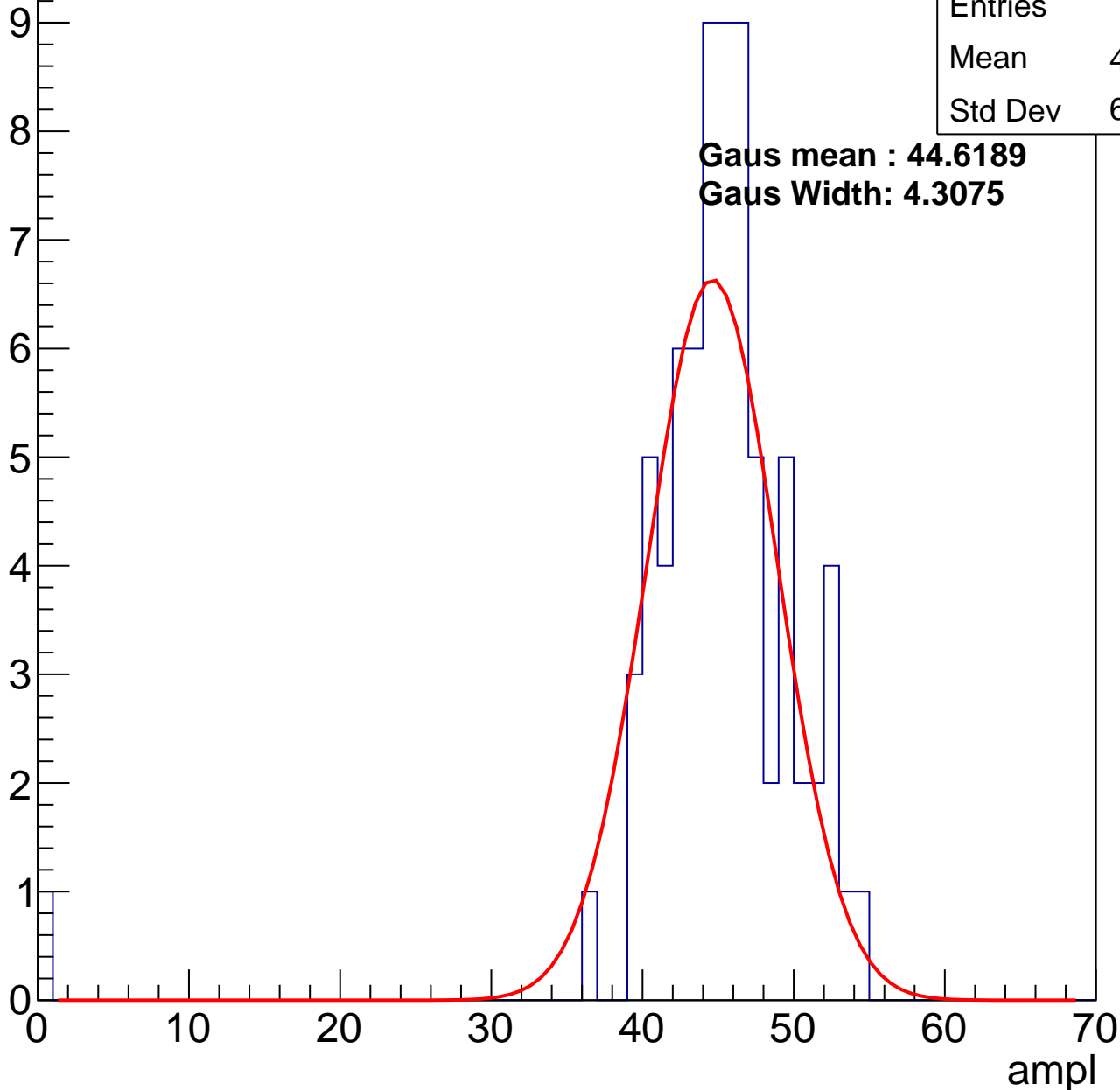
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	75
Mean	44.47
Std Dev	6.386

**Gaus mean : 44.6189**

**Gaus Width: 4.3075**

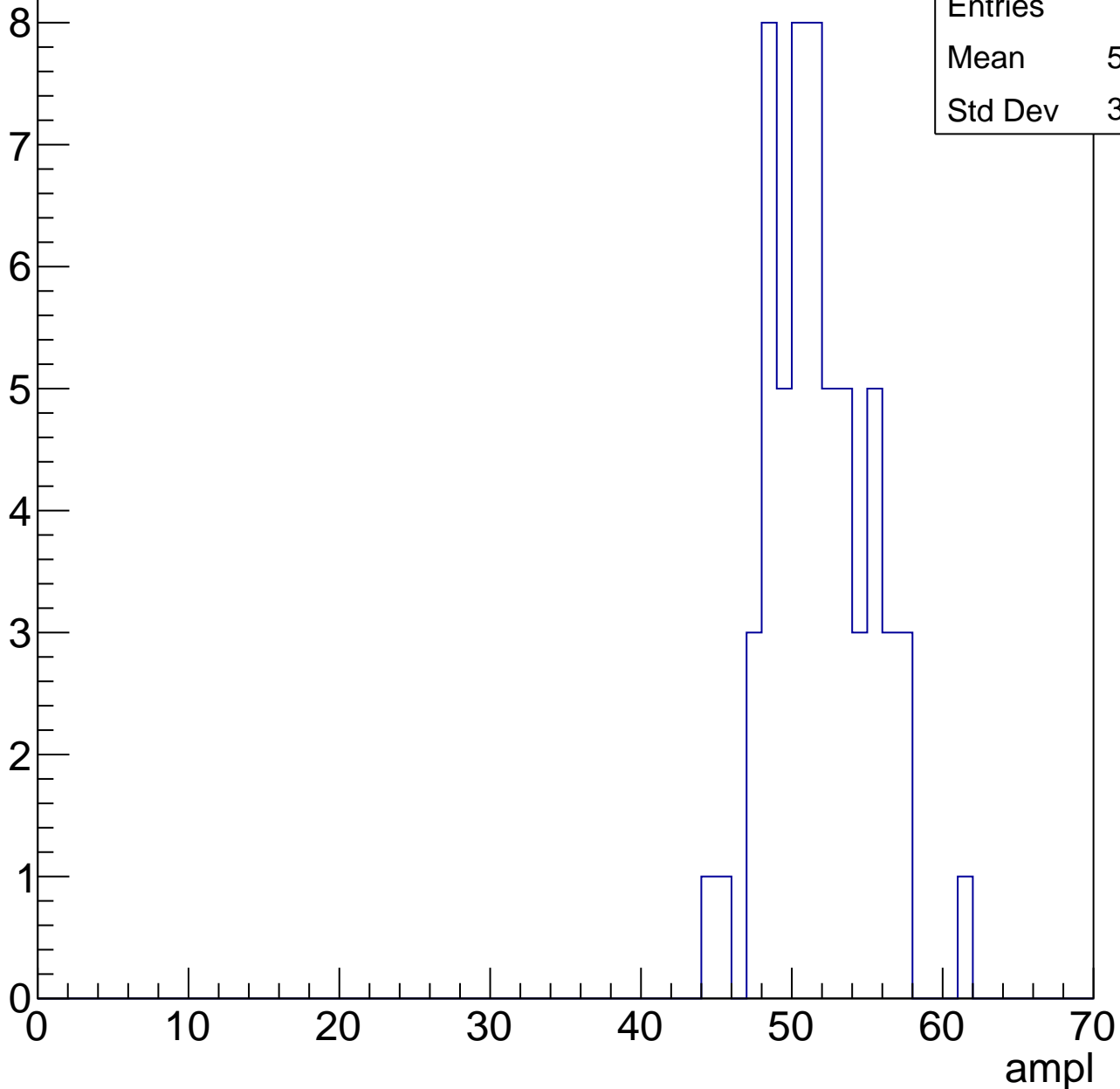


# B1L101S, U22-ch84, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	59
Mean	51.34
Std Dev	3.297

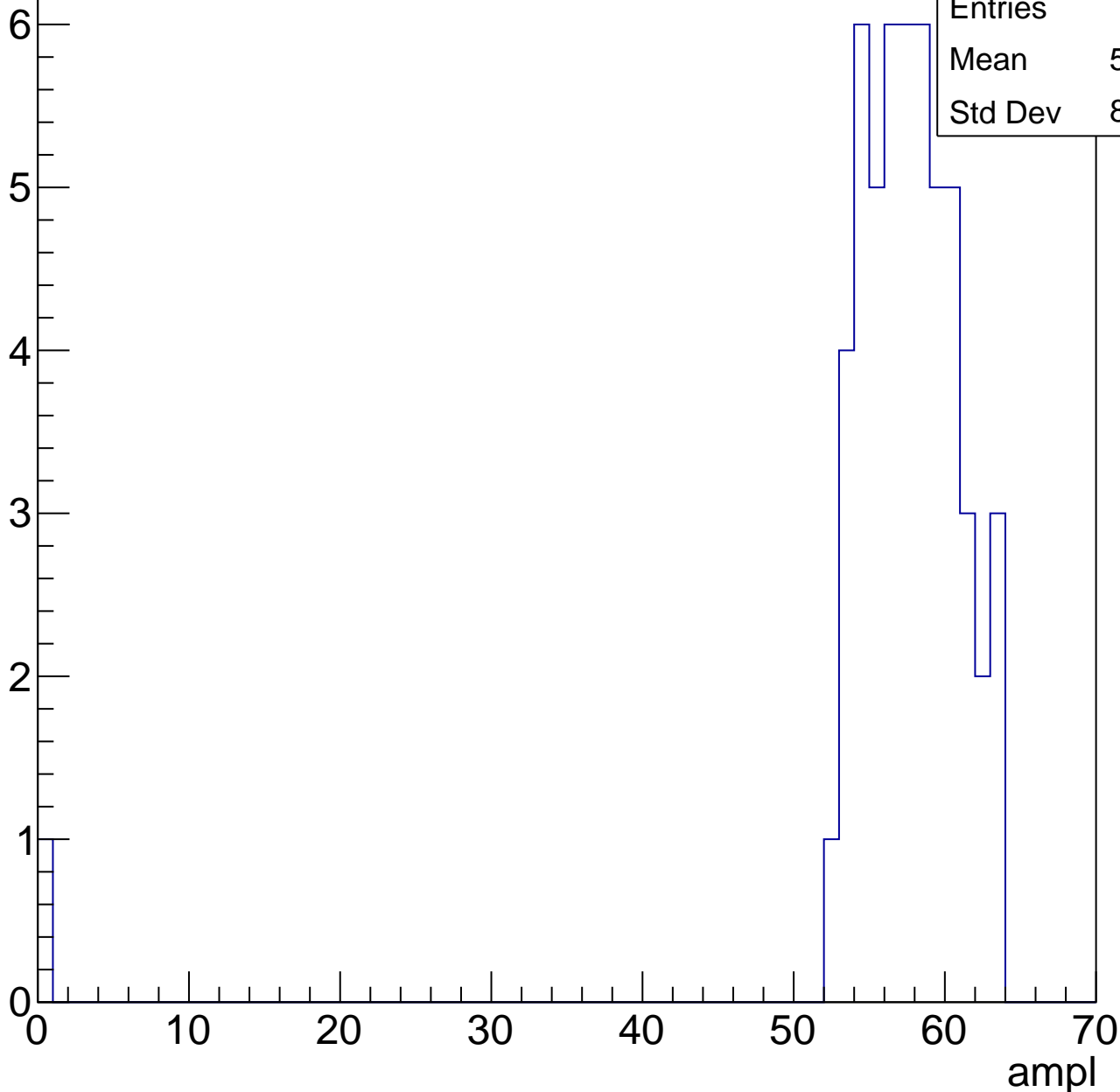


# B1L101S, U22-ch84, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	53
Mean	56.23
Std Dev	8.314



# B1L101S, U22-ch84, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

7

6

5

4

3

2

1

0

Entries

34

Mean

60.5

Std Dev

1.929

ampl

0

10

20

30

40

50

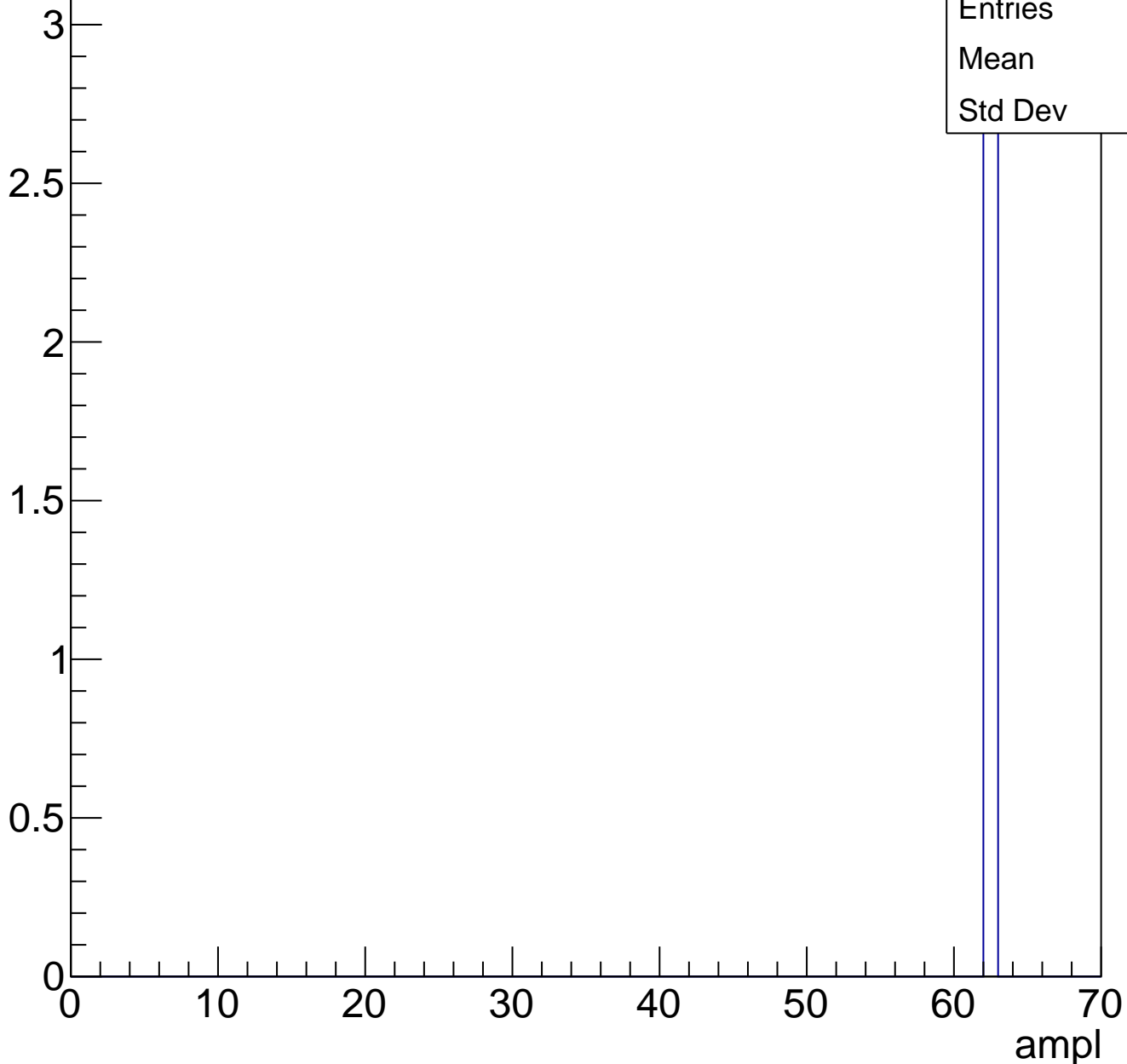
60

70

# B1L101S, U22-ch84, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U22-ch84, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U22-ch85, adc0

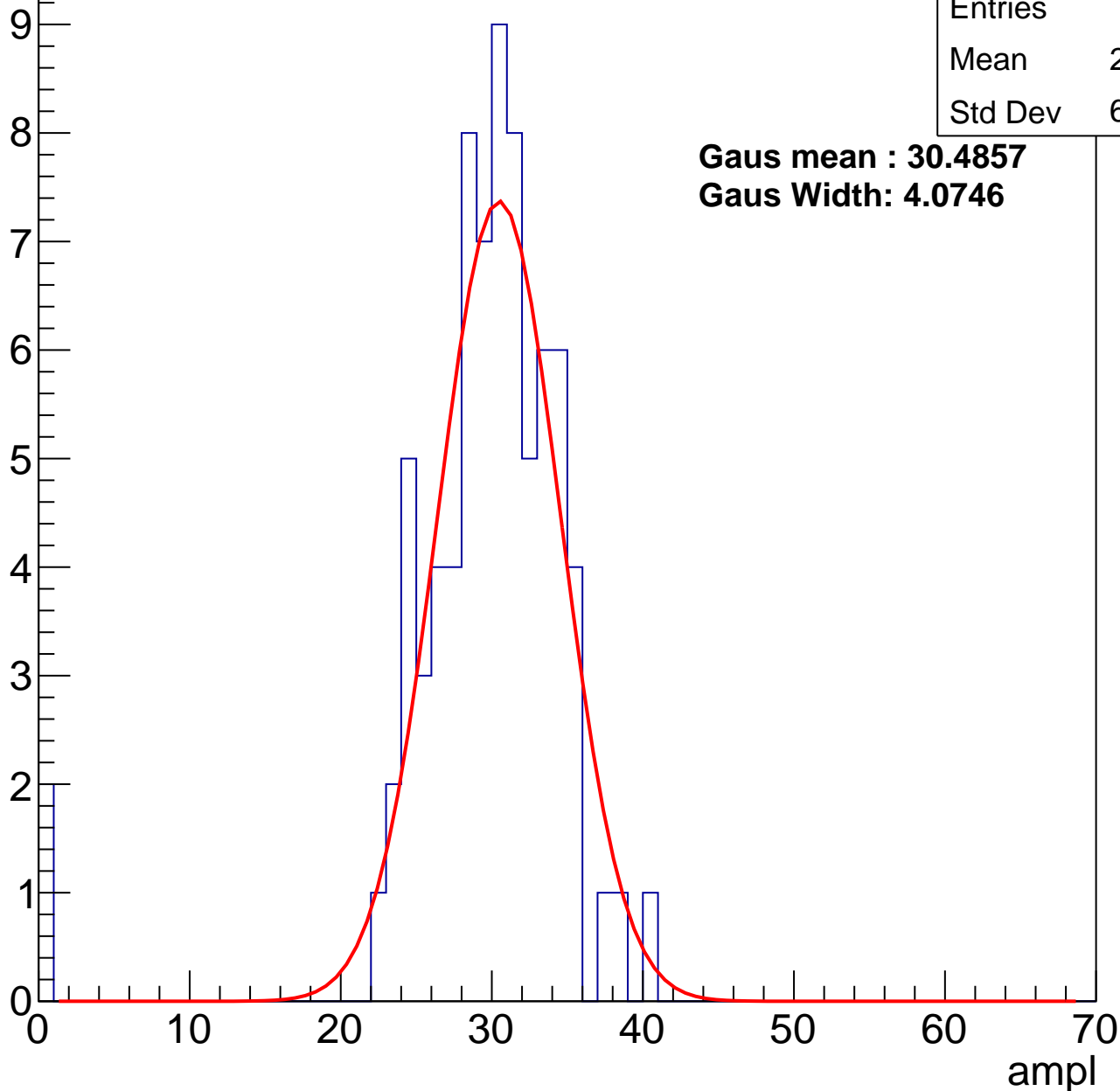
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	77
Mean	29.05
Std Dev	6.006

**Gaus mean : 30.4857**

**Gaus Width: 4.0746**



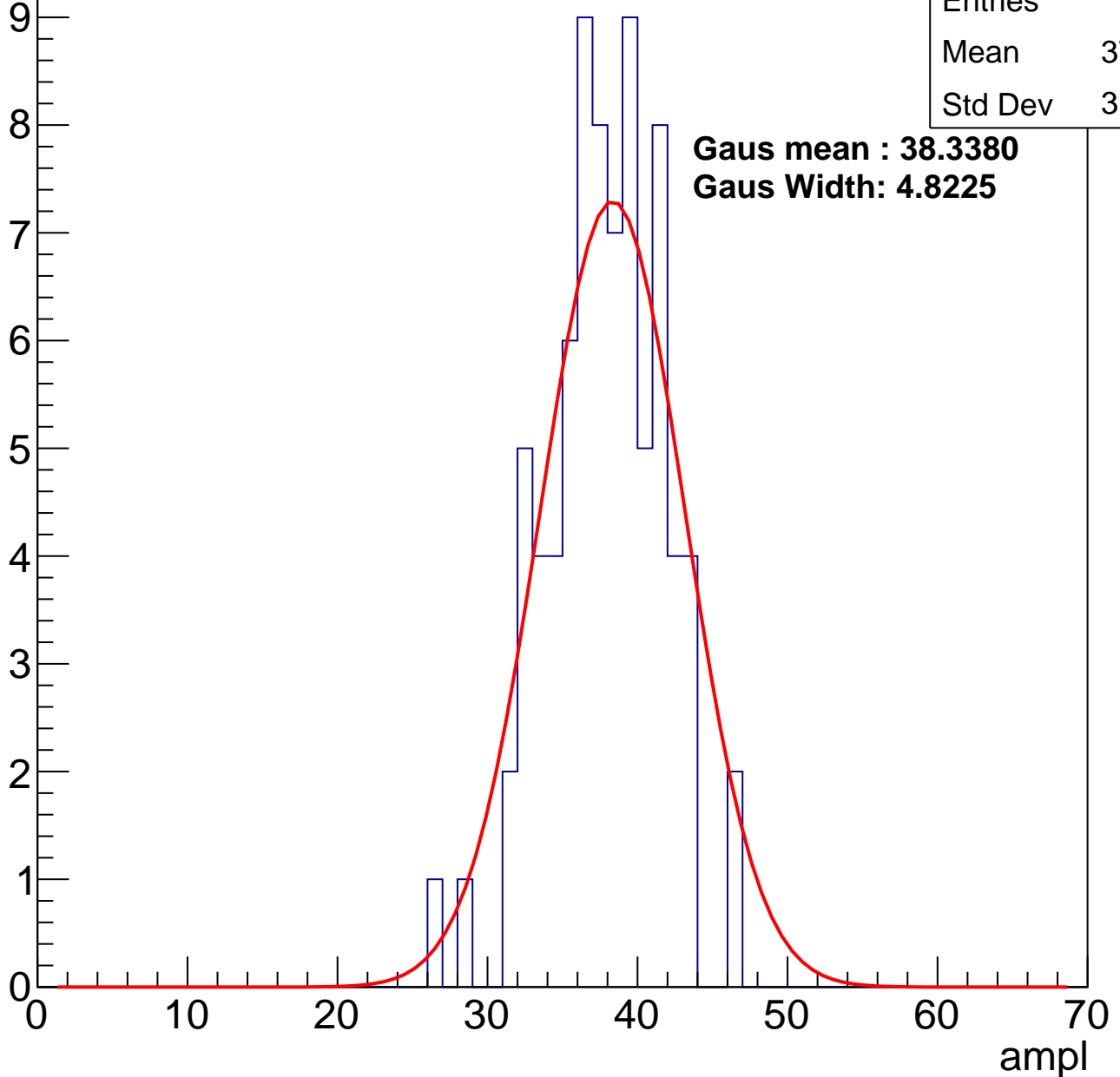
# B1L101S, U22-ch85, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	79
Mean	37.35
Std Dev	3.806

**Gaus mean : 38.3380**  
**Gaus Width: 4.8225**



# B1L101S, U22-ch85, adc2

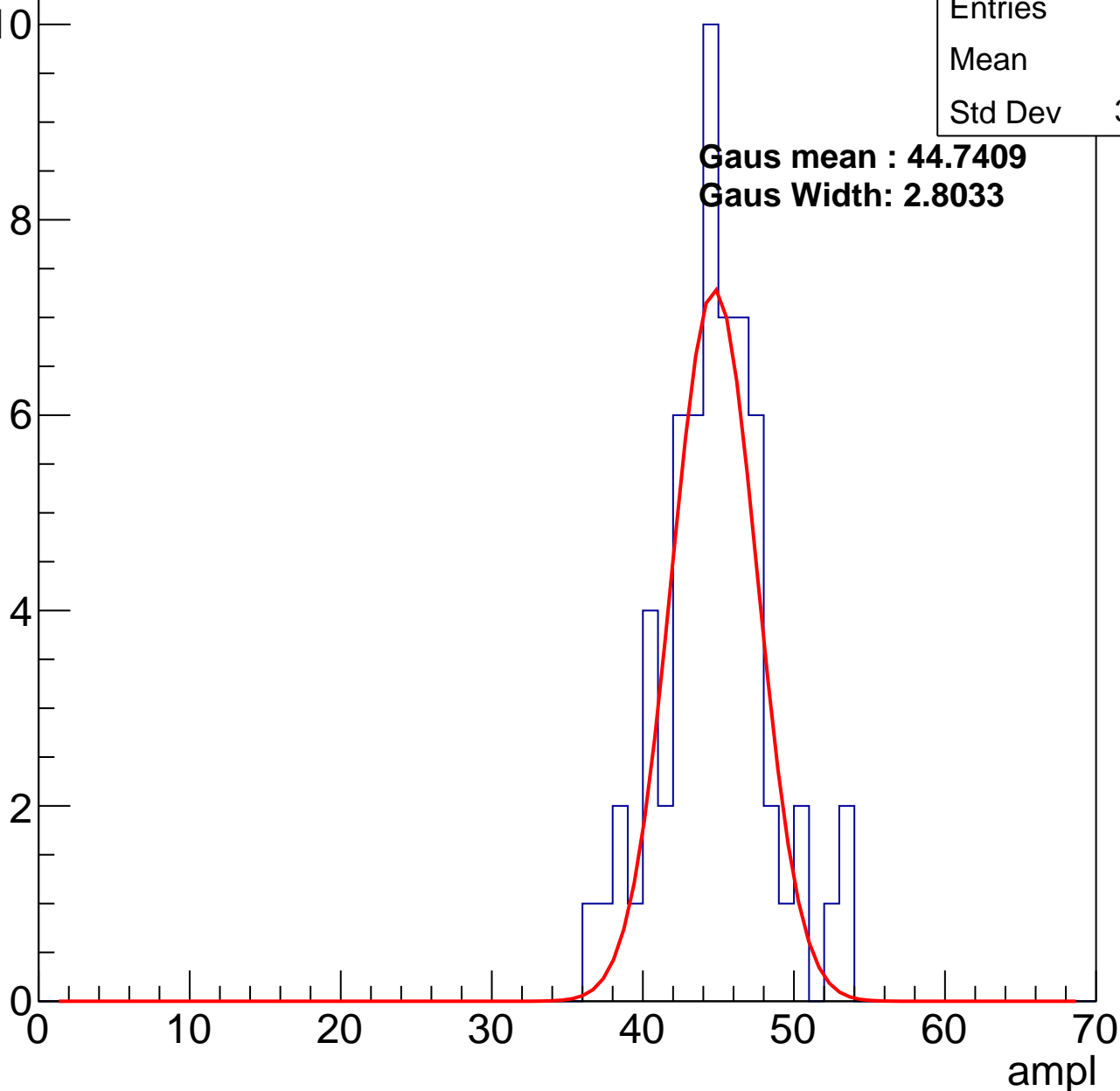
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	44.3
Std Dev	3.531

**Gaus mean : 44.7409**

**Gaus Width: 2.8033**

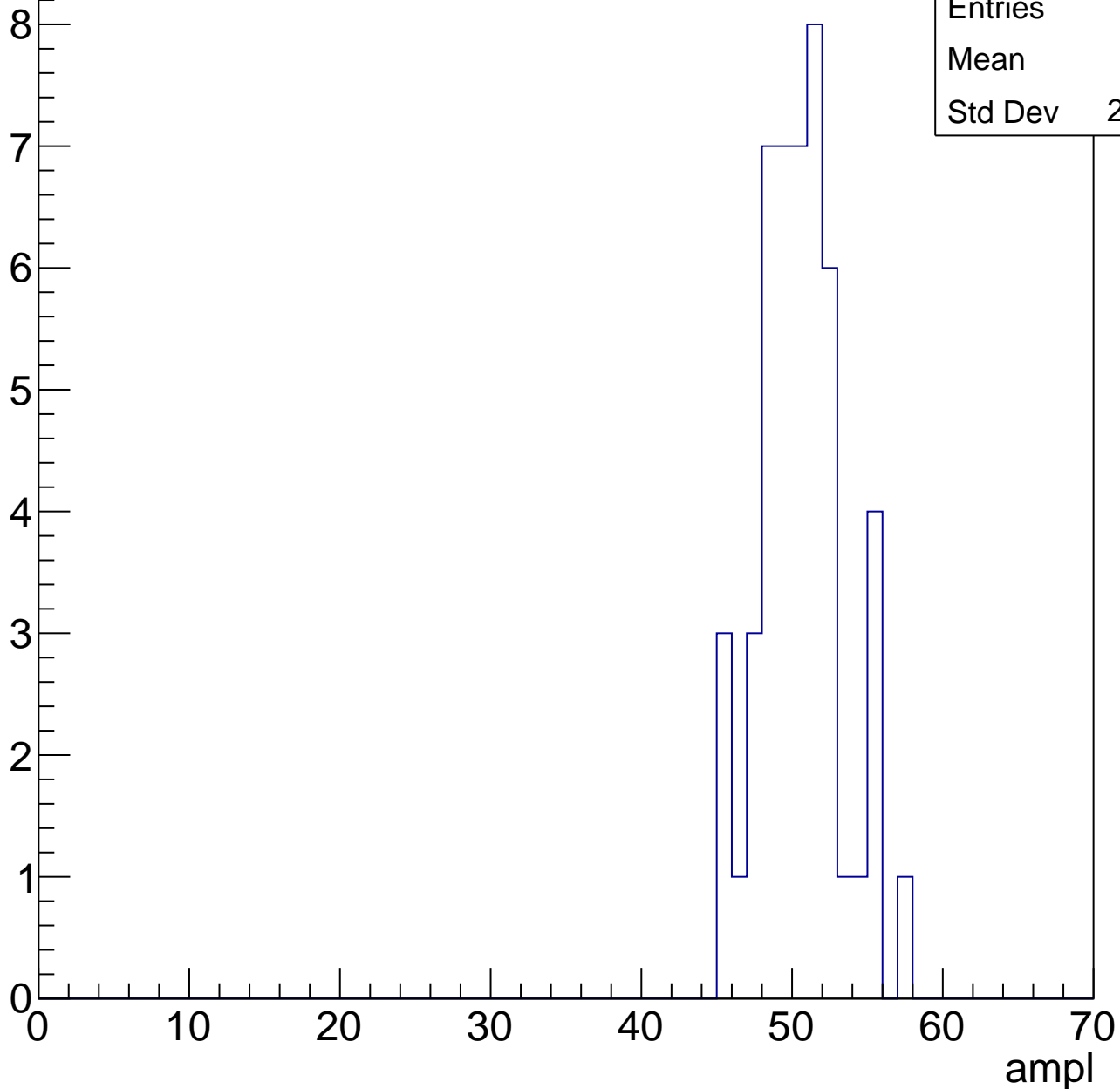


# B1L101S, U22-ch85, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

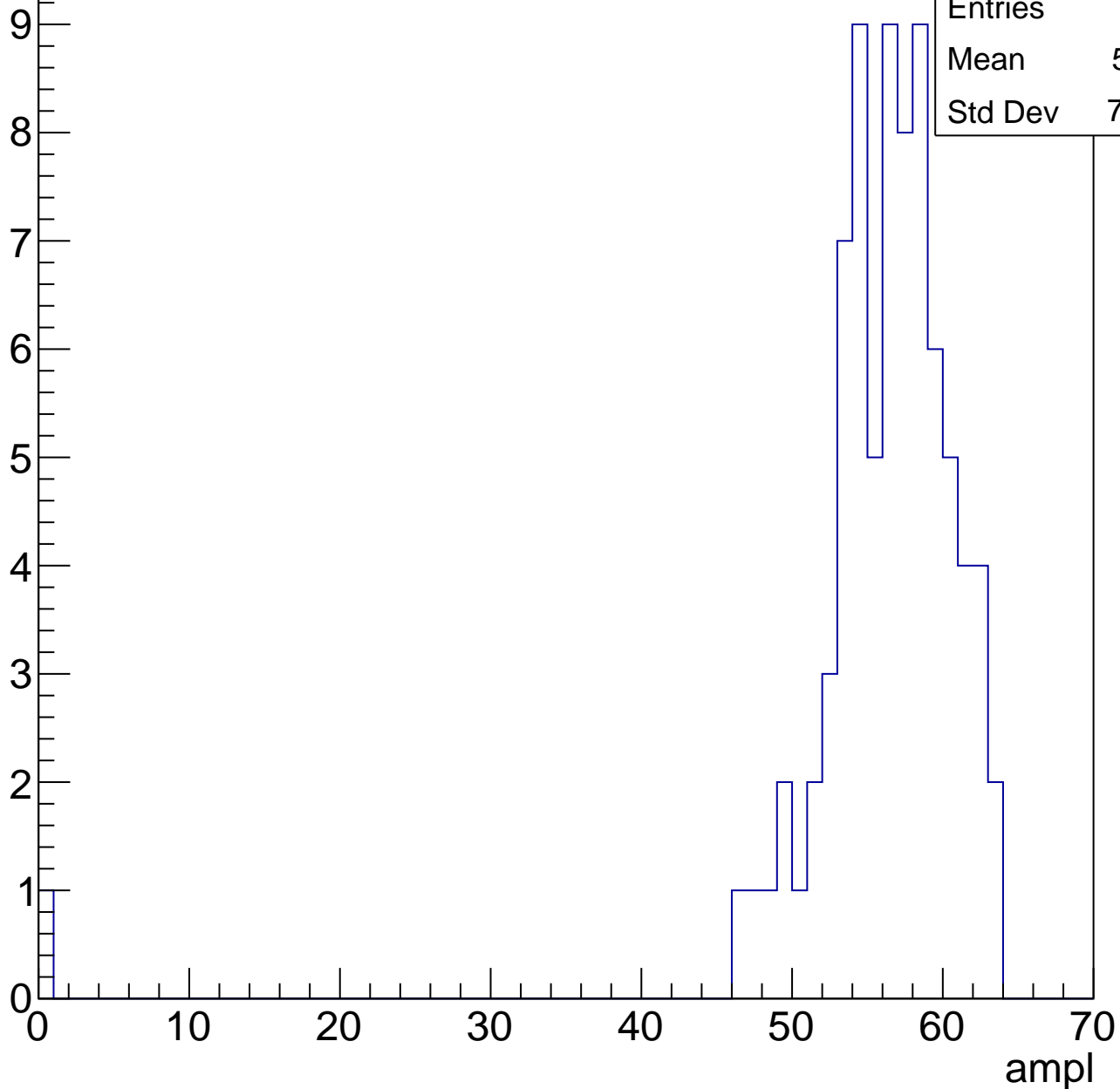
Entries	49
Mean	50.1
Std Dev	2.705



# B1L101S, U22-ch85, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

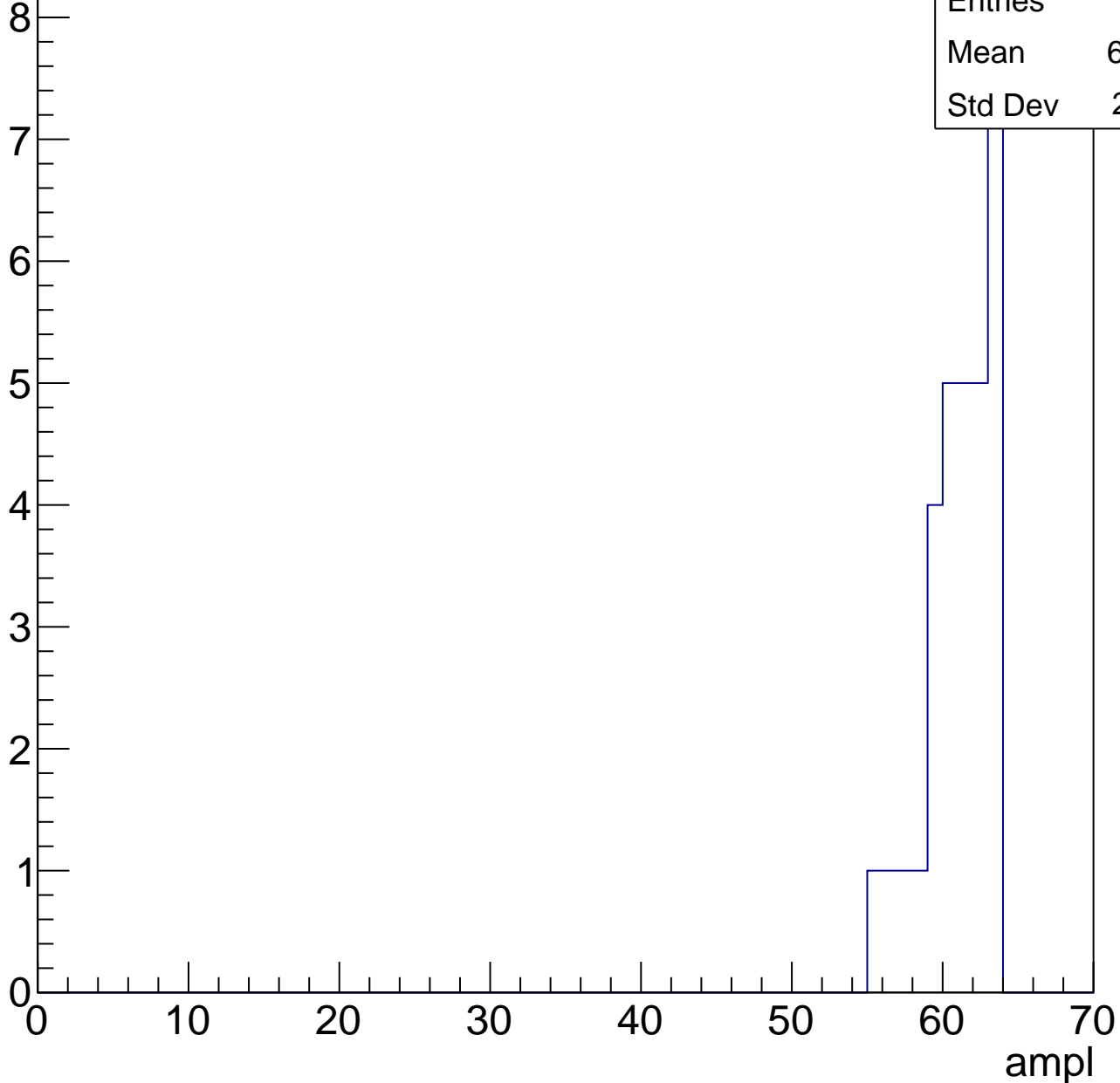


# B1L101S, U22-ch85, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	31
Mean	60.68
Std Dev	2.131



# B1L101S, U22-ch85, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U22-ch85, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U22-ch86, adc0

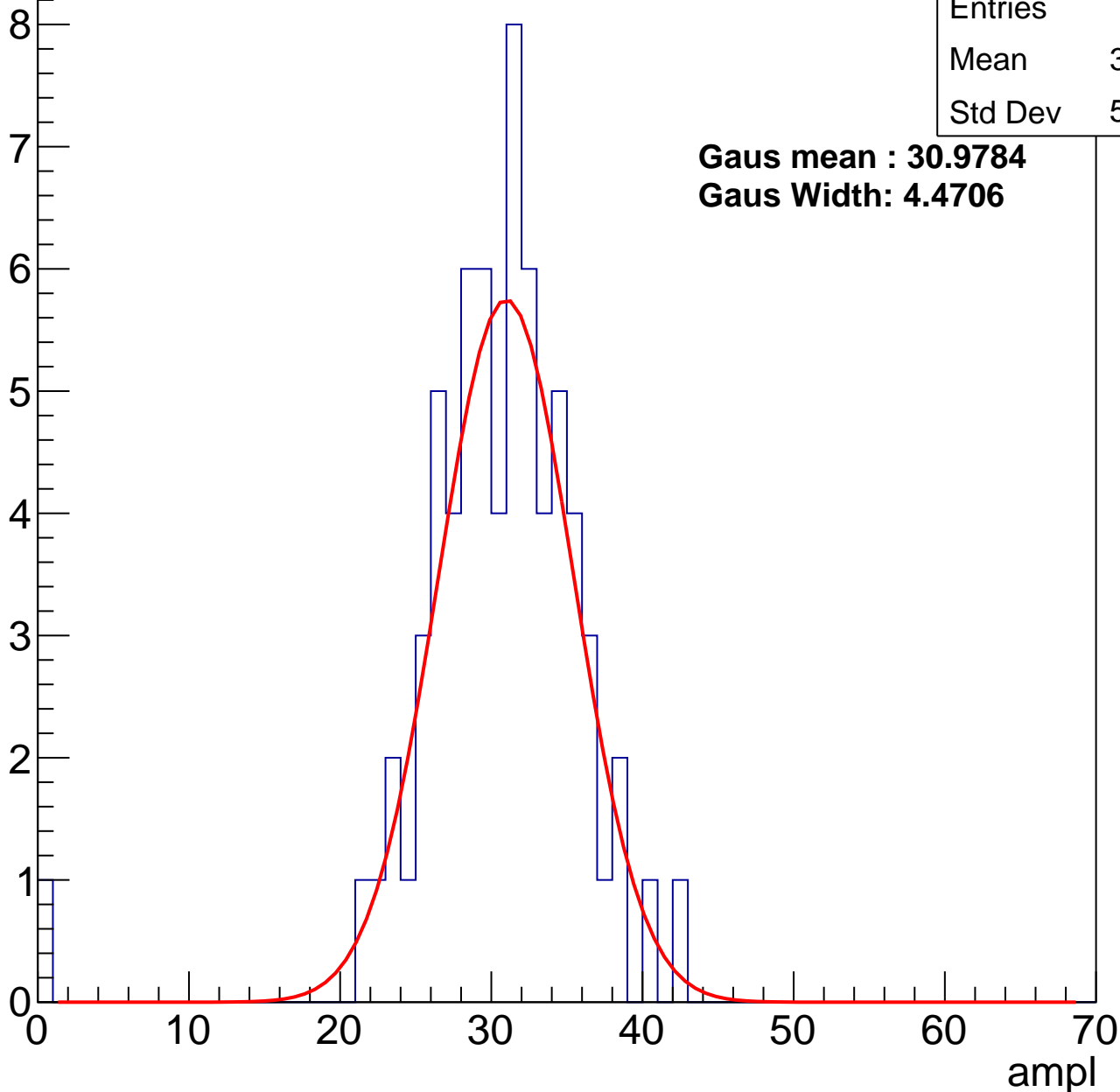
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	30.04
Std Dev	5.617

**Gaus mean : 30.9784**

**Gaus Width: 4.4706**



# B1L101S, U22-ch86, adc1

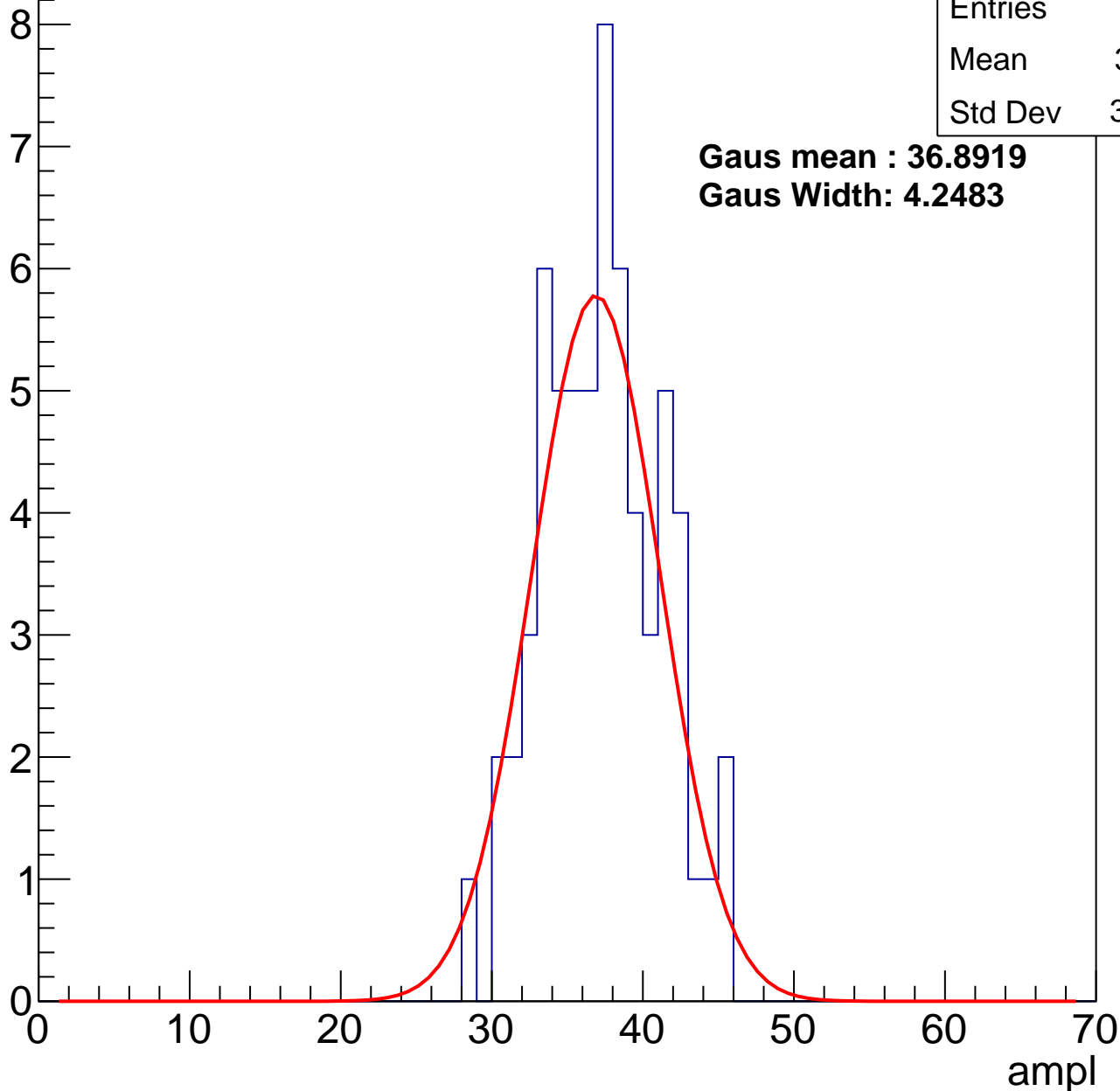
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	36.81
Std Dev	3.846

**Gaus mean : 36.8919**

**Gaus Width: 4.2483**



# B1L101S, U22-ch86, adc2

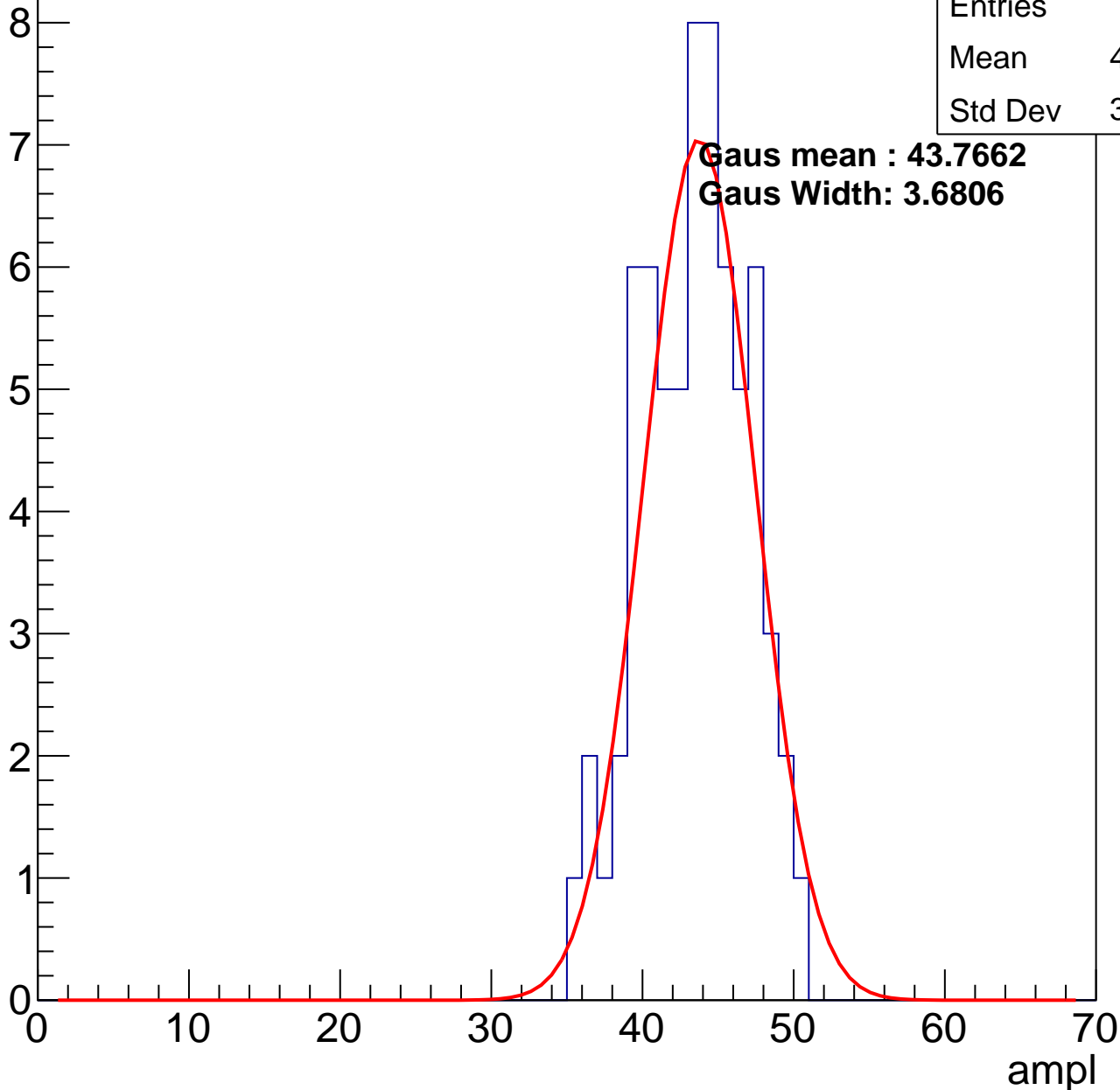
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	67
Mean	42.97
Std Dev	3.438

**Gaus mean : 43.7662**

**Gaus Width: 3.6806**

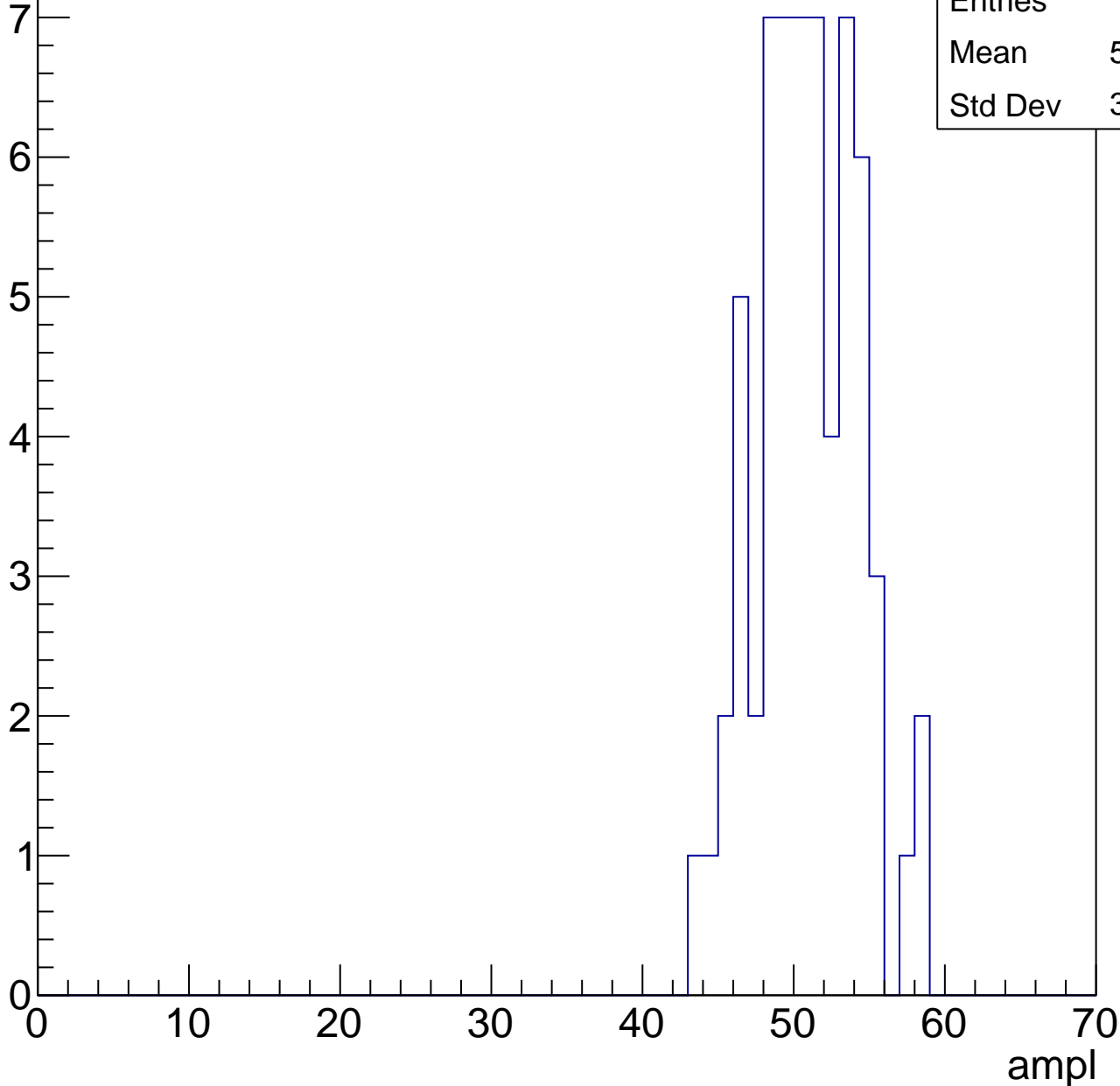


# B1L101S, U22-ch86, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

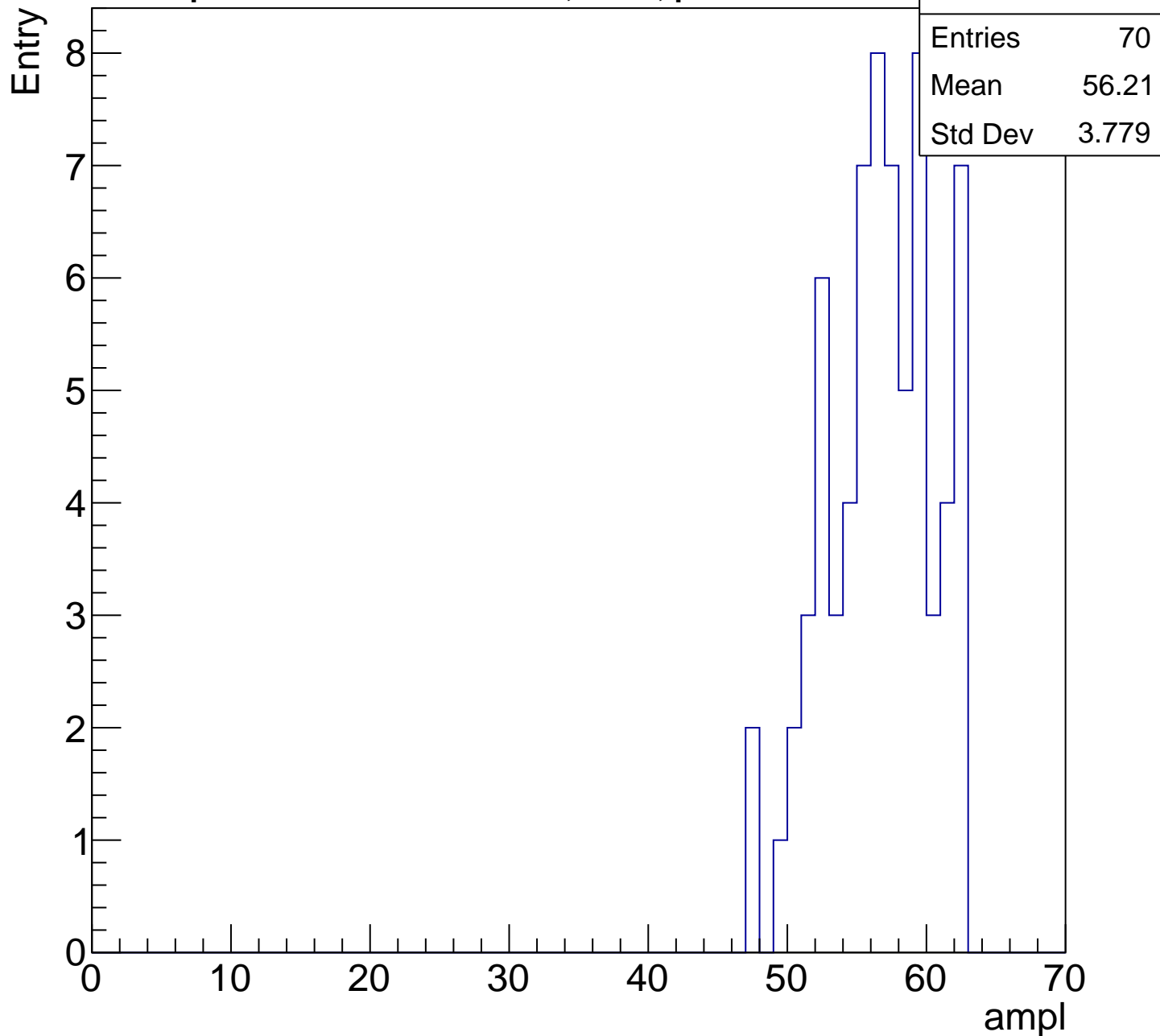
Entry

Entries	62
Mean	50.45
Std Dev	3.334



# B1L101S, U22-ch86, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

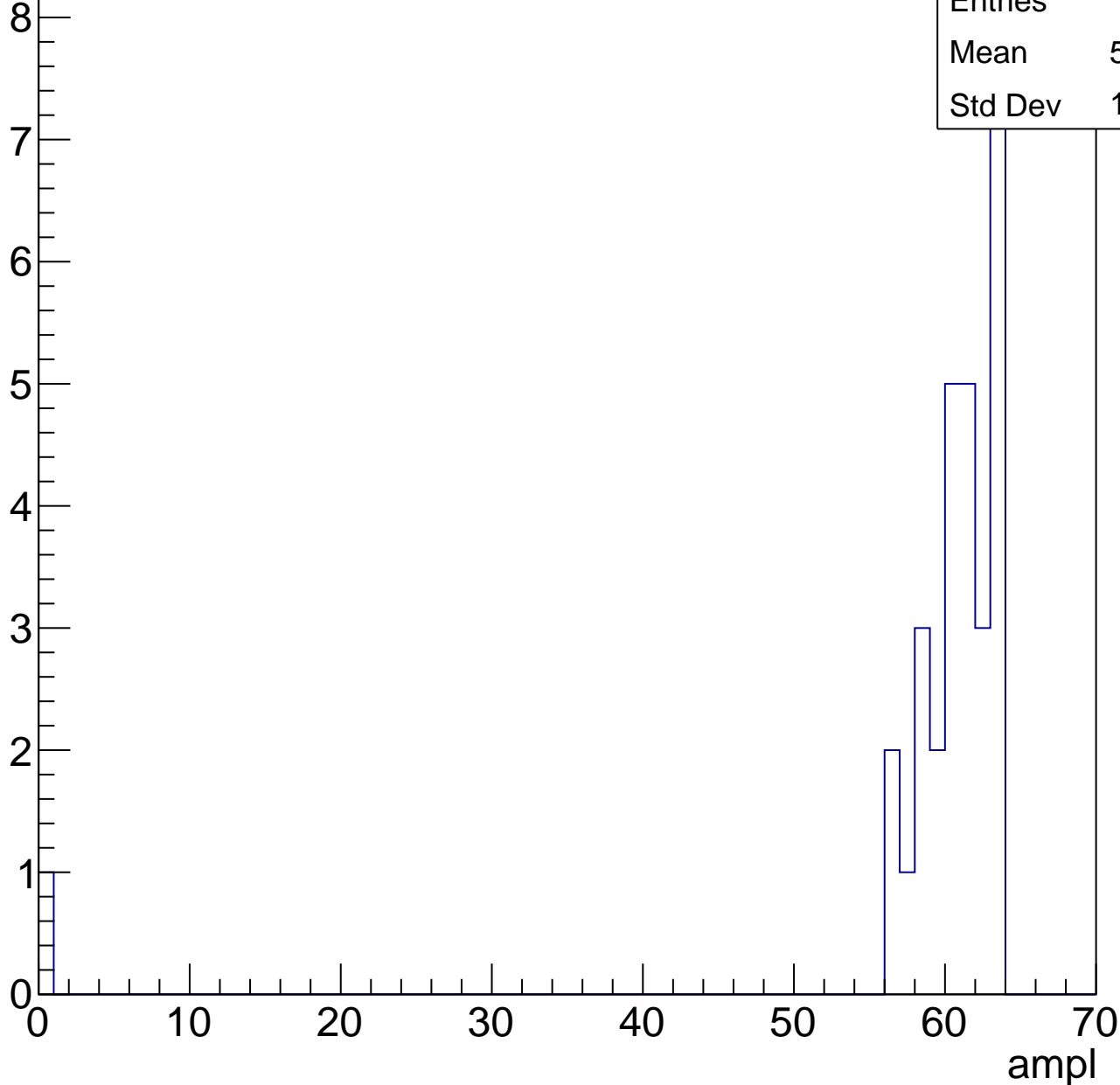


# B1L101S, U22-ch86, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

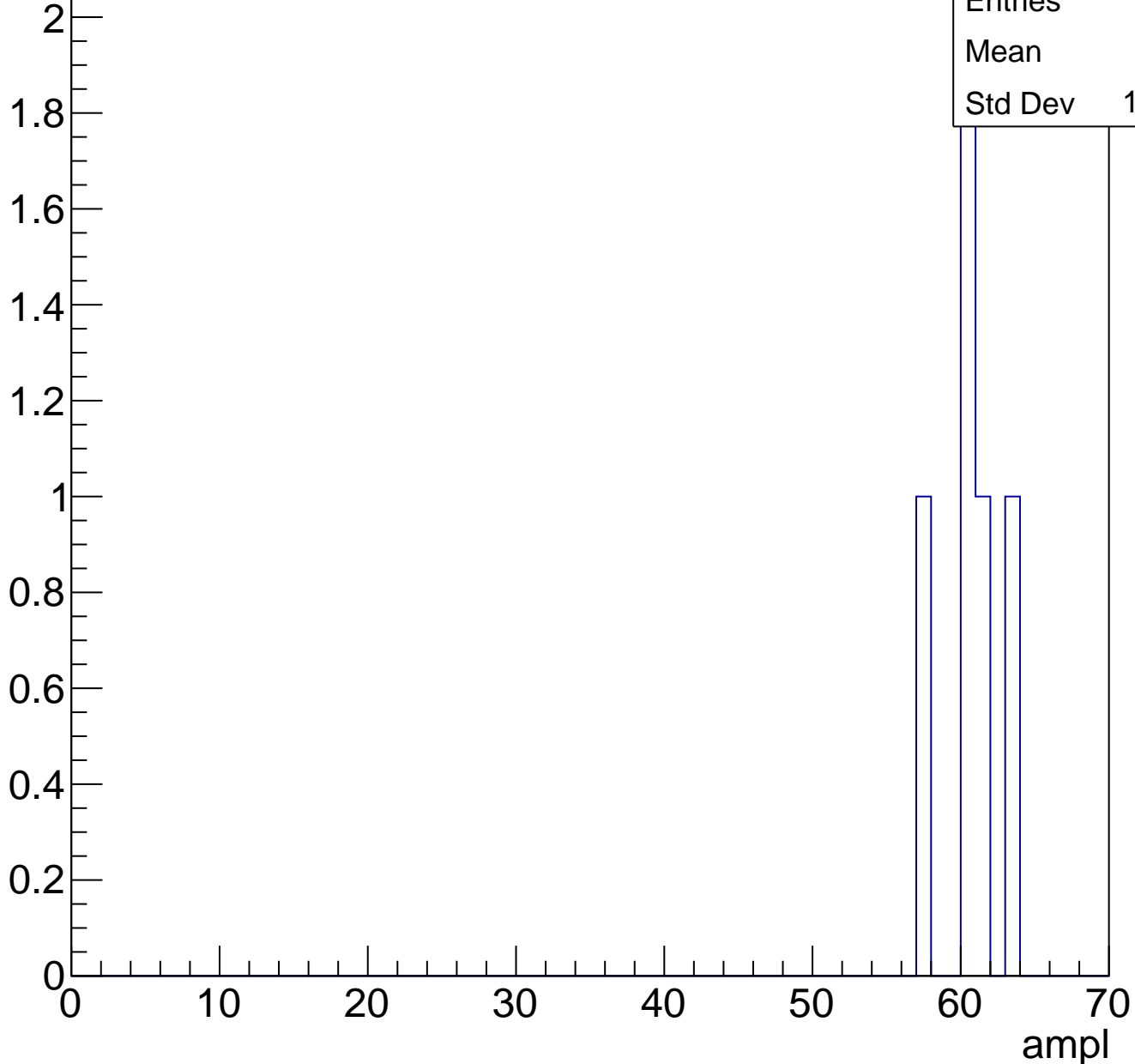
Entries	30
Mean	58.53
Std Dev	11.07



# B1L101S, U22-ch86, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



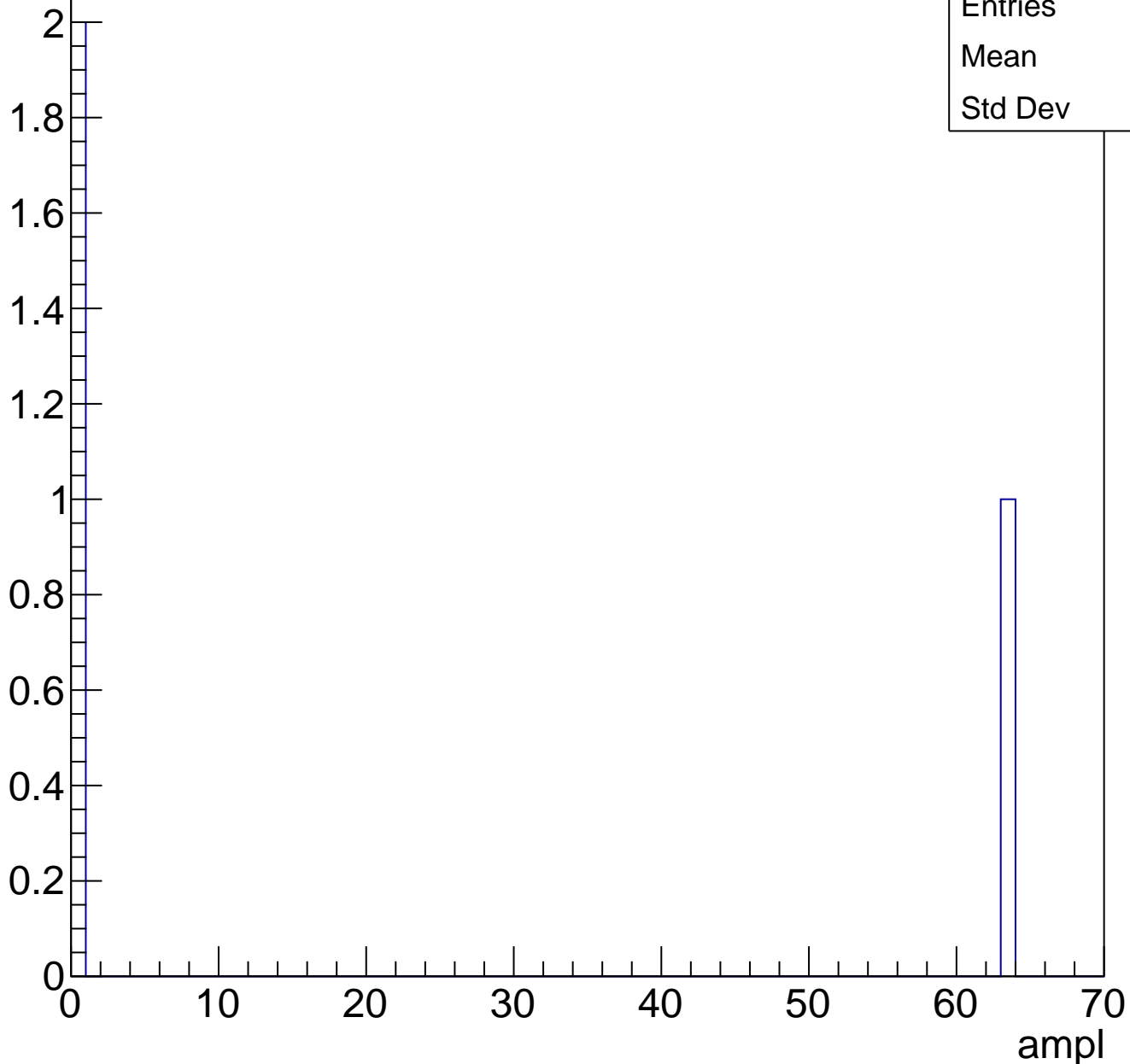
Entries	5
Mean	60.2
Std Dev	1.939



# B1L101S, U22-ch86, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	3
Mean	21
Std Dev	29.7

# B1L101S, U22-ch87, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	83
Mean	29.69
Std Dev	3.789

**Gaus mean : 30.0096**

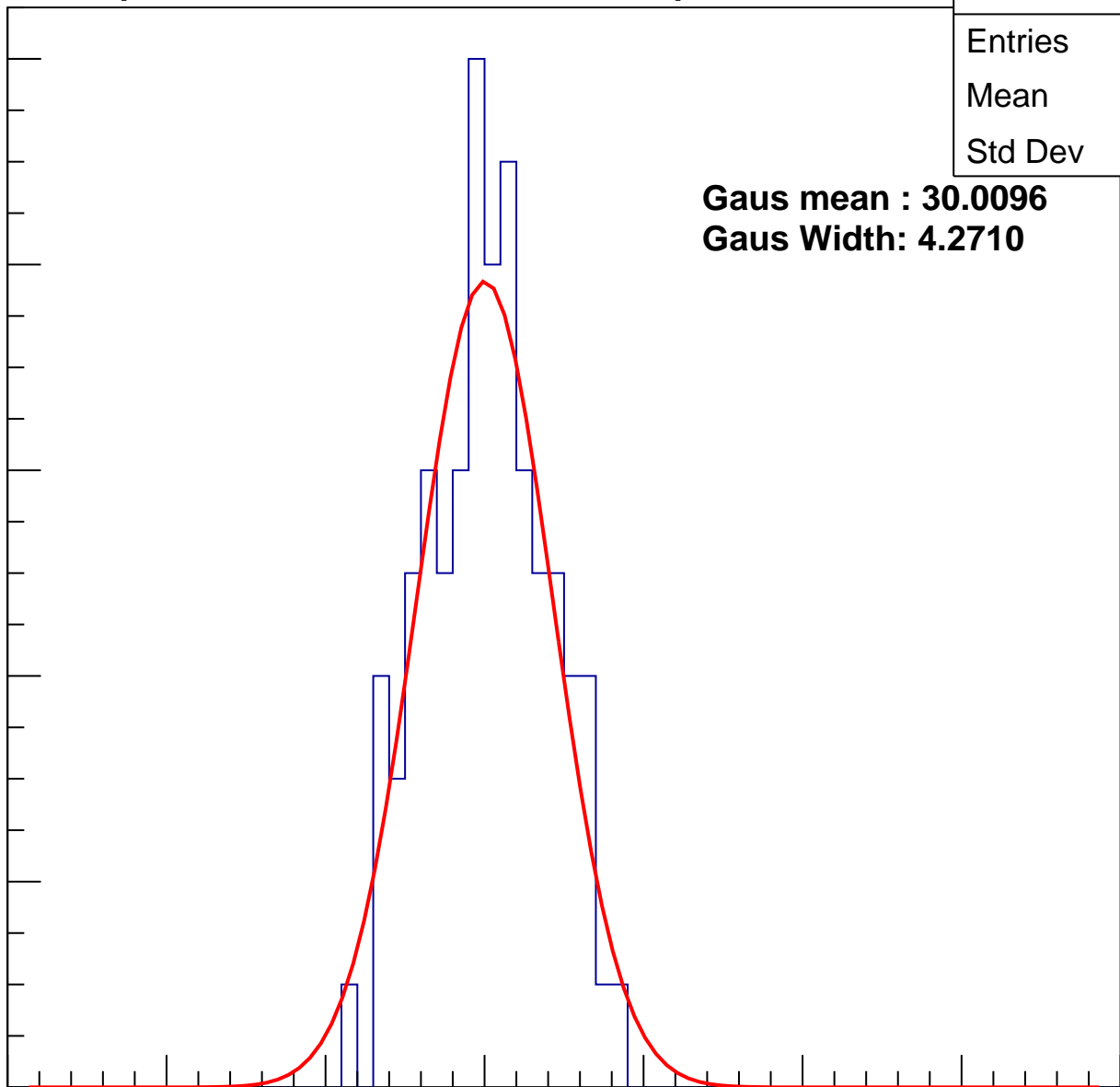
**Gaus Width: 4.2710**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U22-ch87, adc1

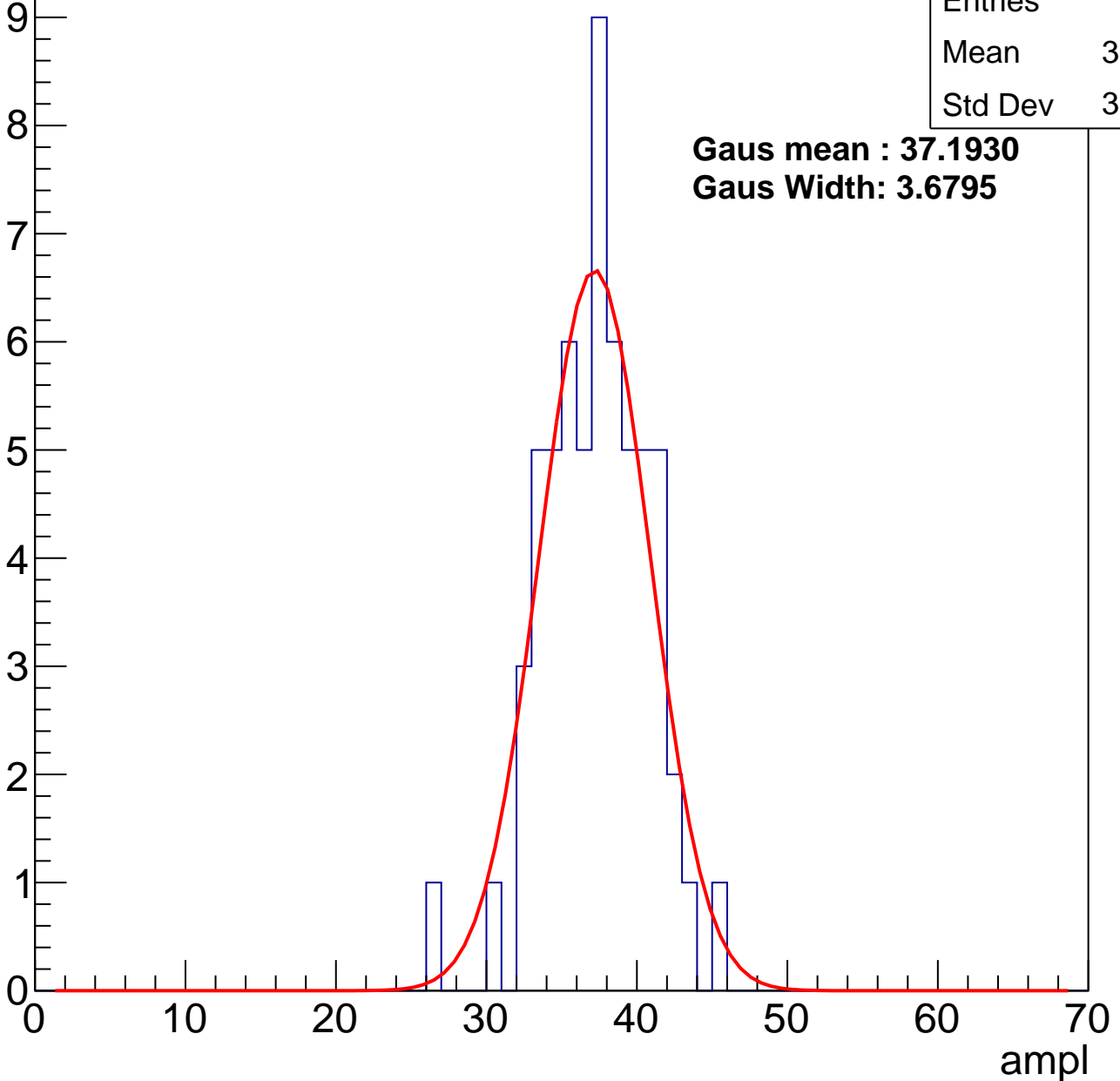
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	60
Mean	36.83
Std Dev	3.412

**Gaus mean : 37.1930**

**Gaus Width: 3.6795**



# B1L101S, U22-ch87, adc2

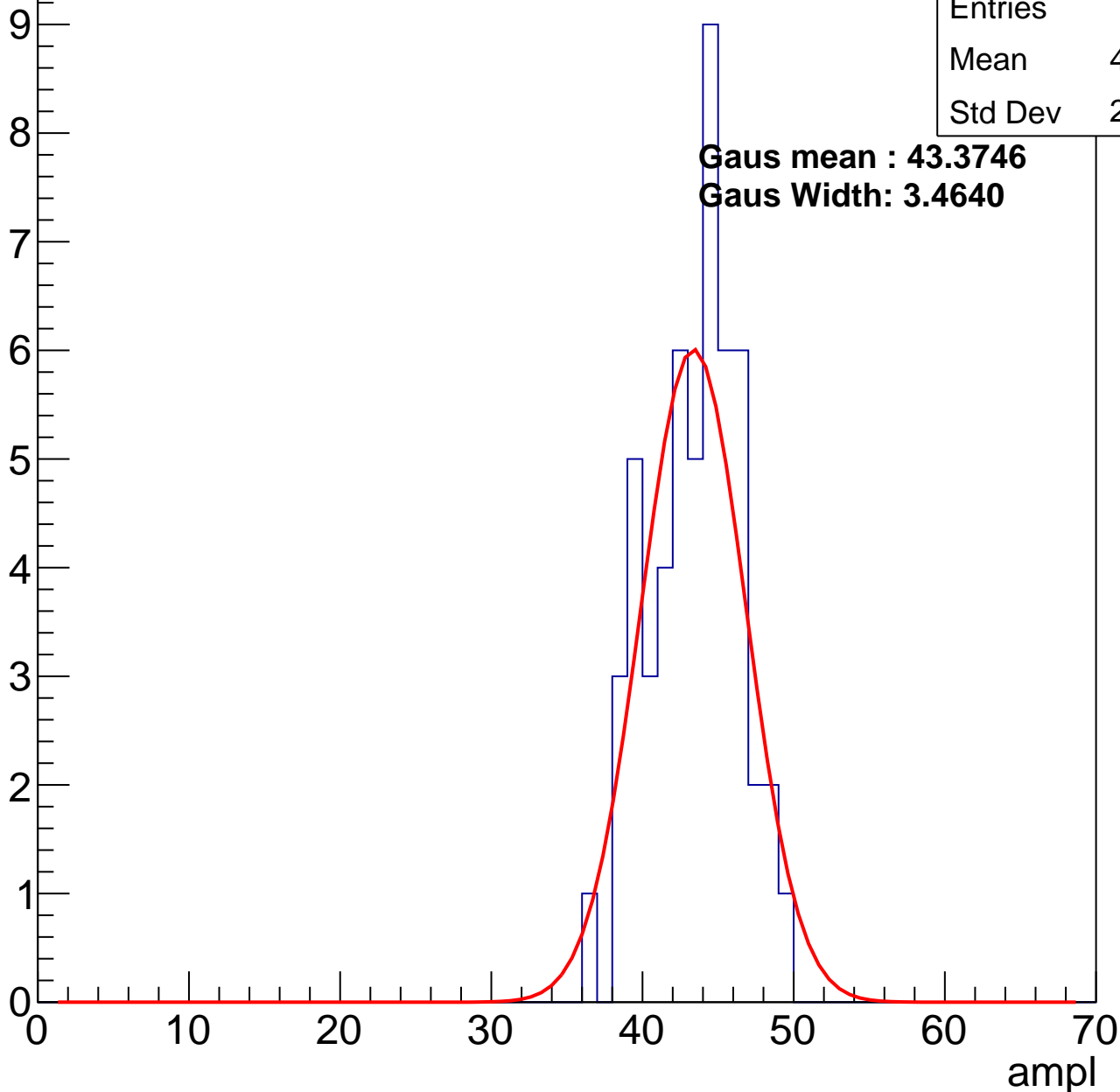
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	53
Mean	42.96
Std Dev	2.939

**Gaus mean : 43.3746**

**Gaus Width: 3.4640**



# B1L101S, U22-ch87, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	101
Mean	50.31
Std Dev	4.256

Entry

10

8

6

4

2

0

0

10

20

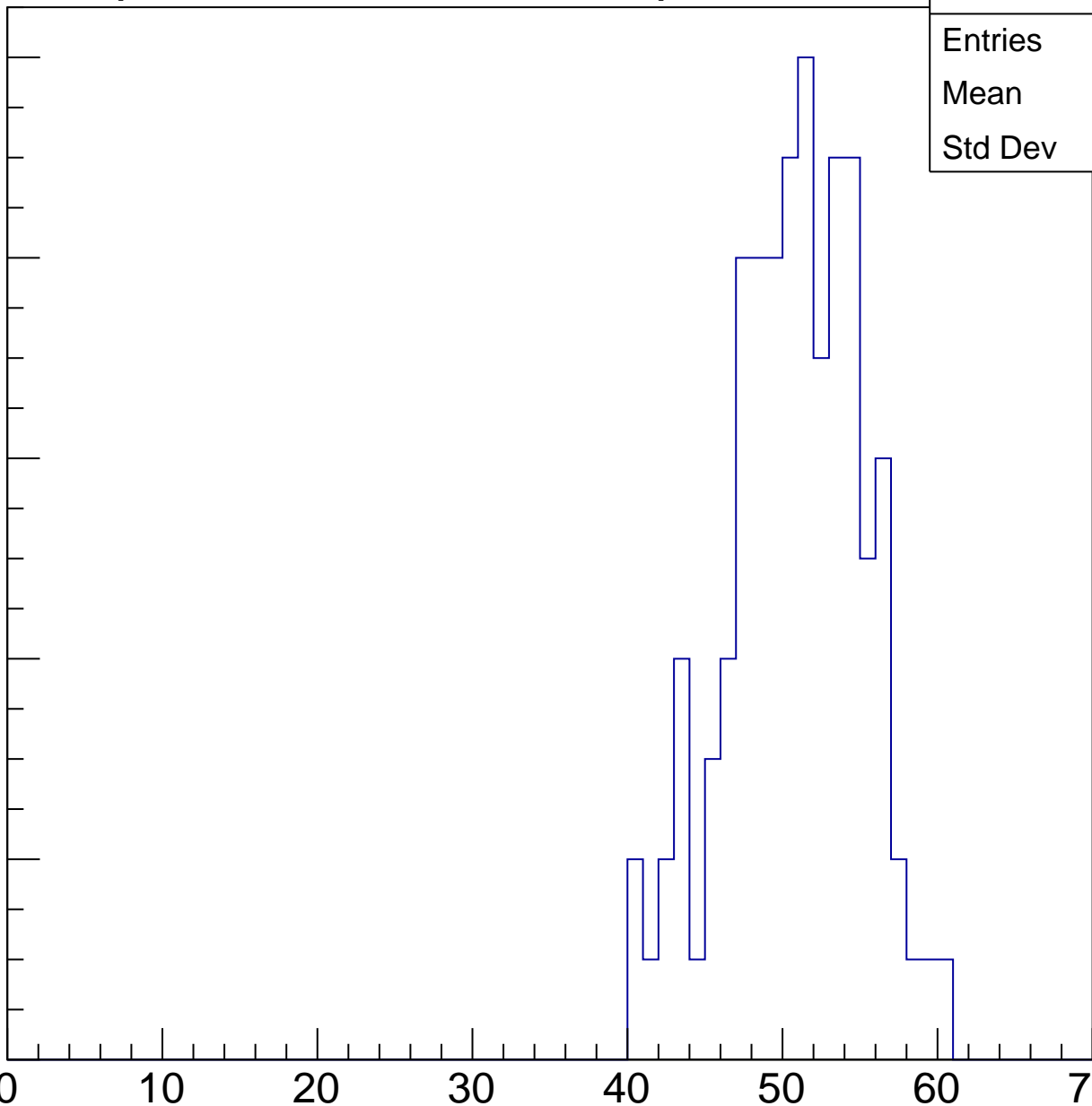
30

40

50

60

ampl

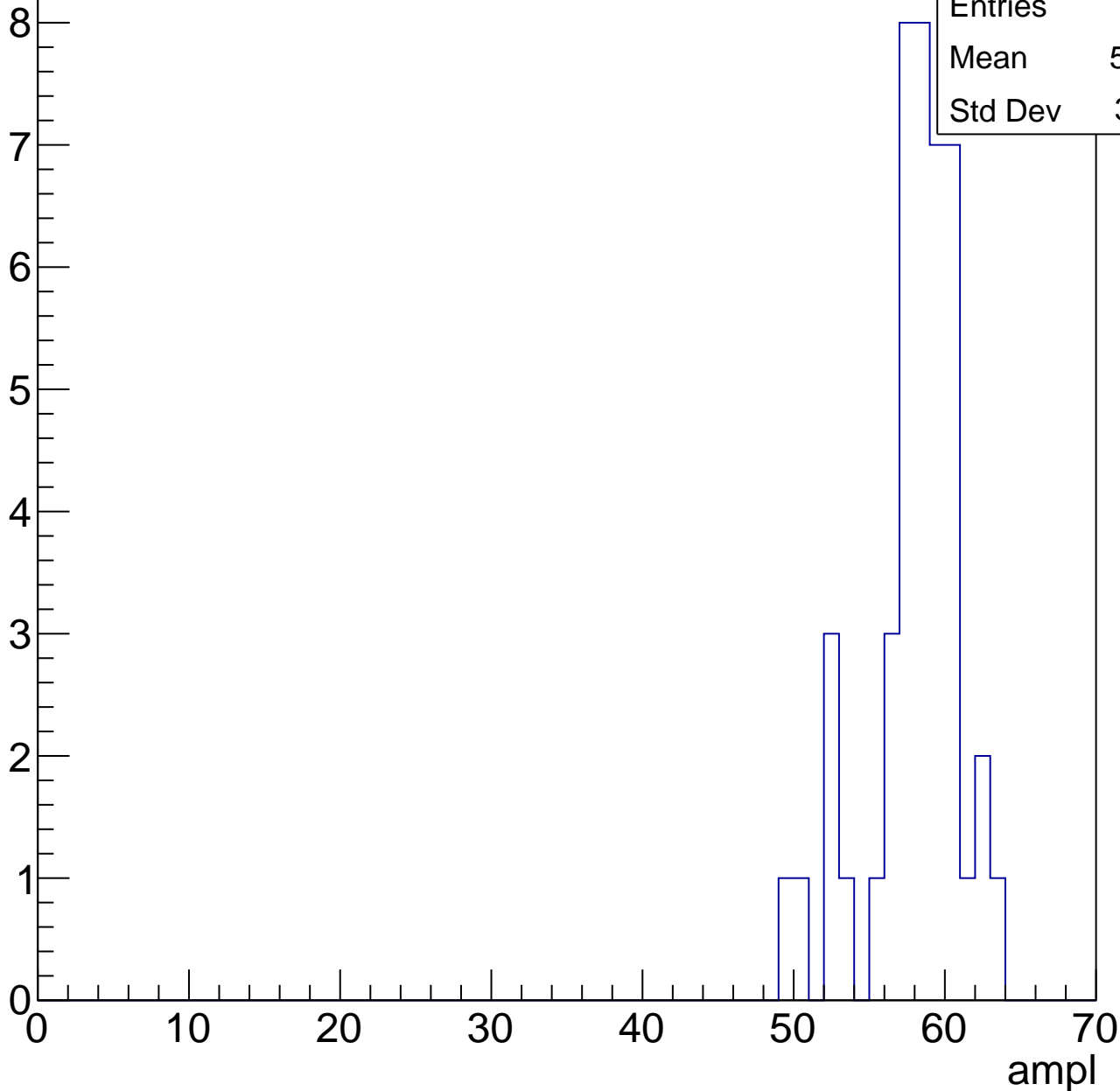


# B1L101S, U22-ch87, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

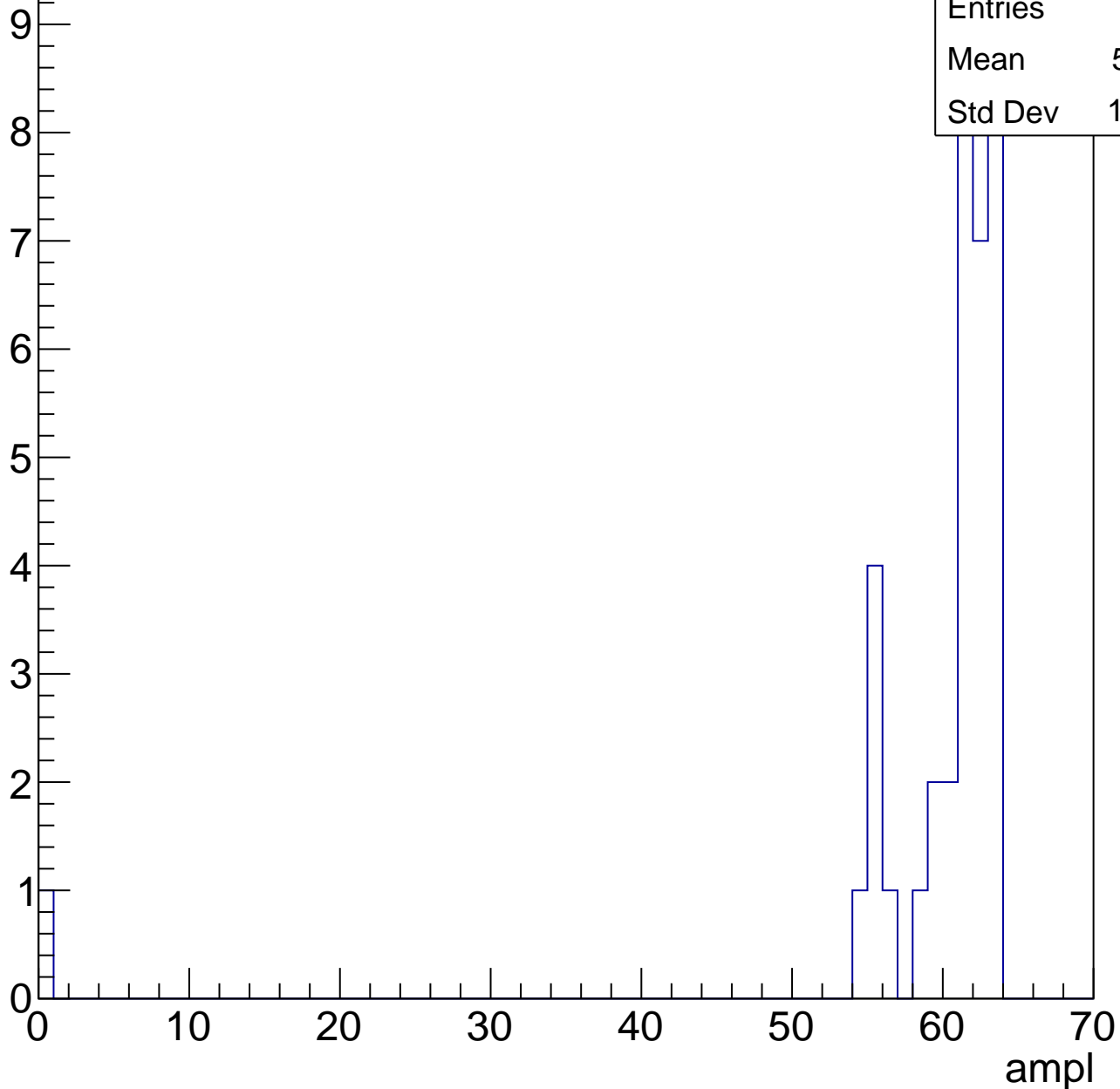
Entries	44
Mean	57.55
Std Dev	3.011



# B1L101S, U22-ch87, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	37
Mean	58.81
Std Dev	10.17

# B1L101S, U22-ch87, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U22-ch87, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U22-ch88, adc0

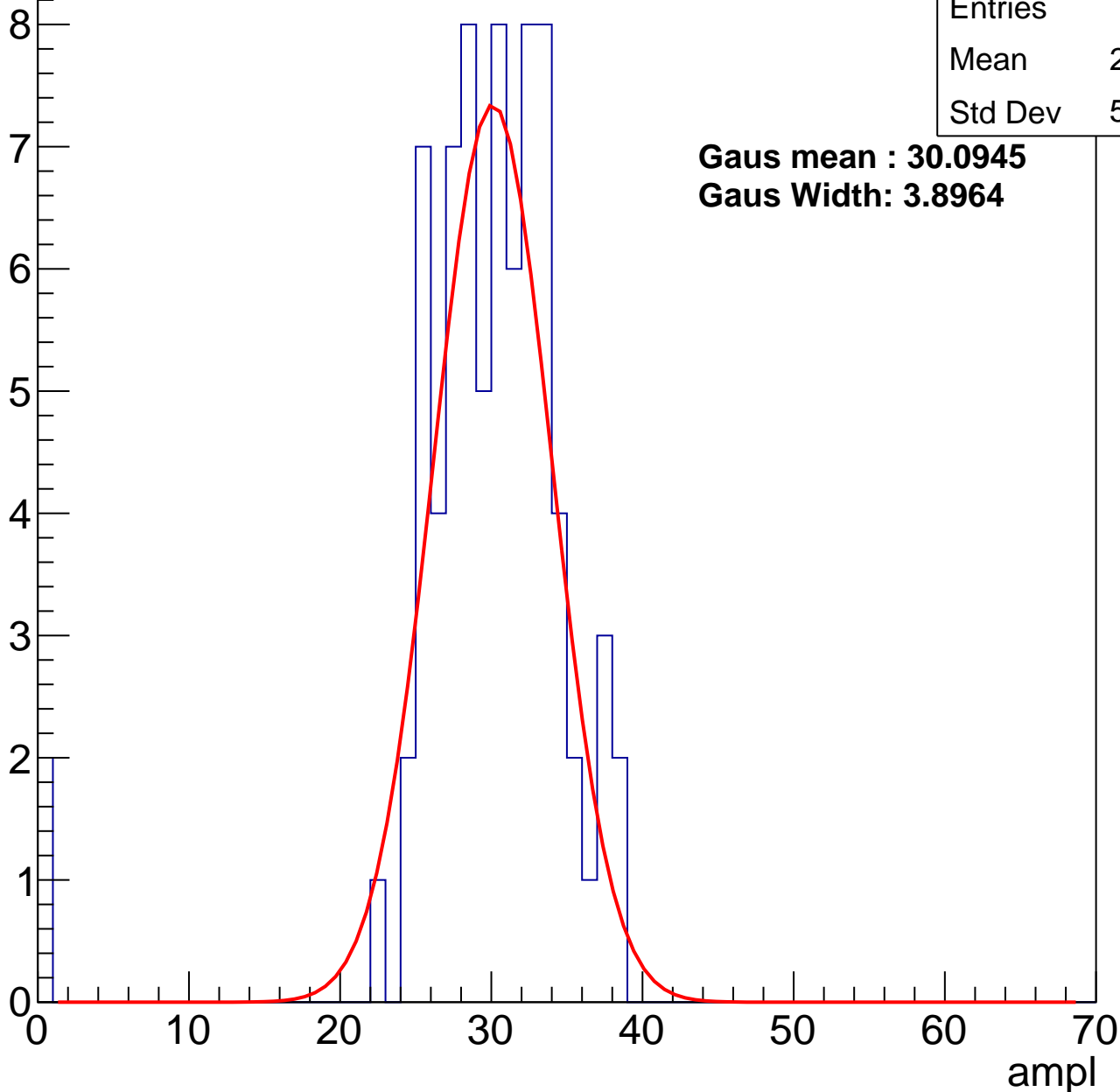
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	78
Mean	29.26
Std Dev	5.956

**Gaus mean : 30.0945**

**Gaus Width: 3.8964**



# B1L101S, U22-ch88, adc1

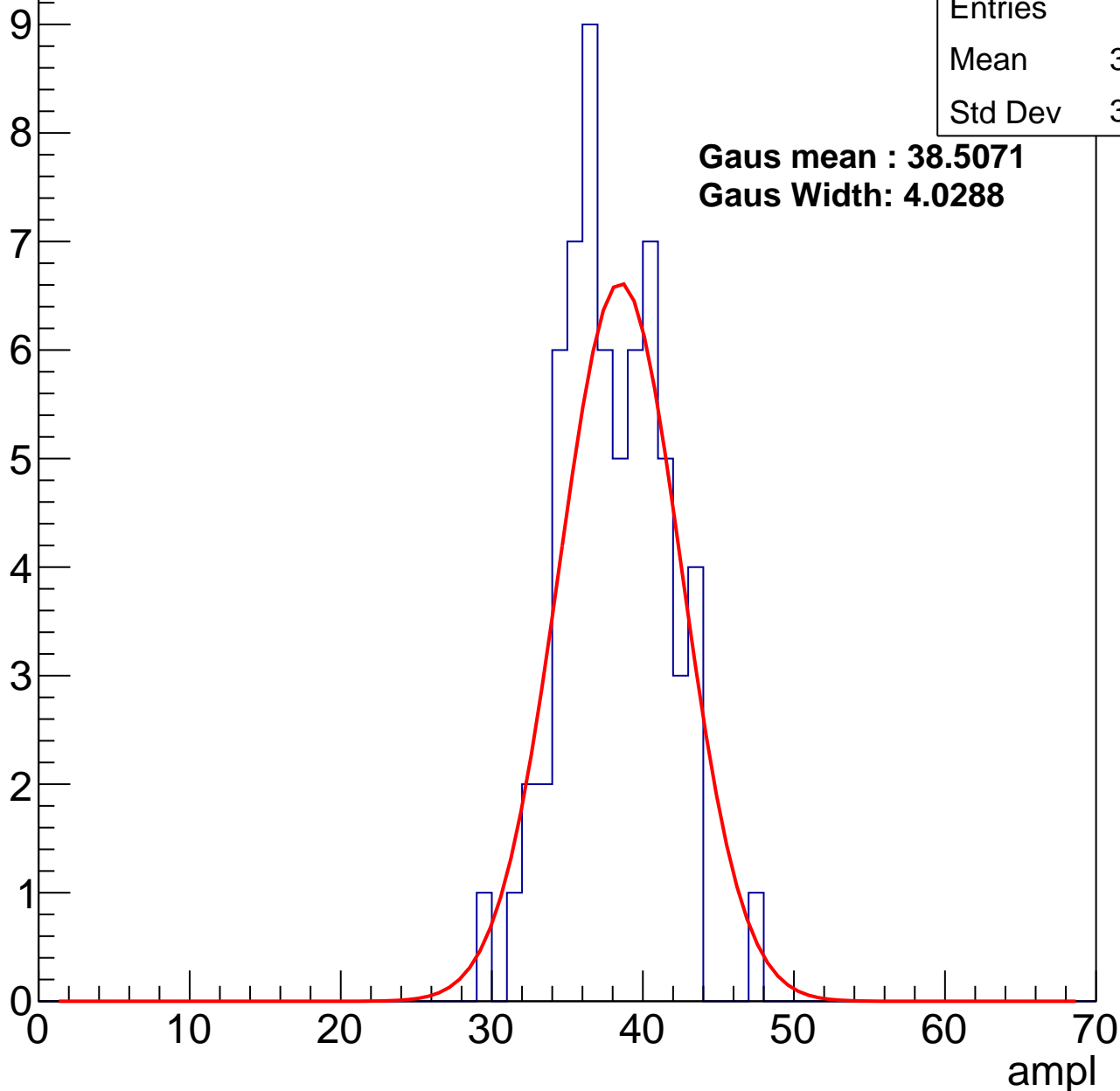
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	37.52
Std Dev	3.388

**Gaus mean : 38.5071**

**Gaus Width: 4.0288**



# B1L101S, U22-ch88, adc2

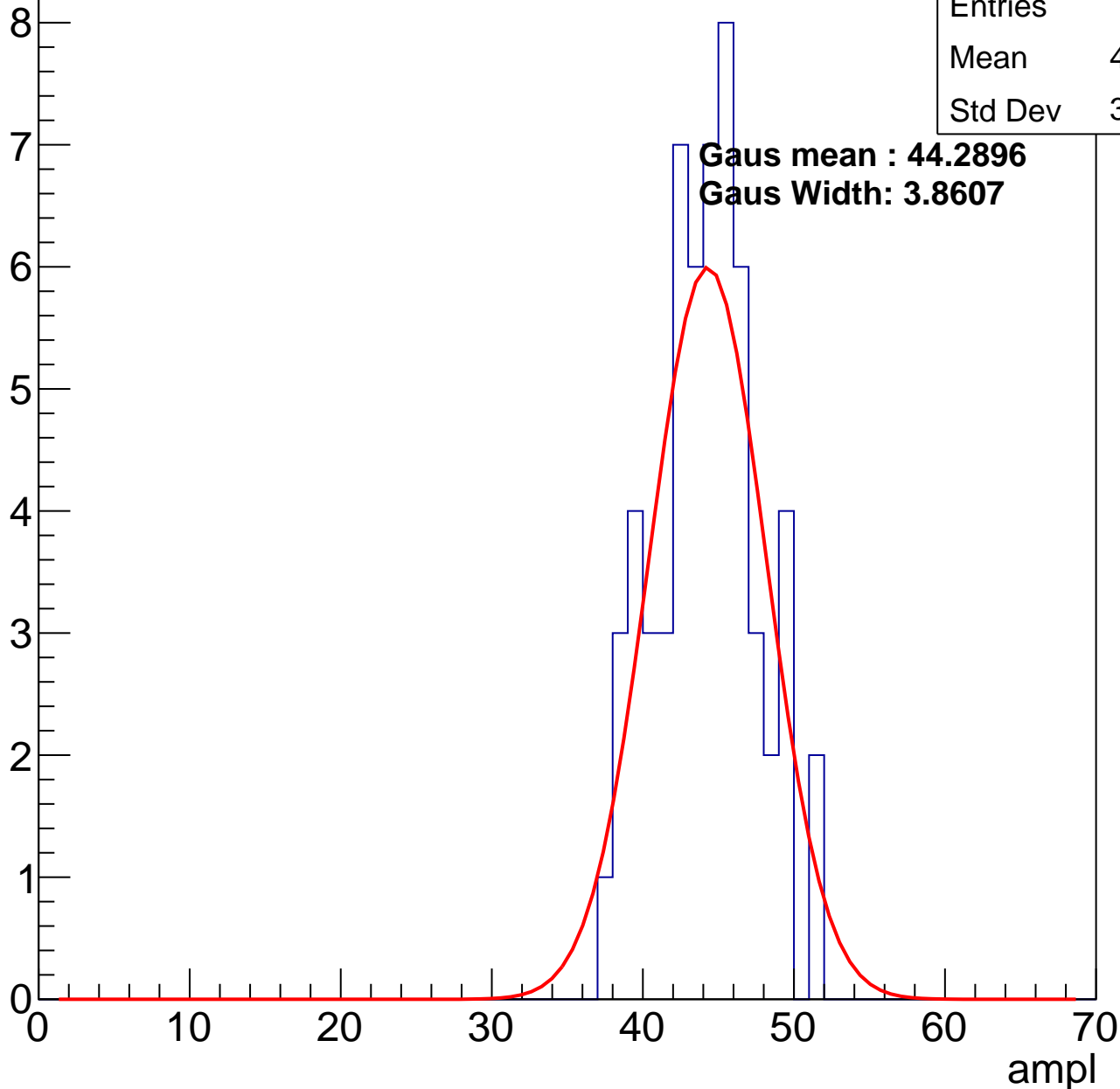
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	59
Mean	43.75
Std Dev	3.322

**Gaus mean : 44.2896**

**Gaus Width: 3.8607**

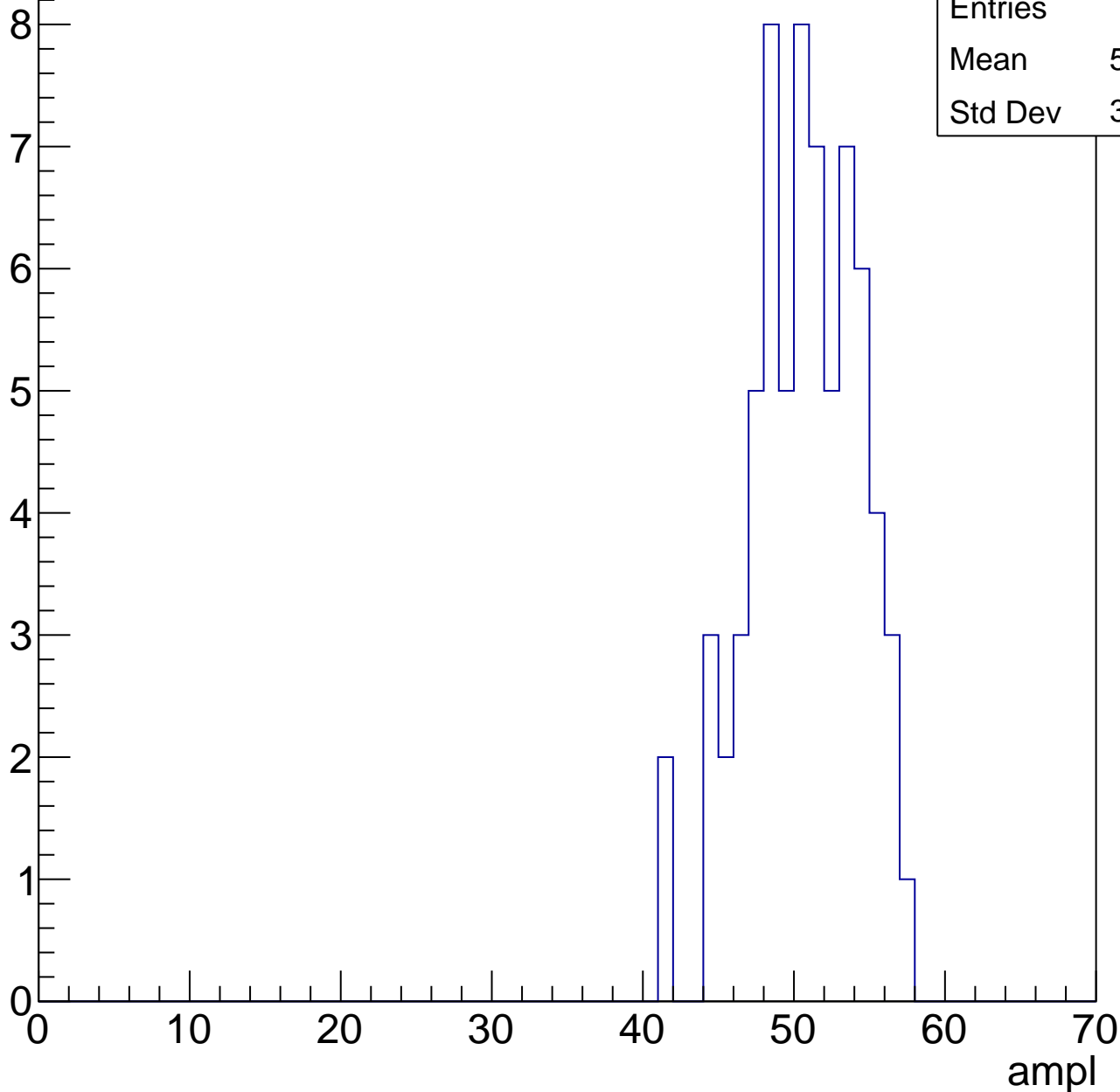


# B1L101S, U22-ch88, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	50.19
Std Dev	3.593

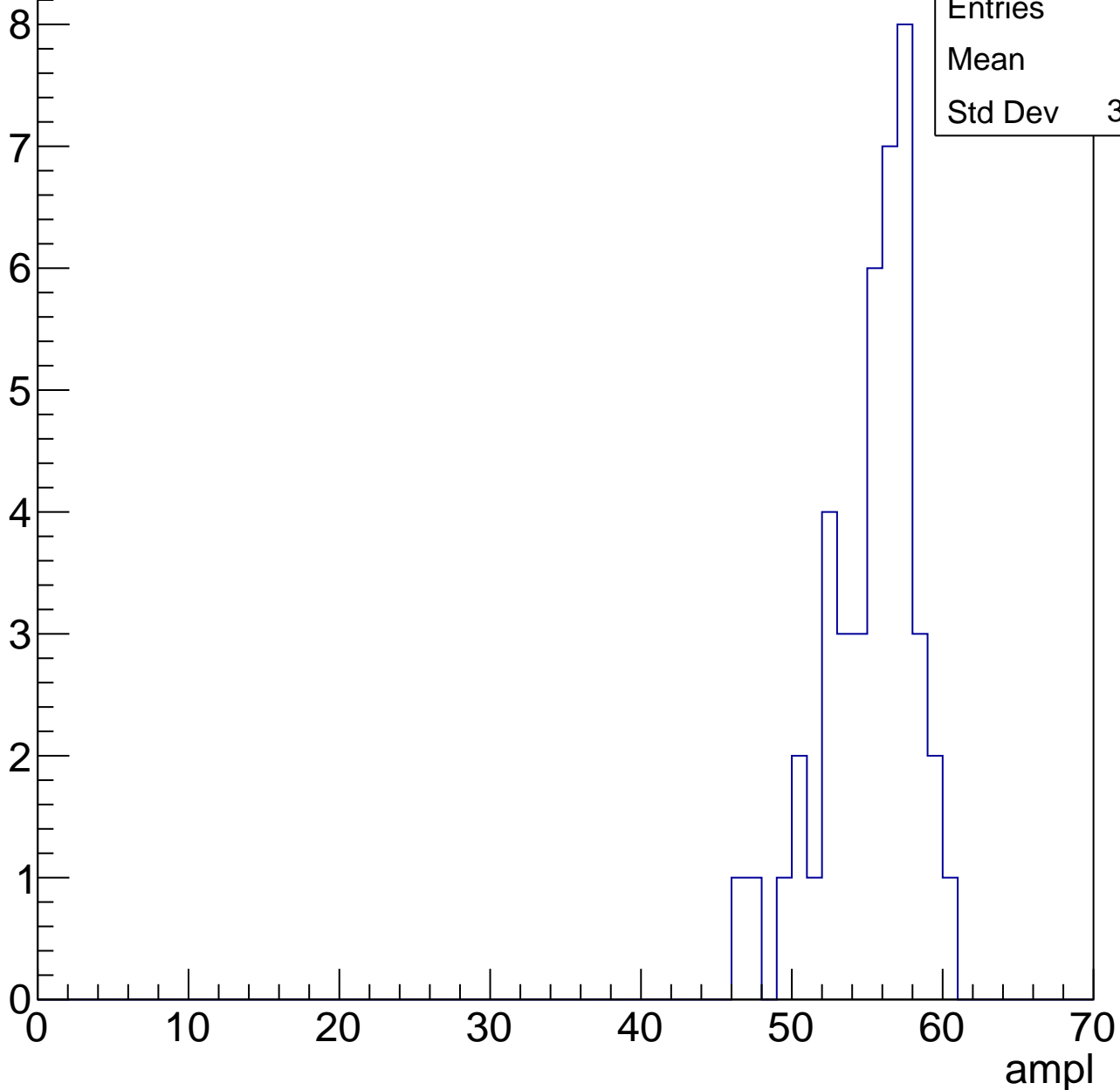


# B1L101S, U22-ch88, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	43
Mean	54.7
Std Dev	3.114



# B1L101S, U22-ch88, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

10

8

6

4

2

0

0

10

20

30

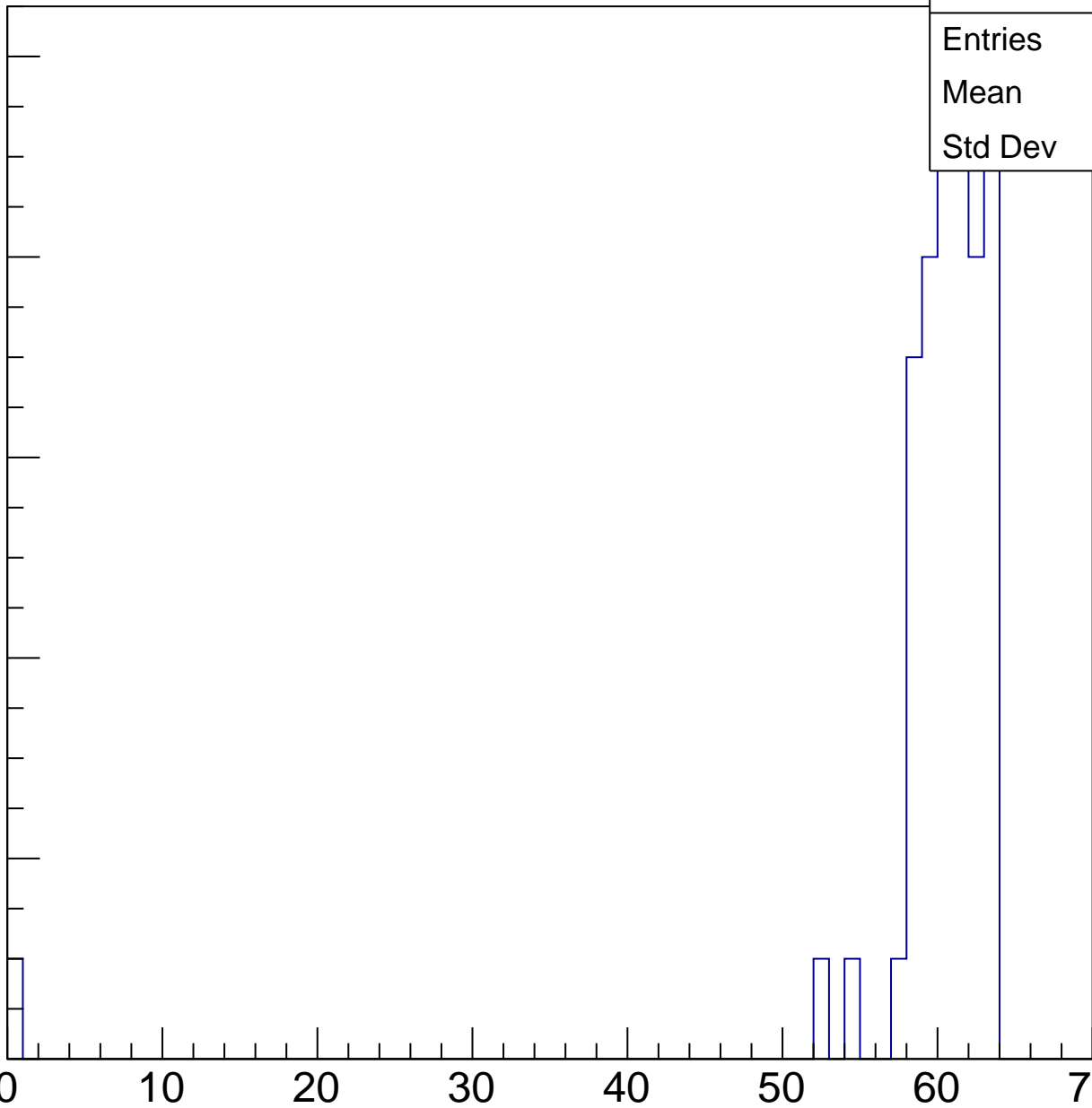
40

50

60

ampl

Entries	56
Mean	59.18
Std Dev	8.27



# B1L101S, U22-ch88, adc6

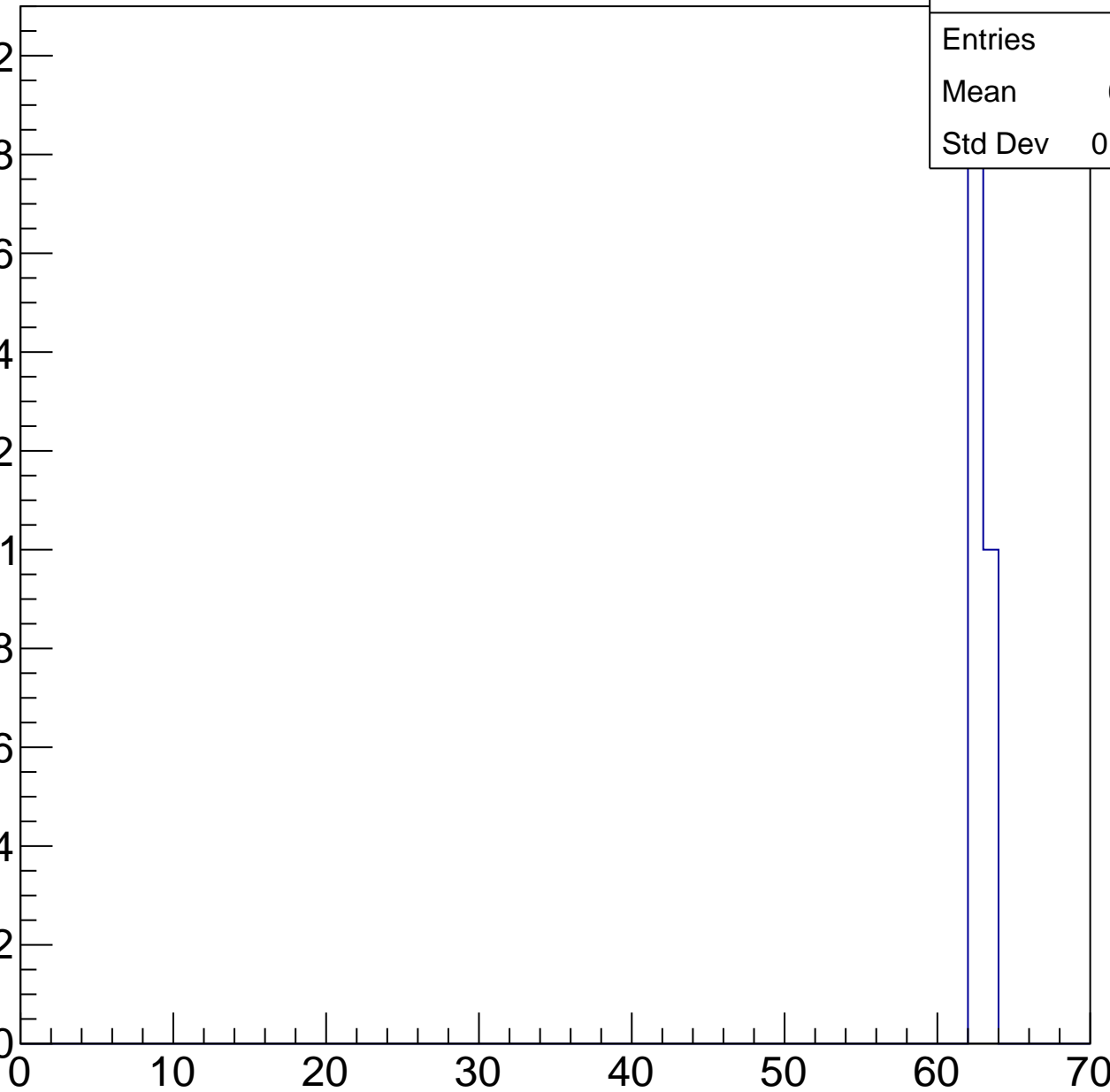
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	3
Mean	62.33
Std Dev	0.4714

ampl

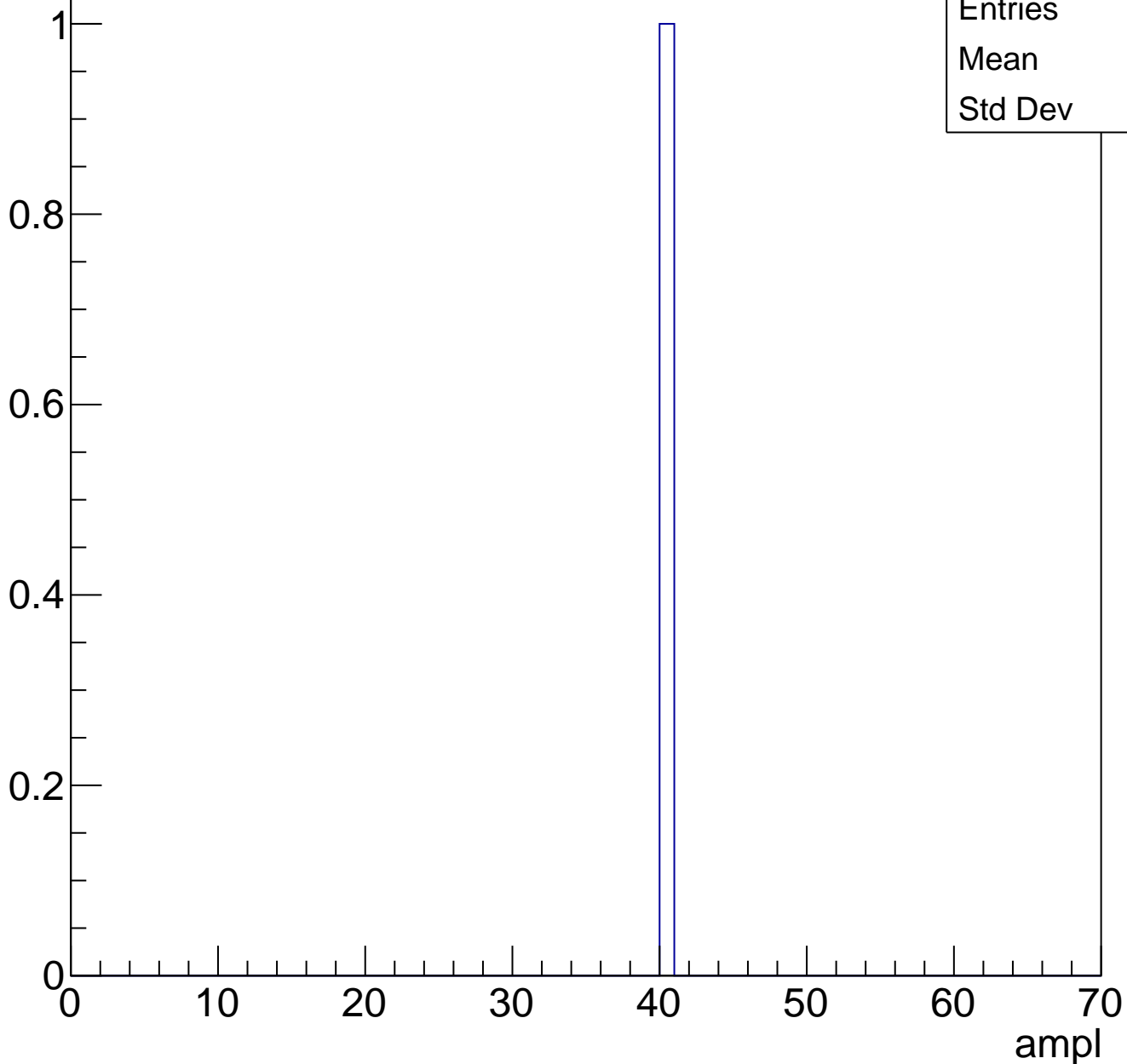




# B1L101S, U22-ch88, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U22-ch89, adc0

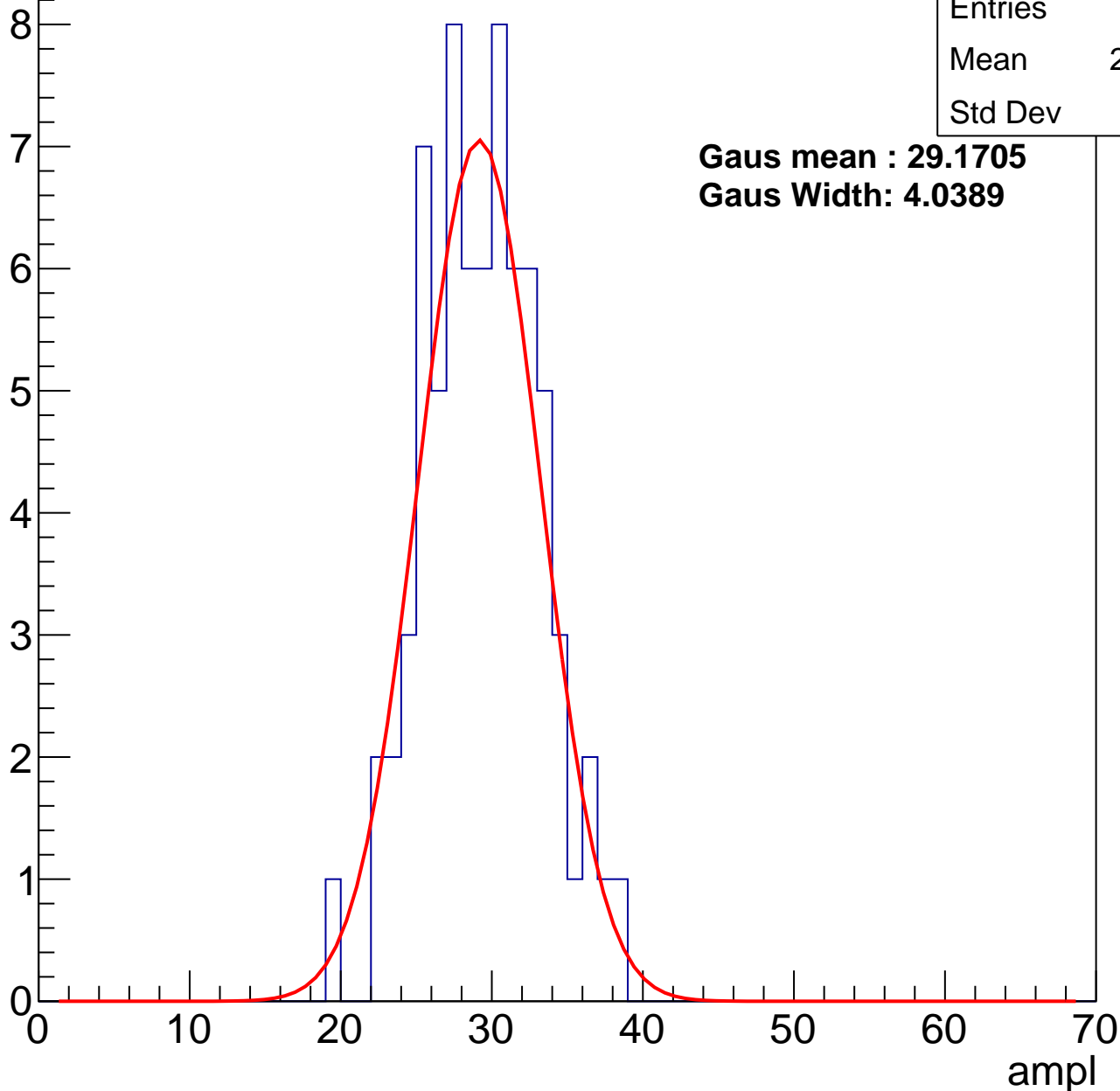
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	73
Mean	28.92
Std Dev	3.81

**Gaus mean : 29.1705**

**Gaus Width: 4.0389**



# B1L101S, U22-ch89, adc1

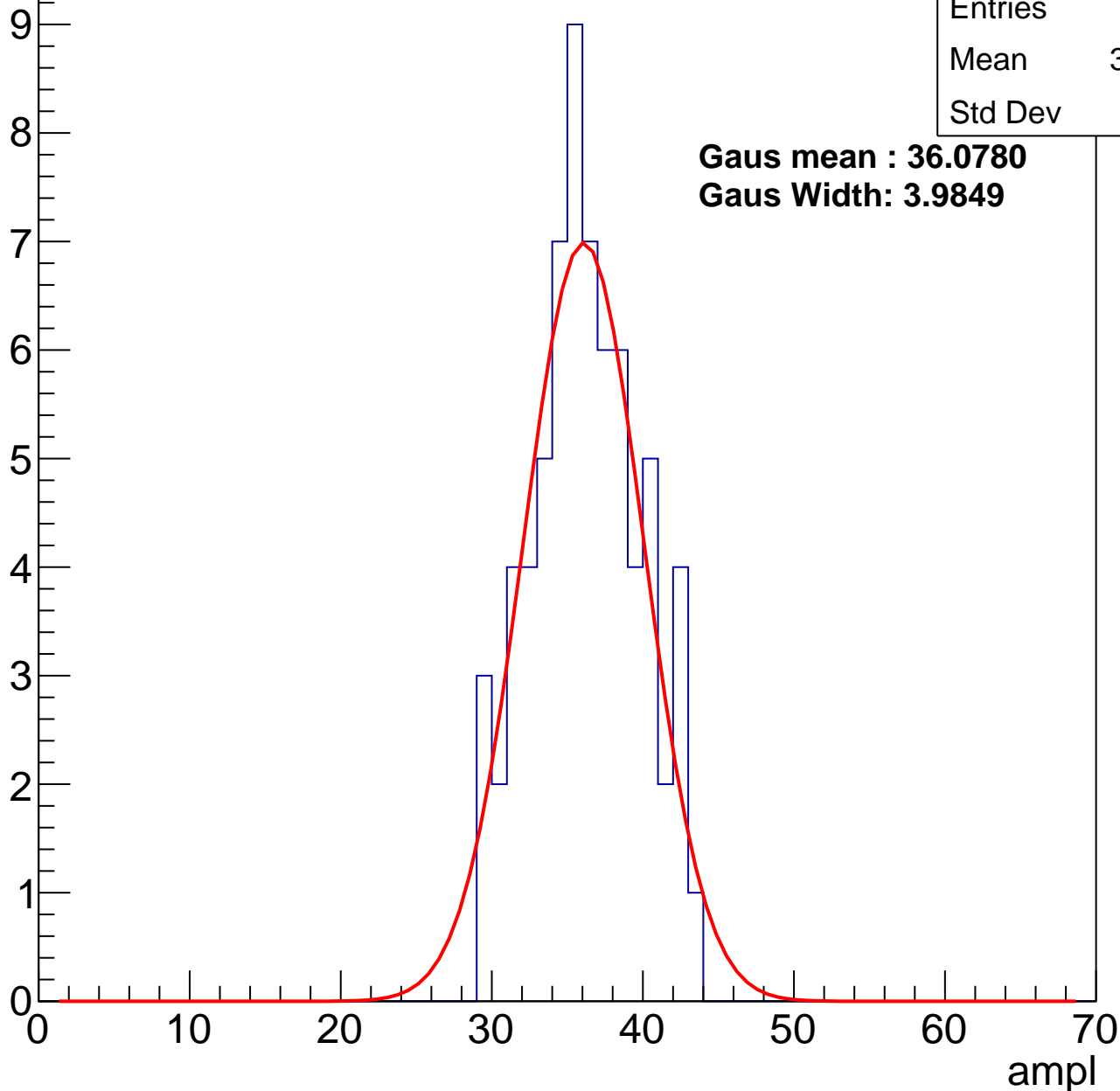
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	35.77
Std Dev	3.51

**Gaus mean : 36.0780**

**Gaus Width: 3.9849**



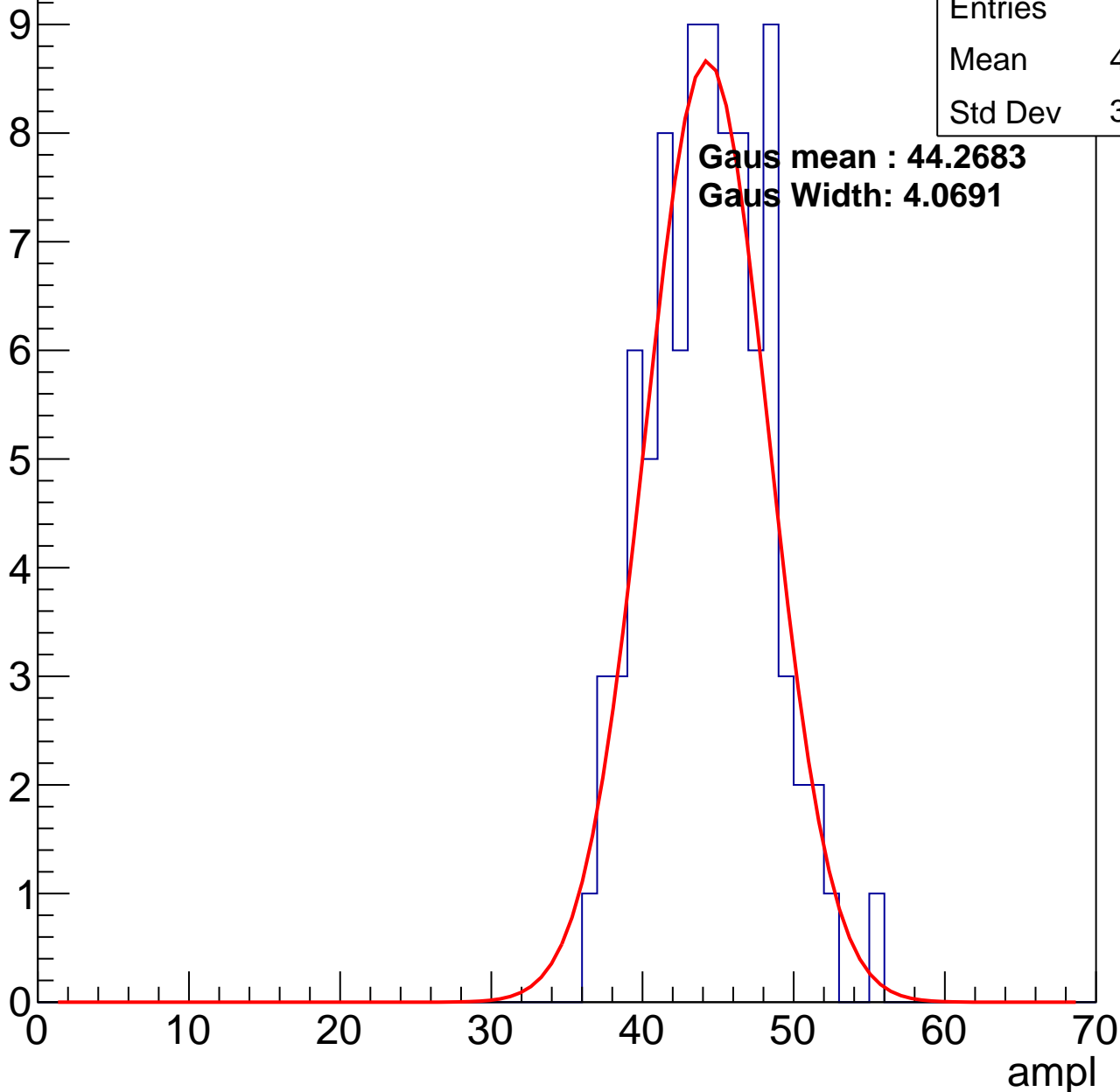
# B1L101S, U22-ch89, adc2

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	90
Mean	43.96
Std Dev	3.832

**Gaus mean : 44.2683**  
**Gaus Width: 4.0691**

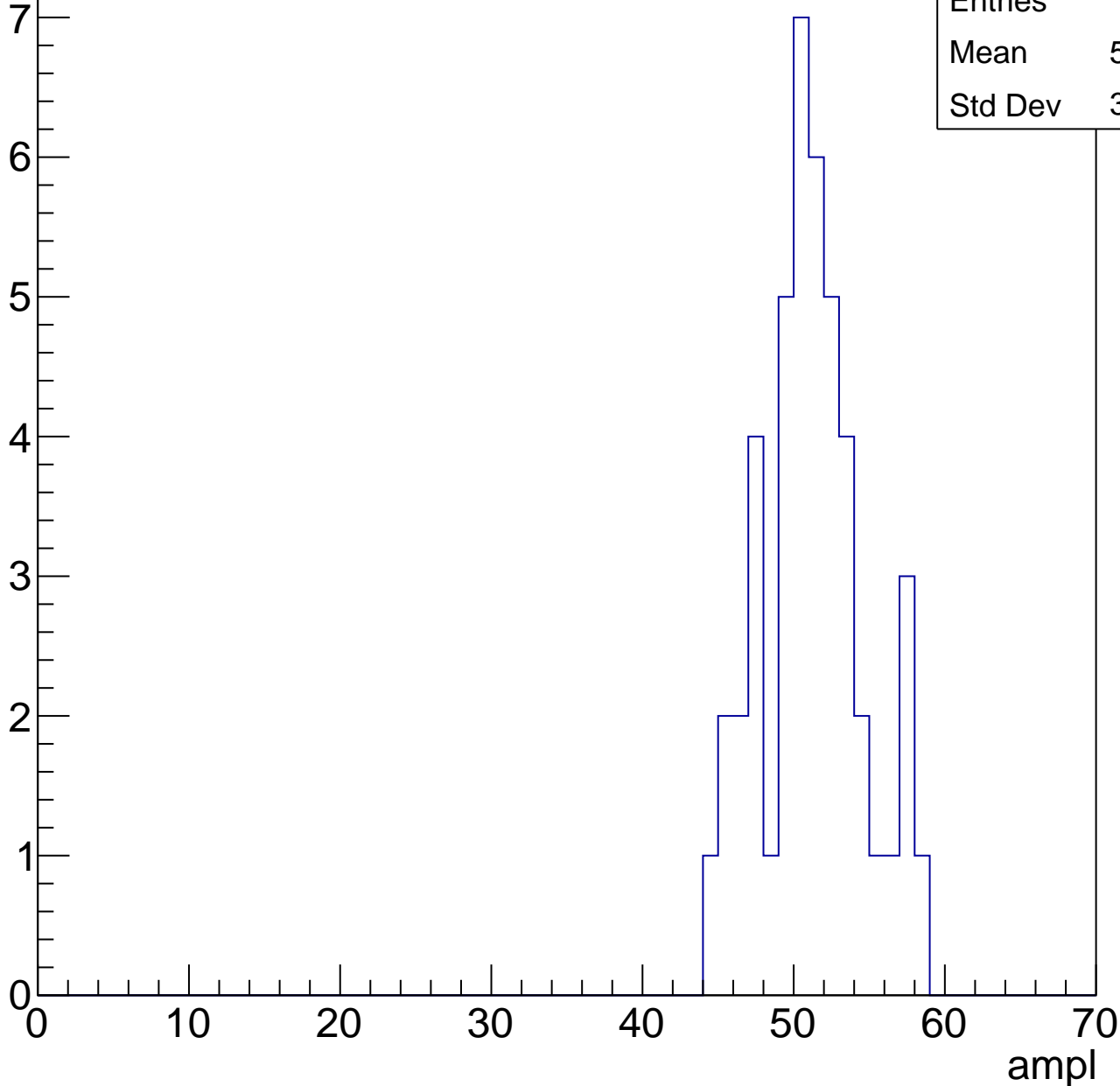


# B1L101S, U22-ch89, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	45
Mean	50.73
Std Dev	3.349

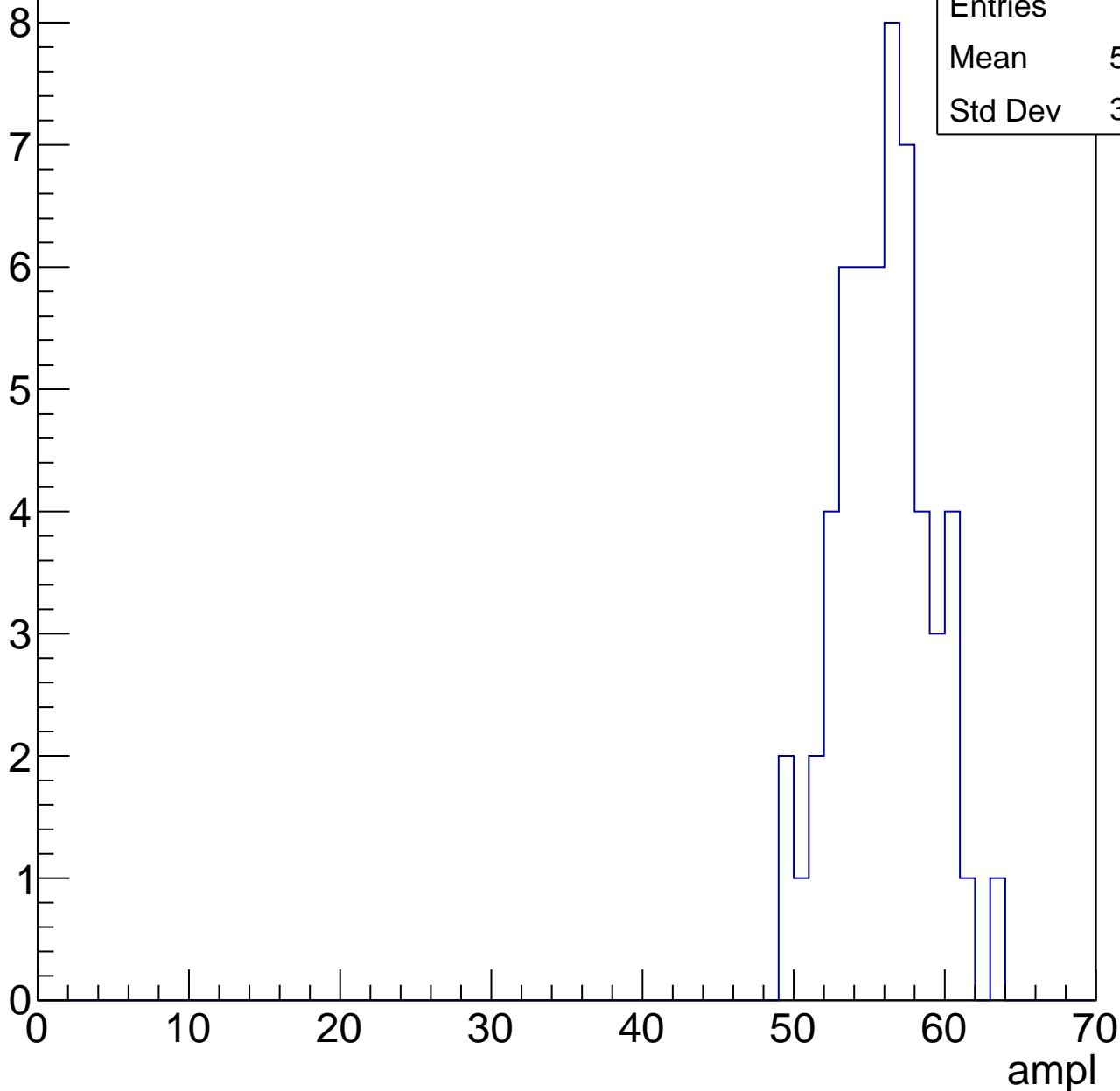


# B1L101S, U22-ch89, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

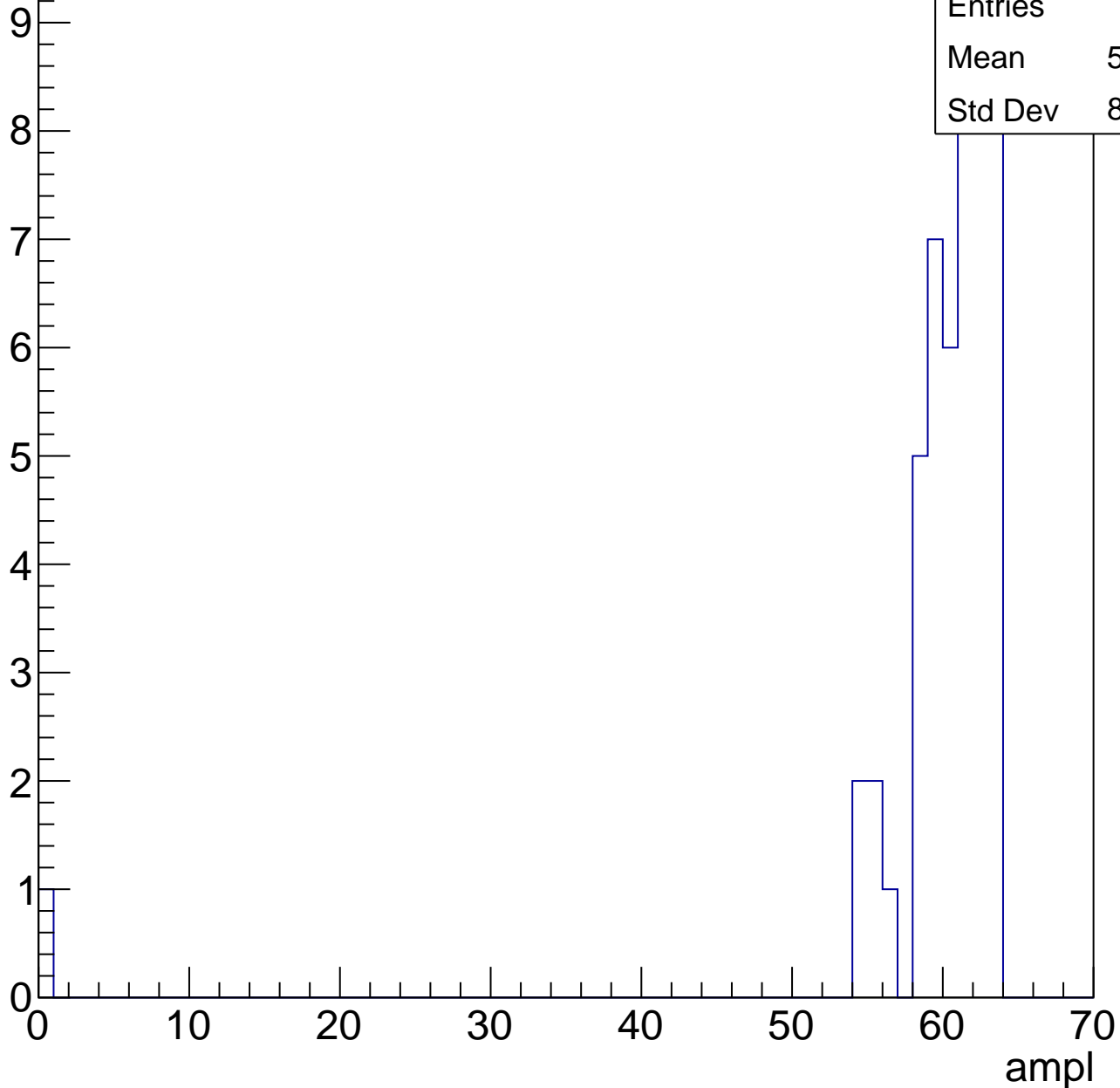
Entries	55
Mean	55.45
Std Dev	3.026



# B1L101S, U22-ch89, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U22-ch89, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	2
Mean	62
Std Dev	0

ampl



# B1L101S, U22-ch89, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U22-ch90, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	74
Mean	29.97
Std Dev	6.254

**Gaus mean : 31.1215**

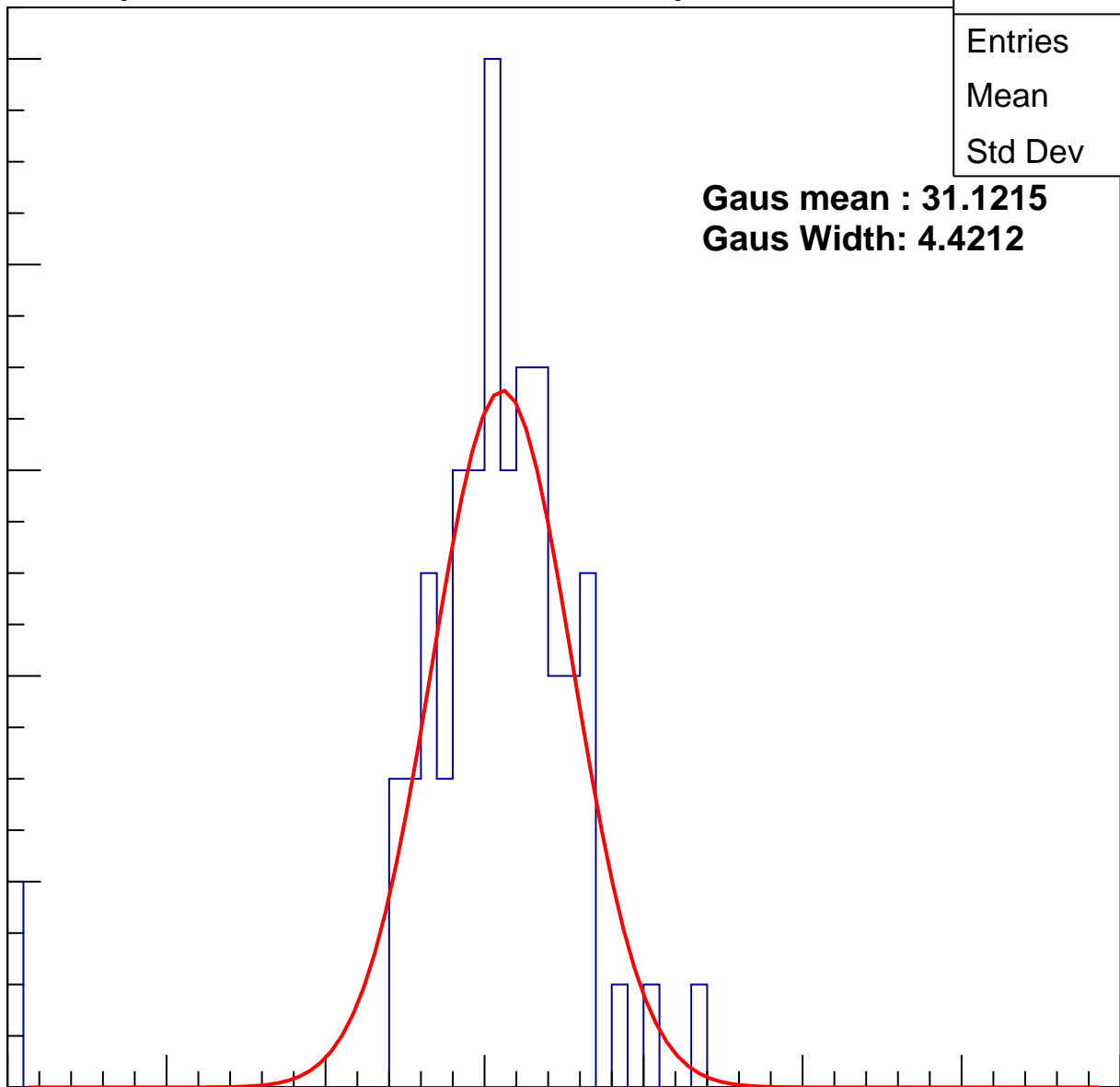
**Gaus Width: 4.4212**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U22-ch90, adc1

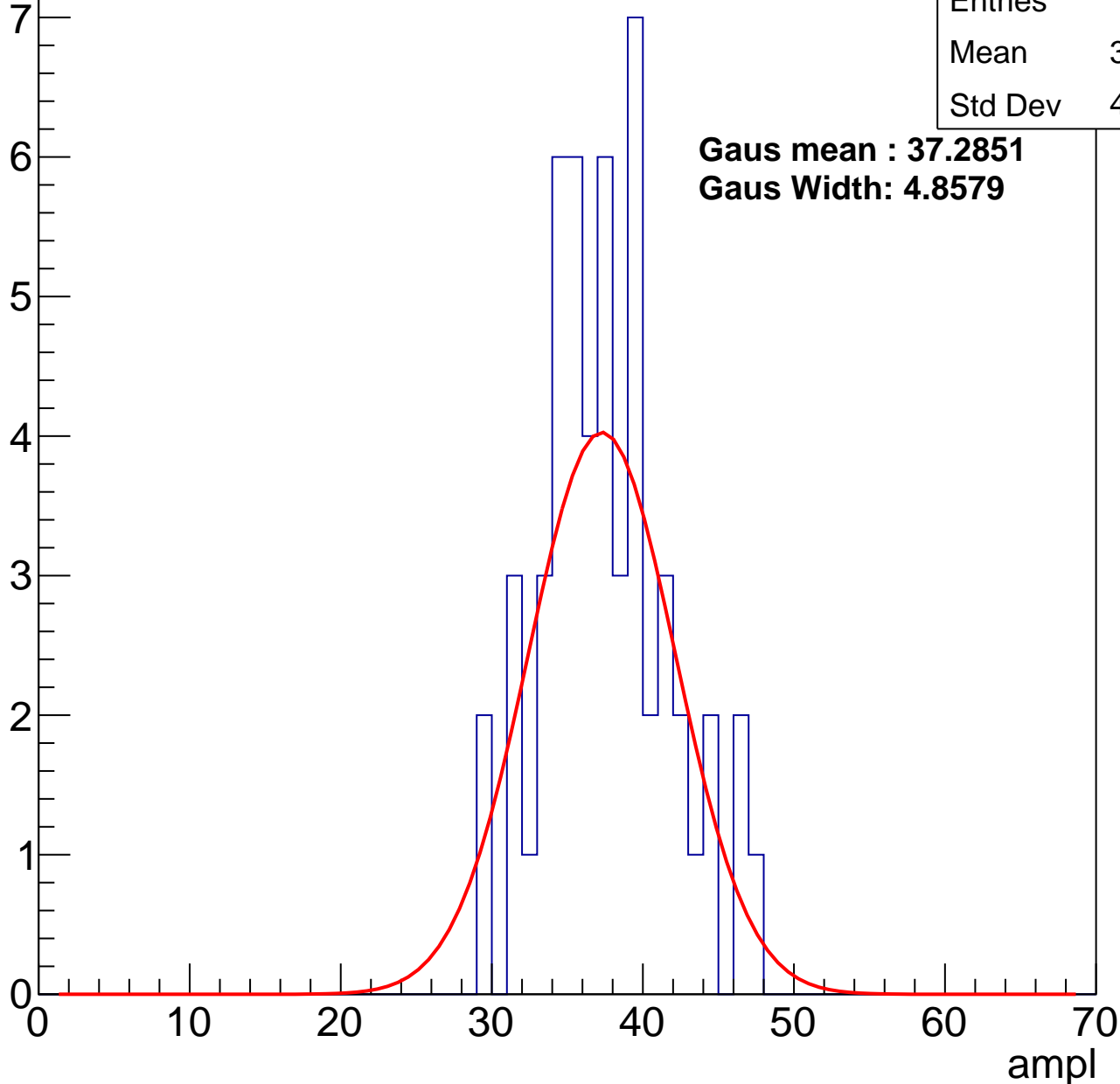
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	54
Mean	37.15
Std Dev	4.156

**Gaus mean : 37.2851**

**Gaus Width: 4.8579**



# B1L101S, U22-ch90, adc2

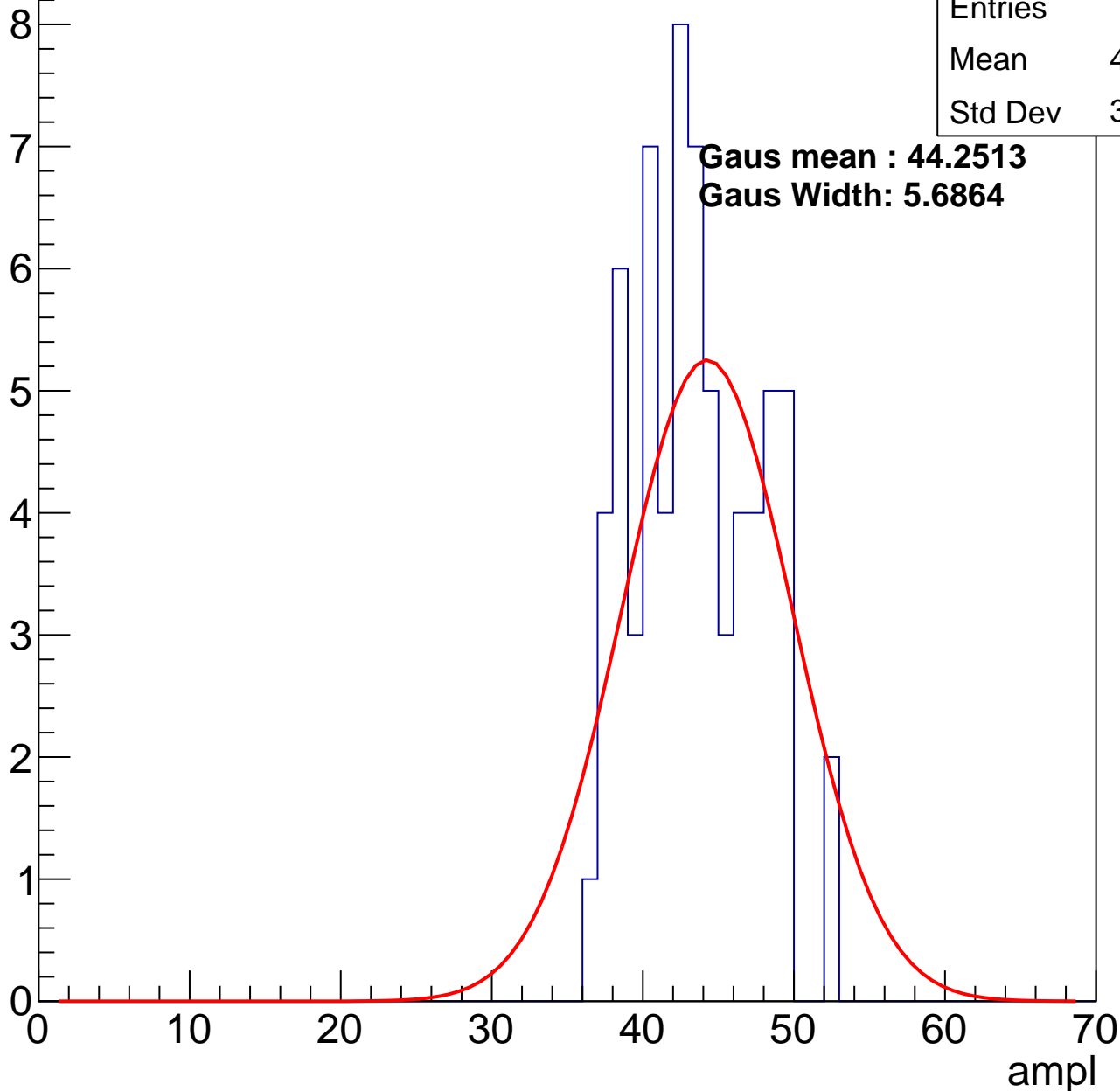
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	43.03
Std Dev	3.952

**Gaus mean : 44.2513**

**Gaus Width: 5.6864**

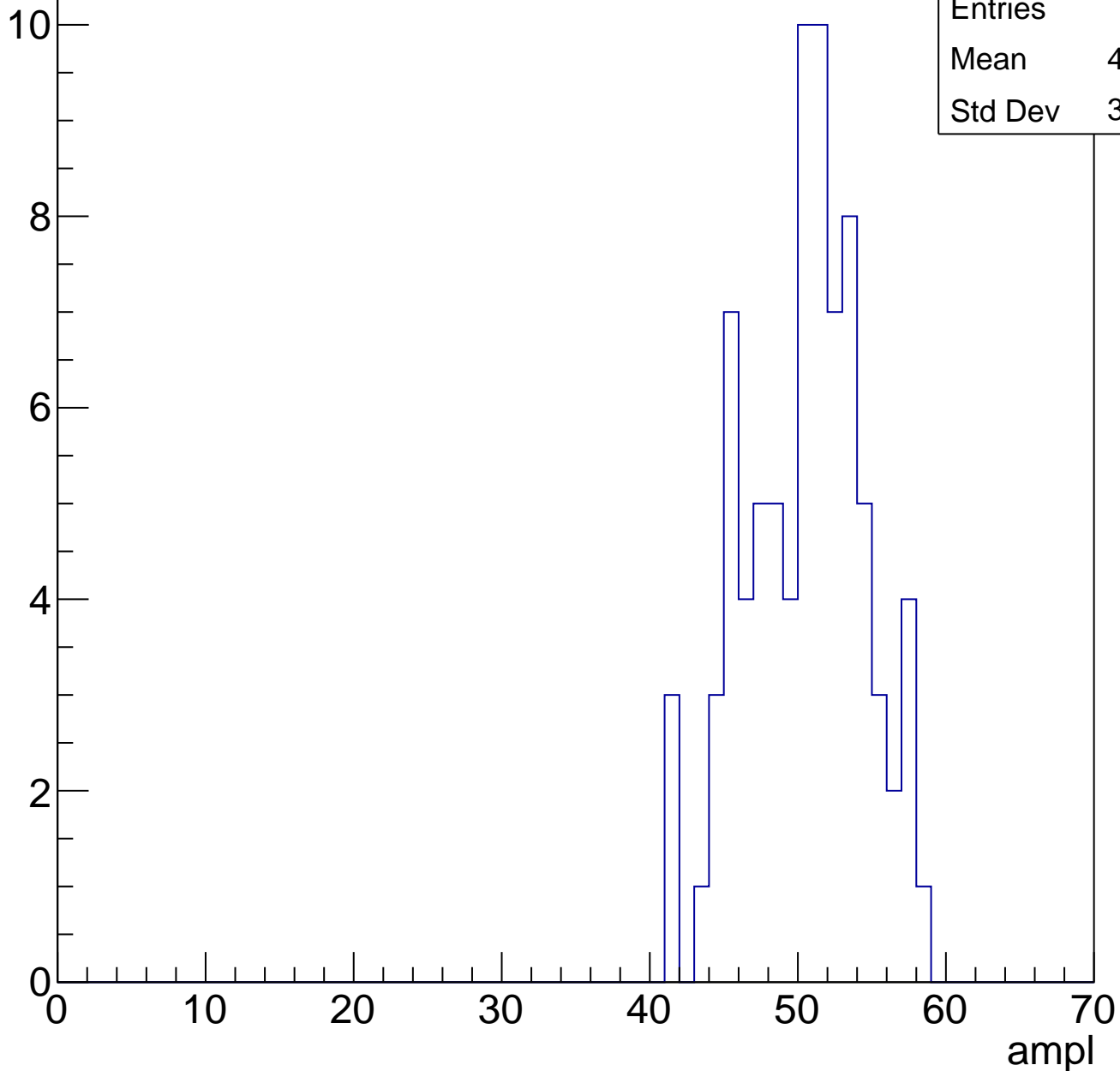


# B1L101S, U22-ch90, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	82
Mean	49.99
Std Dev	3.989

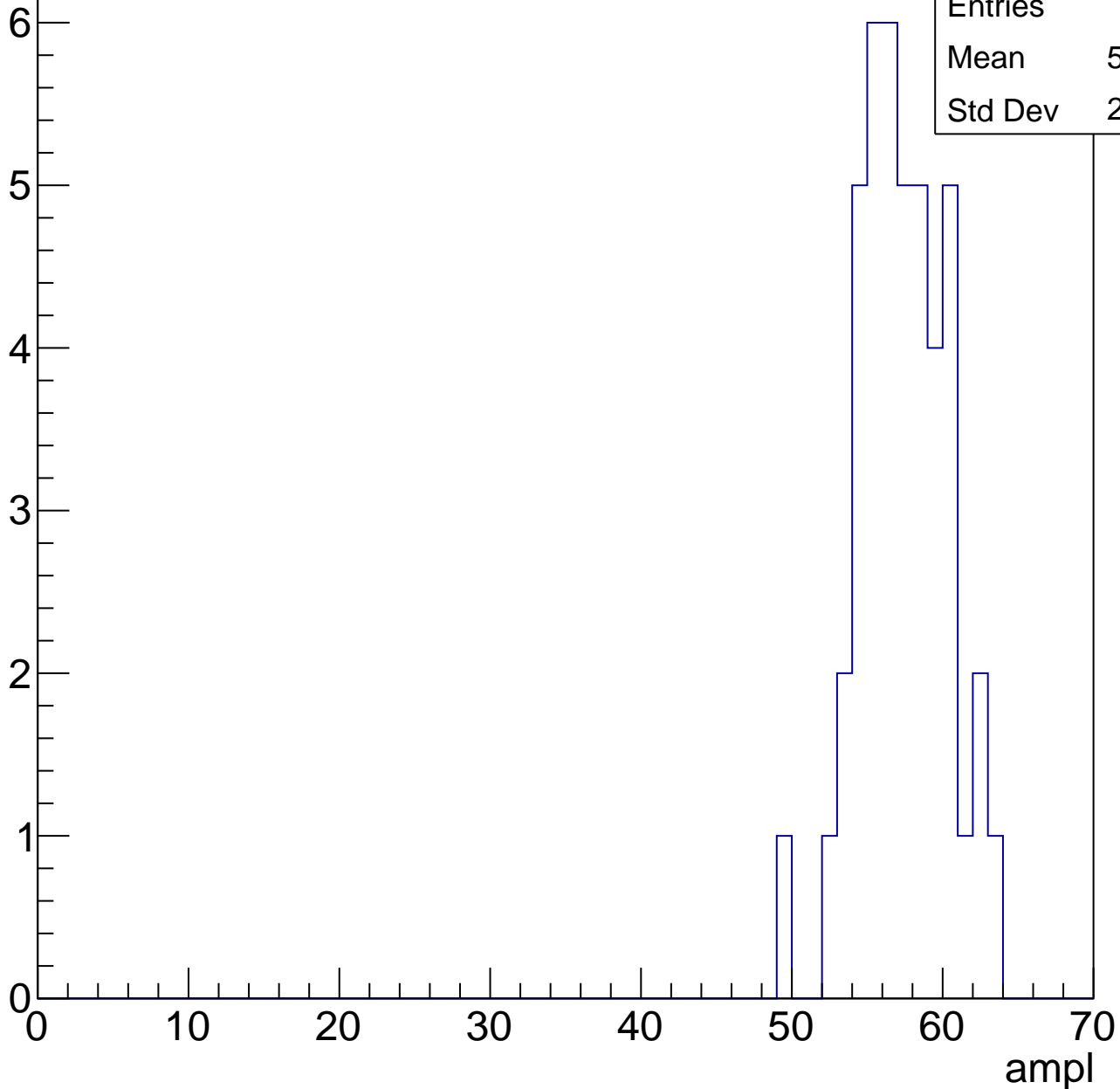


# B1L101S, U22-ch90, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	44
Mean	56.86
Std Dev	2.873

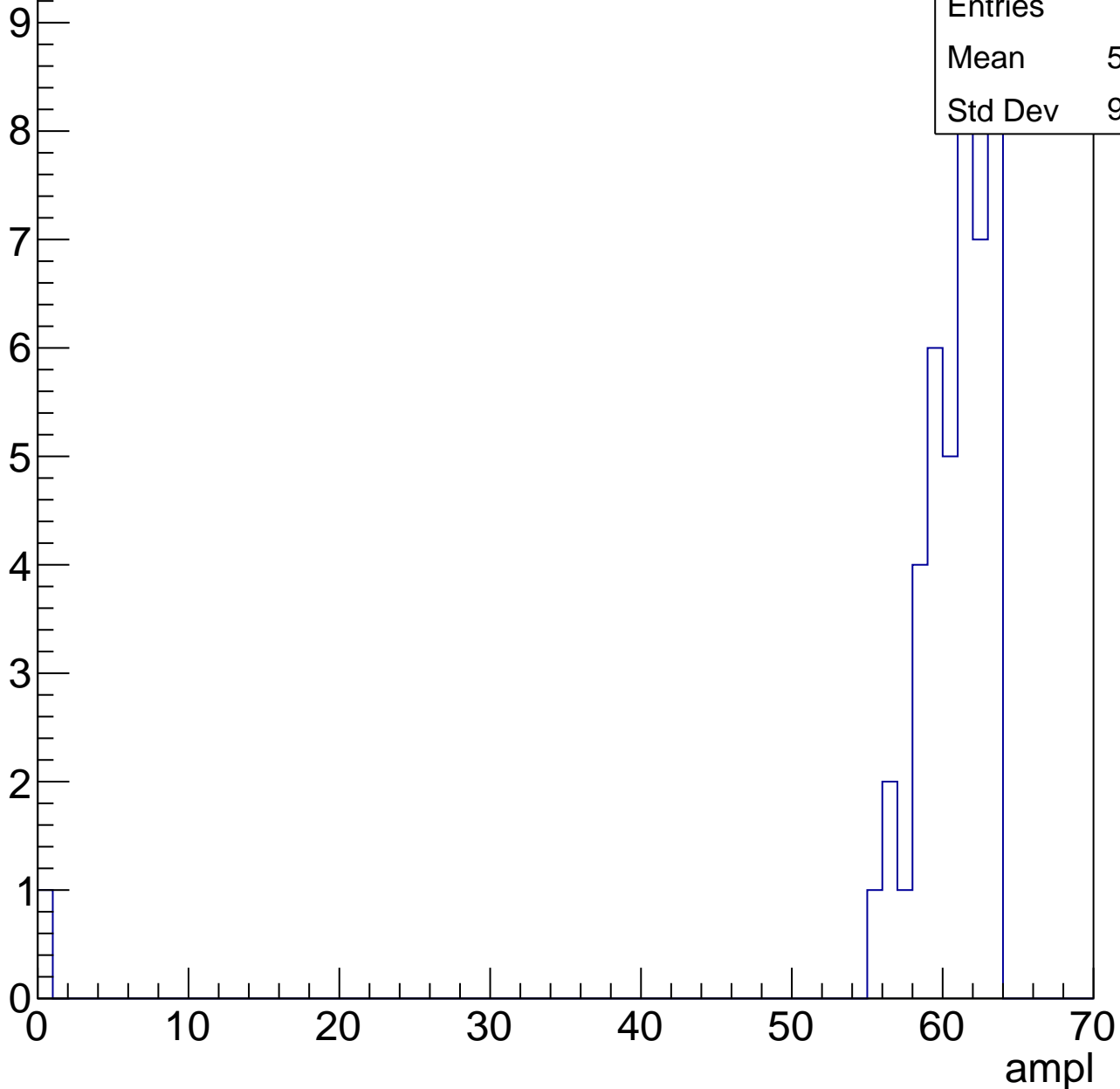


# B1L101S, U22-ch90, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	44
Mean	59.07
Std Dev	9.253



# B1L101S, U22-ch90, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U22-ch90, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U22-ch91, adc0

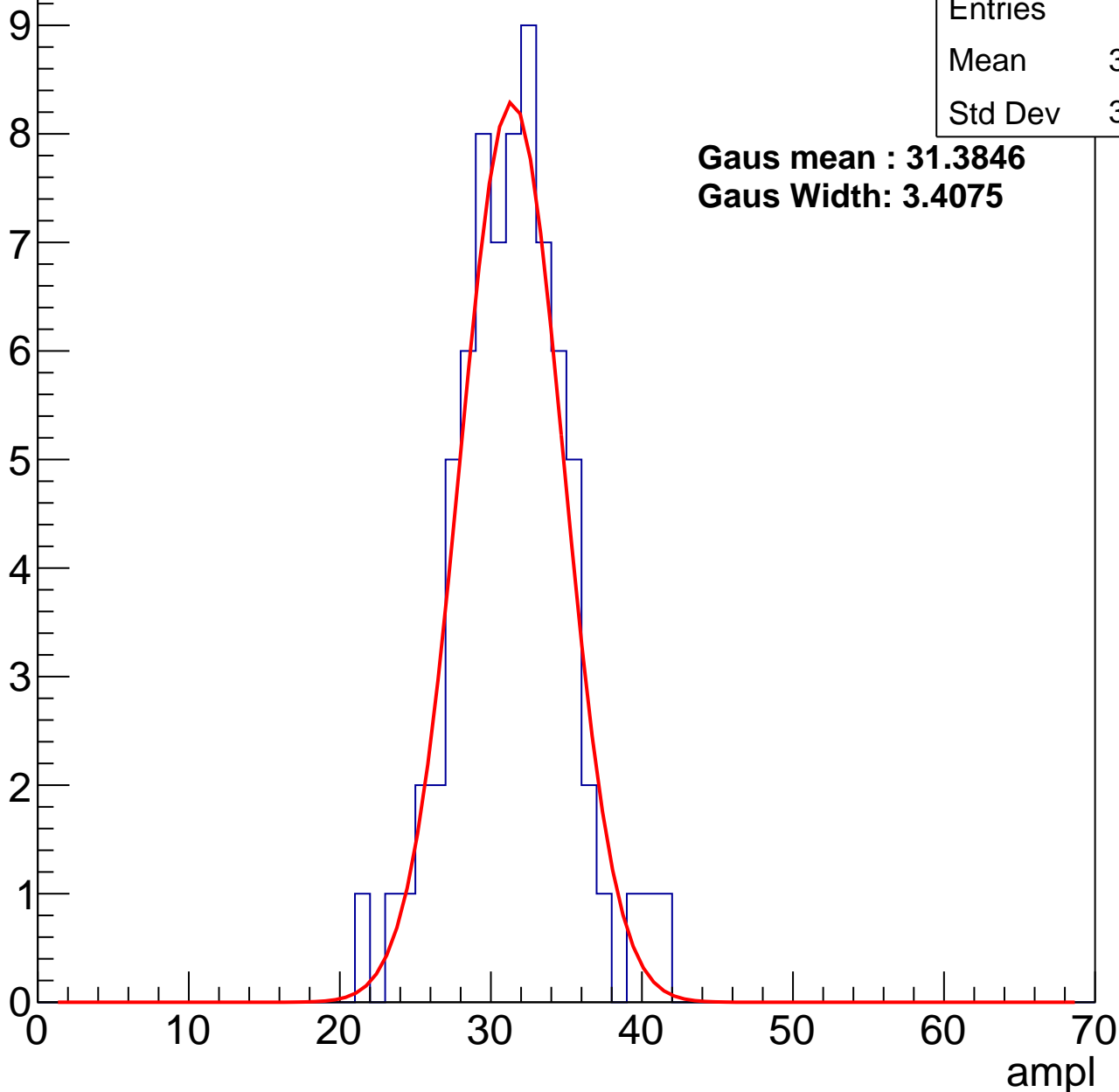
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	74
Mean	30.95
Std Dev	3.694

**Gaus mean : 31.3846**

**Gaus Width: 3.4075**



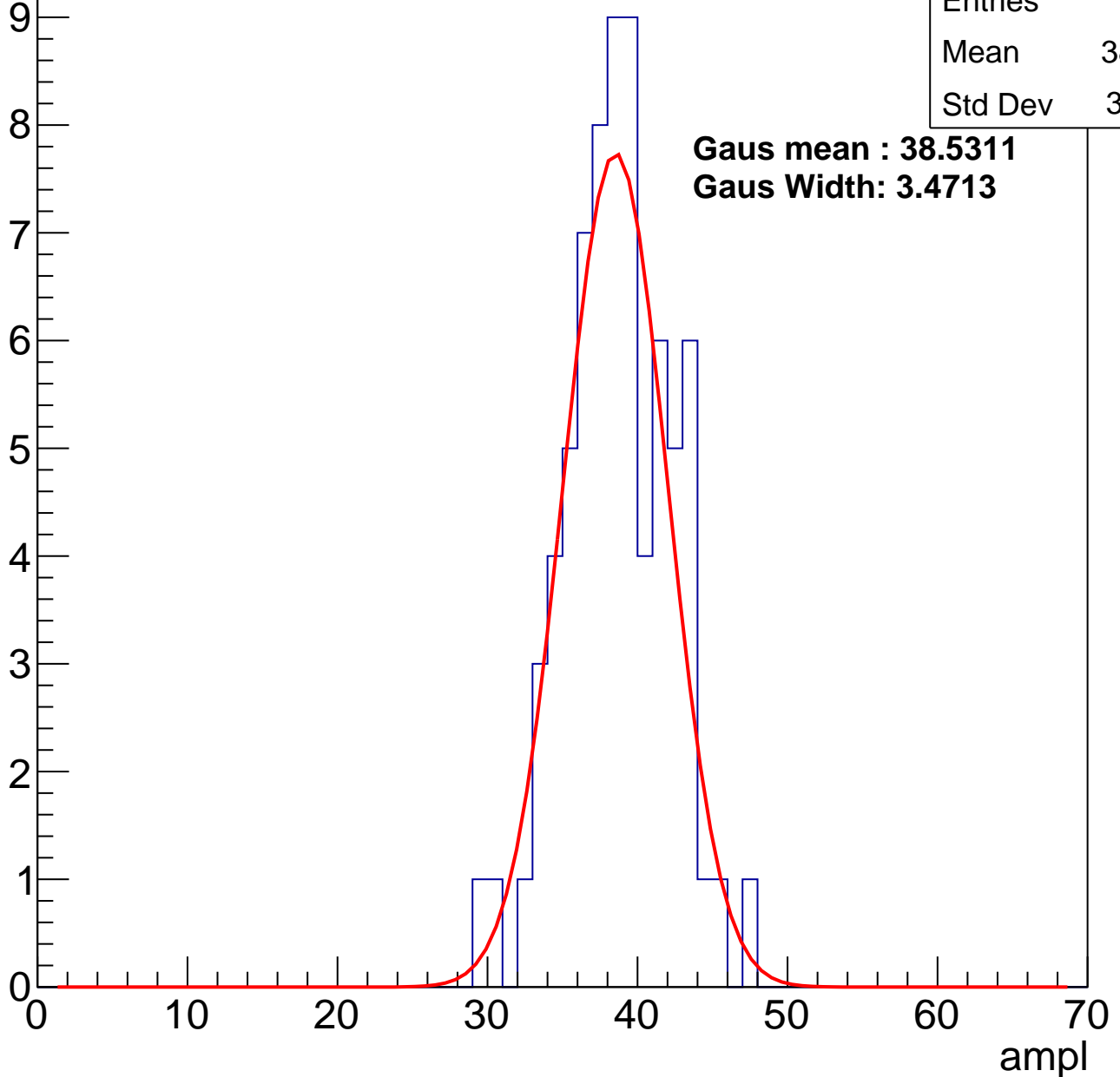
# B1L101S, U22-ch91, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	72
Mean	38.22
Std Dev	3.481

**Gaus mean : 38.5311**  
**Gaus Width: 3.4713**



# B1L101S, U22-ch91, adc2

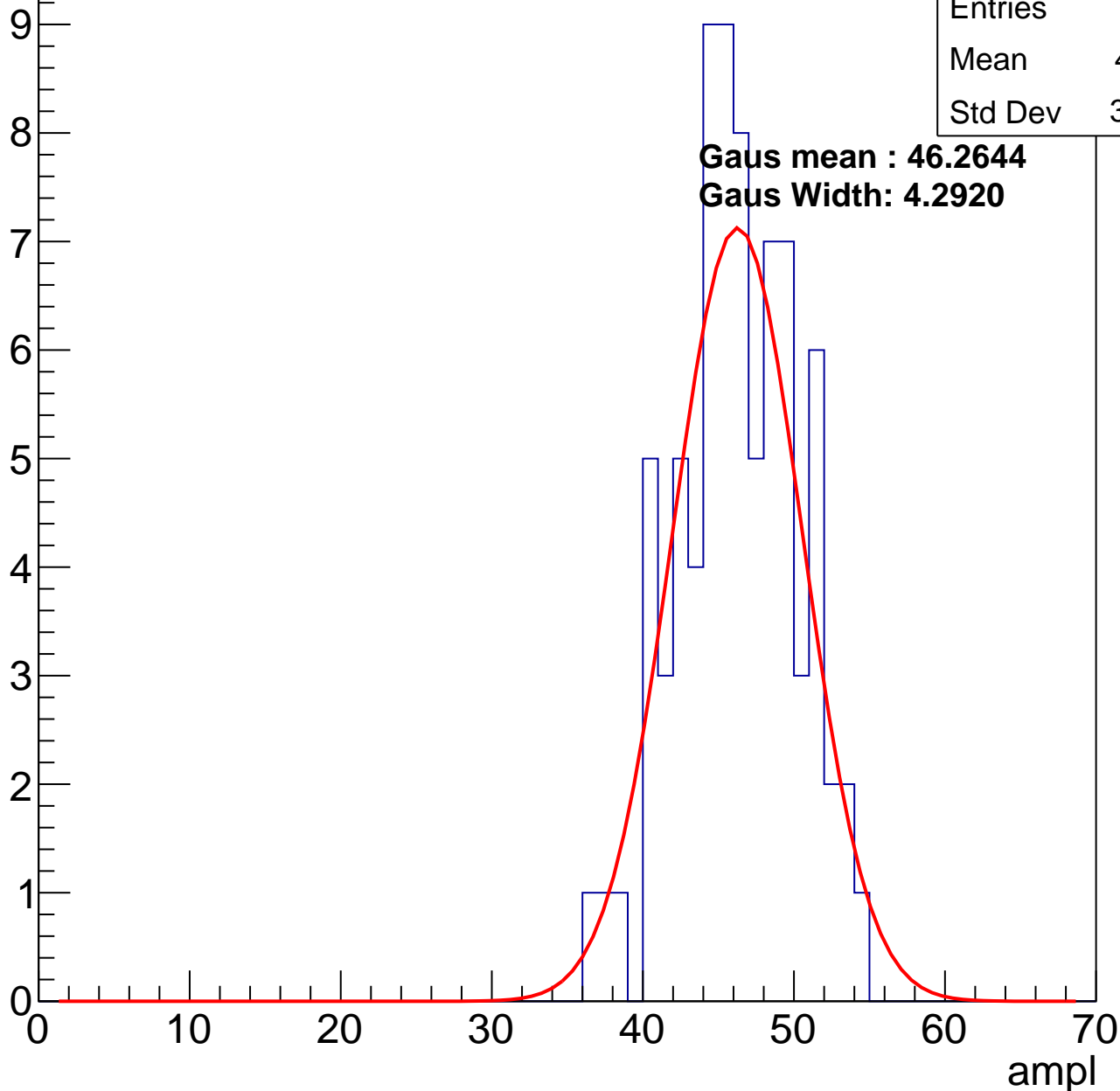
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	79
Mean	45.81
Std Dev	3.875

**Gaus mean : 46.2644**

**Gaus Width: 4.2920**

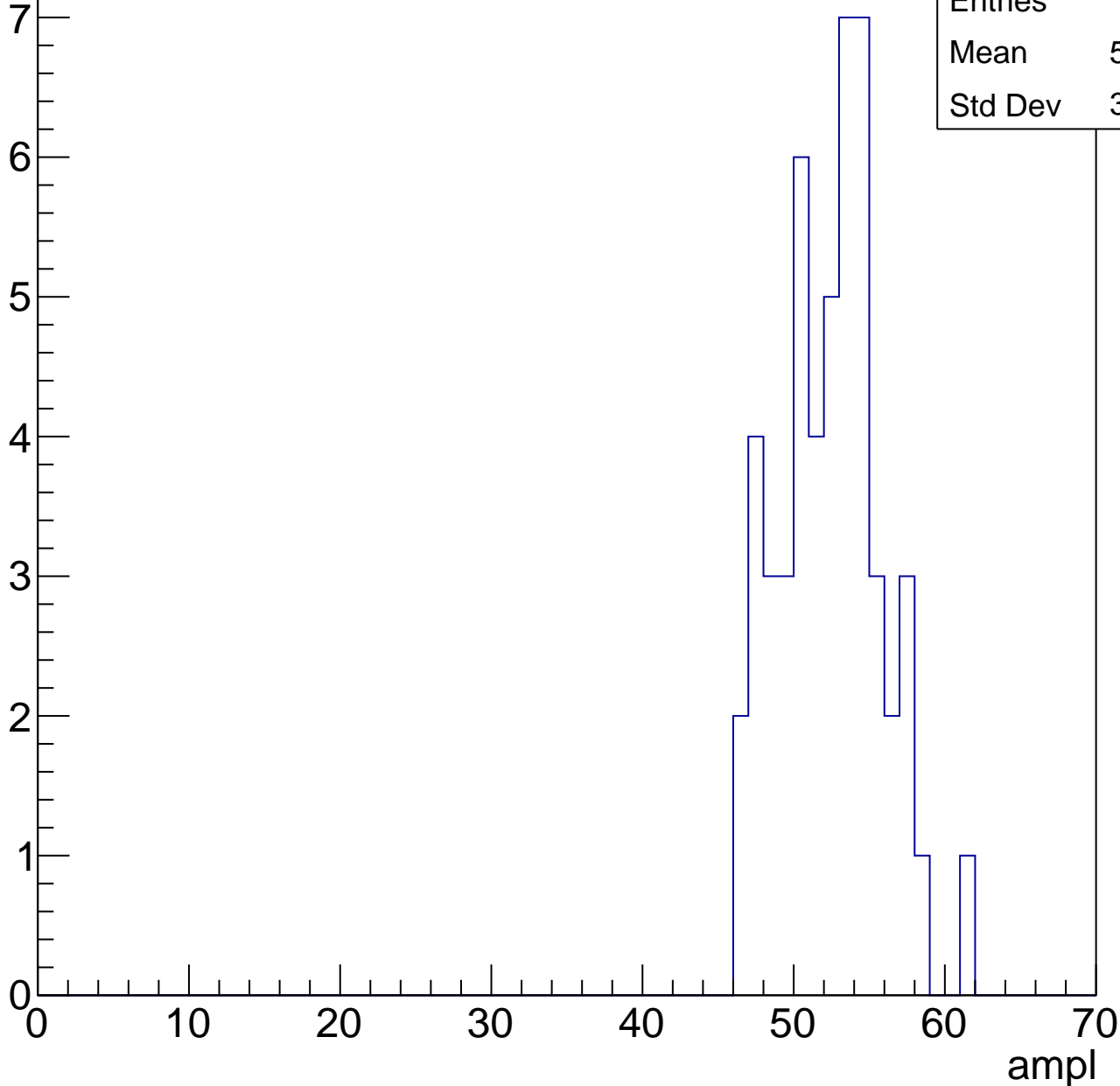


# B1L101S, U22-ch91, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	51
Mean	51.98
Std Dev	3.317

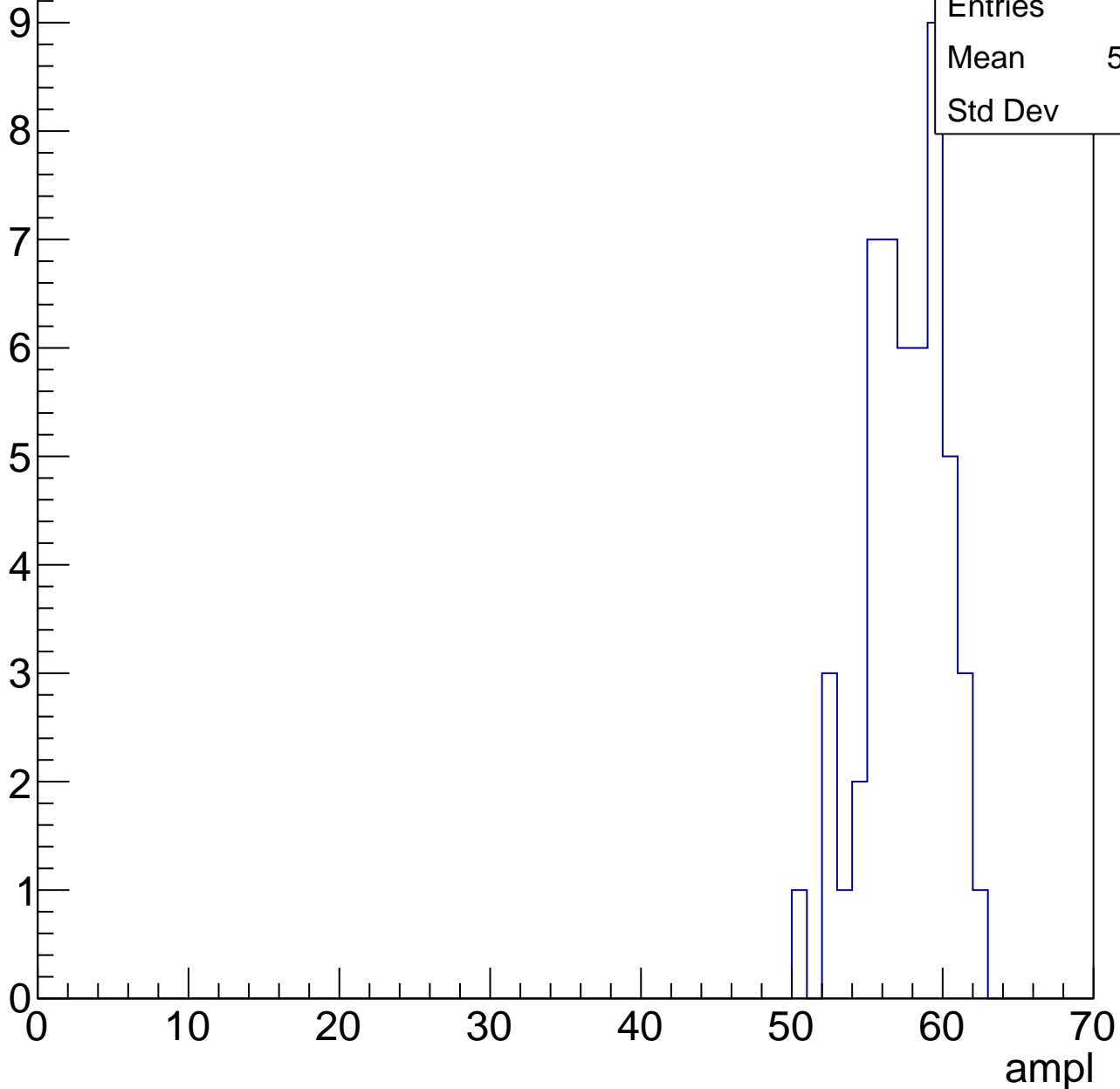


# B1L101S, U22-ch91, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	51
Mean	57.06
Std Dev	2.63

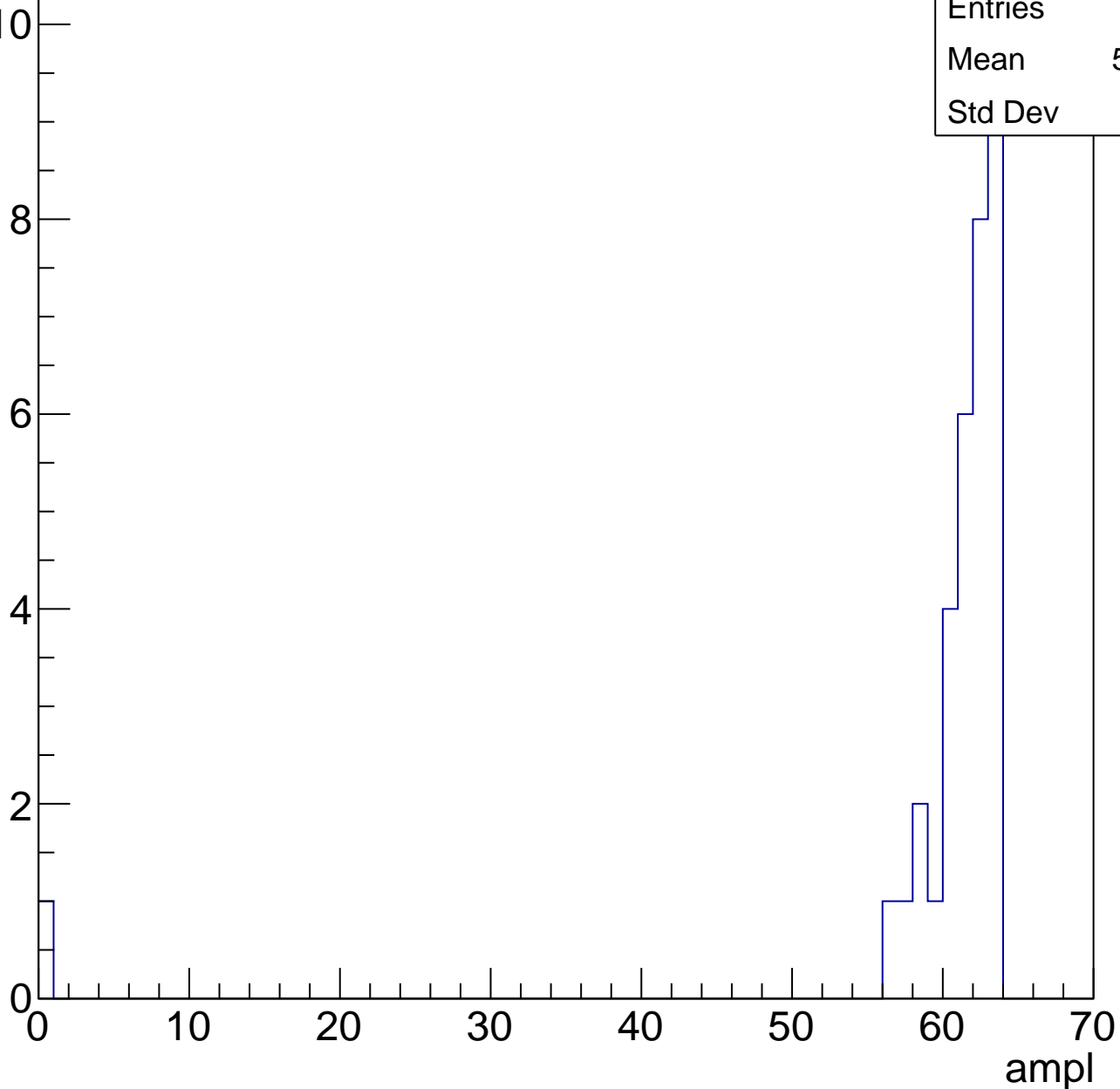


# B1L101S, U22-ch91, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

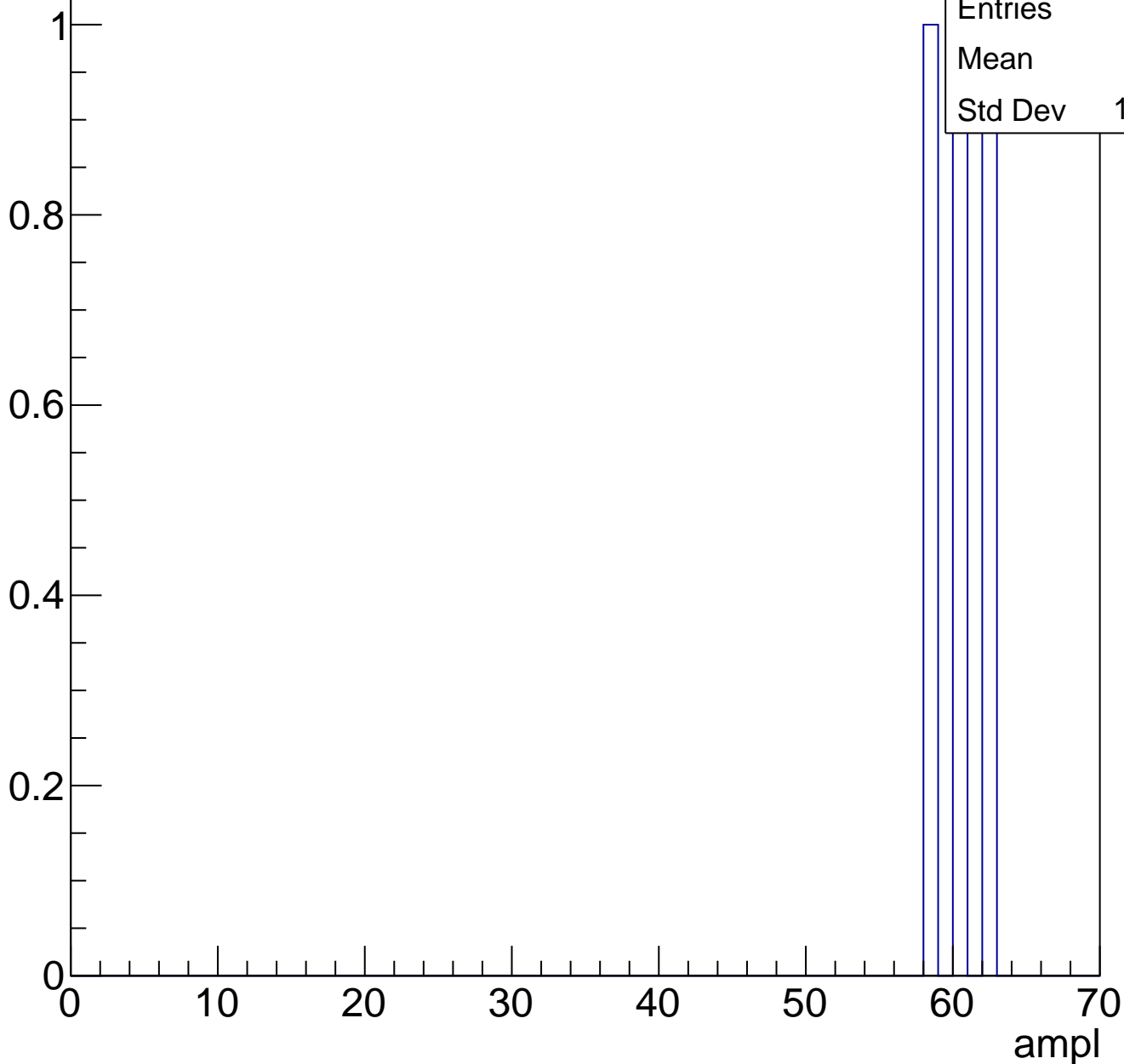
Entries	34
Mean	59.41
Std Dev	10.5



# B1L101S, U22-ch91, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U22-ch91, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	2
Mean	9.5
Std Dev	9.5

# B1L101S, U22-ch92, adc0

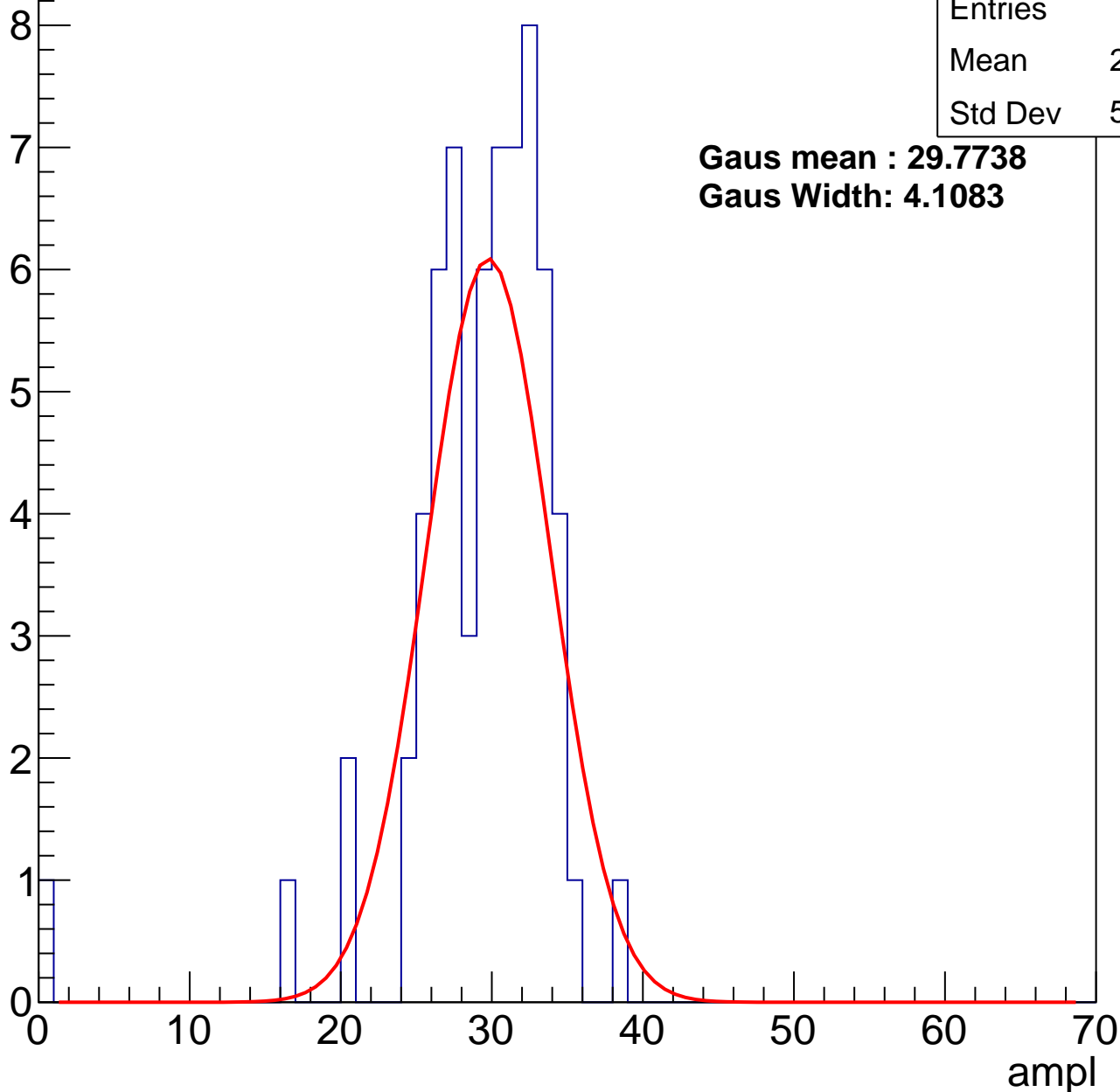
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	66
Mean	28.74
Std Dev	5.203

**Gaus mean : 29.7738**

**Gaus Width: 4.1083**



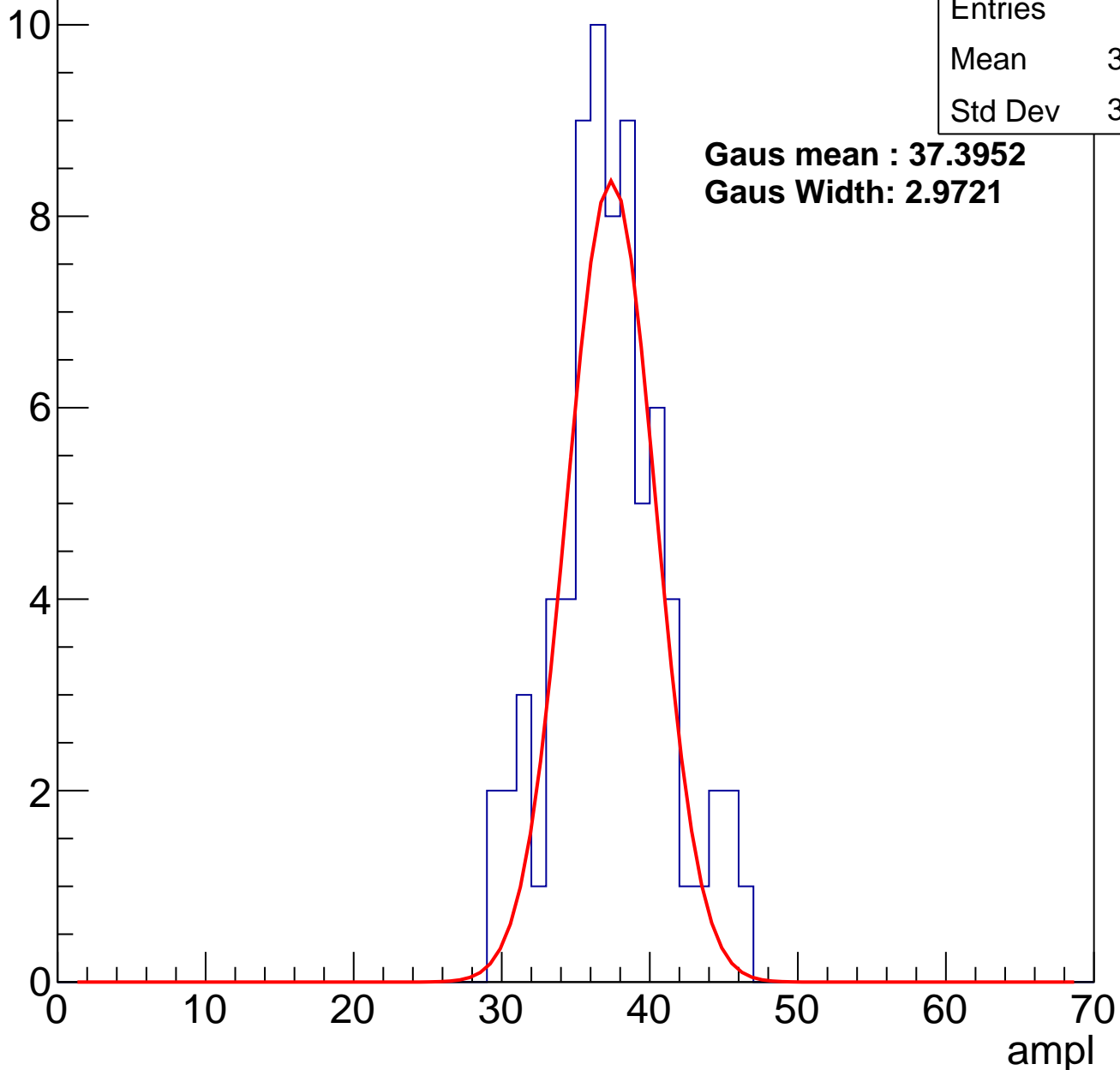
# B1L101S, U22-ch92, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	74
Mean	36.92
Std Dev	3.712

**Gaus mean : 37.3952**  
**Gaus Width: 2.9721**

Entry



# B1L101S, U22-ch92, adc2

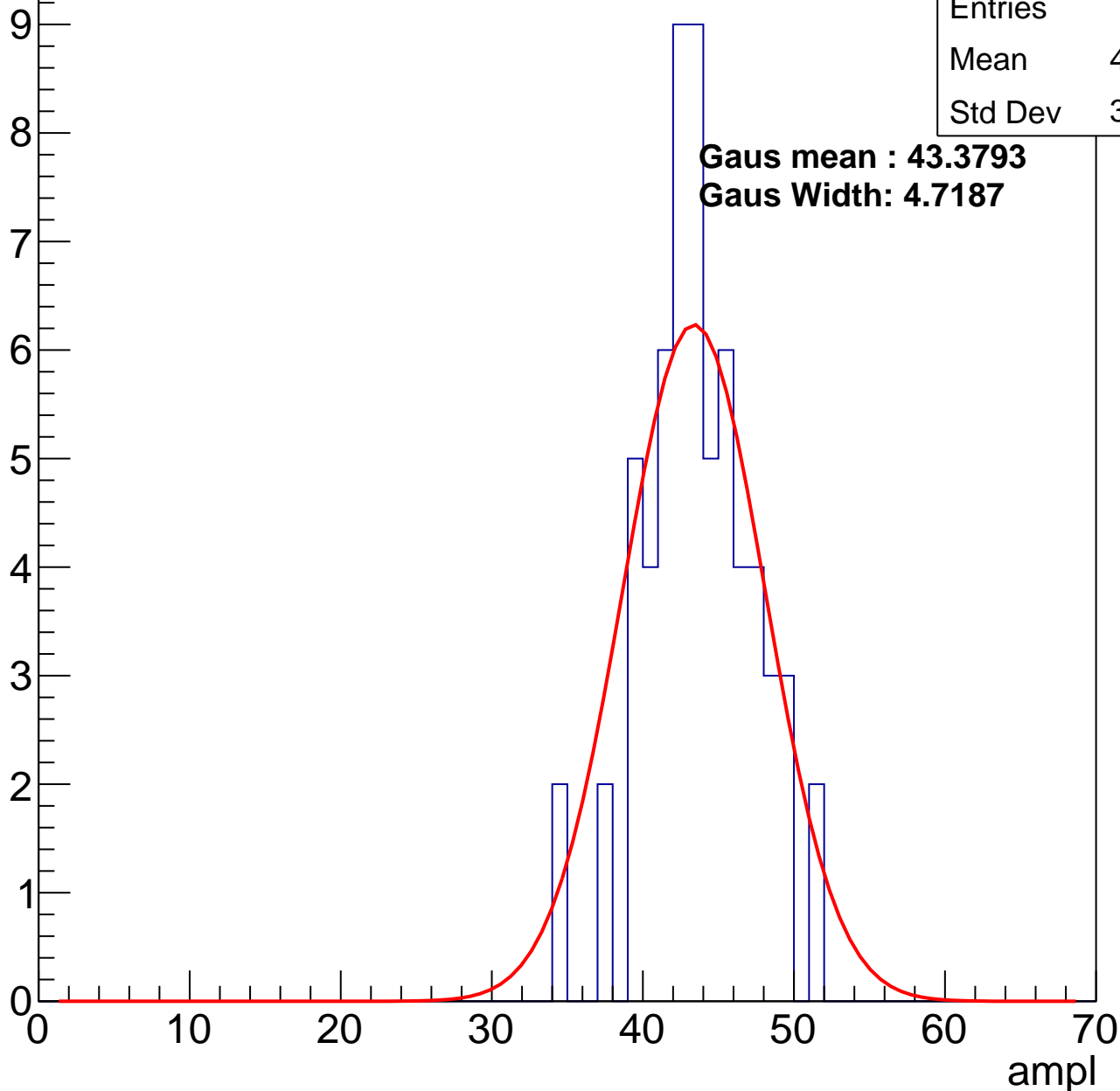
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	43.17
Std Dev	3.582

**Gaus mean : 43.3793**

**Gaus Width: 4.7187**

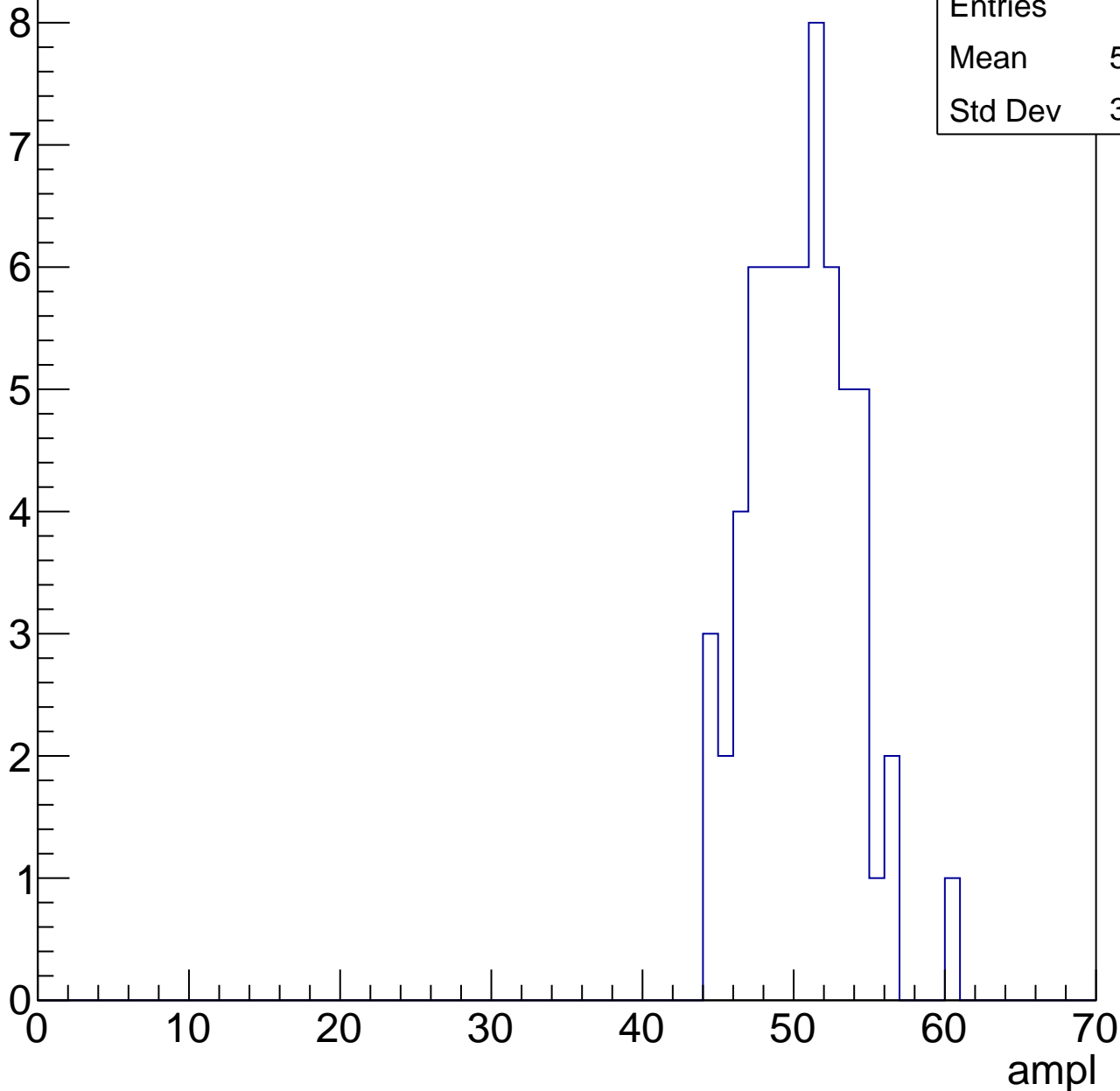


# B1L101S, U22-ch92, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	50.03
Std Dev	3.289

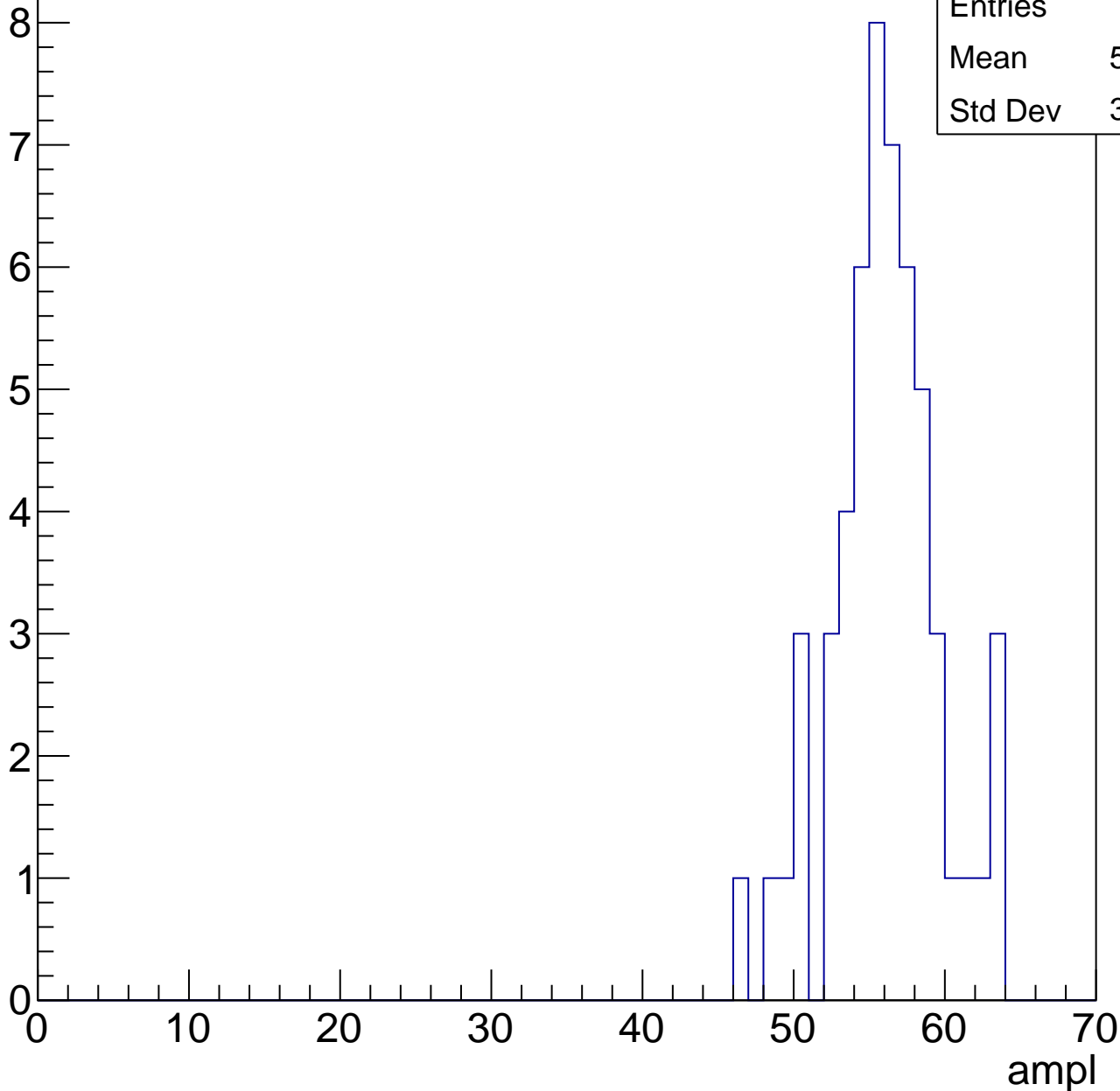


# B1L101S, U22-ch92, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	54
Mean	55.52
Std Dev	3.604

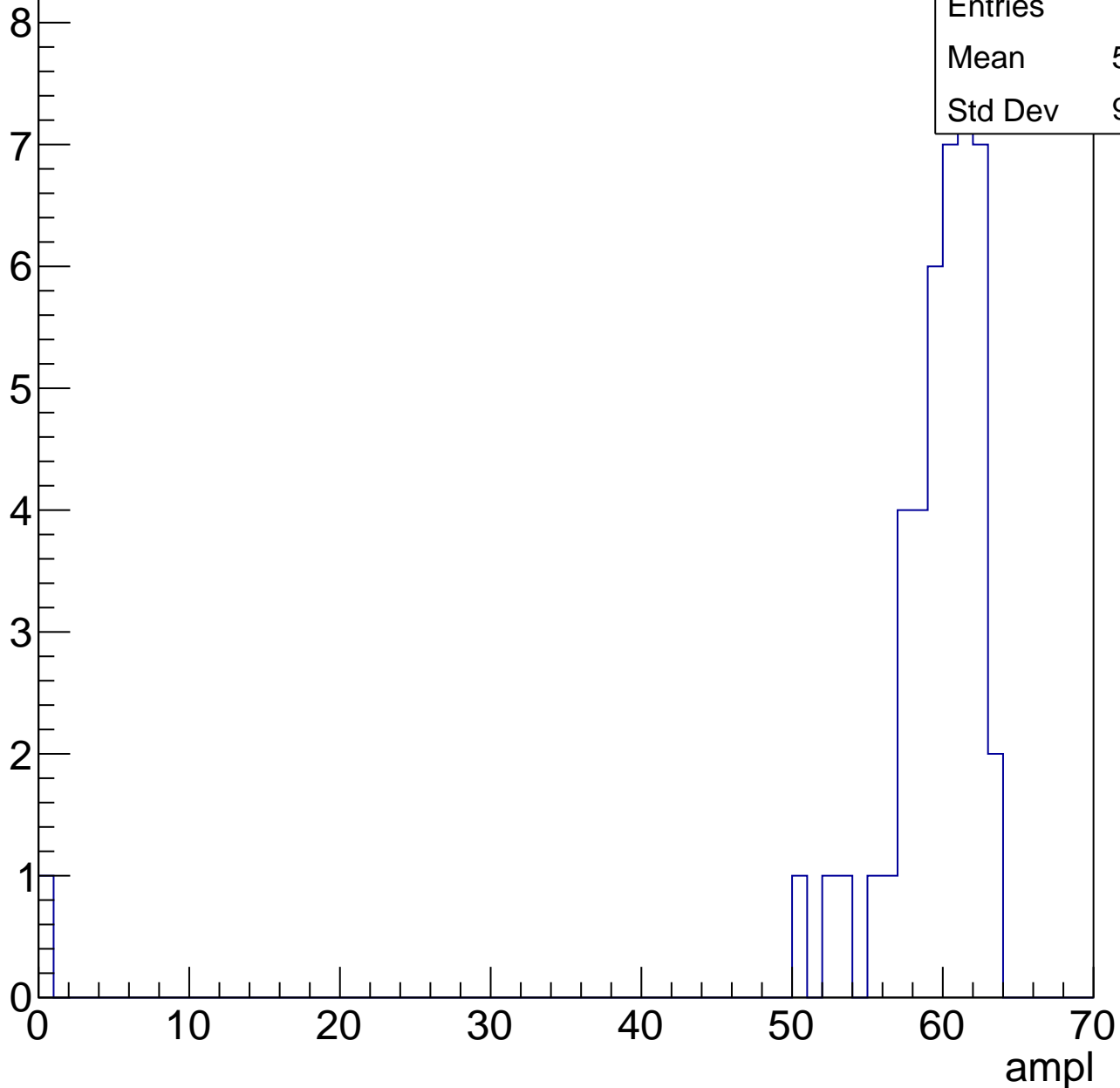


# B1L101S, U22-ch92, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

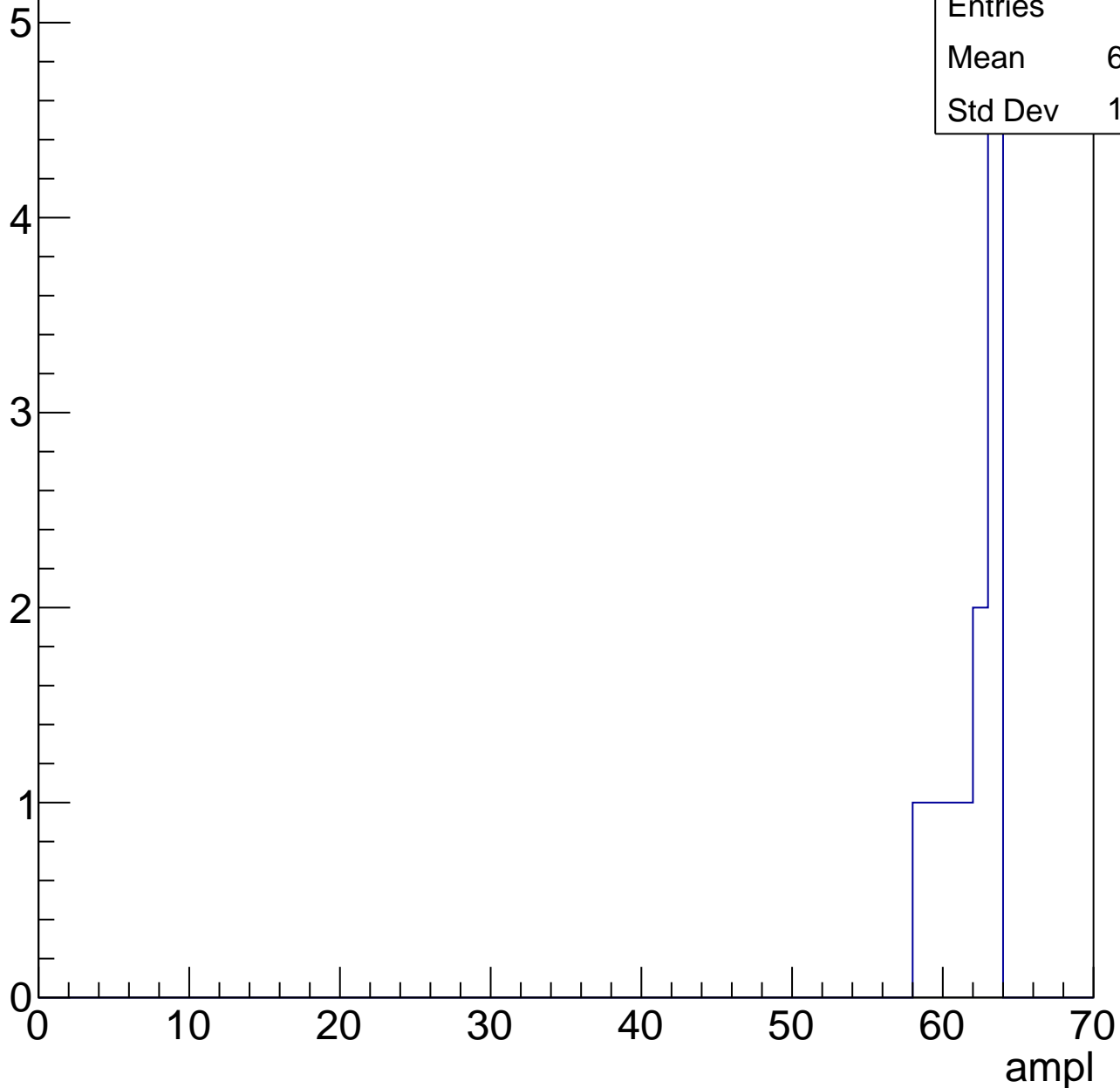
Entries	44
Mean	57.91
Std Dev	9.261



# B1L101S, U22-ch92, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	11
Mean	61.55
Std Dev	1.725



# B1L101S, U22-ch92, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U22-ch93, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	80
Mean	30.3
Std Dev	6.044

**Gaus mean : 30.8530**

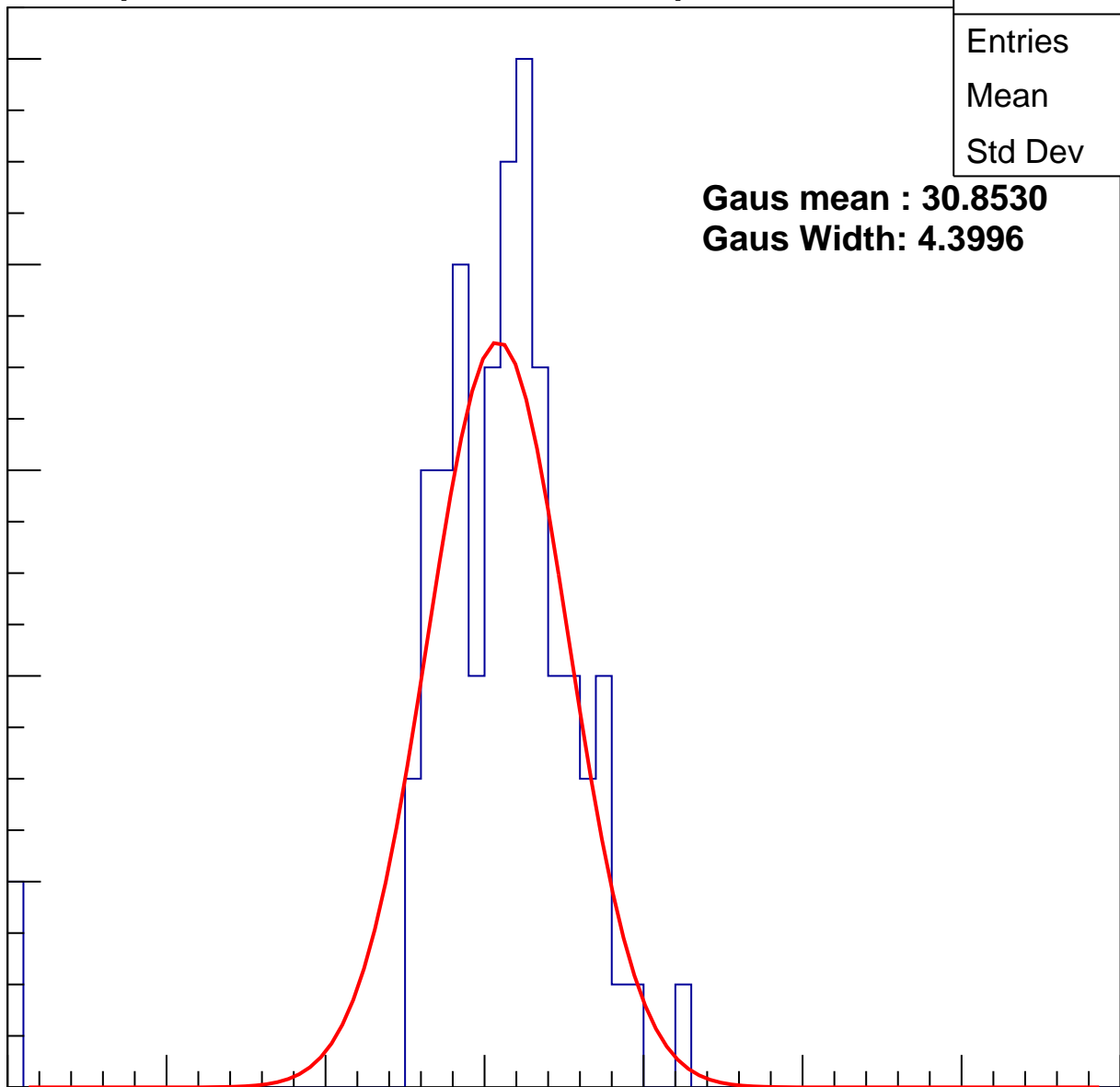
**Gaus Width: 4.3996**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U22-ch93, adc1

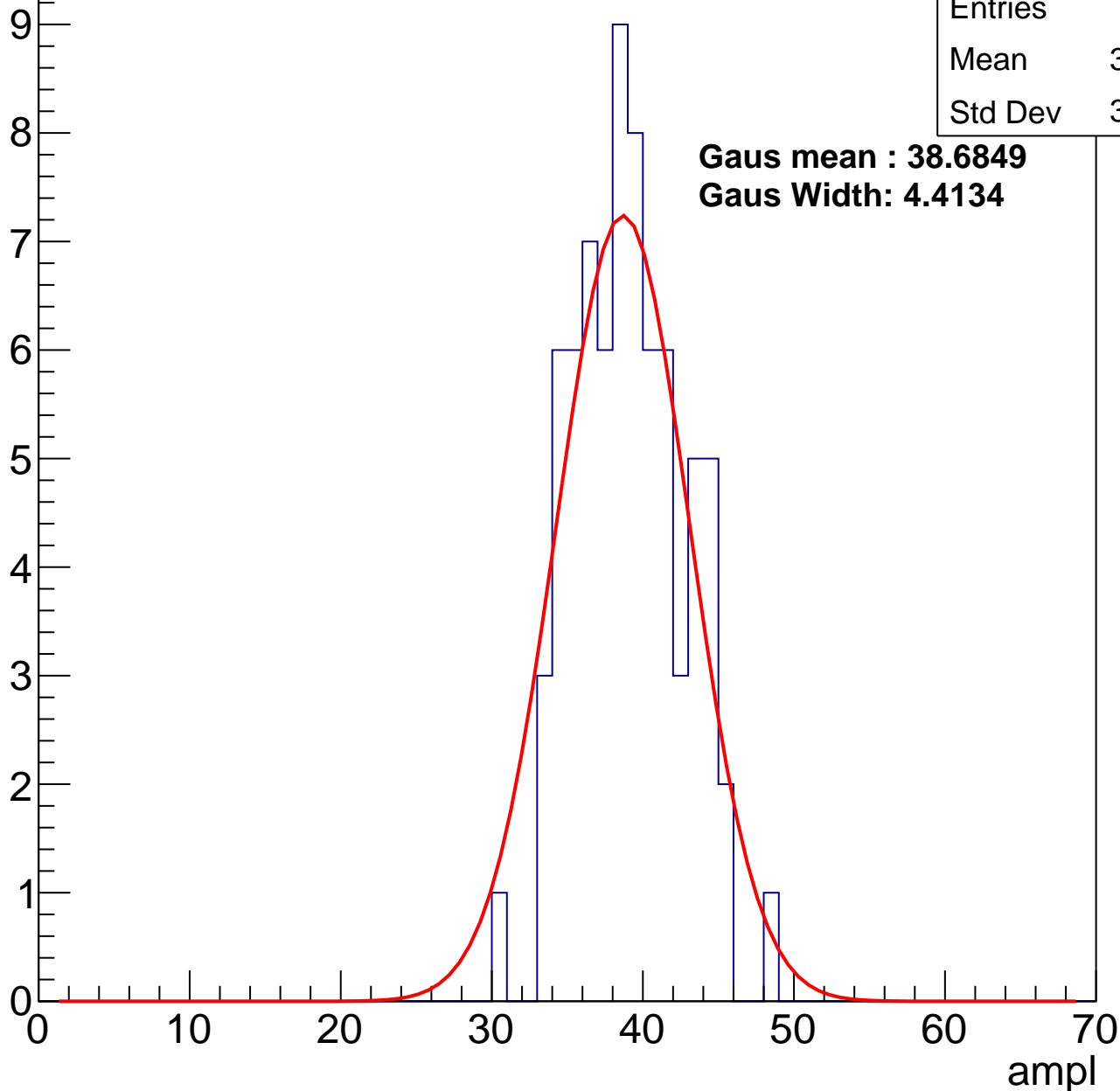
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	74
Mean	38.59
Std Dev	3.552

**Gaus mean : 38.6849**

**Gaus Width: 4.4134**



# B1L101S, U22-ch93, adc2

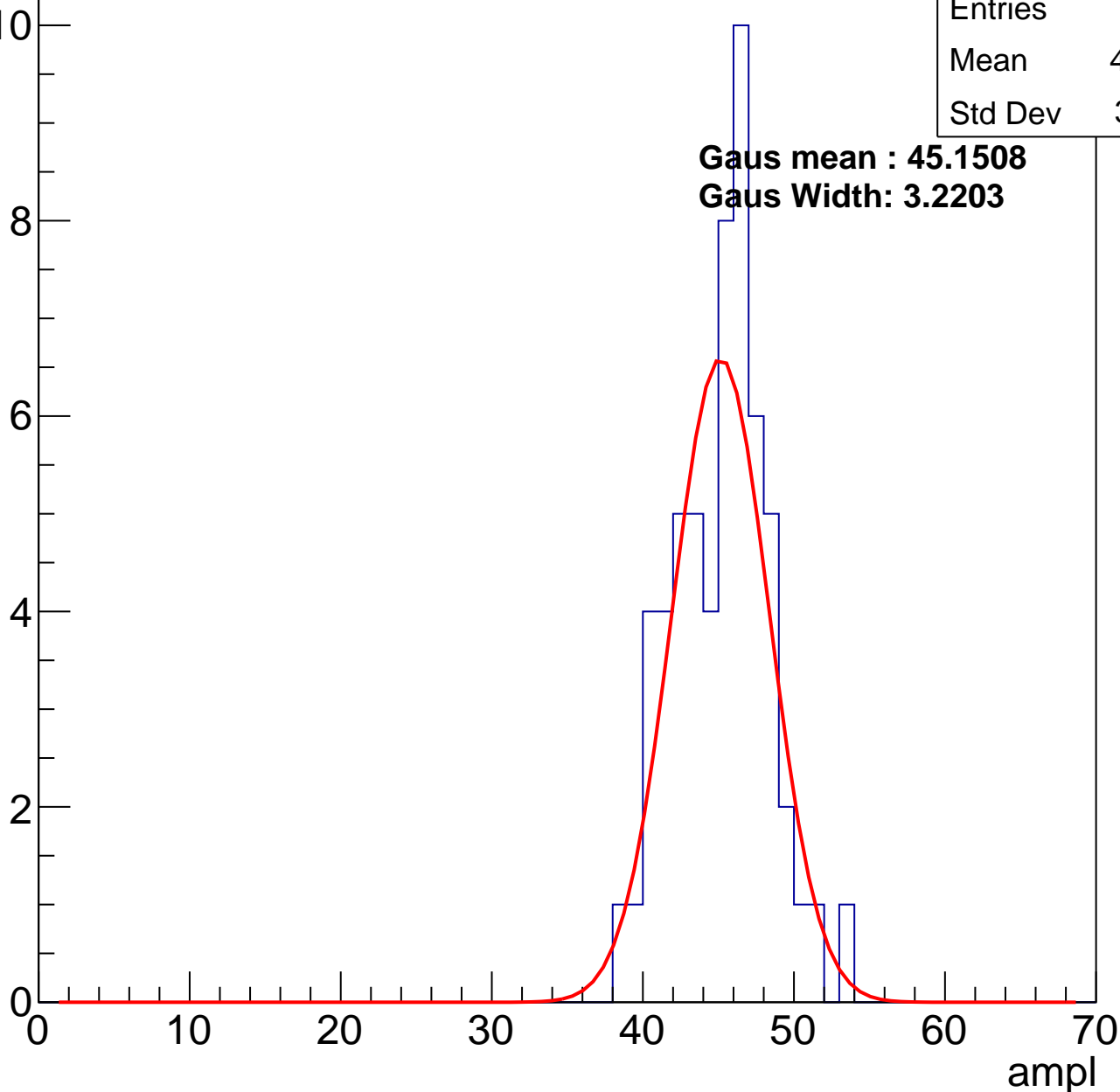
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	58
Mean	44.76
Std Dev	3.081

**Gaus mean : 45.1508**

**Gaus Width: 3.2203**



# B1L101S, U22-ch93, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	86
Mean	52.33
Std Dev	3.476

Entry

10

8

6

4

2

0

0

10

20

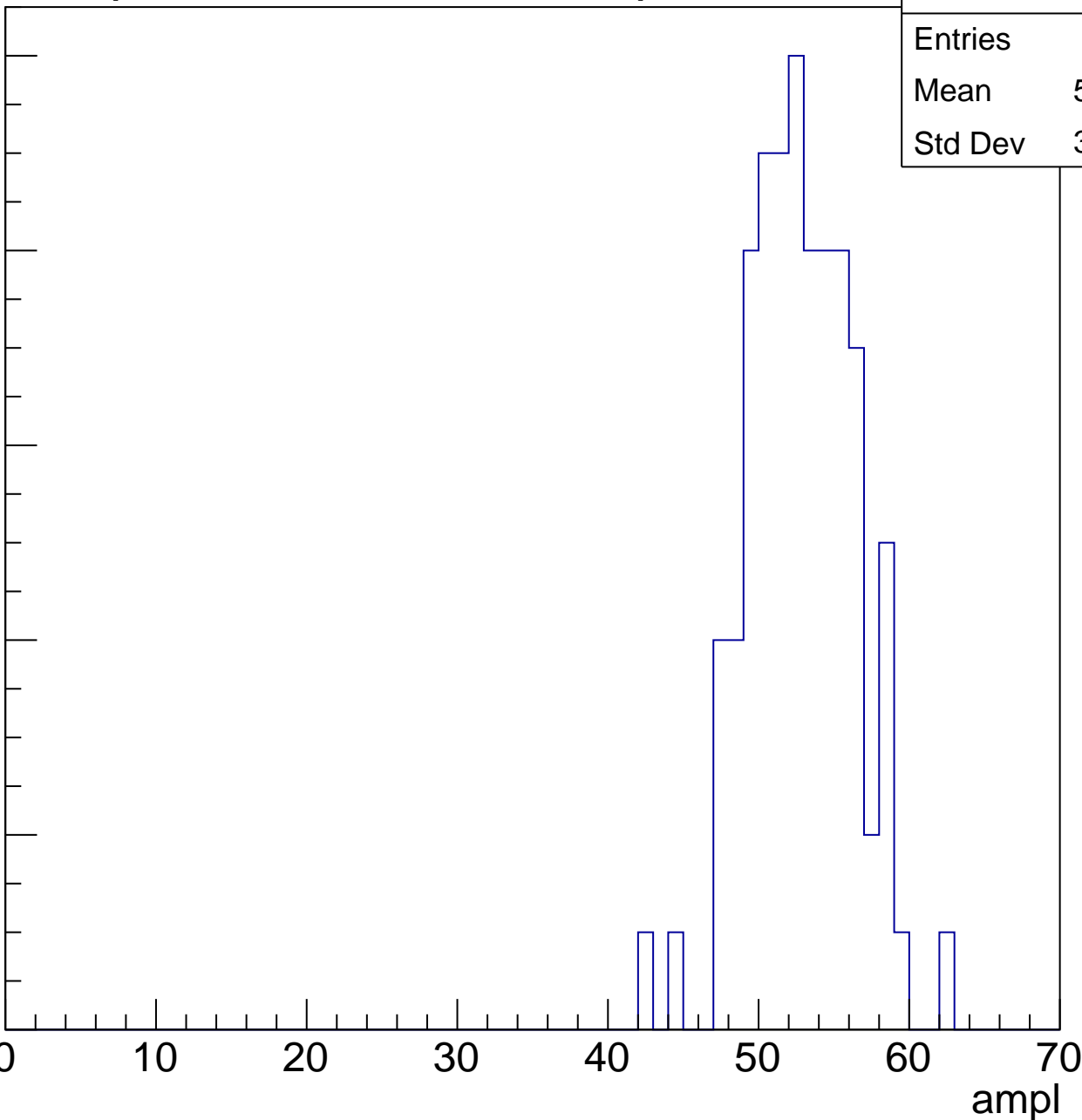
30

40

50

60

ampl

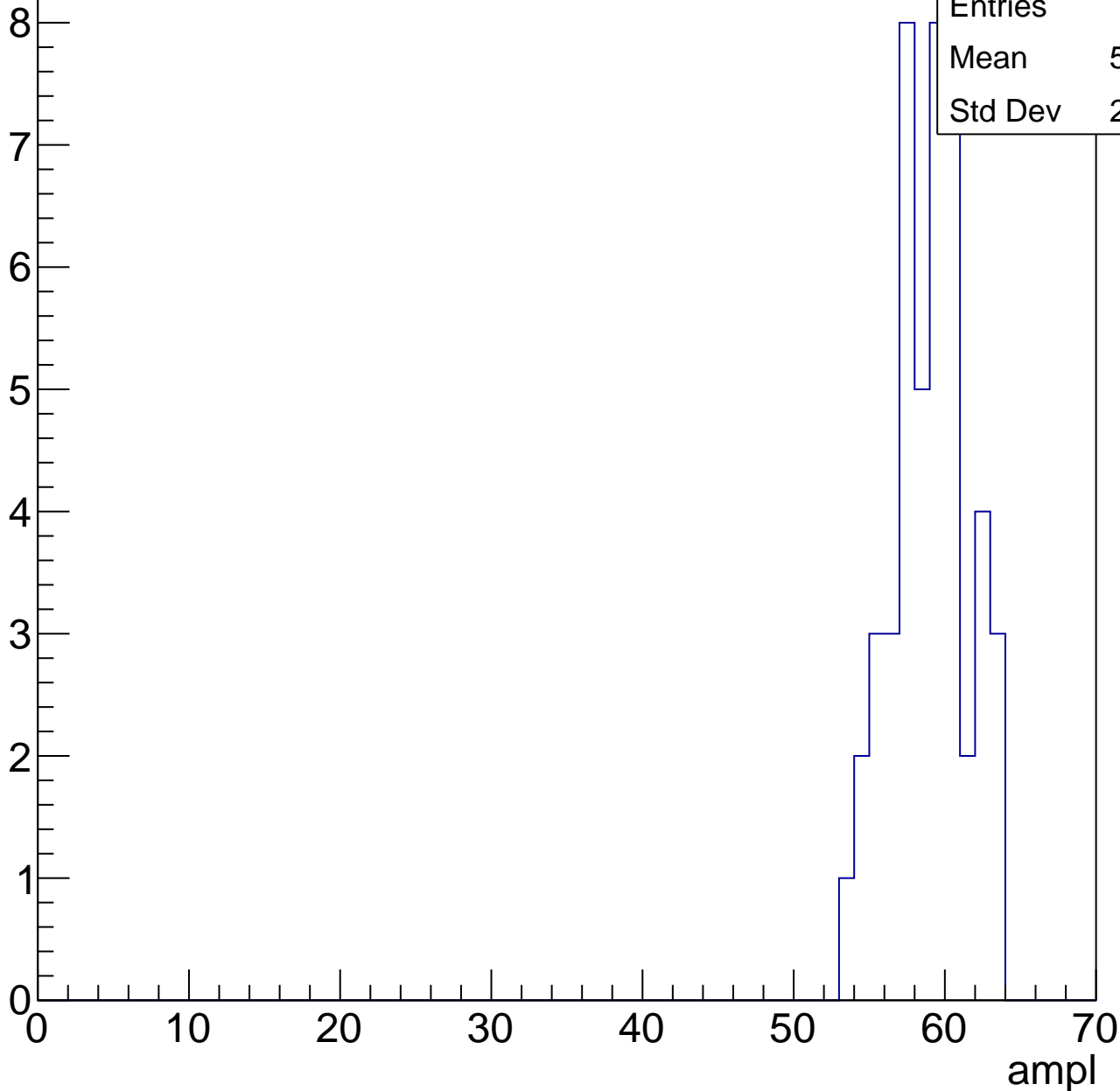


# B1L101S, U22-ch93, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

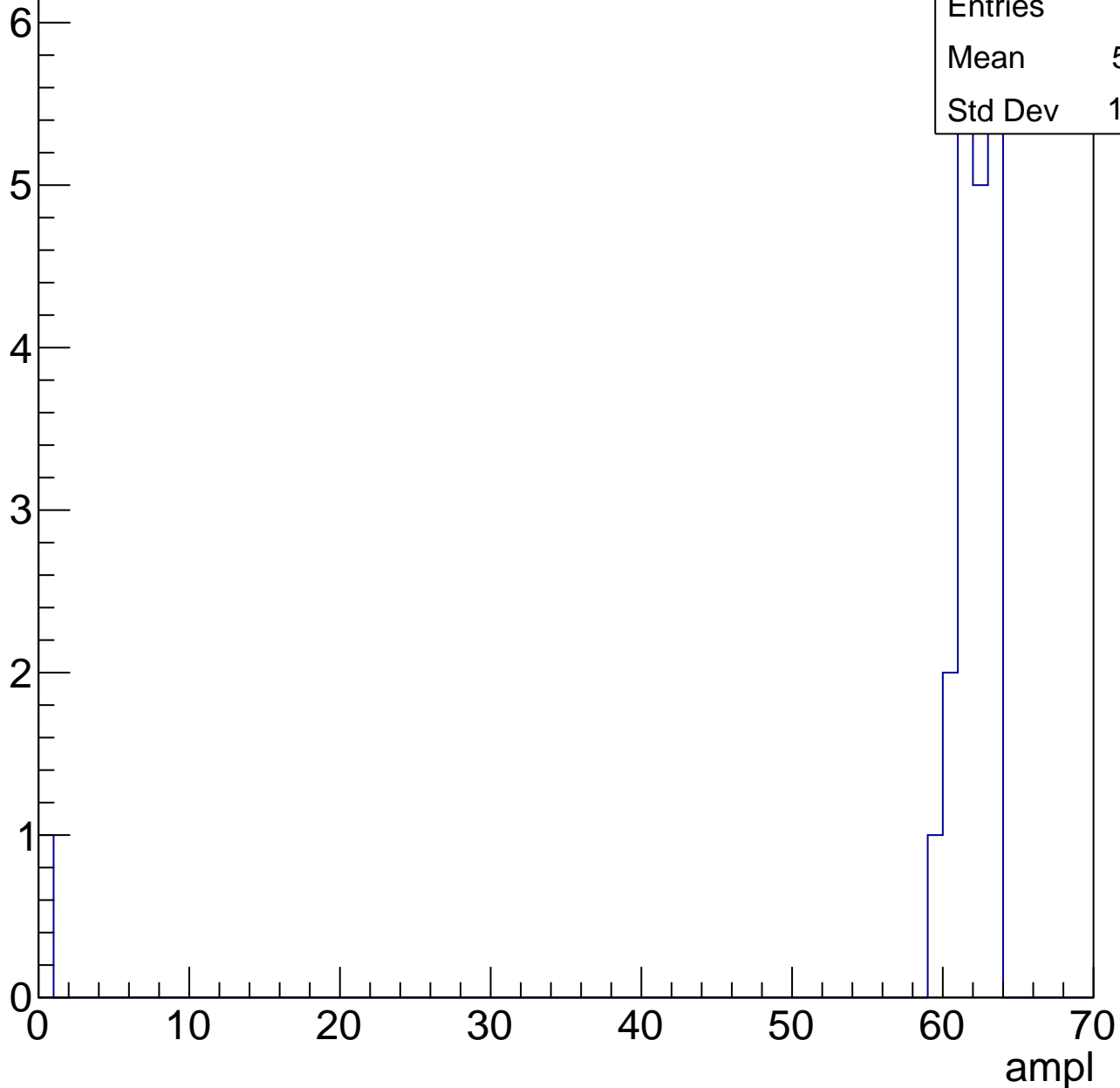
Entries	47
Mean	58.53
Std Dev	2.474



# B1L101S, U22-ch93, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U22-ch93, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U22-ch93, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	3
Mean	7.667
Std Dev	10.84

# B1L101S, U22-ch94, adc0

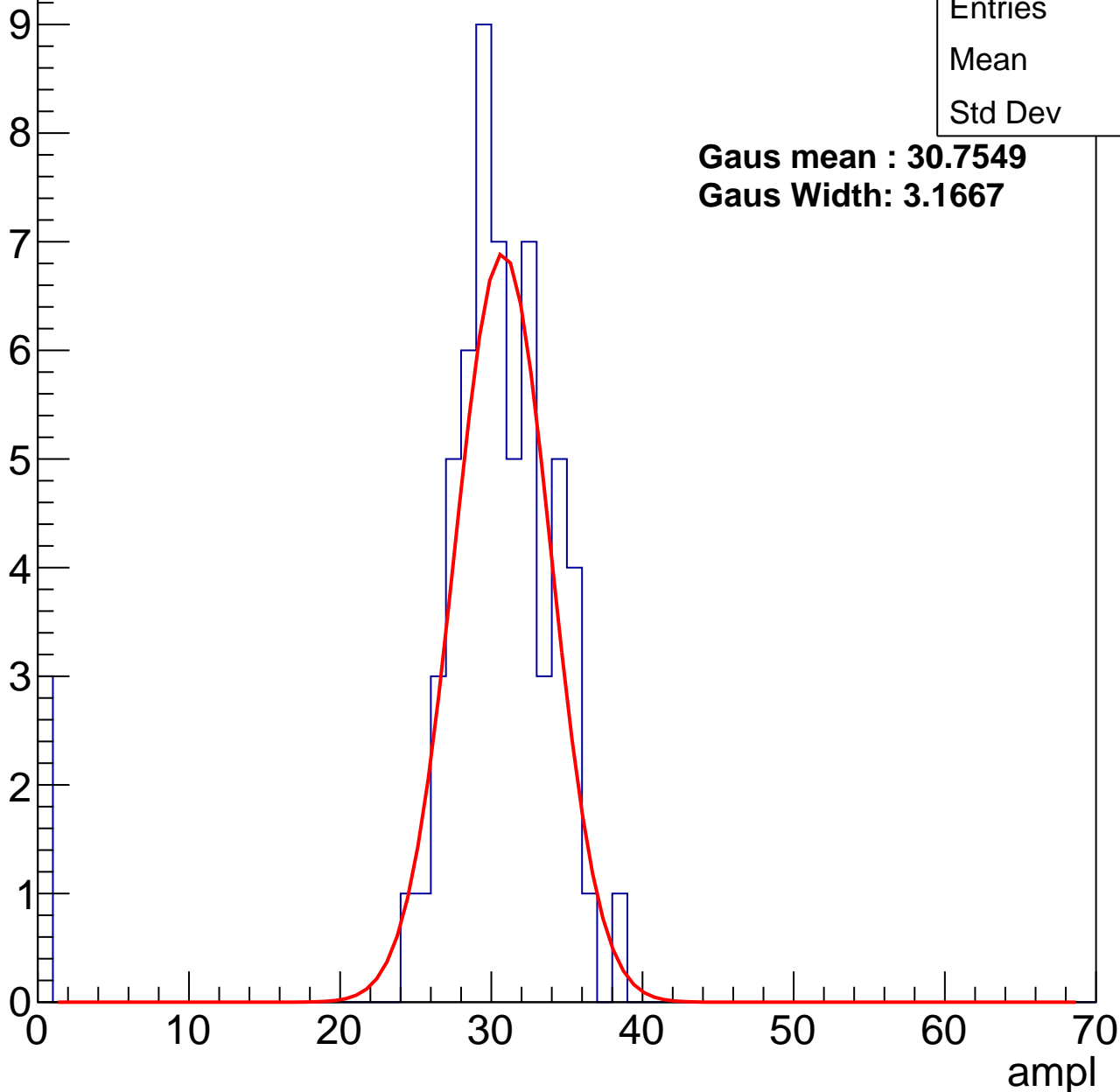
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	28.9
Std Dev	7.19

**Gaus mean : 30.7549**

**Gaus Width: 3.1667**



# B1L101S, U22-ch94, adc1

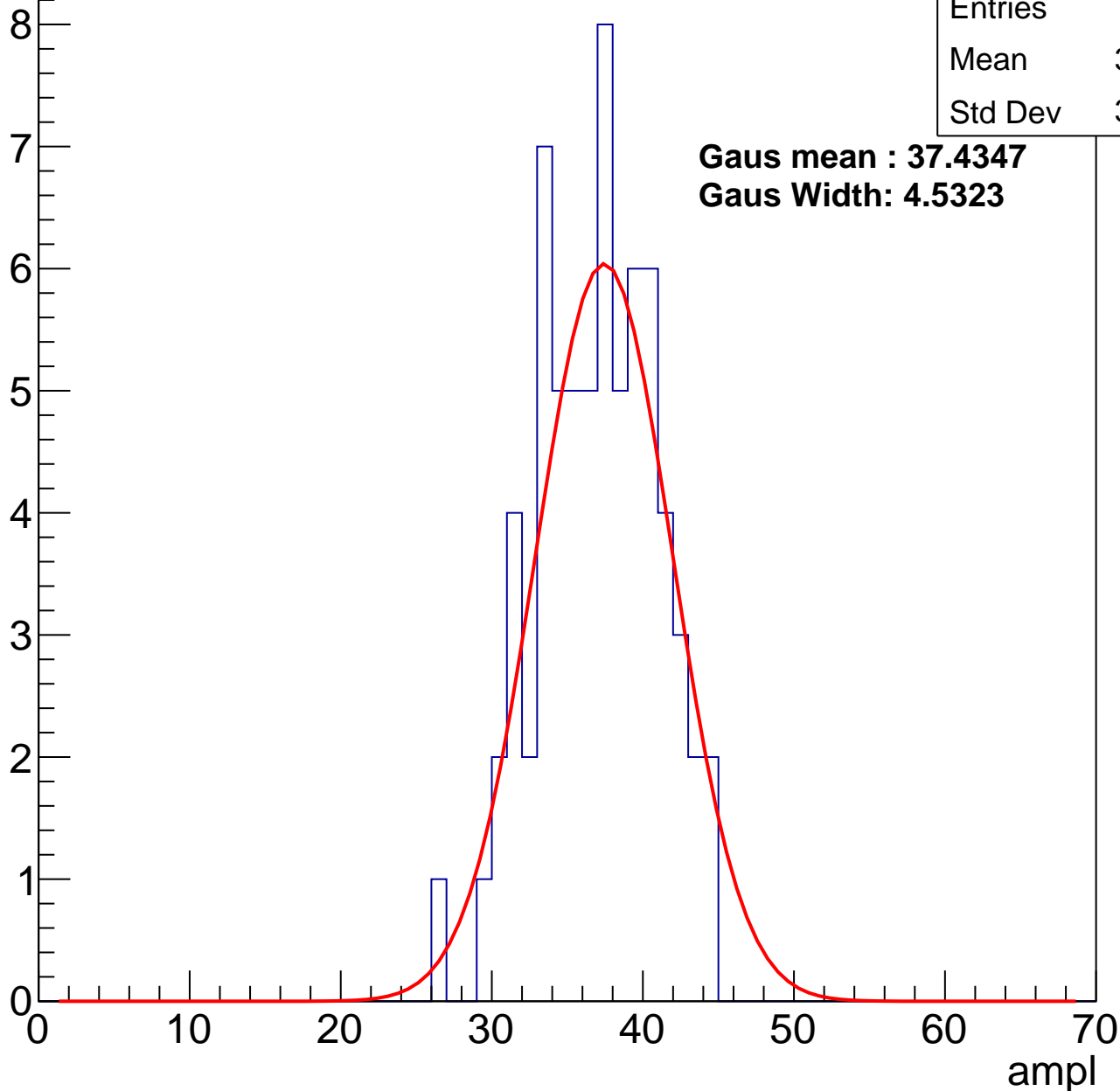
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	36.51
Std Dev	3.901

**Gaus mean : 37.4347**

**Gaus Width: 4.5323**



# B1L101S, U22-ch94, adc2

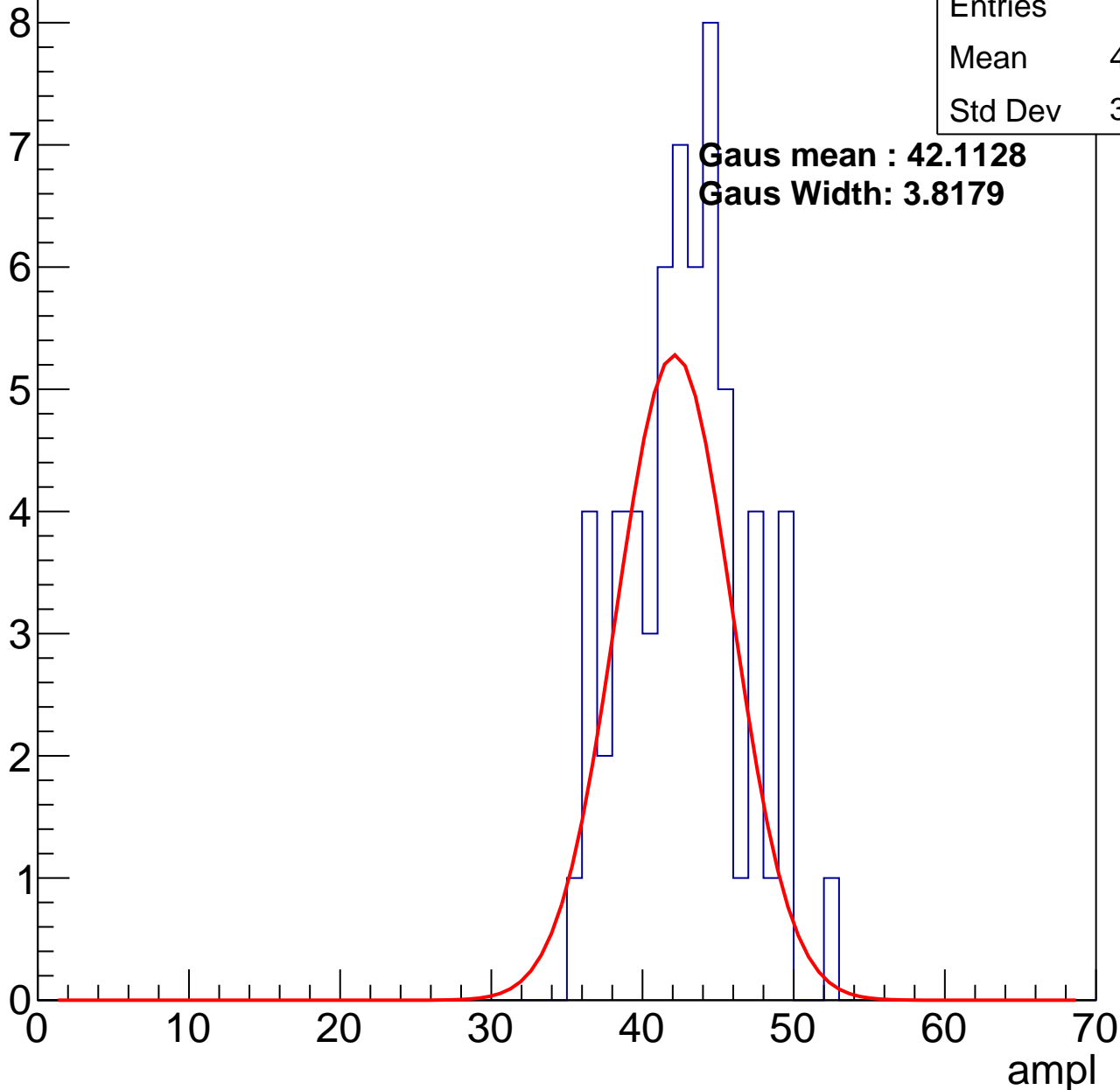
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	42.39
Std Dev	3.804

**Gaus mean : 42.1128**

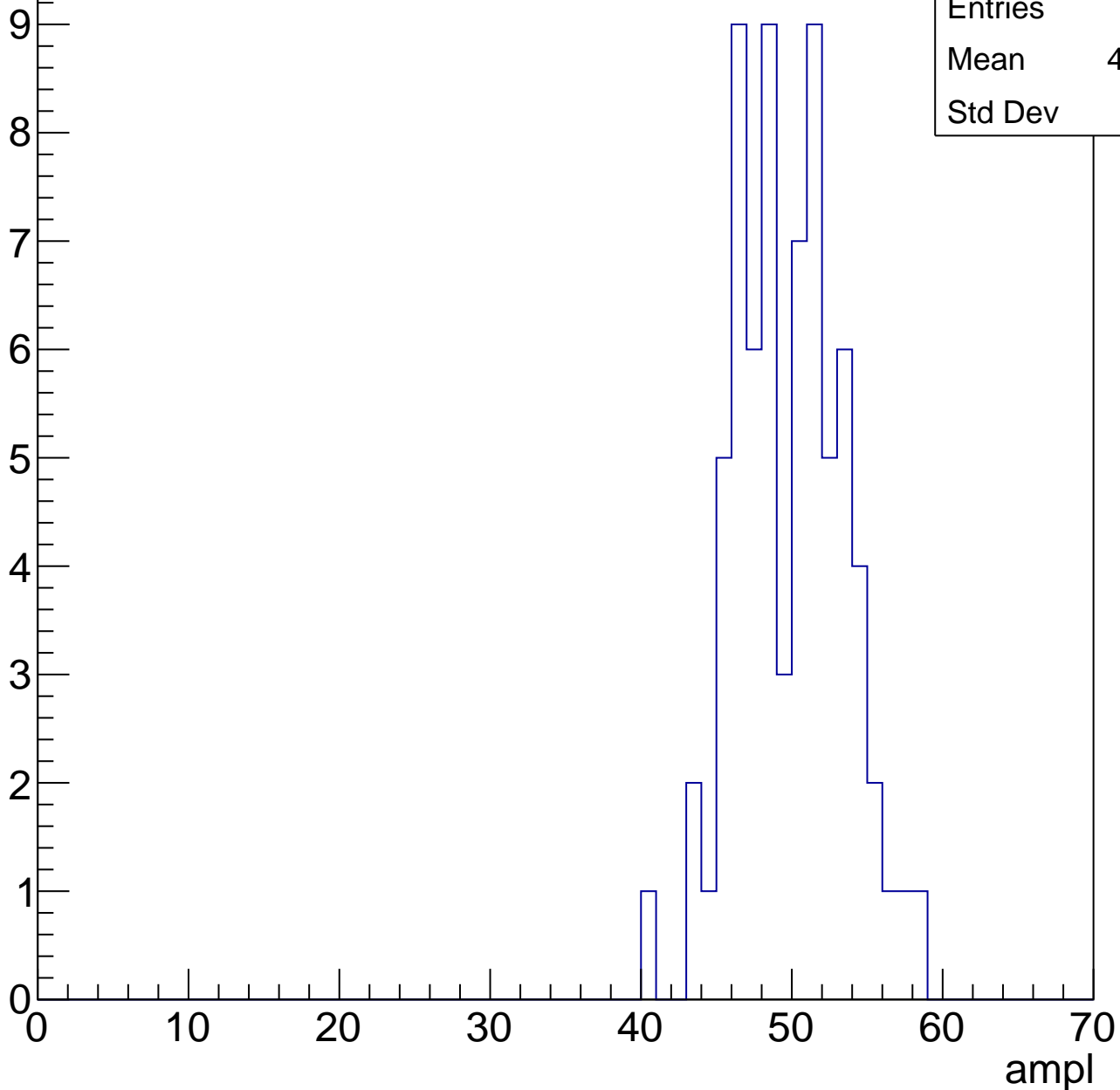
**Gaus Width: 3.8179**



# B1L101S, U22-ch94, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

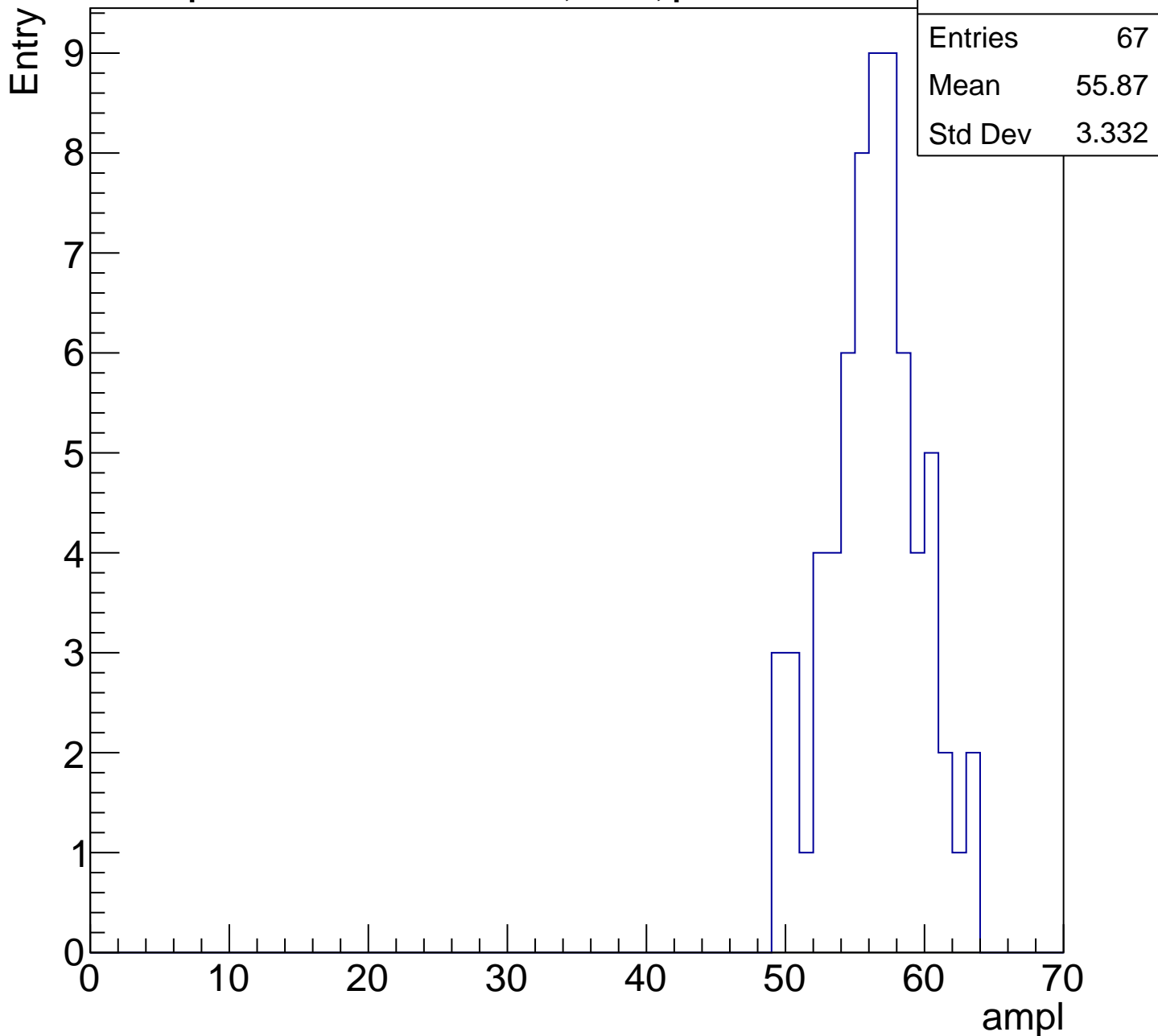
Entry



Entries	72
Mean	49.36
Std Dev	3.56

# B1L101S, U22-ch94, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

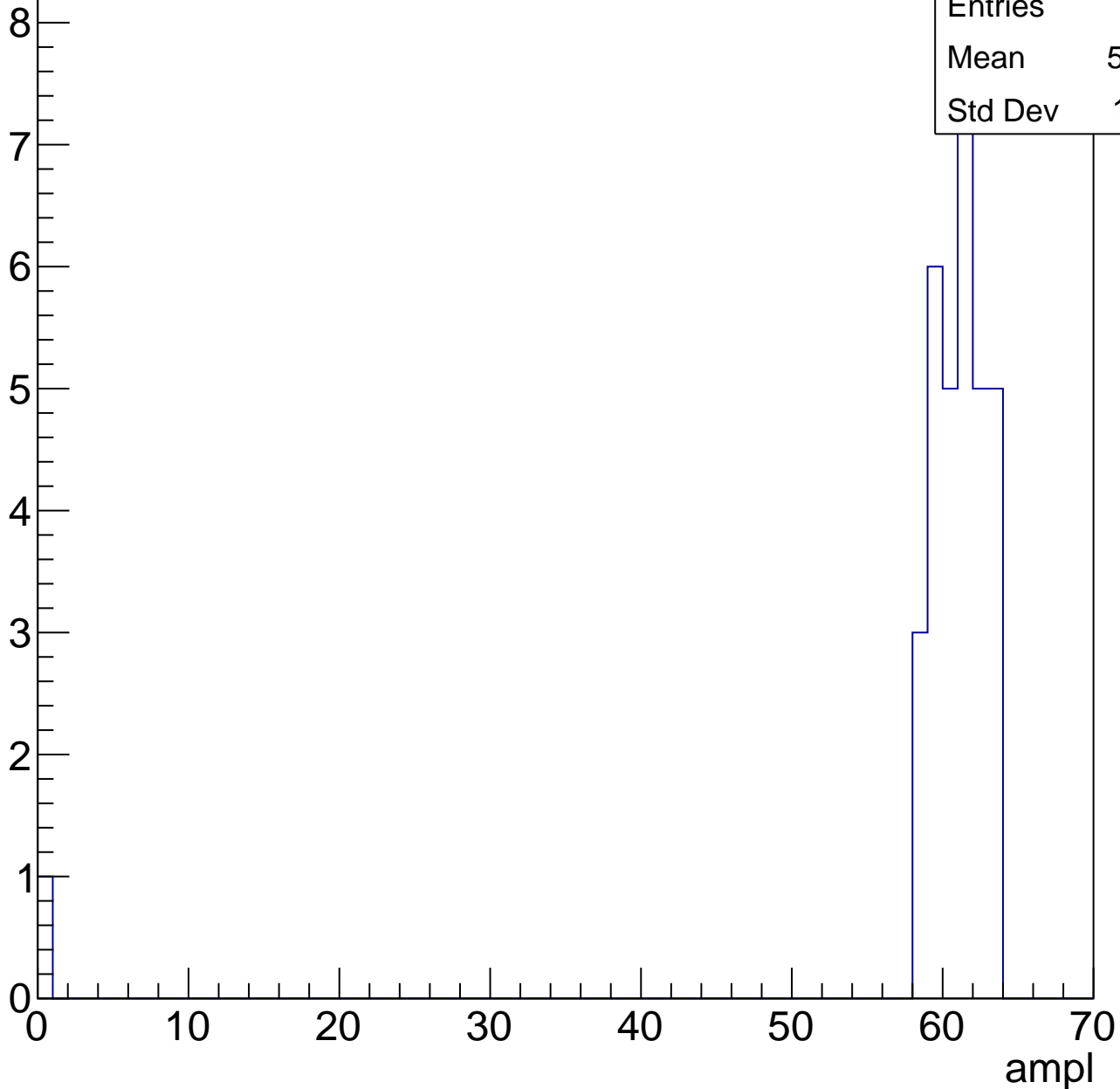


# B1L101S, U22-ch94, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

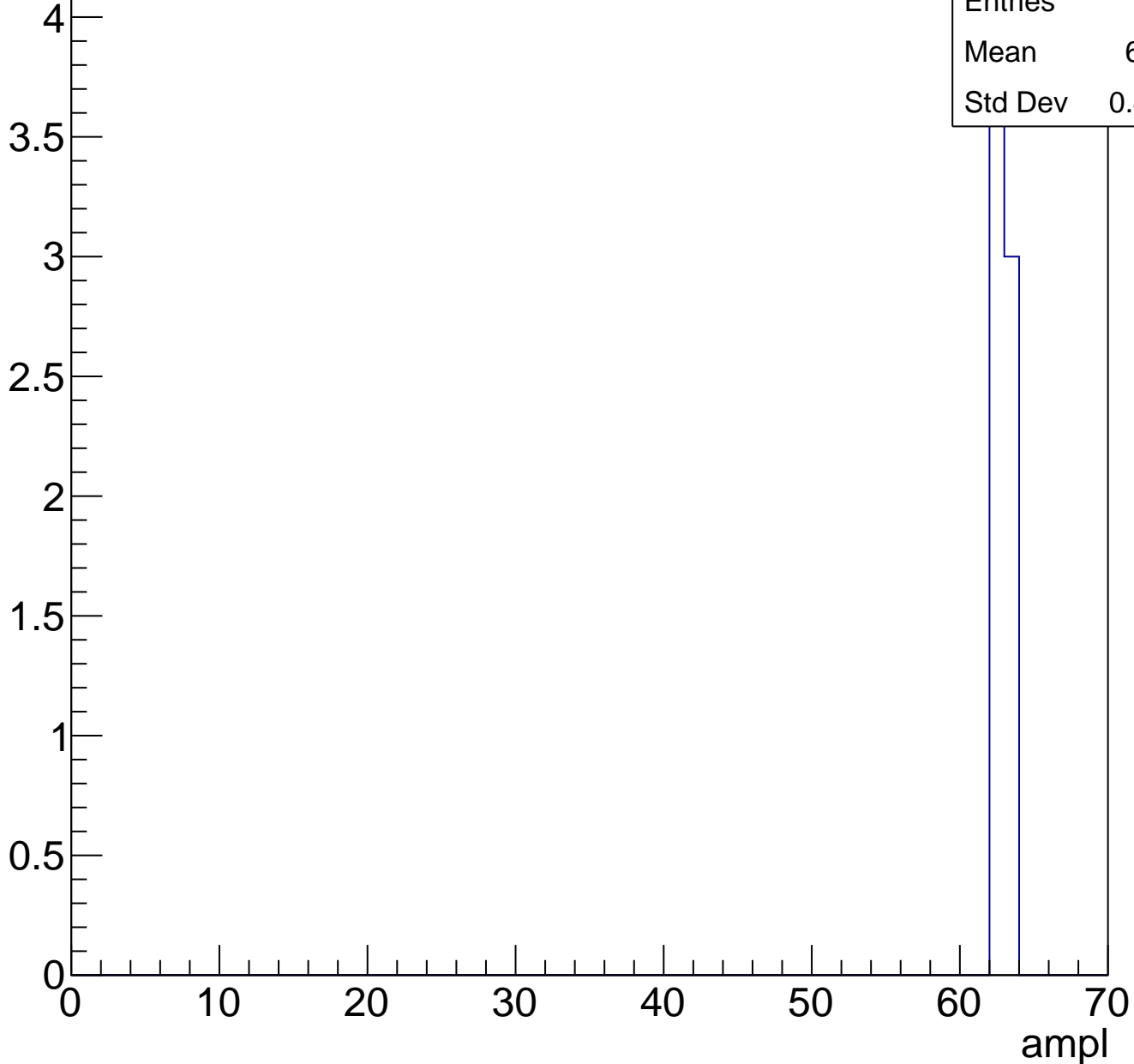
Entries	33
Mean	58.82
Std Dev	10.51



# B1L101S, U22-ch94, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	7
Mean	62.43
Std Dev	0.4949



# B1L101S, U22-ch94, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U22-ch95, adc0

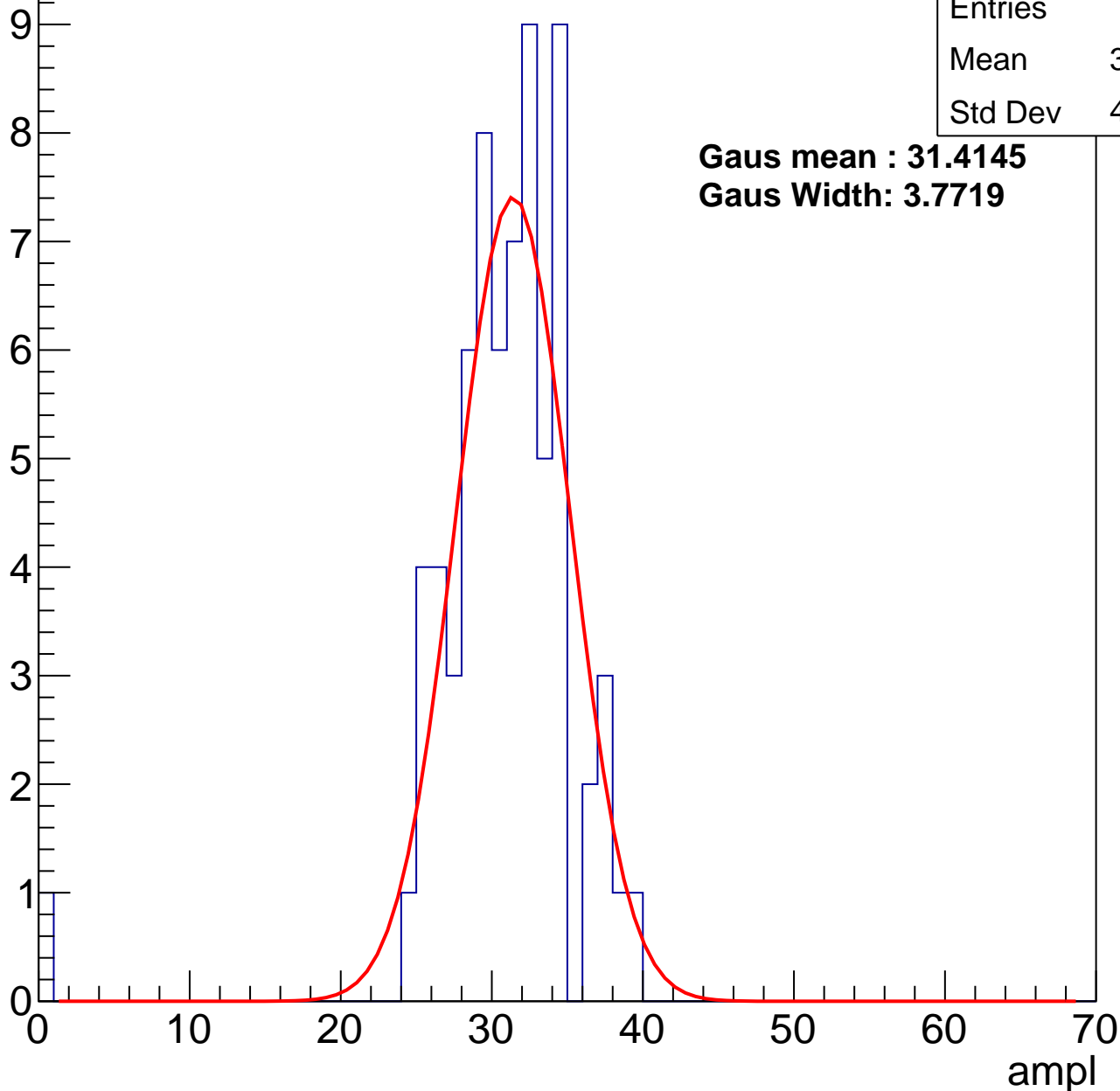
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	30.36
Std Dev	4.994

**Gaus mean : 31.4145**

**Gaus Width: 3.7719**



# B1L101S, U22-ch95, adc1

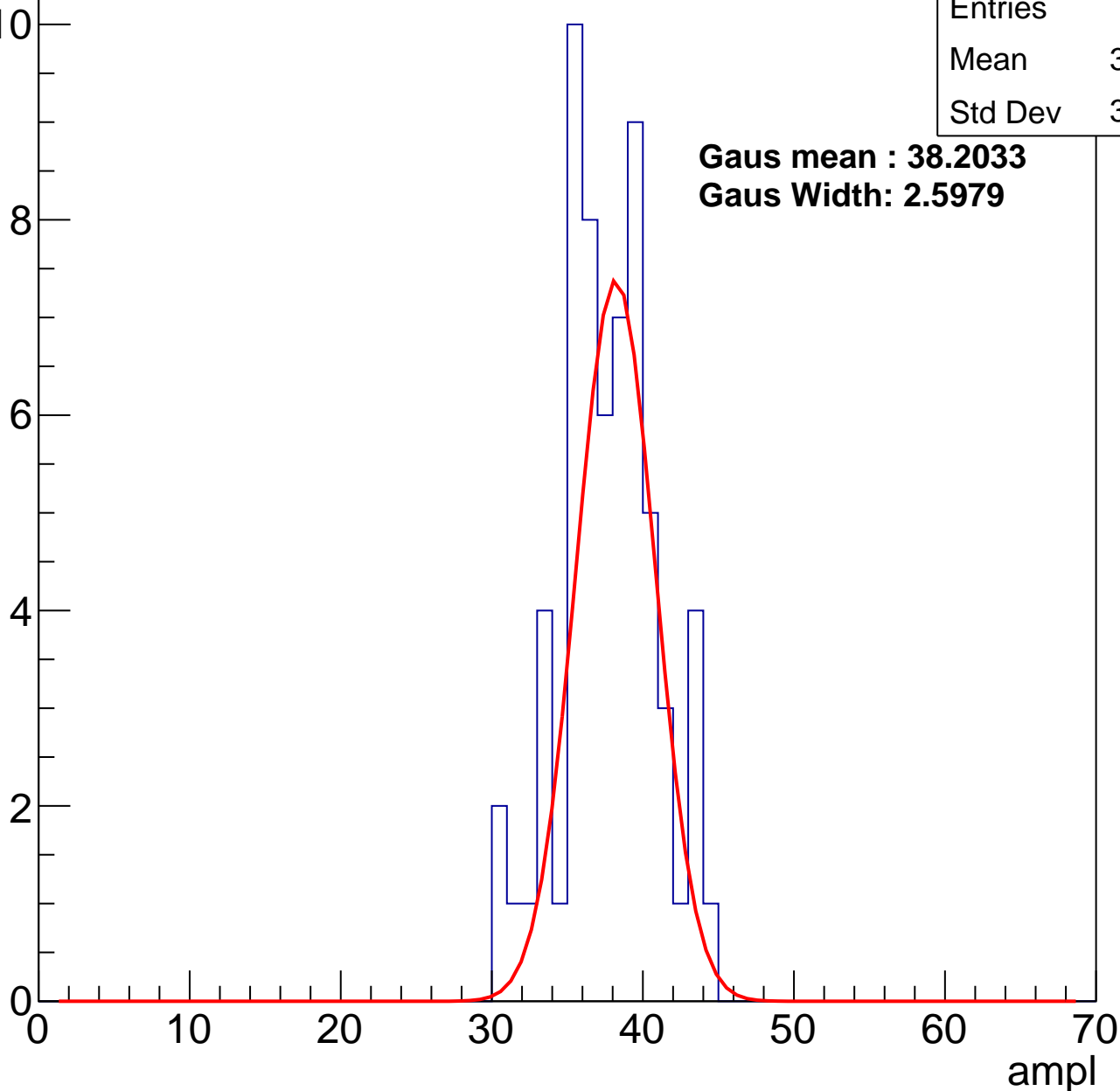
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	37.25
Std Dev	3.162

**Gaus mean : 38.2033**

**Gaus Width: 2.5979**



# B1L101S, U22-ch95, adc2

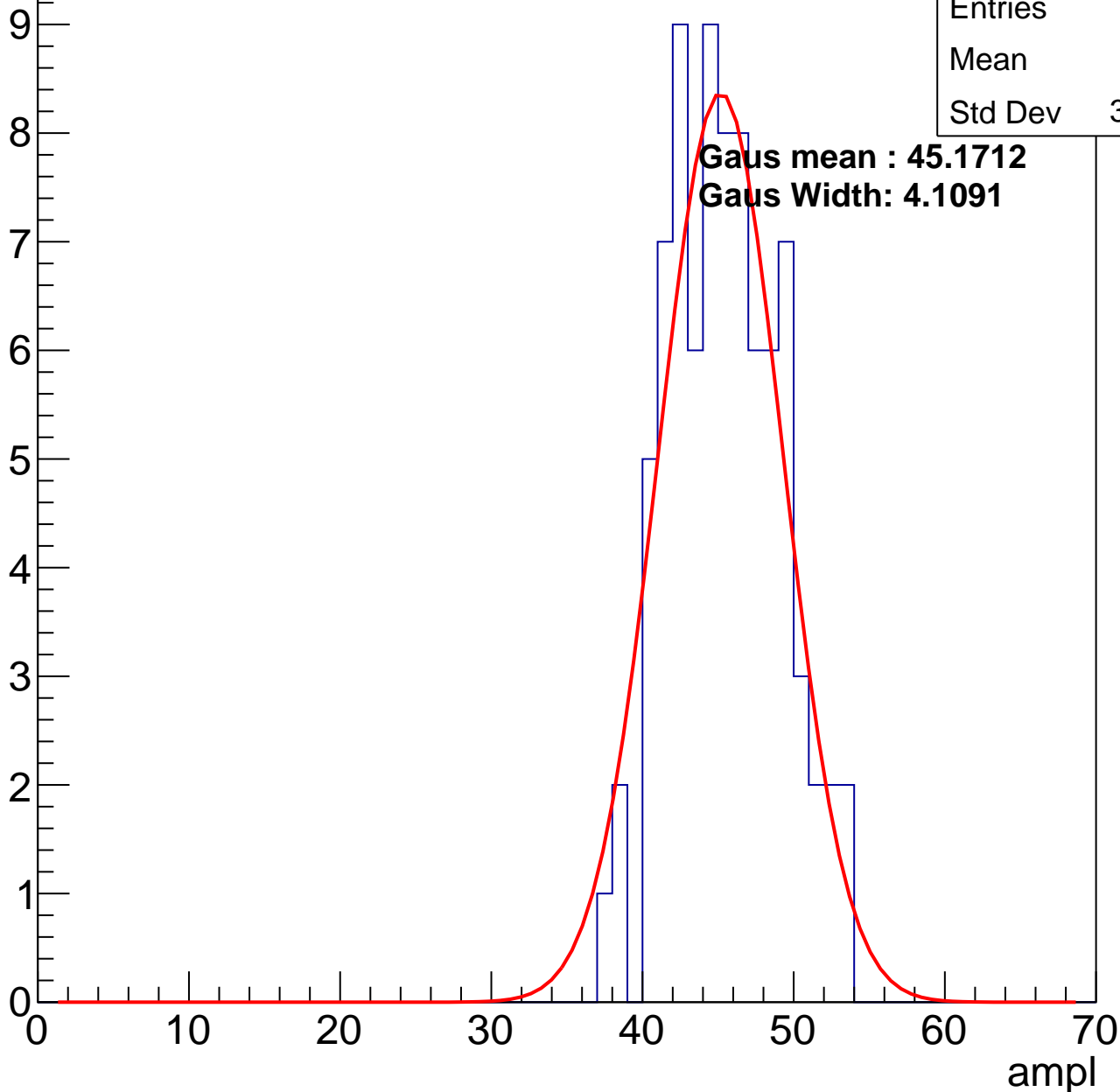
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	83
Mean	45
Std Dev	3.614

**Gaus mean : 45.1712**

**Gaus Width: 4.1091**

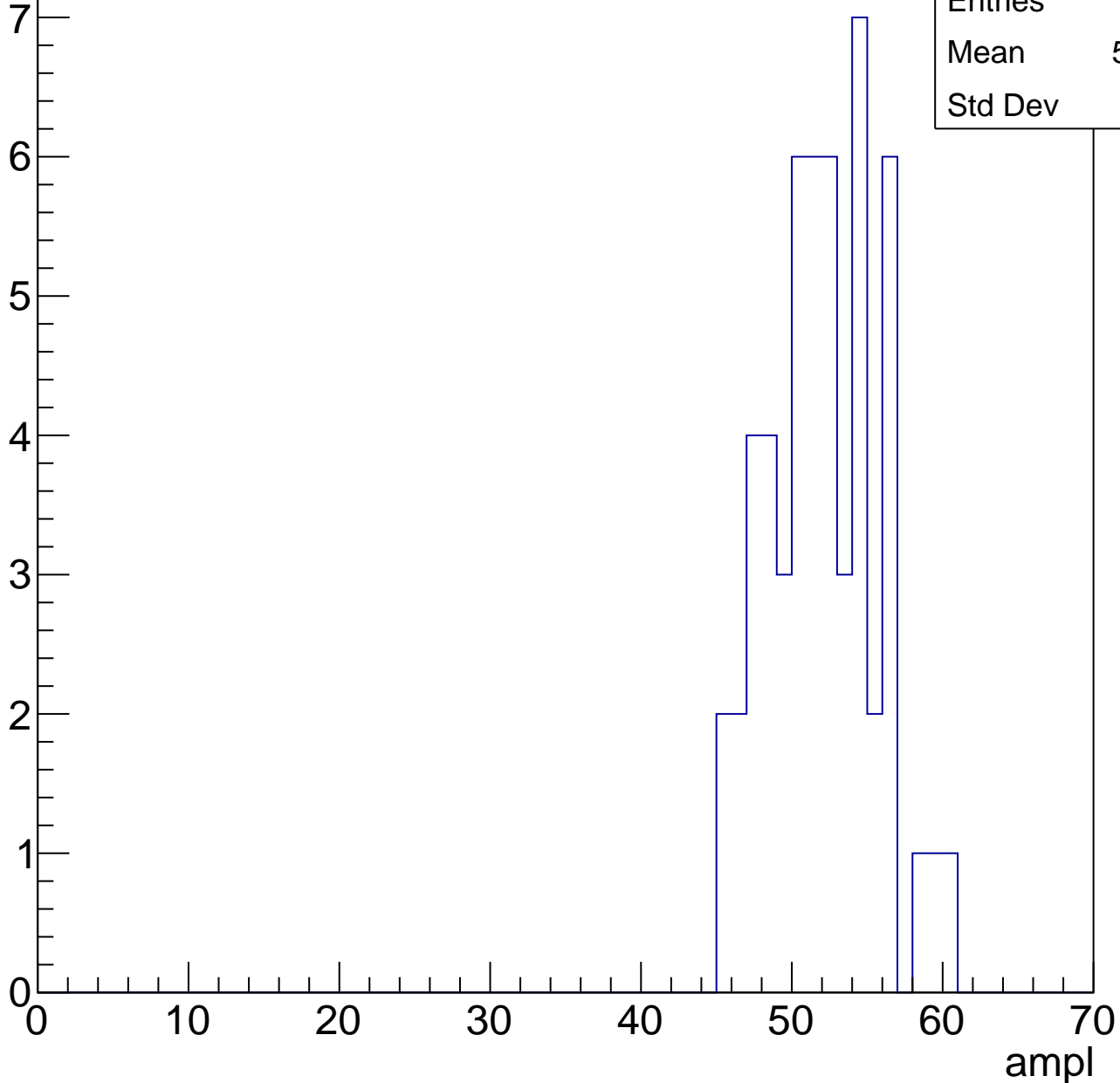


# B1L101S, U22-ch95, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

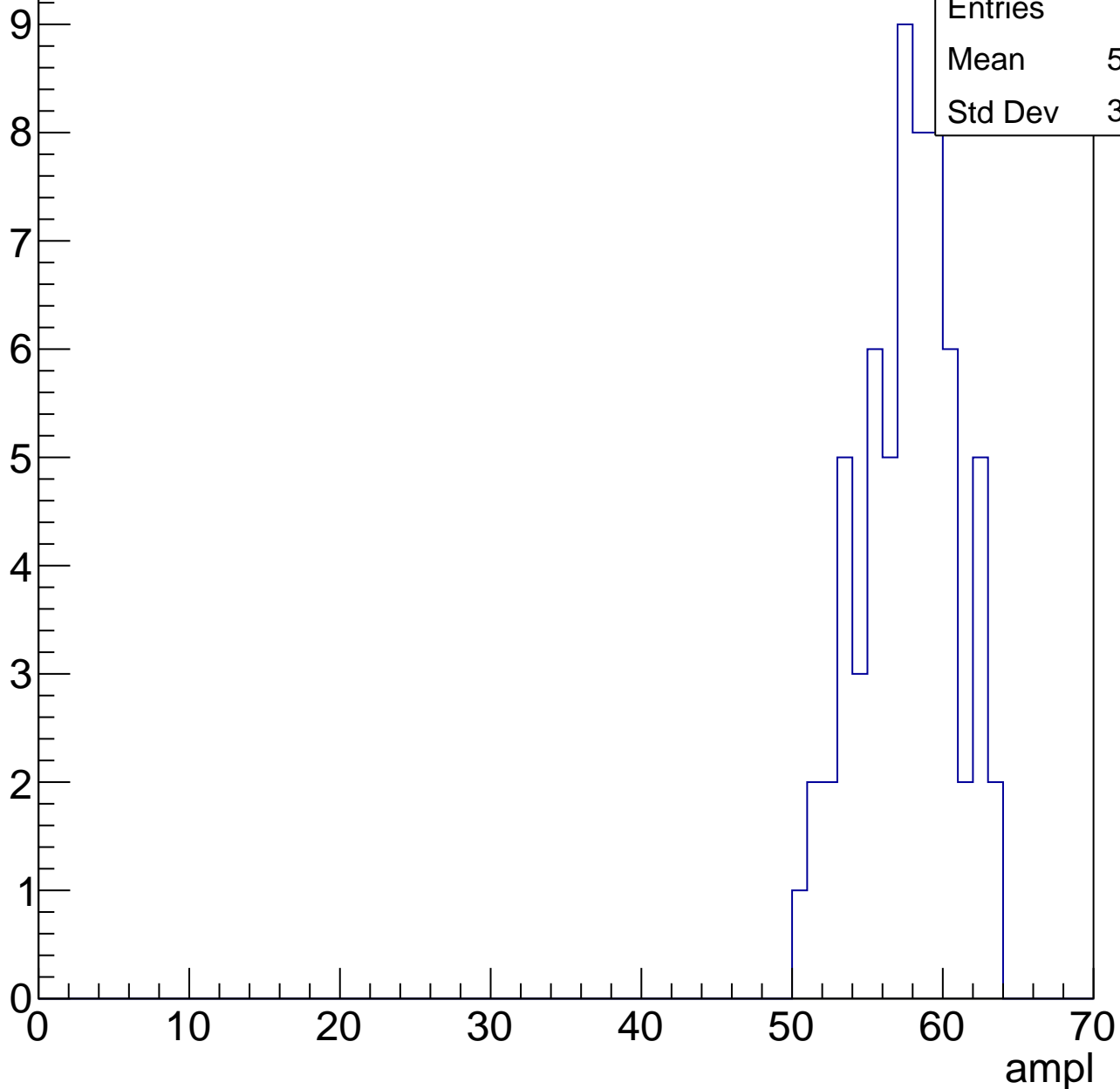
Entries	54
Mean	51.61
Std Dev	3.54



# B1L101S, U22-ch95, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



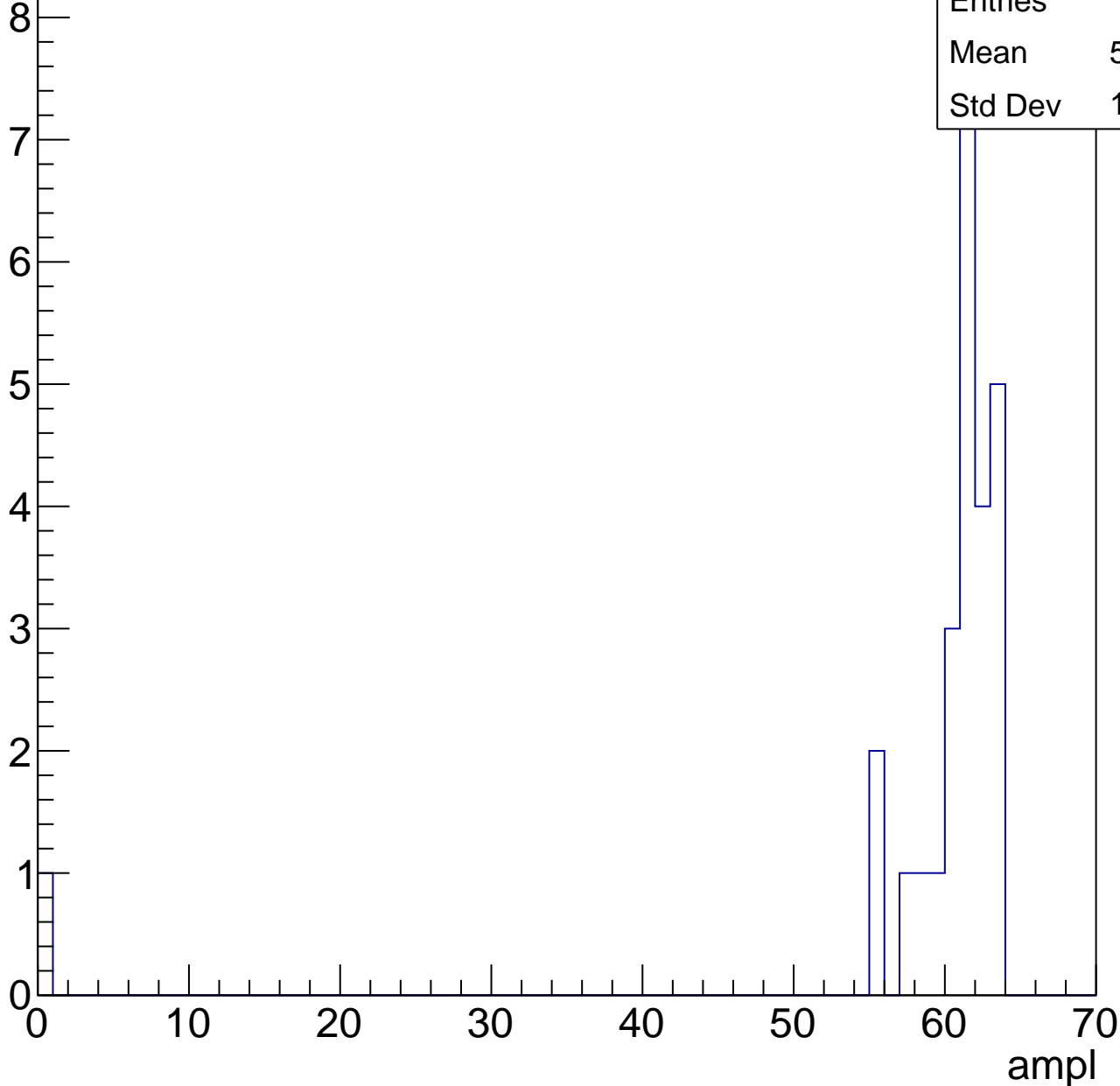
Entries	64
Mean	57.19
Std Dev	3.132

# B1L101S, U22-ch95, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	26
Mean	58.27
Std Dev	11.86



# B1L101S, U22-ch95, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U22-ch95, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U22-ch96, adc0

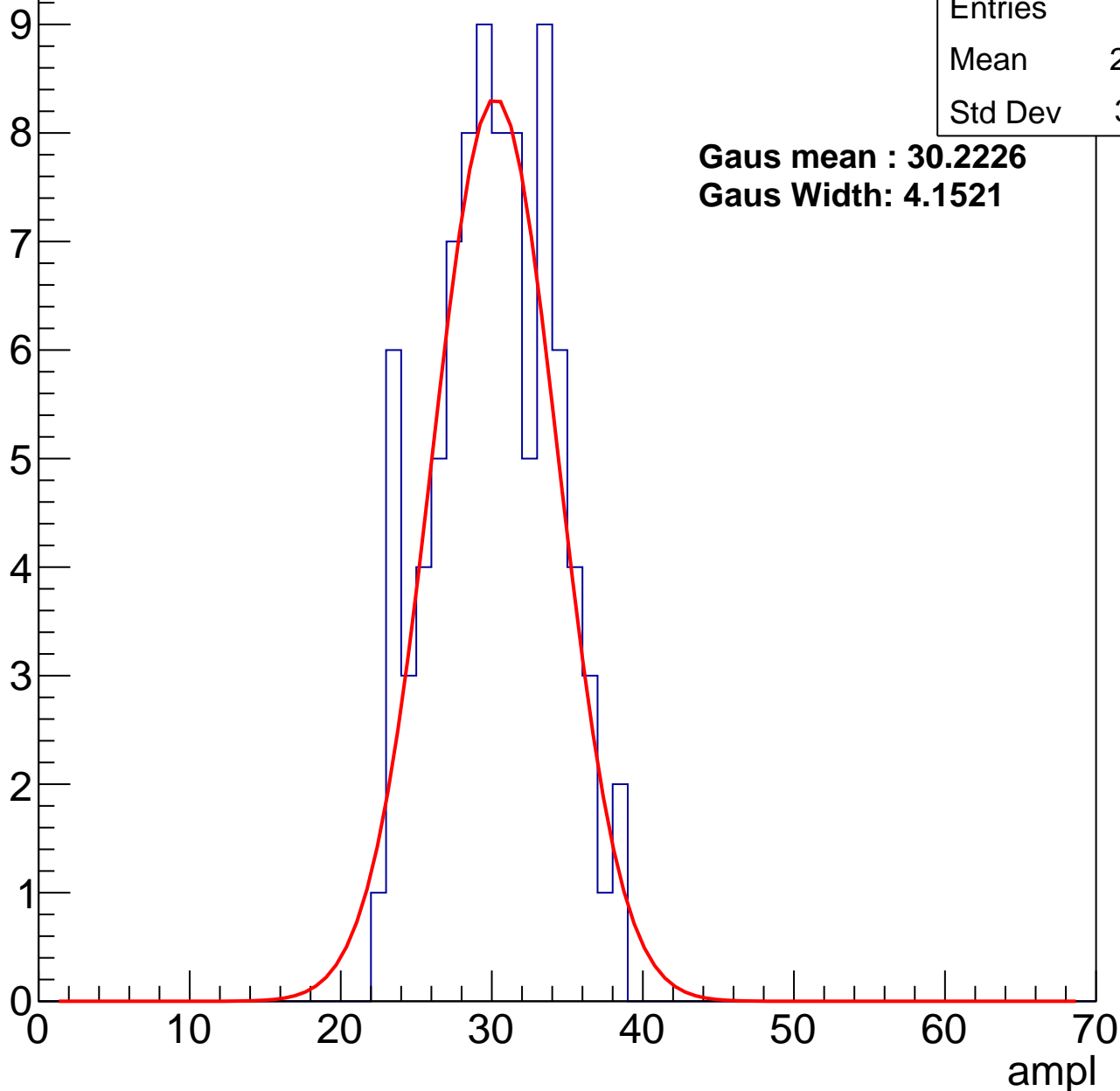
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	89
Mean	29.73
Std Dev	3.871

**Gaus mean : 30.2226**

**Gaus Width: 4.1521**



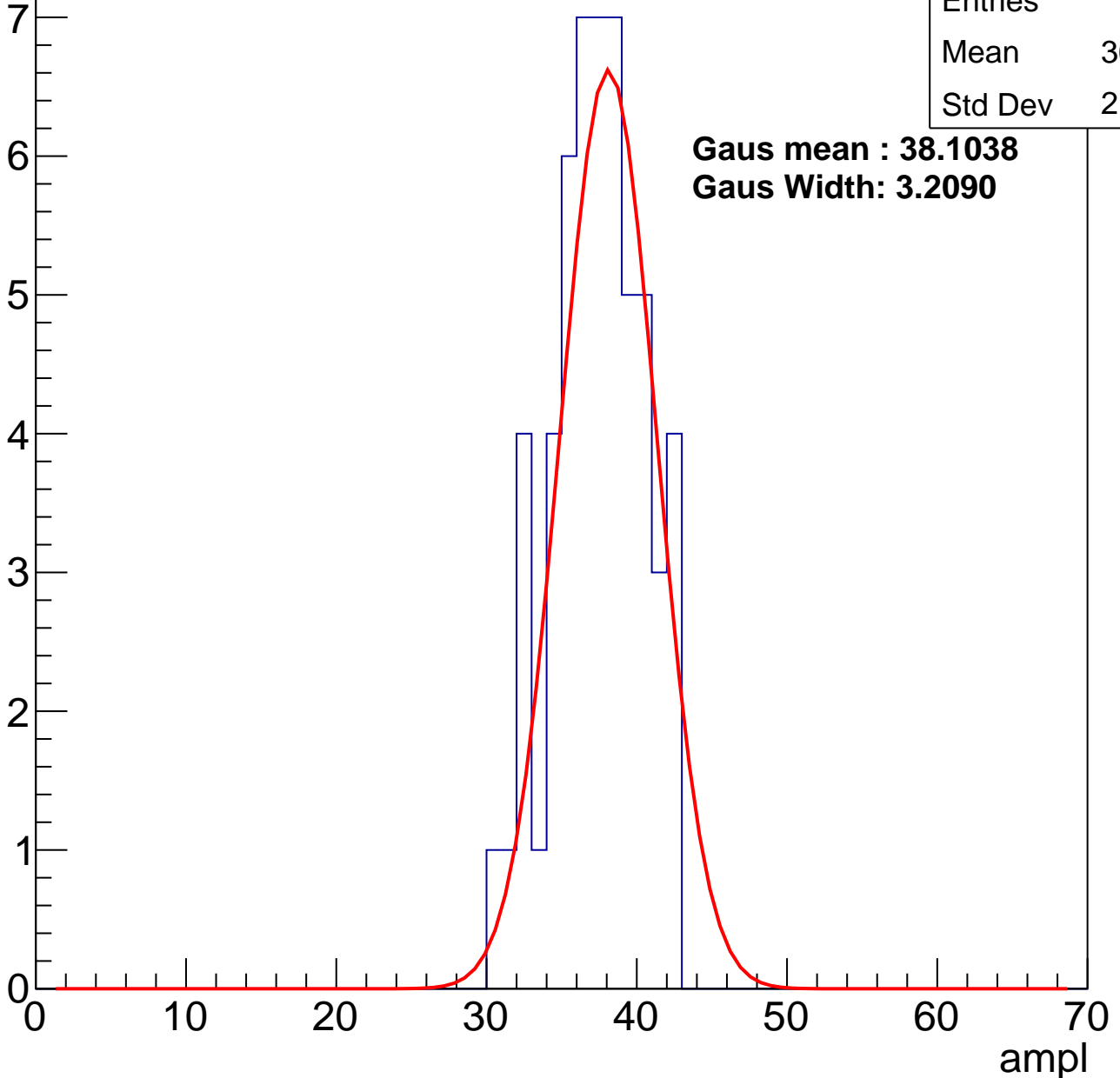
# B1L101S, U22-ch96, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	55
Mean	36.93
Std Dev	2.978

**Gaus mean : 38.1038**  
**Gaus Width: 3.2090**



# B1L101S, U22-ch96, adc2

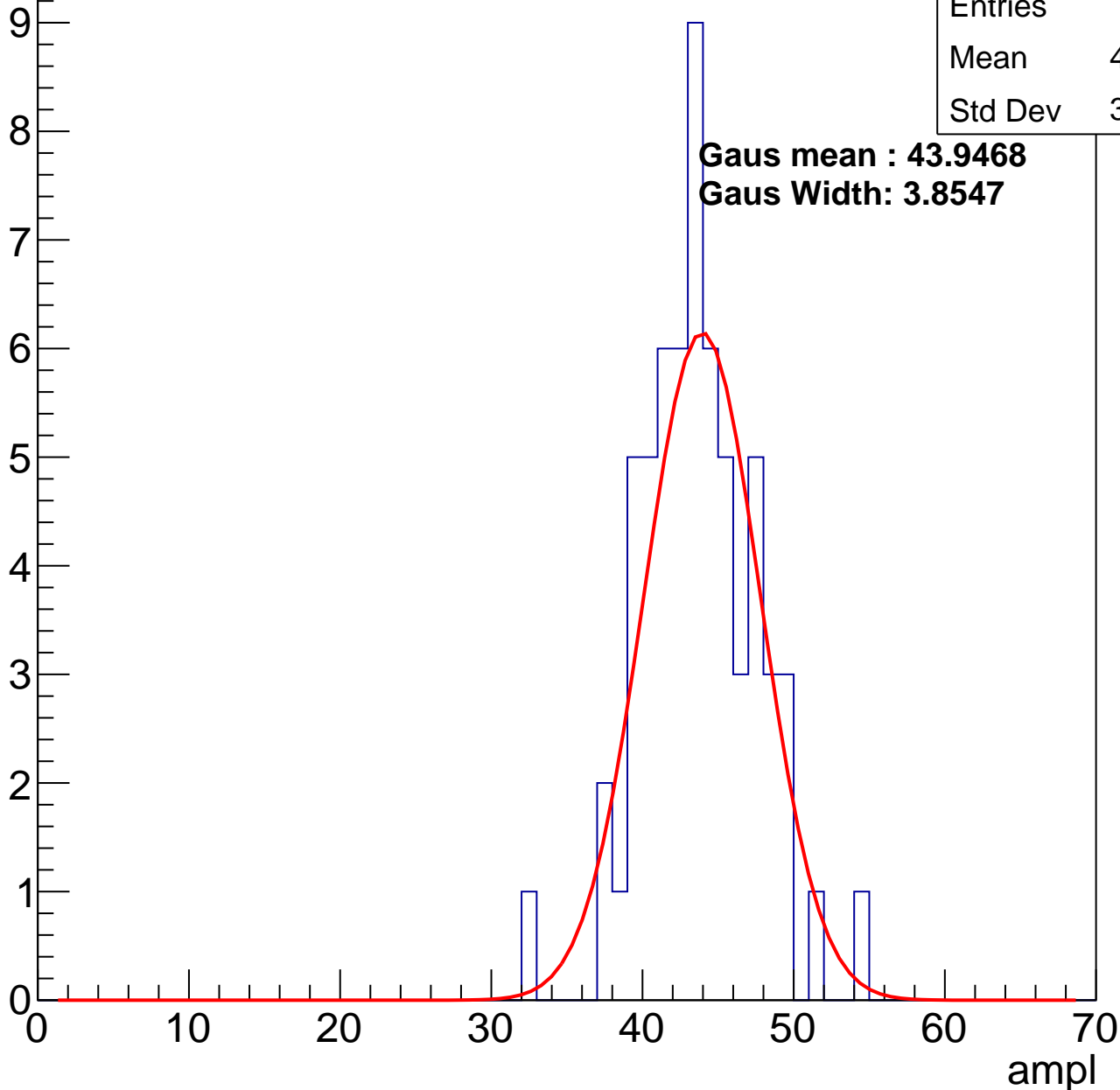
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	43.26
Std Dev	3.746

**Gaus mean : 43.9468**

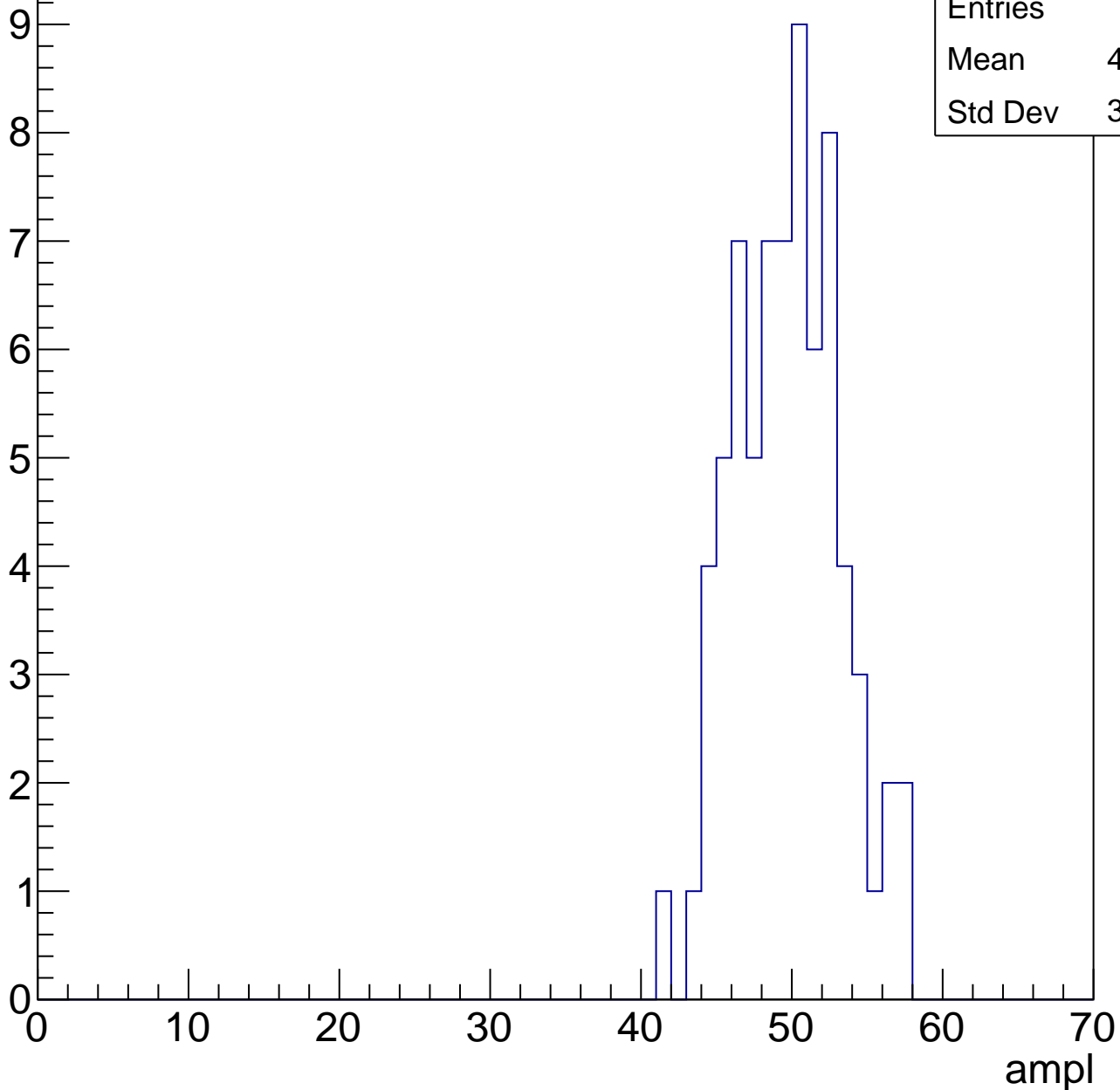
**Gaus Width: 3.8547**



# B1L101S, U22-ch96, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

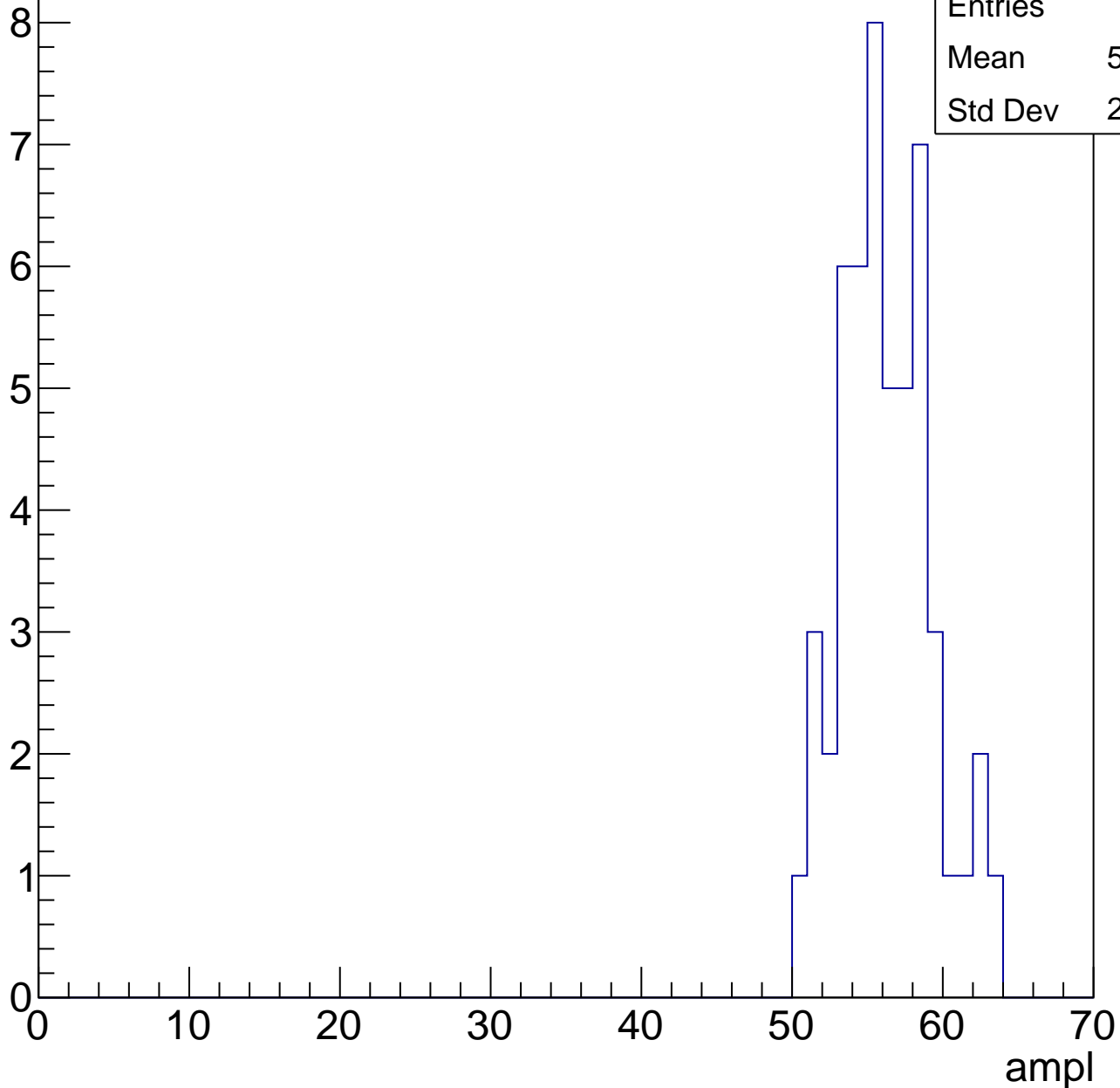
Entry



# B1L101S, U22-ch96, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

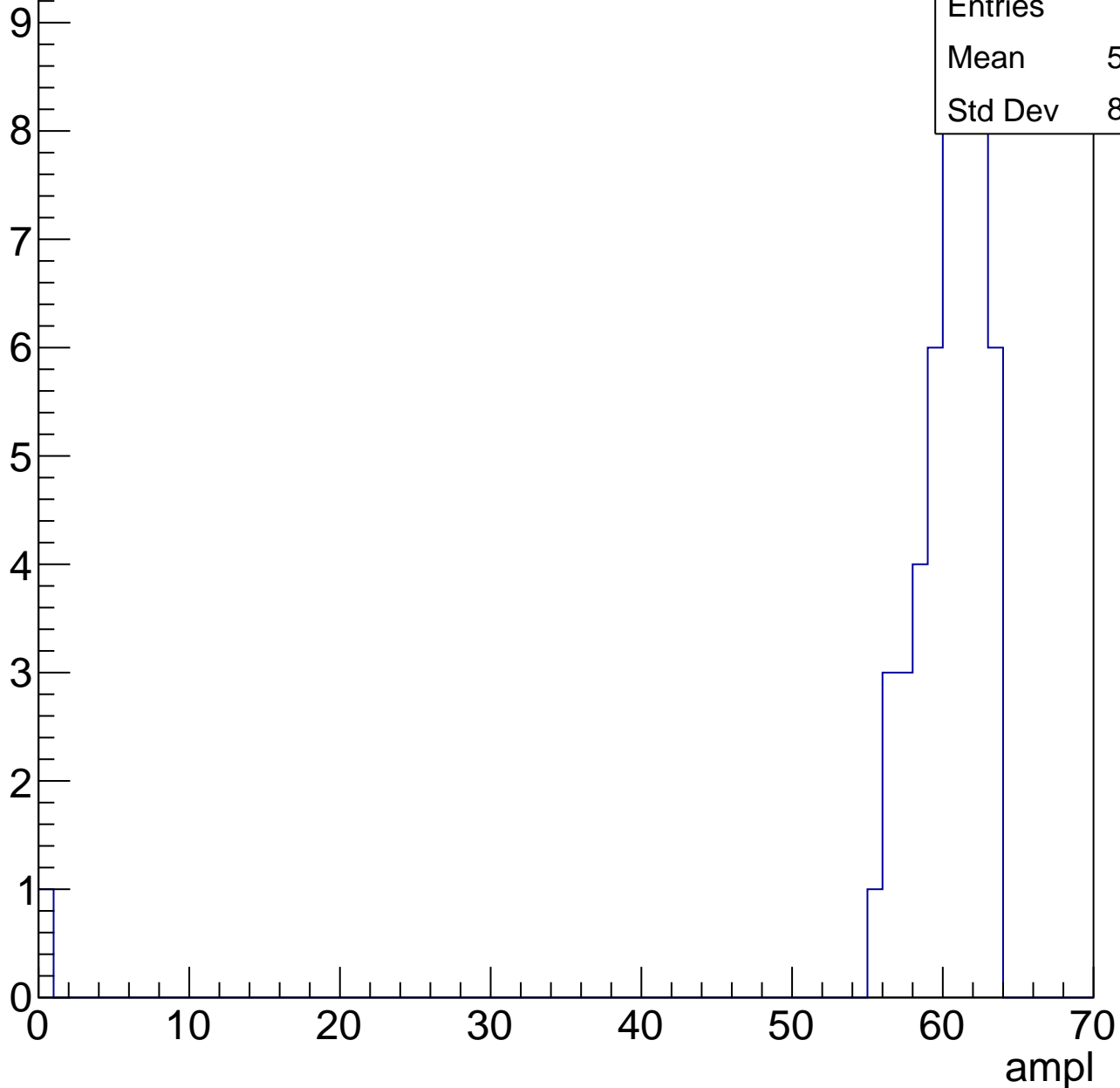


Entries	51
Mean	55.78
Std Dev	2.966

# B1L101S, U22-ch96, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

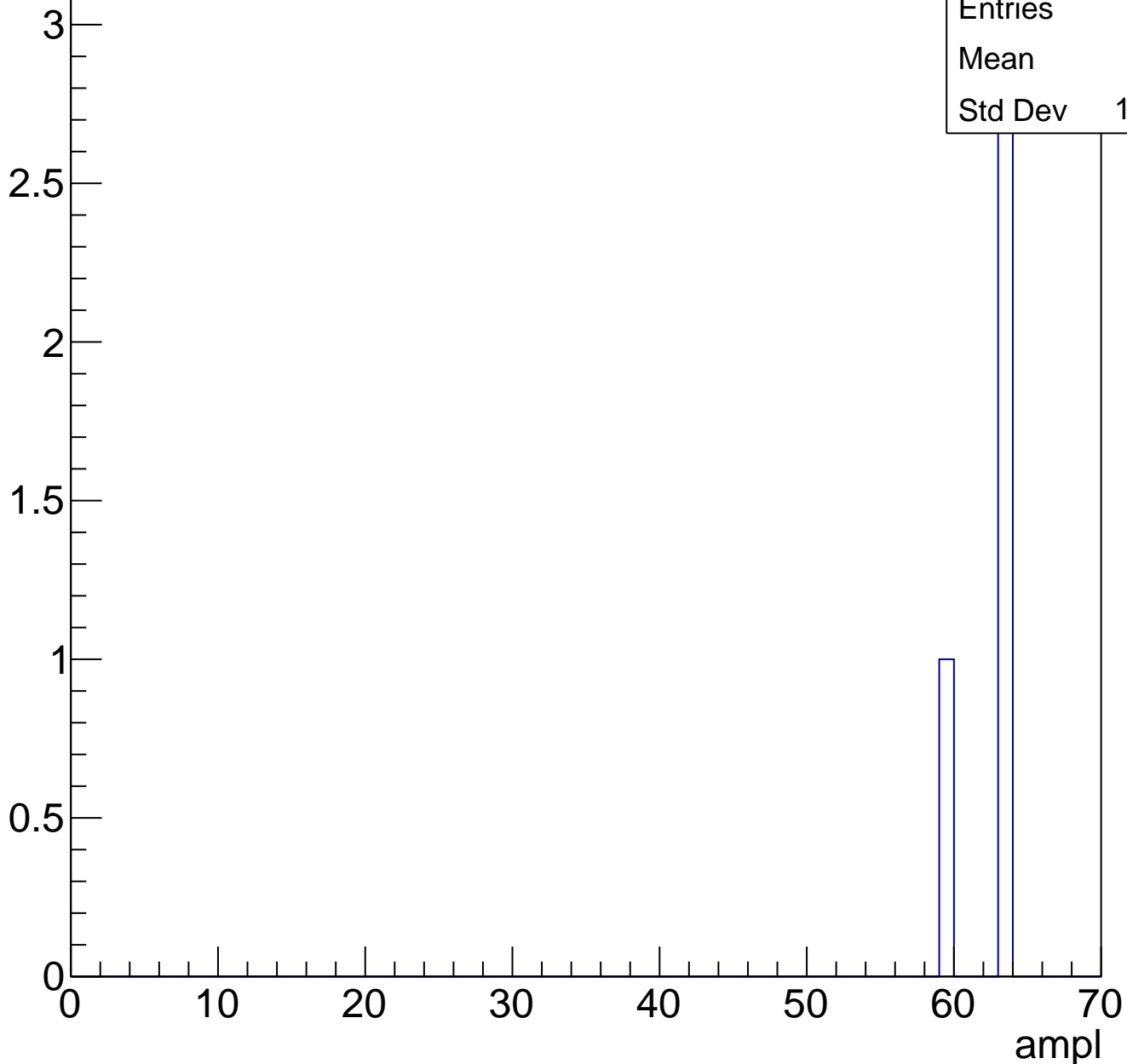
Entry



# B1L101S, U22-ch96, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U22-ch96, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U22-ch97, adc0

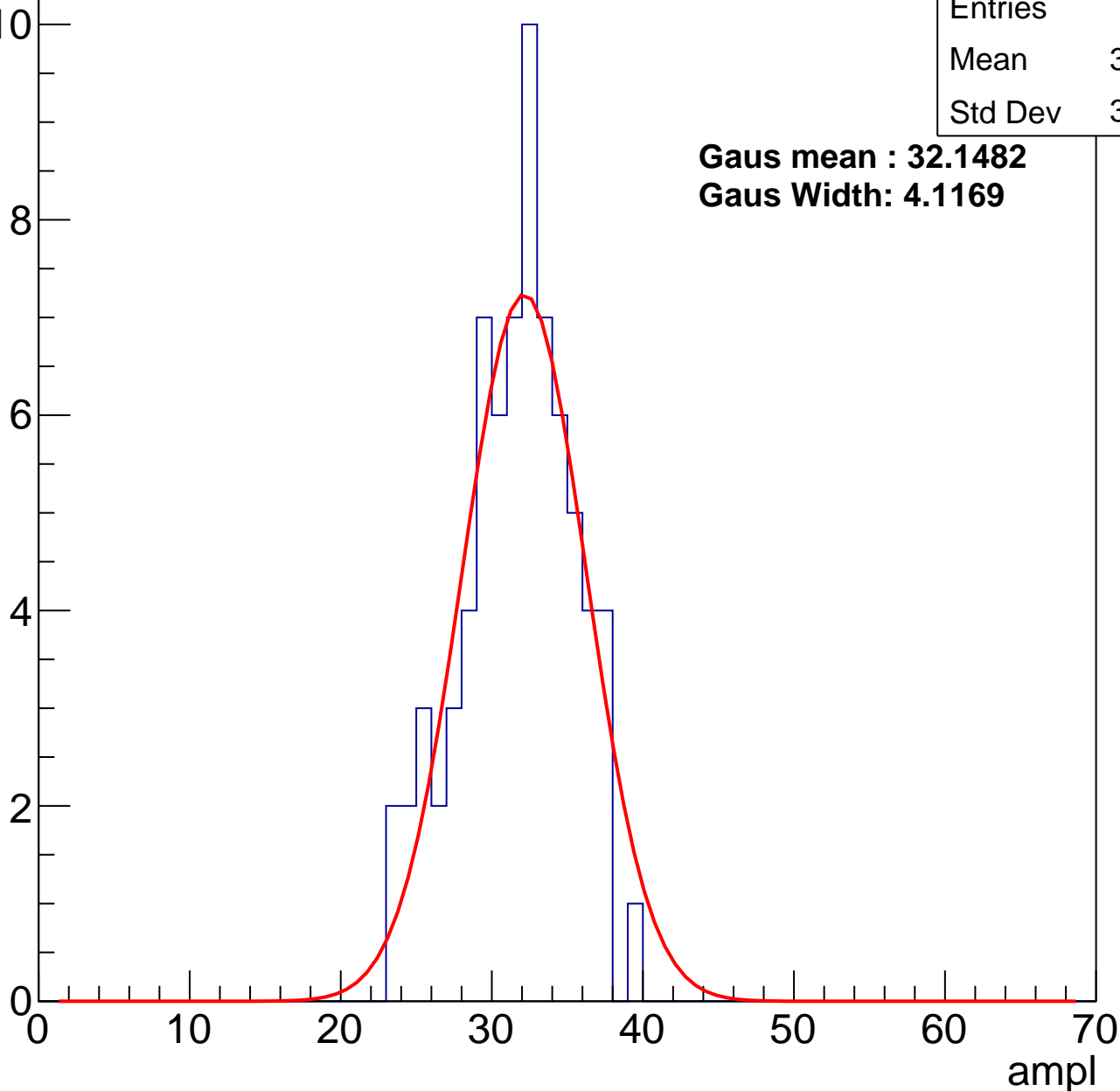
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	73
Mean	31.16
Std Dev	3.664

**Gaus mean : 32.1482**

**Gaus Width: 4.1169**



# B1L101S, U22-ch97, adc1

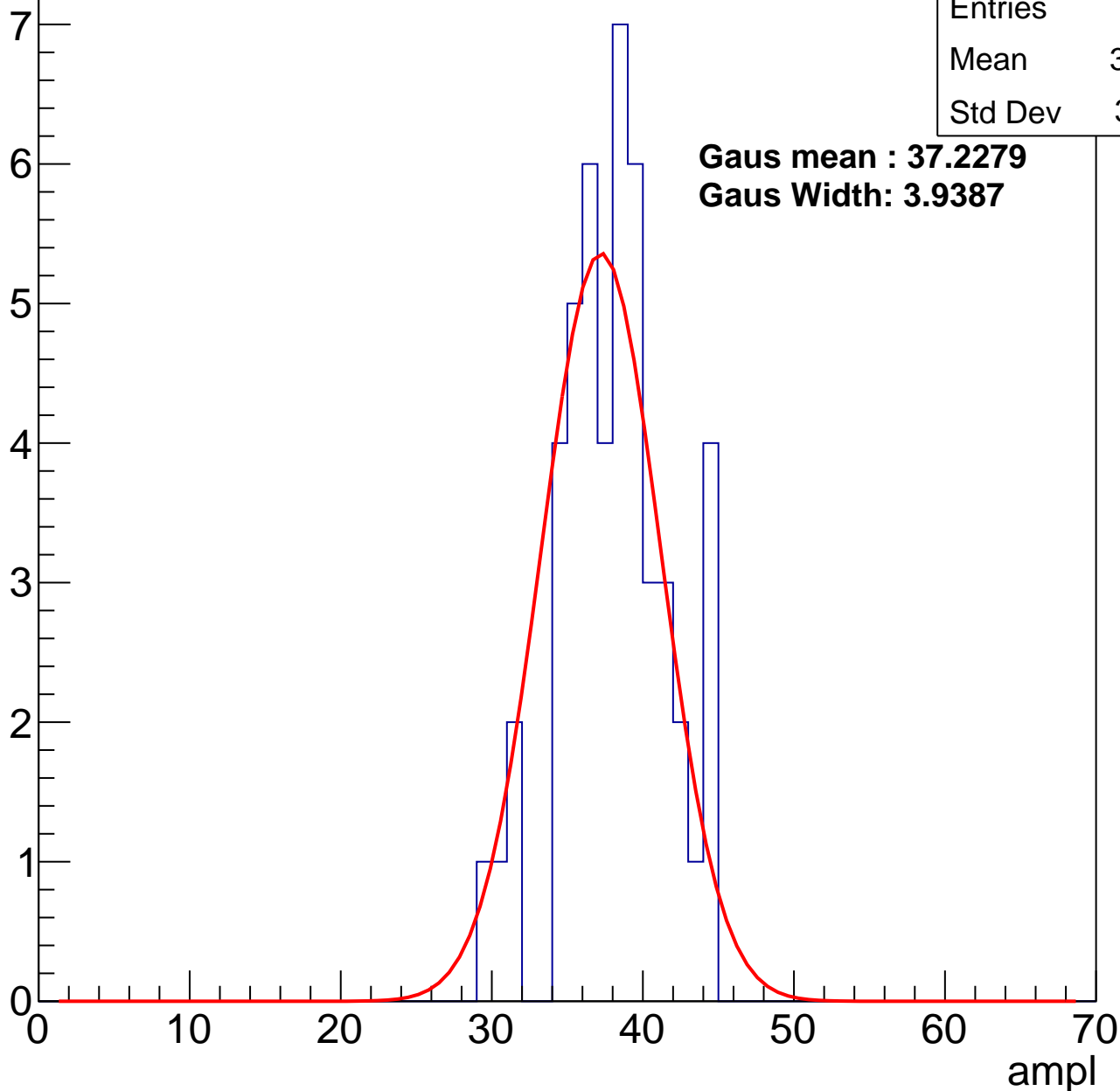
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	49
Mean	37.59
Std Dev	3.551

**Gaus mean : 37.2279**

**Gaus Width: 3.9387**



# B1L101S, U22-ch97, adc2

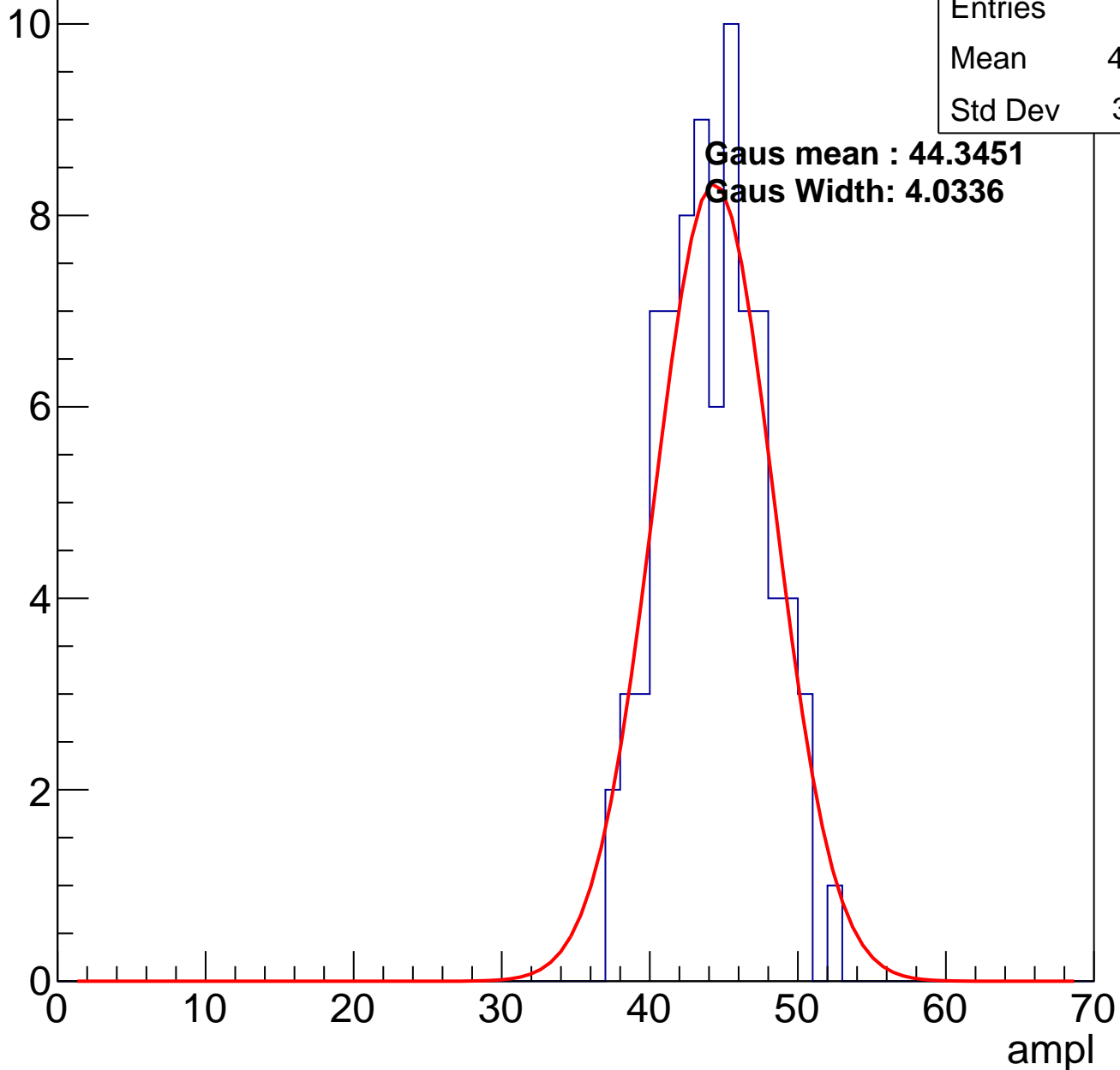
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	81
Mean	43.83
Std Dev	3.391

**Gaus mean : 44.3451**

**Gaus Width: 4.0336**

Entry

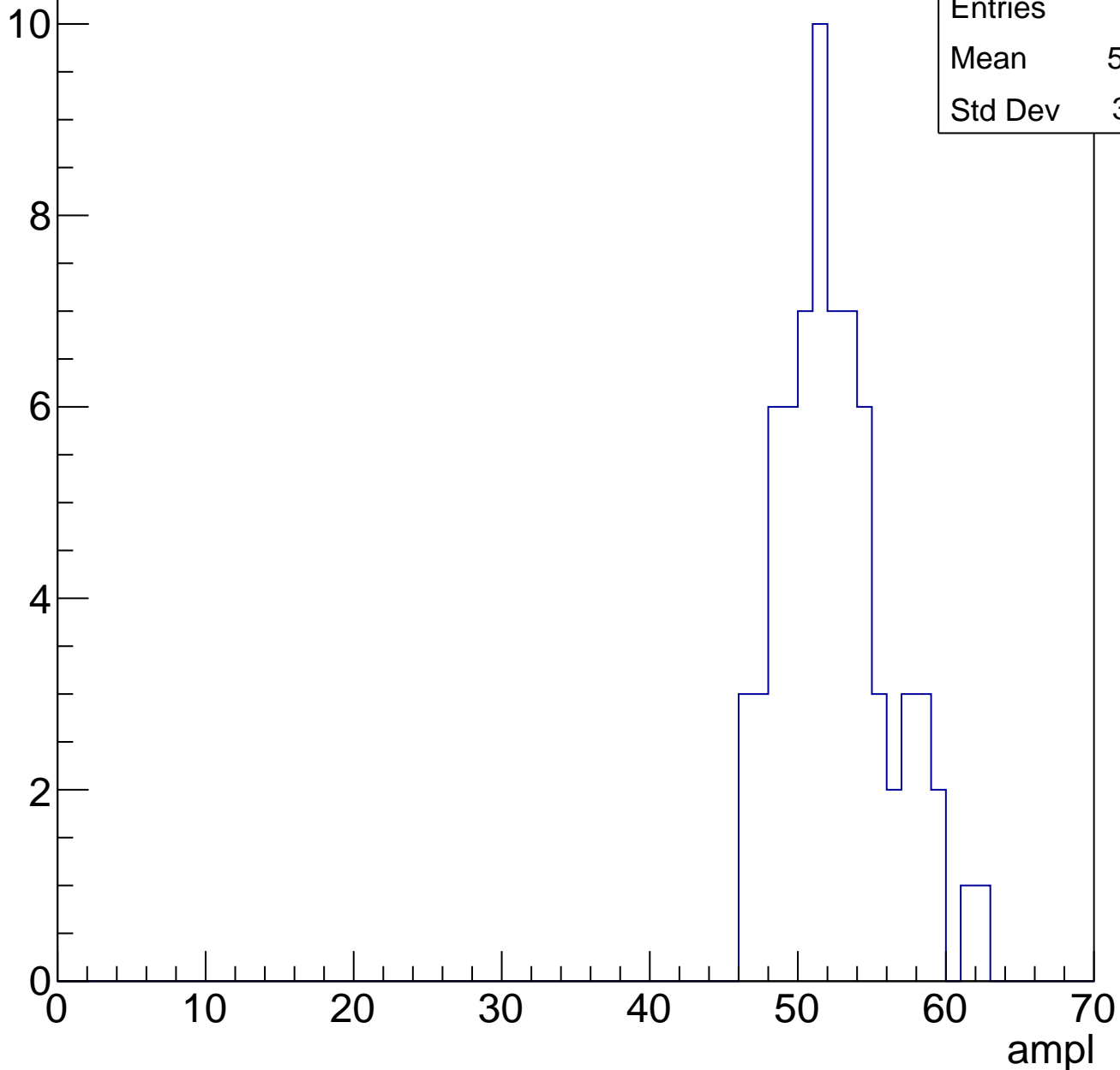


# B1L101S, U22-ch97, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	70
Mean	52.04
Std Dev	3.631

Entry

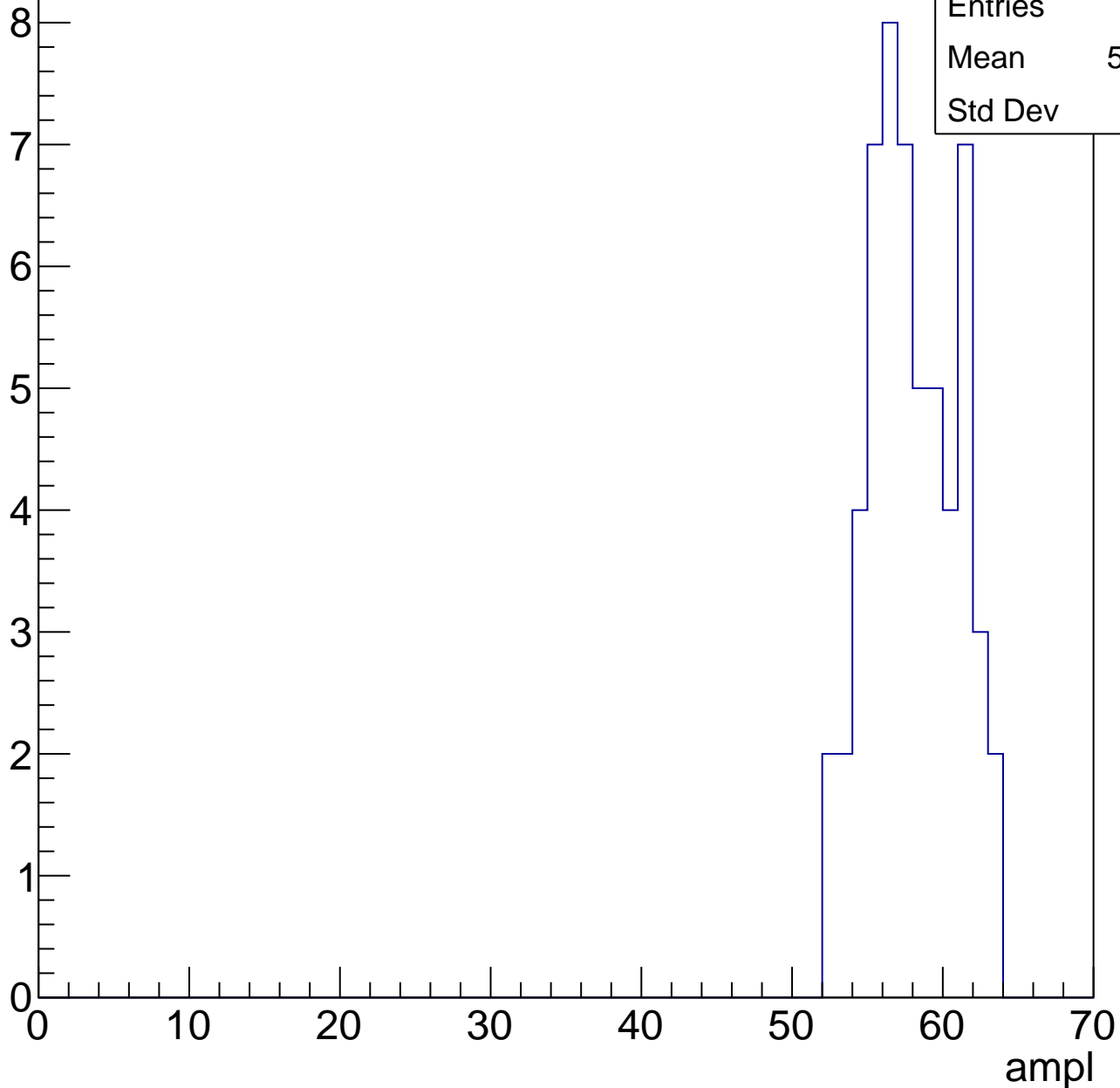


# B1L101S, U22-ch97, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	56
Mean	57.54
Std Dev	2.86

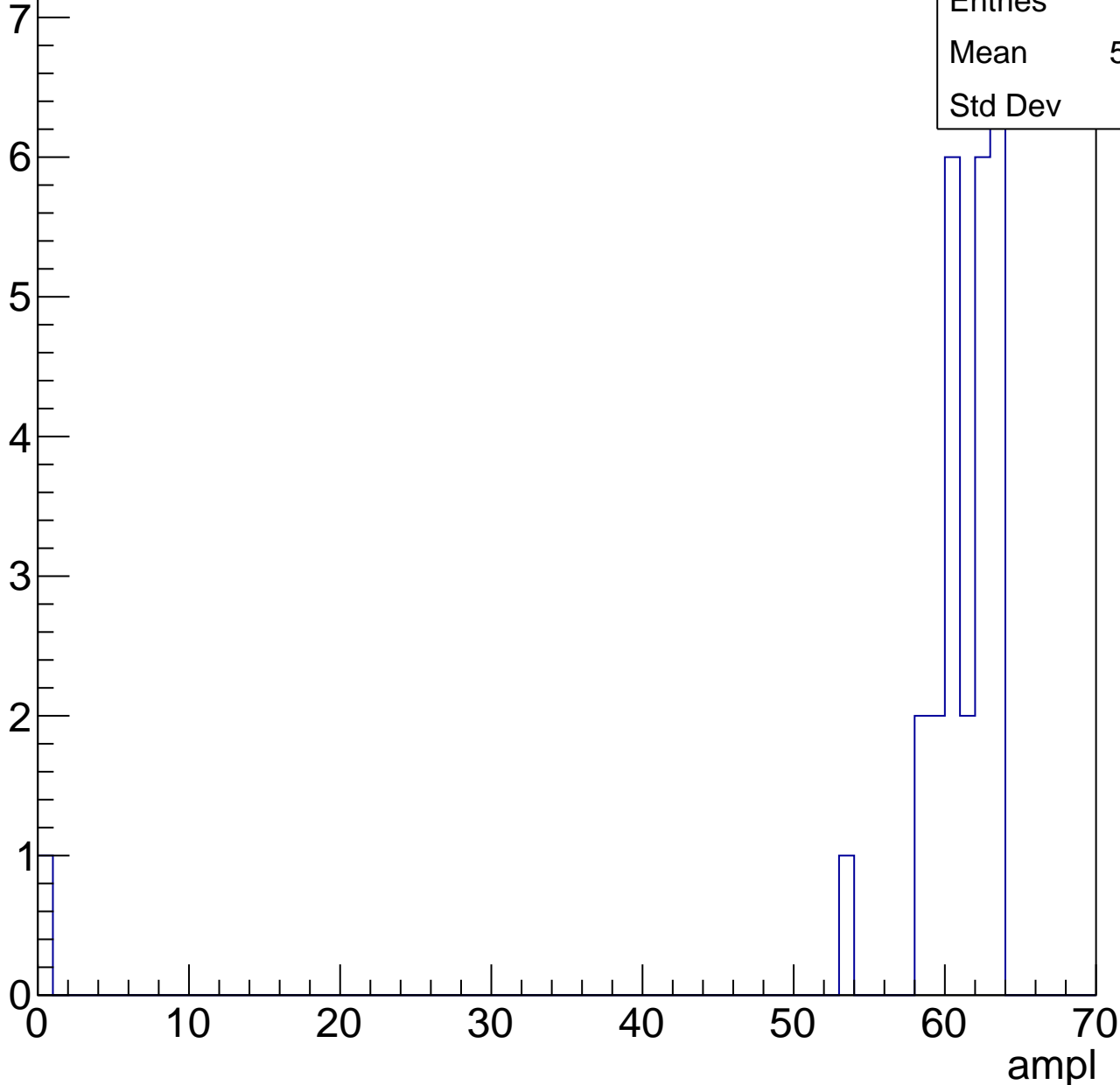


# B1L101S, U22-ch97, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	27
Mean	58.59
Std Dev	11.7



# B1L101S, U22-ch97, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

1

0.8

0.6

0.4

0.2

0

0

10

20

30

40

50

60

70

ampl

Entries

2

Mean

61

Std Dev

2



# B1L101S, U22-ch97, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U22-ch98, adc0

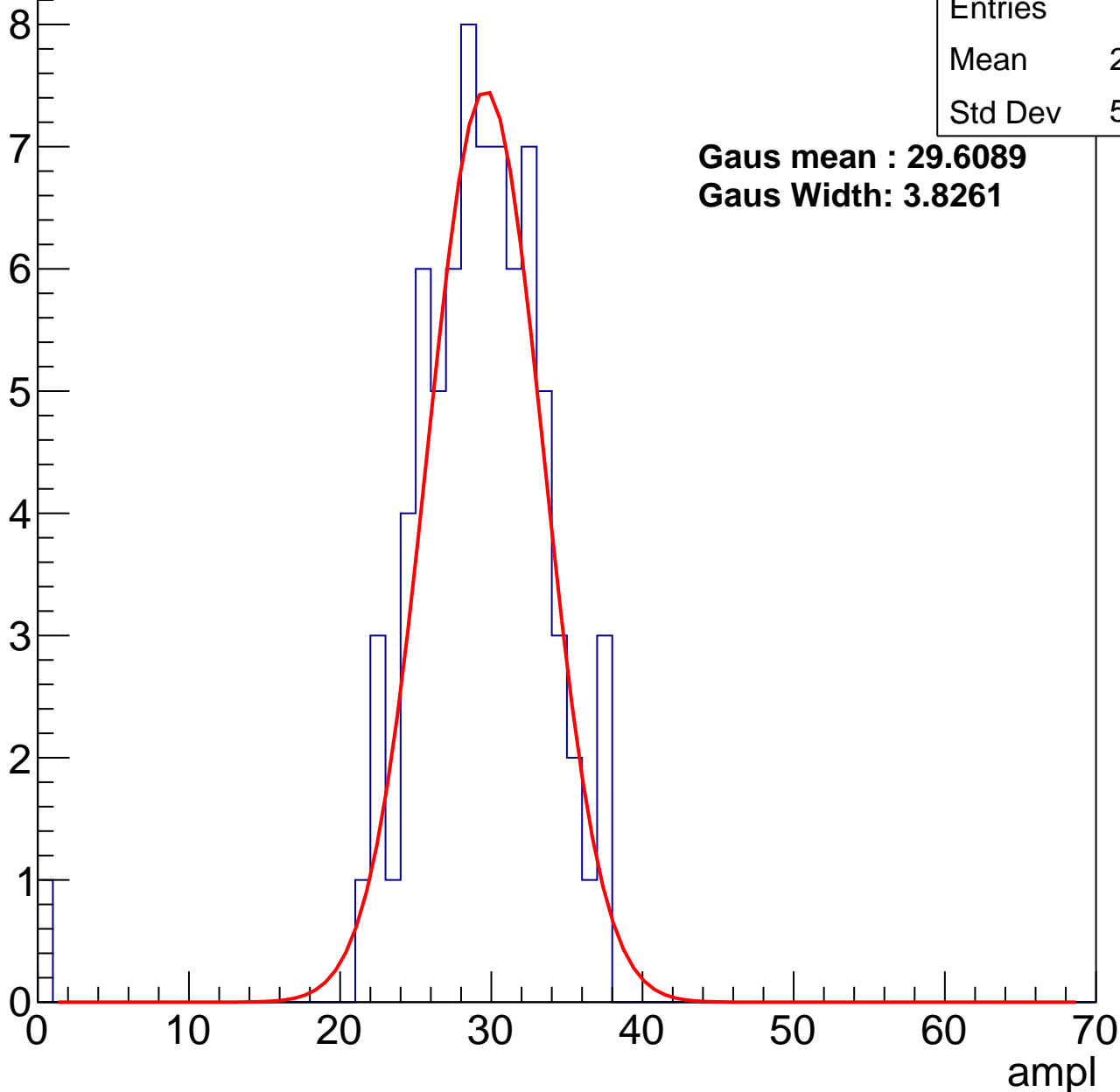
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	76
Mean	28.67
Std Dev	5.019

**Gaus mean : 29.6089**

**Gaus Width: 3.8261**



# B1L101S, U22-ch98, adc1

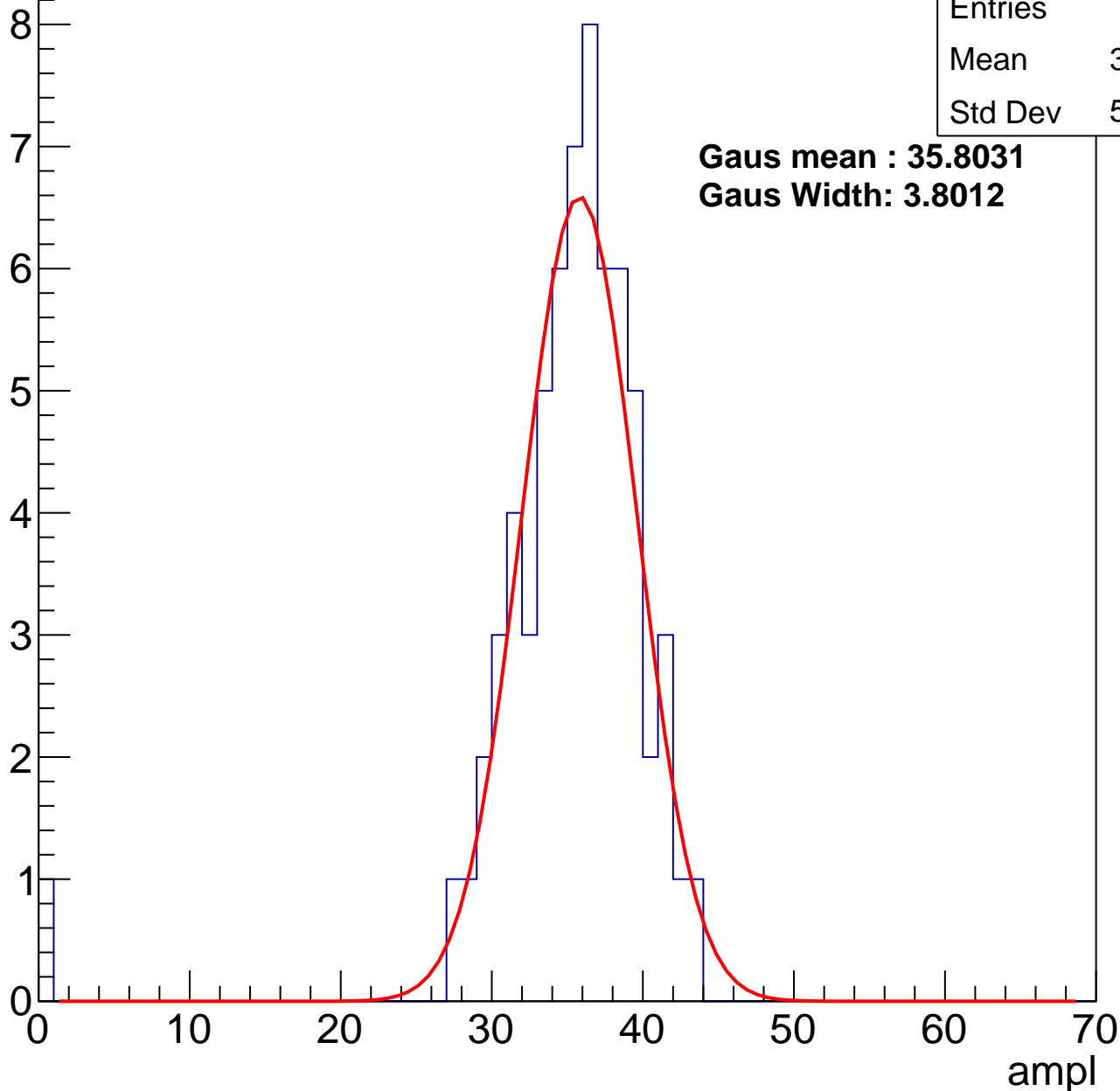
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	34.74
Std Dev	5.595

**Gaus mean : 35.8031**

**Gaus Width: 3.8012**



# B1L101S, U22-ch98, adc2

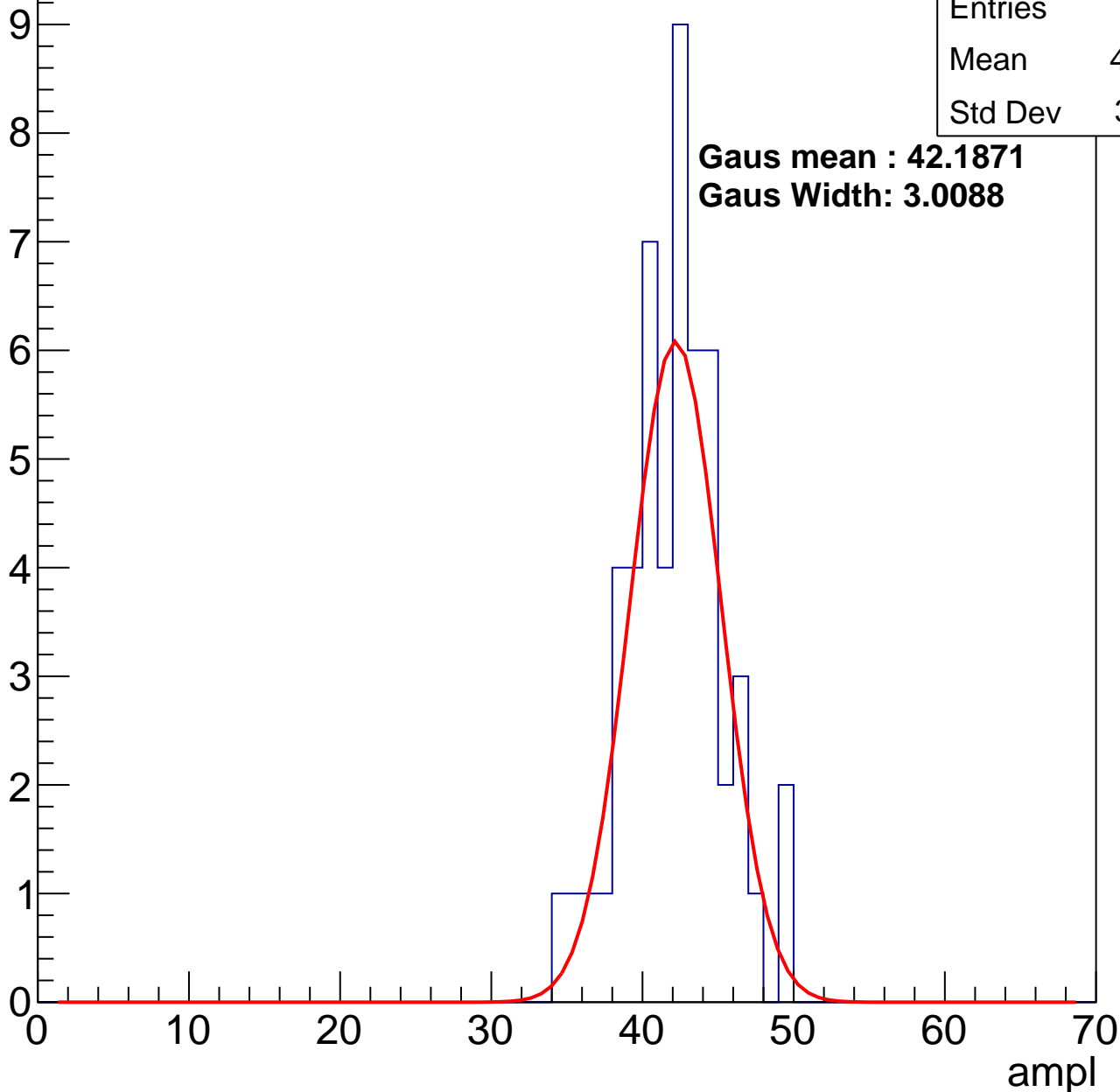
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	52
Mean	41.67
Std Dev	3.161

**Gaus mean : 42.1871**

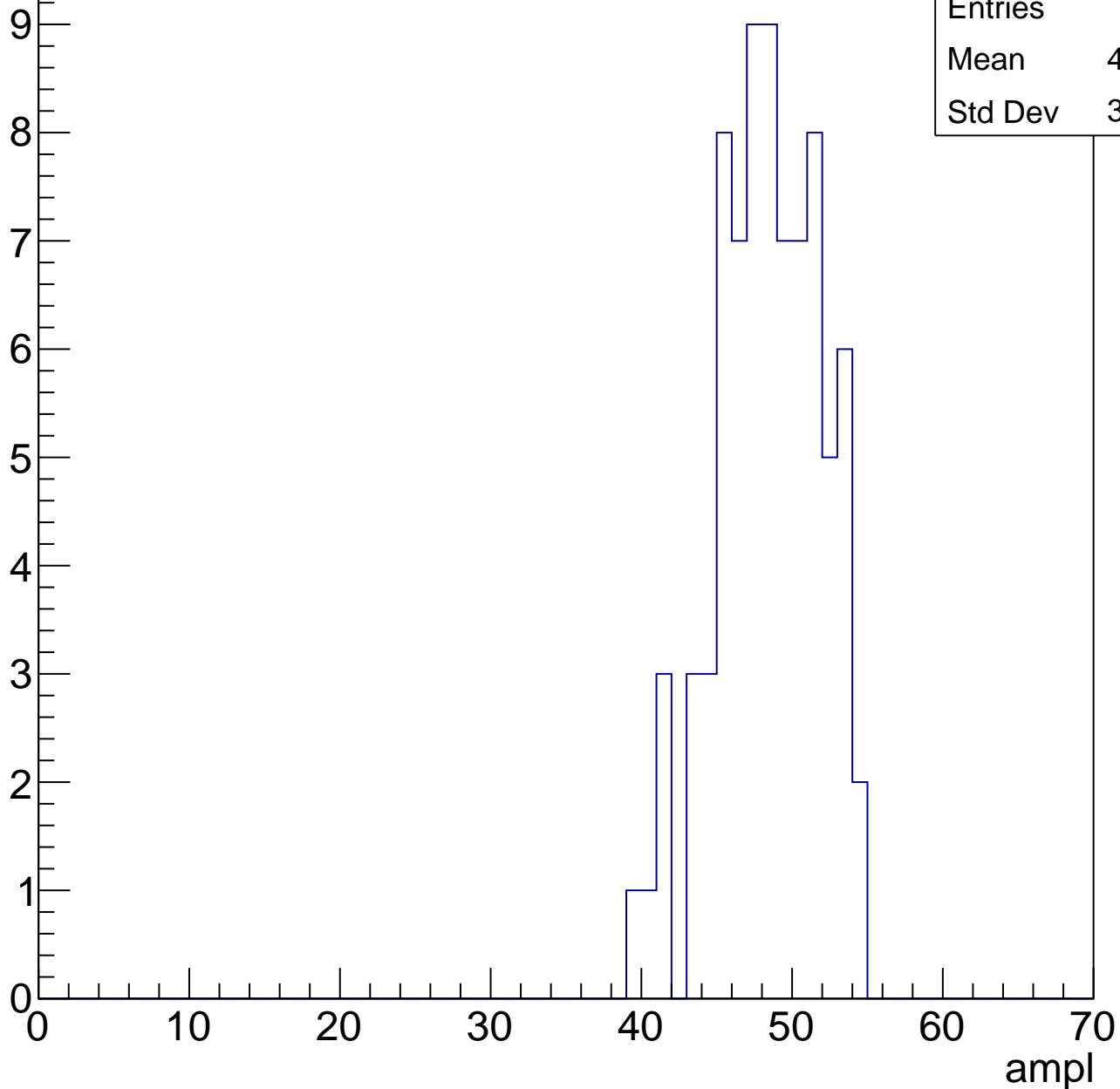
**Gaus Width: 3.0088**



# B1L101S, U22-ch98, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

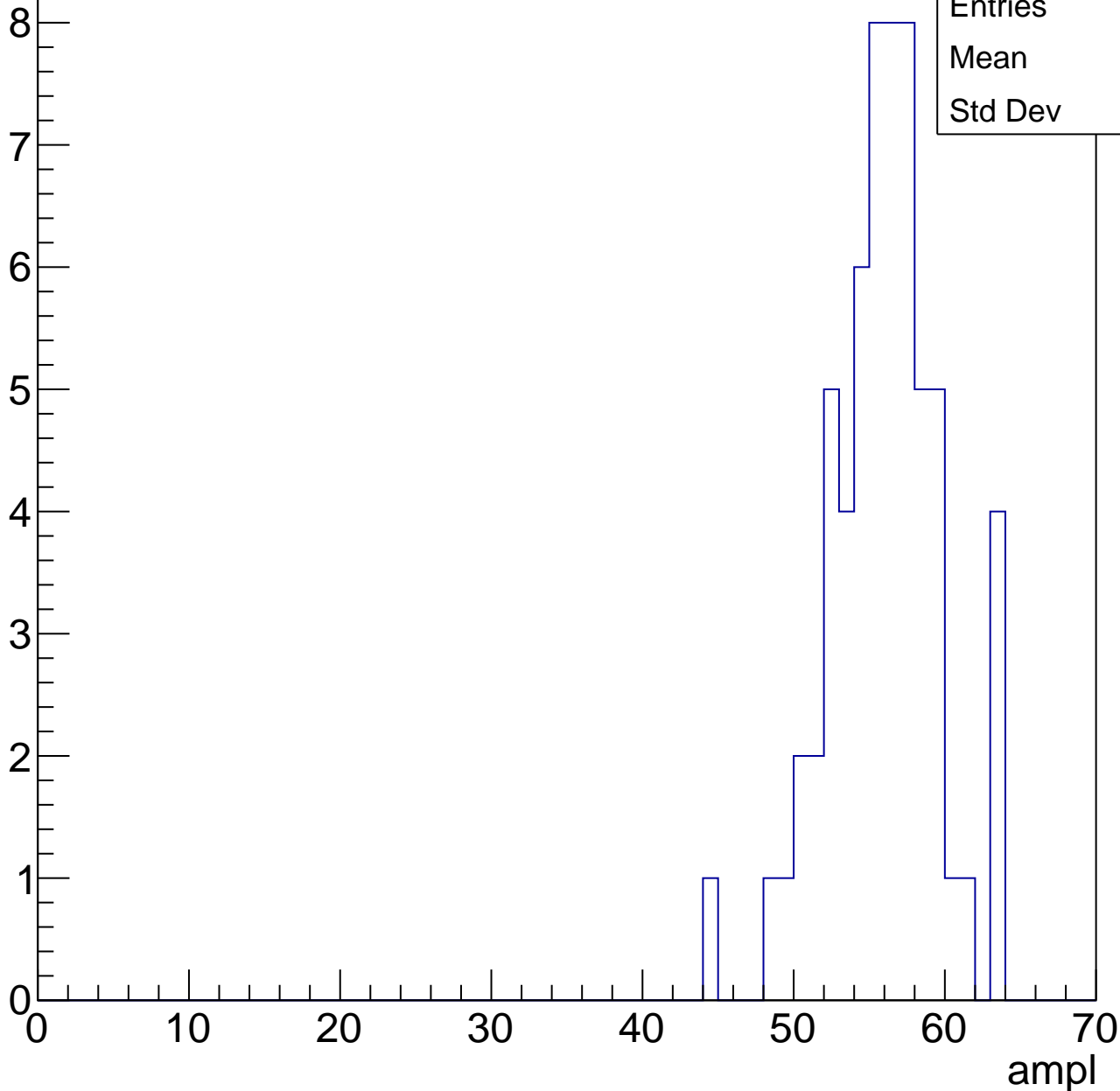


# B1L101S, U22-ch98, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

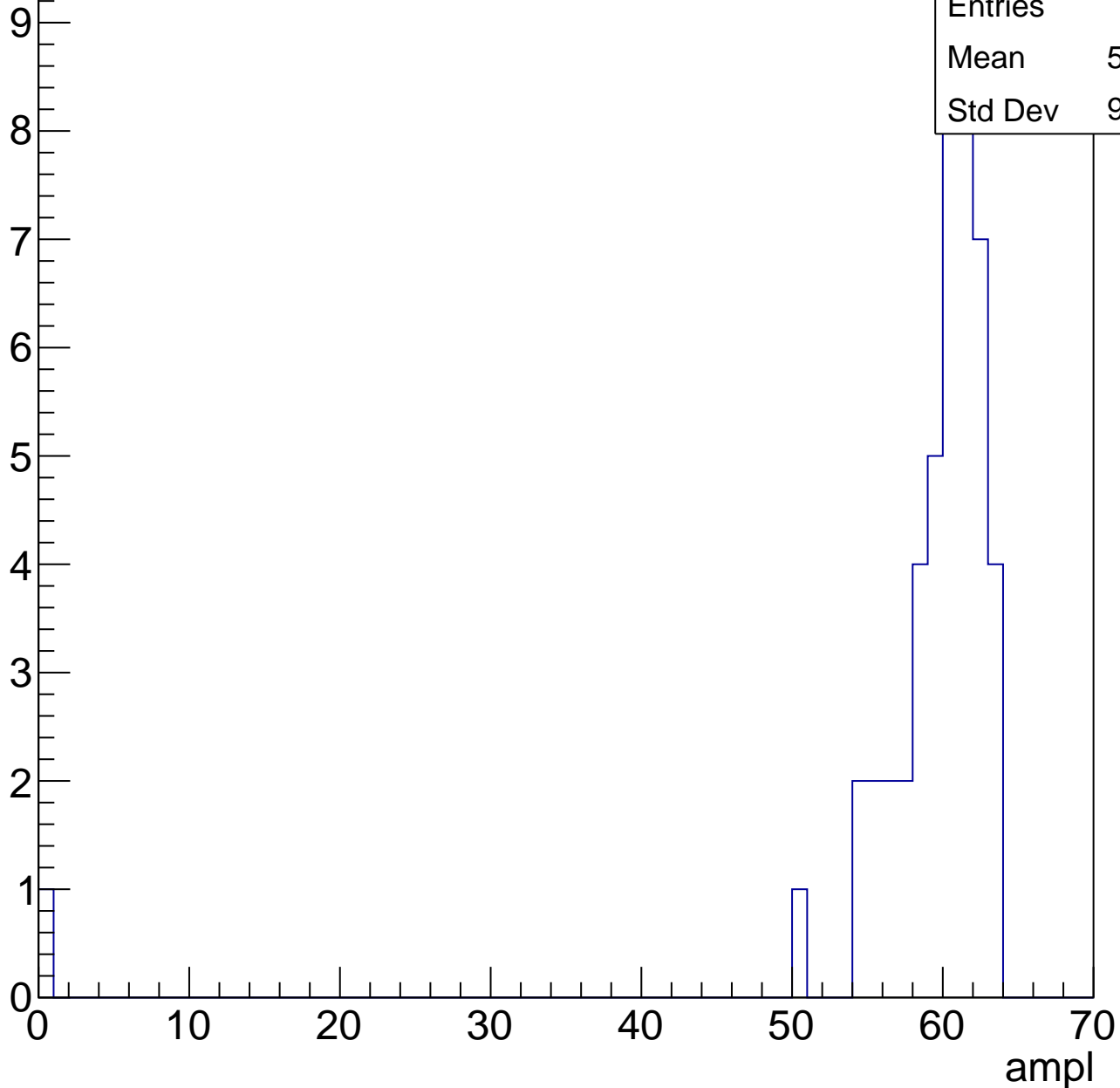
Entries	62
Mean	55.5
Std Dev	3.64



# B1L101S, U22-ch98, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

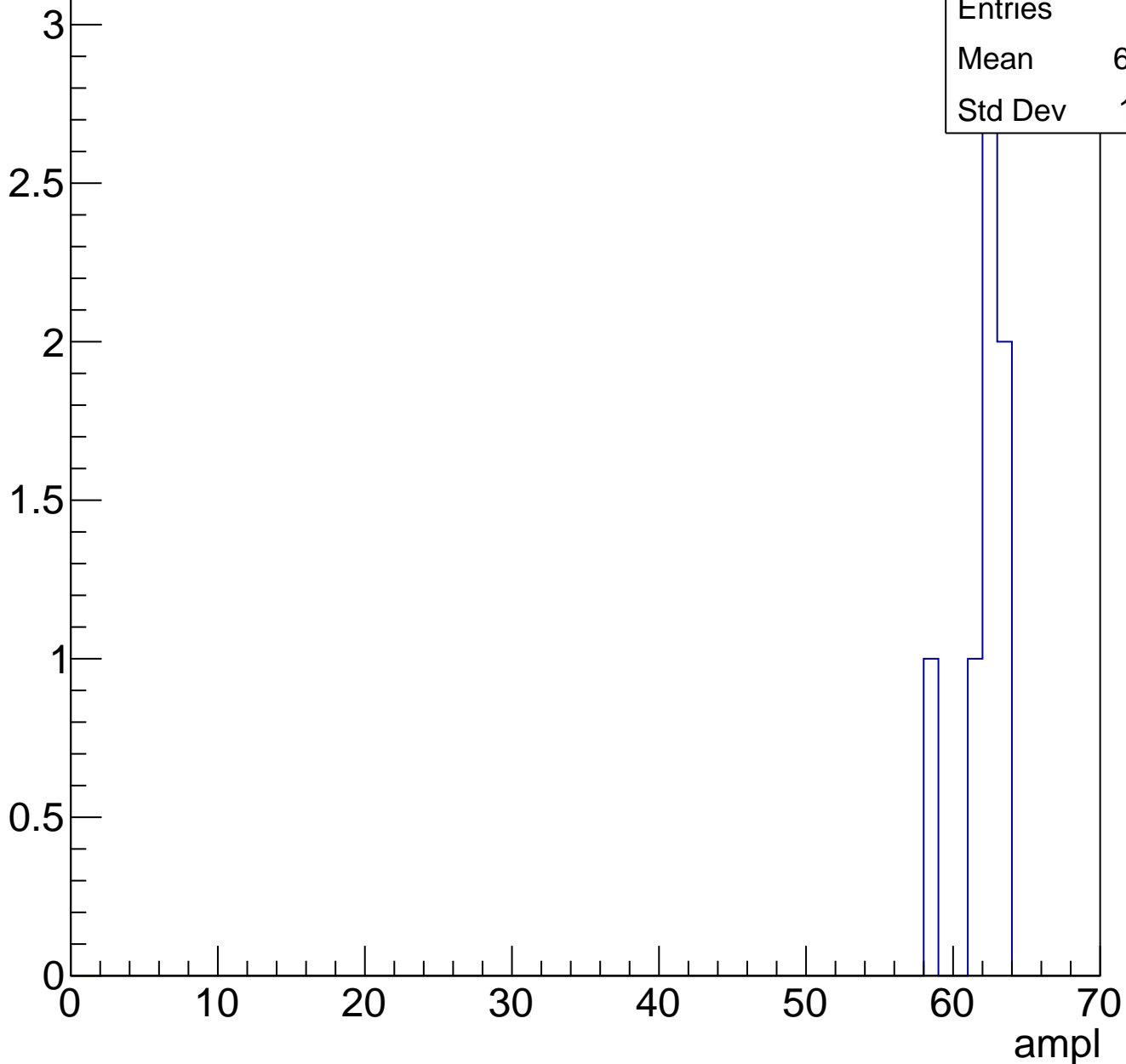
Entry



# B1L101S, U22-ch98, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U22-ch98, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U22-ch99, adc0

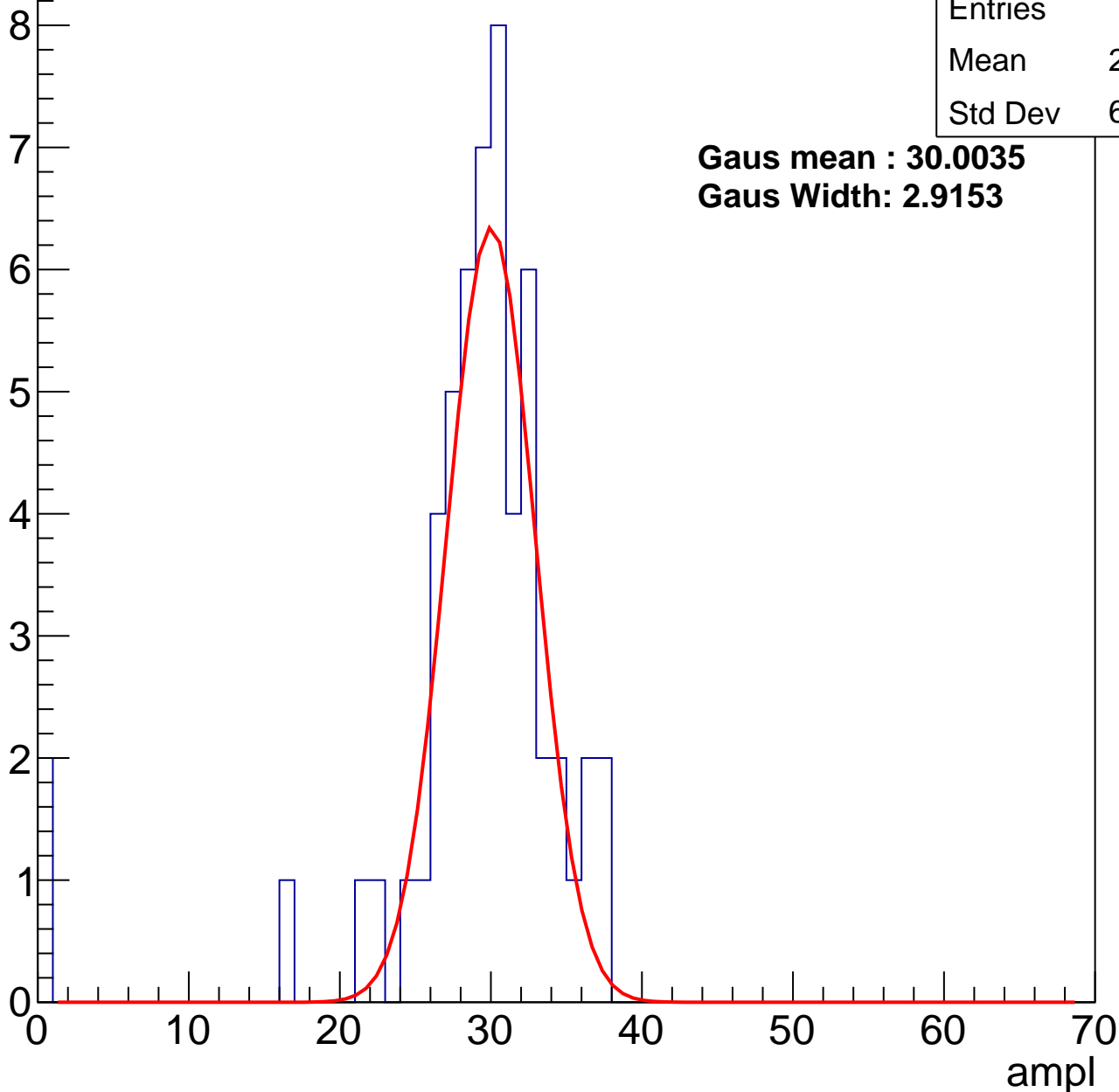
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	56
Mean	28.38
Std Dev	6.637

**Gaus mean : 30.0035**

**Gaus Width: 2.9153**



# B1L101S, U22-ch99, adc1

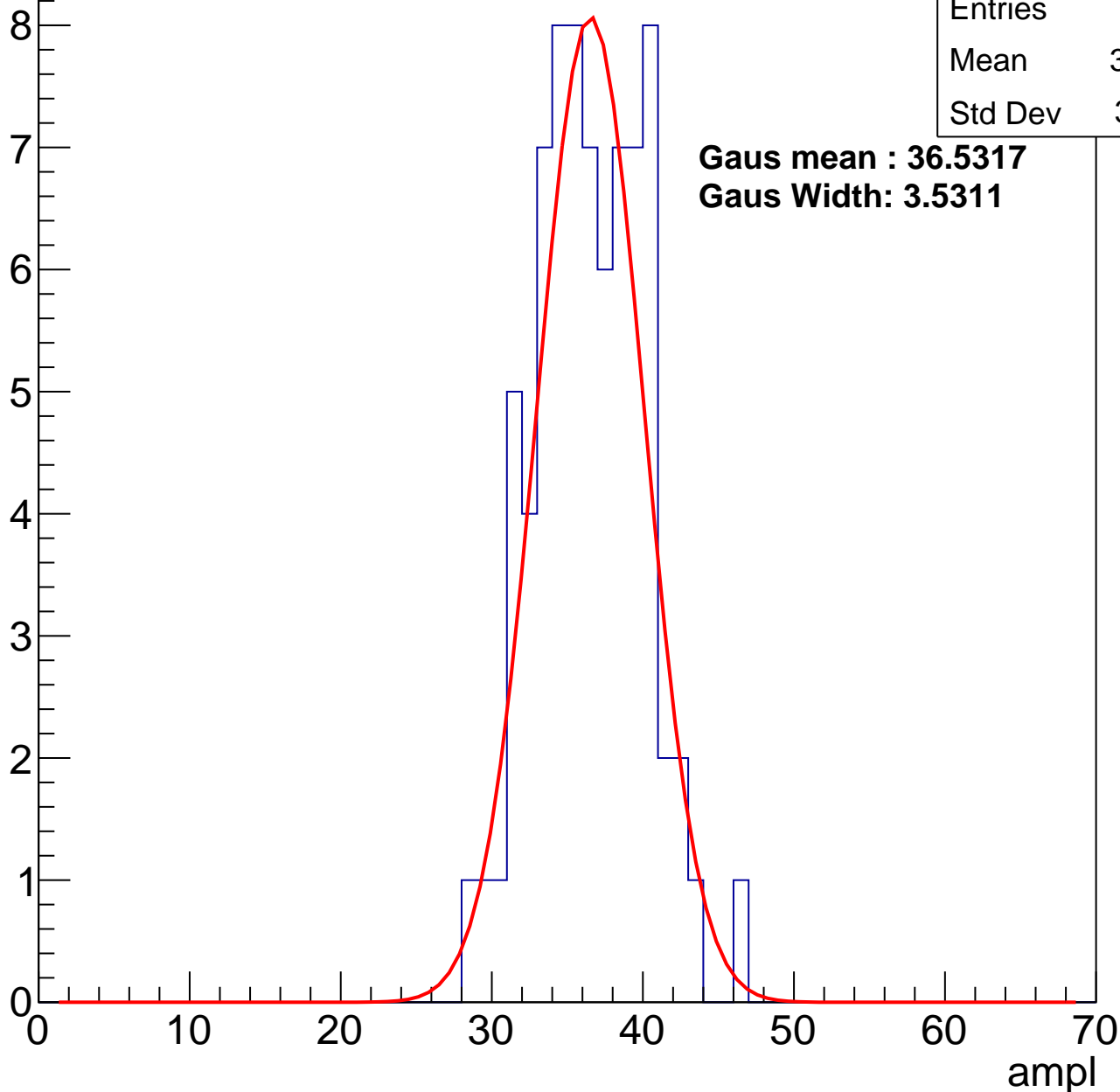
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	76
Mean	36.07
Std Dev	3.511

**Gaus mean : 36.5317**

**Gaus Width: 3.5311**



# B1L101S, U22-ch99, adc2

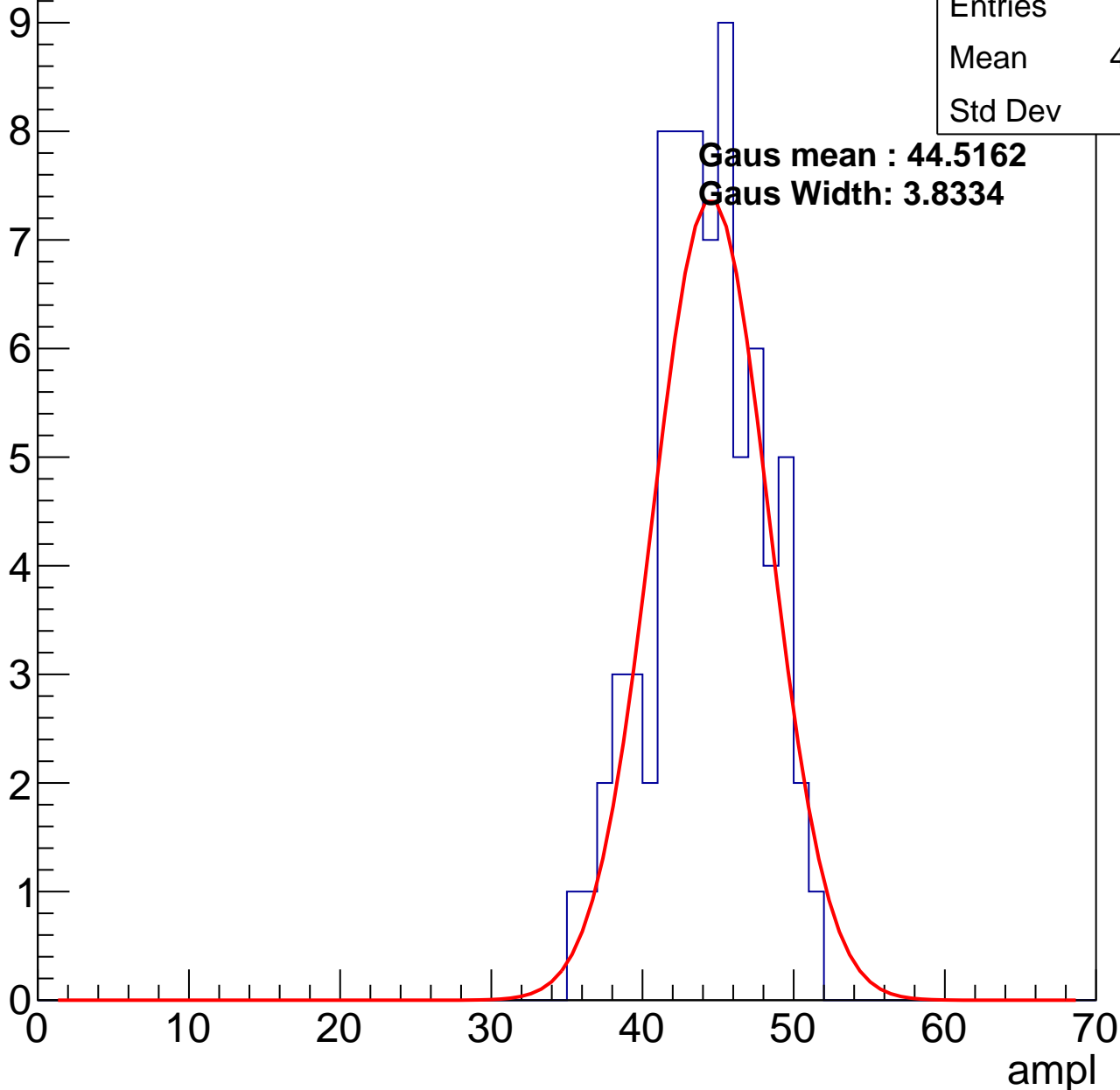
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	75
Mean	43.69
Std Dev	3.57

**Gaus mean : 44.5162**

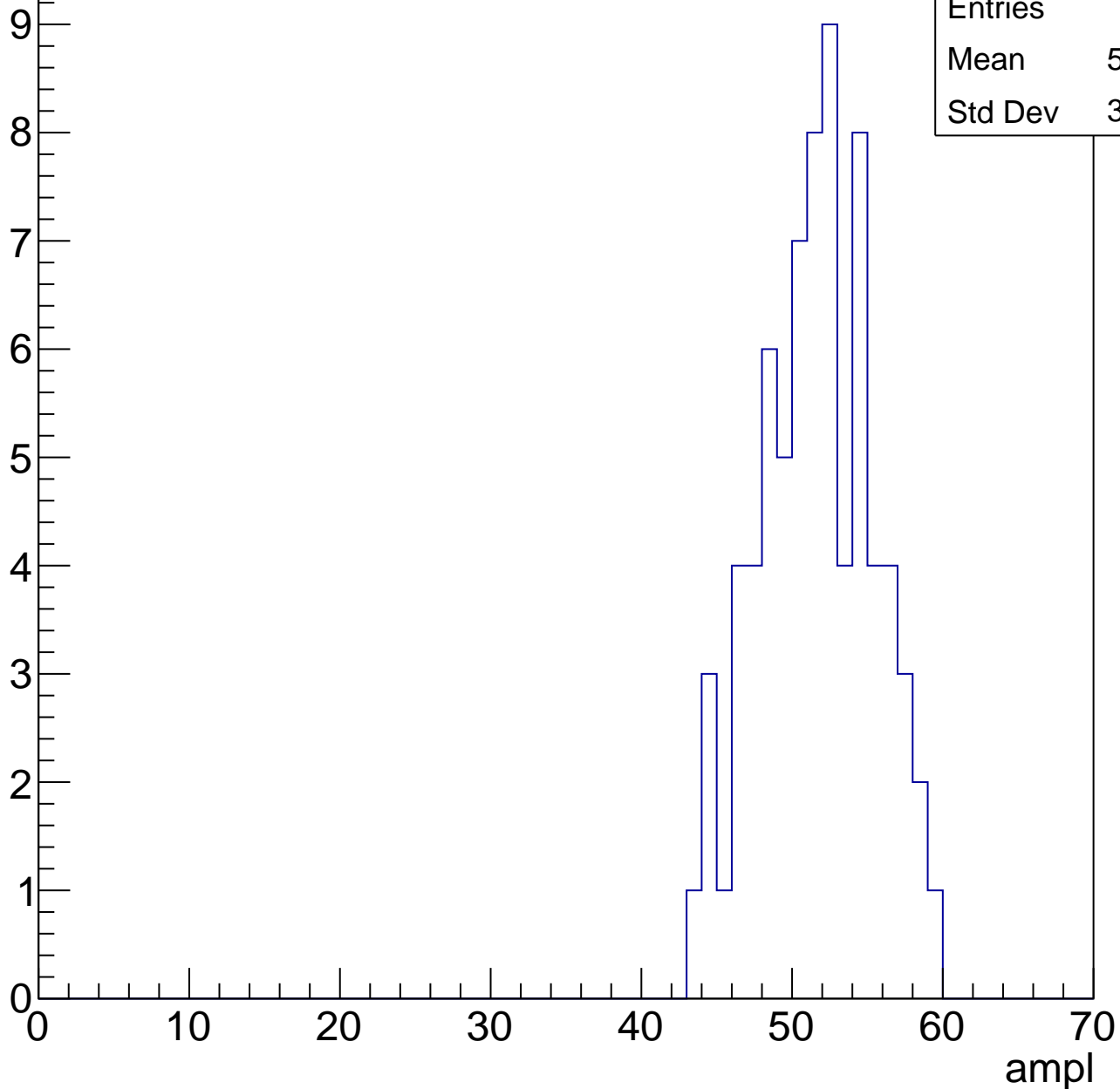
**Gaus Width: 3.8334**



# B1L101S, U22-ch99, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

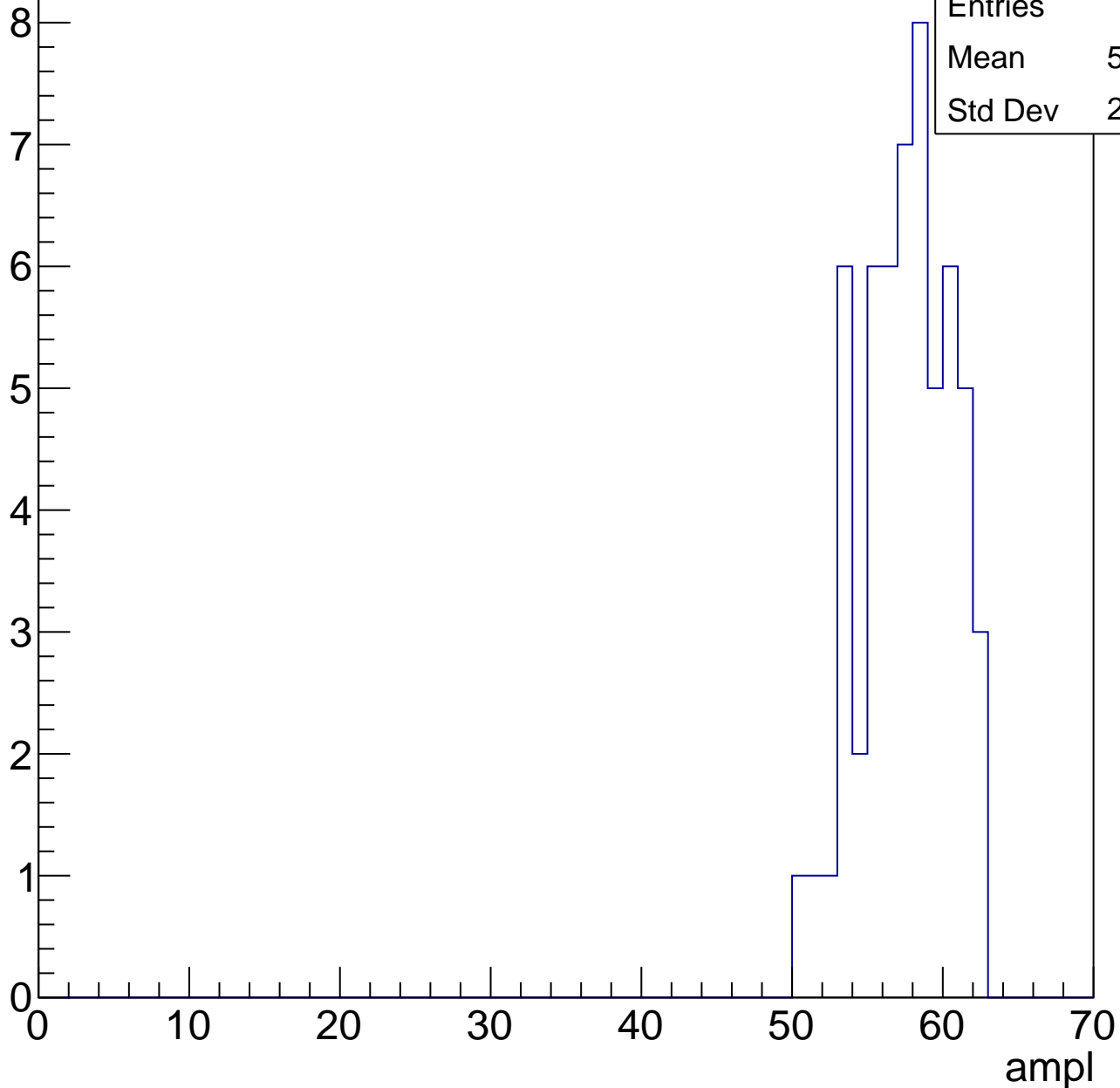
Entry



# B1L101S, U22-ch99, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



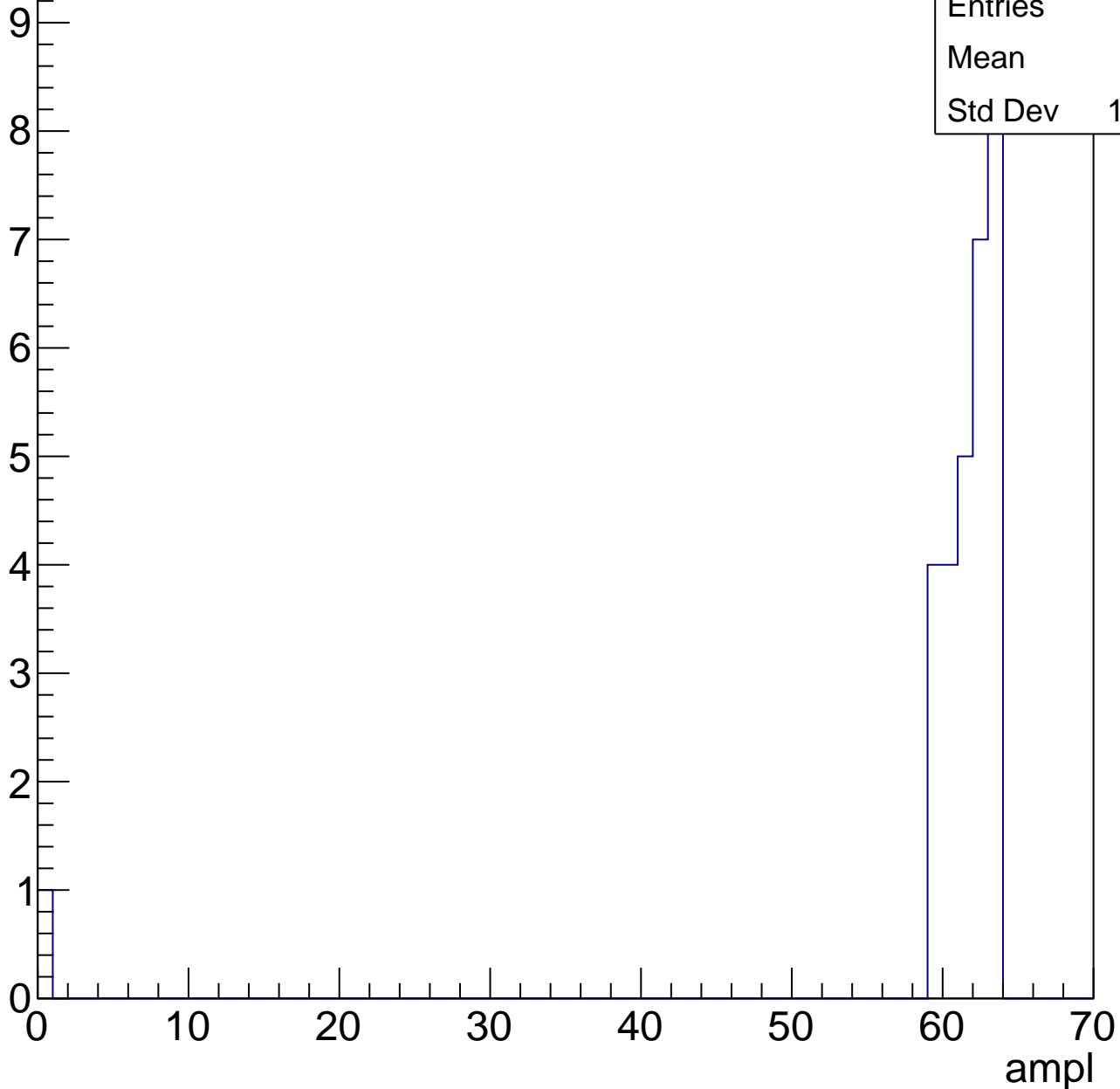
Entries	57
Mean	57.09
Std Dev	2.934

# B1L101S, U22-ch99, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	30
Mean	59.4
Std Dev	11.12



# B1L101S, U22-ch99, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	63
Std Dev	0



# B1L101S, U22-ch99, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L101S, U22-ch100, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	61
Mean	29.95
Std Dev	2.651

**Gaus mean : 30.3008**

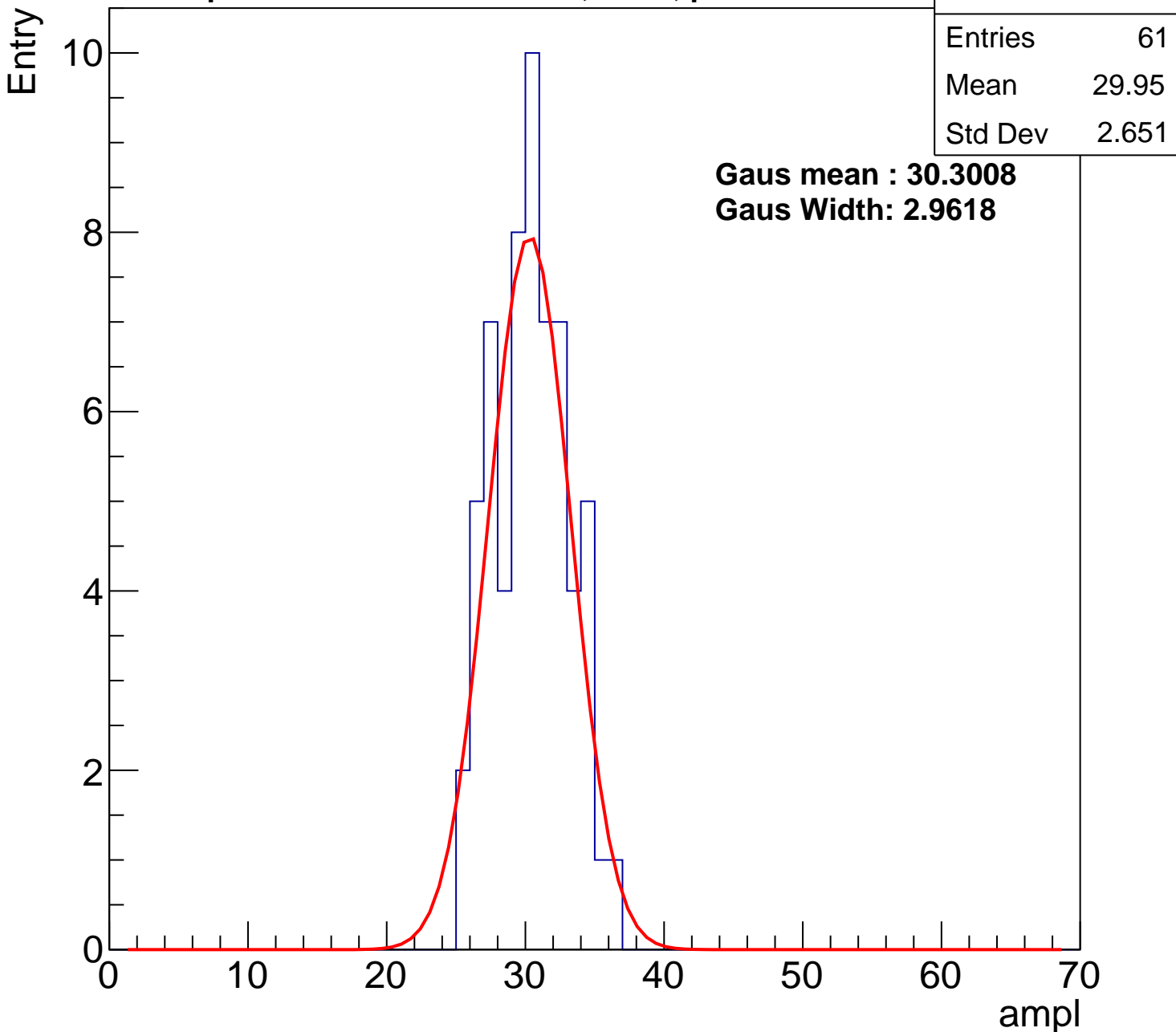
**Gaus Width: 2.9618**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U22-ch100, adc1

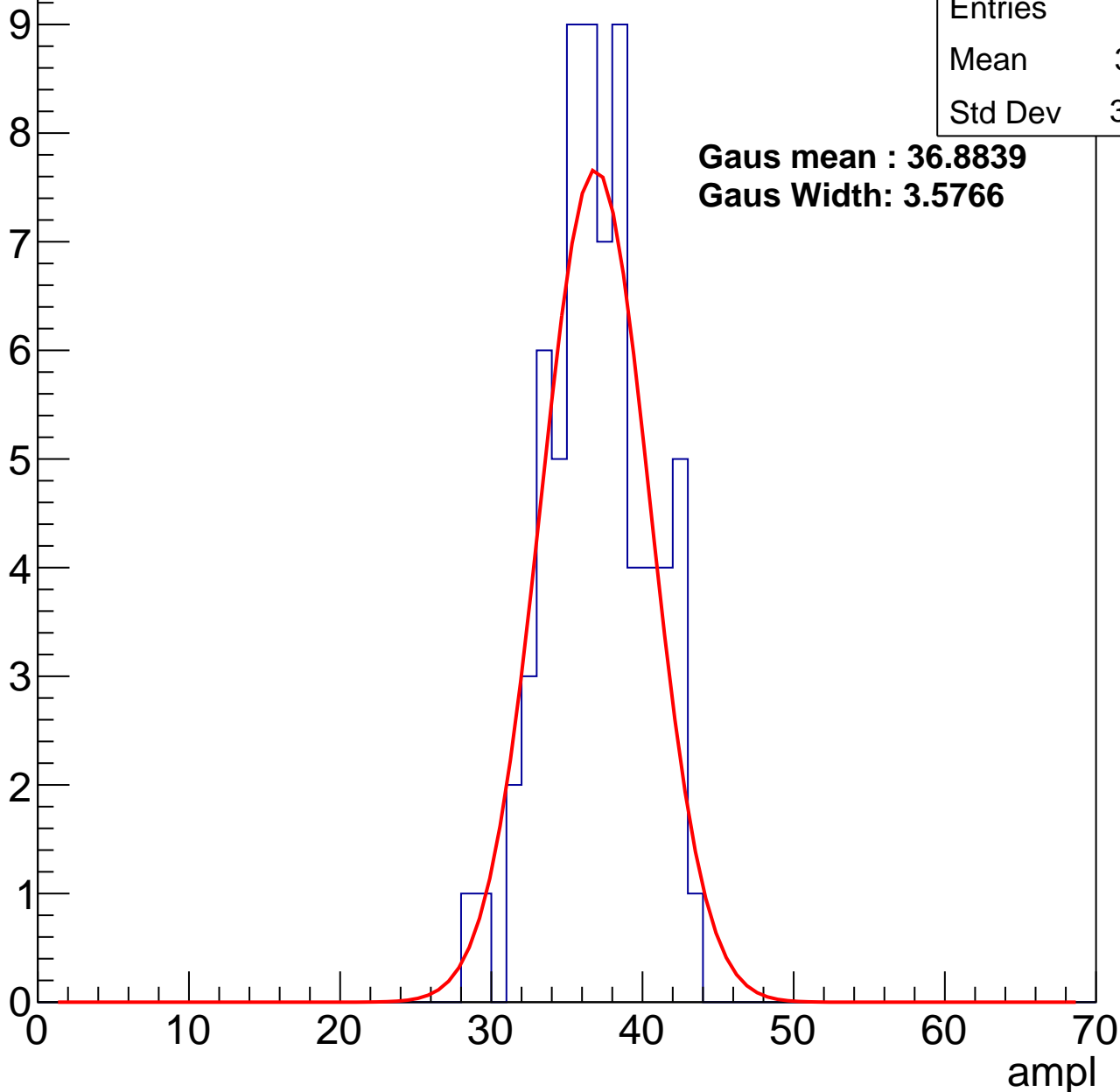
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	36.51
Std Dev	3.268

**Gaus mean : 36.8839**

**Gaus Width: 3.5766**



# B1L101S, U22-ch100, adc2

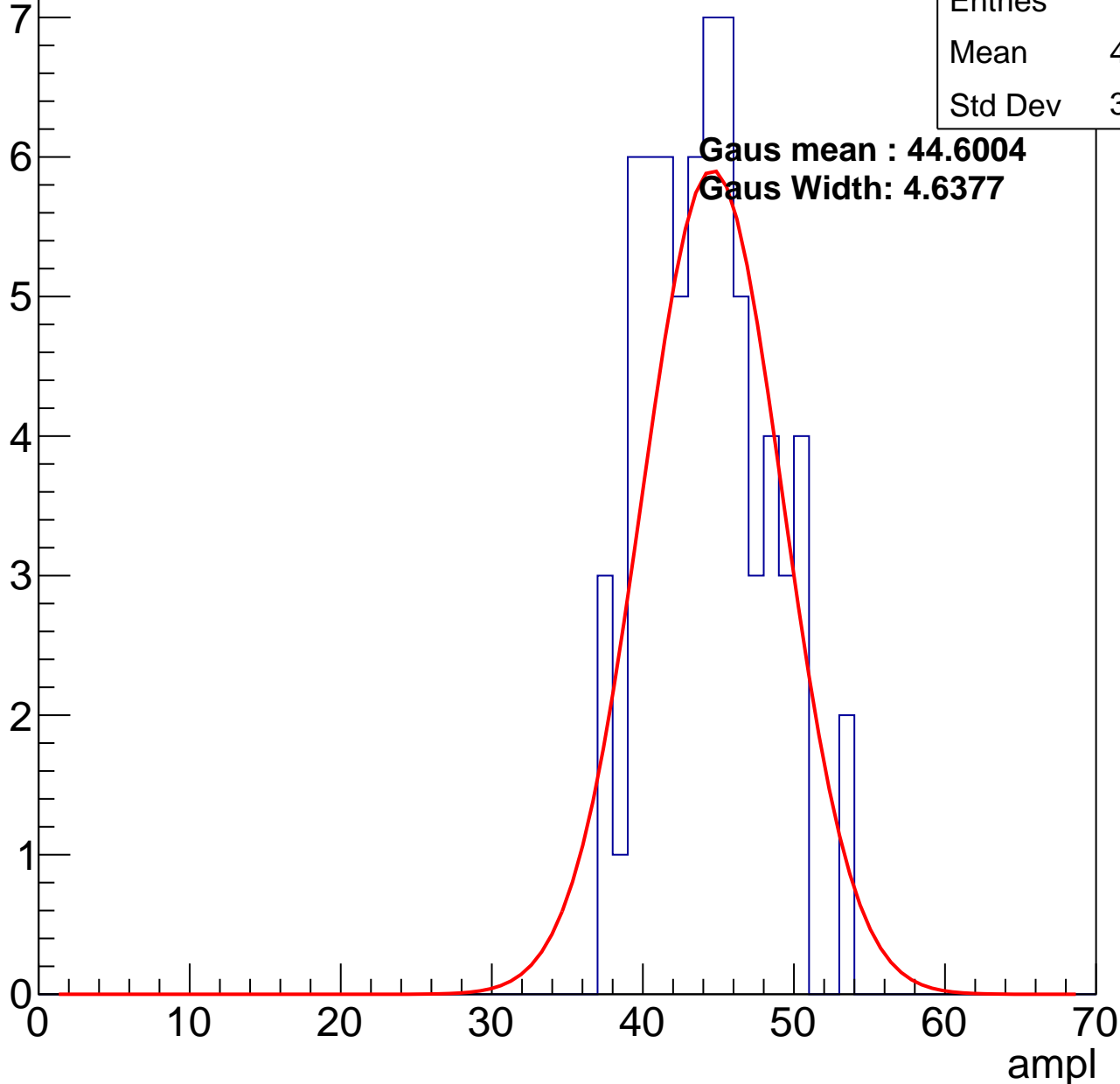
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	43.76
Std Dev	3.843

**Gaus mean : 44.6004**

**Gaus Width: 4.6377**

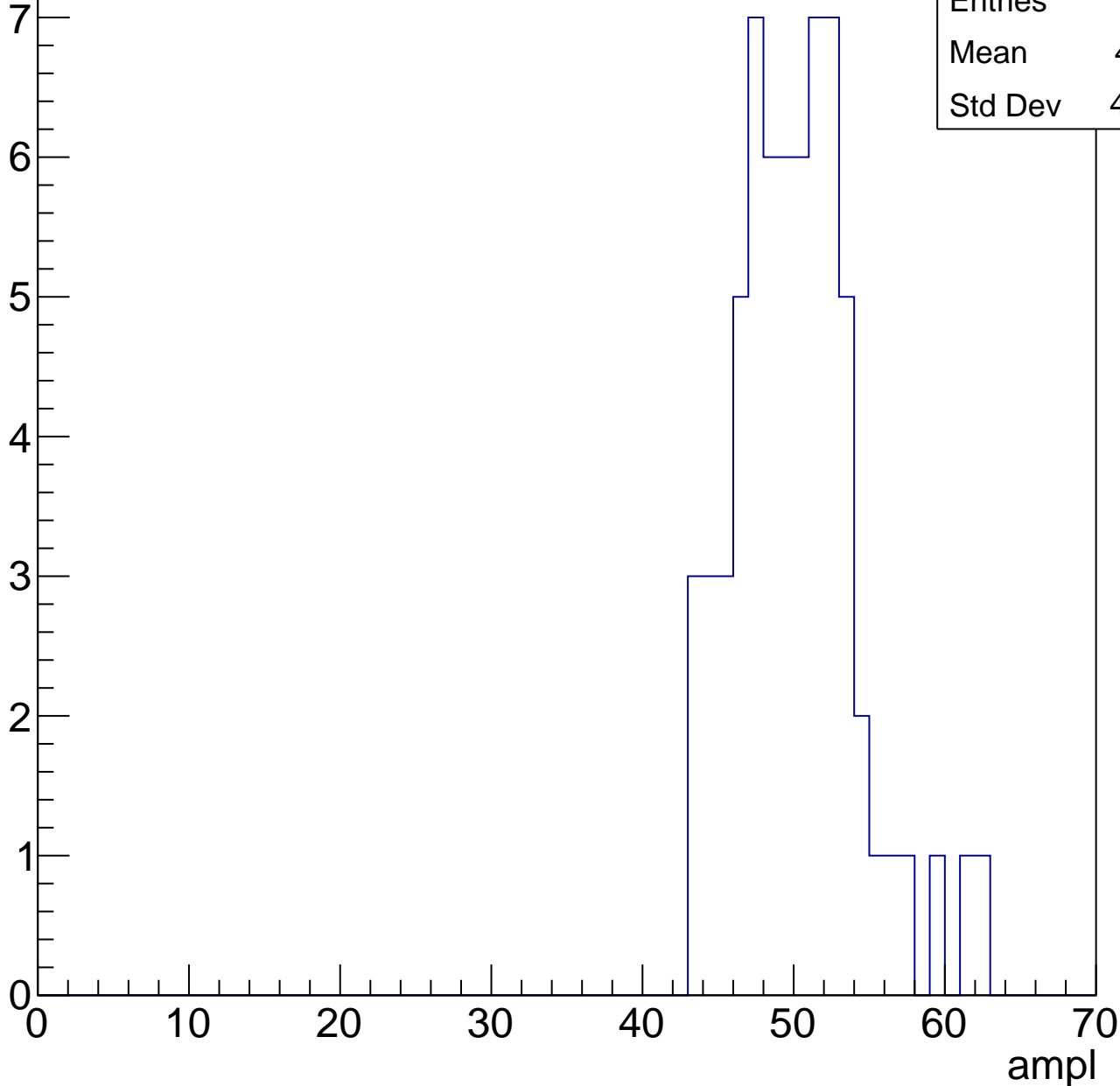


# B1L101S, U22-ch100, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	66
Mean	49.71
Std Dev	4.018

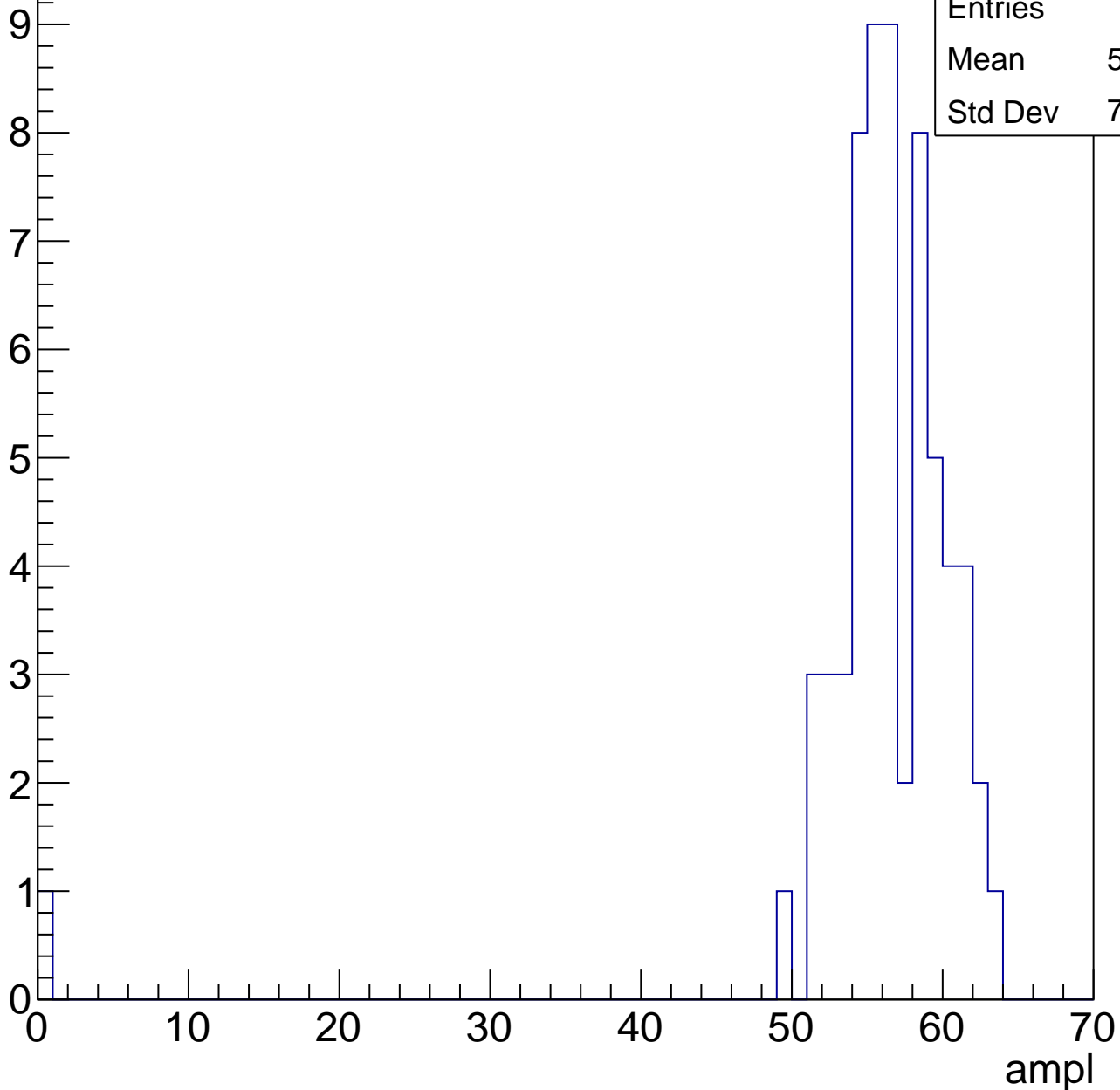


# B1L101S, U22-ch100, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	55.43
Std Dev	7.684

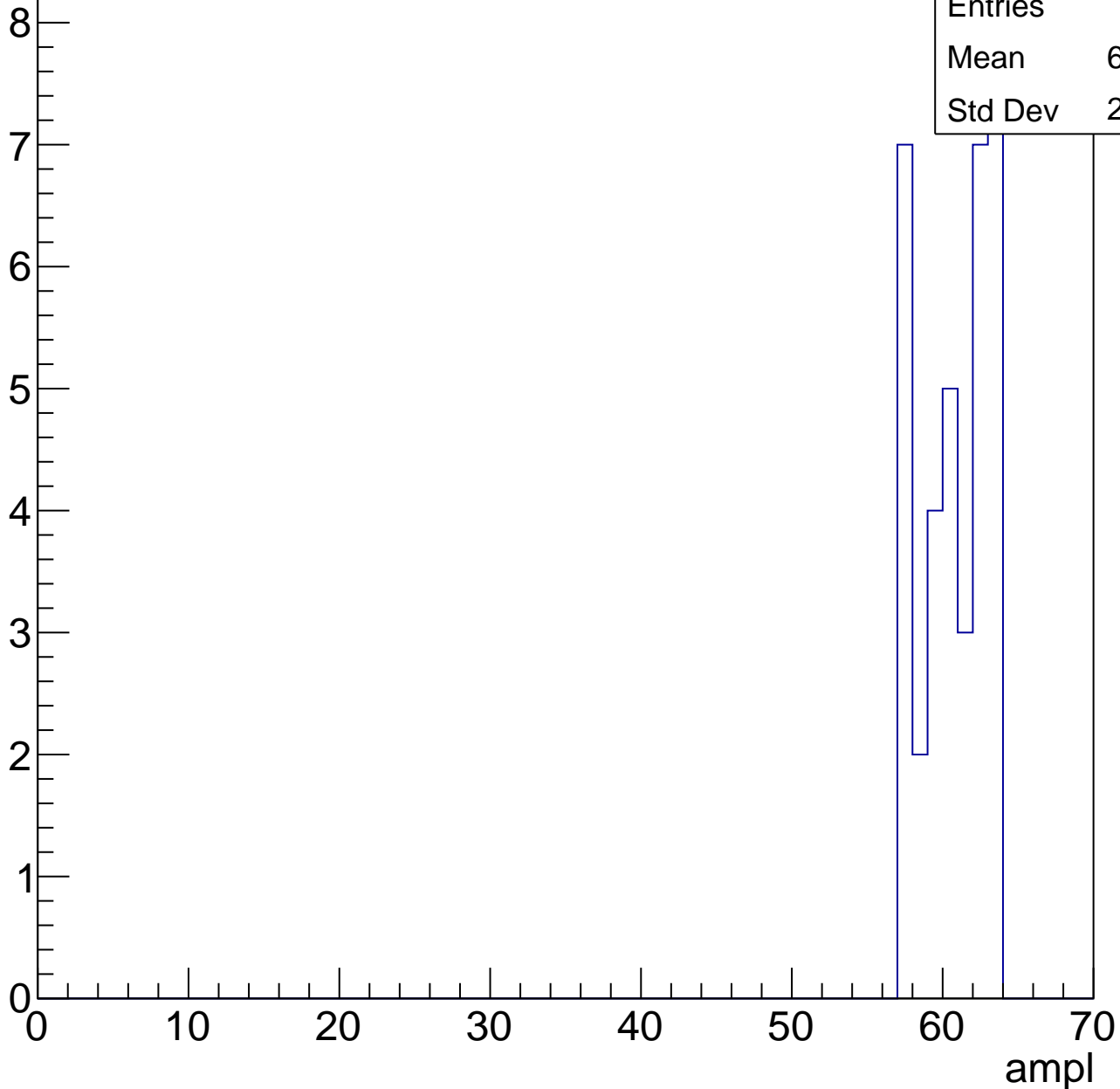


# B1L101S, U22-ch100, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

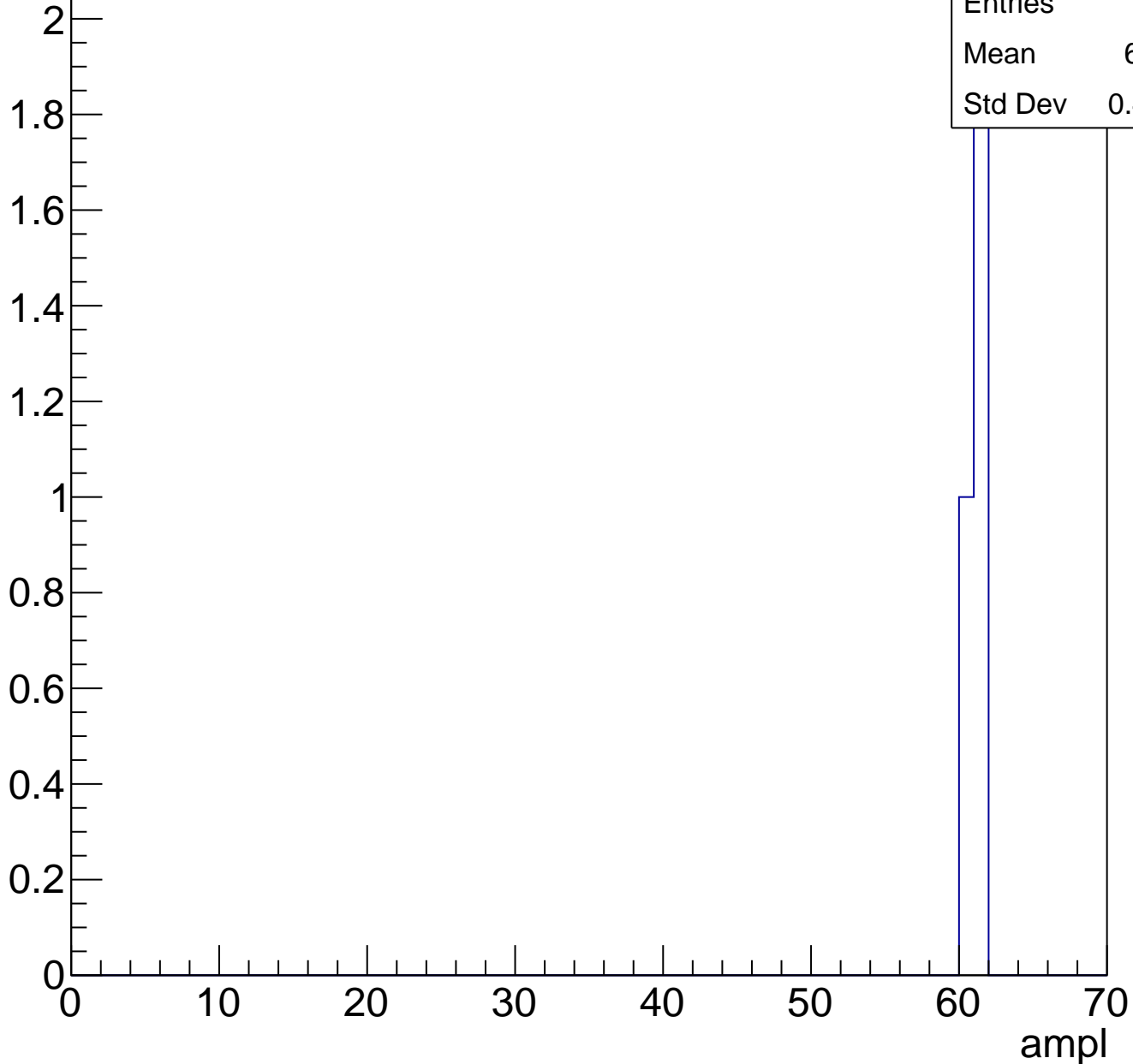
Entries	36
Mean	60.33
Std Dev	2.198



# B1L101S, U22-ch100, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	3
Mean	60.67
Std Dev	0.4714



# B1L101S, U22-ch100, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U22-ch101, adc0

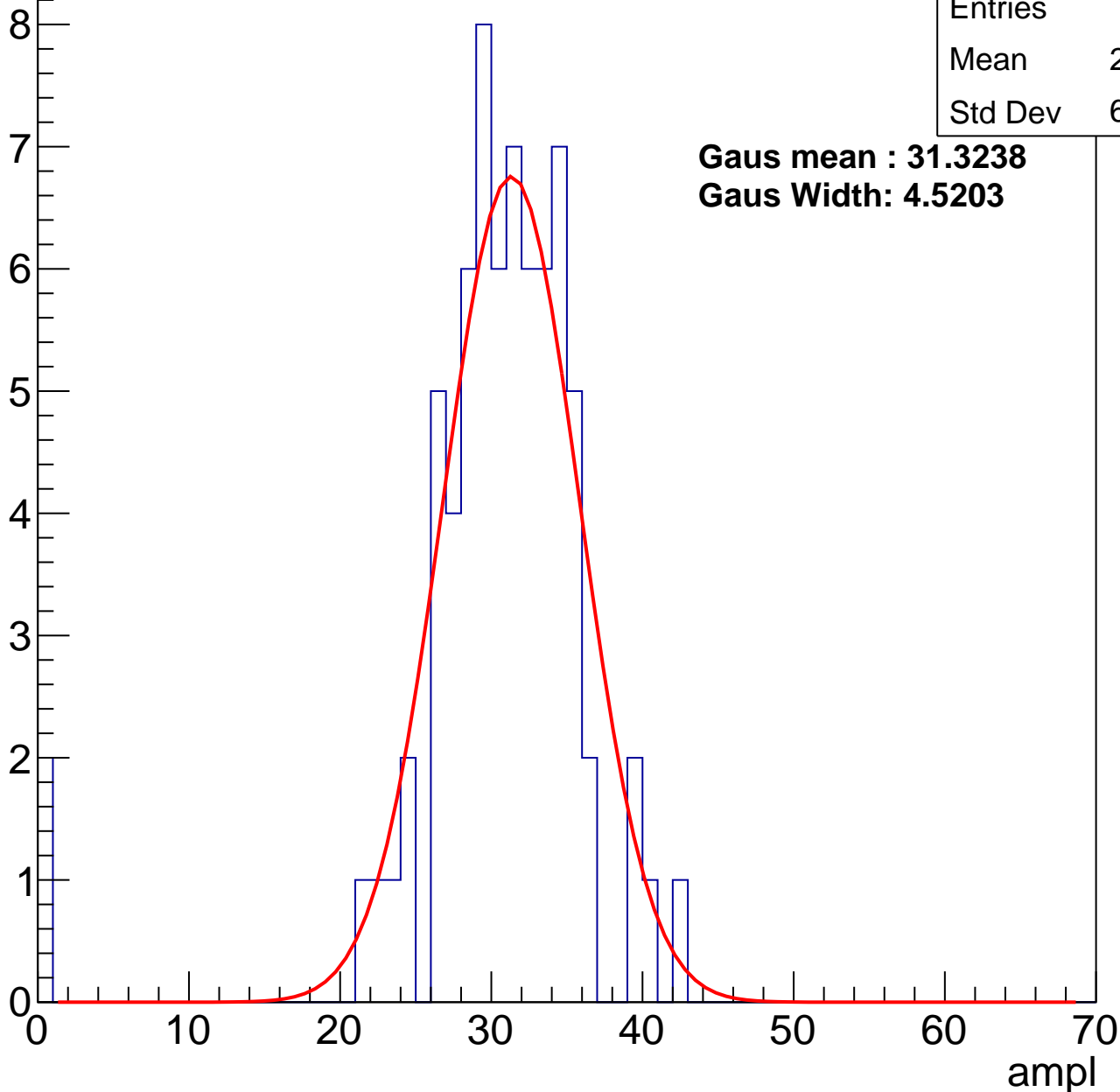
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	73
Mean	29.92
Std Dev	6.425

**Gaus mean : 31.3238**

**Gaus Width: 4.5203**



# B1L101S, U22-ch101, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	65
Mean	37.28
Std Dev	3.431

**Gaus mean : 37.9751**

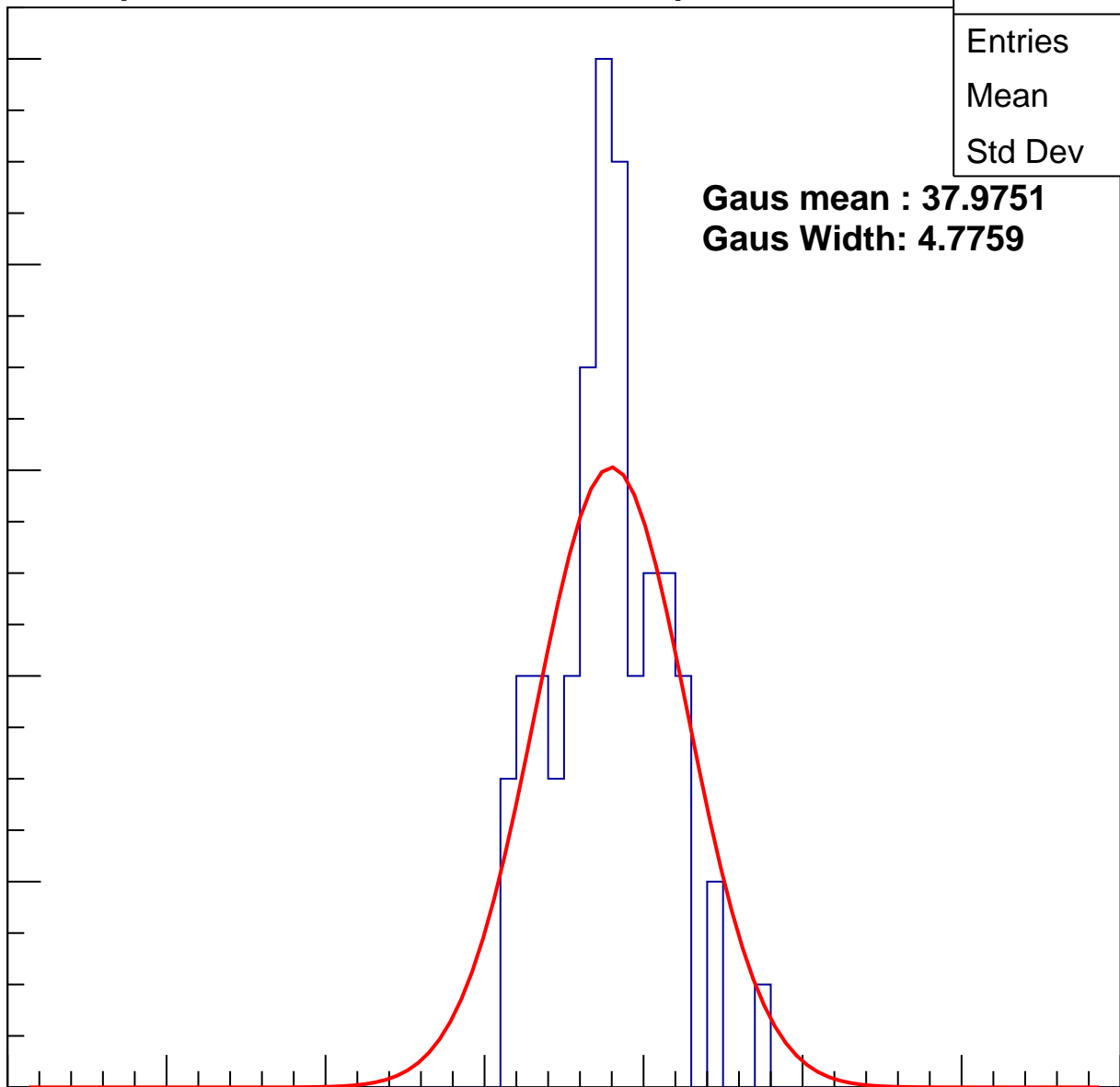
**Gaus Width: 4.7759**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B1L101S, U22-ch101, adc2

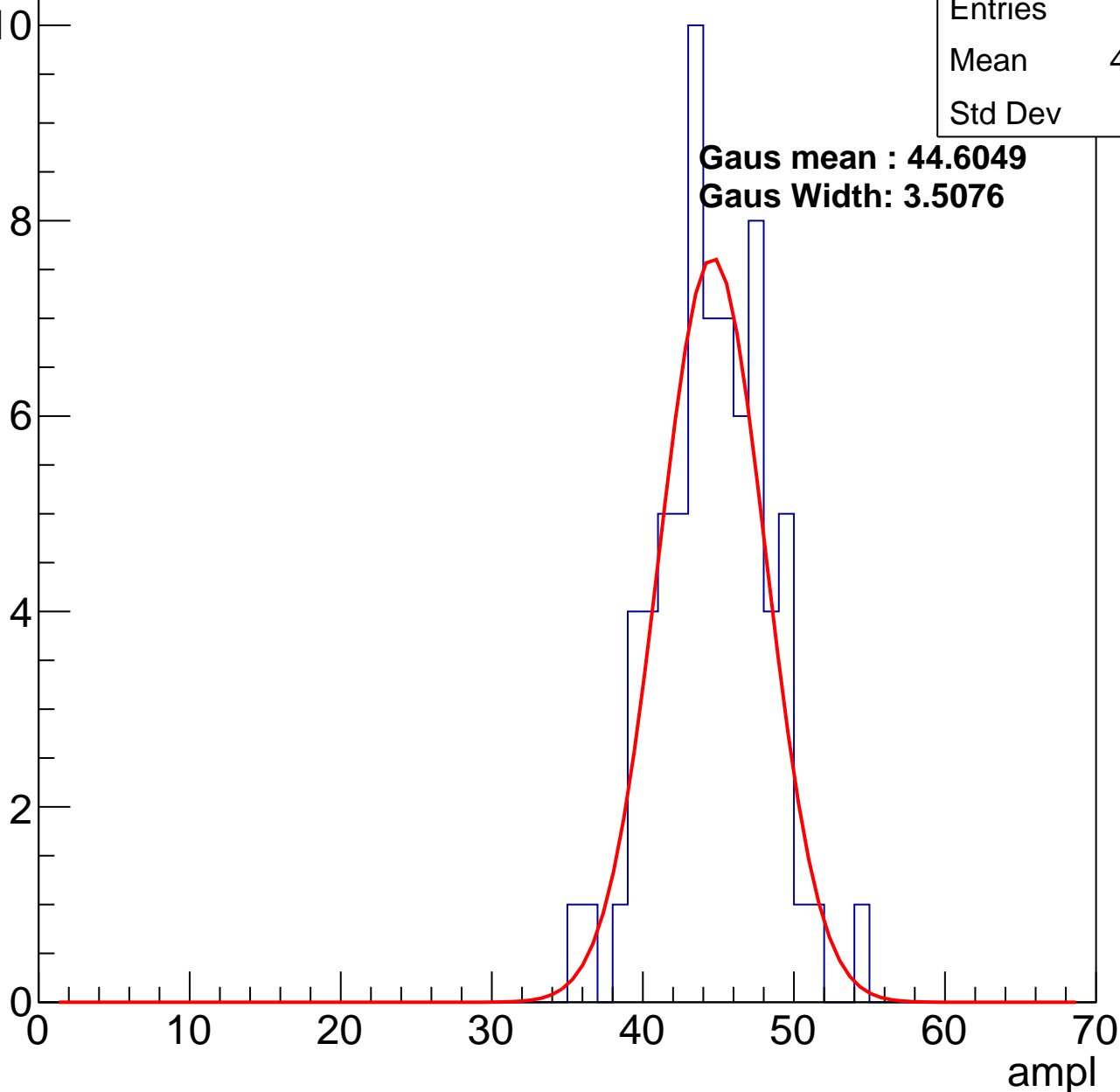
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	71
Mean	44.18
Std Dev	3.55

**Gaus mean : 44.6049**

**Gaus Width: 3.5076**

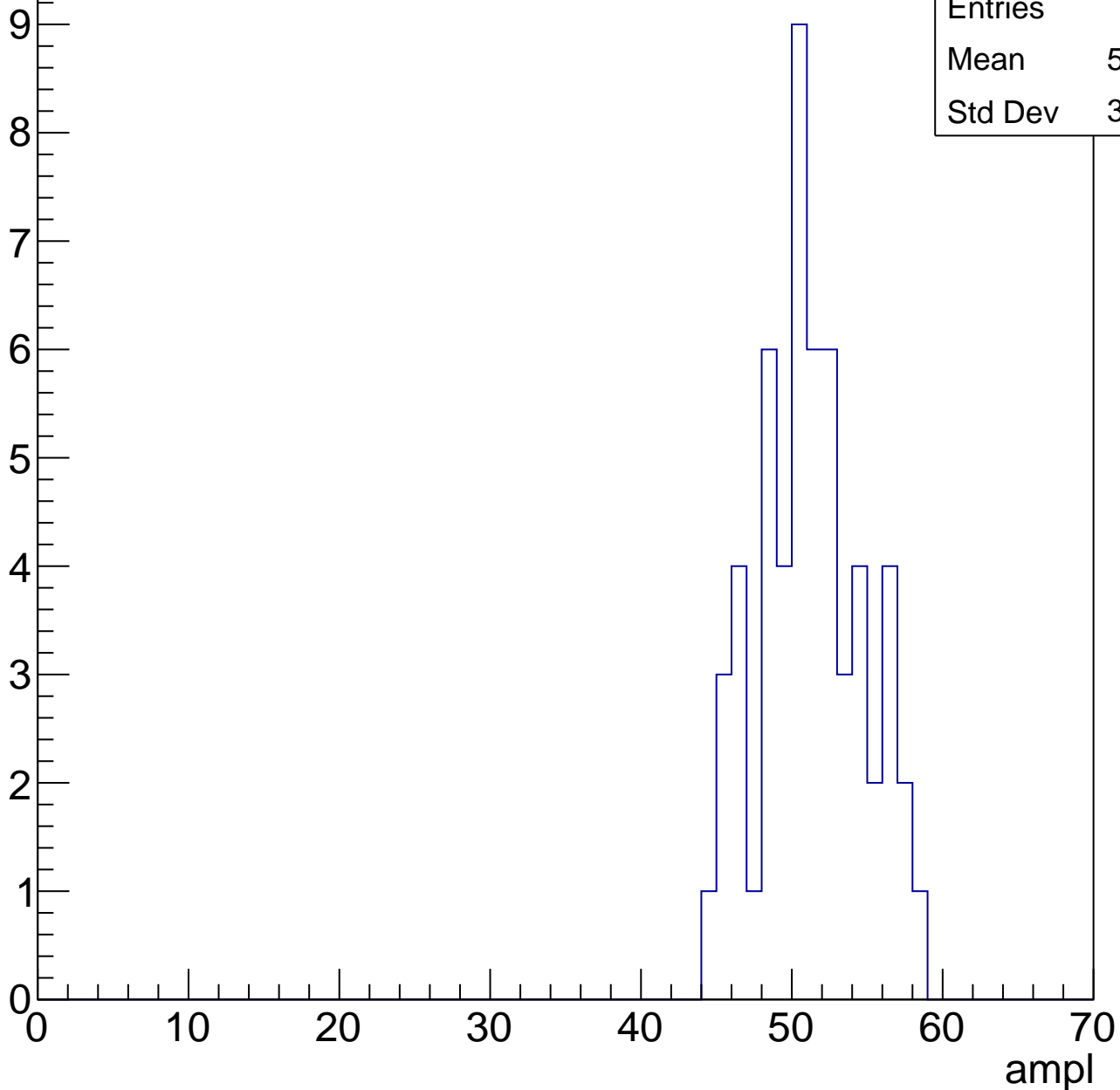


# B1L101S, U22-ch101, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	56
Mean	50.77
Std Dev	3.423

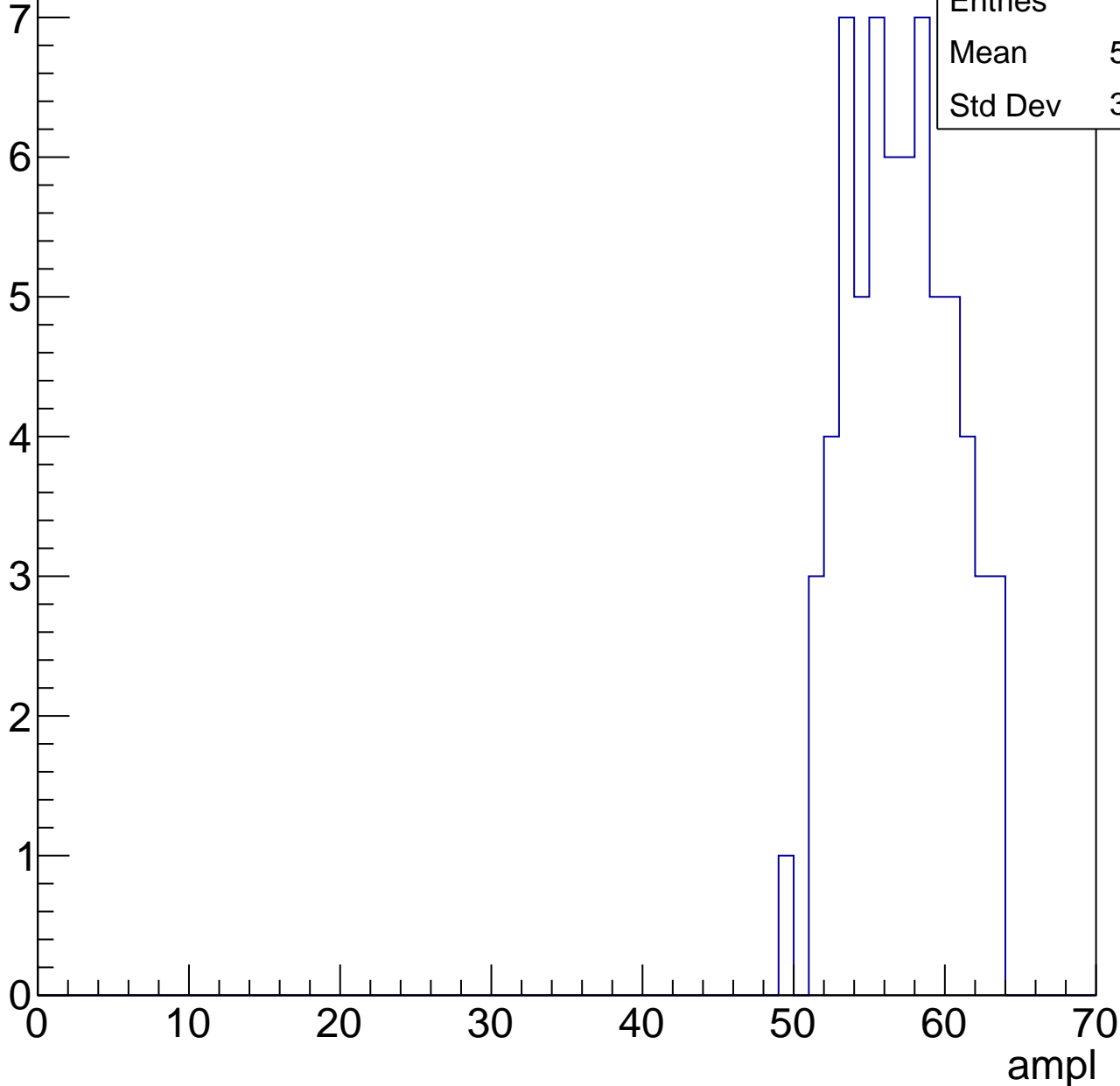


# B1L101S, U22-ch101, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	66
Mean	56.58
Std Dev	3.416

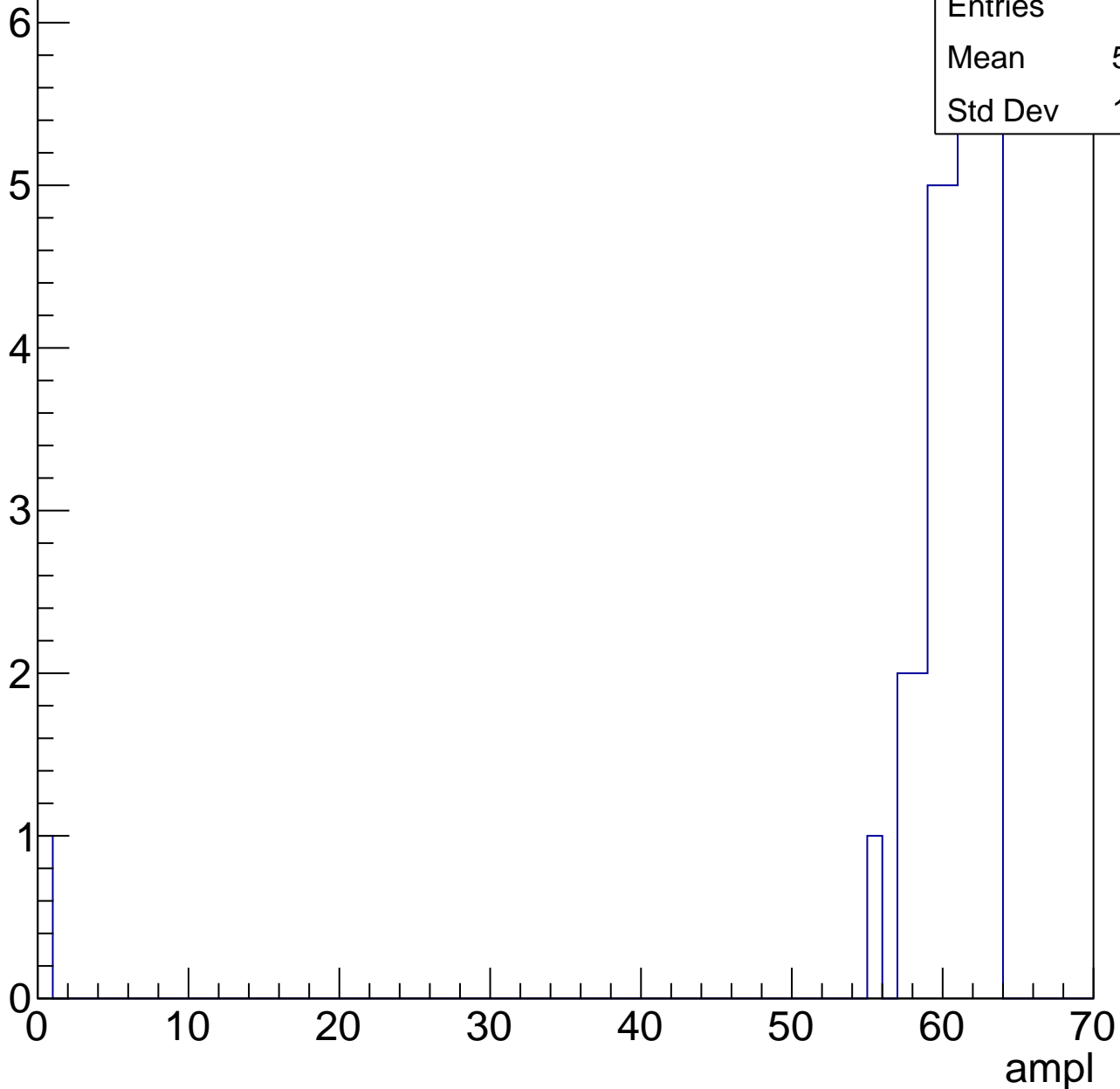


# B1L101S, U22-ch101, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	34
Mean	58.71
Std Dev	10.41



# B1L101S, U22-ch101, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U22-ch101, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U22-ch102, adc0

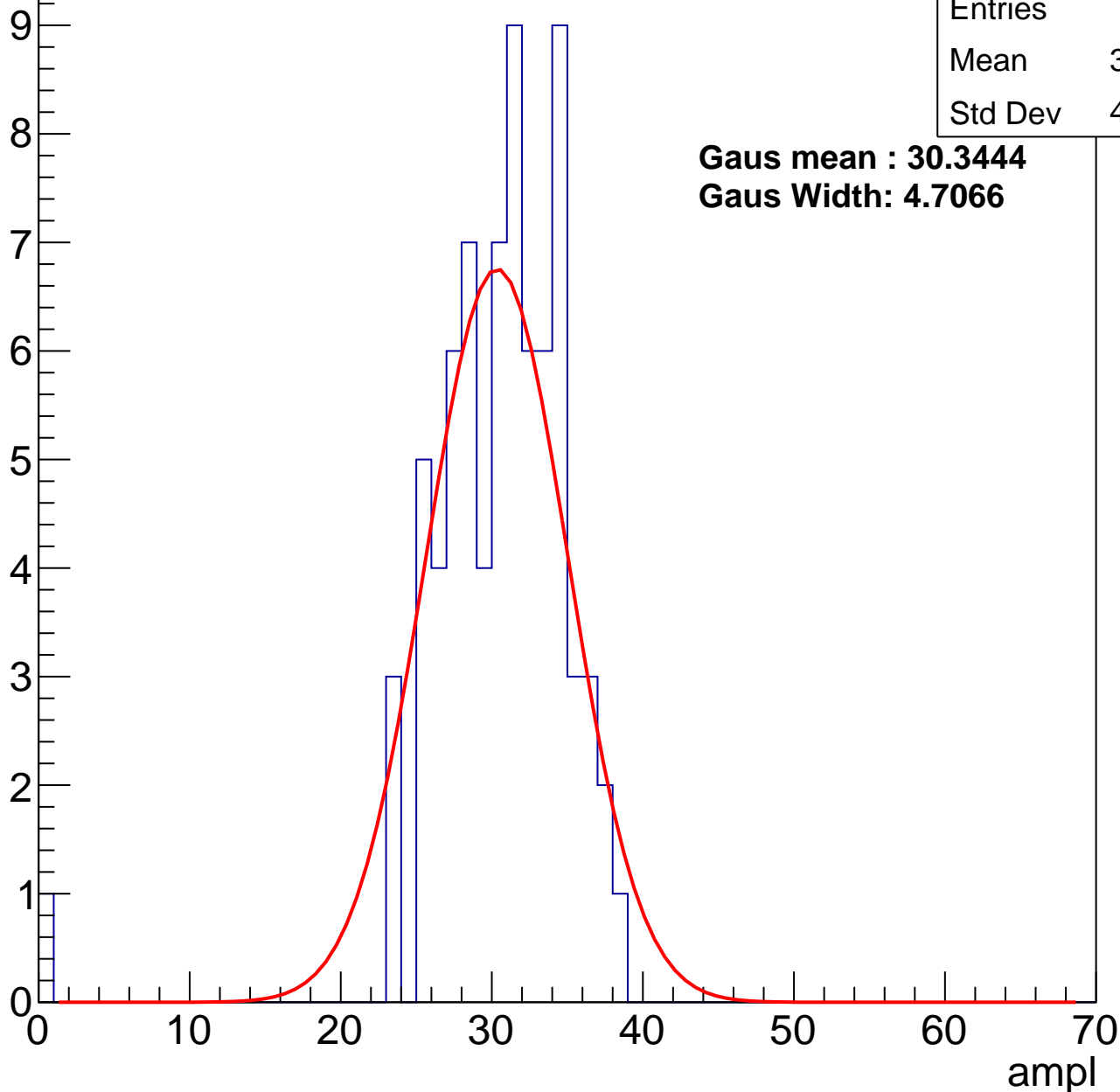
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	76
Mean	30.03
Std Dev	4.997

**Gaus mean : 30.3444**

**Gaus Width: 4.7066**



# B1L101S, U22-ch102, adc1

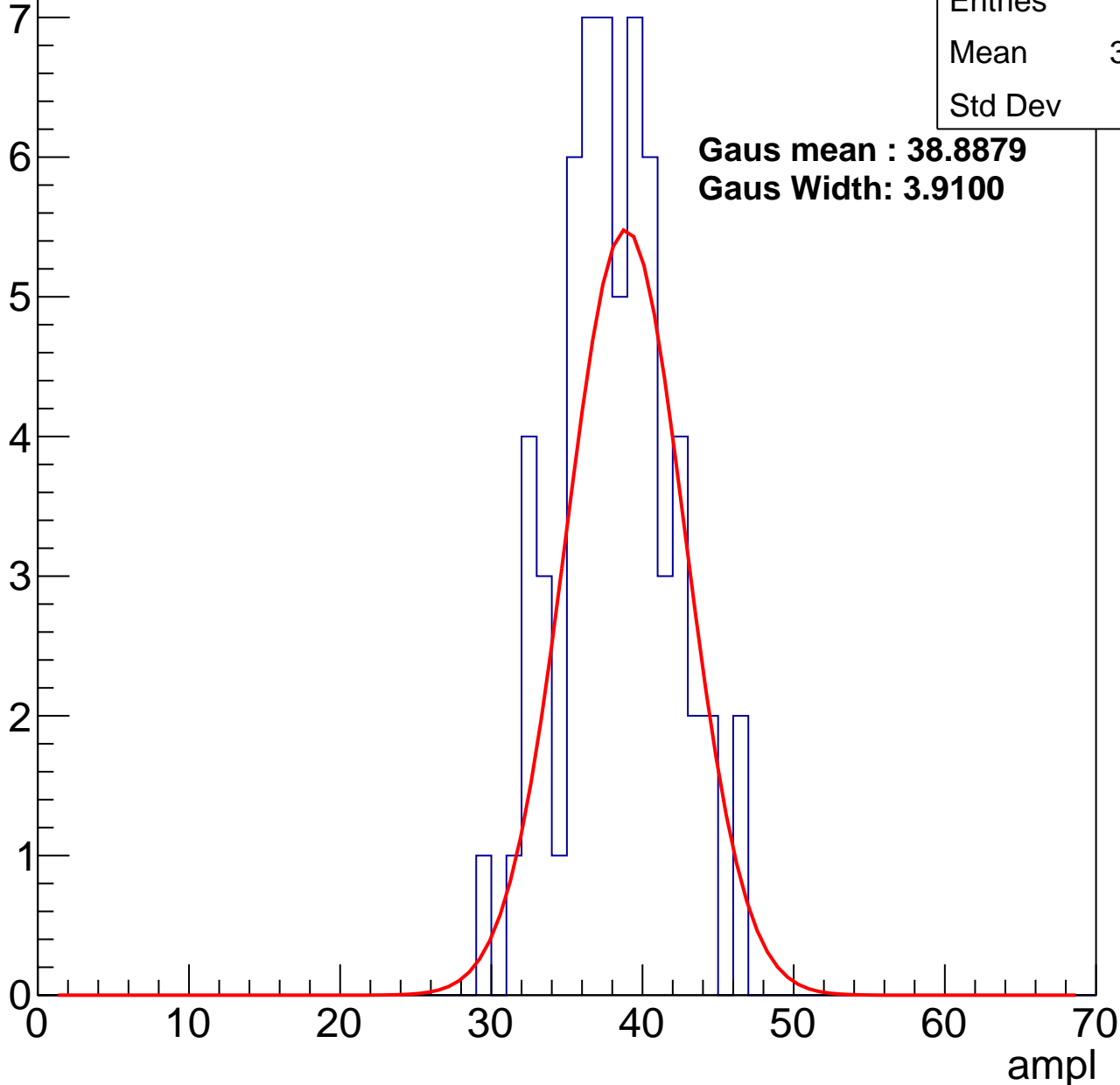
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	37.74
Std Dev	3.67

**Gaus mean : 38.8879**

**Gaus Width: 3.9100**

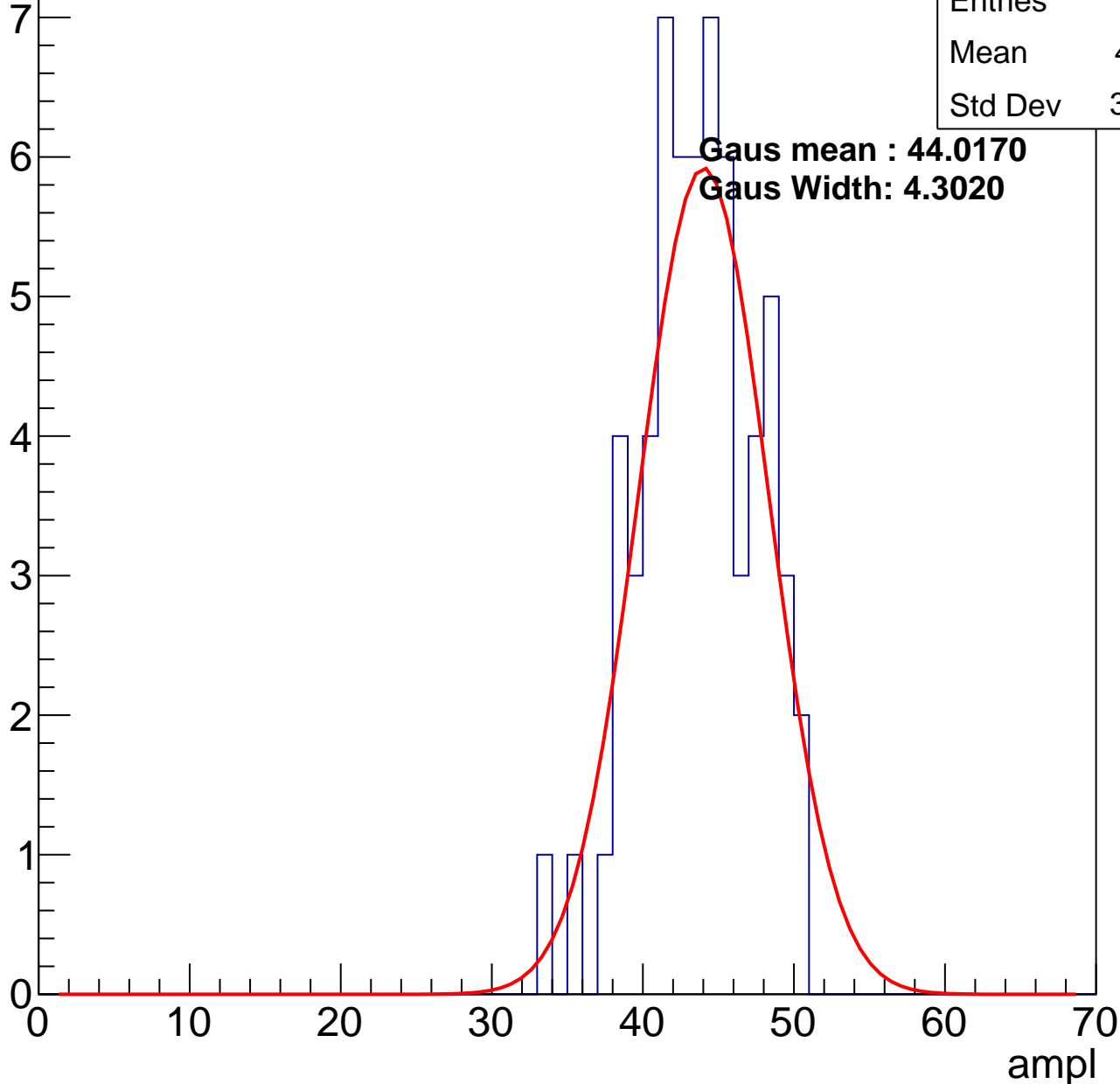


# B1L101S, U22-ch102, adc2

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	43.21
Std Dev	3.713

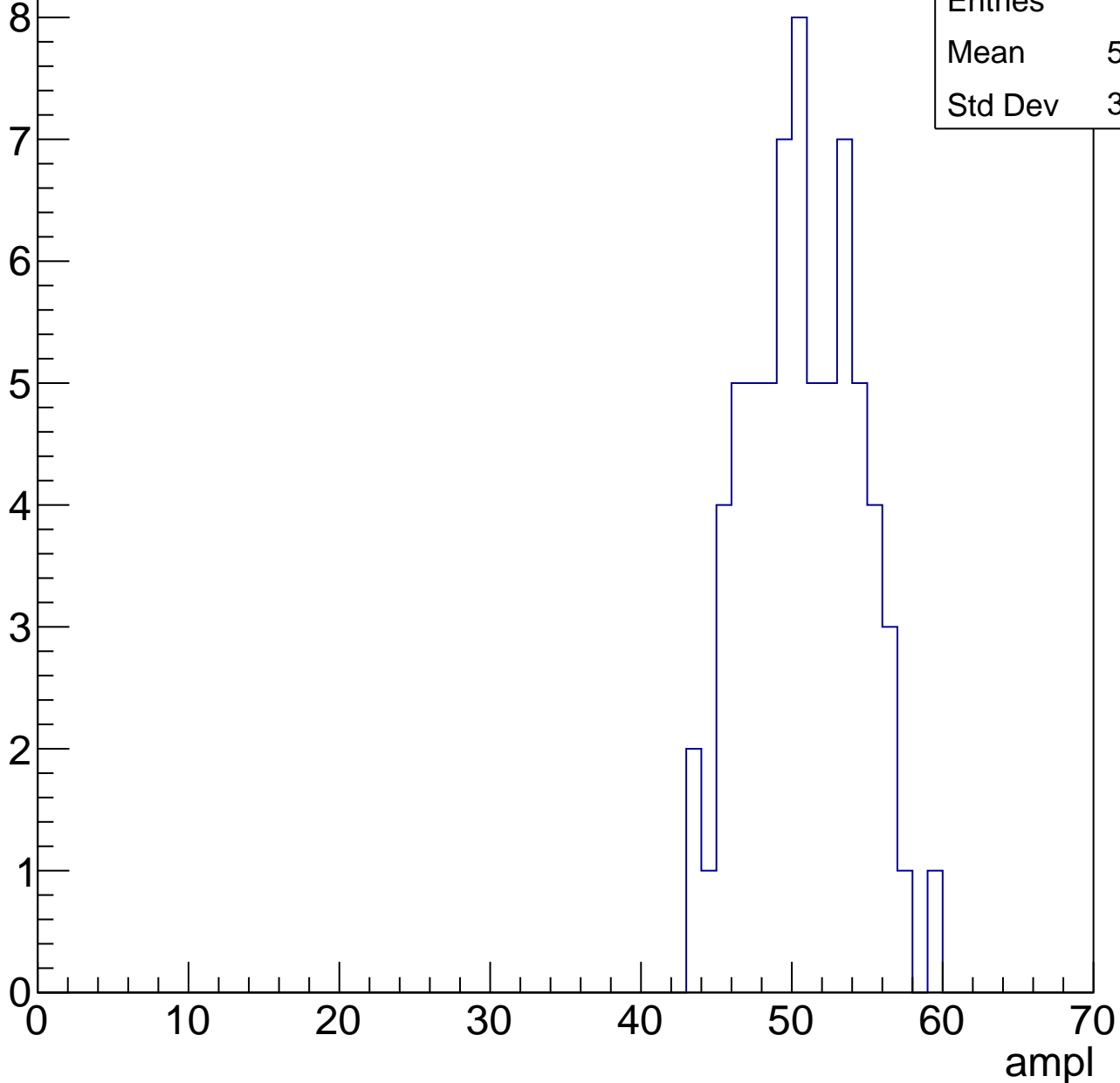


# B1L101S, U22-ch102, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	50.26
Std Dev	3.612

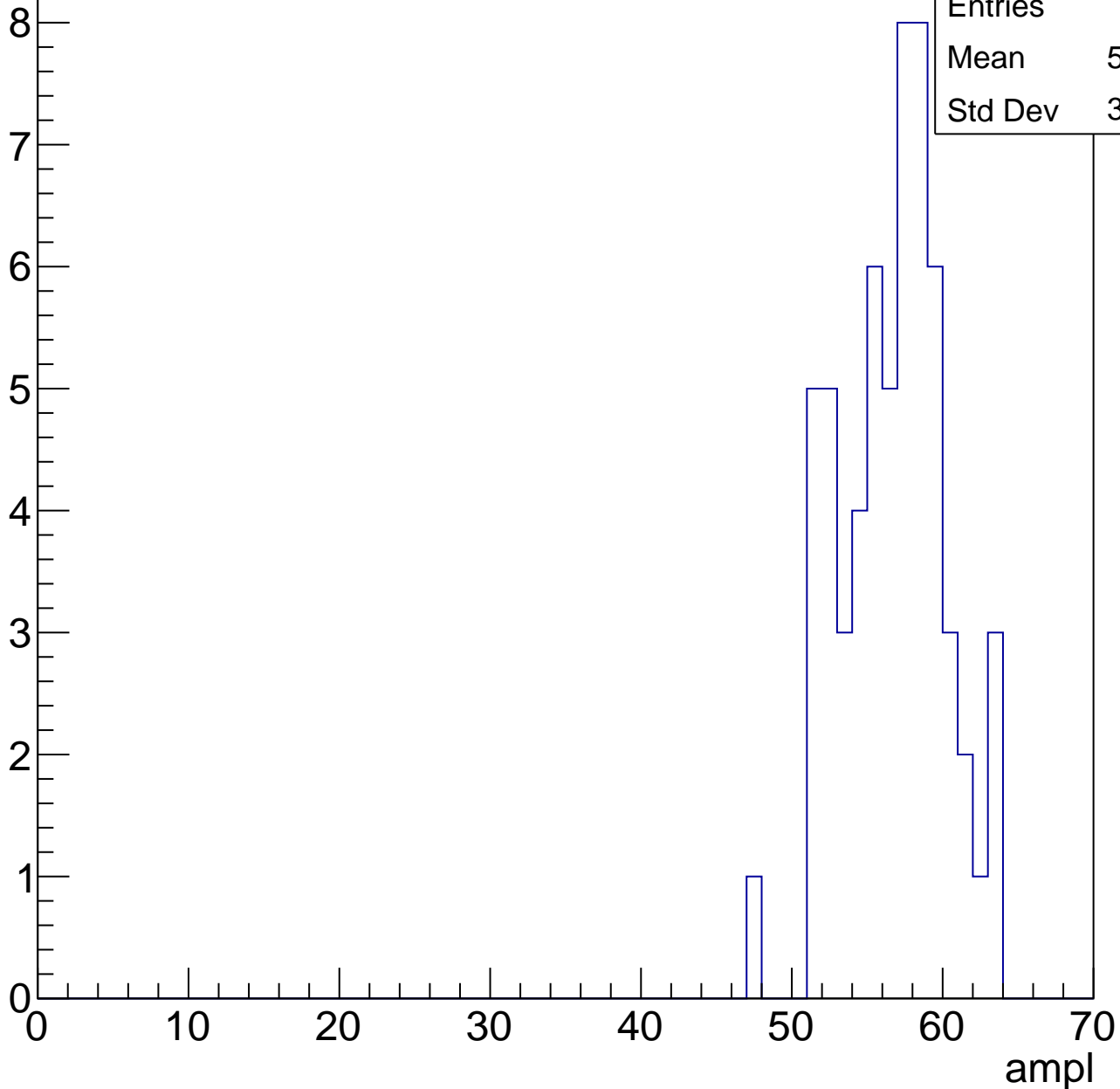


# B1L101S, U22-ch102, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	60
Mean	56.23
Std Dev	3.432

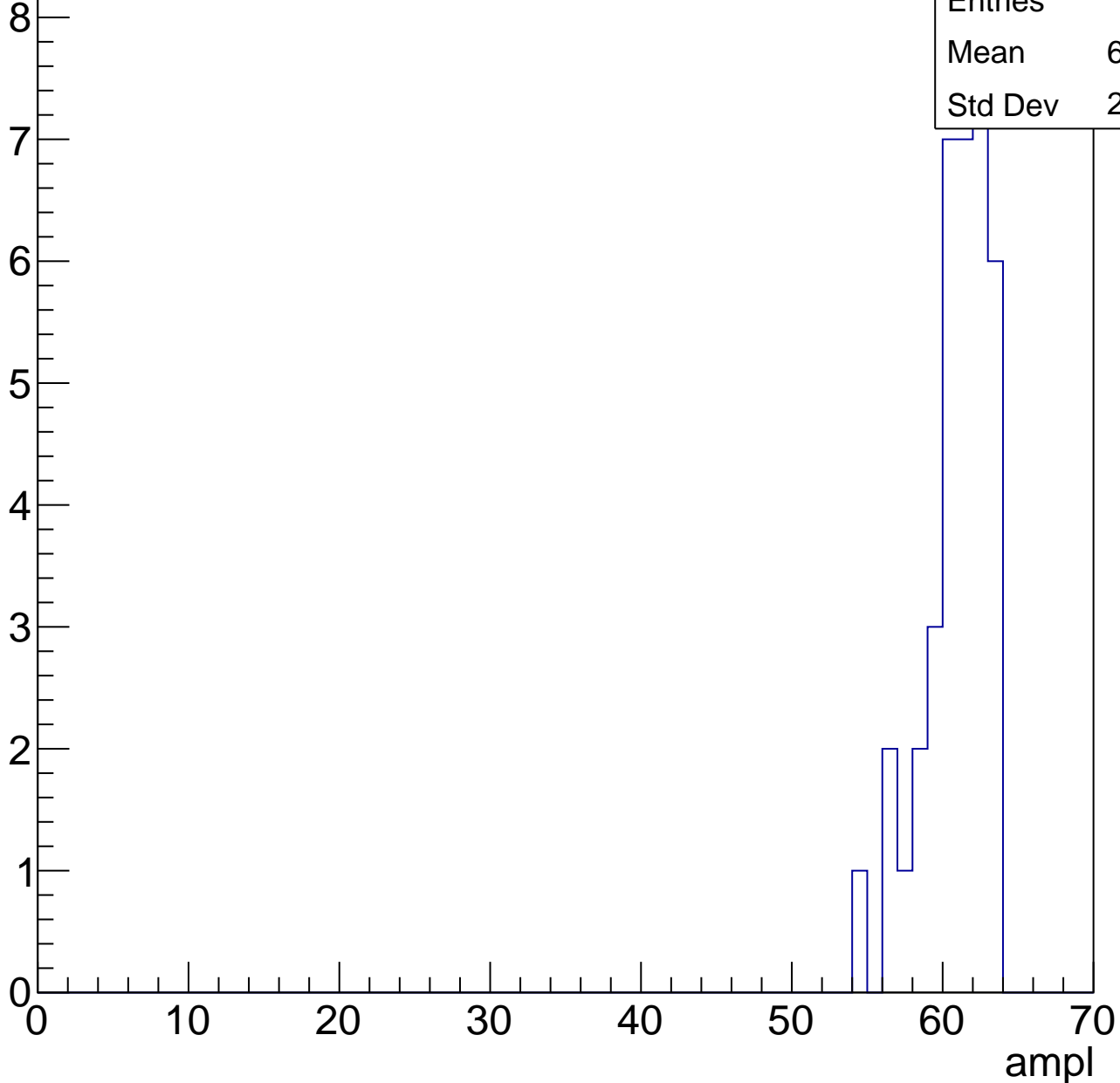


# B1L101S, U22-ch102, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	37
Mean	60.46
Std Dev	2.164



# B1L101S, U22-ch102, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U22-ch102, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U22-ch103, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	69
Mean	31.65
Std Dev	3.434

**Gaus mean : 31.9817**

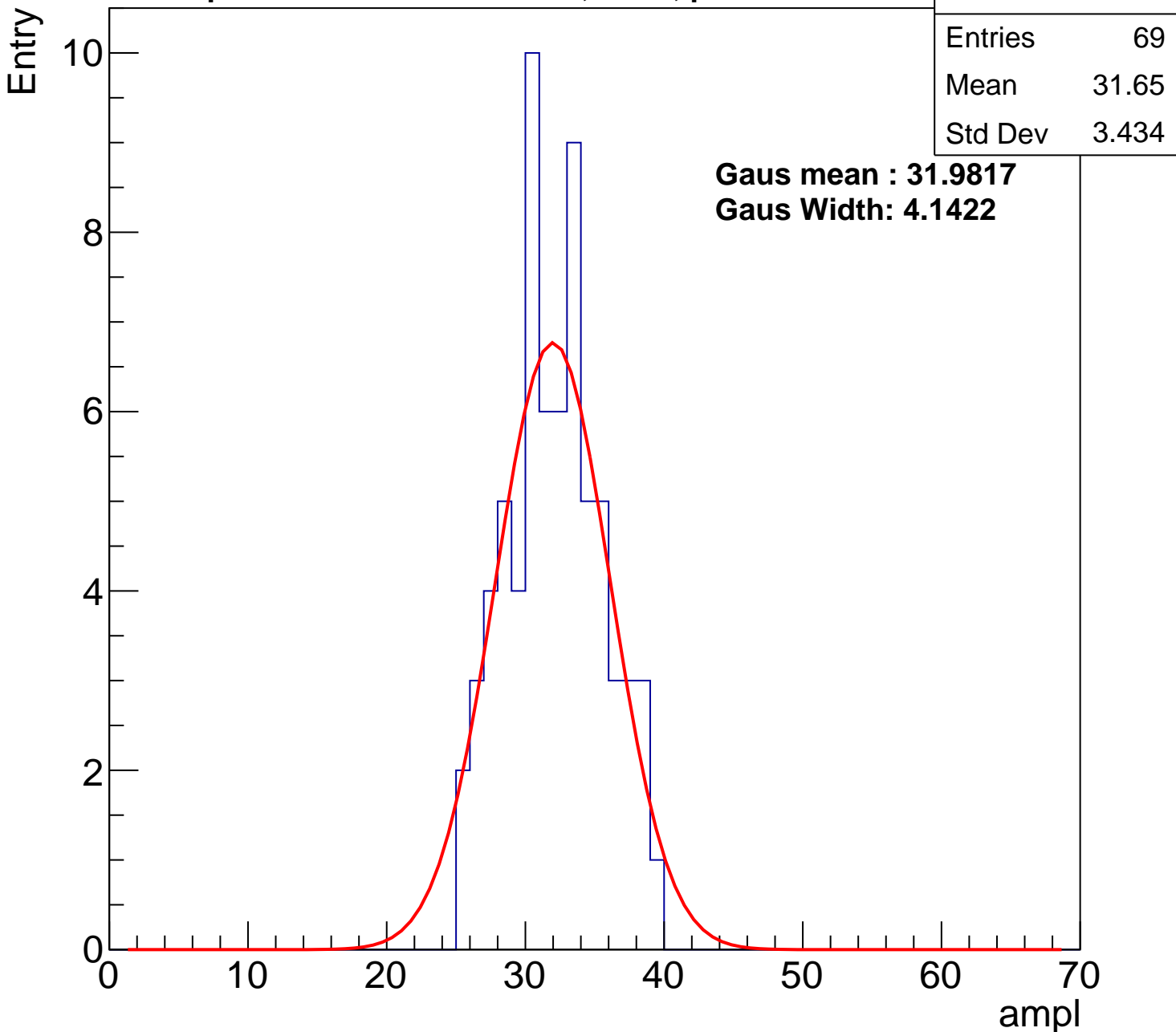
**Gaus Width: 4.1422**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U22-ch103, adc1

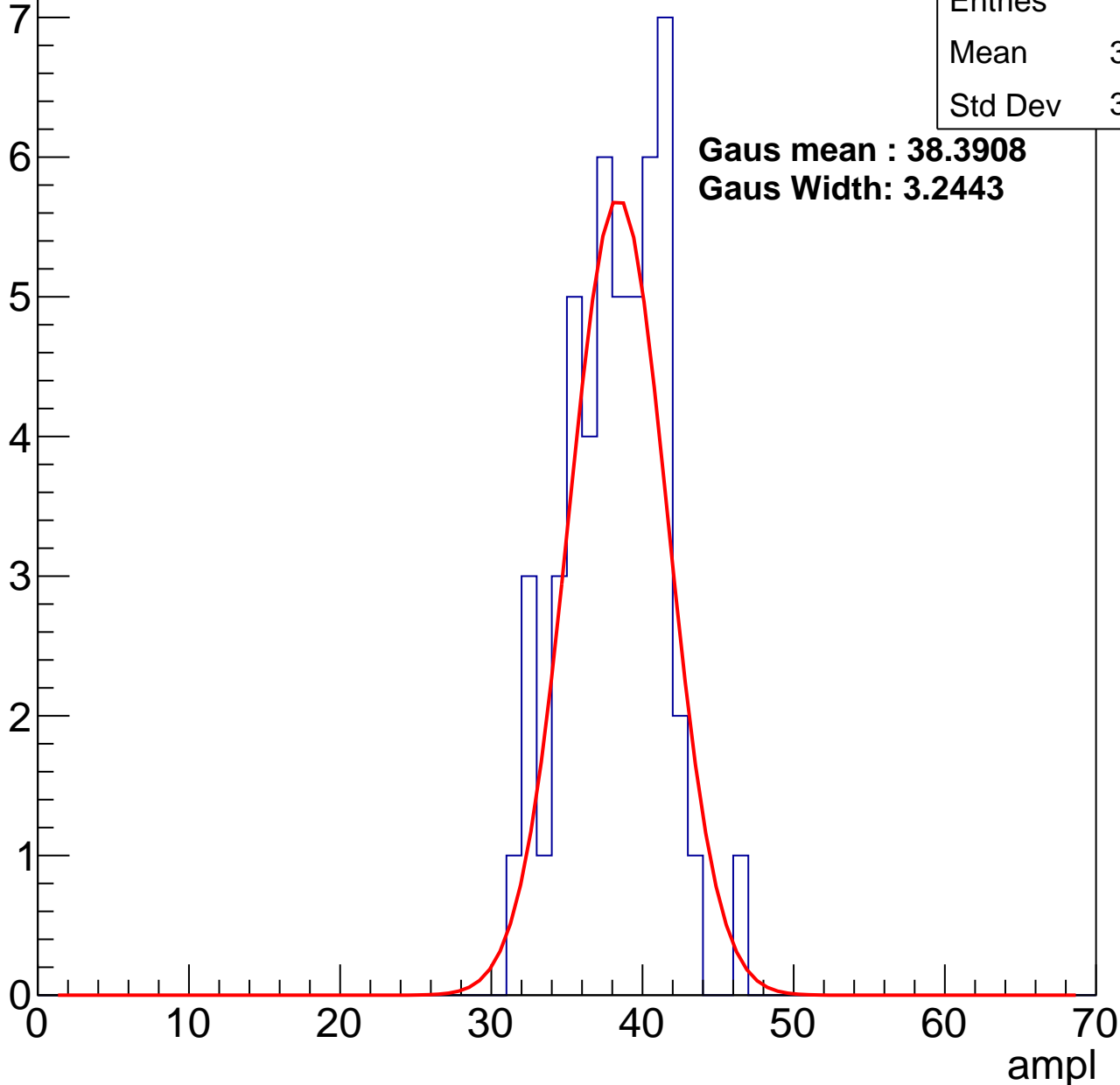
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	50
Mean	37.76
Std Dev	3.185

**Gaus mean : 38.3908**

**Gaus Width: 3.2443**



# B1L101S, U22-ch103, adc2

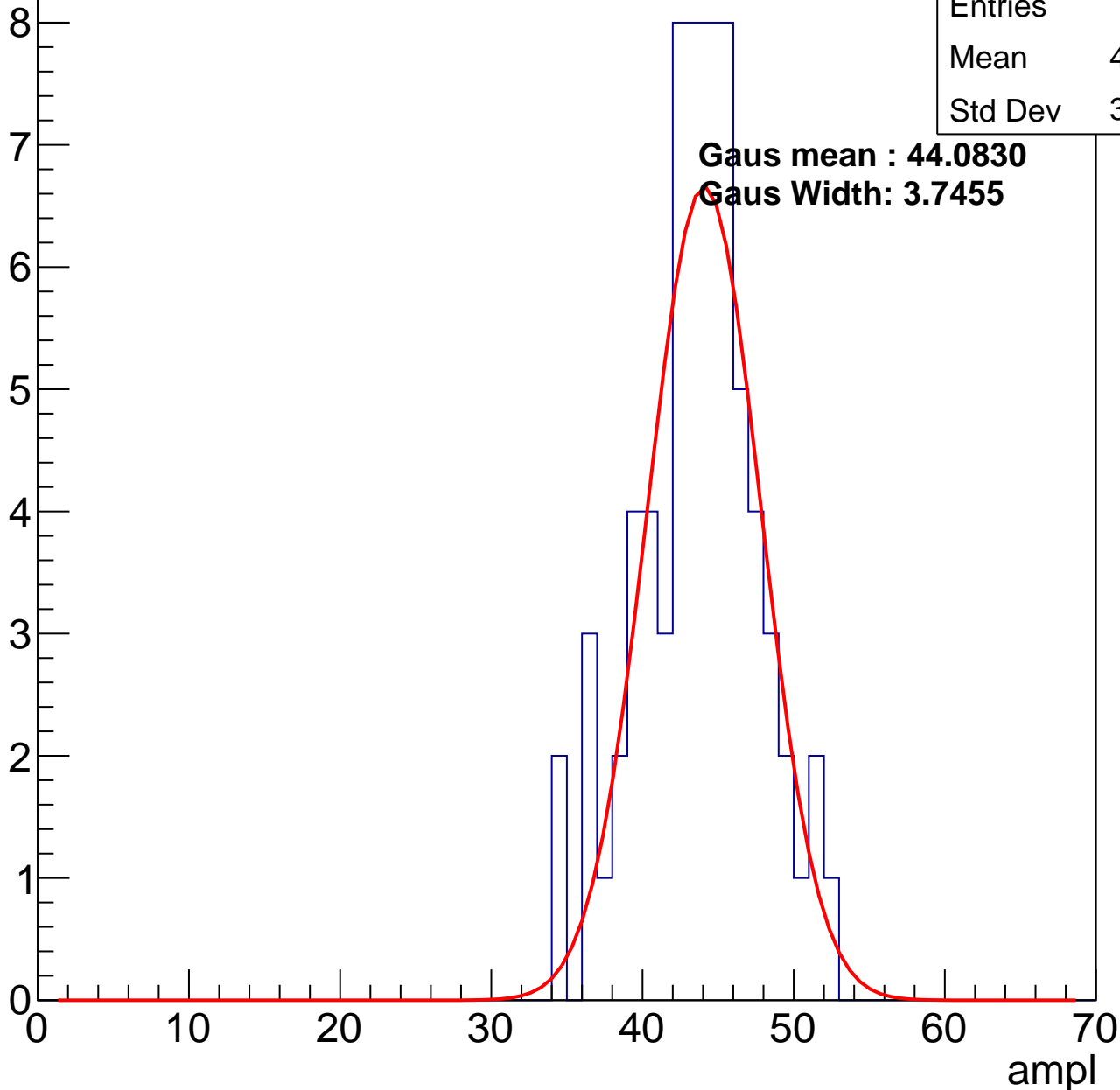
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	43.25
Std Dev	3.928

**Gaus mean : 44.0830**

**Gaus Width: 3.7455**

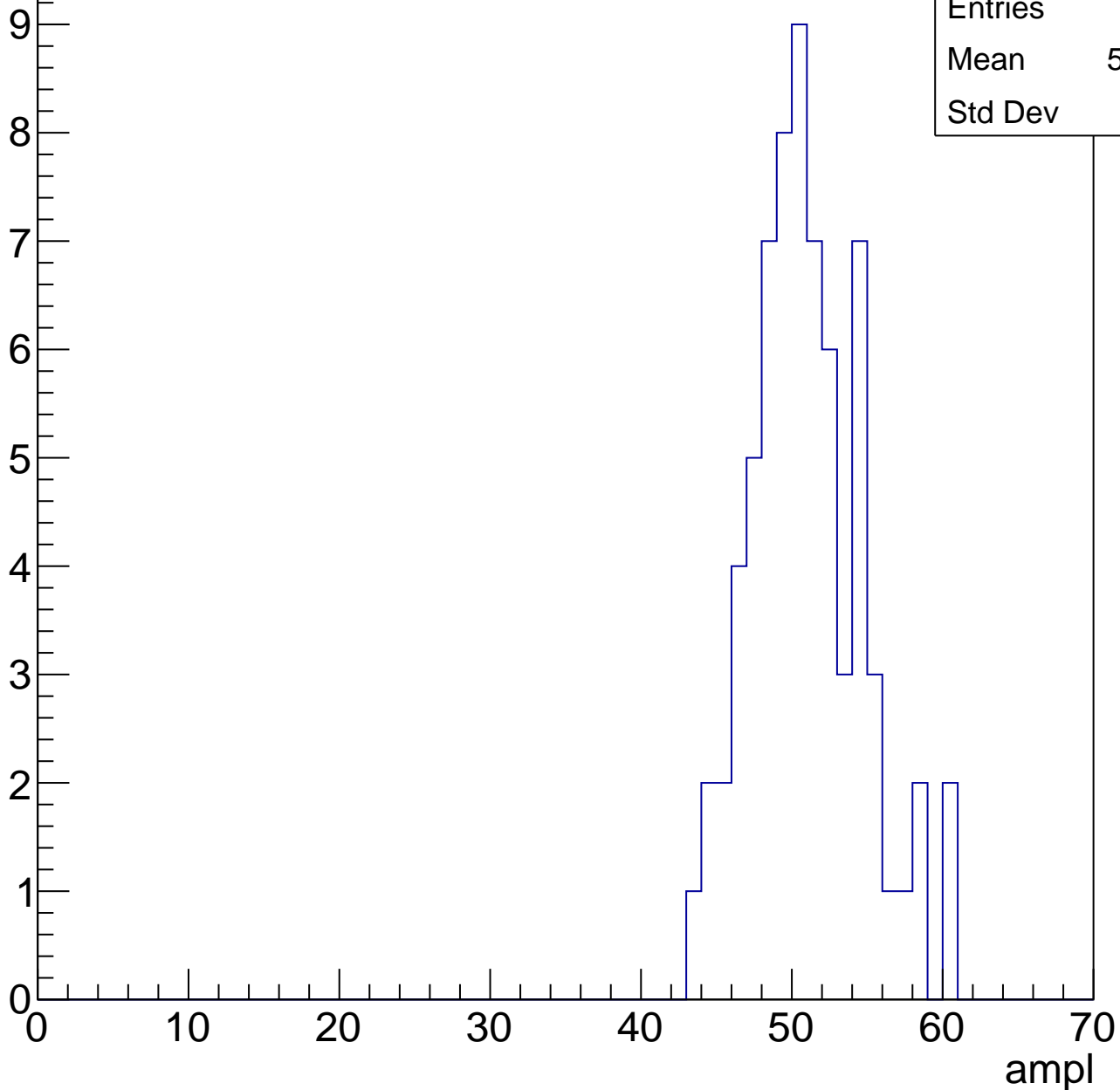


# B1L101S, U22-ch103, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	50.54
Std Dev	3.69

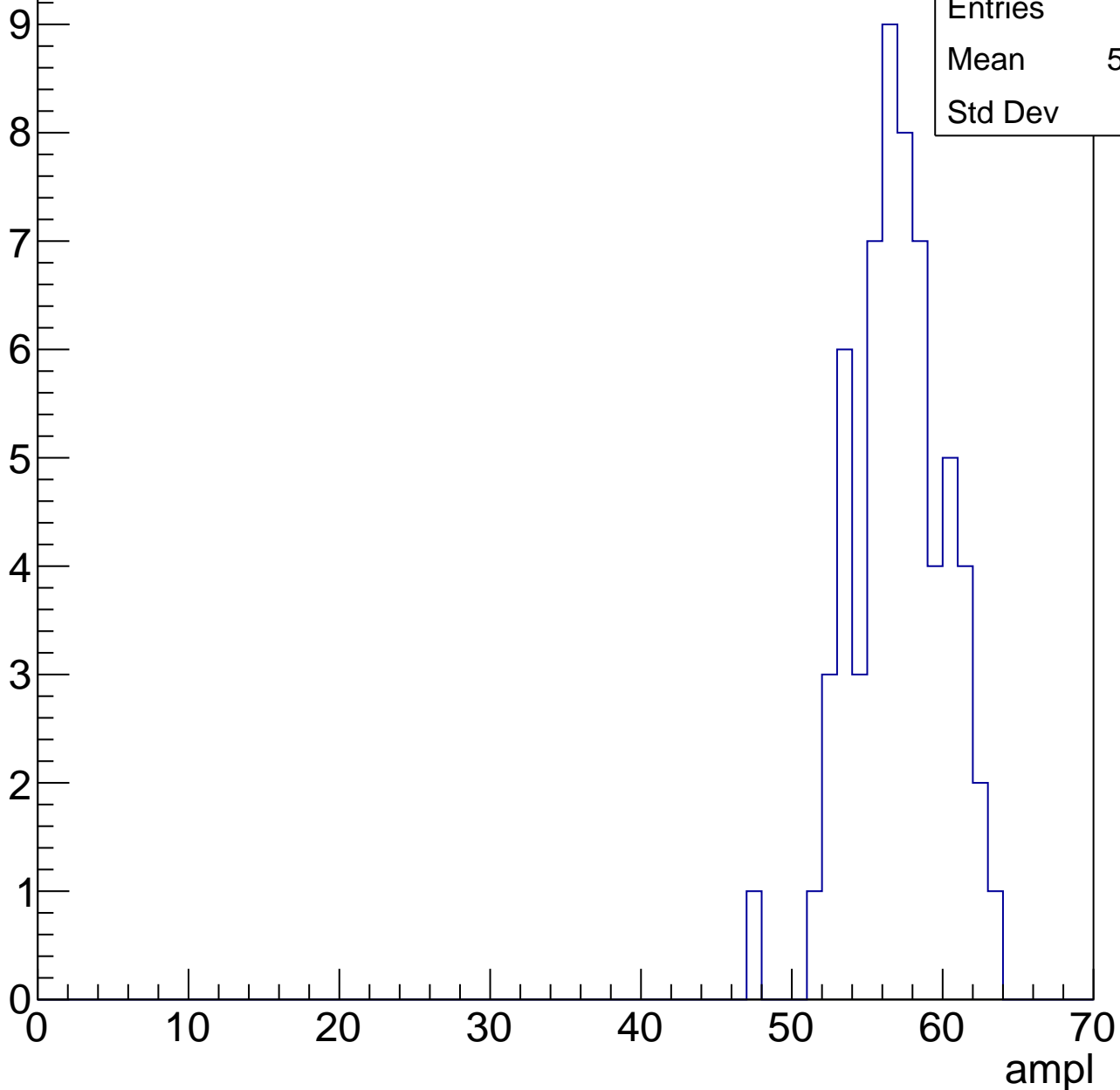


# B1L101S, U22-ch103, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	56.59
Std Dev	3.08

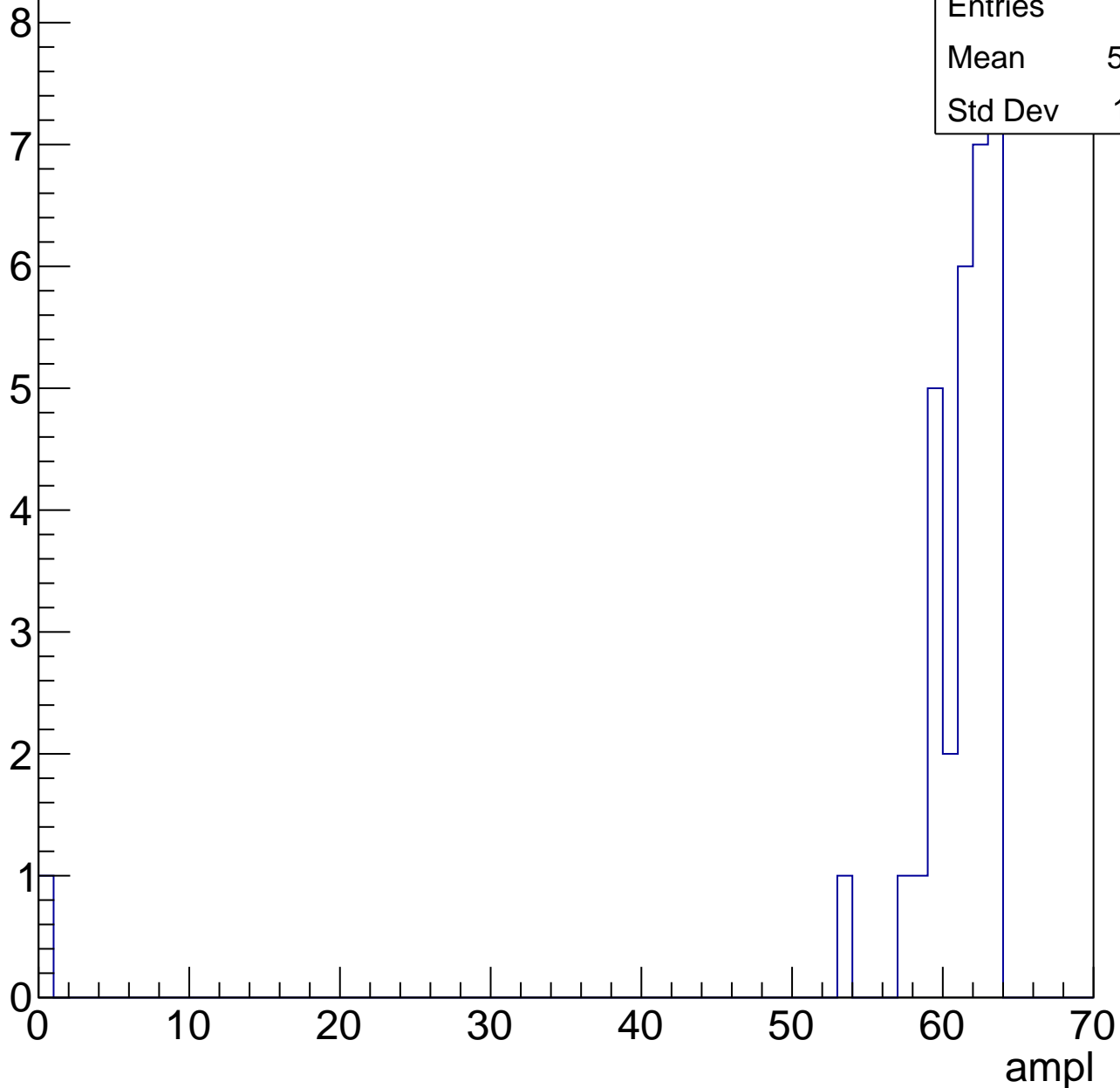


# B1L101S, U22-ch103, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

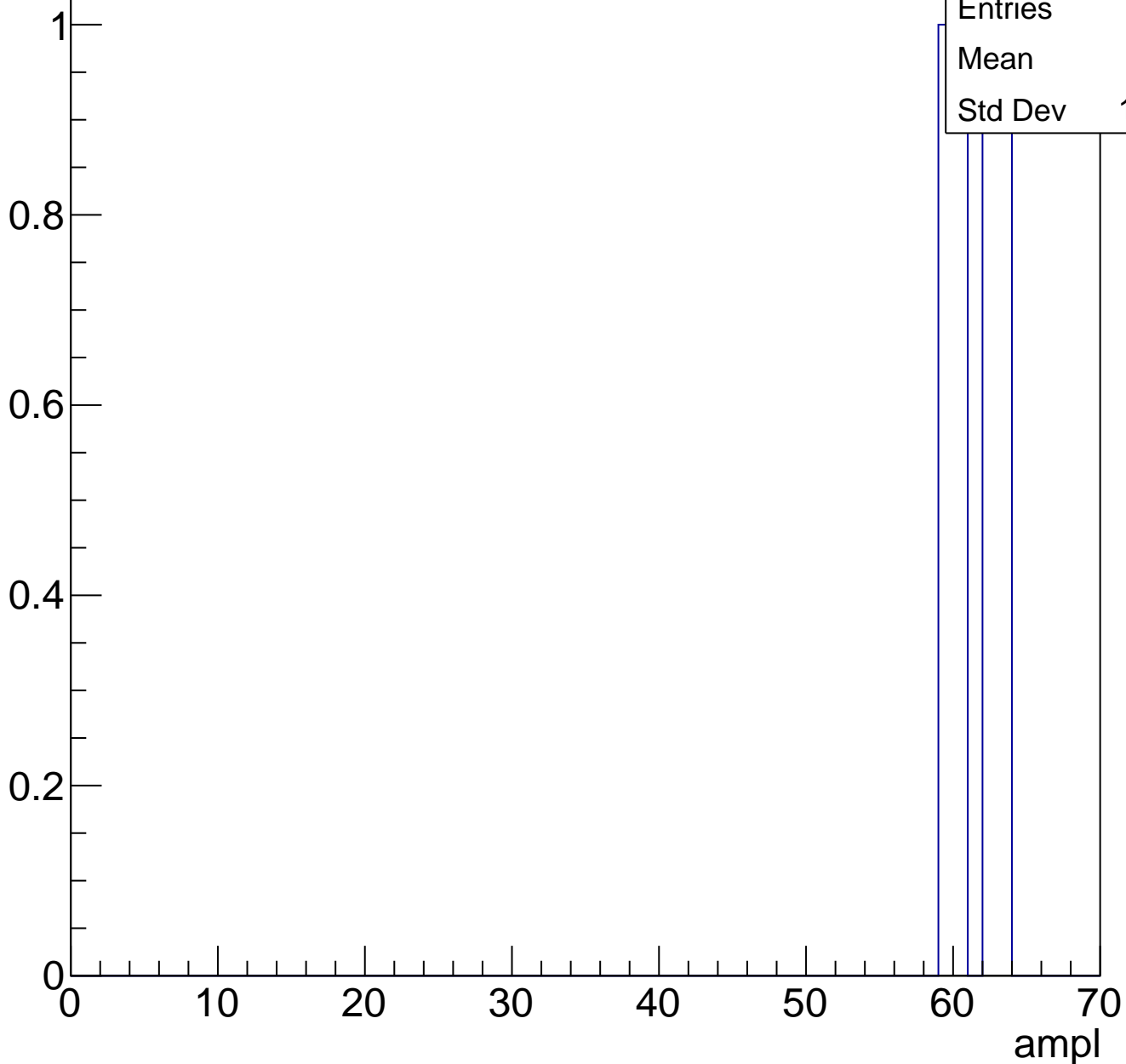
Entries	32
Mean	58.97
Std Dev	10.81



# B1L101S, U22-ch103, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U22-ch103, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L101S, U22-ch104, adc0

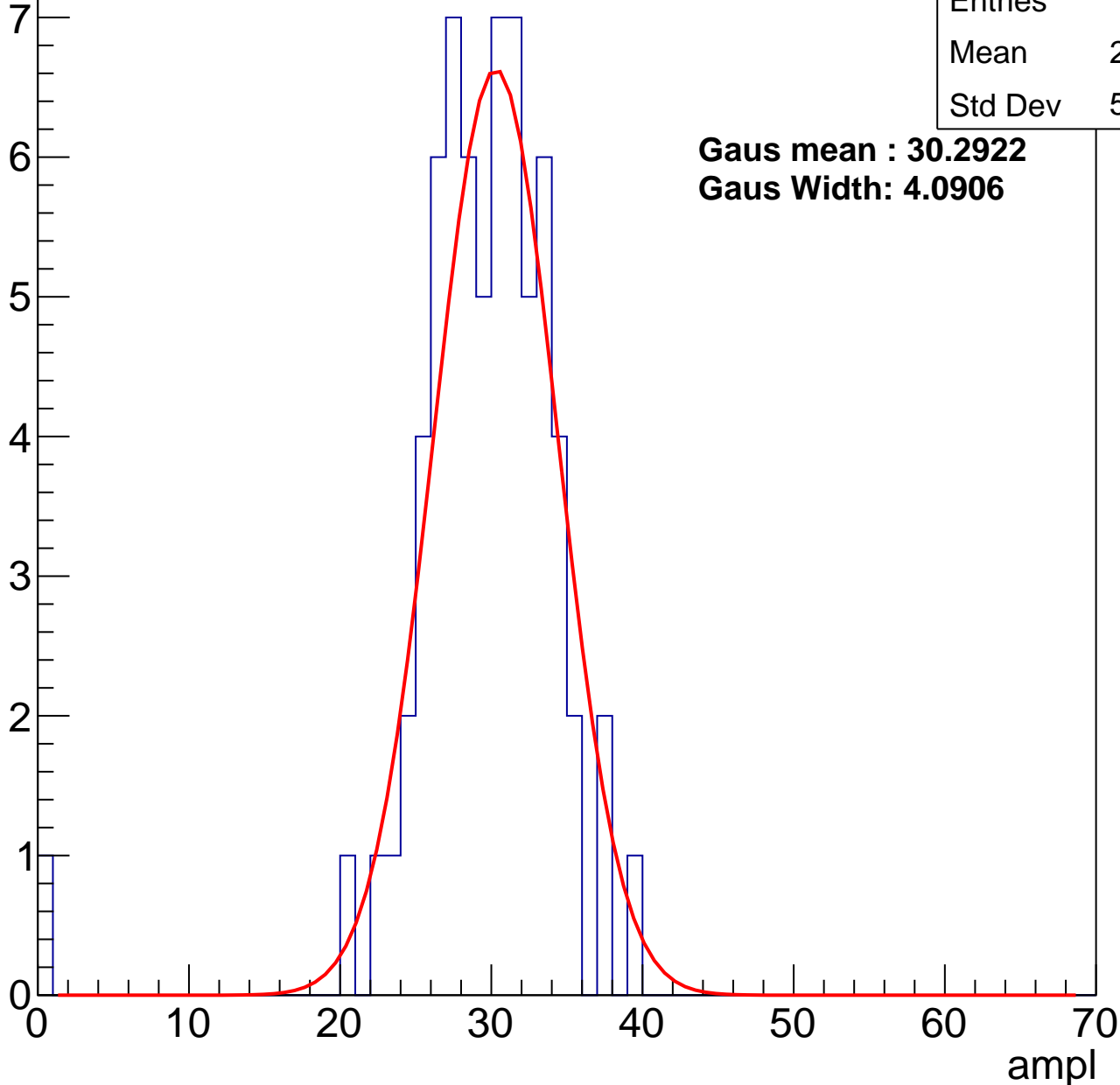
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	29.04
Std Dev	5.123

**Gaus mean : 30.2922**

**Gaus Width: 4.0906**



# B1L101S, U22-ch104, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	80
Mean	36.7
Std Dev	3.703

**Gaus mean : 36.4389**

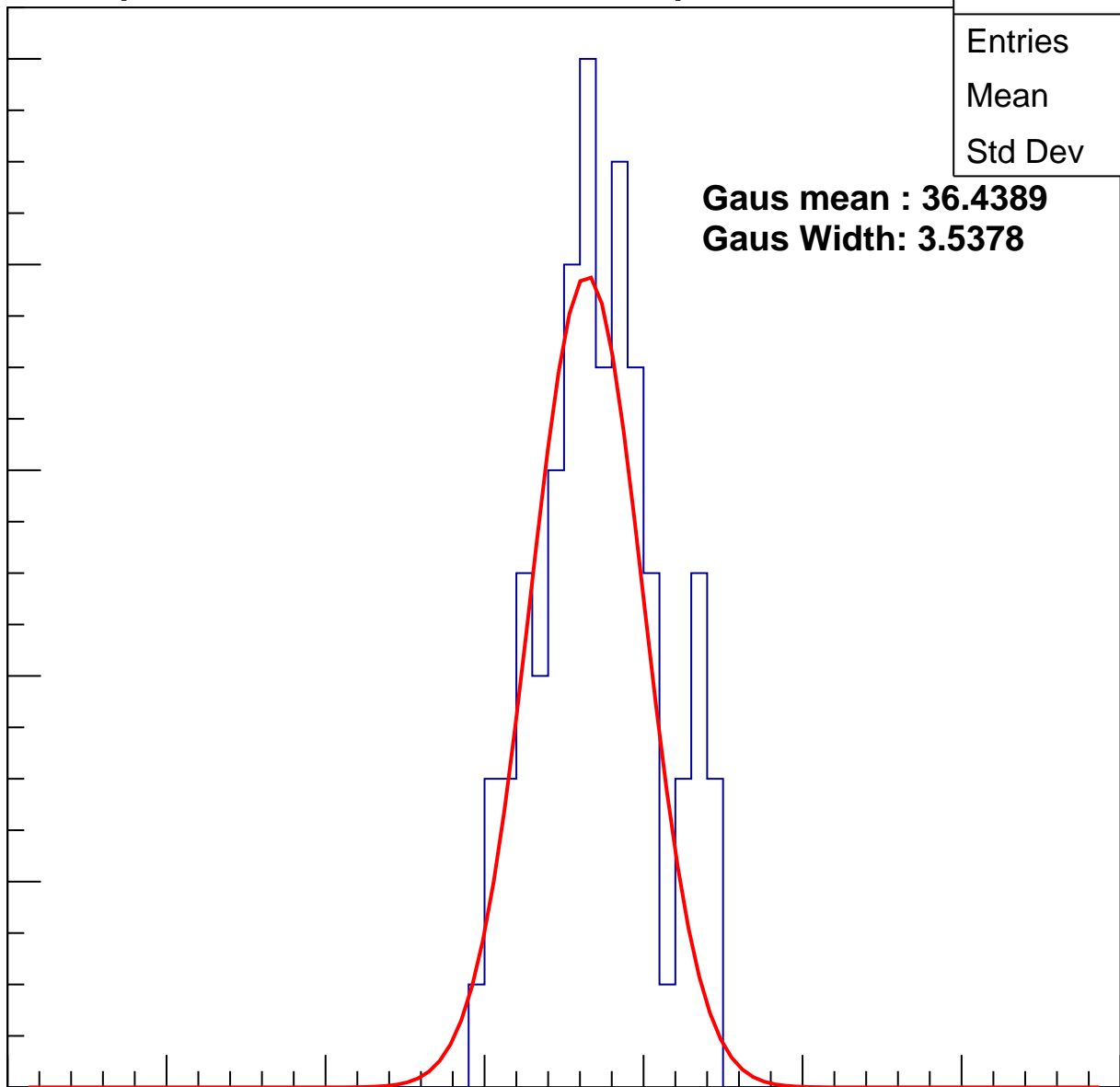
**Gaus Width: 3.5378**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U22-ch104, adc2

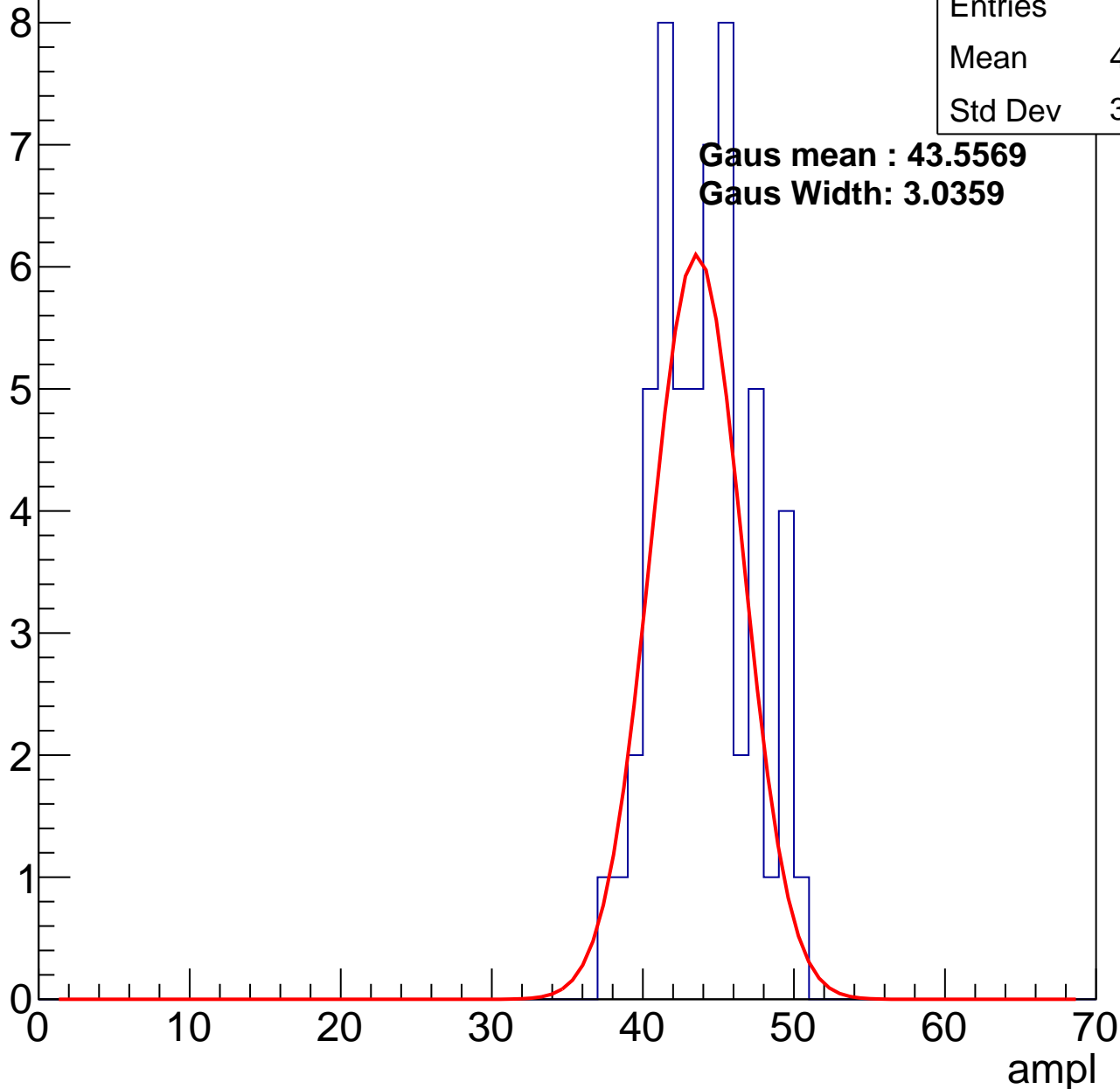
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	55
Mean	43.55
Std Dev	3.056

**Gaus mean : 43.5569**

**Gaus Width: 3.0359**

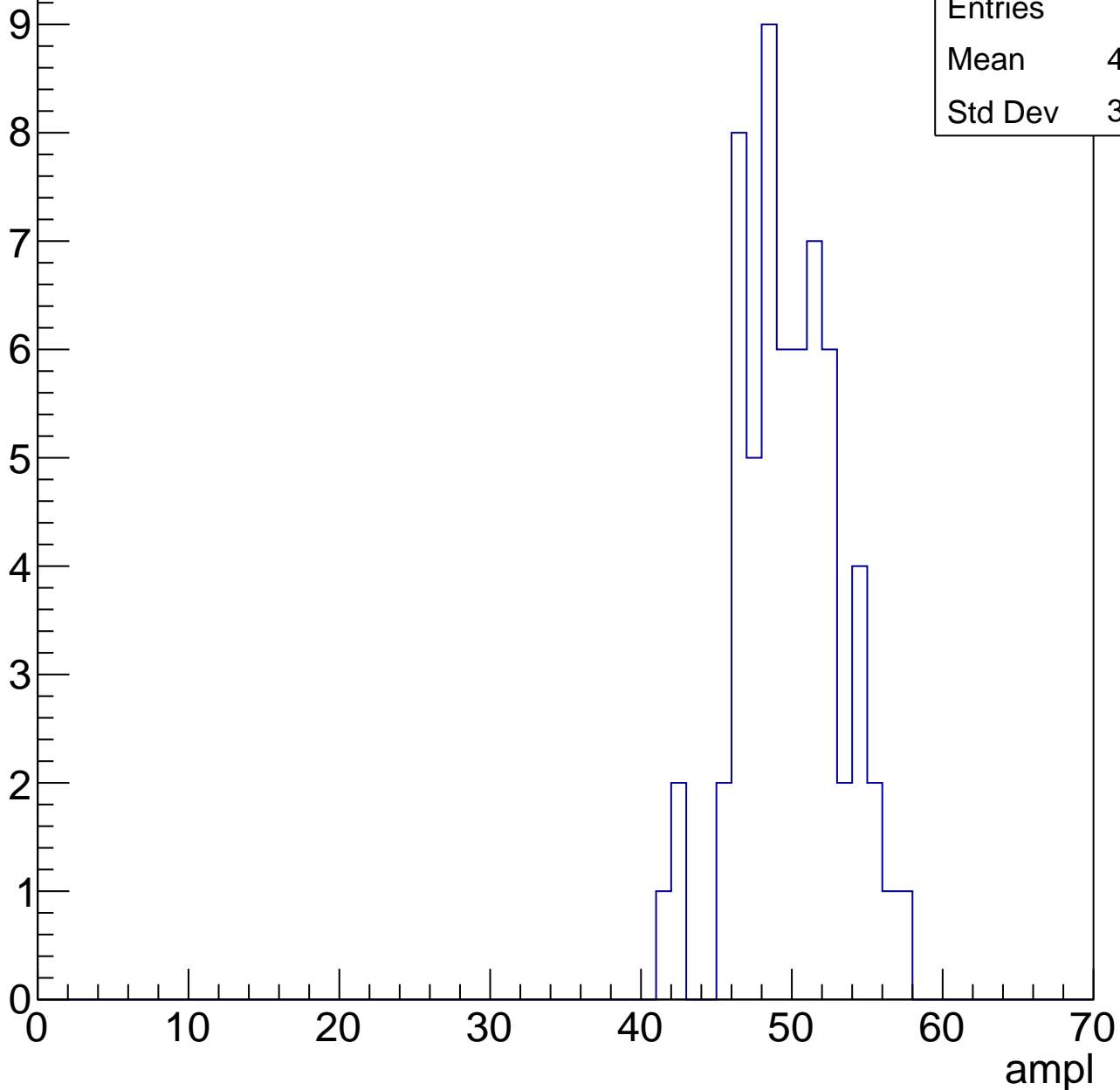


# B1L101S, U22-ch104, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

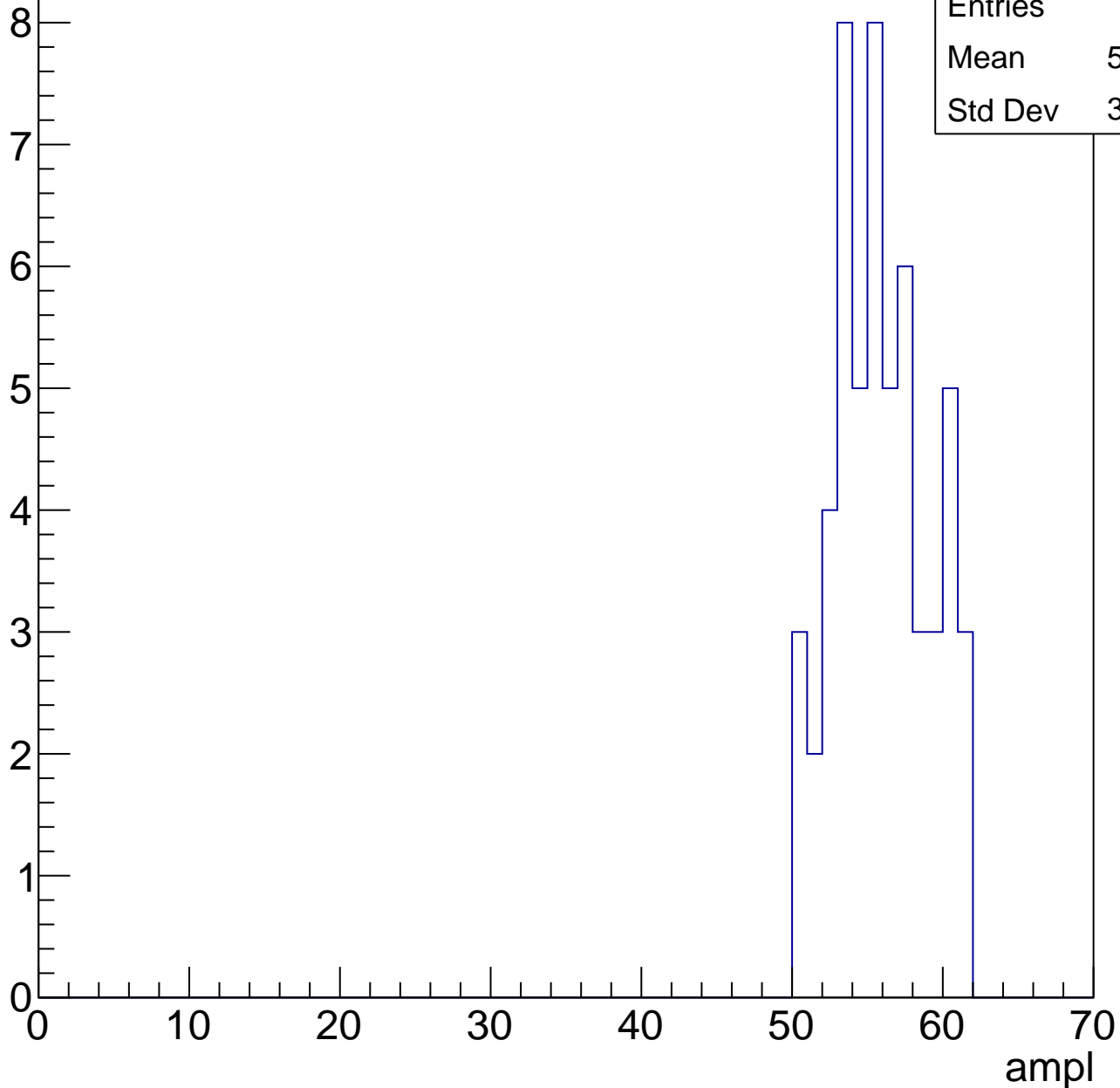
Entries	62
Mean	49.32
Std Dev	3.345



# B1L101S, U22-ch104, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



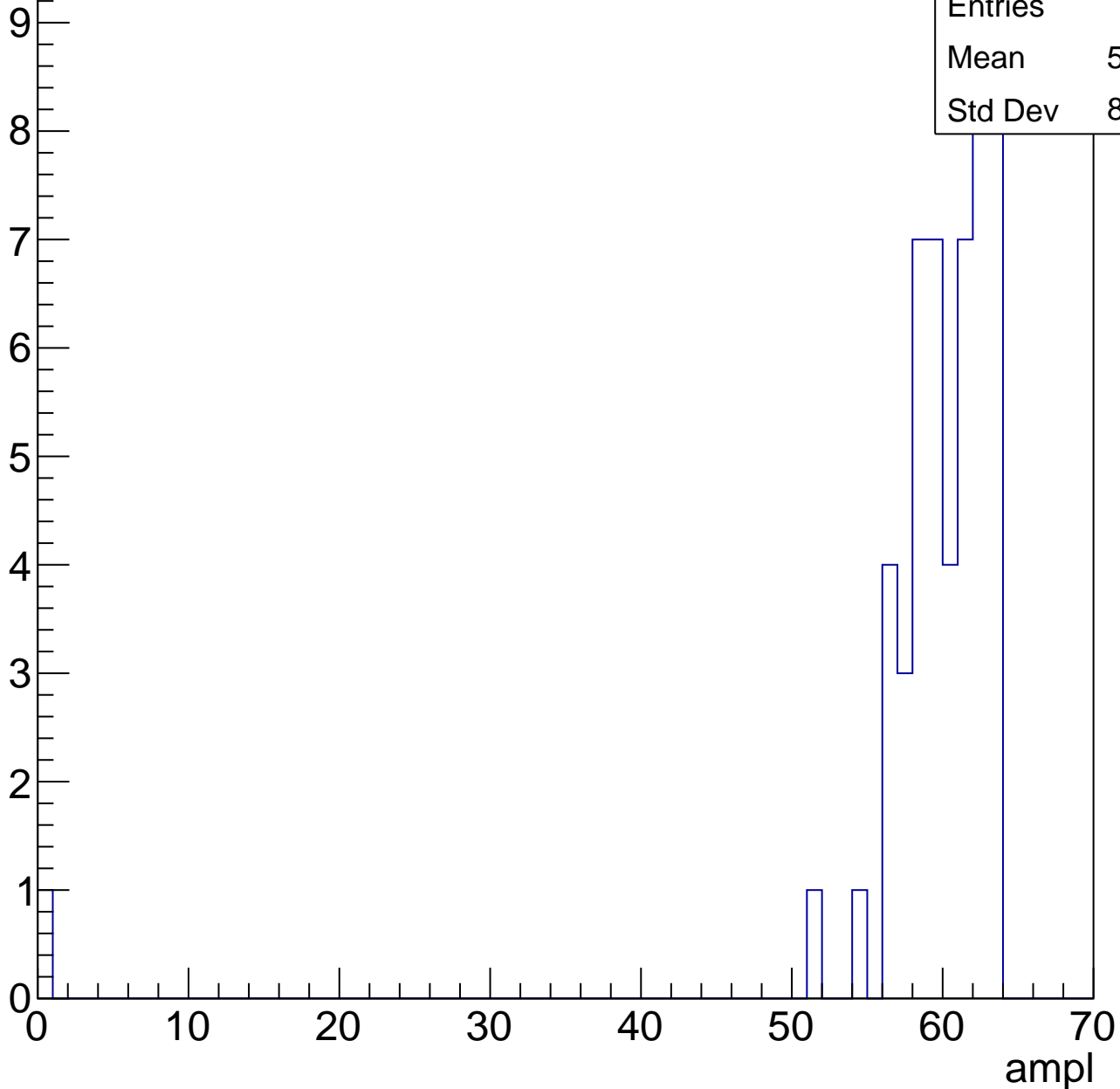
Entries	55
Mean	55.45
Std Dev	3.032

# B1L101S, U22-ch104, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

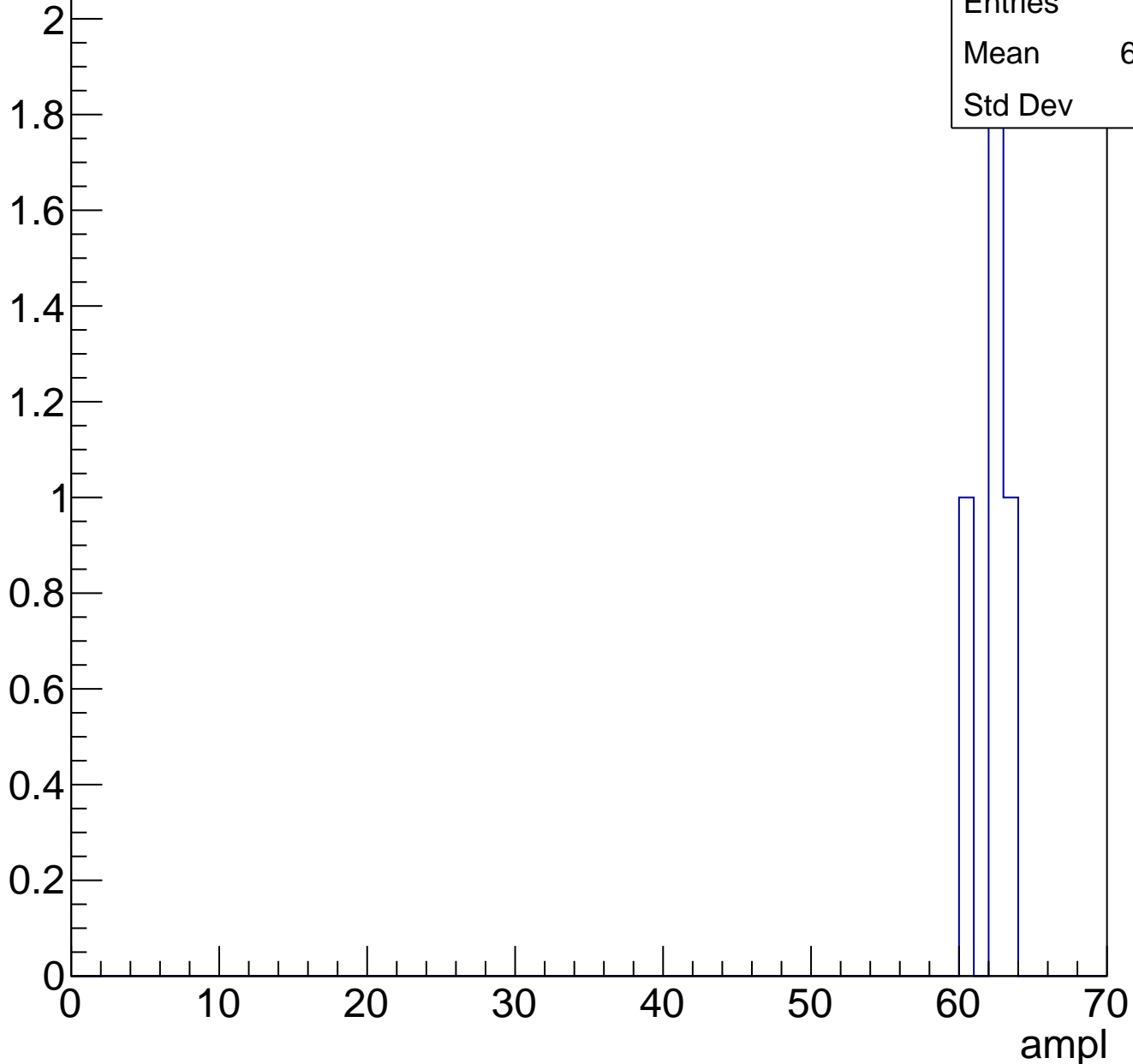
Entries	52
Mean	58.63
Std Dev	8.622



# B1L101S, U22-ch104, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U22-ch104, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L101S, U22-ch105, adc0

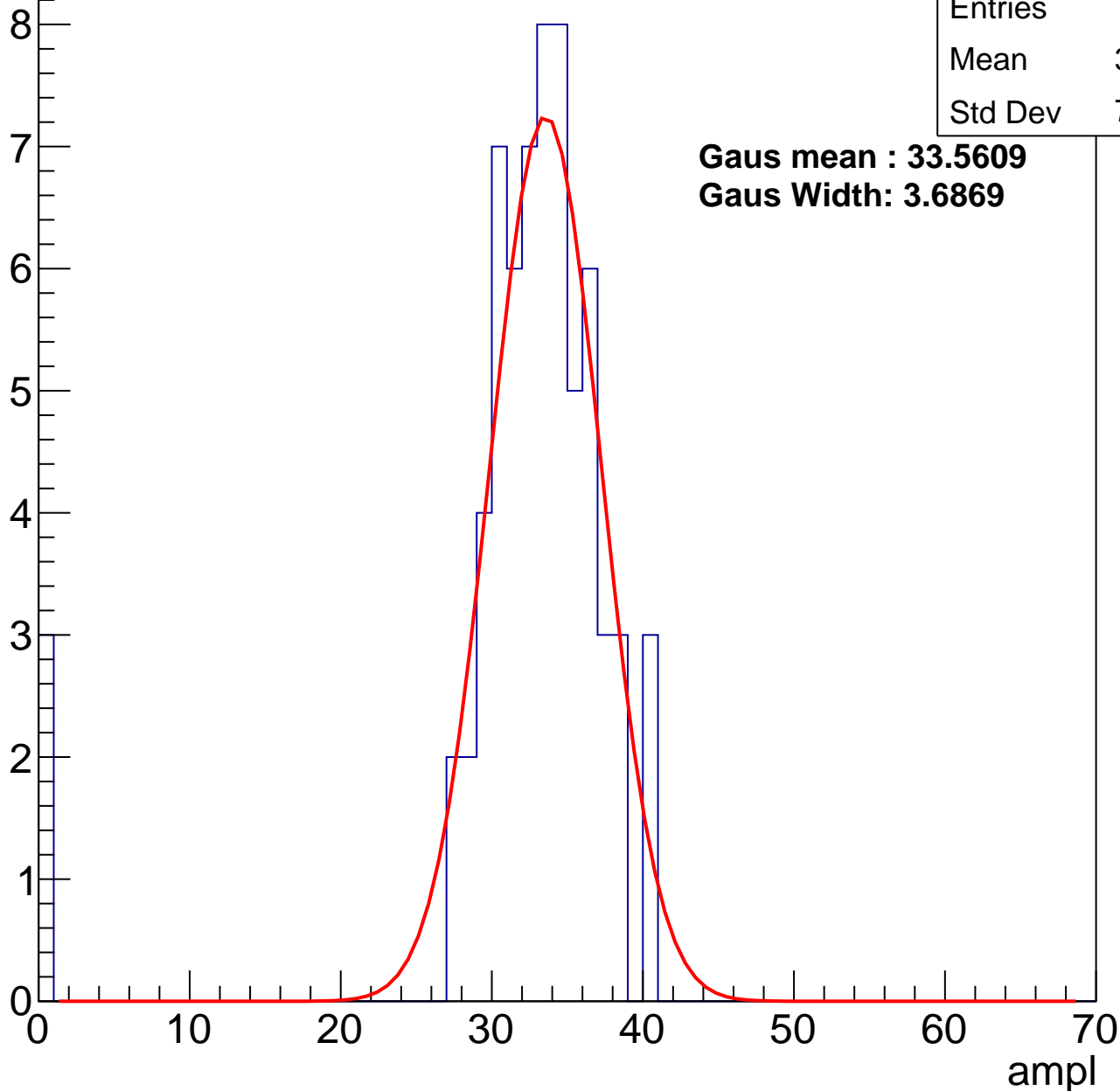
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	67
Mean	31.61
Std Dev	7.501

**Gaus mean : 33.5609**

**Gaus Width: 3.6869**



# B1L101S, U22-ch105, adc1

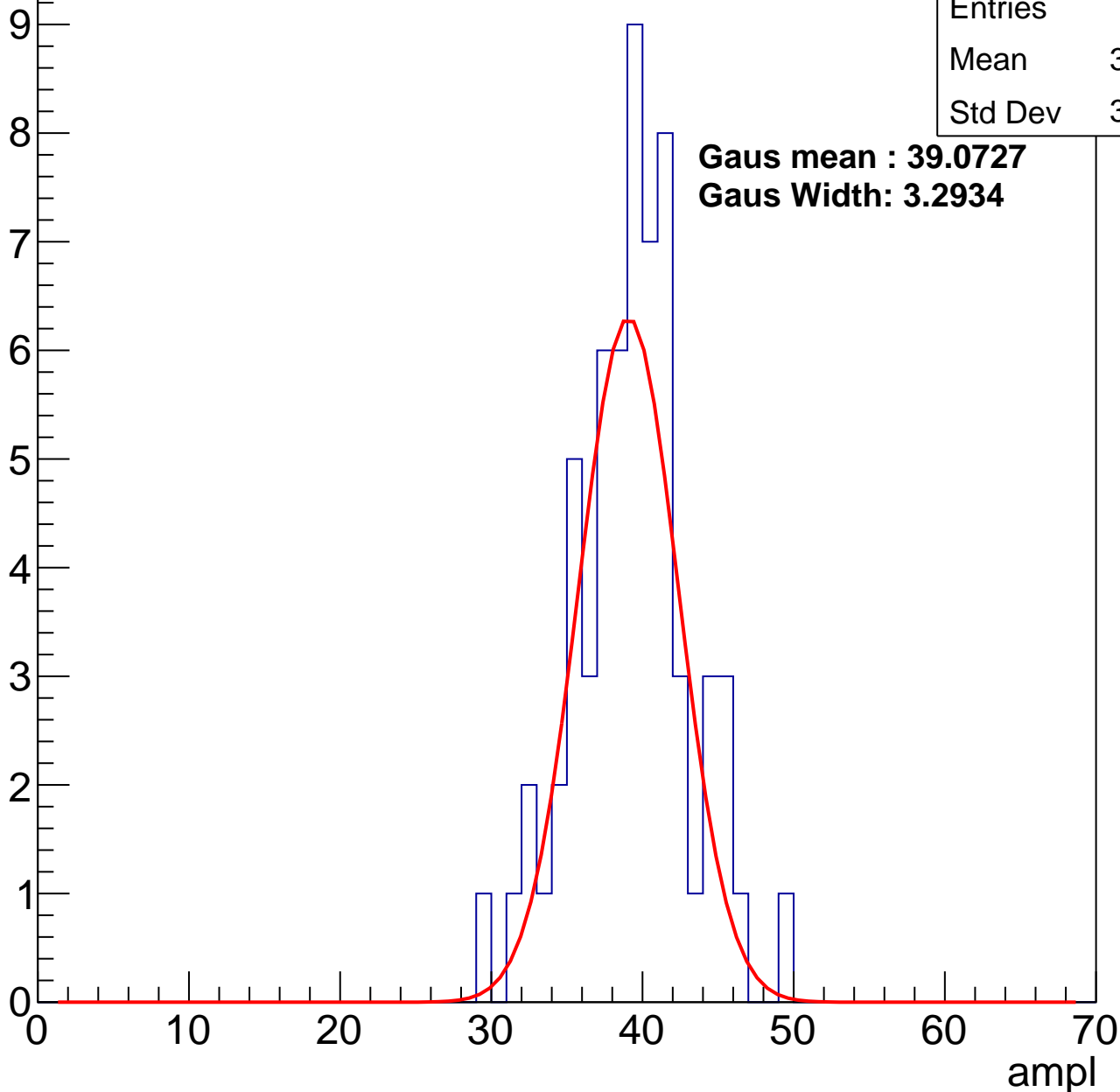
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	38.86
Std Dev	3.775

**Gaus mean : 39.0727**

**Gaus Width: 3.2934**



# B1L101S, U22-ch105, adc2

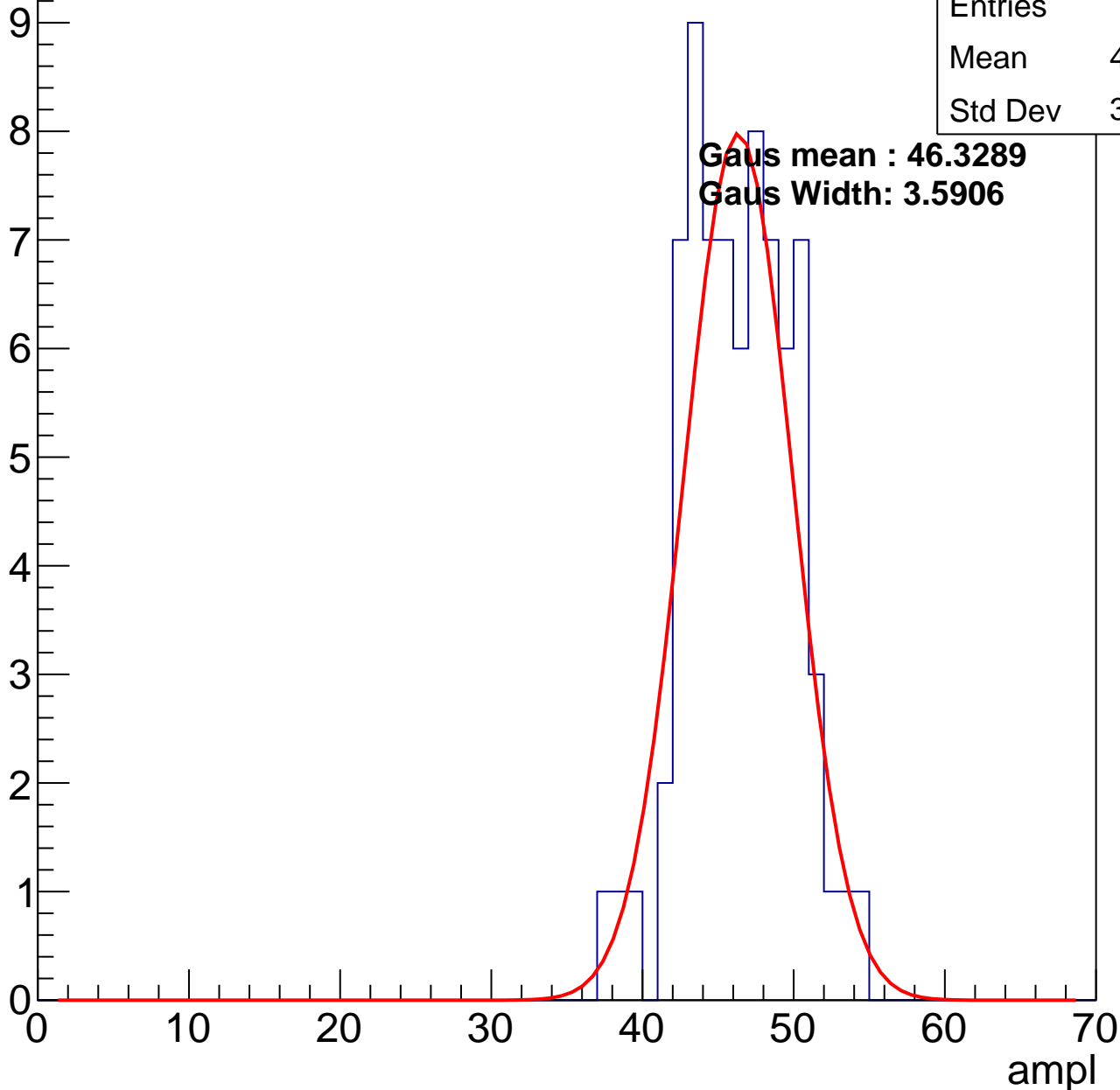
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	75
Mean	45.92
Std Dev	3.459

**Gaus mean : 46.3289**

**Gaus Width: 3.5906**

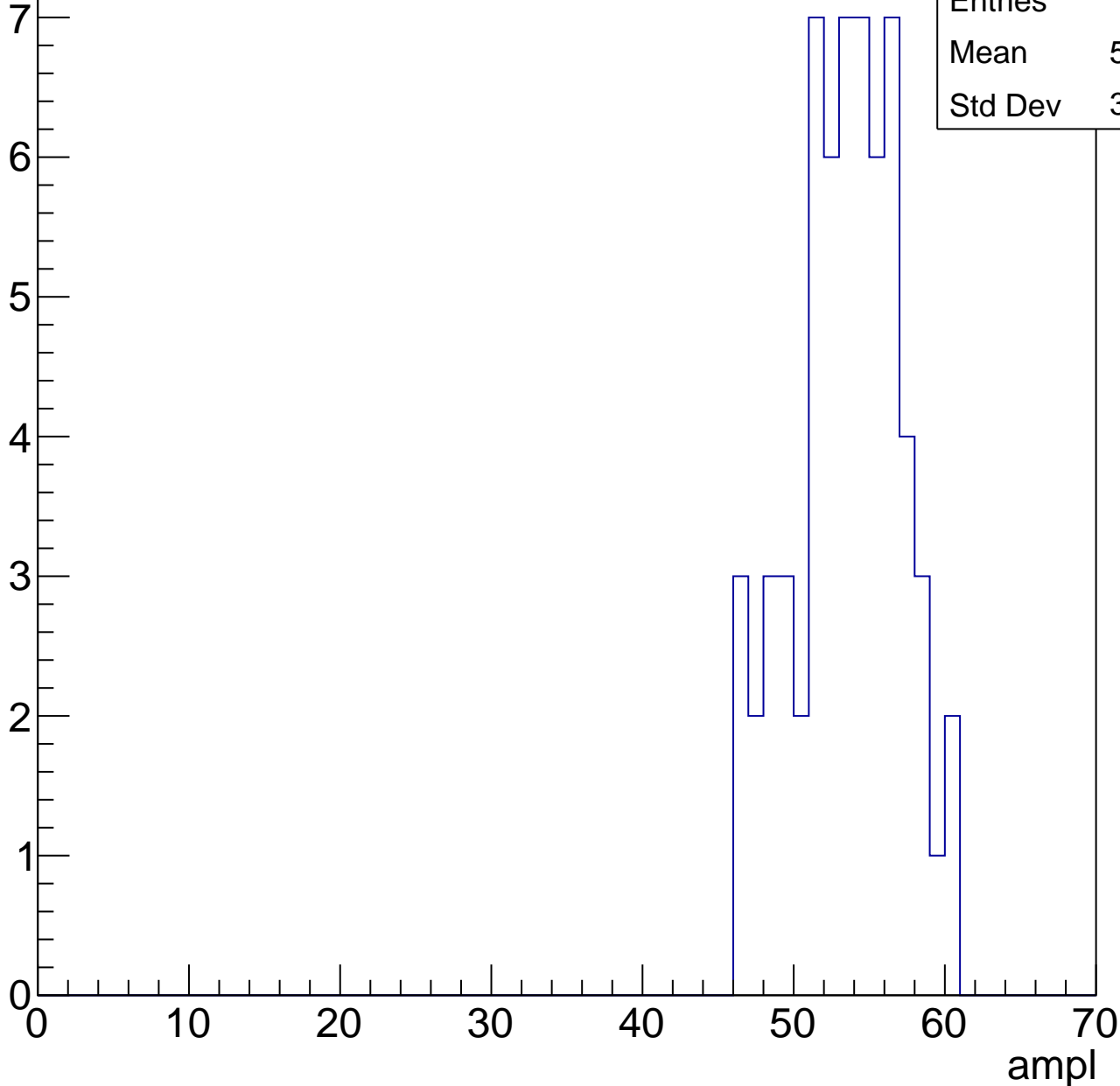


# B1L101S, U22-ch105, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	53.08
Std Dev	3.475

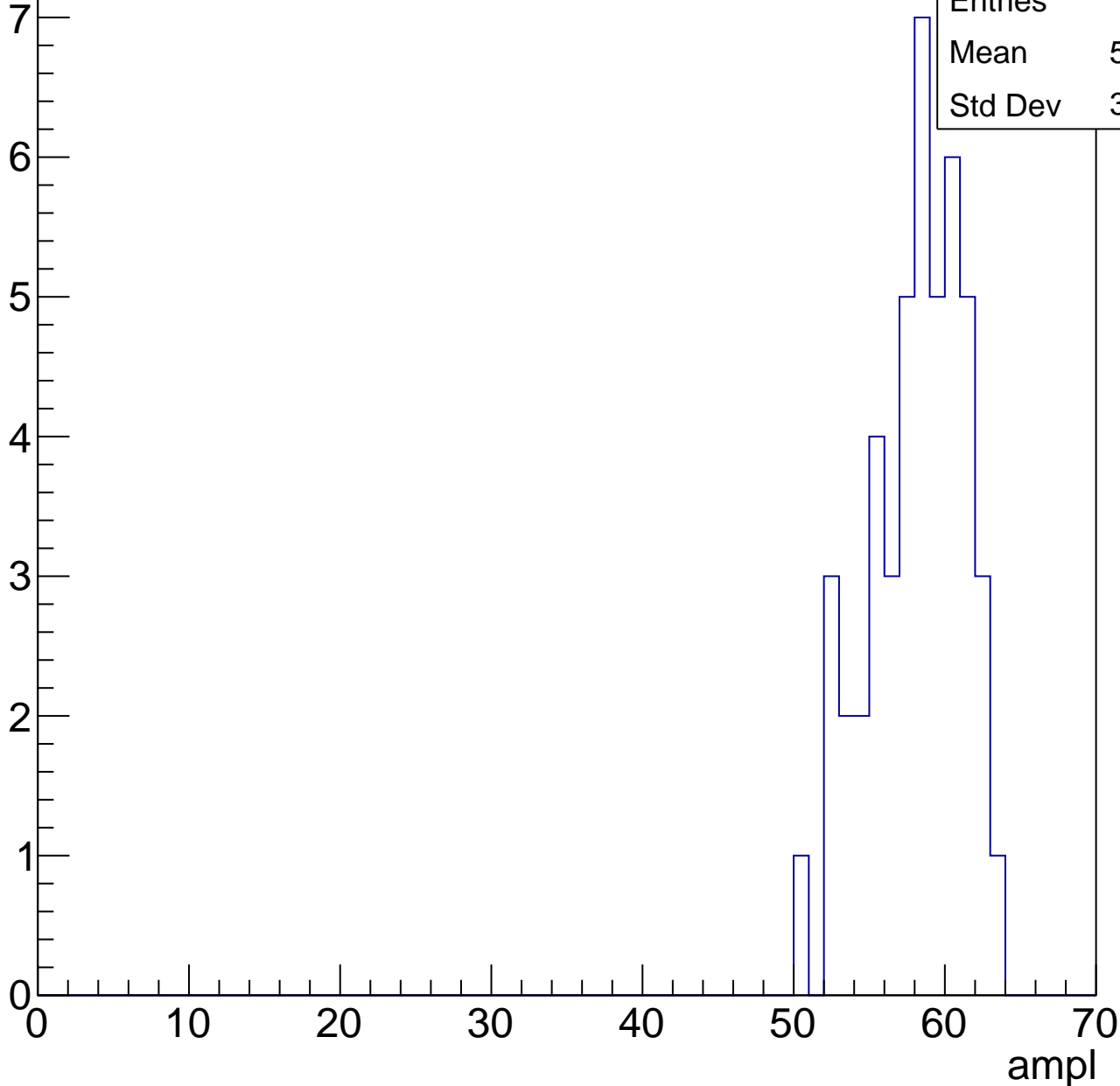


# B1L101S, U22-ch105, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	47
Mean	57.62
Std Dev	3.084

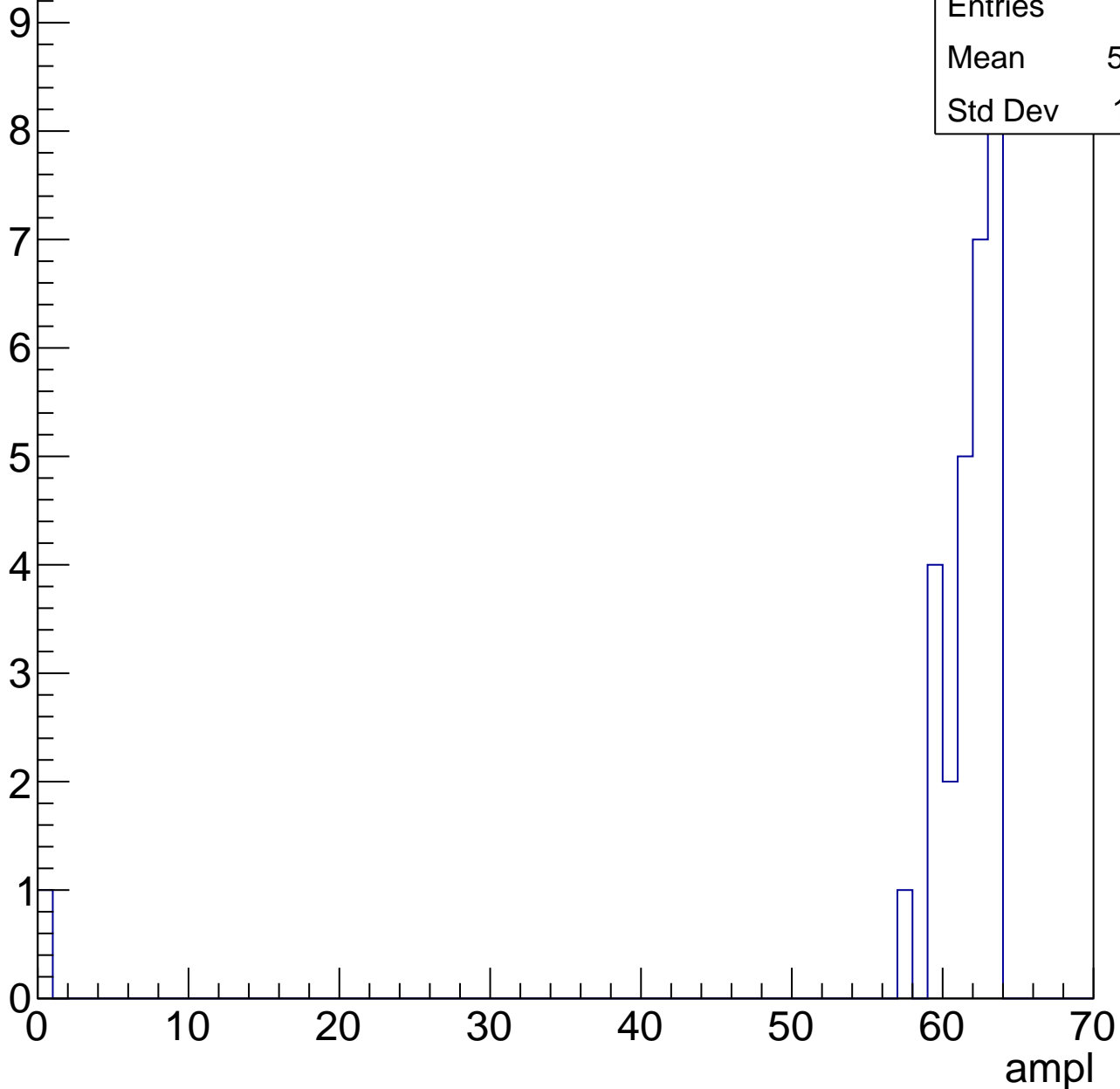


# B1L101S, U22-ch105, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	29
Mean	59.28
Std Dev	11.31



# B1L101S, U22-ch105, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



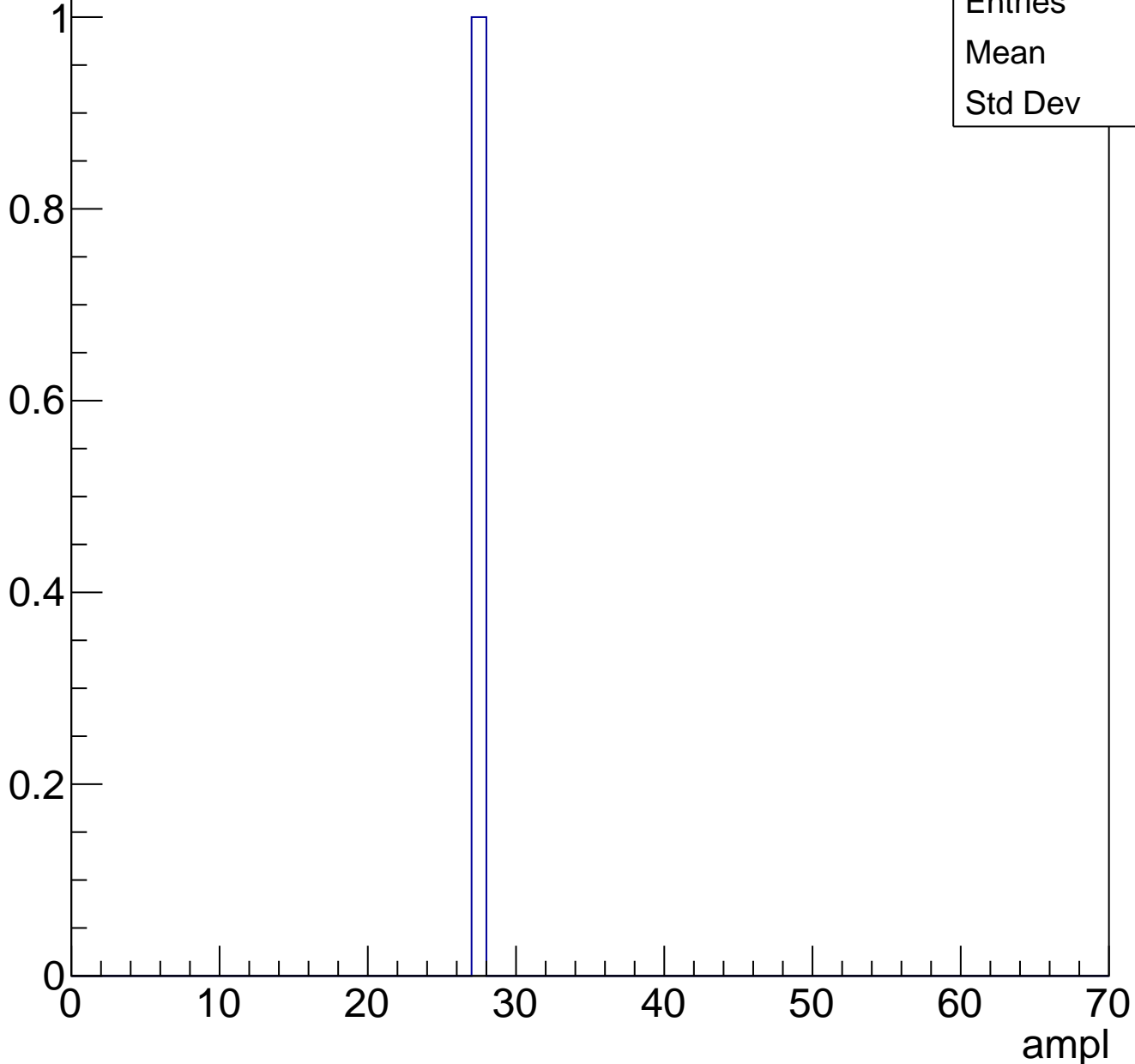
Entries	0
Mean	0
Std Dev	0



# B1L101S, U22-ch105, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	27
Std Dev	0

# B1L101S, U22-ch106, adc0

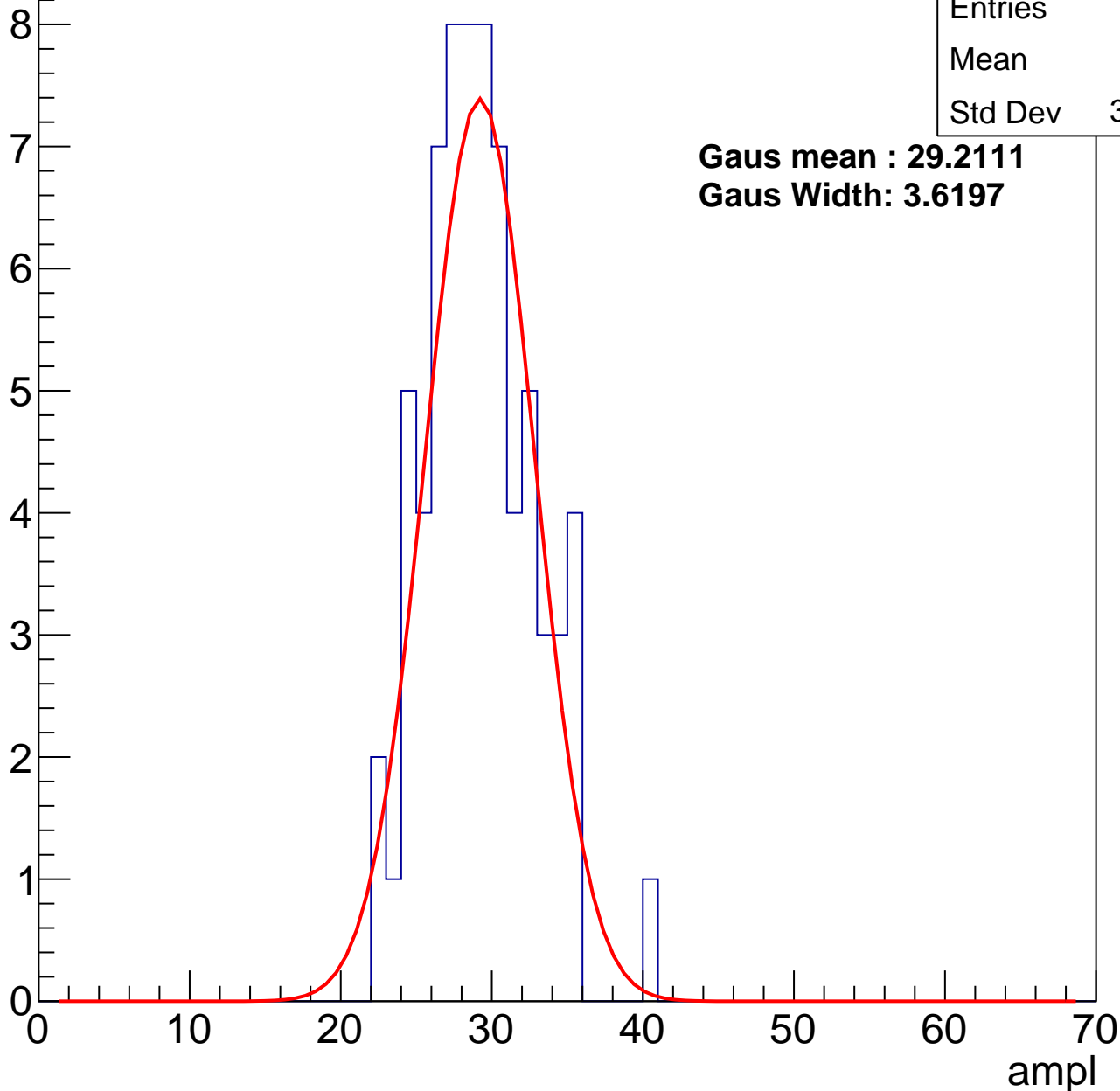
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	28.8
Std Dev	3.544

**Gaus mean : 29.2111**

**Gaus Width: 3.6197**



# B1L101S, U22-ch106, adc1

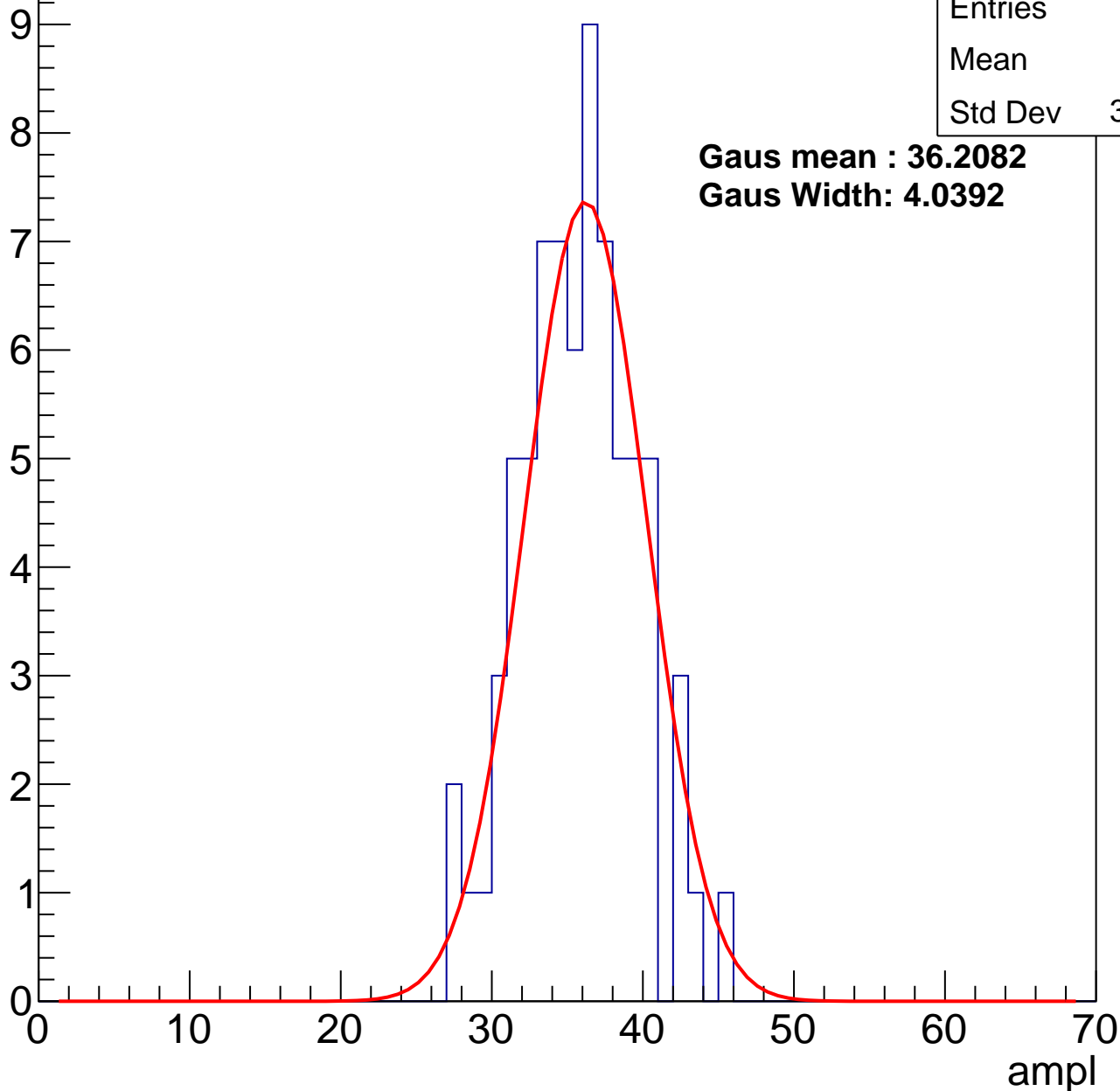
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	73
Mean	35.3
Std Dev	3.773

**Gaus mean : 36.2082**

**Gaus Width: 4.0392**



# B1L101S, U22-ch106, adc2

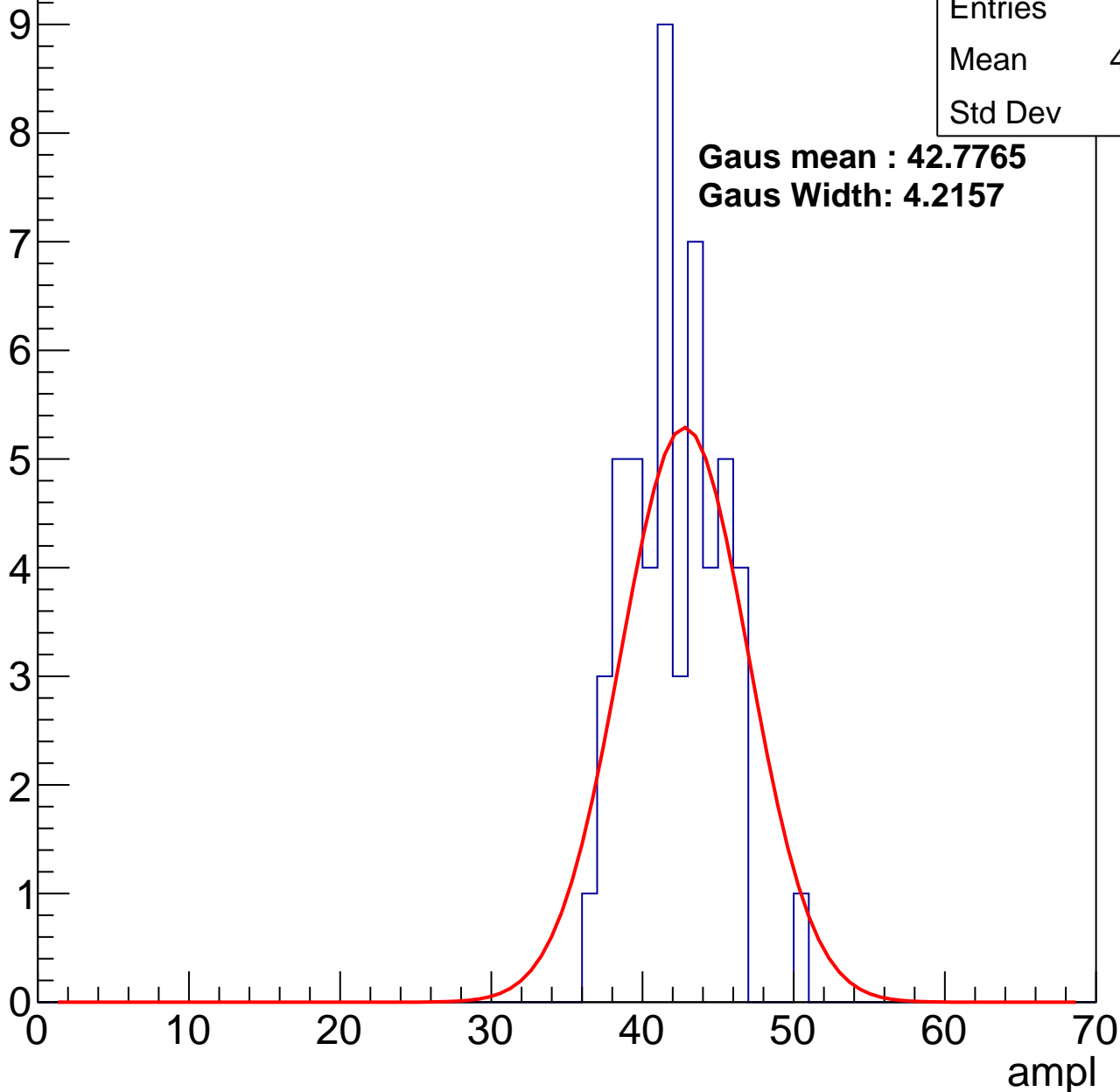
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	51
Mean	41.63
Std Dev	2.97

**Gaus mean : 42.7765**

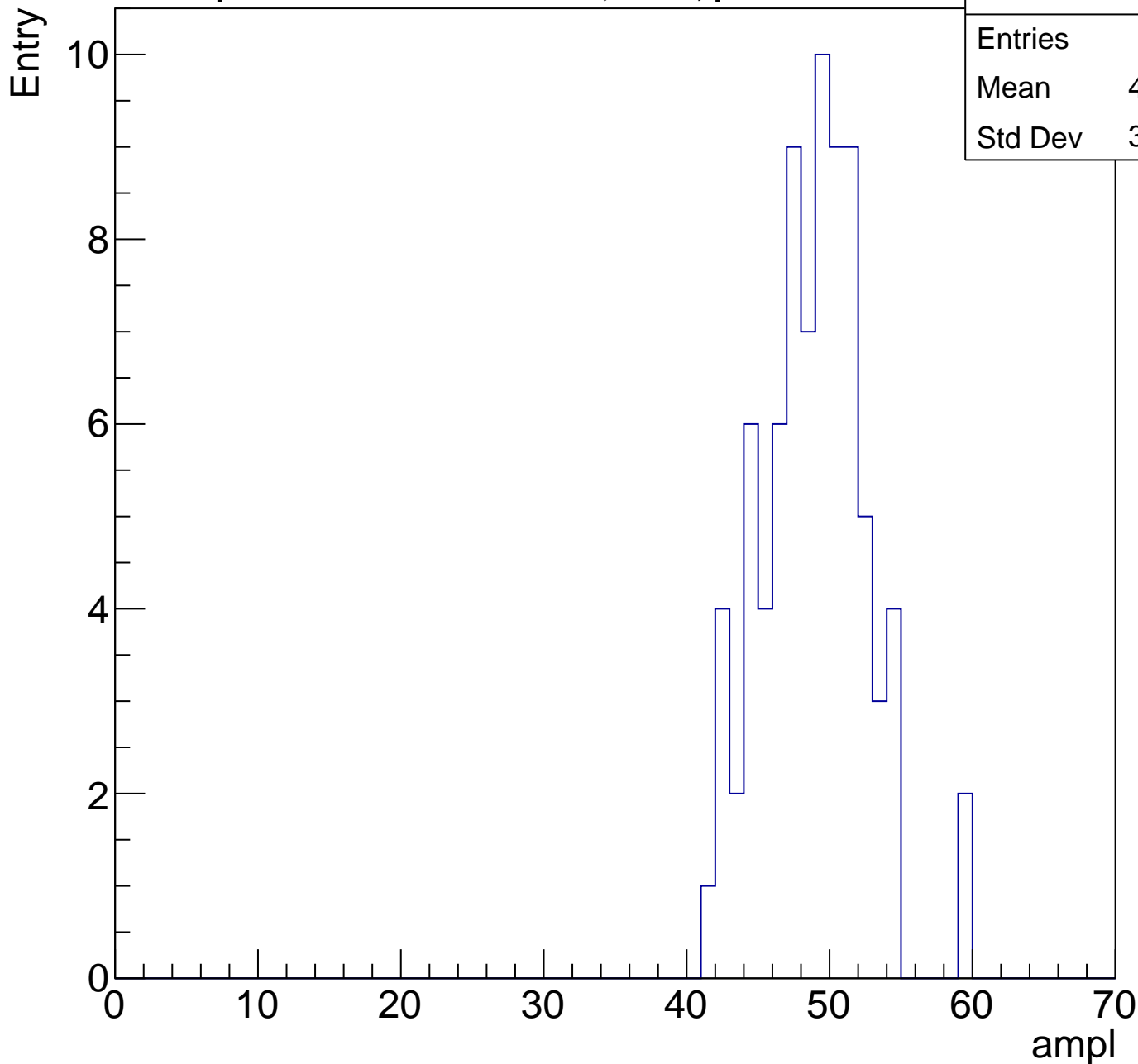
**Gaus Width: 4.2157**



# B1L101S, U22-ch106, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	81
Mean	48.47
Std Dev	3.614

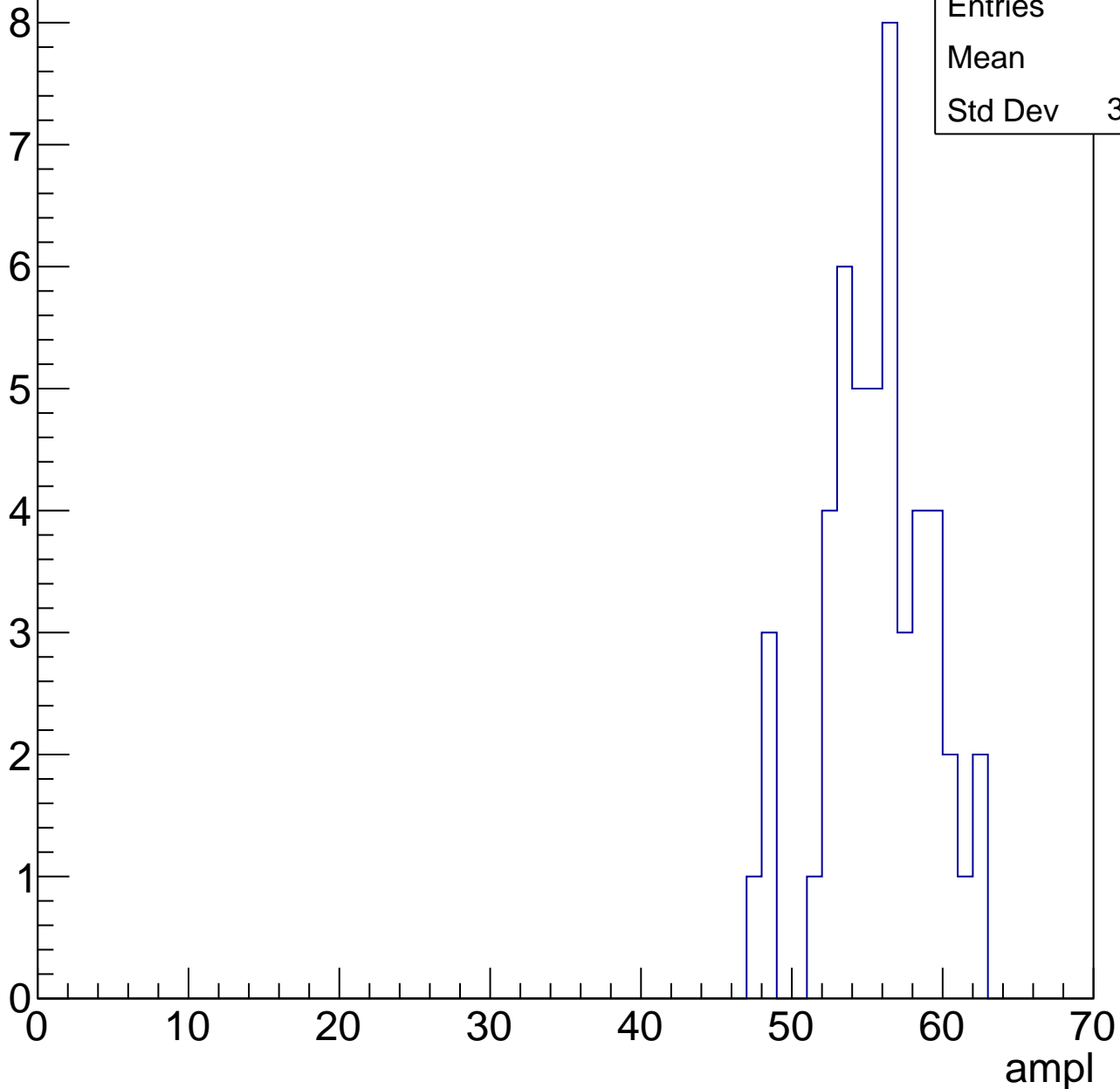


# B1L101S, U22-ch106, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	49
Mean	55.2
Std Dev	3.482

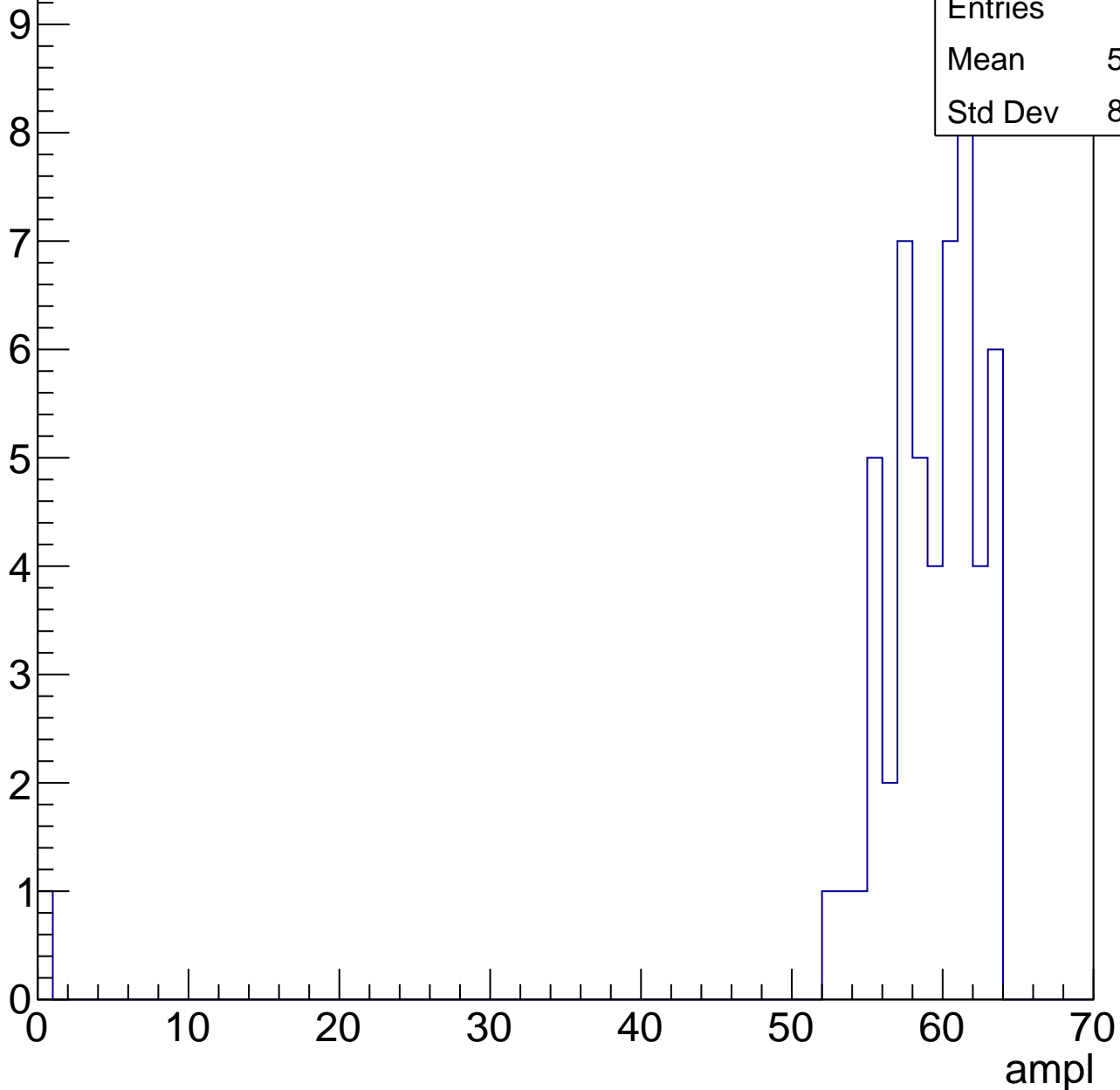


# B1L101S, U22-ch106, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

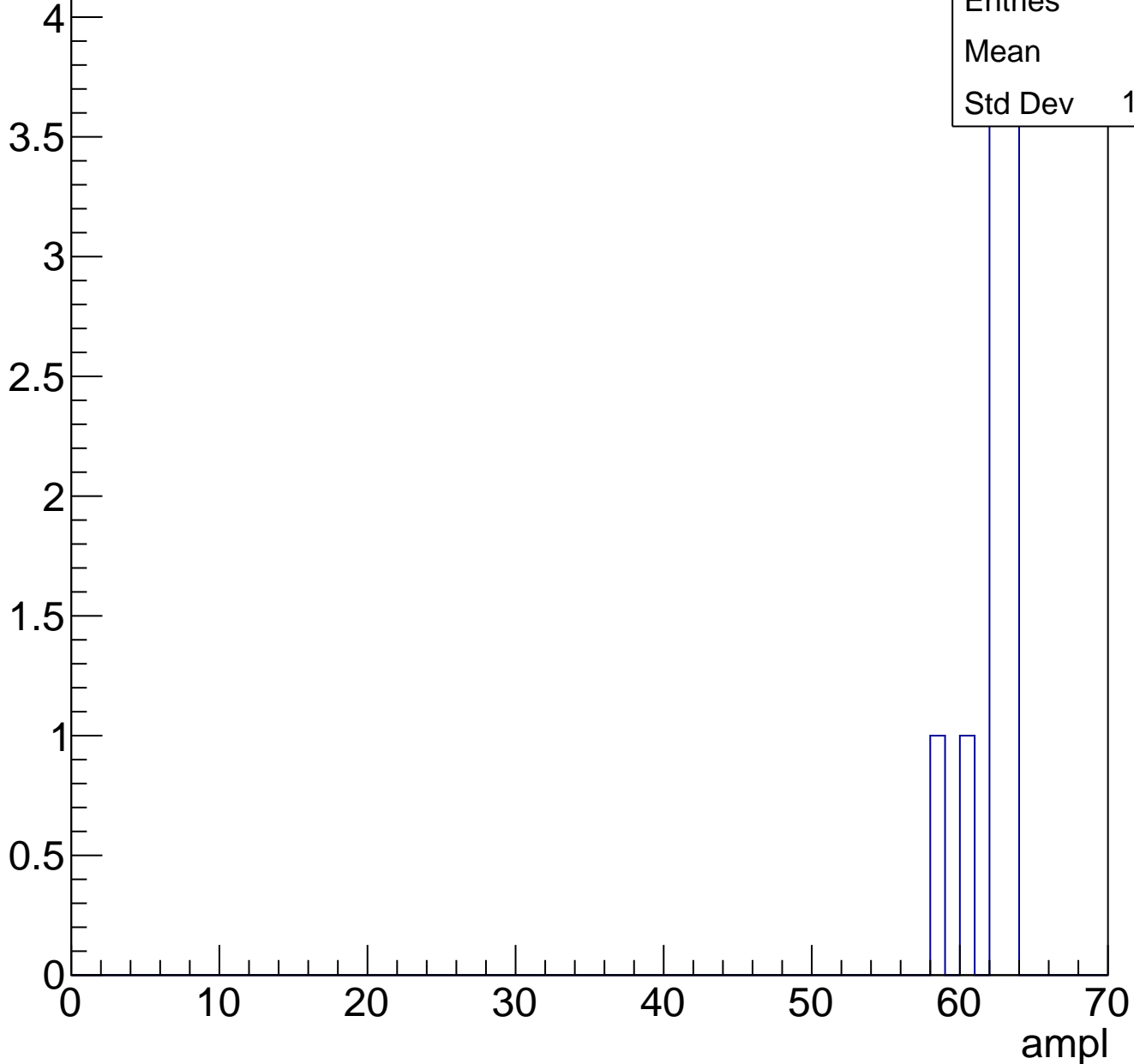
Entries	53
Mean	57.85
Std Dev	8.497



# B1L101S, U22-ch106, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	10
Mean	61.8
Std Dev	1.536



# B1L101S, U22-ch106, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U22-ch107, adc0

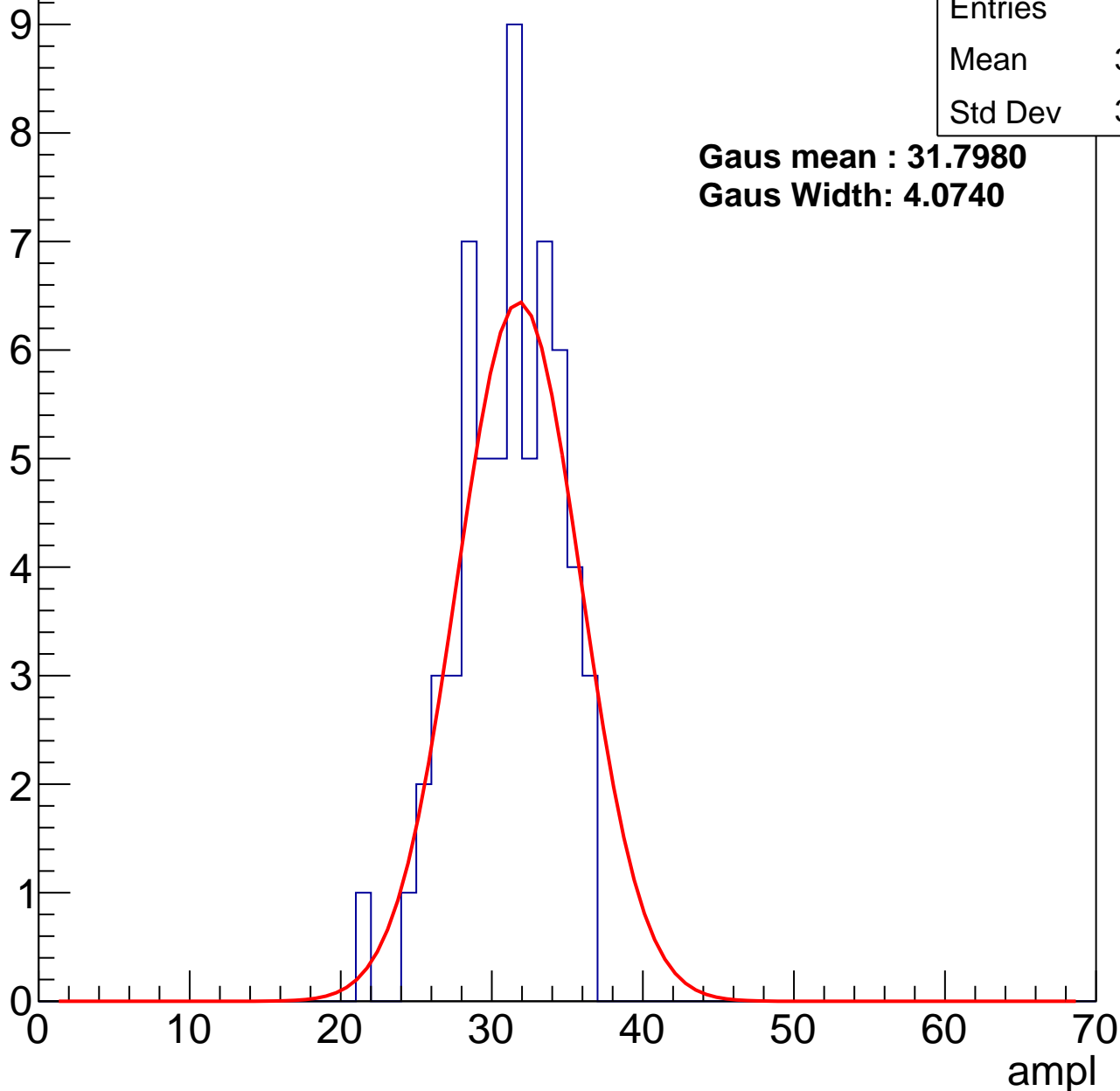
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	30.61
Std Dev	3.261

**Gaus mean : 31.7980**

**Gaus Width: 4.0740**



# B1L101S, U22-ch107, adc1

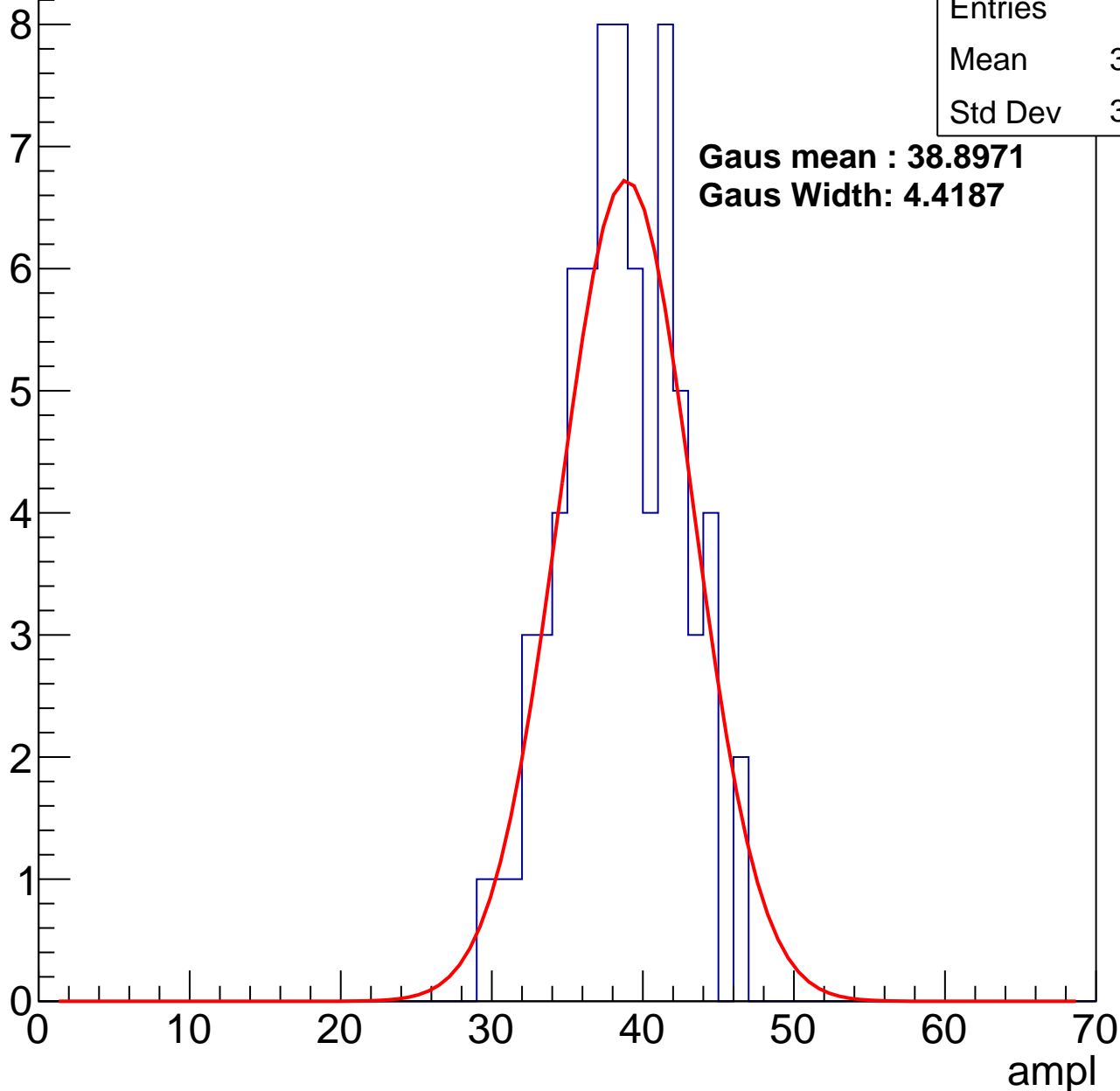
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	73
Mean	38.03
Std Dev	3.789

**Gaus mean : 38.8971**

**Gaus Width: 4.4187**



# B1L101S, U22-ch107, adc2

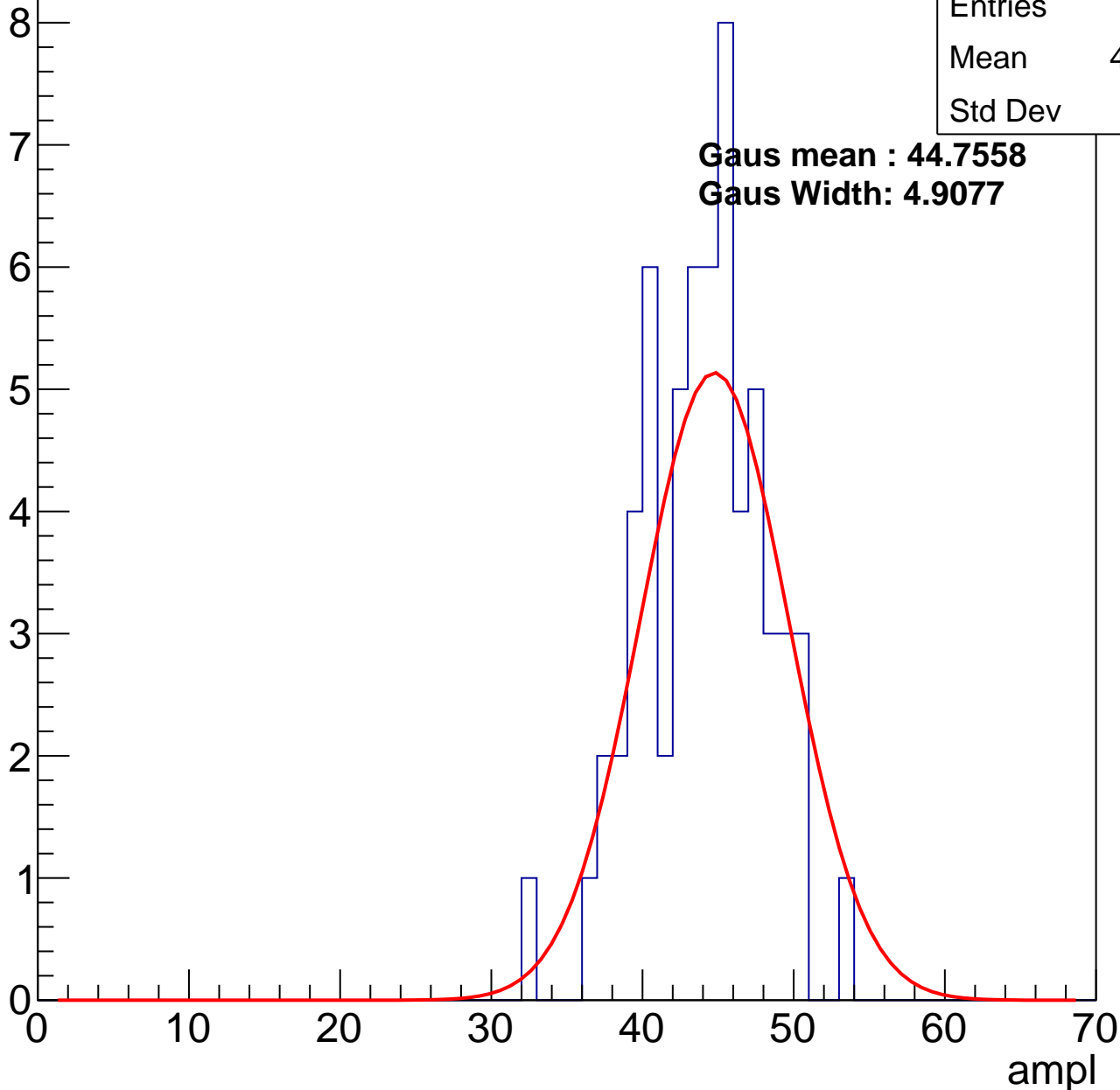
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	43.56
Std Dev	3.99

**Gaus mean : 44.7558**

**Gaus Width: 4.9077**

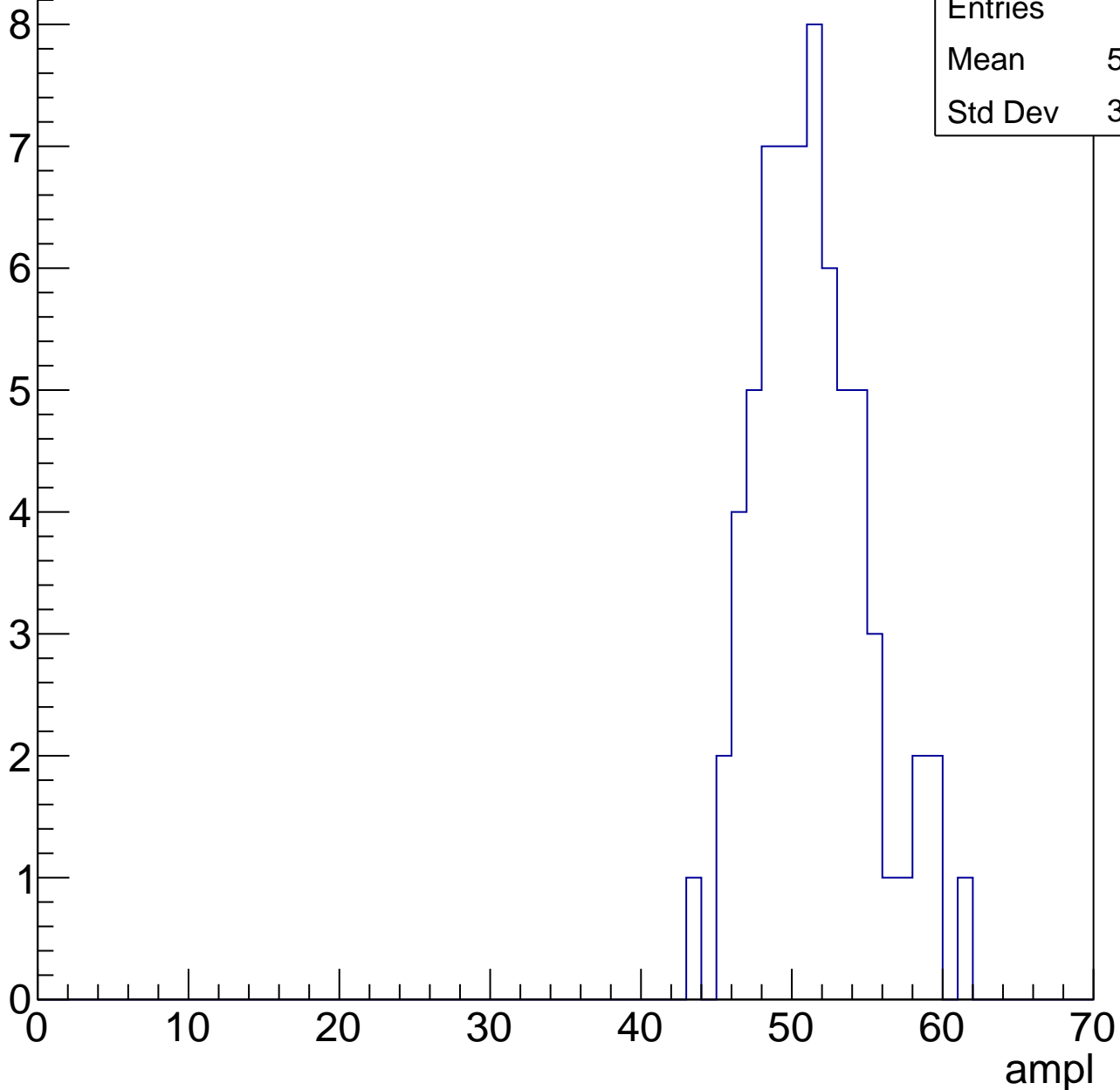


# B1L101S, U22-ch107, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	67
Mean	50.88
Std Dev	3.704



# B1L101S, U22-ch107, adc4

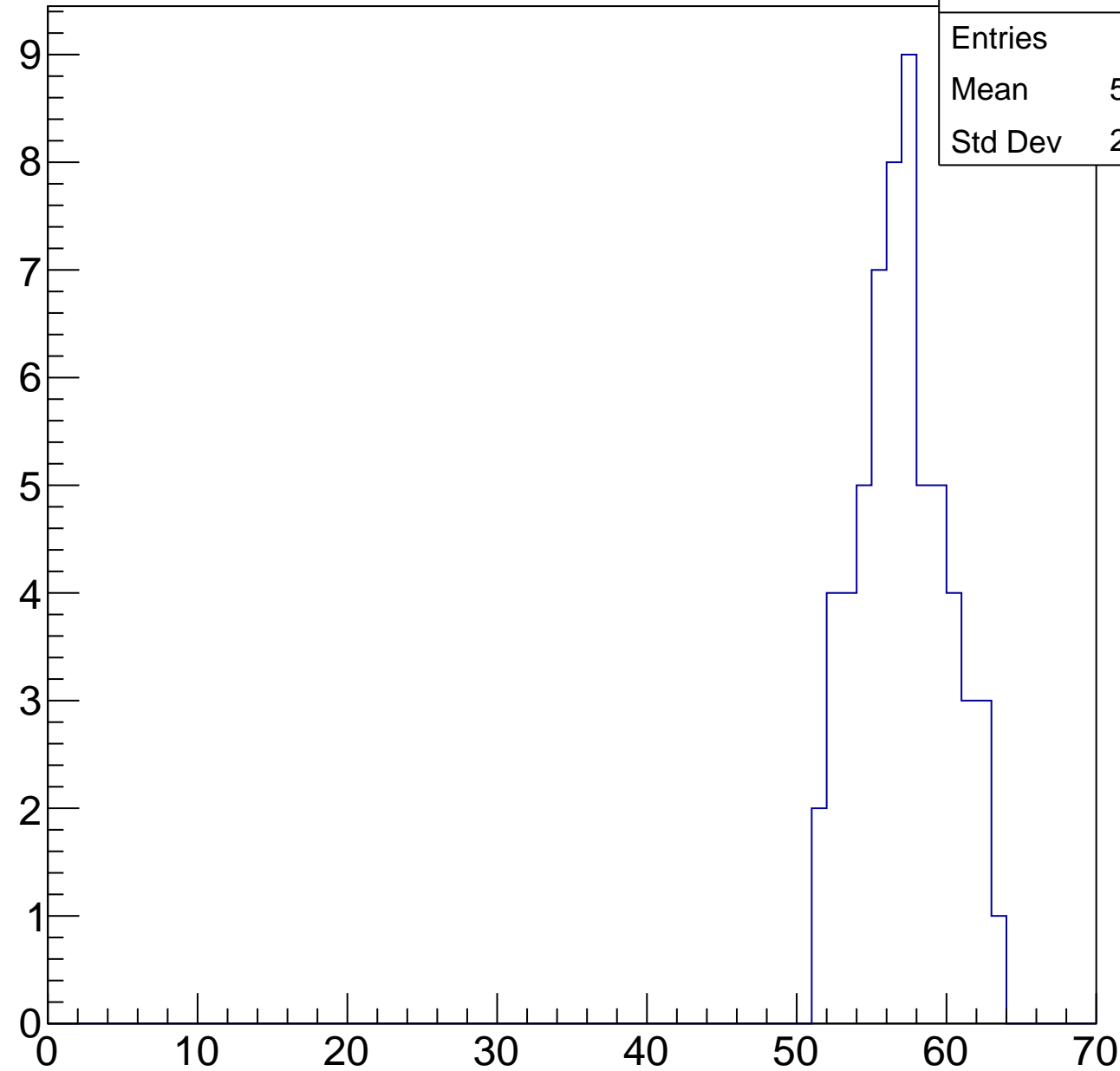
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	60
Mean	56.58
Std Dev	2.962

ampl

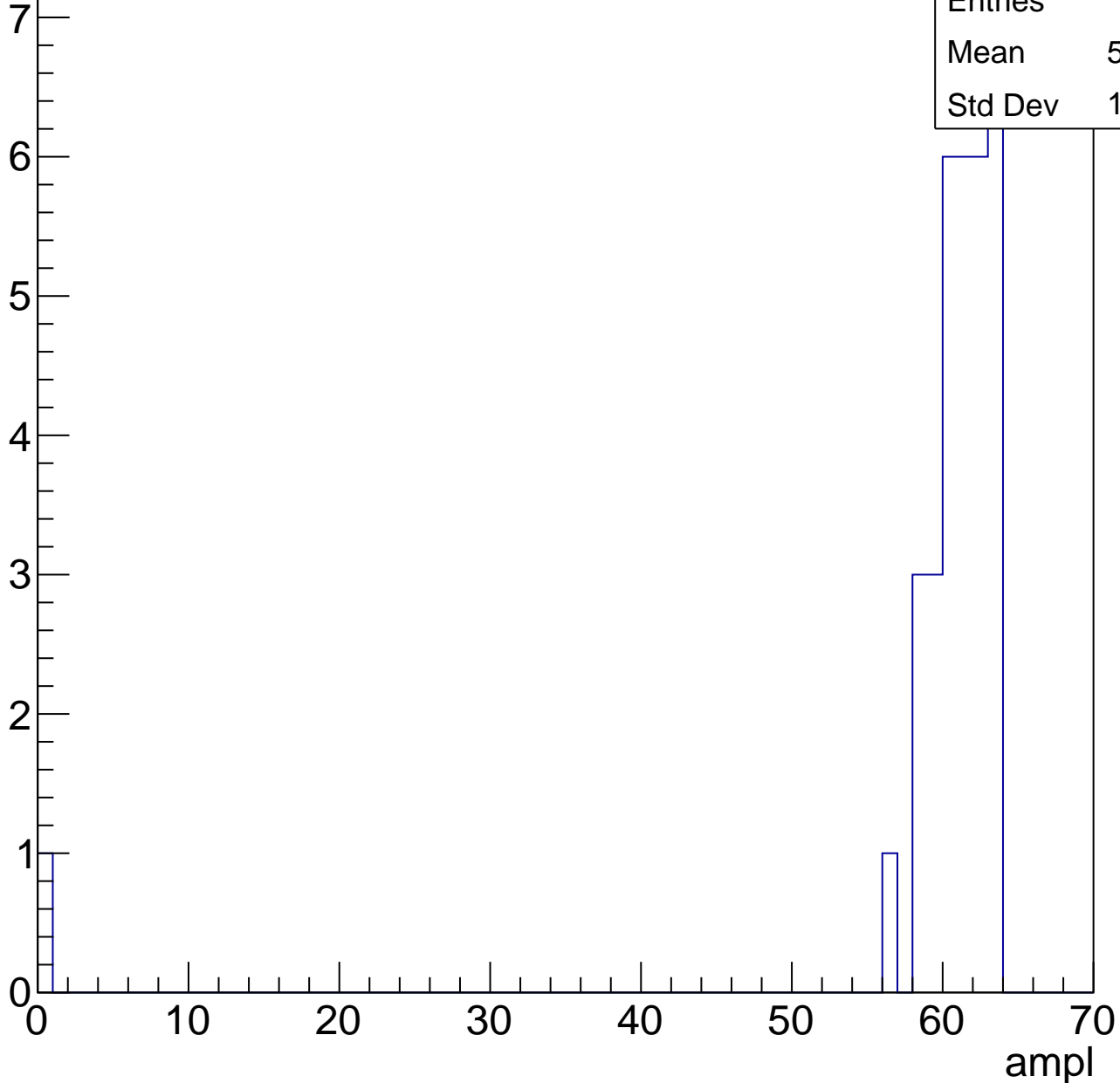


# B1L101S, U22-ch107, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	33
Mean	58.97
Std Dev	10.57



# B1L101S, U22-ch107, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

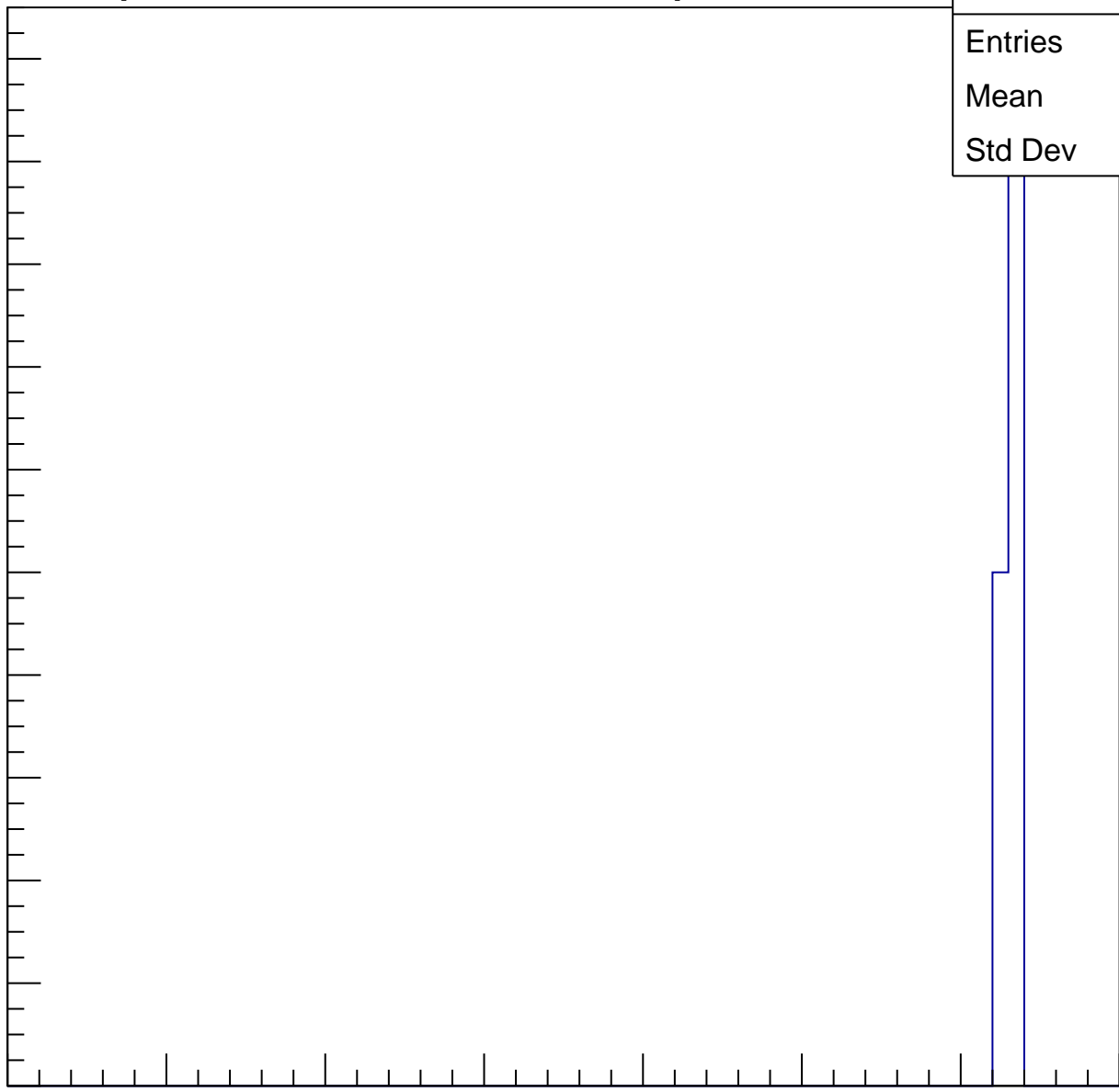
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	3
Mean	62.67
Std Dev	0.4714

ampl

0 10 20 30 40 50 60 70





# B1L101S, U22-ch107, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U22-ch108, adc0

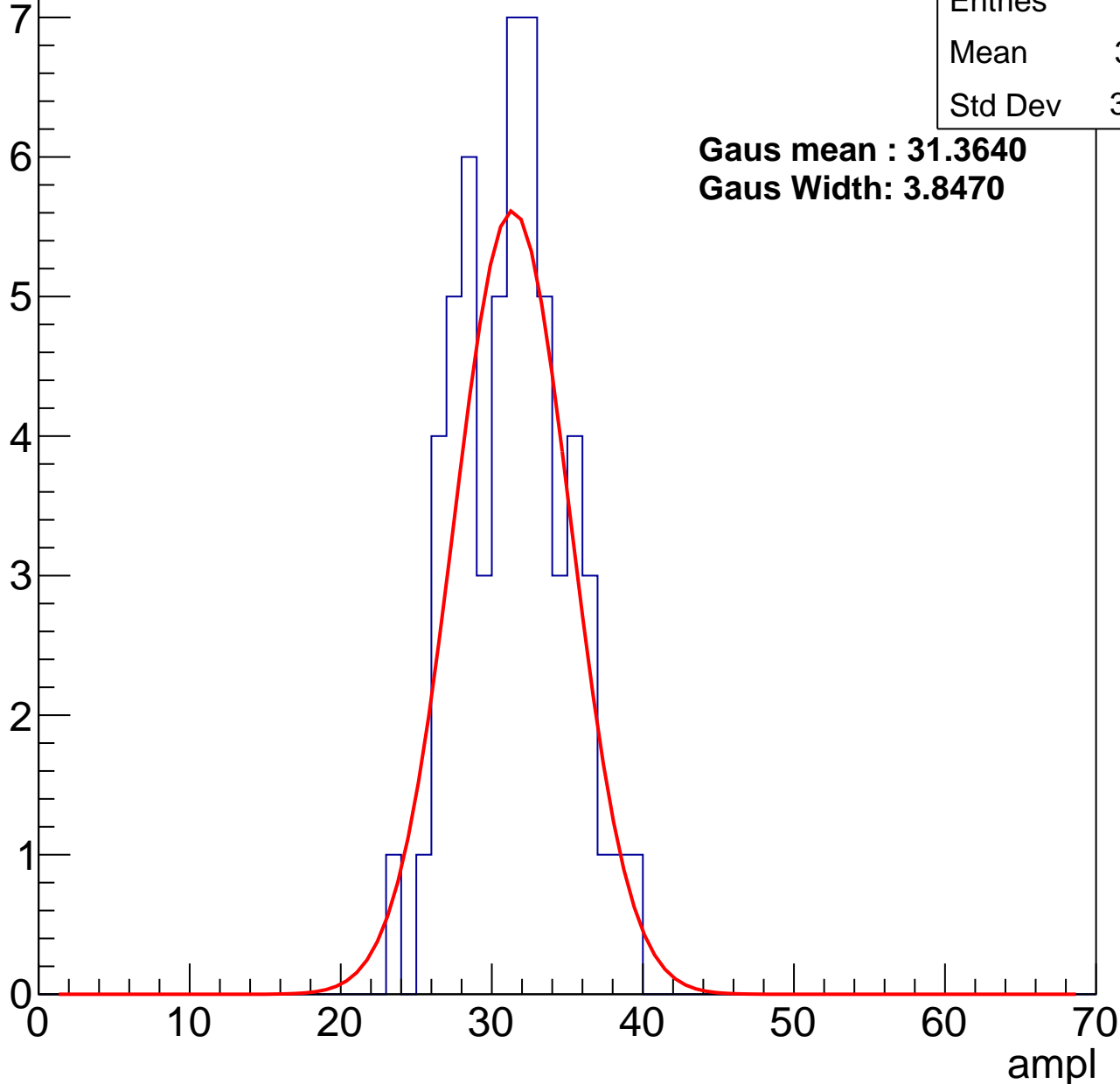
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	57
Mean	30.91
Std Dev	3.486

**Gaus mean : 31.3640**

**Gaus Width: 3.8470**



# B1L101S, U22-ch108, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	78
Mean	37.42
Std Dev	3.597

**Gaus mean : 38.0974**

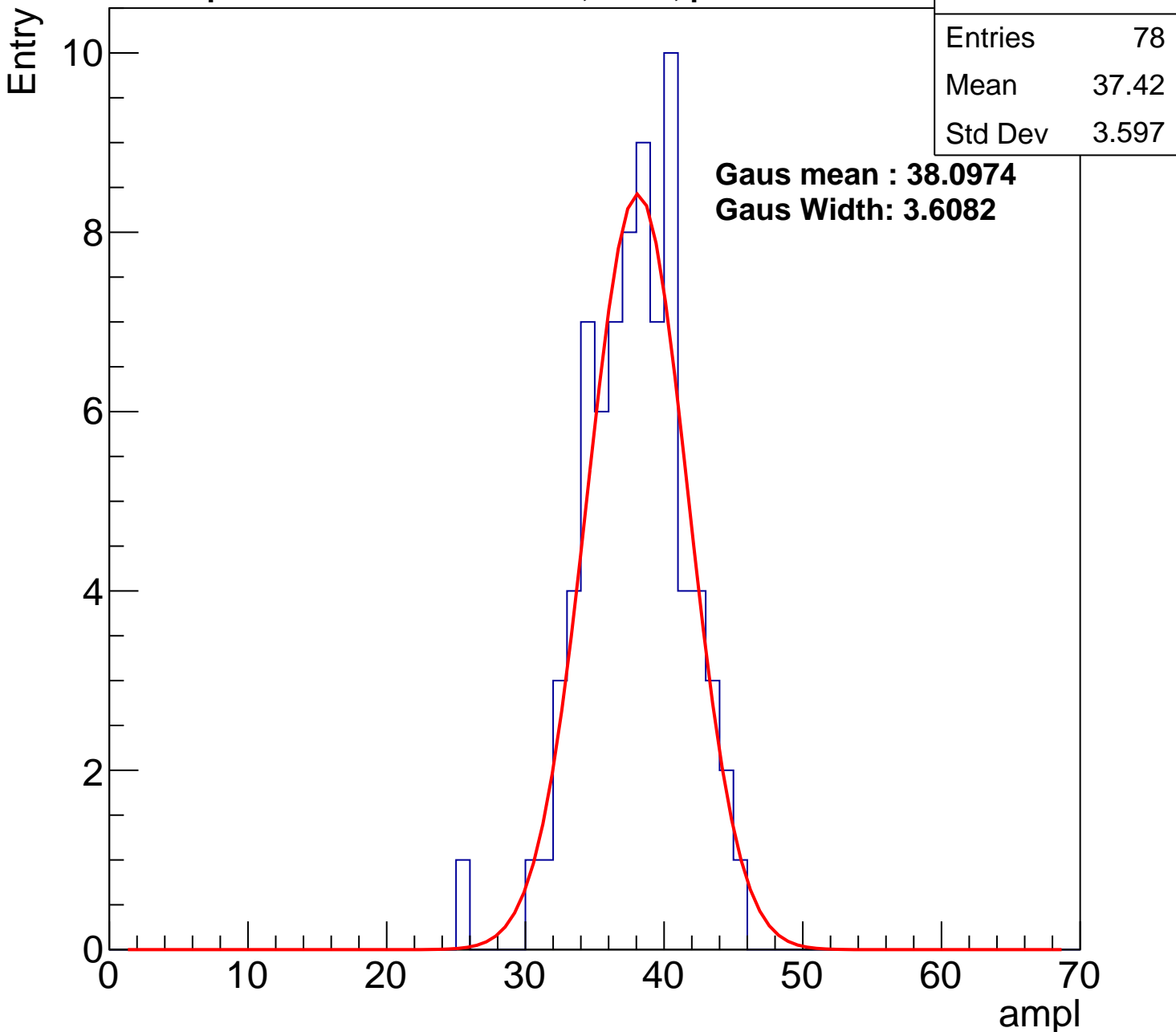
**Gaus Width: 3.6082**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B1L101S, U22-ch108, adc2

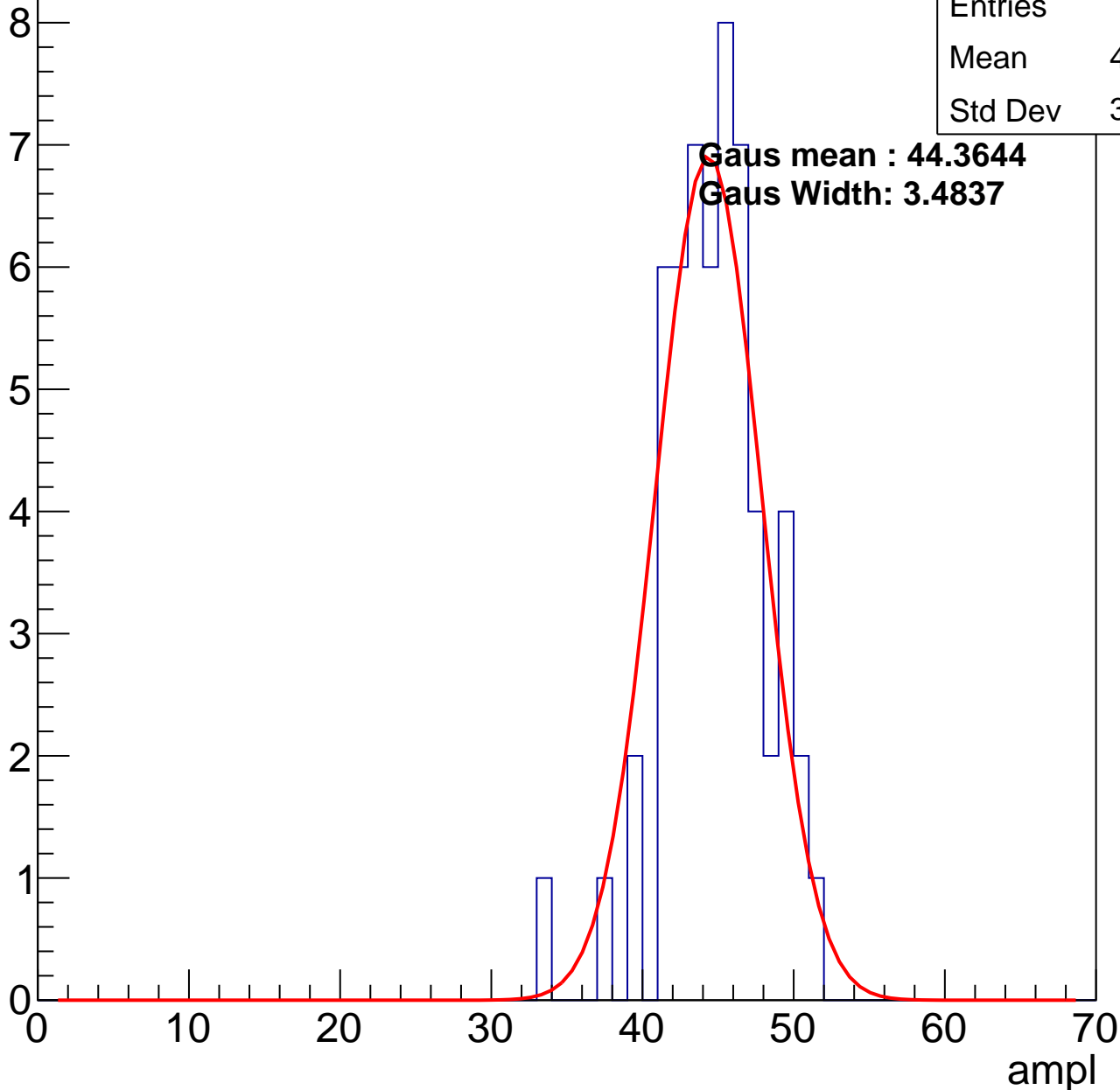
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	57
Mean	44.28
Std Dev	3.313

Gaus mean : 44.3644

Gaus Width: 3.4837

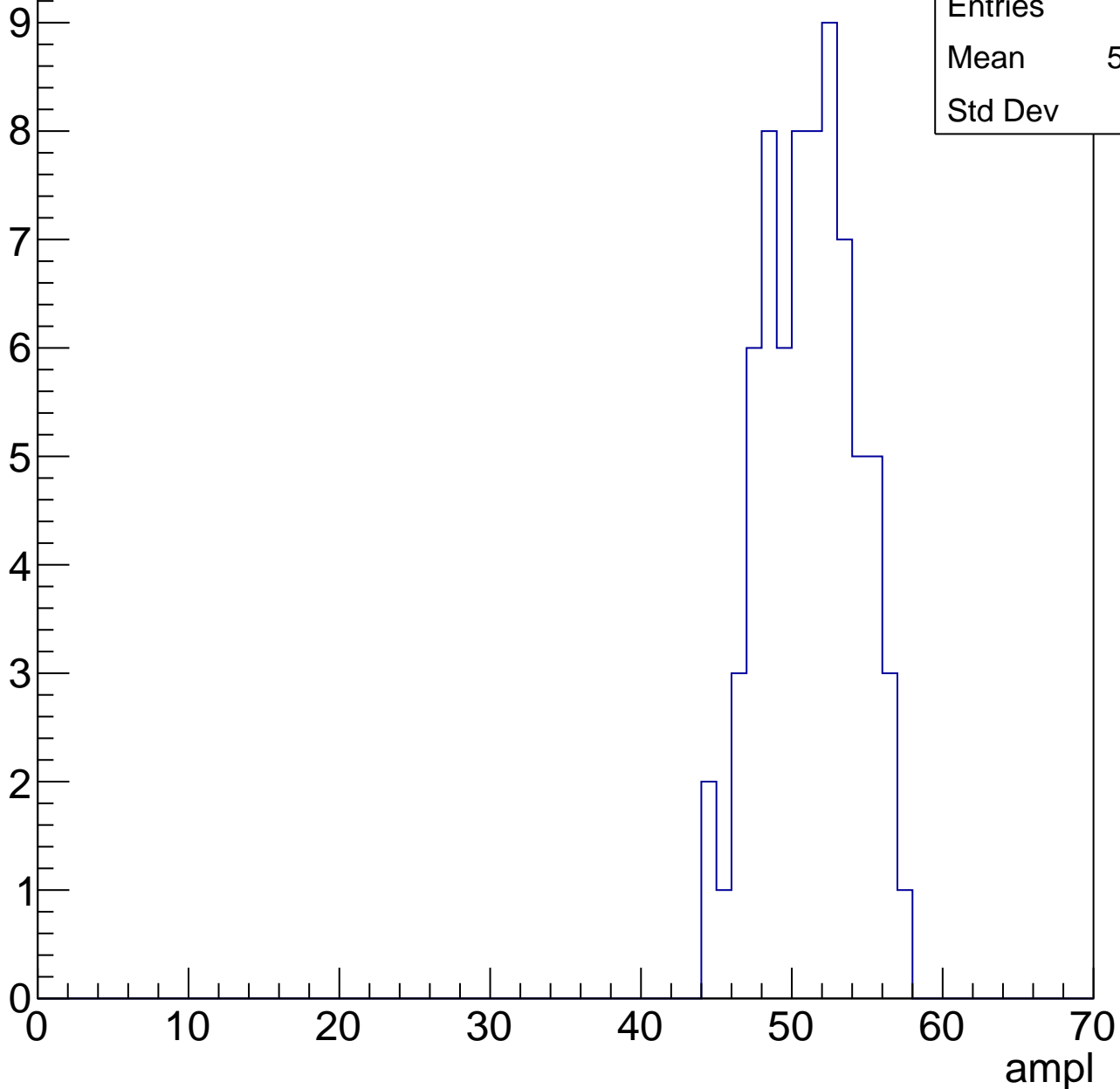


# B1L101S, U22-ch108, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	72
Mean	50.67
Std Dev	3.06

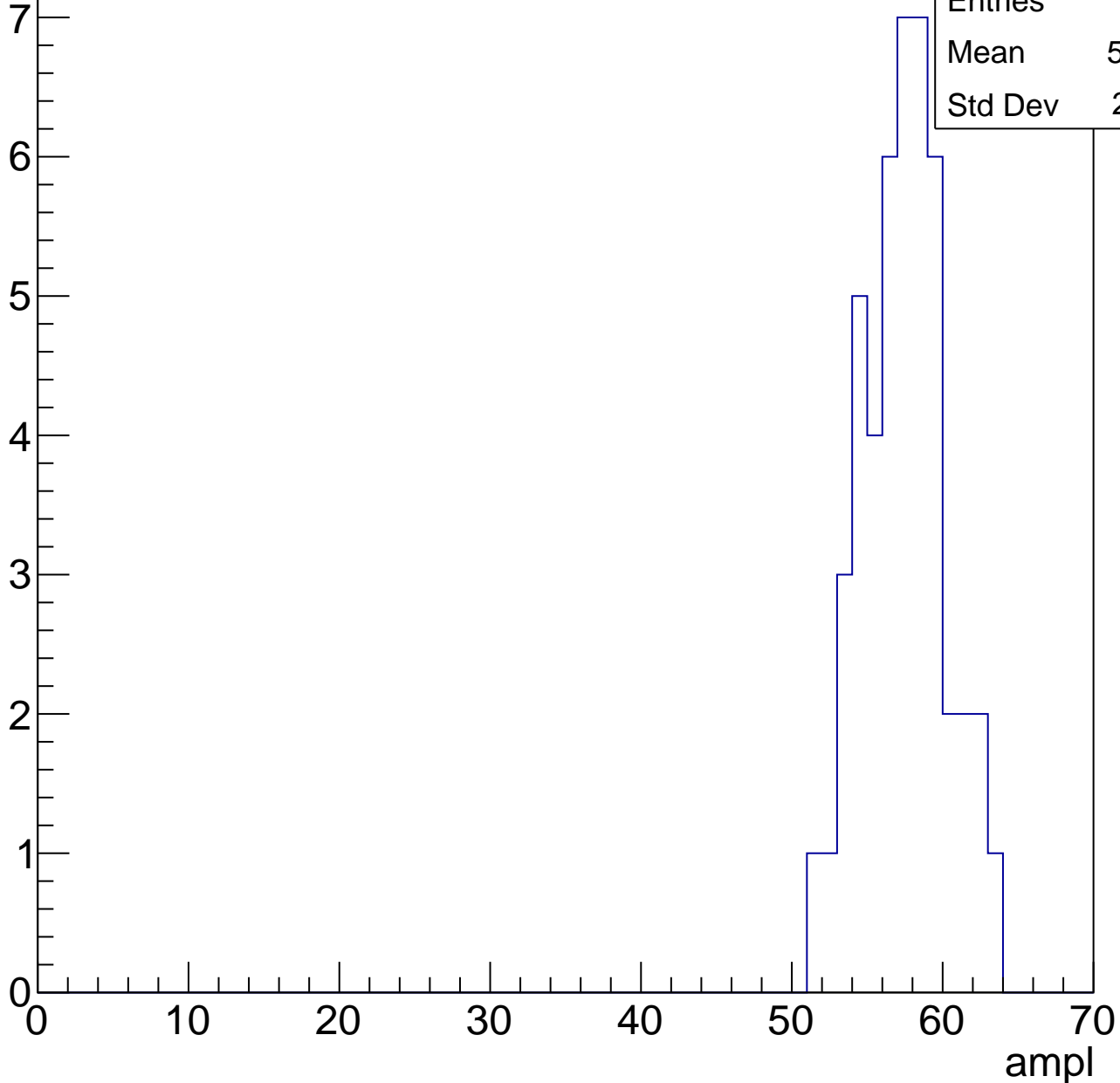


# B1L101S, U22-ch108, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	47
Mean	56.94
Std Dev	2.701



# B1L101S, U22-ch108, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

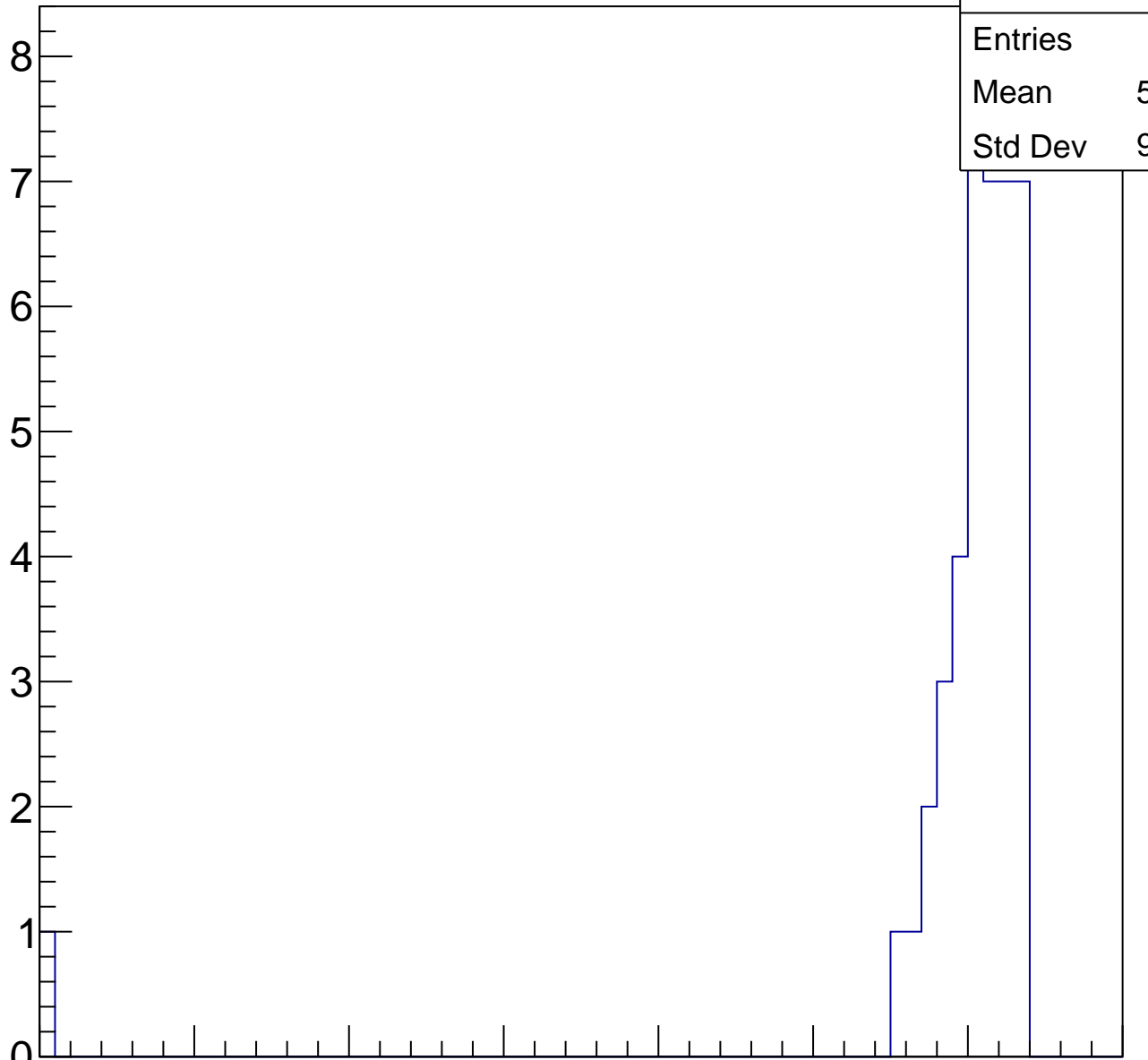
Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	41
Mean	58.95
Std Dev	9.535

ampl

0 10 20 30 40 50 60 70



# B1L101S, U22-ch108, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	4
Mean	62.25
Std Dev	0.8292

ampl

0 10 20 30 40 50 60 70



# B1L101S, U22-ch108, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U22-ch109, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	55
Mean	31.27
Std Dev	3.182

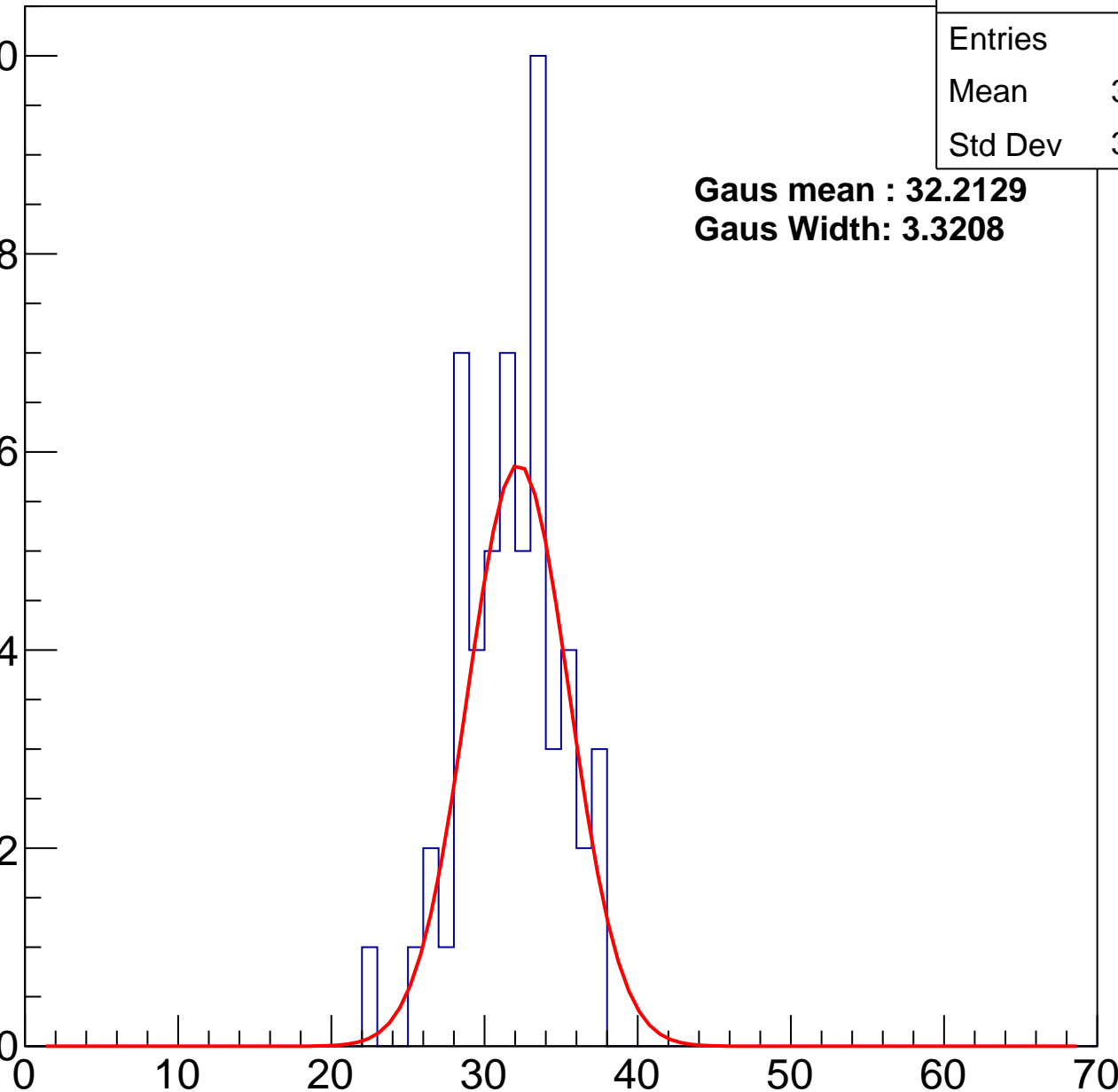
**Gaus mean : 32.2129**

**Gaus Width: 3.3208**

Entry

10  
8  
6  
4  
2  
0

ampl



# B1L101S, U22-ch109, adc1

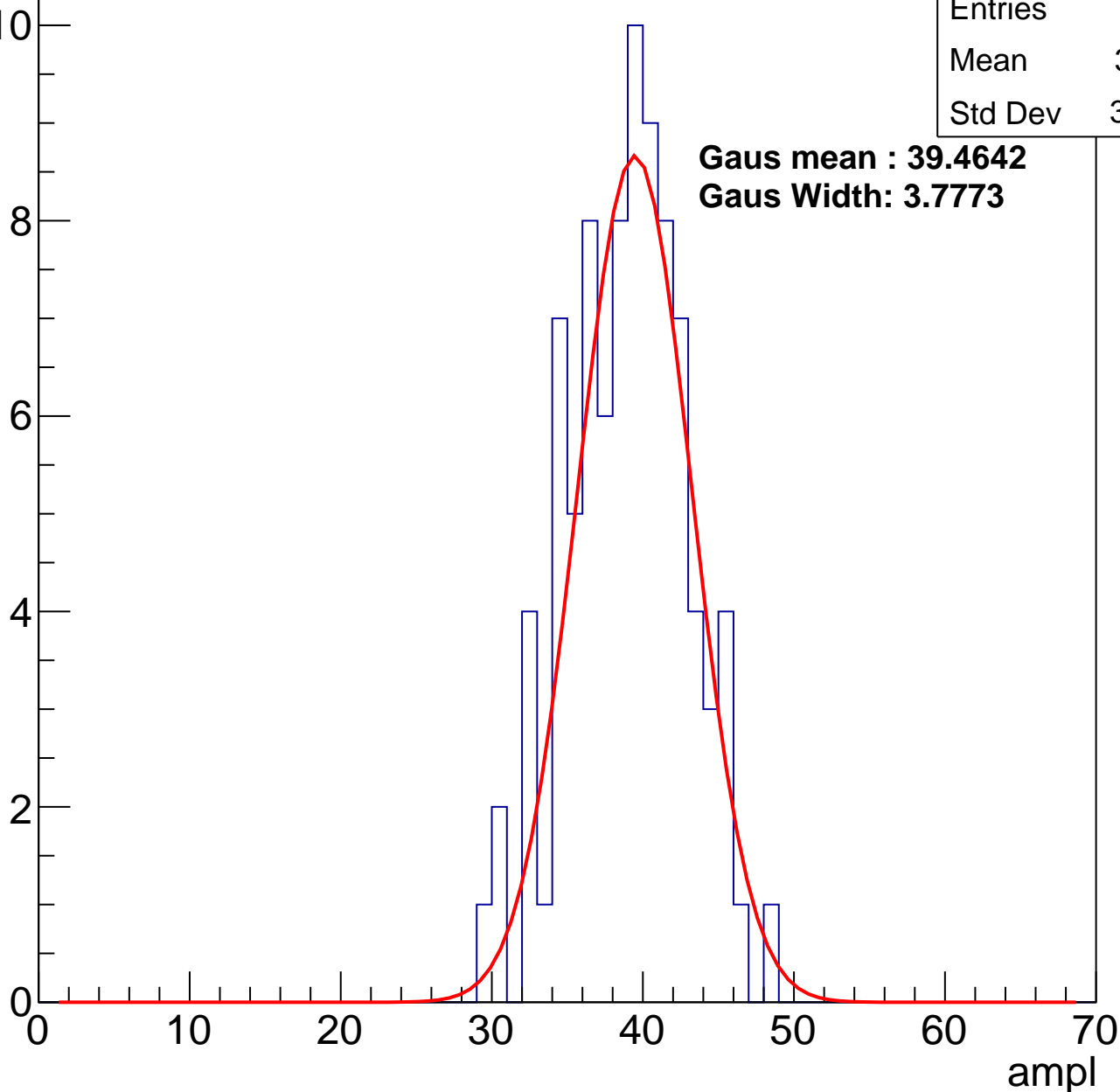
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	89
Mean	38.51
Std Dev	3.892

**Gaus mean : 39.4642**

**Gaus Width: 3.7773**



# B1L101S, U22-ch109, adc2

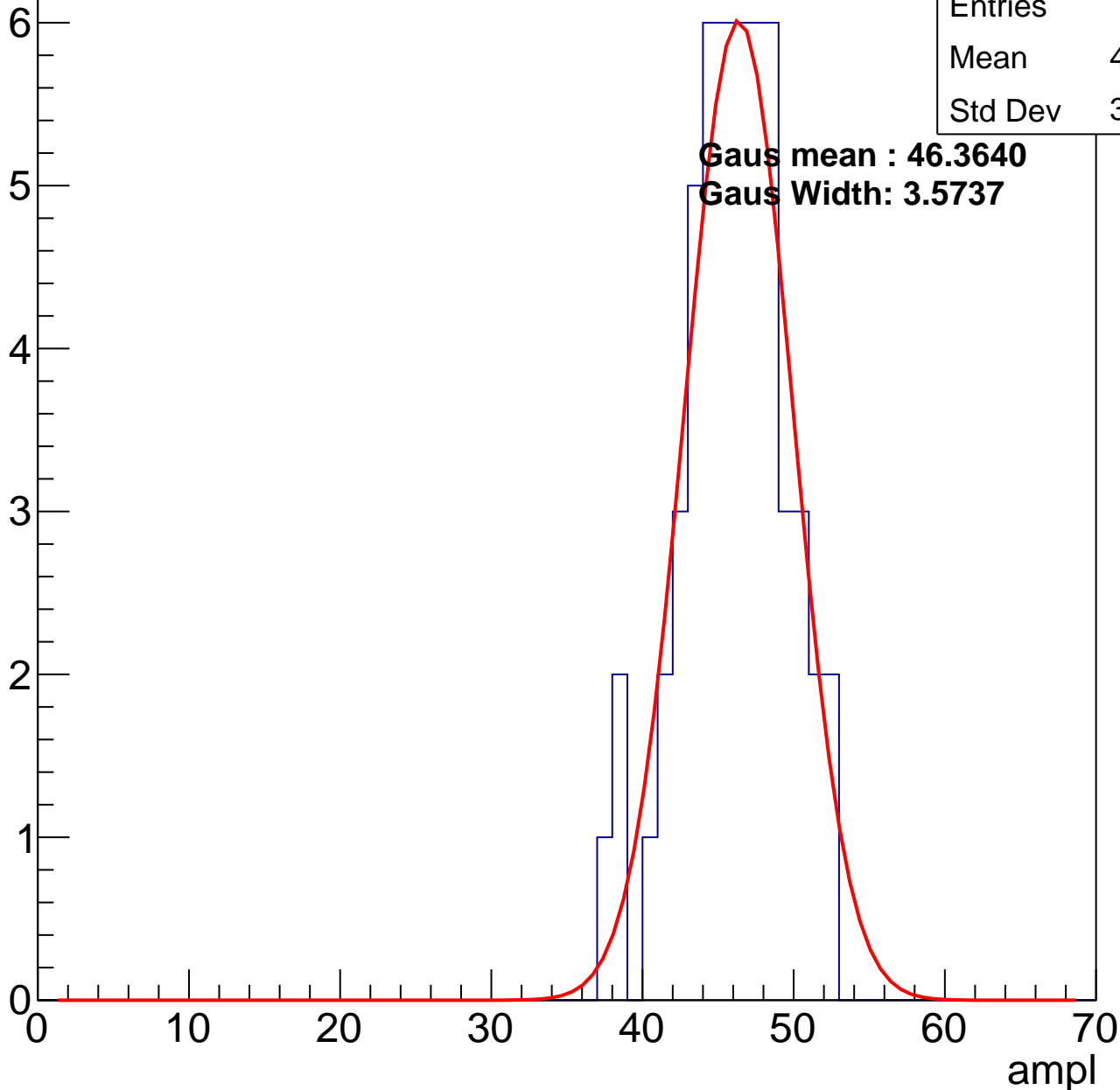
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	54
Mean	45.54
Std Dev	3.425

**Gaus mean : 46.3640**

**Gaus Width: 3.5737**

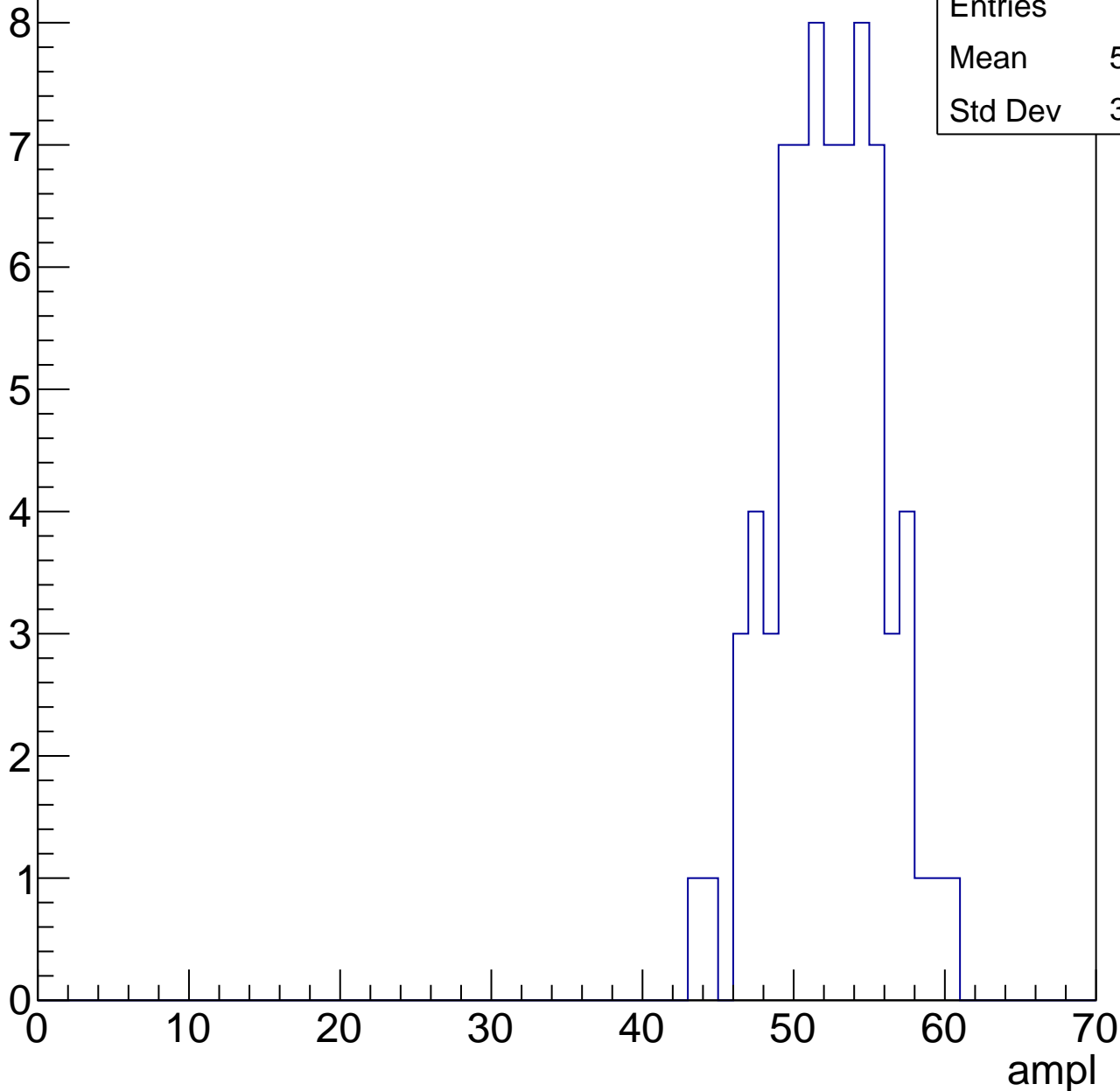


# B1L101S, U22-ch109, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	73
Mean	51.82
Std Dev	3.505

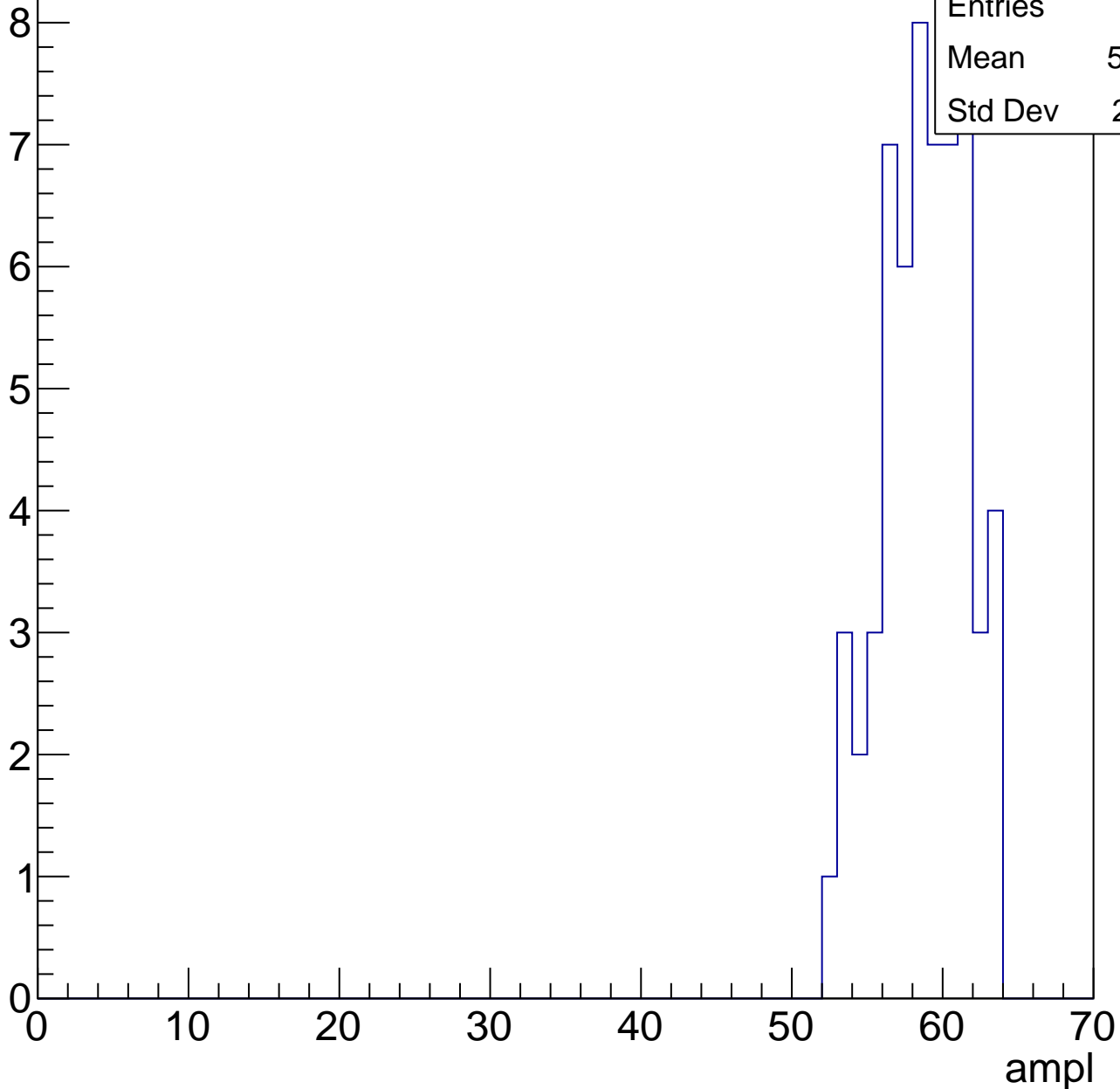


# B1L101S, U22-ch109, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	59
Mean	58.32
Std Dev	2.771

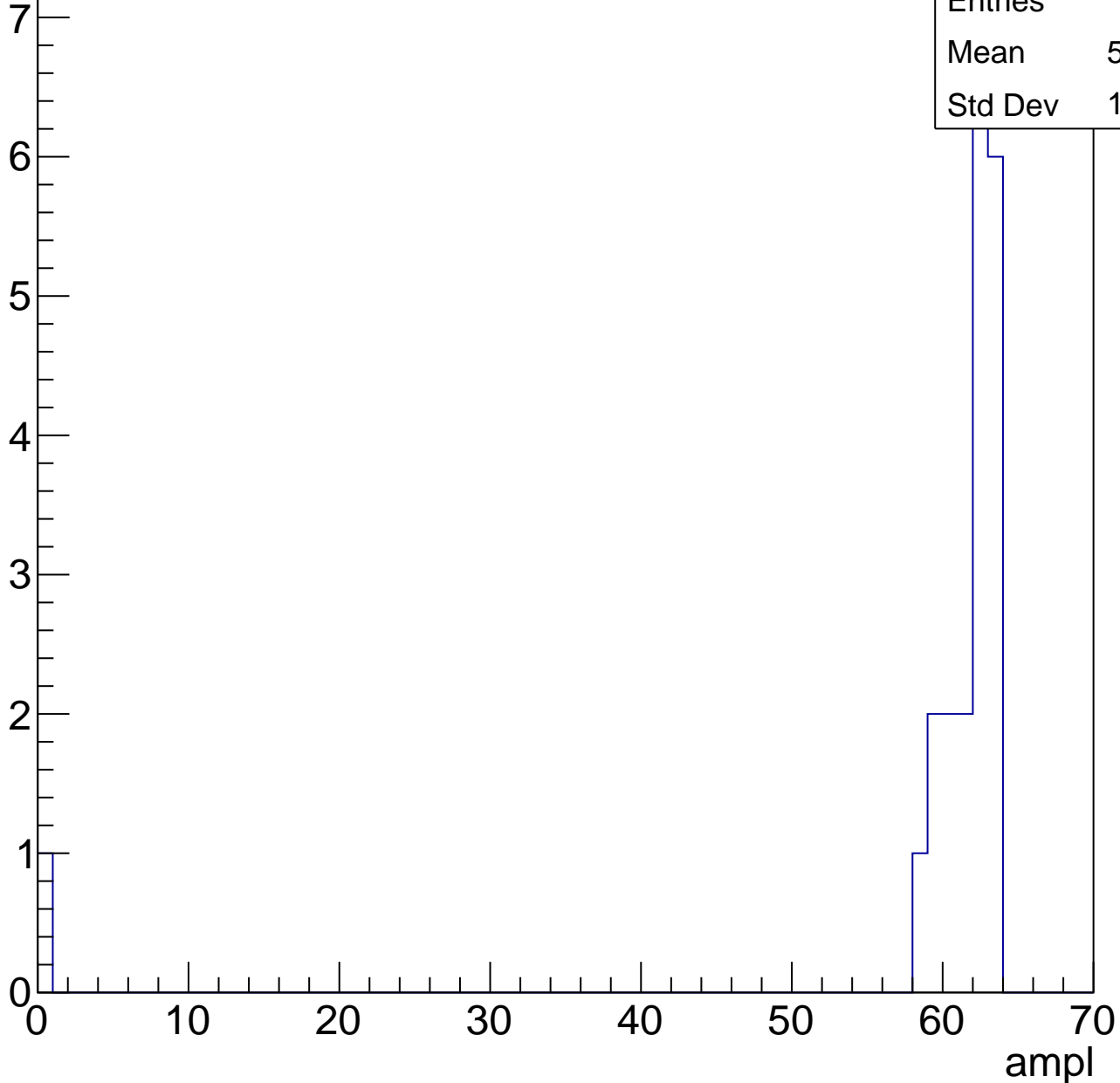


# B1L101S, U22-ch109, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	21
Mean	58.57
Std Dev	13.18



# B1L101S, U22-ch109, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0



# B1L101S, U22-ch109, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U22-ch110, adc0

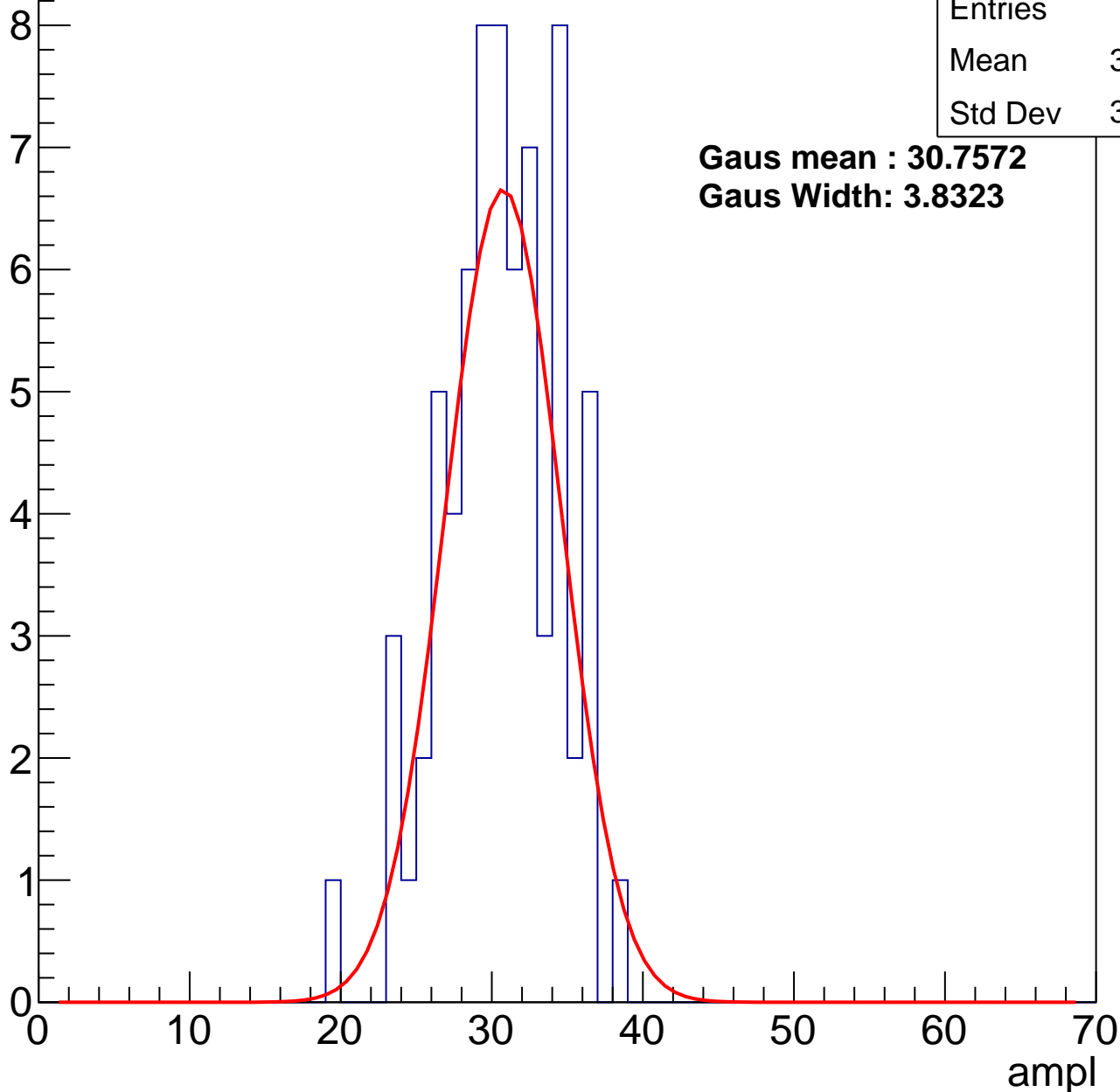
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	30.13
Std Dev	3.749

**Gaus mean : 30.7572**

**Gaus Width: 3.8323**



# B1L101S, U22-ch110, adc1

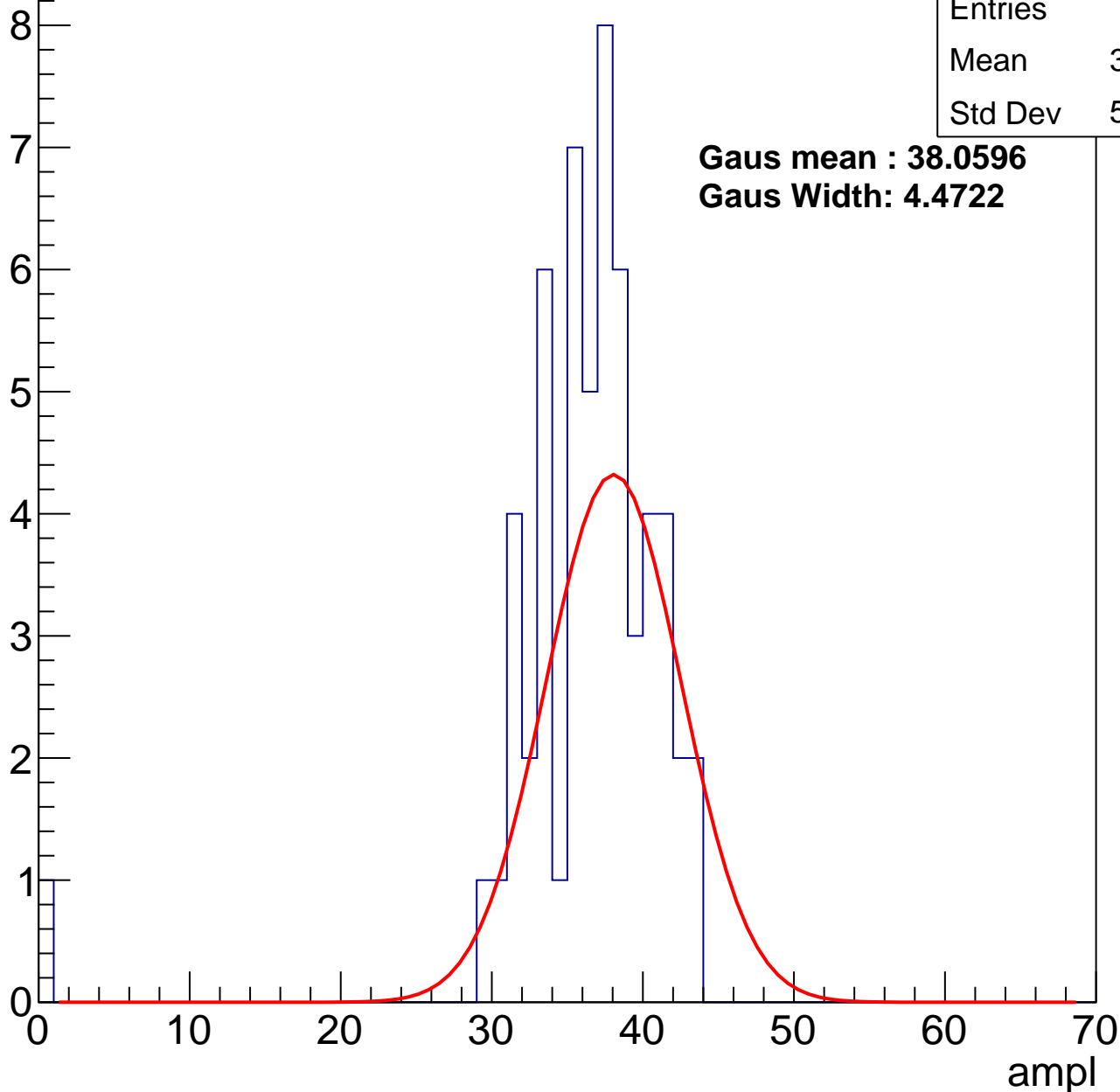
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	57
Mean	35.77
Std Dev	5.876

**Gaus mean : 38.0596**

**Gaus Width: 4.4722**



# B1L101S, U22-ch110, adc2

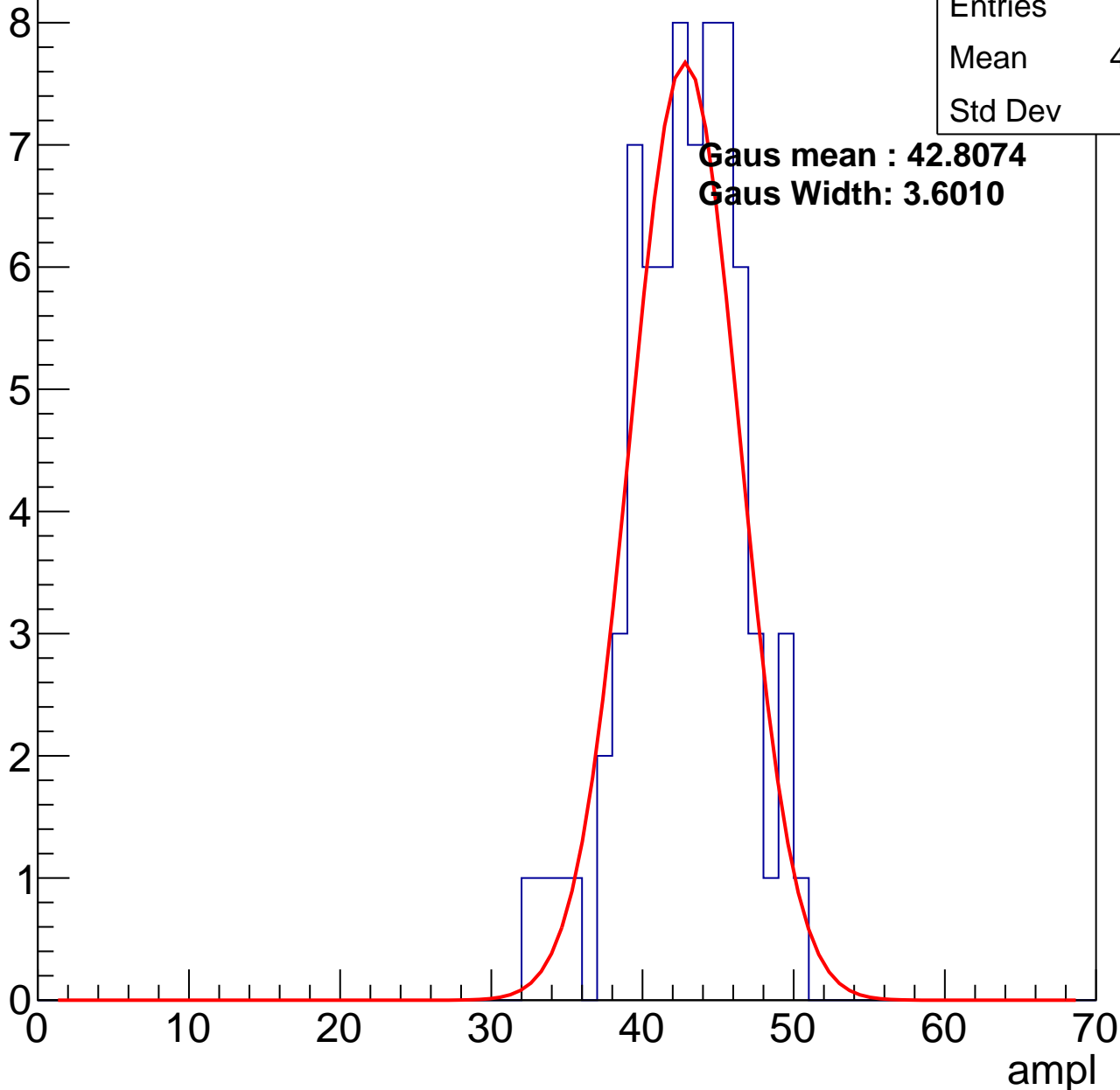
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	73
Mean	42.36
Std Dev	3.71

**Gaus mean : 42.8074**

**Gaus Width: 3.6010**

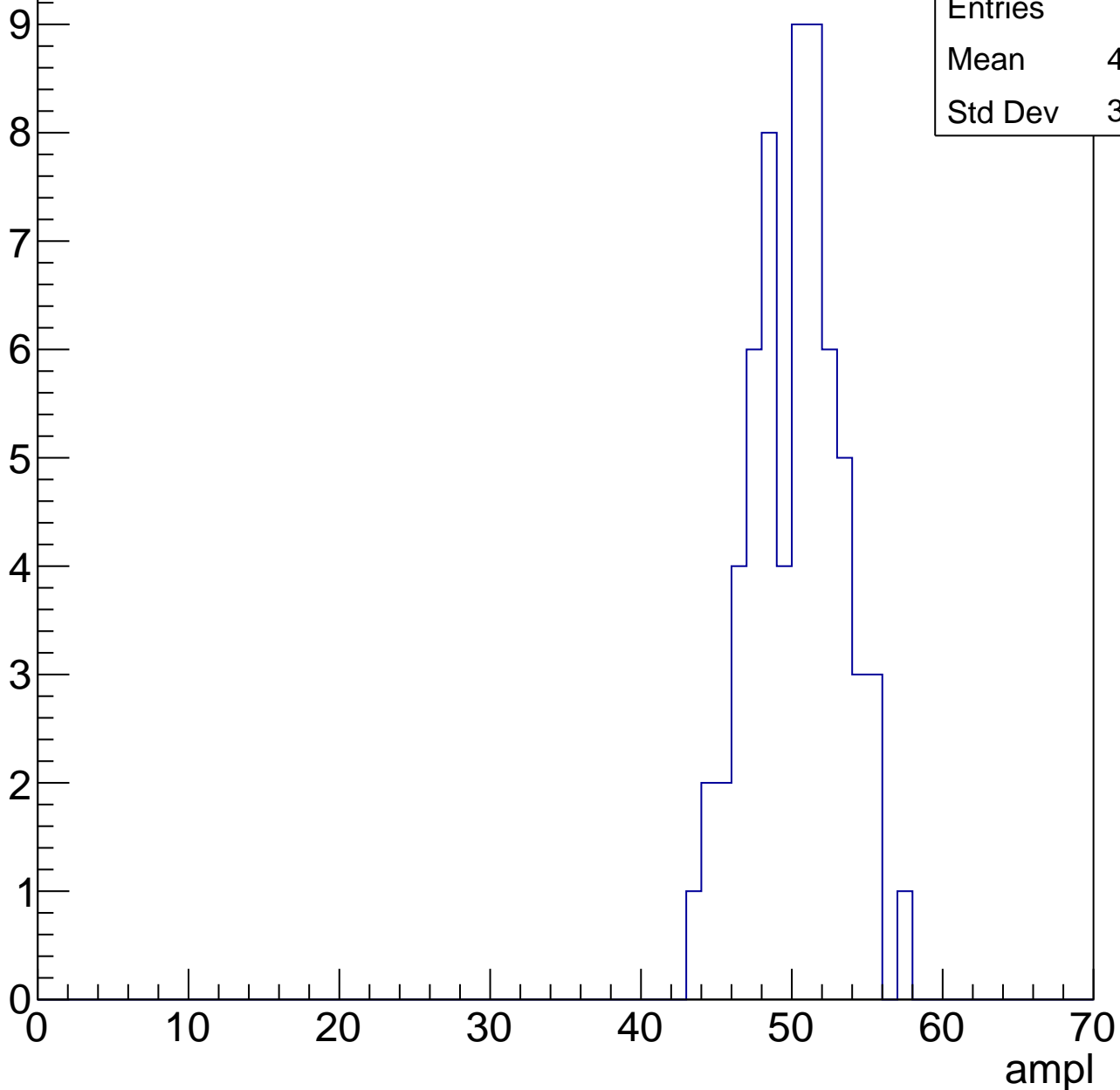


# B1L101S, U22-ch110, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	49.79
Std Dev	3.014

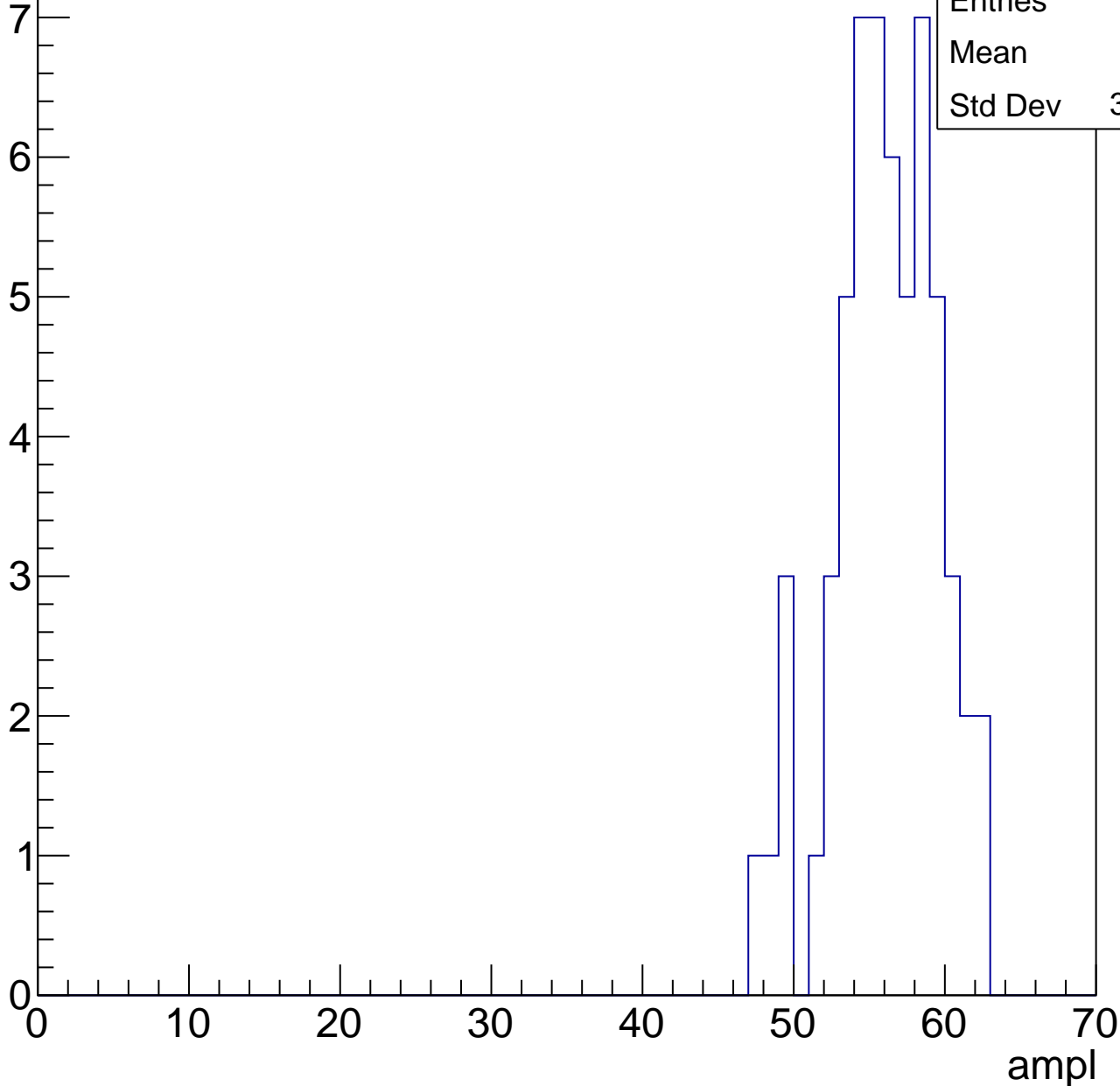


# B1L101S, U22-ch110, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	58
Mean	55.6
Std Dev	3.434

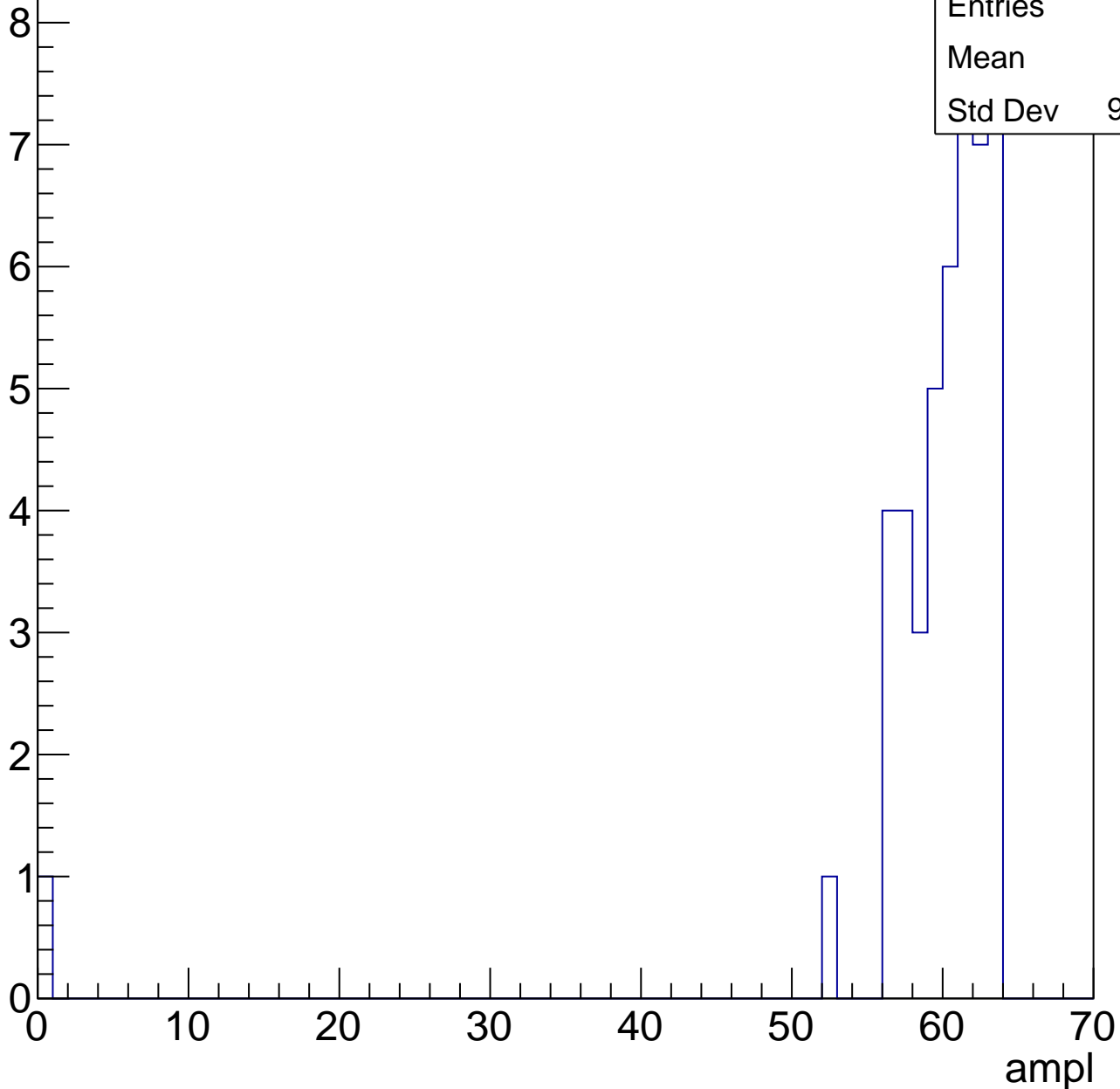


# B1L101S, U22-ch110, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	47
Mean	58.7
Std Dev	9.003



# B1L101S, U22-ch110, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	4
Mean	62
Std Dev	1.225



# B1L101S, U22-ch110, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L101S, U22-ch111, adc0

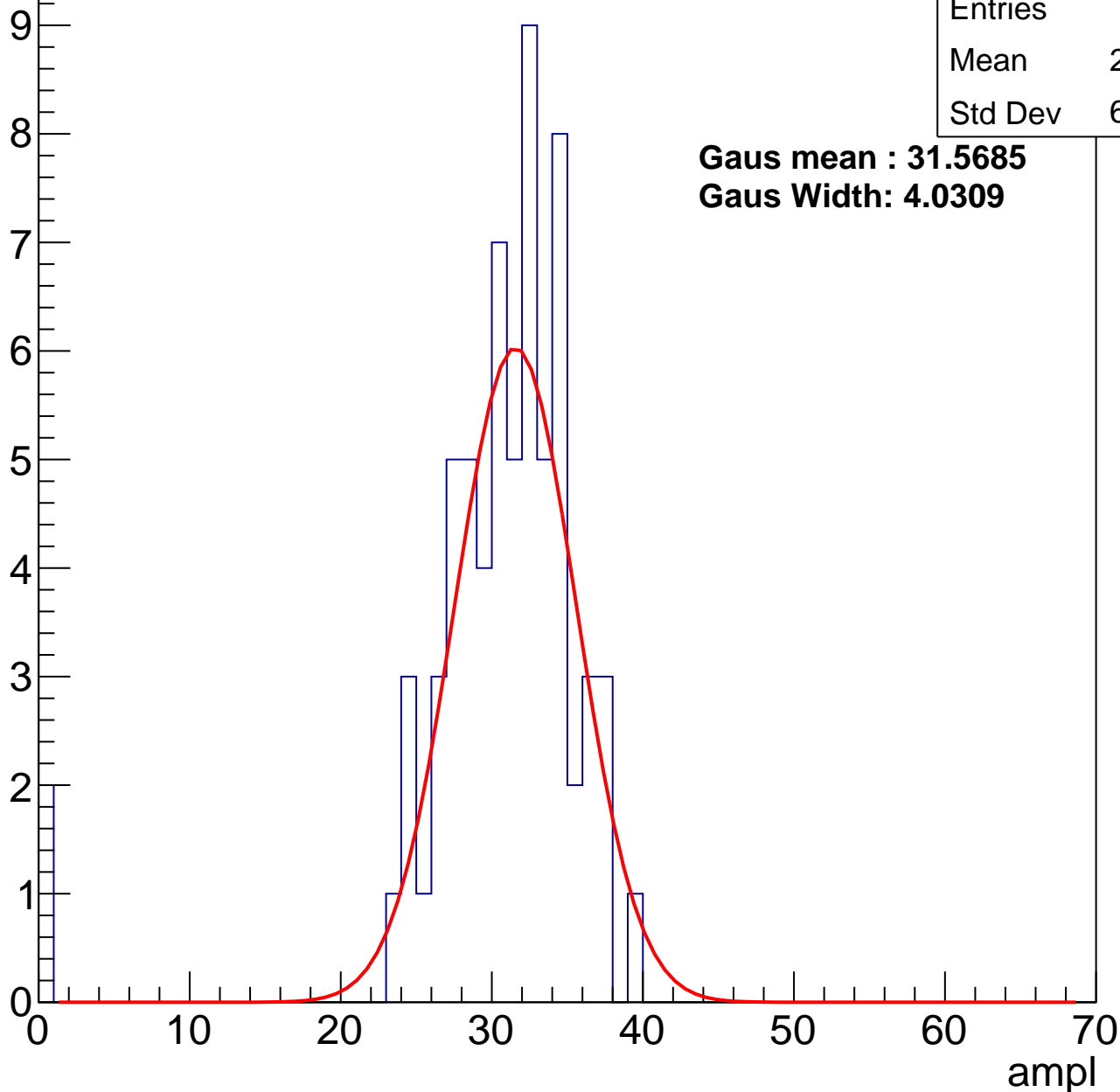
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	67
Mean	29.96
Std Dev	6.347

**Gaus mean : 31.5685**

**Gaus Width: 4.0309**



# B1L101S, U22-ch111, adc1

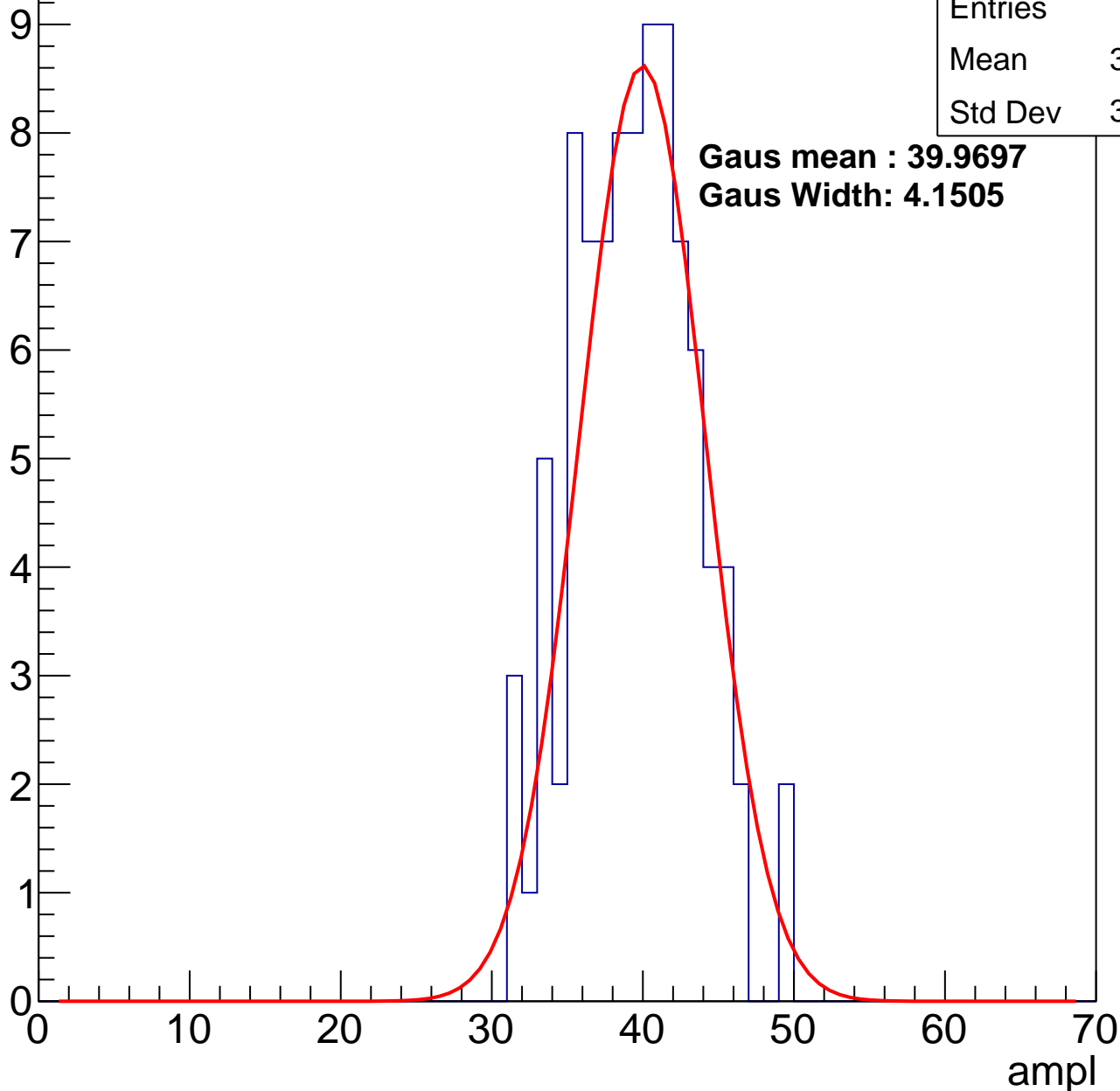
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	92
Mean	39.04
Std Dev	3.962

**Gaus mean : 39.9697**

**Gaus Width: 4.1505**



# B1L101S, U22-ch111, adc2

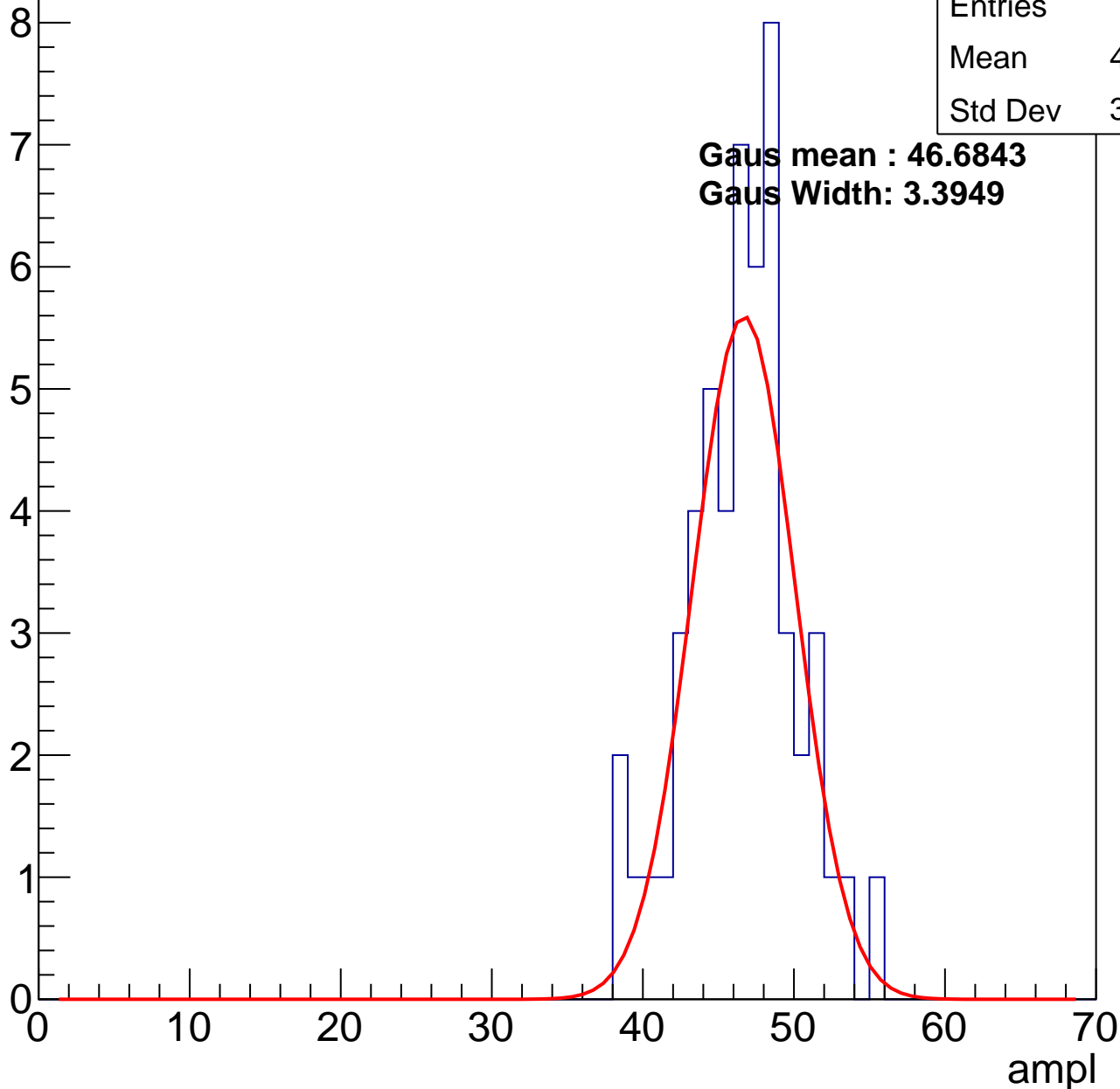
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	53
Mean	46.08
Std Dev	3.592

**Gaus mean : 46.6843**

**Gaus Width: 3.3949**

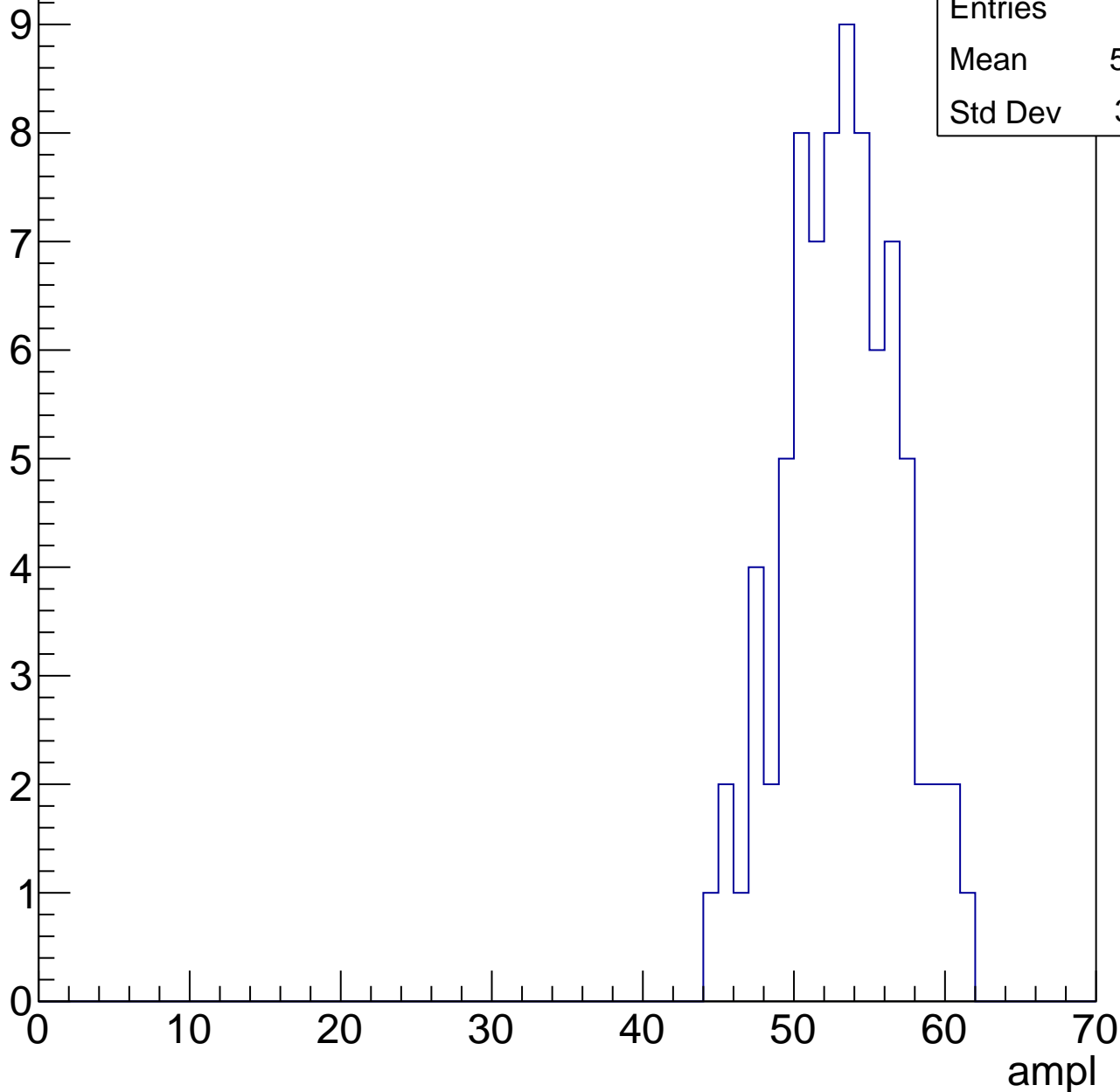


# B1L101S, U22-ch111, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	80
Mean	52.66
Std Dev	3.691

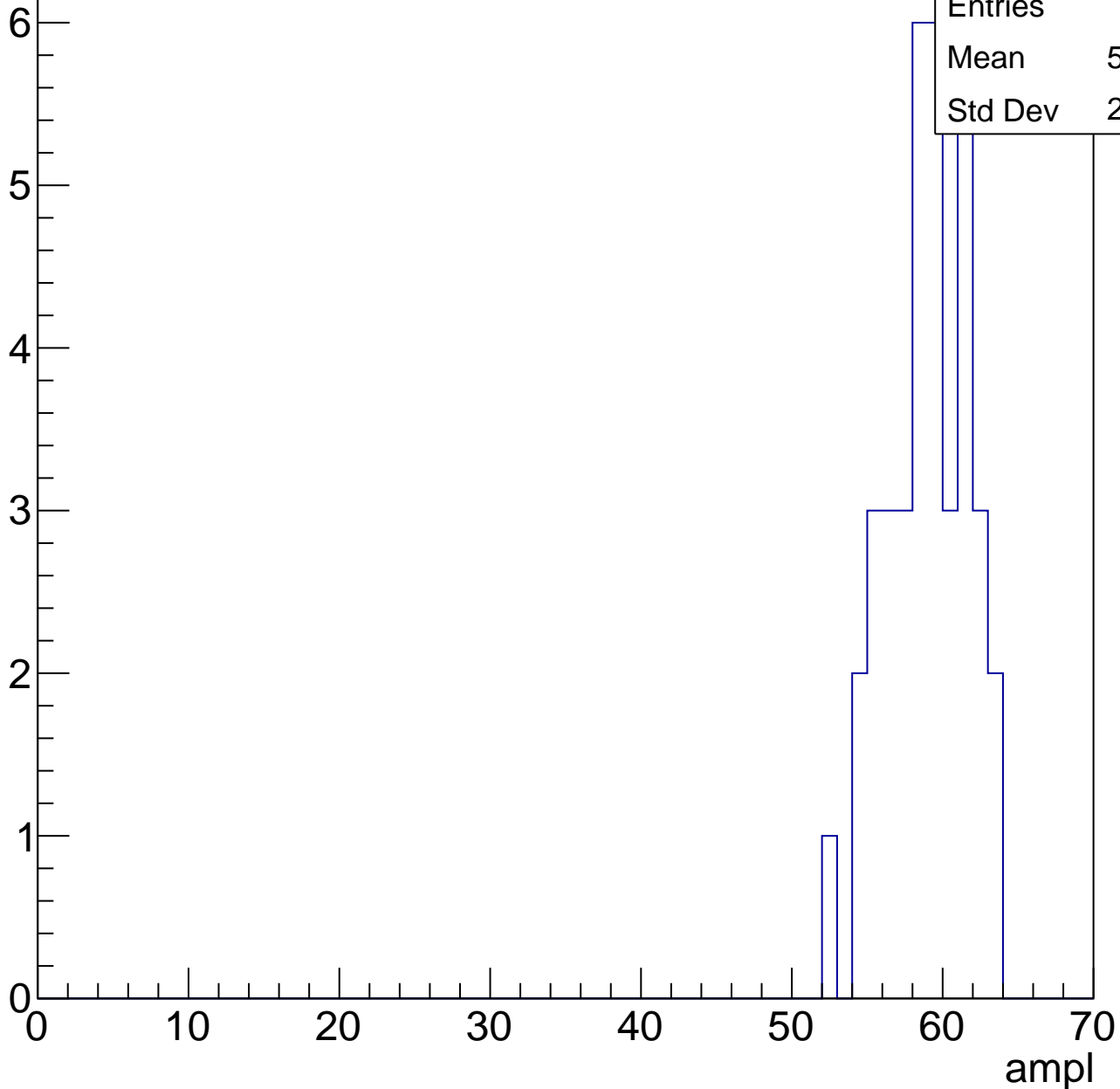


# B1L101S, U22-ch111, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	38
Mean	58.53
Std Dev	2.663

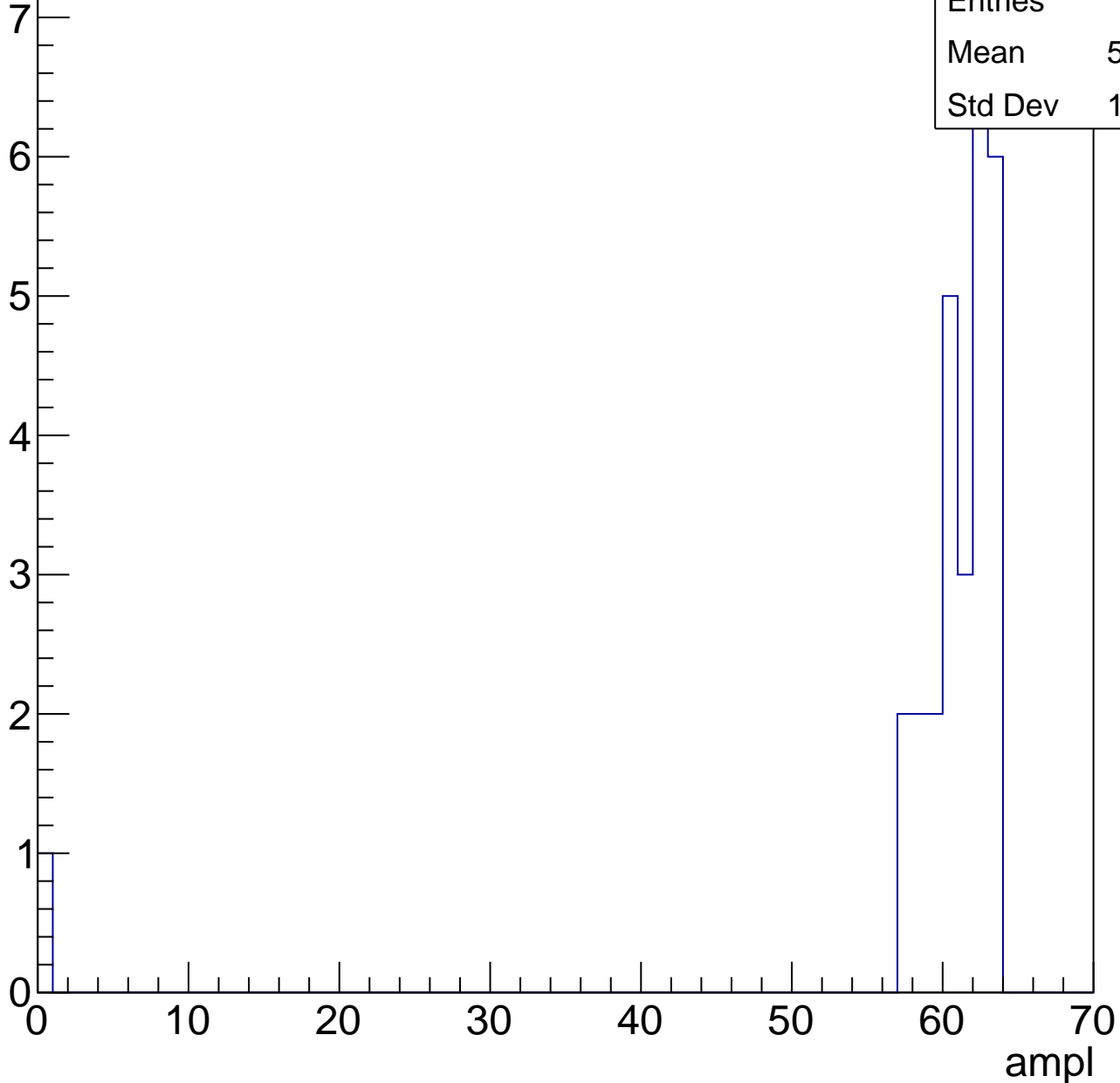


# B1L101S, U22-ch111, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	28
Mean	58.68
Std Dev	11.44



# B1L101S, U22-ch111, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	2
Mean	63
Std Dev	0

ampl



# B1L101S, U22-ch111, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U22-ch112, adc0

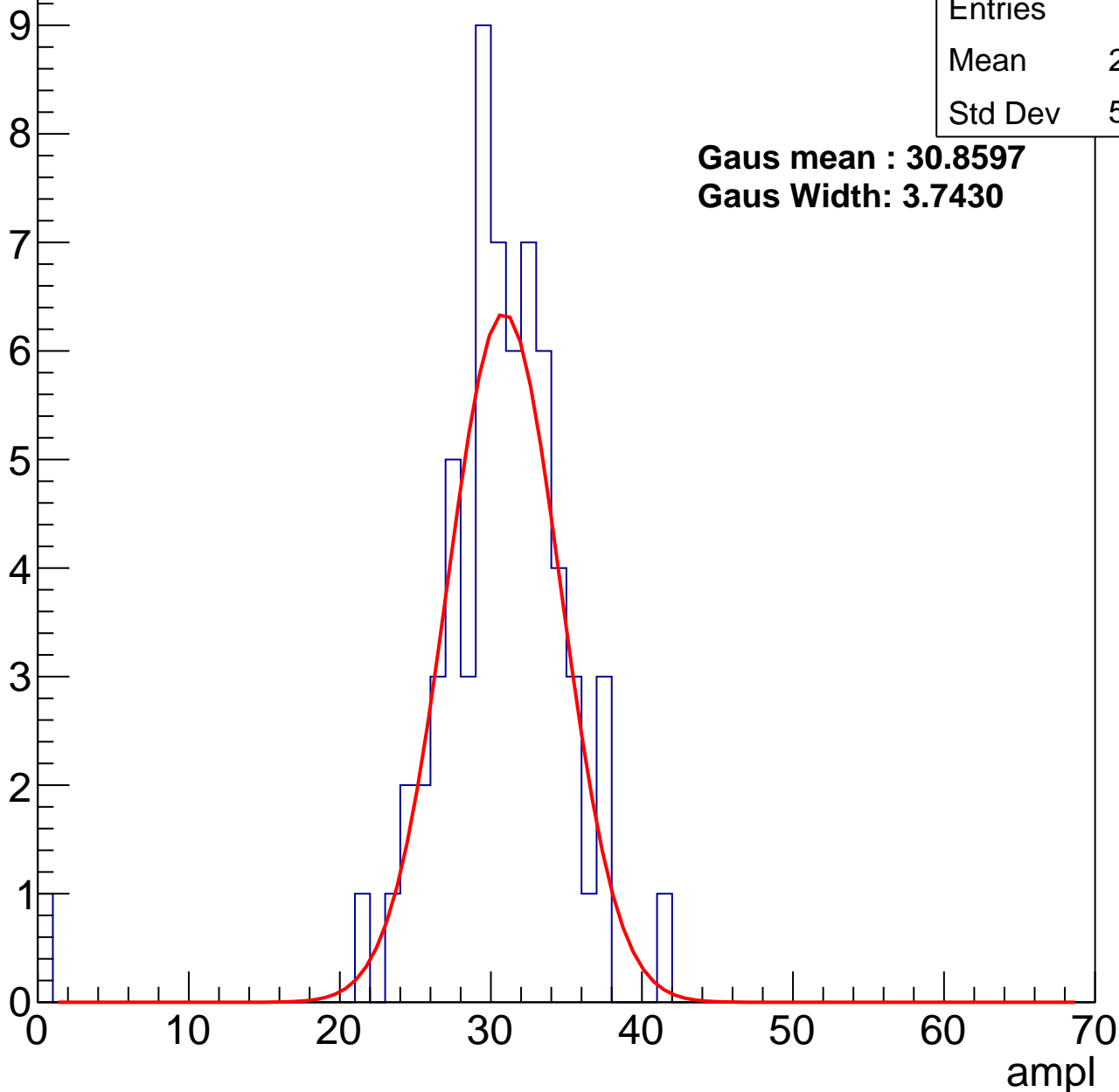
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	29.95
Std Dev	5.258

**Gaus mean : 30.8597**

**Gaus Width: 3.7430**



# B1L101S, U22-ch112, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	73
Mean	38.34
Std Dev	3.597

**Gaus mean : 38.9066**

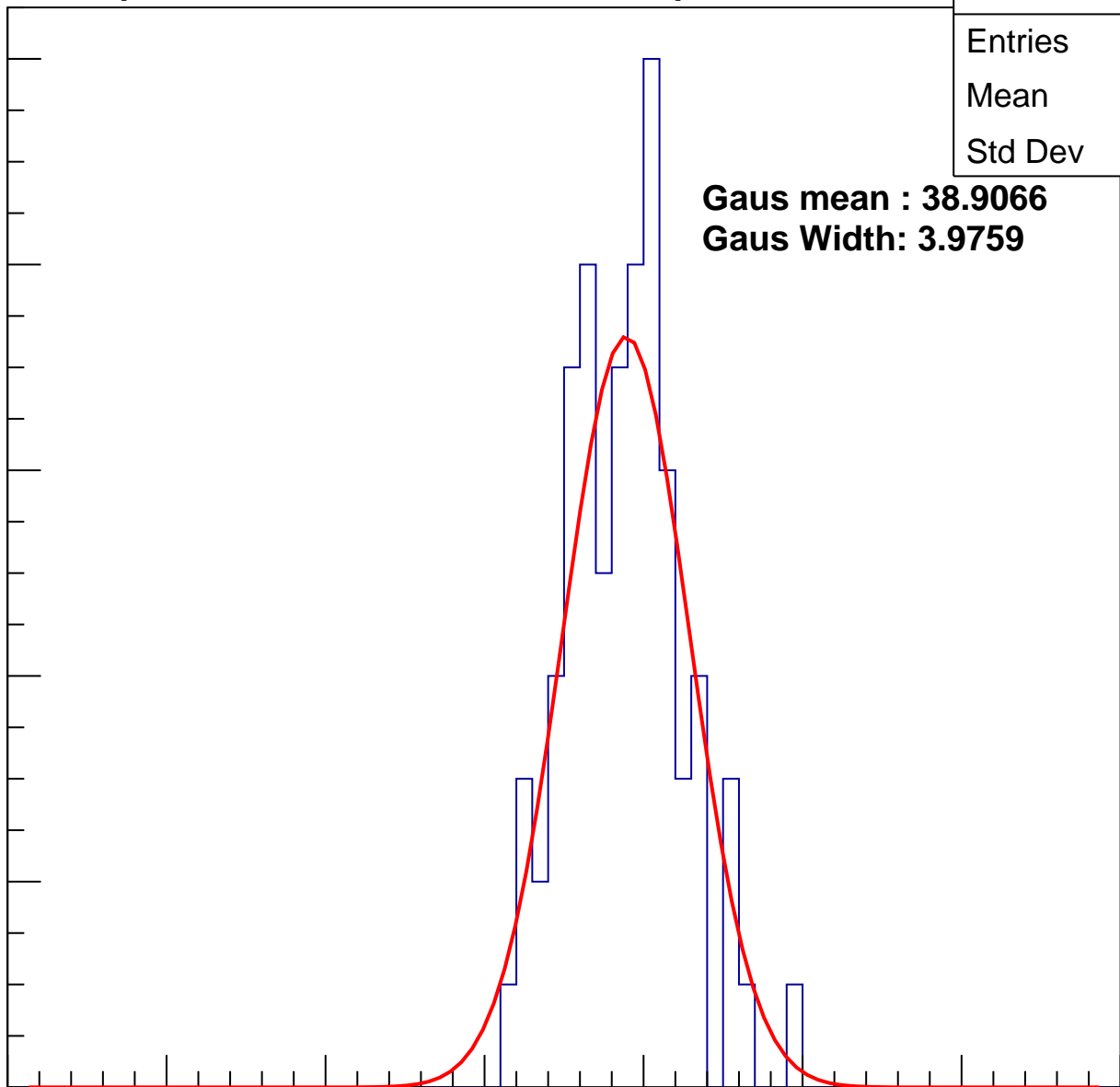
**Gaus Width: 3.9759**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B1L101S, U22-ch112, adc2

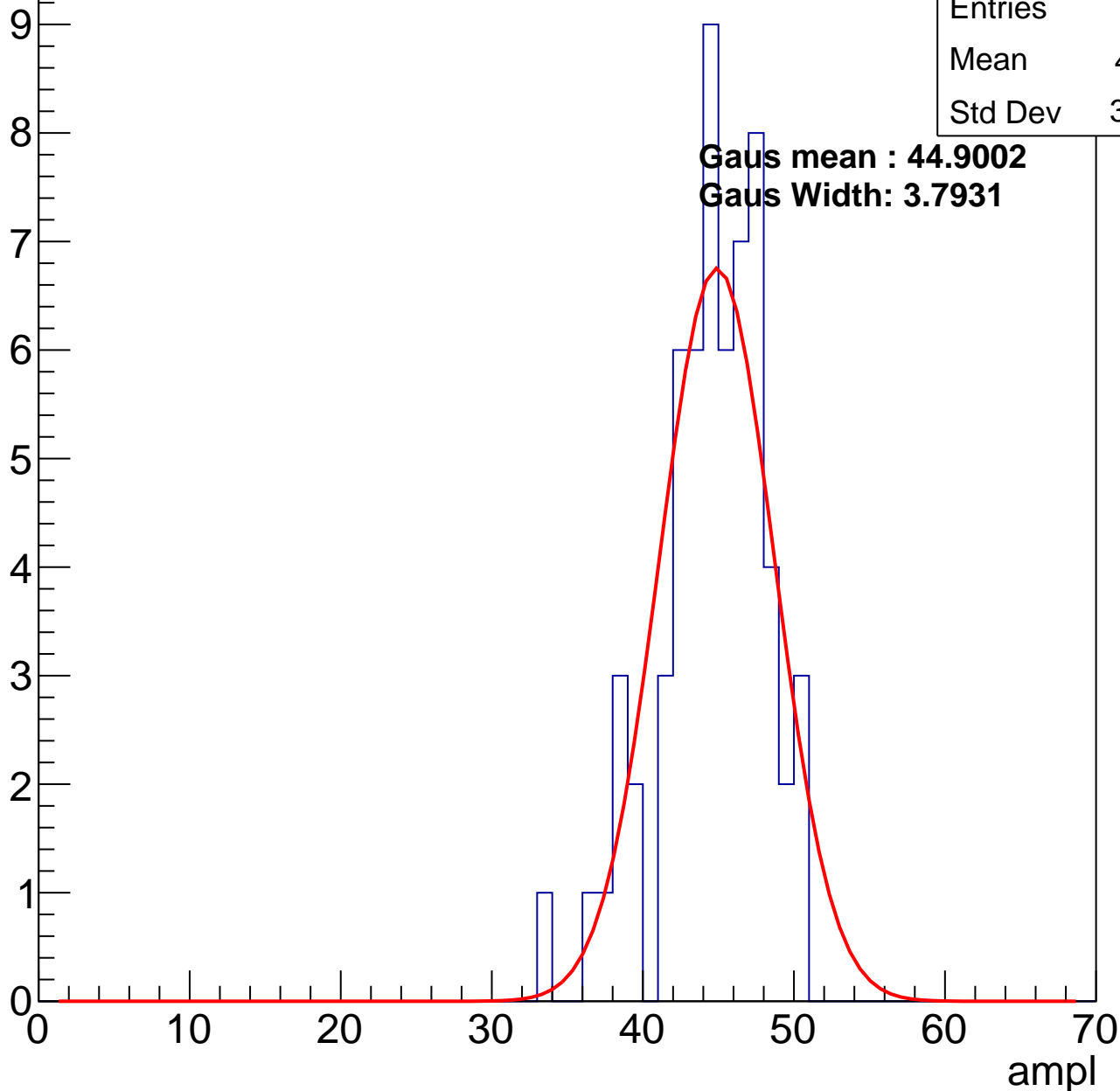
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	44.11
Std Dev	3.538

**Gaus mean : 44.9002**

**Gaus Width: 3.7931**



# B1L101S, U22-ch112, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	68
Mean	51.24
Std Dev	3.726

Entry

10

8

6

4

2

0

0

10

20

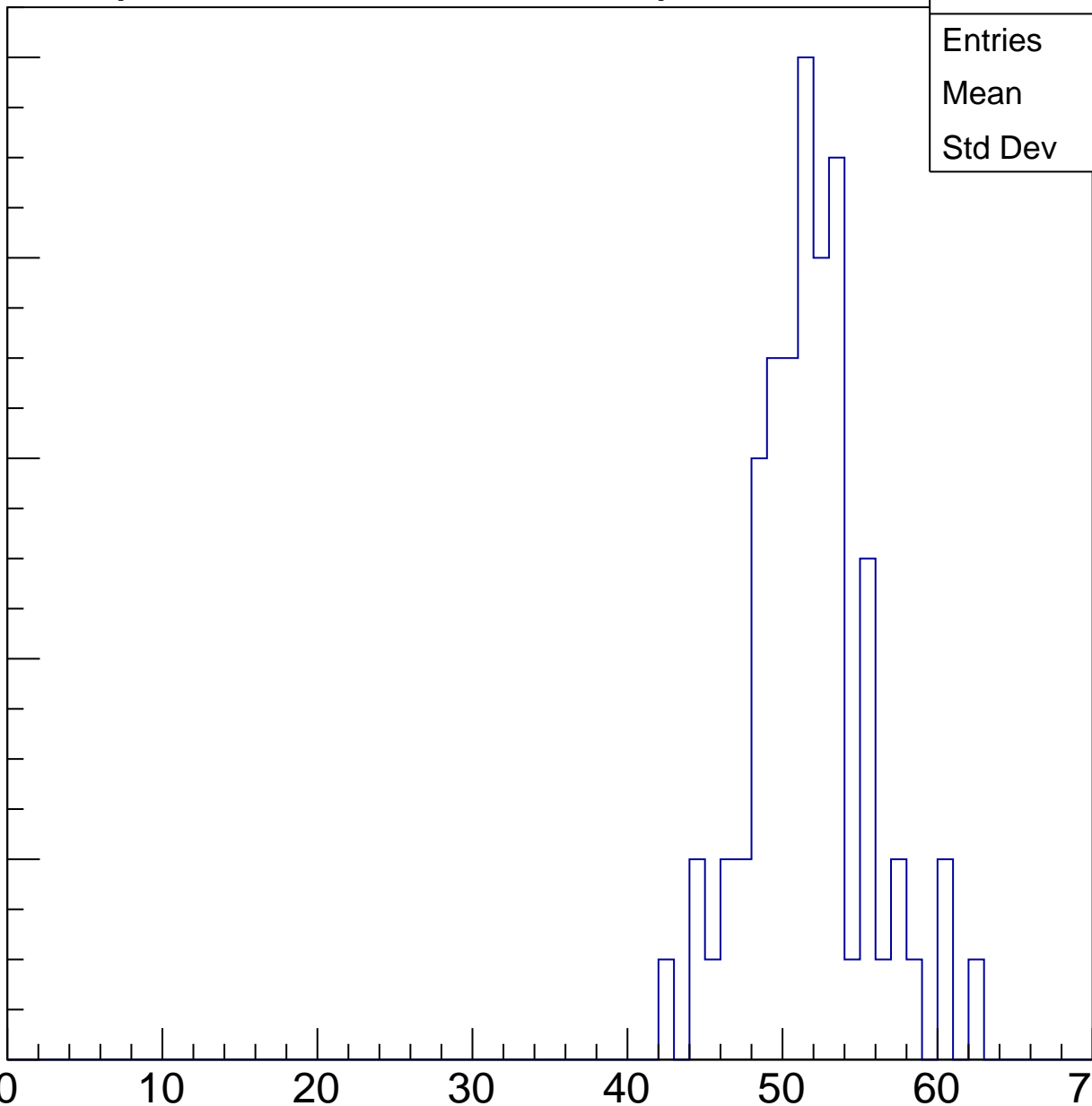
30

40

50

60

ampl

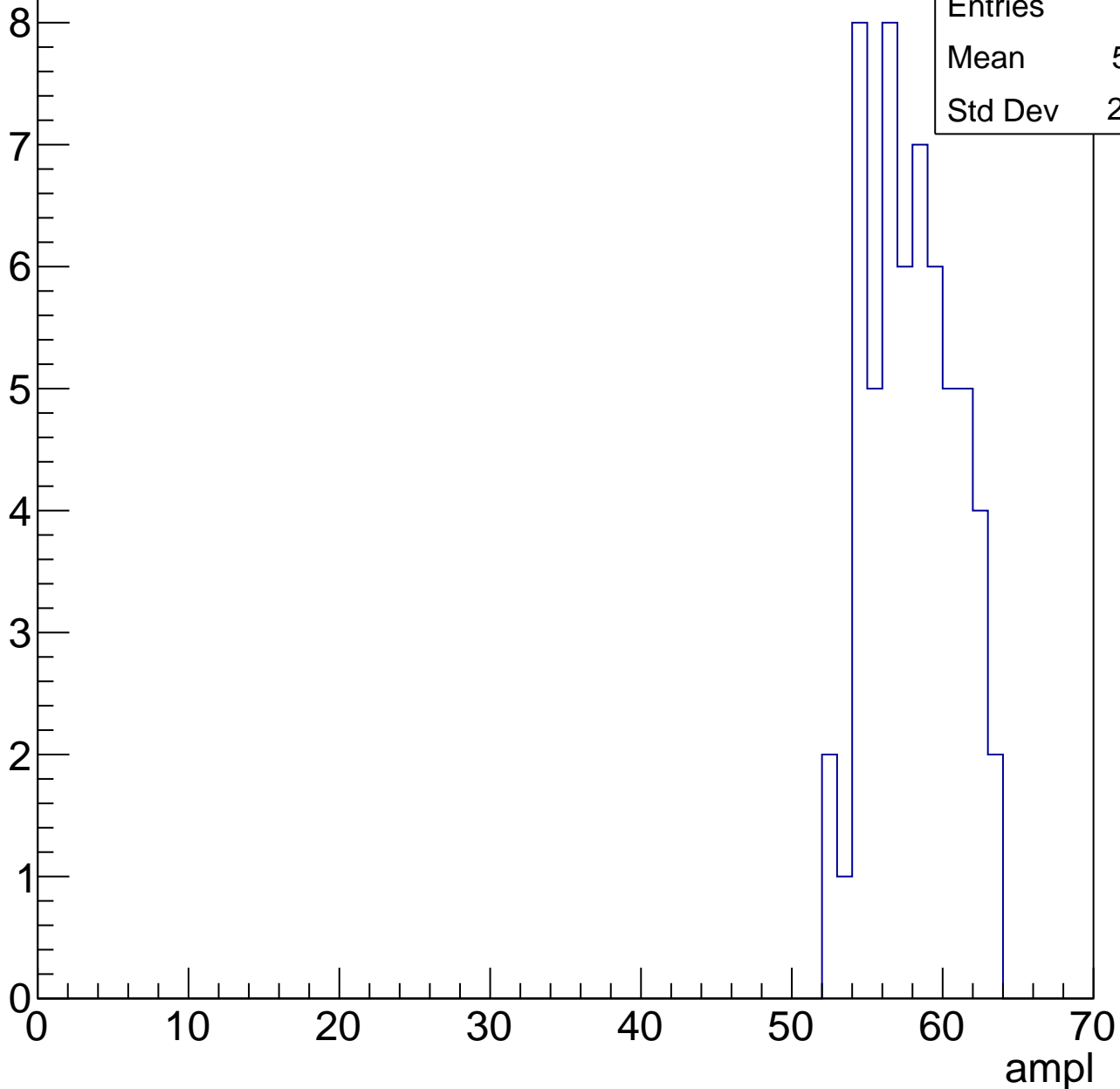


# B1L101S, U22-ch112, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	59
Mean	57.51
Std Dev	2.849

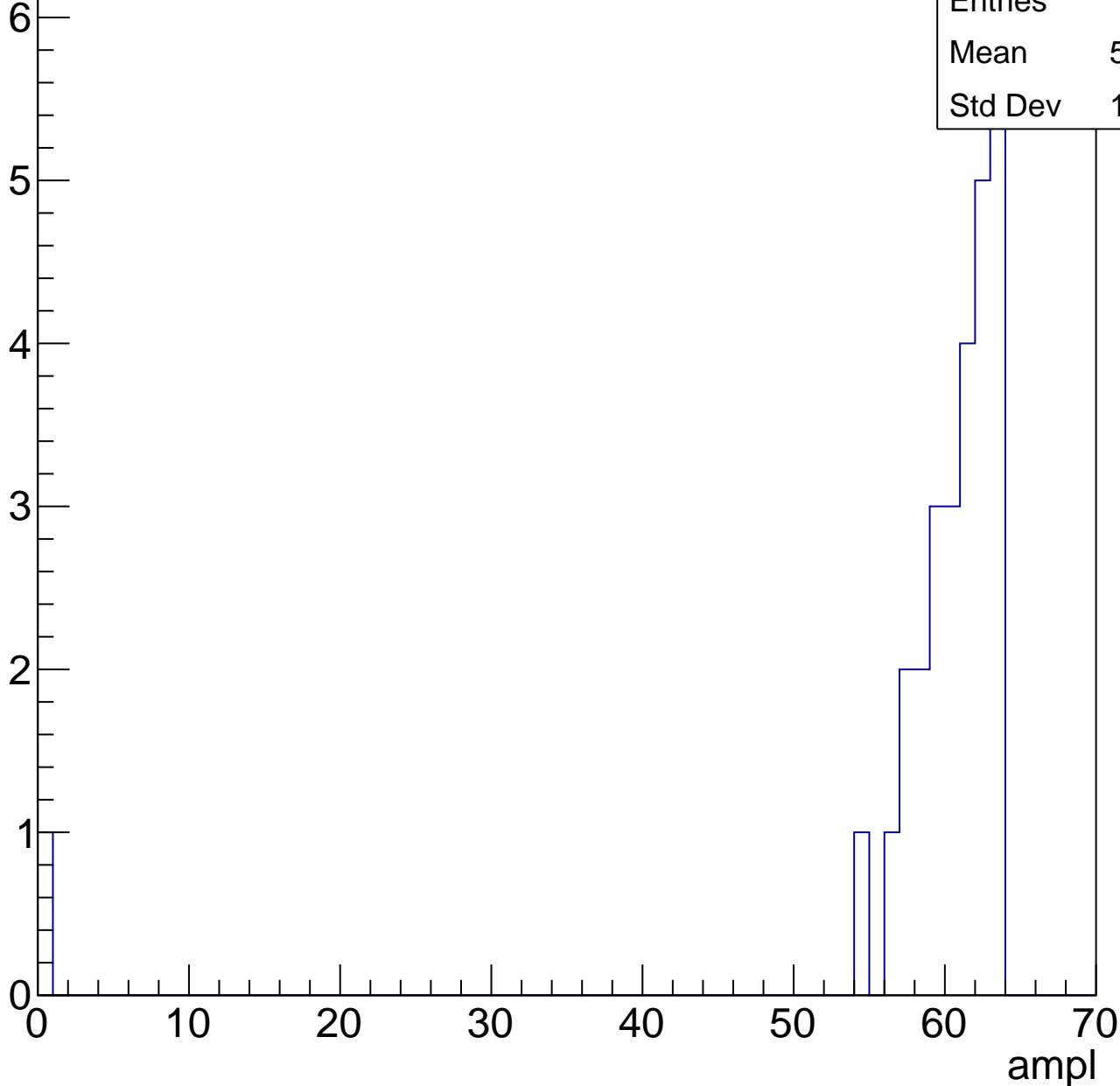


# B1L101S, U22-ch112, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

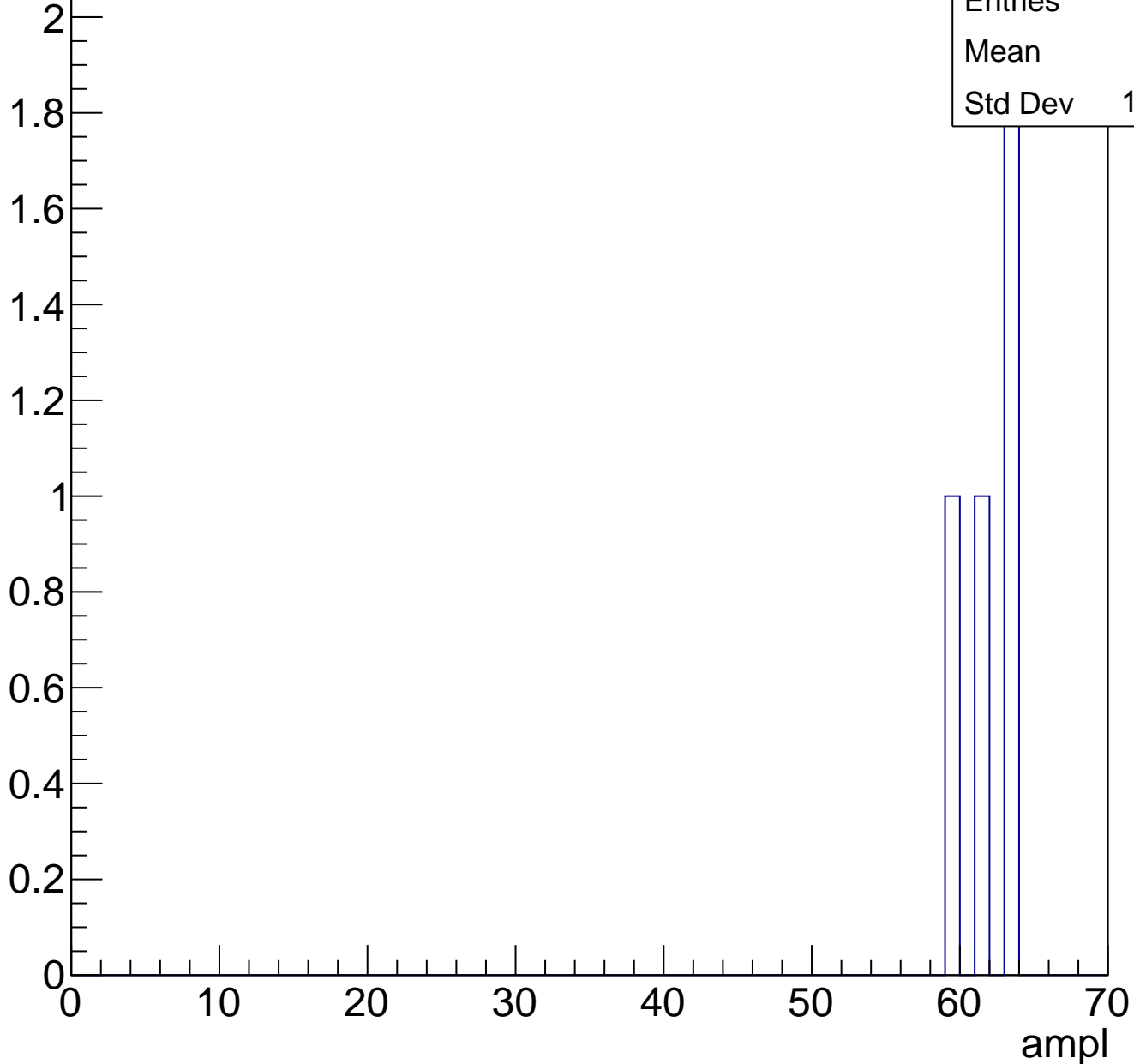
Entries	28
Mean	58.18
Std Dev	11.44



# B1L101S, U22-ch112, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U22-ch112, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L101S, U22-ch113, adc0

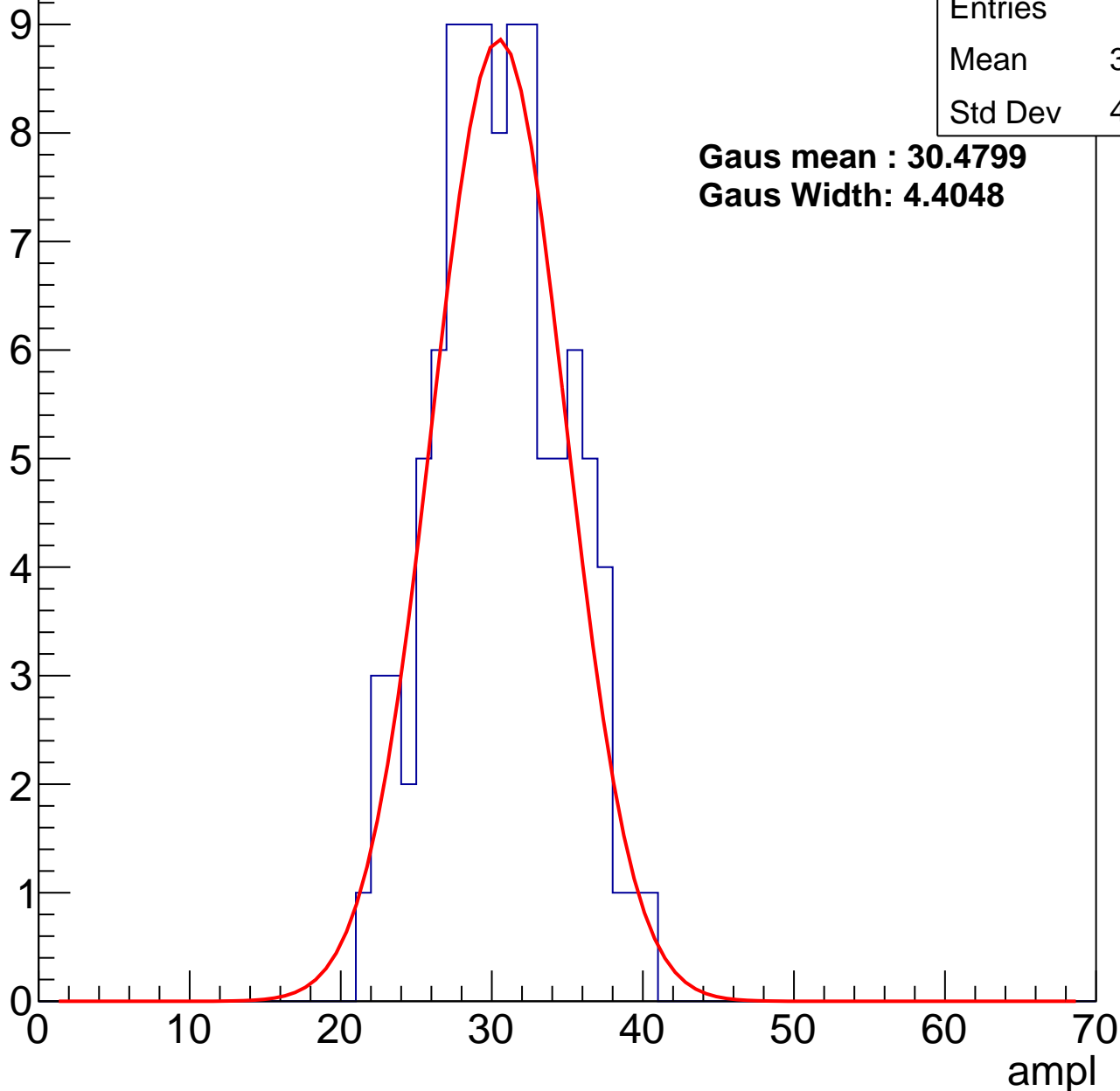
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	101
Mean	30.08
Std Dev	4.197

**Gaus mean : 30.4799**

**Gaus Width: 4.4048**



# B1L101S, U22-ch113, adc1

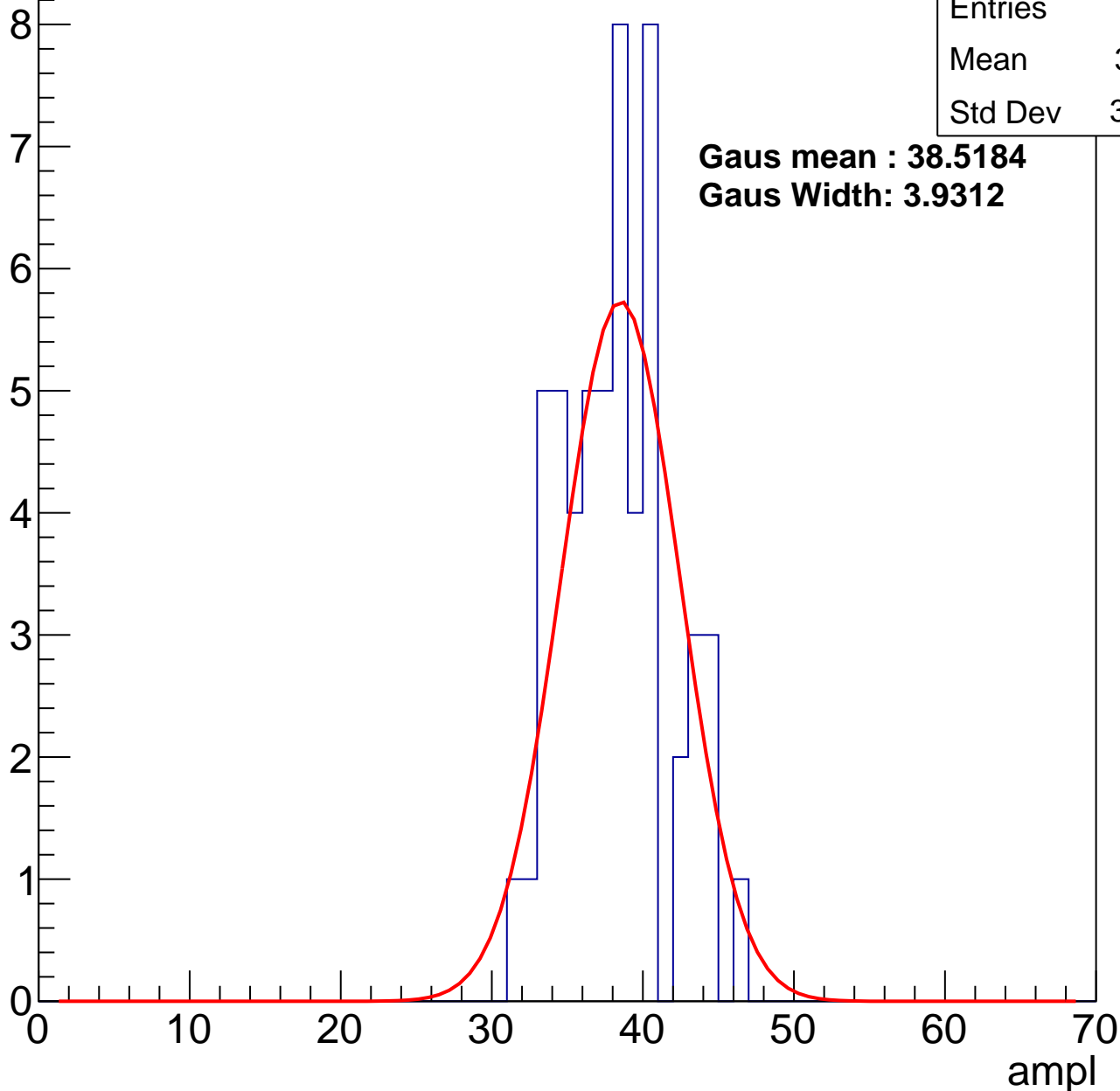
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	55
Mean	37.71
Std Dev	3.468

**Gaus mean : 38.5184**

**Gaus Width: 3.9312**



# B1L101S, U22-ch113, adc2

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	59
Mean	43.44
Std Dev	3.137

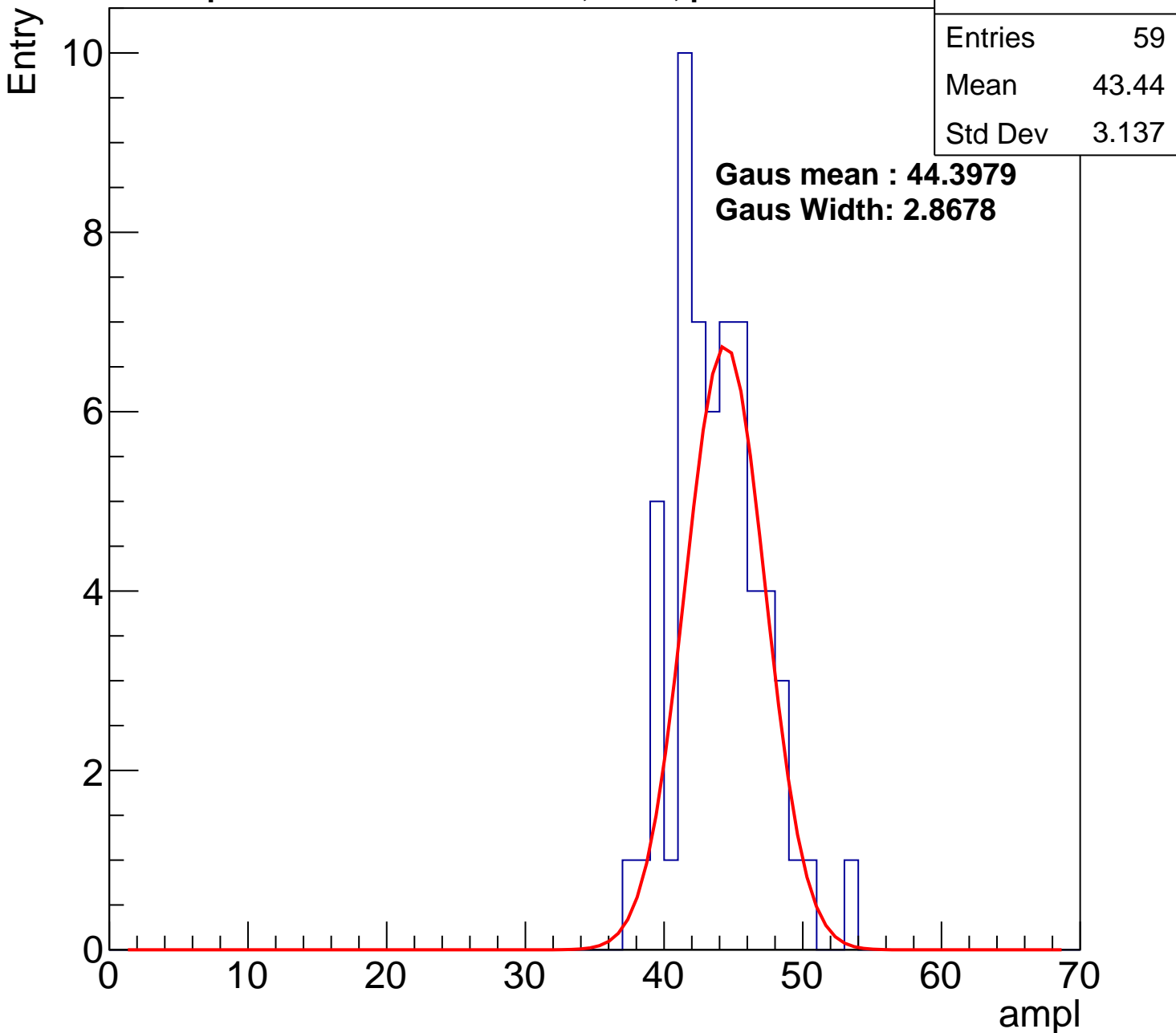
**Gaus mean : 44.3979**  
**Gaus Width: 2.8678**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

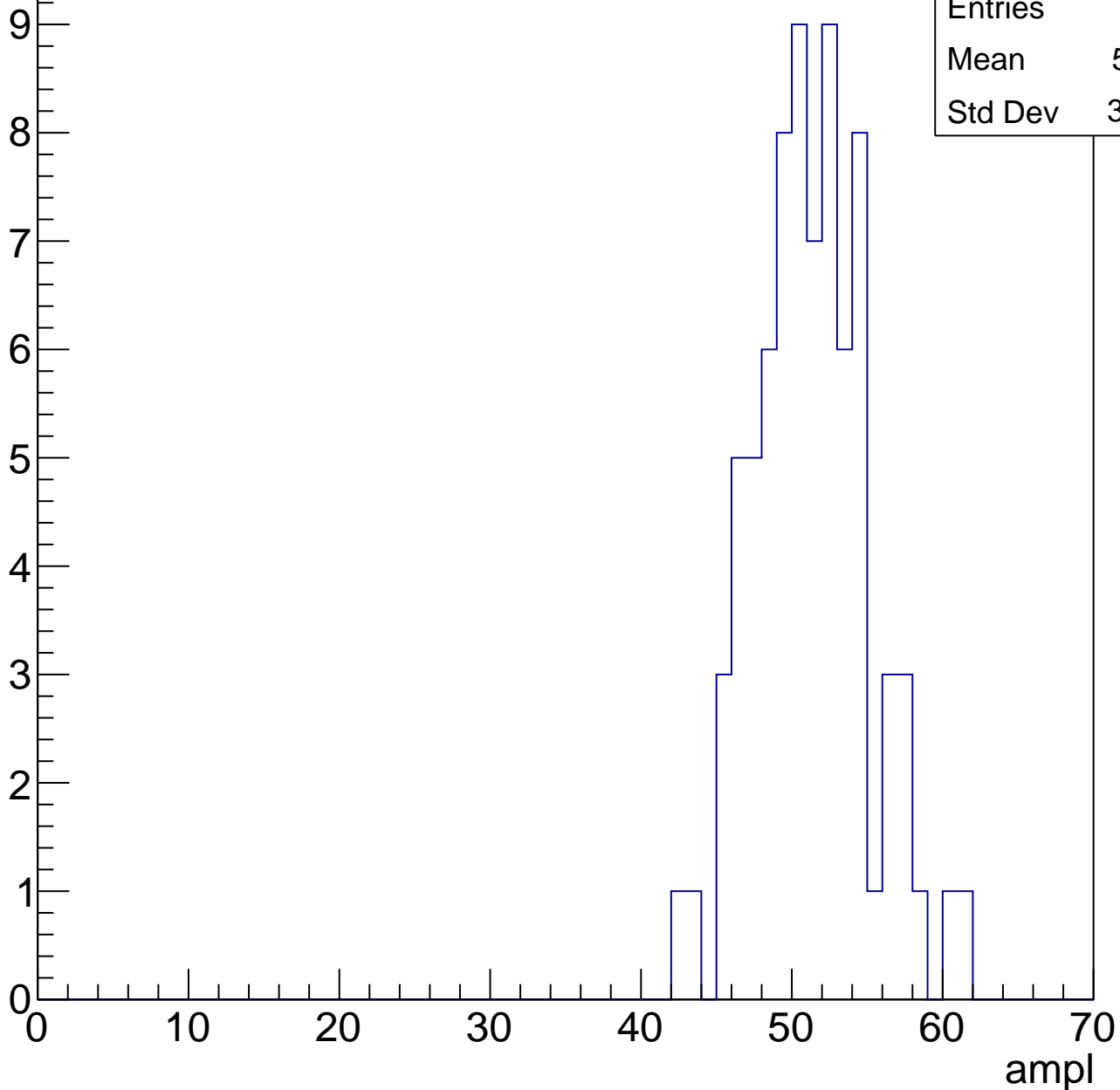


# B1L101S, U22-ch113, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	78
Mean	50.81
Std Dev	3.728



# B1L101S, U22-ch113, adc4

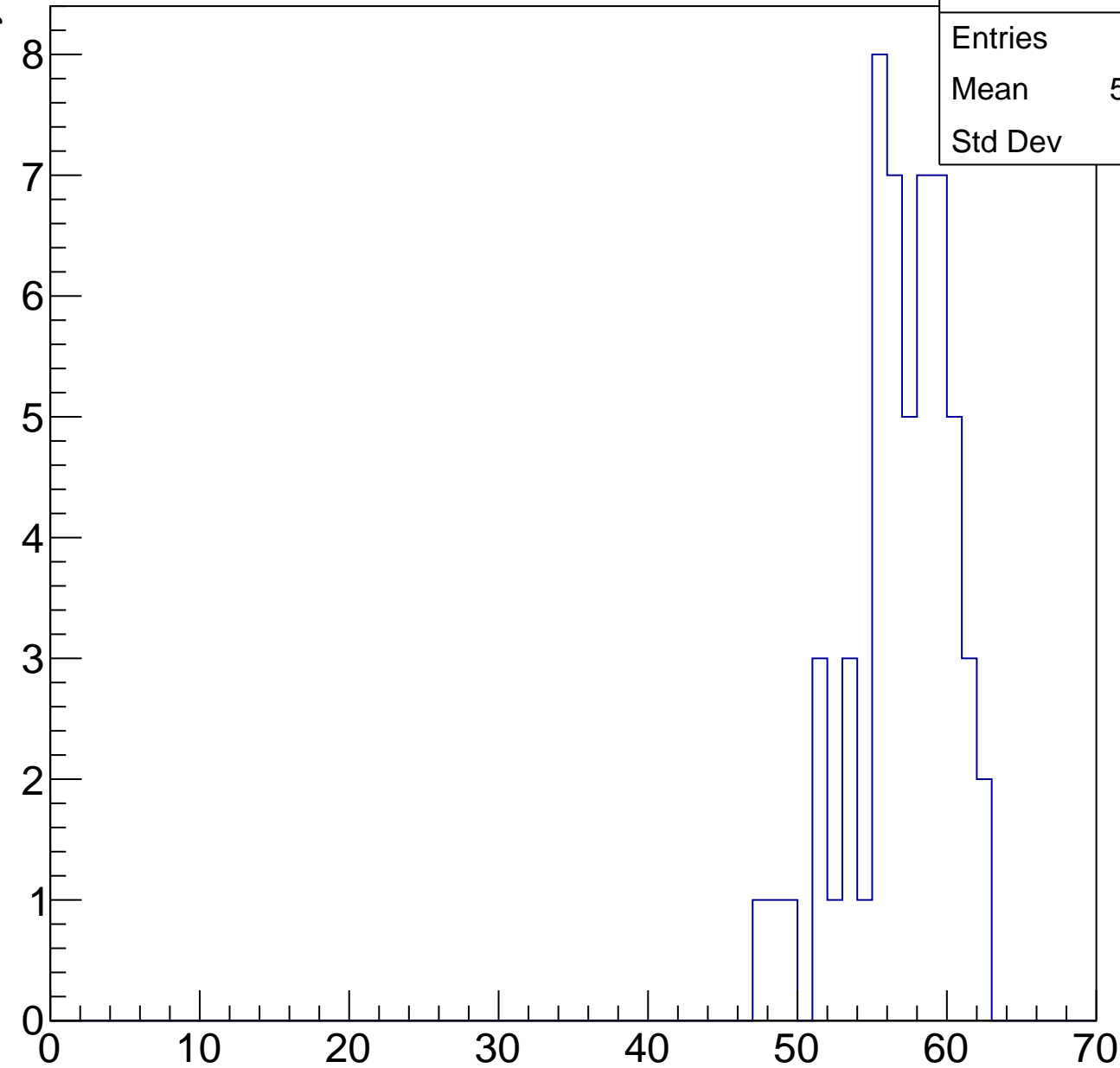
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	55
Mean	56.45
Std Dev	3.4

ampl

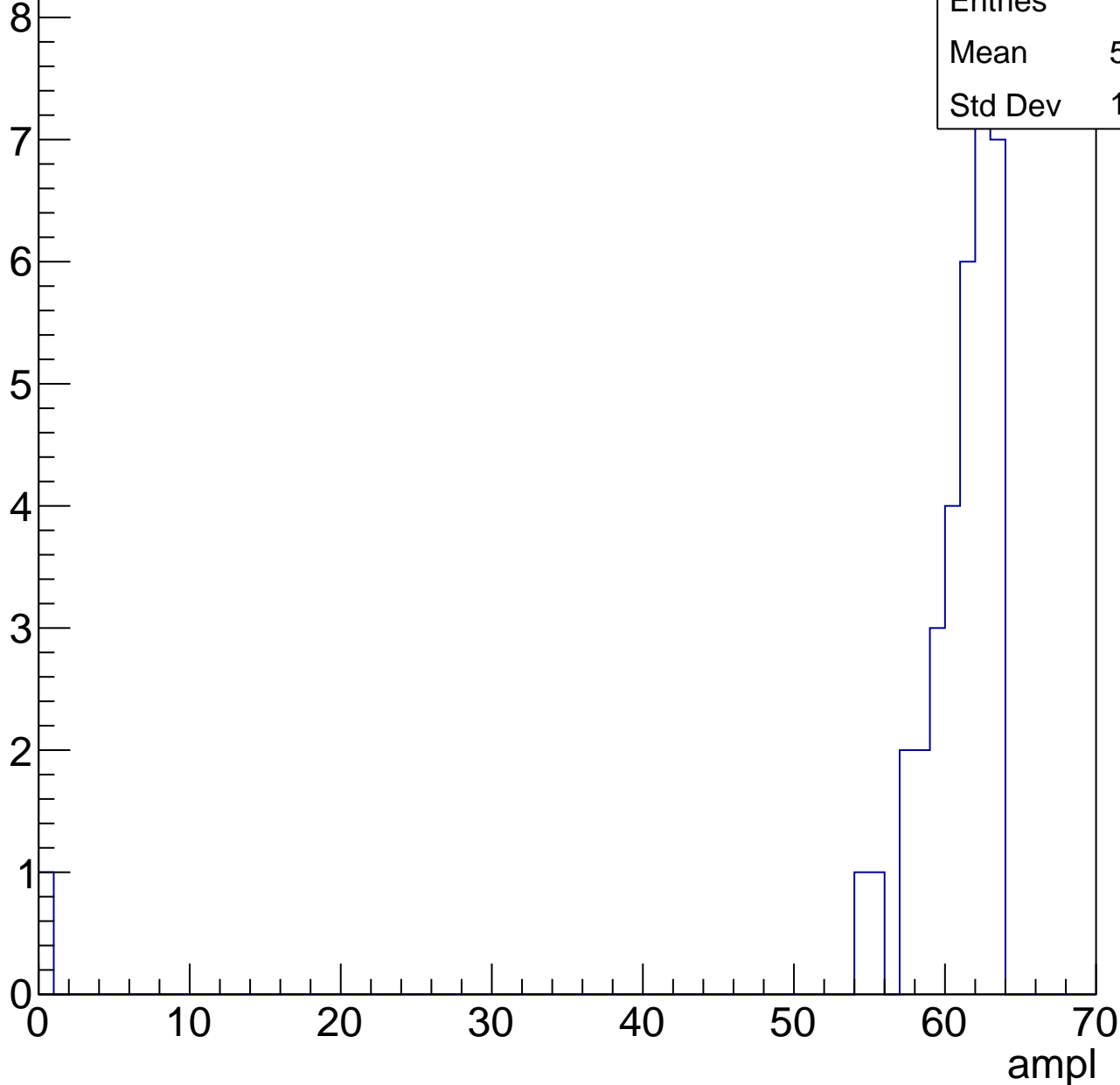


# B1L101S, U22-ch113, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	35
Mean	58.83
Std Dev	10.34



# B1L101S, U22-ch113, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

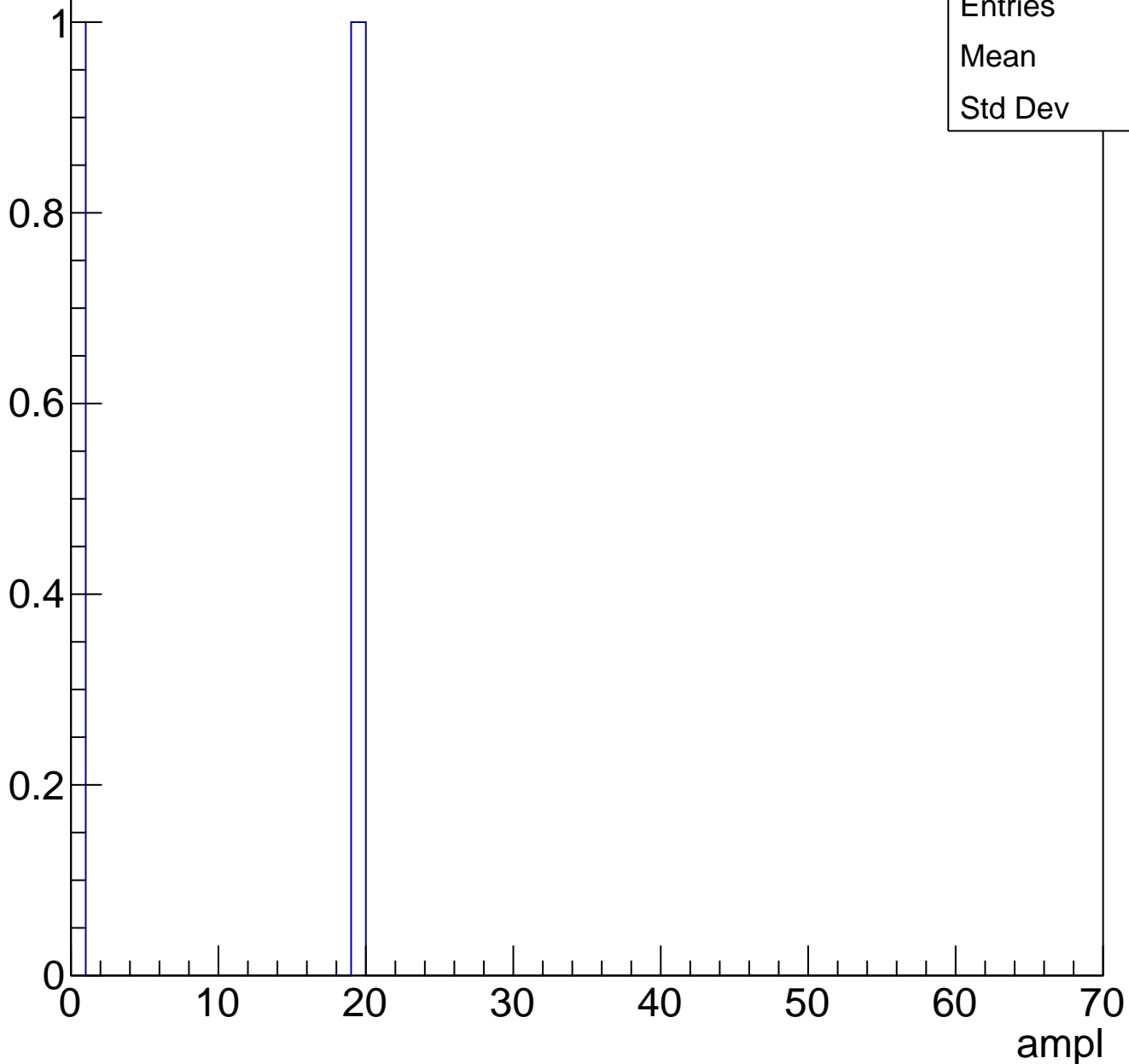




# B1L101S, U22-ch113, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U22-ch114, adc0

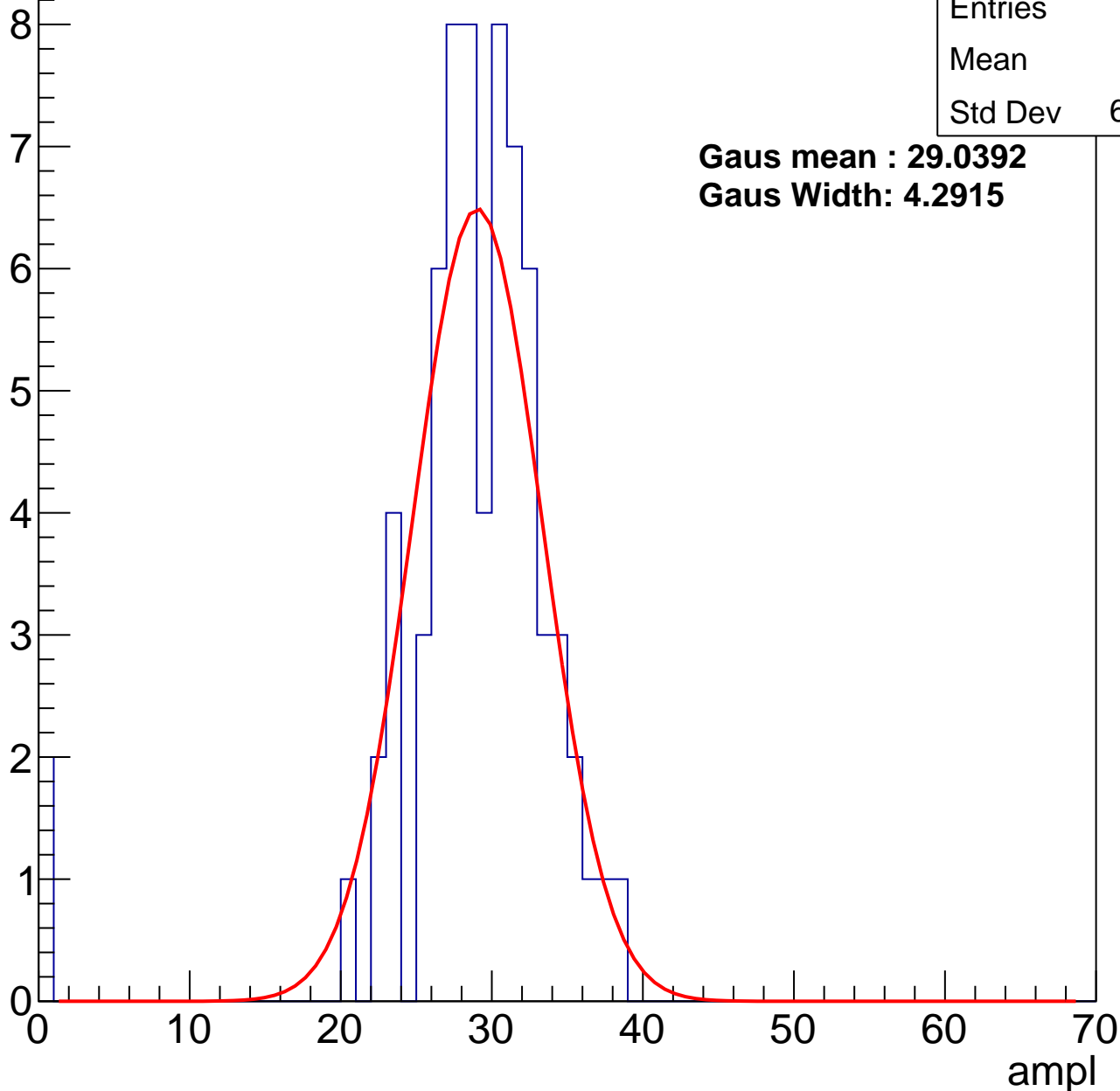
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	28.2
Std Dev	6.072

**Gaus mean : 29.0392**

**Gaus Width: 4.2915**



# B1L101S, U22-ch114, adc1

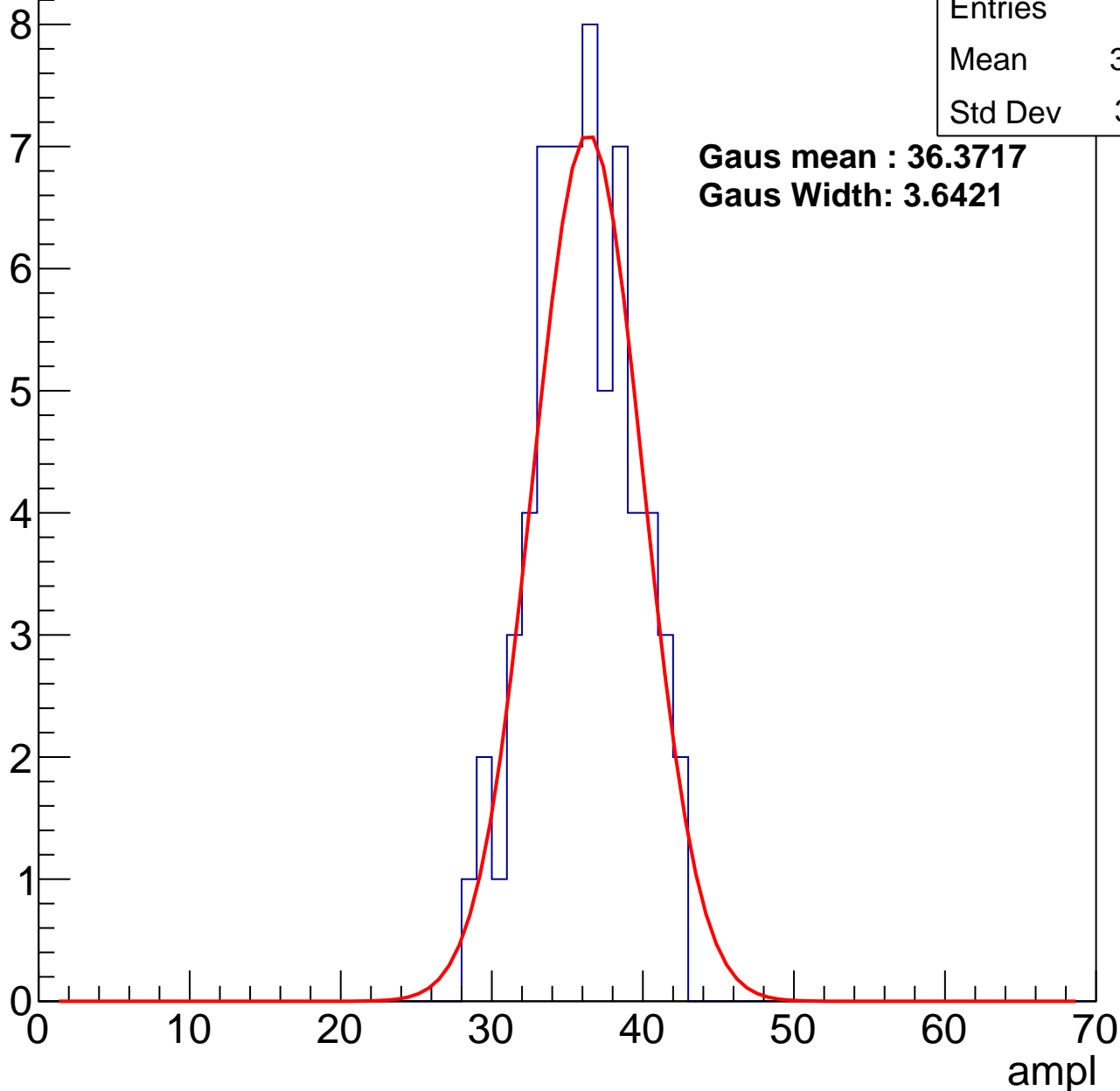
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	35.58
Std Dev	3.291

**Gaus mean : 36.3717**

**Gaus Width: 3.6421**



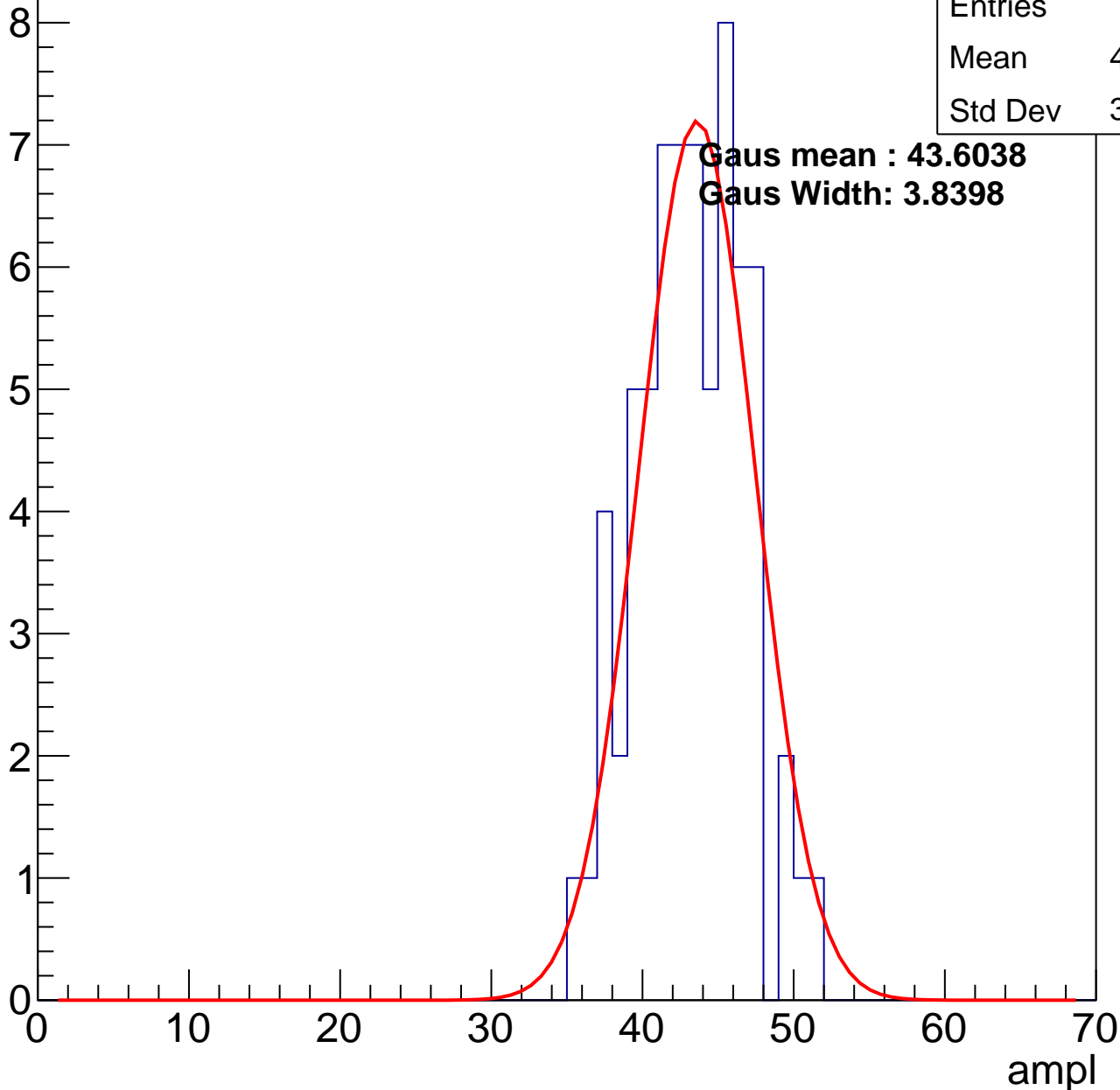
# B1L101S, U22-ch114, adc2

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	42.78
Std Dev	3.506

**Gaus mean : 43.6038**  
**Gaus Width: 3.8398**

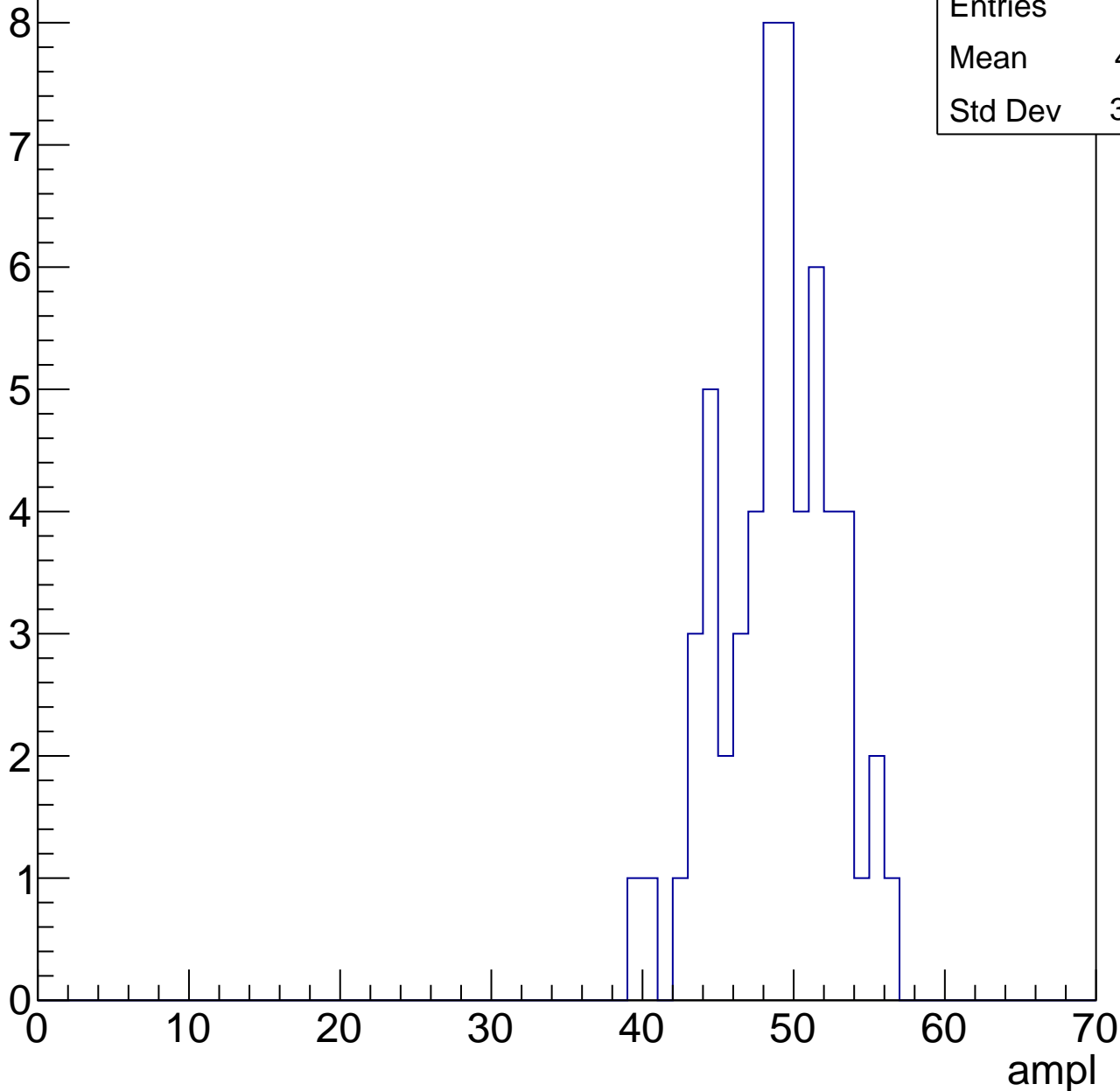


# B1L101S, U22-ch114, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	58
Mean	48.41
Std Dev	3.714

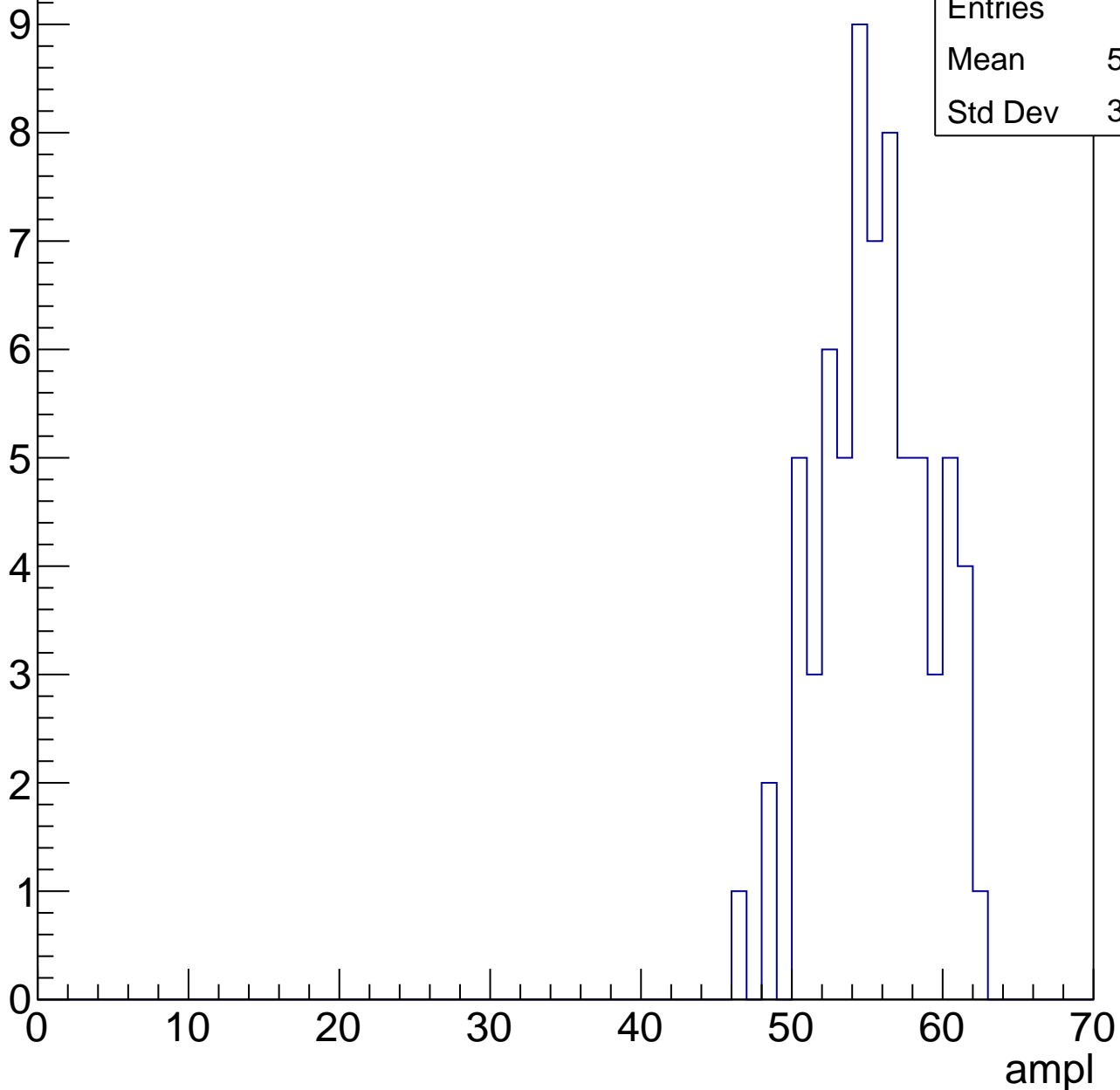


# B1L101S, U22-ch114, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	55.06
Std Dev	3.559

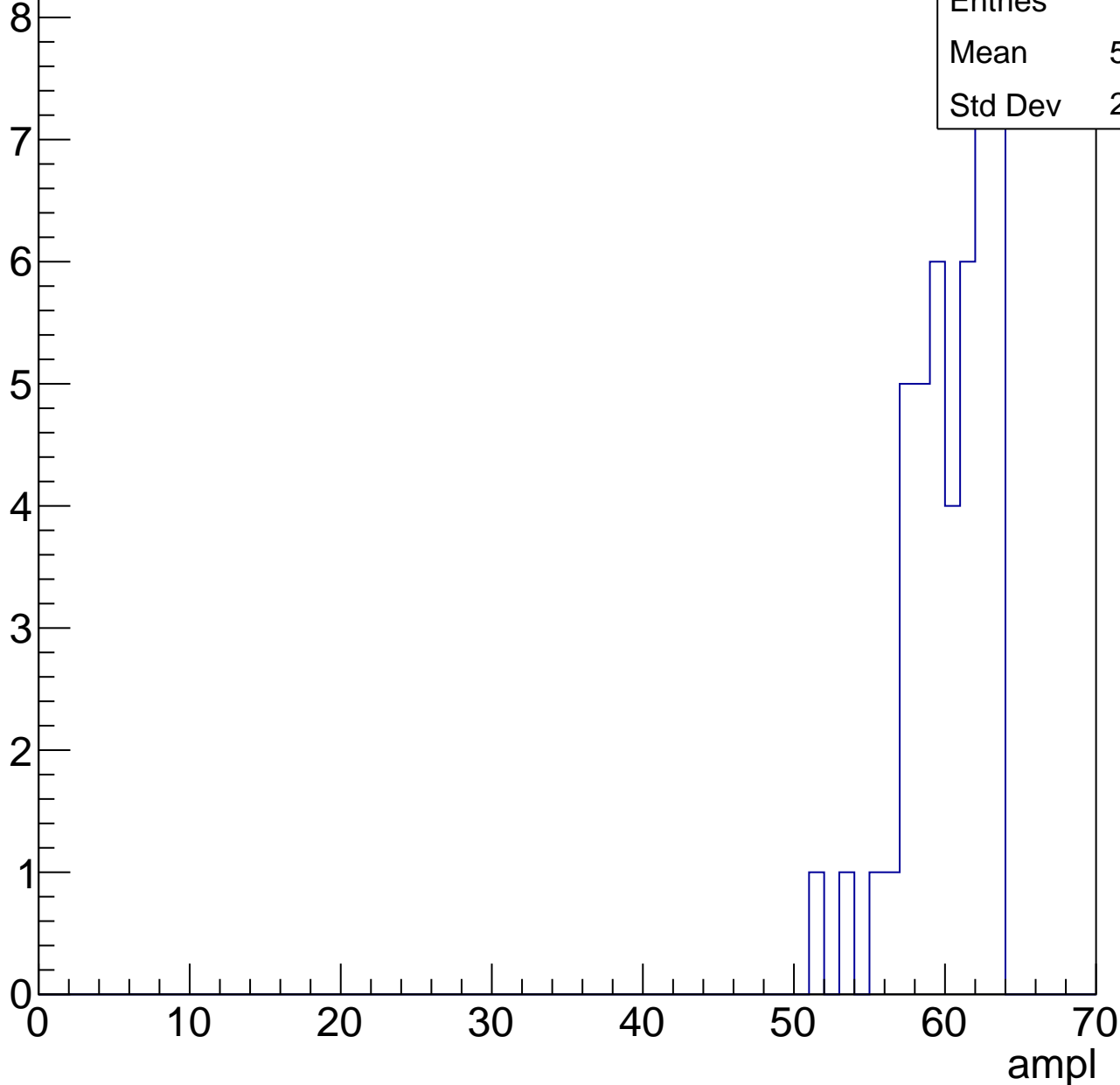


# B1L101S, U22-ch114, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	46
Mean	59.78
Std Dev	2.758



# B1L101S, U22-ch114, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

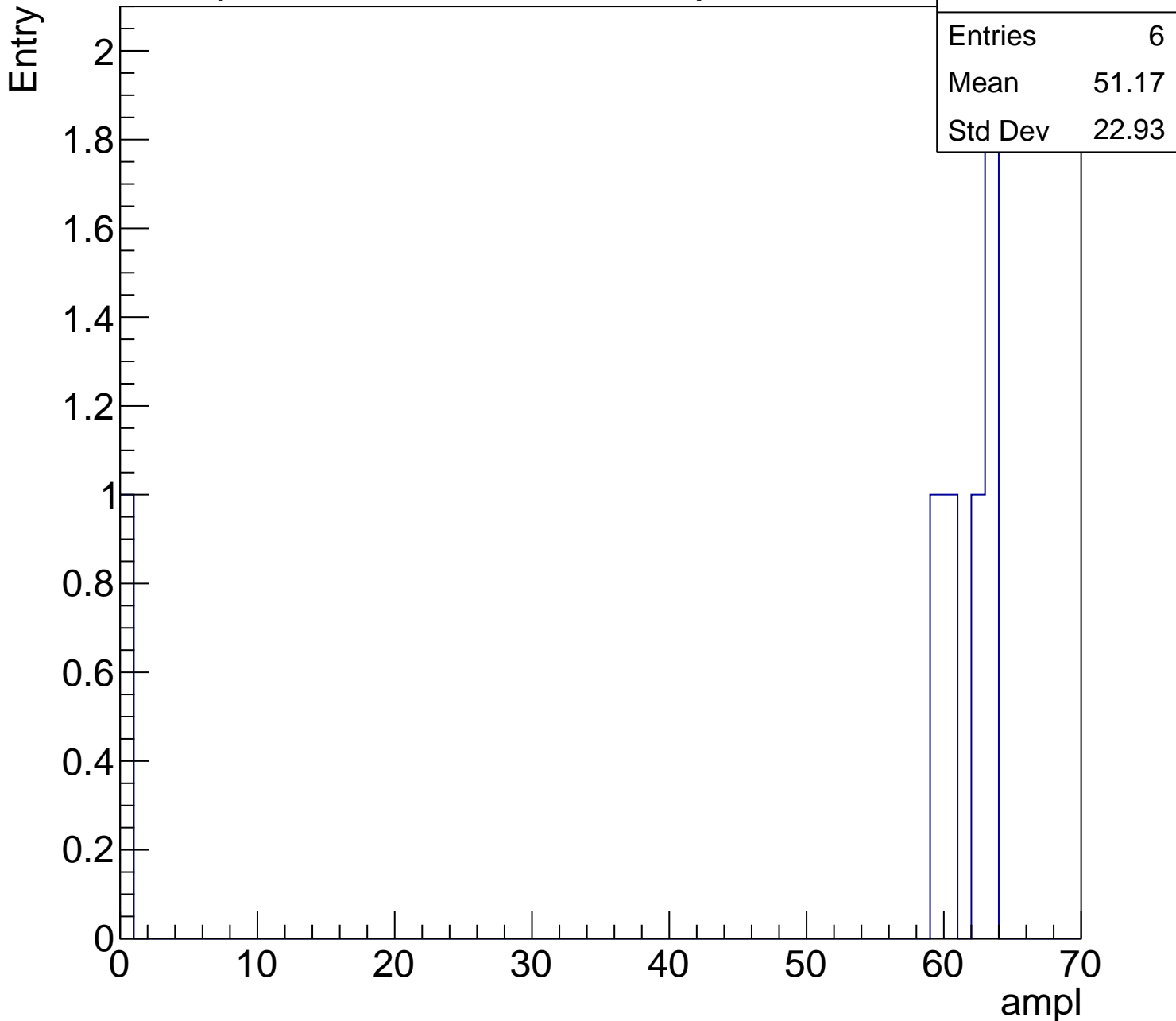
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	6
Mean	51.17
Std Dev	22.93

0 10 20 30 40 50 60 70

ampl





# B1L101S, U22-ch114, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U22-ch115, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	88
Mean	30.64
Std Dev	3.847

**Gaus mean : 30.9569**

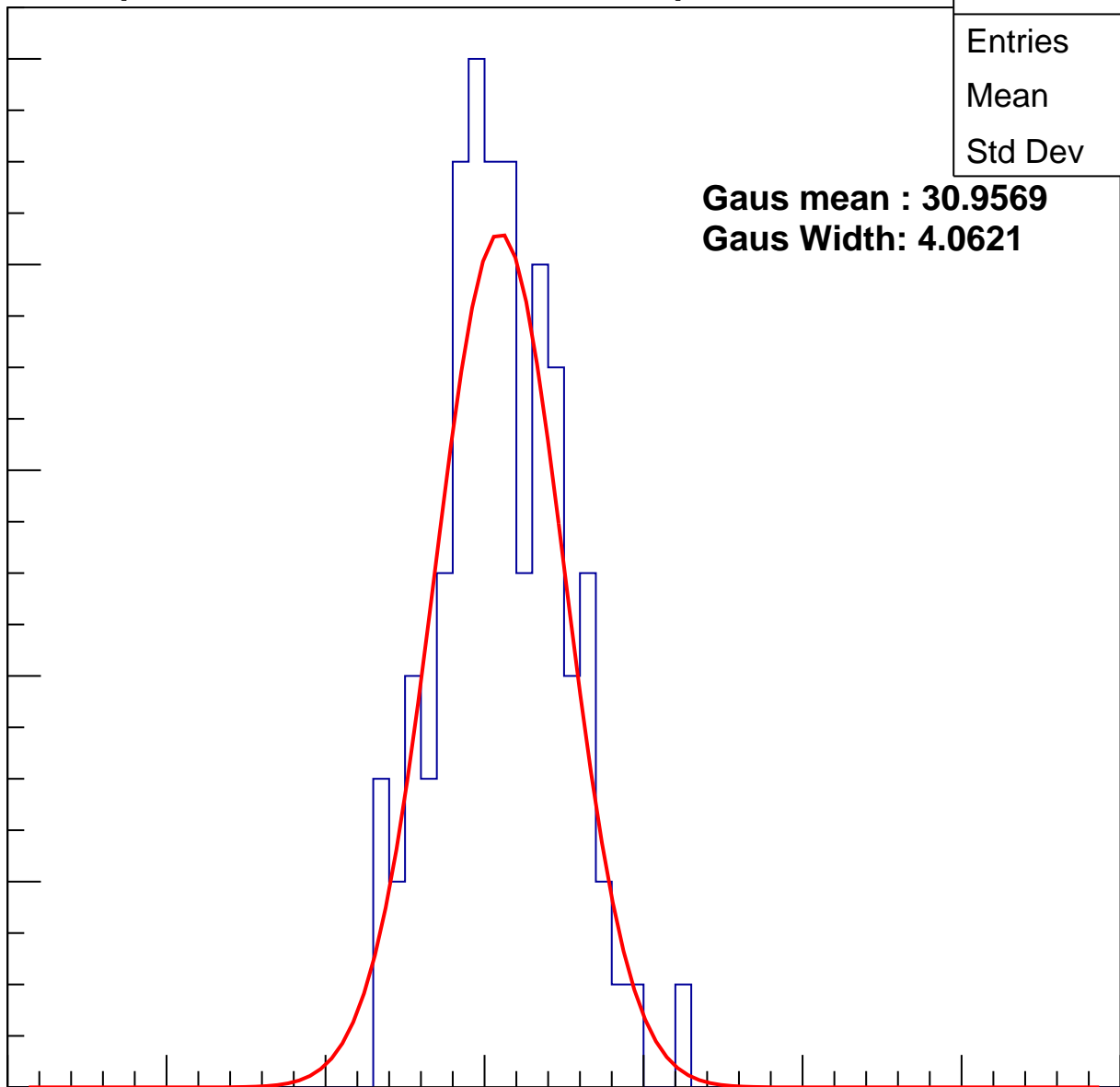
**Gaus Width: 4.0621**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U22-ch115, adc1

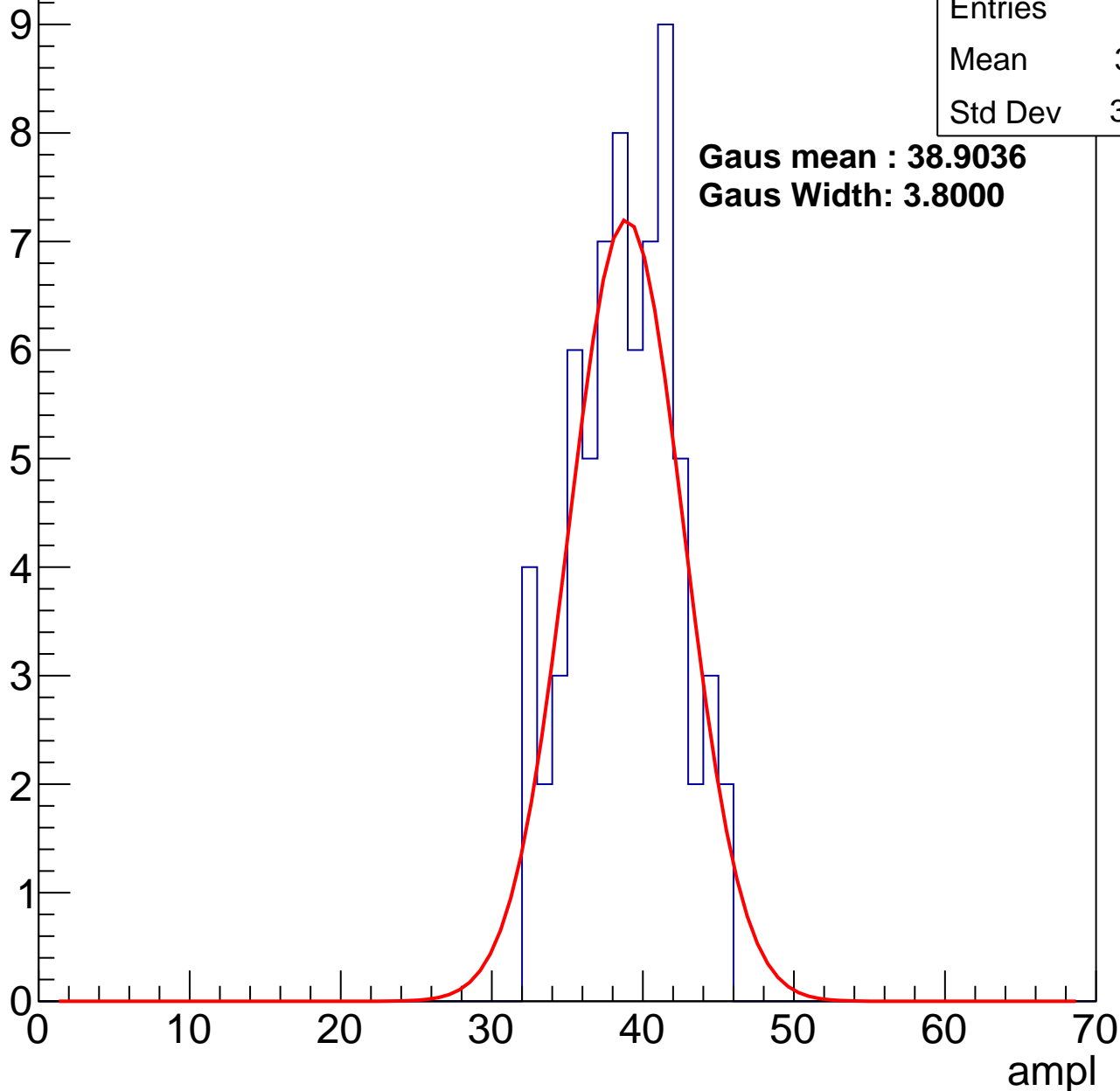
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	38.41
Std Dev	3.325

**Gaus mean : 38.9036**

**Gaus Width: 3.8000**



# B1L101S, U22-ch115, adc2

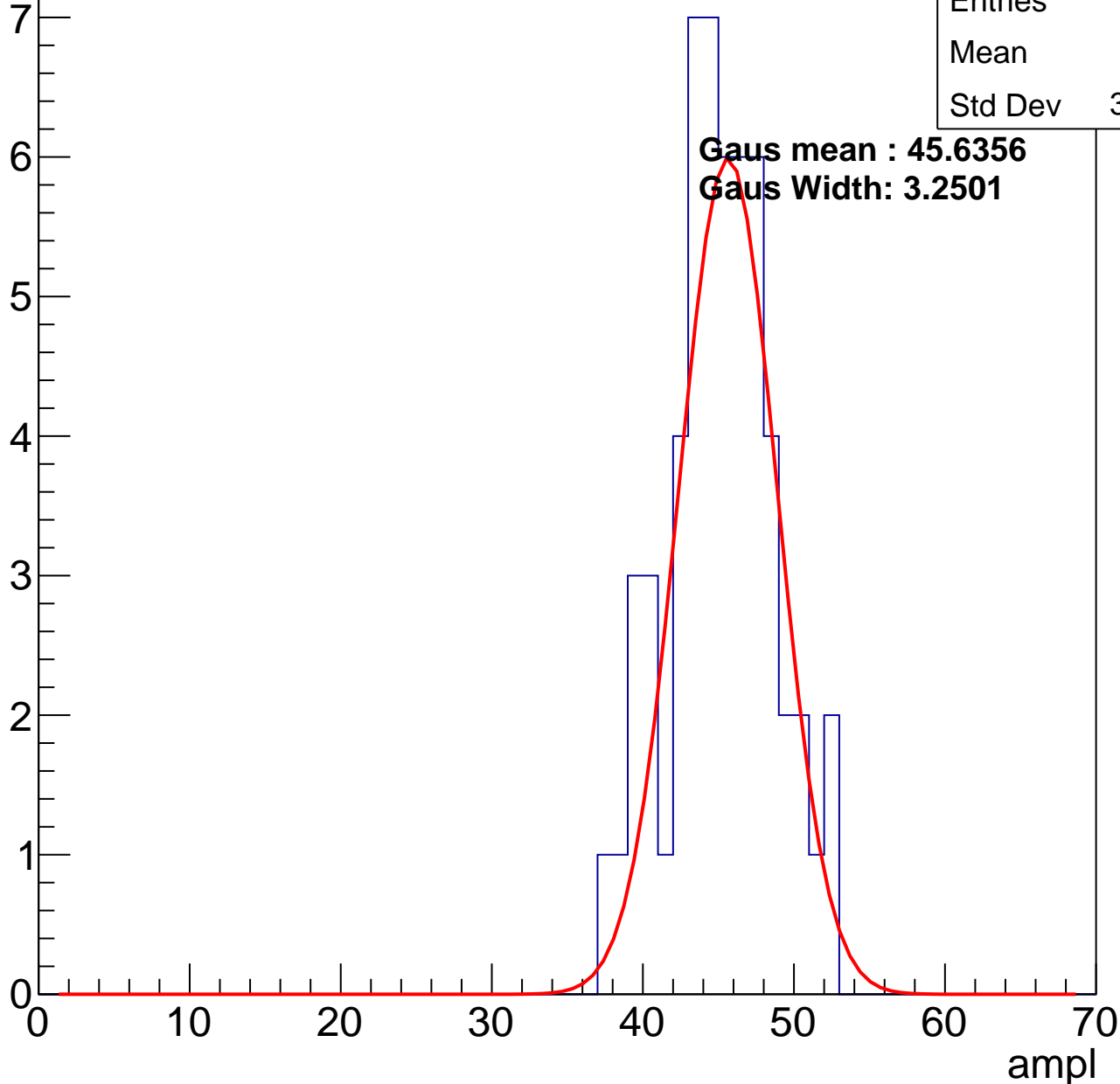
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	56
Mean	44.7
Std Dev	3.433

**Gaus mean : 45.6356**

**Gaus Width: 3.2501**

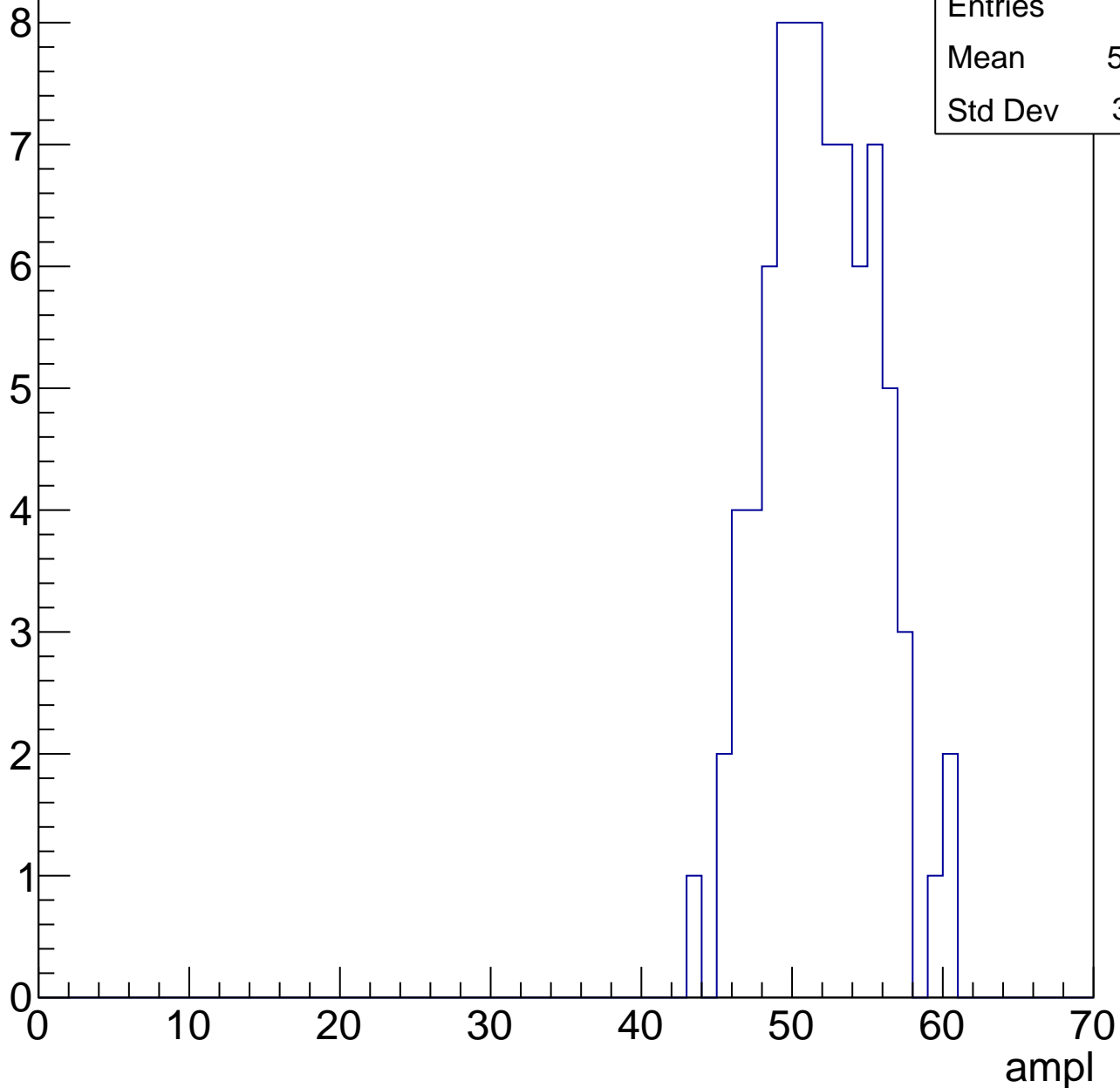


# B1L101S, U22-ch115, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	79
Mean	51.48
Std Dev	3.621

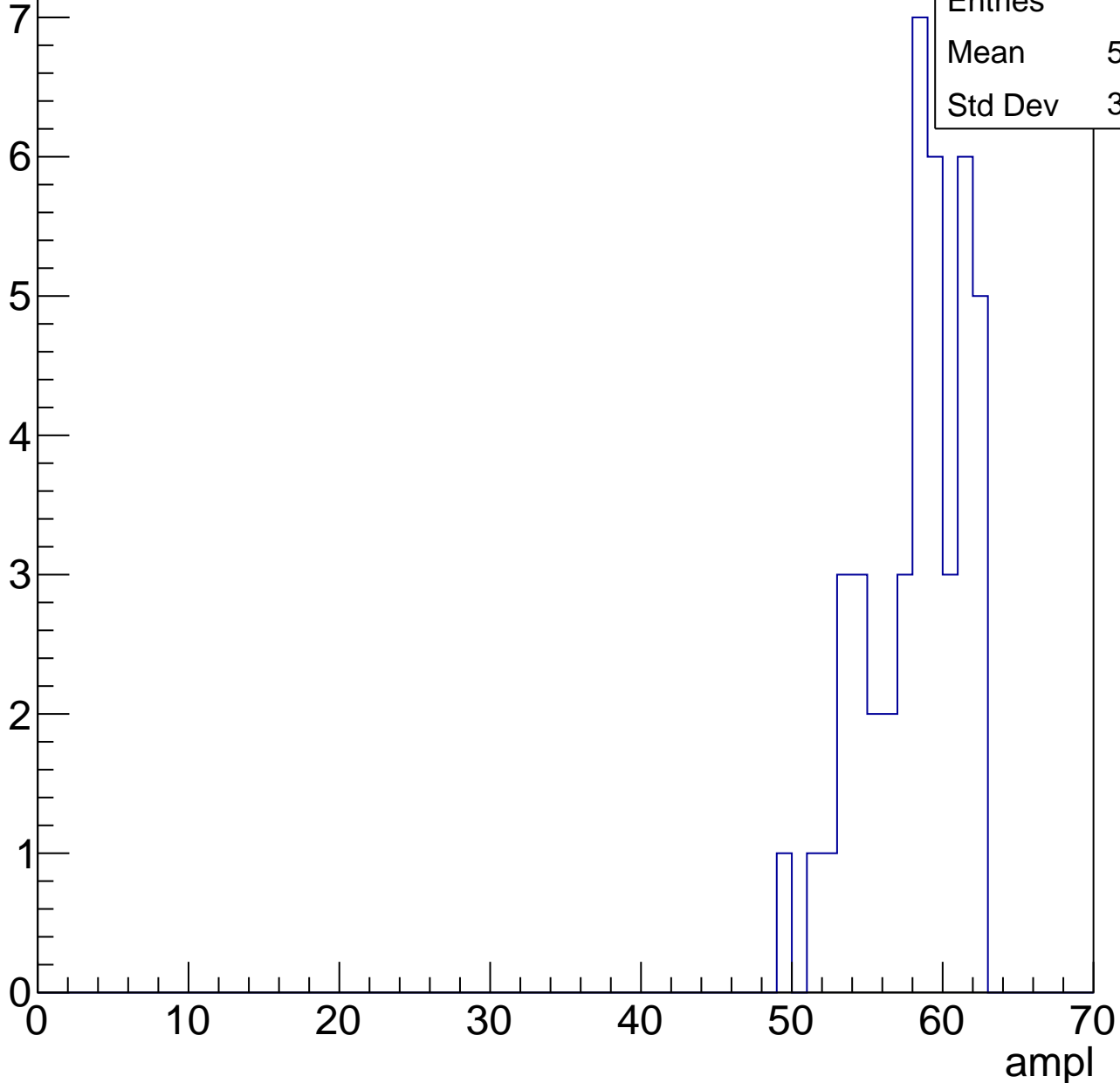


# B1L101S, U22-ch115, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	43
Mean	57.72
Std Dev	3.294

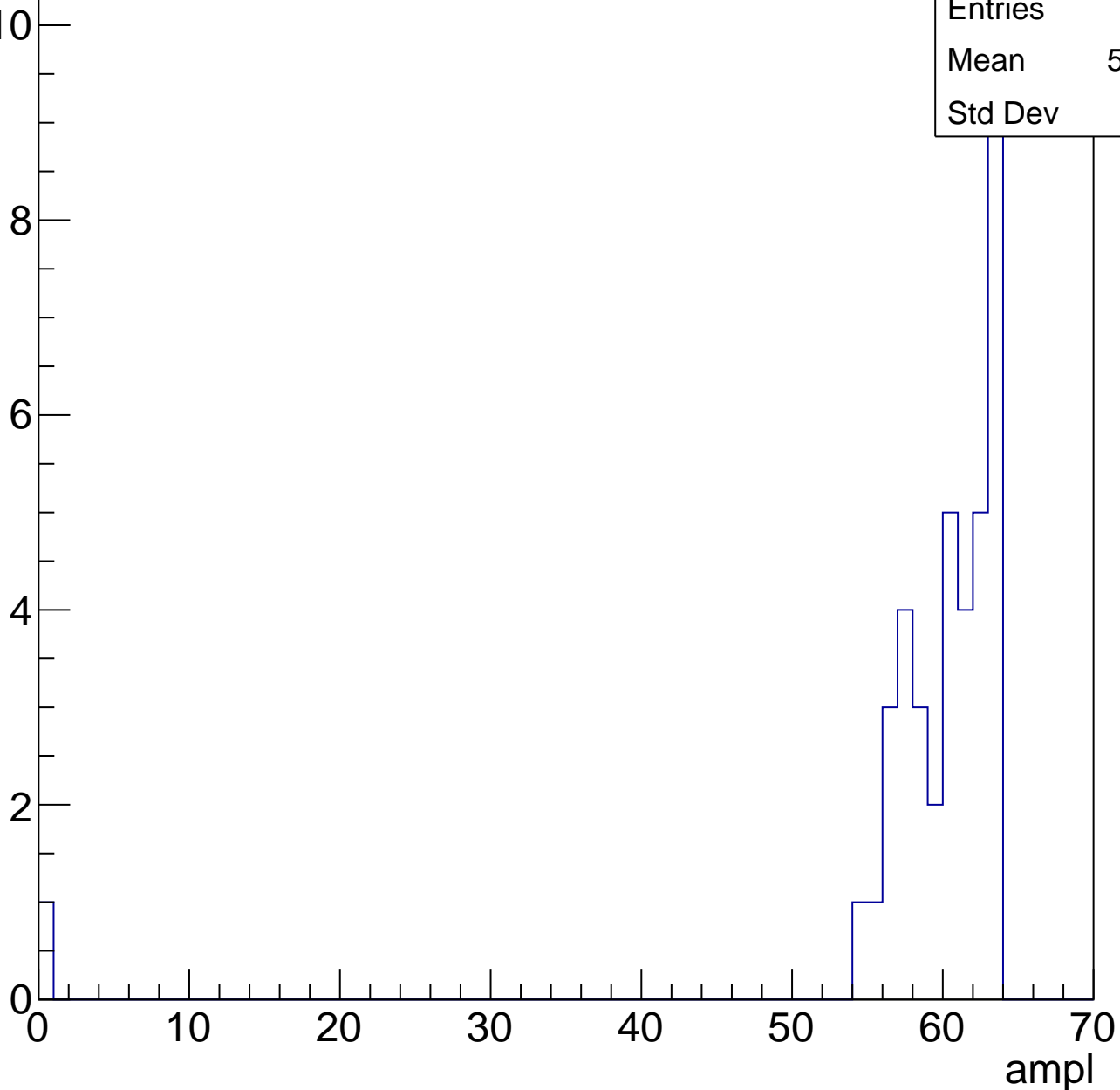


# B1L101S, U22-ch115, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

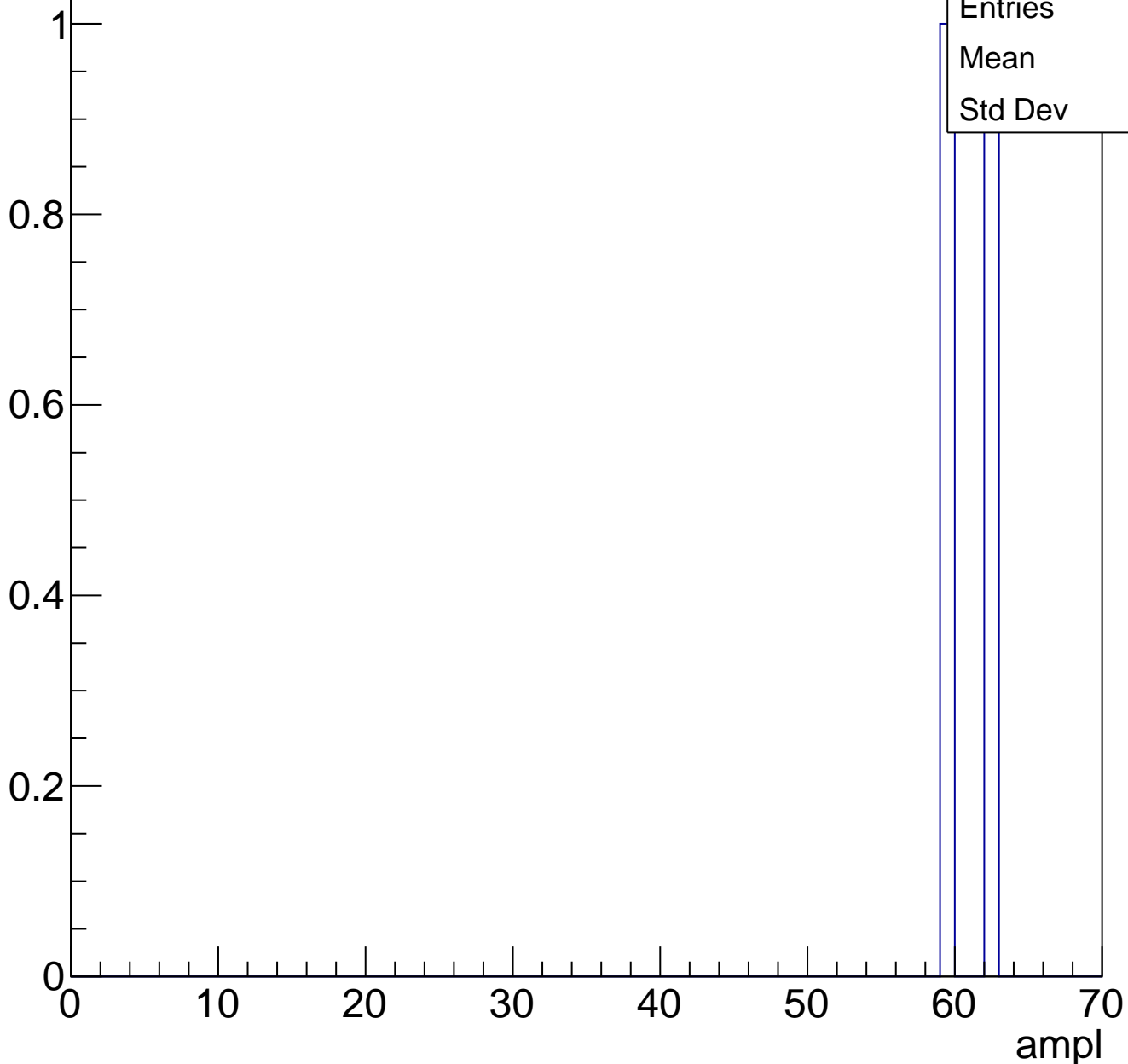
Entries	39
Mean	58.49
Std Dev	9.85



# B1L101S, U22-ch115, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U22-ch115, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U22-ch116, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	84
Mean	27.82
Std Dev	6.4

**Gaus mean : 29.3893**

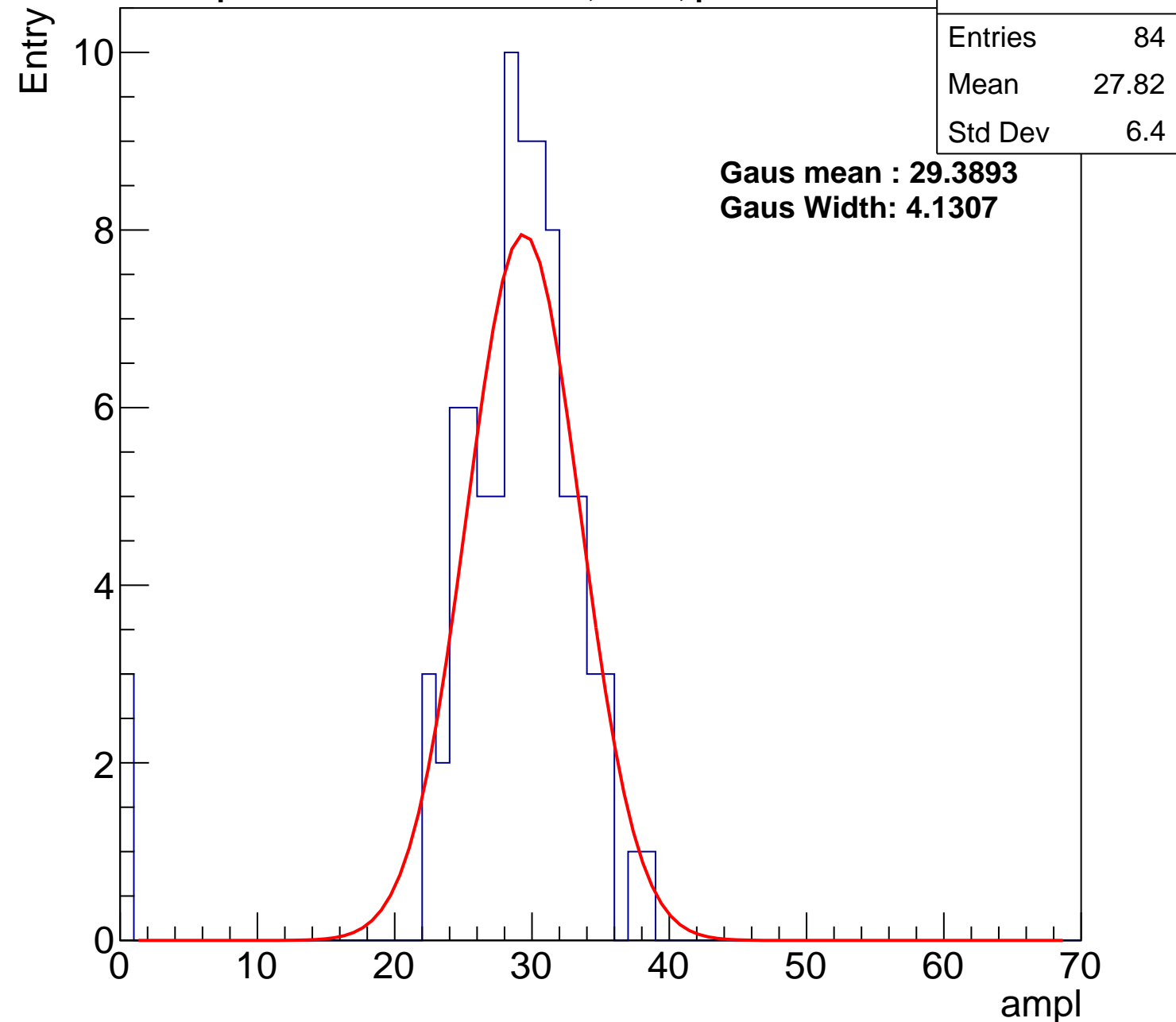
**Gaus Width: 4.1307**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U22-ch116, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	68
Mean	36.22
Std Dev	3.446

**Gaus mean : 36.9236**

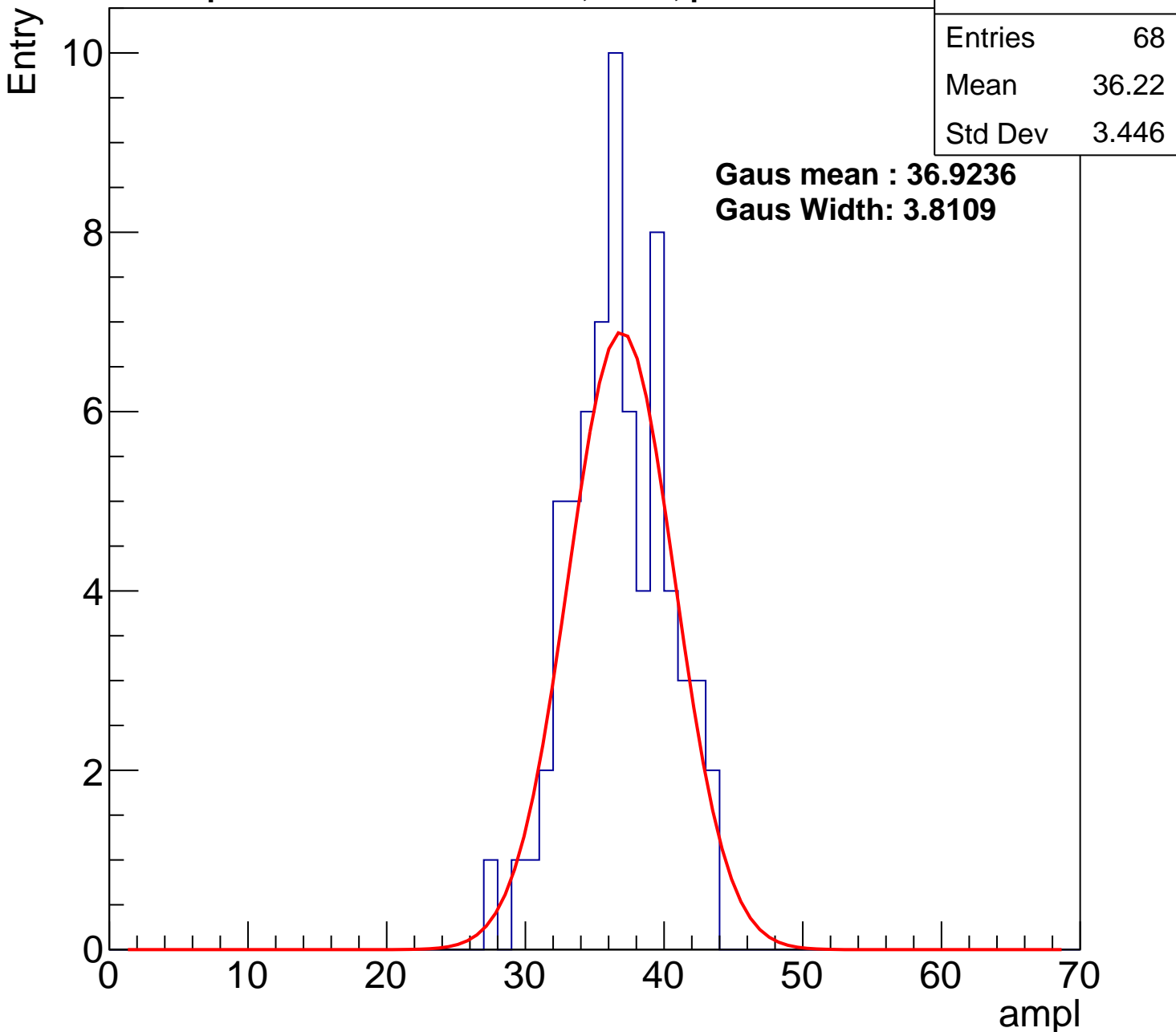
**Gaus Width: 3.8109**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B1L101S, U22-ch116, adc2

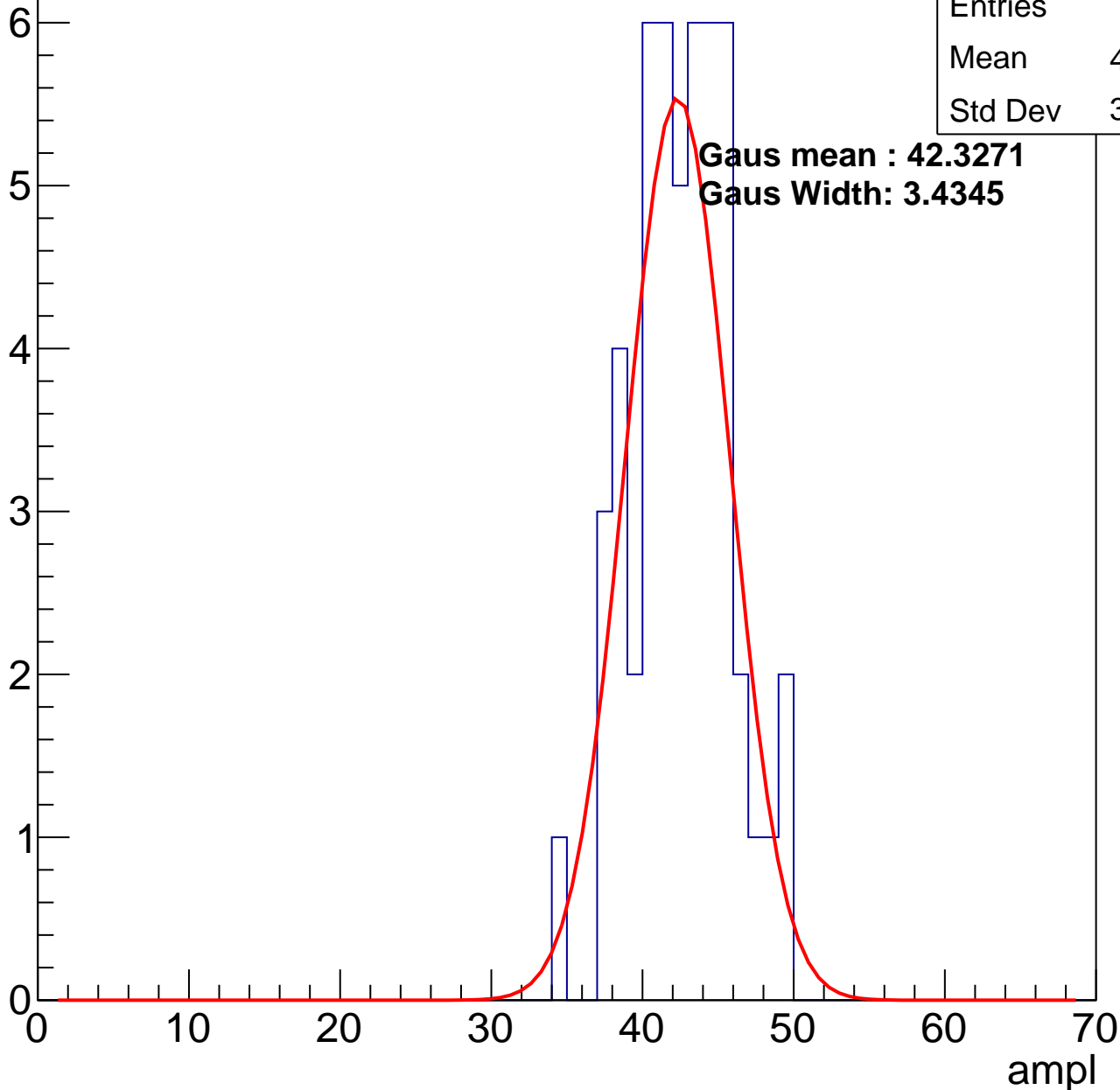
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	51
Mean	42.12
Std Dev	3.209

**Gaus mean : 42.3271**

**Gaus Width: 3.4345**

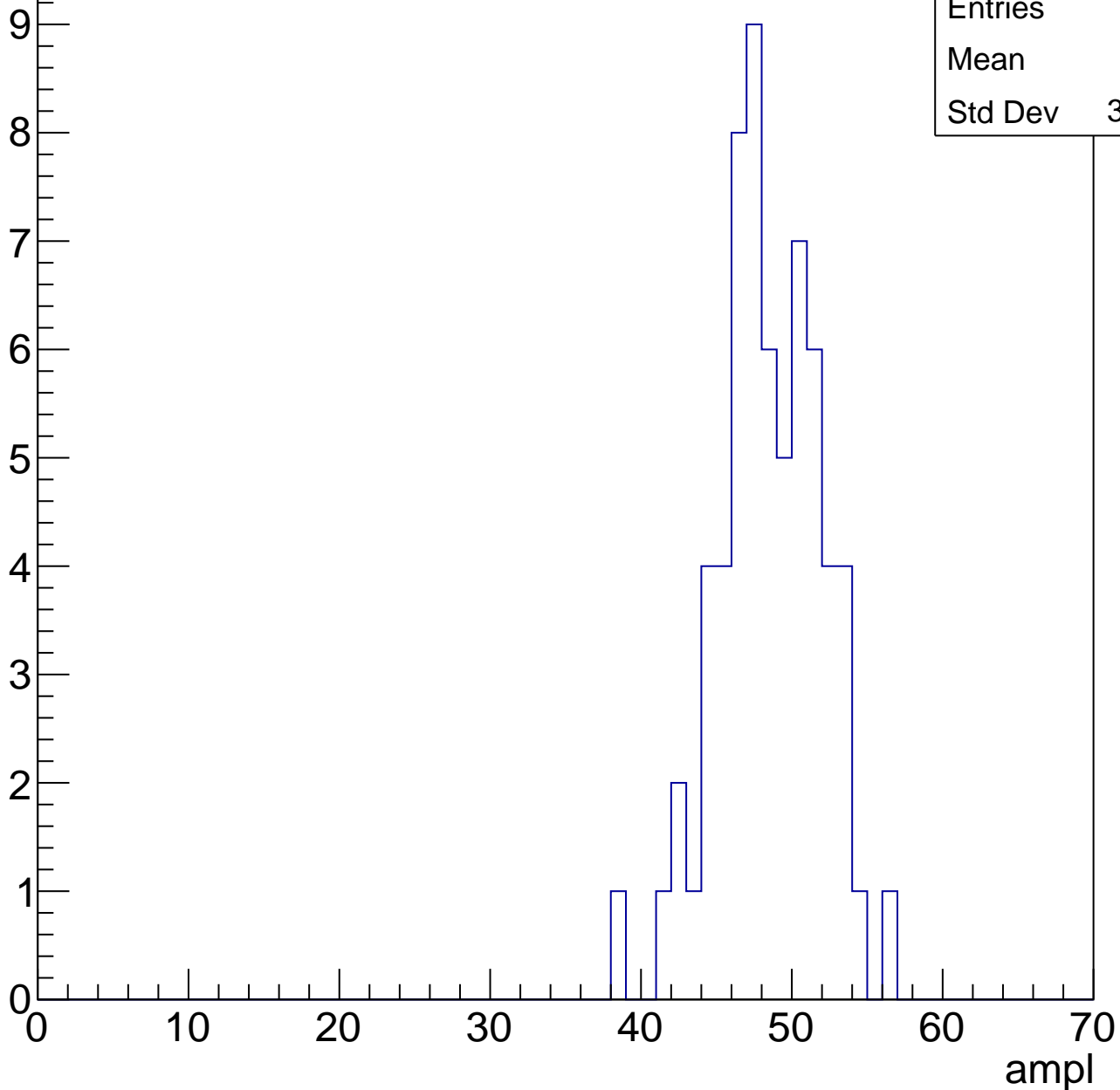


# B1L101S, U22-ch116, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	48
Std Dev	3.396

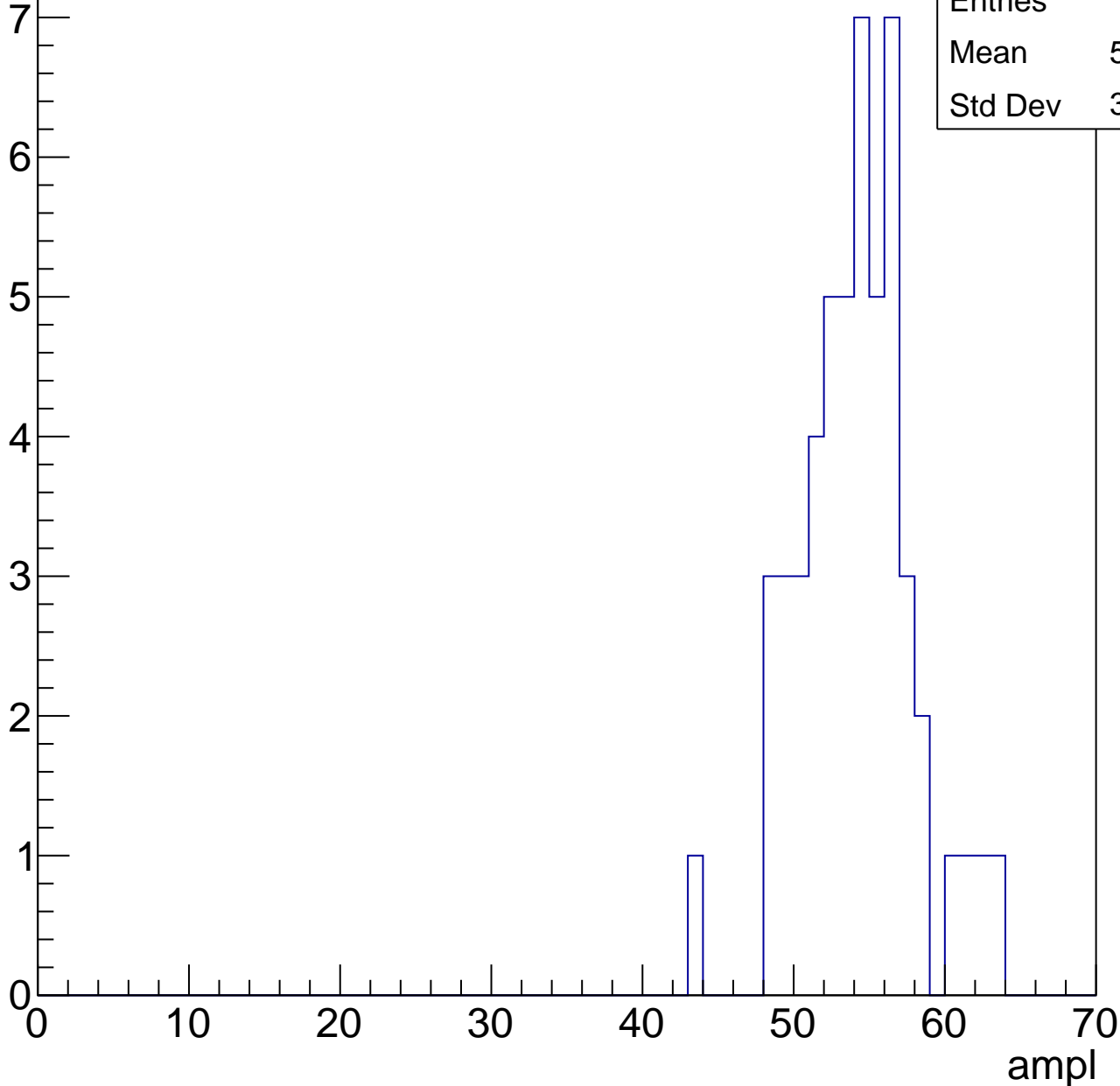


# B1L101S, U22-ch116, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

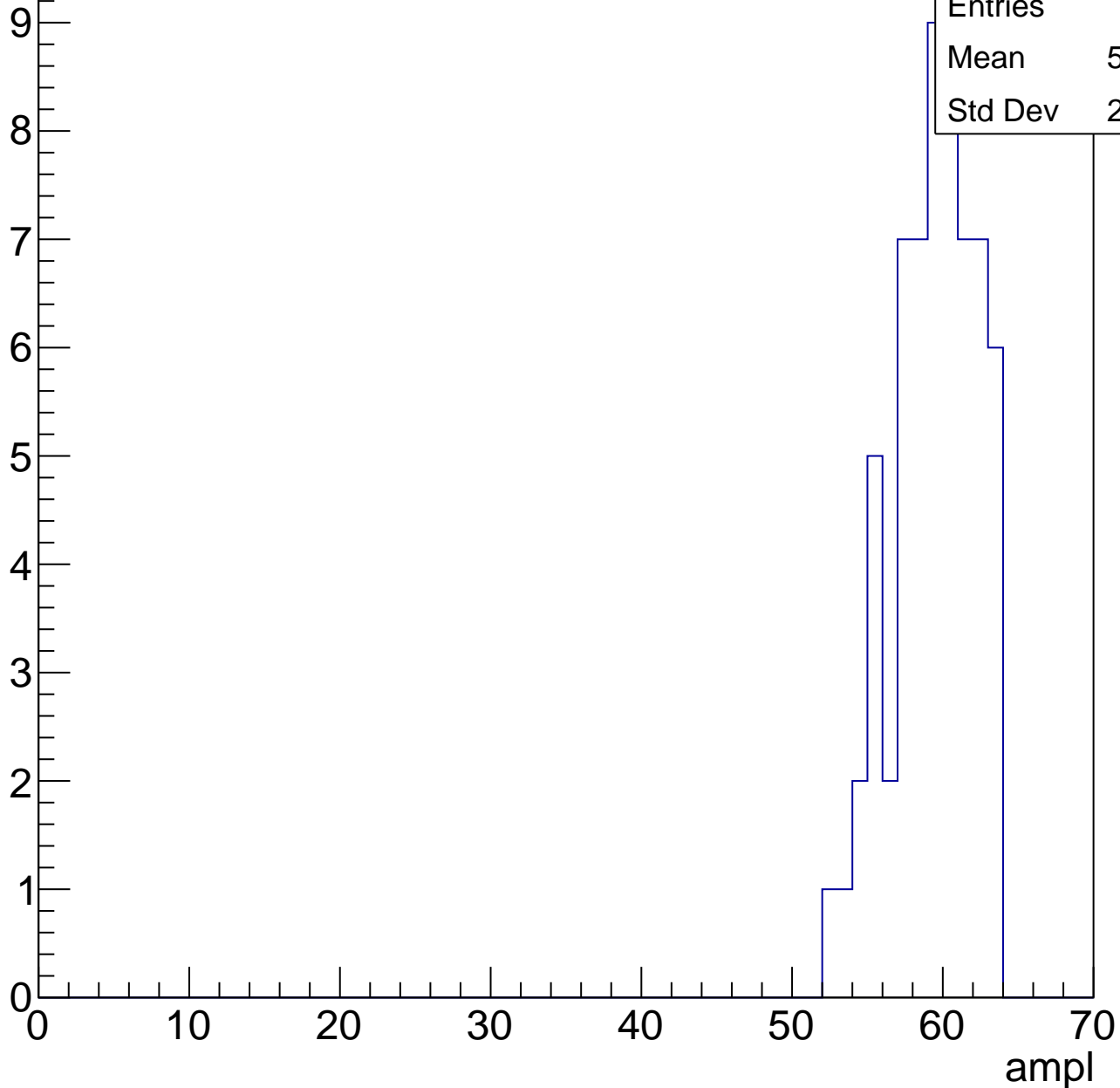
Entries	52
Mean	53.67
Std Dev	3.745



# B1L101S, U22-ch116, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

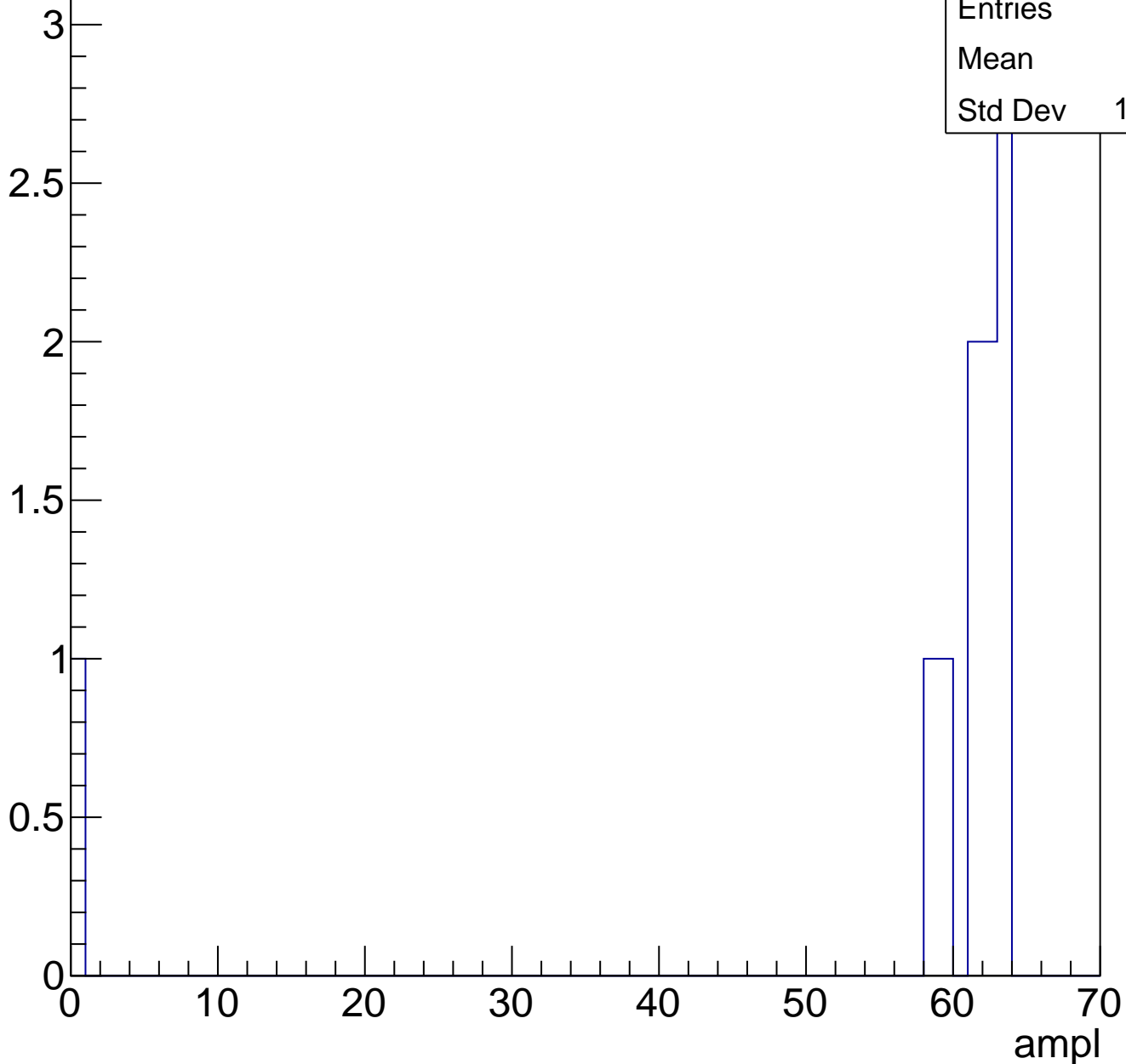


Entries	63
Mean	58.97
Std Dev	2.714

# B1L101S, U22-ch116, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

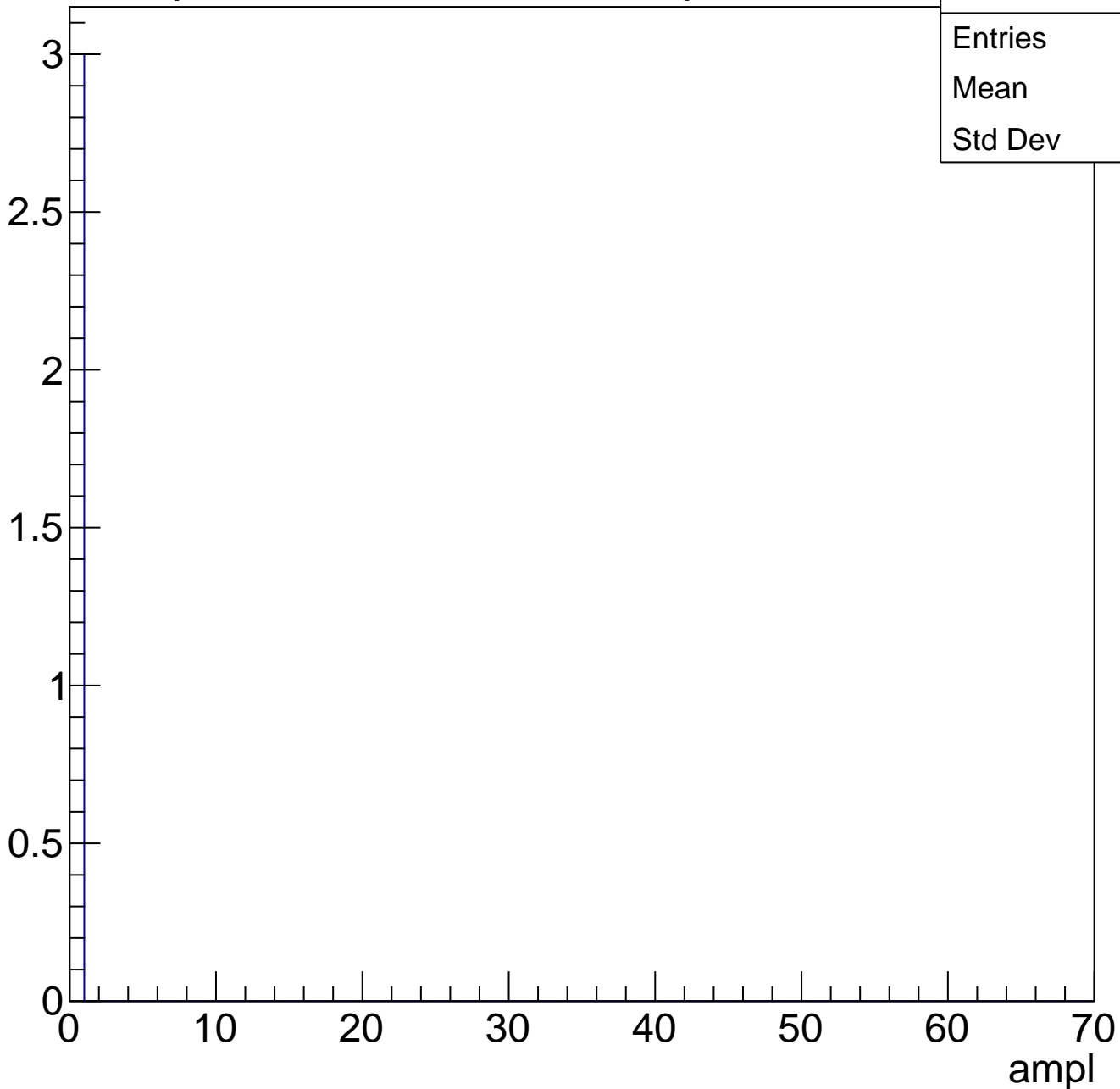




# B1L101S, U22-ch116, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	3
Mean	0
Std Dev	0

# B1L101S, U22-ch117, adc0

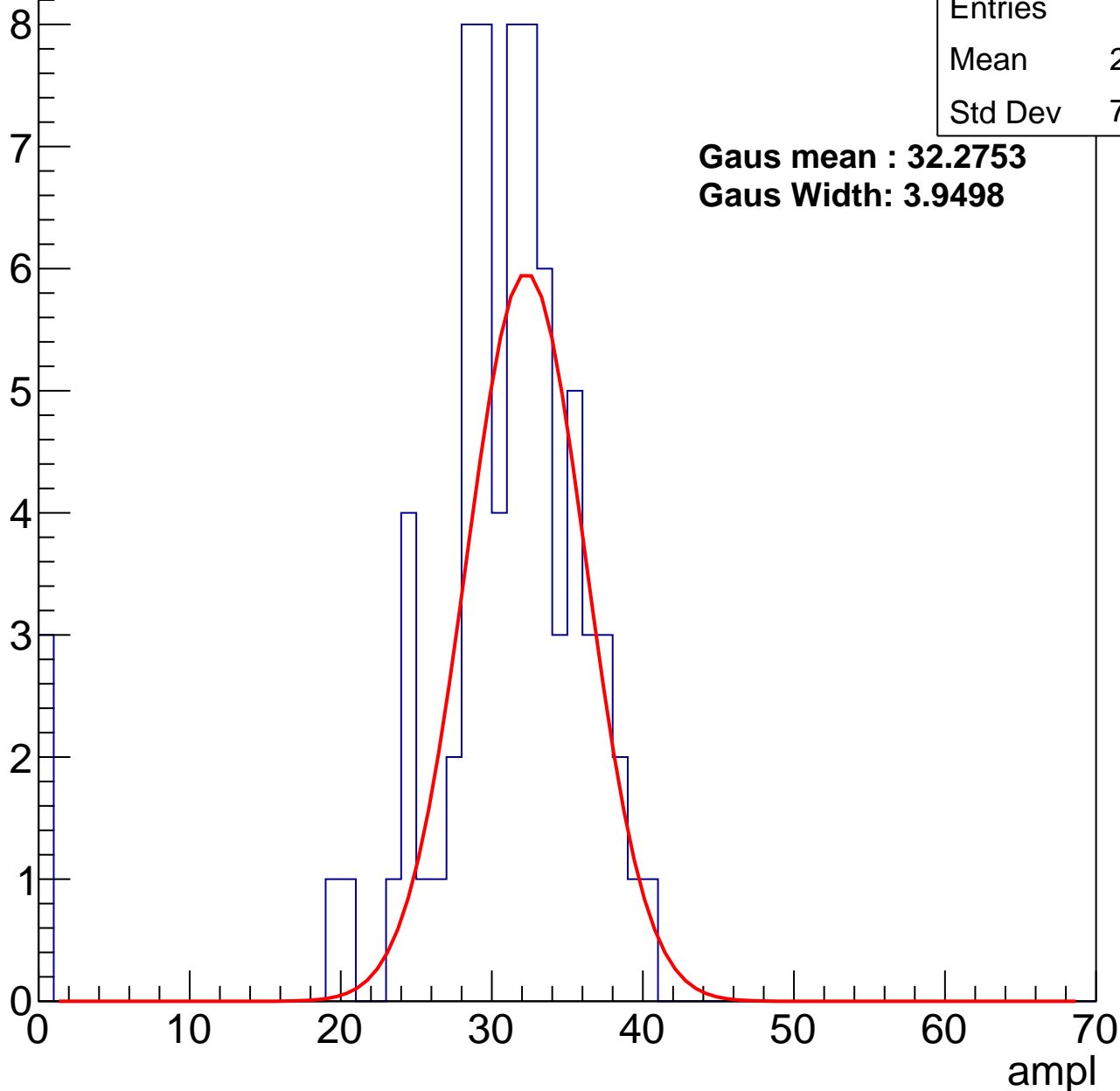
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	74
Mean	29.62
Std Dev	7.383

**Gaus mean : 32.2753**

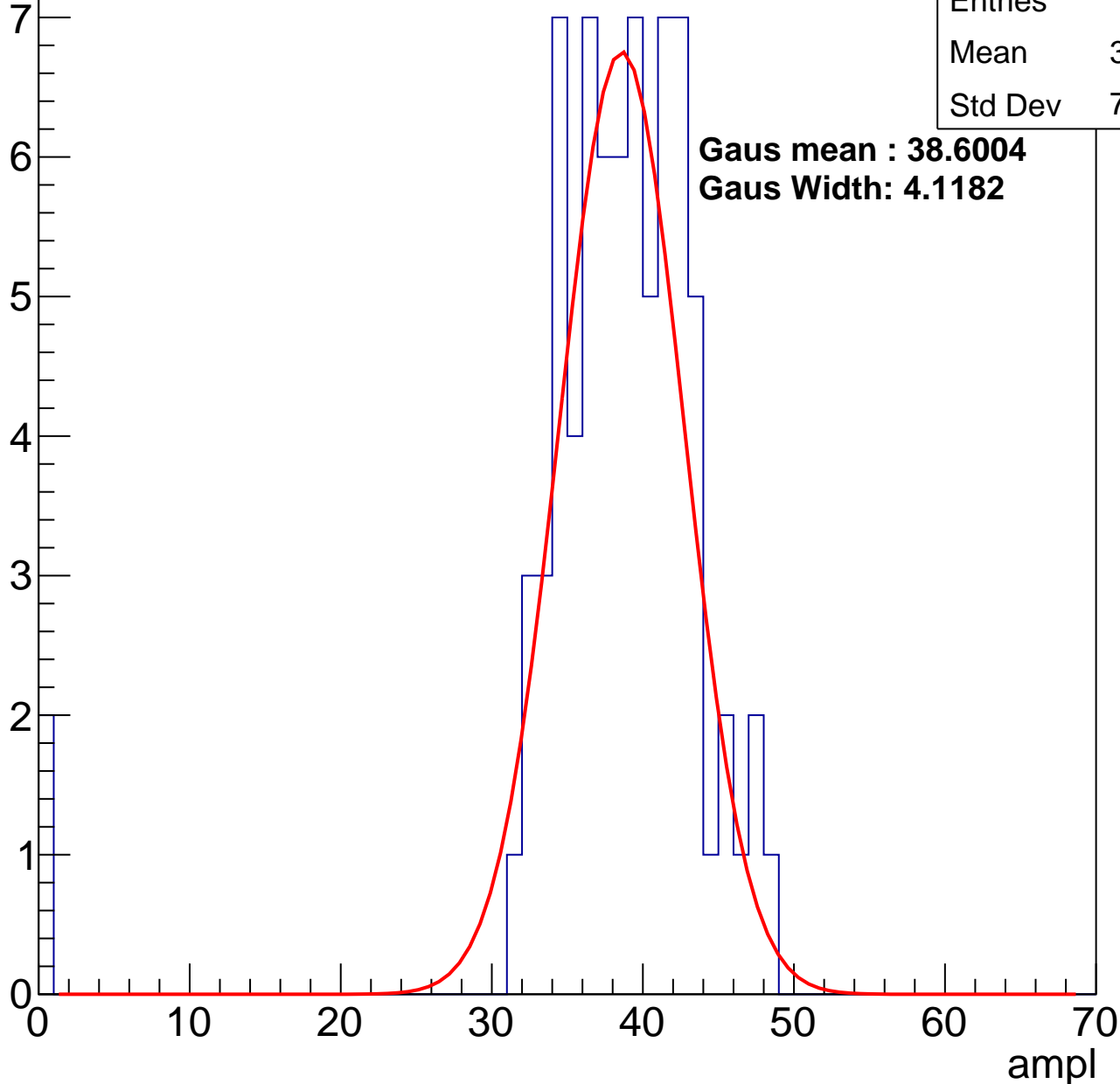
**Gaus Width: 3.9498**



# B1L101S, U22-ch117, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U22-ch117, adc2

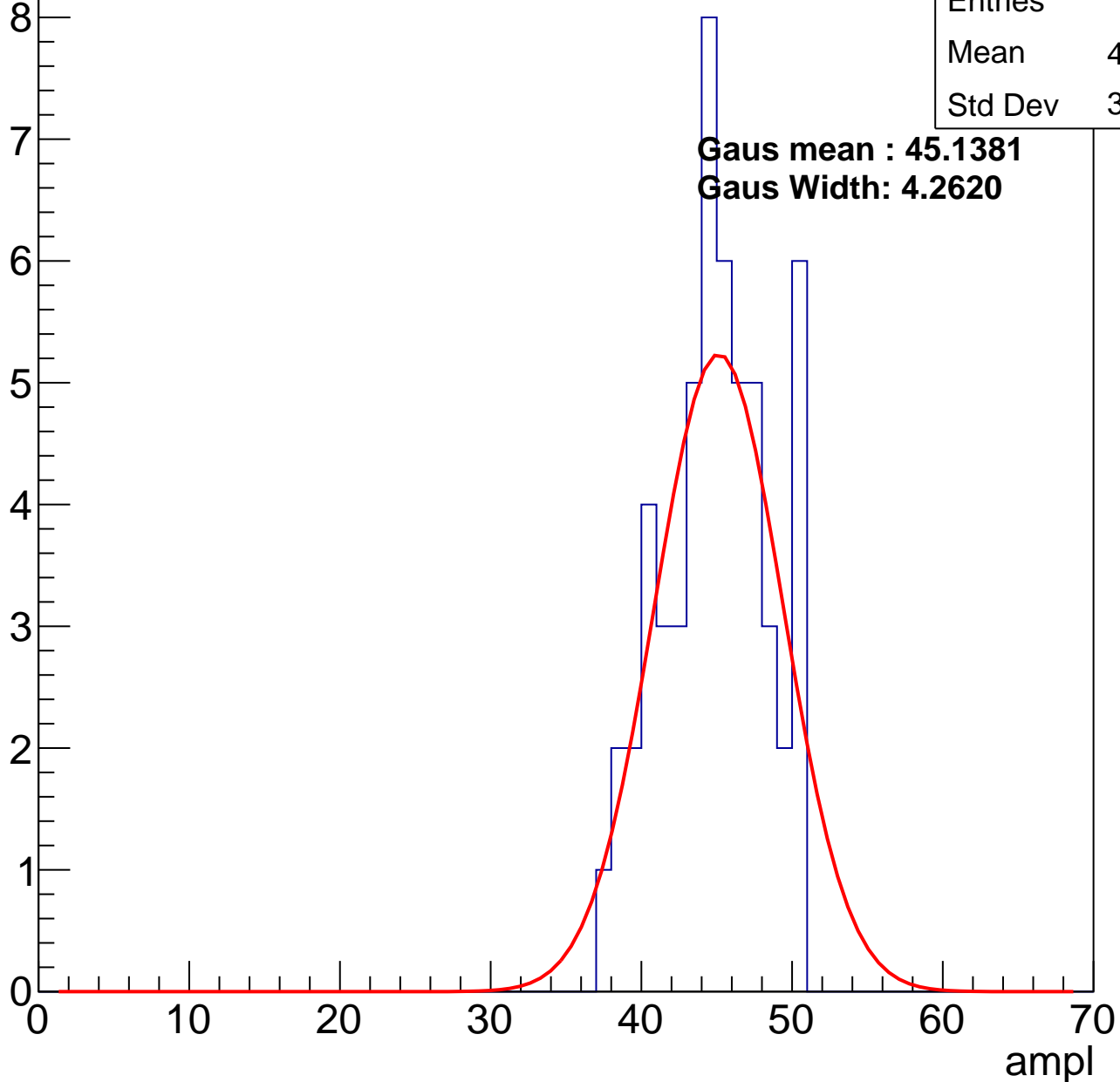
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	55
Mean	44.44
Std Dev	3.447

**Gaus mean : 45.1381**

**Gaus Width: 4.2620**



# B1L101S, U22-ch117, adc3

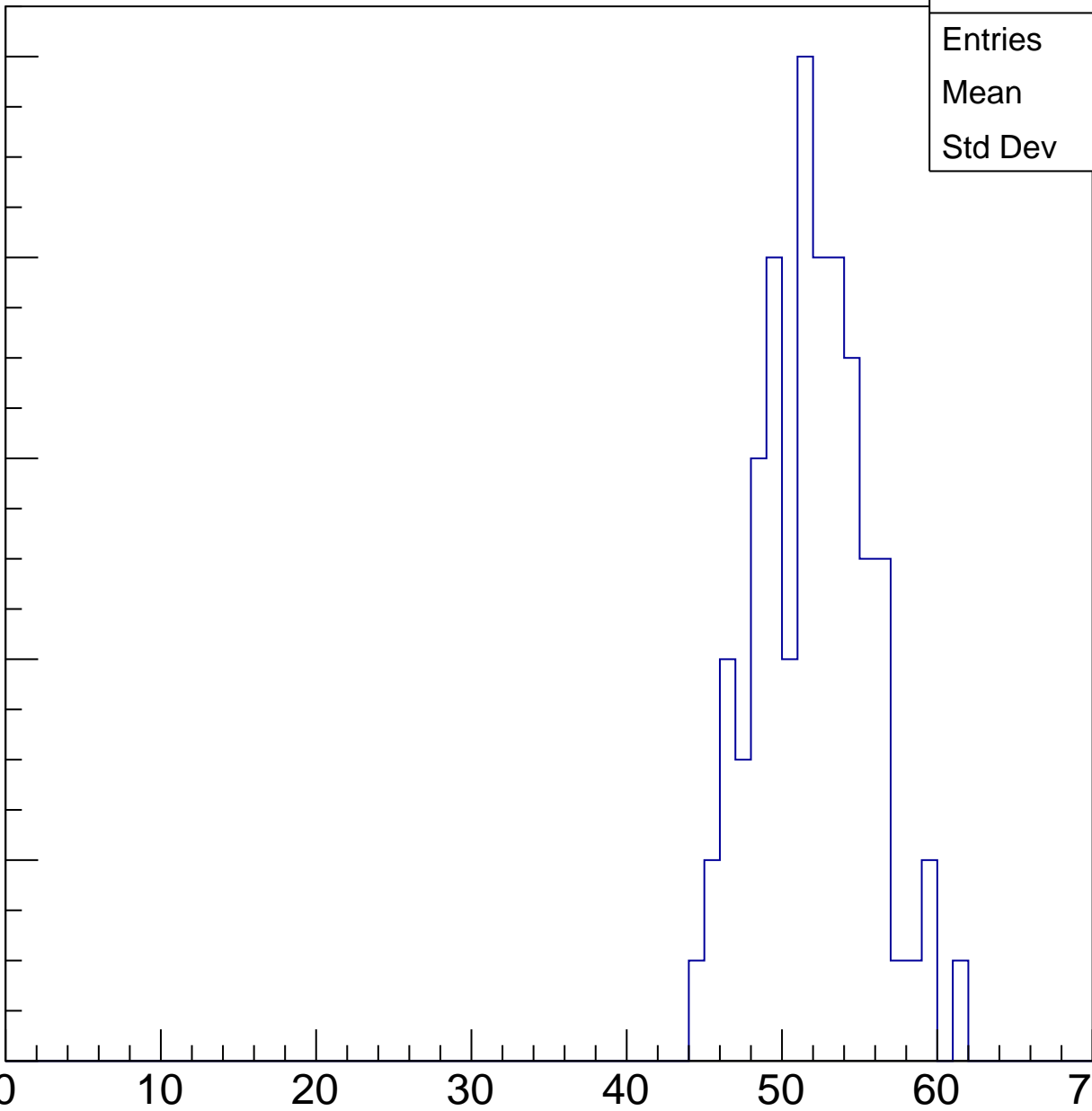
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	76
Mean	51.53
Std Dev	3.552

Entry

10  
8  
6  
4  
2  
0

ampl

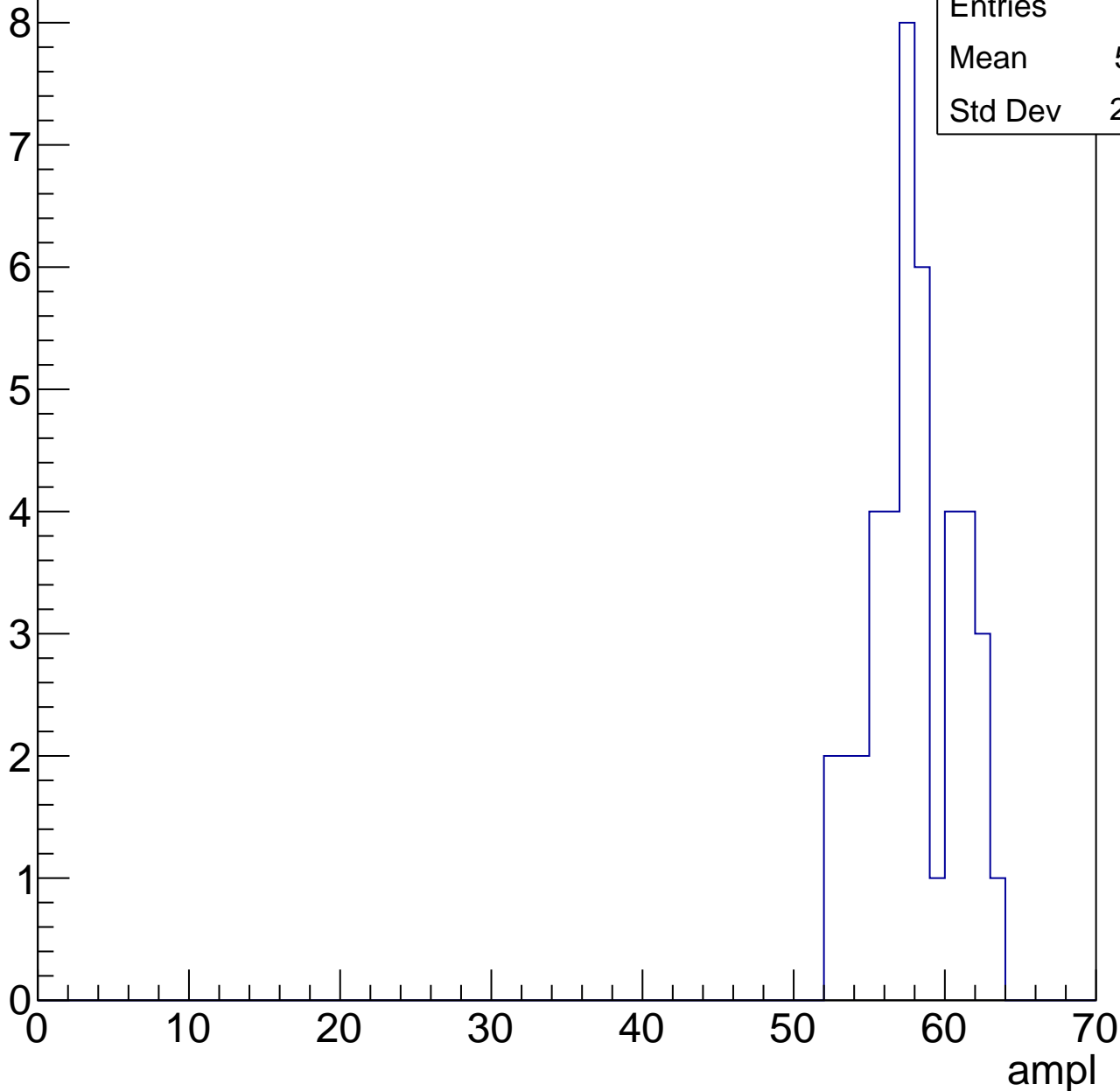


# B1L101S, U22-ch117, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

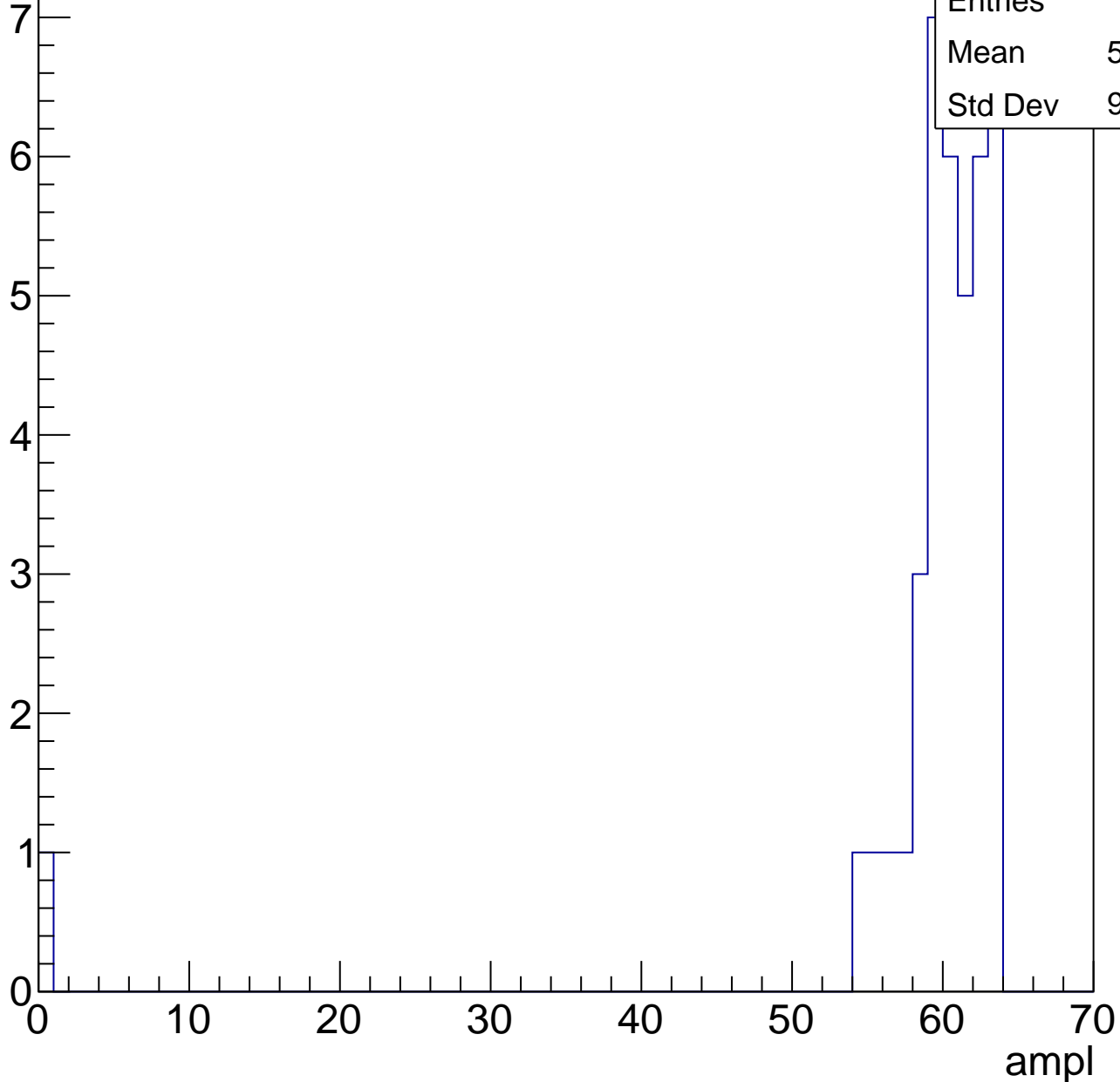
Entries	41
Mean	57.51
Std Dev	2.838



# B1L101S, U22-ch117, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U22-ch117, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	3
Mean	62.67
Std Dev	0.4714

ampl

0 10 20 30 40 50 60 70



# B1L101S, U22-ch117, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U22-ch118, adc0

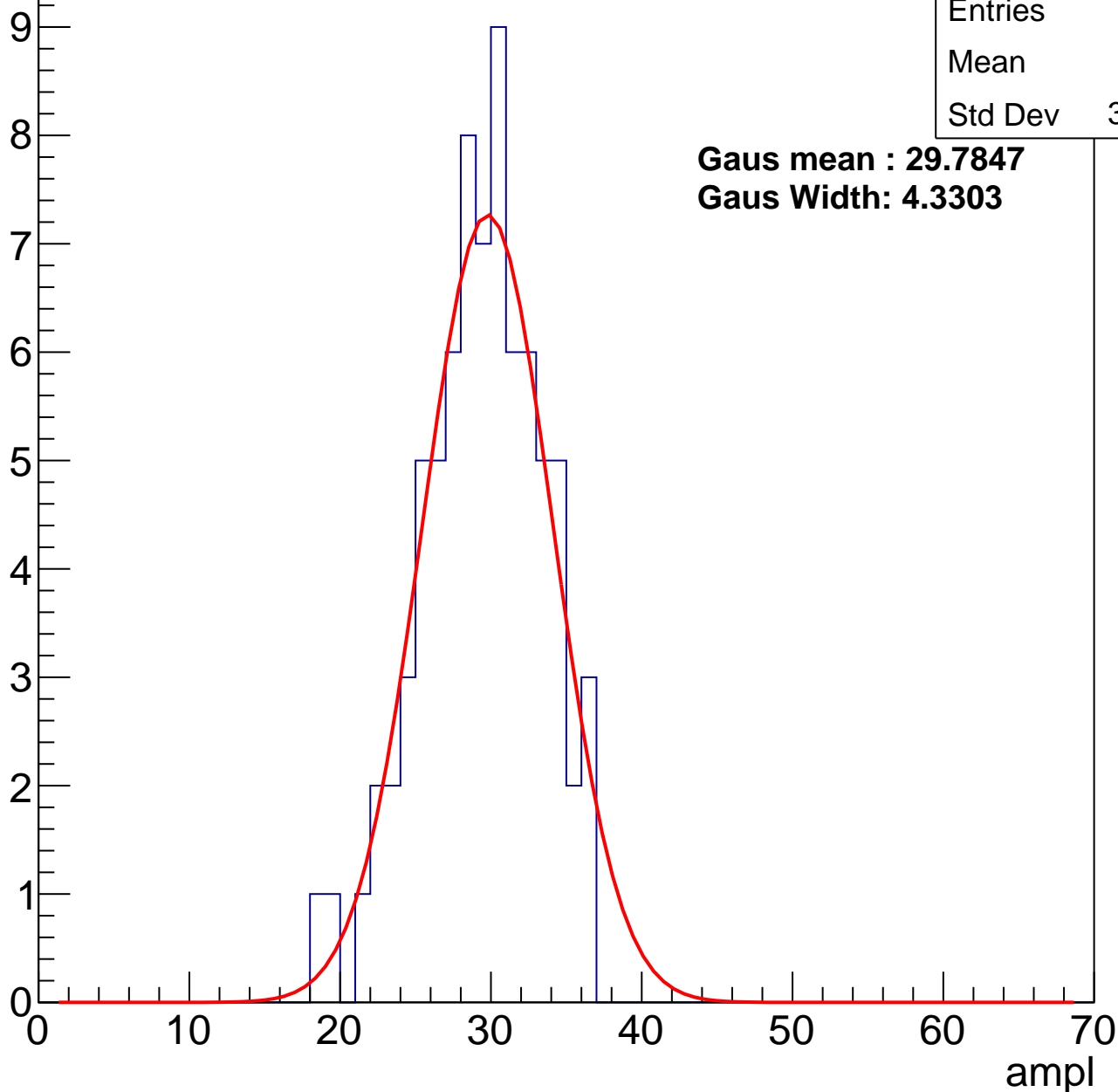
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	77
Mean	28.9
Std Dev	3.943

**Gaus mean : 29.7847**

**Gaus Width: 4.3303**



# B1L101S, U22-ch118, adc1

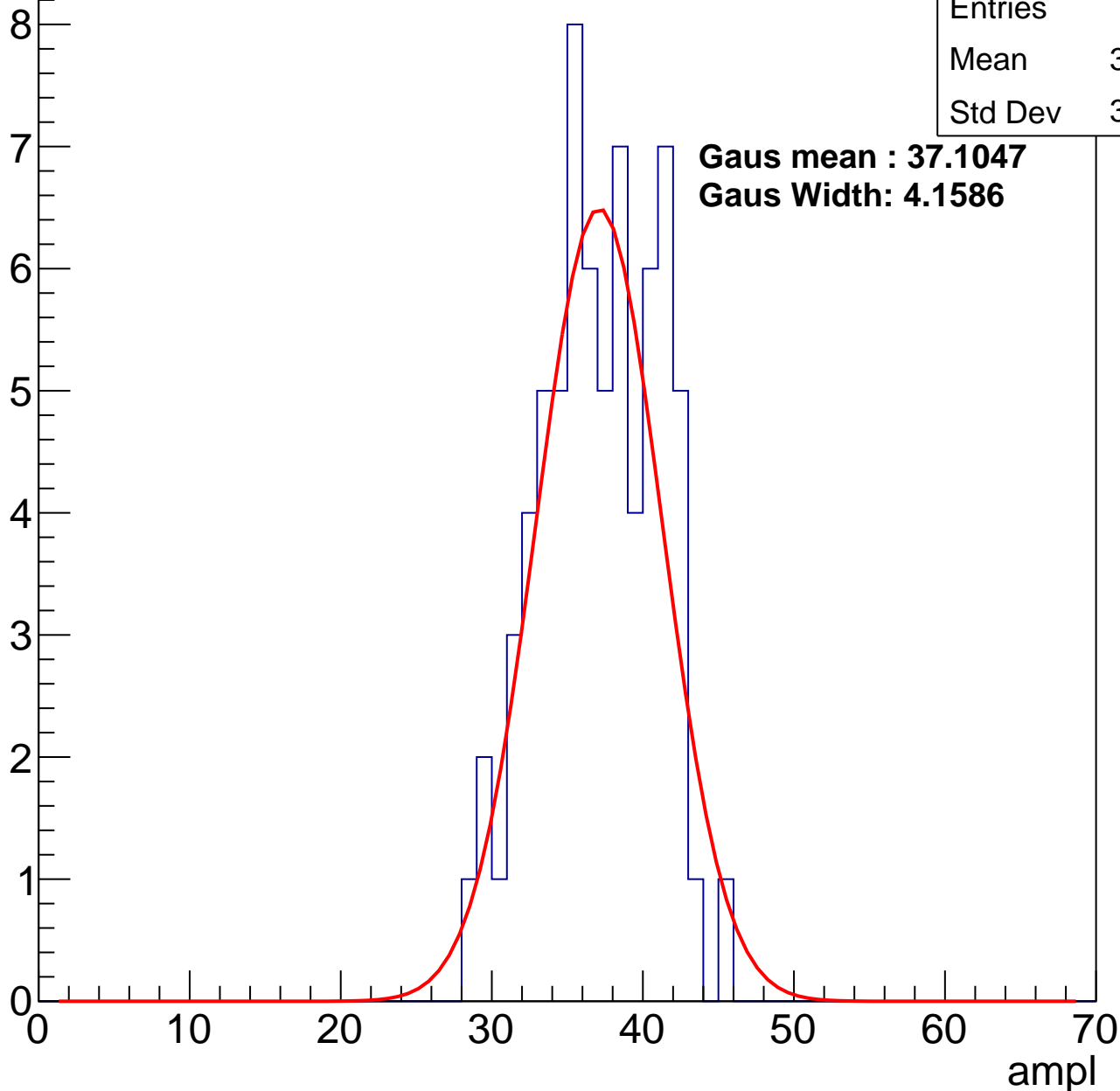
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	71
Mean	36.62
Std Dev	3.814

**Gaus mean : 37.1047**

**Gaus Width: 4.1586**



# B1L101S, U22-ch118, adc2

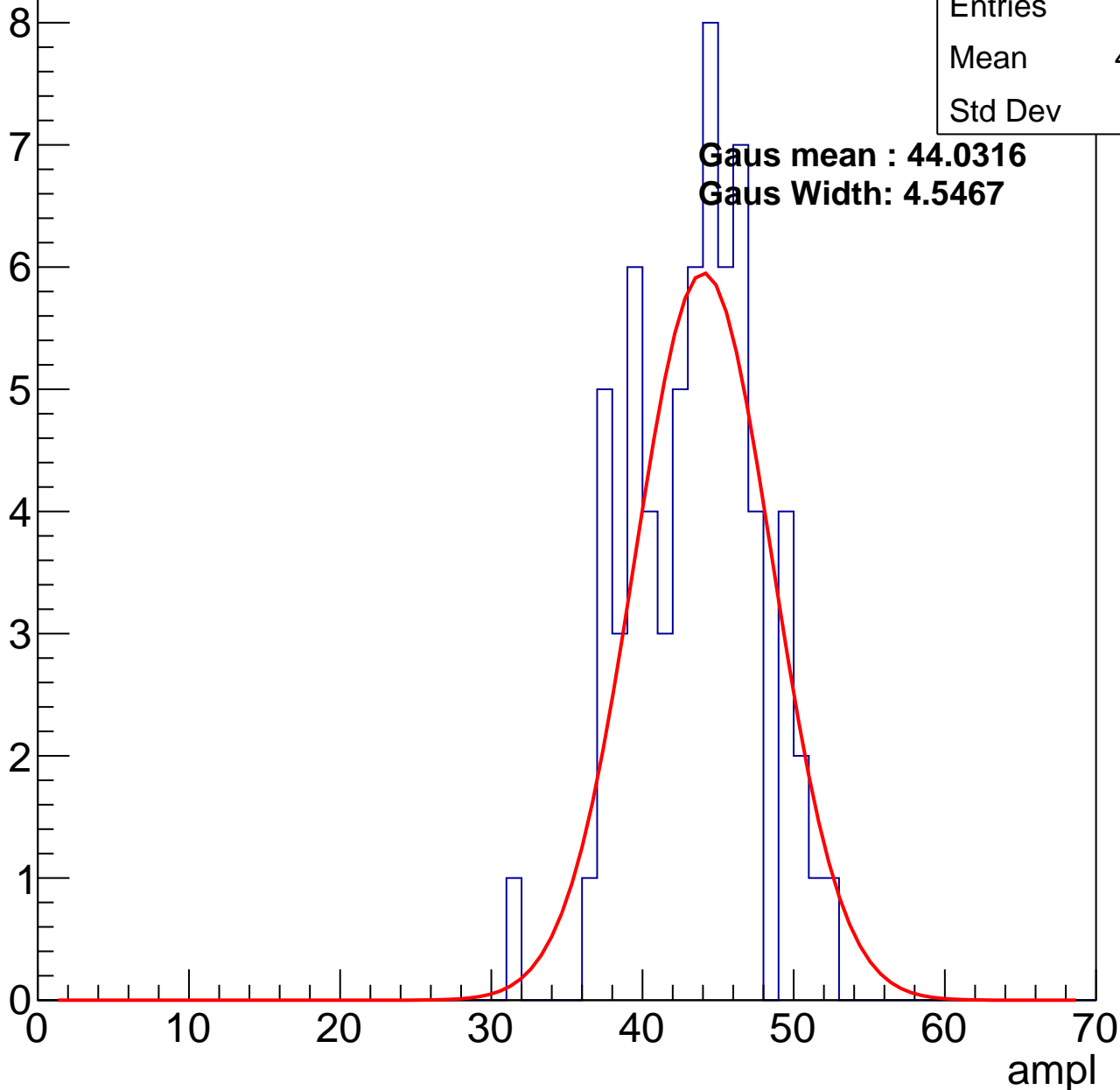
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	67
Mean	43.01
Std Dev	4.13

**Gaus mean : 44.0316**

**Gaus Width: 4.5467**

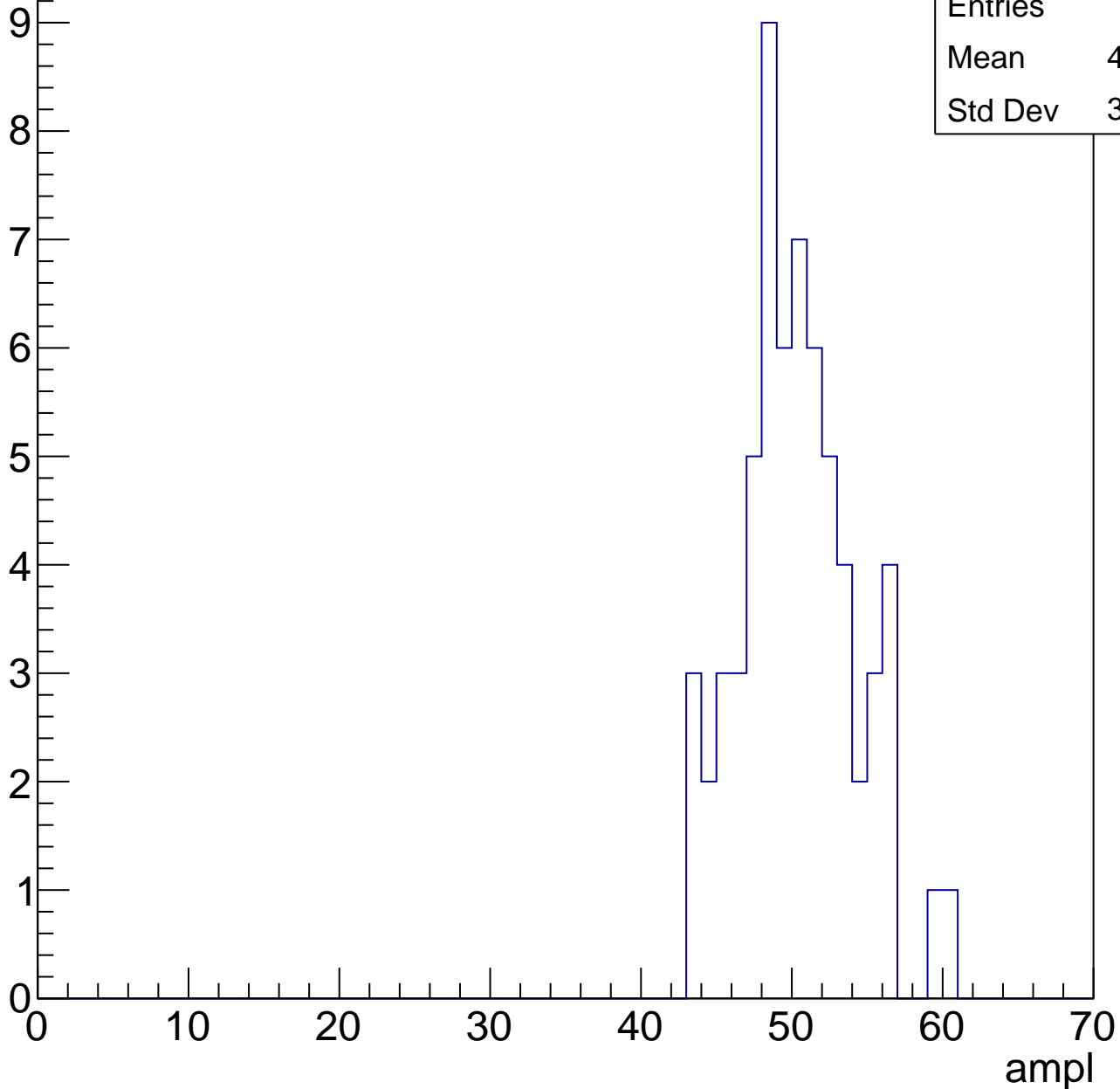


# B1L101S, U22-ch118, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	49.92
Std Dev	3.797

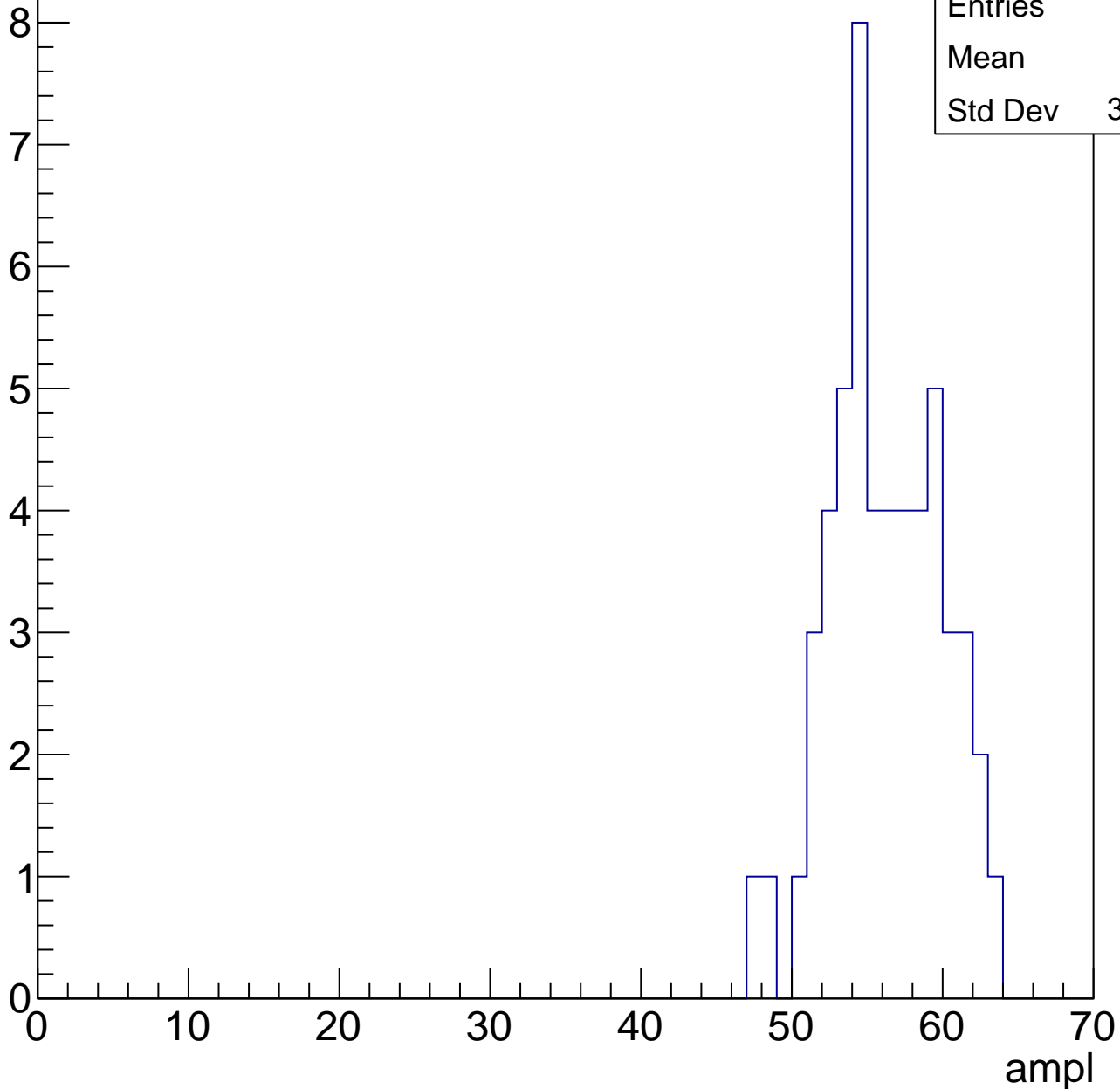


# B1L101S, U22-ch118, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	53
Mean	55.7
Std Dev	3.648

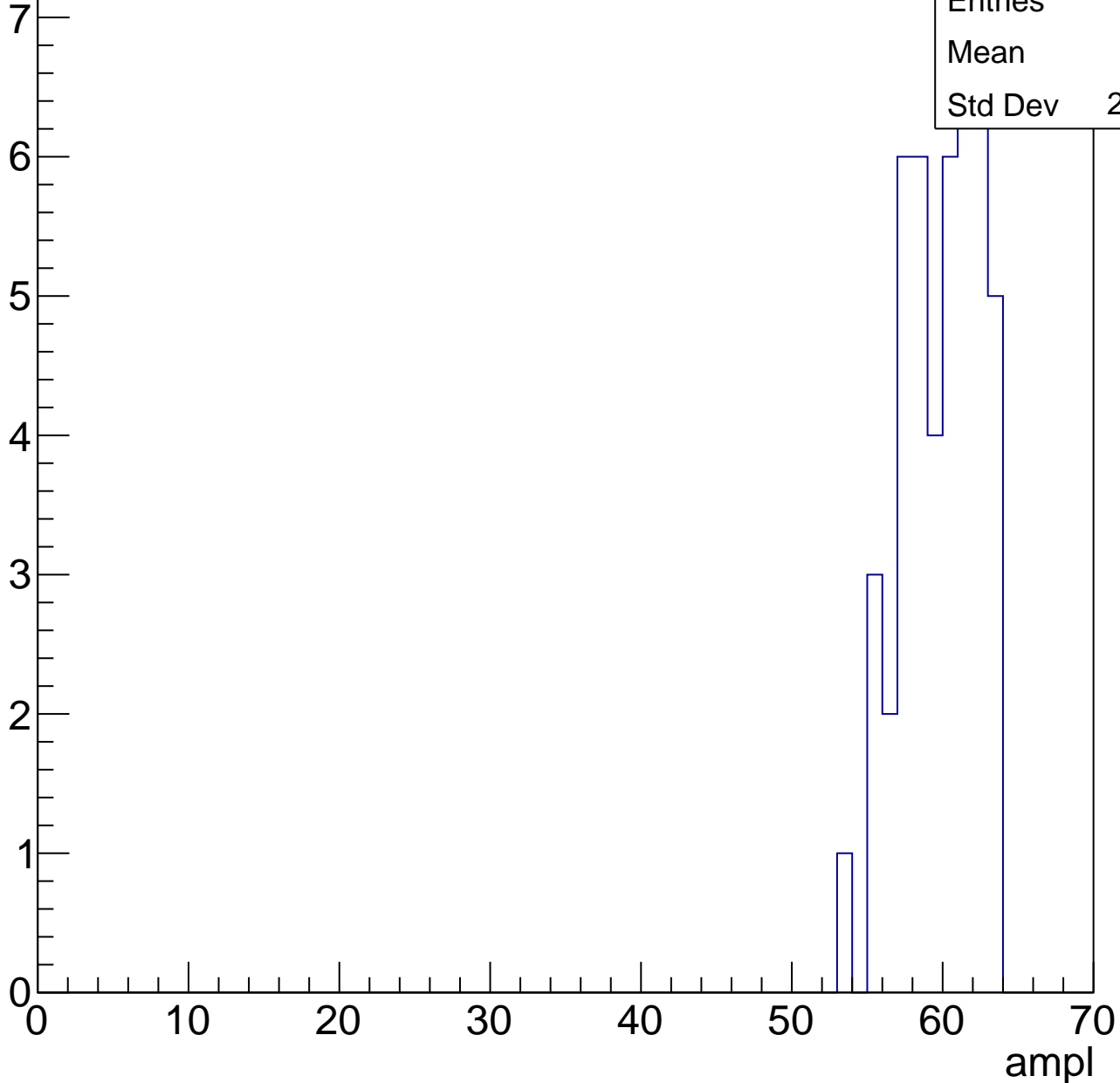


# B1L101S, U22-ch118, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

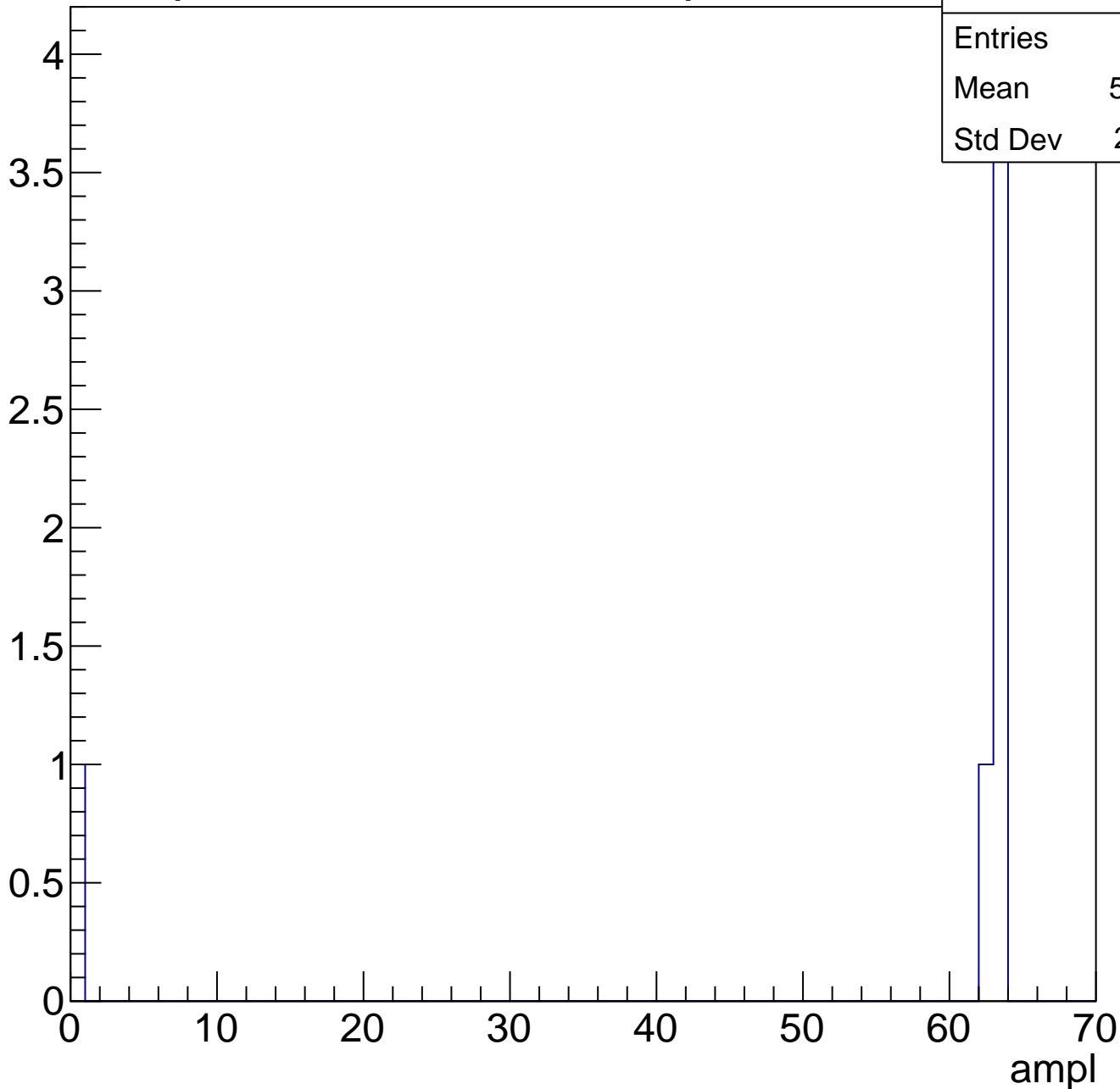
Entries	47
Mean	59.4
Std Dev	2.532



# B1L101S, U22-ch118, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U22-ch118, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U22-ch119, adc0

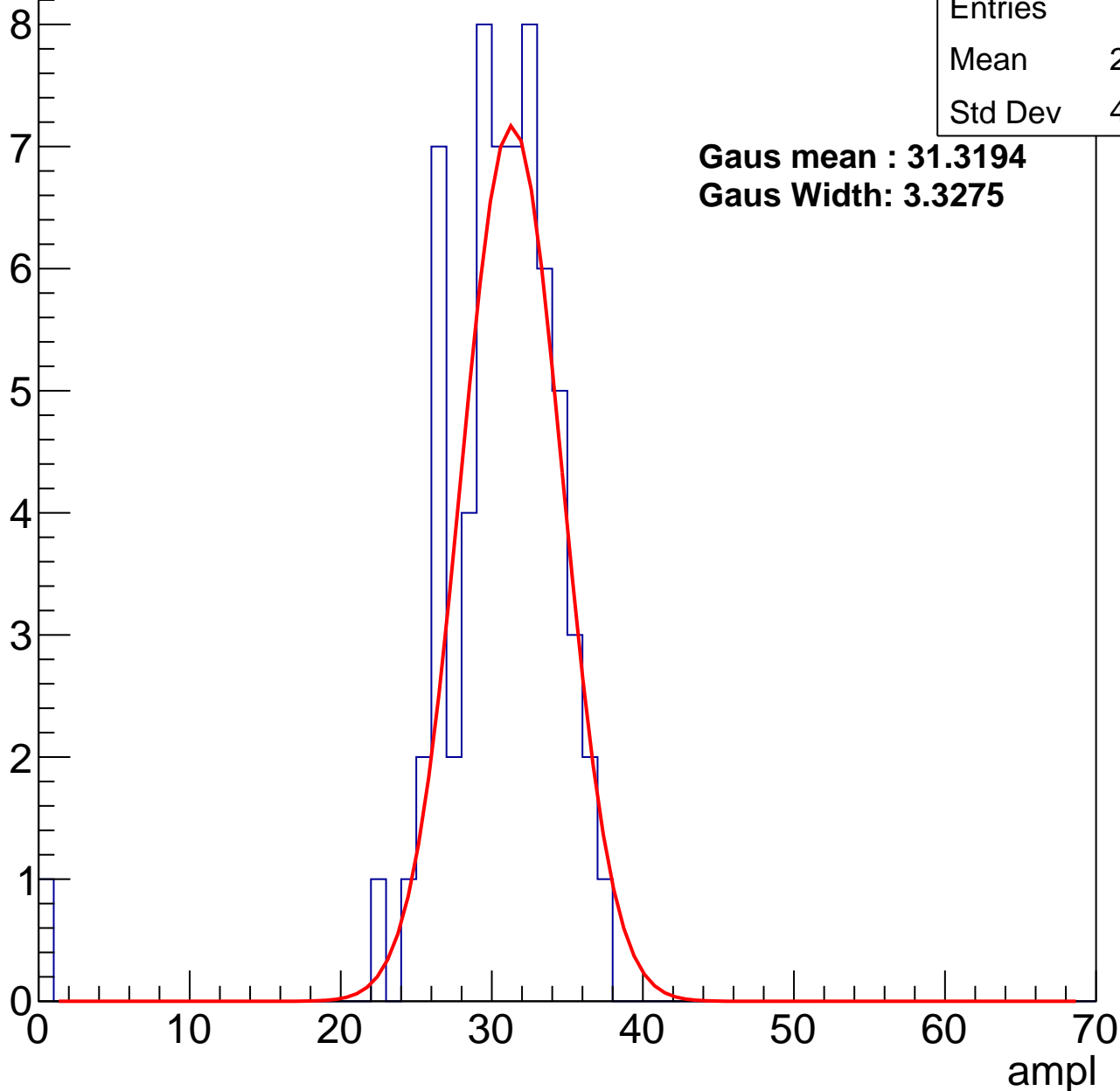
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	29.86
Std Dev	4.917

**Gaus mean : 31.3194**

**Gaus Width: 3.3275**



# B1L101S, U22-ch119, adc1

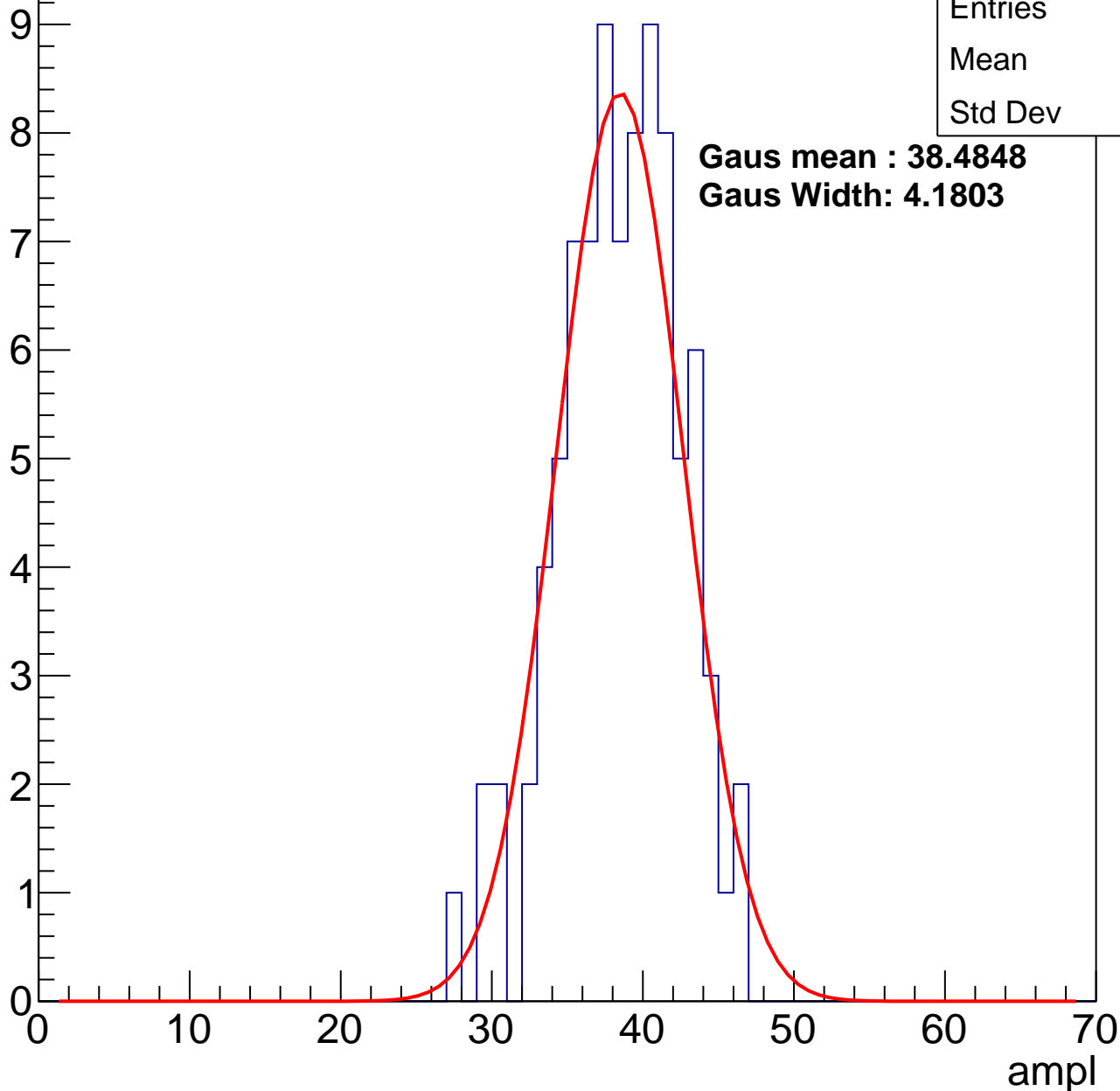
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	88
Mean	38
Std Dev	3.98

**Gaus mean : 38.4848**

**Gaus Width: 4.1803**



# B1L101S, U22-ch119, adc2

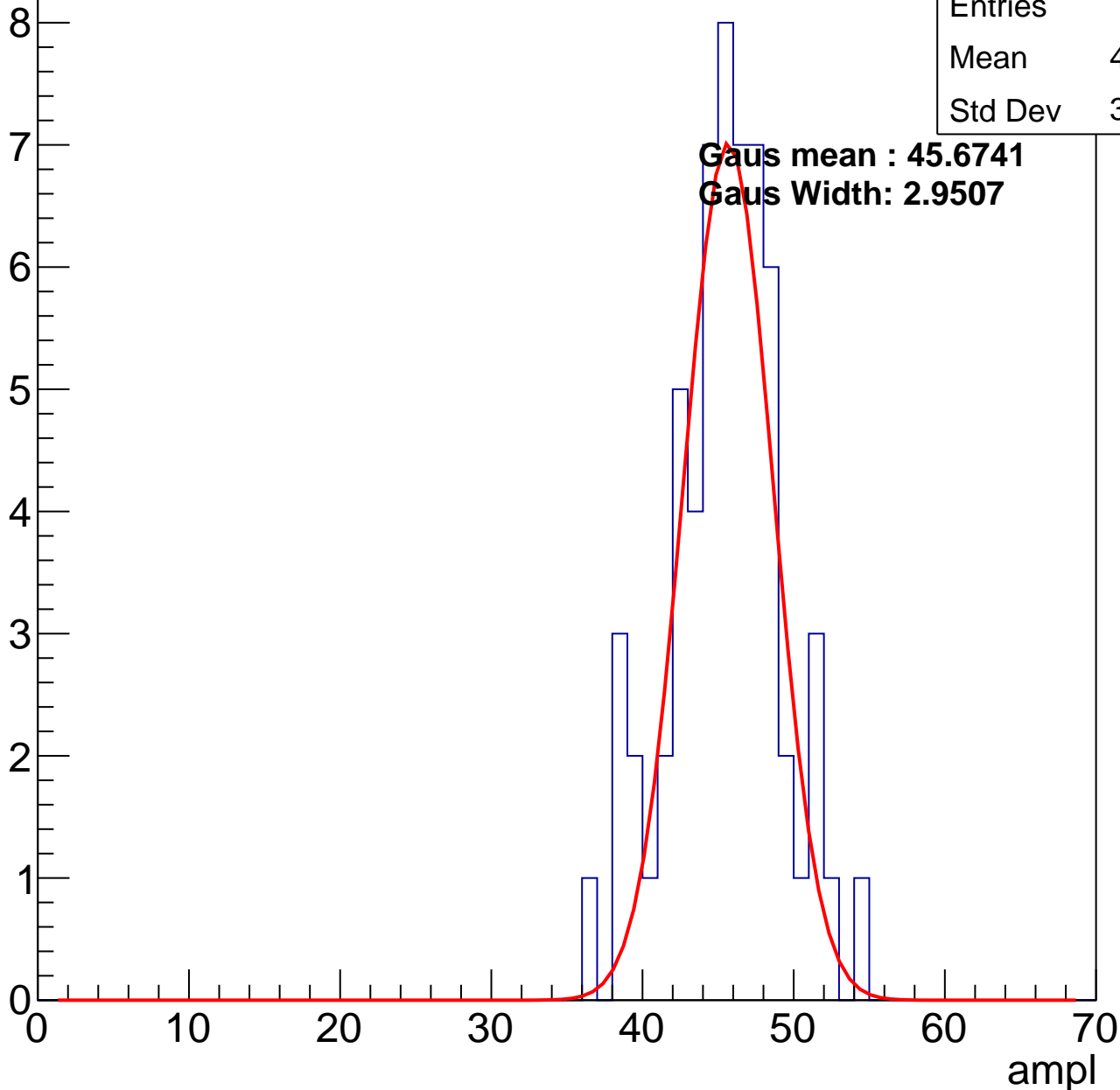
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	45.02
Std Dev	3.642

Gaus mean : 45.6741

Gaus Width: 2.9507

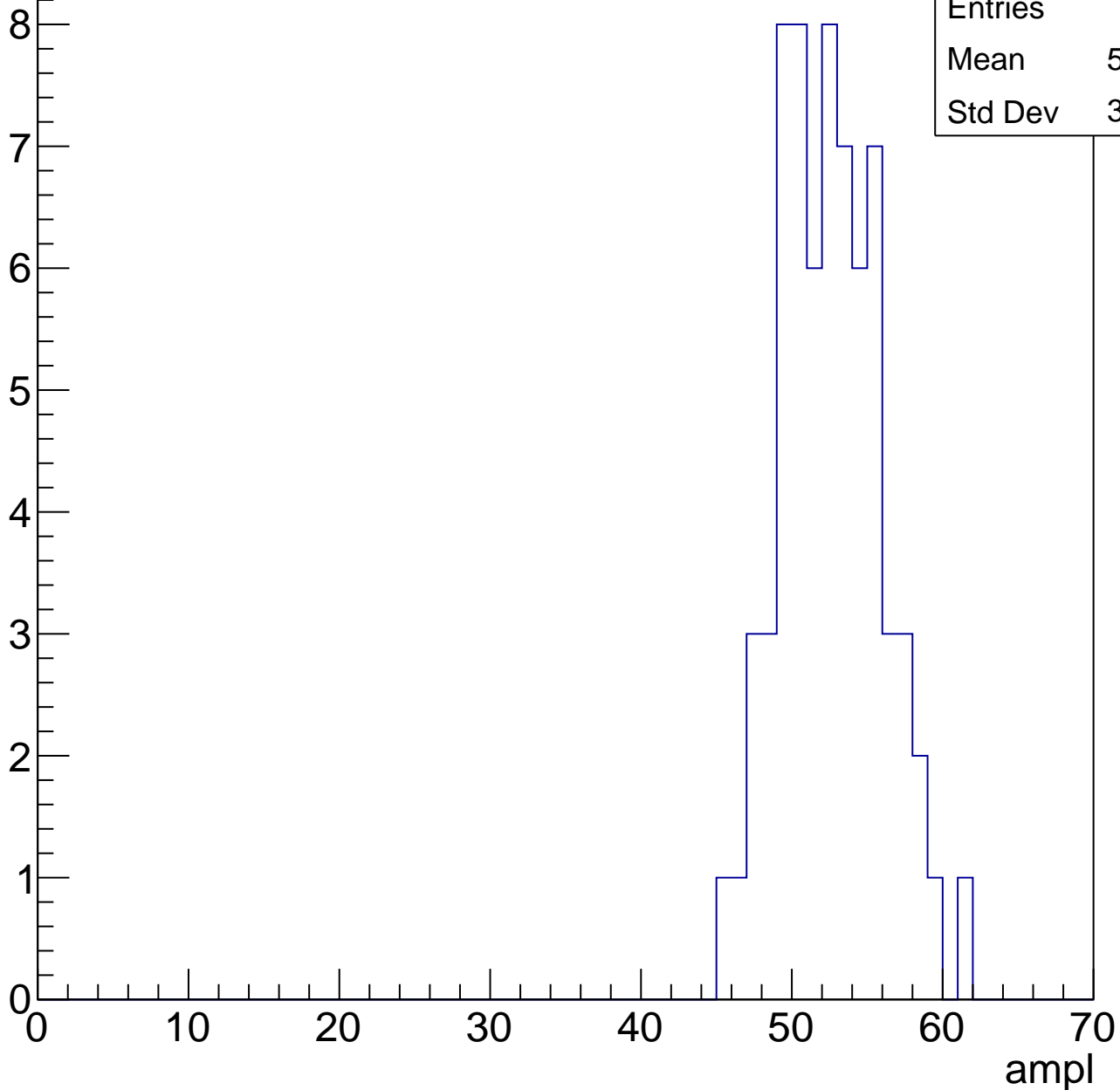


# B1L101S, U22-ch119, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	52.13
Std Dev	3.289

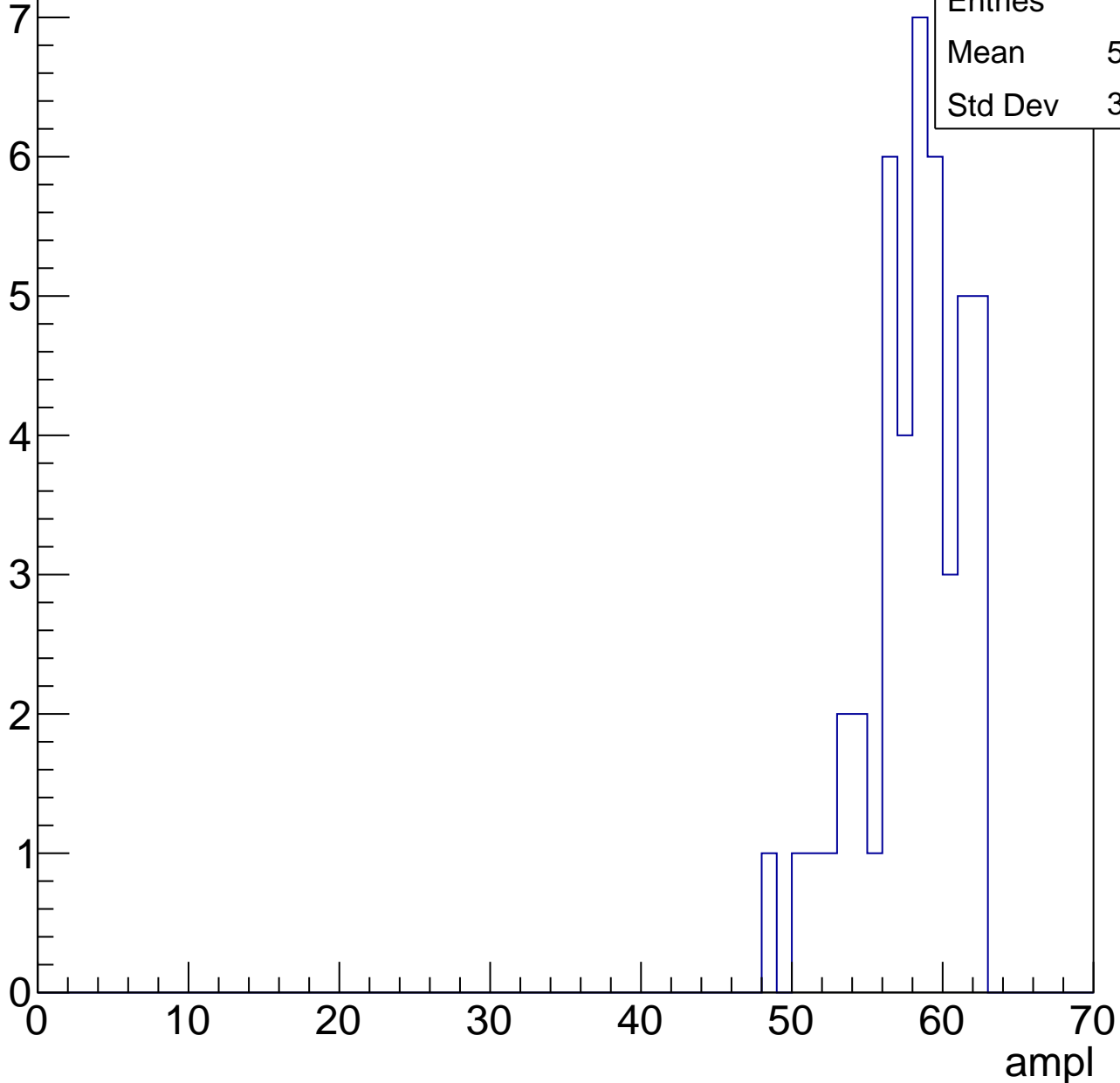


# B1L101S, U22-ch119, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	45
Mean	57.53
Std Dev	3.337

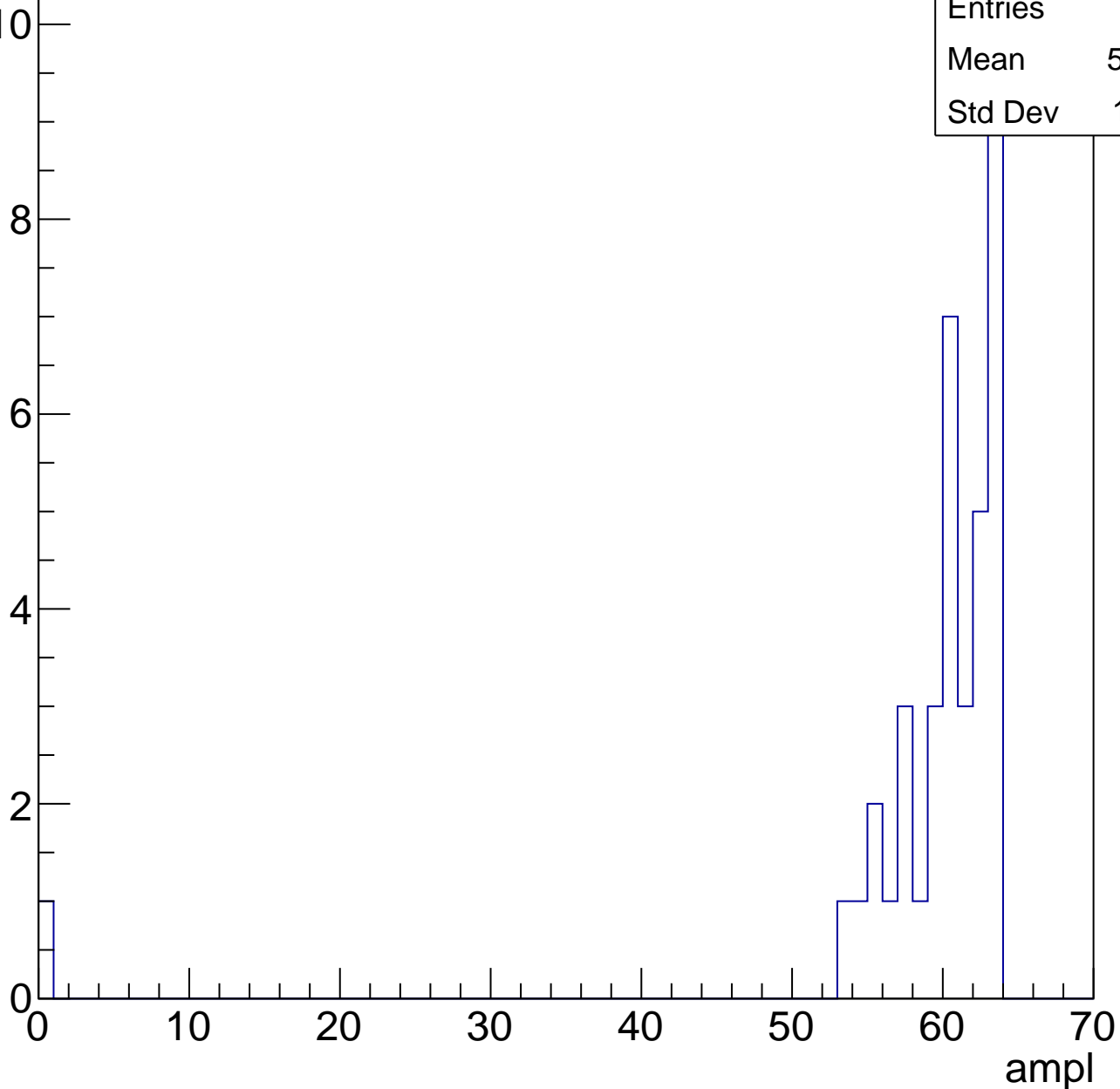


# B1L101S, U22-ch119, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	38
Mean	58.47
Std Dev	10.01



# B1L101S, U22-ch119, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

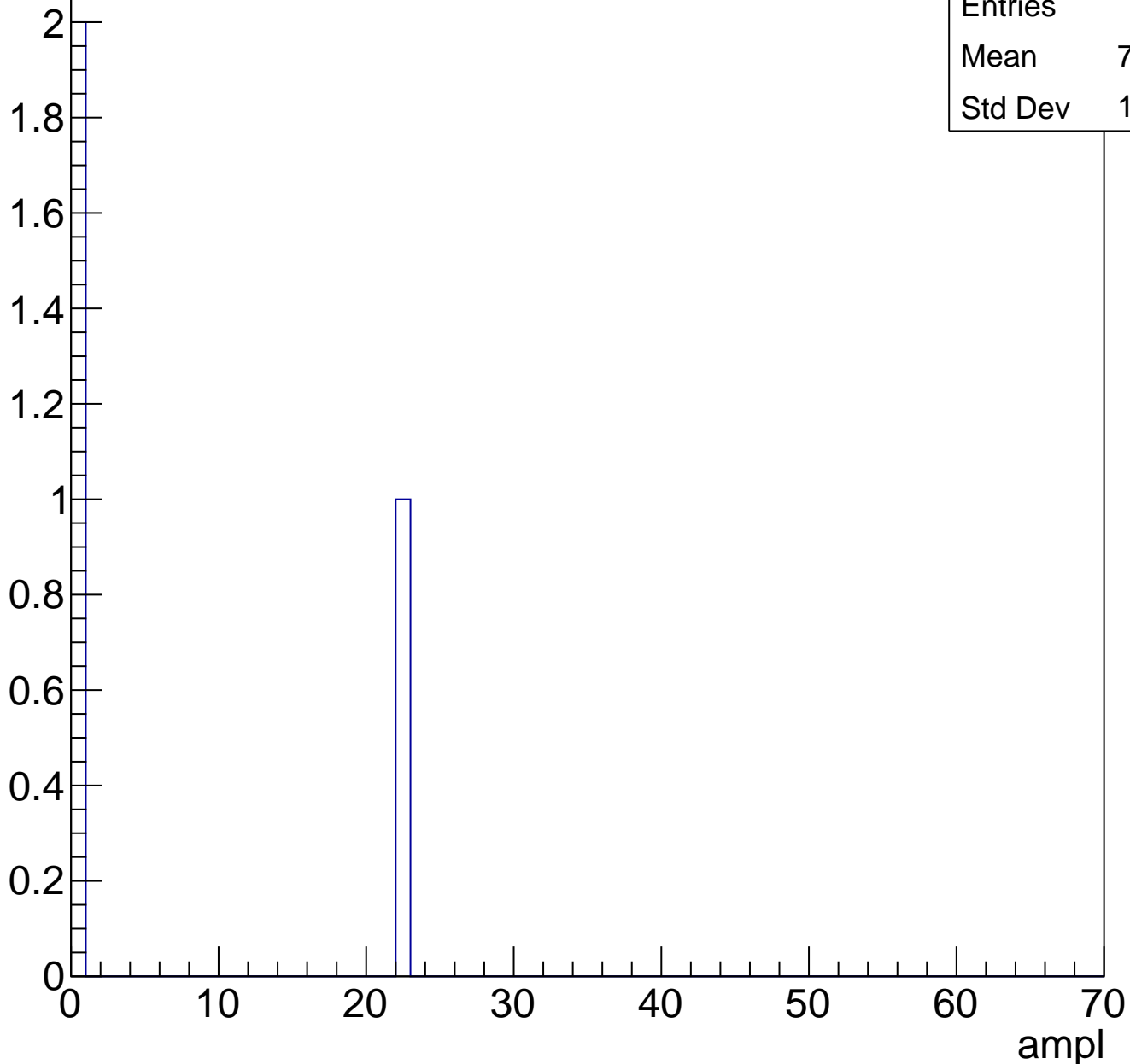




# B1L101S, U22-ch119, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	3
Mean	7.333
Std Dev	10.37

# B1L101S, U22-ch120, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	91
Mean	31.02
Std Dev	6.803

**Gaus mean : 32.7912**

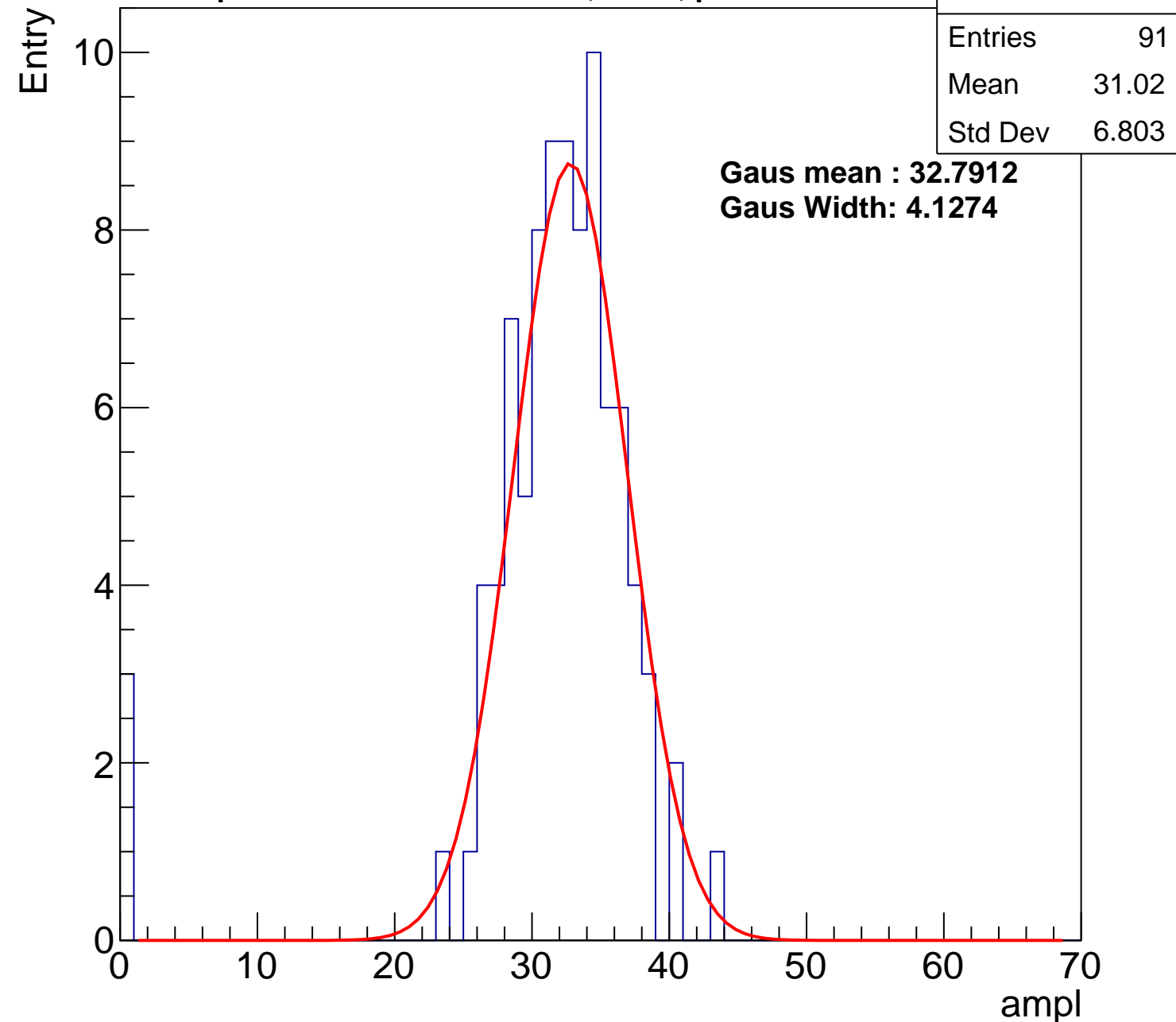
**Gaus Width: 4.1274**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U22-ch120, adc1

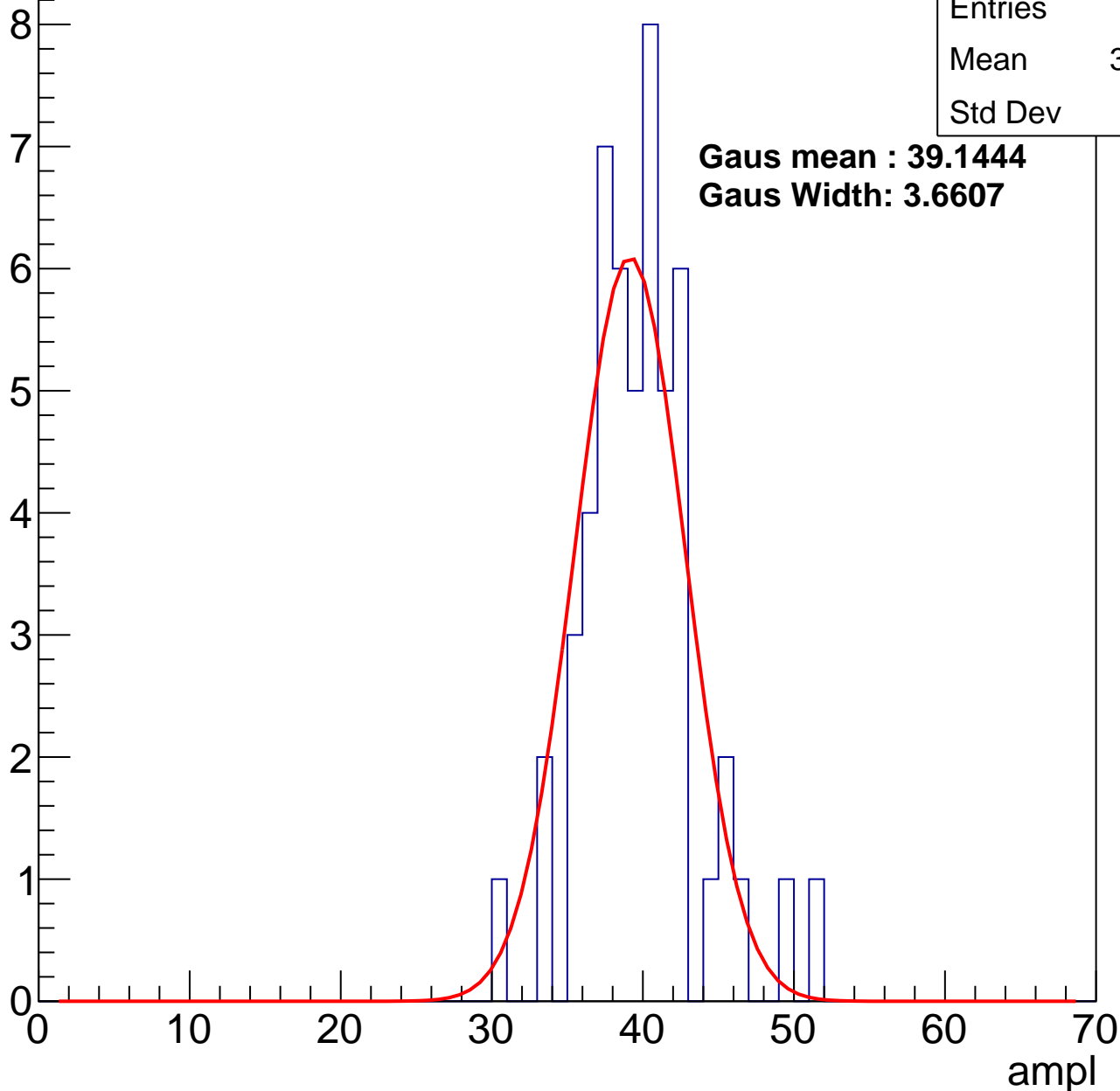
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	53
Mean	39.32
Std Dev	3.73

**Gaus mean : 39.1444**

**Gaus Width: 3.6607**



# B1L101S, U22-ch120, adc2

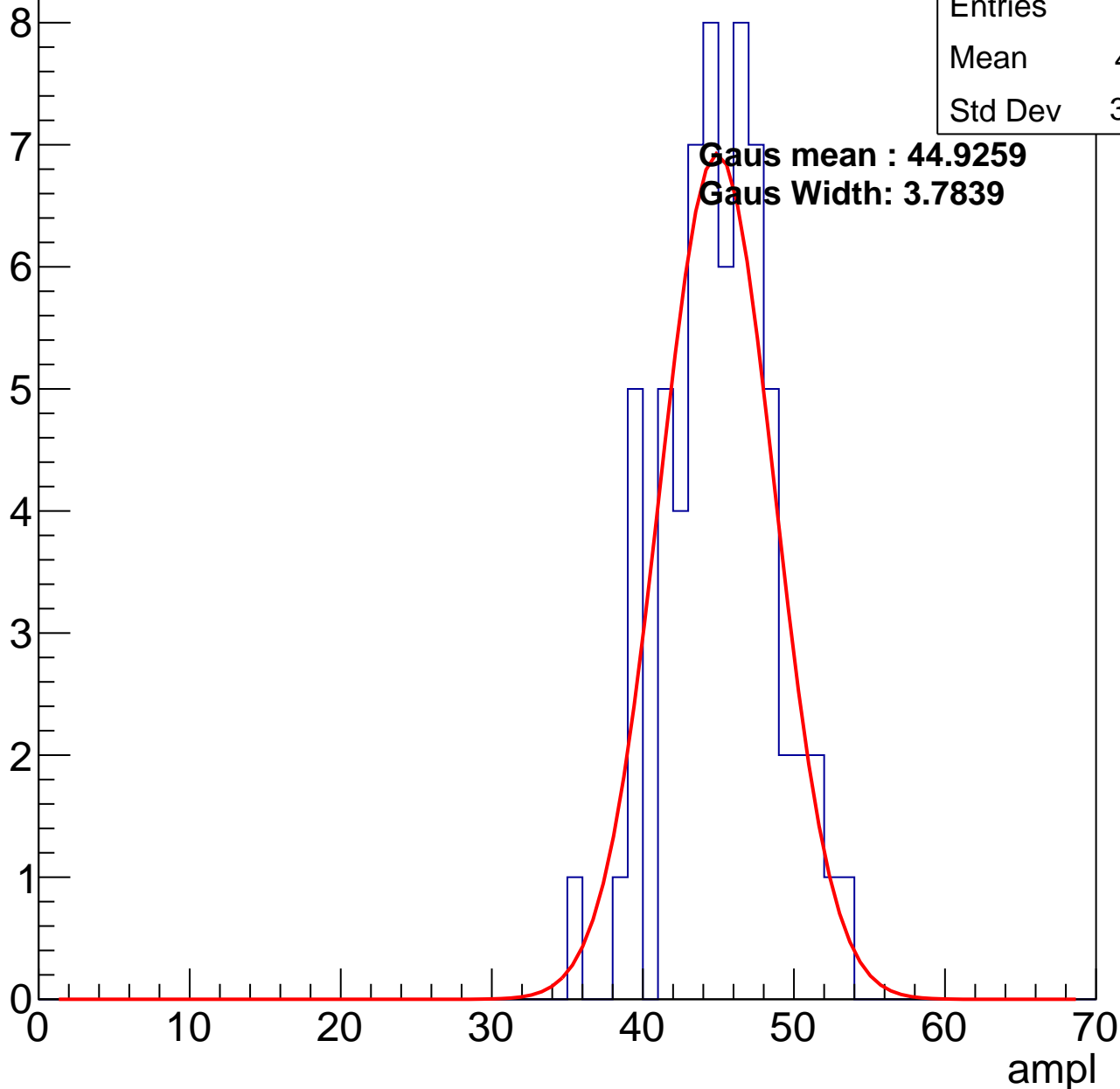
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	44.71
Std Dev	3.559

**Gaus mean : 44.9259**

**Gaus Width: 3.7839**

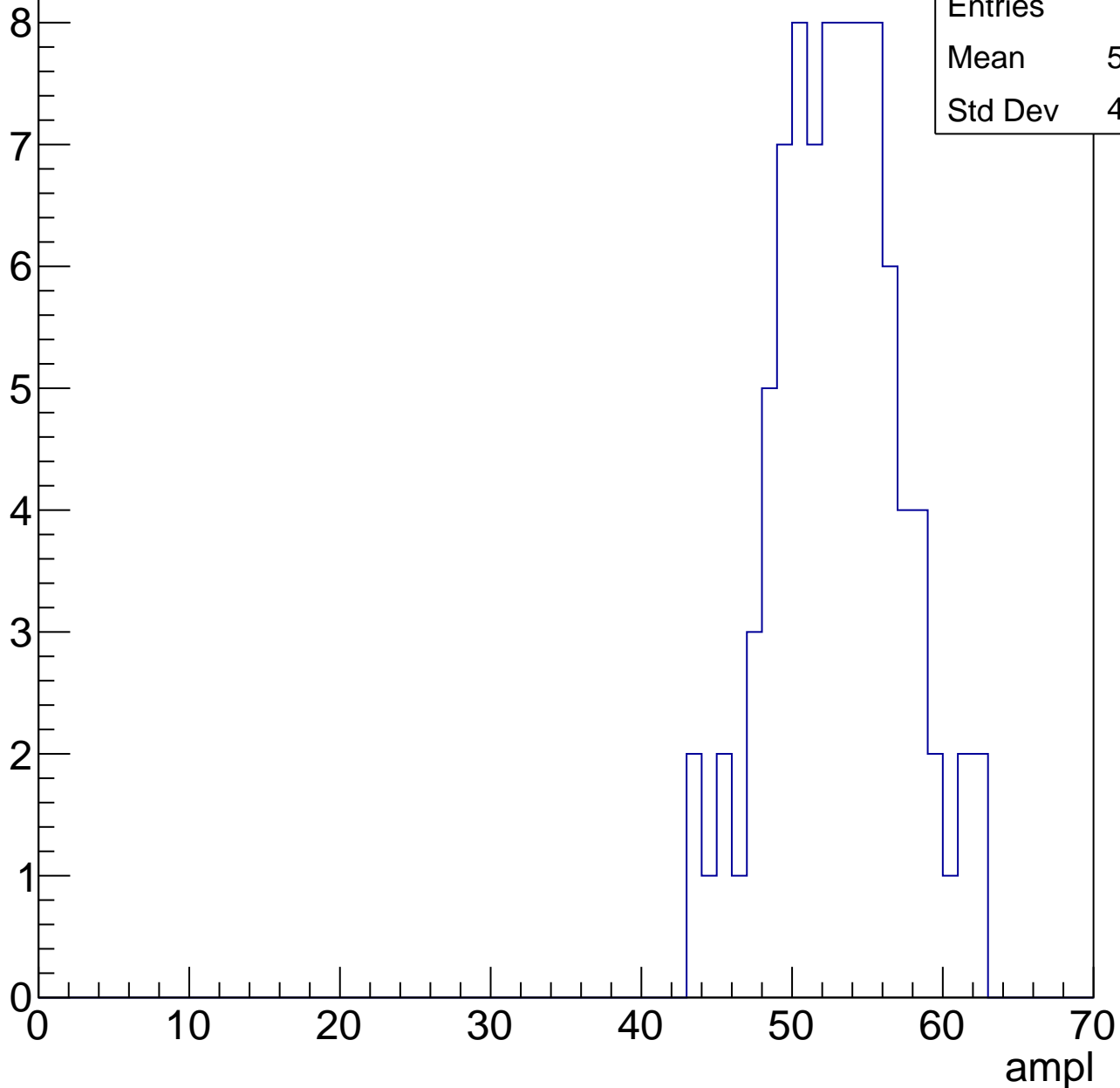


# B1L101S, U22-ch120, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

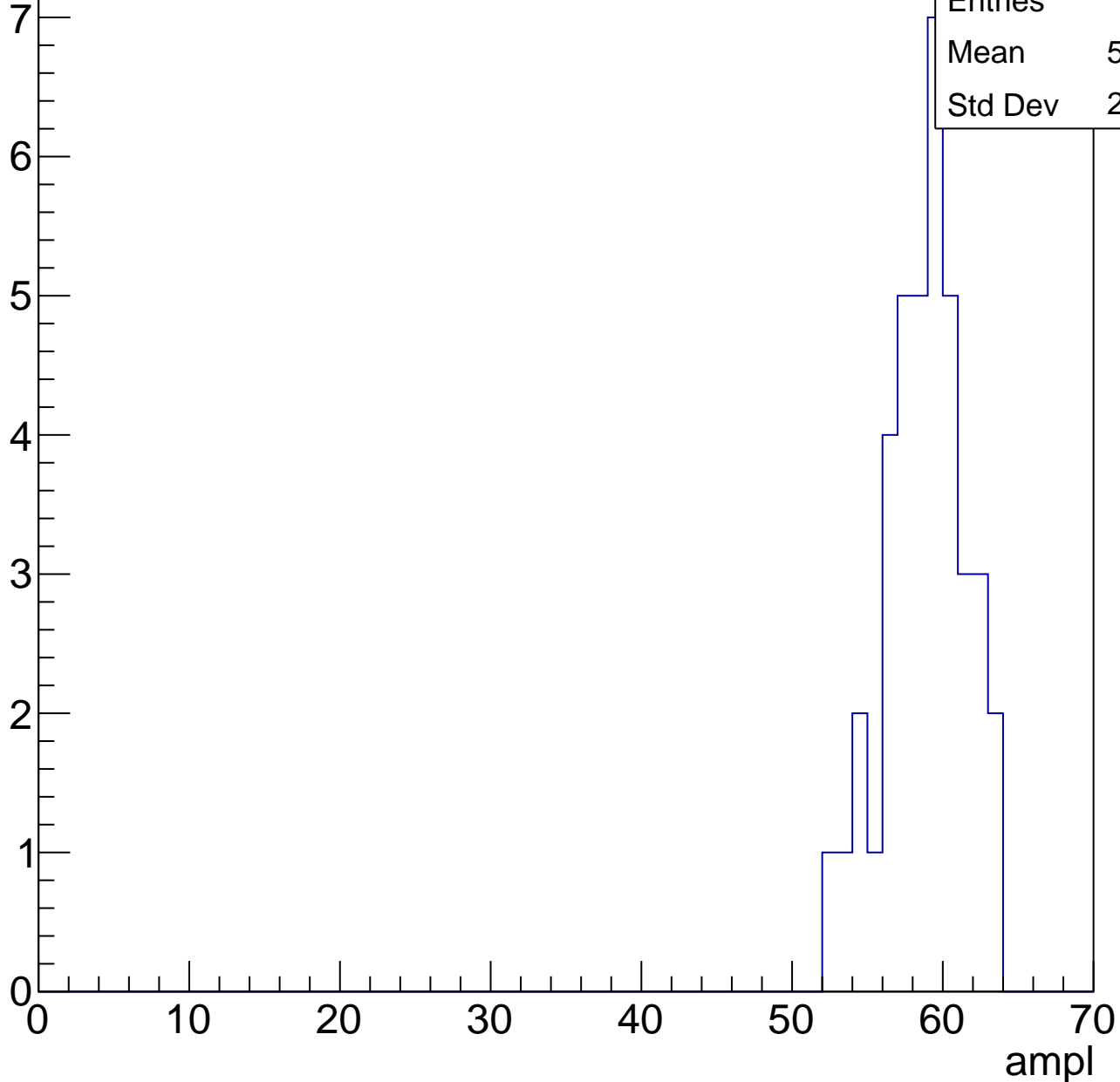
Entries	89
Mean	52.57
Std Dev	4.192



# B1L101S, U22-ch120, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

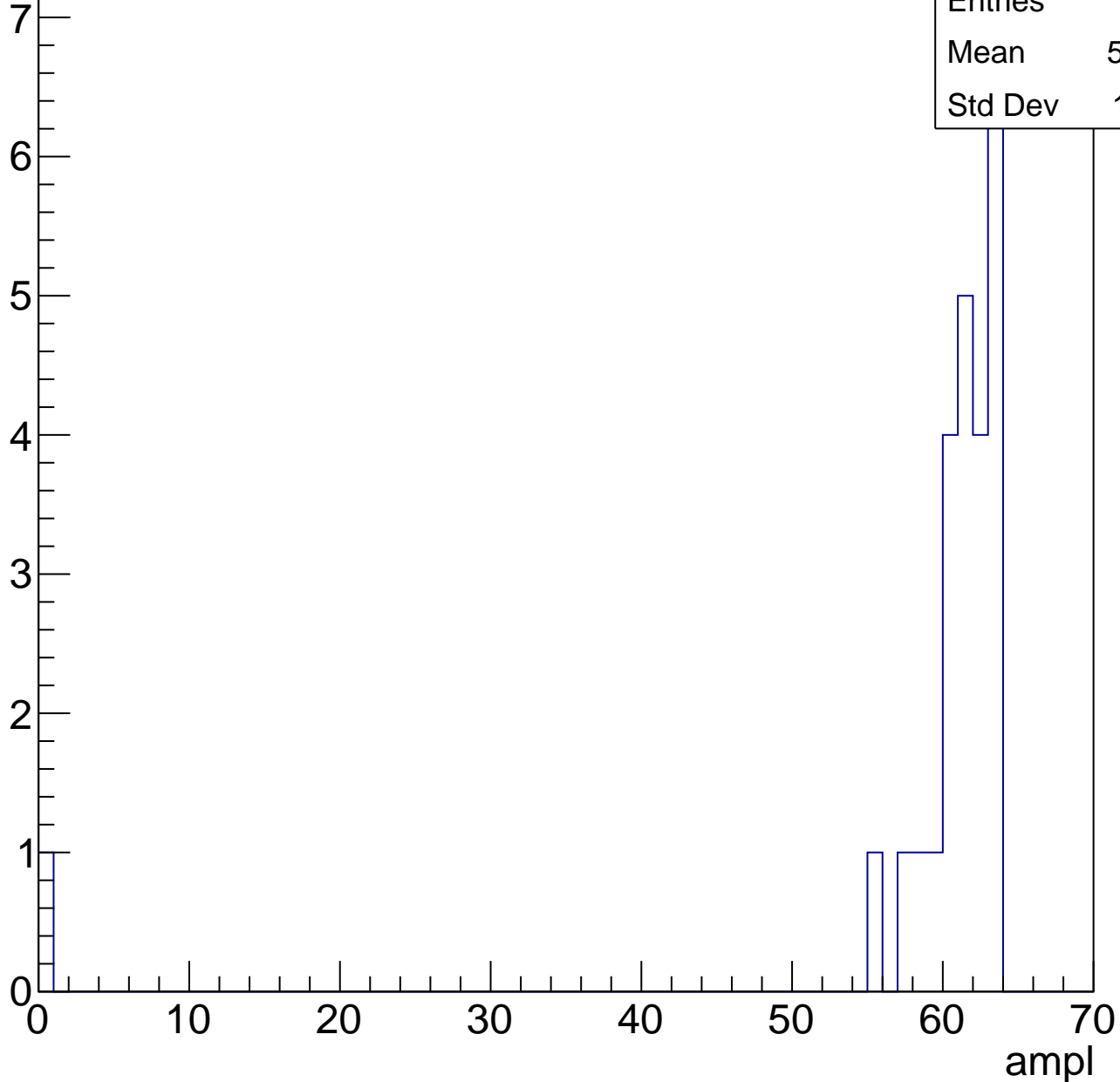


# B1L101S, U22-ch120, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	25
Mean	58.52
Std Dev	12.11



# B1L101S, U22-ch120, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U22-ch120, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U22-ch121, adc0

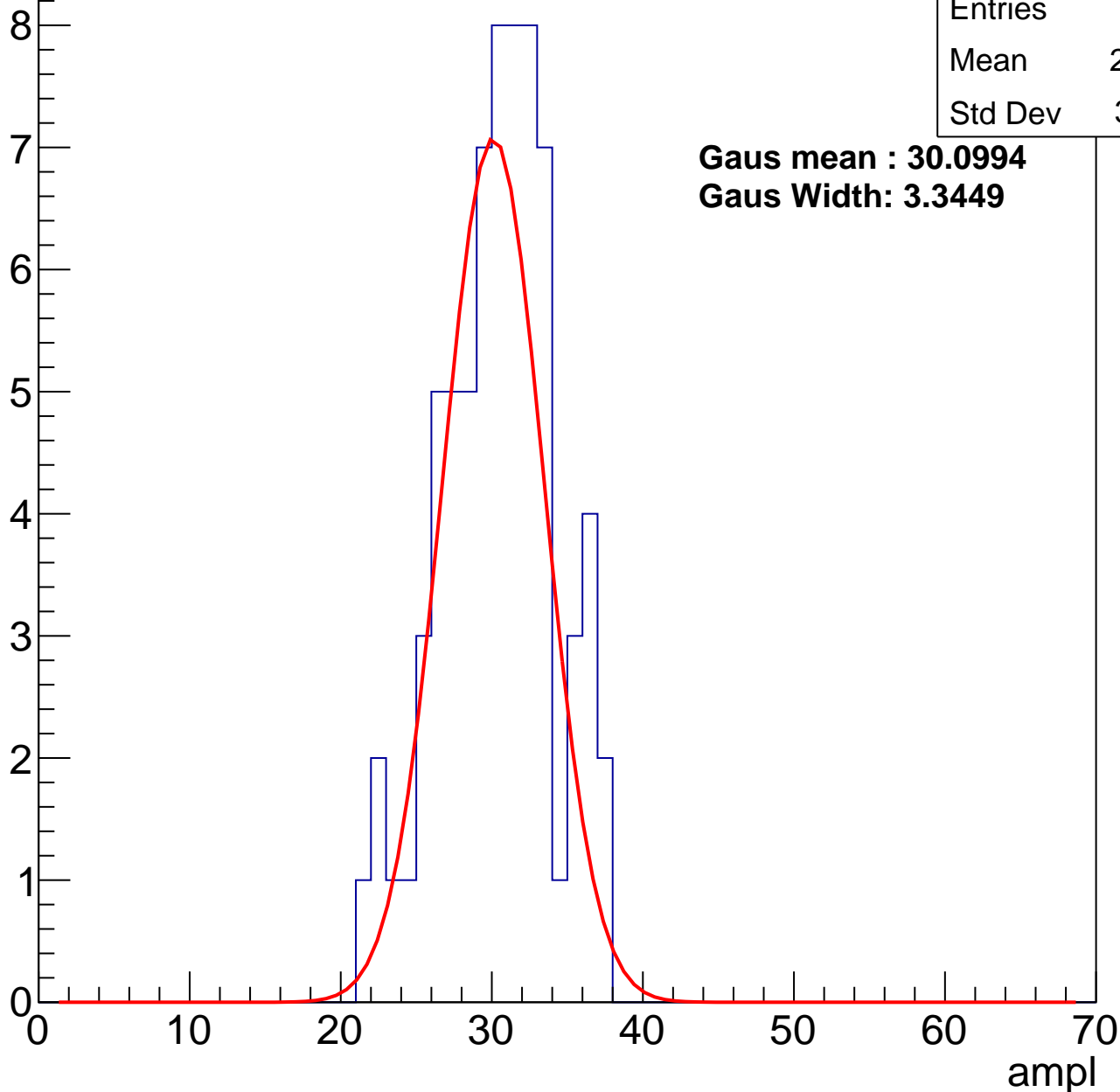
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	71
Mean	29.96
Std Dev	3.671

**Gaus mean : 30.0994**

**Gaus Width: 3.3449**



# B1L101S, U22-ch121, adc1

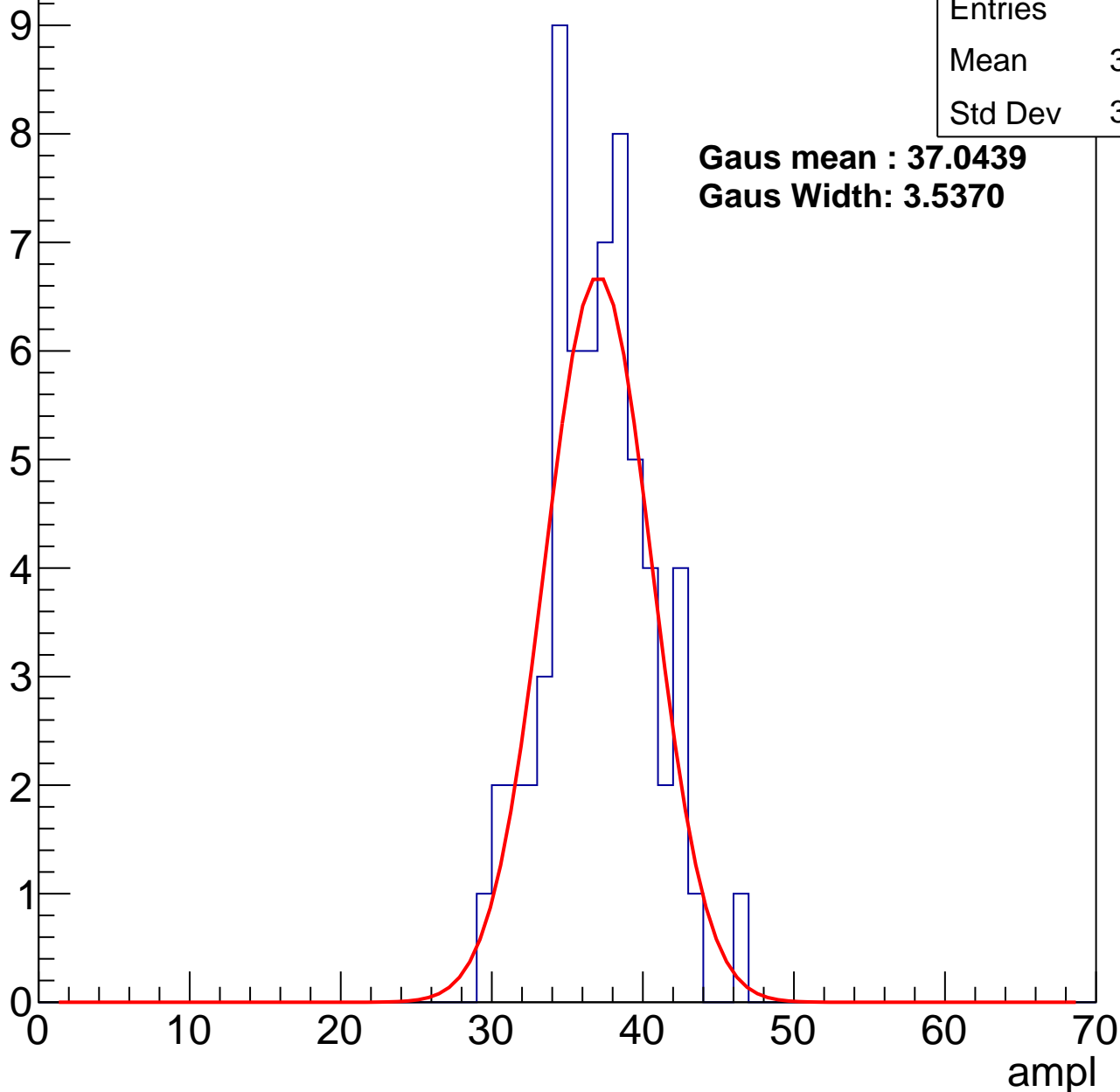
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	36.56
Std Dev	3.435

**Gaus mean : 37.0439**

**Gaus Width: 3.5370**



# B1L101S, U22-ch121, adc2

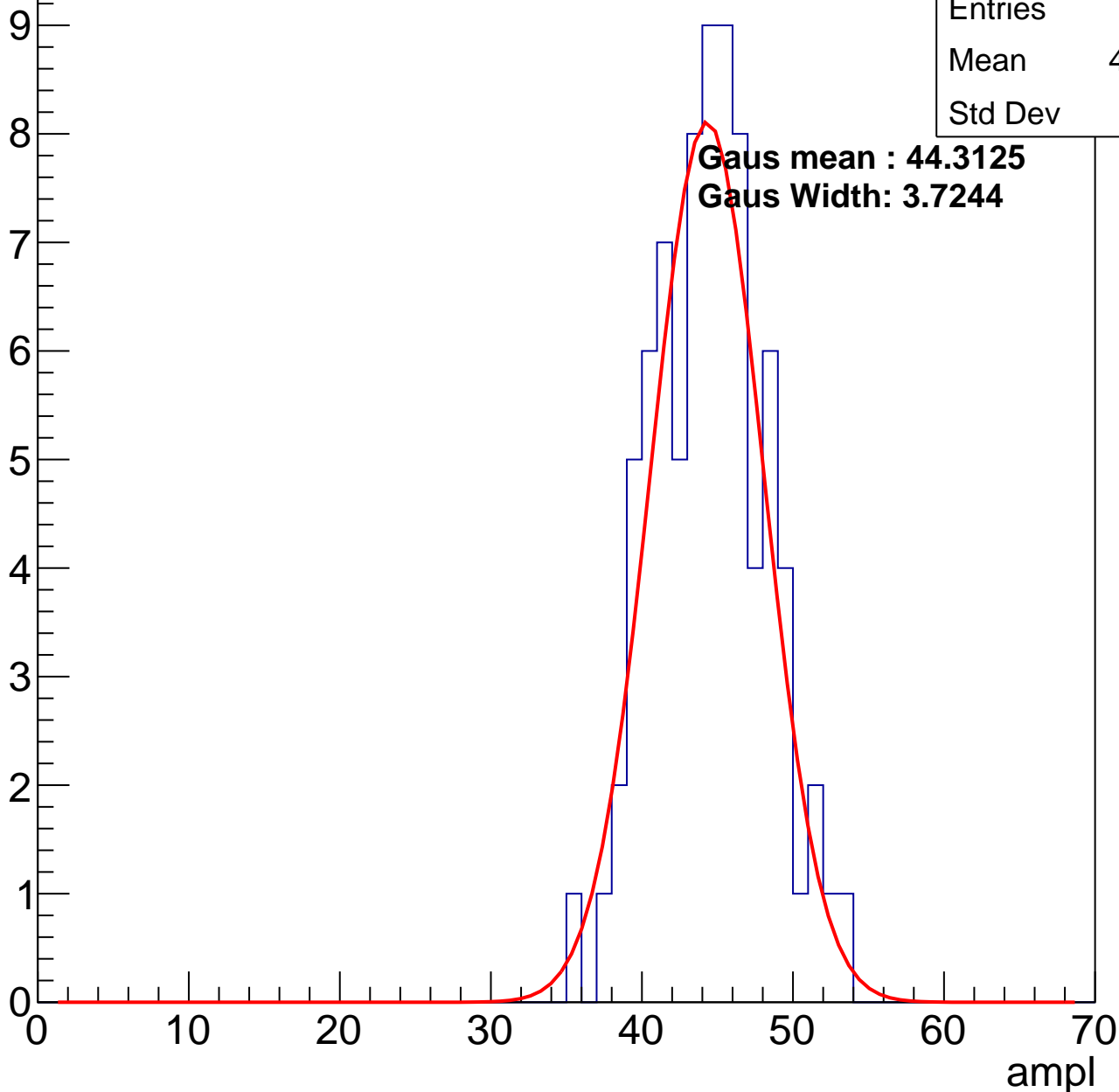
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	80
Mean	44.02
Std Dev	3.65

**Gaus mean : 44.3125**

**Gaus Width: 3.7244**

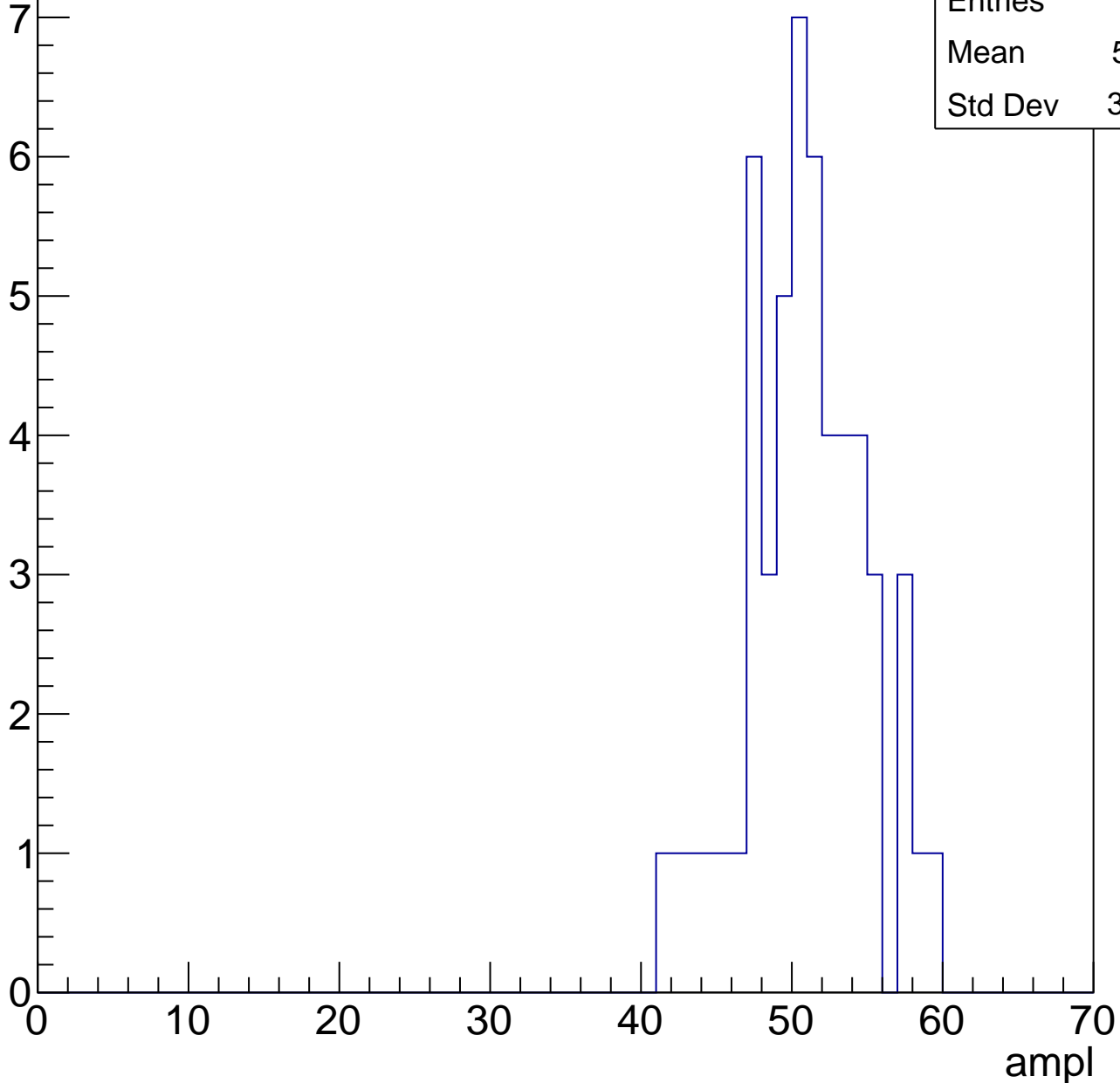


# B1L101S, U22-ch121, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	53
Mean	50.51
Std Dev	3.927

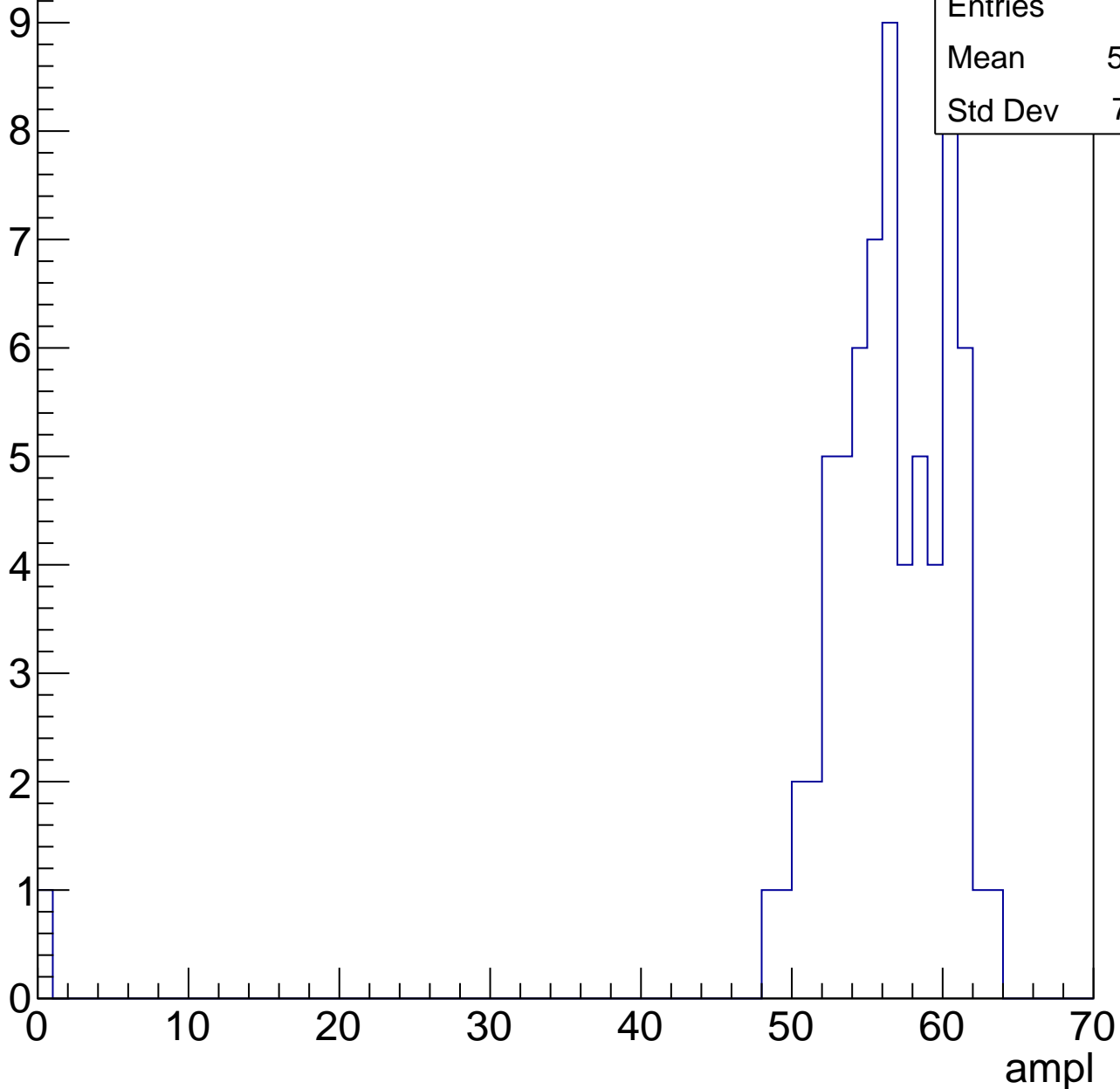


# B1L101S, U22-ch121, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	55.32
Std Dev	7.591

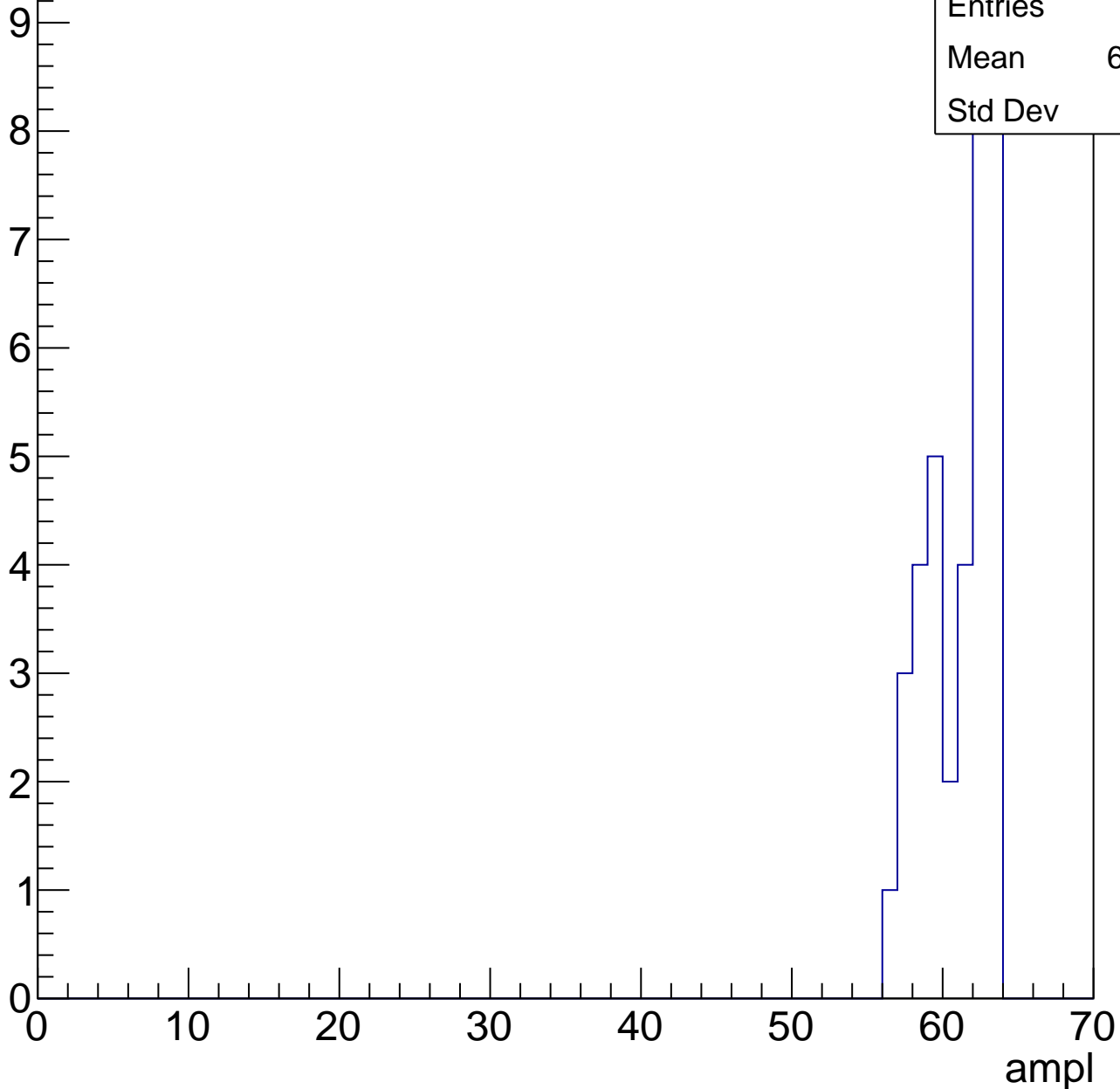


# B1L101S, U22-ch121, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	36
Mean	60.56
Std Dev	2.14



# B1L101S, U22-ch121, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	63
Std Dev	0



# B1L101S, U22-ch121, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L101S, U22-ch122, adc0

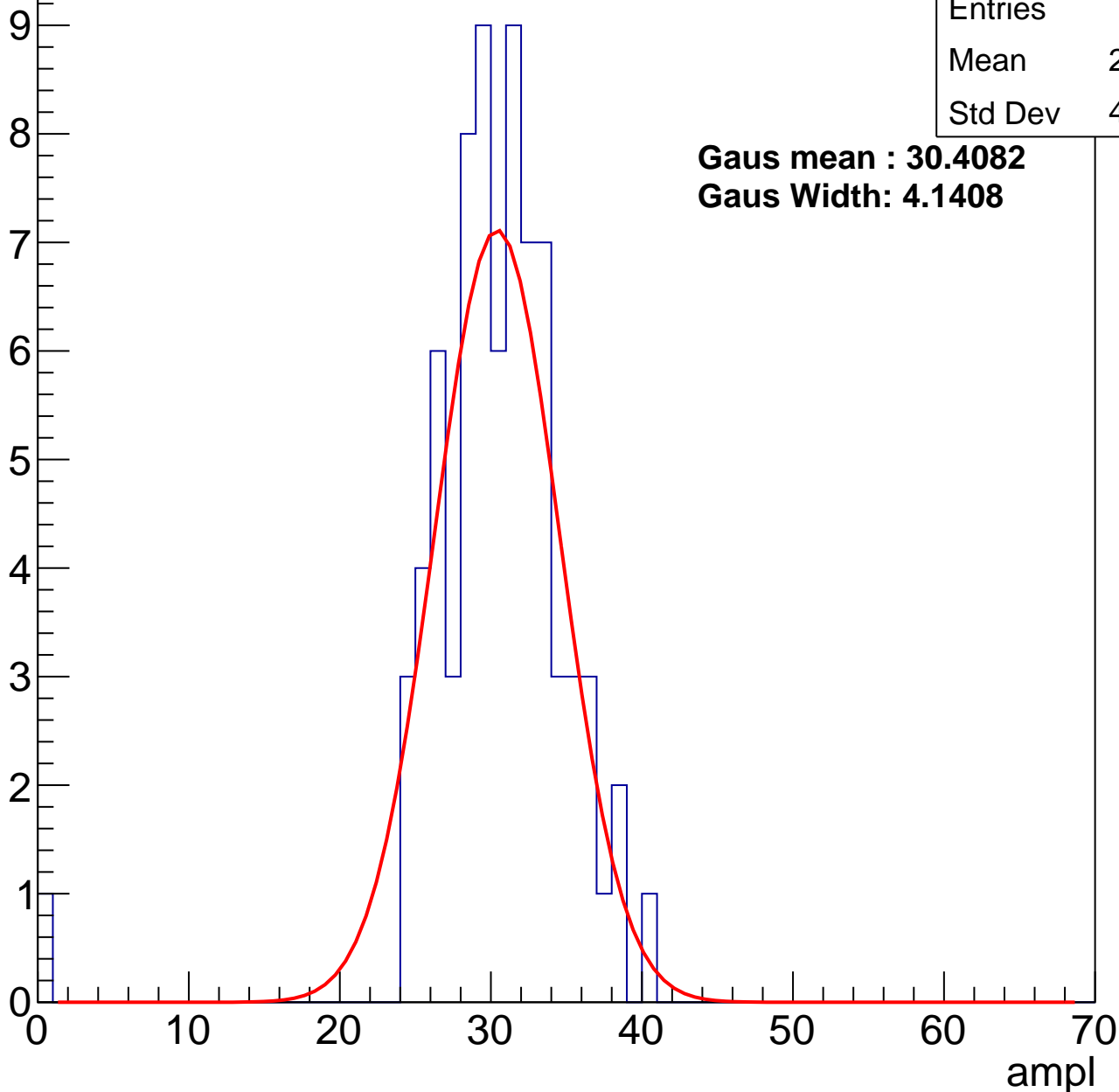
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	76
Mean	29.95
Std Dev	4.973

**Gaus mean : 30.4082**

**Gaus Width: 4.1408**



# B1L101S, U22-ch122, adc1

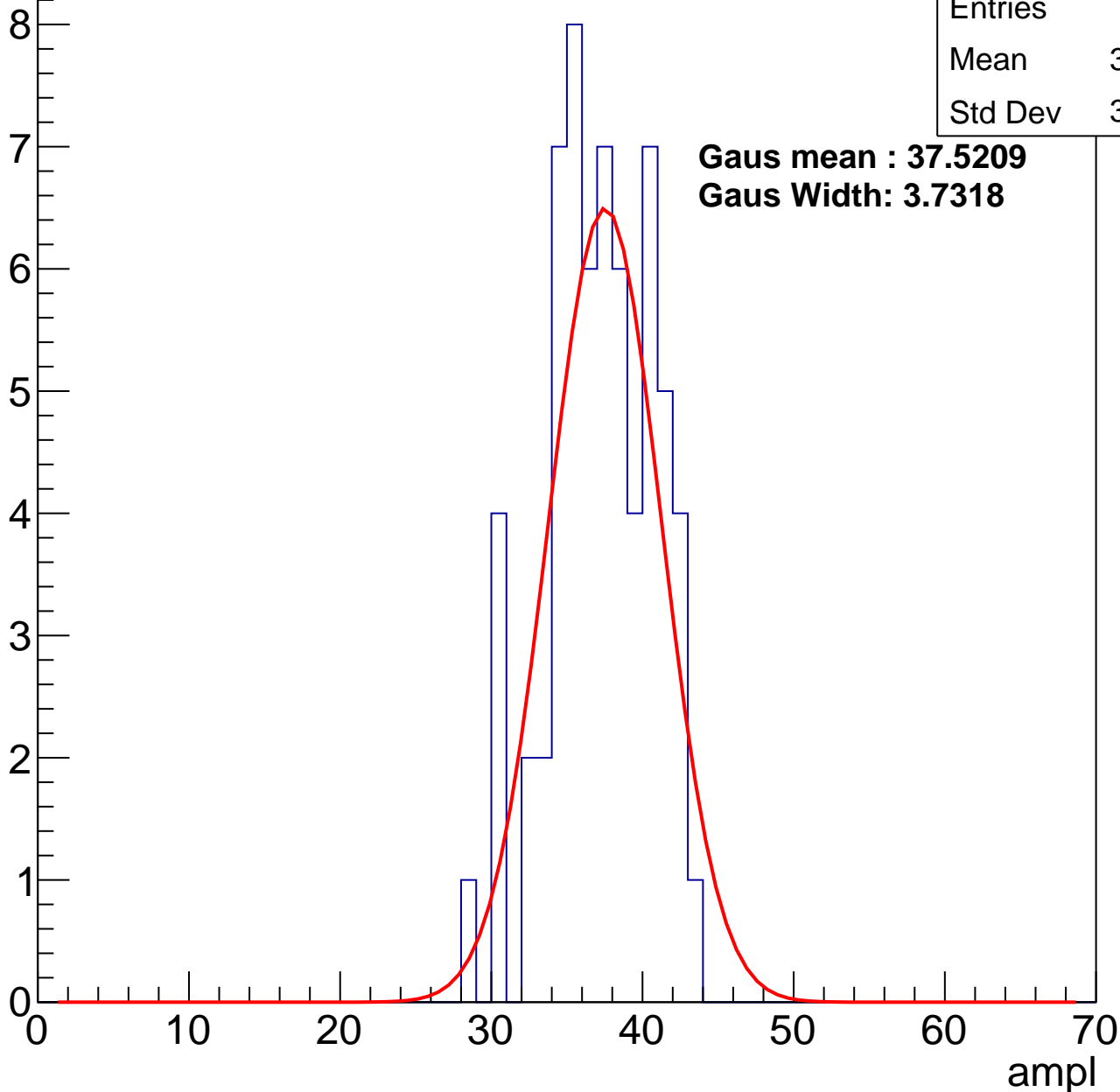
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	36.73
Std Dev	3.438

**Gaus mean : 37.5209**

**Gaus Width: 3.7318**



# B1L101S, U22-ch122, adc2

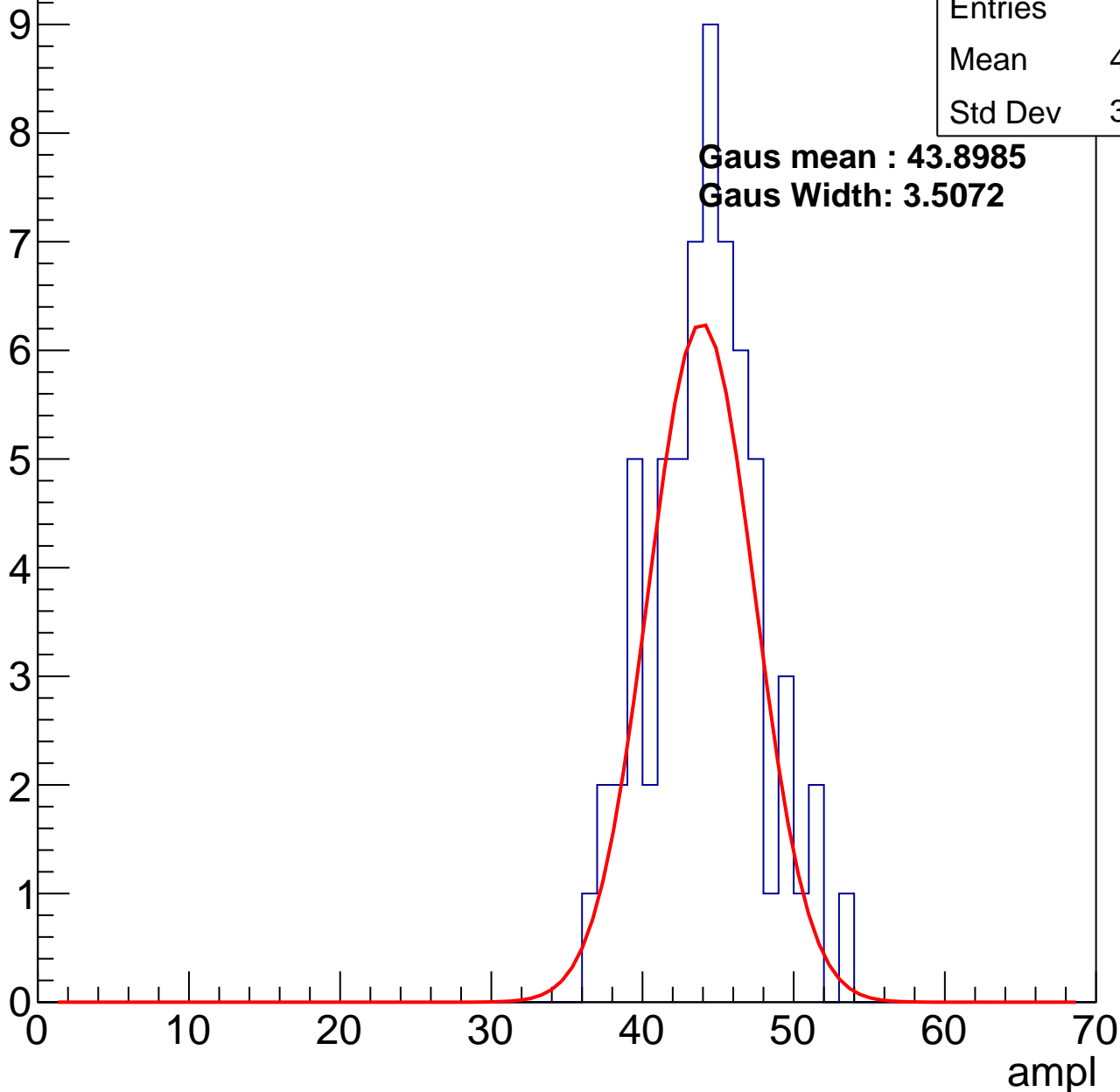
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	43.73
Std Dev	3.624

**Gaus mean : 43.8985**

**Gaus Width: 3.5072**

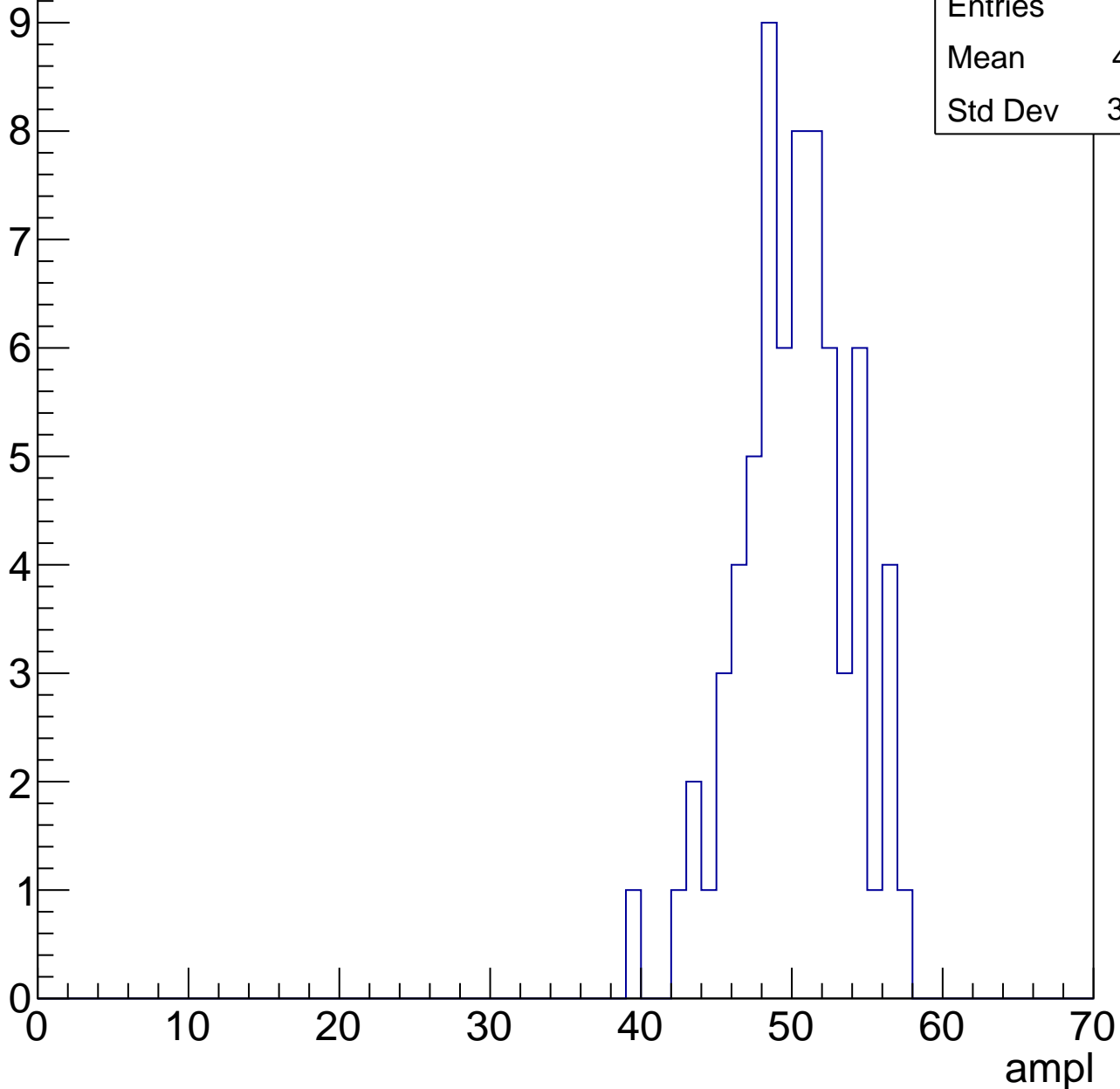


# B1L101S, U22-ch122, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	49.71
Std Dev	3.636

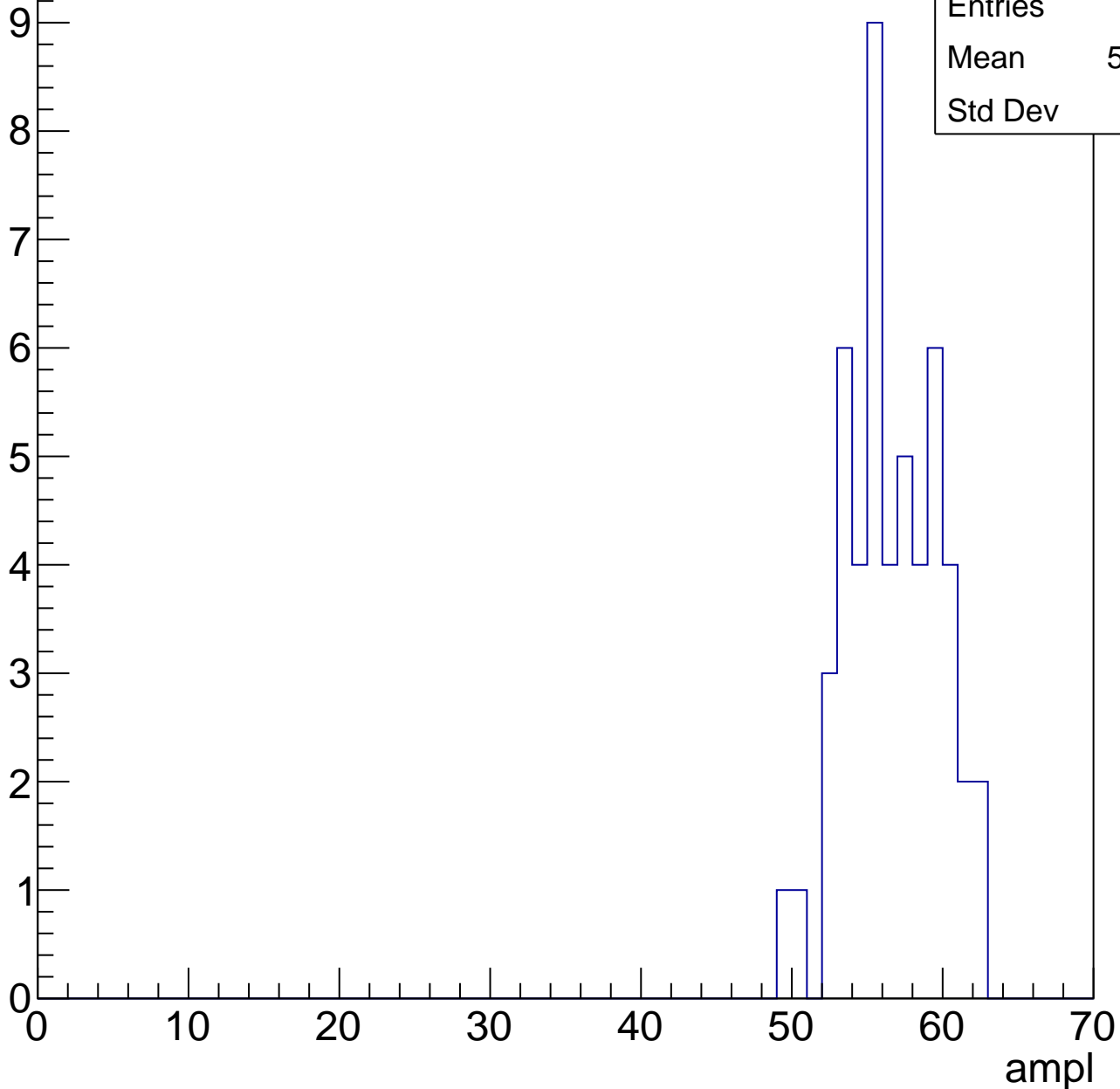


# B1L101S, U22-ch122, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	51
Mean	56.18
Std Dev	3.04

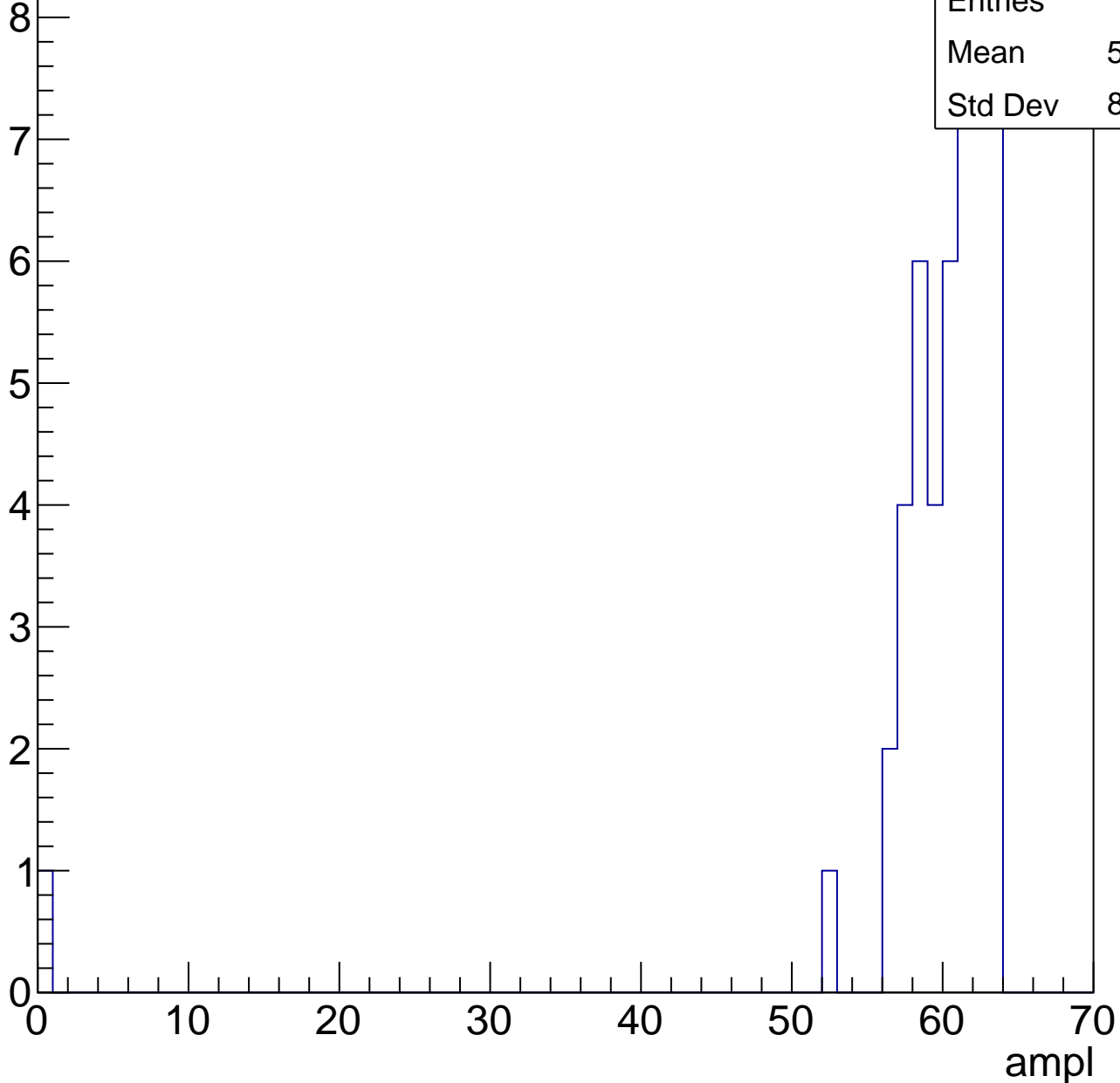


# B1L101S, U22-ch122, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	48
Mean	58.83
Std Dev	8.905



# B1L101S, U22-ch122, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	2
Mean	63
Std Dev	0

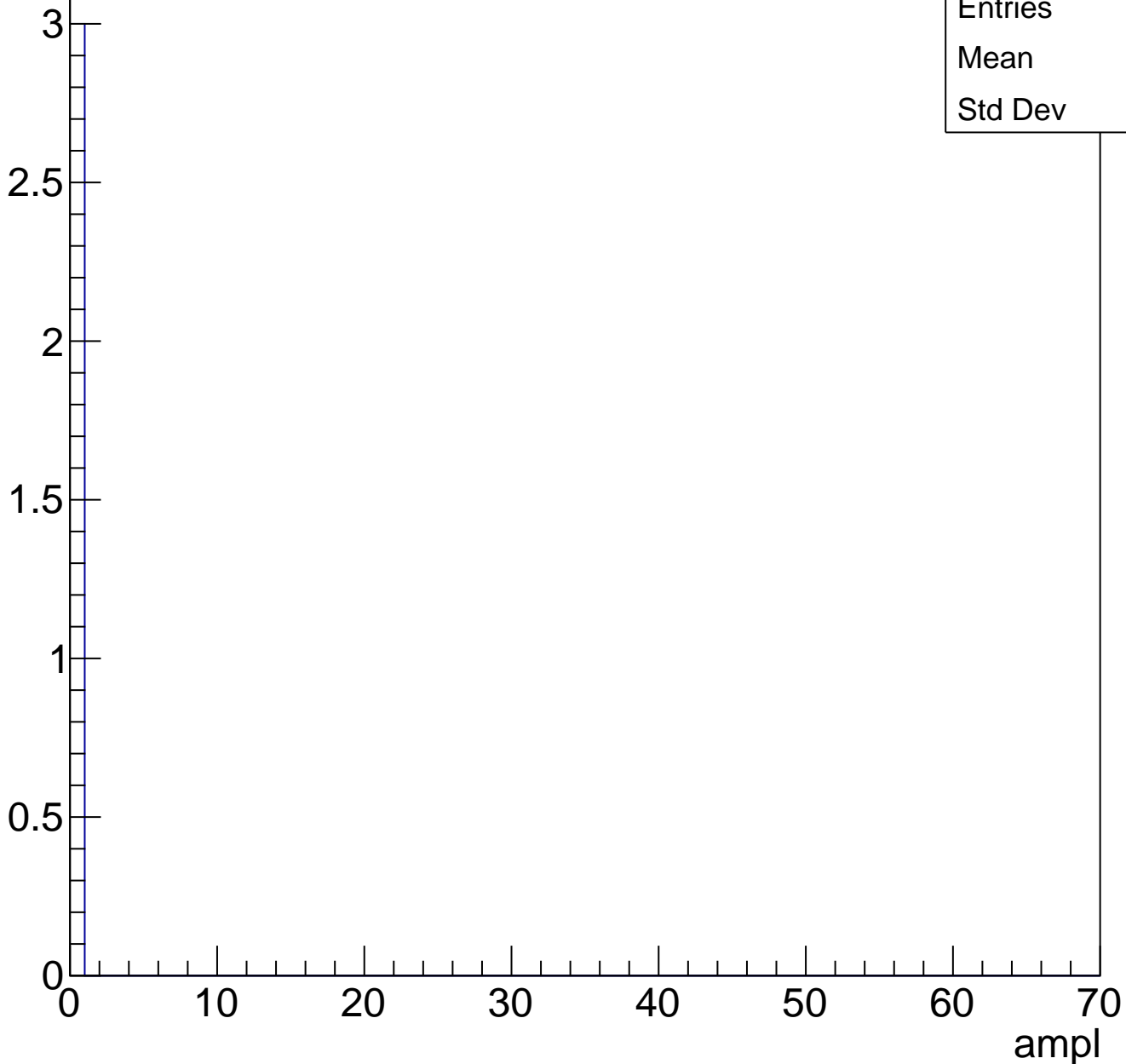
ampl



# B1L101S, U22-ch122, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U22-ch123, adc0

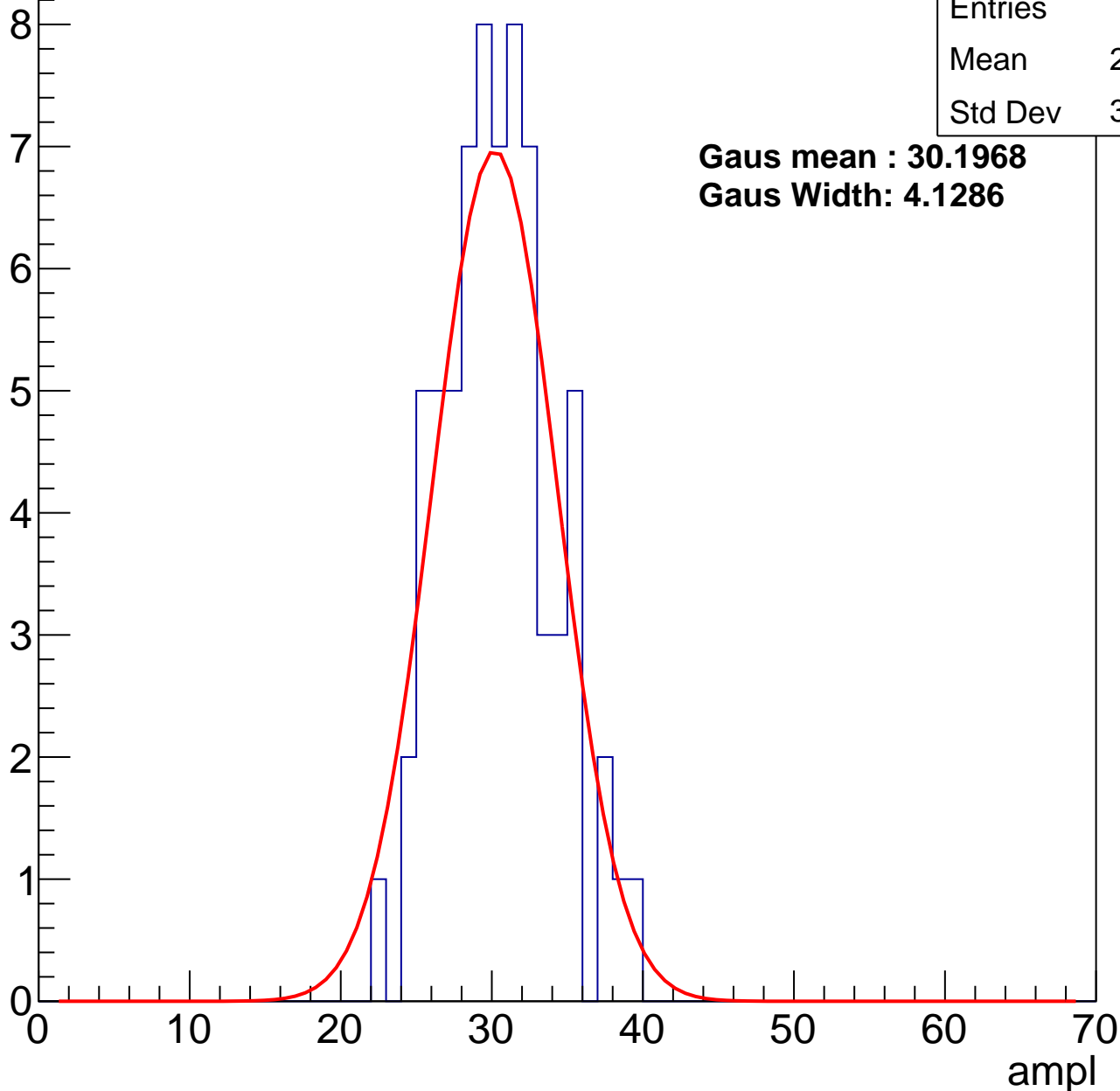
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	29.96
Std Dev	3.587

**Gaus mean : 30.1968**

**Gaus Width: 4.1286**



# B1L101S, U22-ch123, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	85
Mean	37.71
Std Dev	3.999

**Gaus mean : 37.9163**

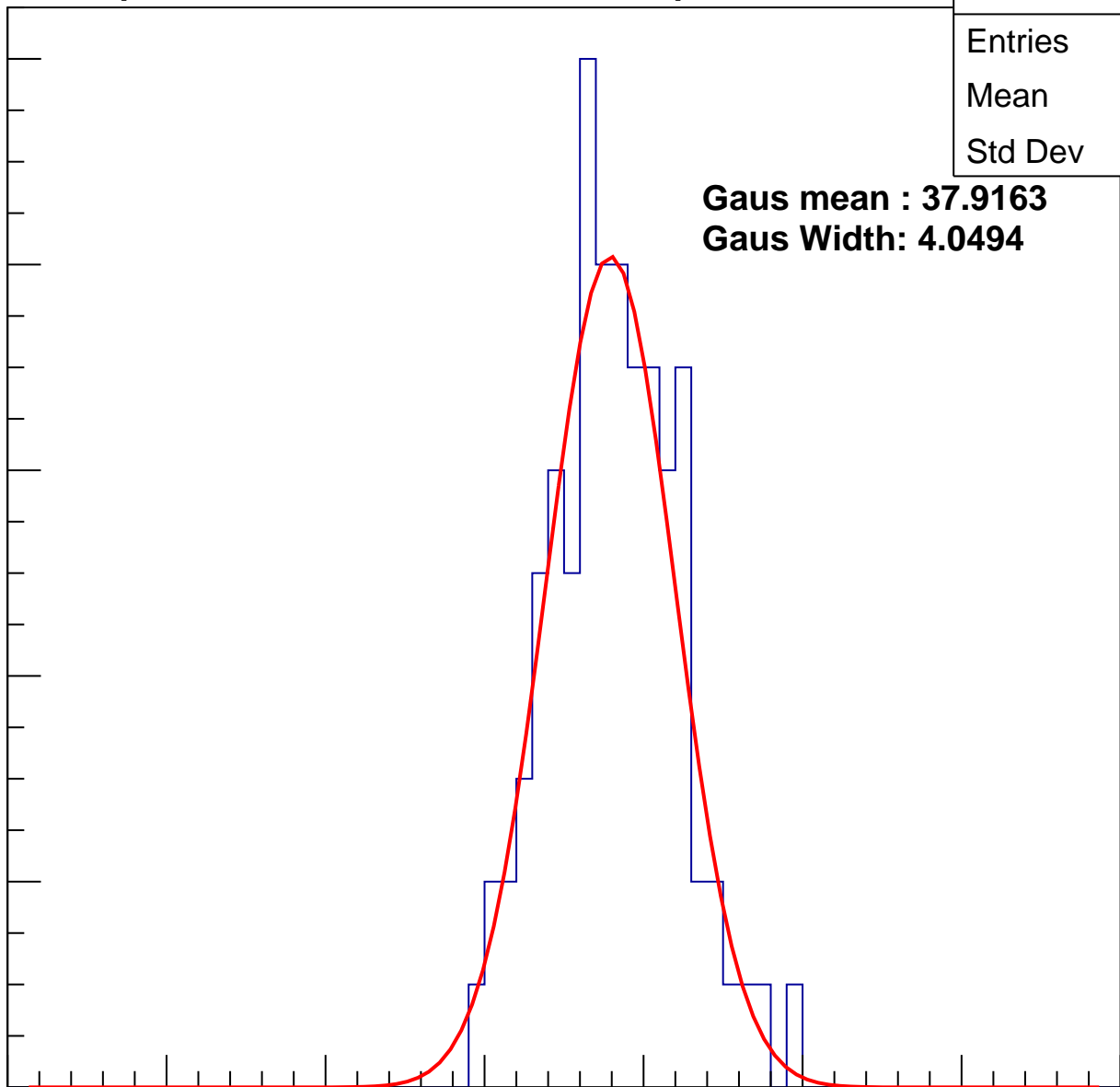
**Gaus Width: 4.0494**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U22-ch123, adc2

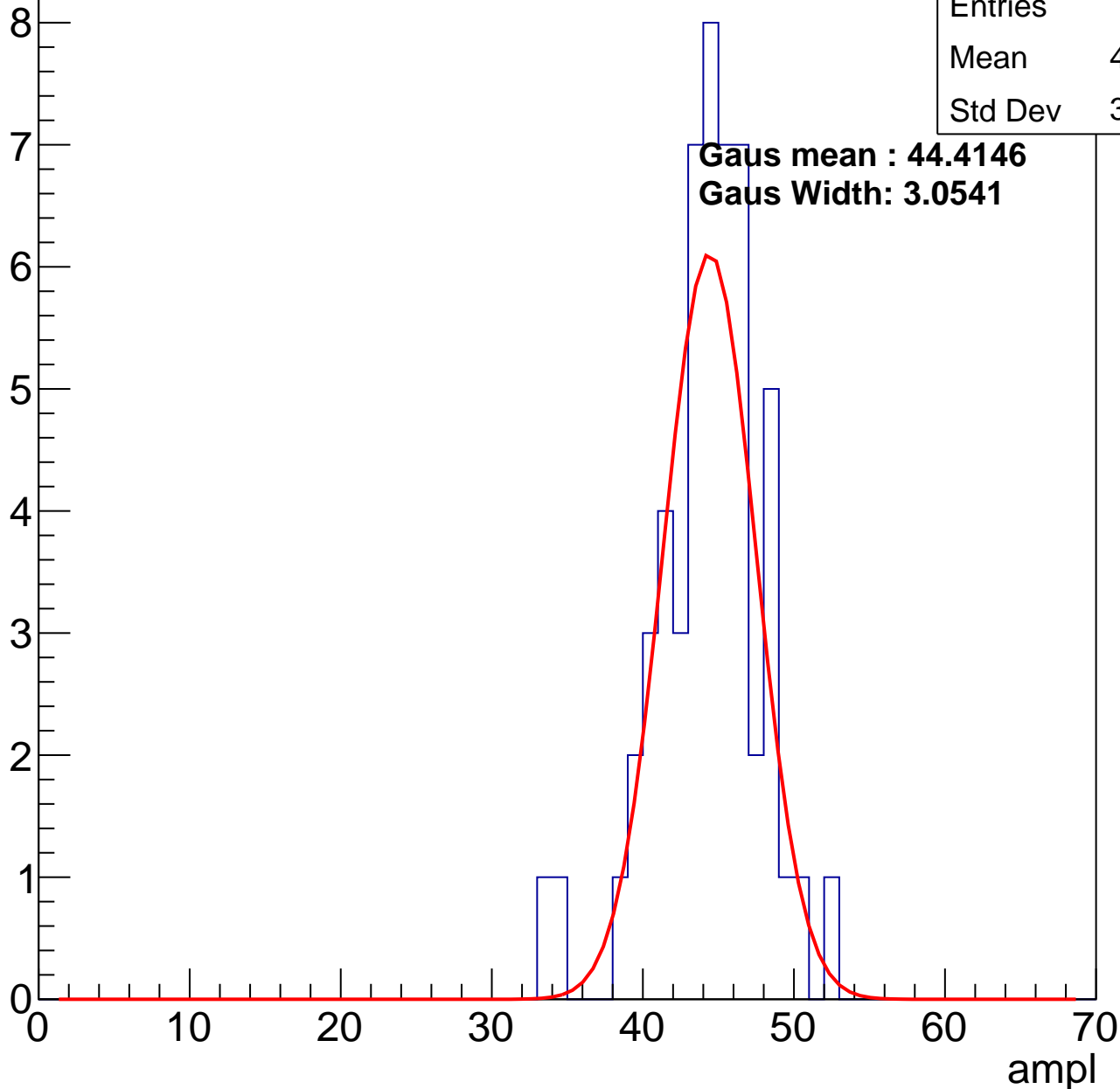
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	54
Mean	43.85
Std Dev	3.514

**Gaus mean : 44.4146**

**Gaus Width: 3.0541**



# B1L101S, U22-ch123, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	86
Mean	51.77
Std Dev	3.665

Entry

10

8

6

4

2

0

0

10

20

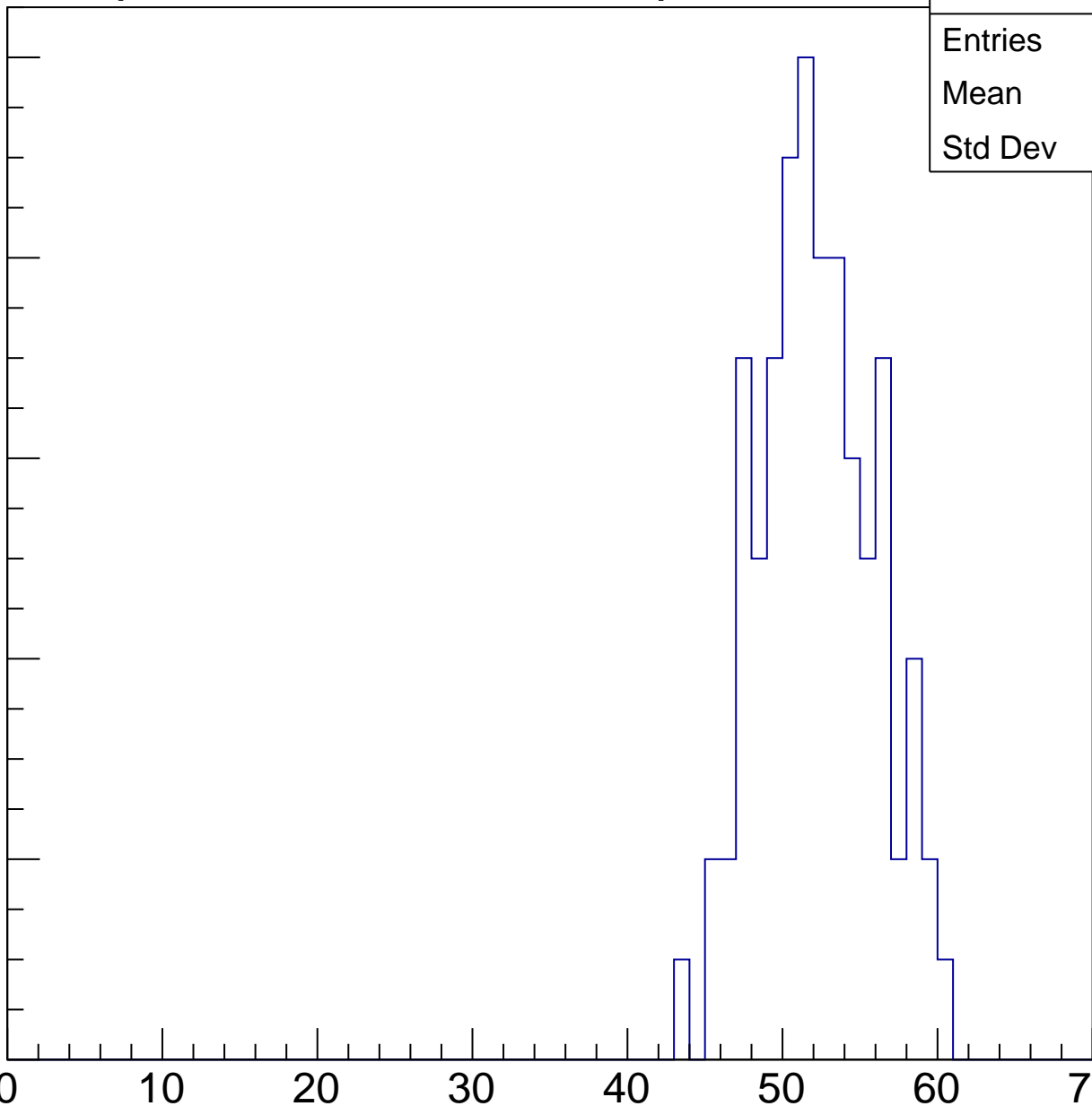
30

40

50

60

ampl

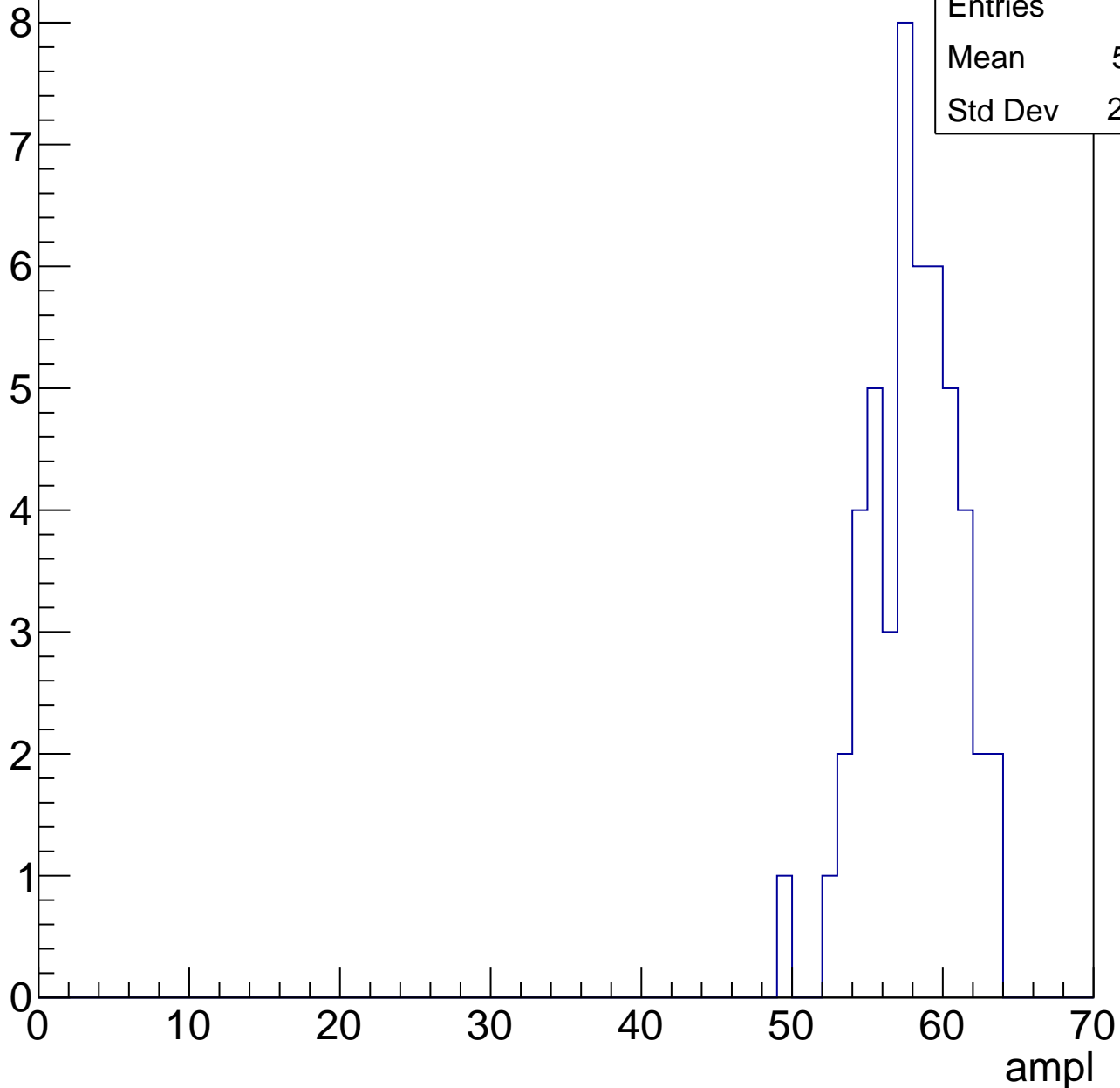


# B1L101S, U22-ch123, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	49
Mean	57.51
Std Dev	2.956

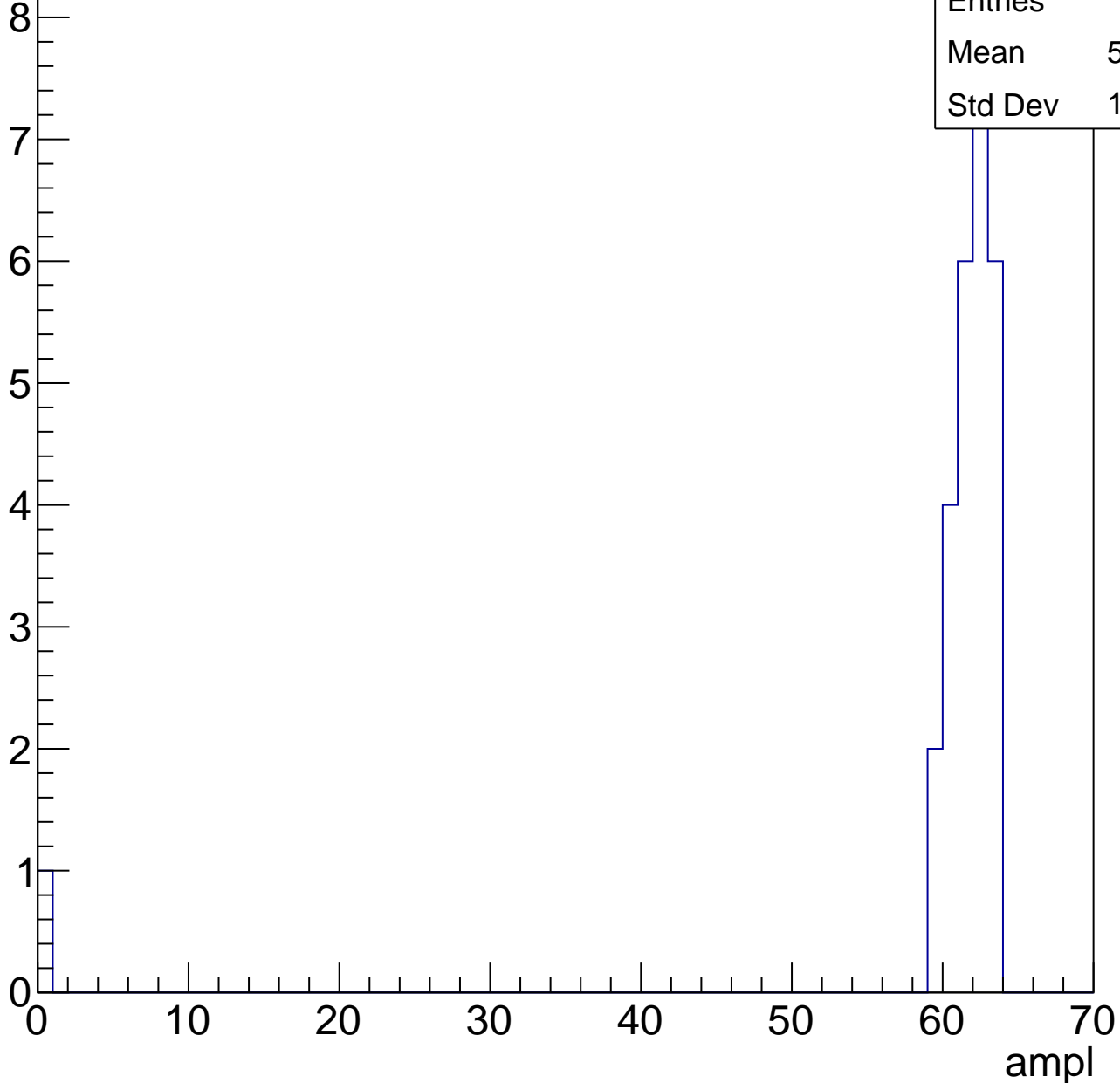


# B1L101S, U22-ch123, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	27
Mean	59.19
Std Dev	11.67



# B1L101S, U22-ch123, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

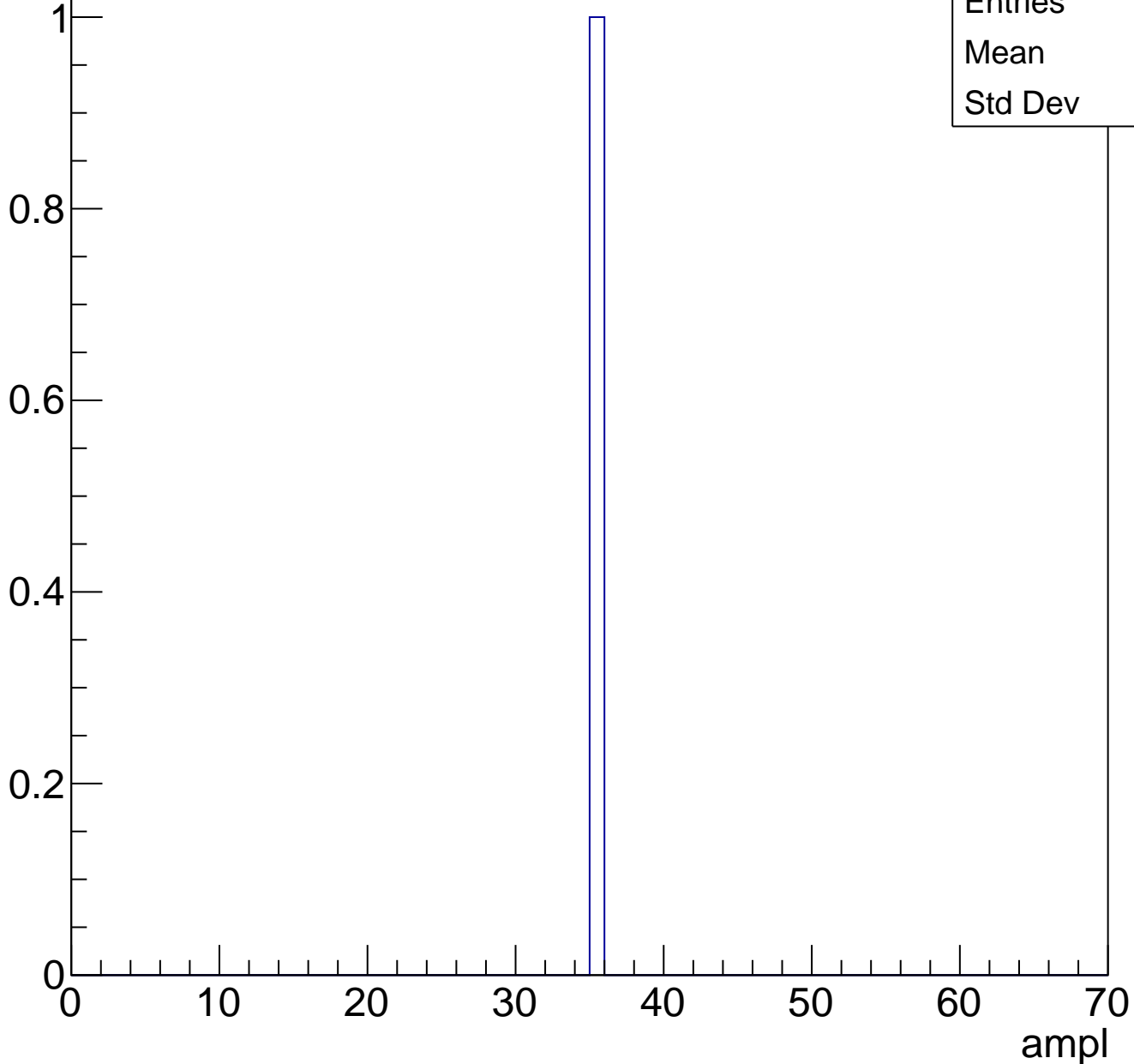




# B1L101S, U22-ch123, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U22-ch124, adc0

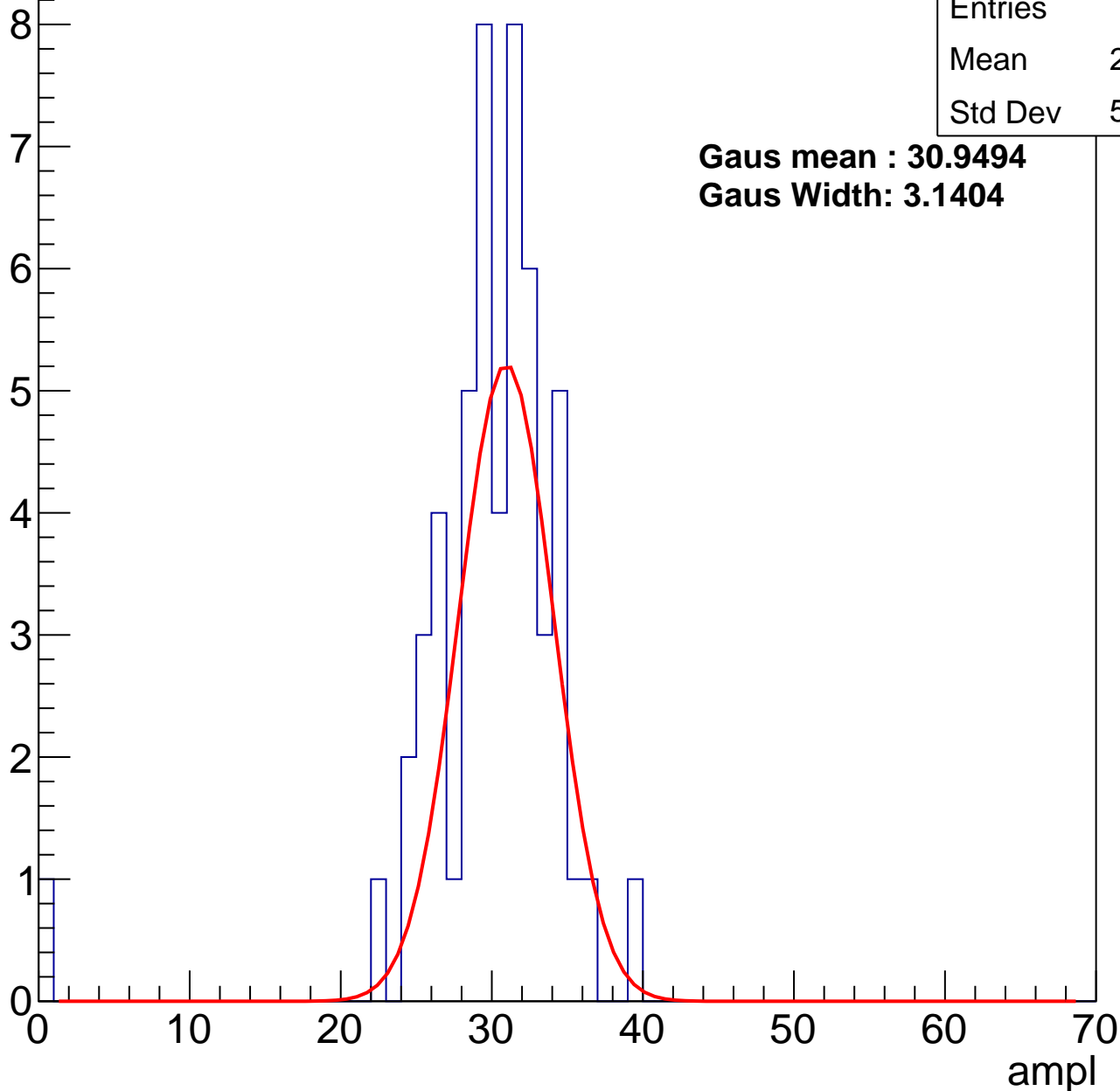
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	54
Mean	29.39
Std Dev	5.223

**Gaus mean : 30.9494**

**Gaus Width: 3.1404**



# B1L101S, U22-ch124, adc1

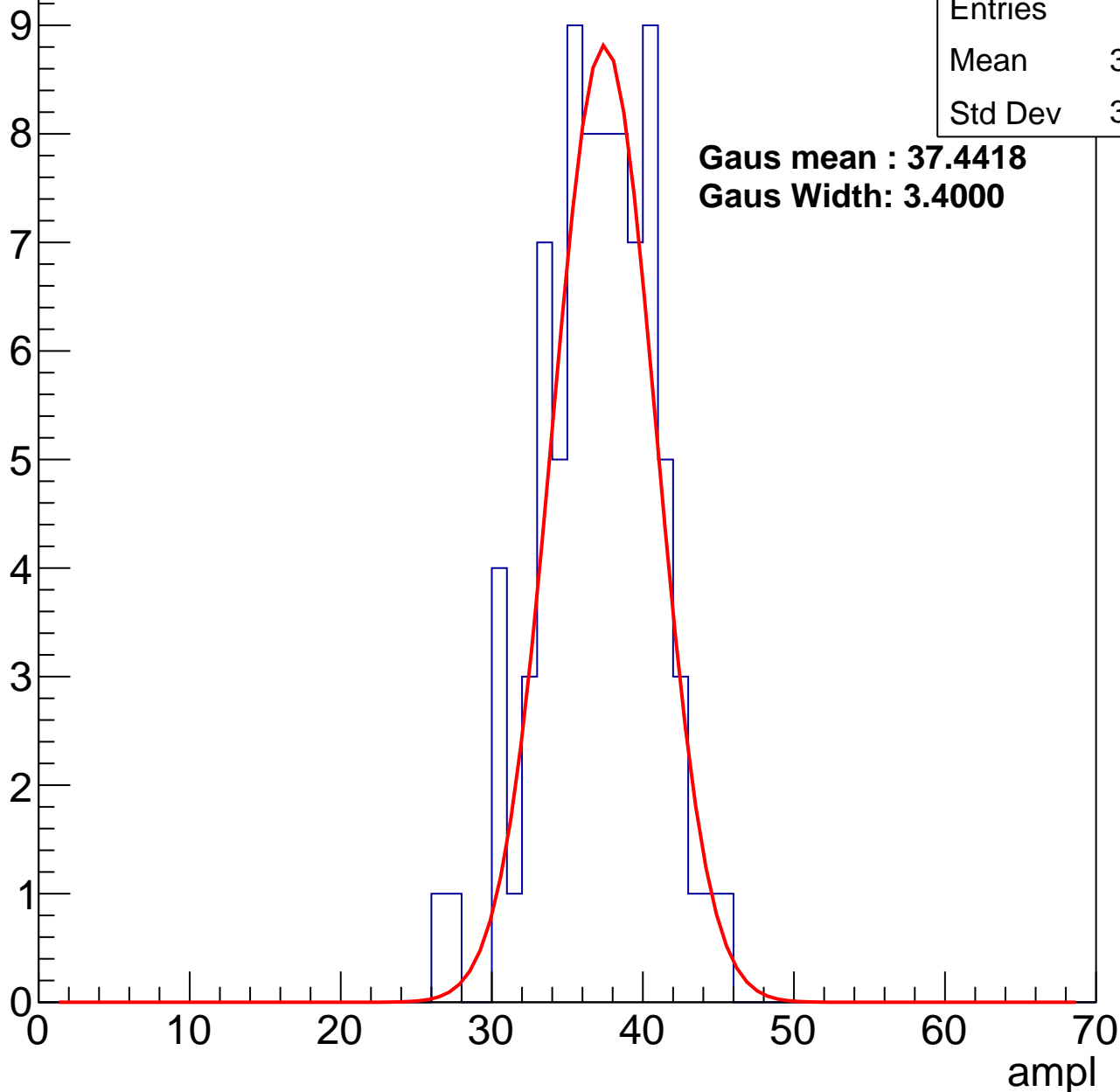
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	82
Mean	36.59
Std Dev	3.722

**Gaus mean : 37.4418**

**Gaus Width: 3.4000**



# B1L101S, U22-ch124, adc2

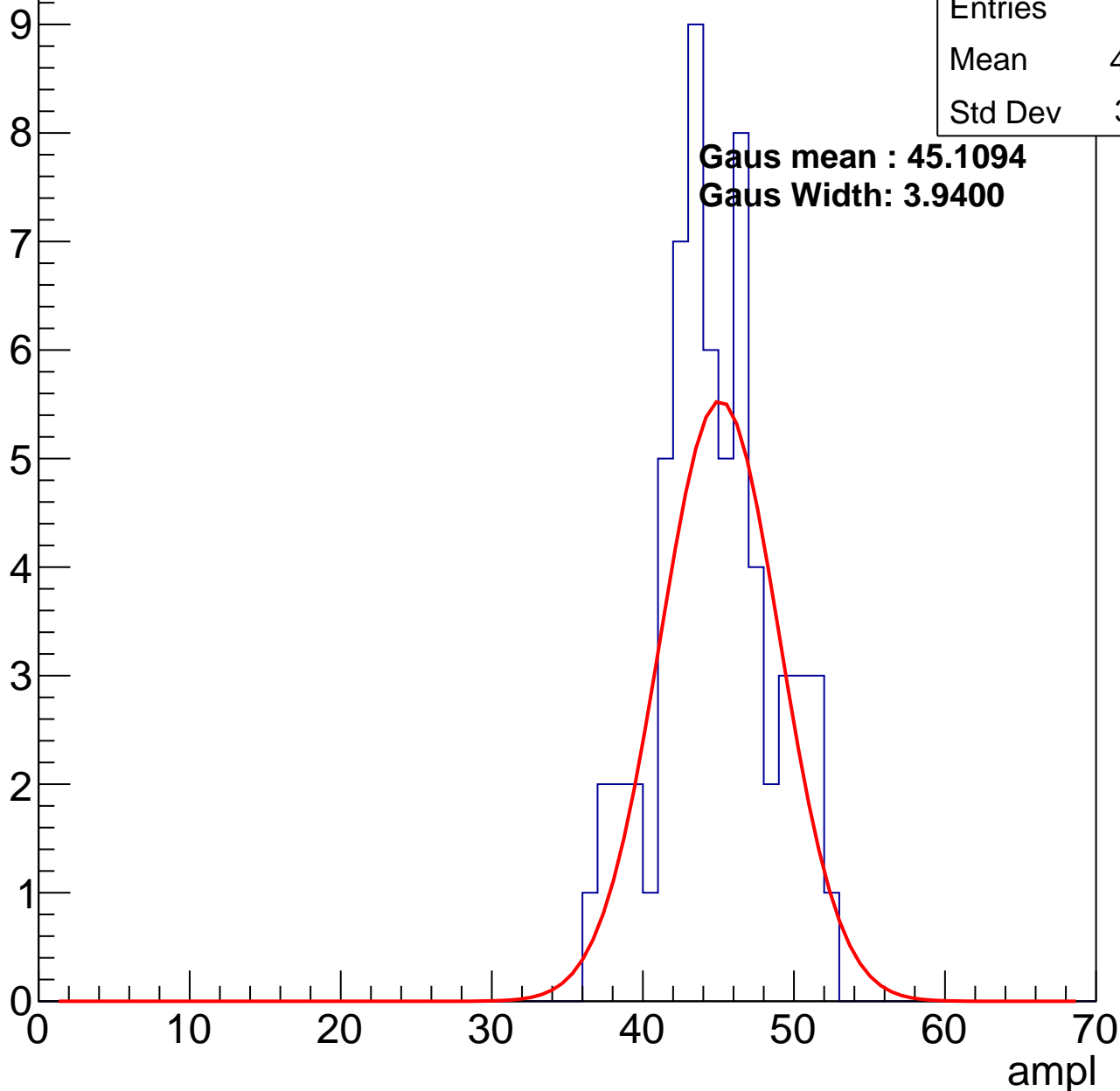
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	44.27
Std Dev	3.701

**Gaus mean : 45.1094**

**Gaus Width: 3.9400**

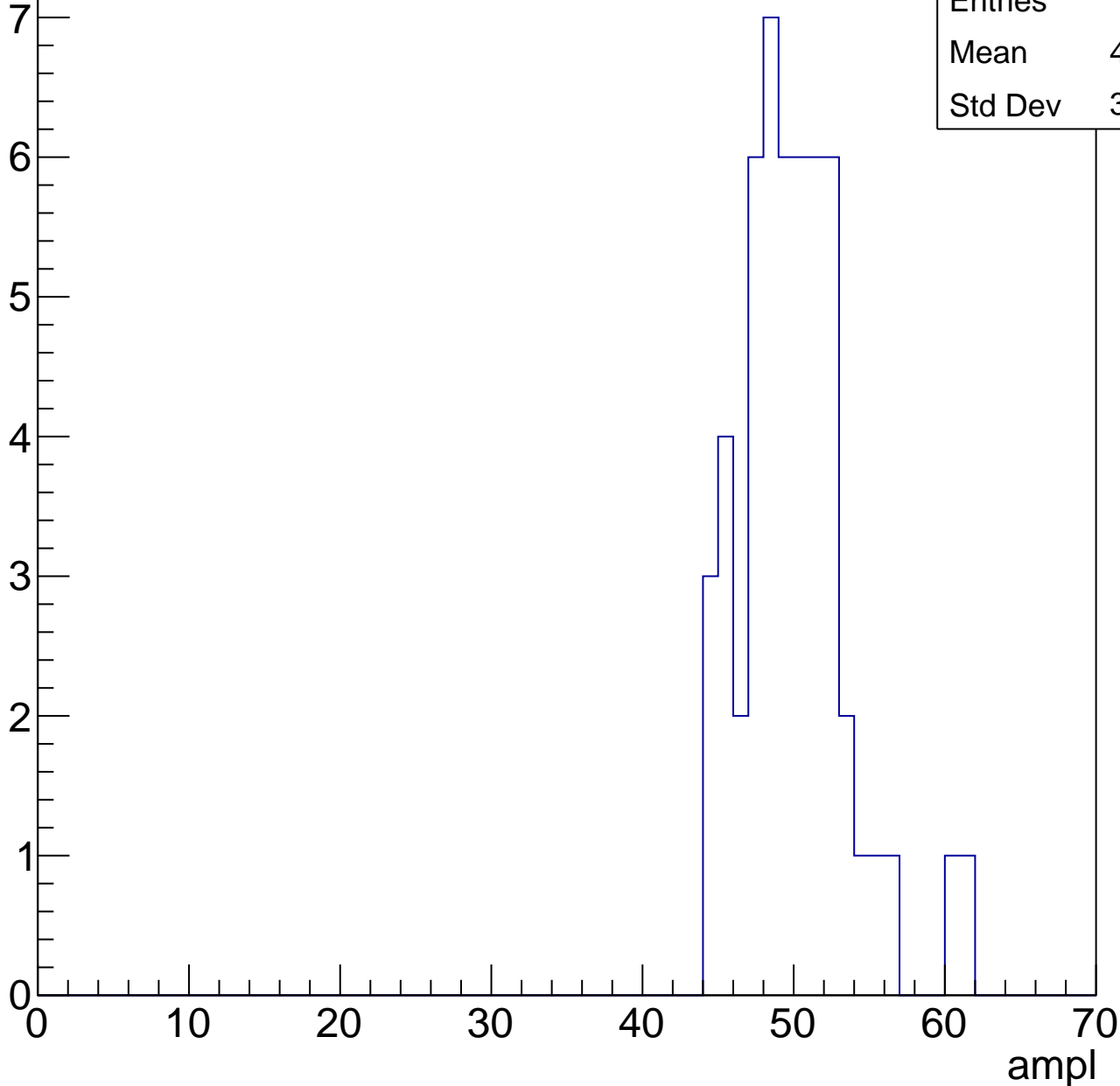


# B1L101S, U22-ch124, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	53
Mean	49.55
Std Dev	3.537

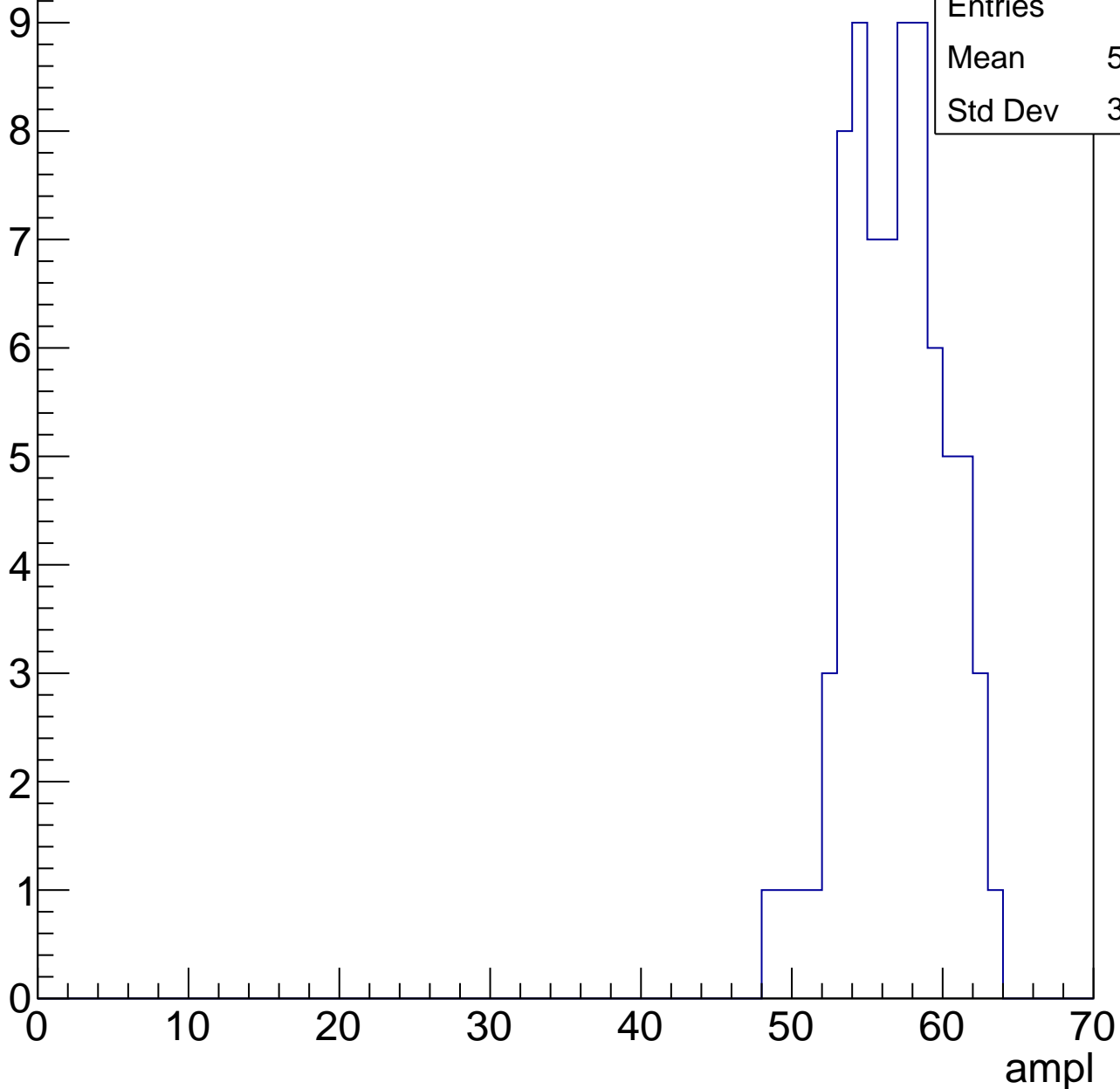


# B1L101S, U22-ch124, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	76
Mean	56.37
Std Dev	3.219

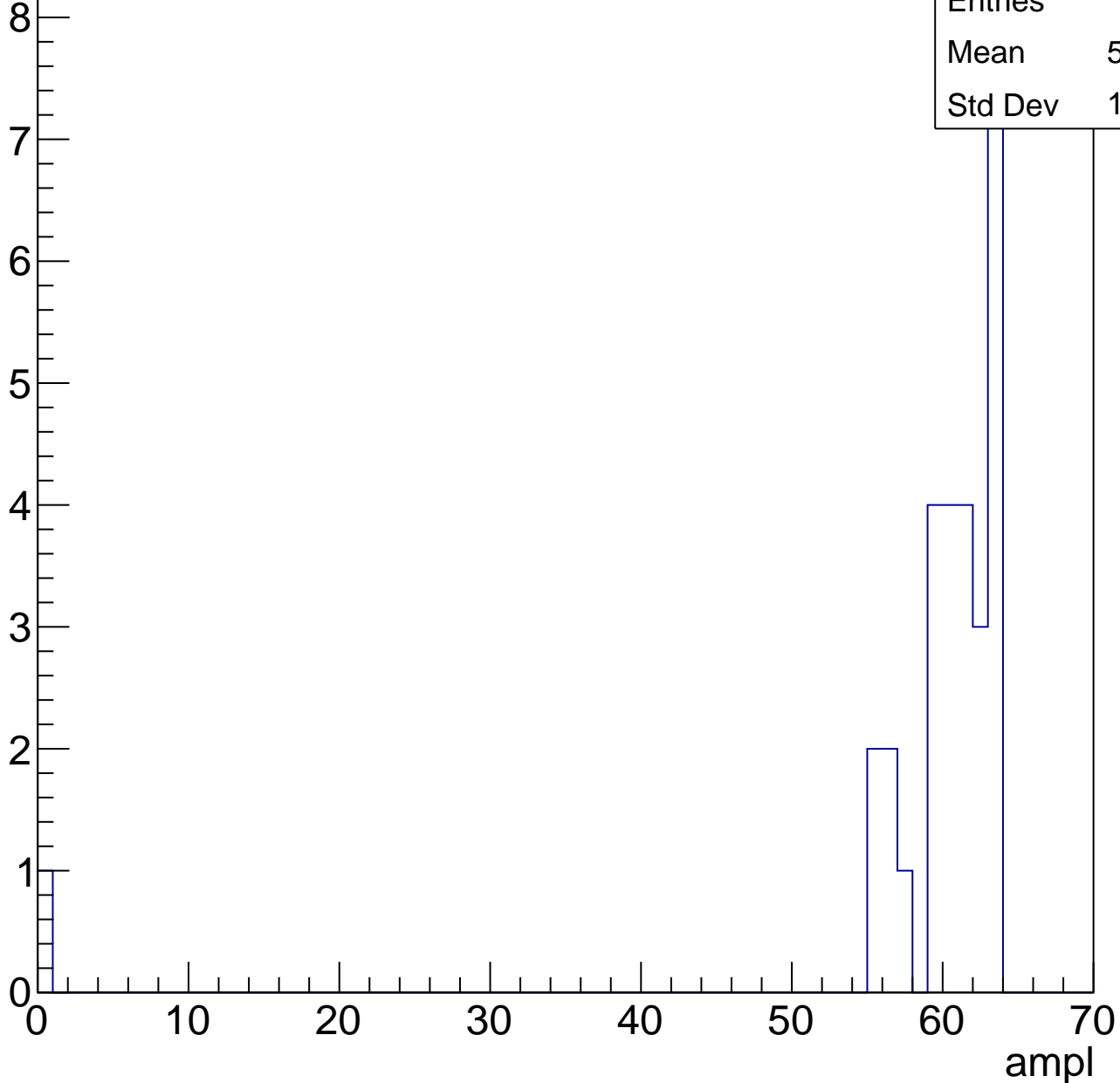


# B1L101S, U22-ch124, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

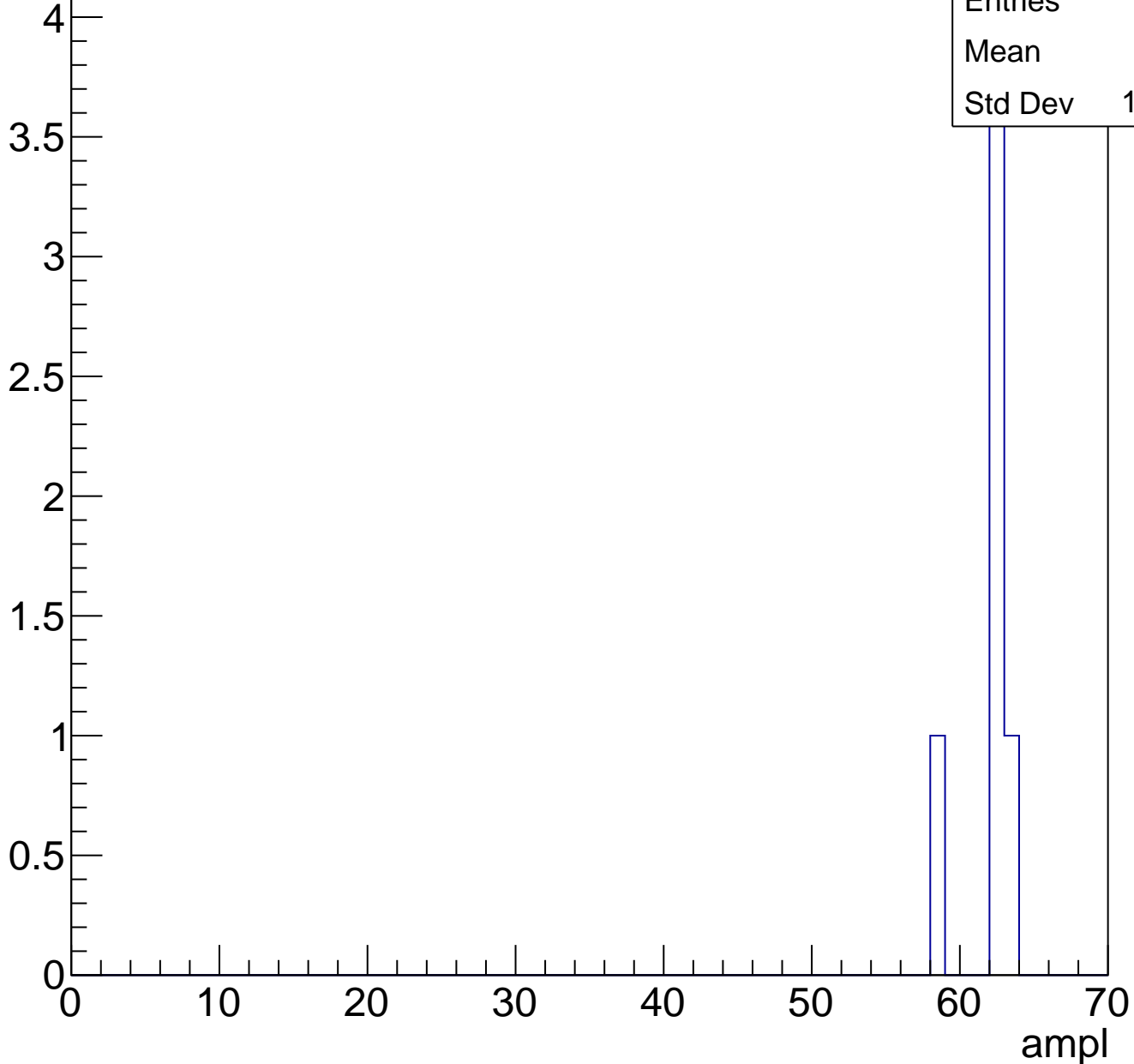
Entries	29
Mean	58.24
Std Dev	11.29



# B1L101S, U22-ch124, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U22-ch124, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U22-ch125, adc0

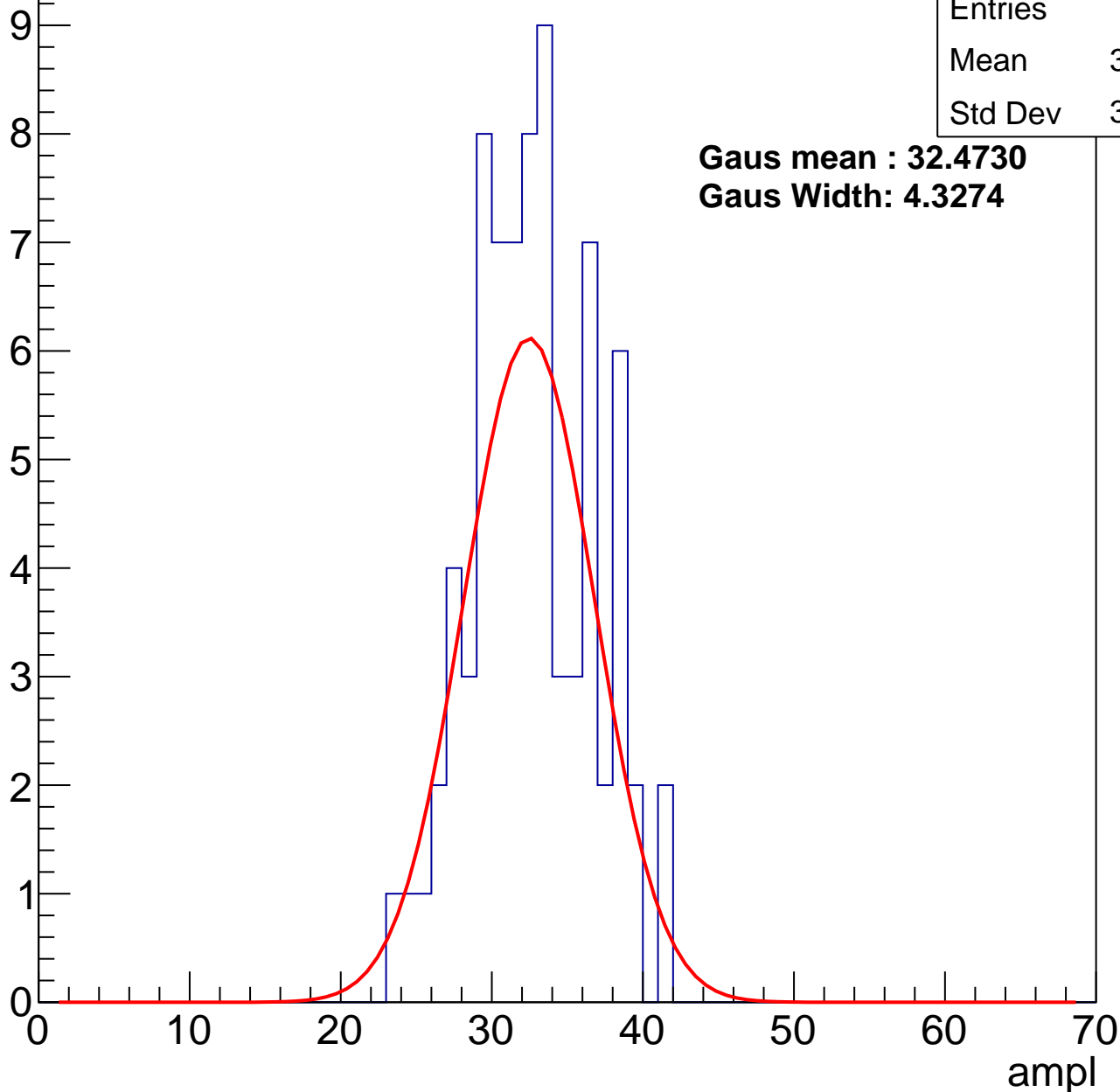
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	76
Mean	32.22
Std Dev	3.979

**Gaus mean : 32.4730**

**Gaus Width: 4.3274**



# B1L101S, U22-ch125, adc1

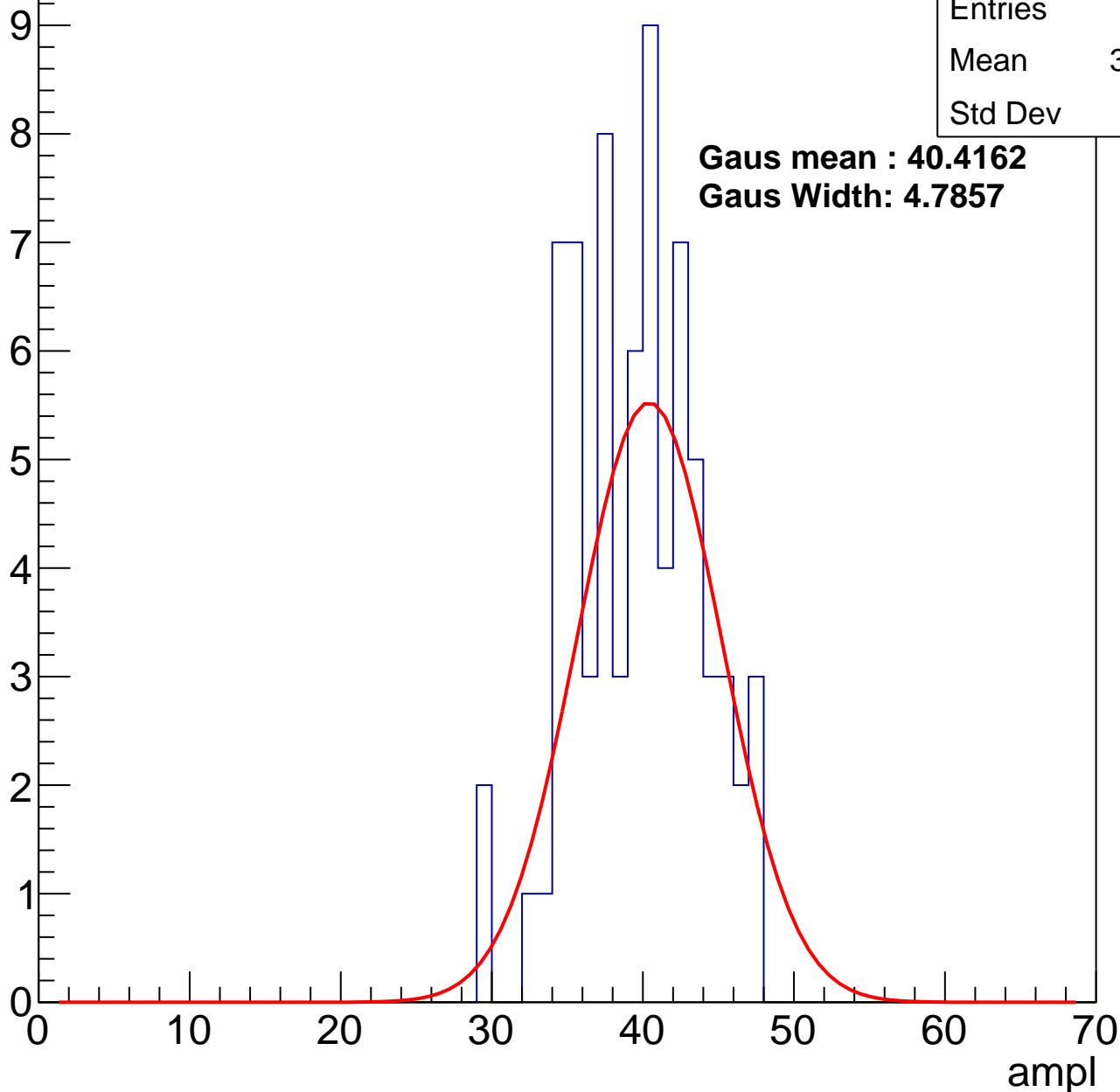
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	74
Mean	39.07
Std Dev	4.15

**Gaus mean : 40.4162**

**Gaus Width: 4.7857**



# B1L101S, U22-ch125, adc2

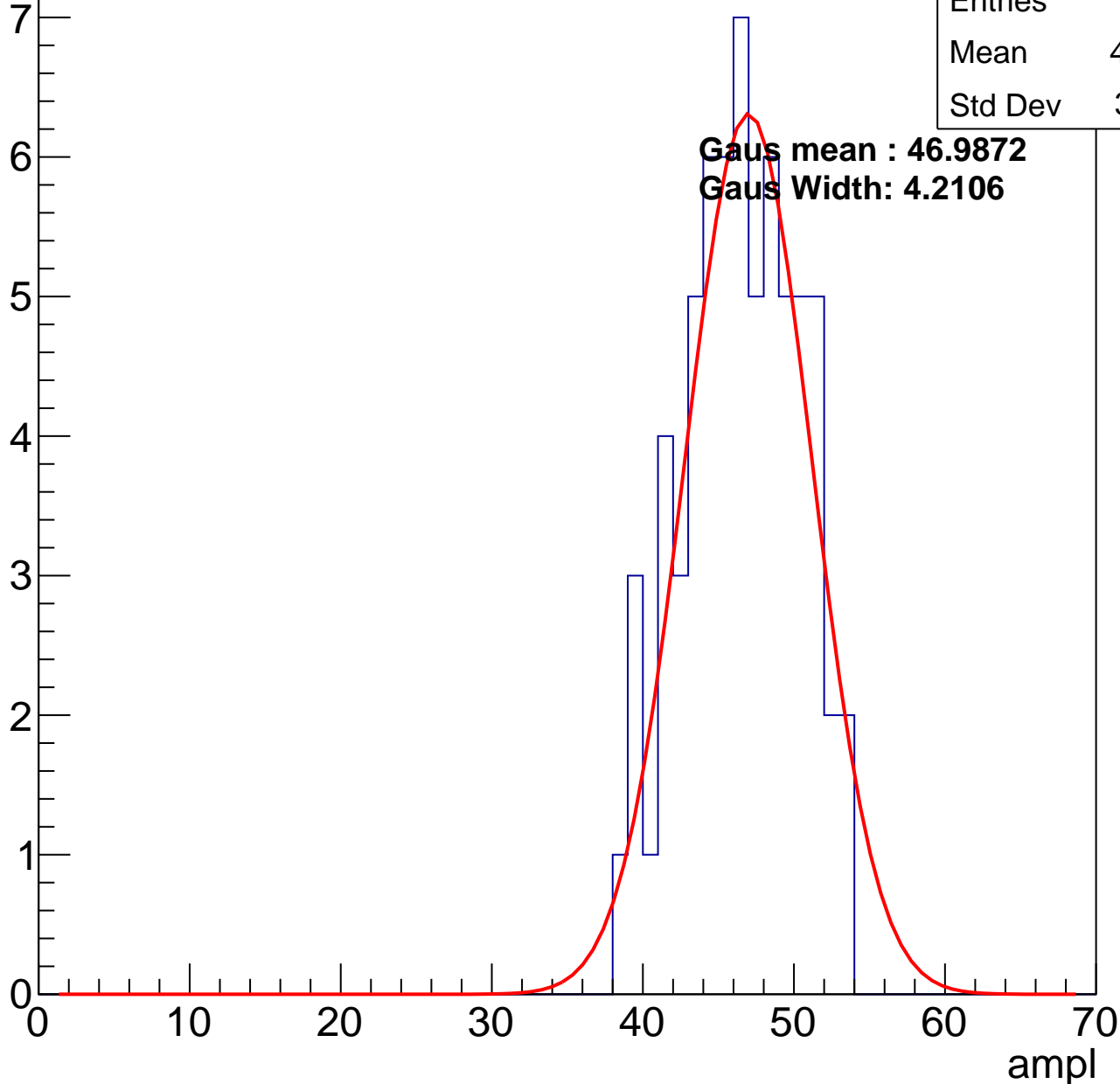
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	66
Mean	46.05
Std Dev	3.731

**Gaus mean : 46.9872**

**Gaus Width: 4.2106**

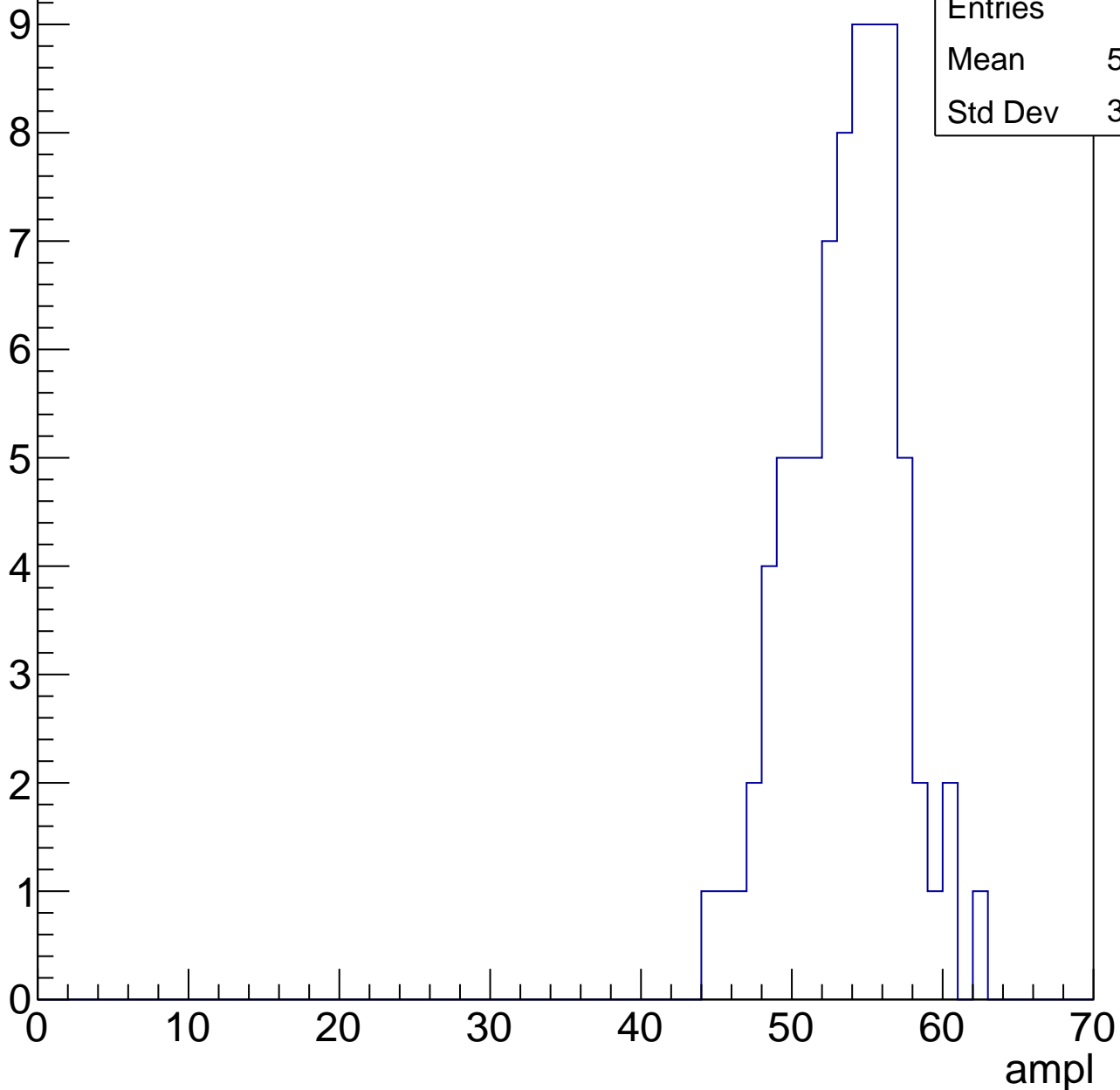


# B1L101S, U22-ch125, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	77
Mean	53.06
Std Dev	3.583

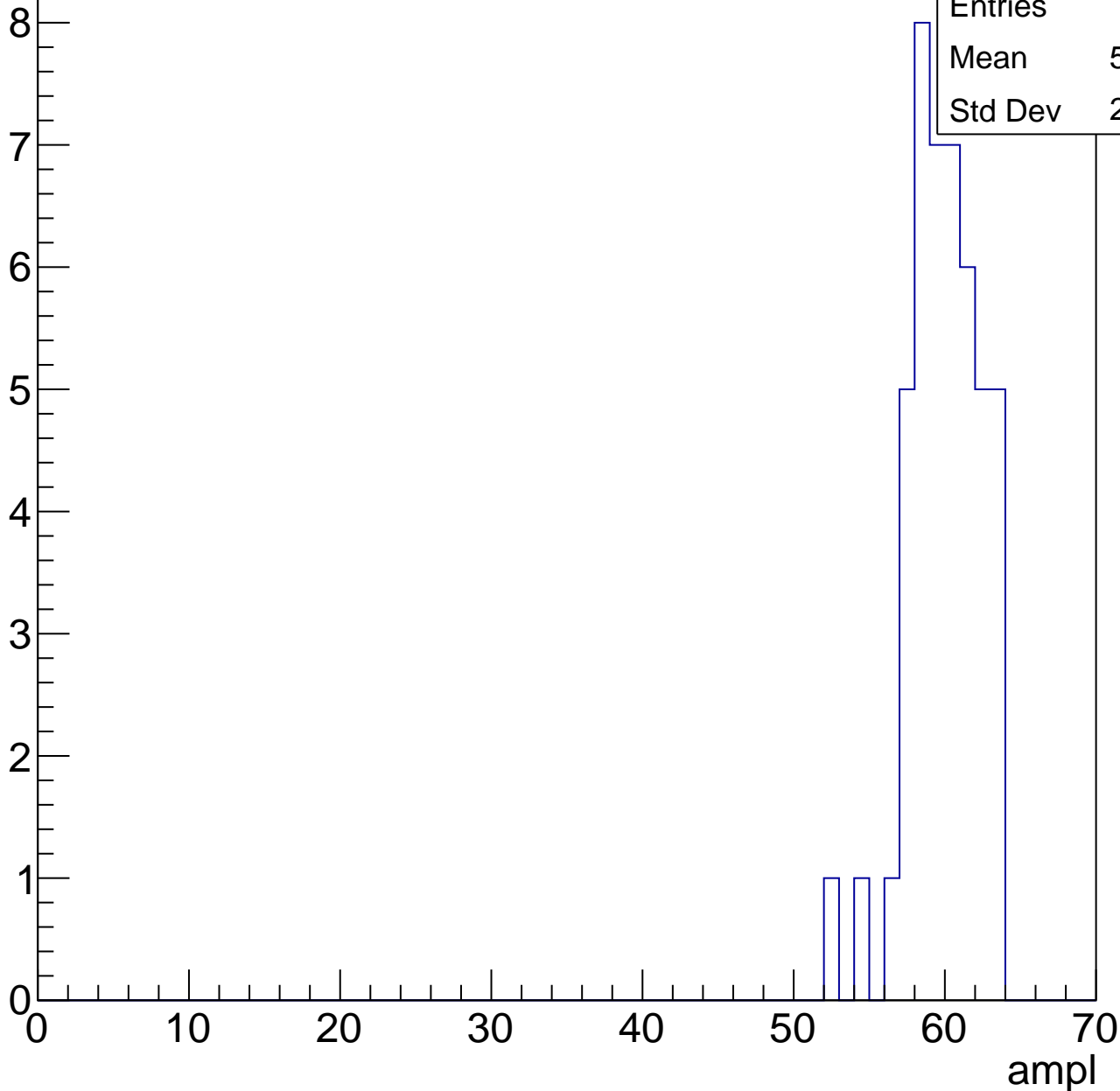


# B1L101S, U22-ch125, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	46
Mean	59.46
Std Dev	2.366

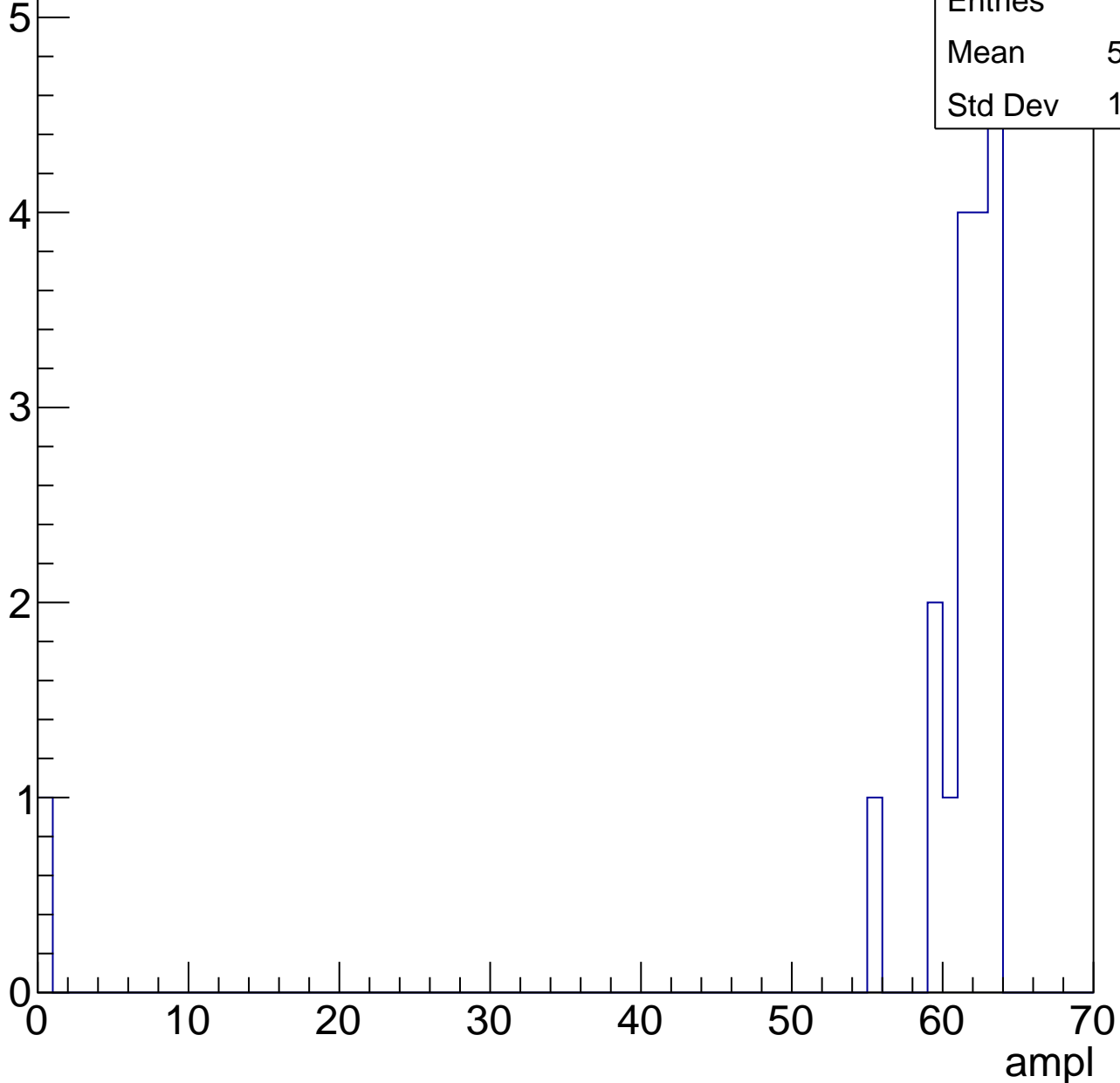


# B1L101S, U22-ch125, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	18
Mean	57.78
Std Dev	14.15



# B1L101S, U22-ch125, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0



# B1L101S, U22-ch125, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	22
Std Dev	0

# B1L101S, U22-ch126, adc0

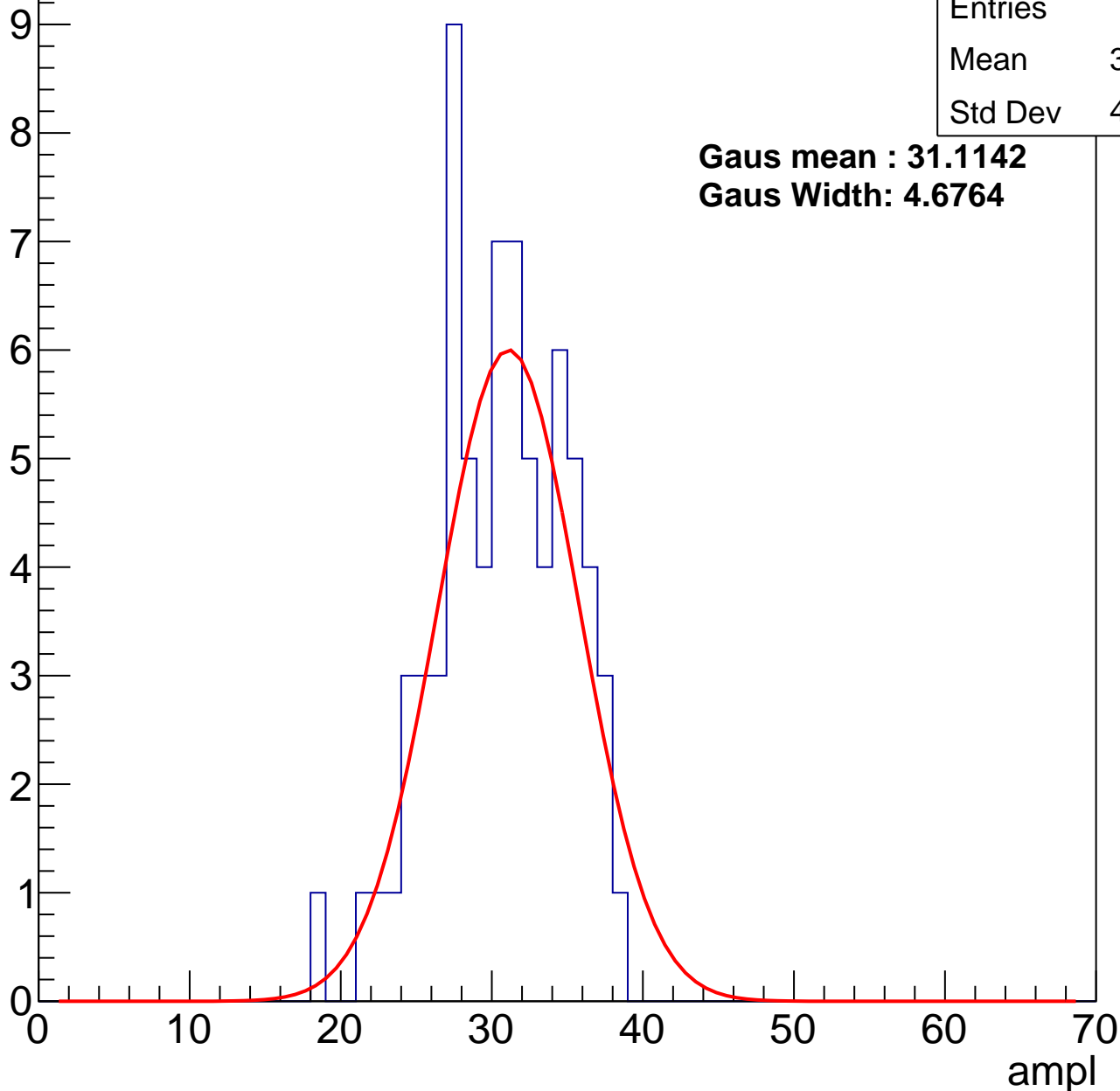
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	73
Mean	30.12
Std Dev	4.239

**Gaus mean : 31.1142**

**Gaus Width: 4.6764**



# B1L101S, U22-ch126, adc1

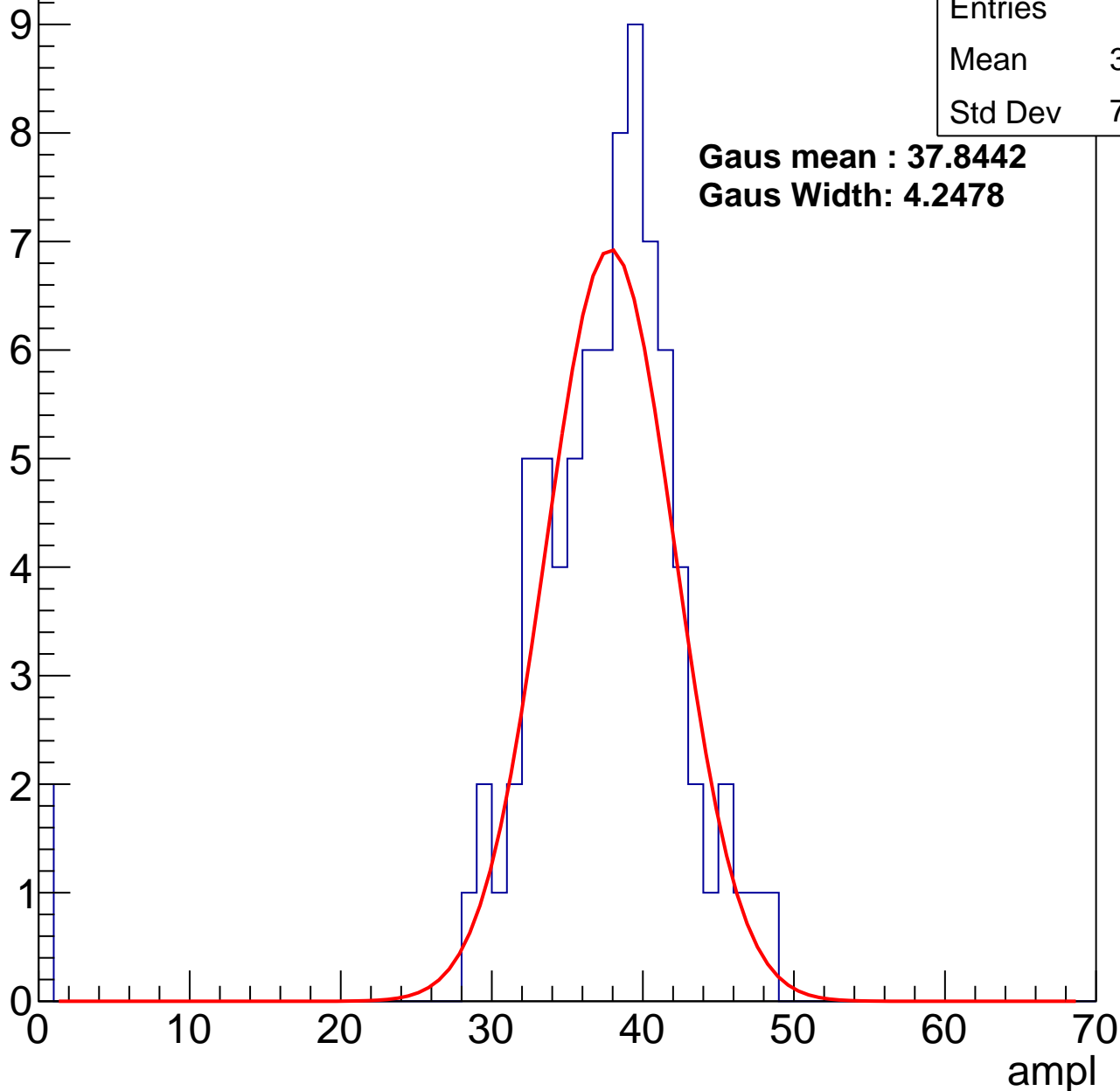
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	81
Mean	36.57
Std Dev	7.178

**Gaus mean : 37.8442**

**Gaus Width: 4.2478**



# B1L101S, U22-ch126, adc2

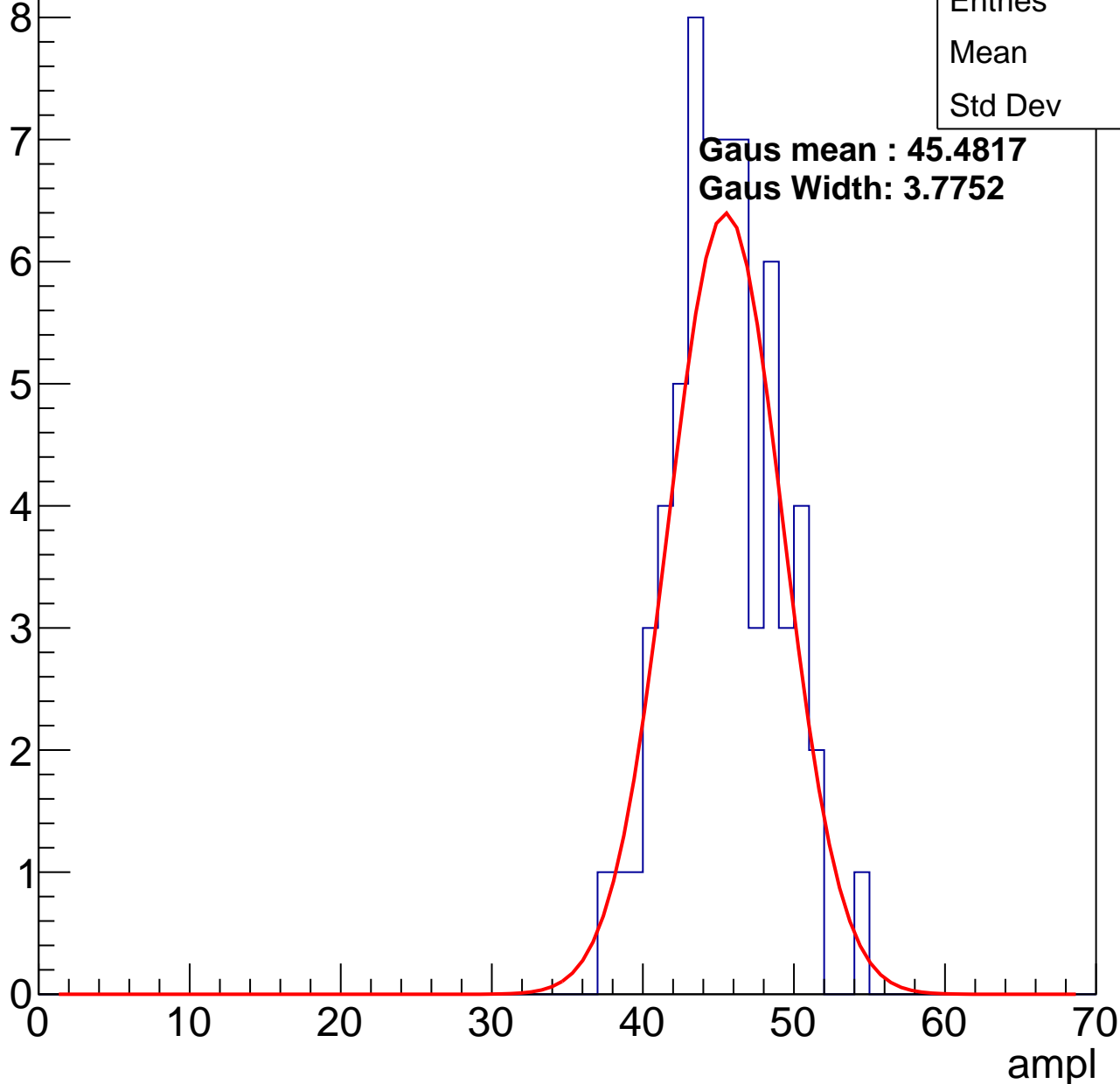
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	44.9
Std Dev	3.44

**Gaus mean : 45.4817**

**Gaus Width: 3.7752**



# B1L101S, U22-ch126, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

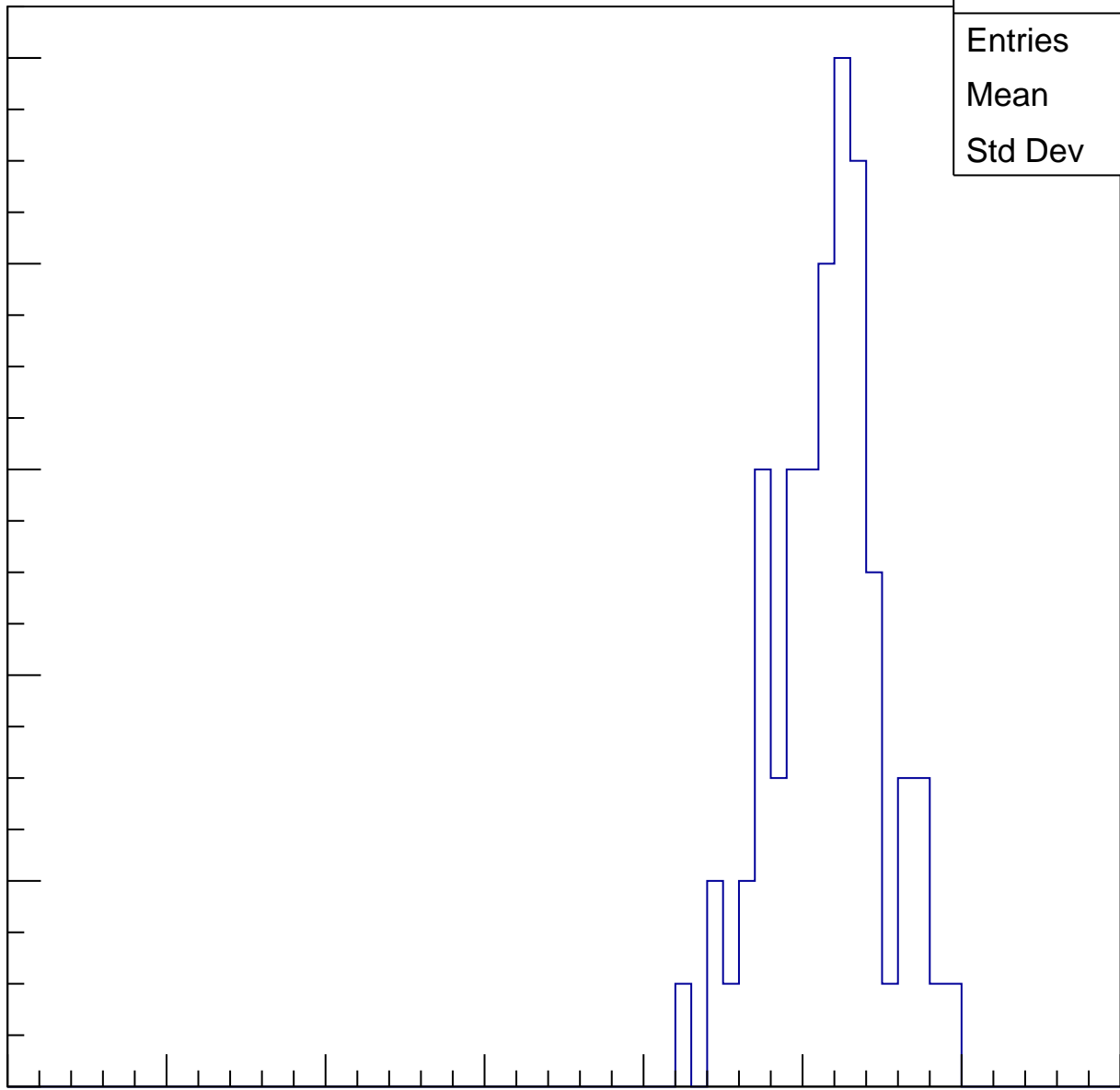
Entries	68
Mean	51.07
Std Dev	3.474

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

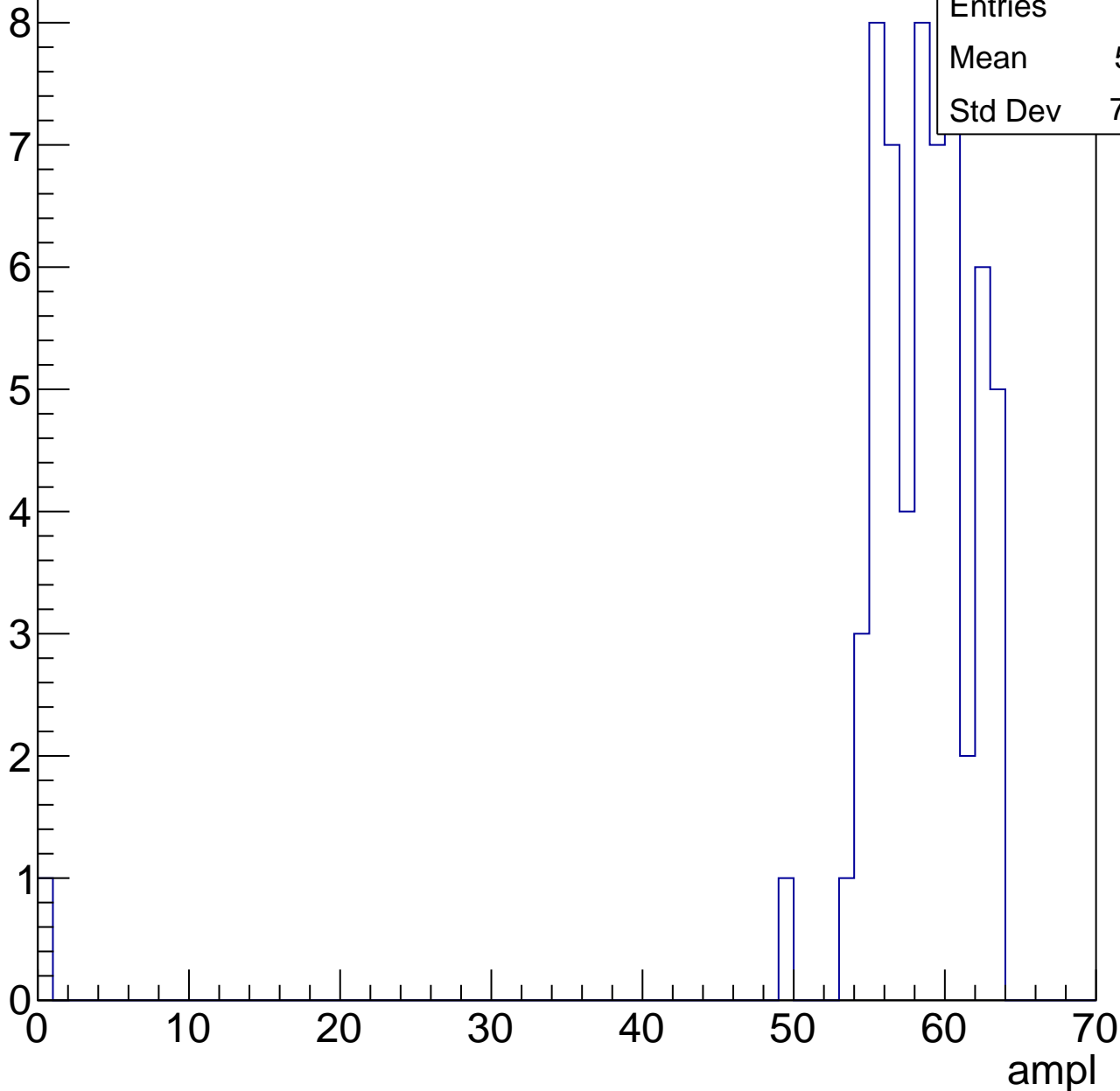


# B1L101S, U22-ch126, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	57.21
Std Dev	7.957

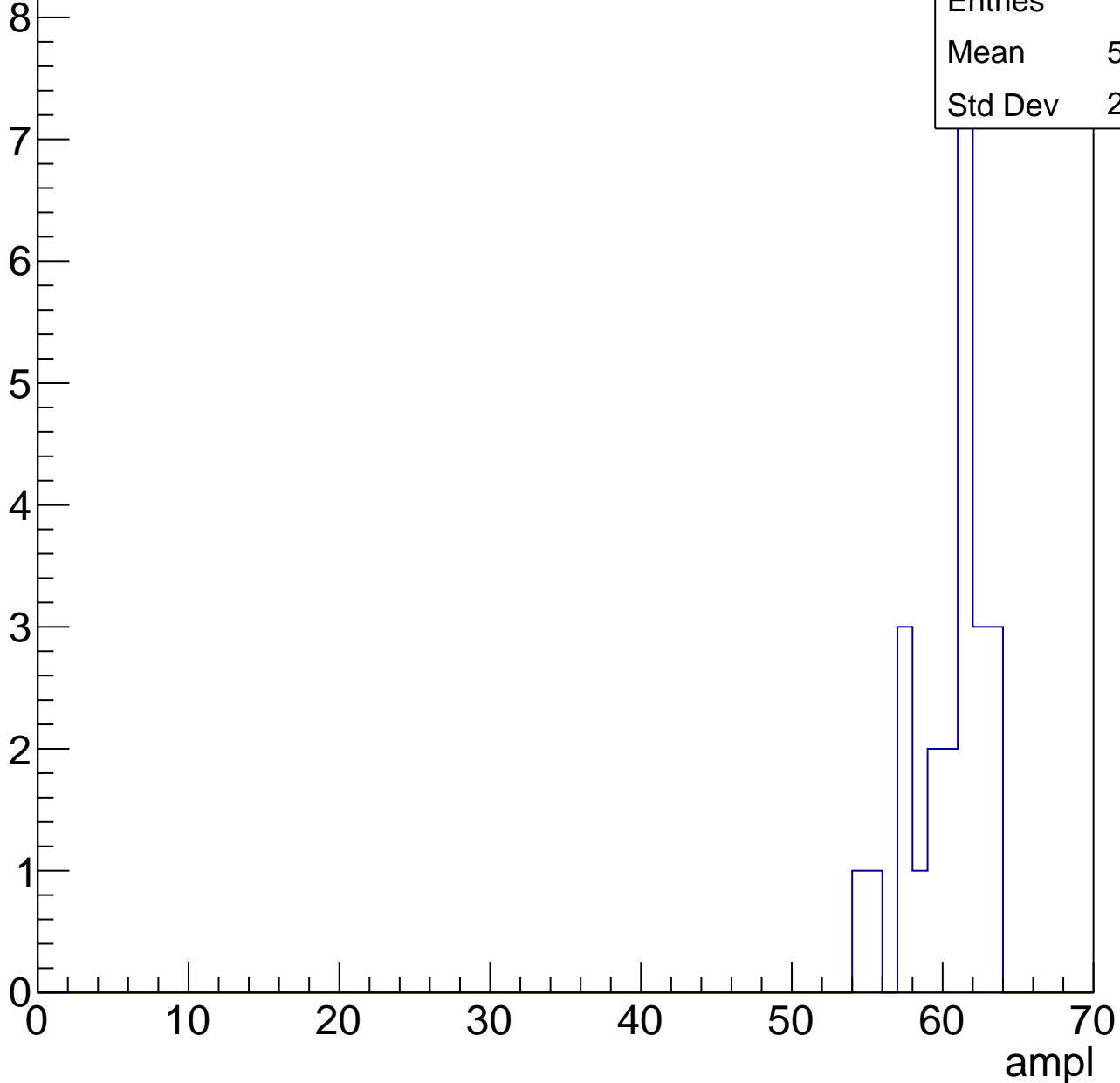


# B1L101S, U22-ch126, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	24
Mean	59.96
Std Dev	2.423



# B1L101S, U22-ch126, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

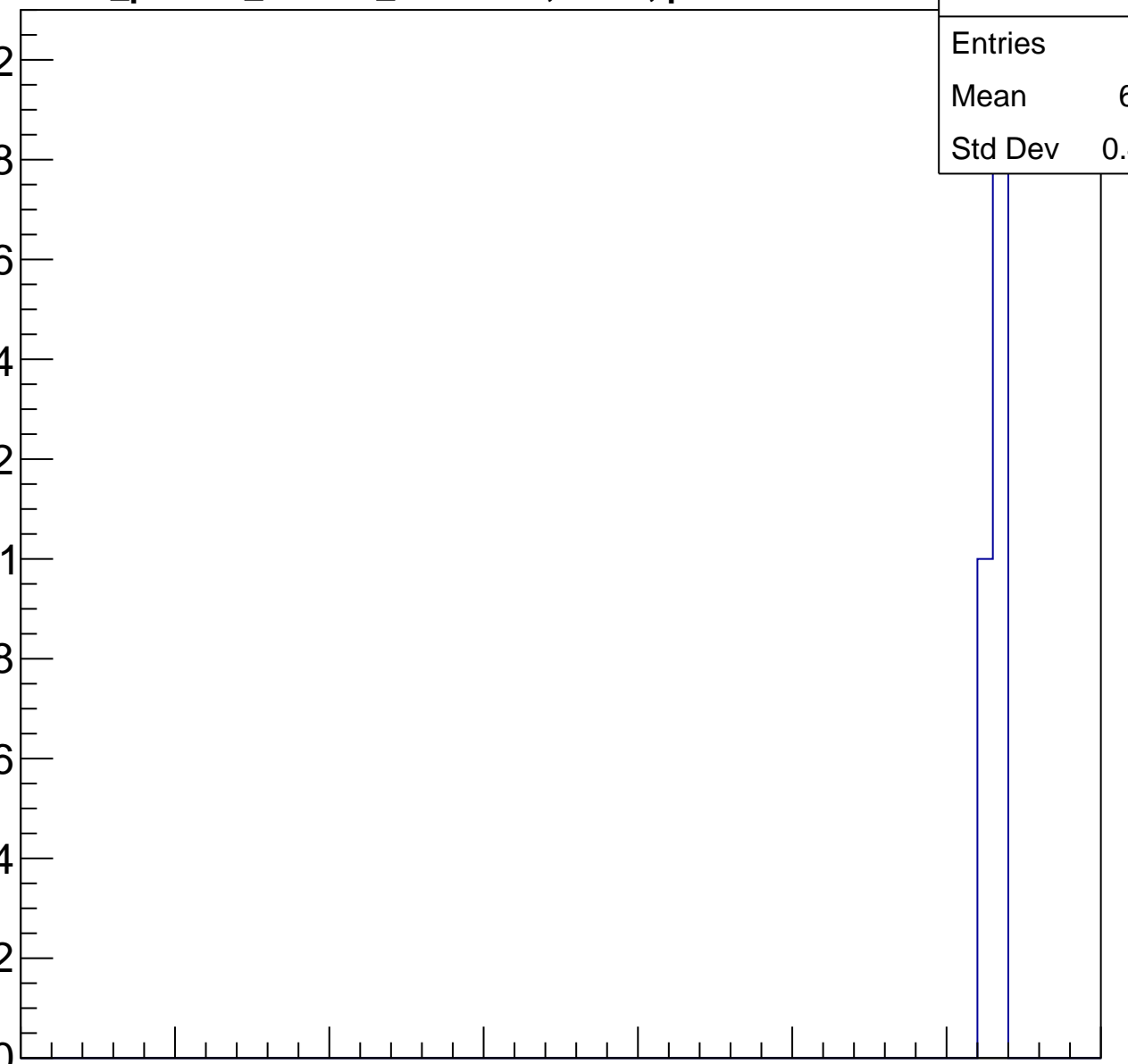
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	3
Mean	62.67
Std Dev	0.4714

ampl

0 10 20 30 40 50 60 70





# B1L101S, U22-ch126, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L101S, U22-ch127, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	84
Mean	30.49
Std Dev	4.802

**Gaus mean : 31.4726**

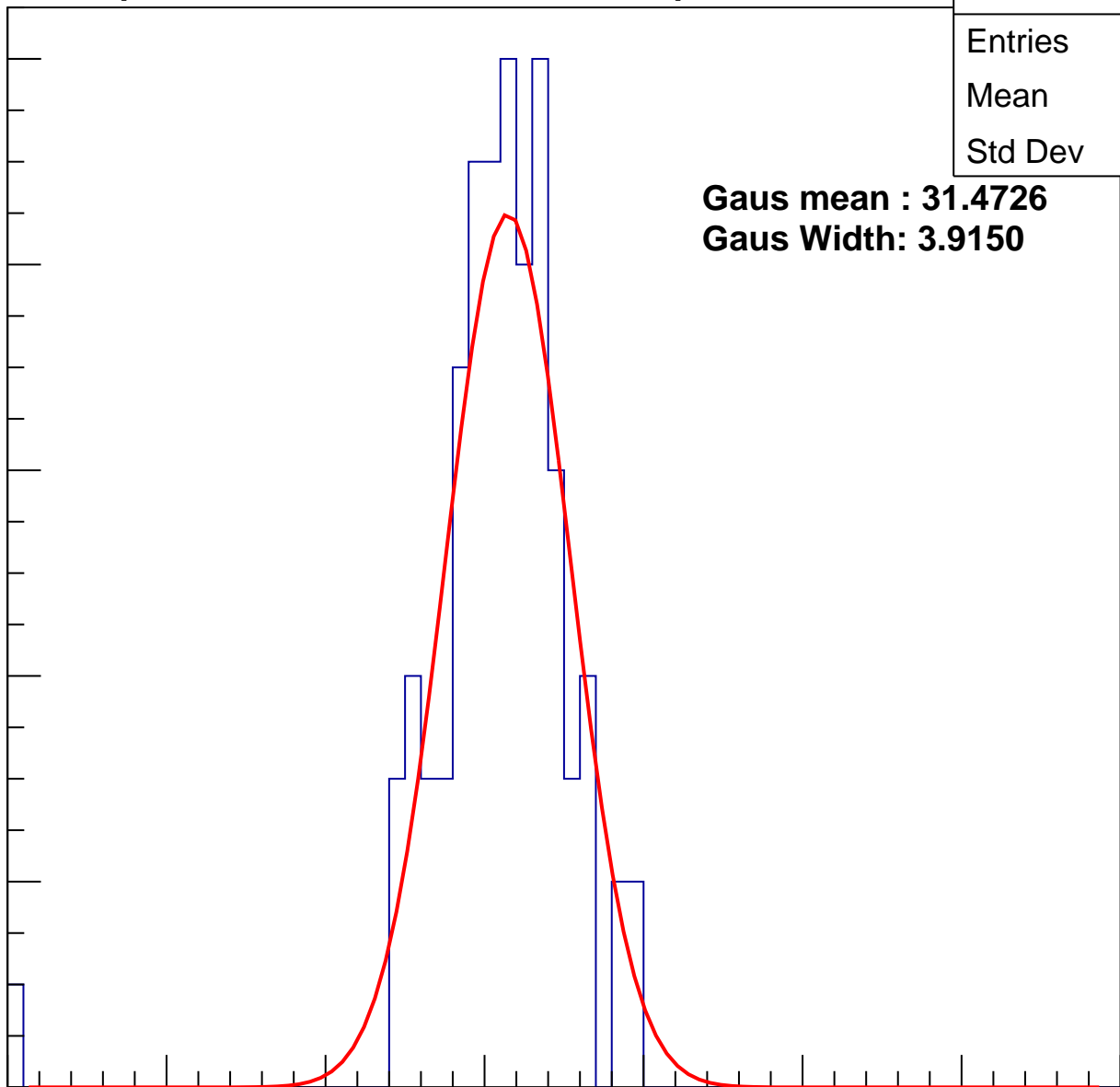
**Gaus Width: 3.9150**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U22-ch127, adc1

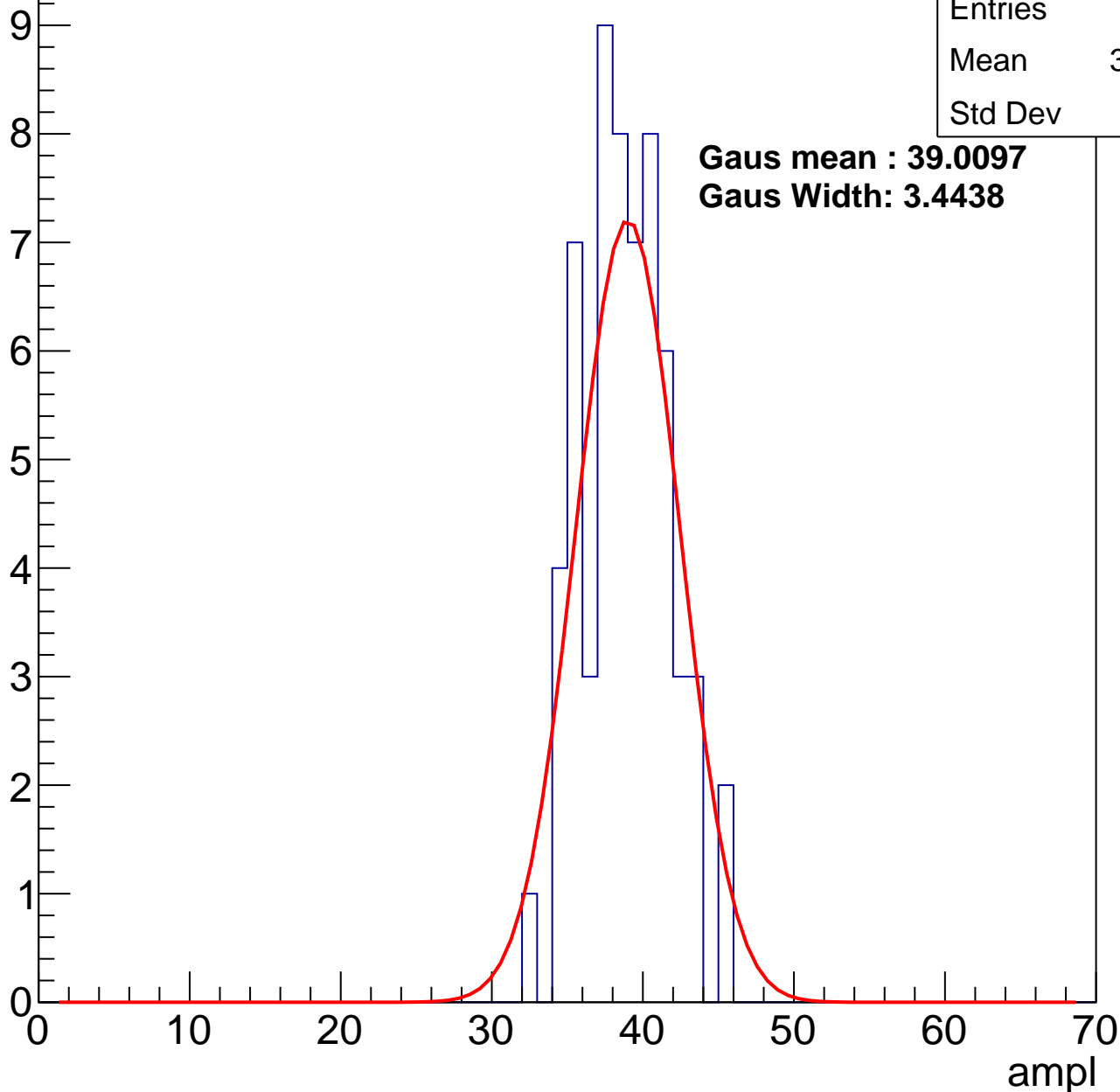
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	38.39
Std Dev	2.83

**Gaus mean : 39.0097**

**Gaus Width: 3.4438**



# B1L101S, U22-ch127, adc2

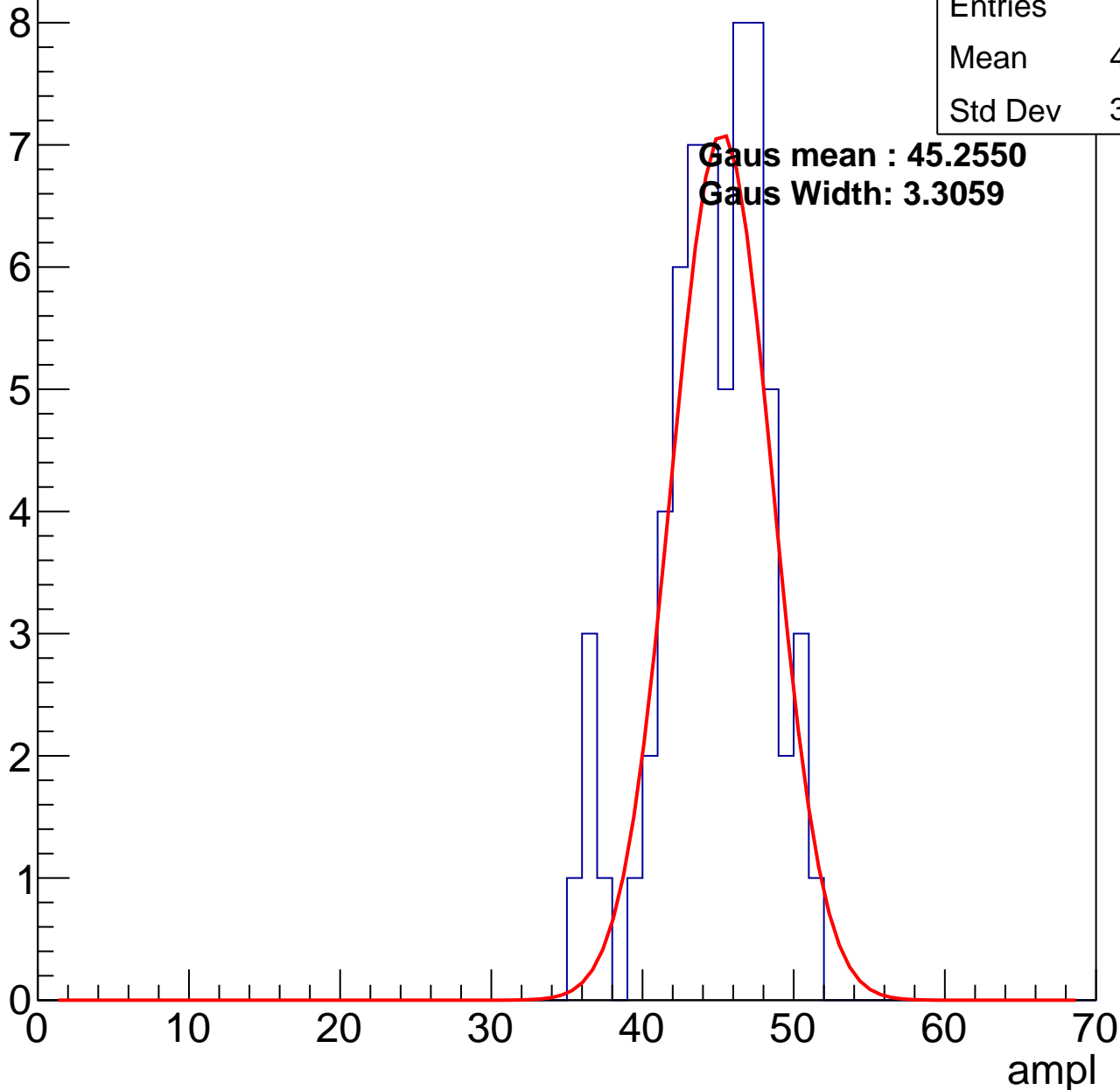
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	44.25
Std Dev	3.619

**Gaus mean : 45.2550**

**Gaus Width: 3.3059**

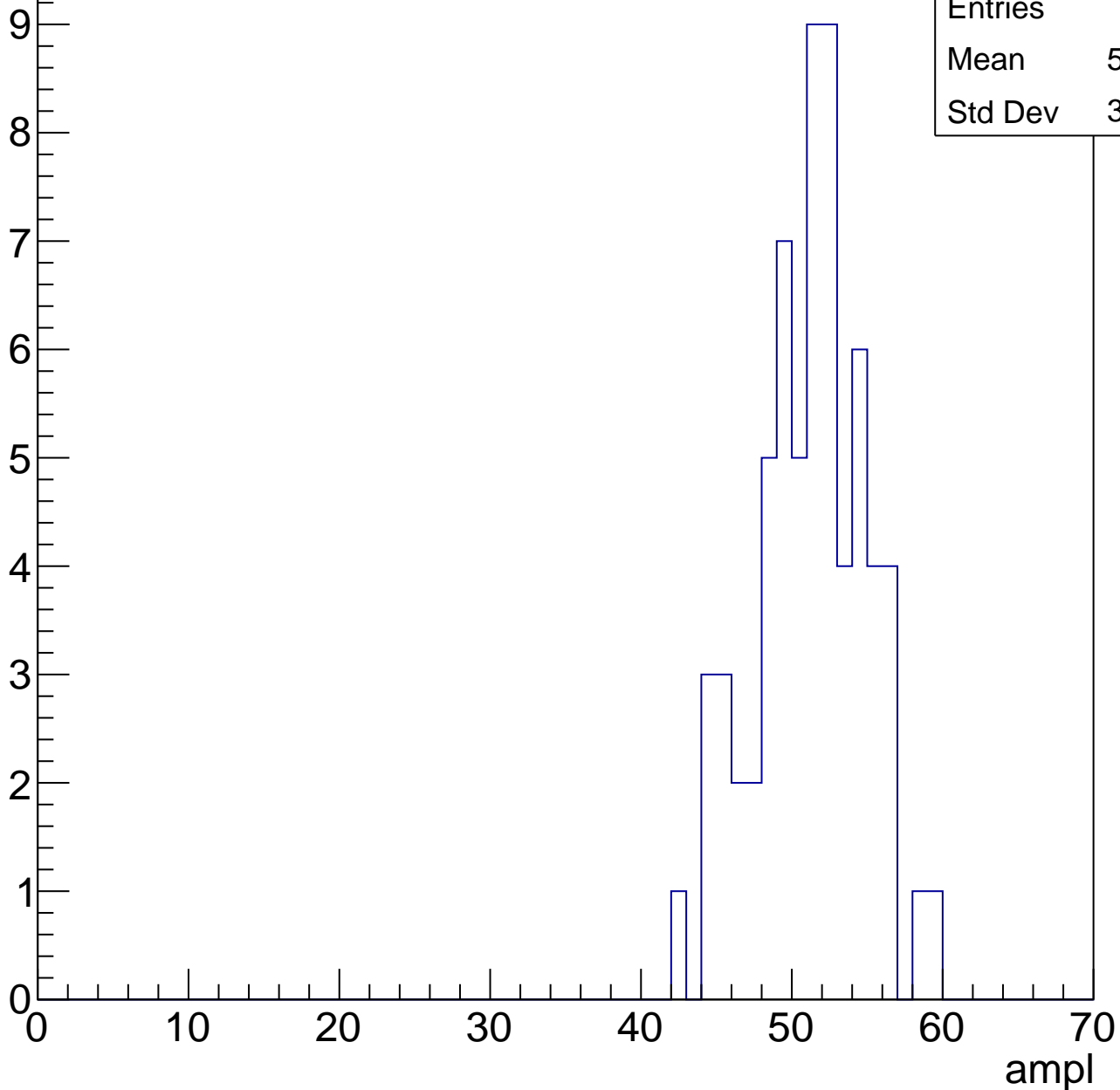


# B1L101S, U22-ch127, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

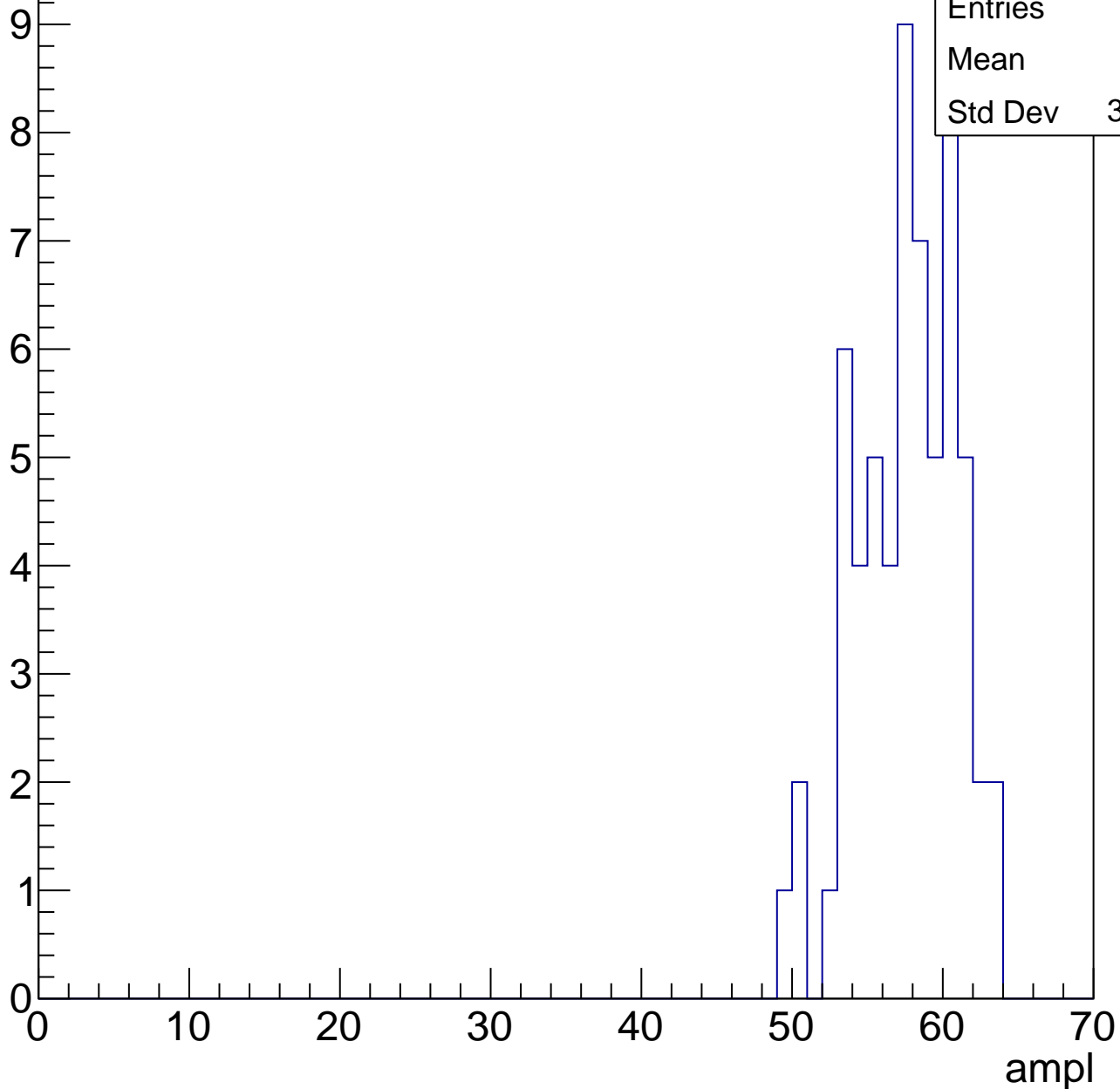
Entries	66
Mean	50.79
Std Dev	3.587



# B1L101S, U22-ch127, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

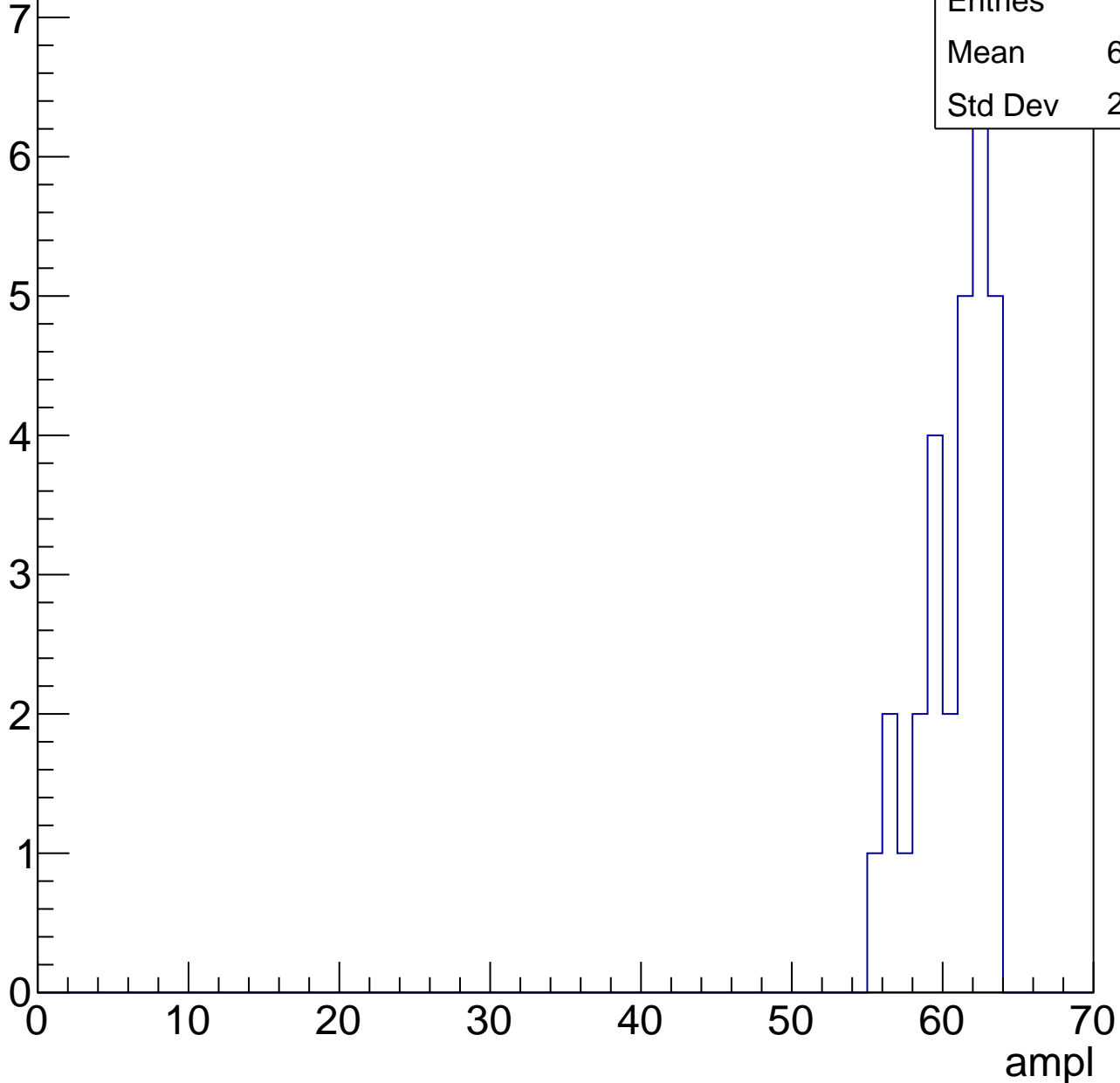


# B1L101S, U22-ch127, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	29
Mean	60.34
Std Dev	2.294



# B1L101S, U22-ch127, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U22-ch127, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

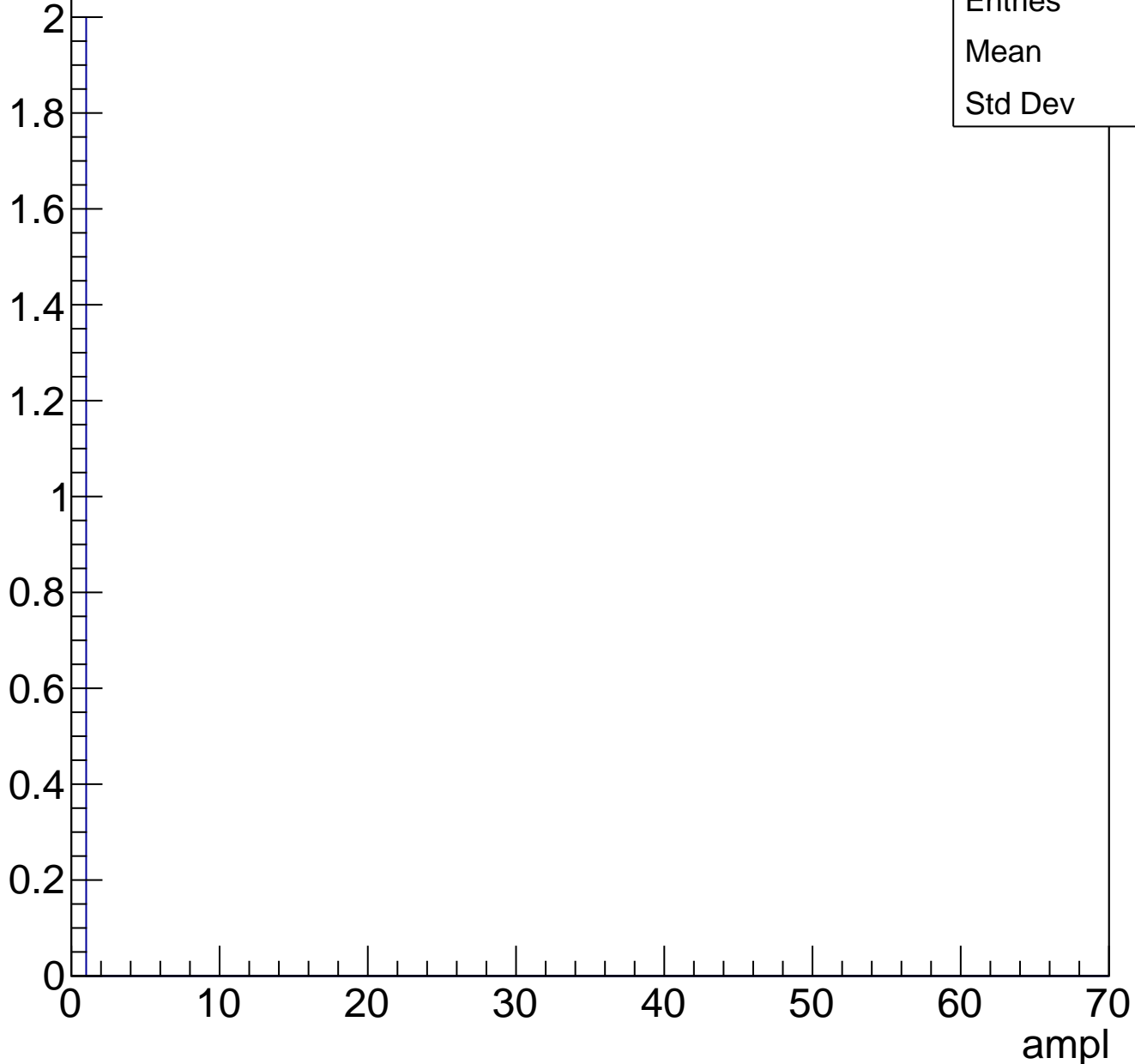


Entries	2
Mean	0
Std Dev	0

# B1L101S, U22-ch127, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	2
Mean	0
Std Dev	0