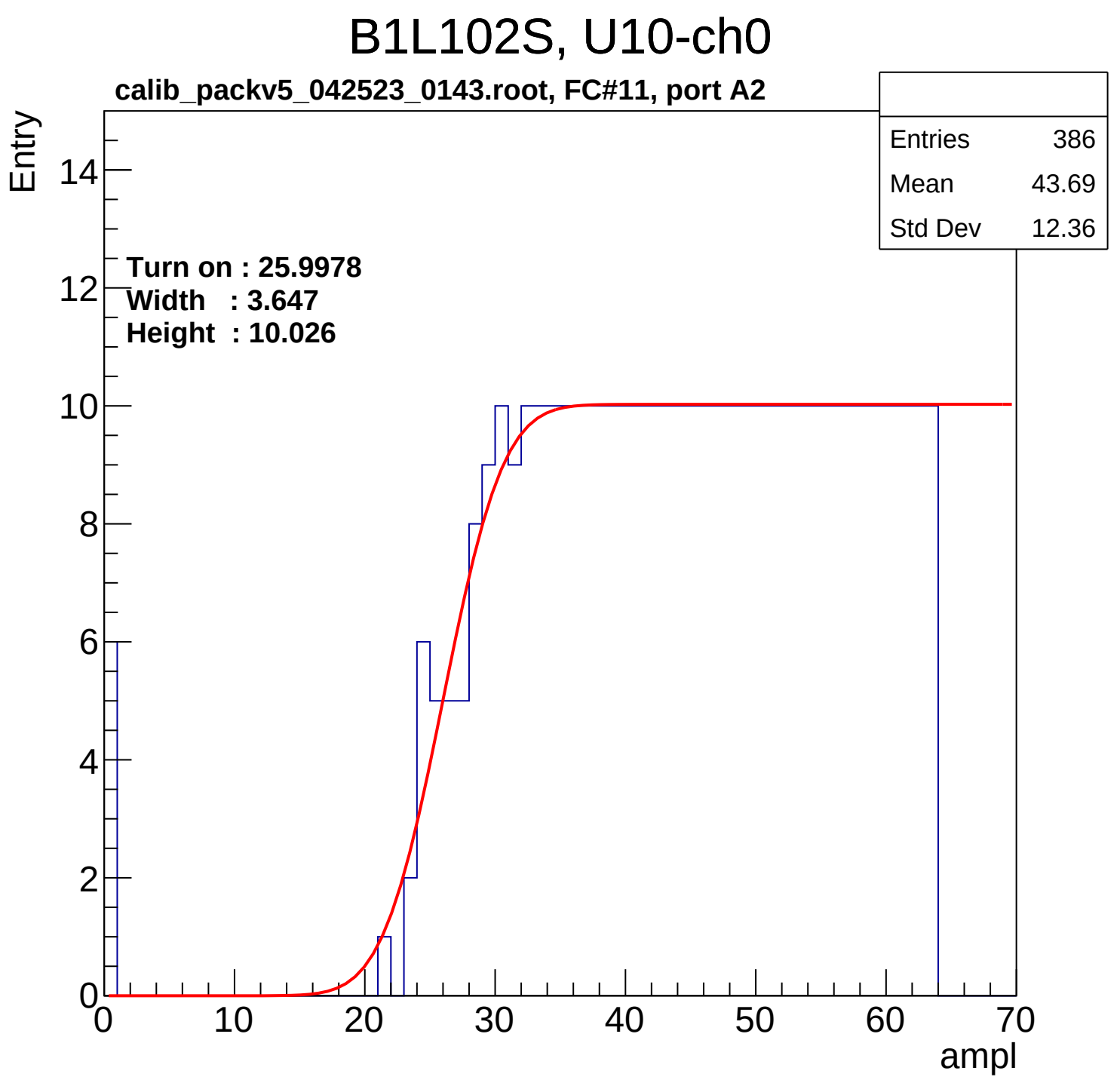
B1L102S, U10-ch0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 386
Mean 43.69
Std Dev 12.36
Turn on : 25.9978
Width : 3.647
Height : 10.026
Entry
ampl
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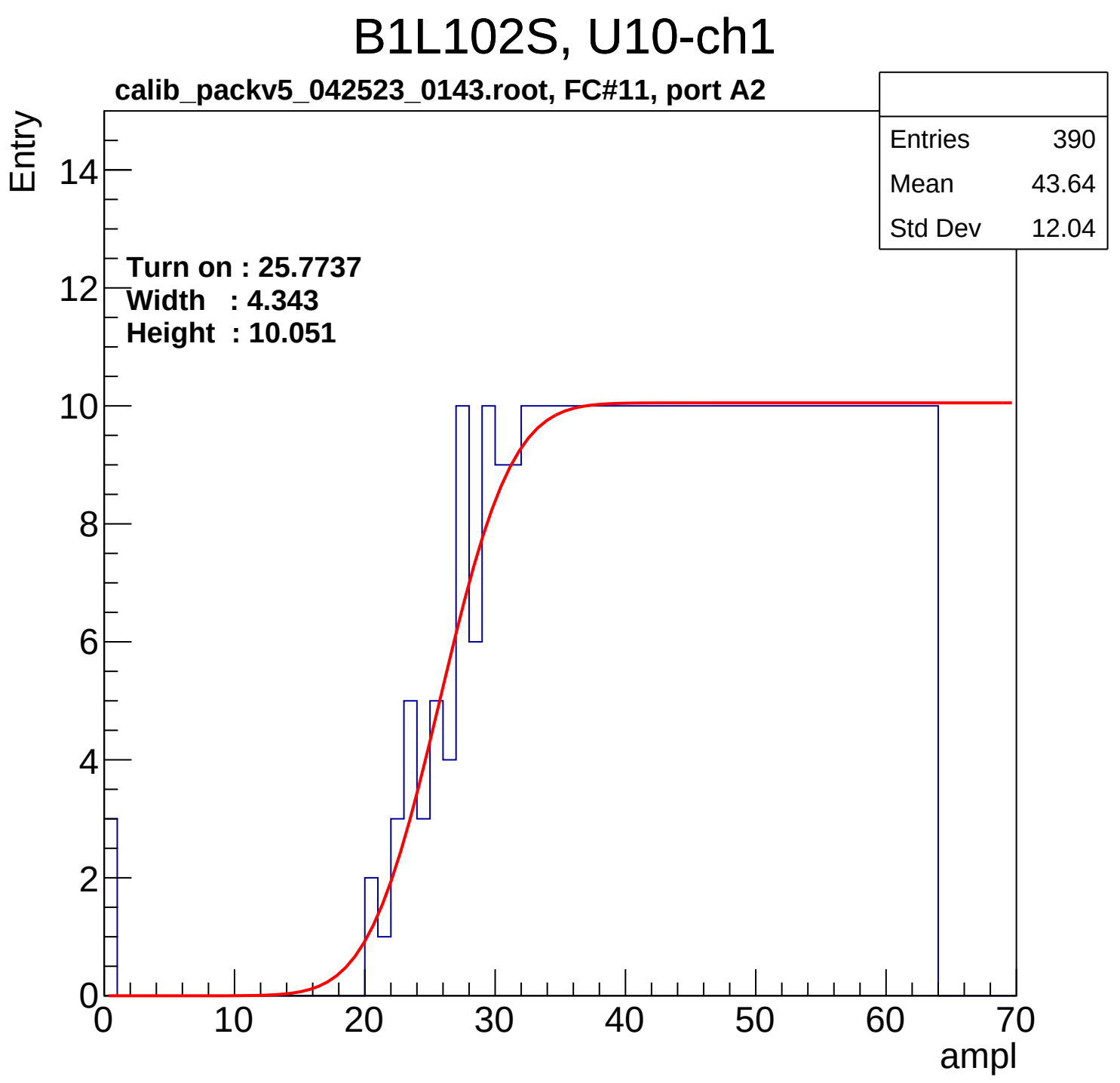
B1L102S, U10-ch1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 390
Mean 43.64
Std Dev 12.04
Turn on : 25.7737
Width : 4.343
Height : 10.051
Entry
ampl
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2
4
6
8
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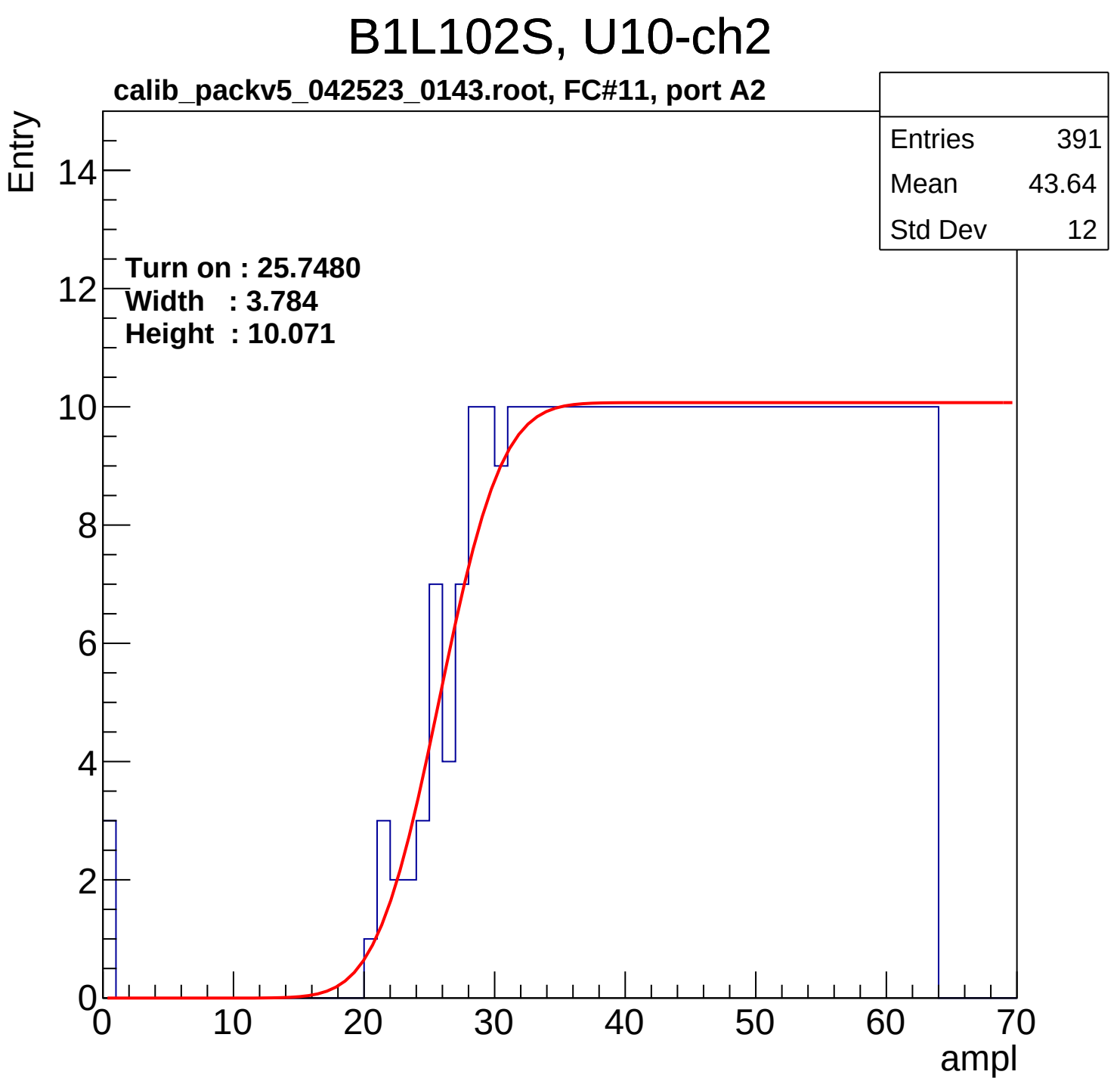
B1L102S, U10-ch2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 391
Mean 43.64
Std Dev 12
Turn on : 25.7480
Width : 3.784
Height : 10.071
Entry
ampl
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2
4
6
8
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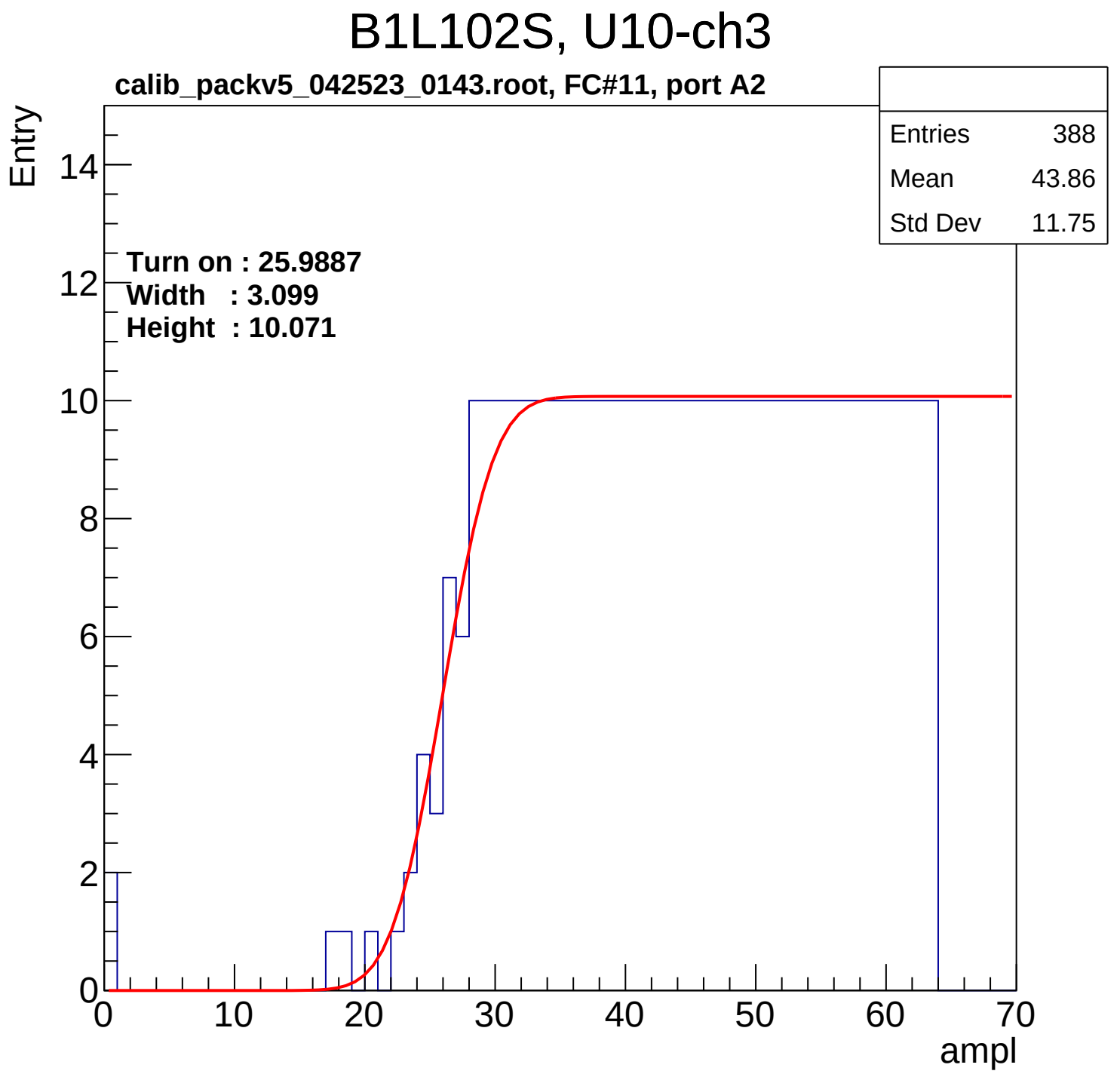
B1L102S, U10-ch3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 388
Mean 43.86
Std Dev 11.75
Turn on : 25.9887
Width : 3.099
Height : 10.071
Entry
ampl
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8
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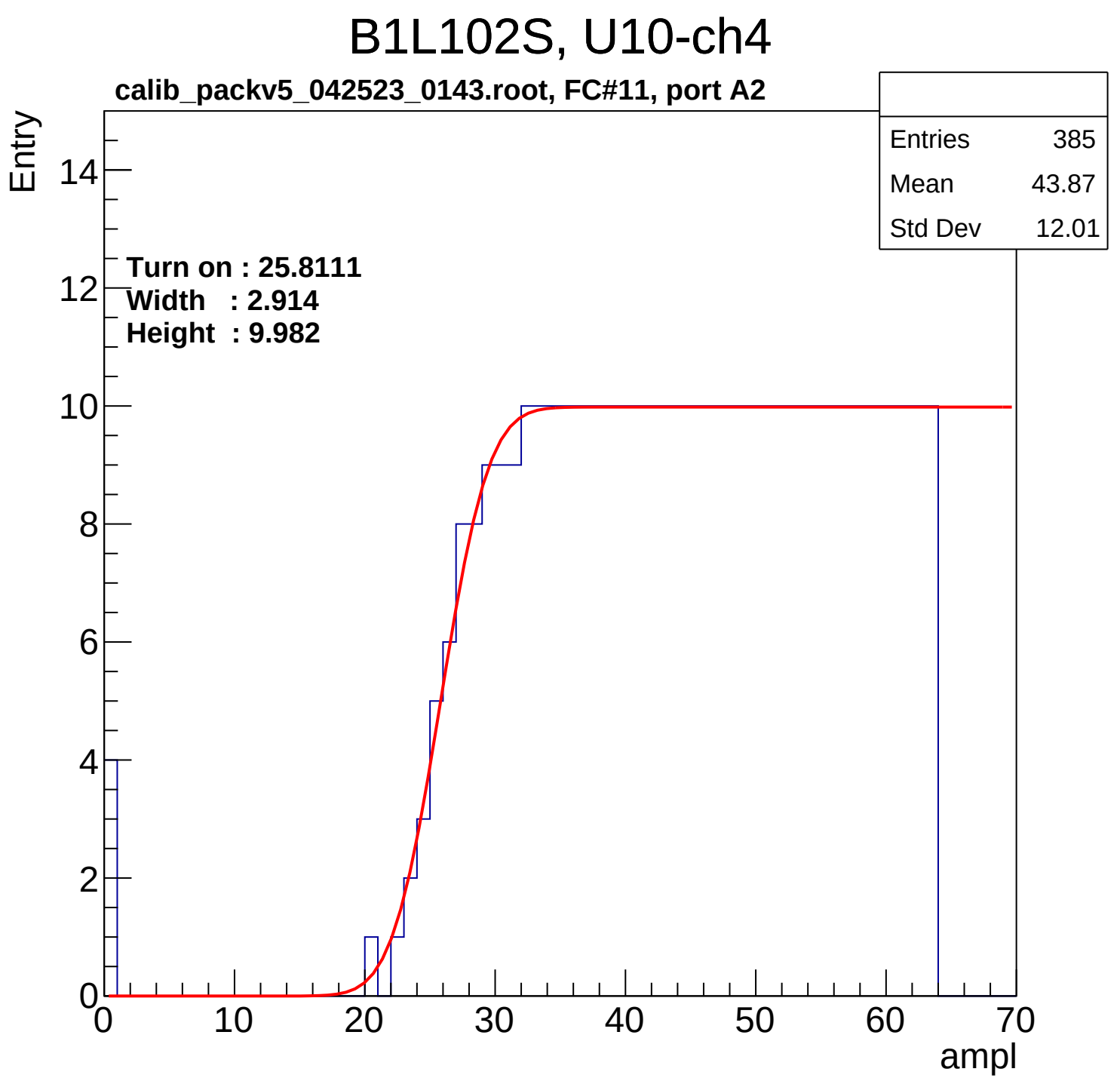
B1L102S, U10-ch4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 385
Mean 43.87
Std Dev 12.01
Turn on : 25.8111
Width : 2.914
Height : 9.982
Entry
ampl
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2
4
6
8
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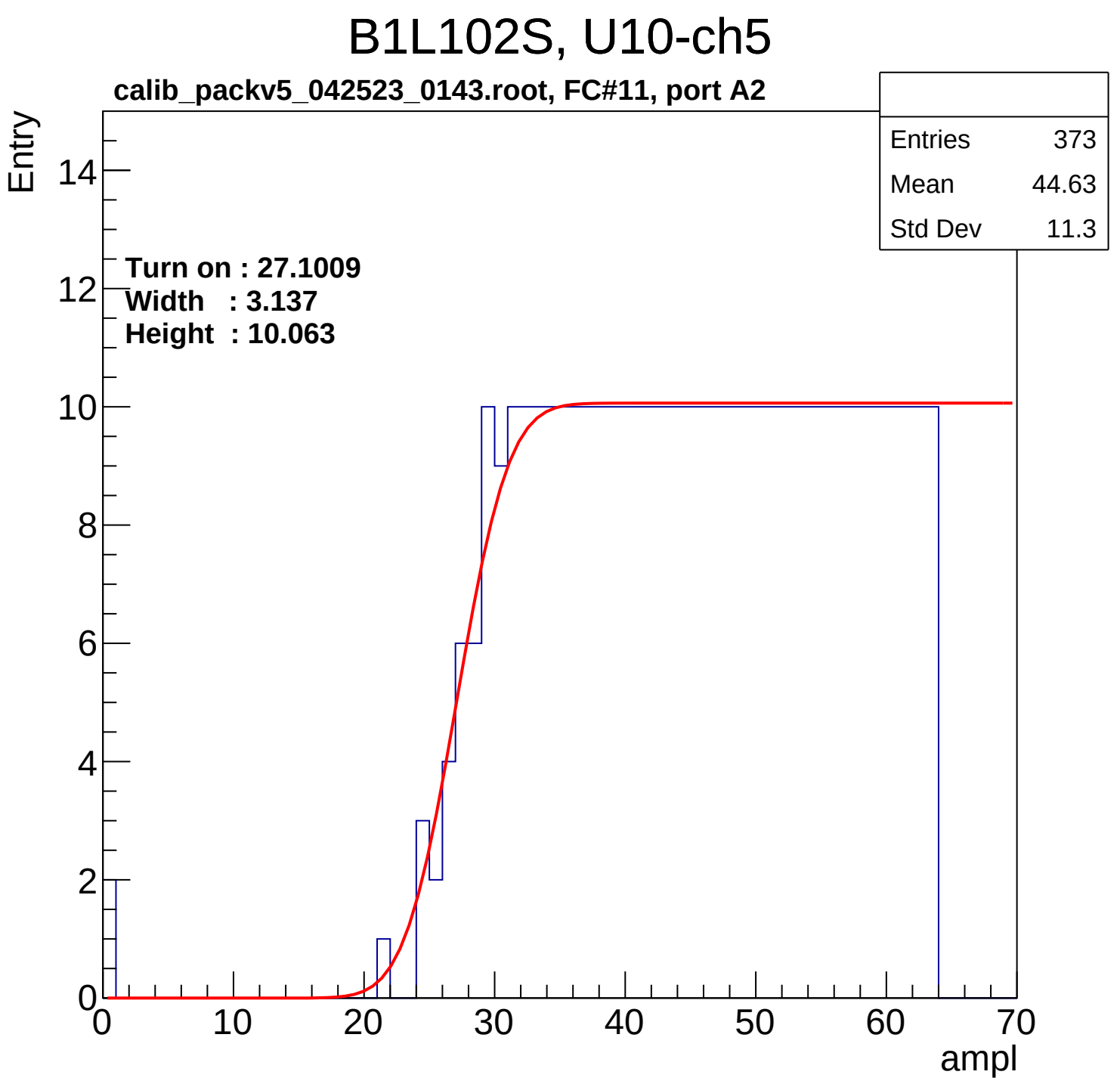
B1L102S, U10-ch5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 373
Mean 44.63
Std Dev 11.3
Turn on : 27.1009
Width : 3.137
Height : 10.063
Entry
ampl
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2
4
6
8
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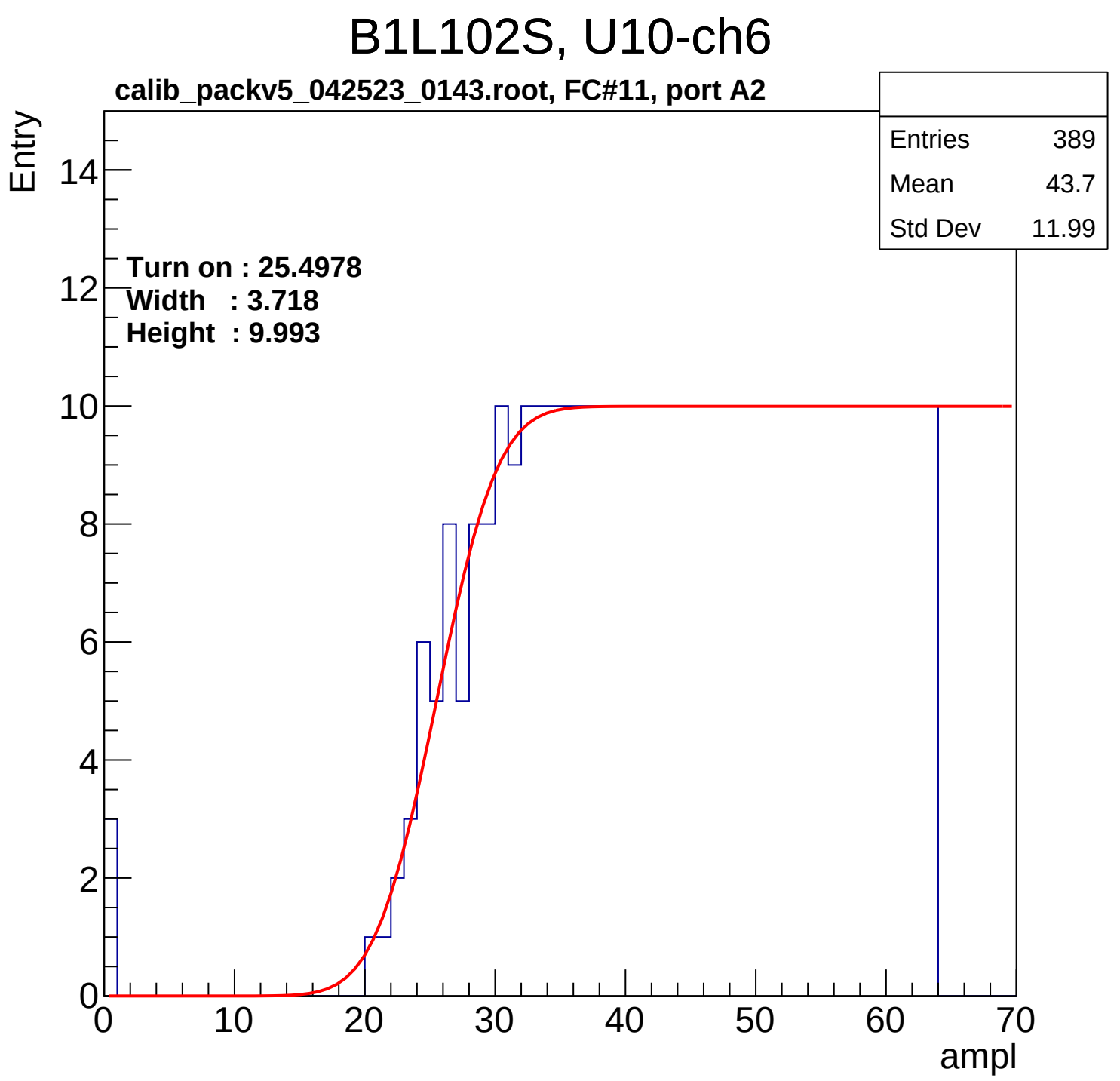
B1L102S, U10-ch6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 389
Mean 43.7
Std Dev 11.99
Turn on : 25.4978
Width : 3.718
Height : 9.993
Entry
ampl
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4
6
8
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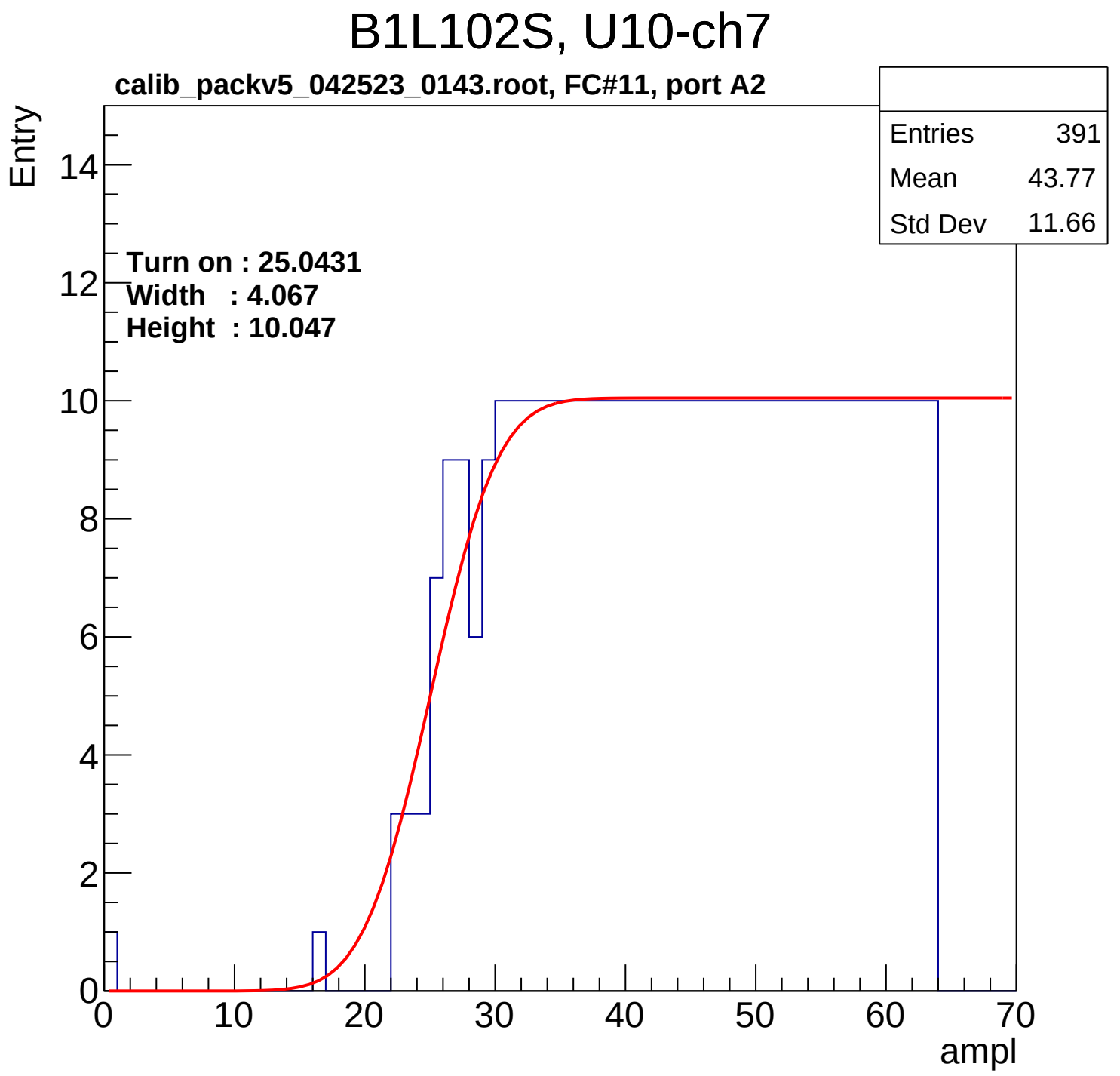
B1L102S, U10-ch7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 391
Mean 43.77
Std Dev 11.66
Turn on : 25.0431
Width : 4.067
Height : 10.047
Entry
ampl
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2
4
6
8
10
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60
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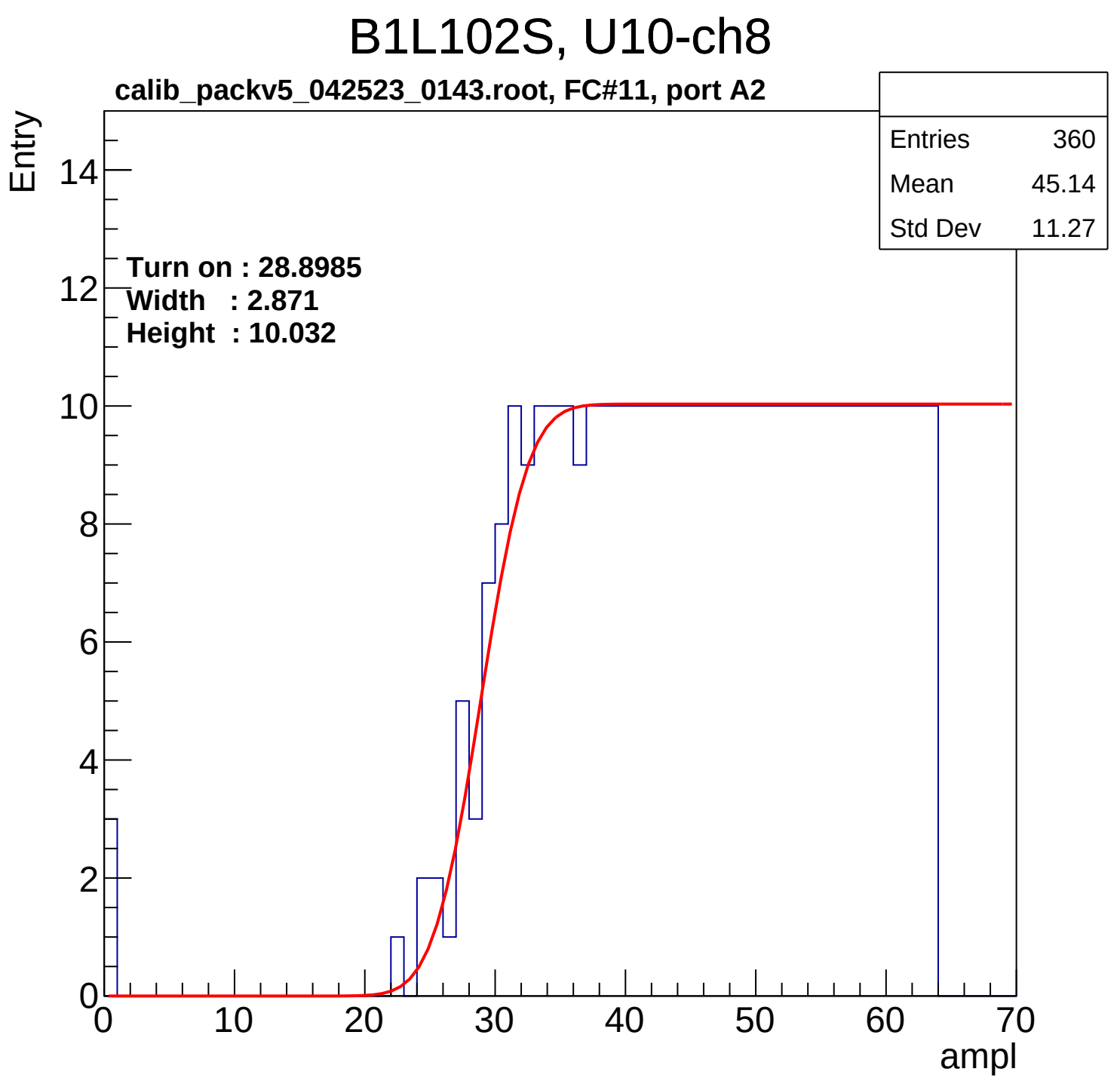
B1L102S, U10-ch8
calib_packv5_042523_0143.root, FC#11, port A2
Entries 360
Mean 45.14
Std Dev 11.27
Turn on : 28.8985
Width : 2.871
Height : 10.032
Entry
ampl
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6
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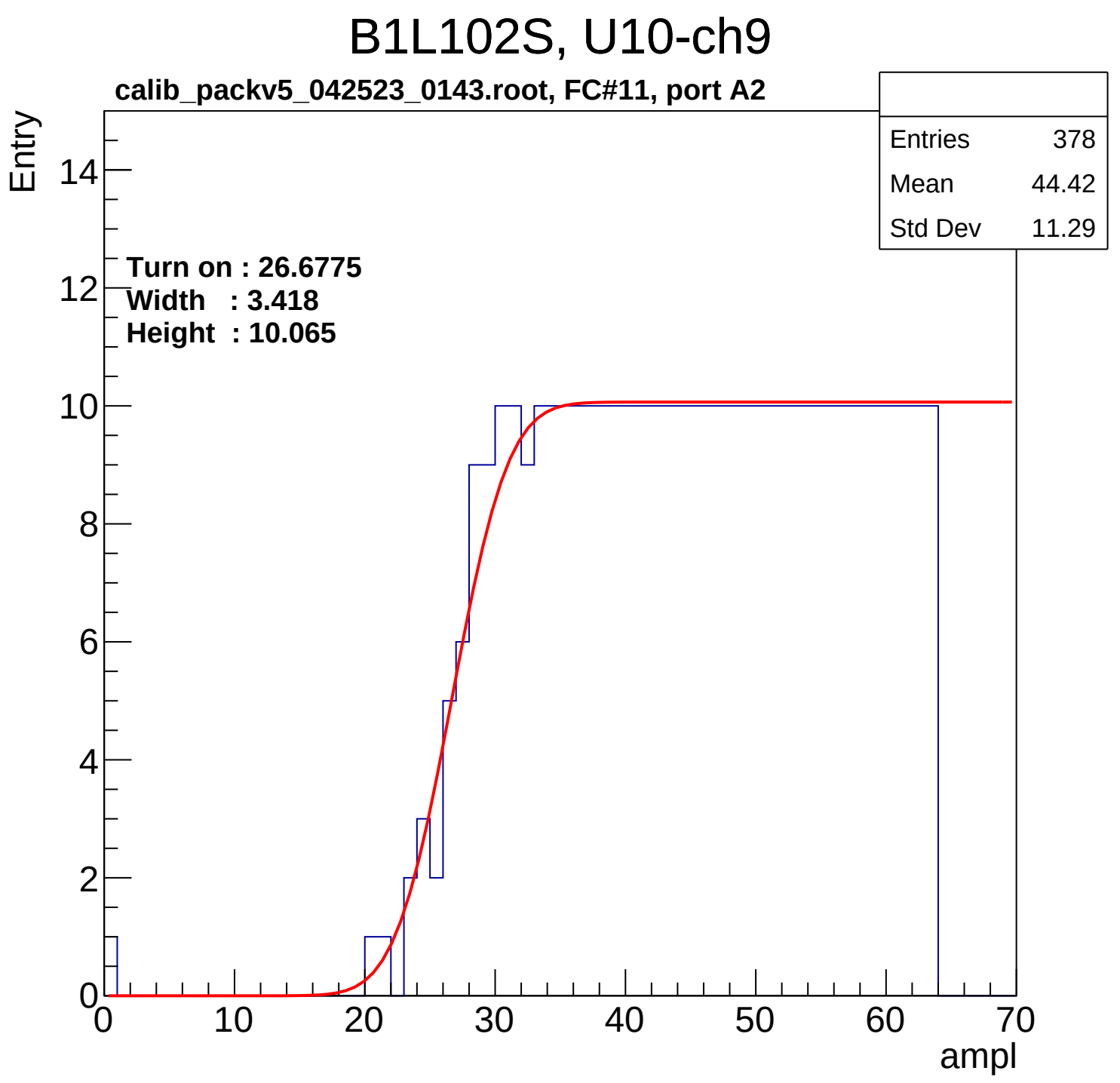
B1L102S, U10-ch9
calib_packv5_042523_0143.root, FC#11, port A2
Entries 378
Mean 44.42
Std Dev 11.29
Turn on : 26.6775
Width : 3.418
Height : 10.065
Entry
ampl
0
2
4
6
8
10
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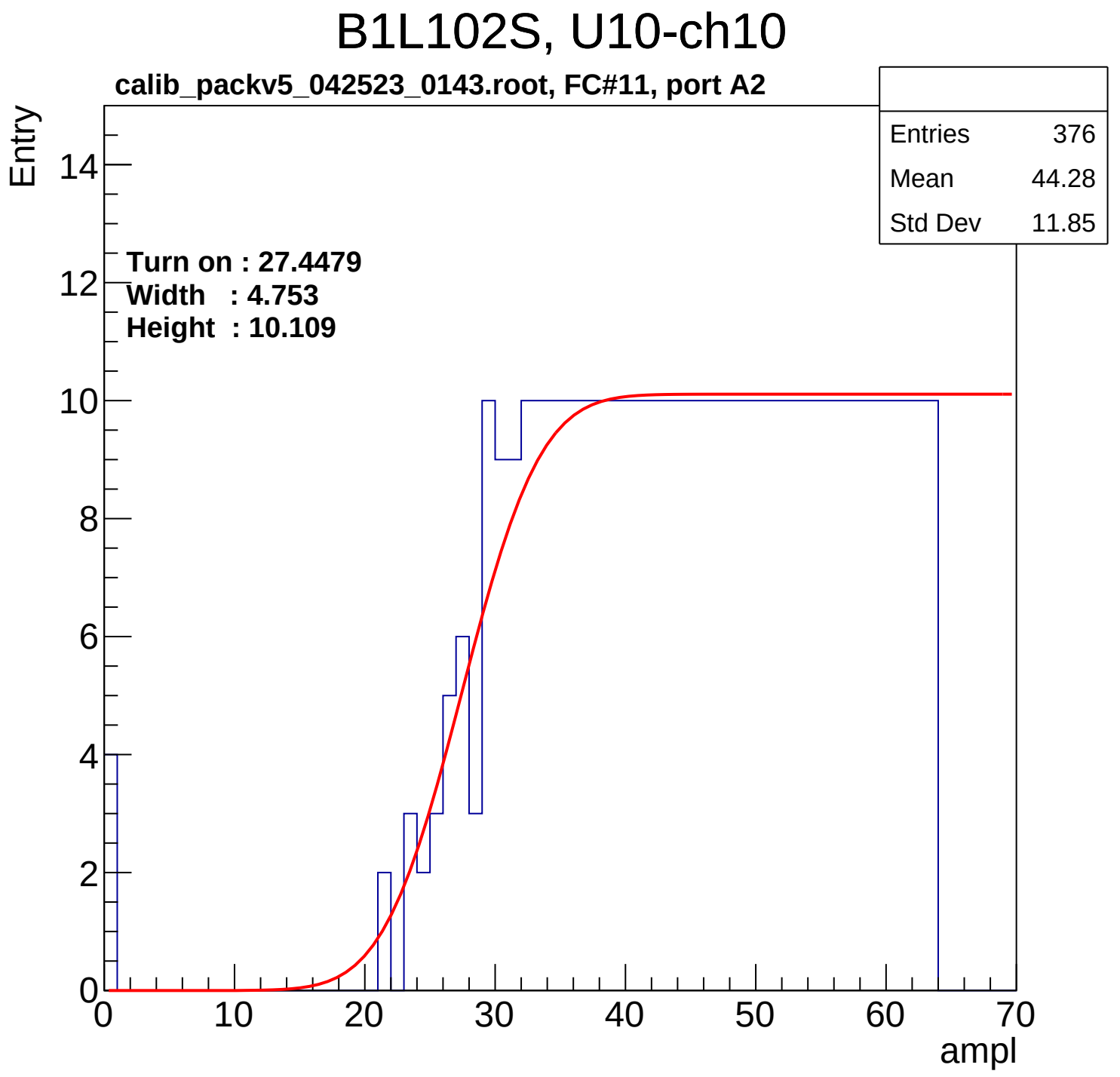
B1L102S, U10-ch10
calib_packv5_042523_0143.root, FC#11, port A2
Entries 376
Mean 44.28
Std Dev 11.85
Turn on : 27.4479
Width : 4.753
Height : 10.109
Entry
ampl
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2
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6
8
10
12
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0
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20
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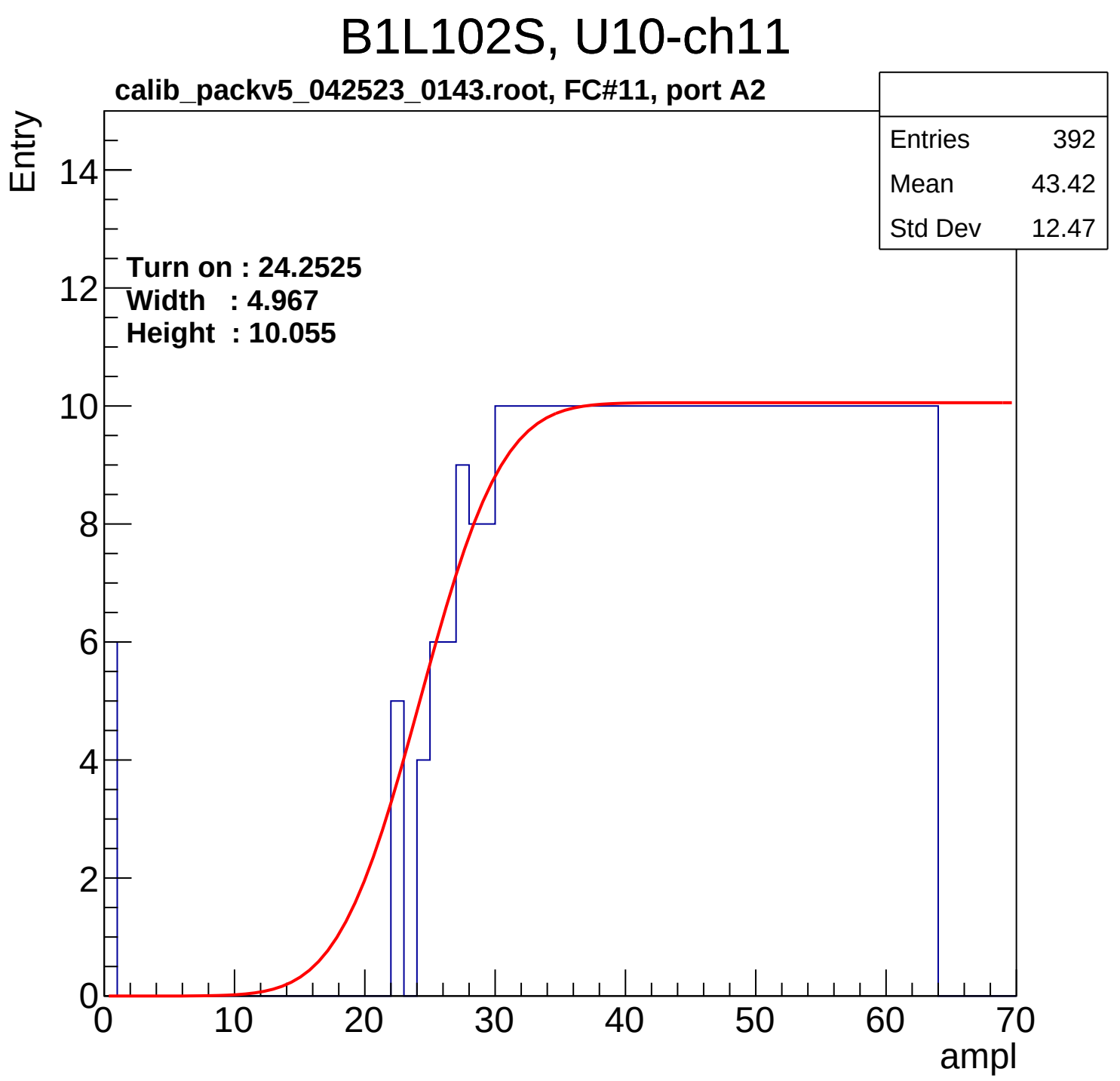
B1L102S, U10-ch11
calib_packv5_042523_0143.root, FC#11, port A2
Entries 392
Mean 43.42
Std Dev 12.47
Turn on : 24.2525
Width : 4.967
Height : 10.055
Entry
ampl
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2
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6
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10
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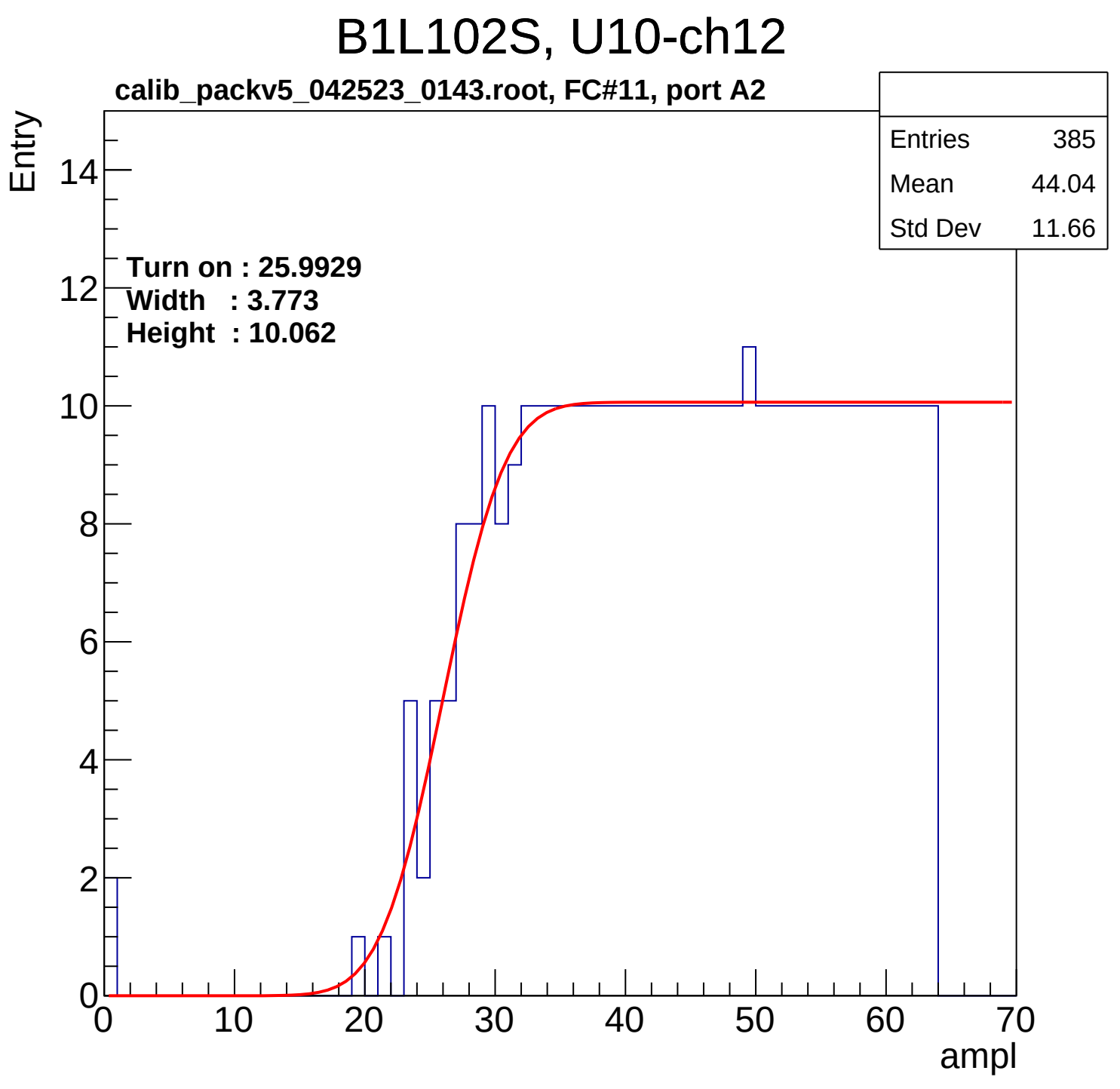
B1L102S, U10-ch12
calib_packv5_042523_0143.root, FC#11, port A2
Entries 385
Mean 44.04
Std Dev 11.66
Turn on : 25.9929
Width : 3.773
Height : 10.062
Entry
ampl
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2
4
6
8
10
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0
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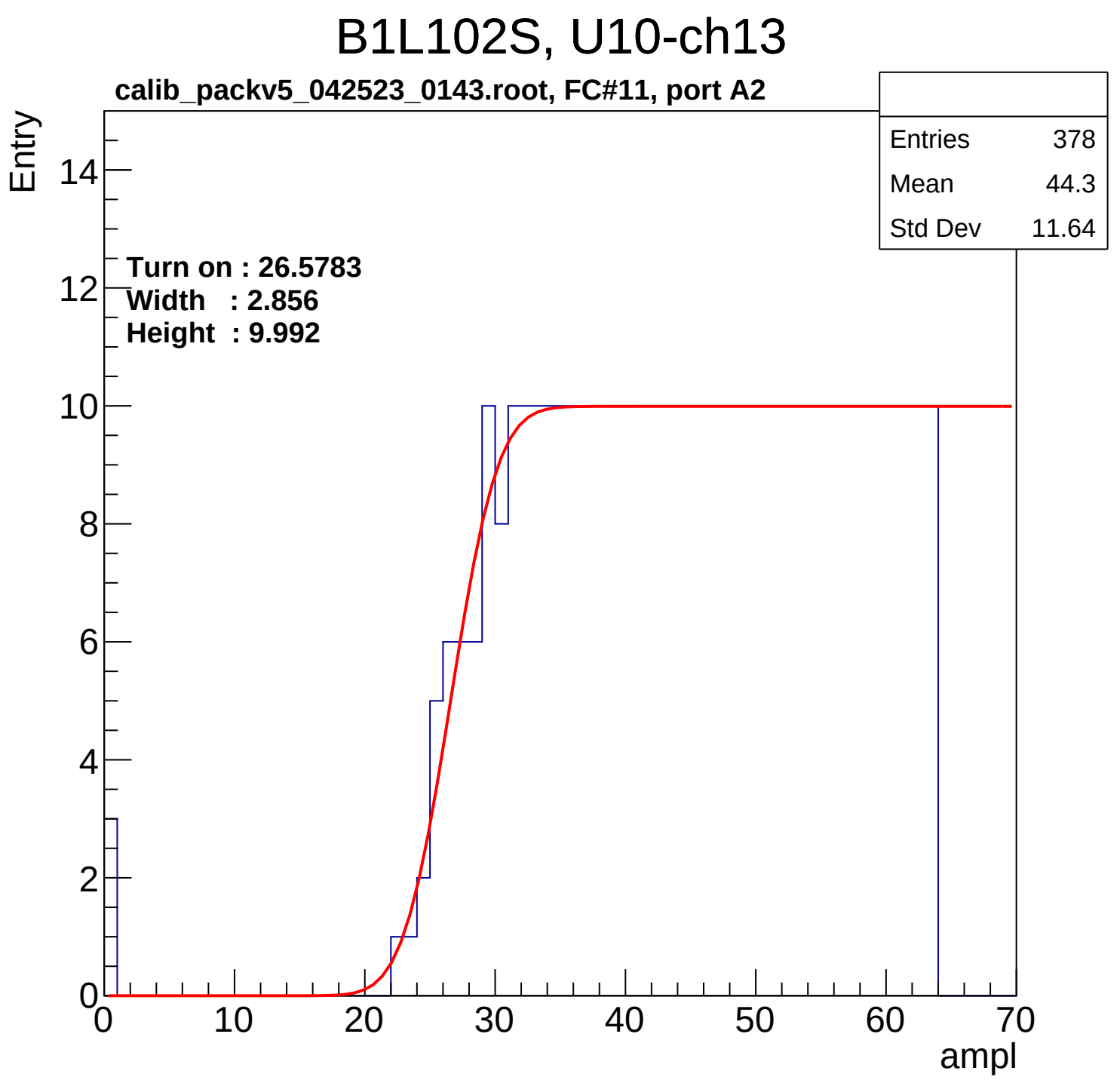
B1L102S, U10-ch13
calib_packv5_042523_0143.root, FC#11, port A2
Entries 378
Mean 44.3
Std Dev 11.64
Turn on : 26.5783
Width : 2.856
Height : 9.992
Entry
ampl
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2
4
6
8
10
12
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0
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60
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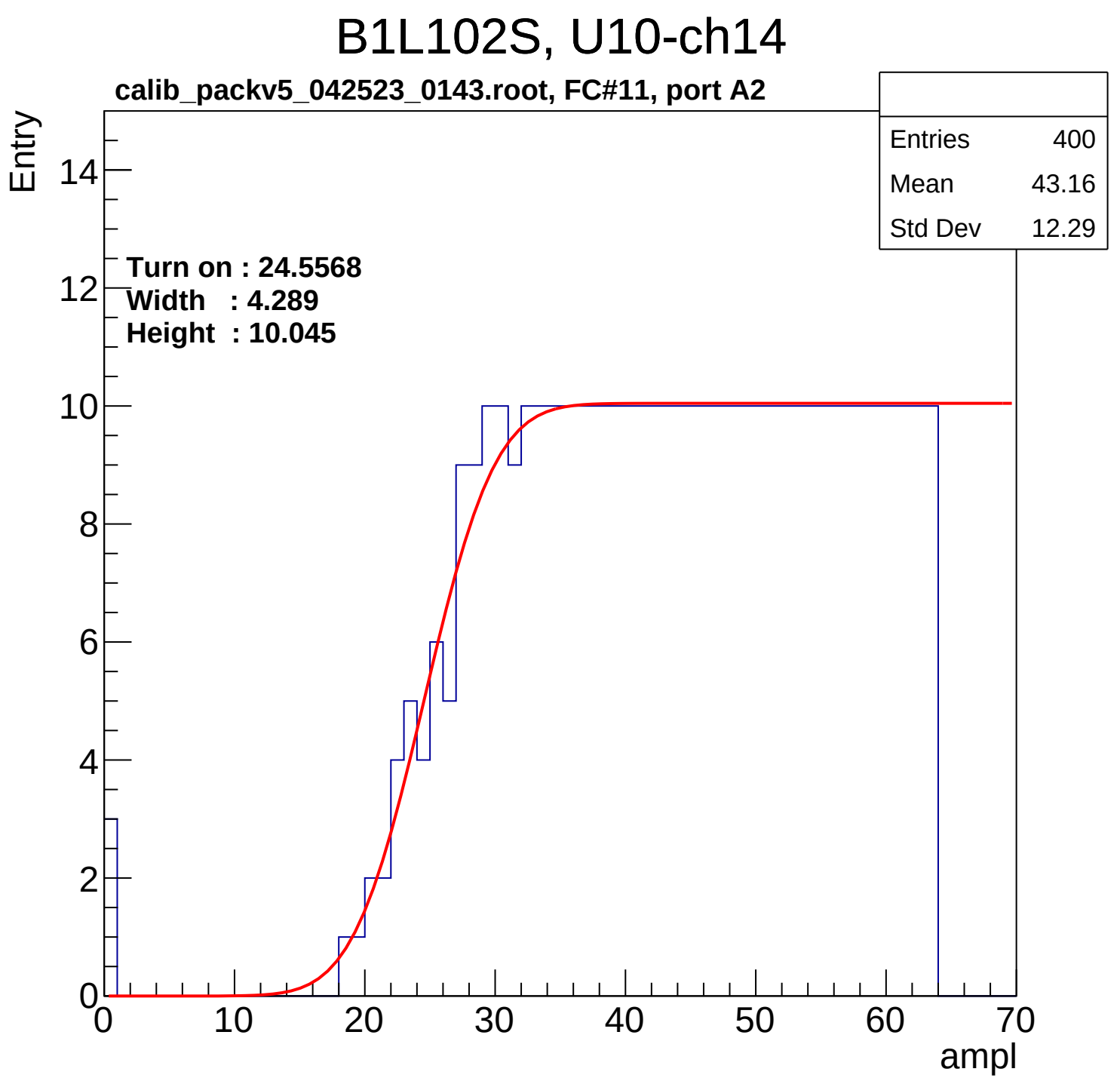
B1L102S, U10-ch14
calib_packv5_042523_0143.root, FC#11, port A2
Entries 400
Mean 43.16
Std Dev 12.29
Turn on : 24.5568
Width : 4.289
Height : 10.045
Entry
ampl
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6
8
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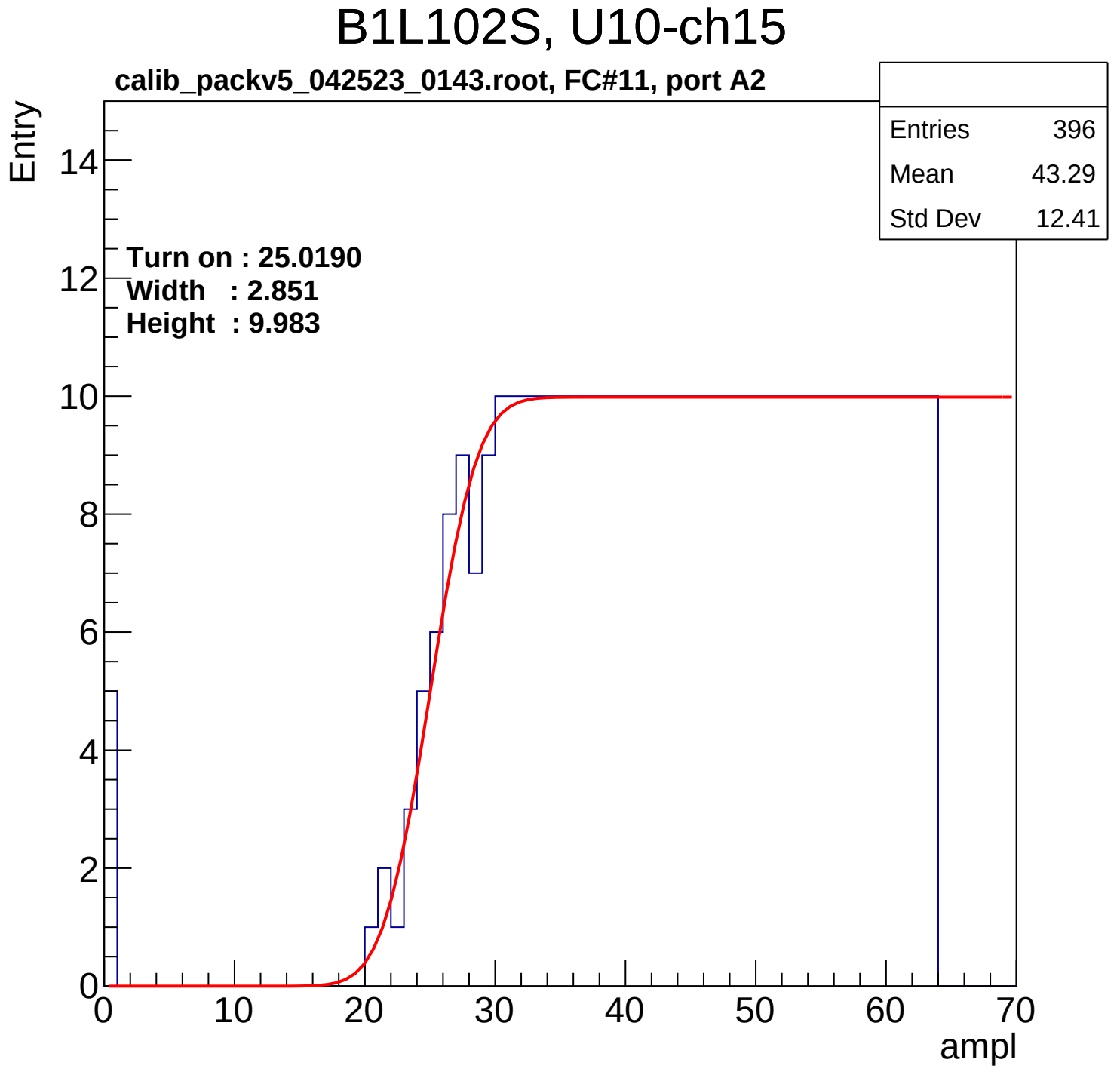
B1L102S, U10-ch15
calib_packv5_042523_0143.root, FC#11, port A2
Entries 396
Mean 43.29
Std Dev 12.41
Turn on : 25.0190
Width : 2.851
Height : 9.983
Entry
ampl
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2
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6
8
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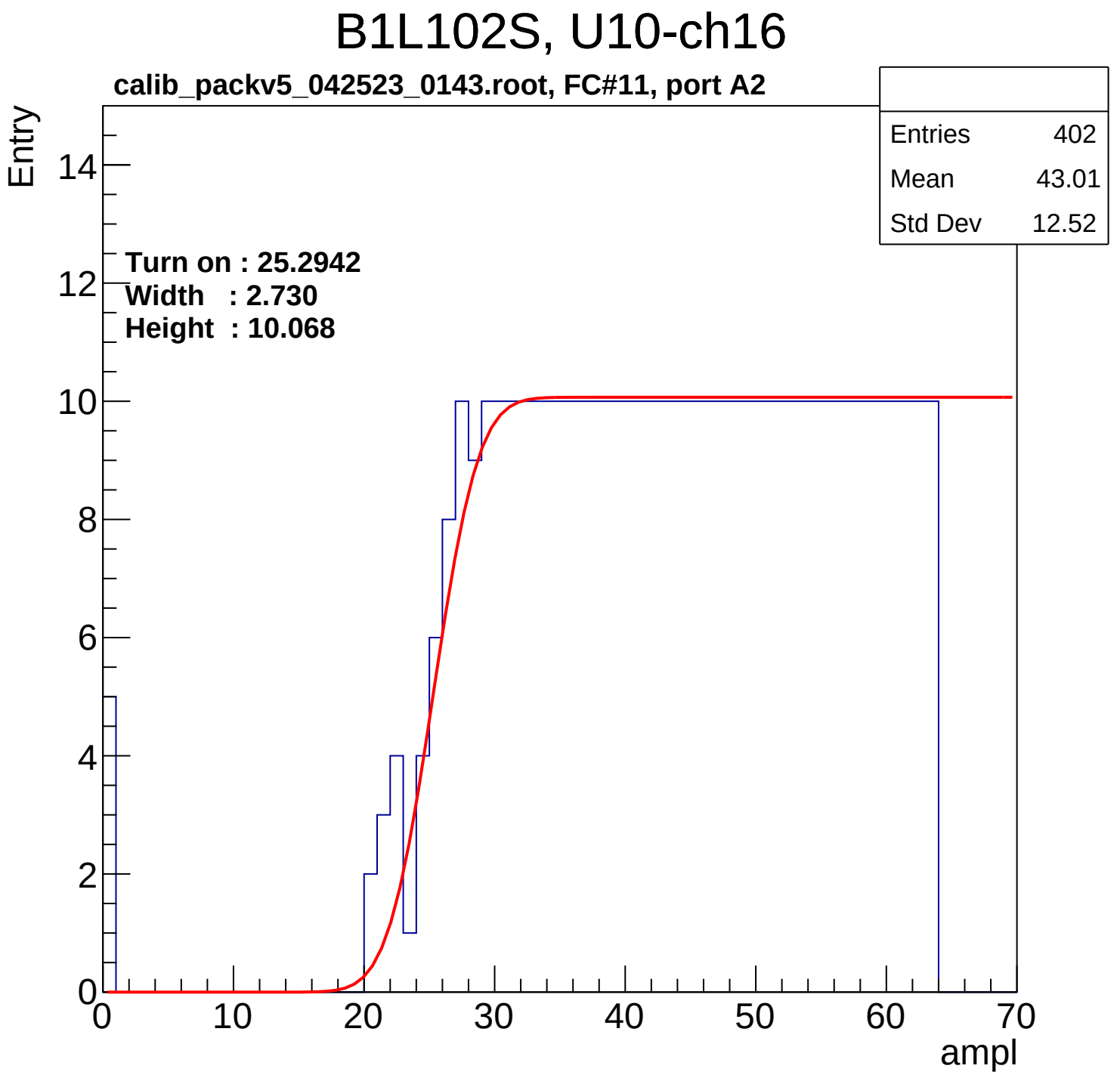
B1L102S, U10-ch16
calib_packv5_042523_0143.root, FC#11, port A2
Entries 402
Mean 43.01
Std Dev 12.52
Turn on : 25.2942
Width : 2.730
Height : 10.068
Entry
ampl
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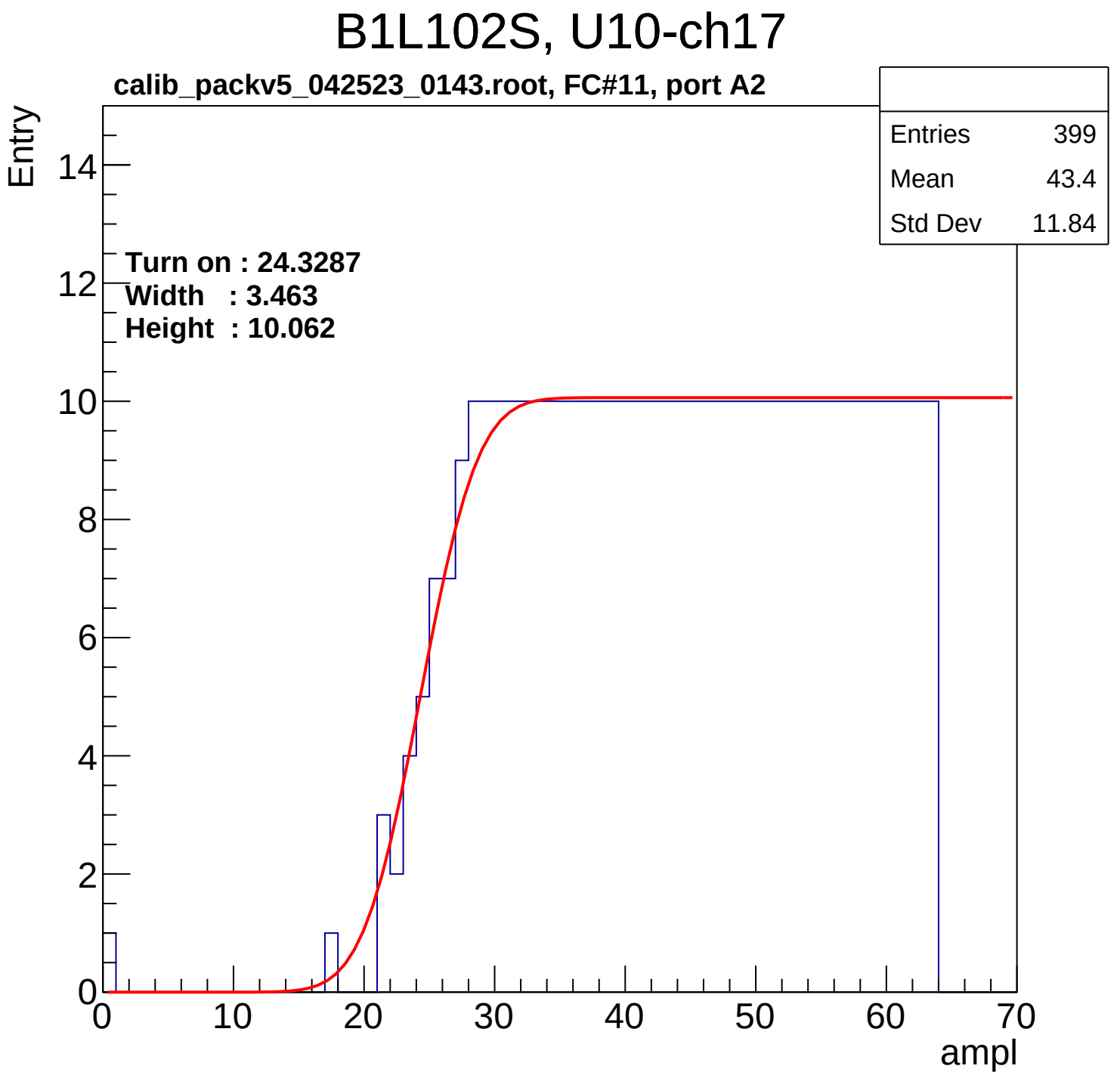
B1L102S, U10-ch17
calib_packv5_042523_0143.root, FC#11, port A2
Entries 399
Mean 43.4
Std Dev 11.84
Turn on : 24.3287
Width : 3.463
Height : 10.062
Entry
ampl
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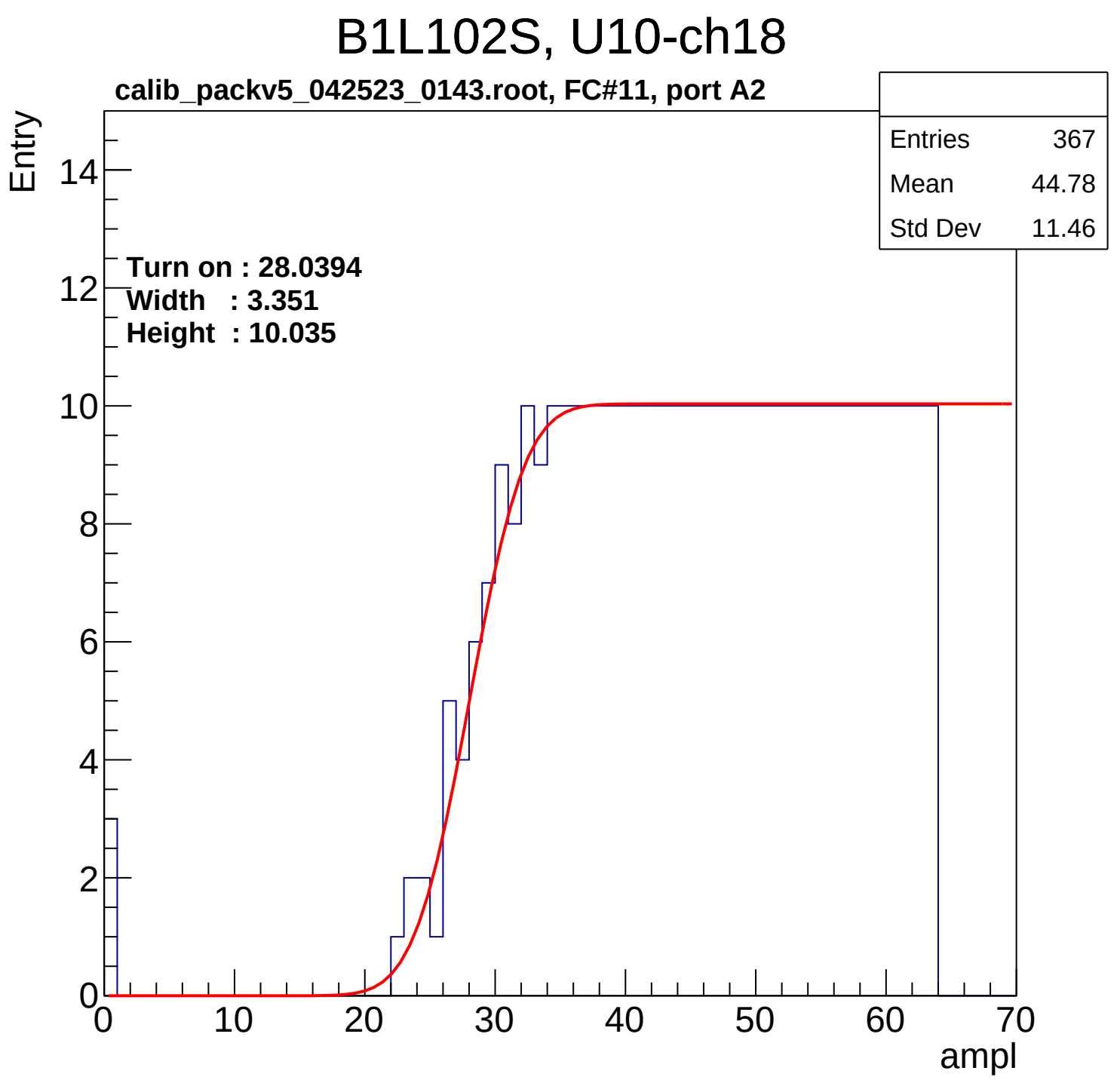
B1L102S, U10-ch18
calib_packv5_042523_0143.root, FC#11, port A2
Entries 367
Mean 44.78
Std Dev 11.46
Turn on : 28.0394
Width : 3.351
Height : 10.035
Entry
ampl
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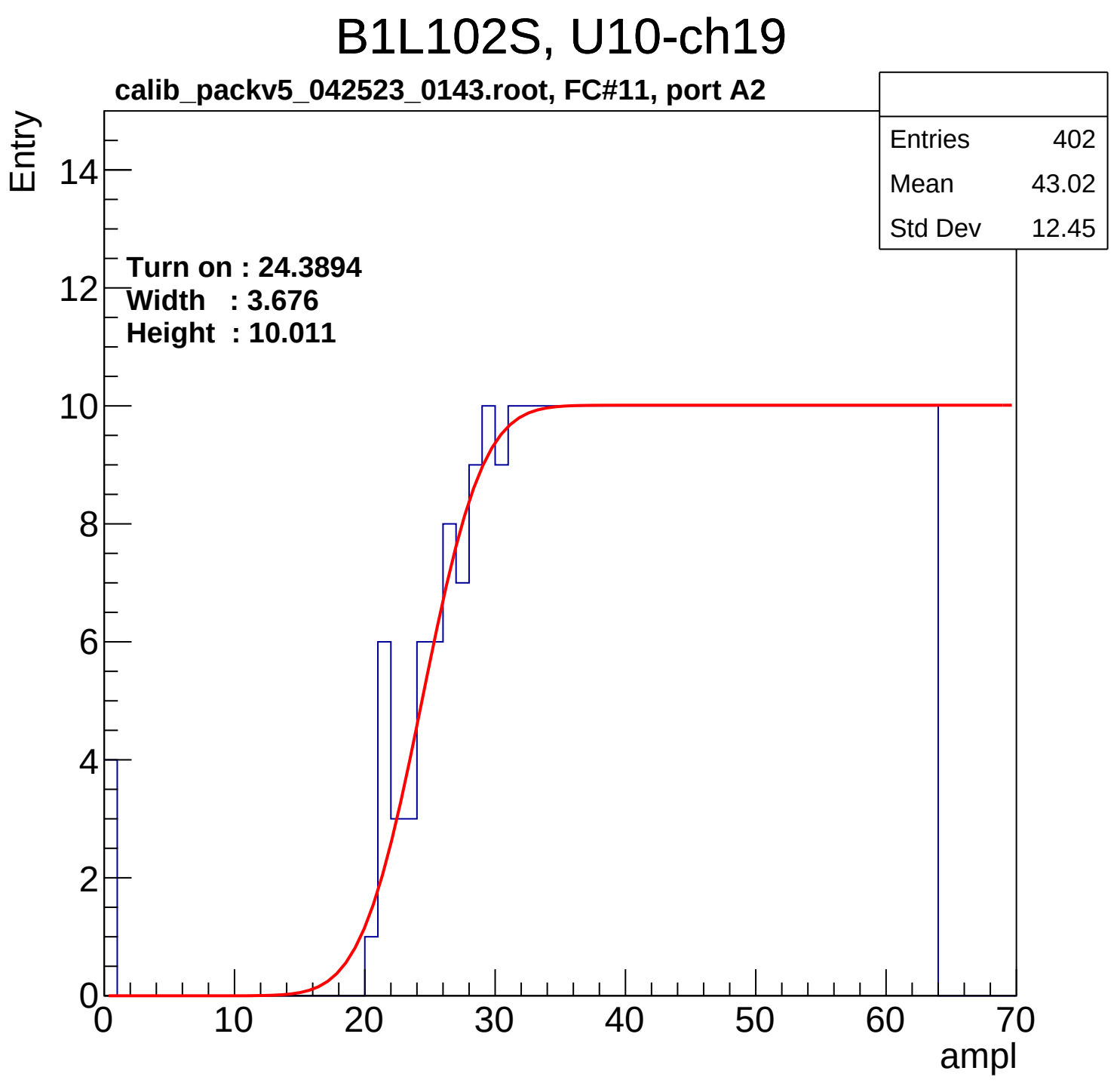
B1L102S, U10-ch19
calib_packv5_042523_0143.root, FC#11, port A2
Entries 402
Mean 43.02
Std Dev 12.45
Turn on : 24.3894
Width : 3.676
Height : 10.011
Entry
ampl
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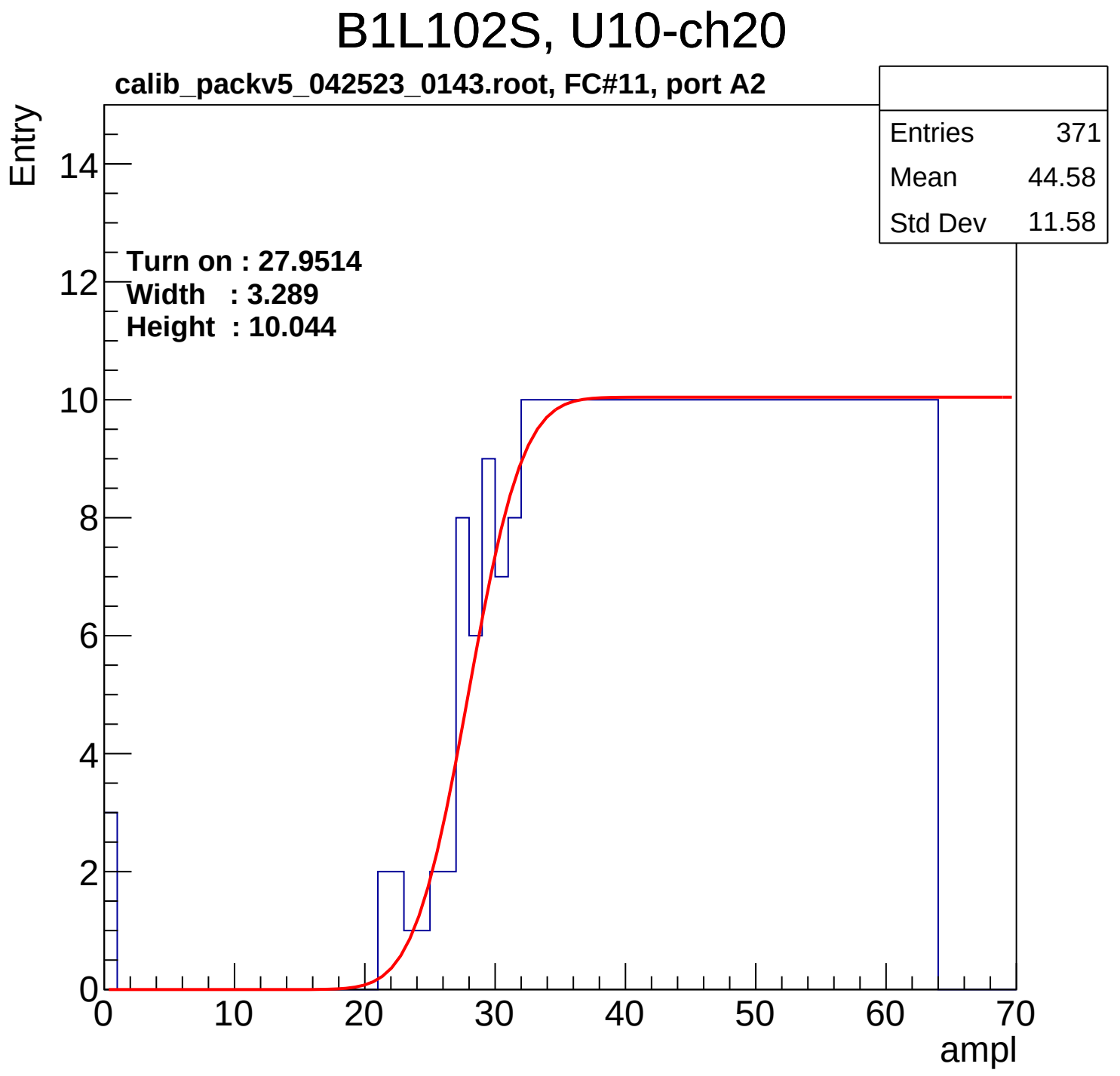
B1L102S, U10-ch20
calib_packv5_042523_0143.root, FC#11, port A2
Entries 371
Mean 44.58
Std Dev 11.58
Turn on : 27.9514
Width : 3.289
Height : 10.044
Entry
ampl
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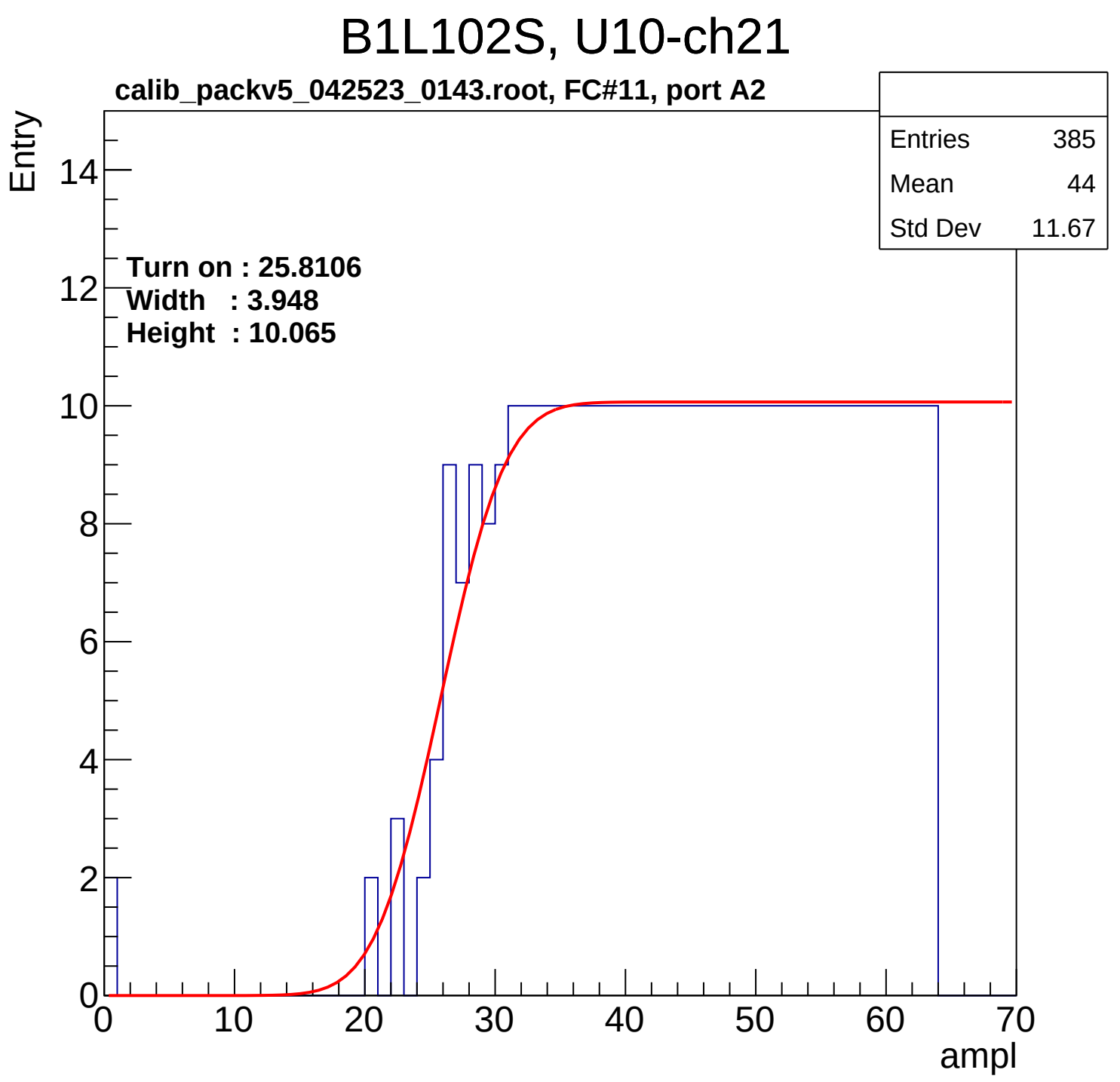
B1L102S, U10-ch21
calib_packv5_042523_0143.root, FC#11, port A2
Entries 385
Mean 44
Std Dev 11.67
Turn on : 25.8106
Width : 3.948
Height : 10.065
Entry
ampl
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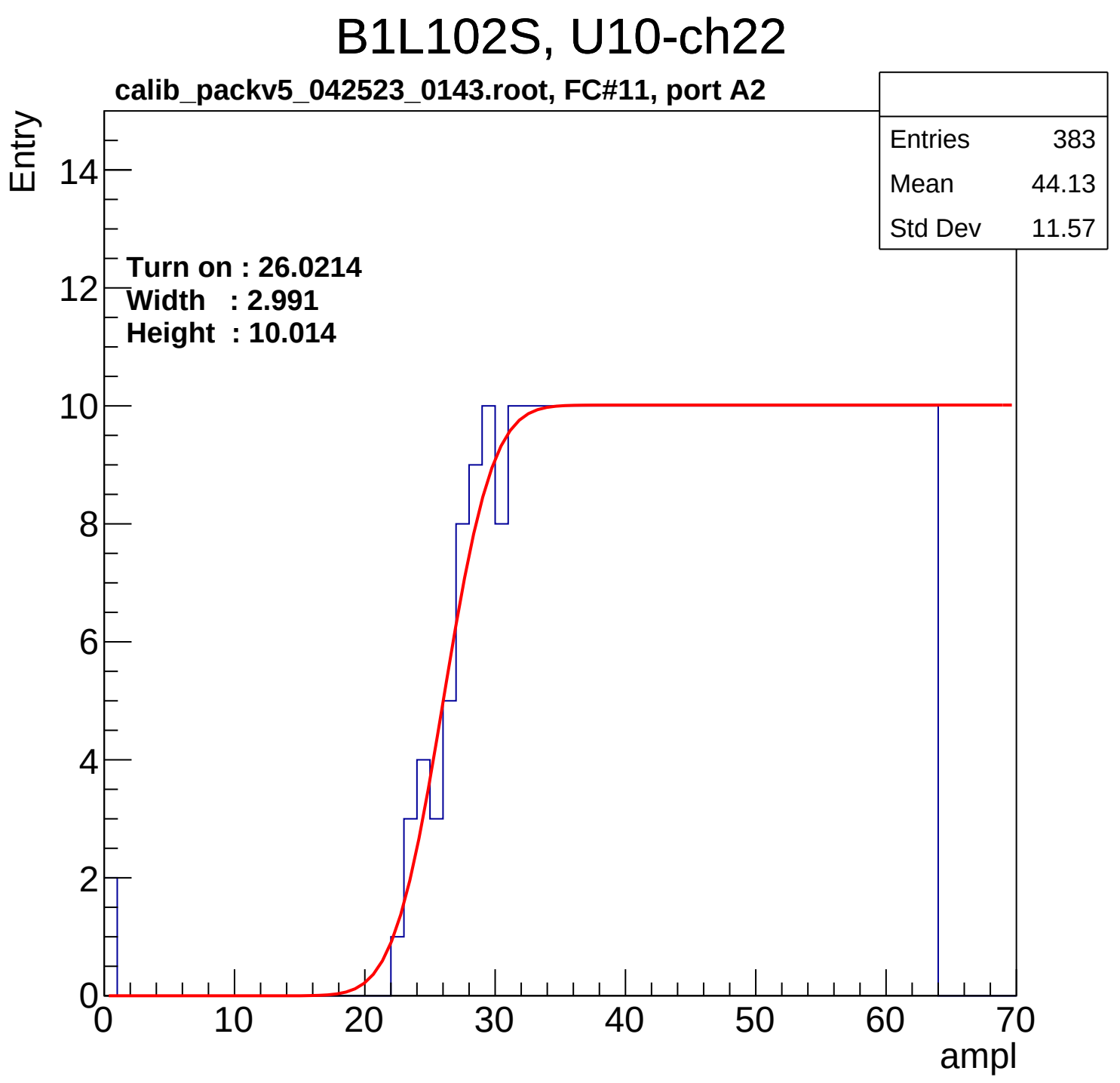
B1L102S, U10-ch22
calib_packv5_042523_0143.root, FC#11, port A2
Entries 383
Mean 44.13
Std Dev 11.57
Turn on : 26.0214
Width : 2.991
Height : 10.014
Entry
ampl
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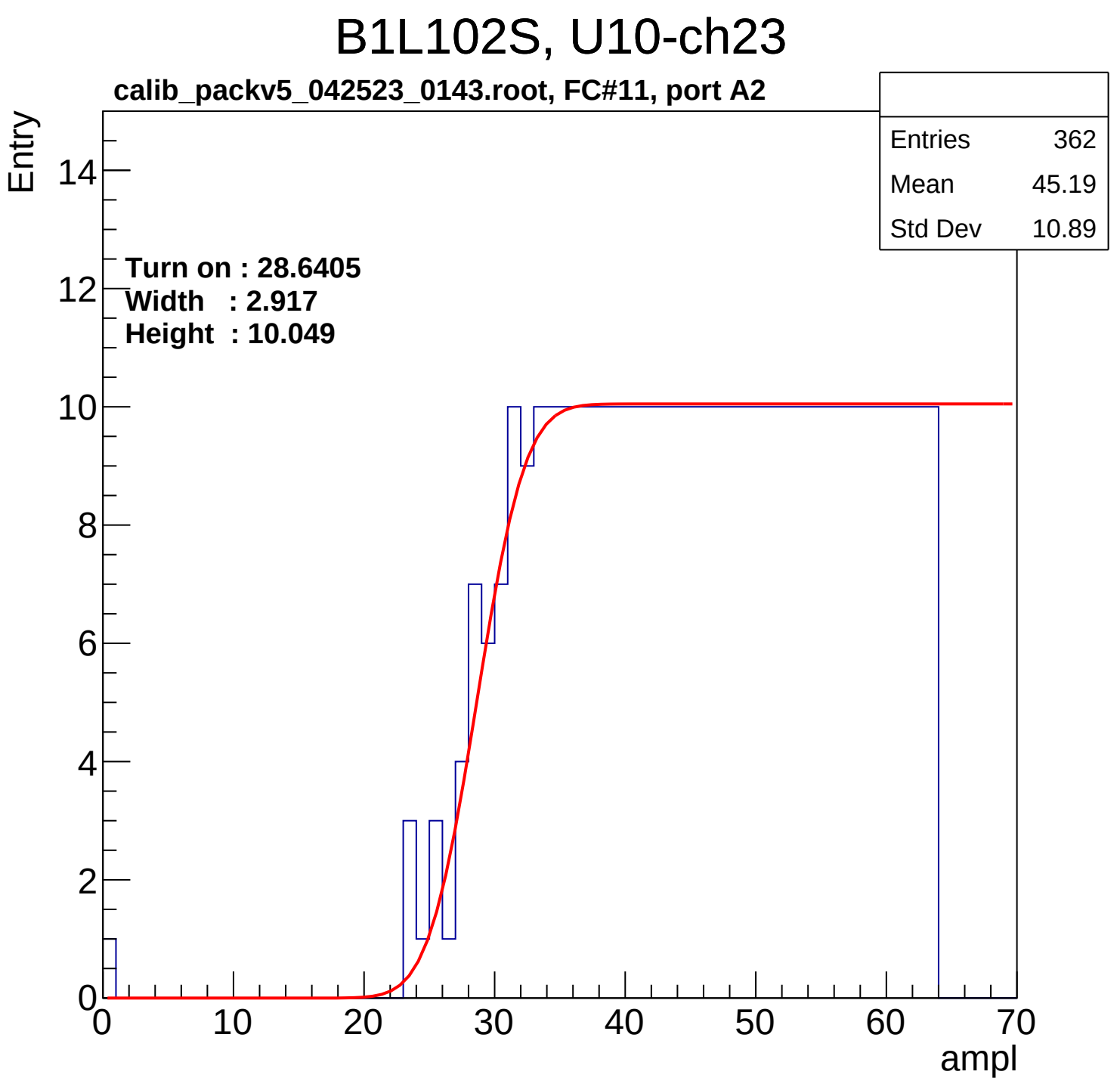
B1L102S, U10-ch23
calib_packv5_042523_0143.root, FC#11, port A2
Entries 362
Mean 45.19
Std Dev 10.89
Turn on : 28.6405
Width : 2.917
Height : 10.049
Entry
ampl
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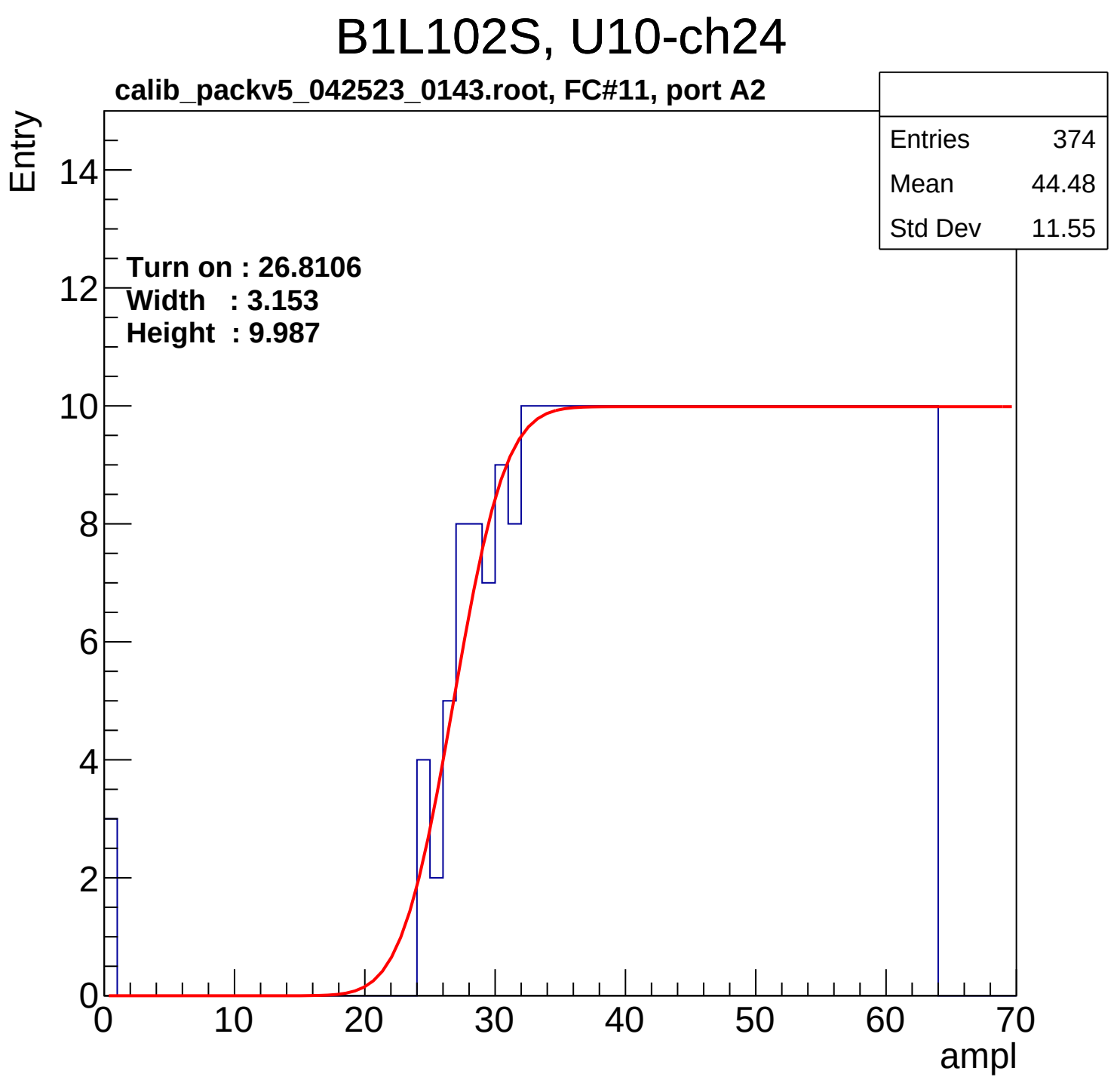
B1L102S, U10-ch24
calib_packv5_042523_0143.root, FC#11, port A2
Entries 374
Mean 44.48
Std Dev 11.55
Turn on : 26.8106
Width : 3.153
Height : 9.987
Entry
ampl
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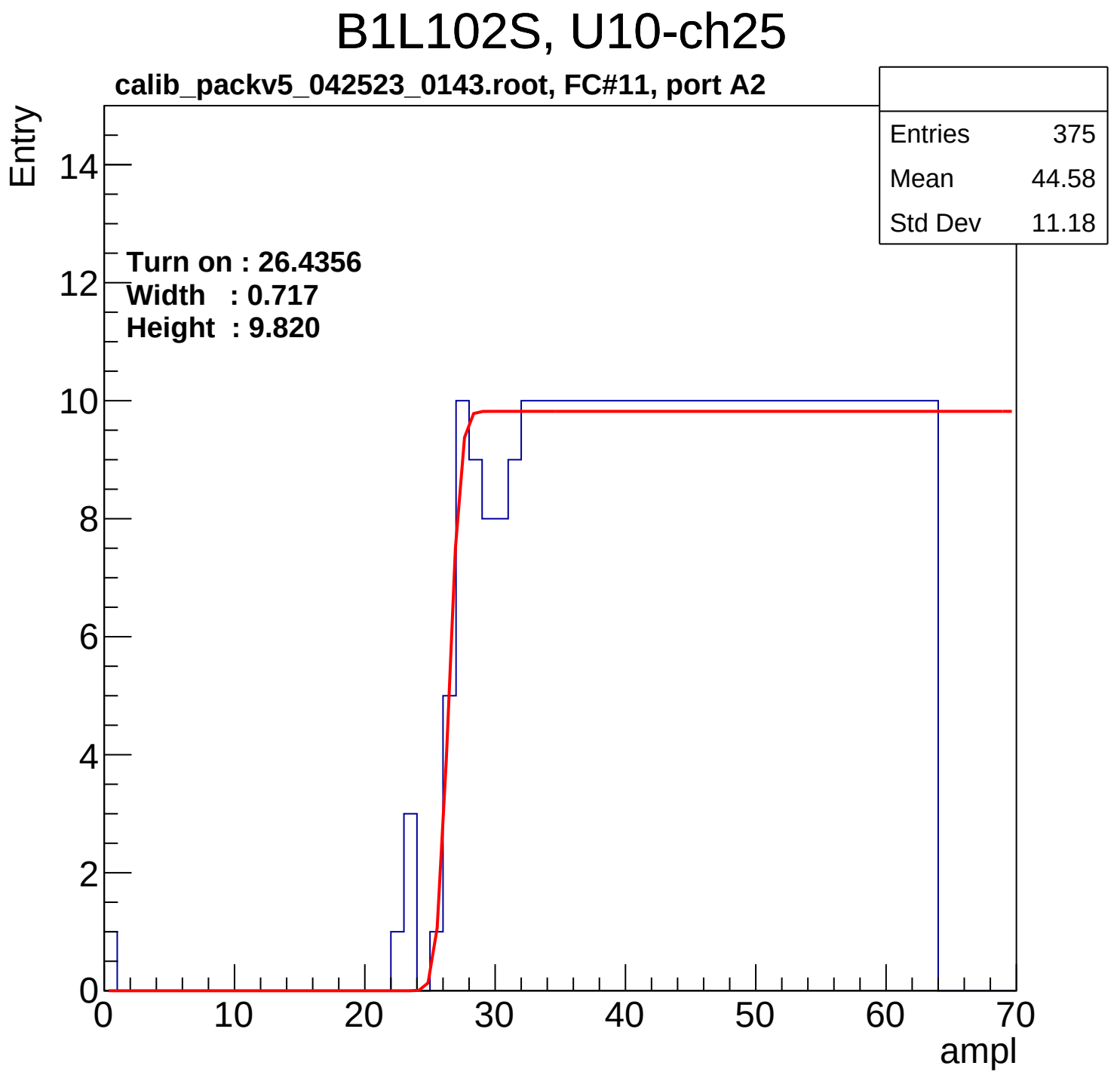
B1L102S, U10-ch25
calib_packv5_042523_0143.root, FC#11, port A2
Entries 375
Mean 44.58
Std Dev 11.18
Turn on : 26.4356
Width : 0.717
Height : 9.820
Entry
ampl
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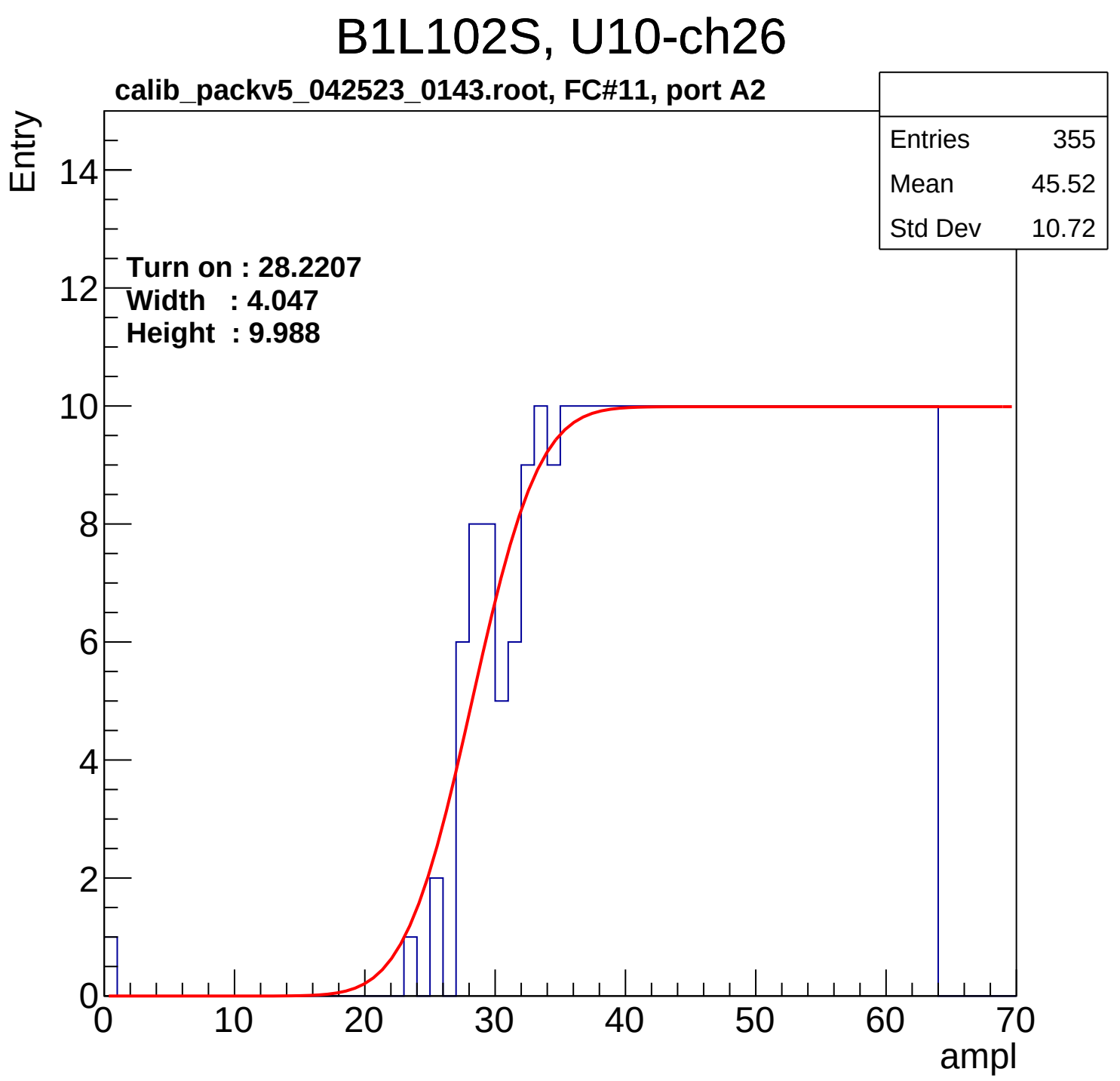
B1L102S, U10-ch26
calib_packv5_042523_0143.root, FC#11, port A2
Entries 355
Mean 45.52
Std Dev 10.72
Turn on : 28.2207
Width : 4.047
Height : 9.988
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ampl
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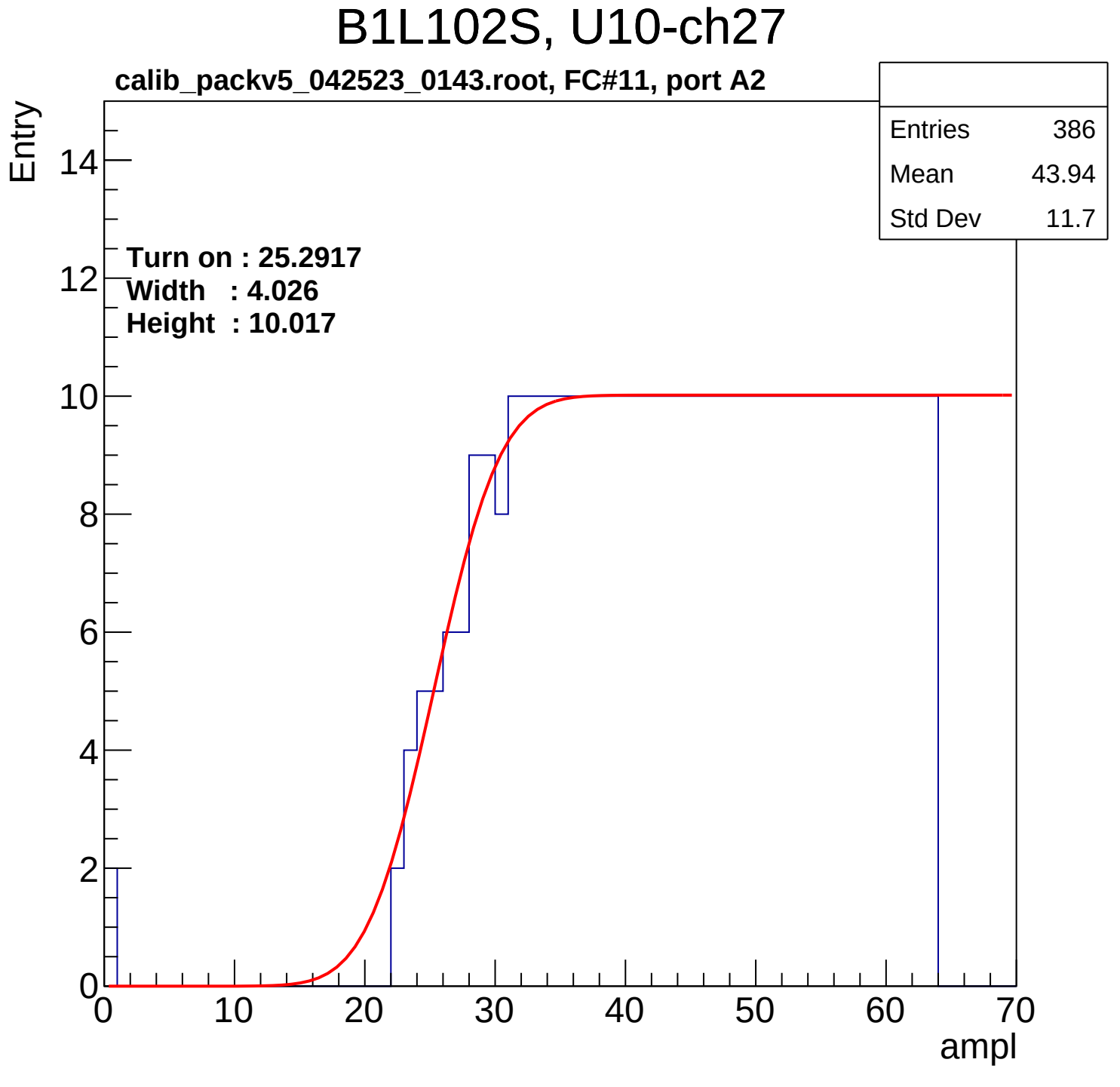
B1L102S, U10-ch27
calib_packv5_042523_0143.root, FC#11, port A2
Entries 386
Mean 43.94
Std Dev 11.7
Turn on : 25.2917
Width : 4.026
Height : 10.017
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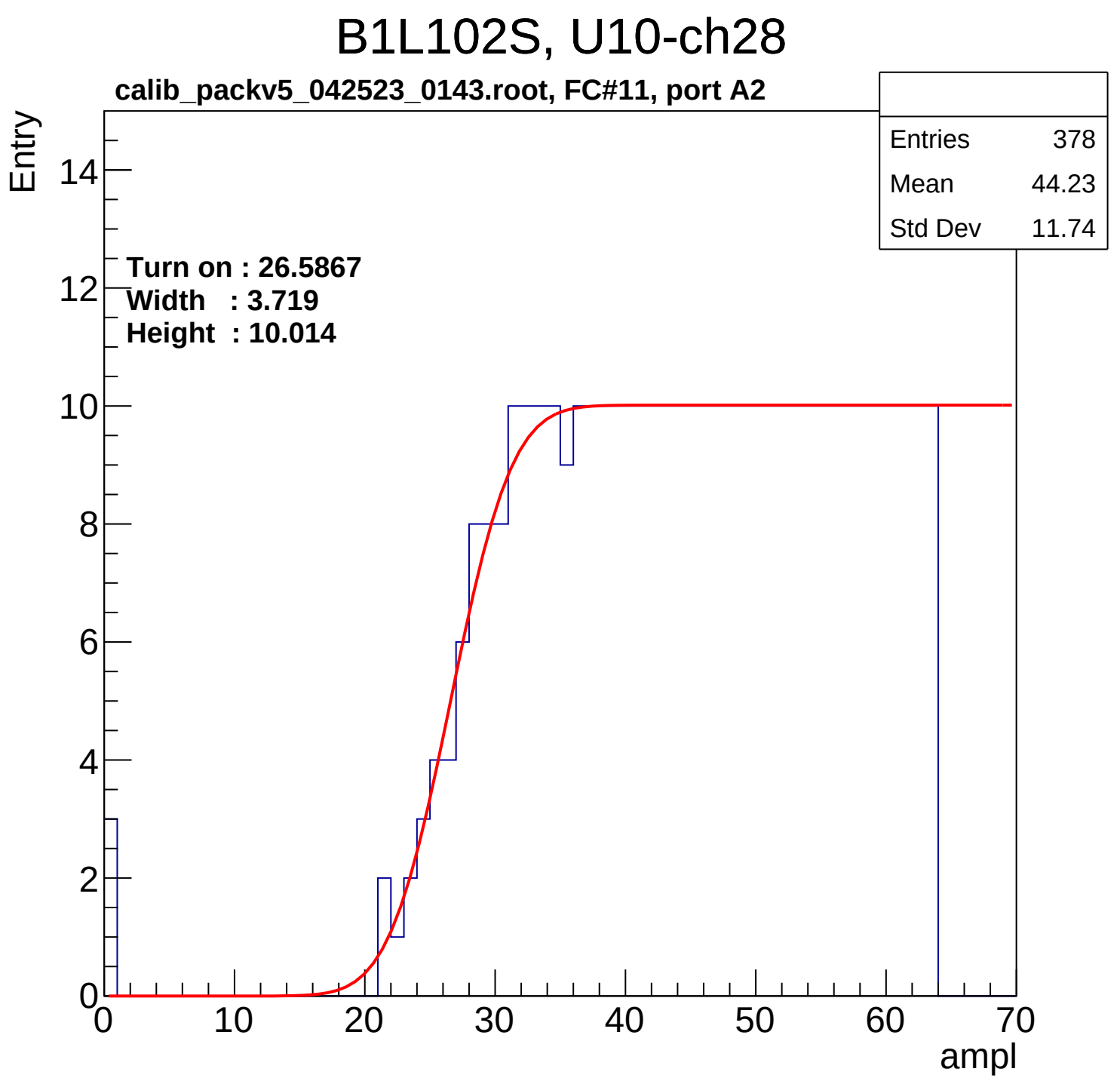
B1L102S, U10-ch28
calib_packv5_042523_0143.root, FC#11, port A2
Entries 378
Mean 44.23
Std Dev 11.74
Turn on : 26.5867
Width : 3.719
Height : 10.014
Entry
ampl
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6
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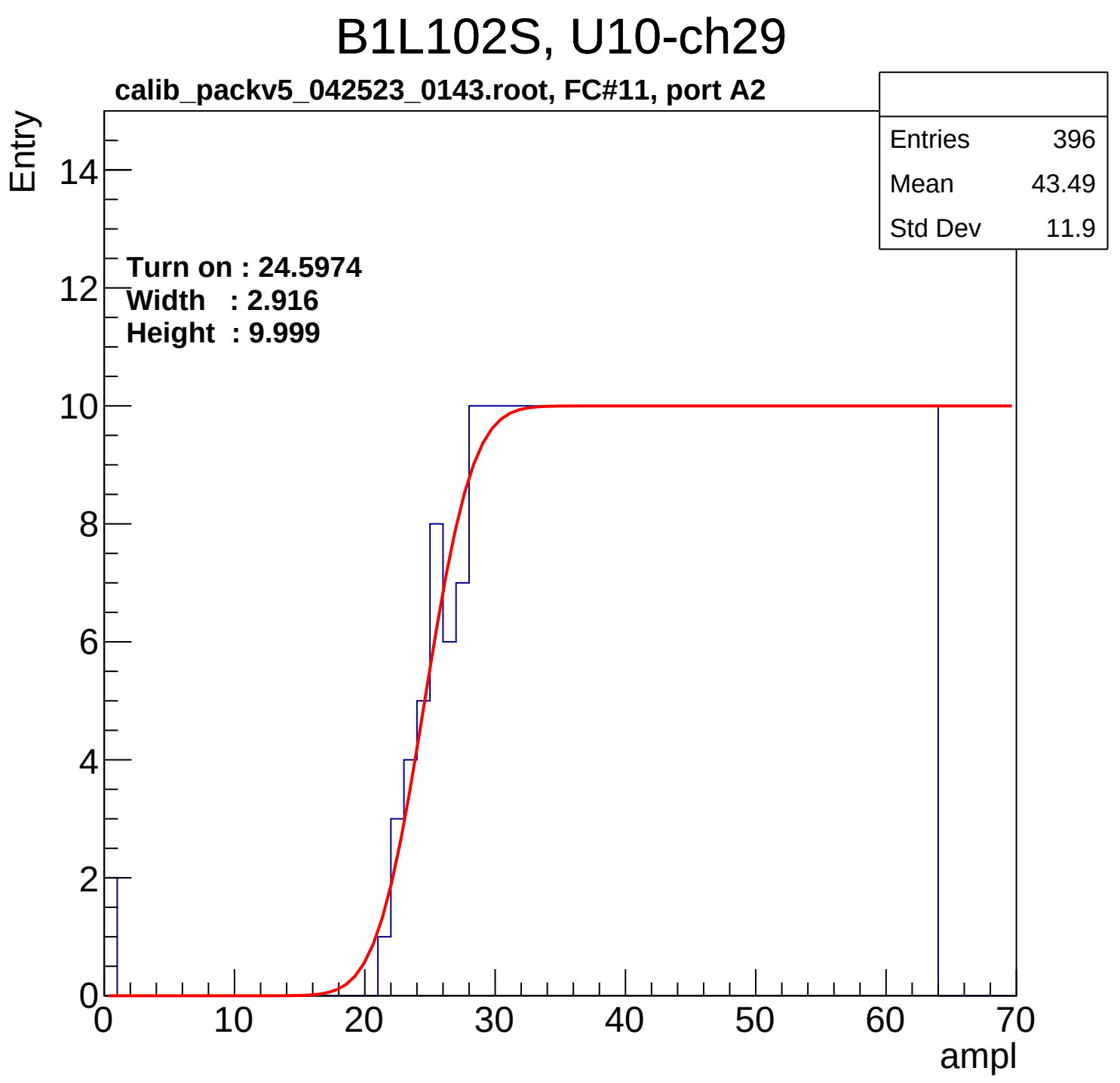
B1L102S, U10-ch29
calib_packv5_042523_0143.root, FC#11, port A2
Entries 396
Mean 43.49
Std Dev 11.9
Turn on : 24.5974
Width : 2.916
Height : 9.999
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ampl
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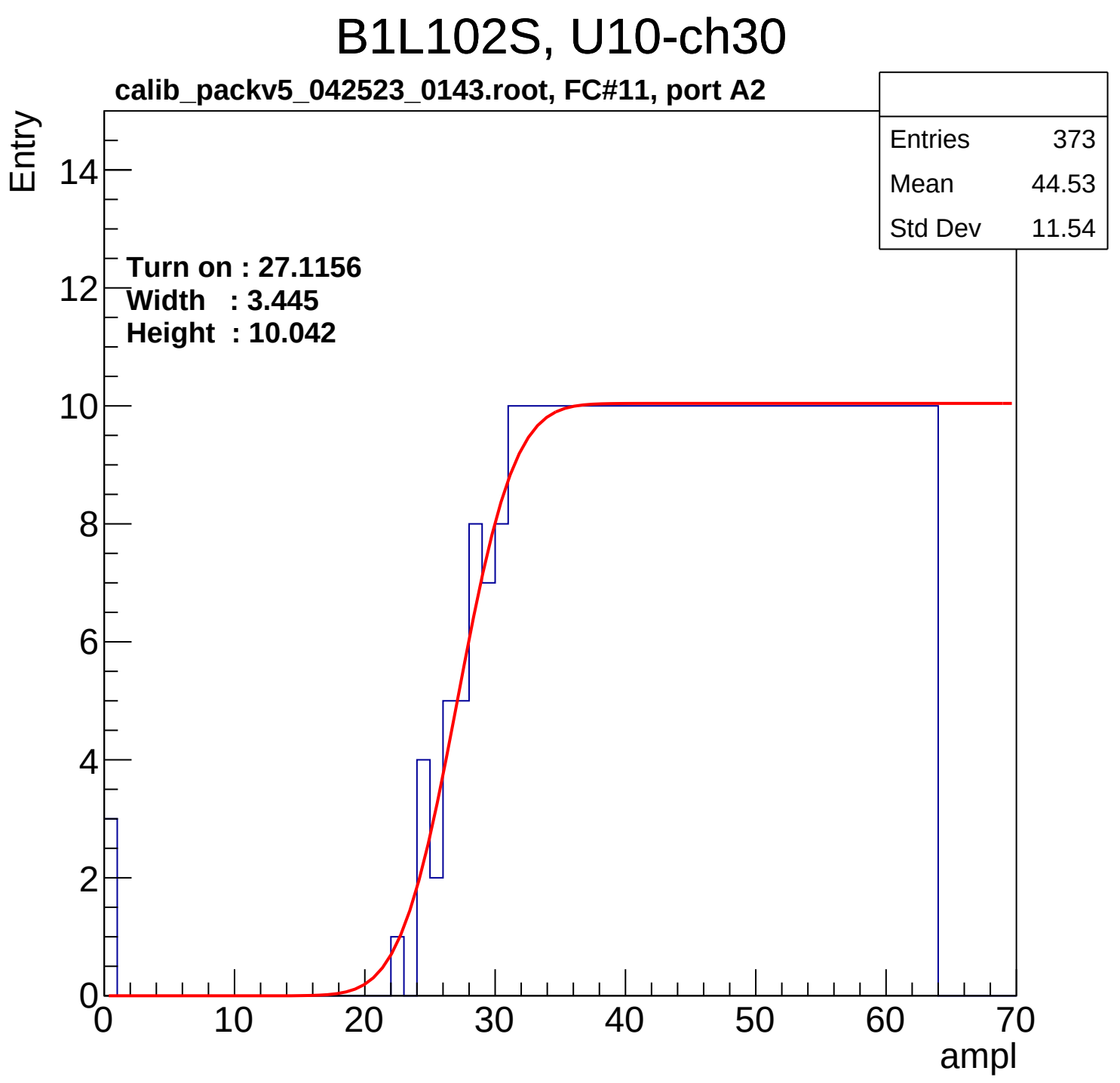
B1L102S, U10-ch30
calib_packv5_042523_0143.root, FC#11, port A2
Entries 373
Mean 44.53
Std Dev 11.54
Turn on : 27.1156
Width : 3.445
Height : 10.042
Entry
ampl
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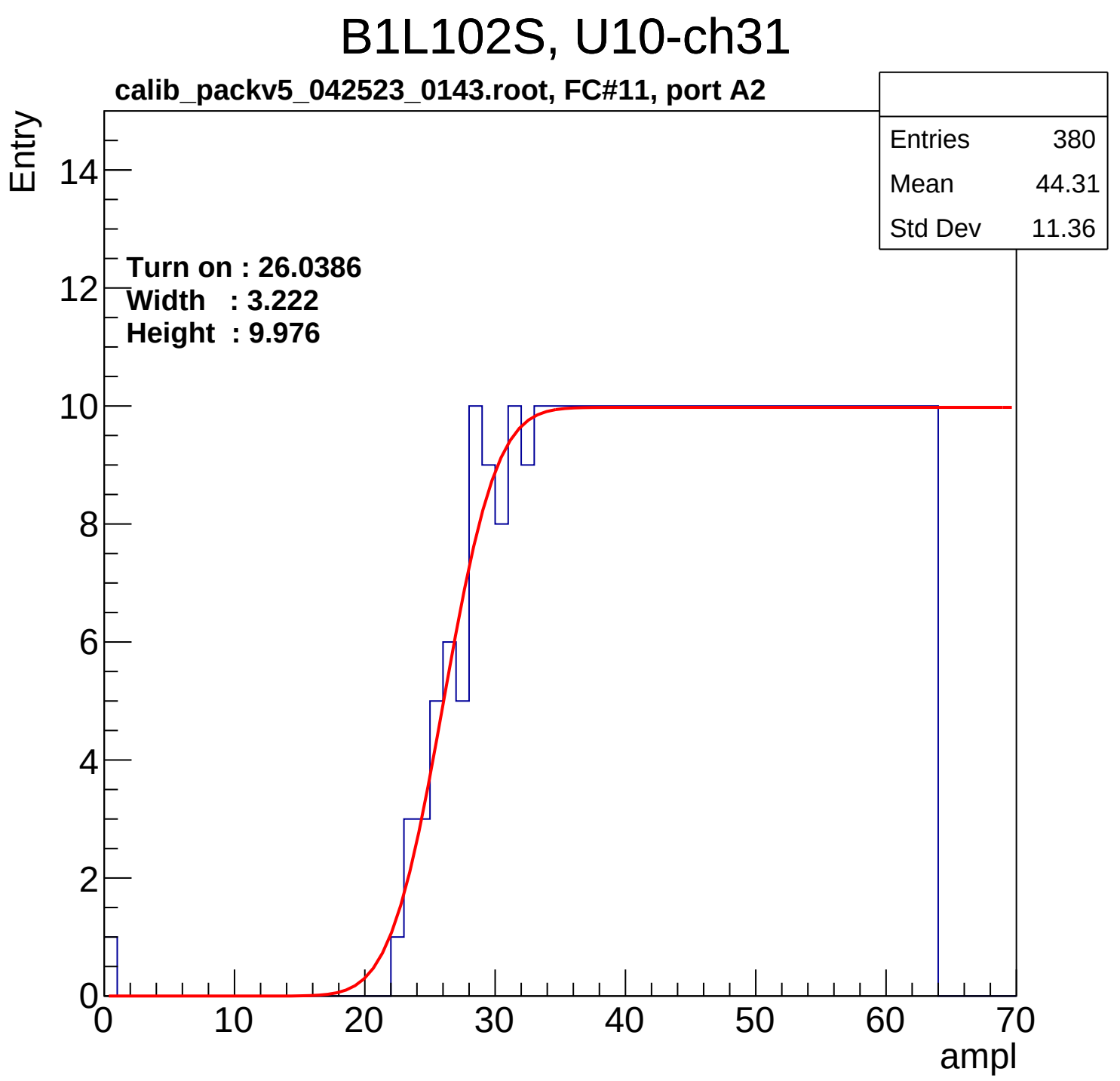
B1L102S, U10-ch31
calib_packv5_042523_0143.root, FC#11, port A2
Entries 380
Mean 44.31
Std Dev 11.36
Turn on : 26.0386
Width : 3.222
Height : 9.976
Entry
ampl
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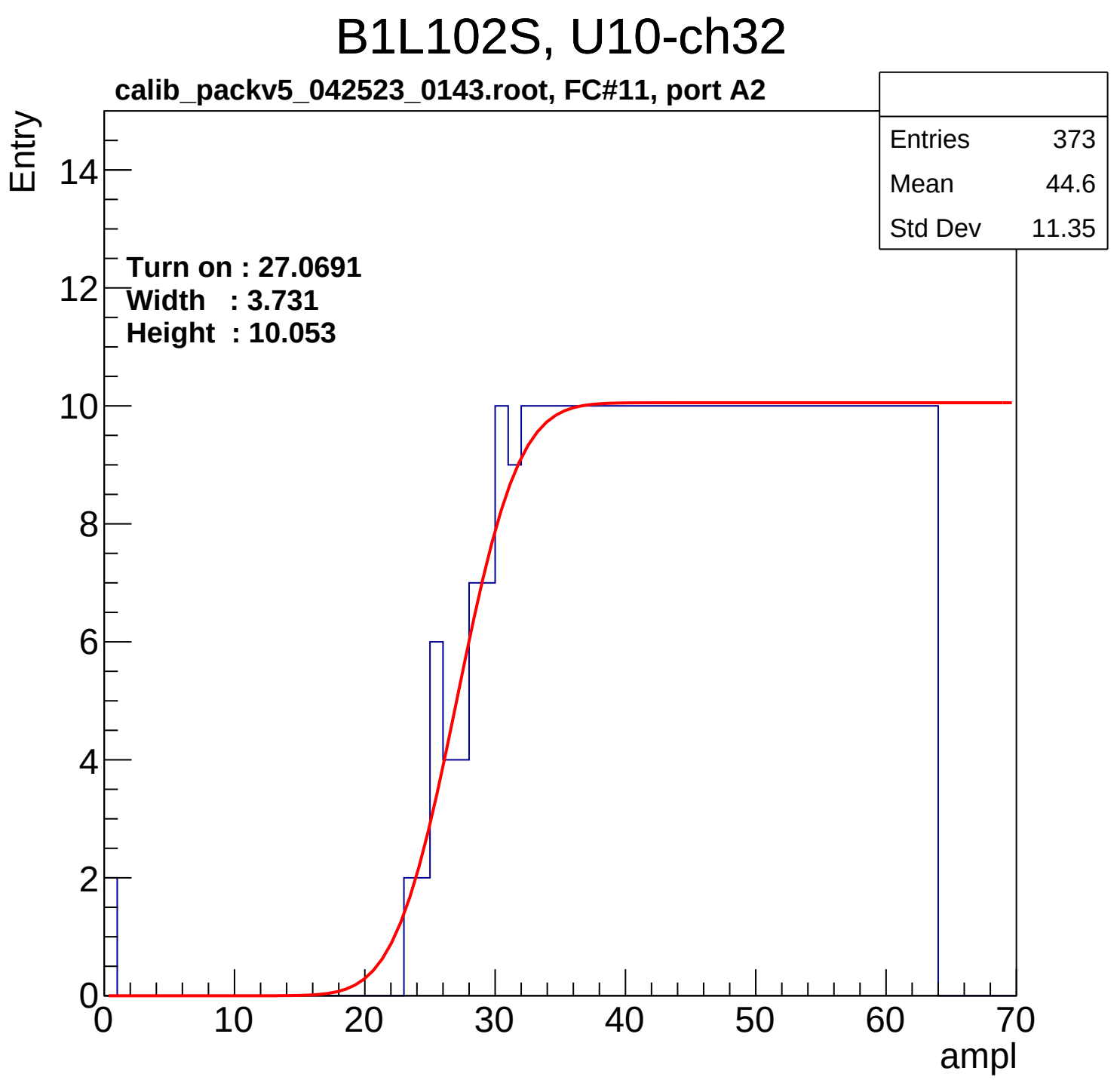
B1L102S, U10-ch32
calib_packv5_042523_0143.root, FC#11, port A2
Entries 373
Mean 44.6
Std Dev 11.35
Turn on : 27.0691
Width : 3.731
Height : 10.053
Entry
ampl
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6
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0
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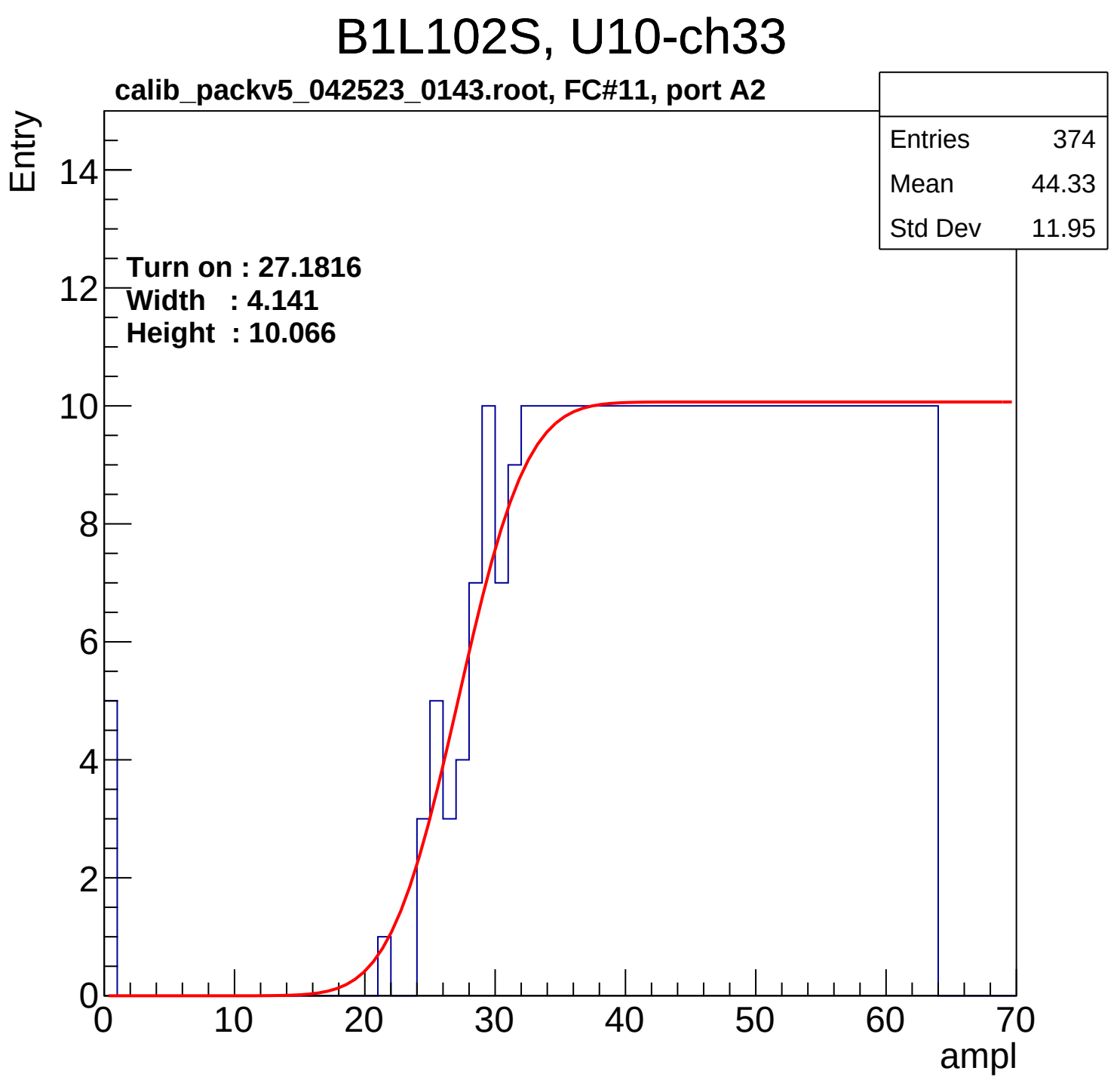
B1L102S, U10-ch33
calib_packv5_042523_0143.root, FC#11, port A2
Entries 374
Mean 44.33
Std Dev 11.95
Turn on : 27.1816
Width : 4.141
Height : 10.066
Entry
ampl
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0
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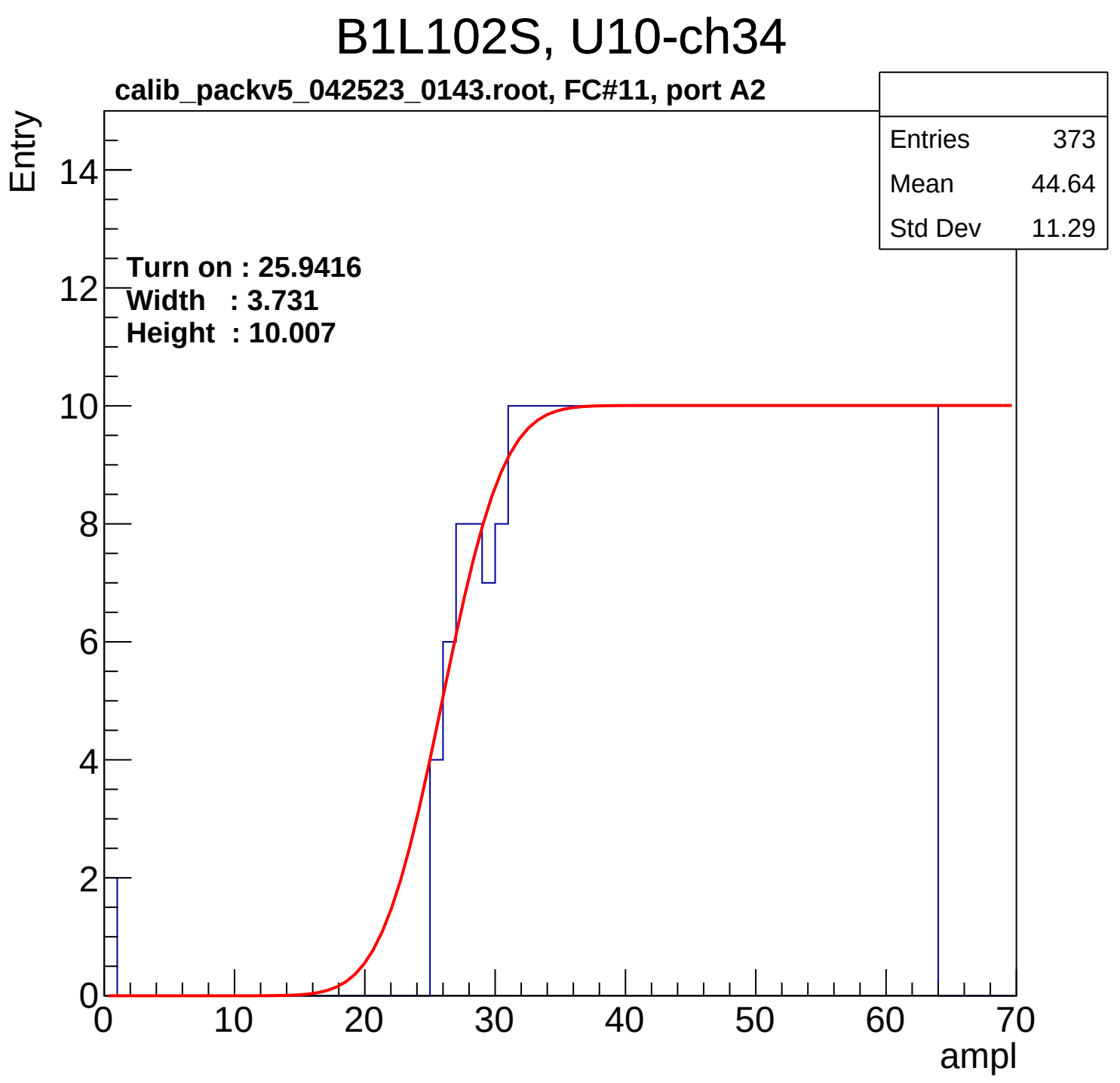
B1L102S, U10-ch34
calib_packv5_042523_0143.root, FC#11, port A2
Entries 373
Mean 44.64
Std Dev 11.29
Turn on : 25.9416
Width : 3.731
Height : 10.007
Entry
ampl
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2
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6
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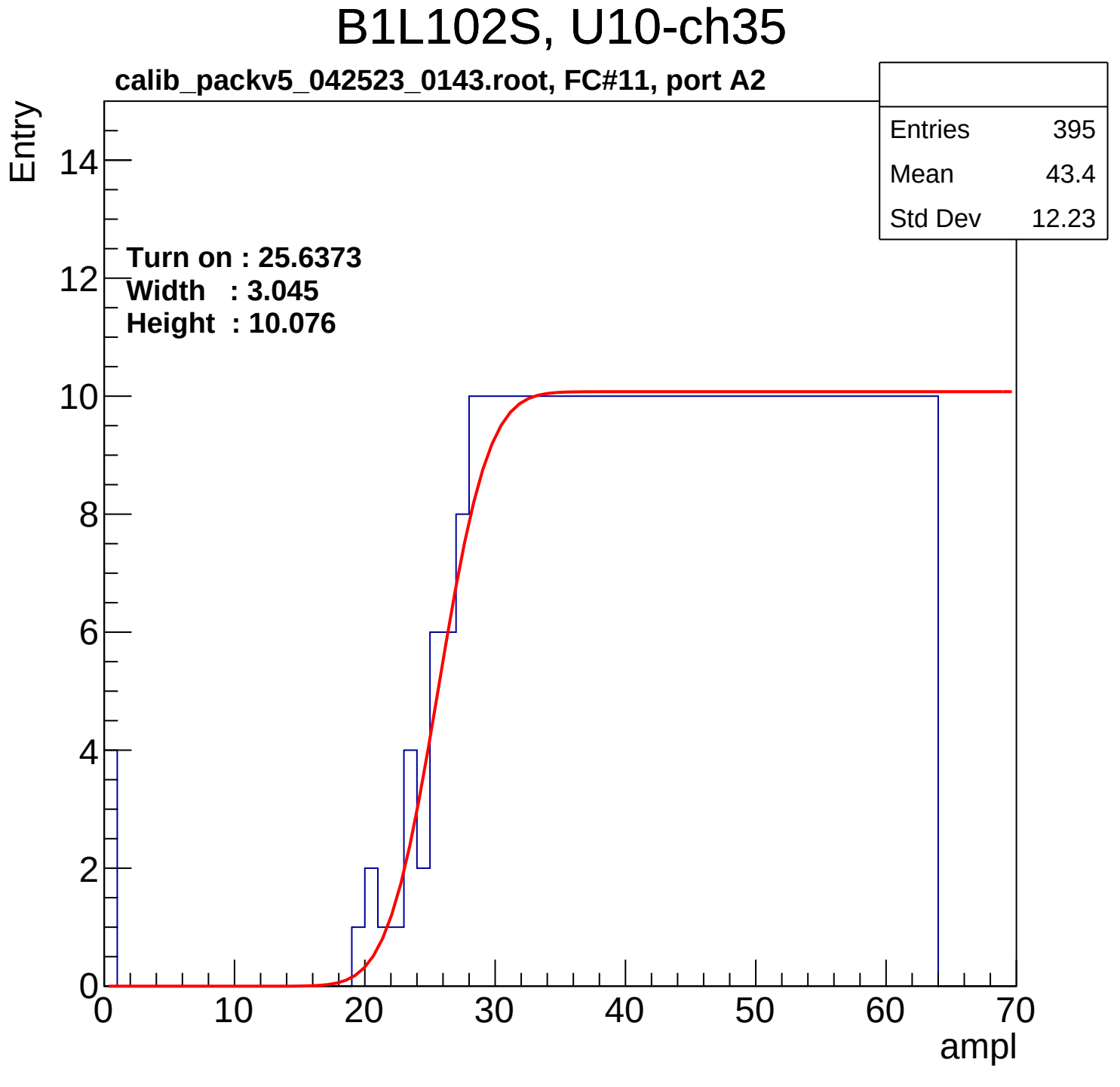
B1L102S, U10-ch35
calib_packv5_042523_0143.root, FC#11, port A2
Entries 395
Mean 43.4
Std Dev 12.23
Turn on : 25.6373
Width : 3.045
Height : 10.076
Entry
ampl
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8
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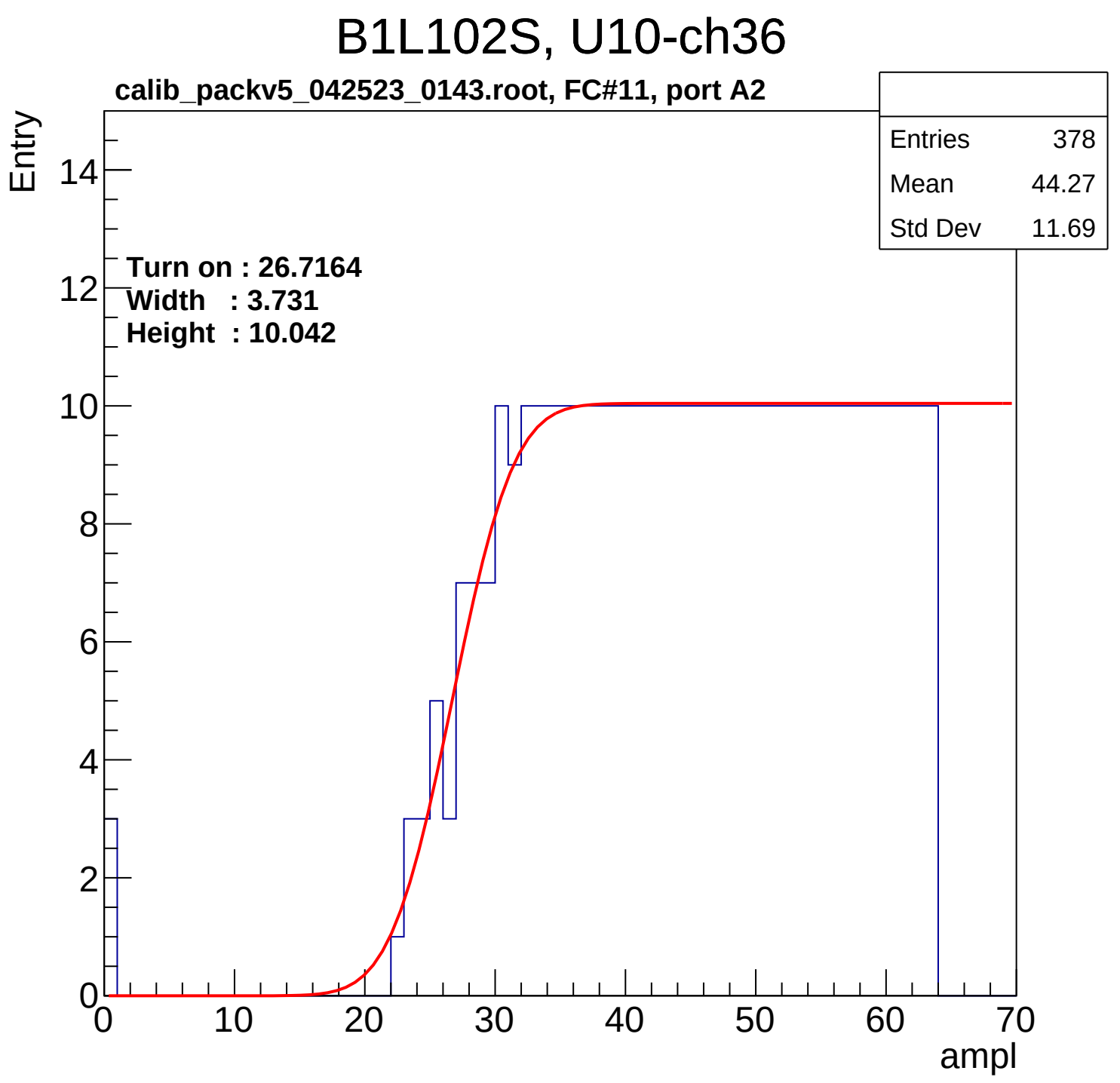
B1L102S, U10-ch36
calib_packv5_042523_0143.root, FC#11, port A2
Entries 378
Mean 44.27
Std Dev 11.69
Turn on : 26.7164
Width : 3.731
Height : 10.042
Entry
ampl
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4
6
8
10
12
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0
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20
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40
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60
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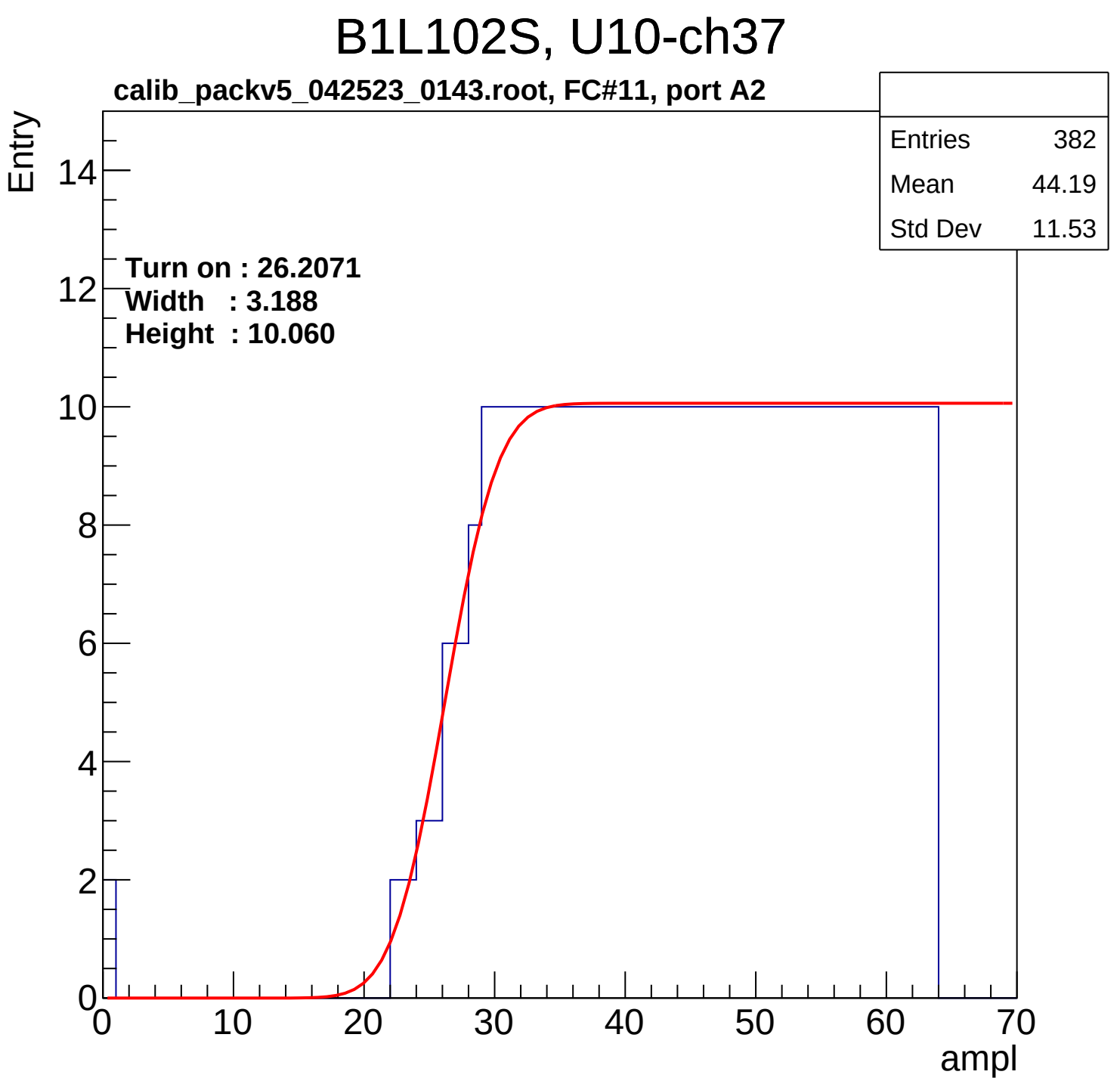
B1L102S, U10-ch37
calib_packv5_042523_0143.root, FC#11, port A2
Entries 382
Mean 44.19
Std Dev 11.53
Turn on : 26.2071
Width : 3.188
Height : 10.060
Entry
ampl
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2
4
6
8
10
12
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60
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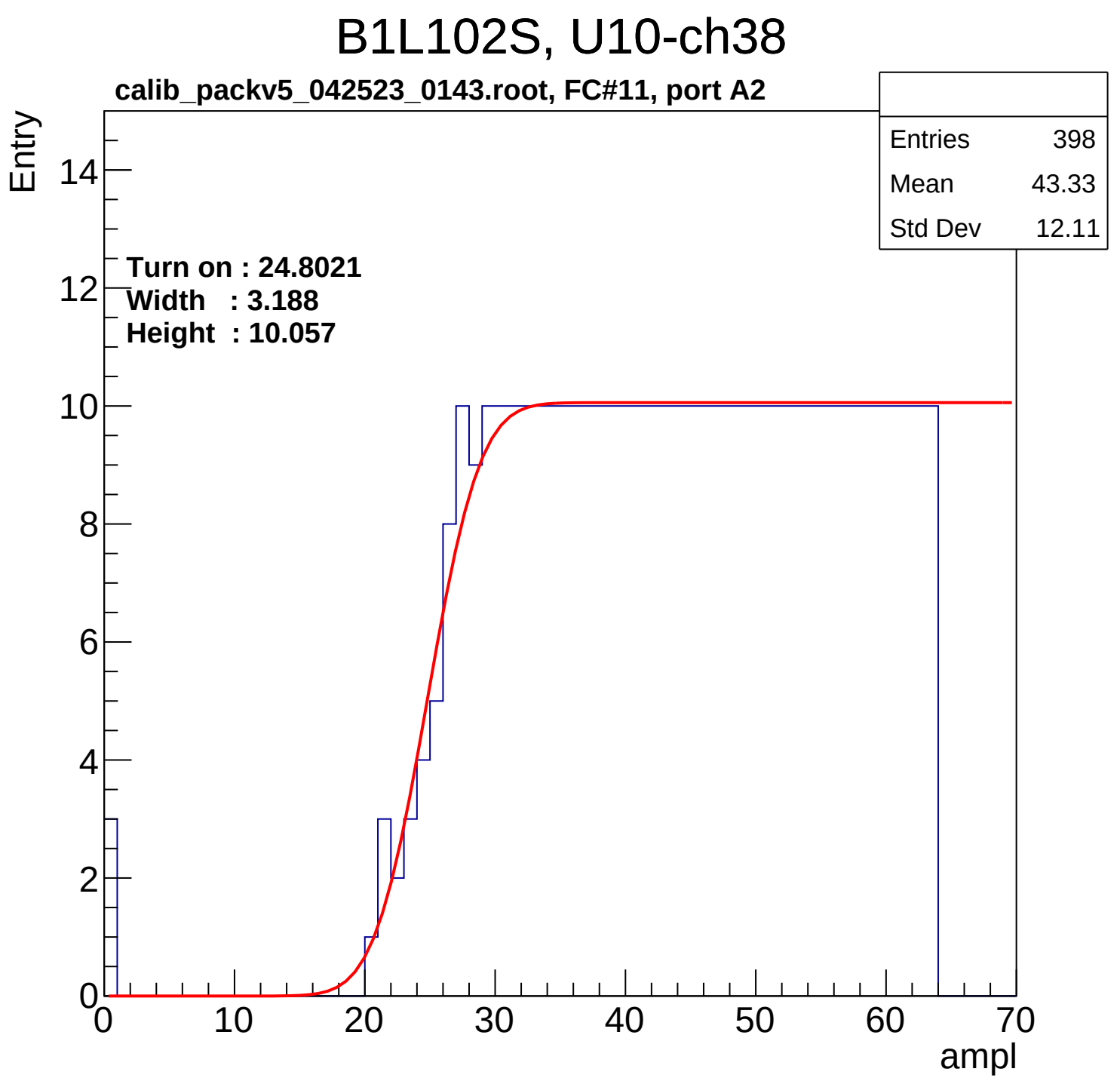
B1L102S, U10-ch38
calib_packv5_042523_0143.root, FC#11, port A2
Entries 398
Mean 43.33
Std Dev 12.11
Turn on : 24.8021
Width : 3.188
Height : 10.057
Entry
ampl
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6
8
10
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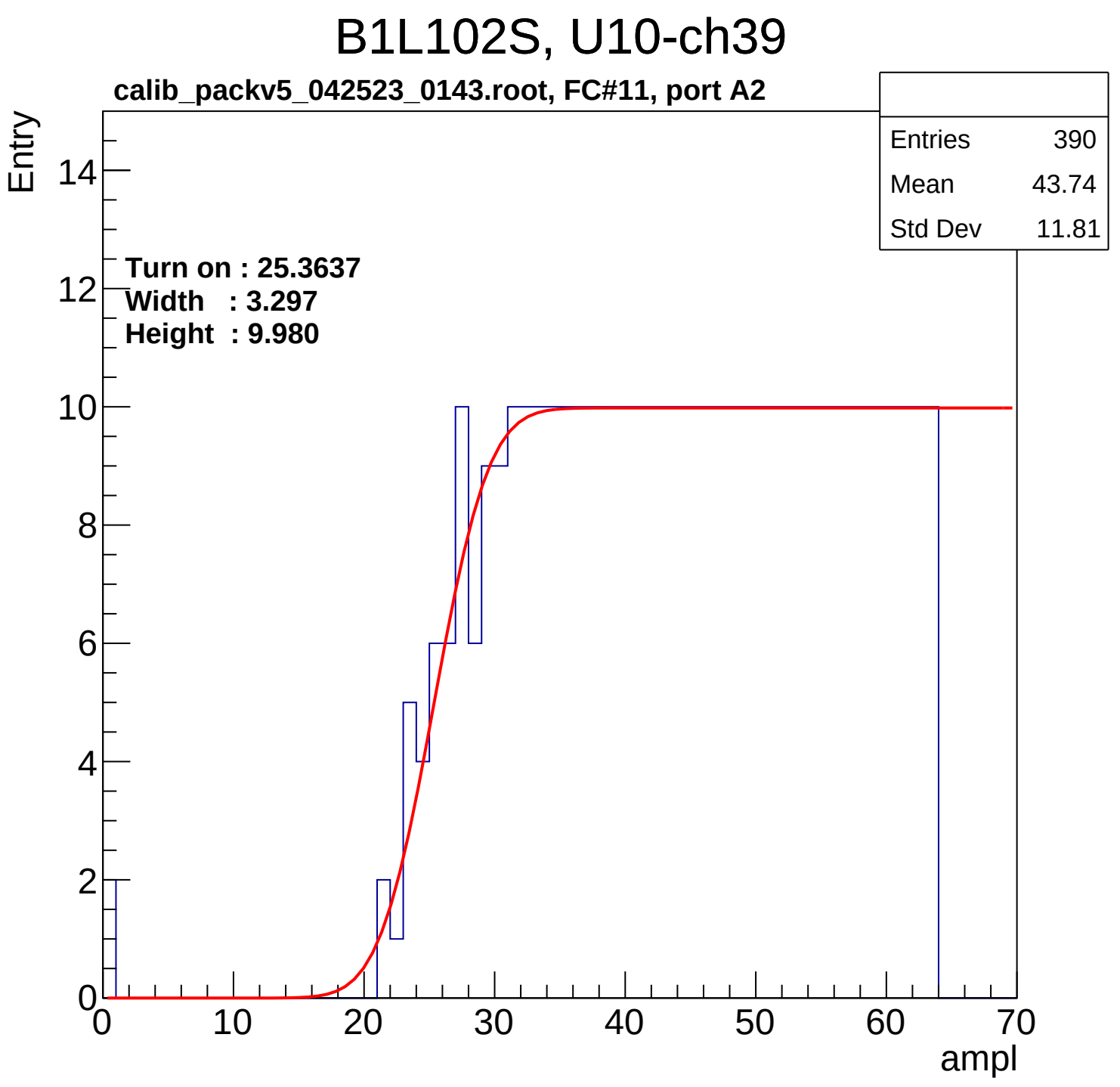
B1L102S, U10-ch39
calib_packv5_042523_0143.root, FC#11, port A2
Entries 390
Mean 43.74
Std Dev 11.81
Turn on : 25.3637
Width : 3.297
Height : 9.980
Entry
ampl
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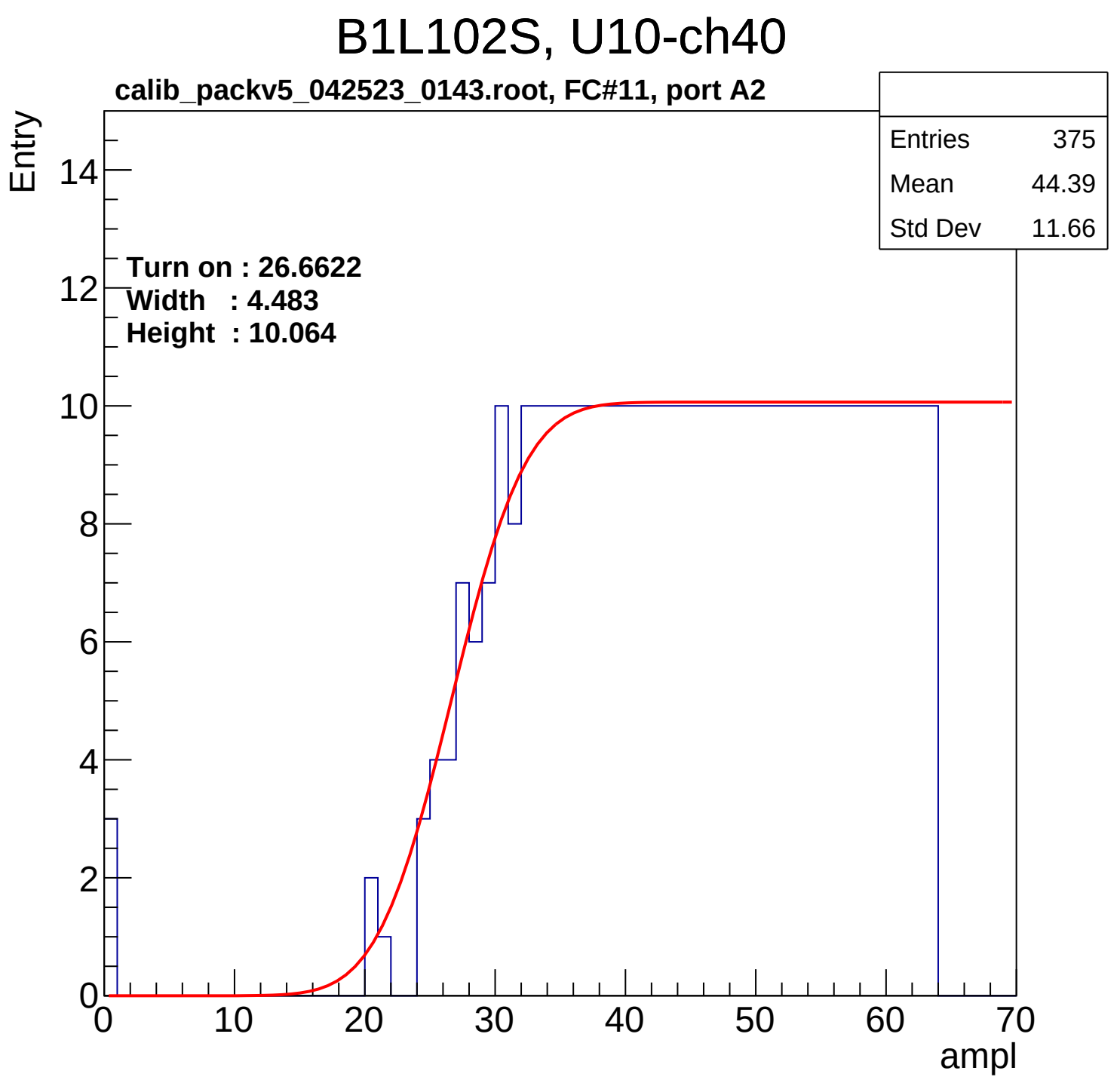
B1L102S, U10-ch40
calib_packv5_042523_0143.root, FC#11, port A2
Entries 375
Mean 44.39
Std Dev 11.66
Turn on : 26.6622
Width : 4.483
Height : 10.064
Entry
ampl
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8
10
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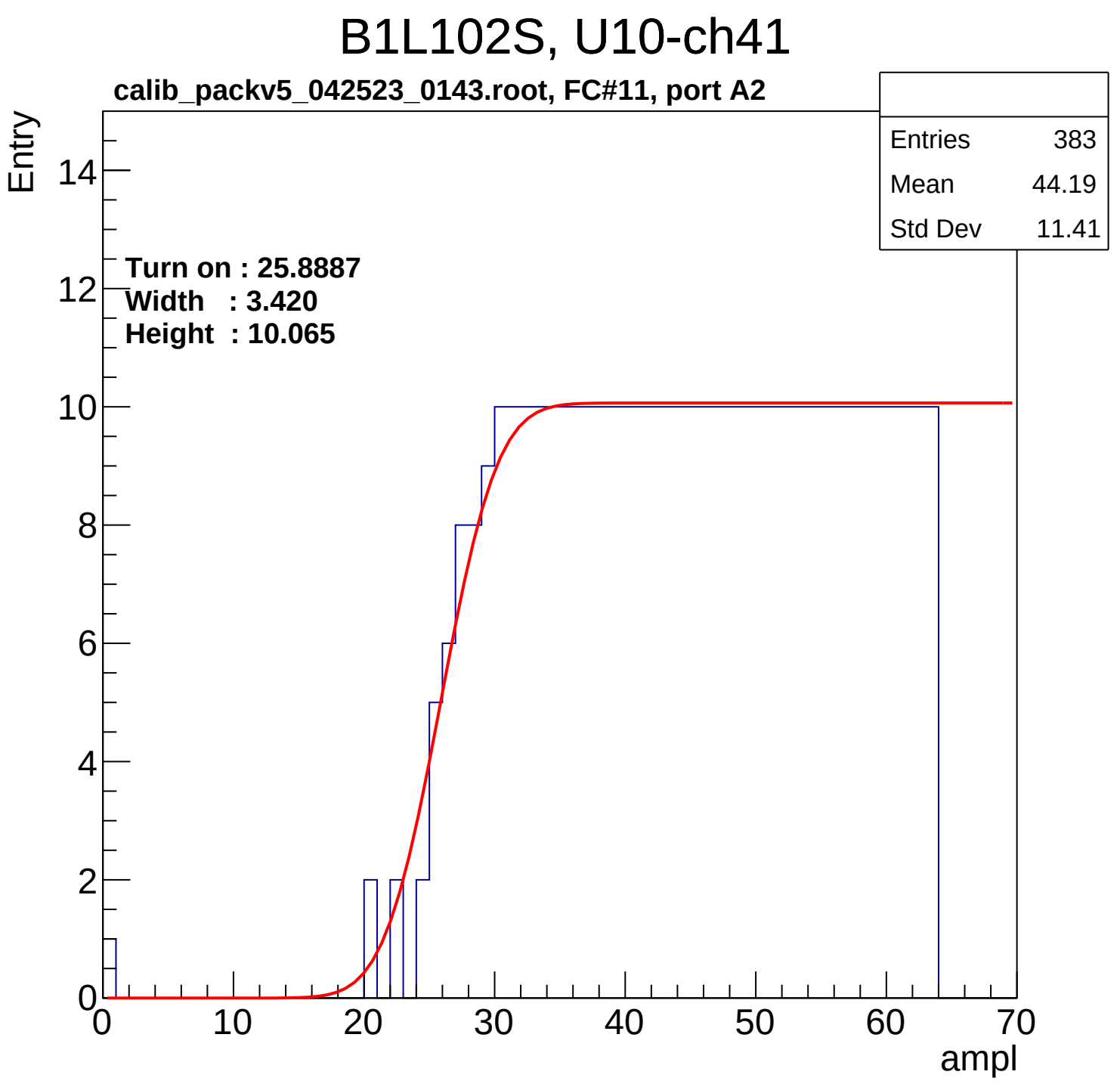
B1L102S, U10-ch41
calib_packv5_042523_0143.root, FC#11, port A2
Entries 383
Mean 44.19
Std Dev 11.41
Turn on : 25.8887
Width : 3.420
Height : 10.065
Entry
ampl
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6
8
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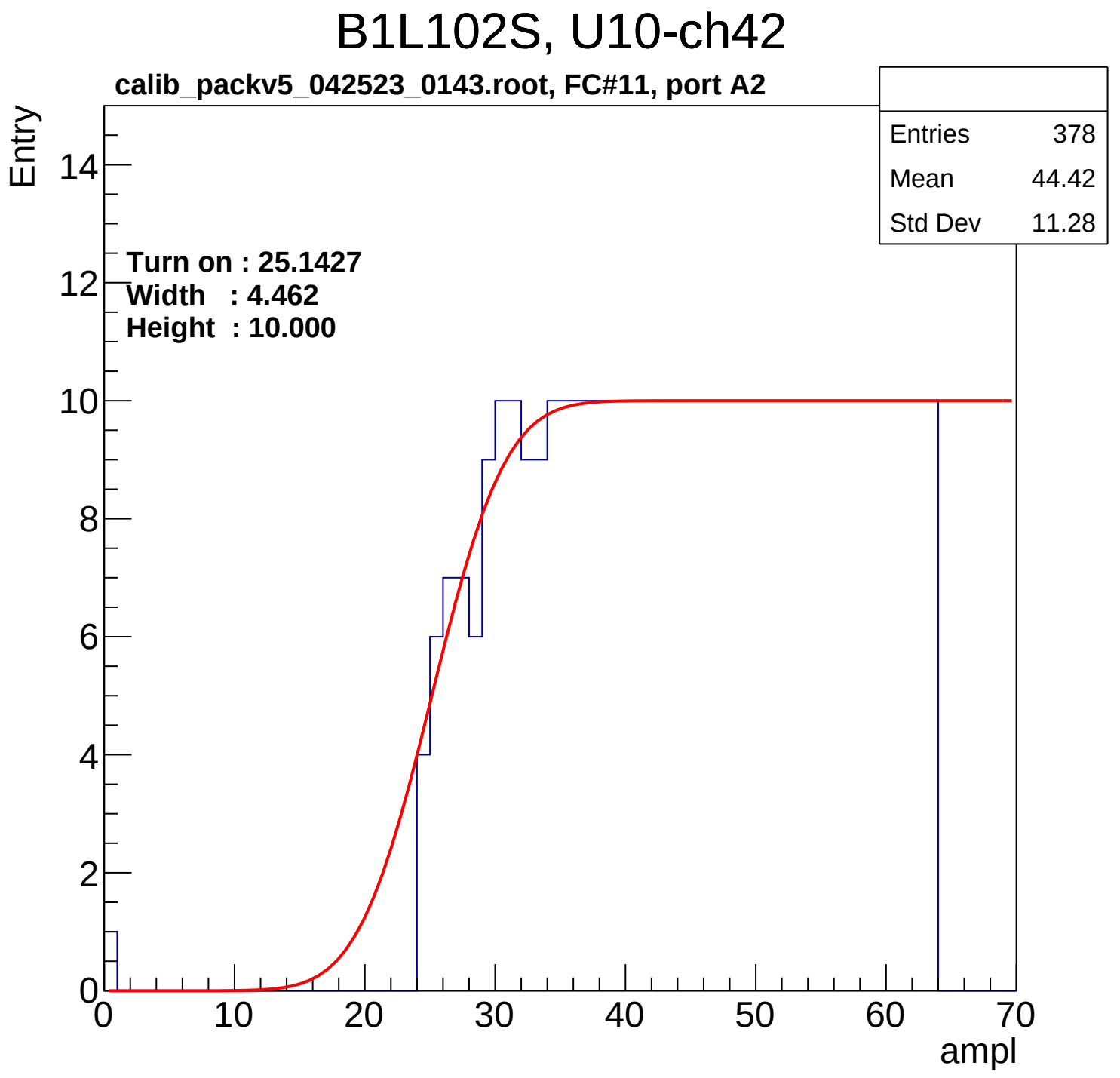
B1L102S, U10-ch42
calib_packv5_042523_0143.root, FC#11, port A2
Entries 378
Mean 44.42
Std Dev 11.28
Turn on : 25.1427
Width : 4.462
Height : 10.000
Entry
ampl
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6
8
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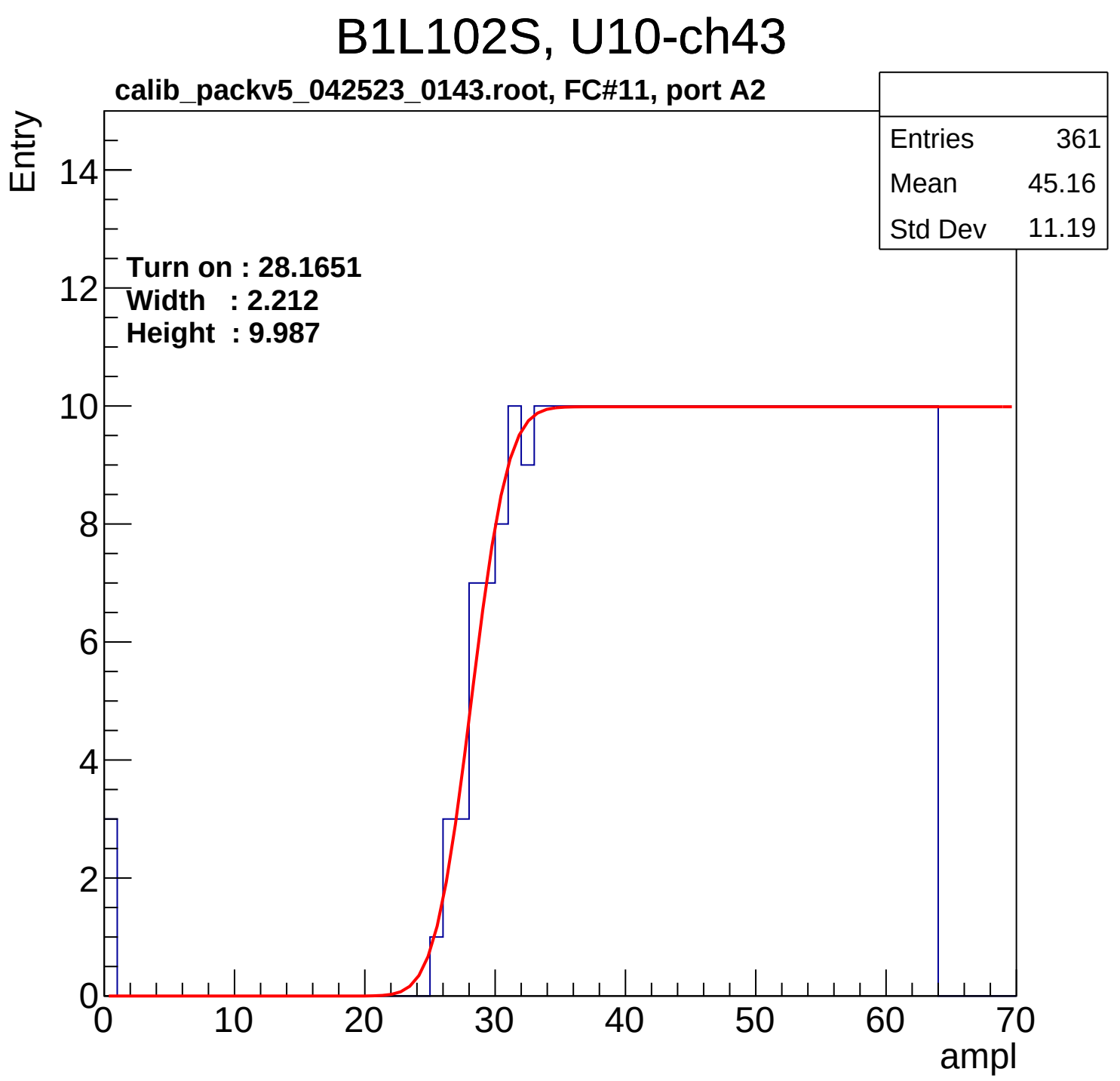
B1L102S, U10-ch43
calib_packv5_042523_0143.root, FC#11, port A2
Entries 361
Mean 45.16
Std Dev 11.19
Turn on : 28.1651
Width : 2.212
Height : 9.987
Entry
ampl
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6
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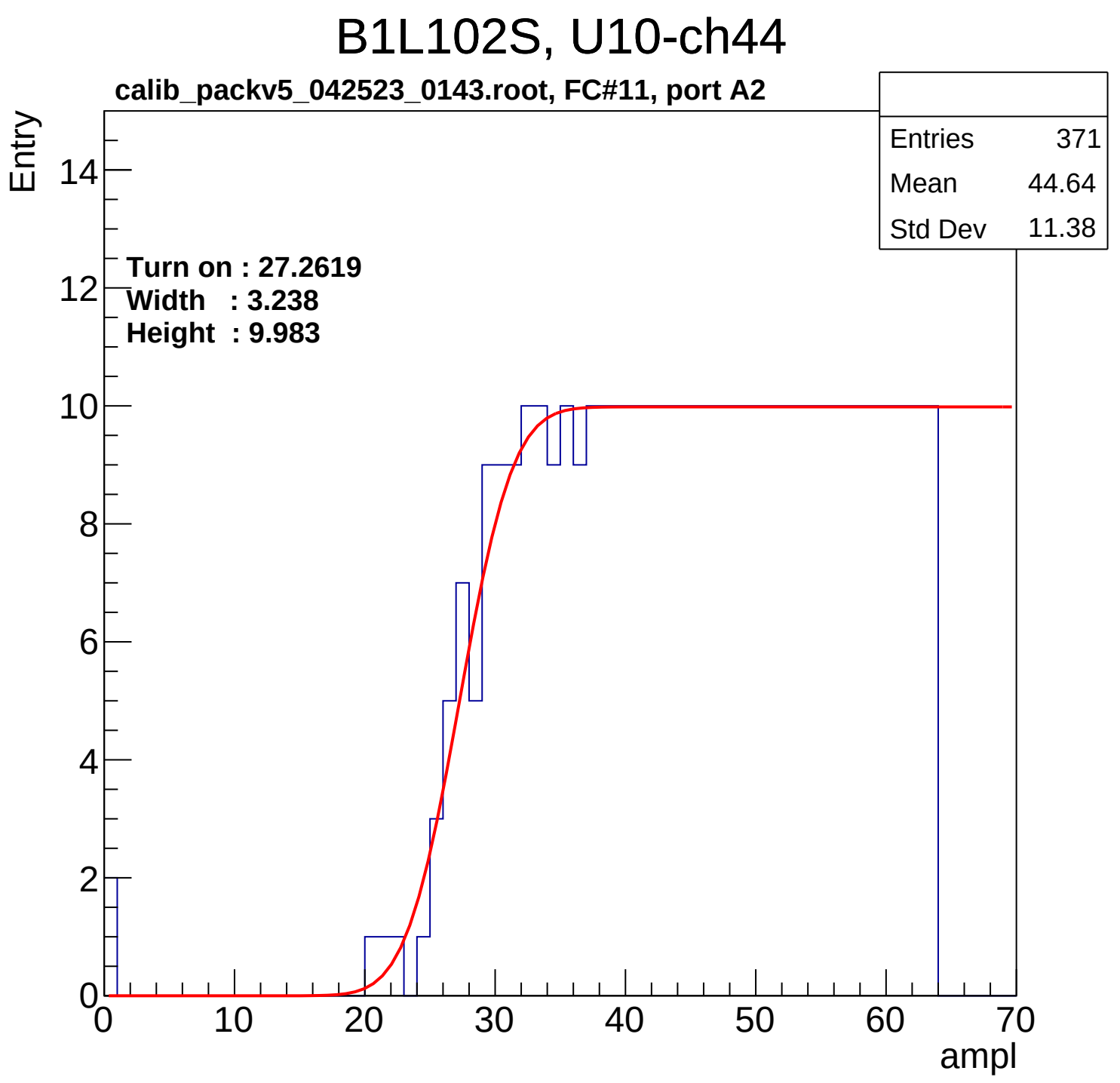
B1L102S, U10-ch44
calib_packv5_042523_0143.root, FC#11, port A2
Entries 371
Mean 44.64
Std Dev 11.38
Turn on : 27.2619
Width : 3.238
Height : 9.983
Entry
ampl
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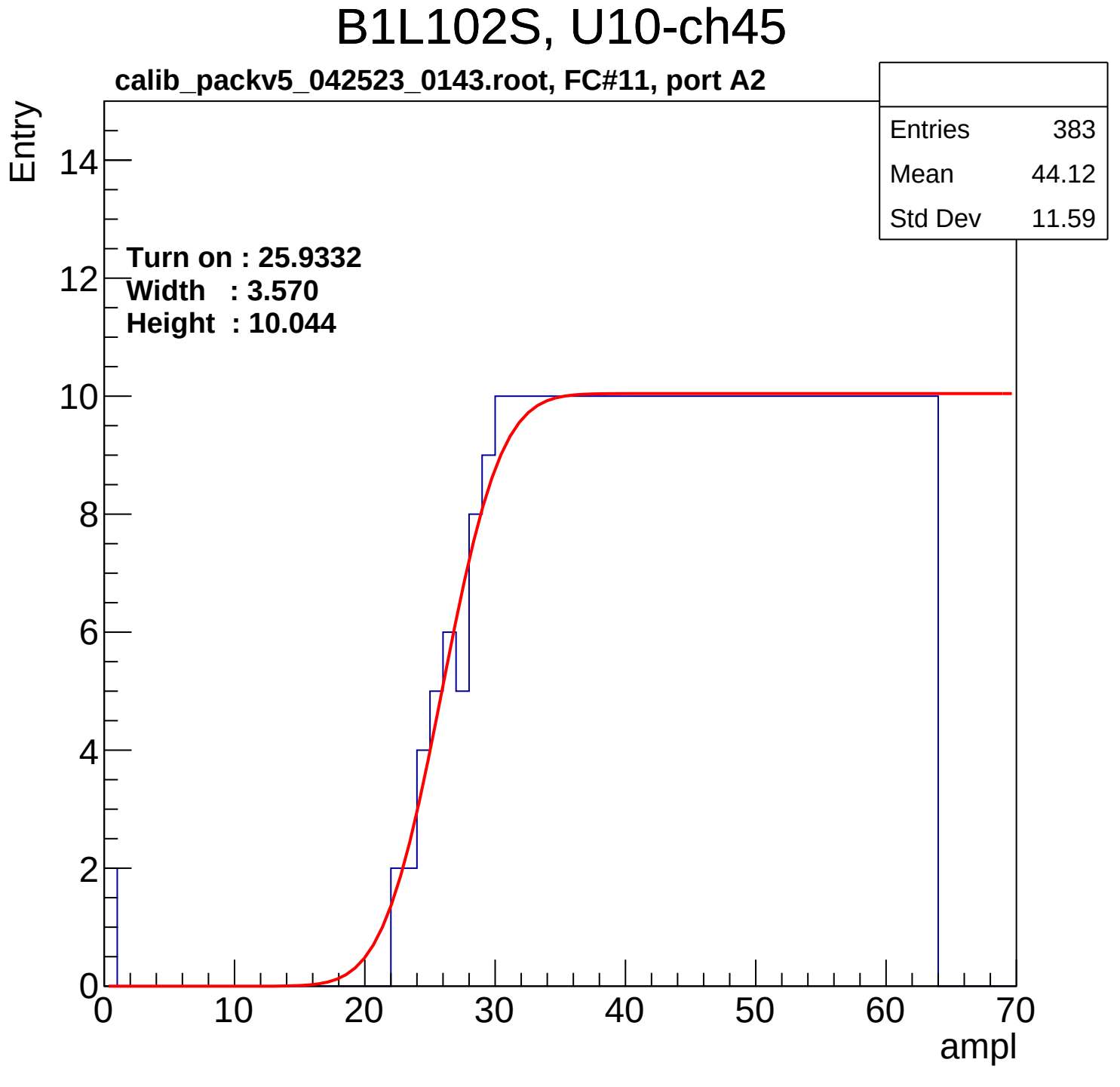
B1L102S, U10-ch45
calib_packv5_042523_0143.root, FC#11, port A2
Entries 383
Mean 44.12
Std Dev 11.59
Turn on : 25.9332
Width : 3.570
Height : 10.044
Entry
ampl
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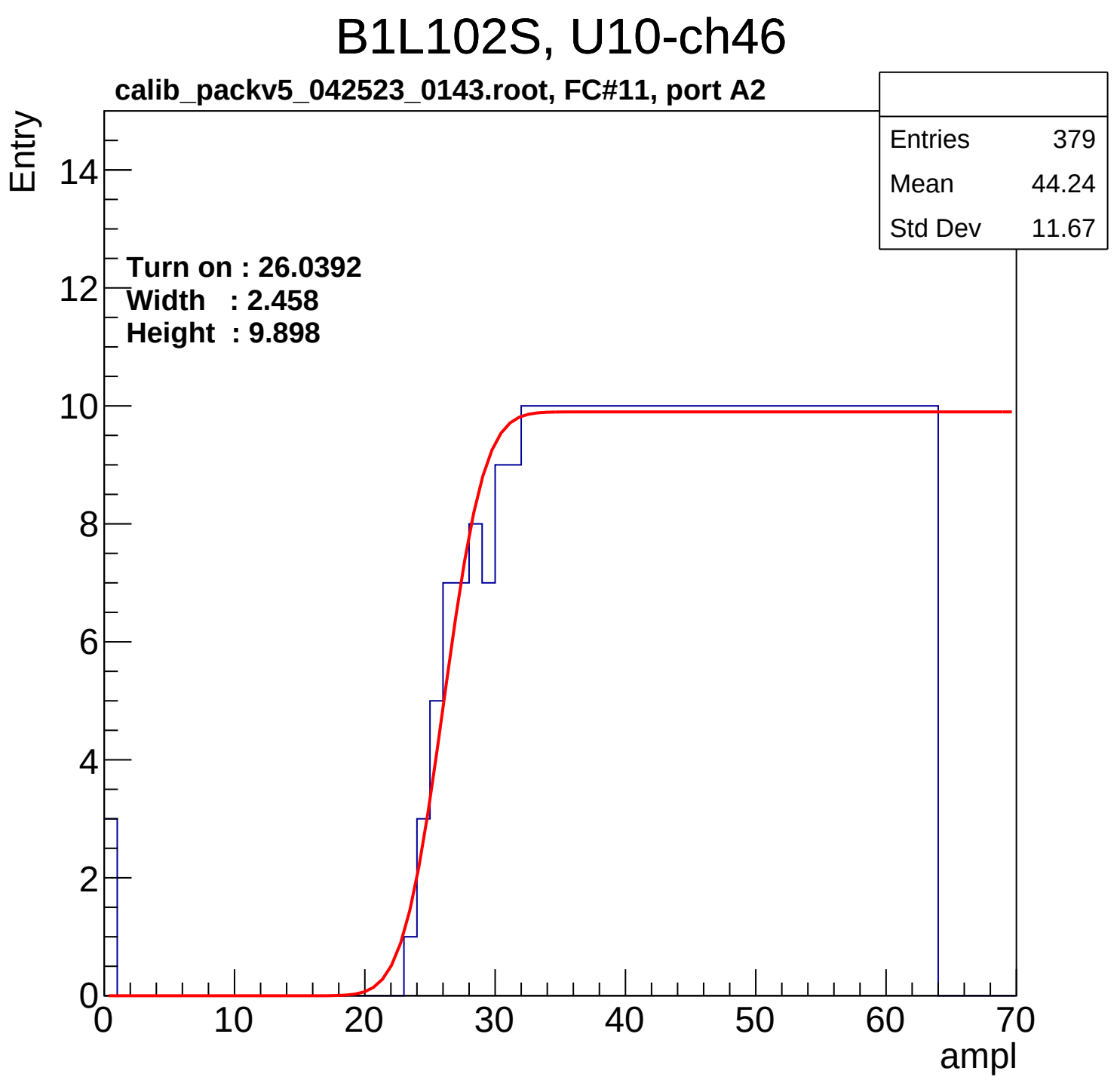
B1L102S, U10-ch46
calib_packv5_042523_0143.root, FC#11, port A2
Entries 379
Mean 44.24
Std Dev 11.67
Turn on : 26.0392
Width : 2.458
Height : 9.898
Entry
ampl
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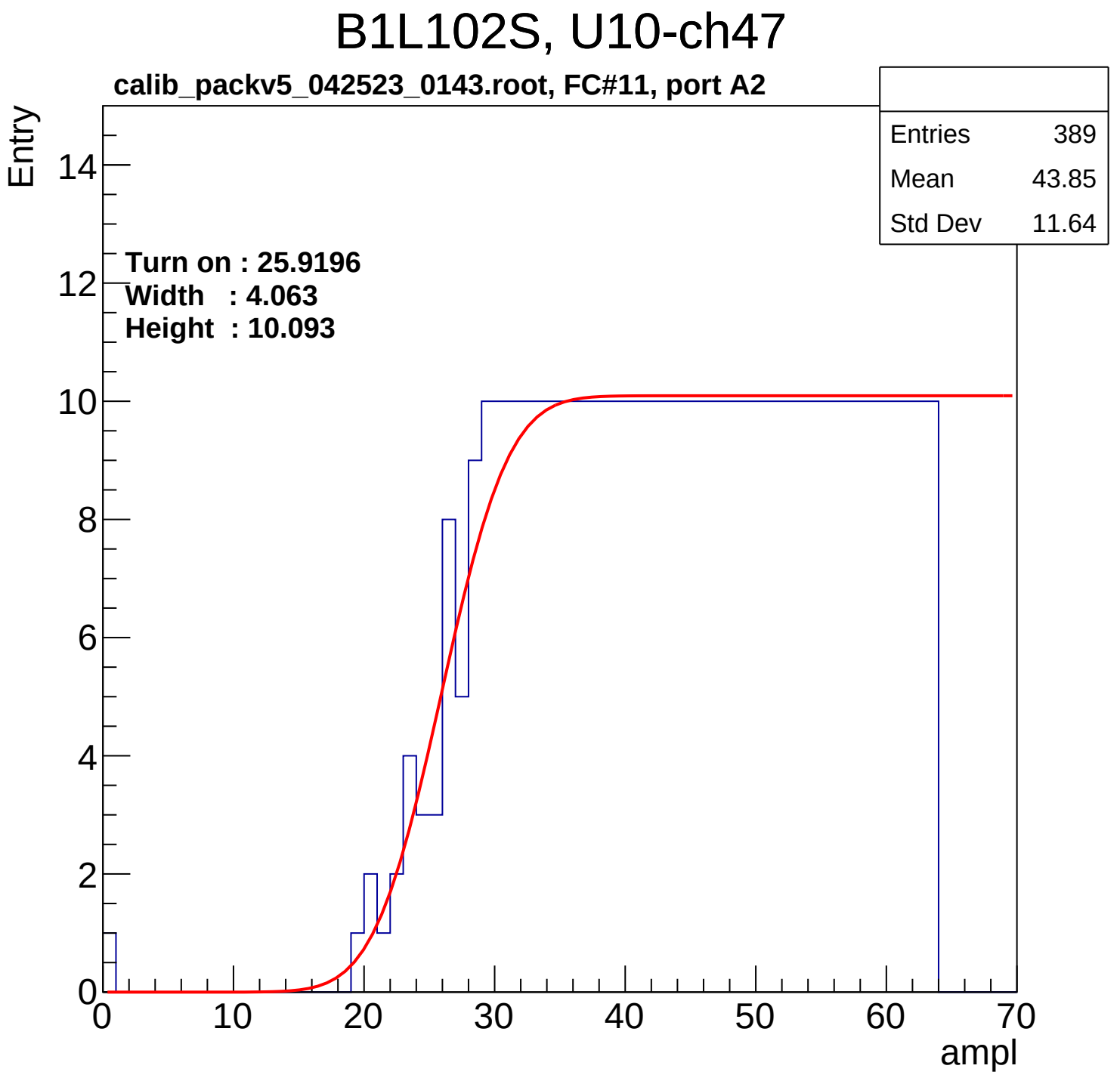
B1L102S, U10-ch47
calib_packv5_042523_0143.root, FC#11, port A2
Entries 389
Mean 43.85
Std Dev 11.64
Turn on : 25.9196
Width : 4.063
Height : 10.093
Entry
ampl
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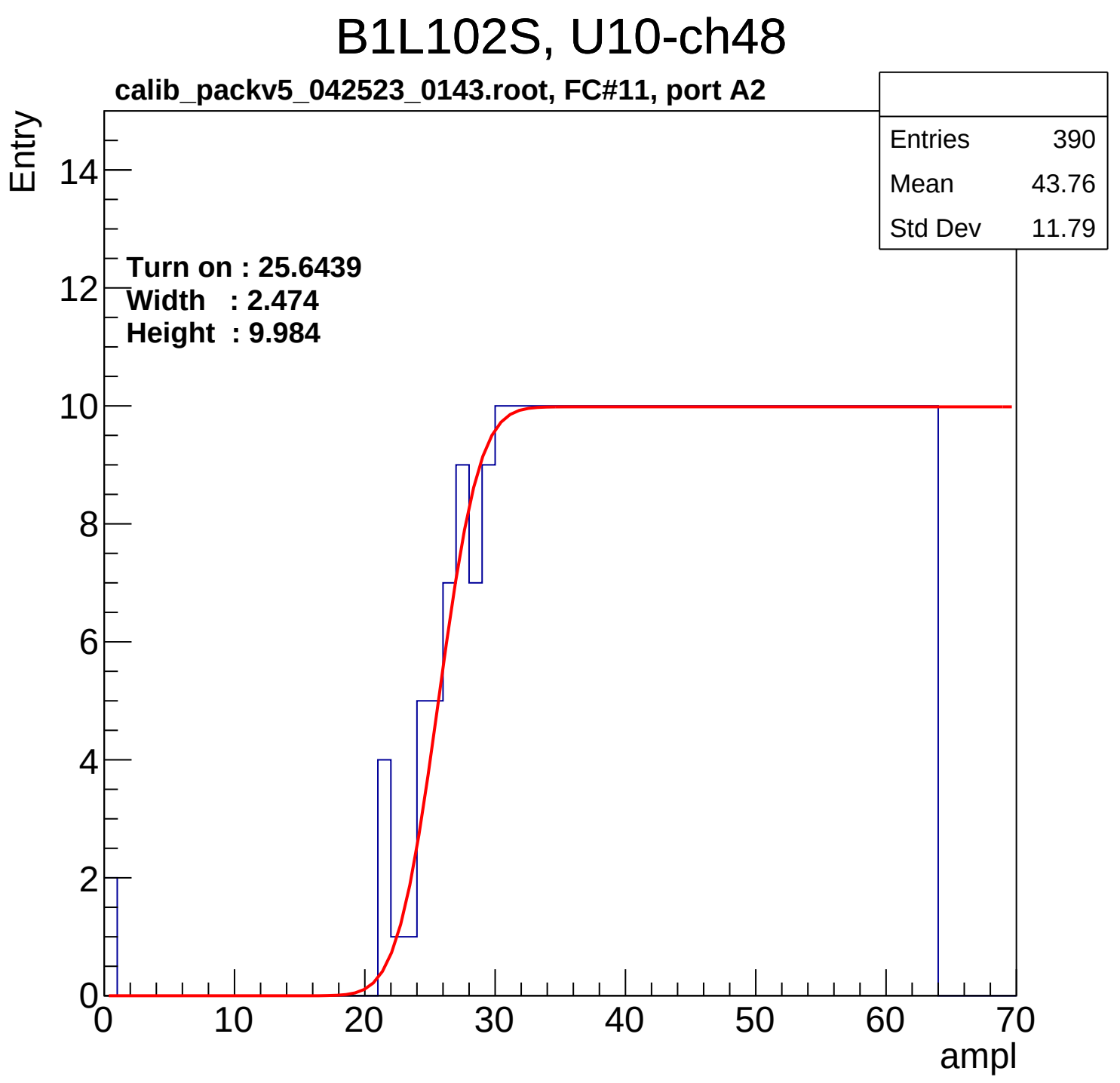
B1L102S, U10-ch48
calib_packv5_042523_0143.root, FC#11, port A2
Entries 390
Mean 43.76
Std Dev 11.79
Turn on : 25.6439
Width : 2.474
Height : 9.984
Entry
ampl
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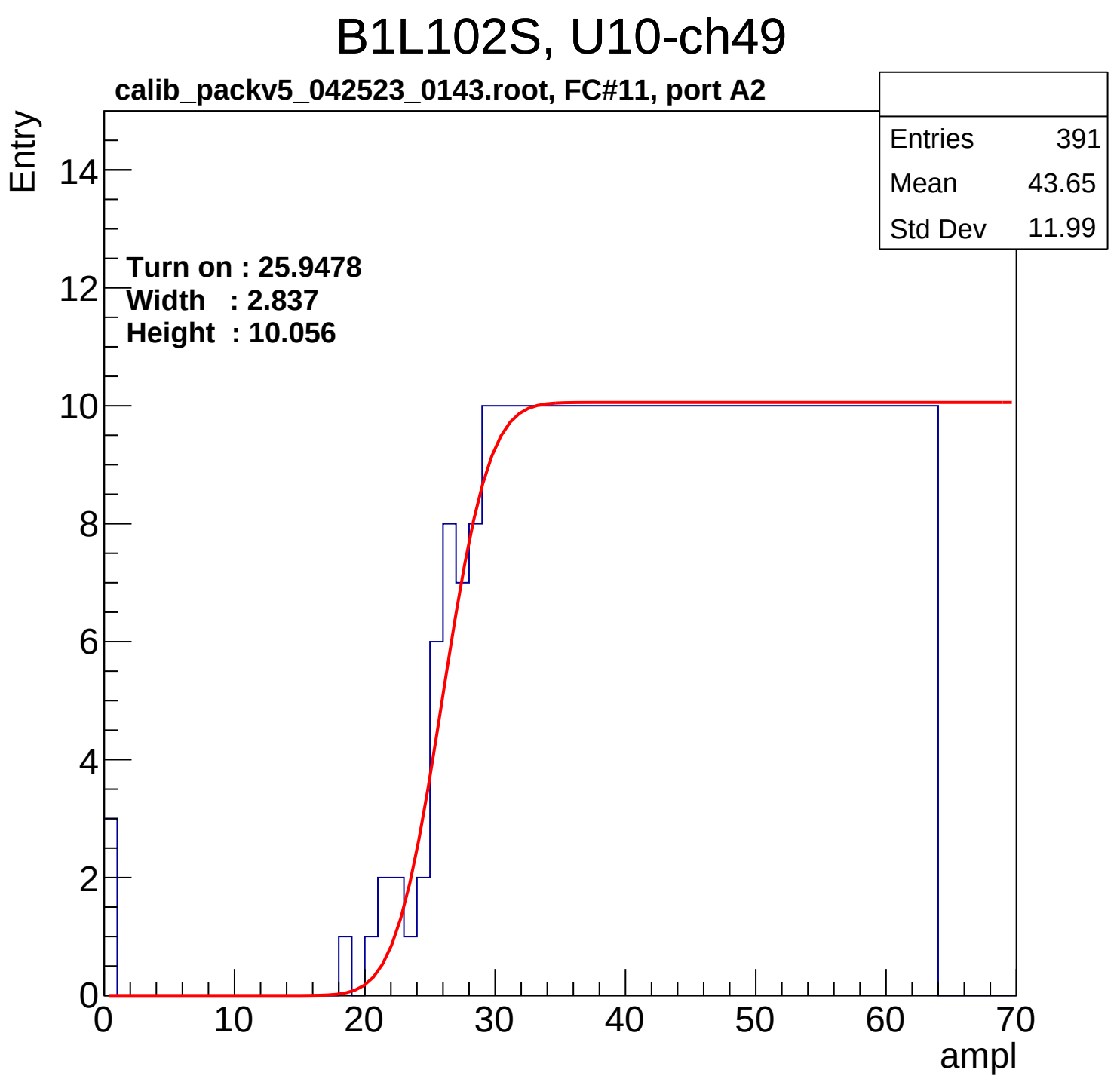
B1L102S, U10-ch49
calib_packv5_042523_0143.root, FC#11, port A2
Entries 391
Mean 43.65
Std Dev 11.99
Turn on : 25.9478
Width : 2.837
Height : 10.056
Entry
ampl
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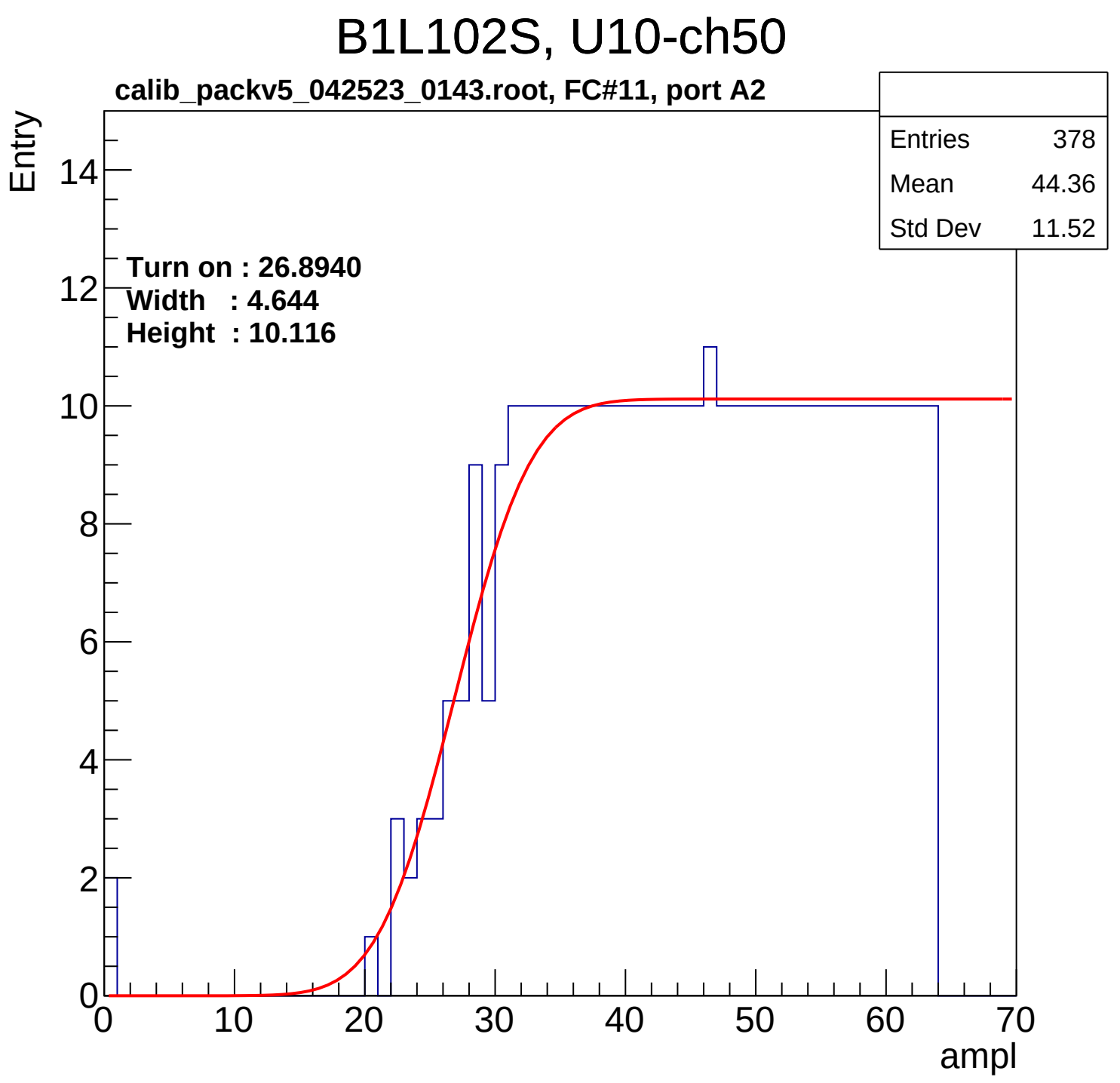
B1L102S, U10-ch50
calib_packv5_042523_0143.root, FC#11, port A2
Entries 378
Mean 44.36
Std Dev 11.52
Turn on : 26.8940
Width : 4.644
Height : 10.116
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ampl
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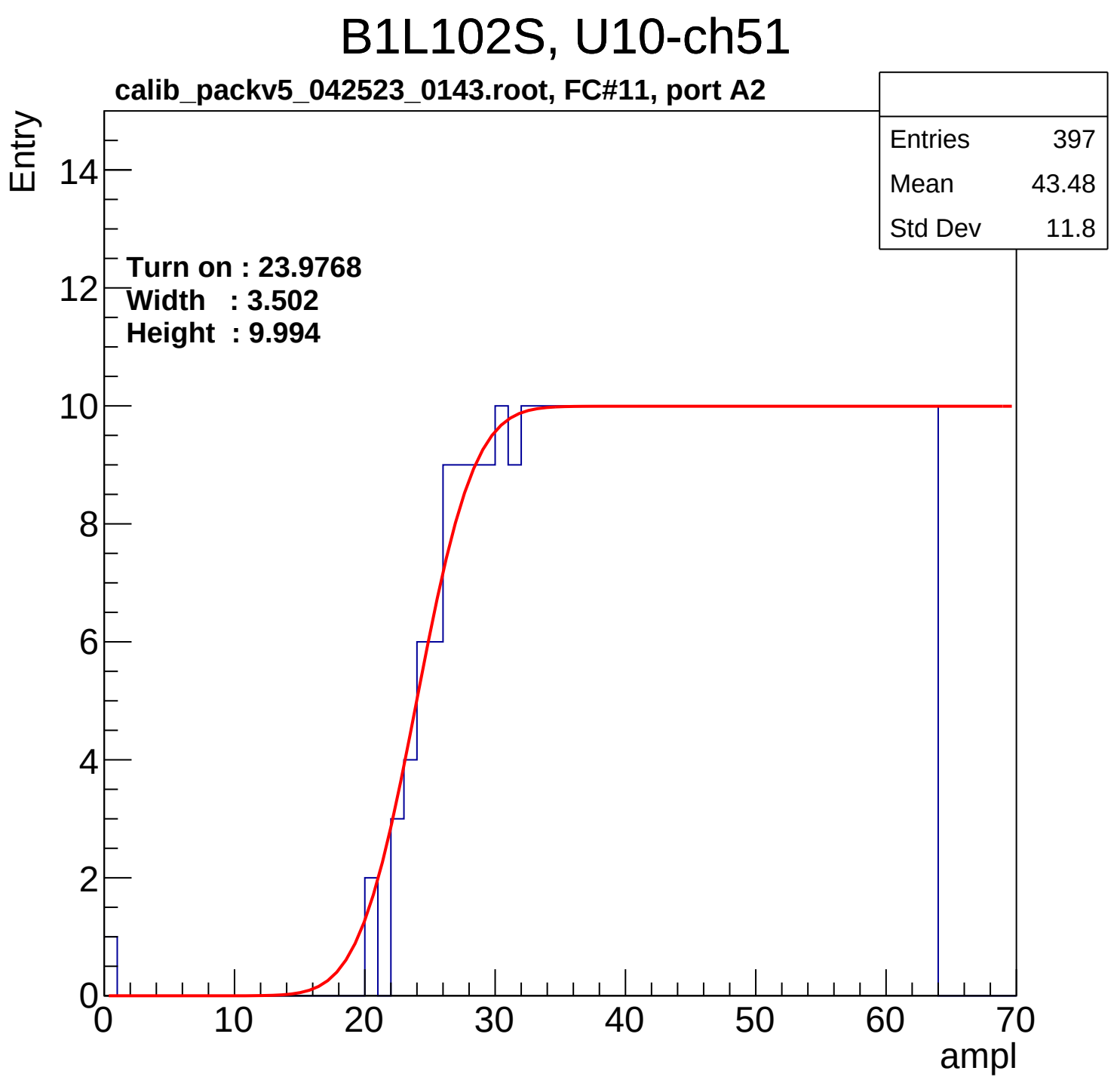
B1L102S, U10-ch51
calib_packv5_042523_0143.root, FC#11, port A2
Entries 397
Mean 43.48
Std Dev 11.8
Turn on : 23.9768
Width : 3.502
Height : 9.994
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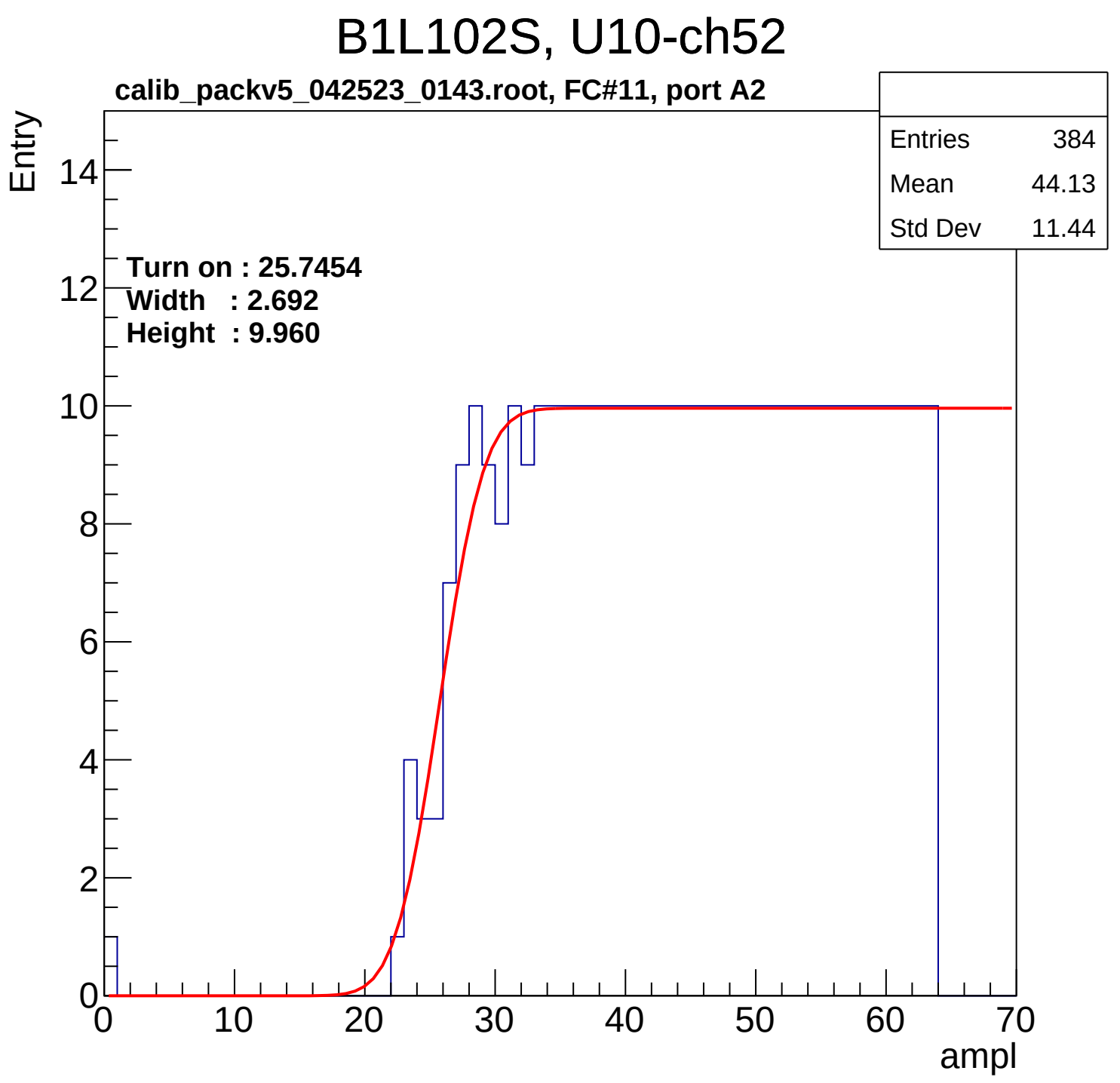
B1L102S, U10-ch52
calib_packv5_042523_0143.root, FC#11, port A2
Entries 384
Mean 44.13
Std Dev 11.44
Turn on : 25.7454
Width : 2.692
Height : 9.960
Entry
ampl
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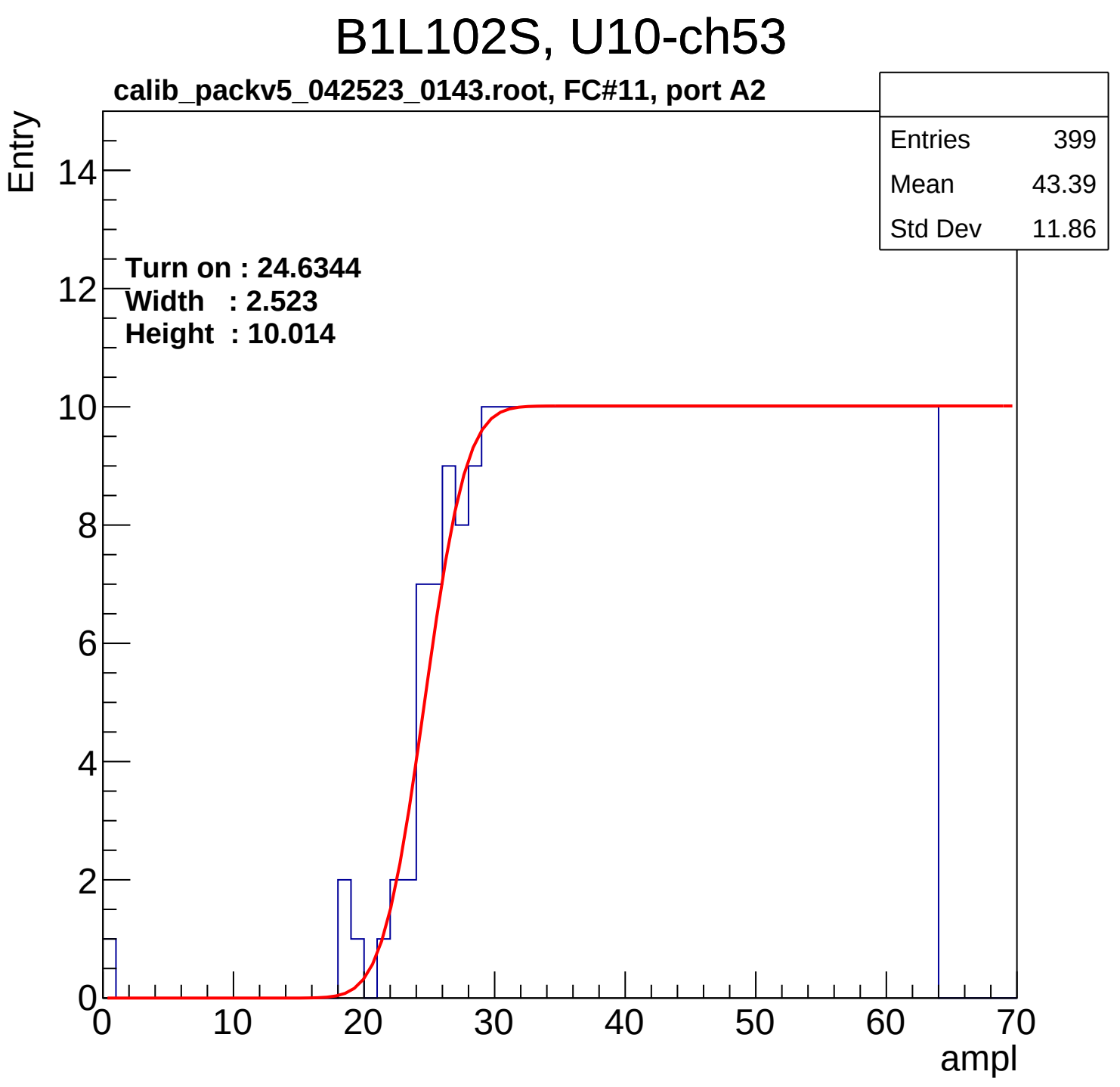
B1L102S, U10-ch53
calib_packv5_042523_0143.root, FC#11, port A2
Entries 399
Mean 43.39
Std Dev 11.86
Turn on : 24.6344
Width : 2.523
Height : 10.014
Entry
ampl
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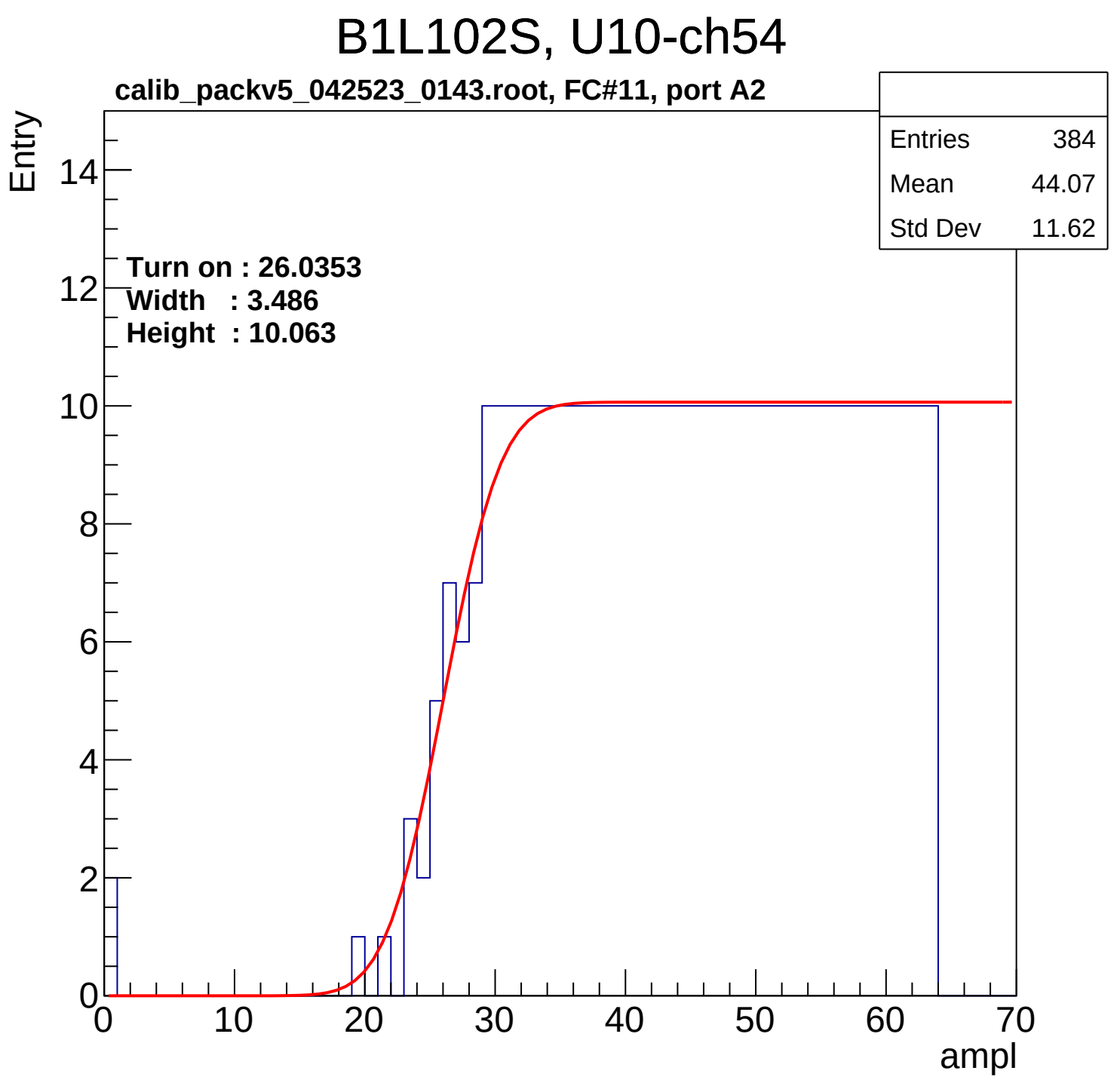
B1L102S, U10-ch54
calib_packv5_042523_0143.root, FC#11, port A2
Entries 384
Mean 44.07
Std Dev 11.62
Turn on : 26.0353
Width : 3.486
Height : 10.063
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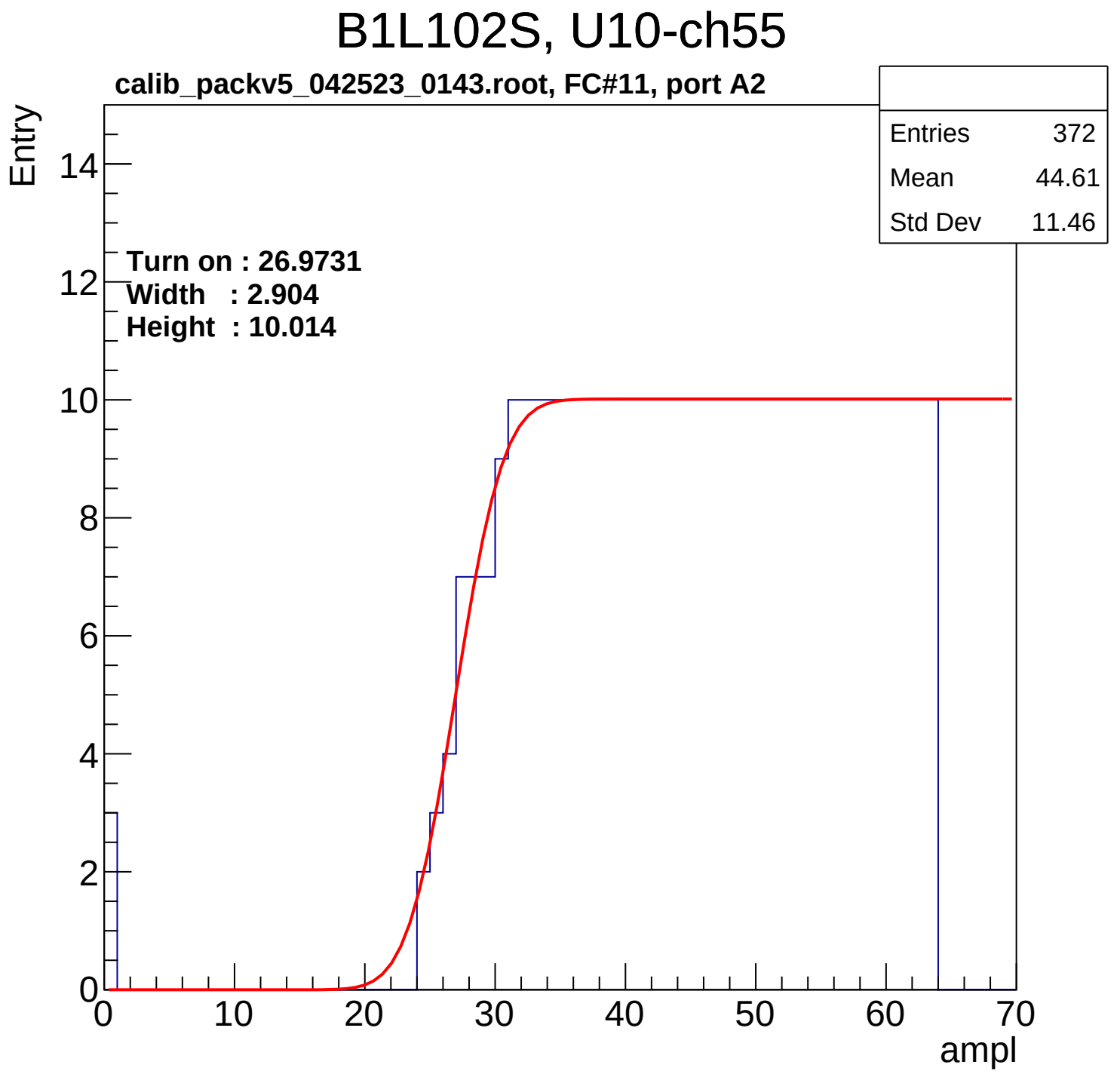
B1L102S, U10-ch55
calib_packv5_042523_0143.root, FC#11, port A2
Entries 372
Mean 44.61
Std Dev 11.46
Turn on : 26.9731
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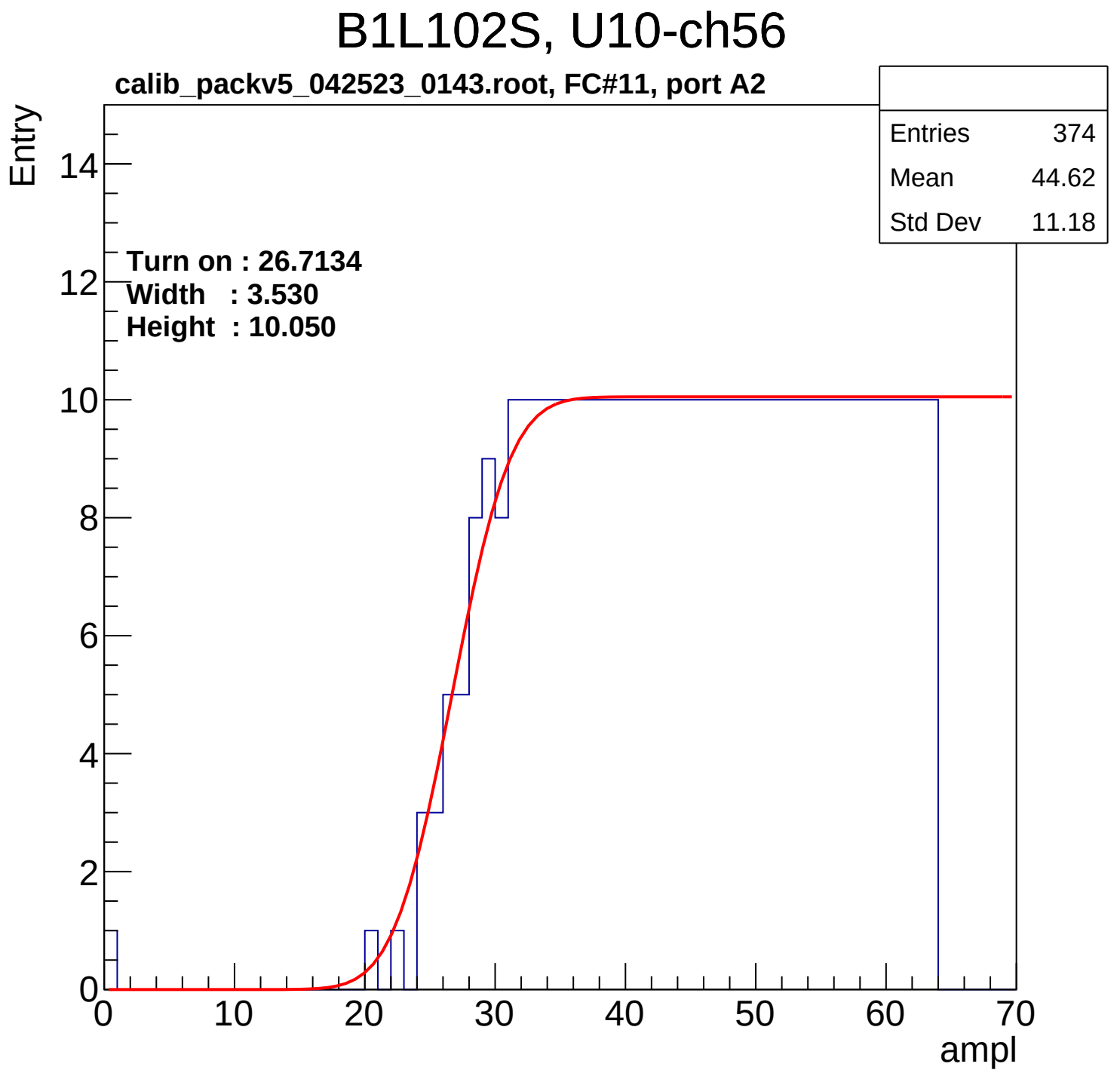
B1L102S, U10-ch56
calib_packv5_042523_0143.root, FC#11, port A2
Entries 374
Mean 44.62
Std Dev 11.18
Turn on : 26.7134
Width : 3.530
Height : 10.050
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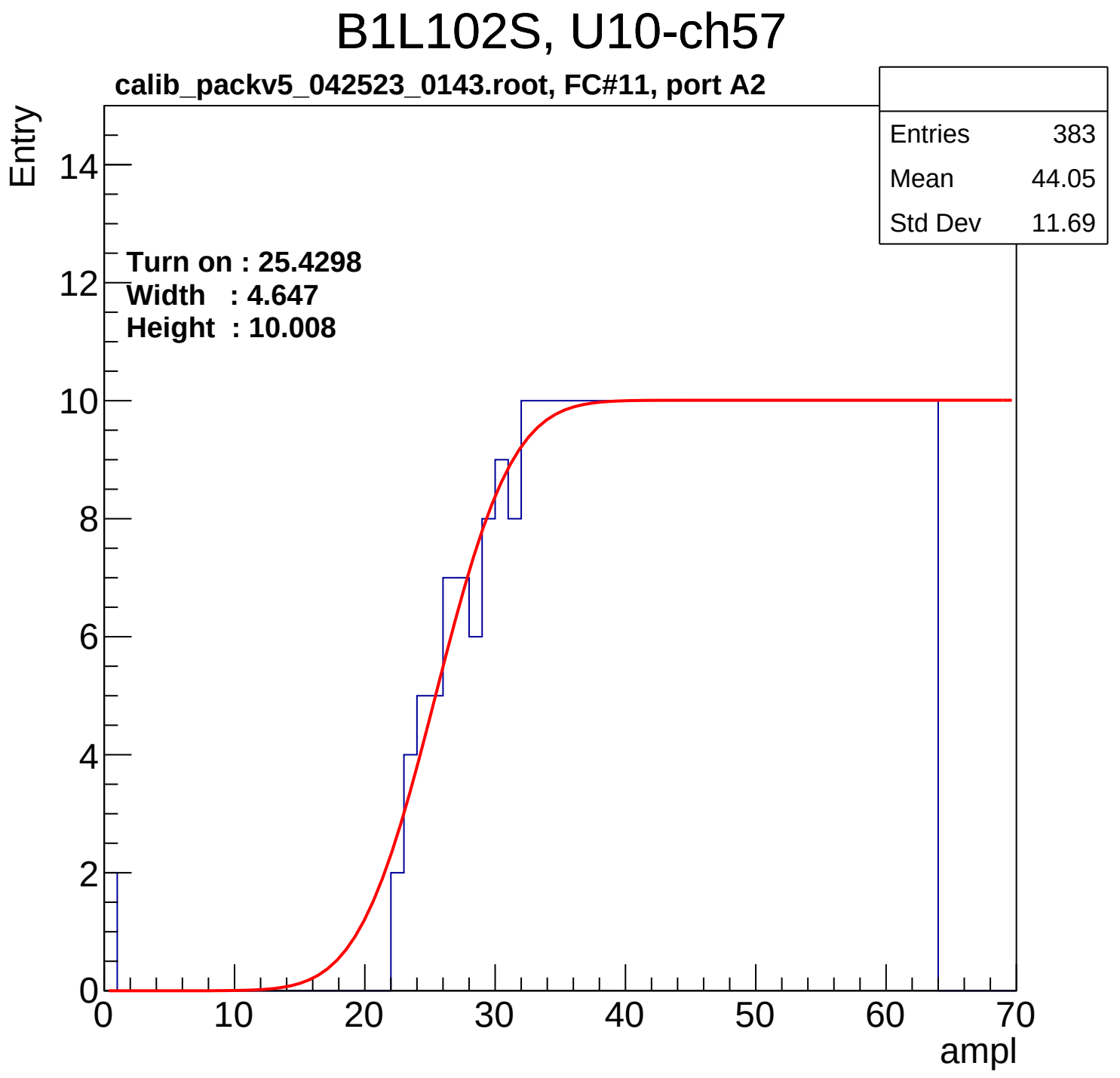
B1L102S, U10-ch57
calib_packv5_042523_0143.root, FC#11, port A2
Entries 383
Mean 44.05
Std Dev 11.69
Turn on : 25.4298
Width : 4.647
Height : 10.008
Entry
ampl
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4
6
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10
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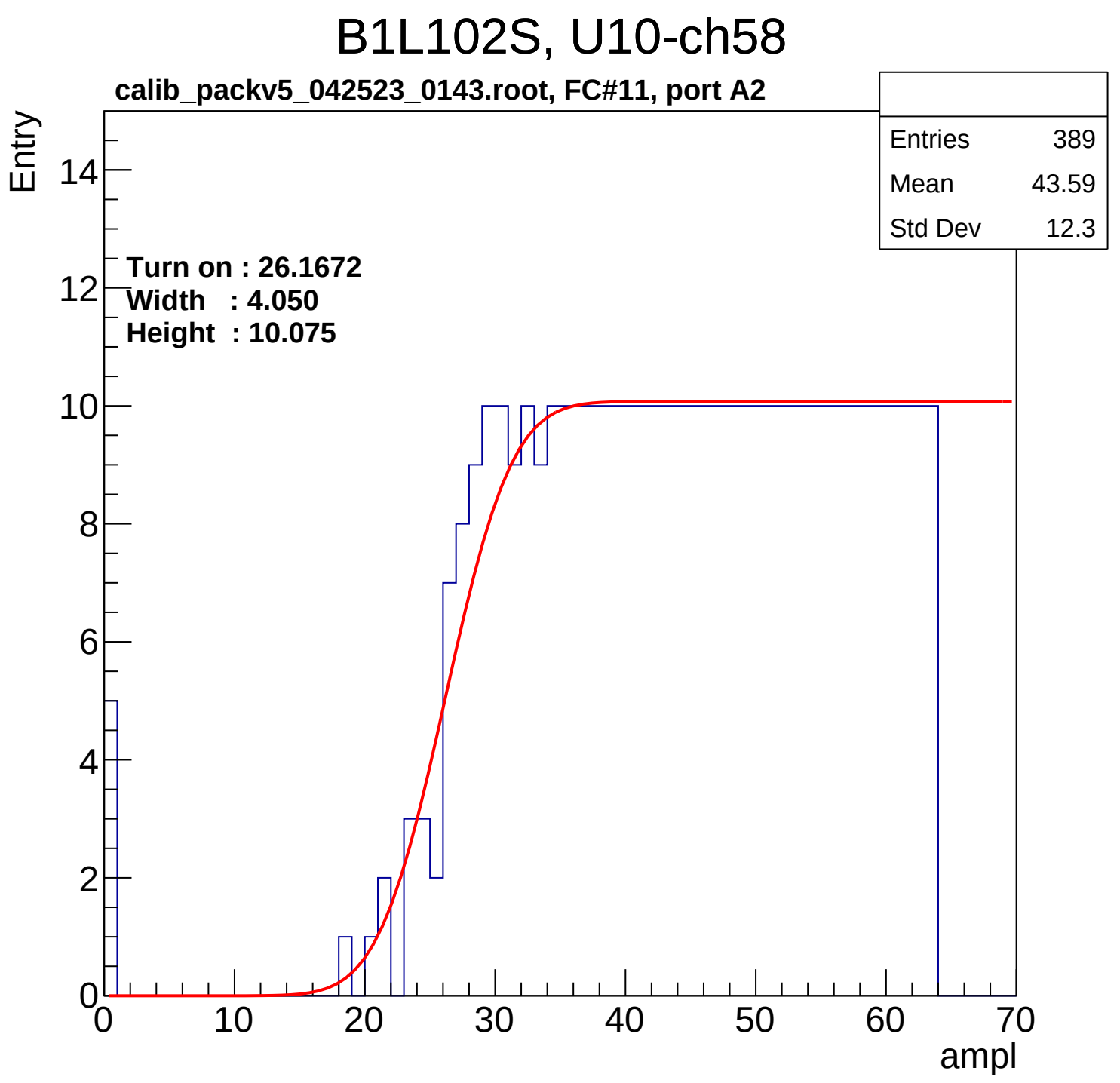
B1L102S, U10-ch58
calib_packv5_042523_0143.root, FC#11, port A2
Entries 389
Mean 43.59
Std Dev 12.3
Turn on : 26.1672
Width : 4.050
Height : 10.075
Entry
ampl
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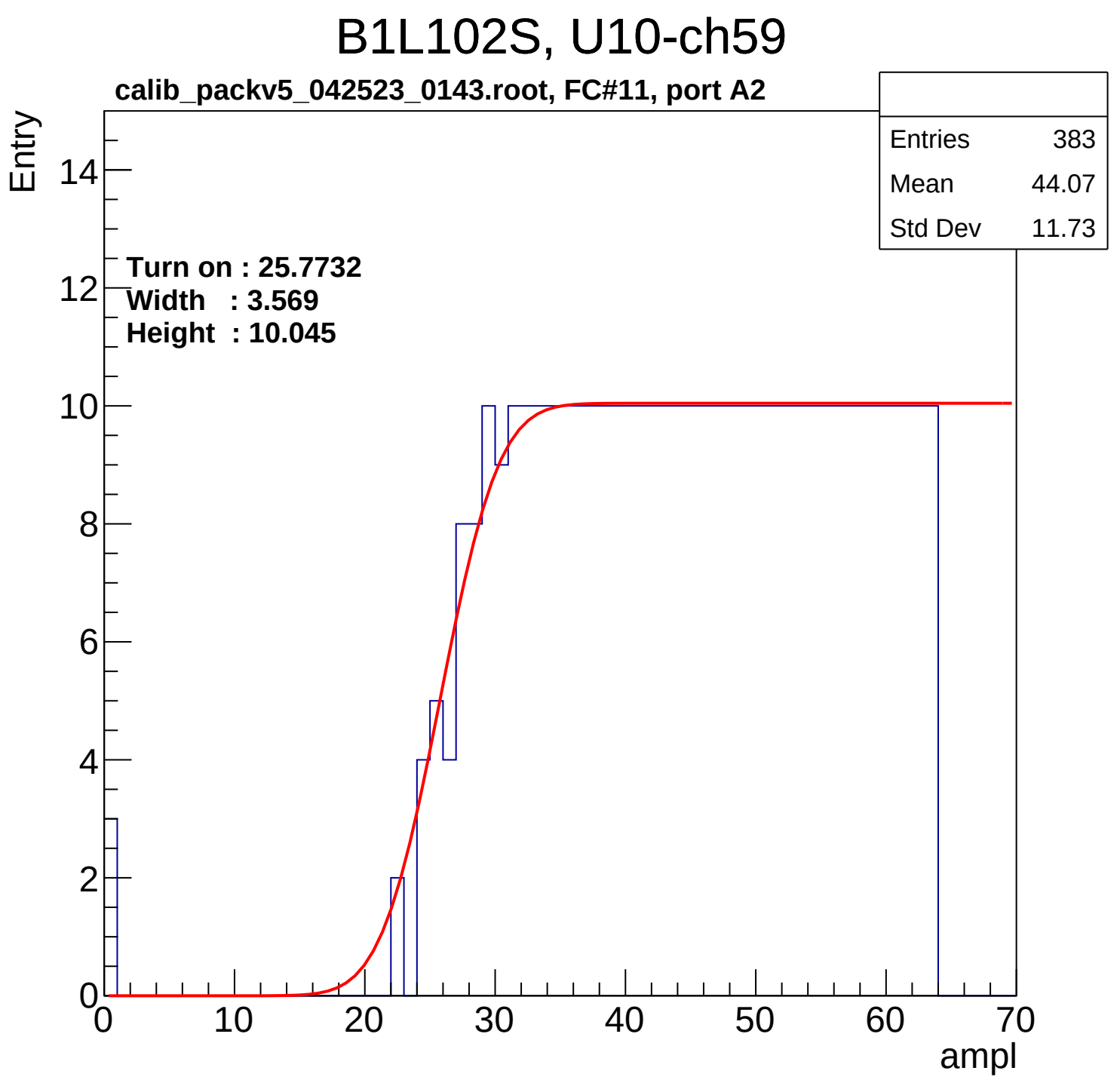
B1L102S, U10-ch59
calib_packv5_042523_0143.root, FC#11, port A2
Entries 383
Mean 44.07
Std Dev 11.73
Turn on : 25.7732
Width : 3.569
Height : 10.045
Entry
ampl
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4
6
8
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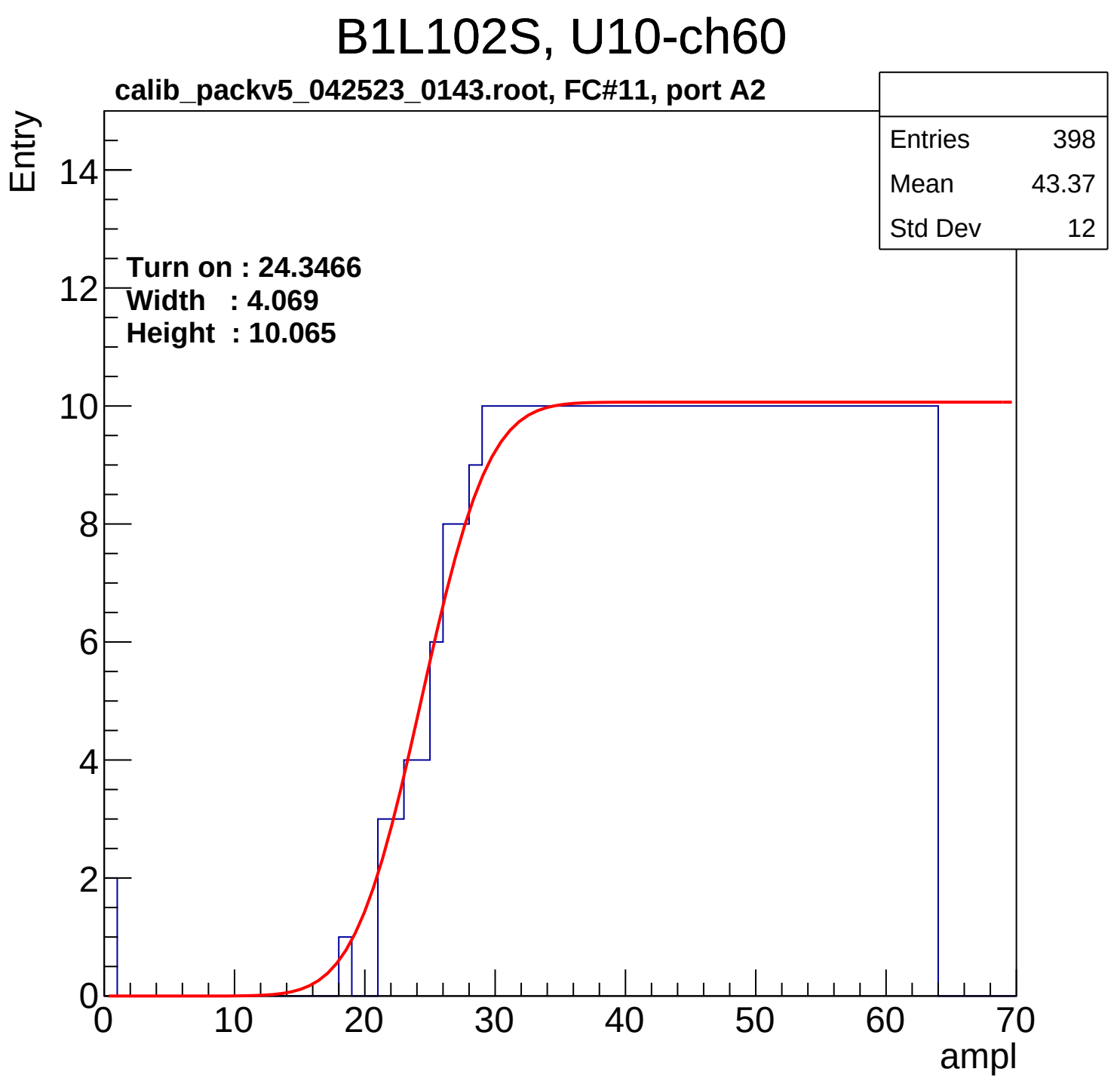
B1L102S, U10-ch60
calib_packv5_042523_0143.root, FC#11, port A2
Entries 398
Mean 43.37
Std Dev 12
Turn on : 24.3466
Width : 4.069
Height : 10.065
Entry
ampl
0
2
4
6
8
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12
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40
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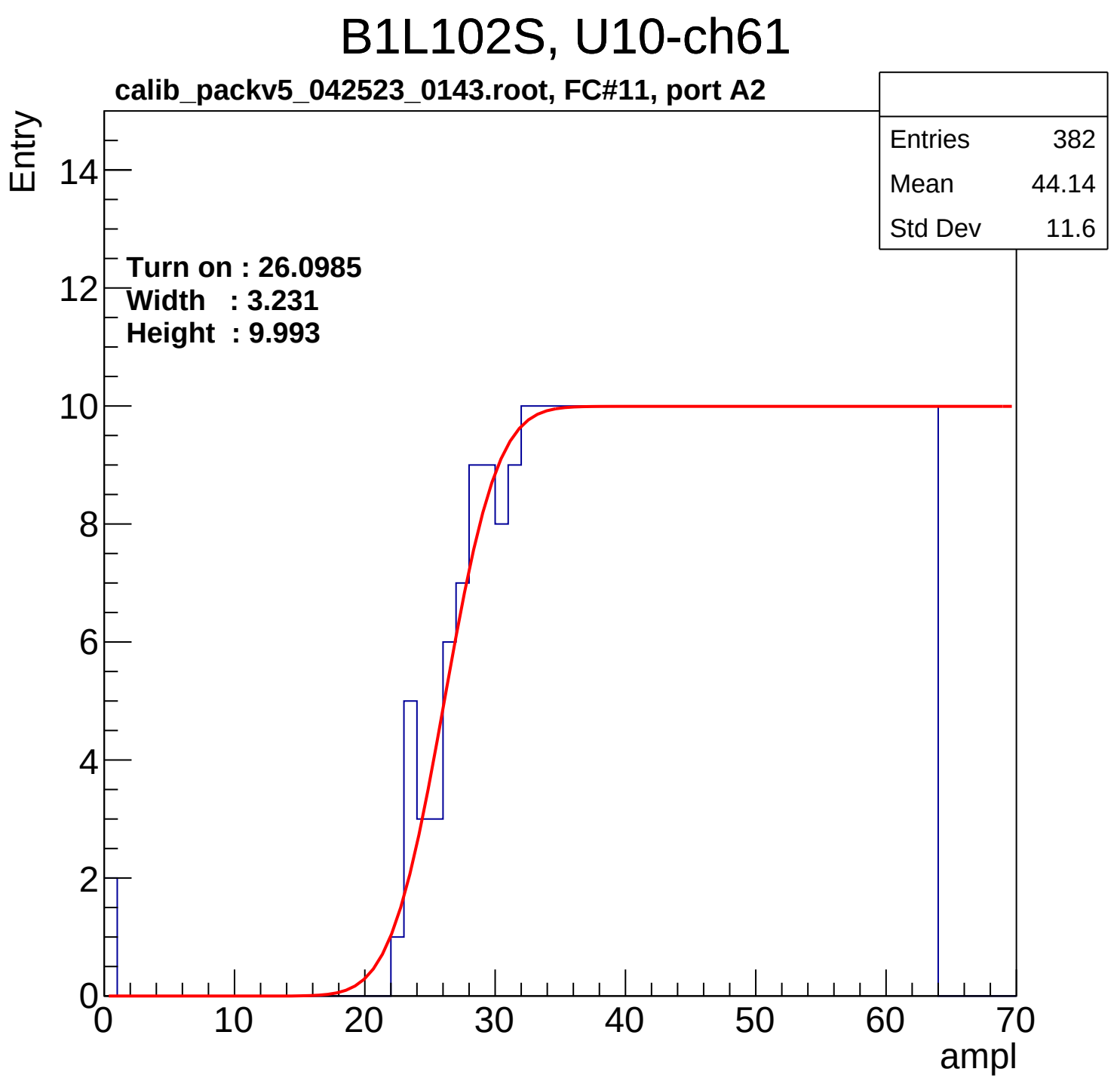
B1L102S, U10-ch61
calib_packv5_042523_0143.root, FC#11, port A2
Entries 382
Mean 44.14
Std Dev 11.6
Turn on : 26.0985
Width : 3.231
Height : 9.993
Entry
ampl
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2
4
6
8
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0
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60
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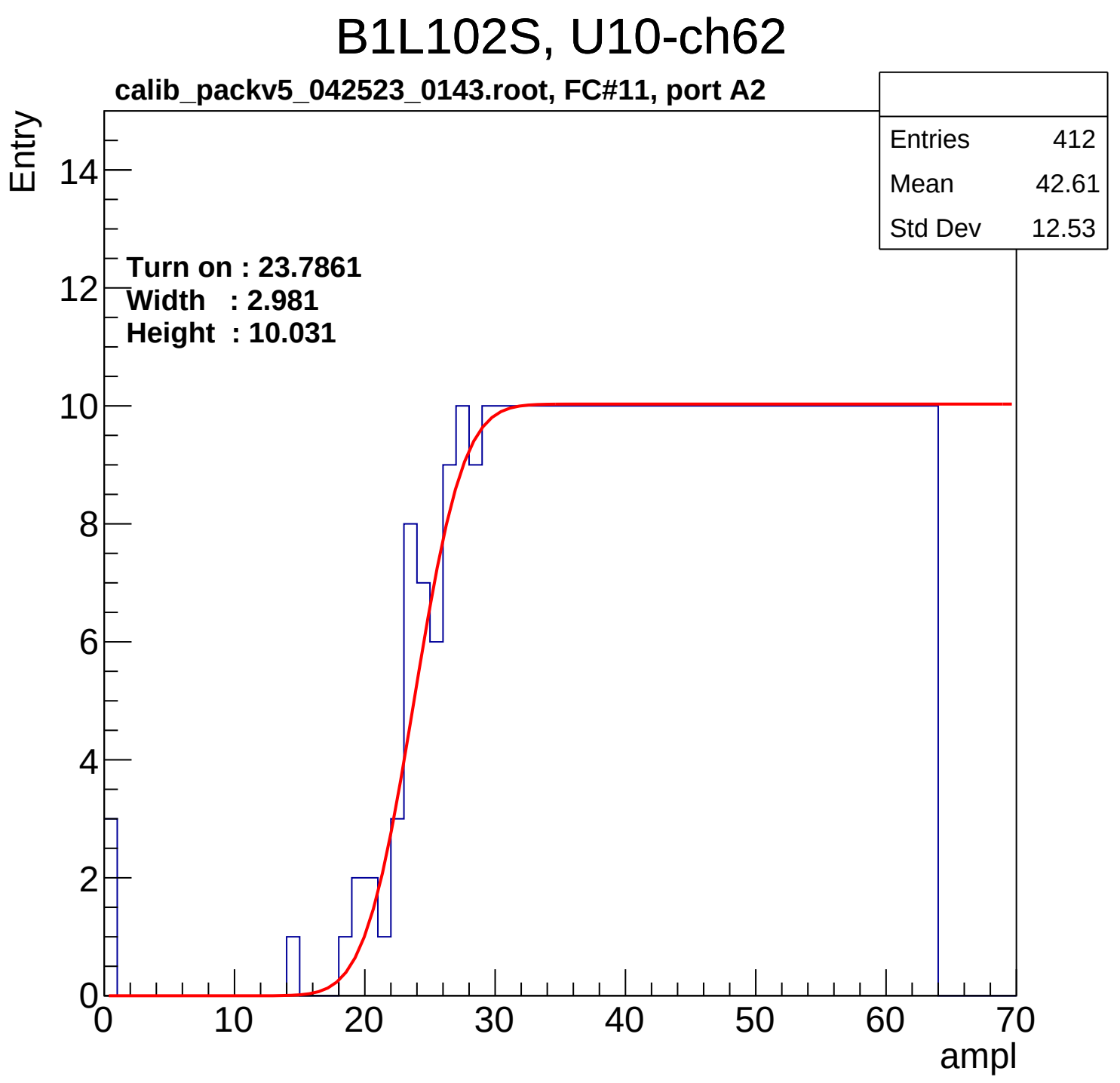
B1L102S, U10-ch62
calib_packv5_042523_0143.root, FC#11, port A2
Entries 412
Mean 42.61
Std Dev 12.53
Turn on : 23.7861
Width : 2.981
Height : 10.031
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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60
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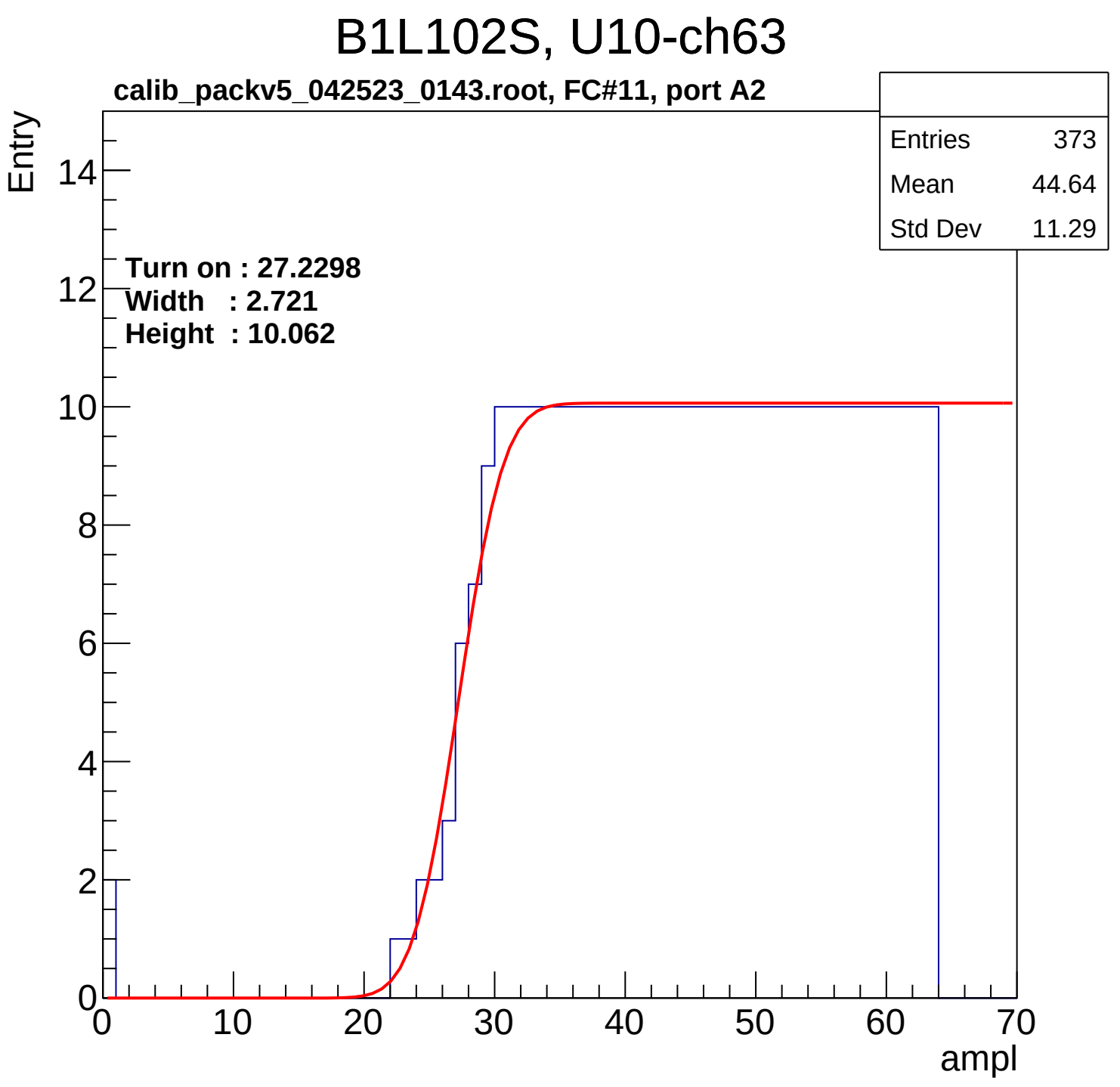
B1L102S, U10-ch63
calib_packv5_042523_0143.root, FC#11, port A2
Entries 373
Mean 44.64
Std Dev 11.29
Turn on : 27.2298
Width : 2.721
Height : 10.062
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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40
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60
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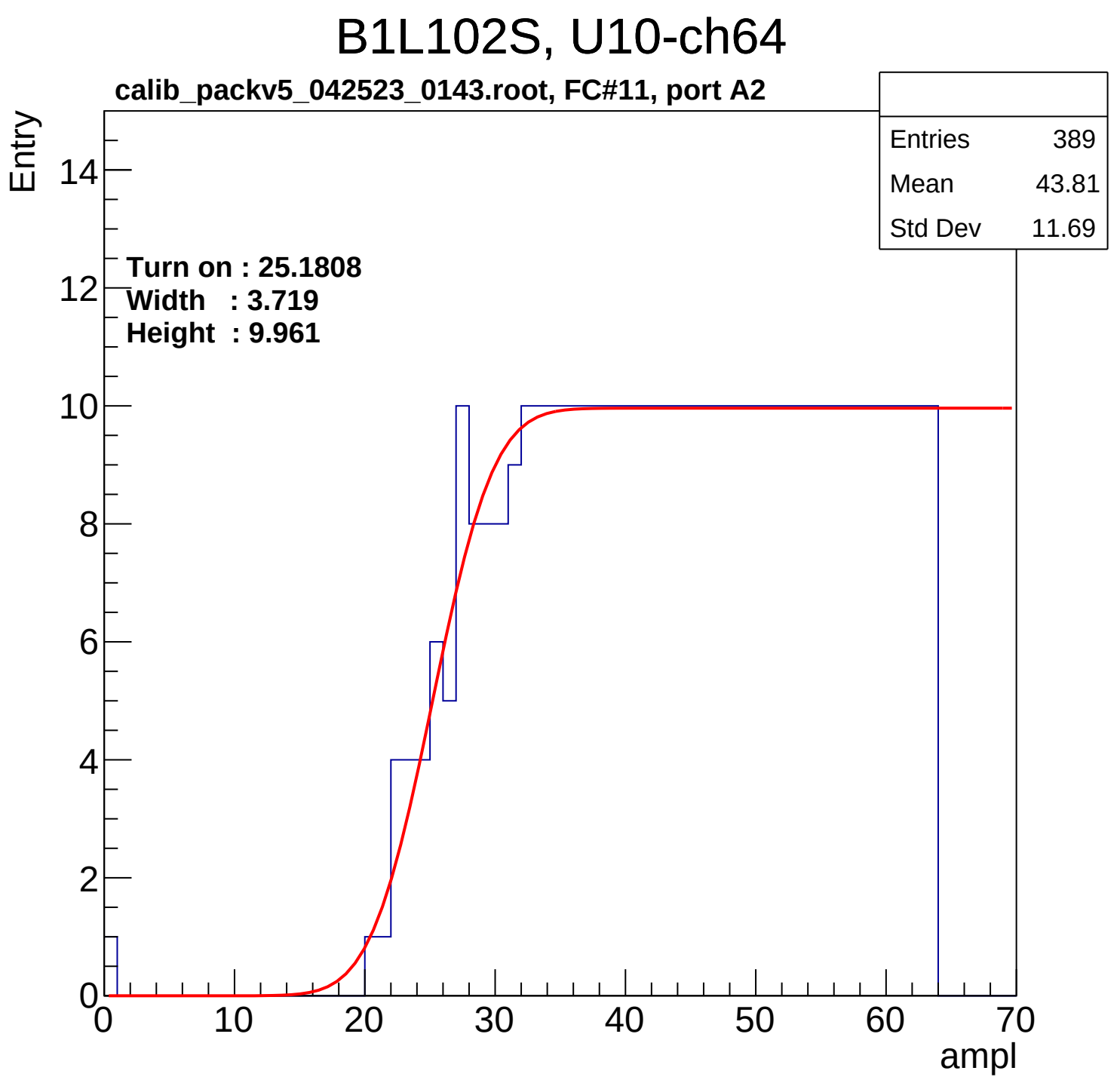
B1L102S, U10-ch64
calib_packv5_042523_0143.root, FC#11, port A2
Entries 389
Mean 43.81
Std Dev 11.69
Turn on : 25.1808
Width : 3.719
Height : 9.961
Entry
ampl
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2
4
6
8
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0
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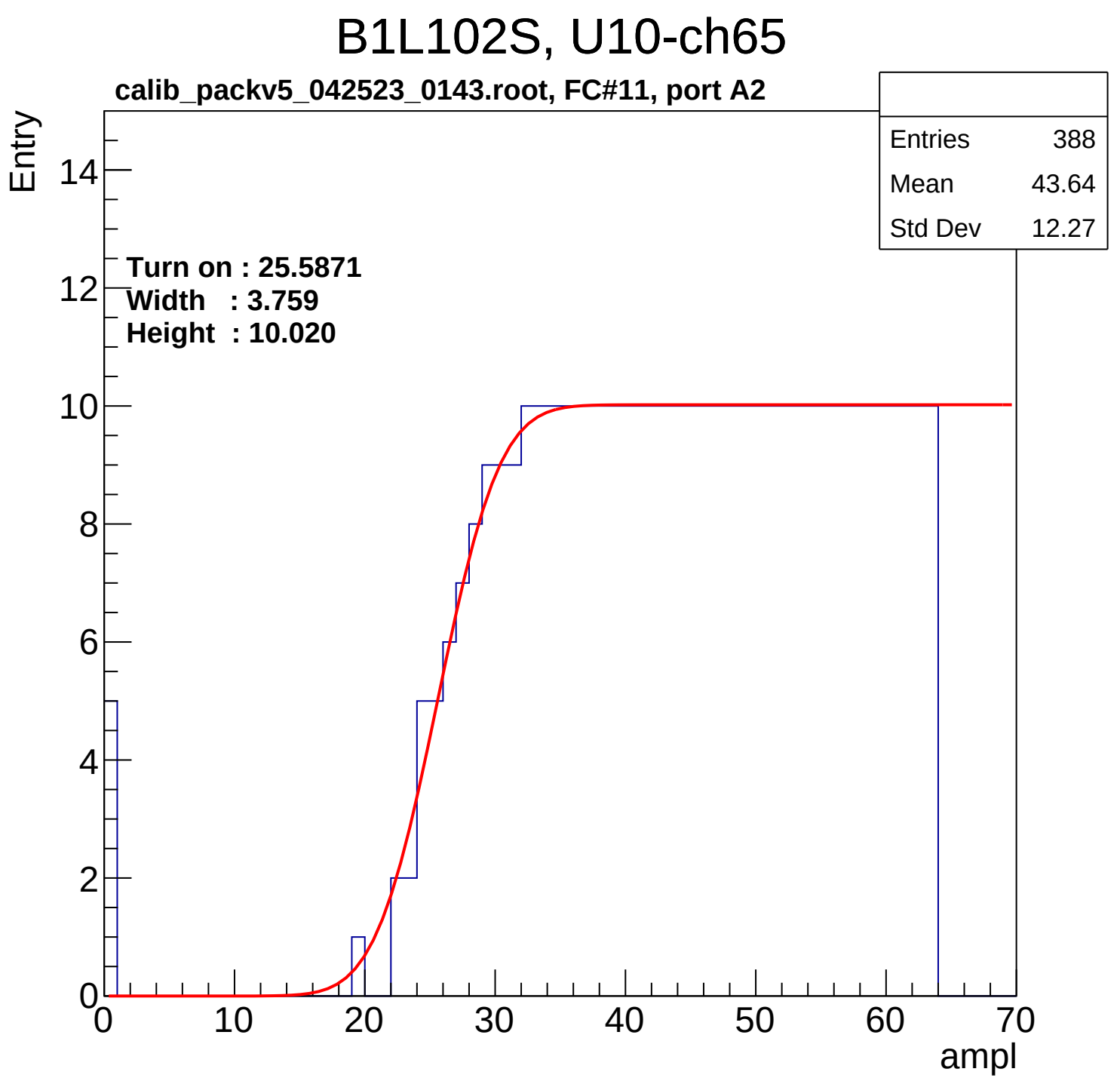
B1L102S, U10-ch65
calib_packv5_042523_0143.root, FC#11, port A2
Entries 388
Mean 43.64
Std Dev 12.27
Turn on : 25.5871
Width : 3.759
Height : 10.020
Entry
ampl
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2
4
6
8
10
12
14
0
10
20
30
40
50
60
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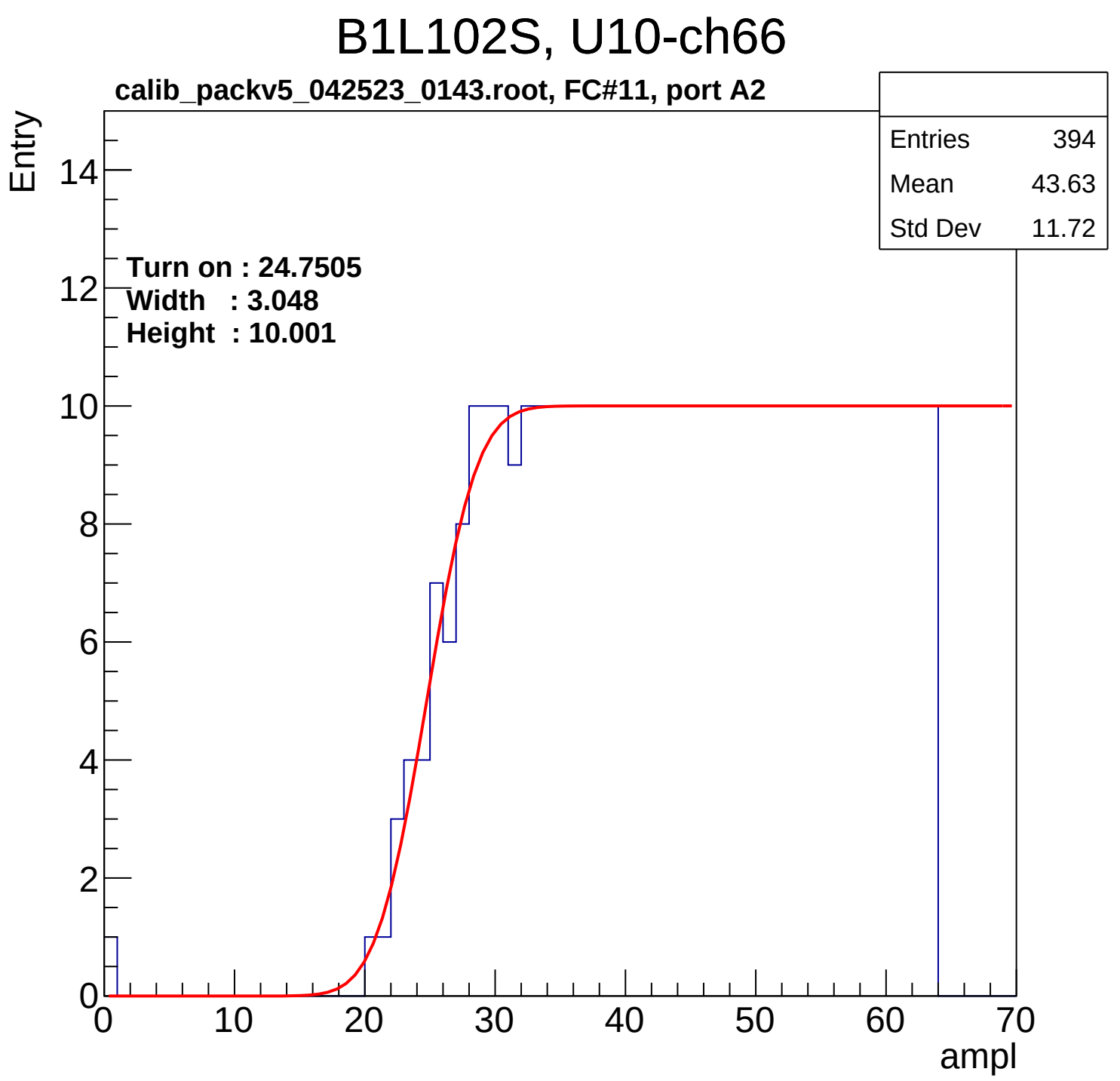
B1L102S, U10-ch66
calib_packv5_042523_0143.root, FC#11, port A2
Entries 394
Mean 43.63
Std Dev 11.72
Turn on : 24.7505
Width : 3.048
Height : 10.001
Entry
ampl
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6
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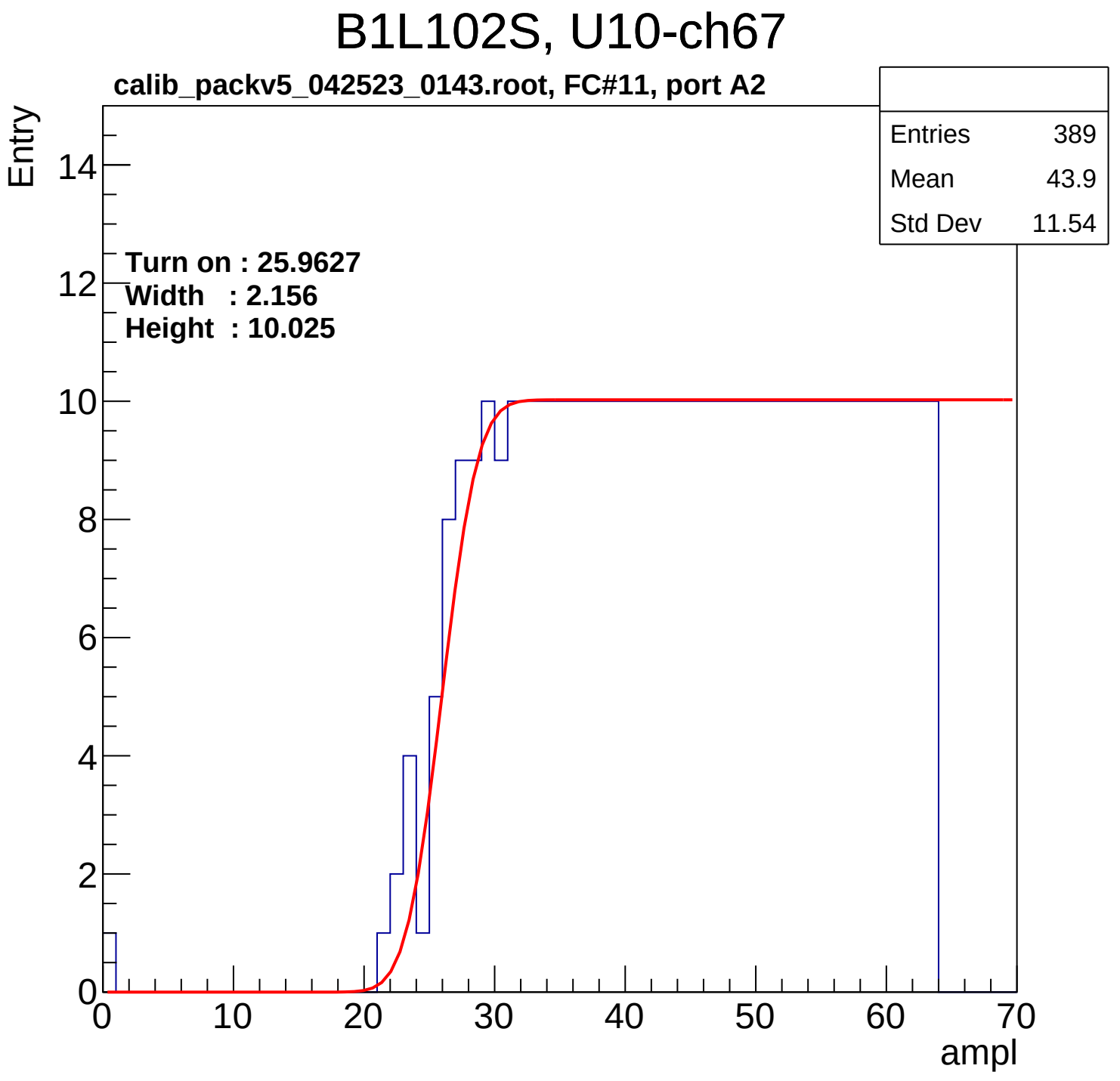
B1L102S, U10-ch67
calib_packv5_042523_0143.root, FC#11, port A2
Entries 389
Mean 43.9
Std Dev 11.54
Turn on : 25.9627
Width : 2.156
Height : 10.025
Entry
ampl
0
2
4
6
8
10
12
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0
10
20
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60
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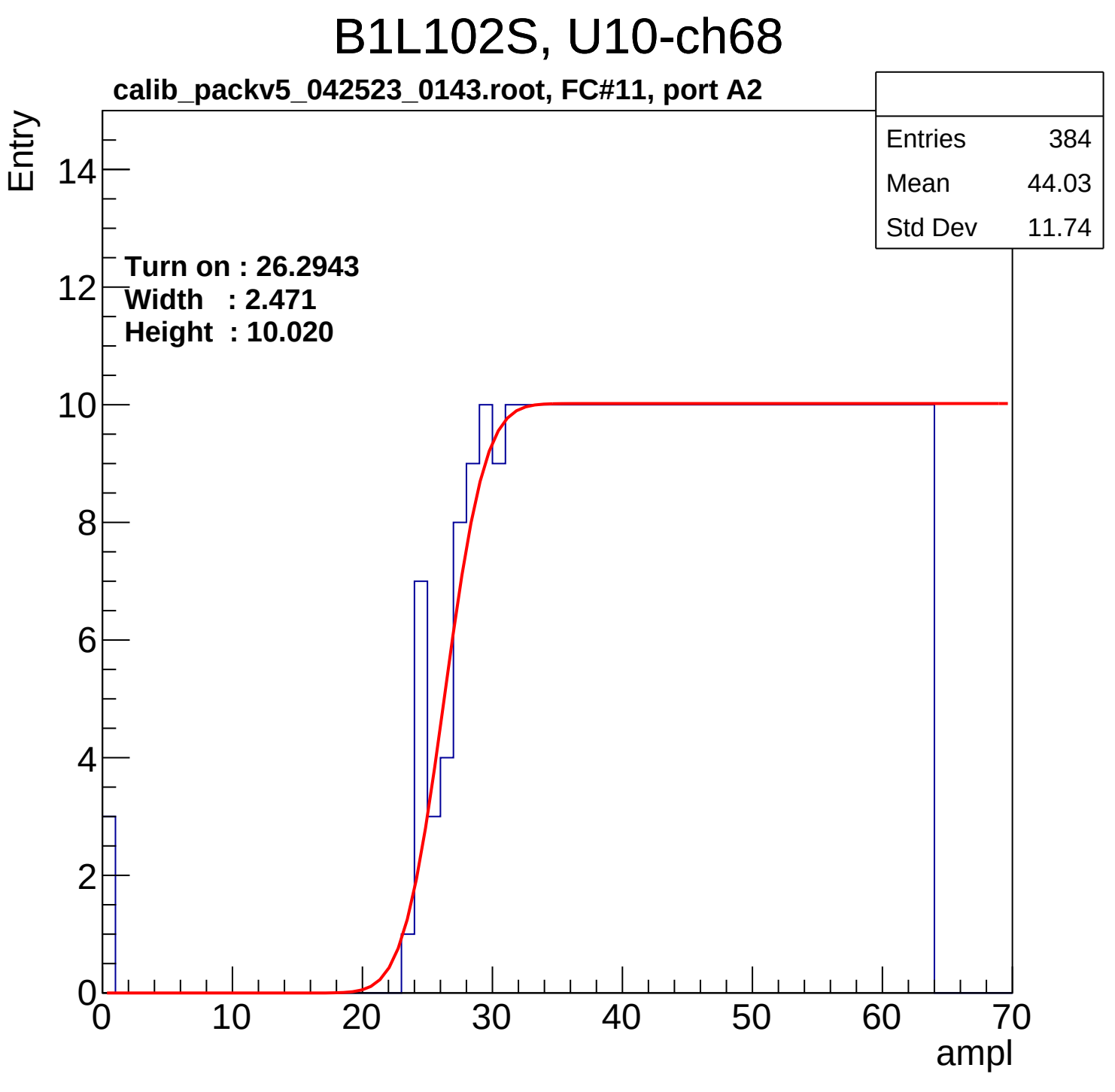
B1L102S, U10-ch68
calib_packv5_042523_0143.root, FC#11, port A2
Entries 384
Mean 44.03
Std Dev 11.74
Turn on : 26.2943
Width : 2.471
Height : 10.020
Entry
ampl
0
2
4
6
8
10
12
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0
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20
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40
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60
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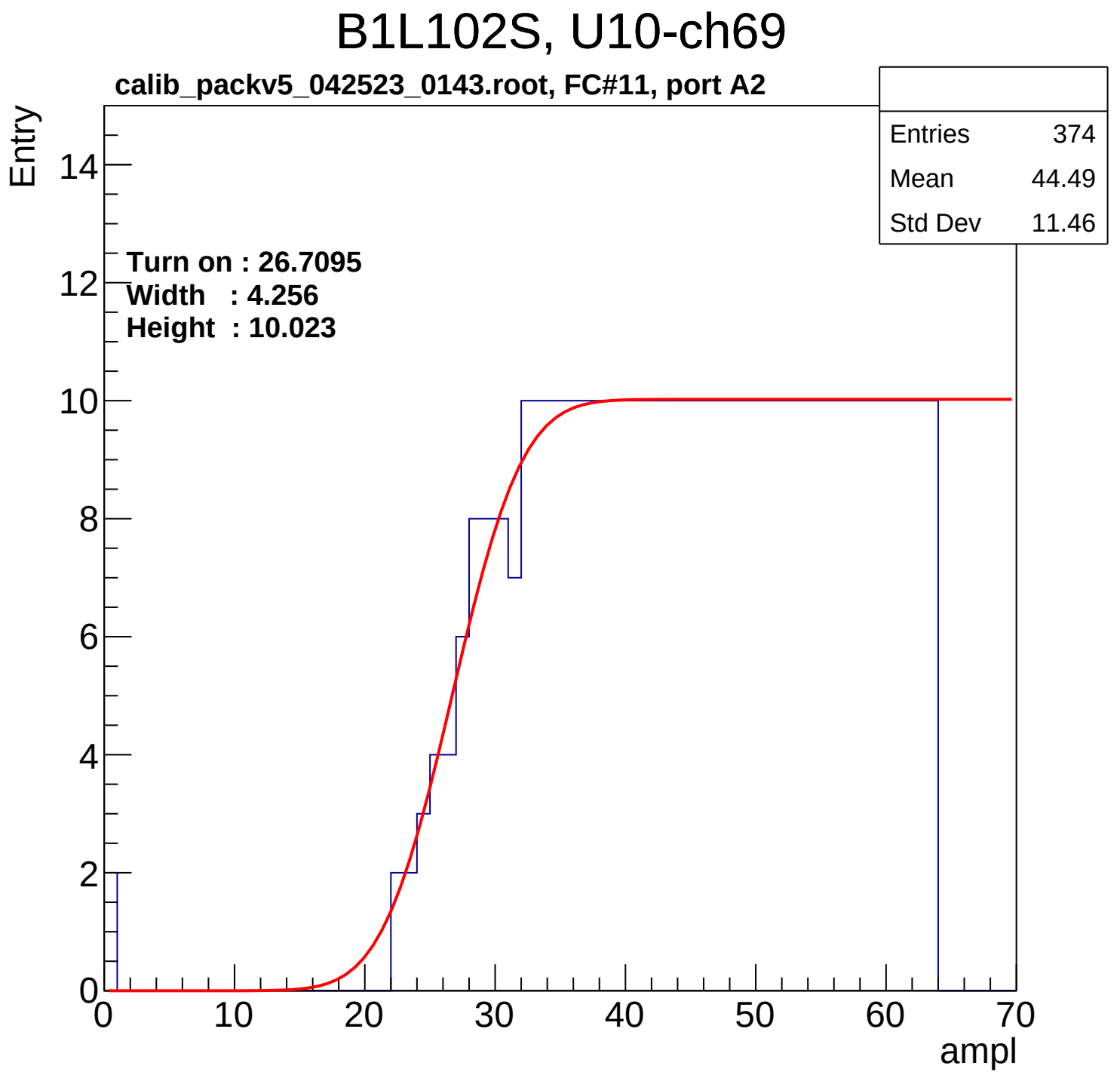
B1L102S, U10-ch69
calib_packv5_042523_0143.root, FC#11, port A2
Entries 374
Mean 44.49
Std Dev 11.46
Turn on : 26.7095
Width : 4.256
Height : 10.023
Entry
ampl
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2
4
6
8
10
12
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0
10
20
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60
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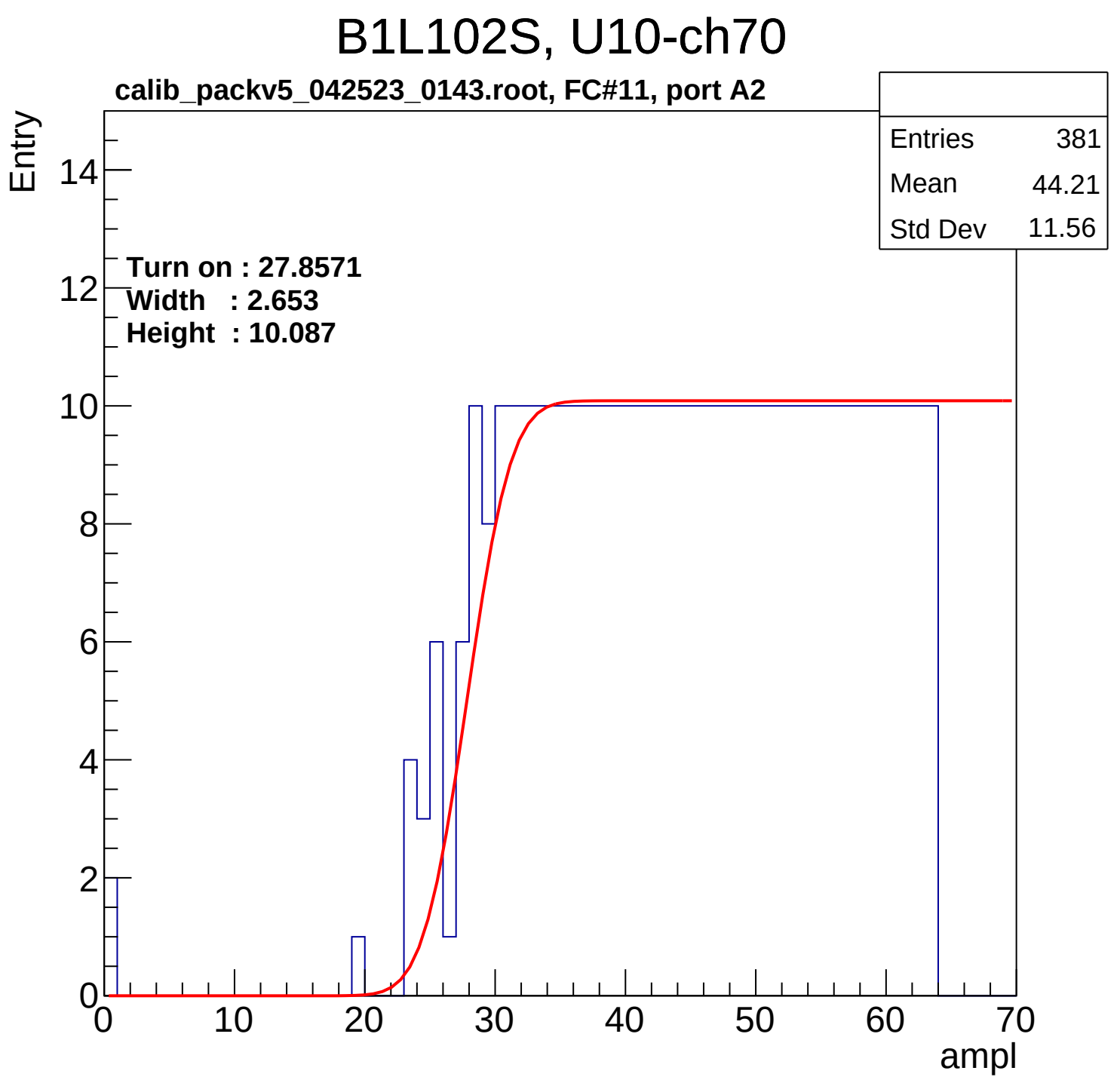
B1L102S, U10-ch70
calib_packv5_042523_0143.root, FC#11, port A2
Entries 381
Mean 44.21
Std Dev 11.56
Turn on : 27.8571
Width : 2.653
Height : 10.087
Entry
ampl
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2
4
6
8
10
12
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0
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20
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60
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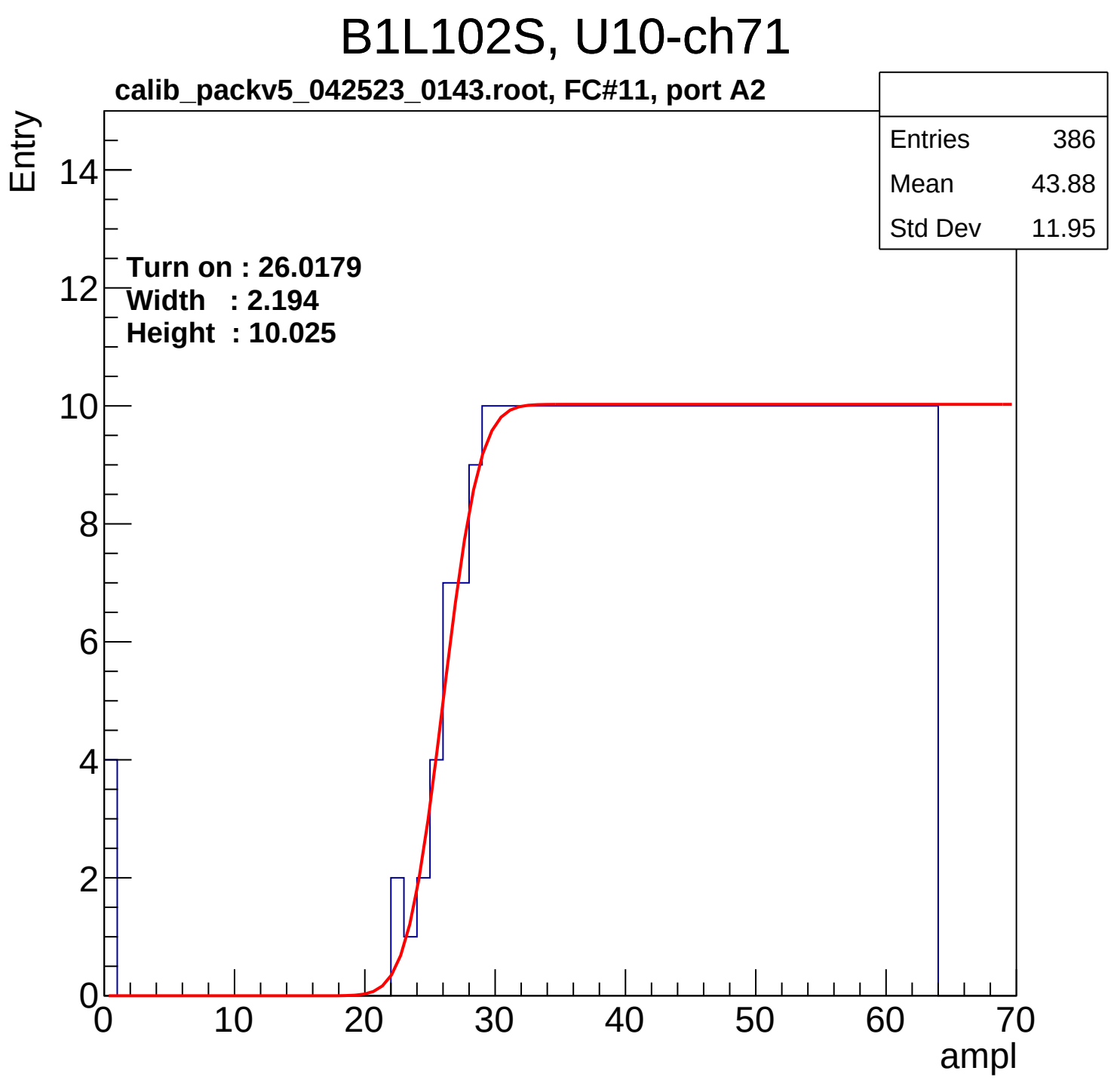
B1L102S, U10-ch71
calib_packv5_042523_0143.root, FC#11, port A2
Entries 386
Mean 43.88
Std Dev 11.95
Turn on : 26.0179
Width : 2.194
Height : 10.025
Entry
ampl
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2
4
6
8
10
12
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0
10
20
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60
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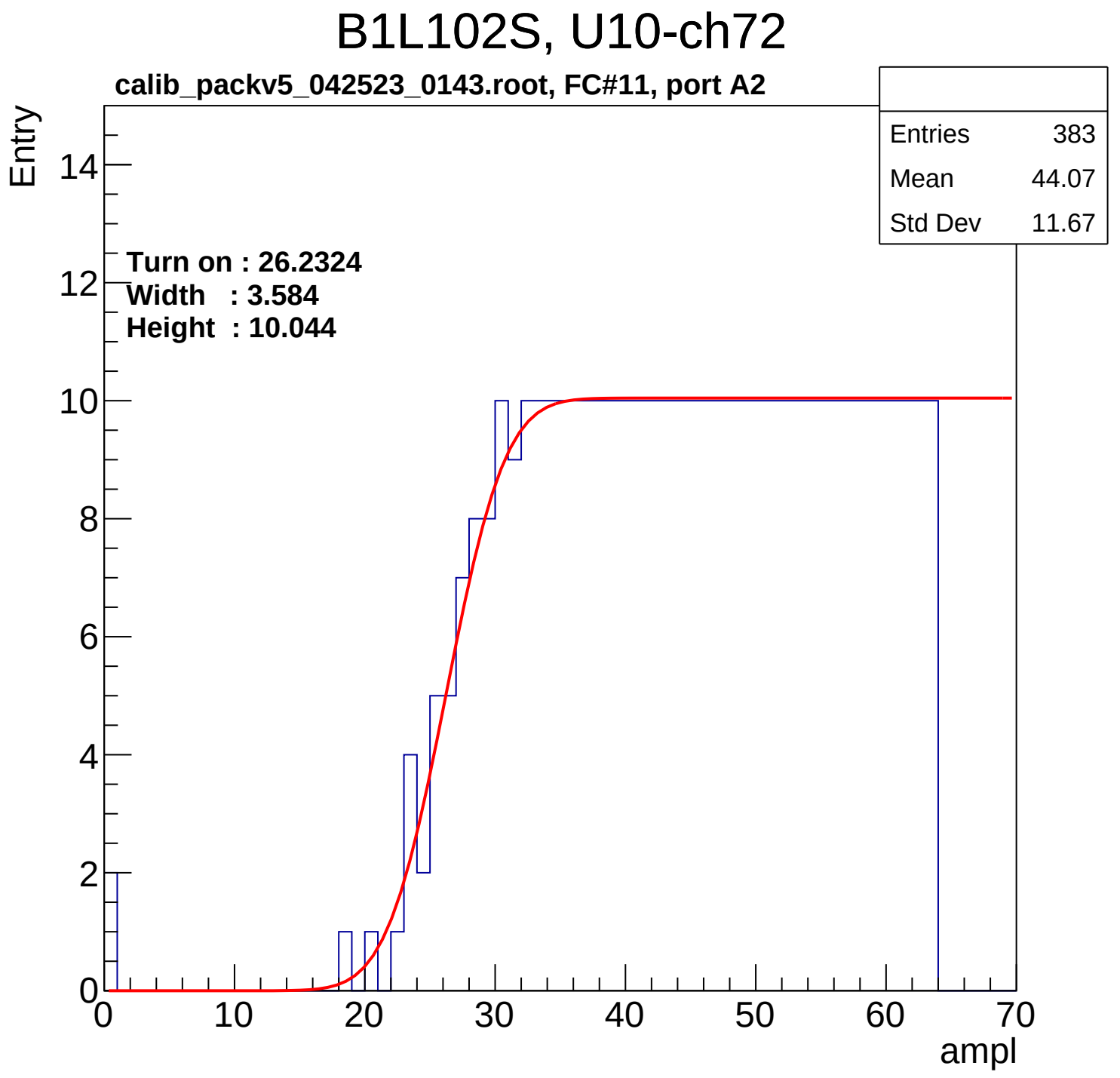
B1L102S, U10-ch72
calib_packv5_042523_0143.root, FC#11, port A2
Entries 383
Mean 44.07
Std Dev 11.67
Turn on : 26.2324
Width : 3.584
Height : 10.044
Entry
ampl
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6
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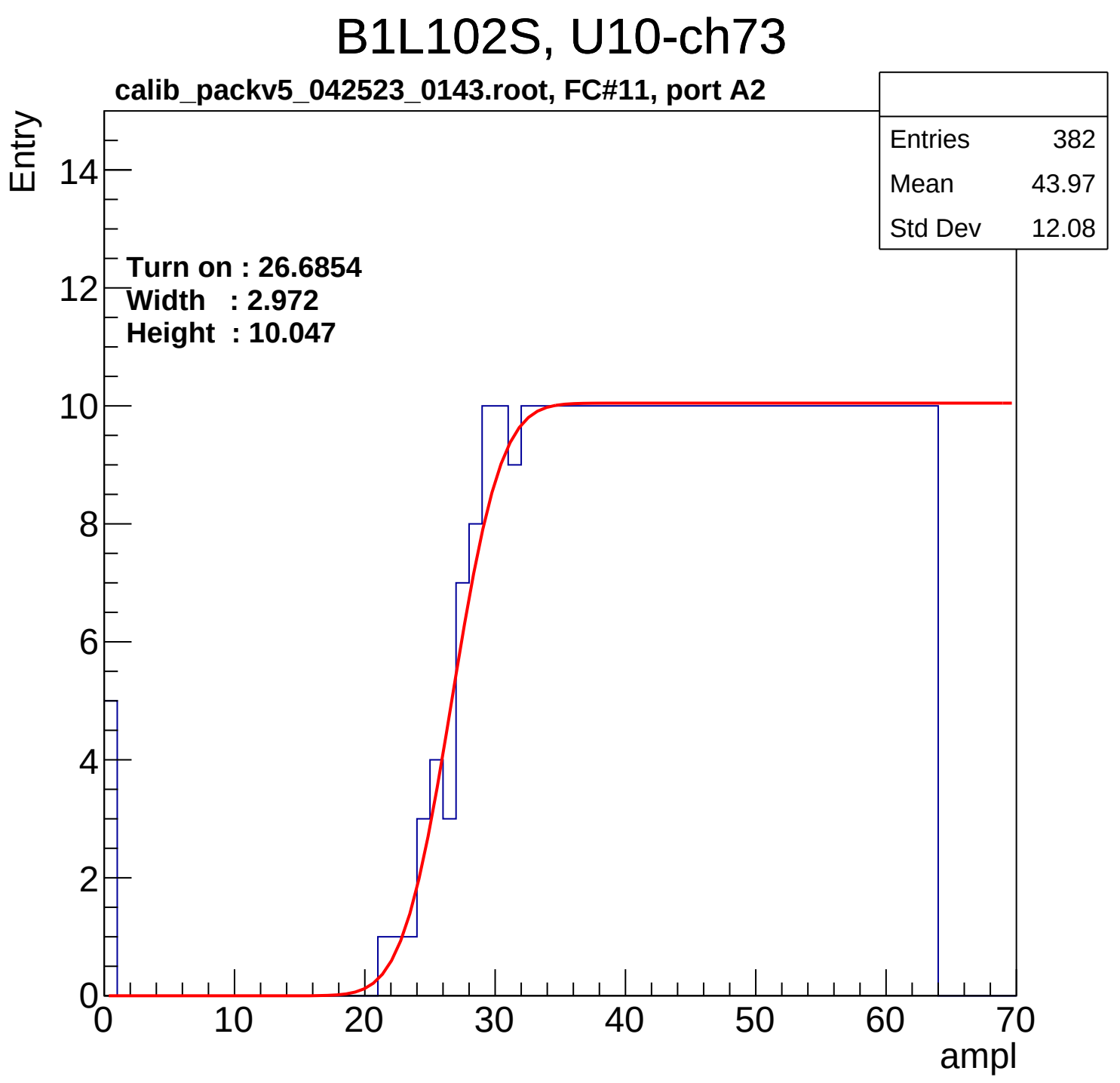
B1L102S, U10-ch73
calib_packv5_042523_0143.root, FC#11, port A2
Entries 382
Mean 43.97
Std Dev 12.08
Turn on : 26.6854
Width : 2.972
Height : 10.047
Entry
ampl
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4
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8
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0
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60
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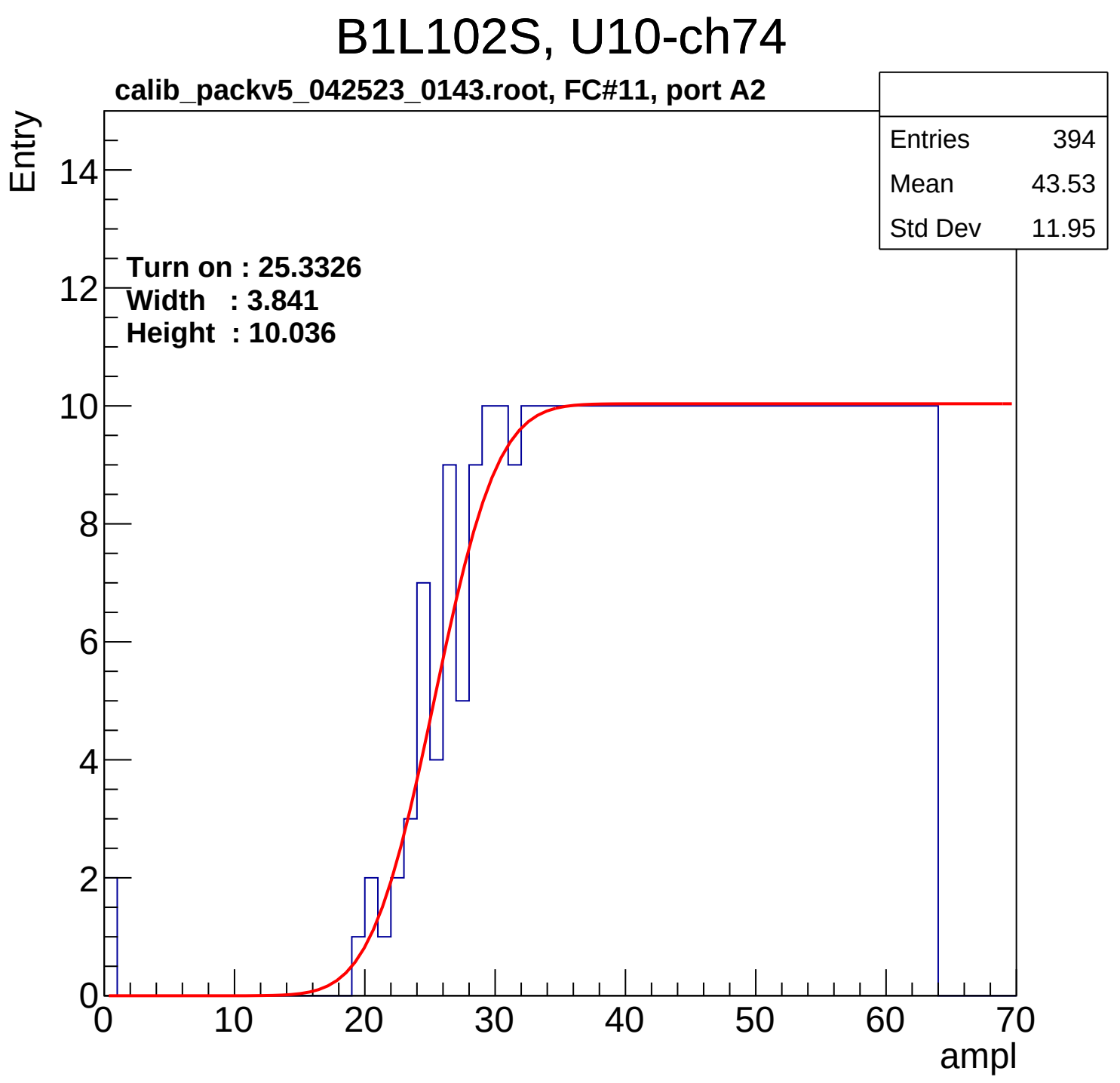
B1L102S, U10-ch74
calib_packv5_042523_0143.root, FC#11, port A2
Entries 394
Mean 43.53
Std Dev 11.95
Turn on : 25.3326
Width : 3.841
Height : 10.036
Entry
ampl
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8
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0
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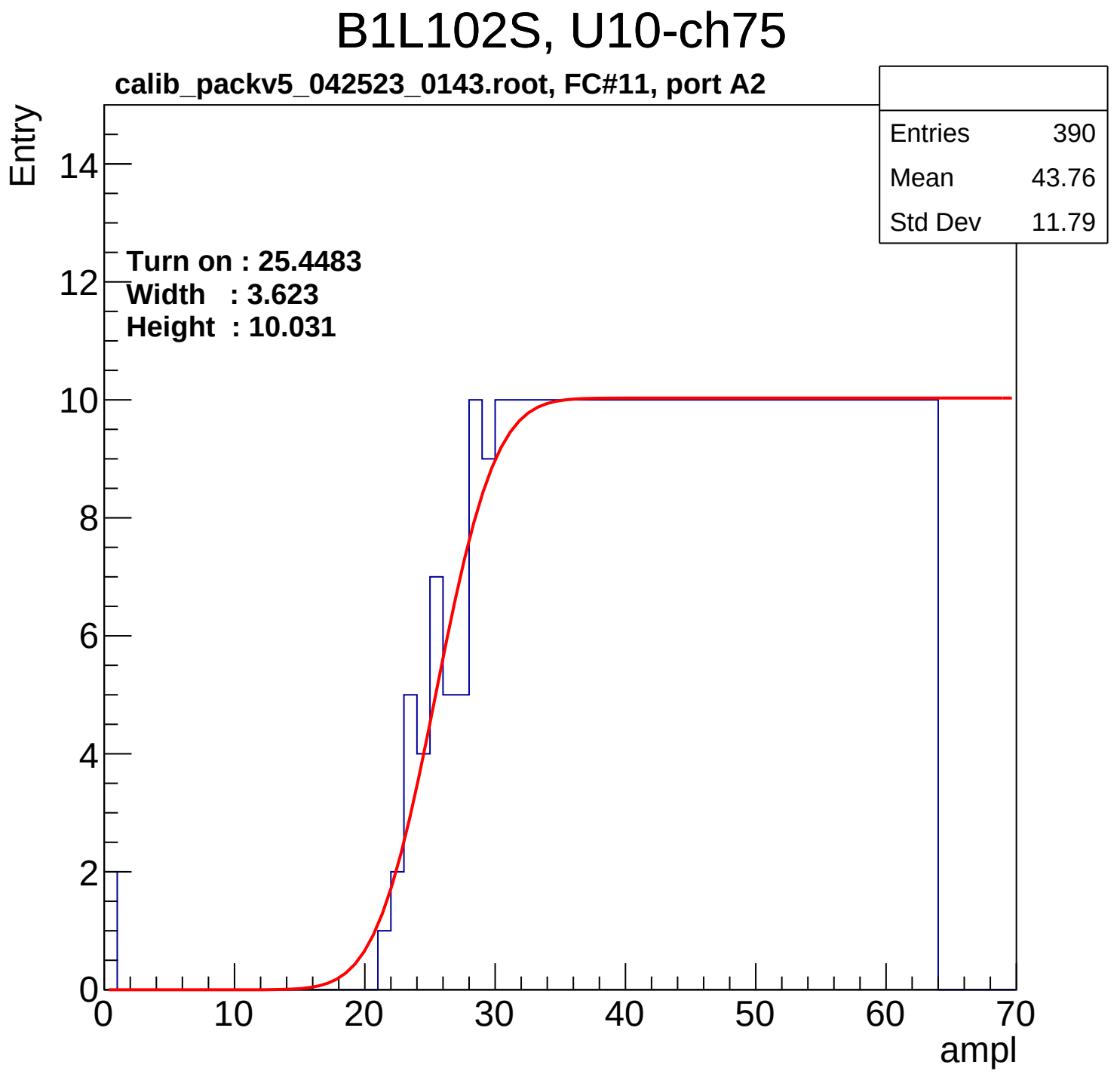
B1L102S, U10-ch75
calib_packv5_042523_0143.root, FC#11, port A2
Entries 390
Mean 43.76
Std Dev 11.79
Turn on : 25.4483
Width : 3.623
Height : 10.031
Entry
ampl
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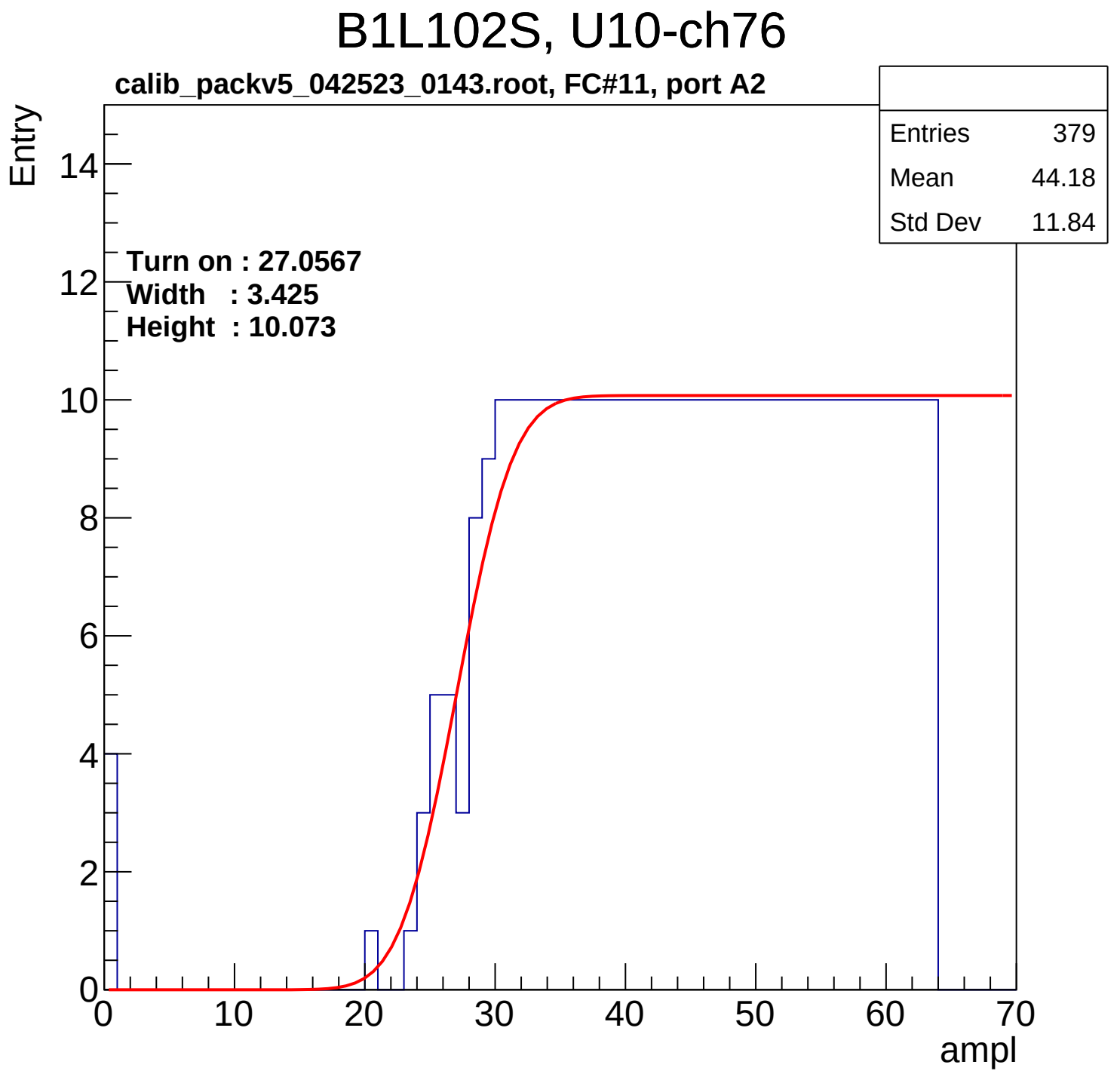
B1L102S, U10-ch76
calib_packv5_042523_0143.root, FC#11, port A2
Entries 379
Mean 44.18
Std Dev 11.84
Turn on : 27.0567
Width : 3.425
Height : 10.073
Entry
ampl
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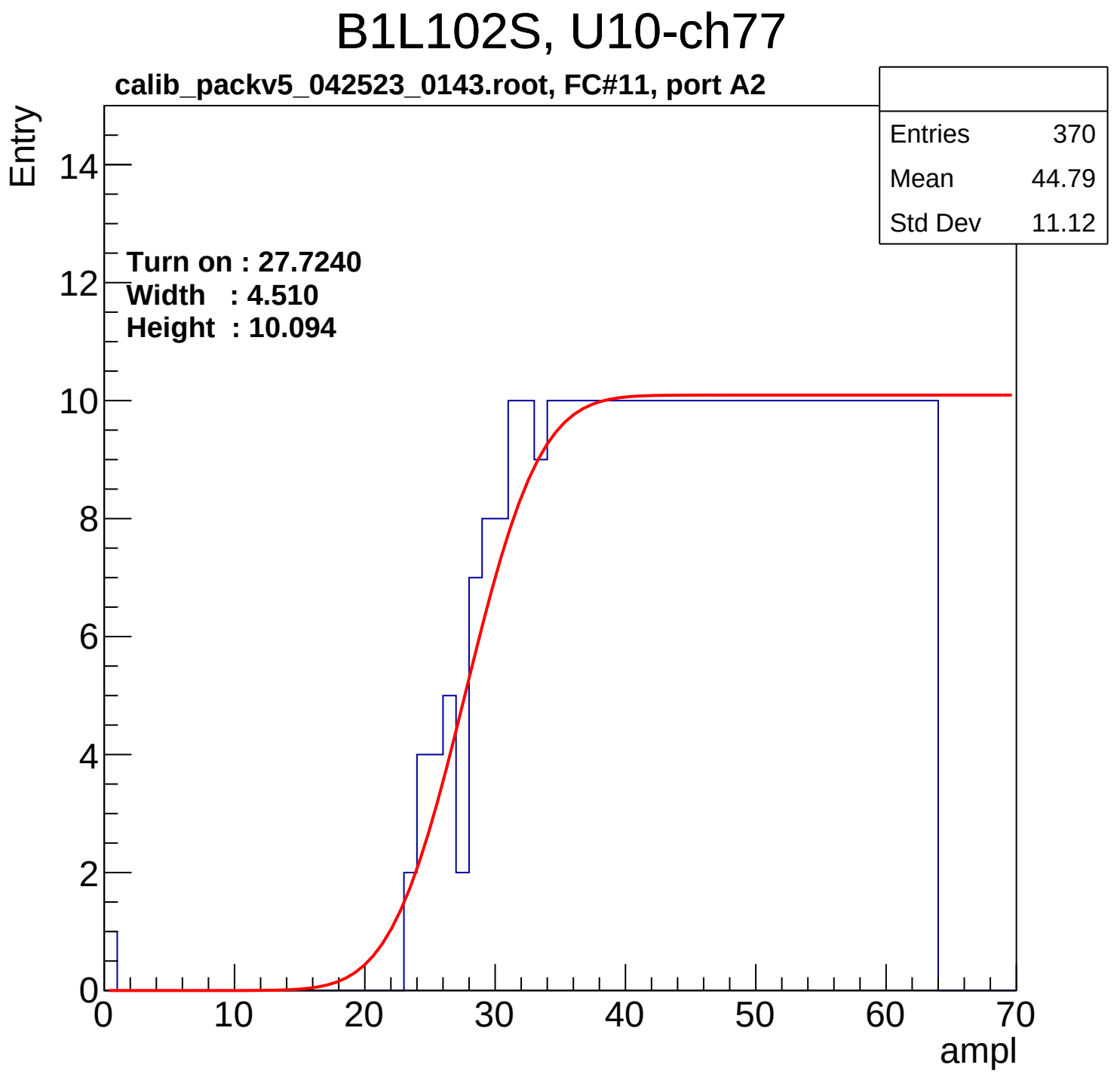
B1L102S, U10-ch77
calib_packv5_042523_0143.root, FC#11, port A2
Entries 370
Mean 44.79
Std Dev 11.12
Turn on : 27.7240
Width : 4.510
Height : 10.094
Entry
ampl
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8
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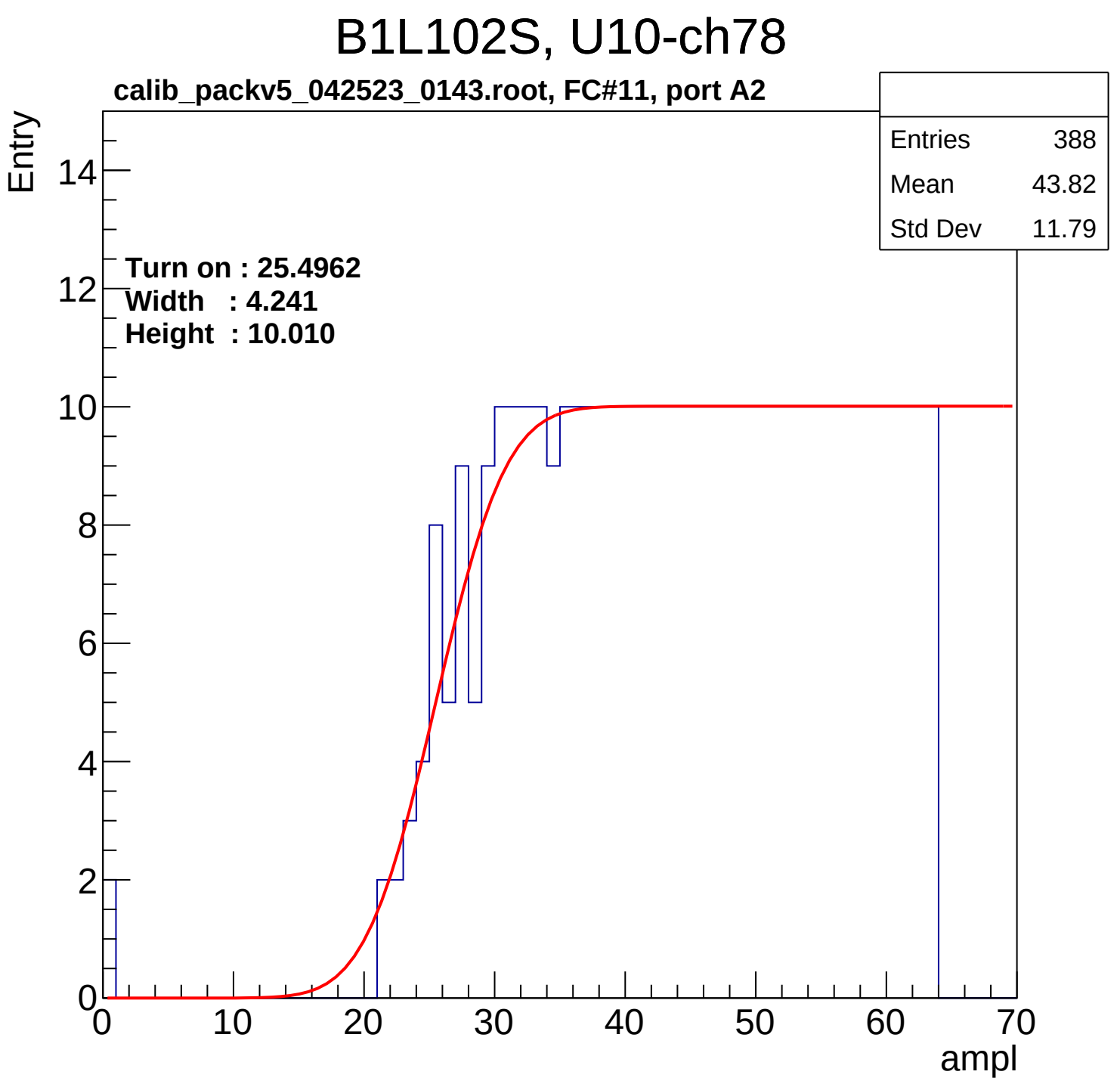
B1L102S, U10-ch78
calib_packv5_042523_0143.root, FC#11, port A2
Entries 388
Mean 43.82
Std Dev 11.79
Turn on : 25.4962
Width : 4.241
Height : 10.010
Entry
ampl
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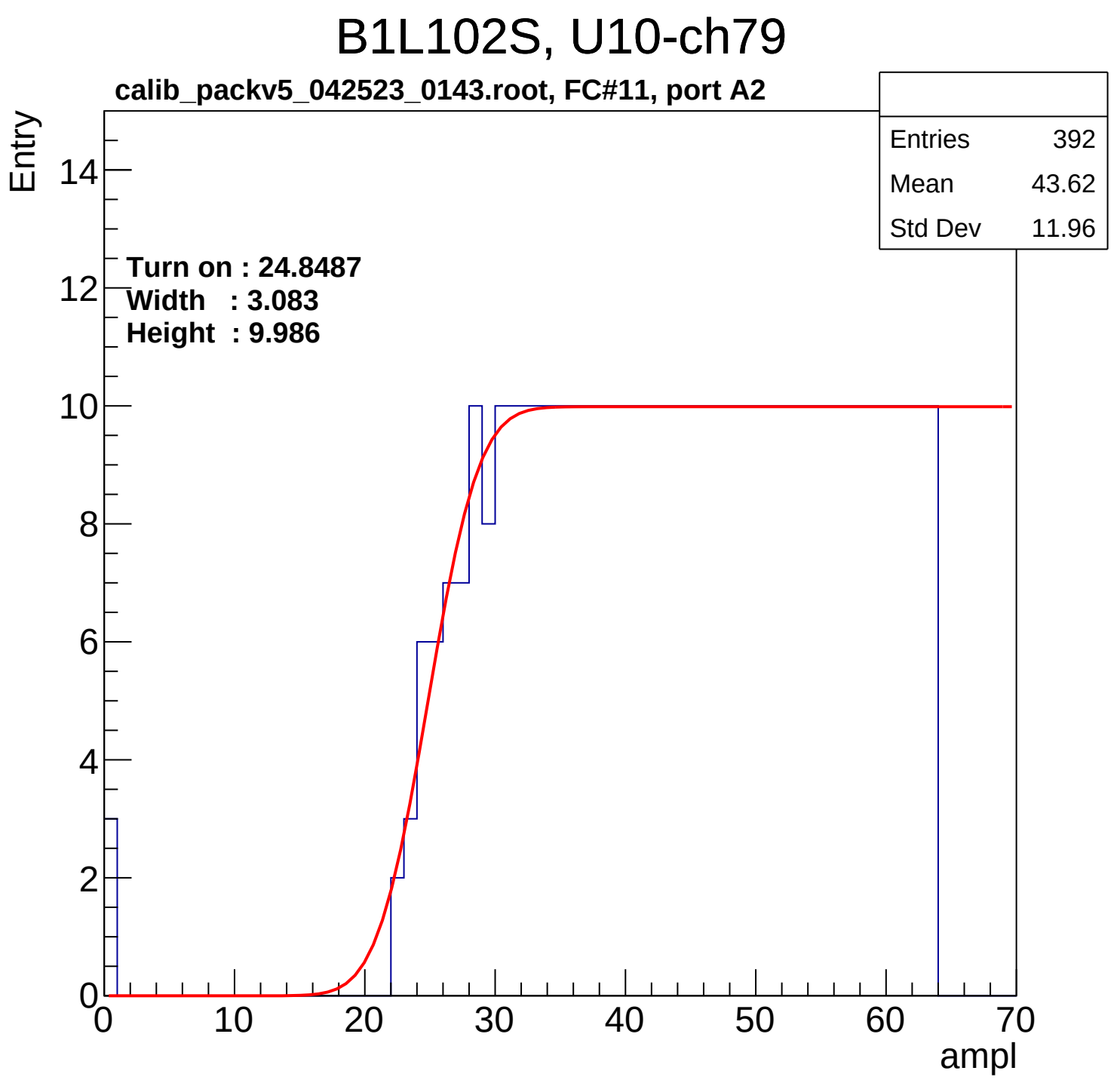
B1L102S, U10-ch79
calib_packv5_042523_0143.root, FC#11, port A2
Entries 392
Mean 43.62
Std Dev 11.96
Turn on : 24.8487
Width : 3.083
Height : 9.986
Entry
ampl
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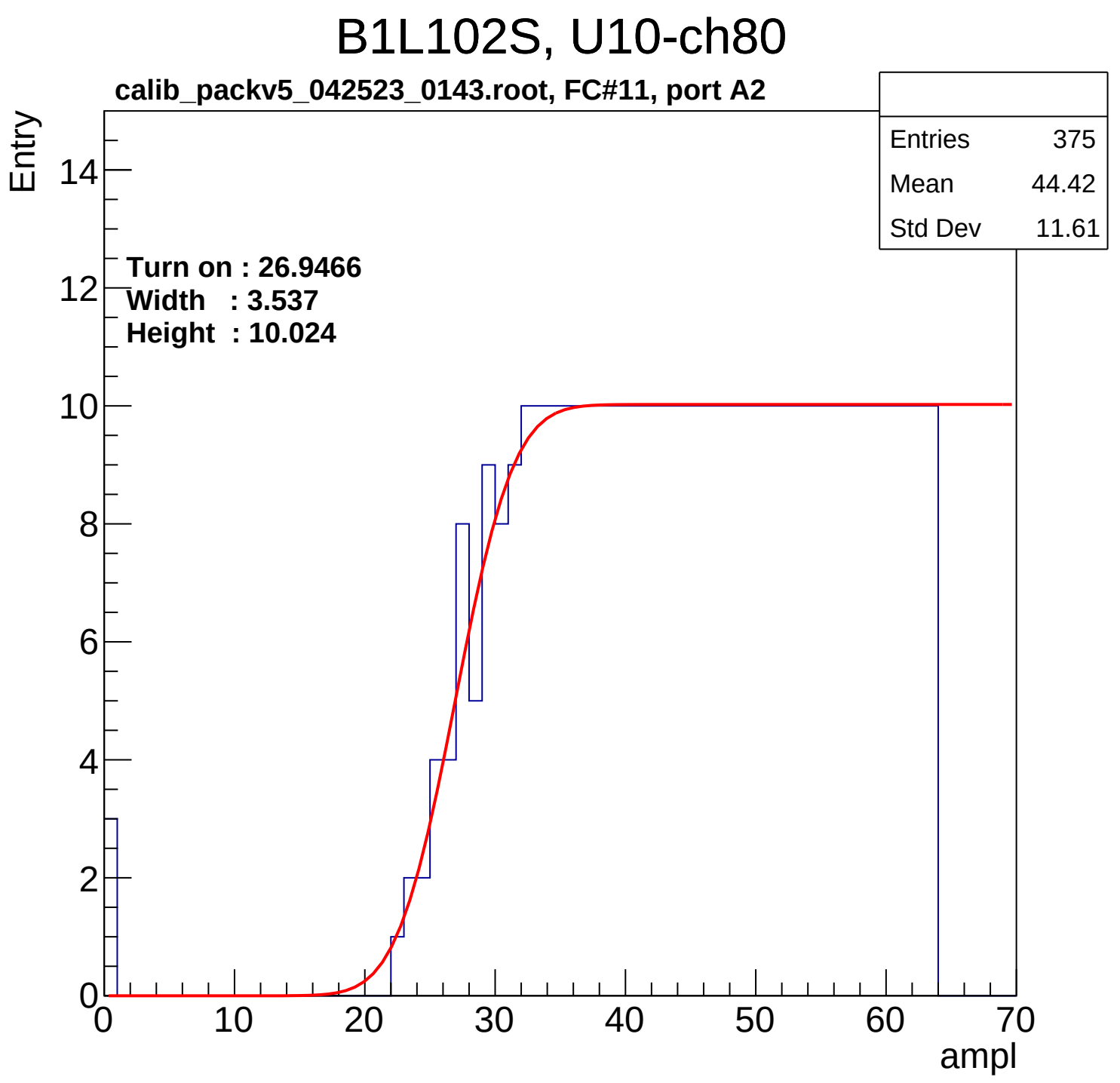
B1L102S, U10-ch80
calib_packv5_042523_0143.root, FC#11, port A2
Entries 375
Mean 44.42
Std Dev 11.61
Turn on : 26.9466
Width : 3.537
Height : 10.024
Entry
ampl
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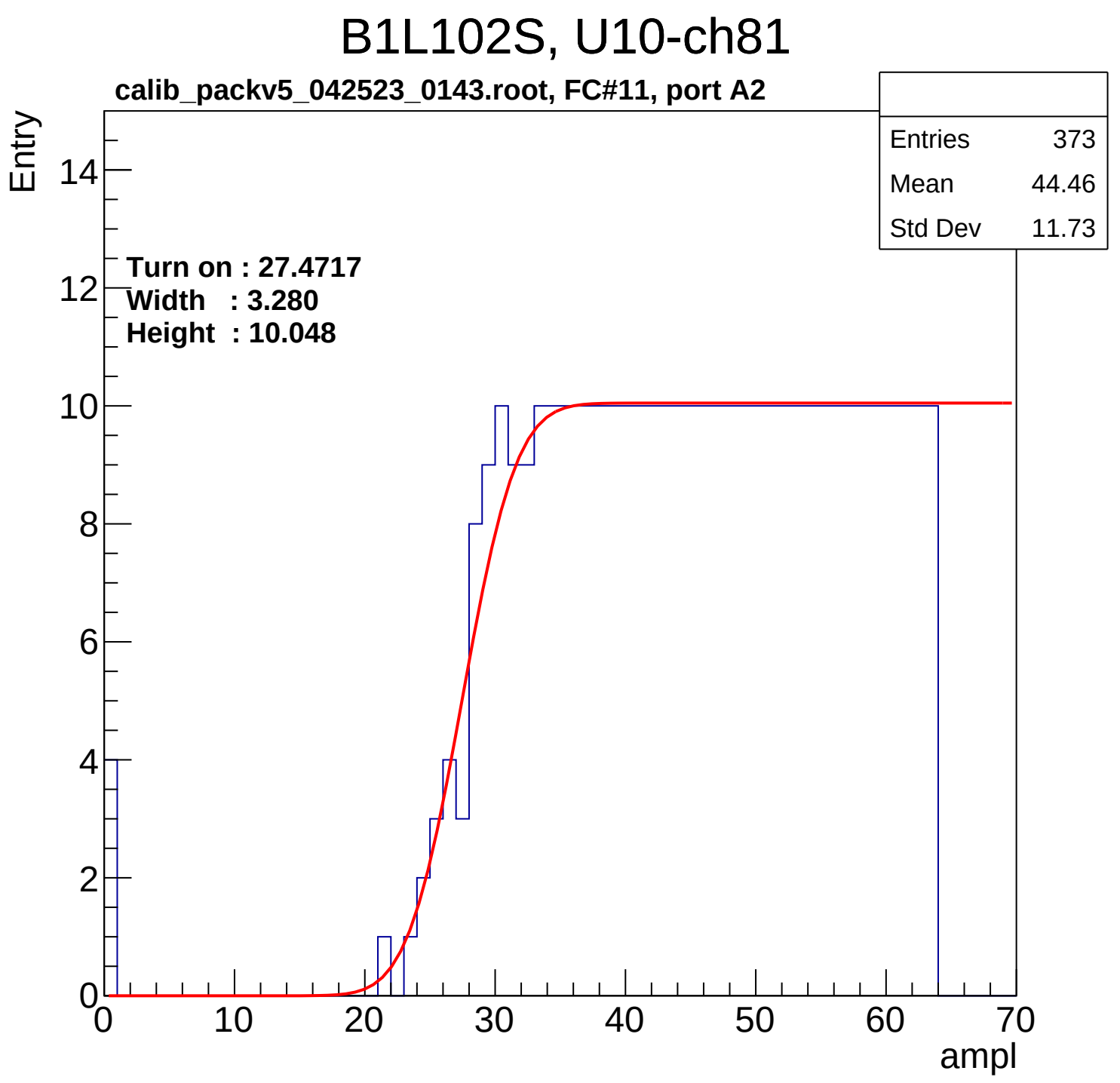
B1L102S, U10-ch81
calib_packv5_042523_0143.root, FC#11, port A2
Entries 373
Mean 44.46
Std Dev 11.73
Turn on : 27.4717
Width : 3.280
Height : 10.048
Entry
ampl
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4
6
8
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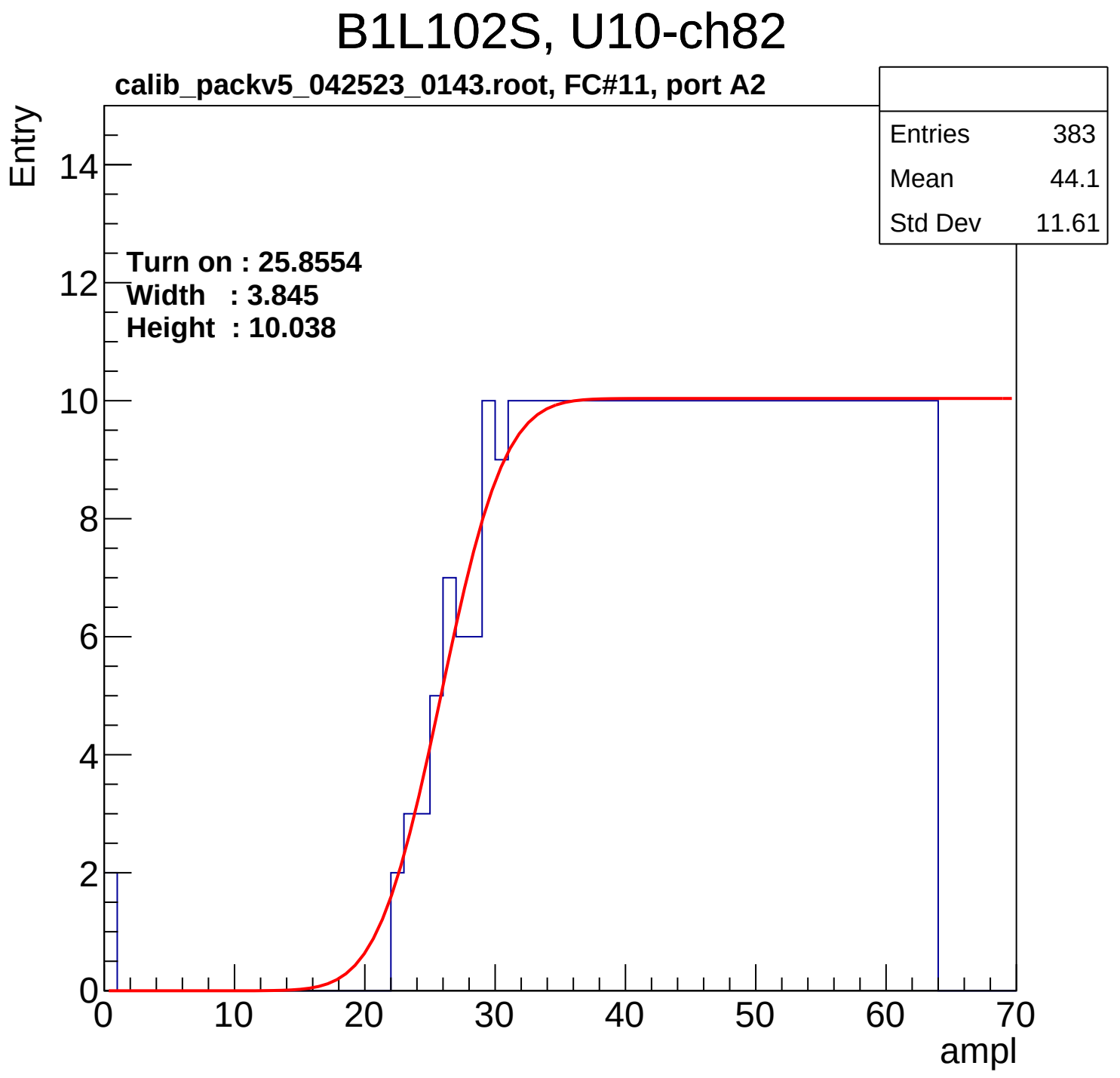
B1L102S, U10-ch82
calib_packv5_042523_0143.root, FC#11, port A2
Entries 383
Mean 44.1
Std Dev 11.61
Turn on : 25.8554
Width : 3.845
Height : 10.038
Entry
ampl
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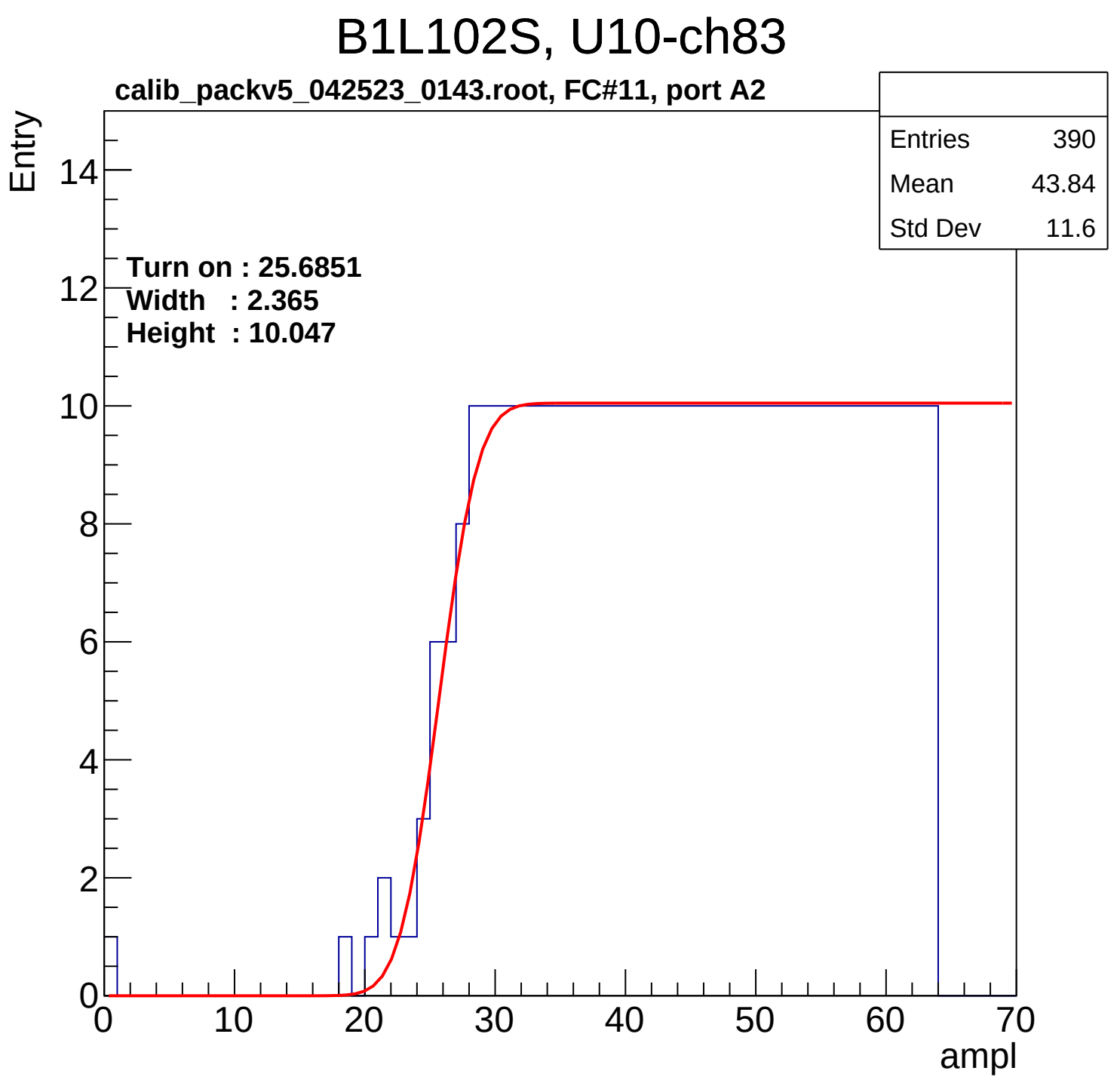
B1L102S, U10-ch83
calib_packv5_042523_0143.root, FC#11, port A2
Entries 390
Mean 43.84
Std Dev 11.6
Turn on : 25.6851
Width : 2.365
Height : 10.047
Entry
ampl
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4
6
8
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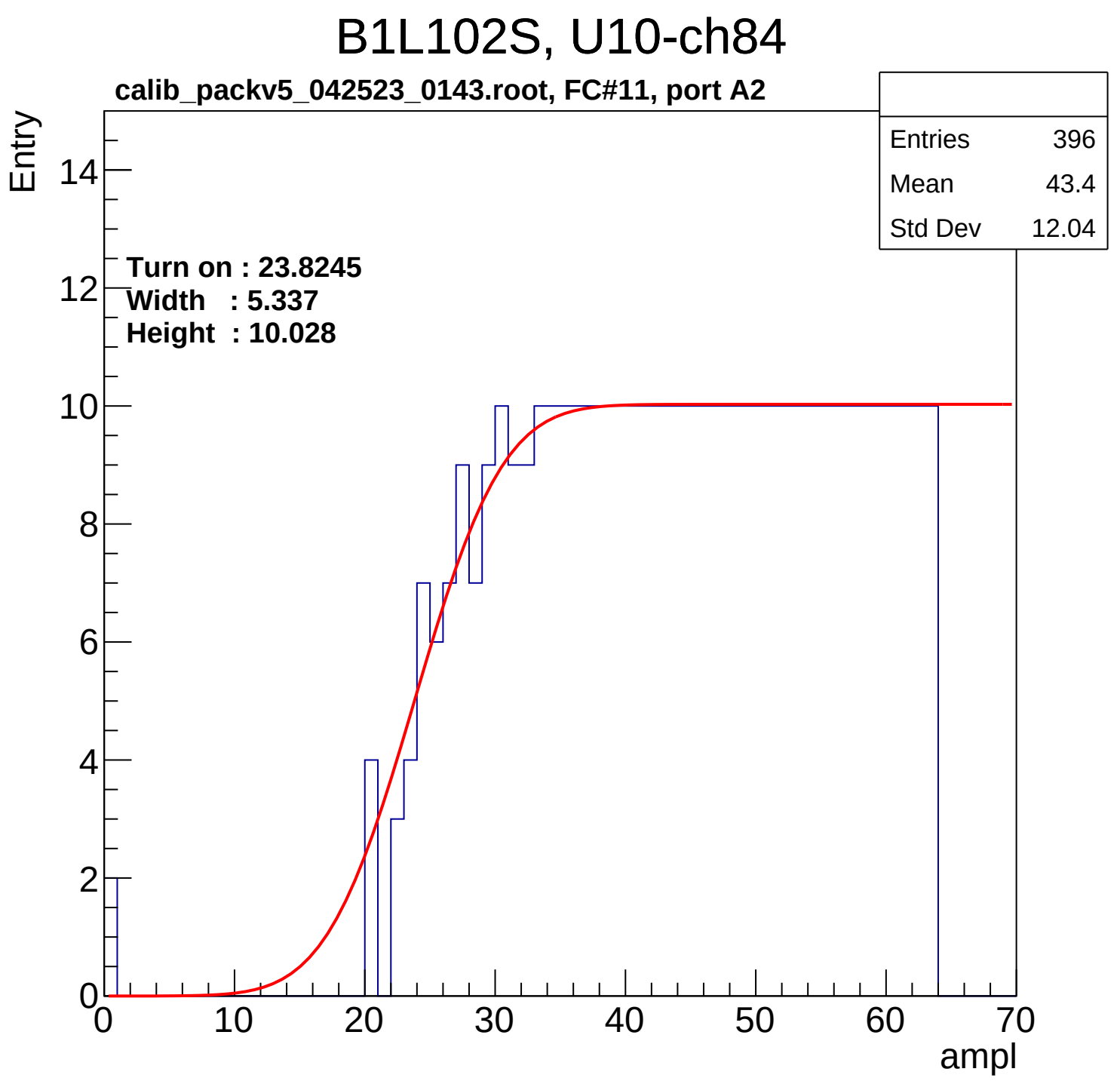
B1L102S, U10-ch84
calib_packv5_042523_0143.root, FC#11, port A2
Entries 396
Mean 43.4
Std Dev 12.04
Turn on : 23.8245
Width : 5.337
Height : 10.028
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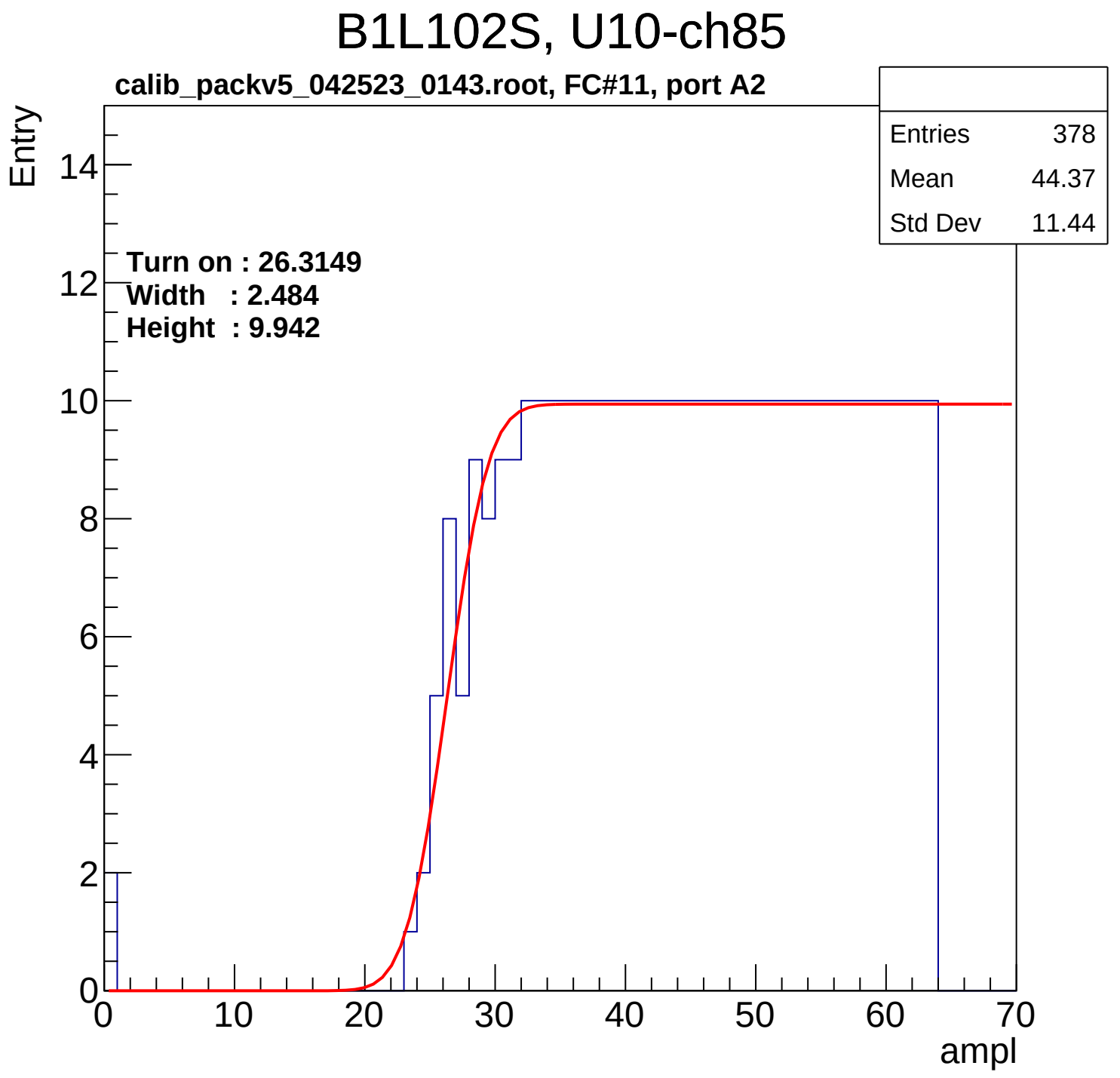
B1L102S, U10-ch85
calib_packv5_042523_0143.root, FC#11, port A2
Entries 378
Mean 44.37
Std Dev 11.44
Turn on : 26.3149
Width : 2.484
Height : 9.942
Entry
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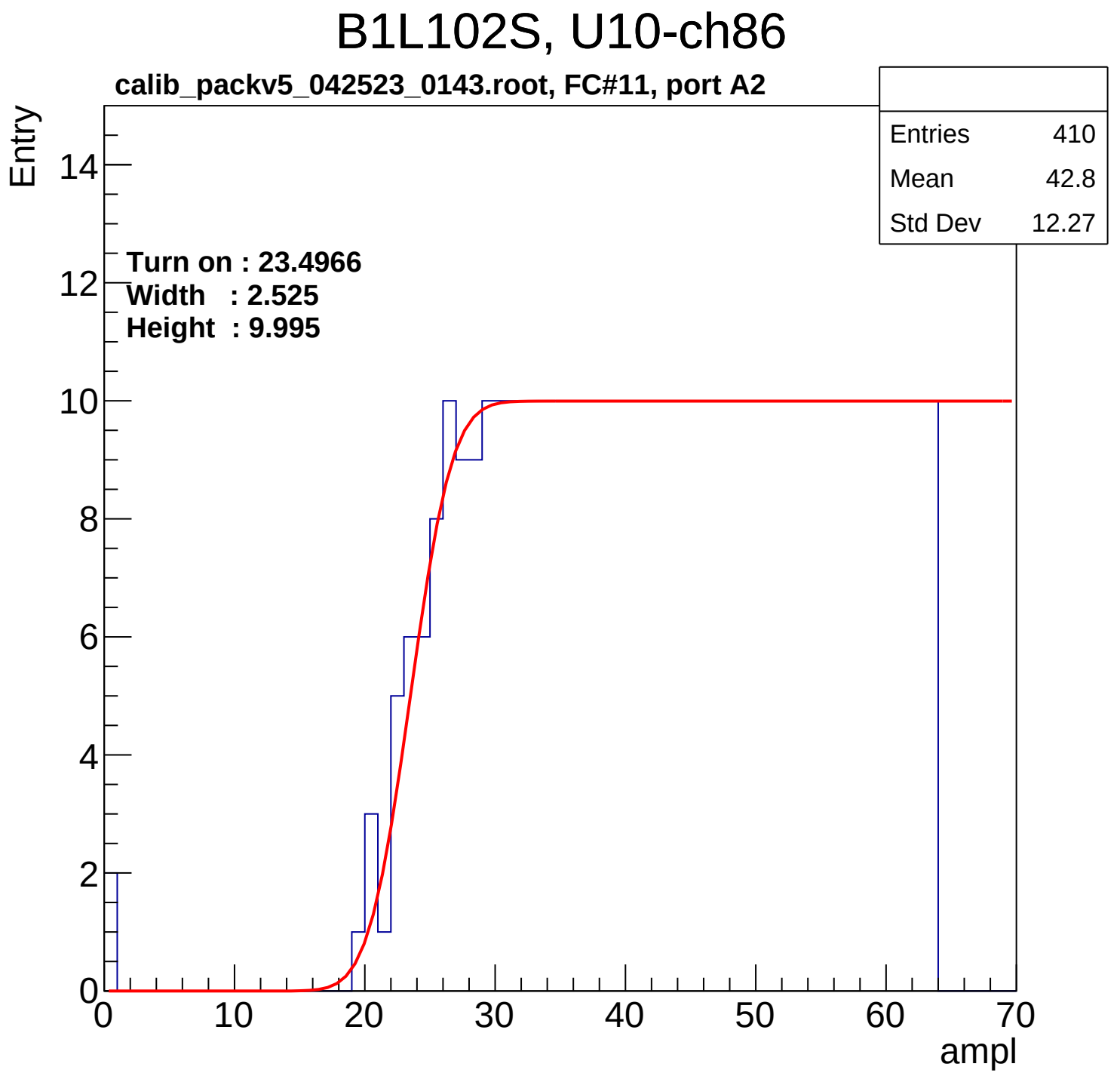
B1L102S, U10-ch86
calib_packv5_042523_0143.root, FC#11, port A2
Entries 410
Mean 42.8
Std Dev 12.27
Turn on : 23.4966
Width : 2.525
Height : 9.995
Entry
ampl
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2
4
6
8
10
12
14
0
10
20
30
40
50
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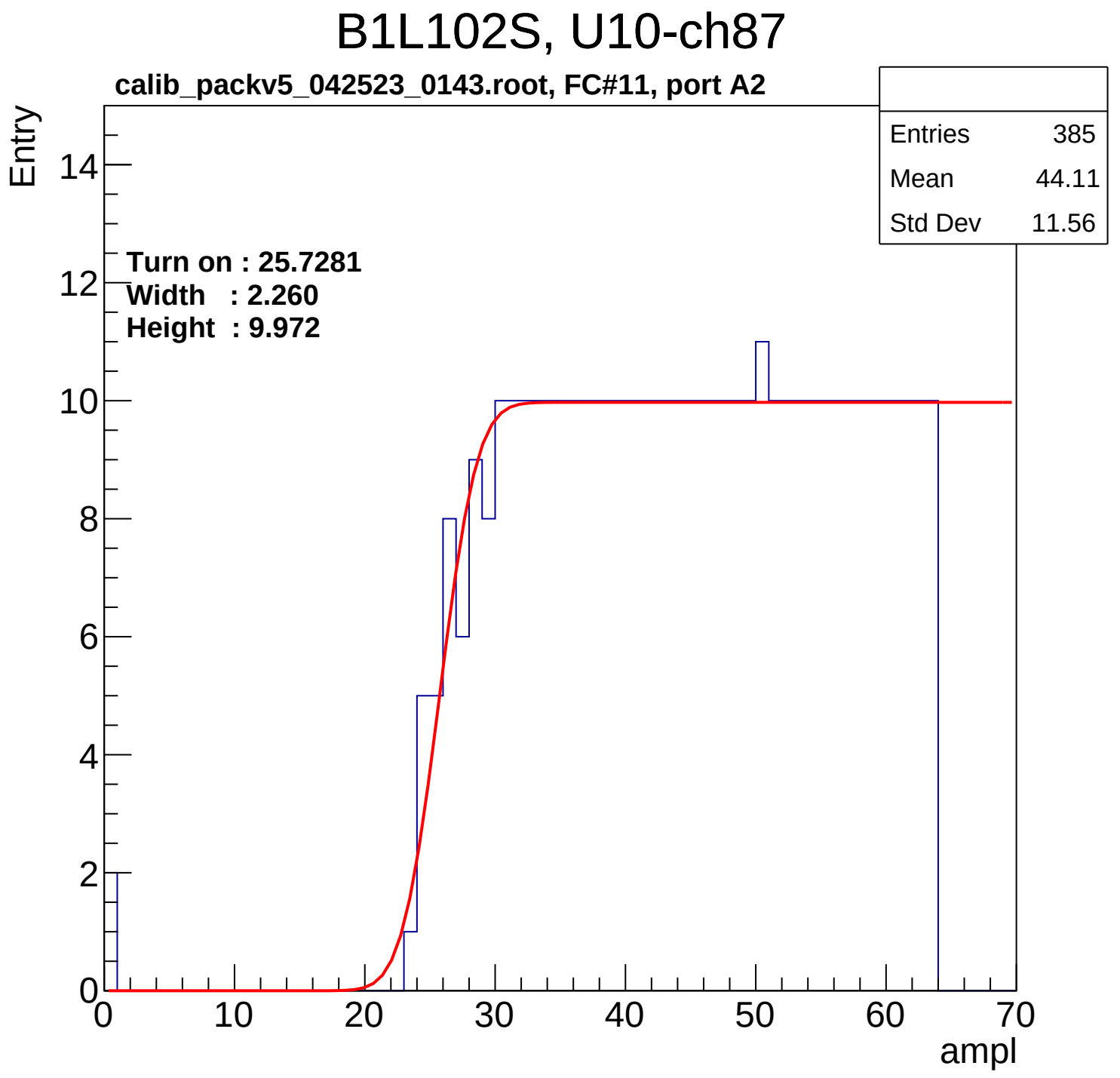
B1L102S, U10-ch87
calib_packv5_042523_0143.root, FC#11, port A2
Entries 385
Mean 44.11
Std Dev 11.56
Turn on : 25.7281
Width : 2.260
Height : 9.972
Entry
ampl
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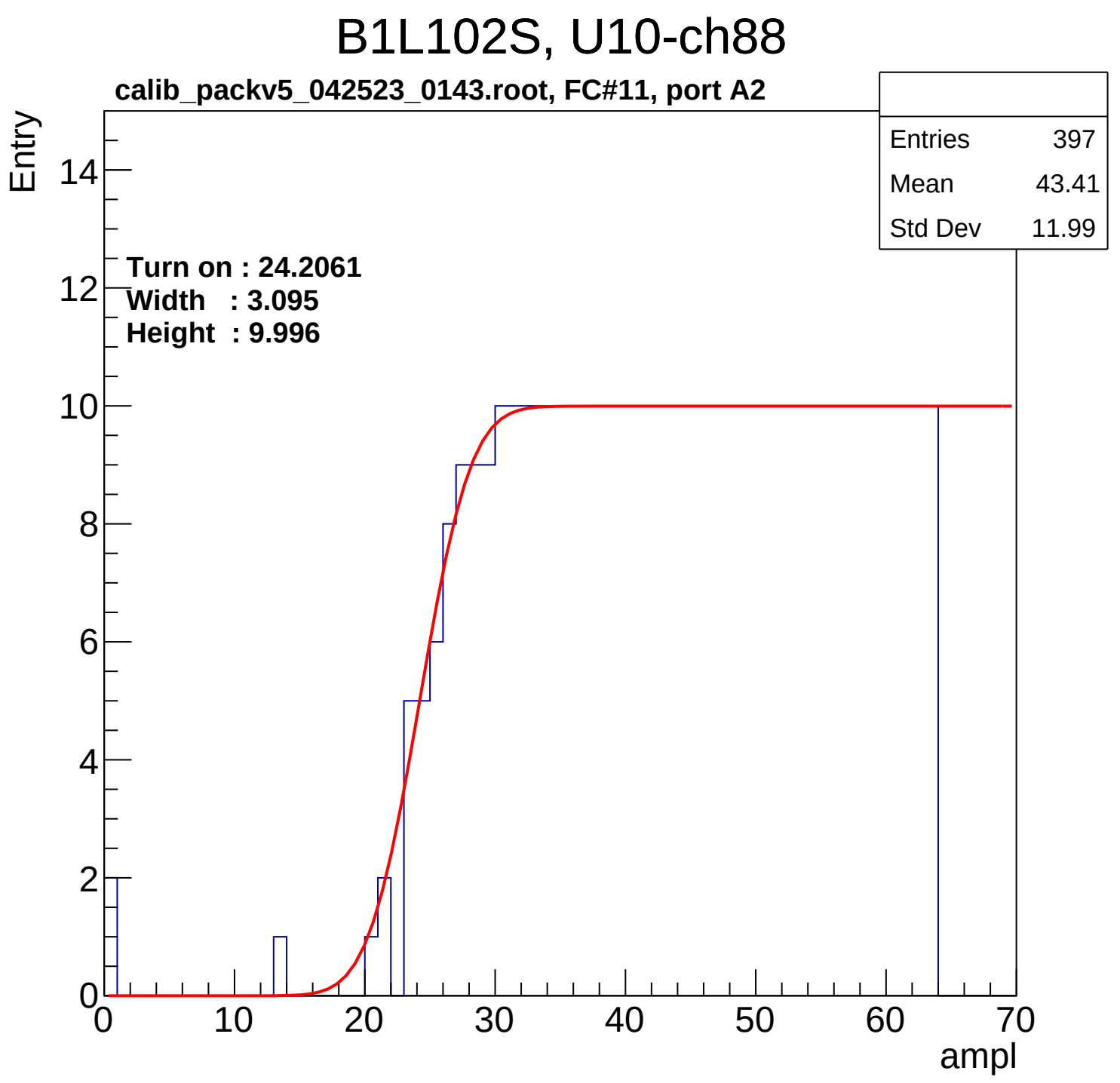
B1L102S, U10-ch88
calib_packv5_042523_0143.root, FC#11, port A2
Entries 397
Mean 43.41
Std Dev 11.99
Turn on : 24.2061
Width : 3.095
Height : 9.996
Entry
ampl
0
2
4
6
8
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0
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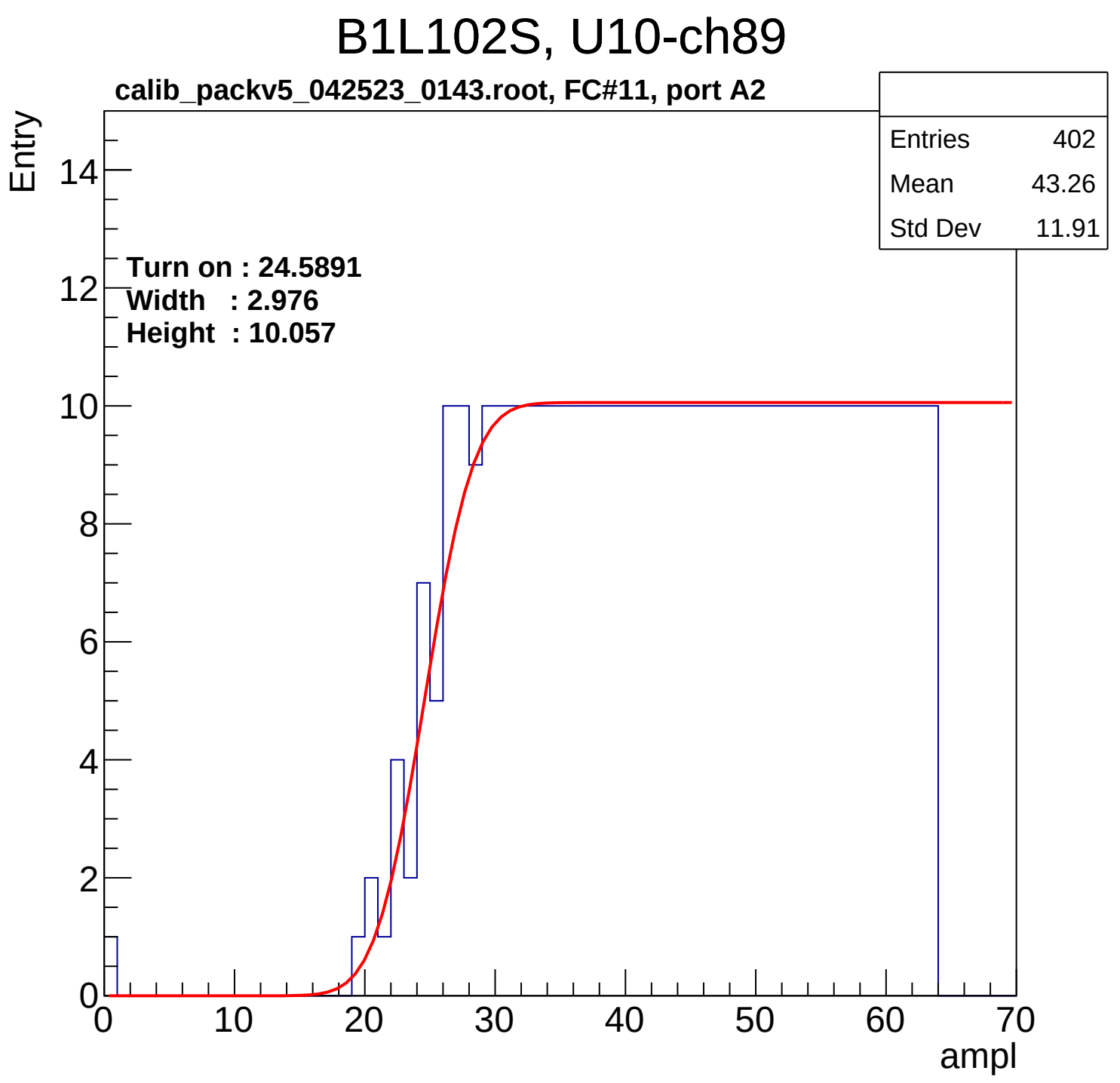
B1L102S, U10-ch89
calib_packv5_042523_0143.root, FC#11, port A2
Entries 402
Mean 43.26
Std Dev 11.91
Turn on : 24.5891
Width : 2.976
Height : 10.057
Entry
ampl
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2
4
6
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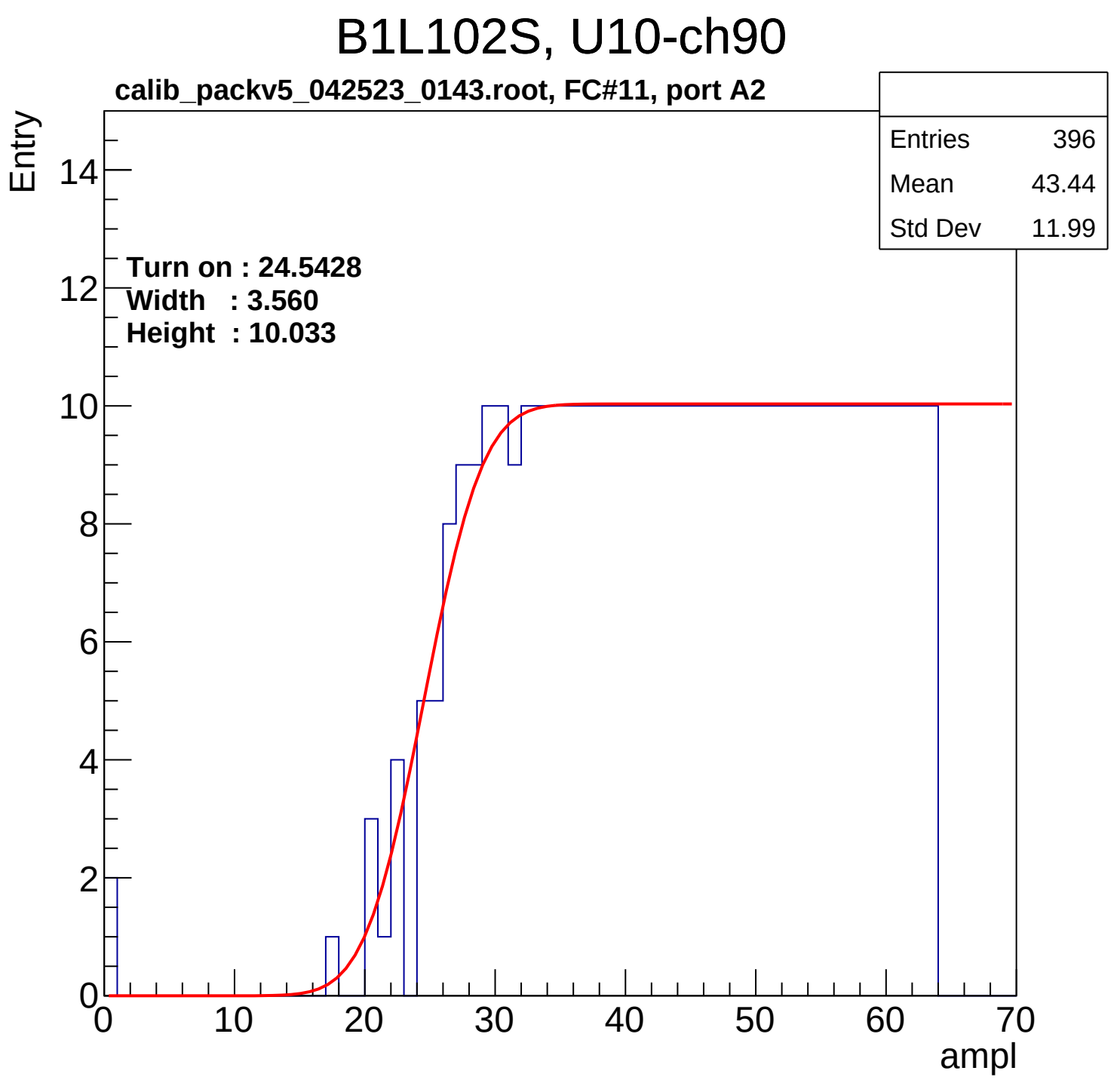
B1L102S, U10-ch90
calib_packv5_042523_0143.root, FC#11, port A2
Entries 396
Mean 43.44
Std Dev 11.99
Turn on : 24.5428
Width : 3.560
Height : 10.033
Entry
ampl
0
2
4
6
8
10
12
14
0
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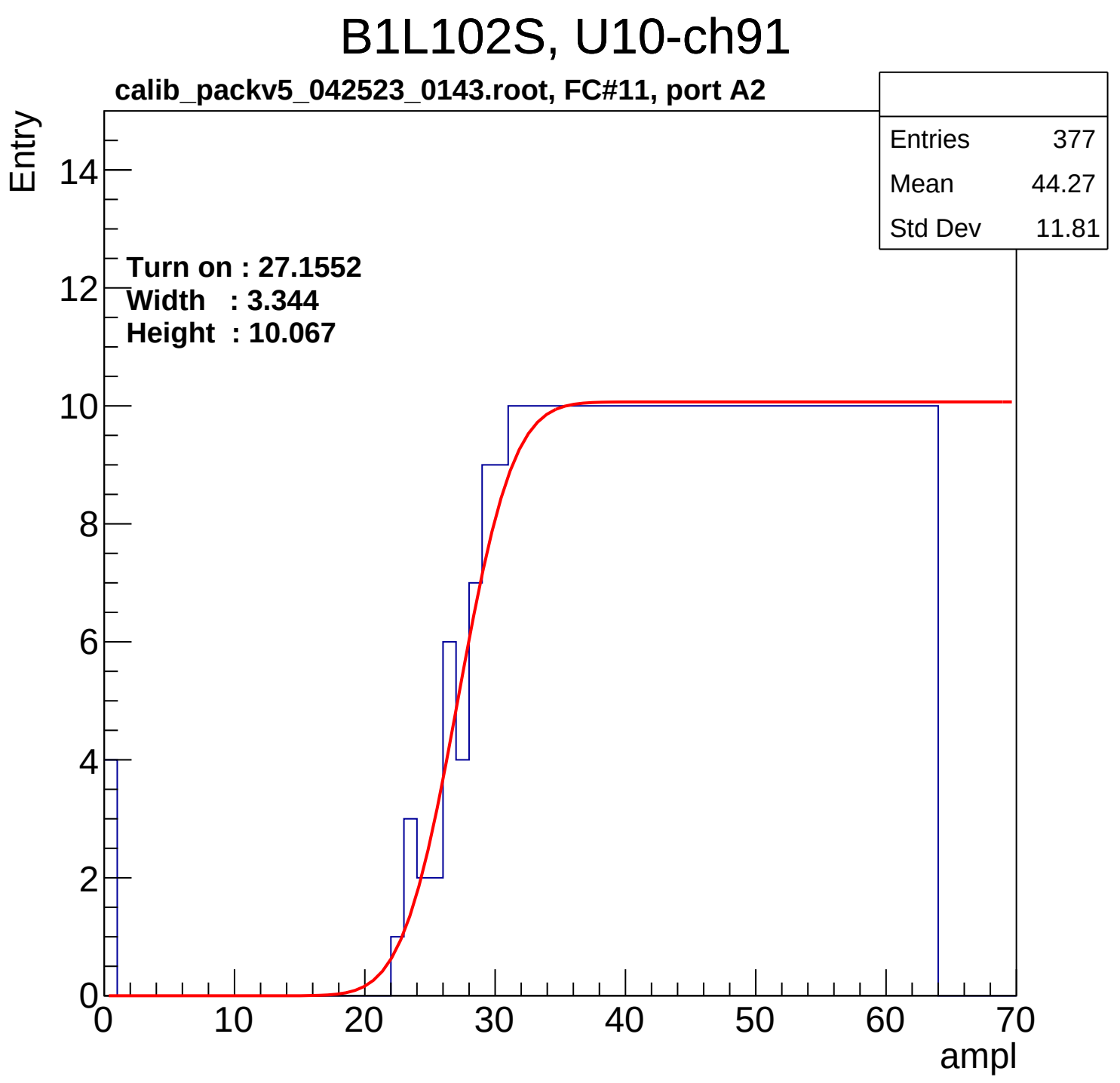
B1L102S, U10-ch91
calib_packv5_042523_0143.root, FC#11, port A2
Entries 377
Mean 44.27
Std Dev 11.81
Turn on : 27.1552
Width : 3.344
Height : 10.067
Entry
ampl
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2
4
6
8
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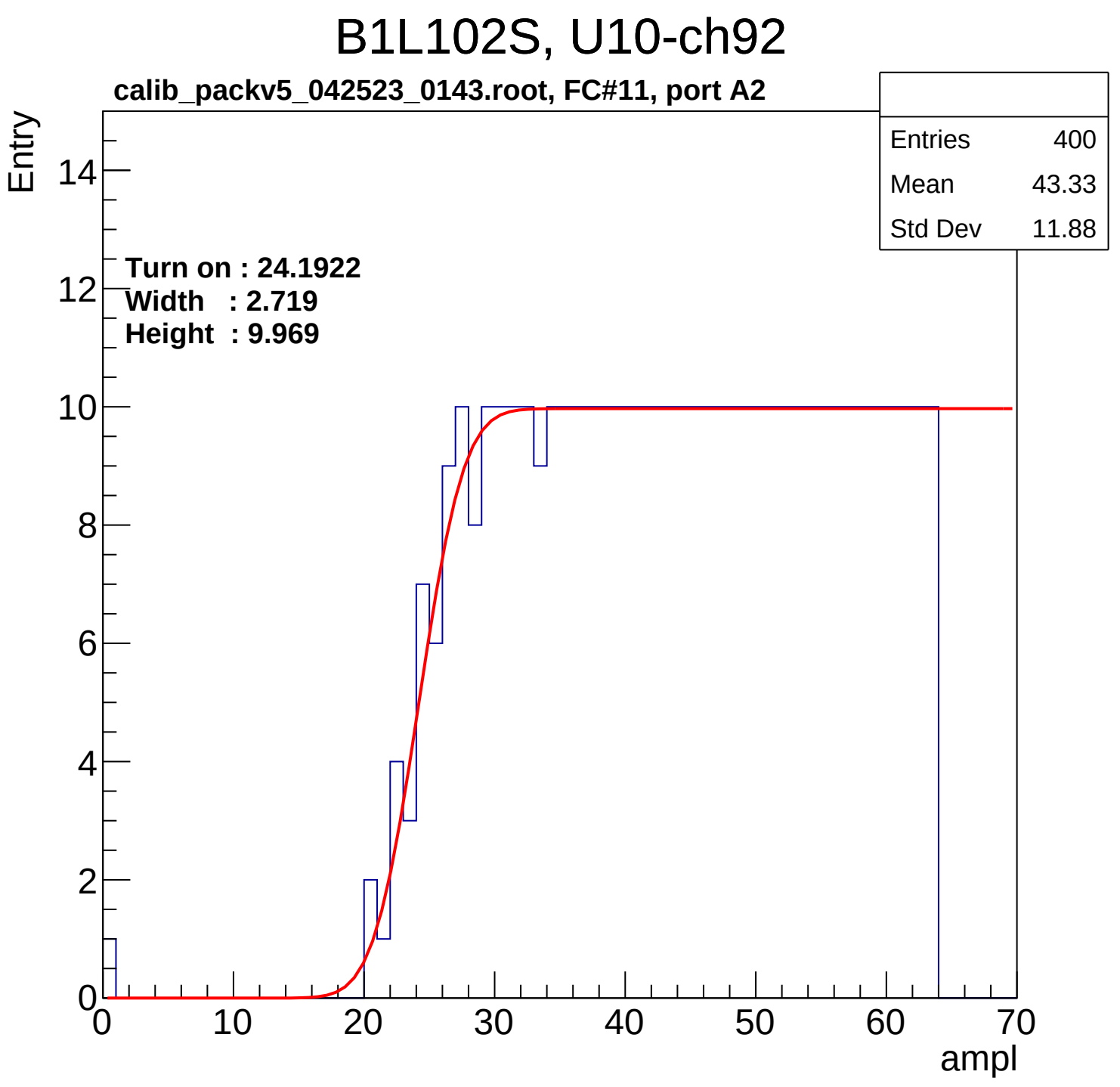
B1L102S, U10-ch92
calib_packv5_042523_0143.root, FC#11, port A2
Entries 400
Mean 43.33
Std Dev 11.88
Turn on : 24.1922
Width : 2.719
Height : 9.969
Entry
ampl
0
2
4
6
8
10
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0
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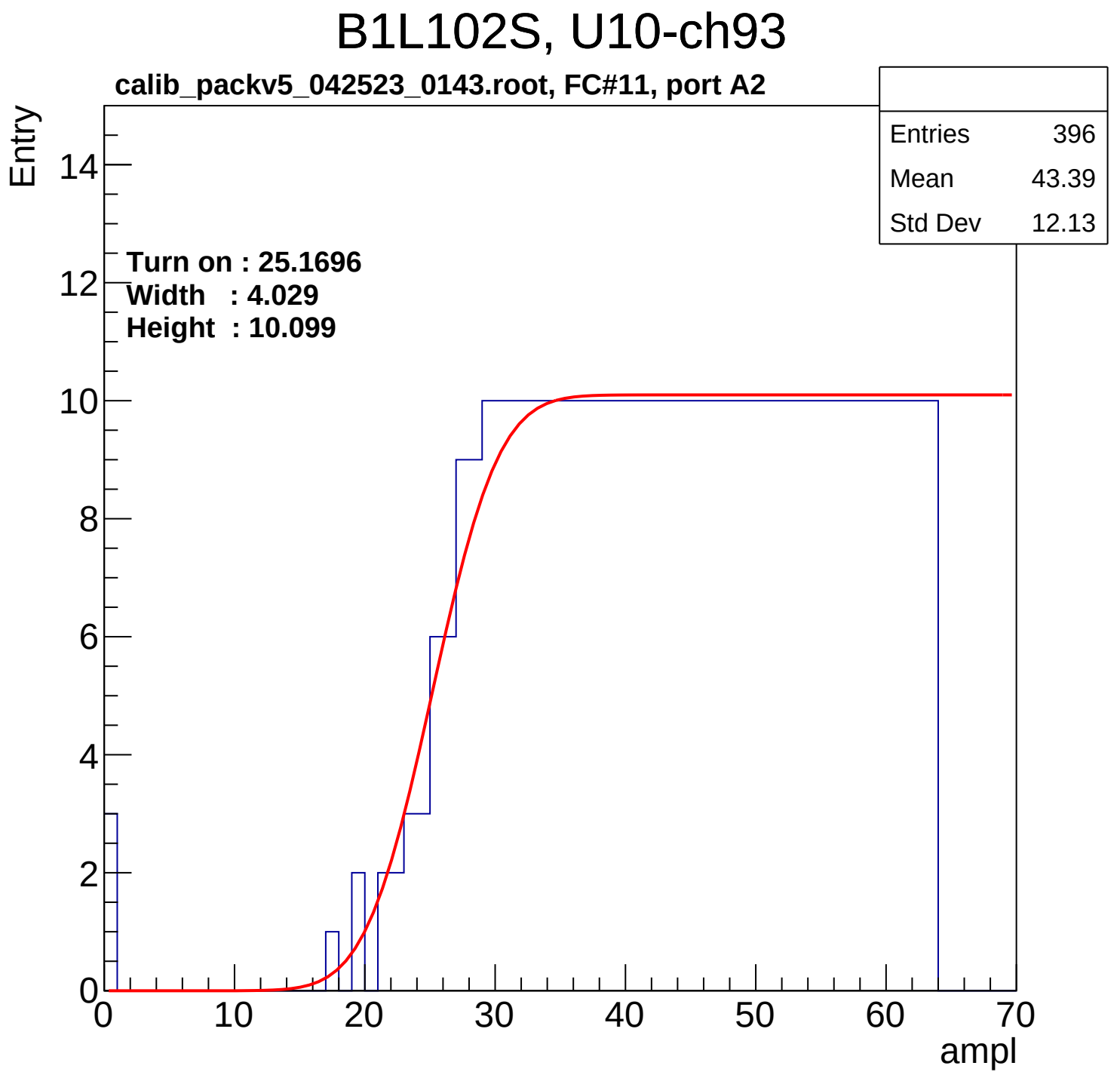
B1L102S, U10-ch93
calib_packv5_042523_0143.root, FC#11, port A2
Entries 396
Mean 43.39
Std Dev 12.13
Turn on : 25.1696
Width : 4.029
Height : 10.099
Entry
ampl
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2
4
6
8
10
12
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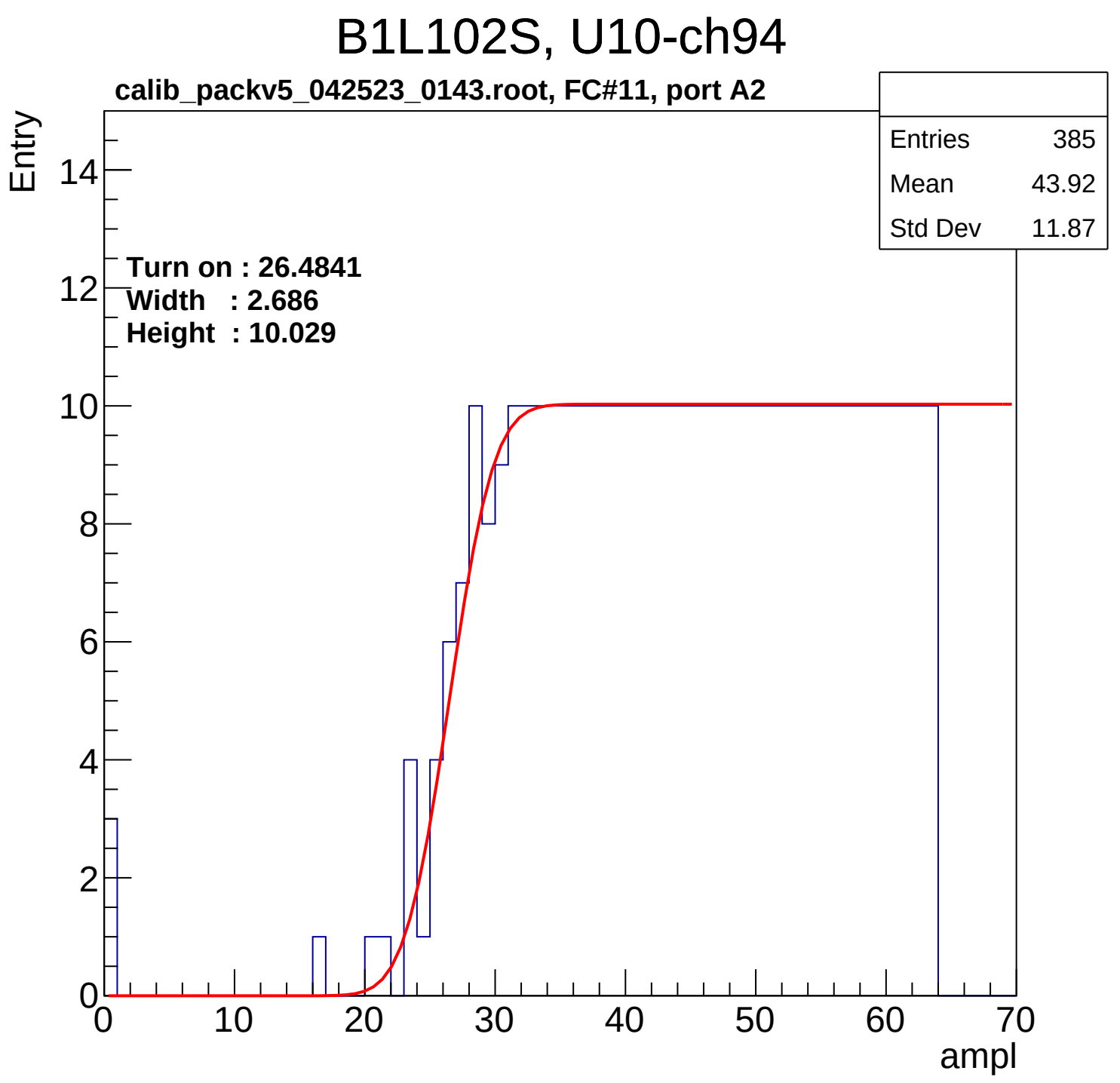
B1L102S, U10-ch94
calib_packv5_042523_0143.root, FC#11, port A2
Entries 385
Mean 43.92
Std Dev 11.87
Turn on : 26.4841
Width : 2.686
Height : 10.029
Entry
ampl
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2
4
6
8
10
12
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60
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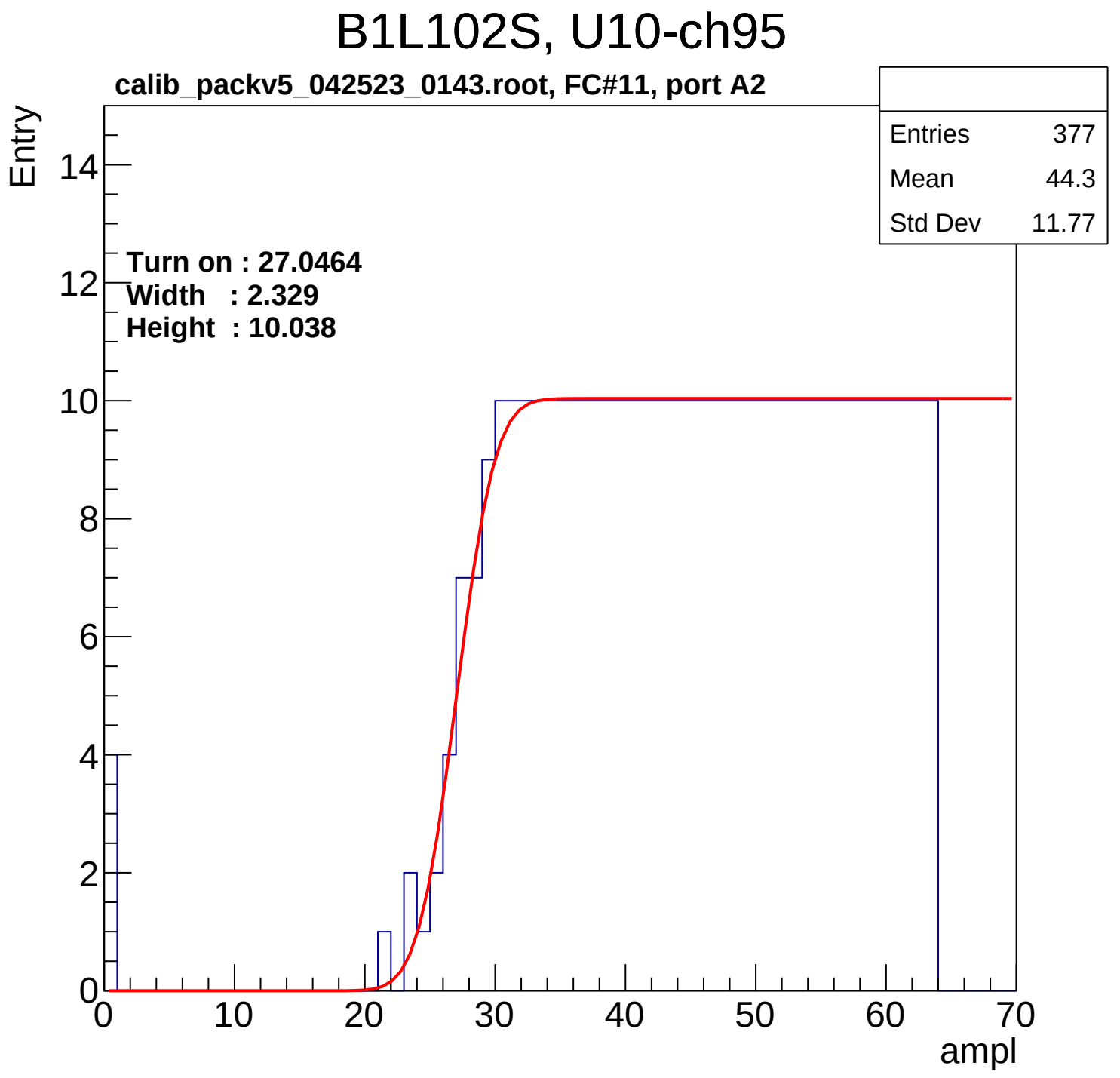
B1L102S, U10-ch95
calib_packv5_042523_0143.root, FC#11, port A2
Entries 377
Mean 44.3
Std Dev 11.77
Turn on : 27.0464
Width : 2.329
Height : 10.038
Entry
ampl
0
2
4
6
8
10
12
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0
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20
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60
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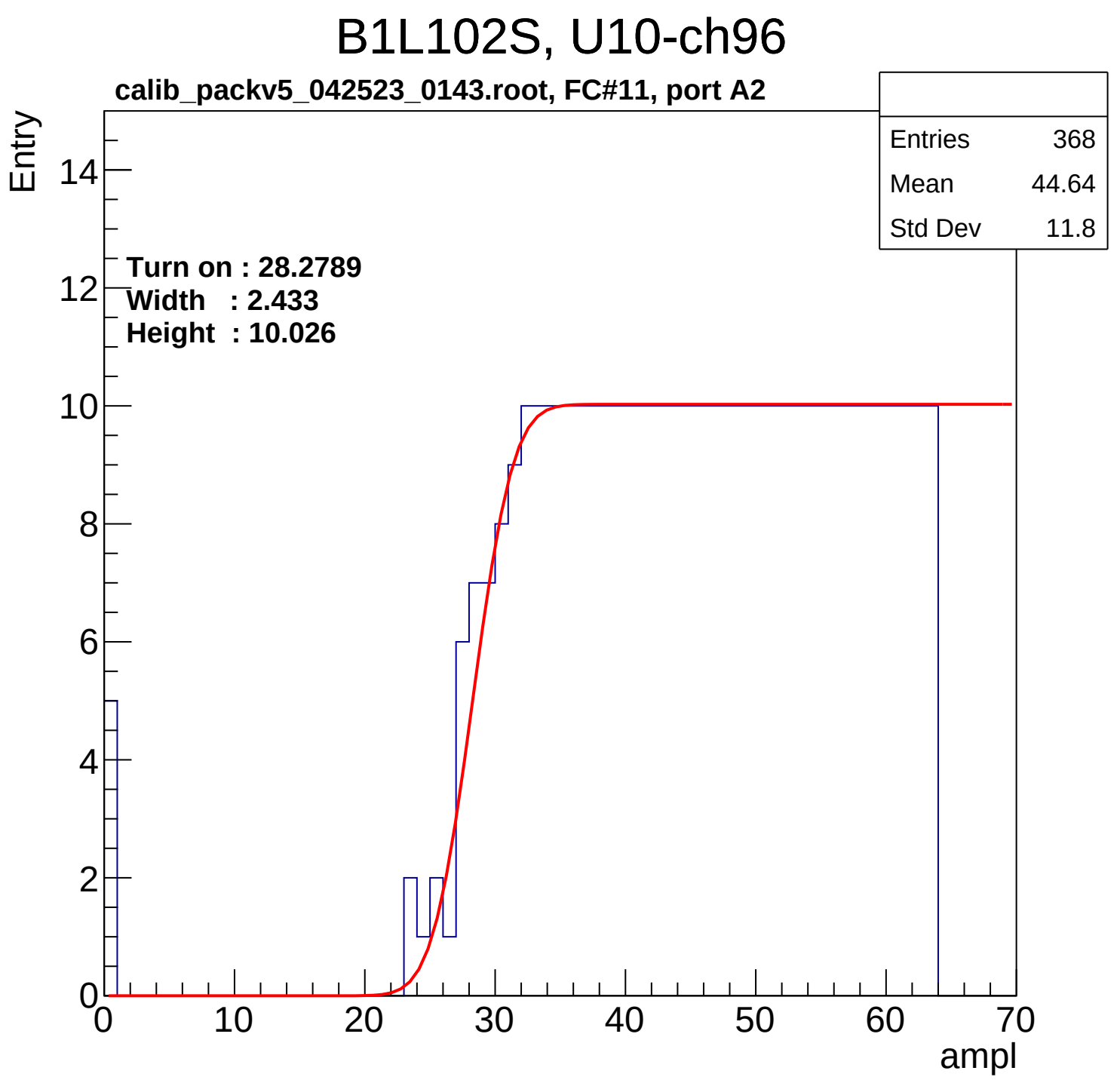
B1L102S, U10-ch96
calib_packv5_042523_0143.root, FC#11, port A2
Entries 368
Mean 44.64
Std Dev 11.8
Turn on : 28.2789
Width : 2.433
Height : 10.026
Entry
ampl
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2
4
6
8
10
12
14
0
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20
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40
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60
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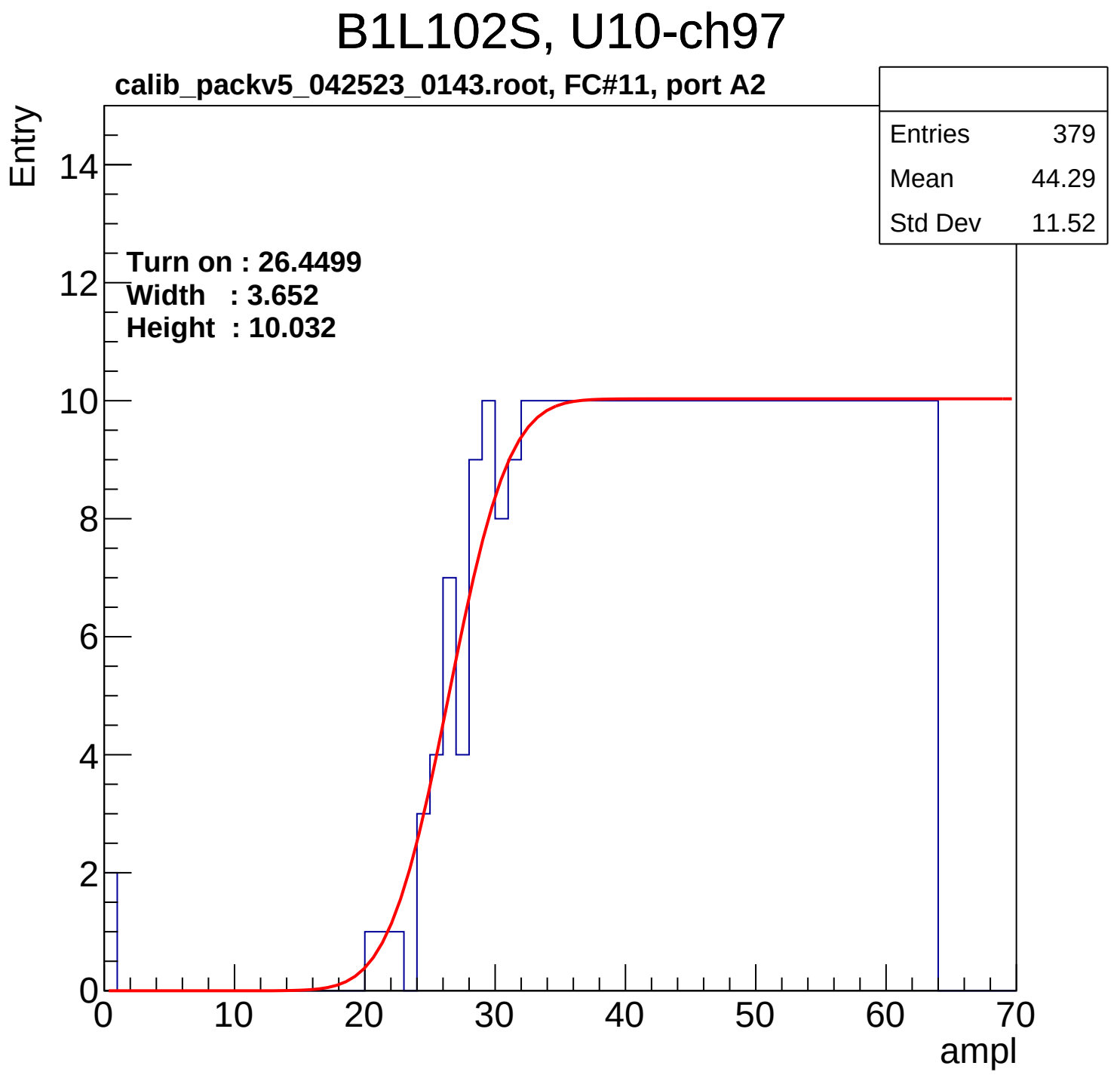
B1L102S, U10-ch97
calib_packv5_042523_0143.root, FC#11, port A2
Entries 379
Mean 44.29
Std Dev 11.52
Turn on : 26.4499
Width : 3.652
Height : 10.032
Entry
ampl
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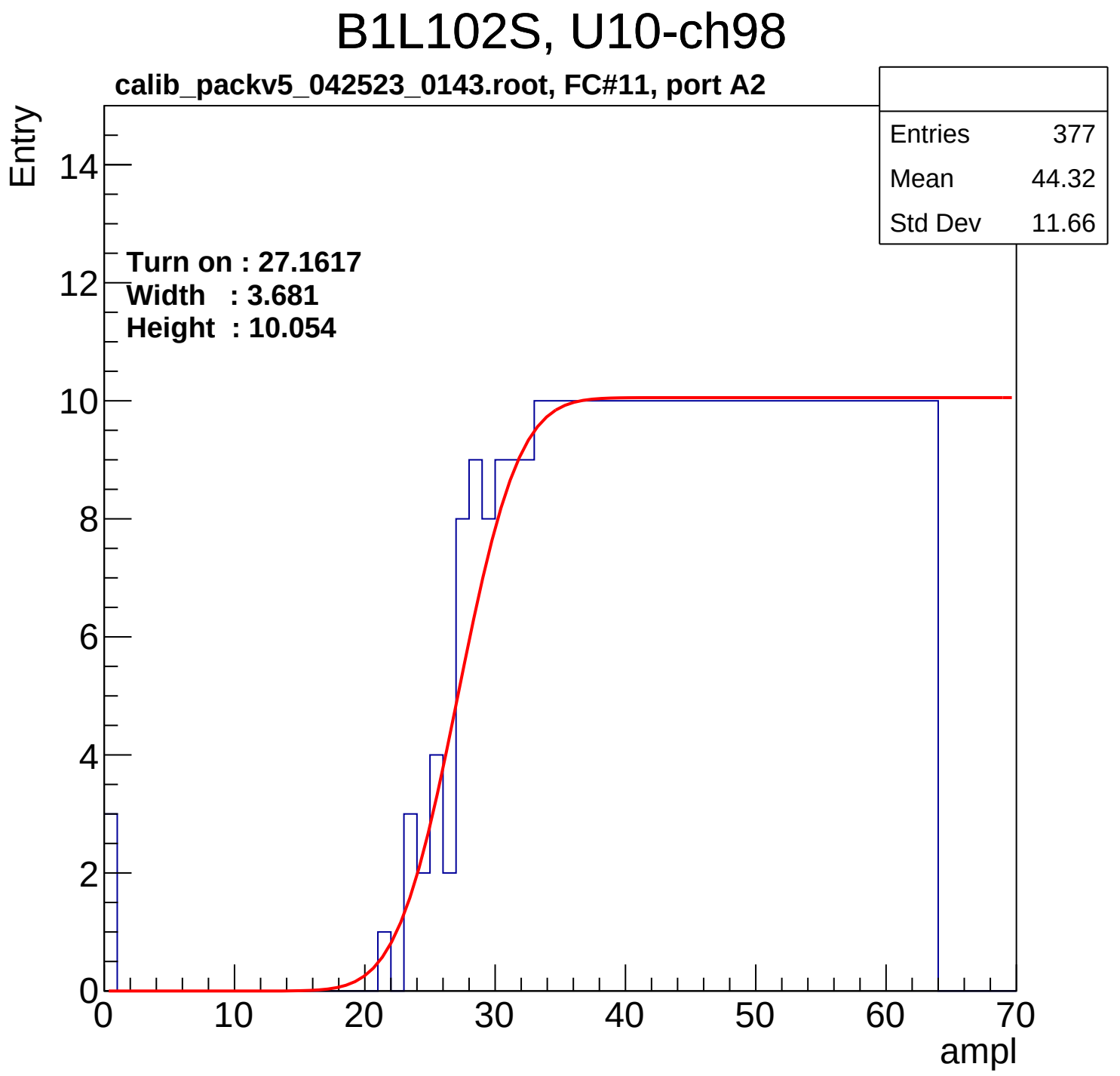
B1L102S, U10-ch98
calib_packv5_042523_0143.root, FC#11, port A2
Entries 377
Mean 44.32
Std Dev 11.66
Turn on : 27.1617
Width : 3.681
Height : 10.054
Entry
ampl
0
2
4
6
8
10
12
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0
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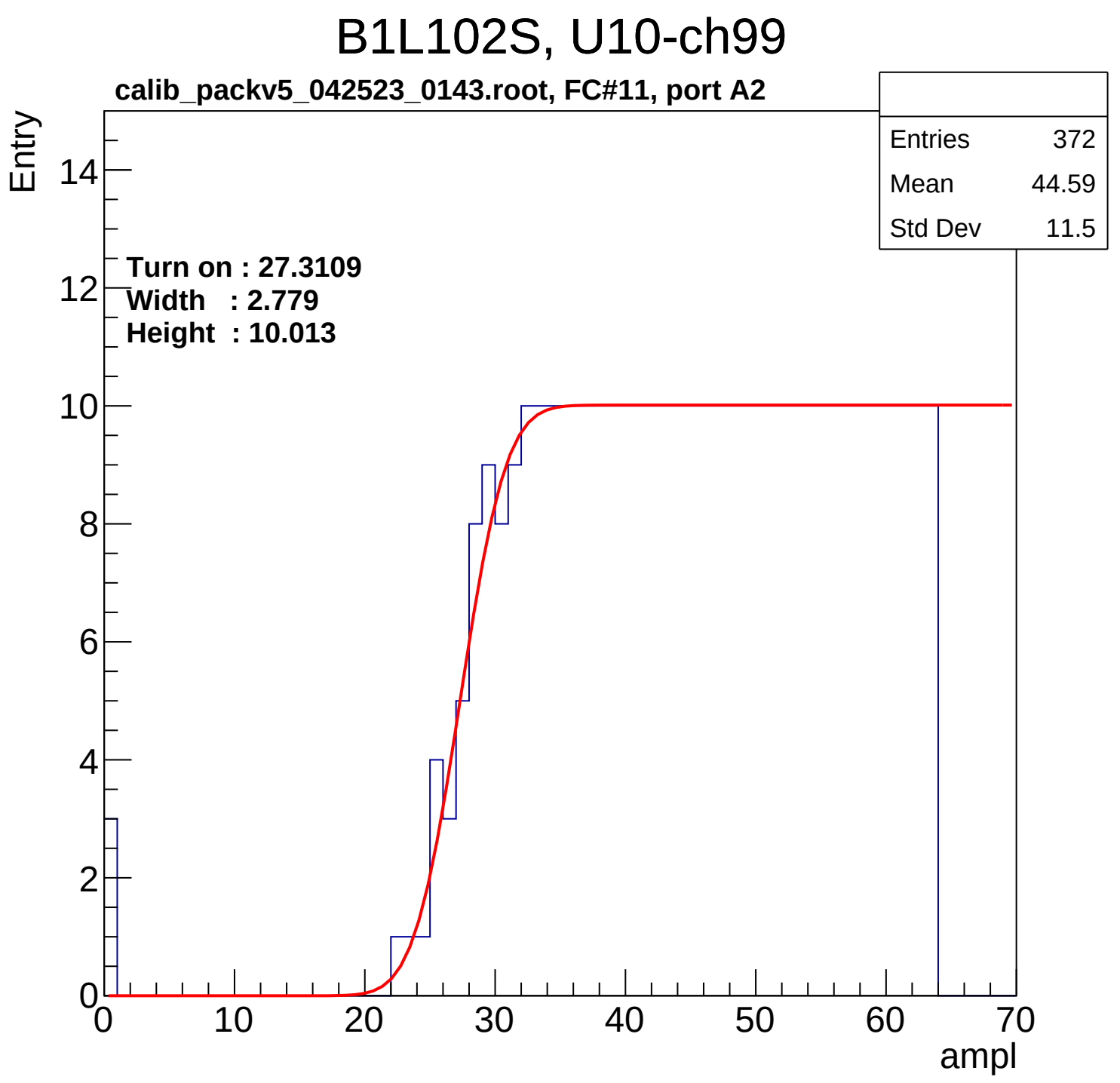
B1L102S, U10-ch99
calib_packv5_042523_0143.root, FC#11, port A2
Entries 372
Mean 44.59
Std Dev 11.5
Turn on : 27.3109
Width : 2.779
Height : 10.013
Entry
ampl
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6
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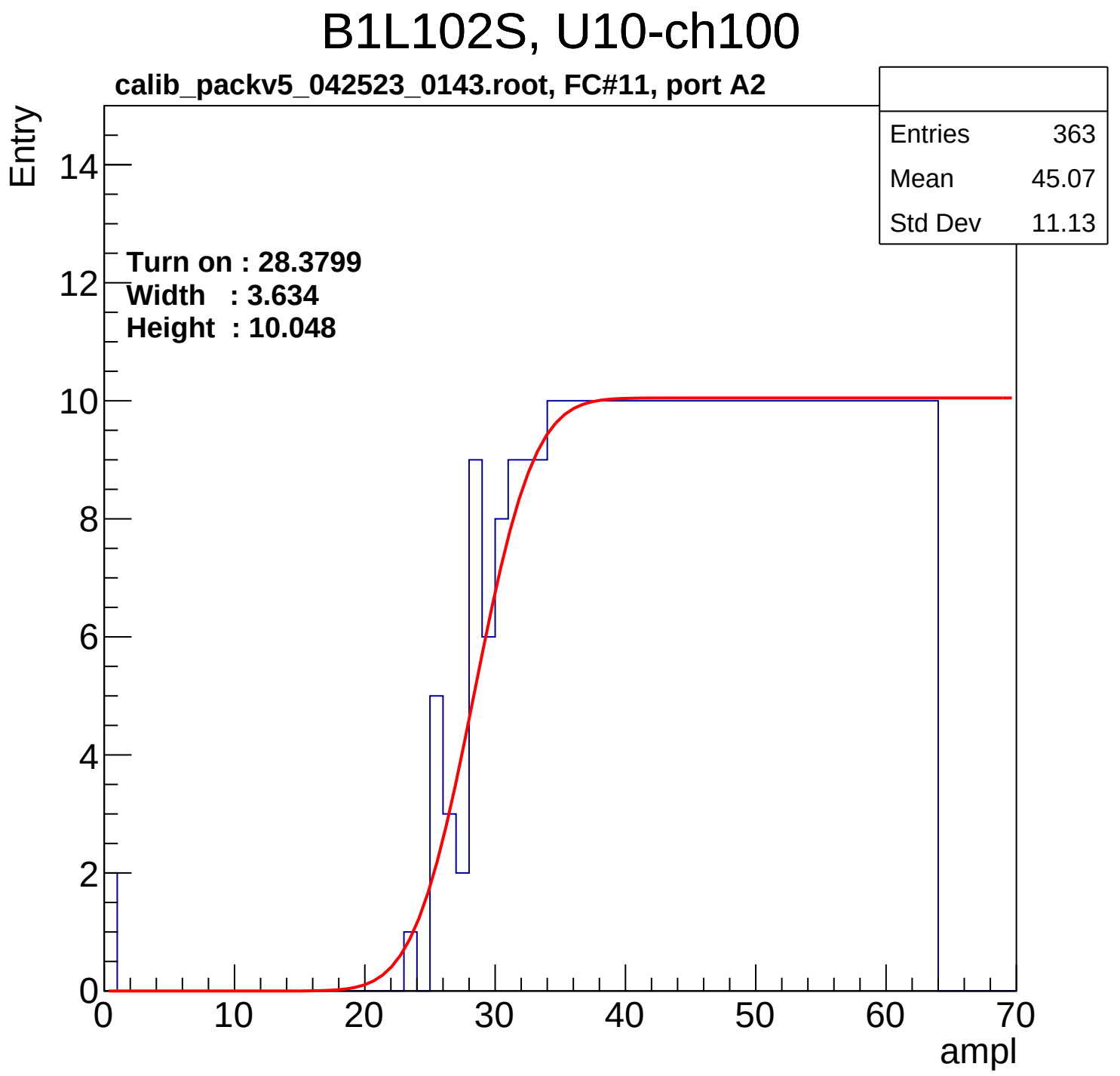
B1L102S, U10-ch100
calib_packv5_042523_0143.root, FC#11, port A2
Entries 363
Mean 45.07
Std Dev 11.13
Turn on : 28.3799
Width : 3.634
Height : 10.048
Entry
ampl
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8
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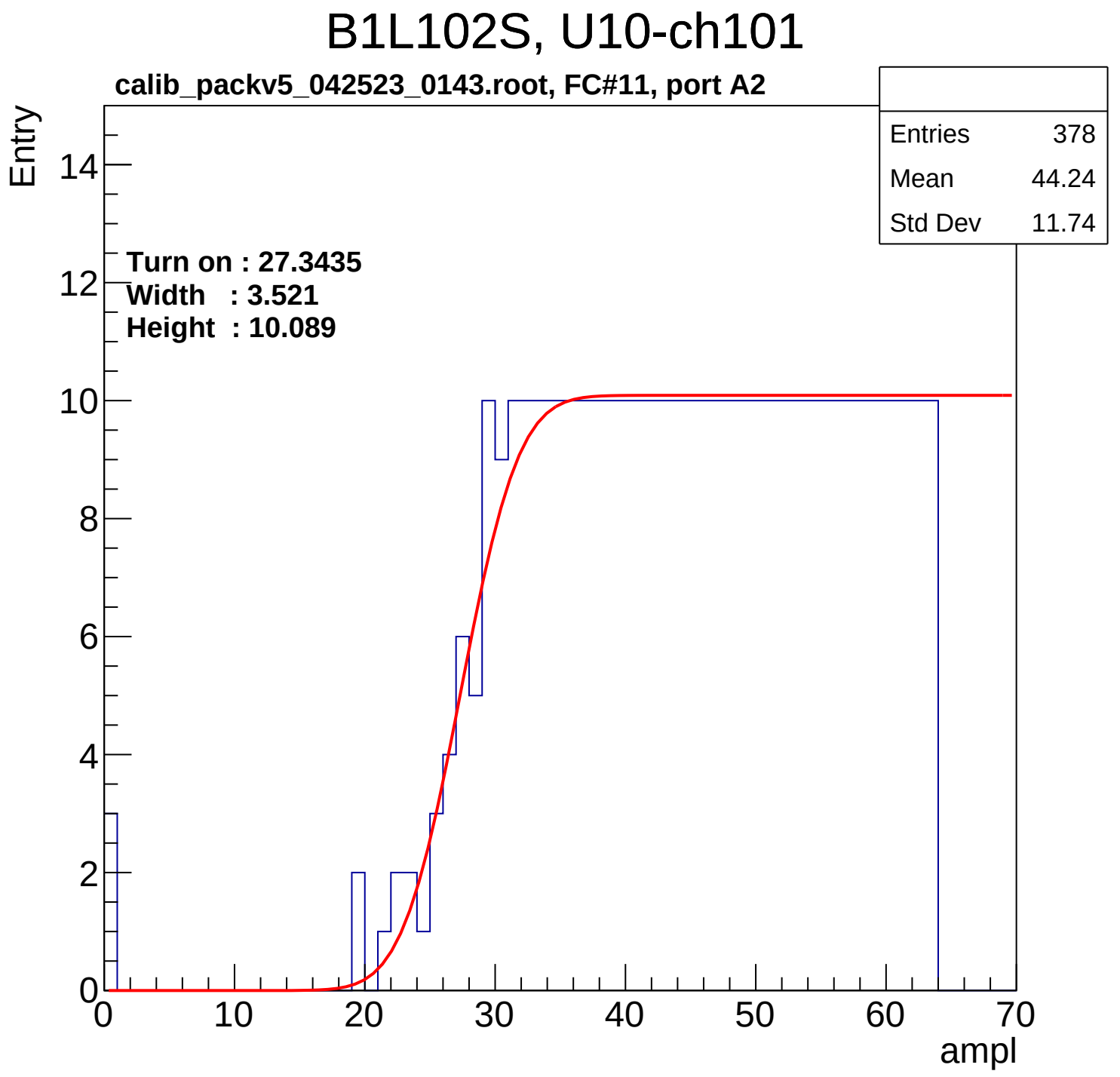
B1L102S, U10-ch101
calib_packv5_042523_0143.root, FC#11, port A2
Entries 378
Mean 44.24
Std Dev 11.74
Turn on : 27.3435
Width : 3.521
Height : 10.089
Entry
ampl
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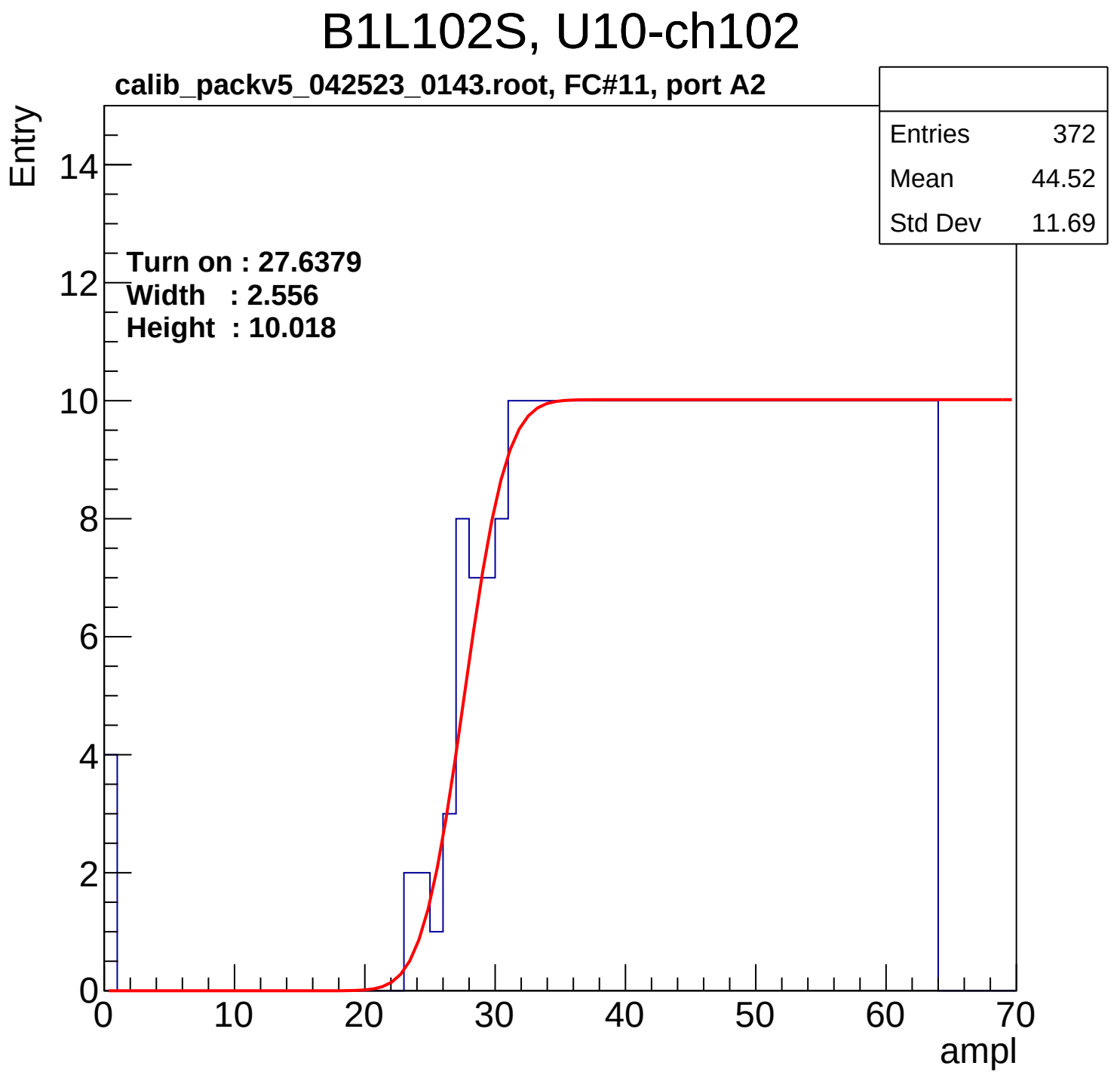
B1L102S, U10-ch102
calib_packv5_042523_0143.root, FC#11, port A2
Entries 372
Mean 44.52
Std Dev 11.69
Turn on : 27.6379
Width : 2.556
Height : 10.018
Entry
ampl
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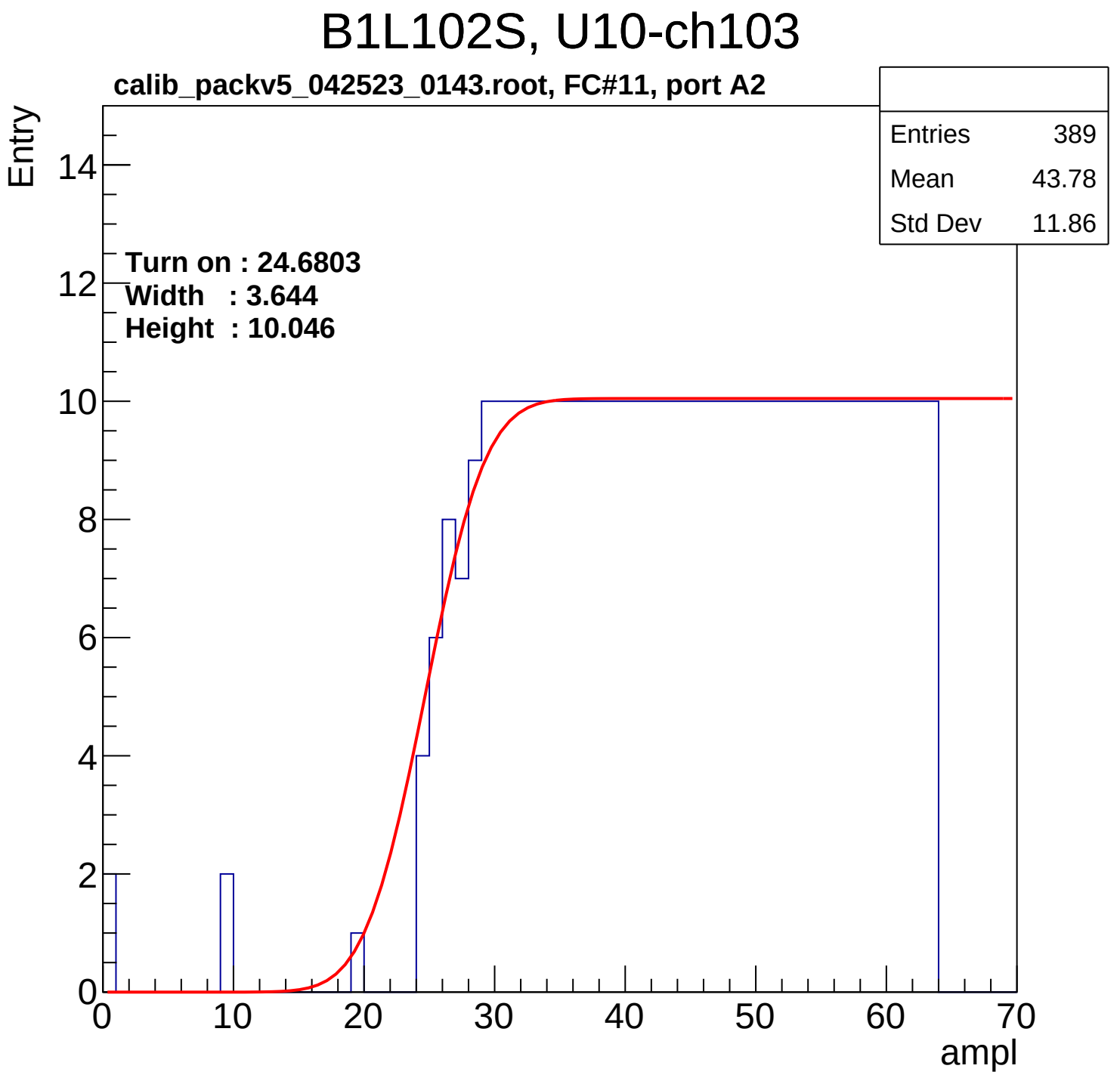
B1L102S, U10-ch103
calib_packv5_042523_0143.root, FC#11, port A2
Entries 389
Mean 43.78
Std Dev 11.86
Turn on : 24.6803
Width : 3.644
Height : 10.046
Entry
ampl
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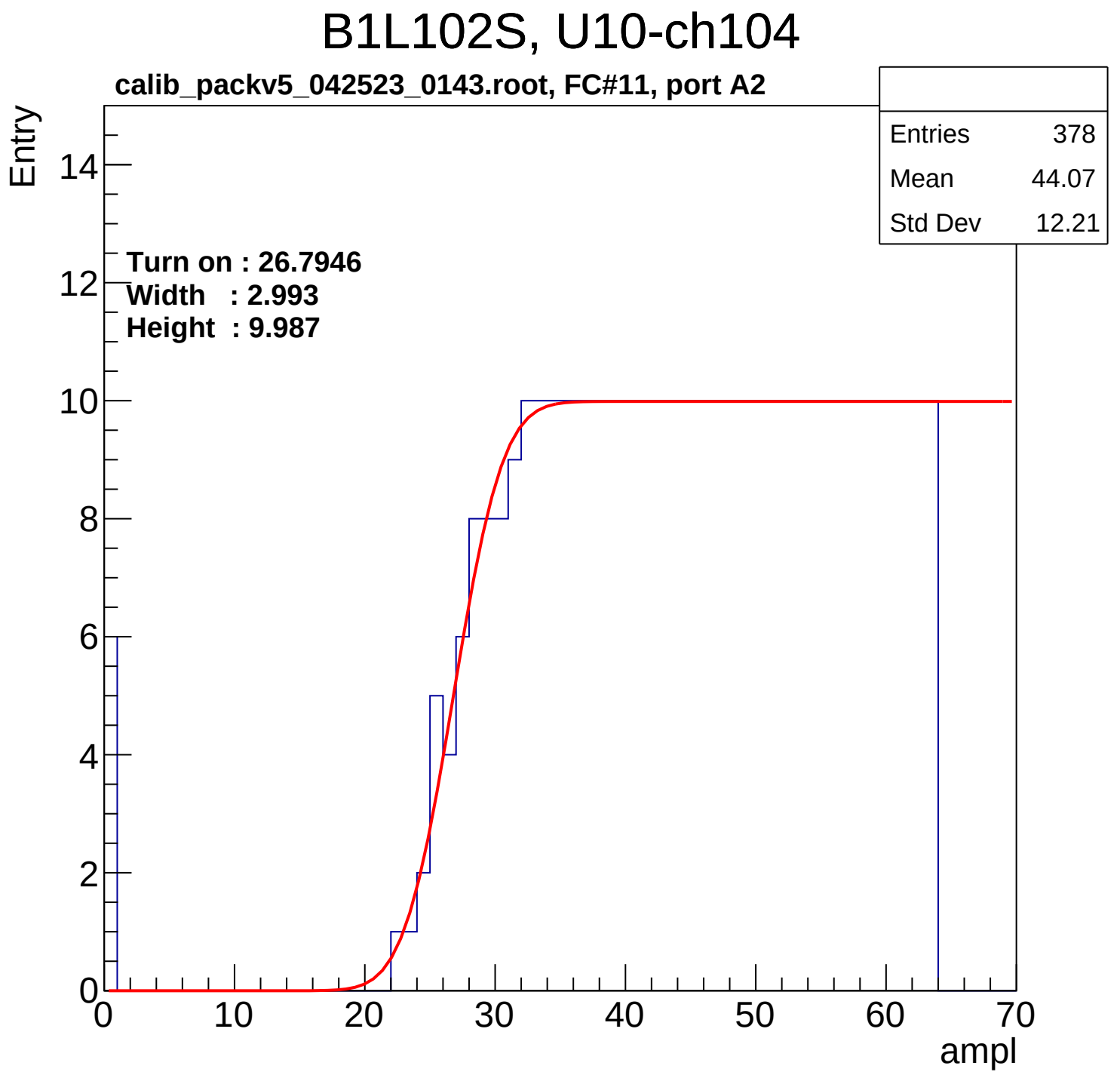
B1L102S, U10-ch104
calib_packv5_042523_0143.root, FC#11, port A2
Entries 378
Mean 44.07
Std Dev 12.21
Turn on : 26.7946
Width : 2.993
Height : 9.987
Entry
ampl
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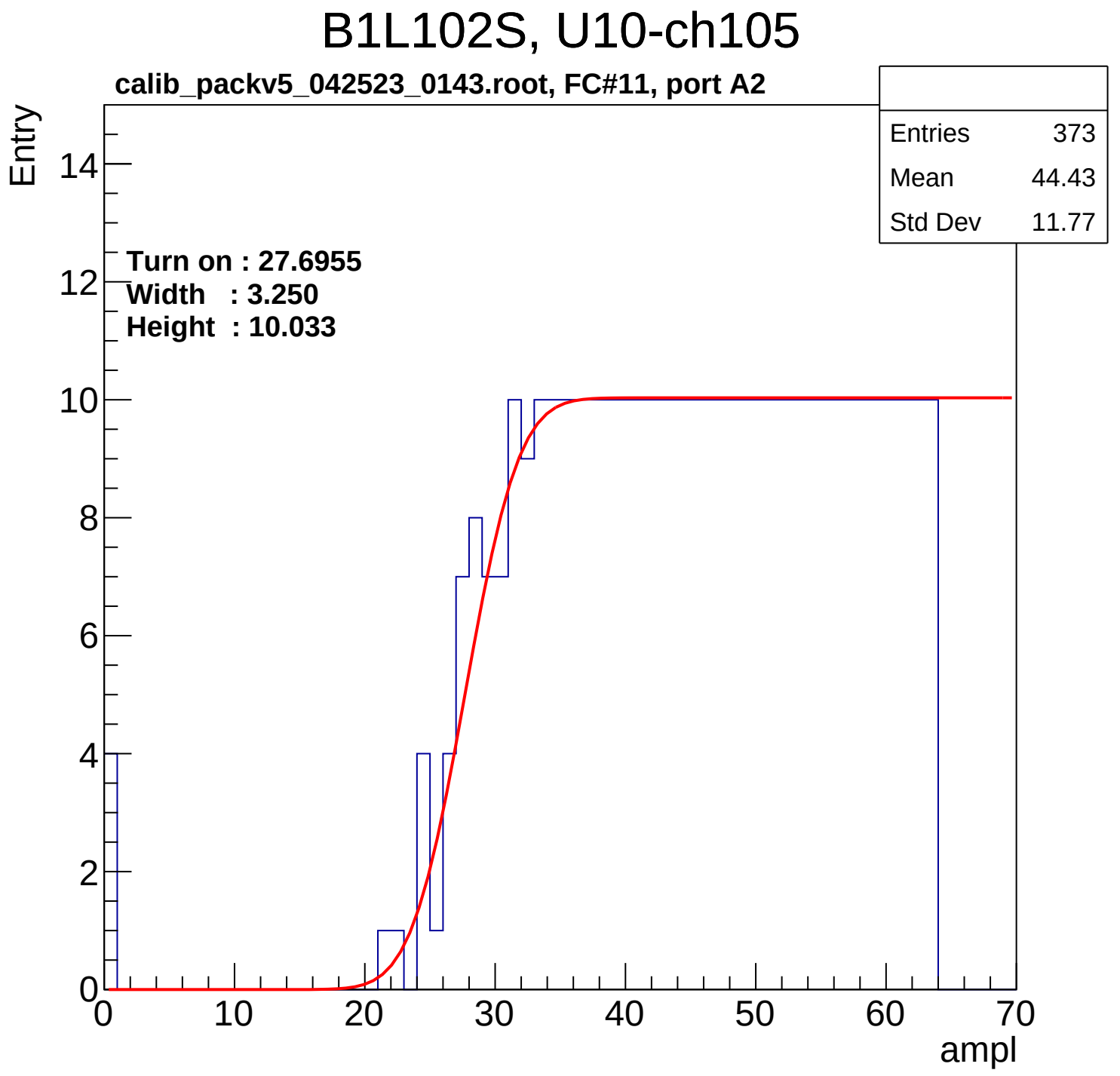
B1L102S, U10-ch105
calib_packv5_042523_0143.root, FC#11, port A2
Entries 373
Mean 44.43
Std Dev 11.77
Turn on : 27.6955
Width : 3.250
Height : 10.033
Entry
ampl
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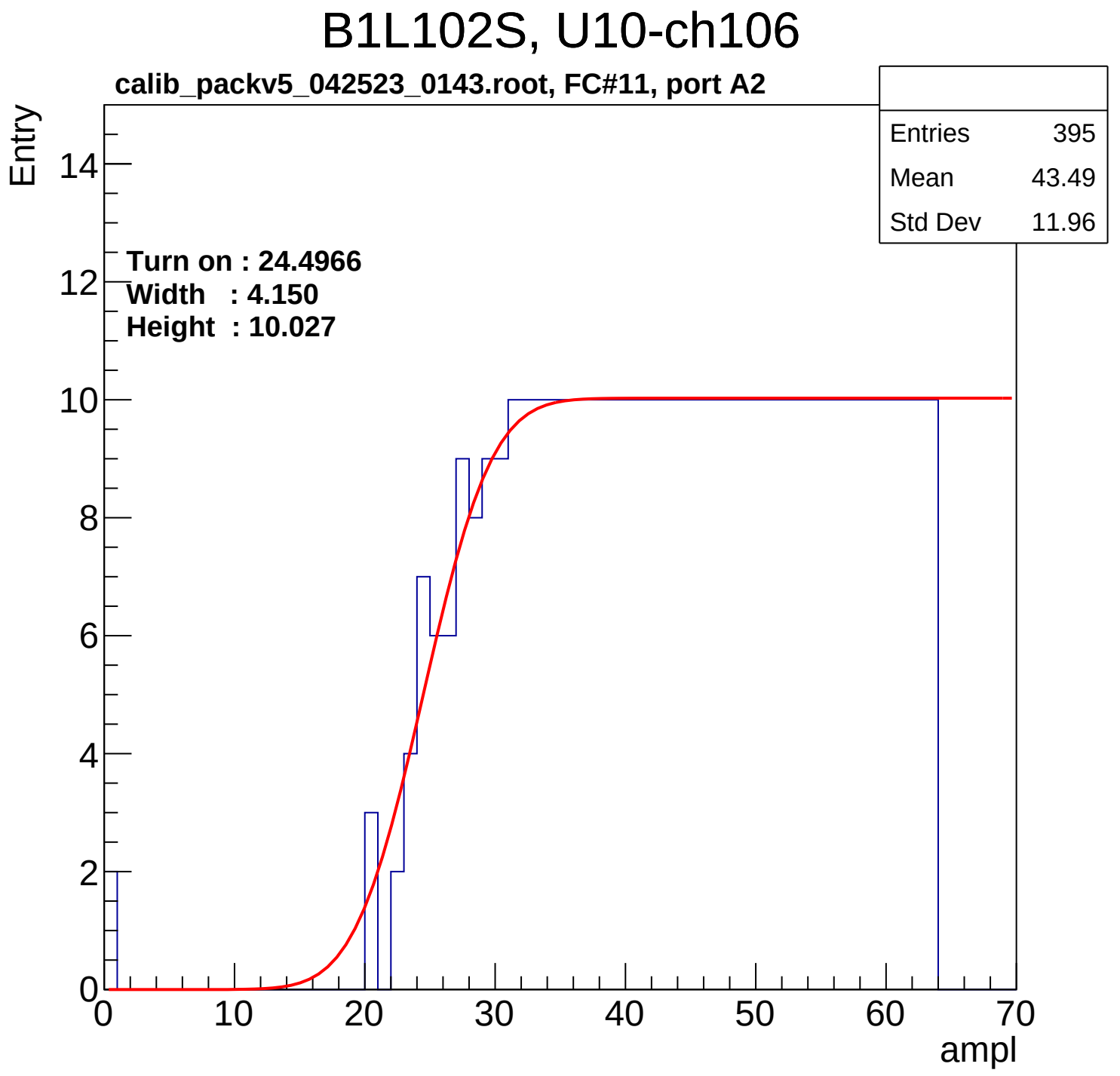
B1L102S, U10-ch106
calib_packv5_042523_0143.root, FC#11, port A2
Entries 395
Mean 43.49
Std Dev 11.96
Turn on : 24.4966
Width : 4.150
Height : 10.027
Entry
ampl
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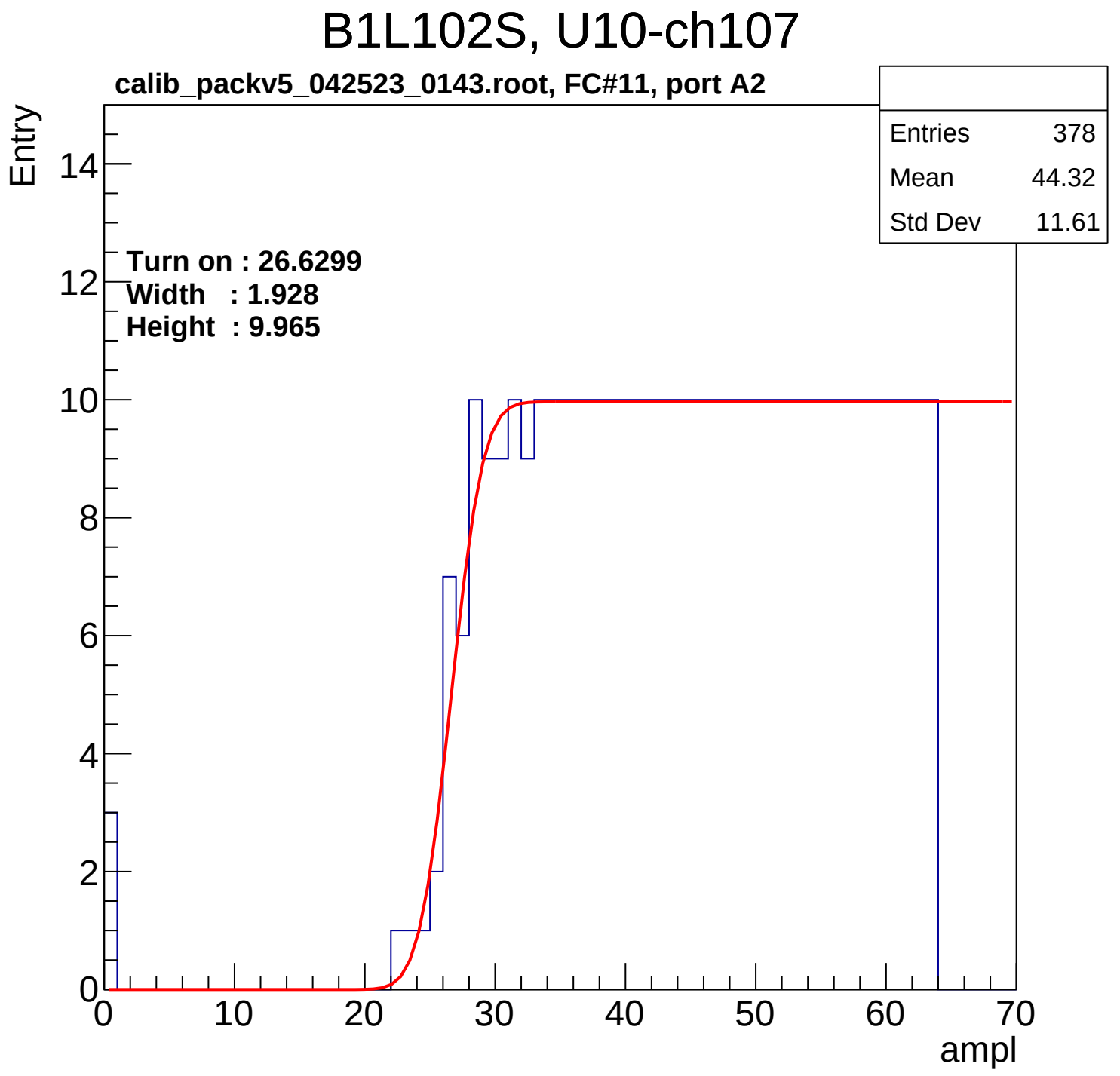
B1L102S, U10-ch107
calib_packv5_042523_0143.root, FC#11, port A2
Entries 378
Mean 44.32
Std Dev 11.61
Turn on : 26.6299
Width : 1.928
Height : 9.965
Entry
ampl
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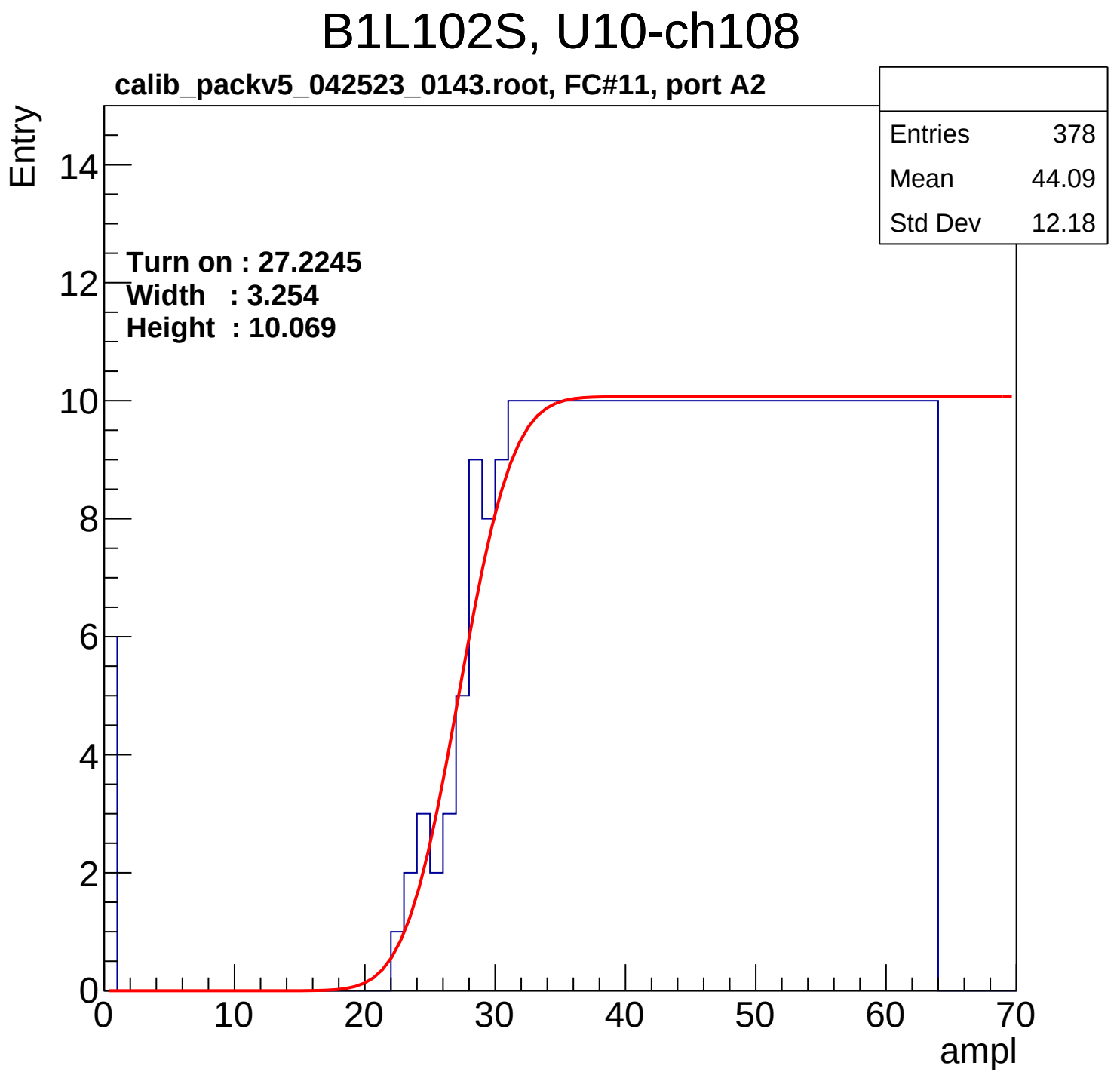
B1L102S, U10-ch108
calib_packv5_042523_0143.root, FC#11, port A2
Entries 378
Mean 44.09
Std Dev 12.18
Turn on : 27.2245
Width : 3.254
Height : 10.069
Entry
ampl
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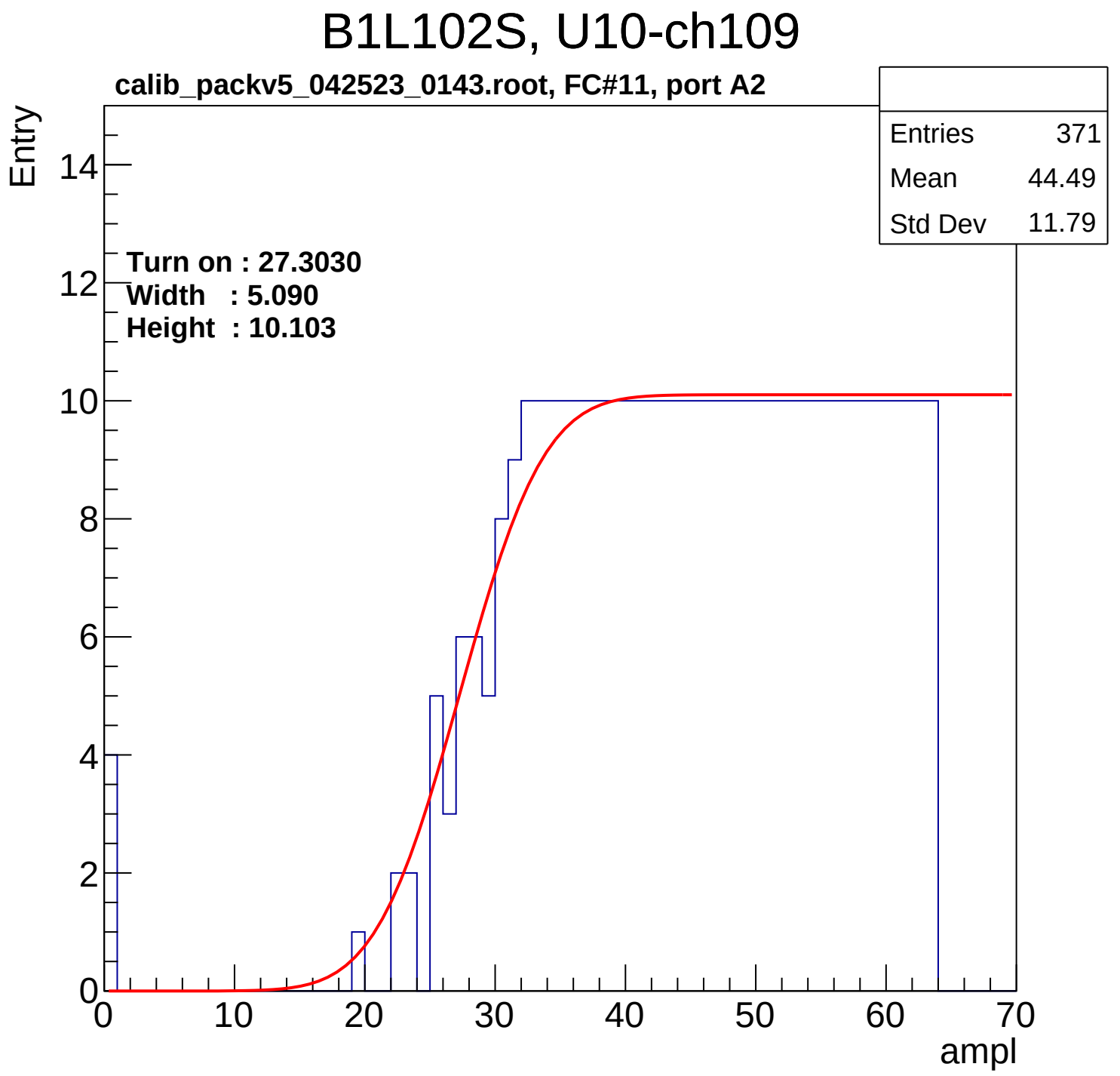
B1L102S, U10-ch109
calib_packv5_042523_0143.root, FC#11, port A2
Entries 371
Mean 44.49
Std Dev 11.79
Turn on : 27.3030
Width : 5.090
Height : 10.103
Entry
ampl
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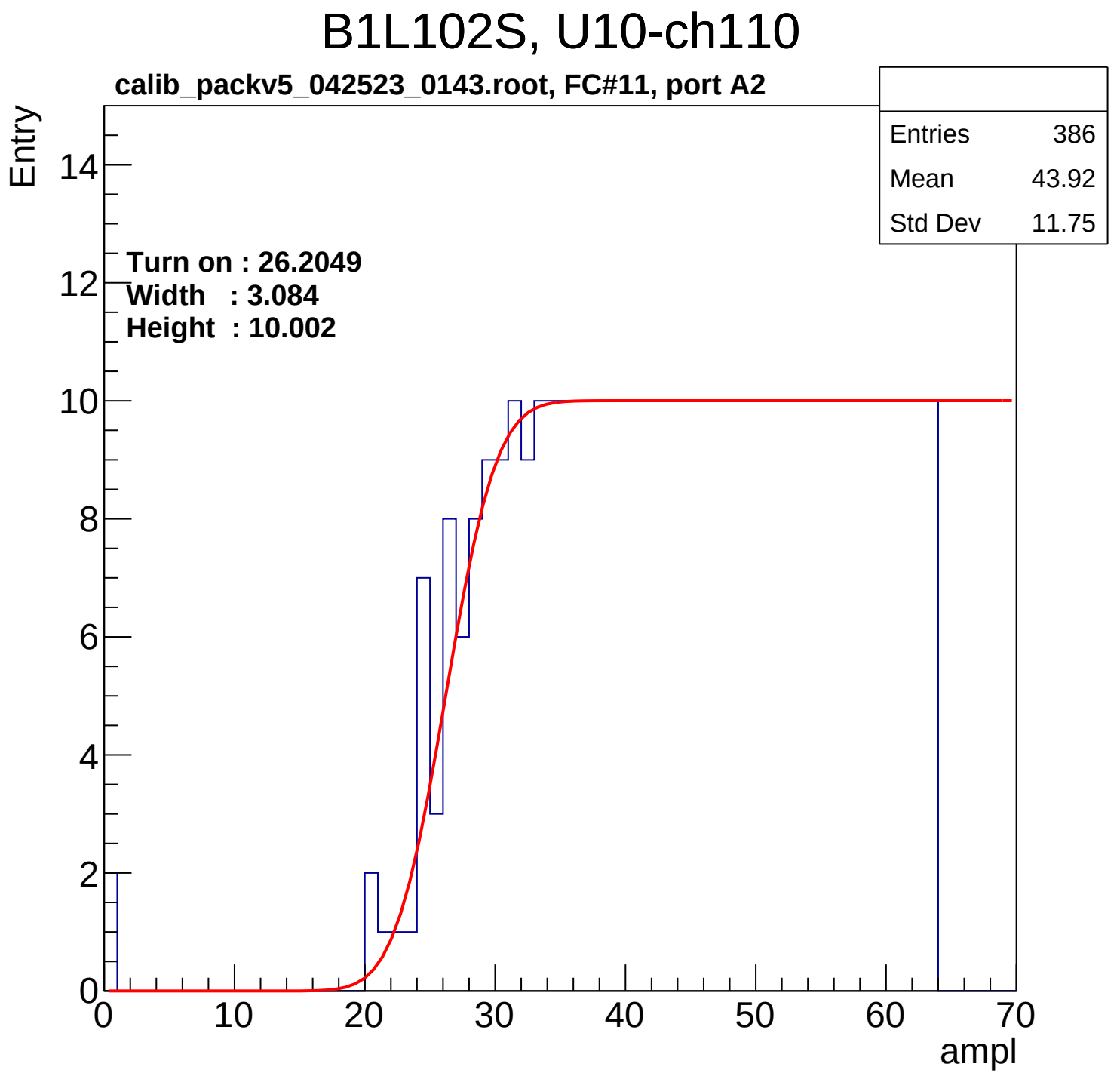
B1L102S, U10-ch110
calib_packv5_042523_0143.root, FC#11, port A2
Entries 386
Mean 43.92
Std Dev 11.75
Turn on : 26.2049
Width : 3.084
Height : 10.002
Entry
ampl
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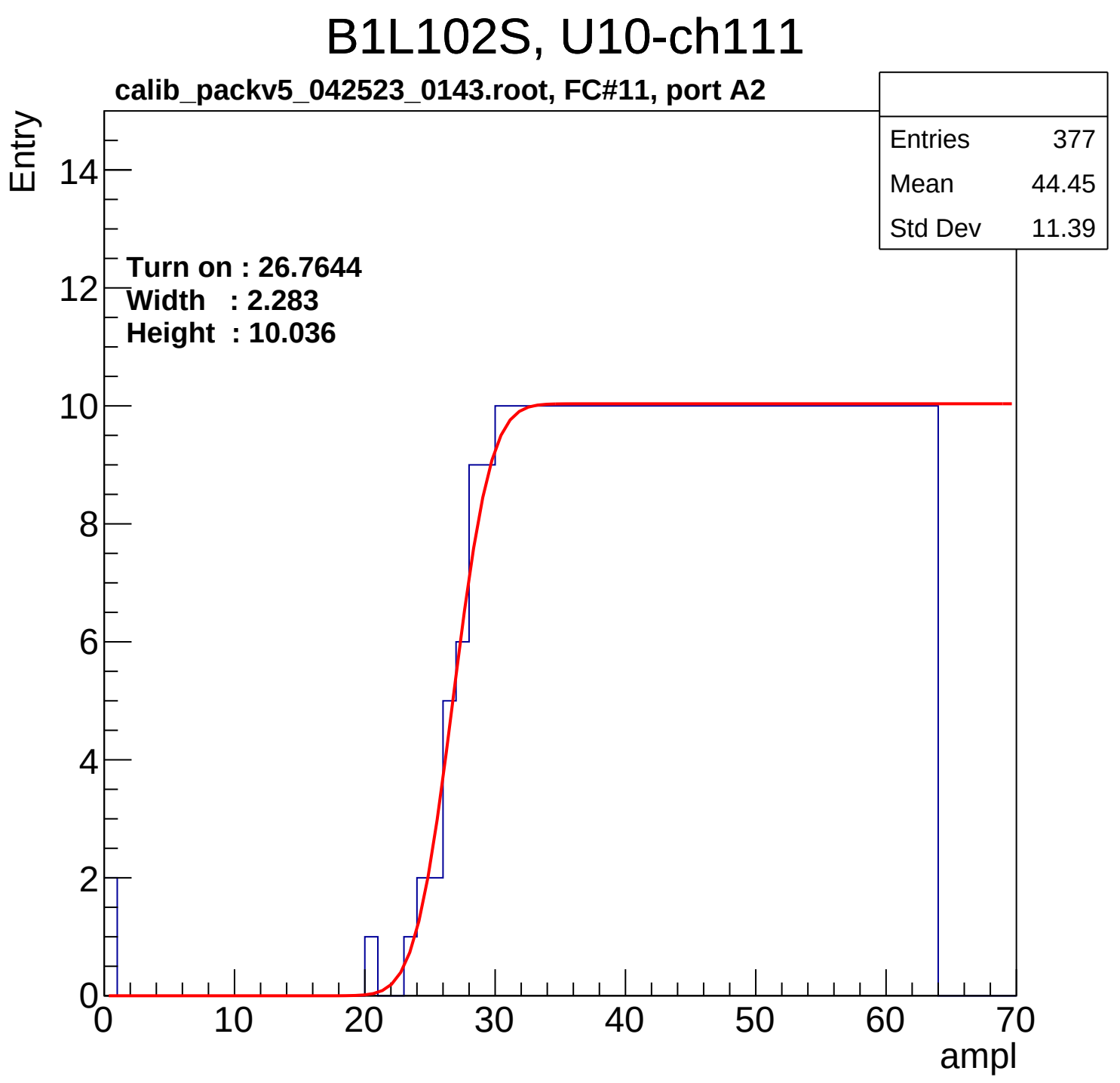
B1L102S, U10-ch111
calib_packv5_042523_0143.root, FC#11, port A2
Entries 377
Mean 44.45
Std Dev 11.39
Turn on : 26.7644
Width : 2.283
Height : 10.036
Entry
ampl
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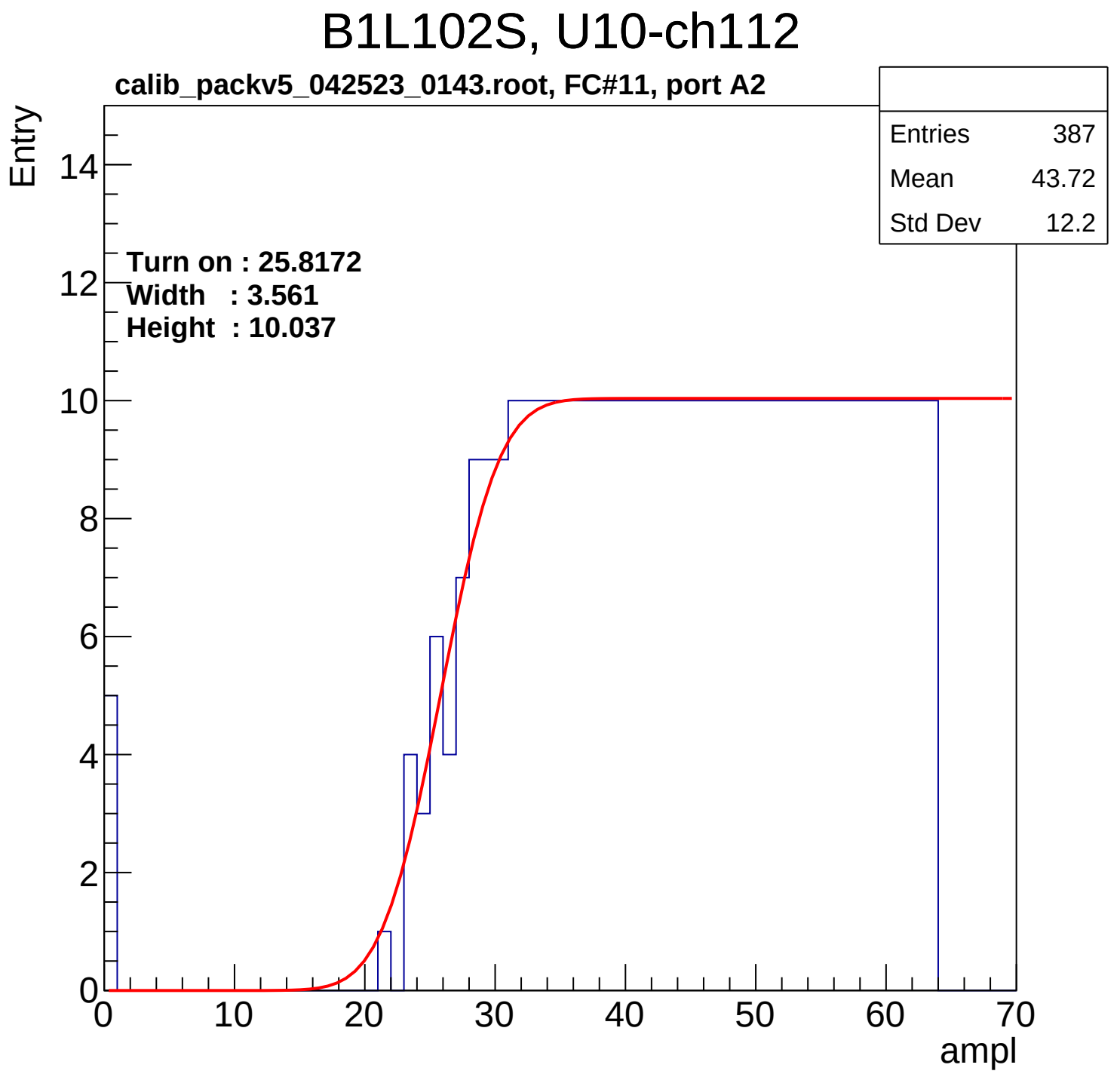
B1L102S, U10-ch112
calib_packv5_042523_0143.root, FC#11, port A2
Entries 387
Mean 43.72
Std Dev 12.2
Turn on : 25.8172
Width : 3.561
Height : 10.037
Entry
ampl
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8
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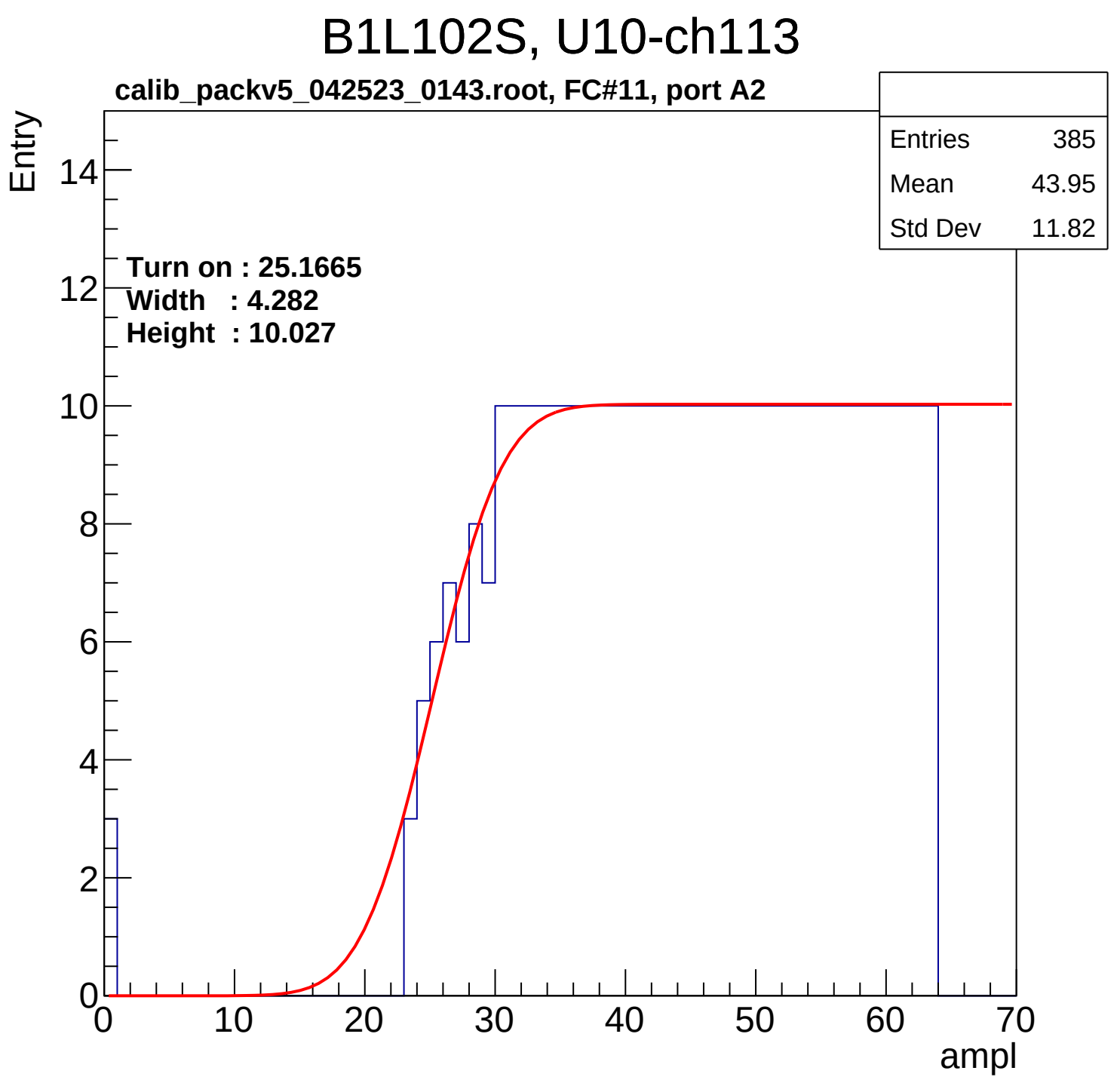
B1L102S, U10-ch113
calib_packv5_042523_0143.root, FC#11, port A2
Entries 385
Mean 43.95
Std Dev 11.82
Turn on : 25.1665
Width : 4.282
Height : 10.027
Entry
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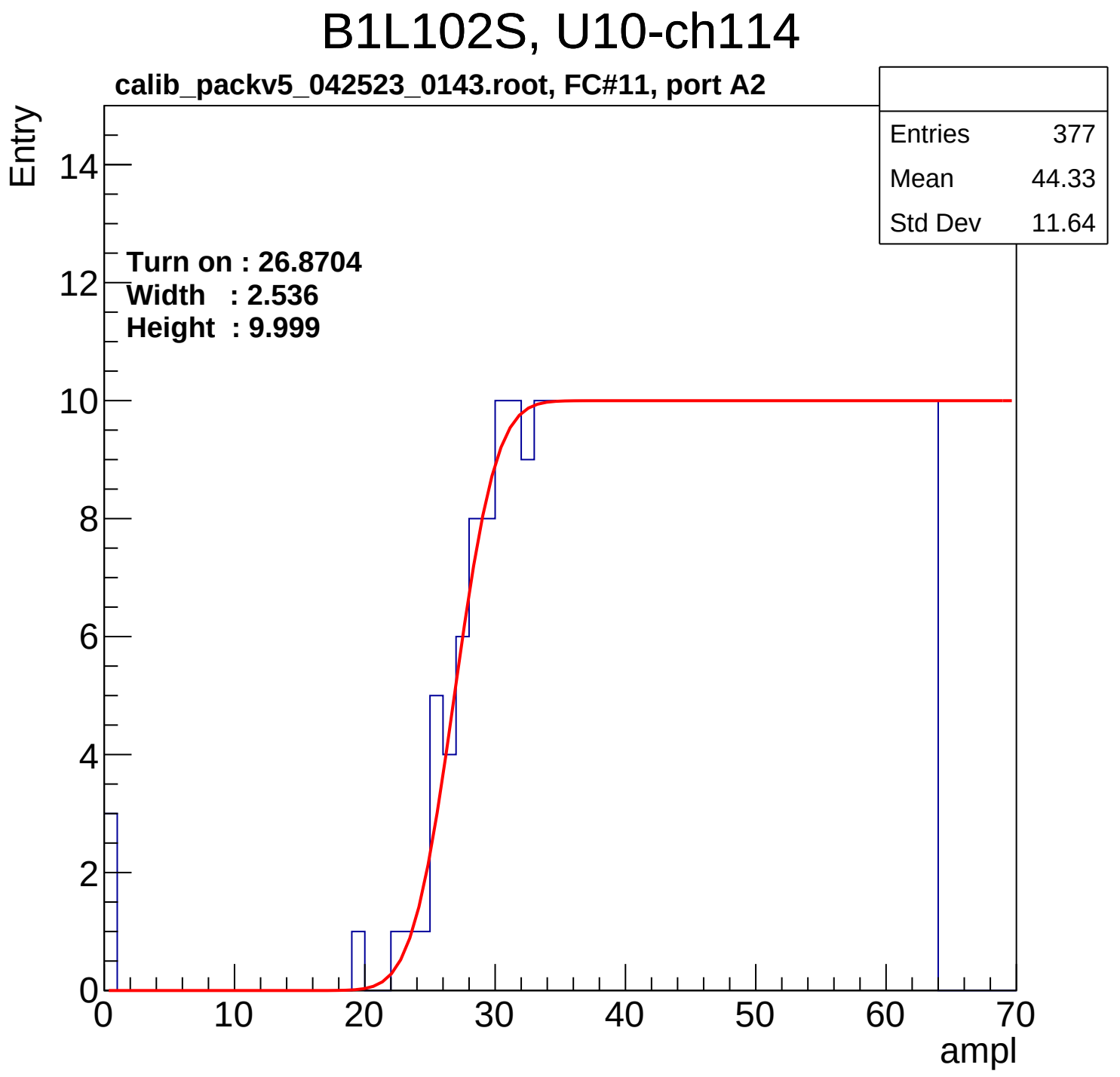
B1L102S, U10-ch114
calib_packv5_042523_0143.root, FC#11, port A2
Entries 377
Mean 44.33
Std Dev 11.64
Turn on : 26.8704
Width : 2.536
Height : 9.999
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ampl
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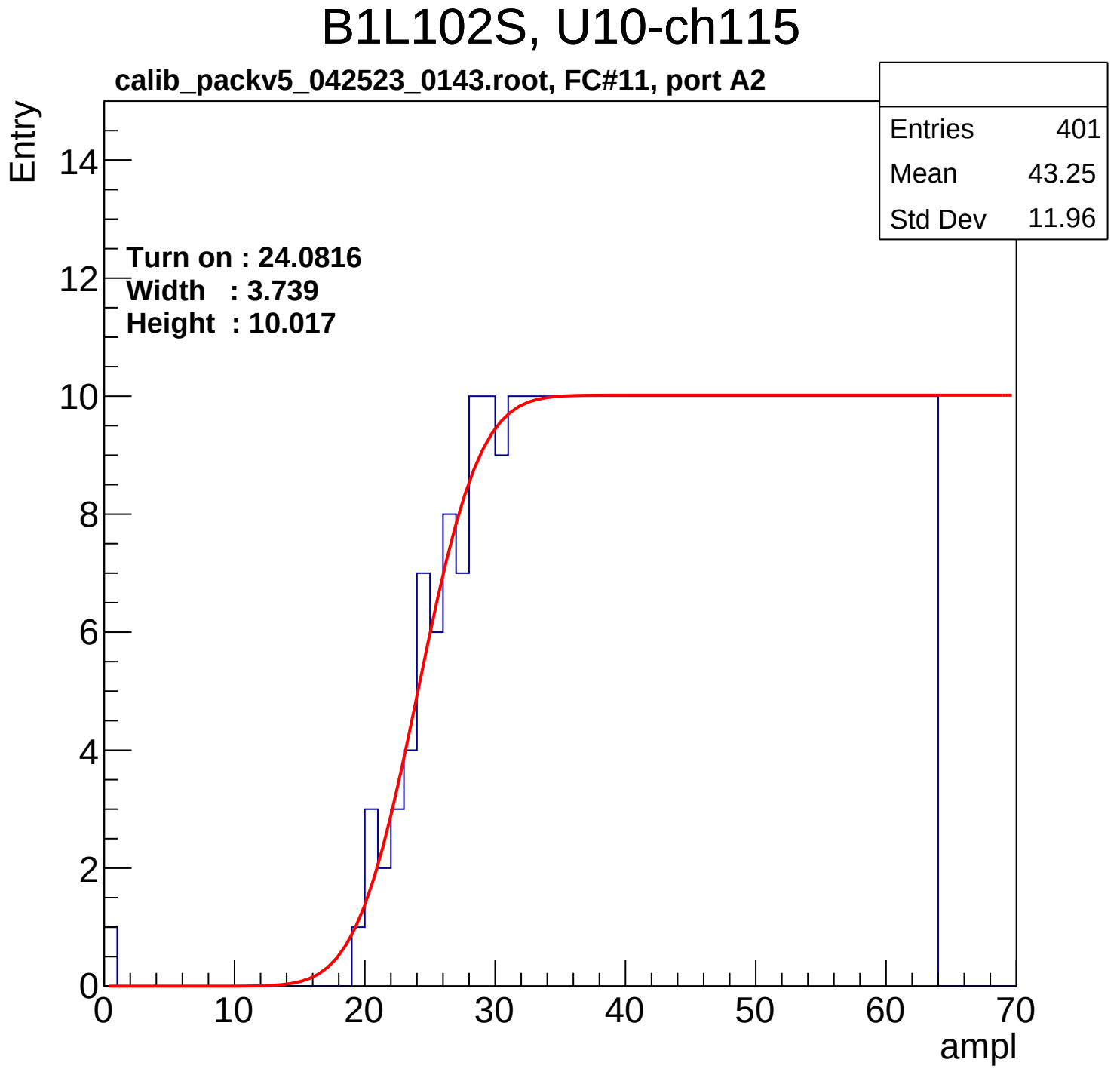
B1L102S, U10-ch115
calib_packv5_042523_0143.root, FC#11, port A2
Entries 401
Mean 43.25
Std Dev 11.96
Turn on : 24.0816
Width : 3.739
Height : 10.017
Entry
ampl
0
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4
6
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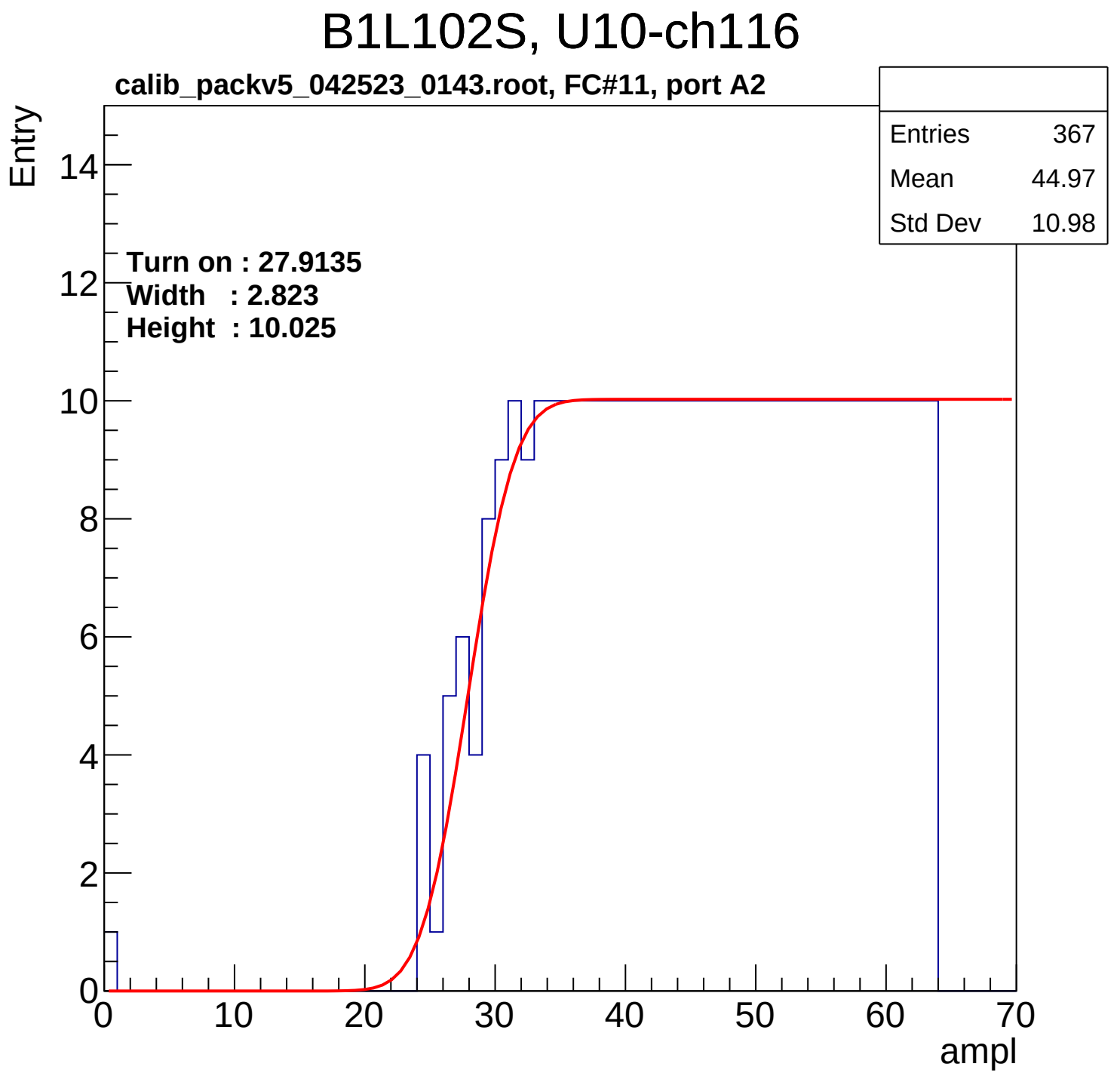
B1L102S, U10-ch116
calib_packv5_042523_0143.root, FC#11, port A2
Entries 367
Mean 44.97
Std Dev 10.98
Turn on : 27.9135
Width : 2.823
Height : 10.025
Entry
ampl
0
2
4
6
8
10
12
14
0
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20
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40
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60
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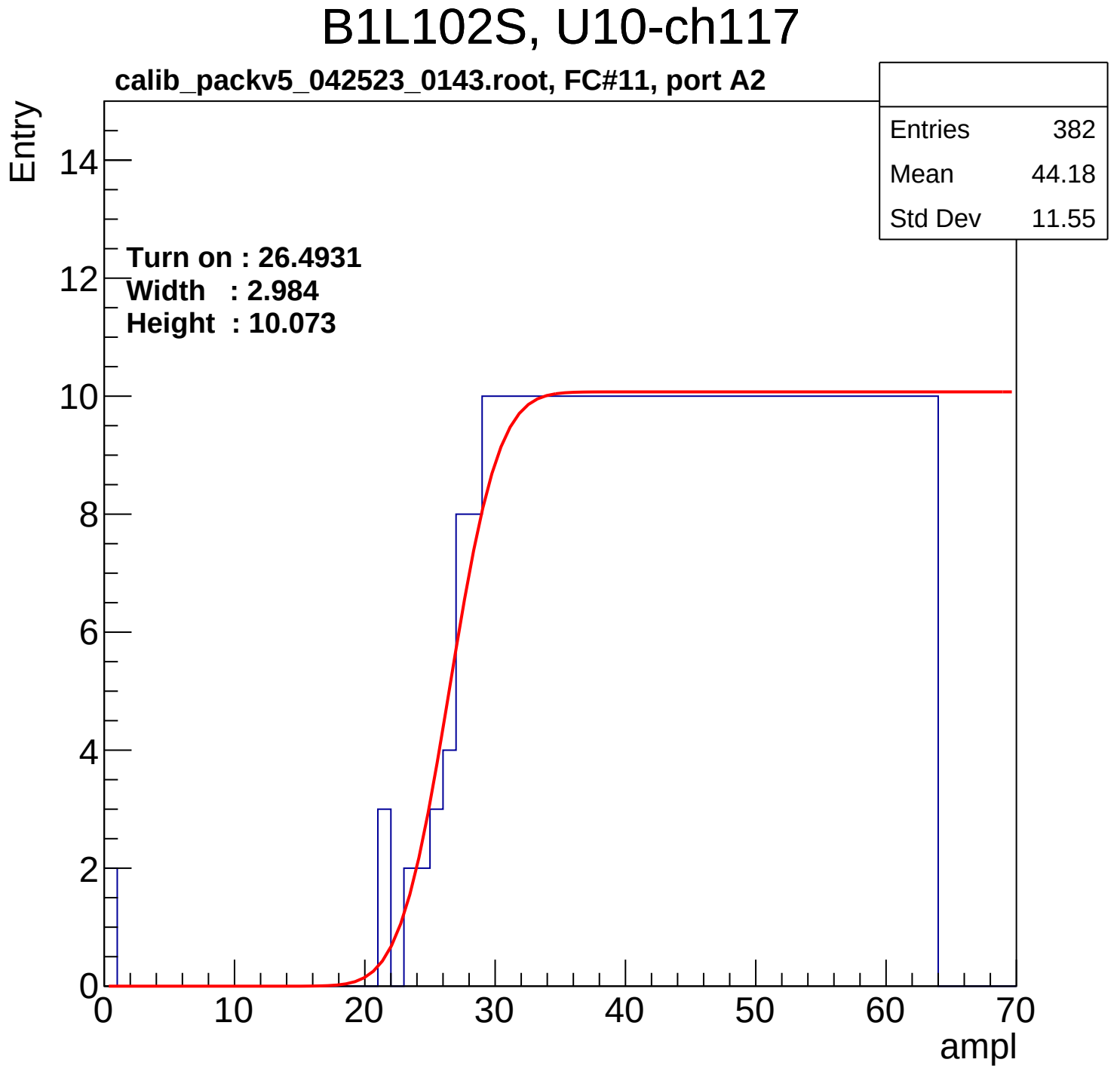
B1L102S, U10-ch117
calib_packv5_042523_0143.root, FC#11, port A2
Entries 382
Mean 44.18
Std Dev 11.55
Turn on : 26.4931
Width : 2.984
Height : 10.073
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
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60
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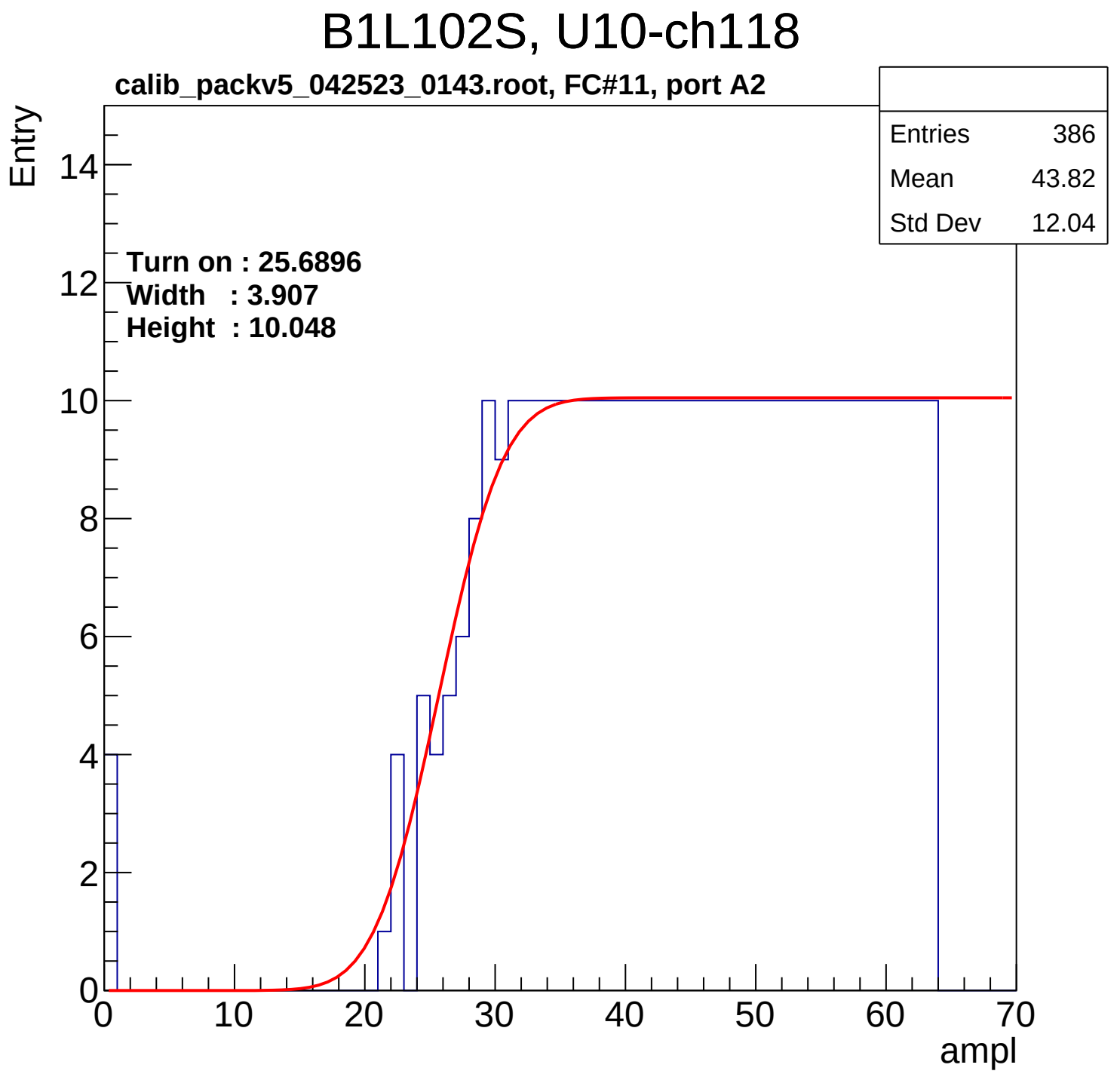
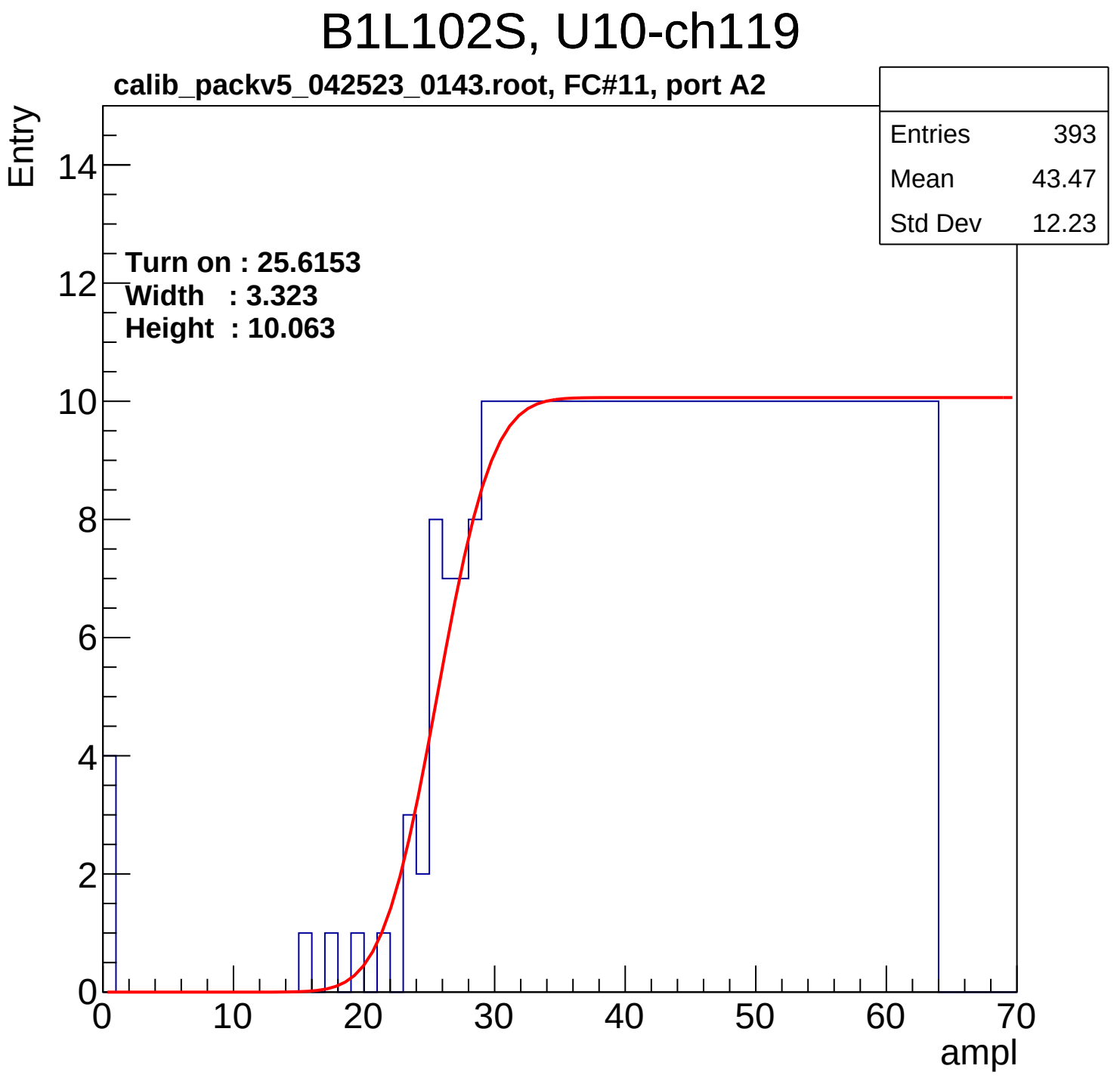
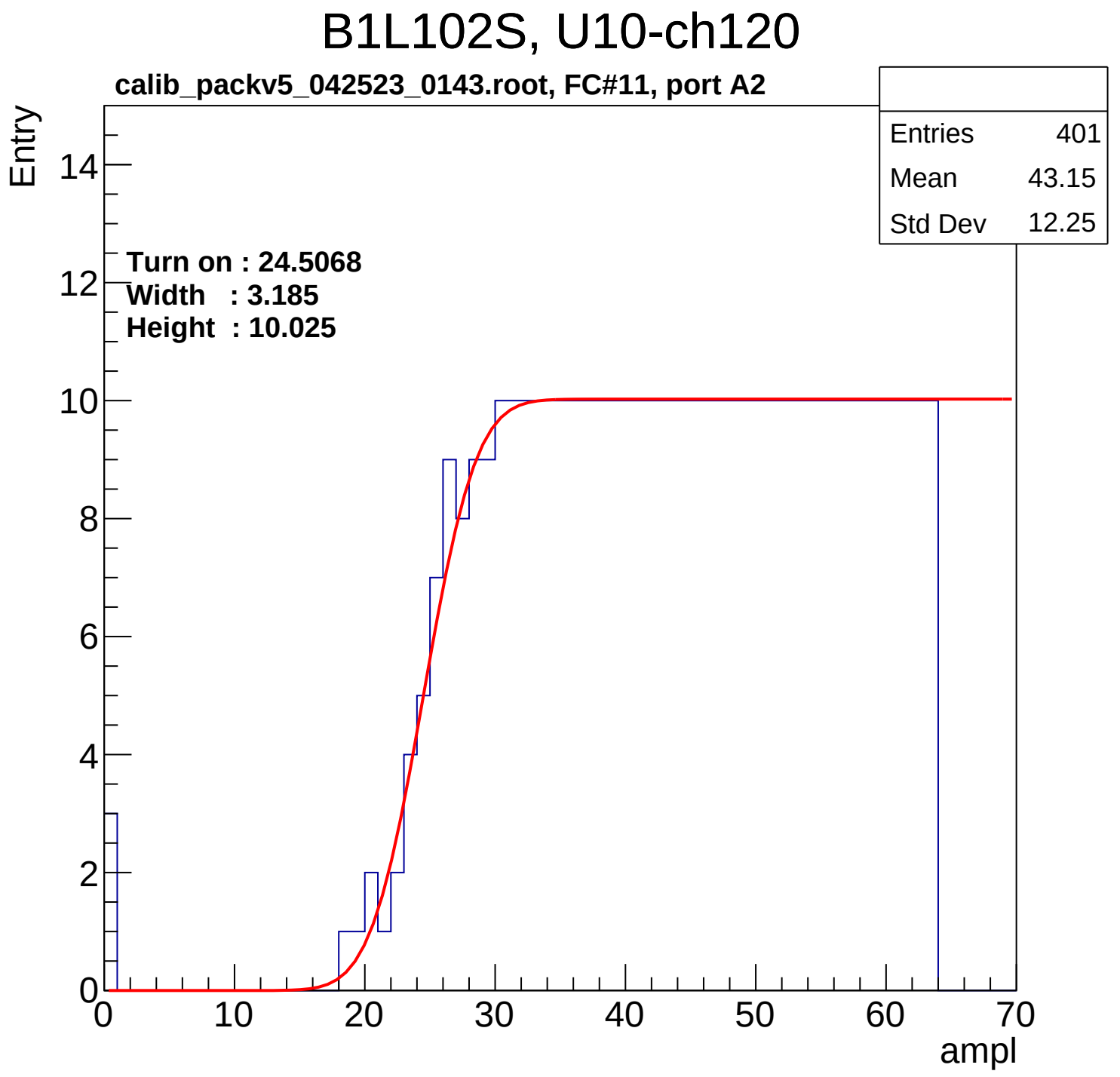
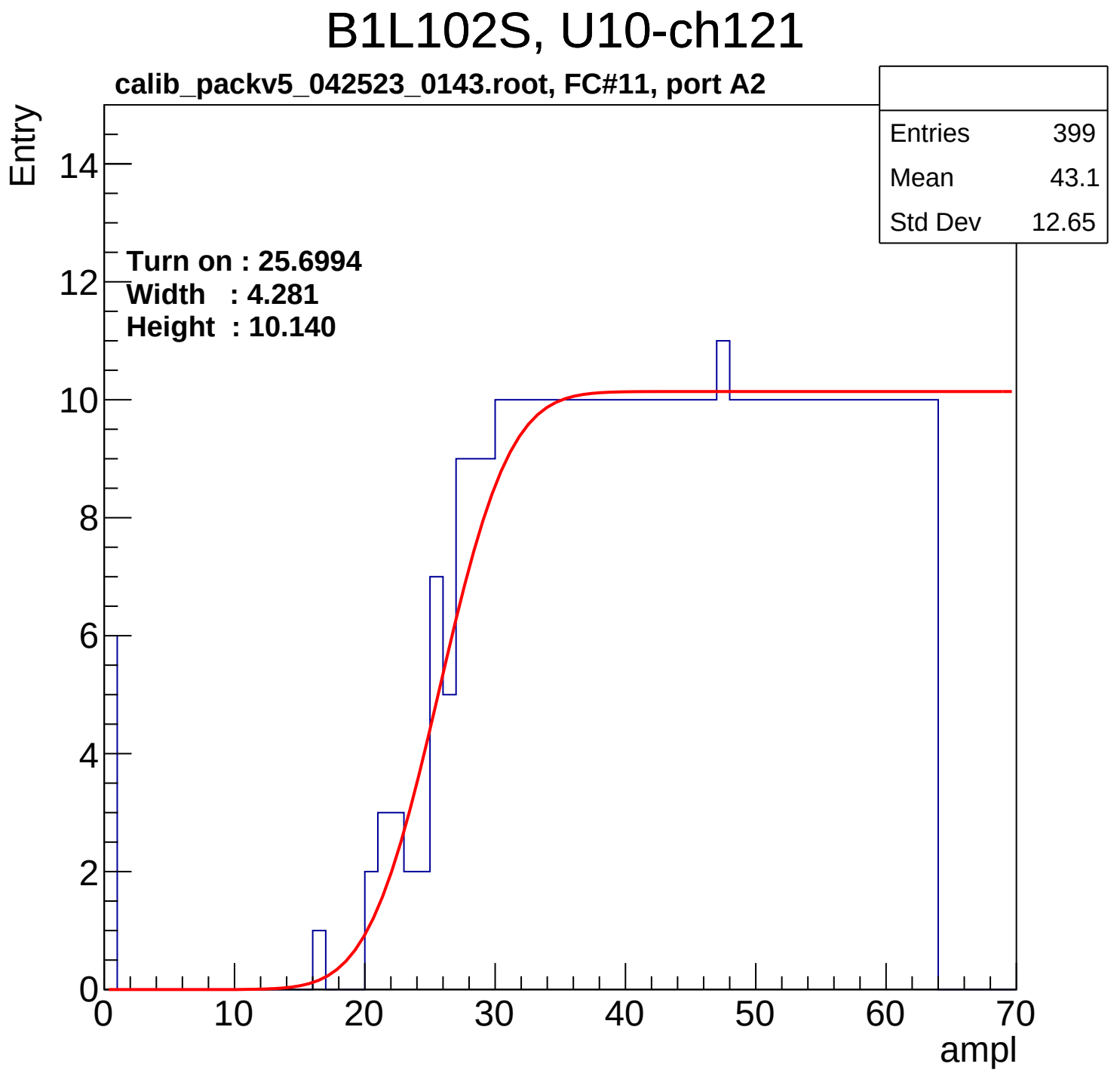
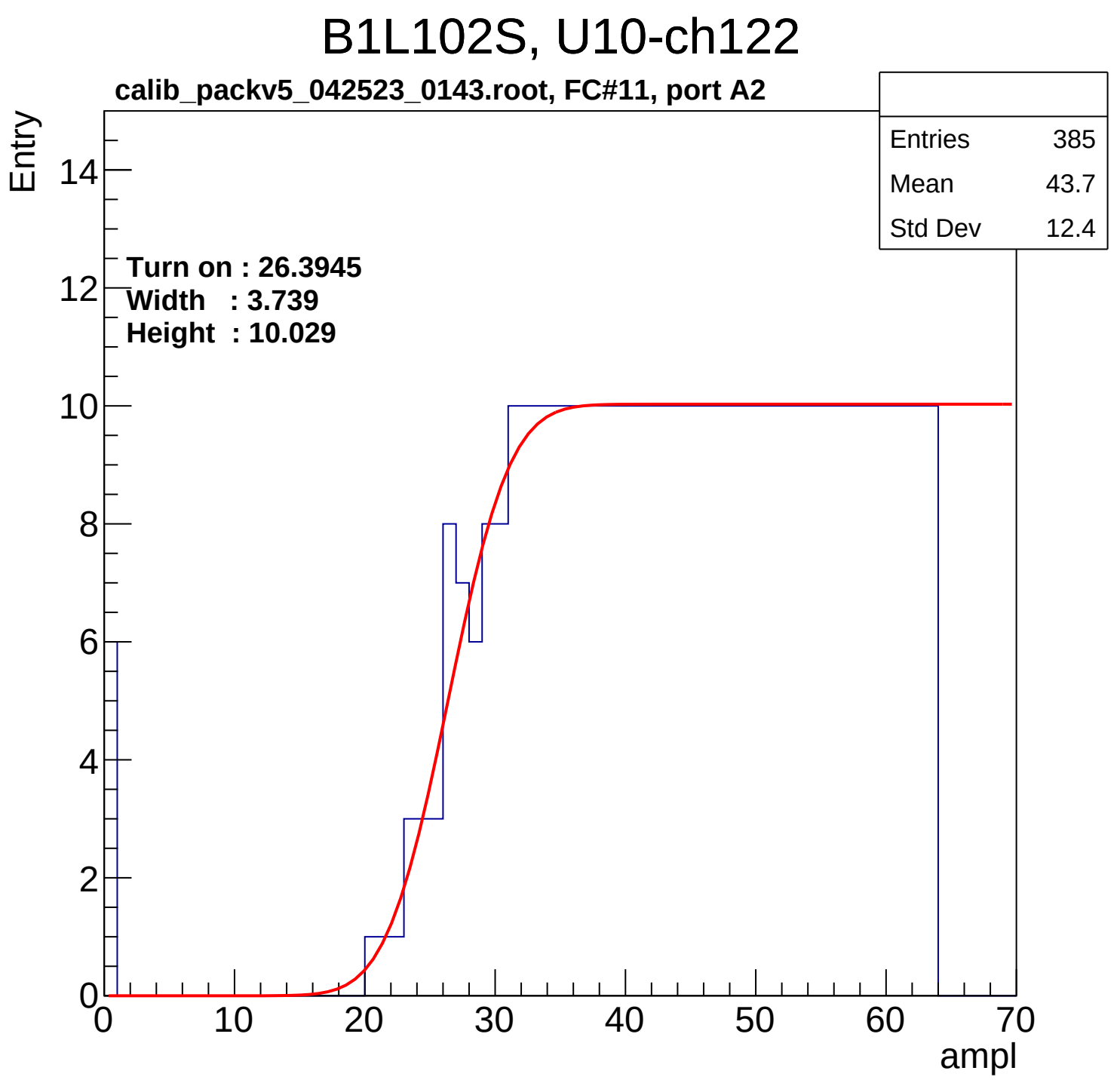

B1L102S, U10-ch118
calib_packv5_042523_0143.root, FC#11, port A2
Entries 386
Mean 43.82
Std Dev 12.04
Turn on : 25.6896
Width : 3.907
Height : 10.048
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L102S, U10-ch119
calib_packv5_042523_0143.root, FC#11, port A2
Entries 393
Mean 43.47
Std Dev 12.23
Turn on : 25.6153
Width : 3.323
Height : 10.063
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L102S, U10-ch120
calib_packv5_042523_0143.root, FC#11, port A2
Entries 401
Mean 43.15
Std Dev 12.25
Turn on : 24.5068
Width : 3.185
Height : 10.025
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L102S, U10-ch121
calib_packv5_042523_0143.root, FC#11, port A2
Entries 399
Mean 43.1
Std Dev 12.65
Turn on : 25.6994
Width : 4.281
Height : 10.140
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L102S, U10-ch122
calib_packv5_042523_0143.root, FC#11, port A2
Entries 385
Mean 43.7
Std Dev 12.4
Turn on : 26.3945
Width : 3.739
Height : 10.029
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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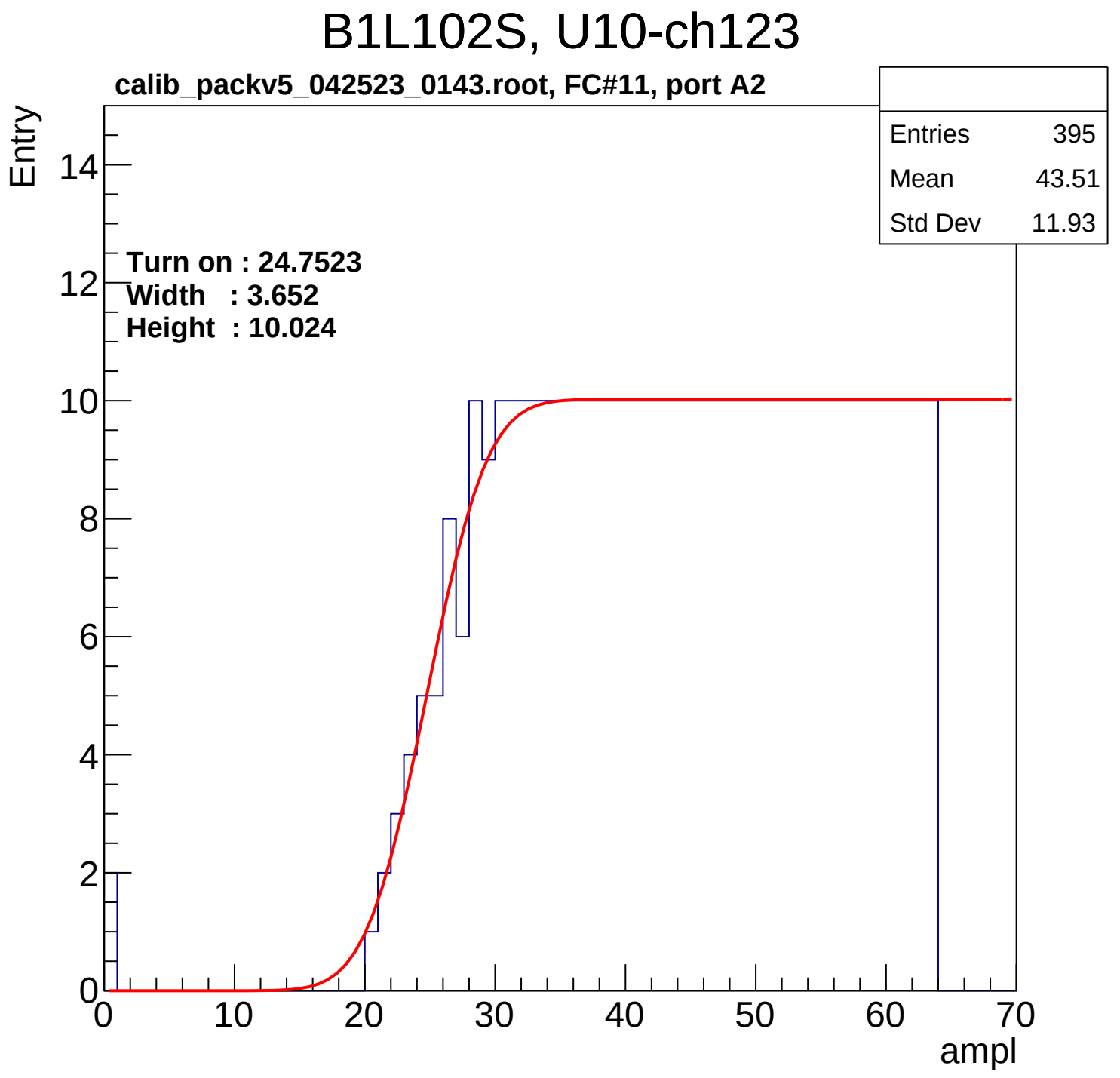
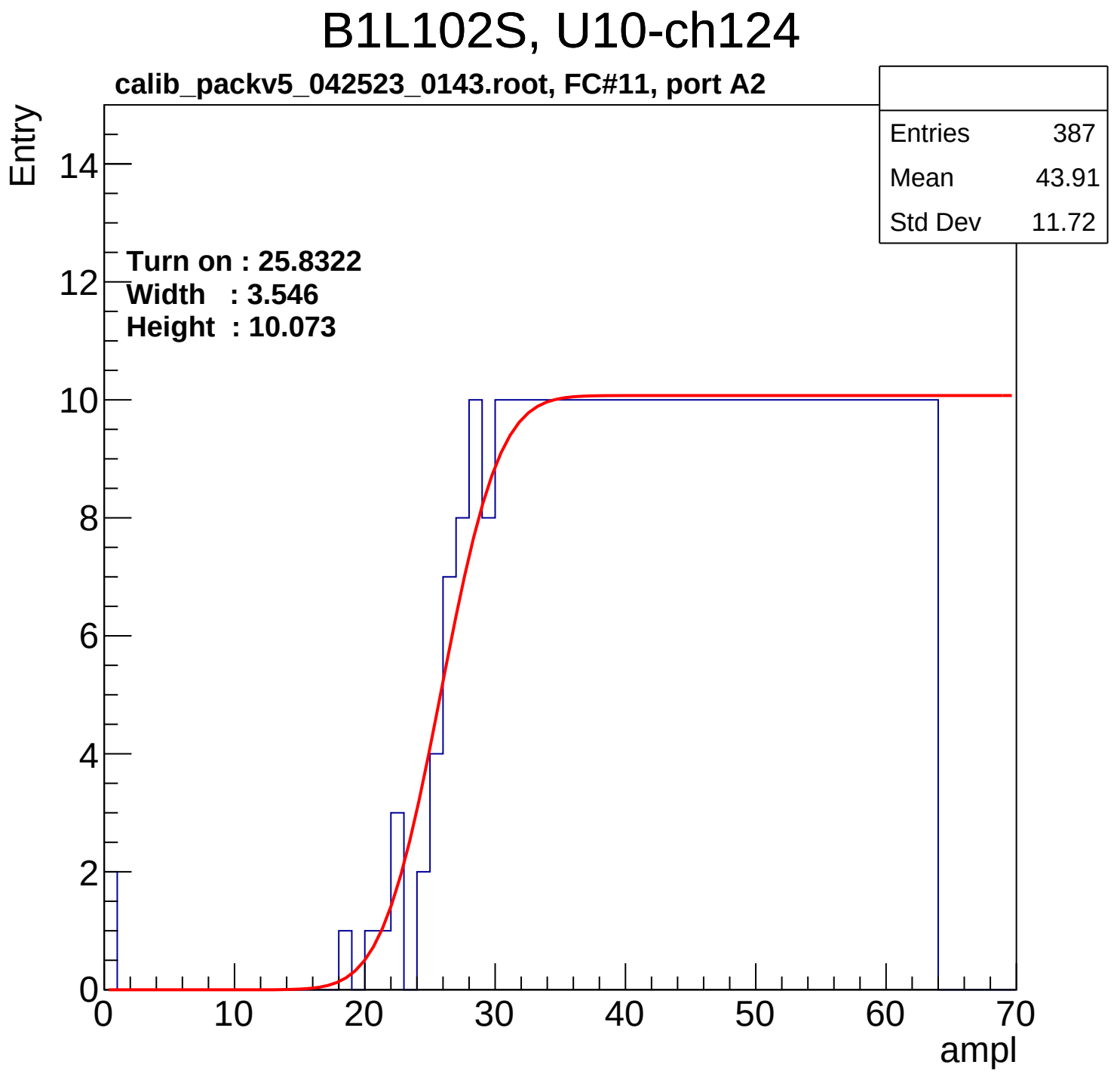

B1L102S, U10-ch123
calib_packv5_042523_0143.root, FC#11, port A2
Entries 395
Mean 43.51
Std Dev 11.93
Turn on : 24.7523
Width : 3.652
Height : 10.024
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L102S, U10-ch124
calib_packv5_042523_0143.root, FC#11, port A2
Entries 387
Mean 43.91
Std Dev 11.72
Turn on : 25.8322
Width : 3.546
Height : 10.073
Entry
ampl
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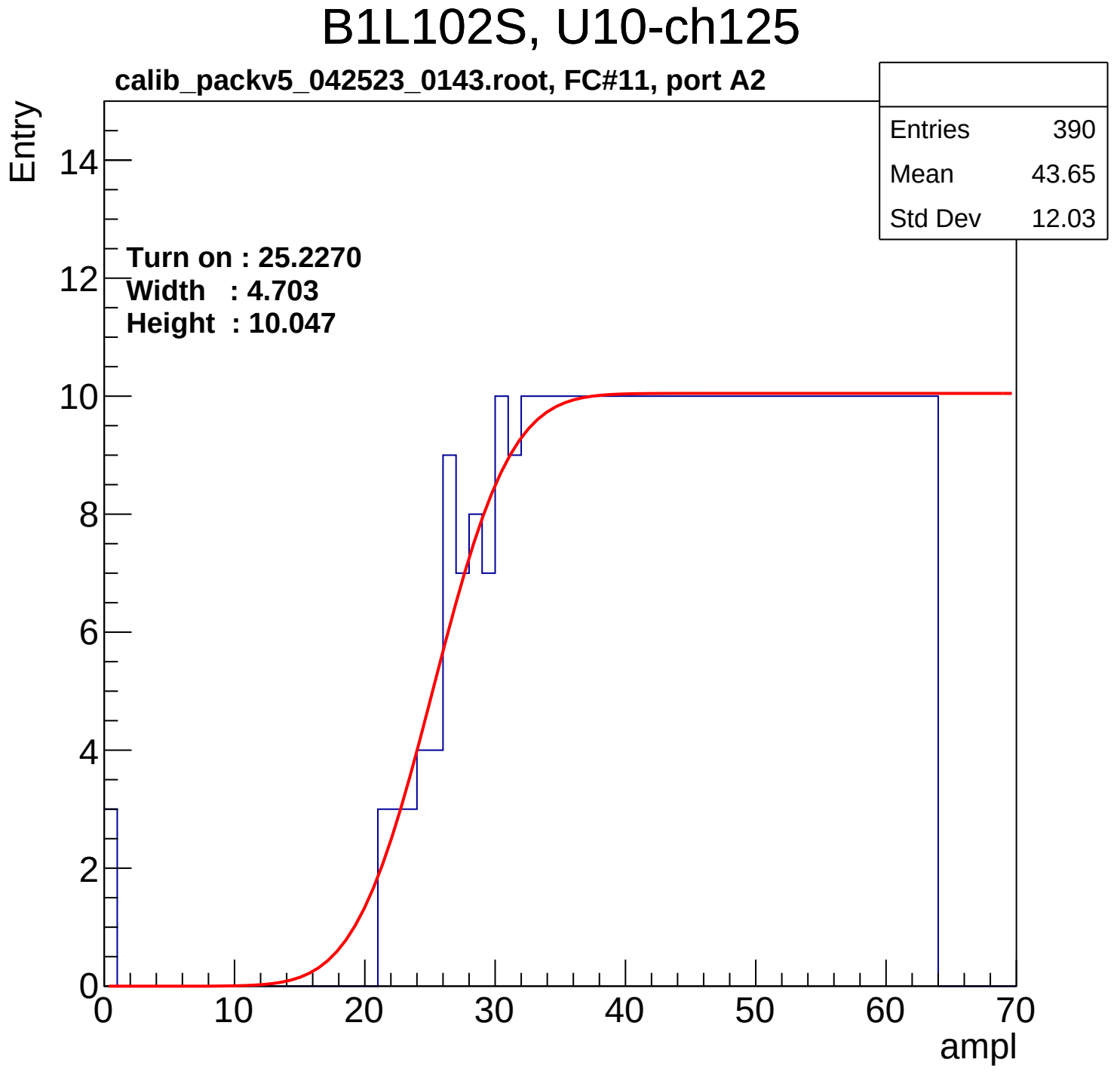
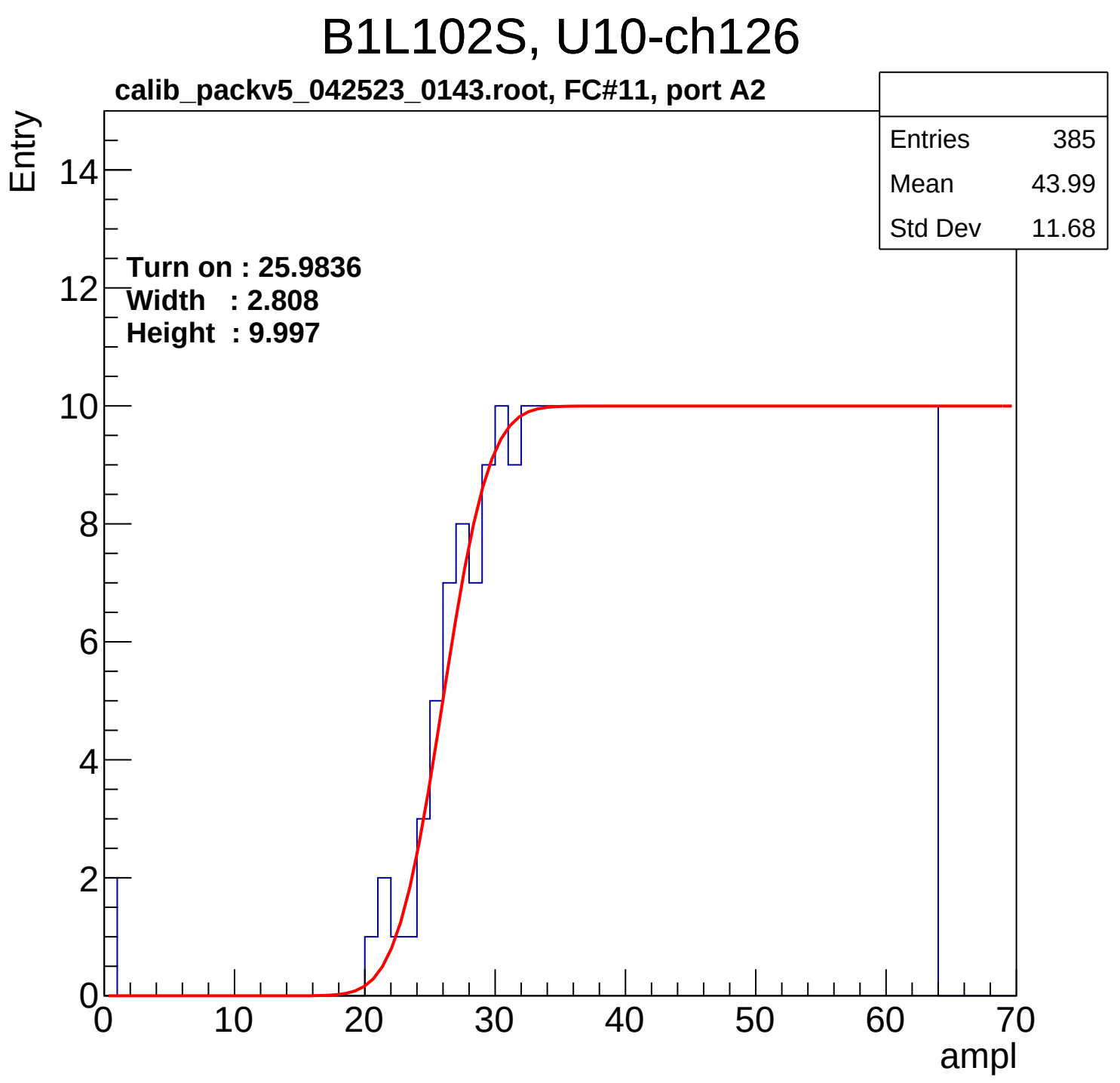
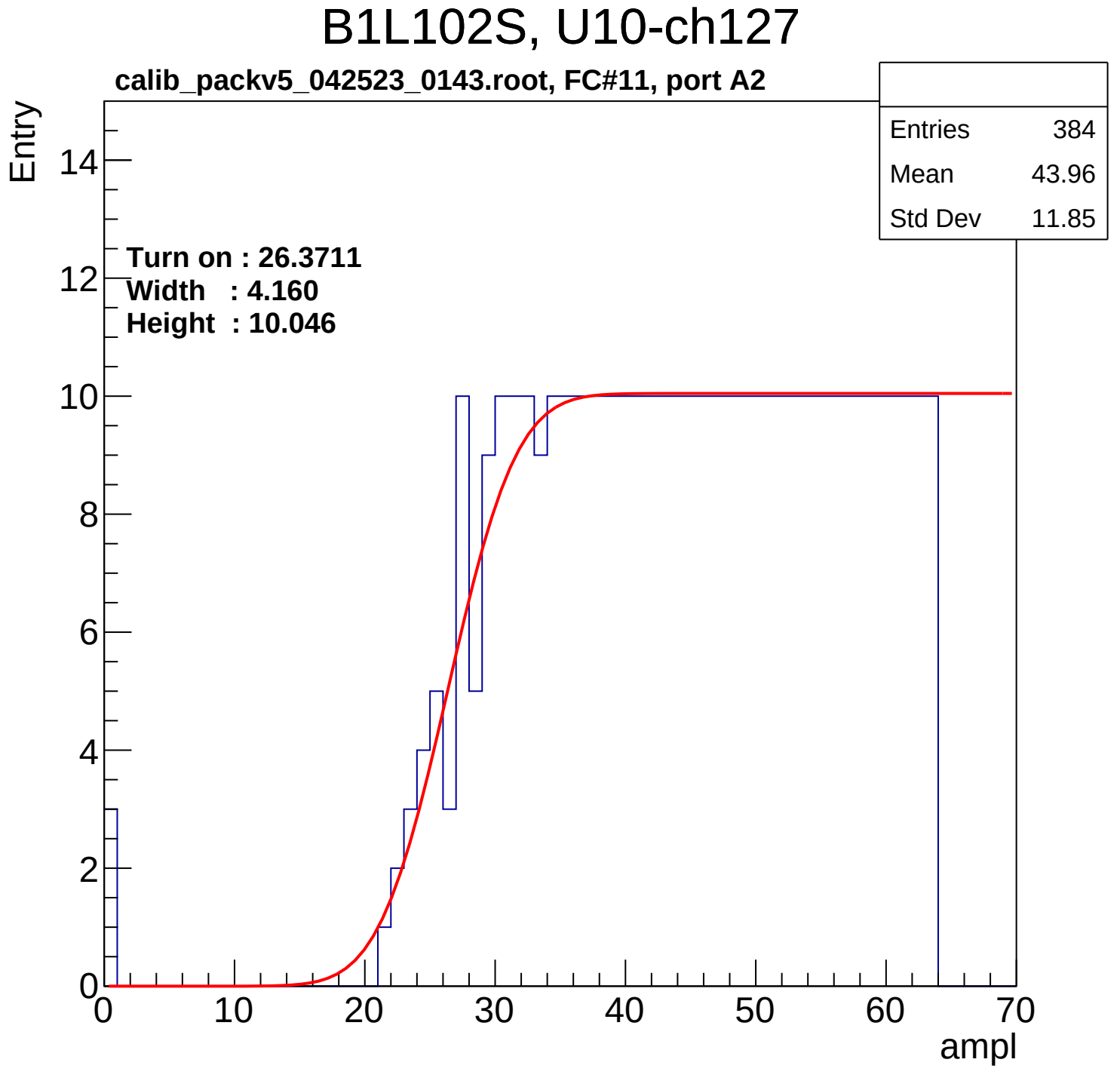
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L102S, U10-ch125
calib_packv5_042523_0143.root, FC#11, port A2
Entries 390
Mean 43.65
Std Dev 12.03
Turn on : 25.2270
Width : 4.703
Height : 10.047
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L102S, U10-ch126
calib_packv5_042523_0143.root, FC#11, port A2
Entries 385
Mean 43.99
Std Dev 11.68
Turn on : 25.9836
Width : 2.808
Height : 9.997
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L102S, U10-ch127
calib_packv5_042523_0143.root, FC#11, port A2
Entries 384
Mean 43.96
Std Dev 11.85
Turn on : 26.3711
Width : 4.160
Height : 10.046
Entry
ampl
0
2
4
6
8
10
12
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0
10
20
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40
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60
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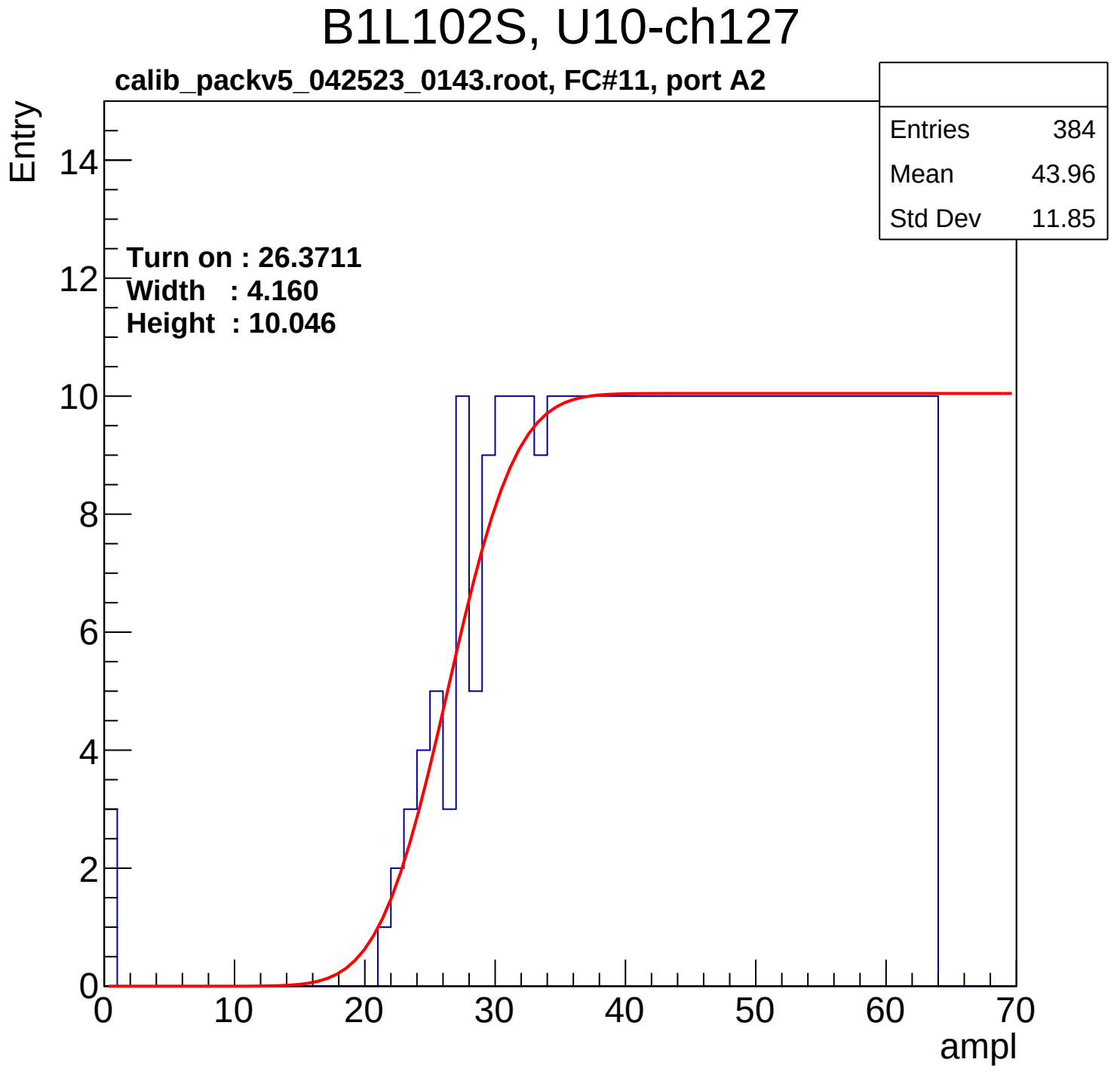
B1L102S, U10-ch127
calib_packv5_042523_0143.root, FC#11, port A2
Entries 384
Mean 43.96
Std Dev 11.85
Turn on : 26.3711
Width : 4.160
Height : 10.046
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70