



# B1L102S, U12-ch0, adc0

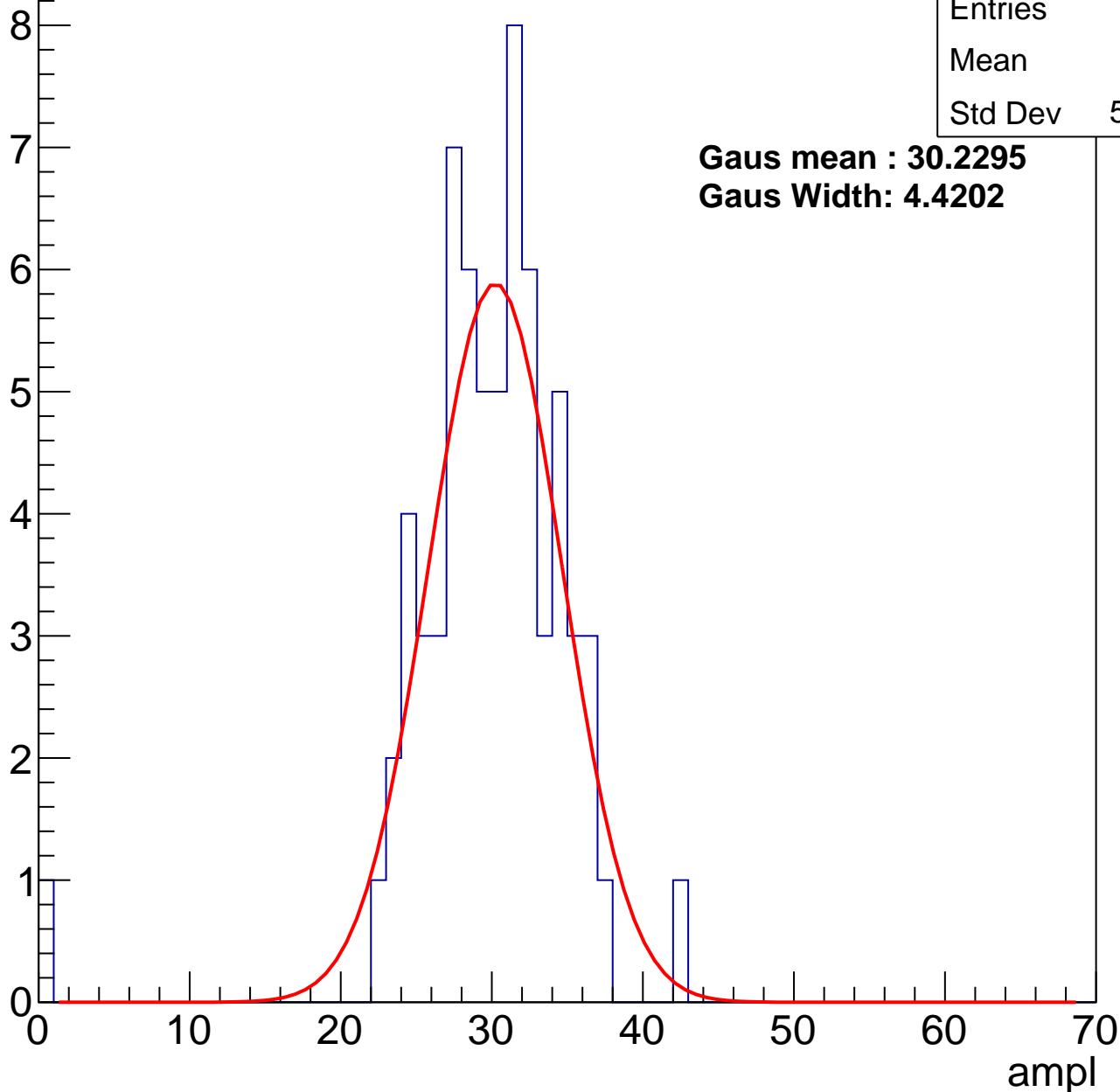
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	67
Mean	29.4
Std Dev	5.342

**Gaus mean : 30.2295**

**Gaus Width: 4.4202**



# B1L102S, U12-ch0, adc1

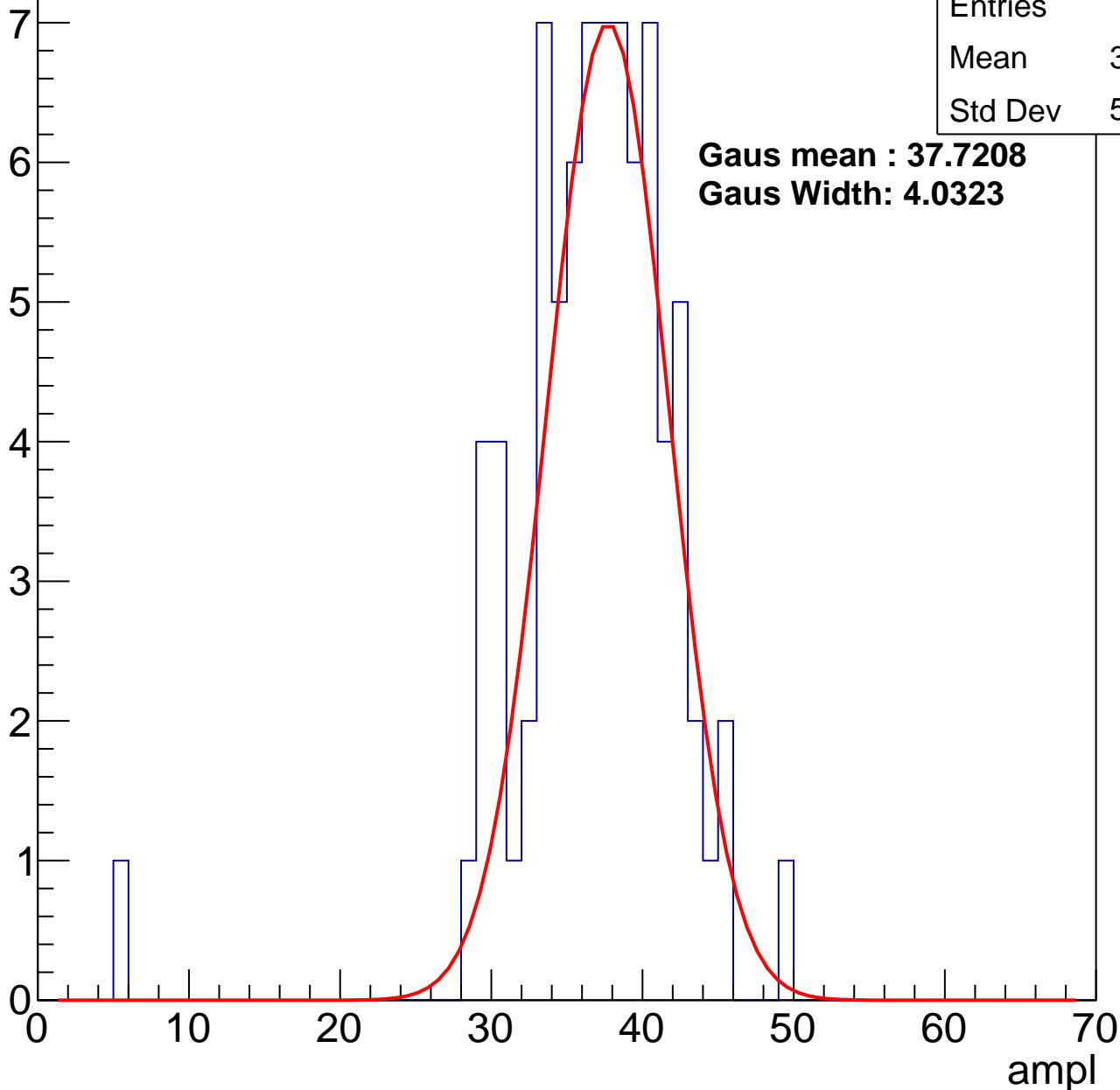
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	80
Mean	36.36
Std Dev	5.562

**Gaus mean : 37.7208**

**Gaus Width: 4.0323**



# B1L102S, U12-ch0, adc2

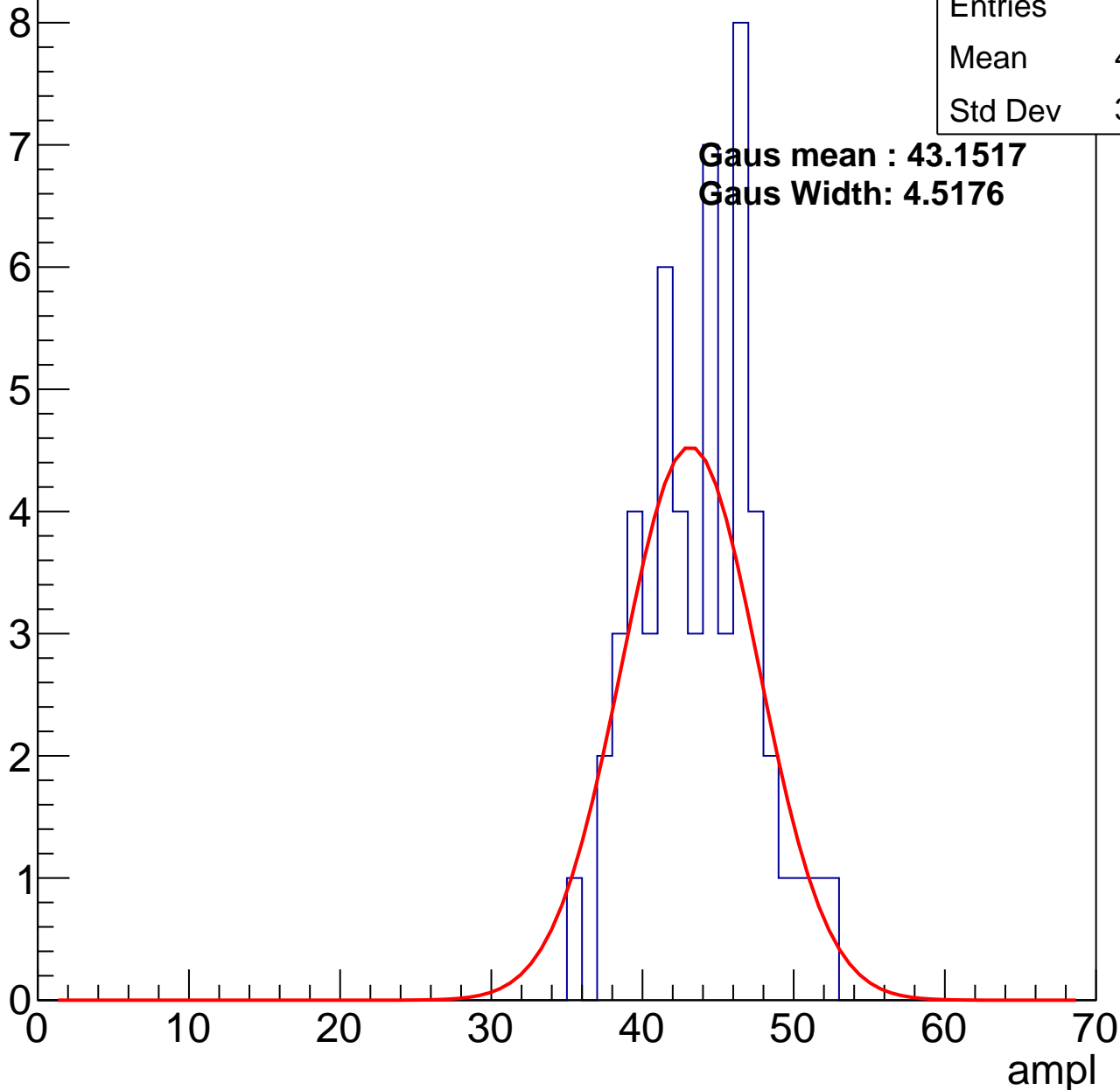
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	54
Mean	43.31
Std Dev	3.751

**Gaus mean : 43.1517**

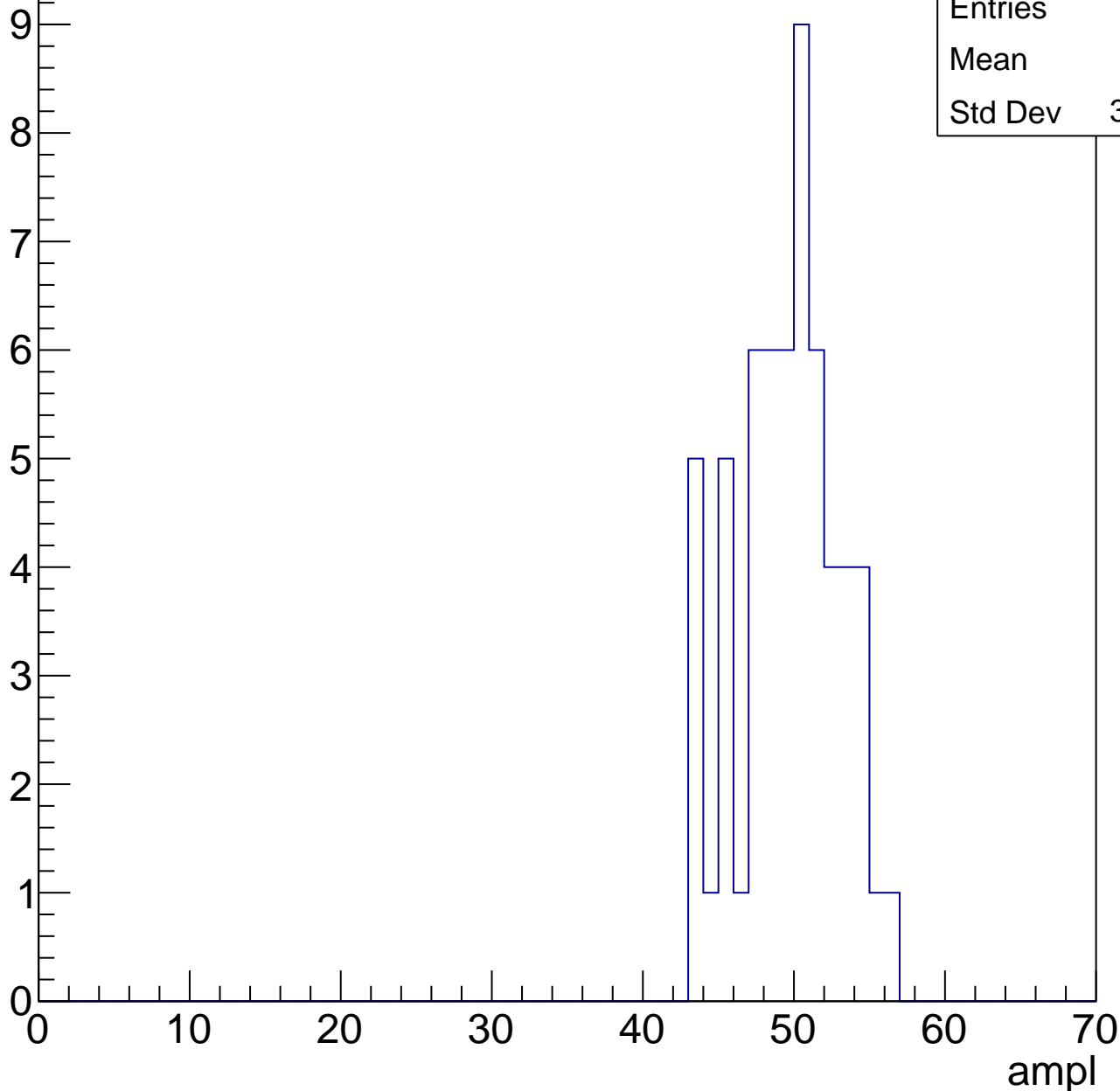
**Gaus Width: 4.5176**



# B1L102S, U12-ch0, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

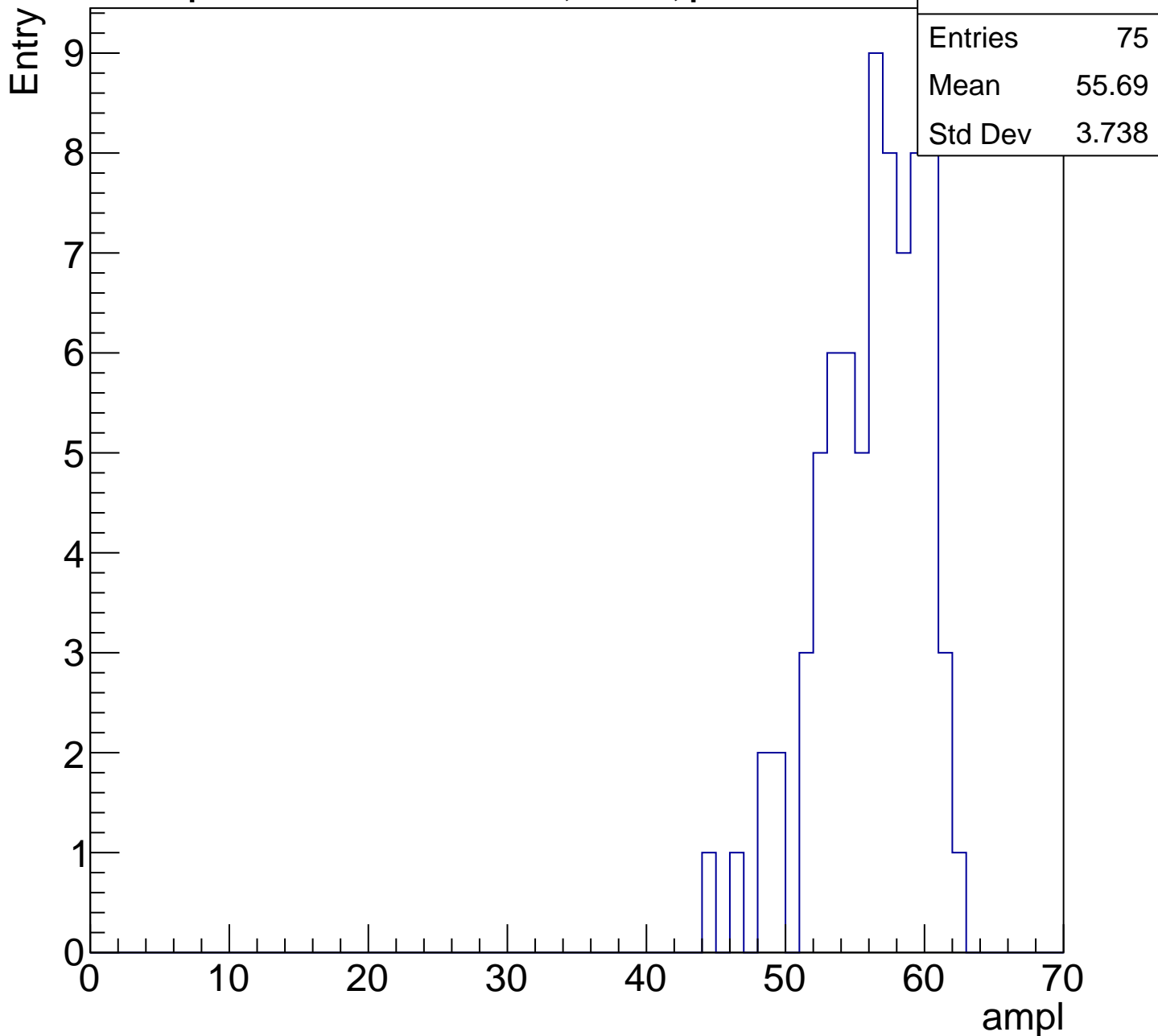
Entry



Entries	59
Mean	49.1
Std Dev	3.297

# B1L102S, U12-ch0, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

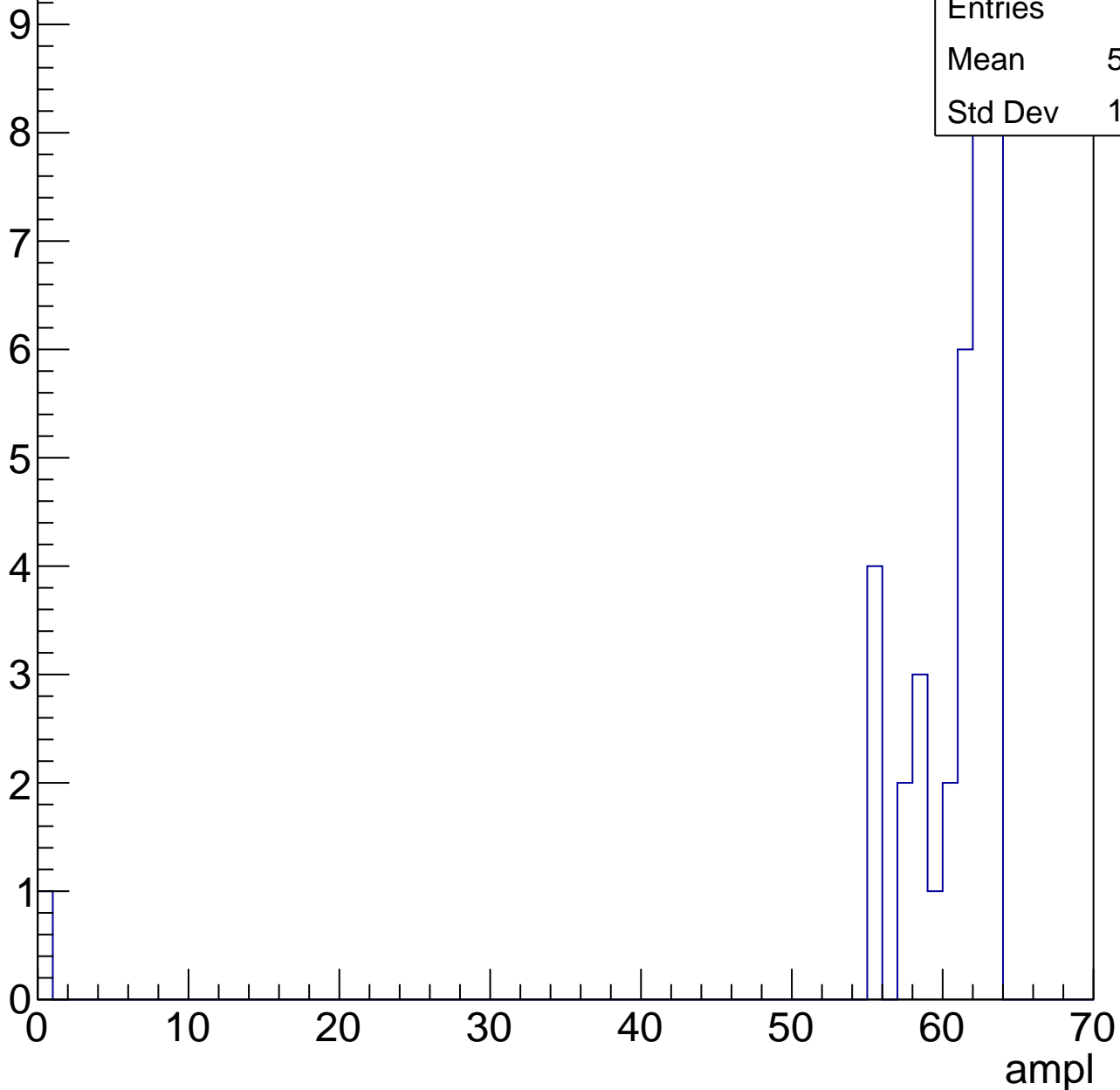


# B1L102S, U12-ch0, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

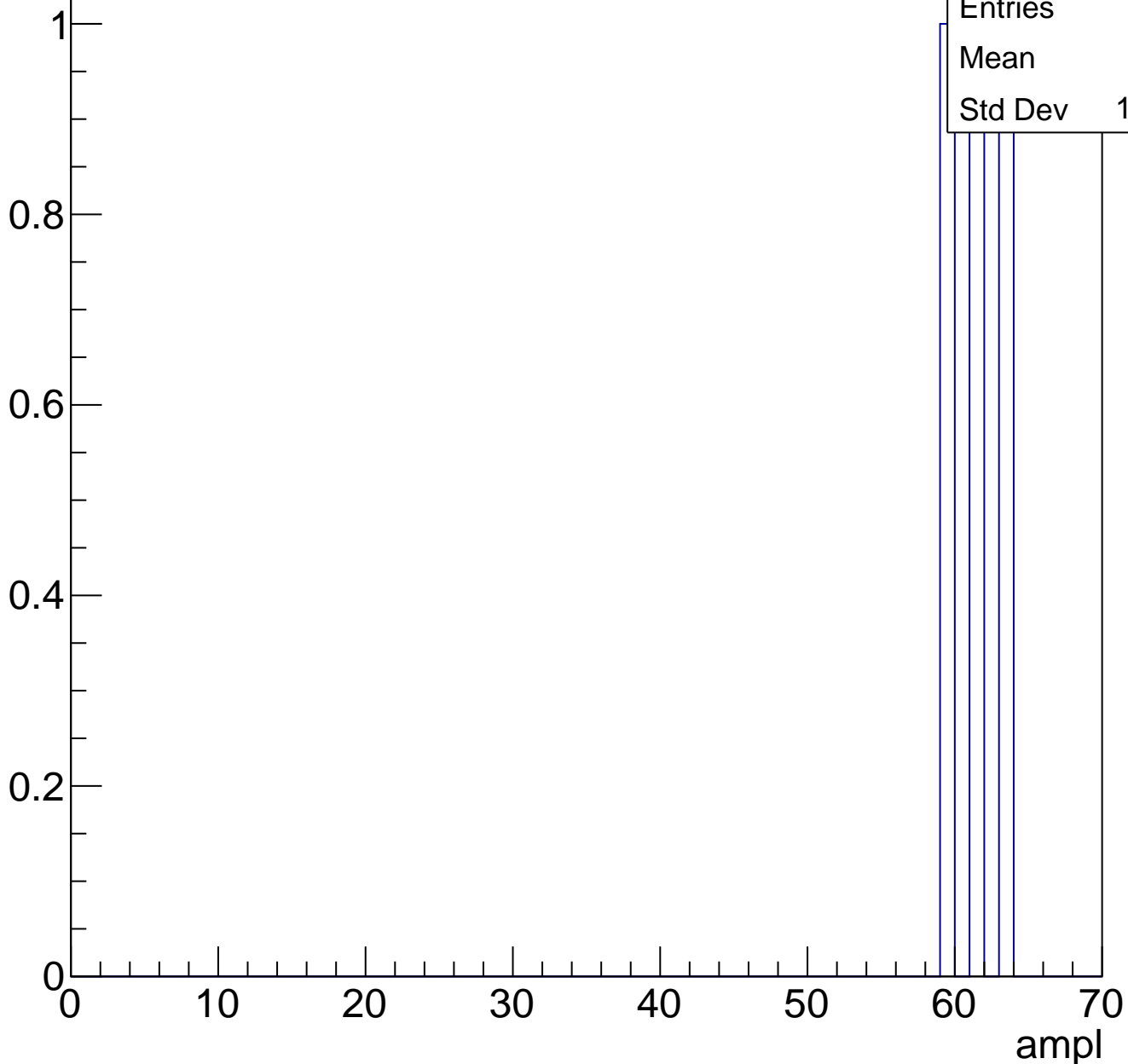
Entries	37
Mean	58.86
Std Dev	10.14



# B1L102S, U12-ch0, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

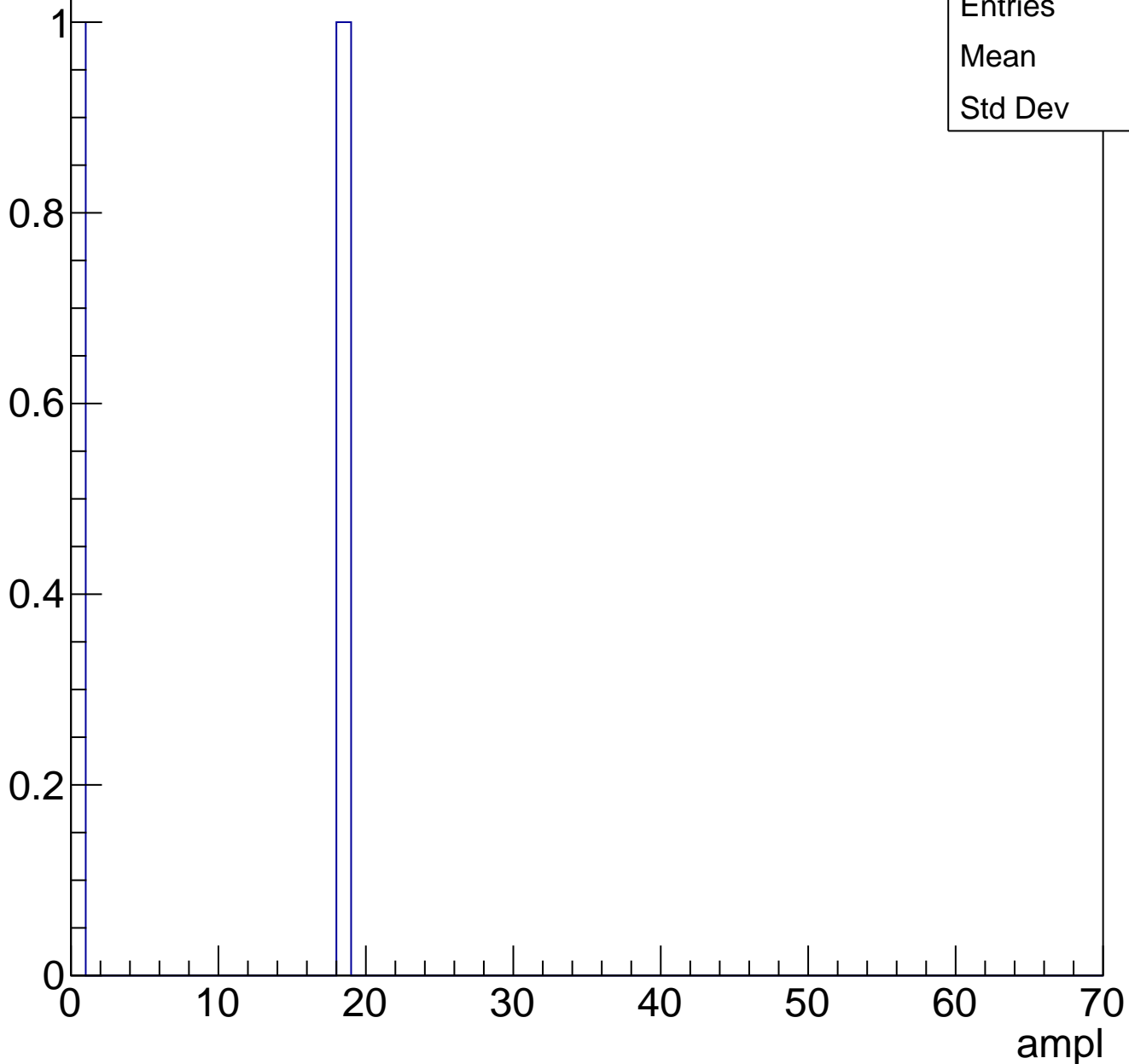




# B1L102S, U12-ch0, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U12-ch1, adc0

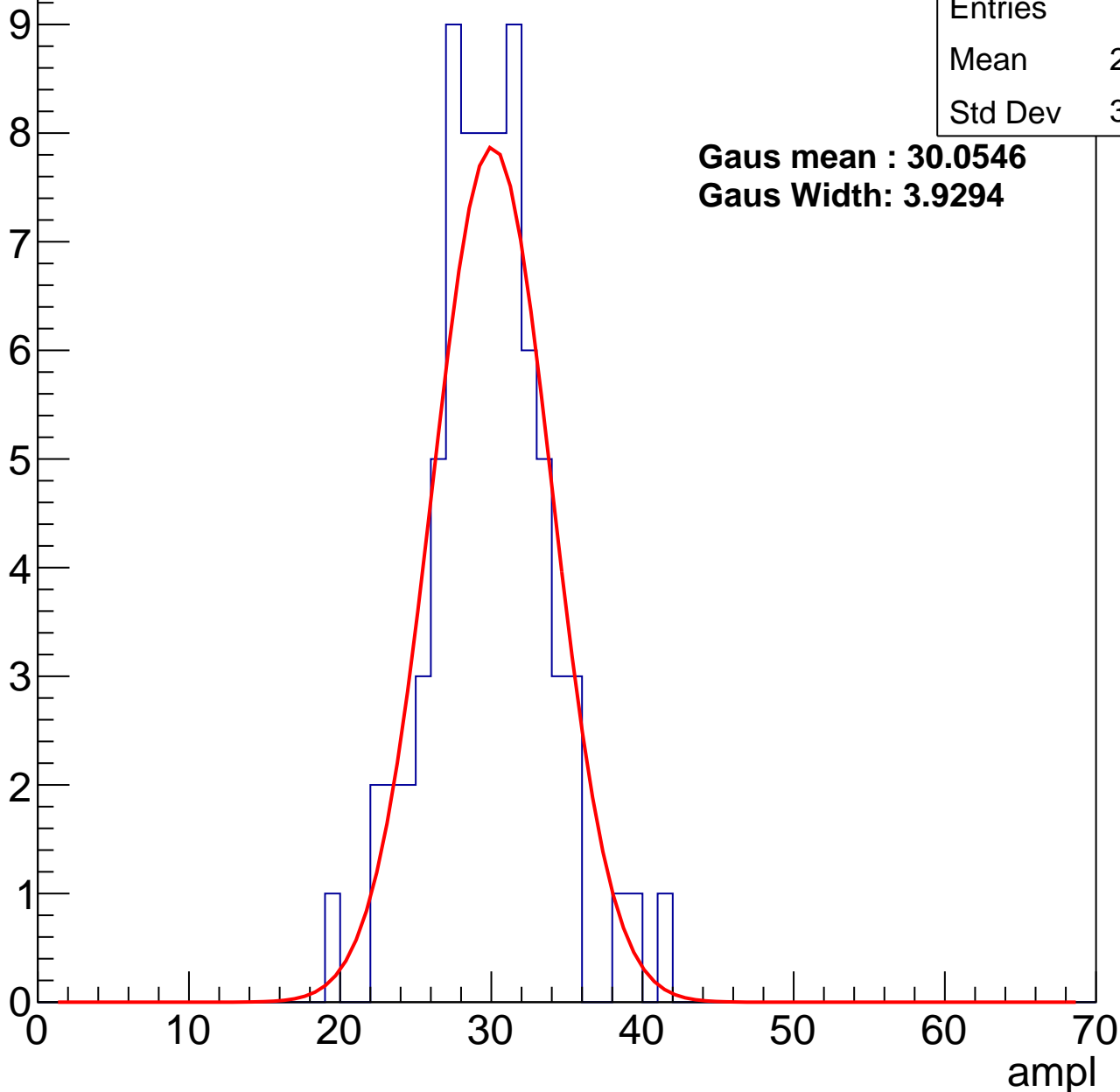
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	77
Mean	29.38
Std Dev	3.834

**Gaus mean : 30.0546**

**Gaus Width: 3.9294**



# B1L102S, U12-ch1, adc1

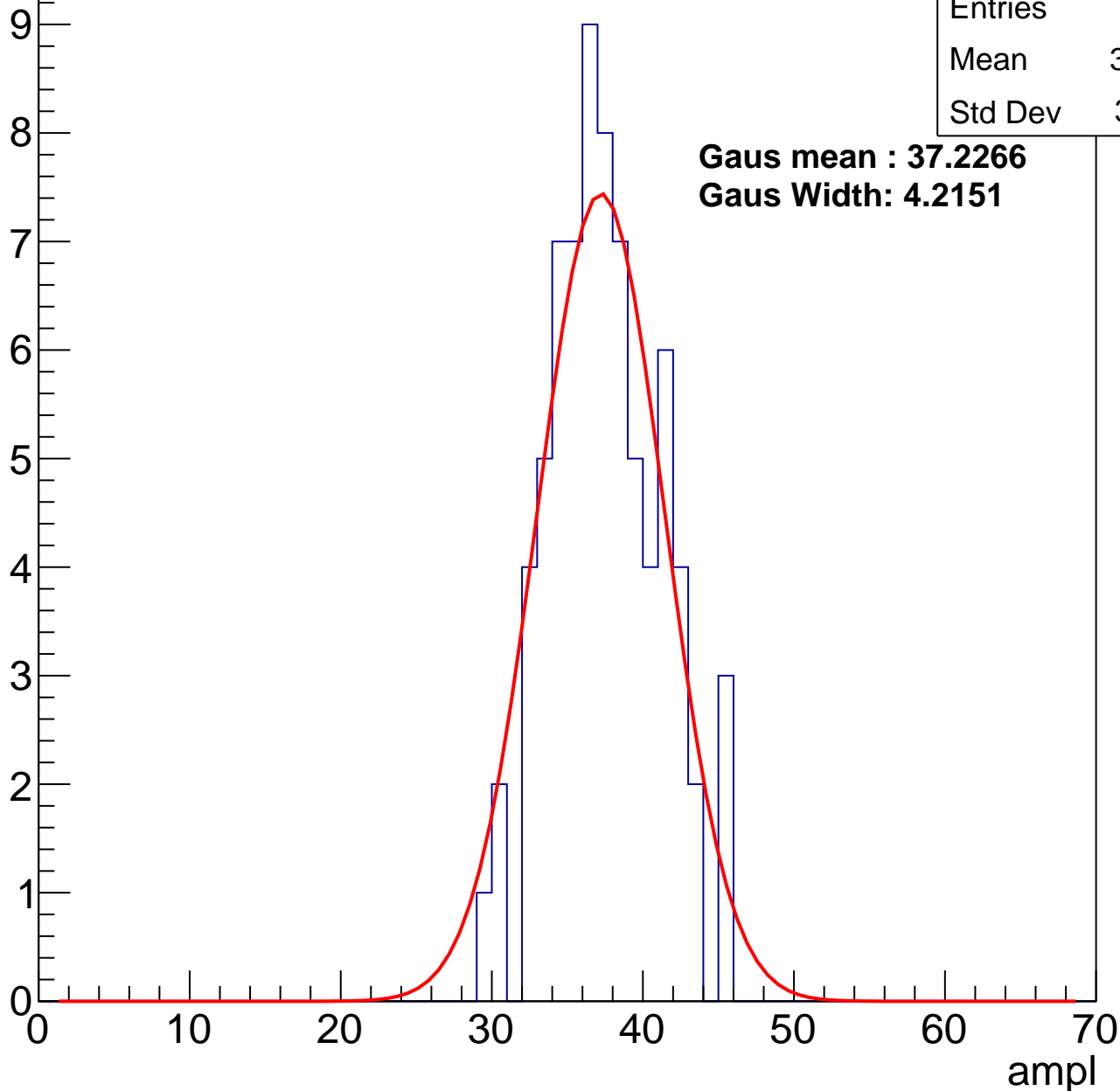
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	74
Mean	37.04
Std Dev	3.611

**Gaus mean : 37.2266**

**Gaus Width: 4.2151**



# B1L102S, U12-ch1, adc2

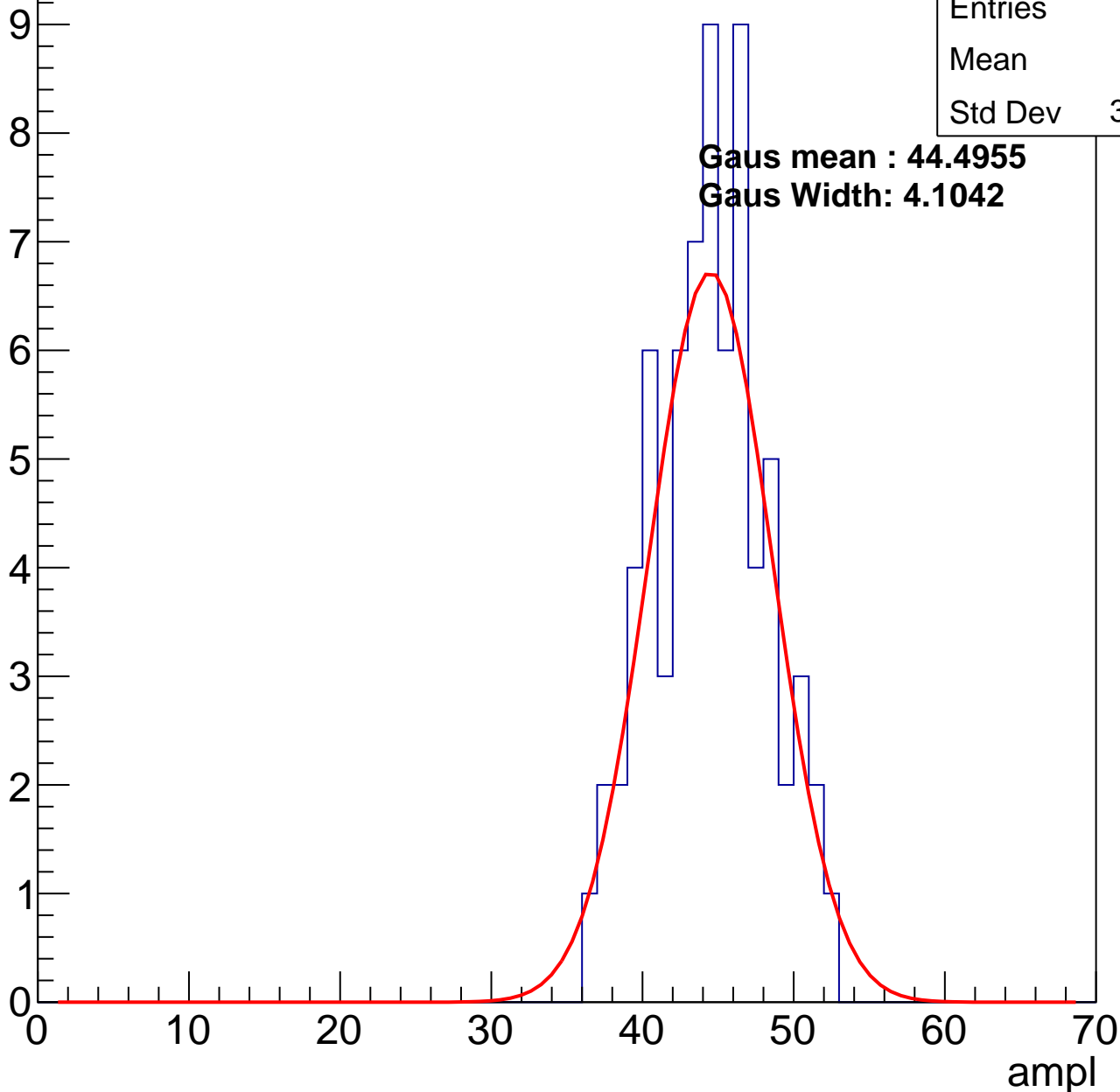
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	72
Mean	44
Std Dev	3.663

**Gaus mean : 44.4955**

**Gaus Width: 4.1042**

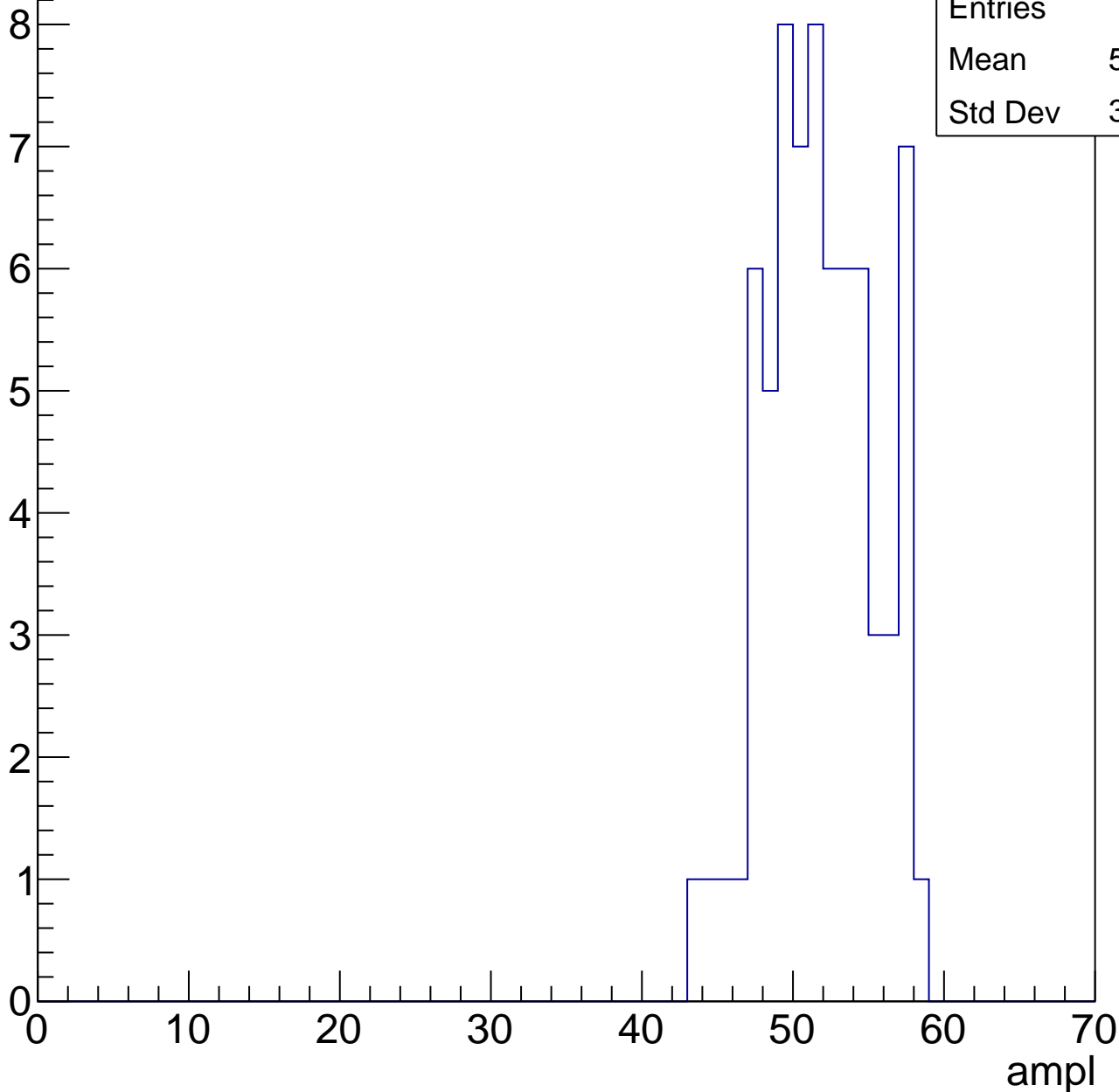


# B1L102S, U12-ch1, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	70
Mean	51.34
Std Dev	3.492

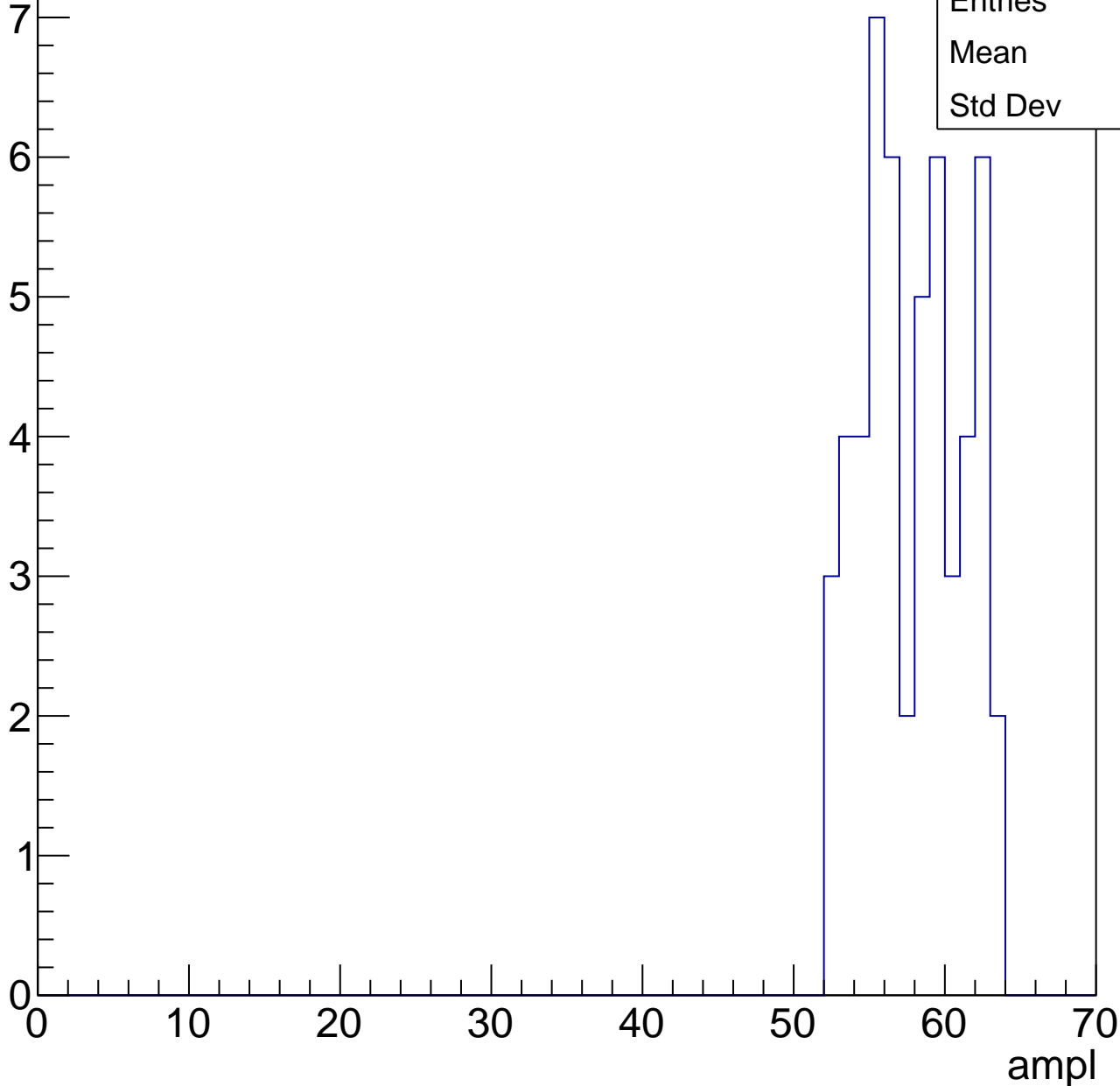


# B1L102S, U12-ch1, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	52
Mean	57.4
Std Dev	3.23

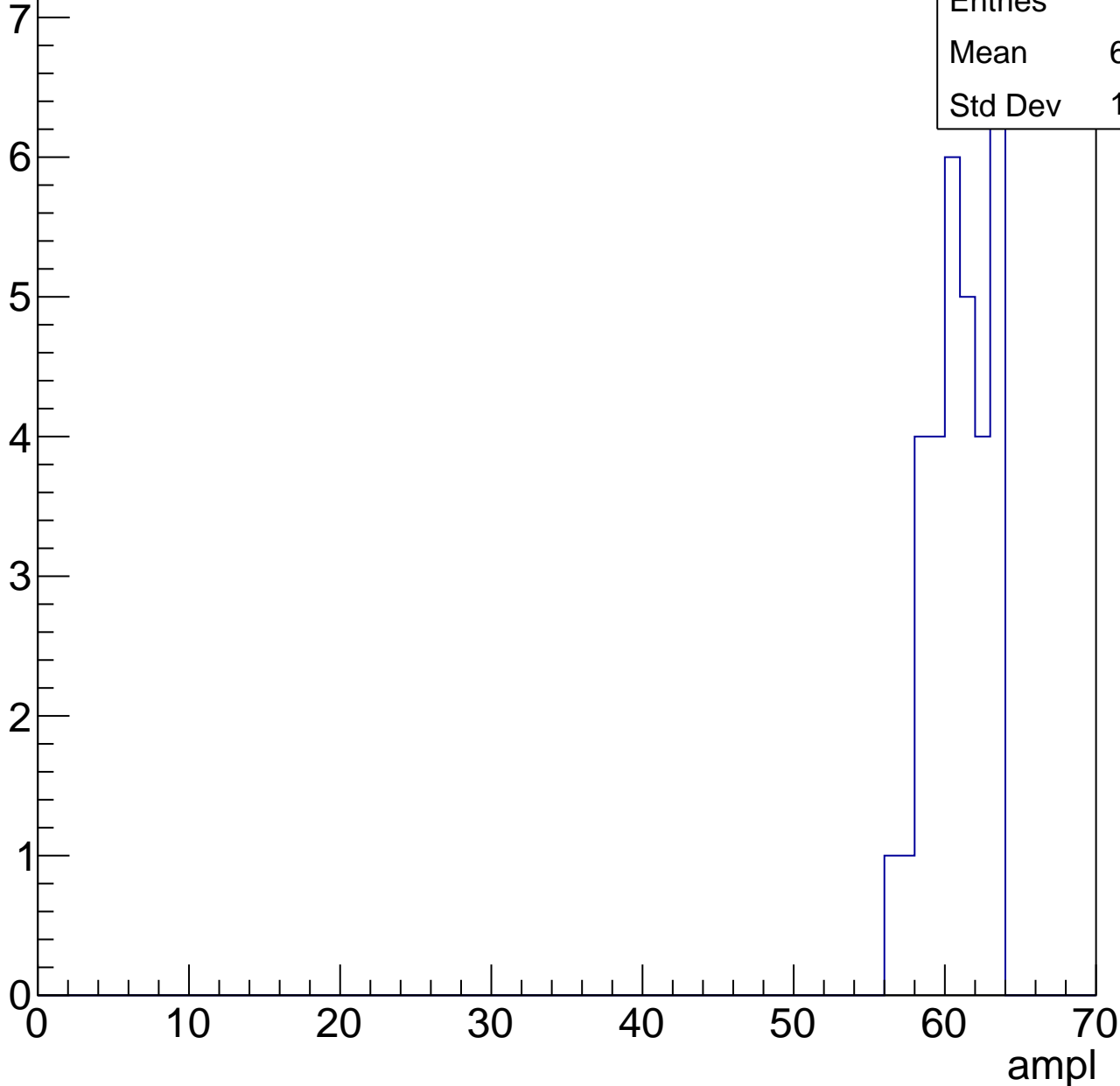


# B1L102S, U12-ch1, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

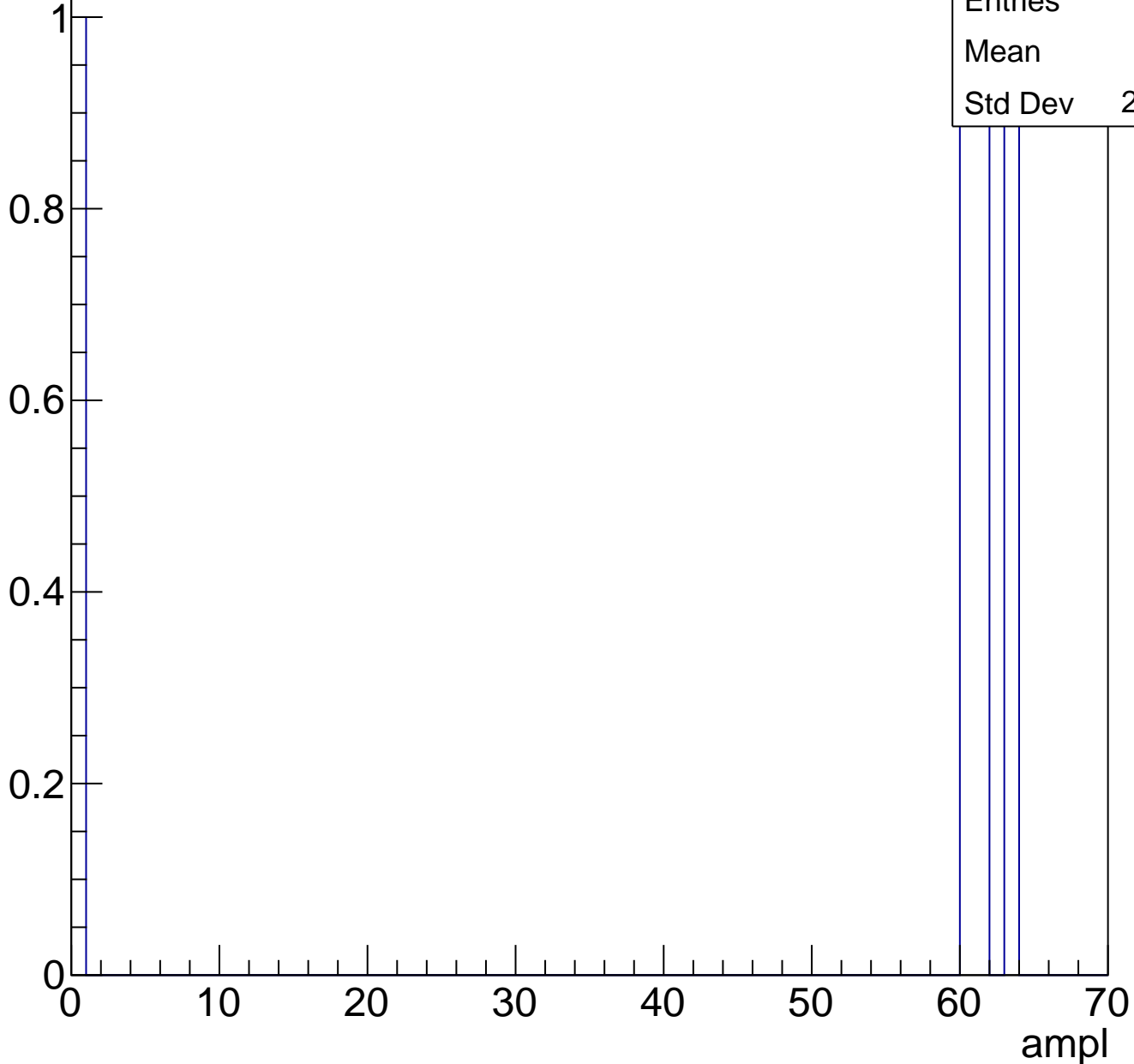
Entries	32
Mean	60.47
Std Dev	1.952



# B1L102S, U12-ch1, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U12-ch1, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U12-ch2, adc0

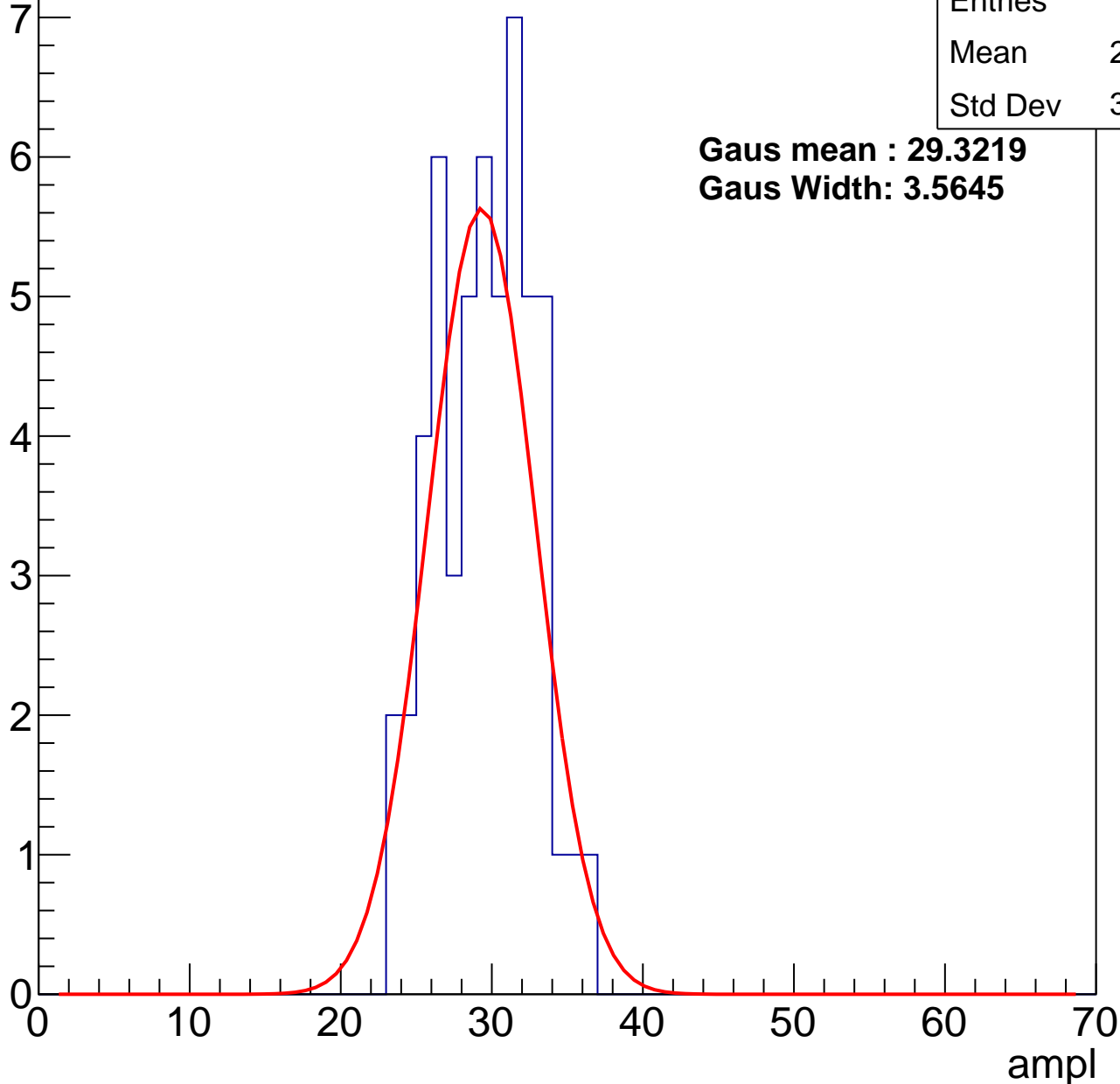
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	53
Mean	29.09
Std Dev	3.146

**Gaus mean : 29.3219**

**Gaus Width: 3.5645**



# B1L102S, U12-ch2, adc1

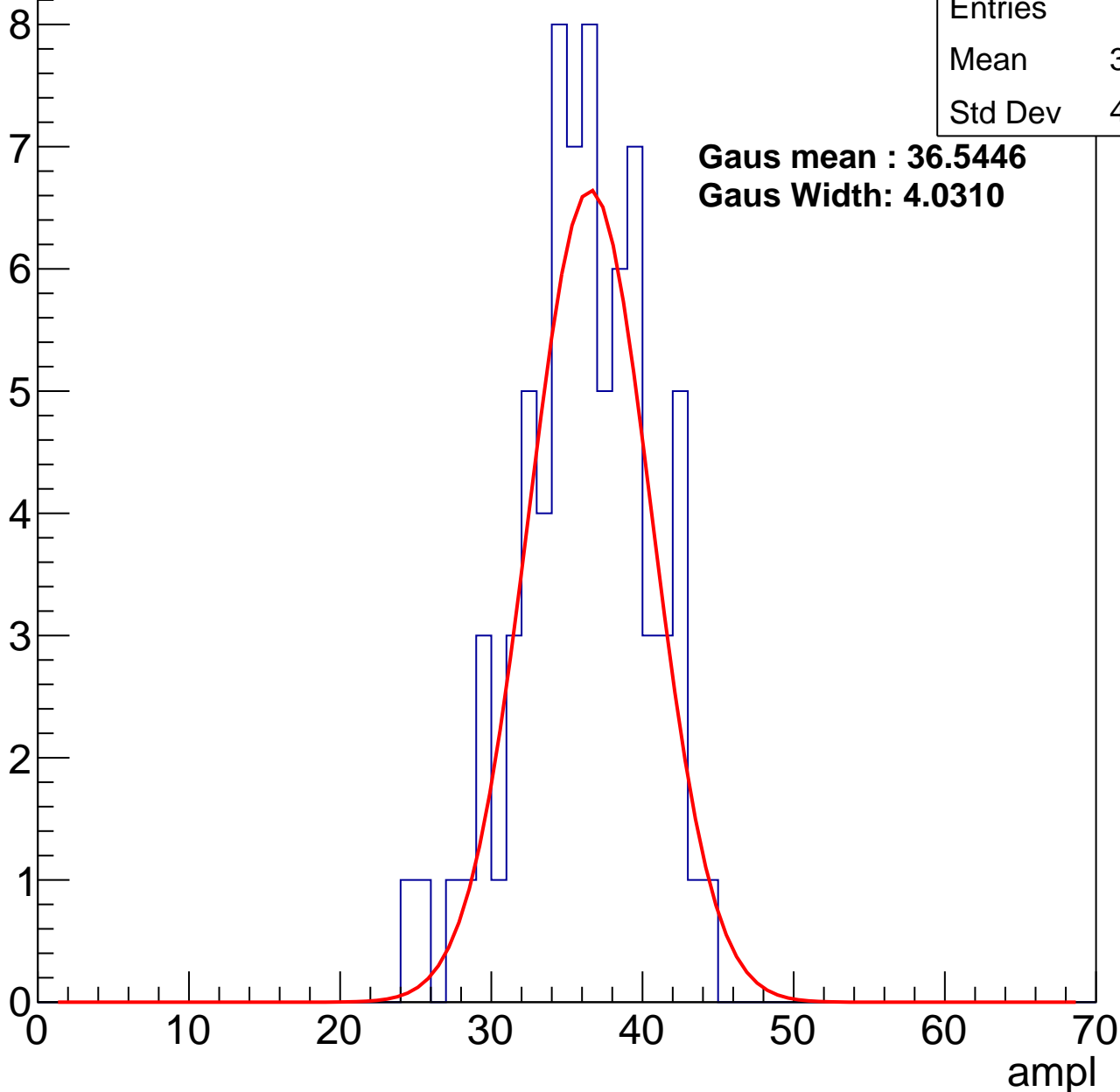
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	74
Mean	35.64
Std Dev	4.225

**Gaus mean : 36.5446**

**Gaus Width: 4.0310**



# B1L102S, U12-ch2, adc2

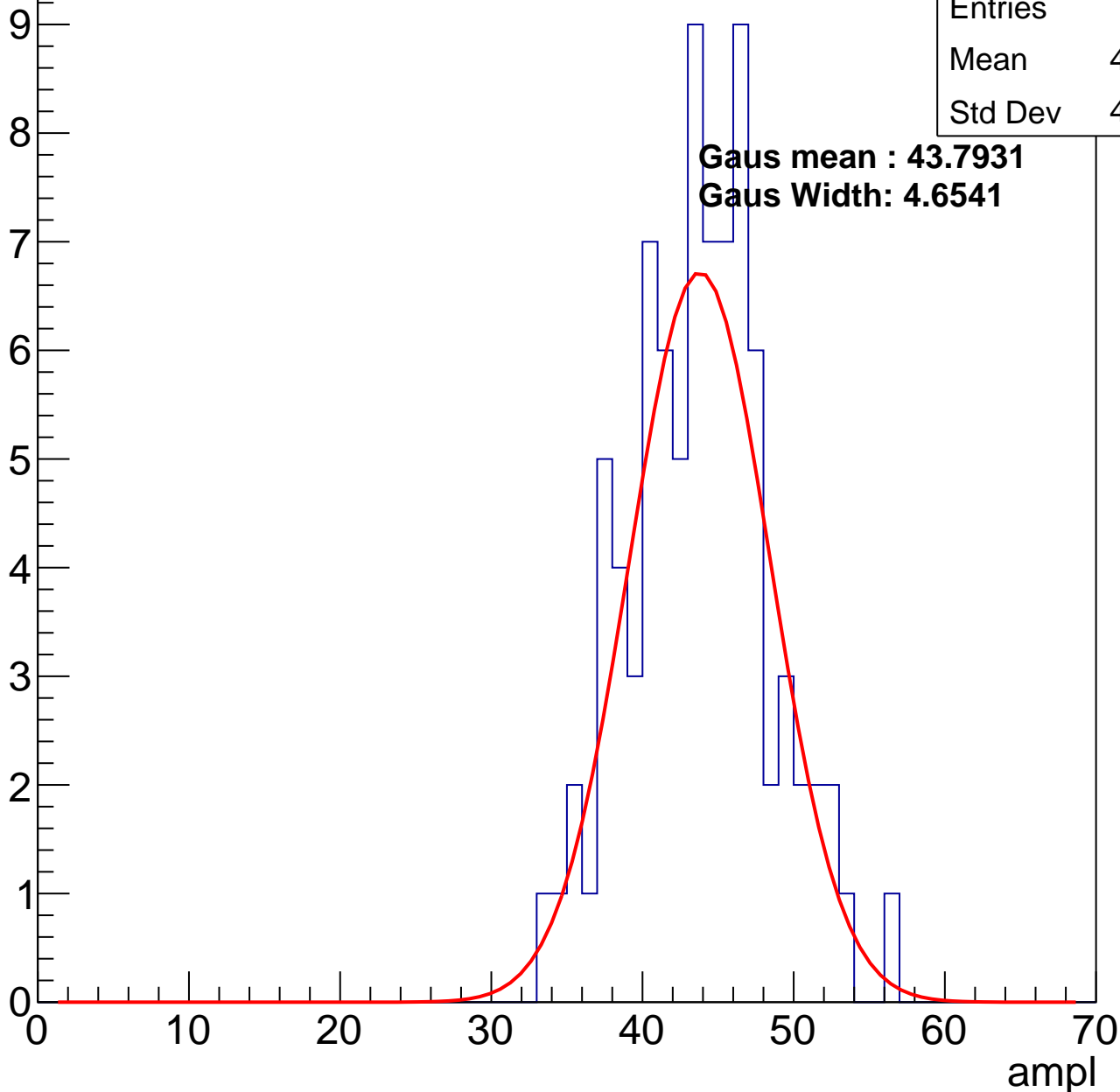
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	86
Mean	43.34
Std Dev	4.569

**Gaus mean : 43.7931**

**Gaus Width: 4.6541**

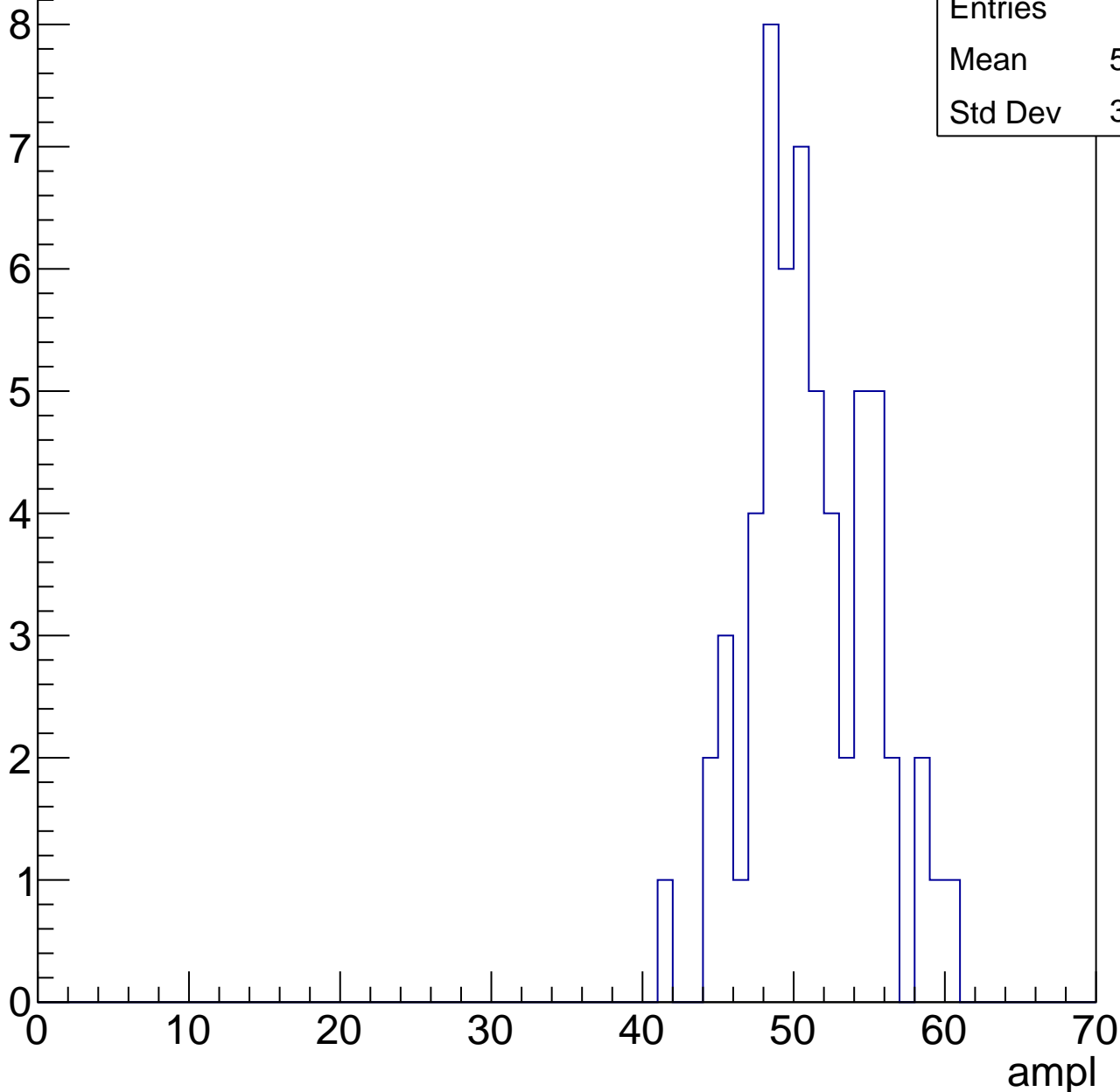


# B1L102S, U12-ch2, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

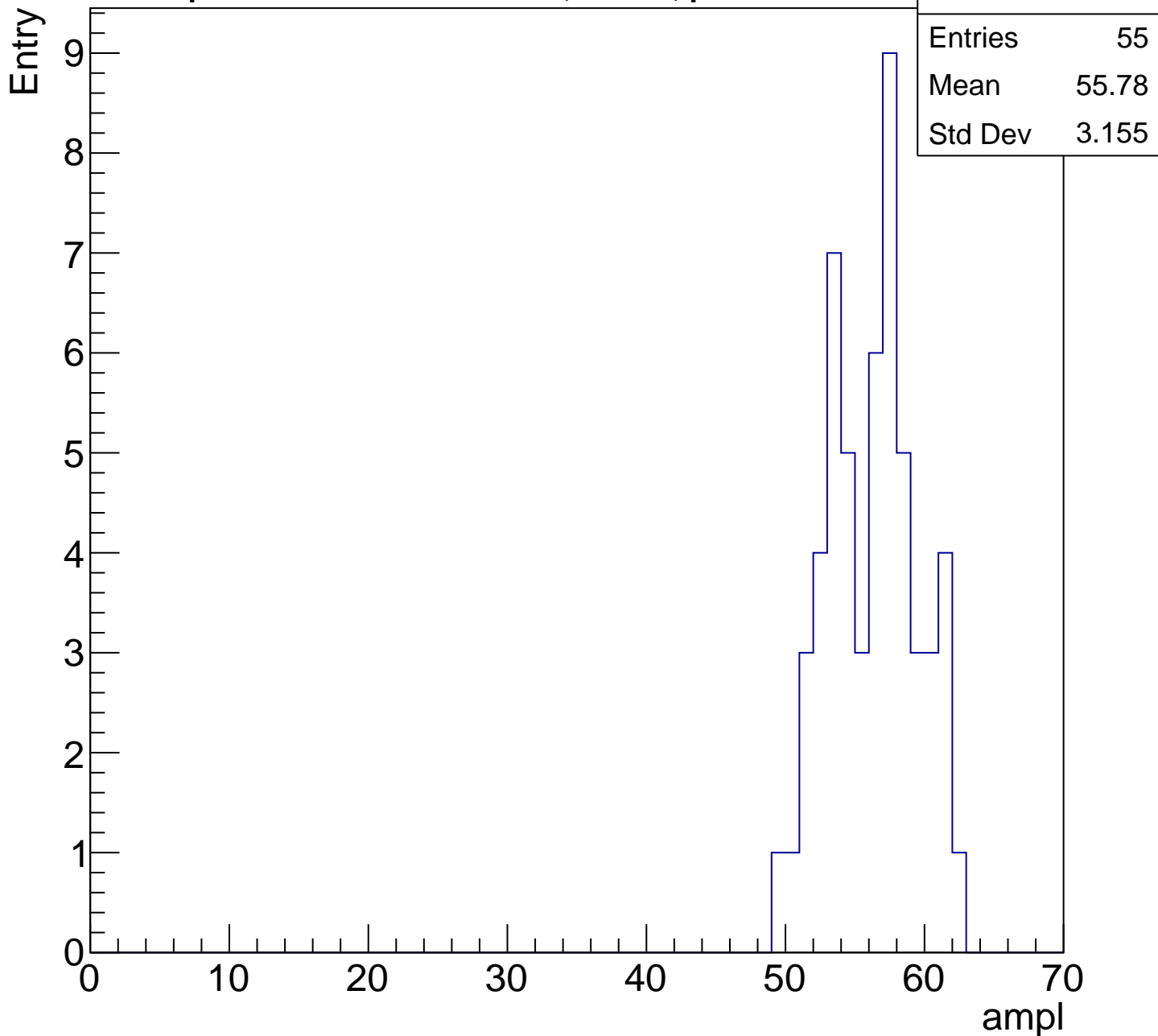
Entry

Entries	59
Mean	50.63
Std Dev	3.948



# B1L102S, U12-ch2, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

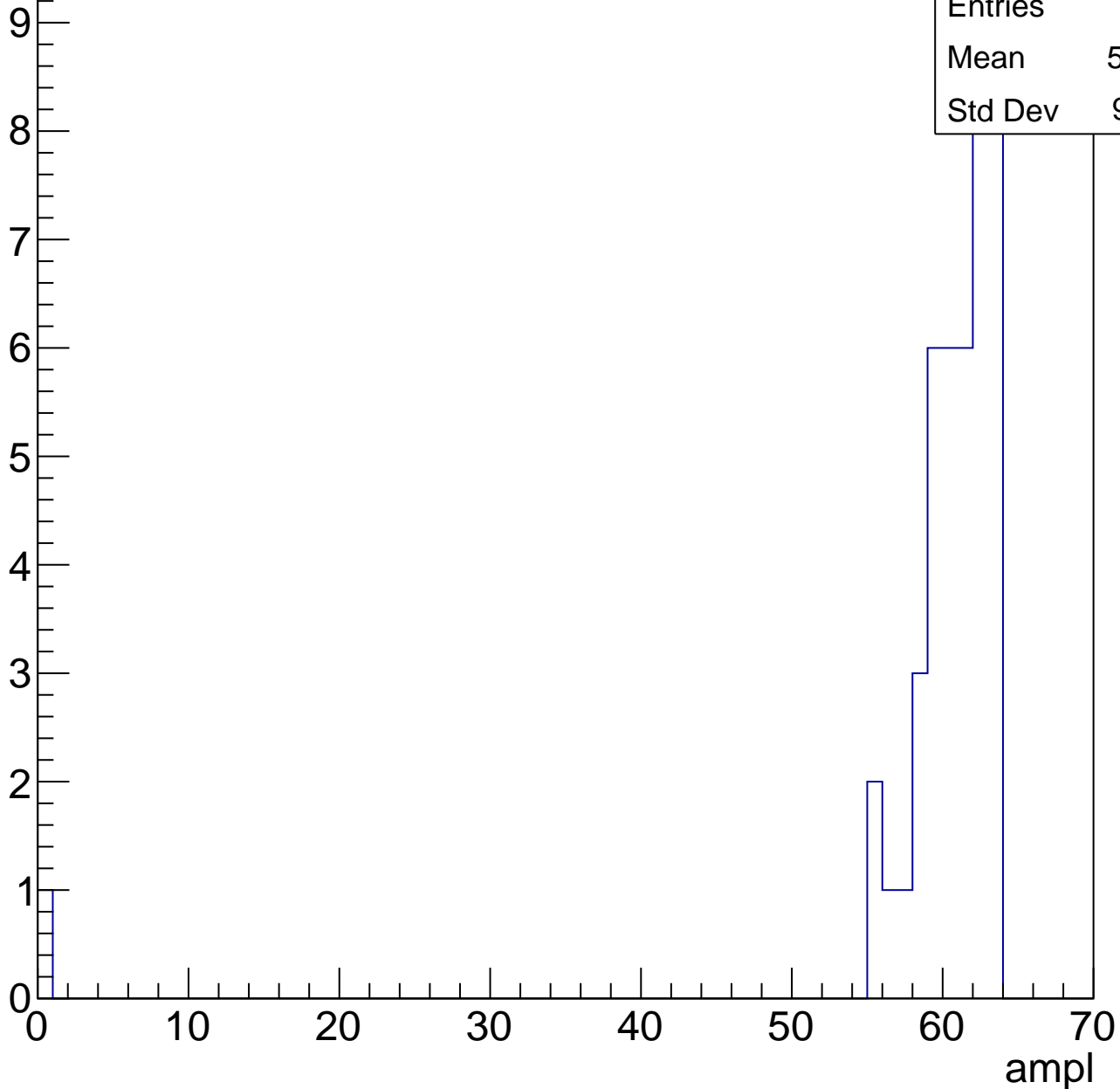


# B1L102S, U12-ch2, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	43
Mean	59.05
Std Dev	9.361



# B1L102S, U12-ch2, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U12-ch2, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U12-ch3, adc0

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	76
Mean	30.05
Std Dev	3.26

**Gaus mean : 30.8054**

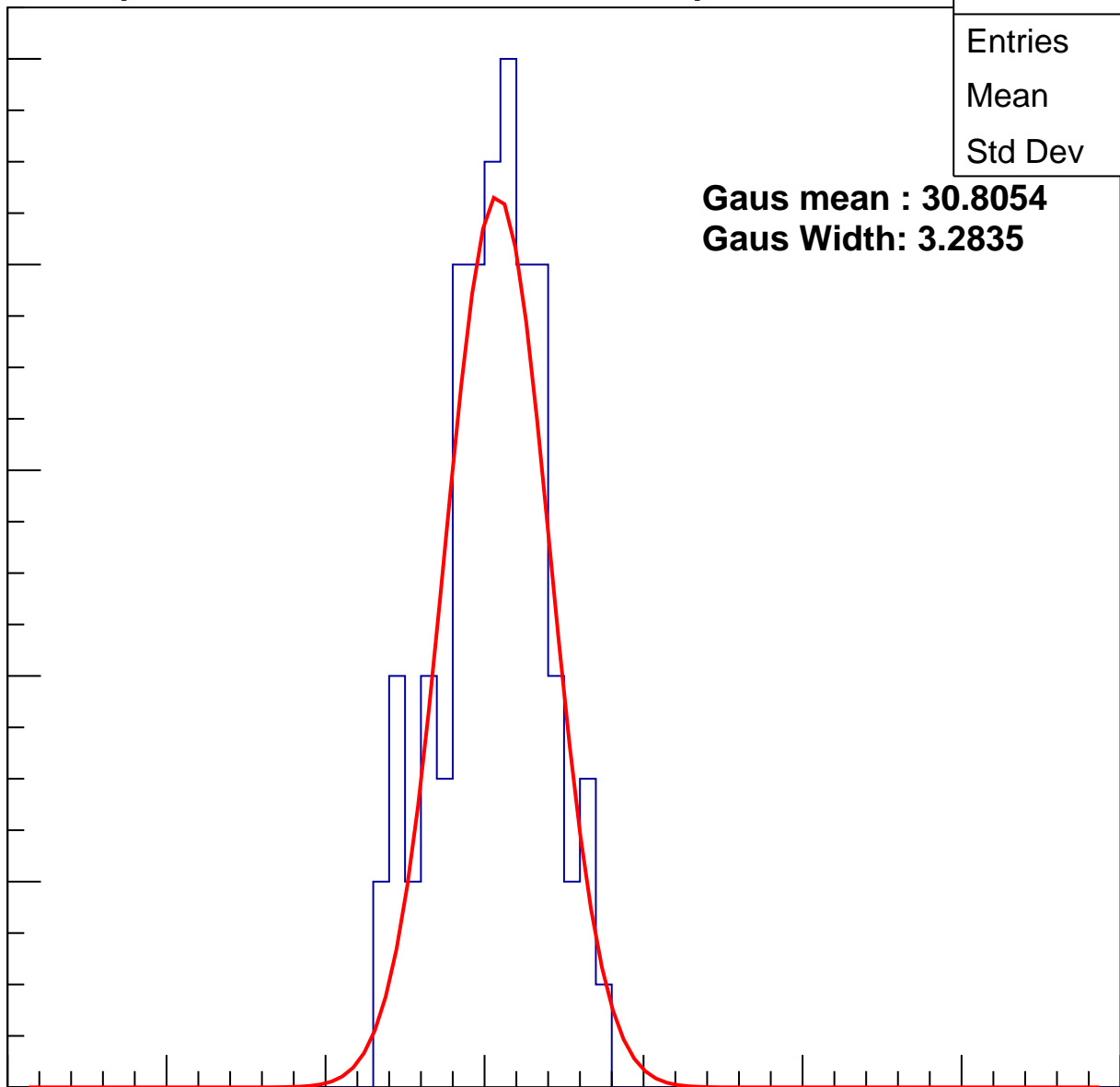
**Gaus Width: 3.2835**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L102S, U12-ch3, adc1

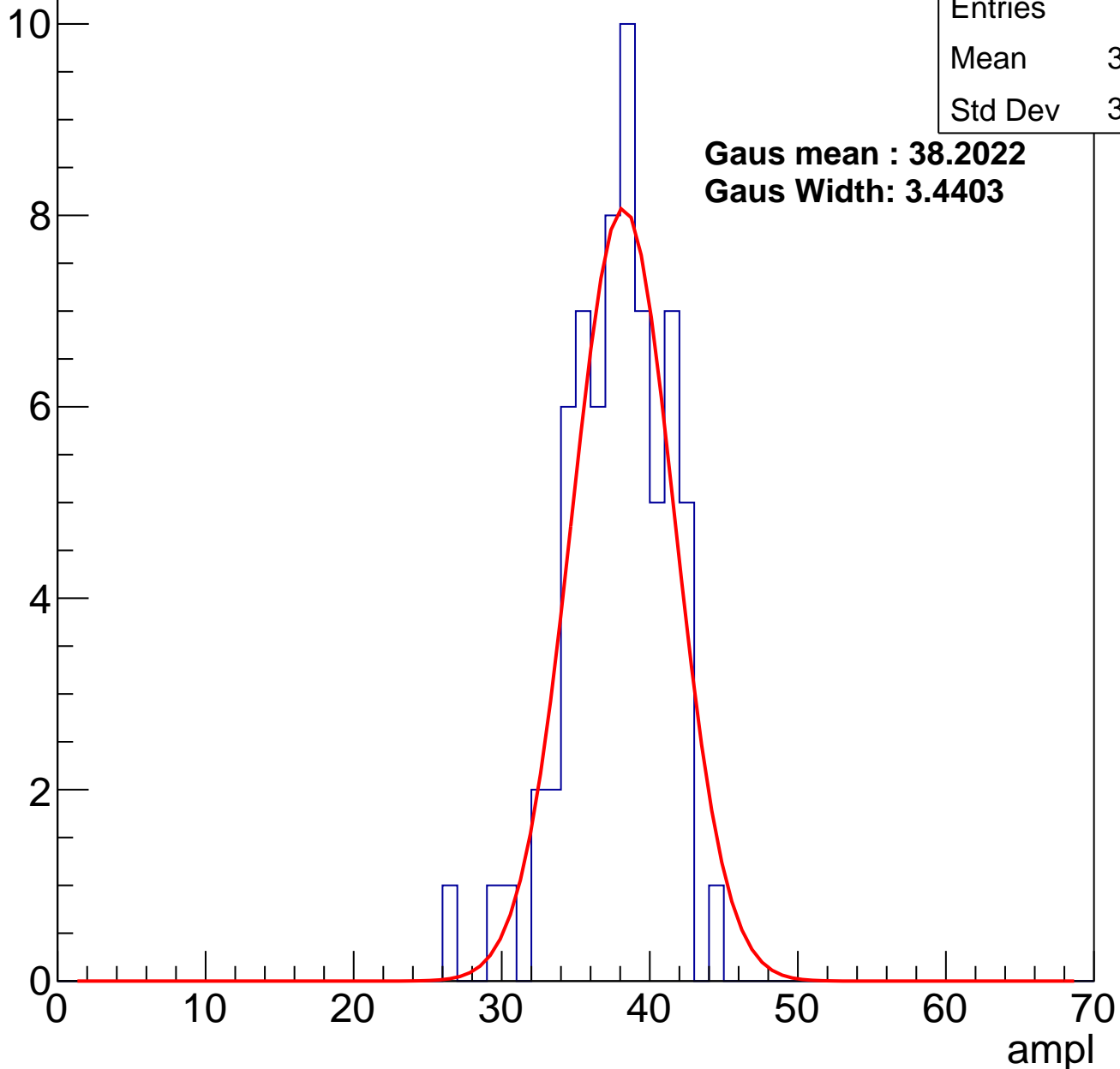
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	69
Mean	37.25
Std Dev	3.338

**Gaus mean : 38.2022**

**Gaus Width: 3.4403**

Entry



# B1L102S, U12-ch3, adc2

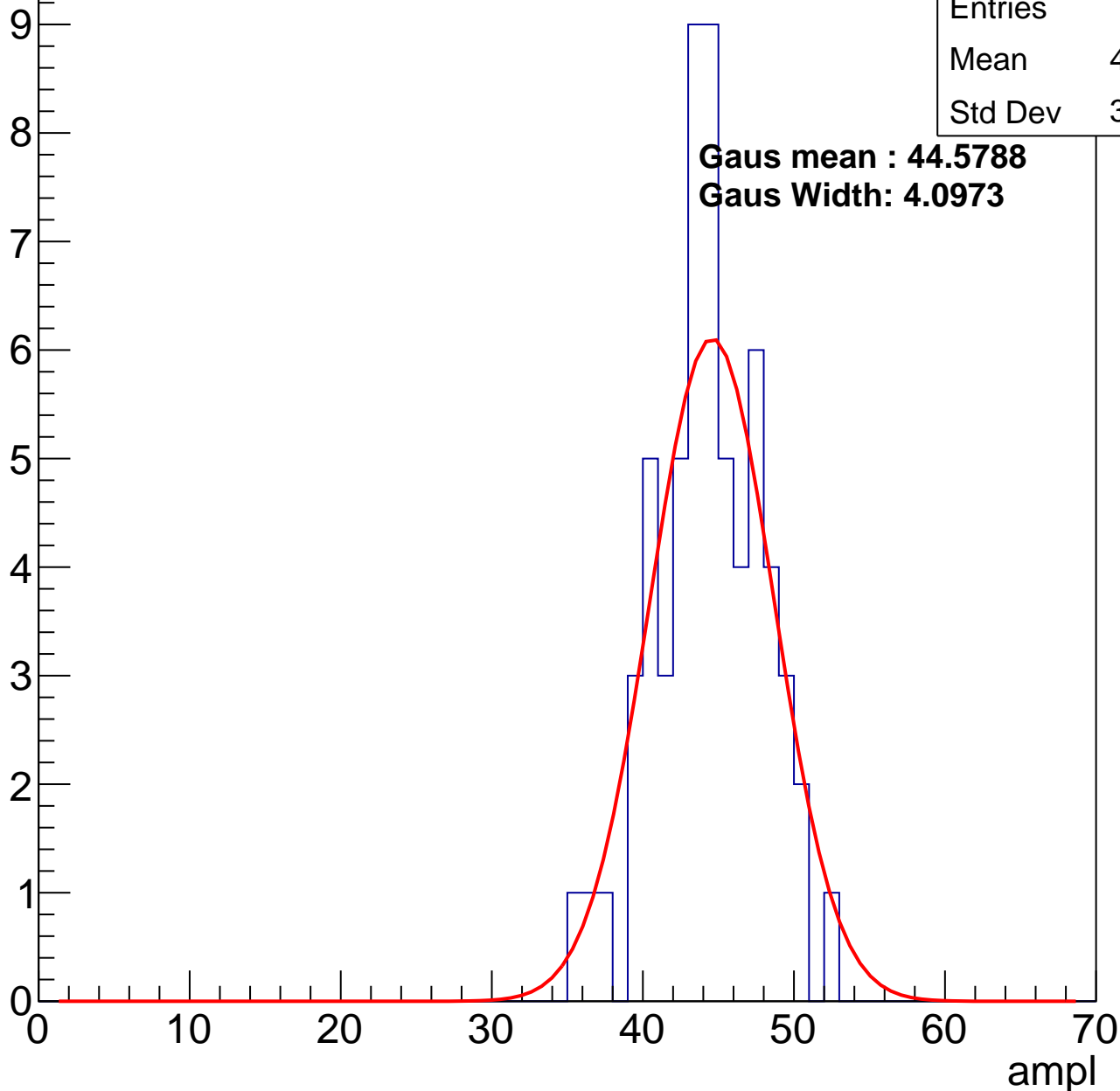
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	62
Mean	43.92
Std Dev	3.489

**Gaus mean : 44.5788**

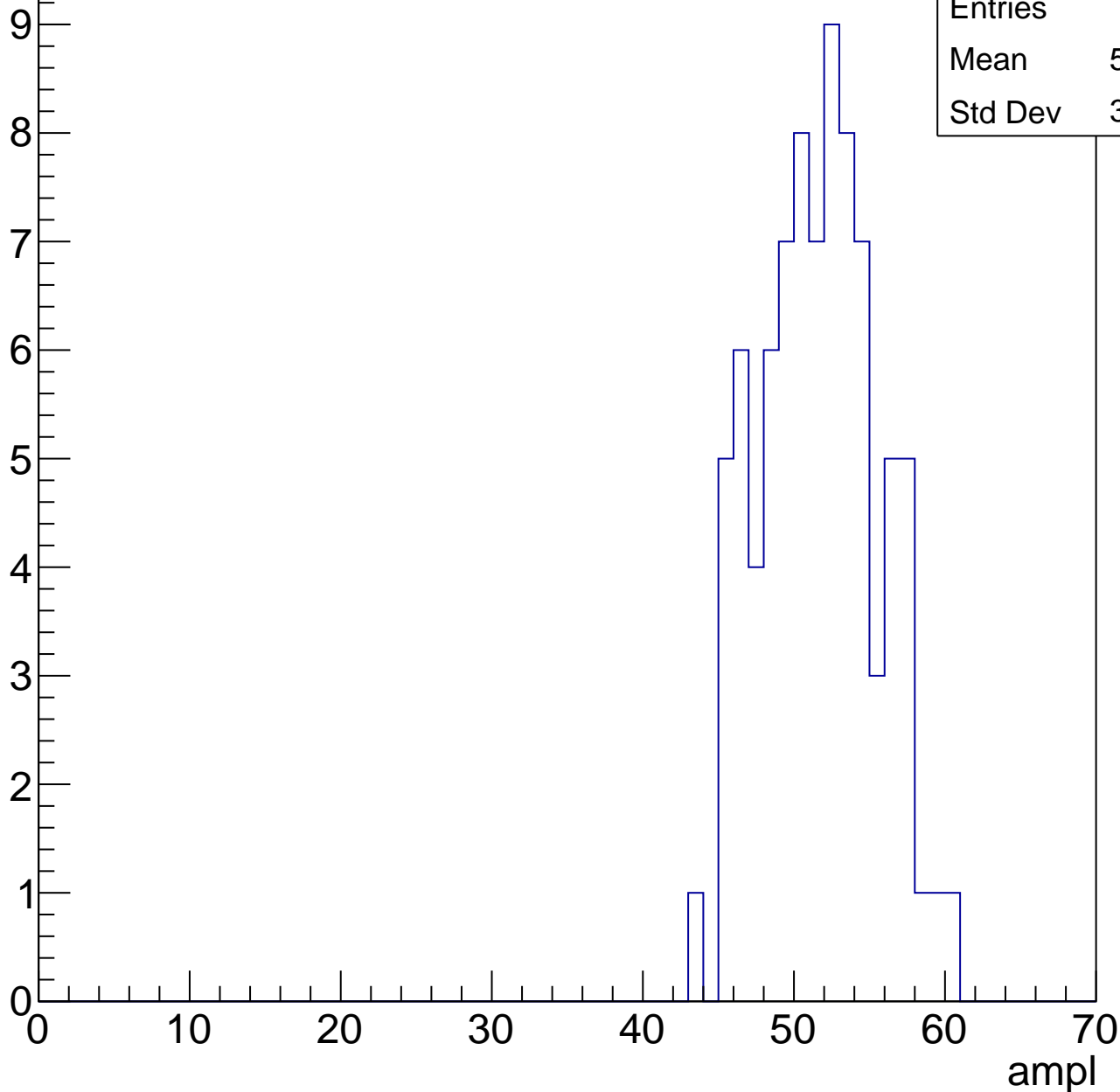
**Gaus Width: 4.0973**



# B1L102S, U12-ch3, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

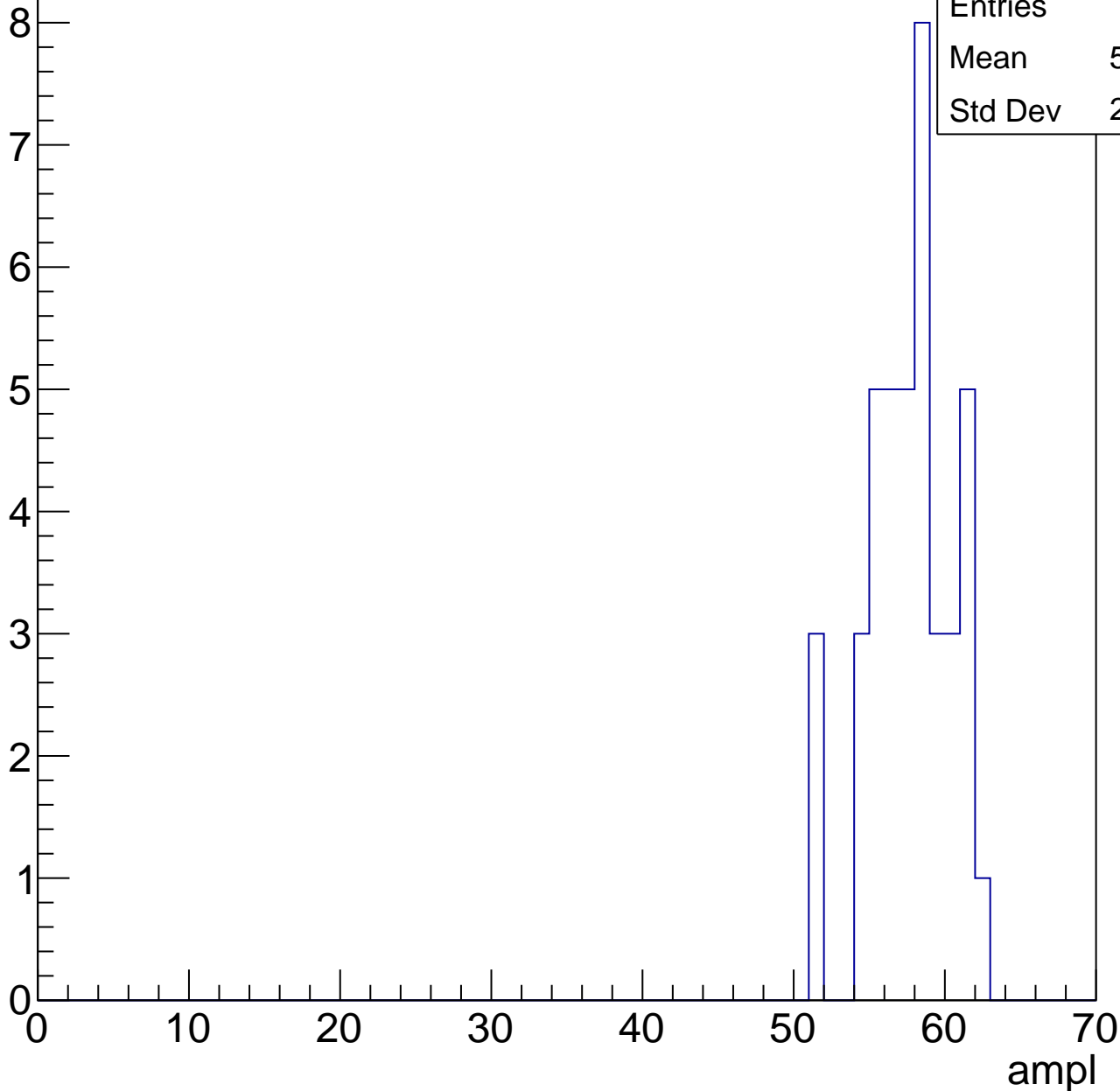


# B1L102S, U12-ch3, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	41
Mean	57.15
Std Dev	2.755

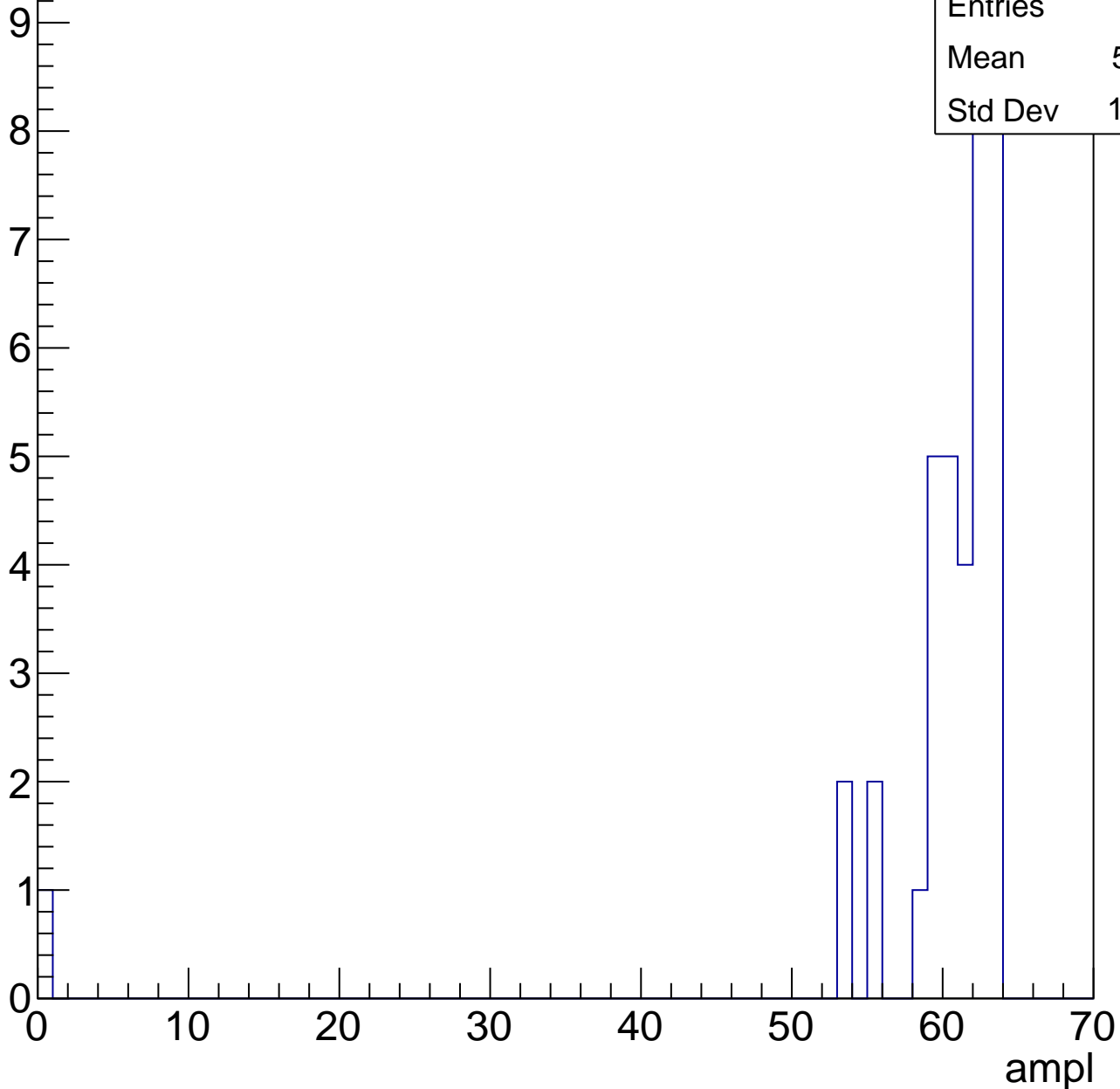


# B1L102S, U12-ch3, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

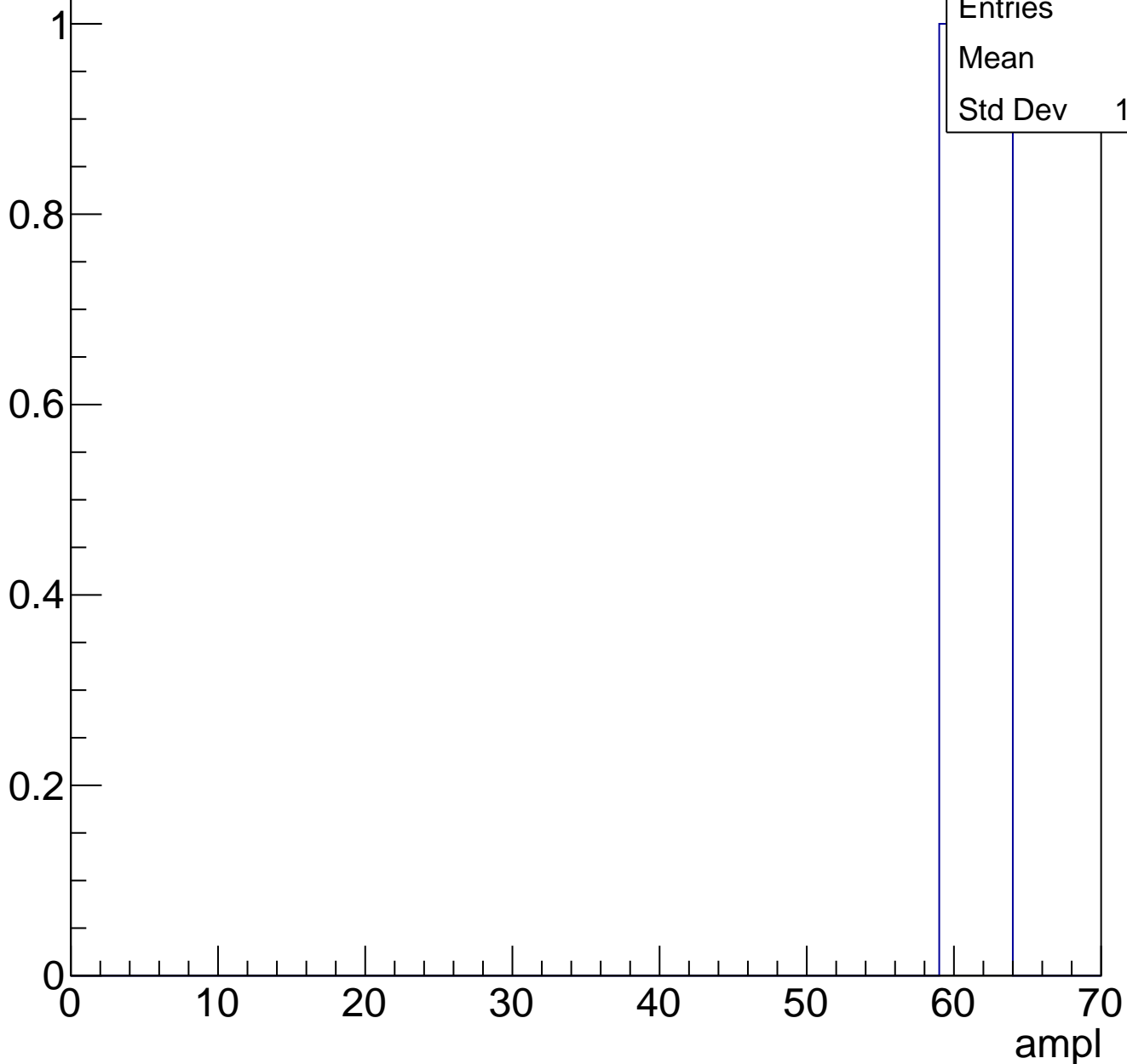
Entries	37
Mean	58.81
Std Dev	10.16



# B1L102S, U12-ch3, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U12-ch3, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U12-ch4, adc0

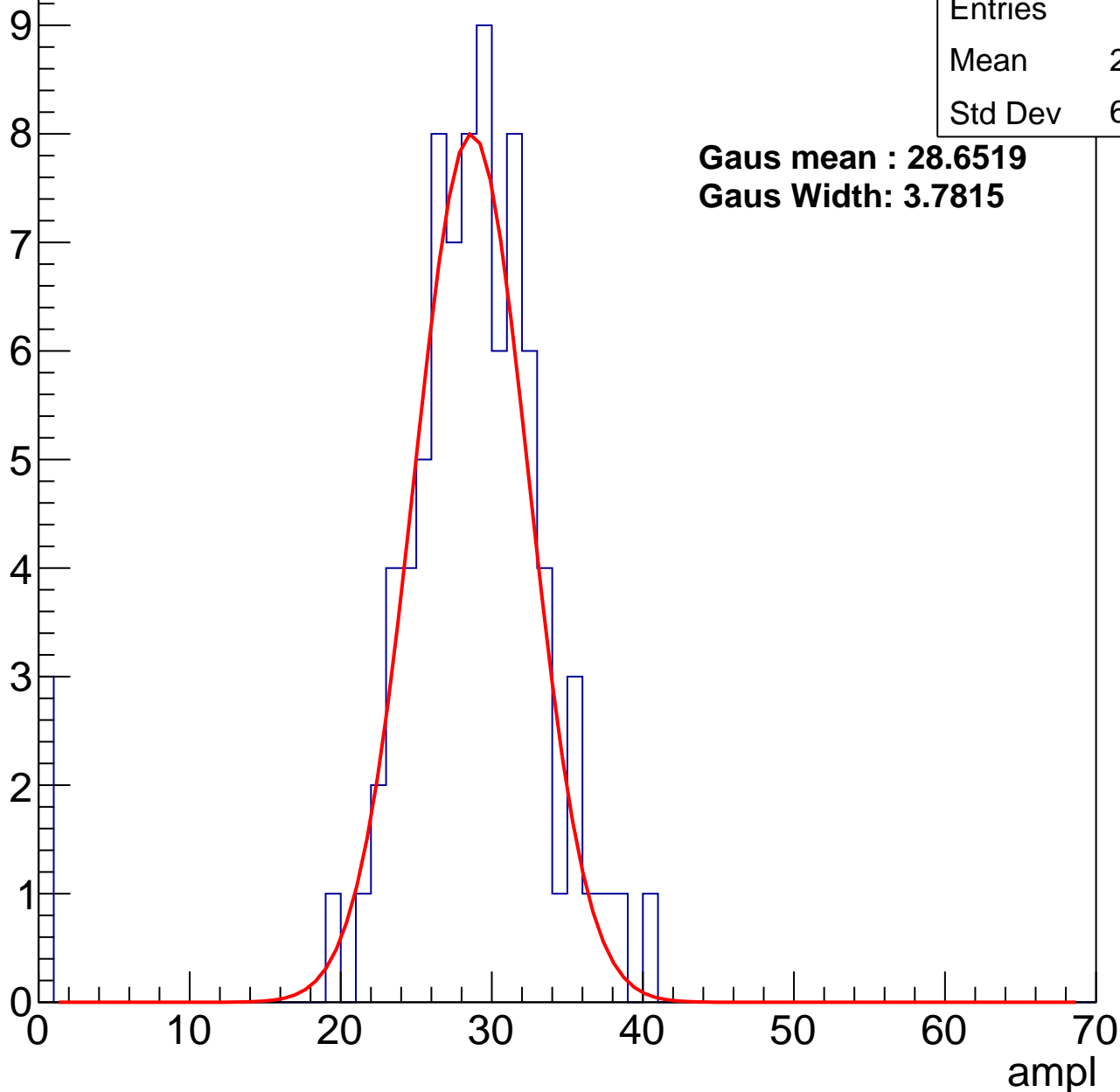
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	84
Mean	27.63
Std Dev	6.604

**Gaus mean : 28.6519**

**Gaus Width: 3.7815**



# B1L102S, U12-ch4, adc1

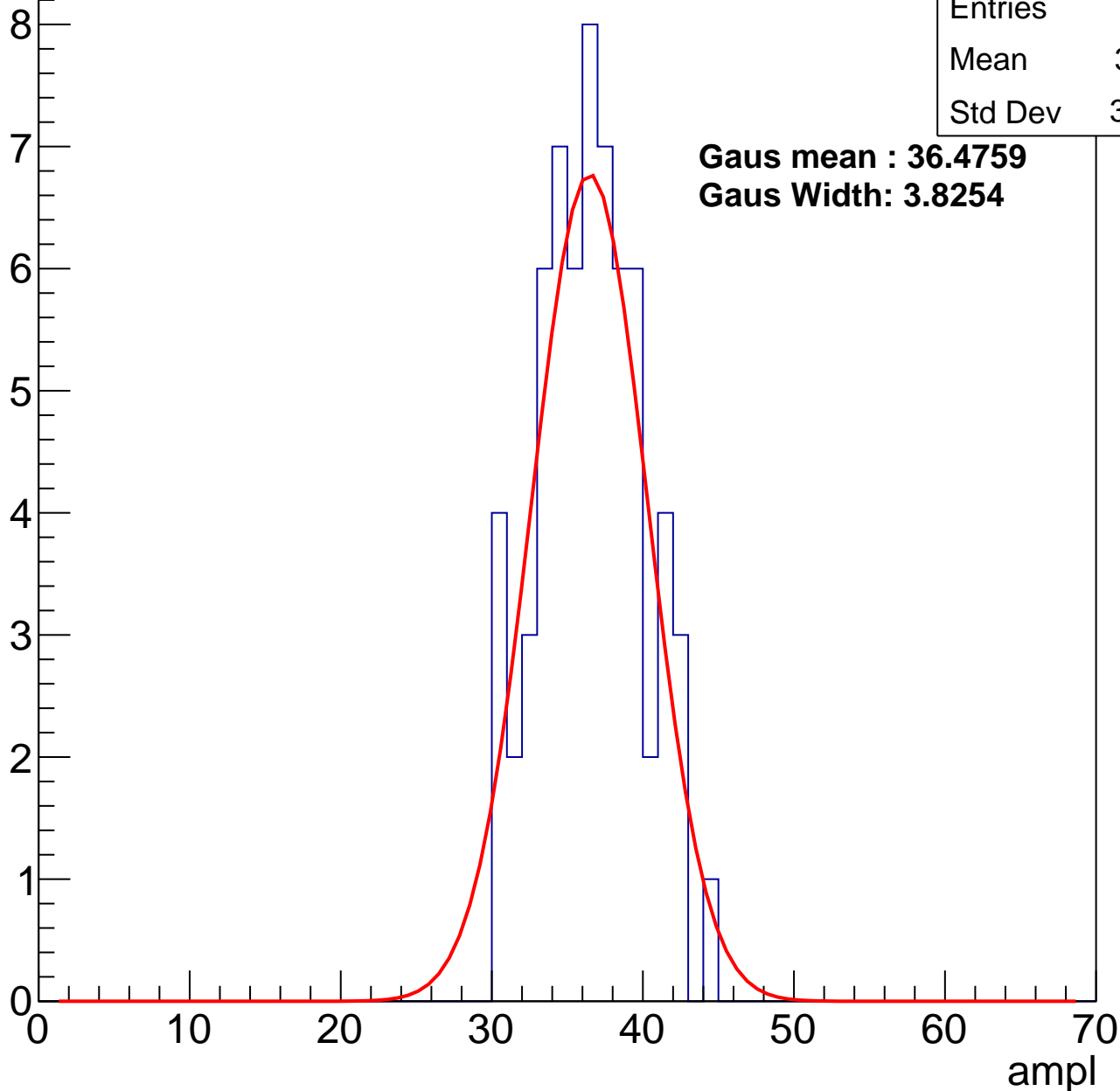
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	65
Mean	36.11
Std Dev	3.324

**Gaus mean : 36.4759**

**Gaus Width: 3.8254**



# B1L102S, U12-ch4, adc2

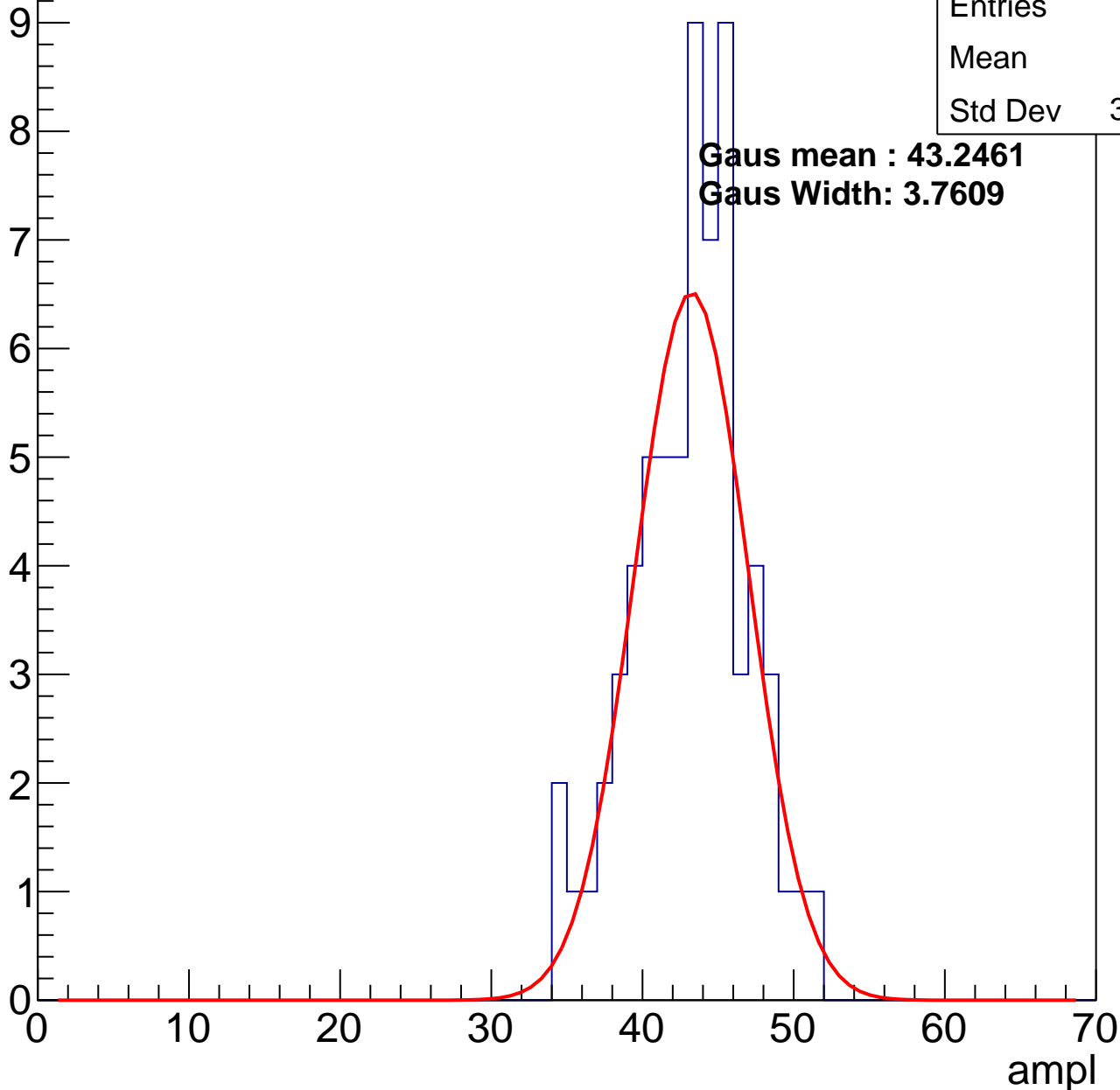
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	42.7
Std Dev	3.709

**Gaus mean : 43.2461**

**Gaus Width: 3.7609**

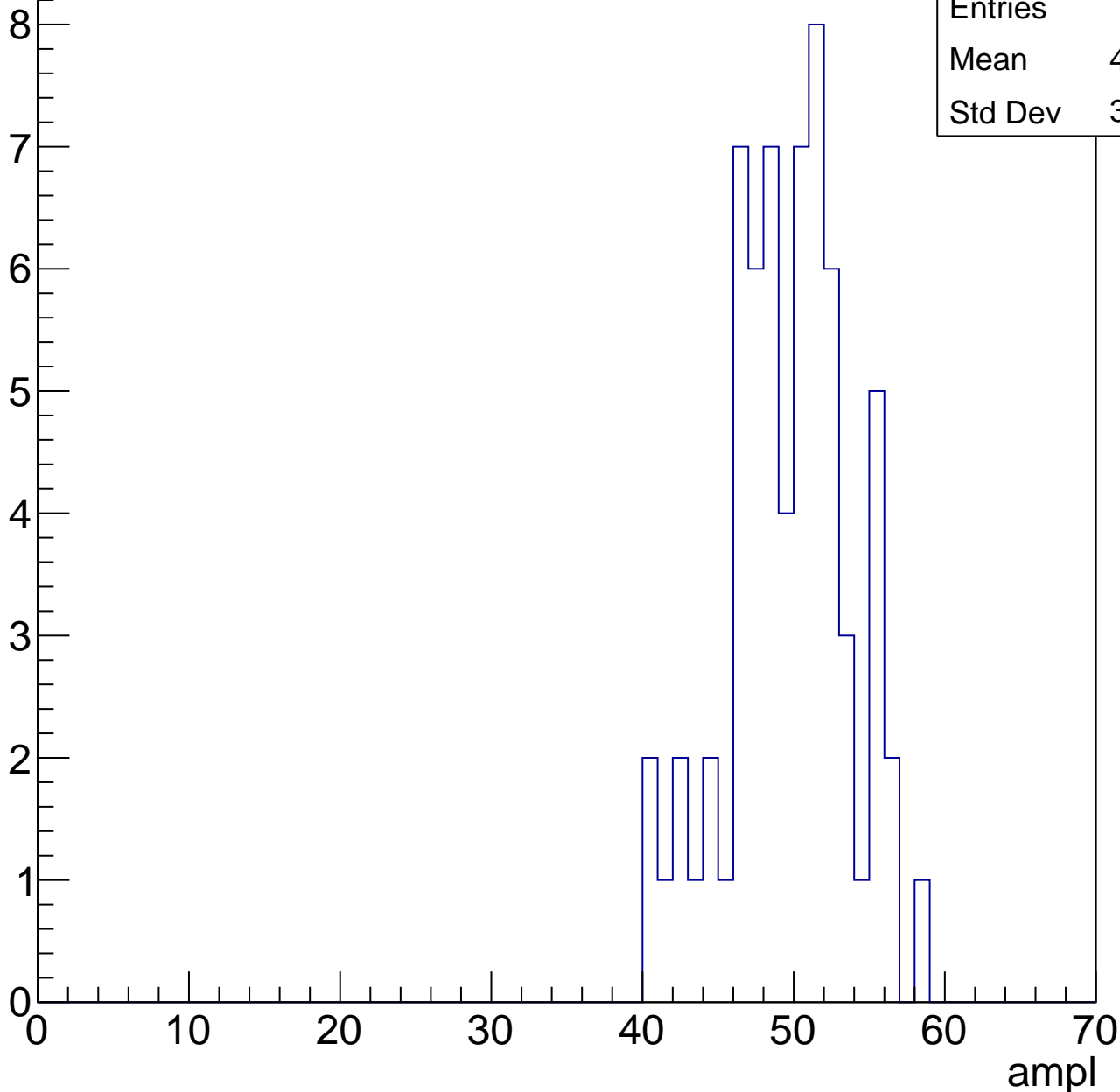


# B1L102S, U12-ch4, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

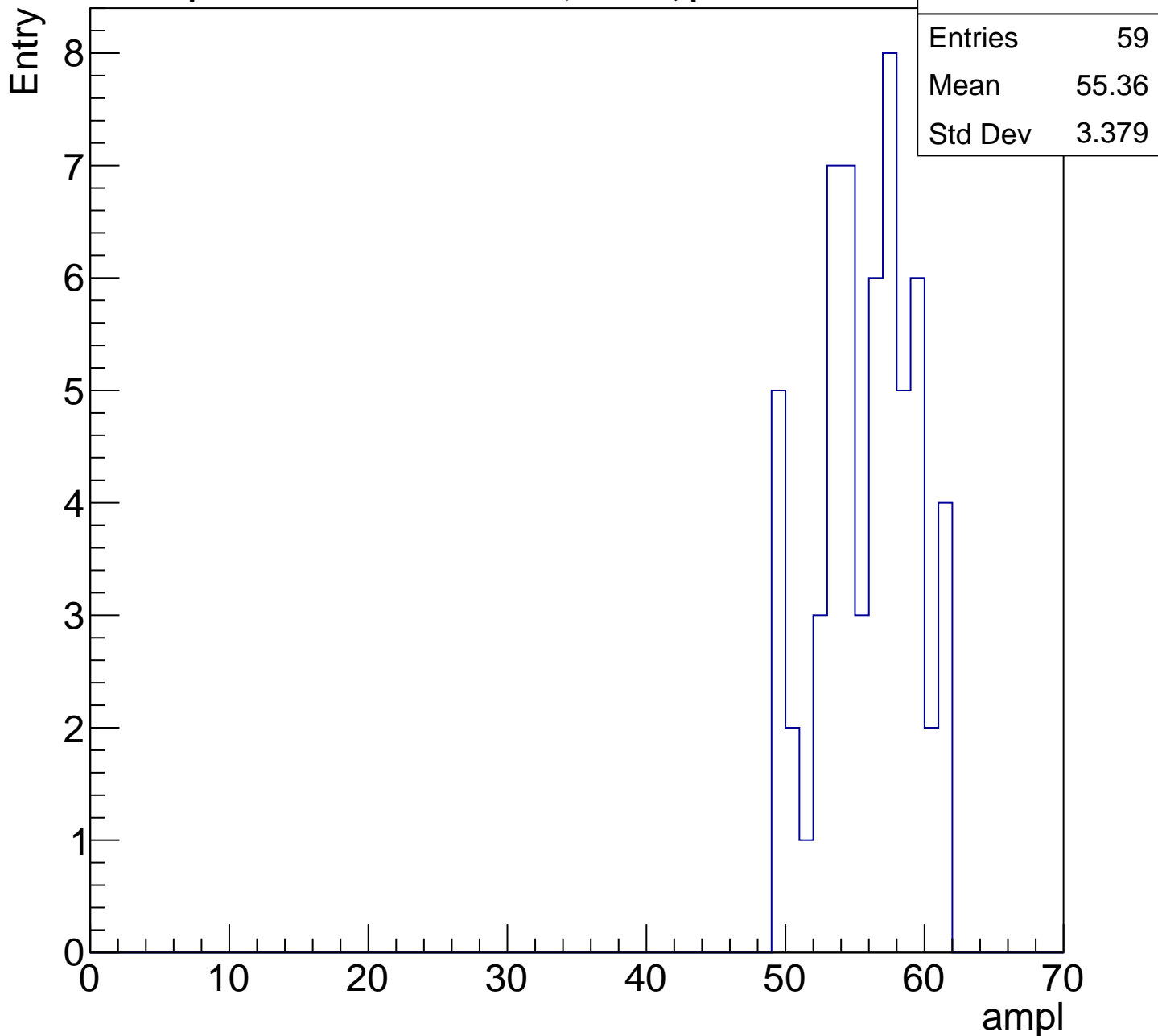
Entry

Entries	66
Mean	49.17
Std Dev	3.976



# B1L102S, U12-ch4, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

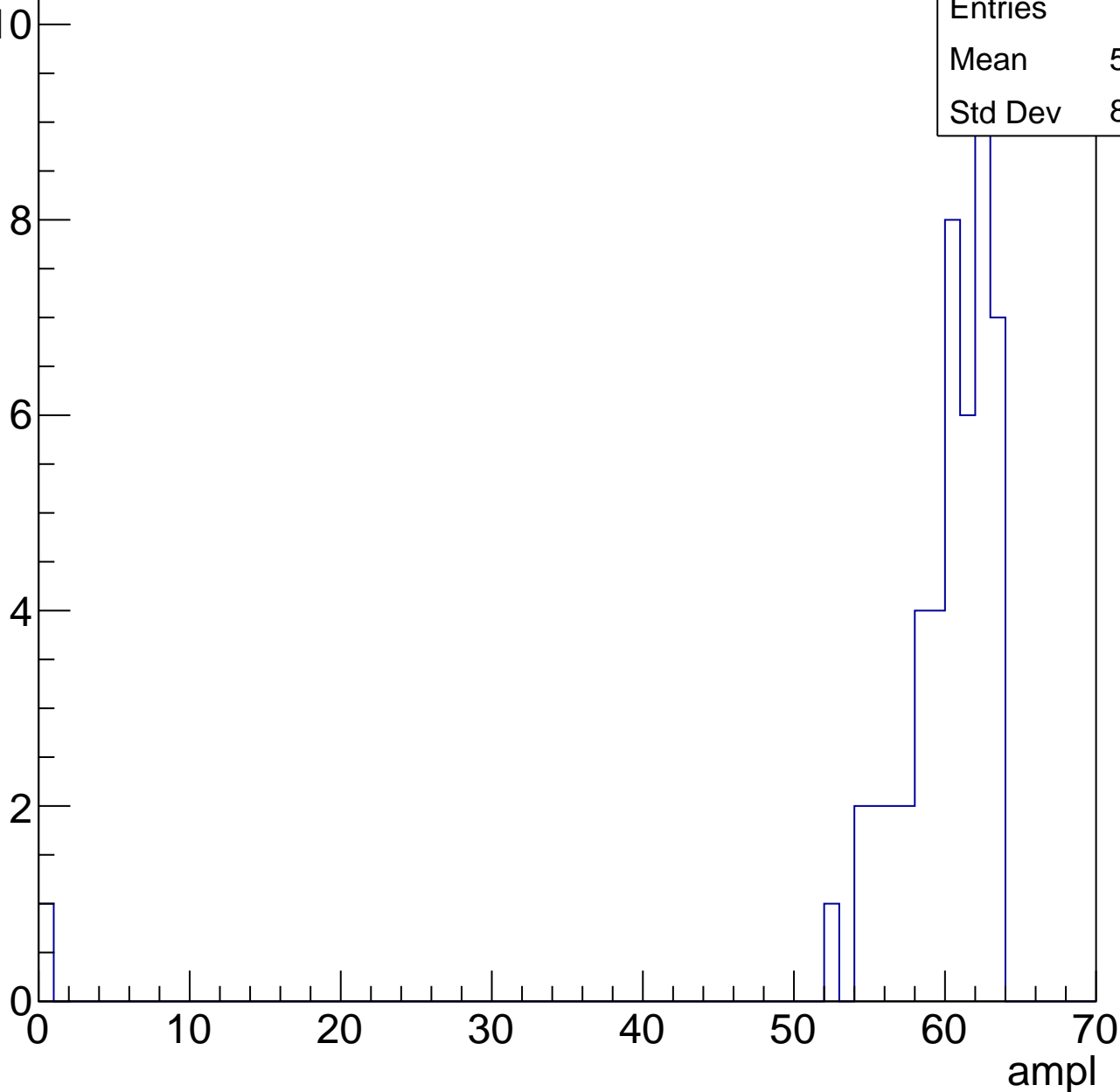


# B1L102S, U12-ch4, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	49
Mean	58.59
Std Dev	8.885



# B1L102S, U12-ch4, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U12-ch4, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

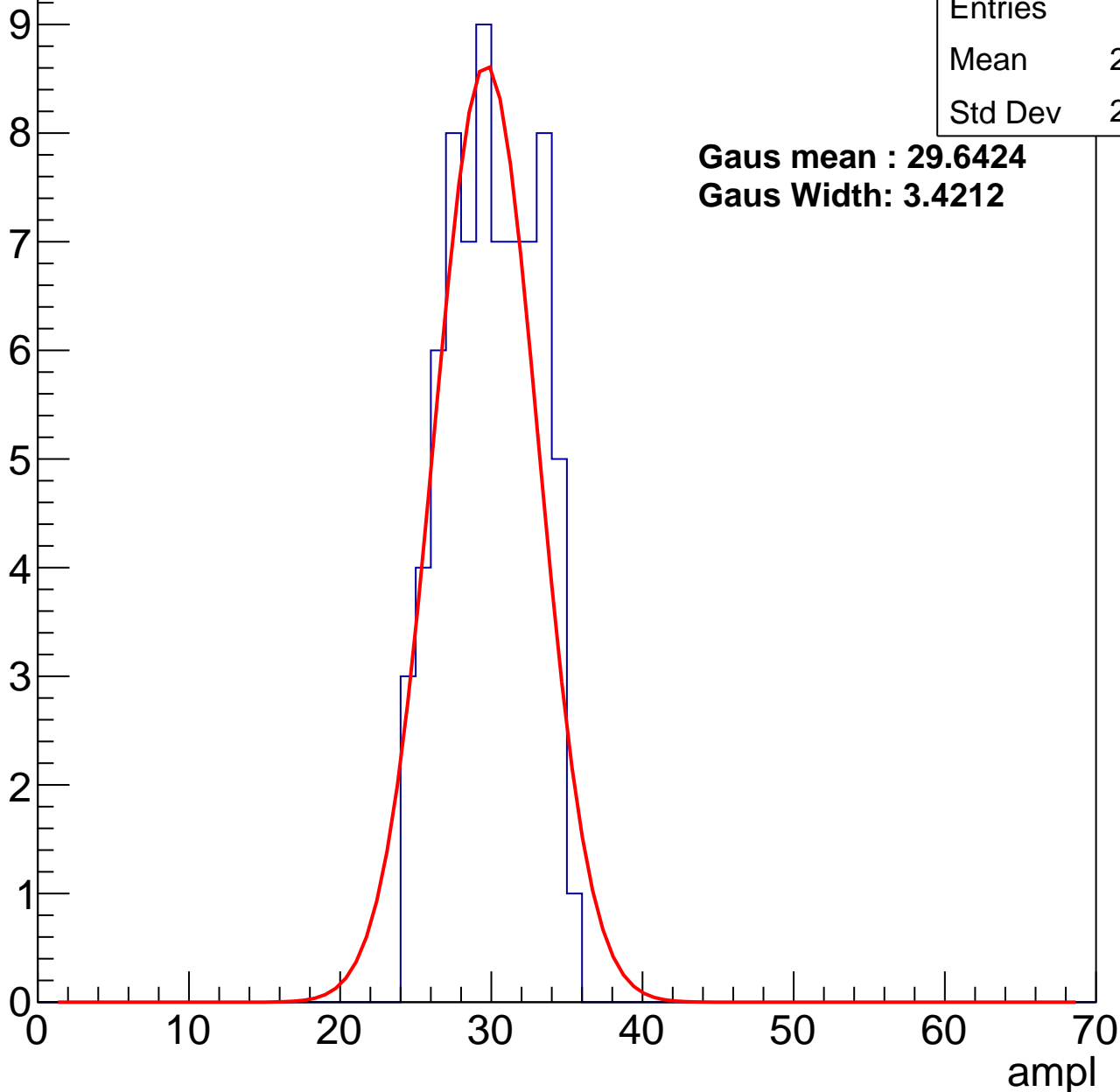


Entries	0
Mean	0
Std Dev	0

# B1L102S, U12-ch5, adc0

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U12-ch5, adc1

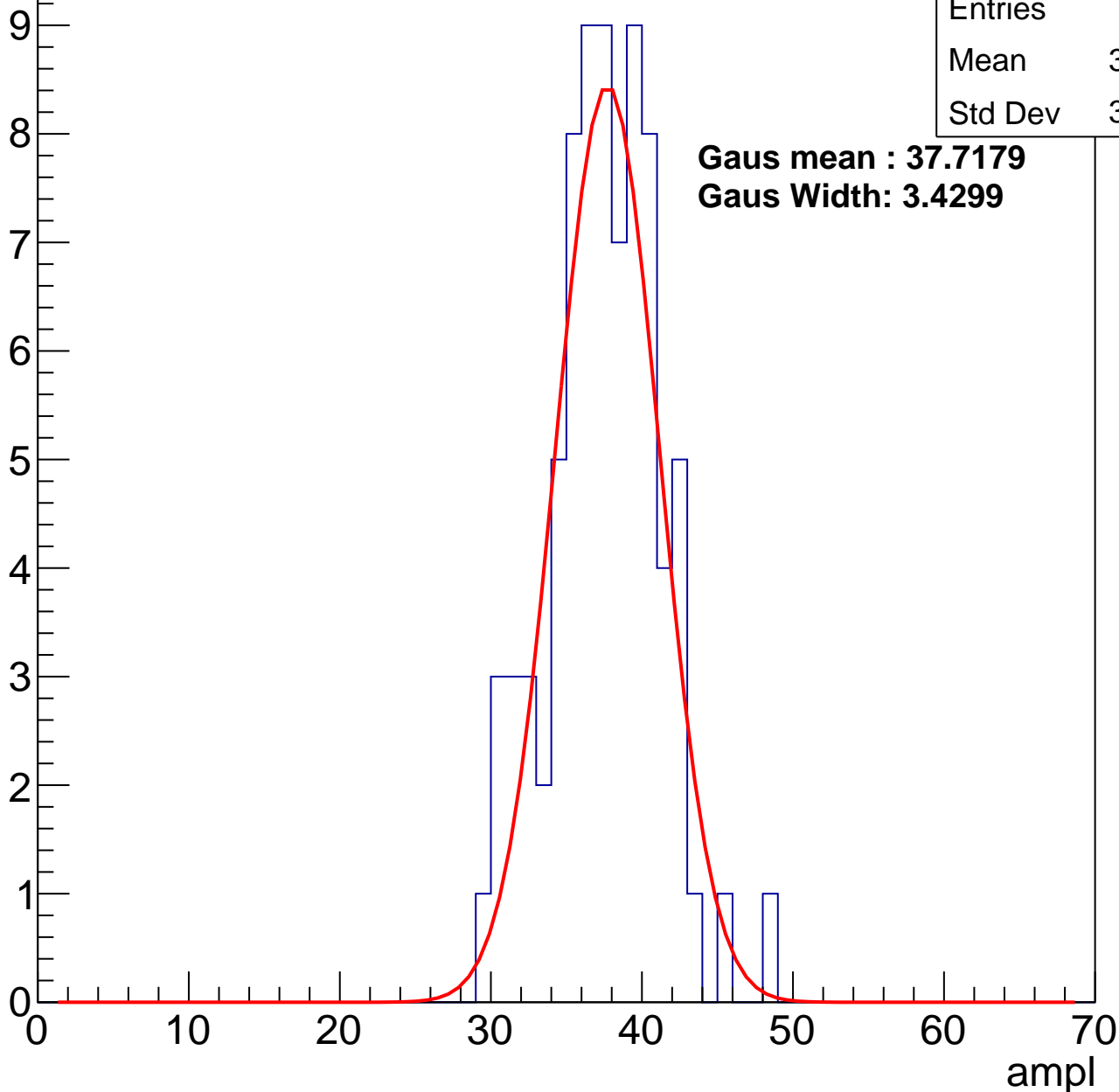
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	79
Mean	37.06
Std Dev	3.623

**Gaus mean : 37.7179**

**Gaus Width: 3.4299**



# B1L102S, U12-ch5, adc2

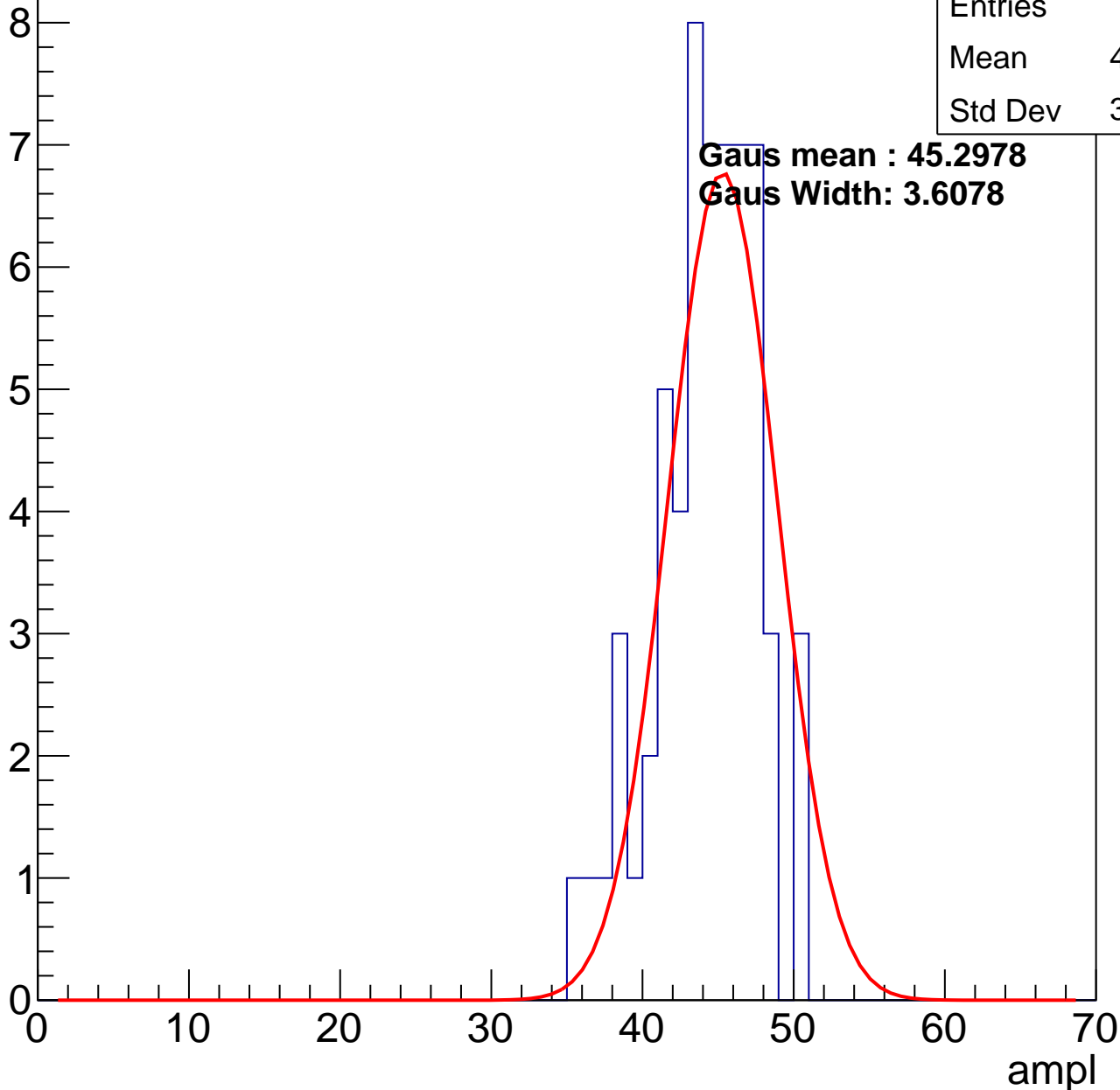
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	60
Mean	43.77
Std Dev	3.363

**Gaus mean : 45.2978**

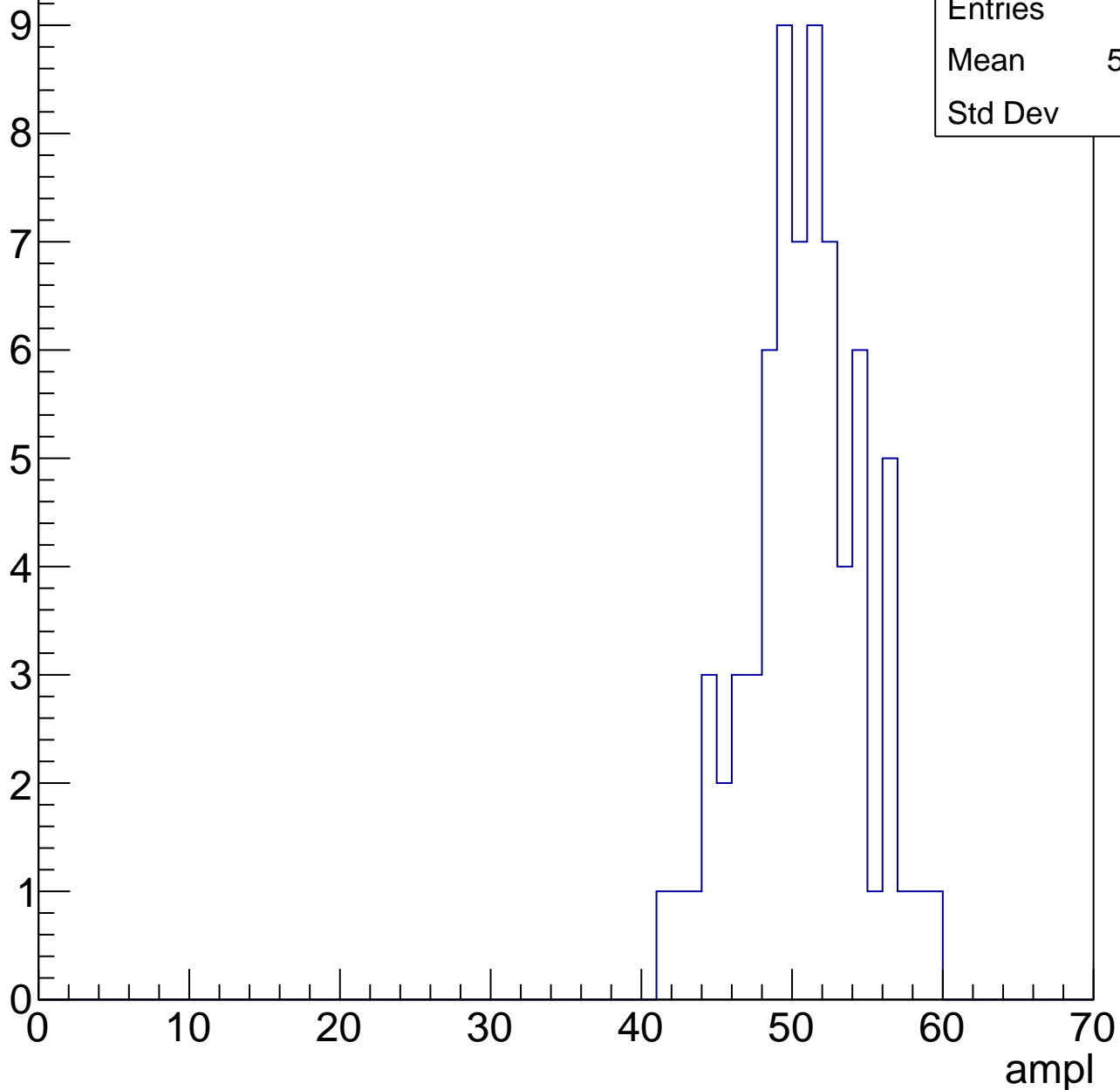
**Gaus Width: 3.6078**



# B1L102S, U12-ch5, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



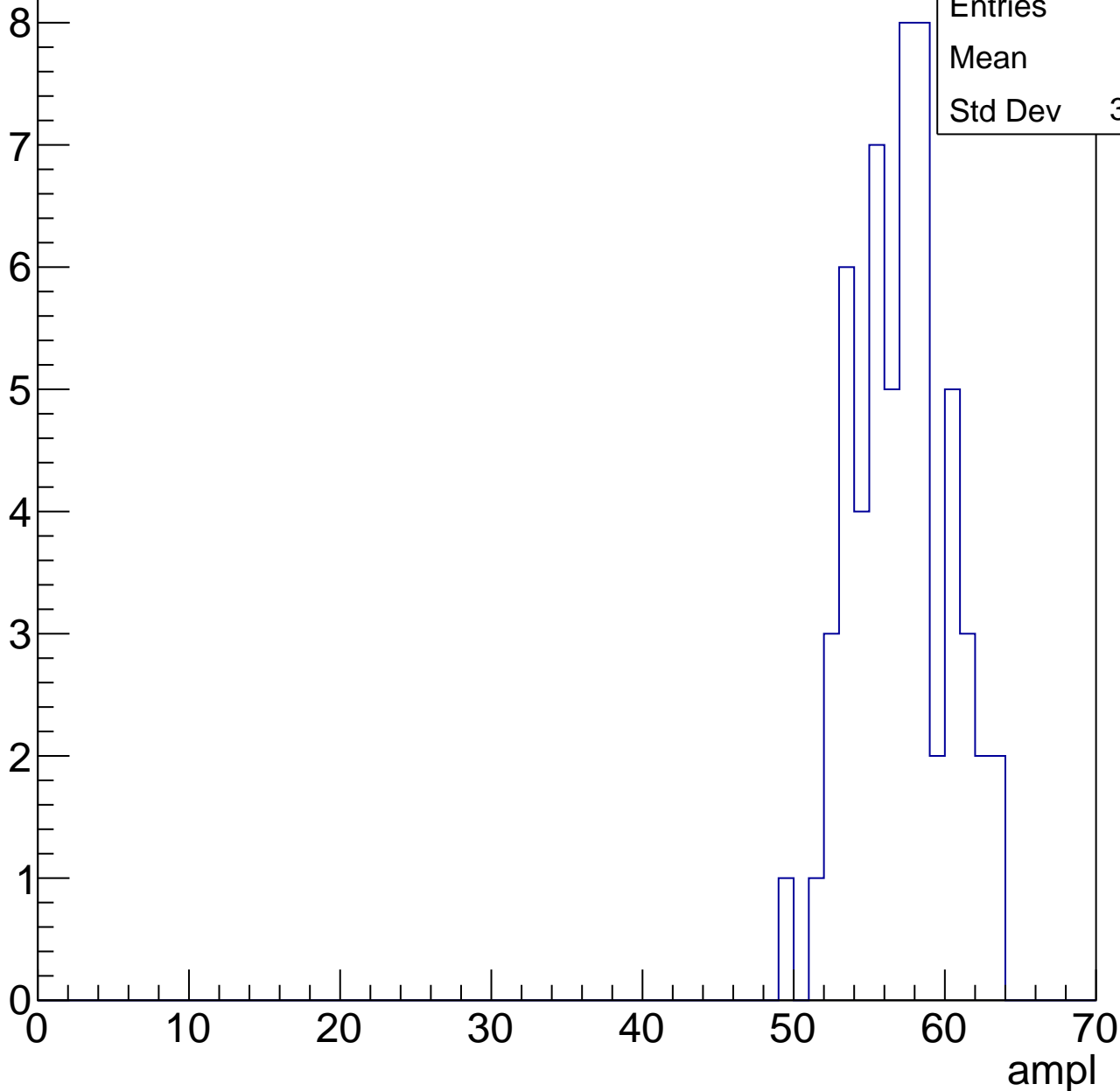
Entries	71
Mean	50.34
Std Dev	3.79

# B1L102S, U12-ch5, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	57
Mean	56.6
Std Dev	3.139



# B1L102S, U12-ch5, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

7

6

5

4

3

2

1

0

Entries

28

Mean

60.39

Std Dev

1.8

ampl

0

10

20

30

40

50

60

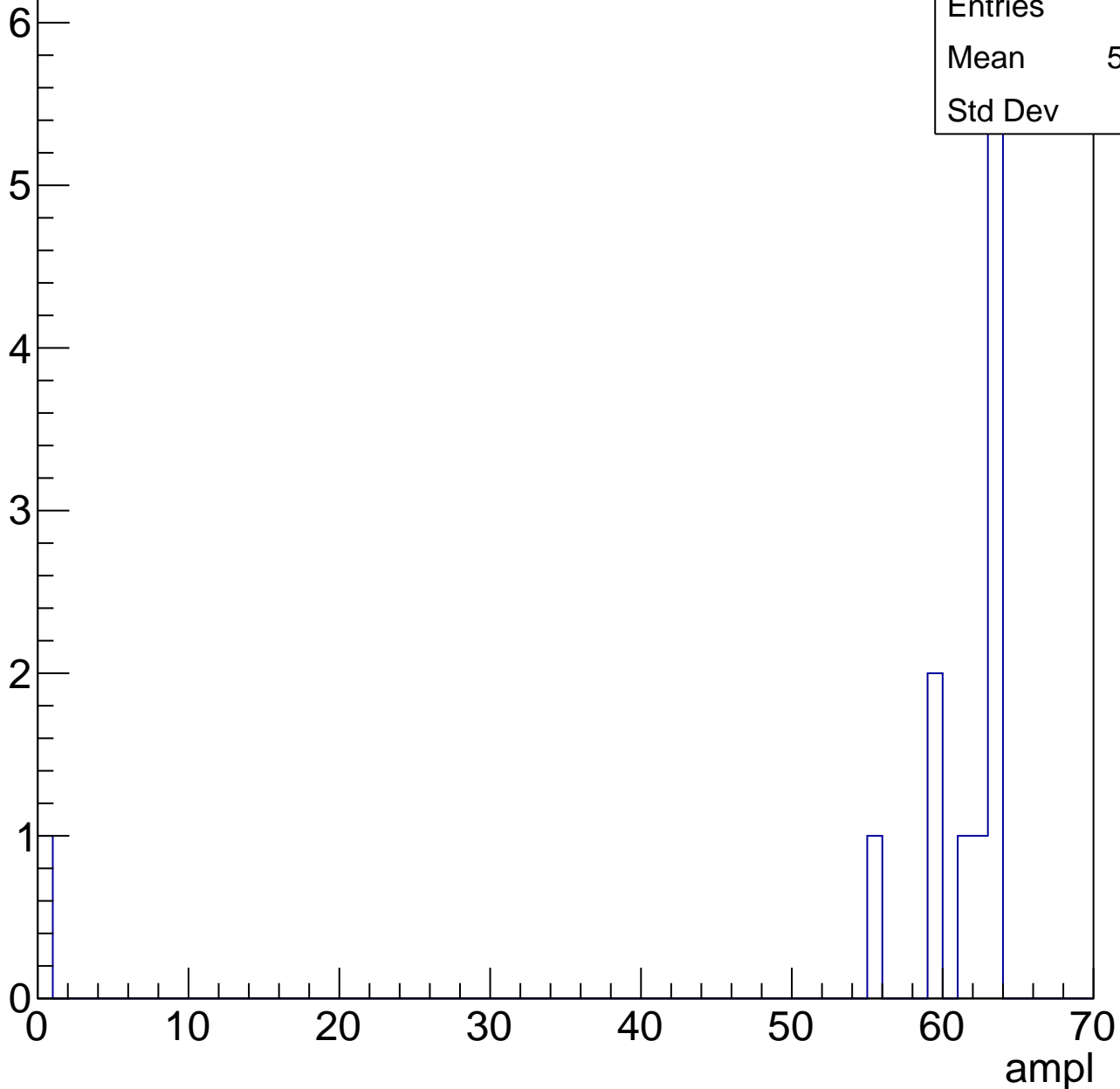
70

# B1L102S, U12-ch5, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	12
Mean	56.17
Std Dev	17.1





# B1L102S, U12-ch5, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U12-ch6, adc0

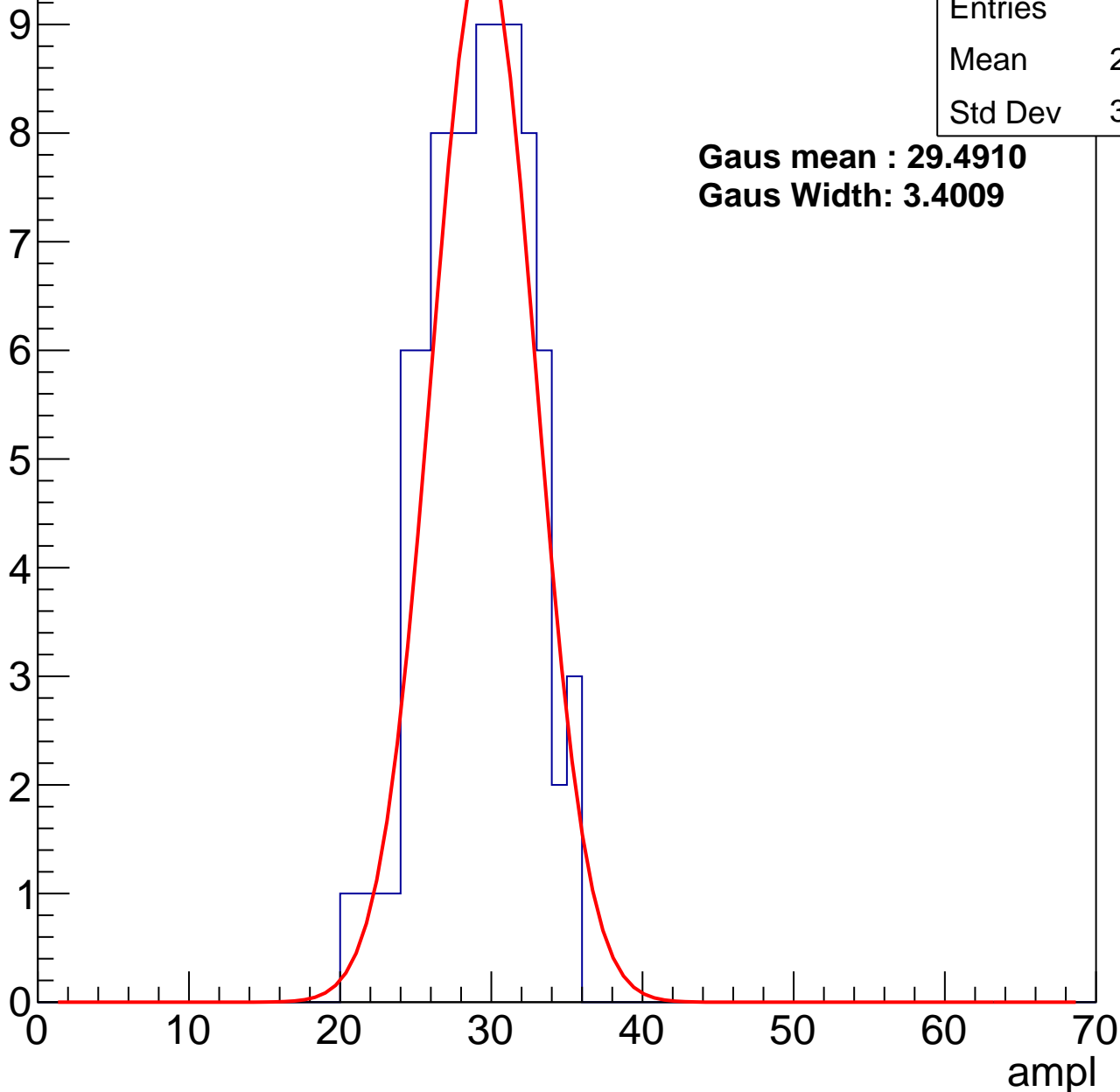
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	86
Mean	28.66
Std Dev	3.322

**Gaus mean : 29.4910**

**Gaus Width: 3.4009**



# B1L102S, U12-ch6, adc1

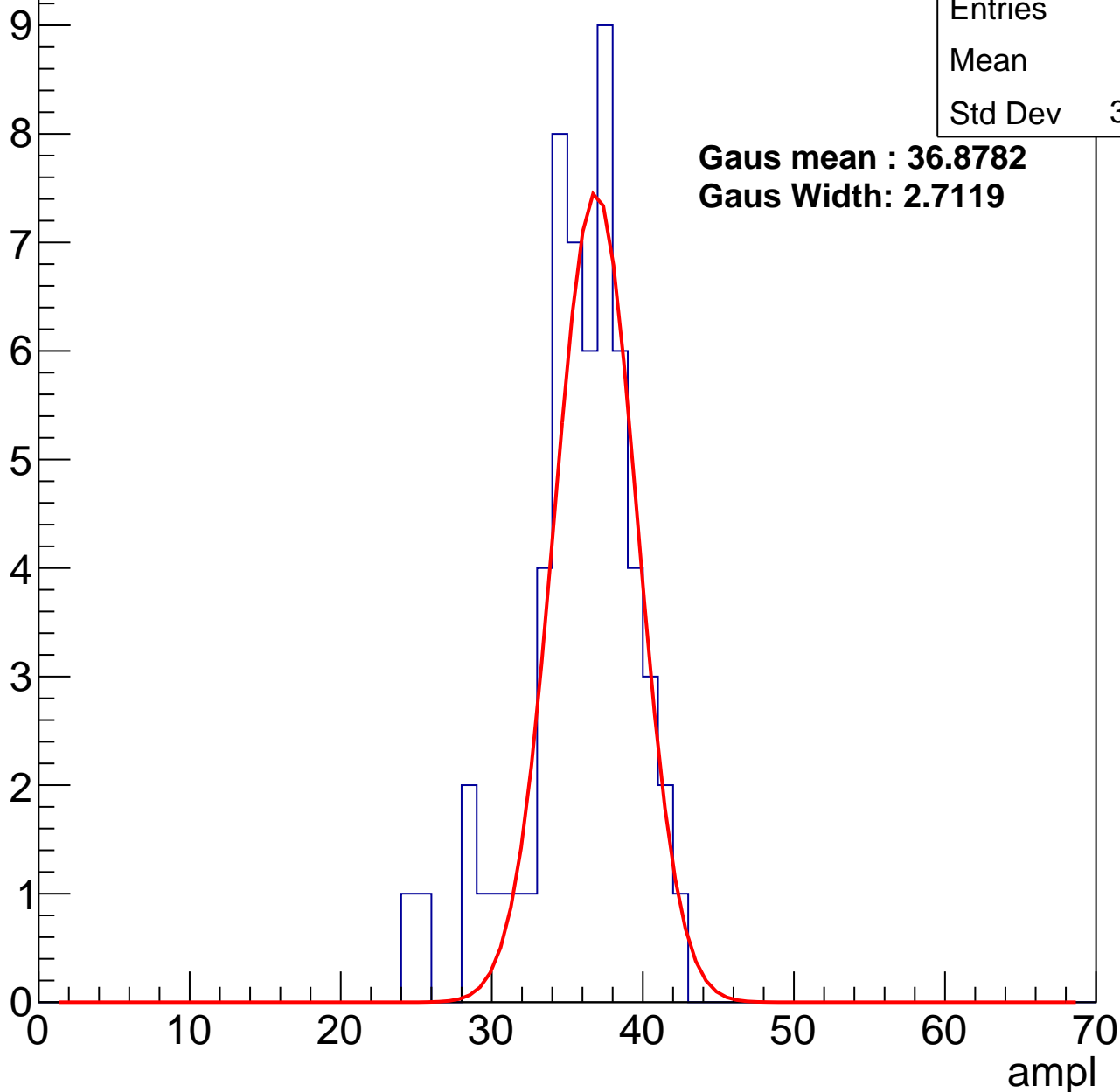
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	58
Mean	35.4
Std Dev	3.657

**Gaus mean : 36.8782**

**Gaus Width: 2.7119**



# B1L102S, U12-ch6, adc2

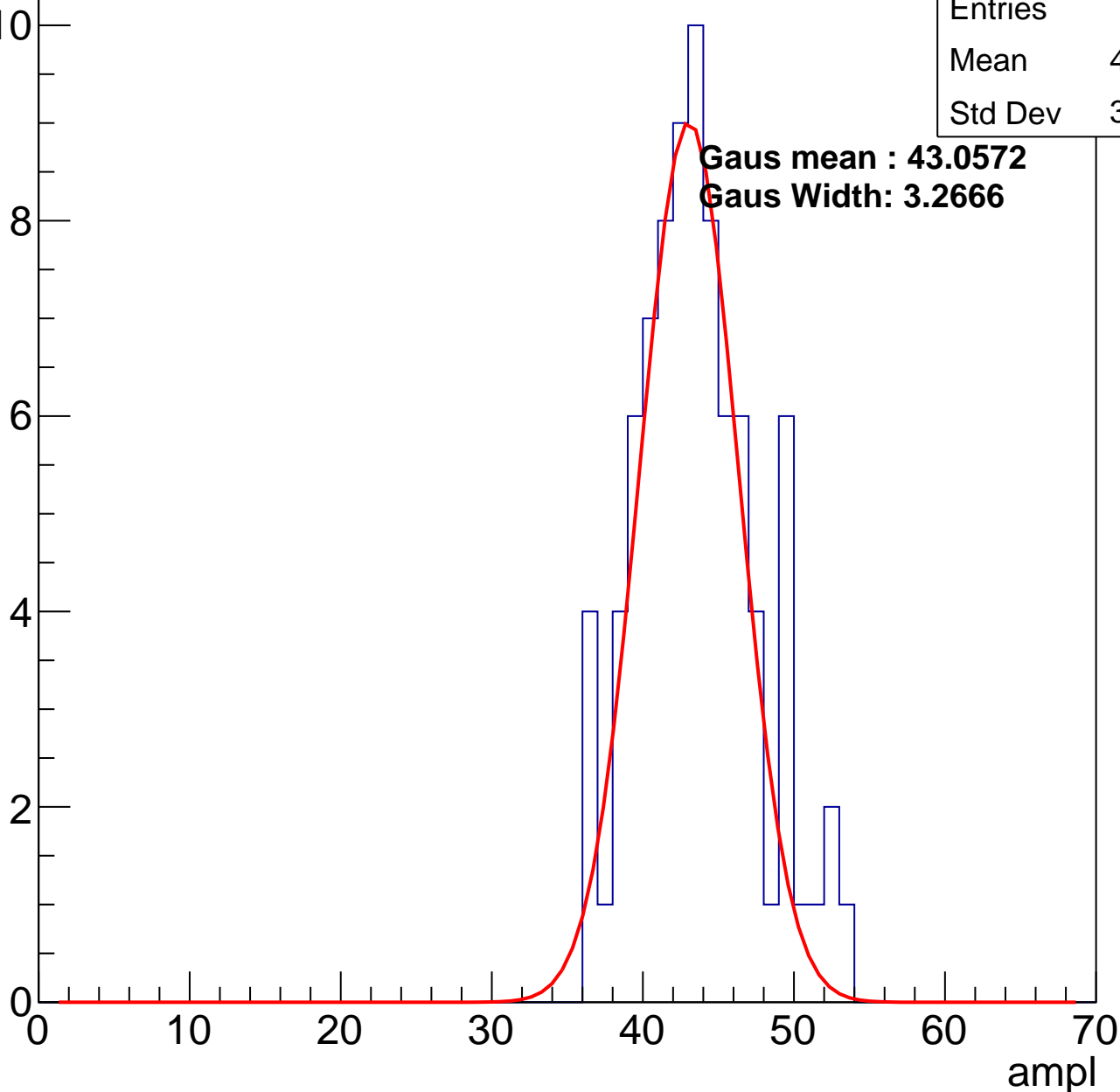
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	85
Mean	43.16
Std Dev	3.904

**Gaus mean : 43.0572**

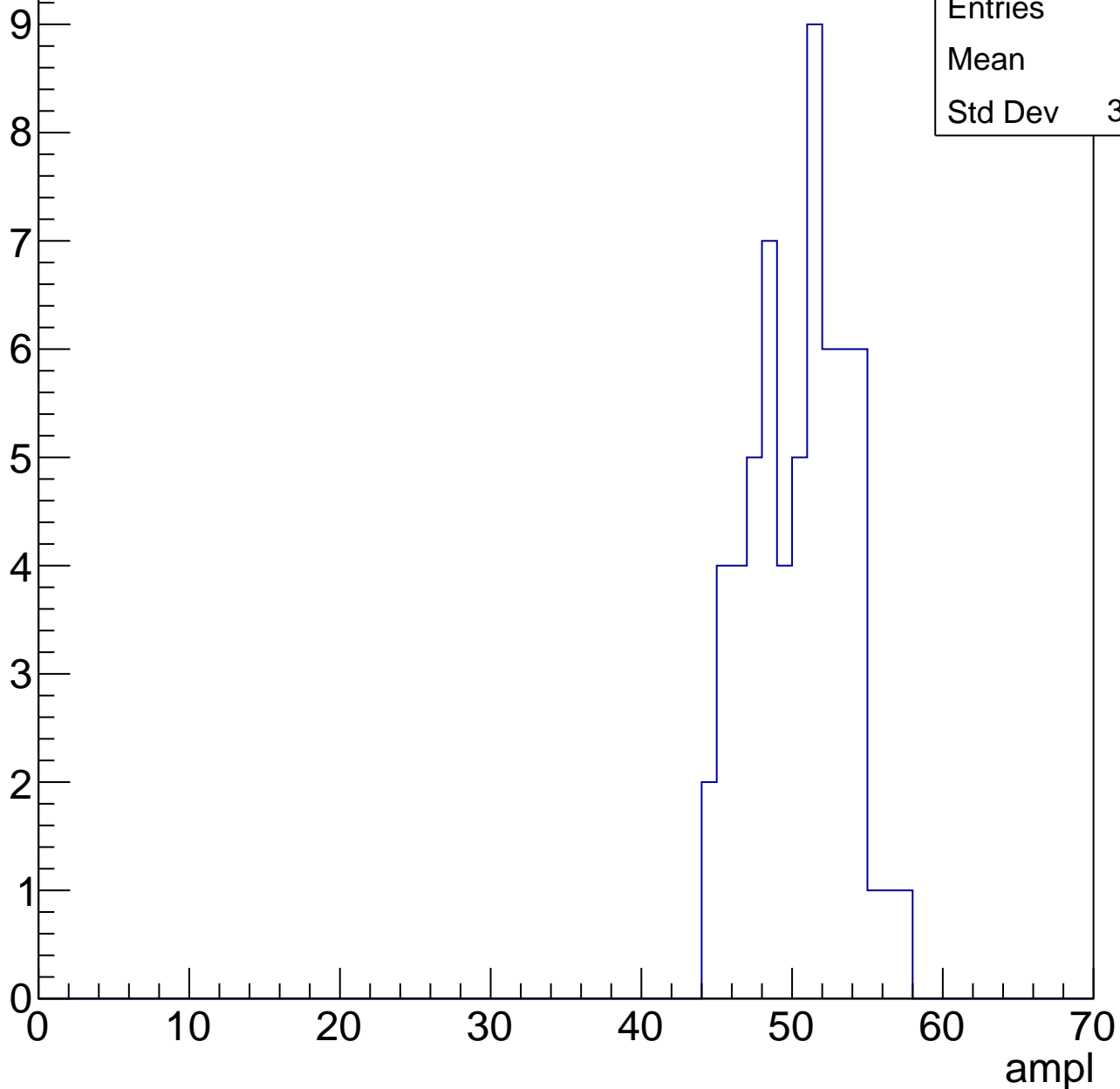
**Gaus Width: 3.2666**



# B1L102S, U12-ch6, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

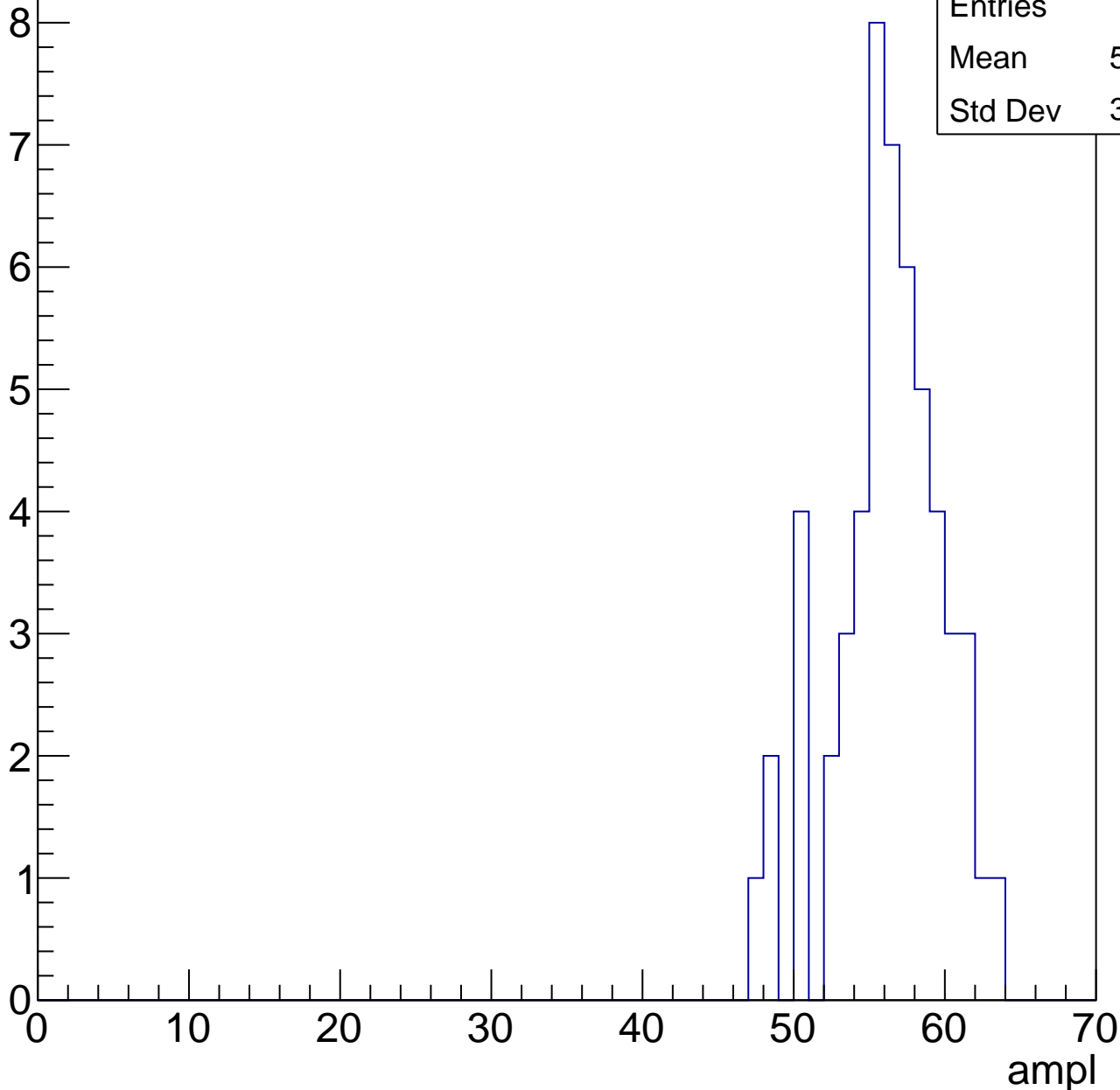


# B1L102S, U12-ch6, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	54
Mean	55.74
Std Dev	3.607

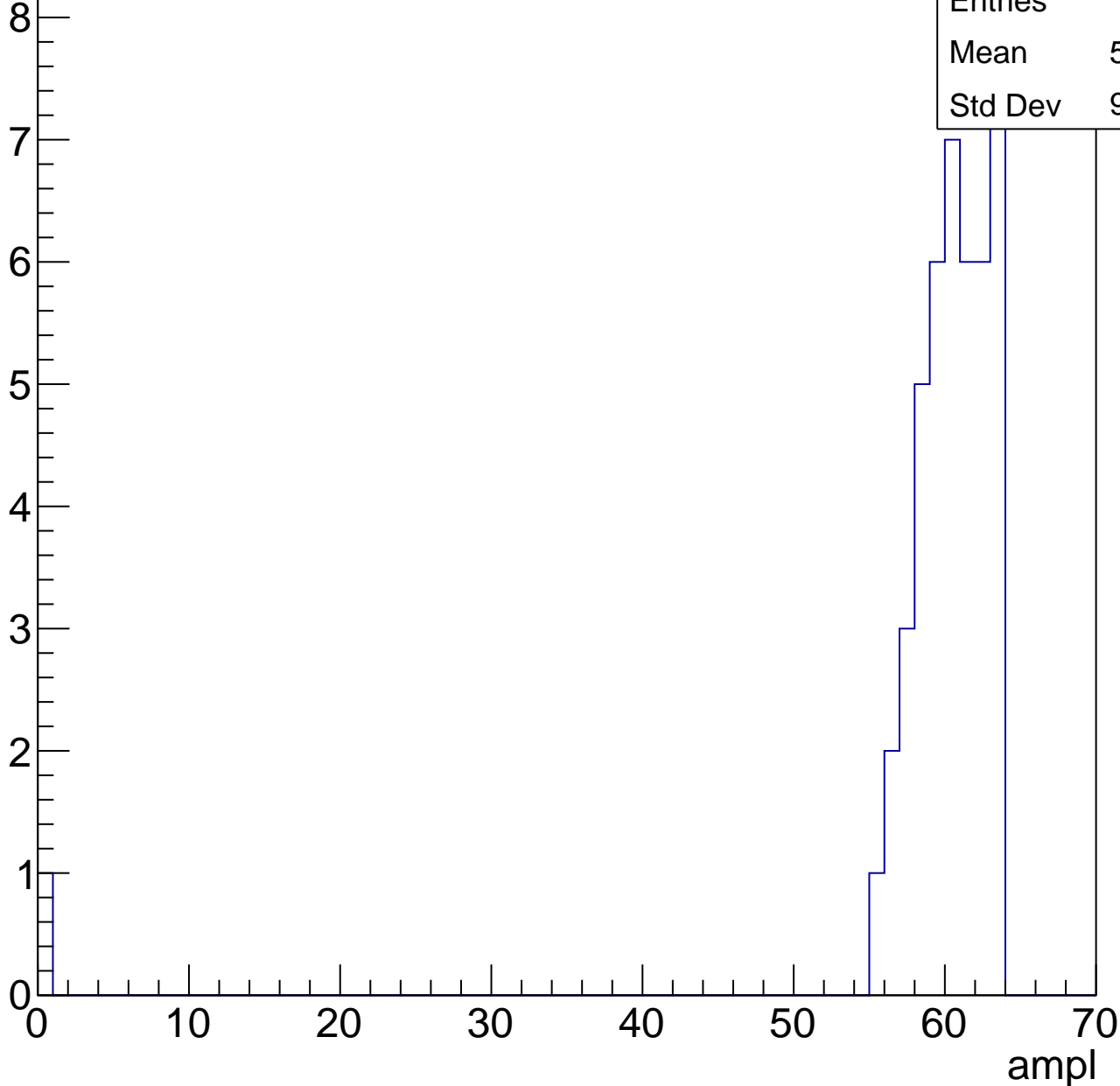


# B1L102S, U12-ch6, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

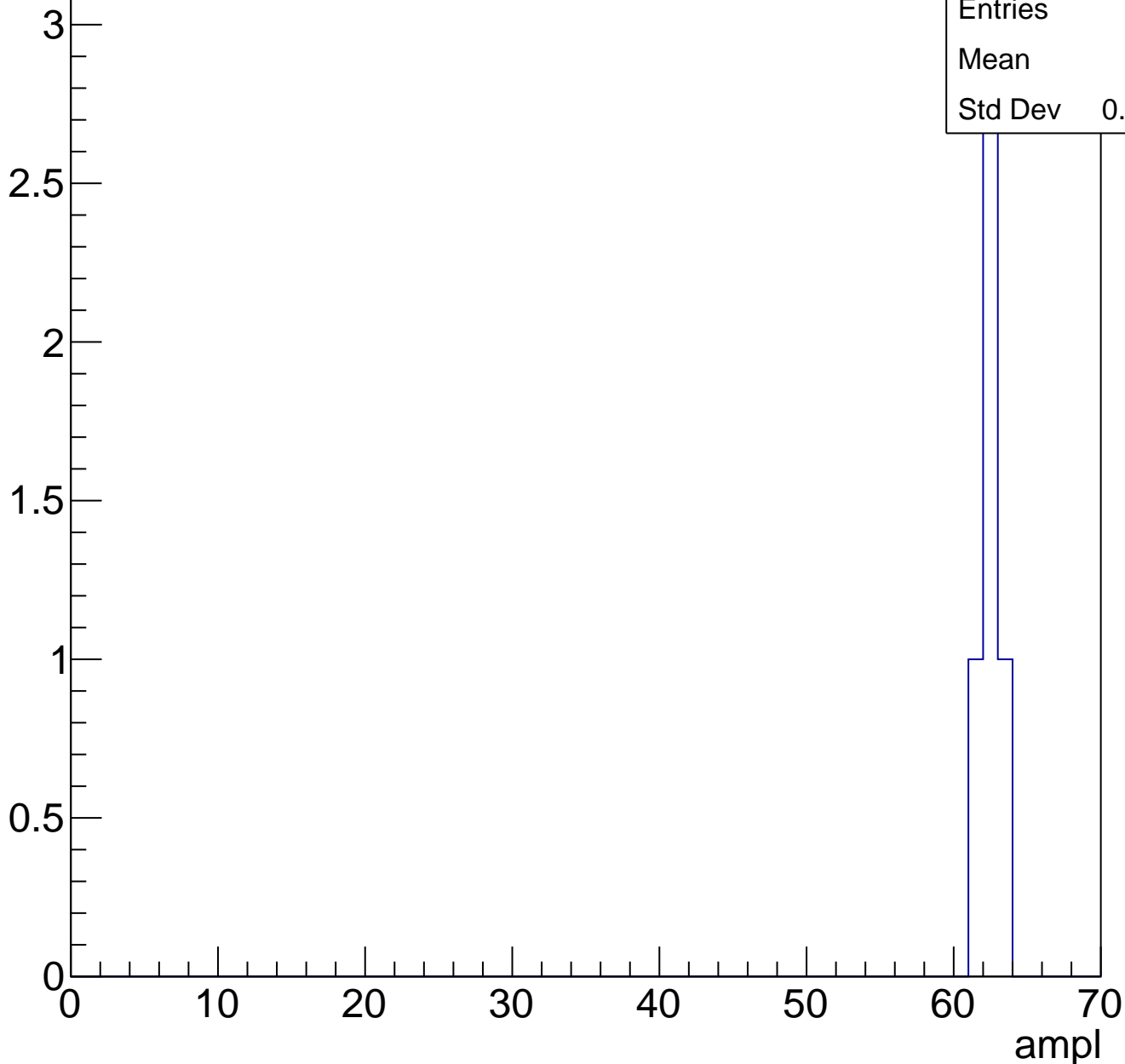
Entries	45
Mean	58.76
Std Dev	9.119



# B1L102S, U12-ch6, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U12-ch6, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U12-ch7, adc0

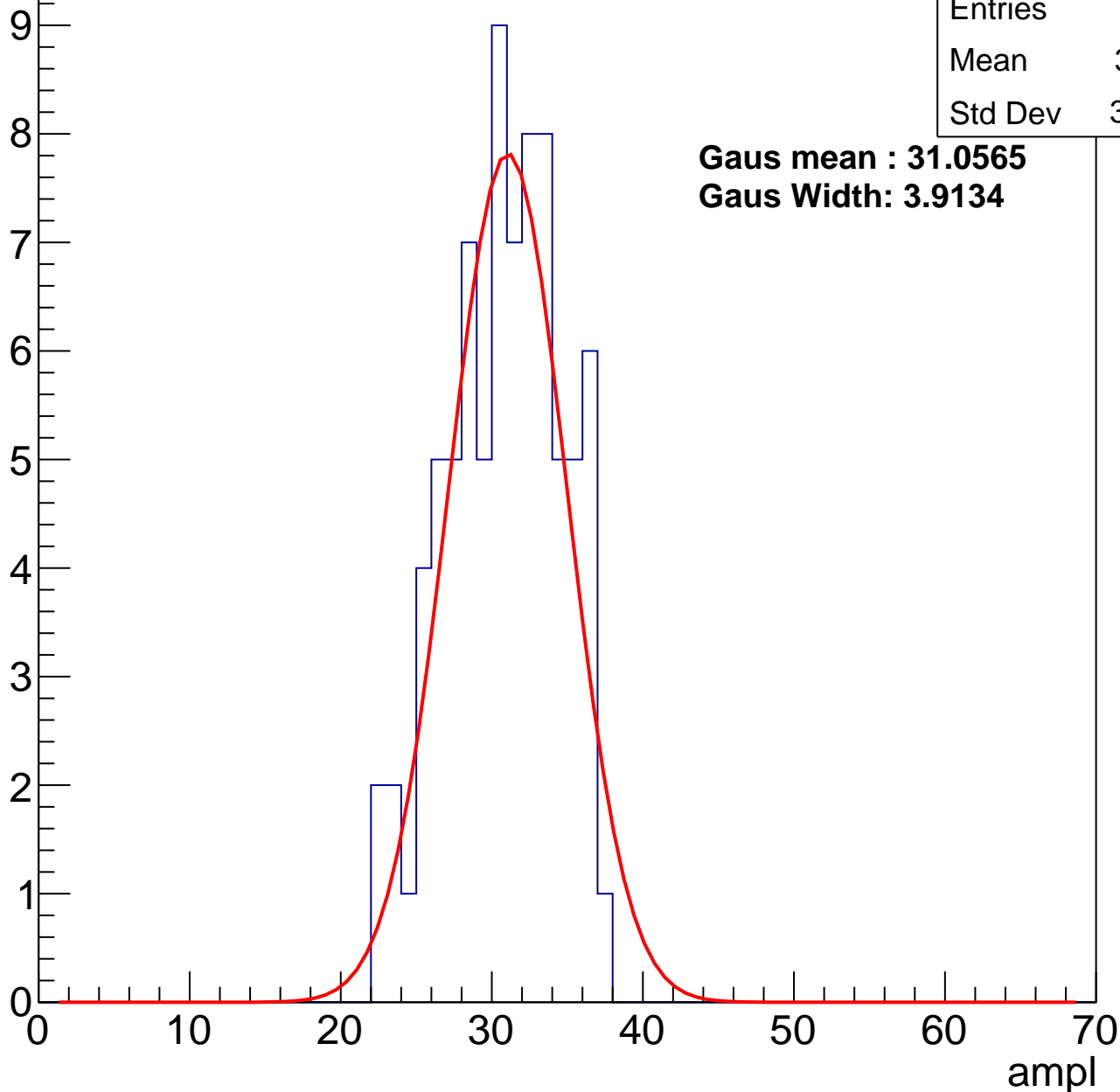
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	80
Mean	30.31
Std Dev	3.697

**Gaus mean : 31.0565**

**Gaus Width: 3.9134**



# B1L102S, U12-ch7, adc1

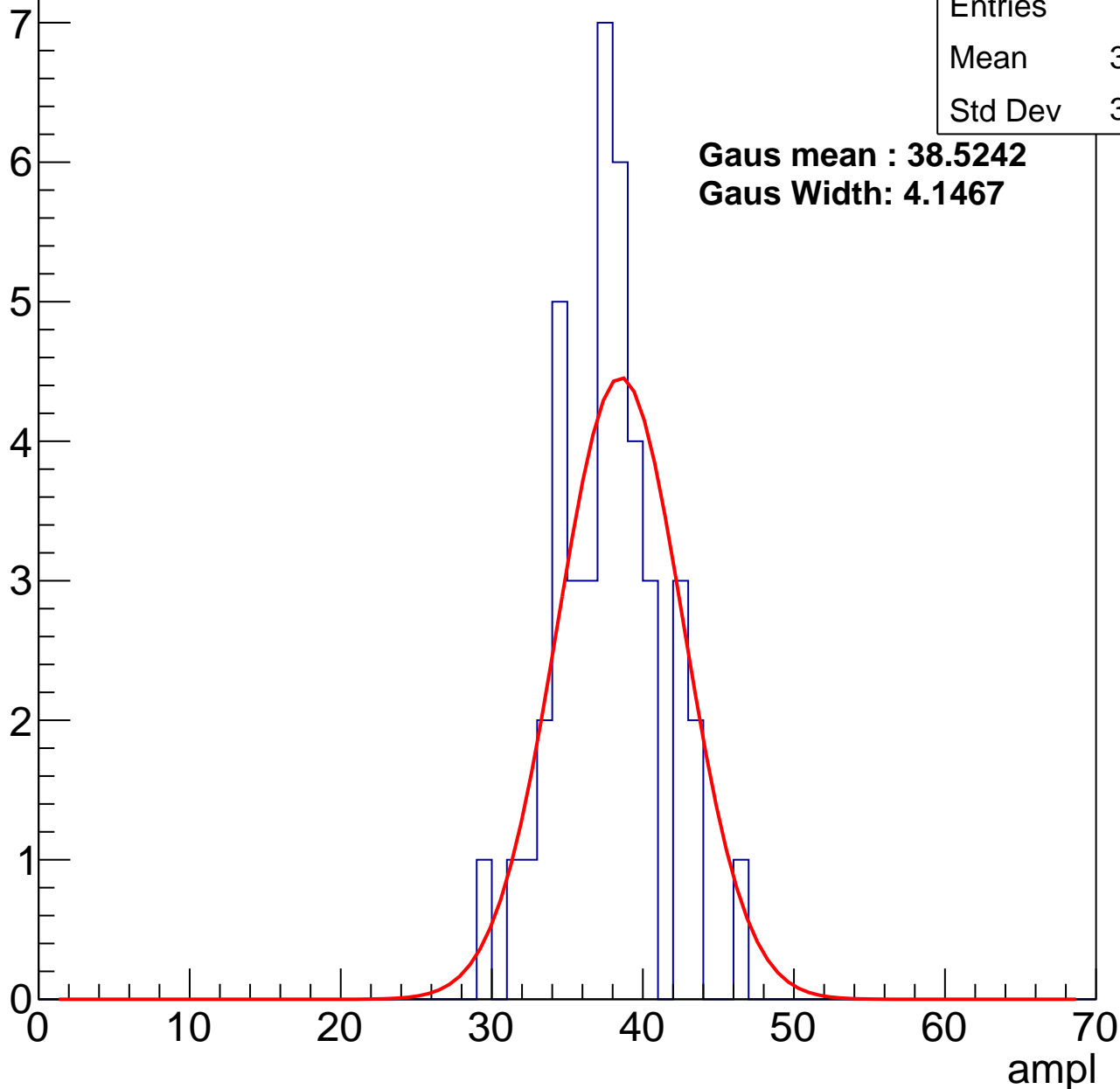
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	42
Mean	37.19
Std Dev	3.424

**Gaus mean : 38.5242**

**Gaus Width: 4.1467**



# B1L102S, U12-ch7, adc2

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	84
Mean	42.82
Std Dev	3.983

**Gaus mean : 43.3568**

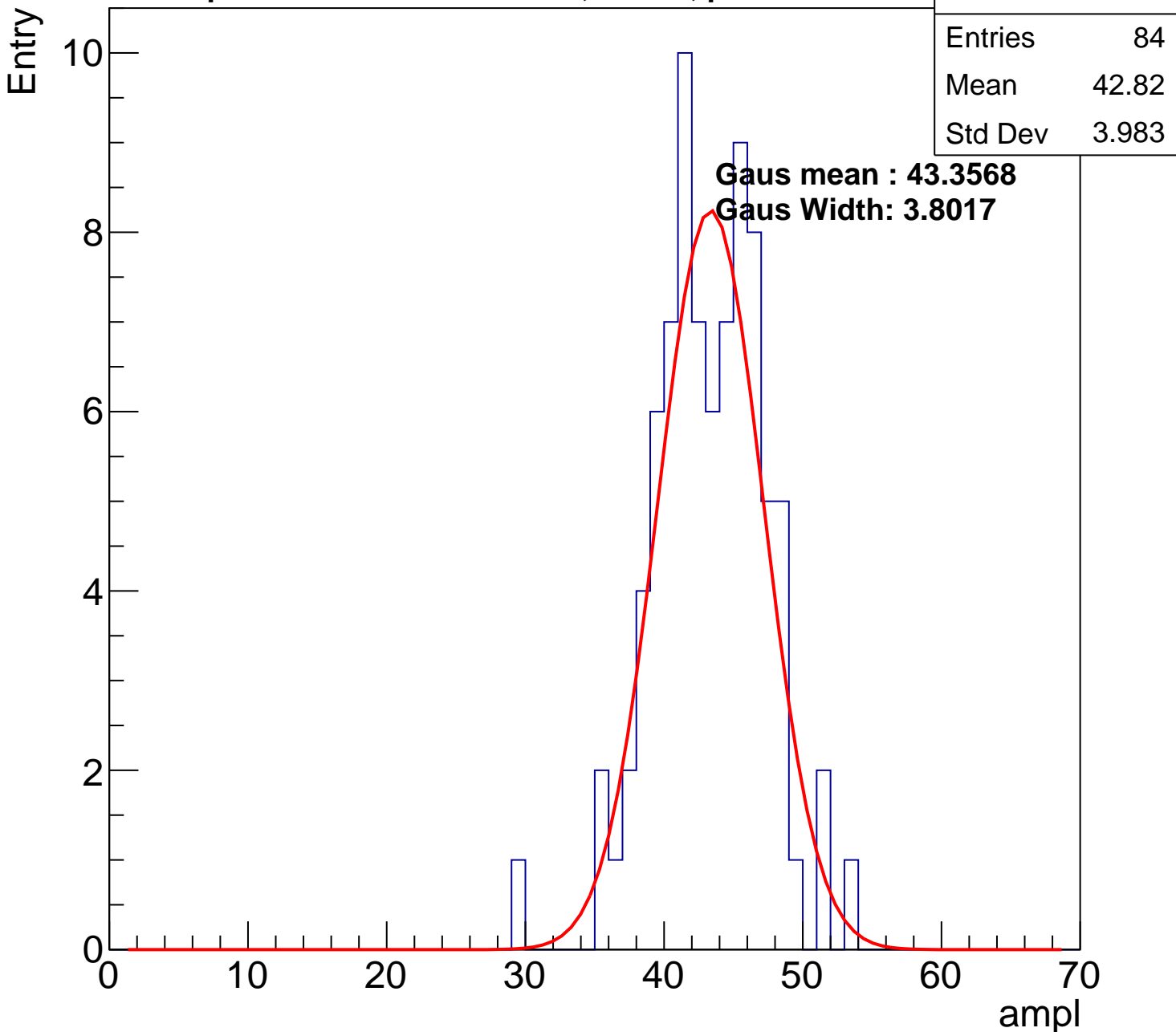
**Gaus Width: 3.8017**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

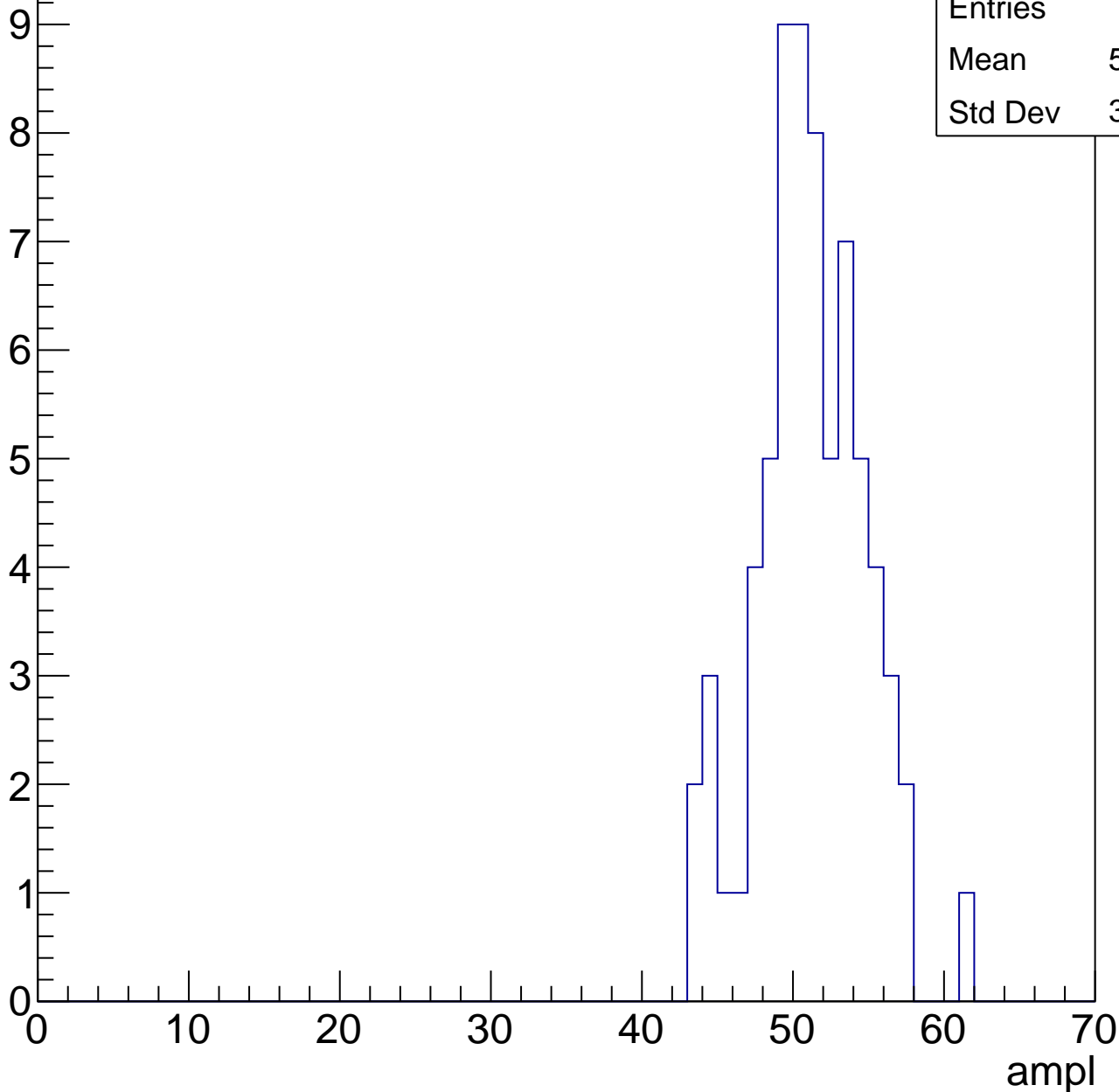


# B1L102S, U12-ch7, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	50.72
Std Dev	3.559

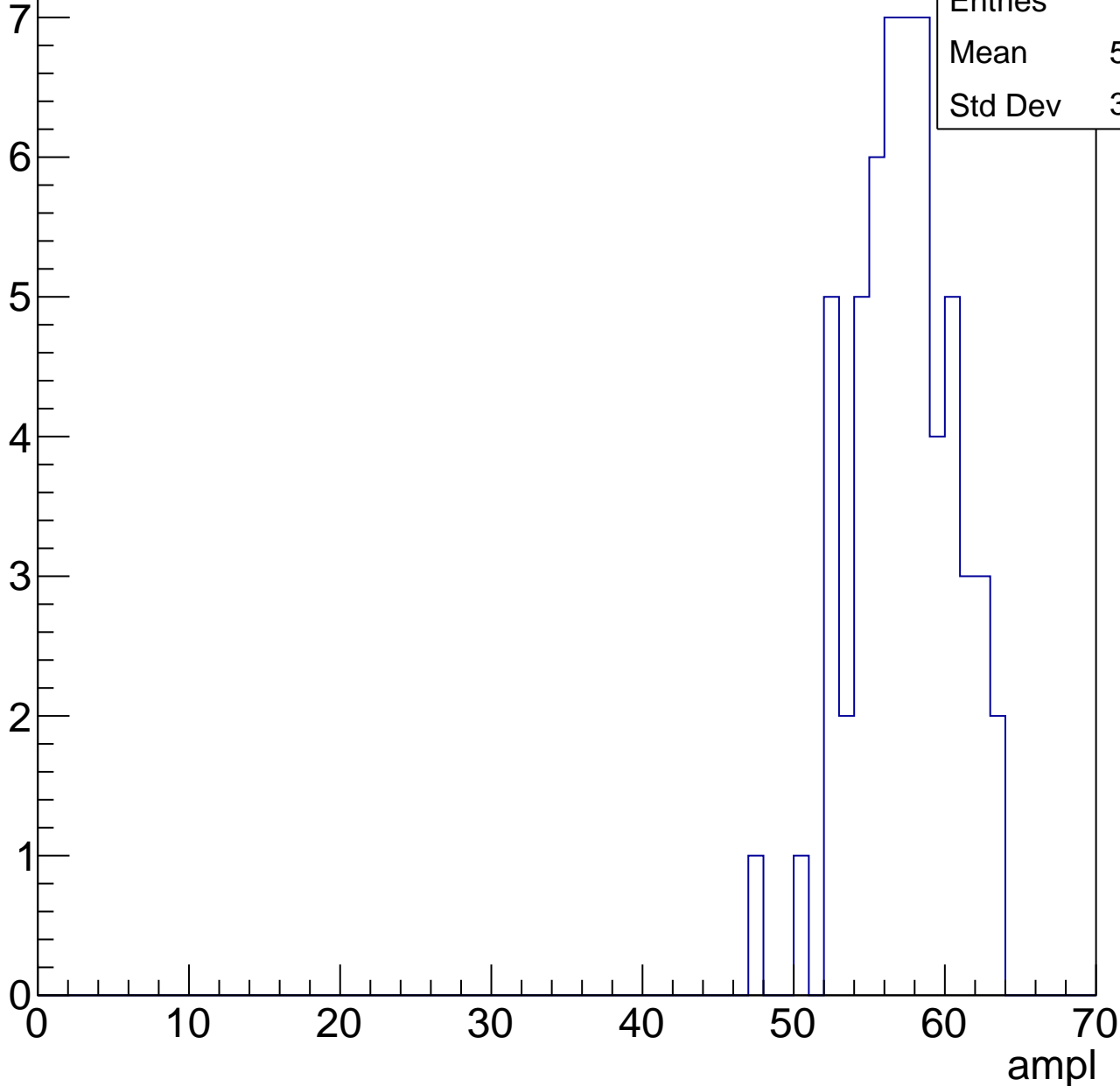


# B1L102S, U12-ch7, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	58
Mean	56.74
Std Dev	3.325

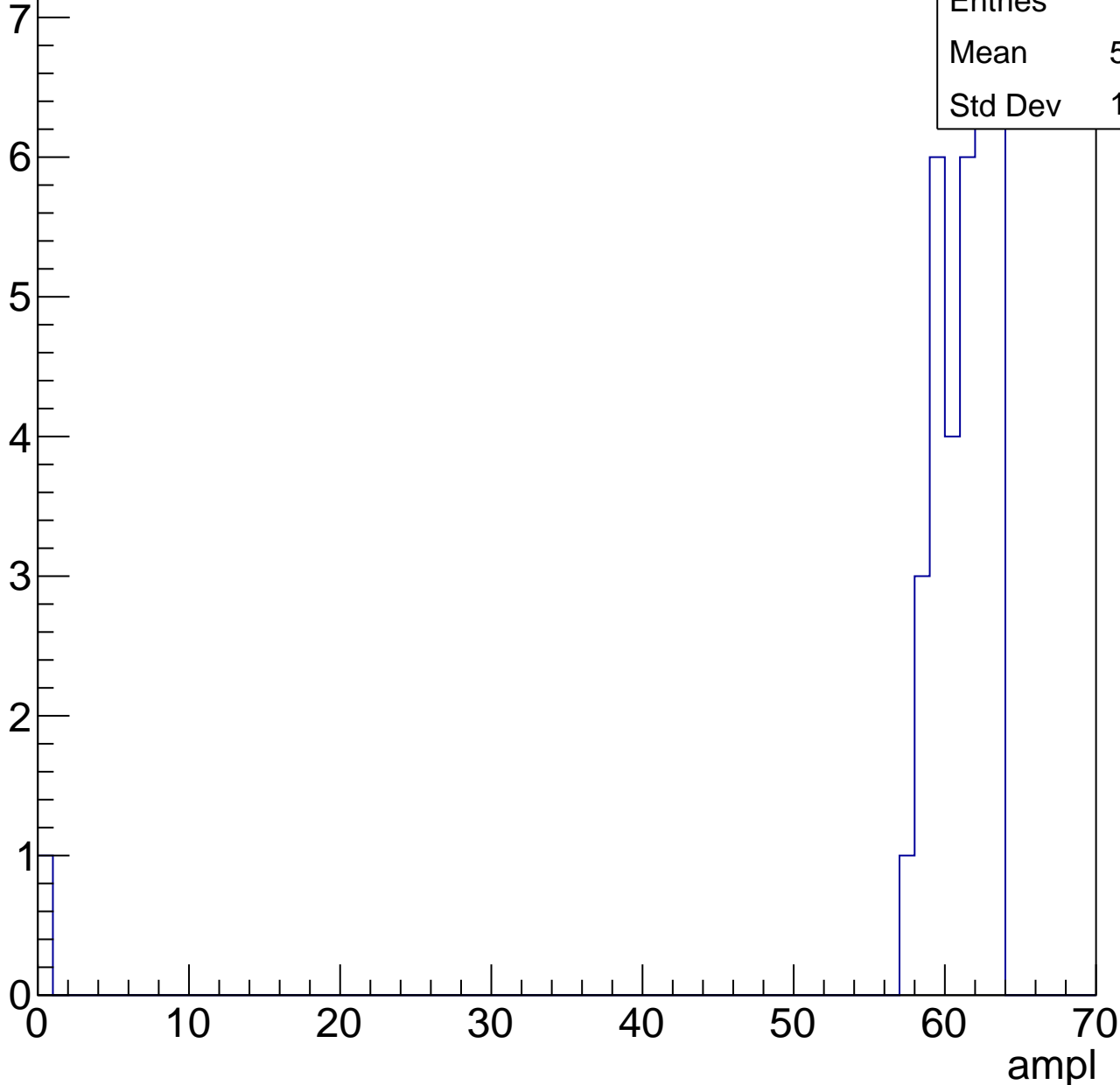


# B1L102S, U12-ch7, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	35
Mean	59.03
Std Dev	10.27



# B1L102S, U12-ch7, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U12-ch7, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U12-ch8, adc0

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	57
Mean	30.56
Std Dev	2.908

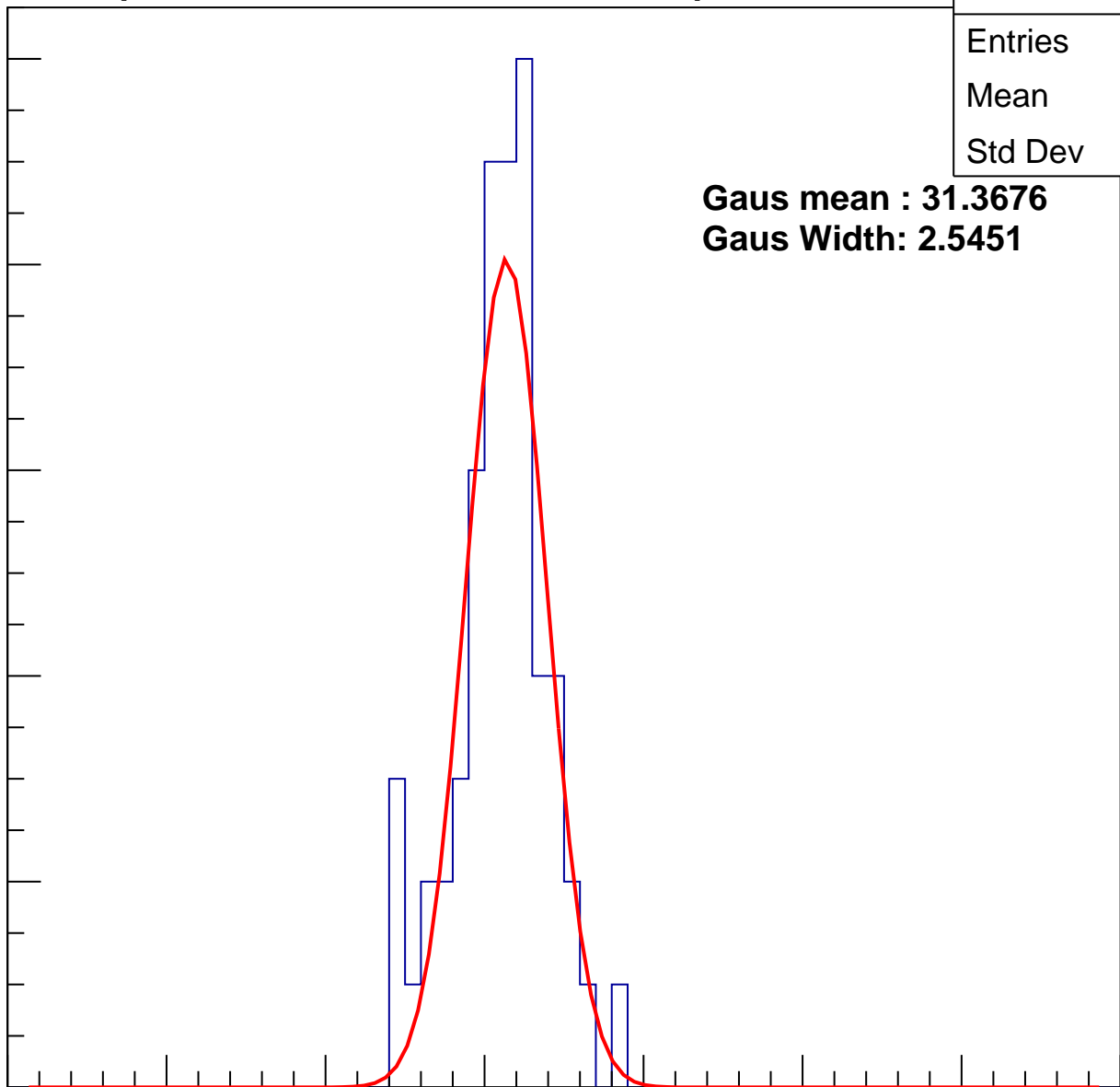
**Gaus mean : 31.3676**

**Gaus Width: 2.5451**

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L102S, U12-ch8, adc1

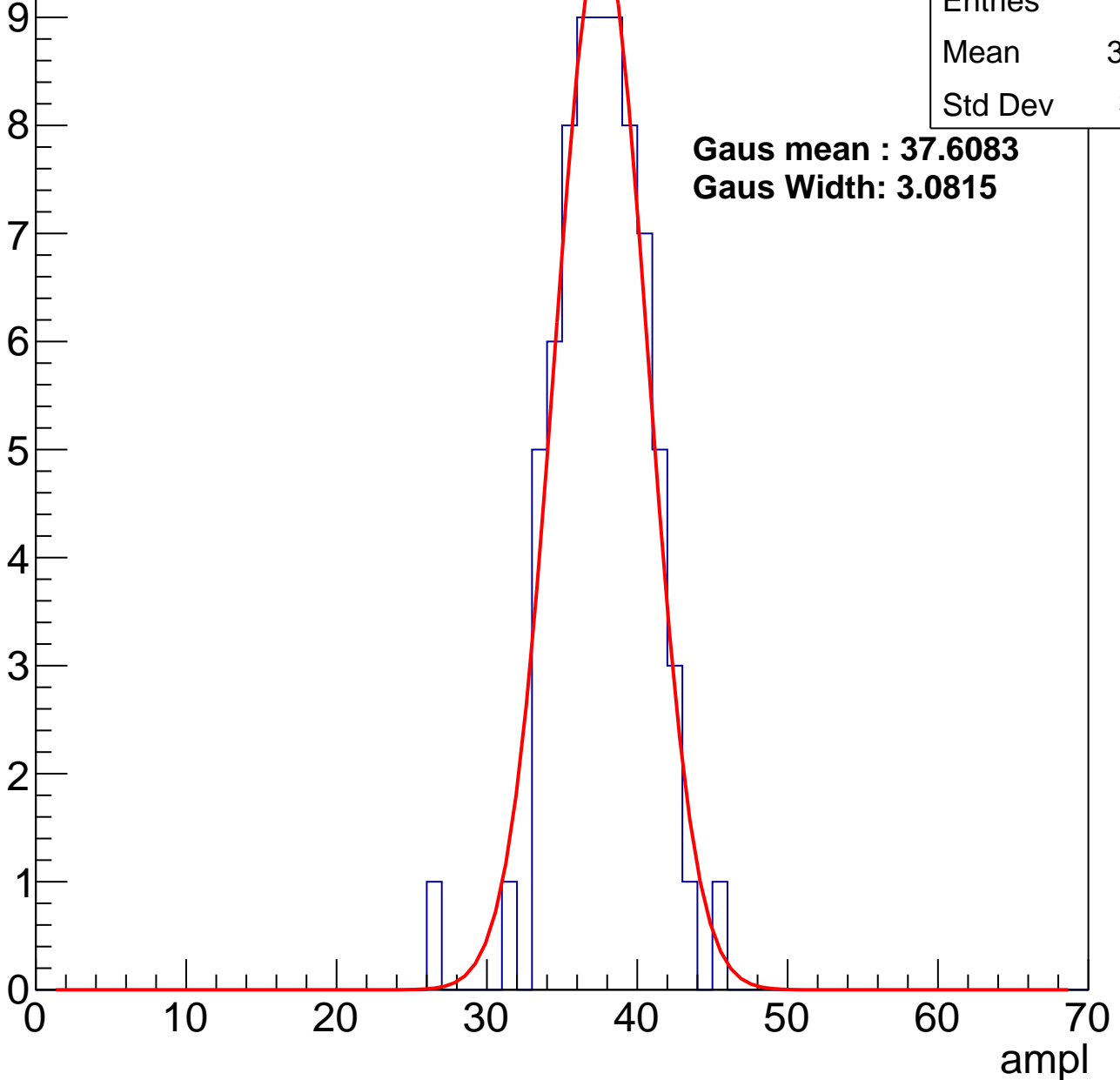
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	73
Mean	37.21
Std Dev	3.07

**Gaus mean : 37.6083**

**Gaus Width: 3.0815**



# B1L102S, U12-ch8, adc2

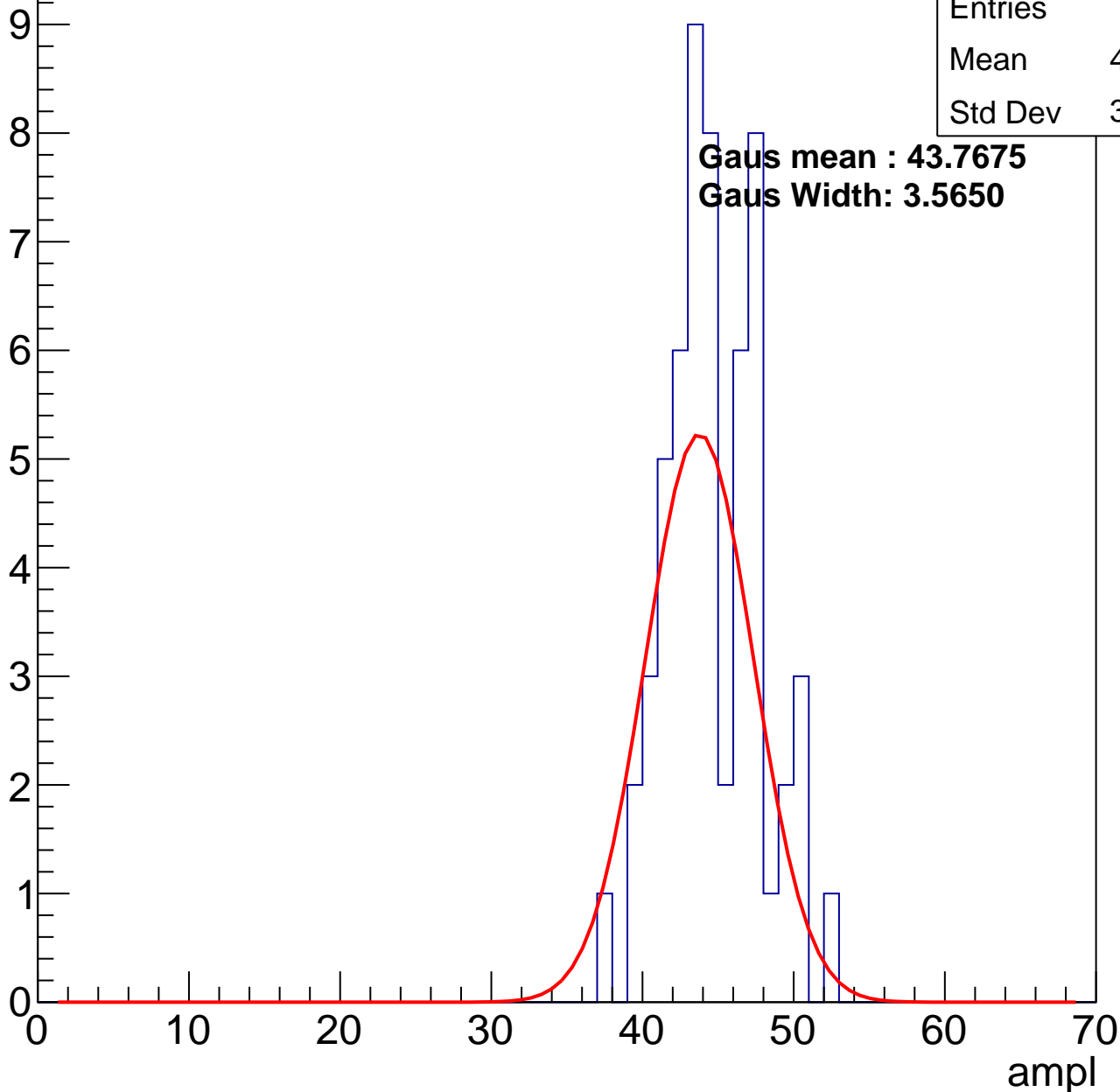
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	57
Mean	44.23
Std Dev	3.129

**Gaus mean : 43.7675**

**Gaus Width: 3.5650**

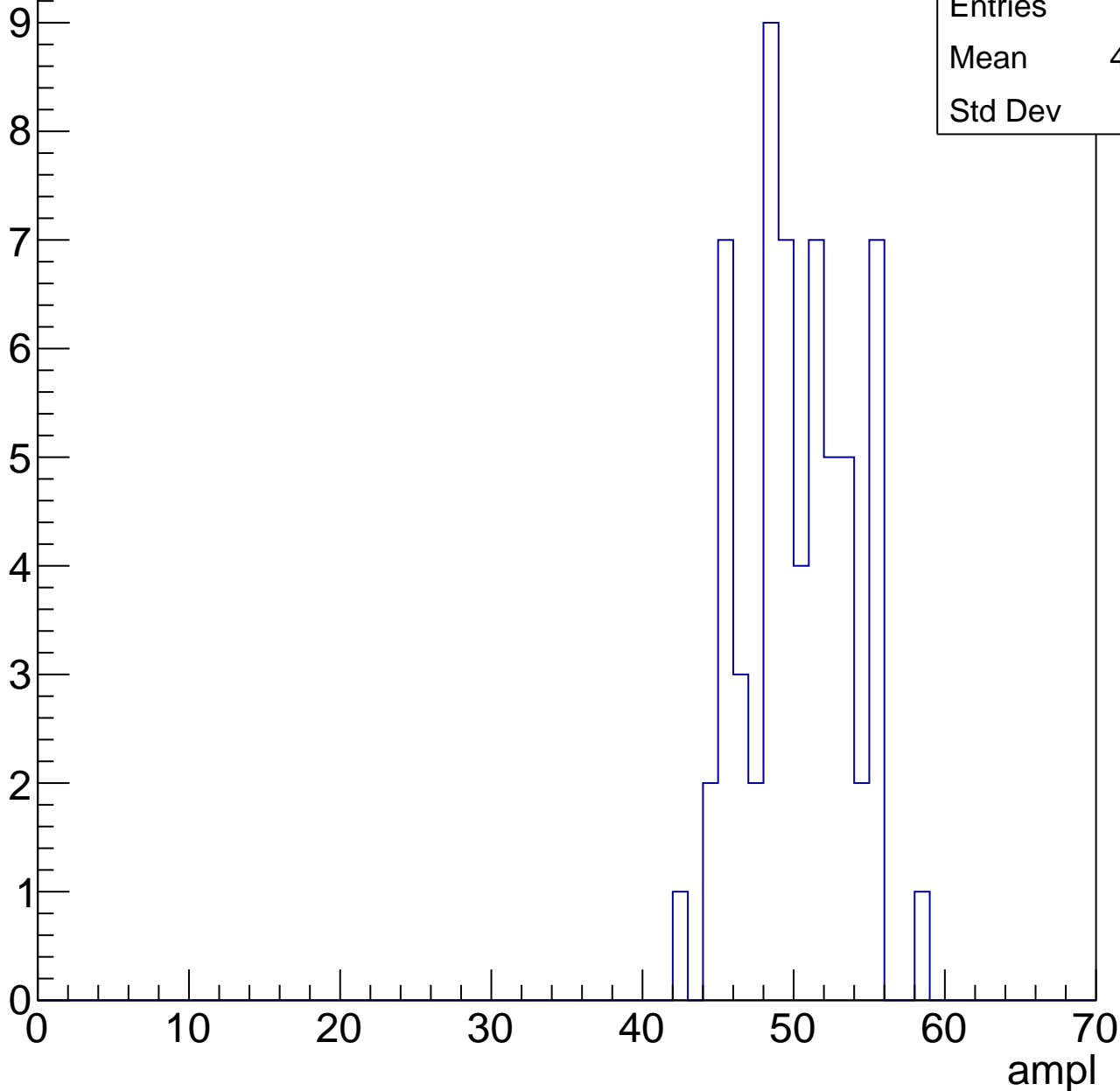


# B1L102S, U12-ch8, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	62
Mean	49.76
Std Dev	3.5



# B1L102S, U12-ch8, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

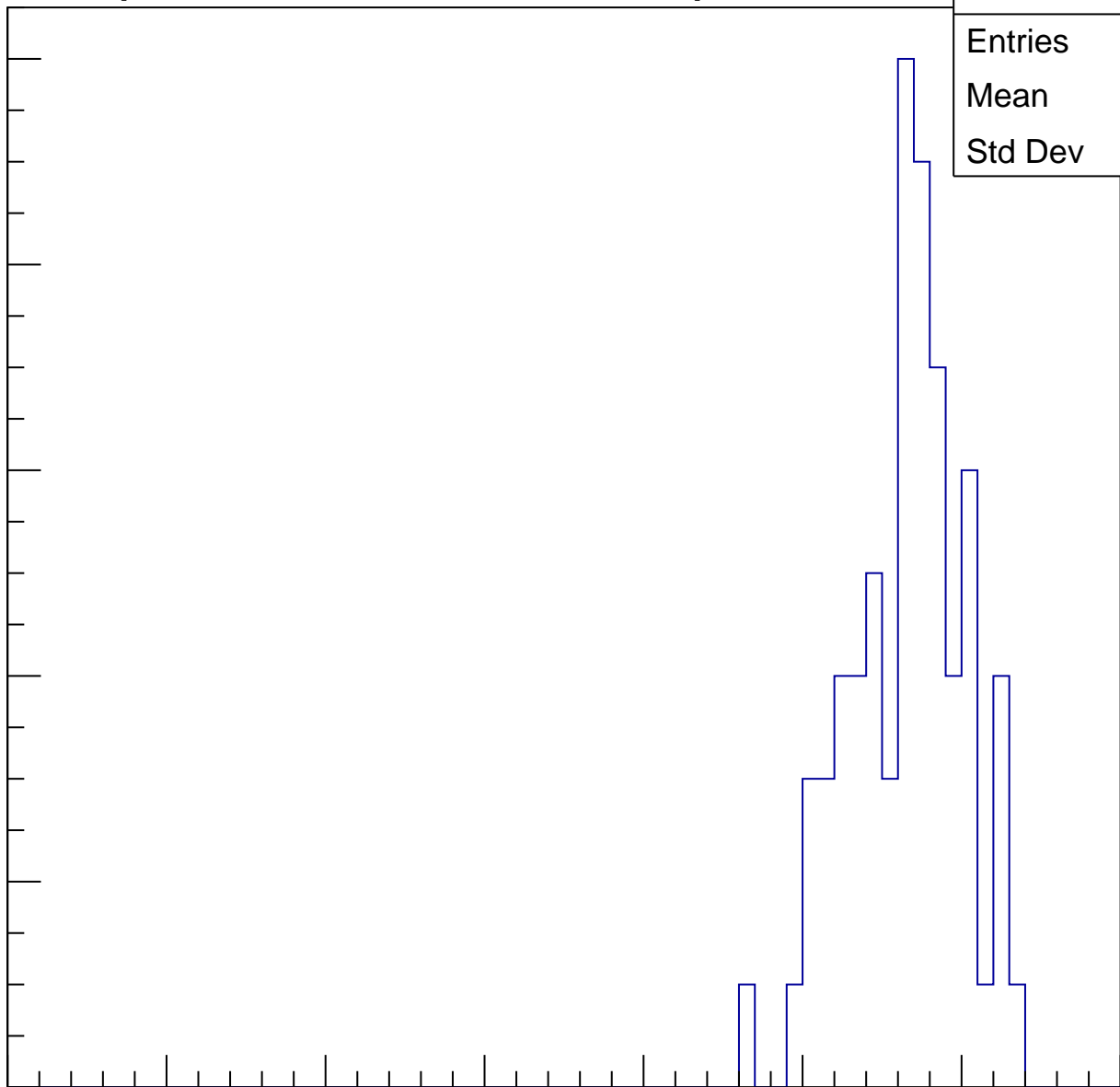
Entries	66
Mean	56.06
Std Dev	3.571

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

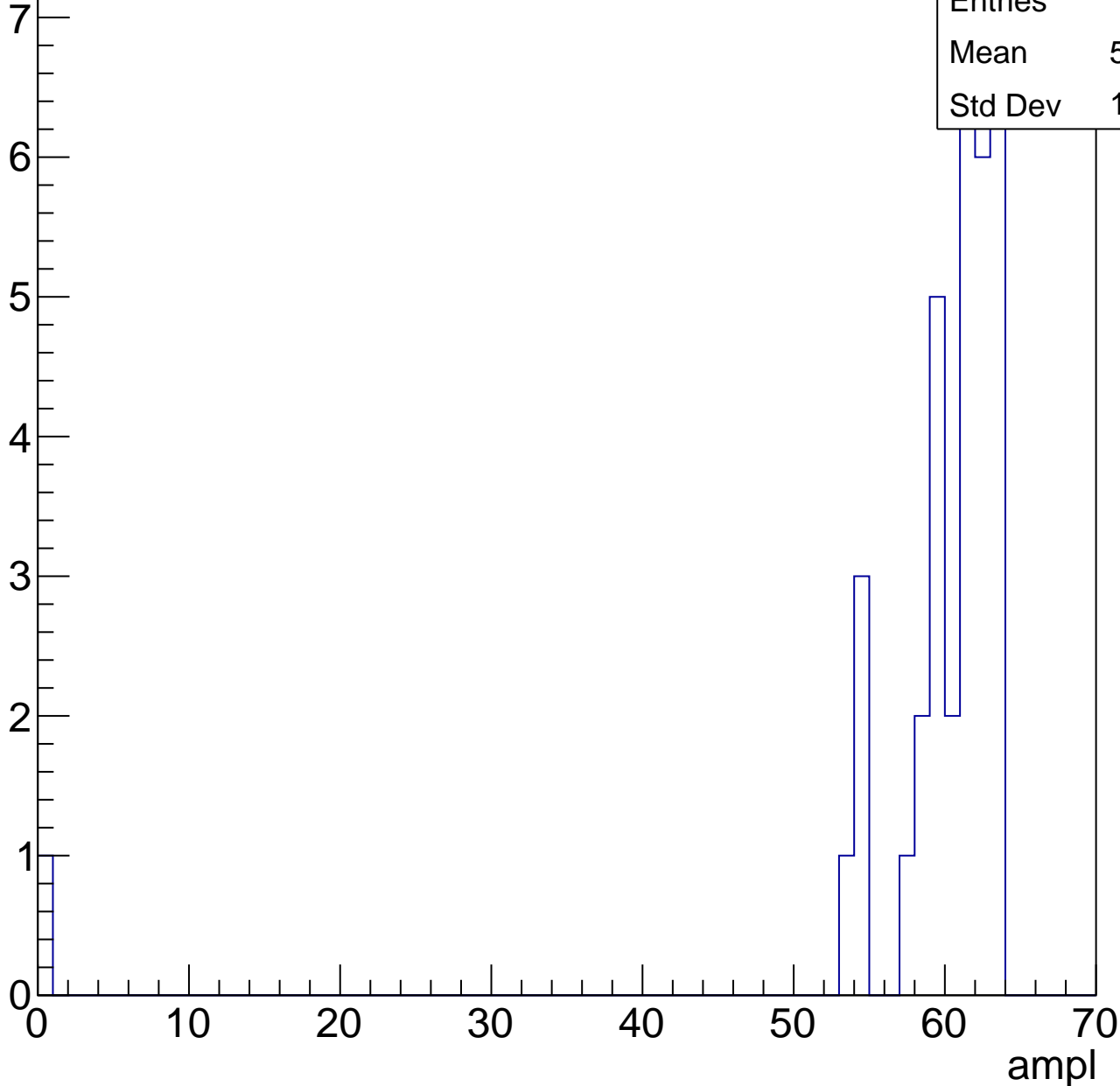


# B1L102S, U12-ch8, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	35
Mean	58.37
Std Dev	10.39



# B1L102S, U12-ch8, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	7
Mean	61
Std Dev	1.414

ampl

0 10 20 30 40 50 60 70



# B1L102S, U12-ch8, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U12-ch9, adc0

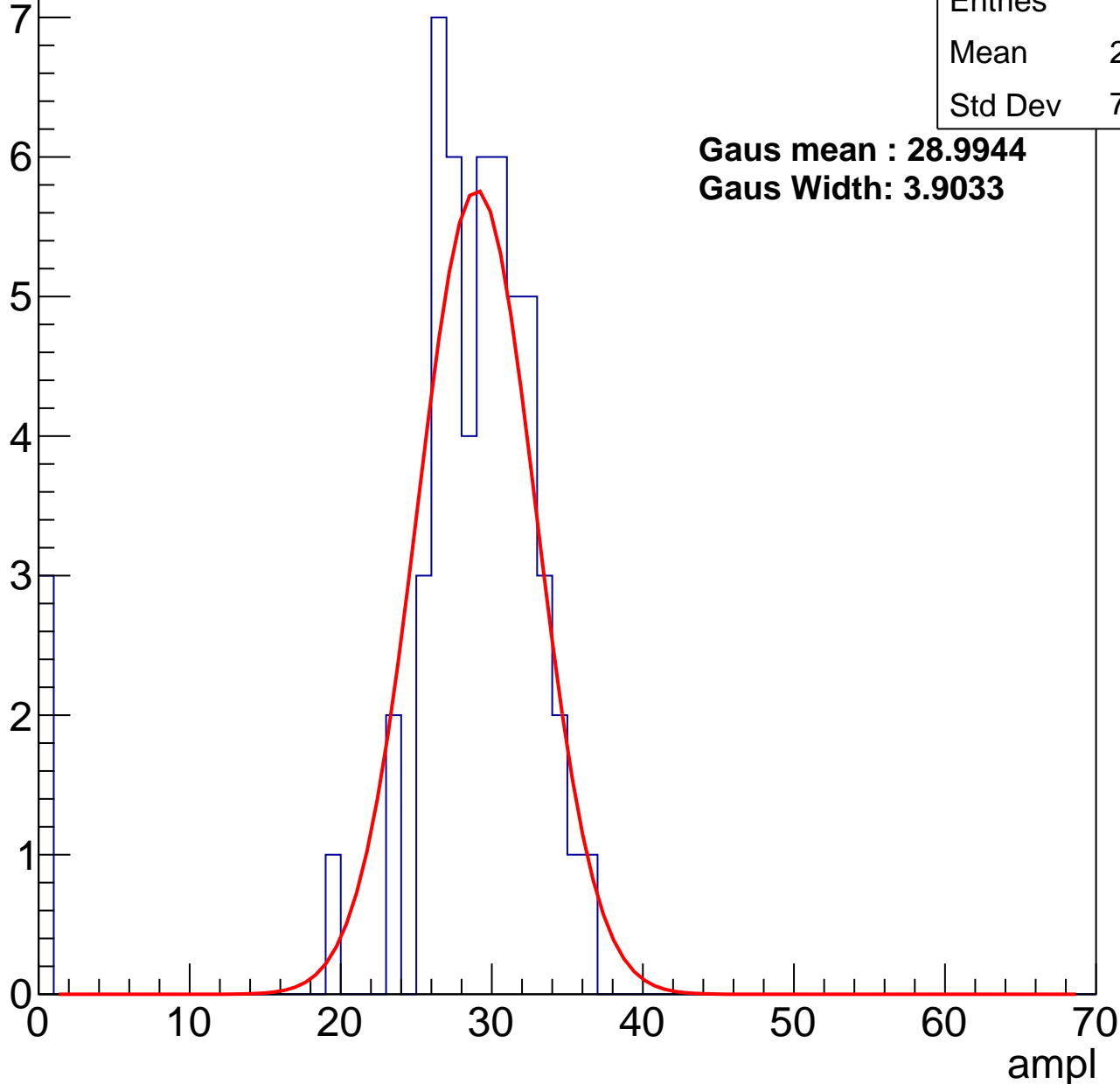
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	55
Mean	27.33
Std Dev	7.304

**Gaus mean : 28.9944**

**Gaus Width: 3.9033**



# B1L102S, U12-ch9, adc1

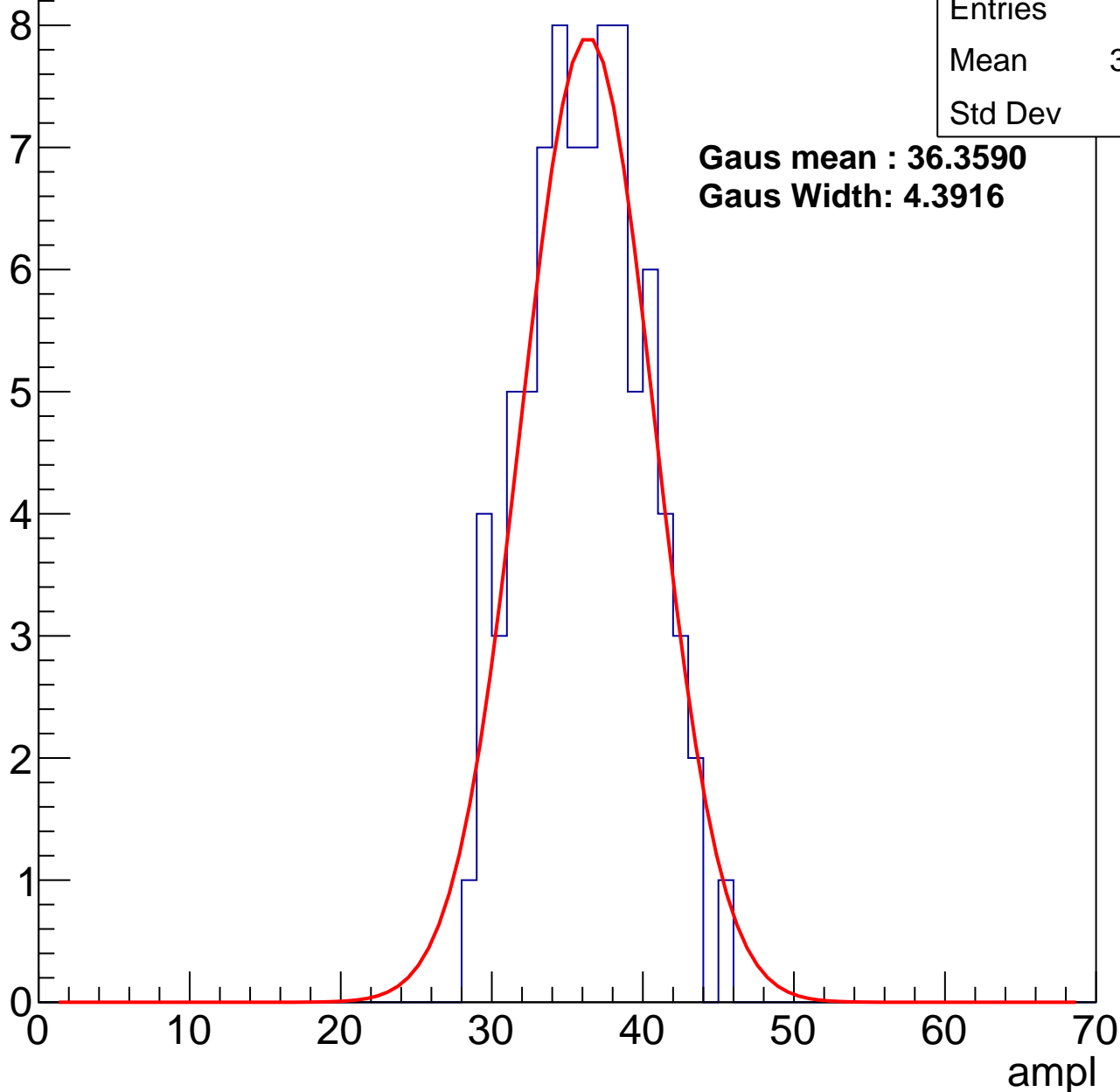
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	84
Mean	35.77
Std Dev	3.84

**Gaus mean : 36.3590**

**Gaus Width: 4.3916**



# B1L102S, U12-ch9, adc2

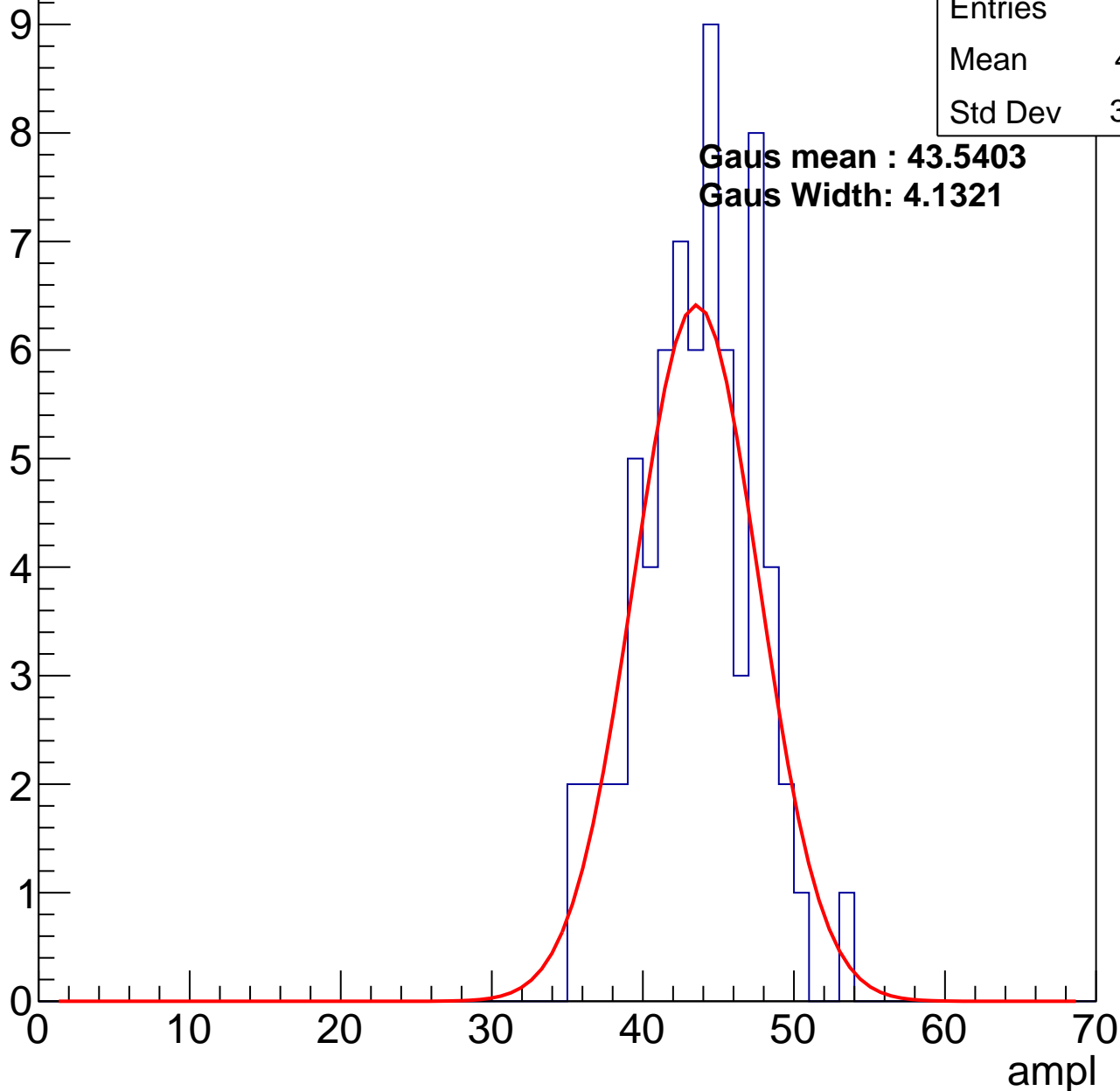
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	70
Mean	43.11
Std Dev	3.785

**Gaus mean : 43.5403**

**Gaus Width: 4.1321**

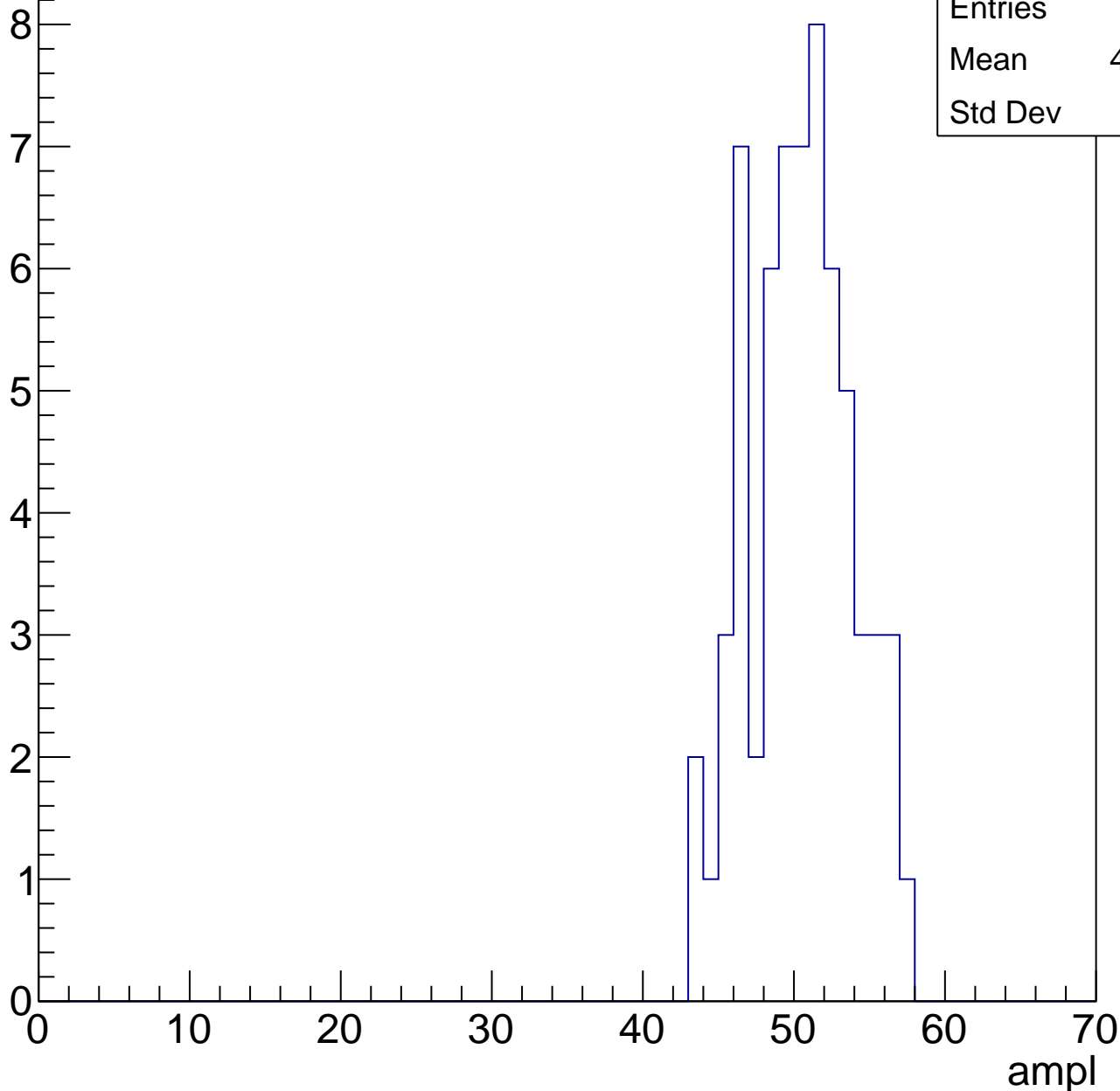


# B1L102S, U12-ch9, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	49.98
Std Dev	3.37

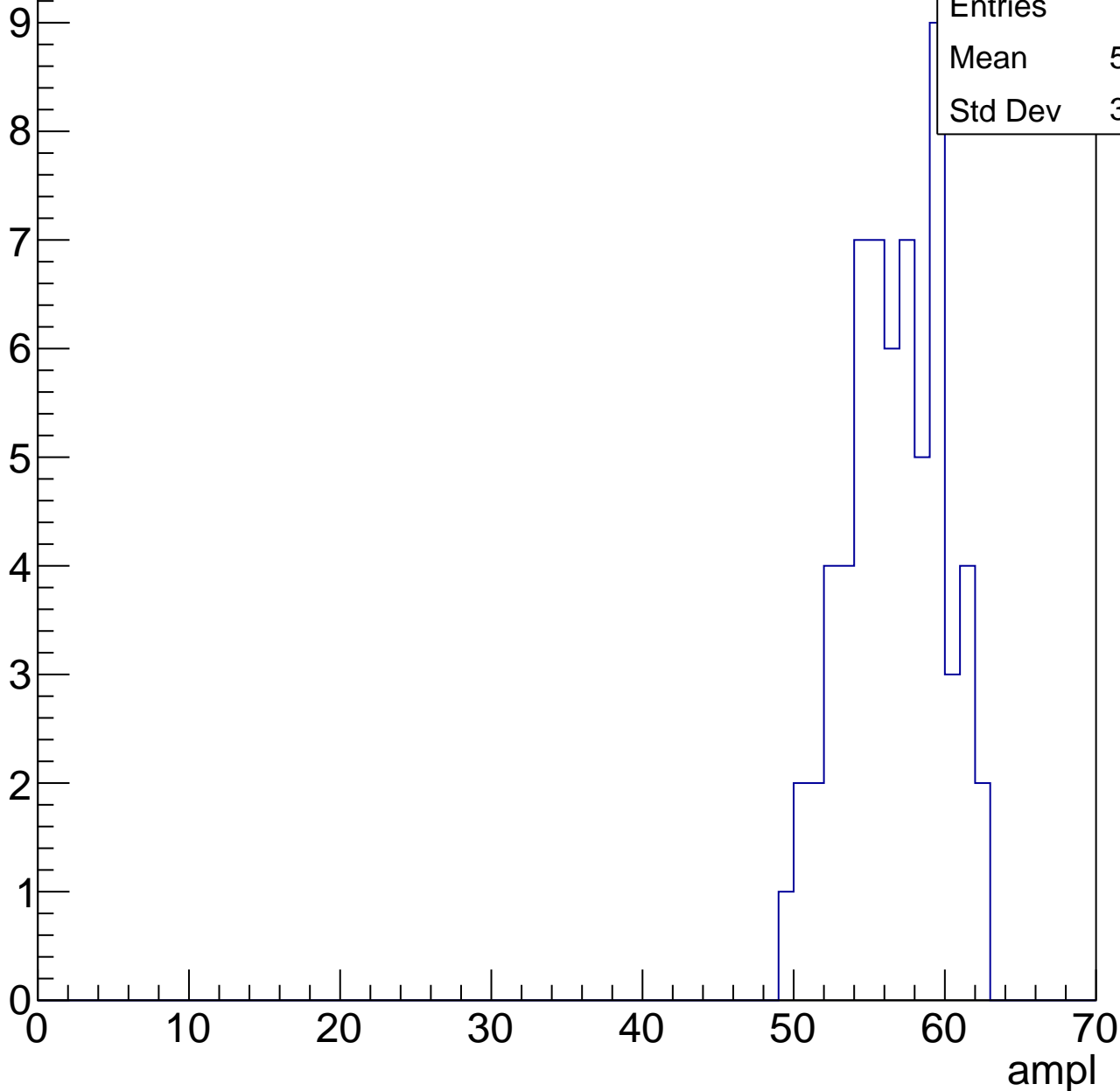


# B1L102S, U12-ch9, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	63
Mean	56.16
Std Dev	3.168

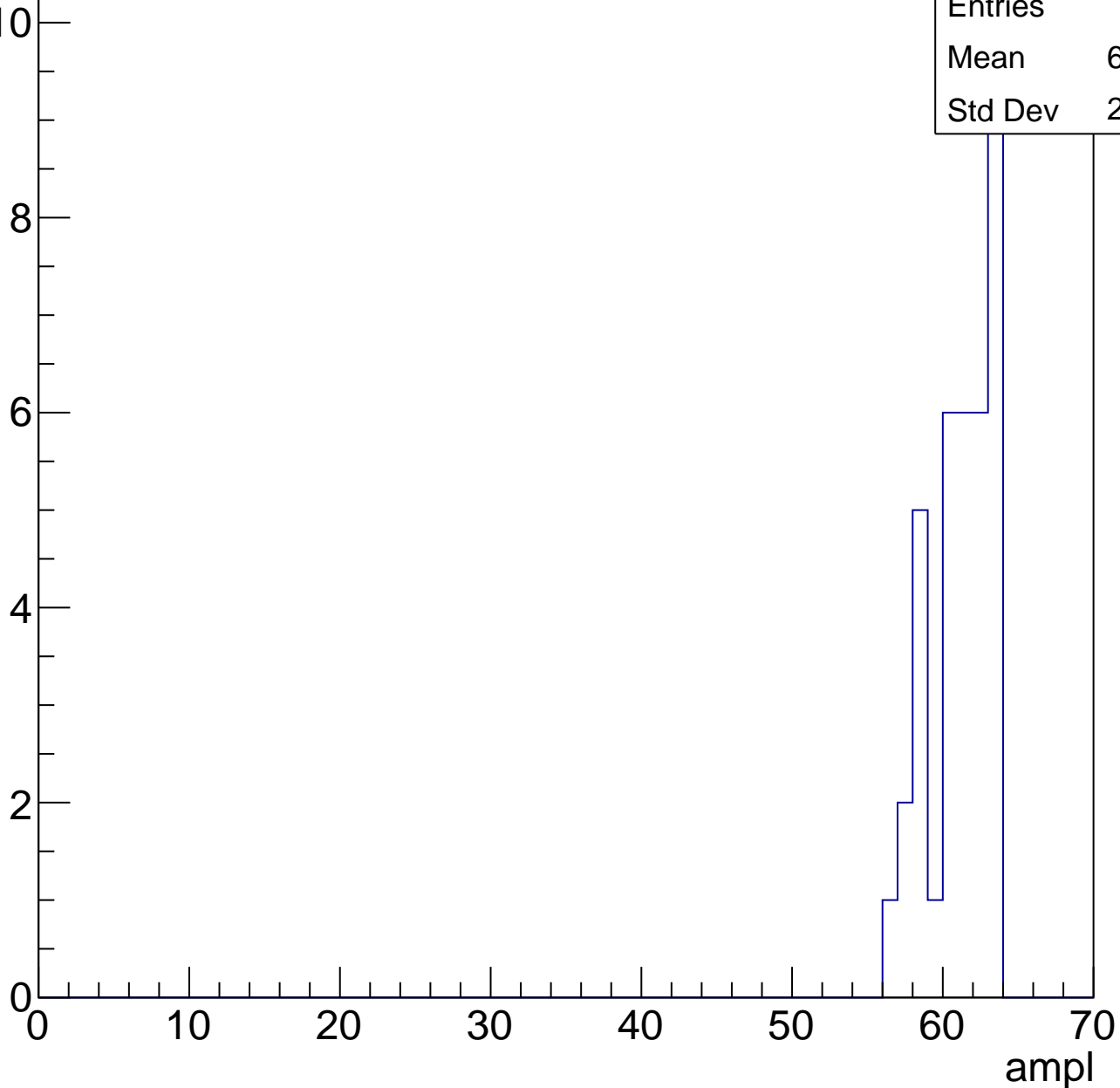


# B1L102S, U12-ch9, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

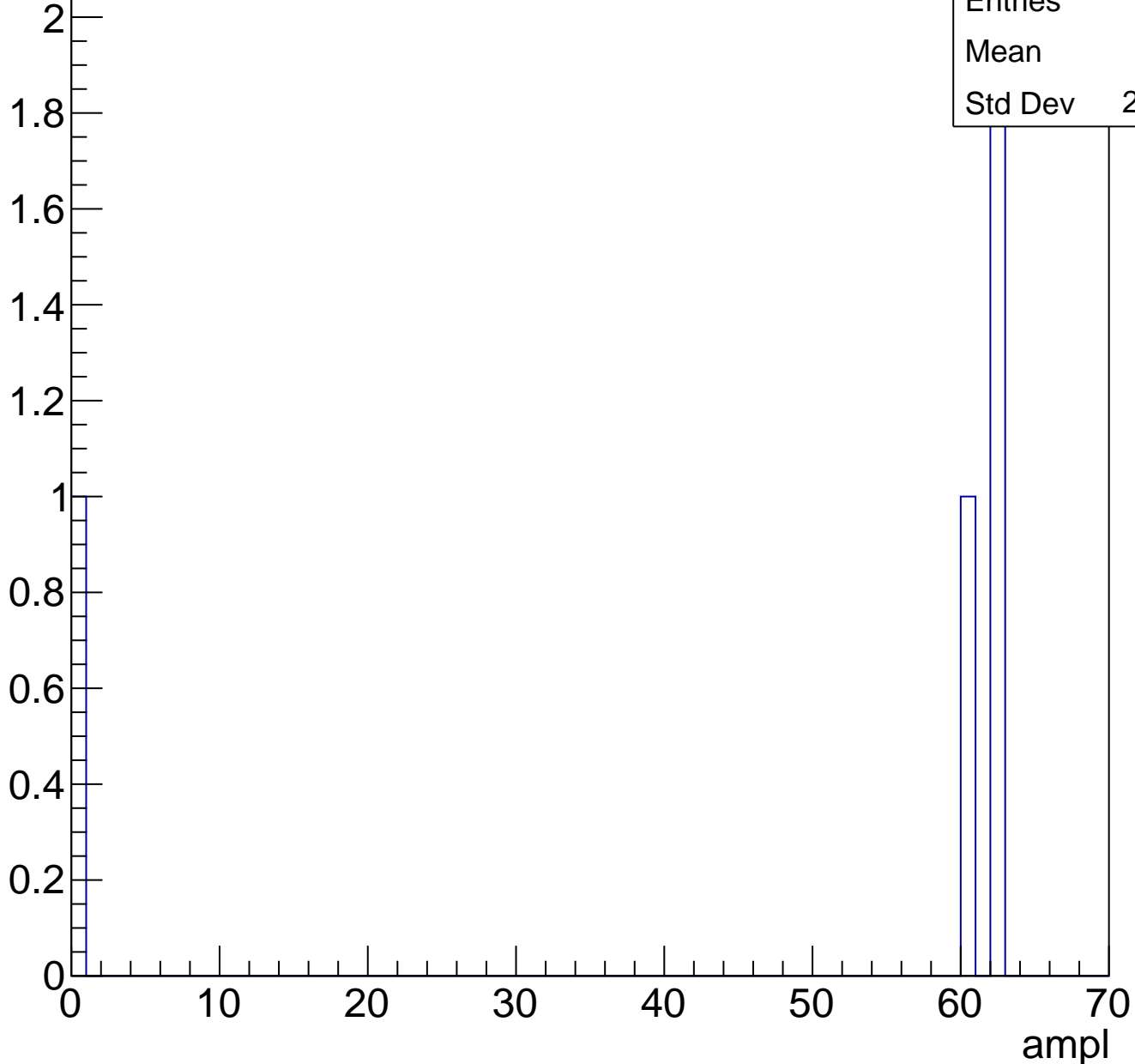
Entries	37
Mean	60.73
Std Dev	2.049



# B1L102S, U12-ch9, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U12-ch9, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L102S, U12-ch10, adc0

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	93
Mean	29.59
Std Dev	3.85

**Gaus mean : 30.4095**

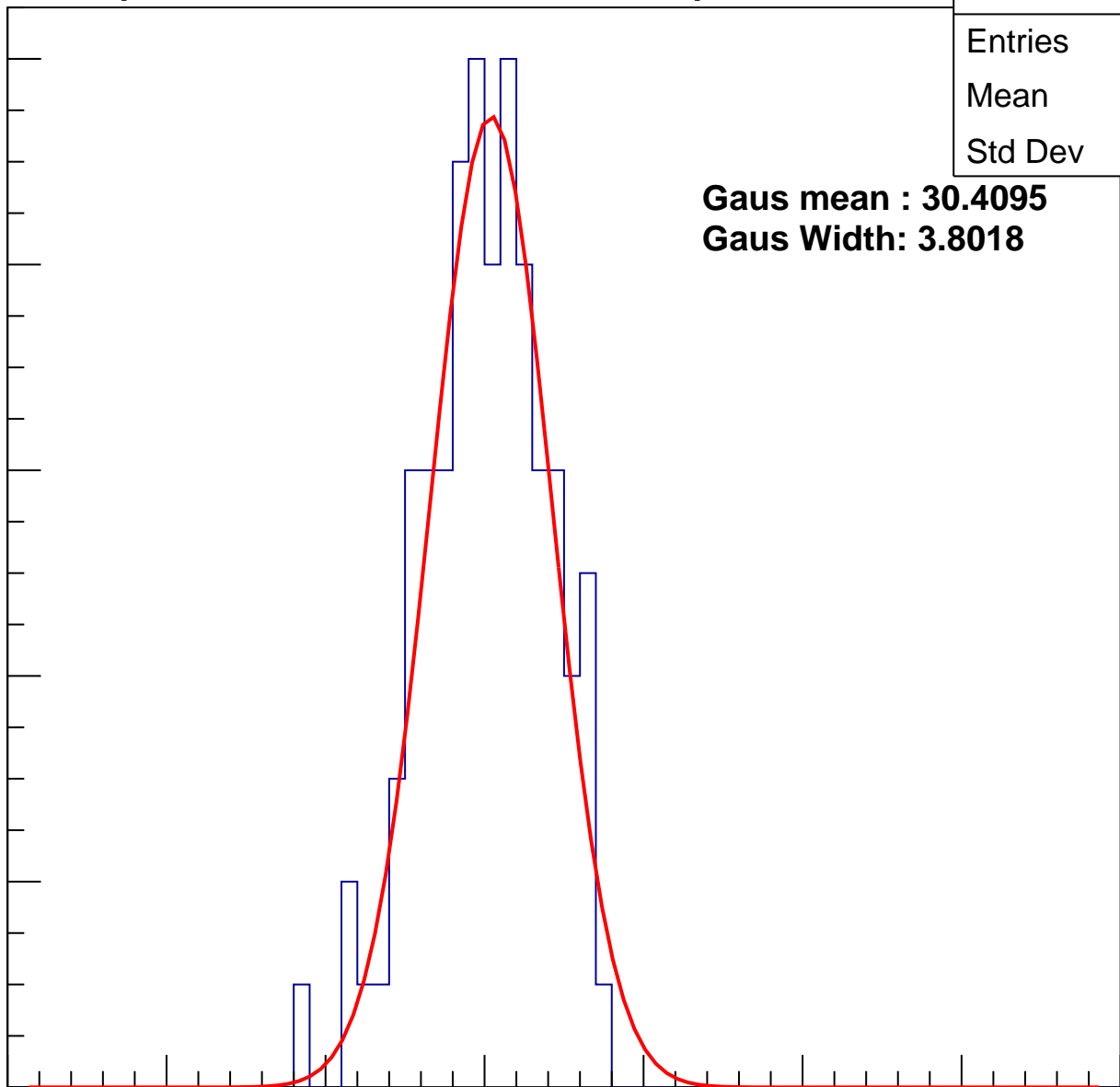
**Gaus Width: 3.8018**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L102S, U12-ch10, adc1

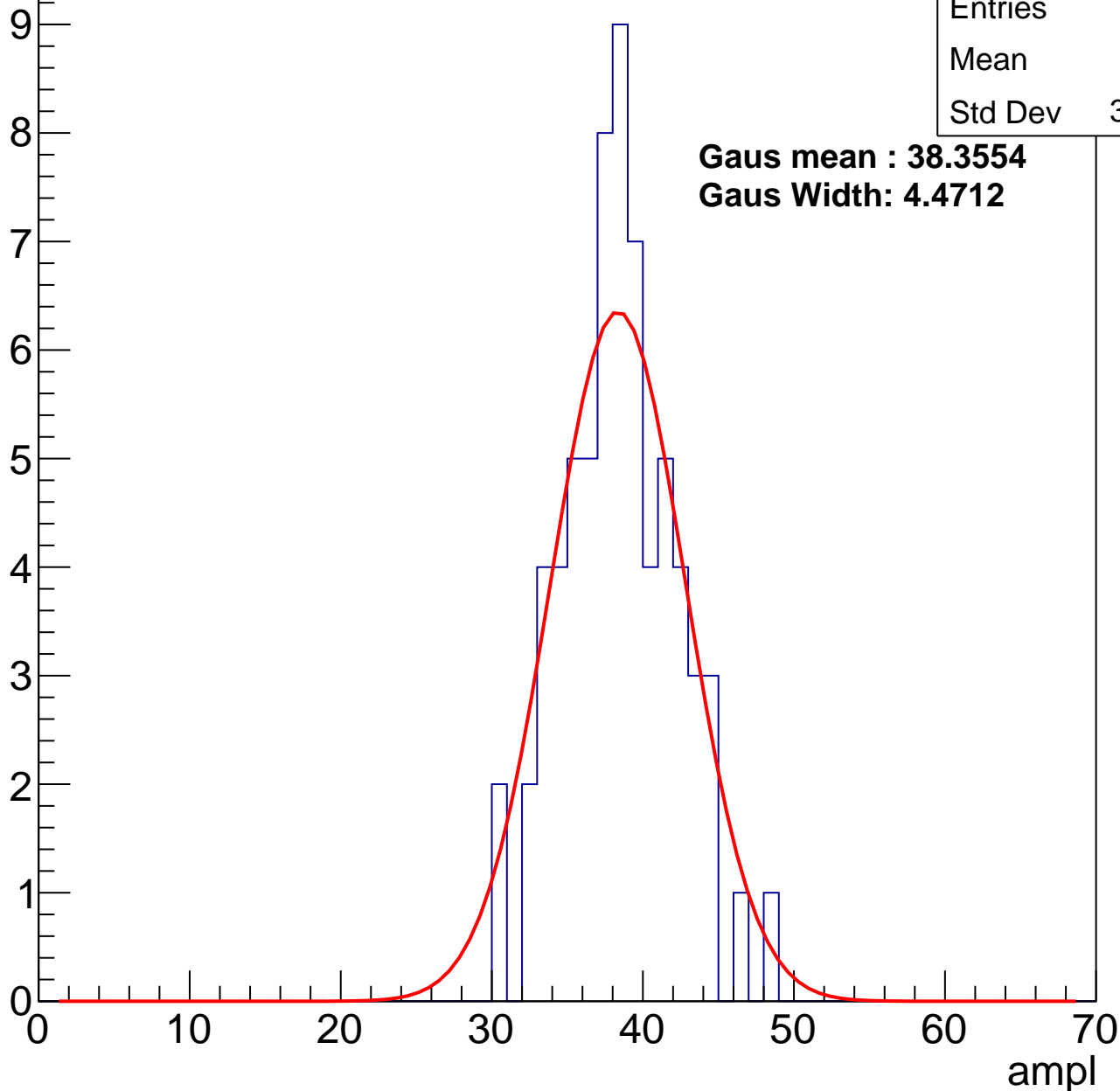
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	67
Mean	38
Std Dev	3.698

**Gaus mean : 38.3554**

**Gaus Width: 4.4712**



# B1L102S, U12-ch10, adc2

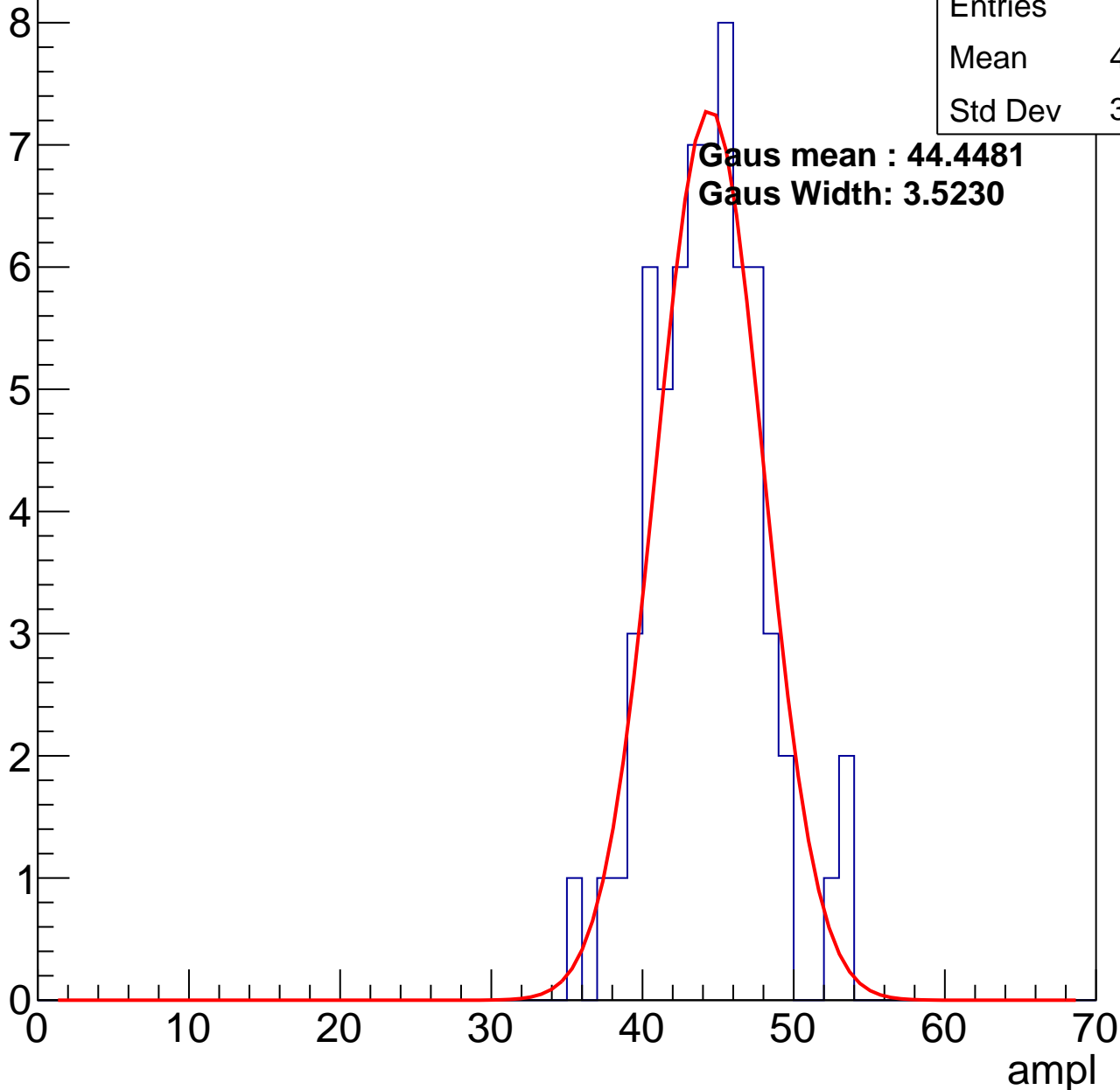
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	65
Mean	43.86
Std Dev	3.556

**Gaus mean : 44.4481**

**Gaus Width: 3.5230**

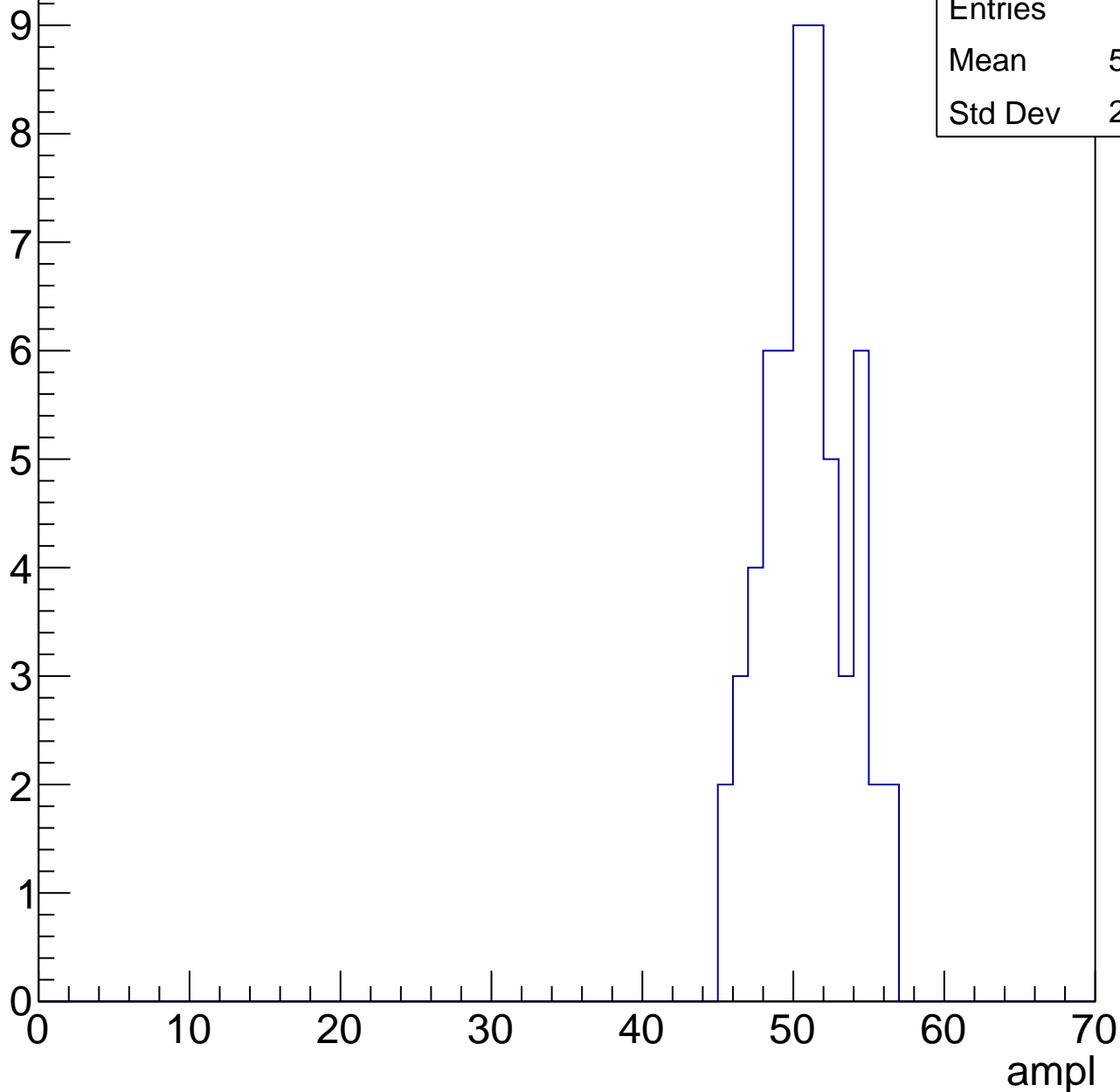


# B1L102S, U12-ch10, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	57
Mean	50.39
Std Dev	2.745

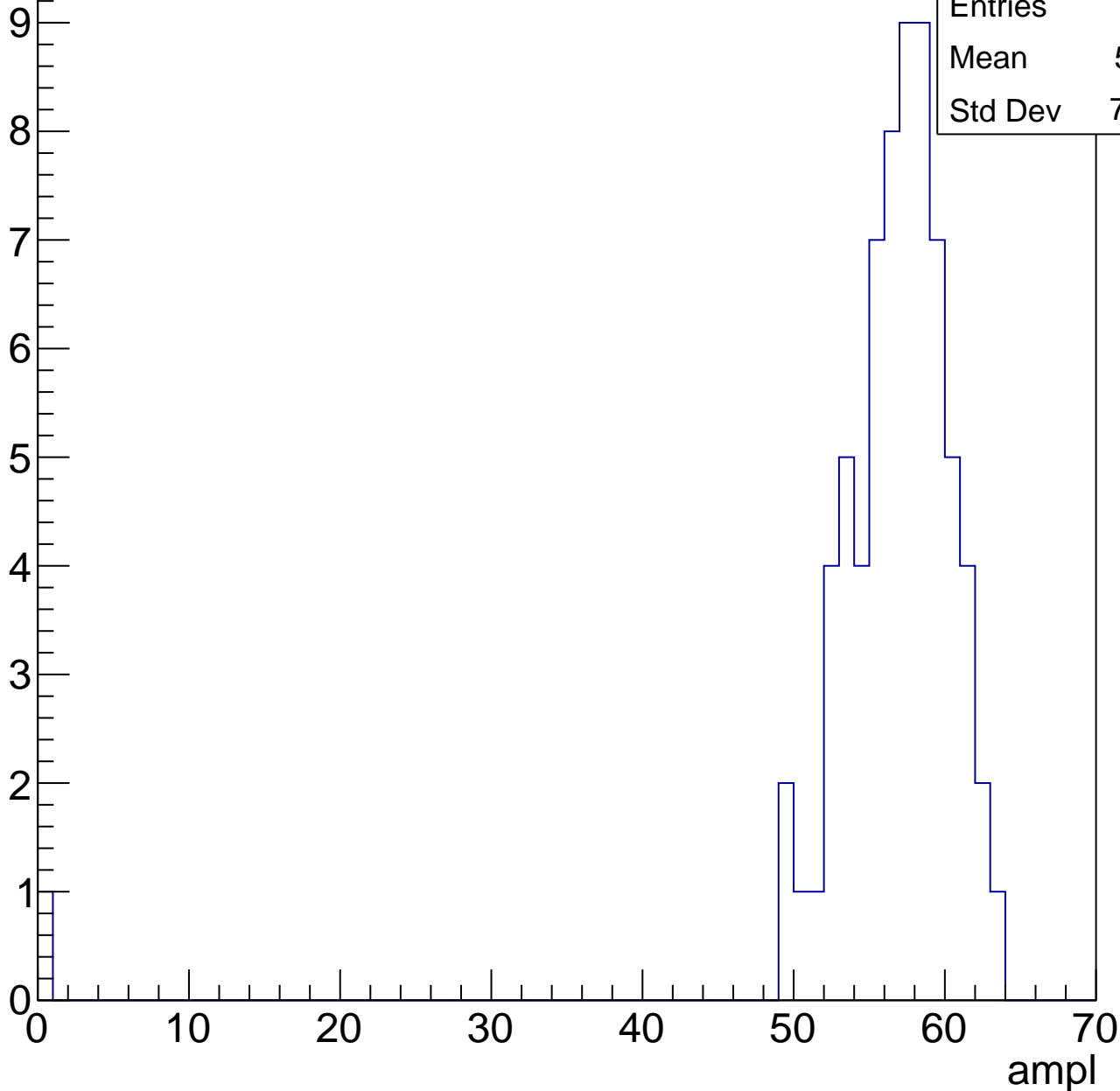


# B1L102S, U12-ch10, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	70
Mean	55.71
Std Dev	7.397

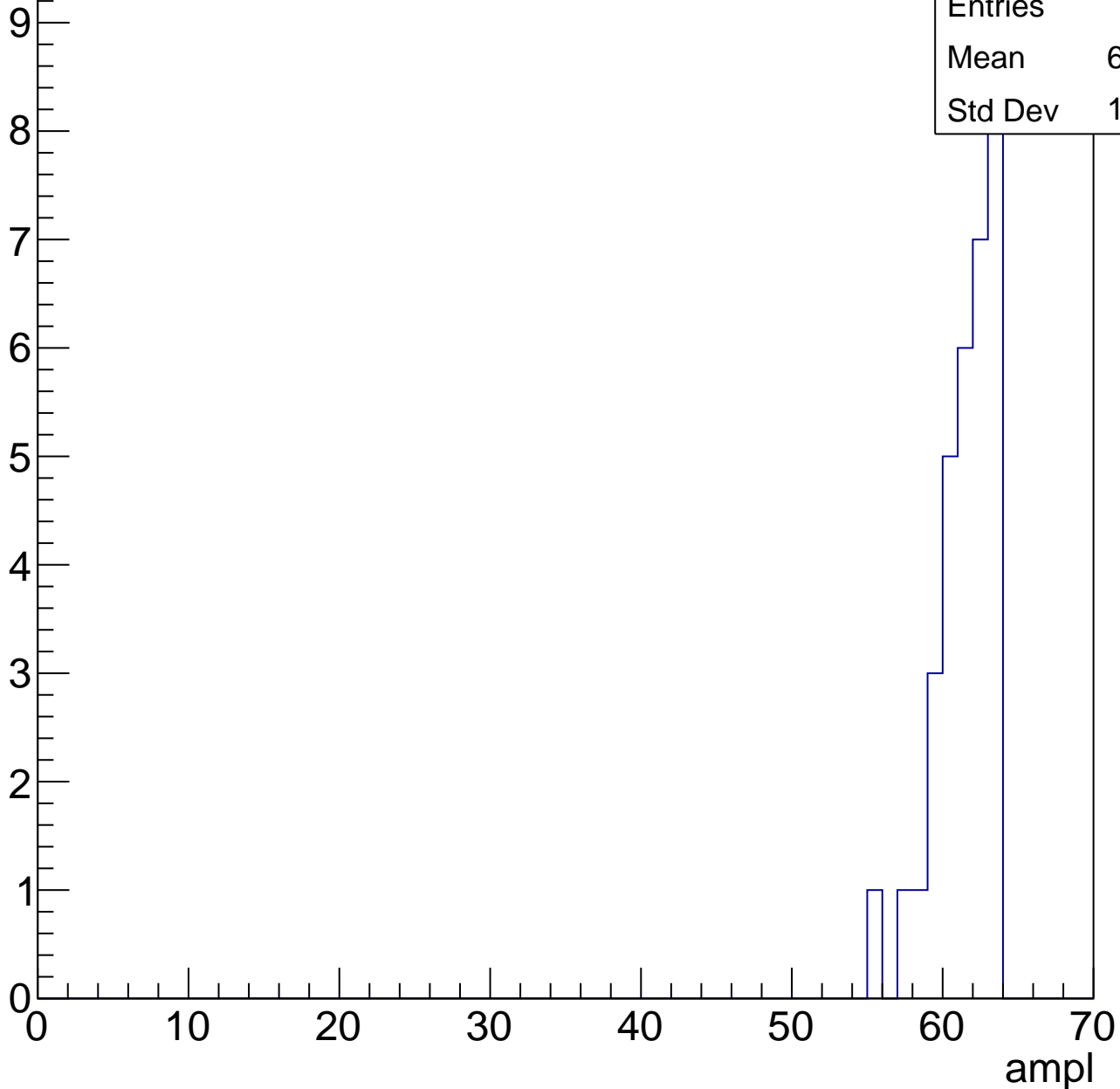


# B1L102S, U12-ch10, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	33
Mean	61.03
Std Dev	1.915



# B1L102S, U12-ch10, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U12-ch10, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U12-ch11, adc0

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	74
Mean	28.51
Std Dev	4.847

**Gaus mean : 29.0702**

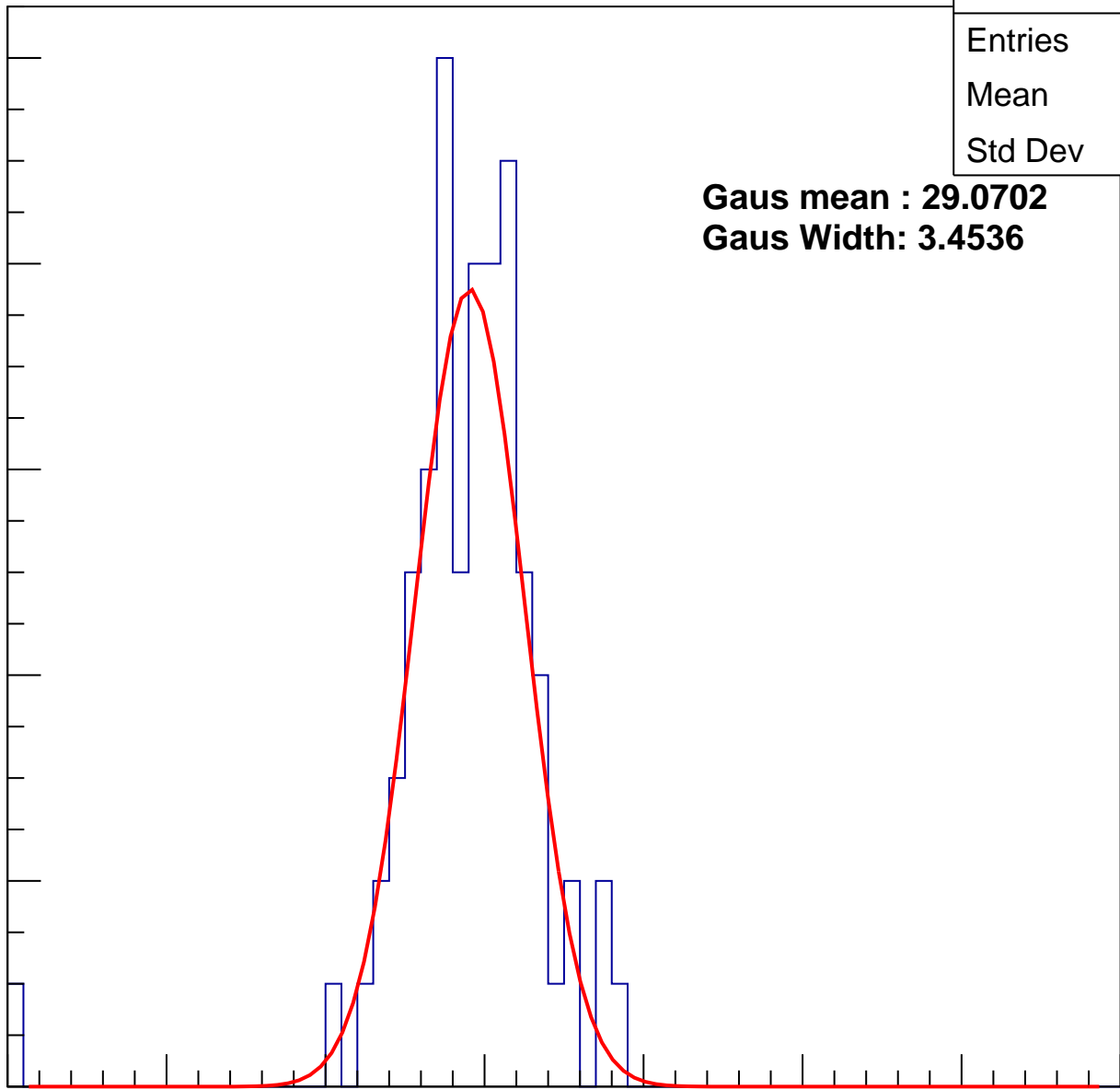
**Gaus Width: 3.4536**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L102S, U12-ch11, adc1

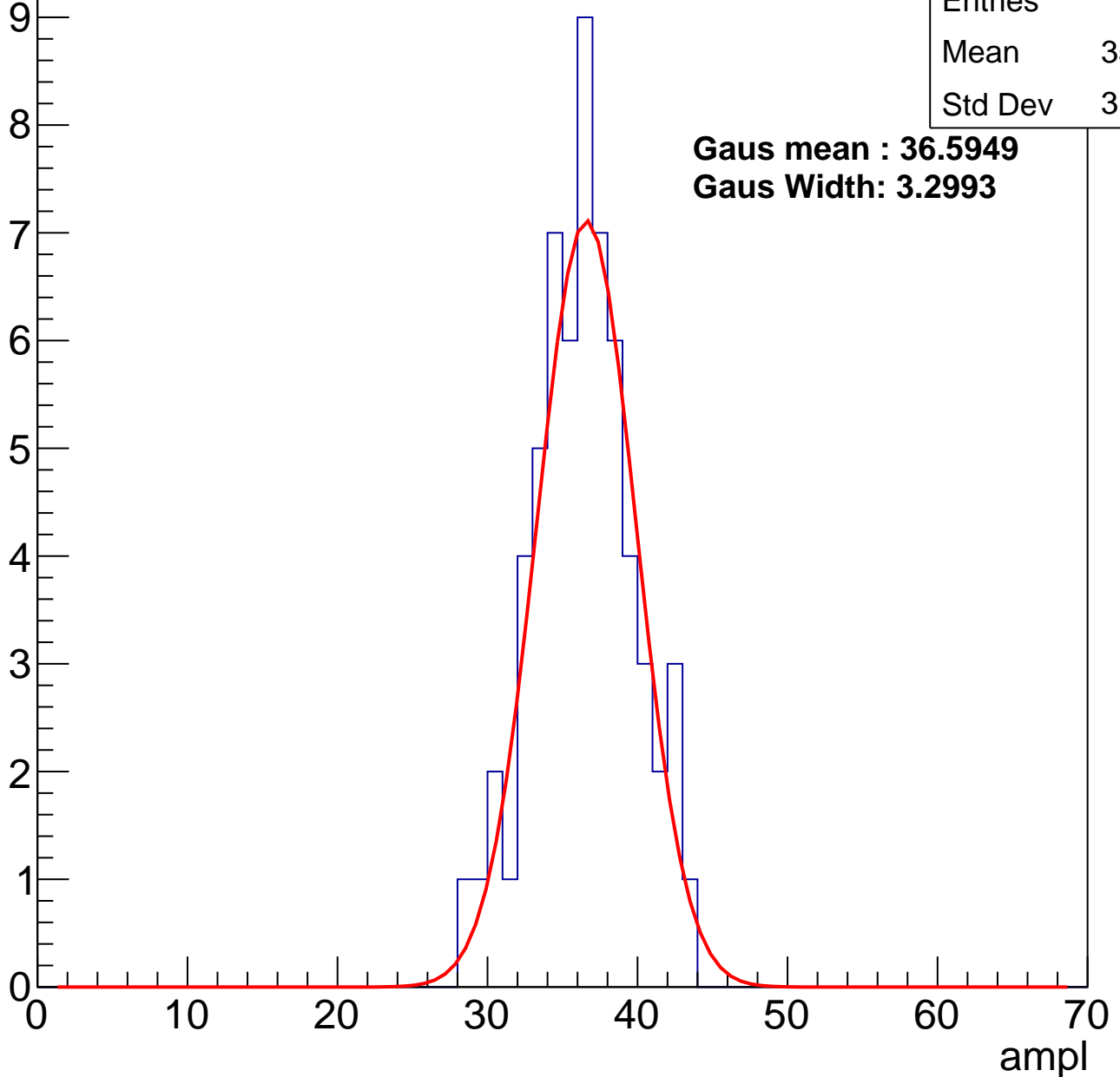
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	62
Mean	35.92
Std Dev	3.299

**Gaus mean : 36.5949**

**Gaus Width: 3.2993**



# B1L102S, U12-ch11, adc2

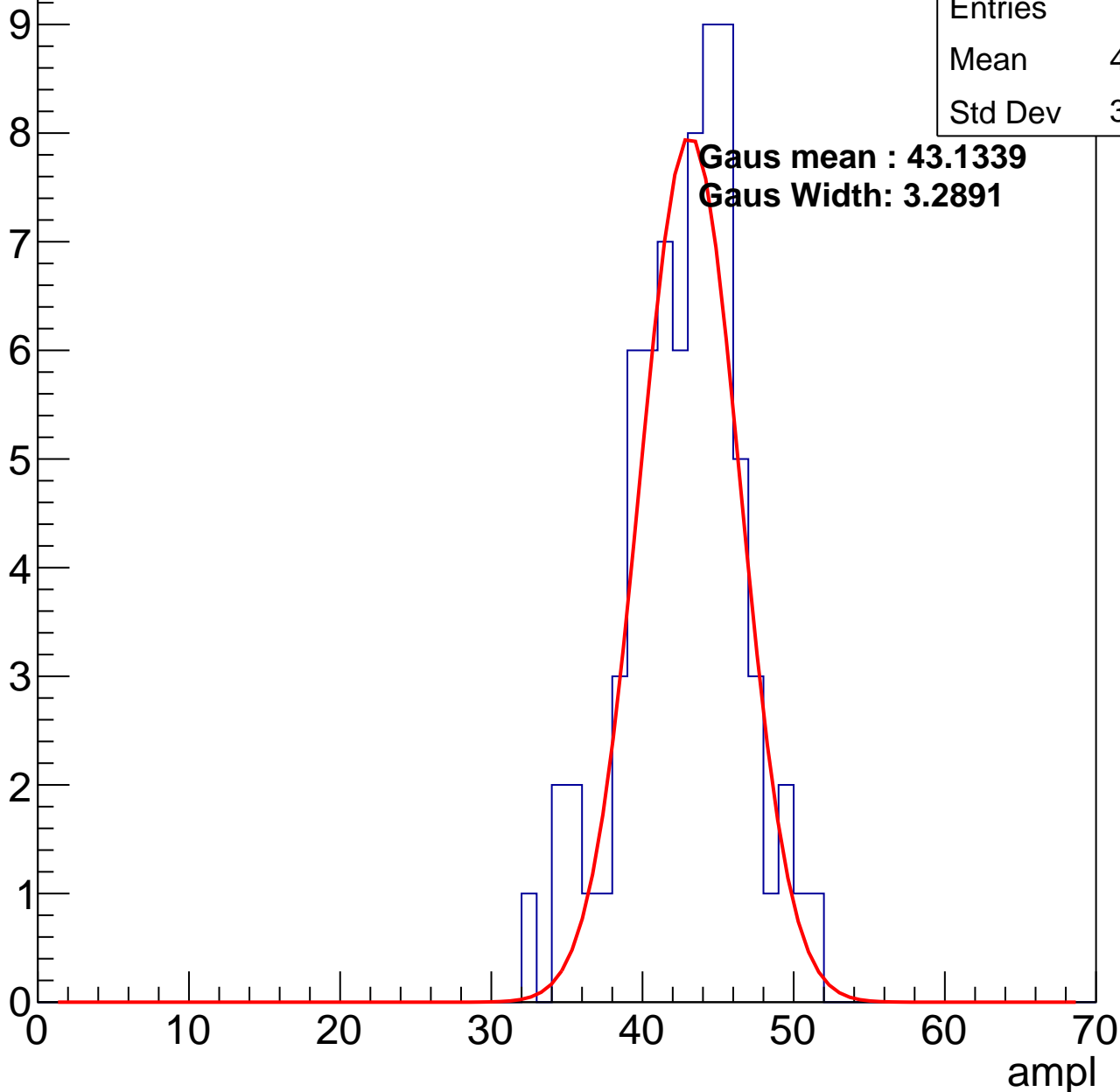
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	74
Mean	42.34
Std Dev	3.804

**Gaus mean : 43.1339**

**Gaus Width: 3.2891**

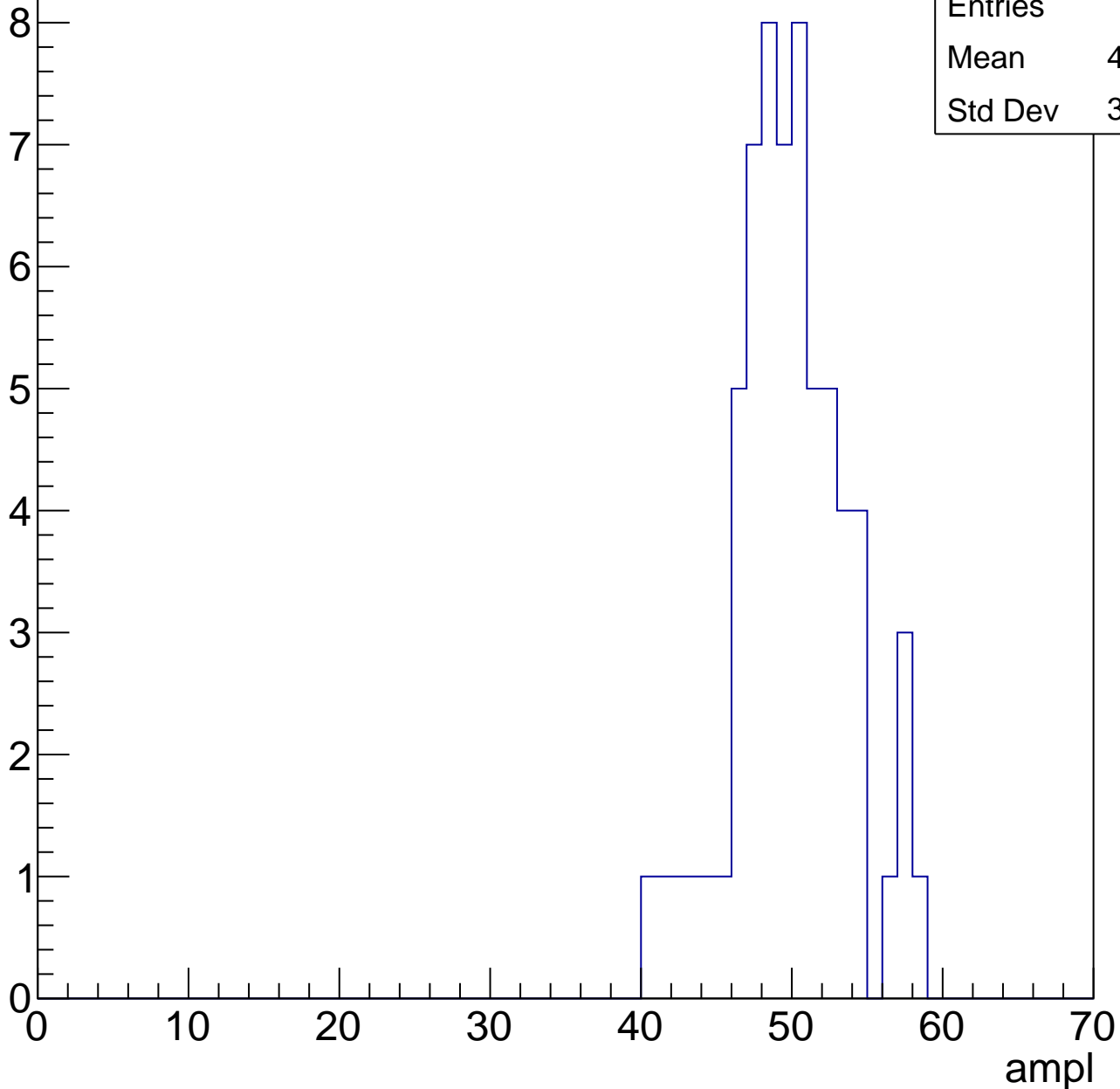


# B1L102S, U12-ch11, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	49.52
Std Dev	3.737

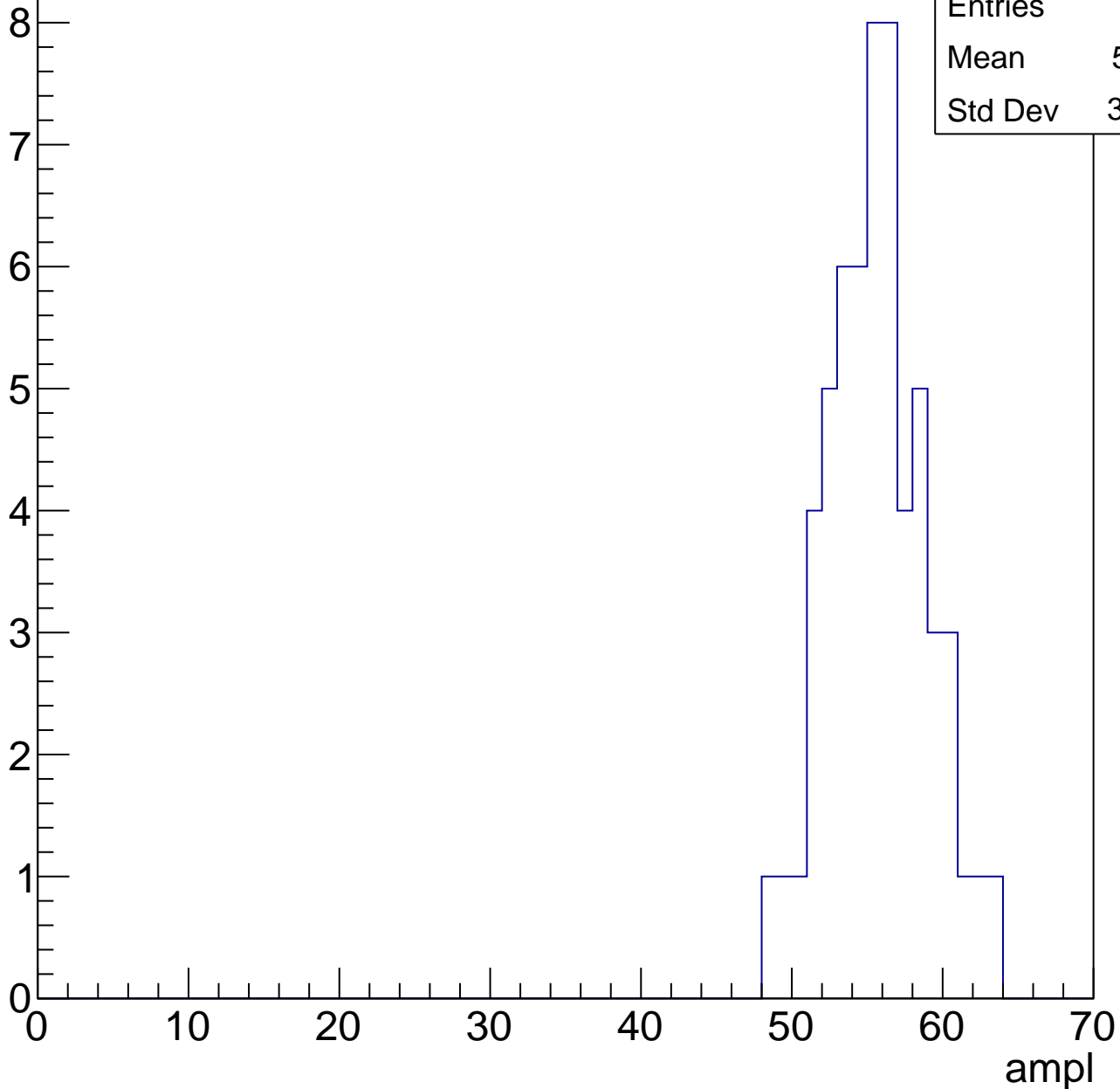


# B1L102S, U12-ch11, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	58
Mean	55.21
Std Dev	3.183

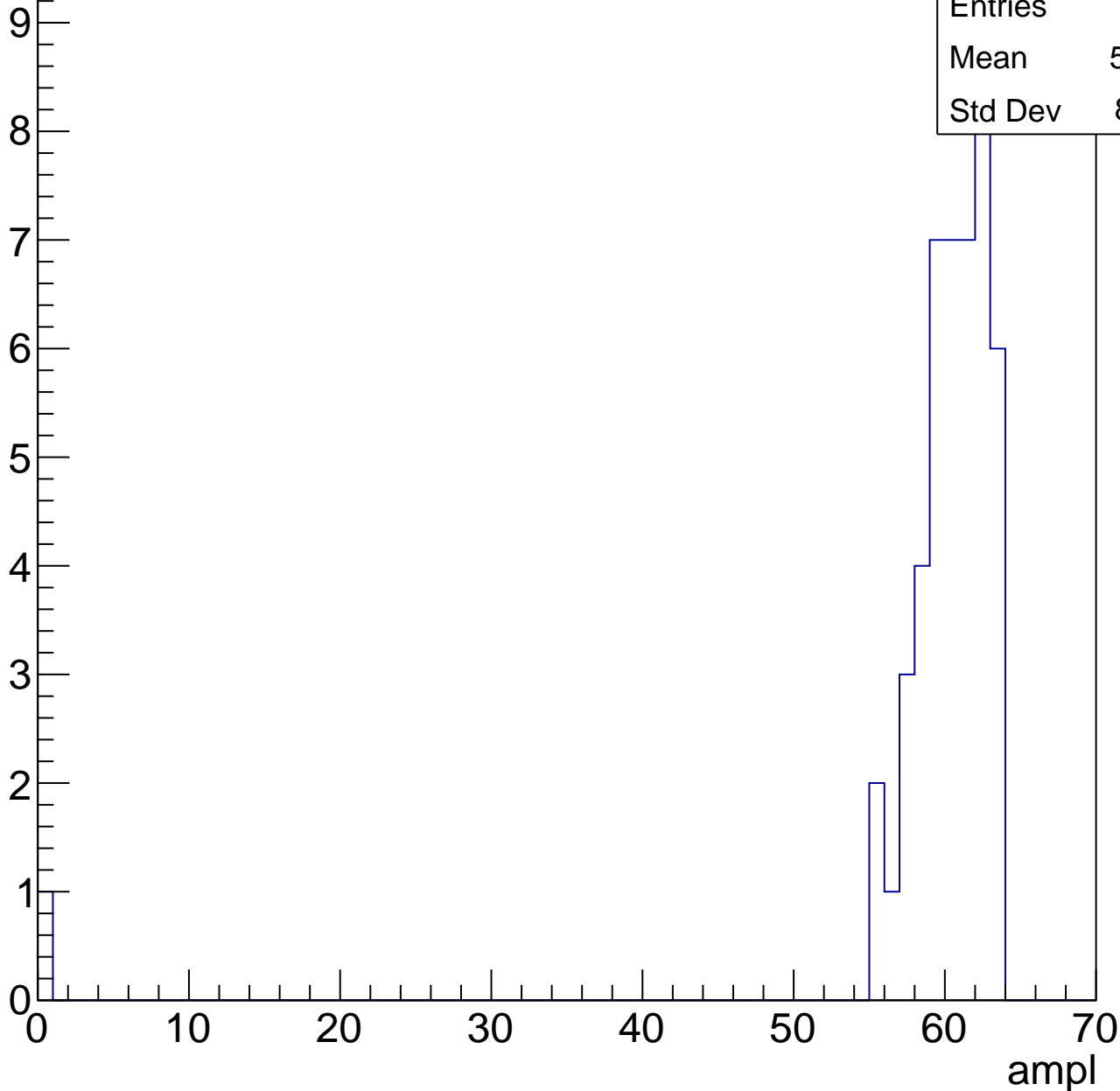


# B1L102S, U12-ch11, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	47
Mean	58.83
Std Dev	8.931



# B1L102S, U12-ch11, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U12-ch11, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U12-ch12, adc0

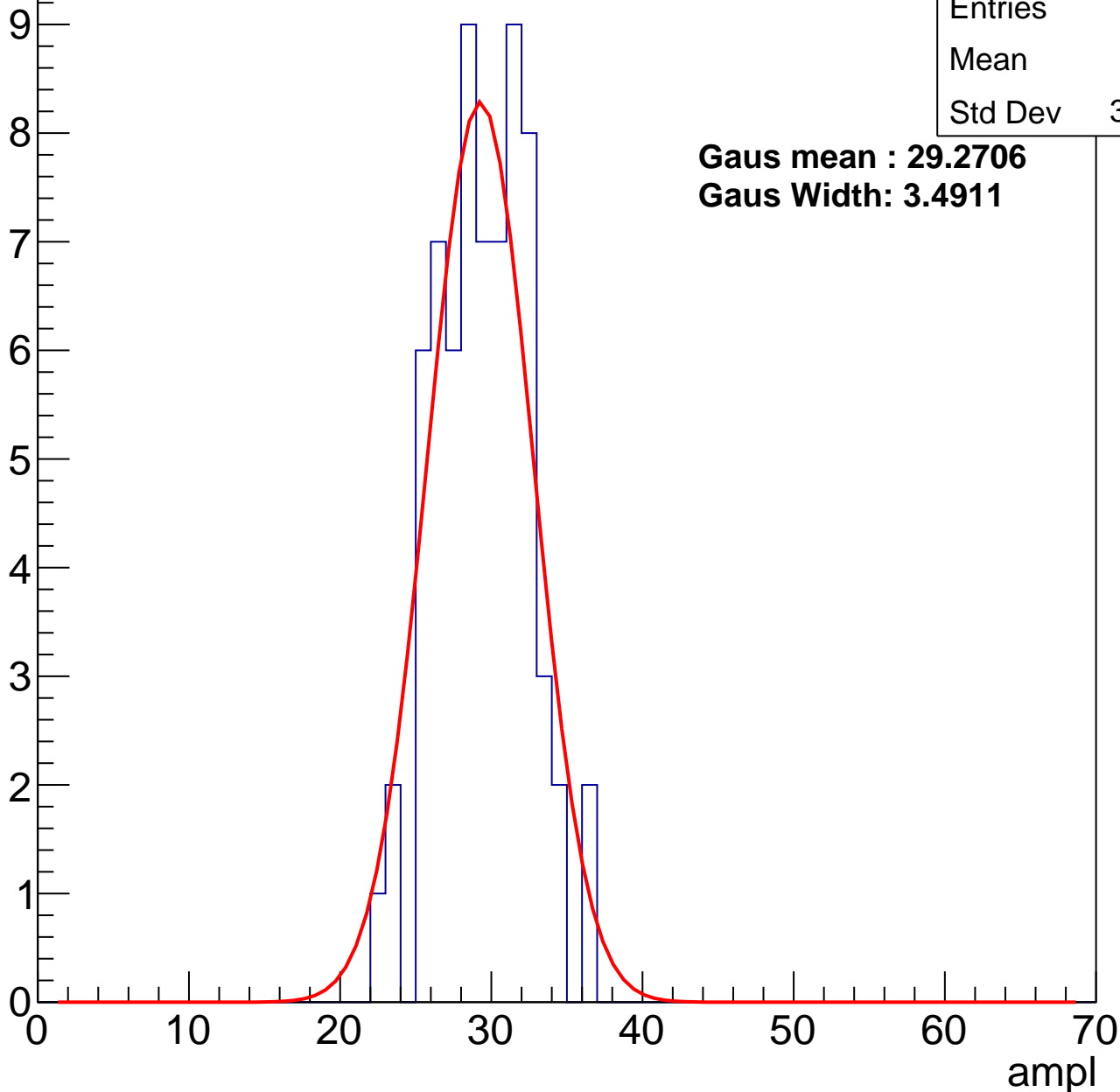
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	29
Std Dev	3.007

**Gaus mean : 29.2706**

**Gaus Width: 3.4911**



# B1L102S, U12-ch12, adc1

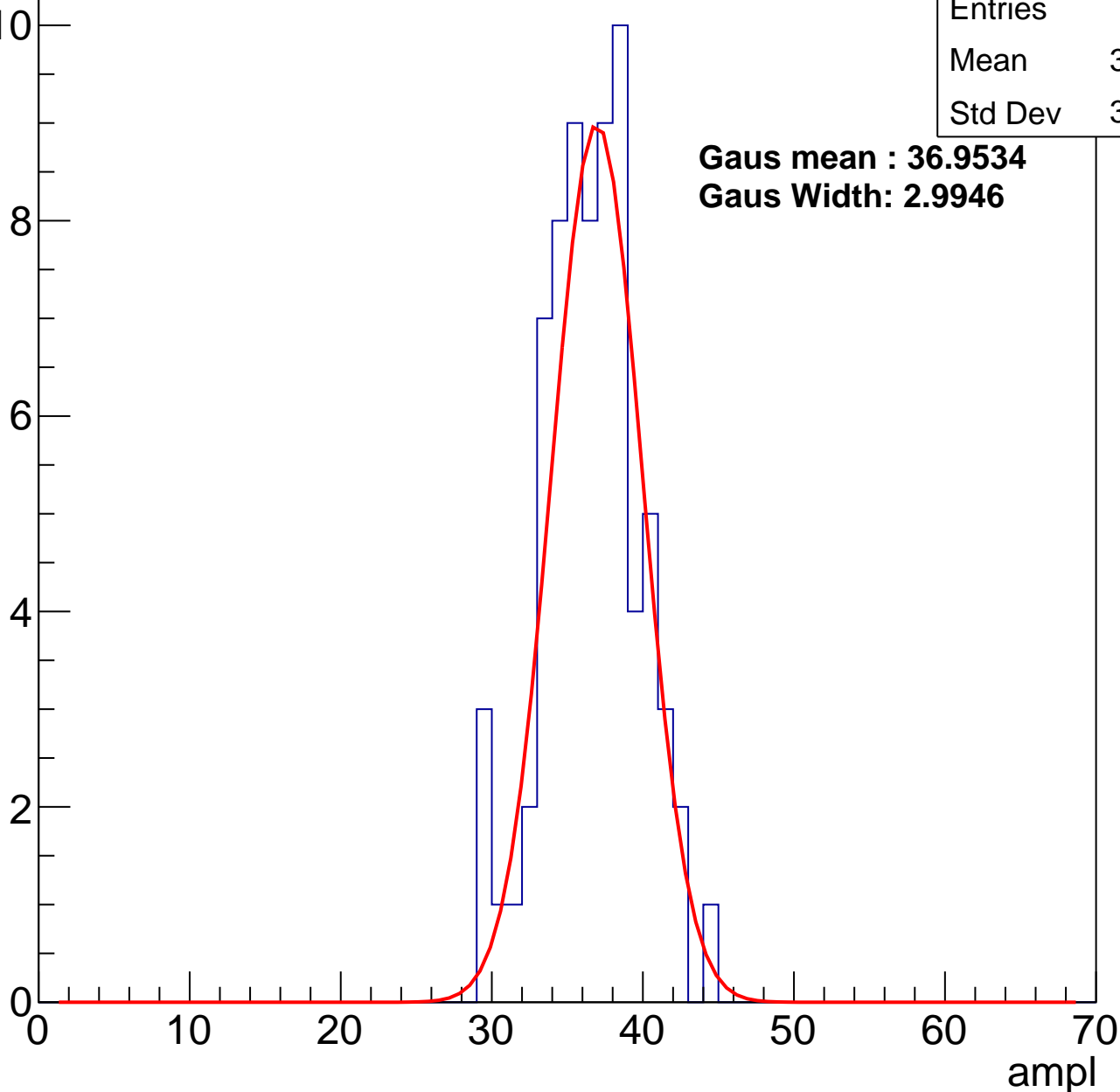
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	73
Mean	36.14
Std Dev	3.138

**Gaus mean : 36.9534**

**Gaus Width: 2.9946**



# B1L102S, U12-ch12, adc2

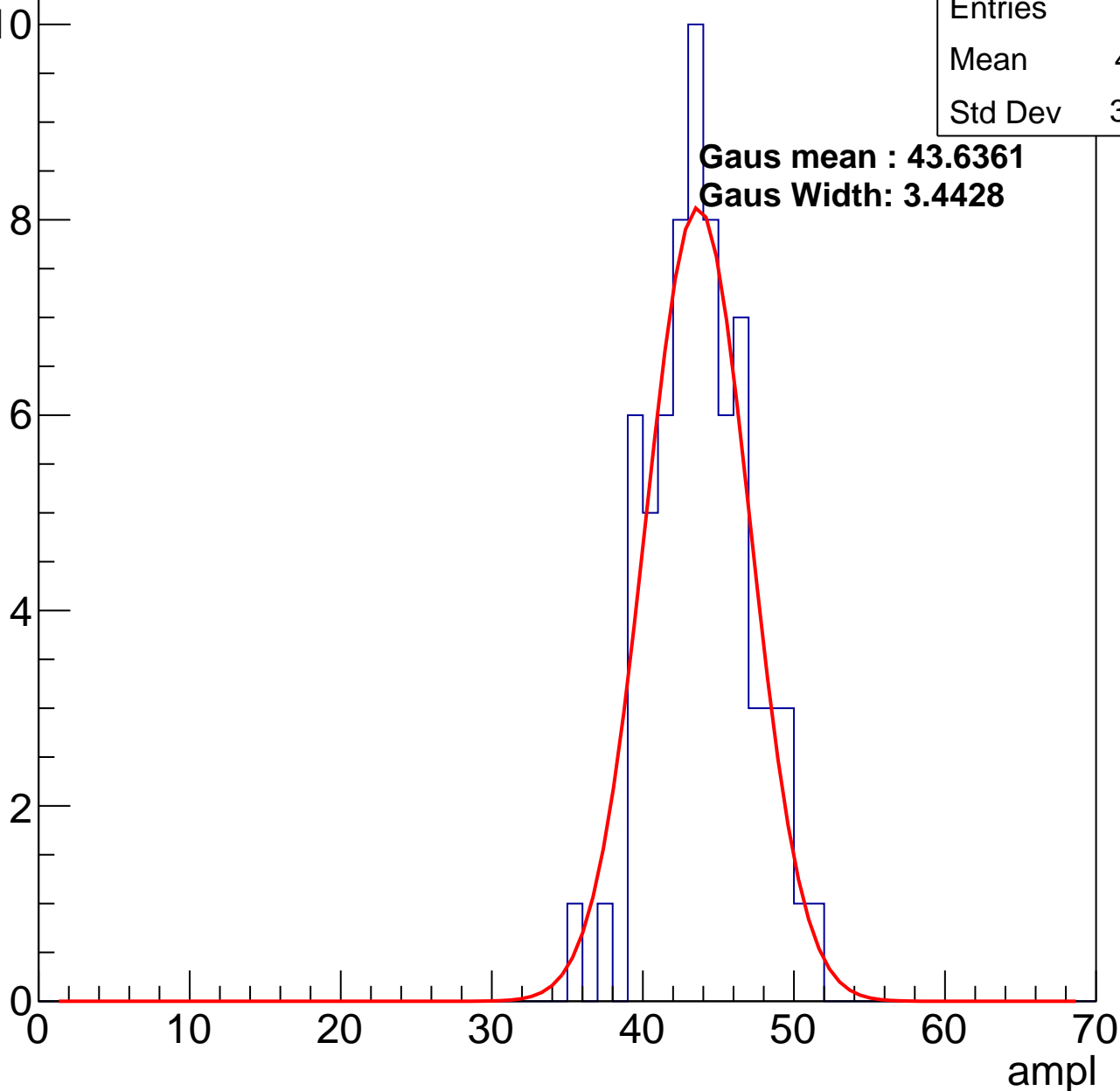
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	43.41
Std Dev	3.187

**Gaus mean : 43.6361**

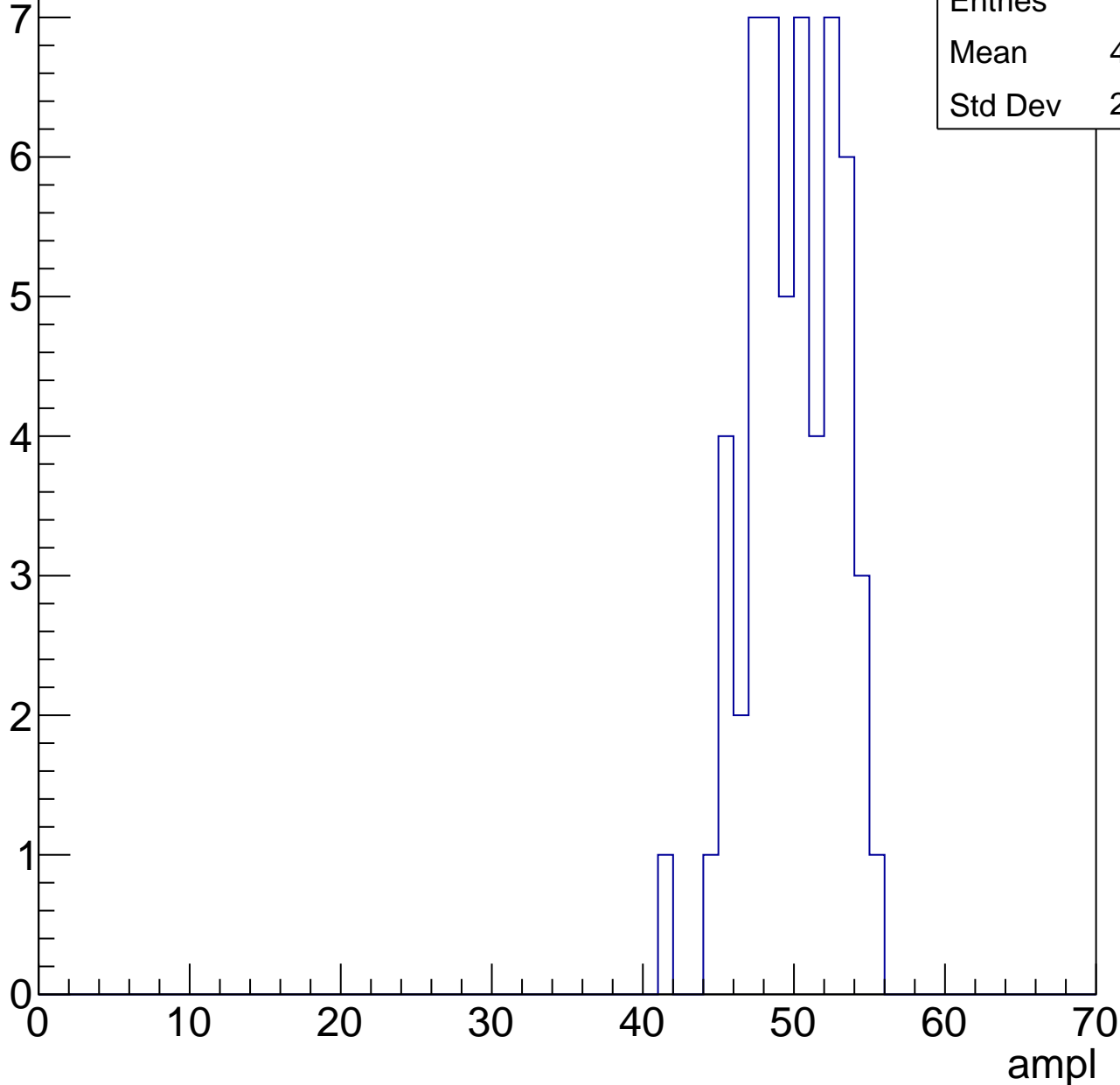
**Gaus Width: 3.4428**



# B1L102S, U12-ch12, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



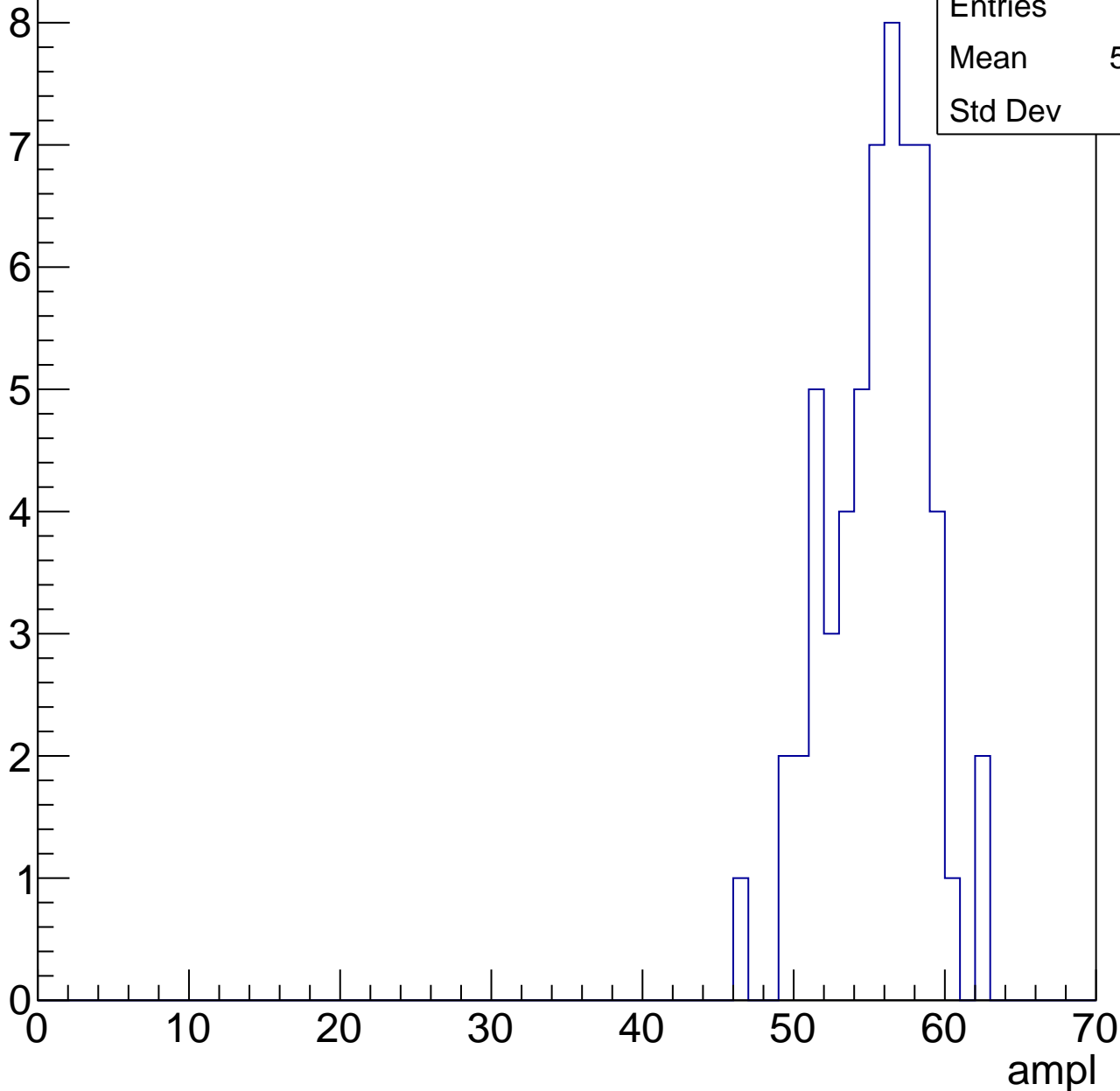
Entries	55
Mean	49.45
Std Dev	2.978

# B1L102S, U12-ch12, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

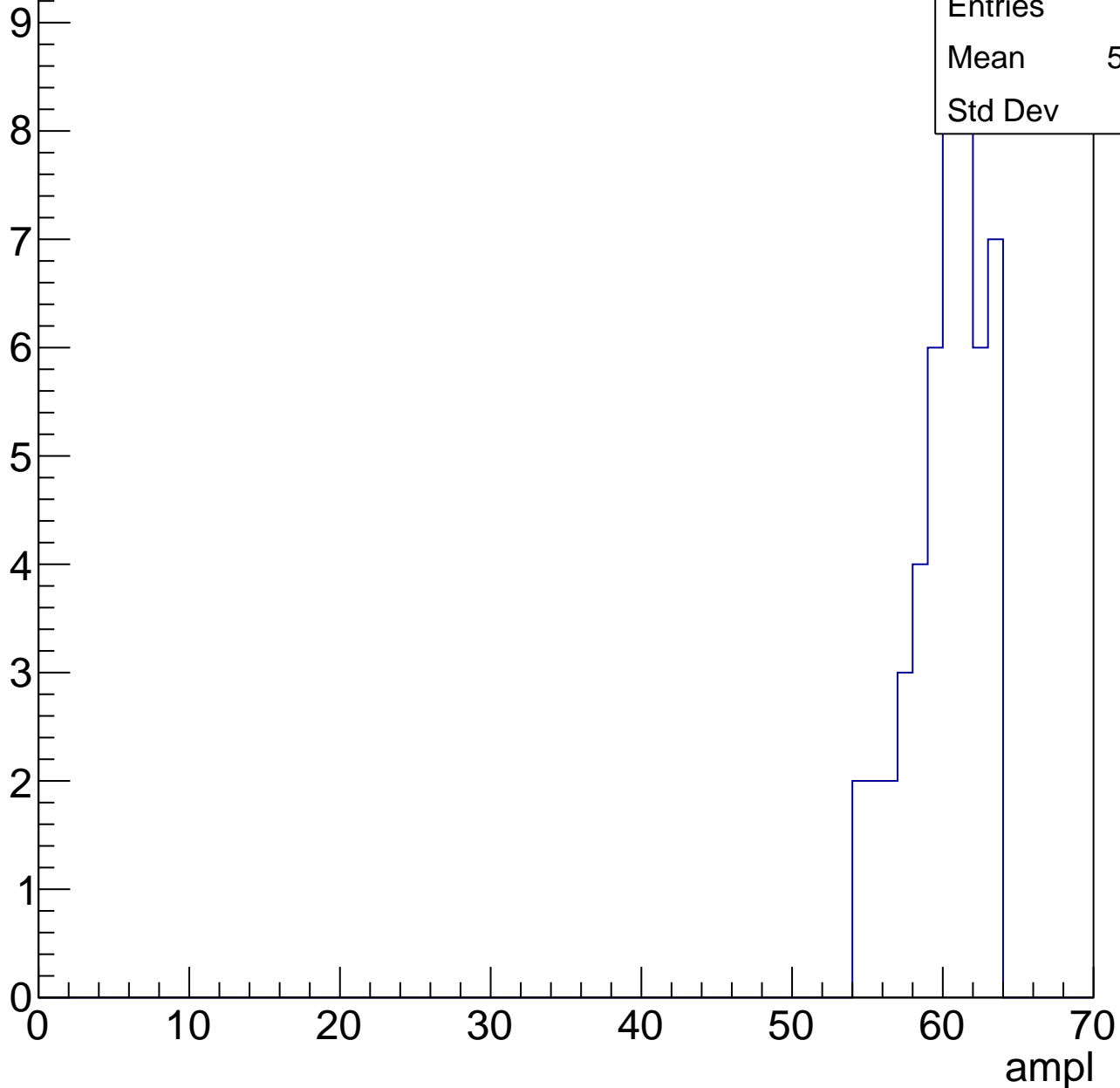
Entries	58
Mean	55.09
Std Dev	3.26



# B1L102S, U12-ch12, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

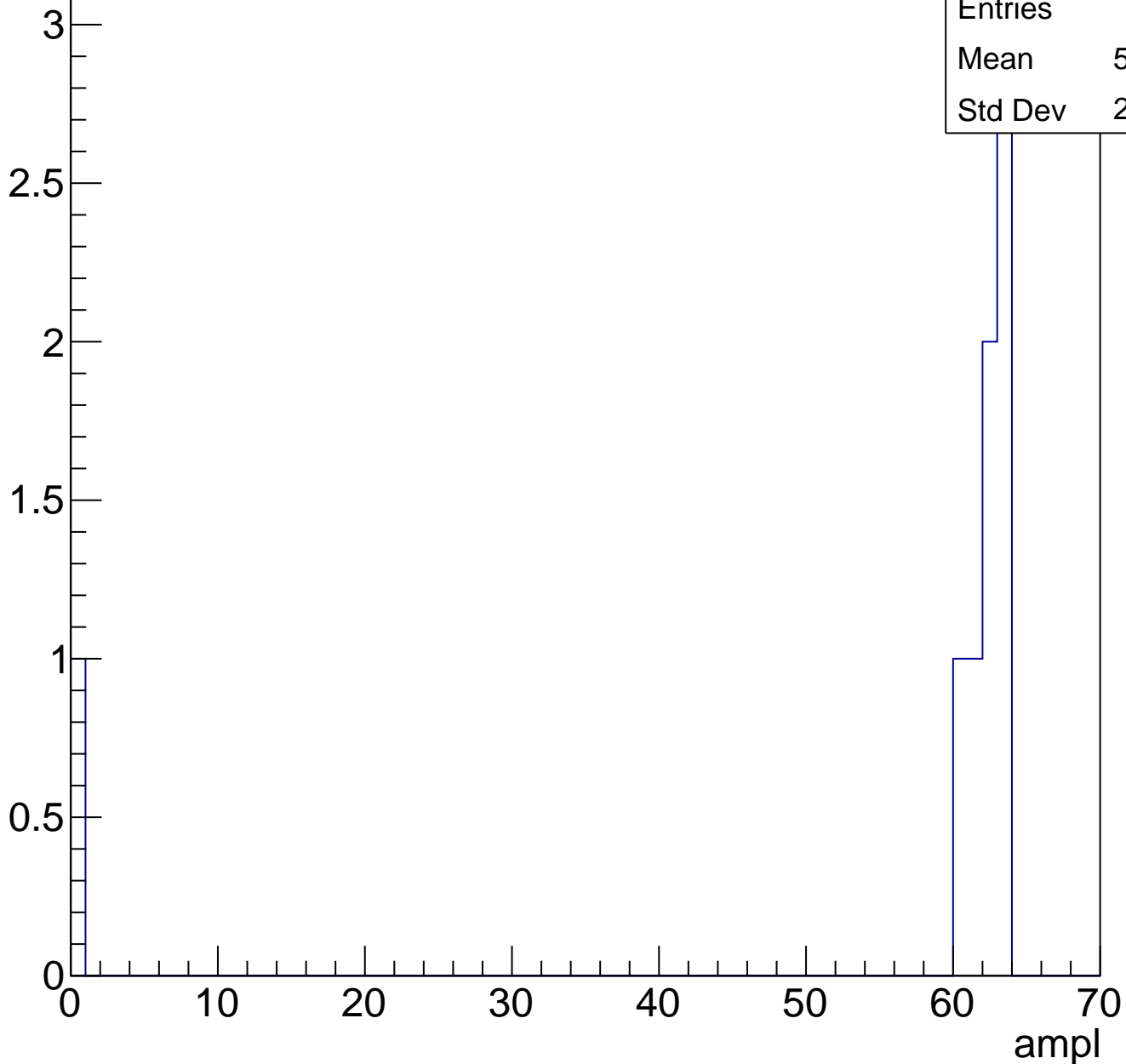
Entry



# B1L102S, U12-ch12, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	8
Mean	54.25
Std Dev	20.53



# B1L102S, U12-ch12, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U12-ch13, adc0

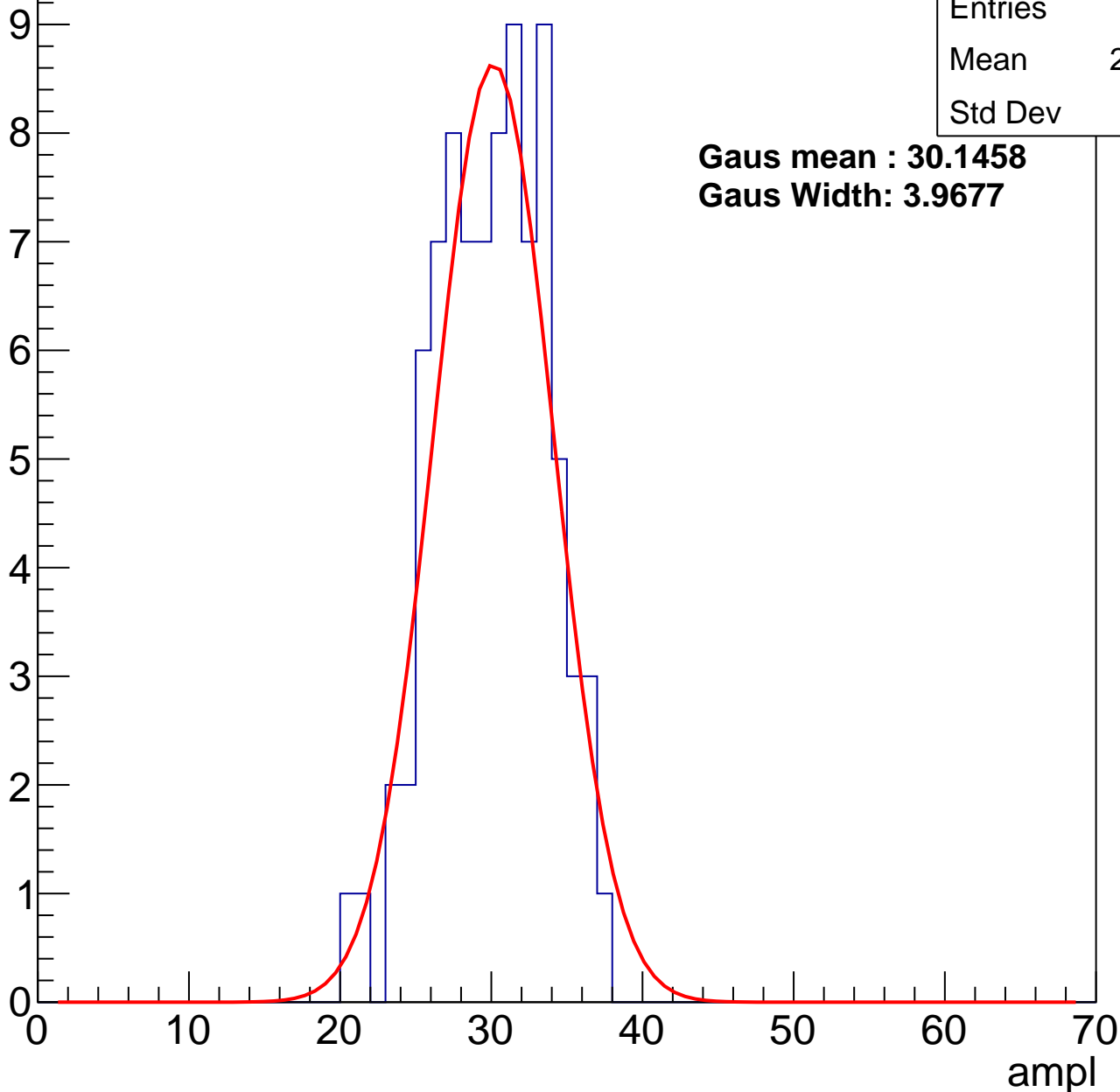
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	86
Mean	29.56
Std Dev	3.63

**Gaus mean : 30.1458**

**Gaus Width: 3.9677**



# B1L102S, U12-ch13, adc1

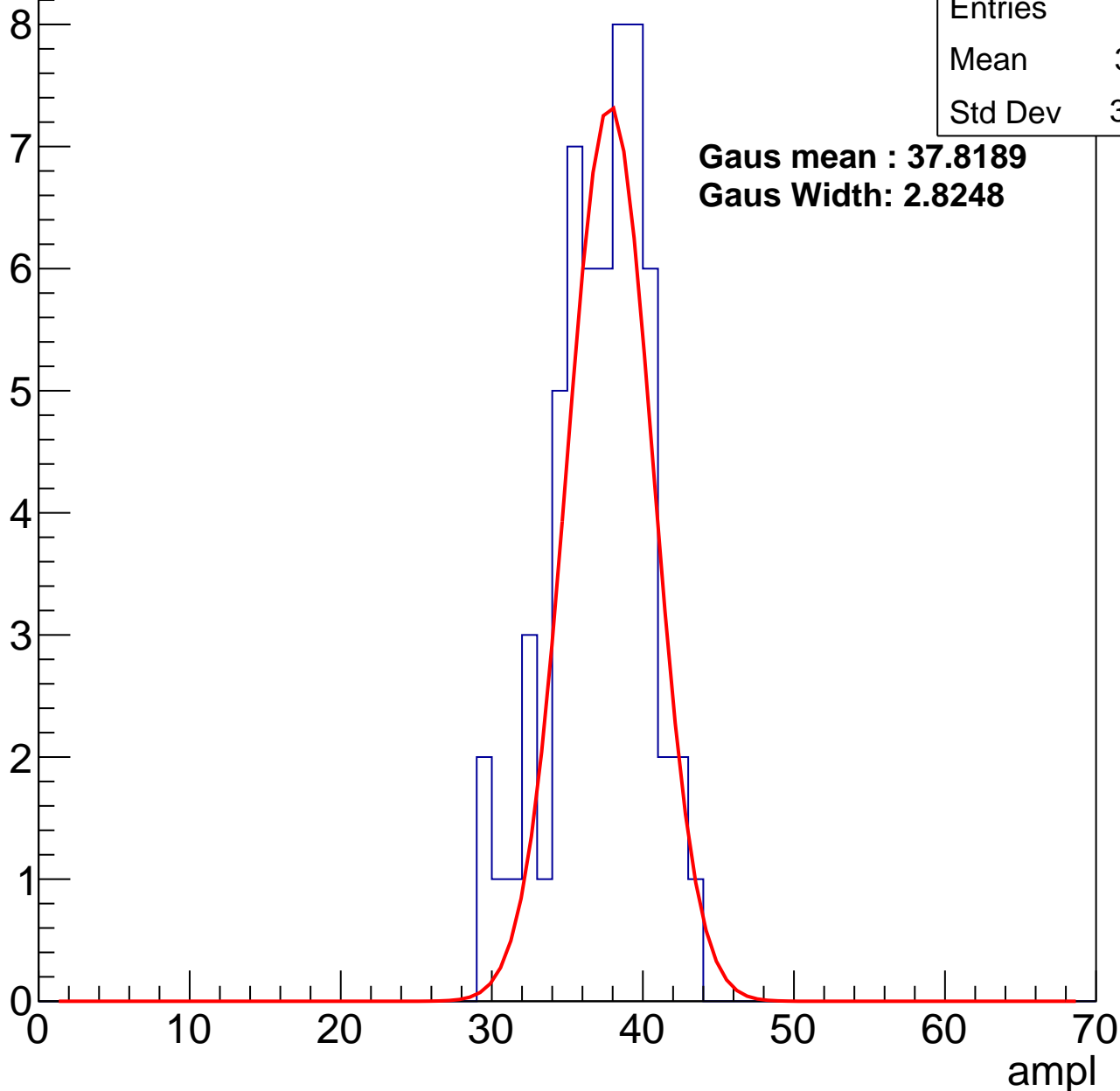
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	59
Mean	36.71
Std Dev	3.163

**Gaus mean : 37.8189**

**Gaus Width: 2.8248**



# B1L102S, U12-ch13, adc2

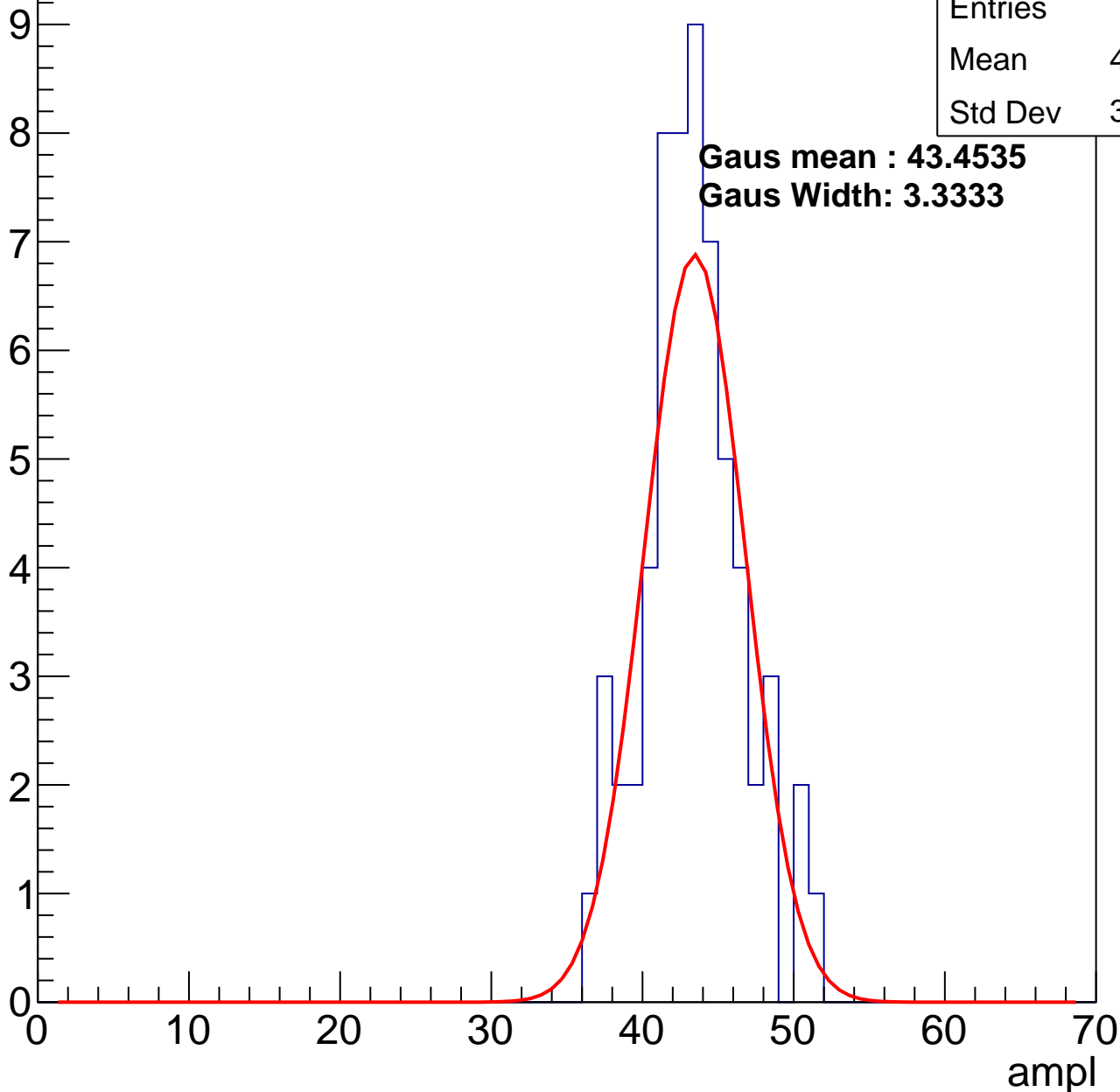
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	42.92
Std Dev	3.256

**Gaus mean : 43.4535**

**Gaus Width: 3.3333**

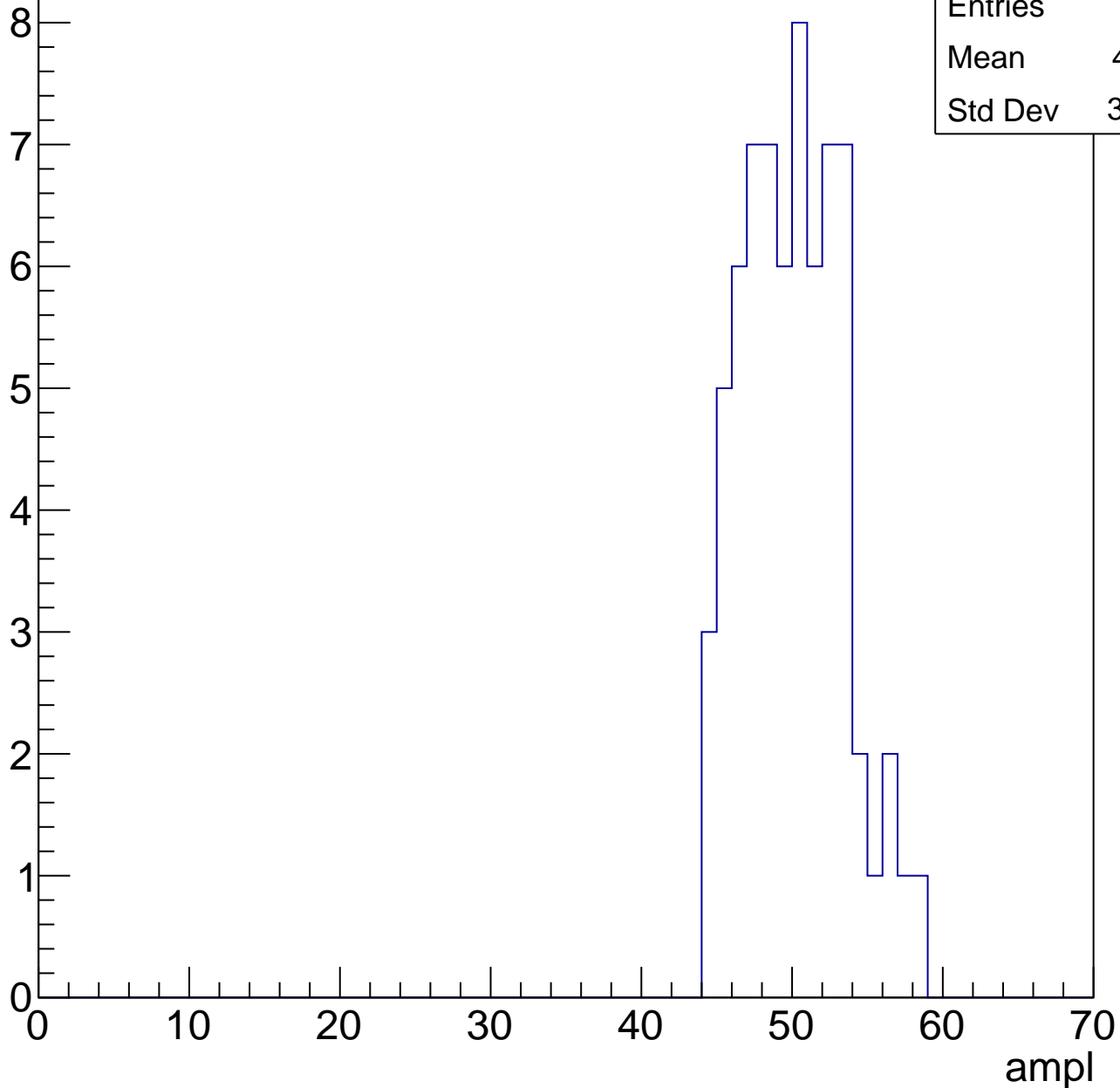


# B1L102S, U12-ch13, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

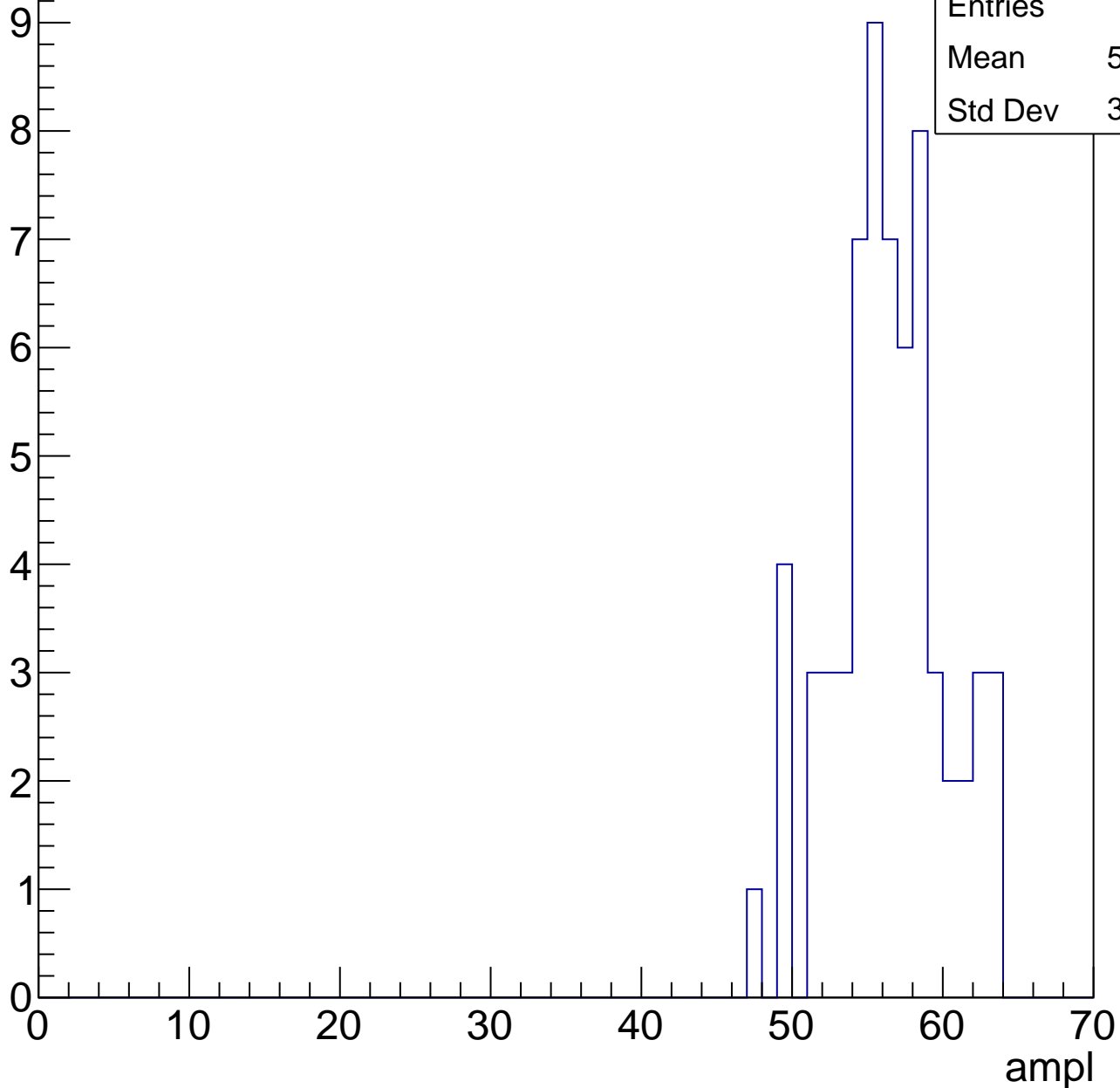
Entries	69
Mean	49.61
Std Dev	3.307



# B1L102S, U12-ch13, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



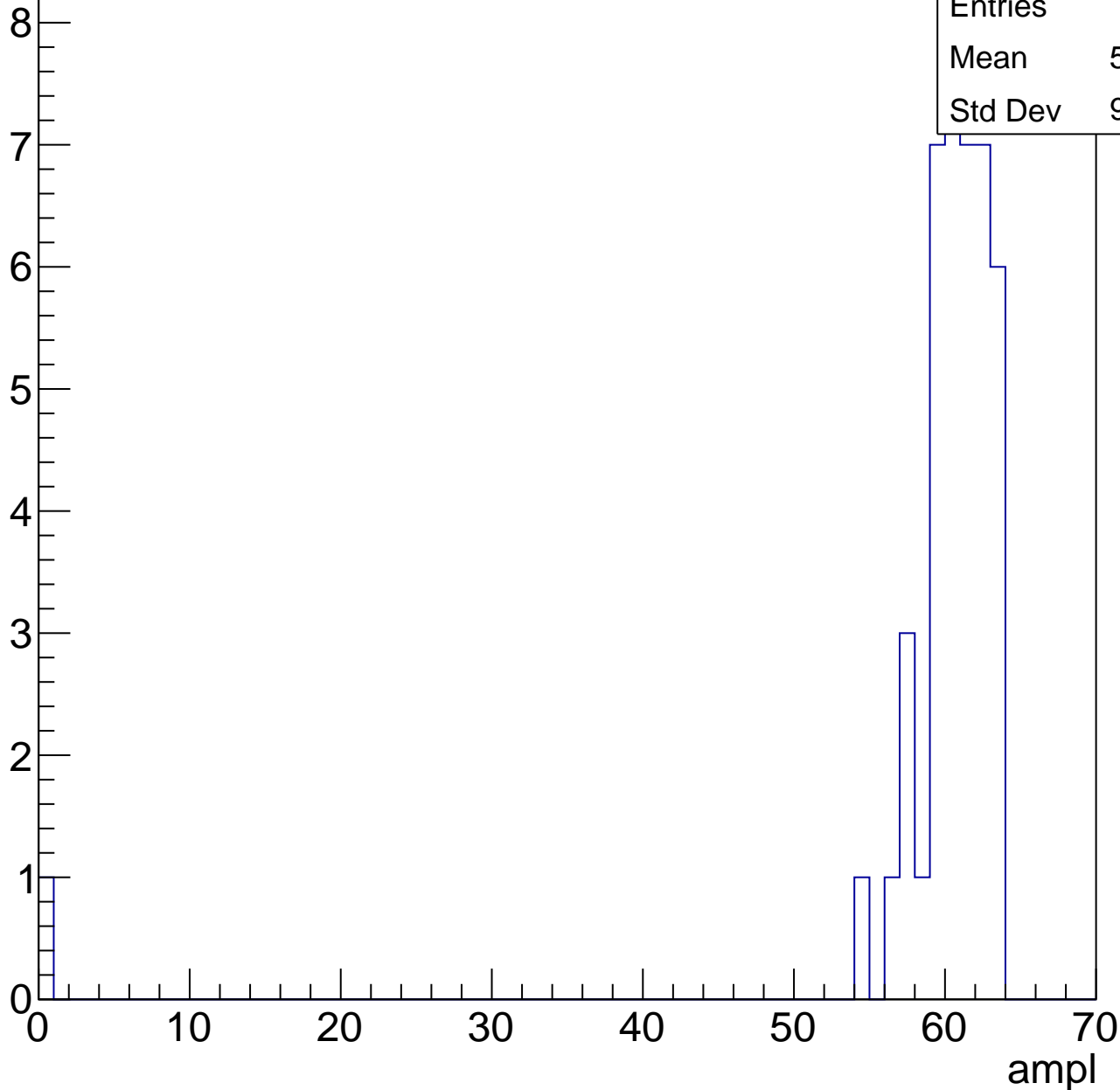
Entries	64
Mean	55.88
Std Dev	3.676

# B1L102S, U12-ch13, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	42
Mean	58.83
Std Dev	9.414



# B1L102S, U12-ch13, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U12-ch13, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U12-ch14, adc0

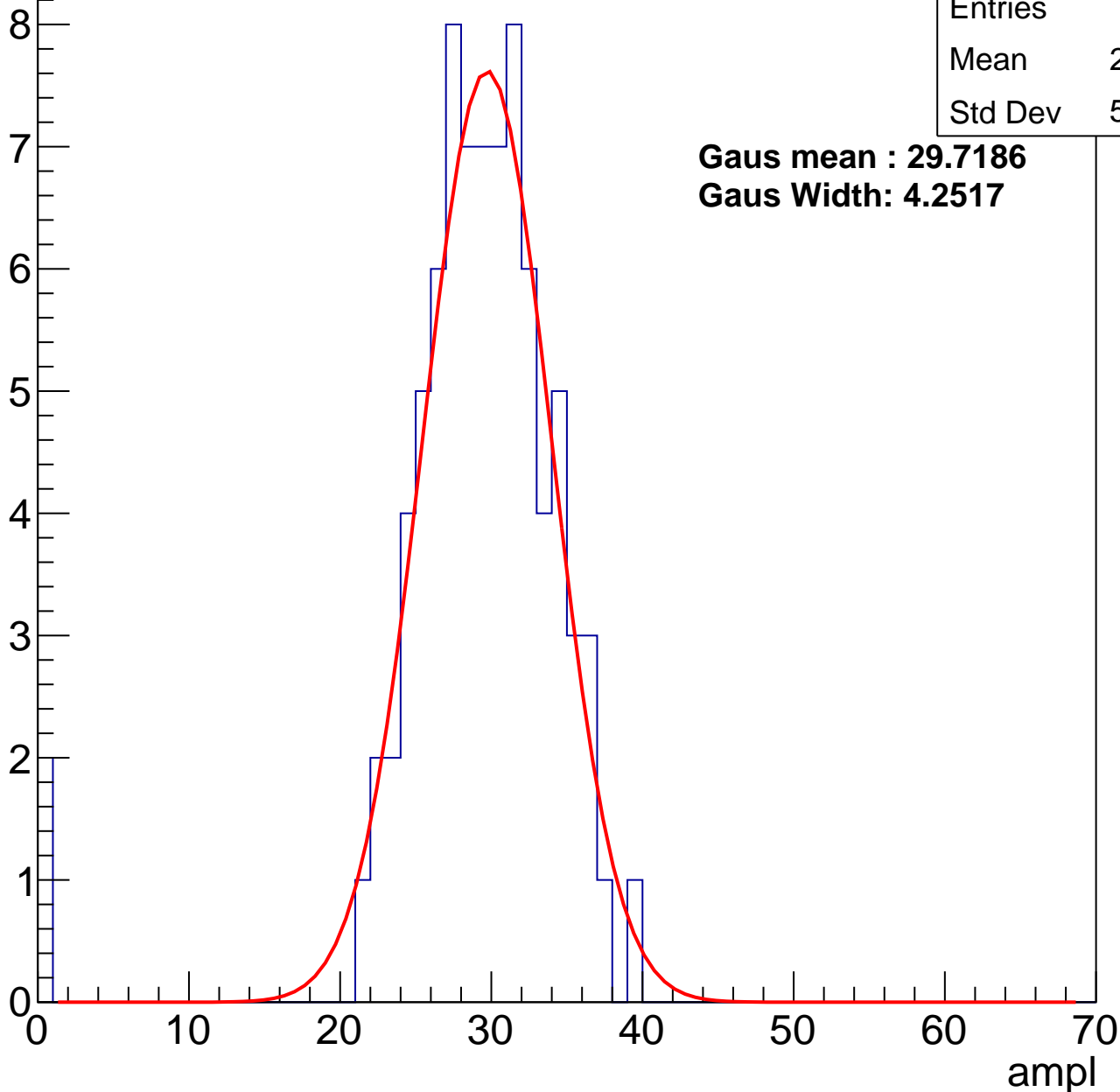
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	82
Mean	28.59
Std Dev	5.922

**Gaus mean : 29.7186**

**Gaus Width: 4.2517**



# B1L102S, U12-ch14, adc1

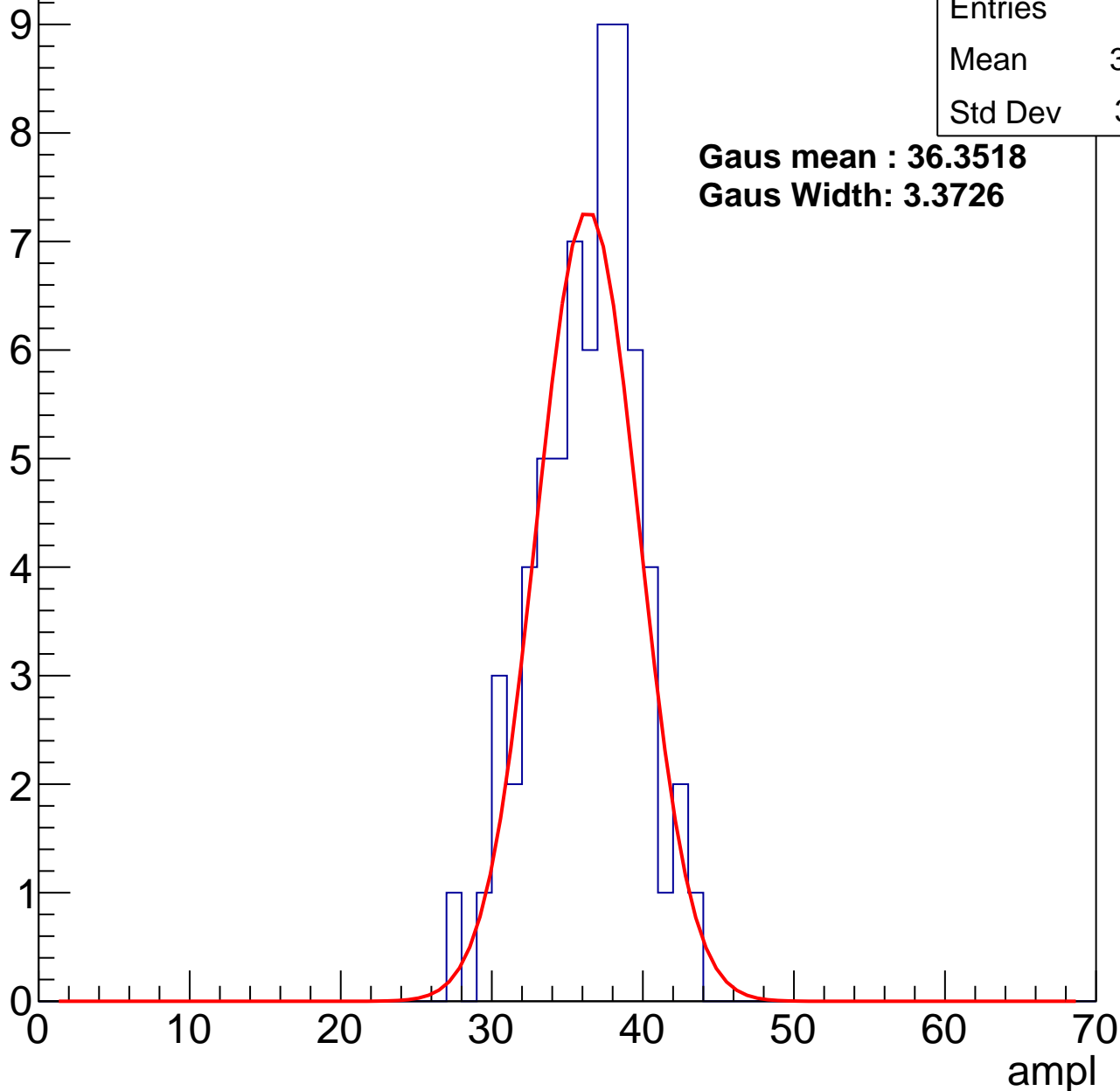
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	35.89
Std Dev	3.331

**Gaus mean : 36.3518**

**Gaus Width: 3.3726**



# B1L102S, U12-ch14, adc2

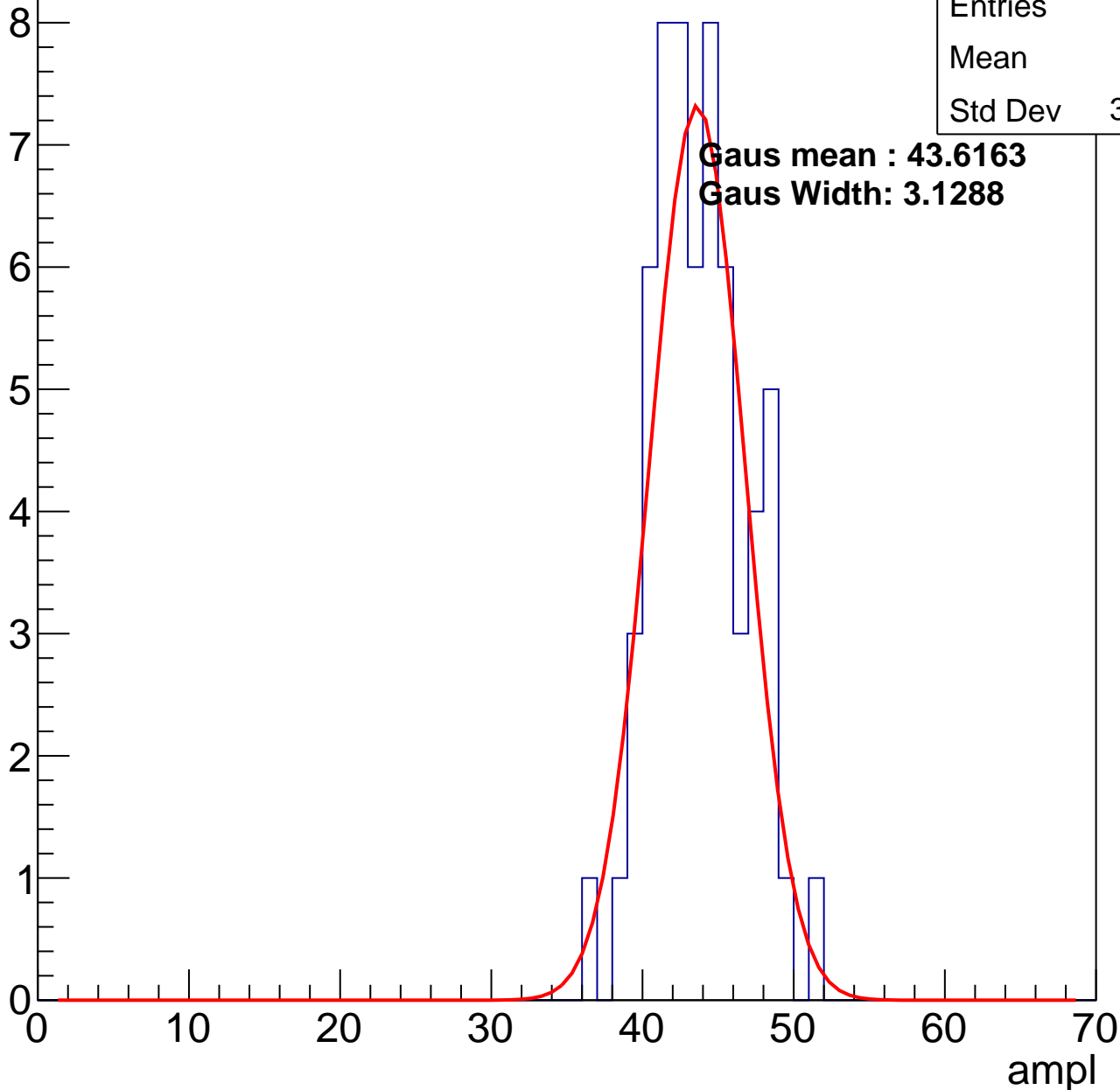
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	43.3
Std Dev	3.026

**Gaus mean : 43.6163**

**Gaus Width: 3.1288**

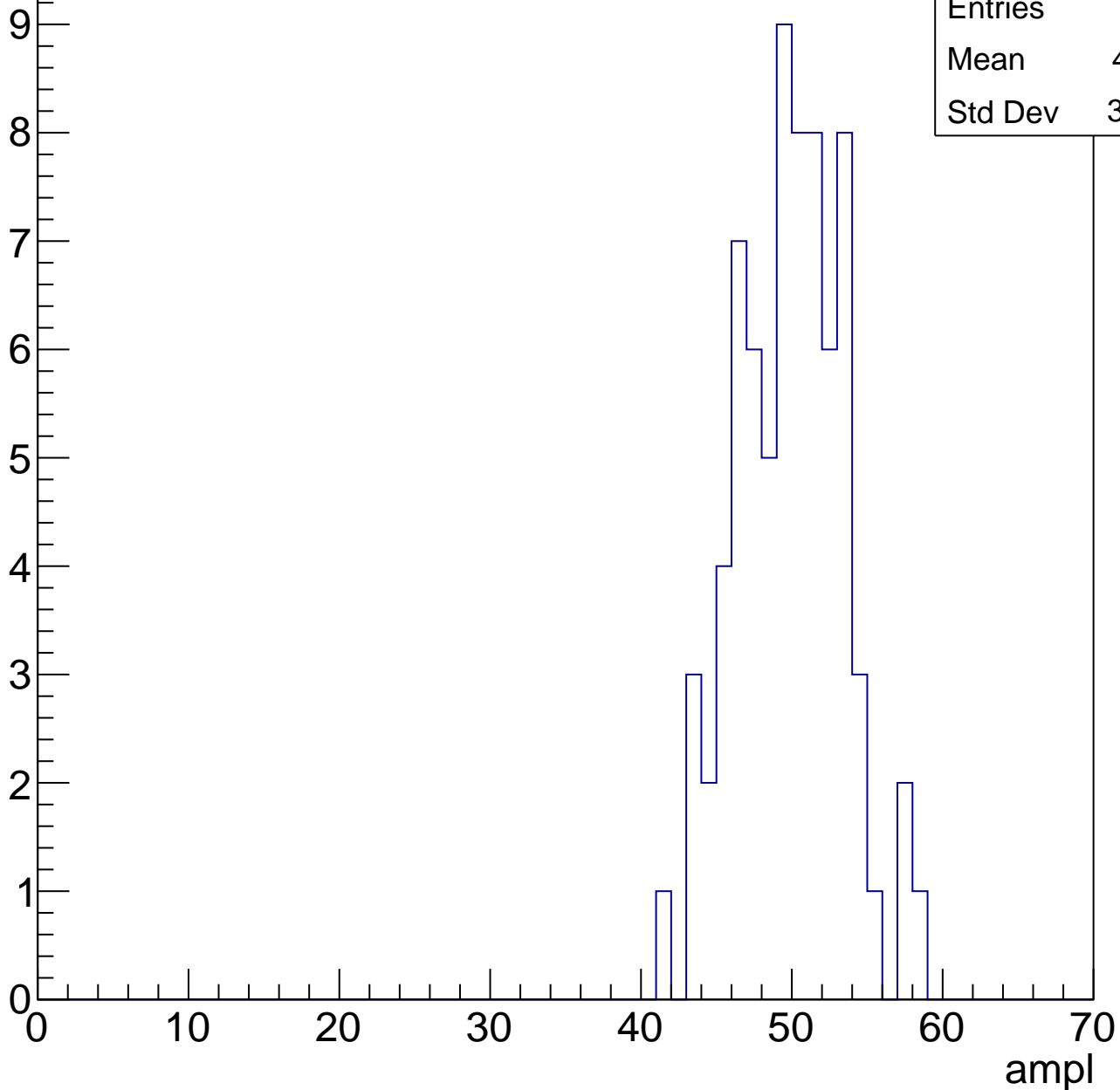


# B1L102S, U12-ch14, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	74
Mean	49.41
Std Dev	3.503

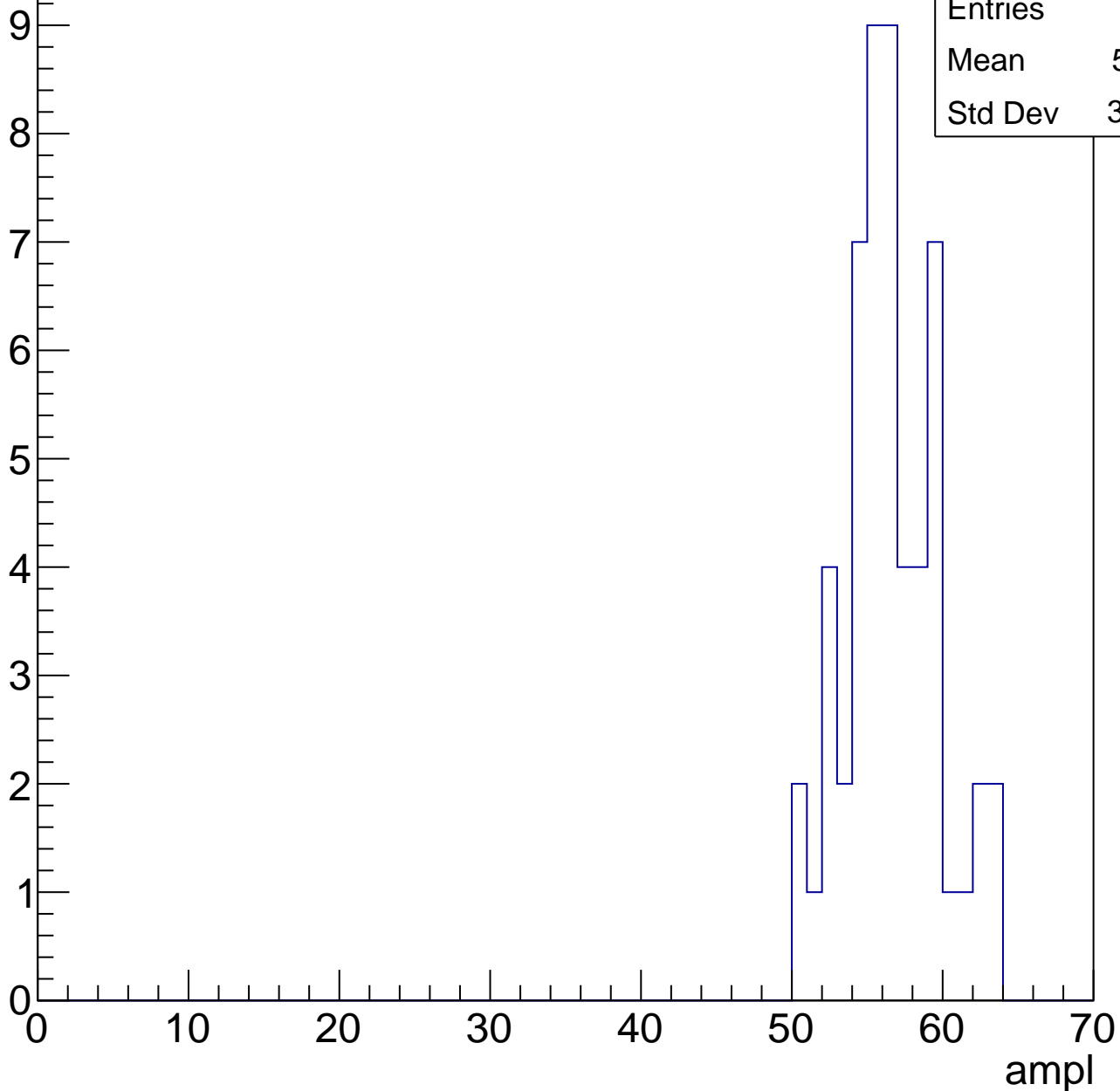


# B1L102S, U12-ch14, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	55
Mean	56.11
Std Dev	3.043

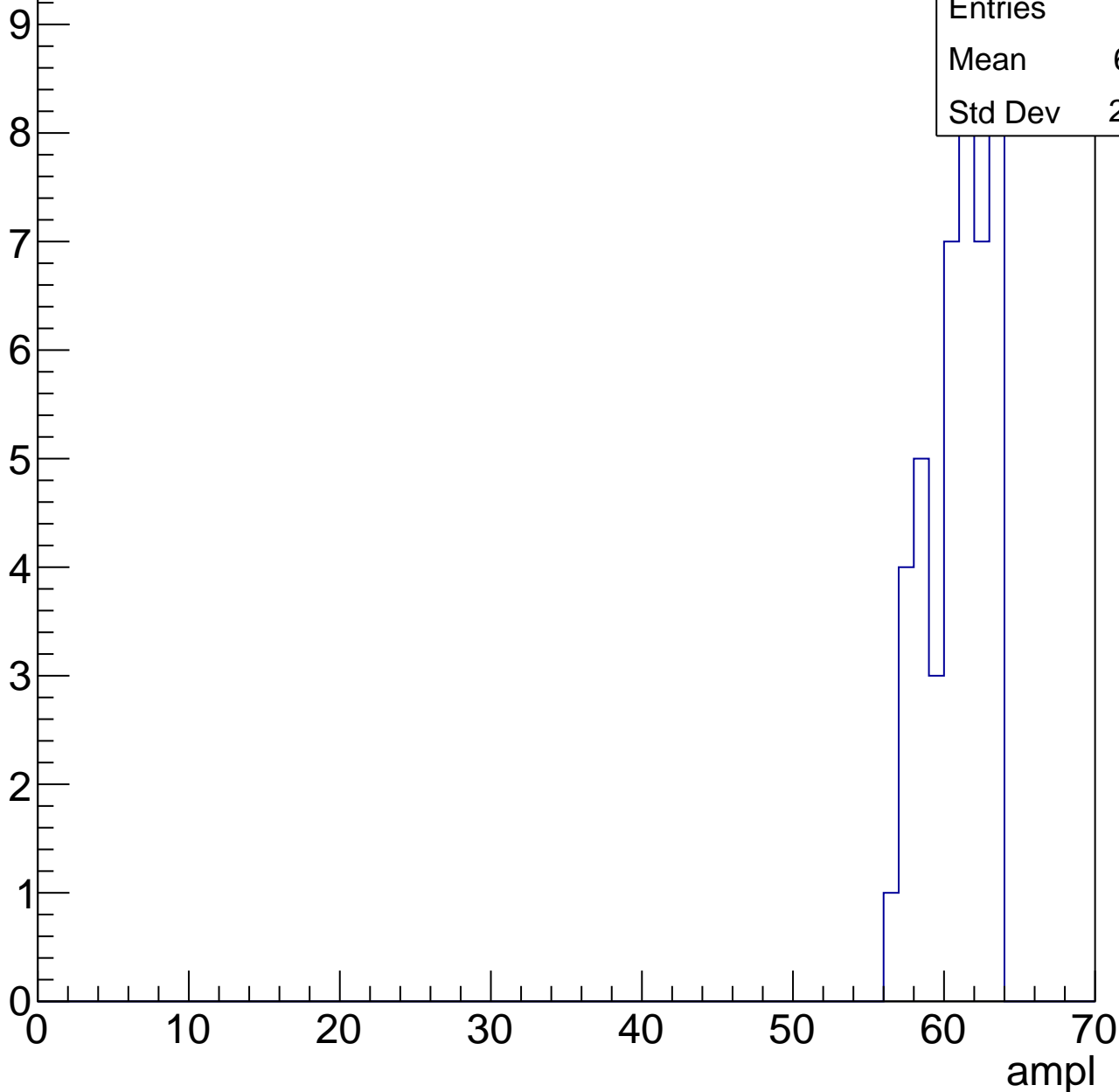


# B1L102S, U12-ch14, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

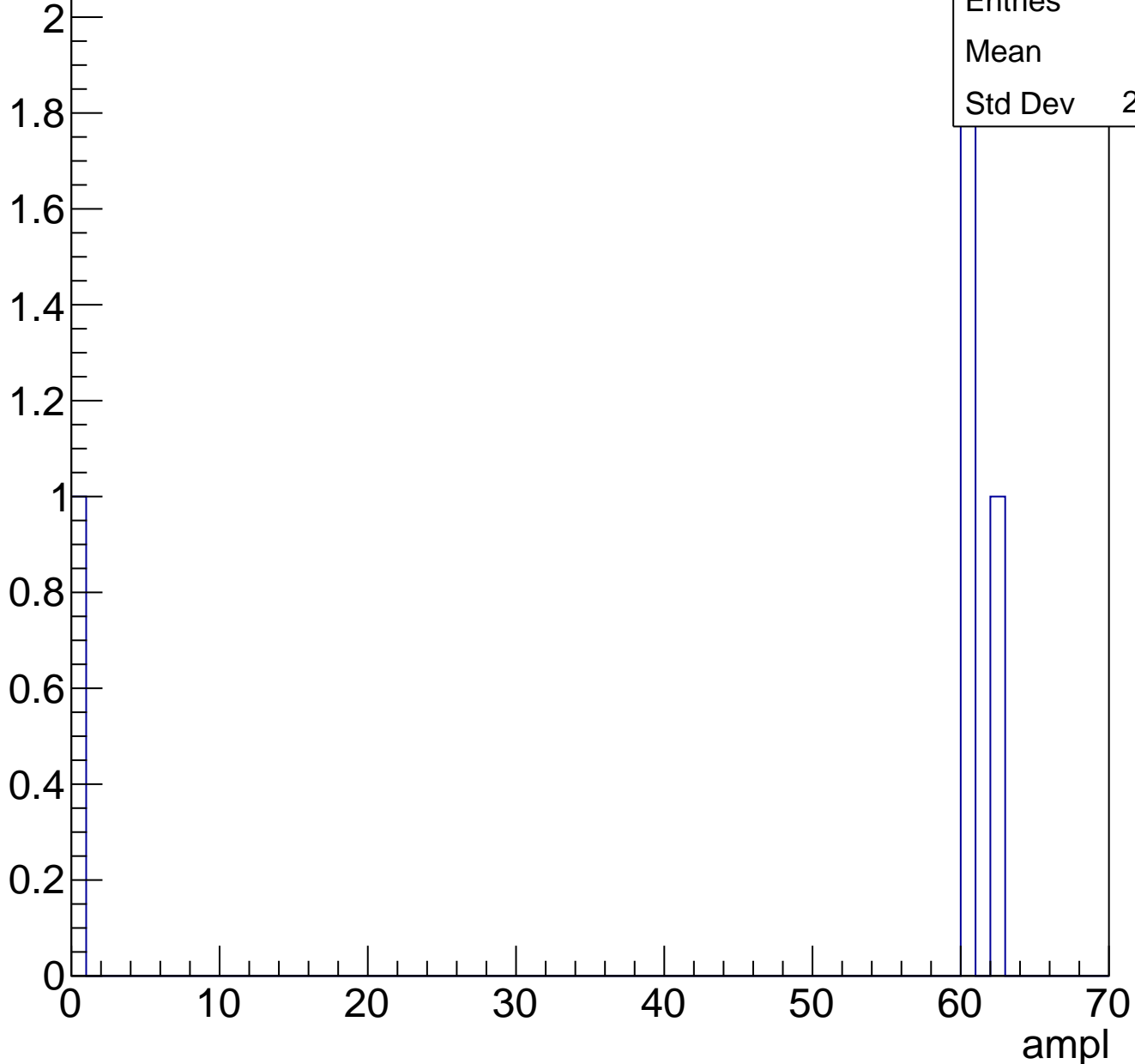
Entries	44
Mean	60.41
Std Dev	2.004



# B1L102S, U12-ch14, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	4
Mean	45.5
Std Dev	26.28



# B1L102S, U12-ch14, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L102S, U12-ch15, adc0

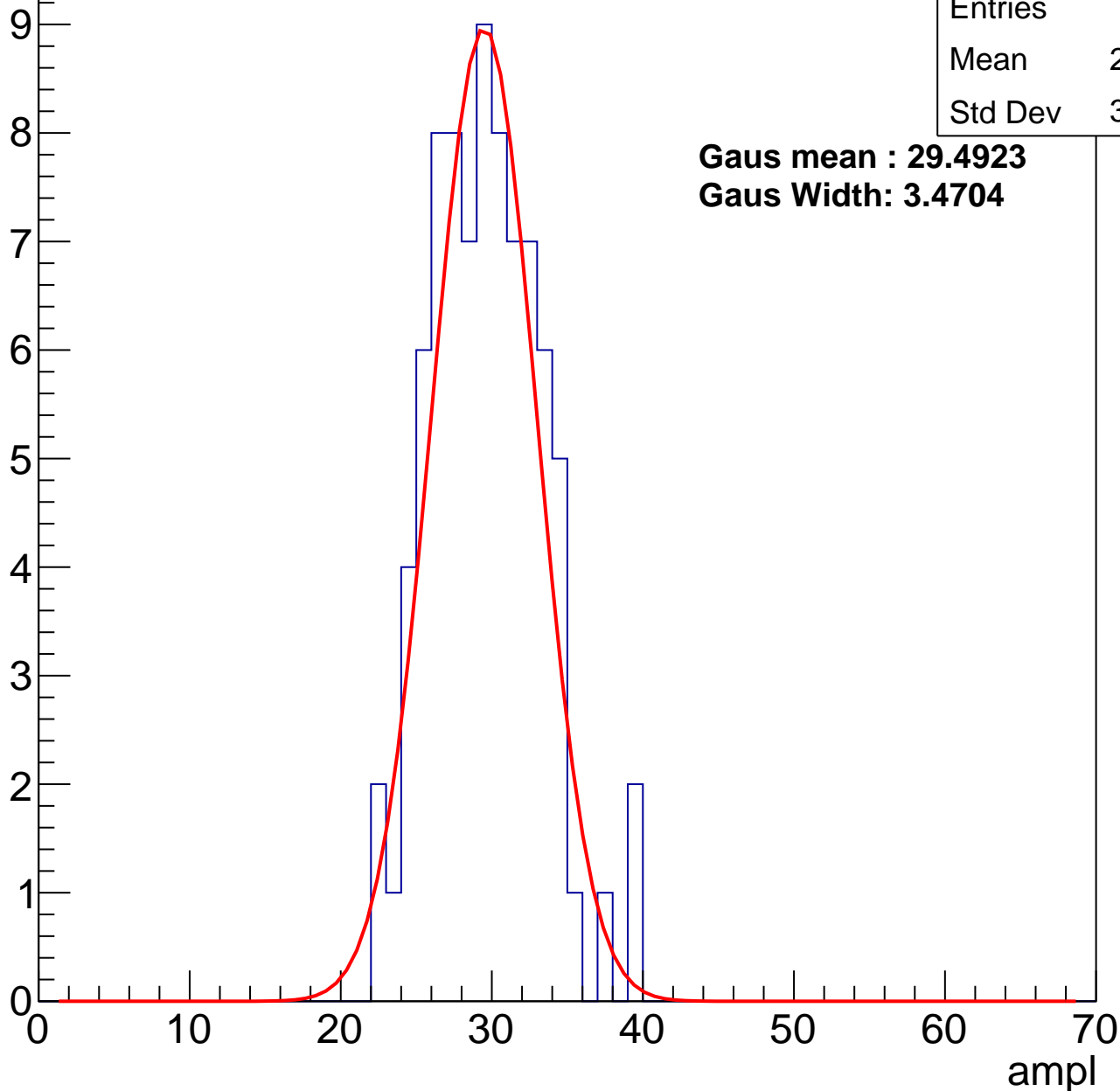
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	82
Mean	29.18
Std Dev	3.592

**Gaus mean : 29.4923**

**Gaus Width: 3.4704**



# B1L102S, U12-ch15, adc1

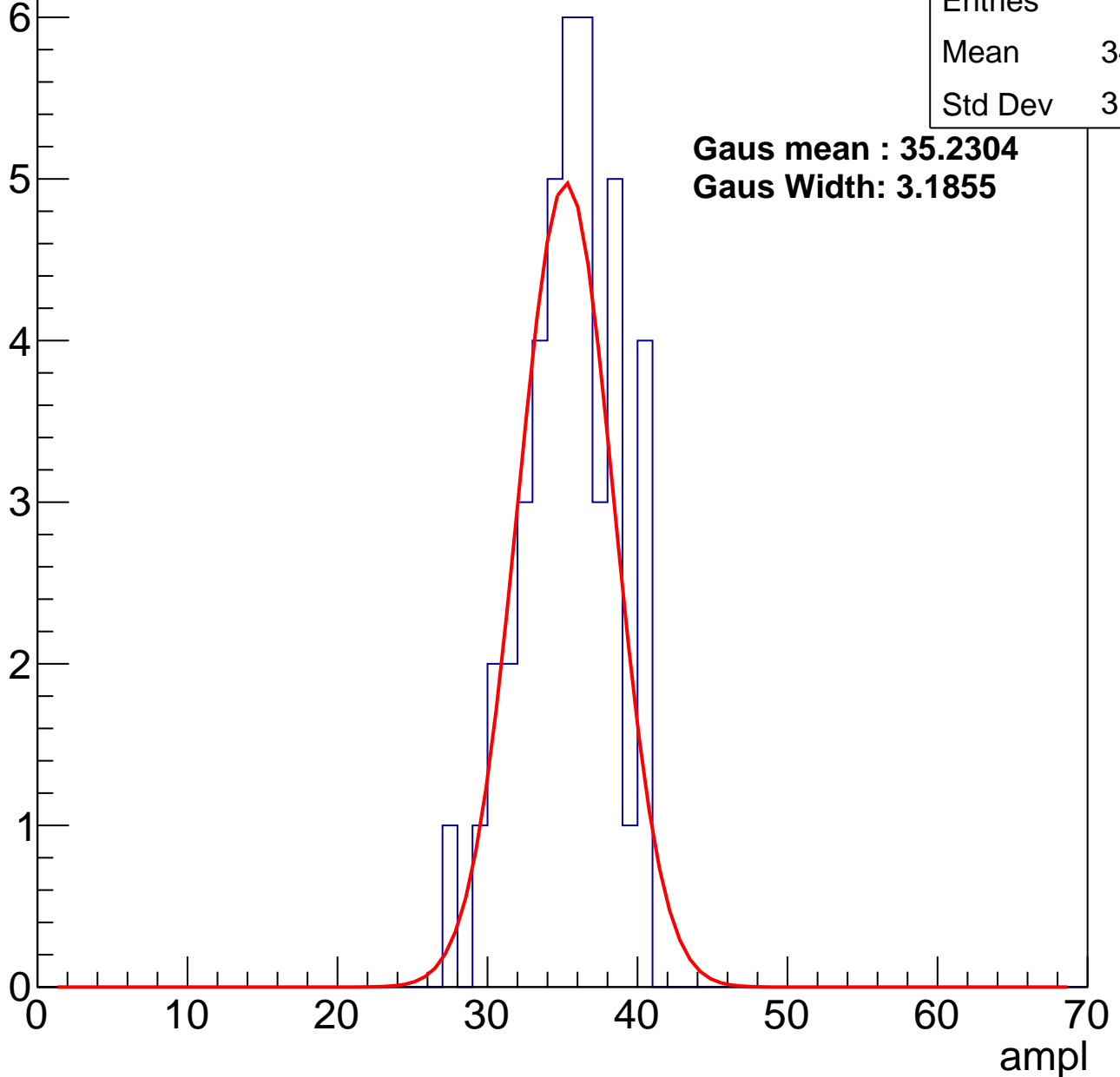
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	43
Mean	34.93
Std Dev	3.083

**Gaus mean : 35.2304**

**Gaus Width: 3.1855**



# B1L102S, U12-ch15, adc2

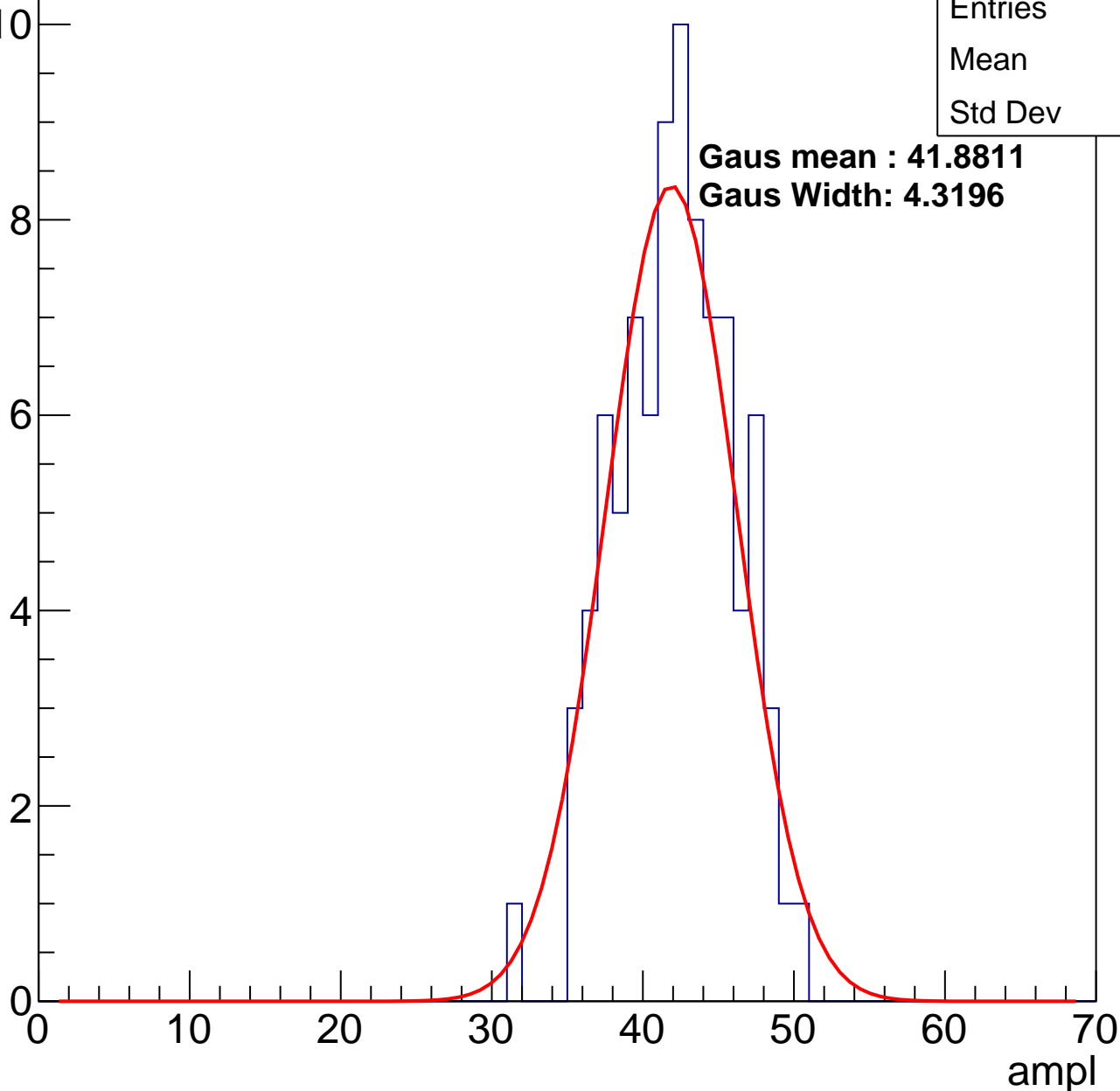
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	88
Mean	41.7
Std Dev	3.79

**Gaus mean : 41.8811**

**Gaus Width: 4.3196**

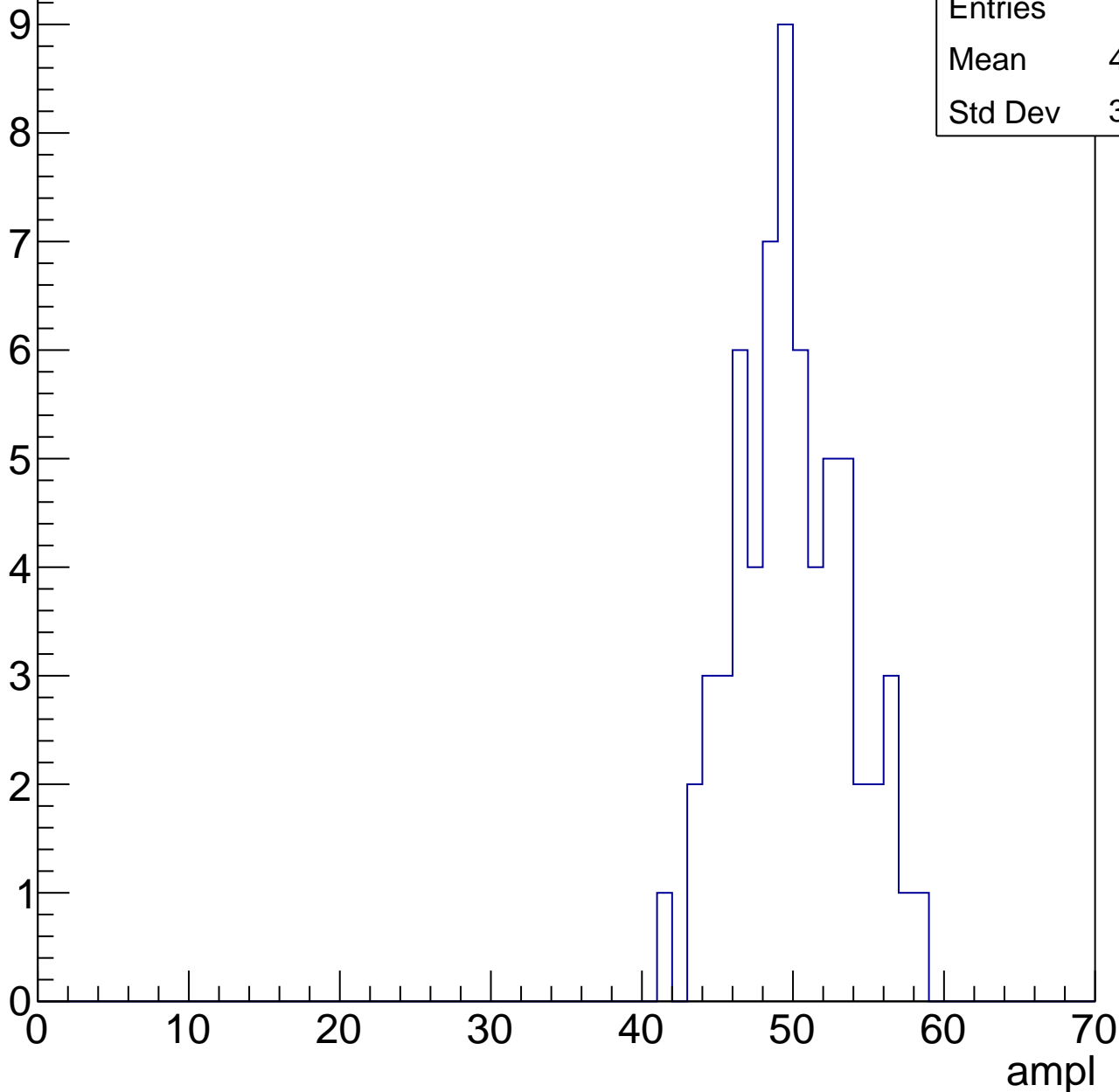


# B1L102S, U12-ch15, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	49.45
Std Dev	3.716

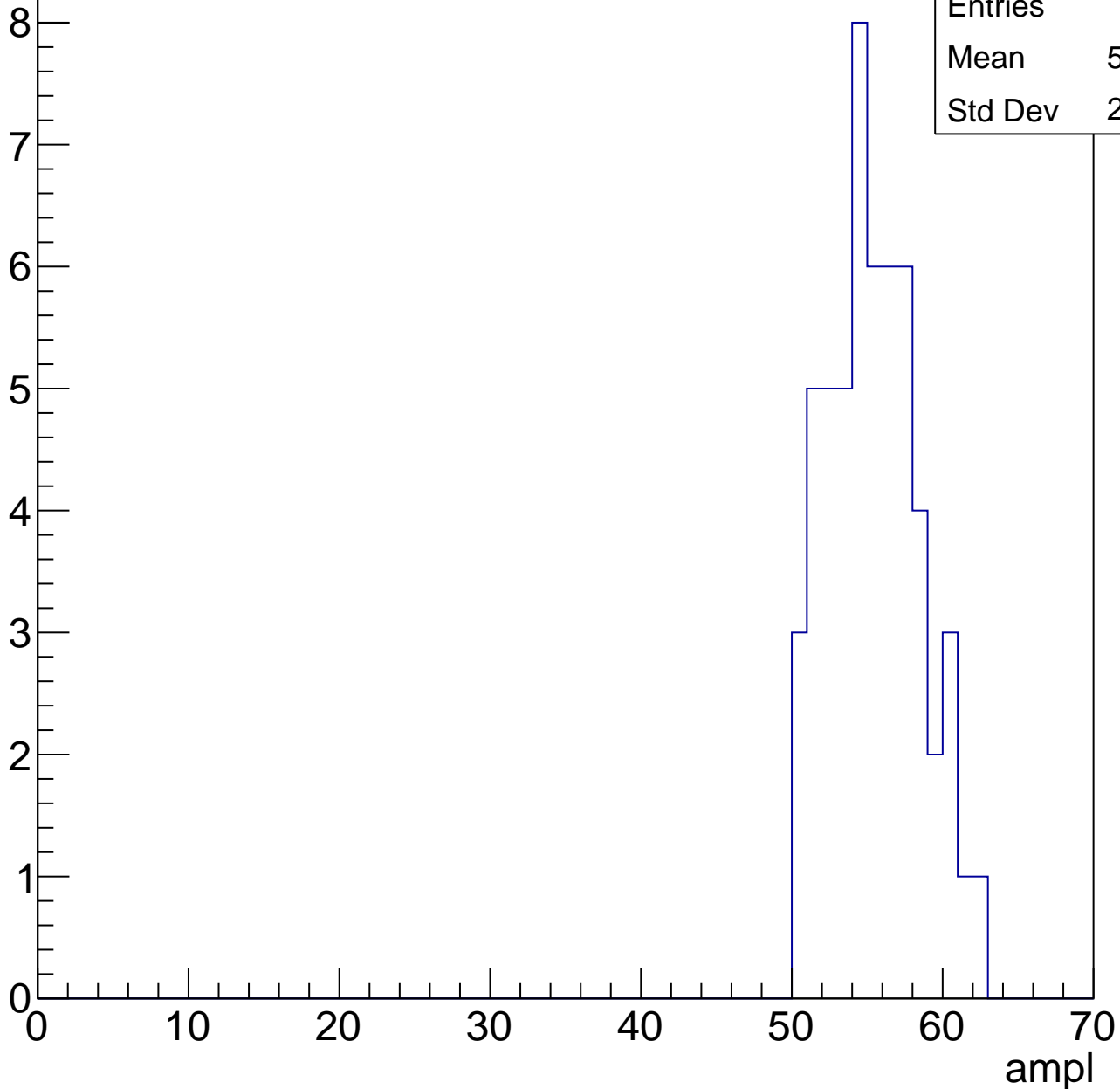


# B1L102S, U12-ch15, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	55
Mean	54.96
Std Dev	2.972

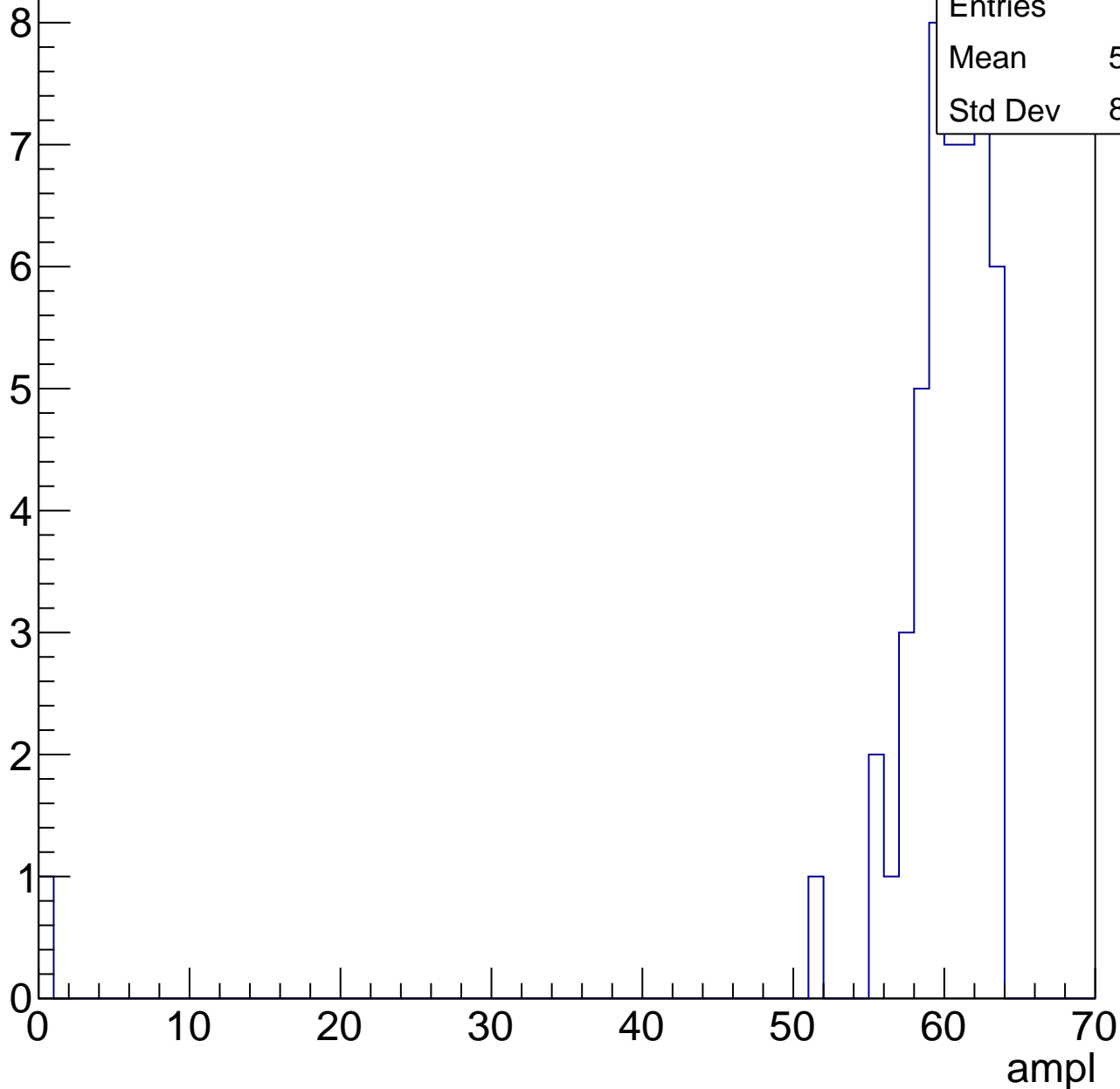


# B1L102S, U12-ch15, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

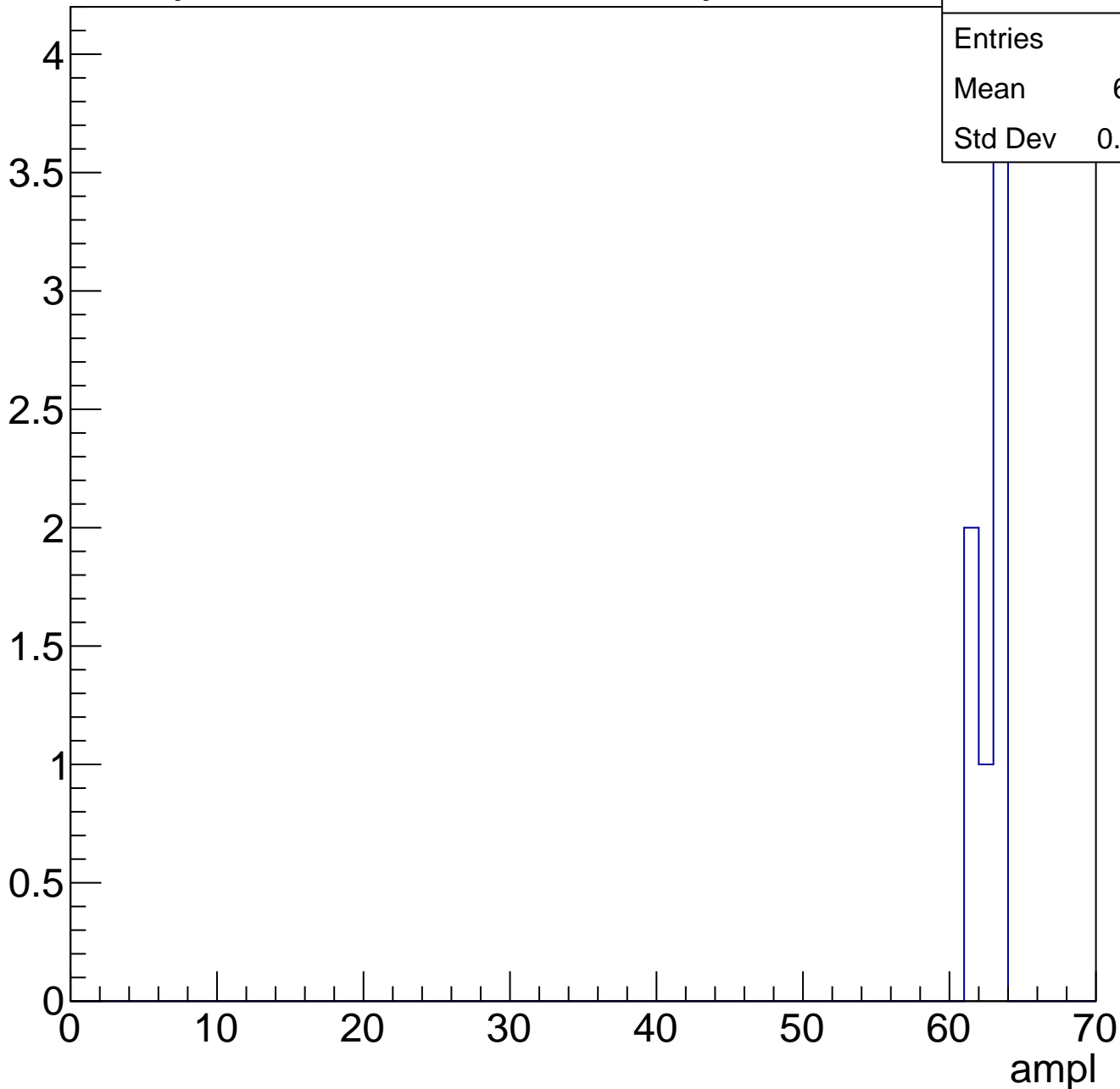
Entries	49
Mean	58.59
Std Dev	8.804



# B1L102S, U12-ch15, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U12-ch15, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U12-ch16, adc0

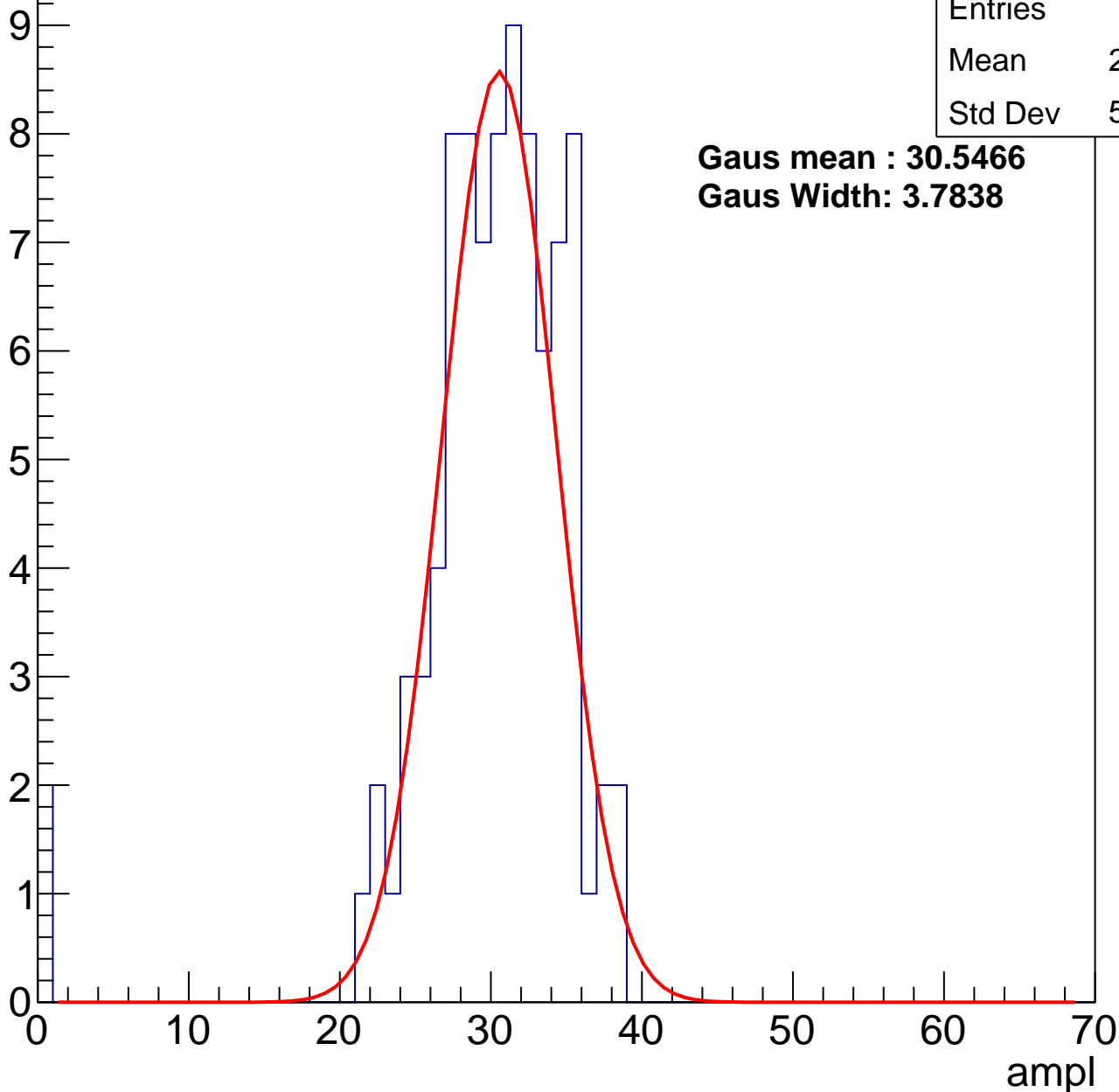
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	90
Mean	29.54
Std Dev	5.837

**Gaus mean : 30.5466**

**Gaus Width: 3.7838**



# B1L102S, U12-ch16, adc1

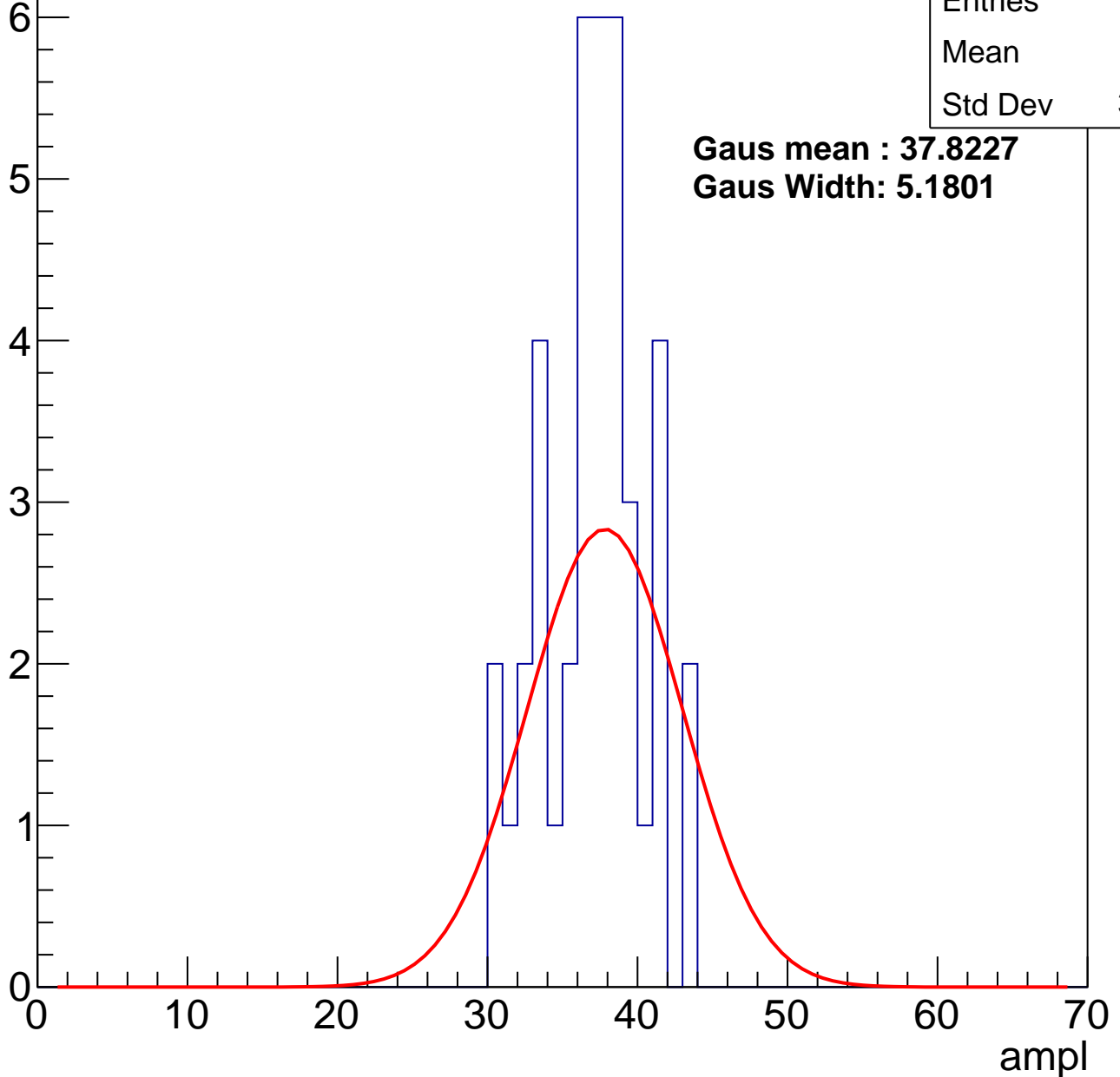
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	40
Mean	36.6
Std Dev	3.27

**Gaus mean : 37.8227**

**Gaus Width: 5.1801**



# B1L102S, U12-ch16, adc2

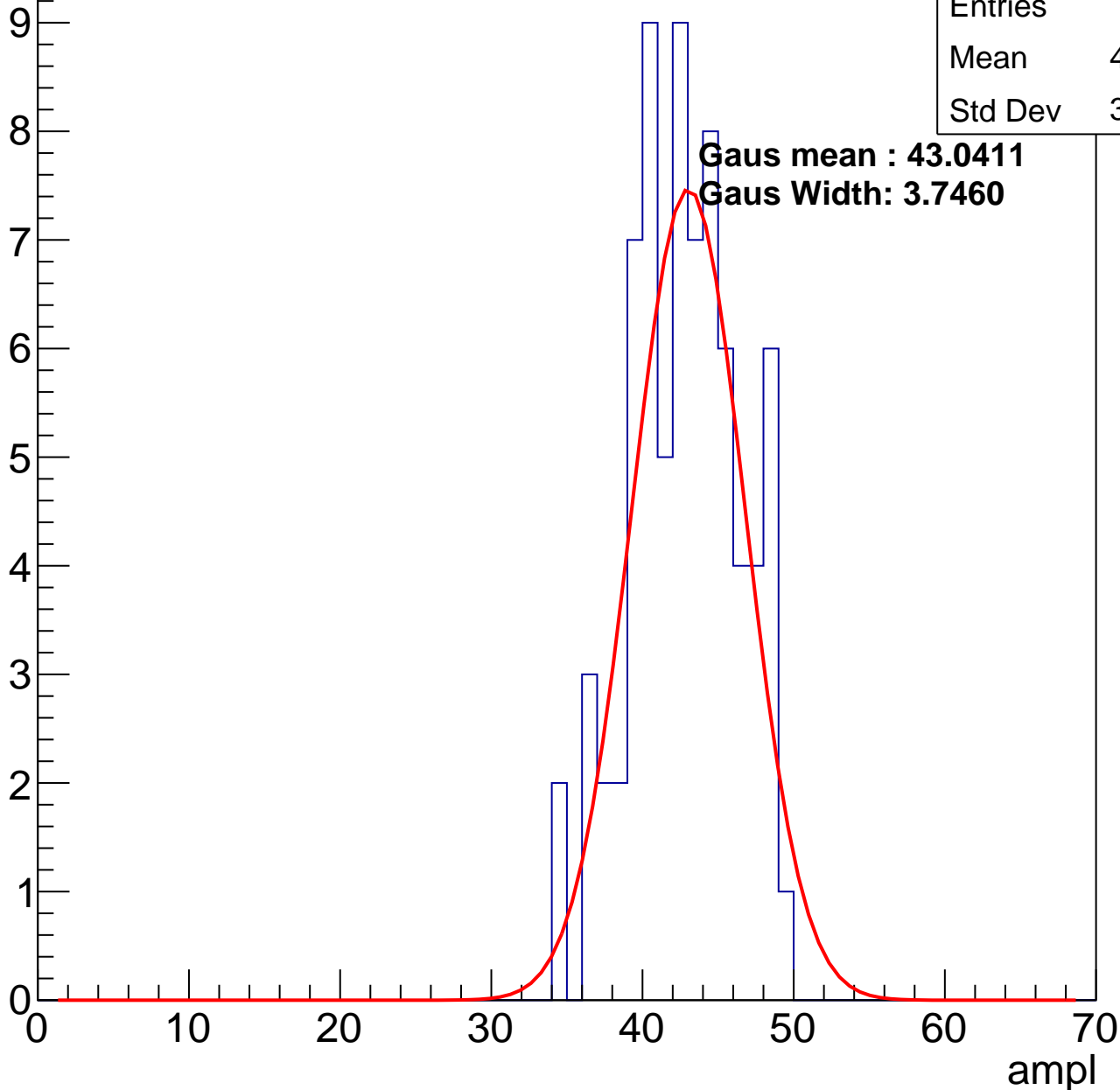
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	75
Mean	42.32
Std Dev	3.533

**Gaus mean : 43.0411**

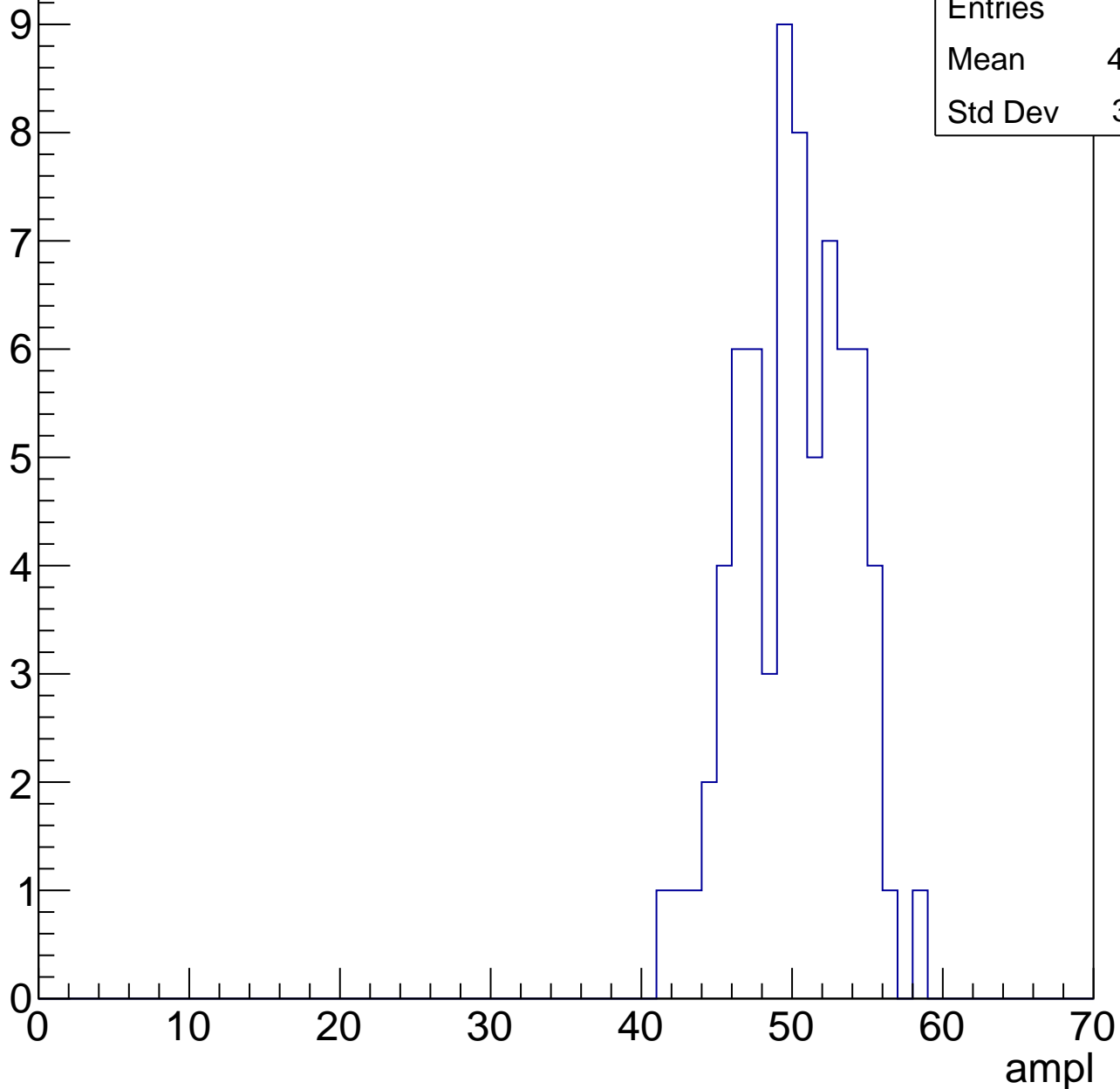
**Gaus Width: 3.7460**



# B1L102S, U12-ch16, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



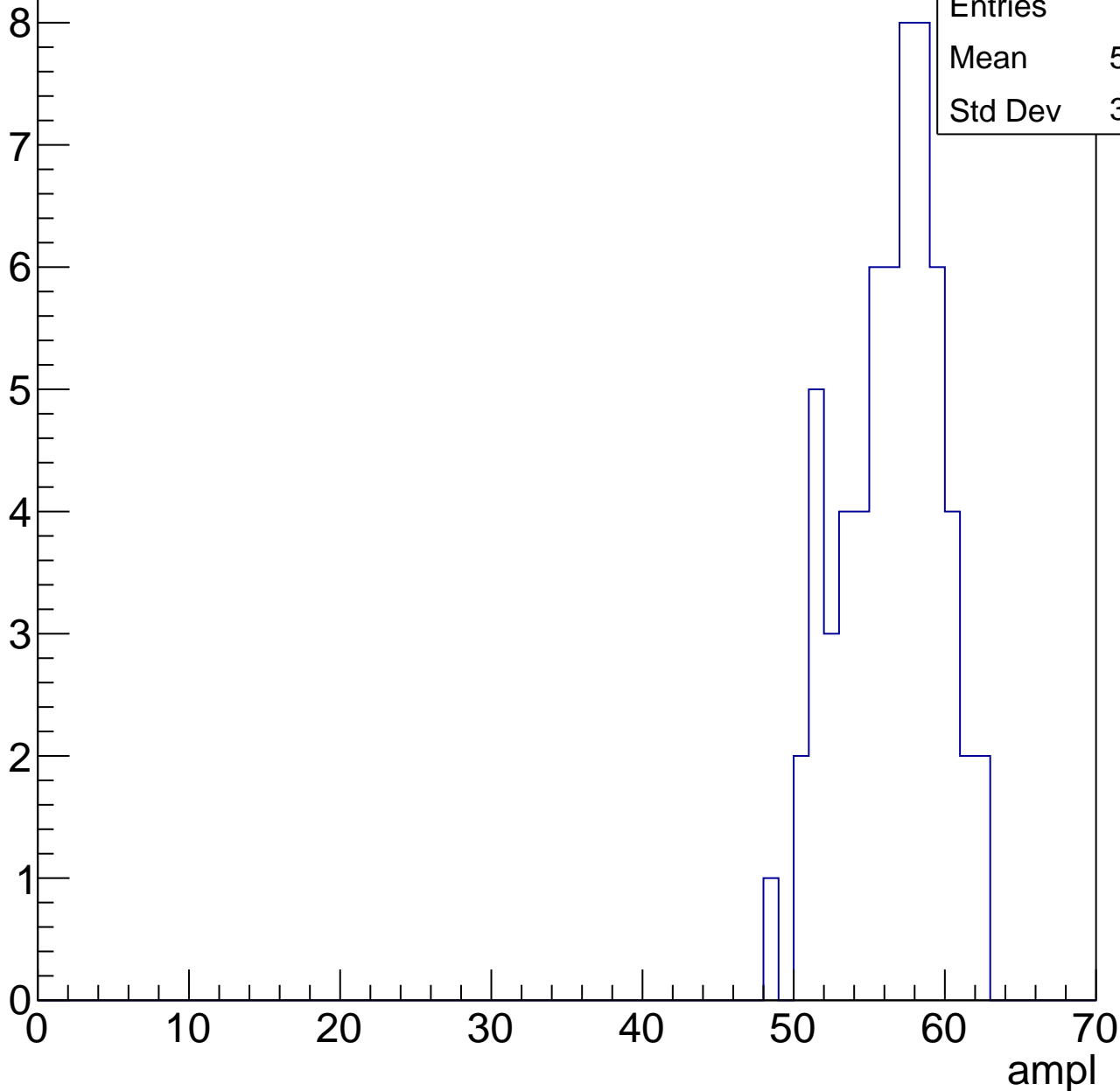
Entries	71
Mean	49.75
Std Dev	3.591

# B1L102S, U12-ch16, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	55.95
Std Dev	3.256

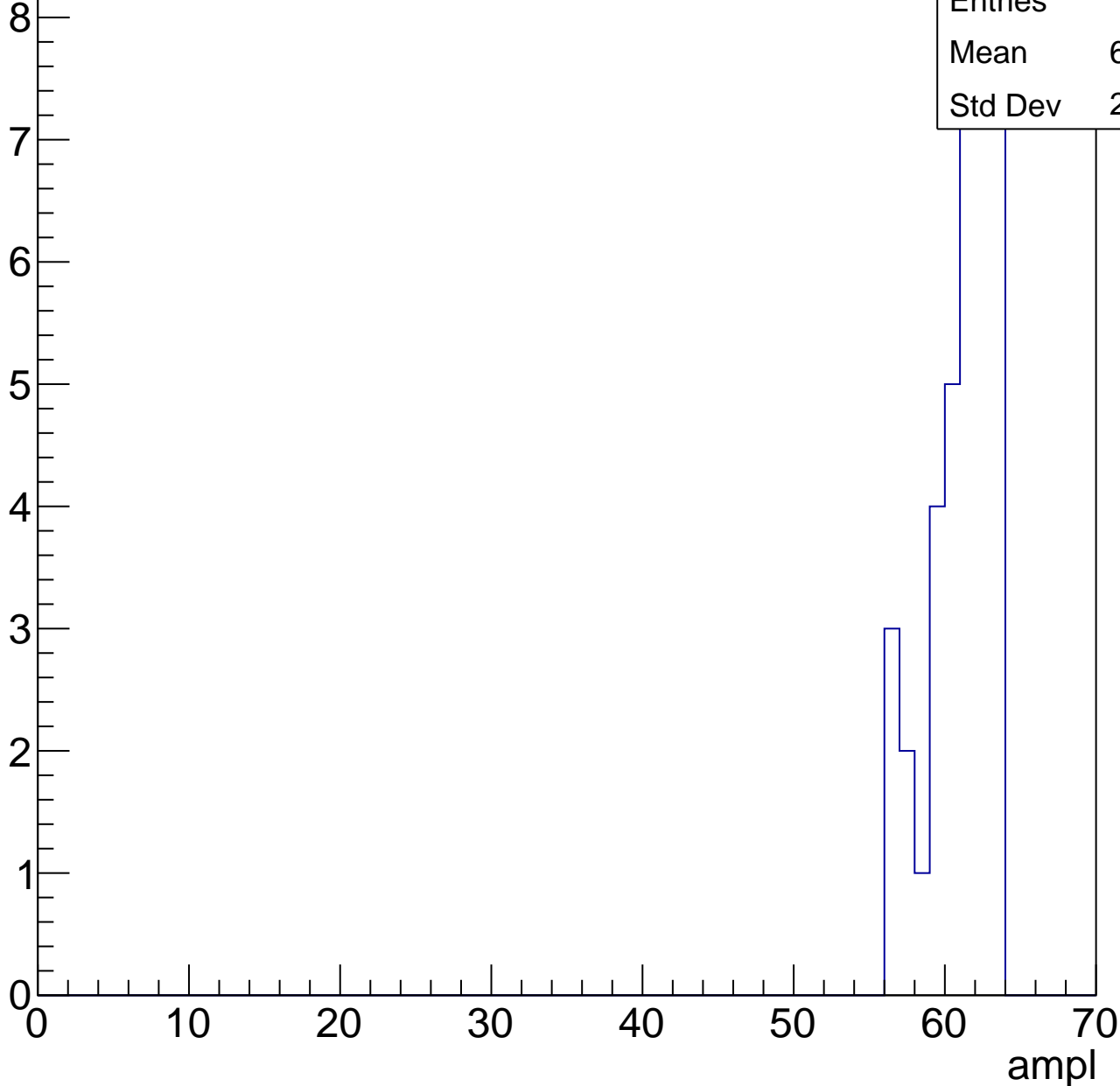


# B1L102S, U12-ch16, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

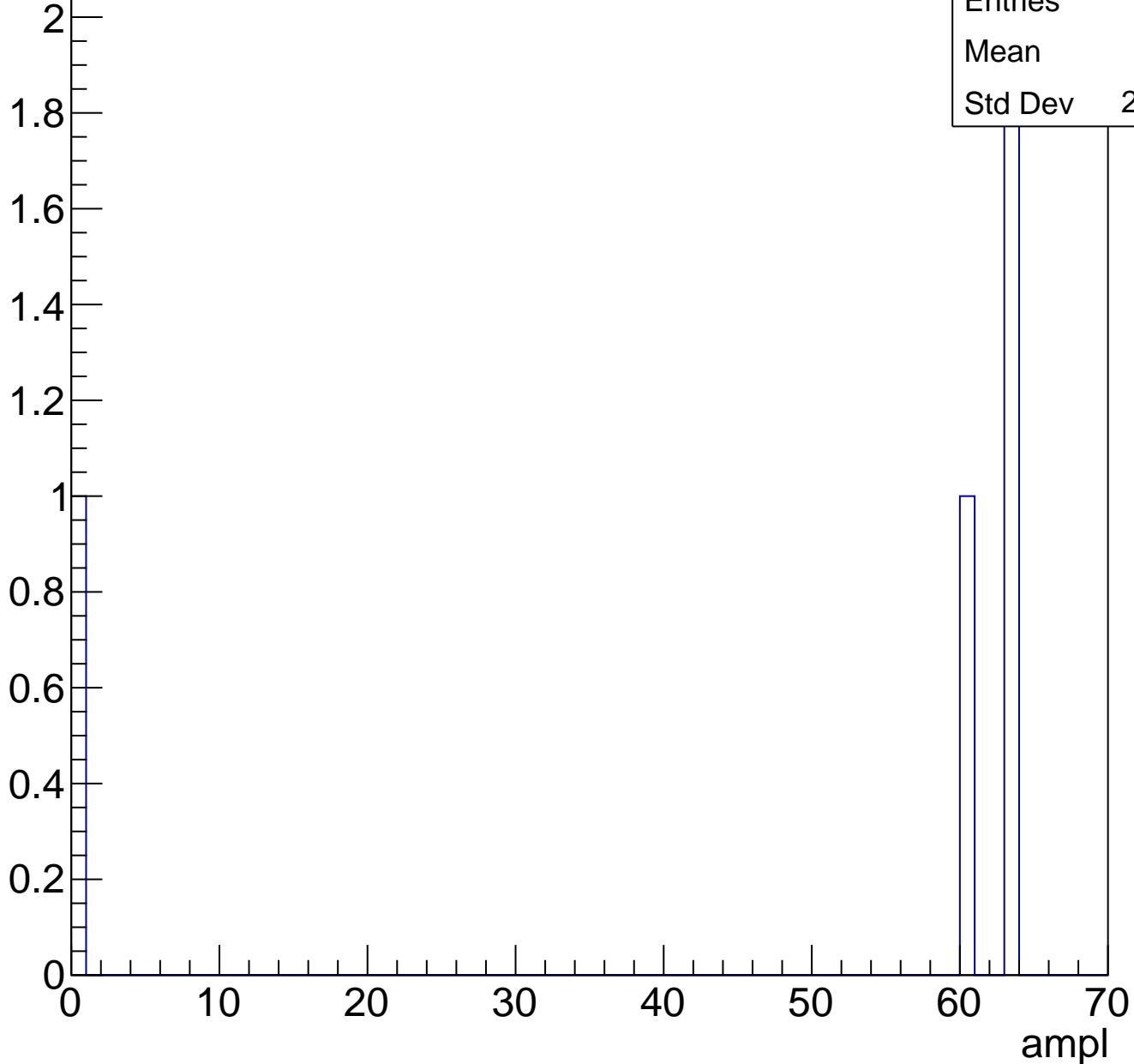
Entries	39
Mean	60.62
Std Dev	2.095



# B1L102S, U12-ch16, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U12-ch16, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U12-ch17, adc0

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	69
Mean	30.33
Std Dev	3.091

**Gaus mean : 31.3074**

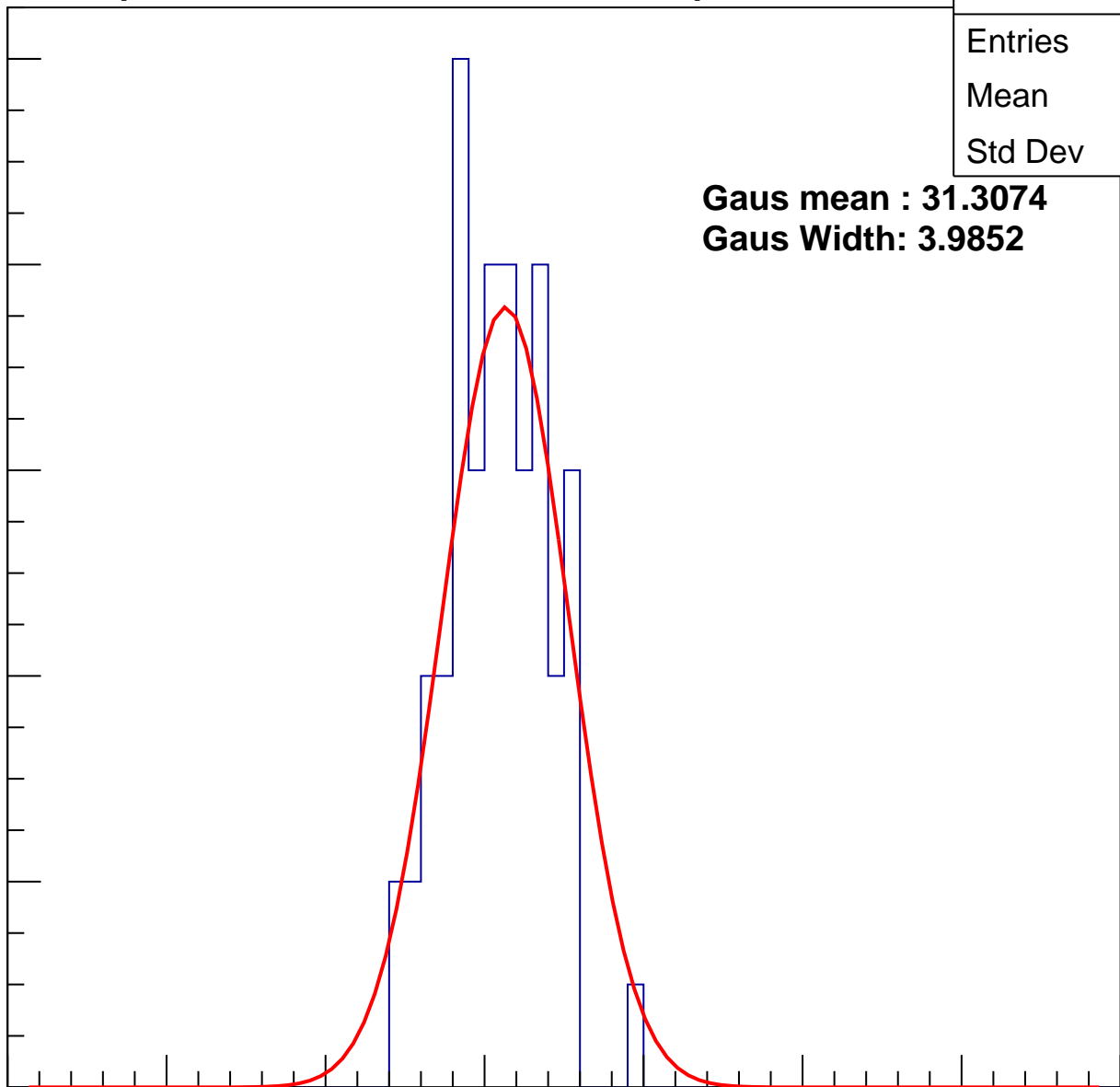
**Gaus Width: 3.9852**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L102S, U12-ch17, adc1

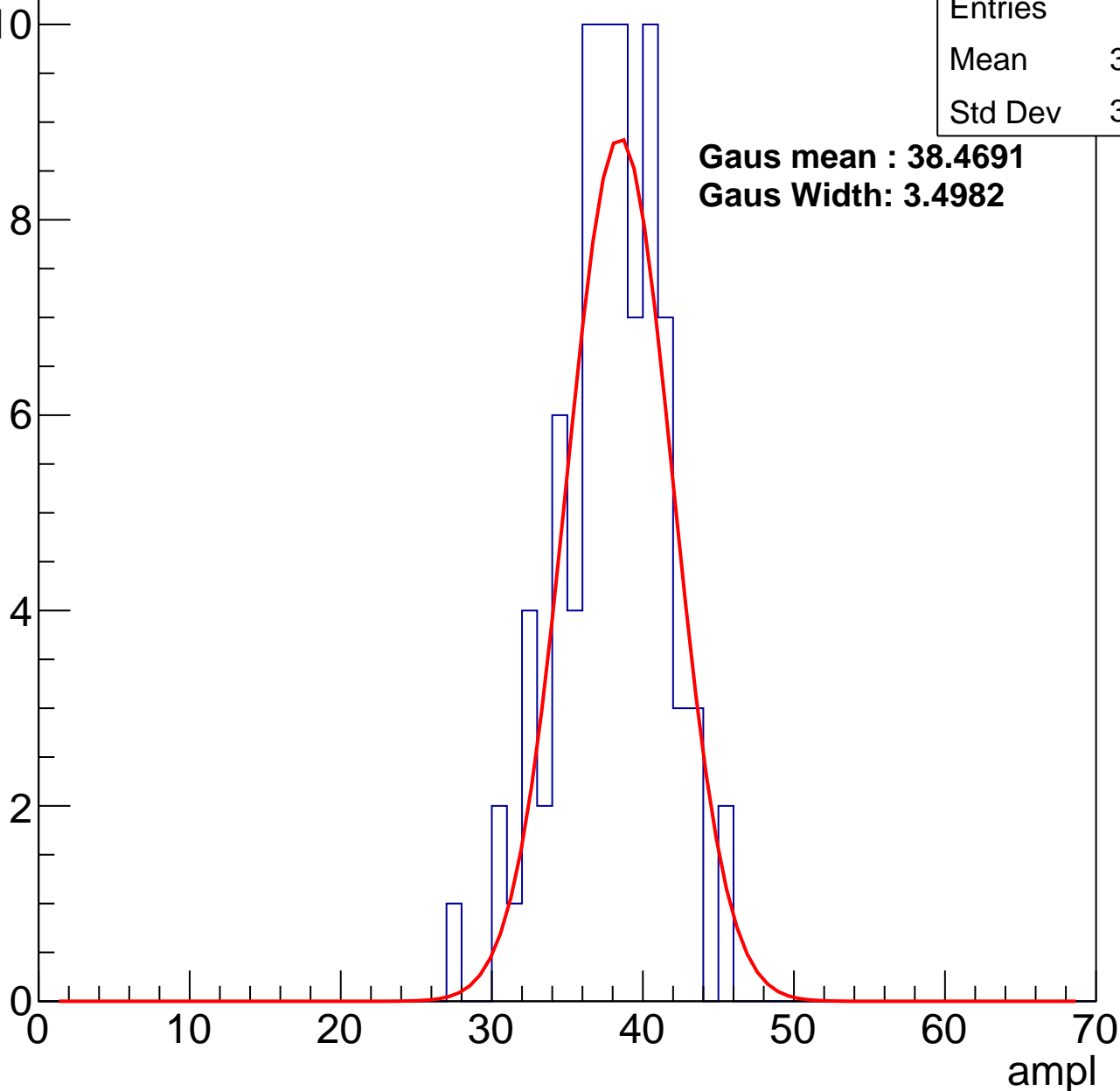
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	82
Mean	37.45
Std Dev	3.458

**Gaus mean : 38.4691**

**Gaus Width: 3.4982**



# B1L102S, U12-ch17, adc2

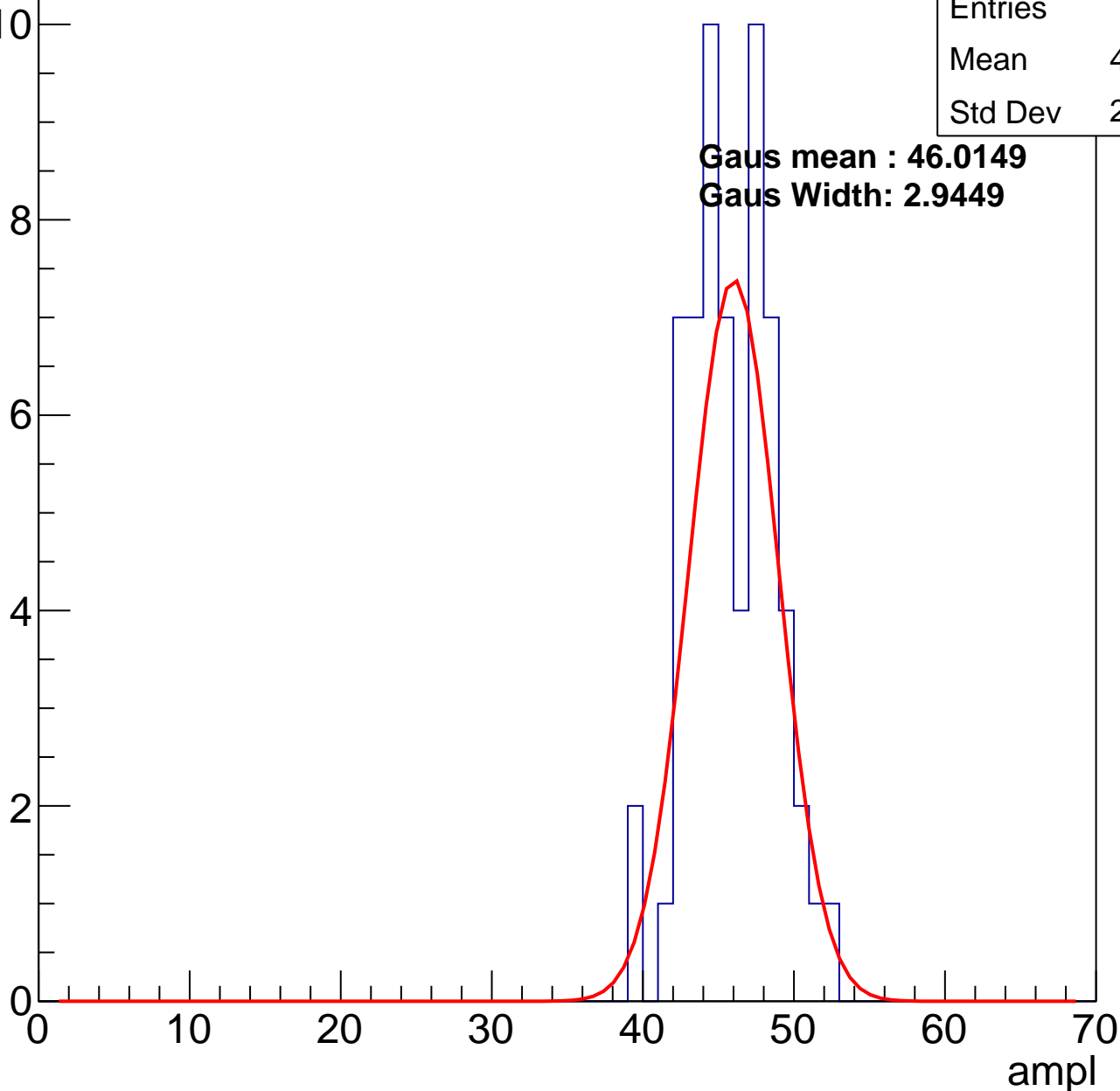
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	63
Mean	45.37
Std Dev	2.779

**Gaus mean : 46.0149**

**Gaus Width: 2.9449**

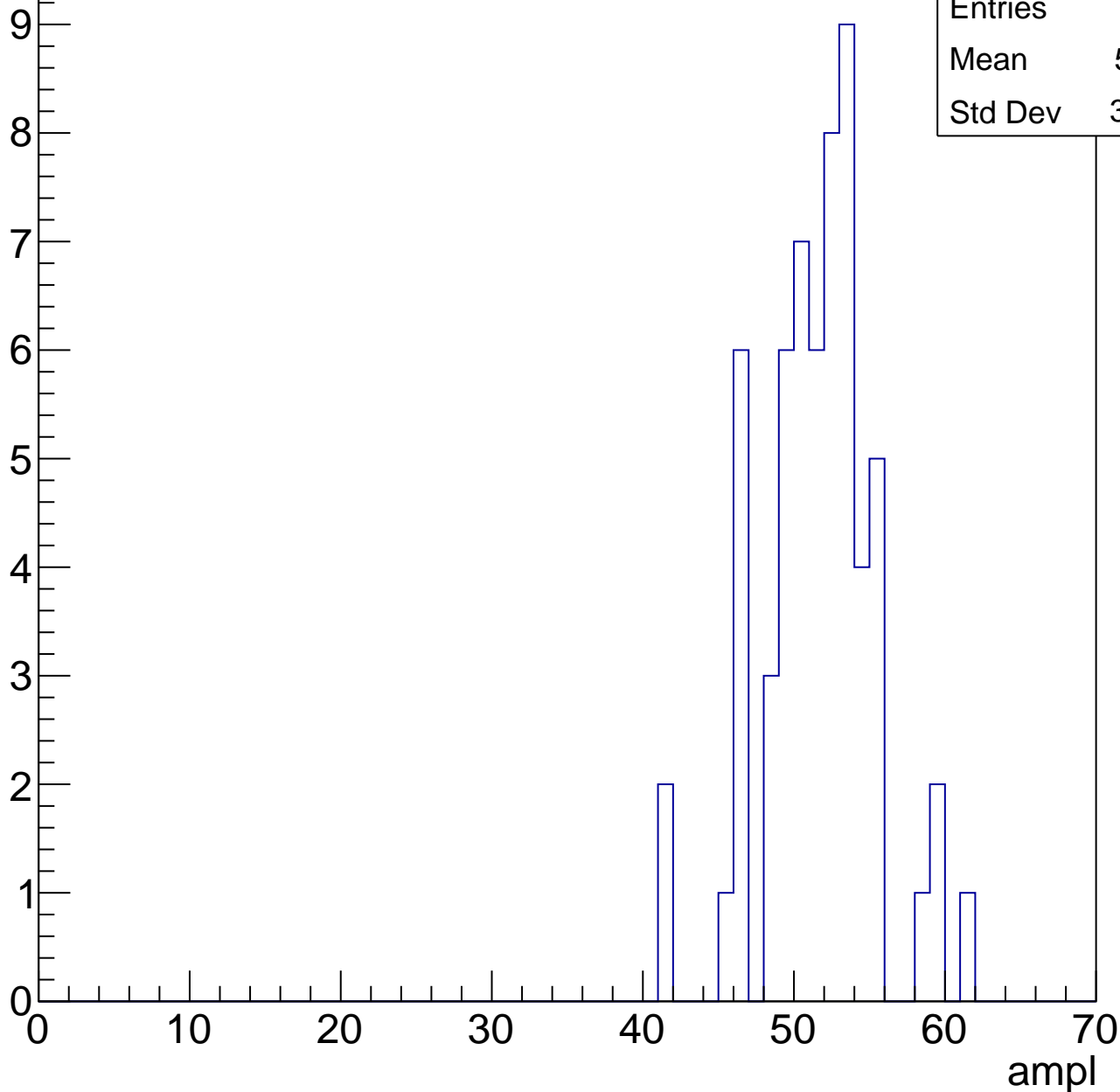


# B1L102S, U12-ch17, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	51.11
Std Dev	3.799

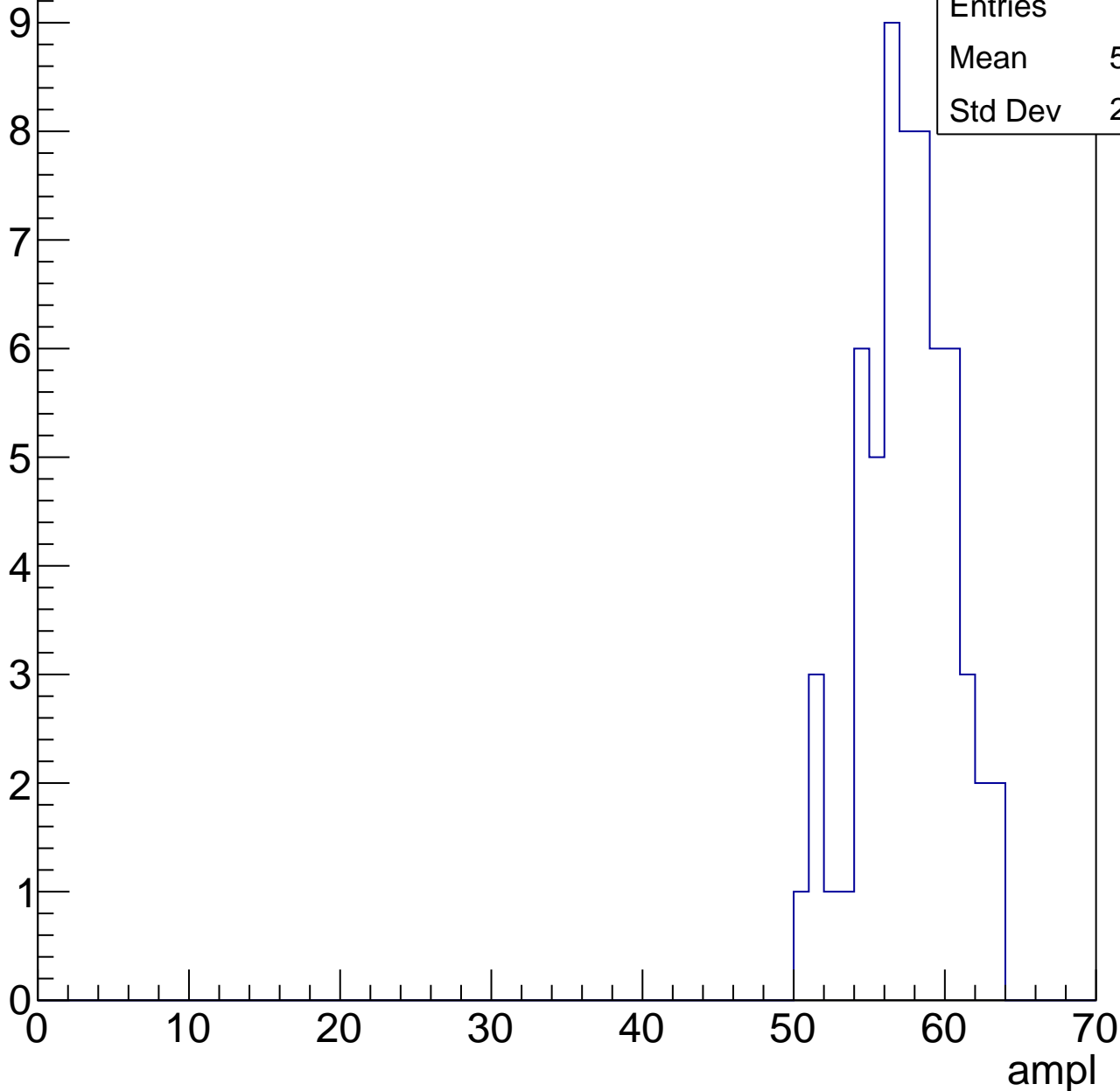


# B1L102S, U12-ch17, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	57.02
Std Dev	2.967

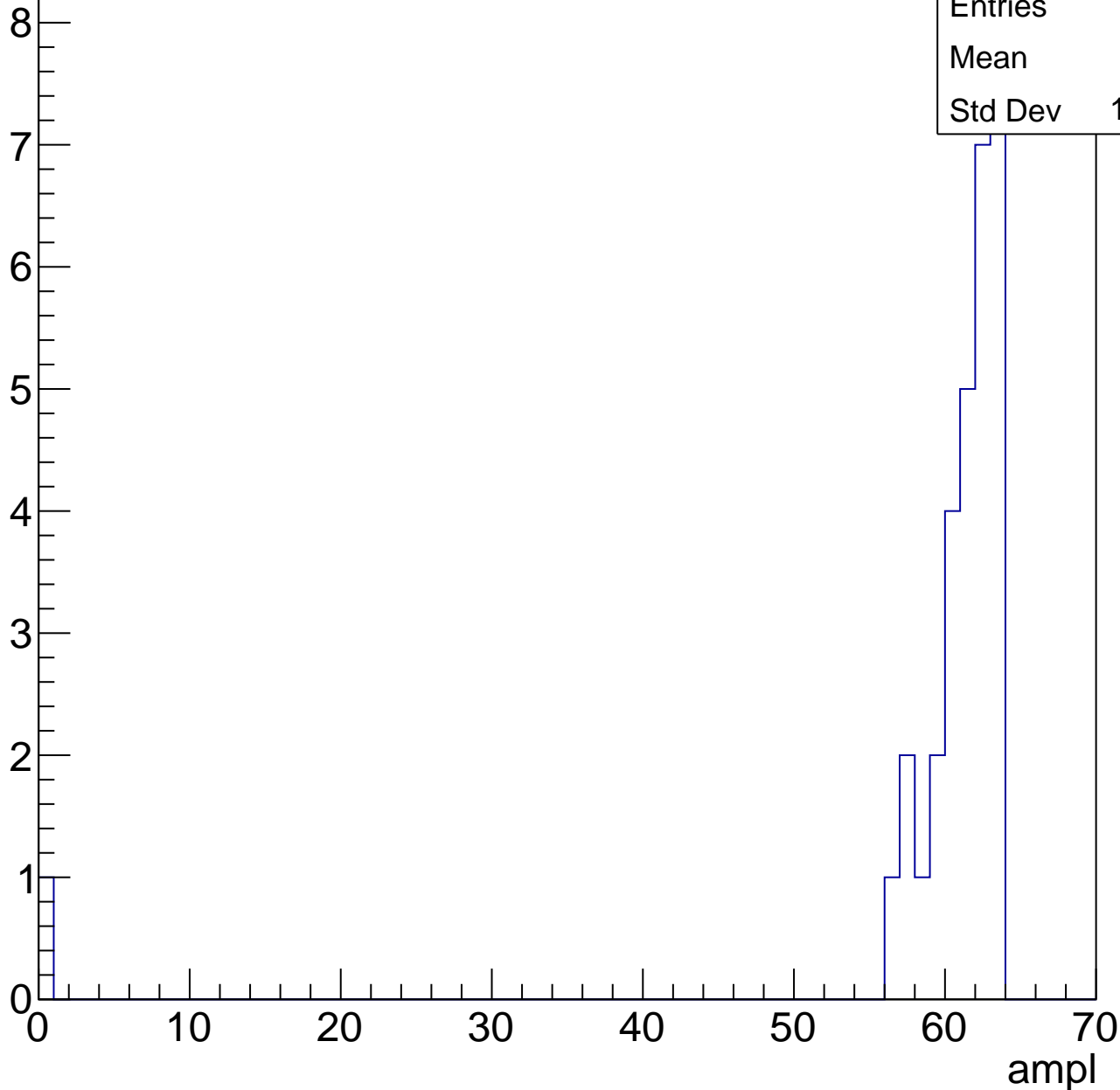


# B1L102S, U12-ch17, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	31
Mean	59
Std Dev	10.95



# B1L102S, U12-ch17, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

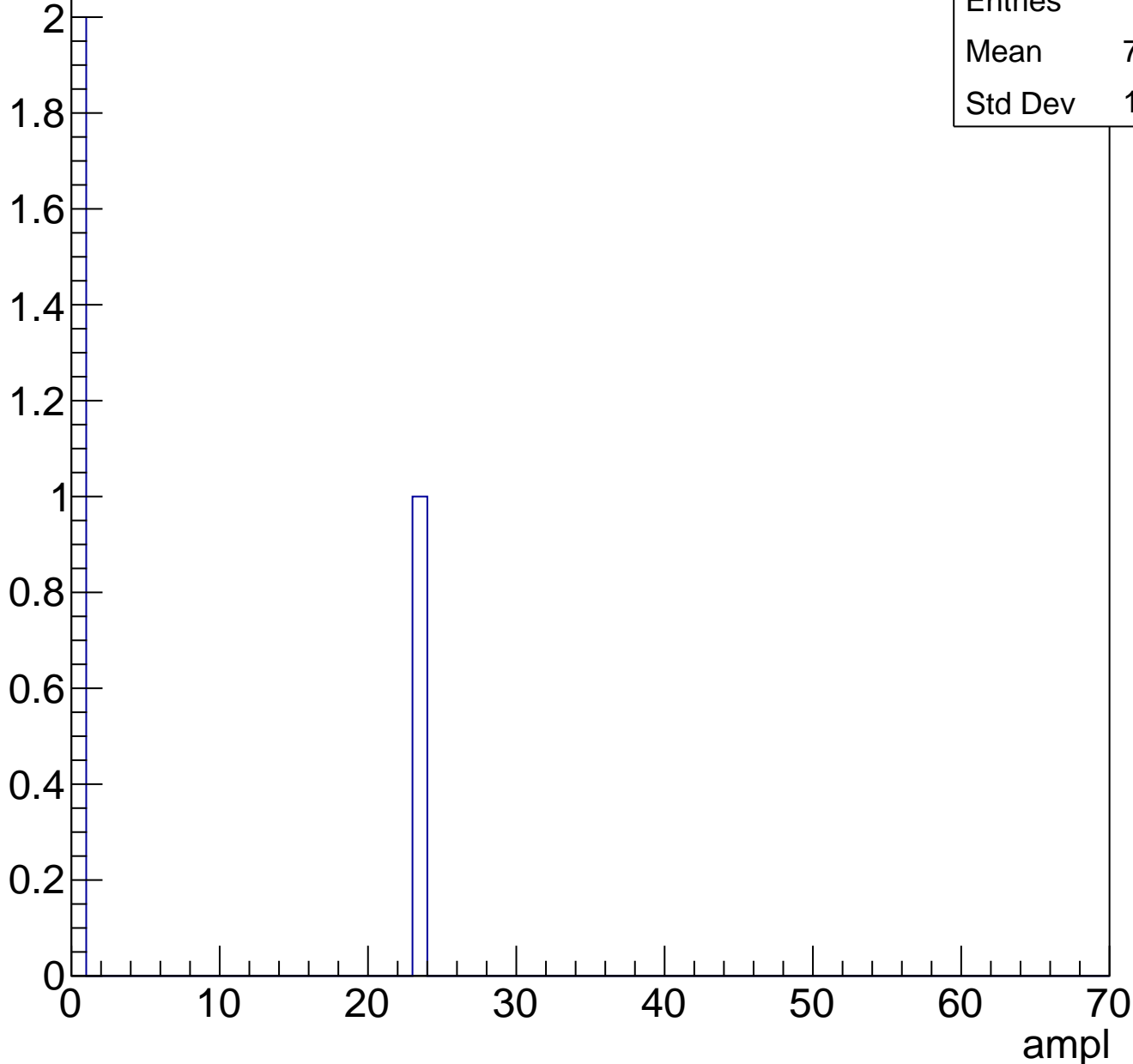




# B1L102S, U12-ch17, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	3
Mean	7.667
Std Dev	10.84

# B1L102S, U12-ch18, adc0

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	75
Mean	28.01
Std Dev	4.002

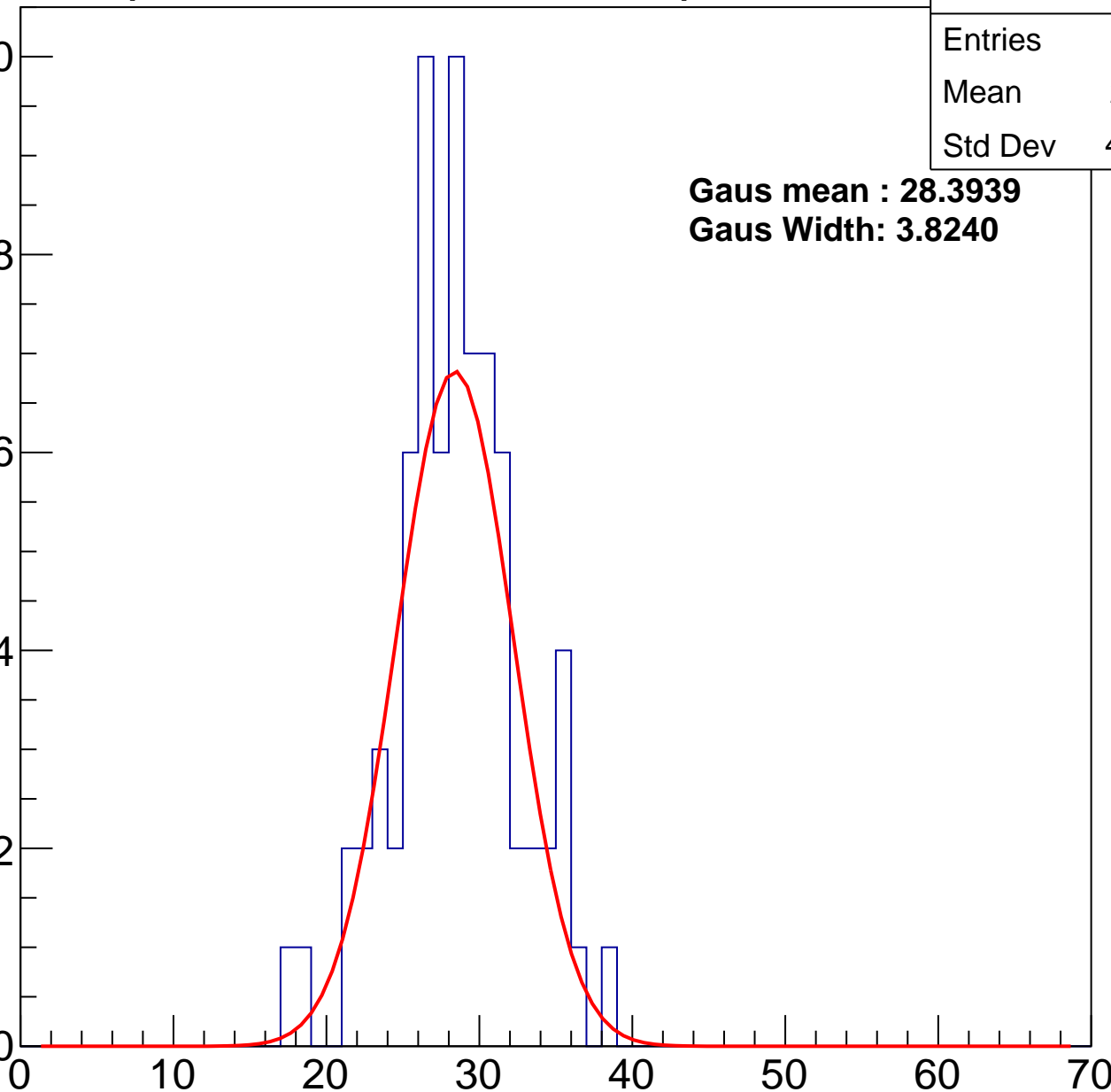
**Gaus mean : 28.3939**

**Gaus Width: 3.8240**

Entry

10  
8  
6  
4  
2  
0

ampl



# B1L102S, U12-ch18, adc1

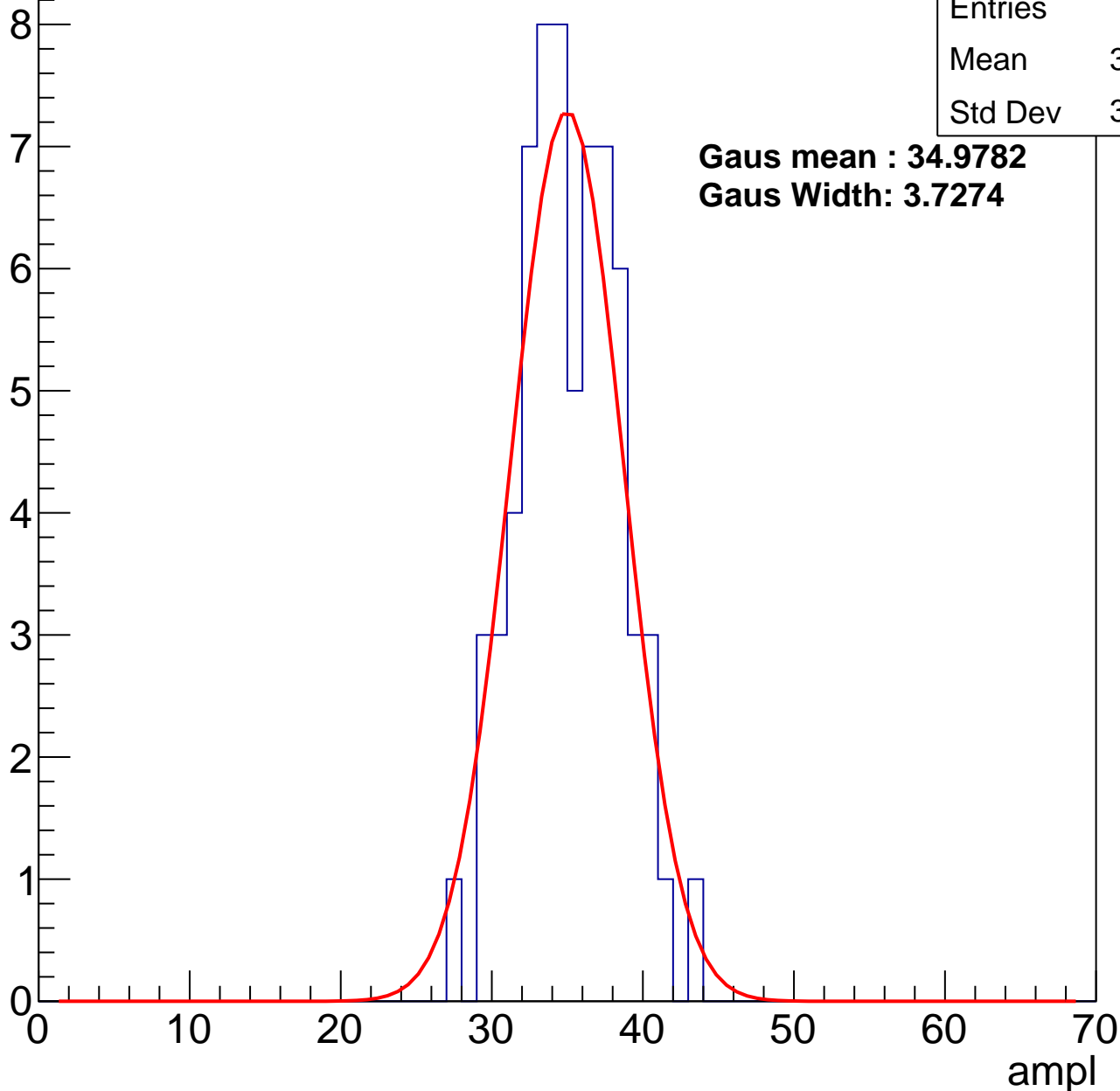
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	67
Mean	34.67
Std Dev	3.275

**Gaus mean : 34.9782**

**Gaus Width: 3.7274**



# B1L102S, U12-ch18, adc2

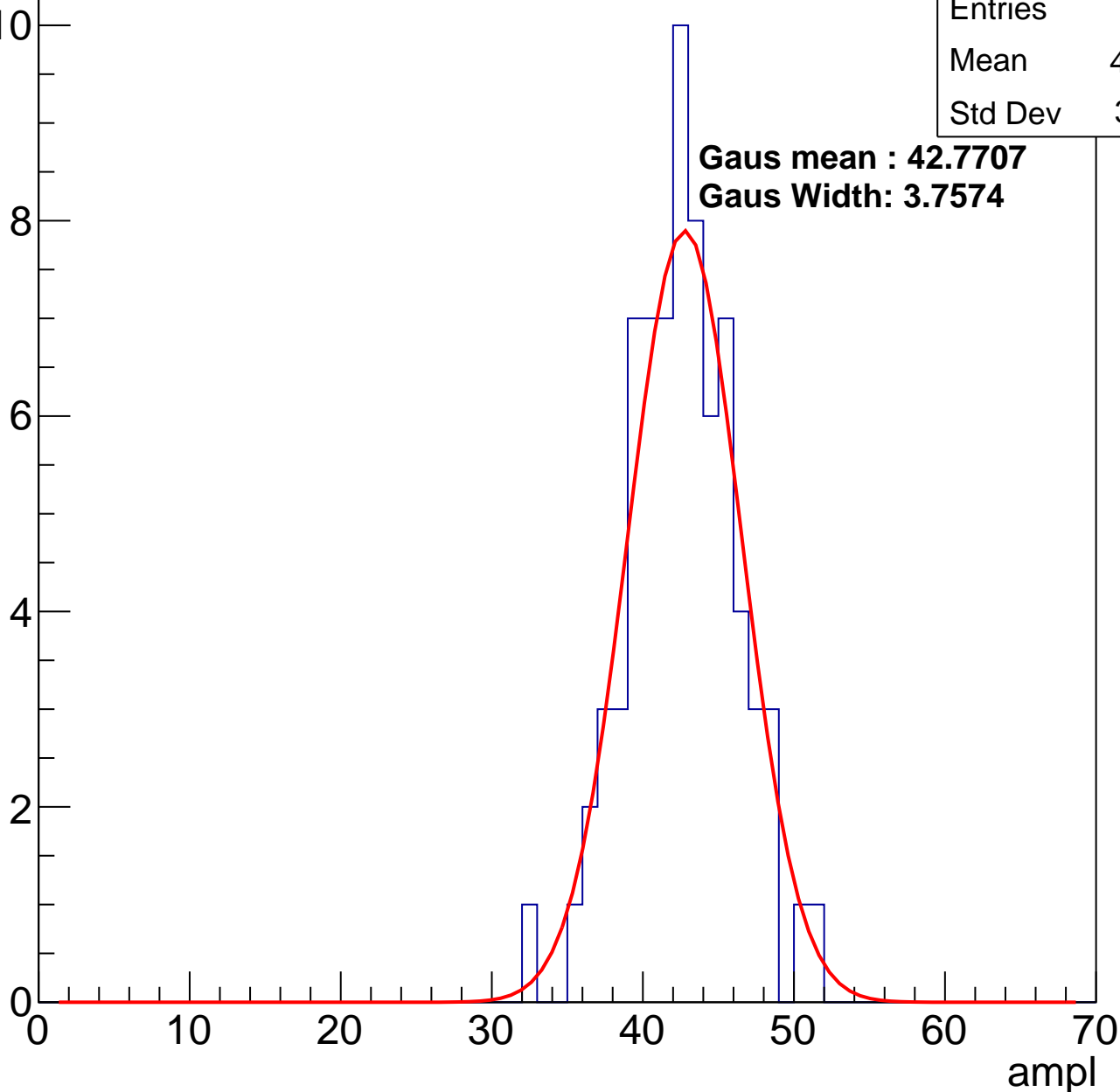
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	74
Mean	42.12
Std Dev	3.541

**Gaus mean : 42.7707**

**Gaus Width: 3.7574**

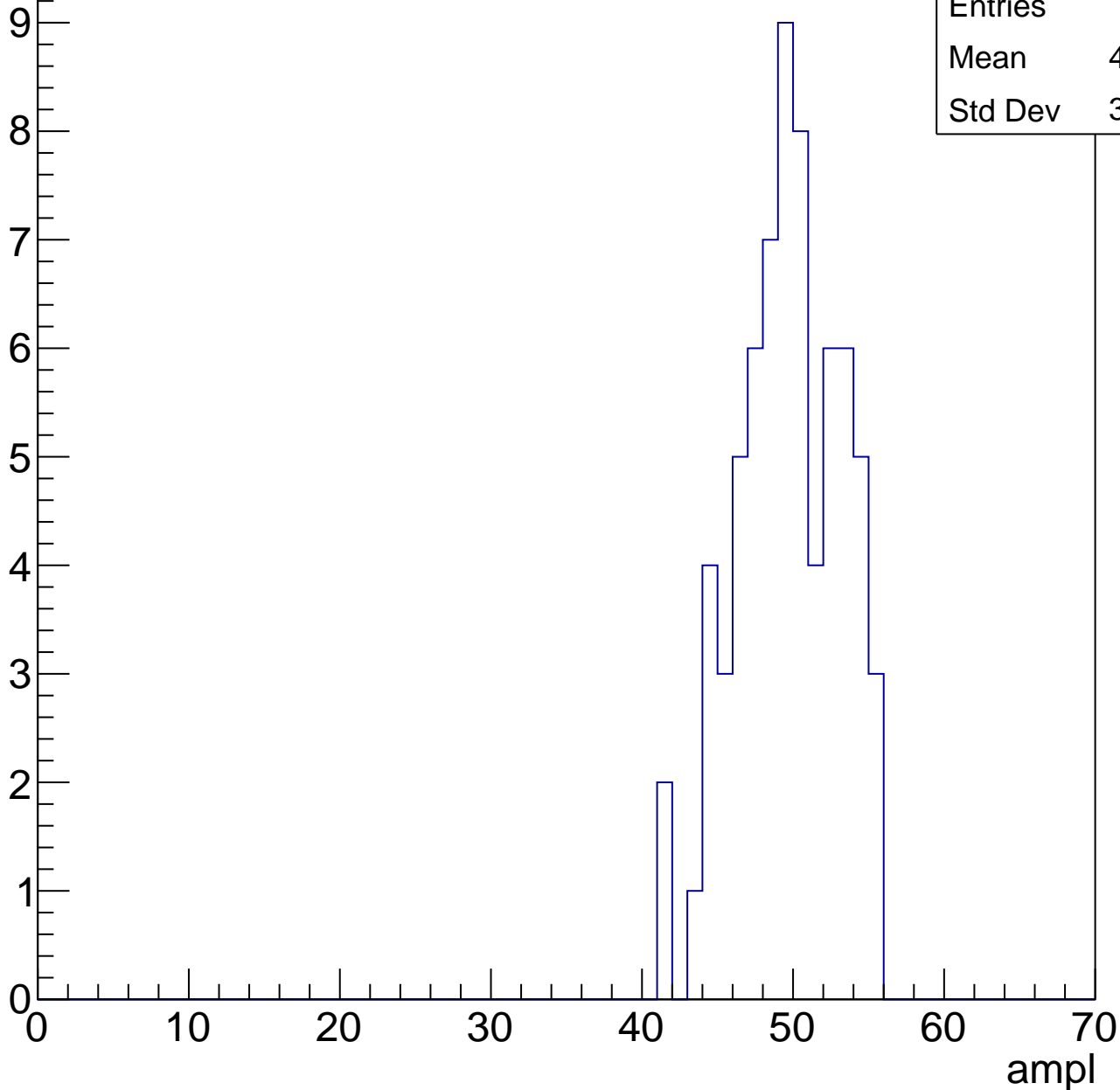


# B1L102S, U12-ch18, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	49.19
Std Dev	3.389

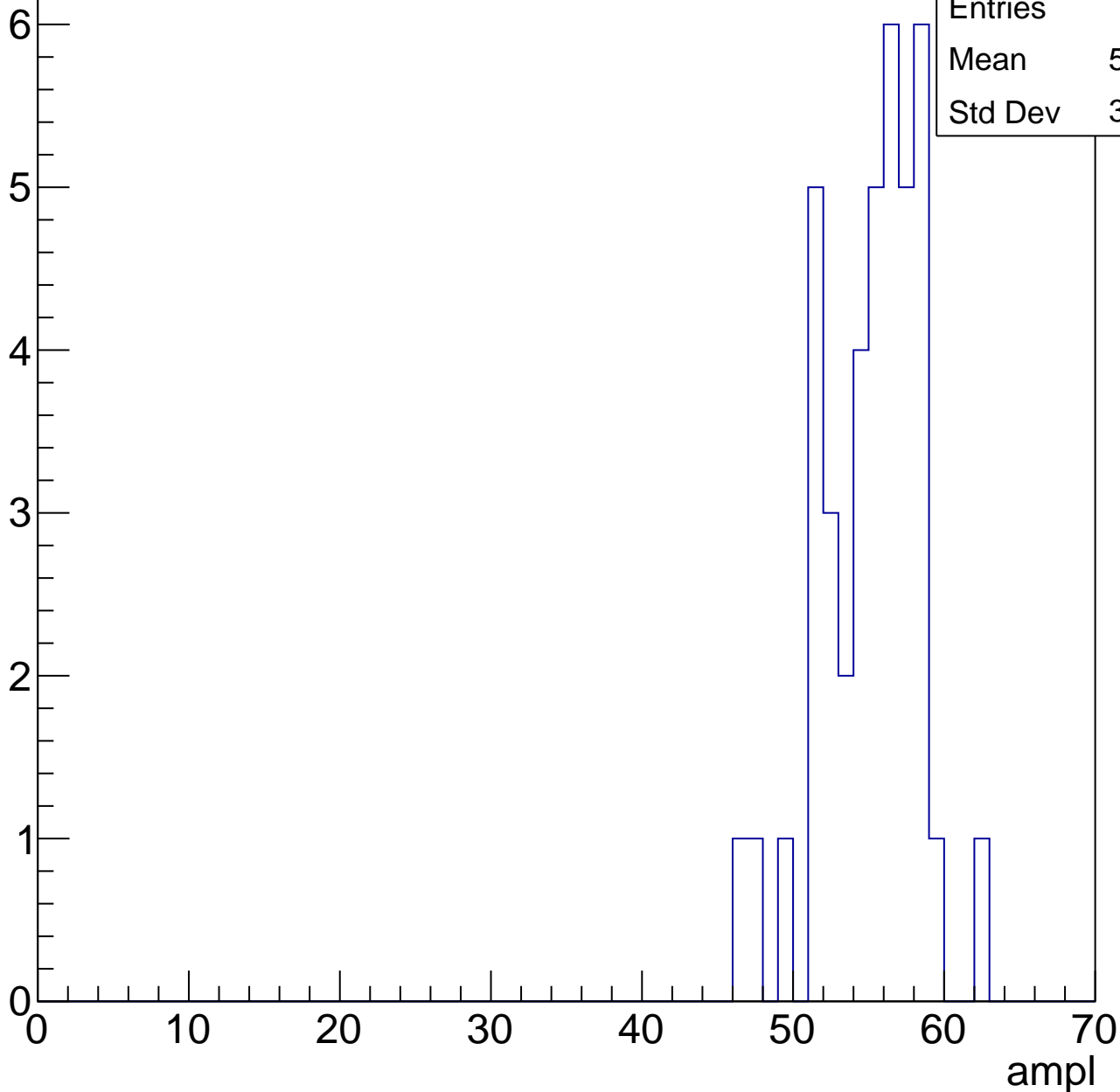


# B1L102S, U12-ch18, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	41
Mean	54.63
Std Dev	3.274

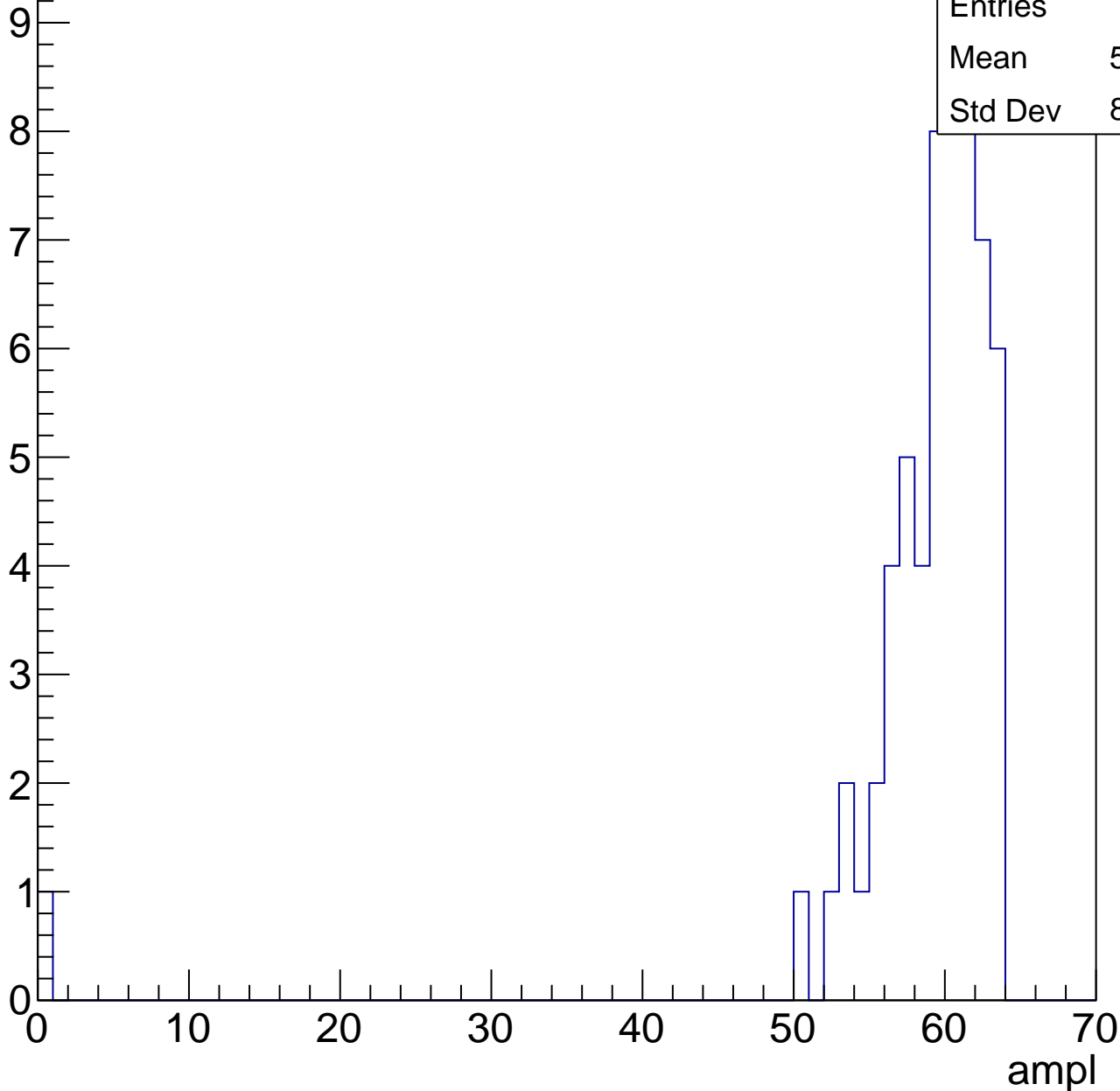


# B1L102S, U12-ch18, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

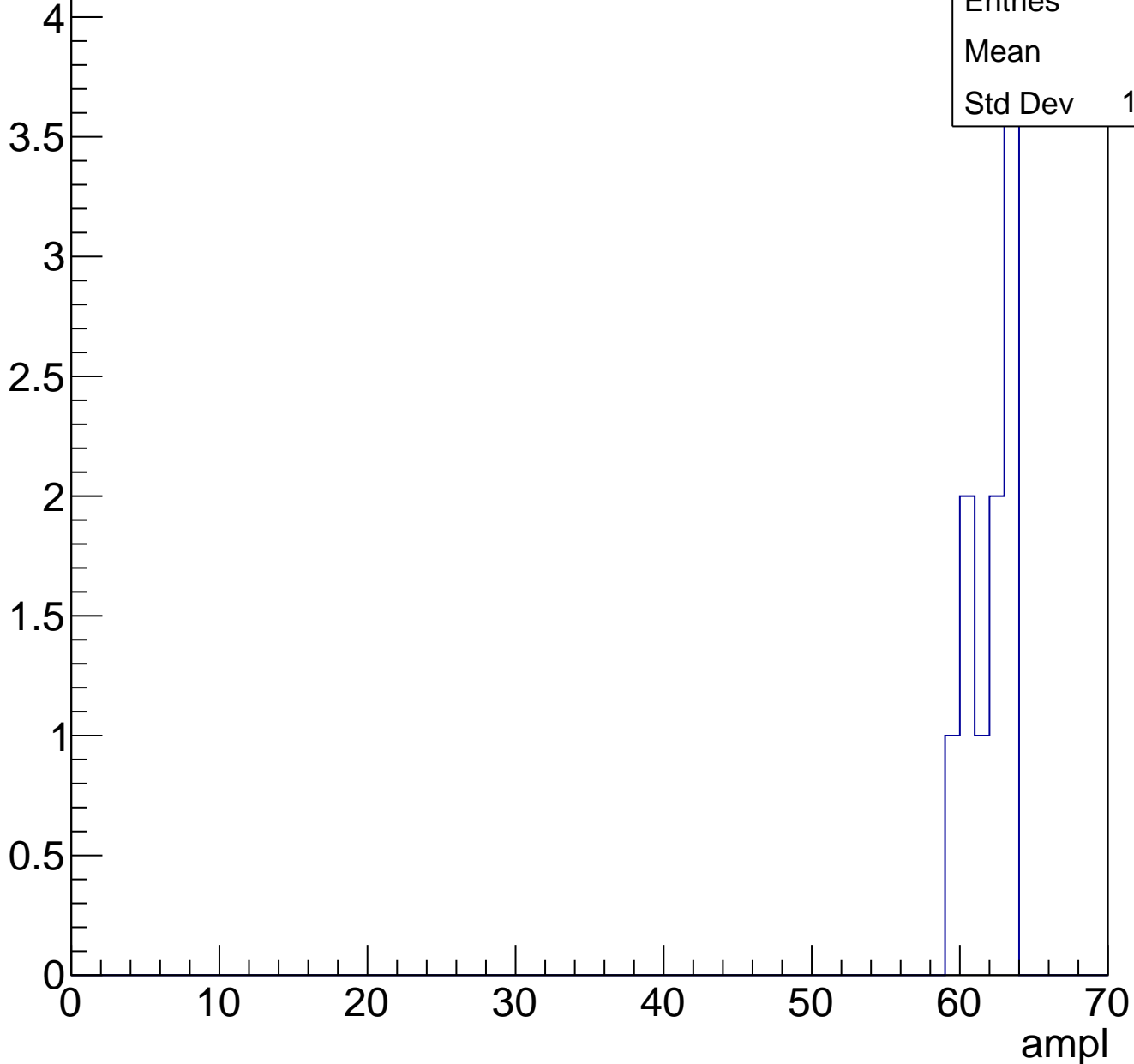
Entries	59
Mean	58.07
Std Dev	8.184



# B1L102S, U12-ch18, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U12-ch18, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U12-ch19, adc0

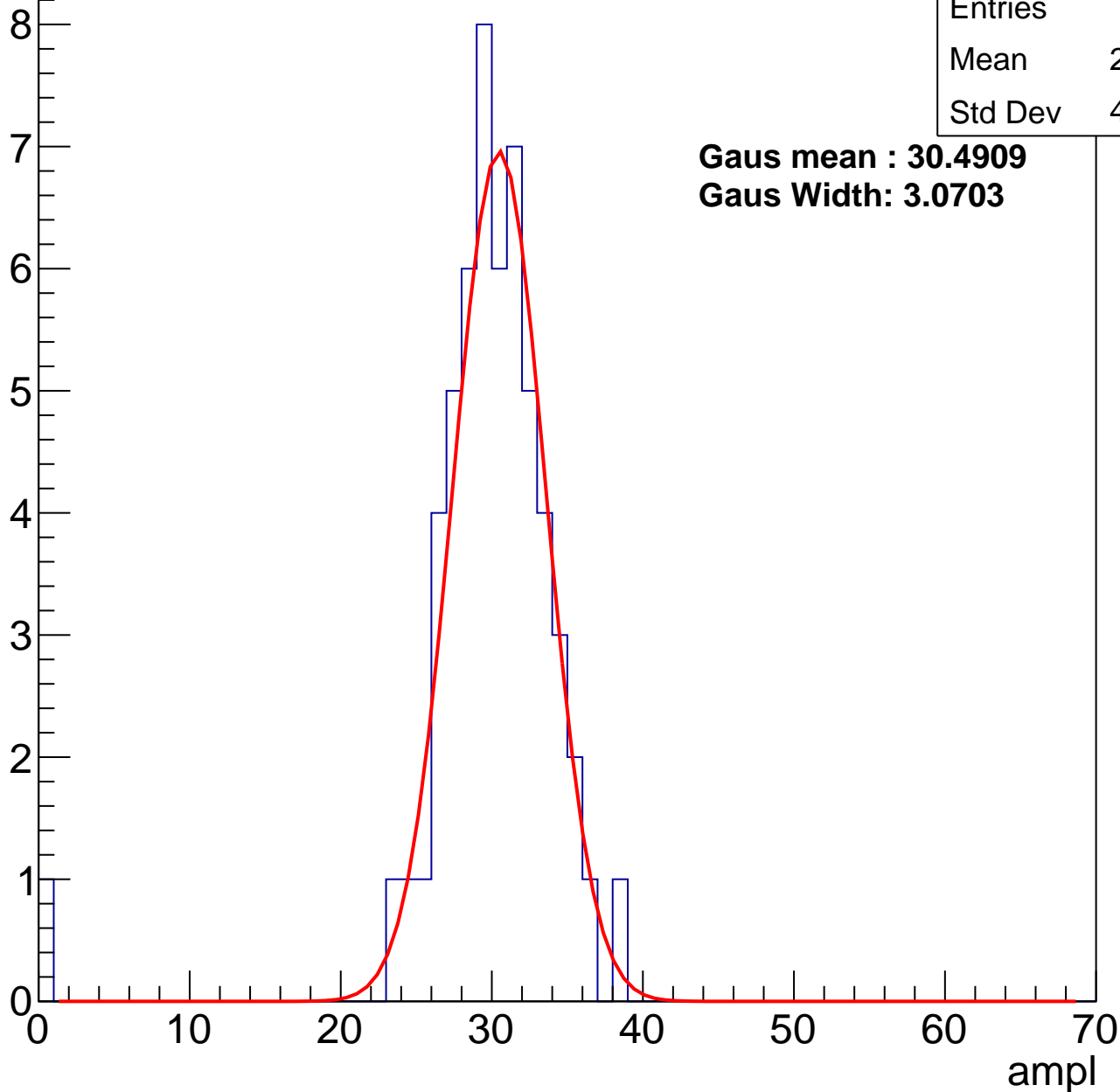
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	56
Mean	29.39
Std Dev	4.985

**Gaus mean : 30.4909**

**Gaus Width: 3.0703**



# B1L102S, U12-ch19, adc1

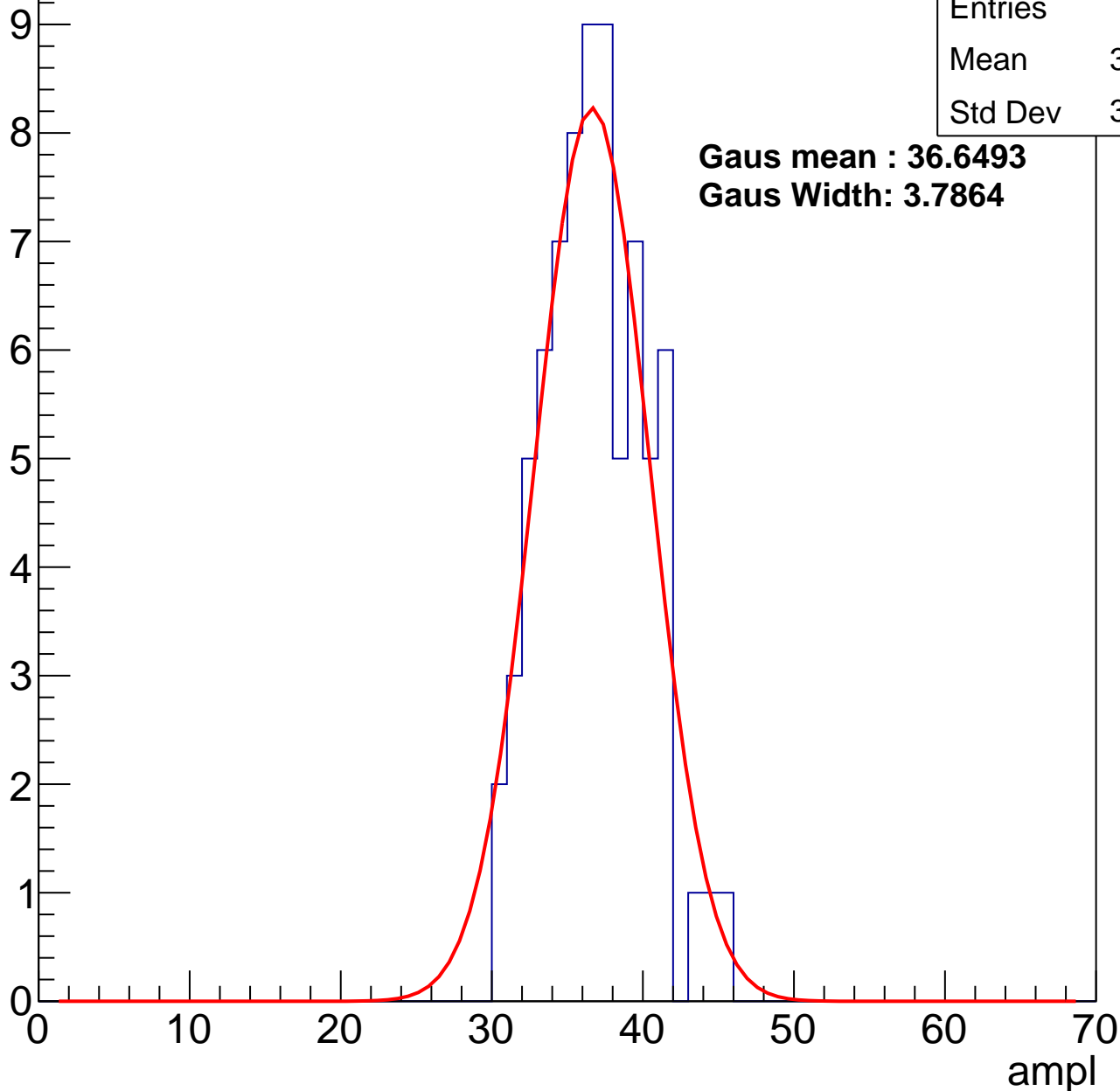
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	75
Mean	36.36
Std Dev	3.313

**Gaus mean : 36.6493**

**Gaus Width: 3.7864**



# B1L102S, U12-ch19, adc2

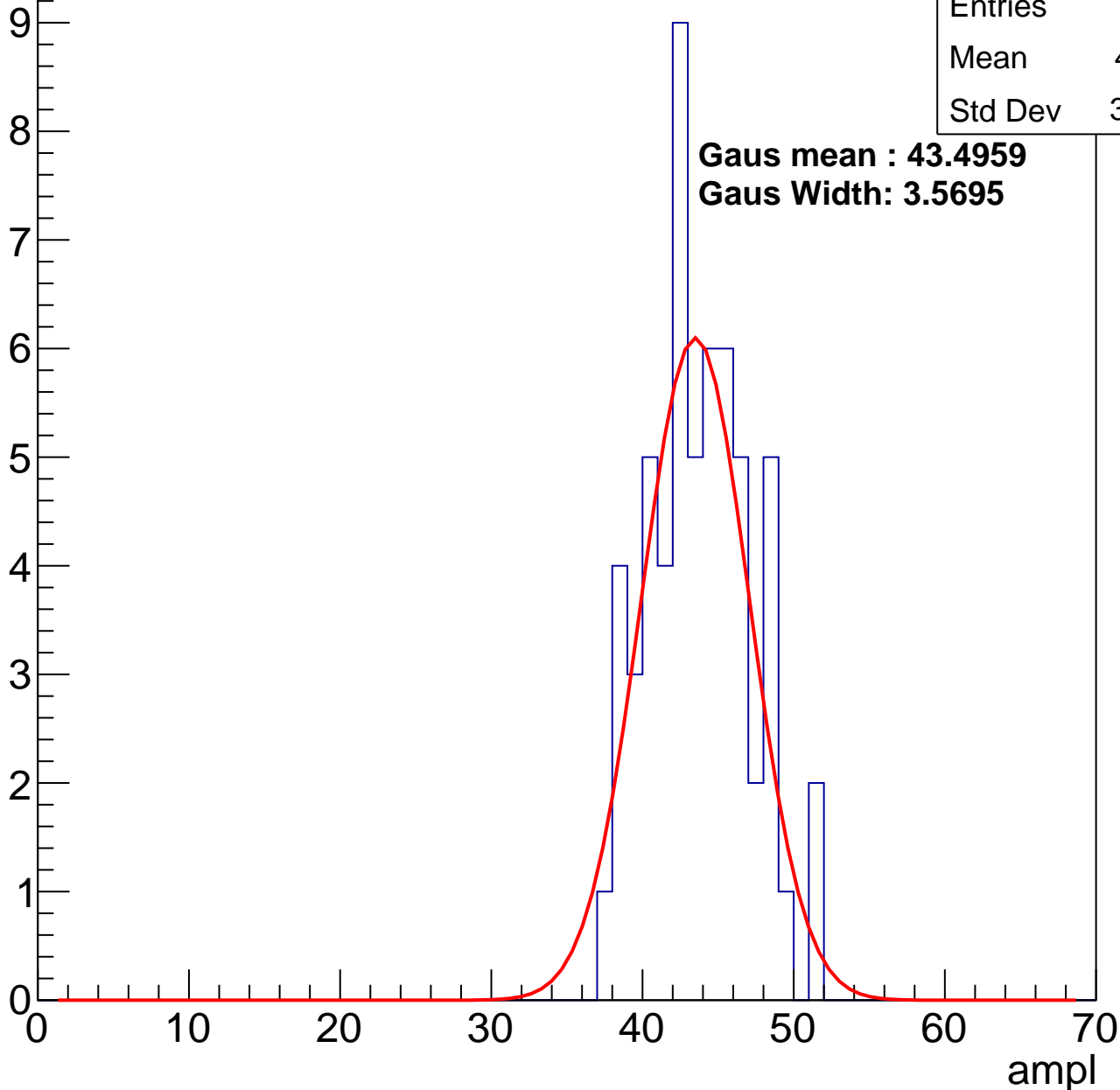
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	58
Mean	43.31
Std Dev	3.333

**Gaus mean : 43.4959**

**Gaus Width: 3.5695**

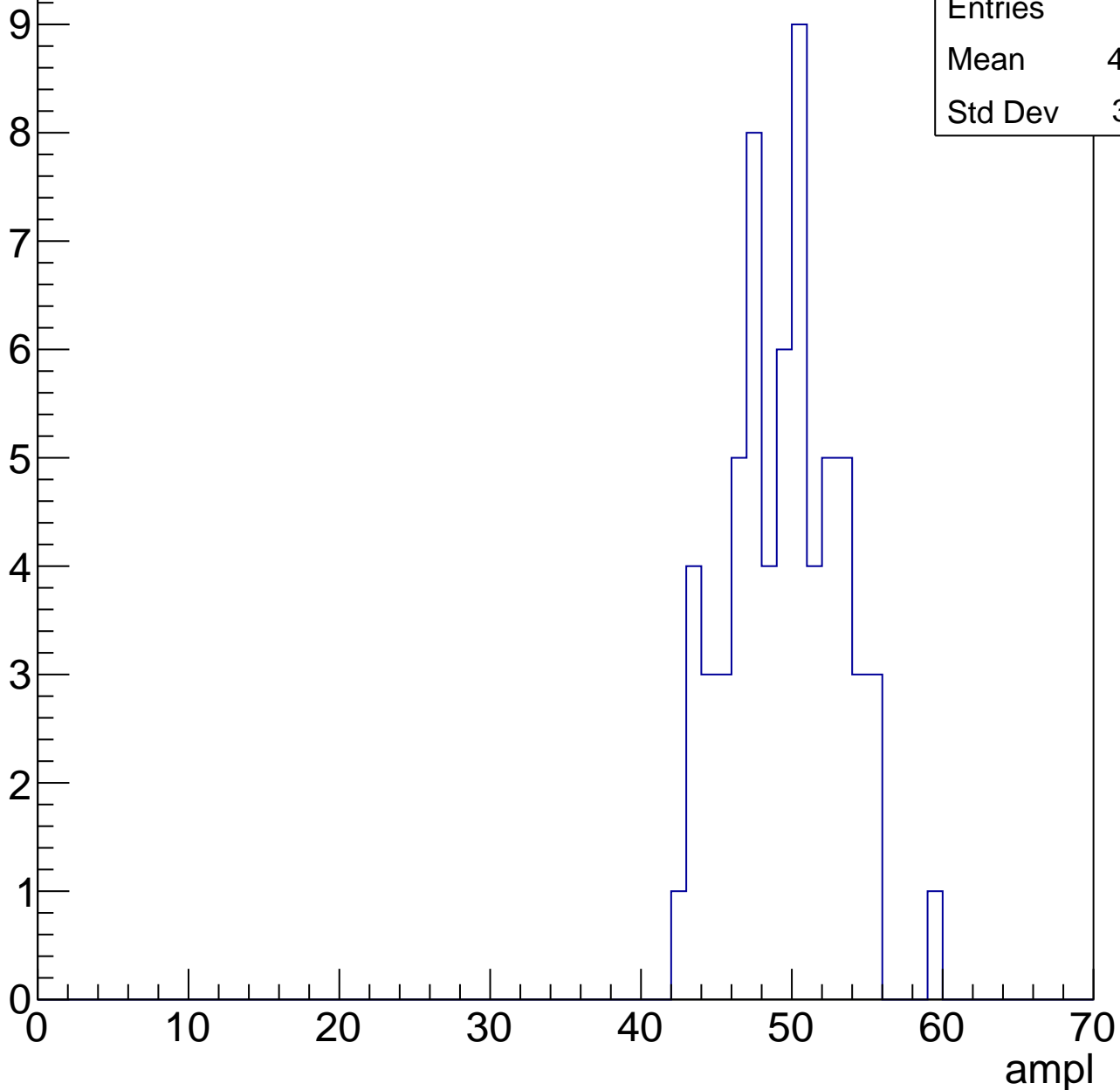


# B1L102S, U12-ch19, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	49.03
Std Dev	3.601

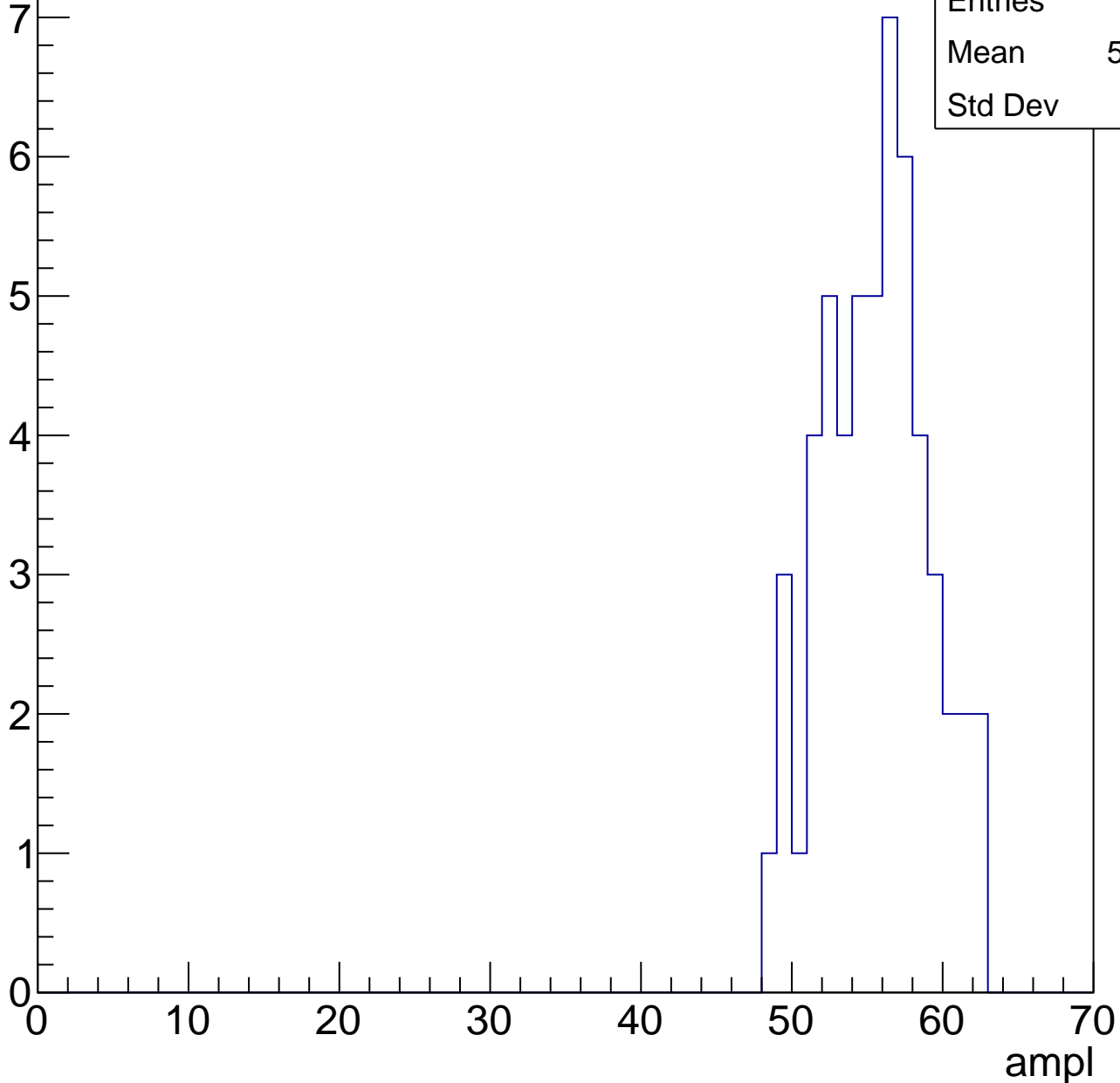


# B1L102S, U12-ch19, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	54
Mean	55.09
Std Dev	3.46



# B1L102S, U12-ch19, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	54
Mean	58.31
Std Dev	8.413

ampl

0

10

20

30

40

50

60

70

# B1L102S, U12-ch19, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U12-ch19, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

1  
0.8  
0.6  
0.4  
0.2  
0

Entries	1
Mean	20
Std Dev	0

ampl

# B1L102S, U12-ch20, adc0

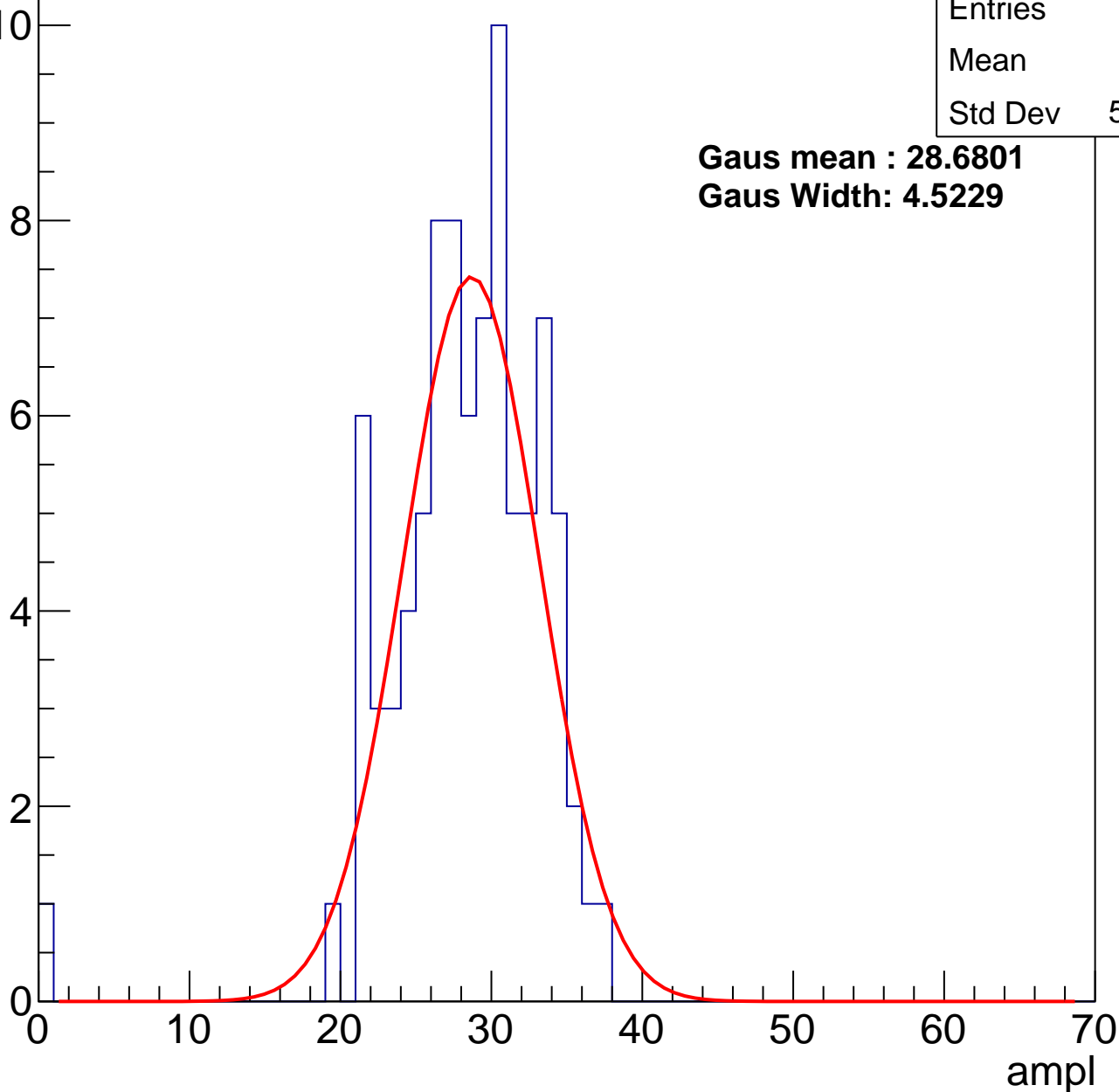
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	88
Mean	27.9
Std Dev	5.068

**Gaus mean : 28.6801**

**Gaus Width: 4.5229**



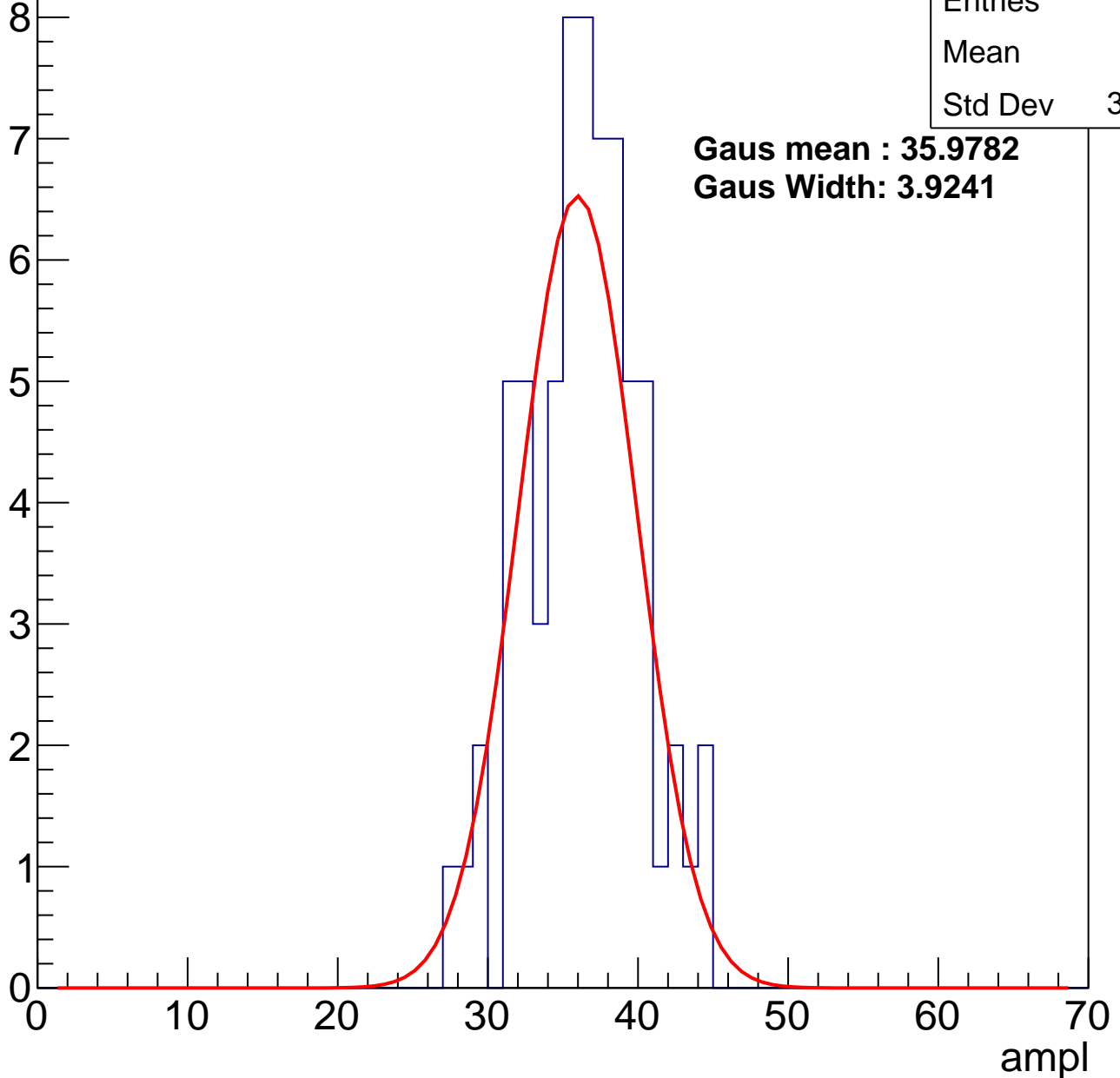
# B1L102S, U12-ch20, adc1

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	35.9
Std Dev	3.711

**Gaus mean : 35.9782**  
**Gaus Width: 3.9241**



# B1L102S, U12-ch20, adc2

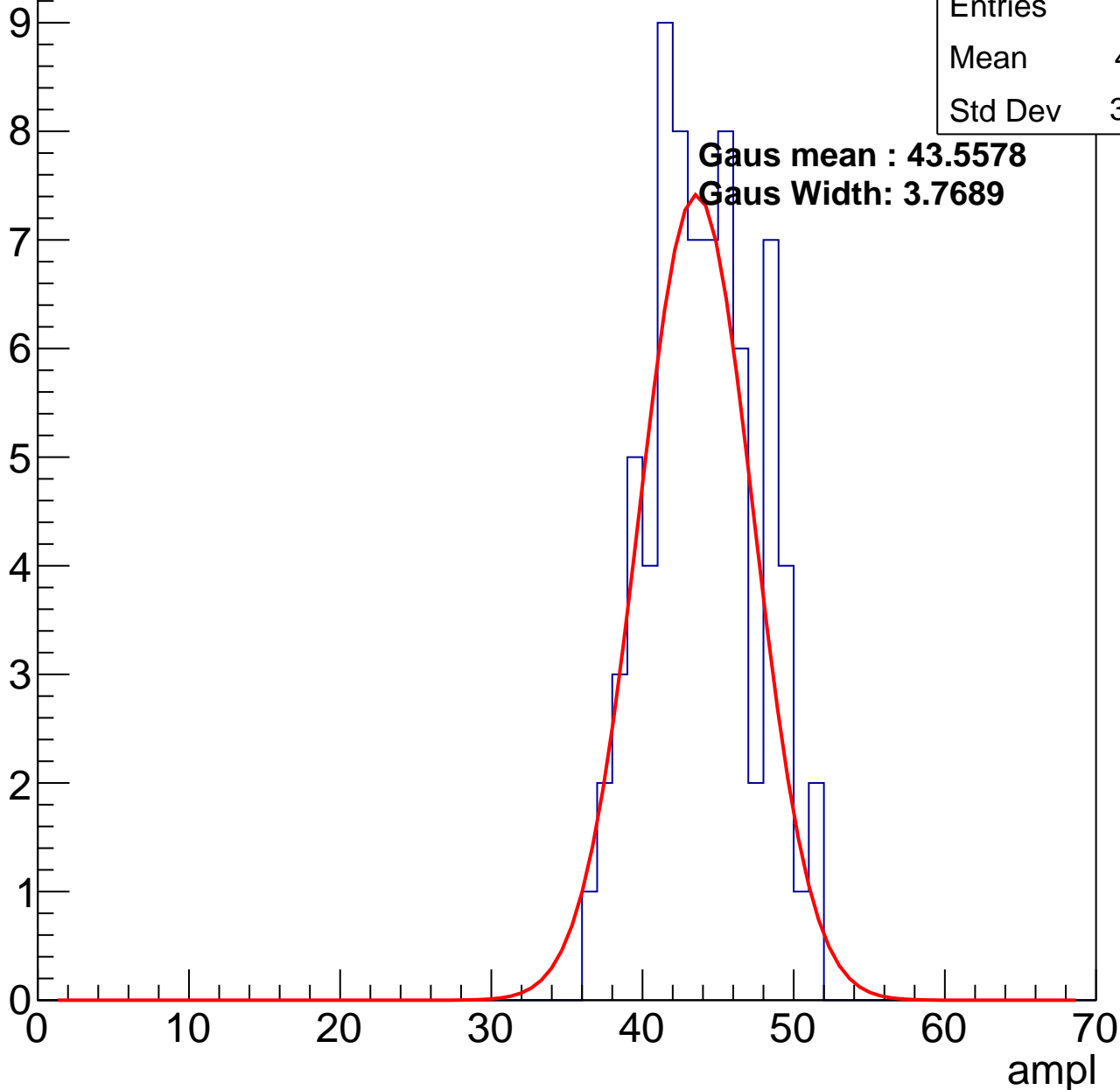
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	76
Mean	43.51
Std Dev	3.549

**Gaus mean : 43.5578**

**Gaus Width: 3.7689**

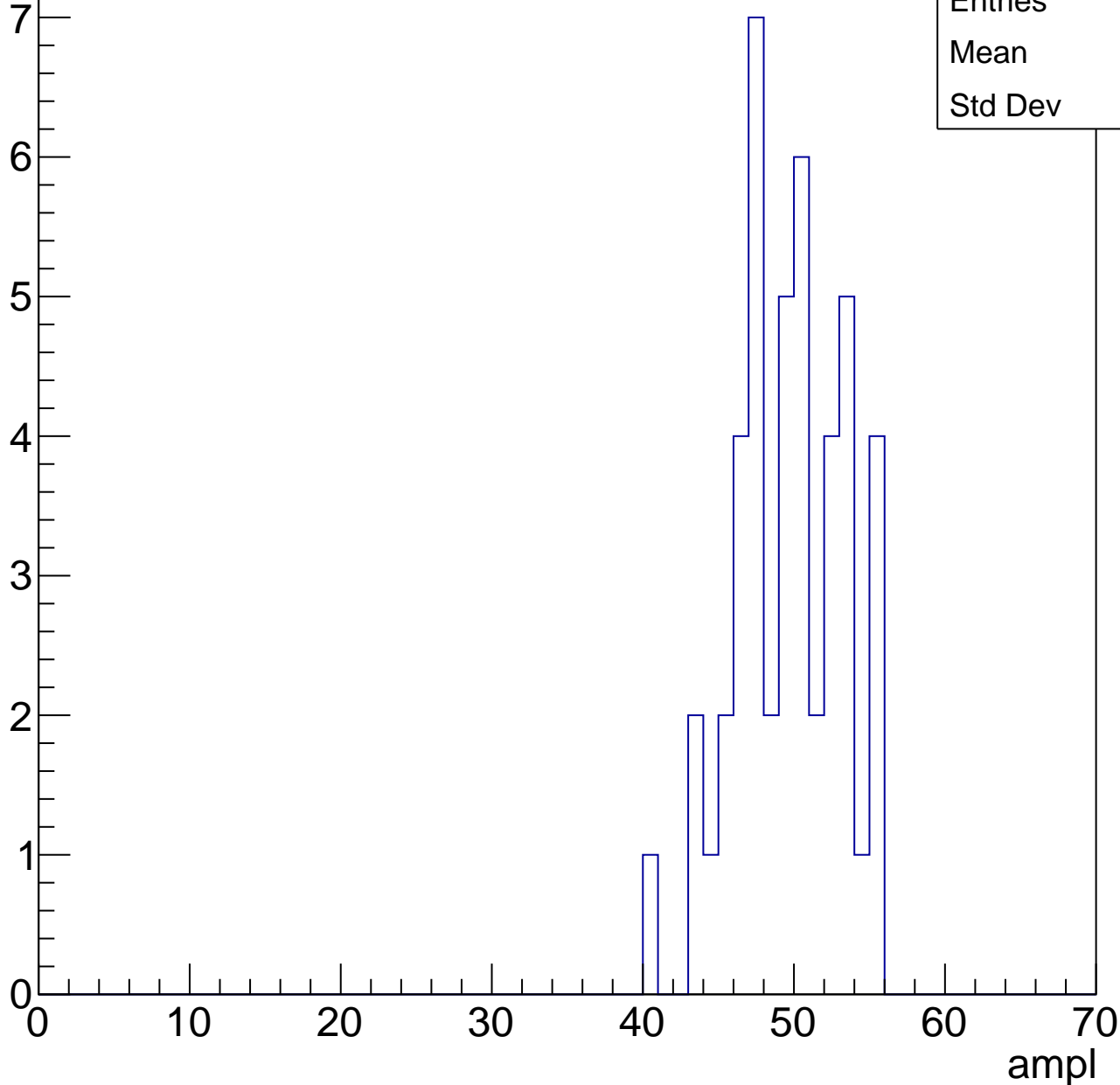


# B1L102S, U12-ch20, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

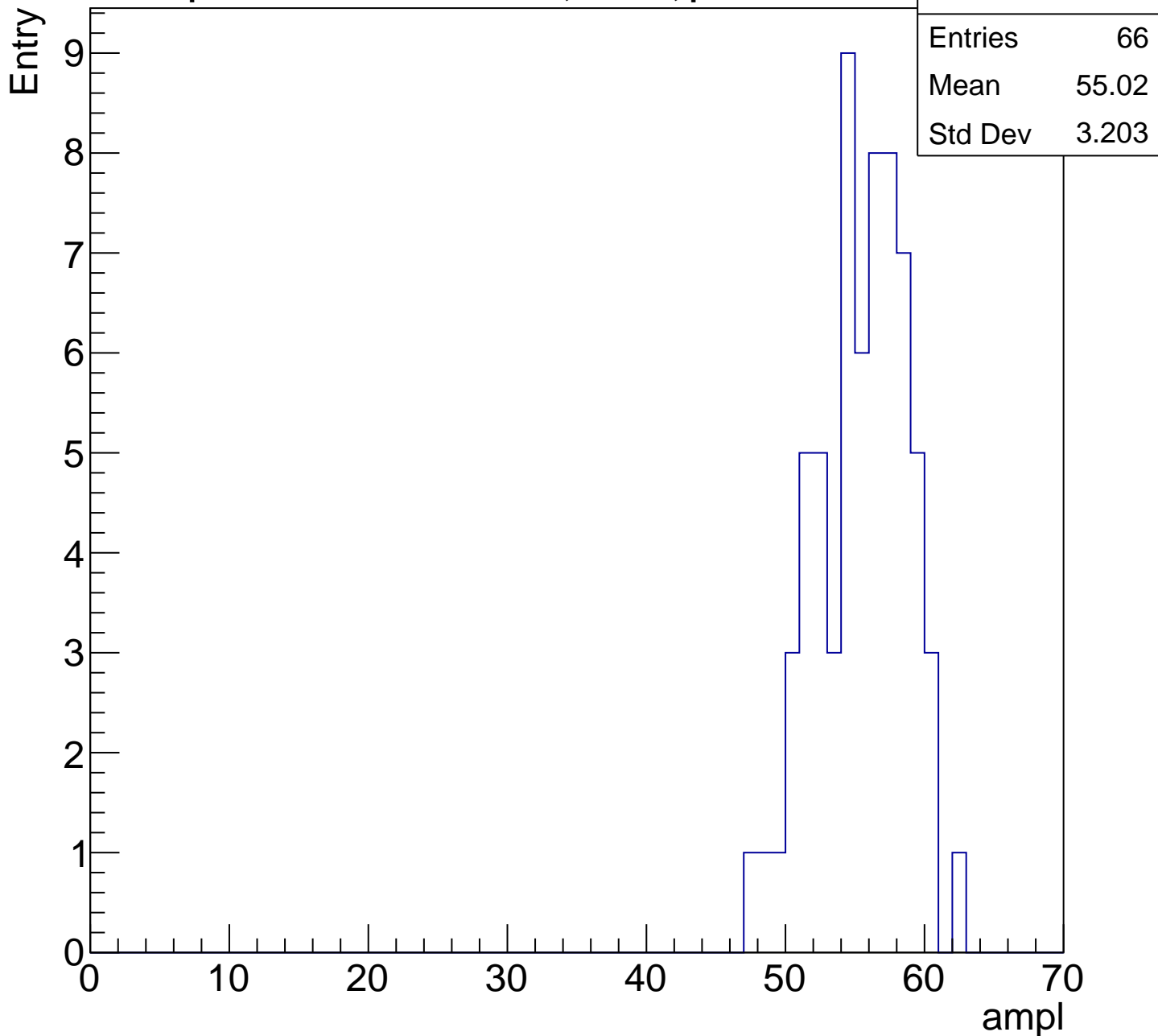
Entry

Entries	46
Mean	49.2
Std Dev	3.53



# B1L102S, U12-ch20, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

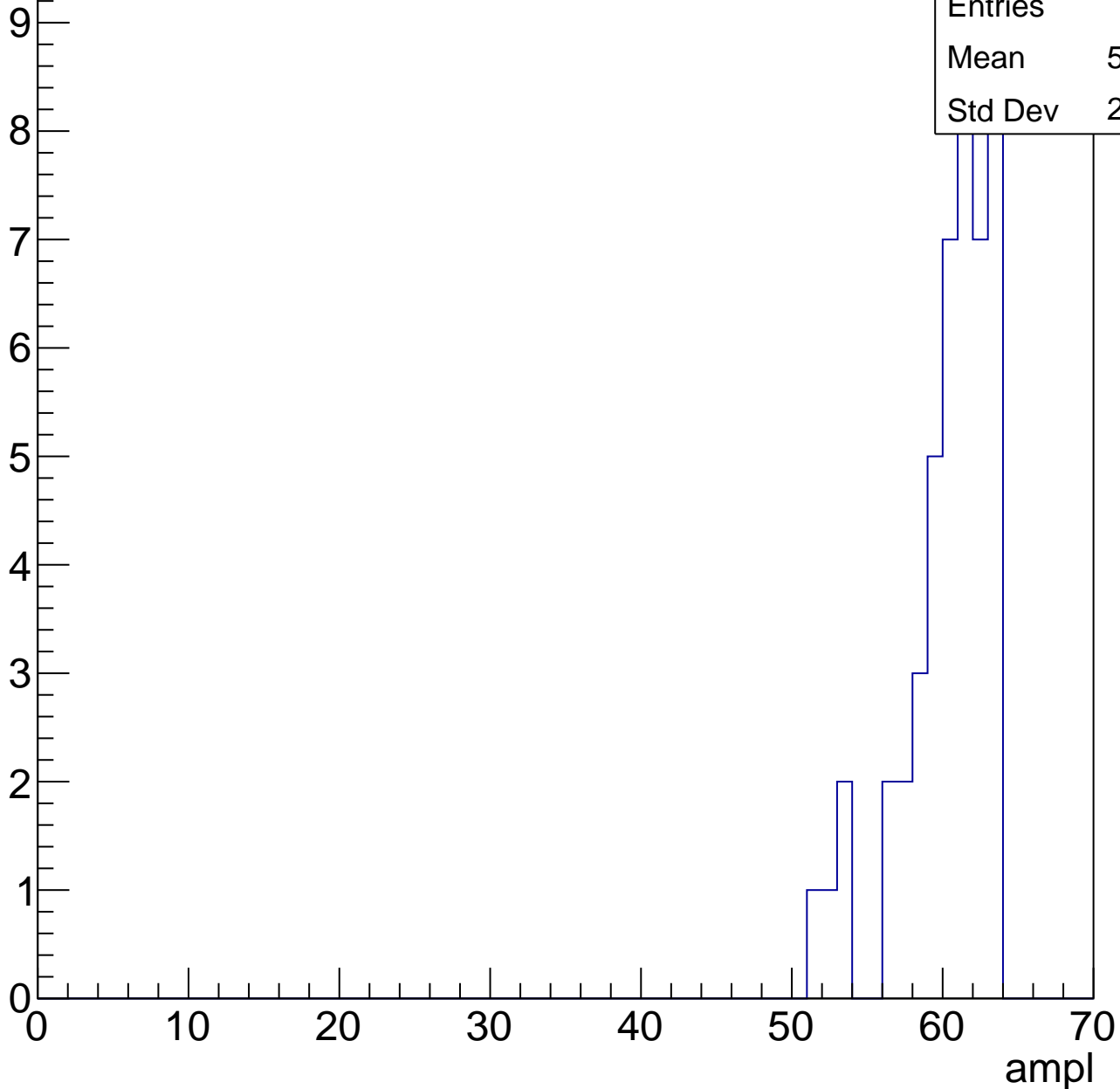


# B1L102S, U12-ch20, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

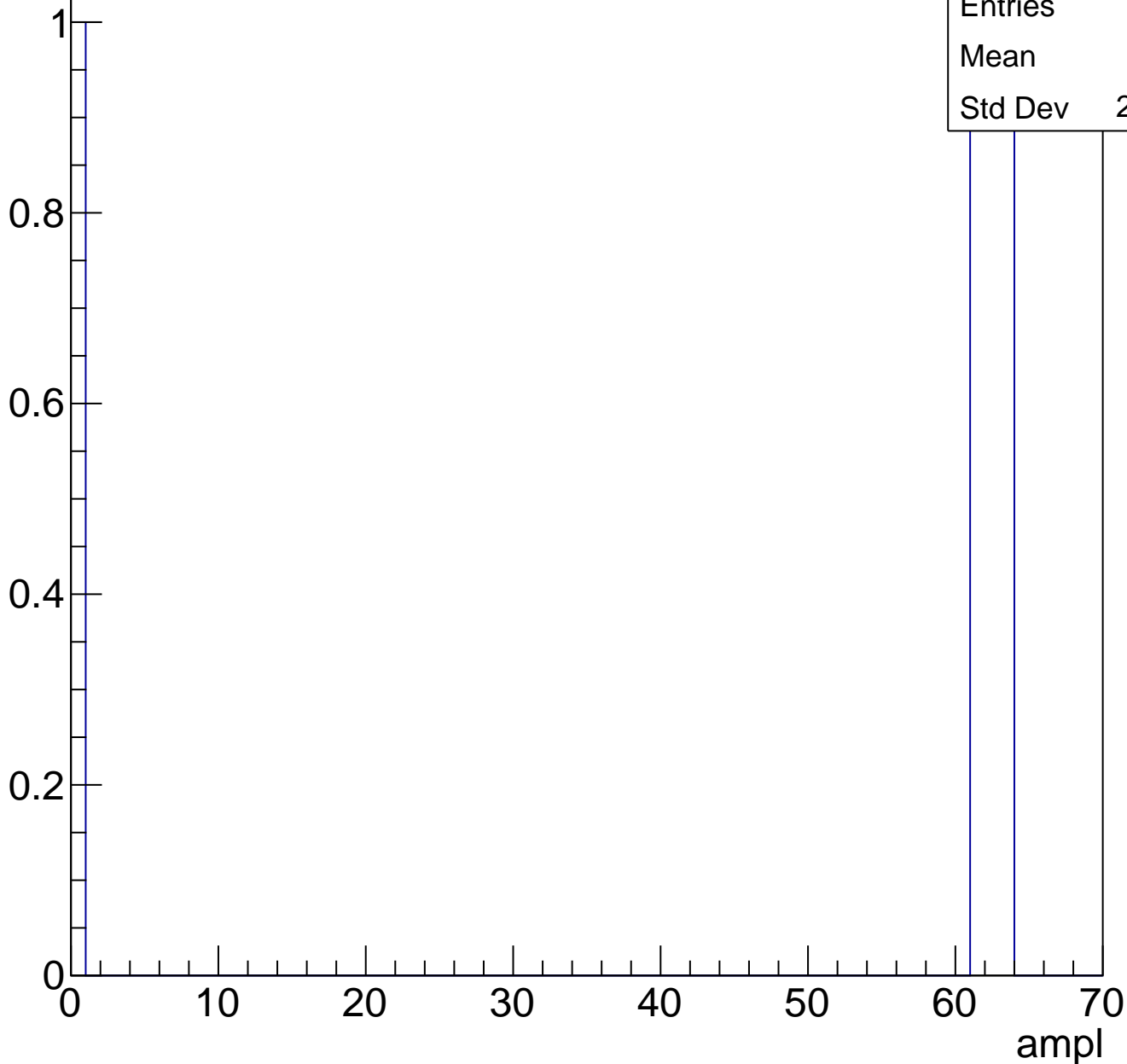
Entries	48
Mean	59.88
Std Dev	2.983



# B1L102S, U12-ch20, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

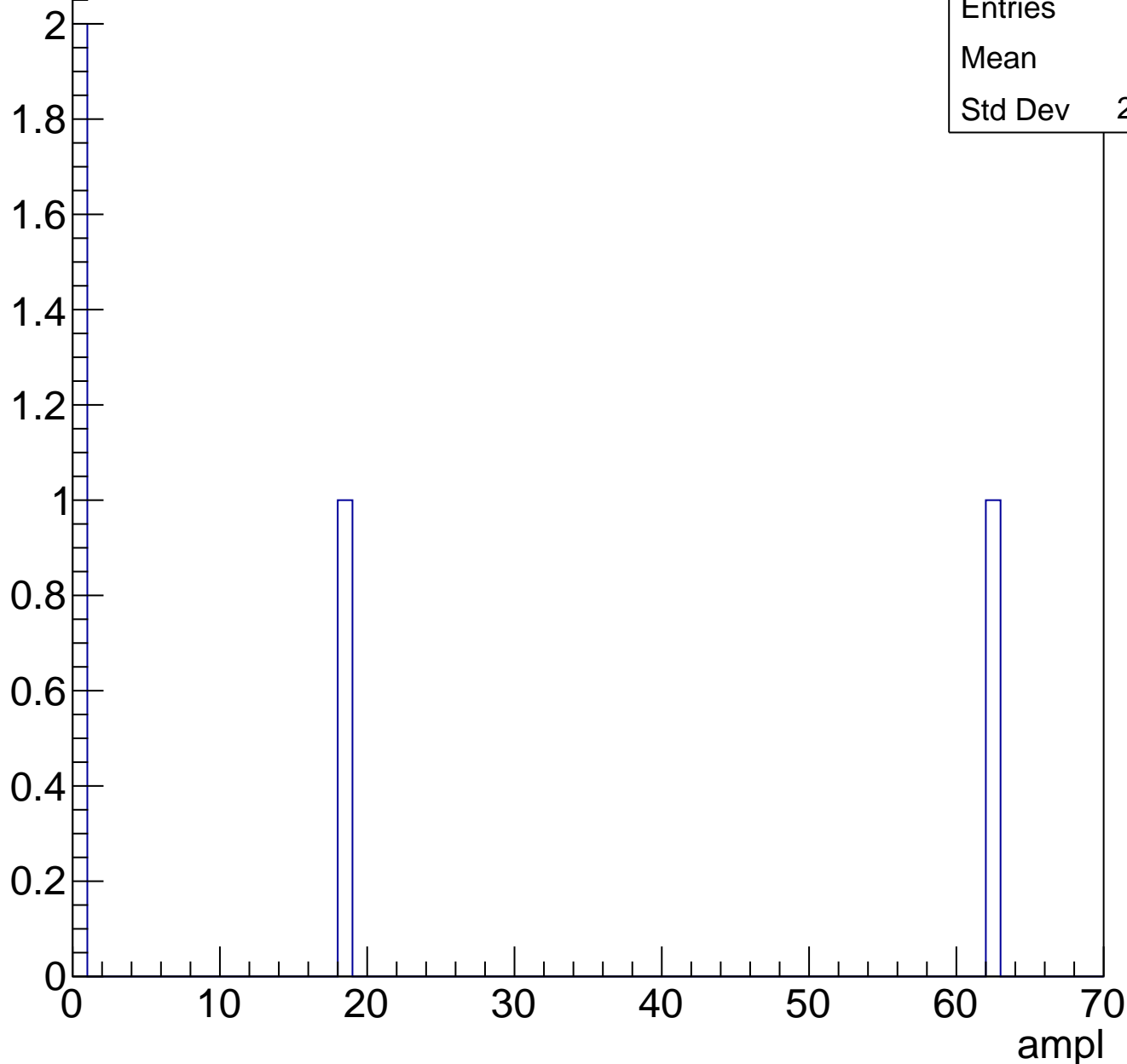




# B1L102S, U12-ch20, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	4
Mean	20
Std Dev	25.34

# B1L102S, U12-ch21, adc0

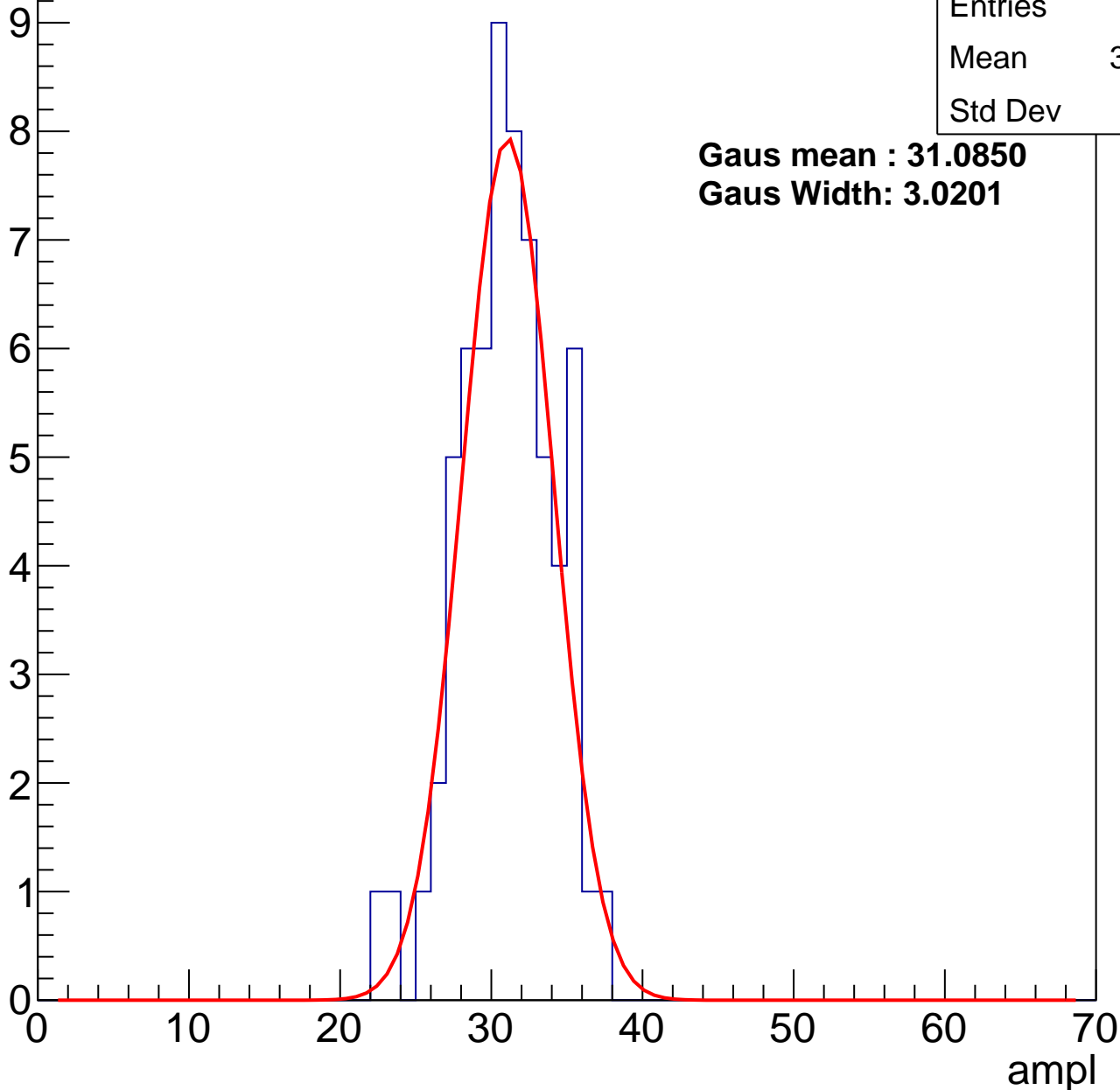
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	63
Mean	30.56
Std Dev	3.1

**Gaus mean : 31.0850**

**Gaus Width: 3.0201**



# B1L102S, U12-ch21, adc1

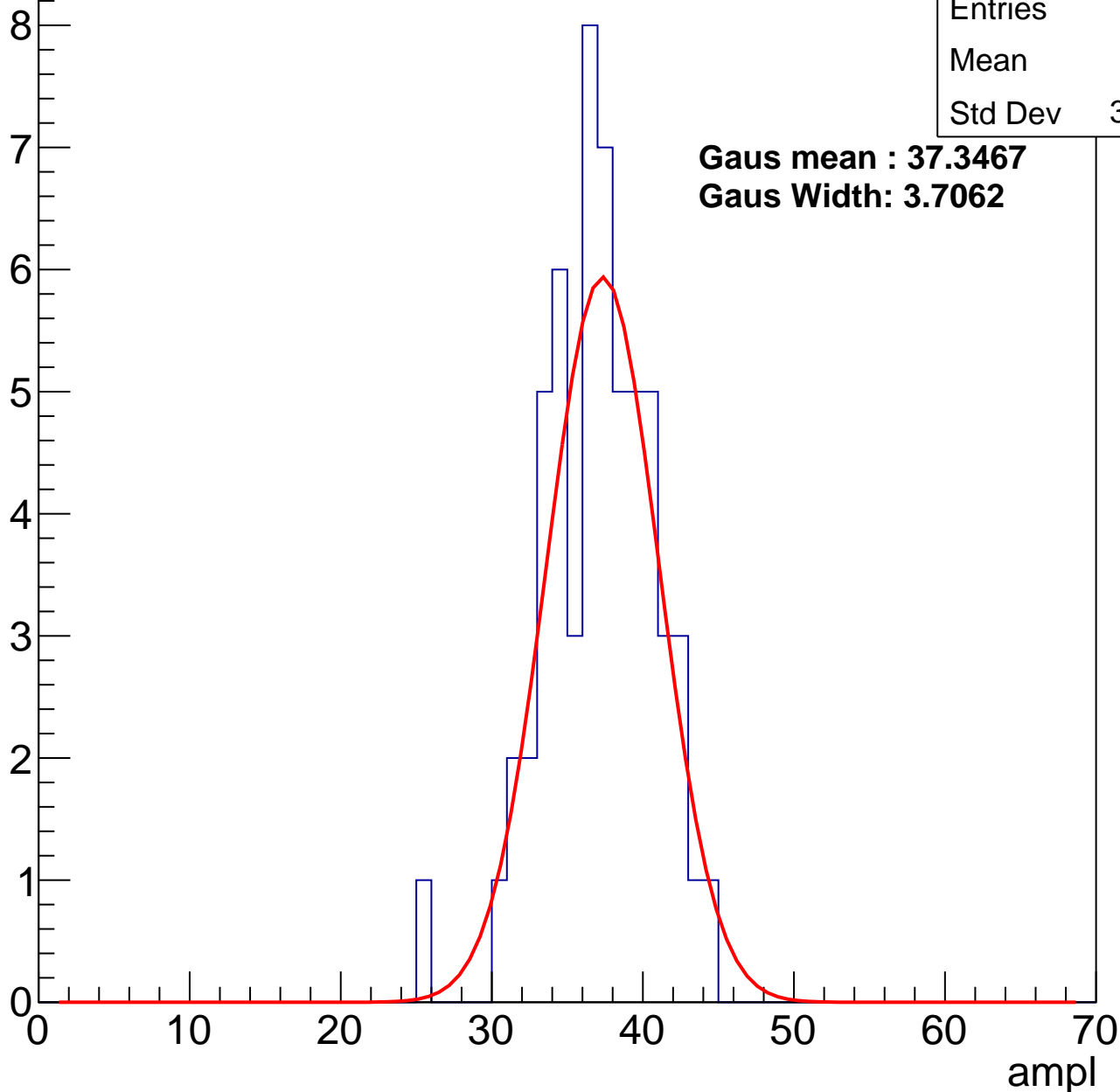
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	58
Mean	36.6
Std Dev	3.567

**Gaus mean : 37.3467**

**Gaus Width: 3.7062**



# B1L102S, U12-ch21, adc2

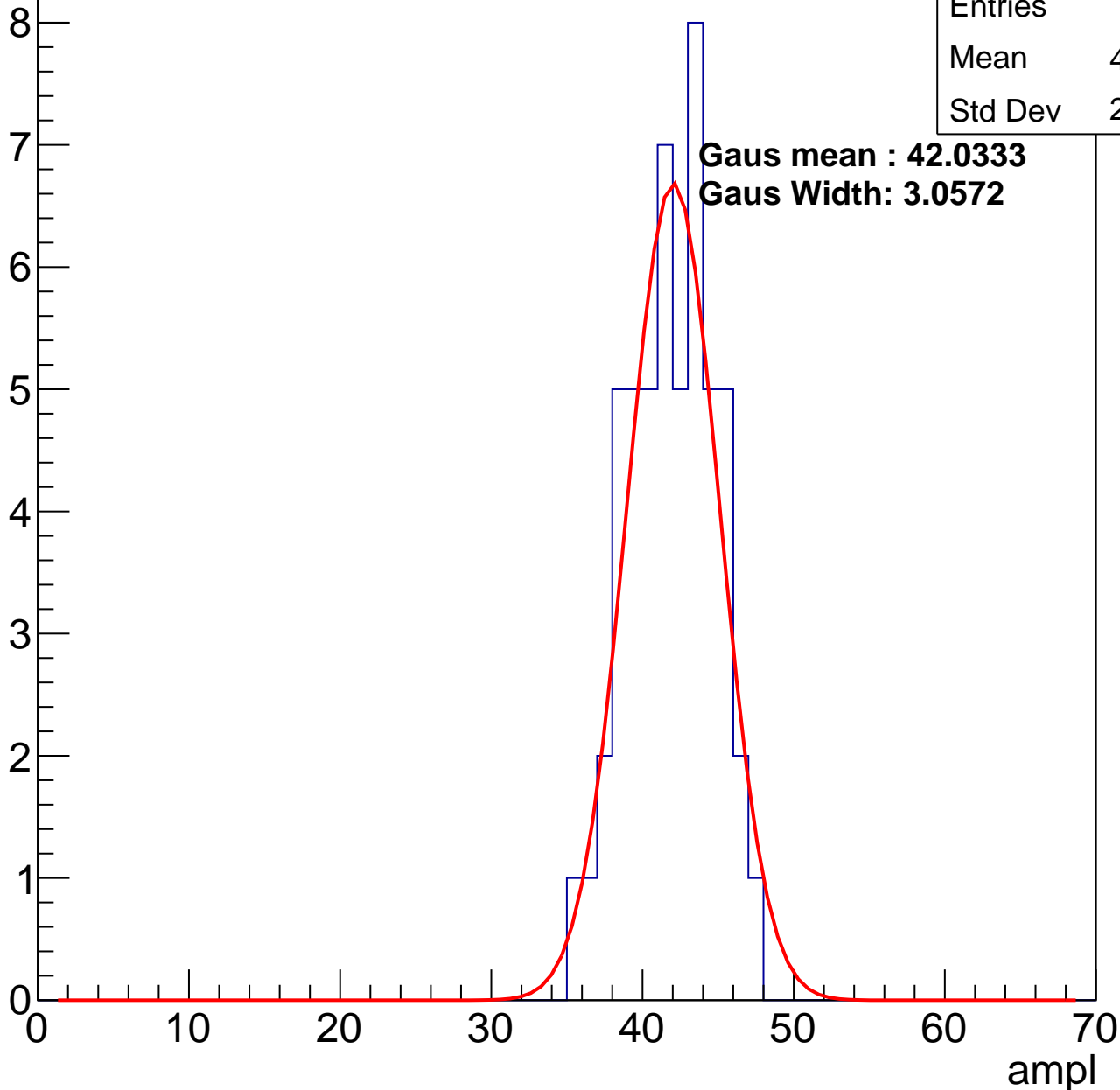
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	52
Mean	41.44
Std Dev	2.776

**Gaus mean : 42.0333**

**Gaus Width: 3.0572**

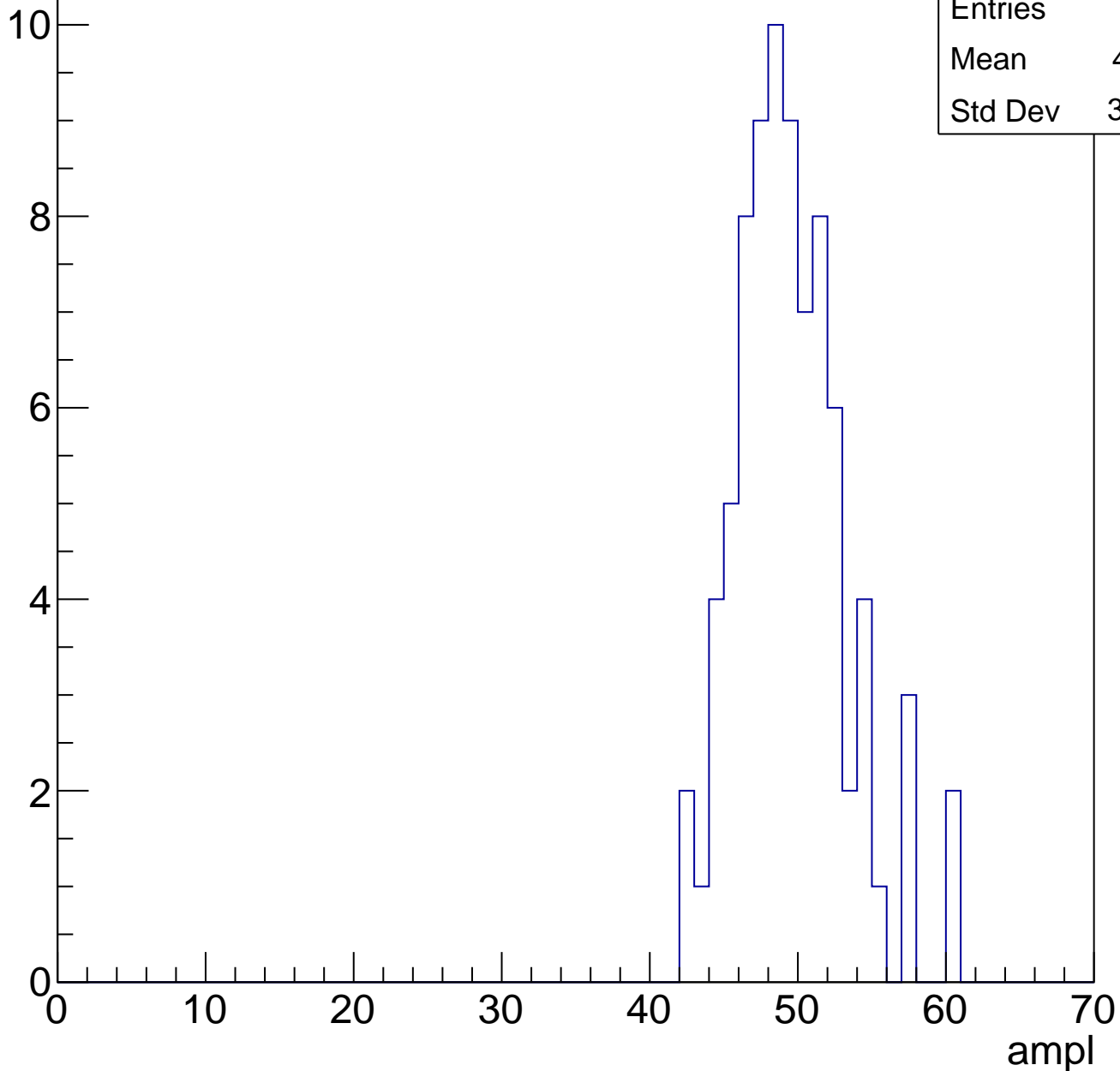


# B1L102S, U12-ch21, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	81
Mean	49.11
Std Dev	3.728

Entry

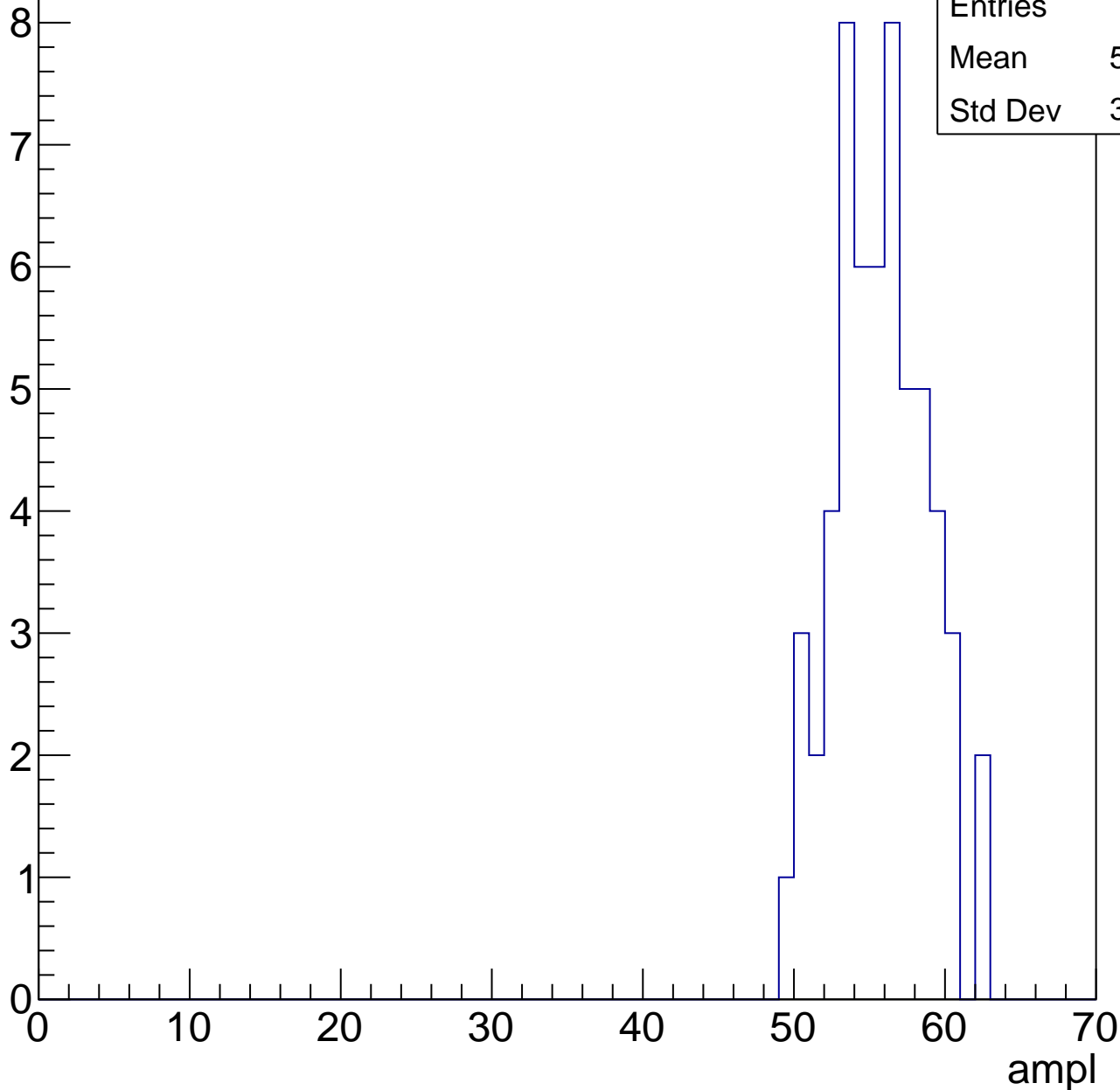


# B1L102S, U12-ch21, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	57
Mean	55.26
Std Dev	3.029

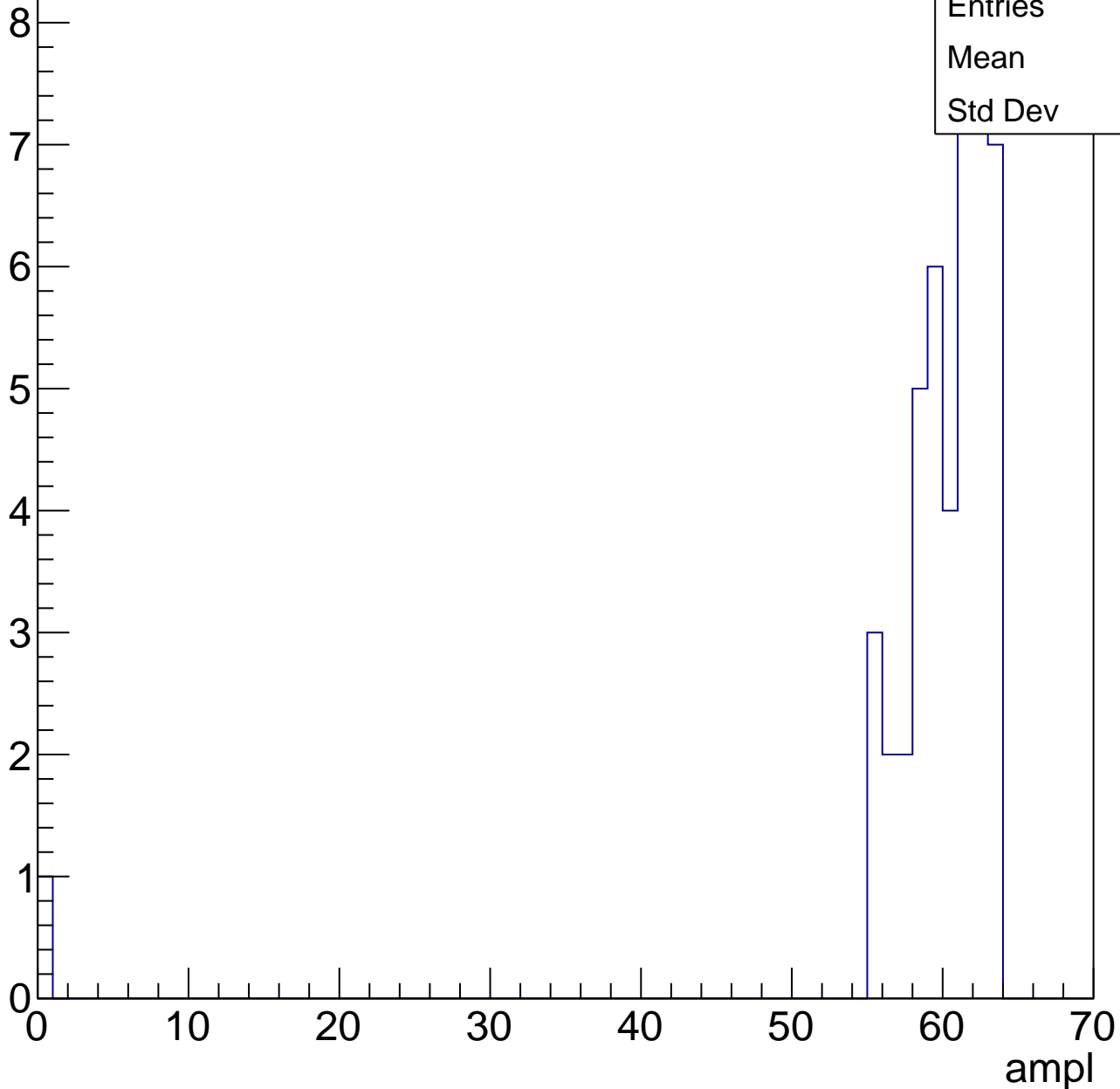


# B1L102S, U12-ch21, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

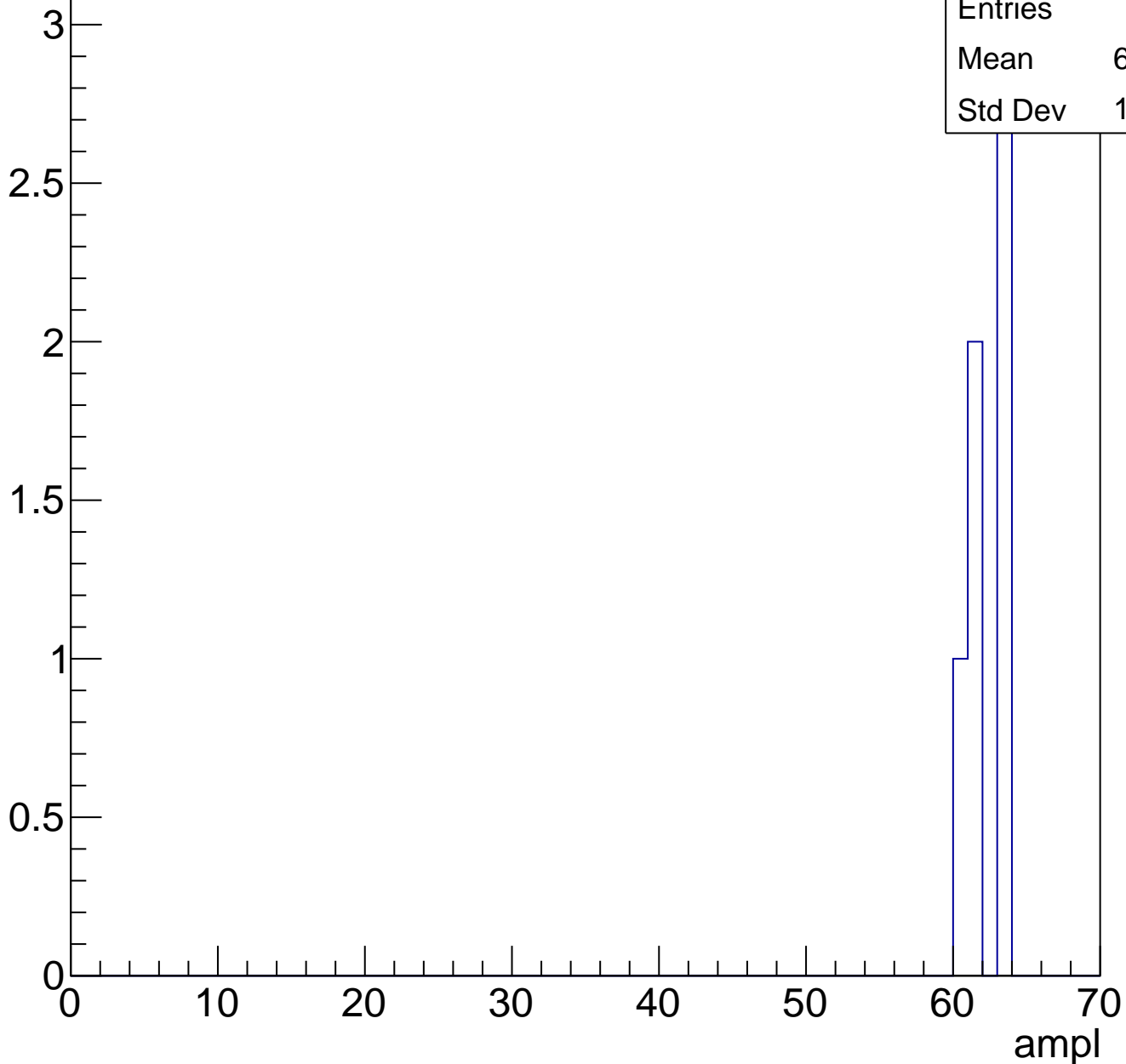
Entries	46
Mean	58.7
Std Dev	9.06



# B1L102S, U12-ch21, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U12-ch21, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U12-ch22, adc0

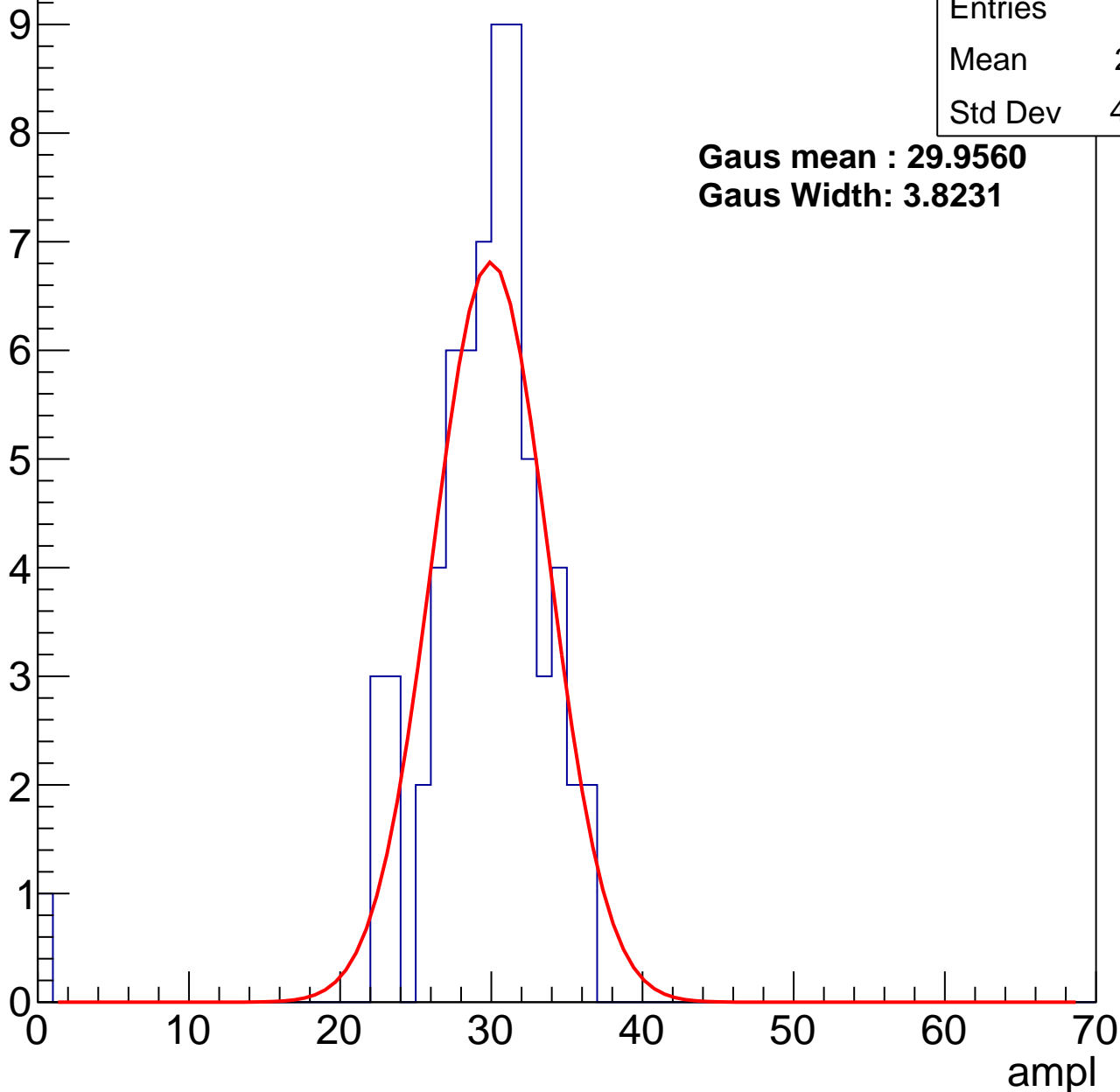
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	28.91
Std Dev	4.926

**Gaus mean : 29.9560**

**Gaus Width: 3.8231**



# B1L102S, U12-ch22, adc1

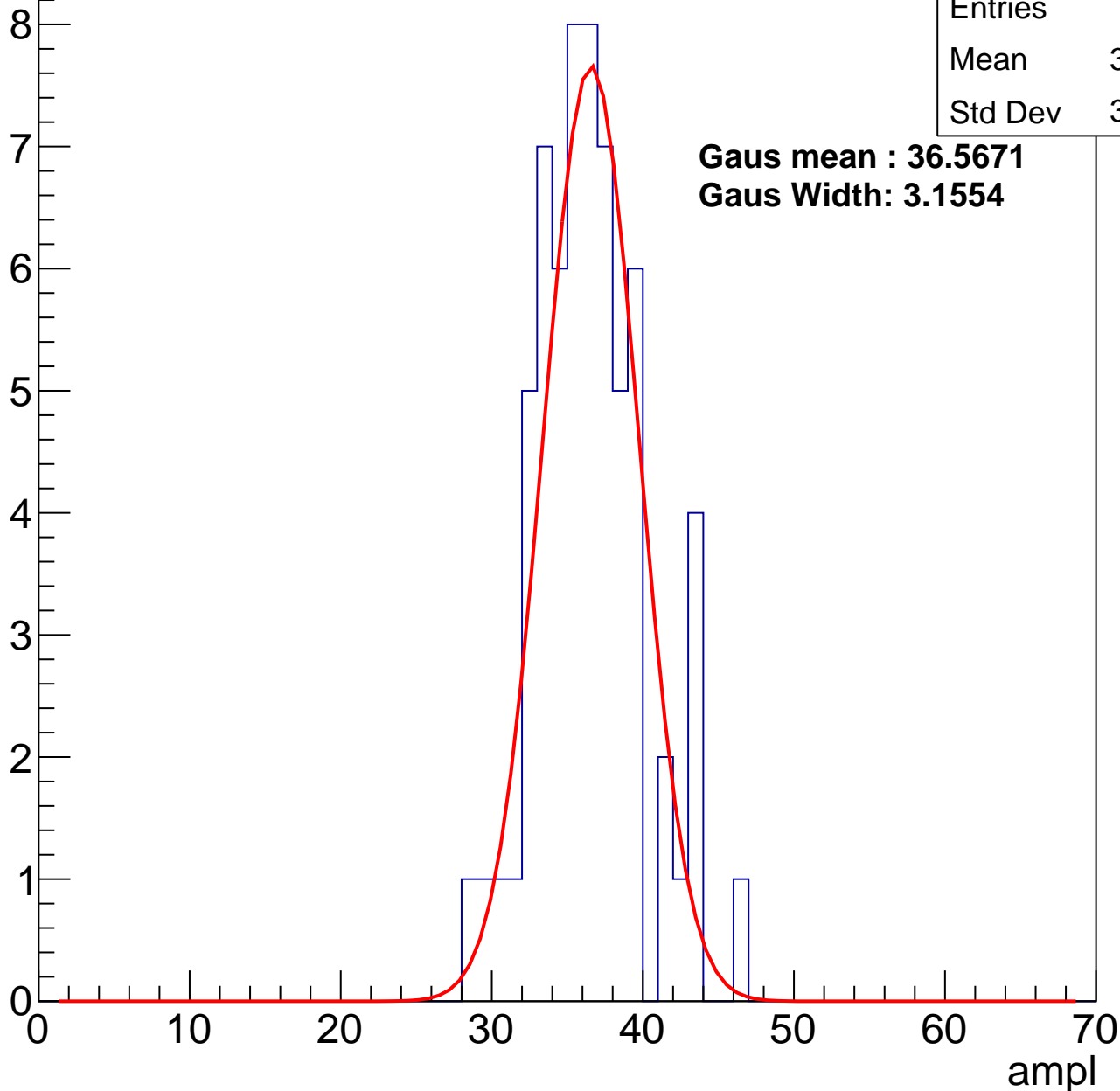
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	36.03
Std Dev	3.562

**Gaus mean : 36.5671**

**Gaus Width: 3.1554**



# B1L102S, U12-ch22, adc2

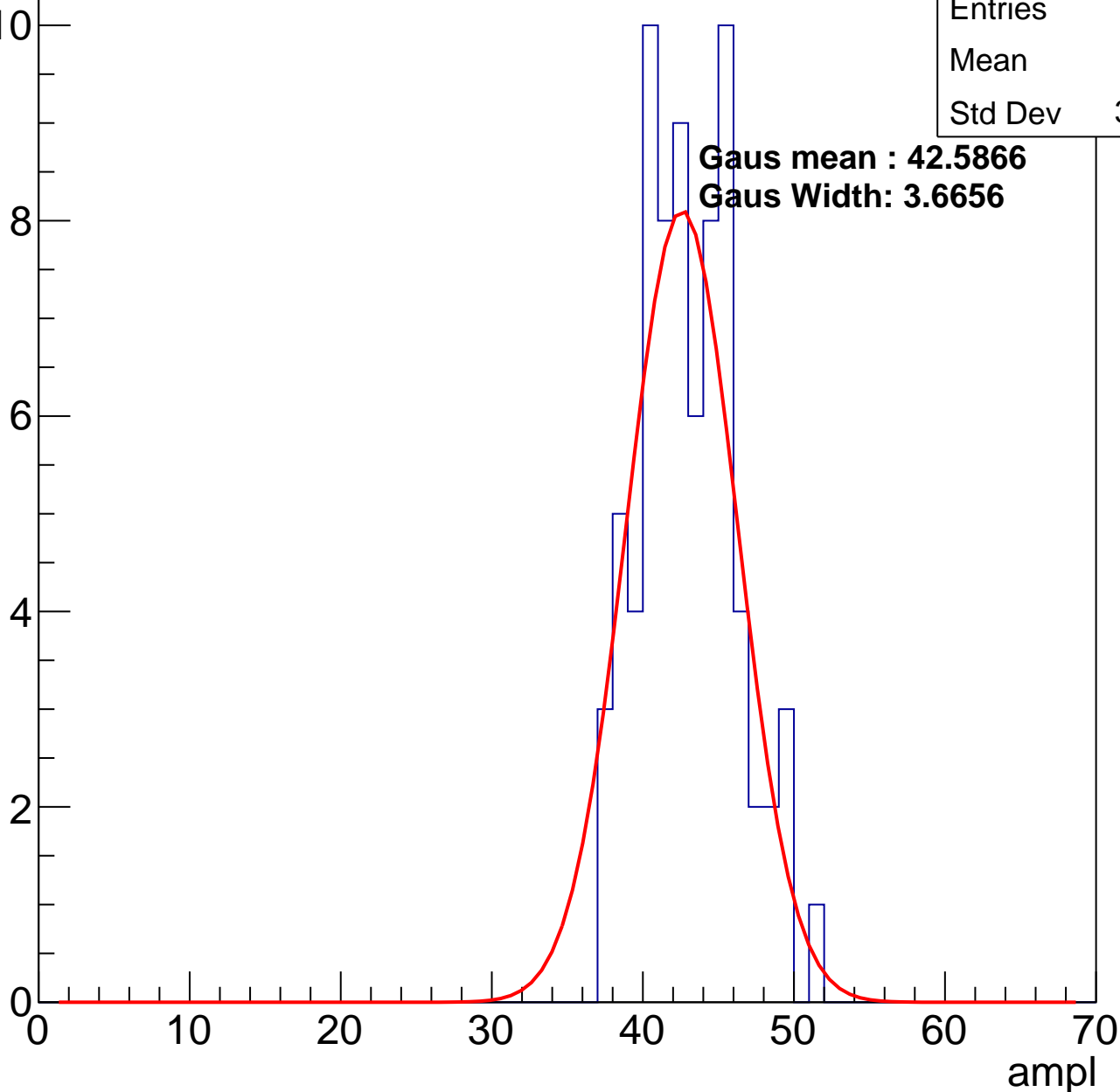
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	75
Mean	42.6
Std Dev	3.171

**Gaus mean : 42.5866**

**Gaus Width: 3.6656**



# B1L102S, U12-ch22, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	72
Mean	50.38
Std Dev	3.297

Entry

10

8

6

4

2

0

0

10

20

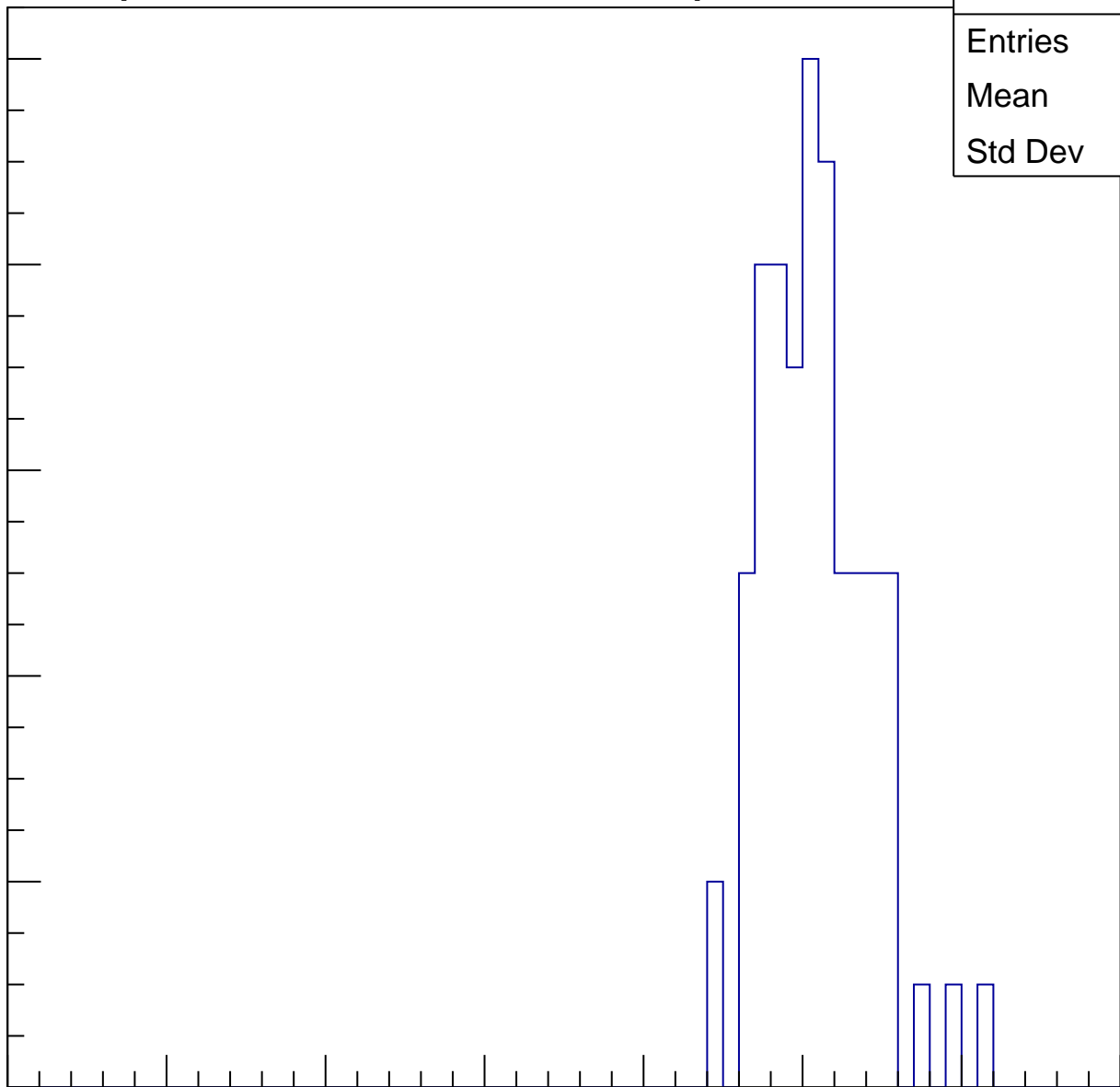
30

40

50

60

ampl

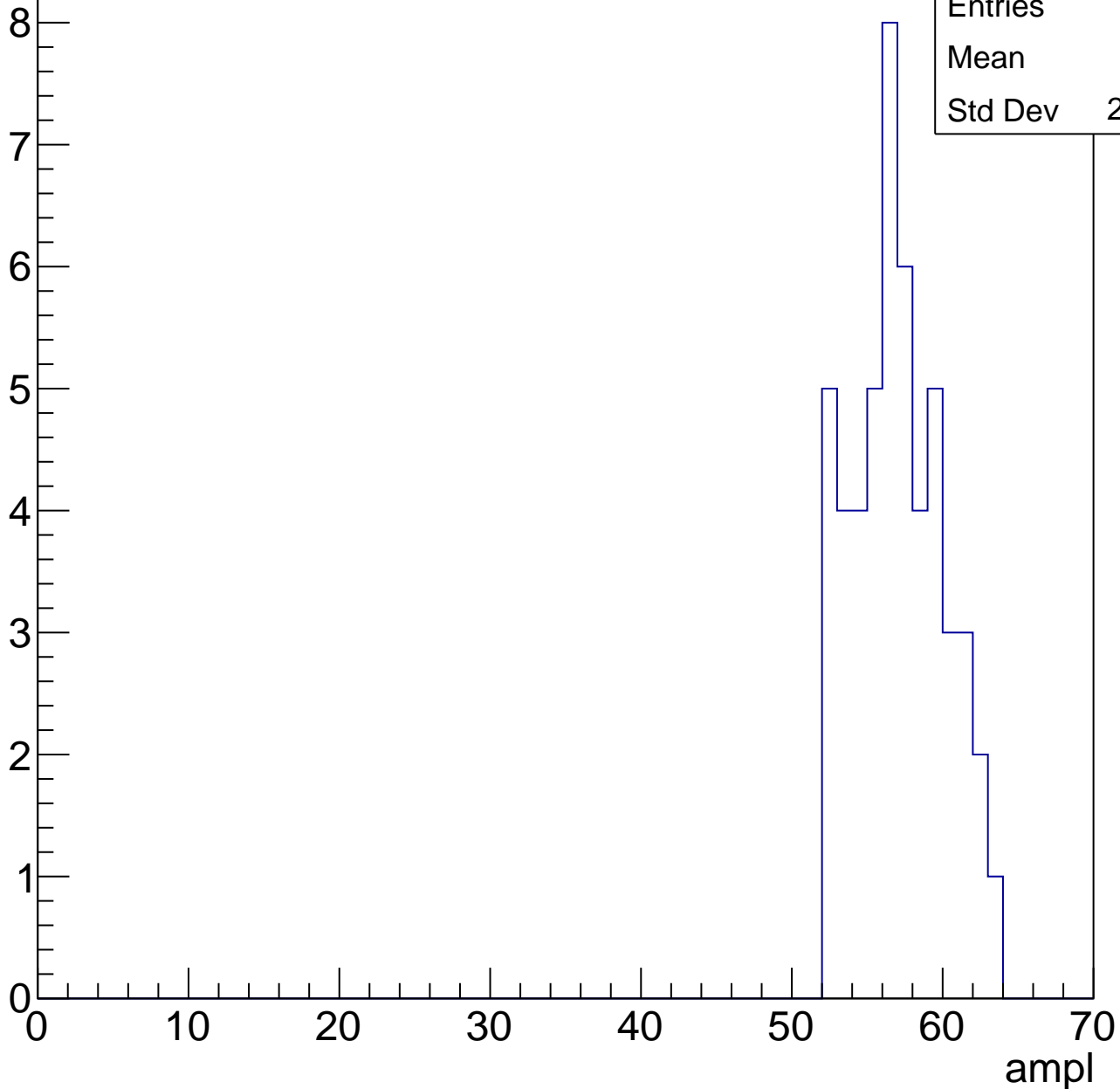


# B1L102S, U12-ch22, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	50
Mean	56.6
Std Dev	2.933

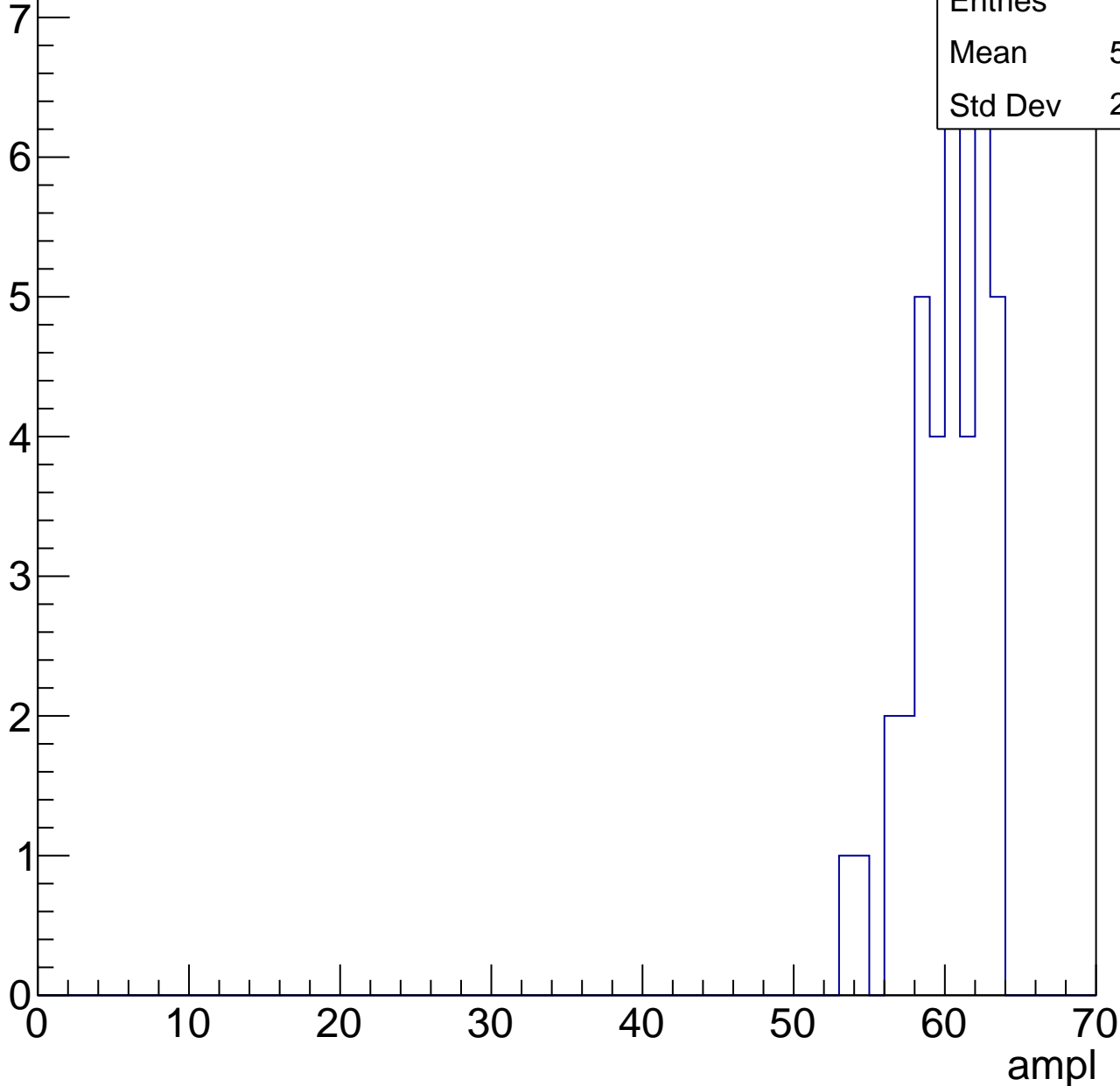


# B1L102S, U12-ch22, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

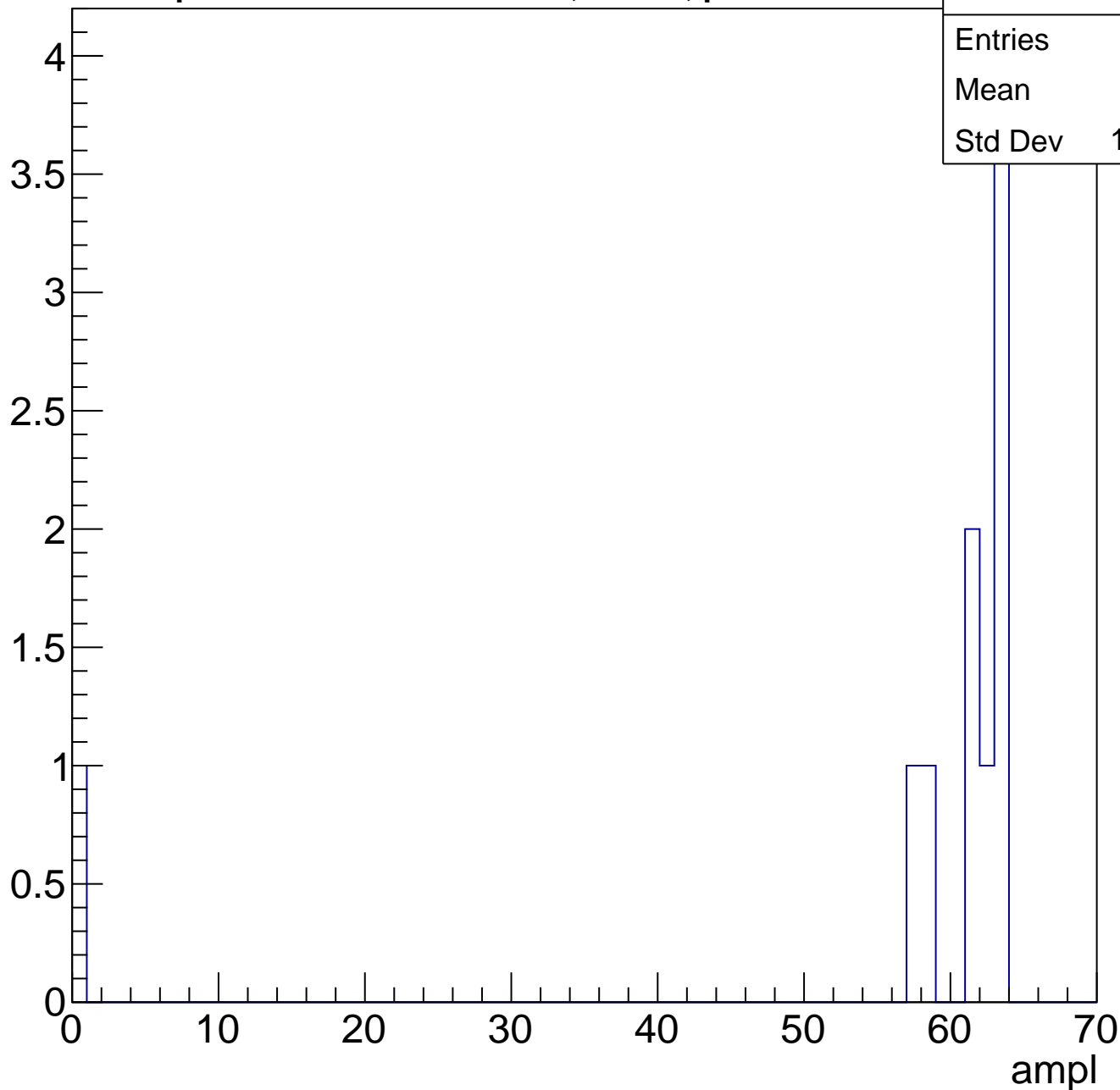
Entries	38
Mean	59.79
Std Dev	2.483



# B1L102S, U12-ch22, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U12-ch22, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	2
Mean	10.5
Std Dev	10.5

# B1L102S, U12-ch23, adc0

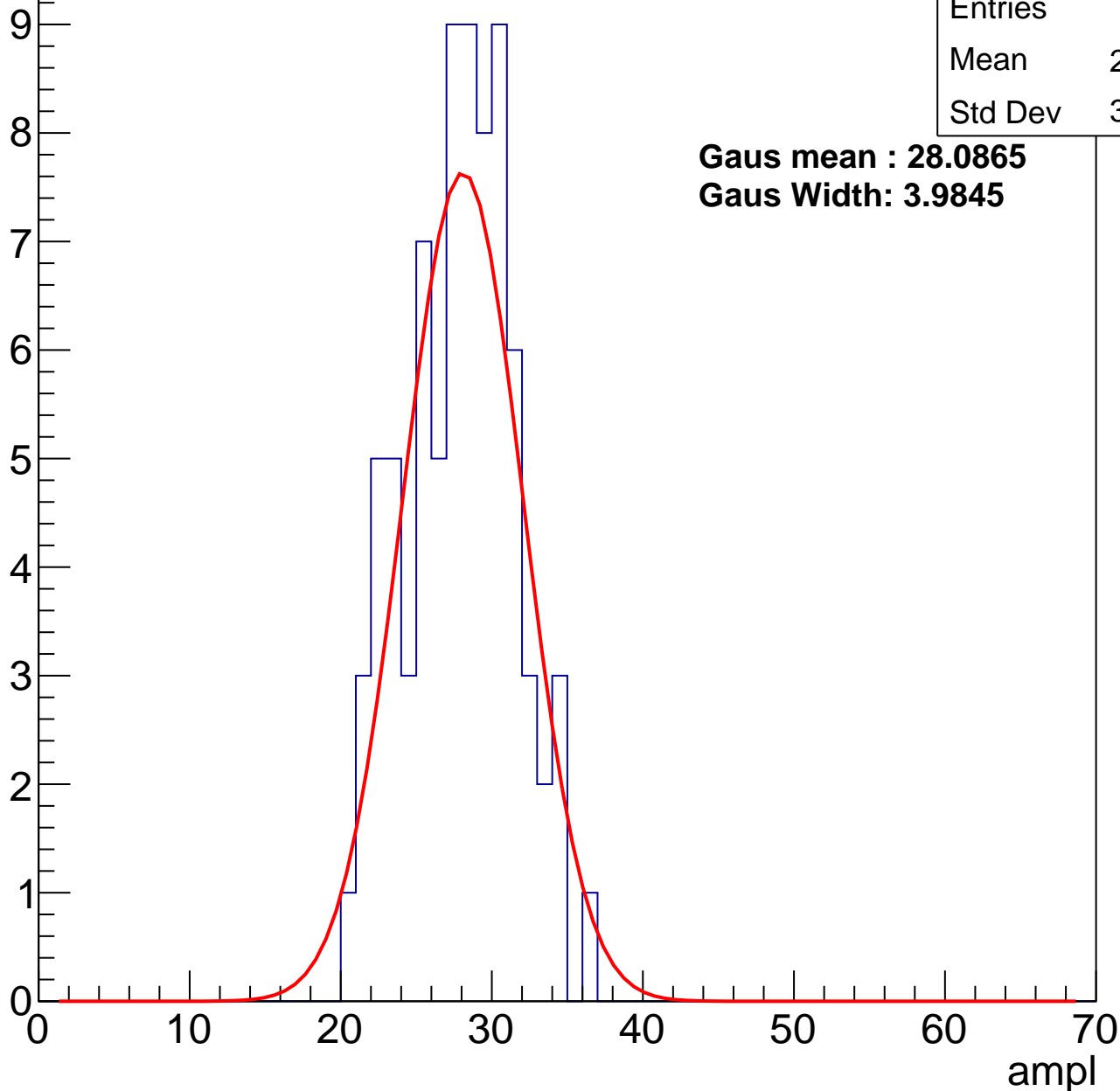
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	79
Mean	27.44
Std Dev	3.557

**Gaus mean : 28.0865**

**Gaus Width: 3.9845**



# B1L102S, U12-ch23, adc1

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	70
Mean	35.79
Std Dev	3.533

**Gaus mean : 36.0711**

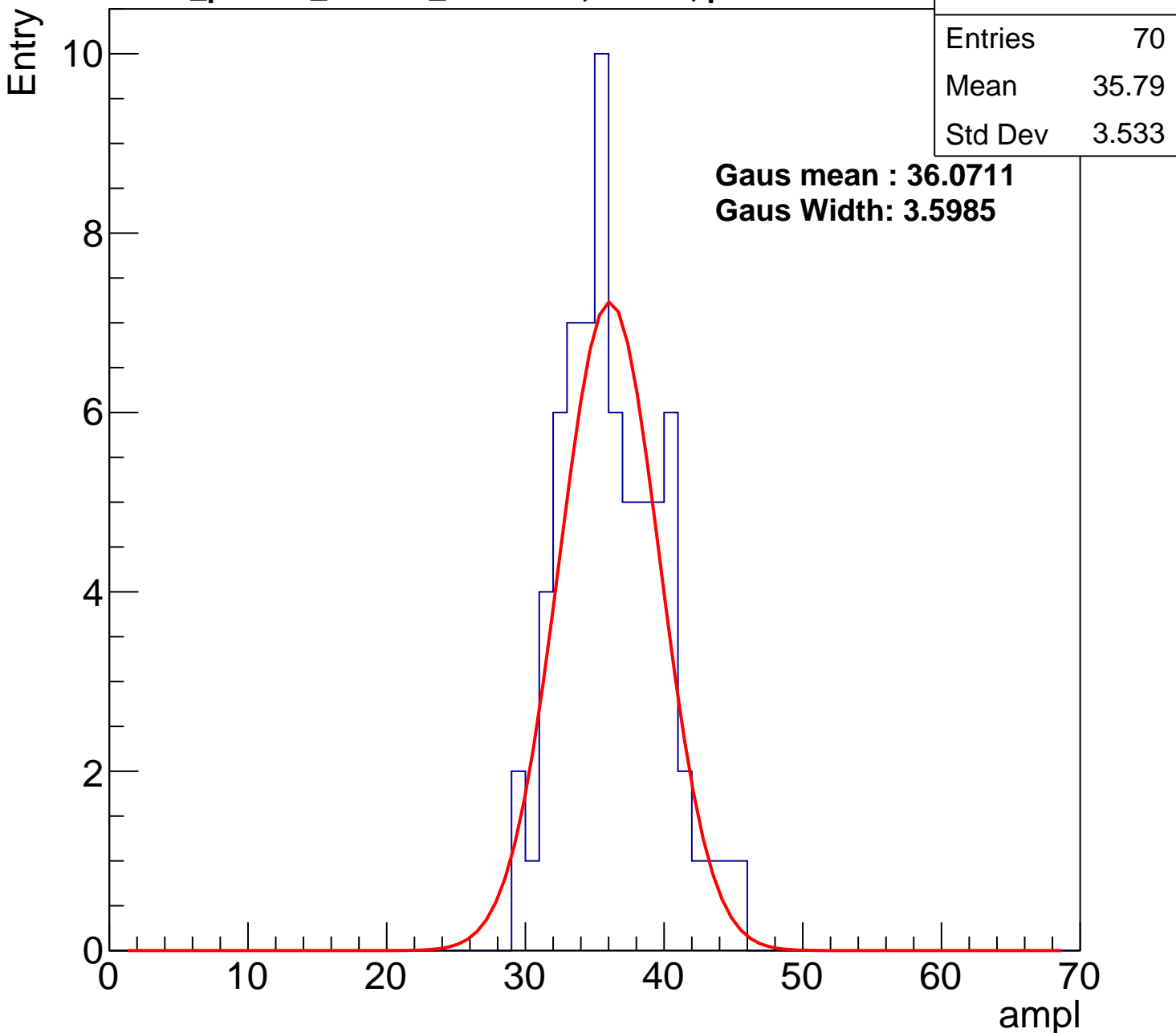
**Gaus Width: 3.5985**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L102S, U12-ch23, adc2

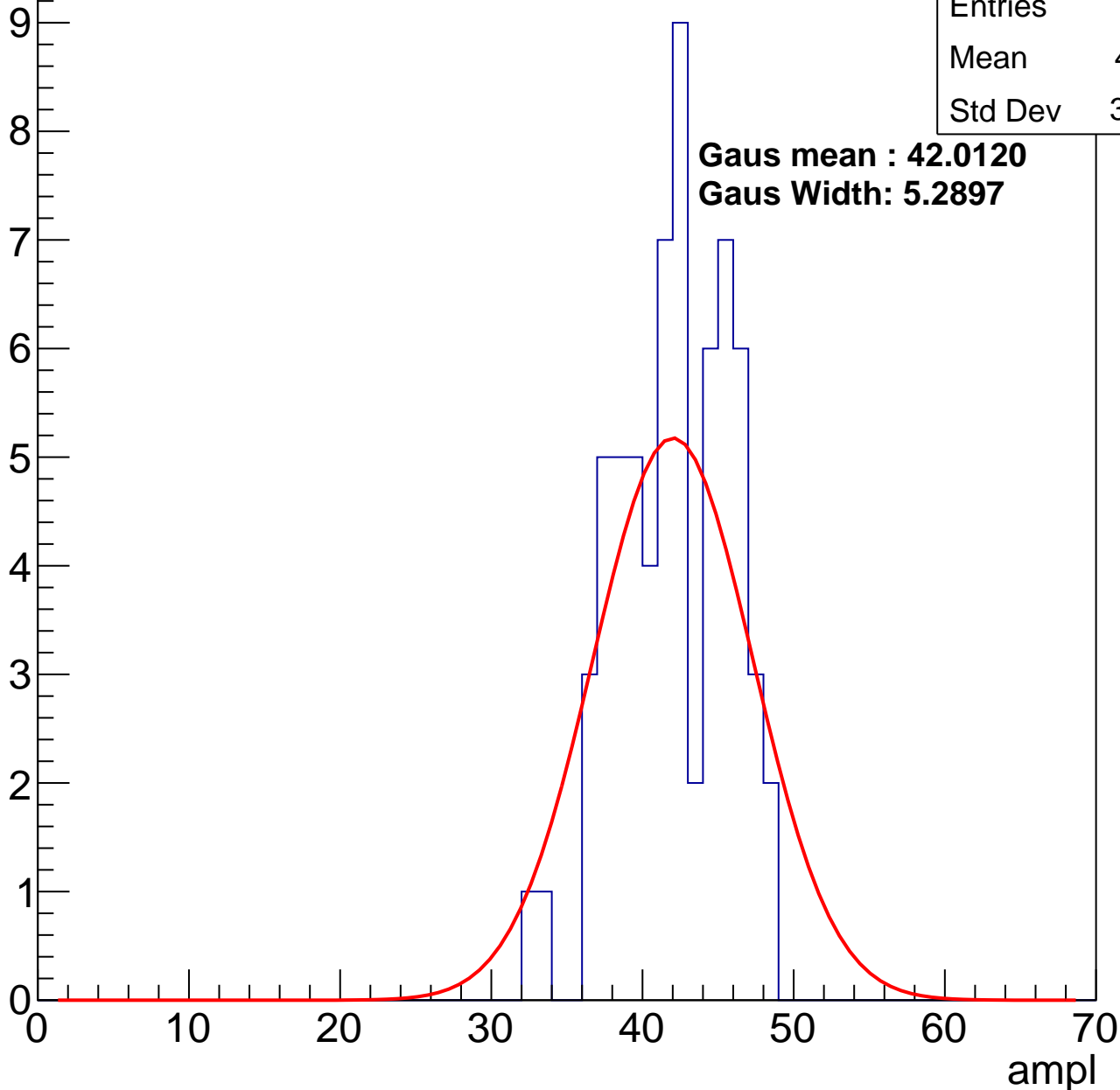
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	41.61
Std Dev	3.659

**Gaus mean : 42.0120**

**Gaus Width: 5.2897**

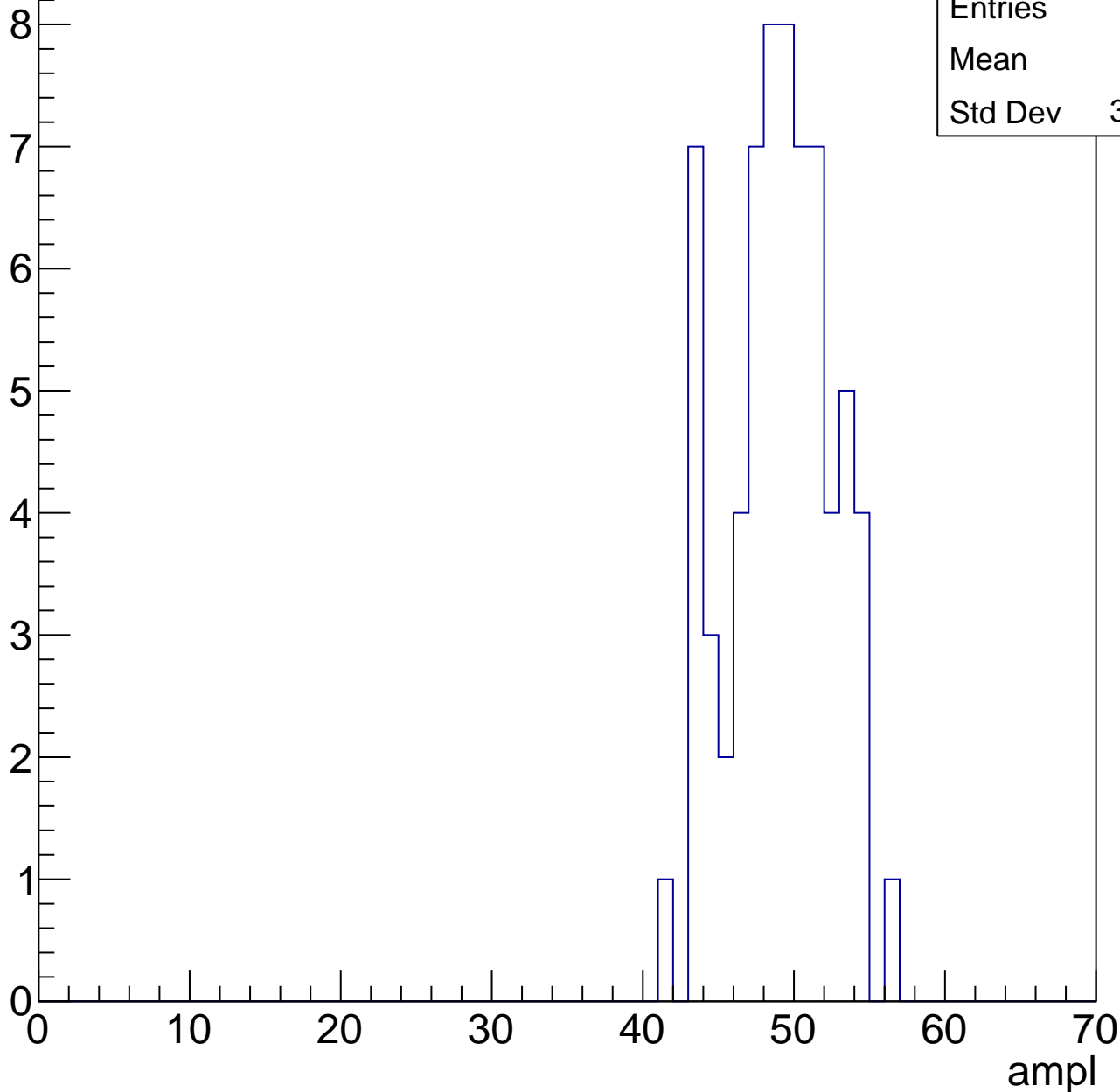


# B1L102S, U12-ch23, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	48.6
Std Dev	3.396

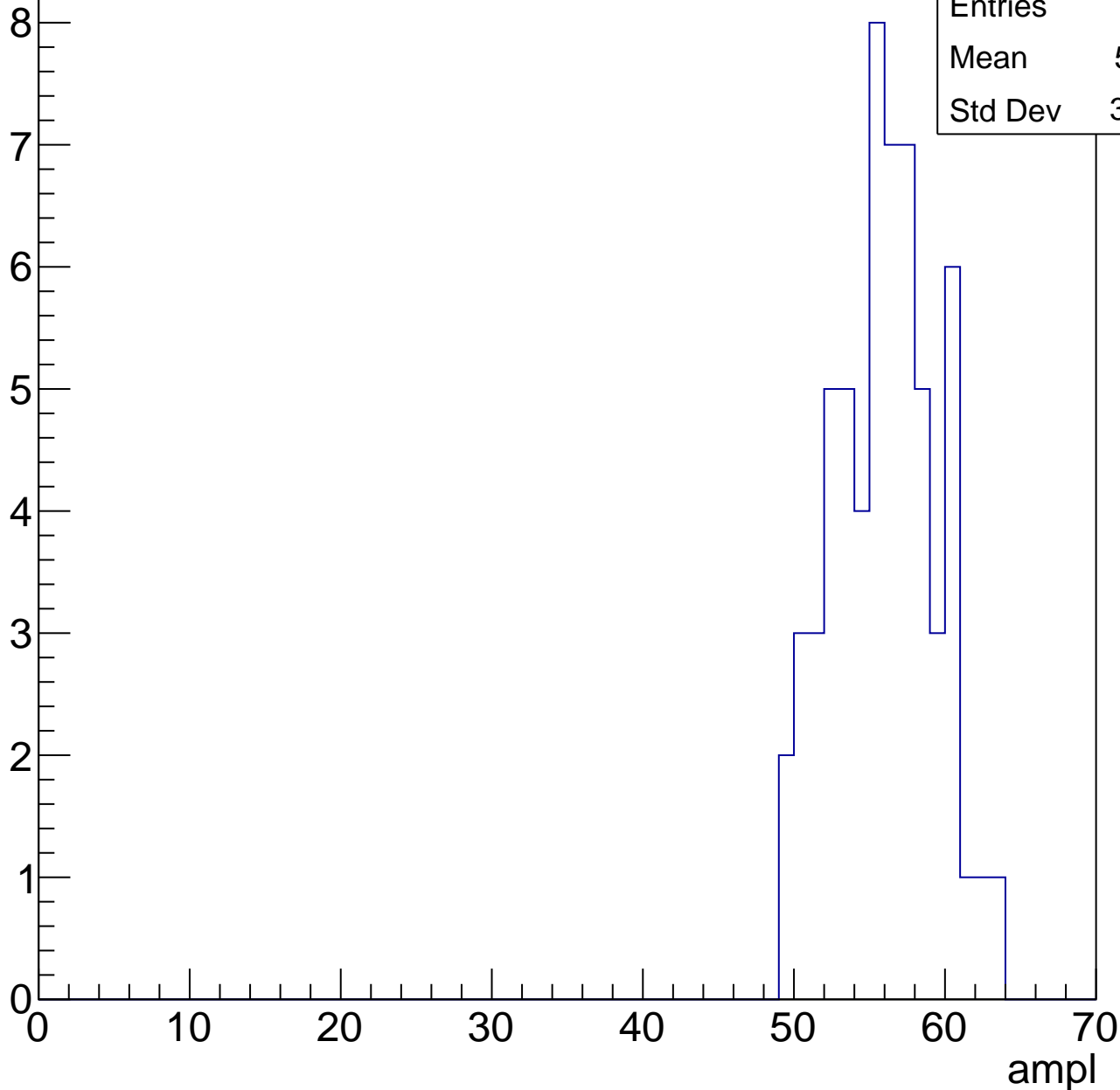


# B1L102S, U12-ch23, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	55.51
Std Dev	3.327

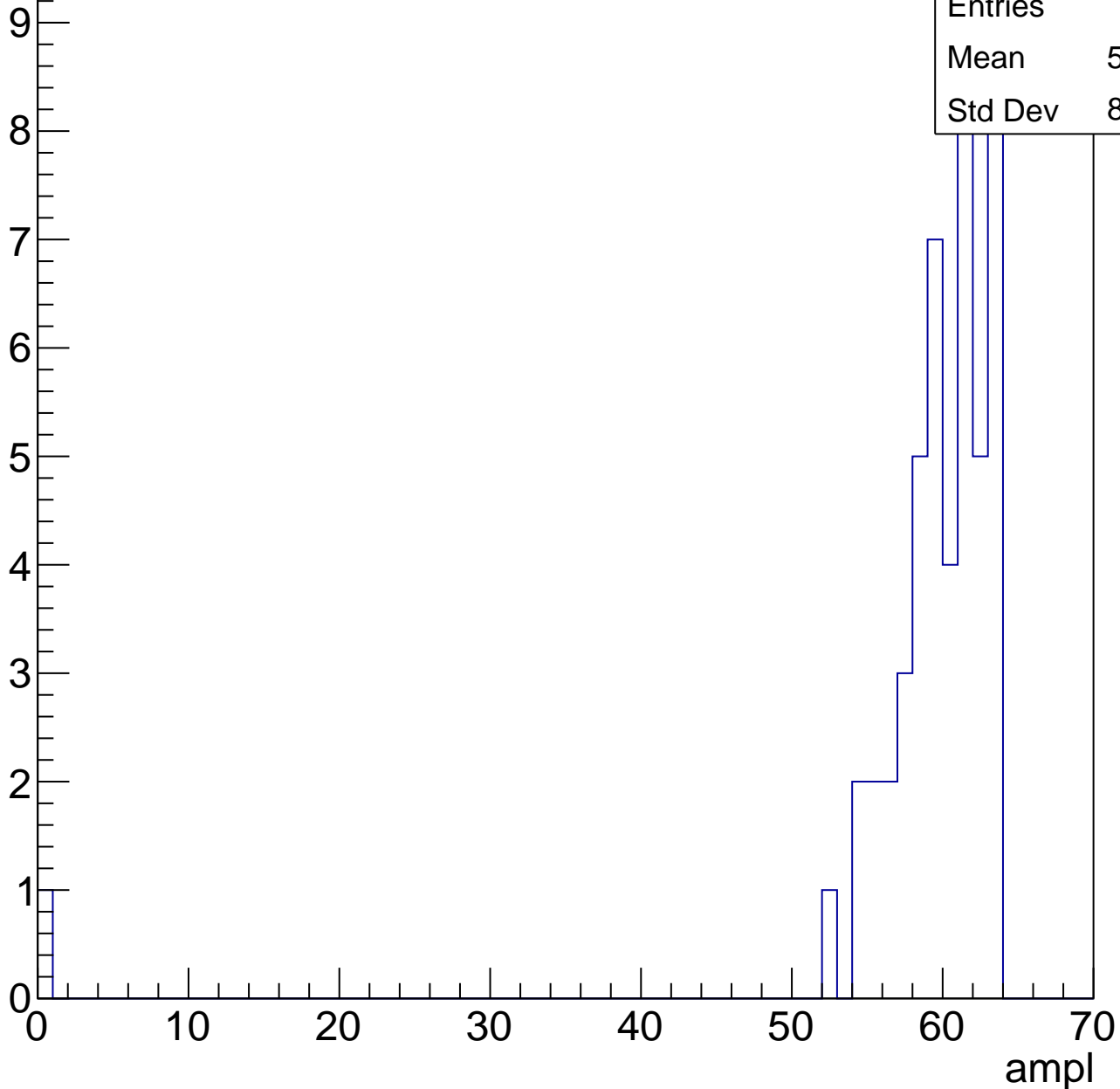


# B1L102S, U12-ch23, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

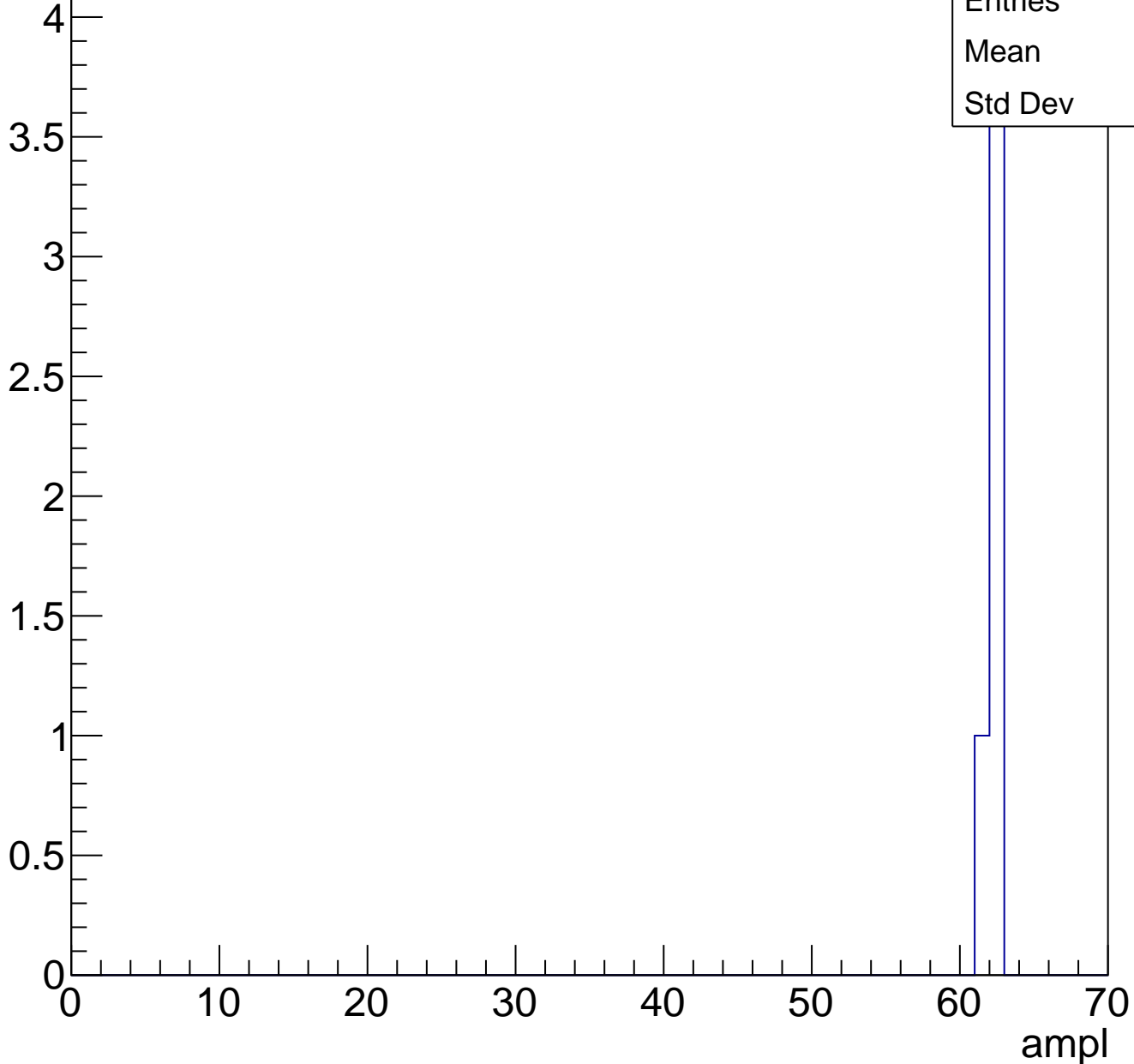
Entries	49
Mean	58.39
Std Dev	8.868



# B1L102S, U12-ch23, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U12-ch23, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U12-ch24, adc0

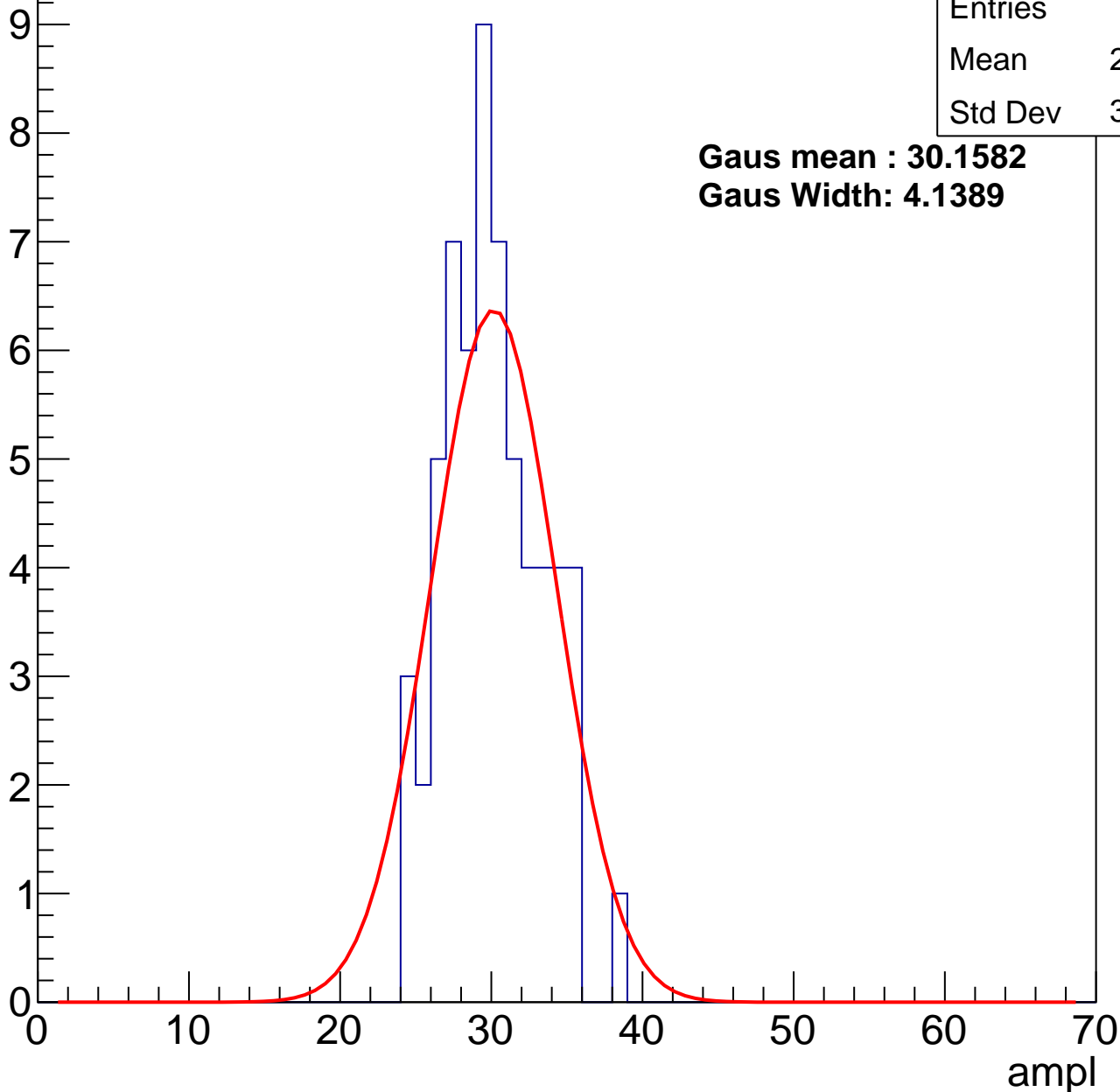
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	29.66
Std Dev	3.167

**Gaus mean : 30.1582**

**Gaus Width: 4.1389**



# B1L102S, U12-ch24, adc1

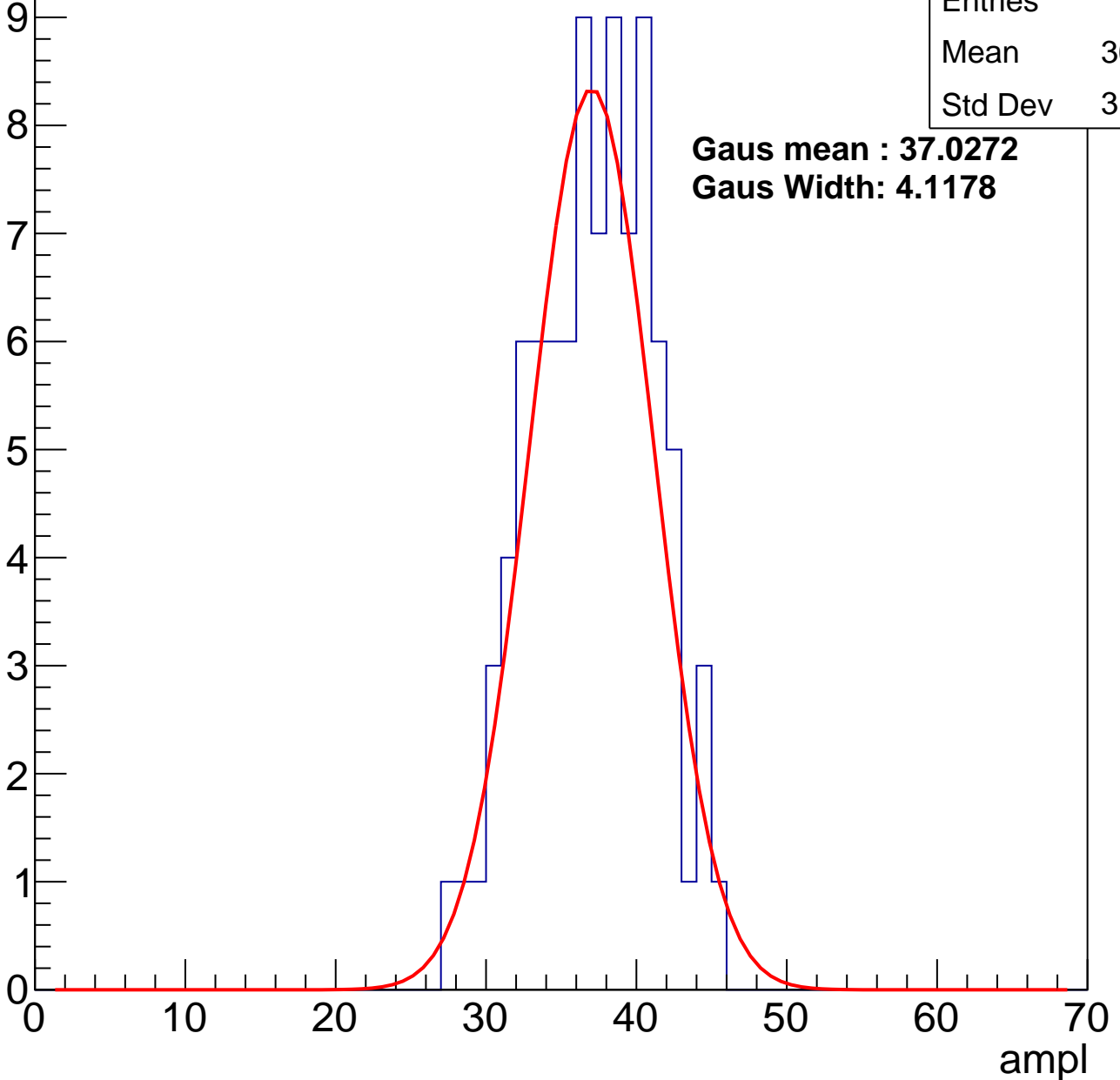
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	91
Mean	36.66
Std Dev	3.984

**Gaus mean : 37.0272**

**Gaus Width: 4.1178**



# B1L102S, U12-ch24, adc2

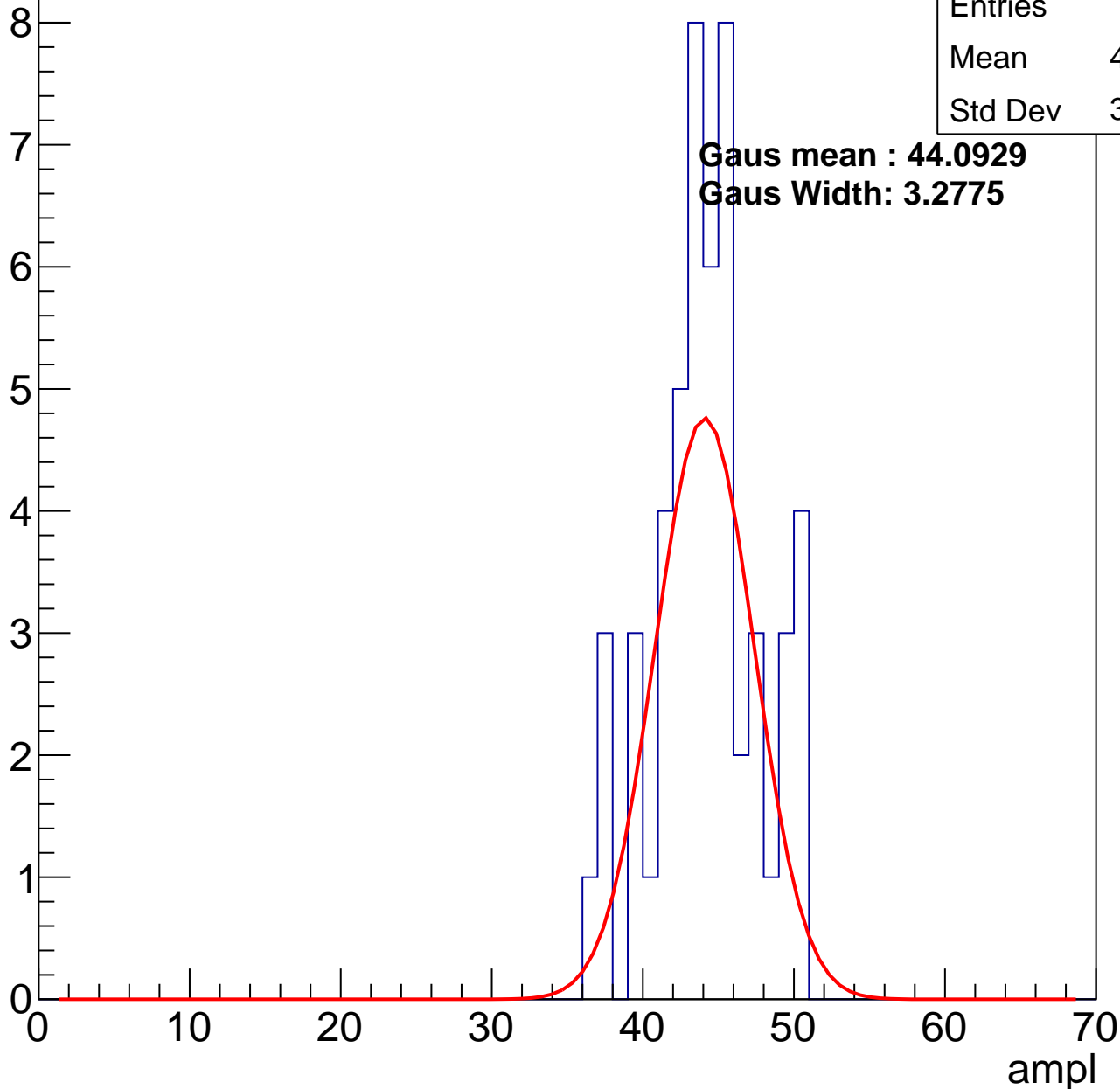
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	52
Mean	43.73
Std Dev	3.509

**Gaus mean : 44.0929**

**Gaus Width: 3.2775**

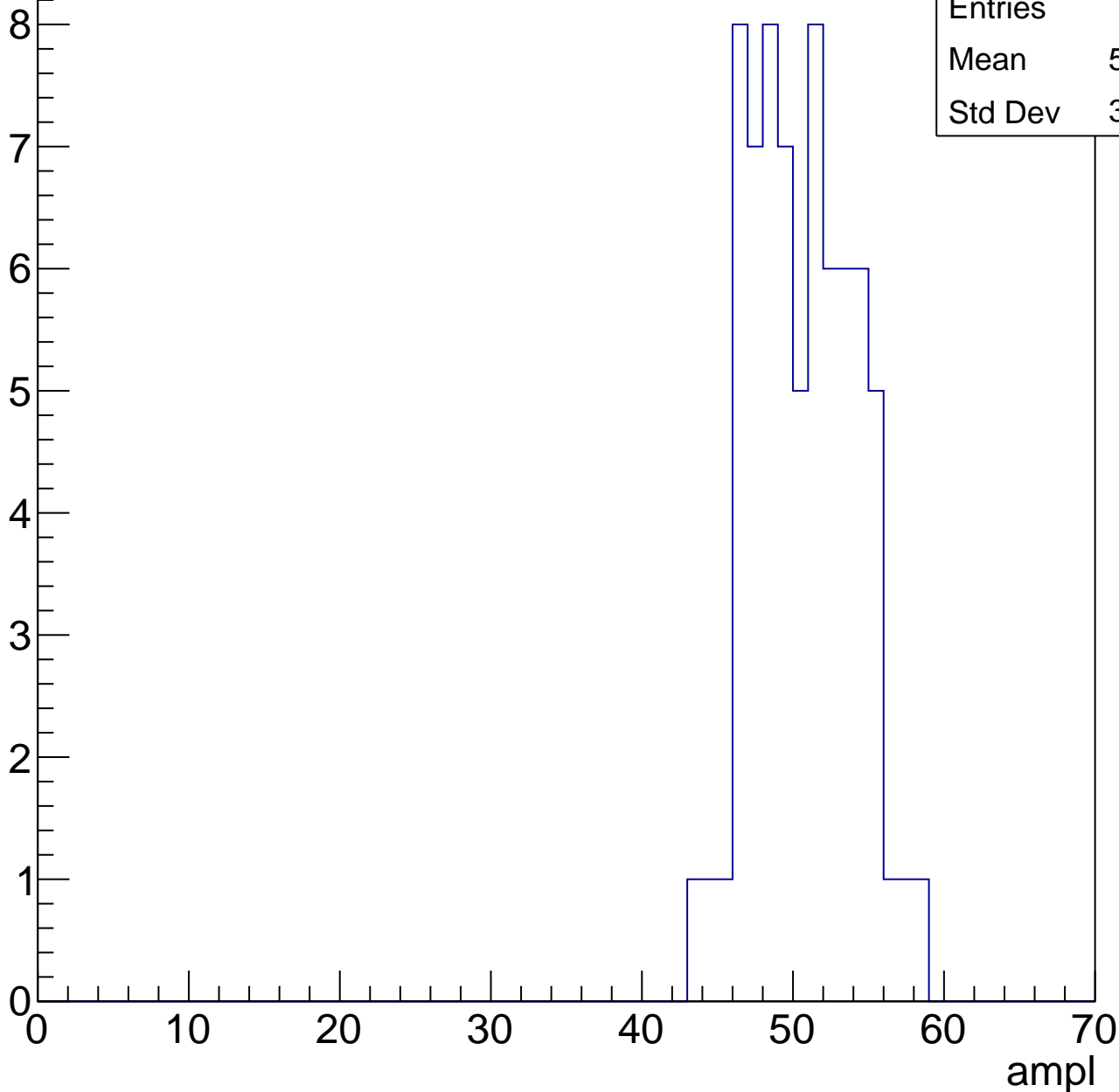


# B1L102S, U12-ch24, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	72
Mean	50.19
Std Dev	3.319

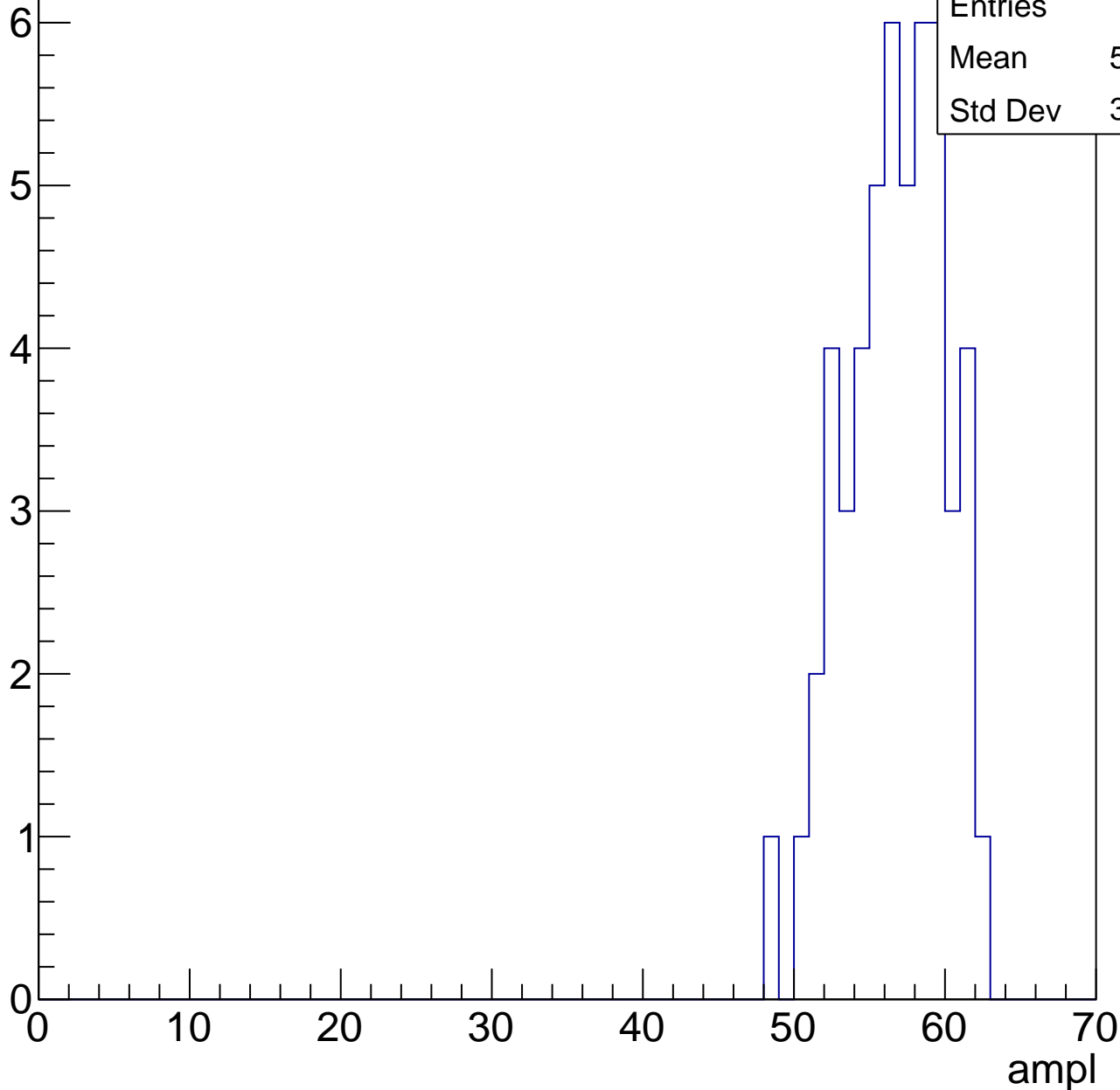


# B1L102S, U12-ch24, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	51
Mean	56.22
Std Dev	3.213

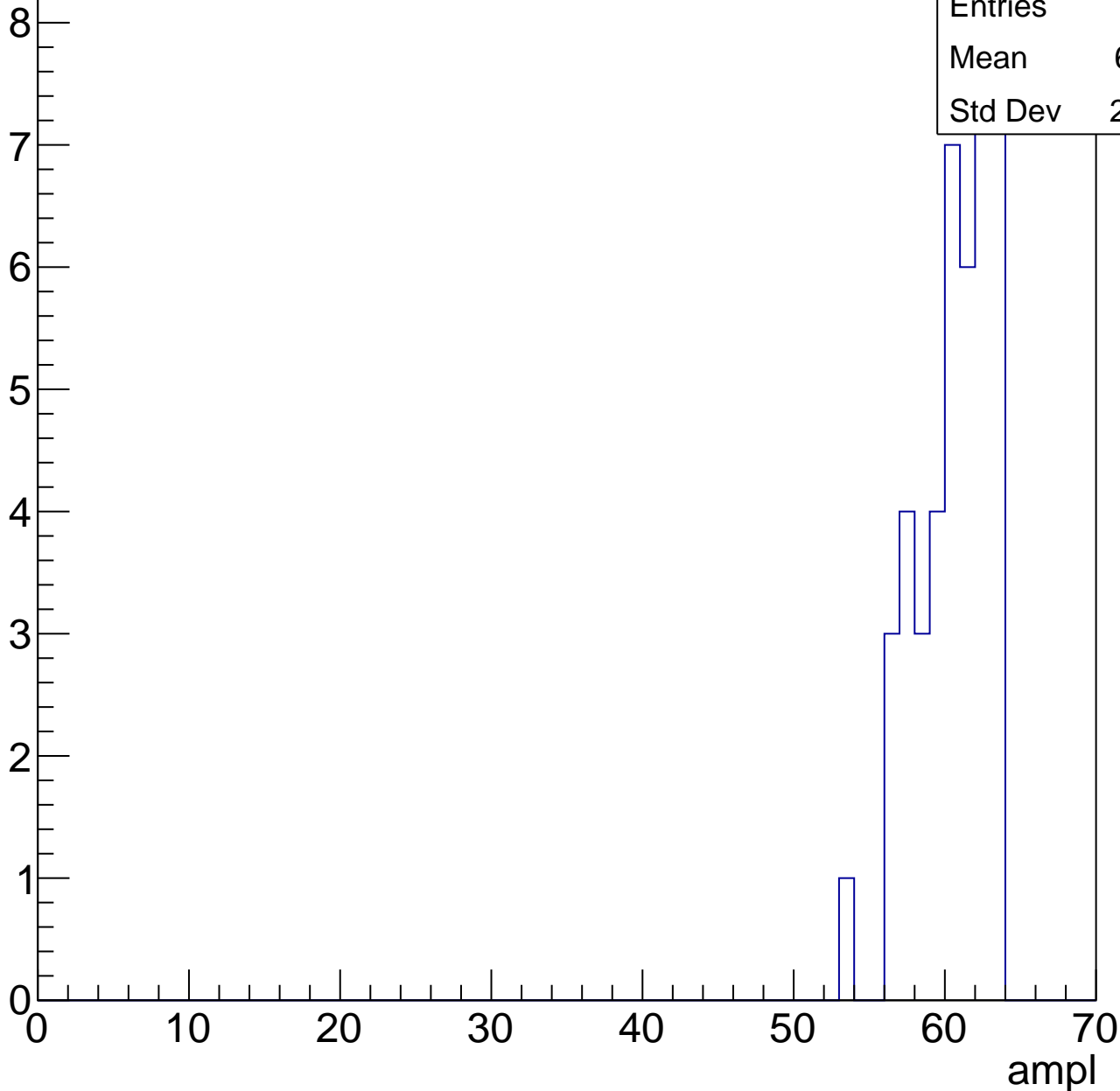


# B1L102S, U12-ch24, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	44
Mean	60.11
Std Dev	2.424



# B1L102S, U12-ch24, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U12-ch24, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U12-ch25, adc0

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	78
Mean	30.73
Std Dev	3.054

**Gaus mean : 30.9547**

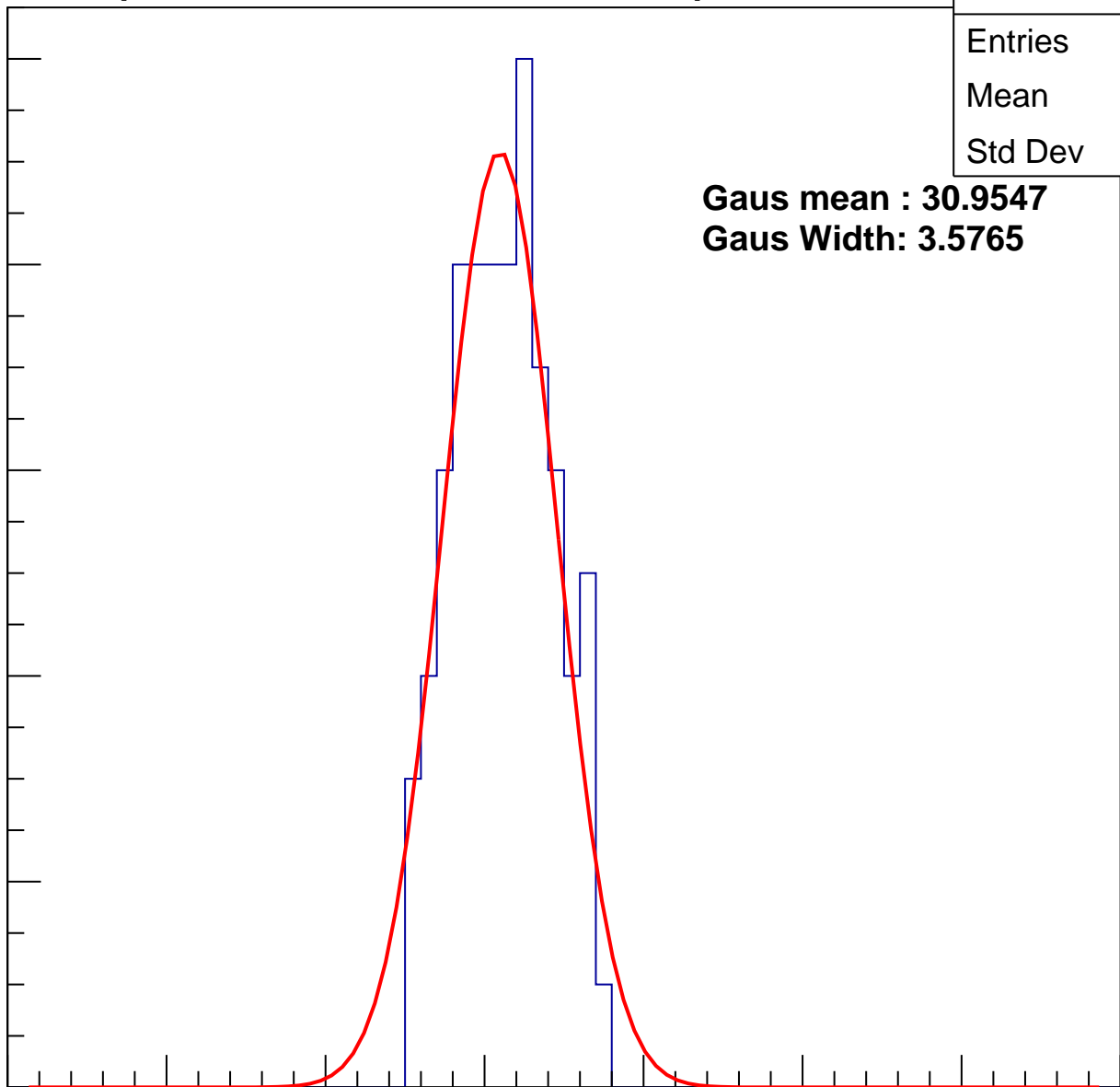
**Gaus Width: 3.5765**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L102S, U12-ch25, adc1

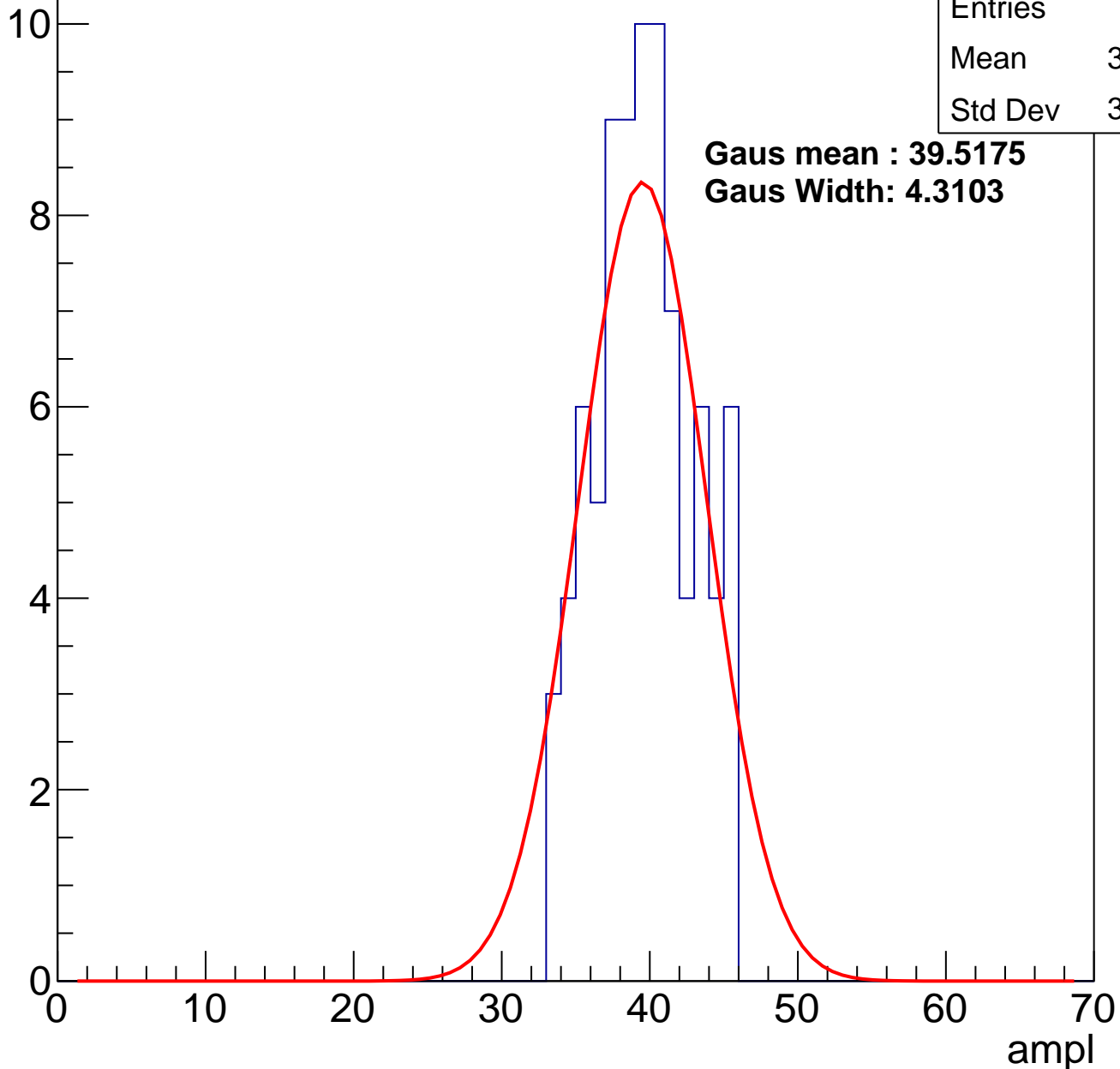
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	83
Mean	39.14
Std Dev	3.253

**Gaus mean : 39.5175**

**Gaus Width: 4.3103**

Entry



# B1L102S, U12-ch25, adc2

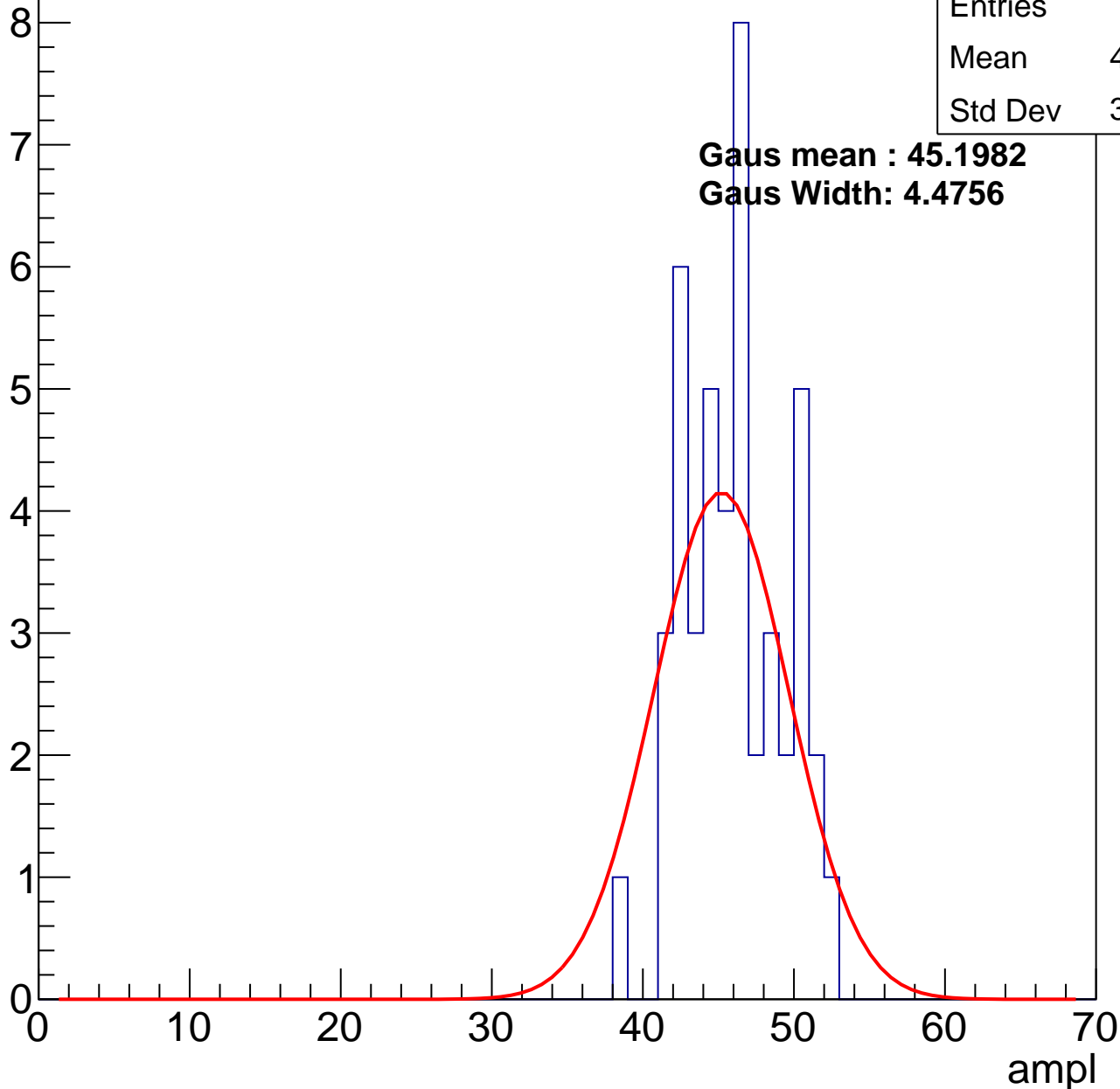
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	45
Mean	45.56
Std Dev	3.249

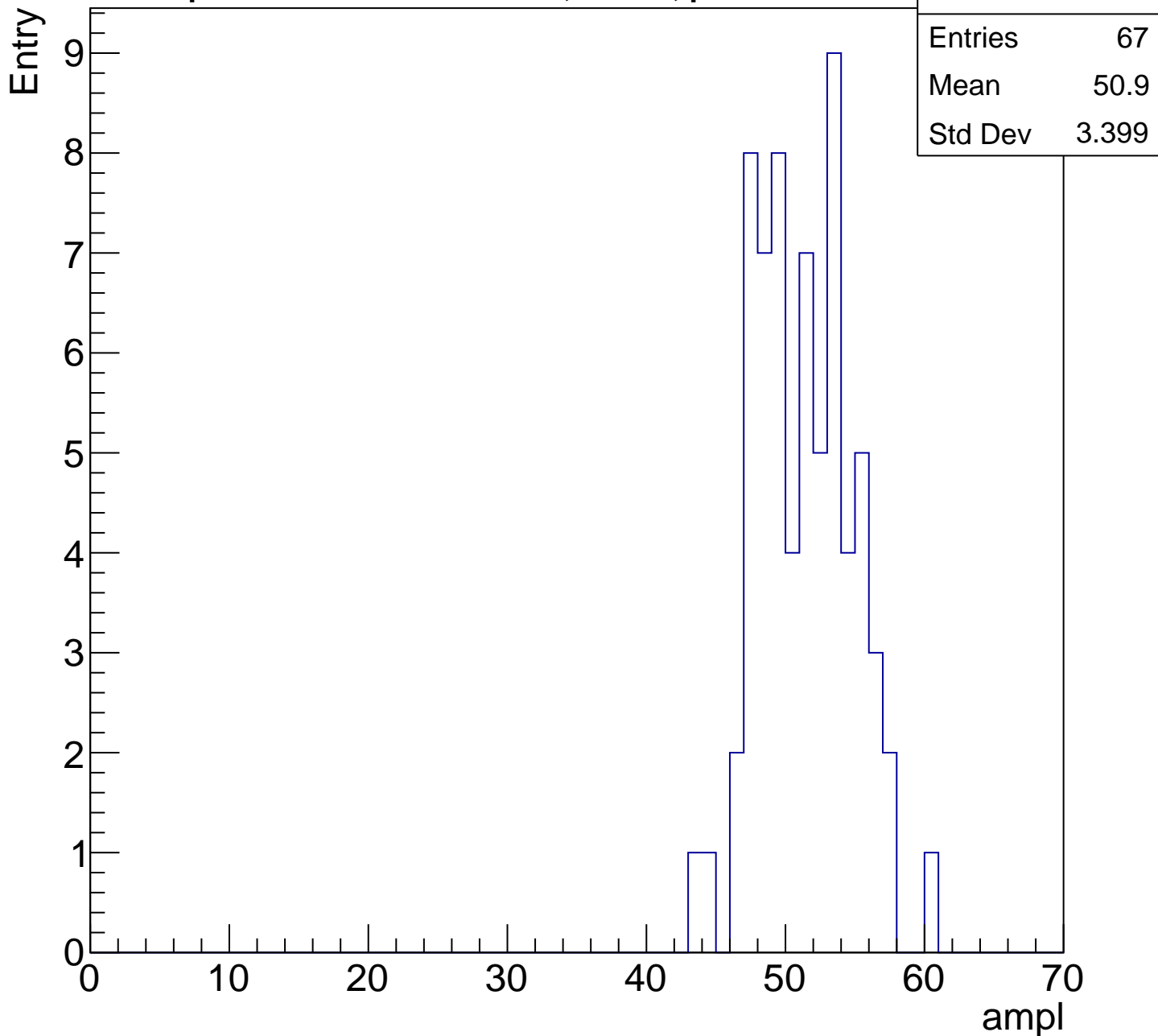
**Gaus mean : 45.1982**

**Gaus Width: 4.4756**



# B1L102S, U12-ch25, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

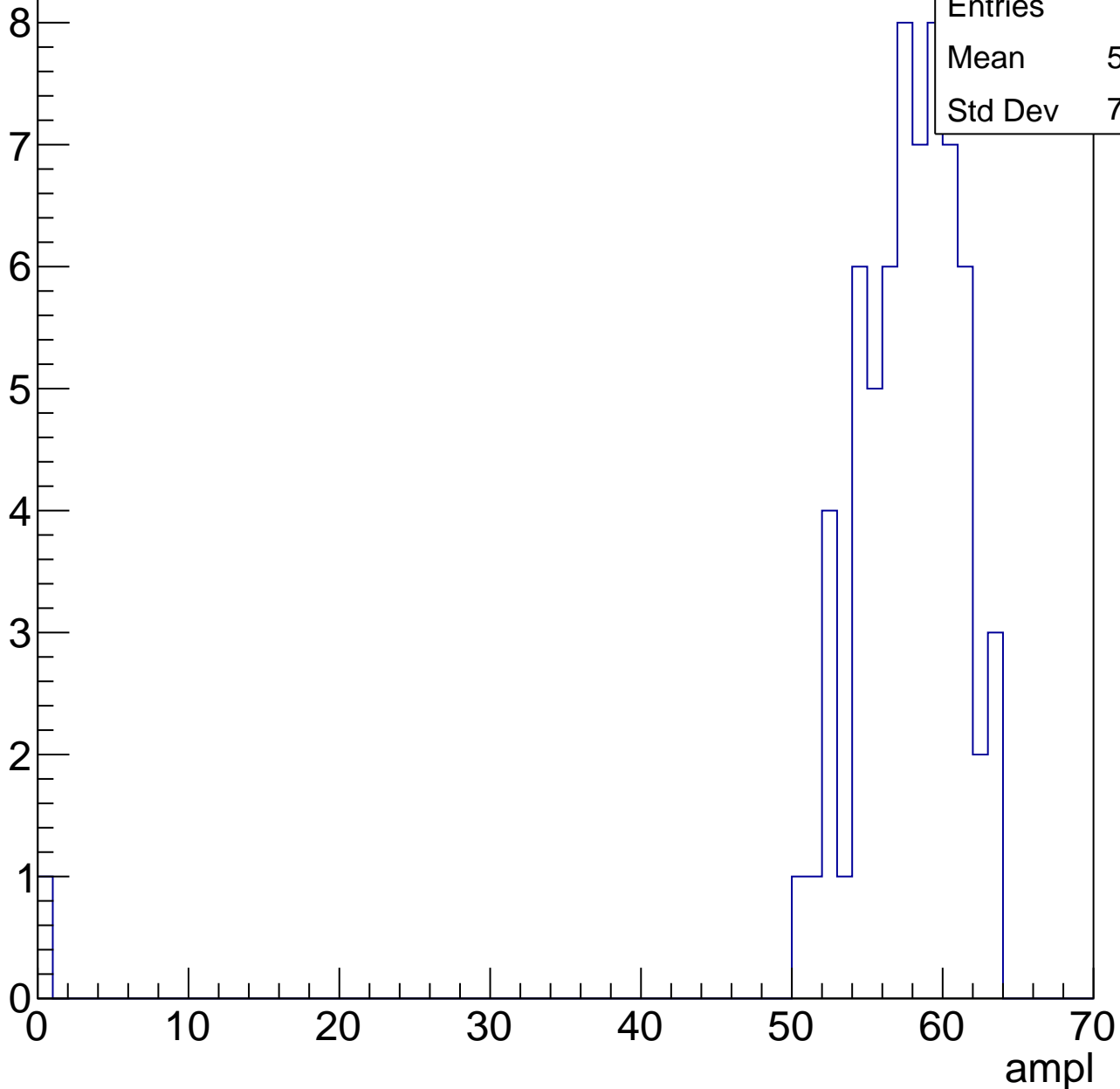


# B1L102S, U12-ch25, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	56.52
Std Dev	7.658

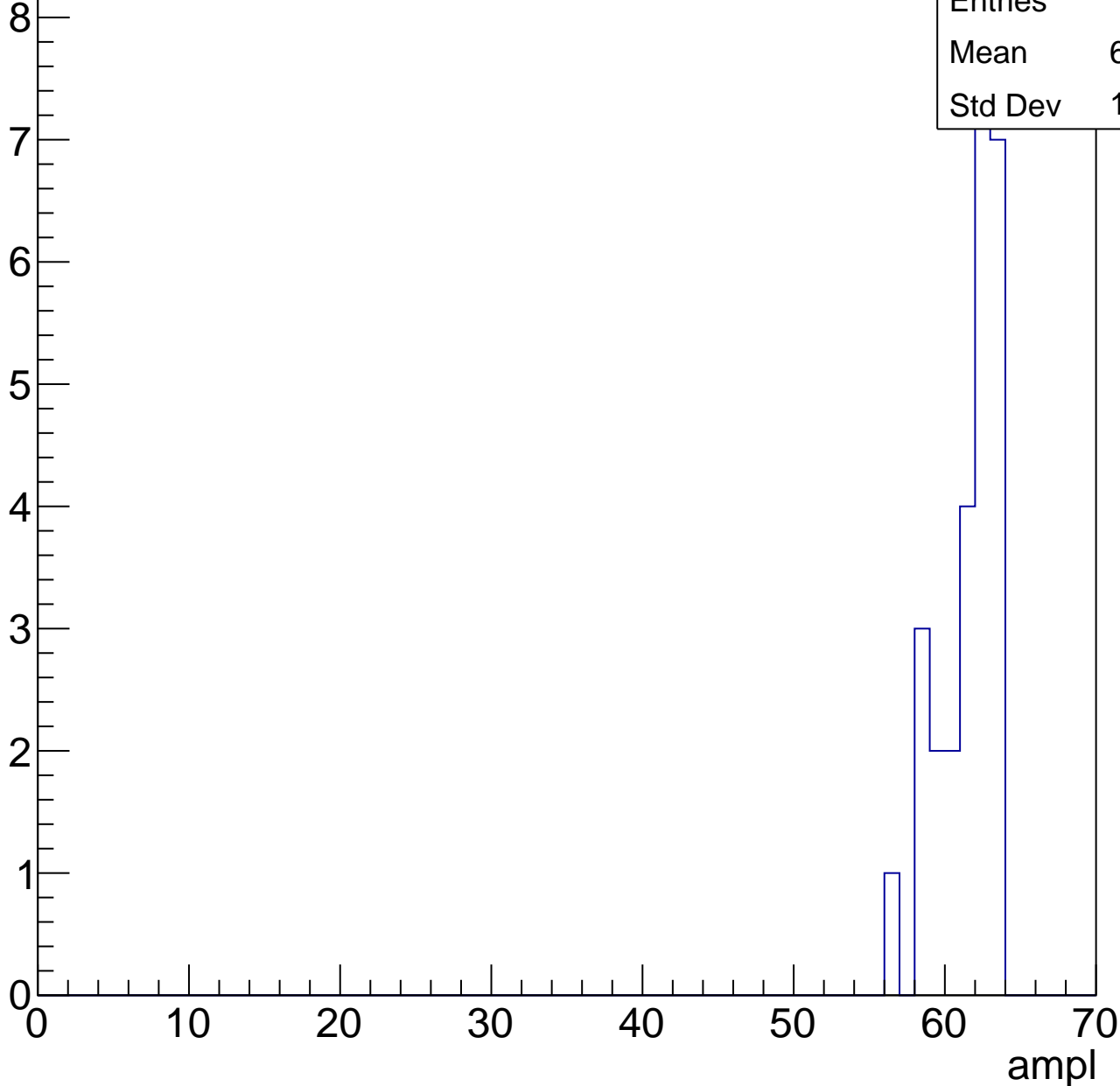


# B1L102S, U12-ch25, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	27
Mean	61.07
Std Dev	1.904



# B1L102S, U12-ch25, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0



# B1L102S, U12-ch25, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U12-ch26, adc0

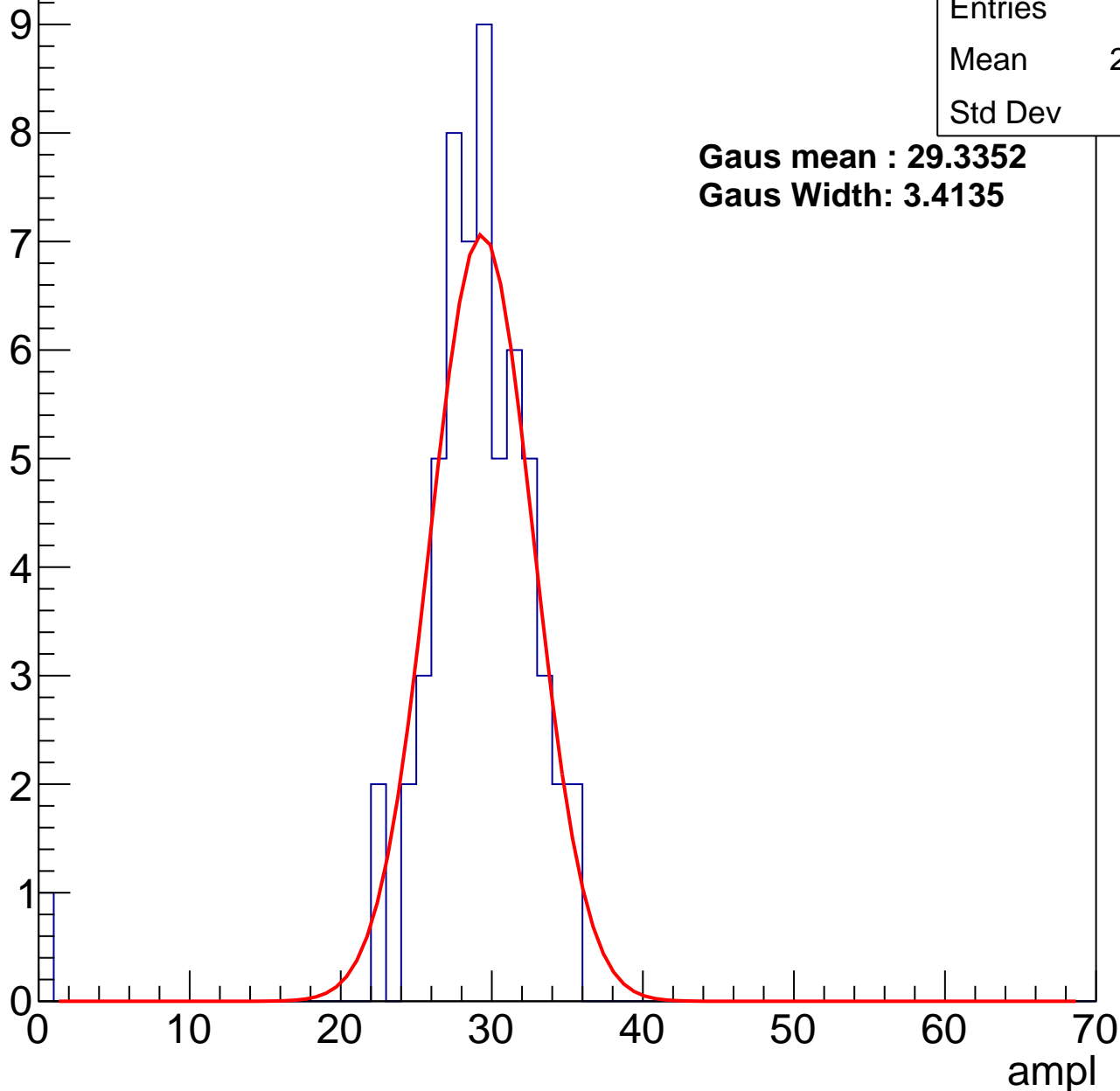
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	60
Mean	28.38
Std Dev	4.73

**Gaus mean : 29.3352**

**Gaus Width: 3.4135**



# B1L102S, U12-ch26, adc1

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	88
Mean	36.41
Std Dev	3.713

**Gaus mean : 36.5666**

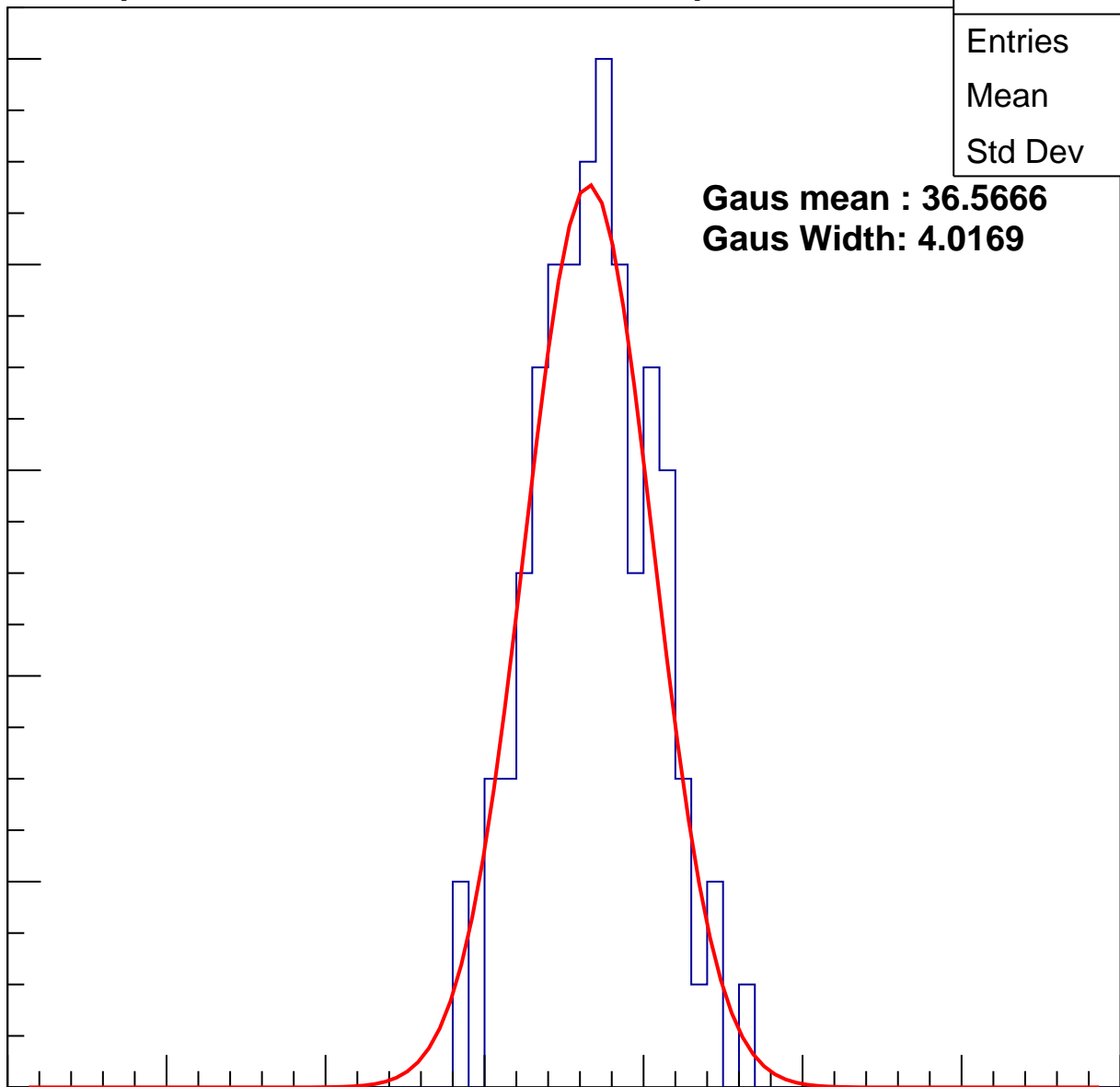
**Gaus Width: 4.0169**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L102S, U12-ch26, adc2

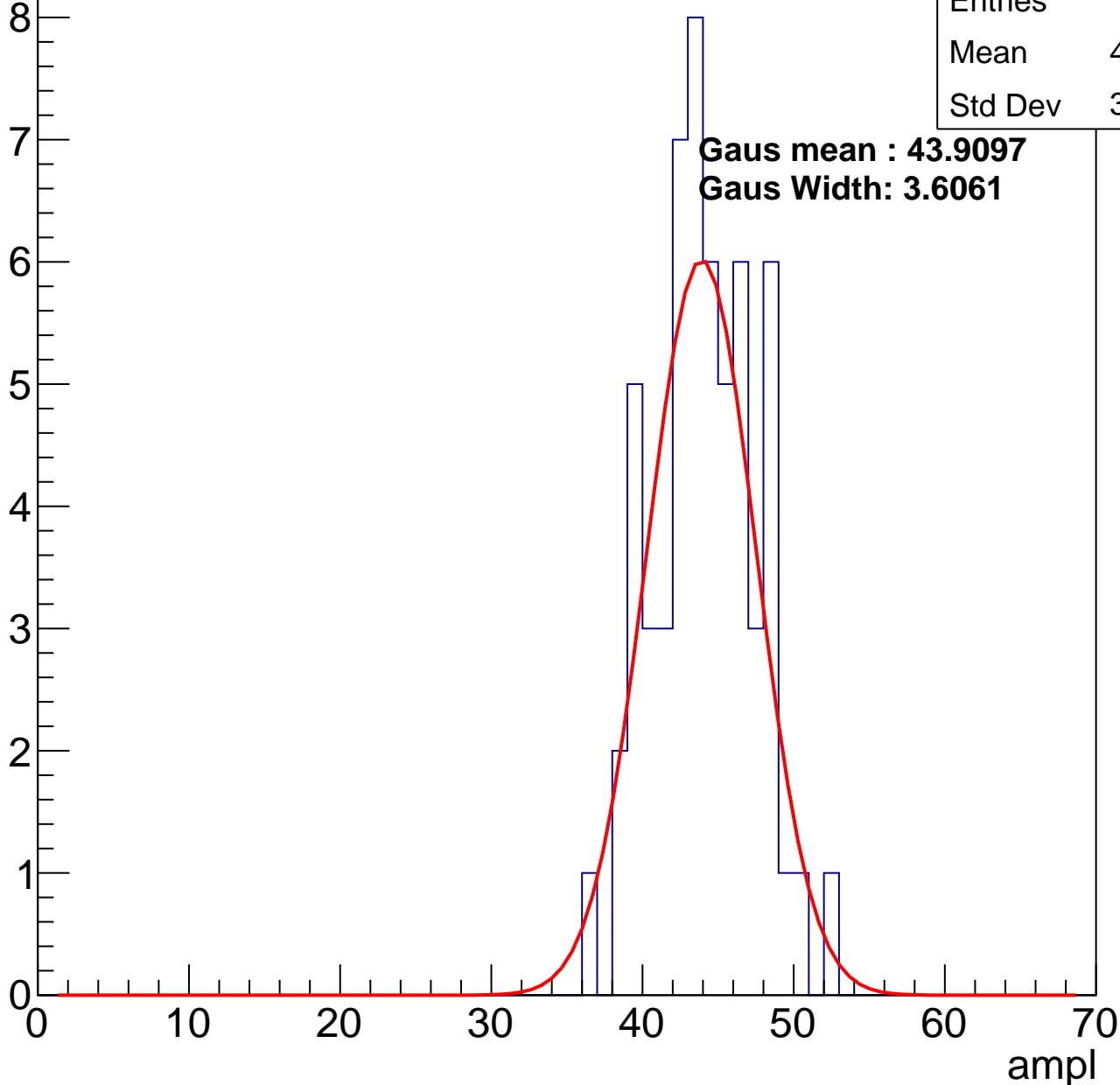
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	58
Mean	43.67
Std Dev	3.329

**Gaus mean : 43.9097**

**Gaus Width: 3.6061**

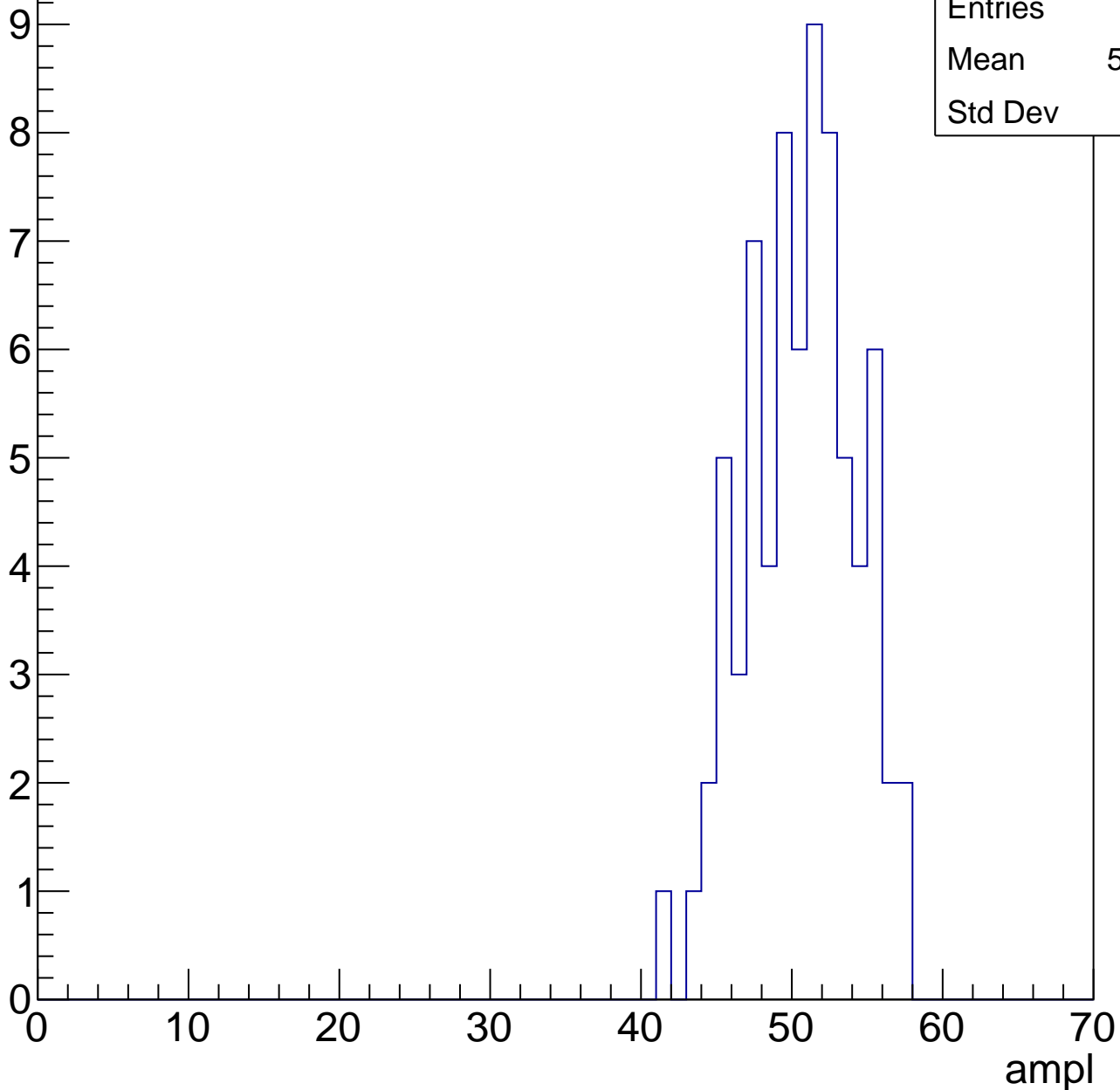


# B1L102S, U12-ch26, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	73
Mean	50.14
Std Dev	3.57

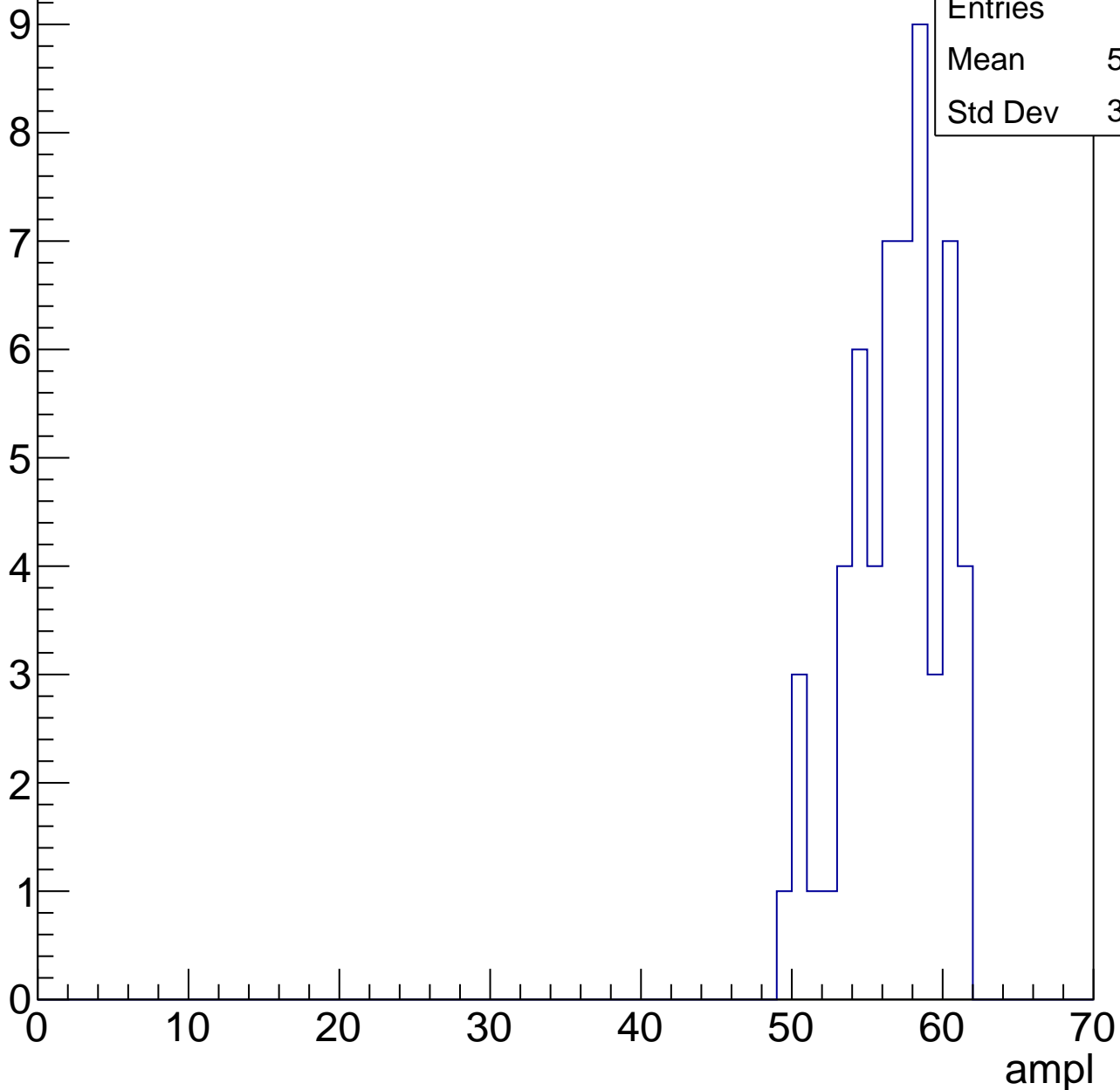


# B1L102S, U12-ch26, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	57
Mean	56.35
Std Dev	3.069

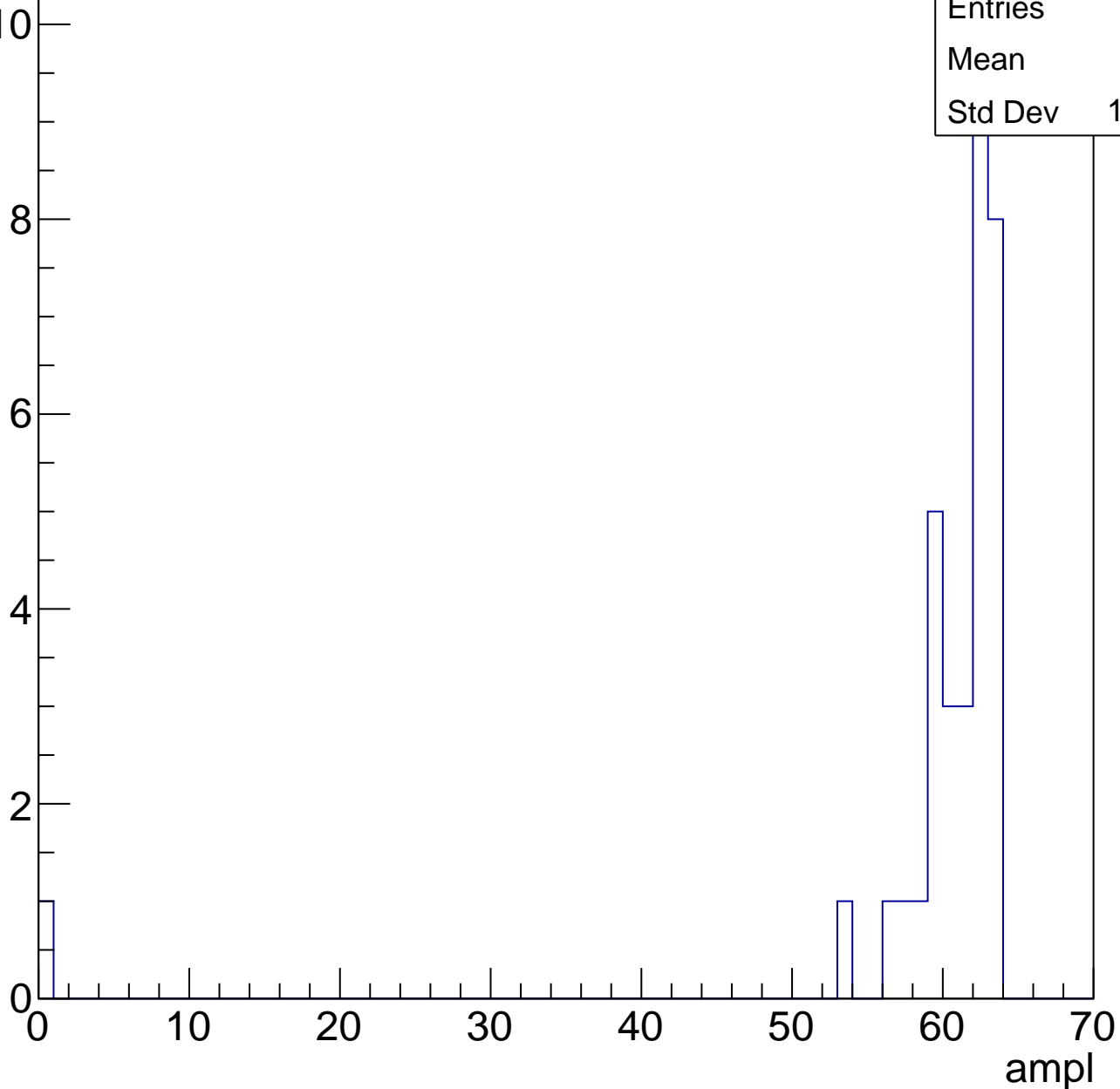


# B1L102S, U12-ch26, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

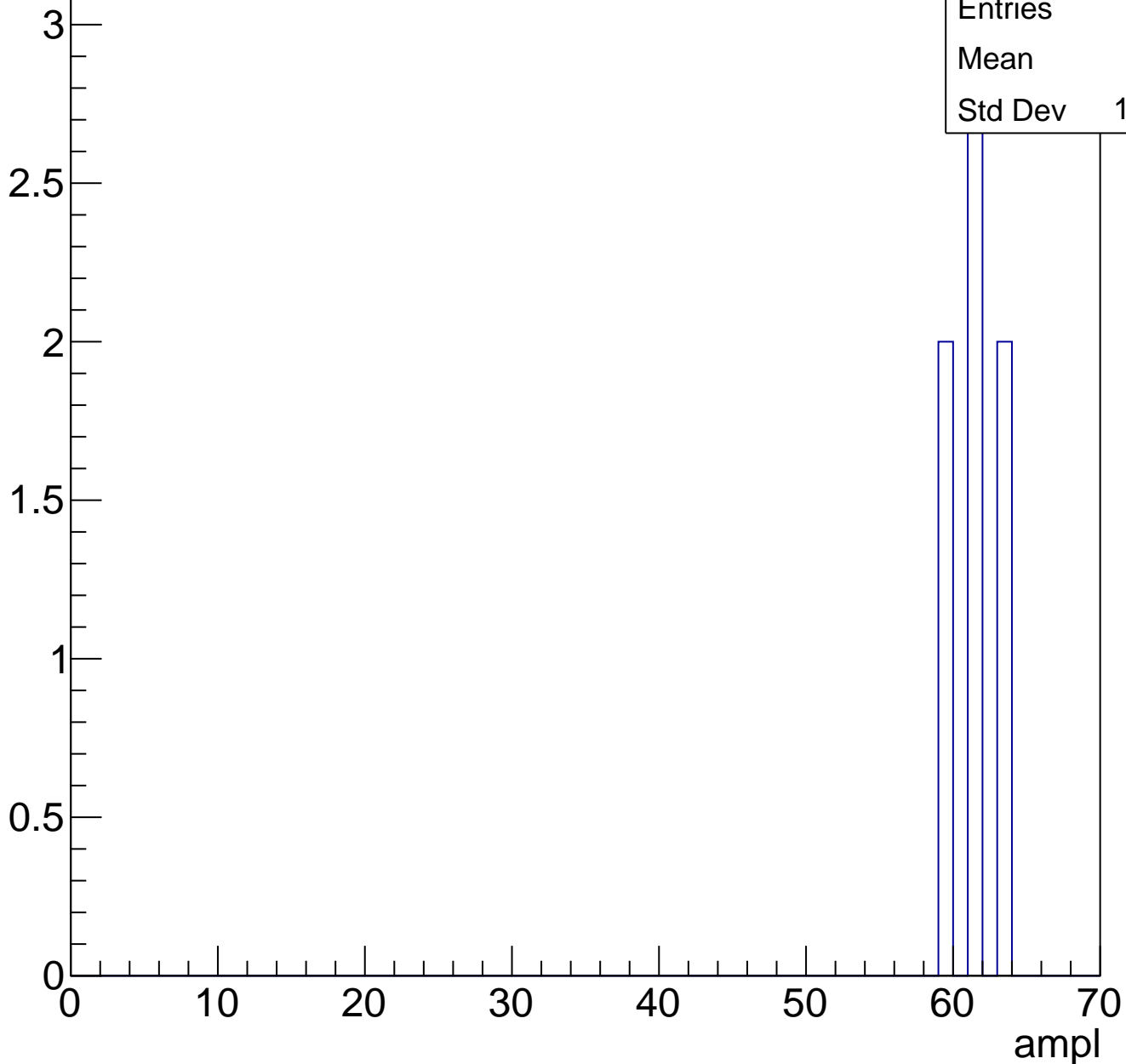
Entries	34
Mean	59
Std Dev	10.52



# B1L102S, U12-ch26, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U12-ch26, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U12-ch27, adc0

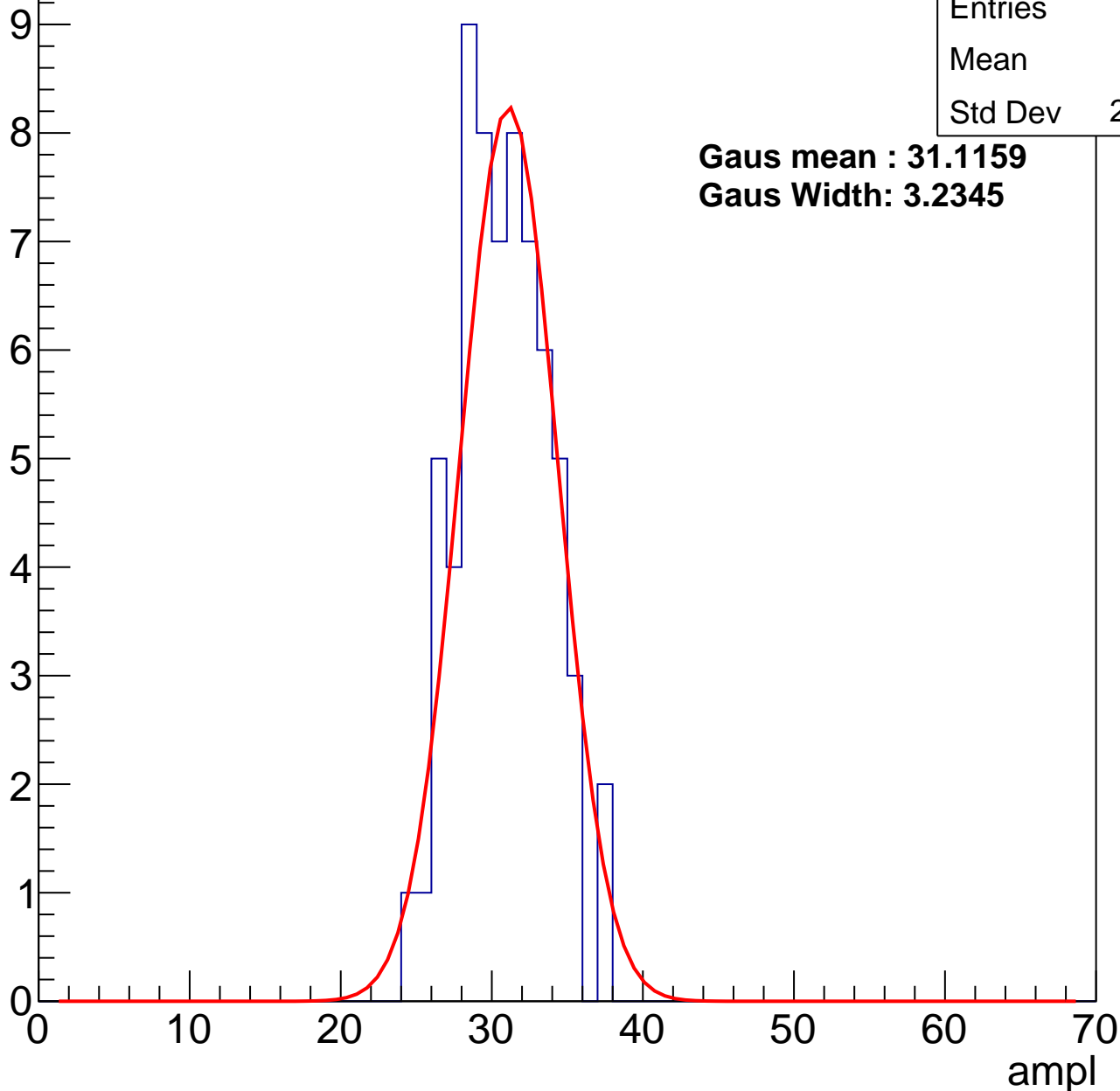
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	30.3
Std Dev	2.908

**Gaus mean : 31.1159**

**Gaus Width: 3.2345**



# B1L102S, U12-ch27, adc1

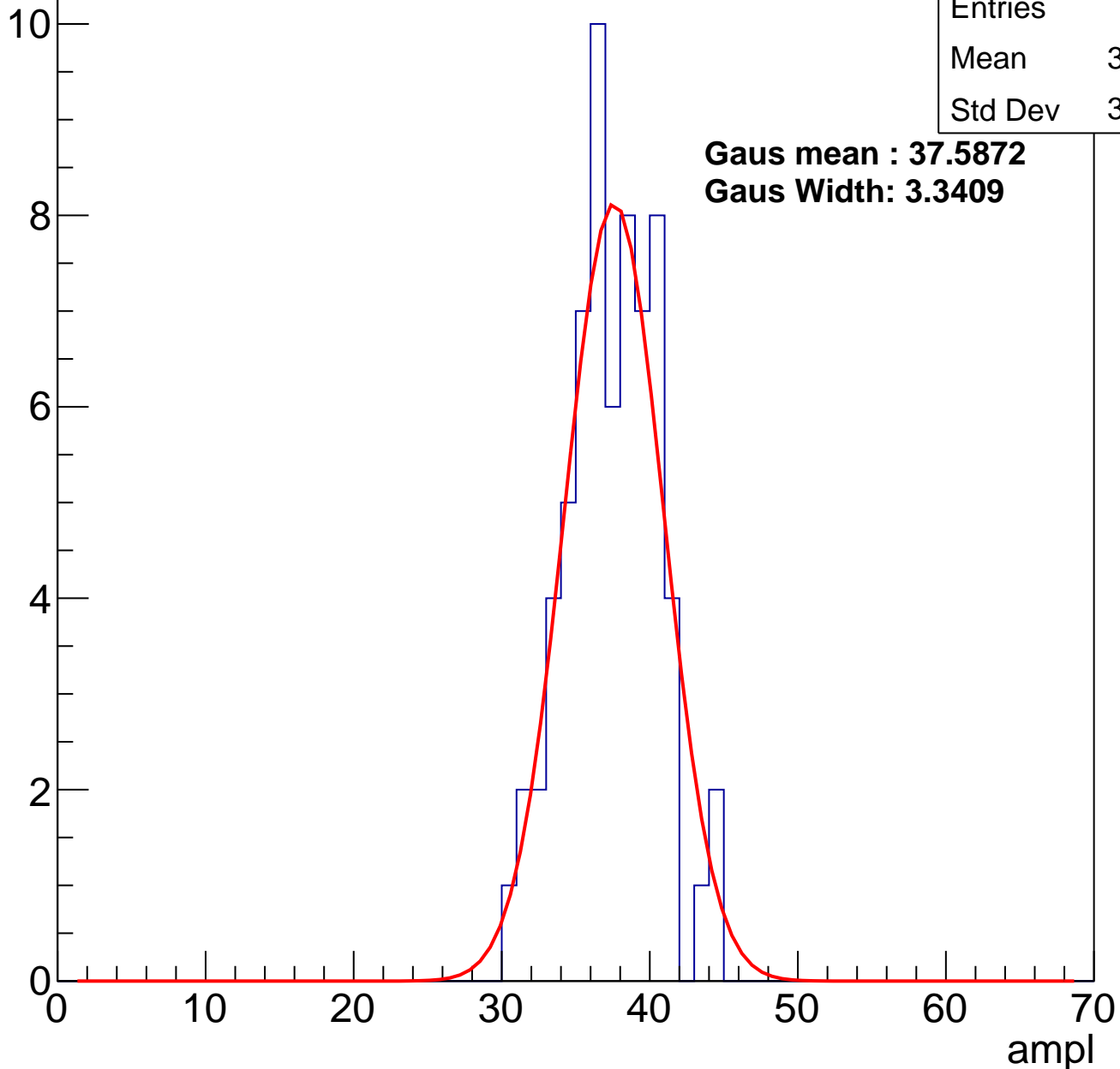
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	67
Mean	36.97
Std Dev	3.052

**Gaus mean : 37.5872**

**Gaus Width: 3.3409**

Entry



# B1L102S, U12-ch27, adc2

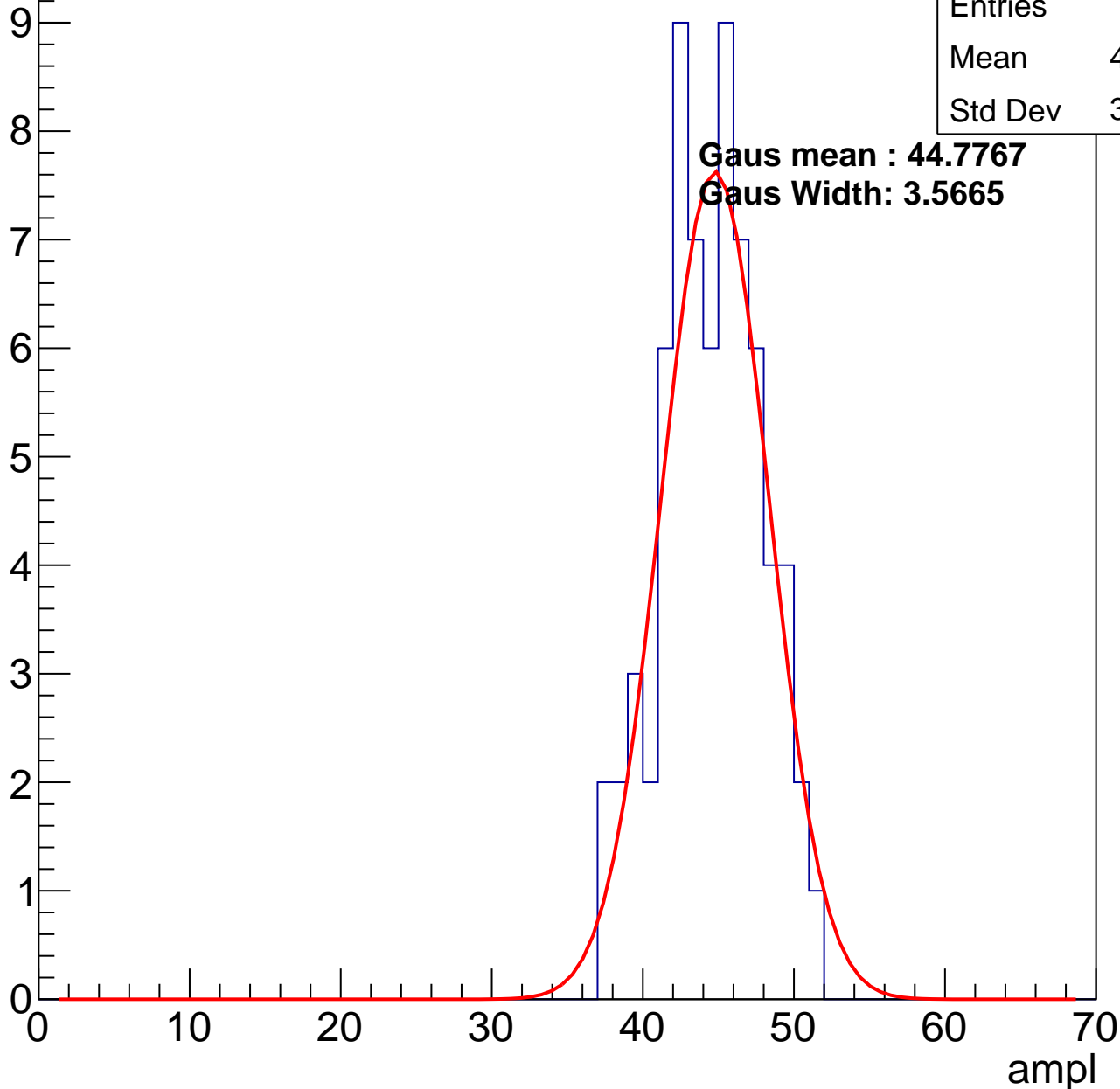
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	70
Mean	44.06
Std Dev	3.273

**Gaus mean : 44.7767**

**Gaus Width: 3.5665**

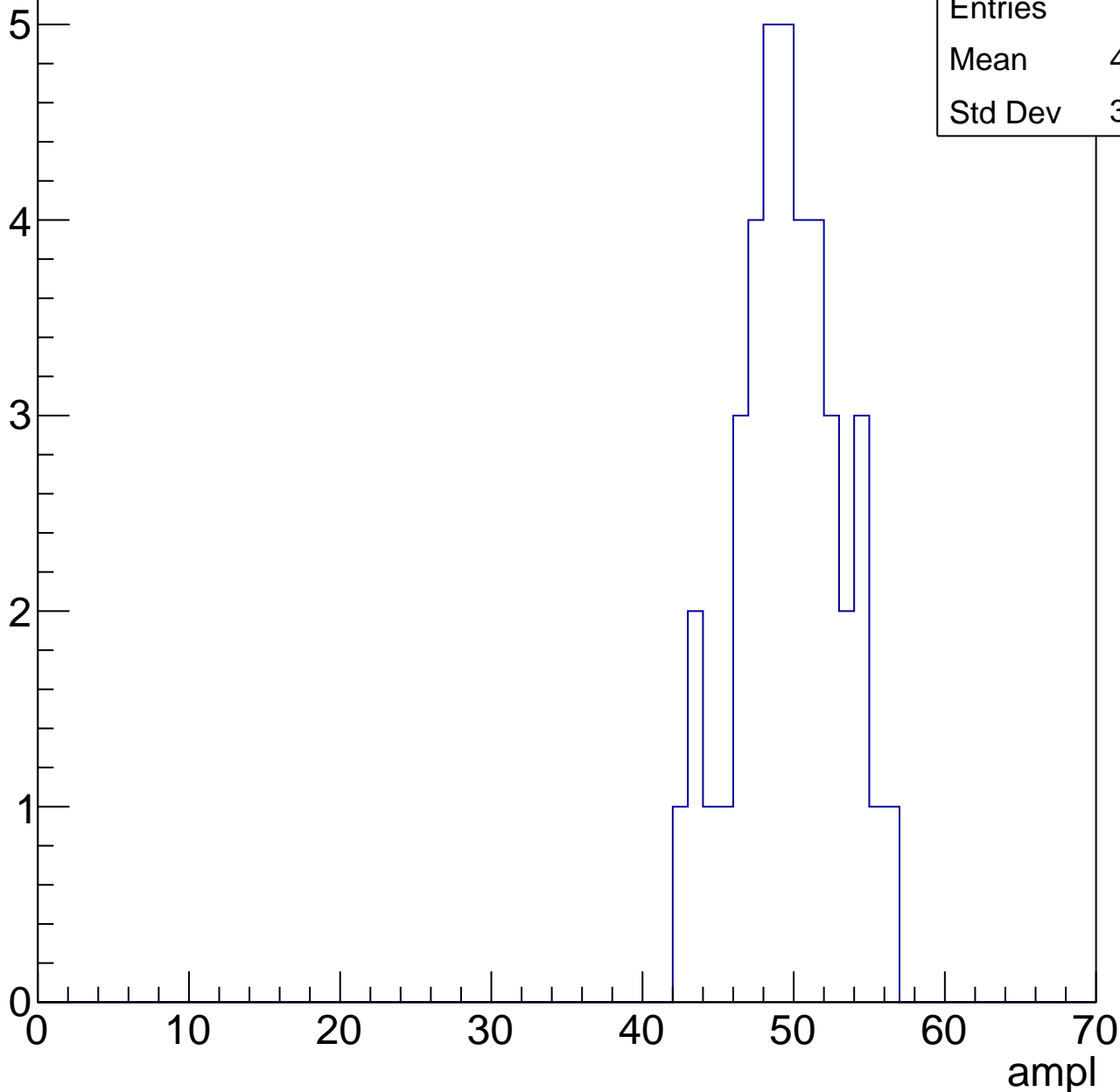


# B1L102S, U12-ch27, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	40
Mean	49.17
Std Dev	3.346

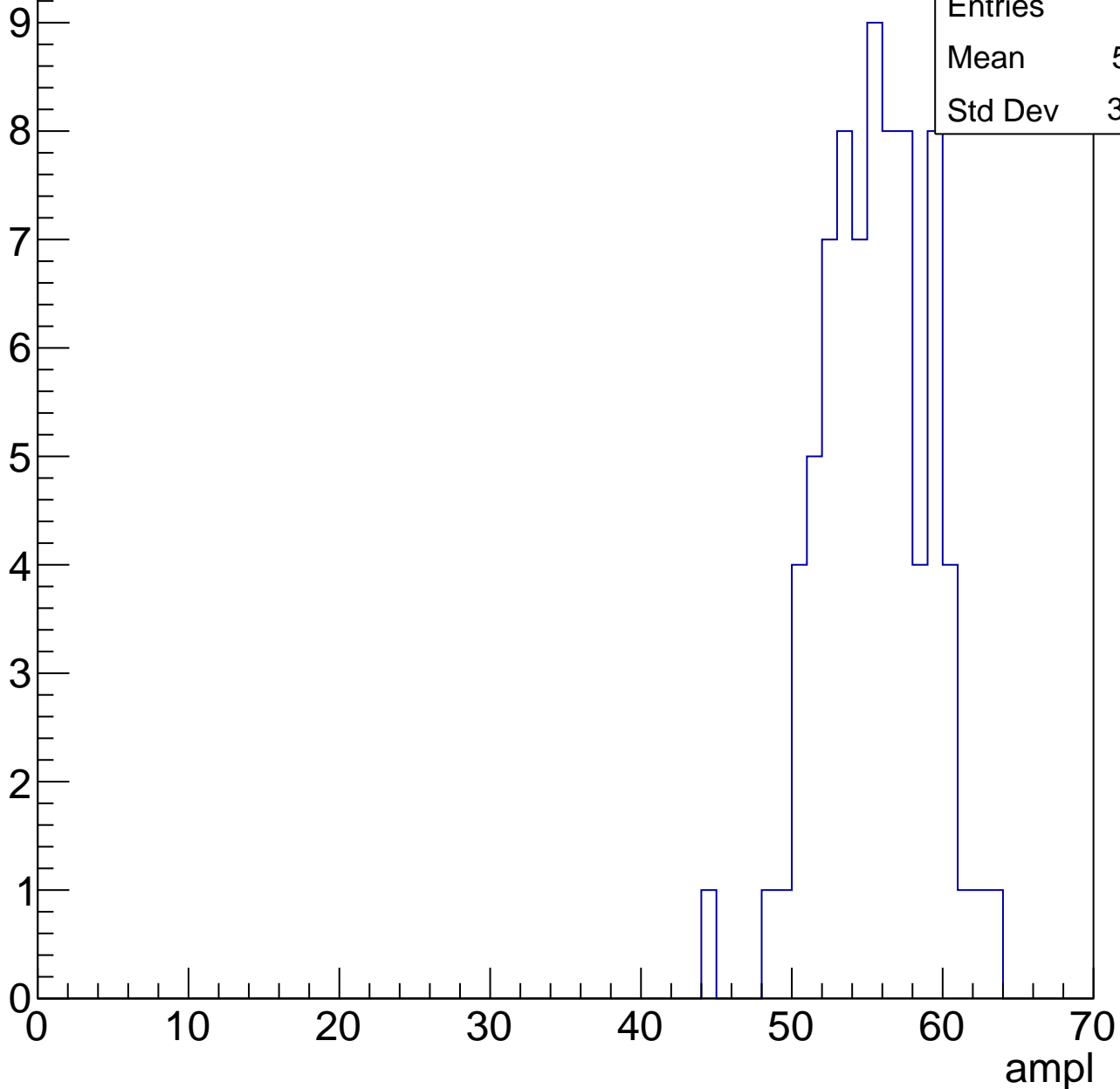


# B1L102S, U12-ch27, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	78
Mean	55.01
Std Dev	3.473

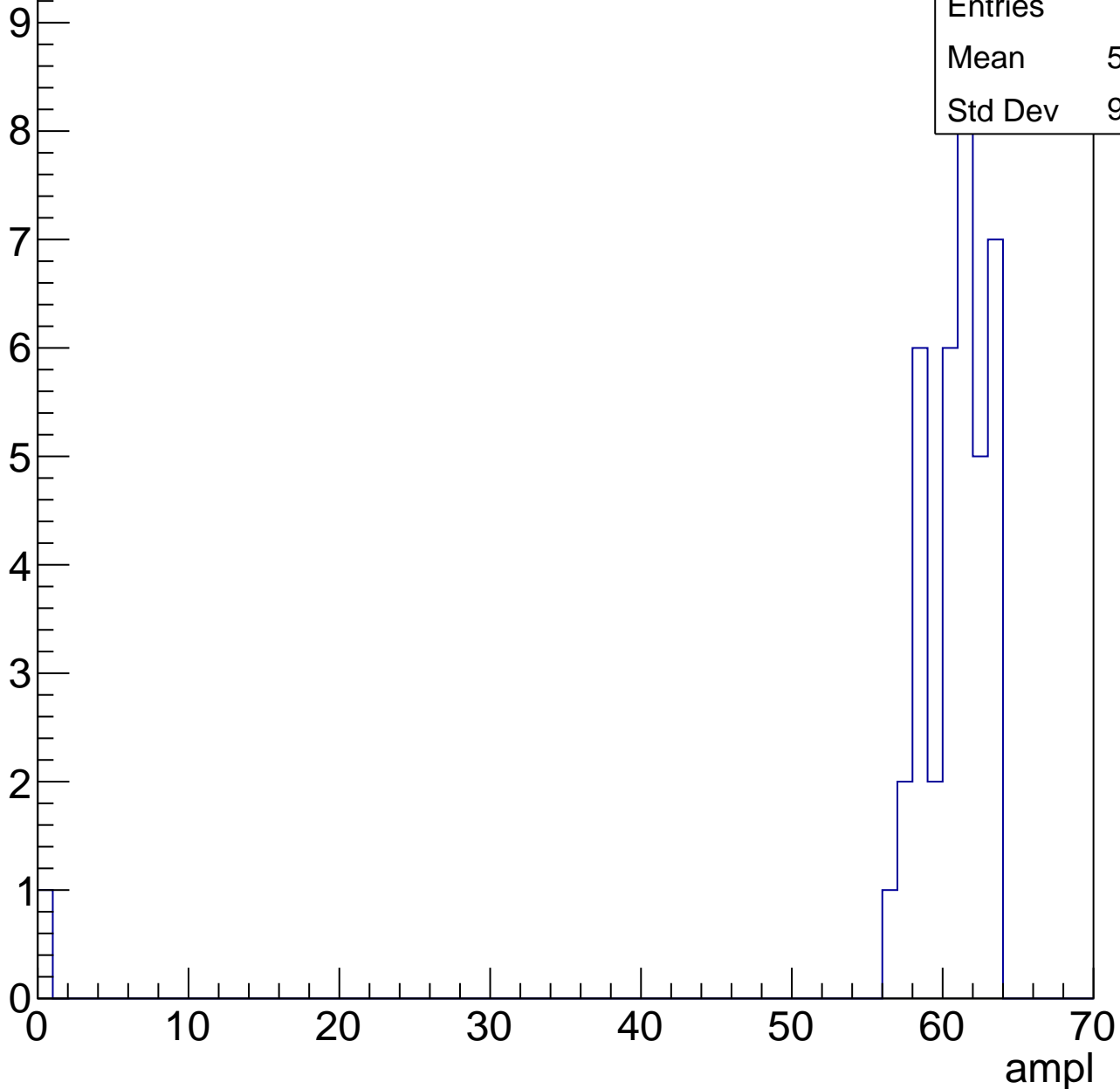


# B1L102S, U12-ch27, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

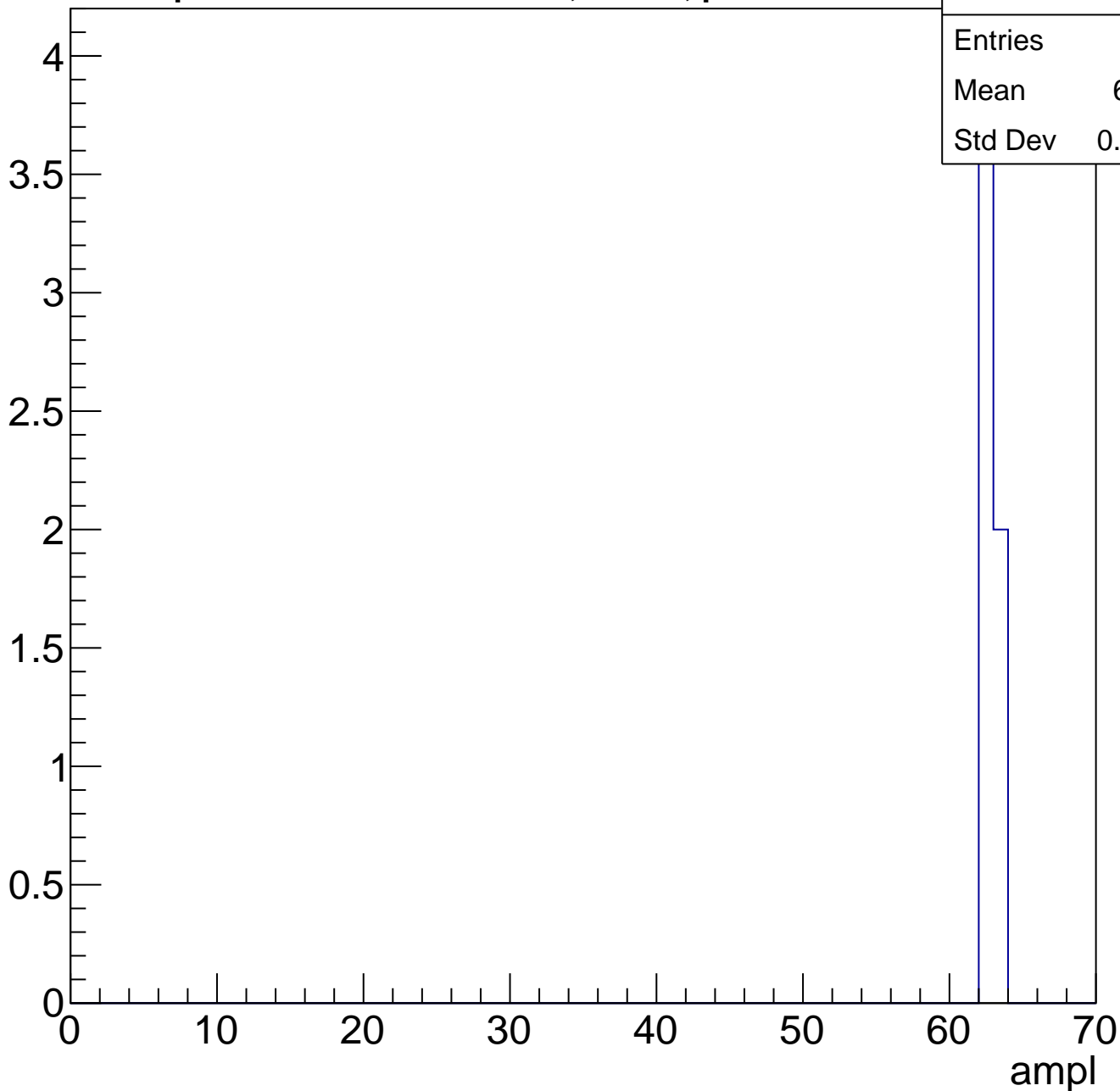
Entries	39
Mean	58.87
Std Dev	9.743



# B1L102S, U12-ch27, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

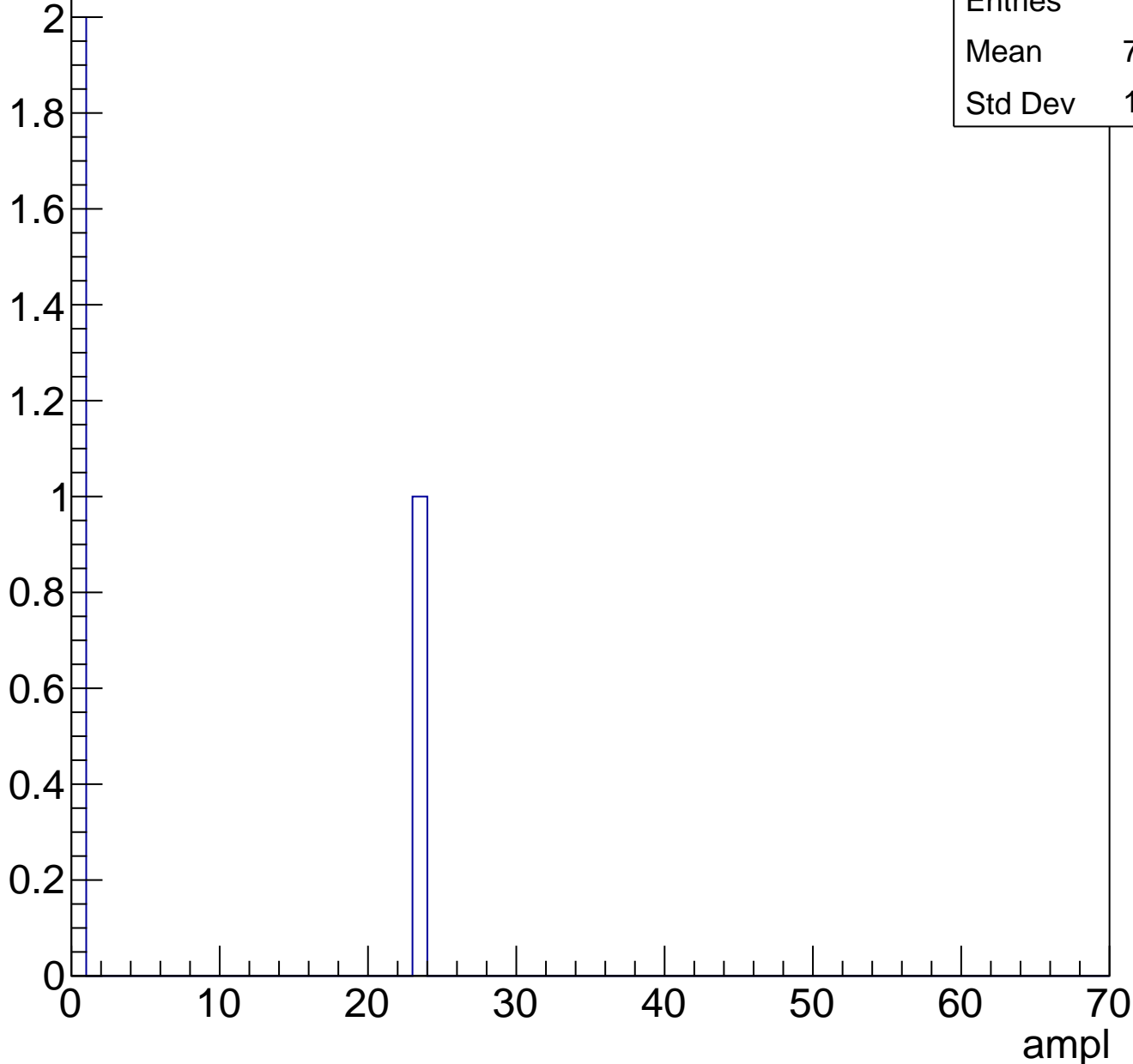




# B1L102S, U12-ch27, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	3
Mean	7.667
Std Dev	10.84

# B1L102S, U12-ch28, adc0

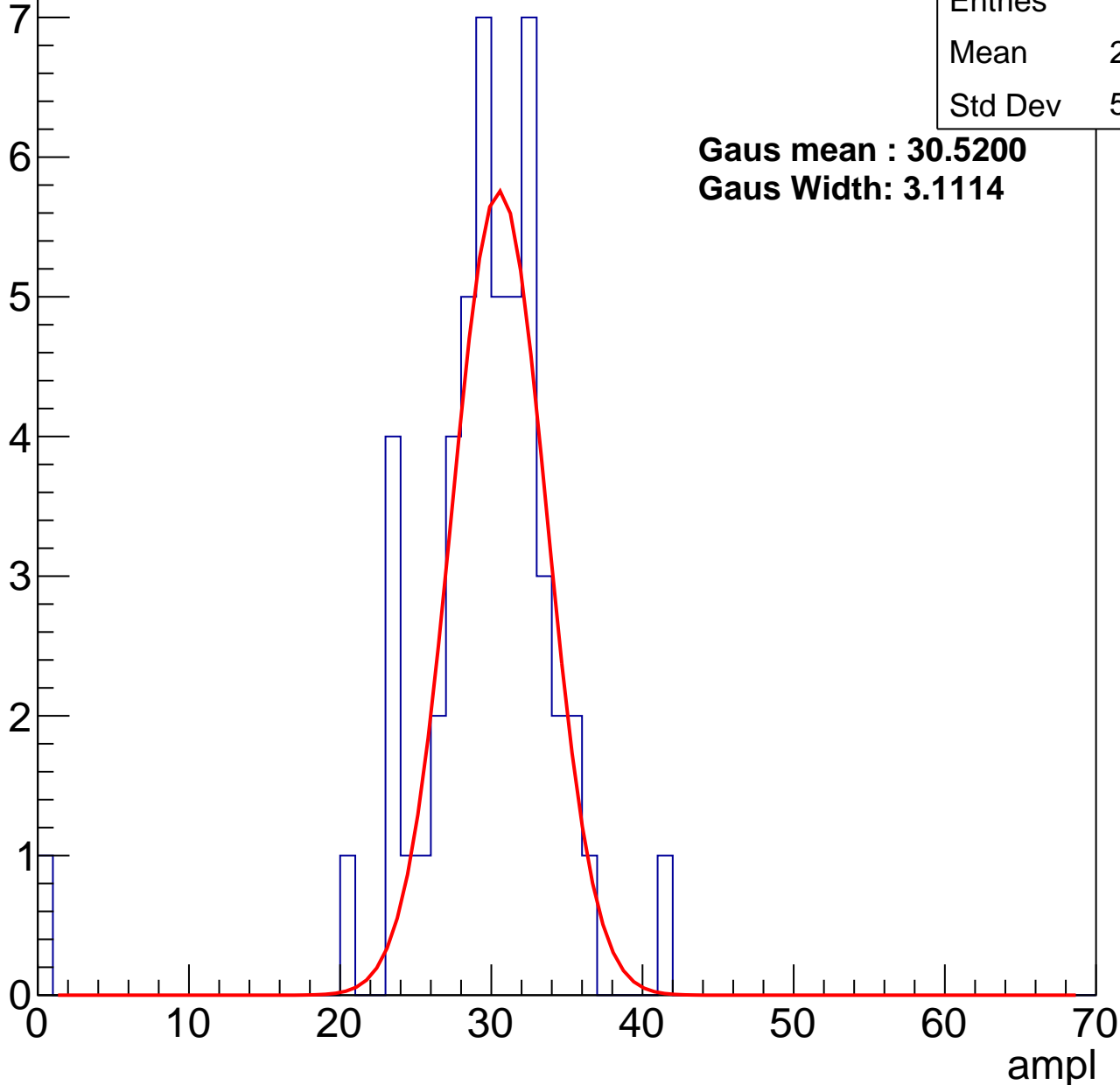
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	52
Mean	28.98
Std Dev	5.542

**Gaus mean : 30.5200**

**Gaus Width: 3.1114**

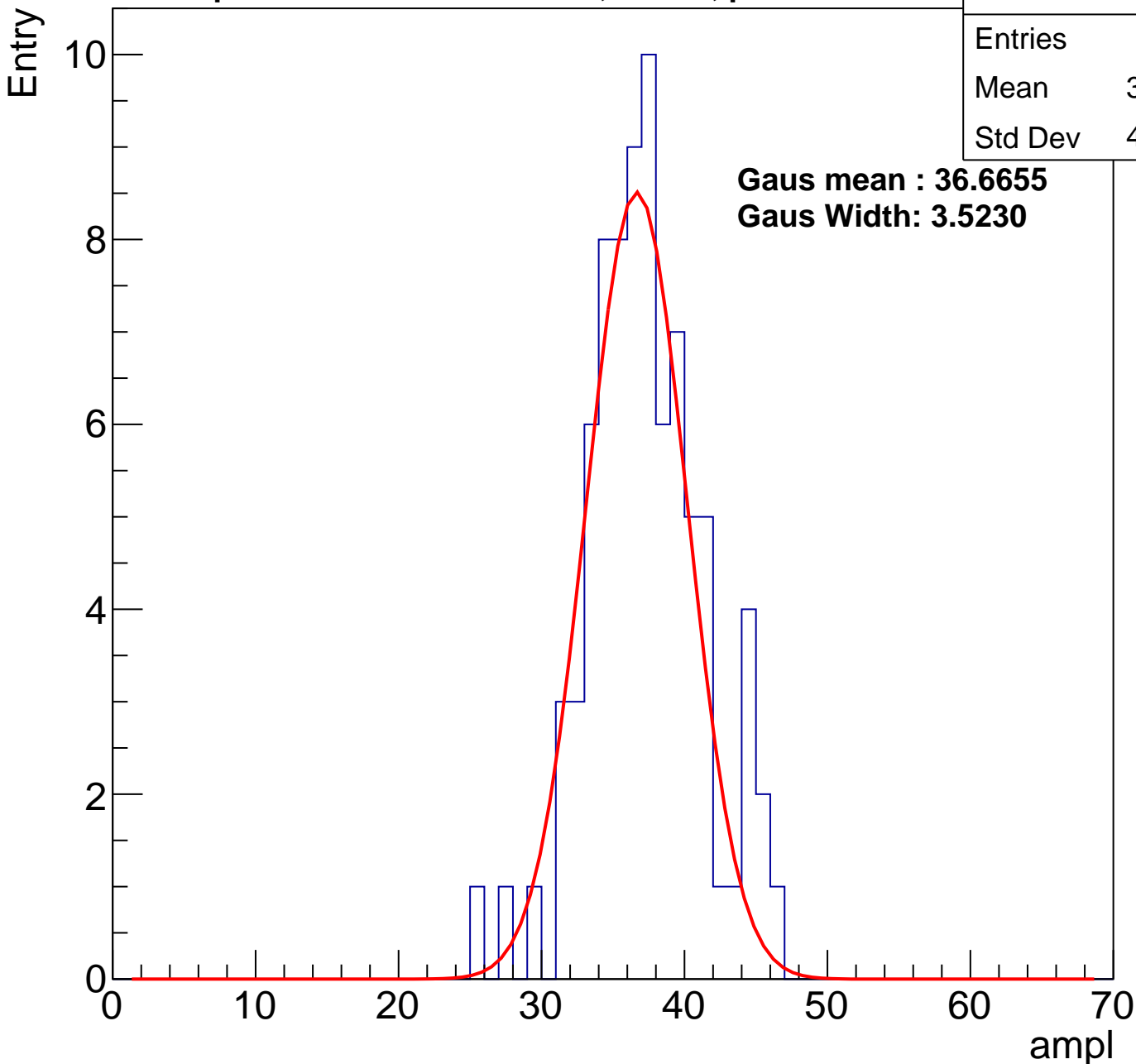


# B1L102S, U12-ch28, adc1

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	82
Mean	36.79
Std Dev	4.014

**Gaus mean : 36.6655**  
**Gaus Width: 3.5230**



# B1L102S, U12-ch28, adc2

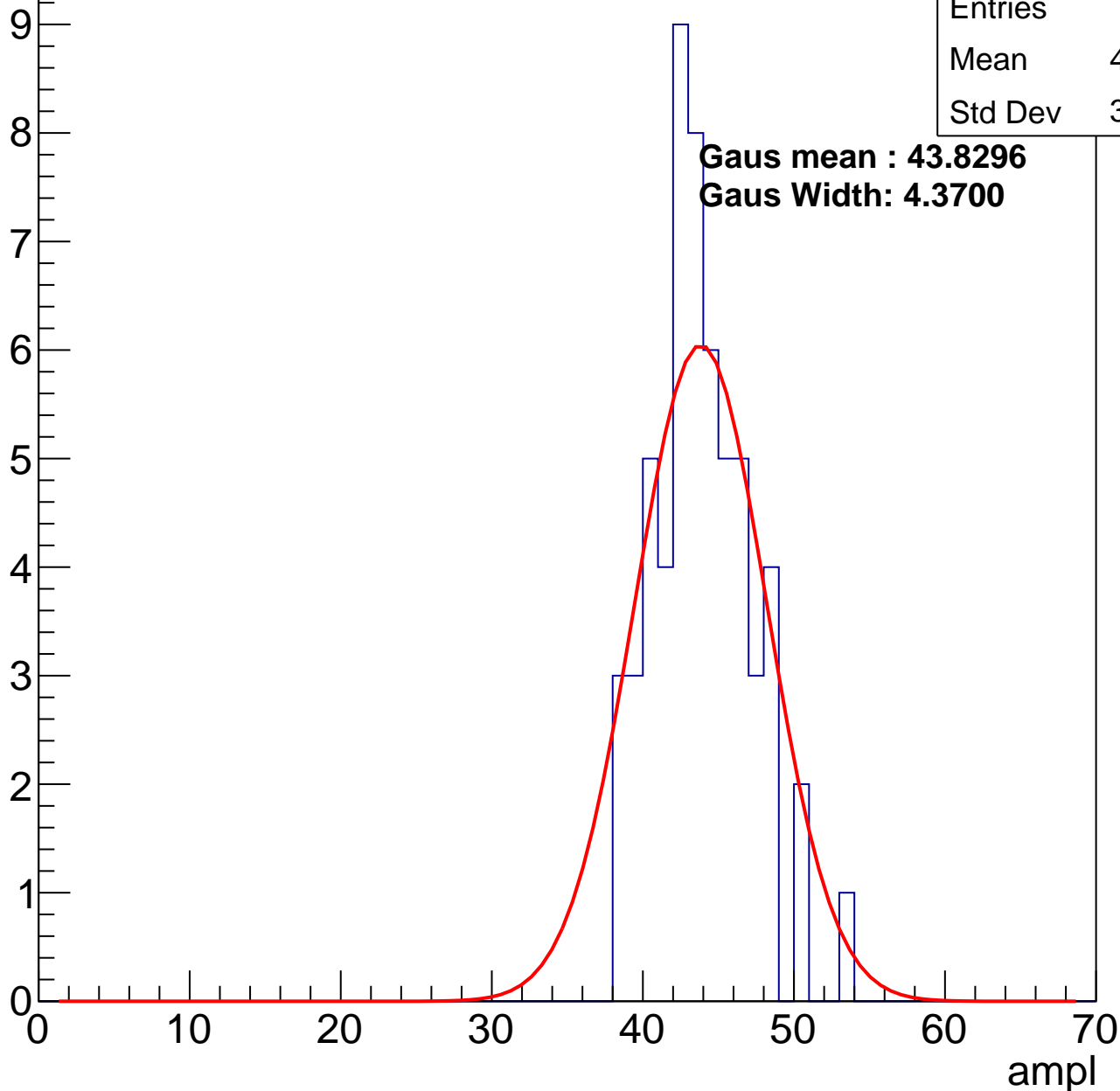
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	58
Mean	43.48
Std Dev	3.207

**Gaus mean : 43.8296**

**Gaus Width: 4.3700**

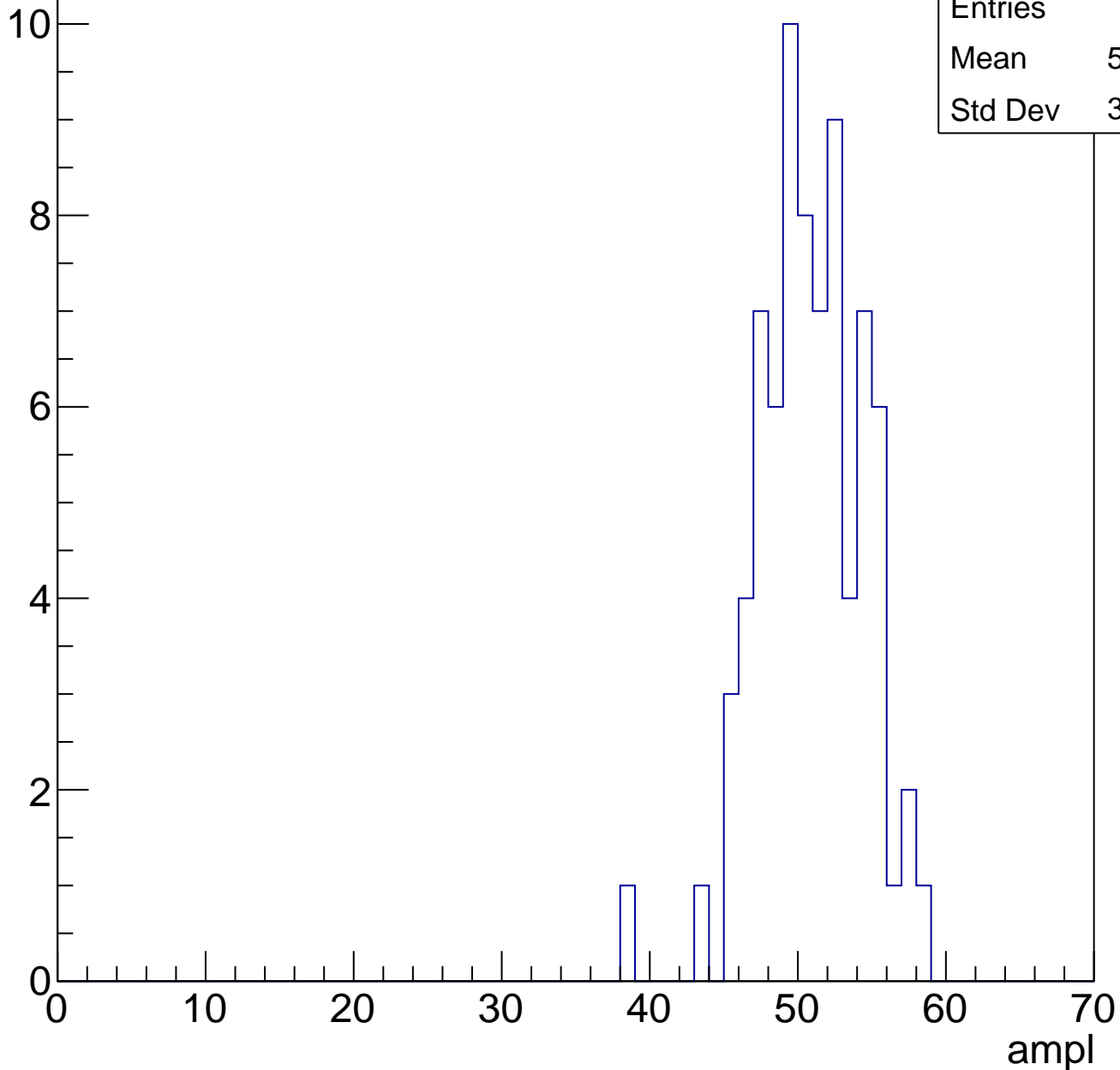


# B1L102S, U12-ch28, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	77
Mean	50.39
Std Dev	3.524

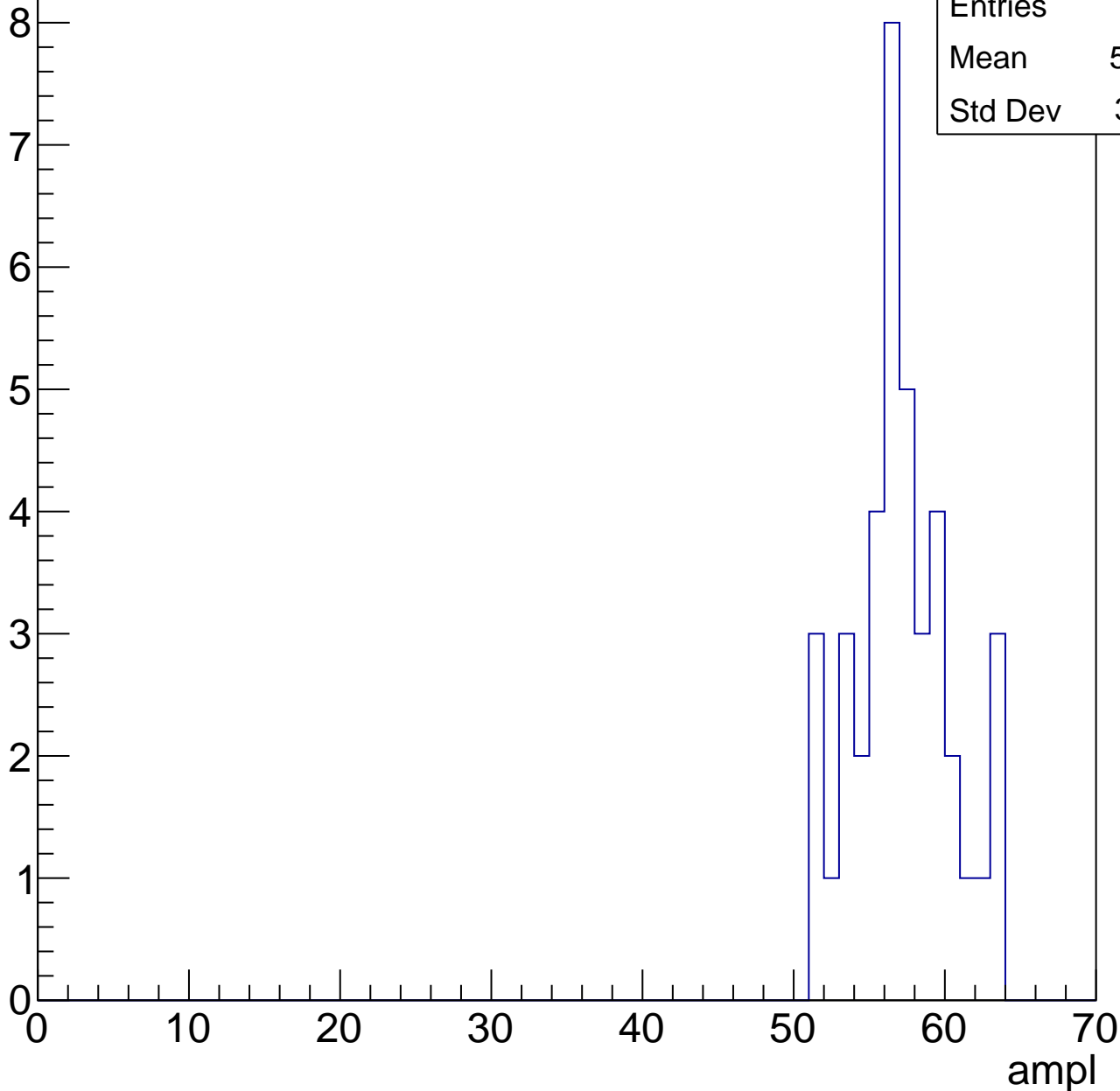


# B1L102S, U12-ch28, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	40
Mean	56.67
Std Dev	3.181

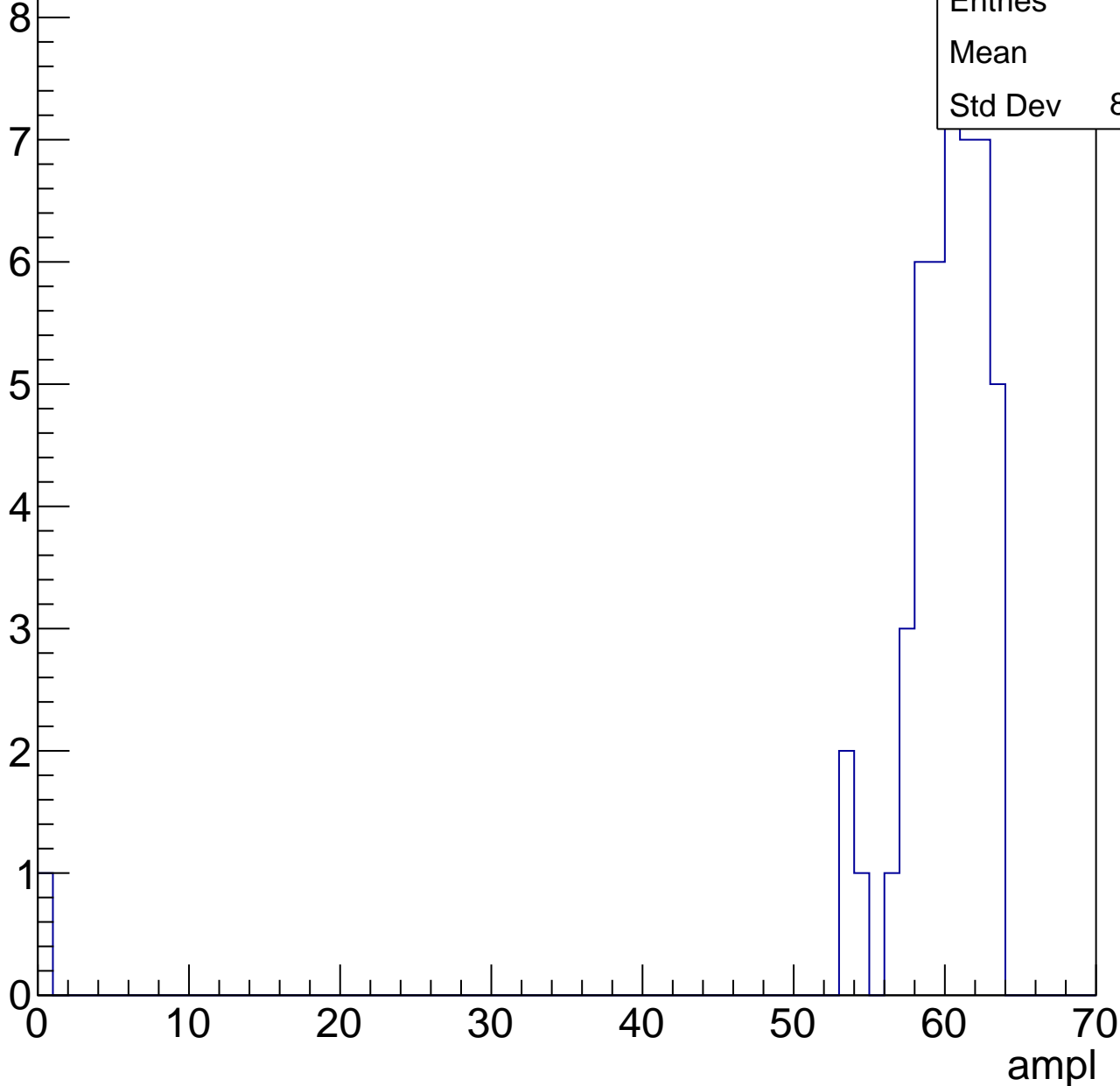


# B1L102S, U12-ch28, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	47
Mean	58.4
Std Dev	8.953



# B1L102S, U12-ch28, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

0 10 20 30 40 50 60 70

ampl

Entries	6
Mean	62
Std Dev	0.8165



# B1L102S, U12-ch28, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U12-ch29, adc0

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	90
Mean	31.21
Std Dev	3.692

**Gaus mean : 31.4834**

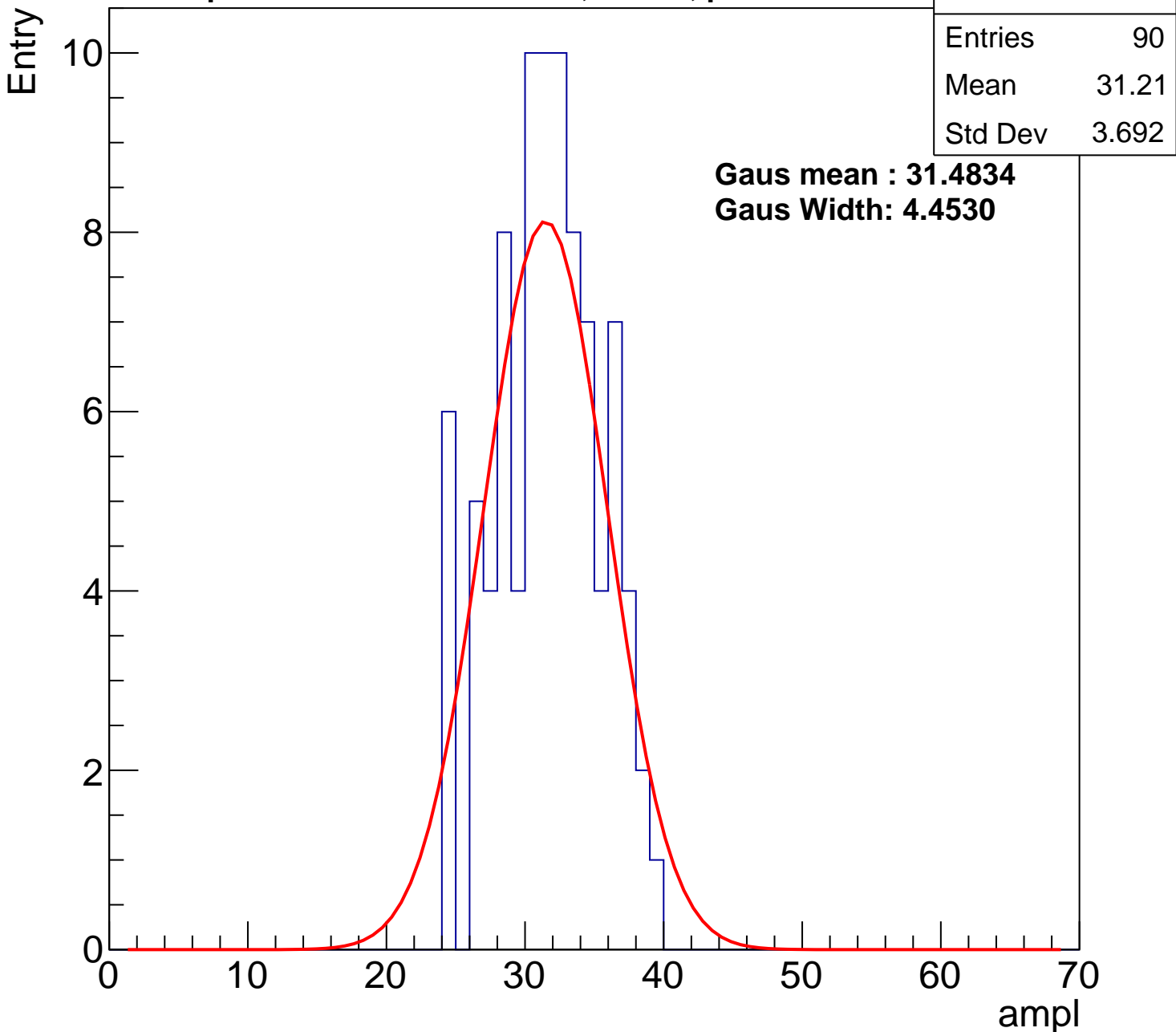
**Gaus Width: 4.4530**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L102S, U12-ch29, adc1

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	64
Mean	38.94
Std Dev	3.071

**Gaus mean : 38.9440**

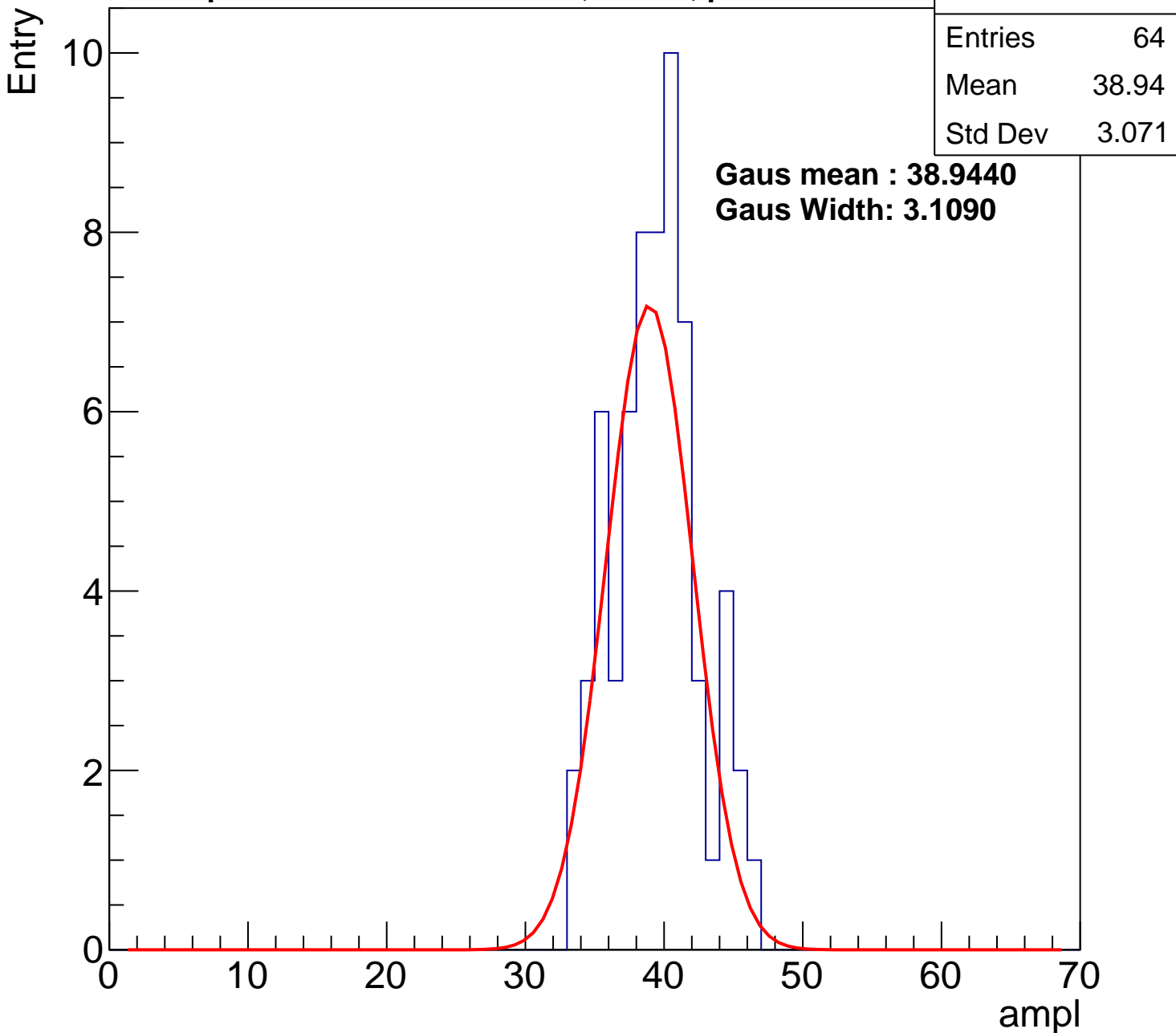
**Gaus Width: 3.1090**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L102S, U12-ch29, adc2

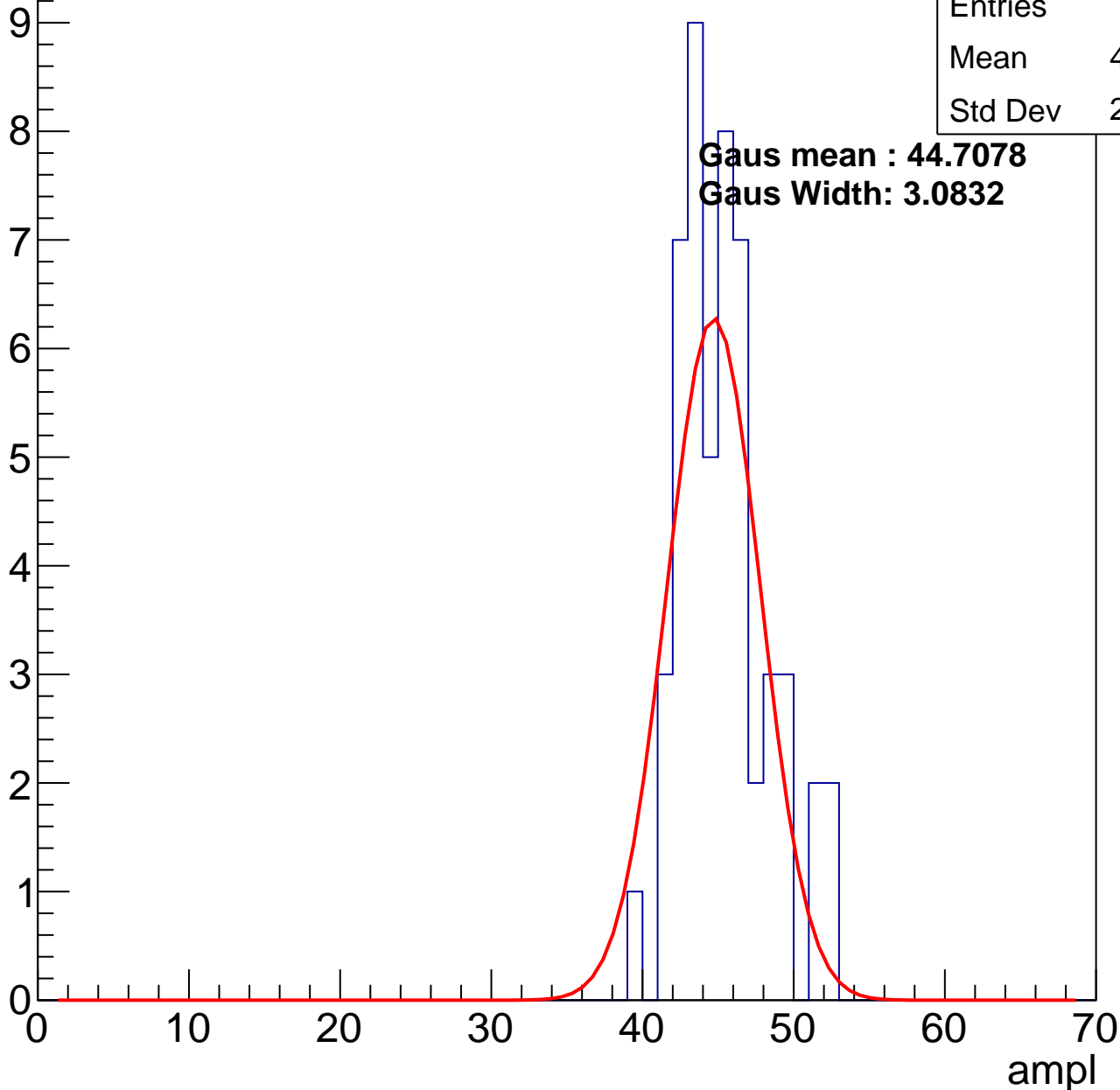
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	52
Mean	44.92
Std Dev	2.934

**Gaus mean : 44.7078**

**Gaus Width: 3.0832**

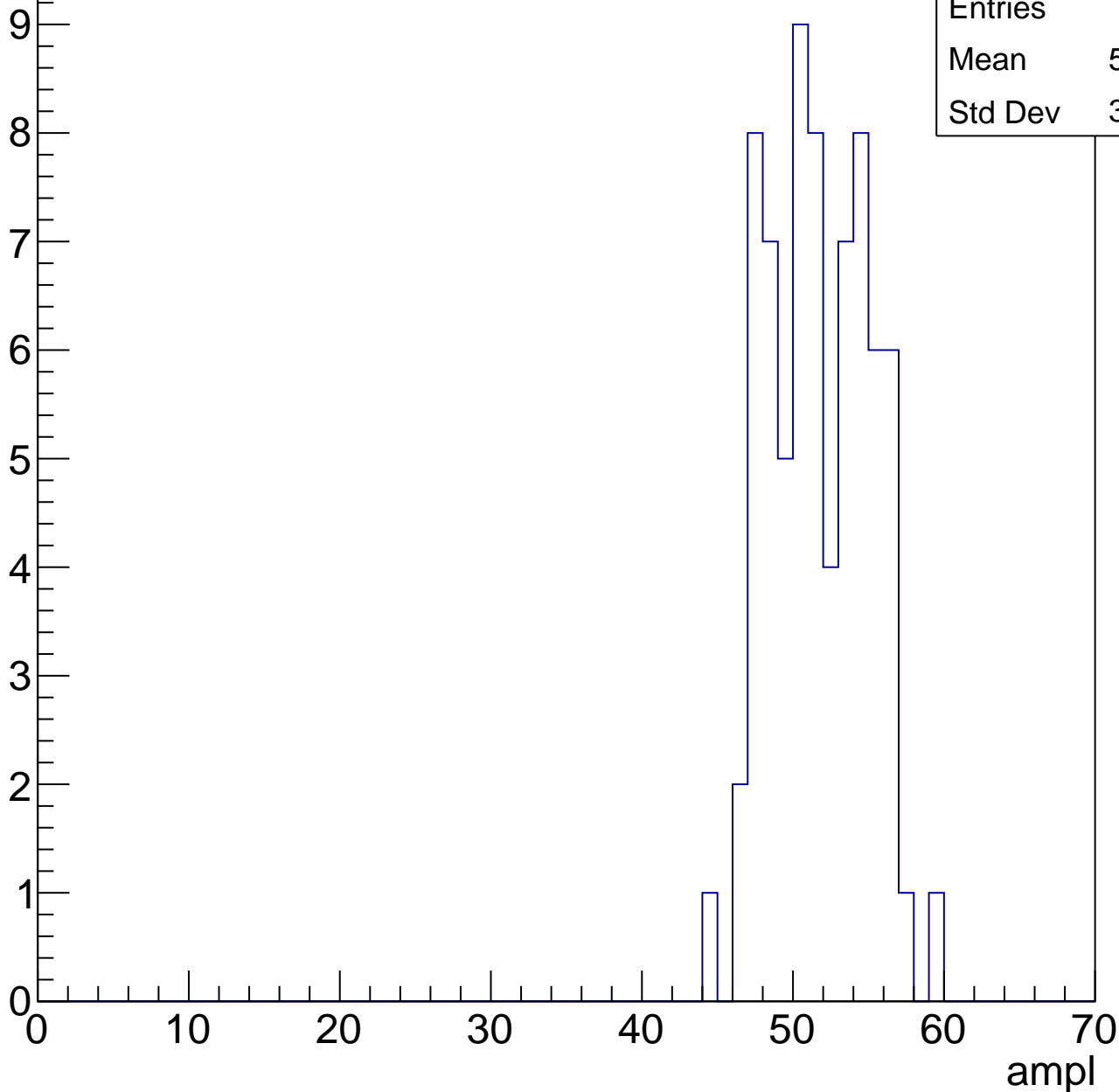


# B1L102S, U12-ch29, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	73
Mean	51.29
Std Dev	3.233

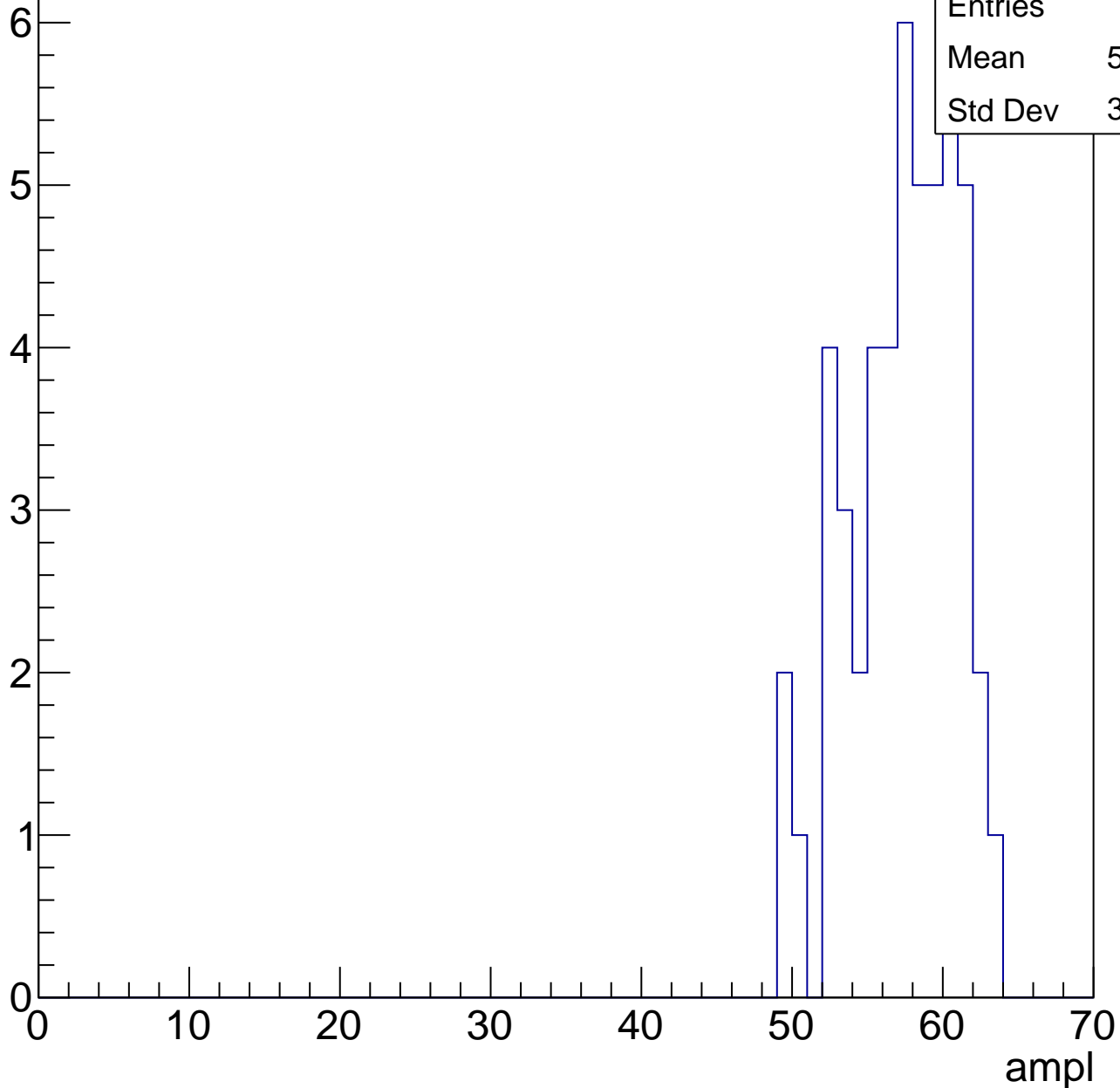


# B1L102S, U12-ch29, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	50
Mean	56.92
Std Dev	3.486

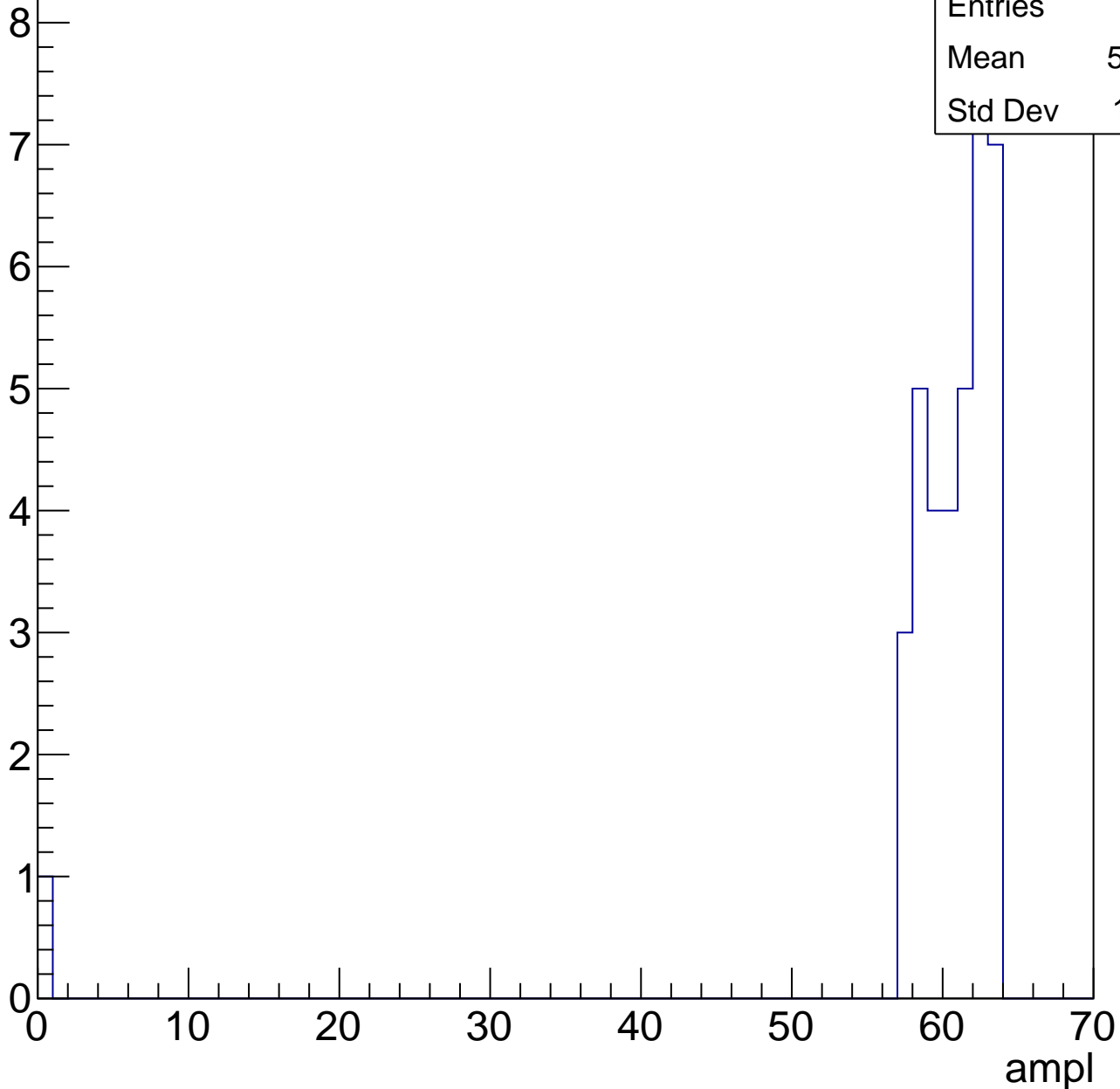


# B1L102S, U12-ch29, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	37
Mean	58.89
Std Dev	10.01



# B1L102S, U12-ch29, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	2
Mean	63
Std Dev	0



# B1L102S, U12-ch29, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U12-ch30, adc0

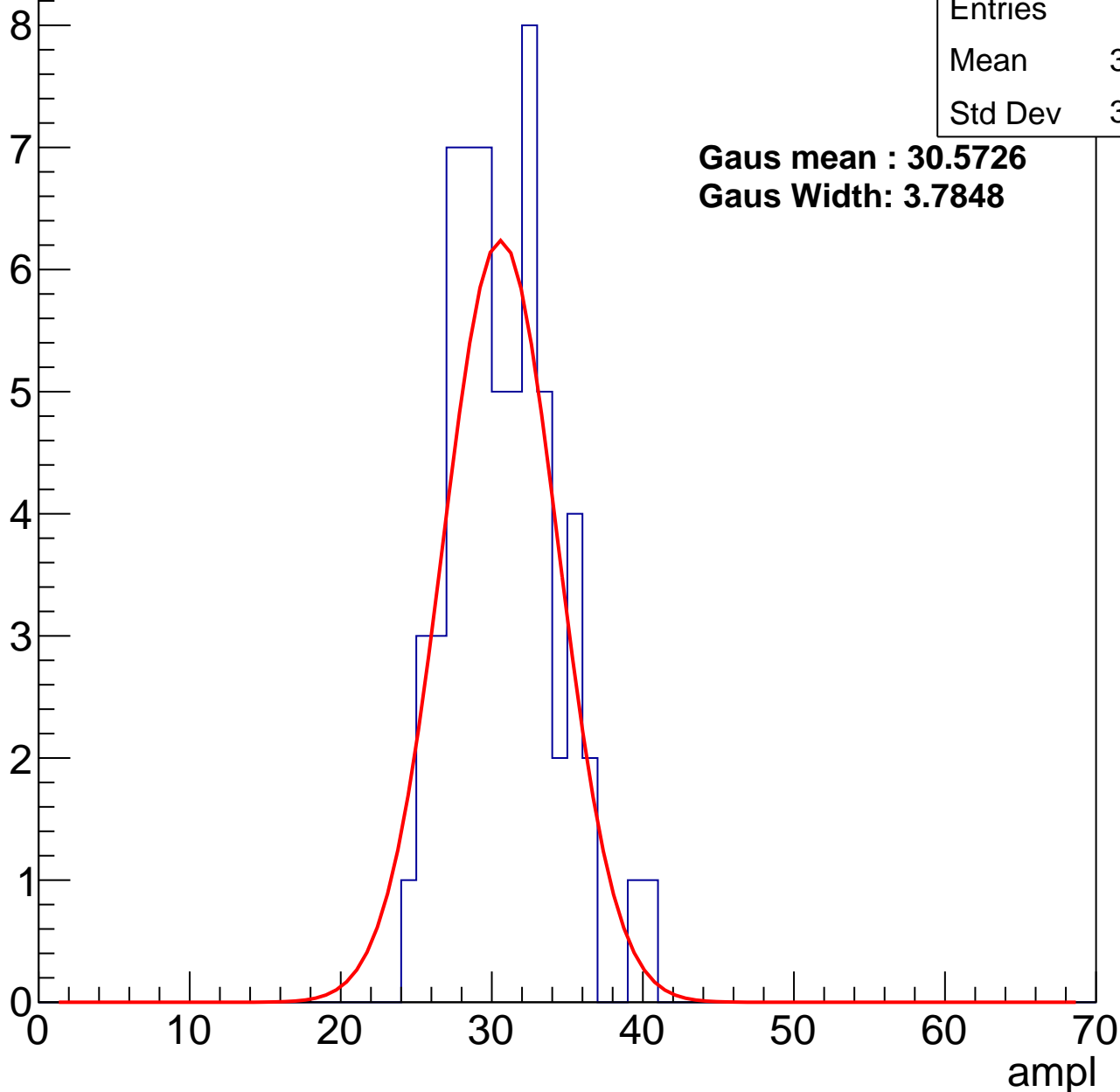
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	30.33
Std Dev	3.429

**Gaus mean : 30.5726**

**Gaus Width: 3.7848**



# B1L102S, U12-ch30, adc1

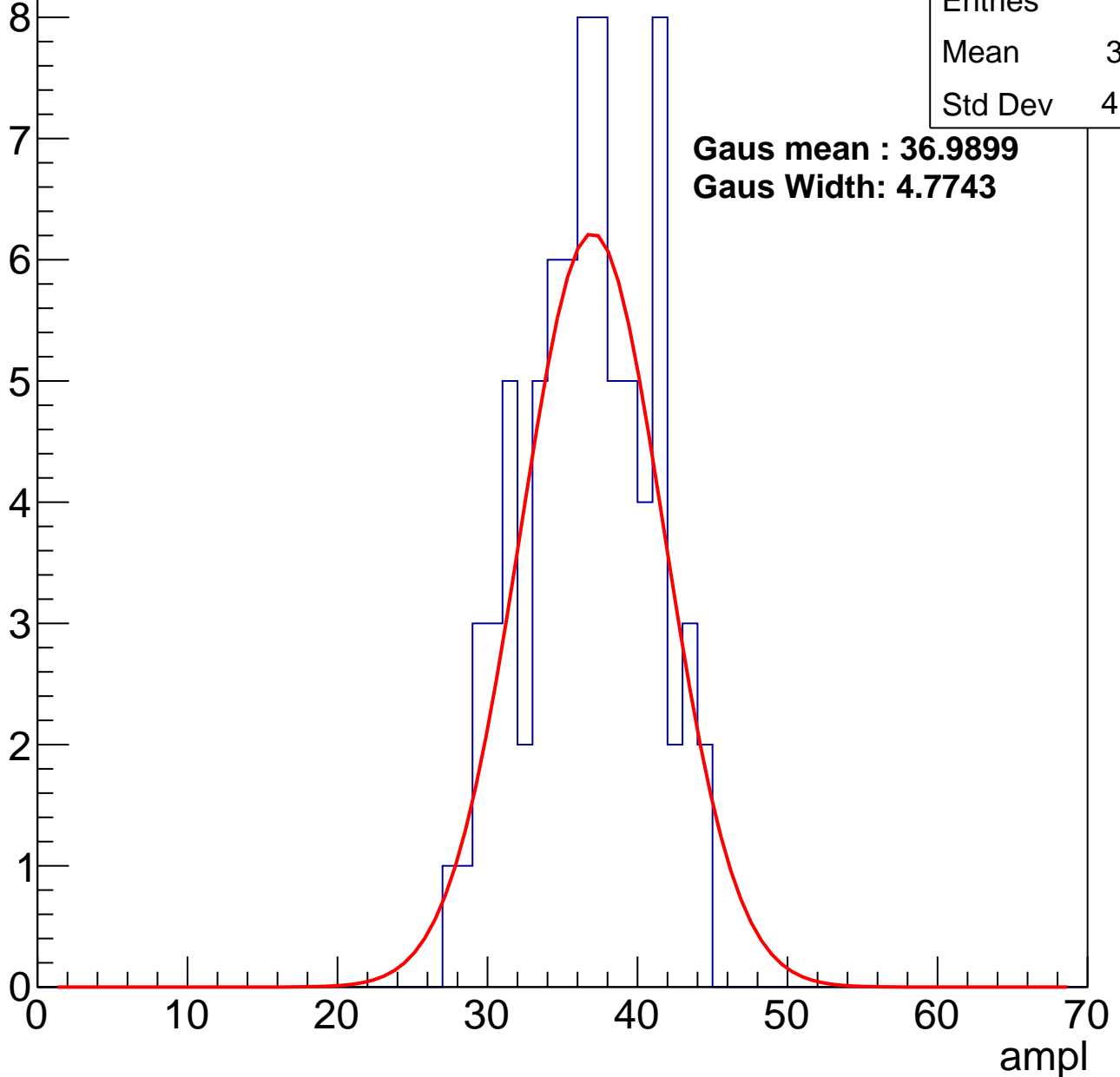
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	77
Mean	36.21
Std Dev	4.129

**Gaus mean : 36.9899**

**Gaus Width: 4.7743**



# B1L102S, U12-ch30, adc2

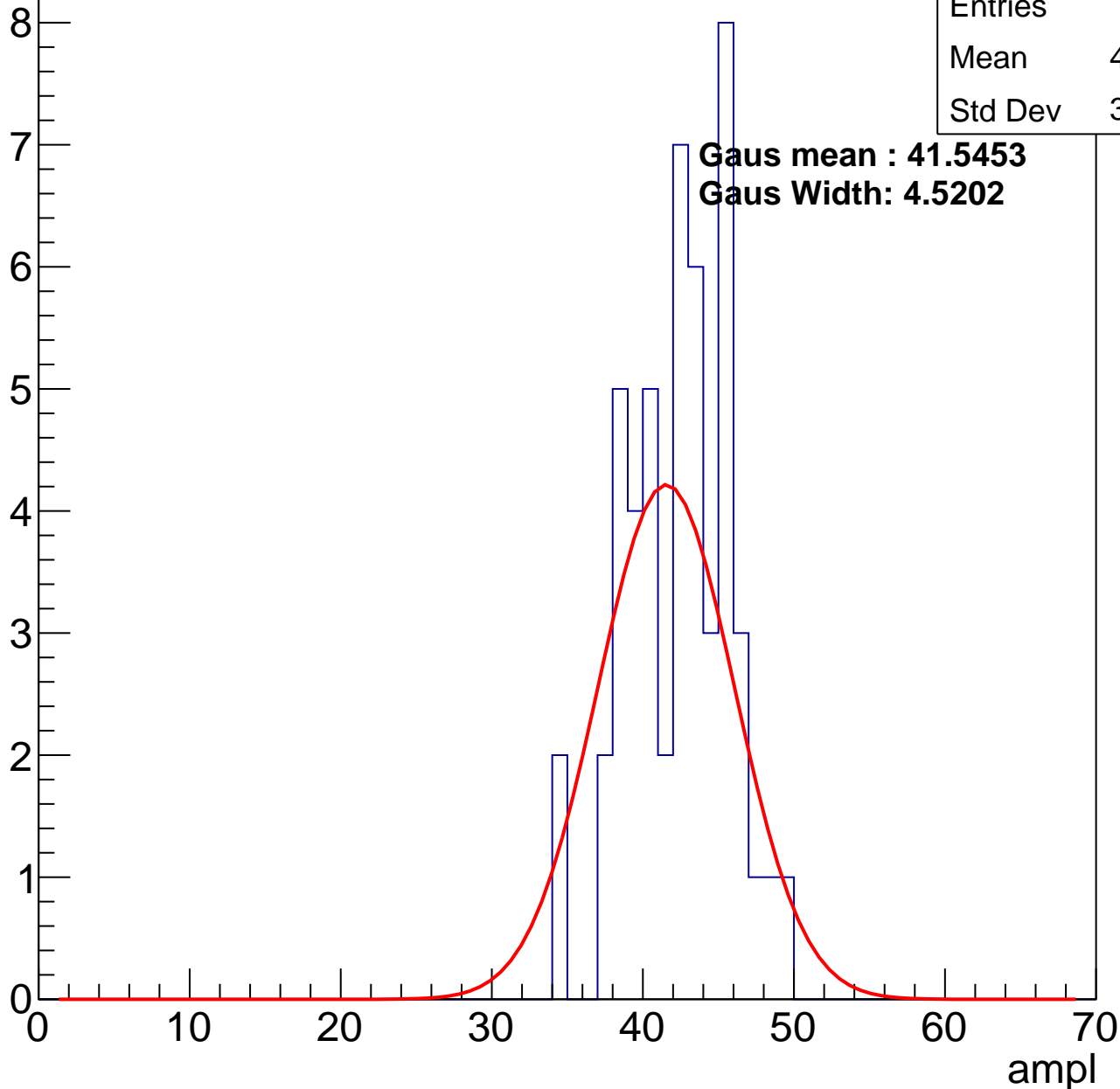
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	50
Mean	41.92
Std Dev	3.358

**Gaus mean : 41.5453**

**Gaus Width: 4.5202**



# B1L102S, U12-ch30, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	83
Mean	49.43
Std Dev	3.246

Entry

10

8

6

4

2

0

0

10

20

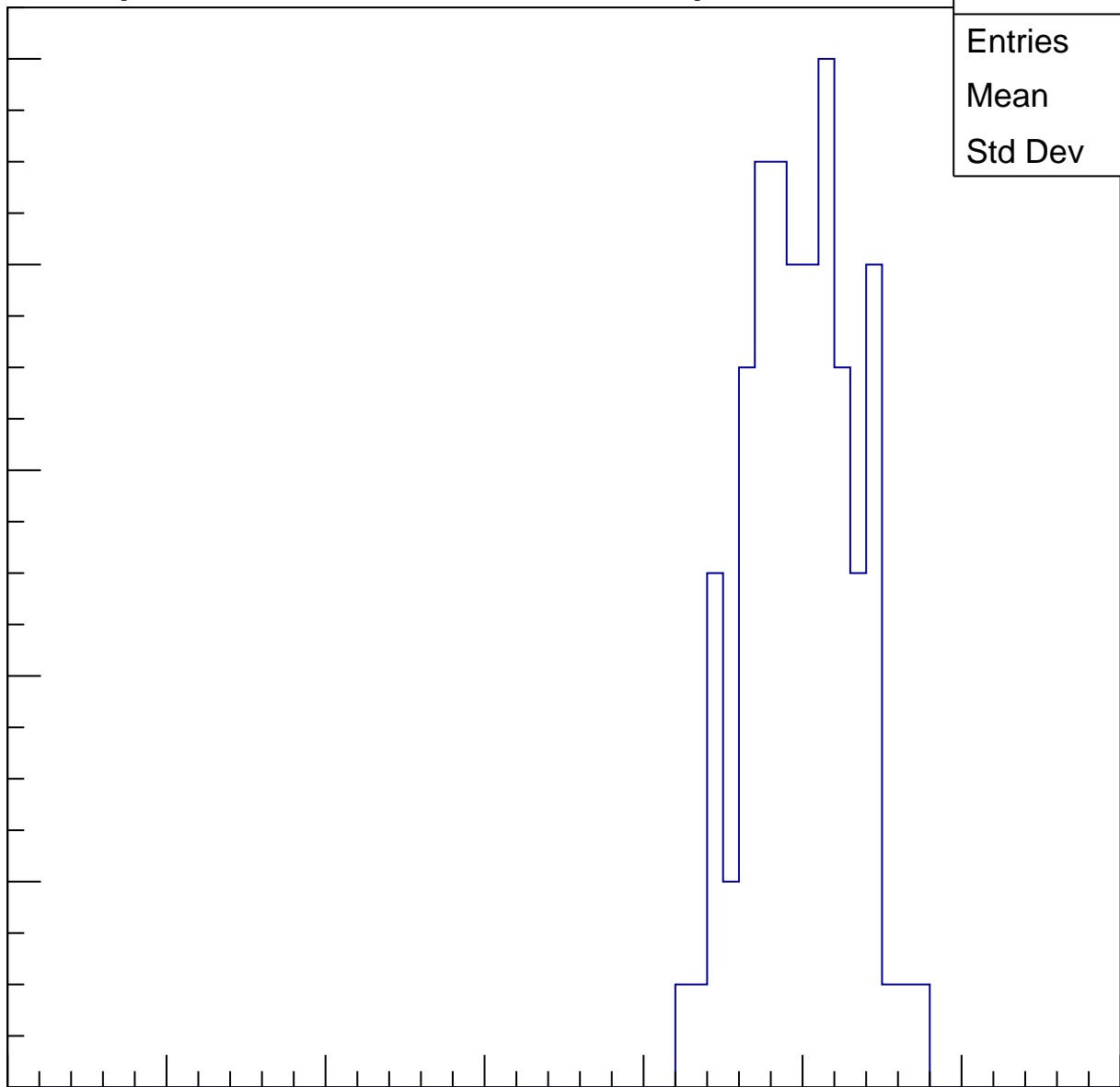
30

40

50

60

ampl



# B1L102S, U12-ch30, adc4

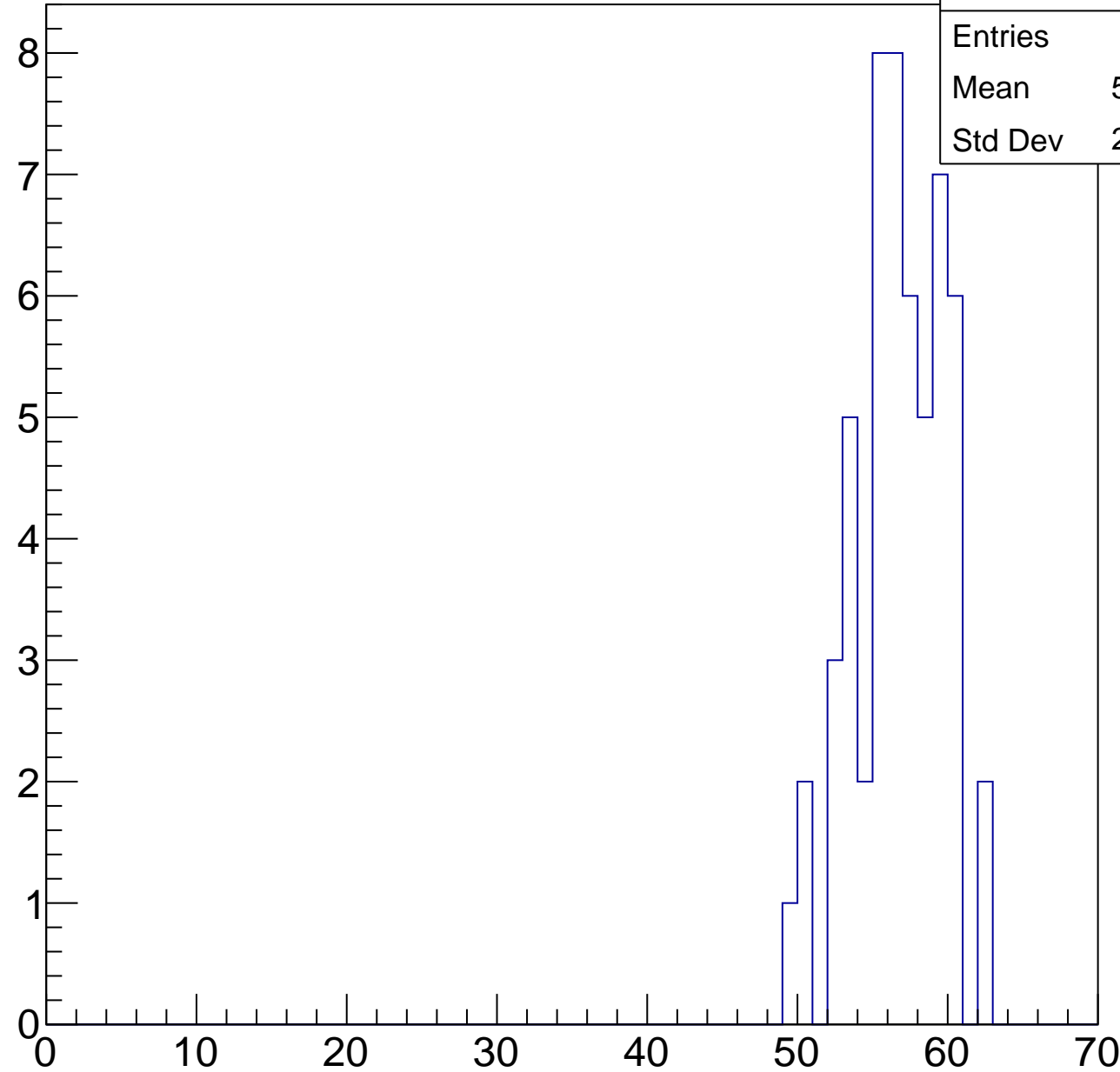
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	55
Mean	56.27
Std Dev	2.963

ampl

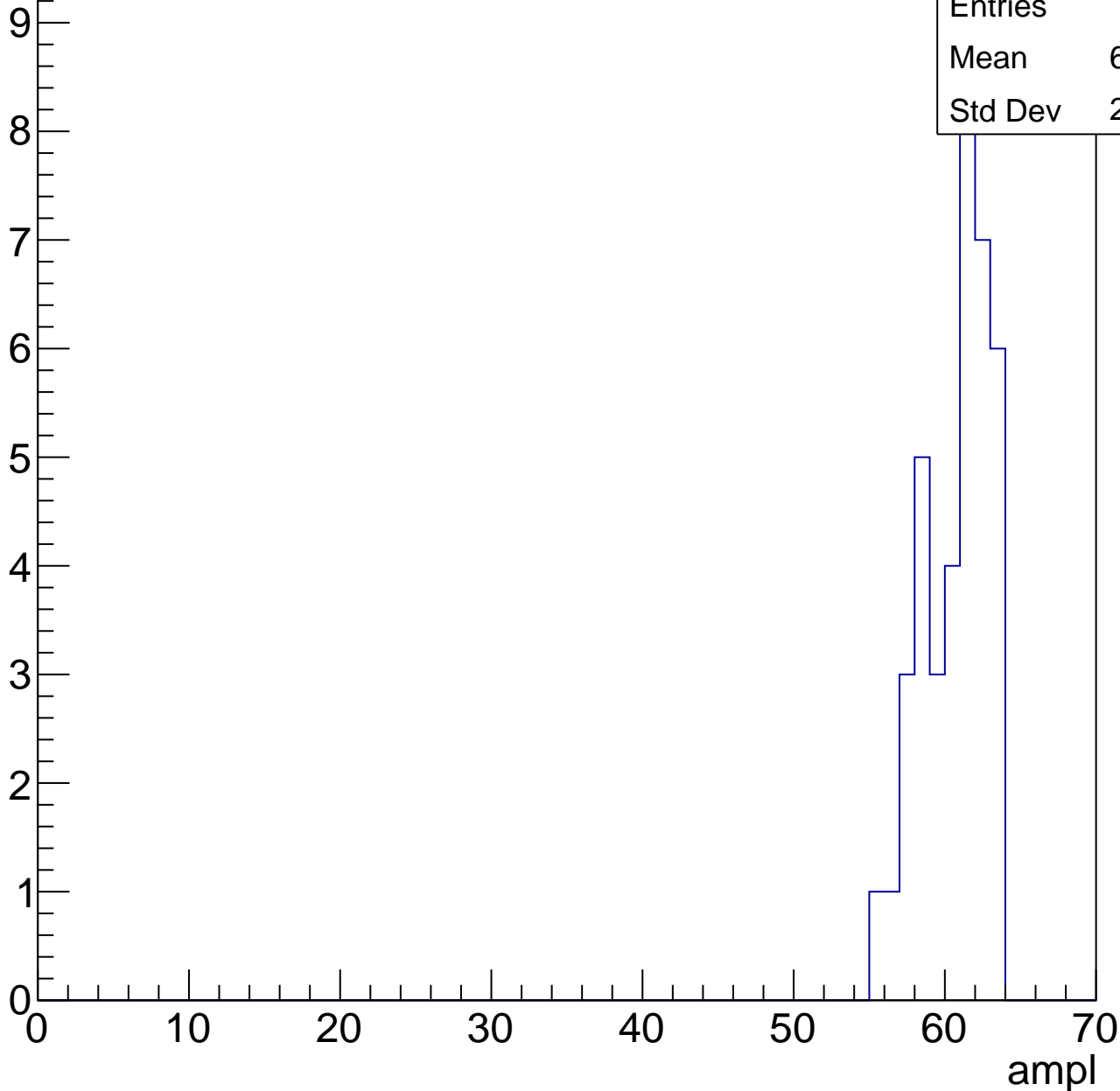


# B1L102S, U12-ch30, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

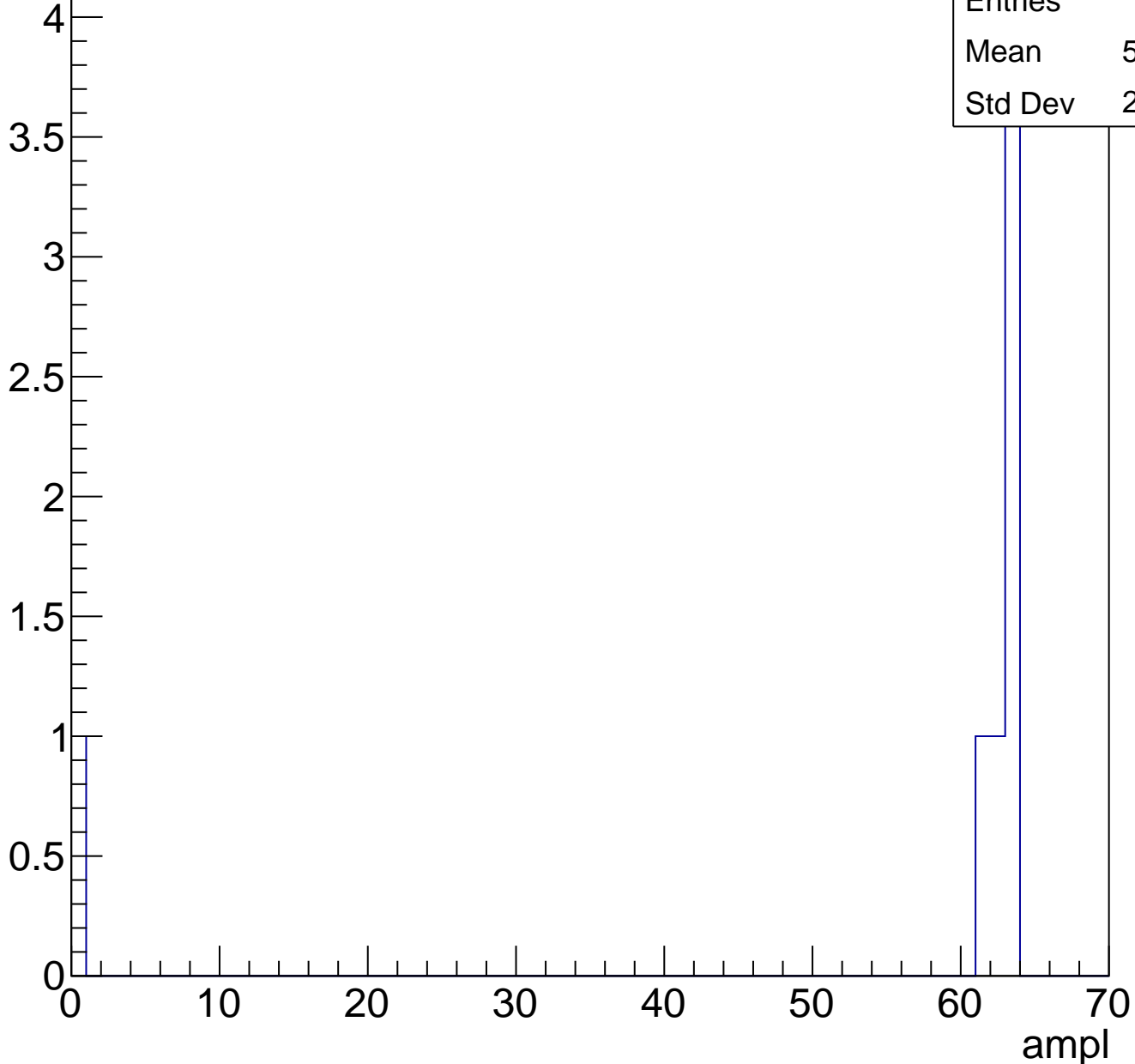
Entries	39
Mean	60.26
Std Dev	2.145



# B1L102S, U12-ch30, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	7
Mean	53.57
Std Dev	21.88



# B1L102S, U12-ch30, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L102S, U12-ch31, adc0

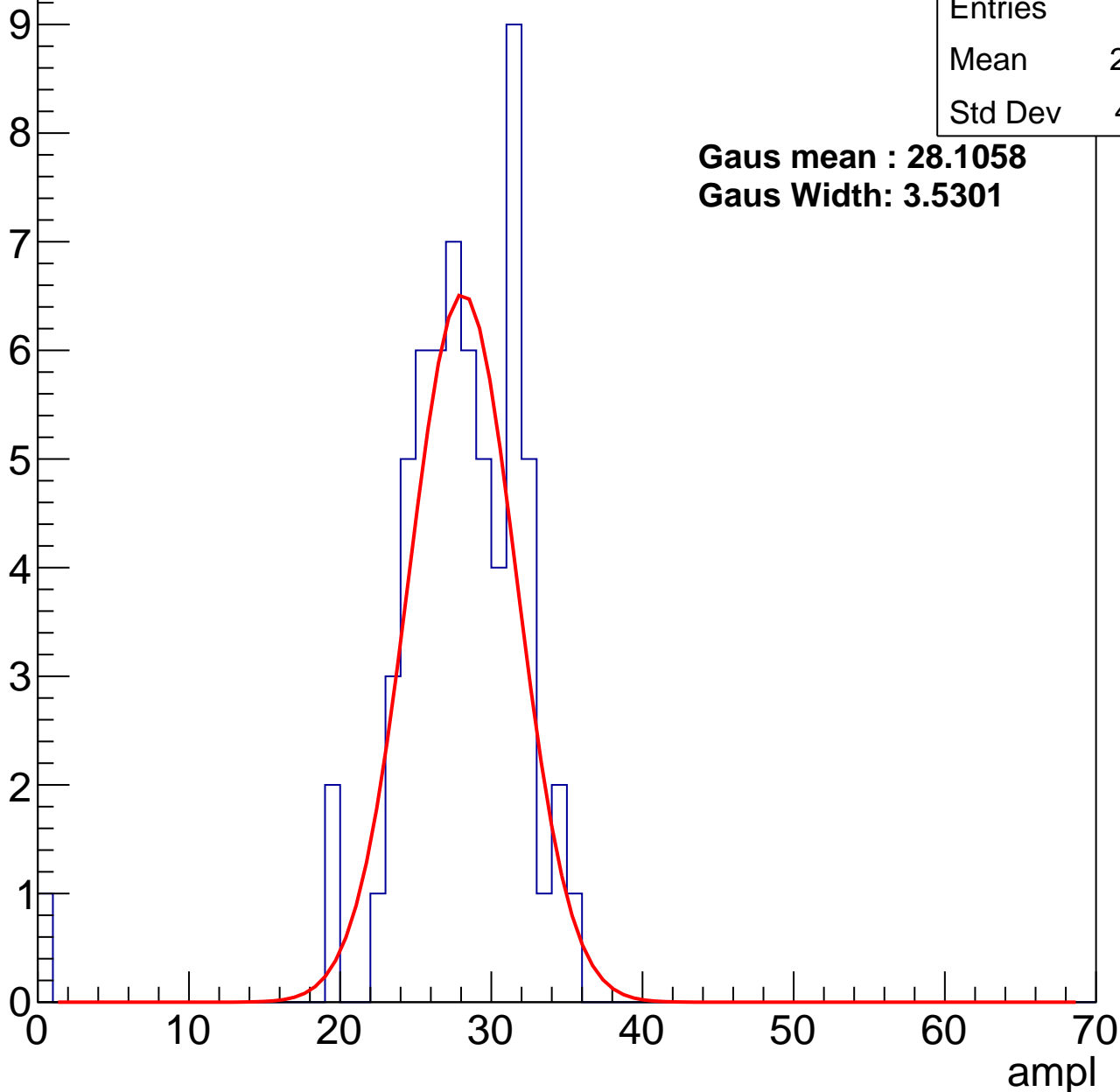
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	27.38
Std Dev	4.881

**Gaus mean : 28.1058**

**Gaus Width: 3.5301**



# B1L102S, U12-ch31, adc1

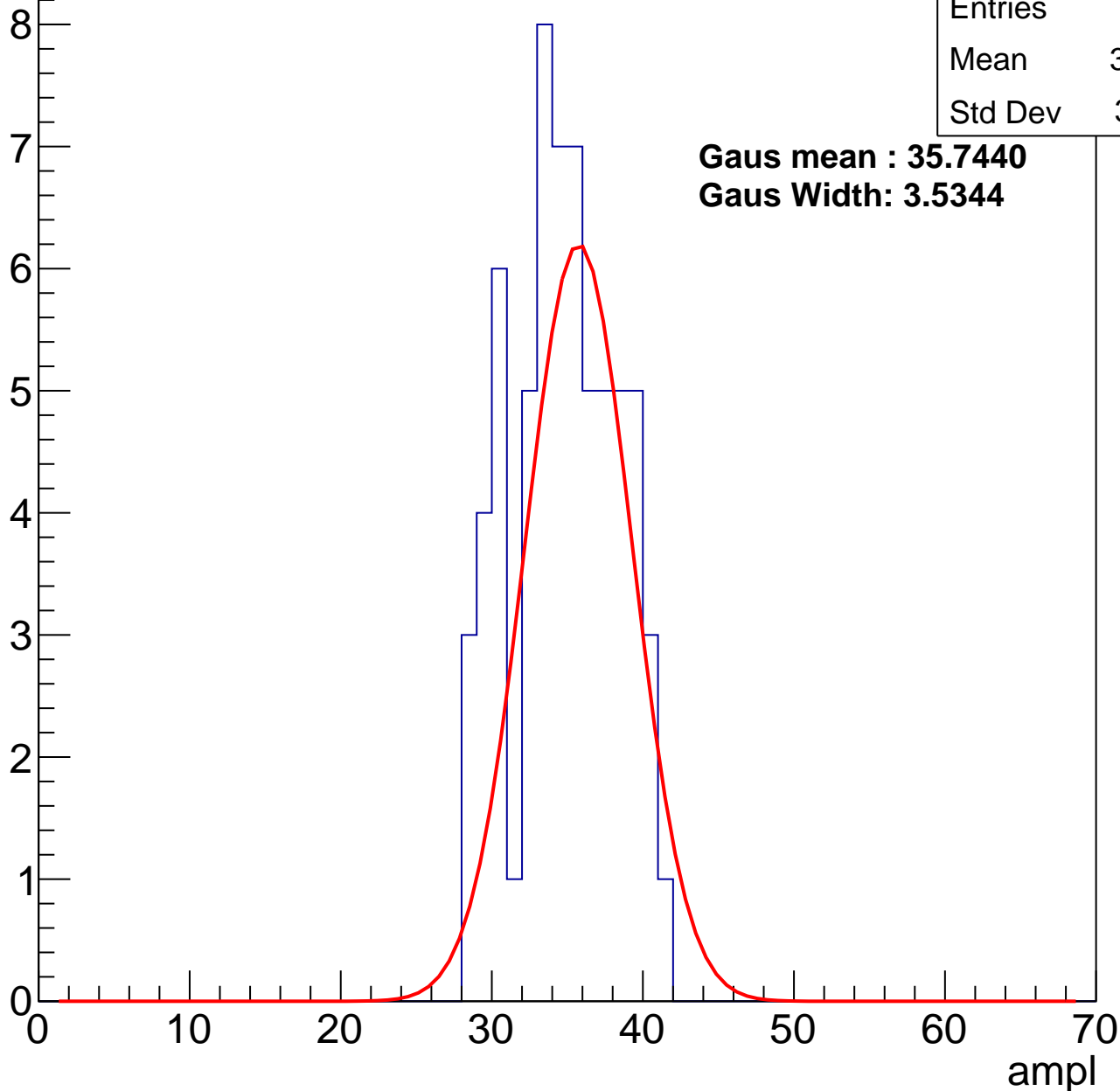
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	65
Mean	34.29
Std Dev	3.441

**Gaus mean : 35.7440**

**Gaus Width: 3.5344**



# B1L102S, U12-ch31, adc2

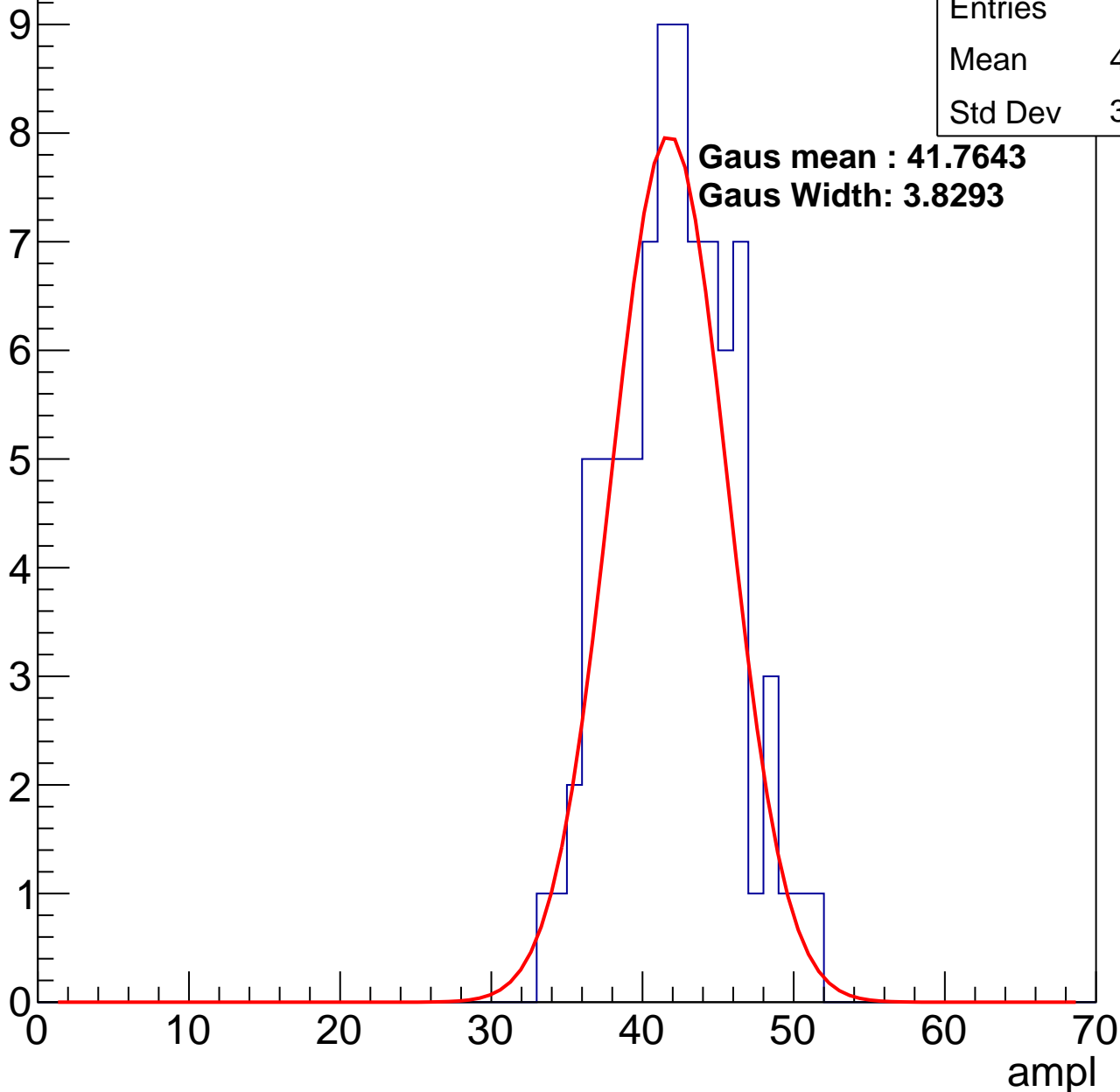
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	83
Mean	41.64
Std Dev	3.845

**Gaus mean : 41.7643**

**Gaus Width: 3.8293**

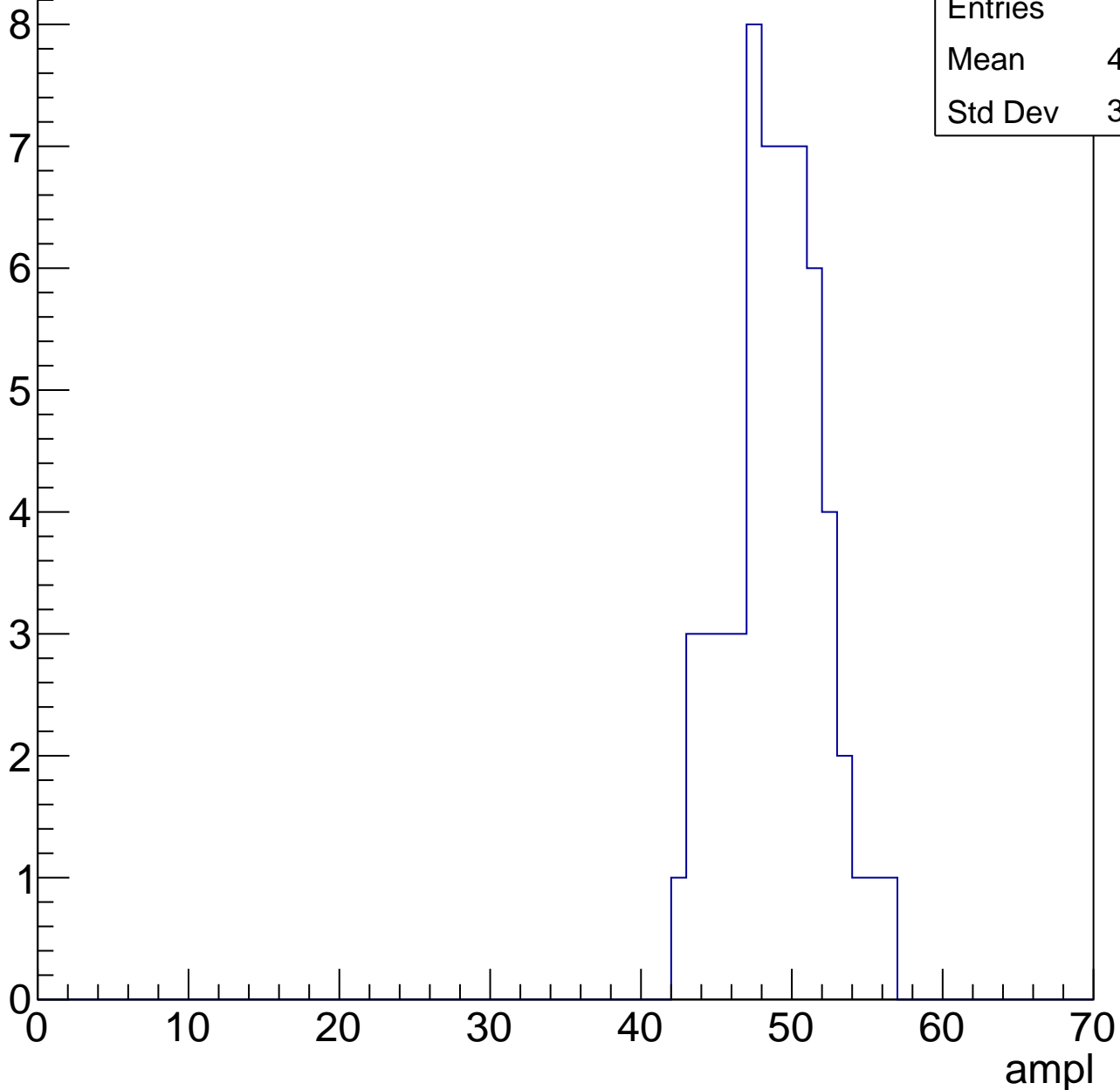


# B1L102S, U12-ch31, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	57
Mean	48.53
Std Dev	3.084

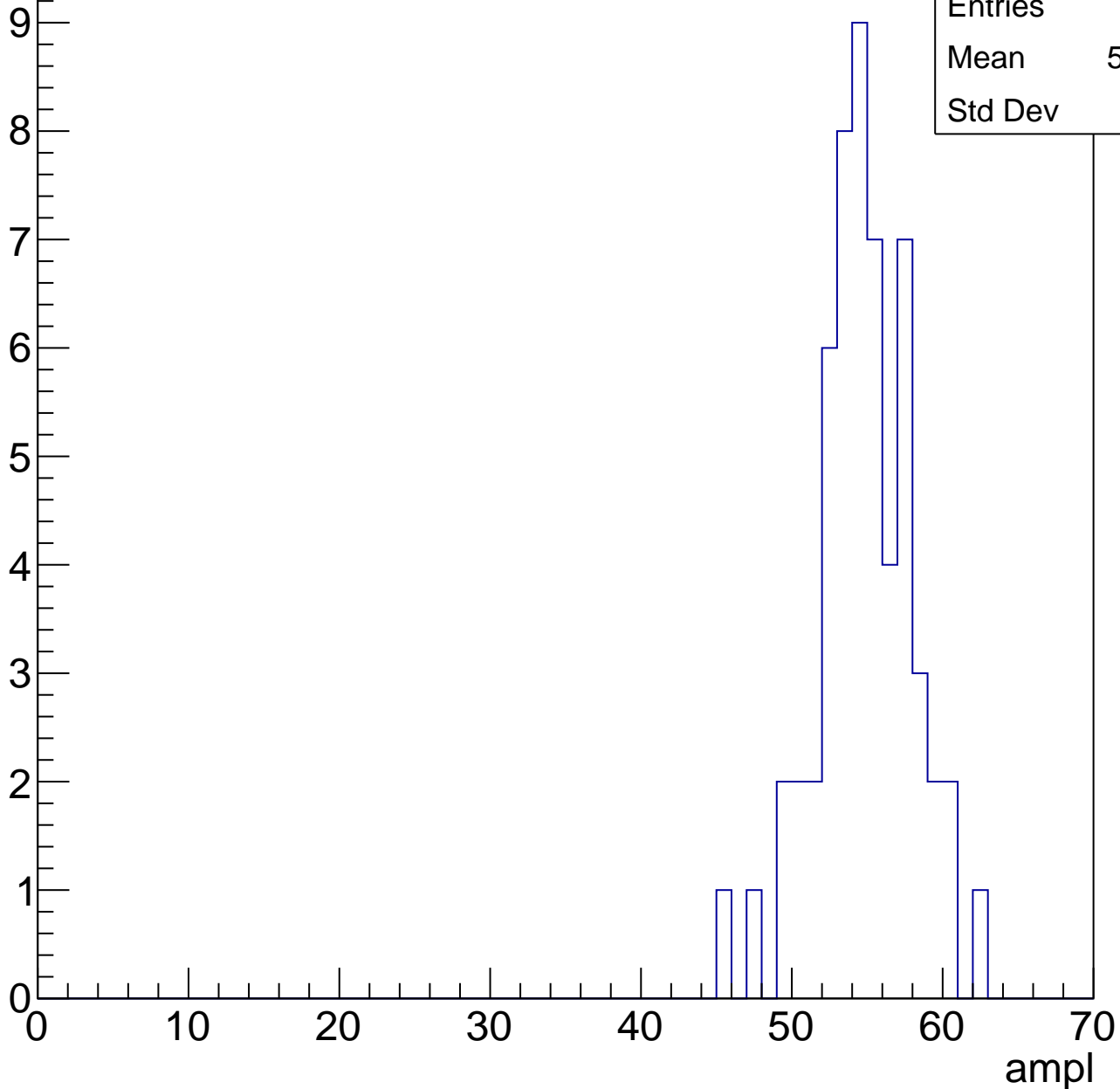


# B1L102S, U12-ch31, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	57
Mean	54.32
Std Dev	3.18

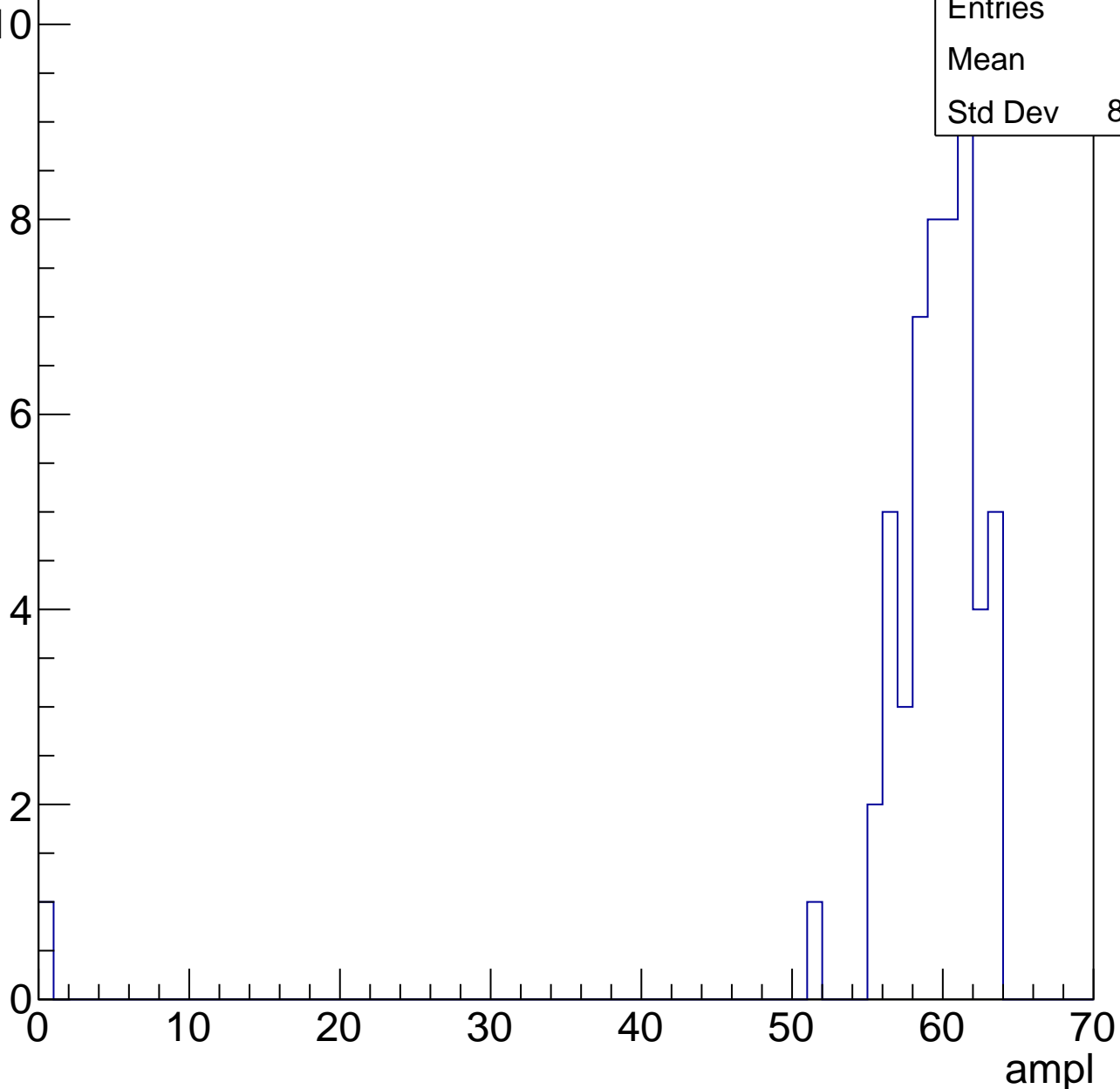


# B1L102S, U12-ch31, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	54
Mean	58.2
Std Dev	8.356

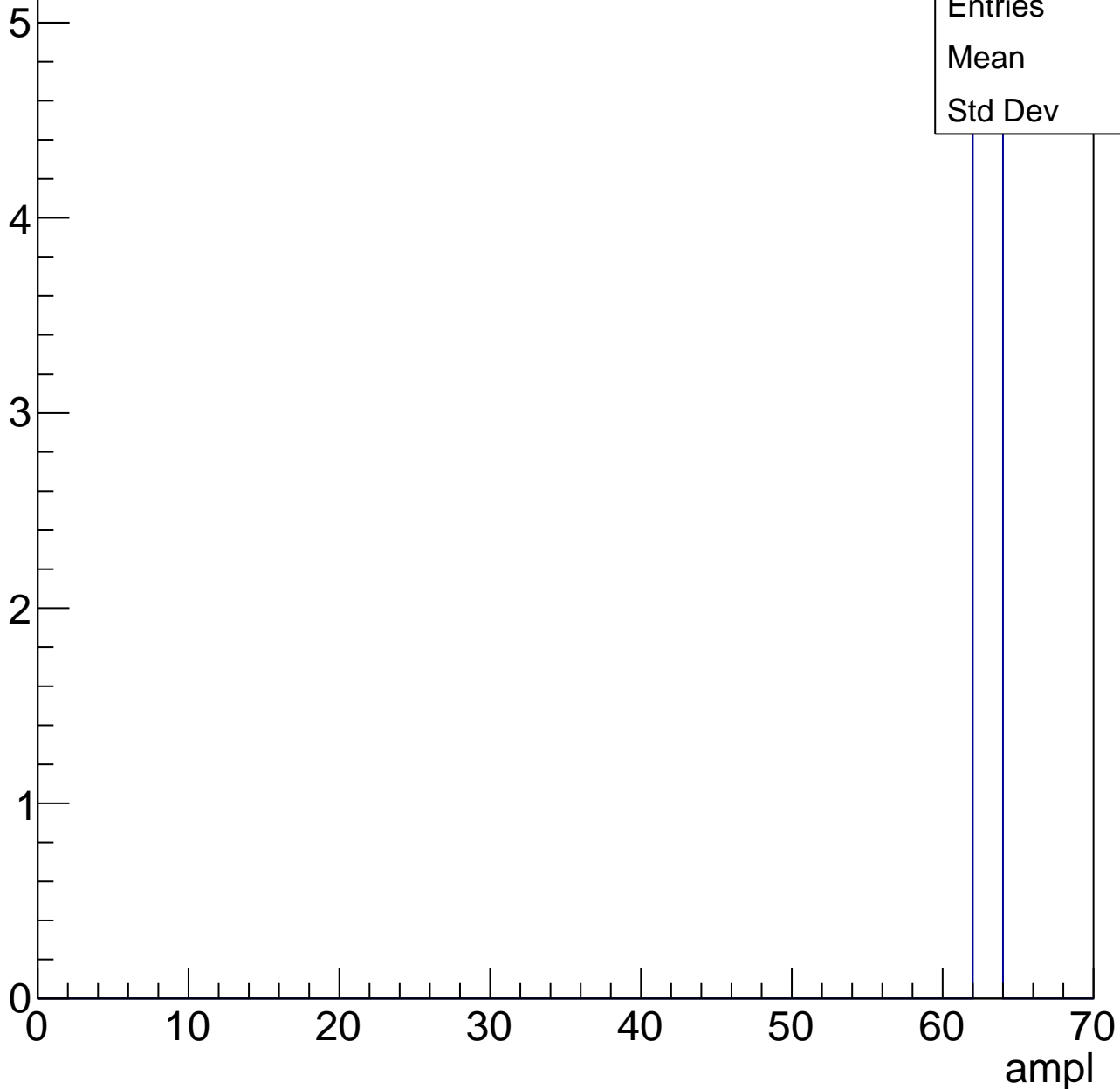


# B1L102S, U12-ch31, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	10
Mean	62.5
Std Dev	0.5





# B1L102S, U12-ch31, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L102S, U12-ch32, adc0

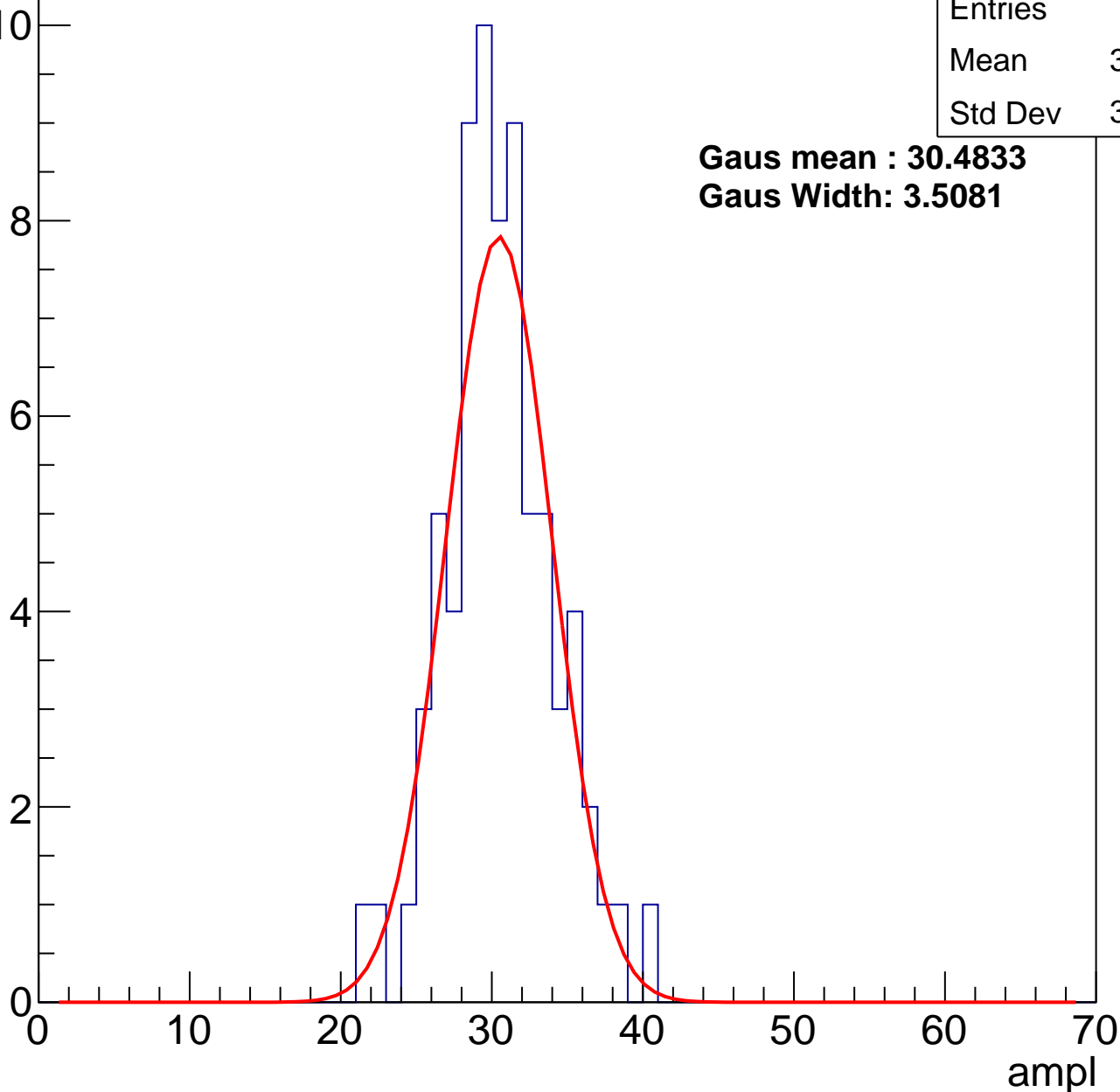
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	73
Mean	30.07
Std Dev	3.559

**Gaus mean : 30.4833**

**Gaus Width: 3.5081**



# B1L102S, U12-ch32, adc1

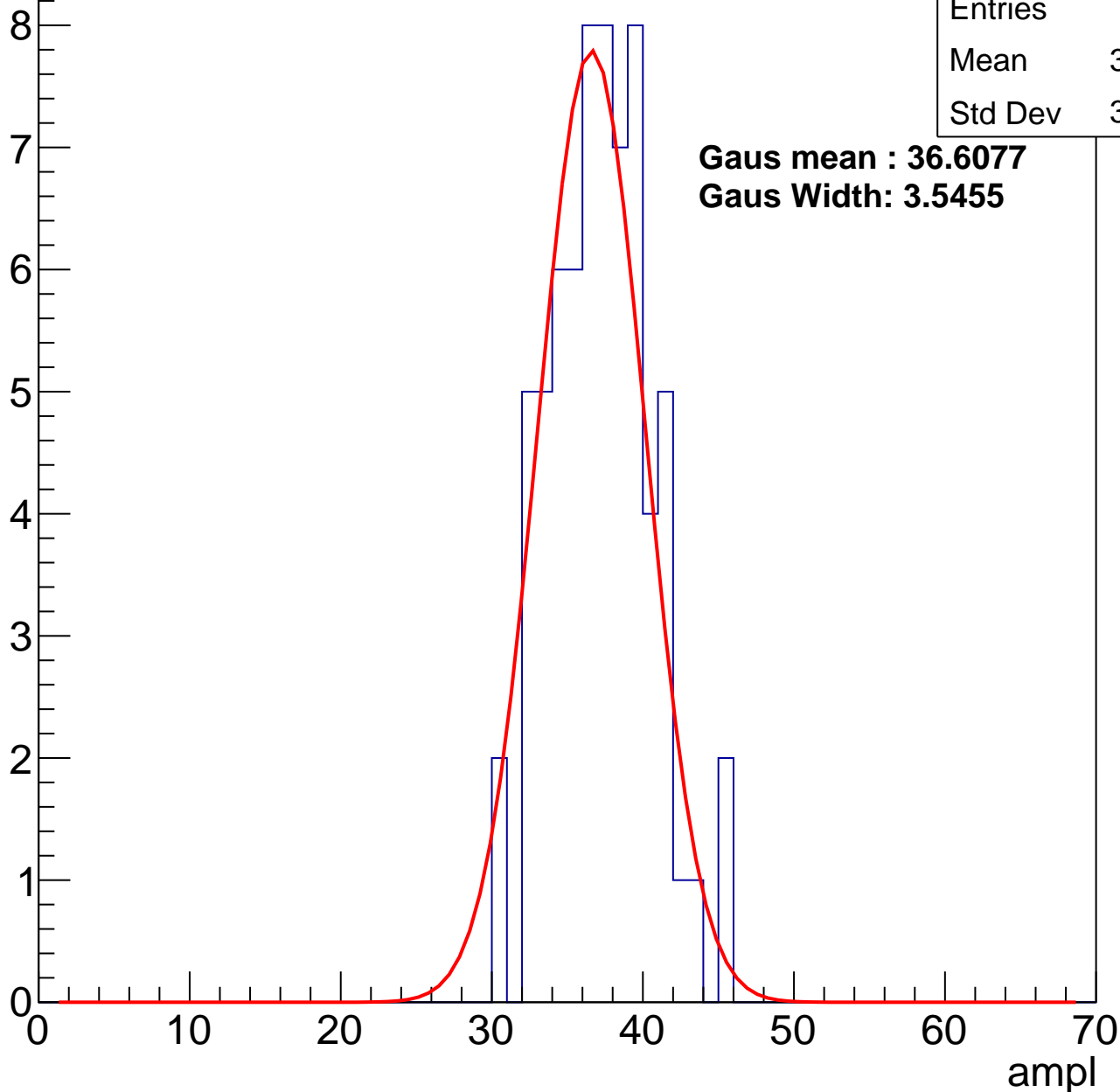
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	36.78
Std Dev	3.276

**Gaus mean : 36.6077**

**Gaus Width: 3.5455**



# B1L102S, U12-ch32, adc2

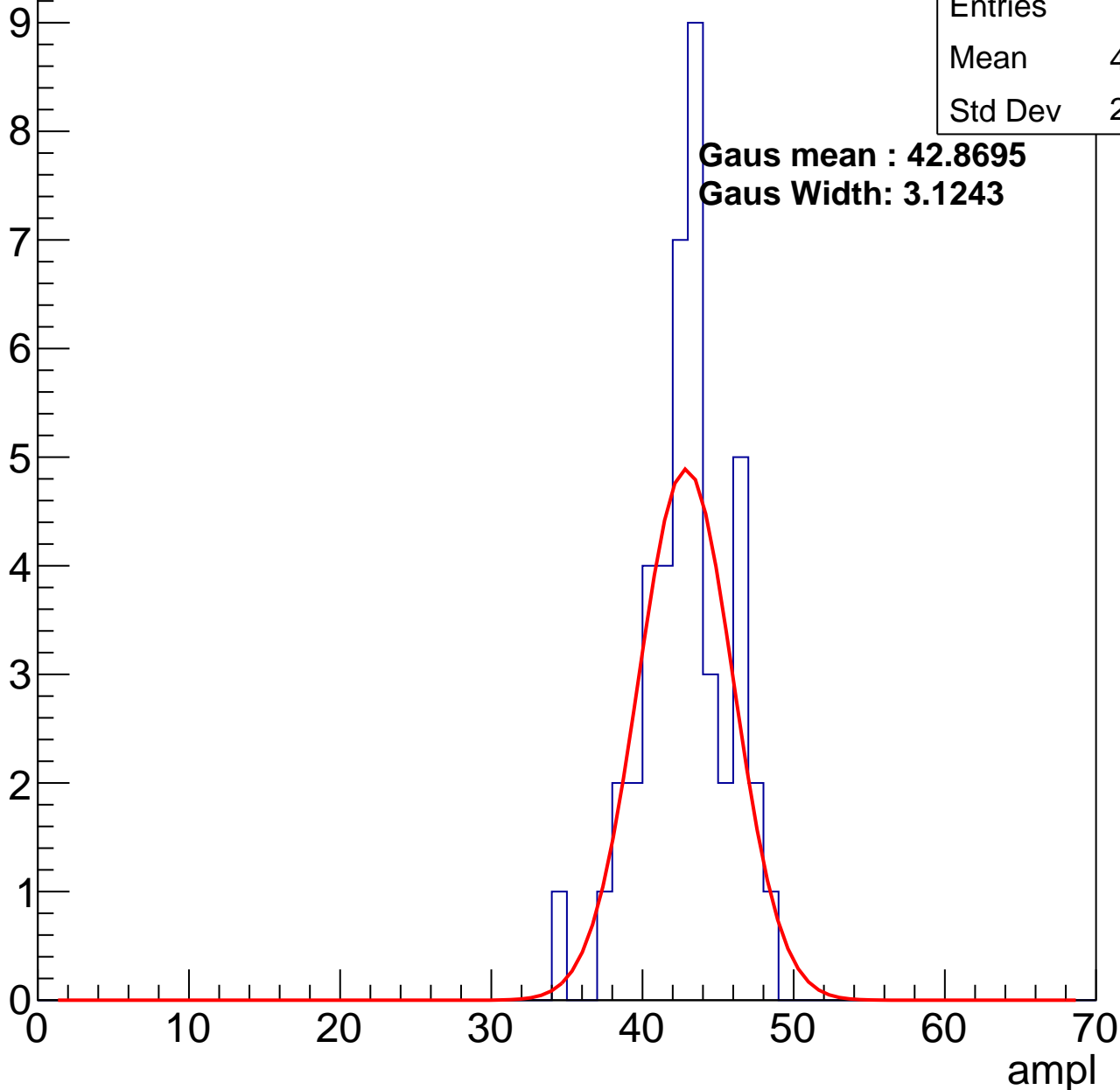
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	43
Mean	42.42
Std Dev	2.879

**Gaus mean : 42.8695**

**Gaus Width: 3.1243**

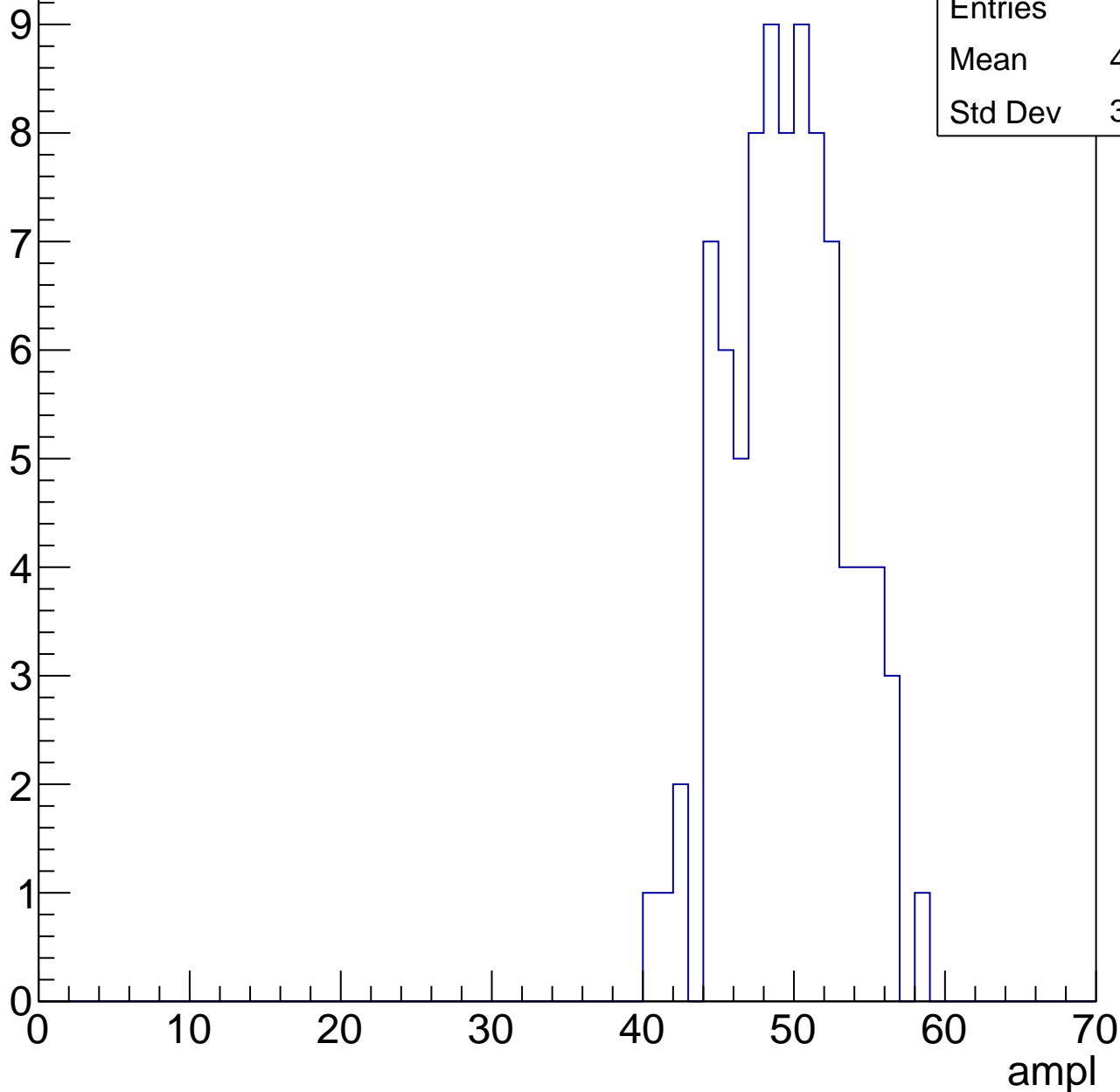


# B1L102S, U12-ch32, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	87
Mean	49.07
Std Dev	3.775

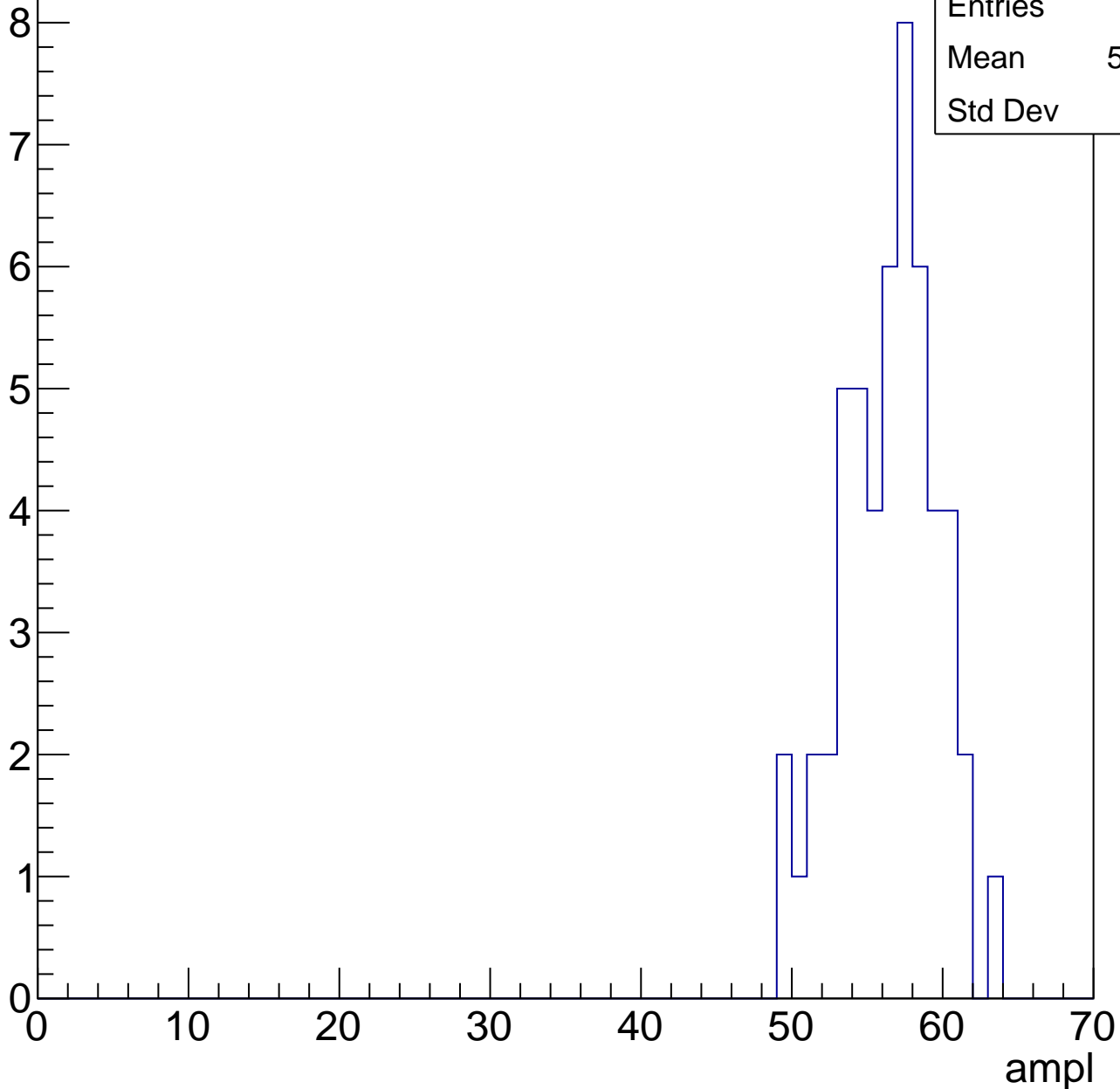


# B1L102S, U12-ch32, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	52
Mean	55.96
Std Dev	3.15

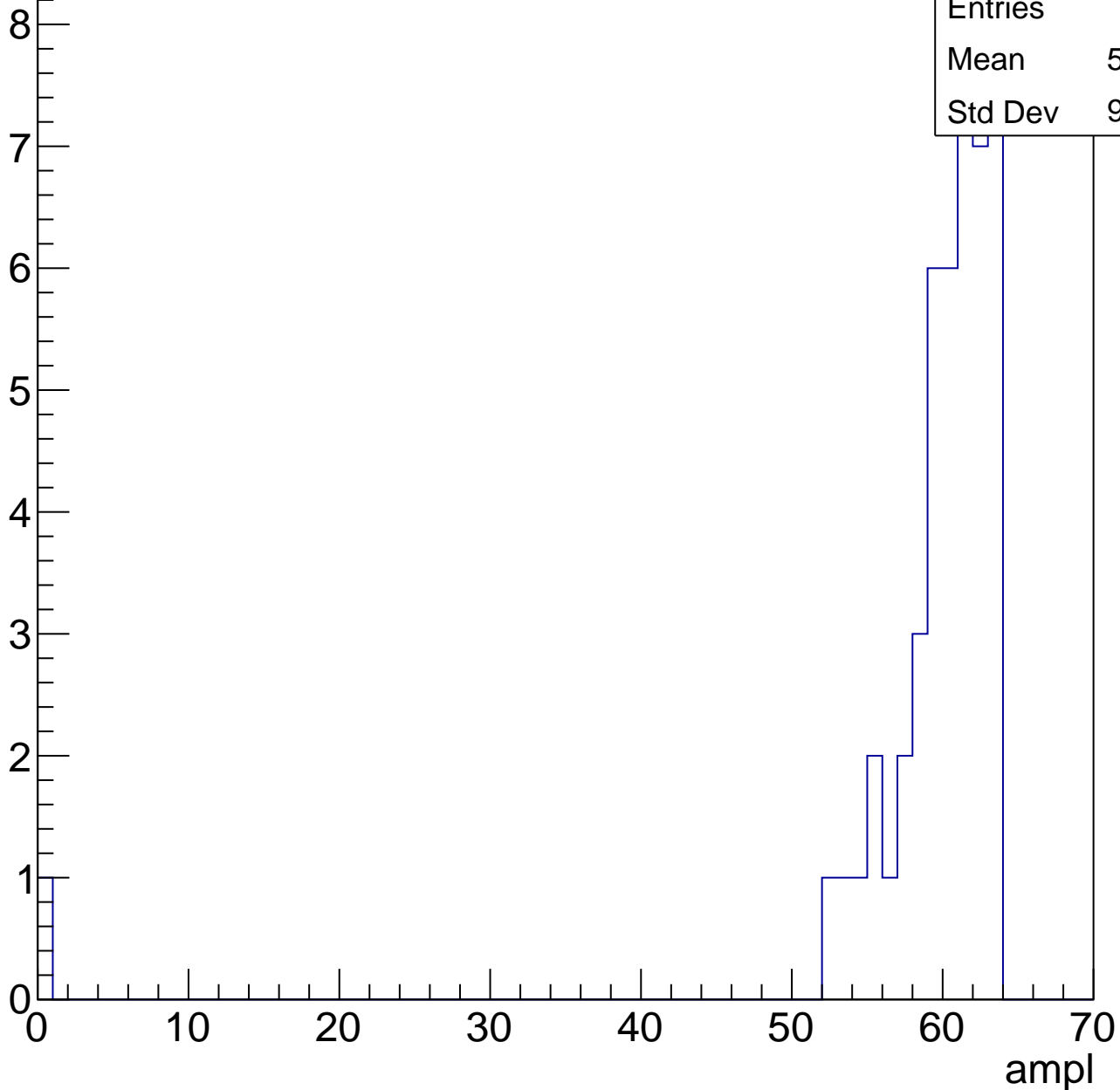


# B1L102S, U12-ch32, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	47
Mean	58.57
Std Dev	9.067



# B1L102S, U12-ch32, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

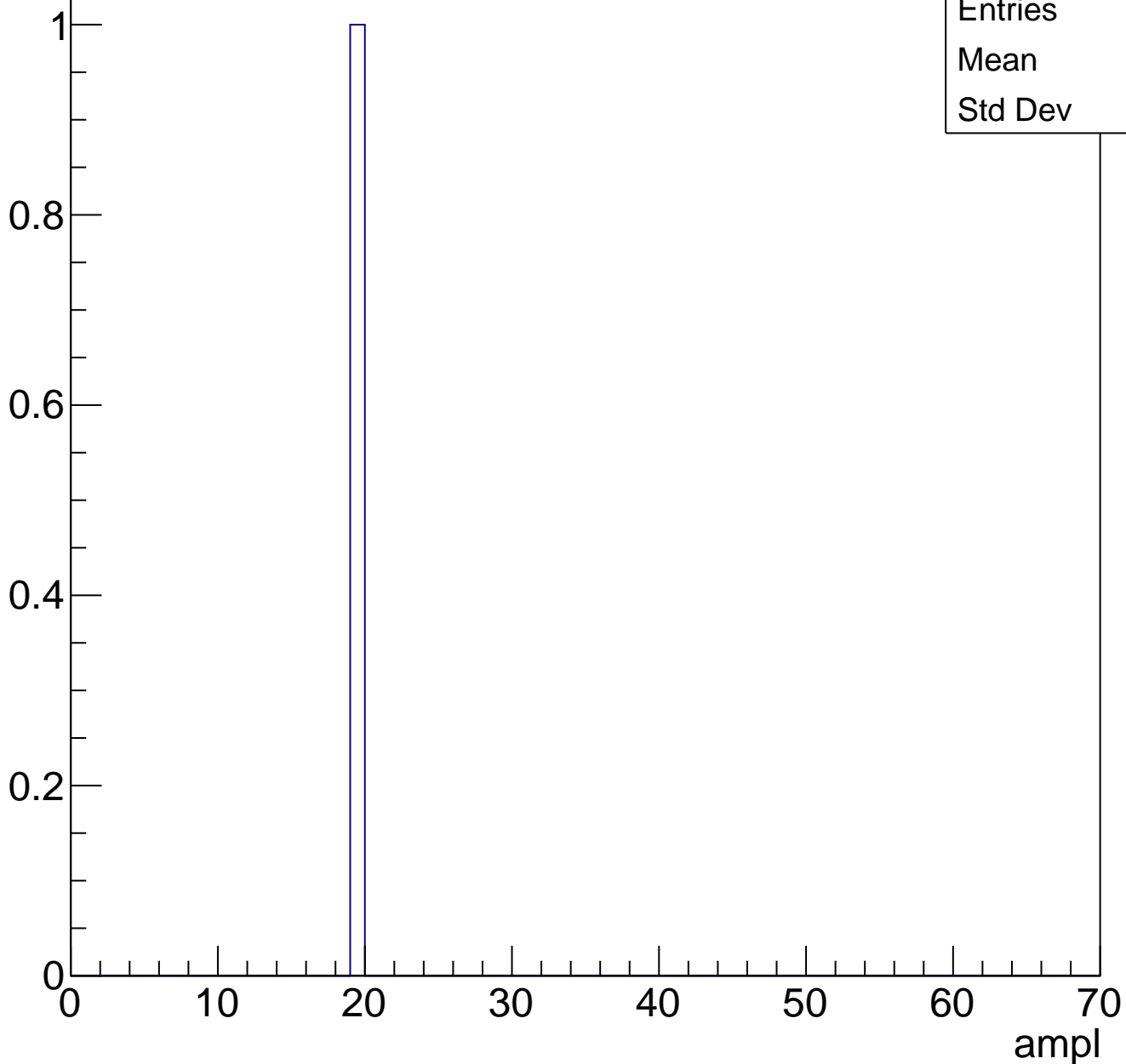




# B1L102S, U12-ch32, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U12-ch33, adc0

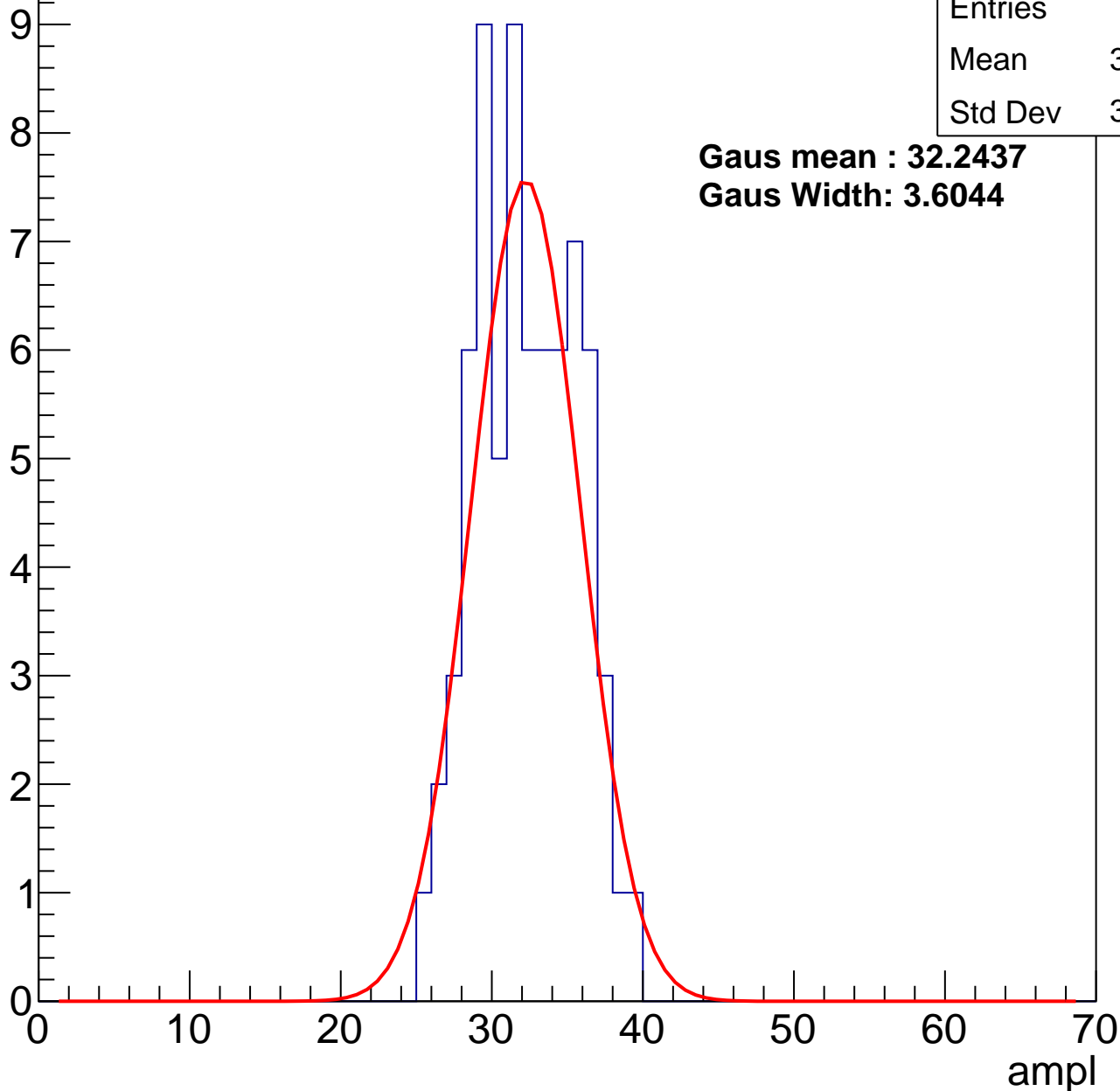
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	71
Mean	31.82
Std Dev	3.247

**Gaus mean : 32.2437**

**Gaus Width: 3.6044**



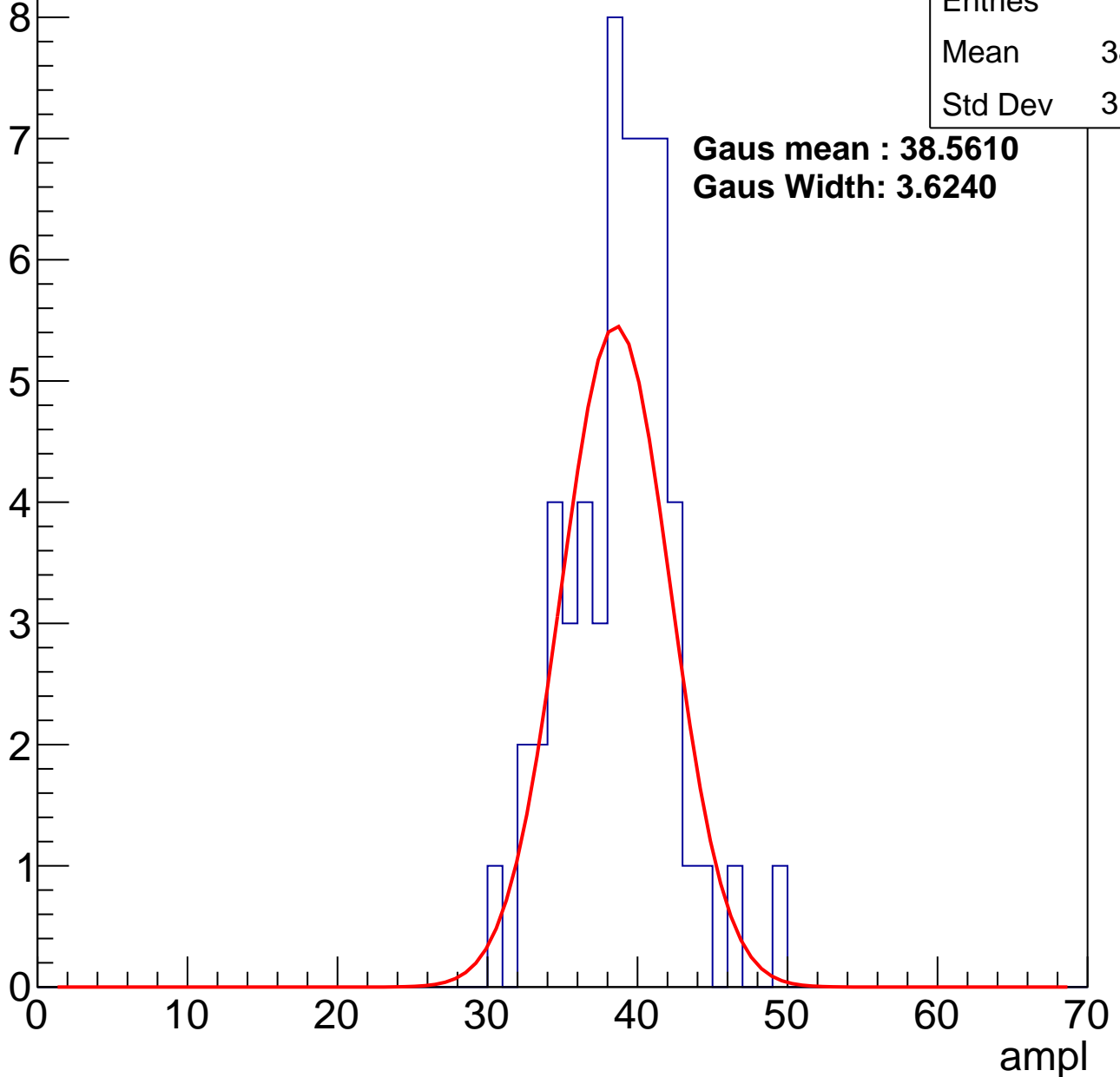
# B1L102S, U12-ch33, adc1

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	56
Mean	38.39
Std Dev	3.524

**Gaus mean : 38.5610**  
**Gaus Width: 3.6240**



# B1L102S, U12-ch33, adc2

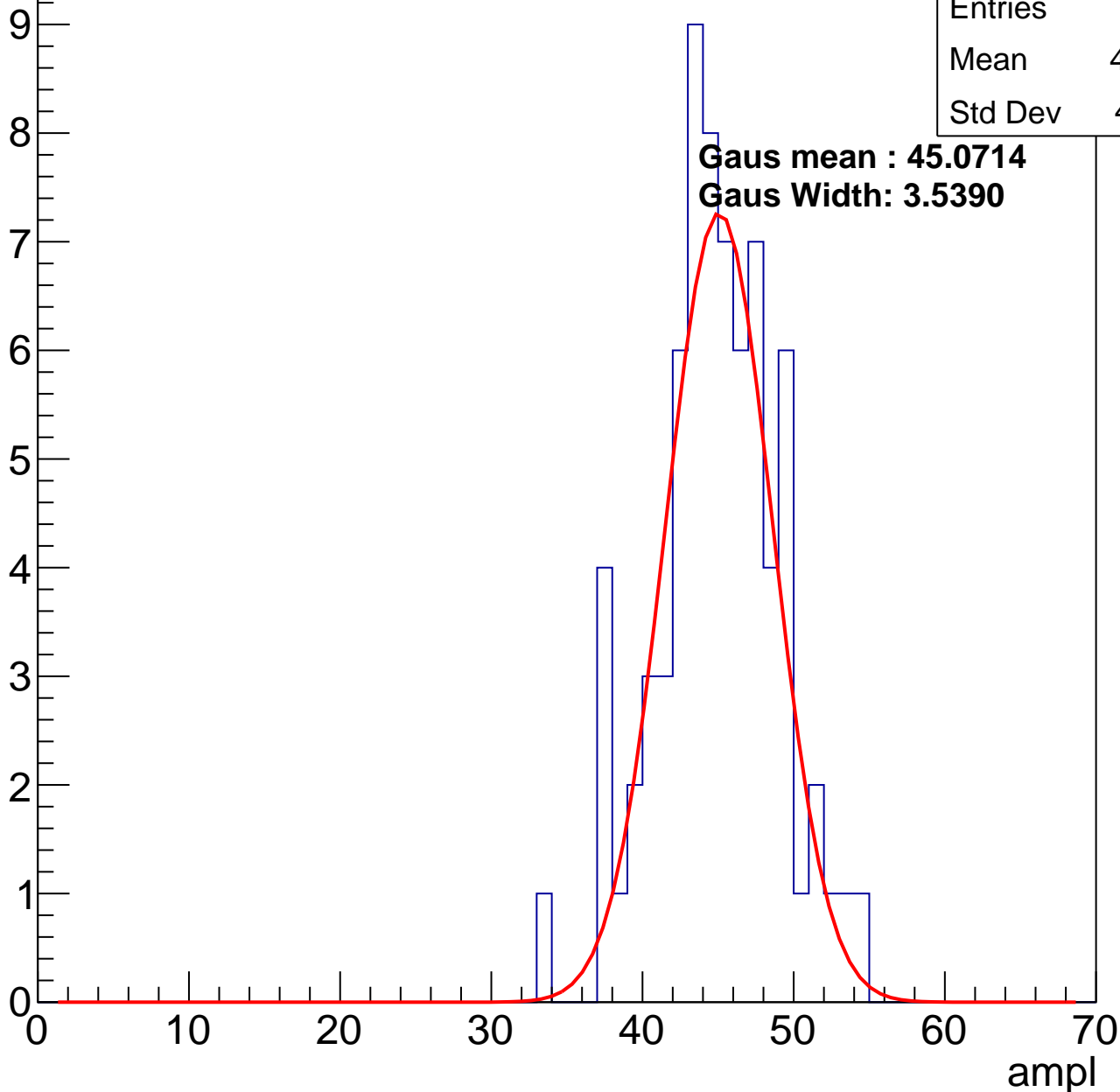
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	73
Mean	44.49
Std Dev	4.021

**Gaus mean : 45.0714**

**Gaus Width: 3.5390**

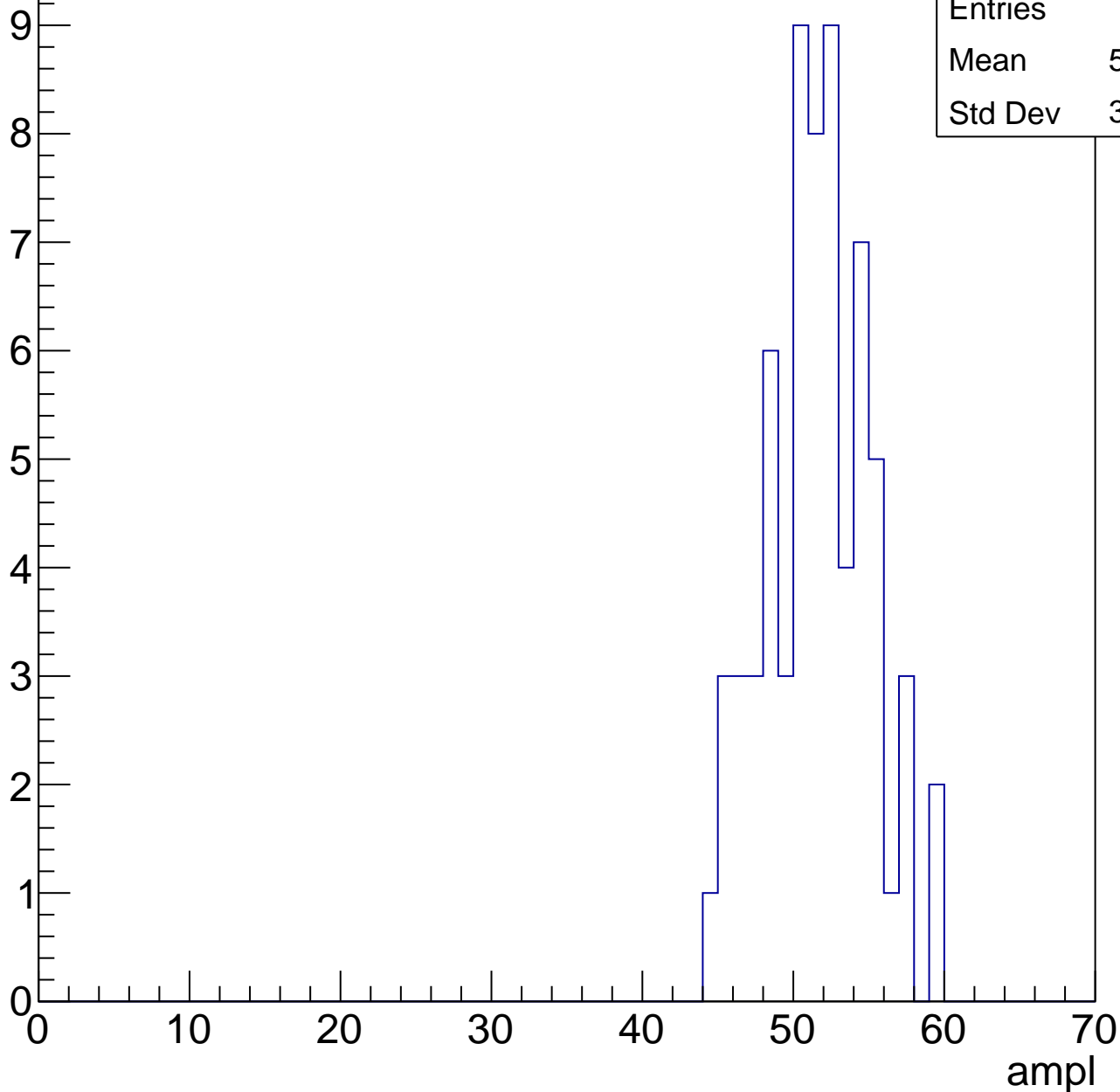


# B1L102S, U12-ch33, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	67
Mean	51.18
Std Dev	3.416

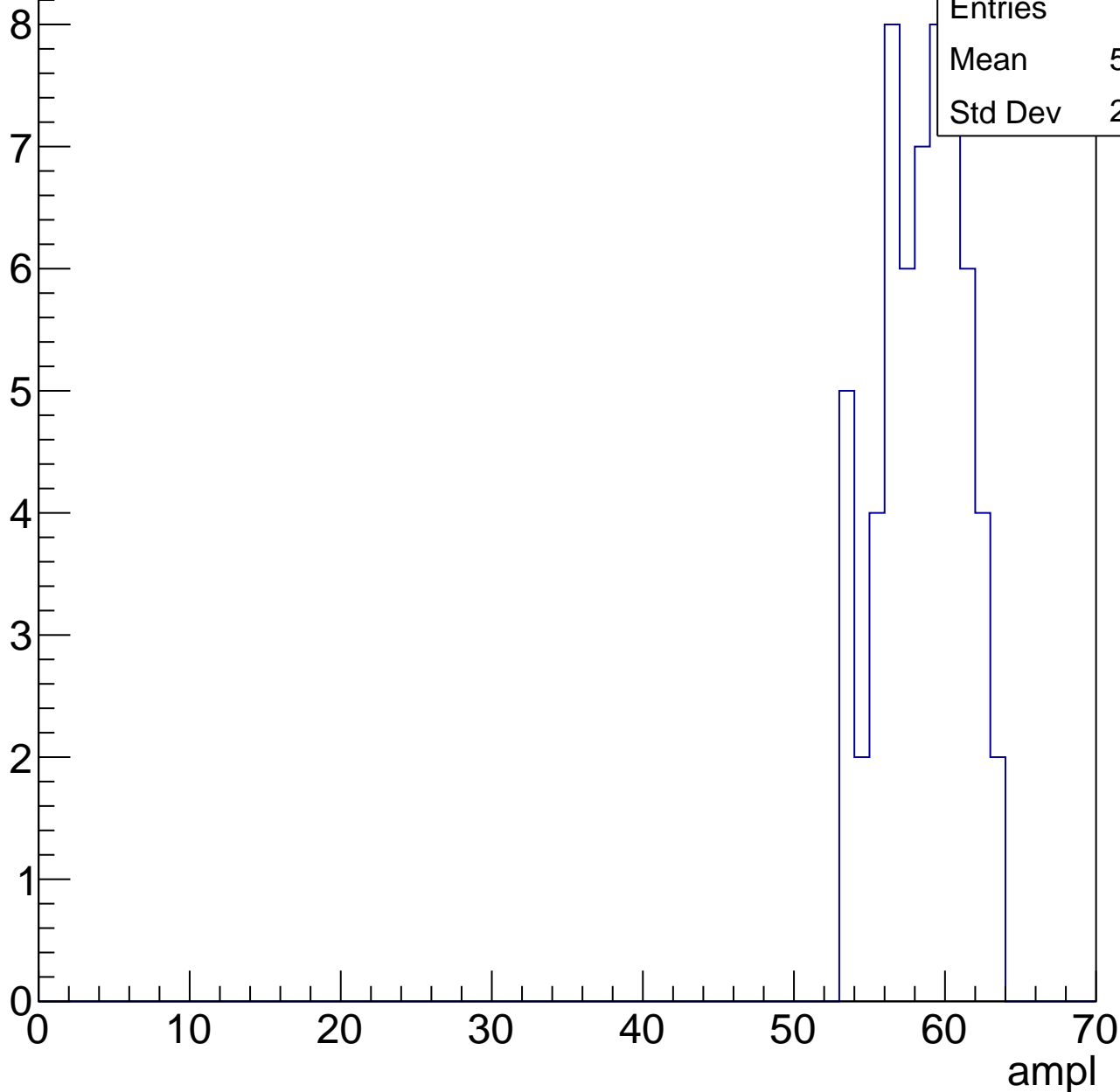


# B1L102S, U12-ch33, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	60
Mean	58.02
Std Dev	2.705

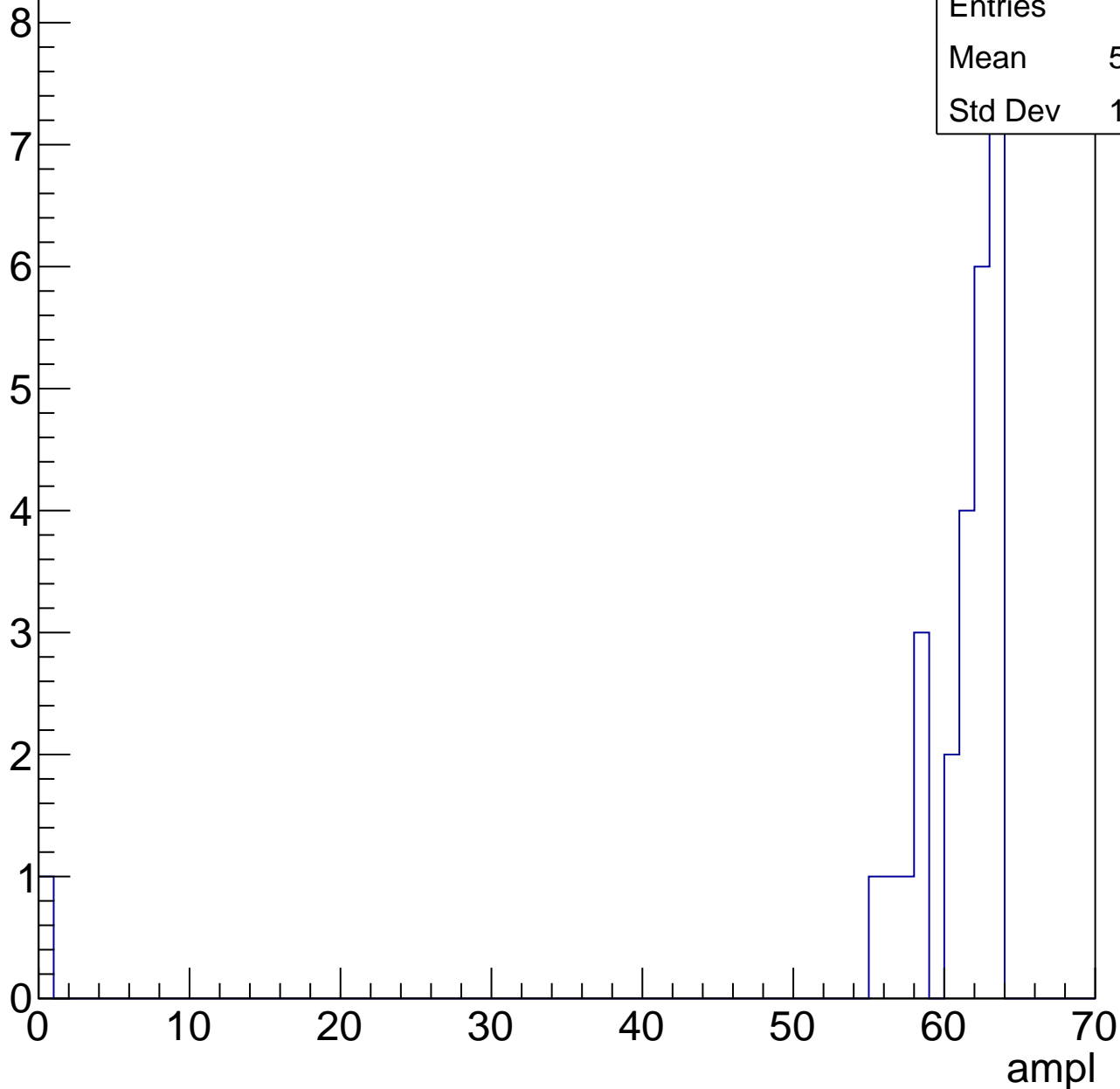


# B1L102S, U12-ch33, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	27
Mean	58.59
Std Dev	11.72



# B1L102S, U12-ch33, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0



# B1L102S, U12-ch33, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U12-ch34, adc0

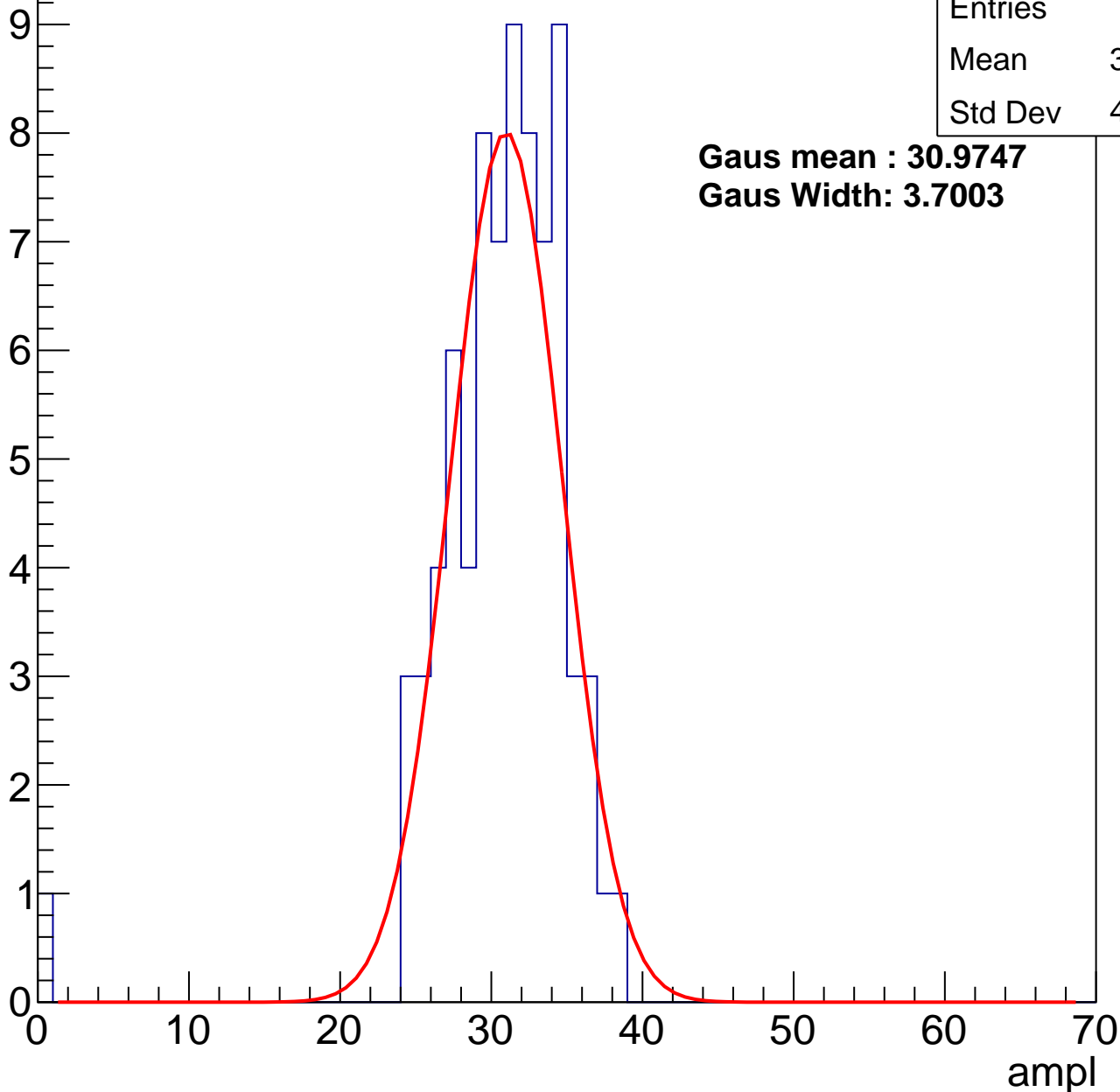
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	77
Mean	30.22
Std Dev	4.788

**Gaus mean : 30.9747**

**Gaus Width: 3.7003**



# B1L102S, U12-ch34, adc1

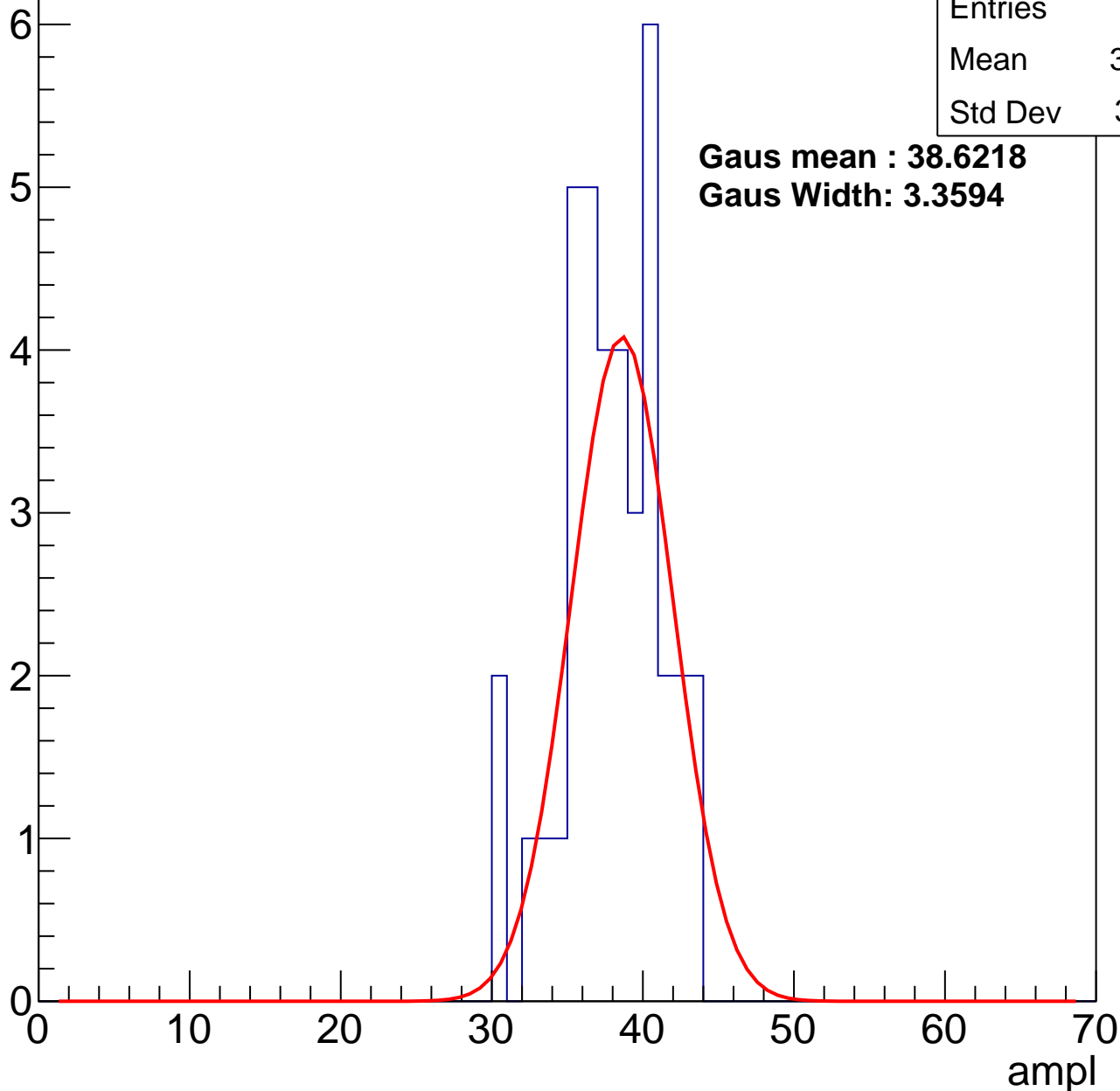
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	38
Mean	37.45
Std Dev	3.201

**Gaus mean : 38.6218**

**Gaus Width: 3.3594**



# B1L102S, U12-ch34, adc2

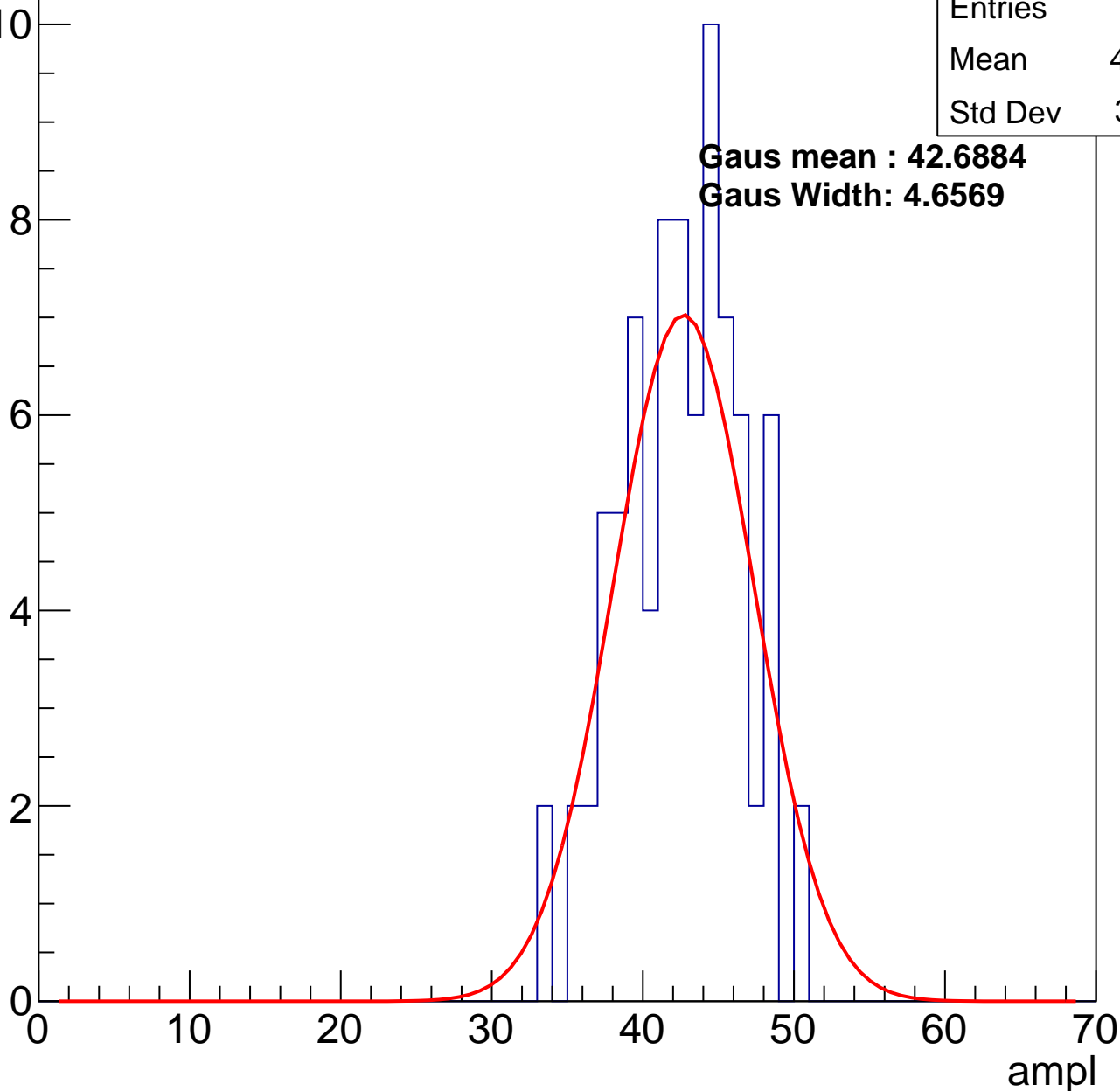
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	82
Mean	42.09
Std Dev	3.861

**Gaus mean : 42.6884**

**Gaus Width: 4.6569**

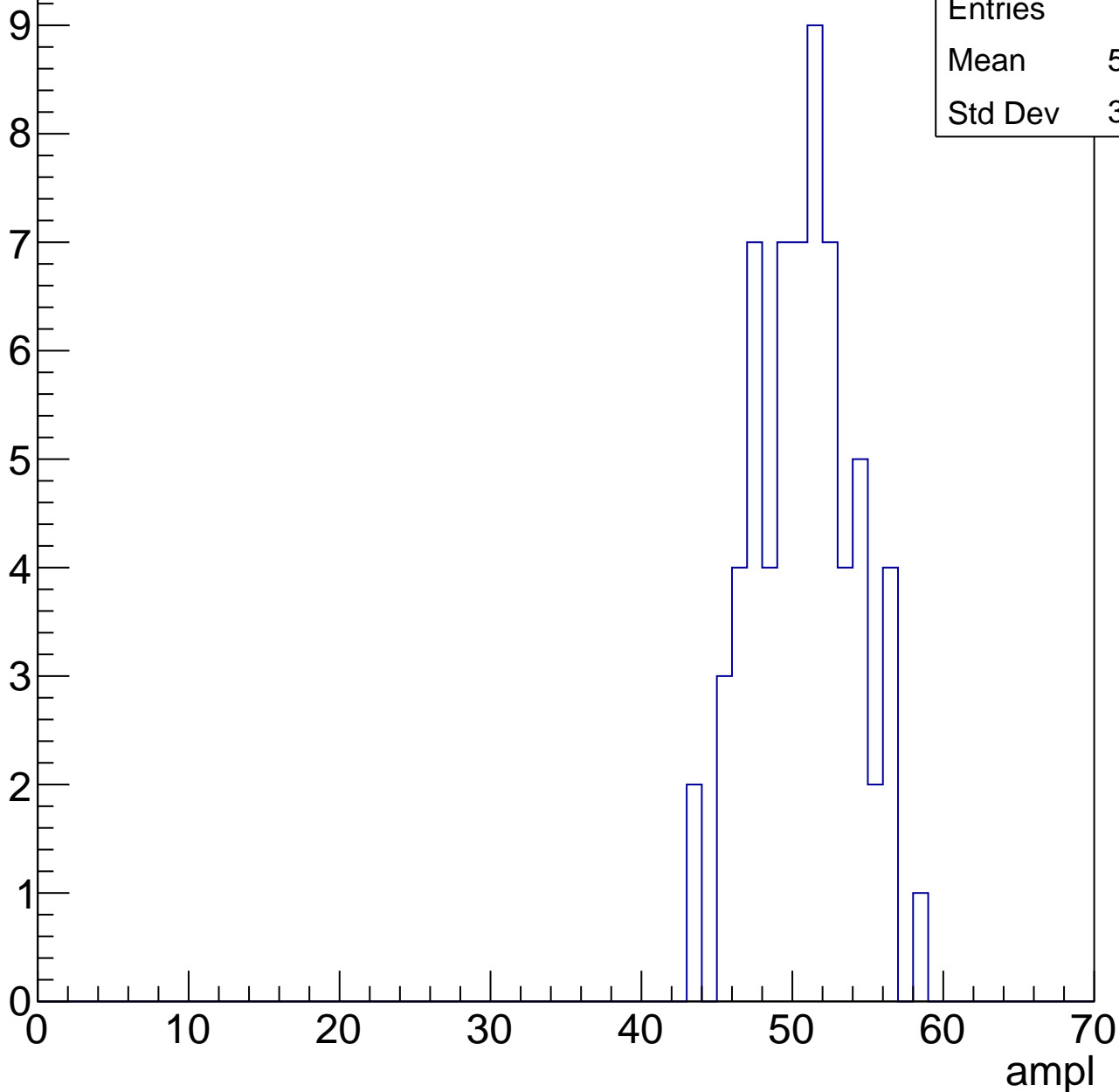


# B1L102S, U12-ch34, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

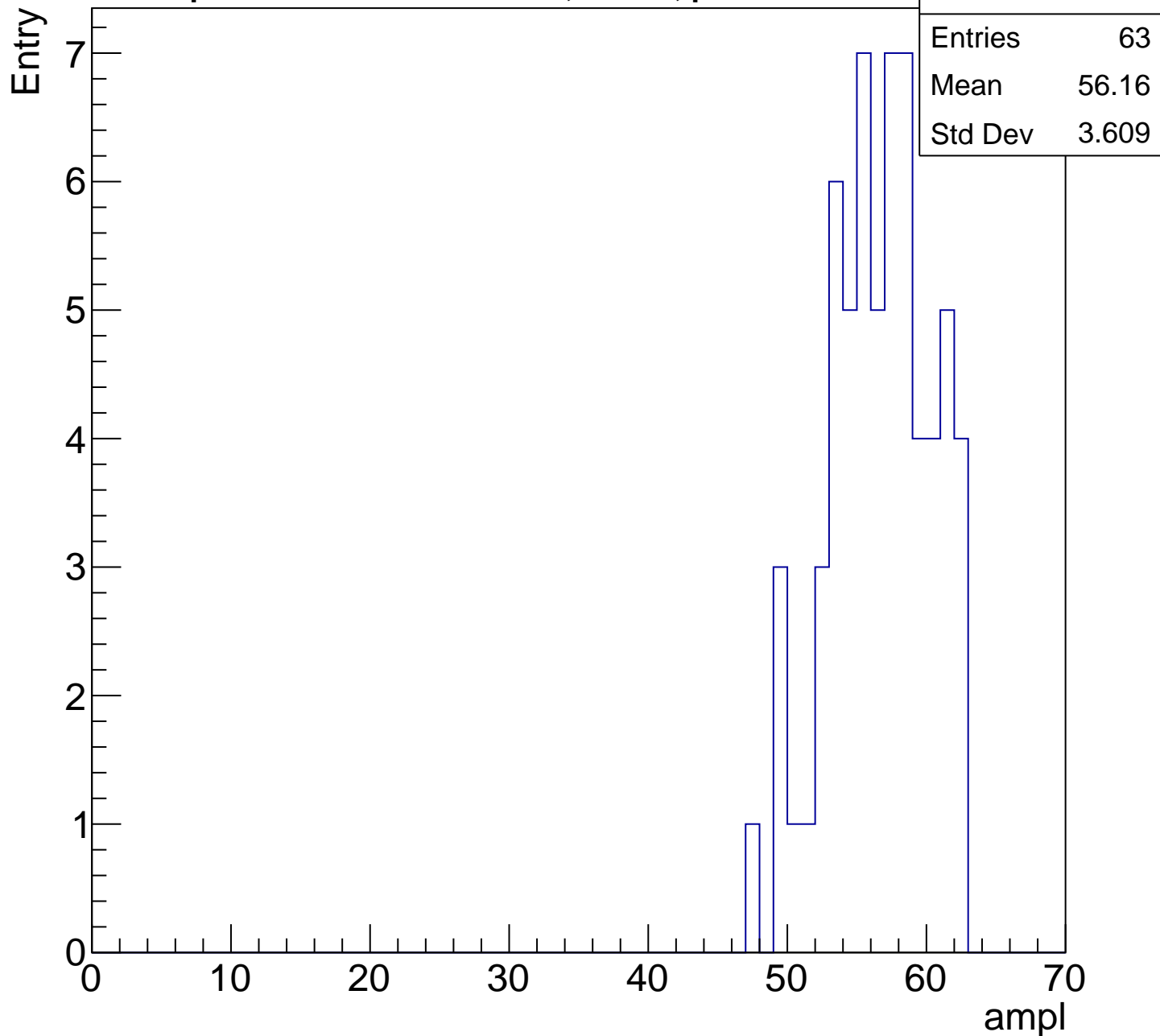
Entry

Entries	66
Mean	50.24
Std Dev	3.326



# B1L102S, U12-ch34, adc4

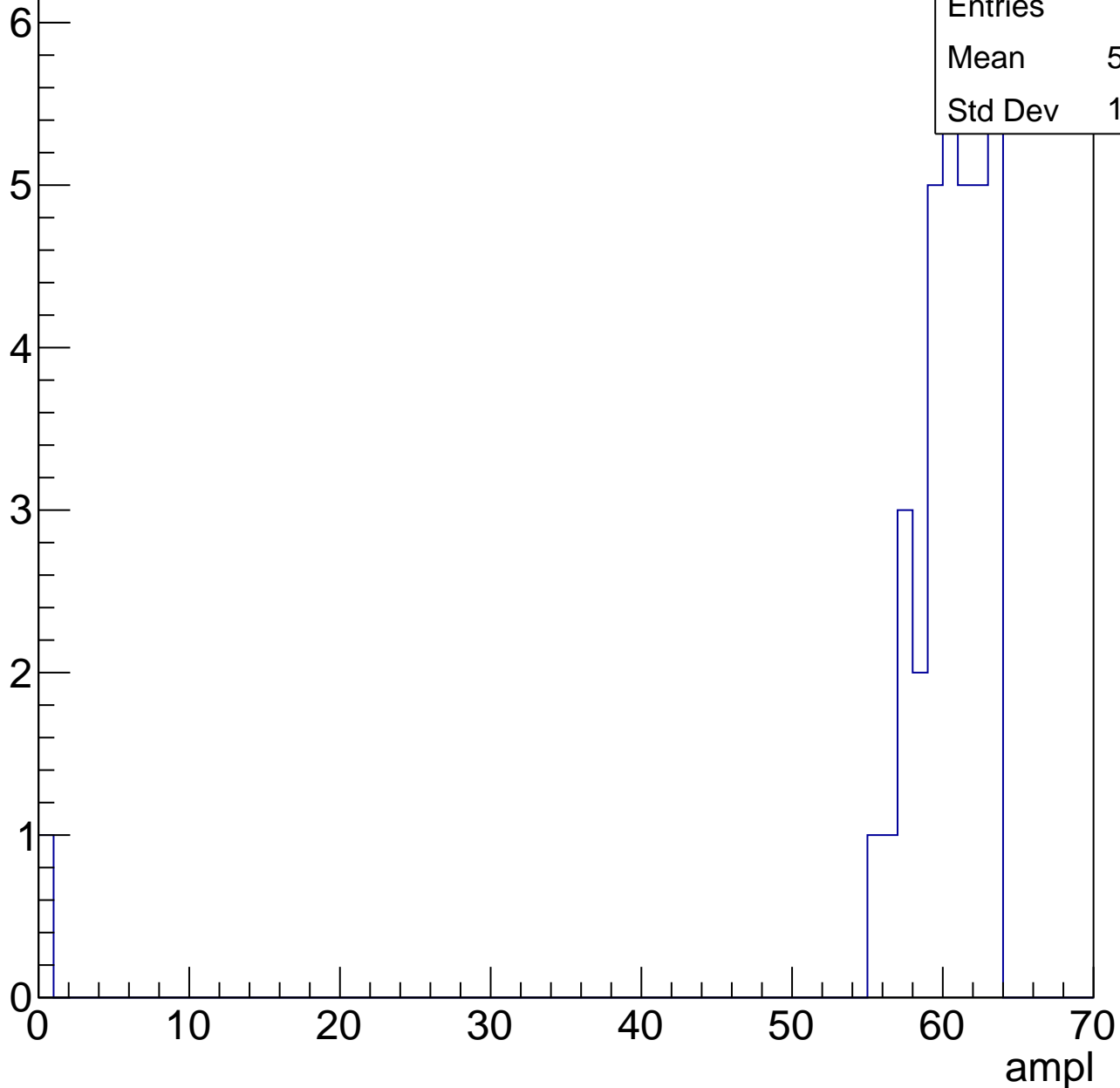
calib\_packv5\_042523\_0143.root, FC#11, port A2



# B1L102S, U12-ch34, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

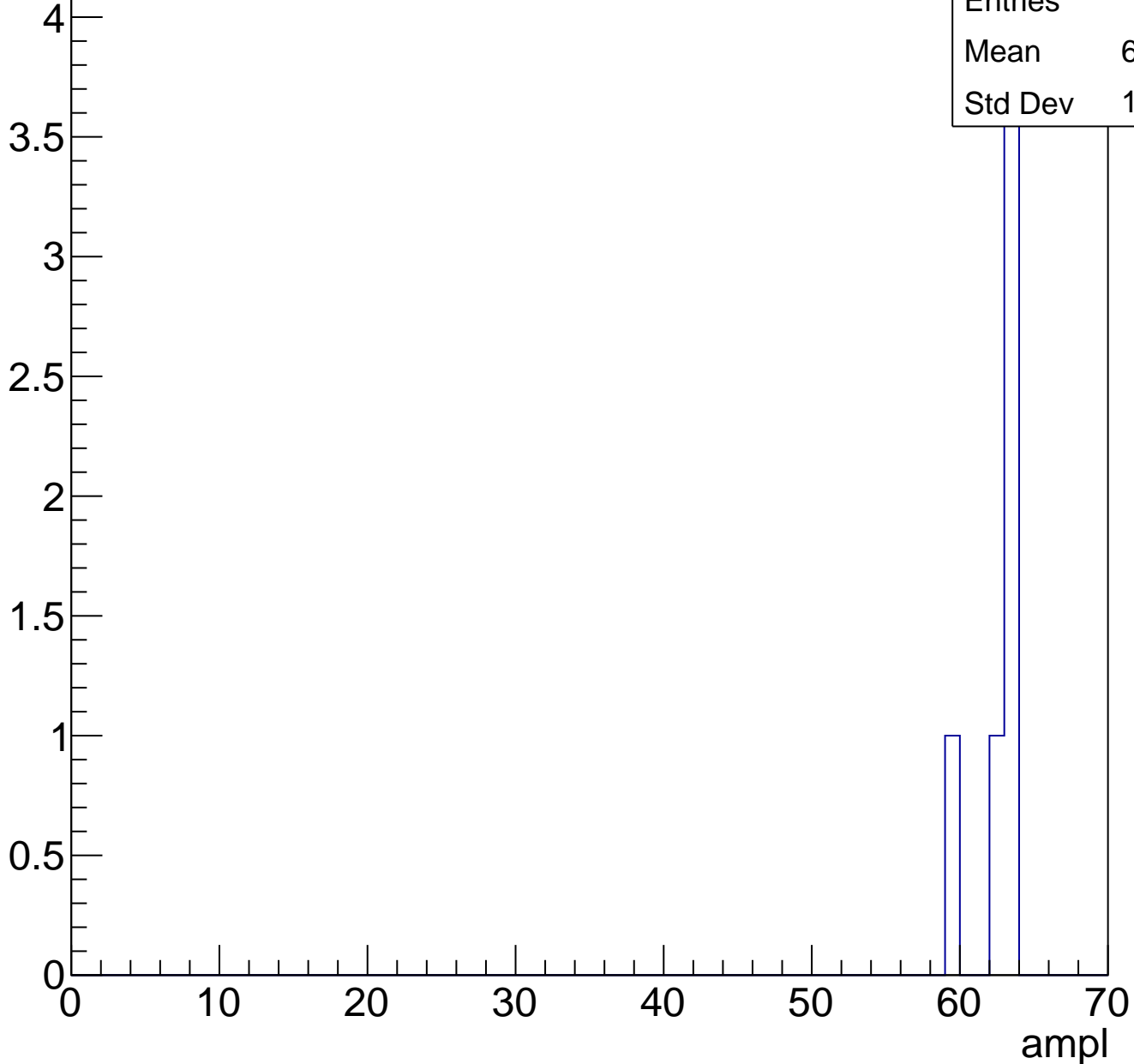
Entry



# B1L102S, U12-ch34, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	6
Mean	62.17
Std Dev	1.462



# B1L102S, U12-ch34, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

1  
0.8  
0.6  
0.4  
0.2  
0

Entries	1
Mean	23
Std Dev	0

ampl

# B1L102S, U12-ch35, adc0

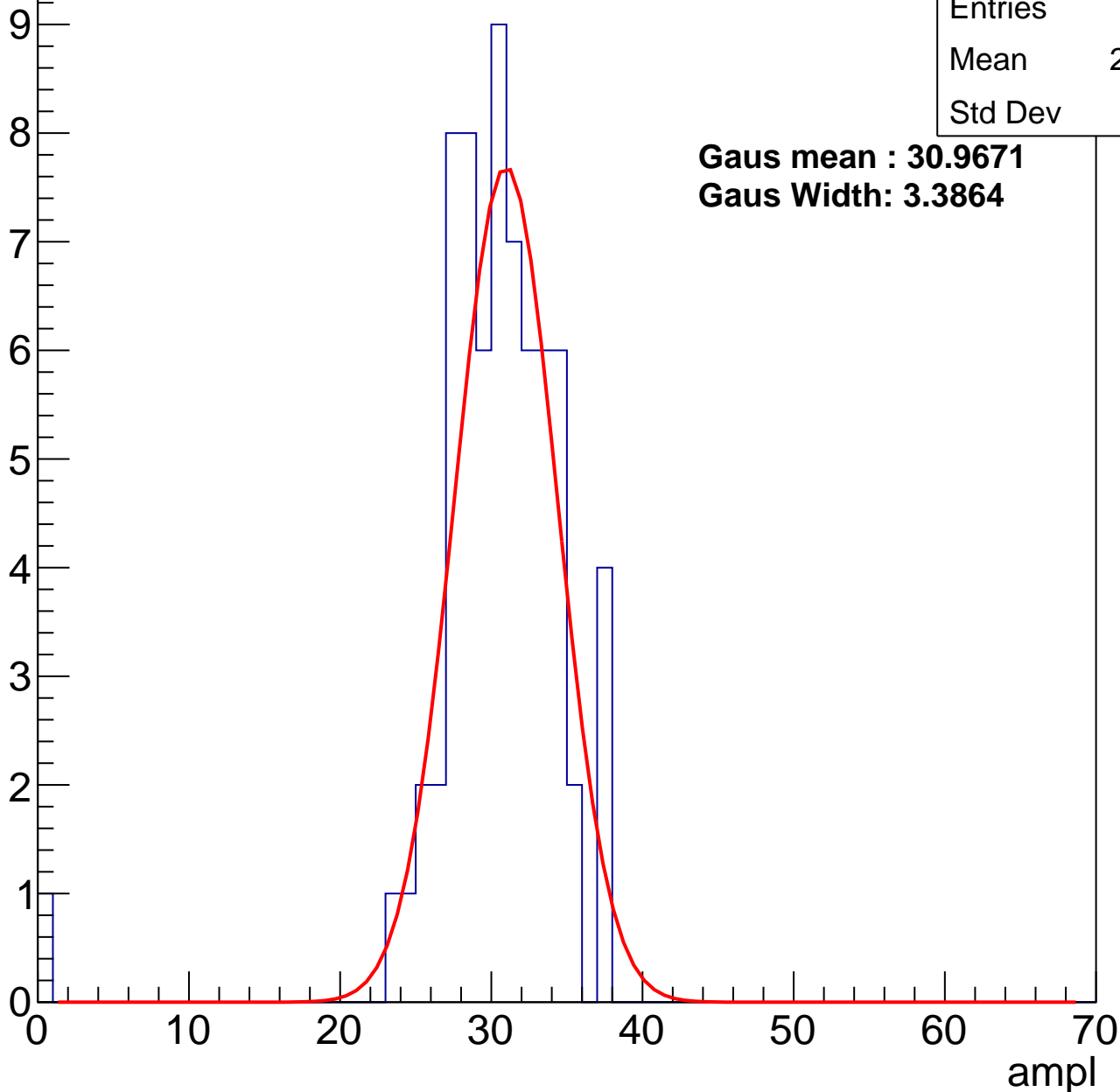
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	29.88
Std Dev	4.82

**Gaus mean : 30.9671**

**Gaus Width: 3.3864**



# B1L102S, U12-ch35, adc1

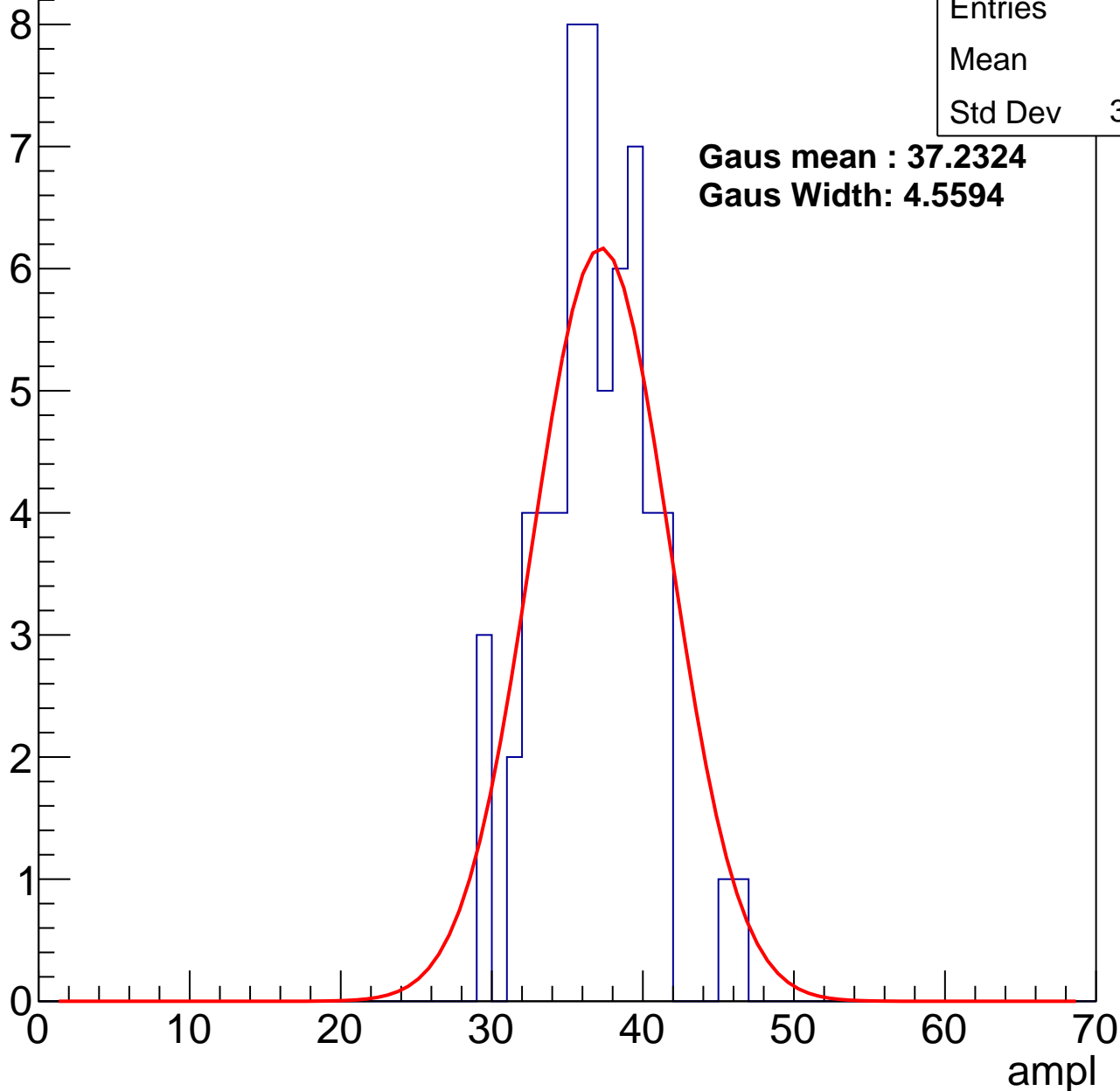
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	36.3
Std Dev	3.513

**Gaus mean : 37.2324**

**Gaus Width: 4.5594**



# B1L102S, U12-ch35, adc2

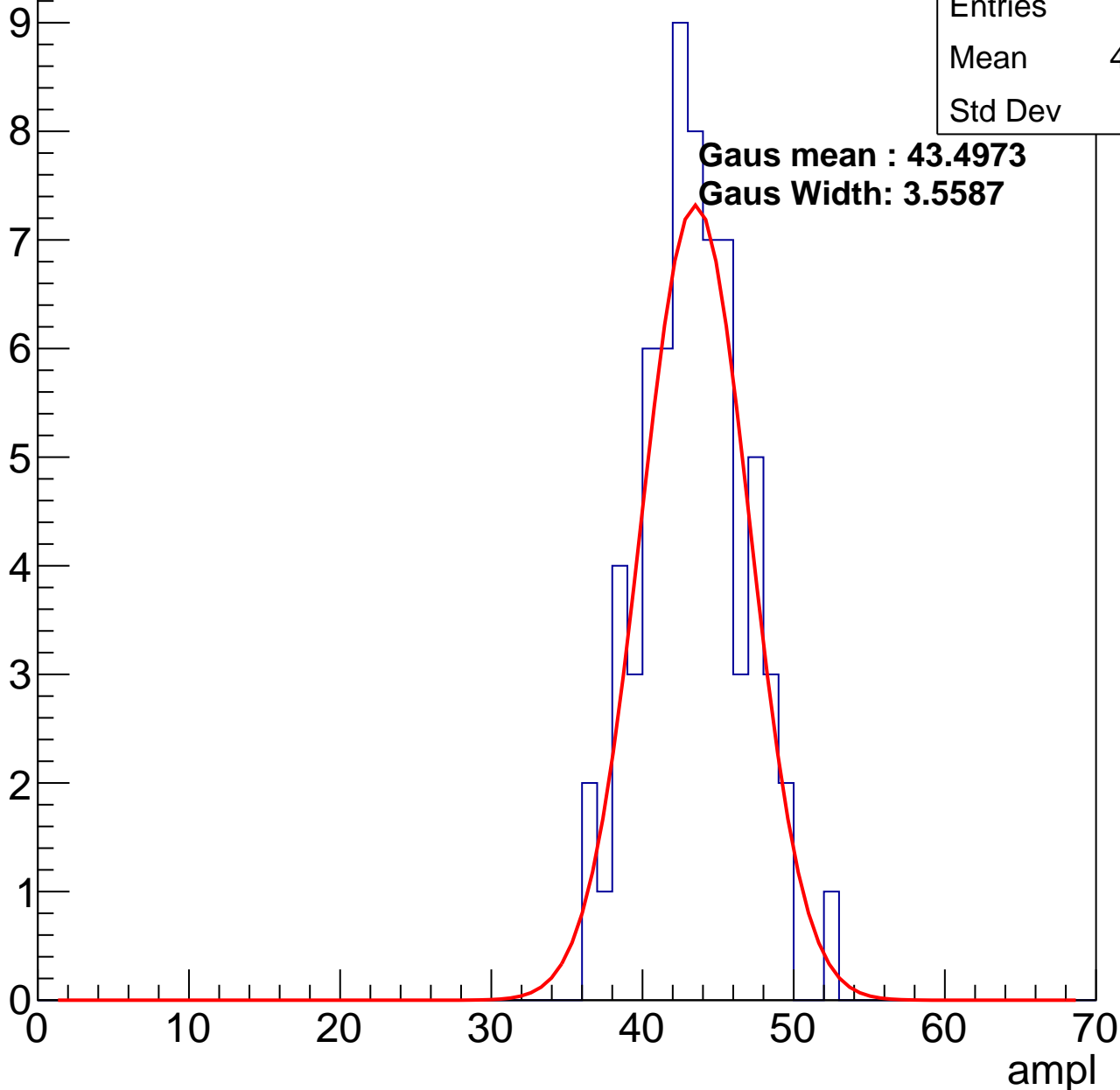
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	67
Mean	42.93
Std Dev	3.32

**Gaus mean : 43.4973**

**Gaus Width: 3.5587**

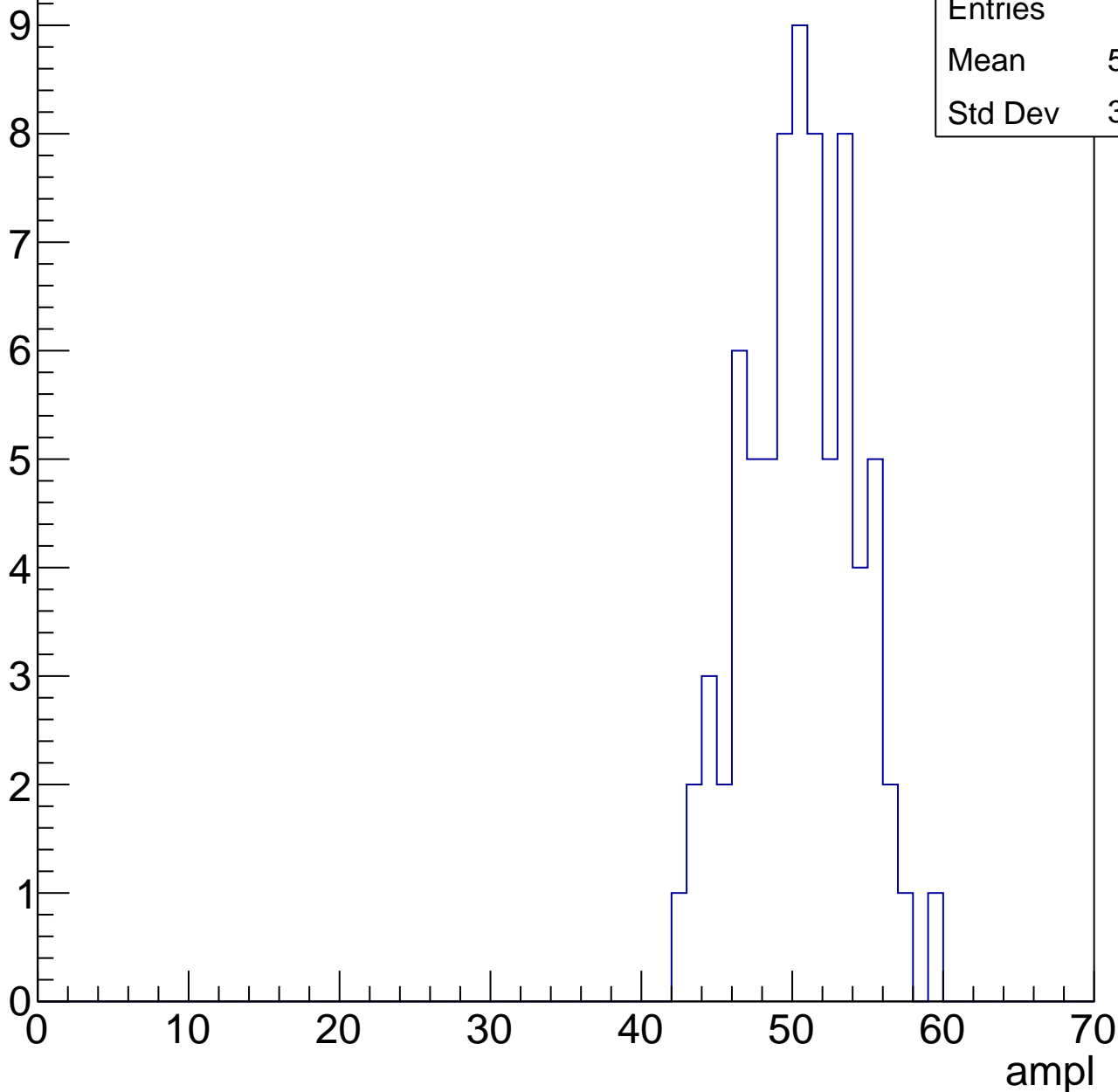


# B1L102S, U12-ch35, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

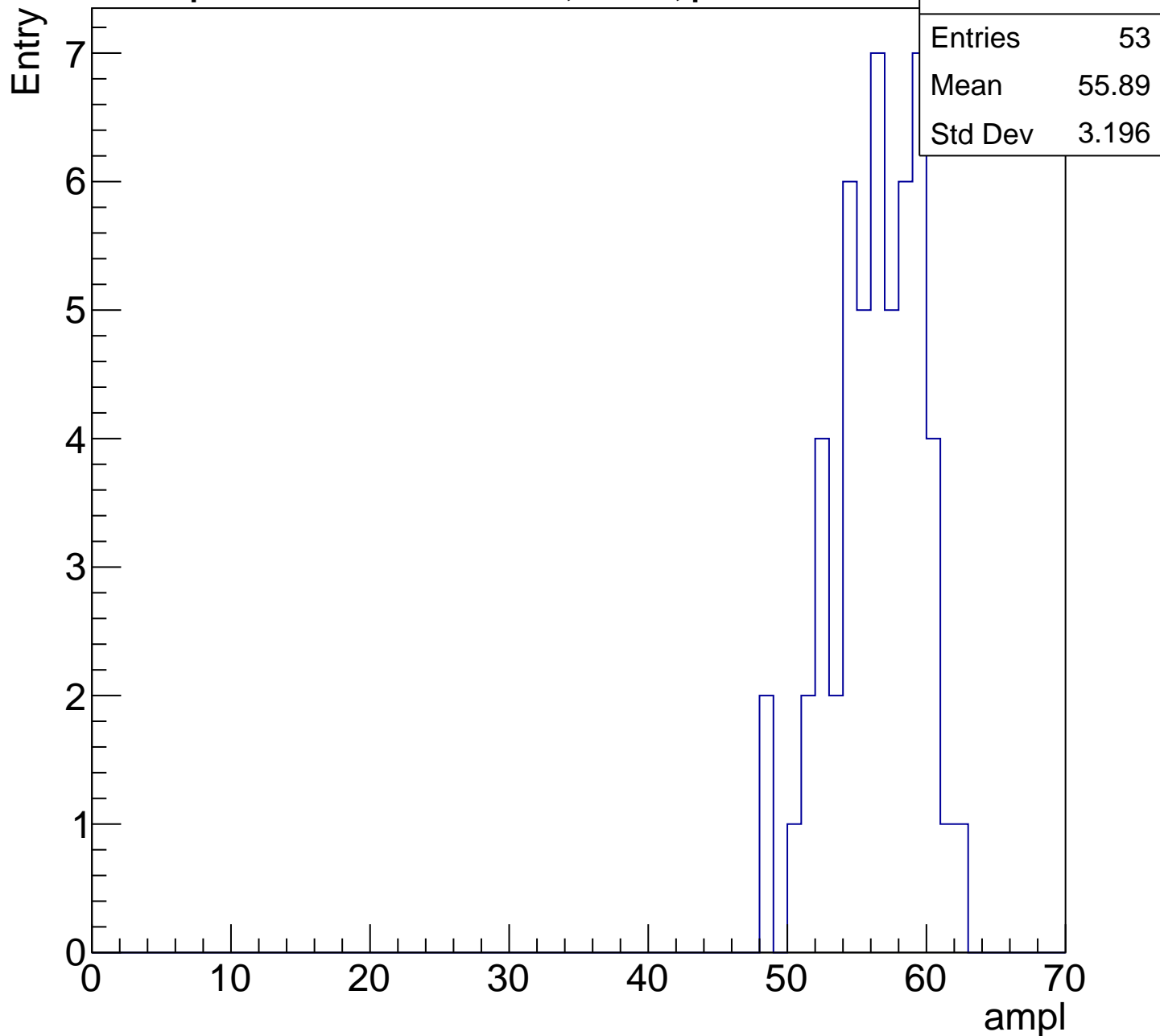
Entry

Entries	75
Mean	50.05
Std Dev	3.614



# B1L102S, U12-ch35, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2



# B1L102S, U12-ch35, adc5

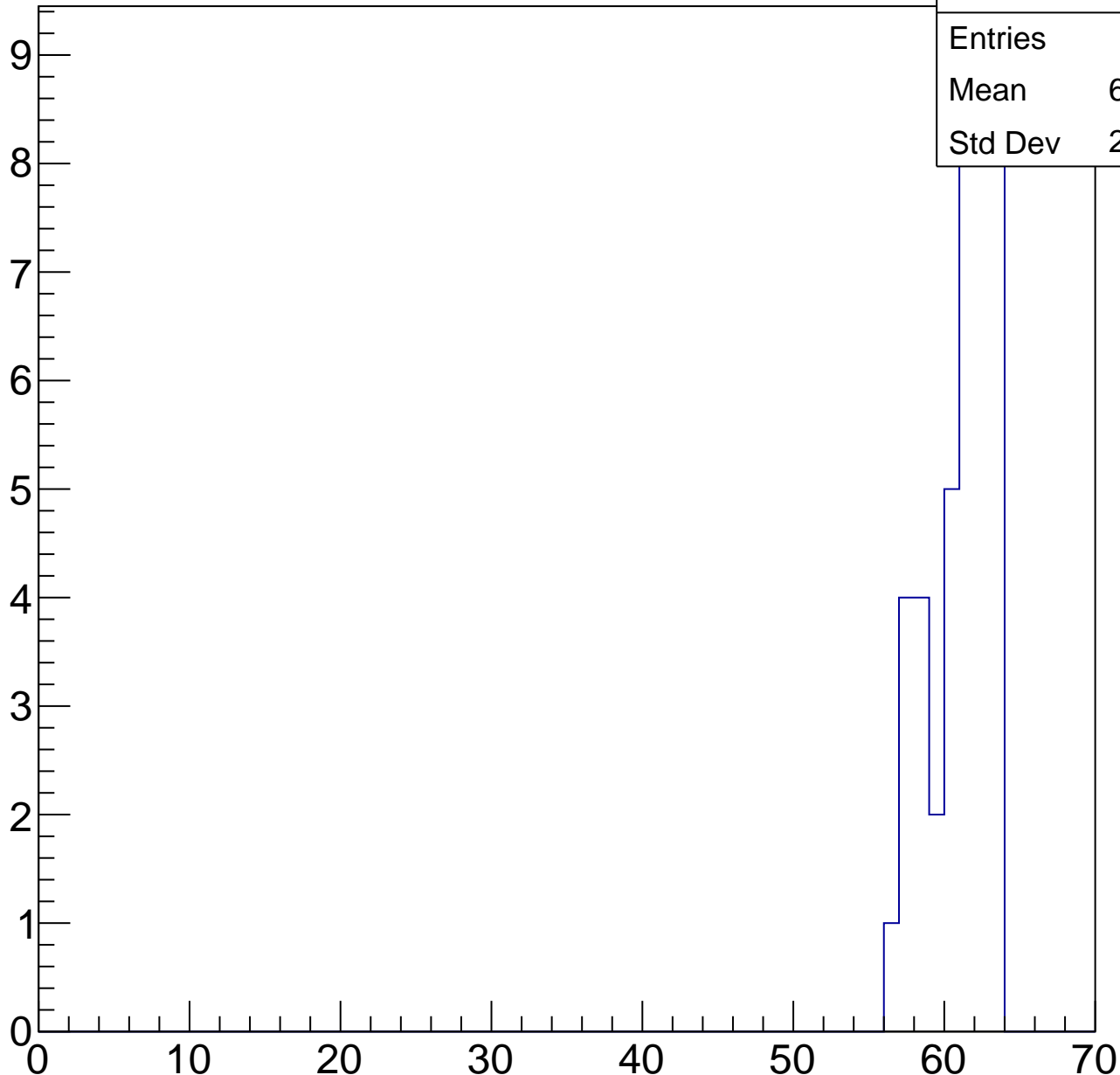
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	41
Mean	60.59
Std Dev	2.048

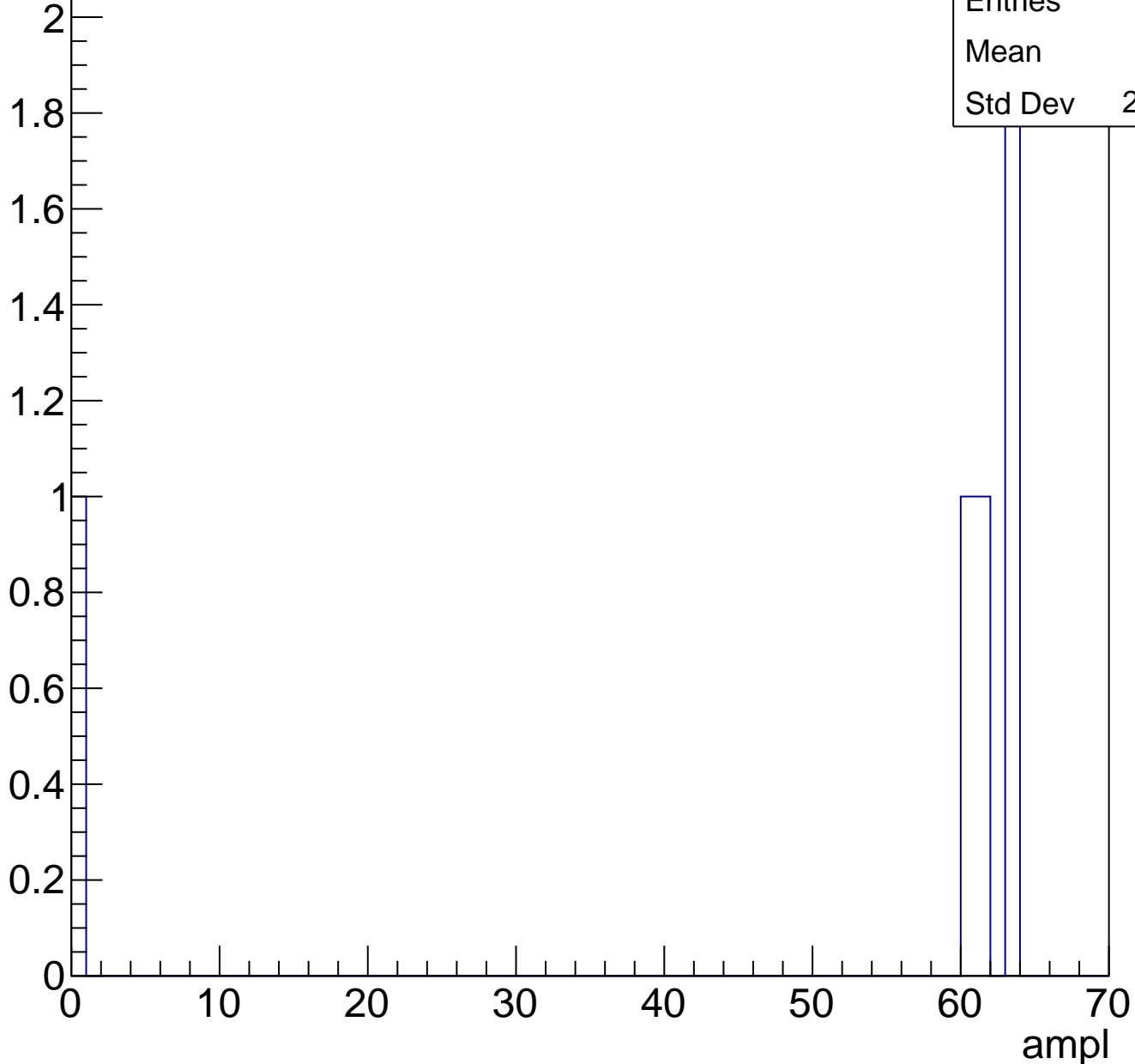
ampl



# B1L102S, U12-ch35, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U12-ch35, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U12-ch36, adc0

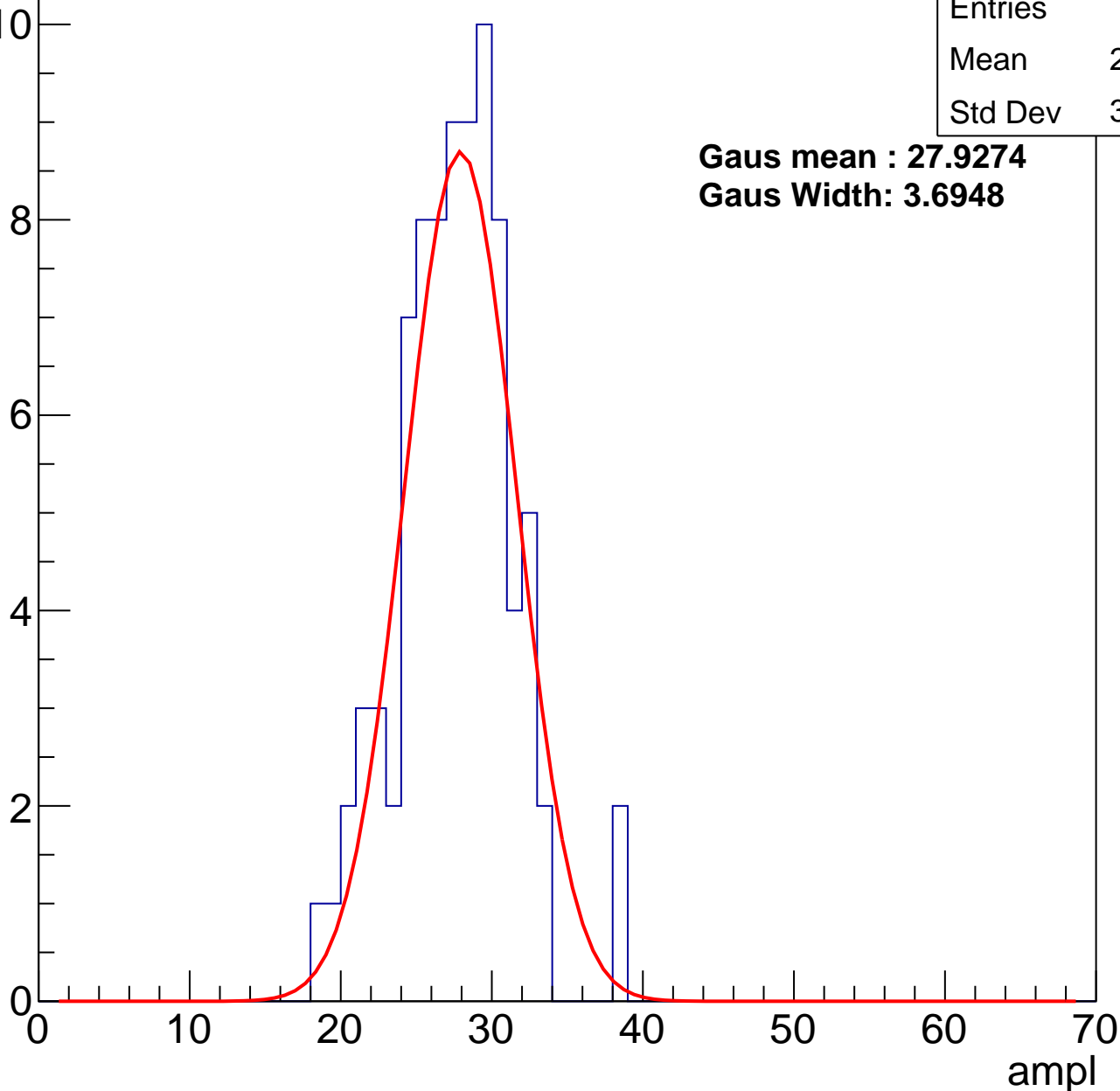
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	84
Mean	27.13
Std Dev	3.754

**Gaus mean : 27.9274**

**Gaus Width: 3.6948**



# B1L102S, U12-ch36, adc1

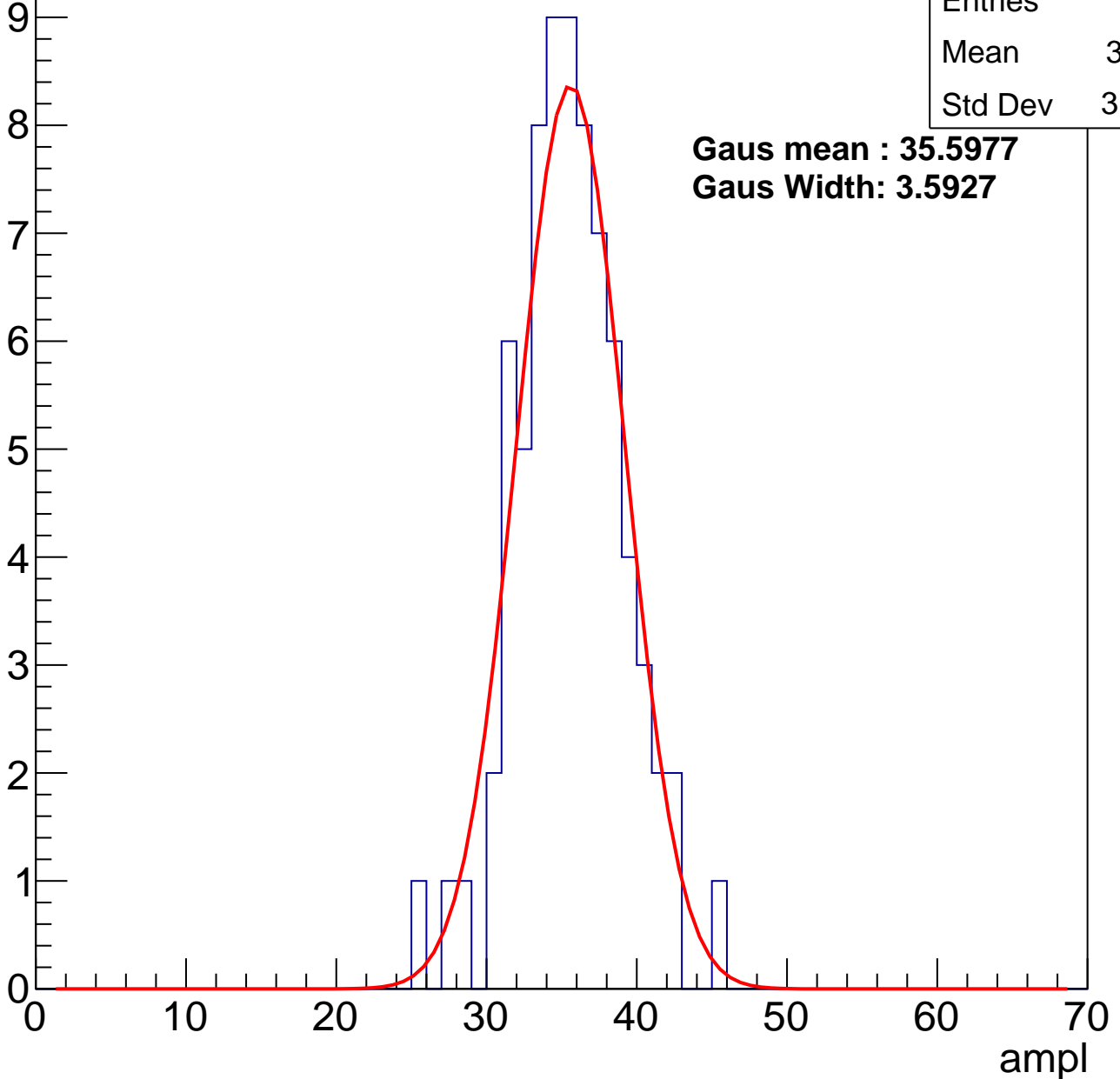
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	75
Mean	35.11
Std Dev	3.546

**Gaus mean : 35.5977**

**Gaus Width: 3.5927**



# B1L102S, U12-ch36, adc2

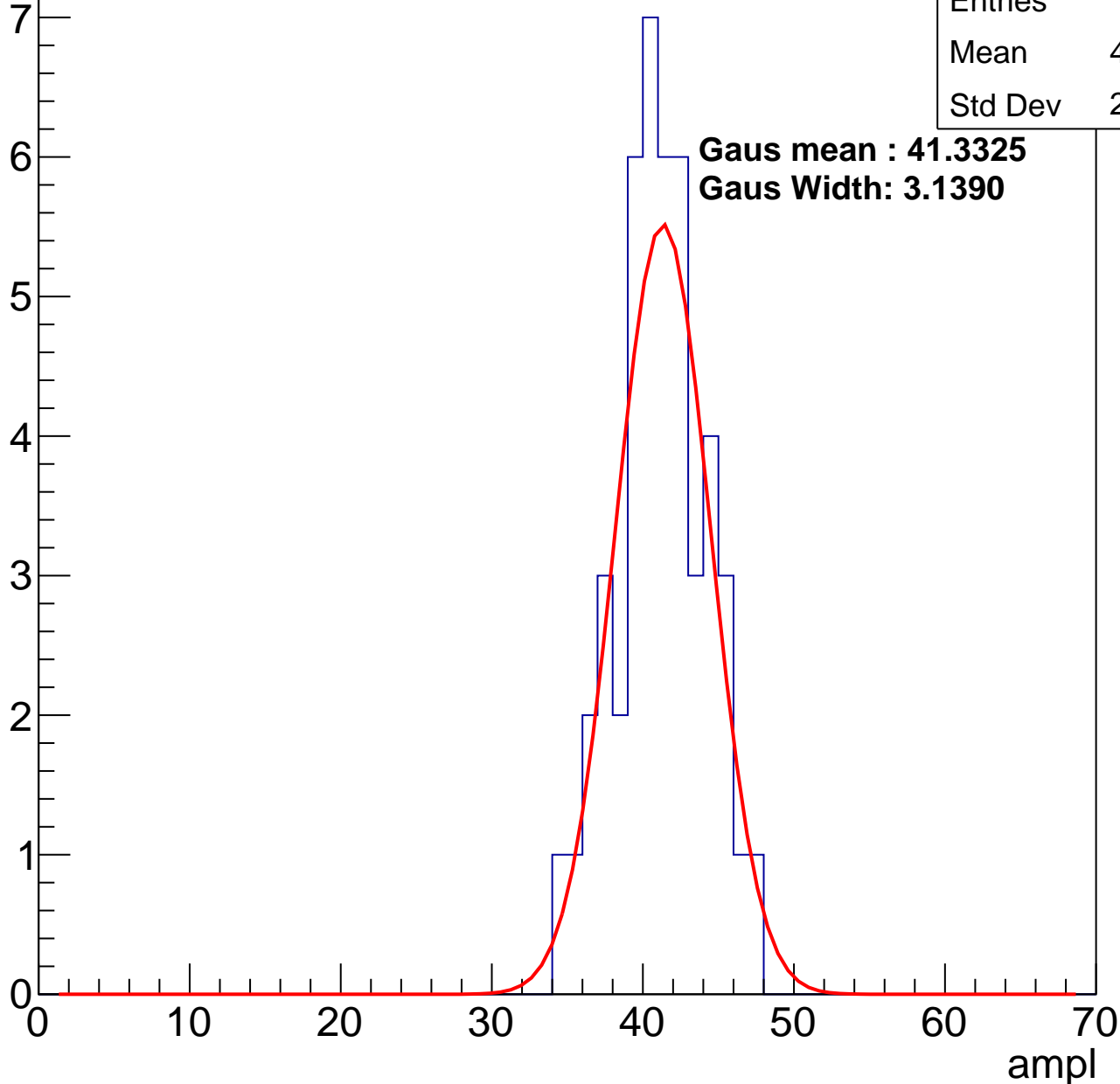
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	46
Mean	40.72
Std Dev	2.917

**Gaus mean : 41.3325**

**Gaus Width: 3.1390**

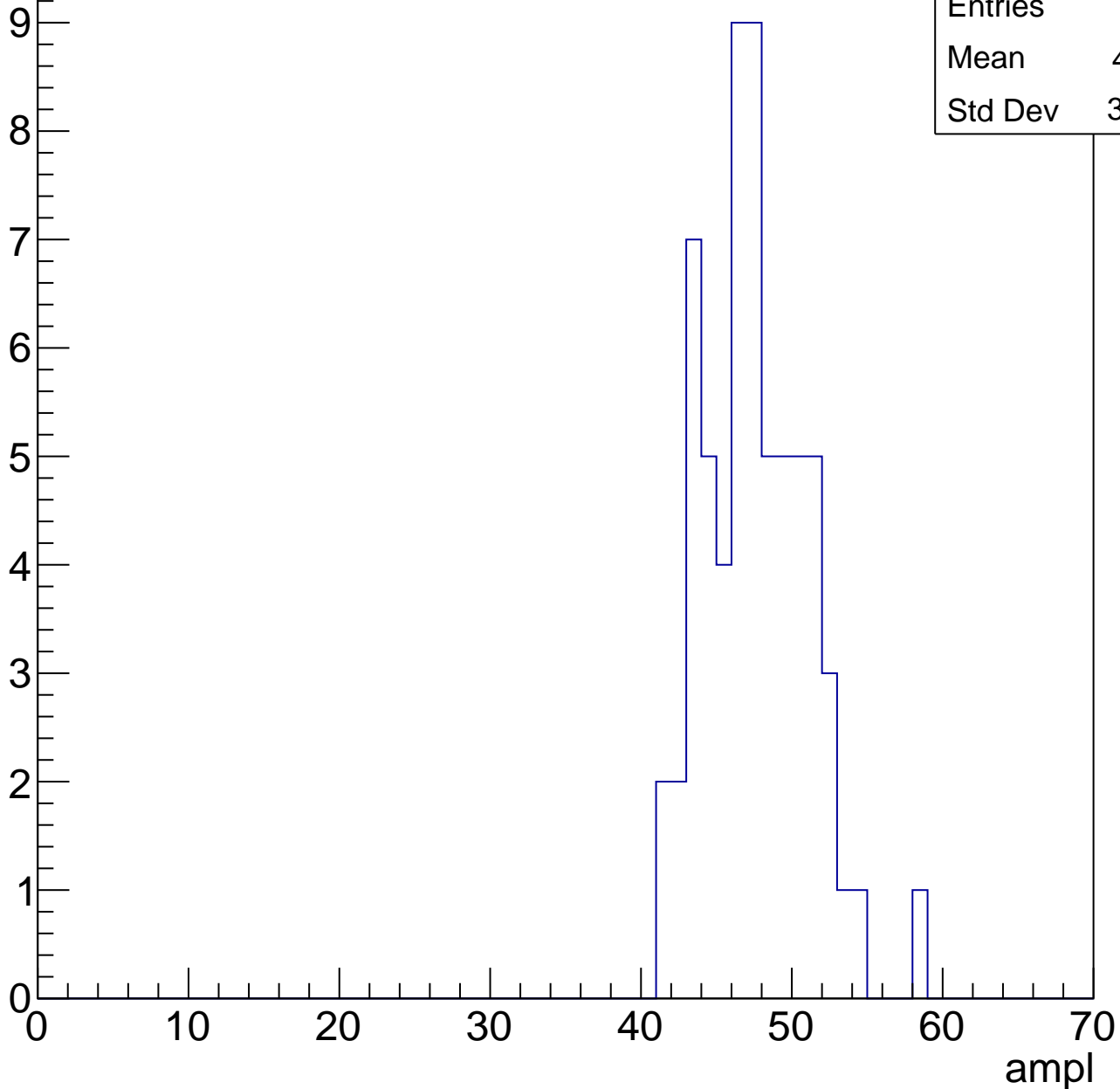


# B1L102S, U12-ch36, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	47.11
Std Dev	3.387

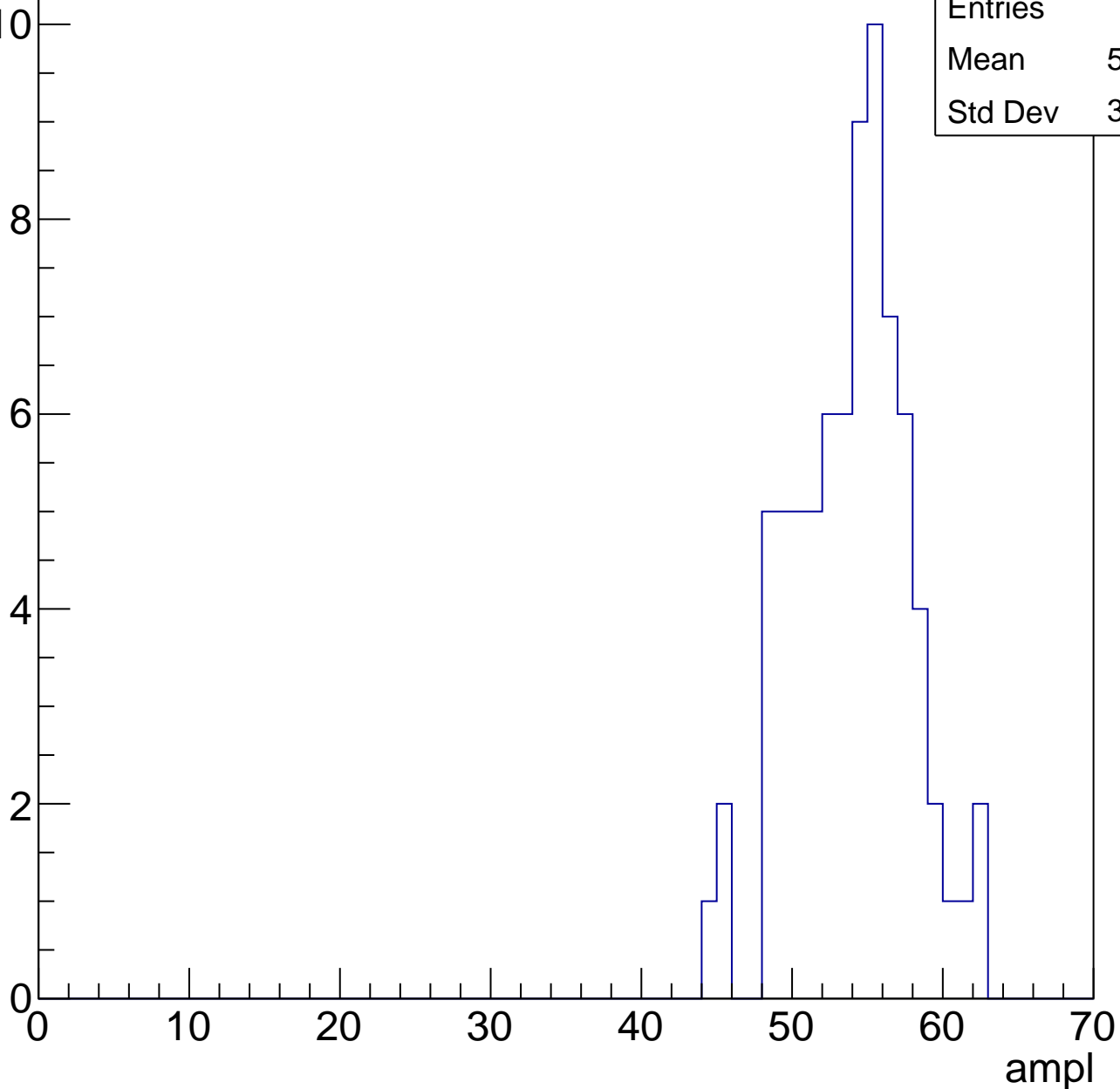


# B1L102S, U12-ch36, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	77
Mean	53.49
Std Dev	3.816



# B1L102S, U12-ch36, adc5

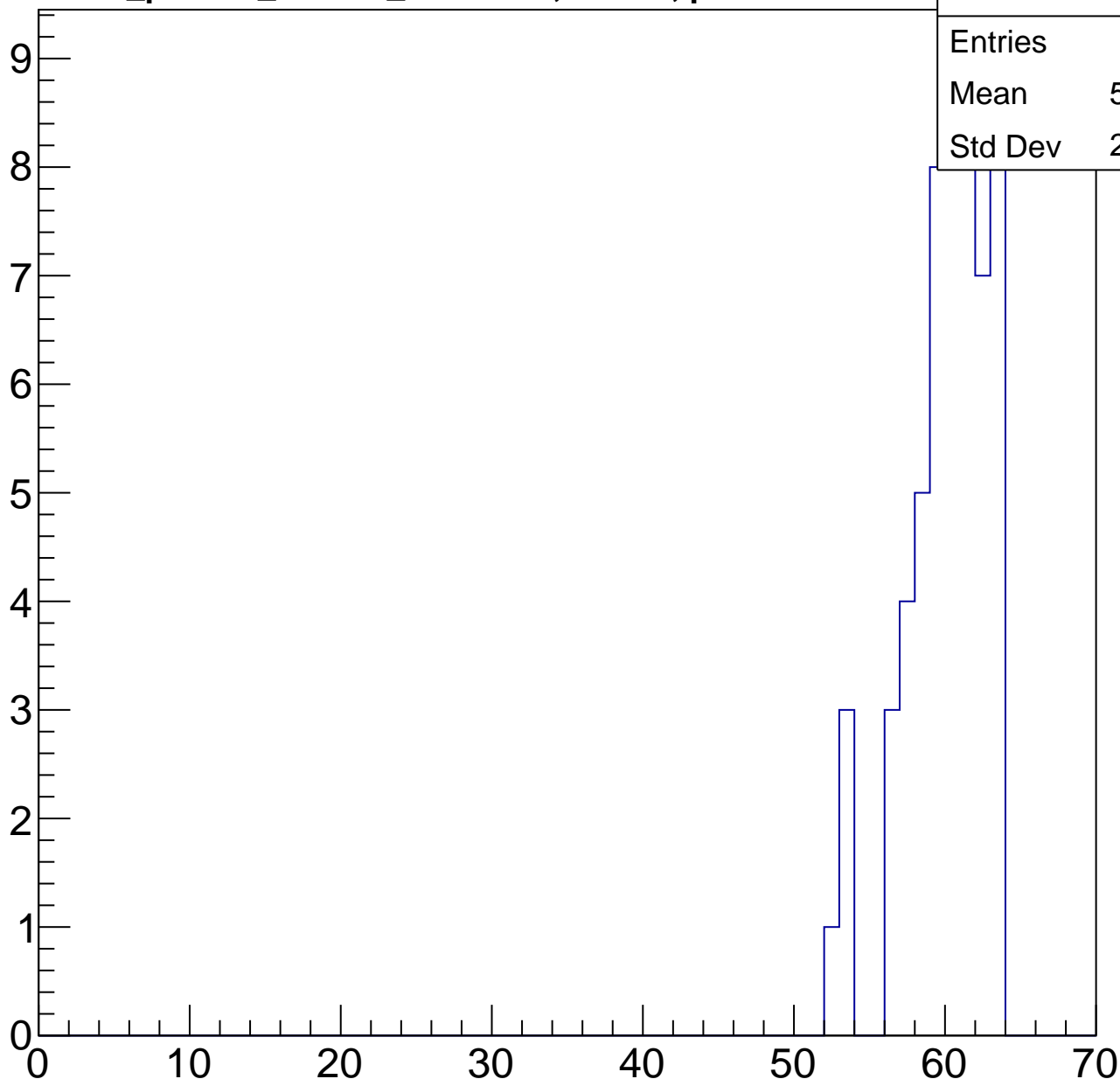
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	56
Mean	59.55
Std Dev	2.738

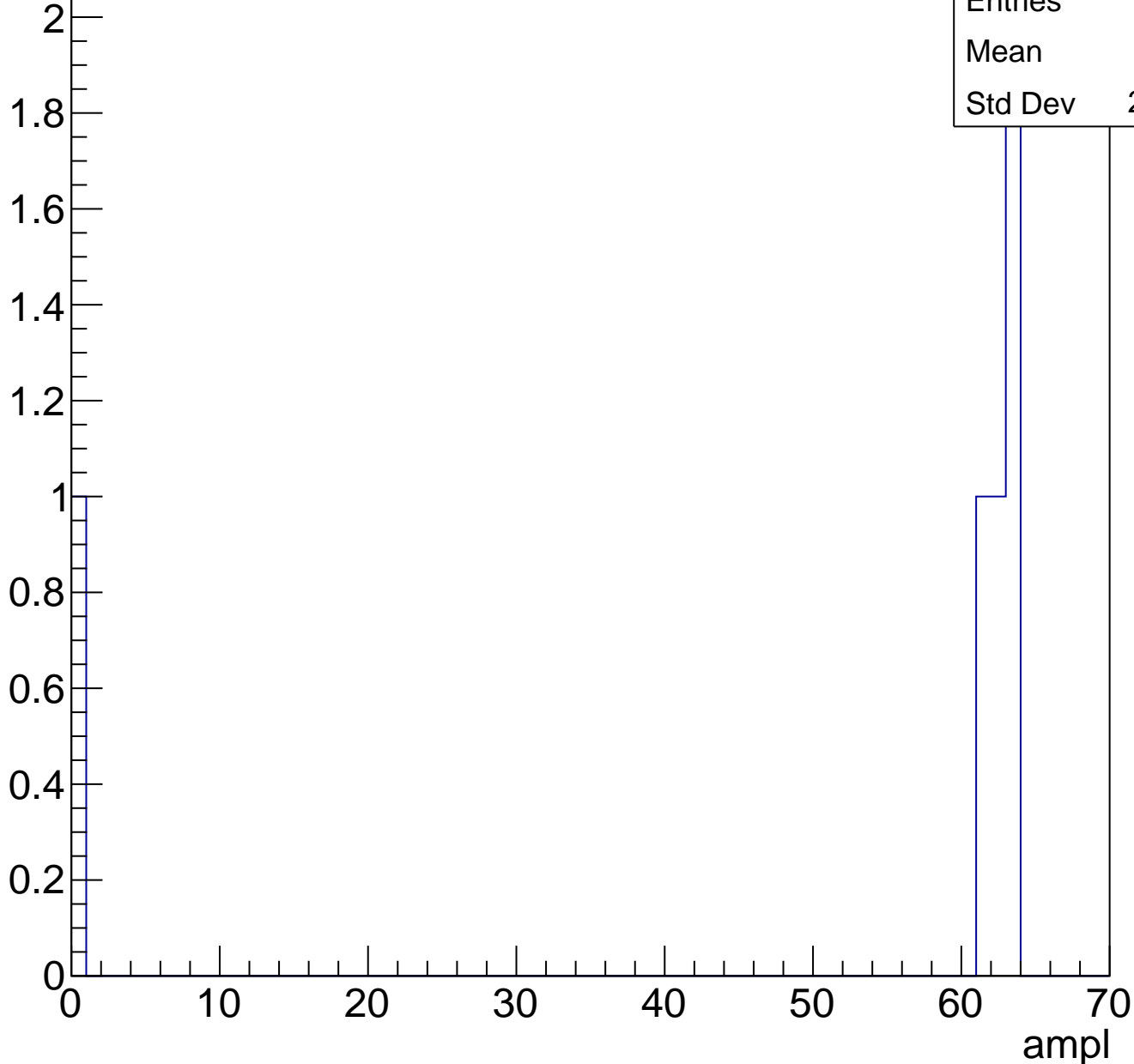
ampl



# B1L102S, U12-ch36, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U12-ch36, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U12-ch37, adc0

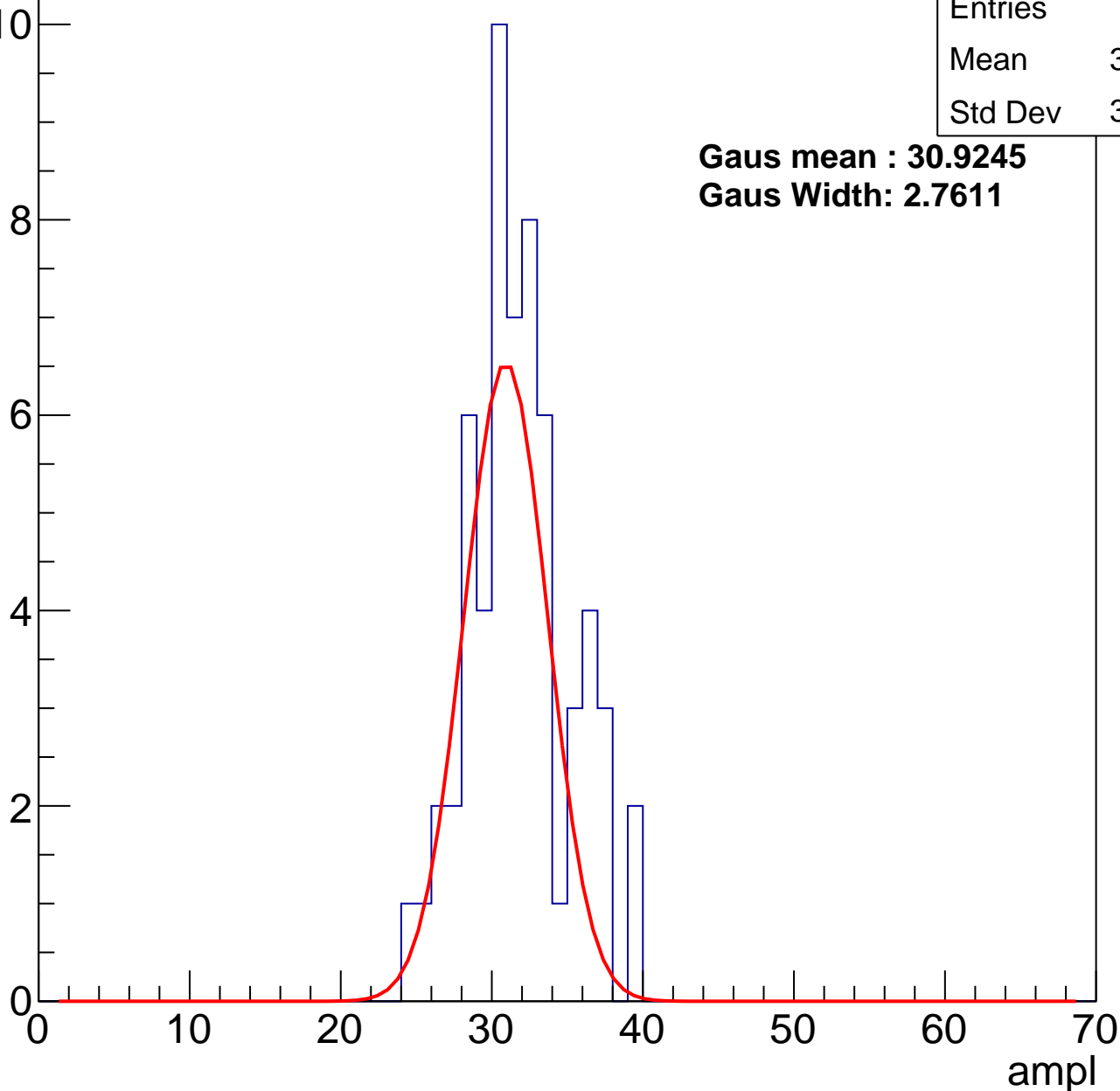
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	60
Mean	31.37
Std Dev	3.326

**Gaus mean : 30.9245**

**Gaus Width: 2.7611**



# B1L102S, U12-ch37, adc1

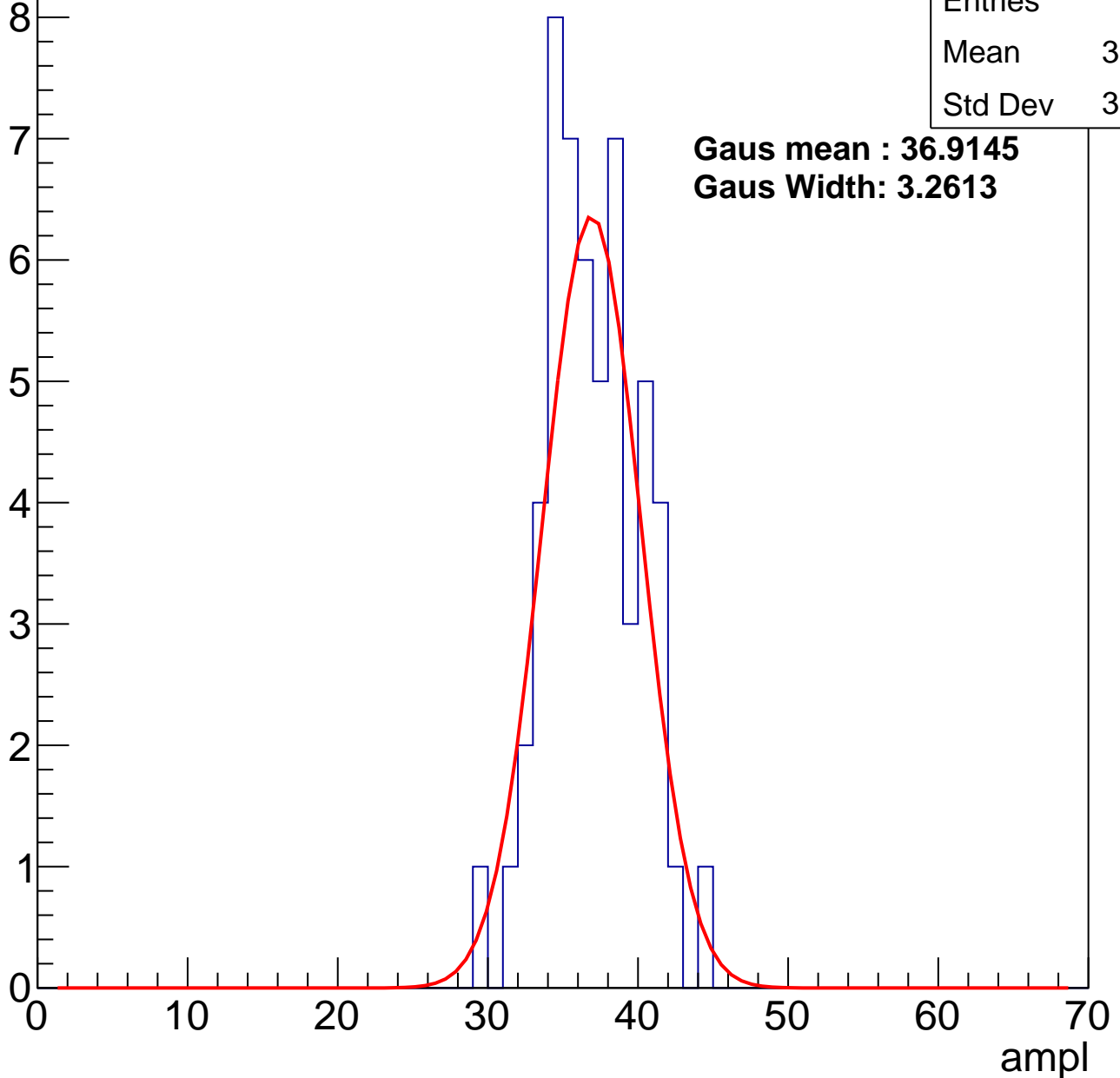
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	55
Mean	36.49
Std Dev	3.038

**Gaus mean : 36.9145**

**Gaus Width: 3.2613**



# B1L102S, U12-ch37, adc2

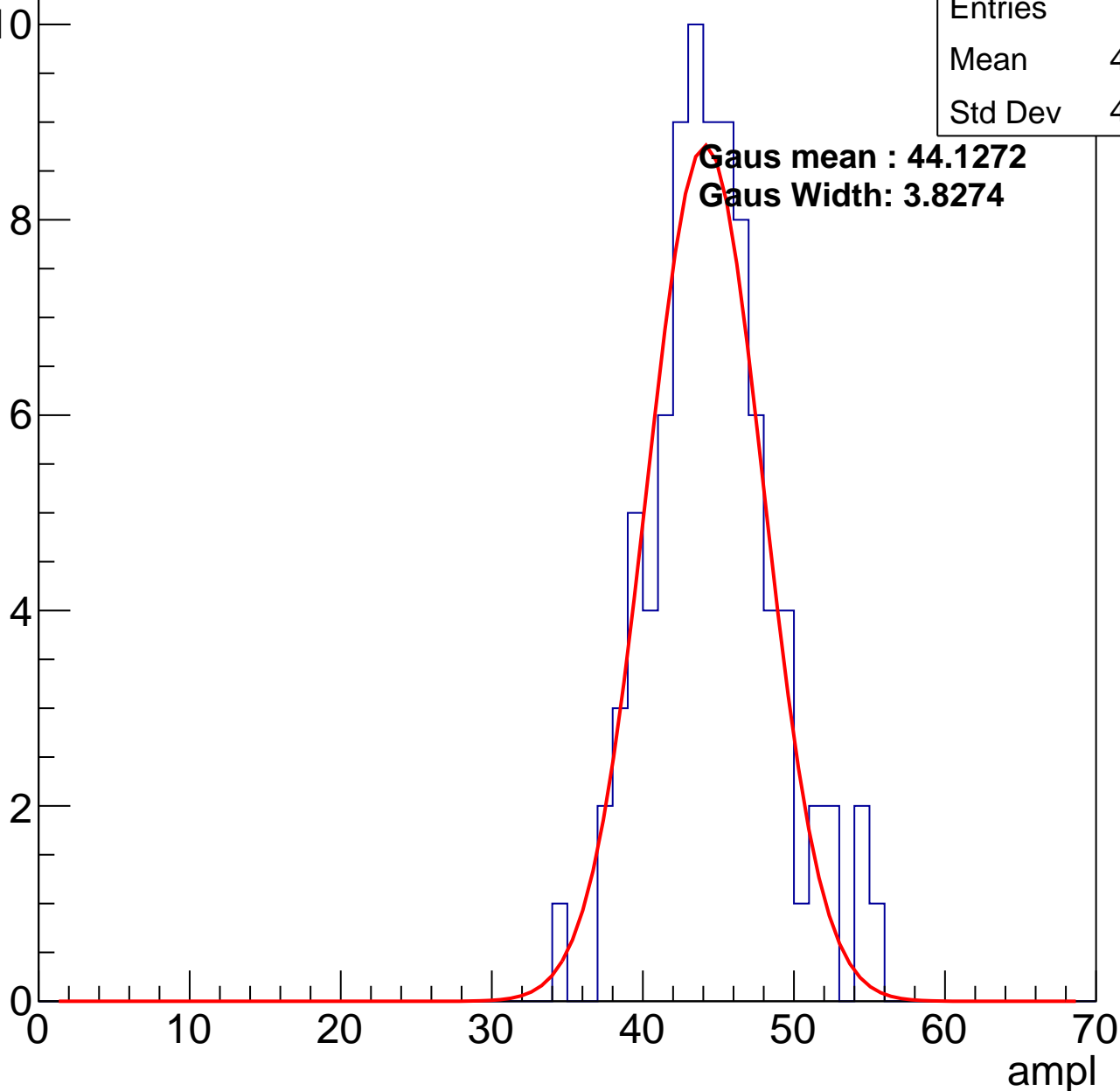
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	88
Mean	44.19
Std Dev	4.036

**Gaus mean : 44.1272**

**Gaus Width: 3.8274**

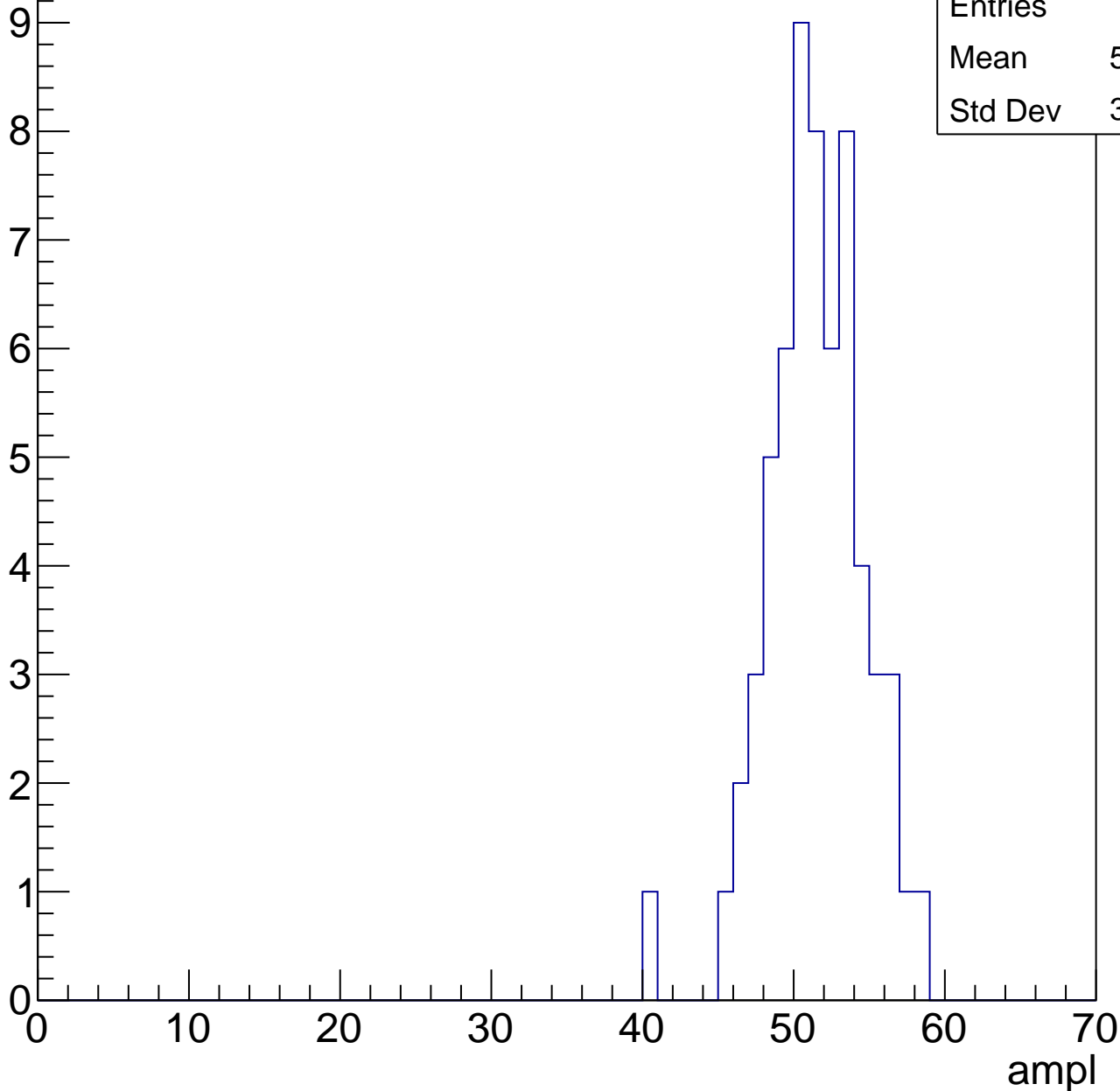


# B1L102S, U12-ch37, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	50.98
Std Dev	3.175

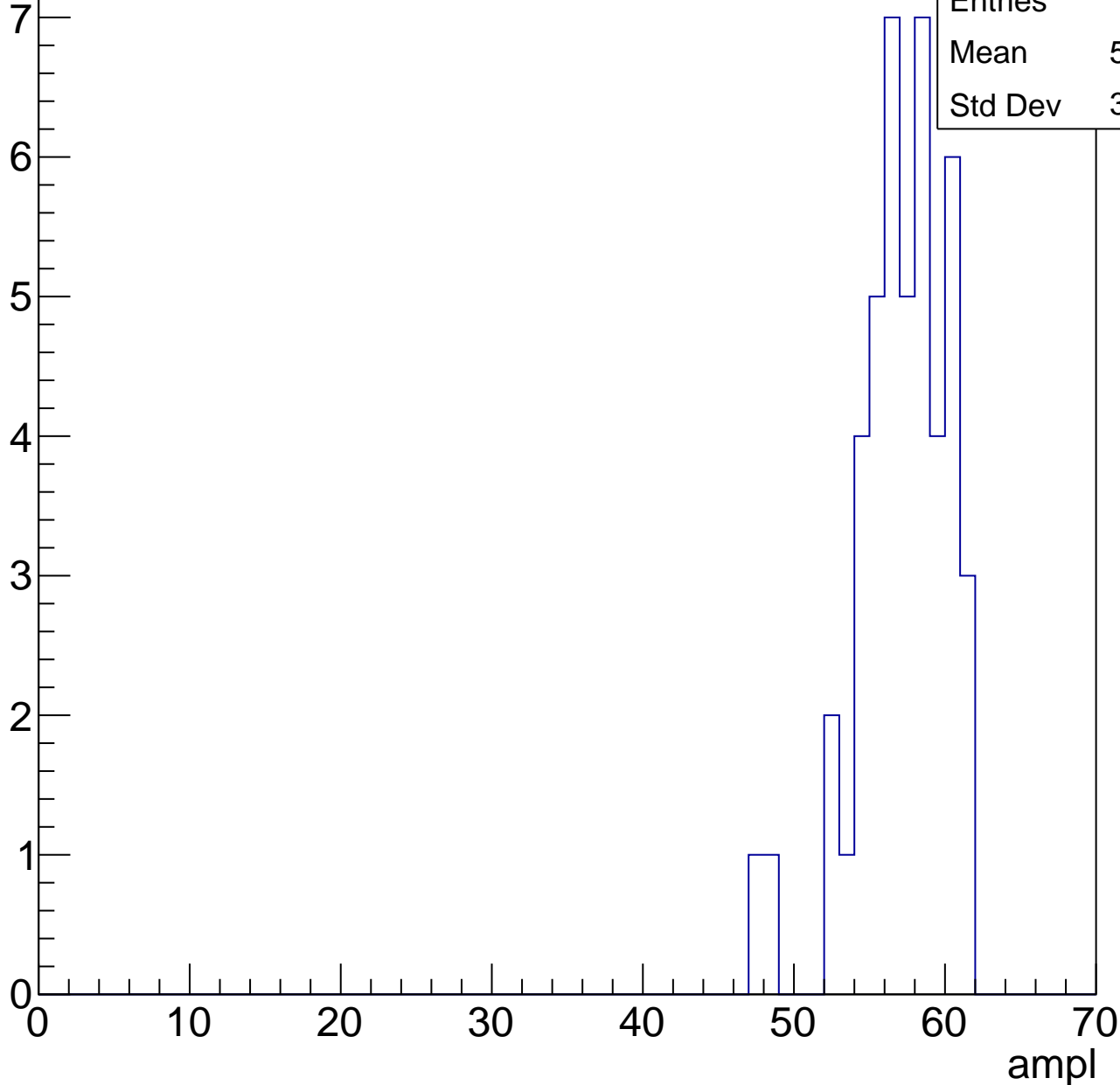


# B1L102S, U12-ch37, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	46
Mean	56.63
Std Dev	3.053

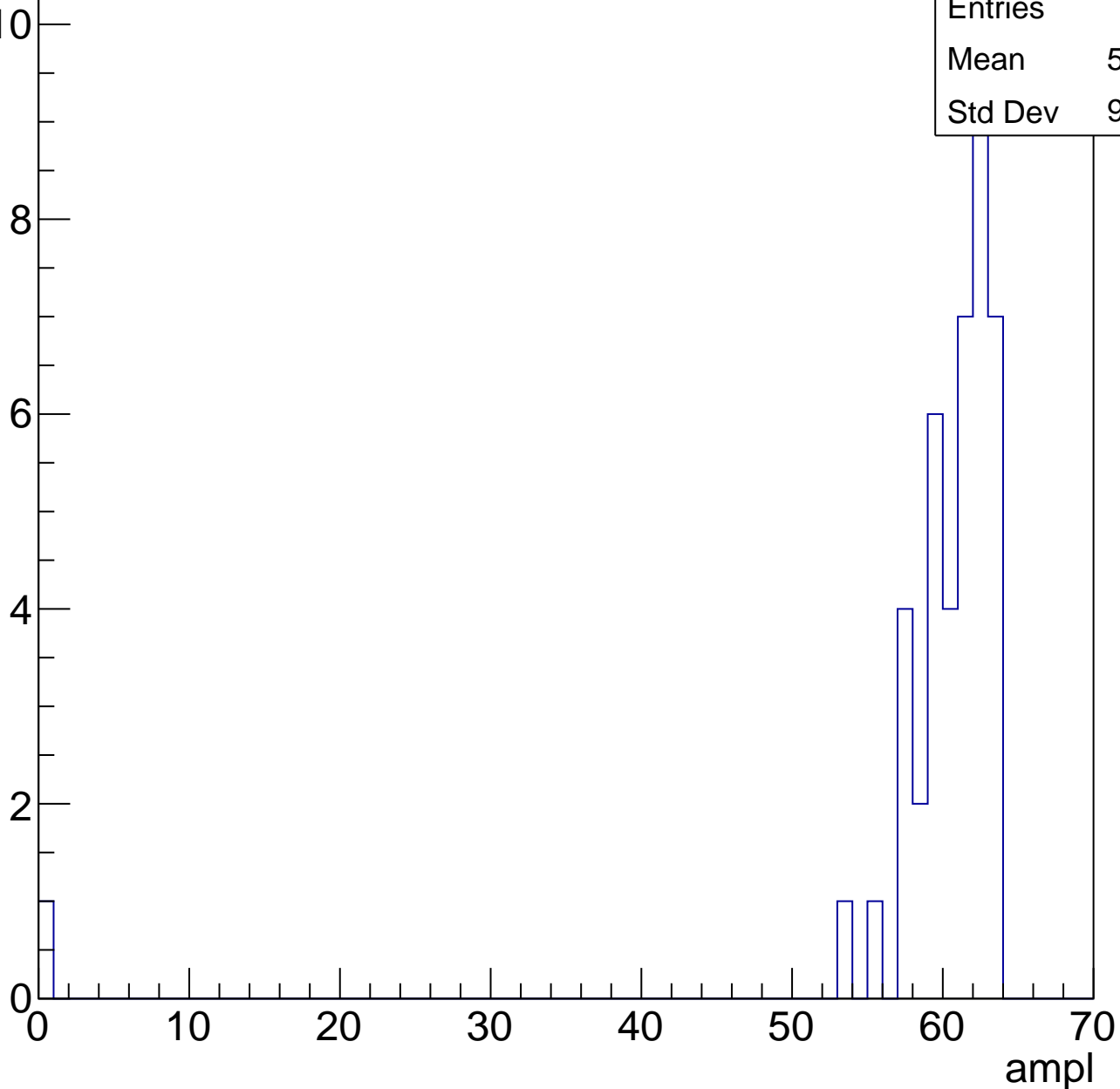


# B1L102S, U12-ch37, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	43
Mean	58.93
Std Dev	9.382



# B1L102S, U12-ch37, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U12-ch37, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U12-ch38, adc0

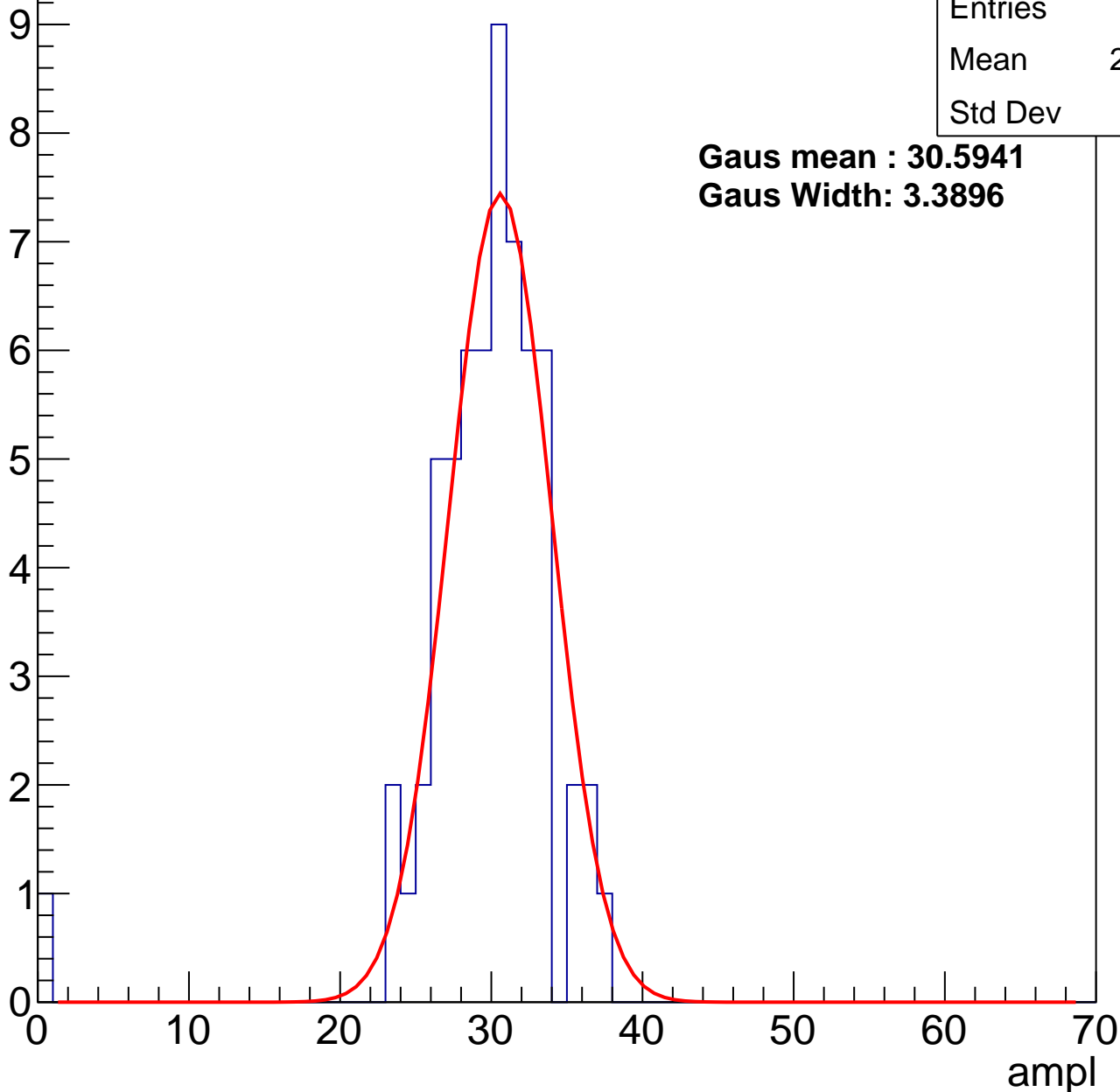
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	29.23
Std Dev	4.89

**Gaus mean : 30.5941**

**Gaus Width: 3.3896**



# B1L102S, U12-ch38, adc1

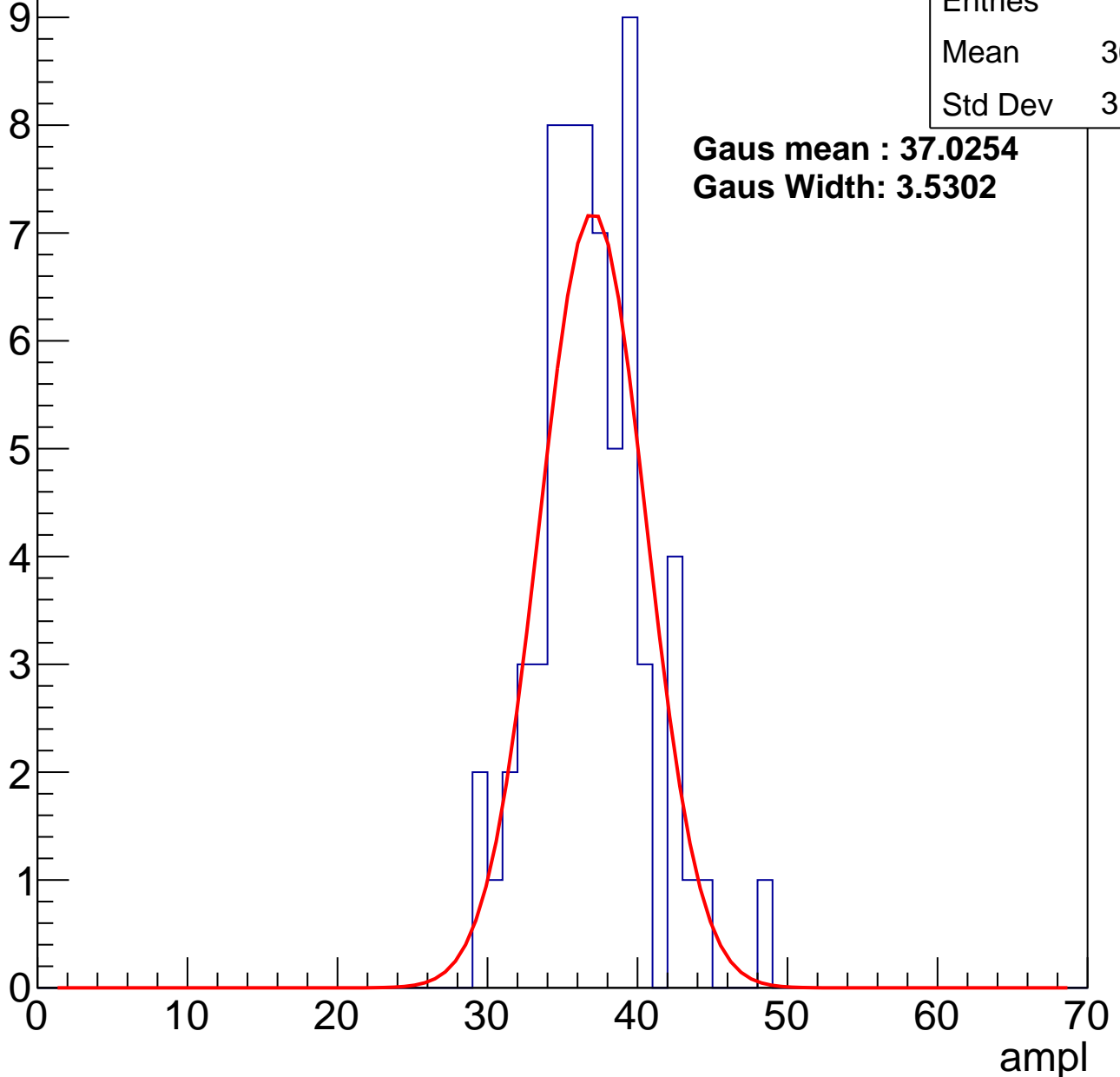
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	36.48
Std Dev	3.569

**Gaus mean : 37.0254**

**Gaus Width: 3.5302**



# B1L102S, U12-ch38, adc2

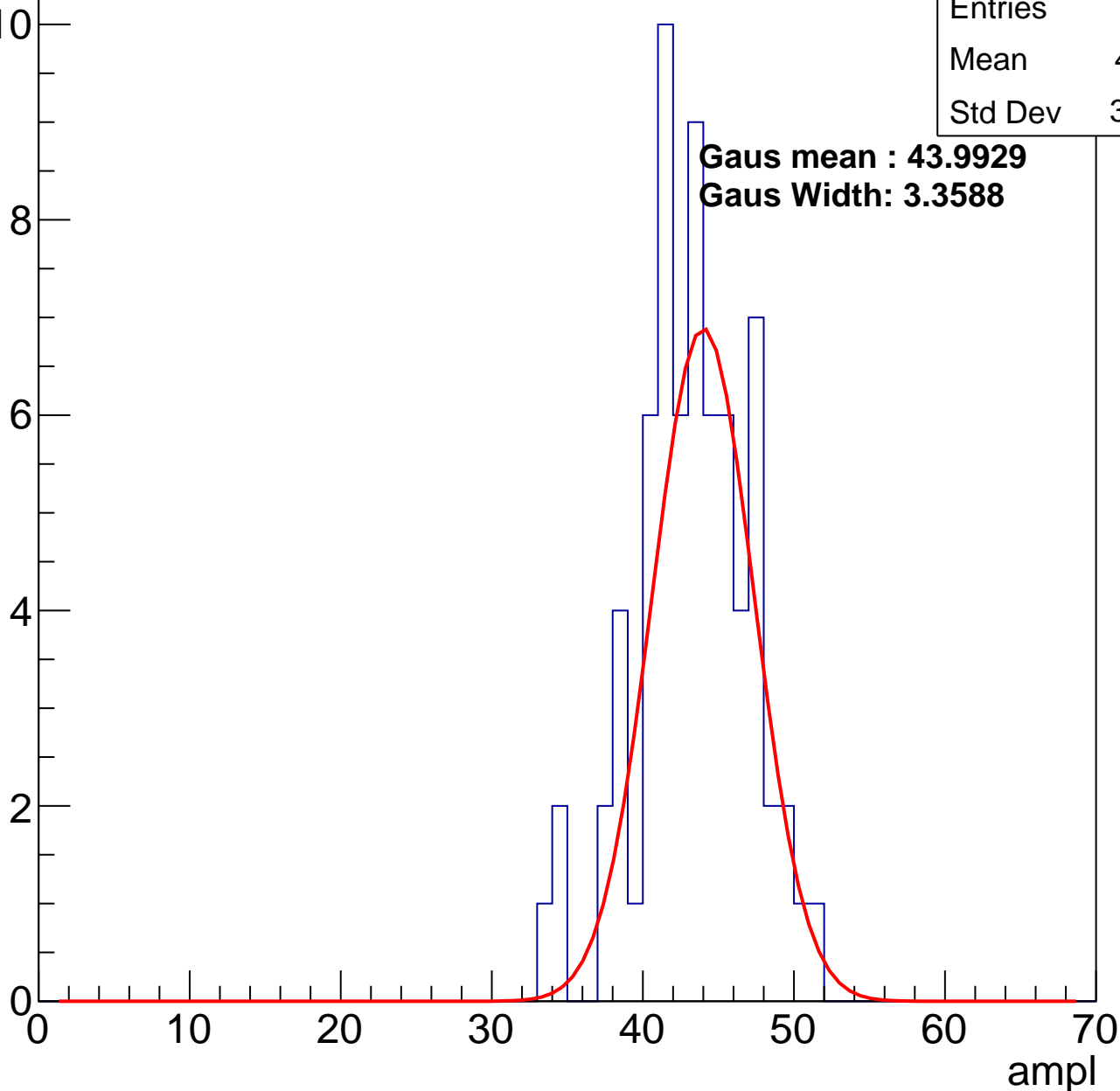
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	70
Mean	42.81
Std Dev	3.704

**Gaus mean : 43.9929**

**Gaus Width: 3.3588**

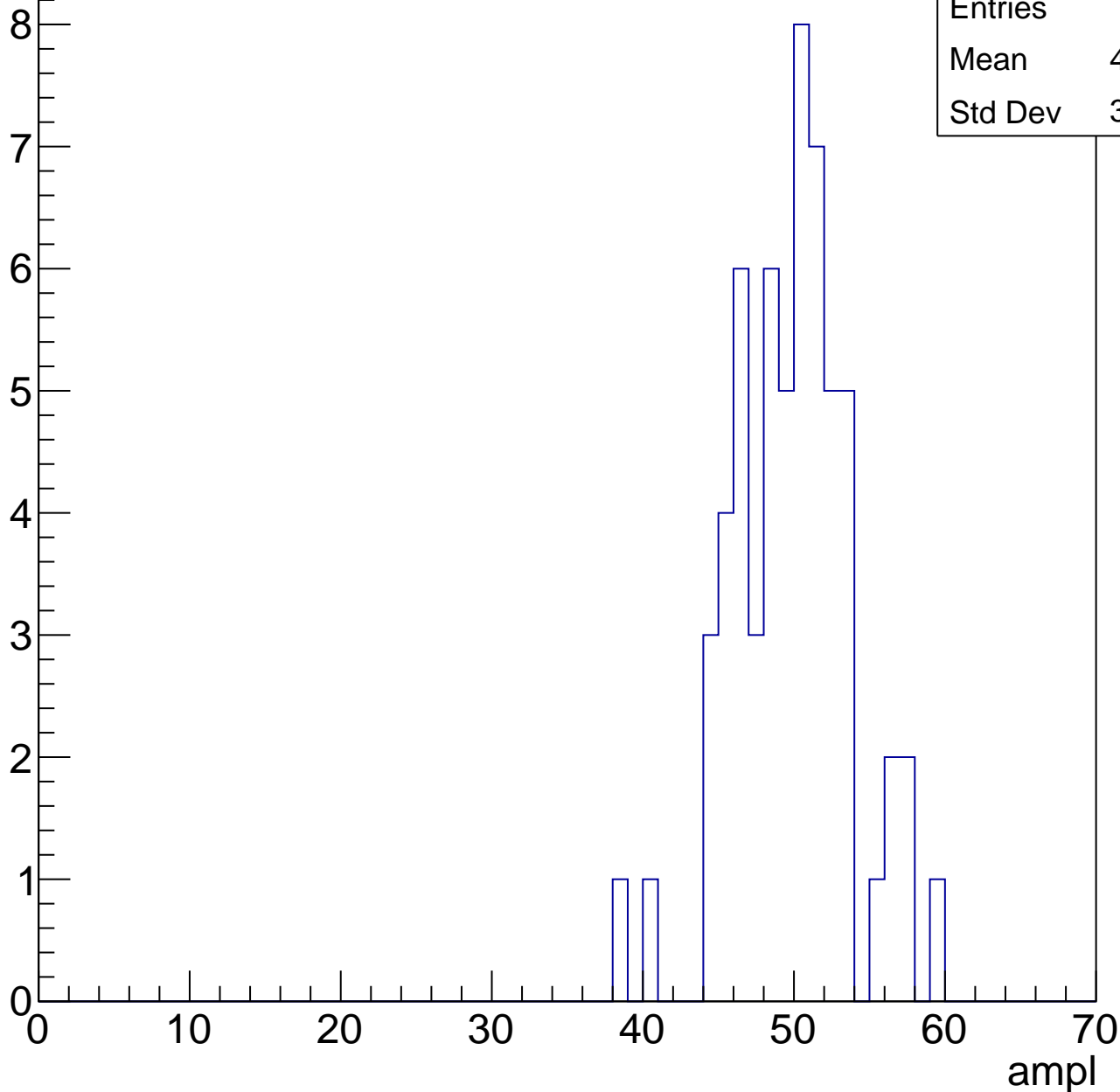


# B1L102S, U12-ch38, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	60
Mean	49.37
Std Dev	3.933

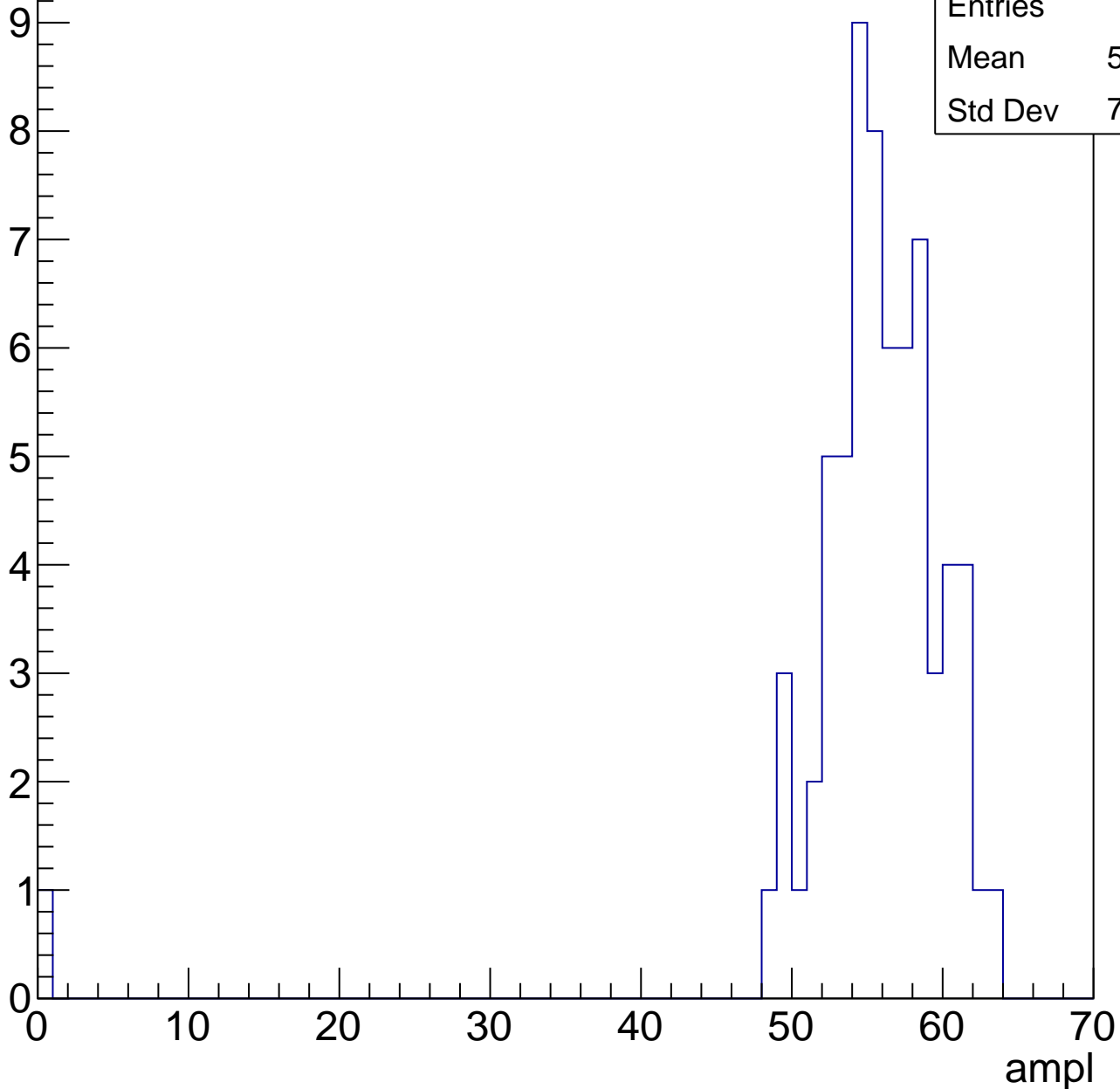


# B1L102S, U12-ch38, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	67
Mean	54.75
Std Dev	7.538

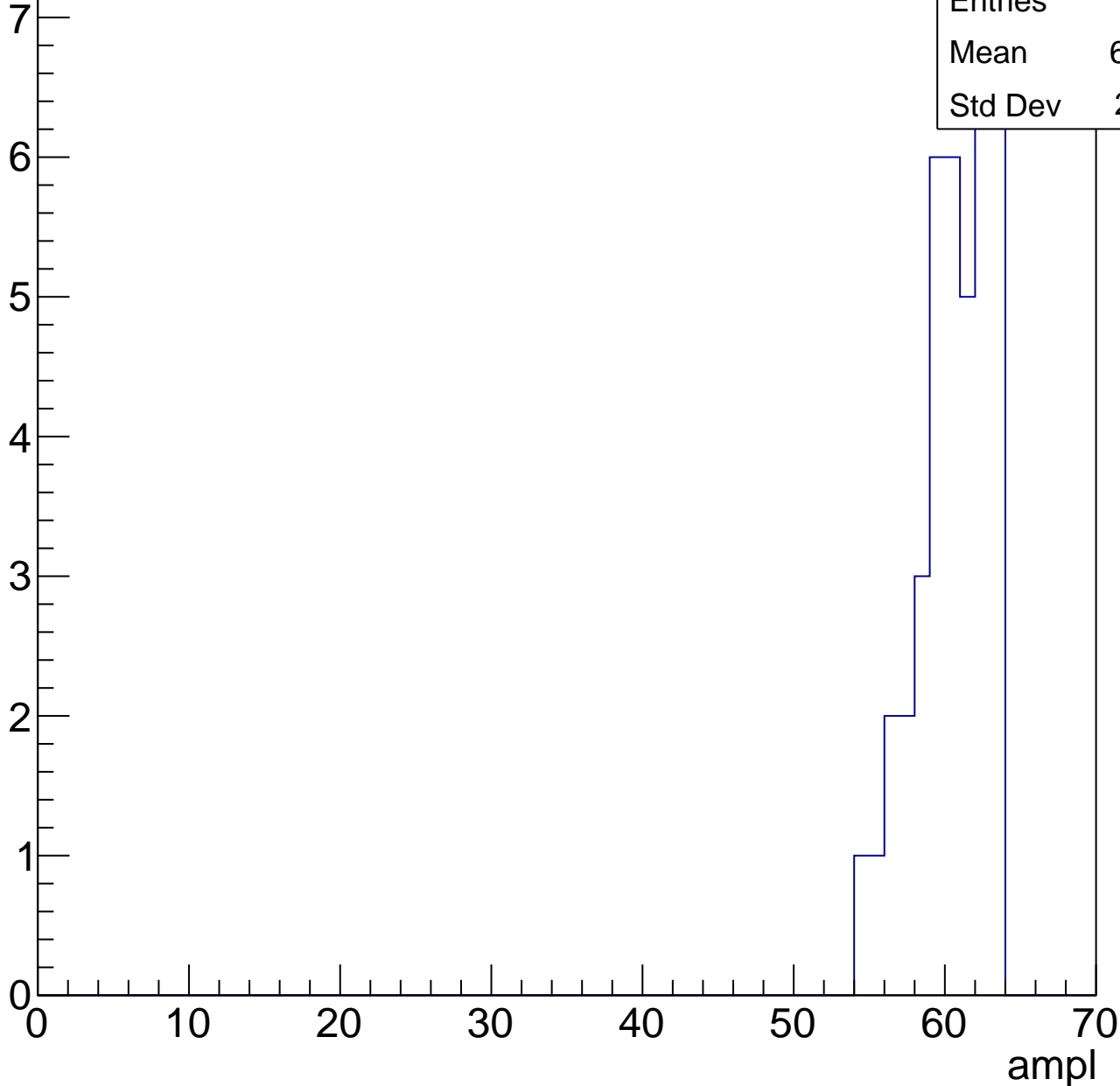


# B1L102S, U12-ch38, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	40
Mean	60.08
Std Dev	2.371



# B1L102S, U12-ch38, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	5
Mean	62.2
Std Dev	0.7483

ampl

0 10 20 30 40 50 60 70



# B1L102S, U12-ch38, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U12-ch39, adc0

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	81
Mean	30.38
Std Dev	3.207

**Gaus mean : 30.9164**

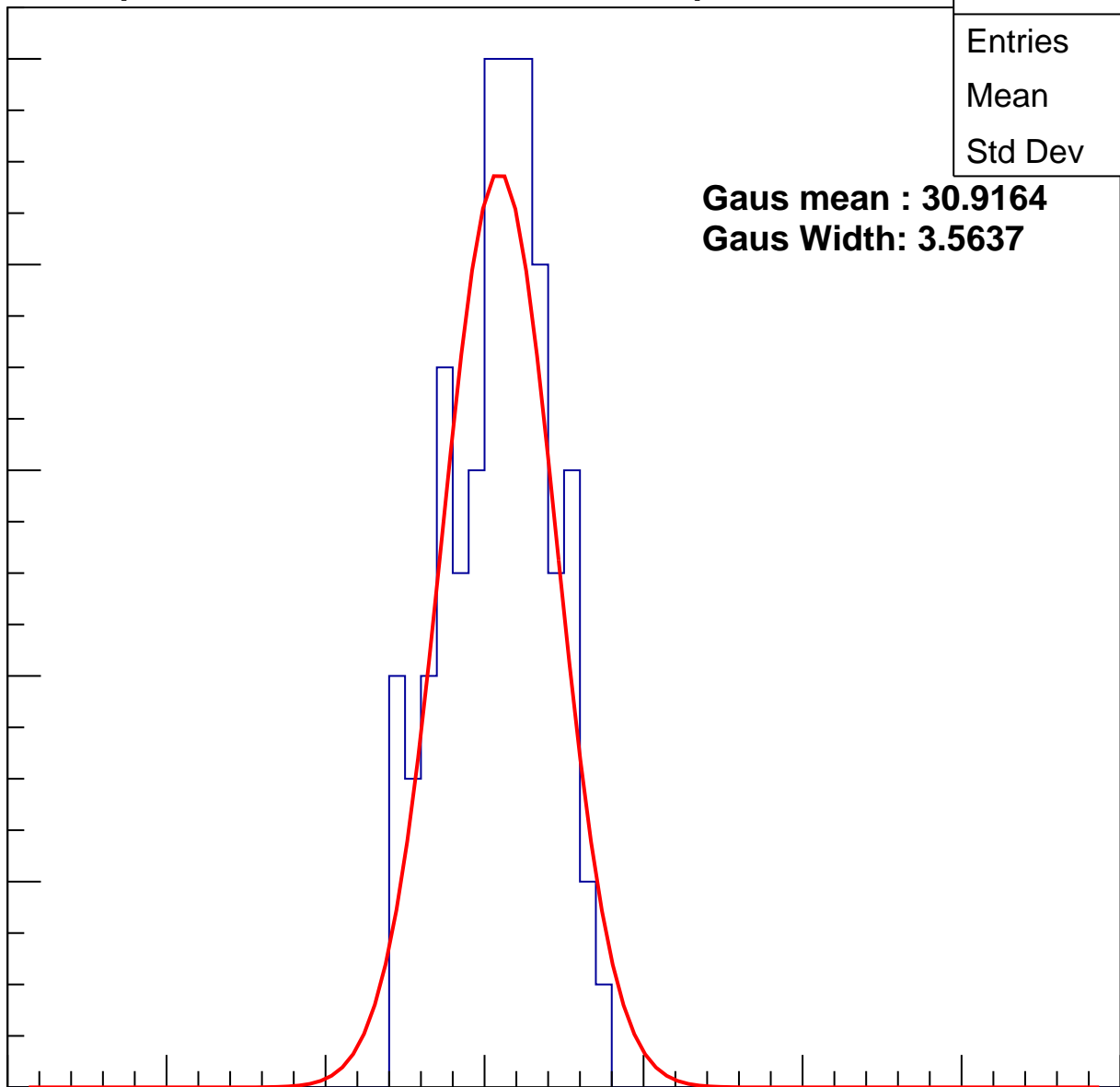
**Gaus Width: 3.5637**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L102S, U12-ch39, adc1

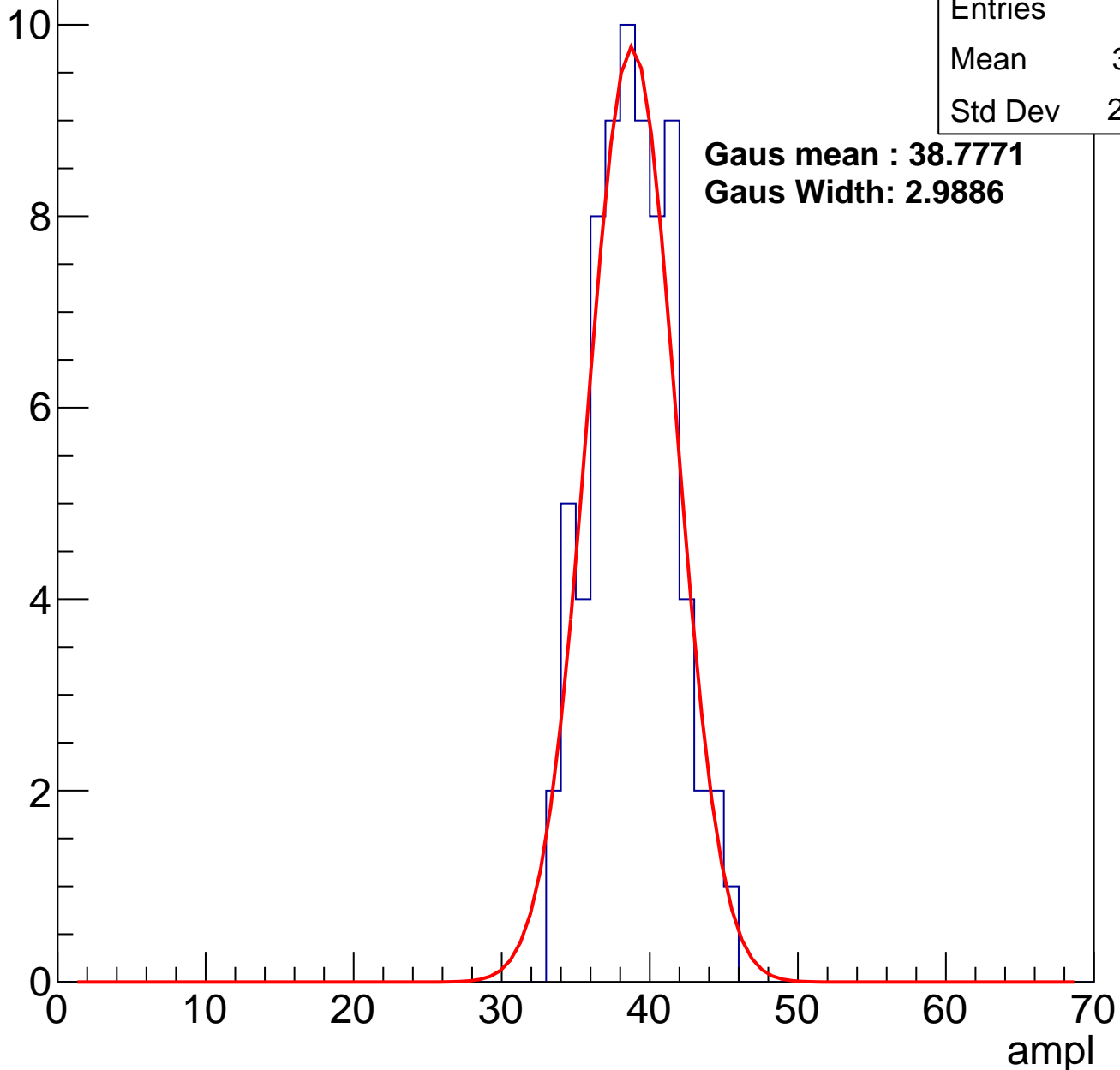
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	73
Mean	38.41
Std Dev	2.749

**Gaus mean : 38.7771**

**Gaus Width: 2.9886**

Entry



# B1L102S, U12-ch39, adc2

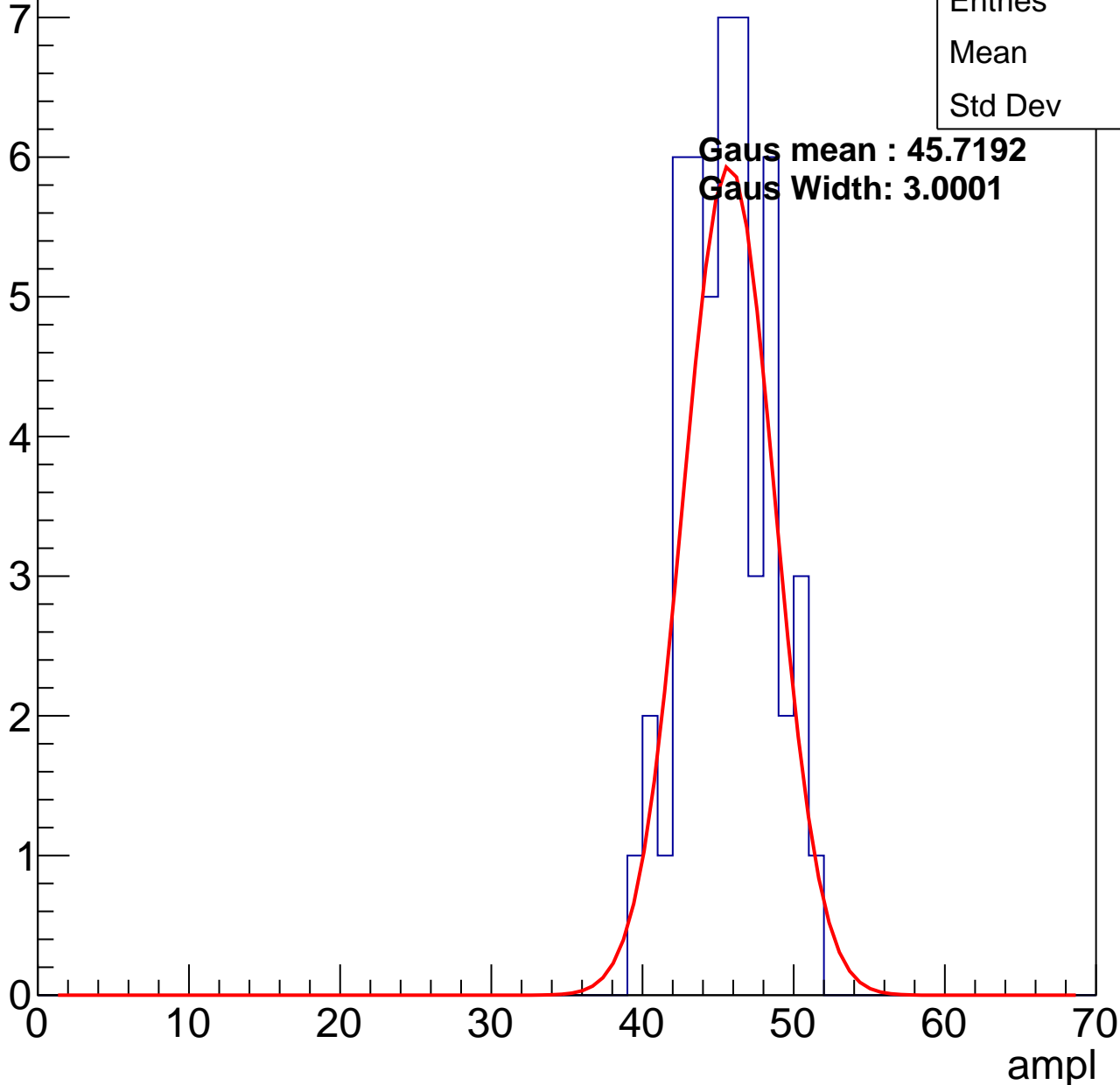
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	50
Mean	45.1
Std Dev	2.83

Gaus mean : 45.7192

Gaus Width: 3.0001

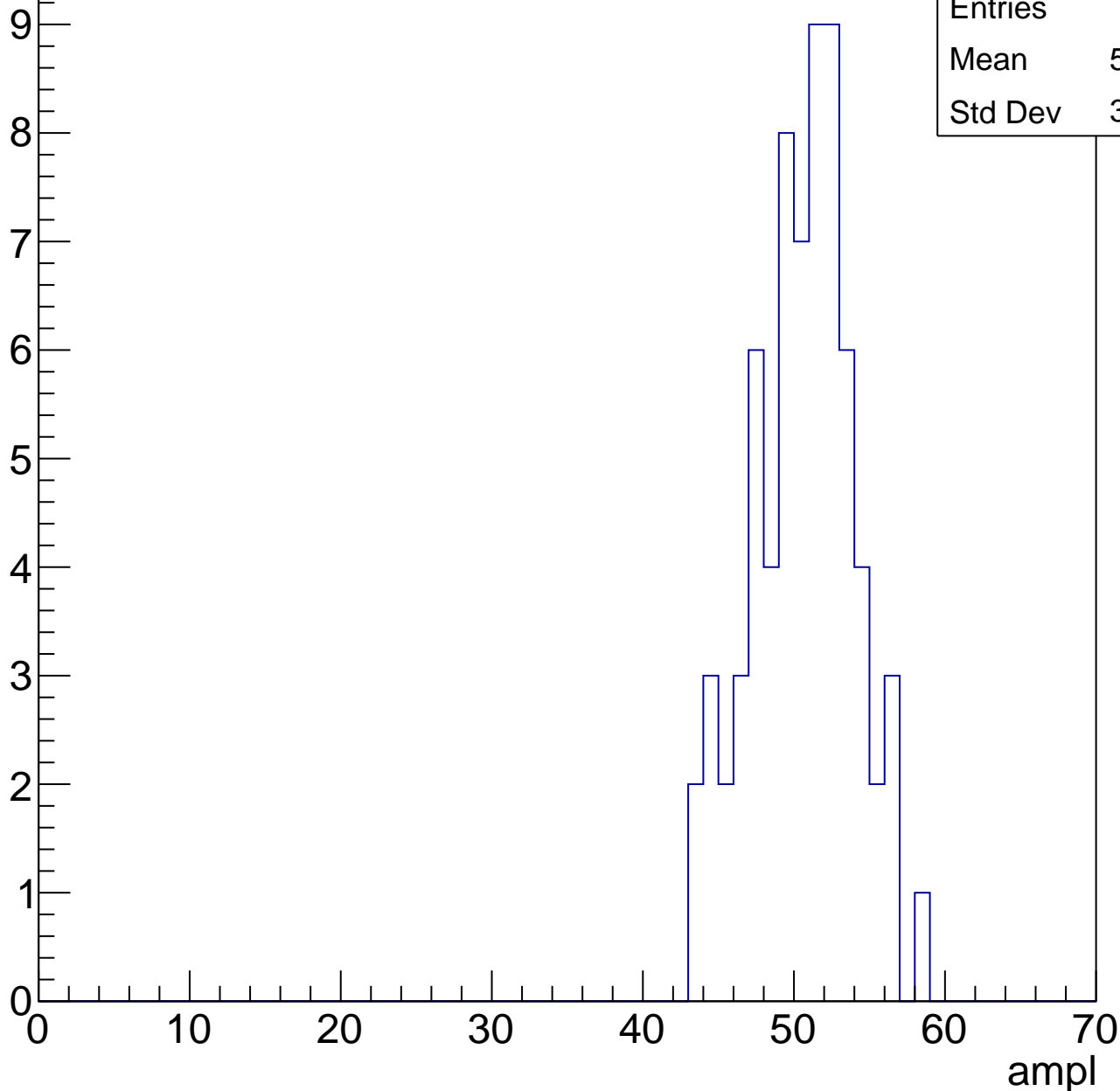


# B1L102S, U12-ch39, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	50.13
Std Dev	3.332



# B1L102S, U12-ch39, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	67
Mean	56.43
Std Dev	7.587

Entry

10

8

6

4

2

0

0

10

20

30

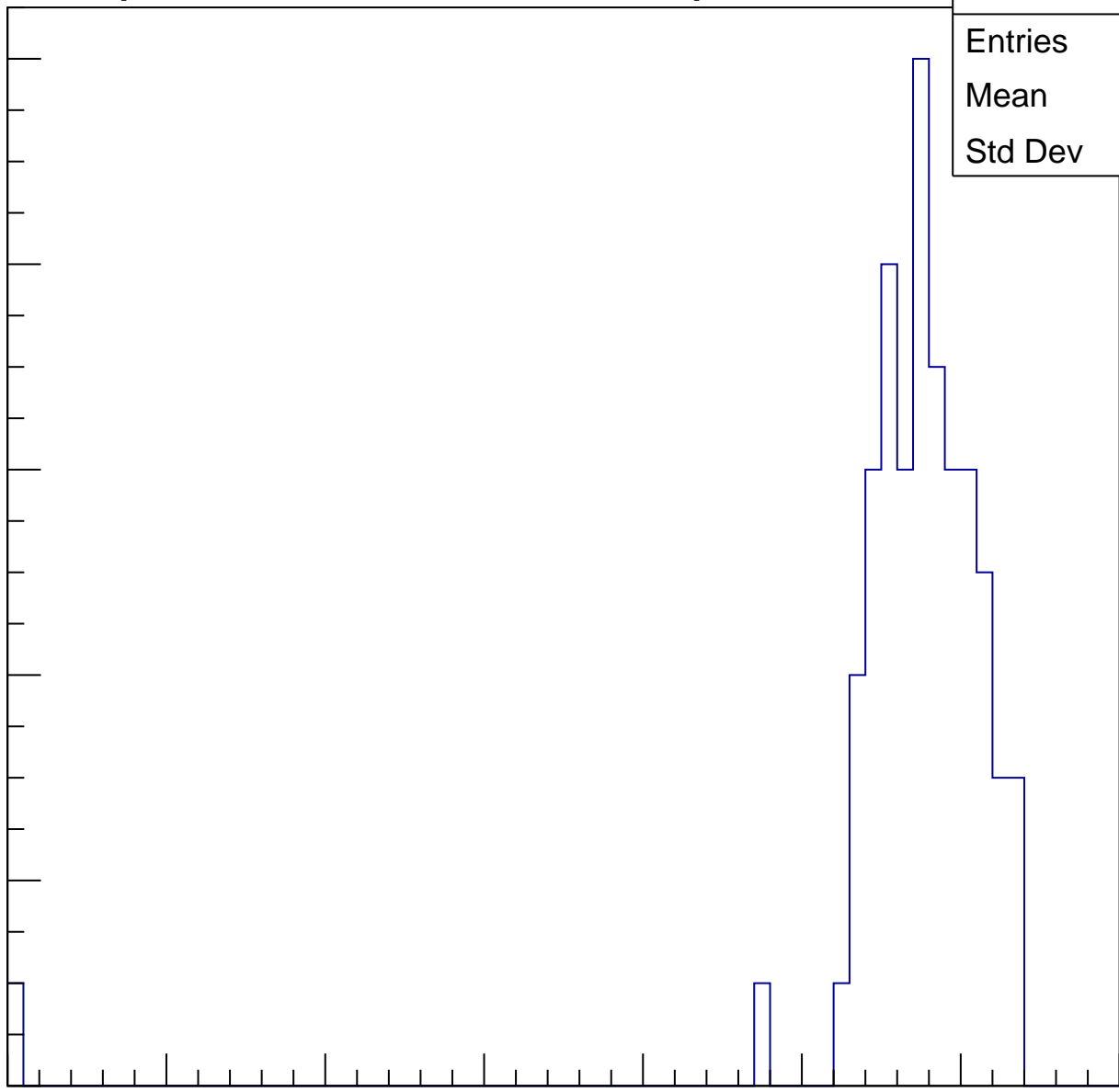
40

50

60

70

ampl

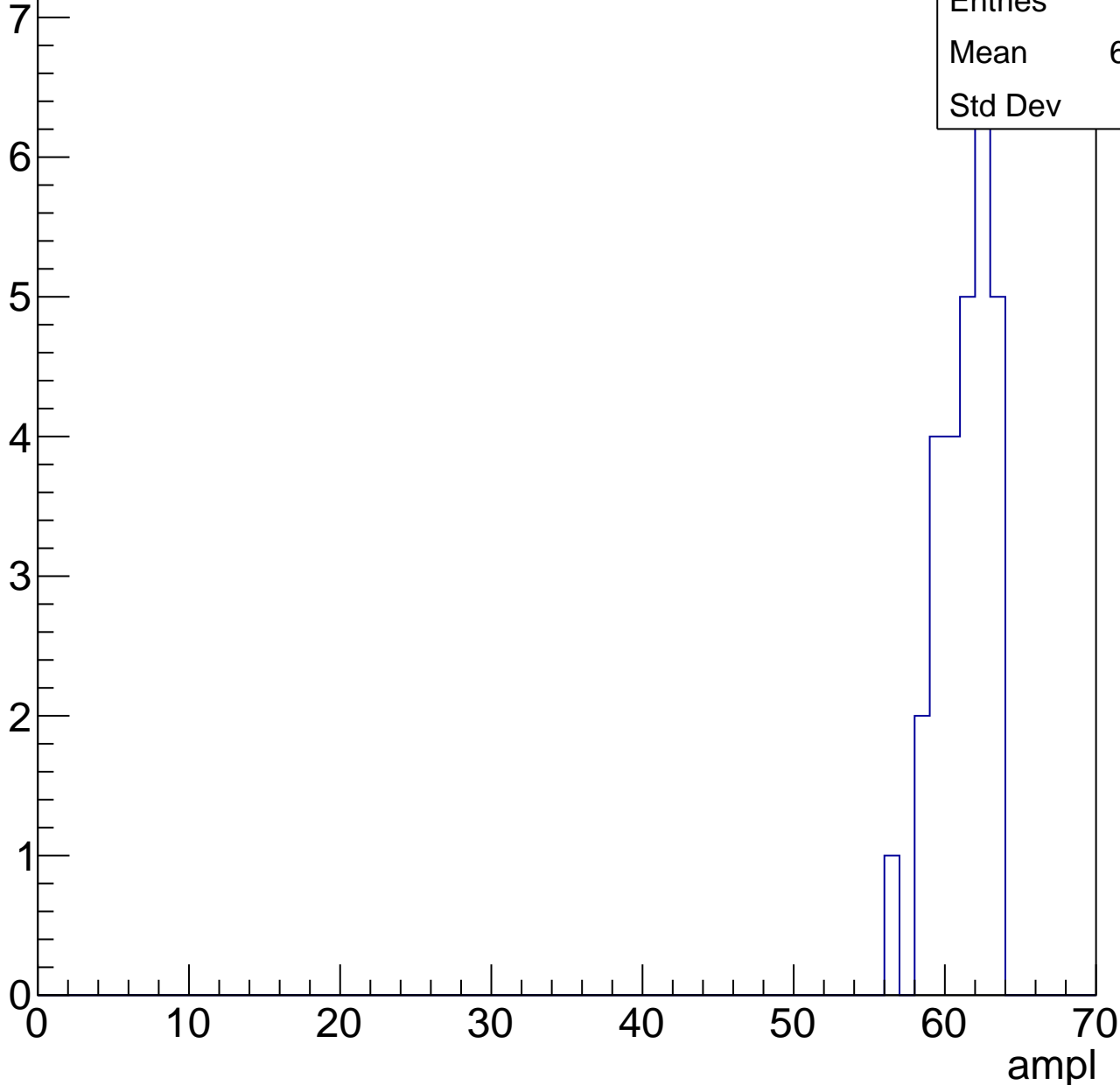


# B1L102S, U12-ch39, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	28
Mean	60.79
Std Dev	1.78



# B1L102S, U12-ch39, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

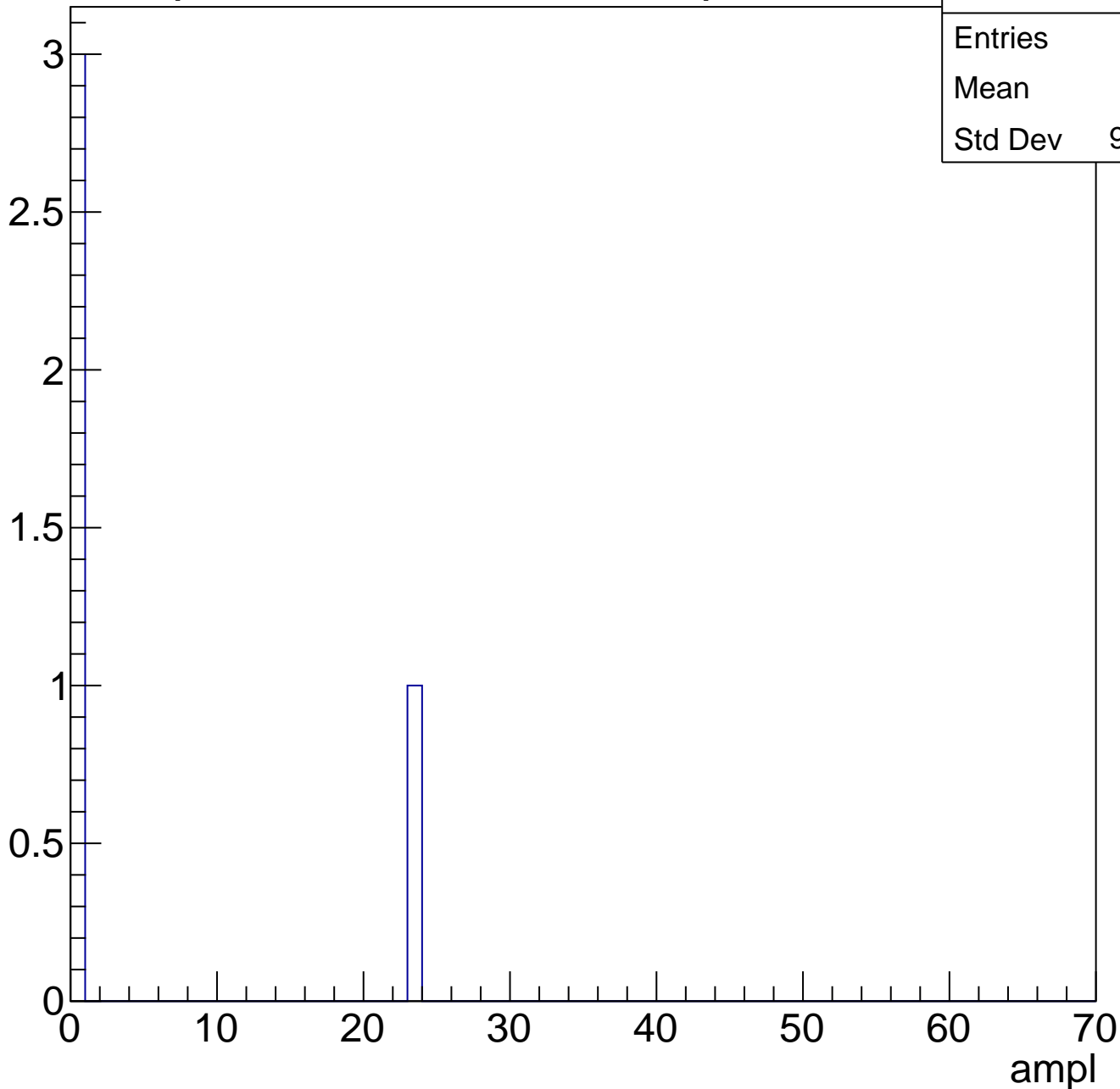




# B1L102S, U12-ch39, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U12-ch40, adc0

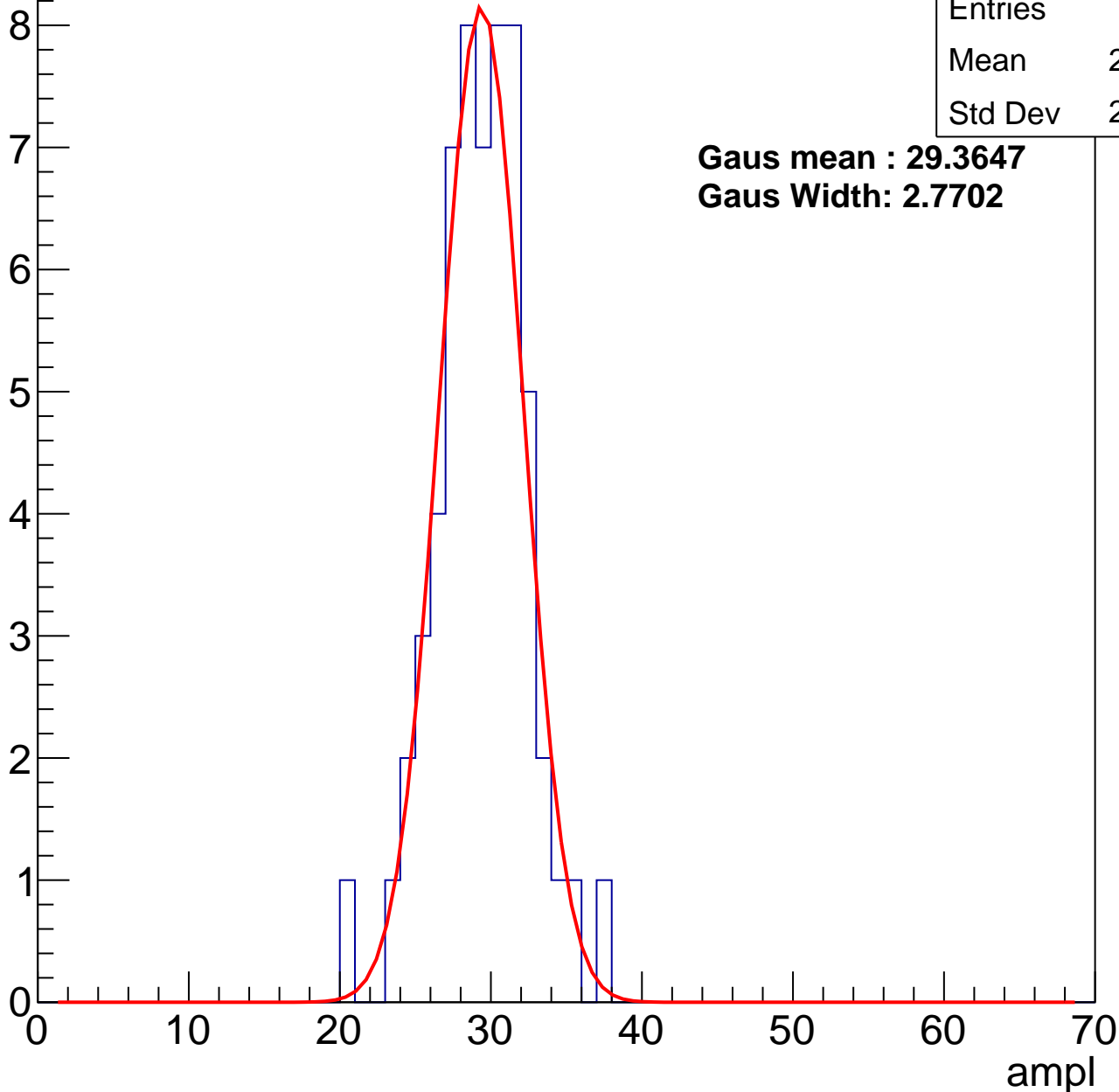
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	59
Mean	28.92
Std Dev	2.993

**Gaus mean : 29.3647**

**Gaus Width: 2.7702**



# B1L102S, U12-ch40, adc1

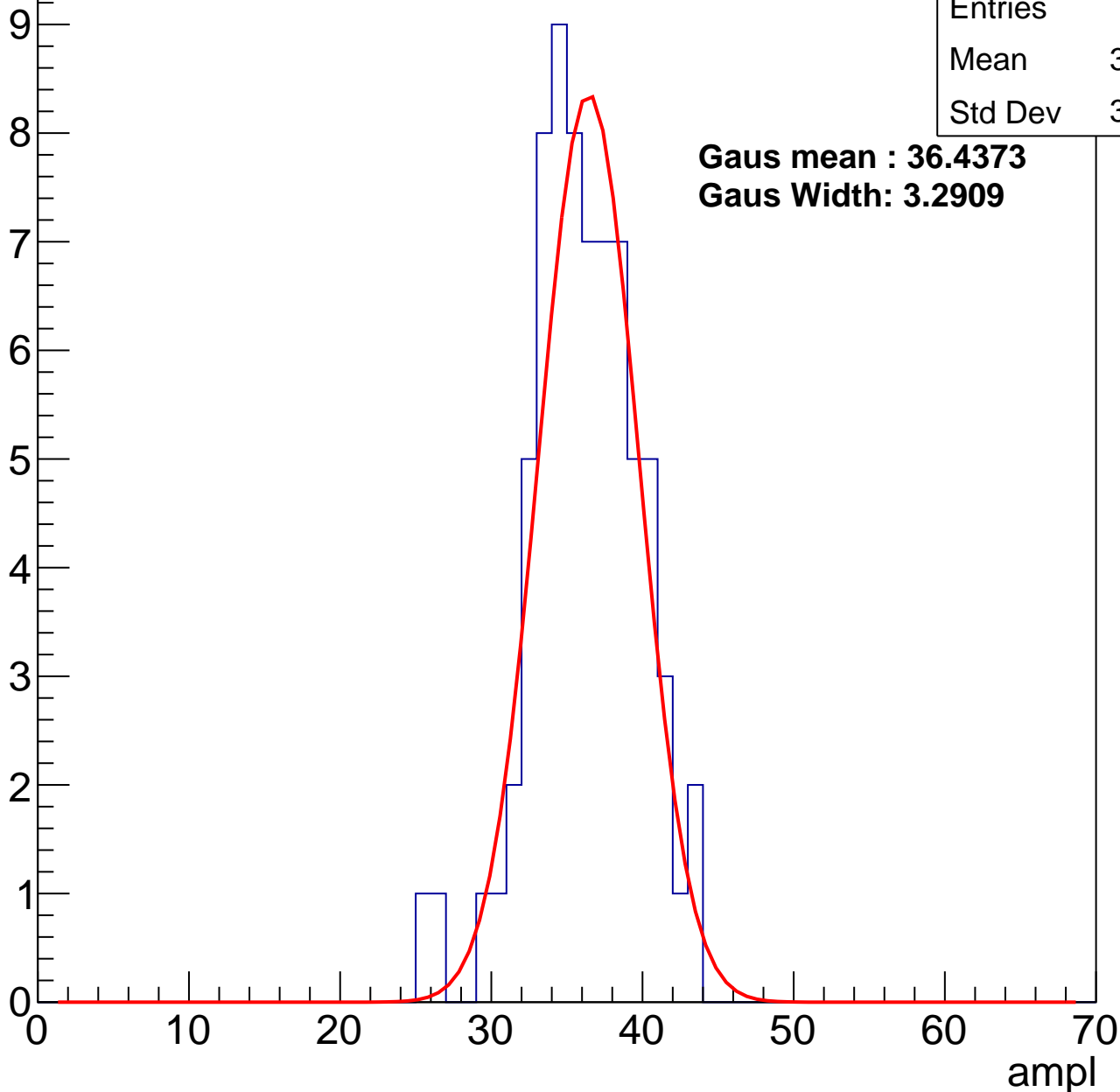
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	73
Mean	35.68
Std Dev	3.538

**Gaus mean : 36.4373**

**Gaus Width: 3.2909**



# B1L102S, U12-ch40, adc2

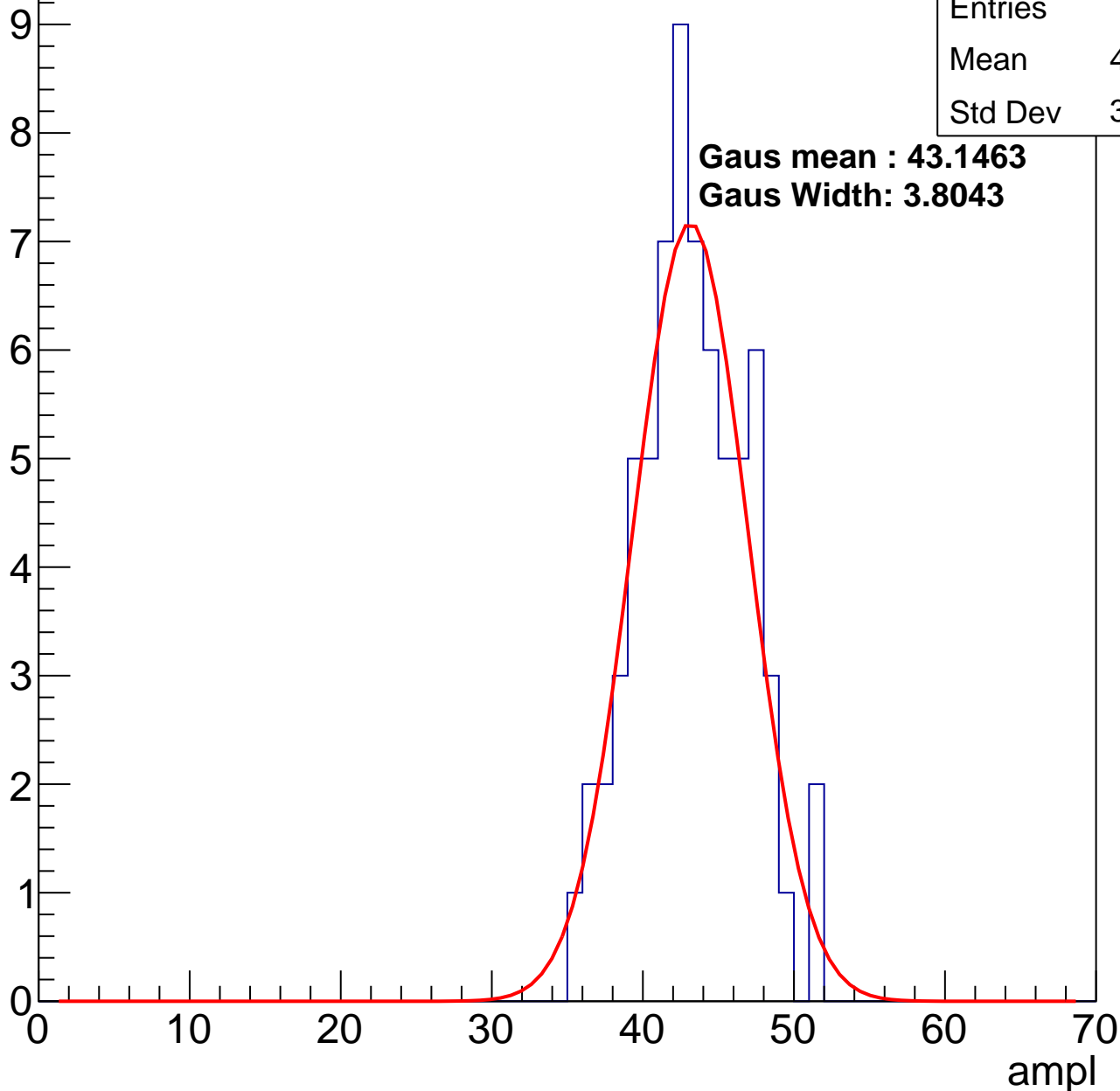
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	42.78
Std Dev	3.558

**Gaus mean : 43.1463**

**Gaus Width: 3.8043**

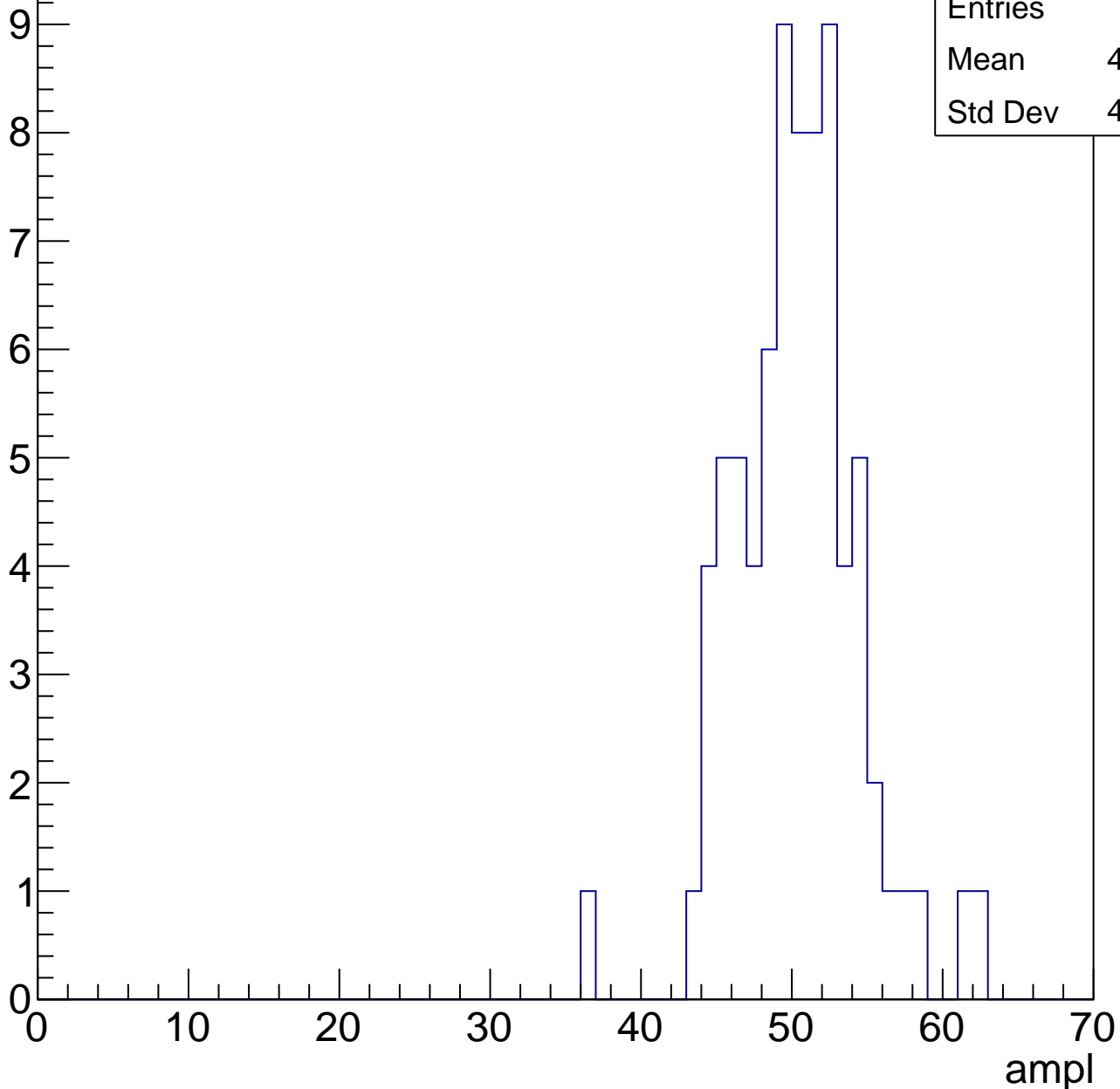


# B1L102S, U12-ch40, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	76
Mean	49.86
Std Dev	4.113

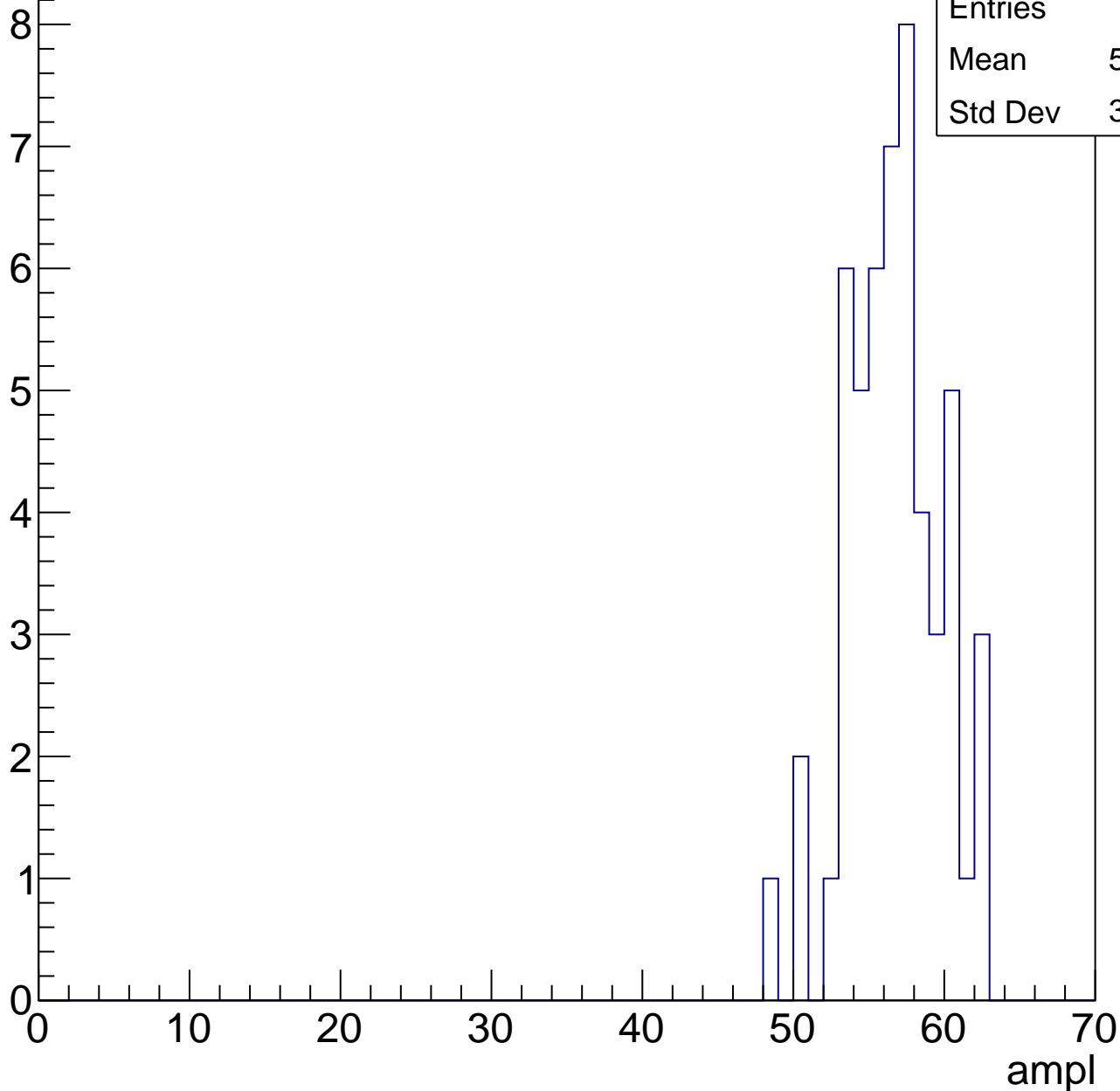


# B1L102S, U12-ch40, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	52
Mean	56.19
Std Dev	3.082



# B1L102S, U12-ch40, adc5

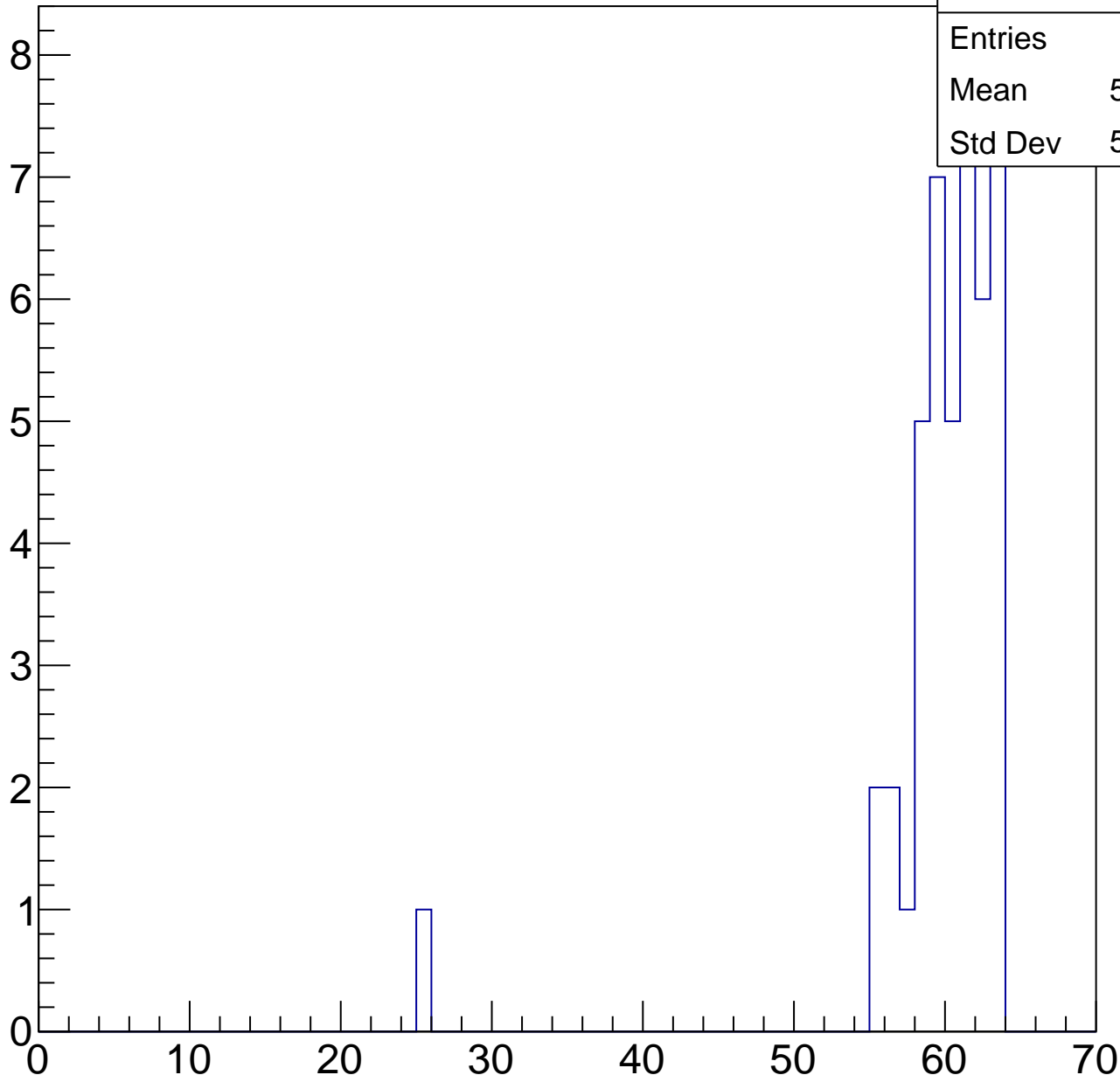
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	45
Mean	59.36
Std Dev	5.634

ampl



# B1L102S, U12-ch40, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U12-ch40, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U12-ch41, adc0

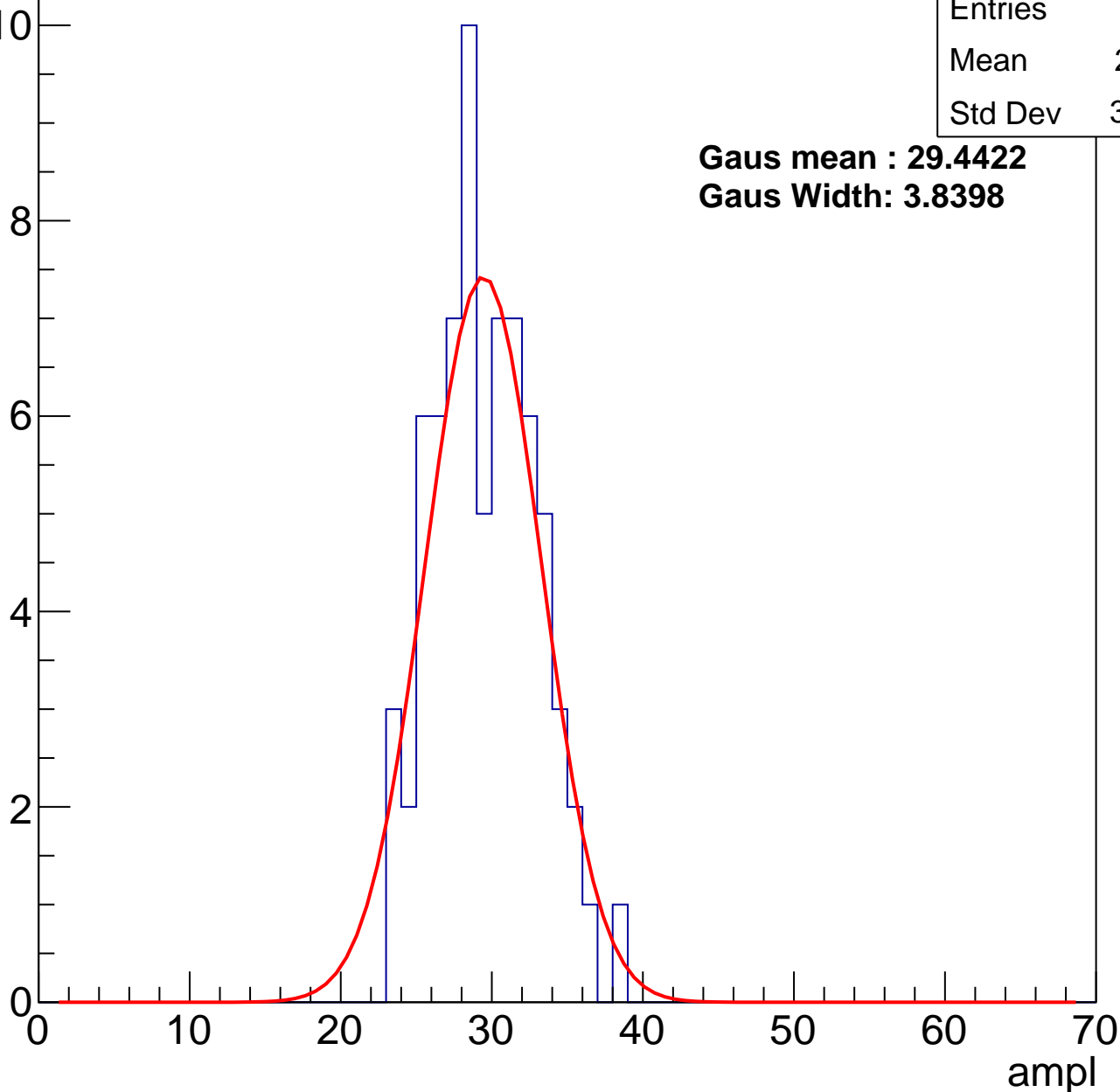
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	71
Mean	29.11
Std Dev	3.338

**Gaus mean : 29.4422**

**Gaus Width: 3.8398**



# B1L102S, U12-ch41, adc1

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	77
Mean	36.38
Std Dev	3.629

**Gaus mean : 36.5898**

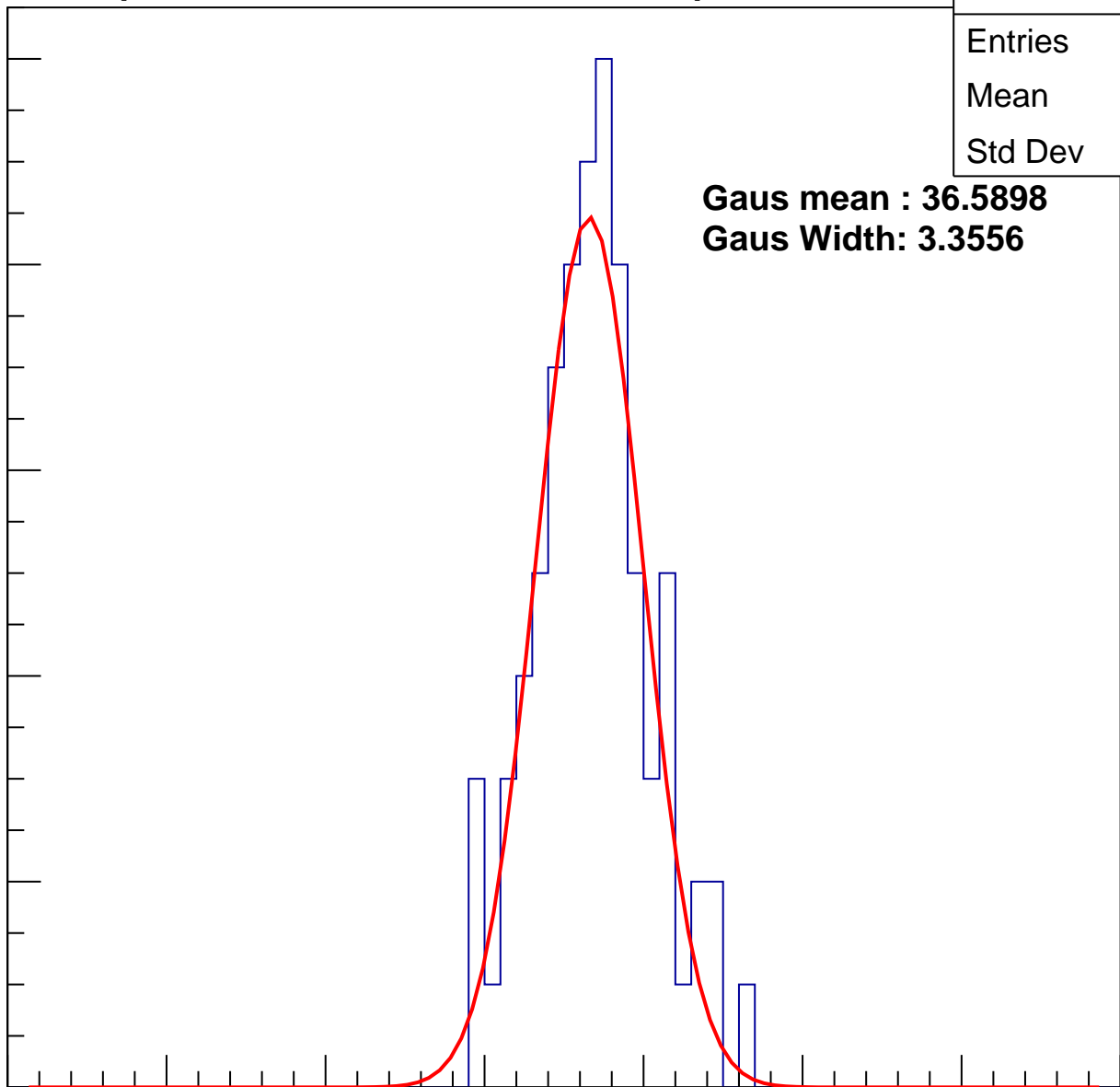
**Gaus Width: 3.3556**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L102S, U12-ch41, adc2

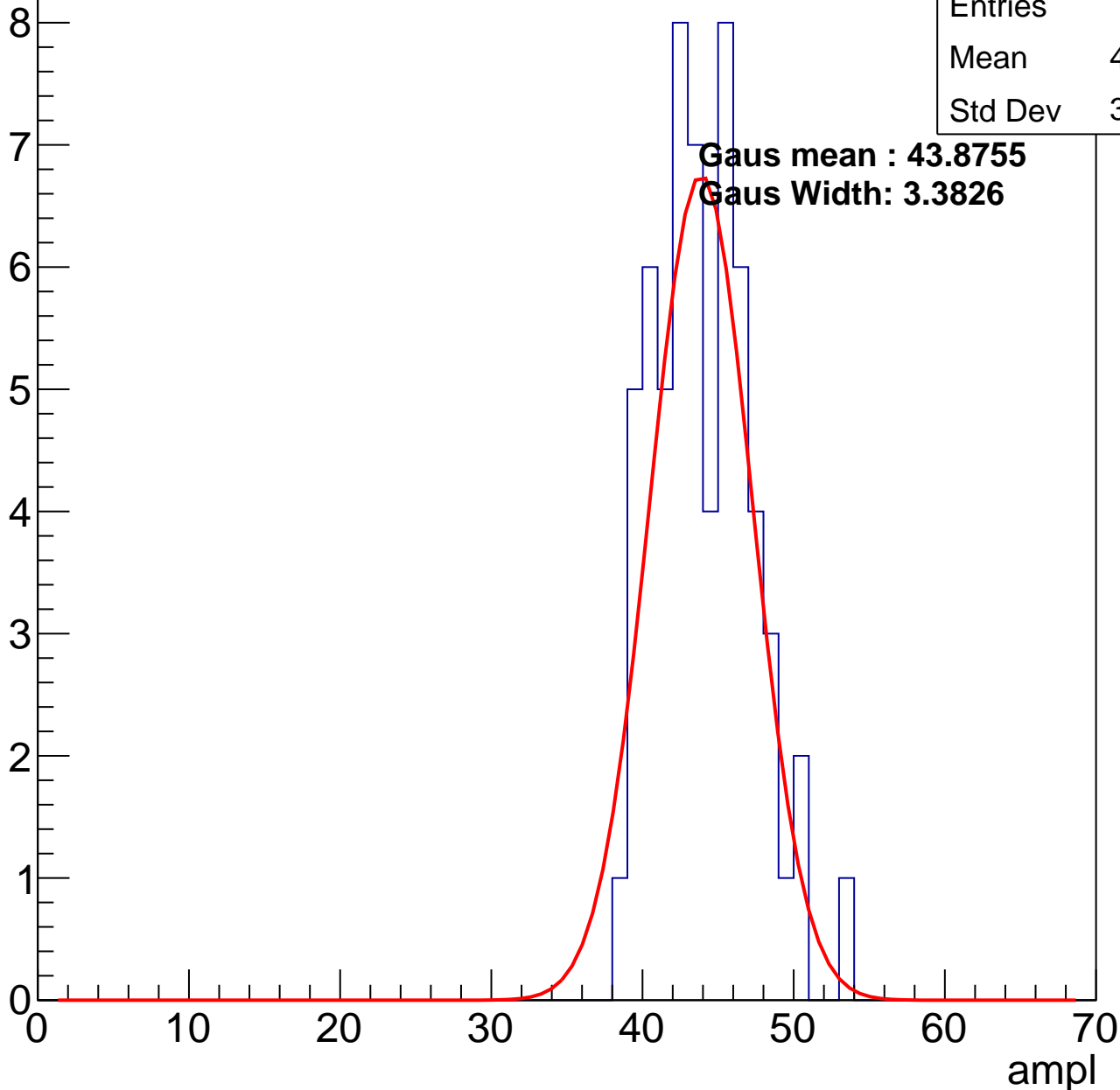
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	43.62
Std Dev	3.204

**Gaus mean : 43.8755**

**Gaus Width: 3.3826**

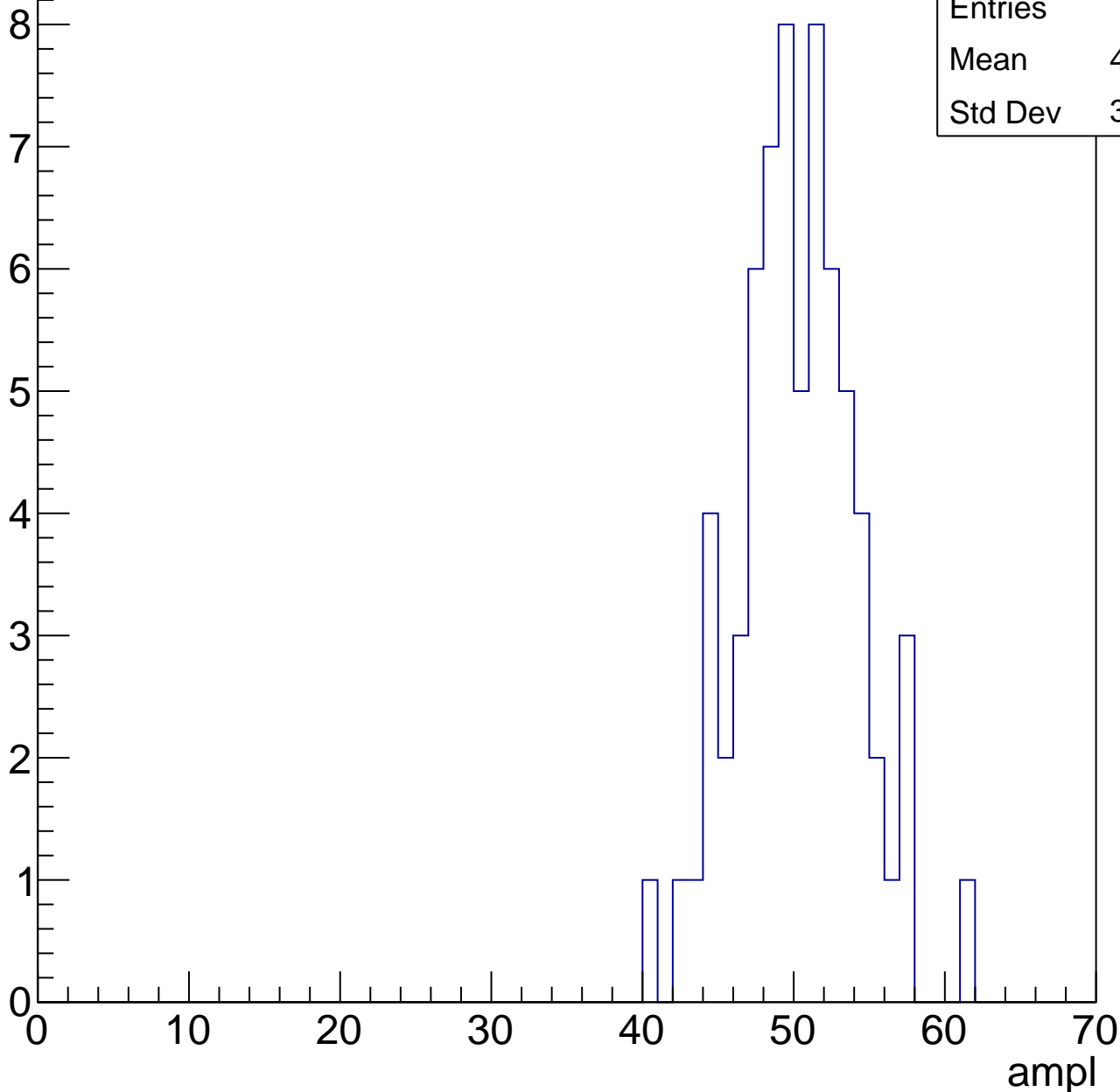


# B1L102S, U12-ch41, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	49.82
Std Dev	3.907

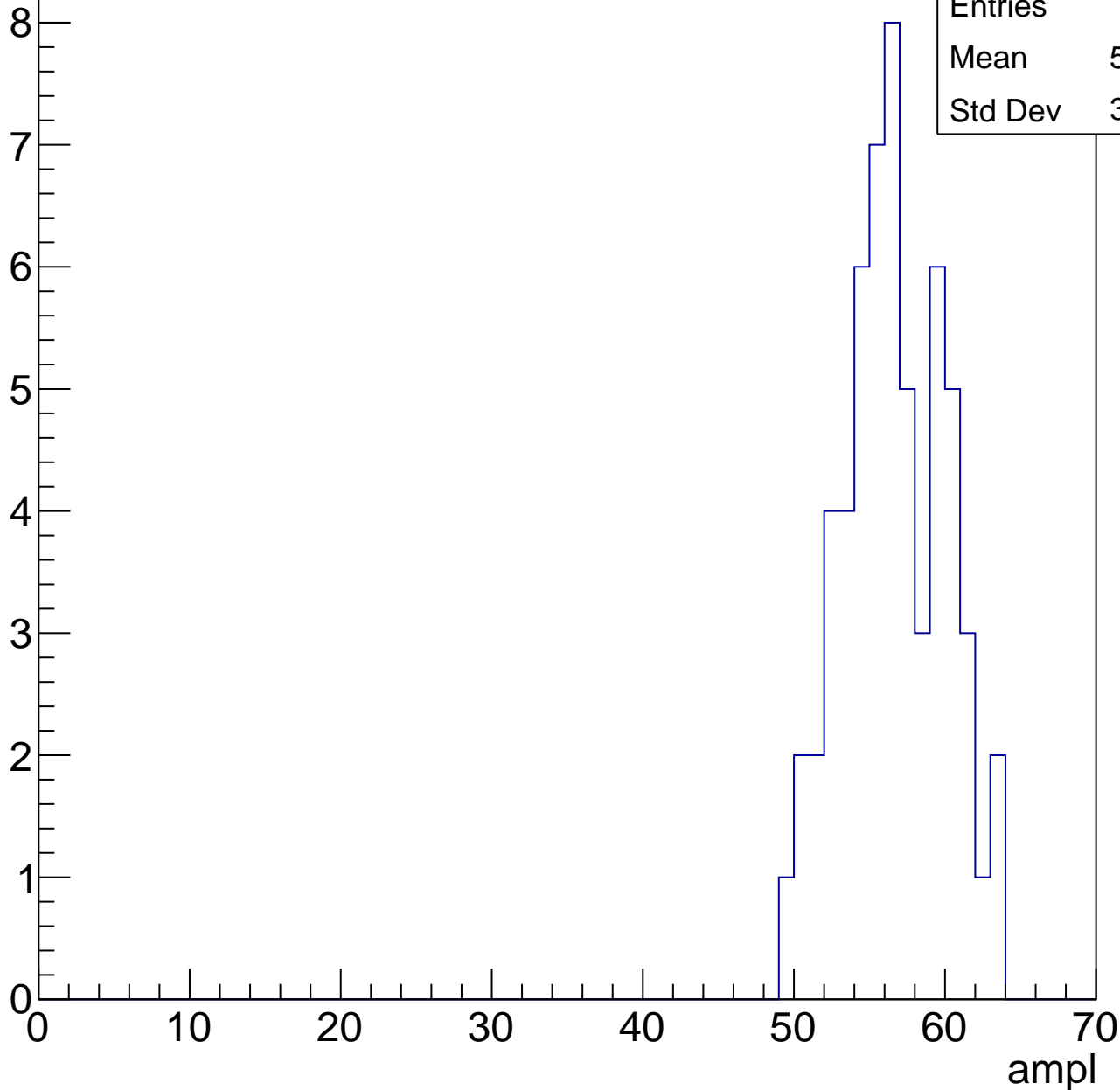


# B1L102S, U12-ch41, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	59
Mean	56.14
Std Dev	3.347

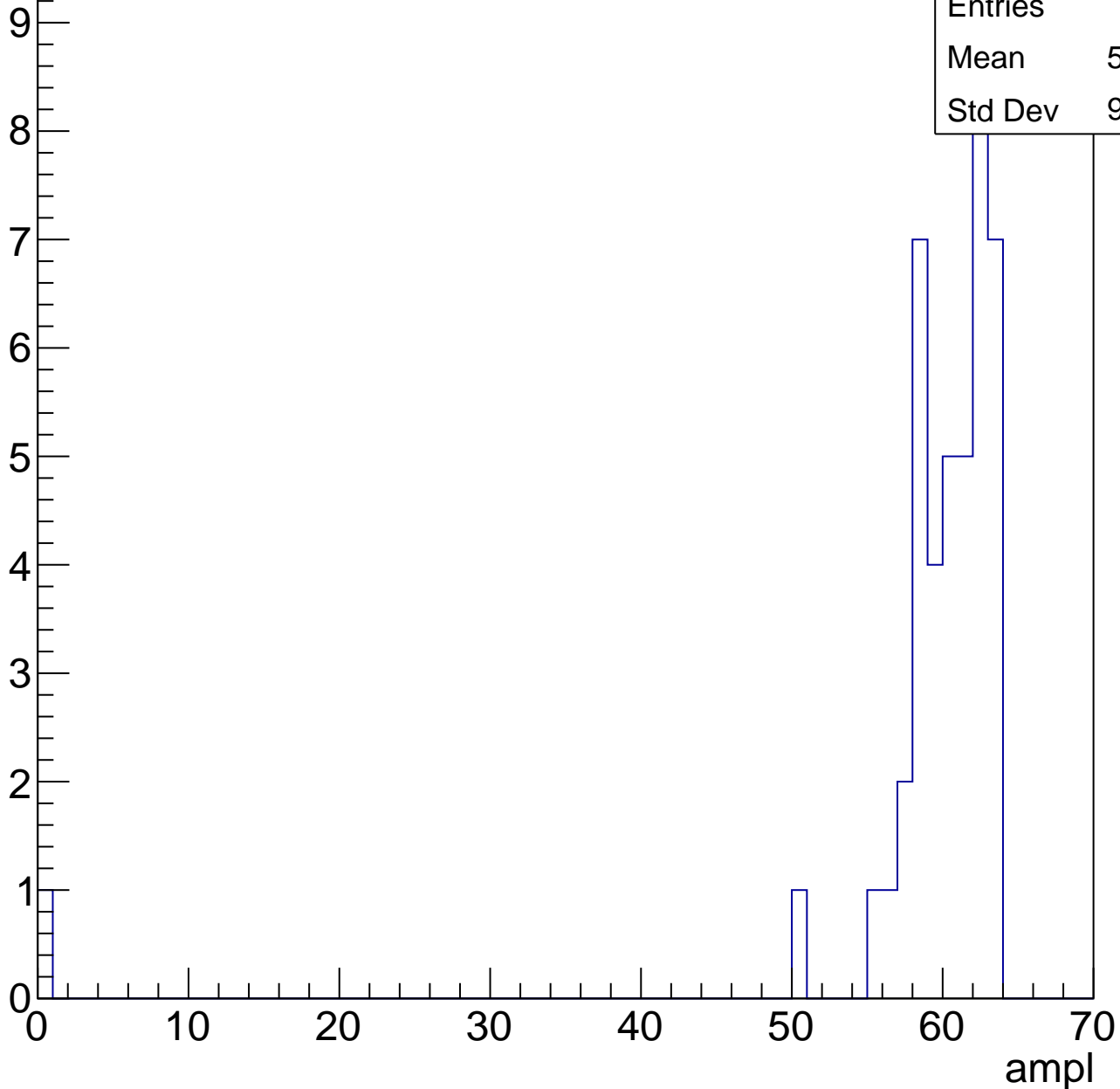


# B1L102S, U12-ch41, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	43
Mean	58.63
Std Dev	9.418



# B1L102S, U12-ch41, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

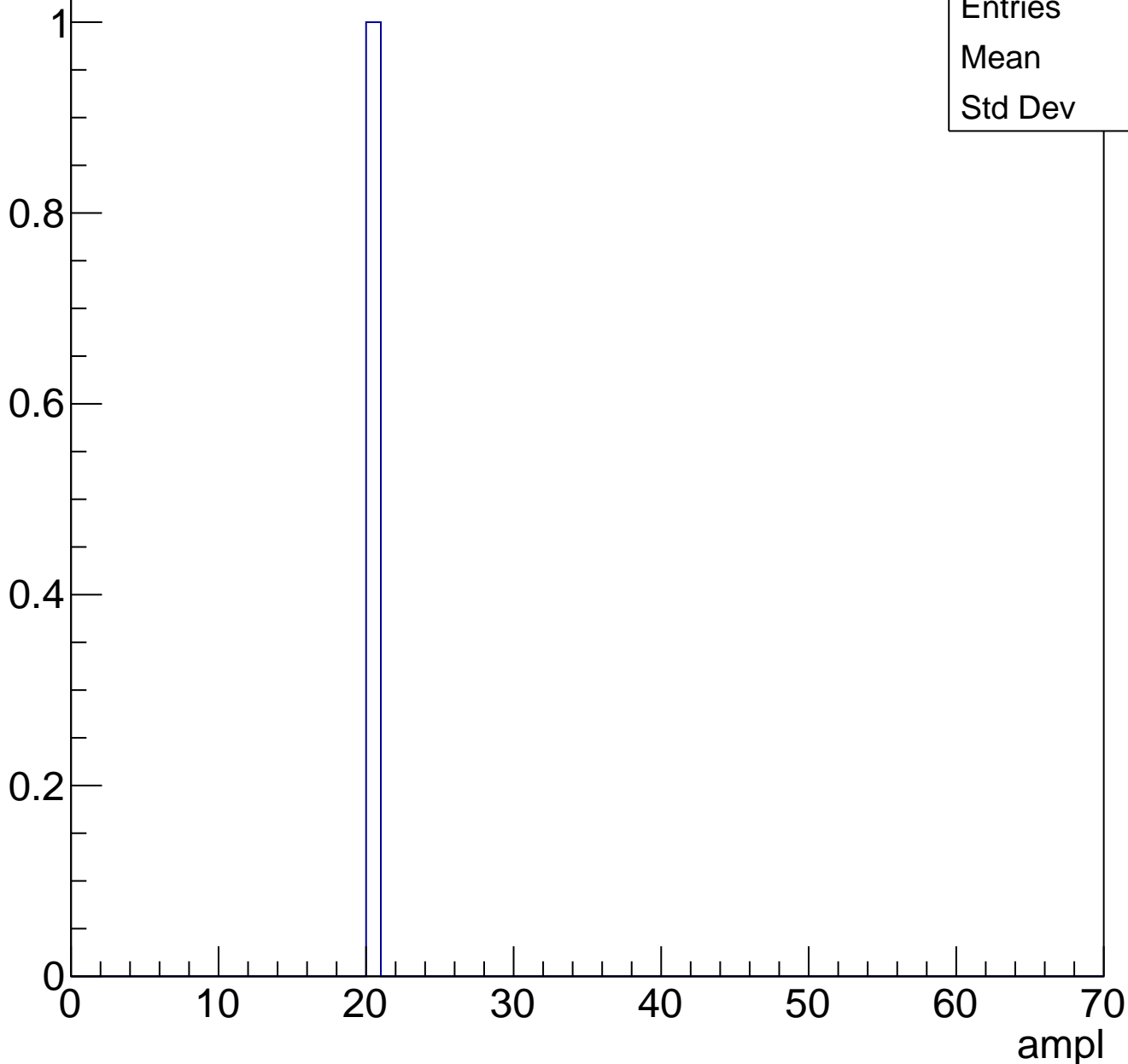




# B1L102S, U12-ch41, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U12-ch42, adc0

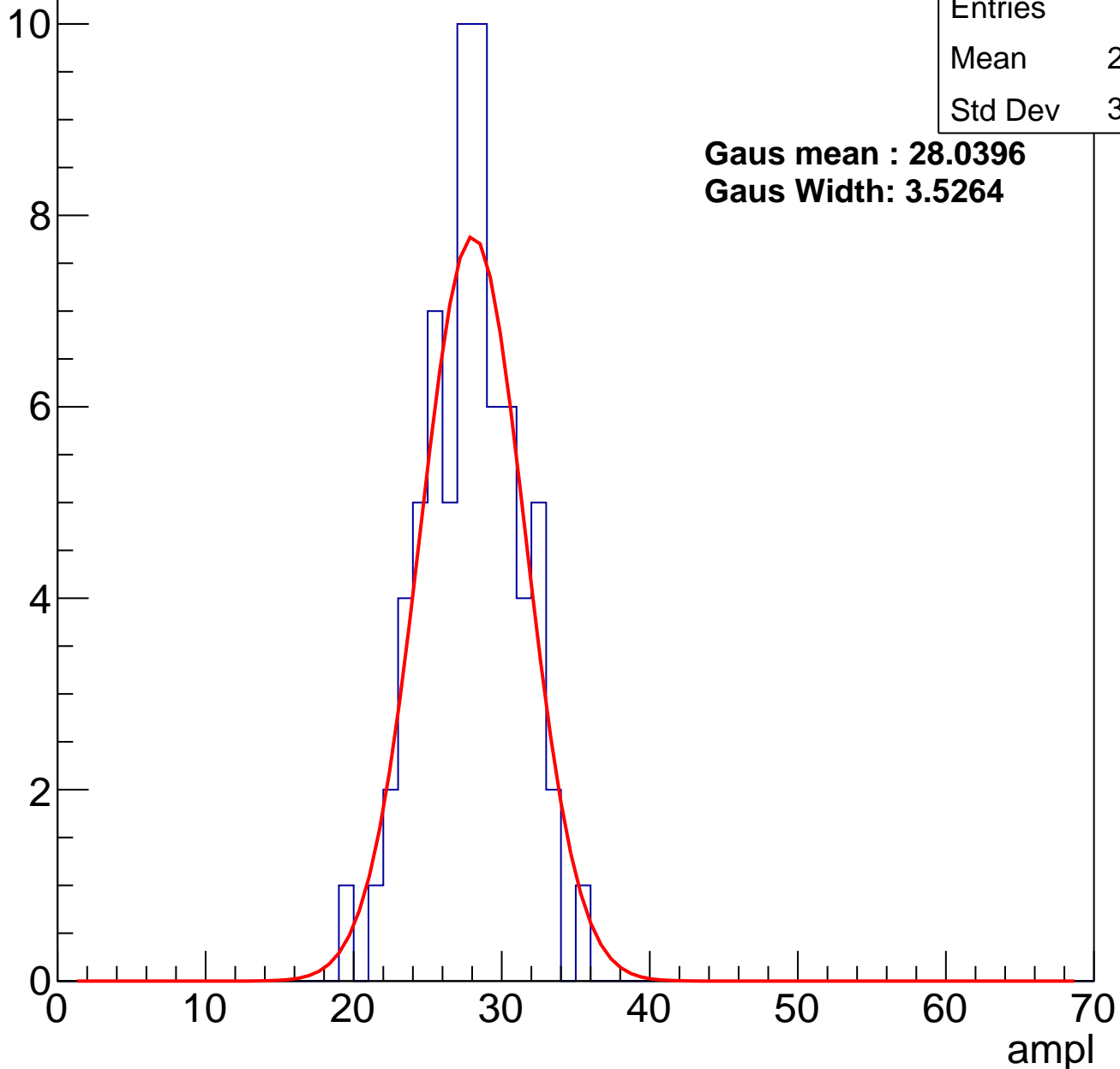
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	69
Mean	27.39
Std Dev	3.172

**Gaus mean : 28.0396**

**Gaus Width: 3.5264**

Entry



# B1L102S, U12-ch42, adc1

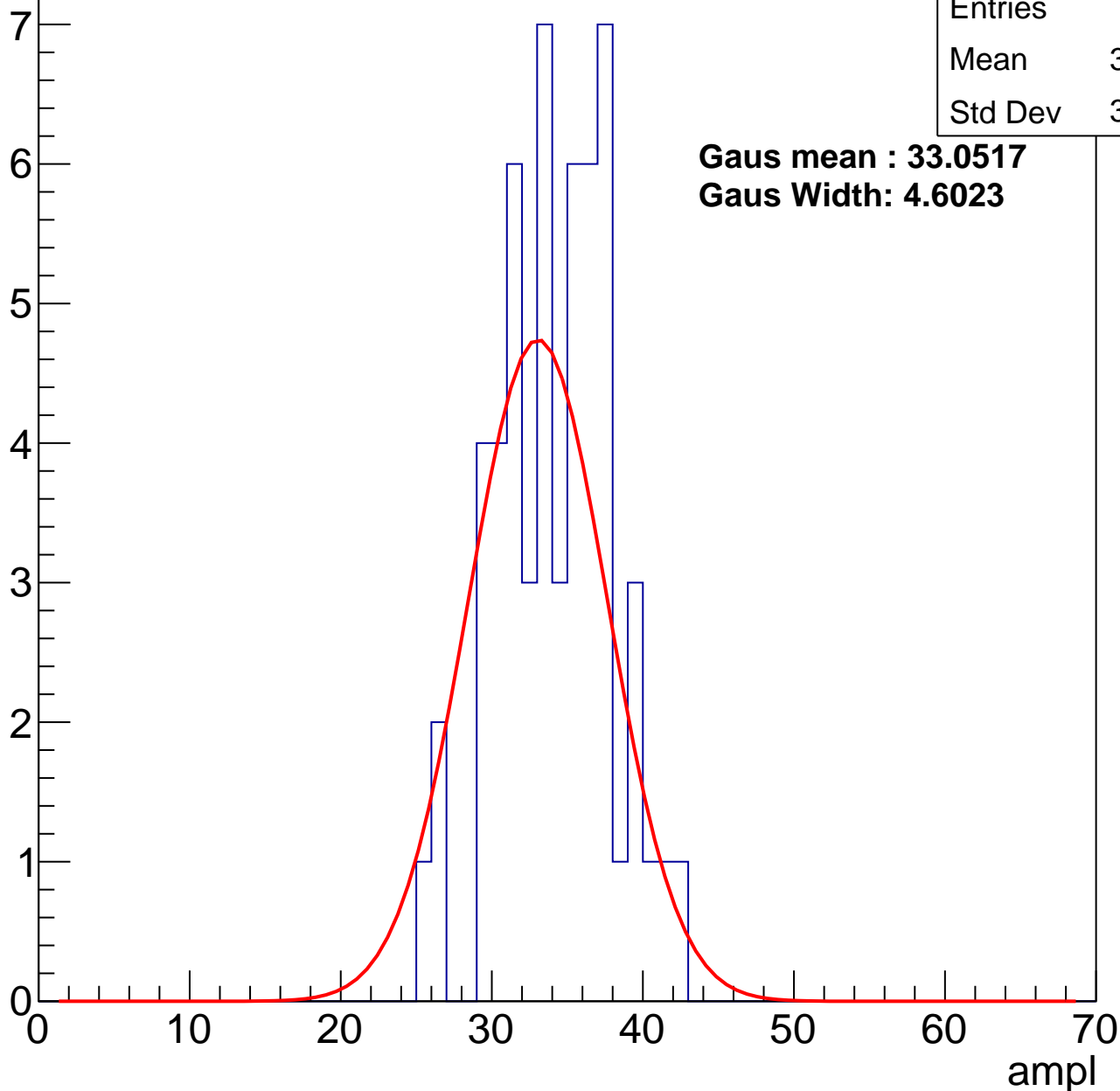
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	56
Mean	33.77
Std Dev	3.722

**Gaus mean : 33.0517**

**Gaus Width: 4.6023**



# B1L102S, U12-ch42, adc2

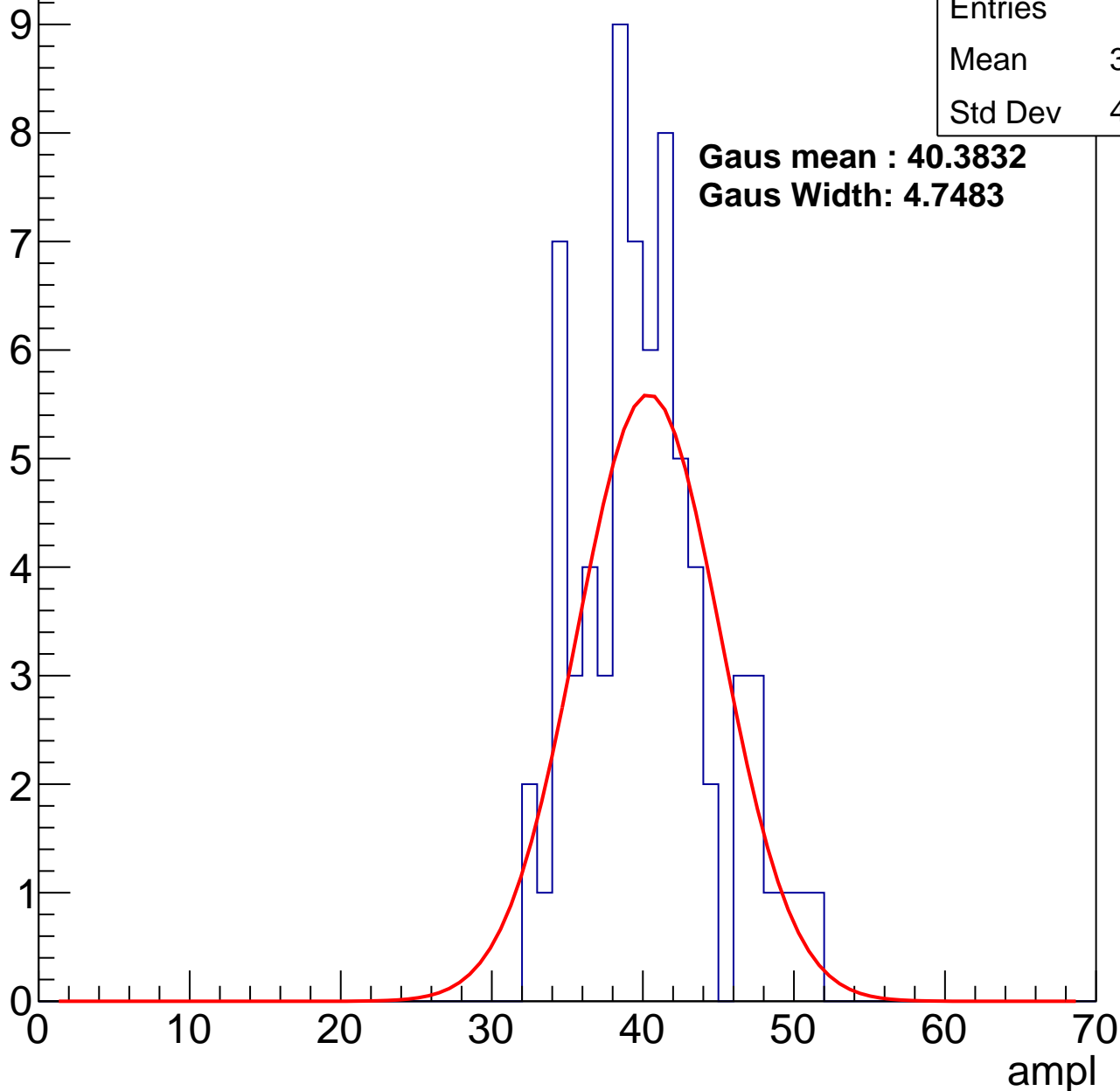
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	71
Mean	39.79
Std Dev	4.363

**Gaus mean : 40.3832**

**Gaus Width: 4.7483**

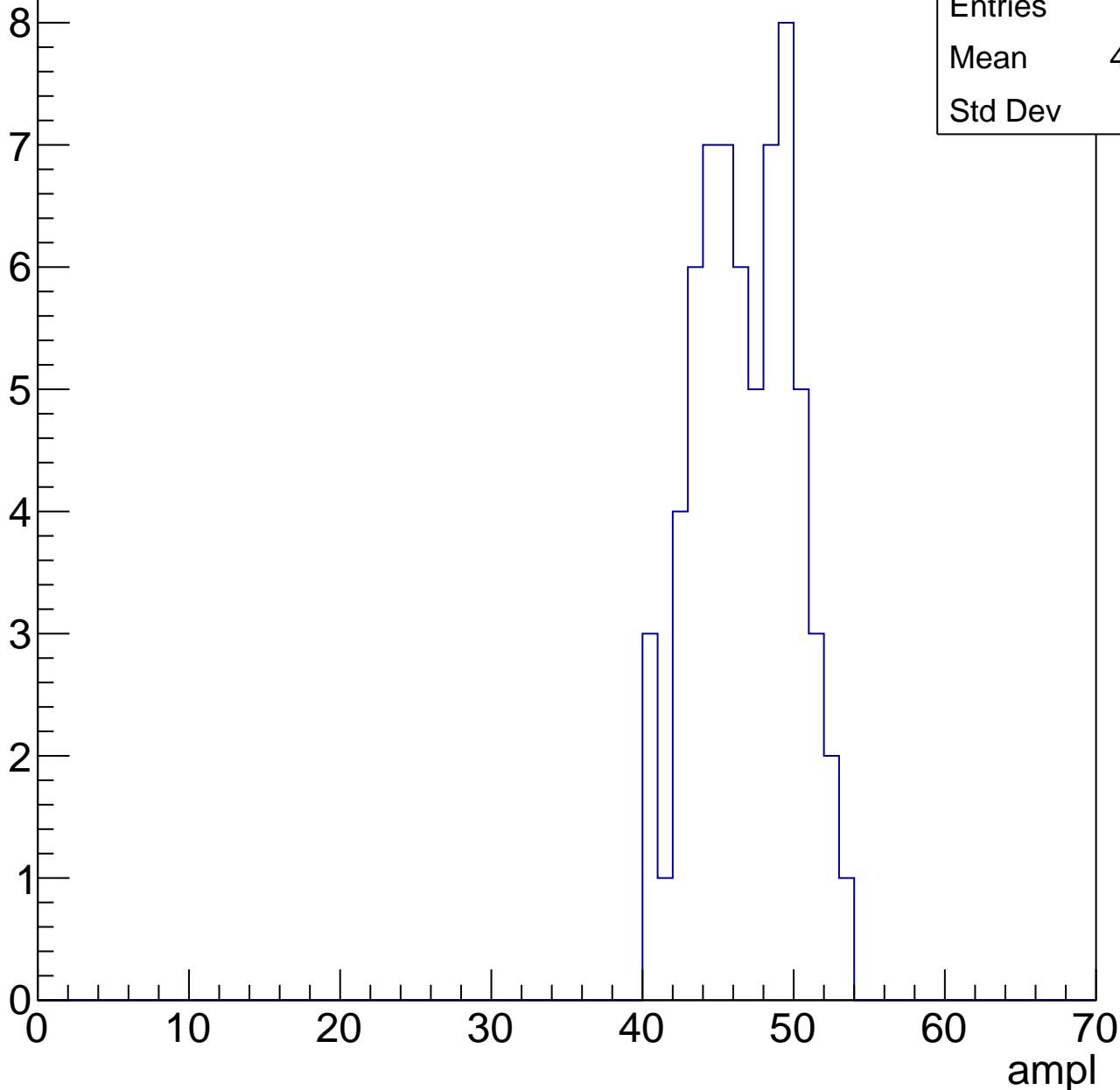


# B1L102S, U12-ch42, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

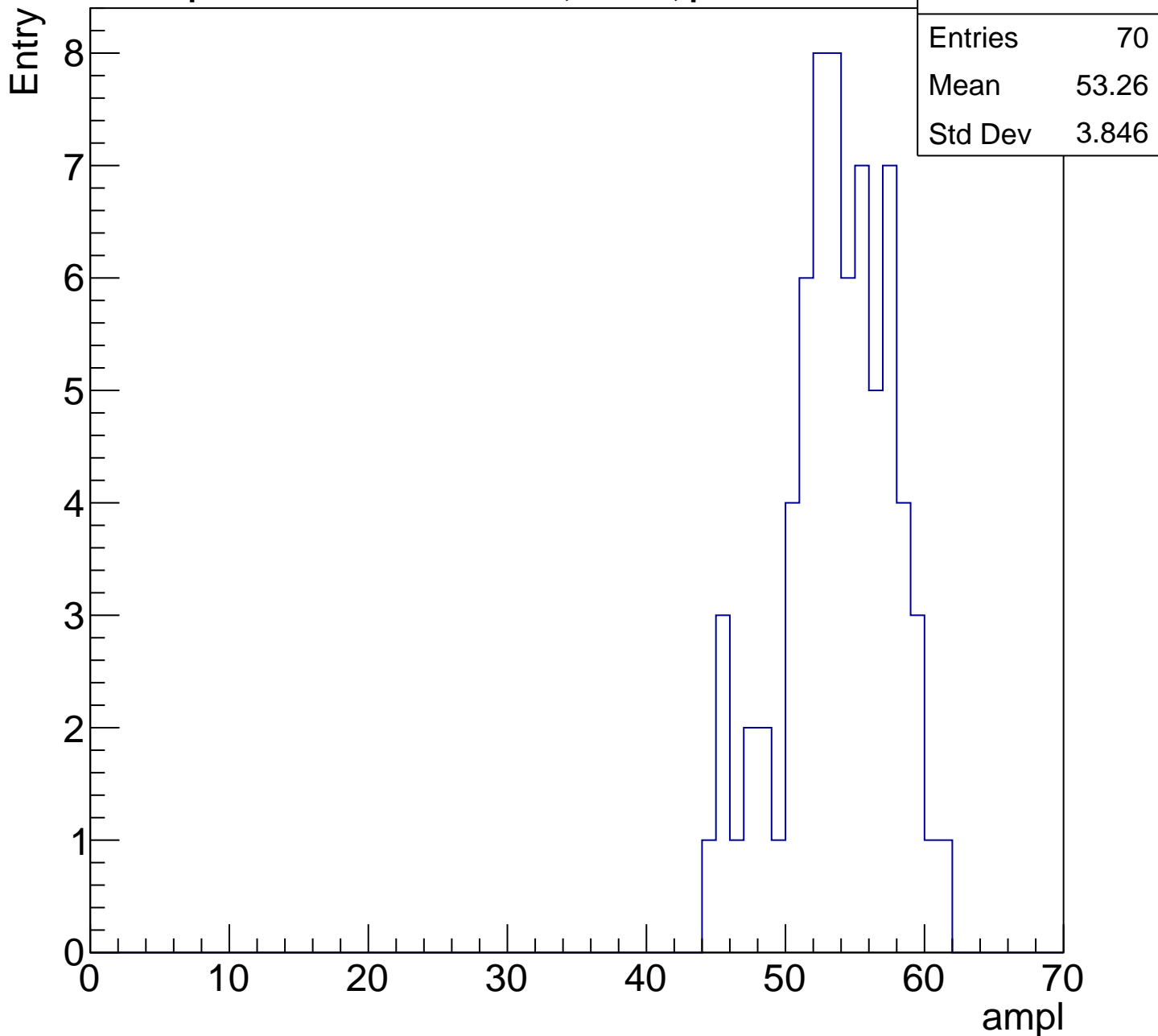
Entry

Entries	65
Mean	46.29
Std Dev	3.19



# B1L102S, U12-ch42, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2



# B1L102S, U12-ch42, adc5

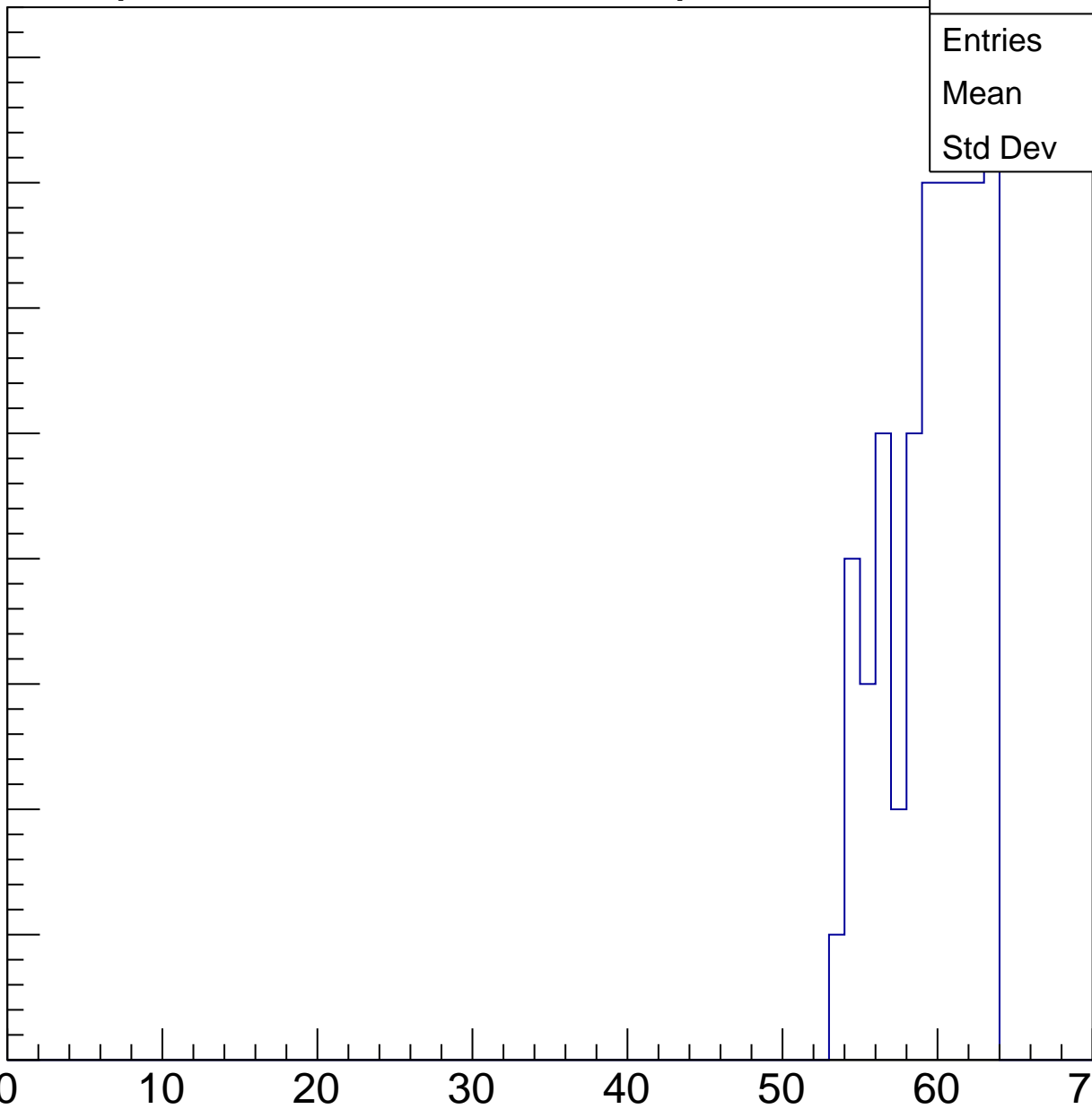
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	56
Mean	59.21
Std Dev	2.883

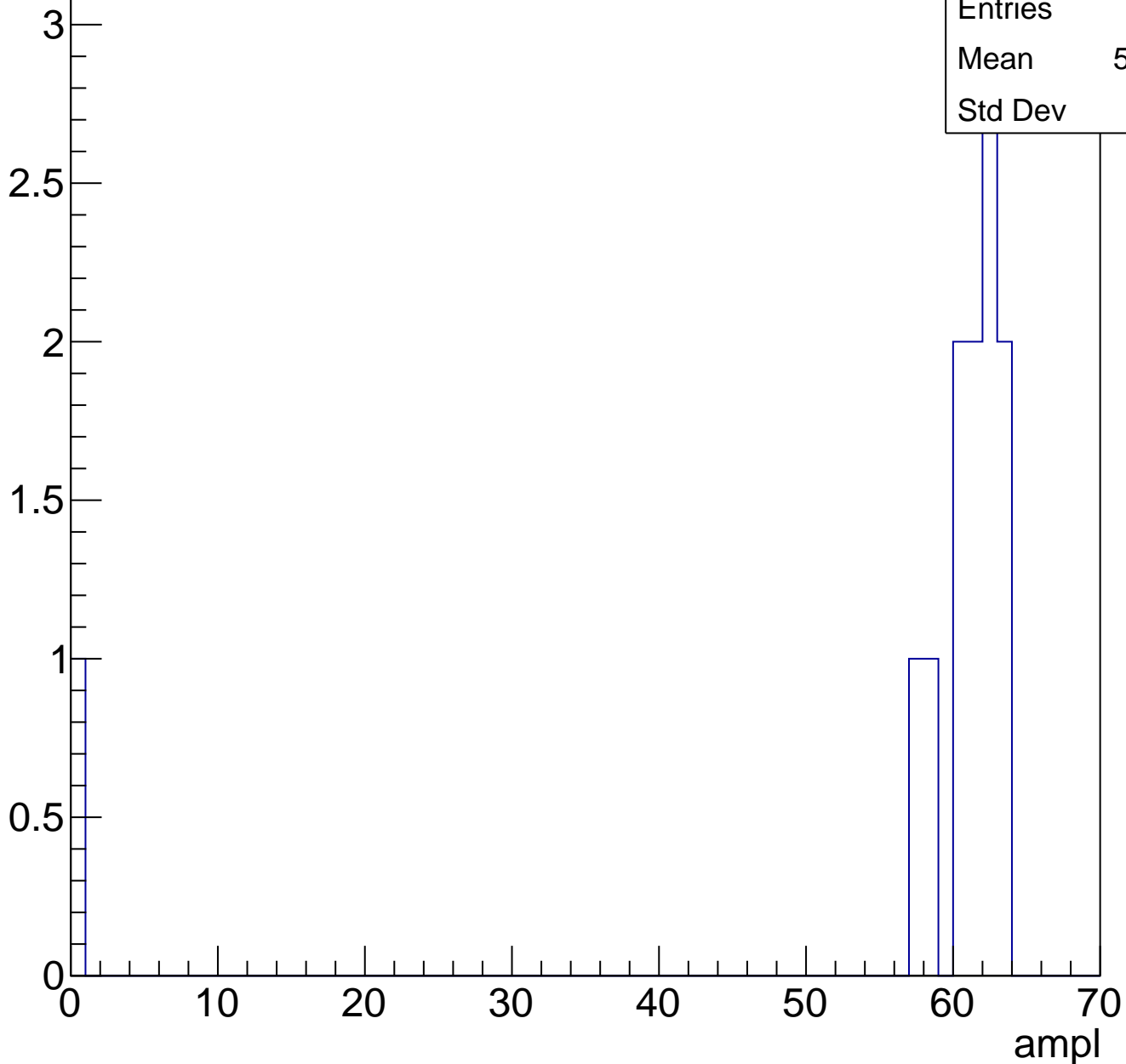
ampl



# B1L102S, U12-ch42, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

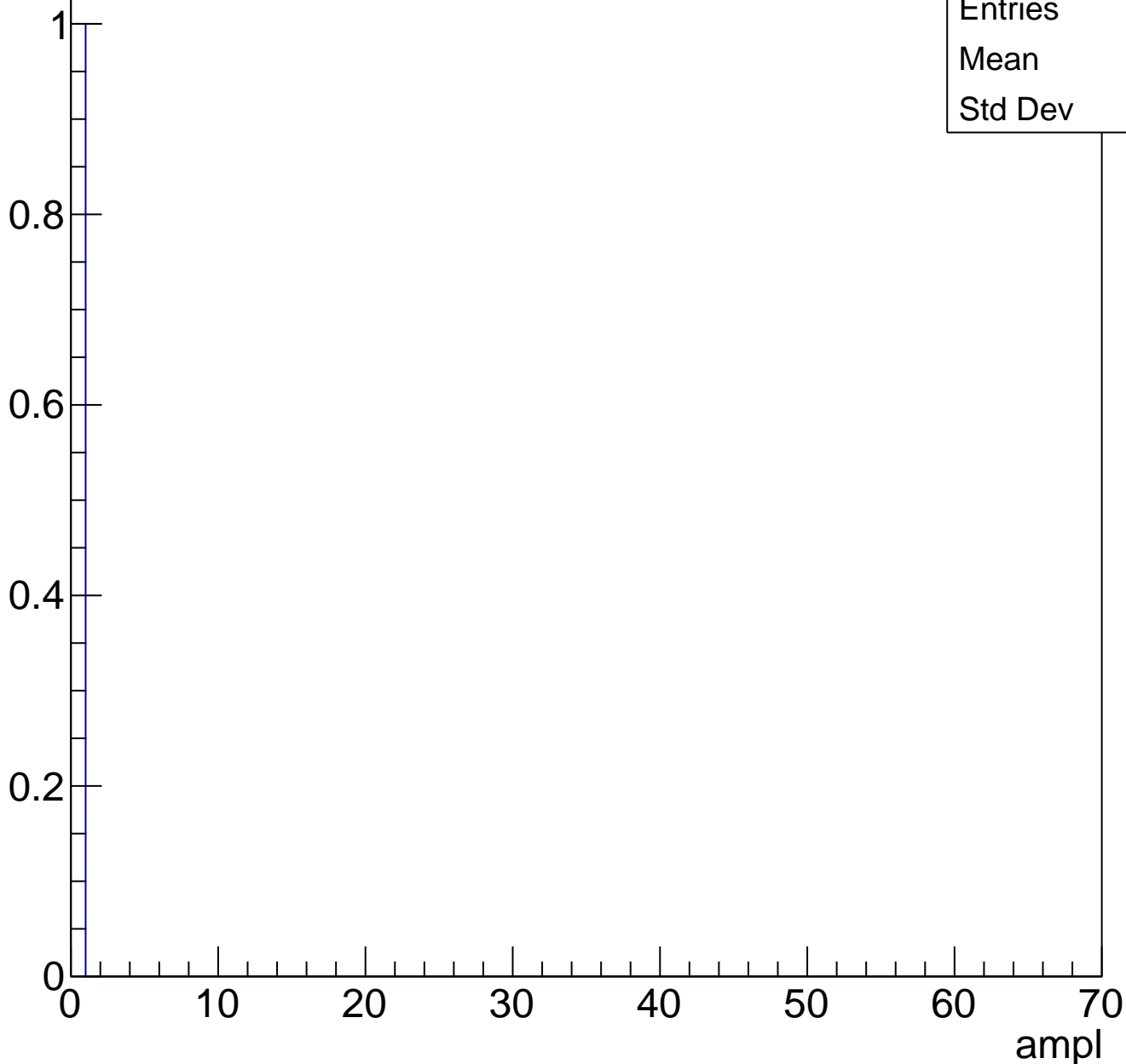




# B1L102S, U12-ch42, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U12-ch43, adc0

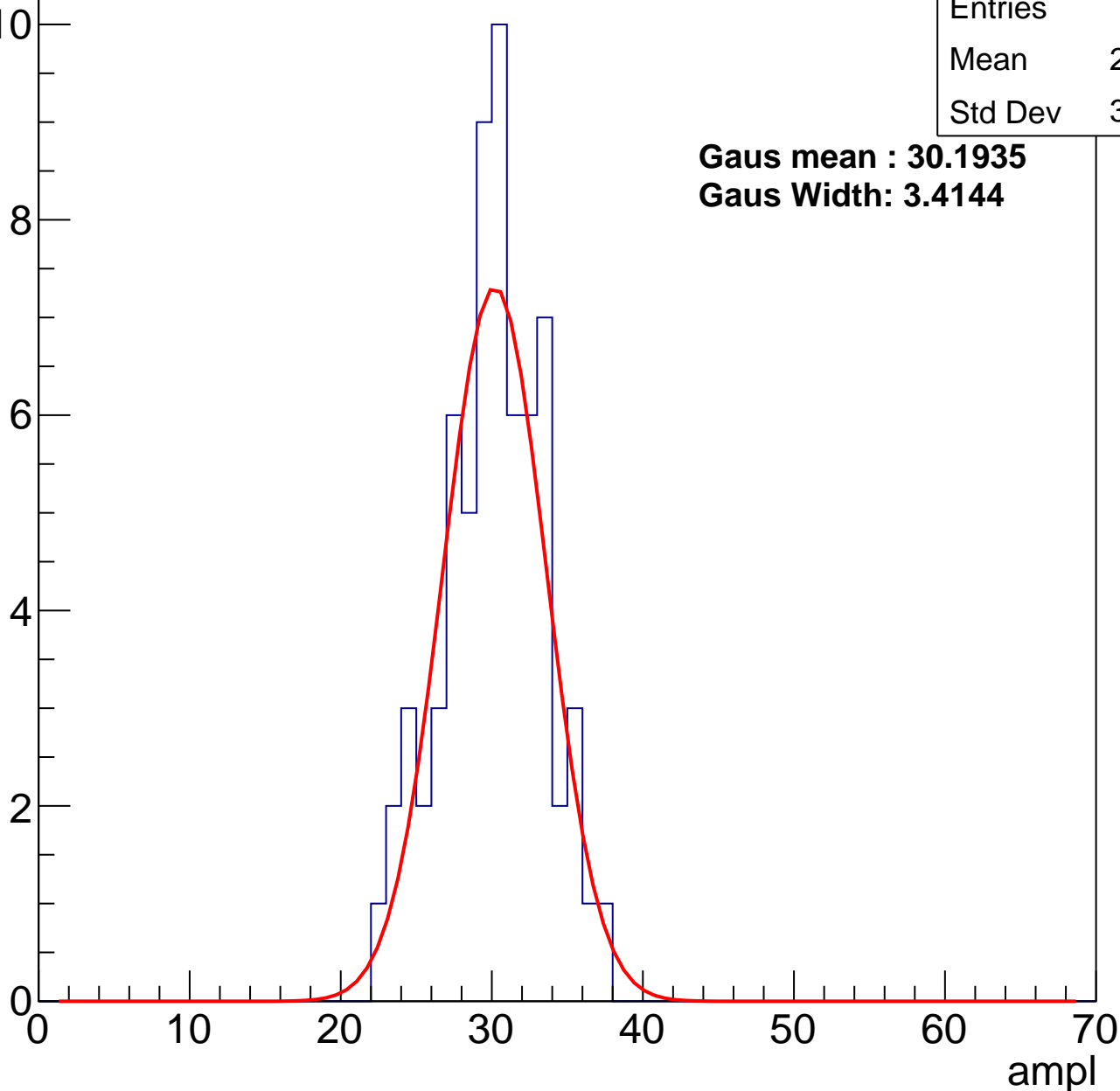
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	67
Mean	29.64
Std Dev	3.295

**Gaus mean : 30.1935**

**Gaus Width: 3.4144**



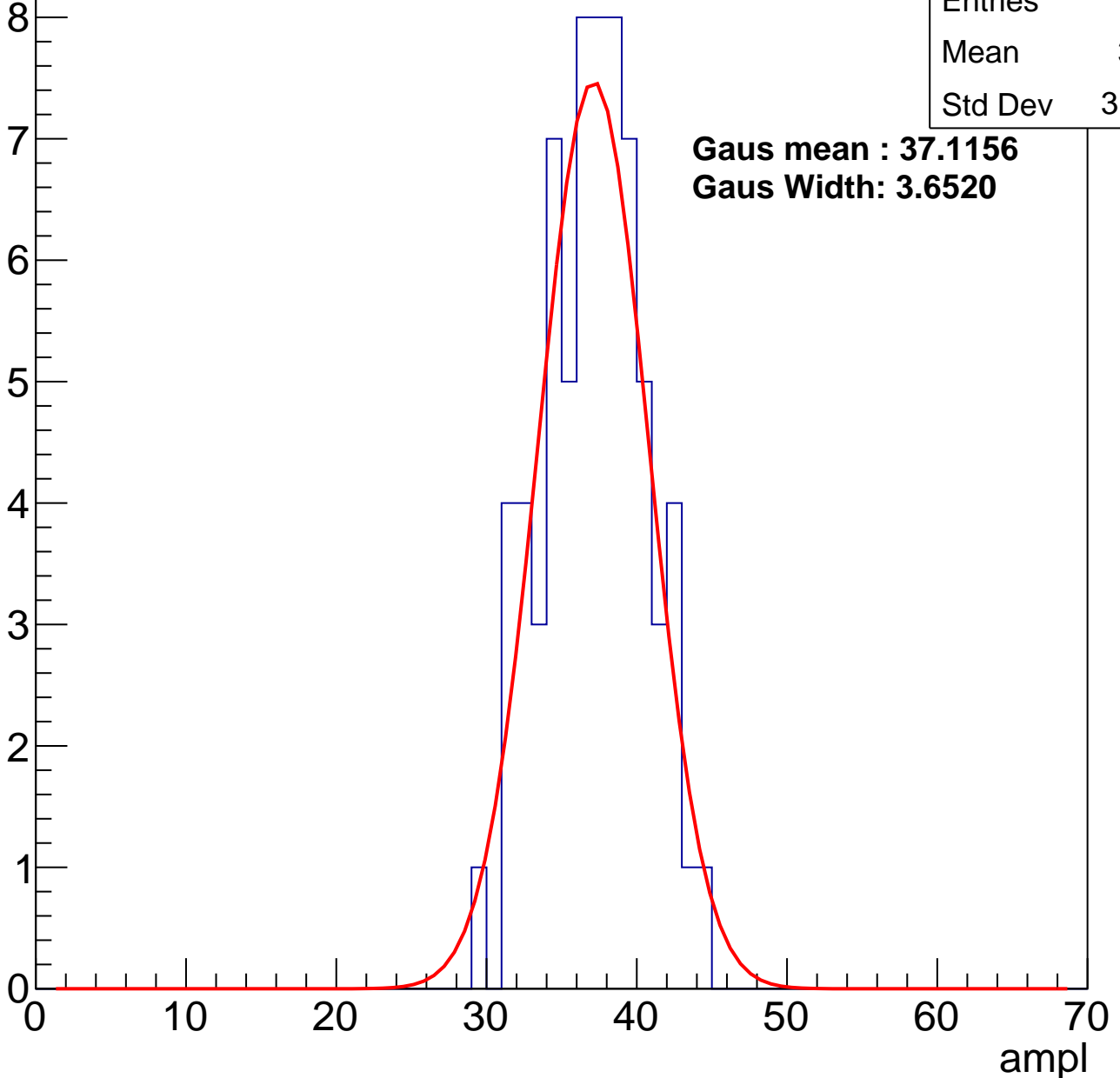
# B1L102S, U12-ch43, adc1

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	36.7
Std Dev	3.307

**Gaus mean : 37.1156**  
**Gaus Width: 3.6520**

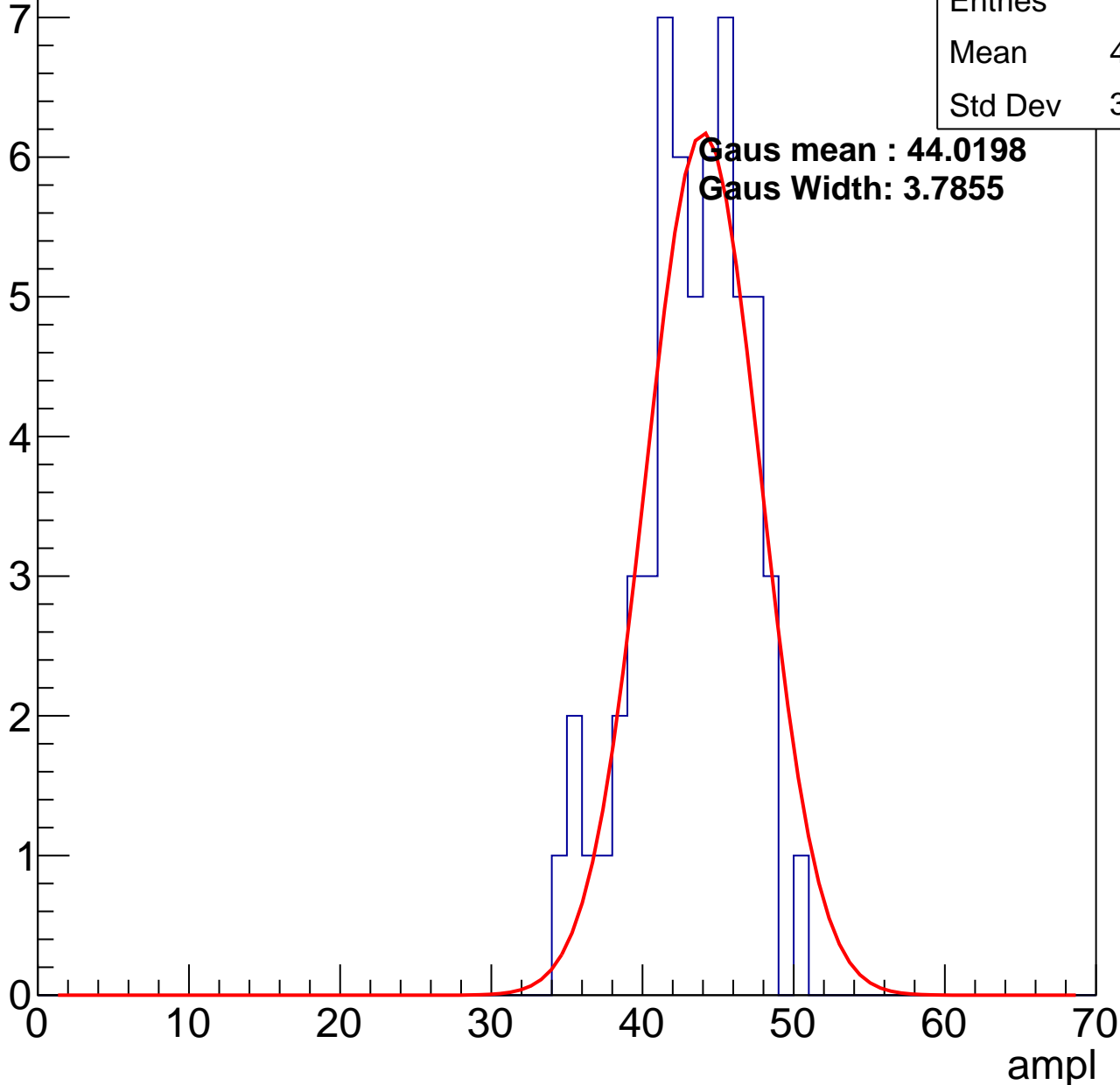


# B1L102S, U12-ch43, adc2

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	58
Mean	42.79
Std Dev	3.556

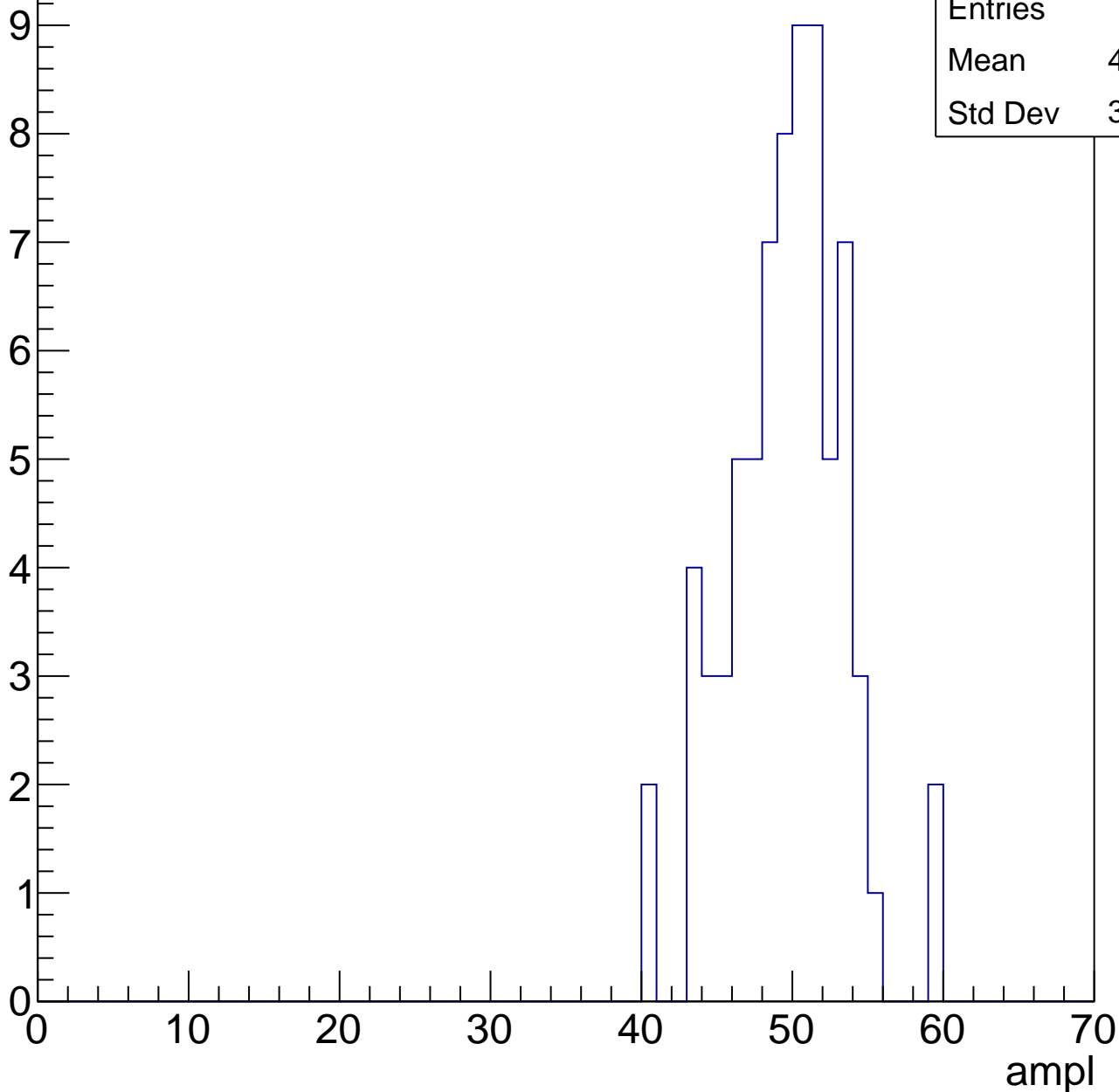


# B1L102S, U12-ch43, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	73
Mean	49.14
Std Dev	3.724

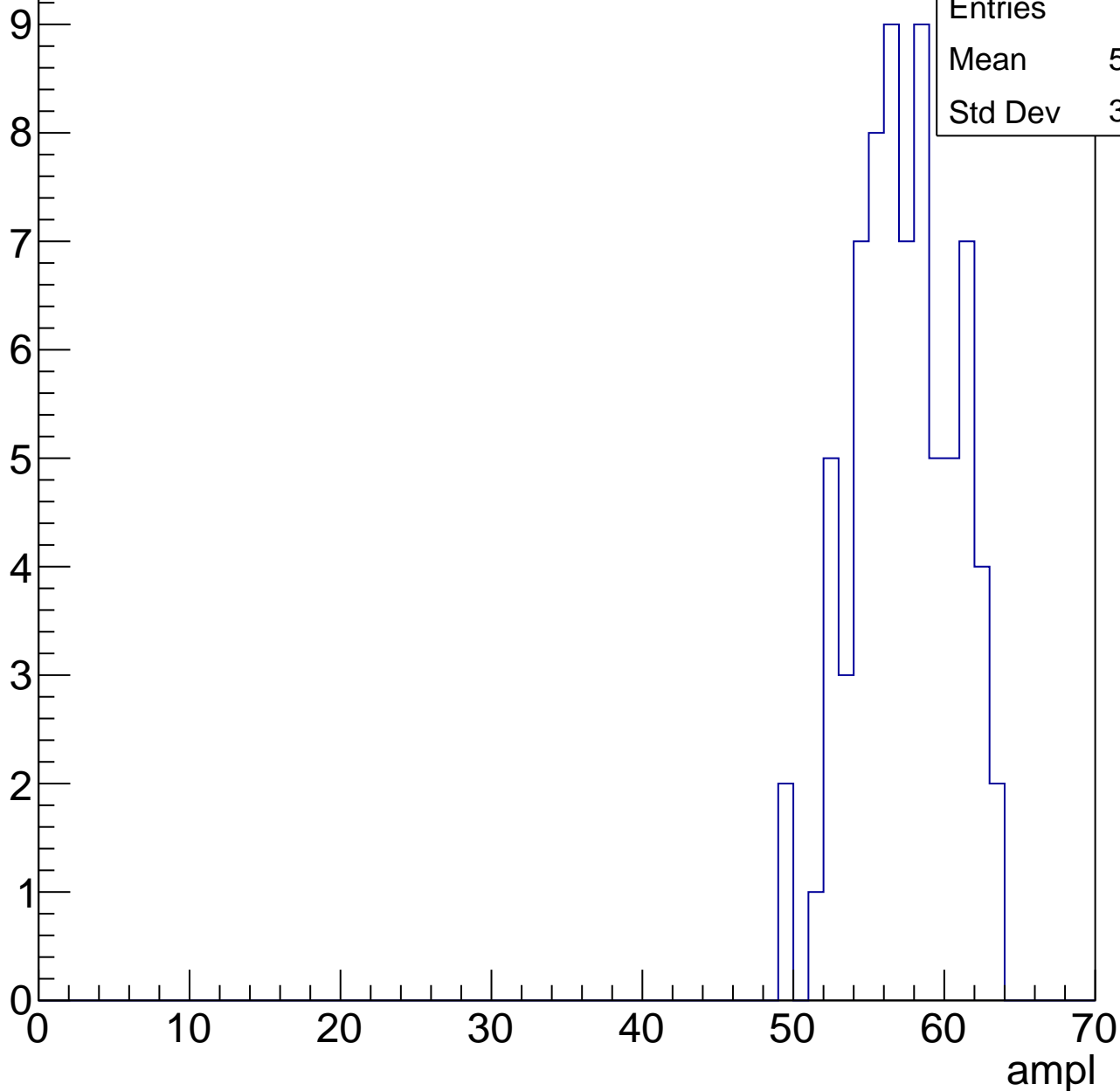


# B1L102S, U12-ch43, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	74
Mean	56.85
Std Dev	3.283

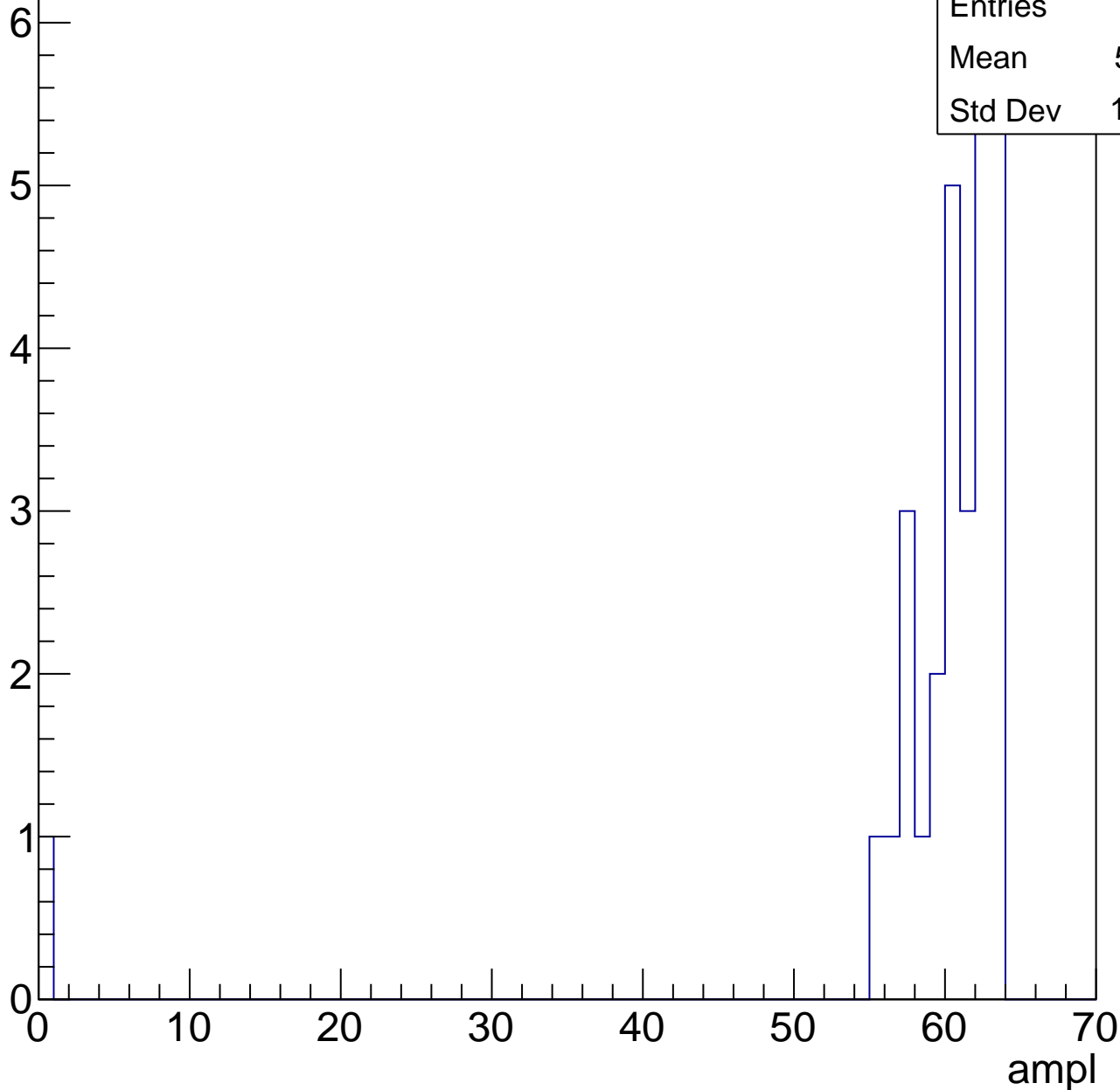


# B1L102S, U12-ch43, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	29
Mean	58.31
Std Dev	11.25



# B1L102S, U12-ch43, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U12-ch43, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L102S, U12-ch44, adc0

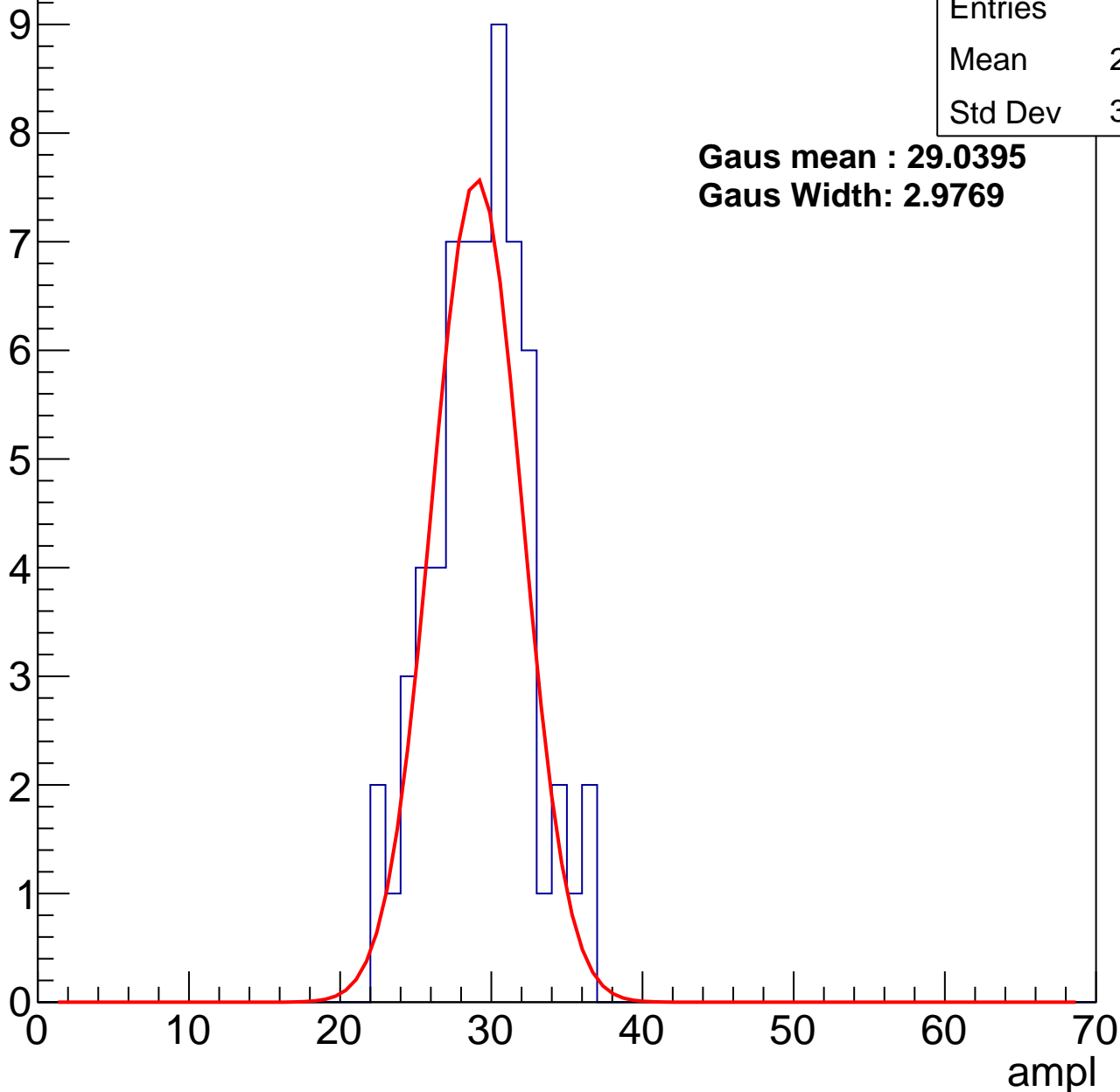
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	63
Mean	28.86
Std Dev	3.172

**Gaus mean : 29.0395**

**Gaus Width: 2.9769**



# B1L102S, U12-ch44, adc1

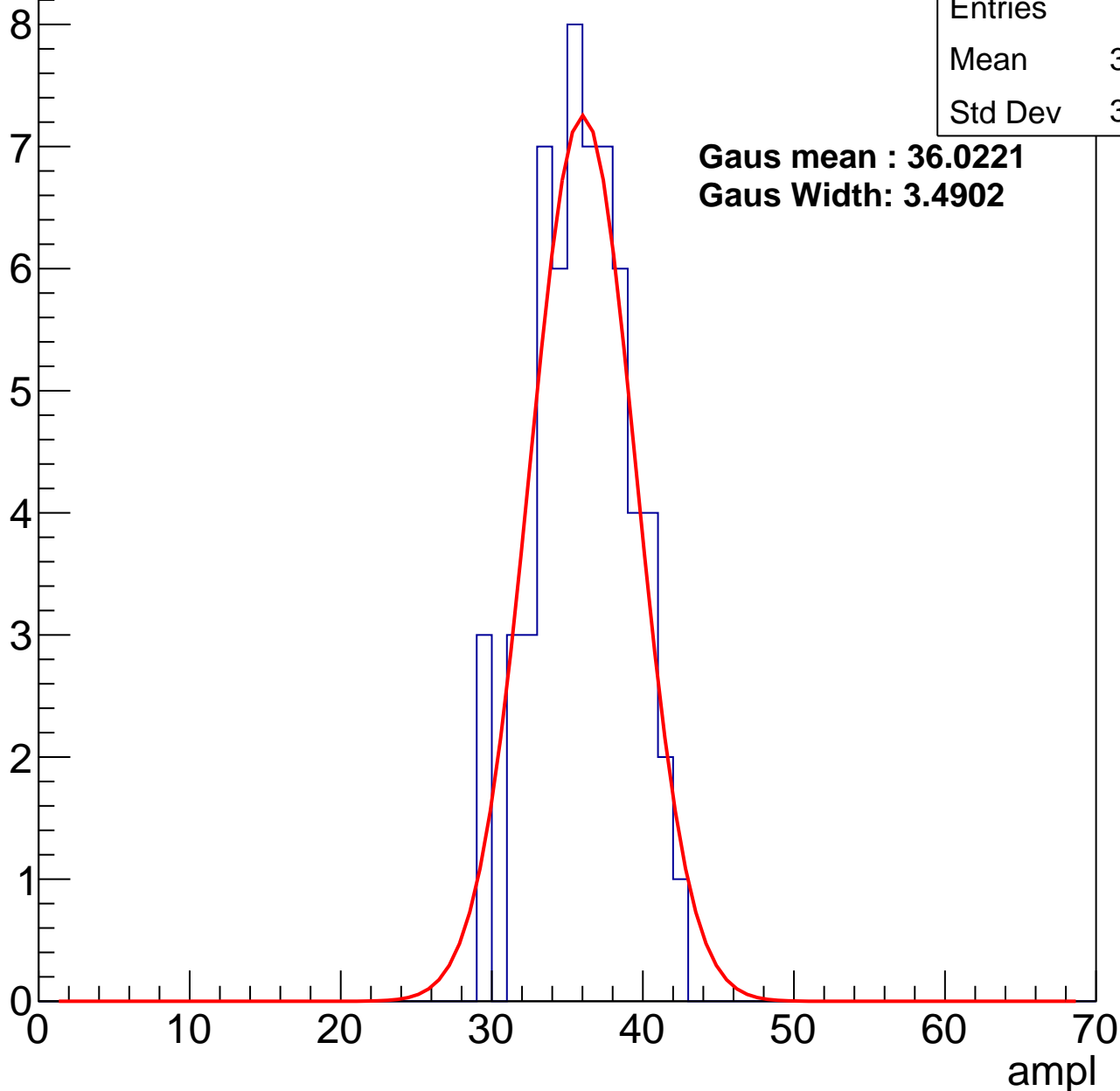
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	35.57
Std Dev	3.059

**Gaus mean : 36.0221**

**Gaus Width: 3.4902**



# B1L102S, U12-ch44, adc2

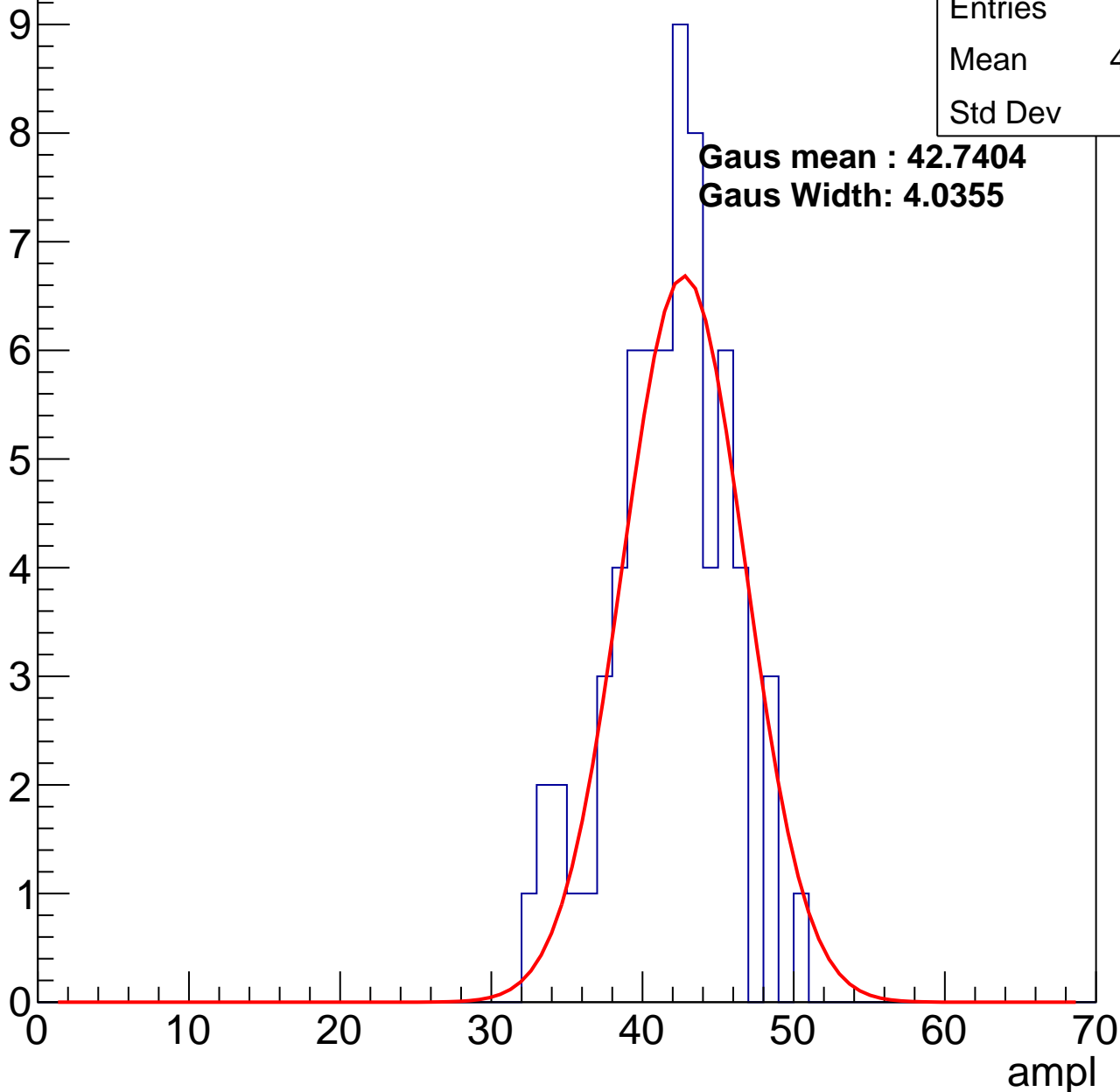
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	67
Mean	41.28
Std Dev	3.82

**Gaus mean : 42.7404**

**Gaus Width: 4.0355**

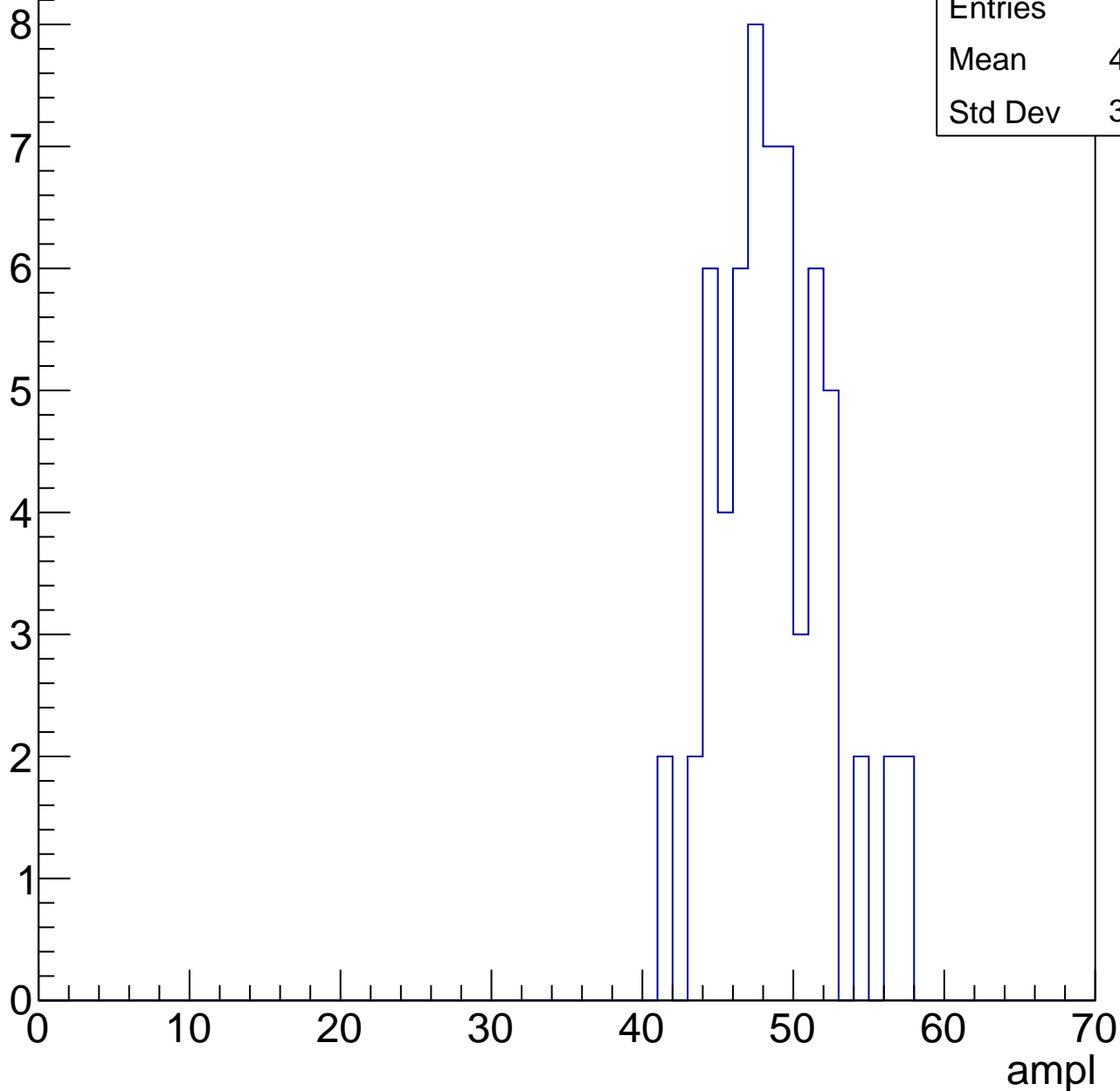


# B1L102S, U12-ch44, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	62
Mean	48.27
Std Dev	3.642

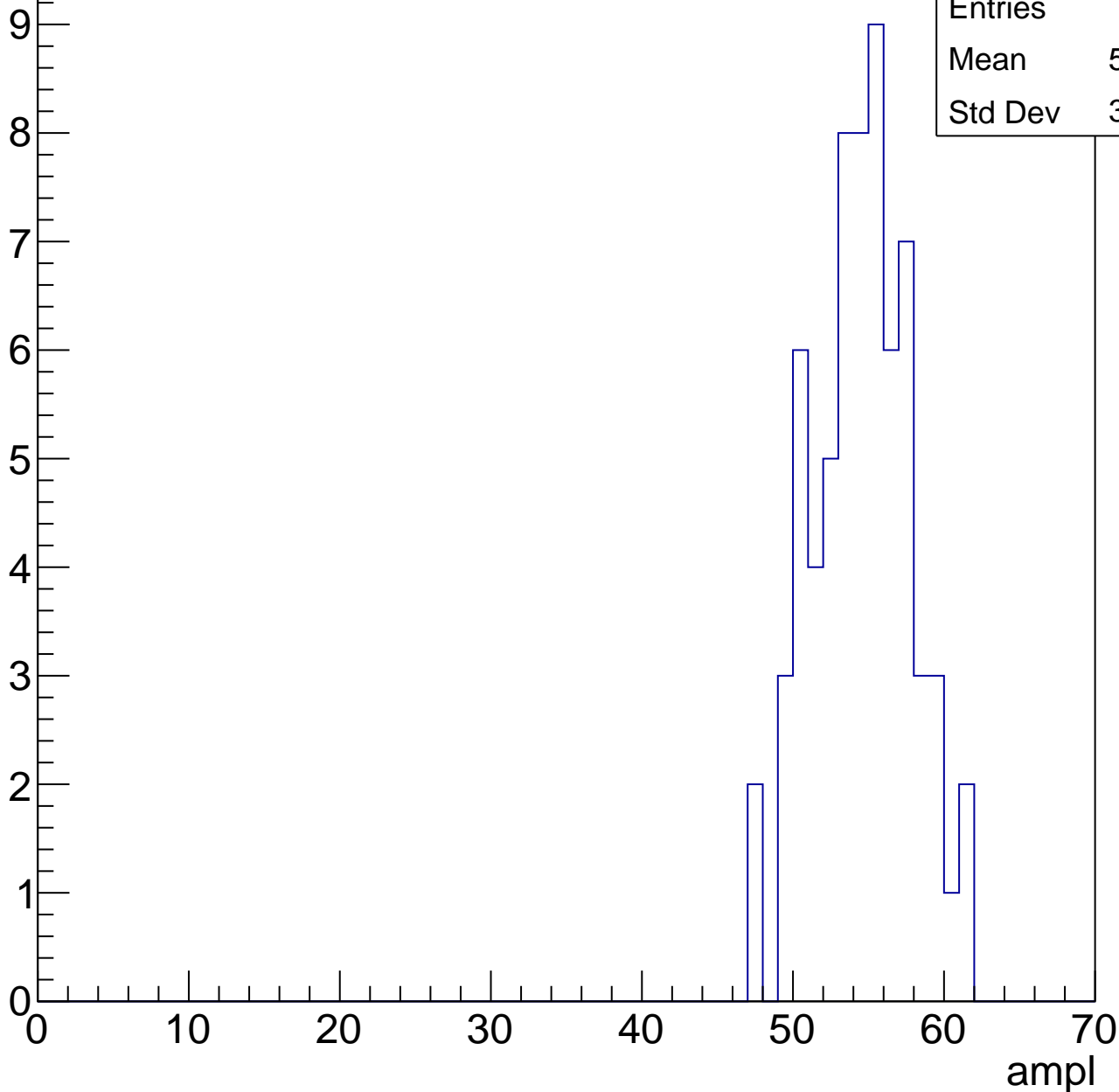


# B1L102S, U12-ch44, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	67
Mean	54.09
Std Dev	3.199

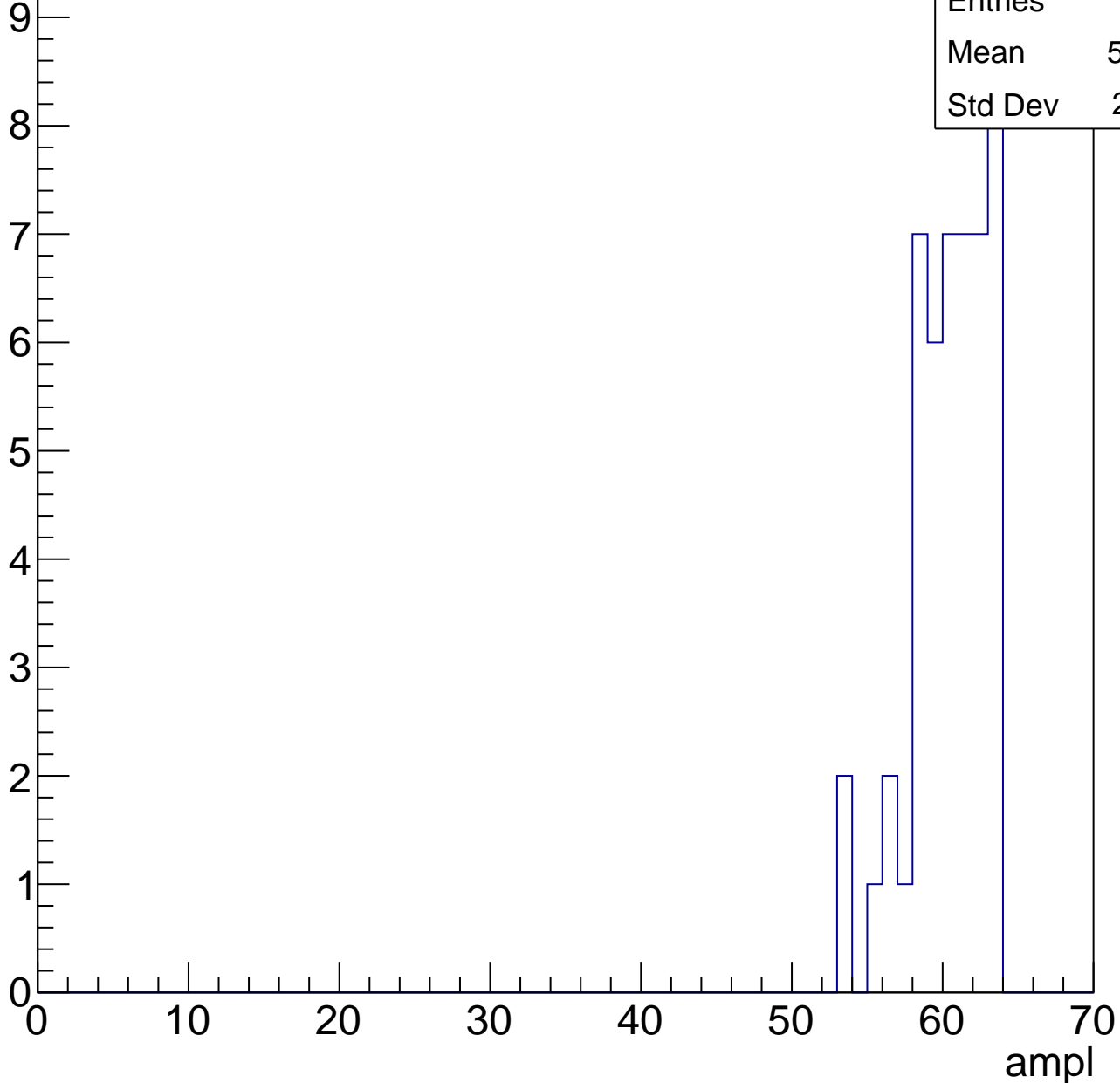


# B1L102S, U12-ch44, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

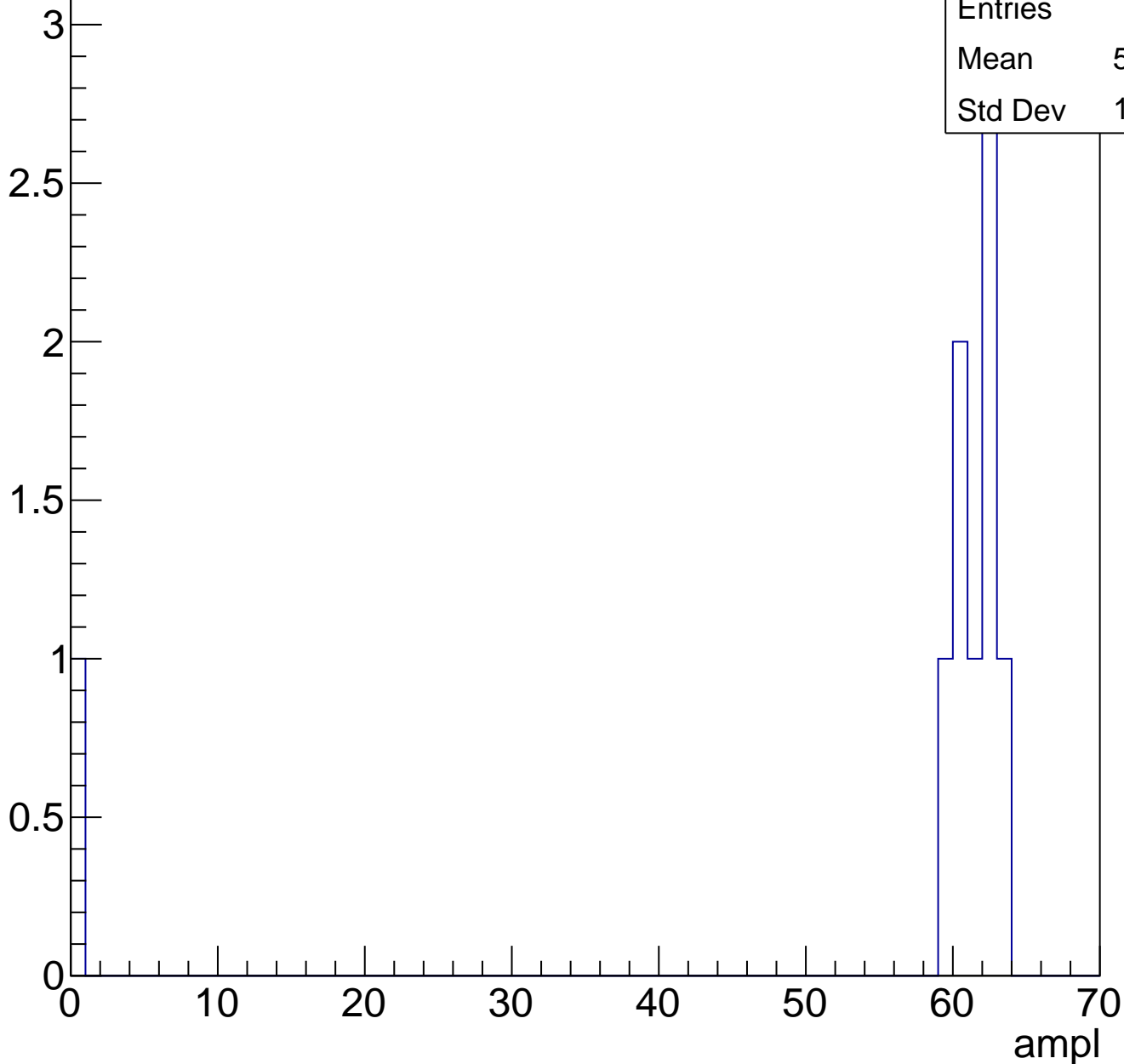
Entries	49
Mean	59.96
Std Dev	2.531



# B1L102S, U12-ch44, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U12-ch44, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	2
Mean	11
Std Dev	11

# B1L102S, U12-ch45, adc0

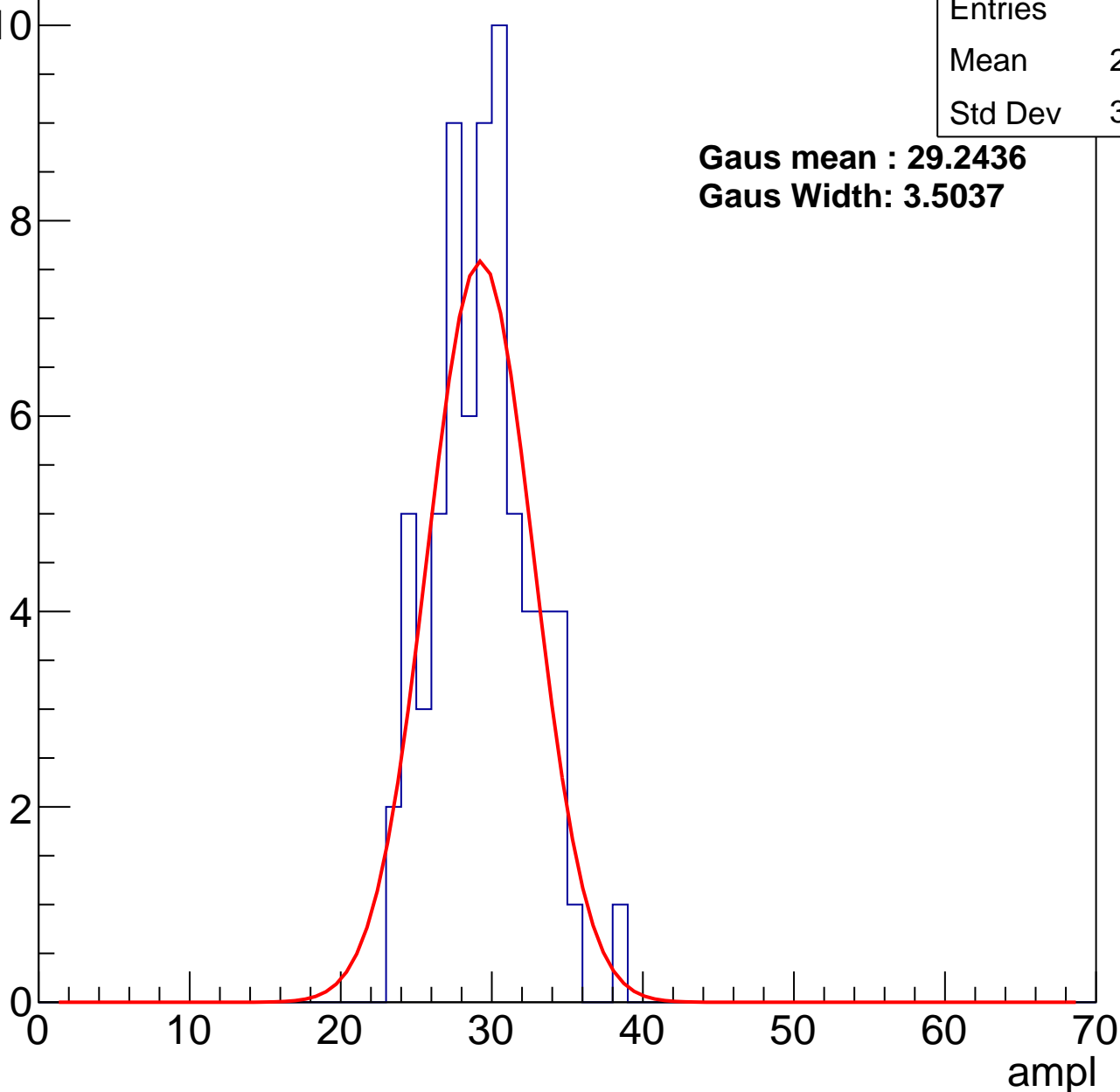
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	28.93
Std Dev	3.159

**Gaus mean : 29.2436**

**Gaus Width: 3.5037**



# B1L102S, U12-ch45, adc1

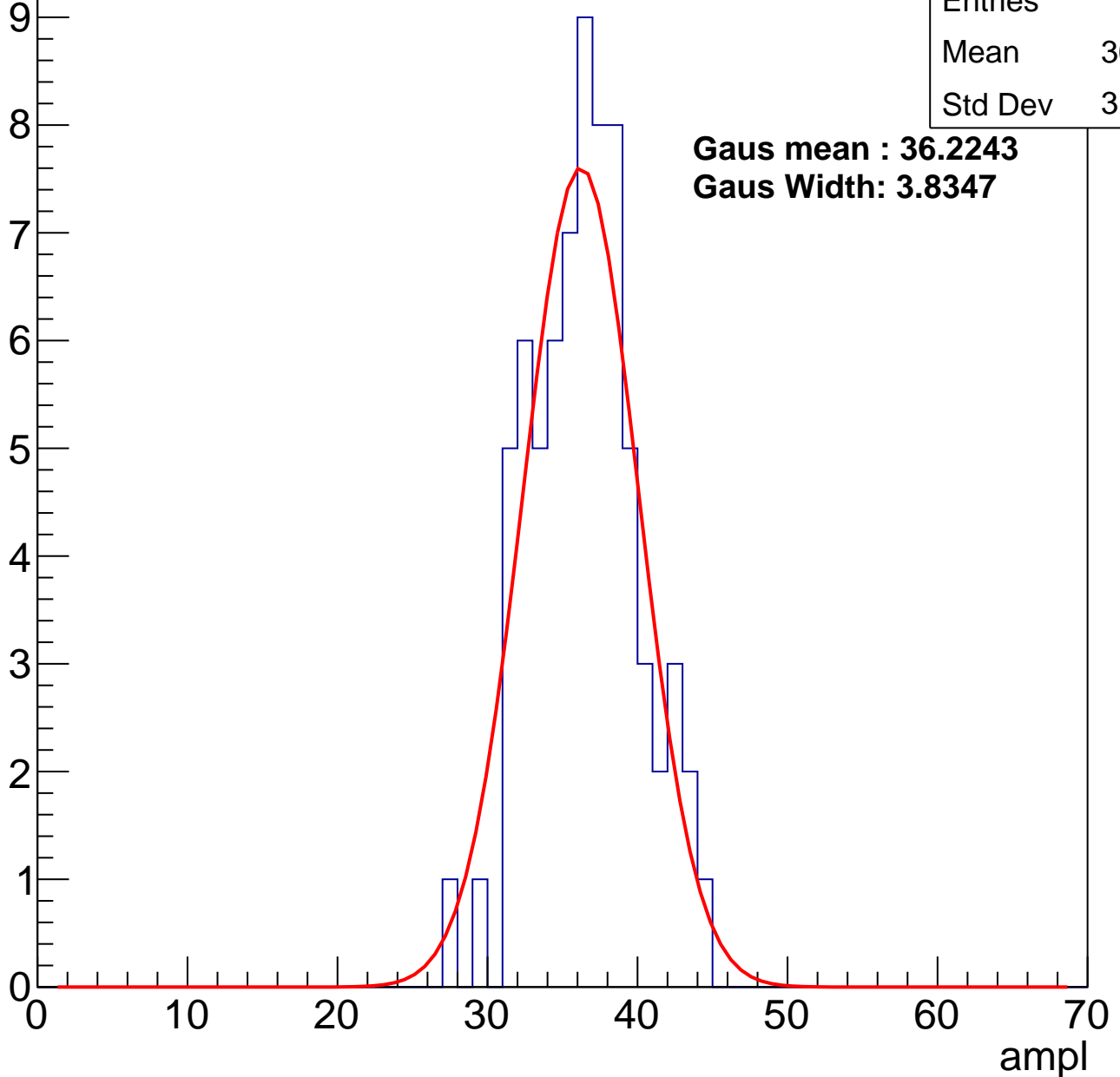
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	72
Mean	36.03
Std Dev	3.496

**Gaus mean : 36.2243**

**Gaus Width: 3.8347**



# B1L102S, U12-ch45, adc2

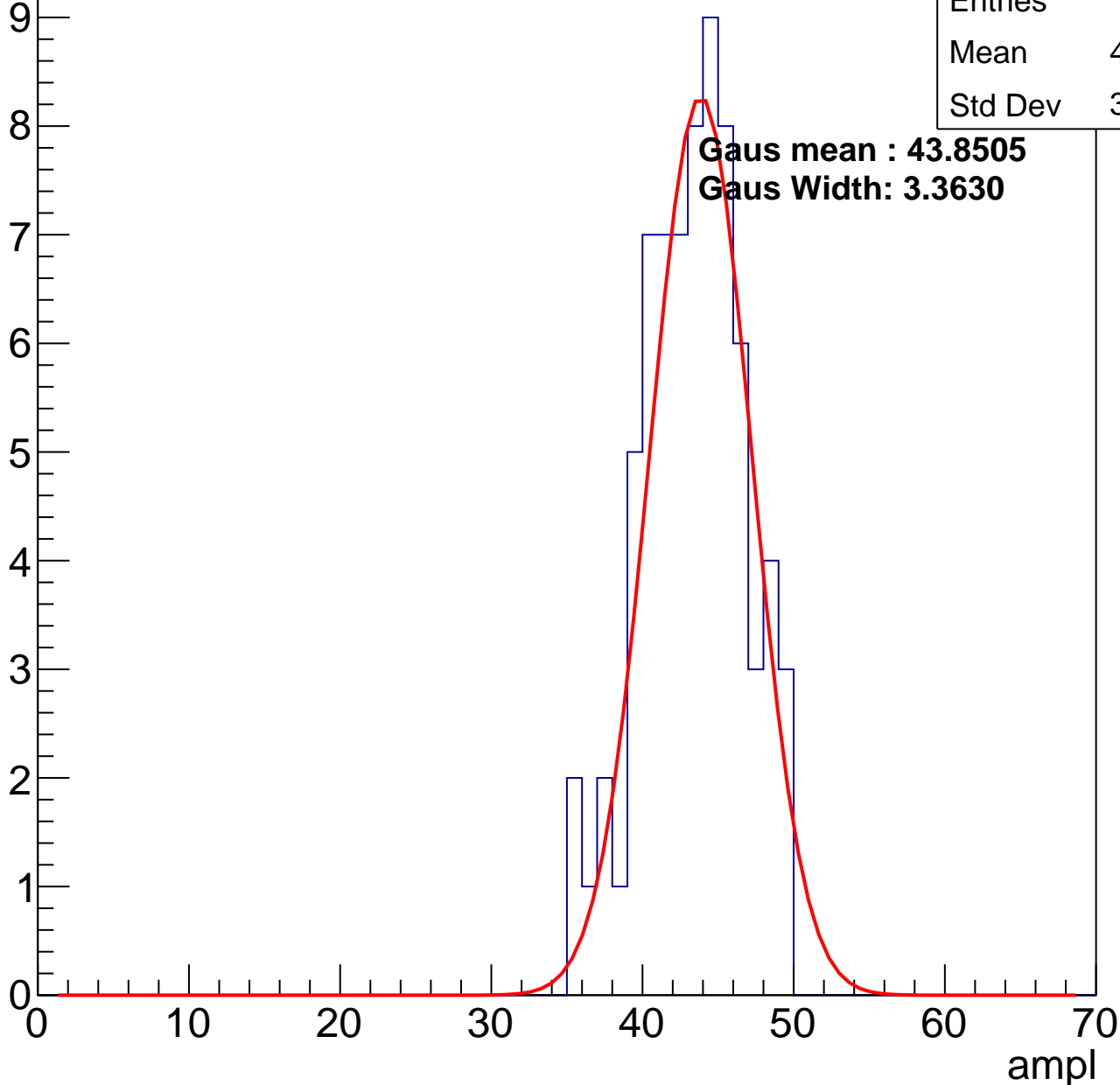
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	73
Mean	42.88
Std Dev	3.314

**Gaus mean : 43.8505**

**Gaus Width: 3.3630**

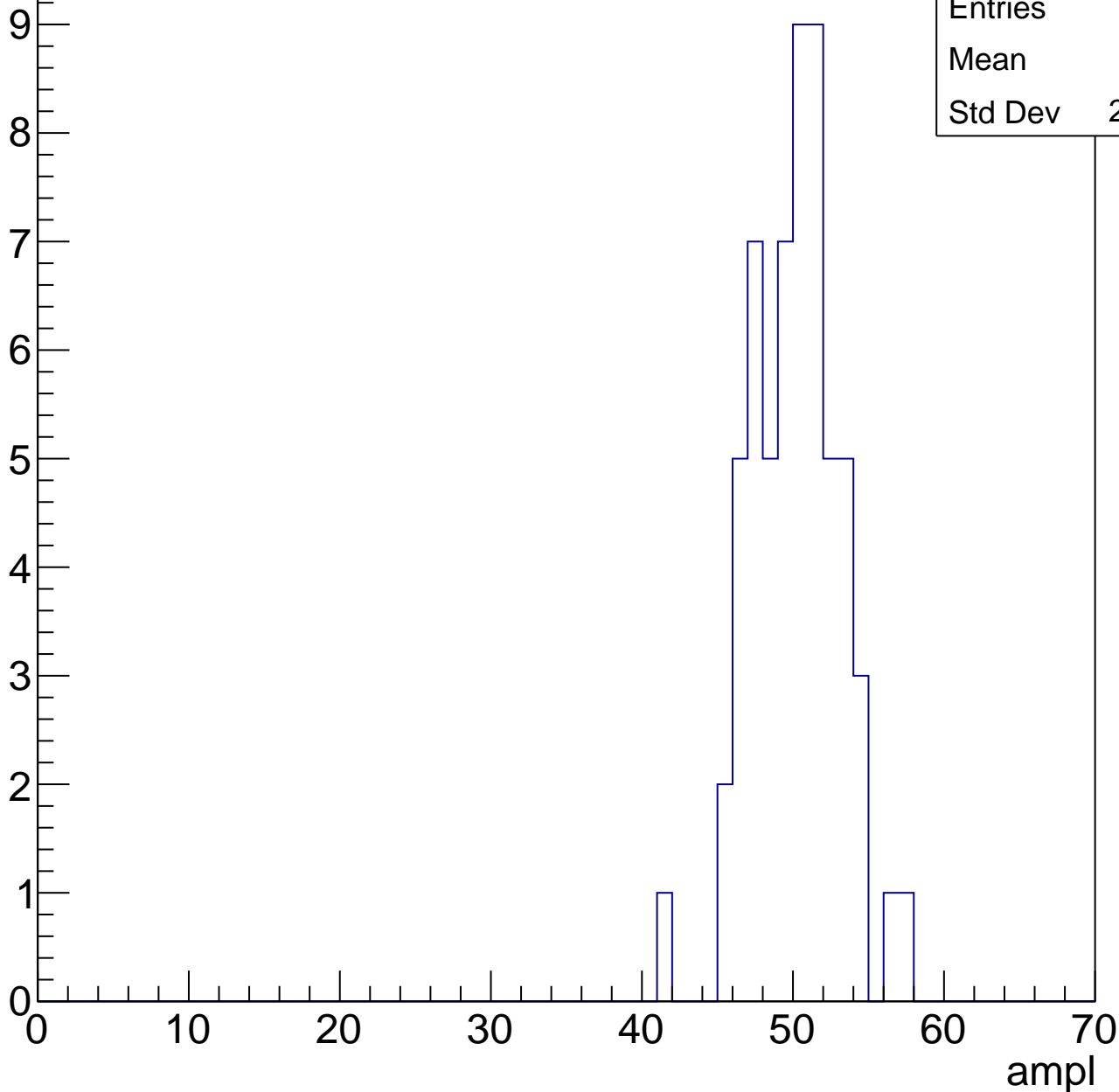


# B1L102S, U12-ch45, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

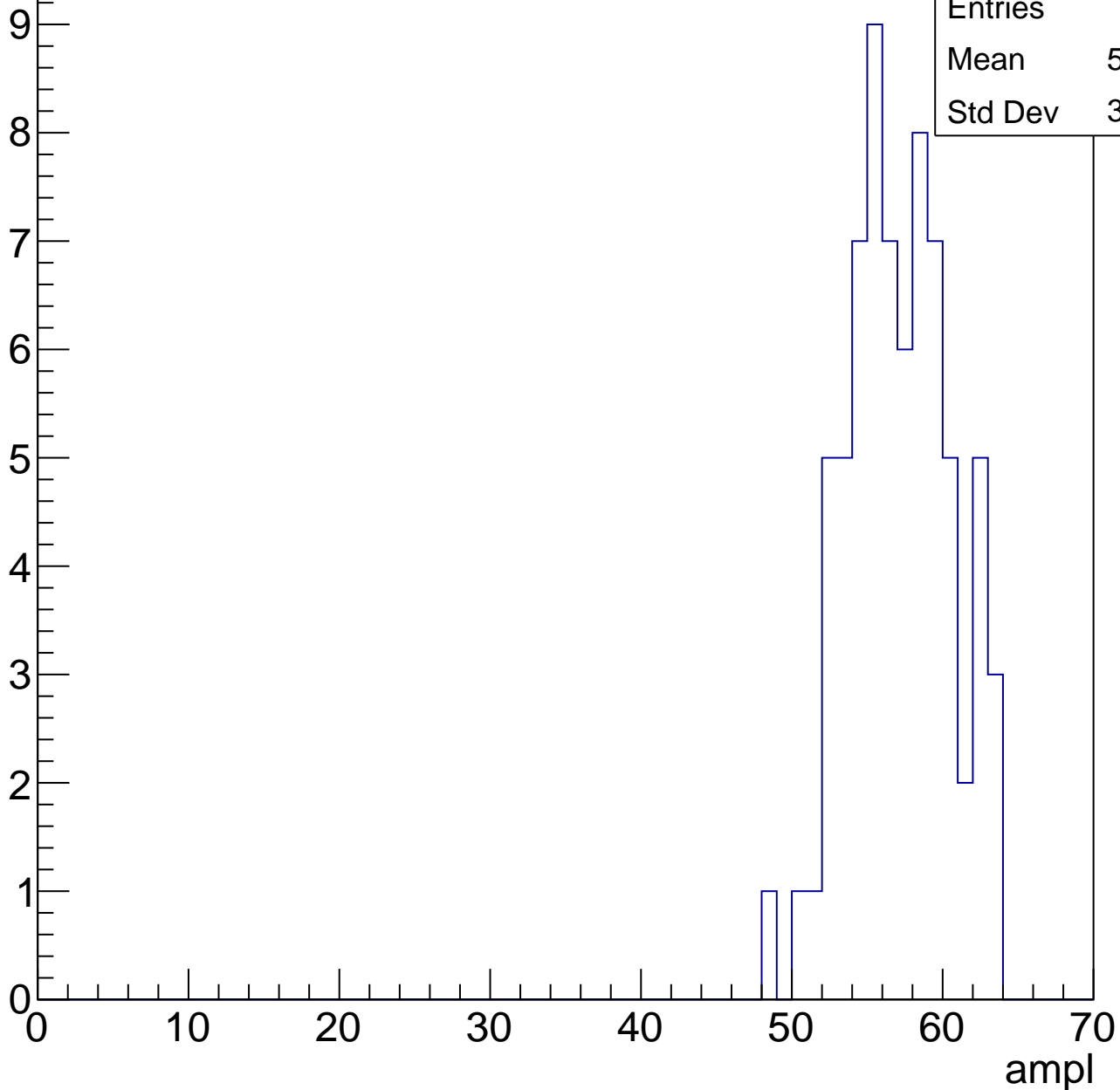
Entries	60
Mean	49.7
Std Dev	2.894



# B1L102S, U12-ch45, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



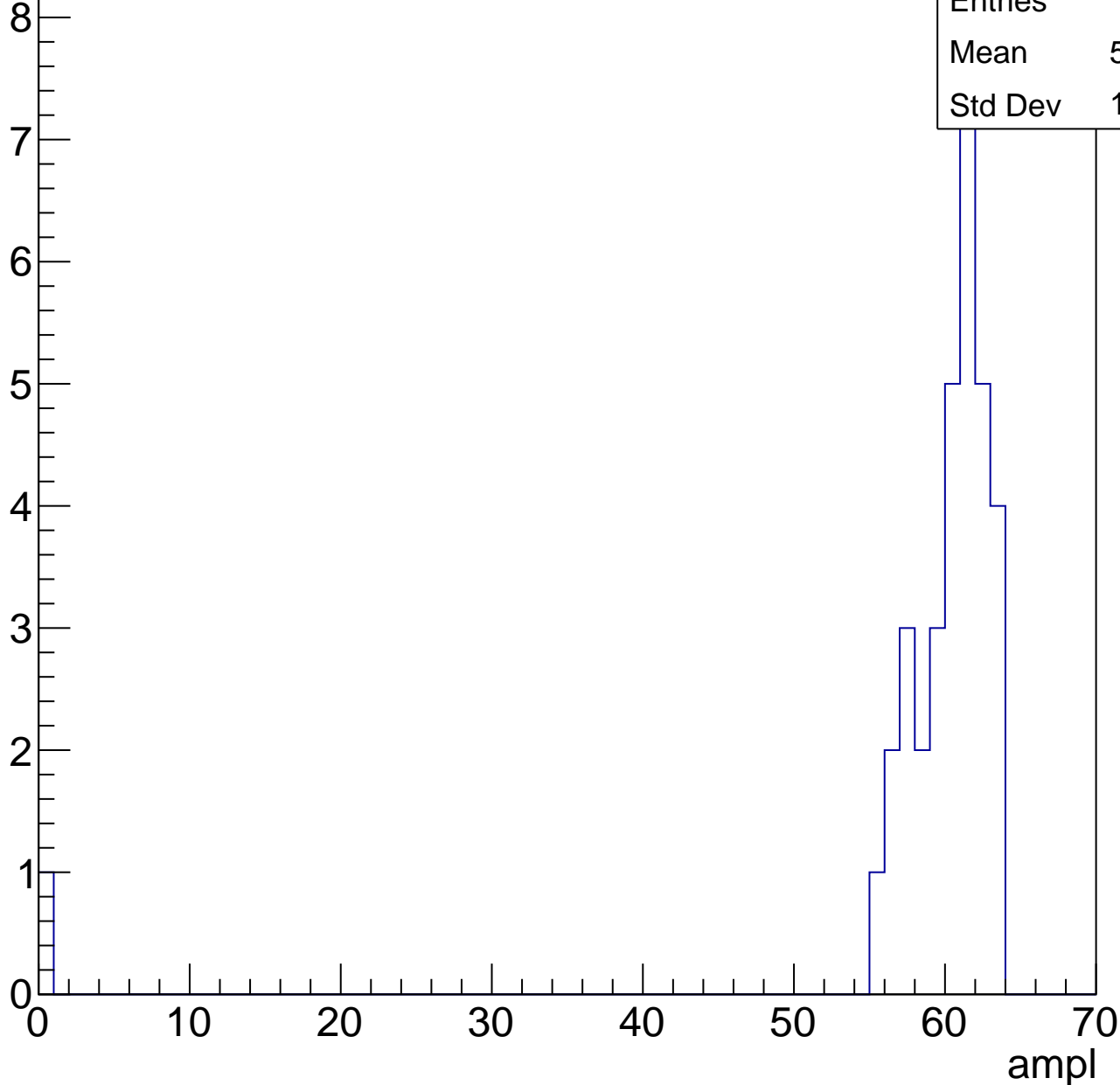
Entries	72
Mean	56.65
Std Dev	3.363

# B1L102S, U12-ch45, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	34
Mean	58.26
Std Dev	10.37



# B1L102S, U12-ch45, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U12-ch45, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U12-ch46, adc0

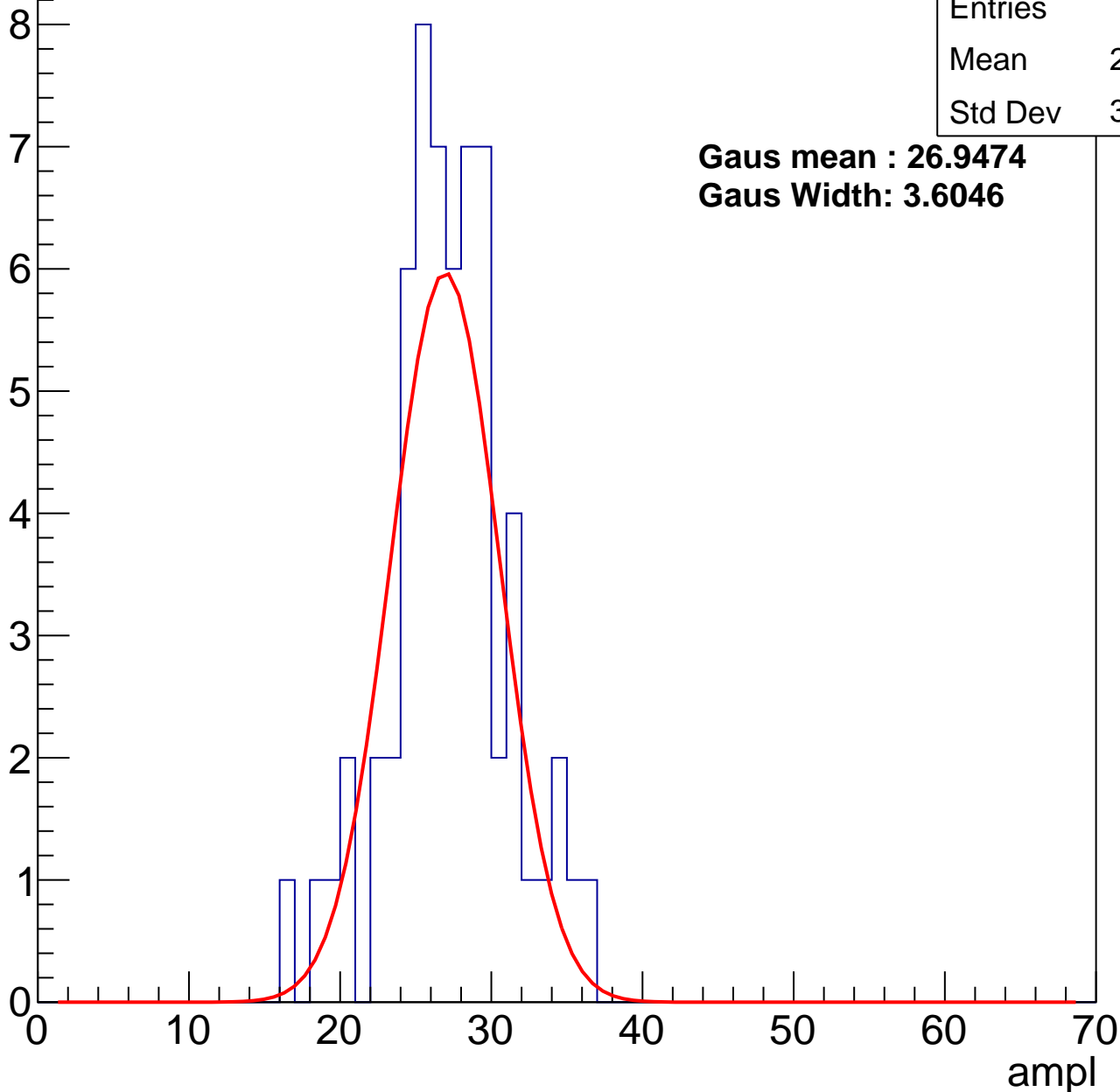
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	62
Mean	26.74
Std Dev	3.926

**Gaus mean : 26.9474**

**Gaus Width: 3.6046**



# B1L102S, U12-ch46, adc1

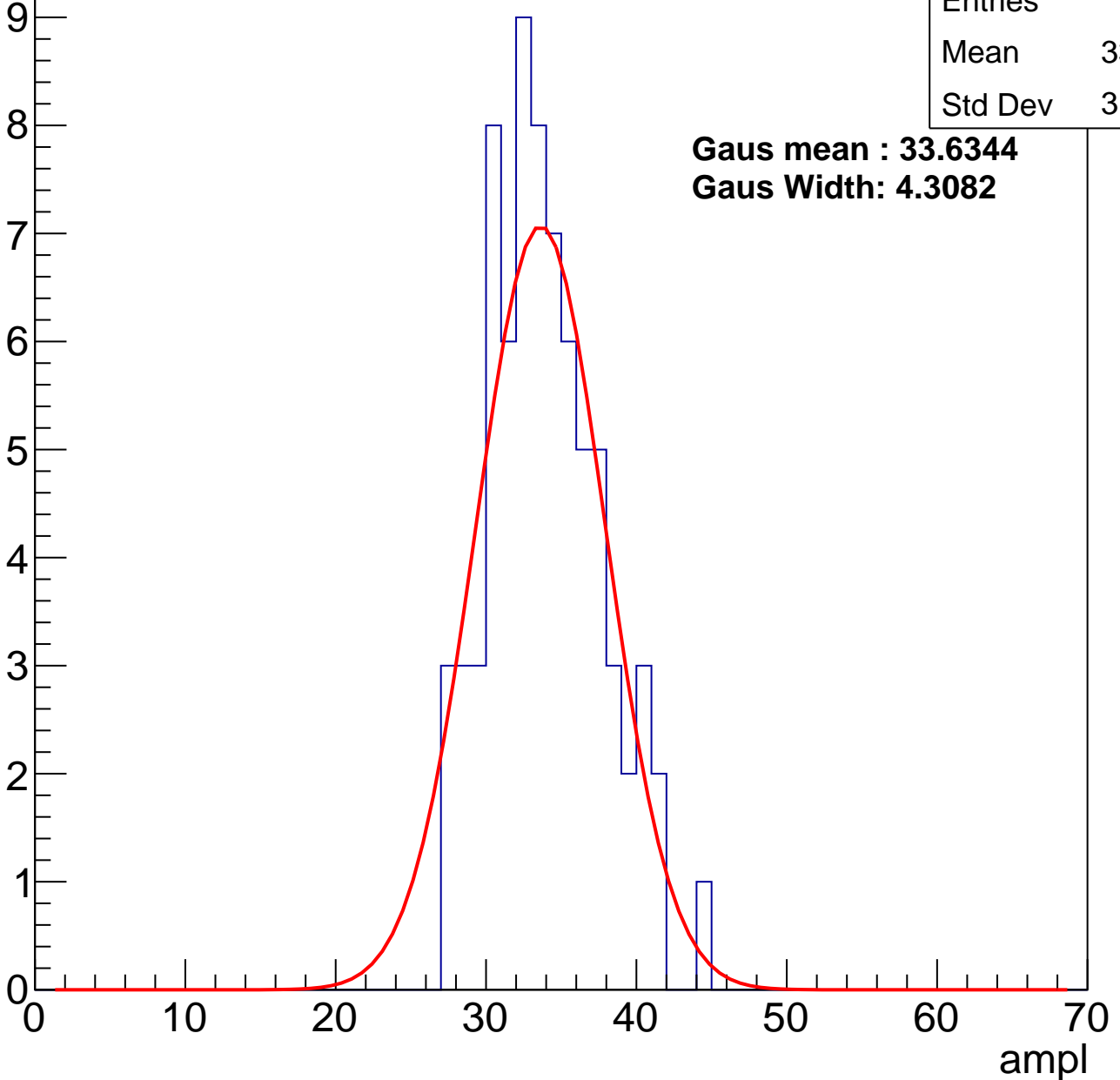
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	74
Mean	33.53
Std Dev	3.703

**Gaus mean : 33.6344**

**Gaus Width: 4.3082**



# B1L102S, U12-ch46, adc2

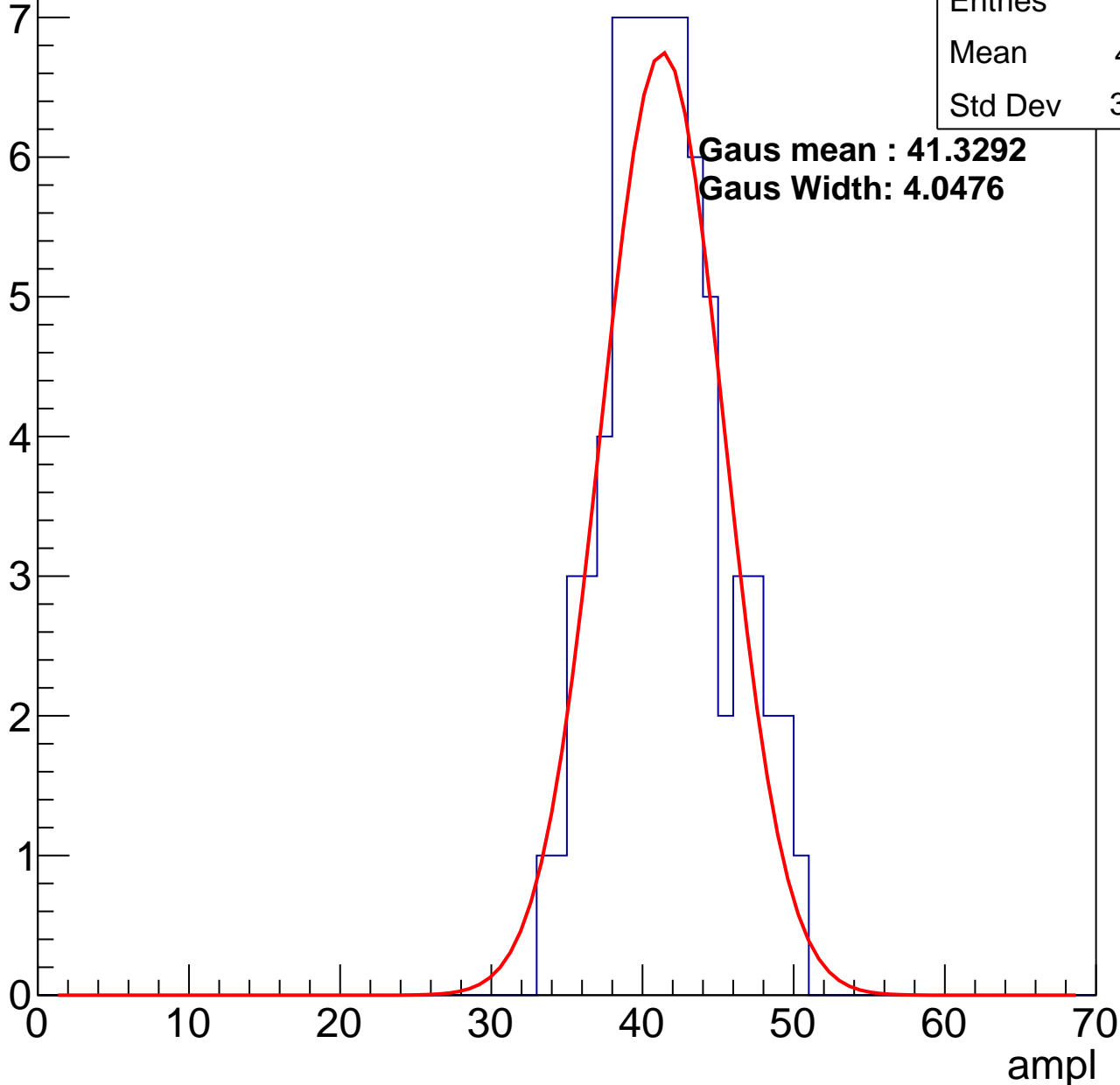
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	71
Mean	41.11
Std Dev	3.855

**Gaus mean : 41.3292**

**Gaus Width: 4.0476**

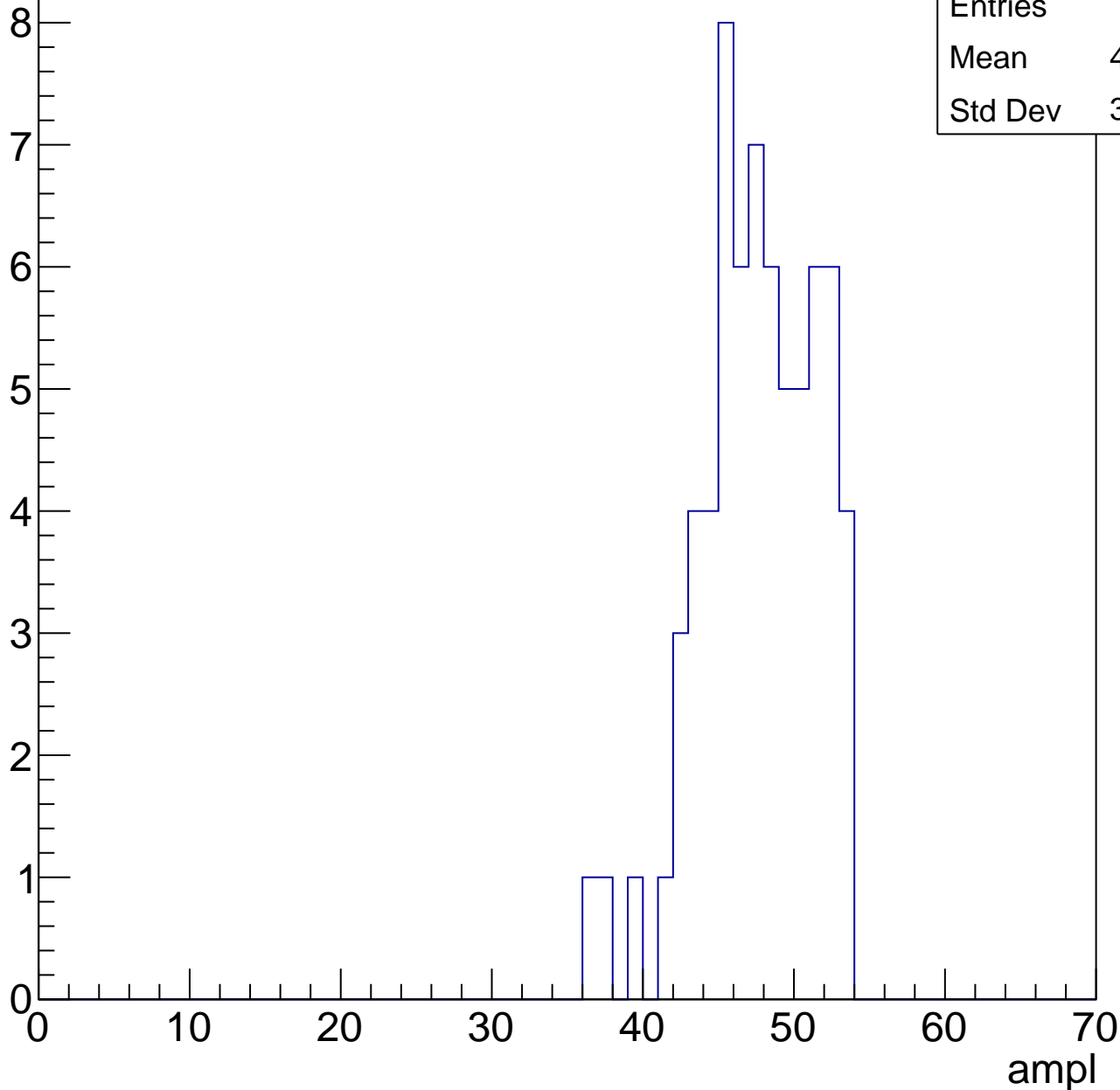


# B1L102S, U12-ch46, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	47.13
Std Dev	3.823

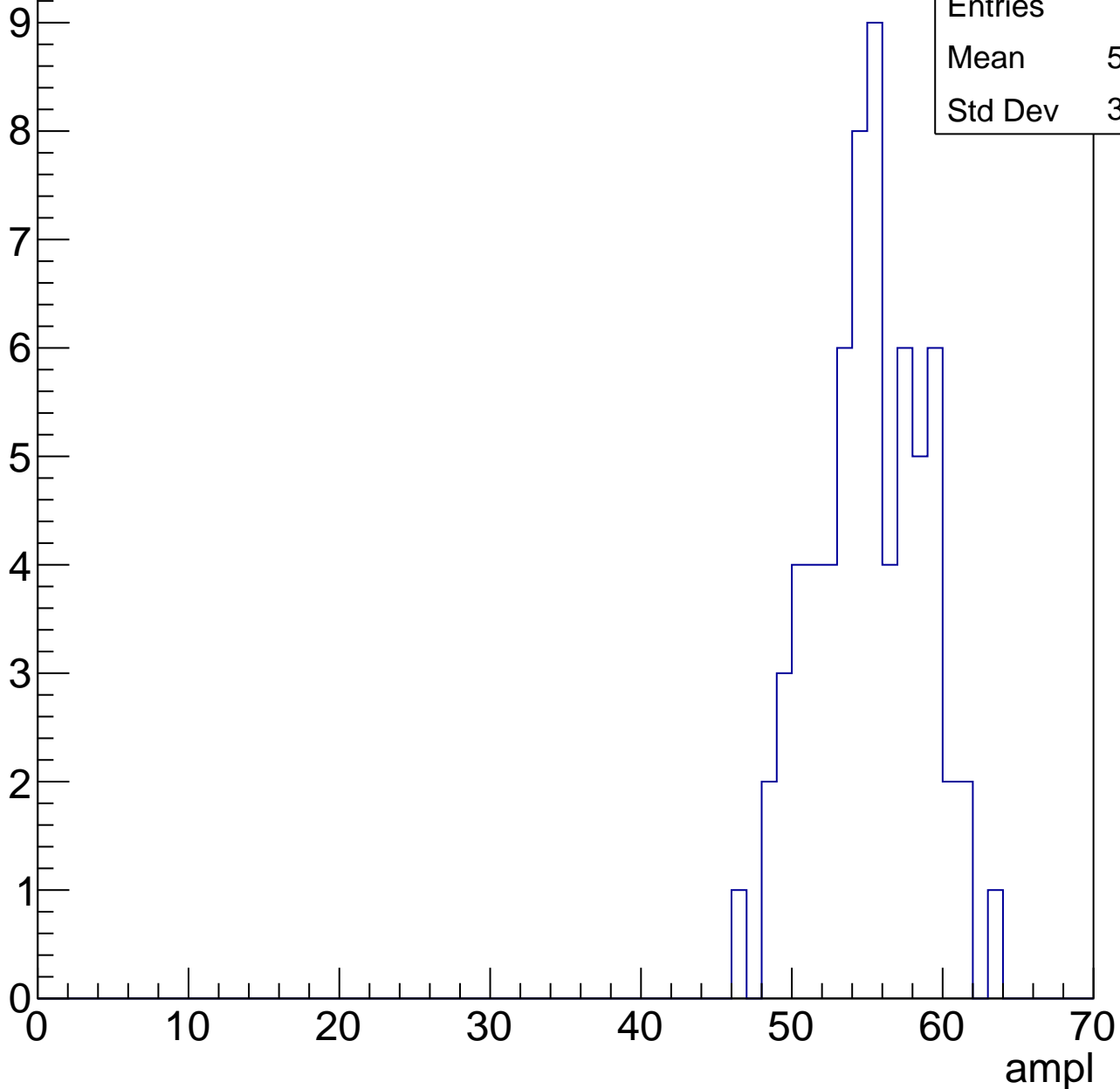


# B1L102S, U12-ch46, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	67
Mean	54.64
Std Dev	3.594

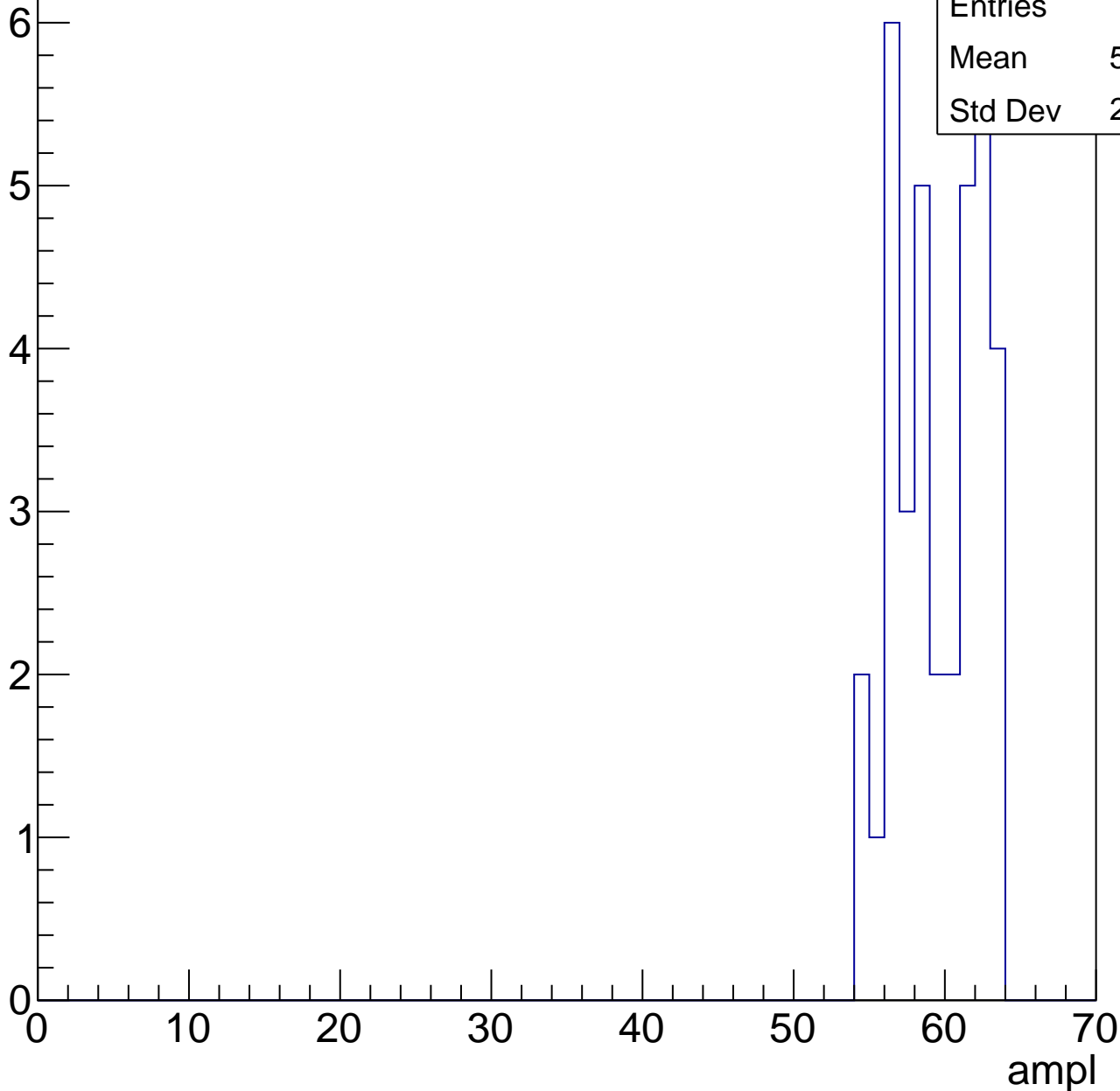


# B1L102S, U12-ch46, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

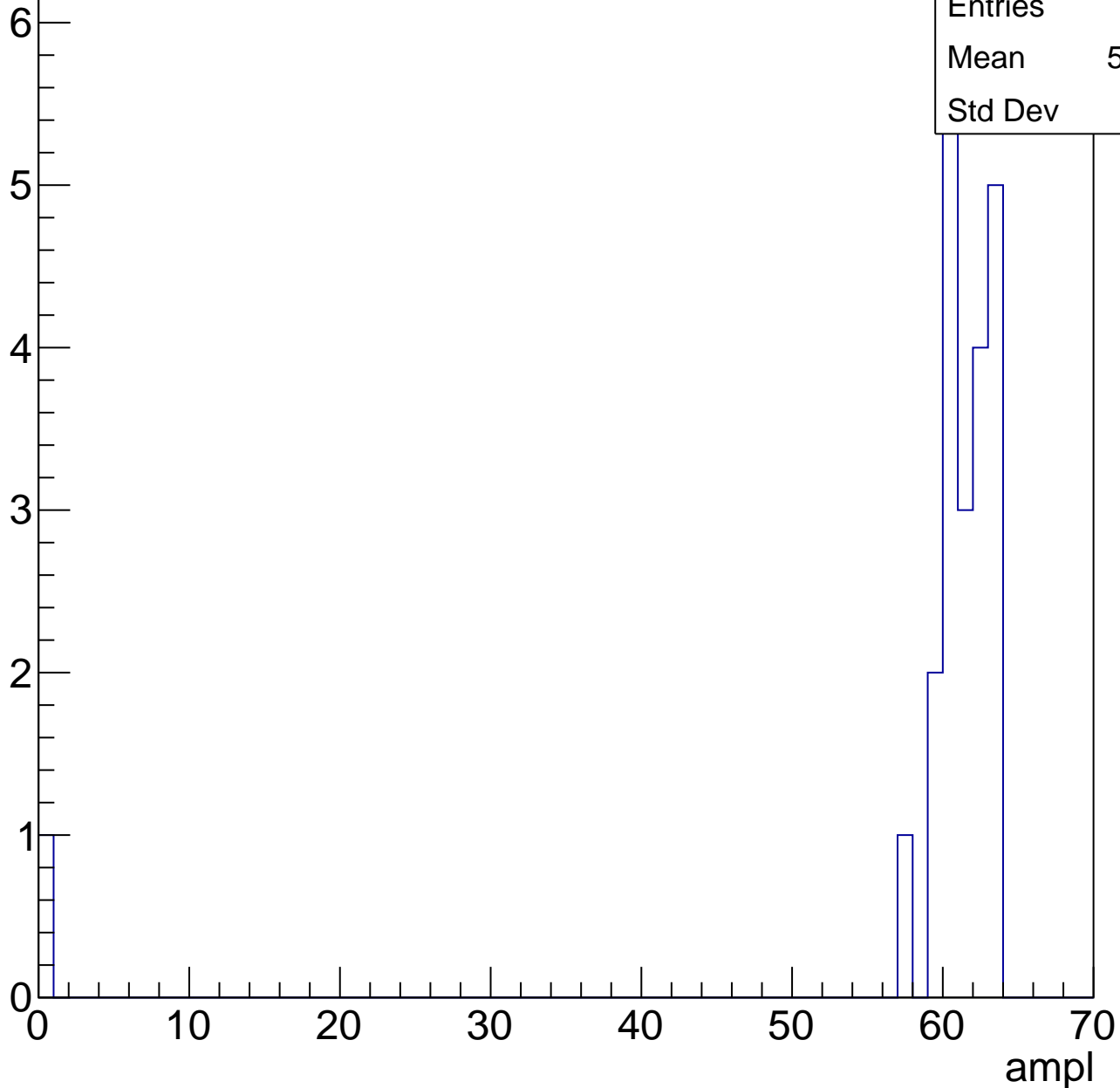
Entries	36
Mean	59.08
Std Dev	2.773



# B1L102S, U12-ch46, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U12-ch46, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U12-ch47, adc0

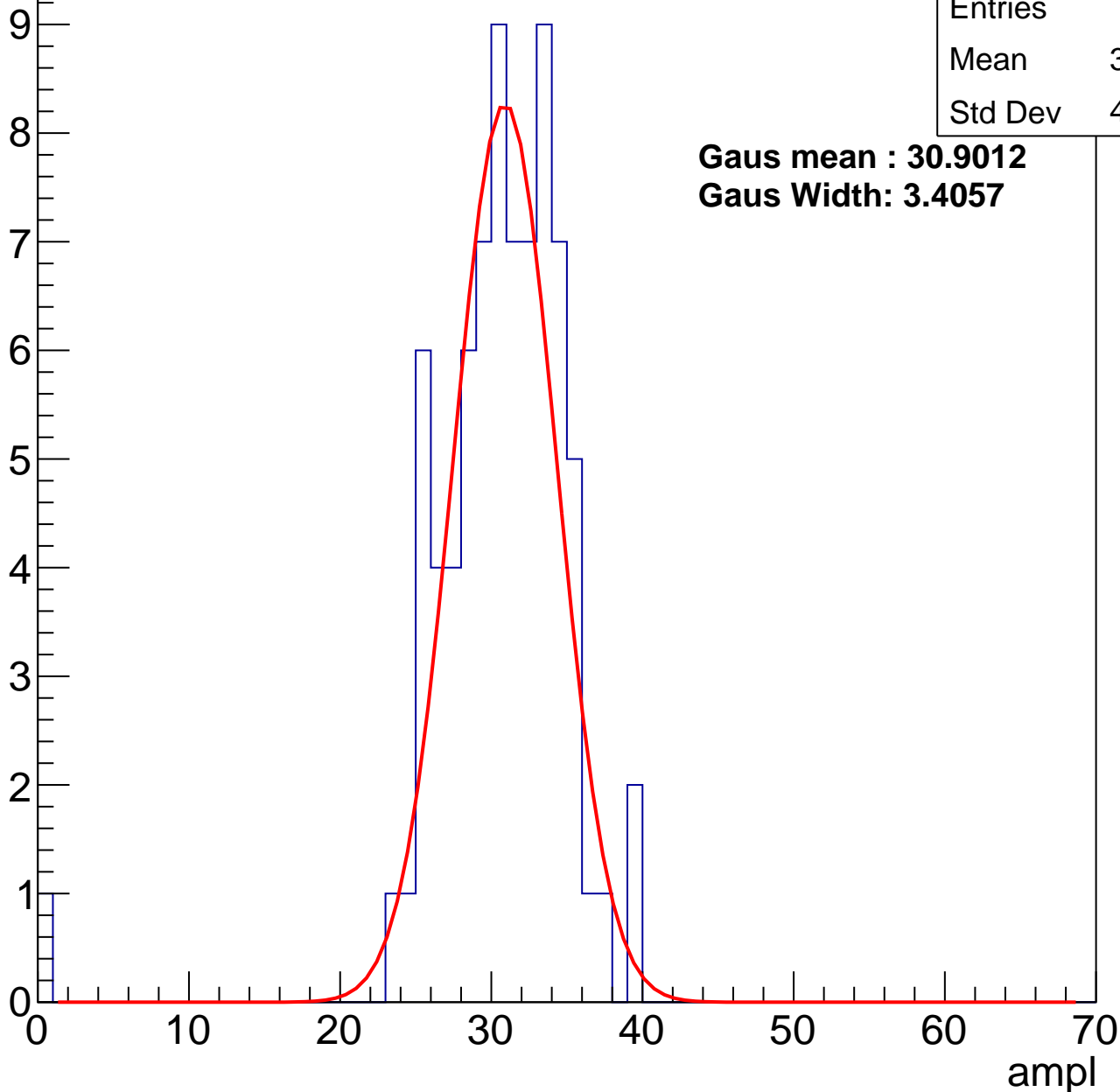
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	78
Mean	30.15
Std Dev	4.889

**Gaus mean : 30.9012**

**Gaus Width: 3.4057**



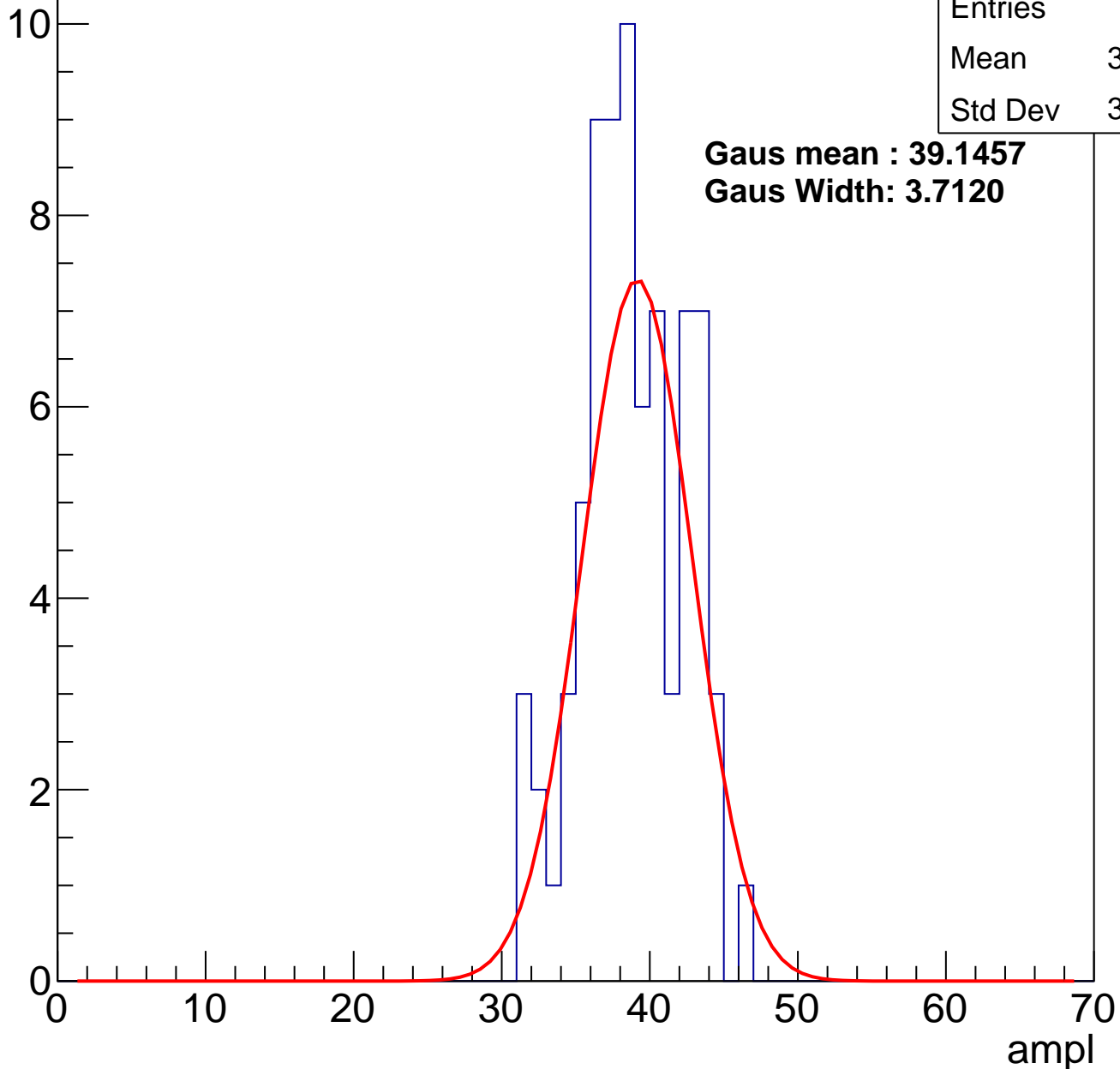
# B1L102S, U12-ch47, adc1

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	76
Mean	38.34
Std Dev	3.428

**Gaus mean : 39.1457**  
**Gaus Width: 3.7120**

Entry



# B1L102S, U12-ch47, adc2

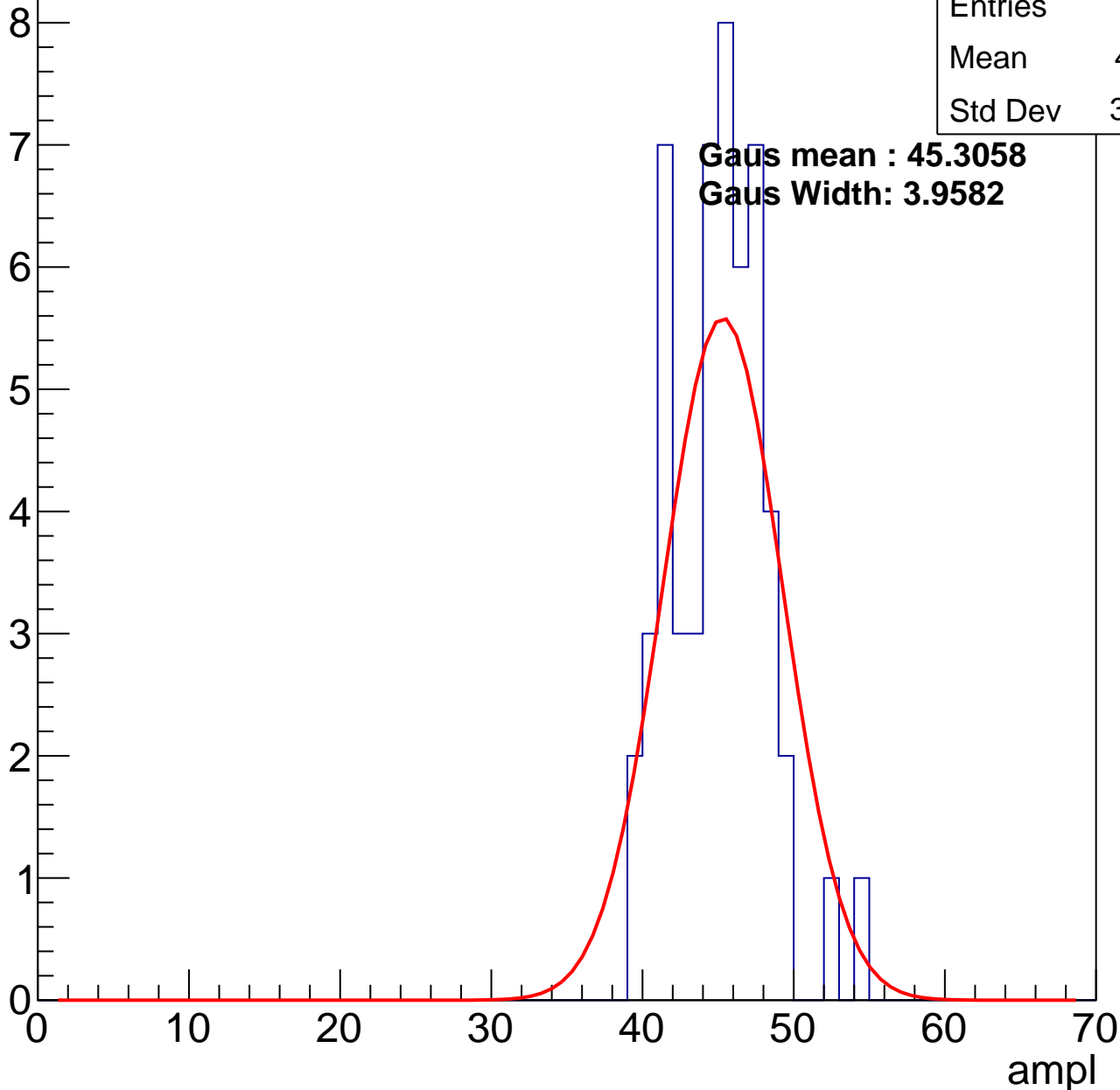
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	54
Mean	44.61
Std Dev	3.129

**Gaus mean : 45.3058**

**Gaus Width: 3.9582**

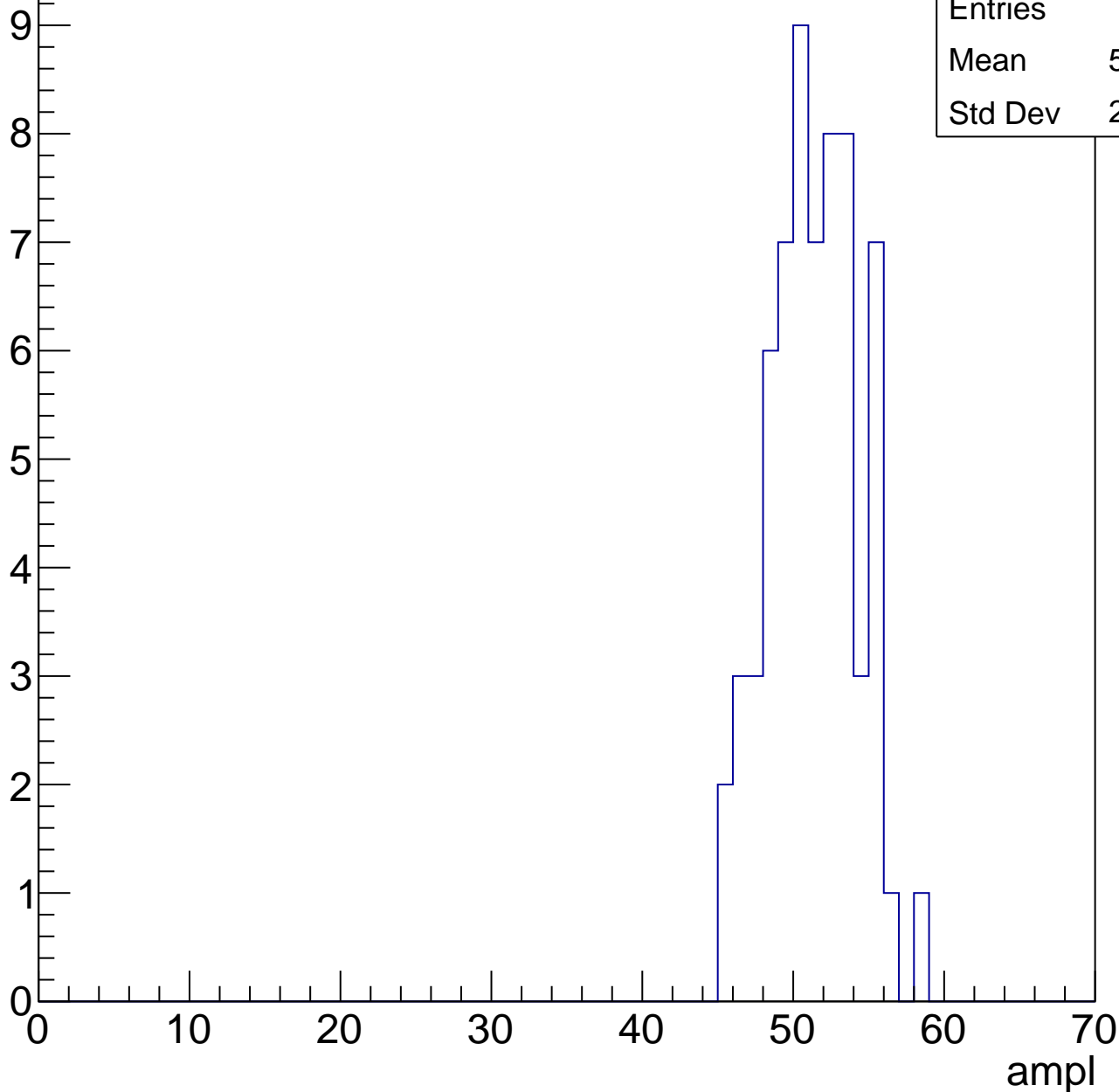


# B1L102S, U12-ch47, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	65
Mean	50.89
Std Dev	2.878

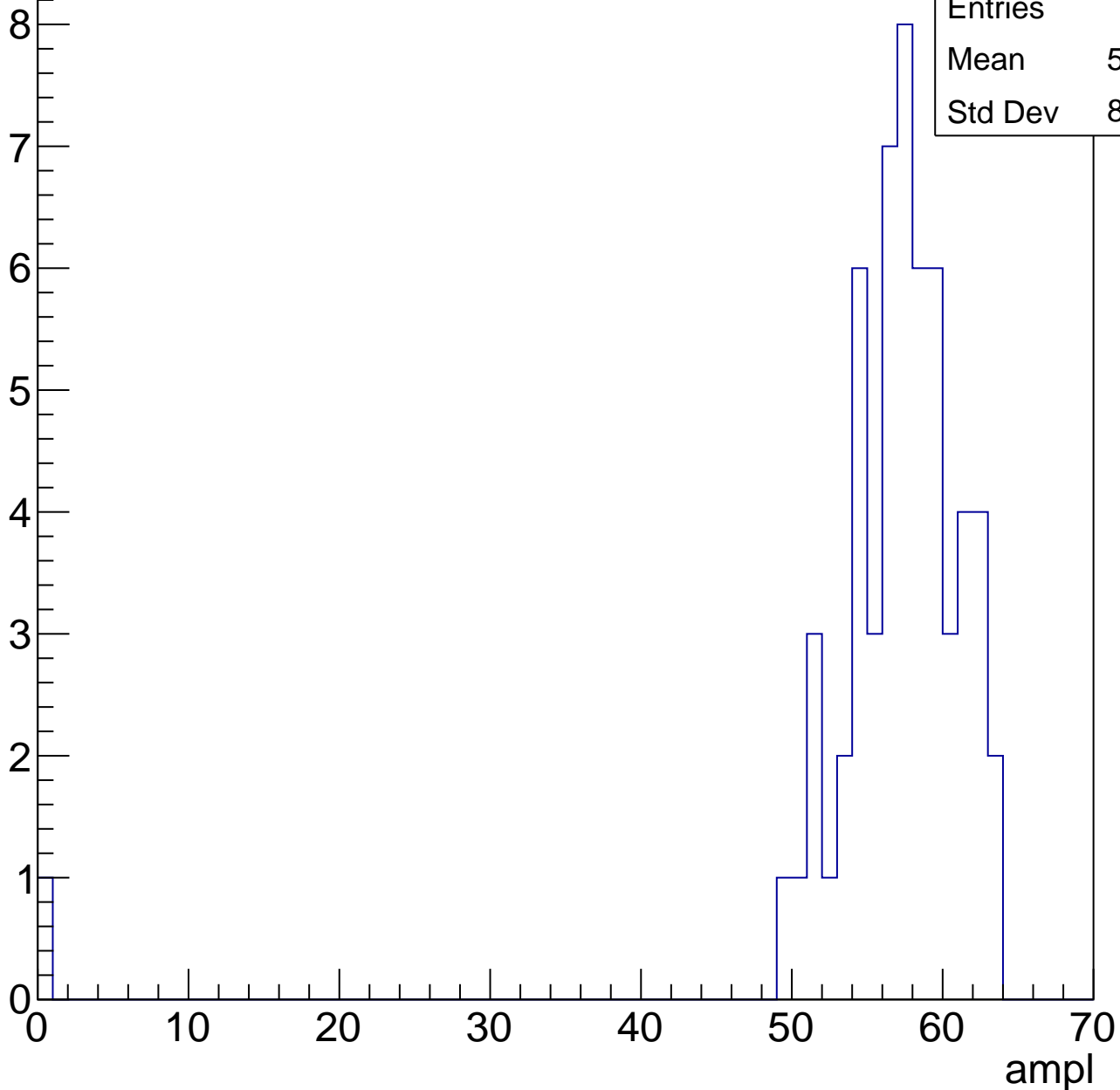


# B1L102S, U12-ch47, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	58
Mean	55.98
Std Dev	8.129



# B1L102S, U12-ch47, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

7

6

5

4

3

2

1

0

Entries

35

Mean

60.31

Std Dev

2.039

ampl

0

10

20

30

40

50

60

70

# B1L102S, U12-ch47, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	3
Mean	62.33
Std Dev	0.9428

0 10 20 30 40 50 60 70

ampl





# B1L102S, U12-ch47, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U12-ch48, adc0

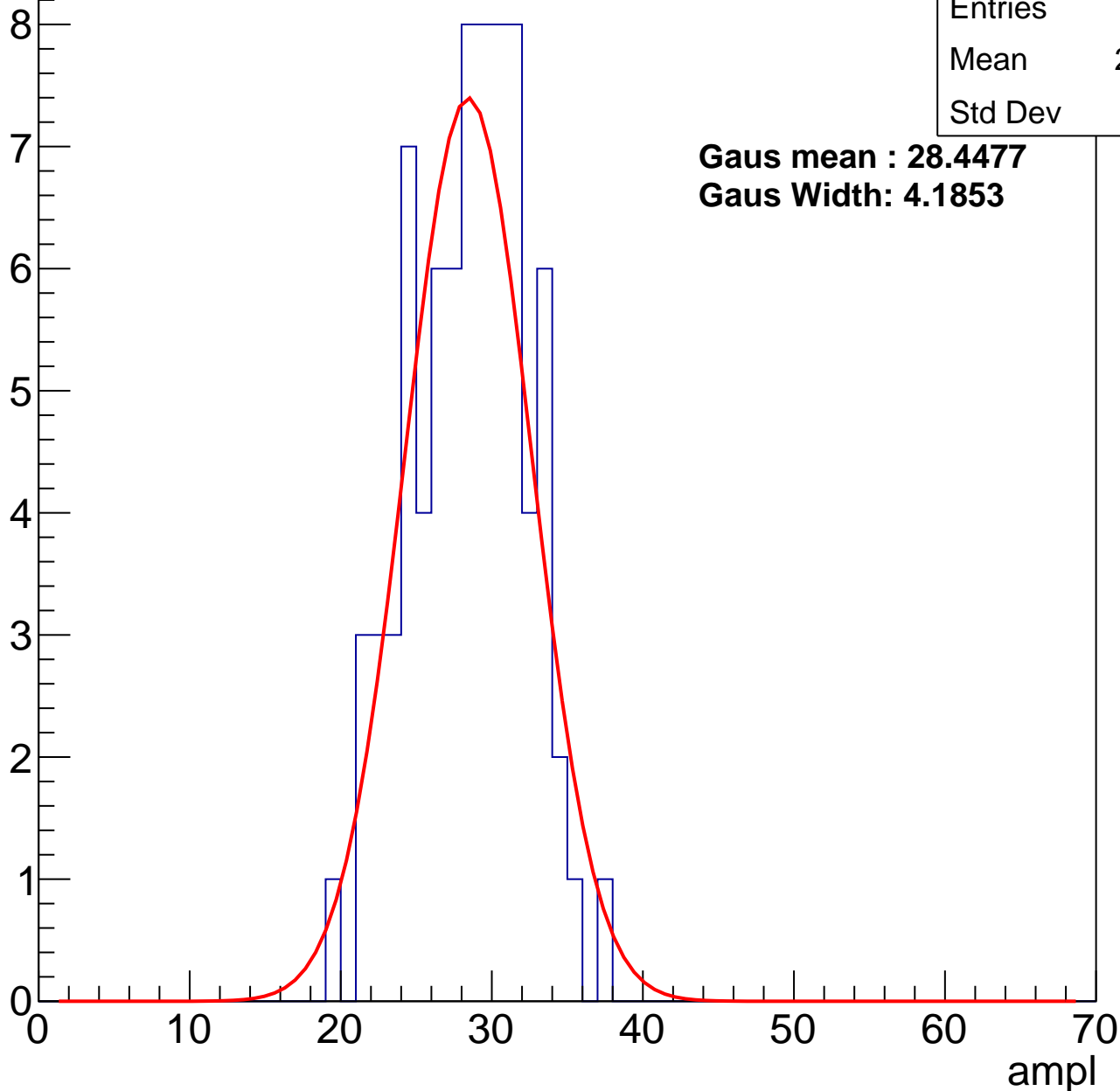
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	79
Mean	28.01
Std Dev	3.76

**Gaus mean : 28.4477**

**Gaus Width: 4.1853**



# B1L102S, U12-ch48, adc1

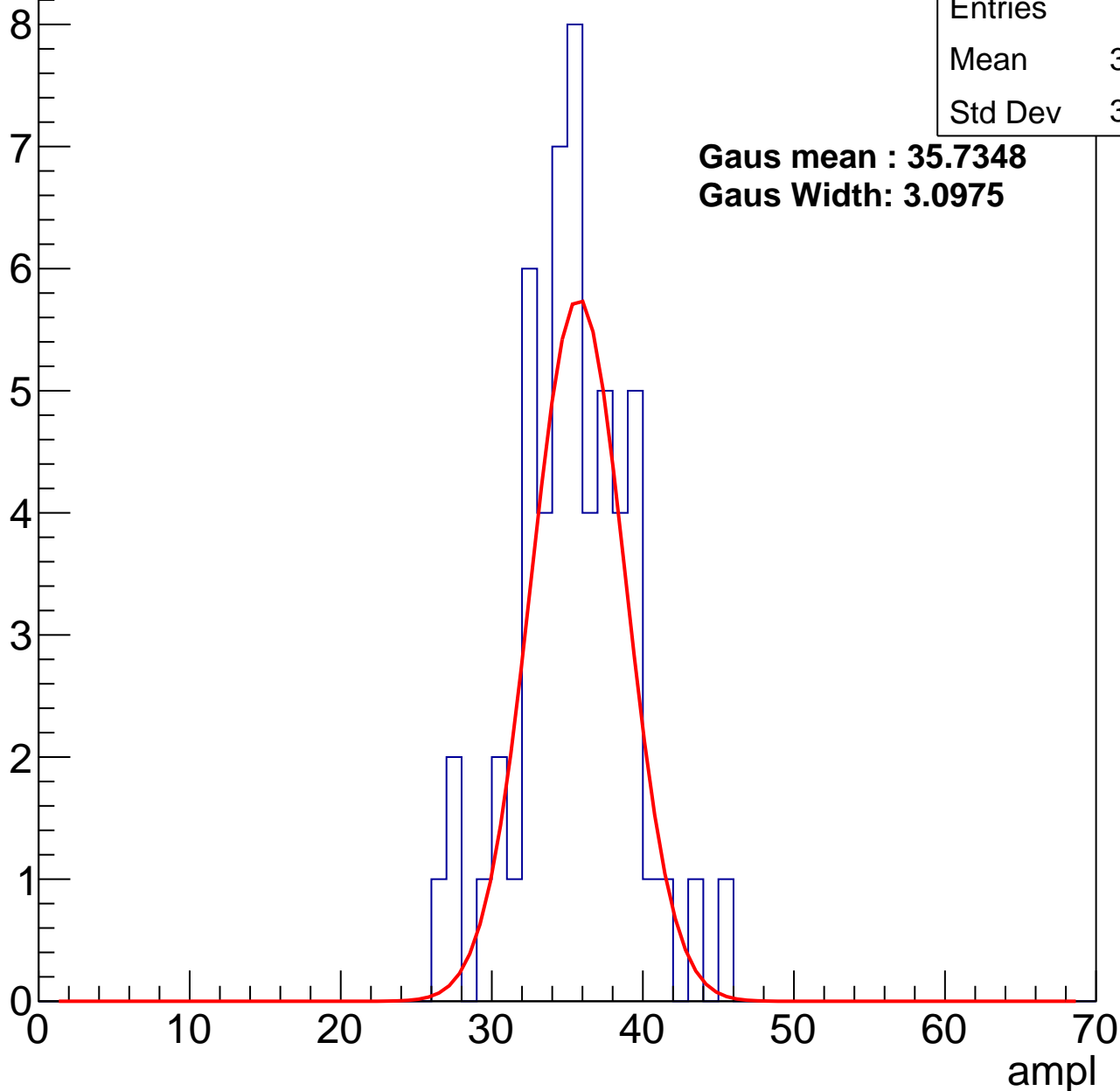
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	54
Mean	34.94
Std Dev	3.734

**Gaus mean : 35.7348**

**Gaus Width: 3.0975**



# B1L102S, U12-ch48, adc2

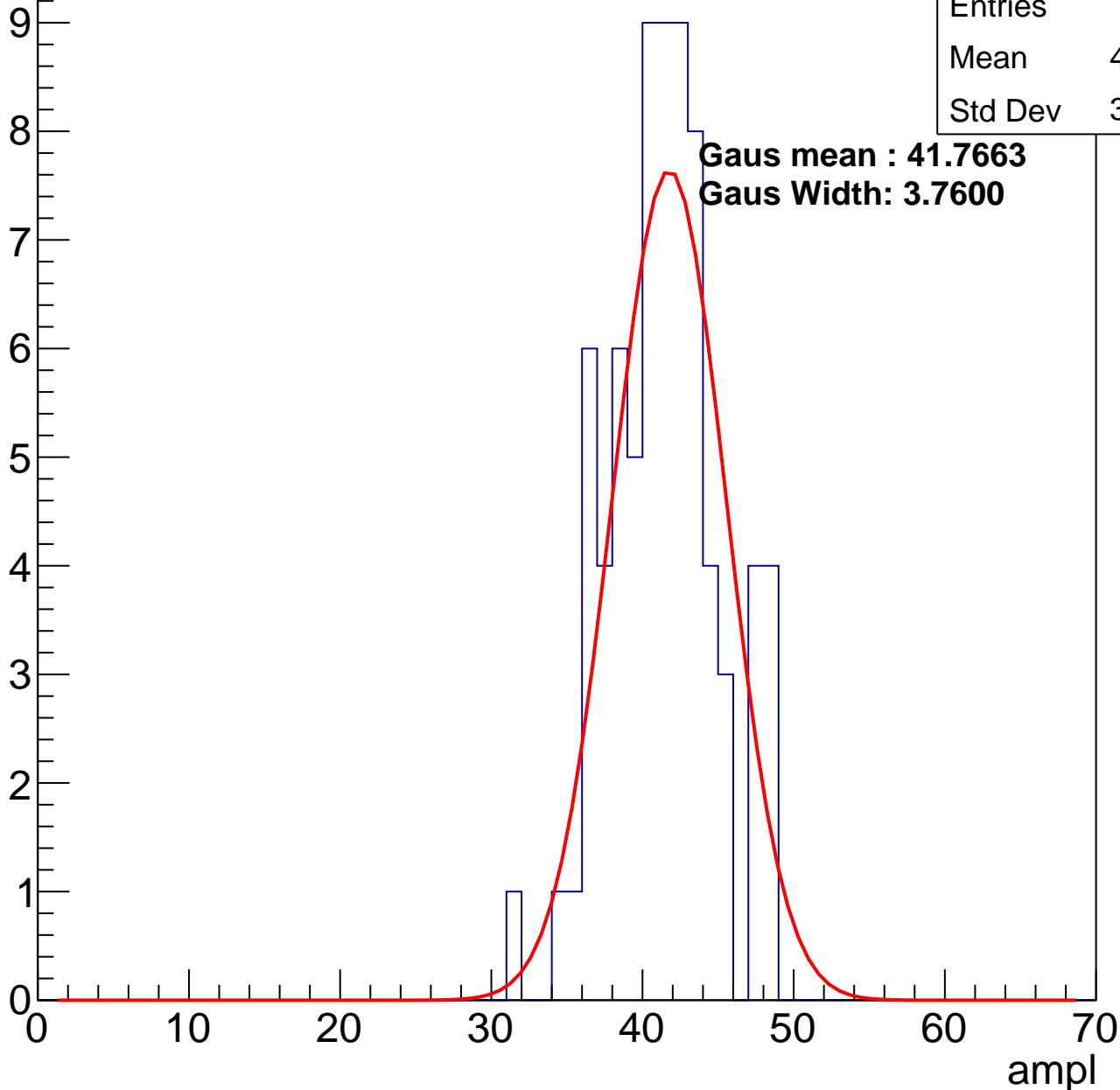
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	74
Mean	40.93
Std Dev	3.577

**Gaus mean : 41.7663**

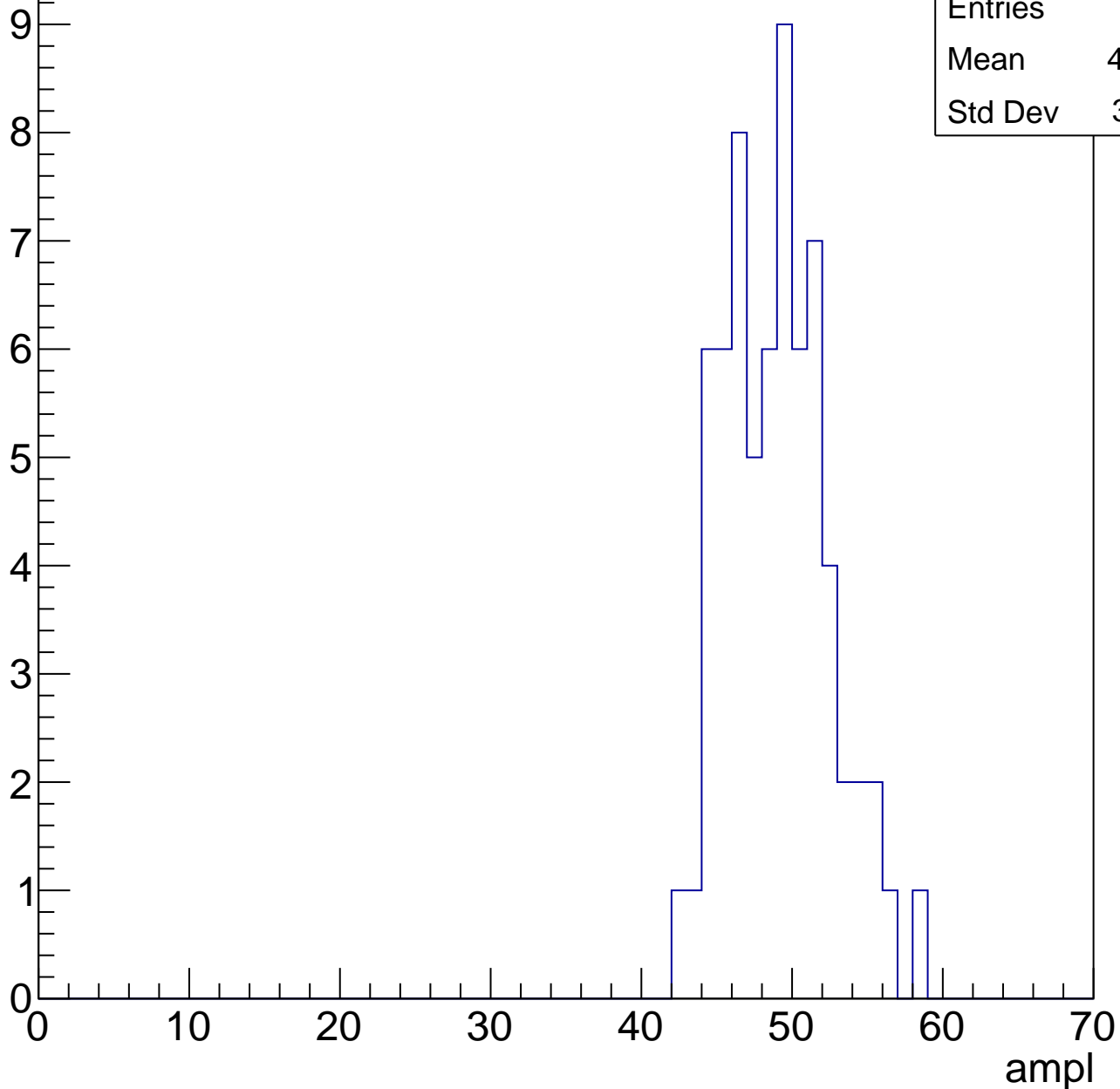
**Gaus Width: 3.7600**



# B1L102S, U12-ch48, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

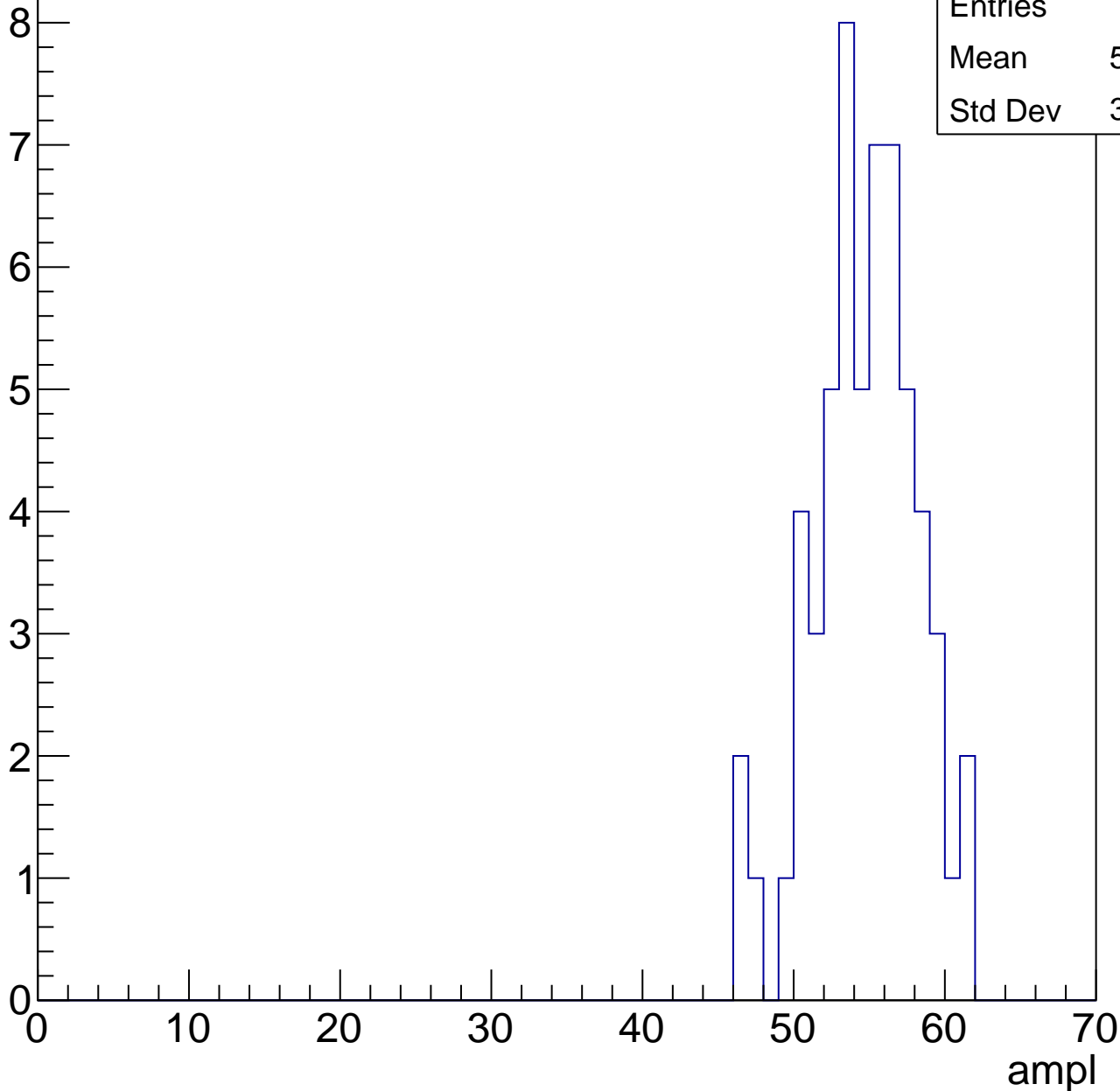


# B1L102S, U12-ch48, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	58
Mean	54.28
Std Dev	3.398

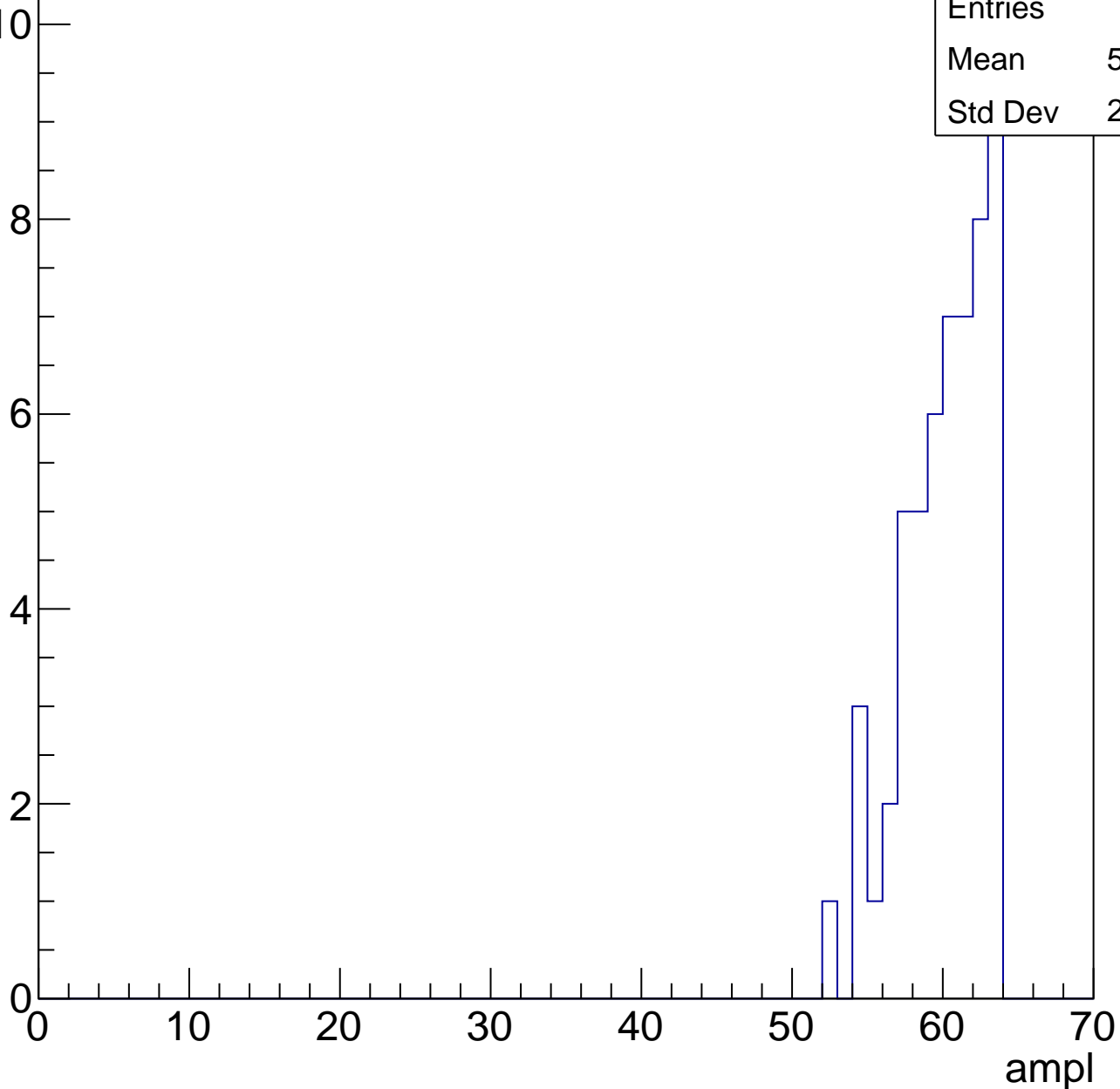


# B1L102S, U12-ch48, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

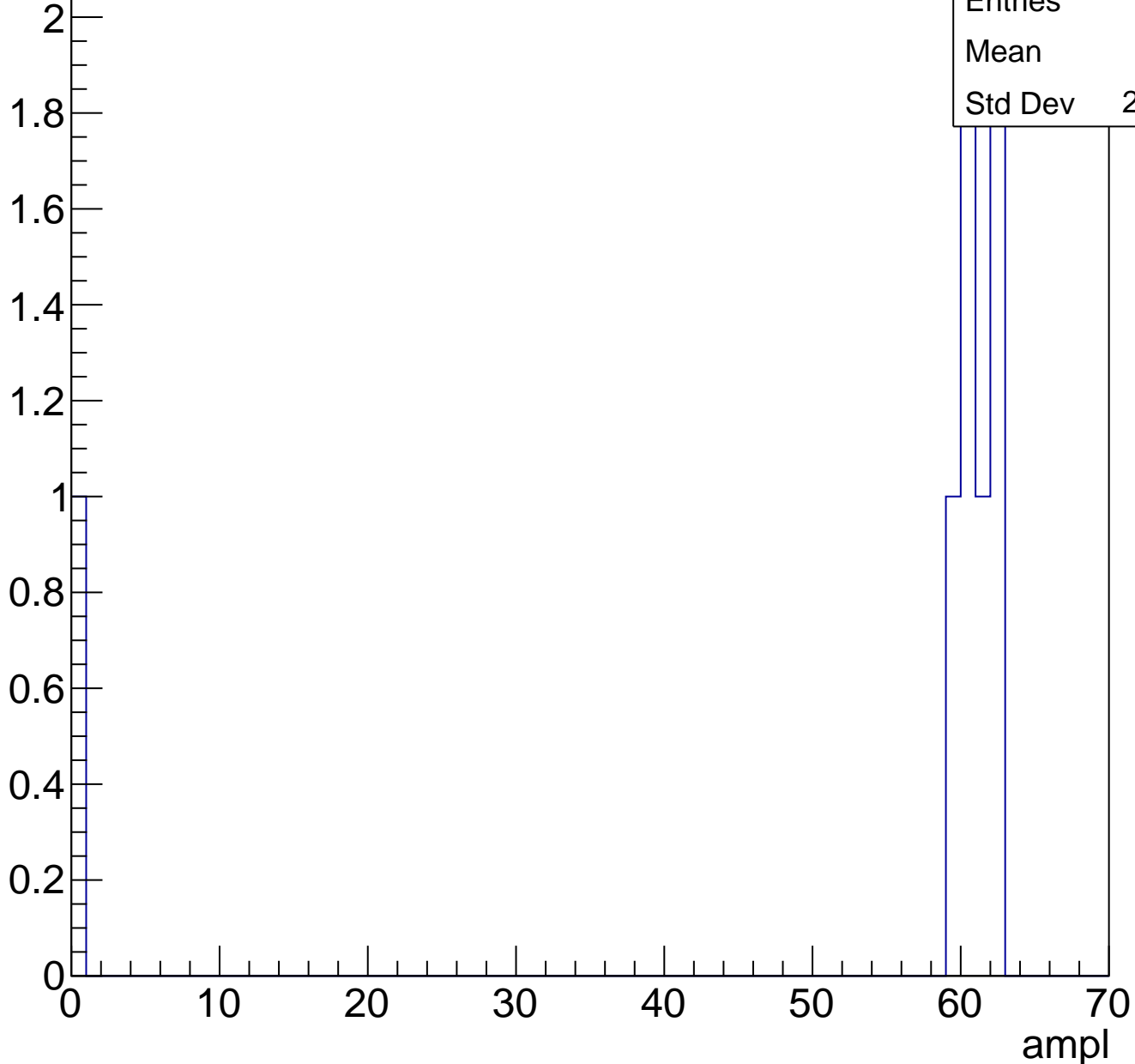
Entries	55
Mean	59.69
Std Dev	2.776



# B1L102S, U12-ch48, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	7
Mean	52
Std Dev	21.25



# B1L102S, U12-ch48, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L102S, U12-ch49, adc0

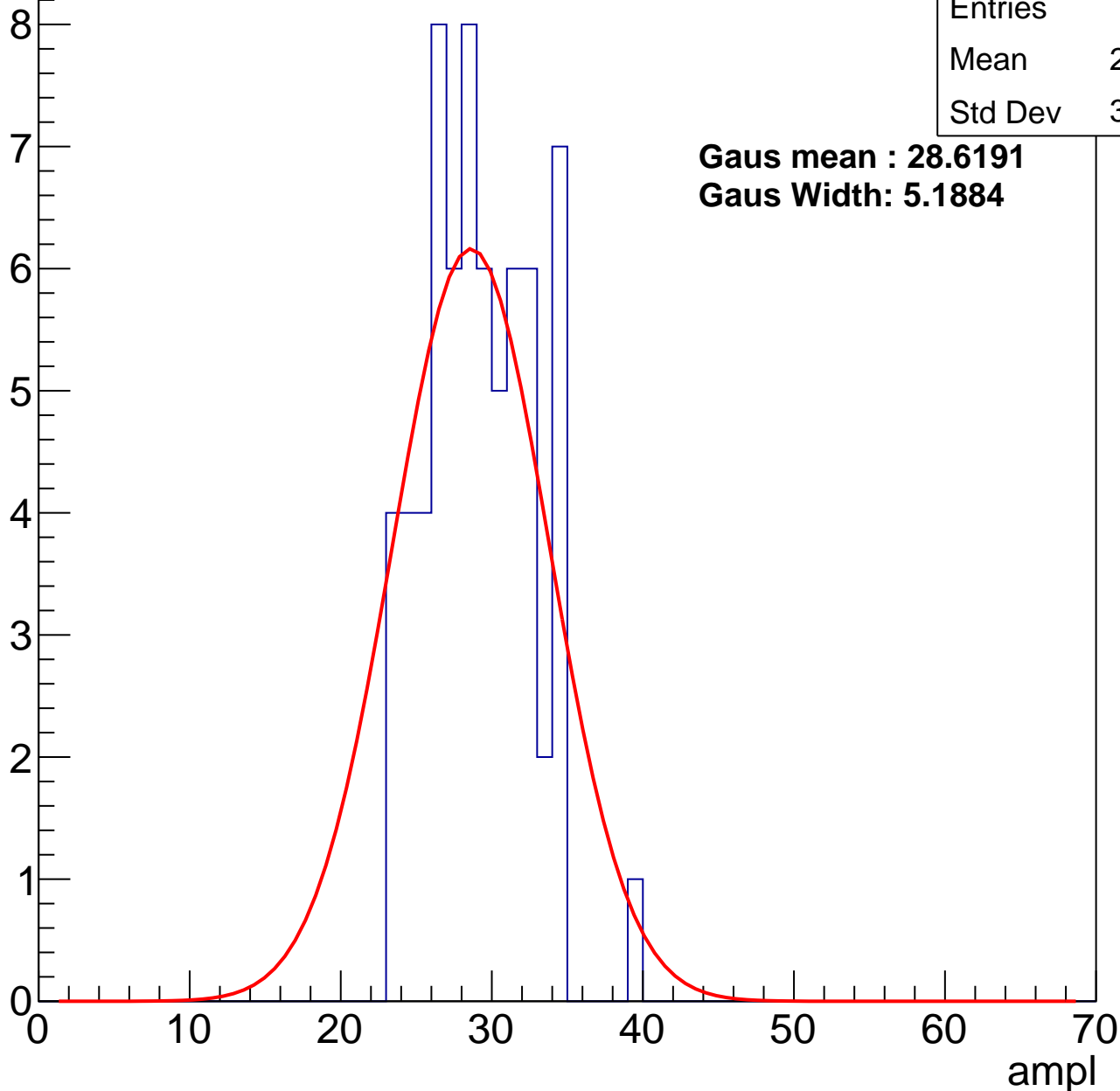
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	67
Mean	28.76
Std Dev	3.452

**Gaus mean : 28.6191**

**Gaus Width: 5.1884**



# B1L102S, U12-ch49, adc1

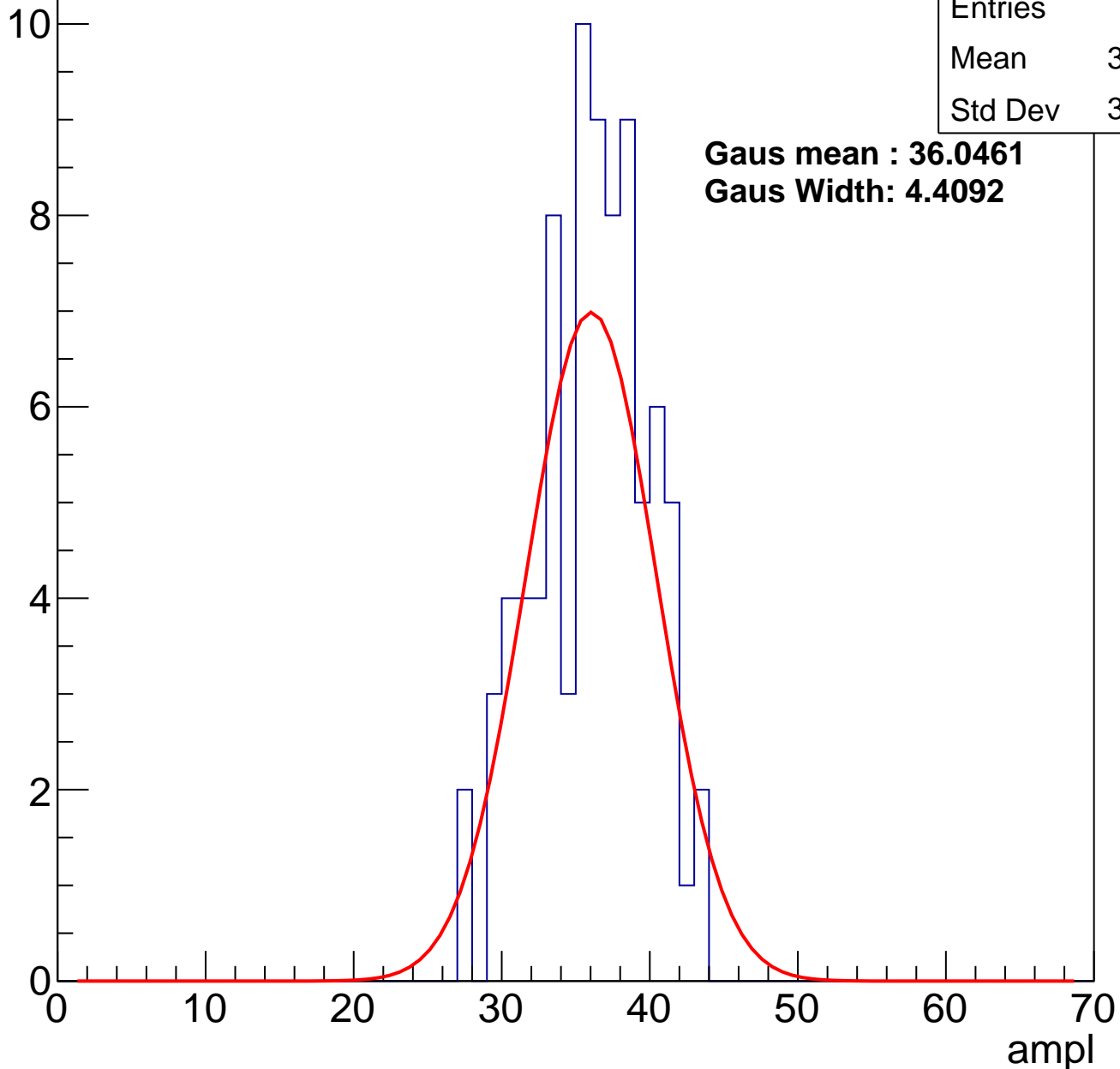
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	83
Mean	35.65
Std Dev	3.714

**Gaus mean : 36.0461**

**Gaus Width: 4.4092**

Entry



# B1L102S, U12-ch49, adc2

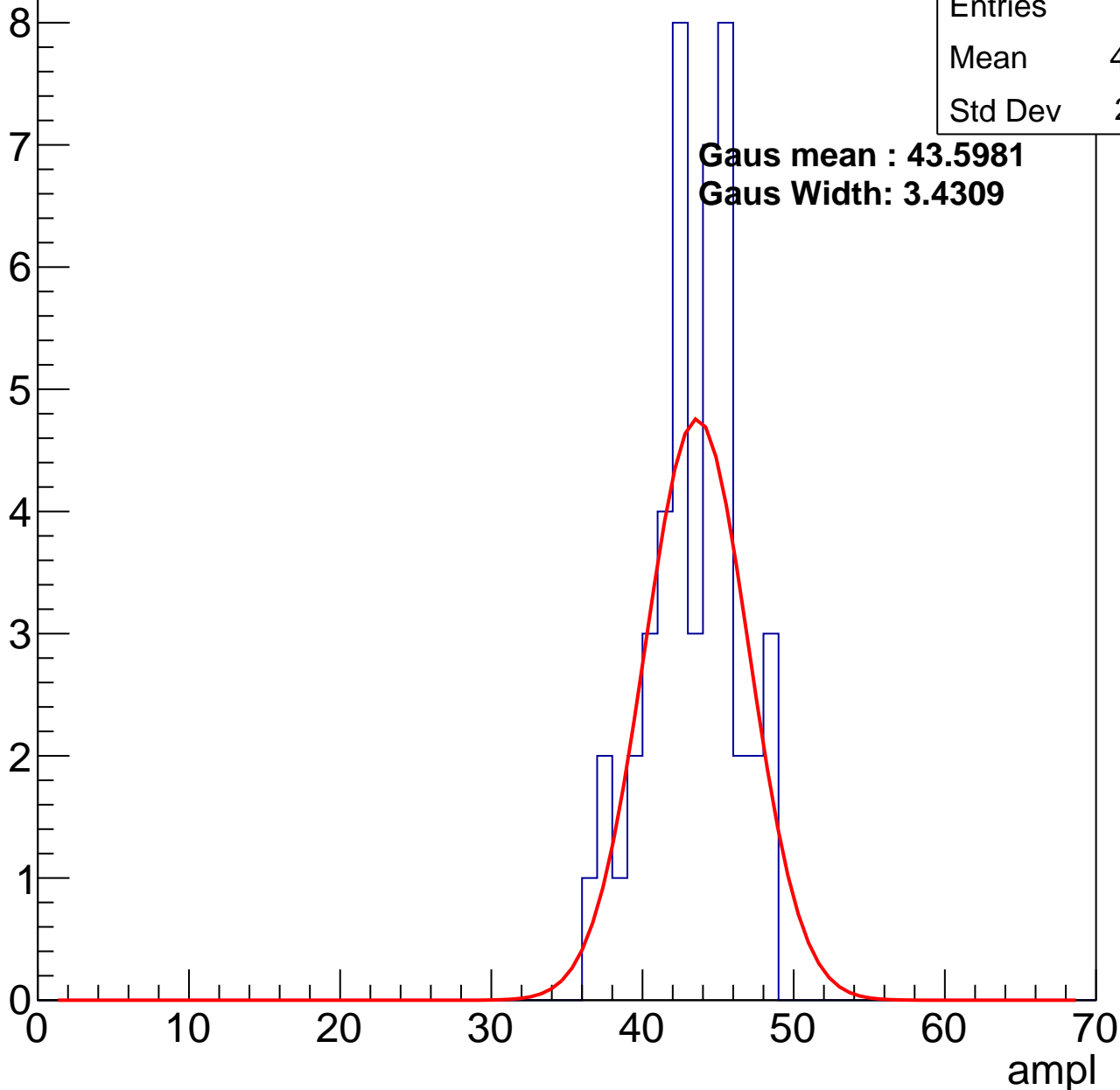
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	46
Mean	42.89
Std Dev	2.921

**Gaus mean : 43.5981**

**Gaus Width: 3.4309**



# B1L102S, U12-ch49, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

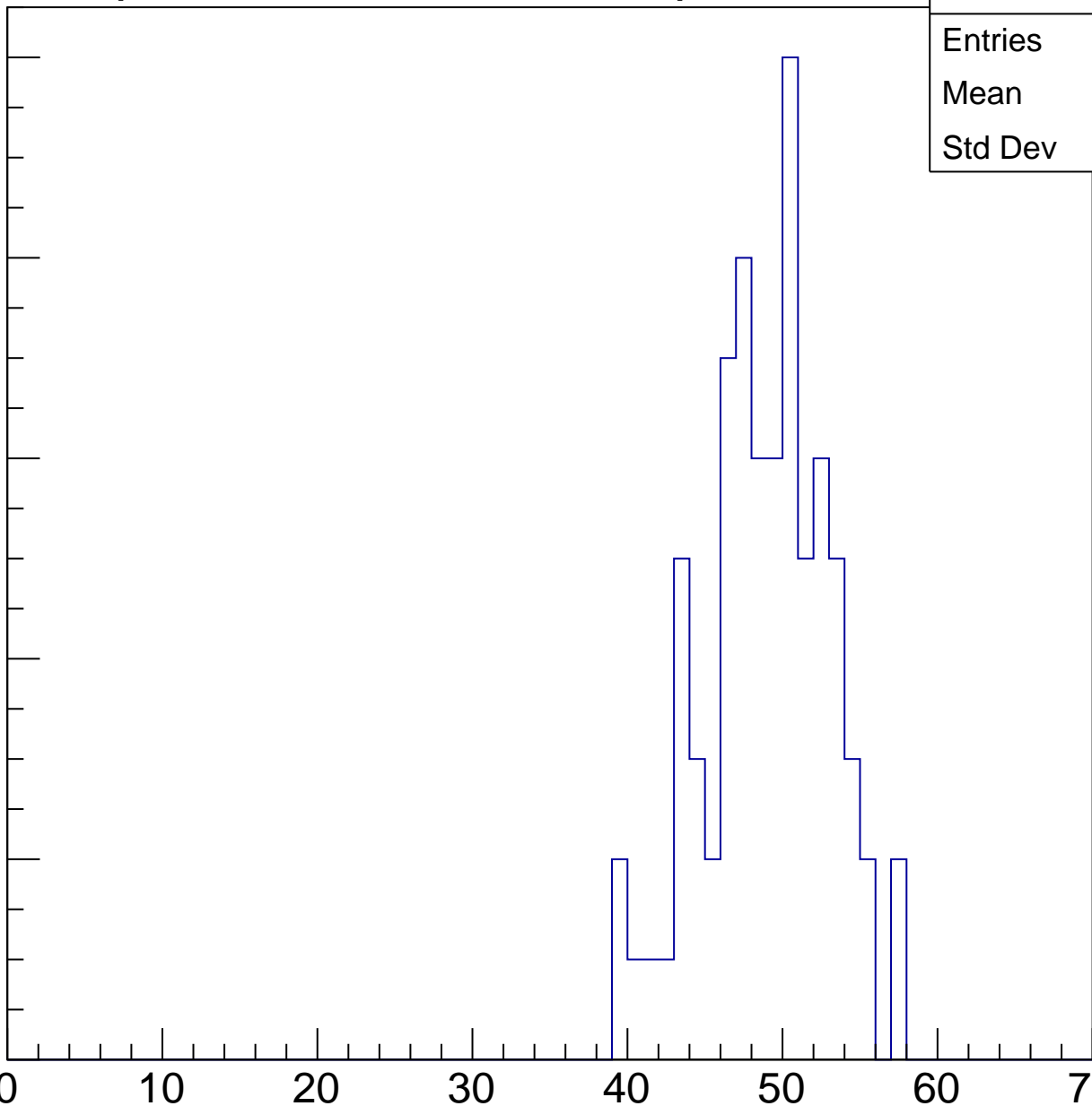
Entries	75
Mean	48.48
Std Dev	4.001

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

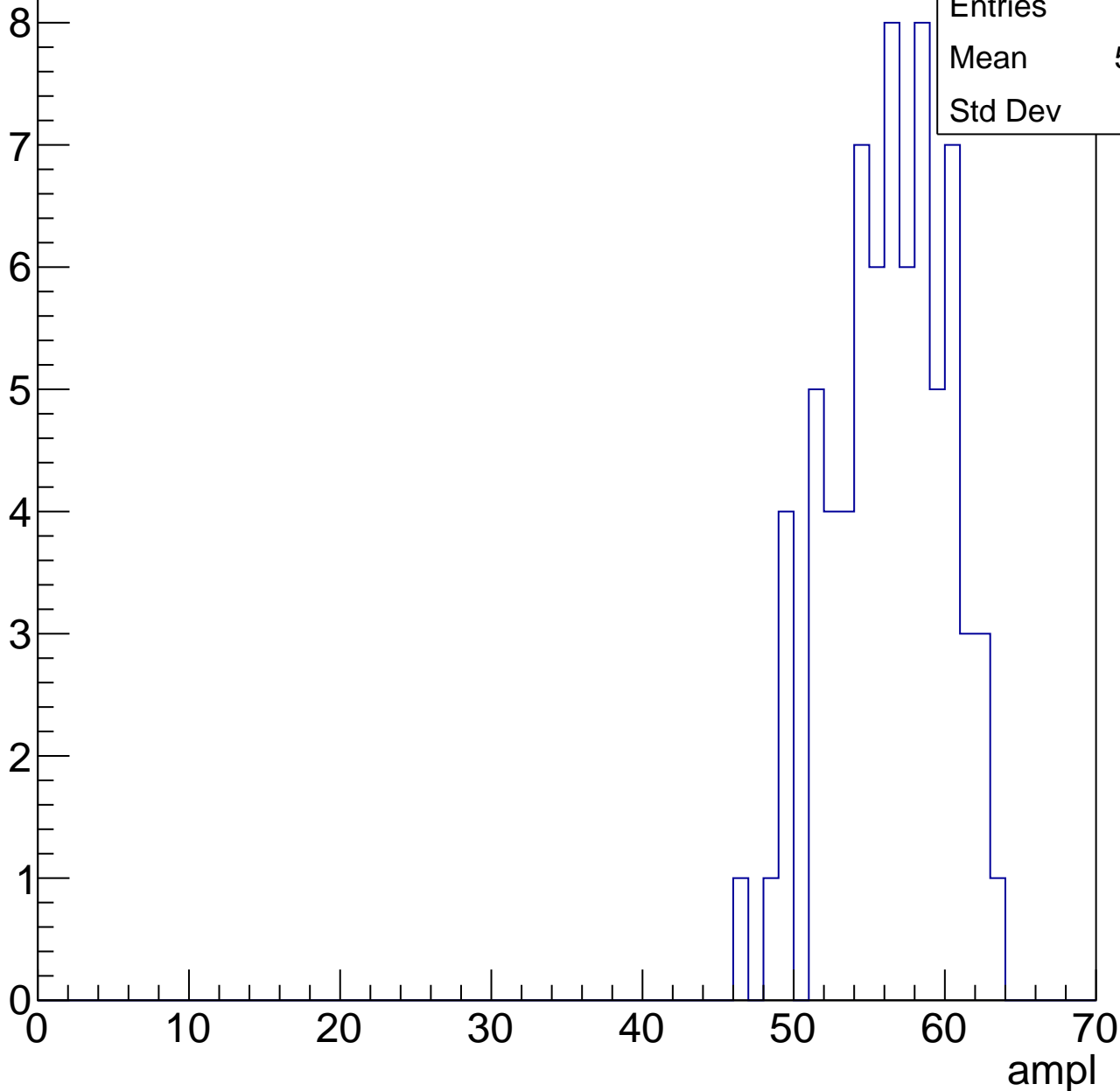


# B1L102S, U12-ch49, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	73
Mean	55.81
Std Dev	3.78

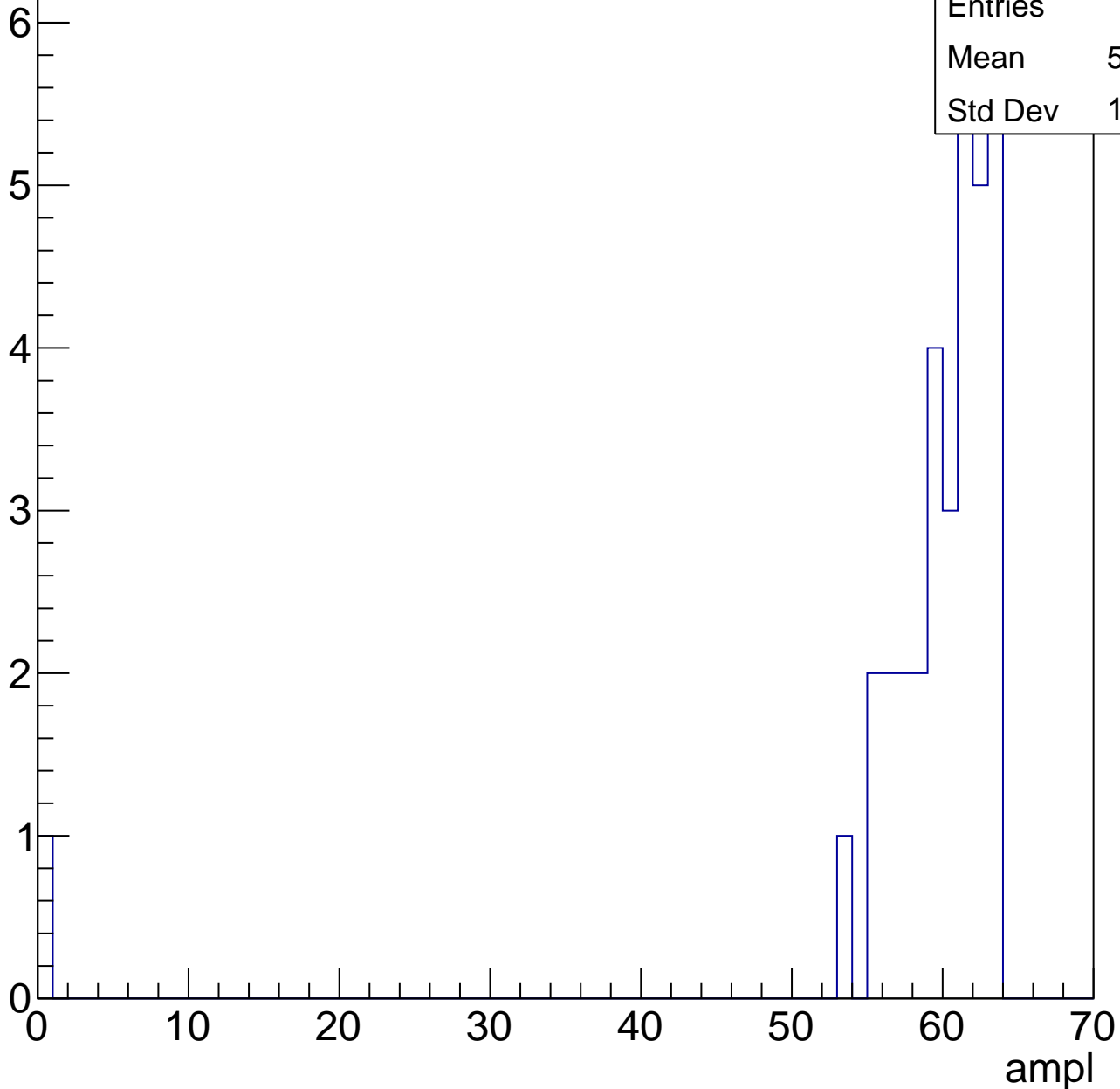


# B1L102S, U12-ch49, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	34
Mean	58.09
Std Dev	10.46



# B1L102S, U12-ch49, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U12-ch49, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U12-ch50, adc0

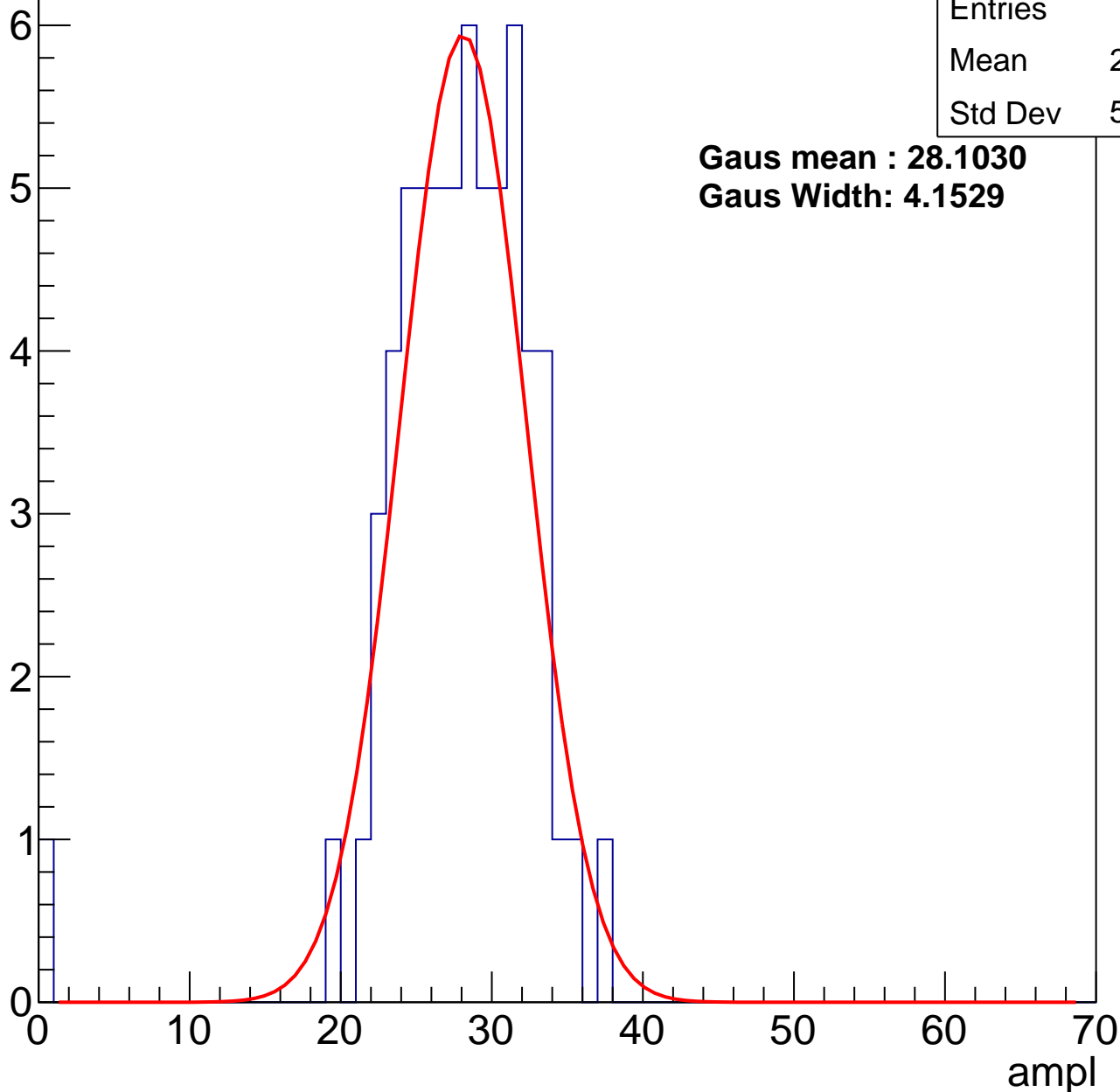
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	63
Mean	27.35
Std Dev	5.124

**Gaus mean : 28.1030**

**Gaus Width: 4.1529**



# B1L102S, U12-ch50, adc1

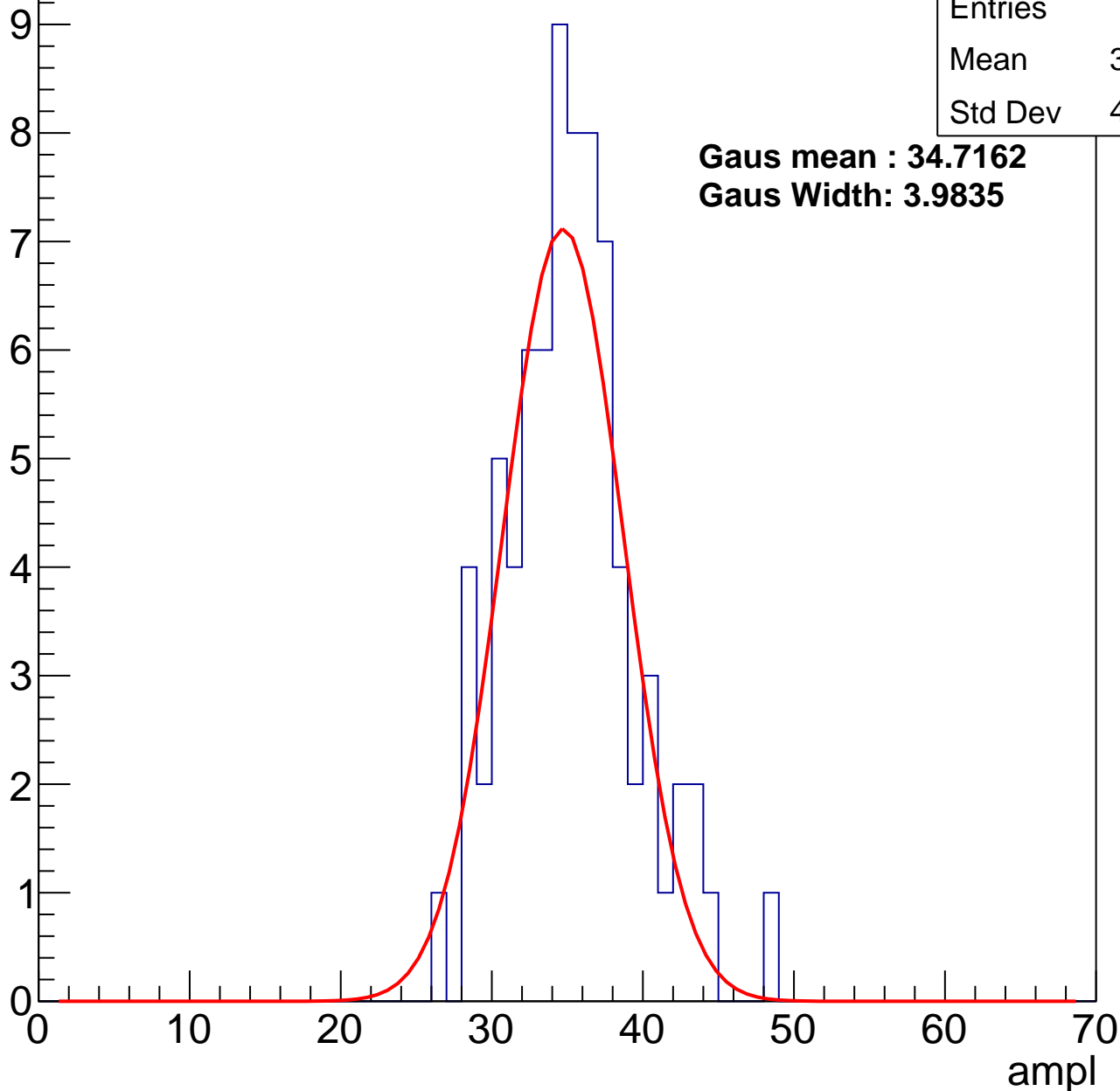
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	76
Mean	34.82
Std Dev	4.157

**Gaus mean : 34.7162**

**Gaus Width: 3.9835**



# B1L102S, U12-ch50, adc2

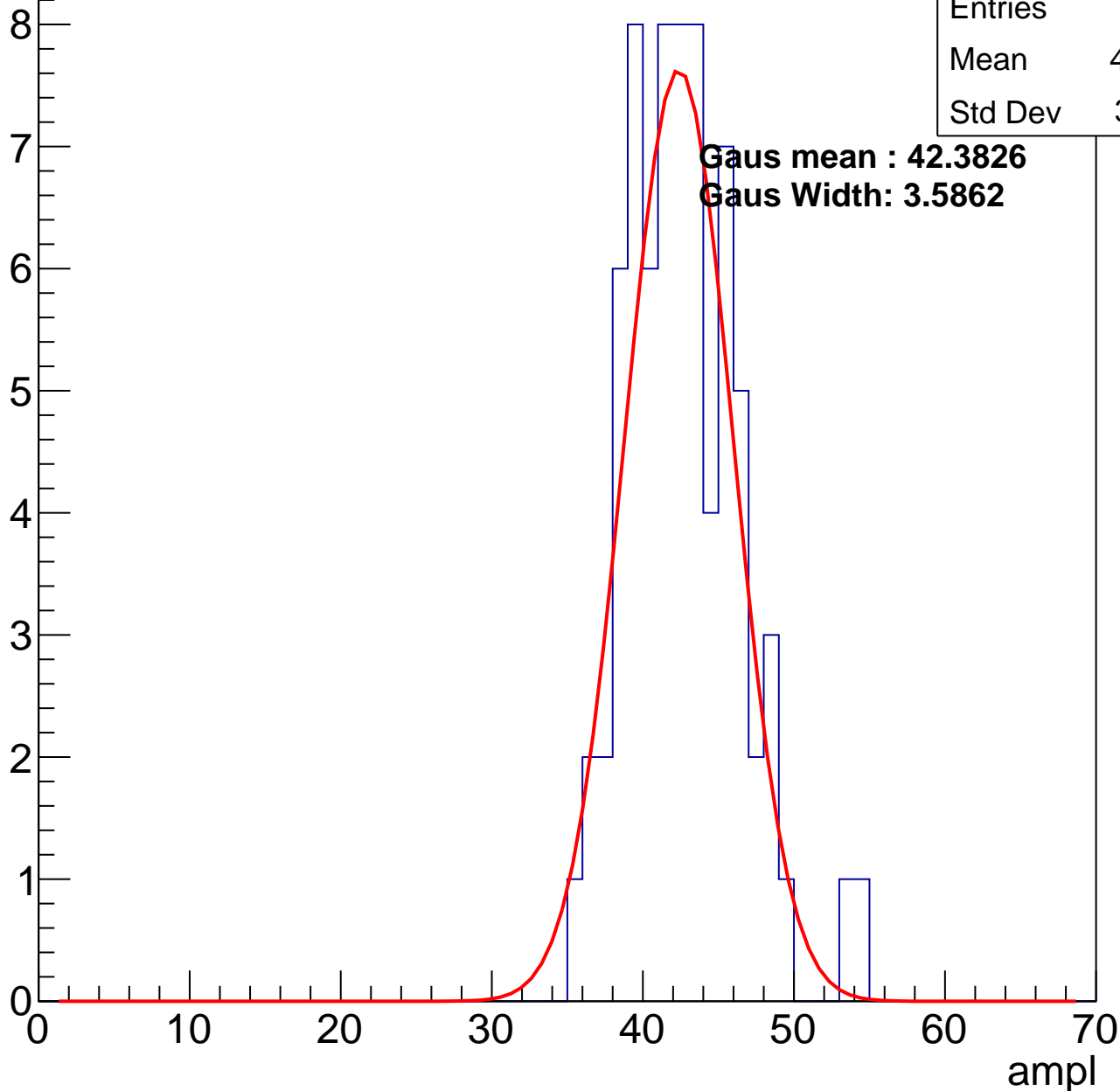
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	73
Mean	42.25
Std Dev	3.711

**Gaus mean : 42.3826**

**Gaus Width: 3.5862**

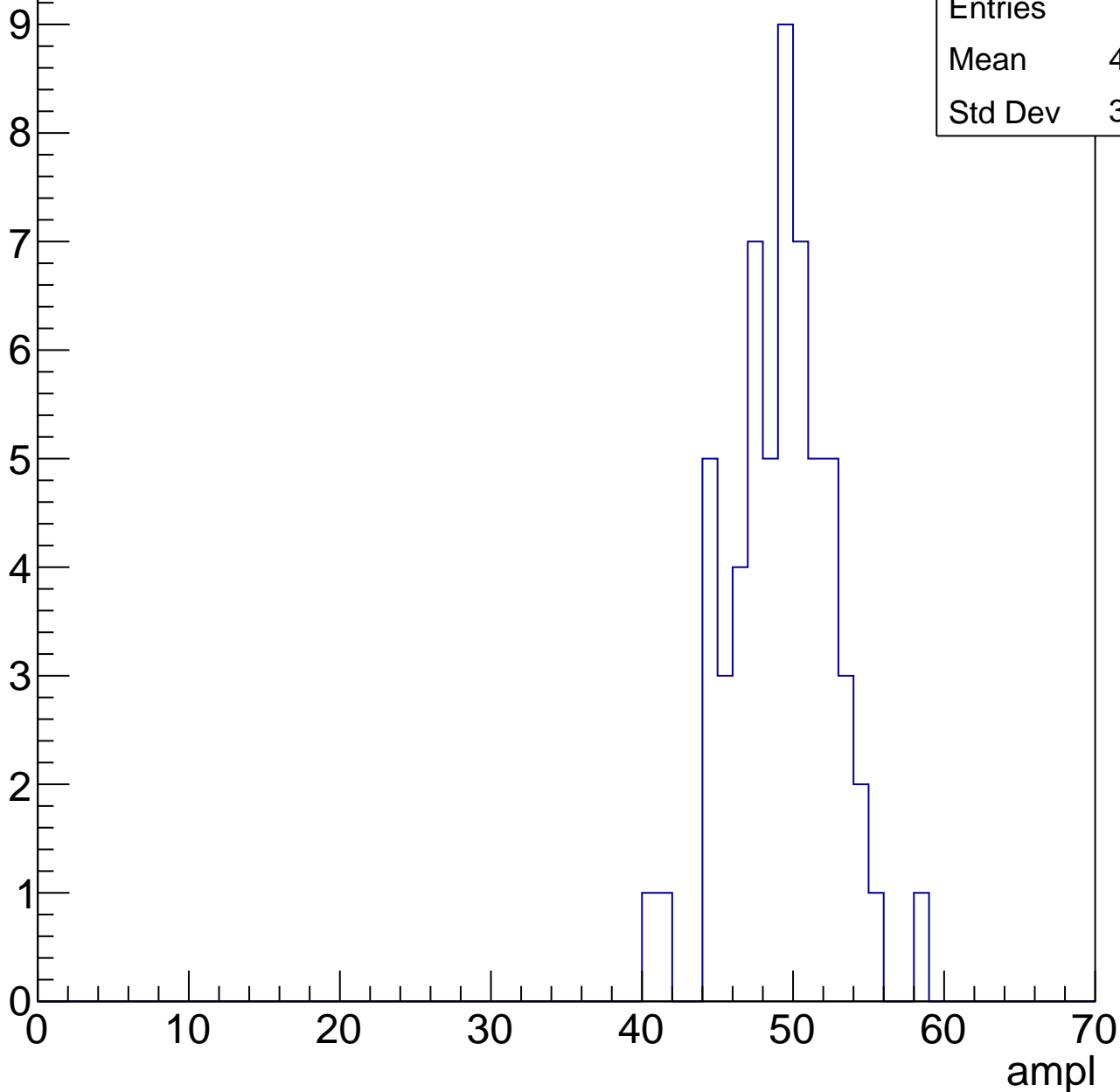


# B1L102S, U12-ch50, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	59
Mean	48.73
Std Dev	3.369

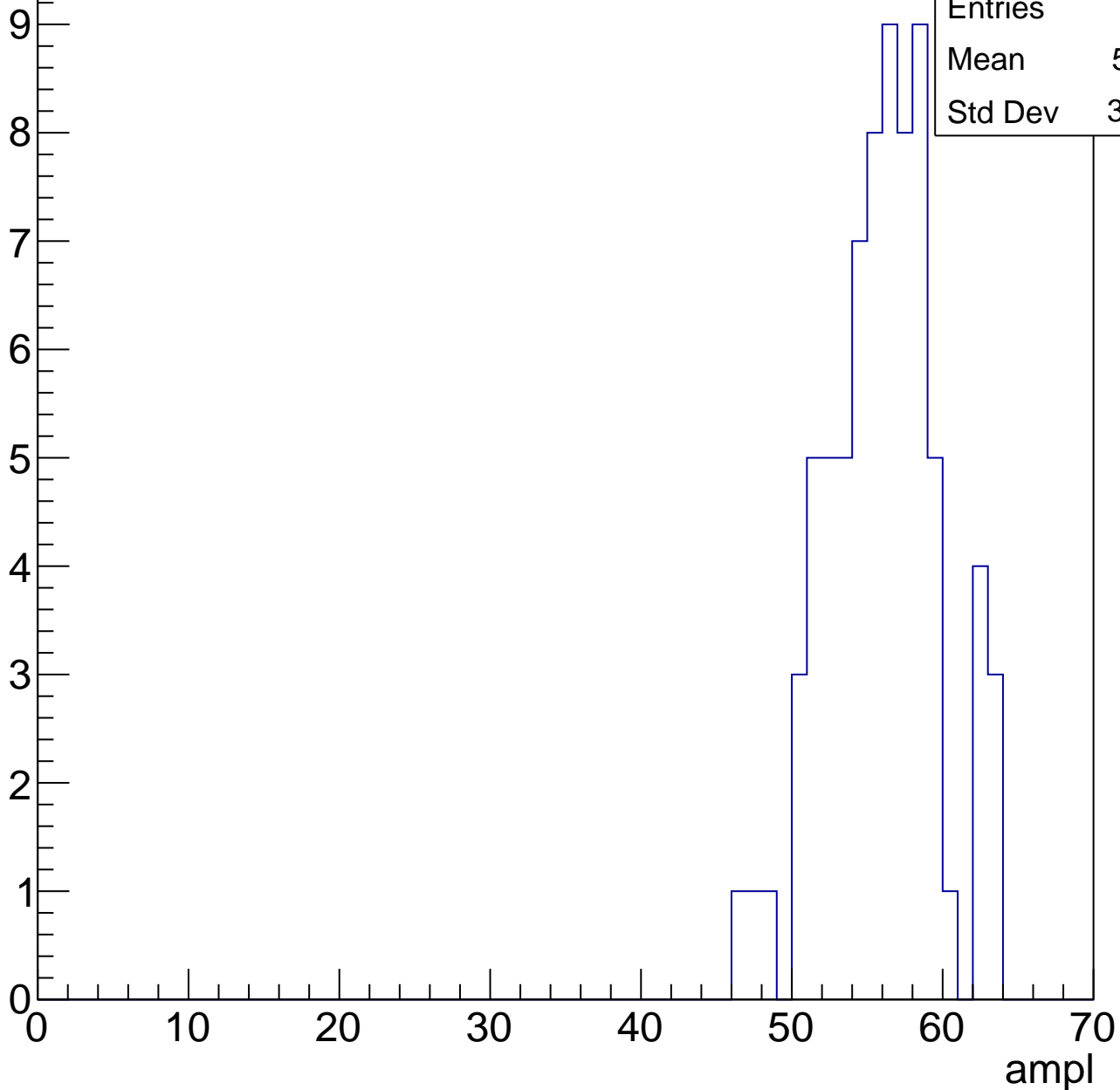


# B1L102S, U12-ch50, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	75
Mean	55.51
Std Dev	3.682



# B1L102S, U12-ch50, adc5

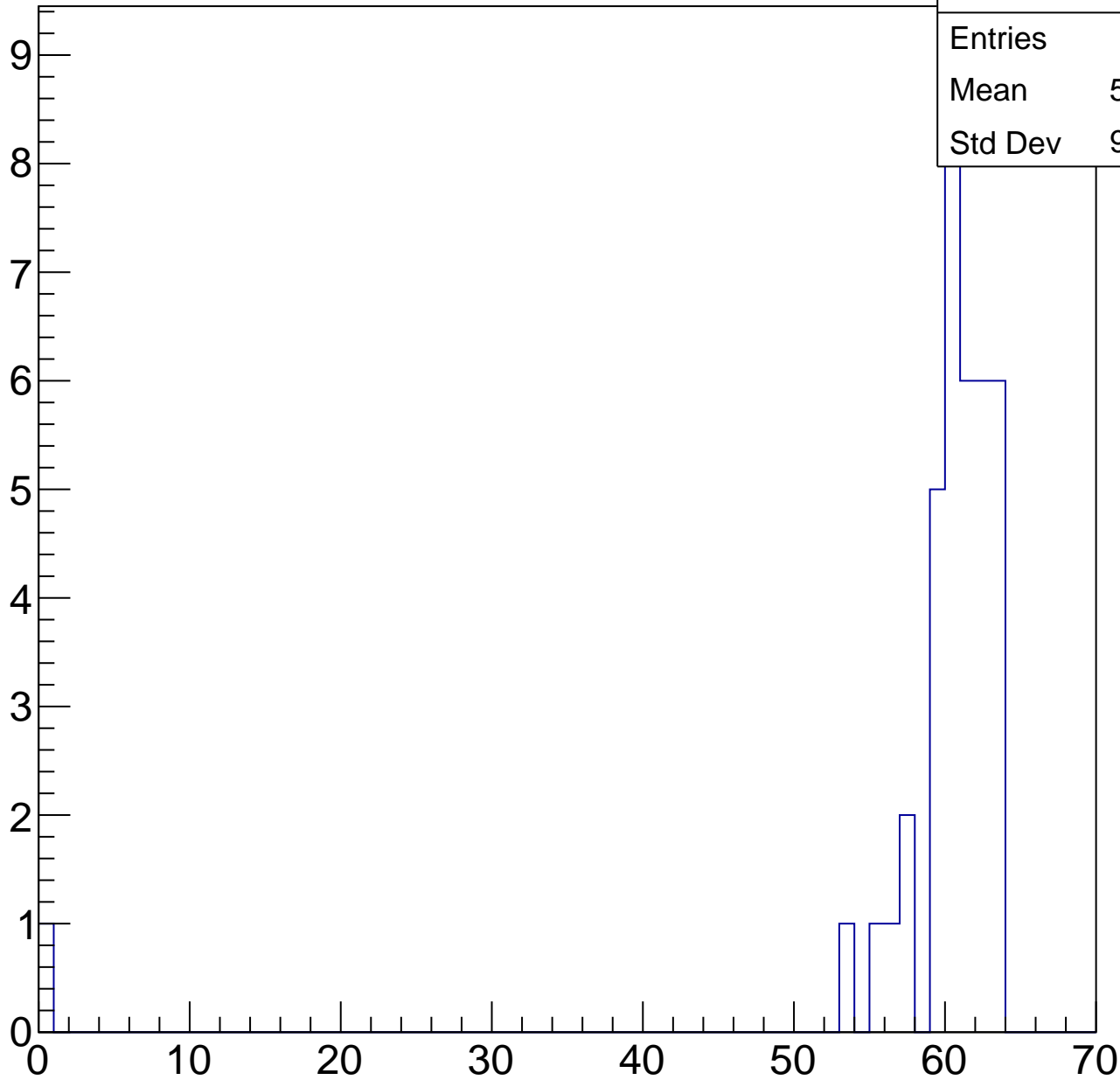
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	38
Mean	58.66
Std Dev	9.906

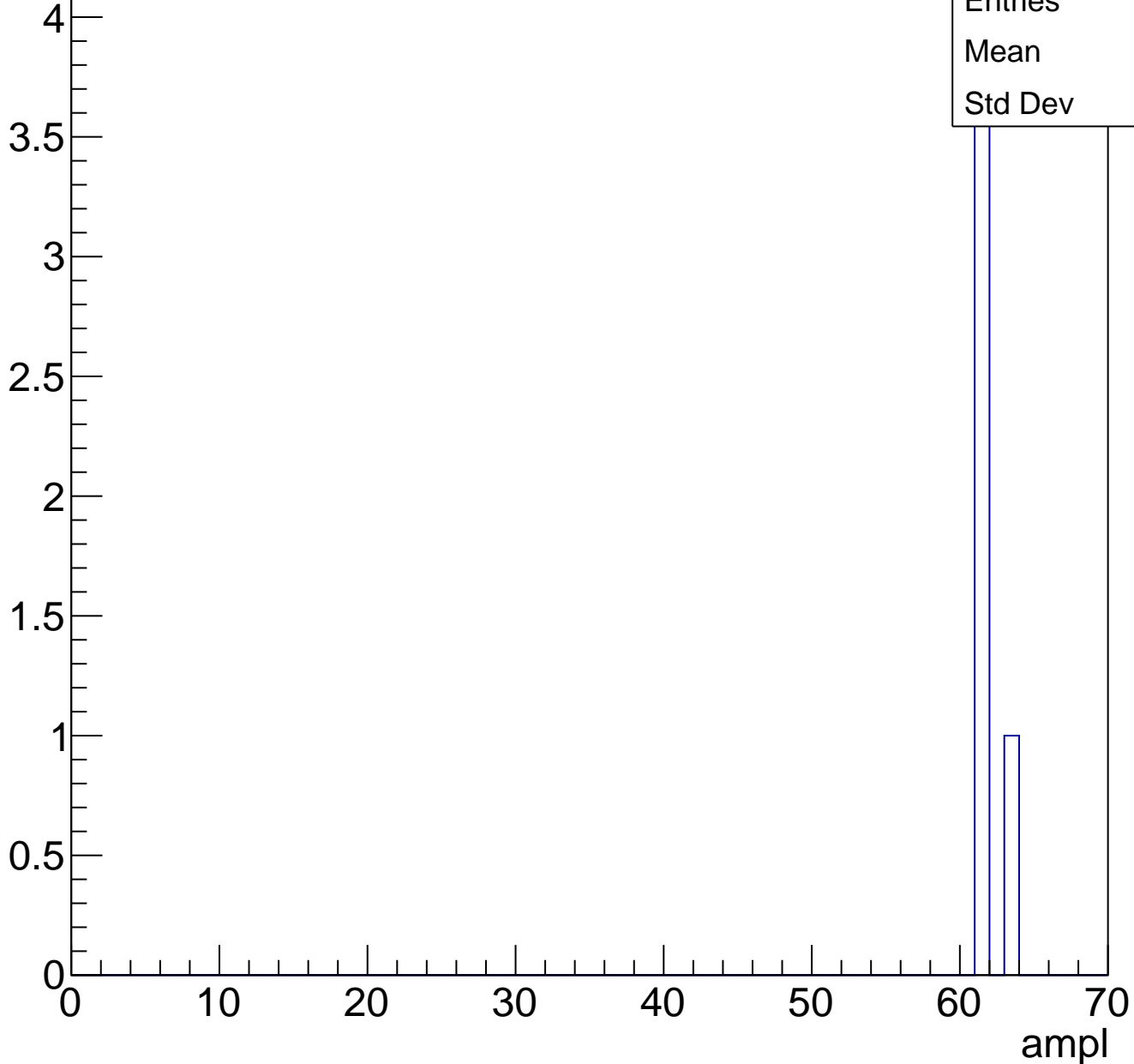
ampl



# B1L102S, U12-ch50, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U12-ch50, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L102S, U12-ch51, adc0

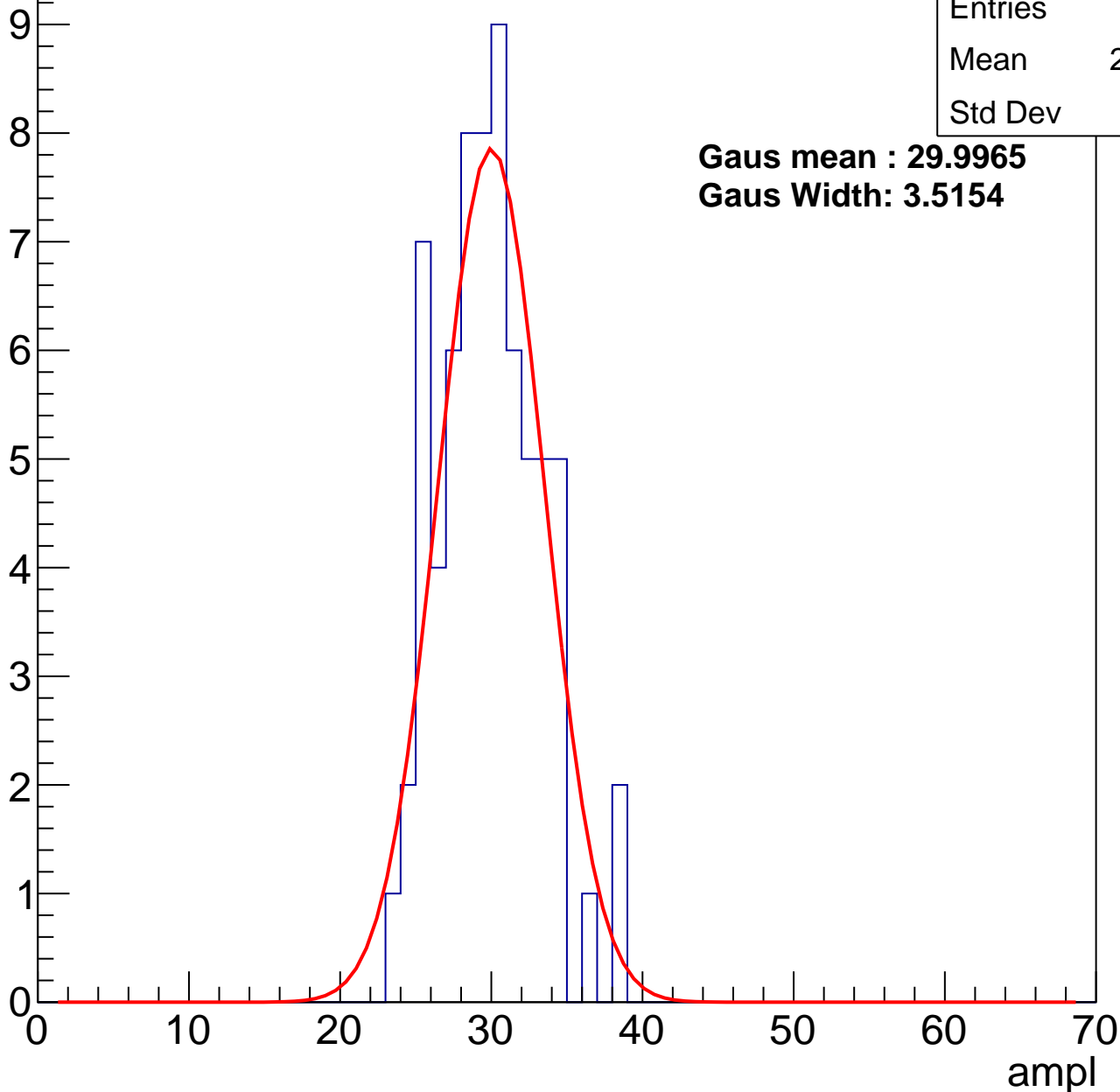
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	29.43
Std Dev	3.29

**Gaus mean : 29.9965**

**Gaus Width: 3.5154**



# B1L102S, U12-ch51, adc1

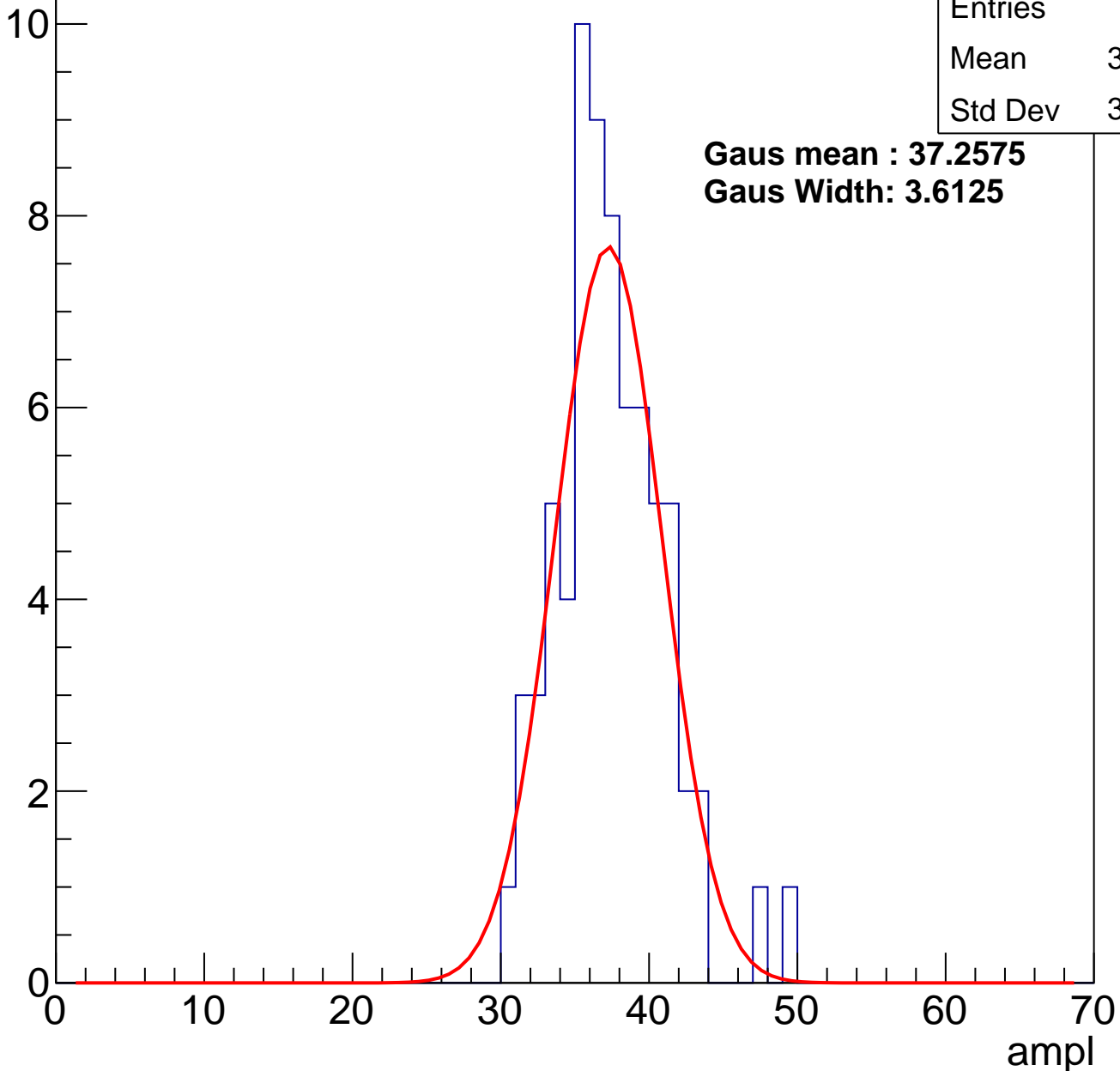
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	71
Mean	36.94
Std Dev	3.595

**Gaus mean : 37.2575**

**Gaus Width: 3.6125**

Entry



# B1L102S, U12-ch51, adc2

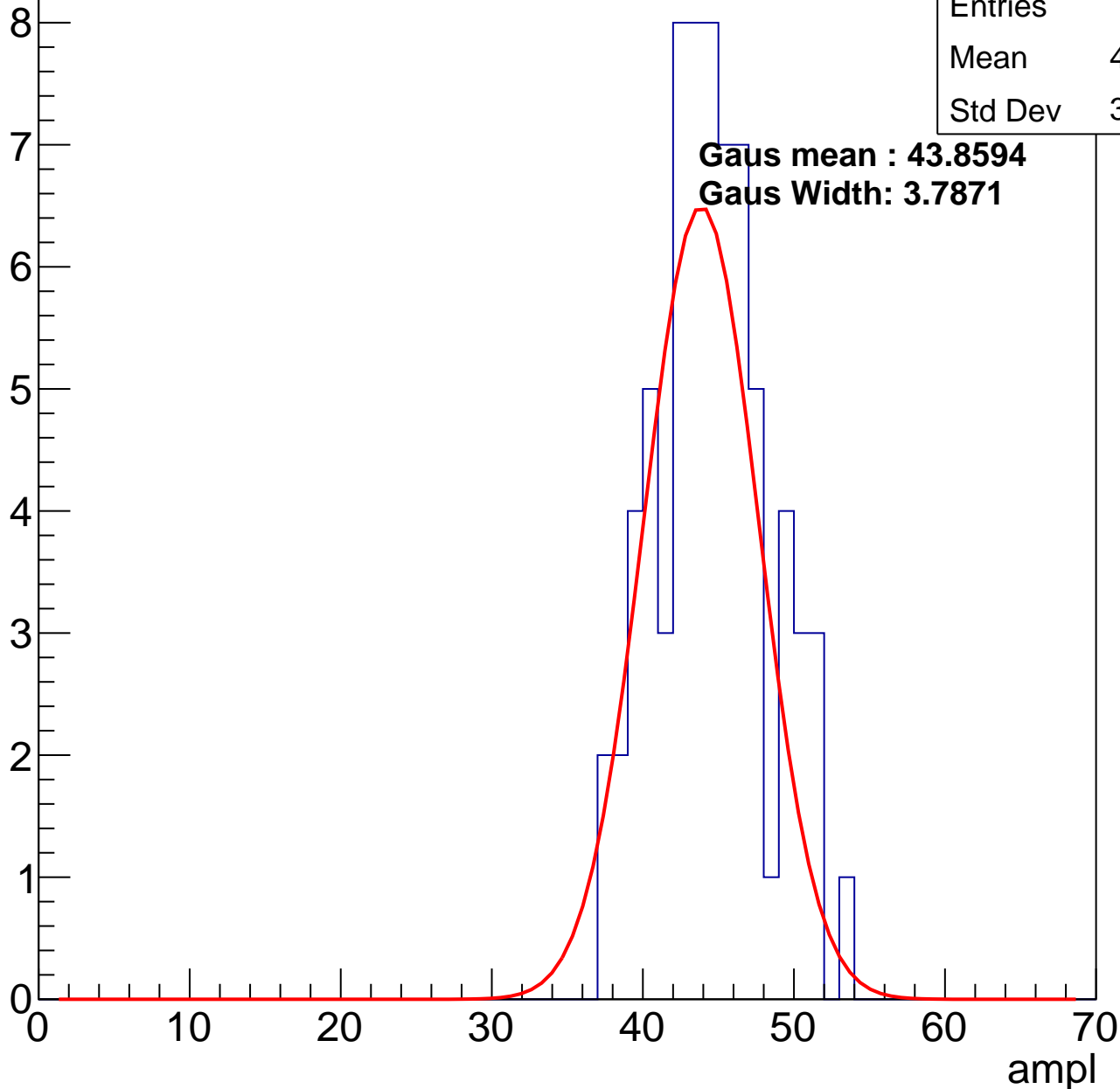
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	71
Mean	44.13
Std Dev	3.654

**Gaus mean : 43.8594**

**Gaus Width: 3.7871**

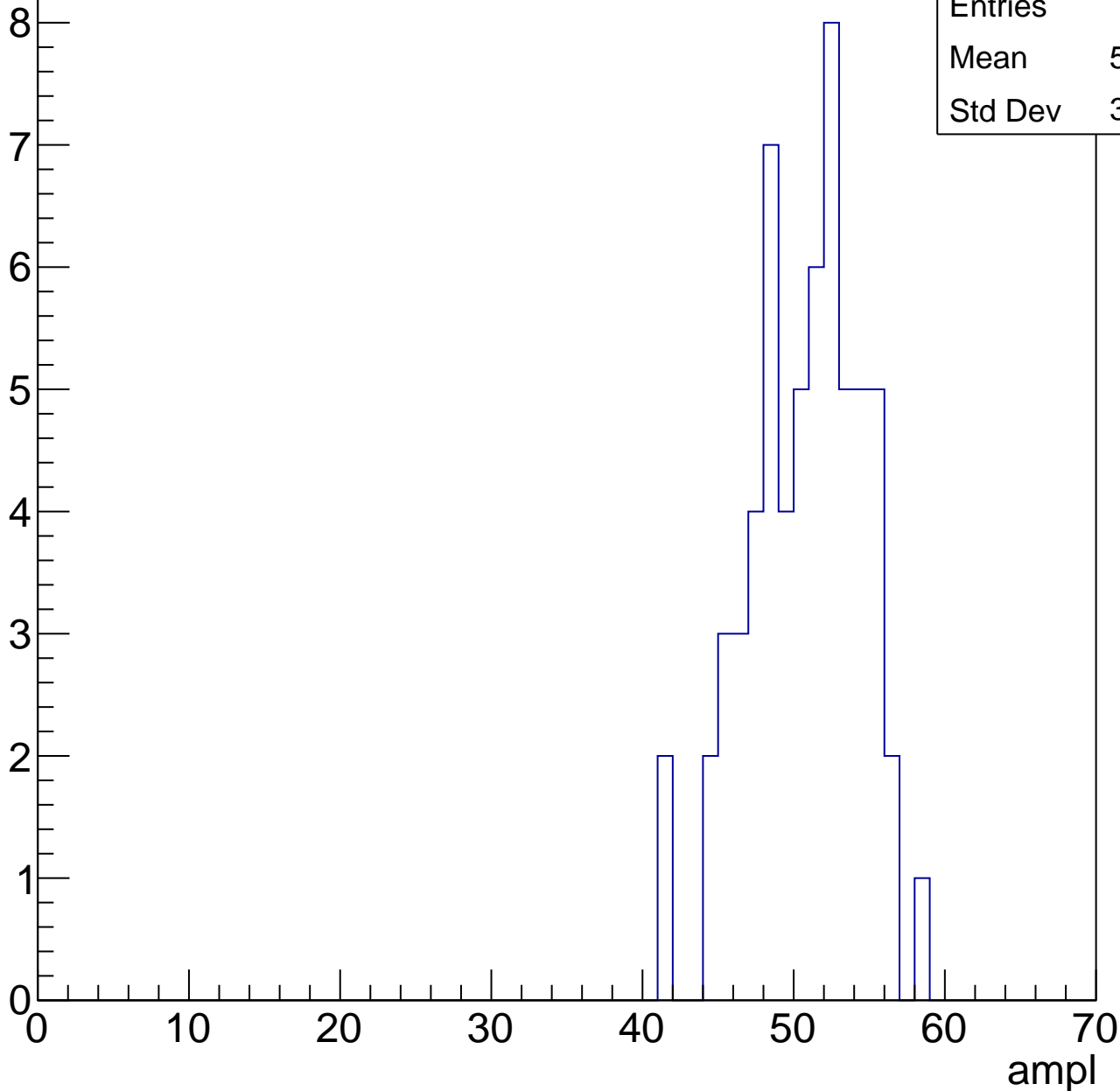


# B1L102S, U12-ch51, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

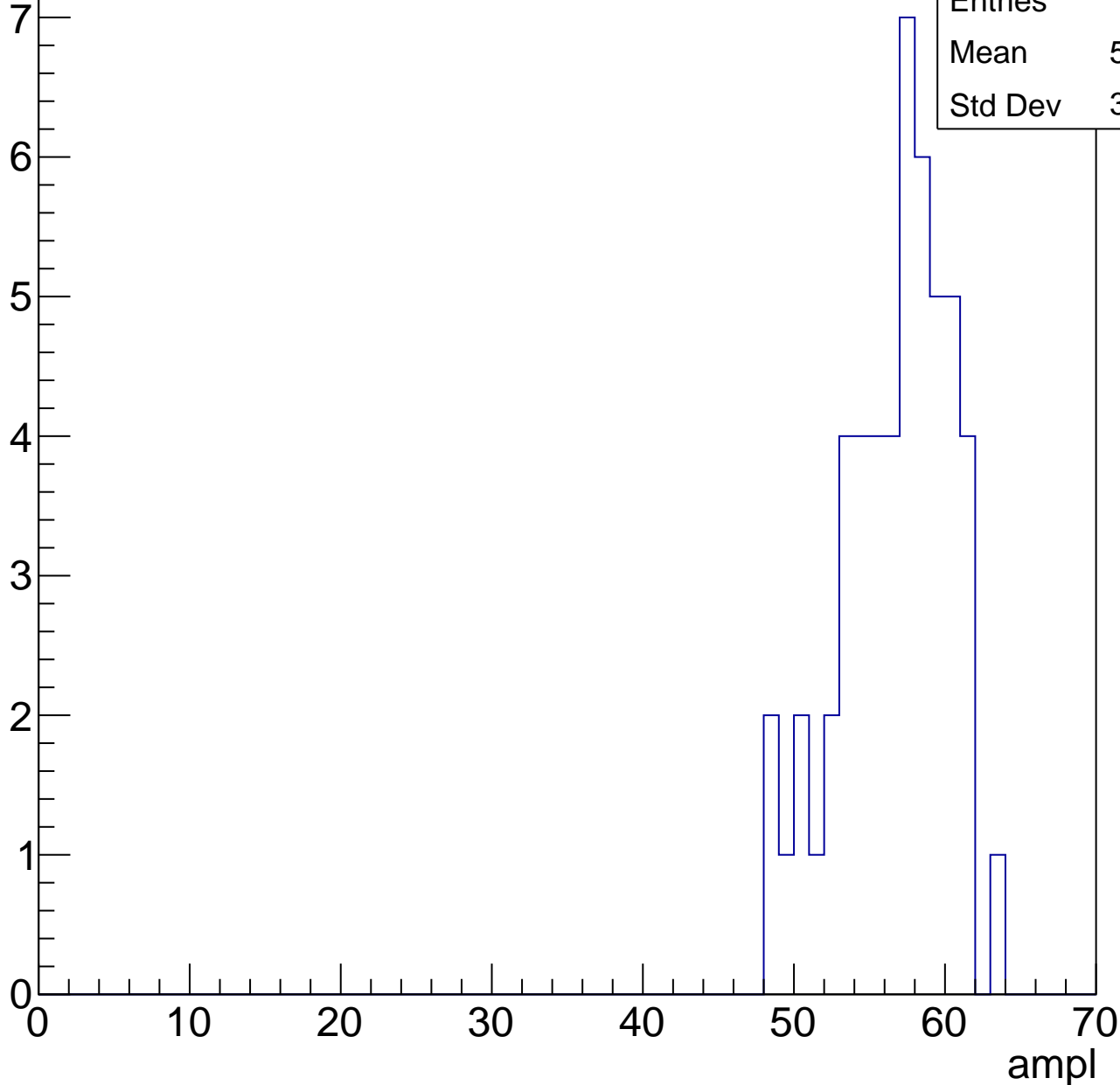
Entries	62
Mean	50.24
Std Dev	3.693



# B1L102S, U12-ch51, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

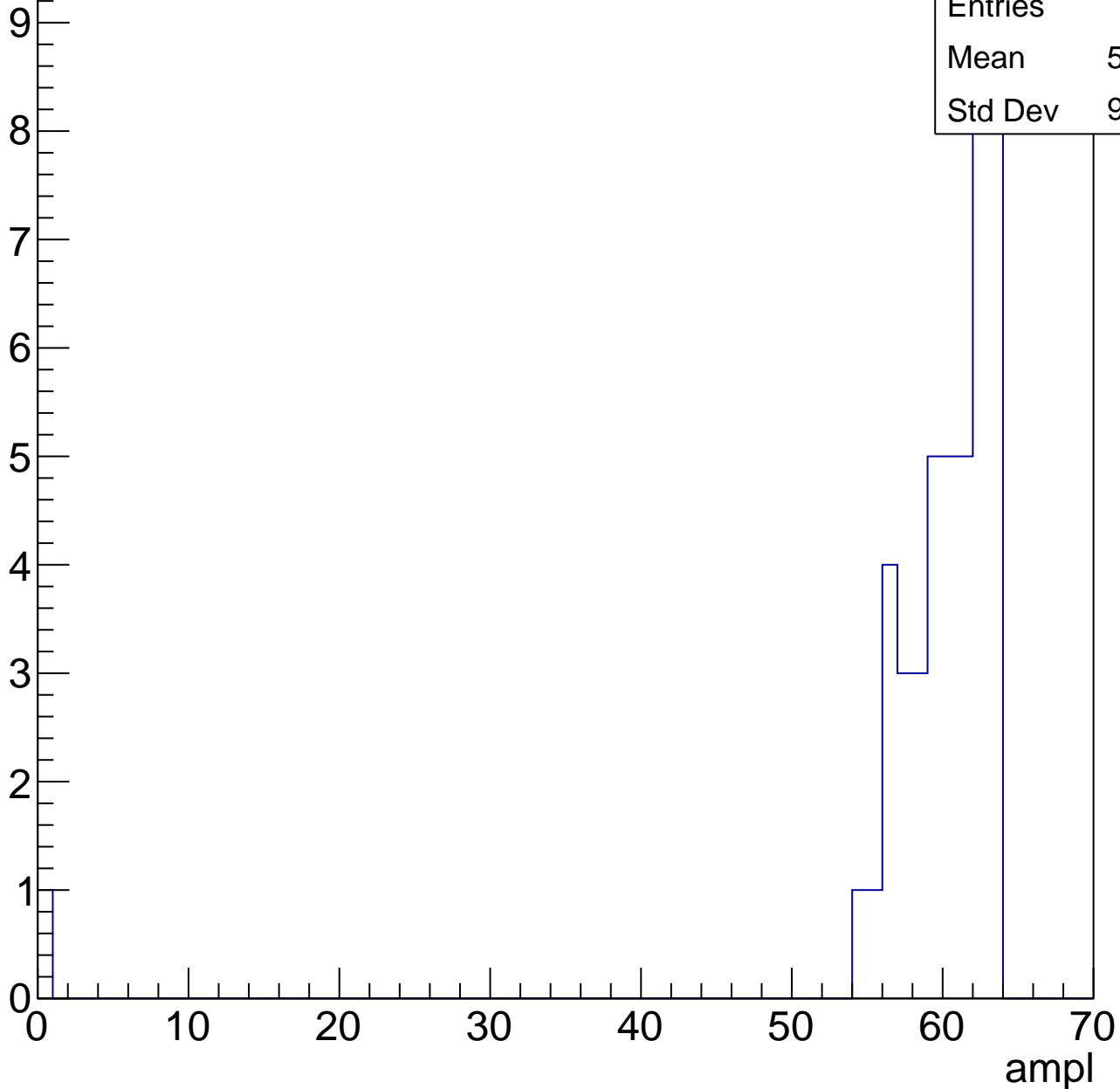


# B1L102S, U12-ch51, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	46
Mean	58.76
Std Dev	9.113



# B1L102S, U12-ch51, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U12-ch51, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U12-ch52, adc0

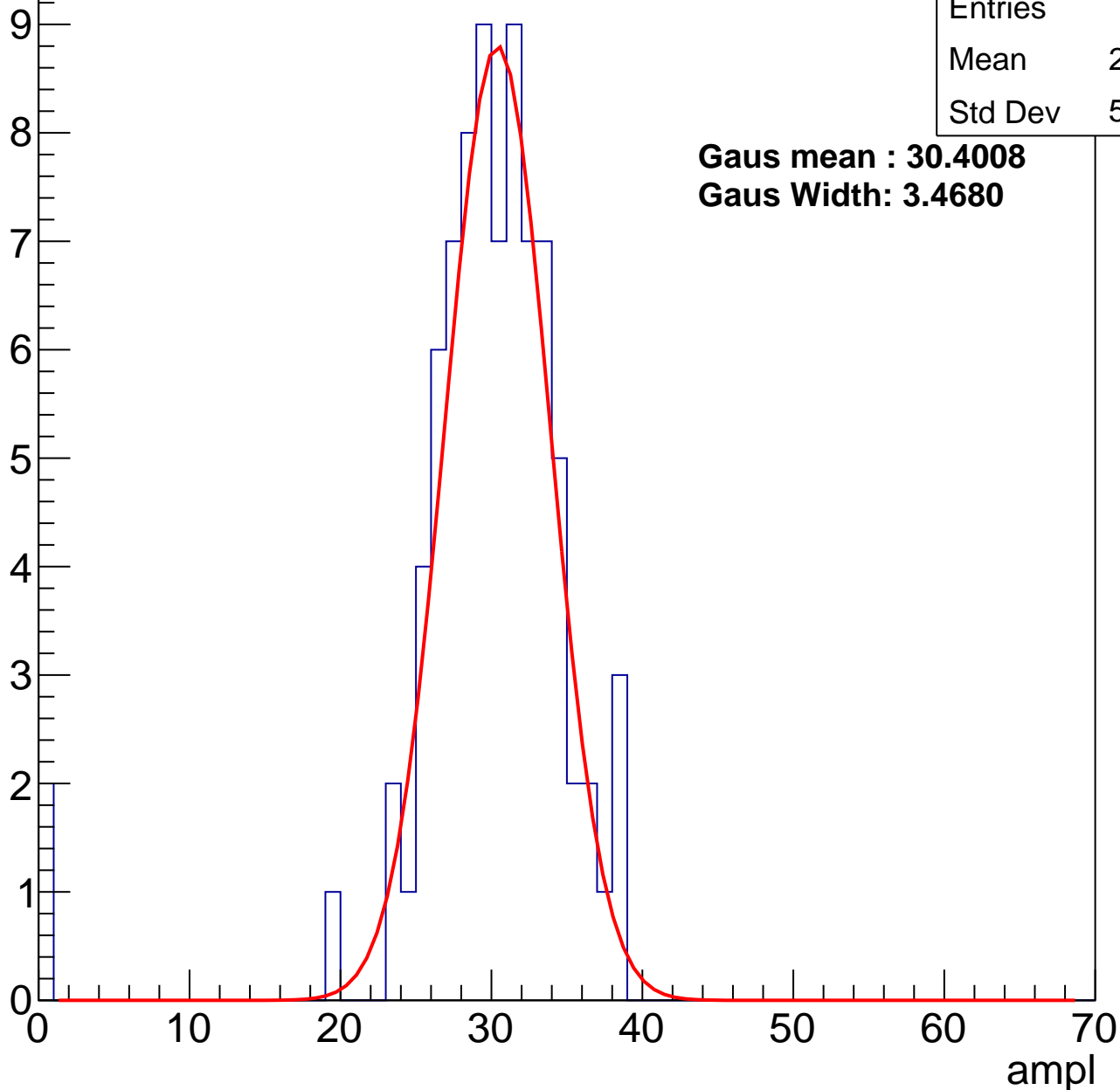
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	83
Mean	29.23
Std Dev	5.858

**Gaus mean : 30.4008**

**Gaus Width: 3.4680**



# B1L102S, U12-ch52, adc1

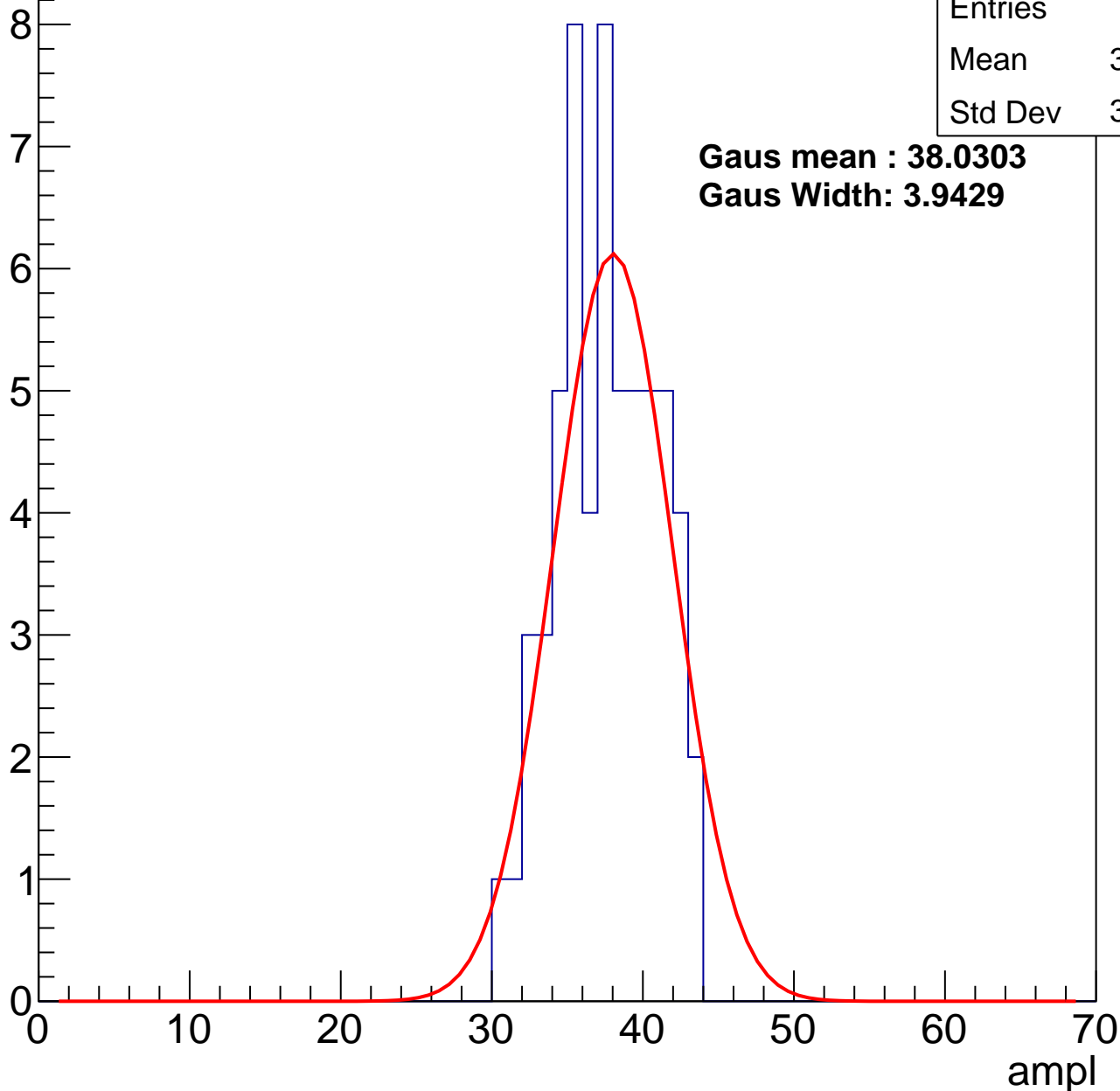
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	59
Mean	37.12
Std Dev	3.216

**Gaus mean : 38.0303**

**Gaus Width: 3.9429**



# B1L102S, U12-ch52, adc2

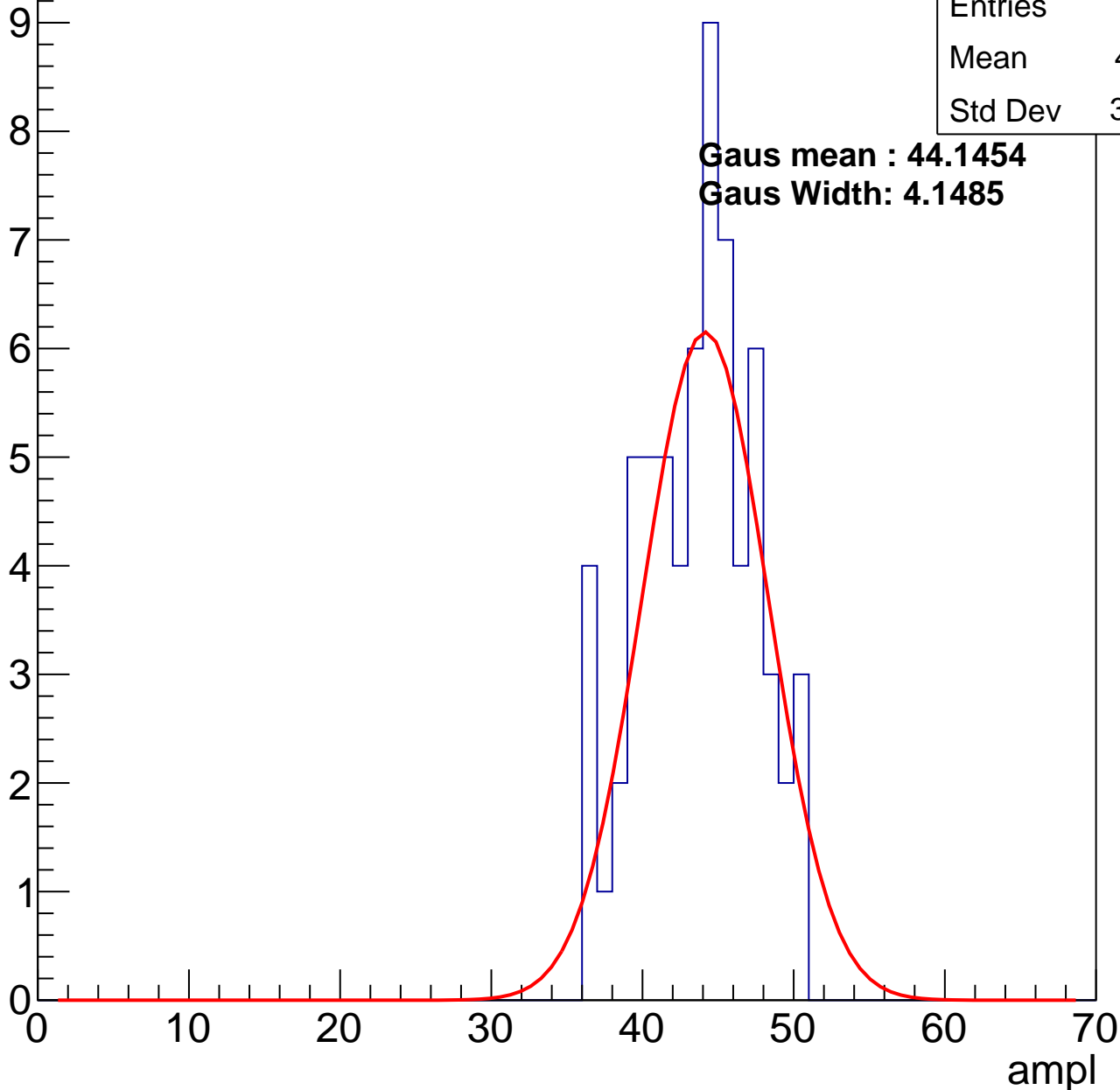
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	43.21
Std Dev	3.674

**Gaus mean : 44.1454**

**Gaus Width: 4.1485**

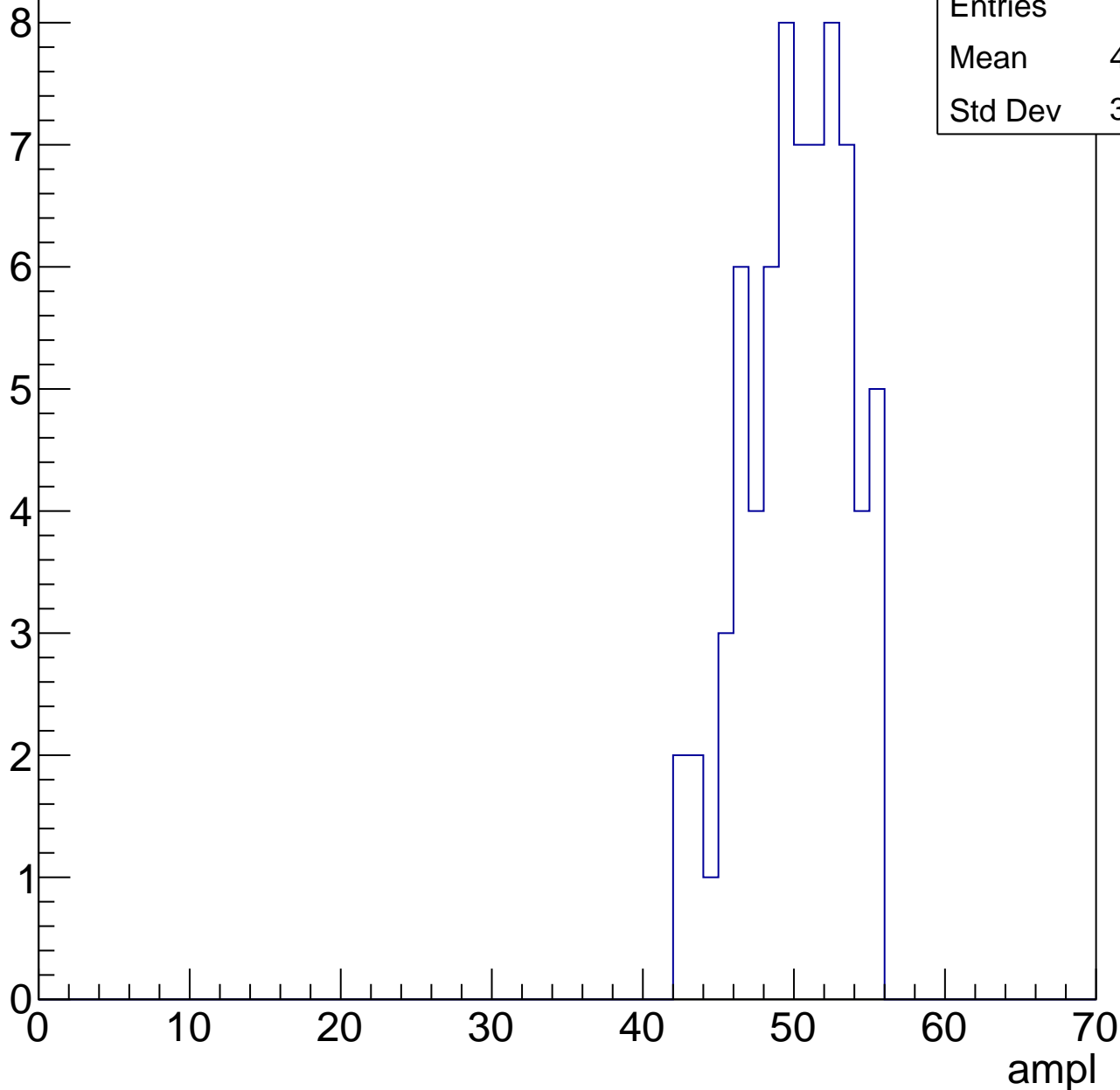


# B1L102S, U12-ch52, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	70
Mean	49.69
Std Dev	3.349

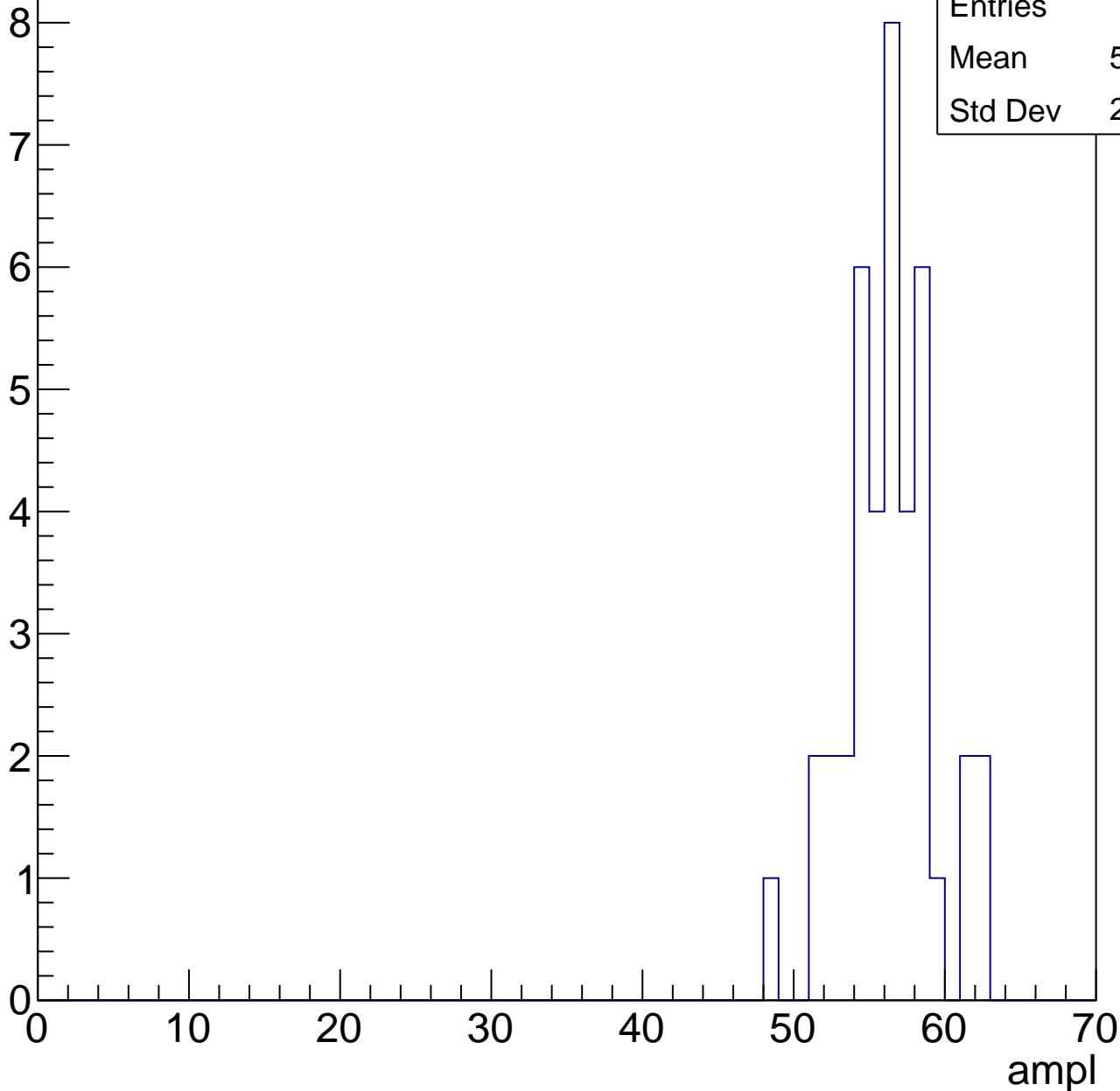


# B1L102S, U12-ch52, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	40
Mean	55.83
Std Dev	2.957



# B1L102S, U12-ch52, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

10

8

6

4

2

0

0

10

20

30

40

50

60

ampl

Entries

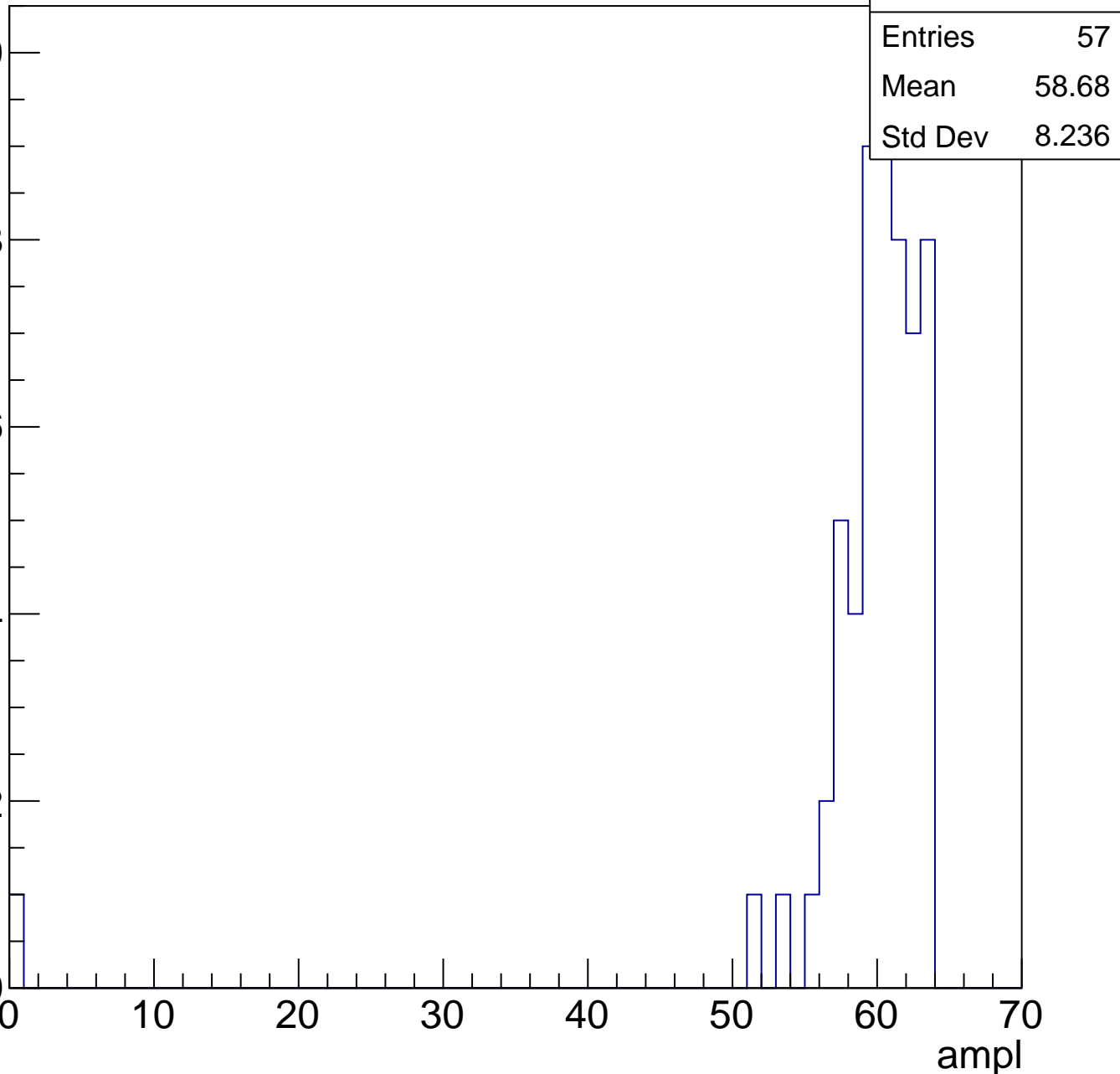
57

Mean

58.68

Std Dev

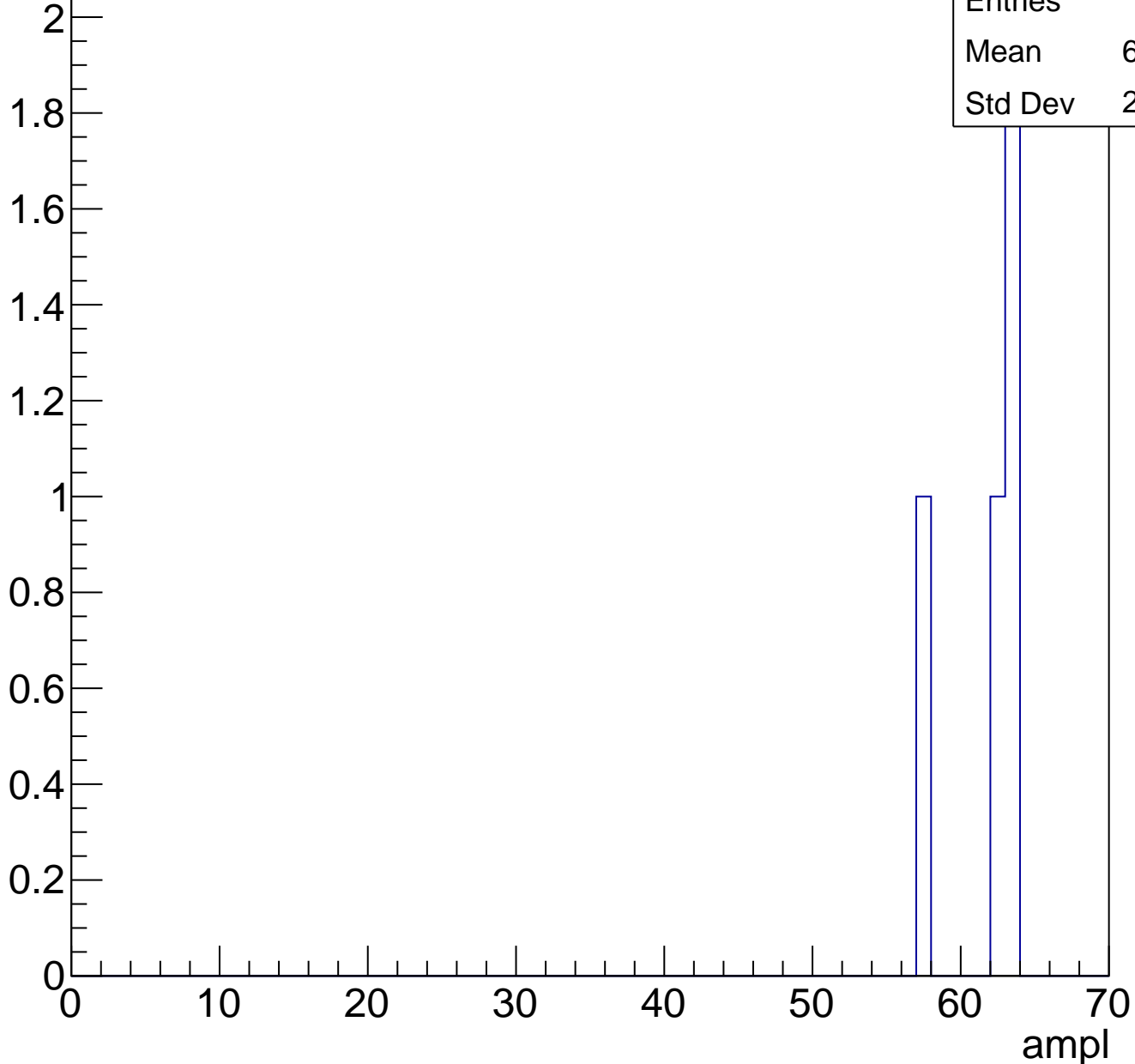
8.236



# B1L102S, U12-ch52, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U12-ch52, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U12-ch53, adc0

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	95
Mean	28.08
Std Dev	5.04

**Gaus mean : 28.7932**

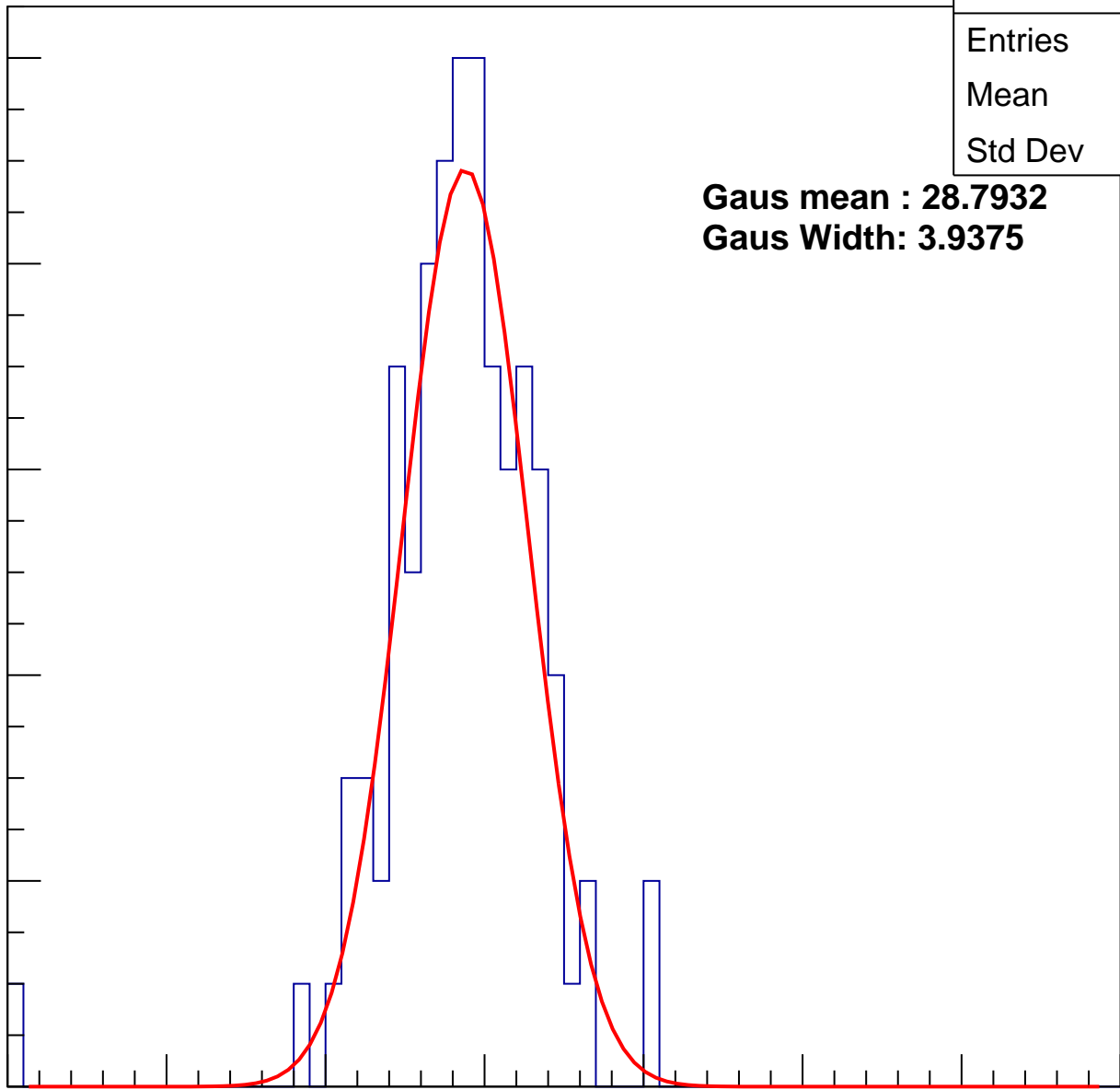
**Gaus Width: 3.9375**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L102S, U12-ch53, adc1

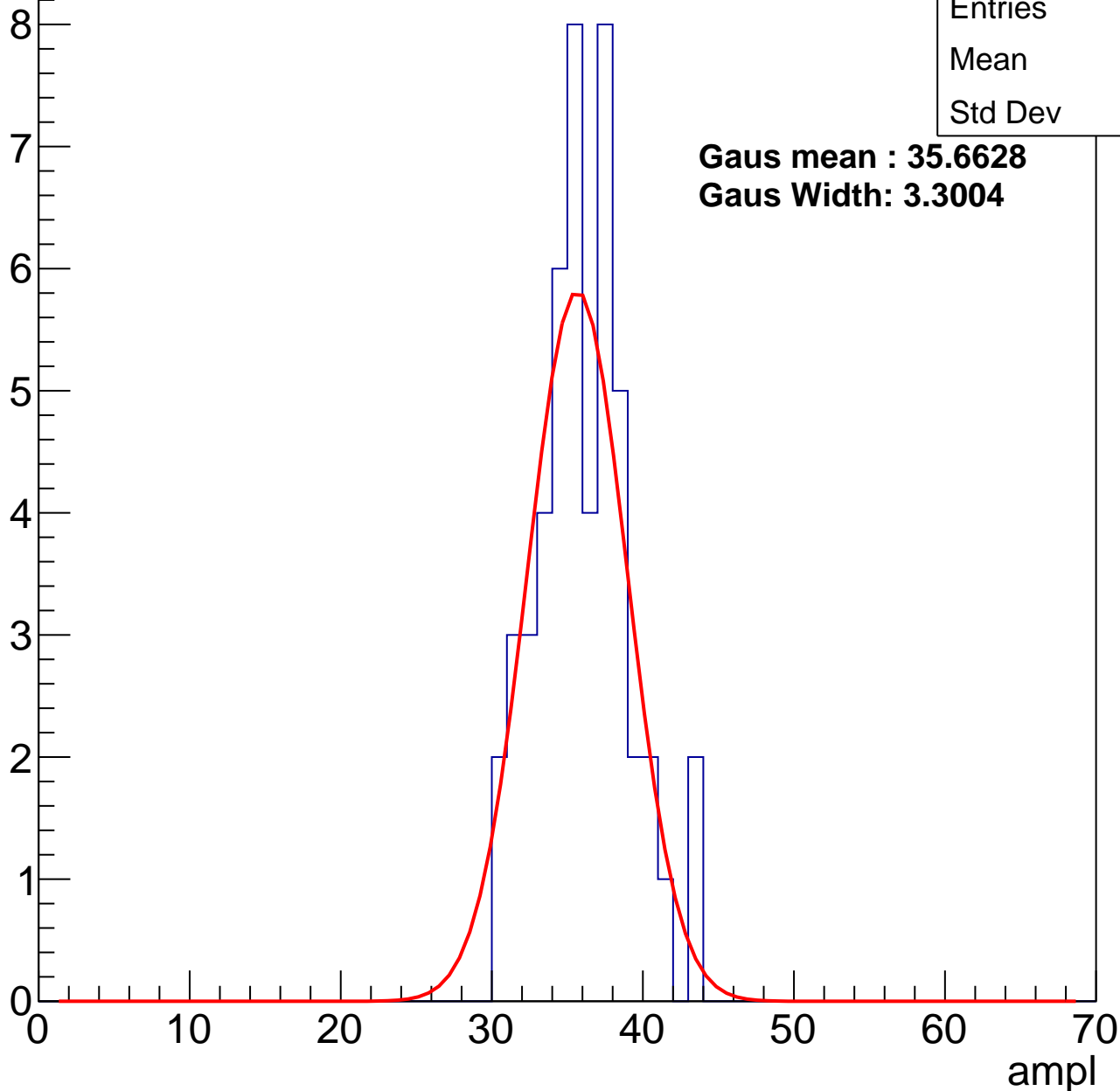
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	50
Mean	35.6
Std Dev	3.02

**Gaus mean : 35.6628**

**Gaus Width: 3.3004**



# B1L102S, U12-ch53, adc2

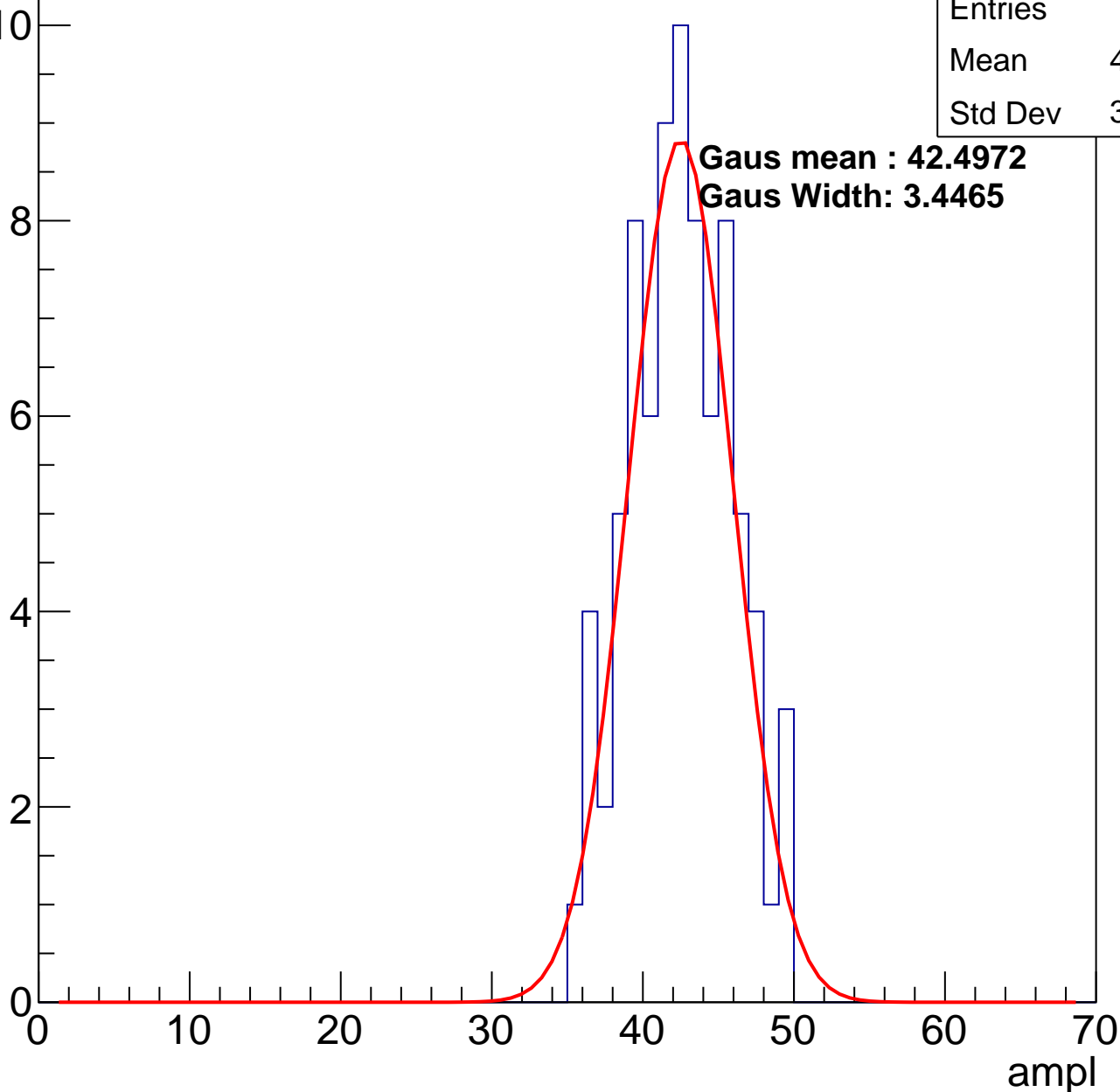
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	80
Mean	42.06
Std Dev	3.344

**Gaus mean : 42.4972**

**Gaus Width: 3.4465**

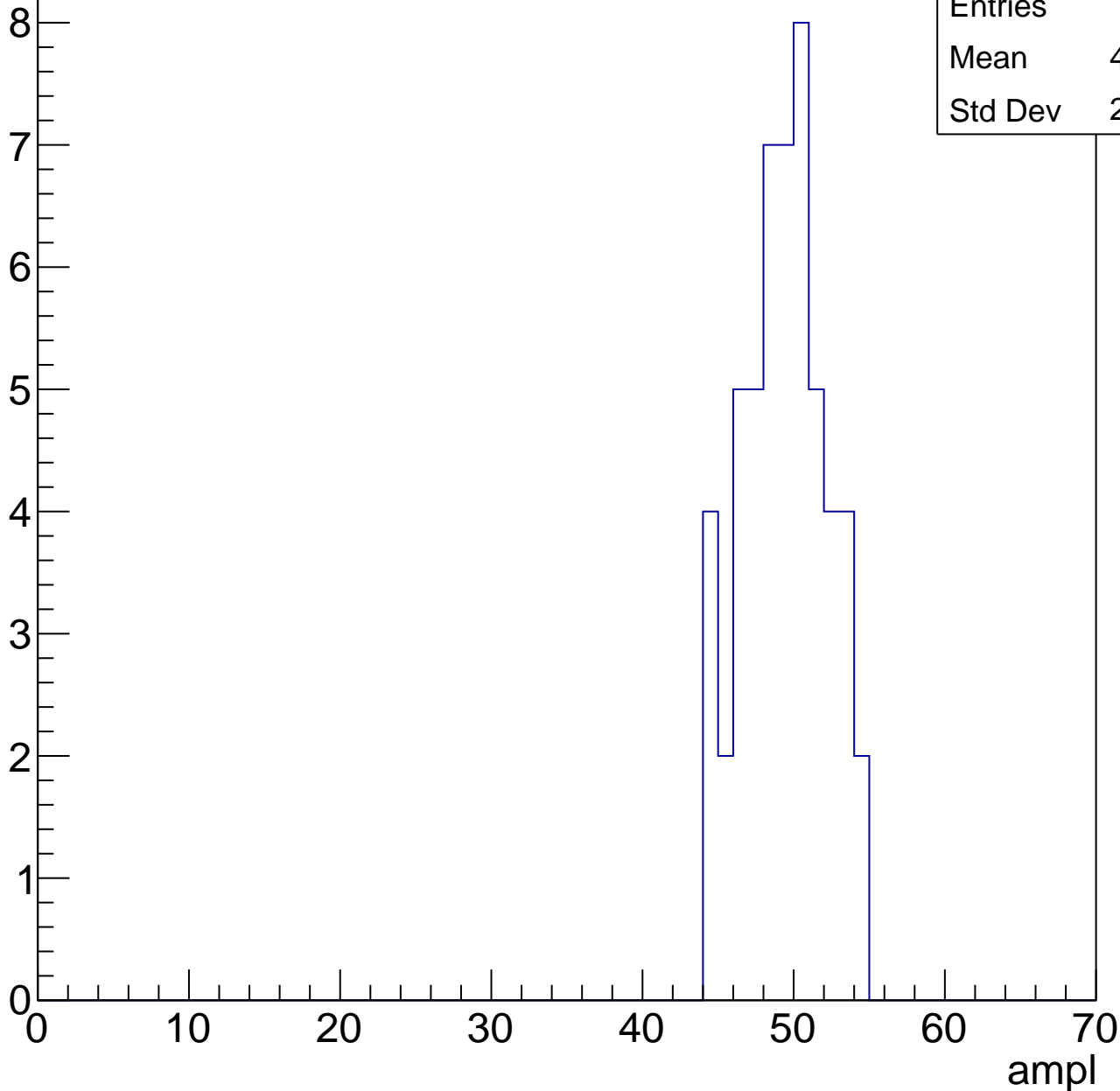


# B1L102S, U12-ch53, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	53
Mean	48.92
Std Dev	2.684

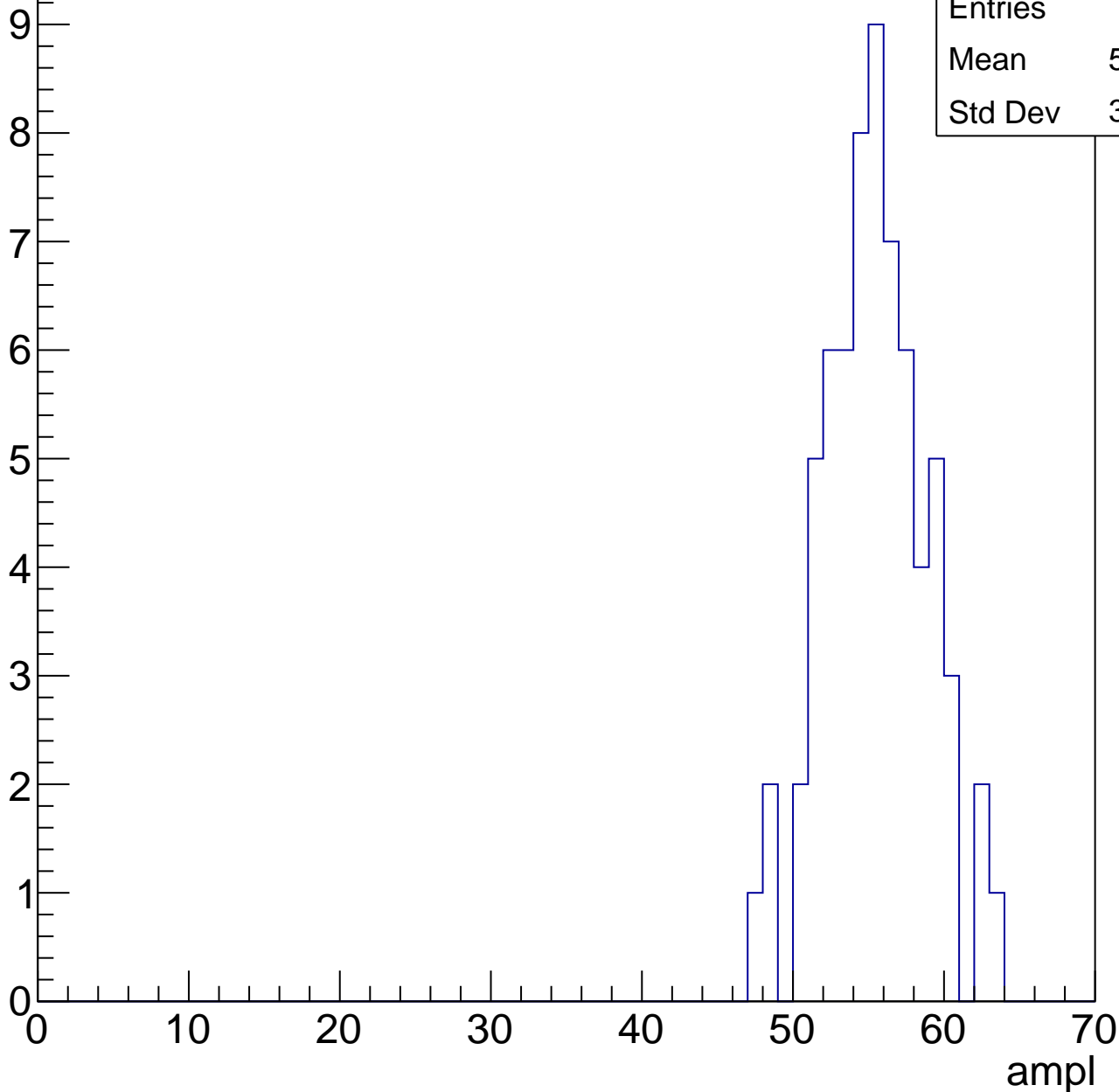


# B1L102S, U12-ch53, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	67
Mean	54.97
Std Dev	3.372



# B1L102S, U12-ch53, adc5

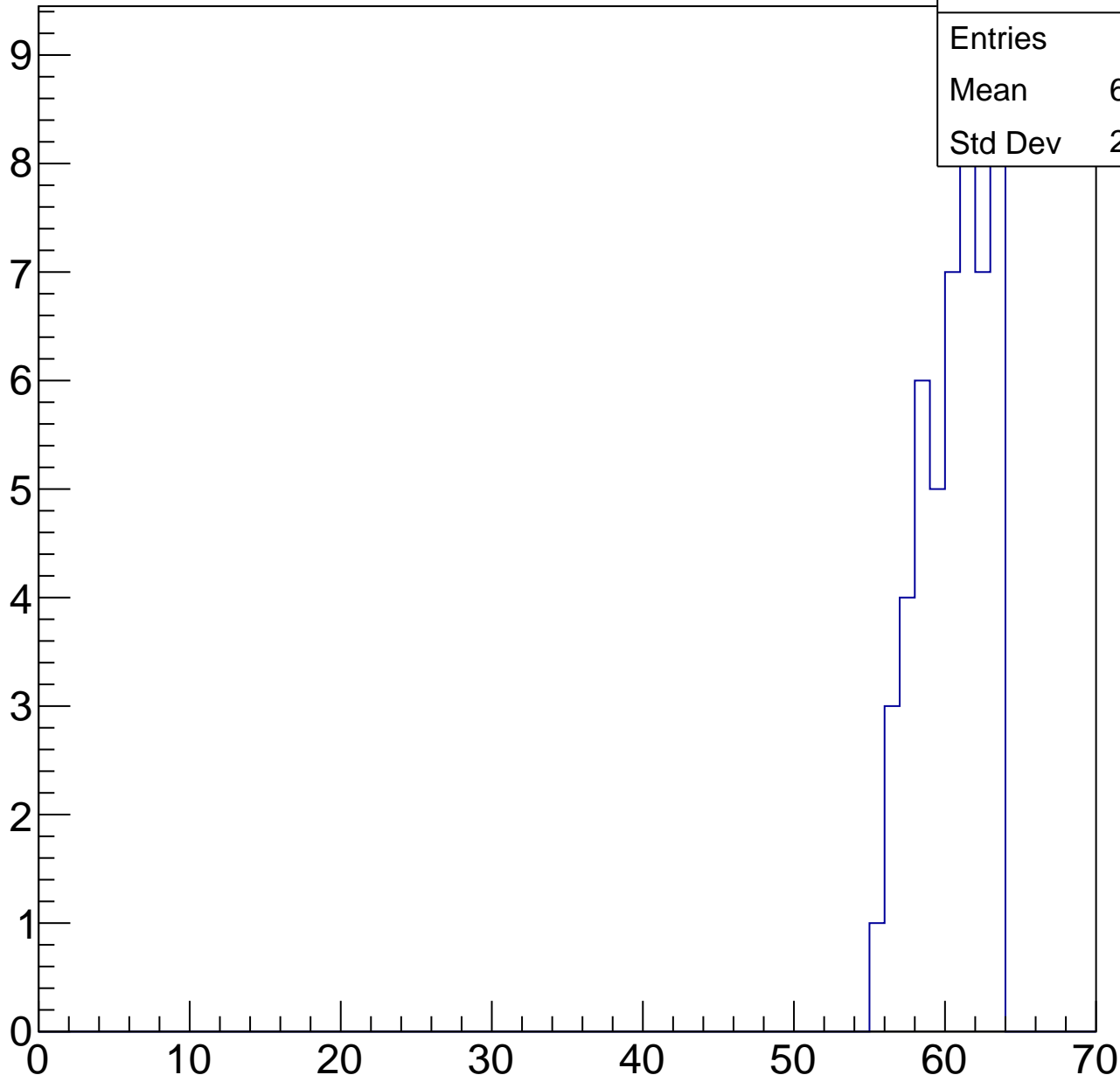
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	50
Mean	60.02
Std Dev	2.223

ampl



# B1L102S, U12-ch53, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U12-ch53, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L102S, U12-ch54, adc0

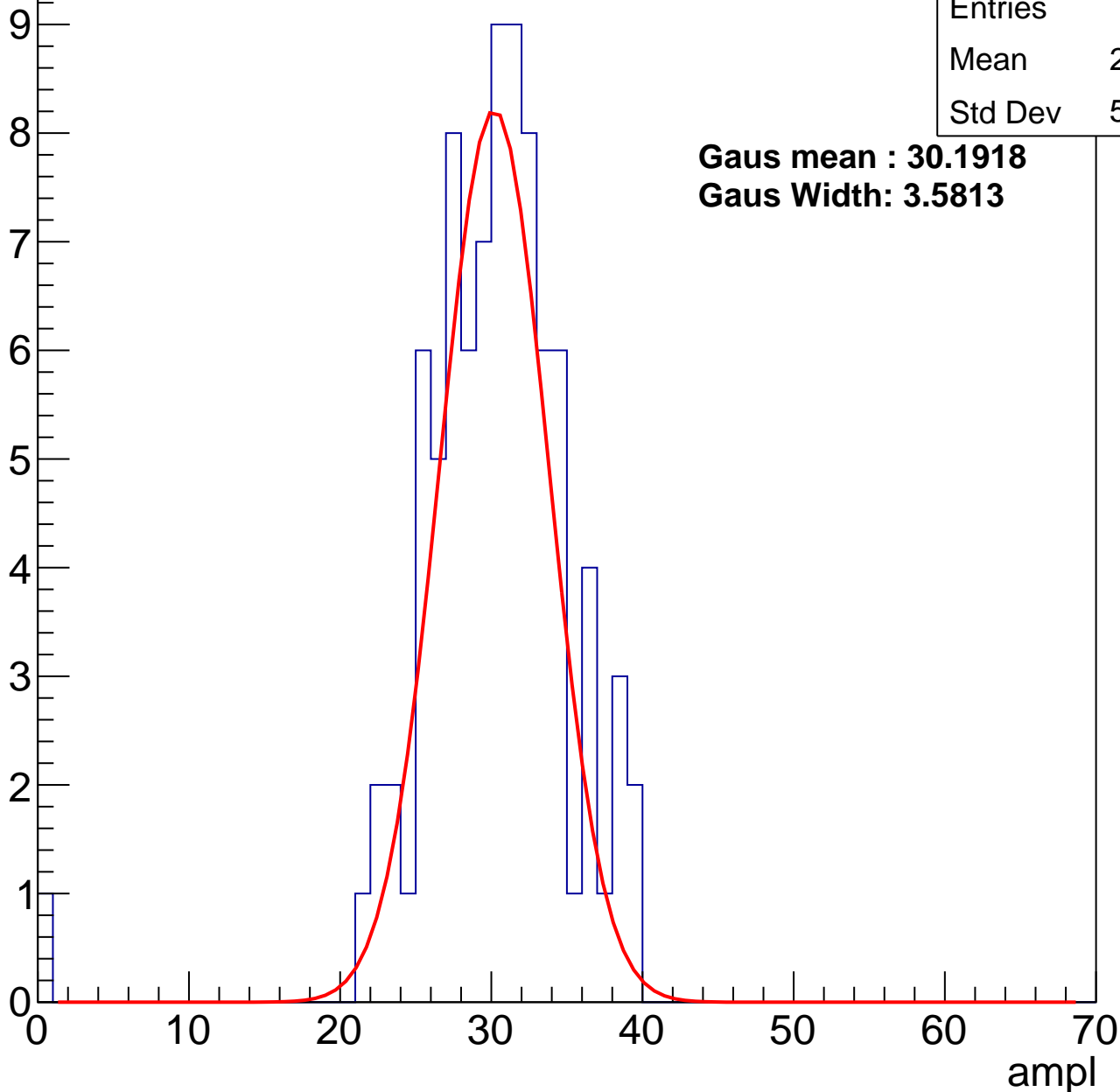
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	88
Mean	29.74
Std Dev	5.149

**Gaus mean : 30.1918**

**Gaus Width: 3.5813**



# B1L102S, U12-ch54, adc1

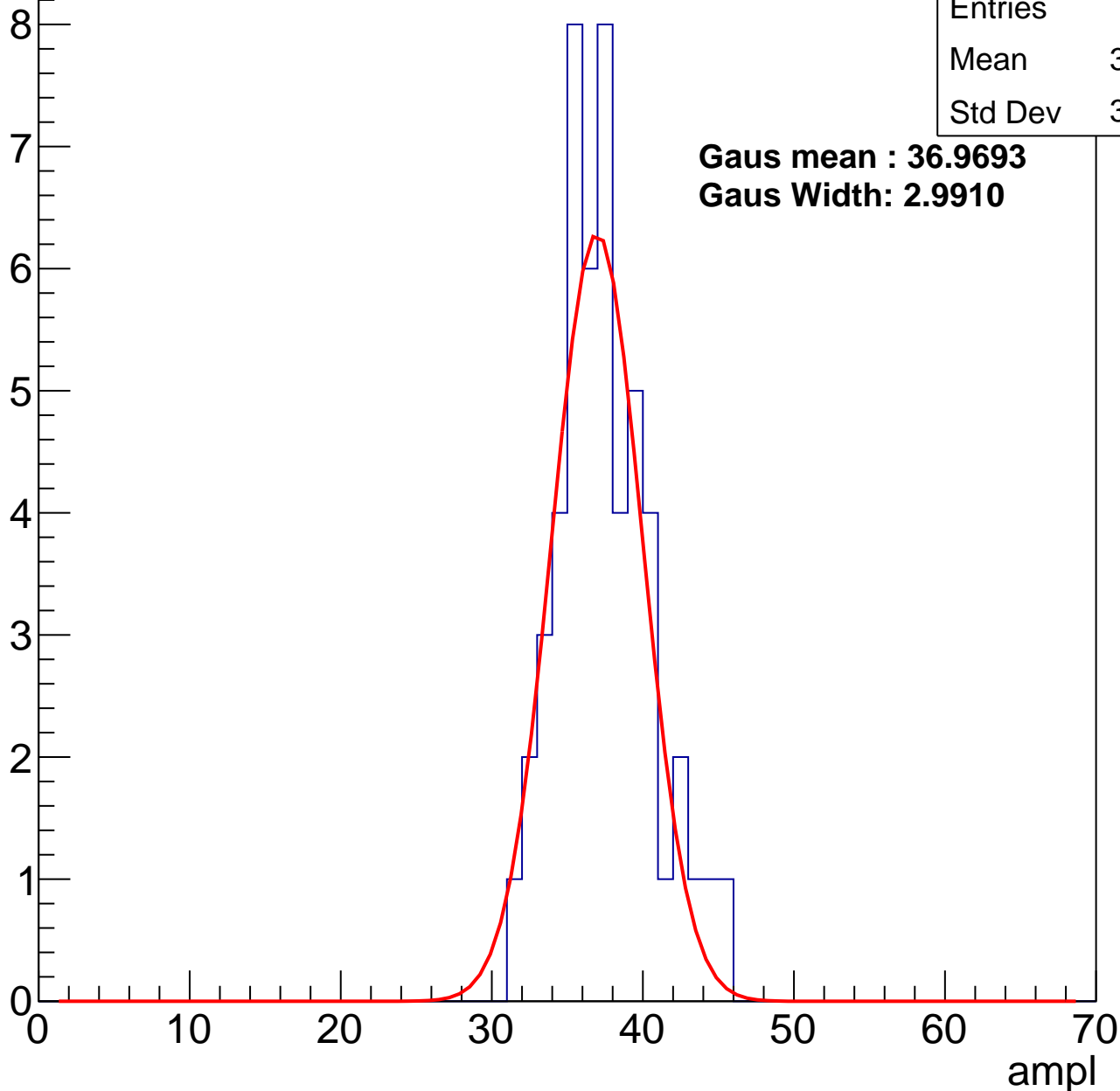
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	51
Mean	36.98
Std Dev	3.077

**Gaus mean : 36.9693**

**Gaus Width: 2.9910**



# B1L102S, U12-ch54, adc2

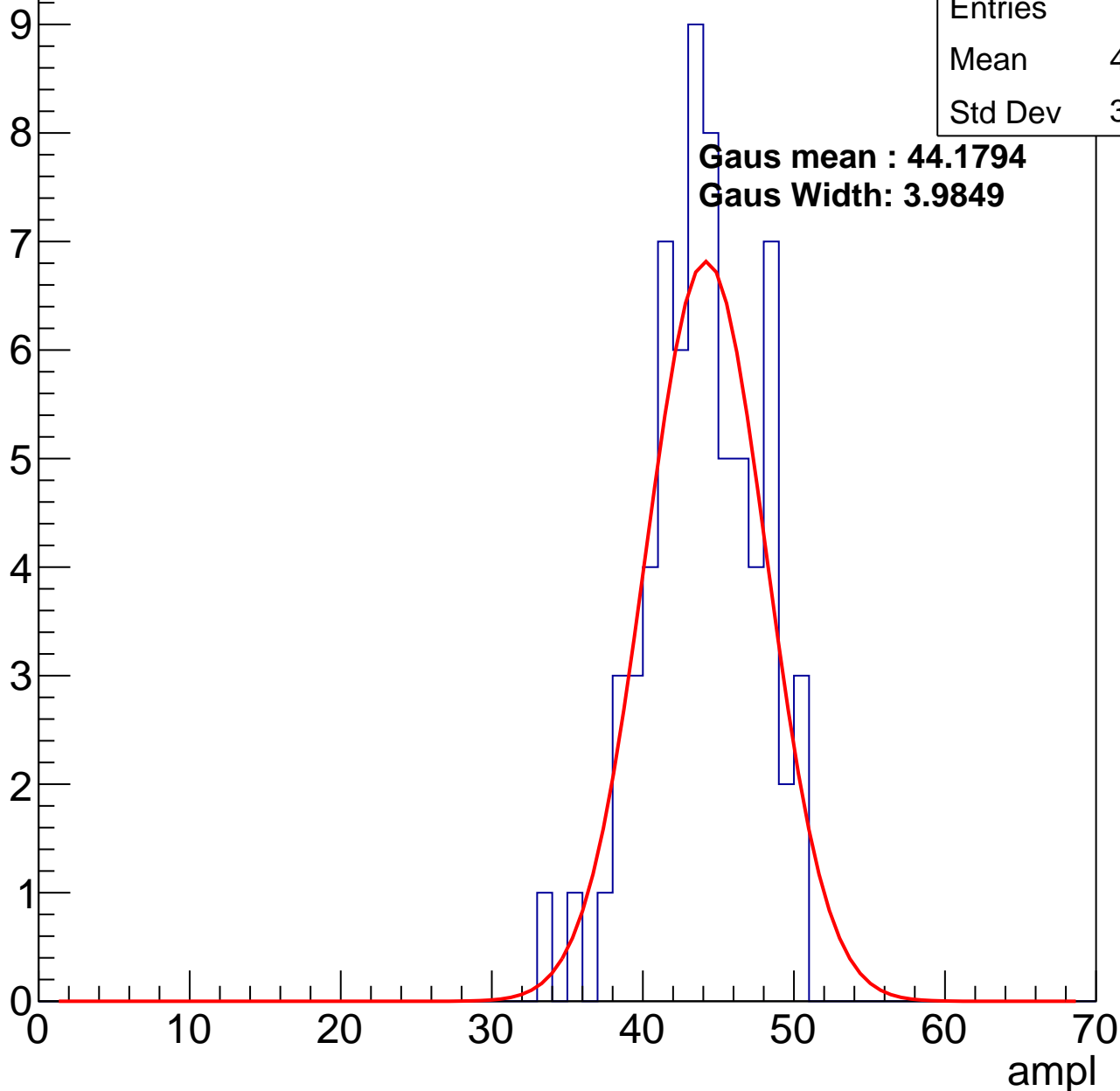
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	43.49
Std Dev	3.626

**Gaus mean : 44.1794**

**Gaus Width: 3.9849**

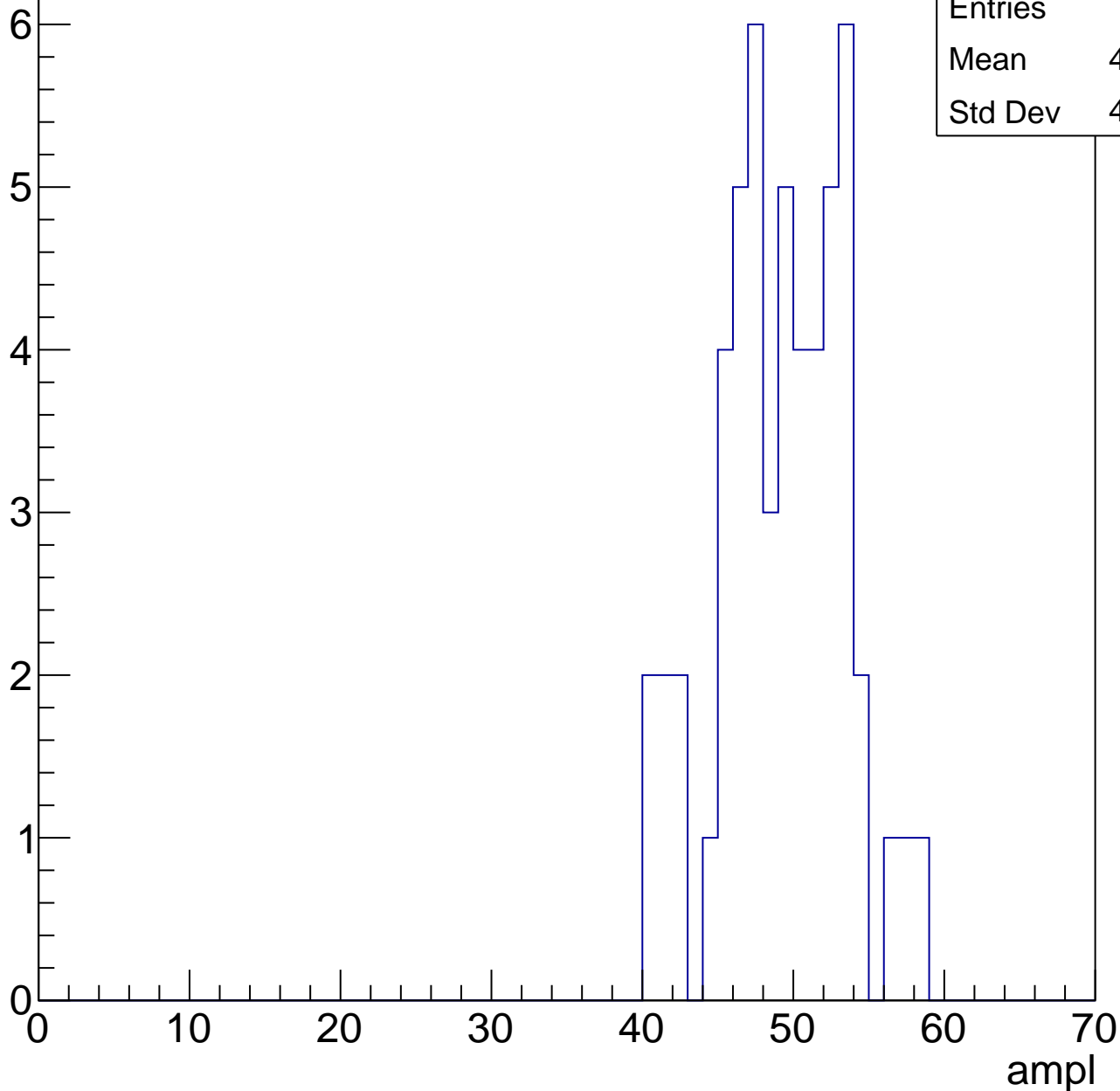


# B1L102S, U12-ch54, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	54
Mean	48.74
Std Dev	4.195

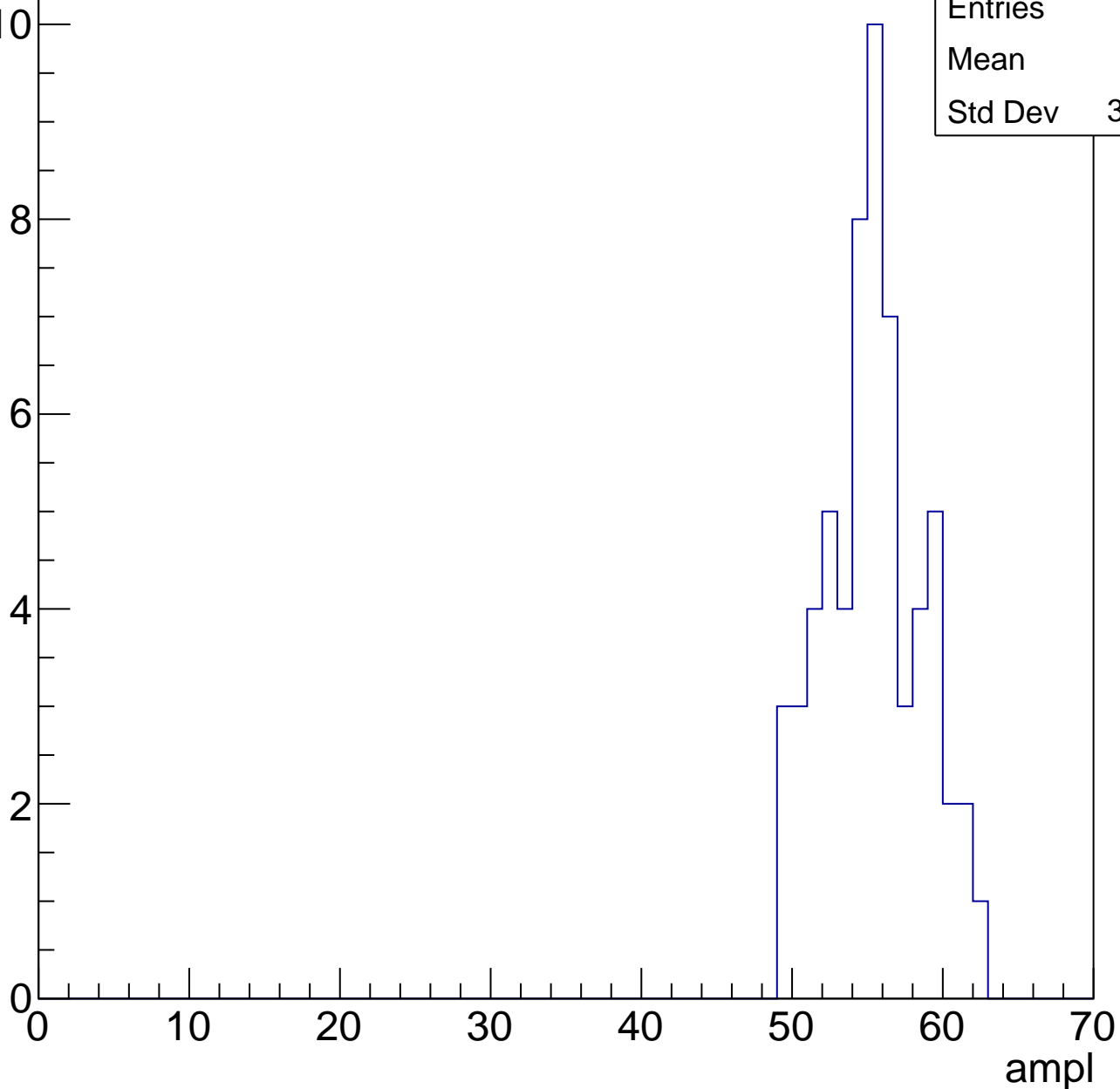


# B1L102S, U12-ch54, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	54.9
Std Dev	3.192

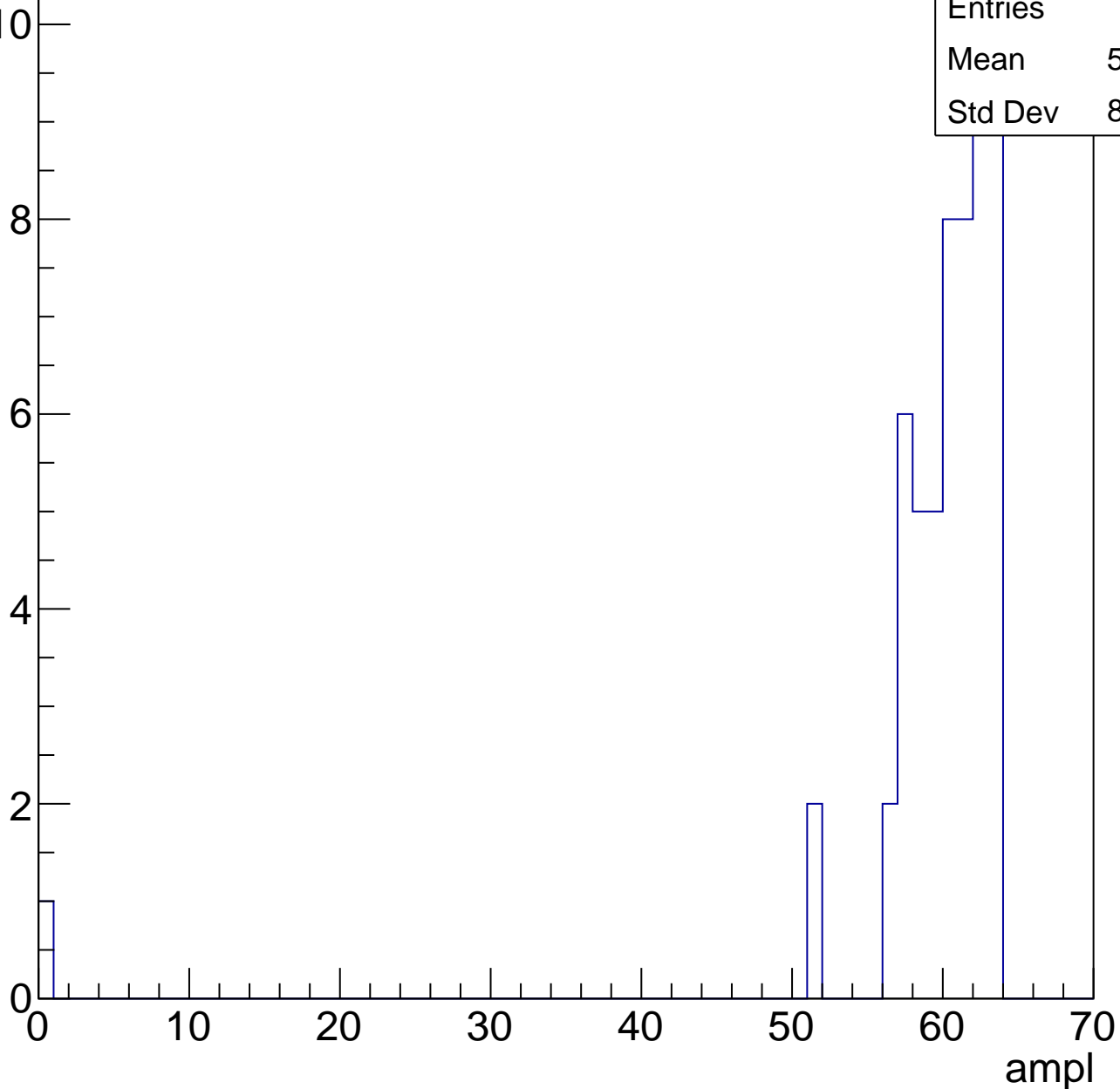


# B1L102S, U12-ch54, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	56
Mean	58.88
Std Dev	8.384



# B1L102S, U12-ch54, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0



# B1L102S, U12-ch54, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U12-ch55, adc0

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	84
Mean	29.55
Std Dev	4.868

**Gaus mean : 30.2437**

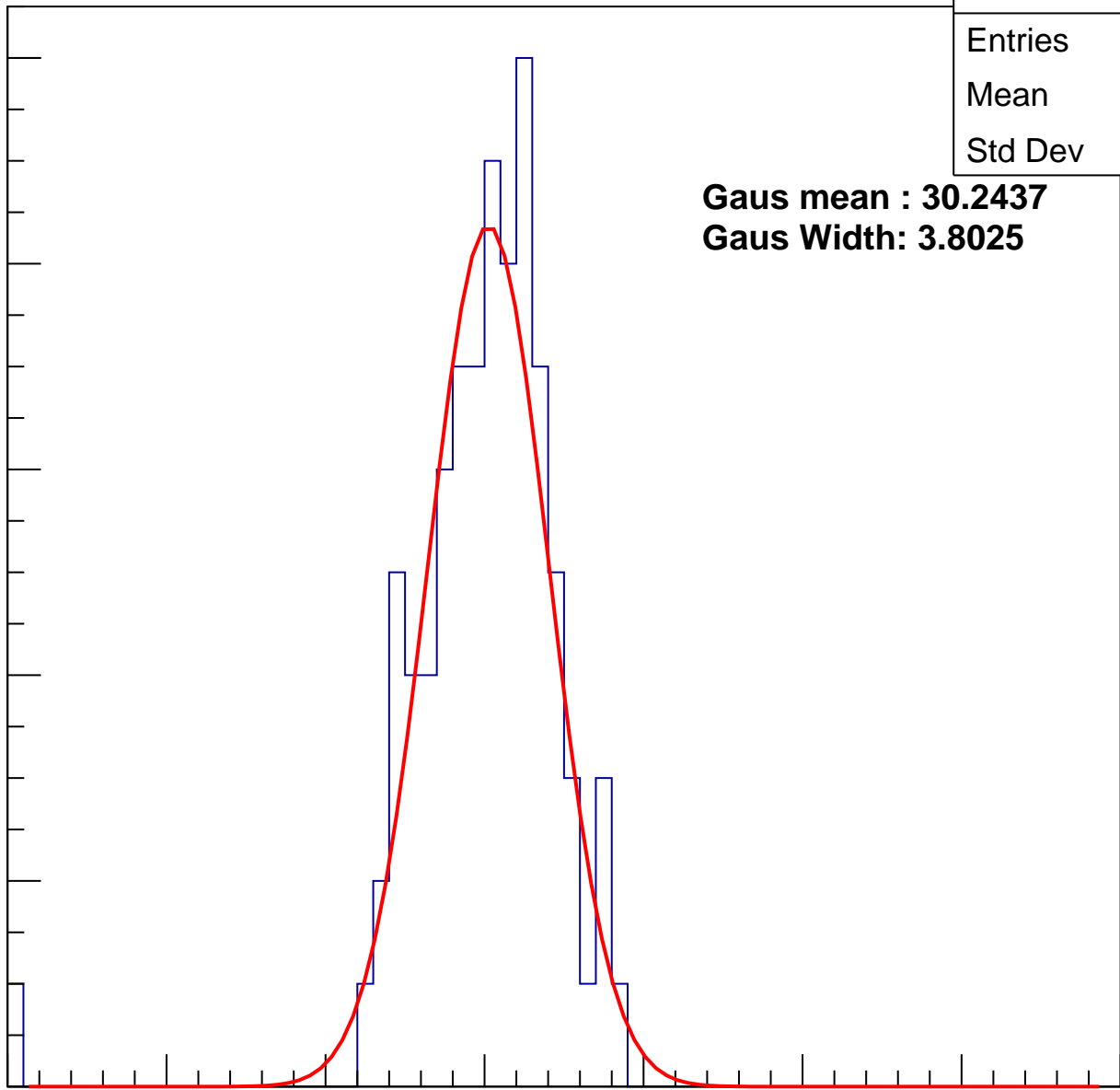
**Gaus Width: 3.8025**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L102S, U12-ch55, adc1

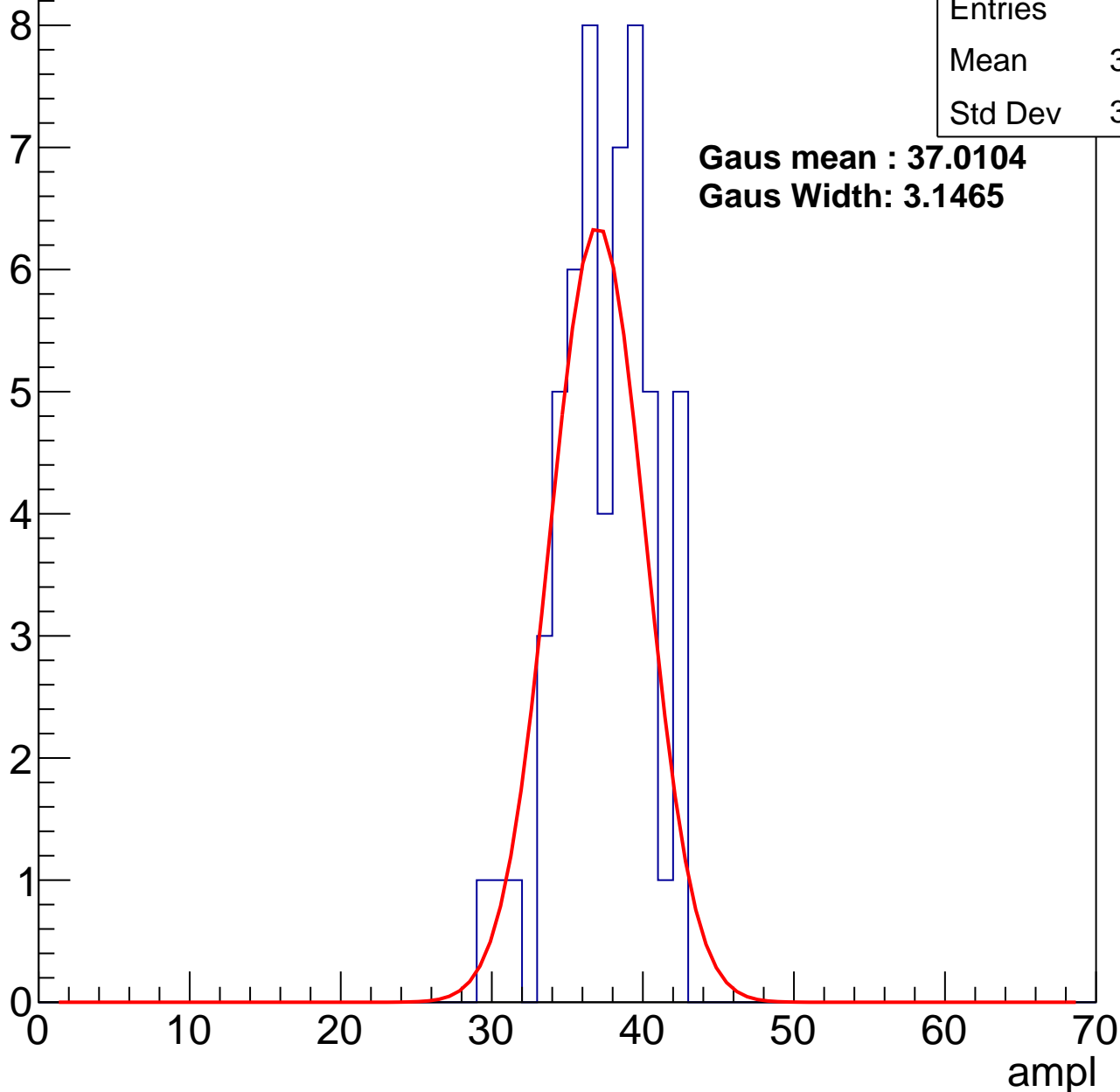
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	55
Mean	36.98
Std Dev	3.012

**Gaus mean : 37.0104**

**Gaus Width: 3.1465**



# B1L102S, U12-ch55, adc2

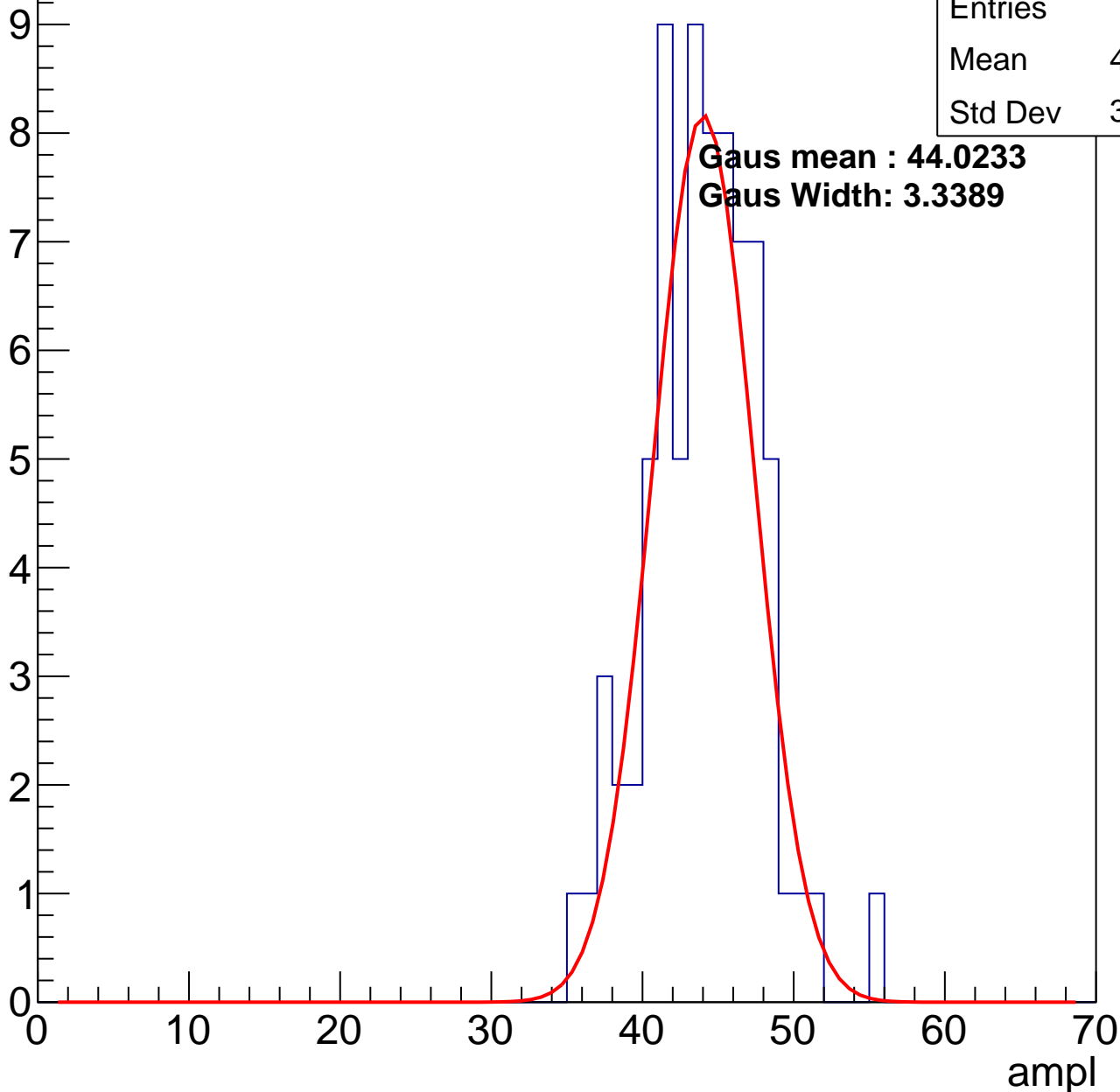
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	76
Mean	43.55
Std Dev	3.625

**Gaus mean : 44.0233**

**Gaus Width: 3.3389**

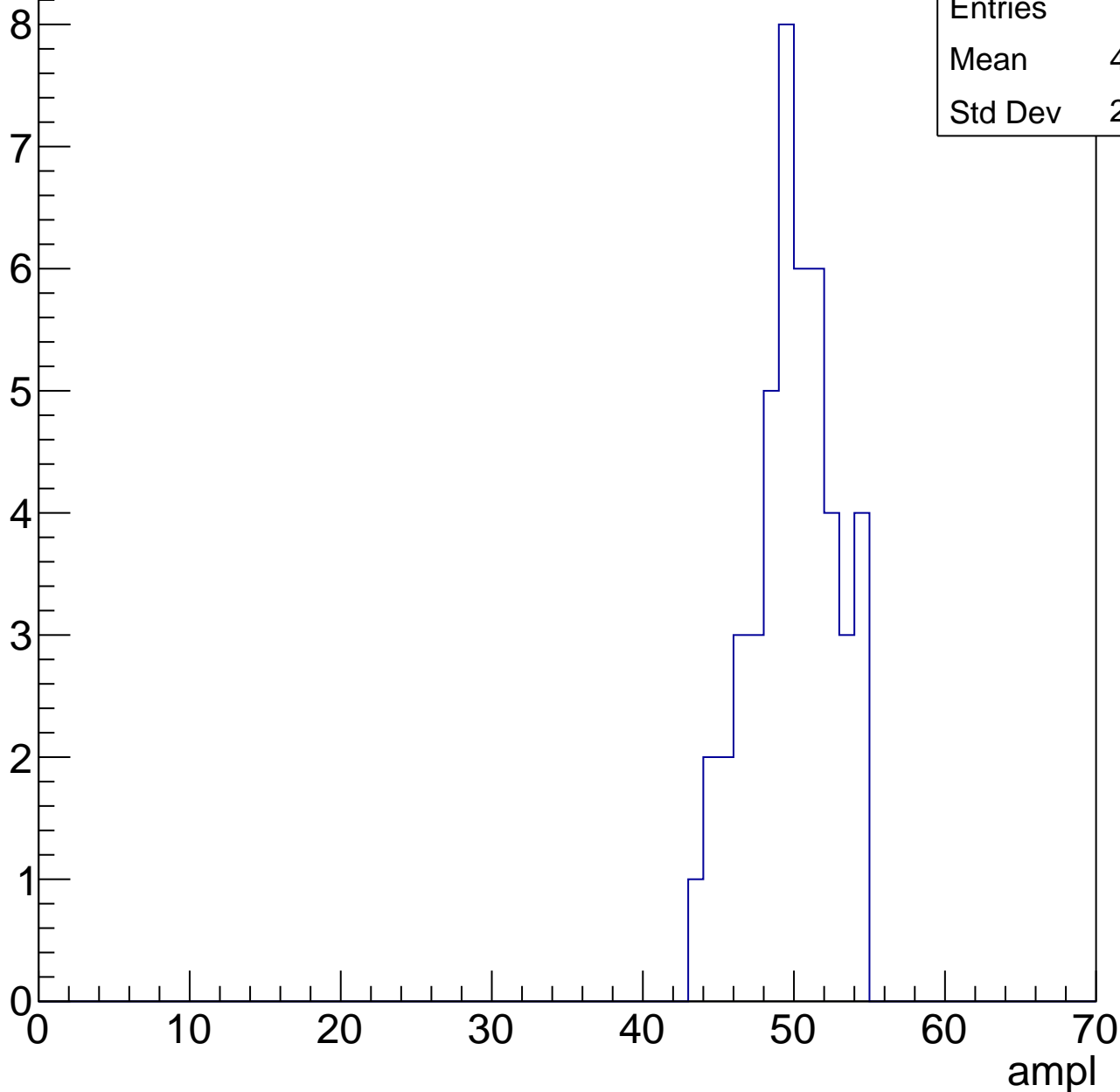


# B1L102S, U12-ch55, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	47
Mean	49.38
Std Dev	2.802

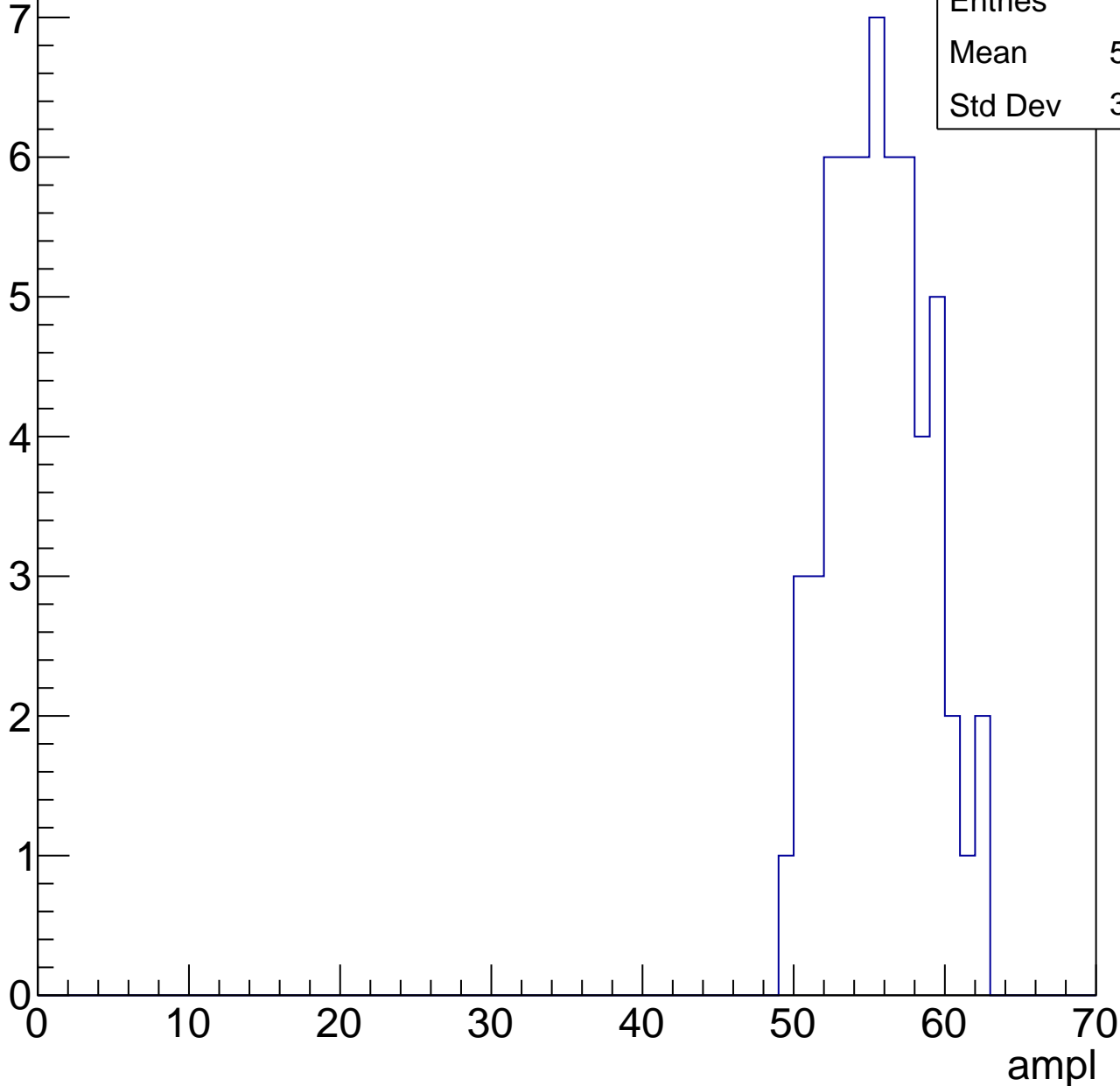


# B1L102S, U12-ch55, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	58
Mean	55.19
Std Dev	3.137



# B1L102S, U12-ch55, adc5

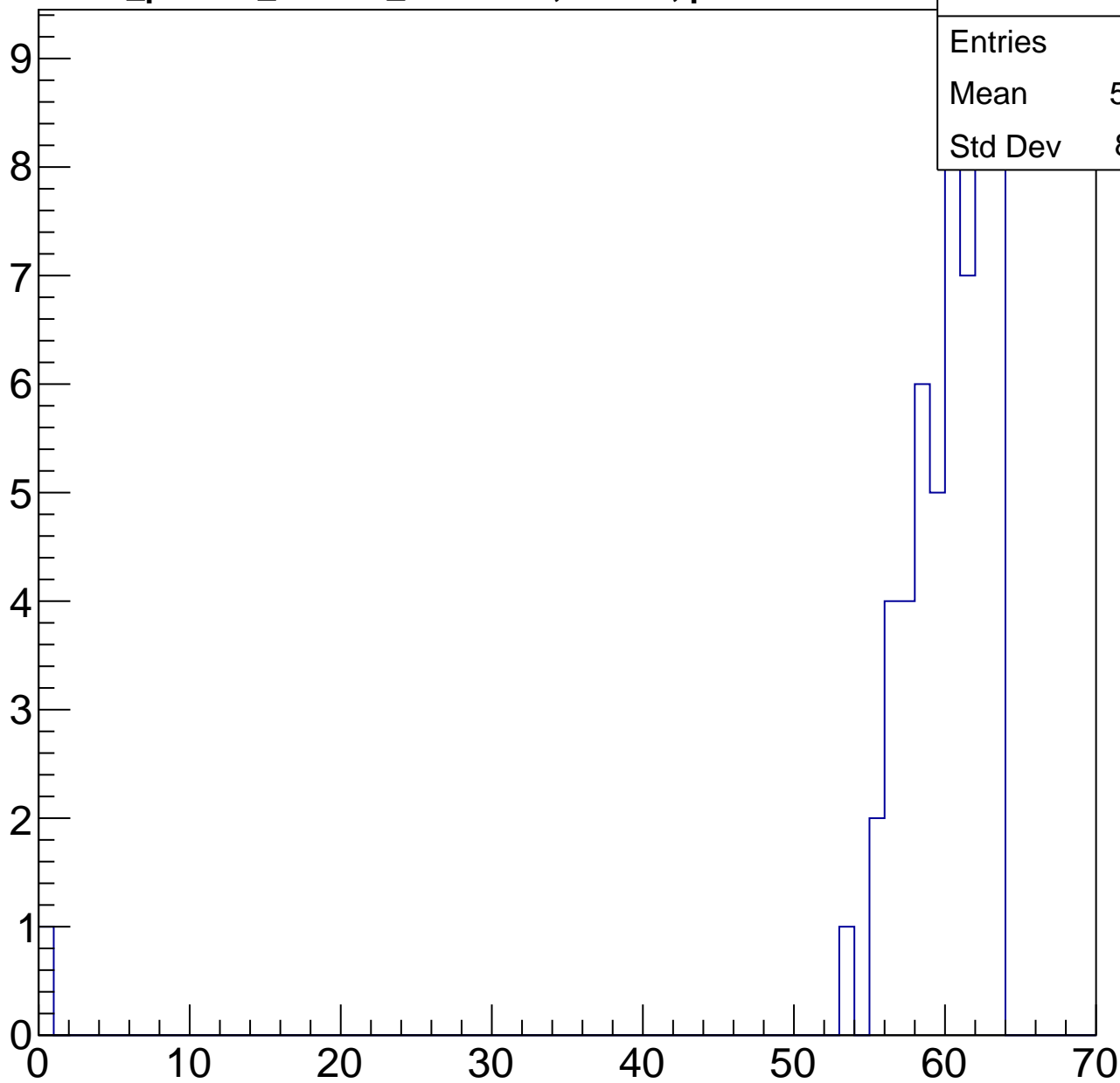
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	55
Mean	58.69
Std Dev	8.371

ampl



# B1L102S, U12-ch55, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	3
Mean	61.67
Std Dev	0.9428



# B1L102S, U12-ch55, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L102S, U12-ch56, adc0

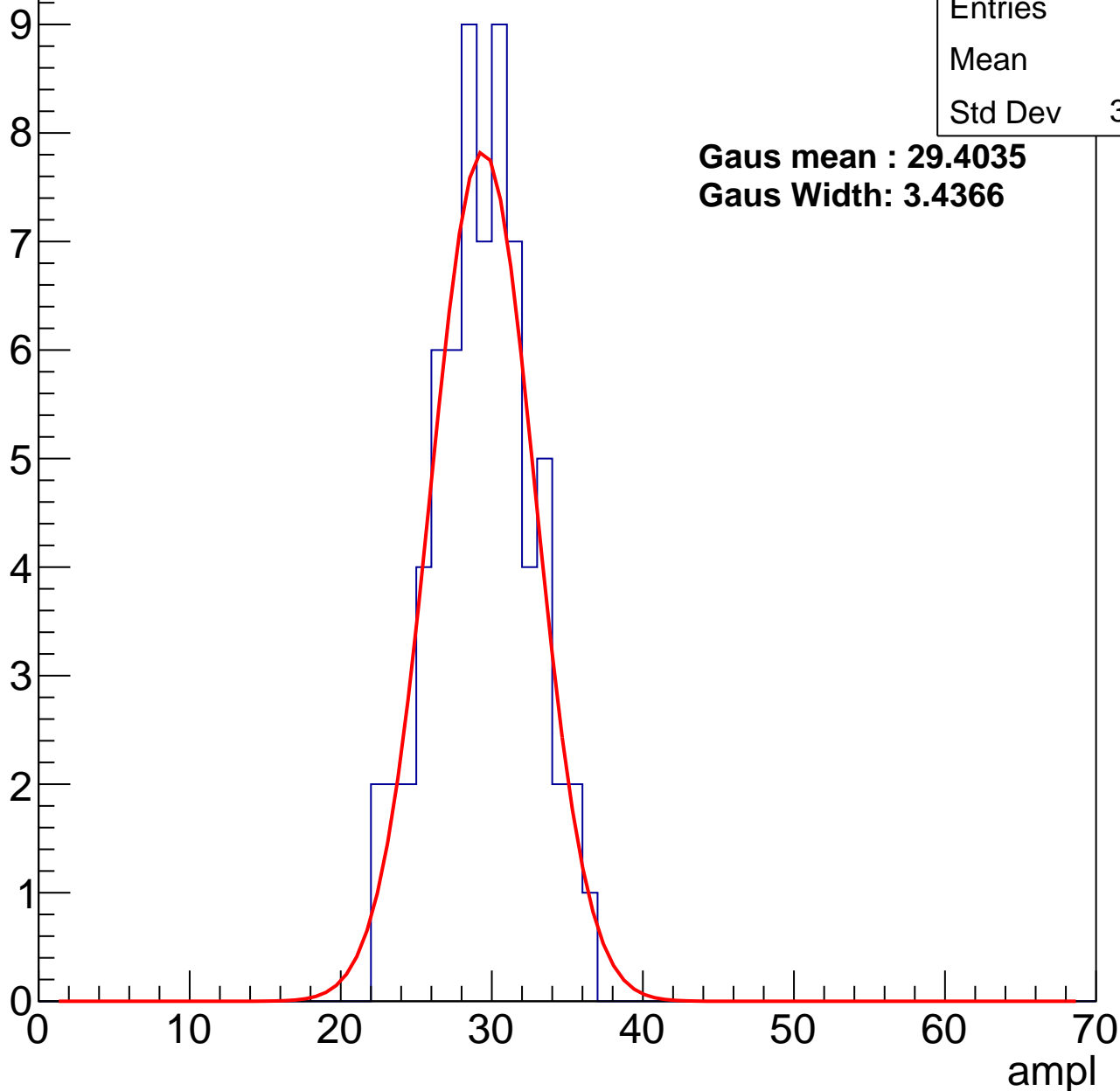
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	28.9
Std Dev	3.195

**Gaus mean : 29.4035**

**Gaus Width: 3.4366**



# B1L102S, U12-ch56, adc1

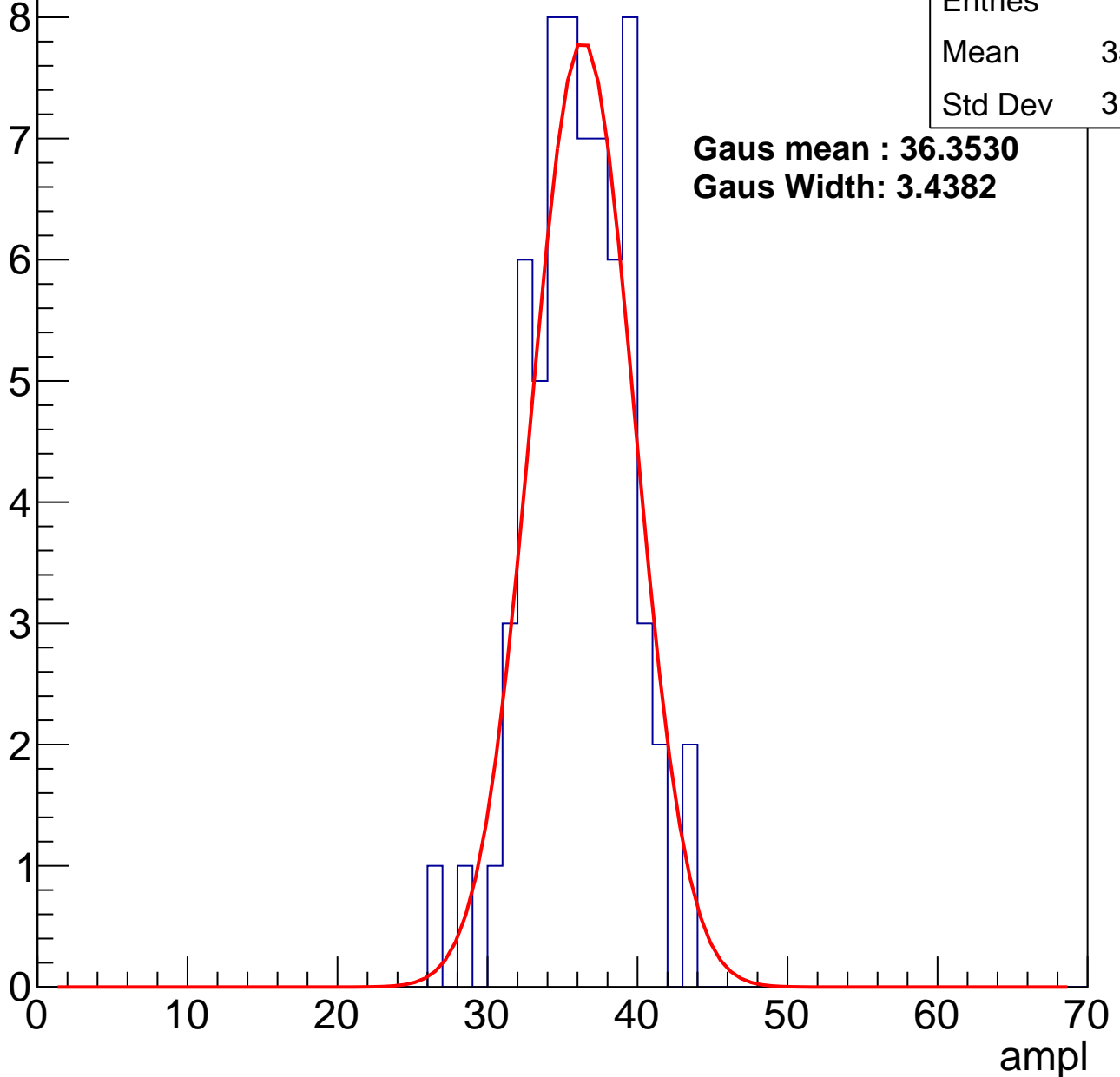
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	35.66
Std Dev	3.315

**Gaus mean : 36.3530**

**Gaus Width: 3.4382**



# B1L102S, U12-ch56, adc2

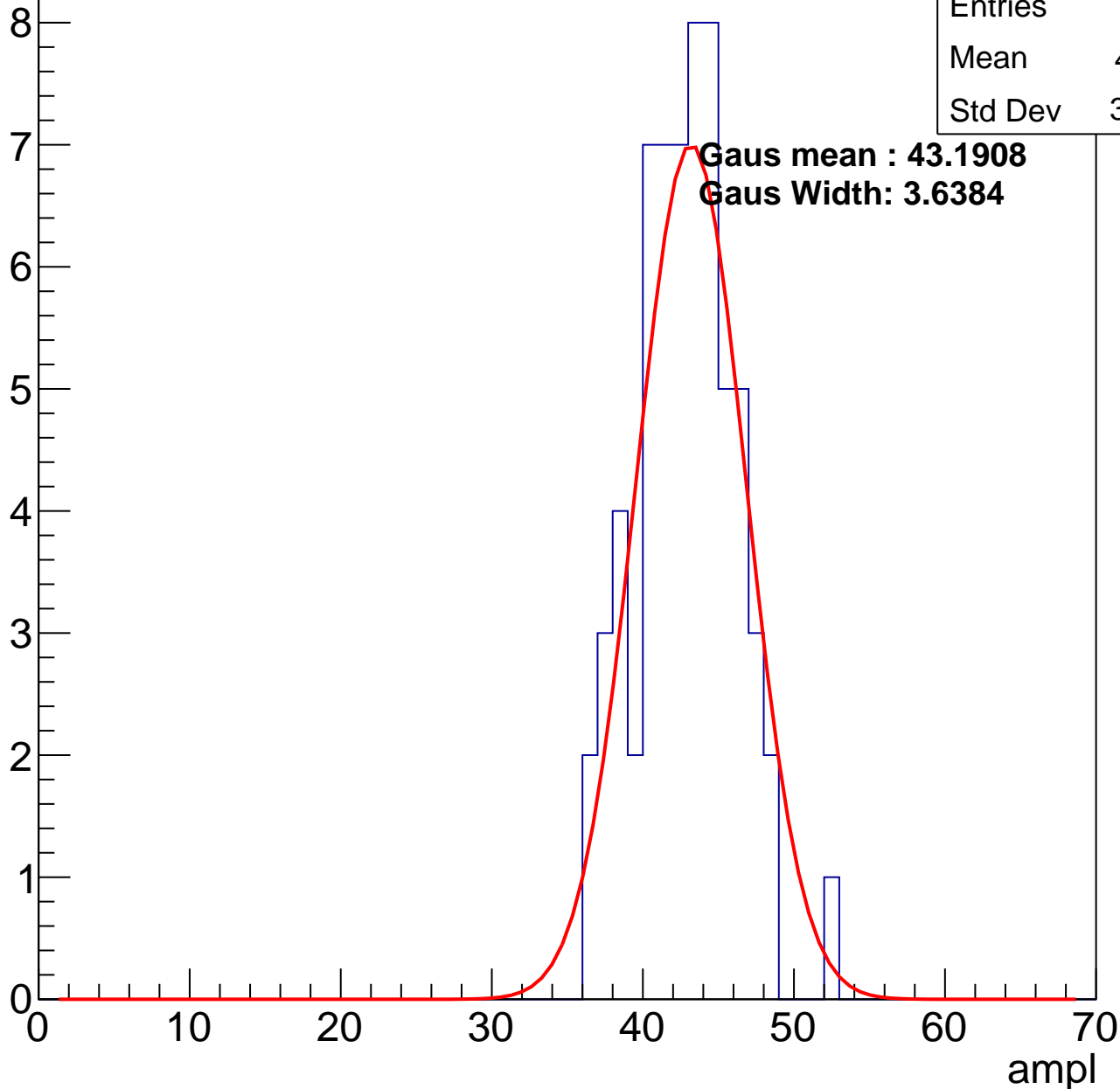
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	42.41
Std Dev	3.225

**Gaus mean : 43.1908**

**Gaus Width: 3.6384**

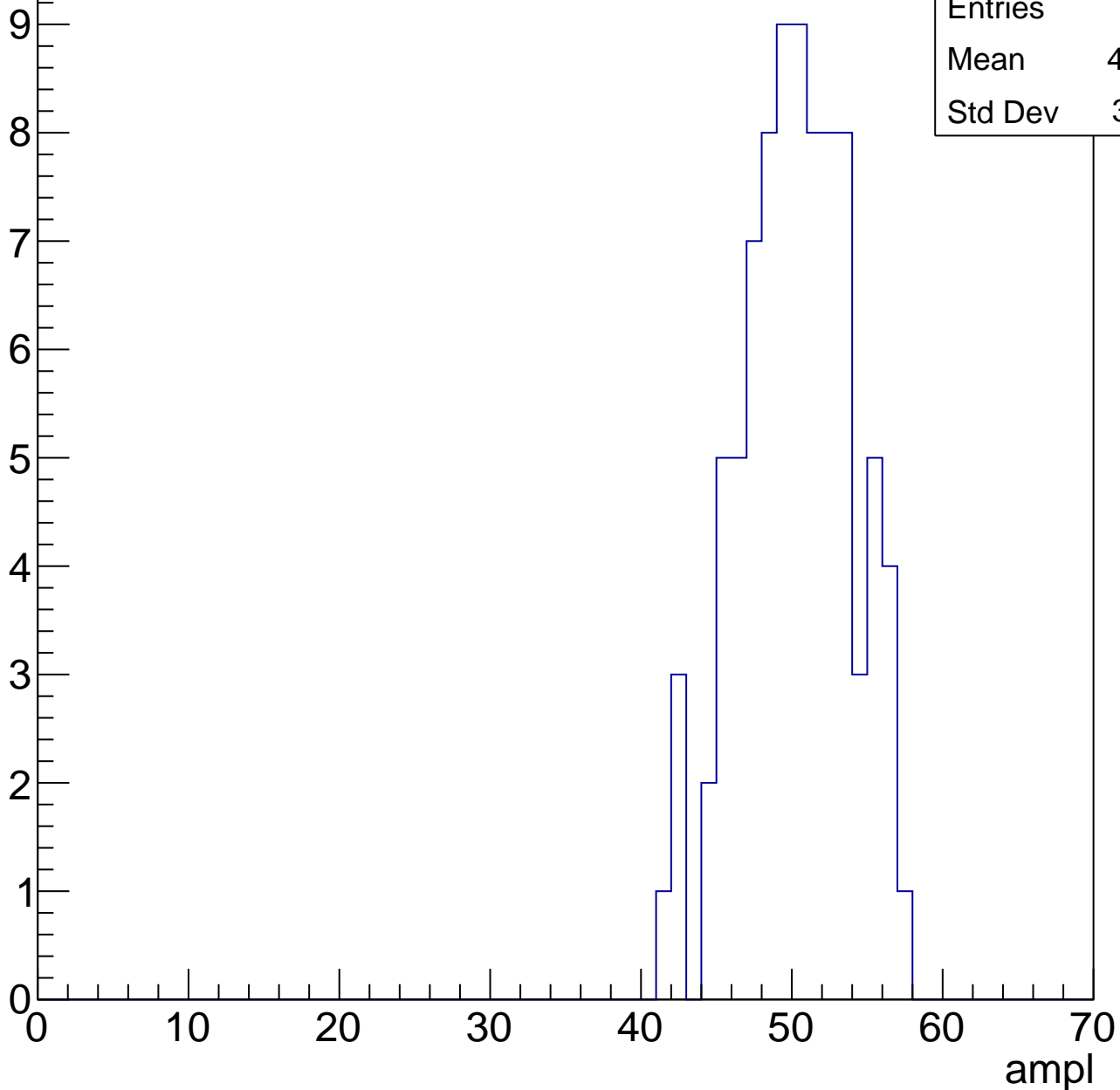


# B1L102S, U12-ch56, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

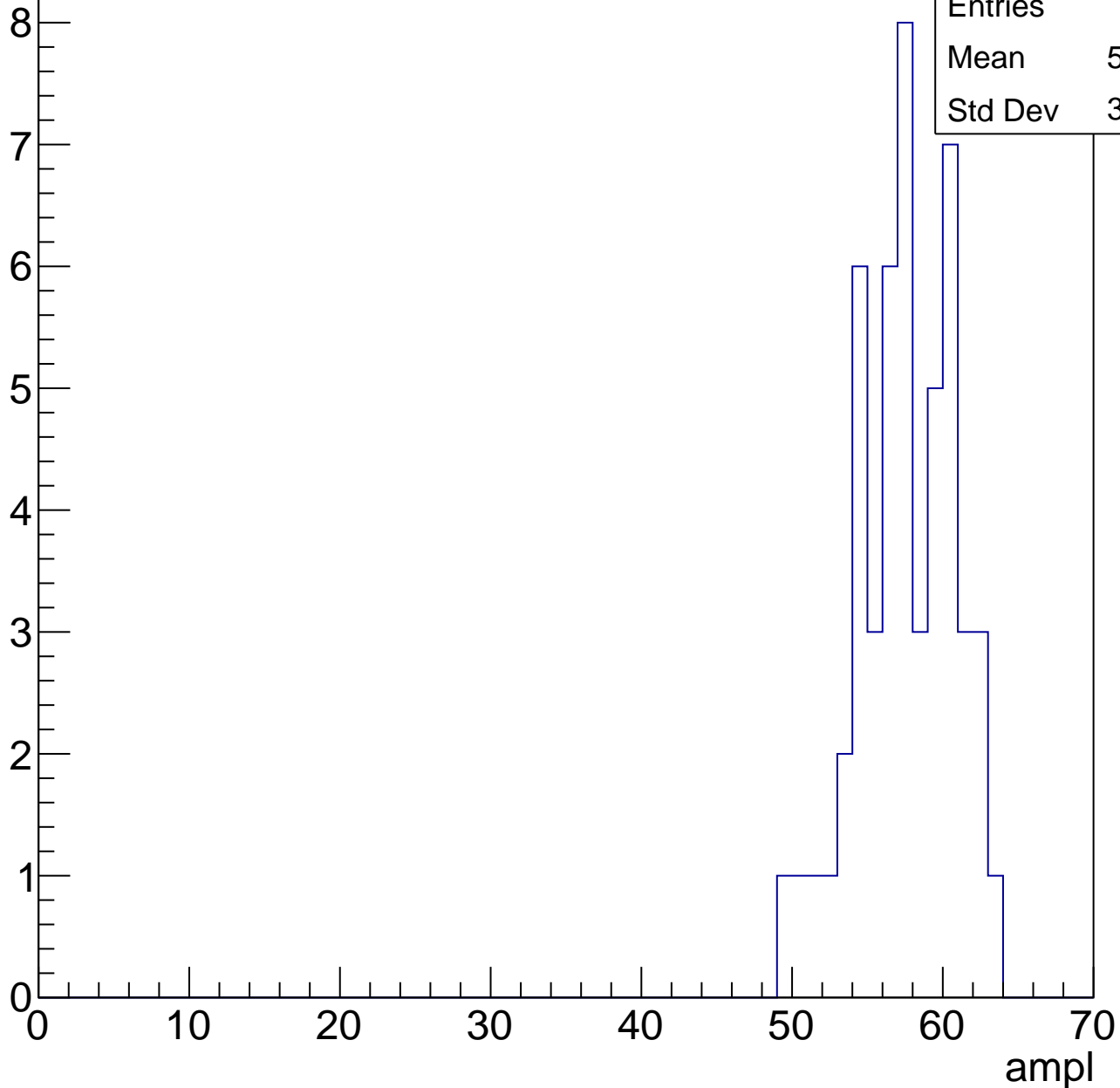
Entries	86
Mean	49.77
Std Dev	3.621



# B1L102S, U12-ch56, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



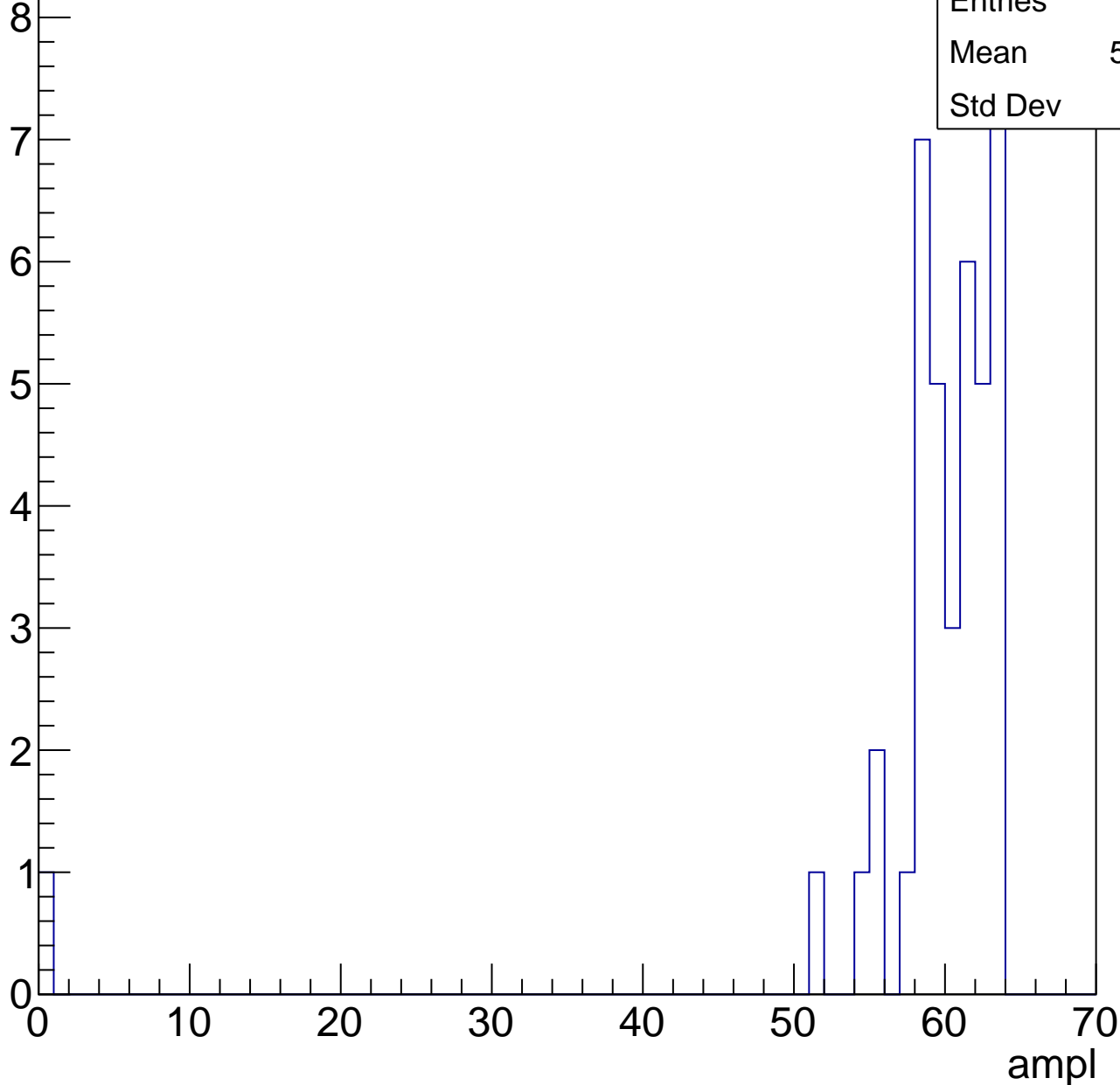
Entries	51
Mean	57.06
Std Dev	3.202

# B1L102S, U12-ch56, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	40
Mean	58.33
Std Dev	9.74



# B1L102S, U12-ch56, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U12-ch56, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

1  
0.8  
0.6  
0.4  
0.2  
0

Entries	1
Mean	21
Std Dev	0

ampl

# B1L102S, U12-ch57, adc0

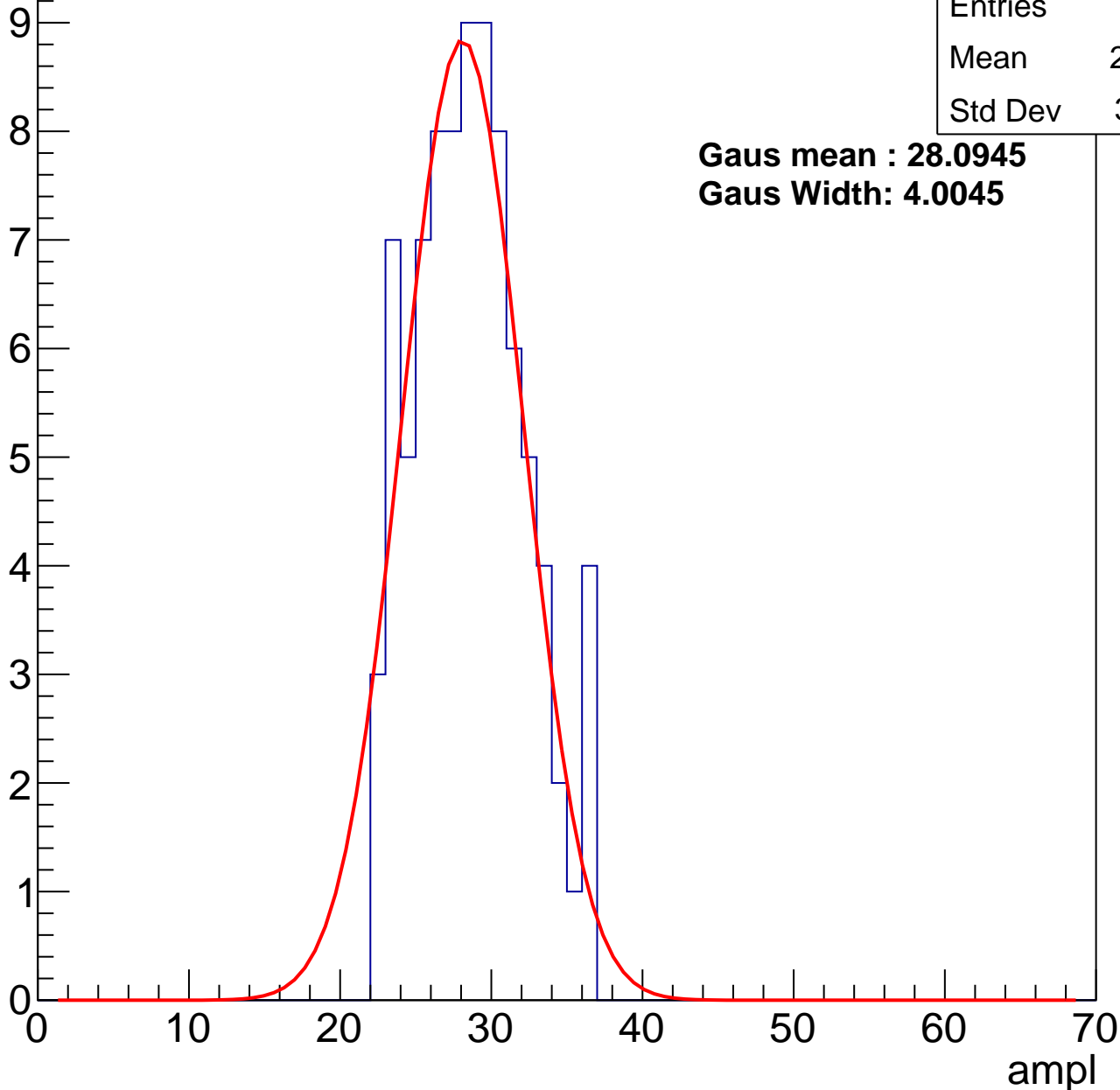
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	86
Mean	28.19
Std Dev	3.601

**Gaus mean : 28.0945**

**Gaus Width: 4.0045**



# B1L102S, U12-ch57, adc1

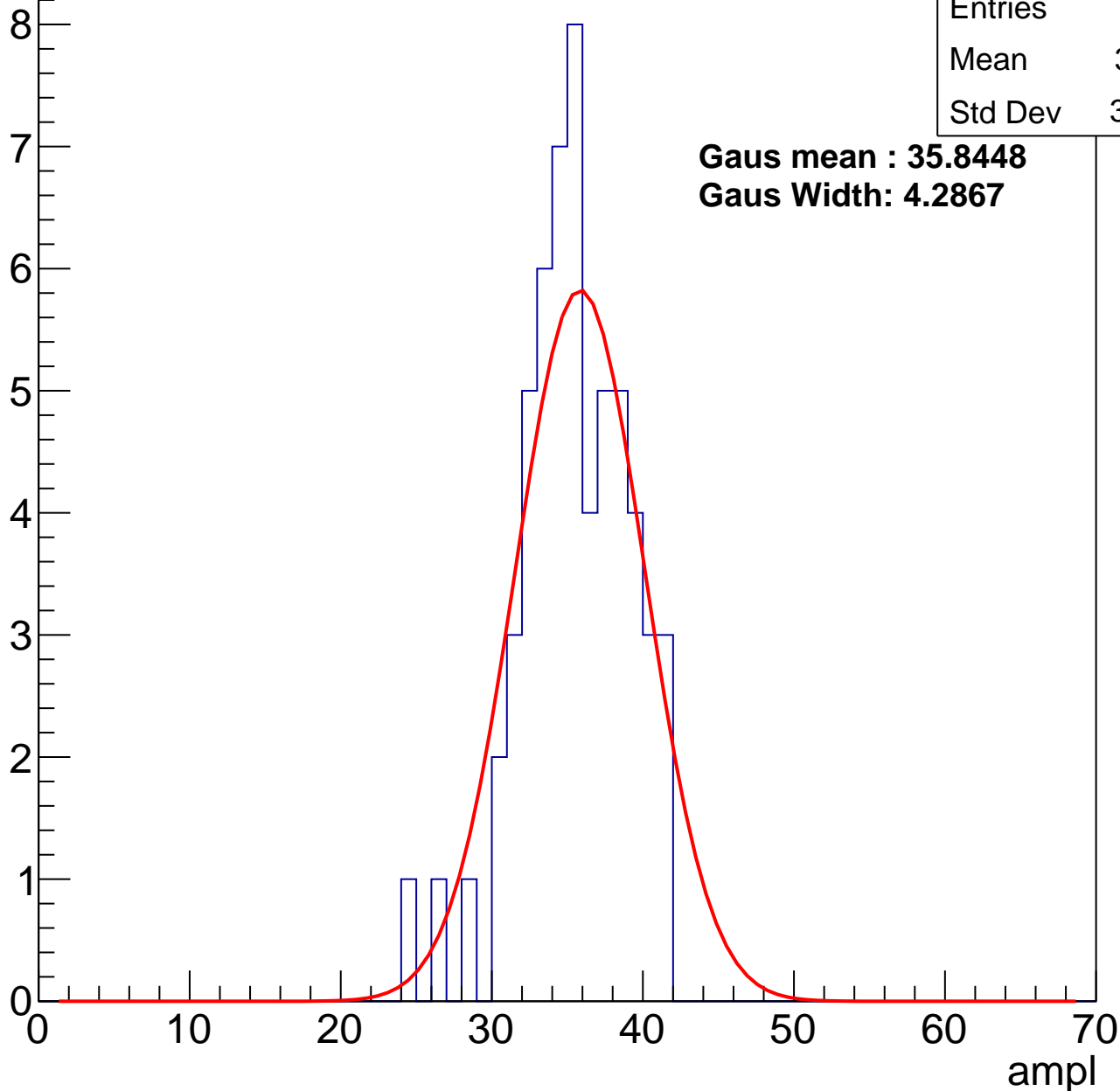
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	58
Mean	34.91
Std Dev	3.573

**Gaus mean : 35.8448**

**Gaus Width: 4.2867**



# B1L102S, U12-ch57, adc2

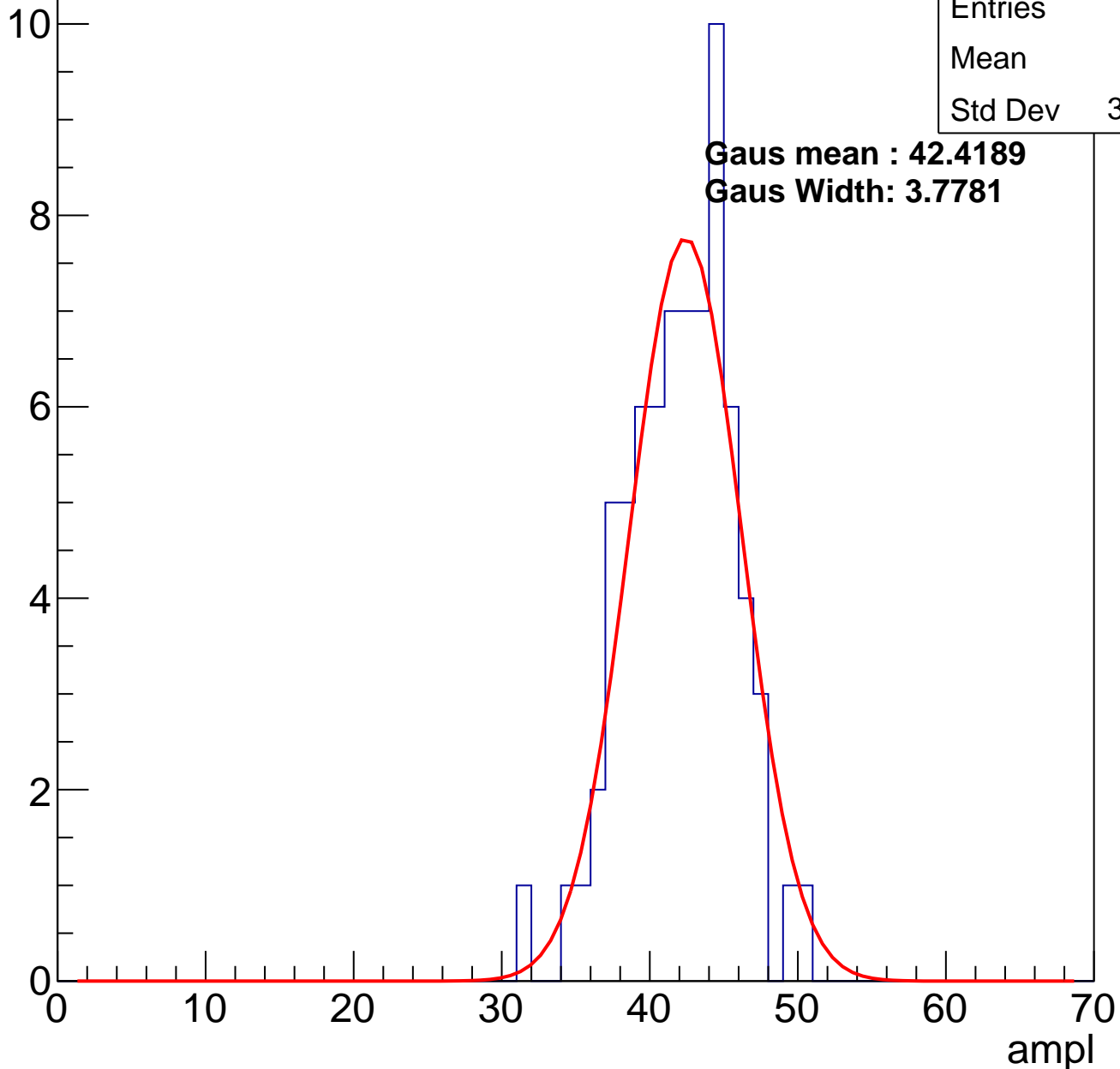
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	73
Mean	41.6
Std Dev	3.584

**Gaus mean : 42.4189**

**Gaus Width: 3.7781**

Entry

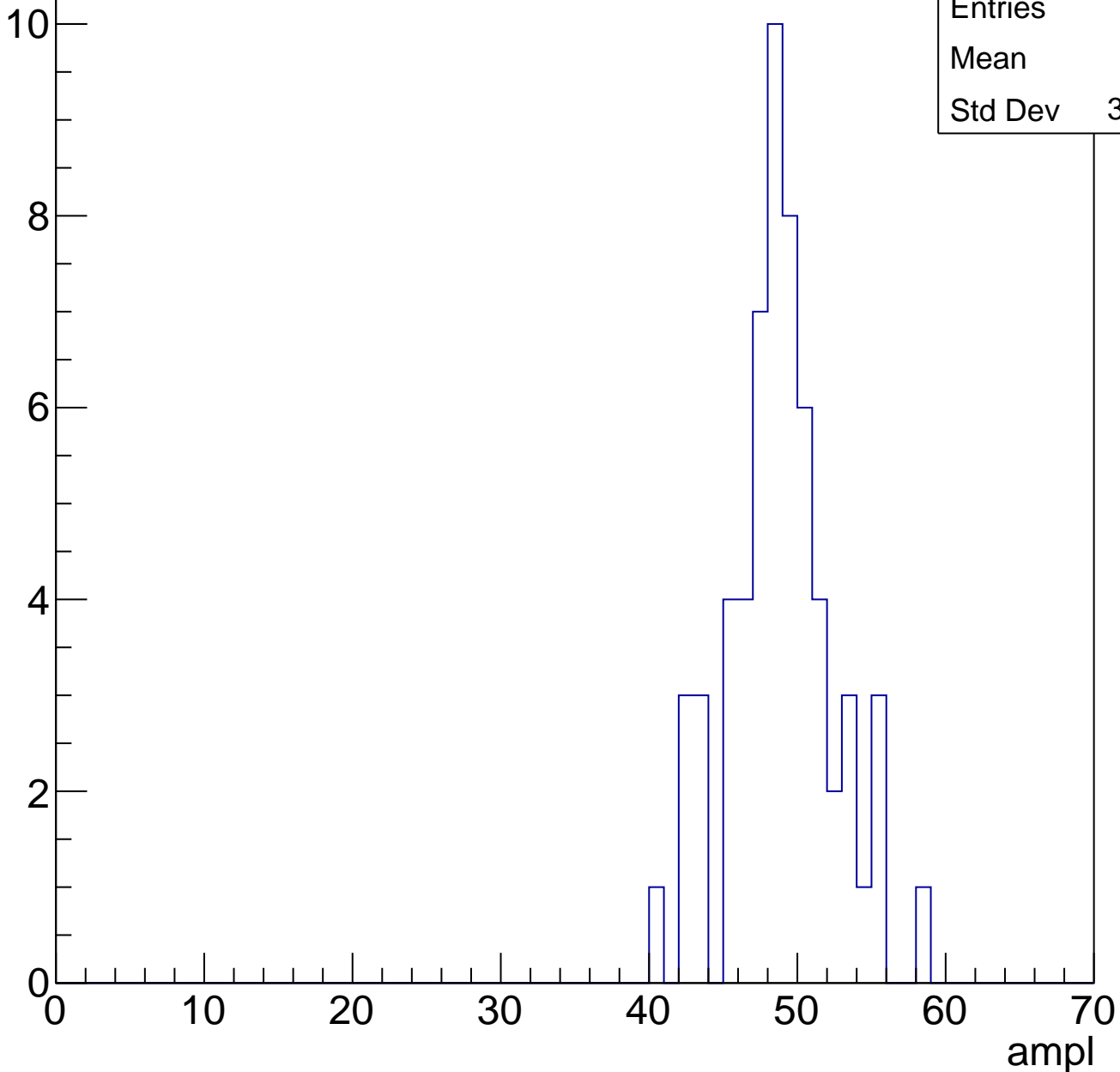


# B1L102S, U12-ch57, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	60
Mean	48.4
Std Dev	3.546

Entry

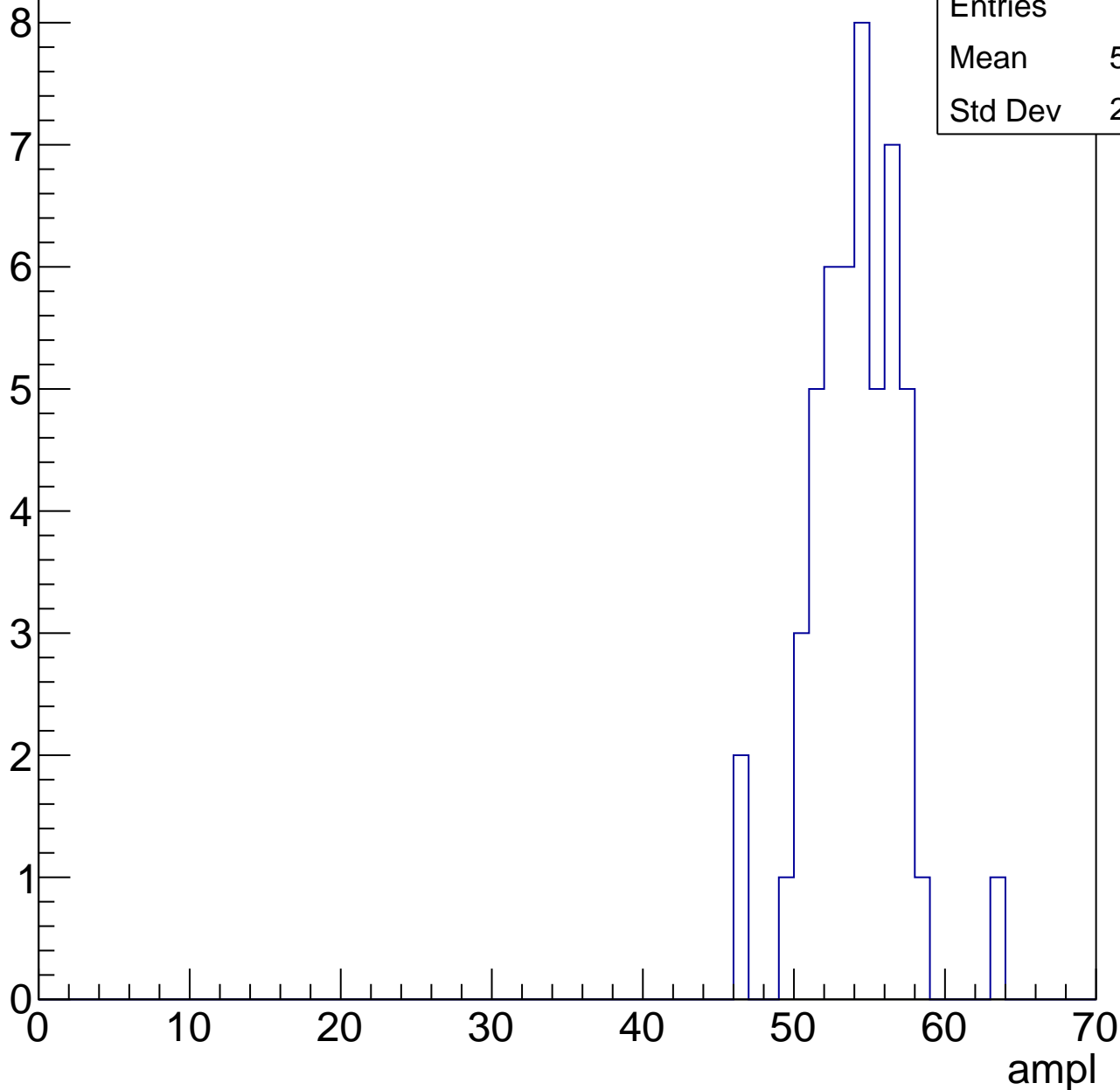


# B1L102S, U12-ch57, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	50
Mean	53.62
Std Dev	2.979

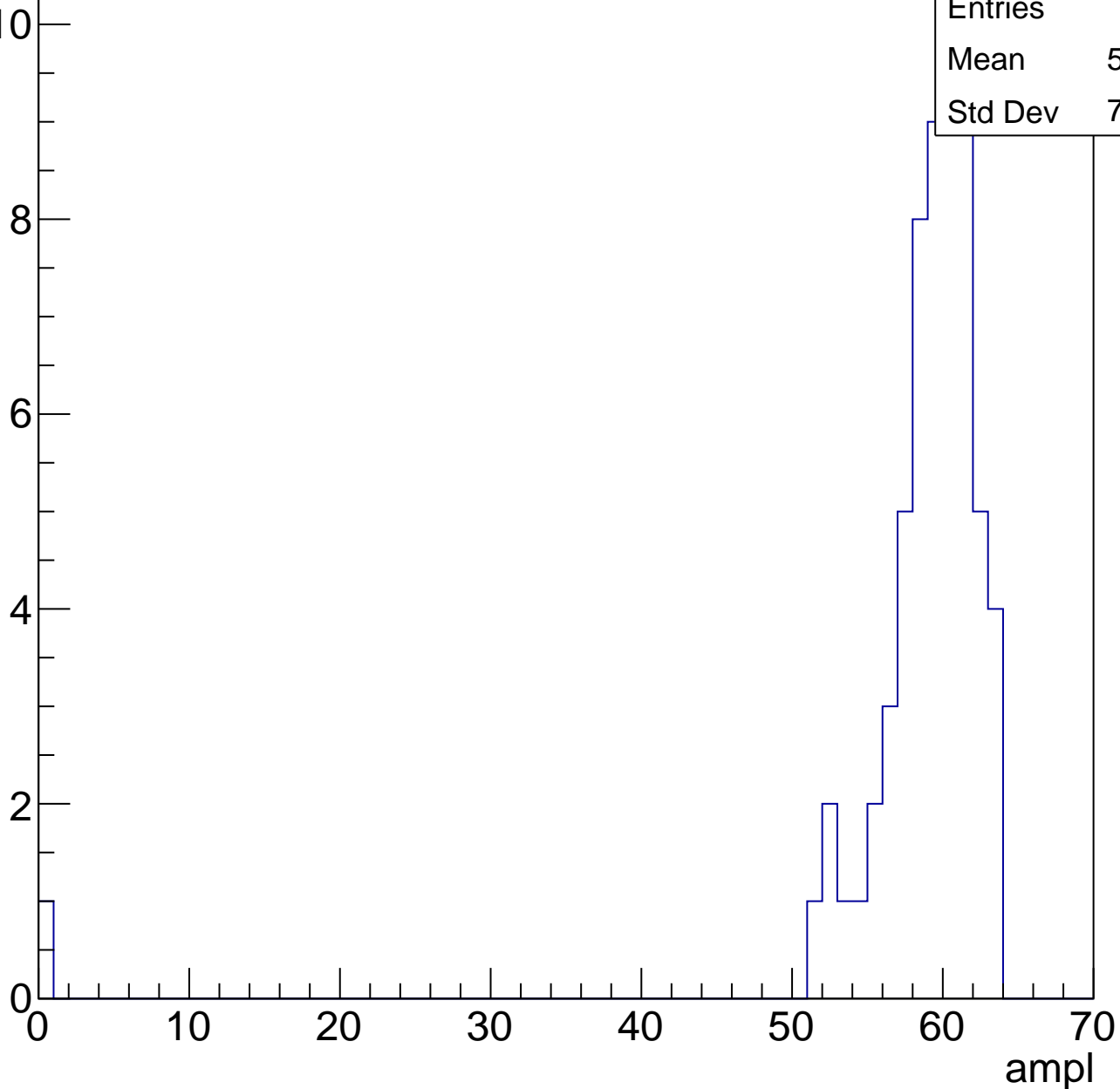


# B1L102S, U12-ch57, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	57.89
Std Dev	7.965

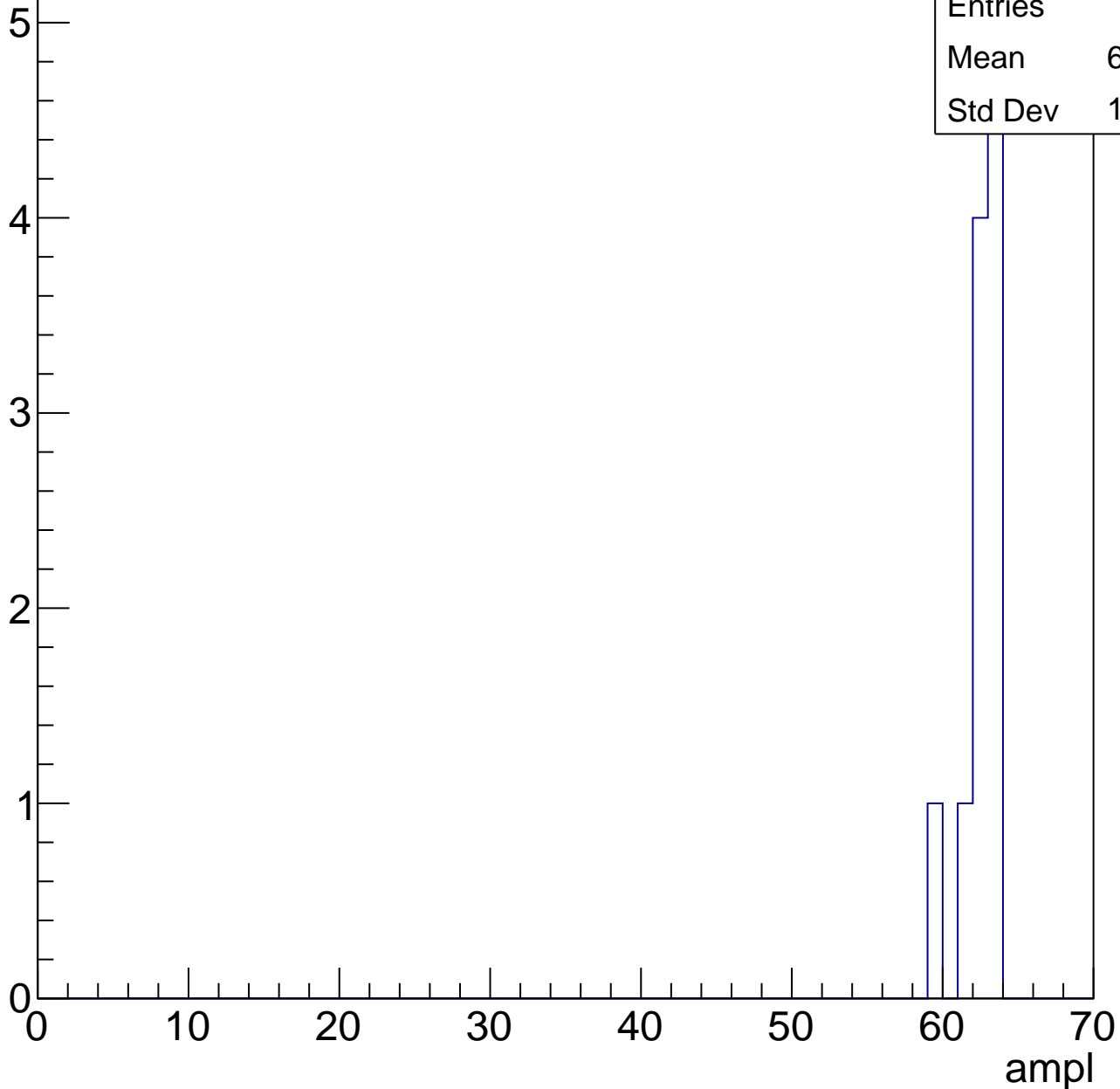


# B1L102S, U12-ch57, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	11
Mean	62.09
Std Dev	1.164





# B1L102S, U12-ch57, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U12-ch58, adc0

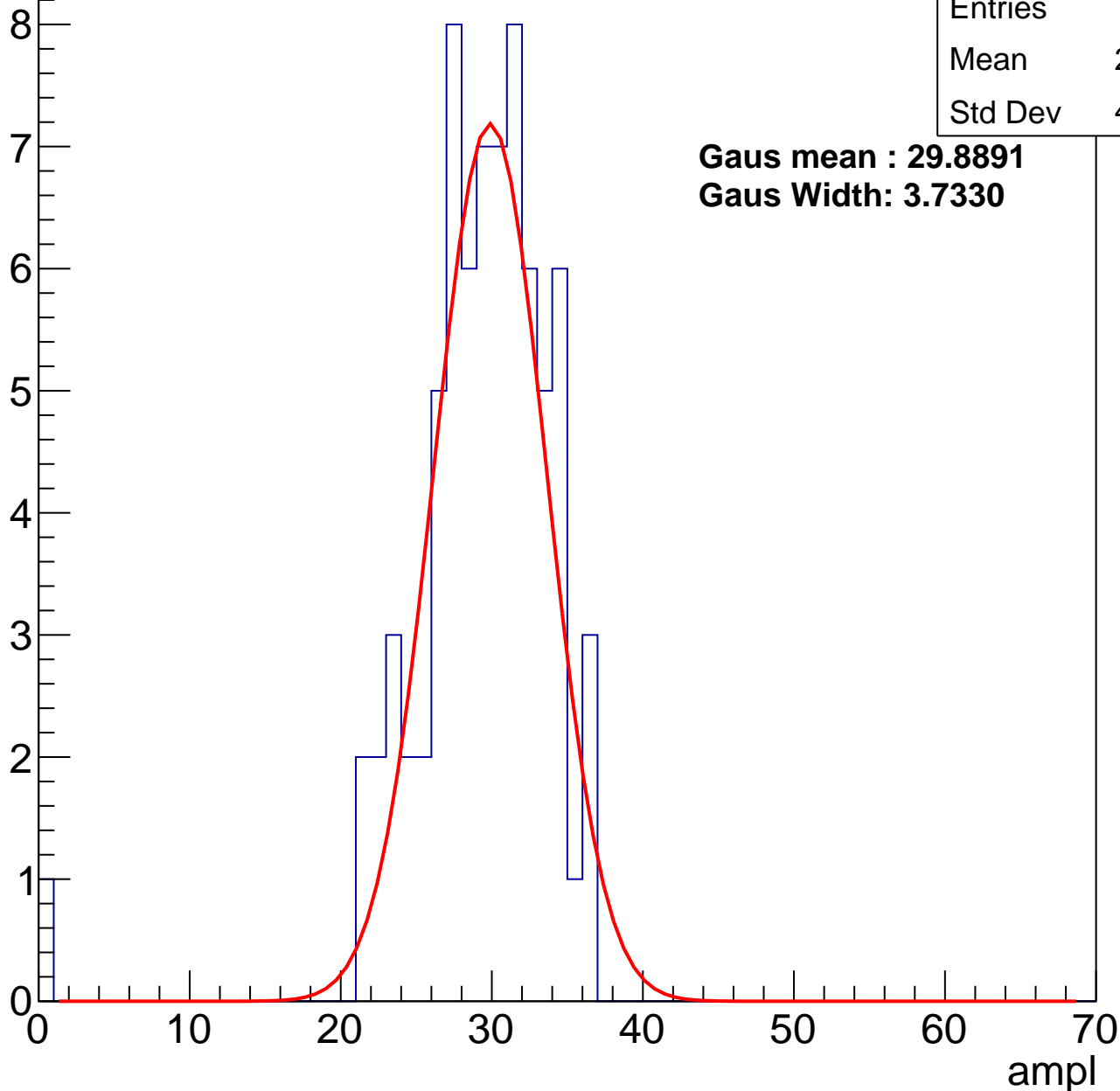
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	74
Mean	28.81
Std Dev	4.991

**Gaus mean : 29.8891**

**Gaus Width: 3.7330**



# B1L102S, U12-ch58, adc1

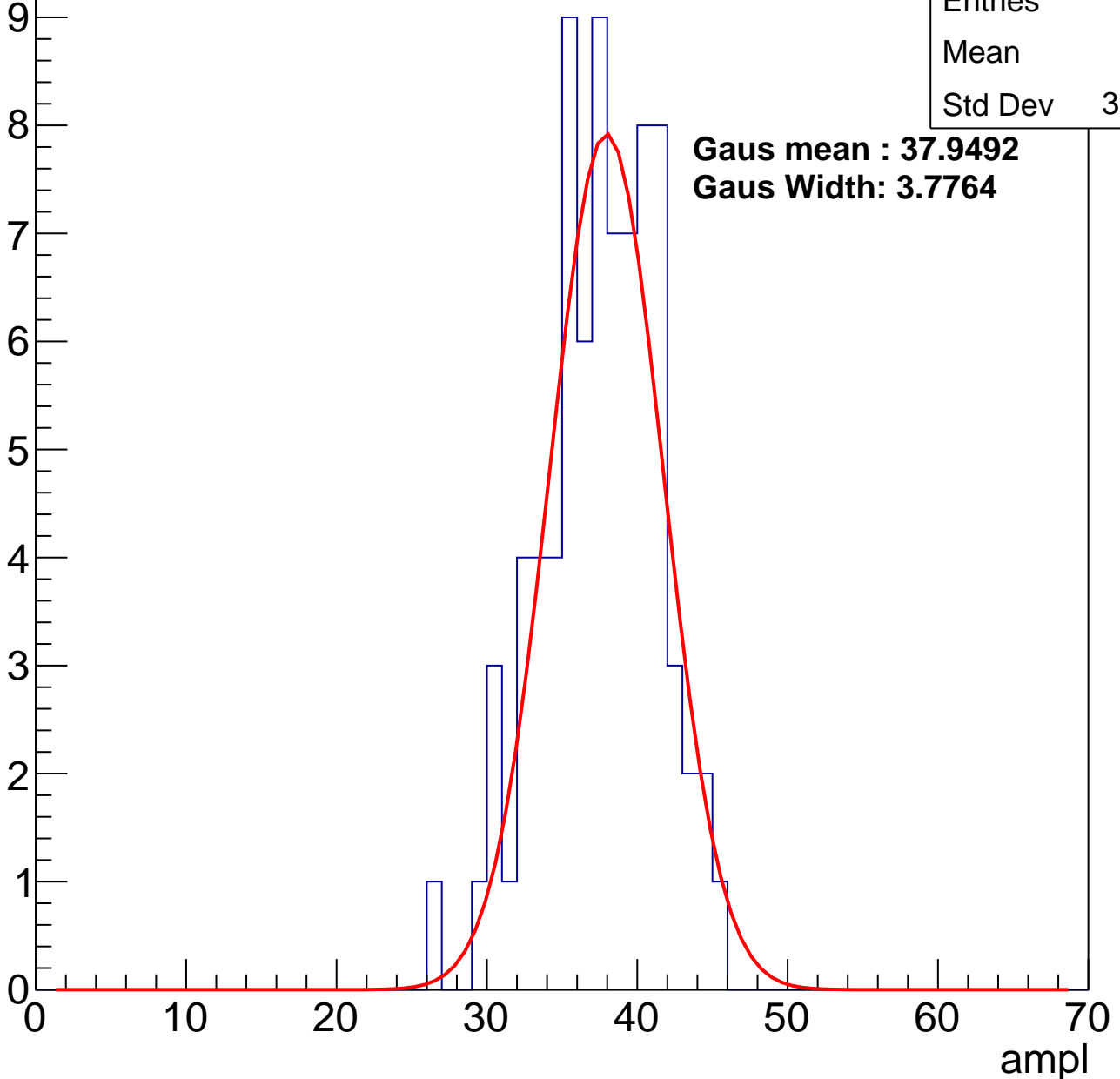
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	80
Mean	37.1
Std Dev	3.797

**Gaus mean : 37.9492**

**Gaus Width: 3.7764**



# B1L102S, U12-ch58, adc2

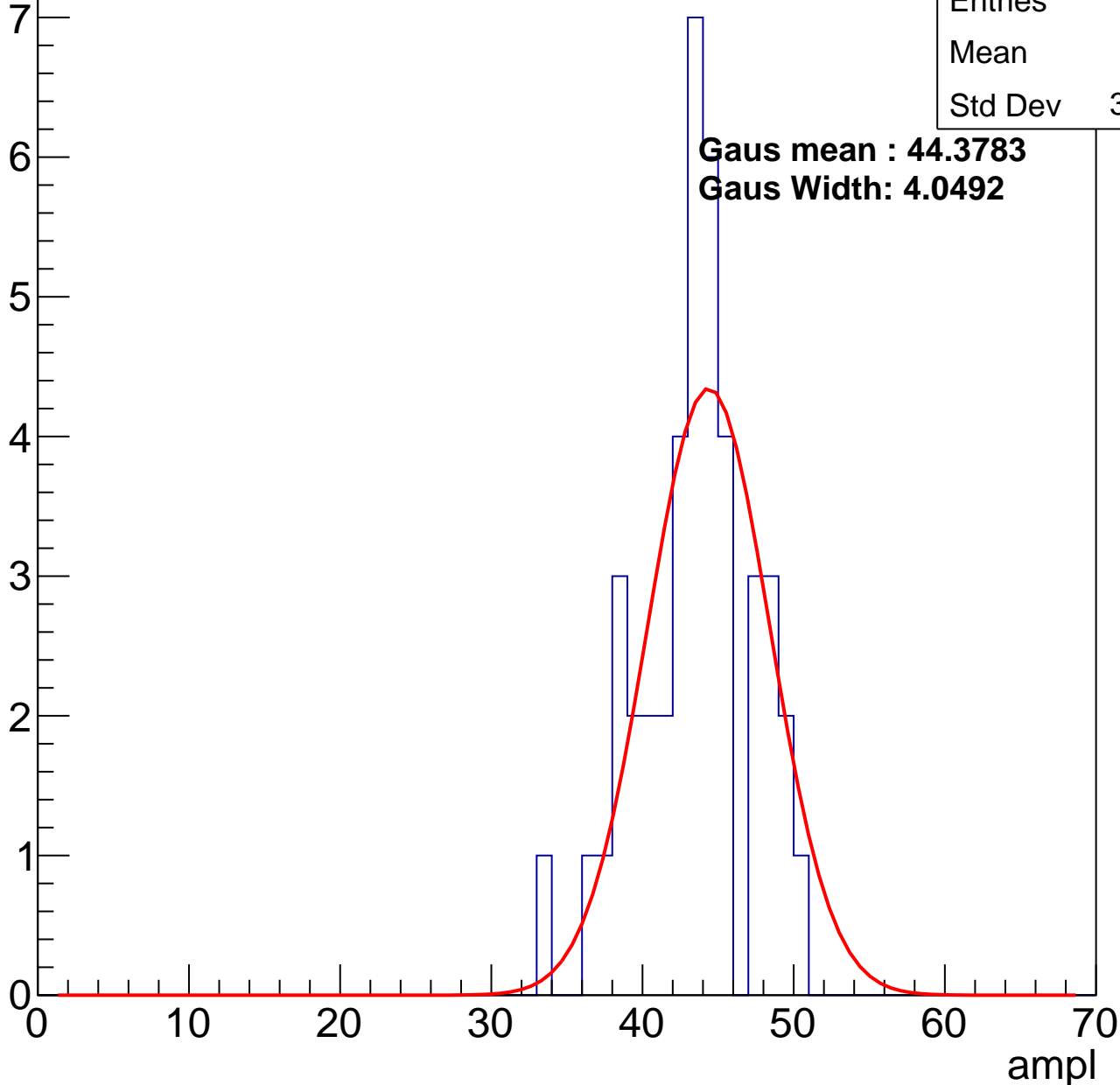
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	42
Mean	43
Std Dev	3.742

**Gaus mean : 44.3783**

**Gaus Width: 4.0492**

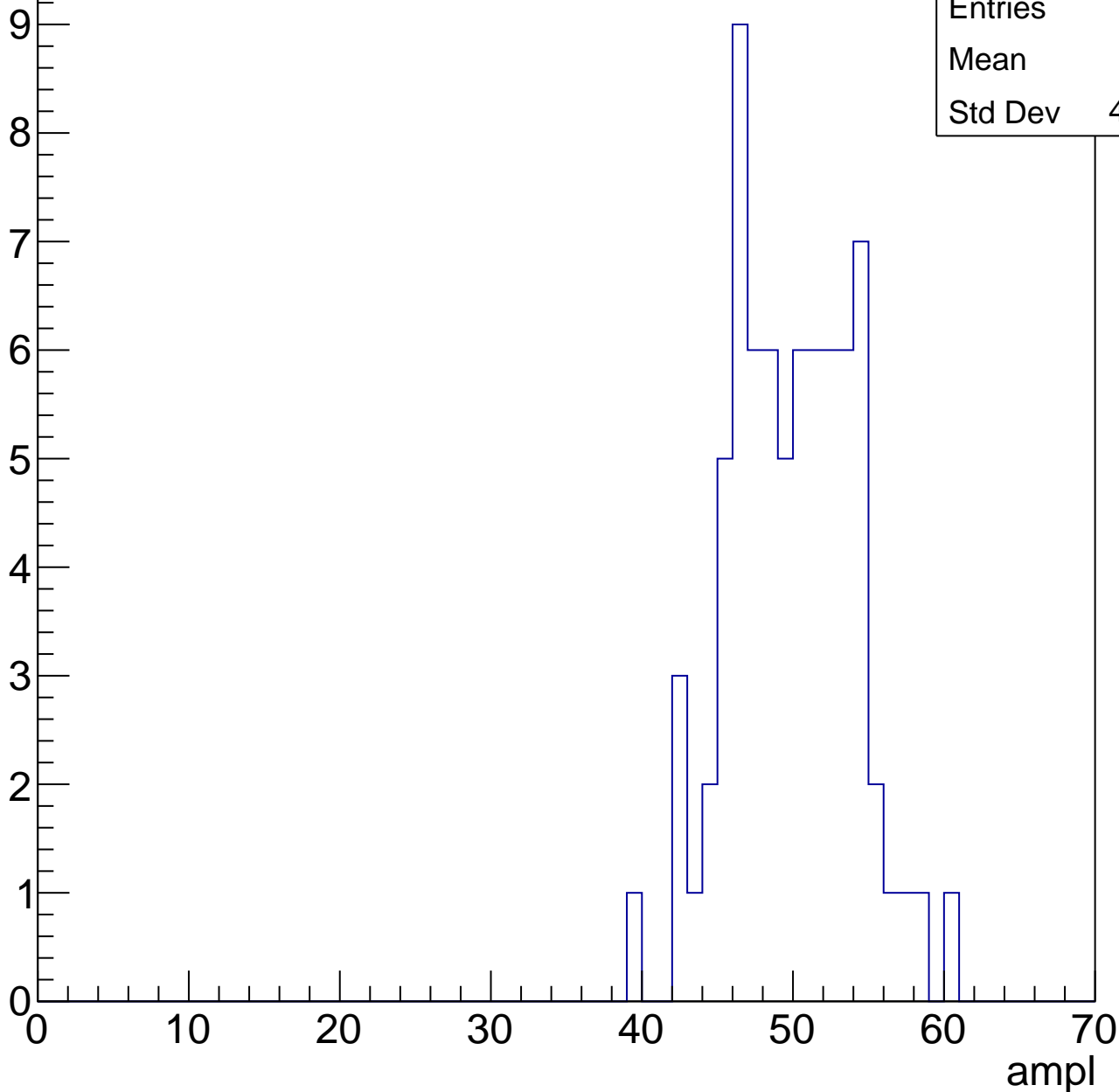


# B1L102S, U12-ch58, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	75
Mean	49.4
Std Dev	4.089

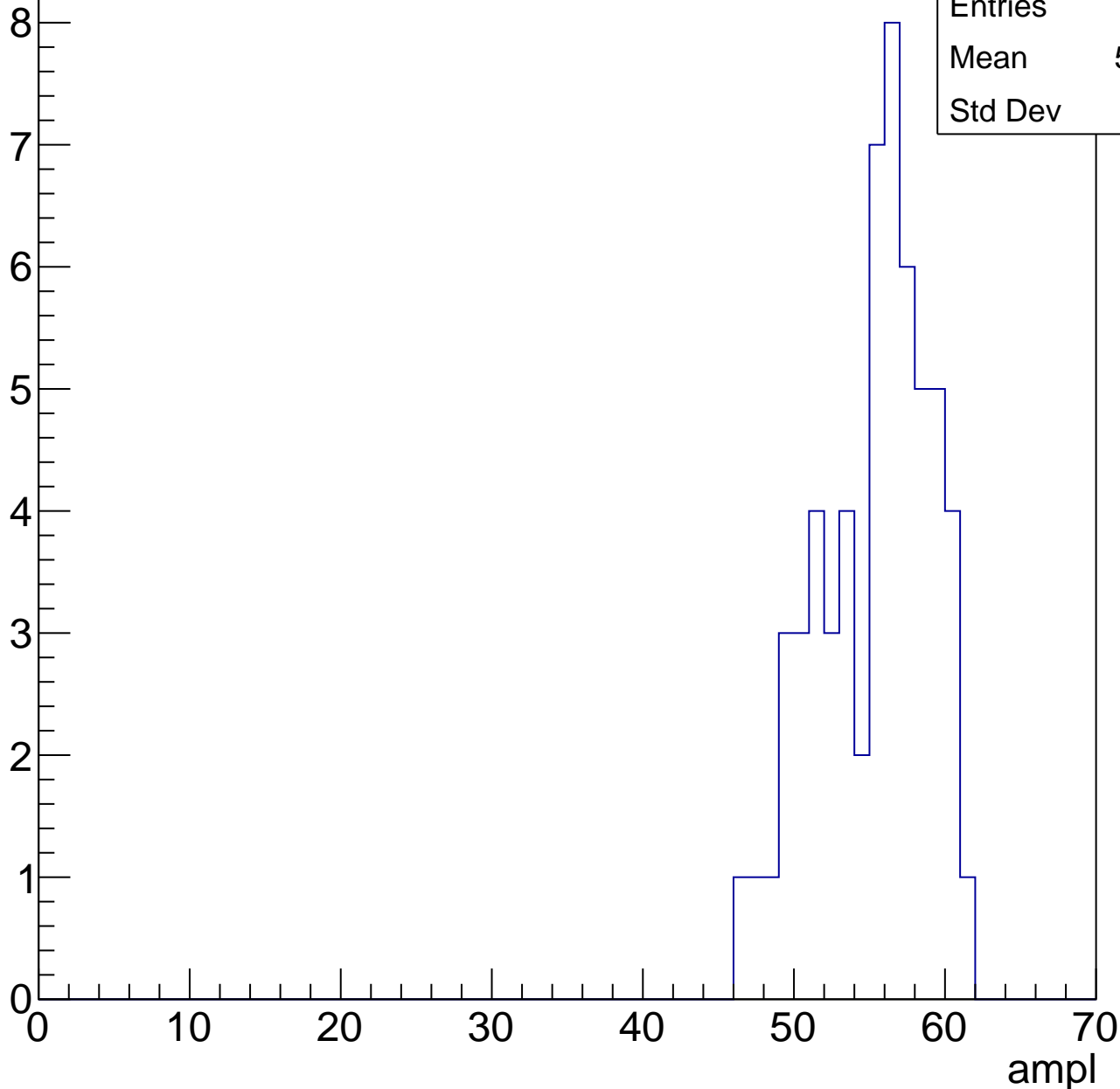


# B1L102S, U12-ch58, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	58
Mean	54.81
Std Dev	3.66

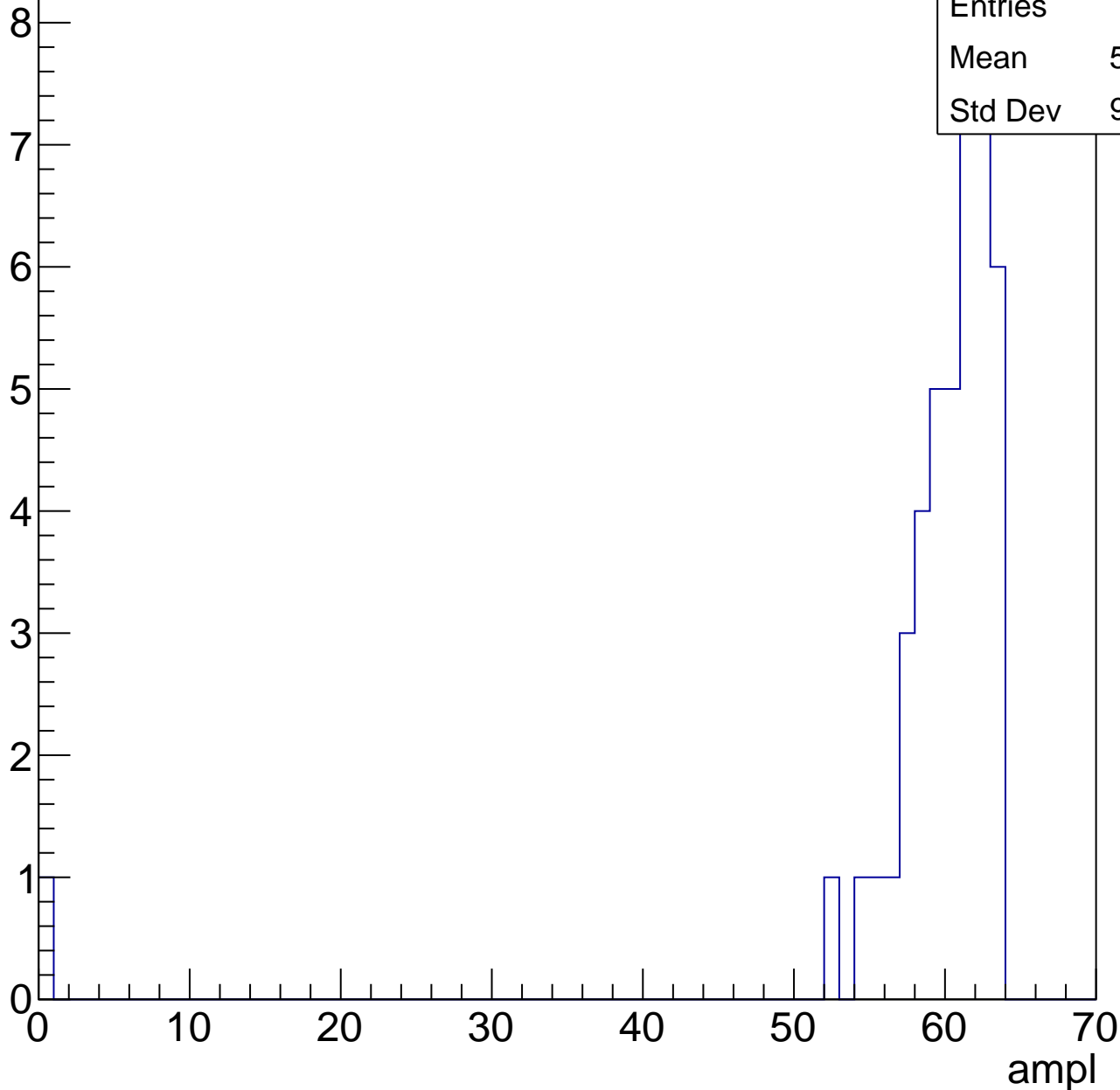


# B1L102S, U12-ch58, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	44
Mean	58.57
Std Dev	9.284



# B1L102S, U12-ch58, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

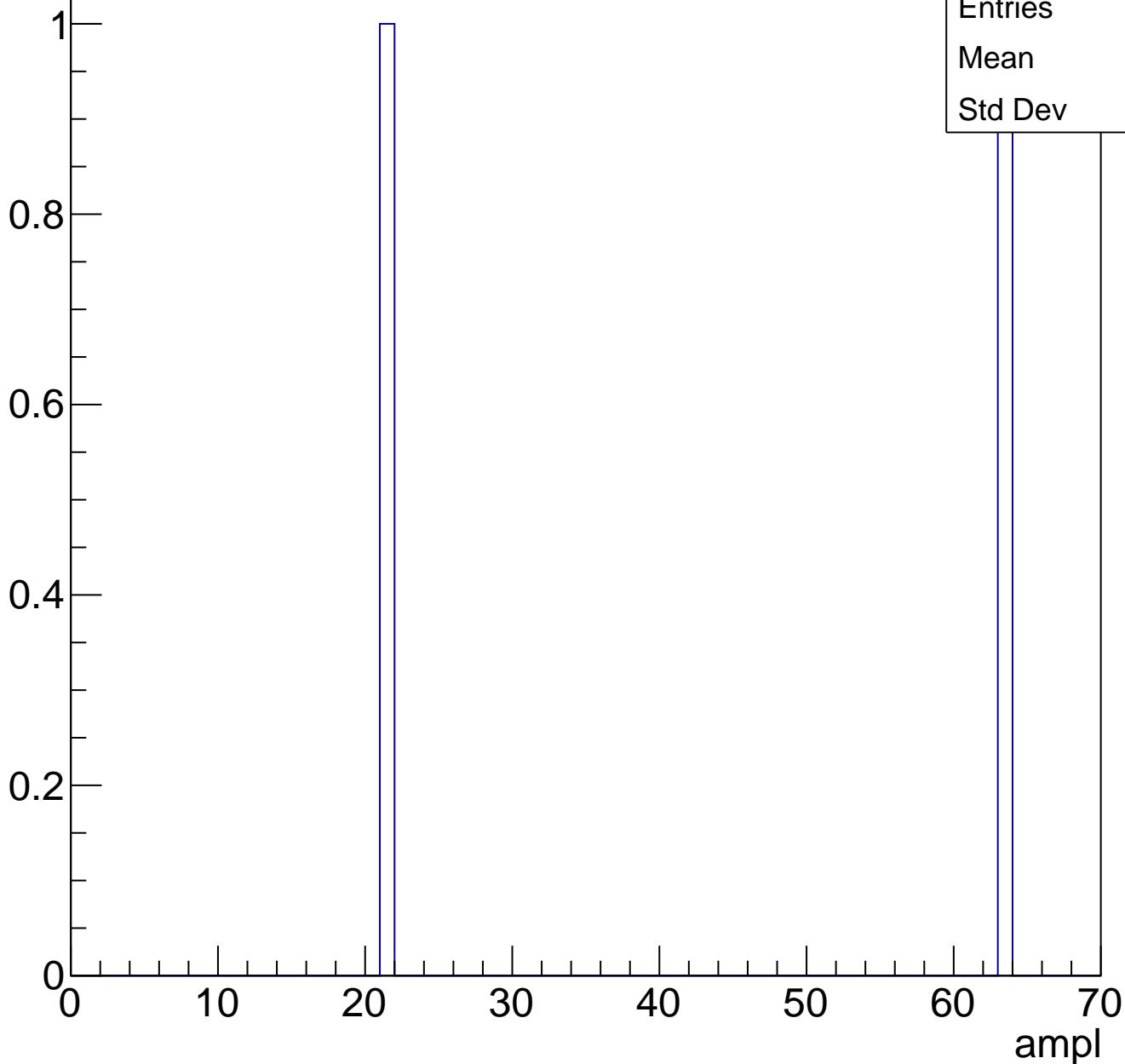




# B1L102S, U12-ch58, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U12-ch59, adc0

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	63
Mean	29.19
Std Dev	3.182

**Gaus mean : 30.5129**

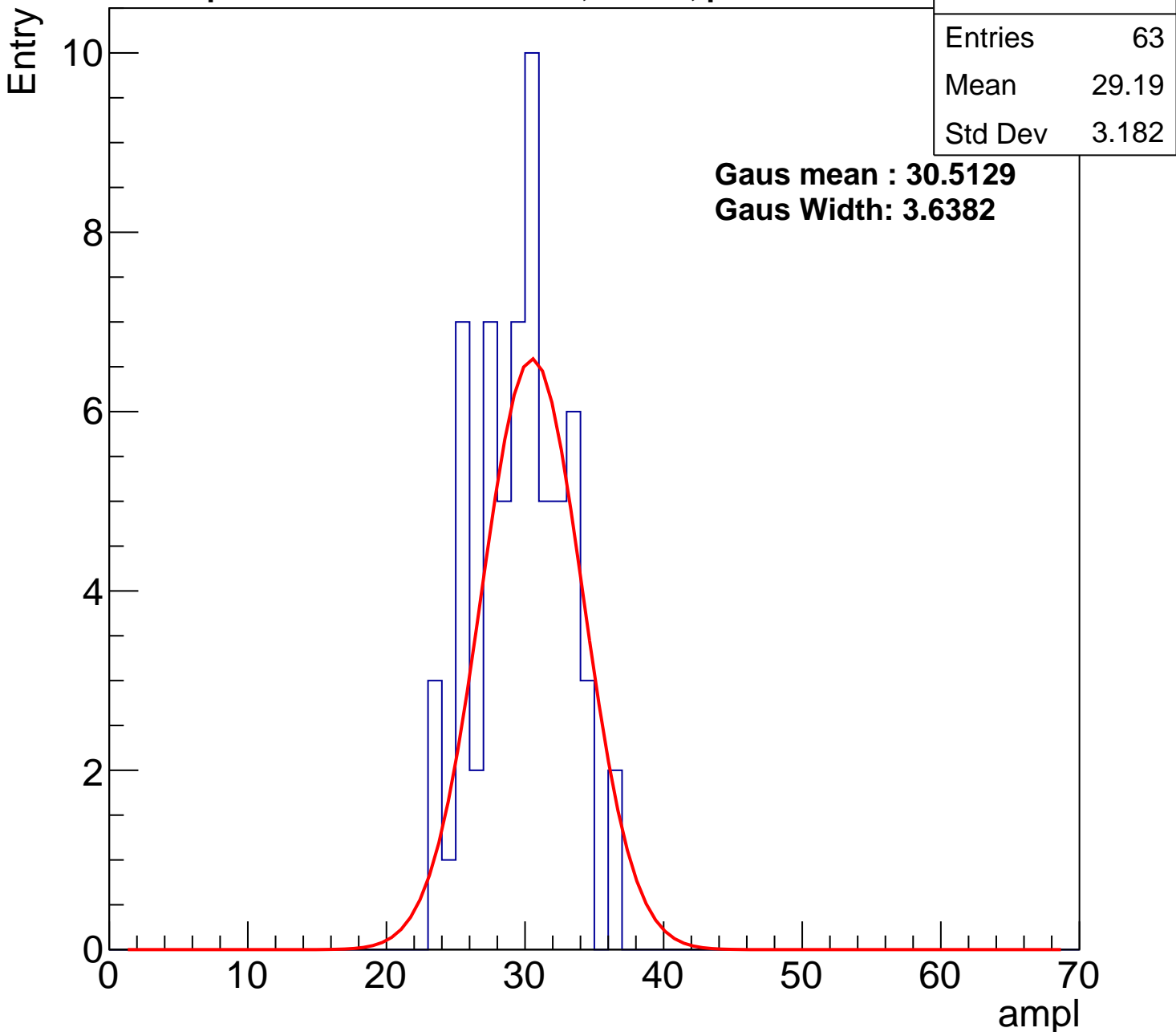
**Gaus Width: 3.6382**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L102S, U12-ch59, adc1

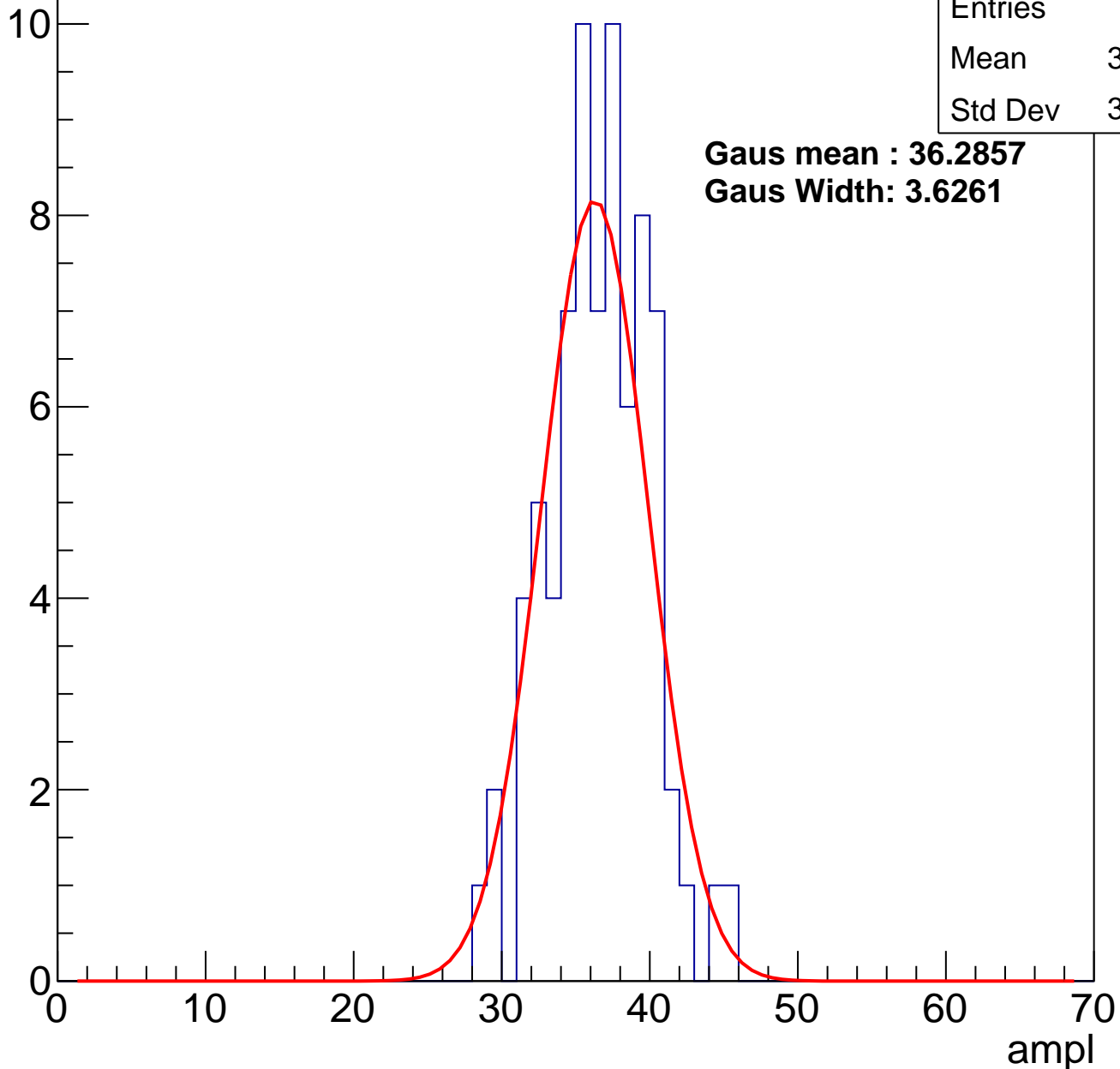
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	76
Mean	36.12
Std Dev	3.372

**Gaus mean : 36.2857**

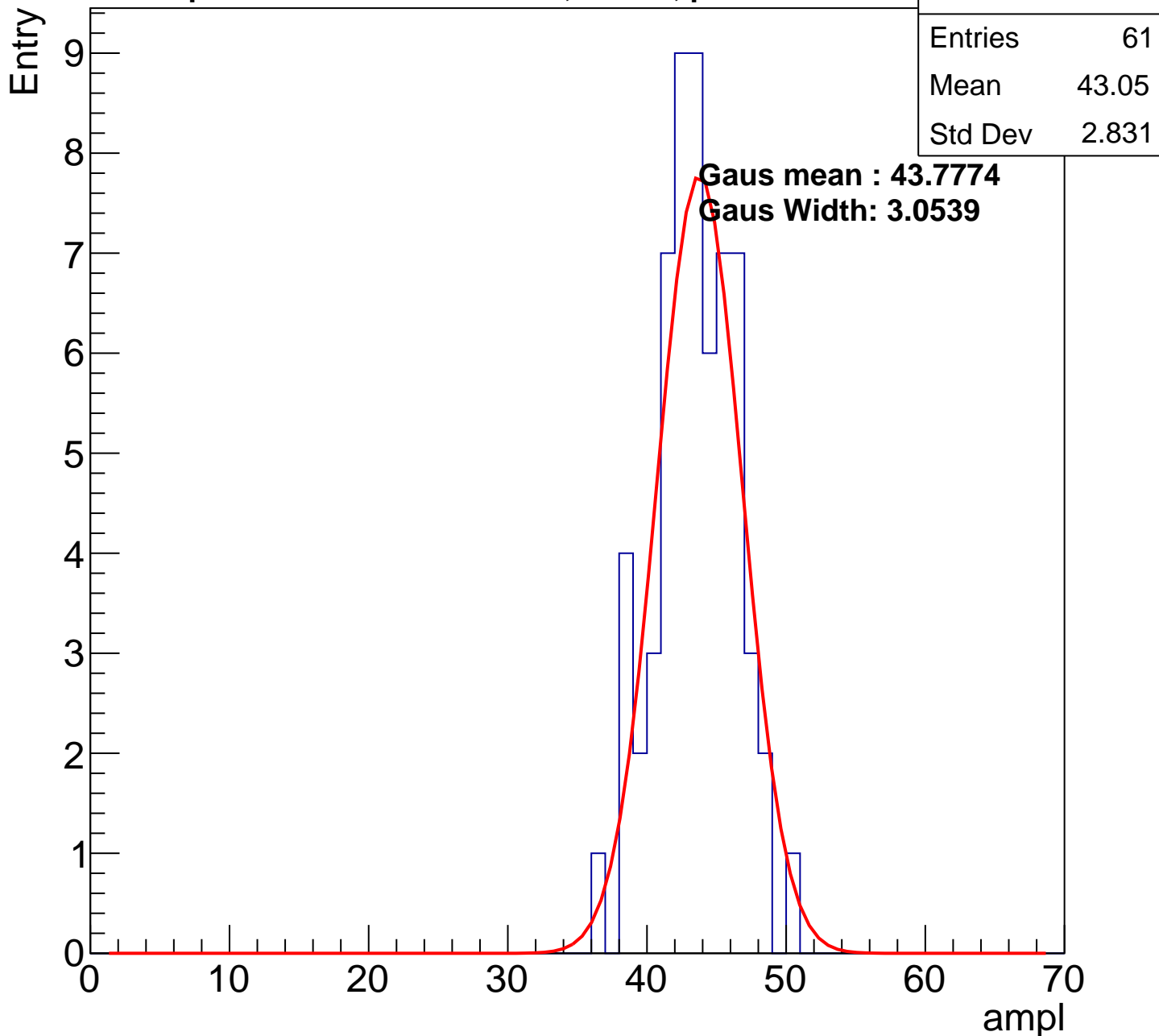
**Gaus Width: 3.6261**

Entry



# B1L102S, U12-ch59, adc2

calib\_packv5\_042523\_0143.root, FC#11, port A2

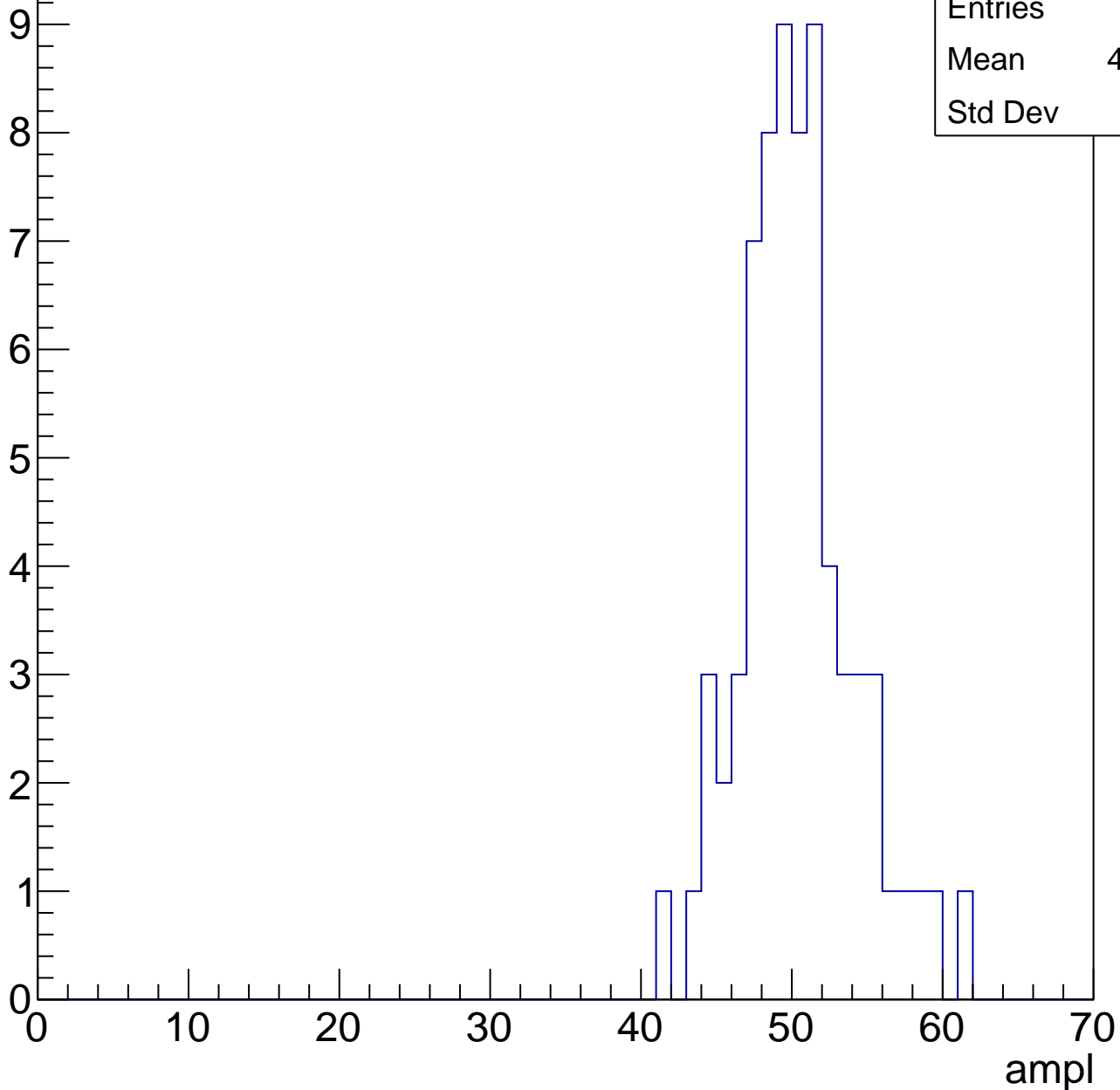


# B1L102S, U12-ch59, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	49.88
Std Dev	3.74

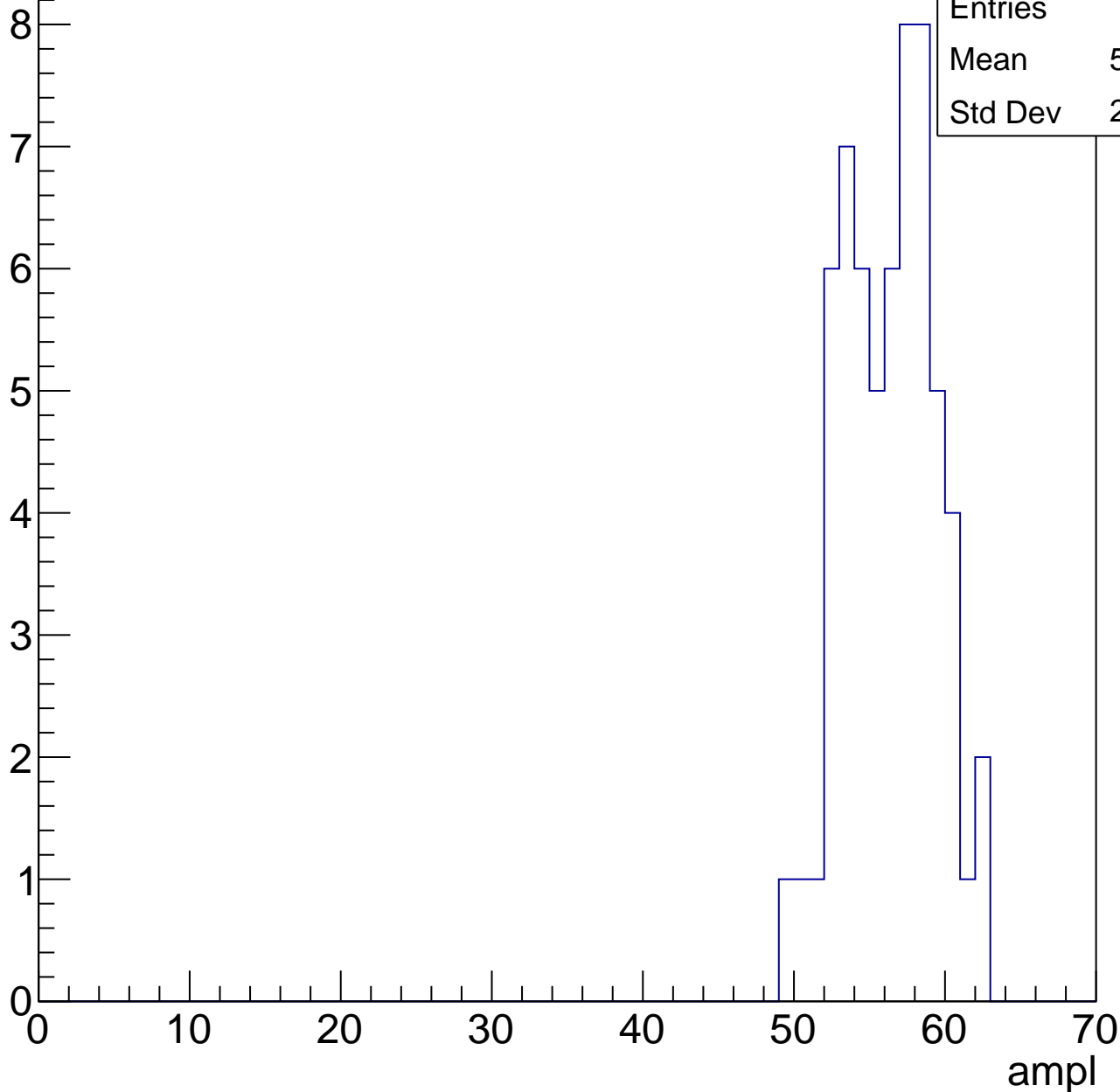


# B1L102S, U12-ch59, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	55.87
Std Dev	2.983

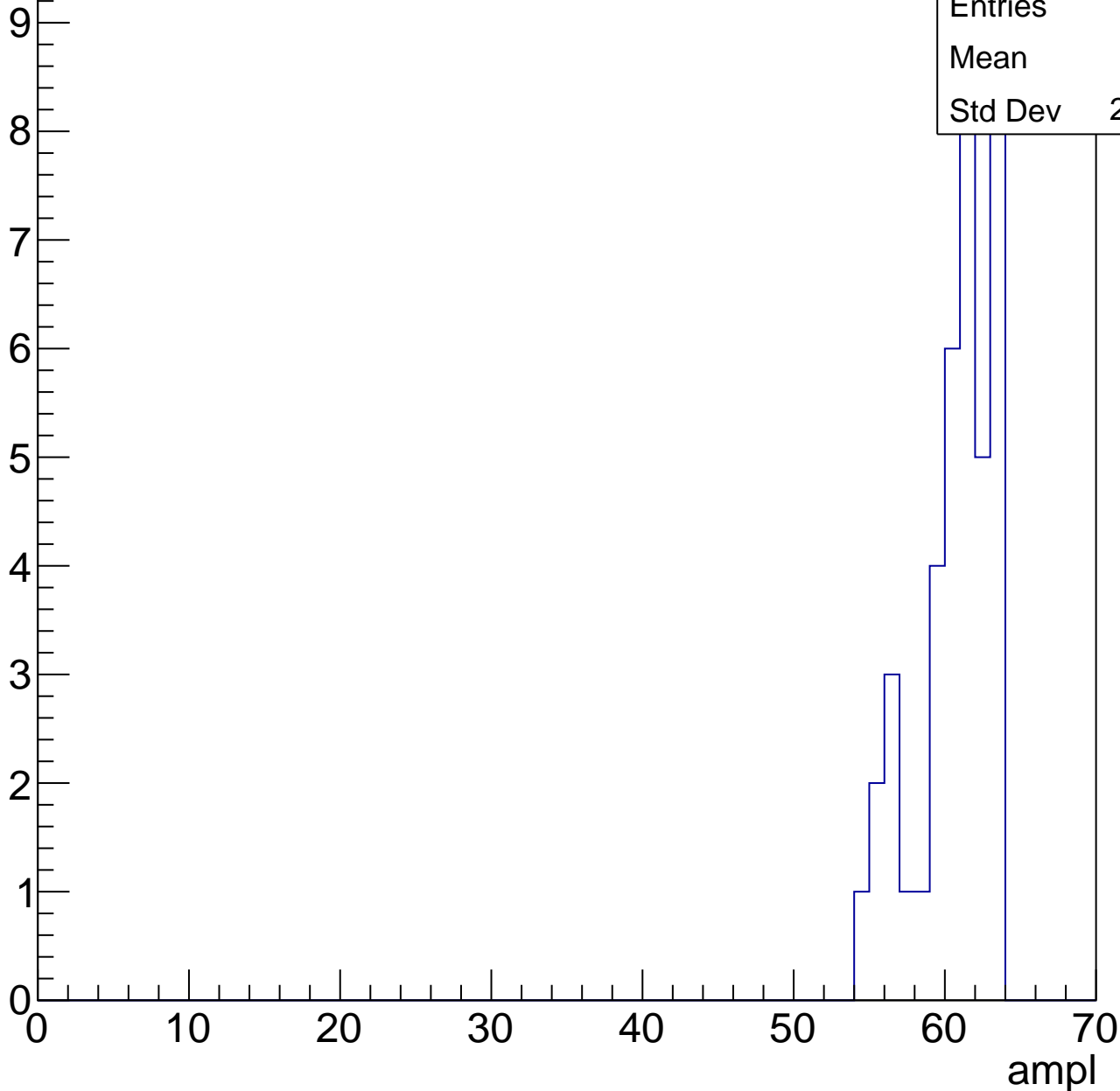


# B1L102S, U12-ch59, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

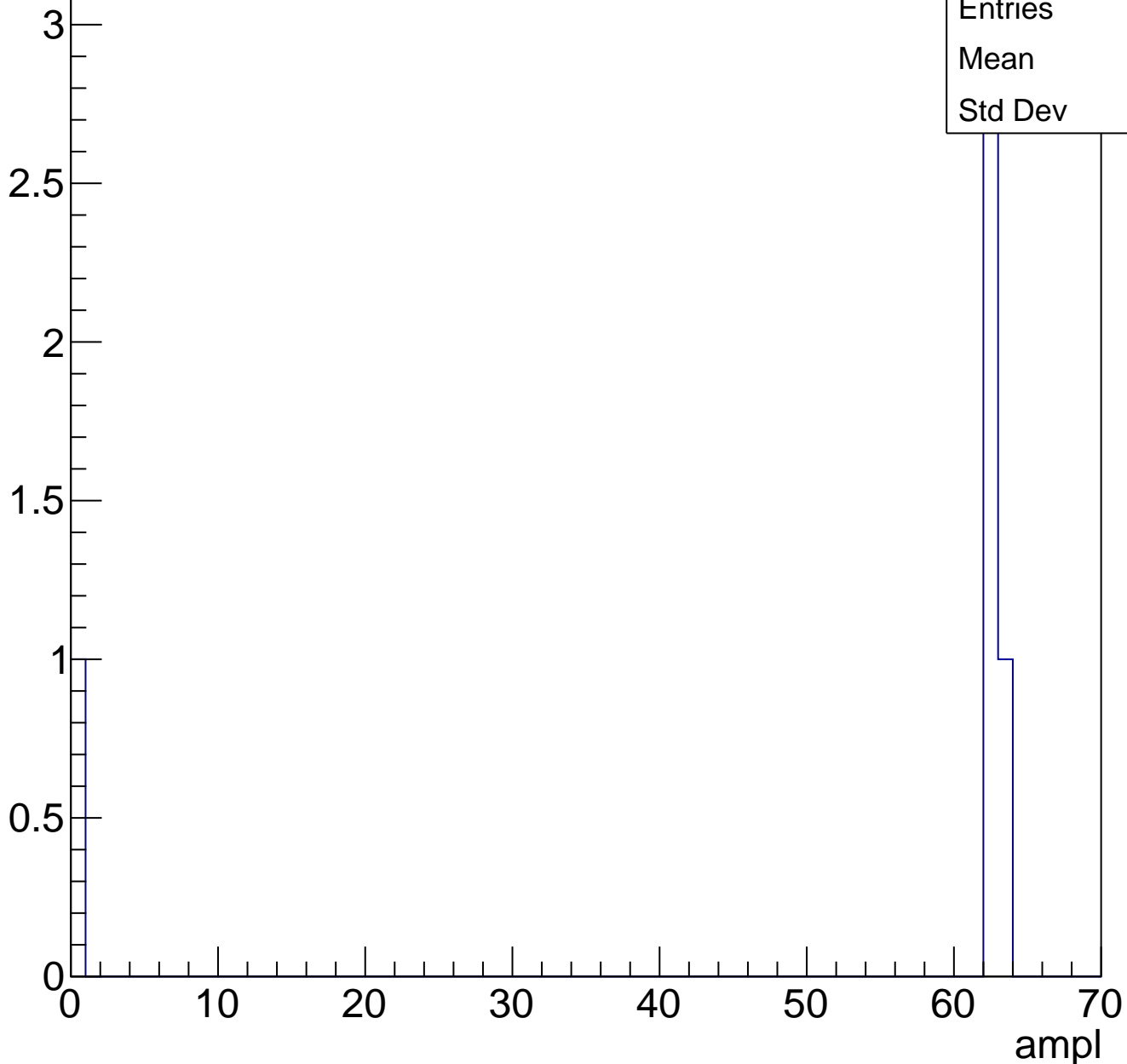
Entries	40
Mean	60.2
Std Dev	2.542



# B1L102S, U12-ch59, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U12-ch59, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U12-ch60, adc0

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	76
Mean	27.66
Std Dev	4.822

**Gaus mean : 28.3560**

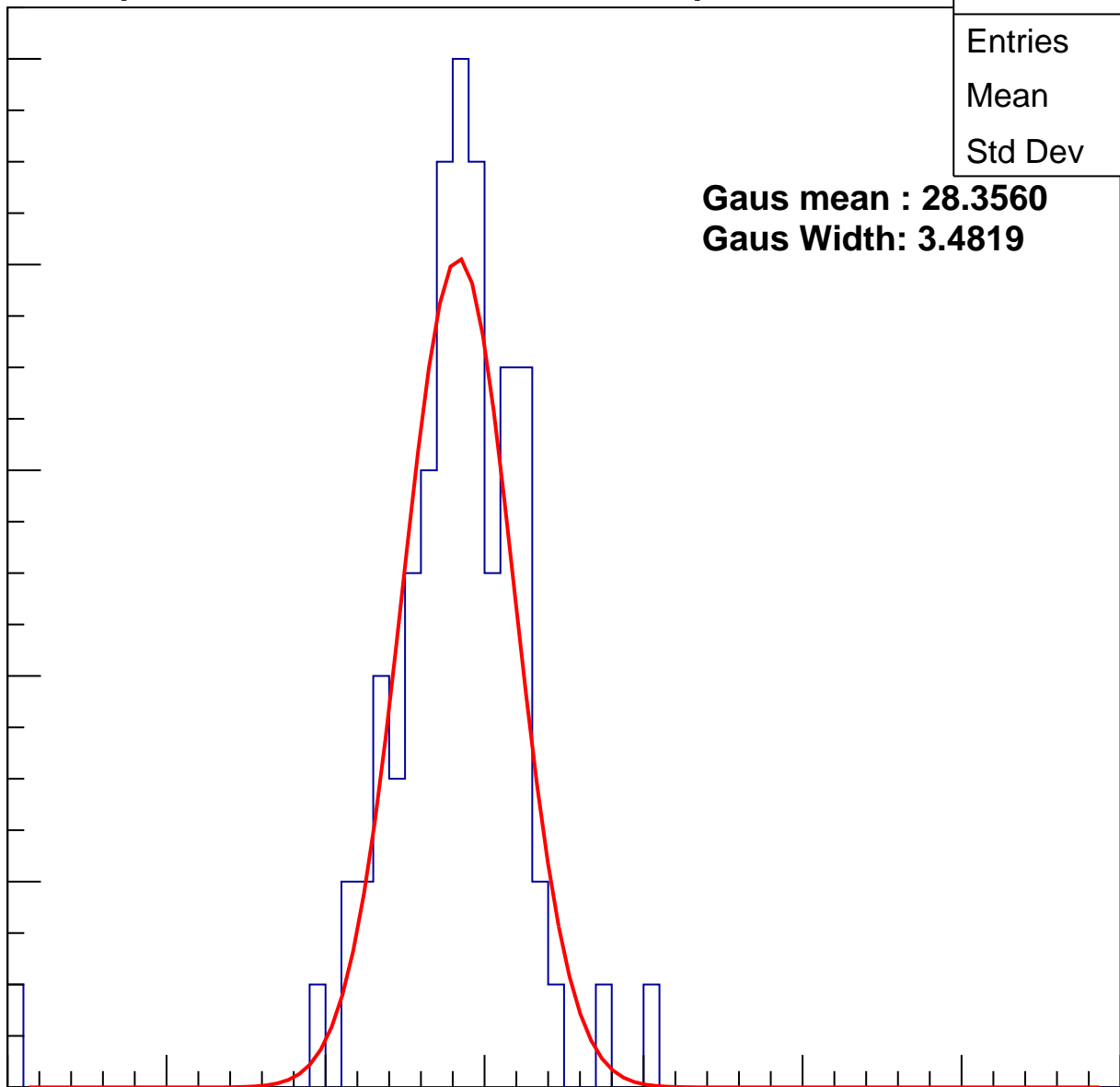
**Gaus Width: 3.4819**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



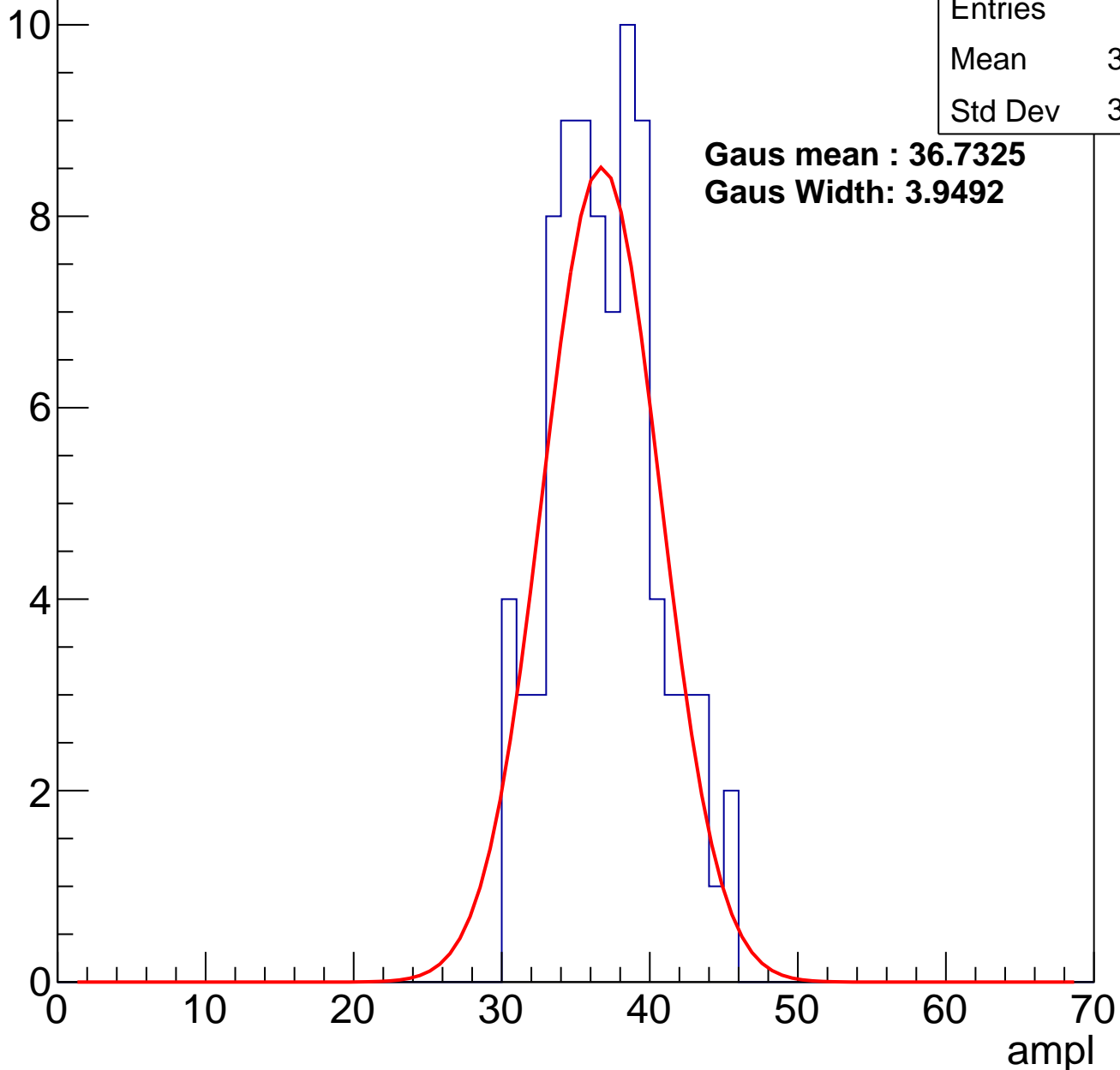
# B1L102S, U12-ch60, adc1

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	86
Mean	36.56
Std Dev	3.585

**Gaus mean : 36.7325**  
**Gaus Width: 3.9492**

Entry



# B1L102S, U12-ch60, adc2

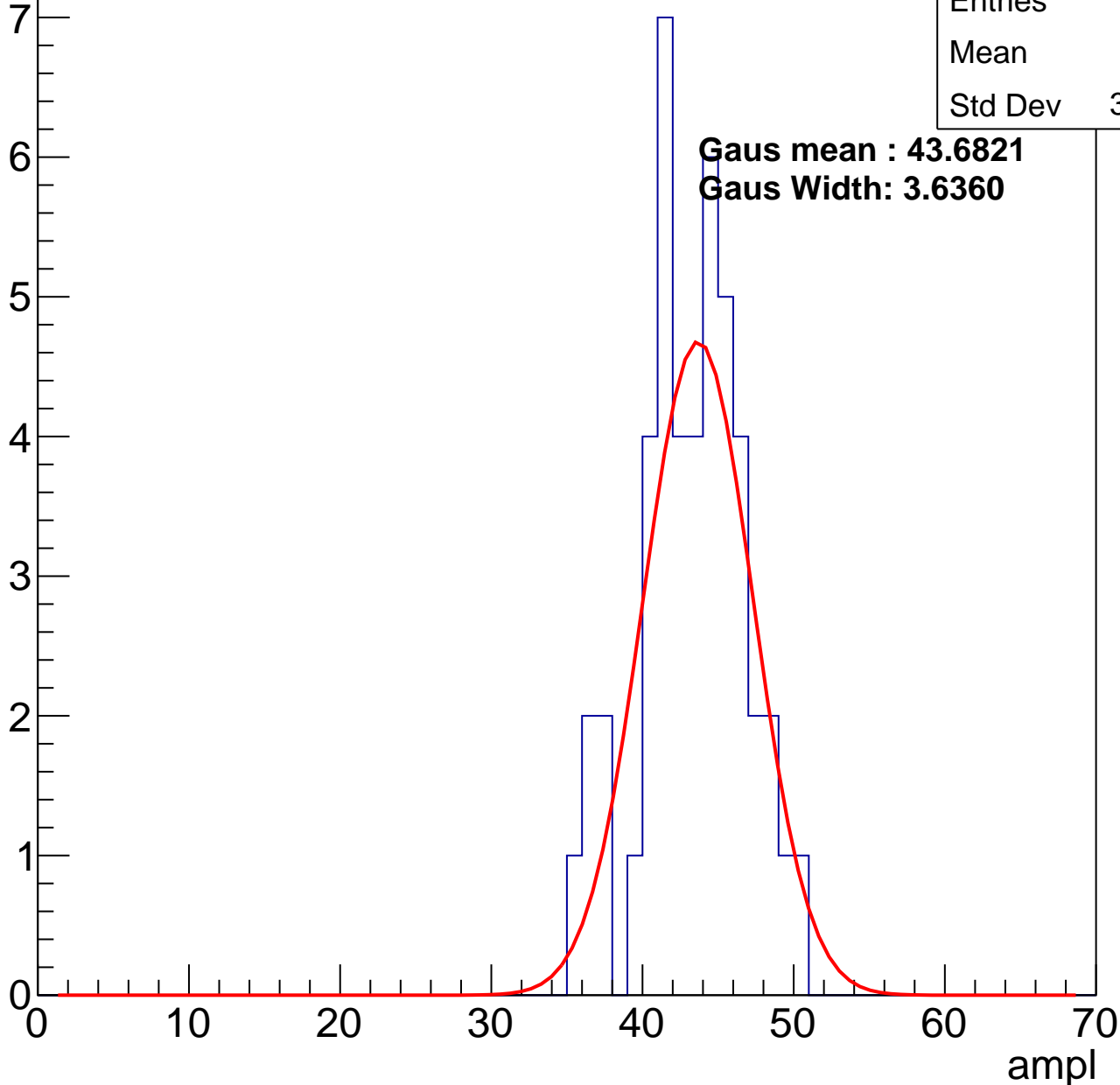
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	46
Mean	42.8
Std Dev	3.443

**Gaus mean : 43.6821**

**Gaus Width: 3.6360**

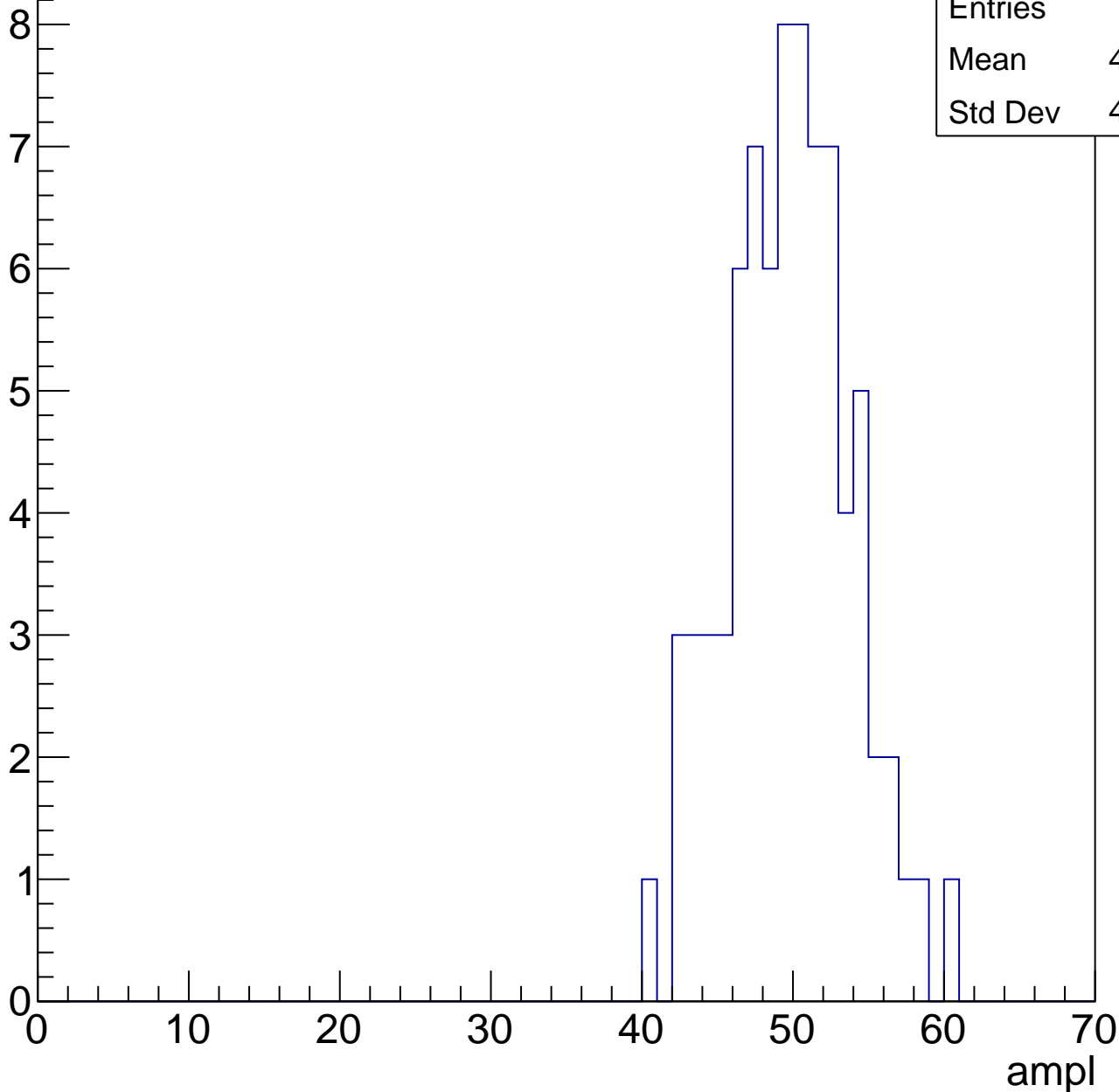


# B1L102S, U12-ch60, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	78
Mean	49.32
Std Dev	4.024

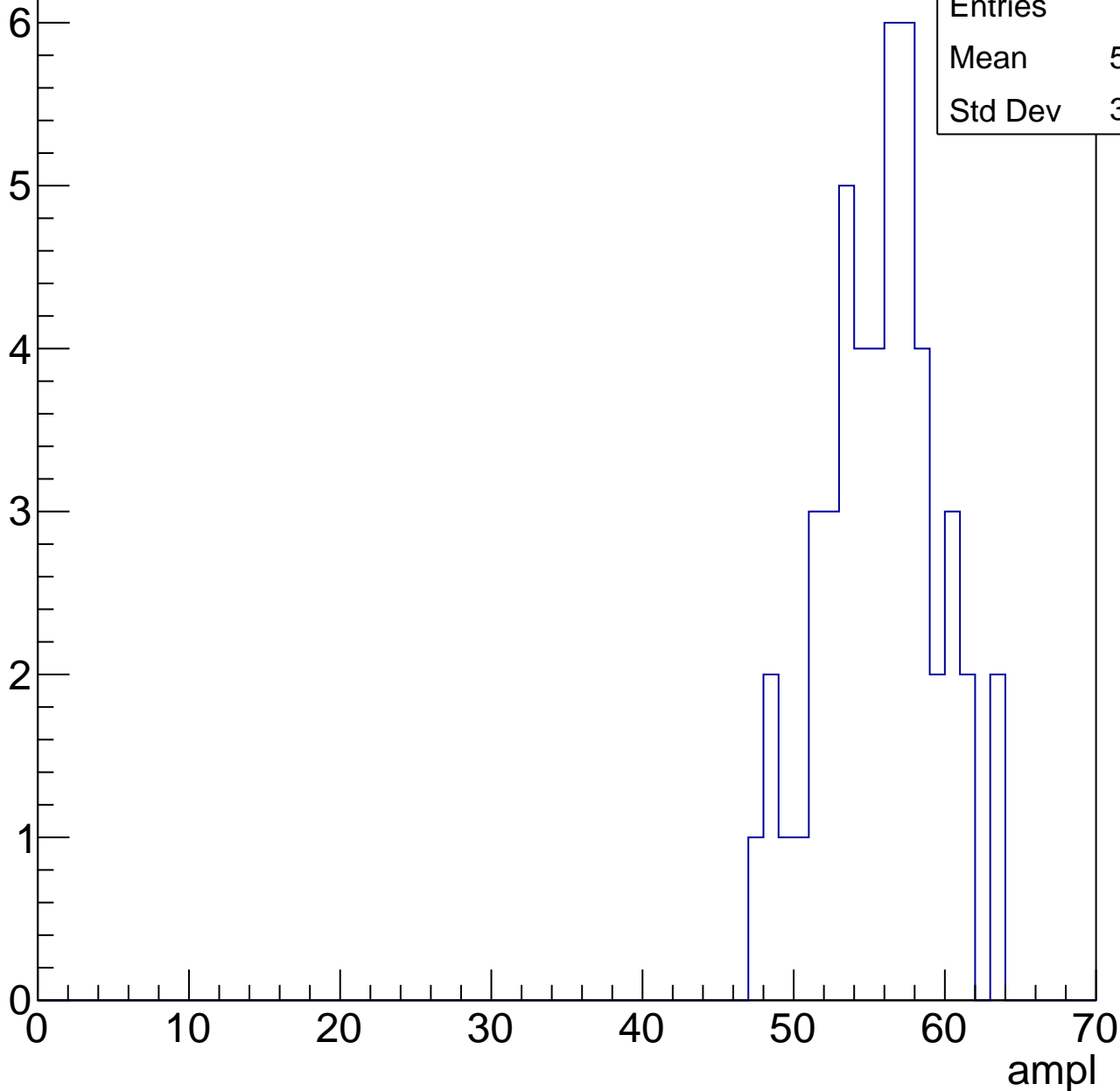


# B1L102S, U12-ch60, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	49
Mean	55.27
Std Dev	3.757

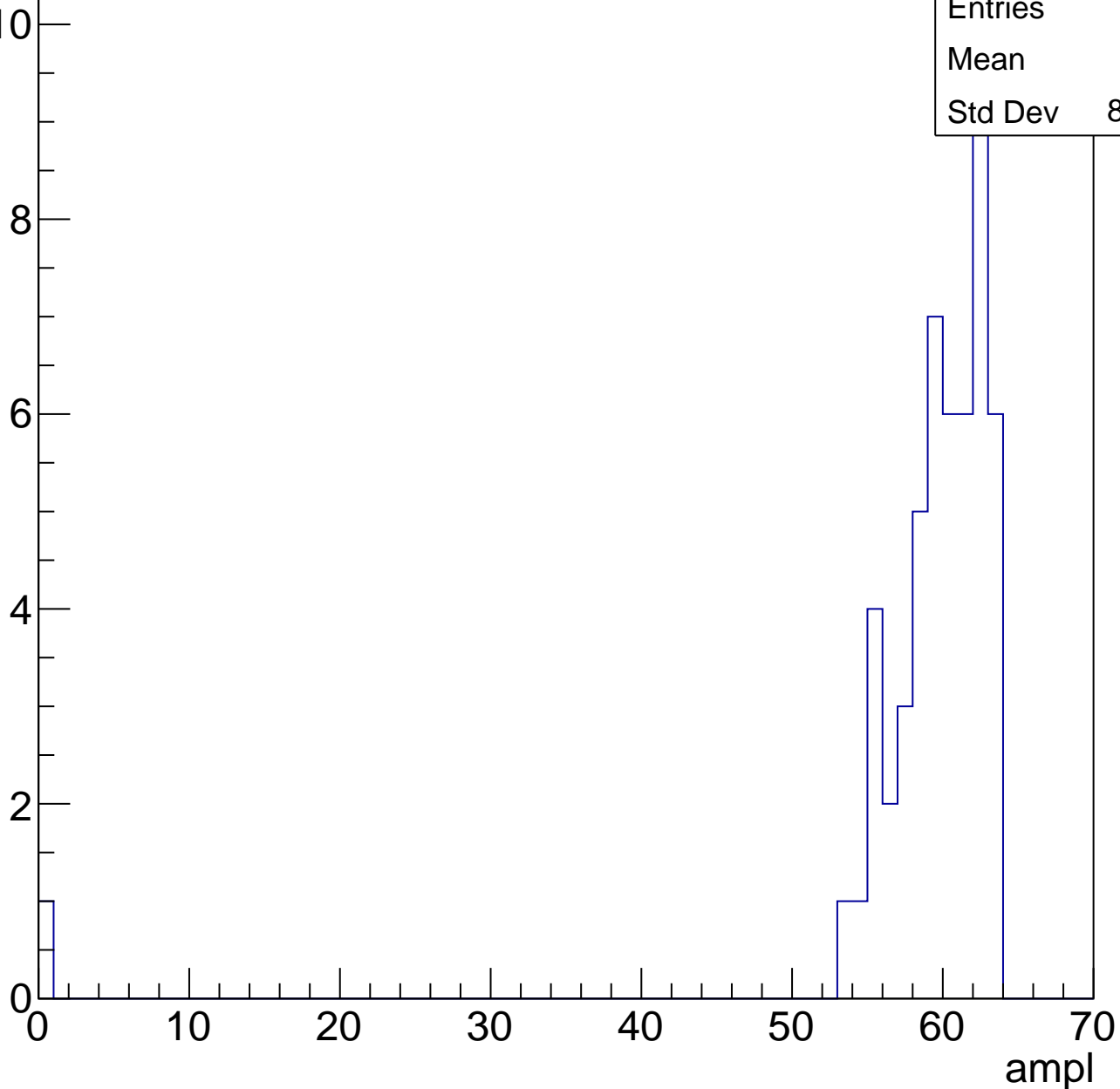


# B1L102S, U12-ch60, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

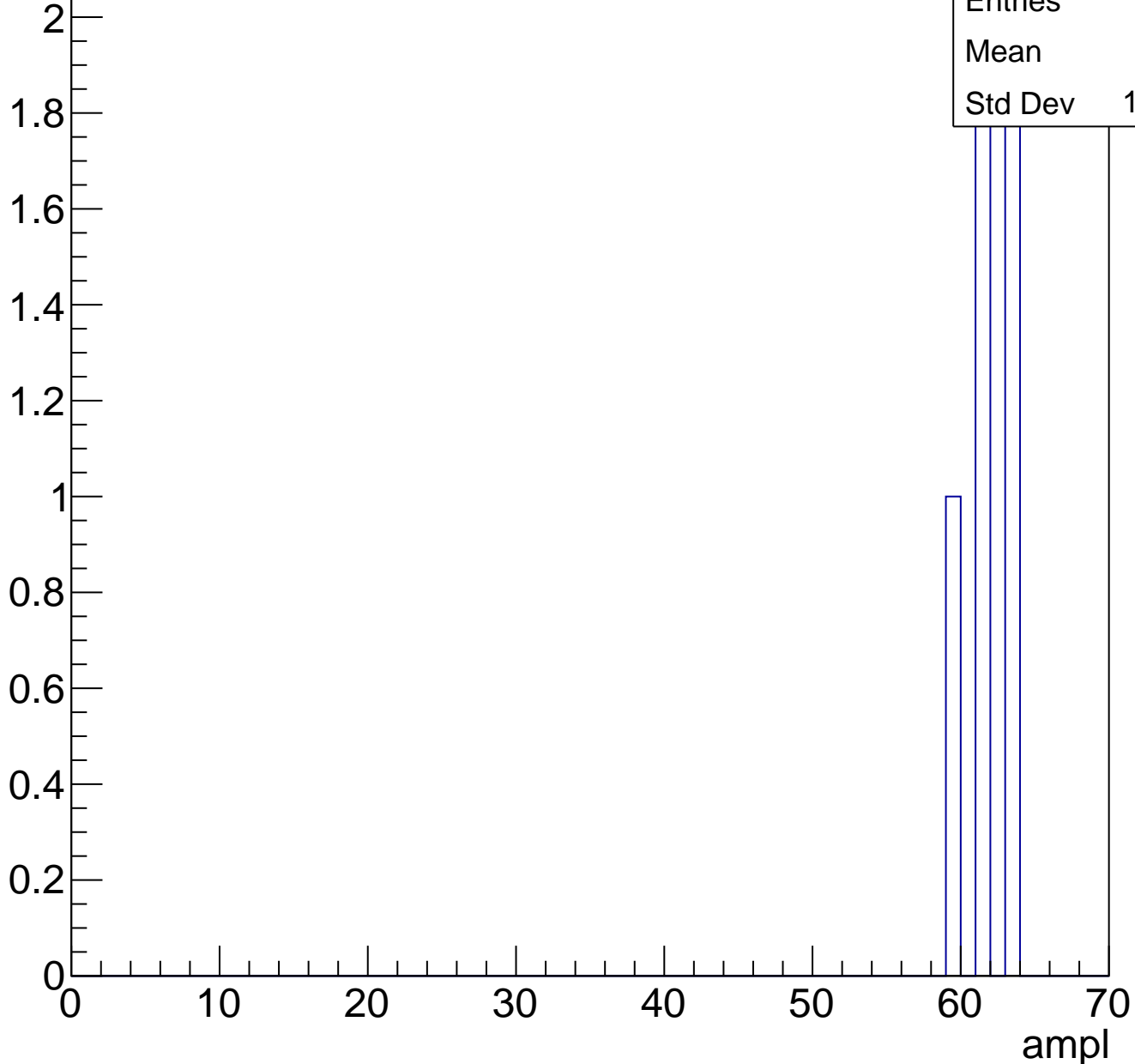
Entries	52
Mean	58.4
Std Dev	8.592



# B1L102S, U12-ch60, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U12-ch60, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U12-ch61, adc0

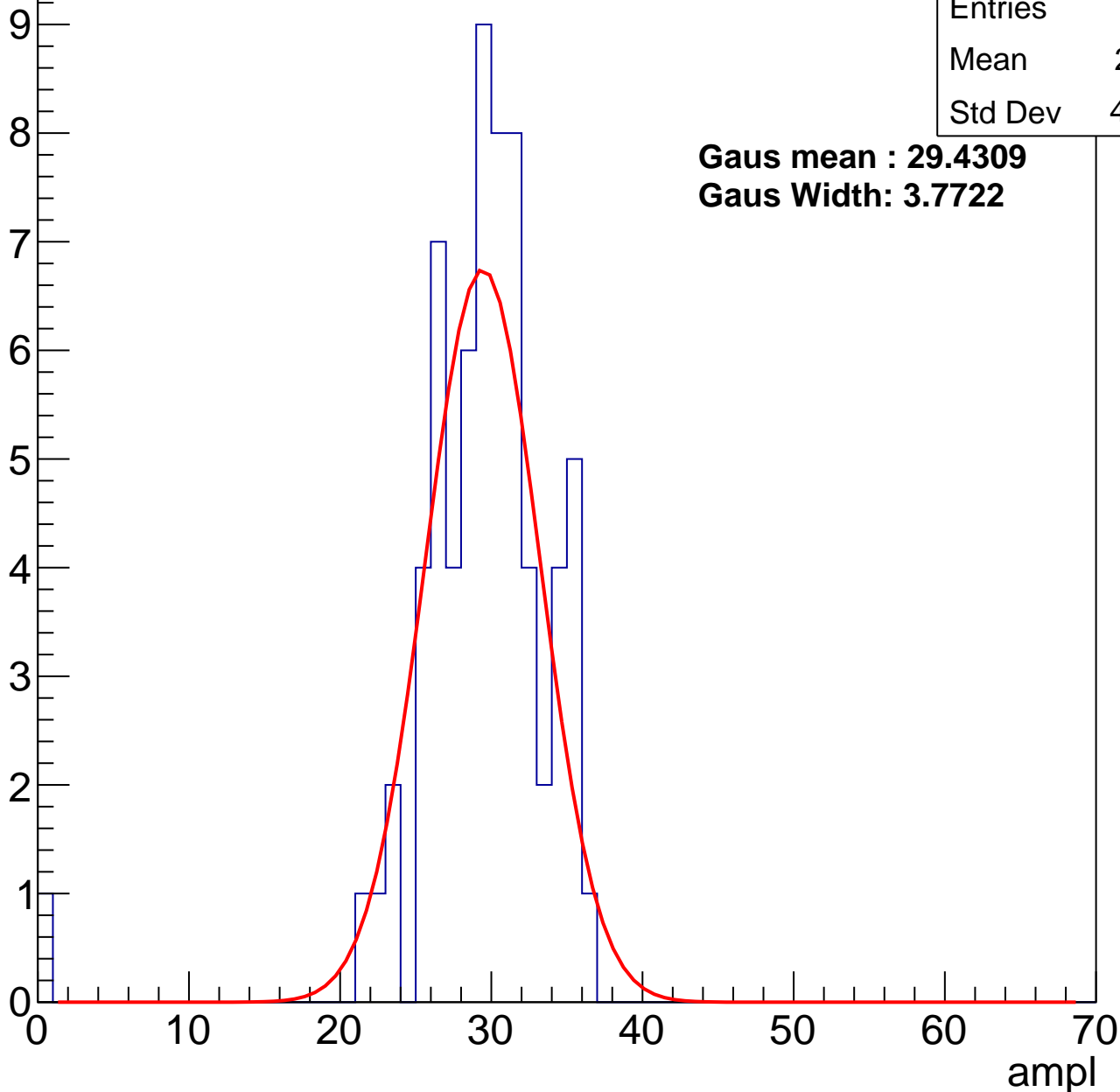
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	67
Mean	28.91
Std Dev	4.904

**Gaus mean : 29.4309**

**Gaus Width: 3.7722**



# B1L102S, U12-ch61, adc1

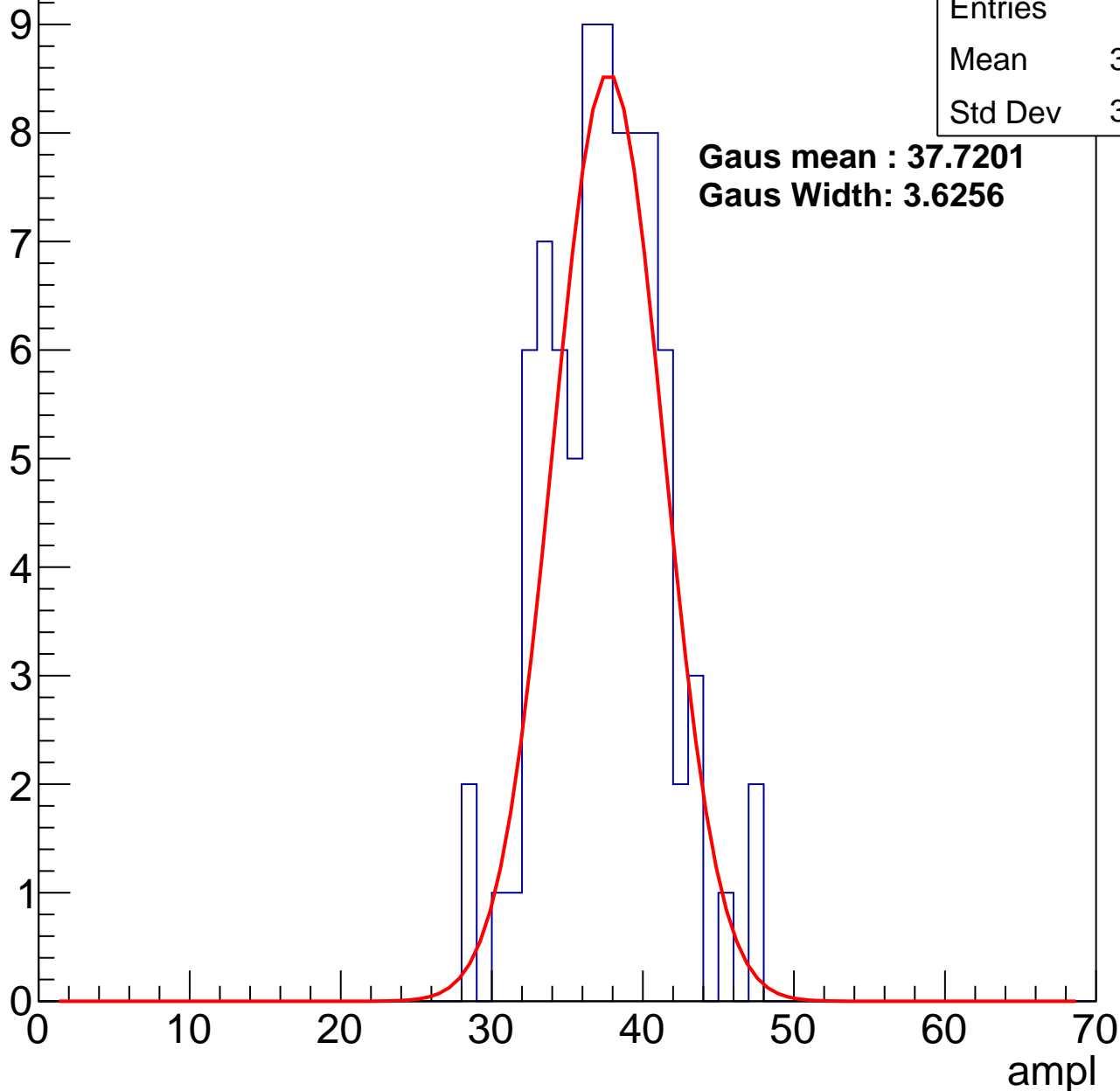
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	84
Mean	37.02
Std Dev	3.814

**Gaus mean : 37.7201**

**Gaus Width: 3.6256**



# B1L102S, U12-ch61, adc2

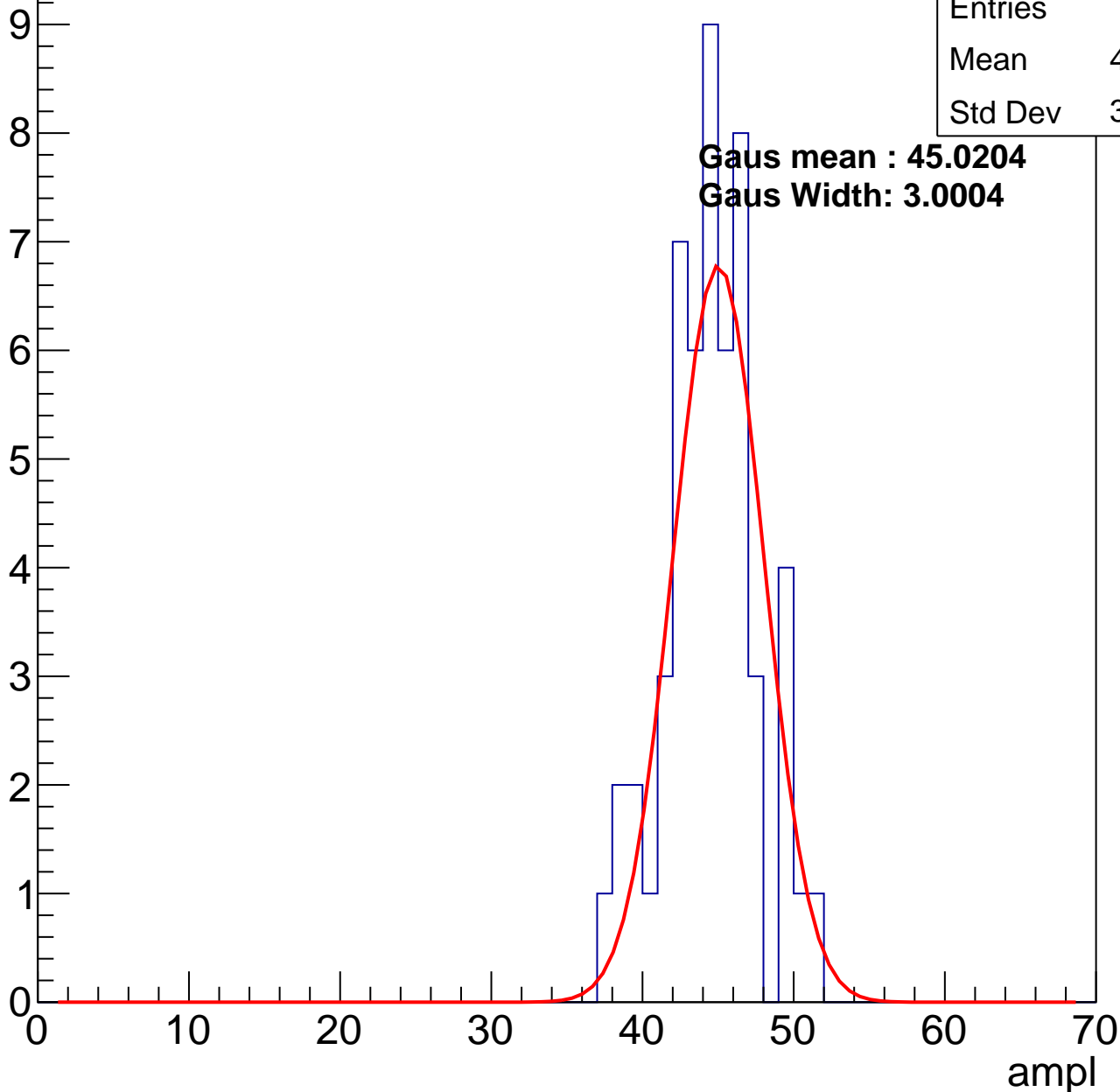
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	54
Mean	44.04
Std Dev	3.037

**Gaus mean : 45.0204**

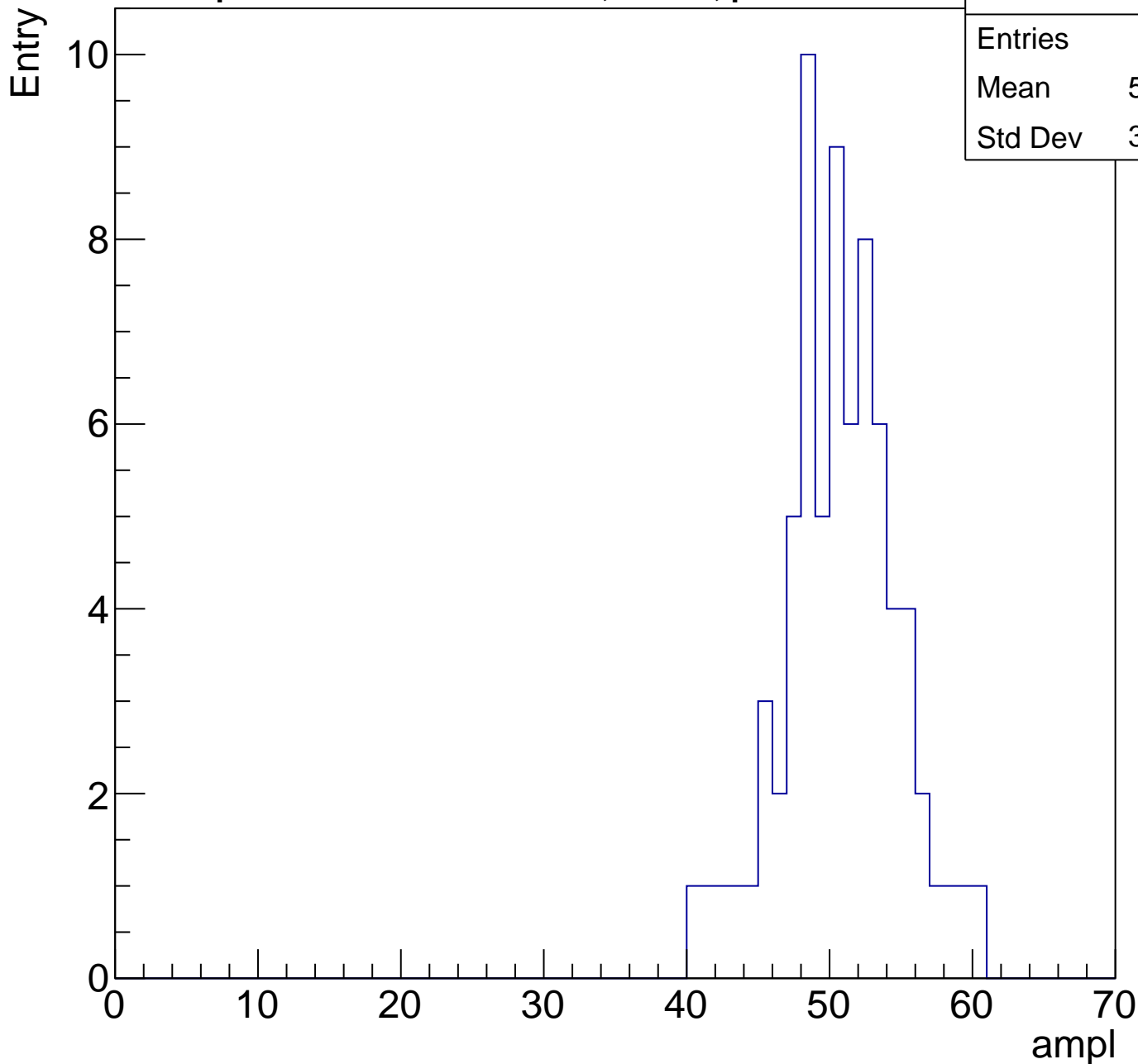
**Gaus Width: 3.0004**



# B1L102S, U12-ch61, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	73
Mean	50.26
Std Dev	3.959

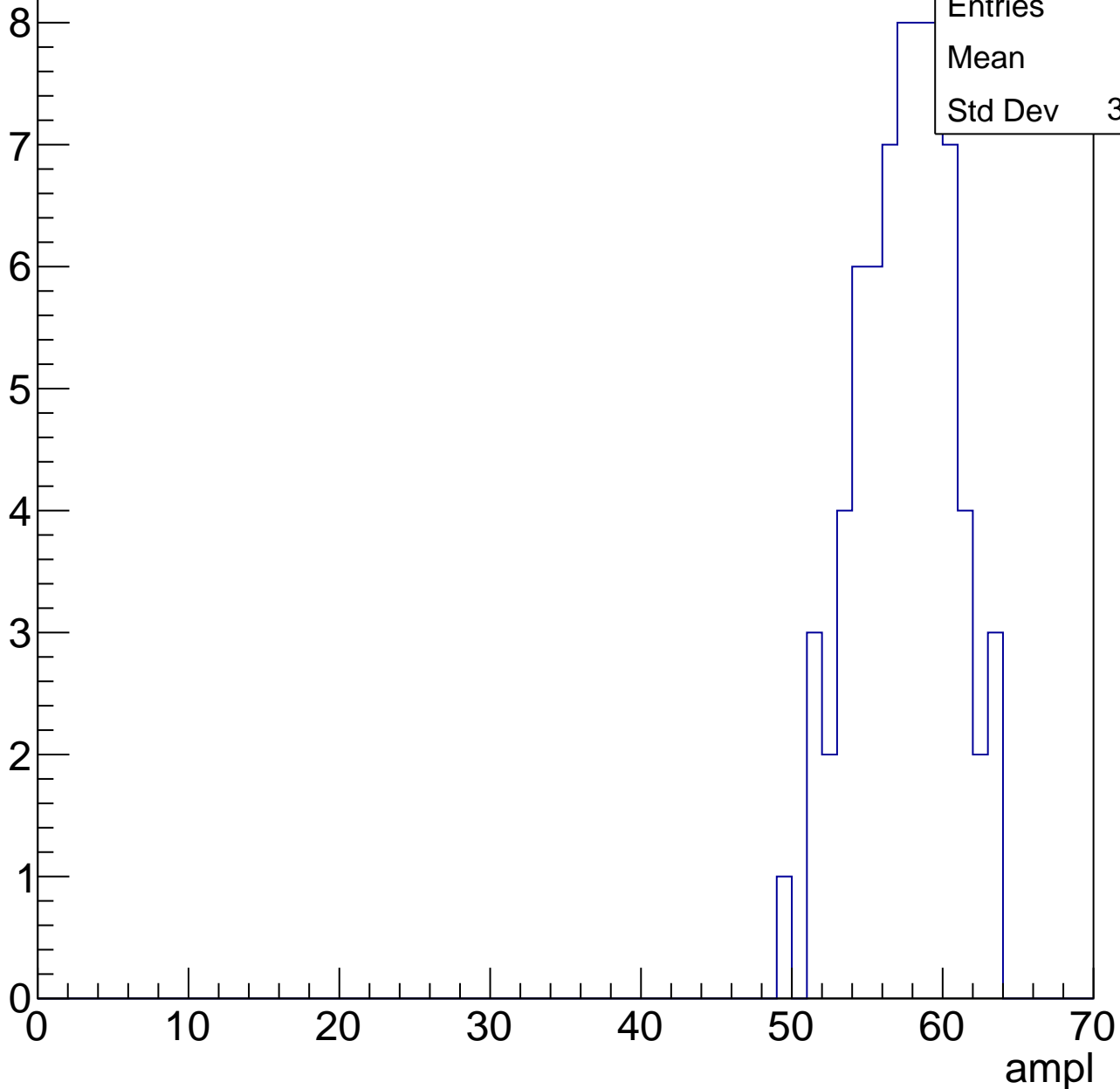


# B1L102S, U12-ch61, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	57
Std Dev	3.176

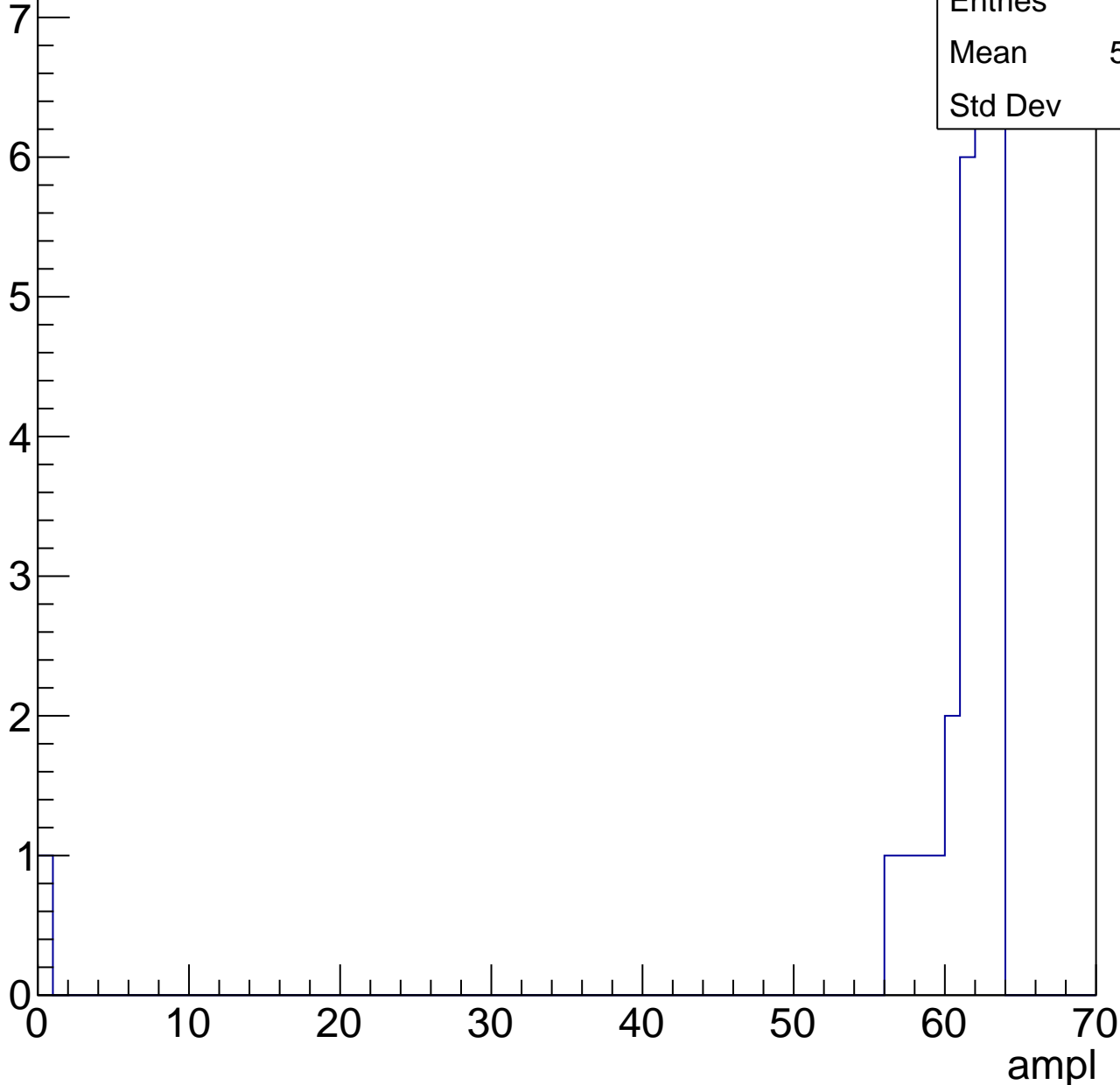


# B1L102S, U12-ch61, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	27
Mean	58.93
Std Dev	11.7



# B1L102S, U12-ch61, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U12-ch61, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U12-ch62, adc0

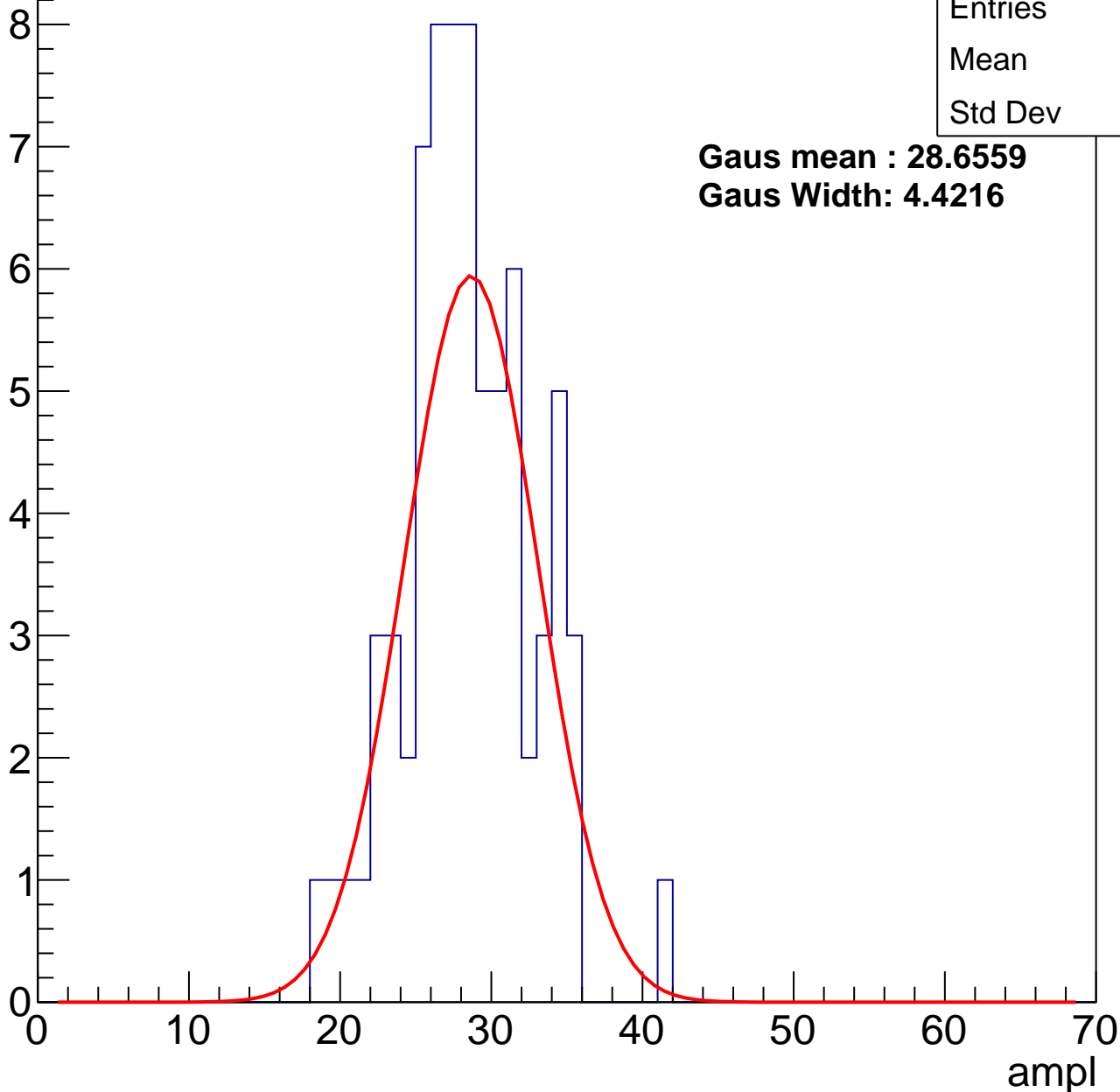
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	73
Mean	28
Std Dev	4.21

**Gaus mean : 28.6559**

**Gaus Width: 4.4216**



# B1L102S, U12-ch62, adc1

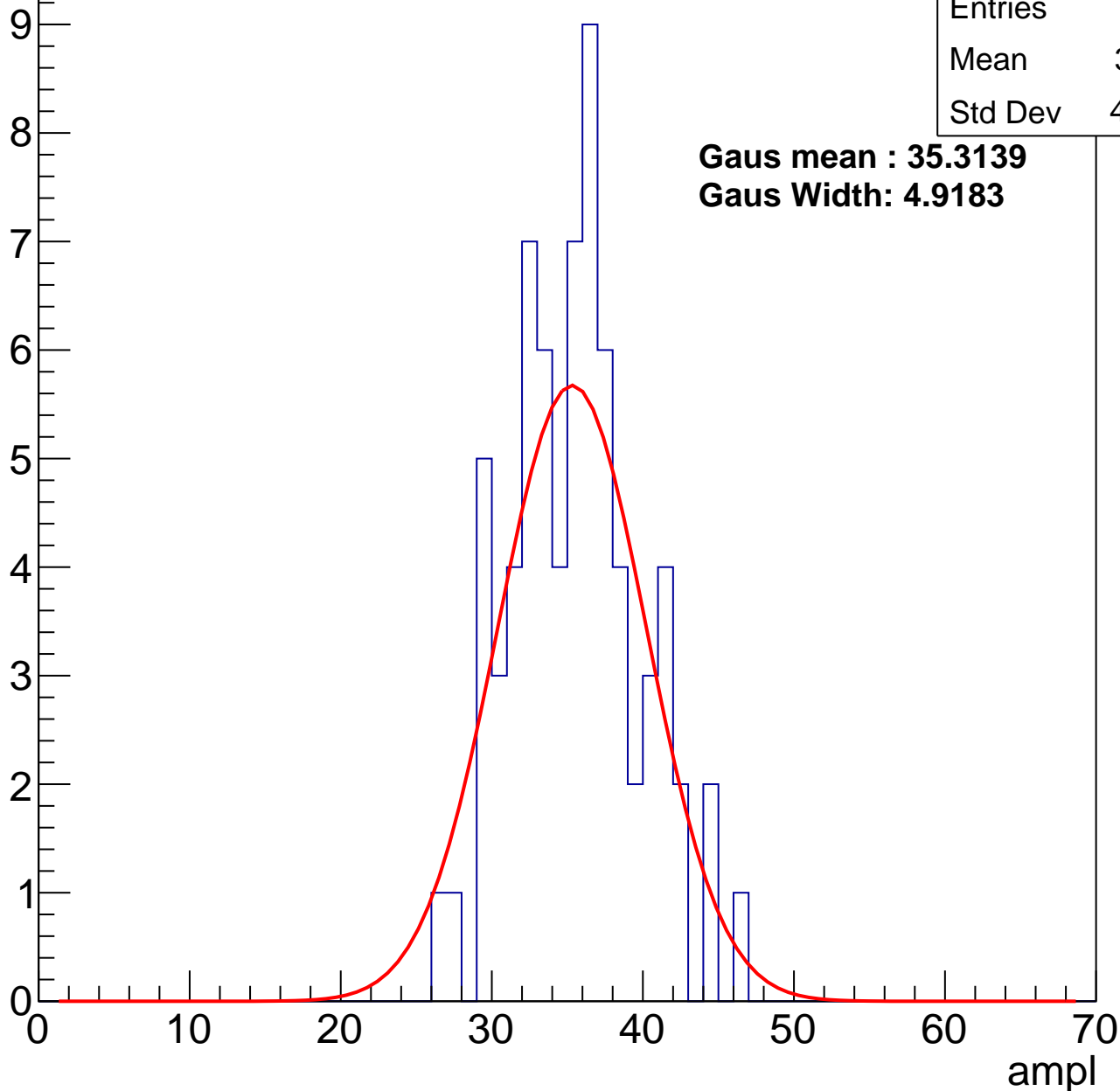
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	71
Mean	35.11
Std Dev	4.204

**Gaus mean : 35.3139**

**Gaus Width: 4.9183**



# B1L102S, U12-ch62, adc2

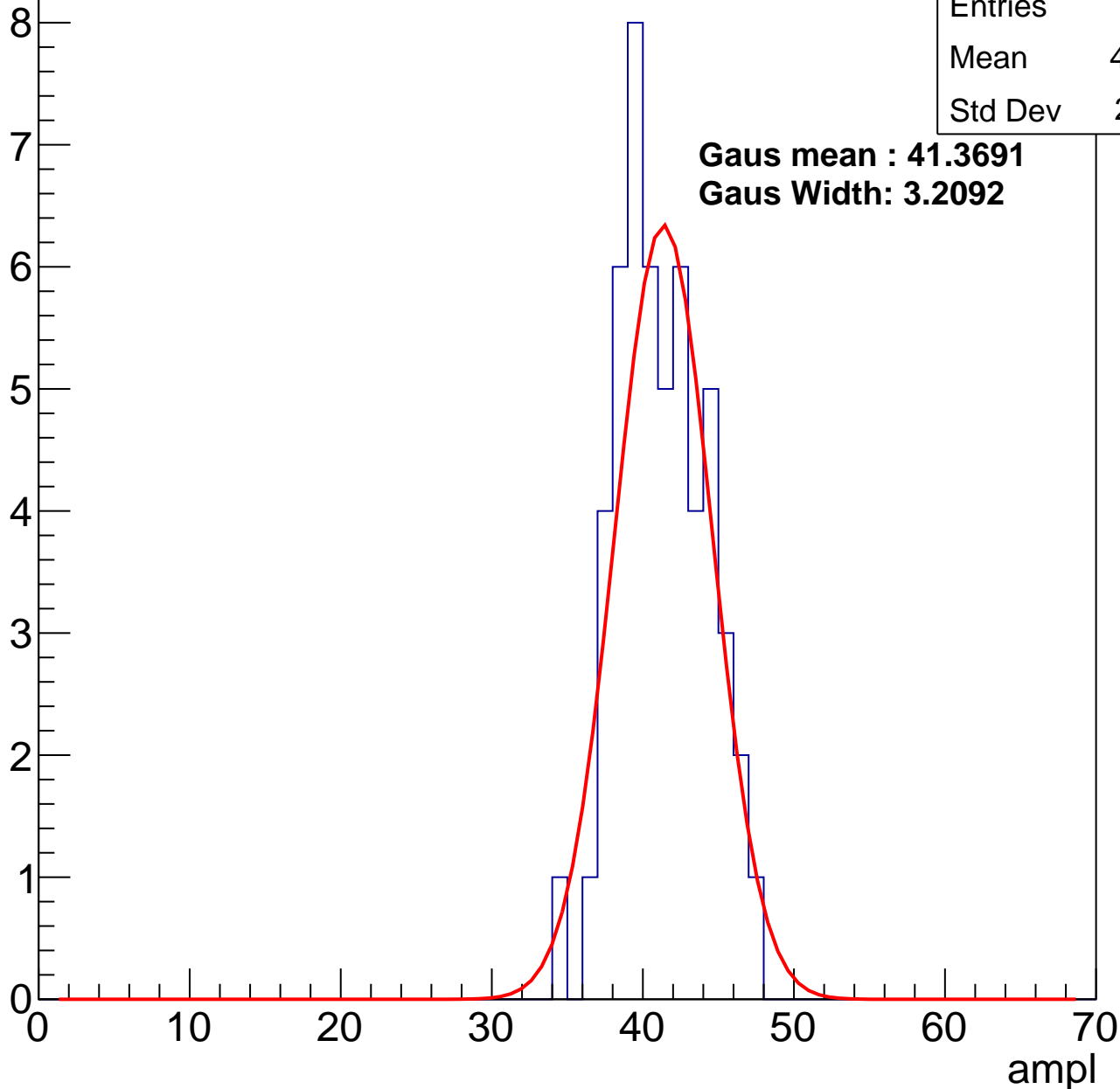
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	52
Mean	40.79
Std Dev	2.871

**Gaus mean : 41.3691**

**Gaus Width: 3.2092**

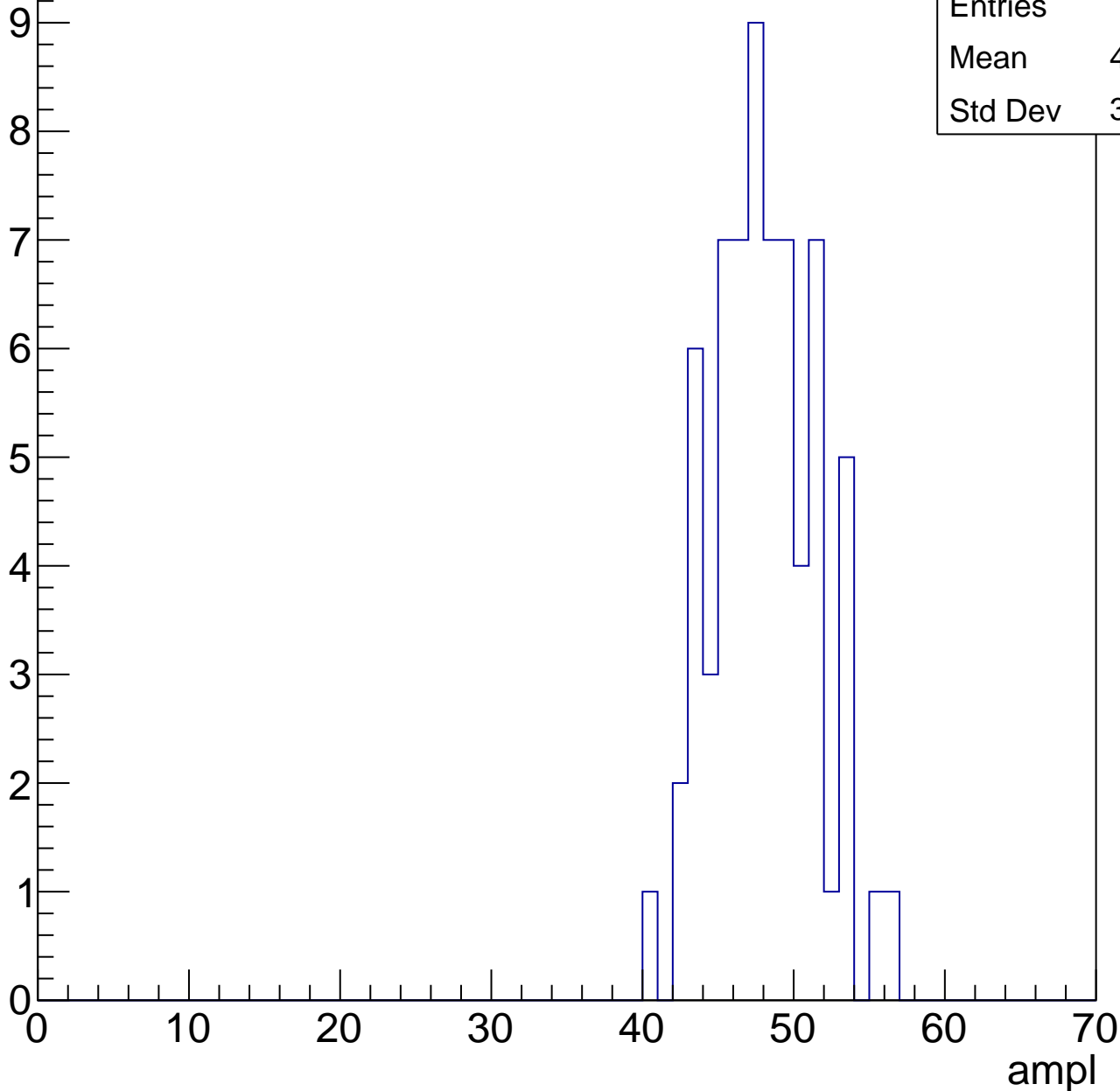


# B1L102S, U12-ch62, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	47.62
Std Dev	3.352

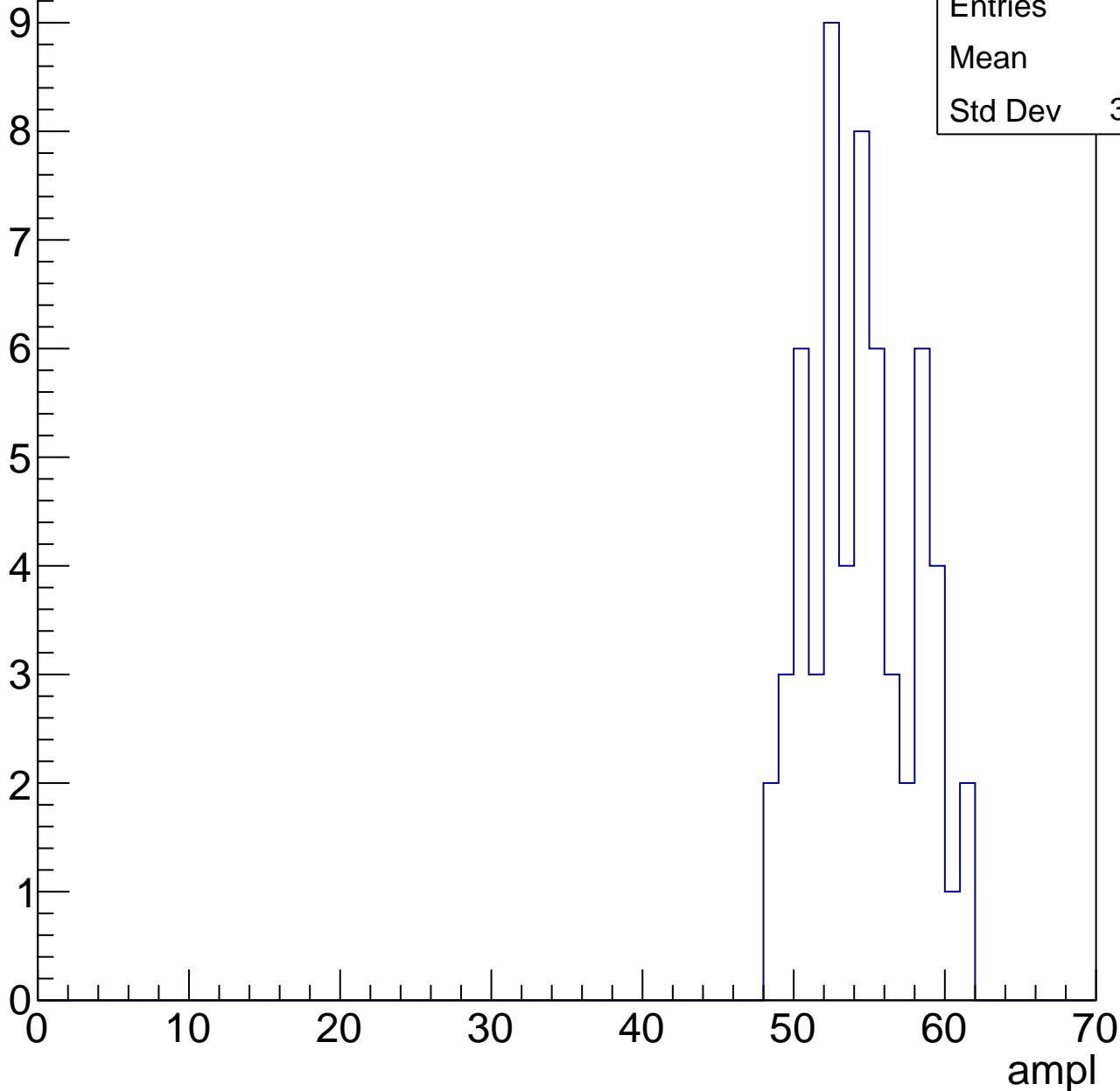


# B1L102S, U12-ch62, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	59
Mean	54
Std Dev	3.385

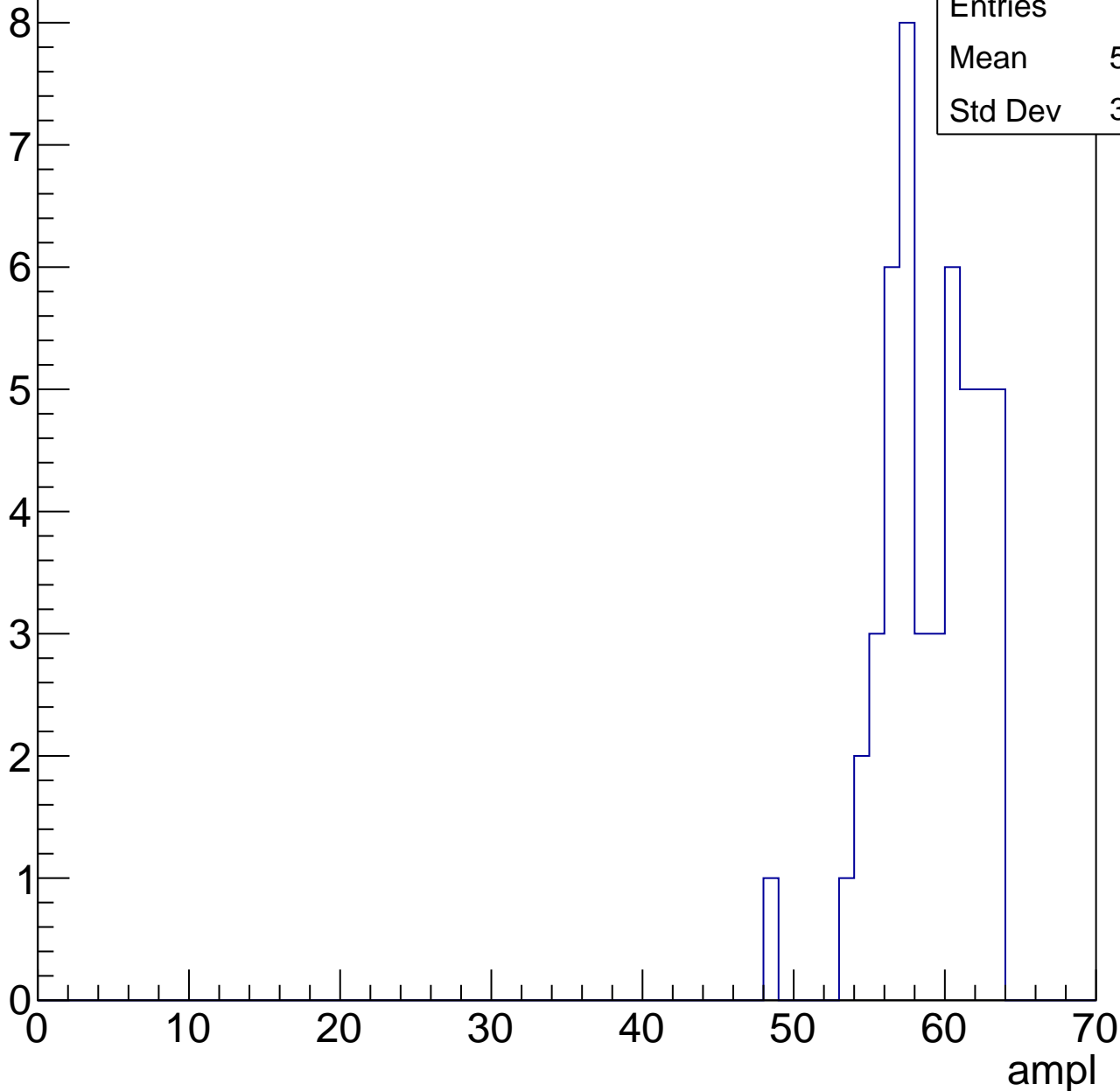


# B1L102S, U12-ch62, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	48
Mean	58.48
Std Dev	3.169

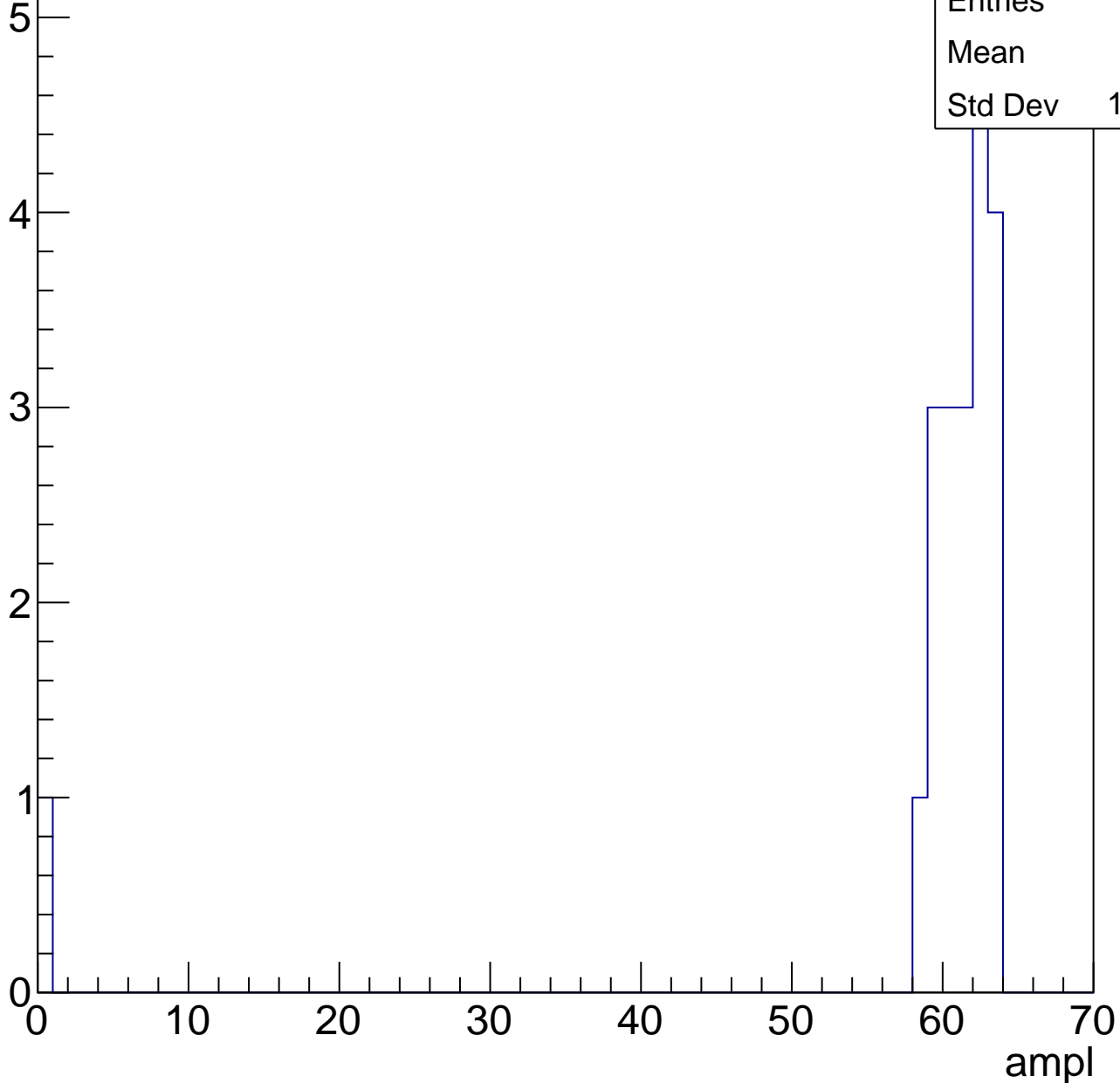


# B1L102S, U12-ch62, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	20
Mean	58
Std Dev	13.39





# B1L102S, U12-ch62, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	1
Mean	63
Std Dev	0

# B1L102S, U12-ch63, adc0

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	71
Mean	30.24
Std Dev	3.652

**Gaus mean : 30.6997**

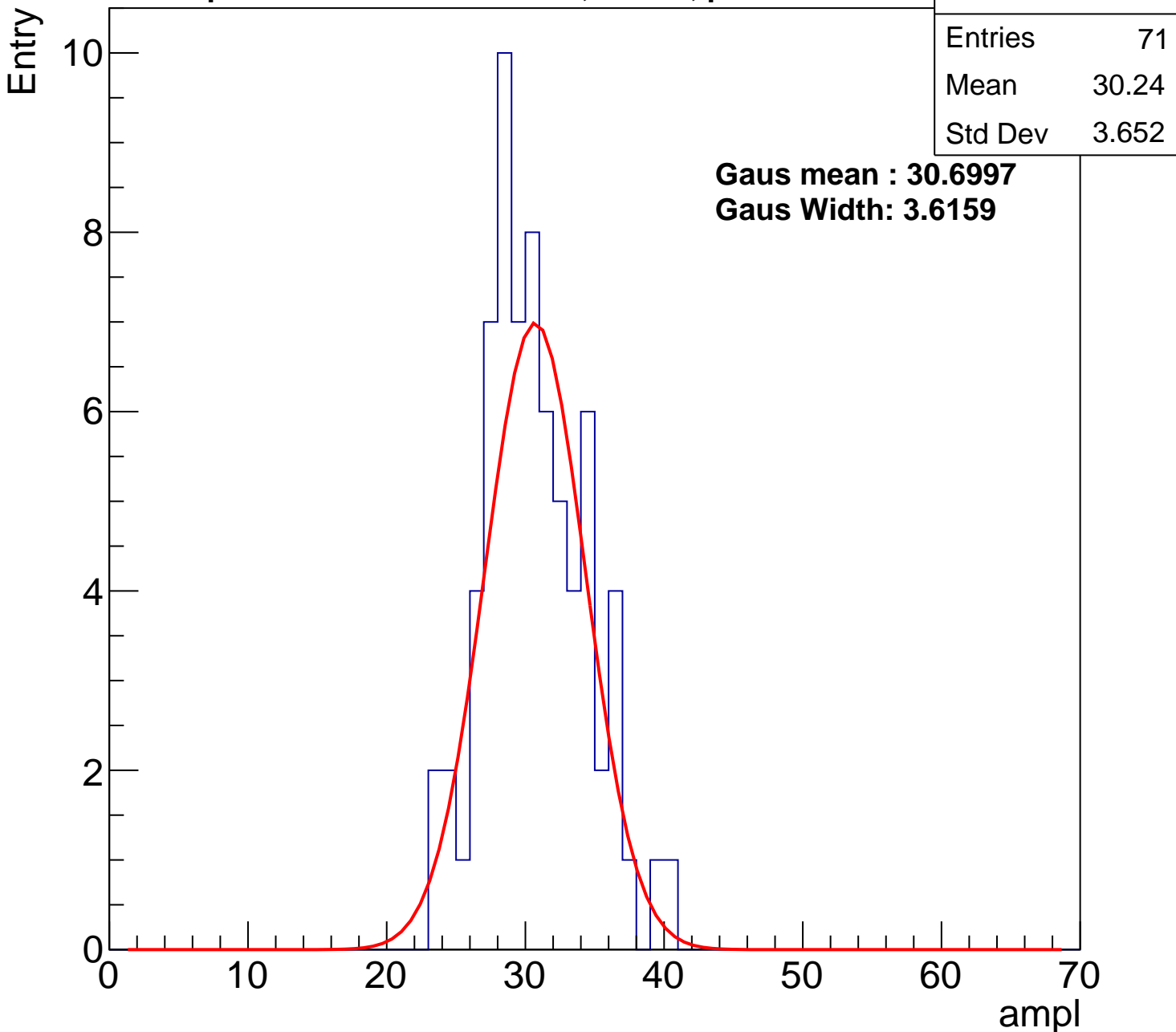
**Gaus Width: 3.6159**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L102S, U12-ch63, adc1

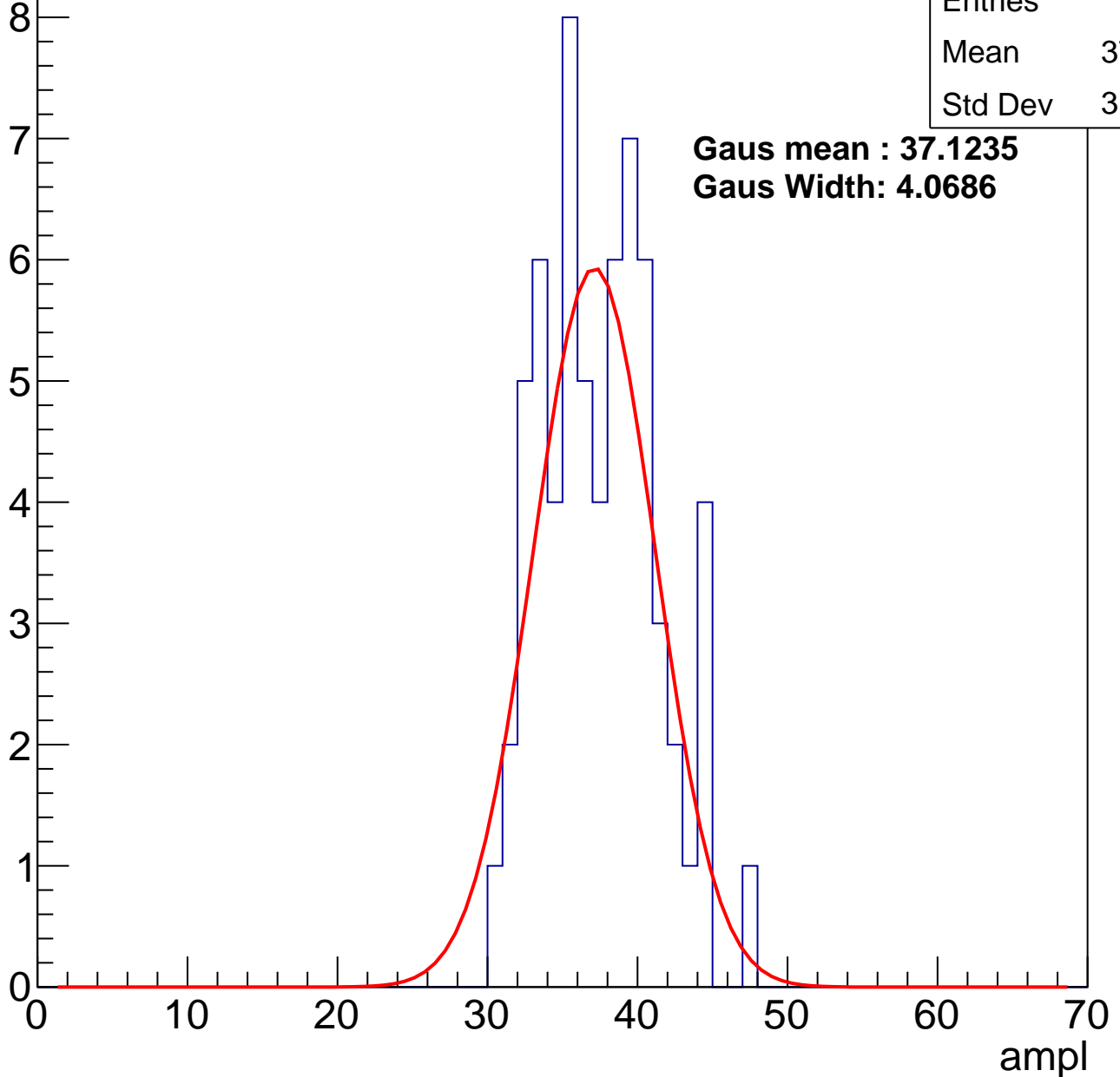
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	65
Mean	37.05
Std Dev	3.788

**Gaus mean : 37.1235**

**Gaus Width: 4.0686**



# B1L102S, U12-ch63, adc2

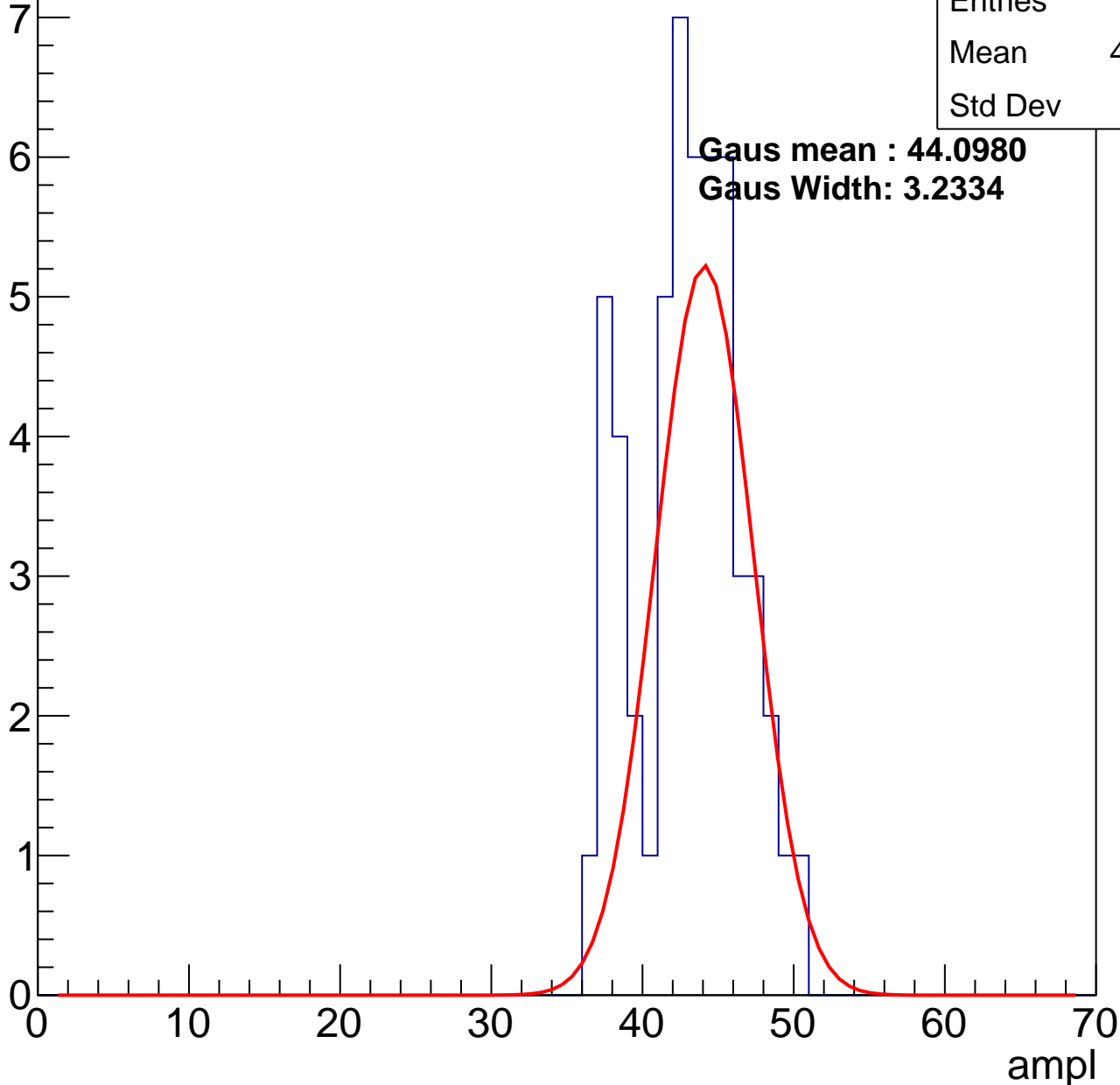
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	53
Mean	42.57
Std Dev	3.44

**Gaus mean : 44.0980**

**Gaus Width: 3.2334**

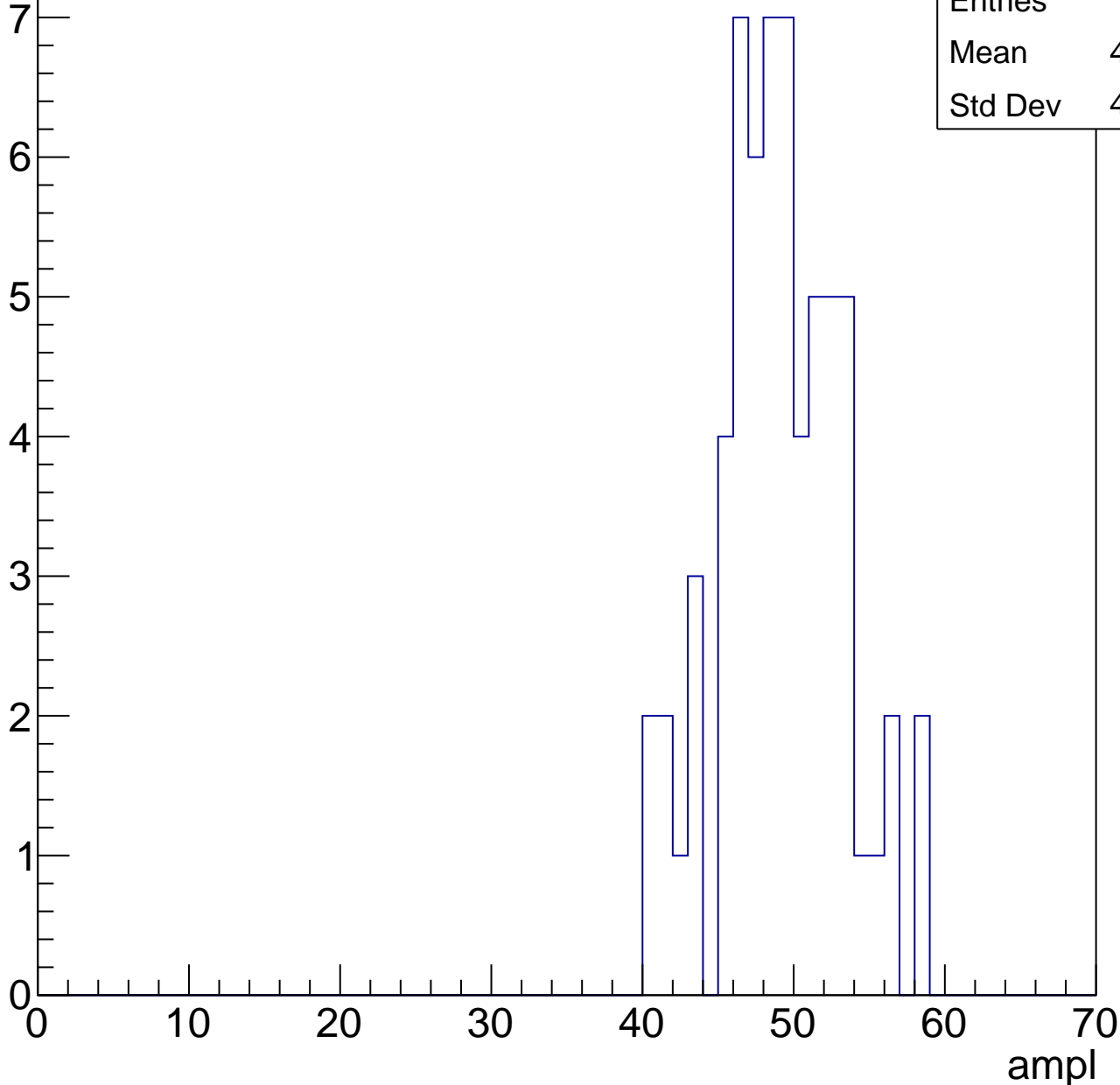


# B1L102S, U12-ch63, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

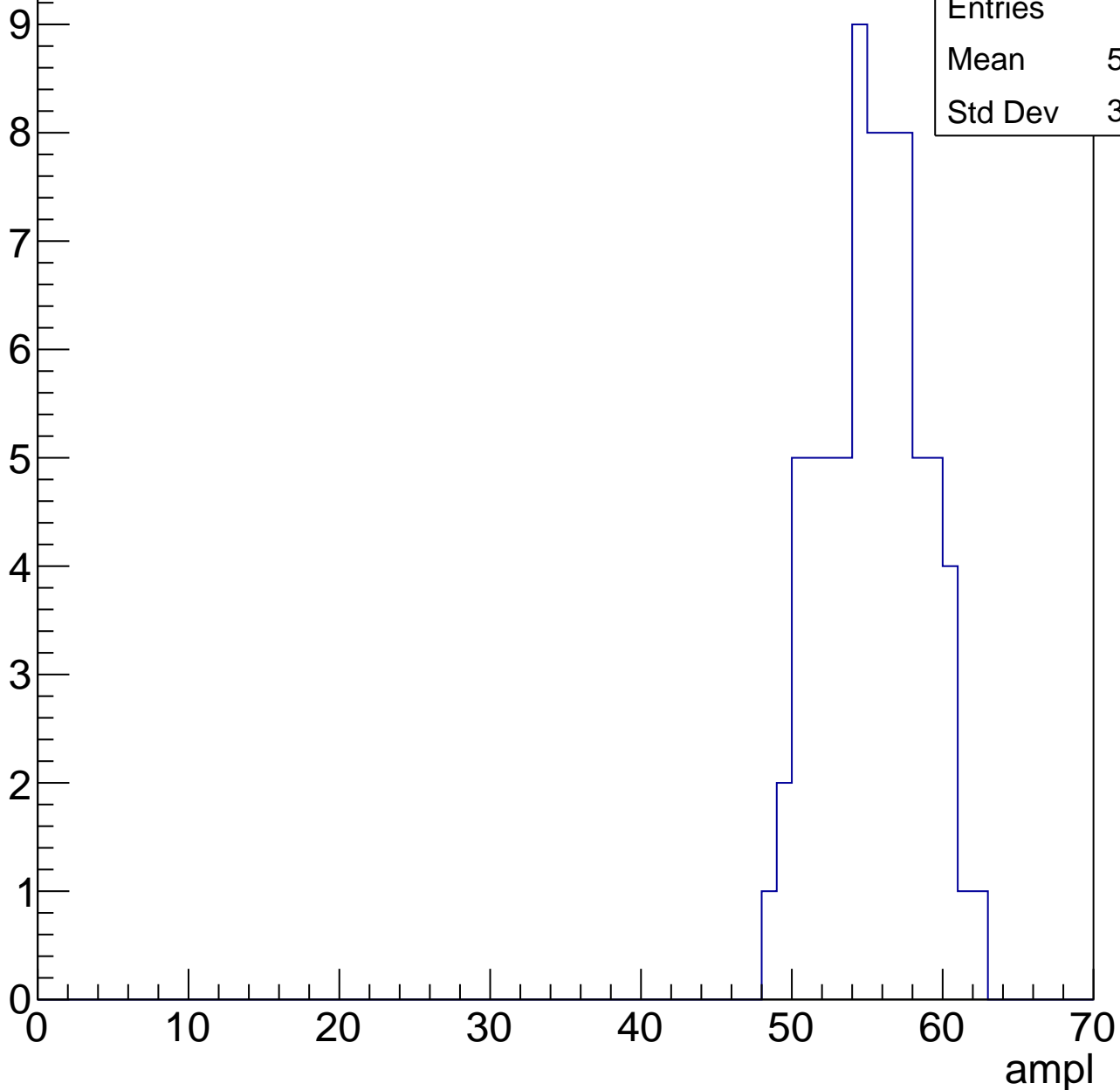
Entries	64
Mean	48.64
Std Dev	4.083



# B1L102S, U12-ch63, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



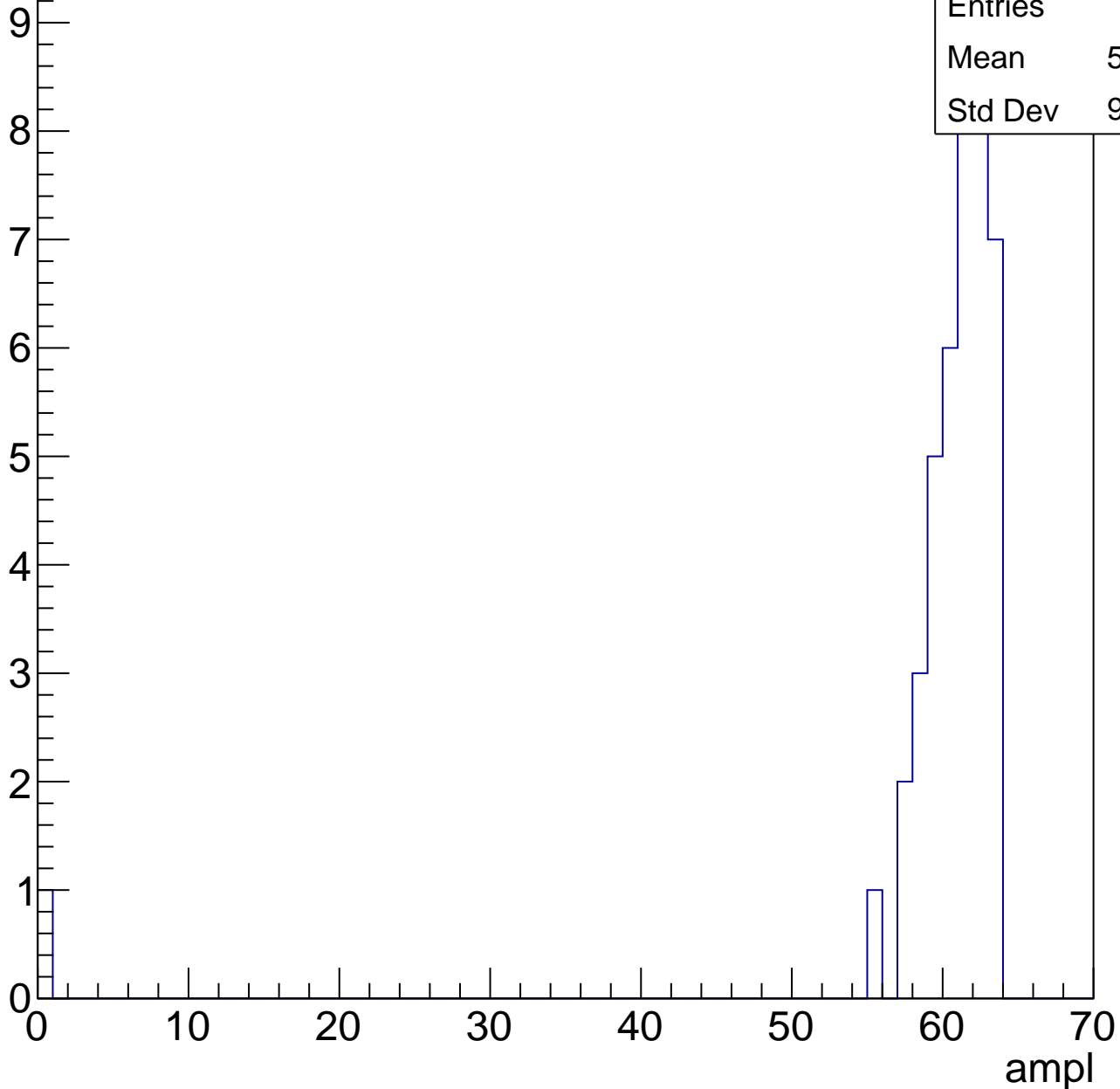
Entries	72
Mean	54.92
Std Dev	3.226

# B1L102S, U12-ch63, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	42
Mean	59.14
Std Dev	9.428



# B1L102S, U12-ch63, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	3
Mean	62.67
Std Dev	0.4714

ampl

0 10 20 30 40 50 60 70



# B1L102S, U12-ch63, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U12-ch64, adc0

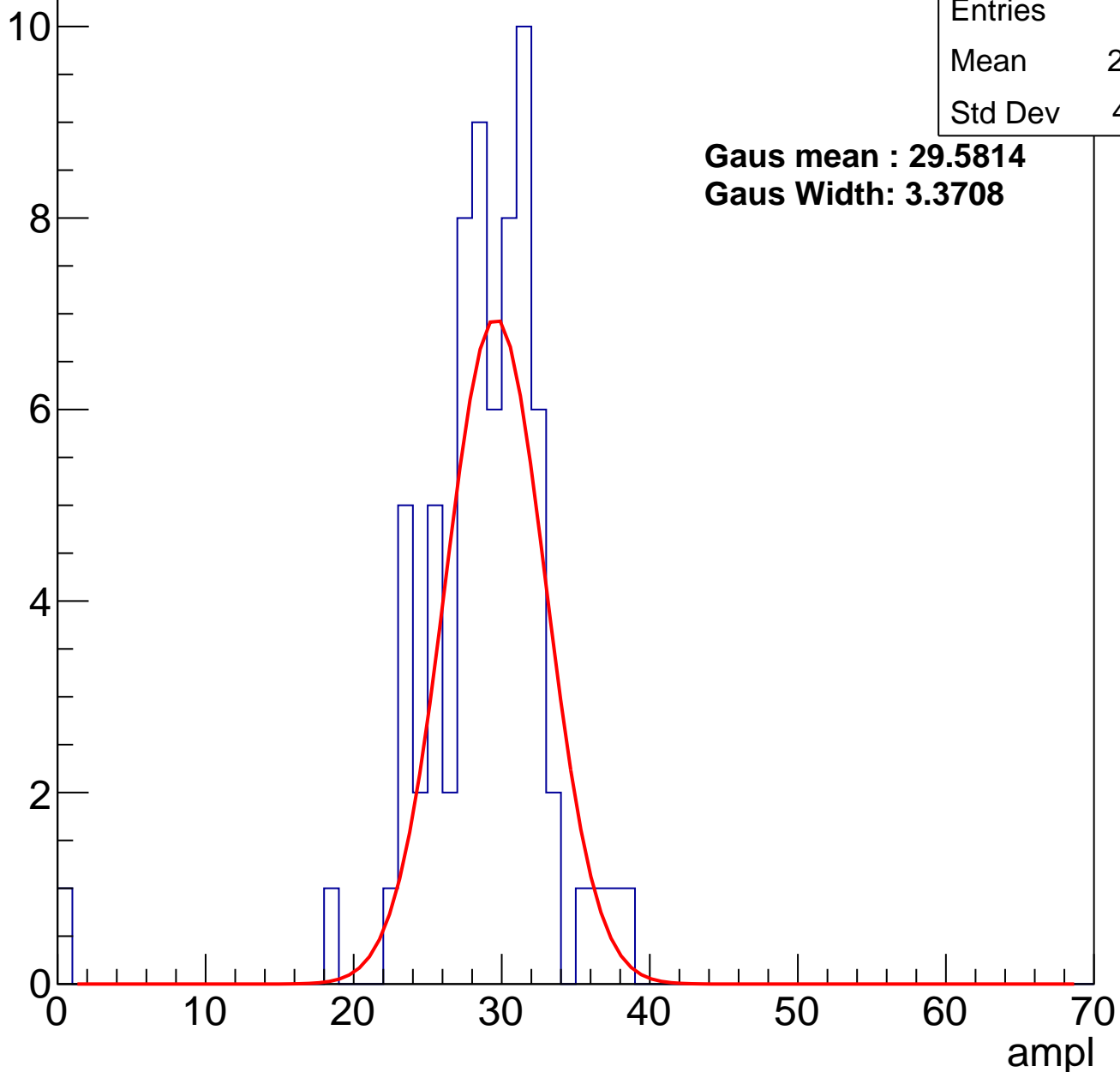
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	70
Mean	28.23
Std Dev	4.931

**Gaus mean : 29.5814**

**Gaus Width: 3.3708**

Entry



# B1L102S, U12-ch64, adc1

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	86
Mean	36.98
Std Dev	3.231

**Gaus mean : 36.7919**

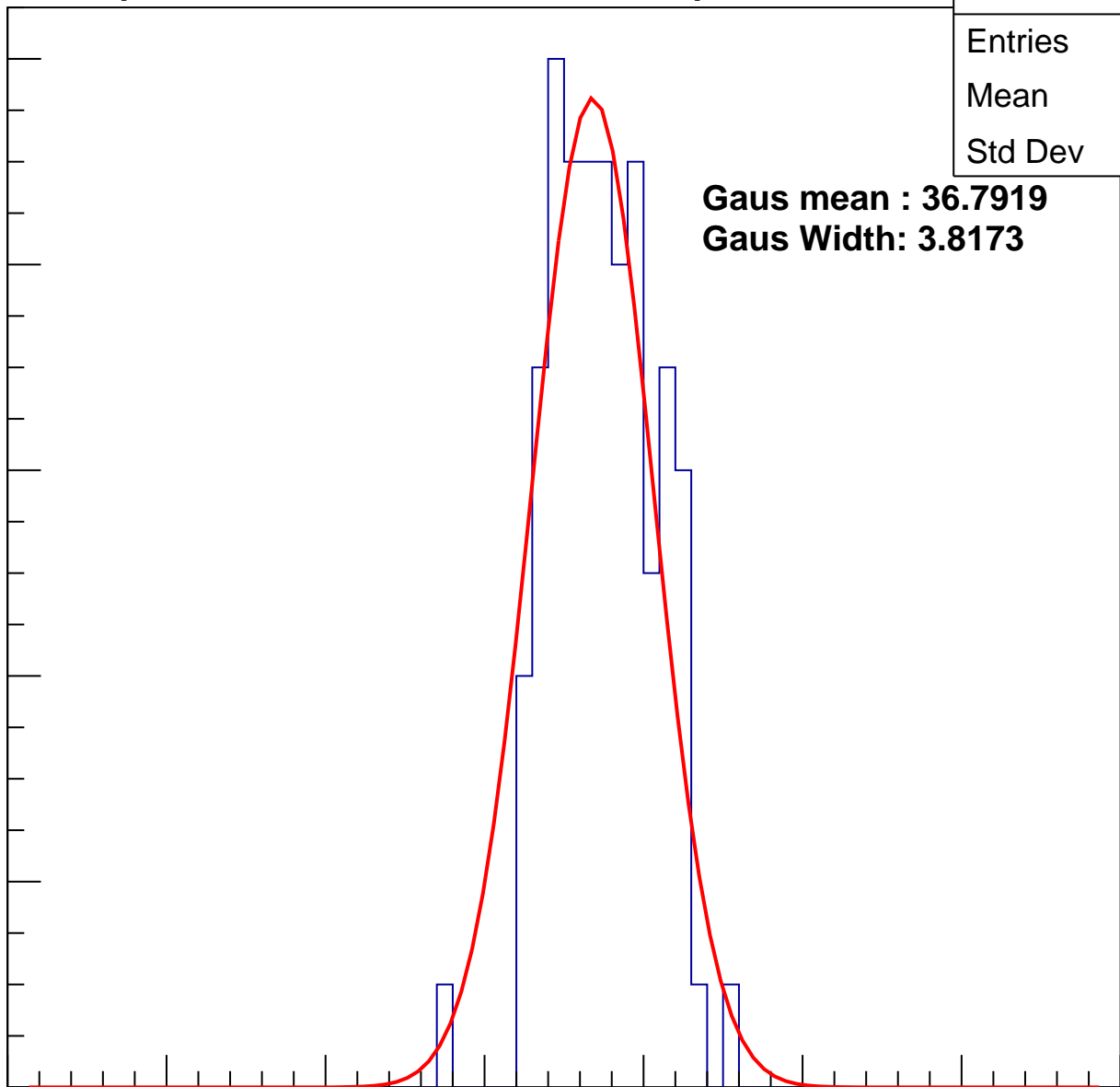
**Gaus Width: 3.8173**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L102S, U12-ch64, adc2

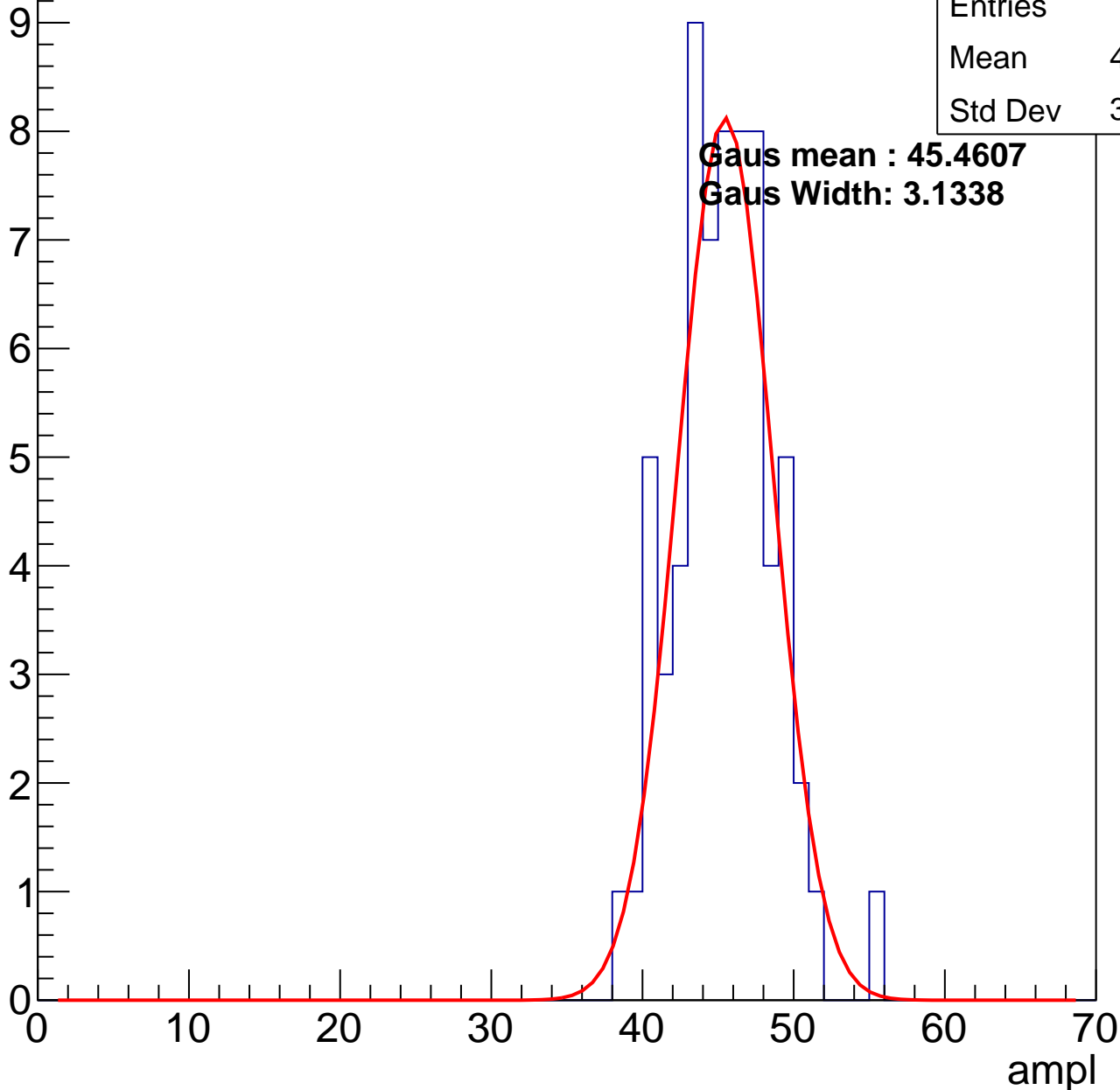
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	67
Mean	44.93
Std Dev	3.183

**Gaus mean : 45.4607**

**Gaus Width: 3.1338**

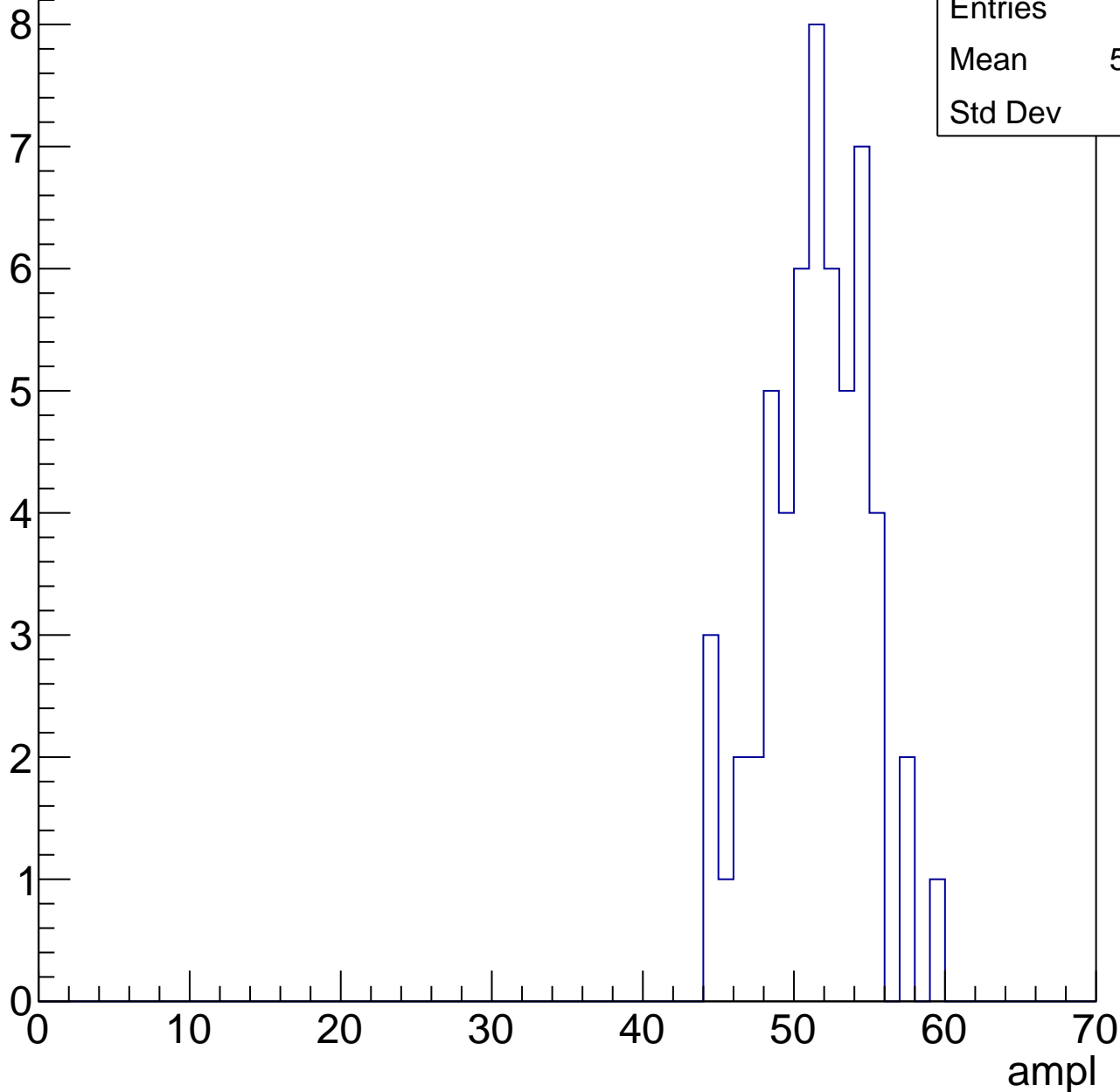


# B1L102S, U12-ch64, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	56
Mean	50.98
Std Dev	3.33

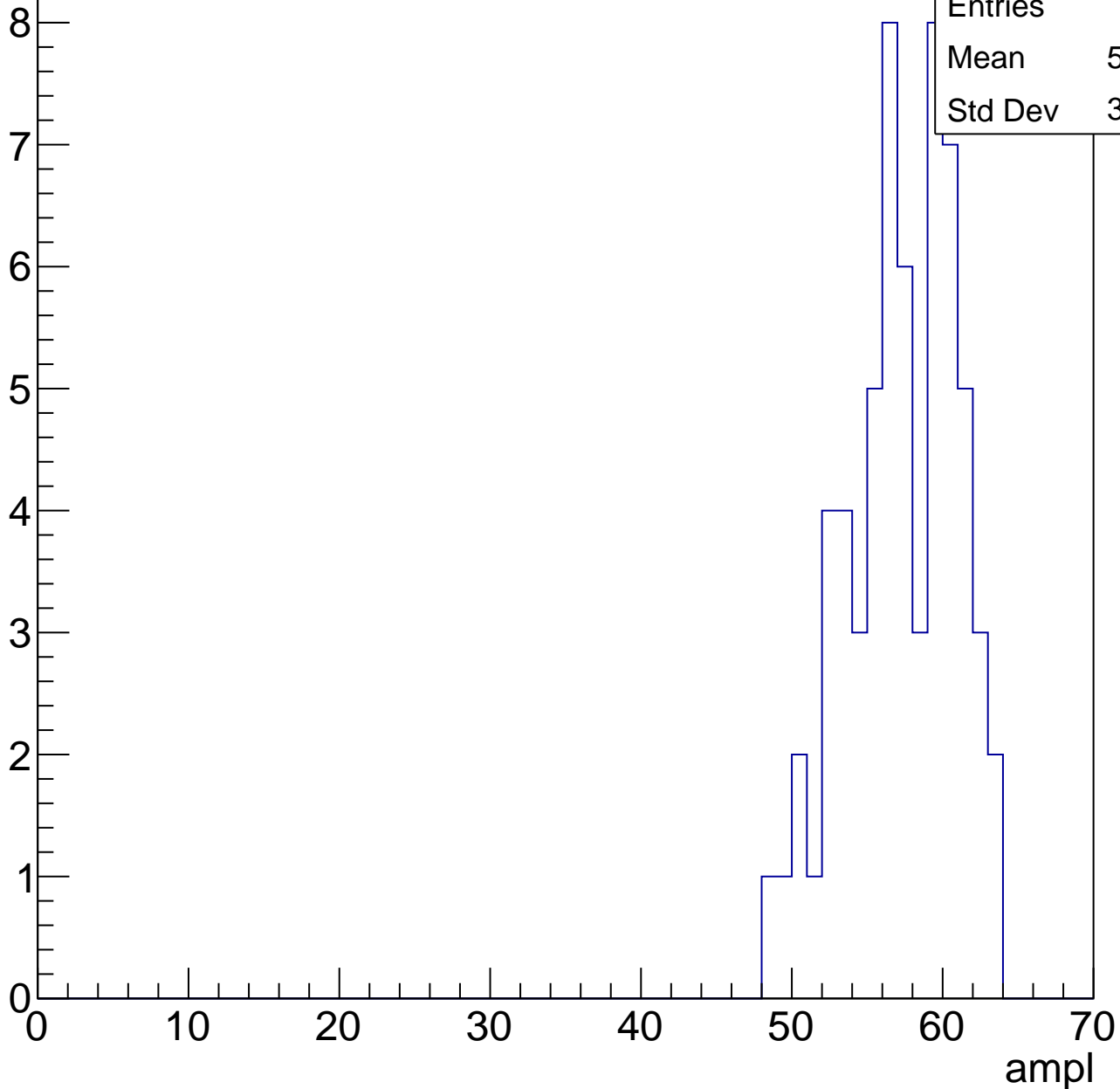


# B1L102S, U12-ch64, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	63
Mean	56.79
Std Dev	3.608

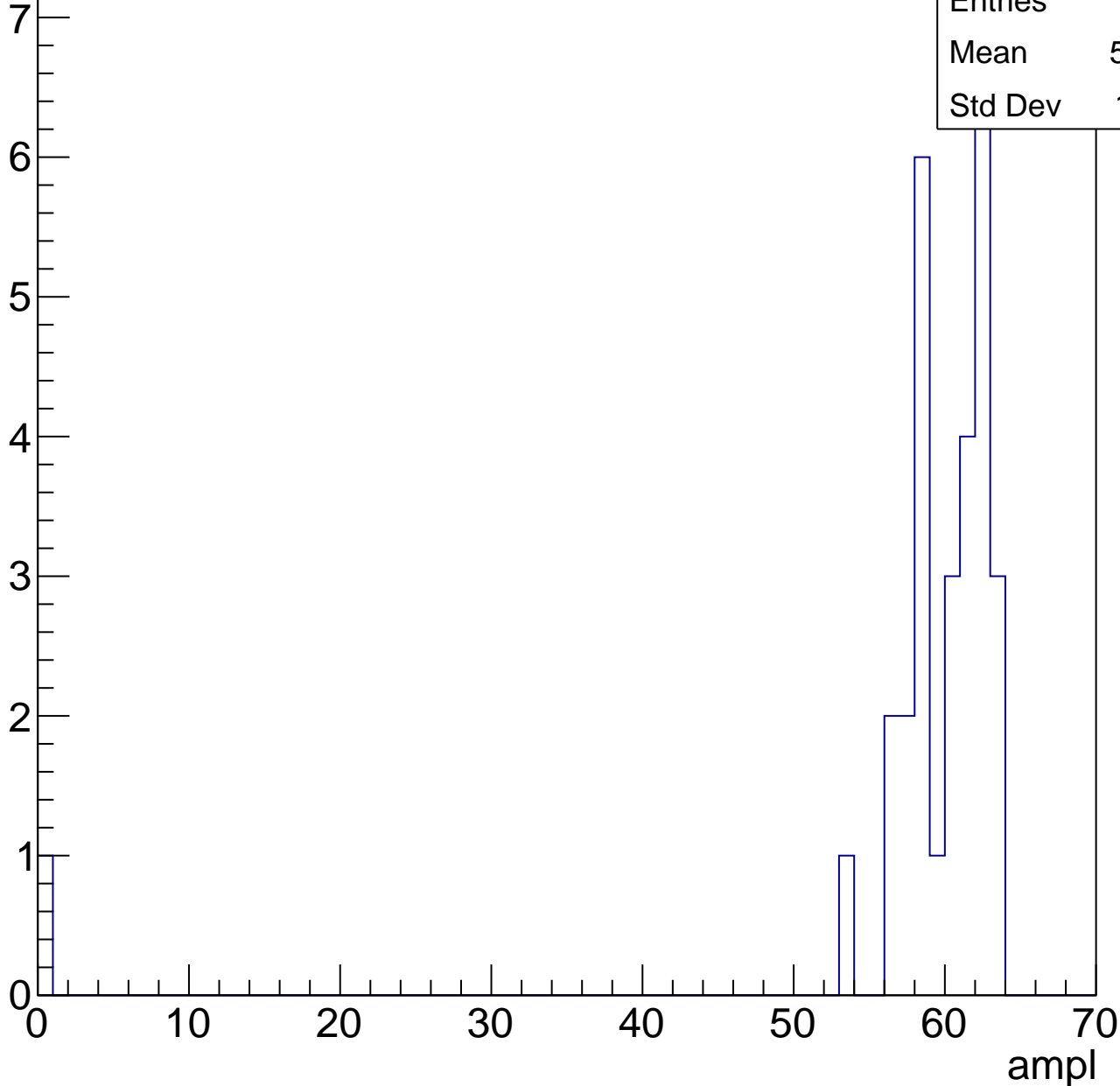


# B1L102S, U12-ch64, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

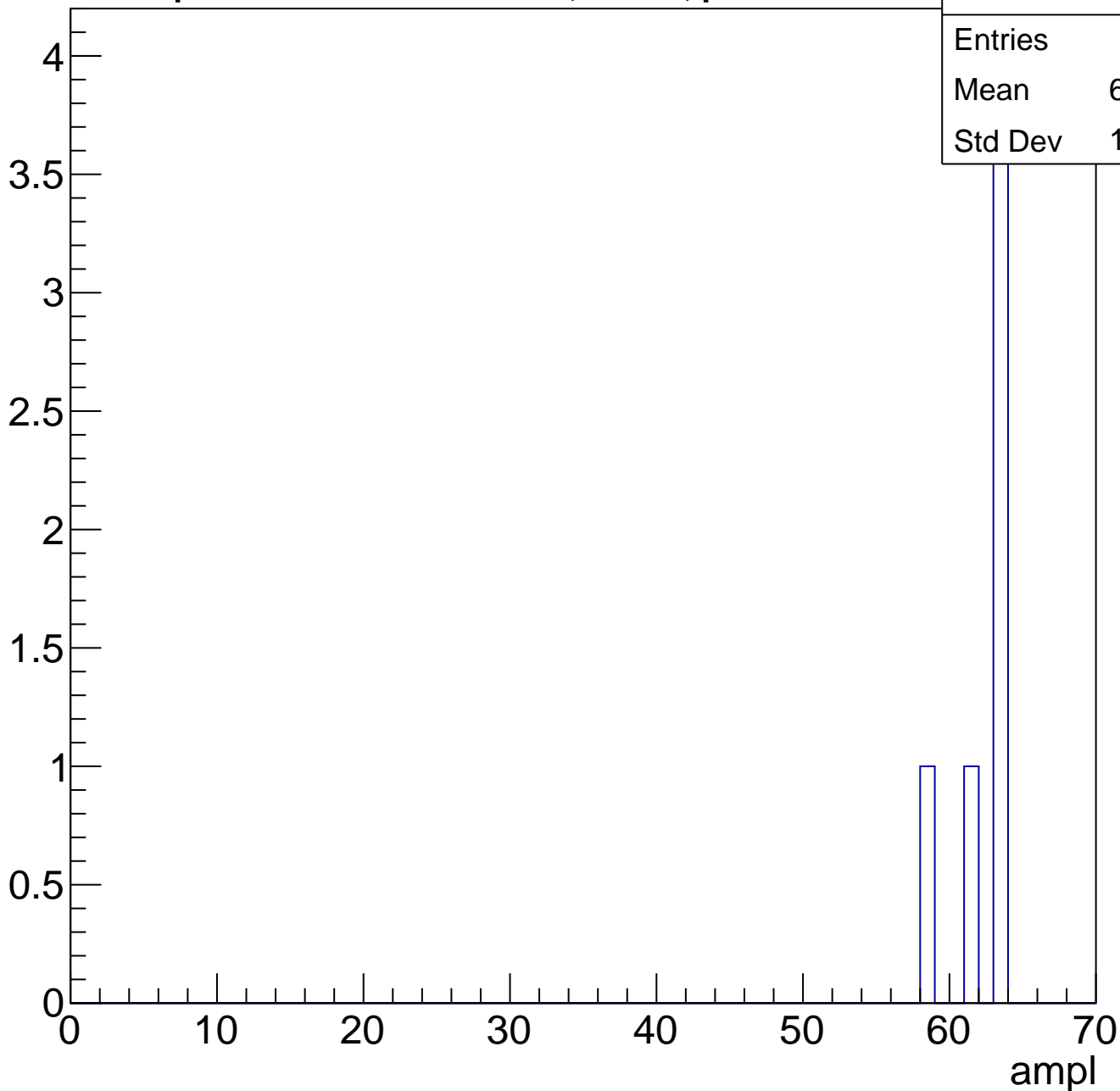
Entries	30
Mean	57.77
Std Dev	11.01



# B1L102S, U12-ch64, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U12-ch64, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U12-ch65, adc0

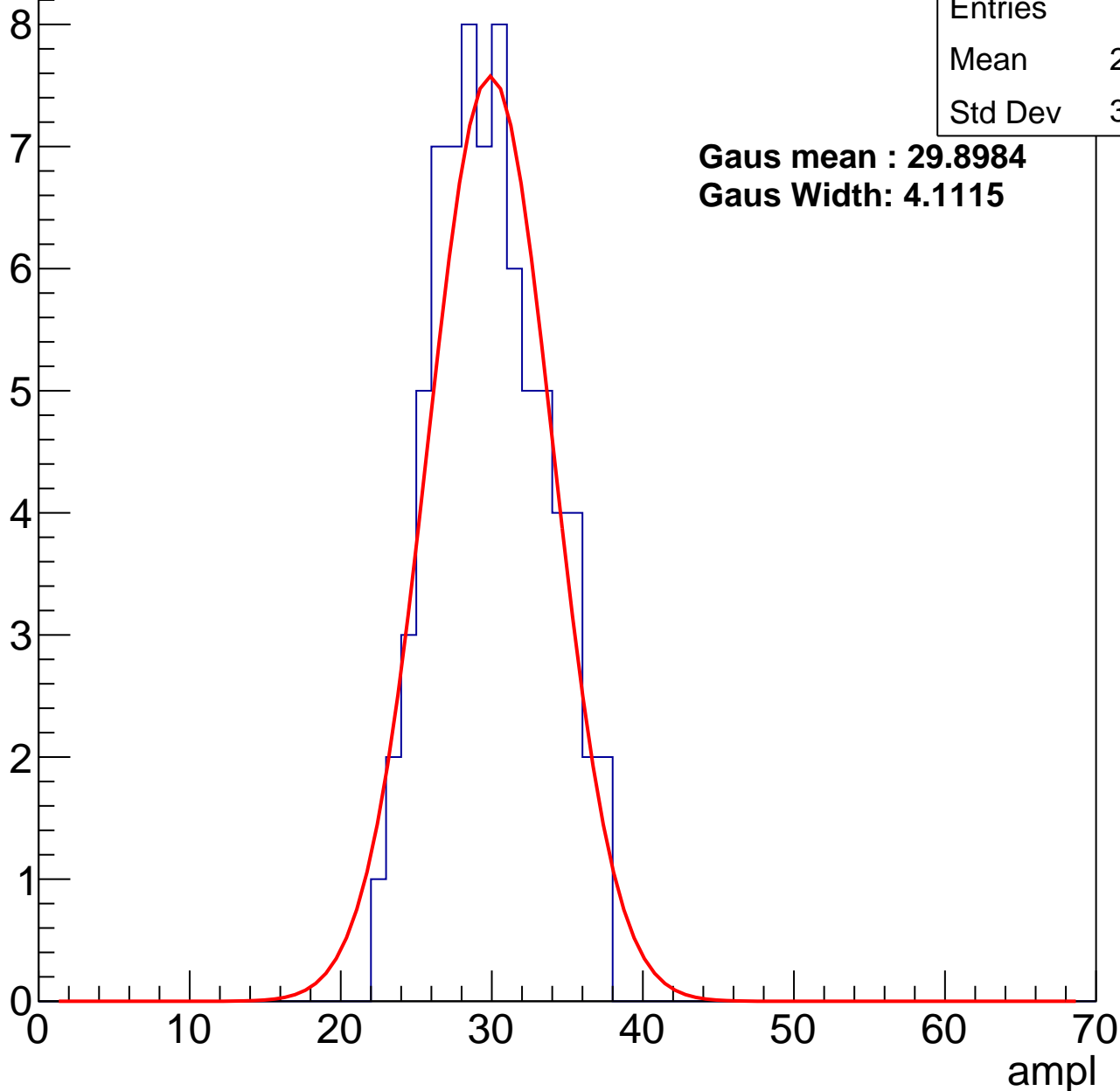
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	76
Mean	29.42
Std Dev	3.607

**Gaus mean : 29.8984**

**Gaus Width: 4.1115**



# B1L102S, U12-ch65, adc1

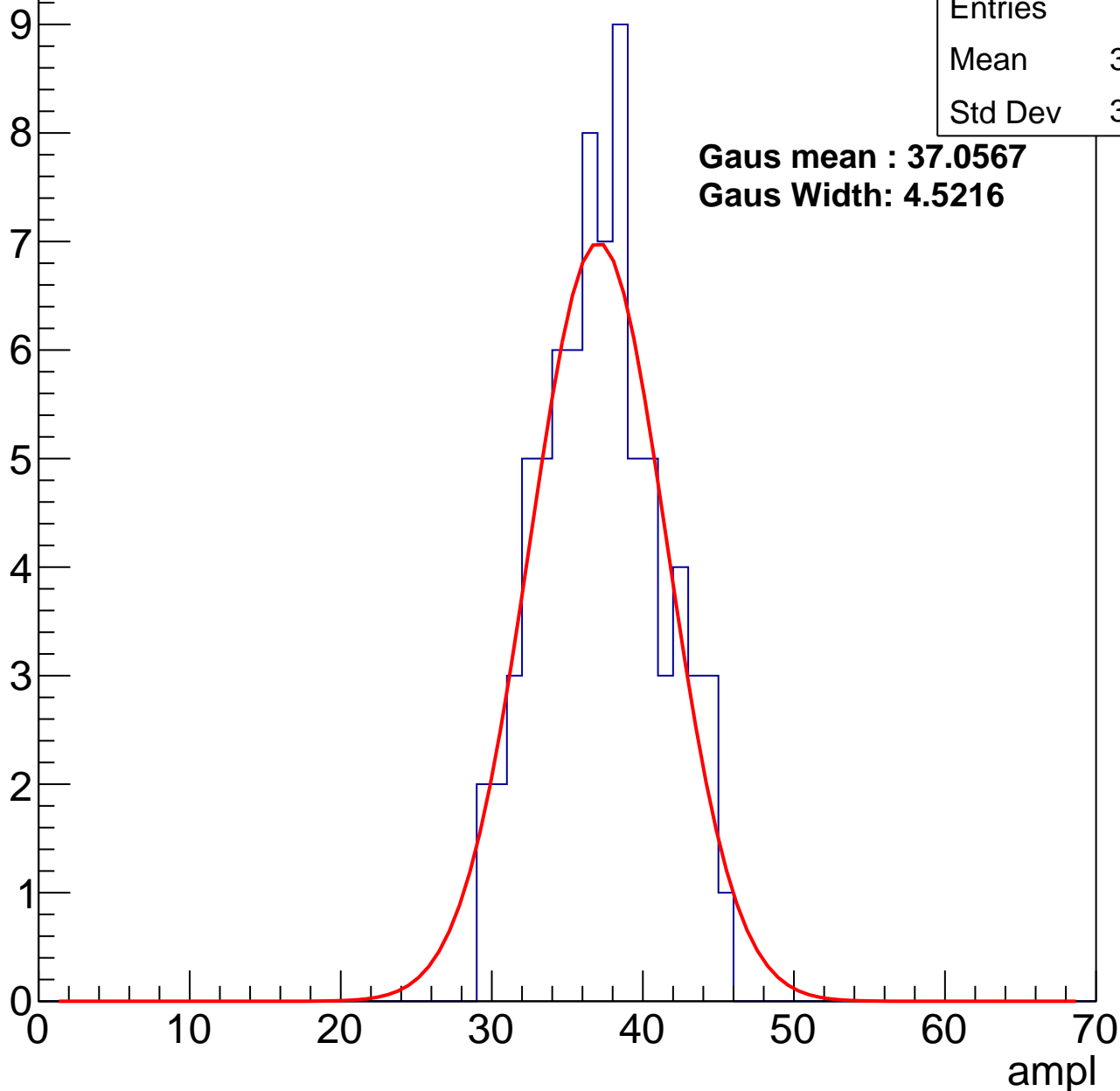
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	77
Mean	36.77
Std Dev	3.884

**Gaus mean : 37.0567**

**Gaus Width: 4.5216**



# B1L102S, U12-ch65, adc2

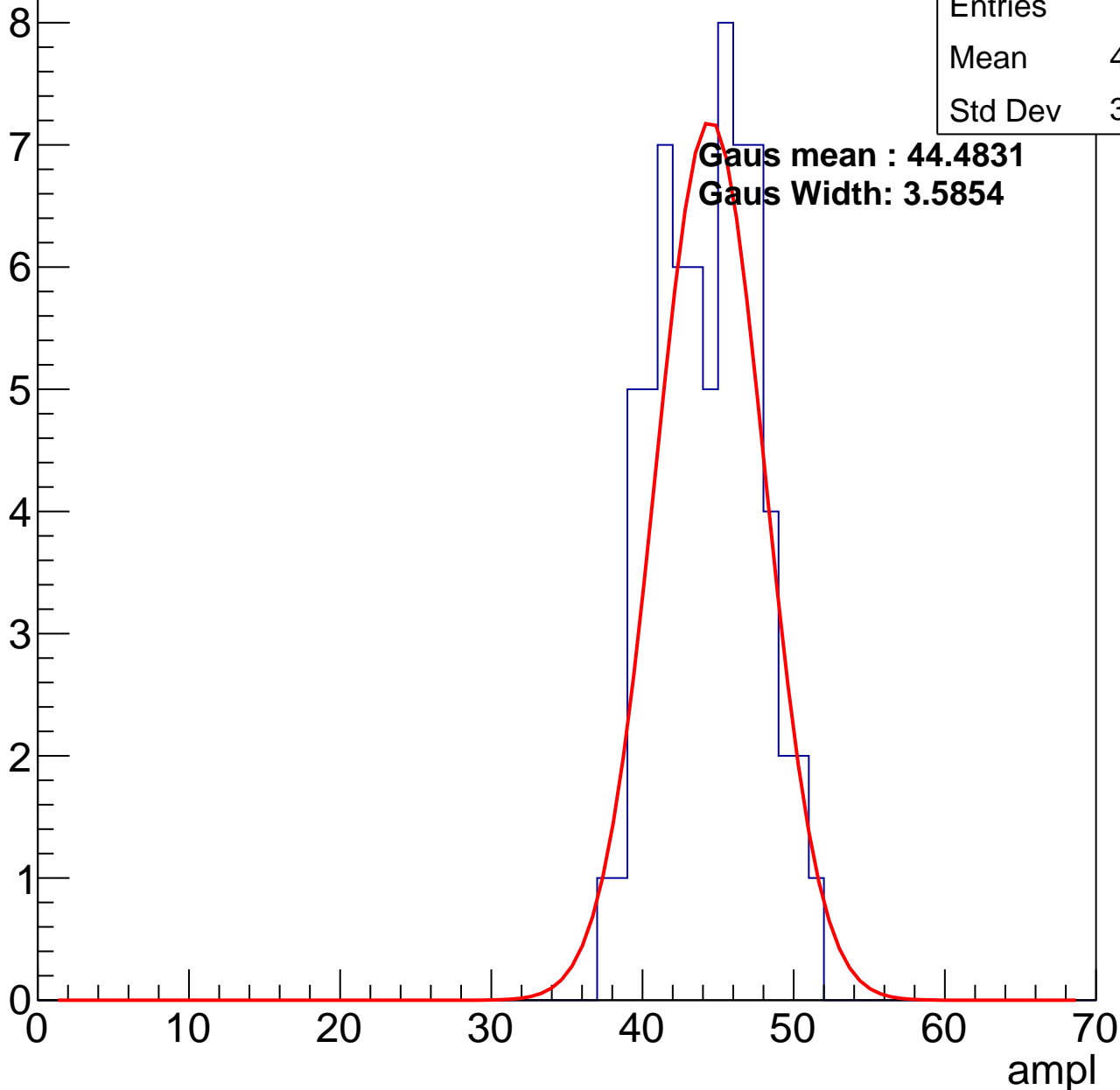
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	67
Mean	43.87
Std Dev	3.269

**Gaus mean : 44.4831**

**Gaus Width: 3.5854**

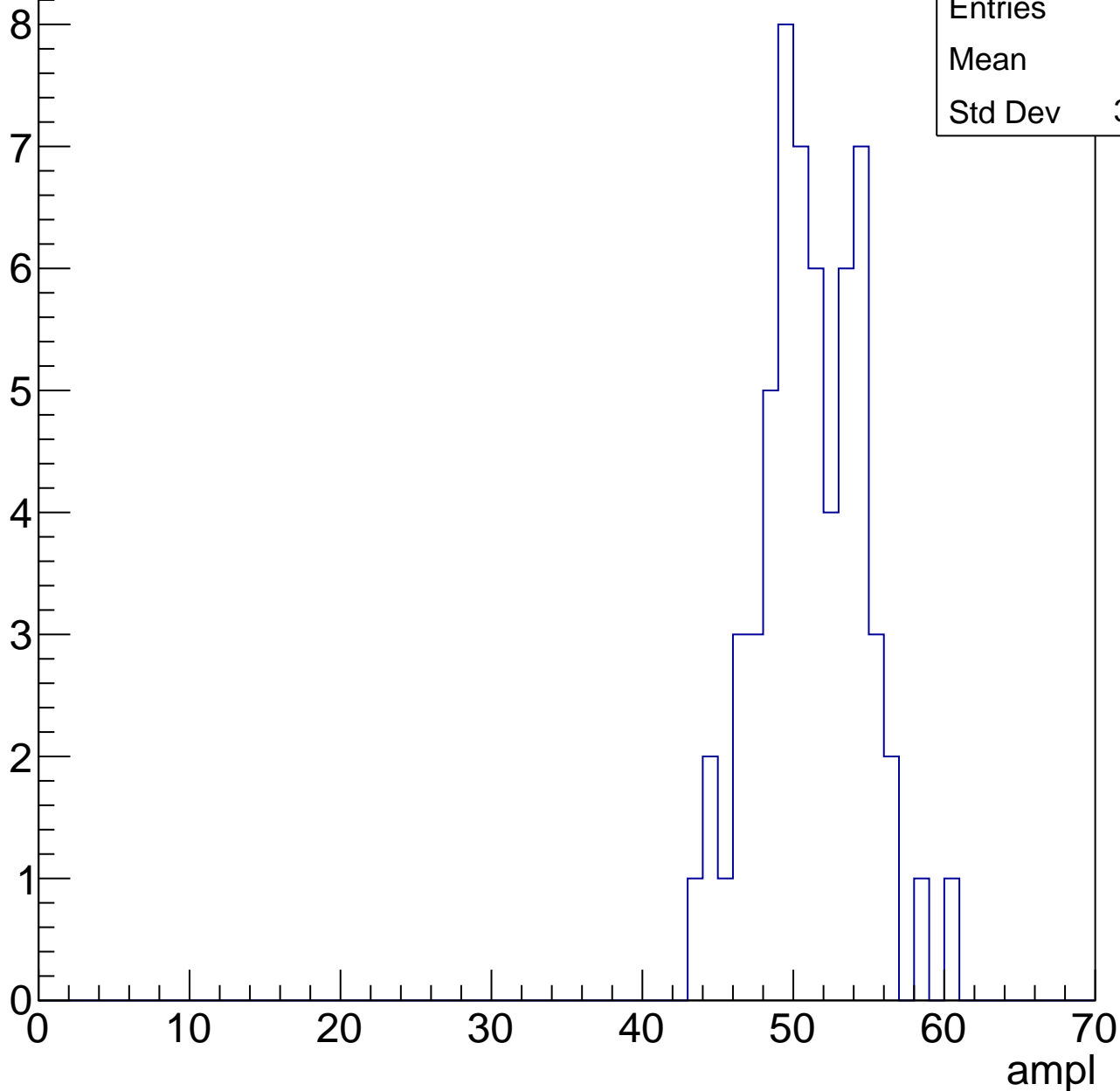


# B1L102S, U12-ch65, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	60
Mean	50.7
Std Dev	3.461

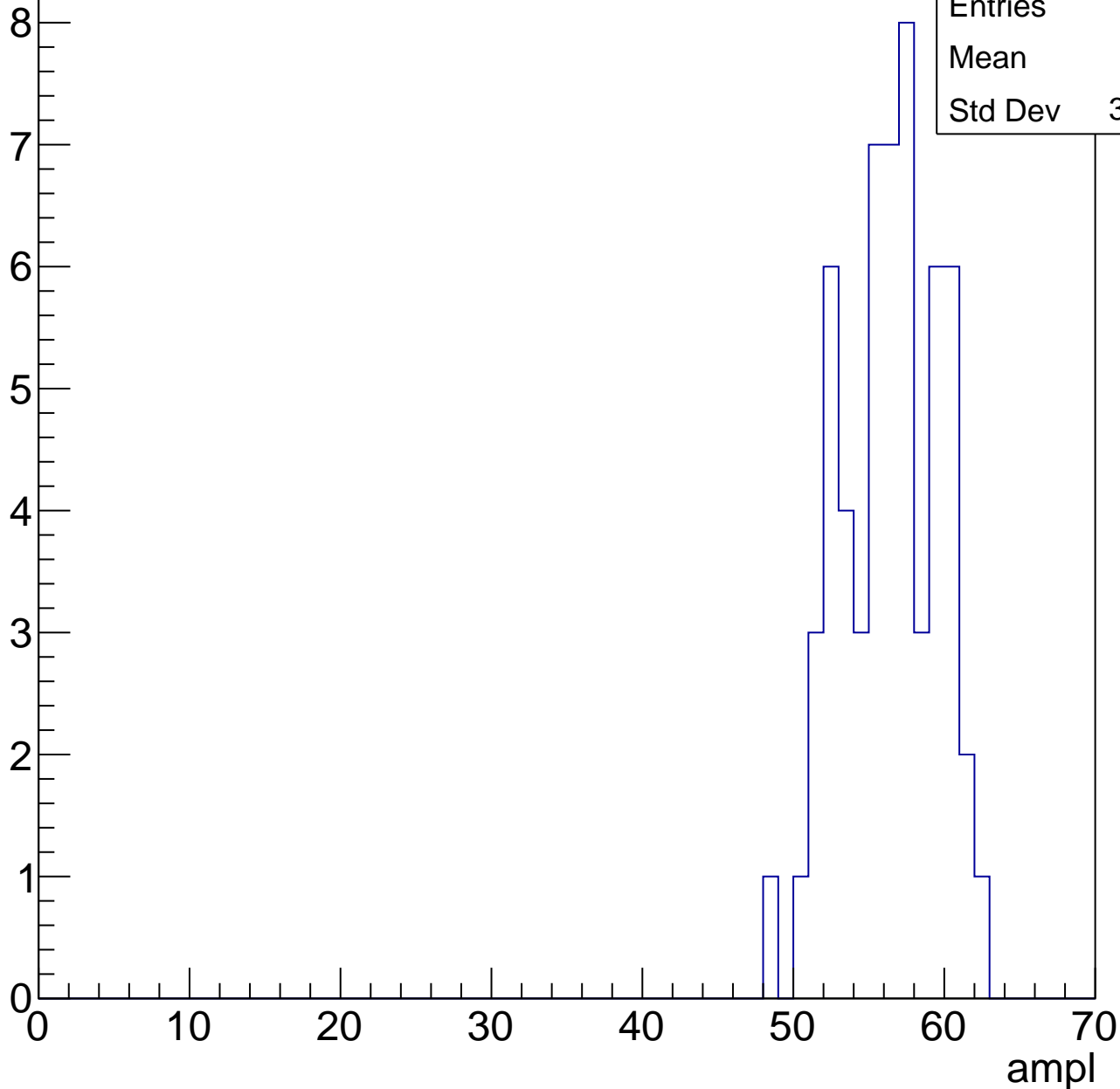


# B1L102S, U12-ch65, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	58
Mean	55.9
Std Dev	3.166

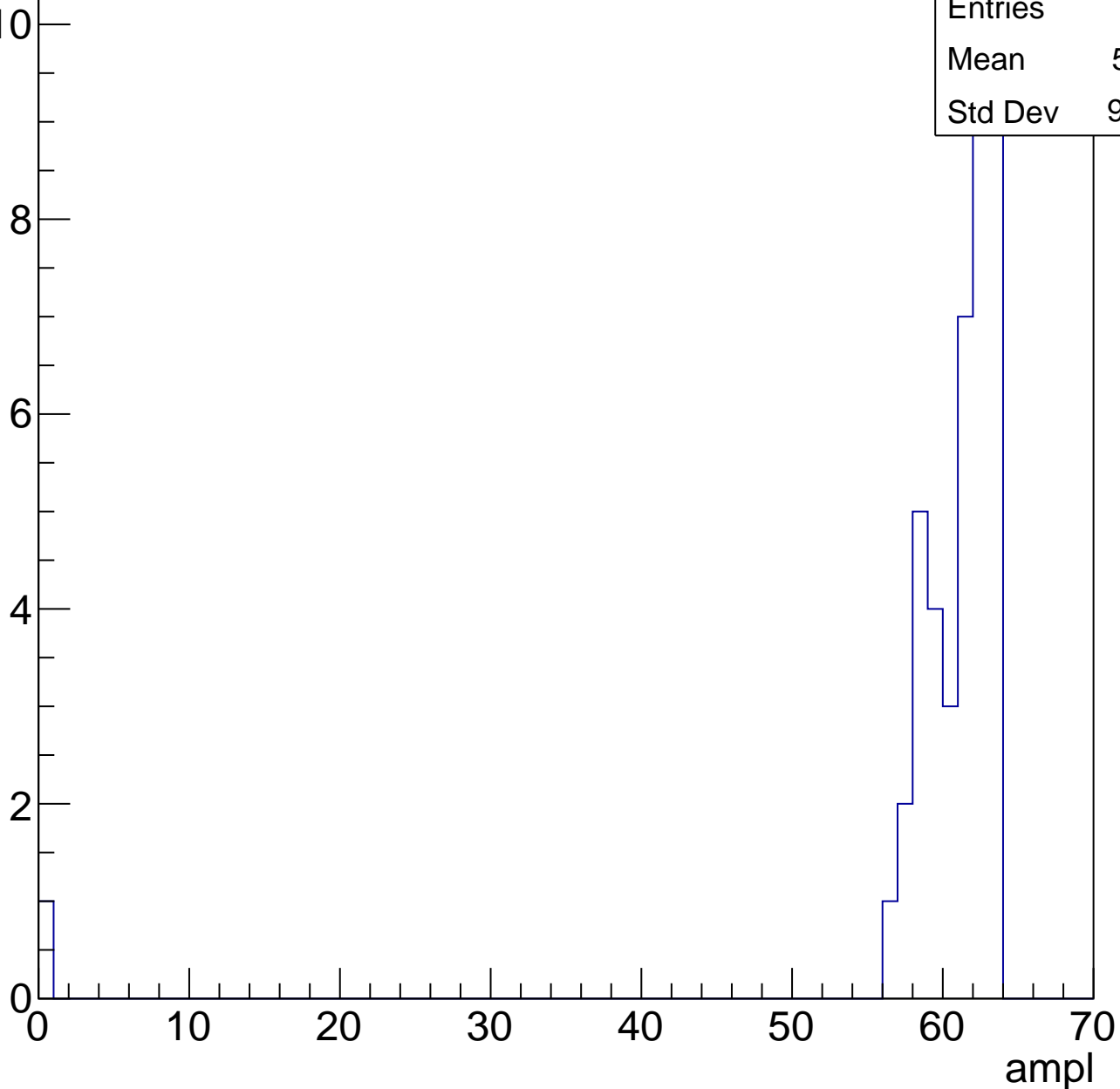


# B1L102S, U12-ch65, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

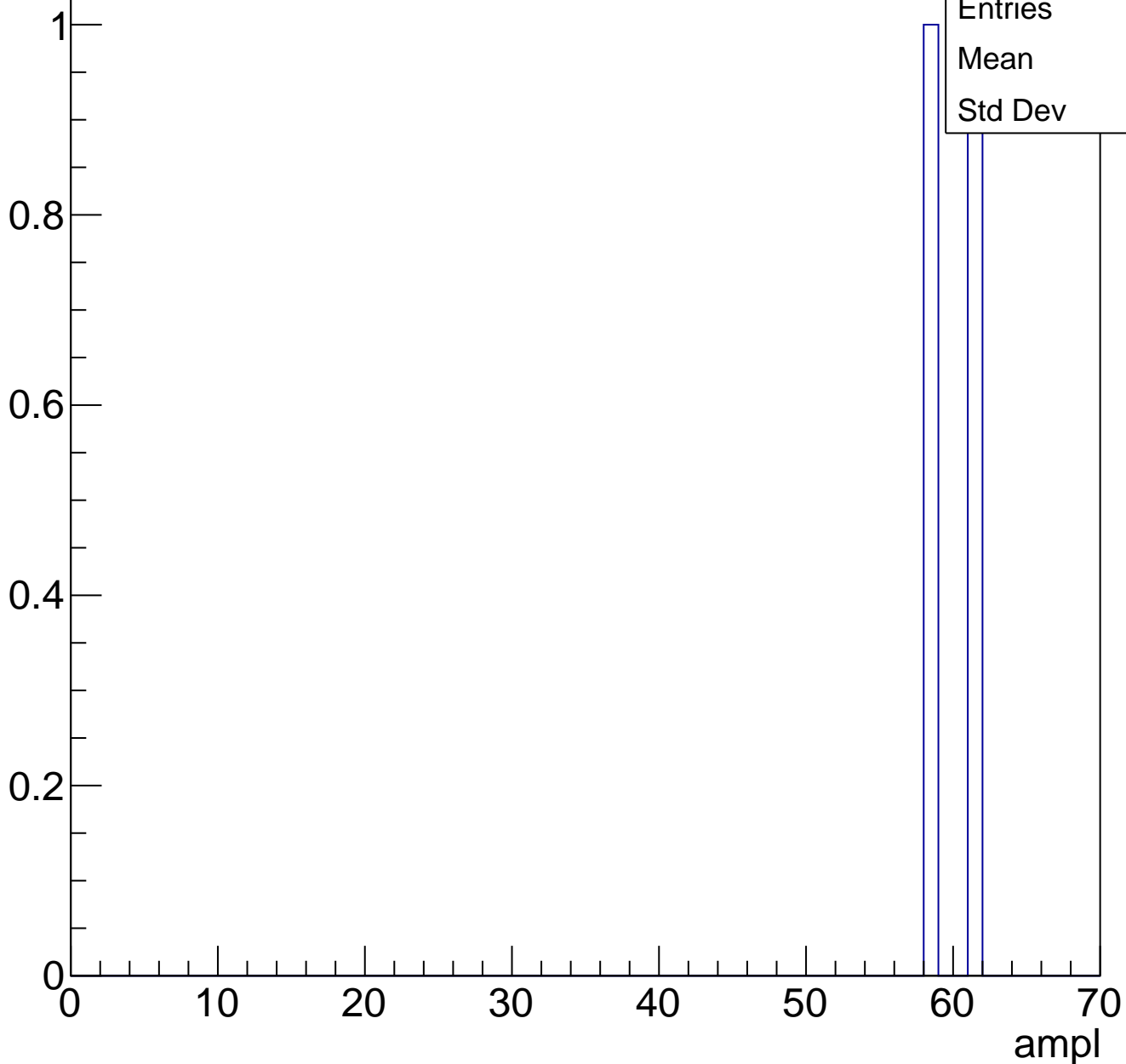
Entries	42
Mean	59.31
Std Dev	9.476



# B1L102S, U12-ch65, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U12-ch65, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U12-ch66, adc0

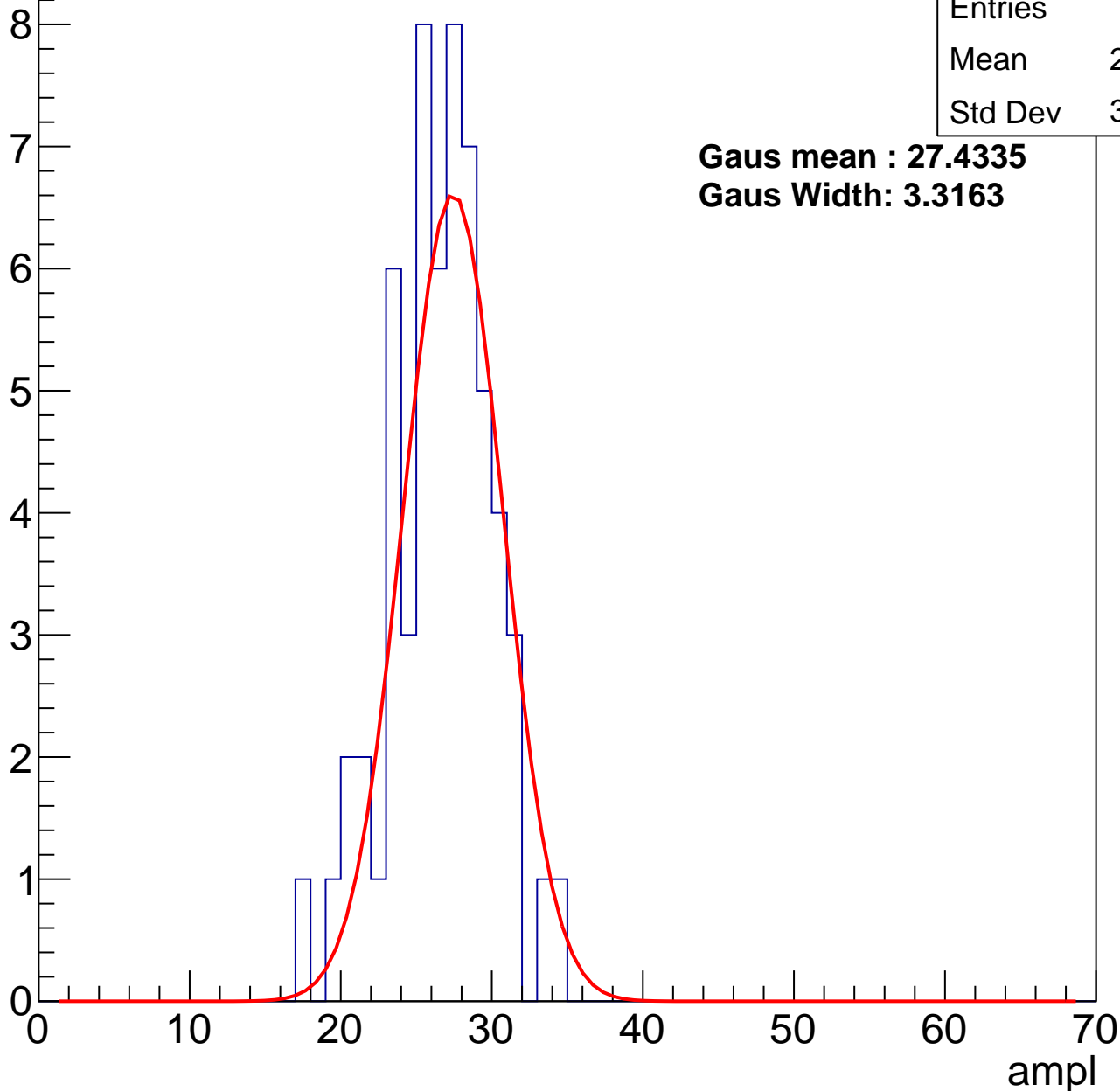
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	59
Mean	26.15
Std Dev	3.379

**Gaus mean : 27.4335**

**Gaus Width: 3.3163**



# B1L102S, U12-ch66, adc1

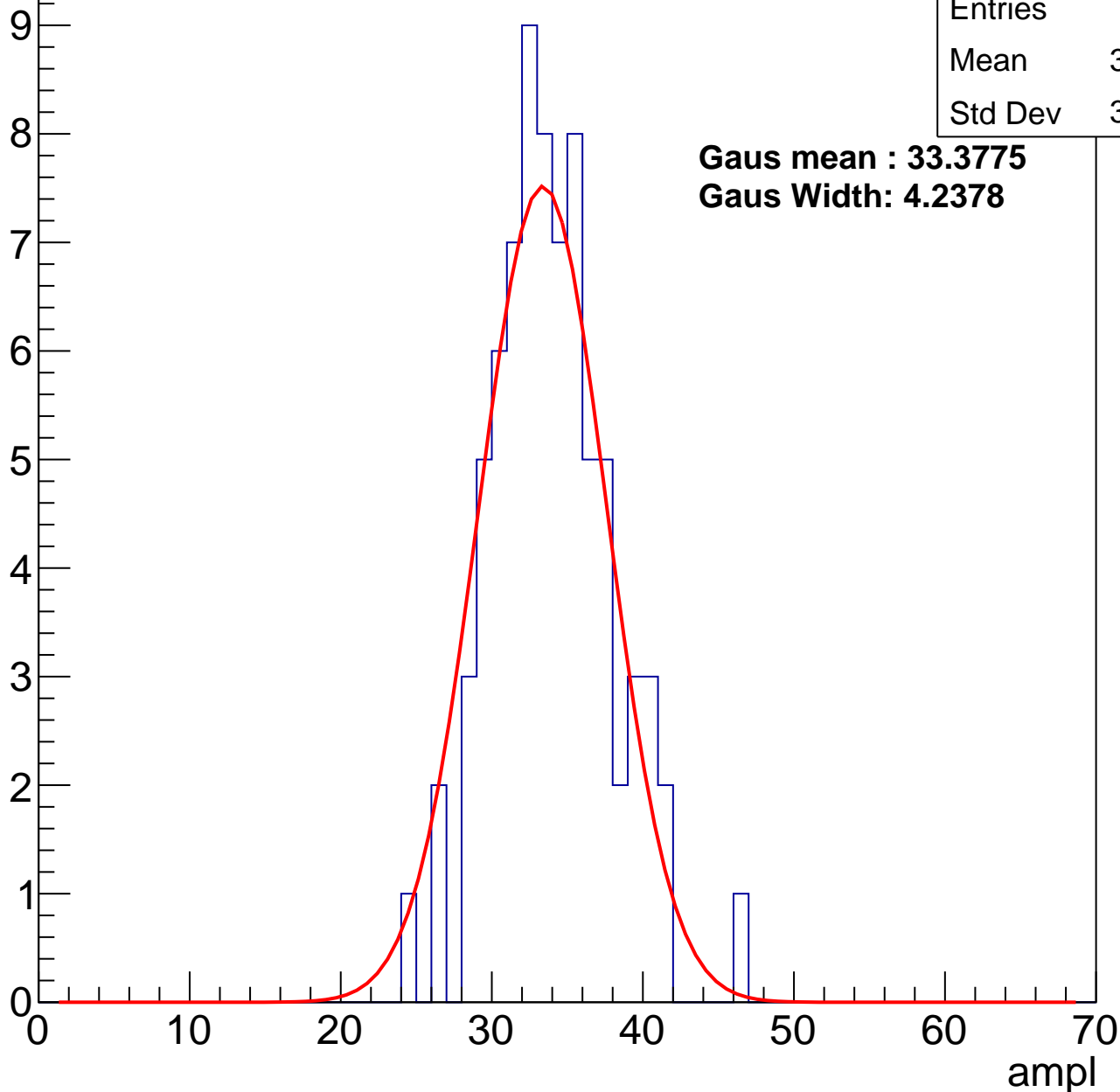
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	77
Mean	33.48
Std Dev	3.903

**Gaus mean : 33.3775**

**Gaus Width: 4.2378**



# B1L102S, U12-ch66, adc2

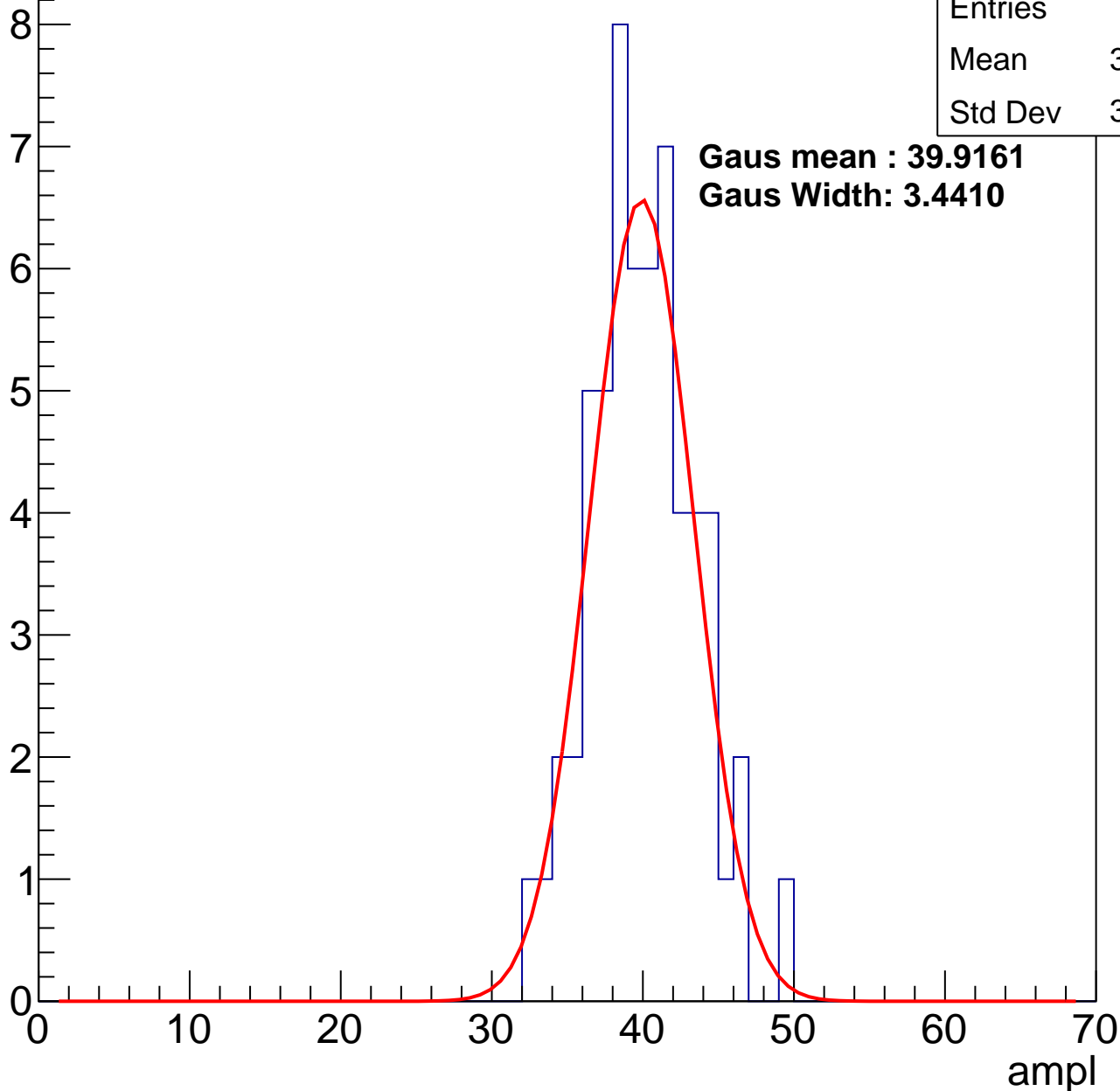
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	59
Mean	39.58
Std Dev	3.416

**Gaus mean : 39.9161**

**Gaus Width: 3.4410**

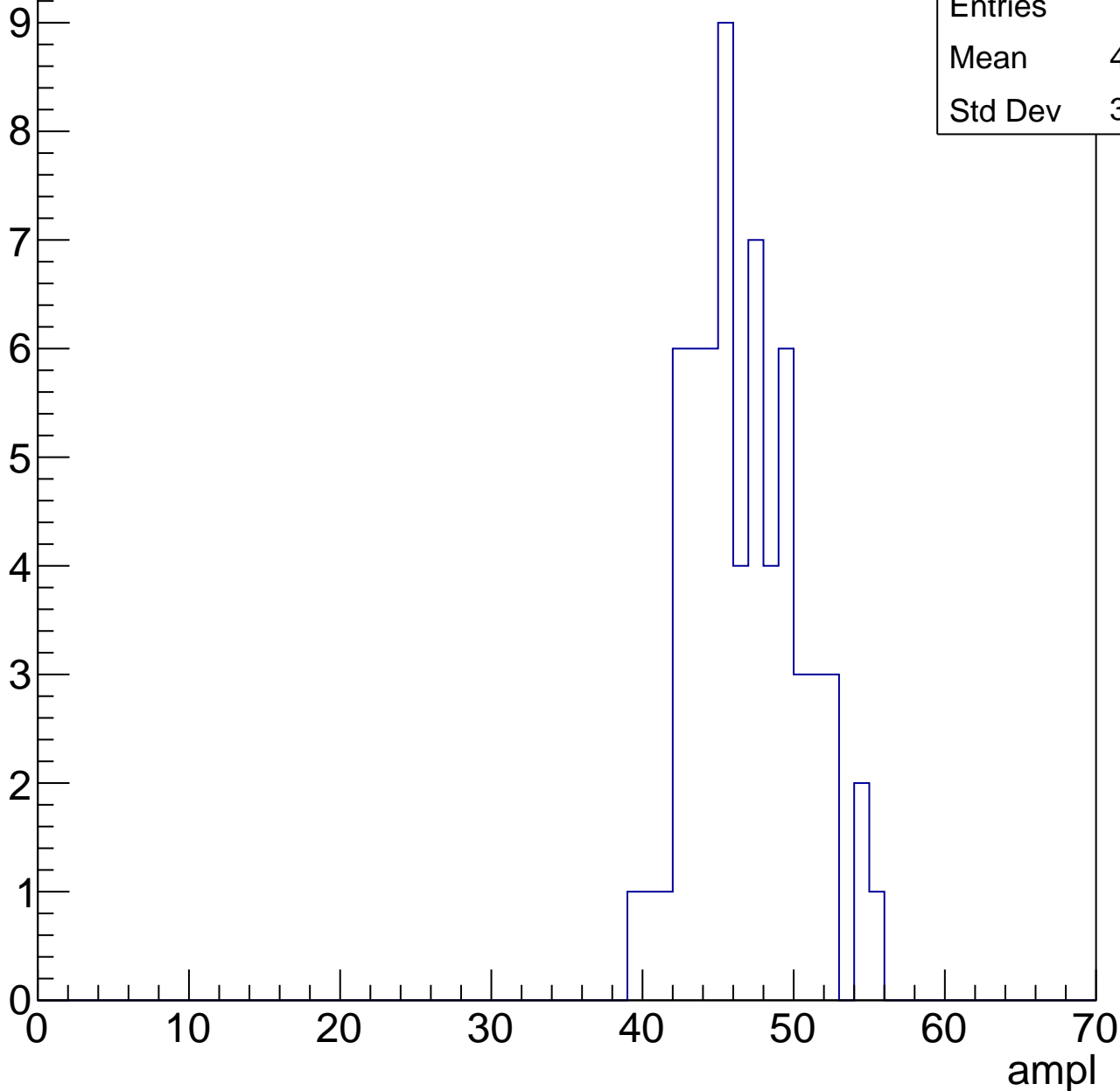


# B1L102S, U12-ch66, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	63
Mean	46.35
Std Dev	3.569

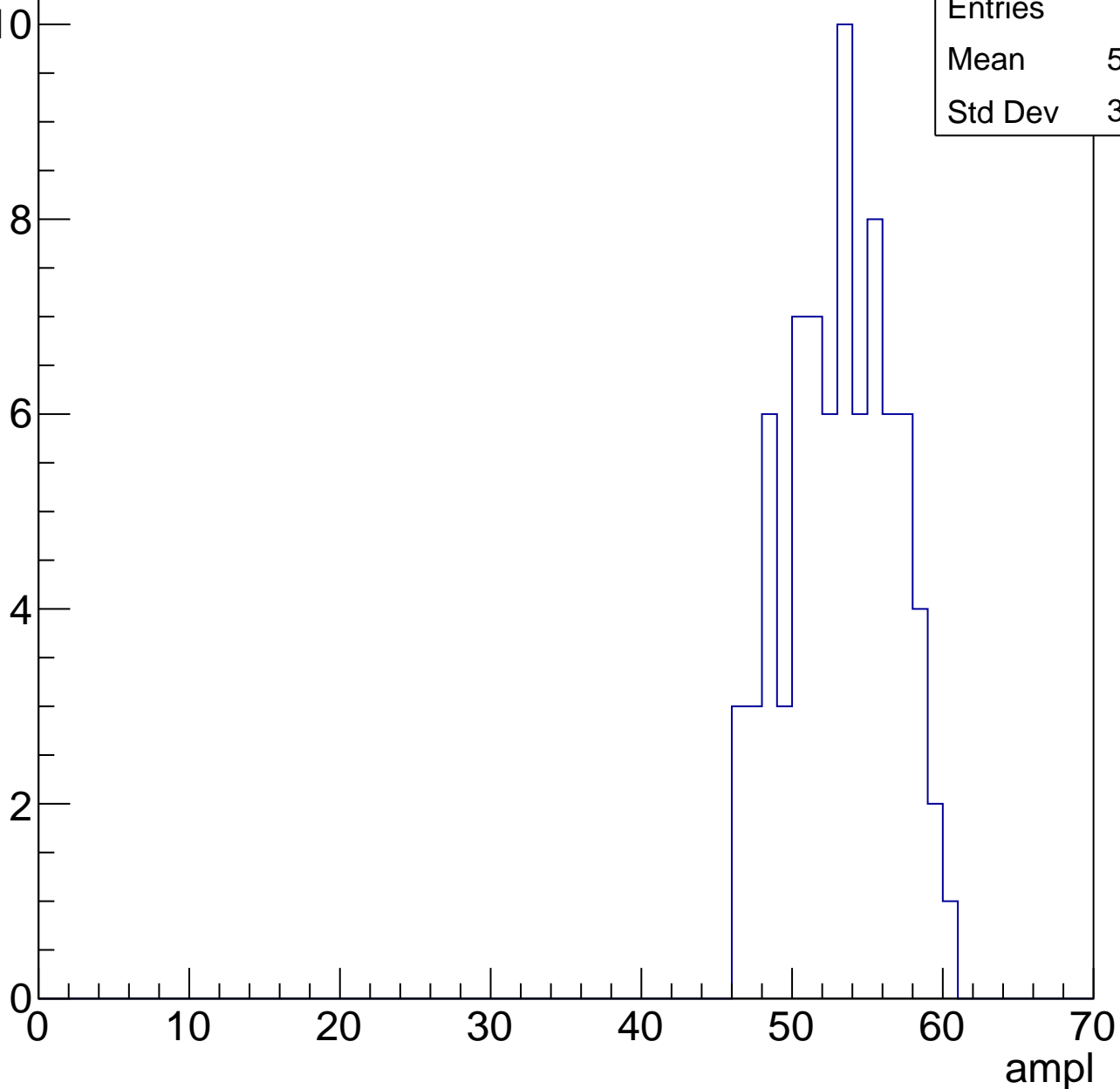


# B1L102S, U12-ch66, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	78
Mean	52.76
Std Dev	3.498

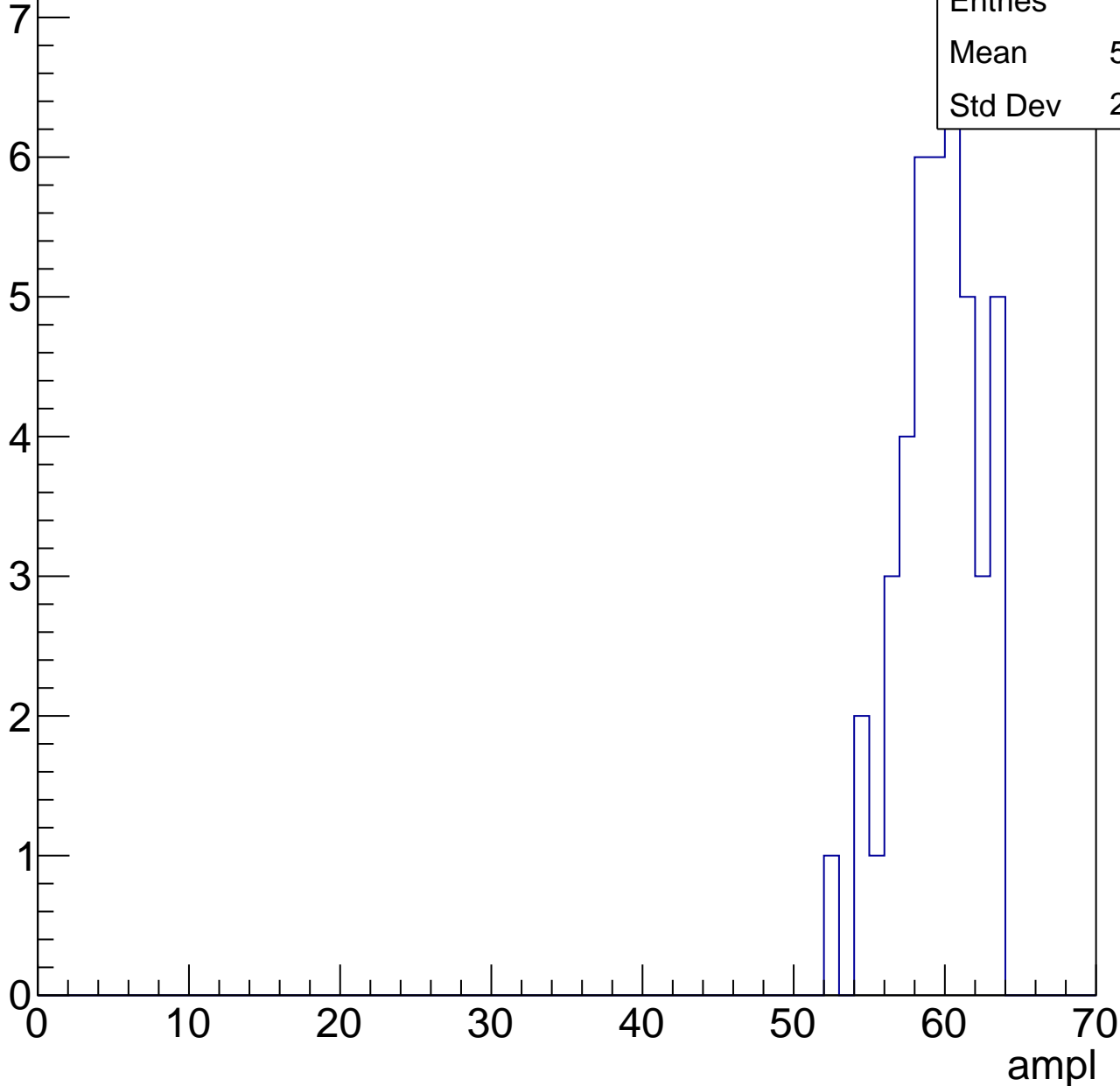


# B1L102S, U12-ch66, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	43
Mean	59.05
Std Dev	2.632

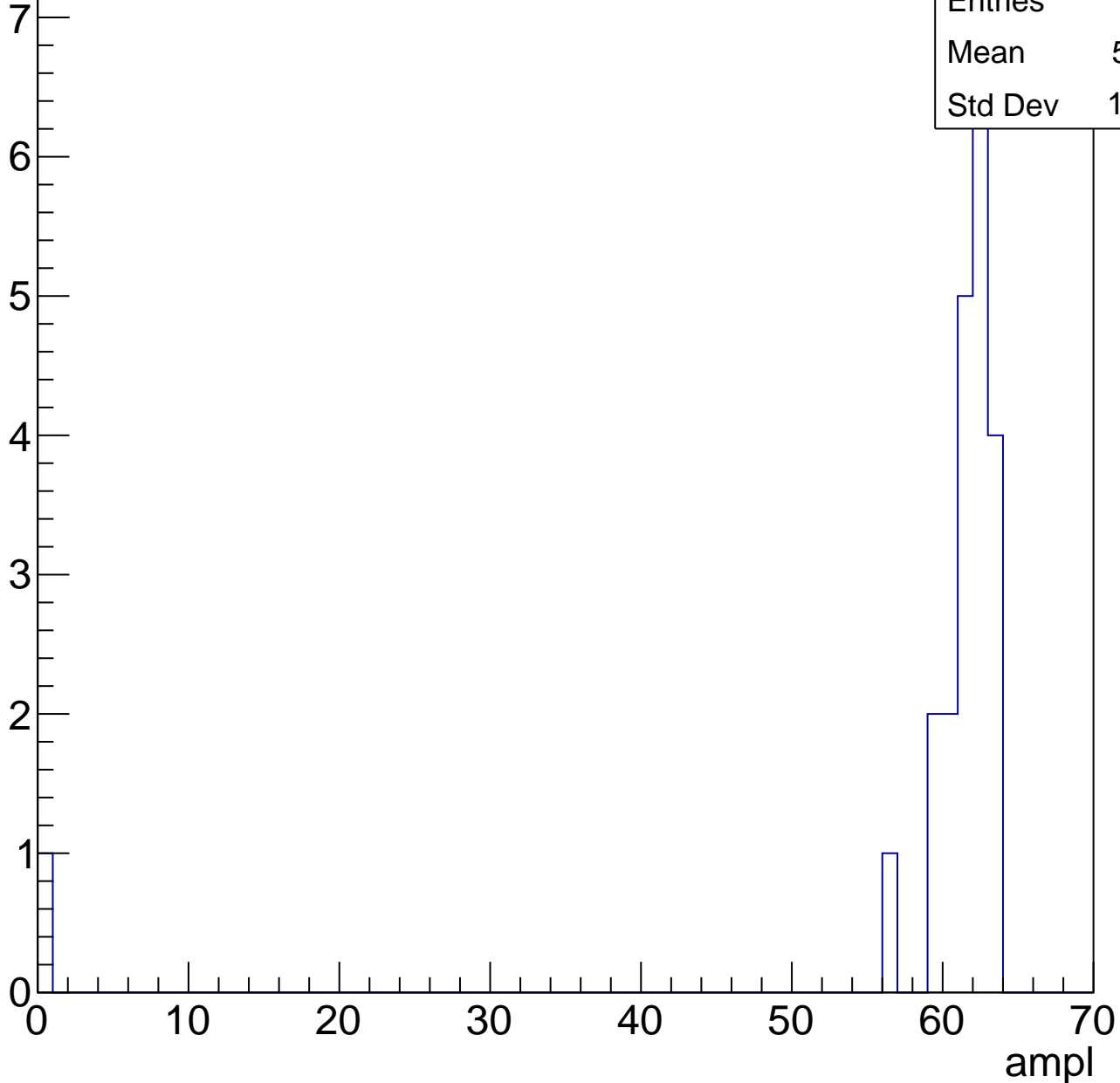


# B1L102S, U12-ch66, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	22
Mean	58.41
Std Dev	12.85





# B1L102S, U12-ch66, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U12-ch67, adc0

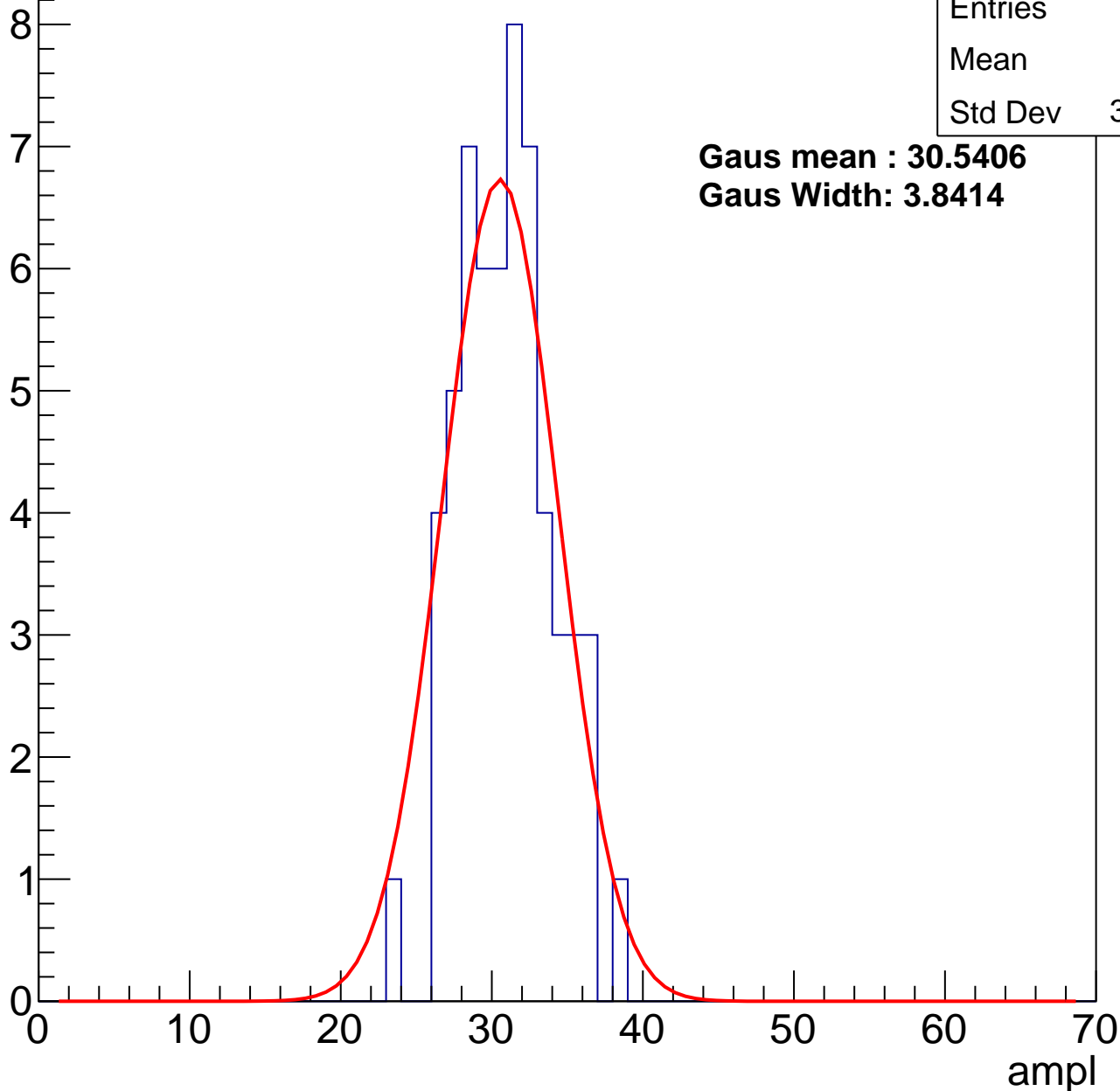
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	58
Mean	30.5
Std Dev	3.064

**Gaus mean : 30.5406**

**Gaus Width: 3.8414**



# B1L102S, U12-ch67, adc1

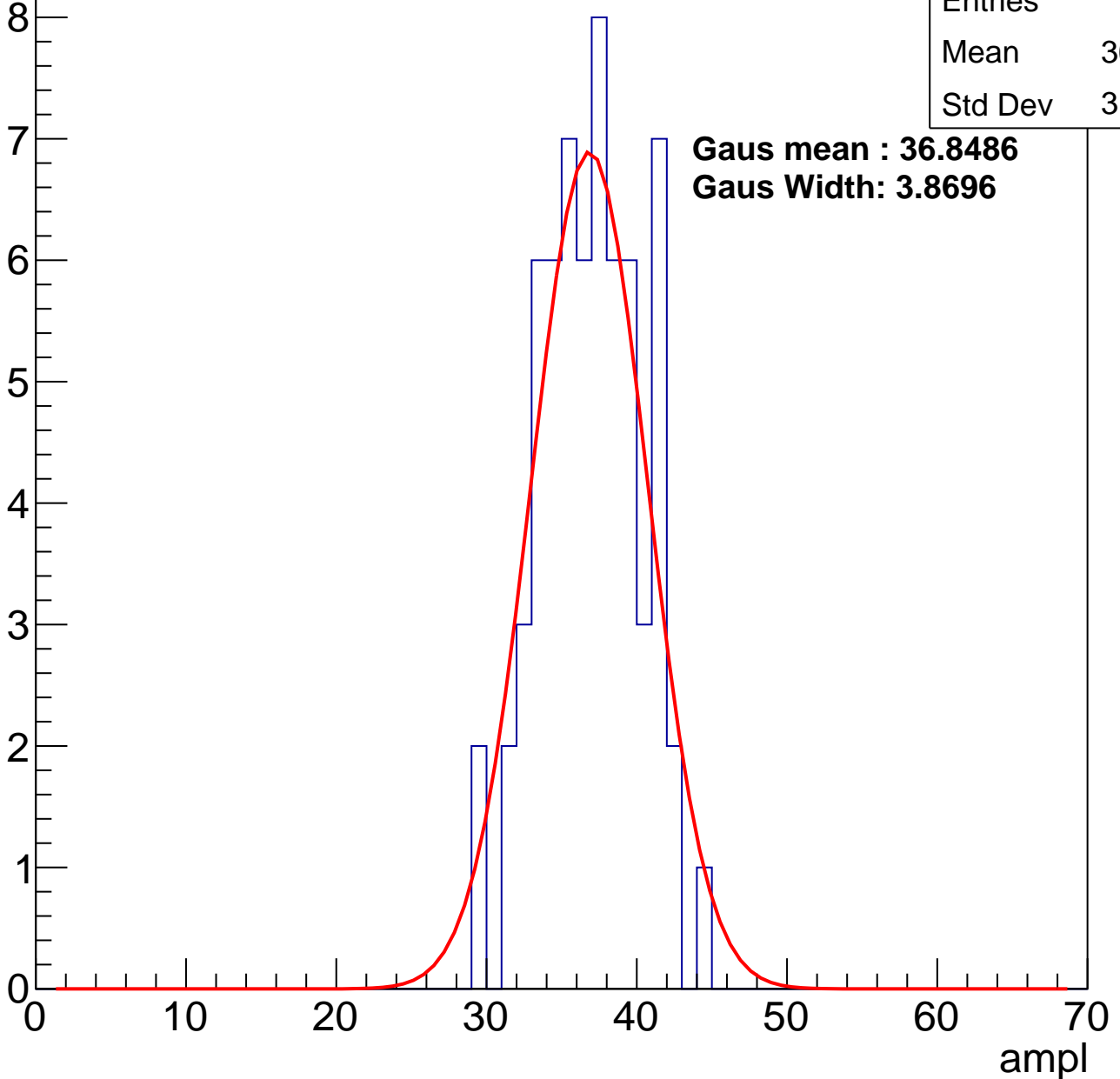
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	65
Mean	36.49
Std Dev	3.306

**Gaus mean : 36.8486**

**Gaus Width: 3.8696**



# B1L102S, U12-ch67, adc2

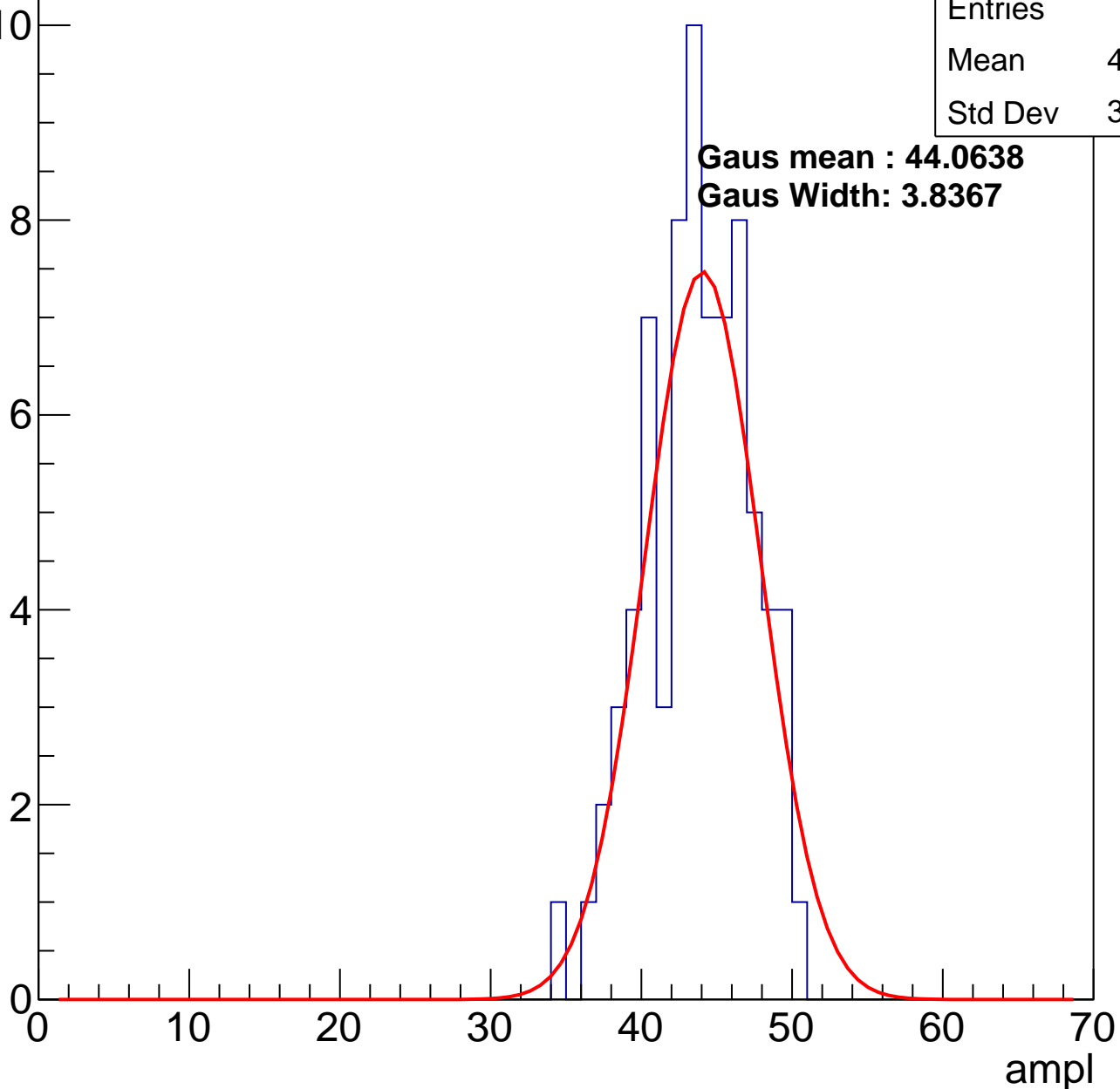
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	75
Mean	43.29
Std Dev	3.459

**Gaus mean : 44.0638**

**Gaus Width: 3.8367**

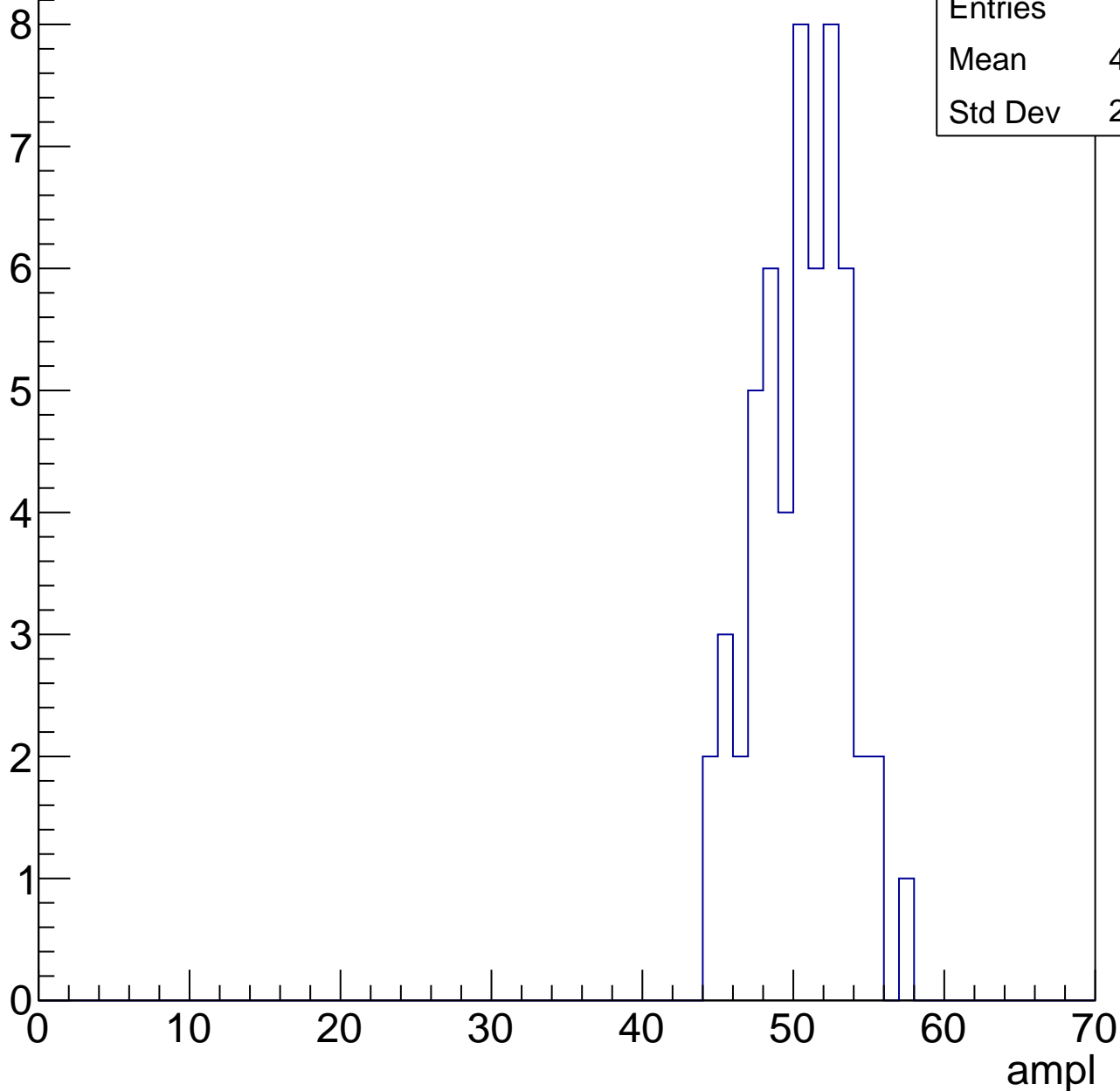


# B1L102S, U12-ch67, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	55
Mean	49.98
Std Dev	2.939

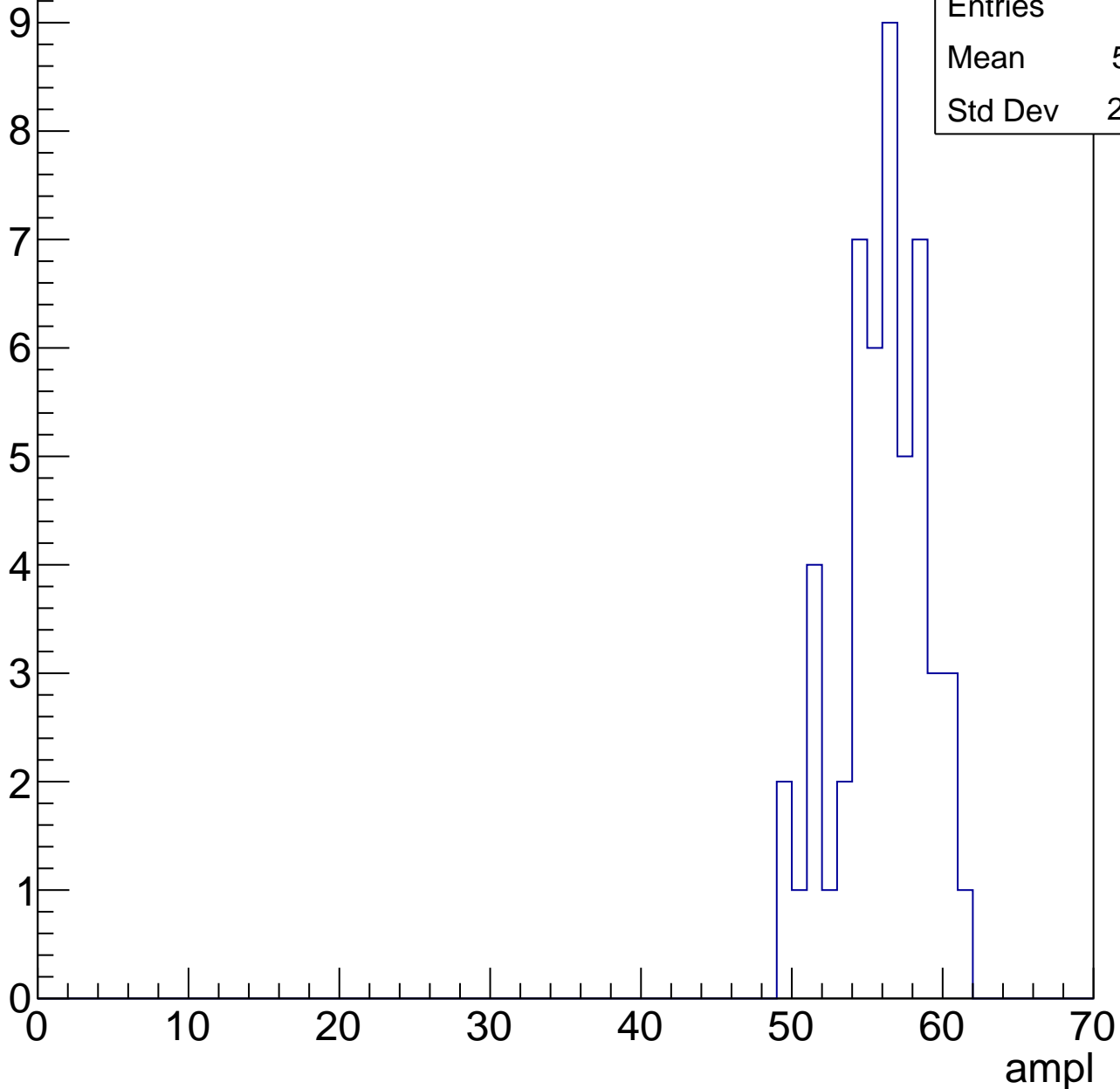


# B1L102S, U12-ch67, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	51
Mean	55.51
Std Dev	2.879

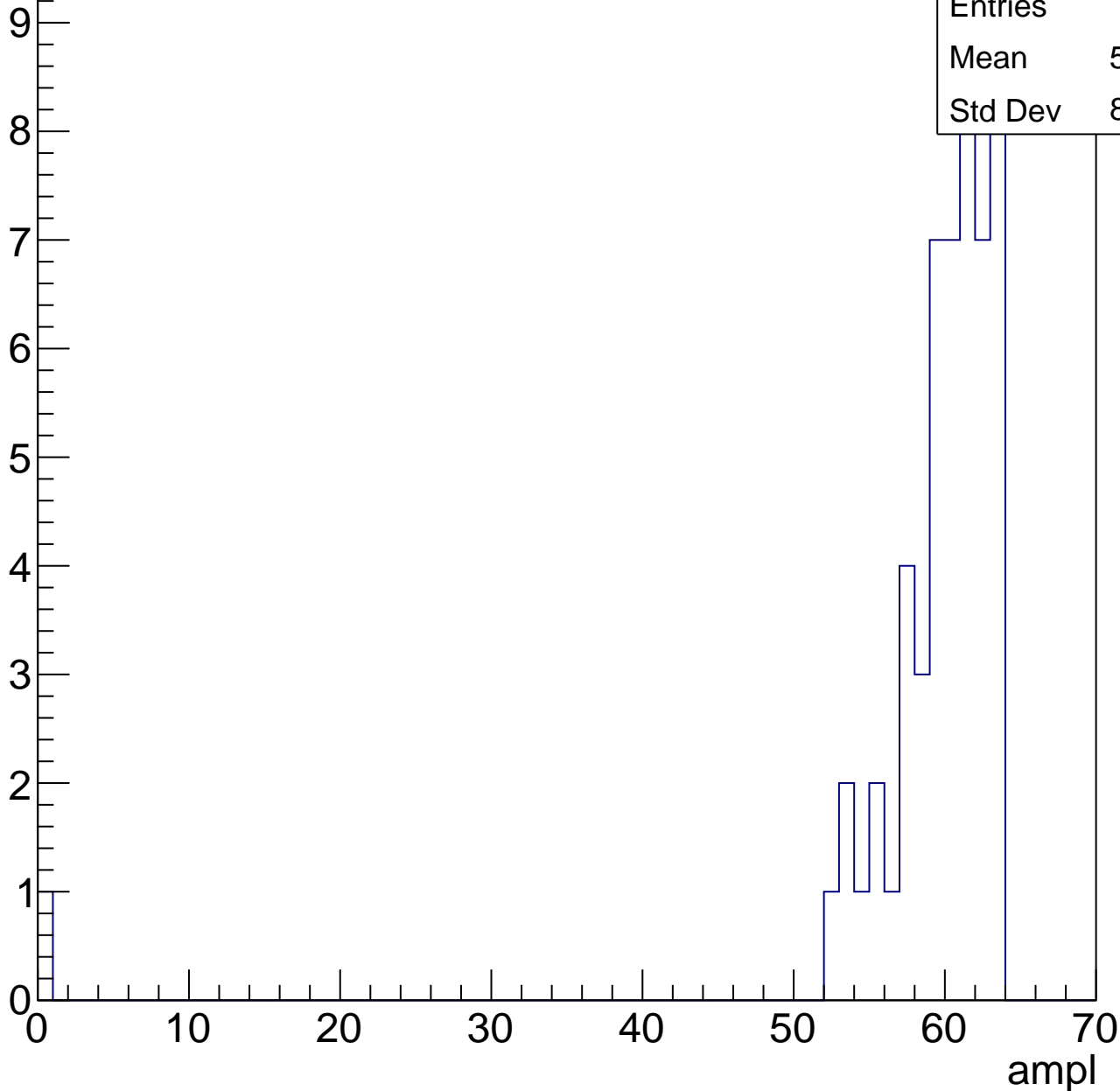


# B1L102S, U12-ch67, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

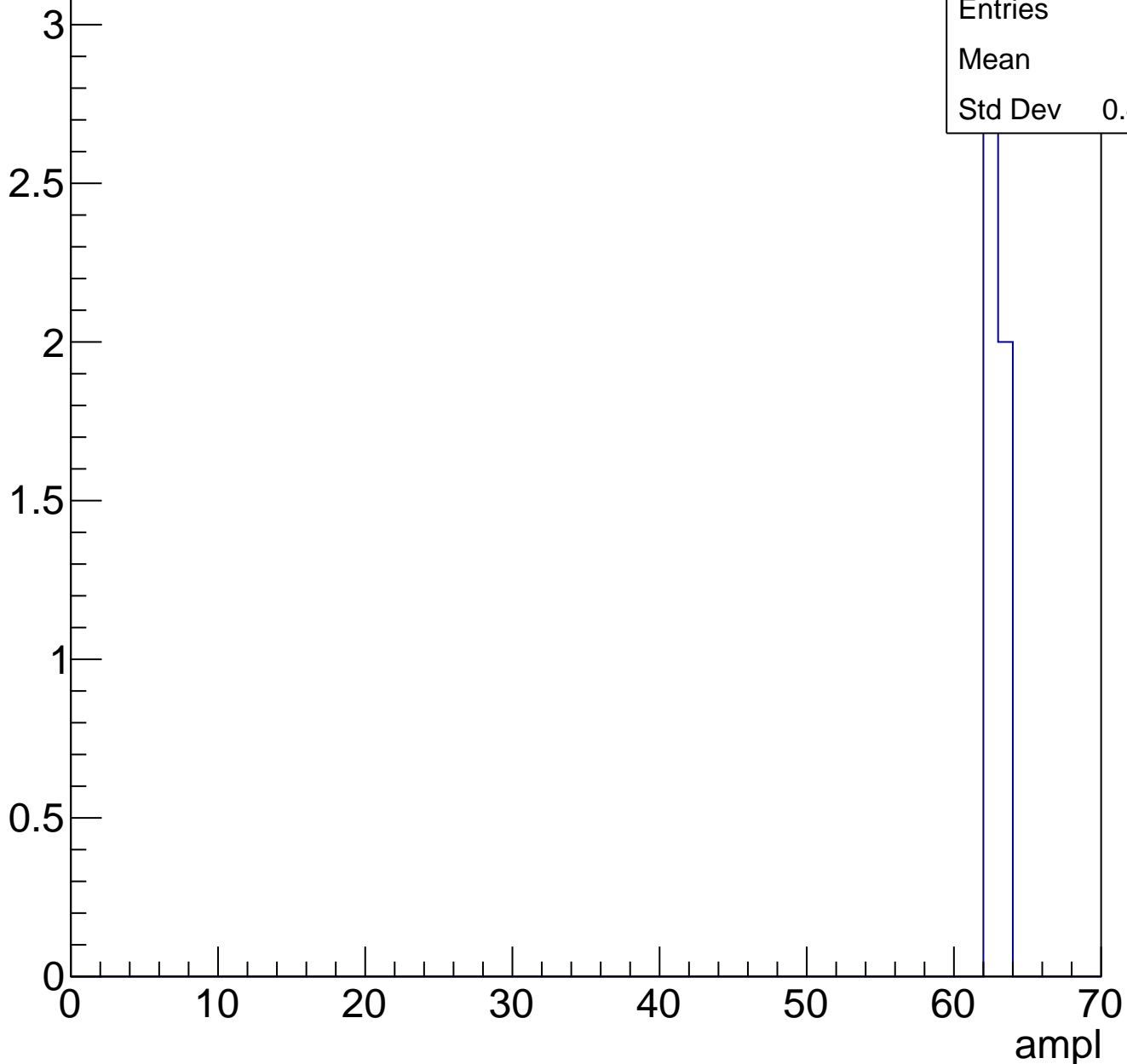
Entries	53
Mean	58.49
Std Dev	8.586



# B1L102S, U12-ch67, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U12-ch67, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U12-ch68, adc0

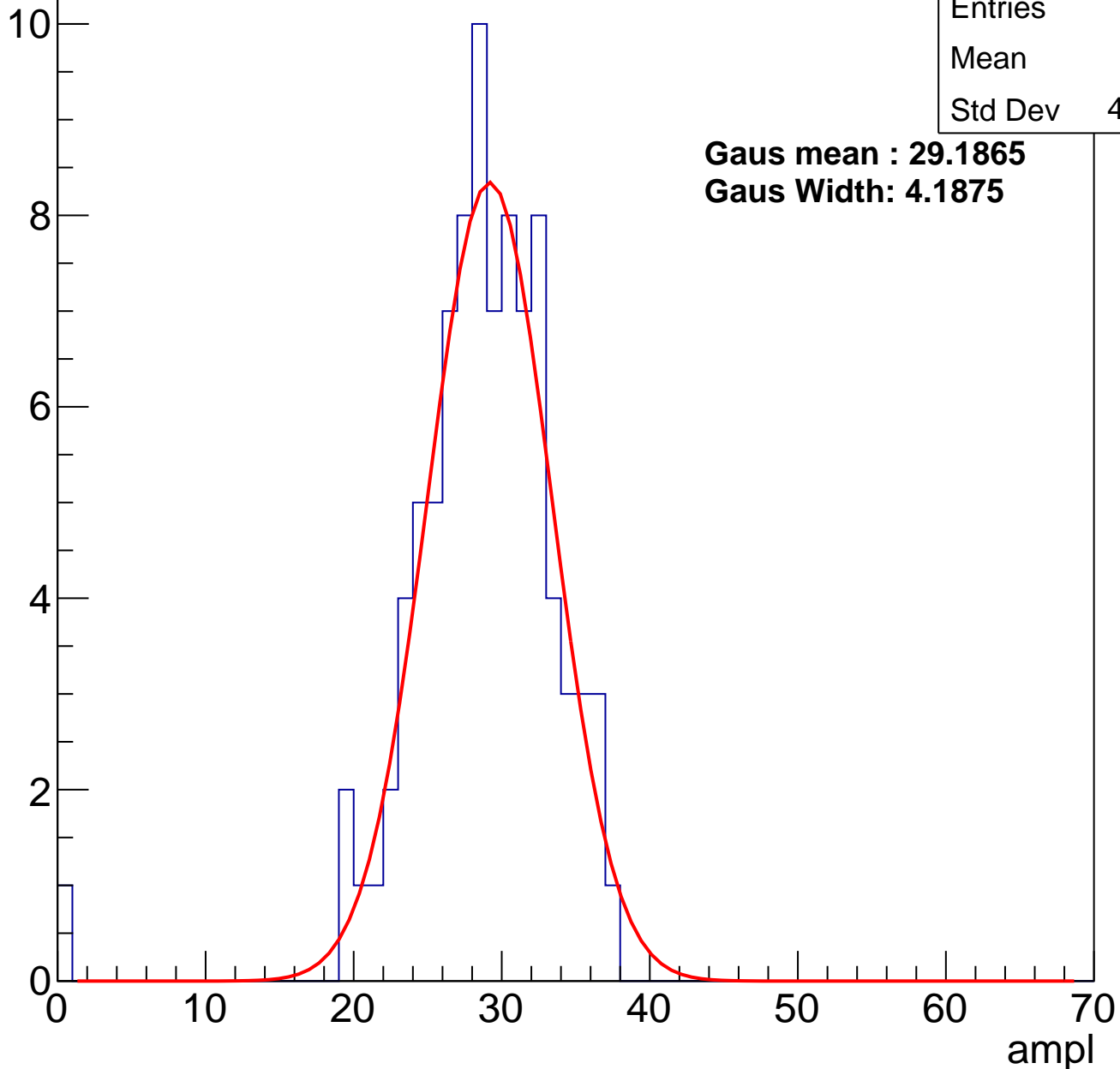
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	90
Mean	28.2
Std Dev	4.996

**Gaus mean : 29.1865**

**Gaus Width: 4.1875**

Entry



# B1L102S, U12-ch68, adc1

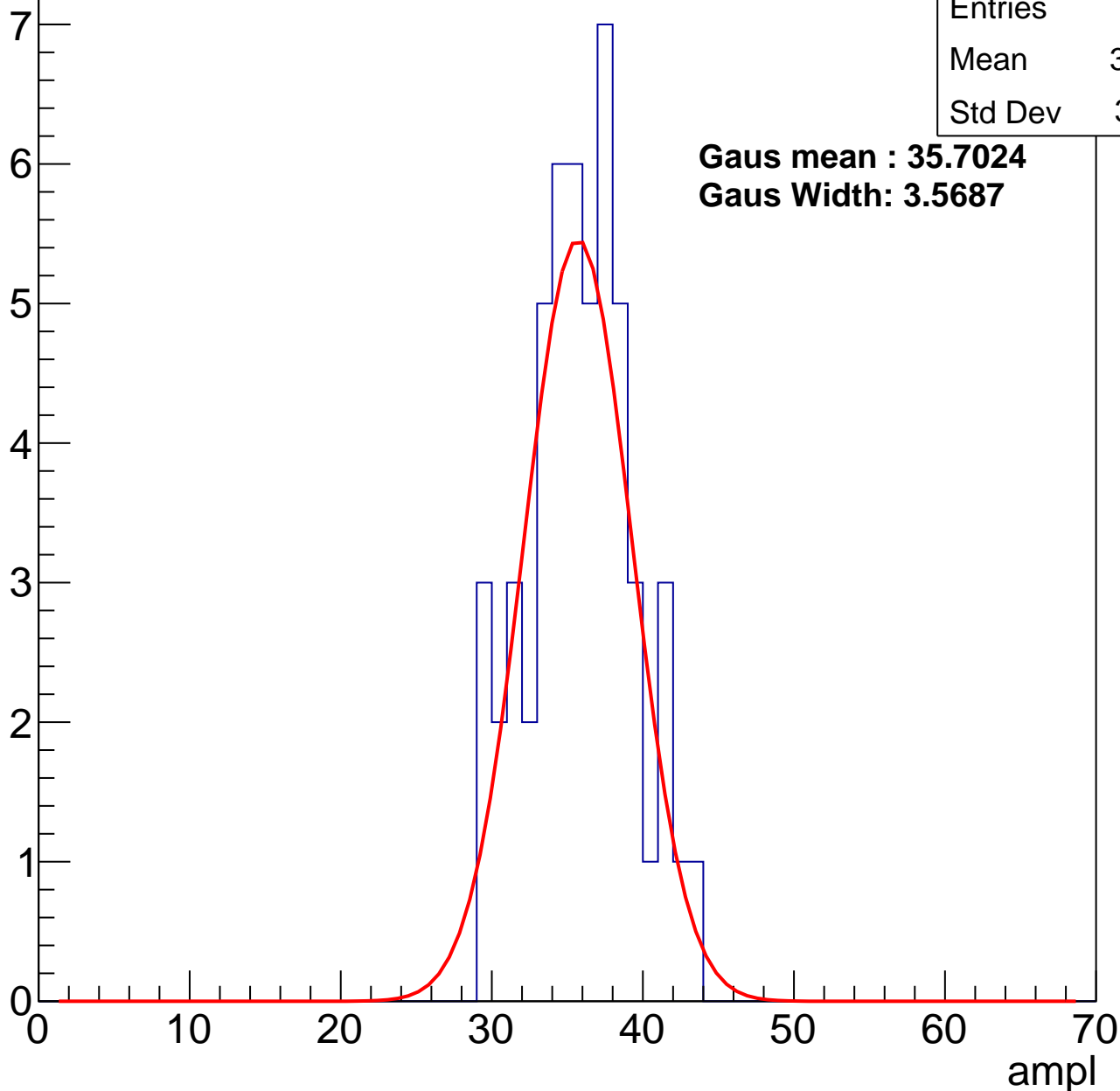
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	53
Mean	35.42
Std Dev	3.401

**Gaus mean : 35.7024**

**Gaus Width: 3.5687**



# B1L102S, U12-ch68, adc2

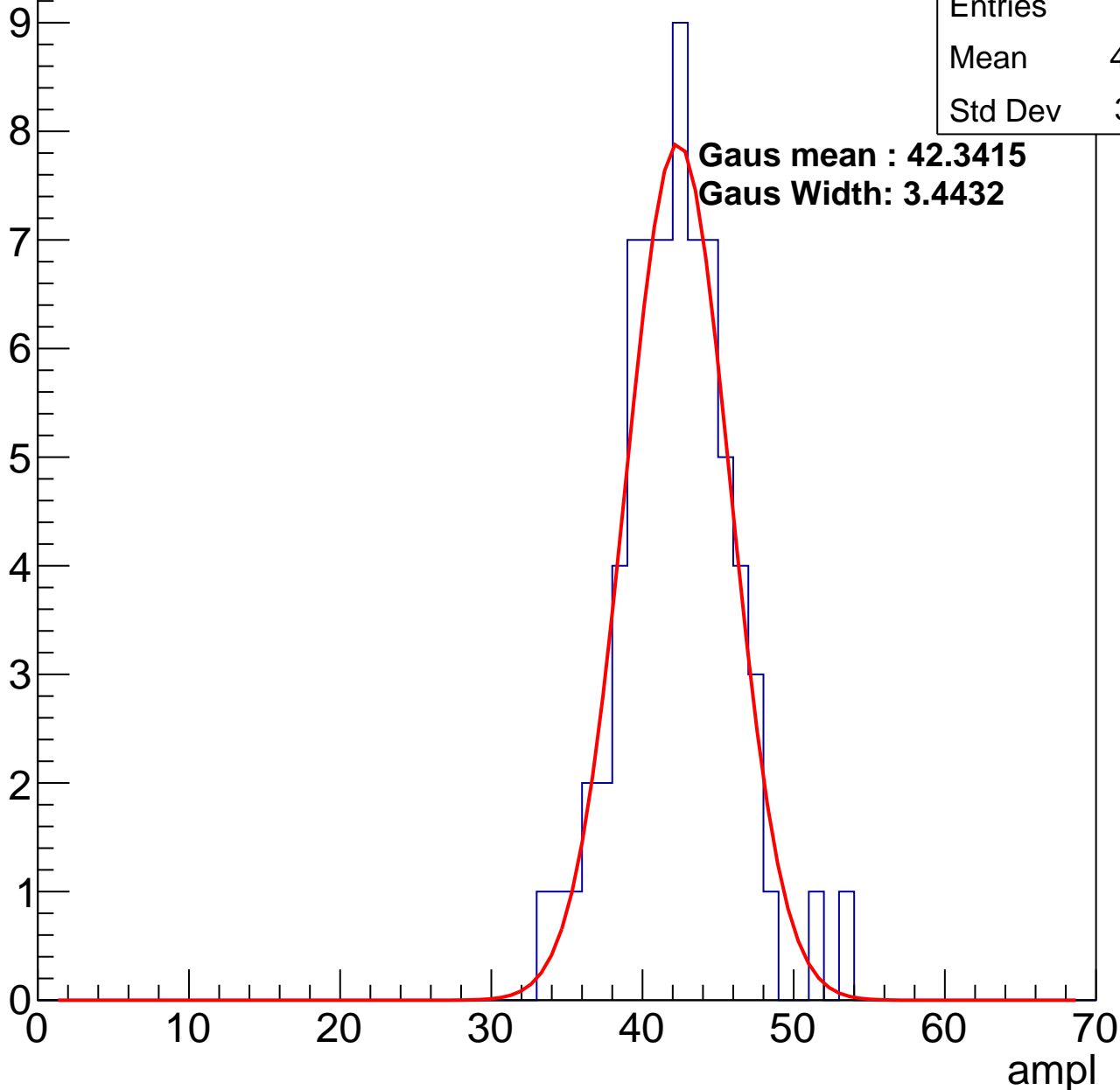
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	70
Mean	41.84
Std Dev	3.651

**Gaus mean : 42.3415**

**Gaus Width: 3.4432**

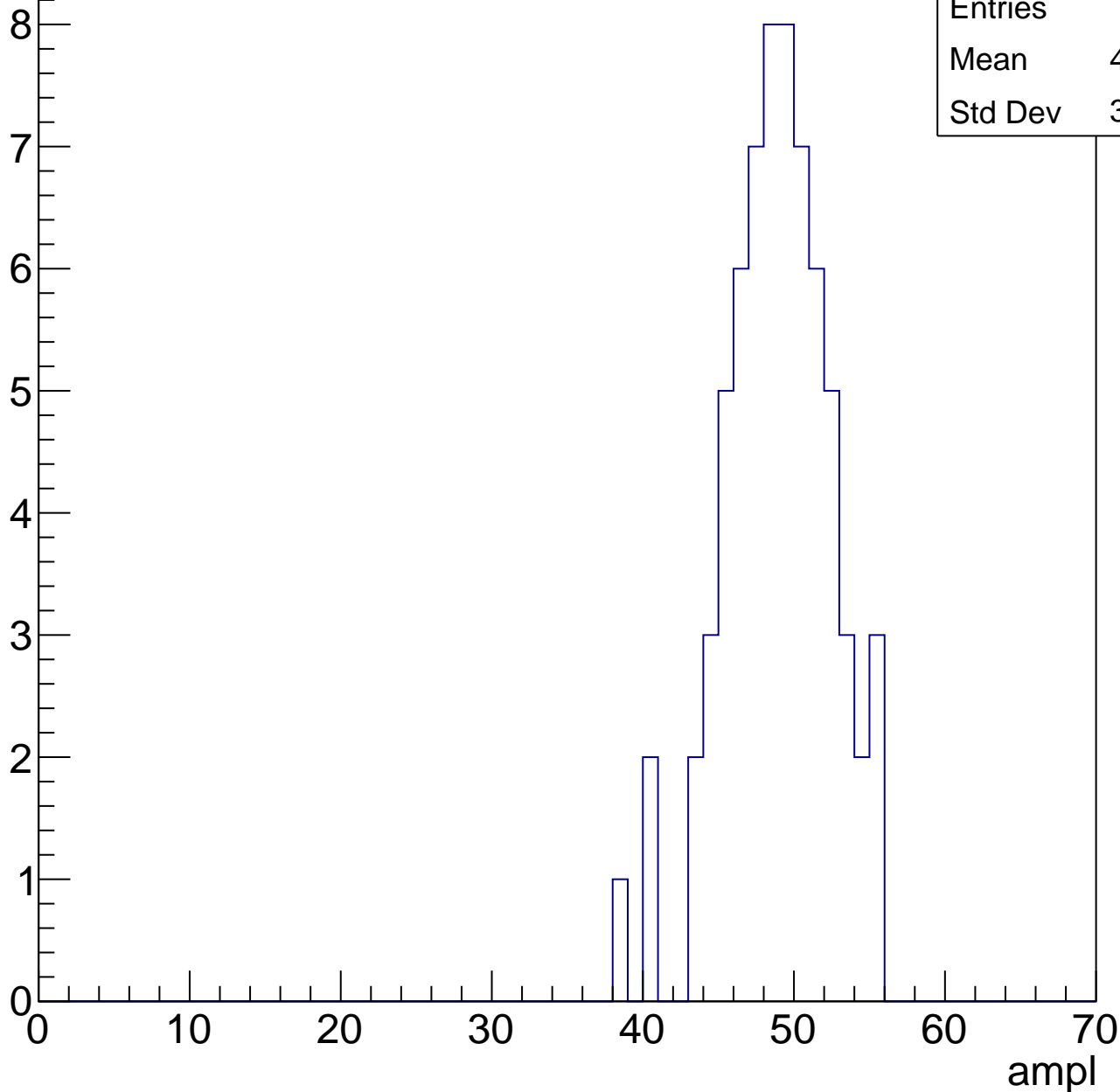


# B1L102S, U12-ch68, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	48.38
Std Dev	3.548

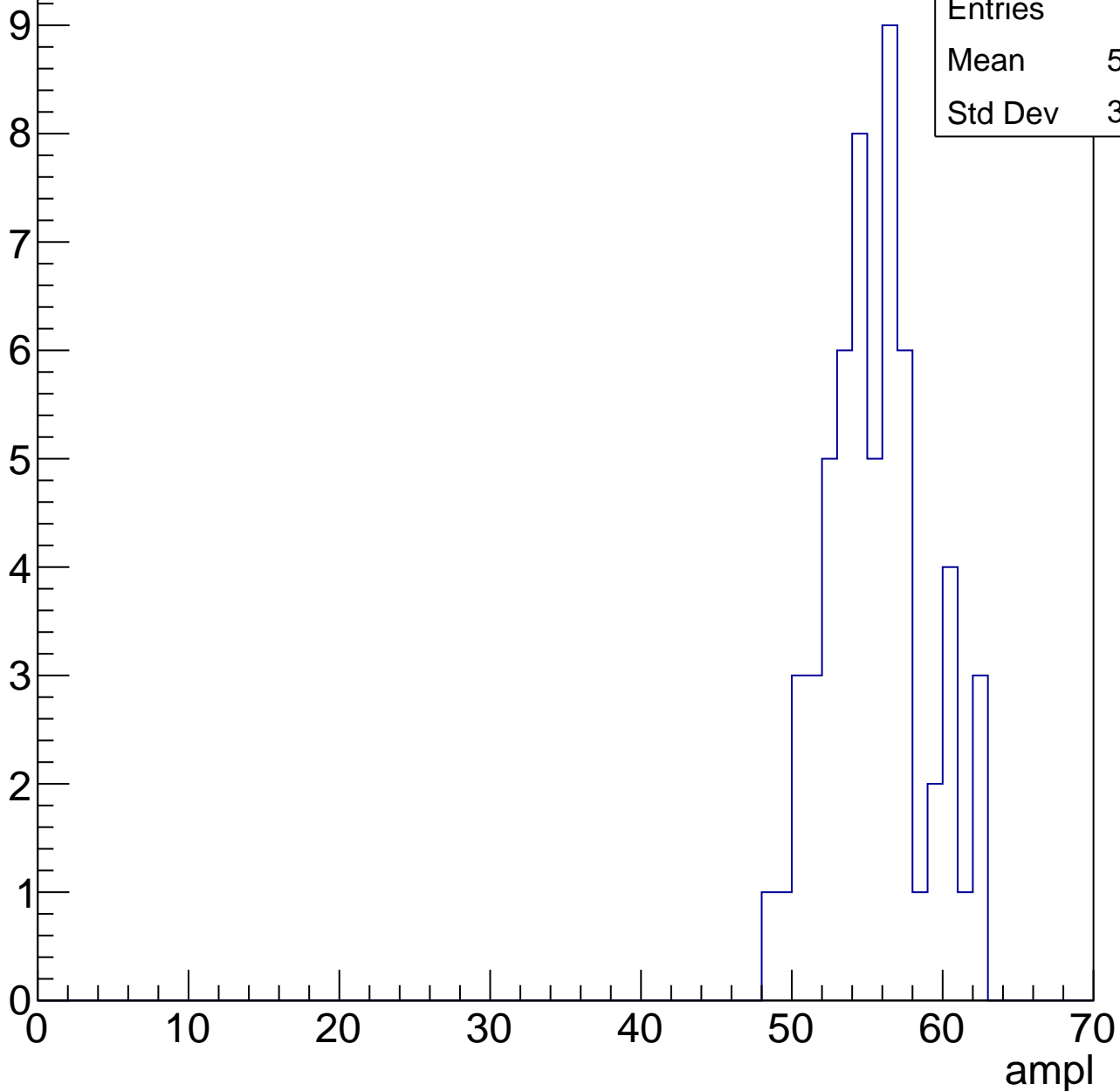


# B1L102S, U12-ch68, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	58
Mean	55.07
Std Dev	3.326



# B1L102S, U12-ch68, adc5

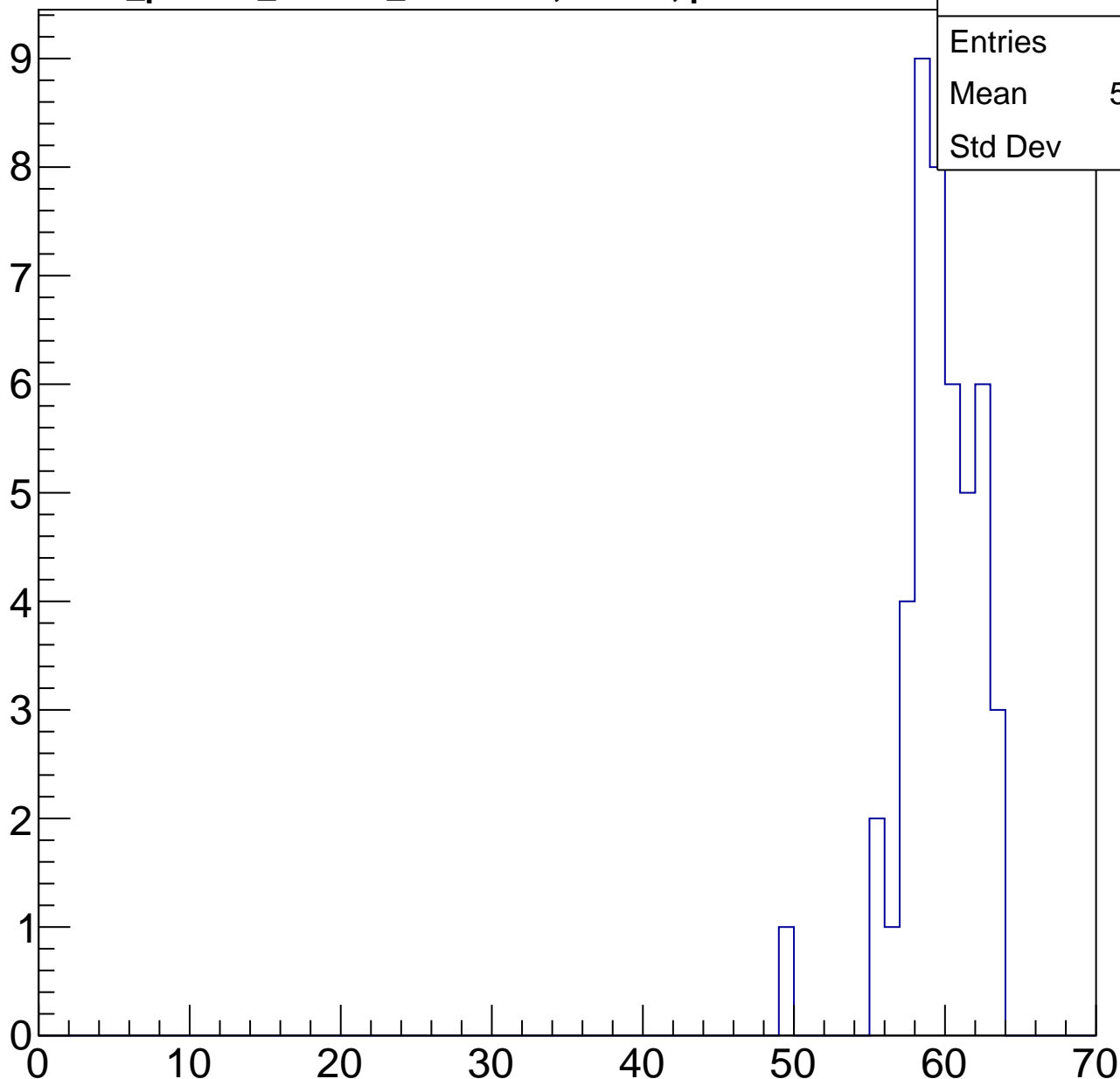
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	45
Mean	59.18
Std Dev	2.55

ampl

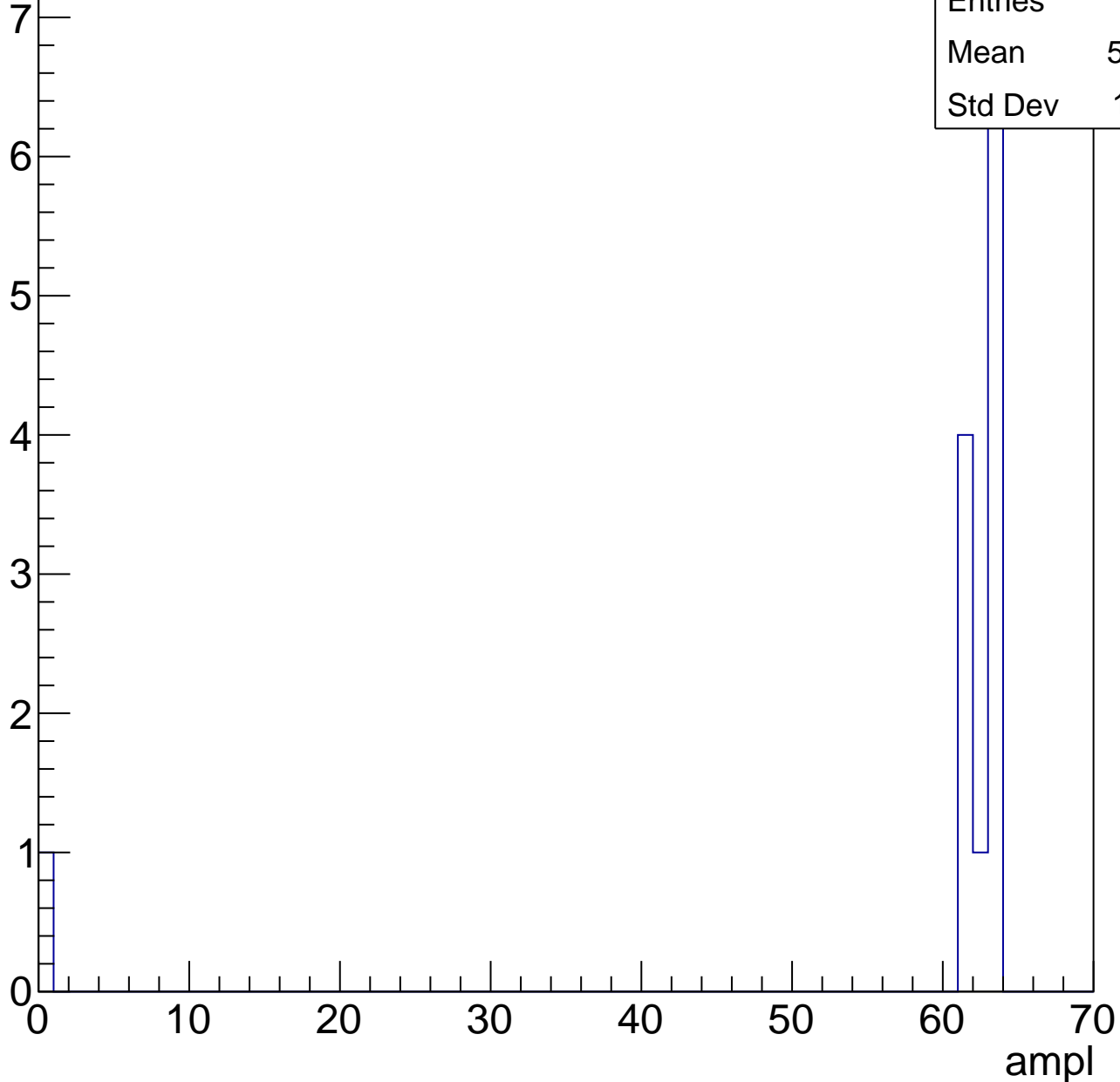


# B1L102S, U12-ch68, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	13
Mean	57.46
Std Dev	16.61





# B1L102S, U12-ch68, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U12-ch69, adc0

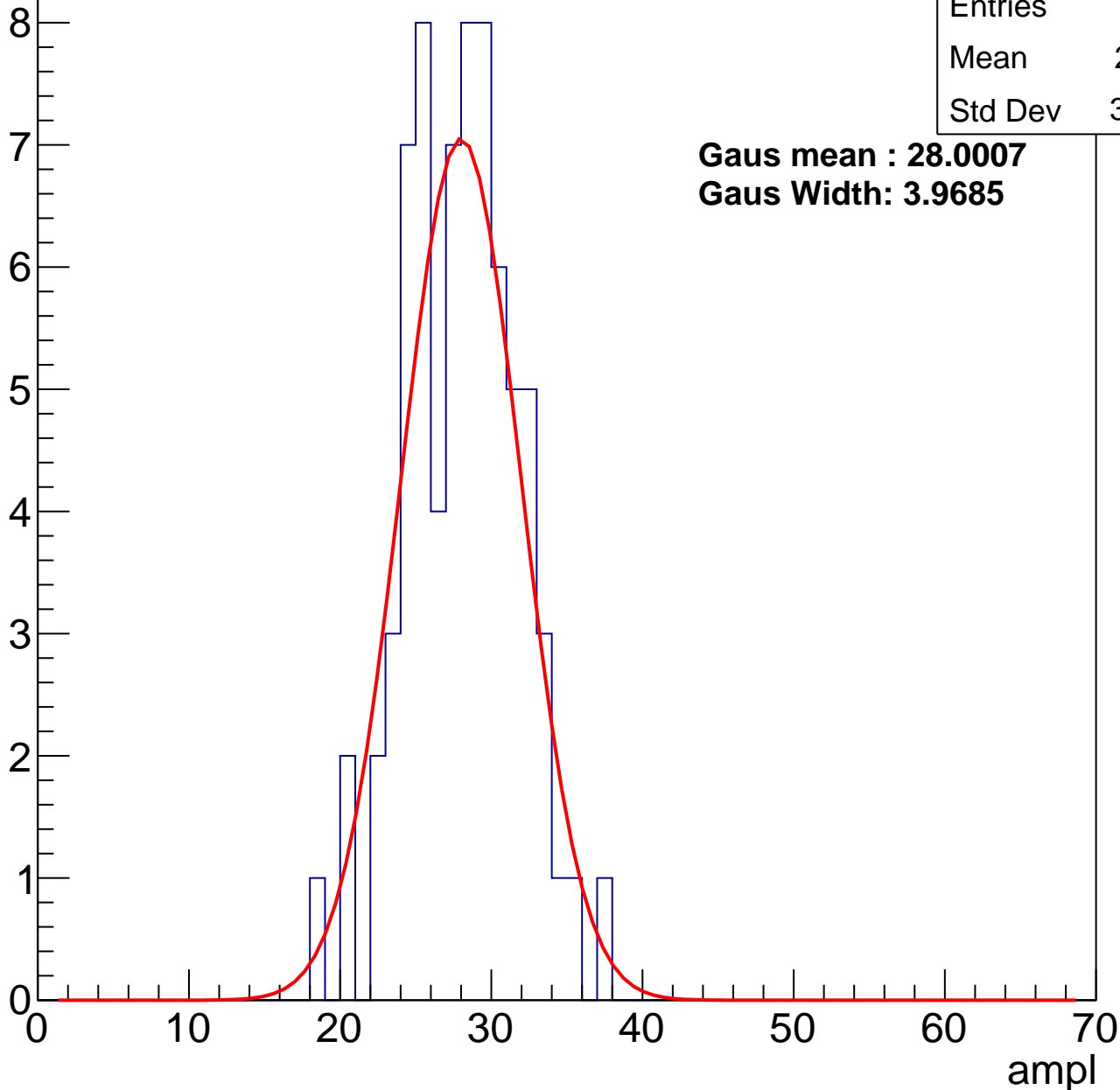
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	72
Mean	27.61
Std Dev	3.669

**Gaus mean : 28.0007**

**Gaus Width: 3.9685**



# B1L102S, U12-ch69, adc1

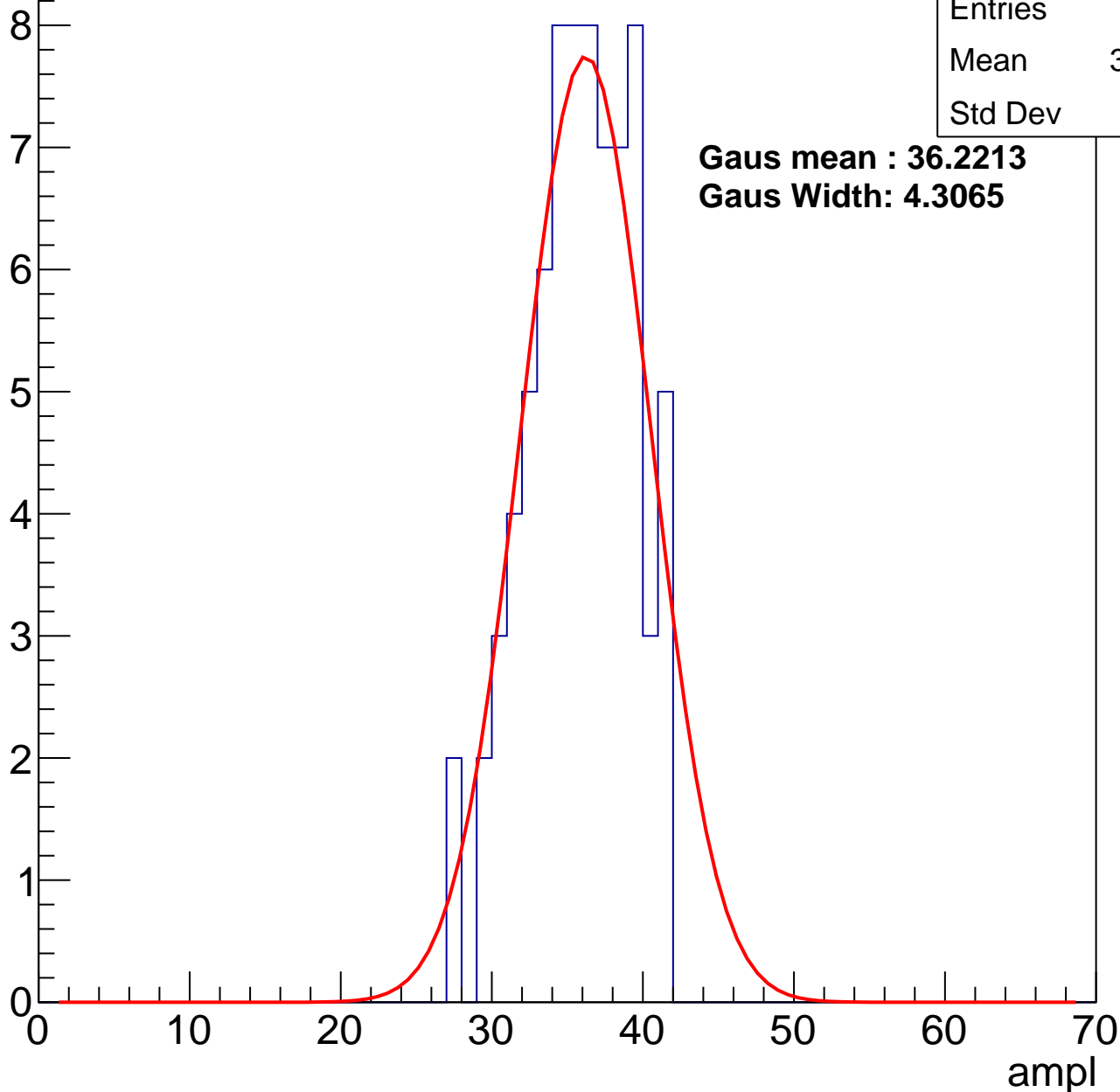
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	76
Mean	35.34
Std Dev	3.42

**Gaus mean : 36.2213**

**Gaus Width: 4.3065**



# B1L102S, U12-ch69, adc2

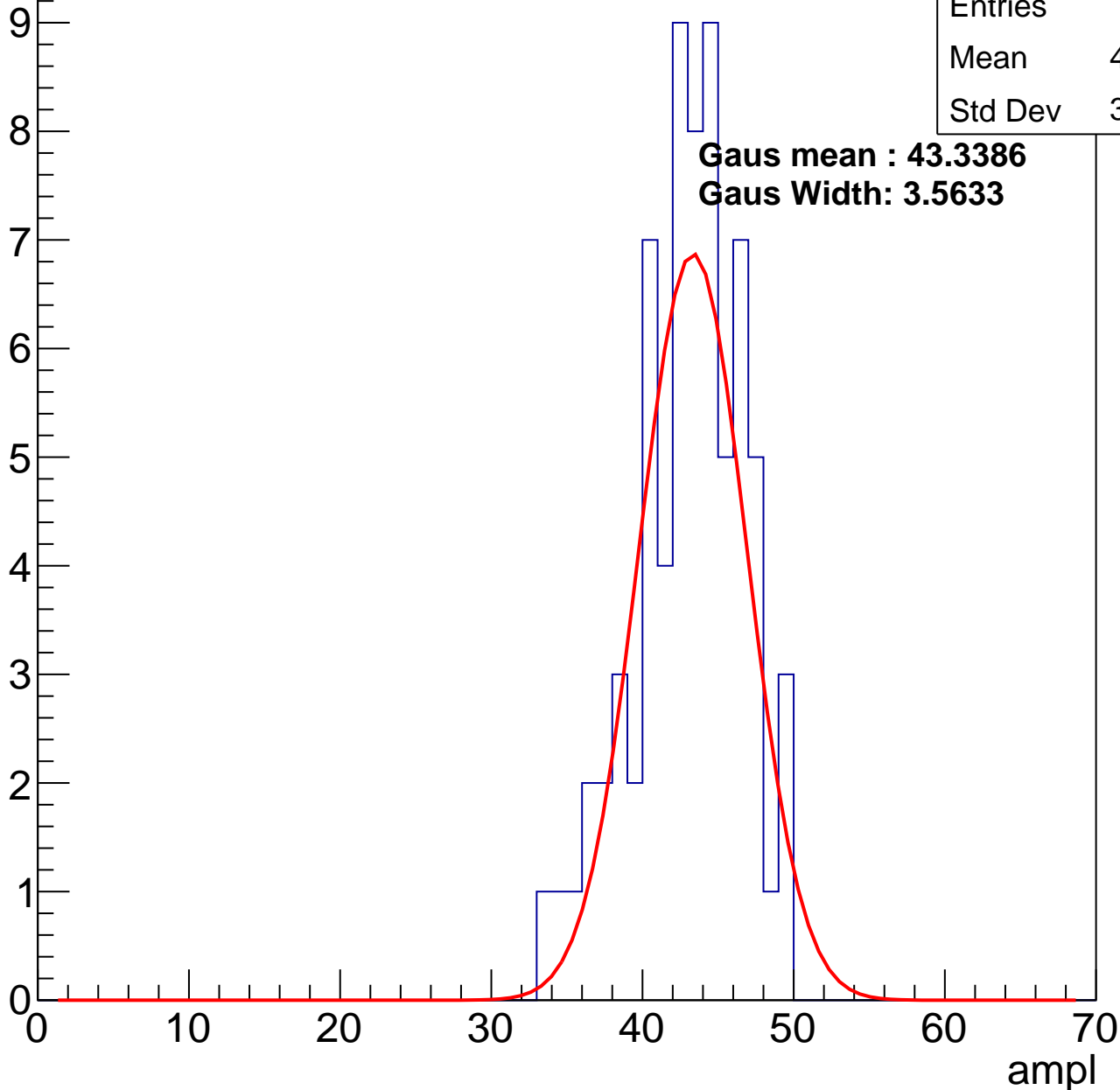
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	70
Mean	42.56
Std Dev	3.588

**Gaus mean : 43.3386**

**Gaus Width: 3.5633**

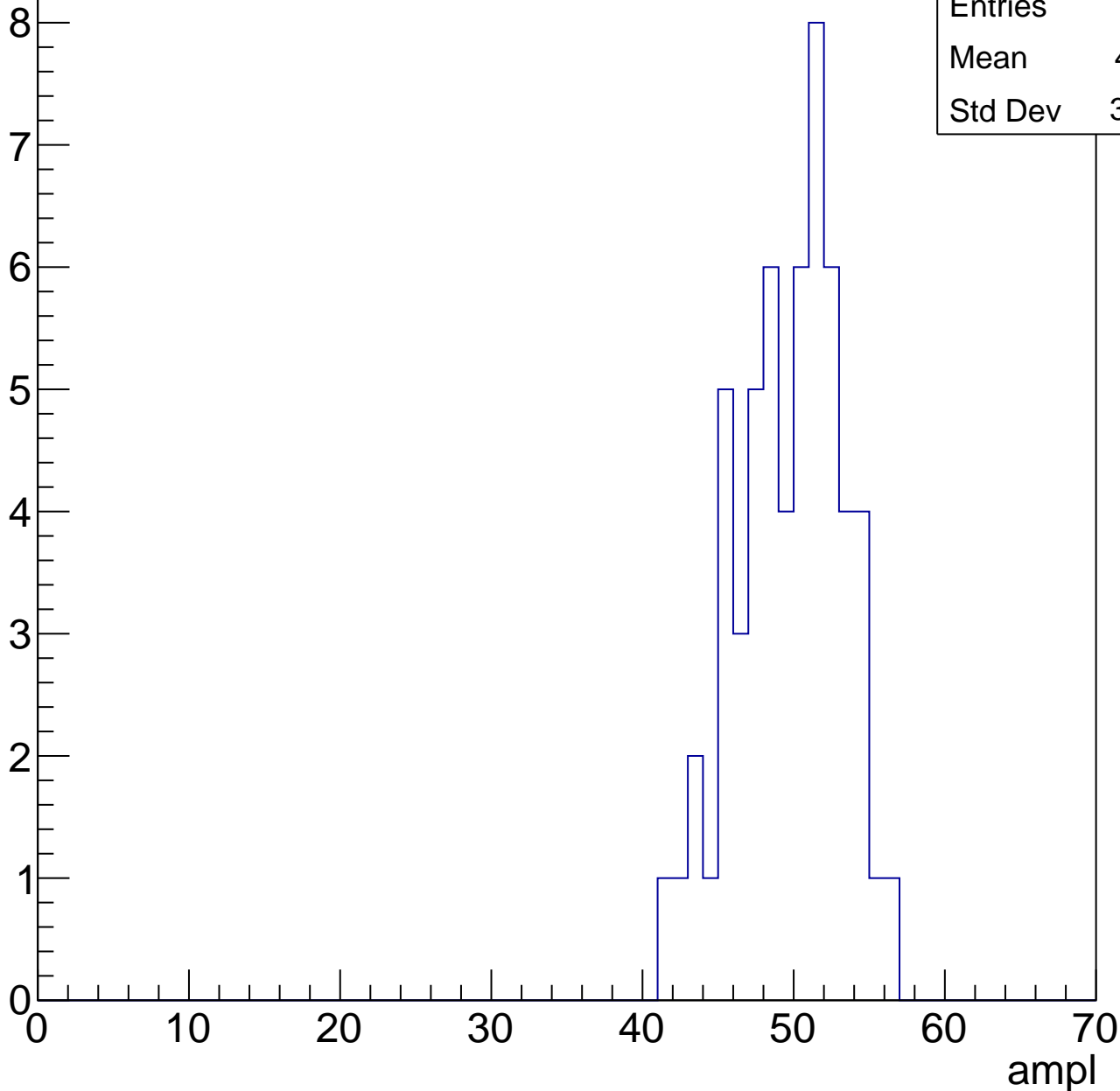


# B1L102S, U12-ch69, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	58
Mean	49.21
Std Dev	3.428

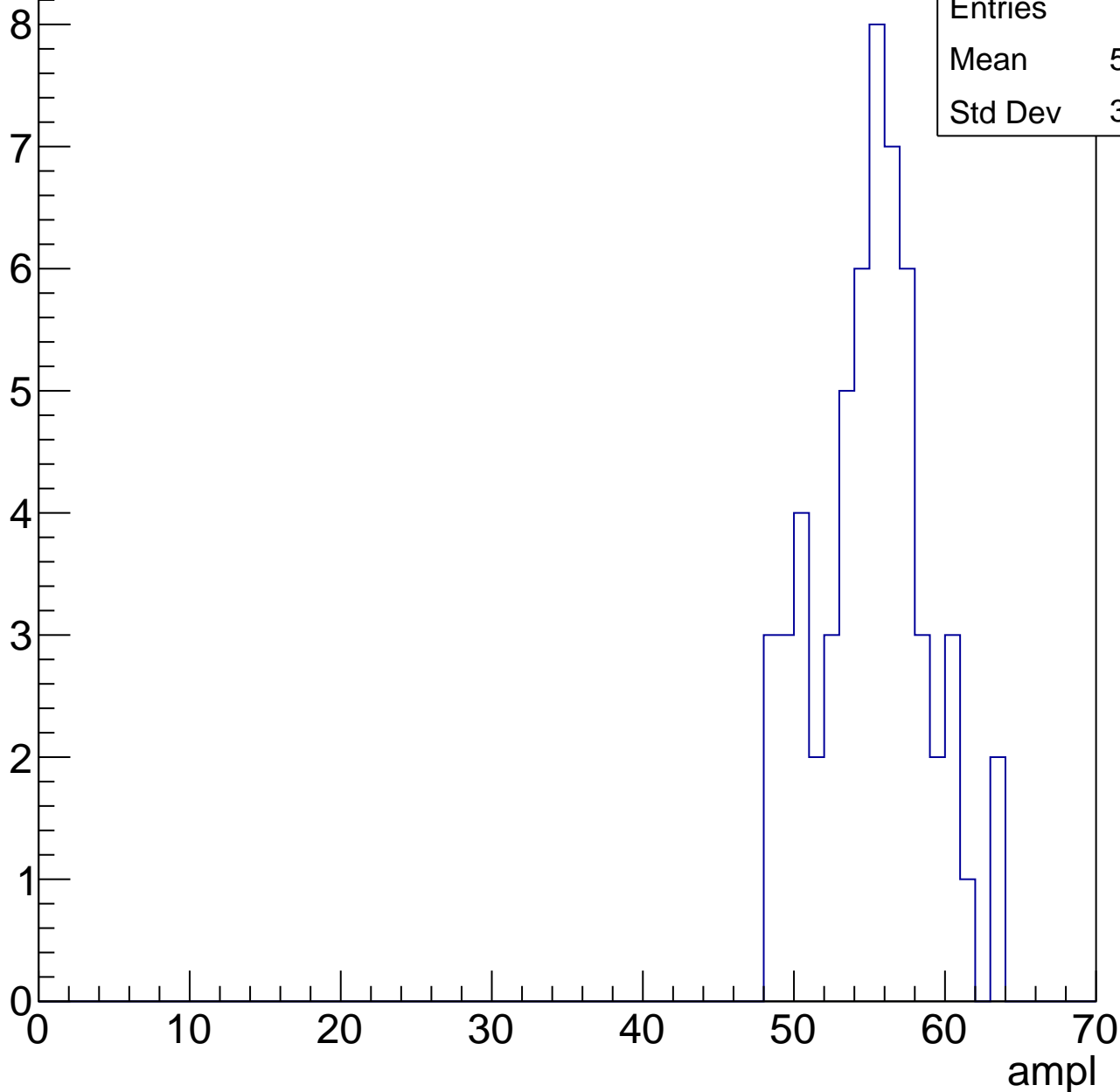


# B1L102S, U12-ch69, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

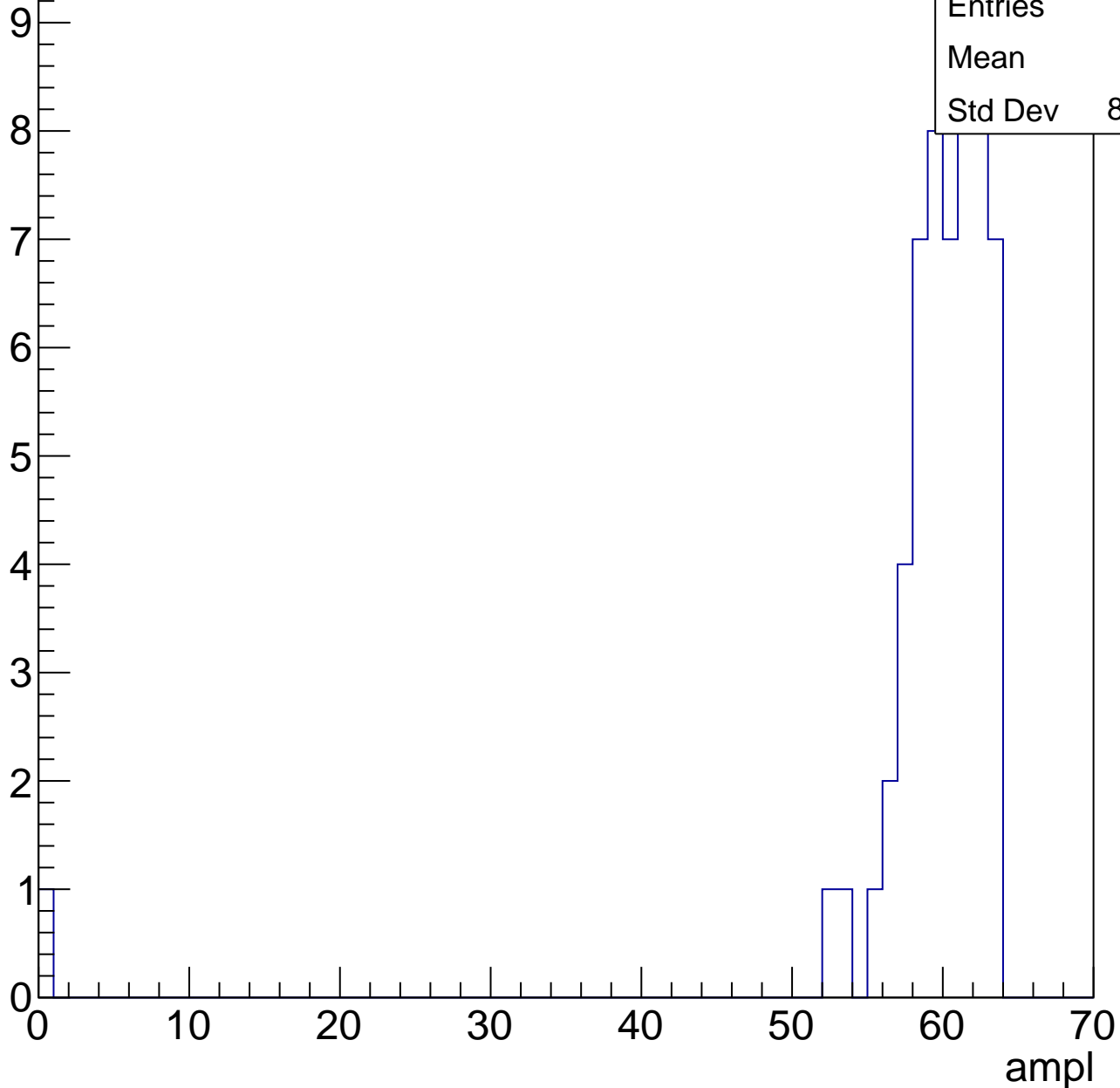
Entries	58
Mean	54.67
Std Dev	3.626



# B1L102S, U12-ch69, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U12-ch69, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U12-ch69, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U12-ch70, adc0

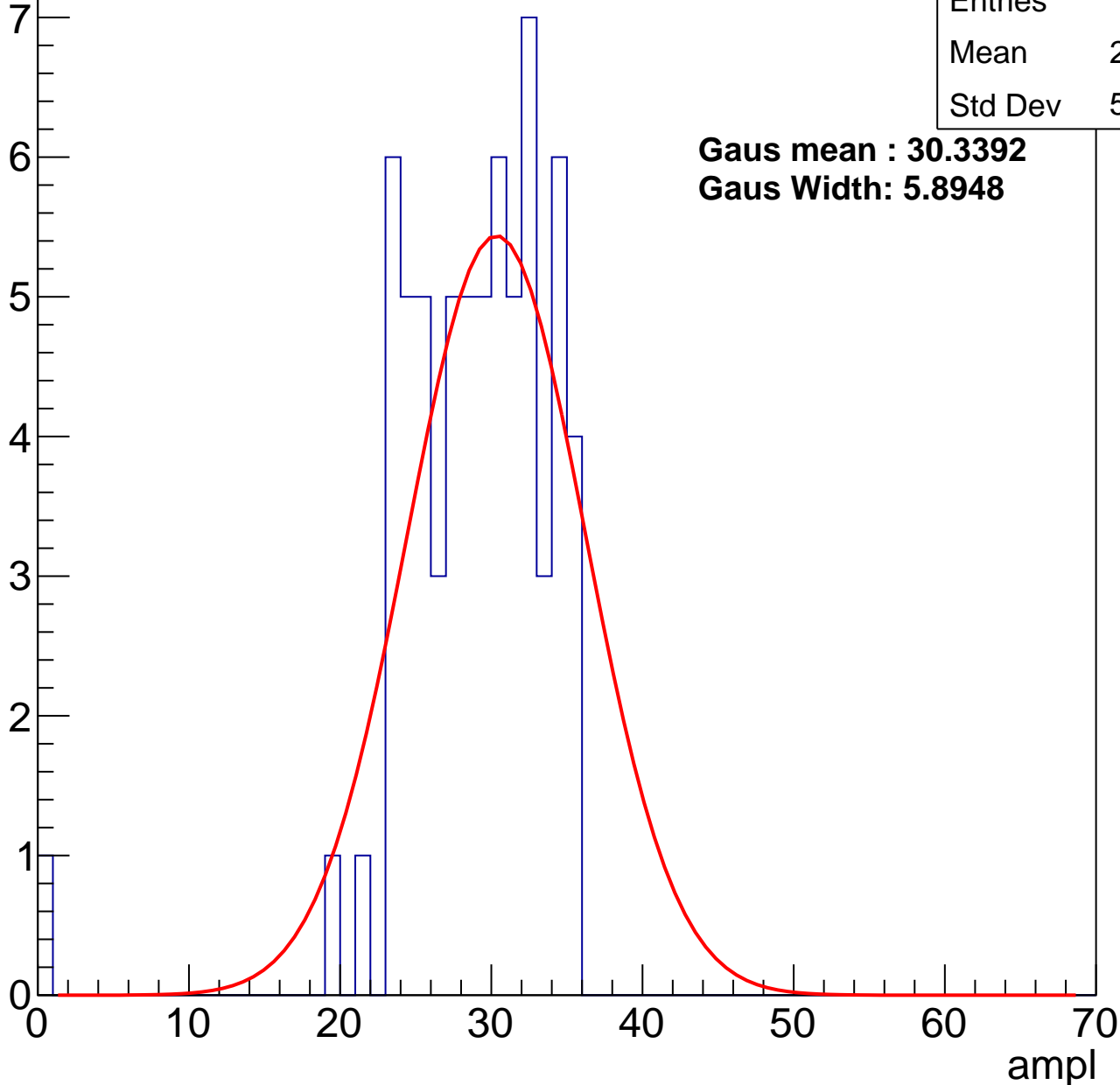
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	28.28
Std Dev	5.249

**Gaus mean : 30.3392**

**Gaus Width: 5.8948**



# B1L102S, U12-ch70, adc1

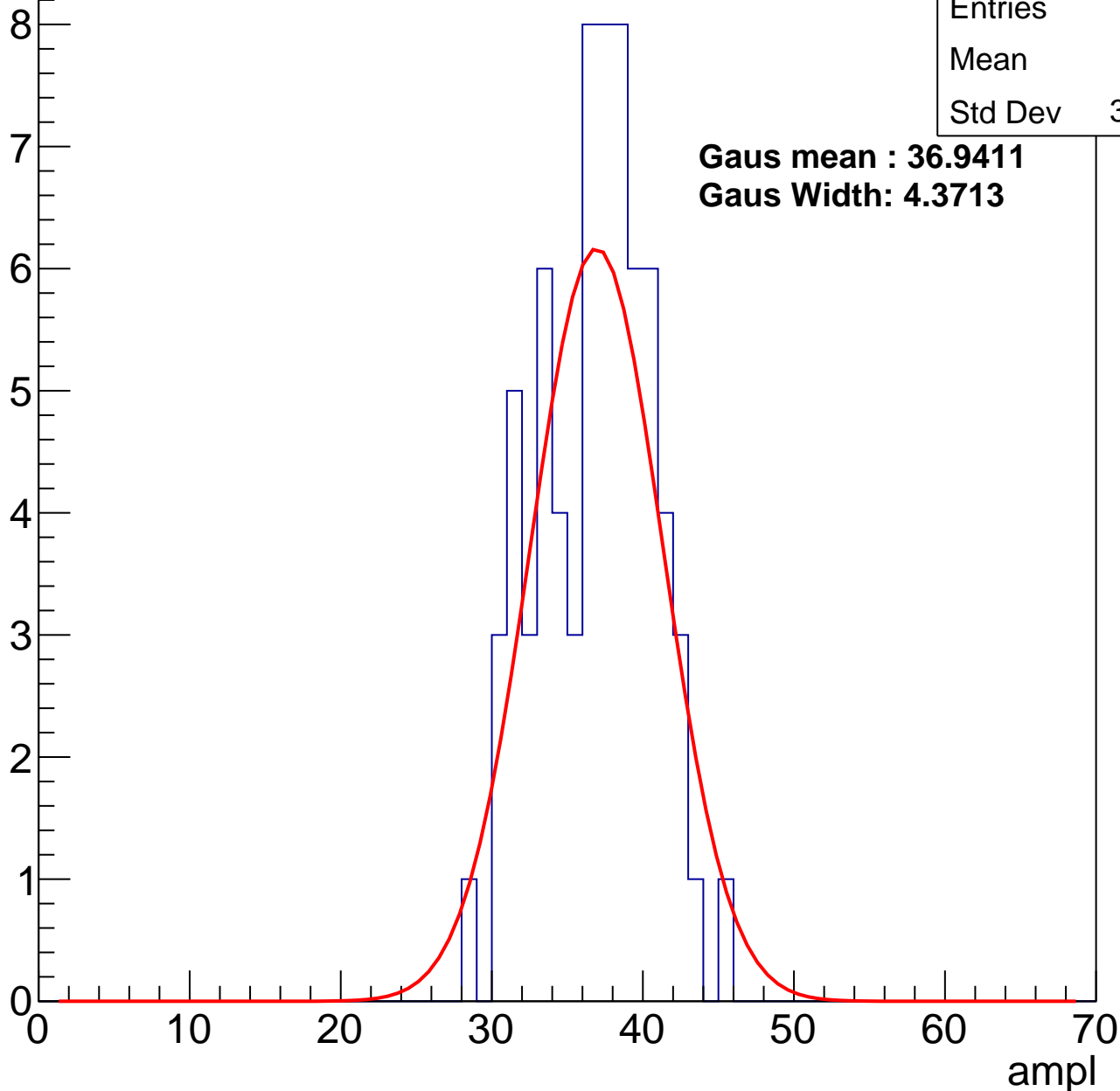
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	70
Mean	36.4
Std Dev	3.654

**Gaus mean : 36.9411**

**Gaus Width: 4.3713**



# B1L102S, U12-ch70, adc2

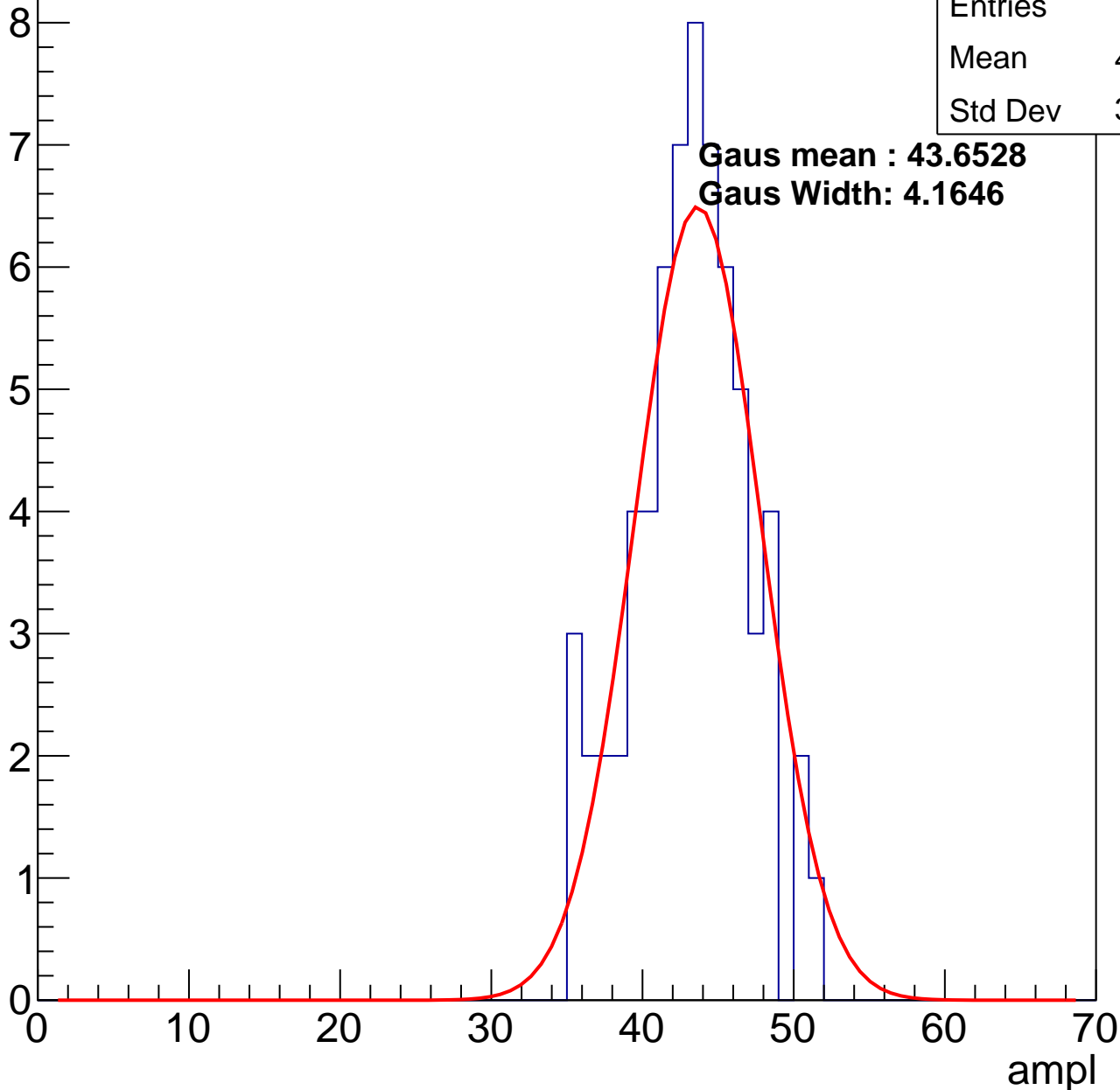
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	42.71
Std Dev	3.741

**Gaus mean : 43.6528**

**Gaus Width: 4.1646**



# B1L102S, U12-ch70, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	84
Mean	50.4
Std Dev	3.522

Entry

10

8

6

4

2

0

0

10

20

30

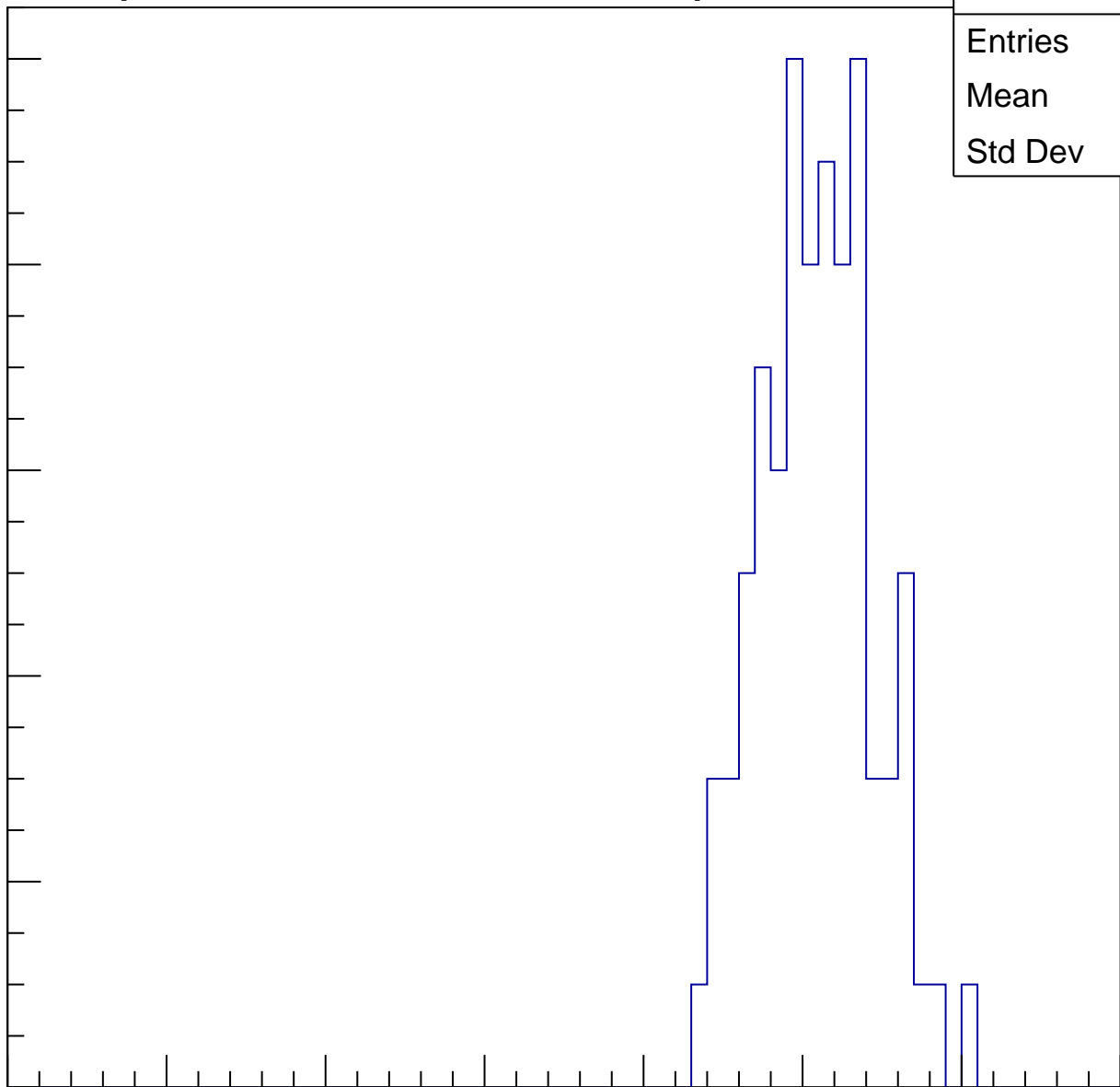
40

50

60

ampl

70

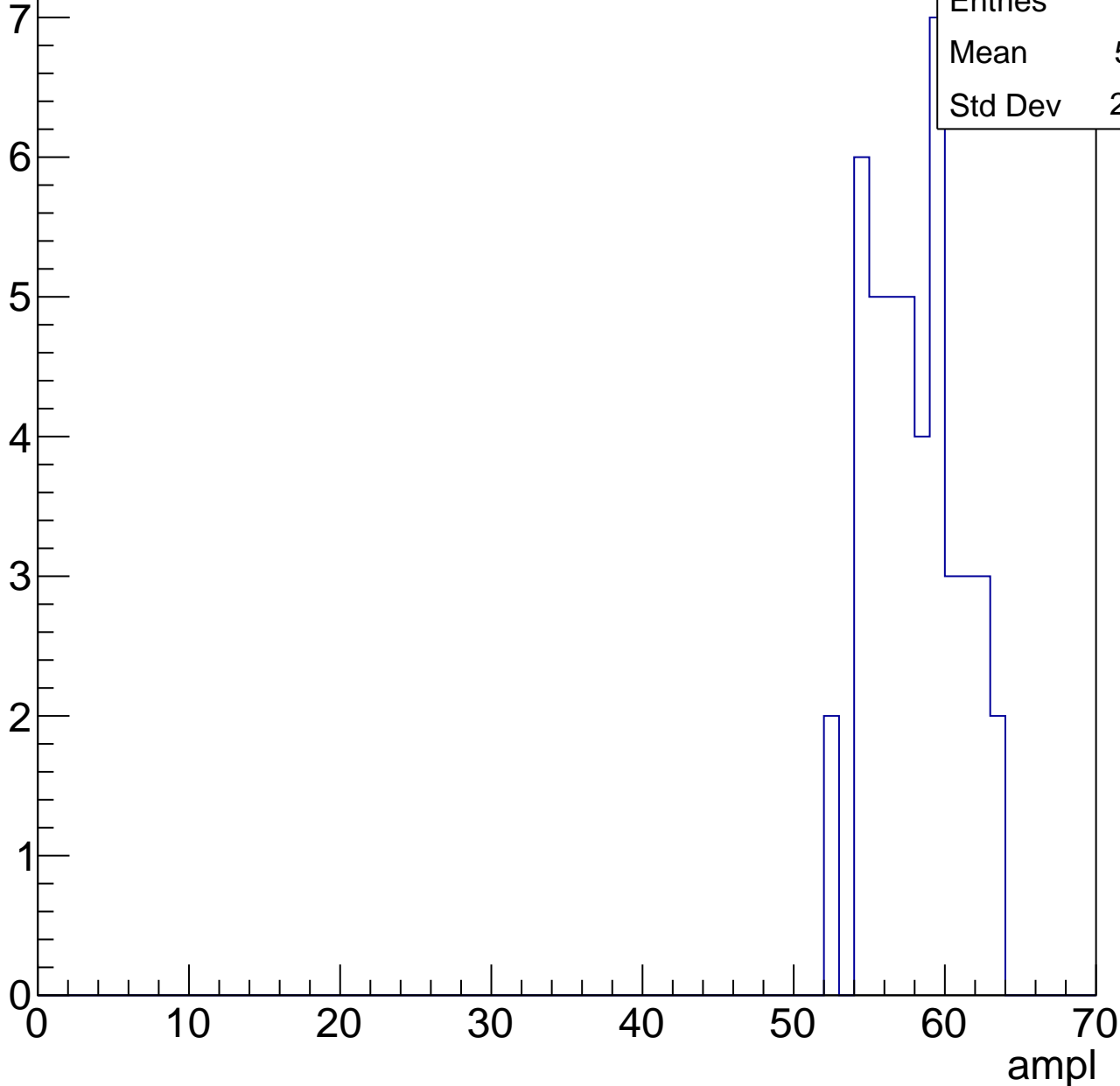


# B1L102S, U12-ch70, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	45
Mean	57.51
Std Dev	2.872

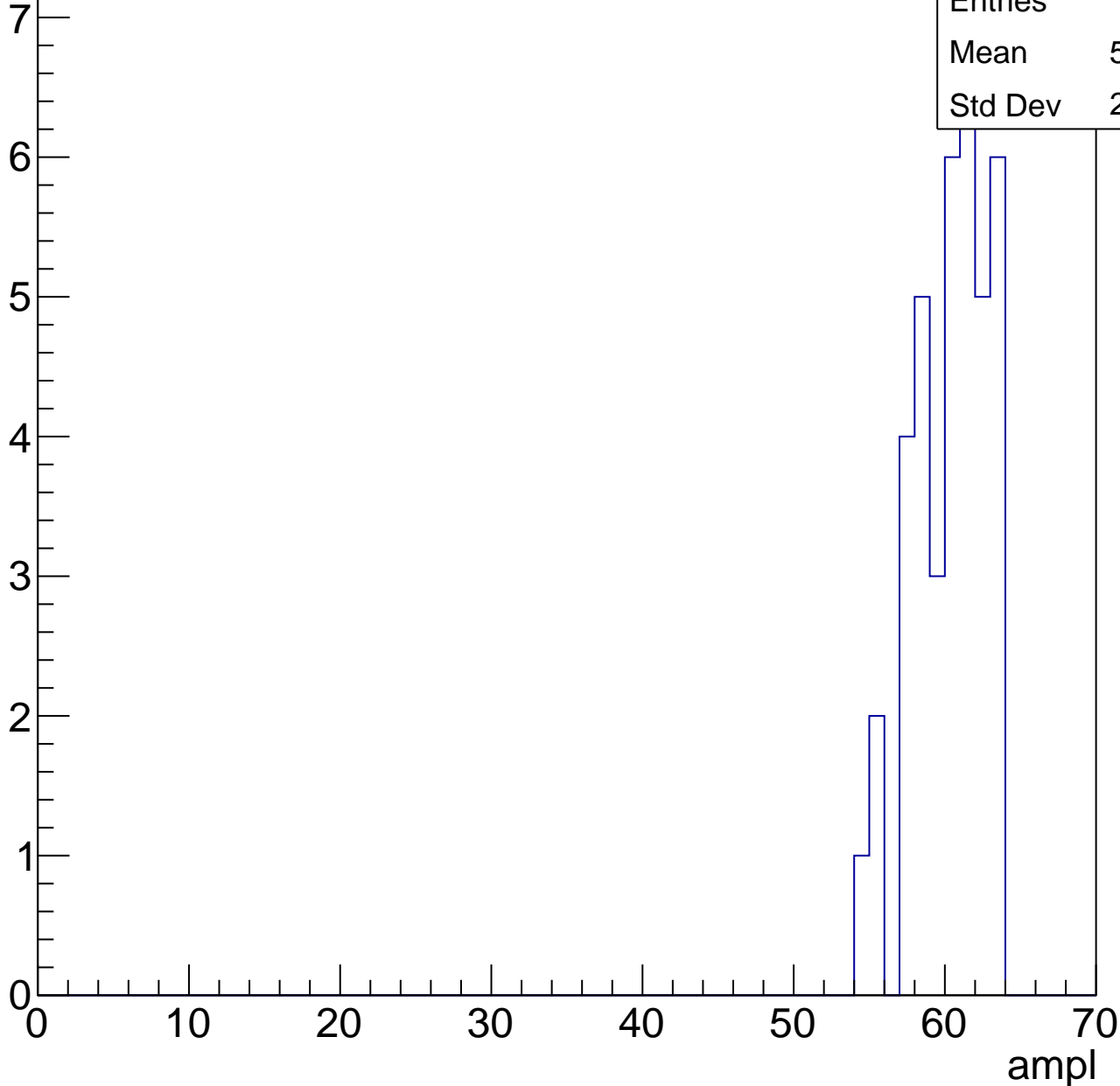


# B1L102S, U12-ch70, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	39
Mean	59.85
Std Dev	2.402



# B1L102S, U12-ch70, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U12-ch70, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U12-ch71, adc0

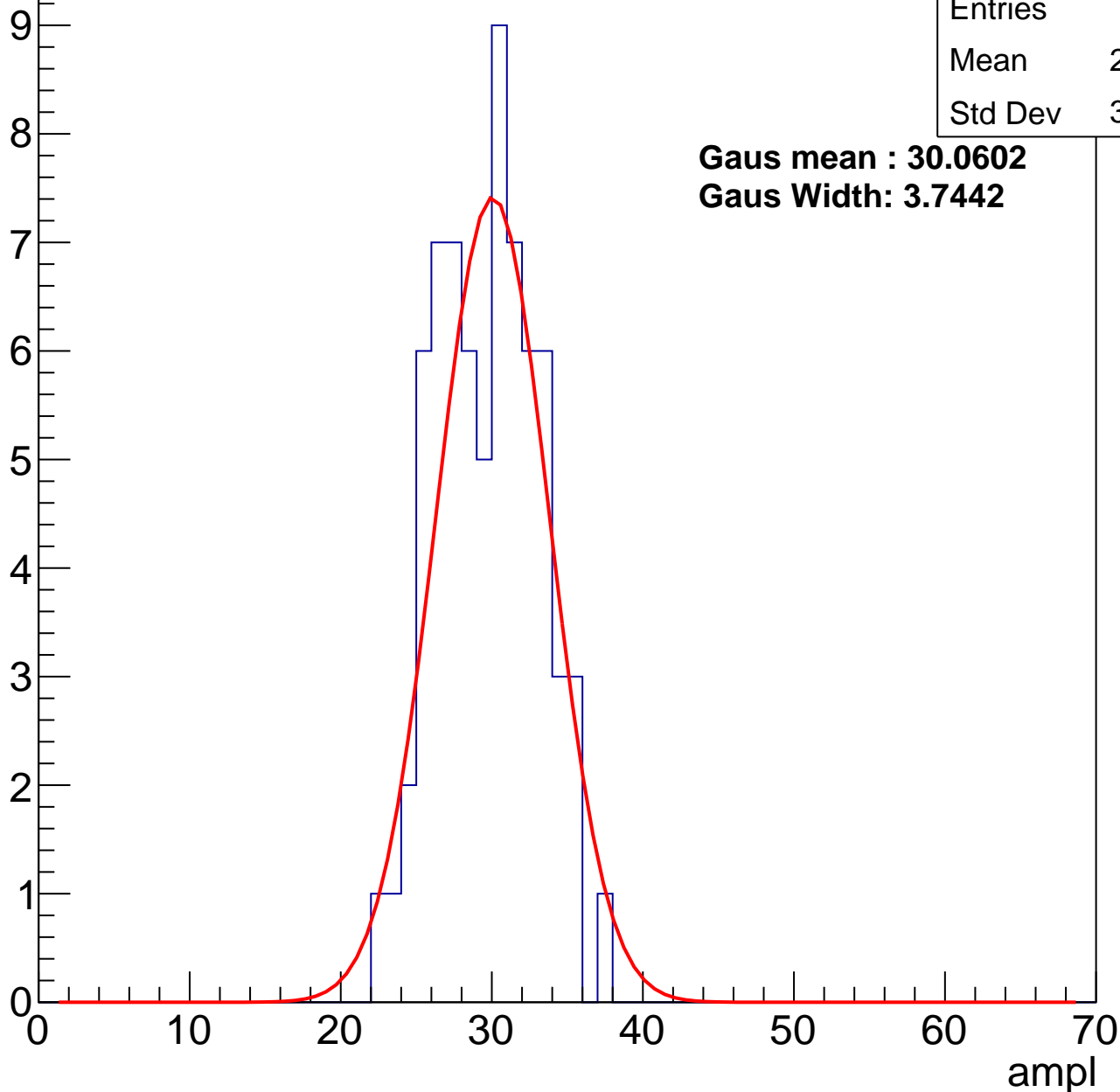
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	70
Mean	29.26
Std Dev	3.289

**Gaus mean : 30.0602**

**Gaus Width: 3.7442**



# B1L102S, U12-ch71, adc1

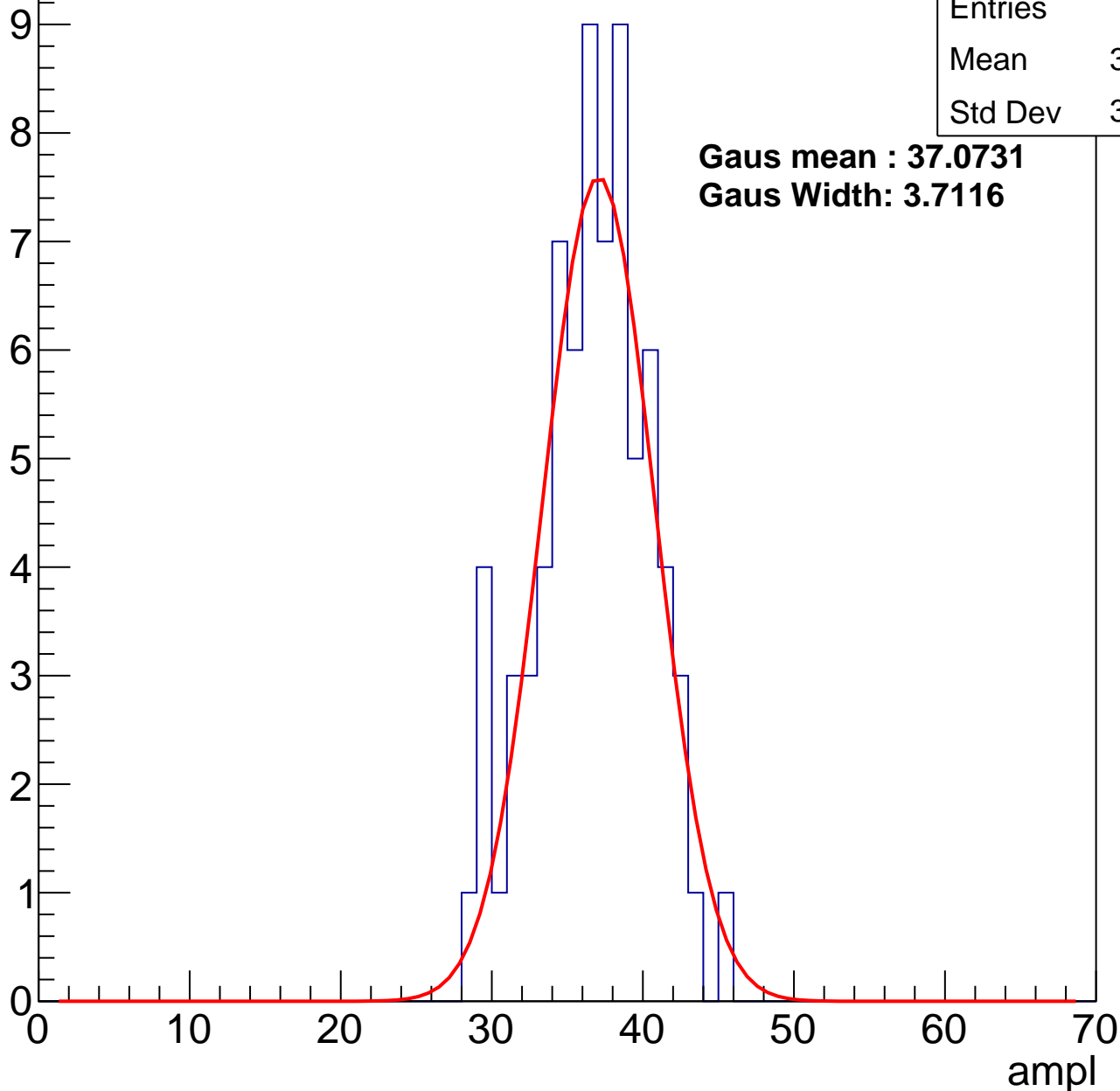
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	74
Mean	36.23
Std Dev	3.689

**Gaus mean : 37.0731**

**Gaus Width: 3.7116**



# B1L102S, U12-ch71, adc2

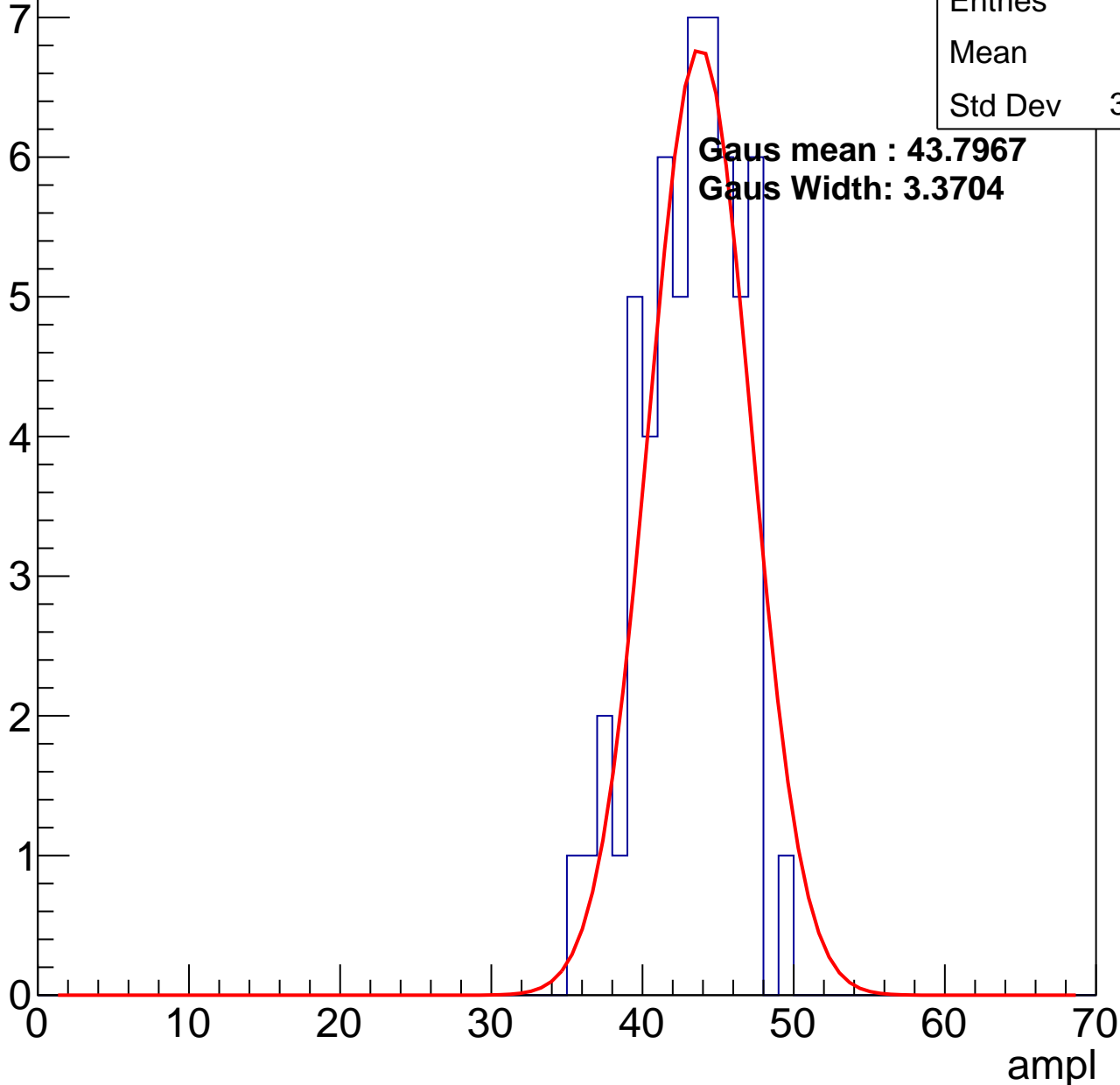
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	57
Mean	42.7
Std Dev	3.129

**Gaus mean : 43.7967**

**Gaus Width: 3.3704**



# B1L102S, U12-ch71, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

10  
8  
6  
4  
2  
0

Entries	64
Mean	48.81
Std Dev	3.132

0

10

20

30

40

50

60

70

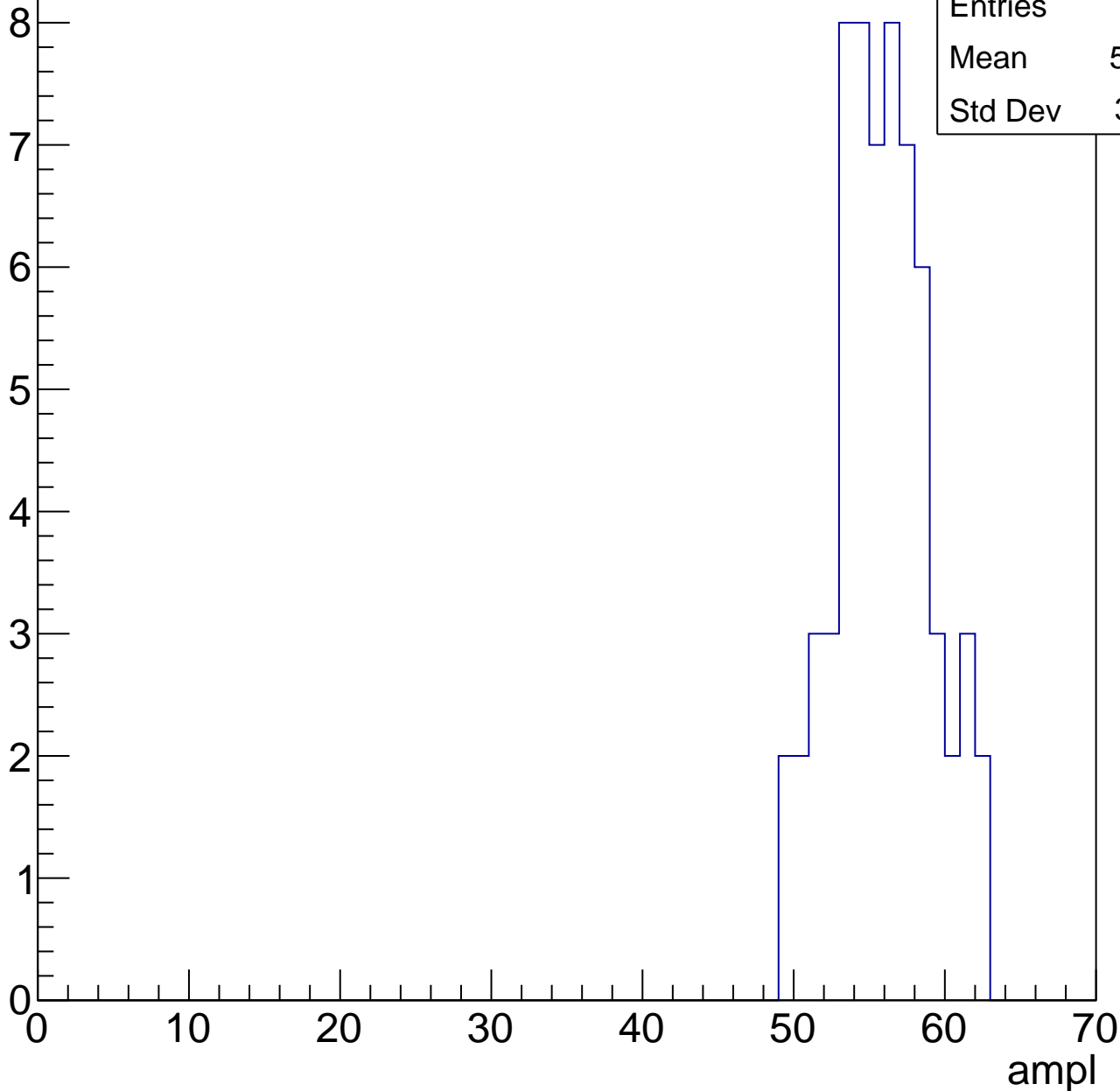
ampl

# B1L102S, U12-ch71, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	55.42
Std Dev	3.111

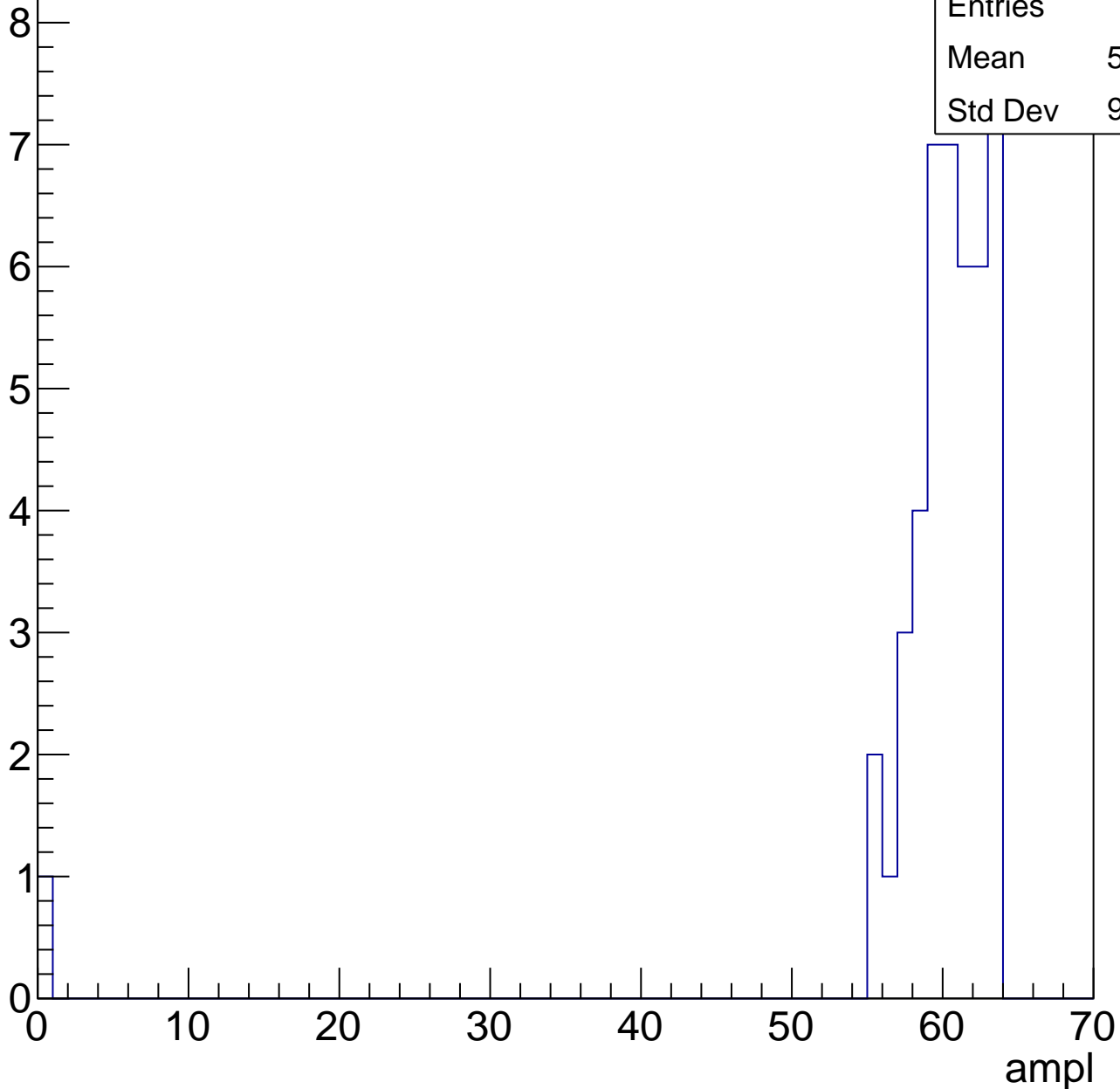


# B1L102S, U12-ch71, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	45
Mean	58.76
Std Dev	9.127



# B1L102S, U12-ch71, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

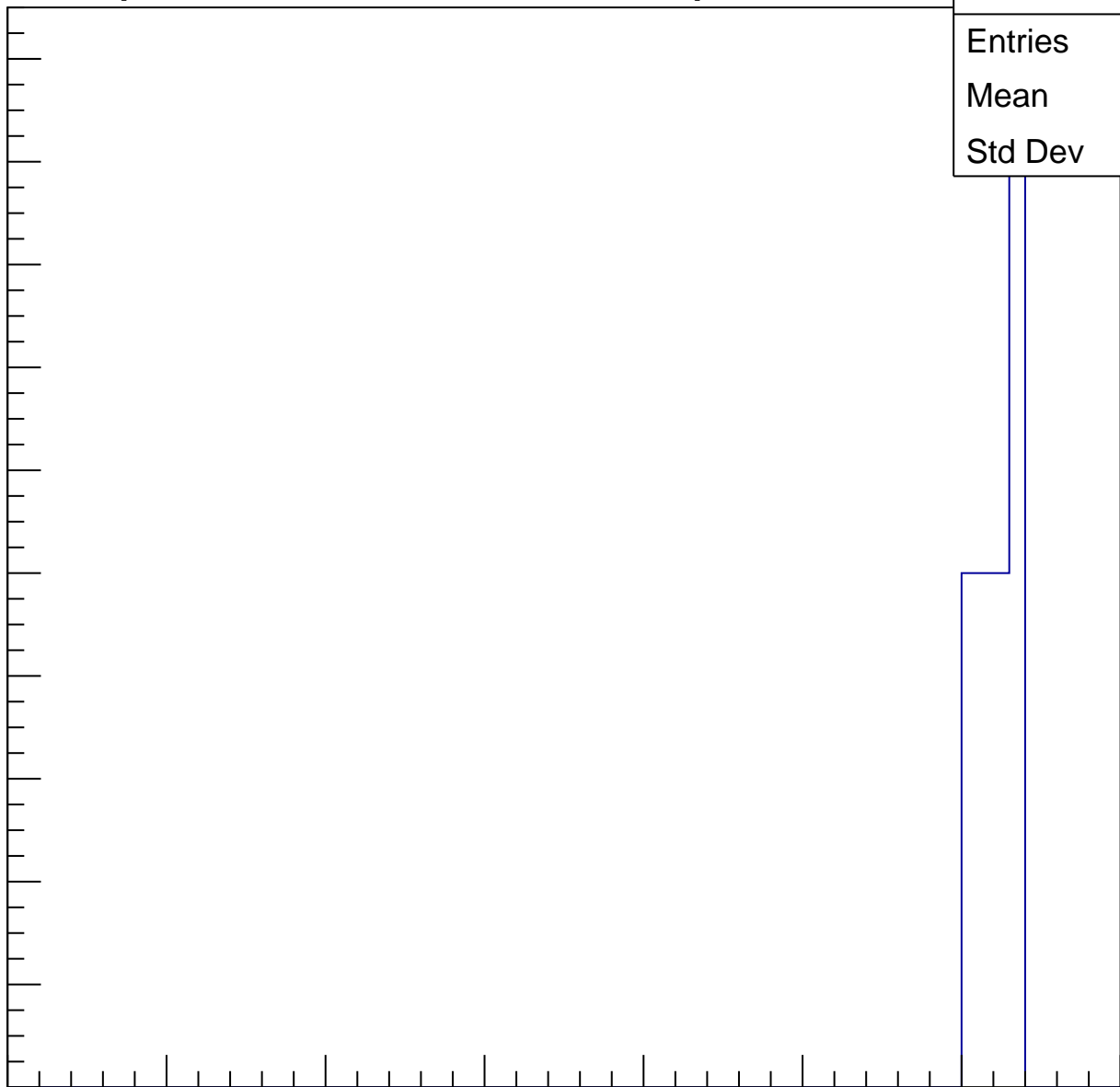
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	5
Mean	61.8
Std Dev	1.166

0 10 20 30 40 50 60 70

ampl

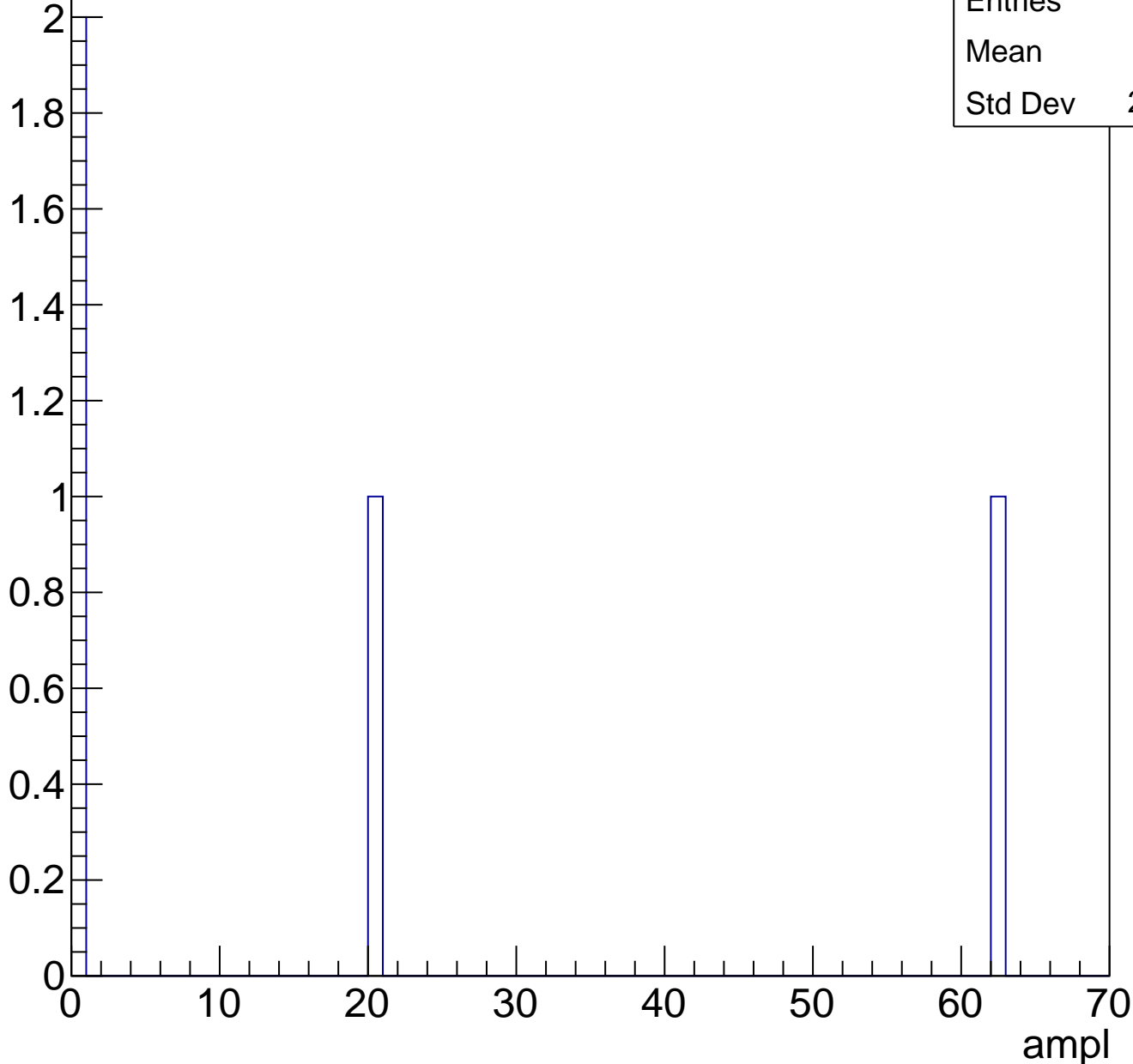




# B1L102S, U12-ch71, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	4
Mean	20.5
Std Dev	25.31

# B1L102S, U12-ch72, adc0

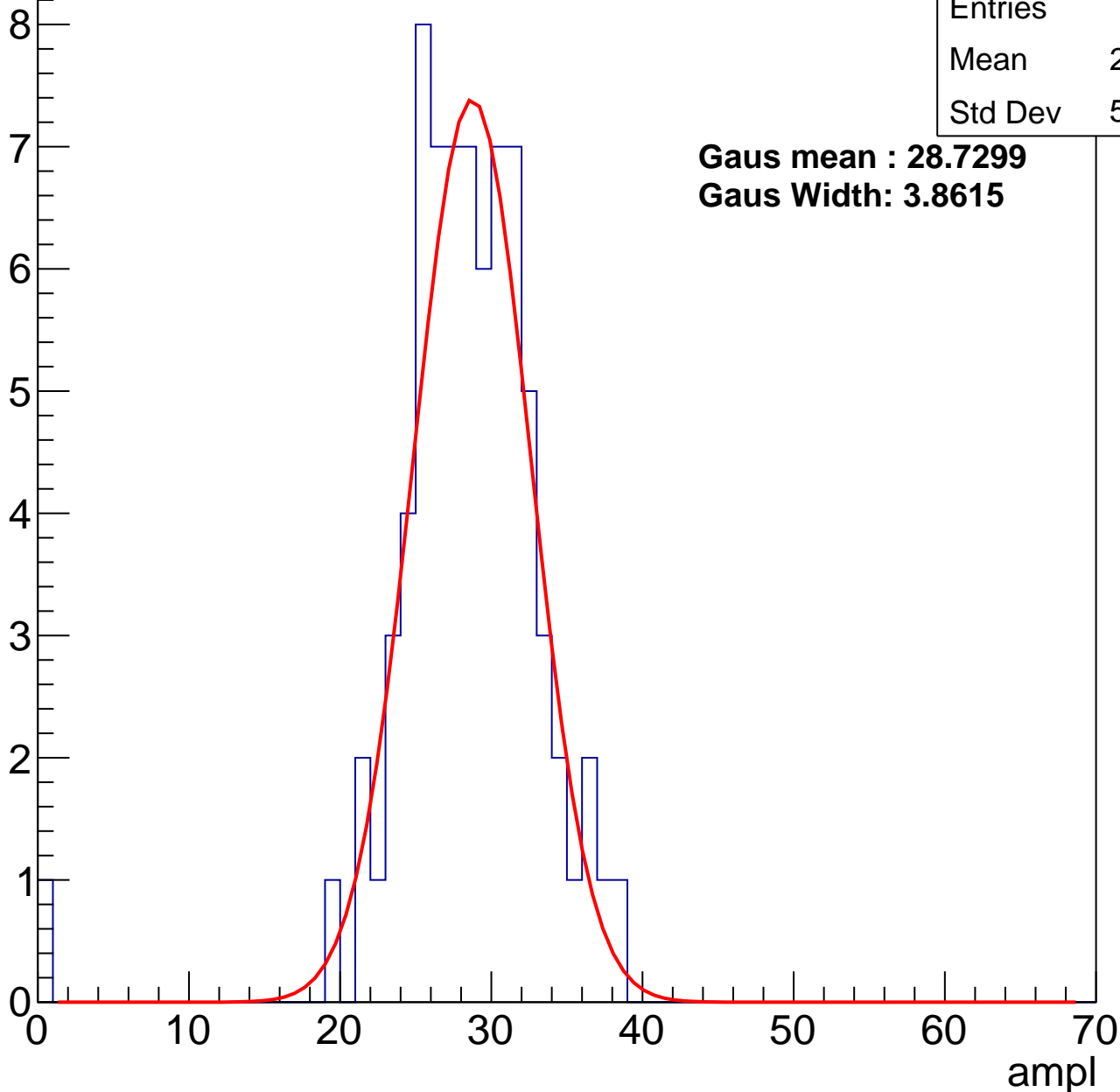
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	76
Mean	27.96
Std Dev	5.035

**Gaus mean : 28.7299**

**Gaus Width: 3.8615**



# B1L102S, U12-ch72, adc1

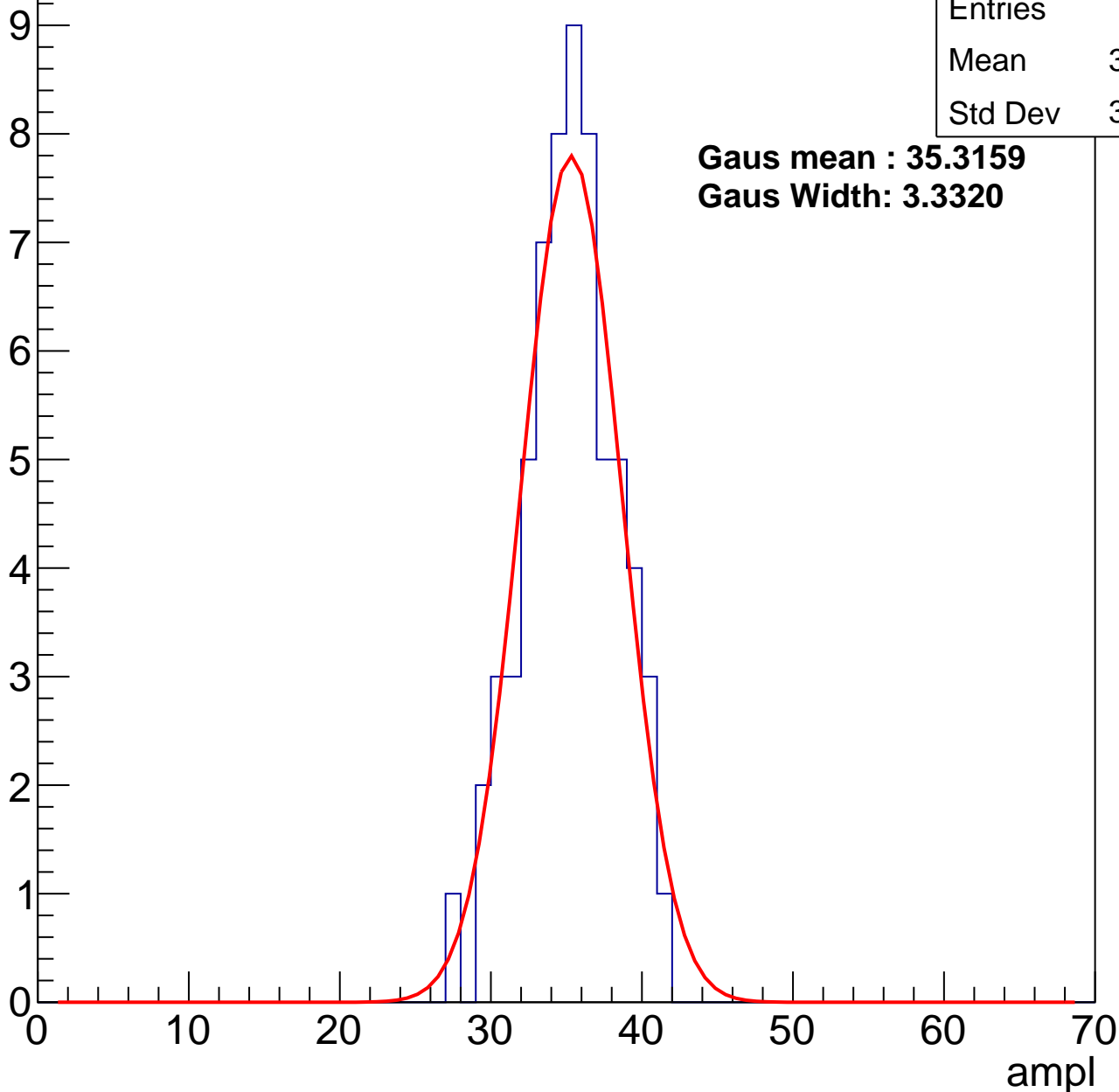
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	34.78
Std Dev	3.023

**Gaus mean : 35.3159**

**Gaus Width: 3.3320**



# B1L102S, U12-ch72, adc2

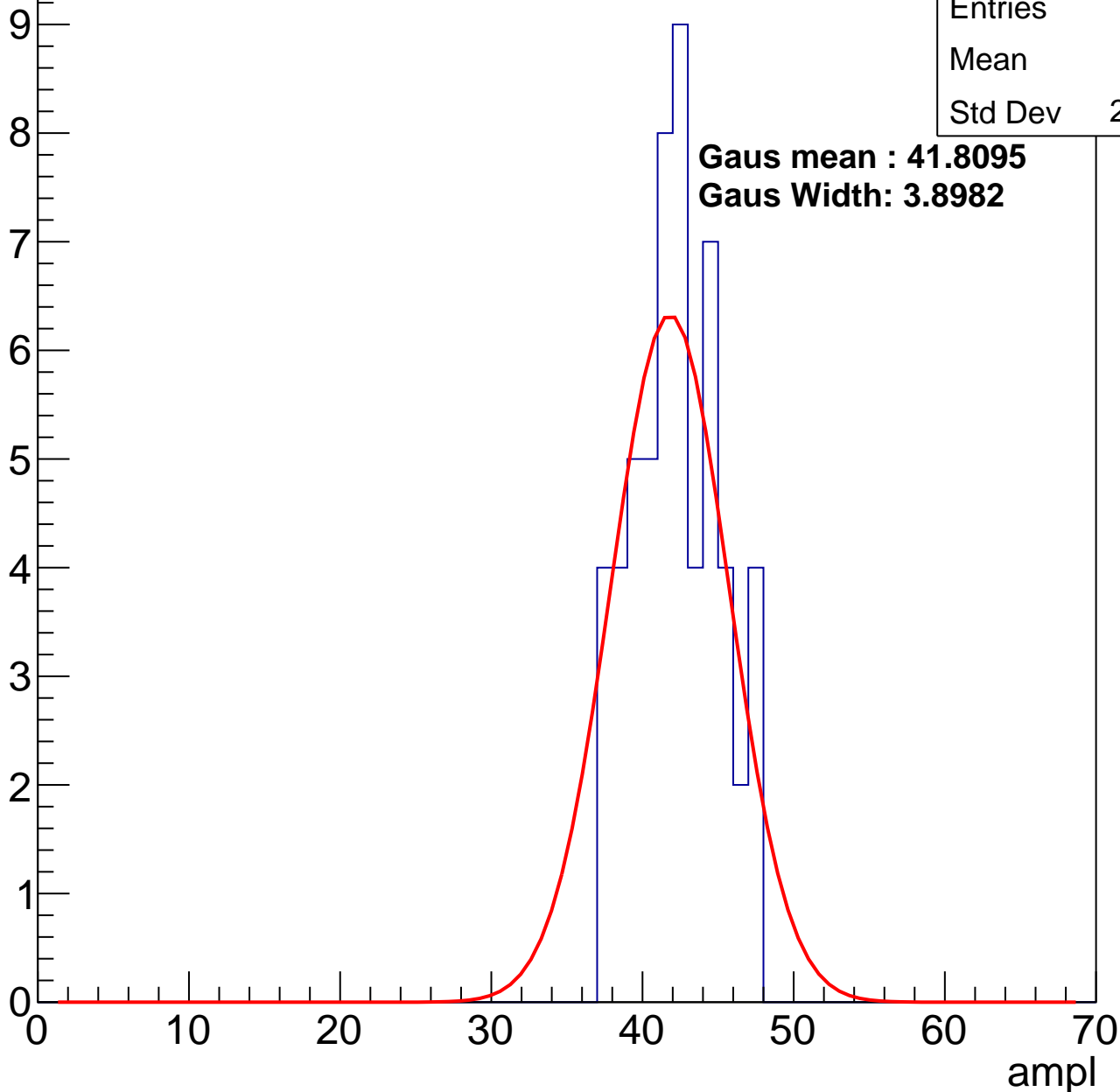
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	56
Mean	41.8
Std Dev	2.787

**Gaus mean : 41.8095**

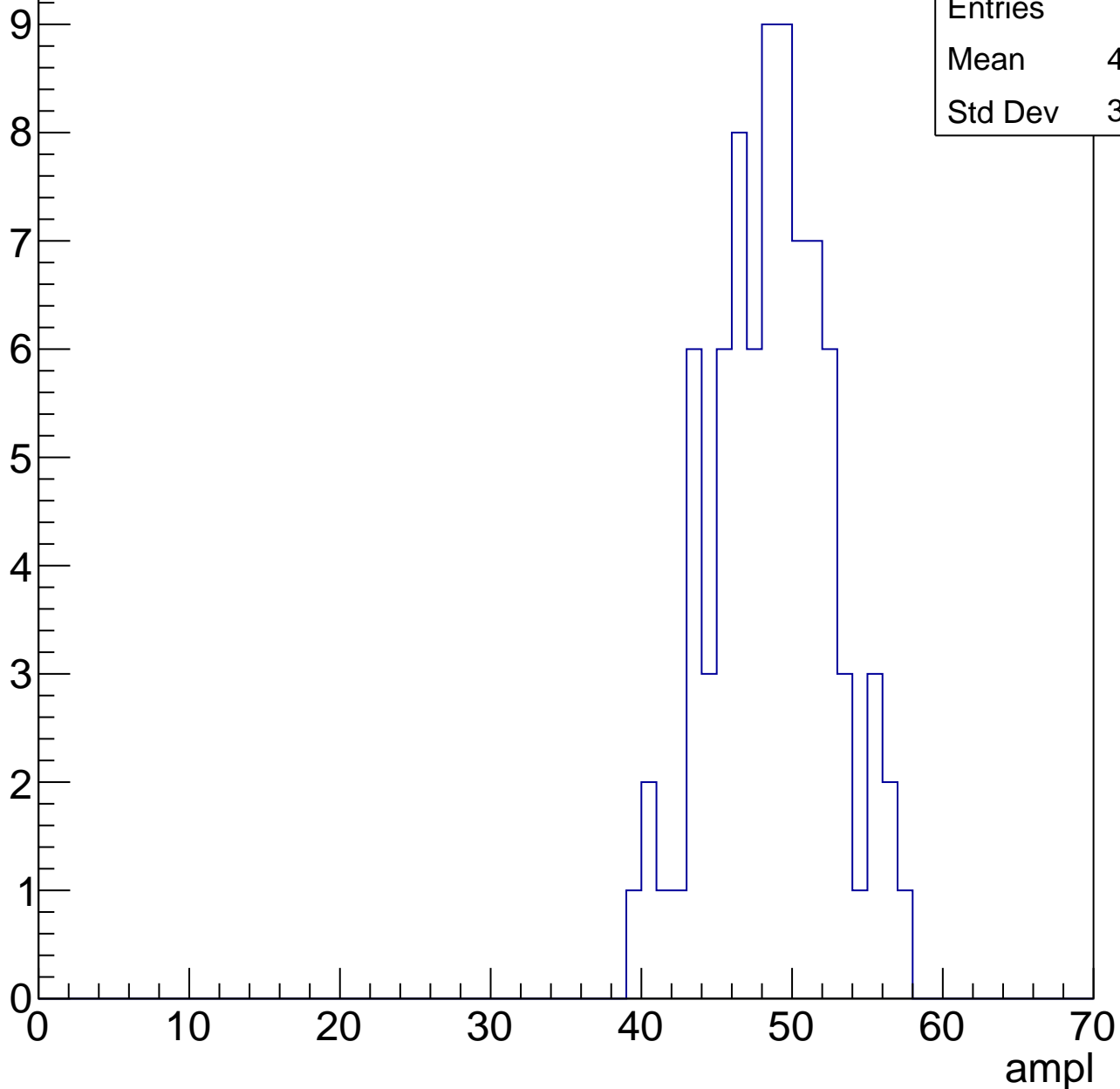
**Gaus Width: 3.8982**



# B1L102S, U12-ch72, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	82
Mean	48.18
Std Dev	3.895

# B1L102S, U12-ch72, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

7

6

5

4

3

2

1

0

Entries 43

Mean 53.98

Std Dev 2.601

0

10

20

30

40

50

60

ampl

0

10

20

30

40

50

60

70

# B1L102S, U12-ch72, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	57
Mean	59.25
Std Dev	2.515

Entry

10

8

6

4

2

0

0

10

20

30

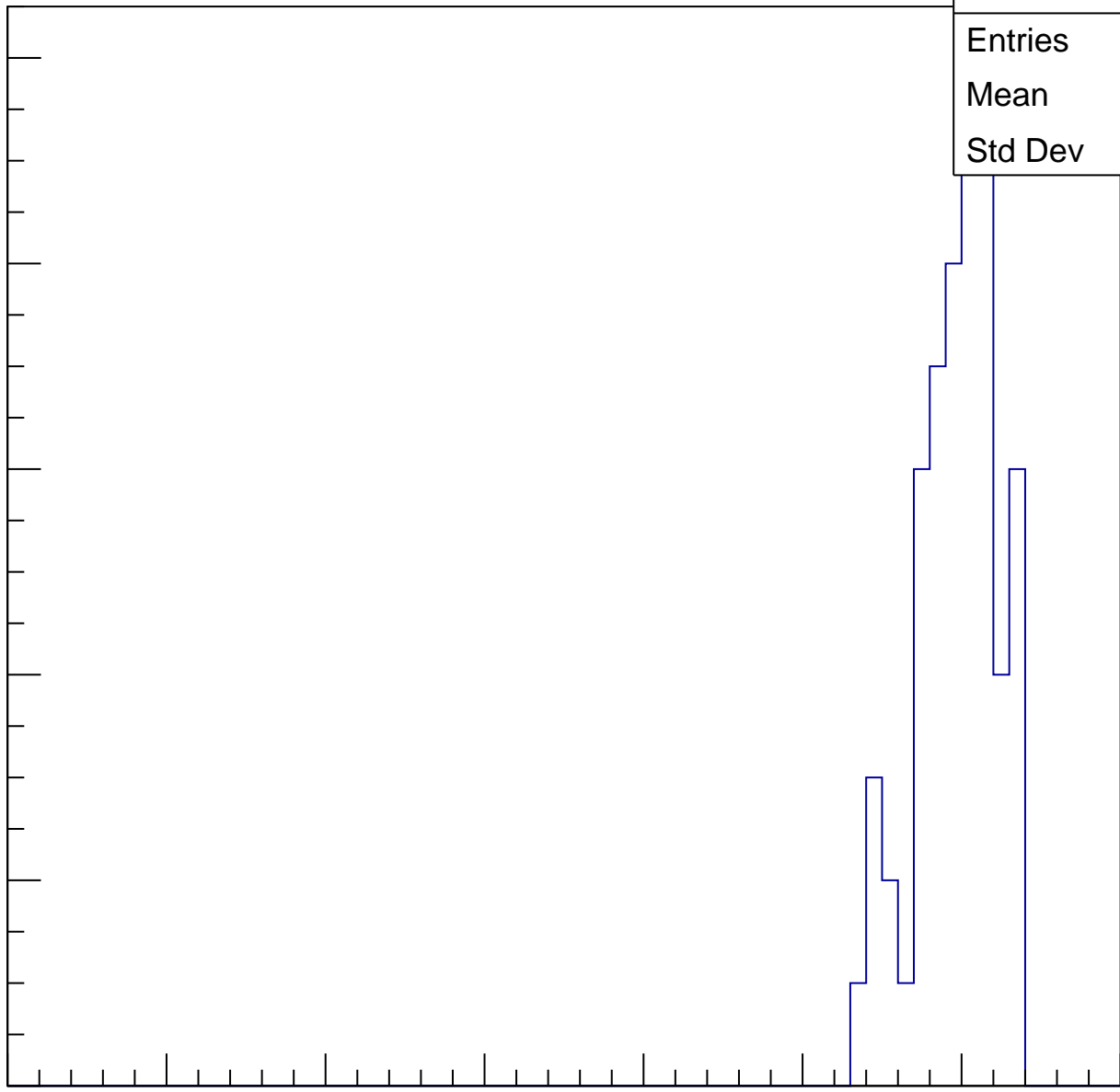
40

50

60

70

ampl

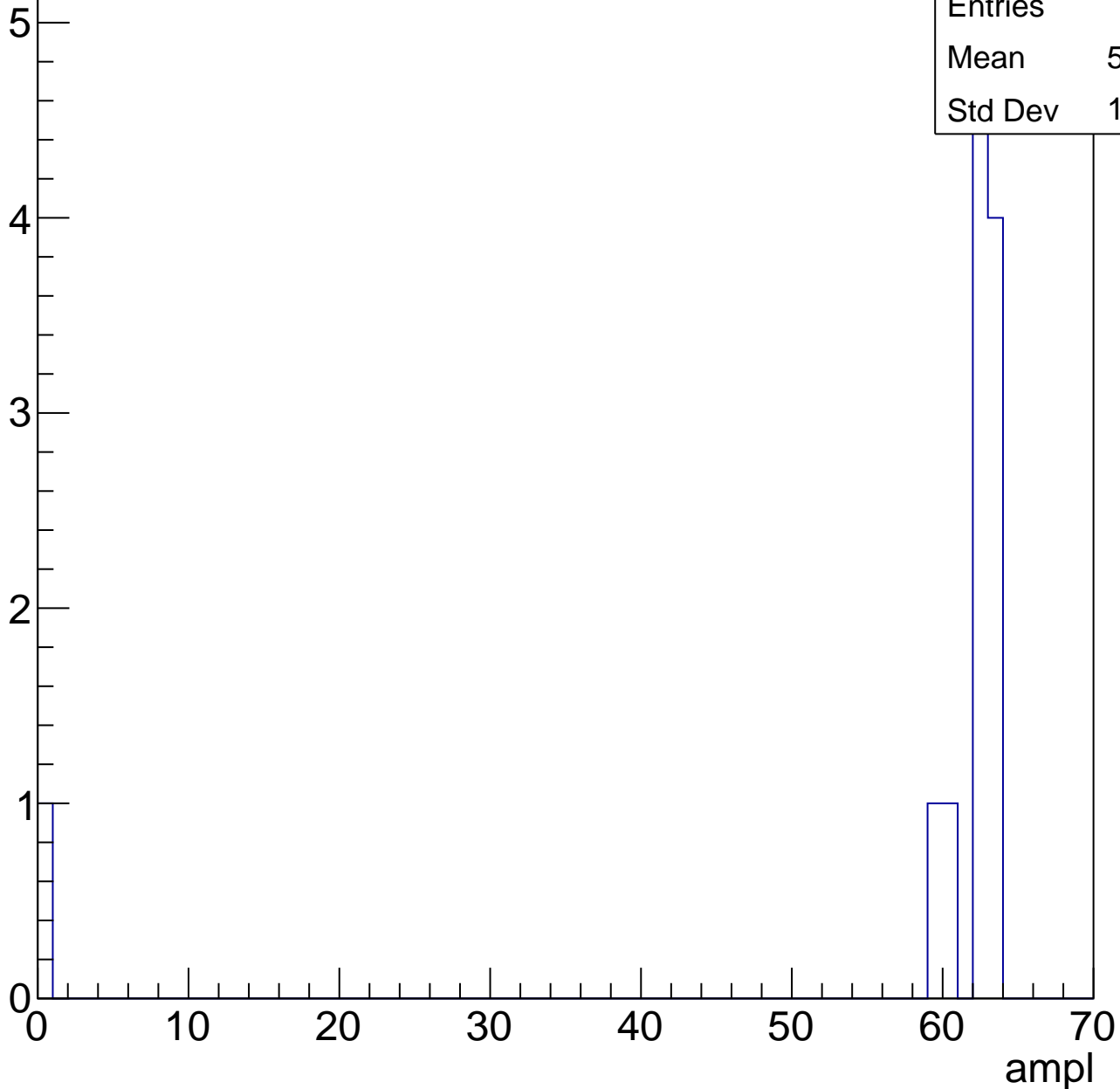


# B1L102S, U12-ch72, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	12
Mean	56.75
Std Dev	17.15





# B1L102S, U12-ch72, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U12-ch73, adc0

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	74
Mean	29.36
Std Dev	3.253

**Gaus mean : 29.8421**

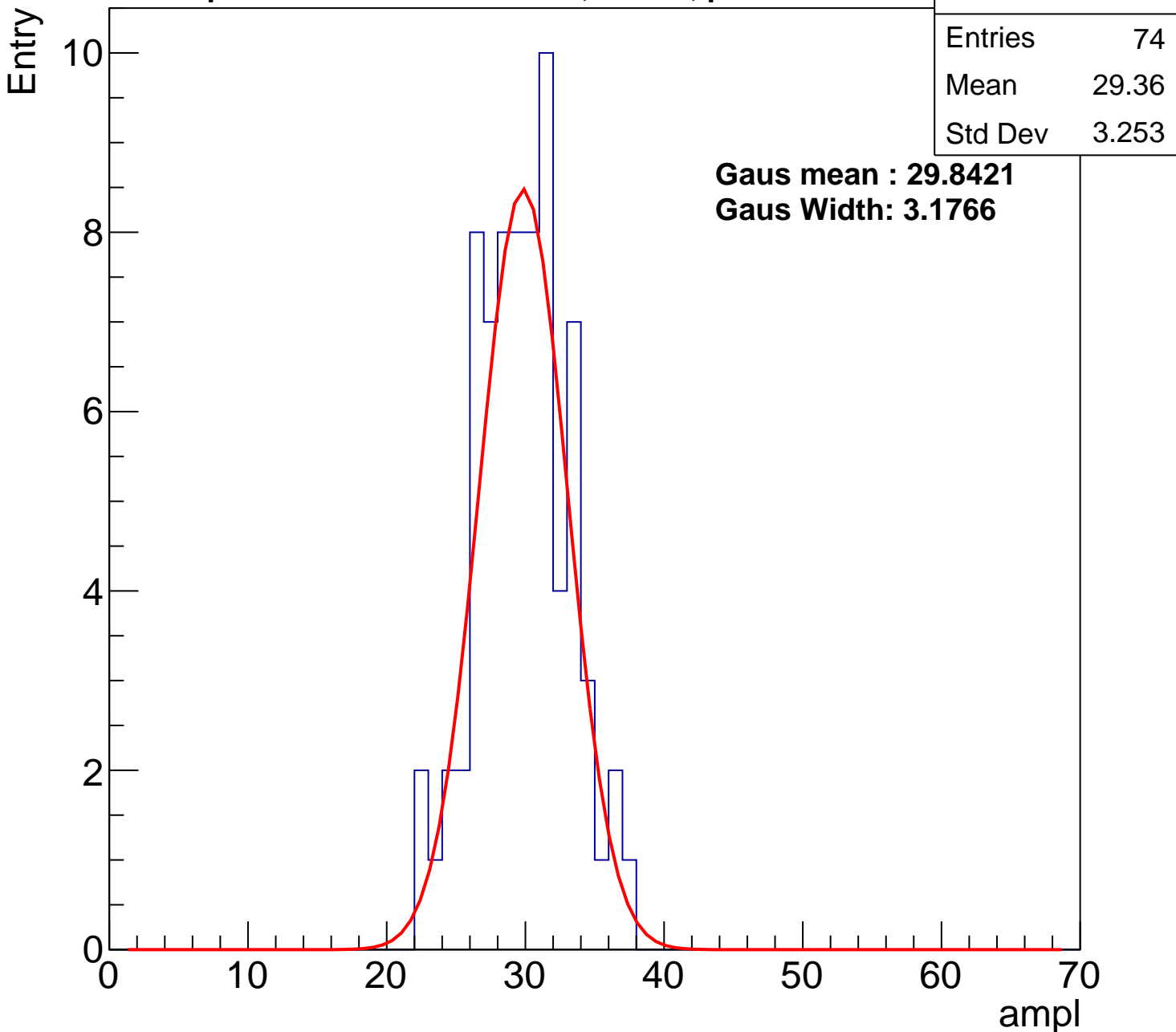
**Gaus Width: 3.1766**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L102S, U12-ch73, adc1

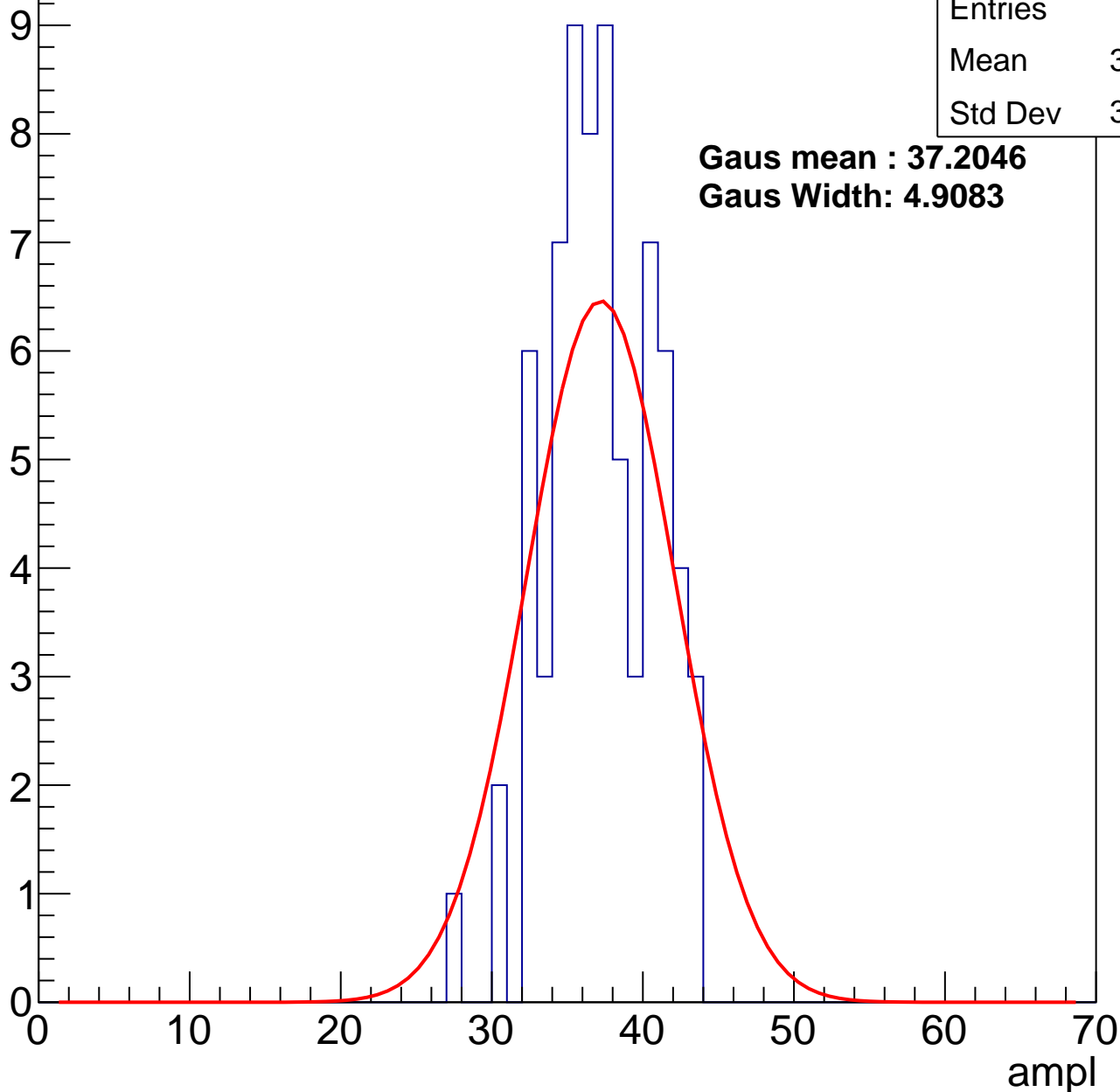
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	73
Mean	36.74
Std Dev	3.476

**Gaus mean : 37.2046**

**Gaus Width: 4.9083**



# B1L102S, U12-ch73, adc2

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	69
Mean	43.91
Std Dev	3.772

**Gaus mean : 43.5853**

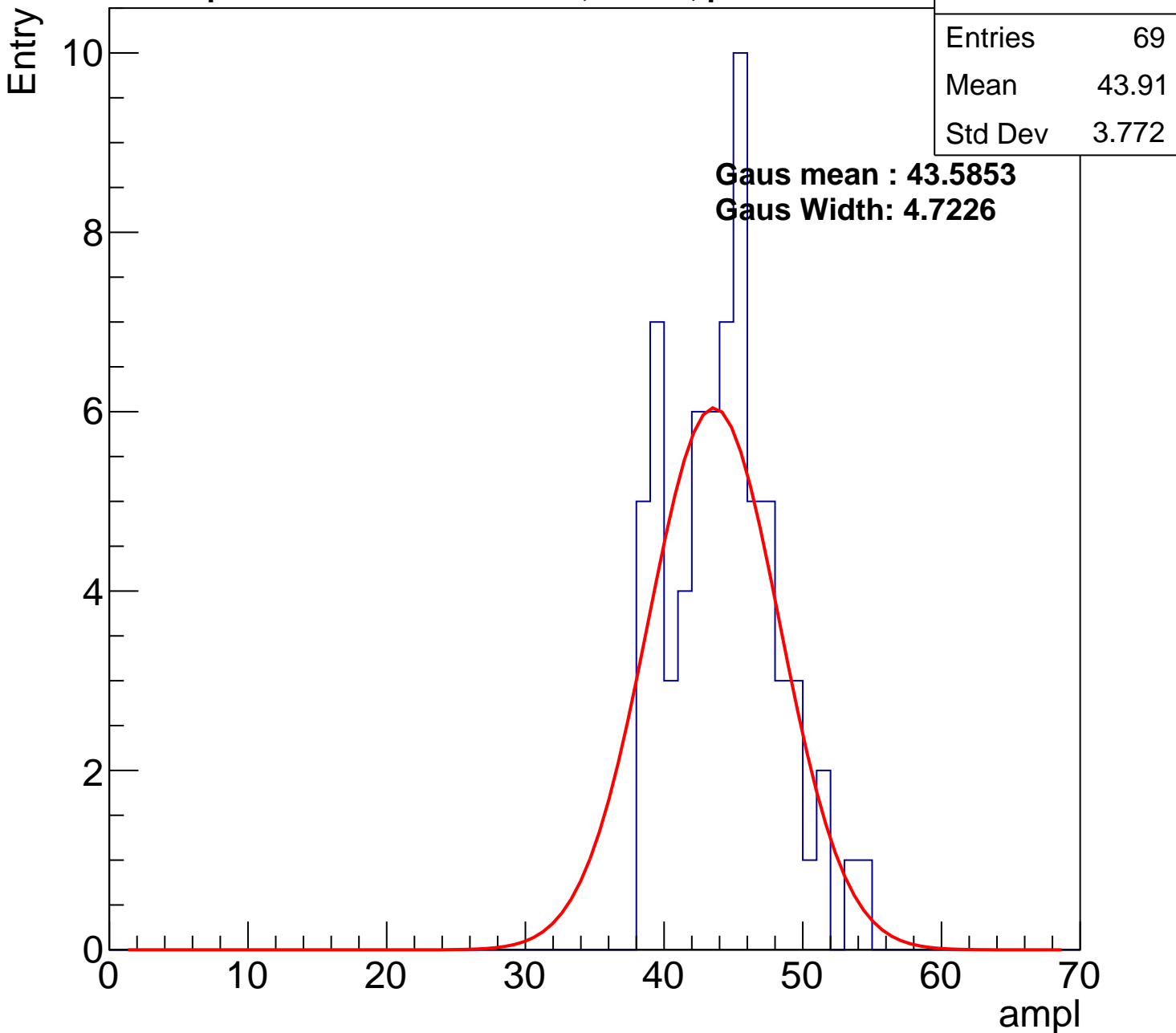
**Gaus Width: 4.7226**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

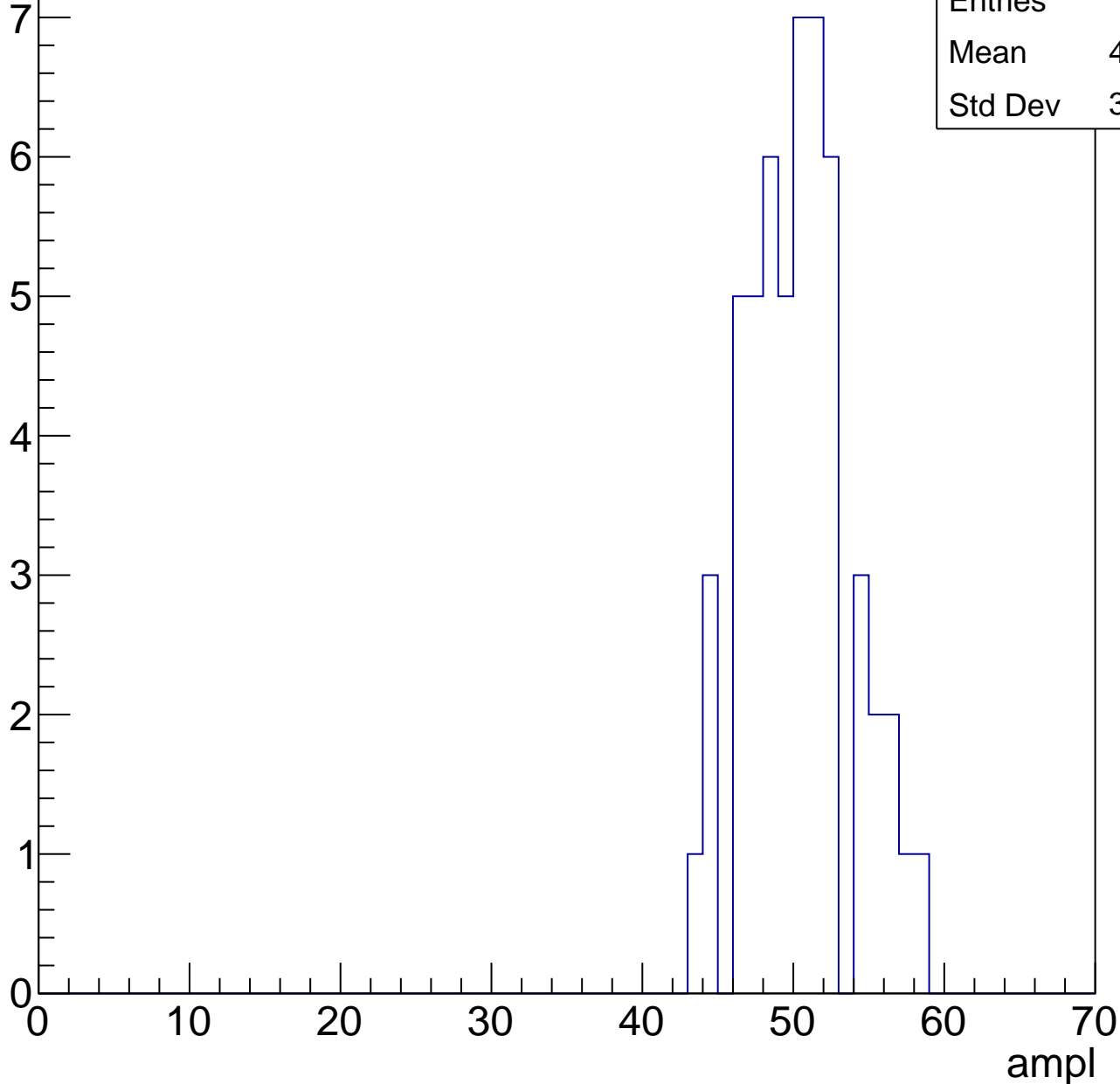


# B1L102S, U12-ch73, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

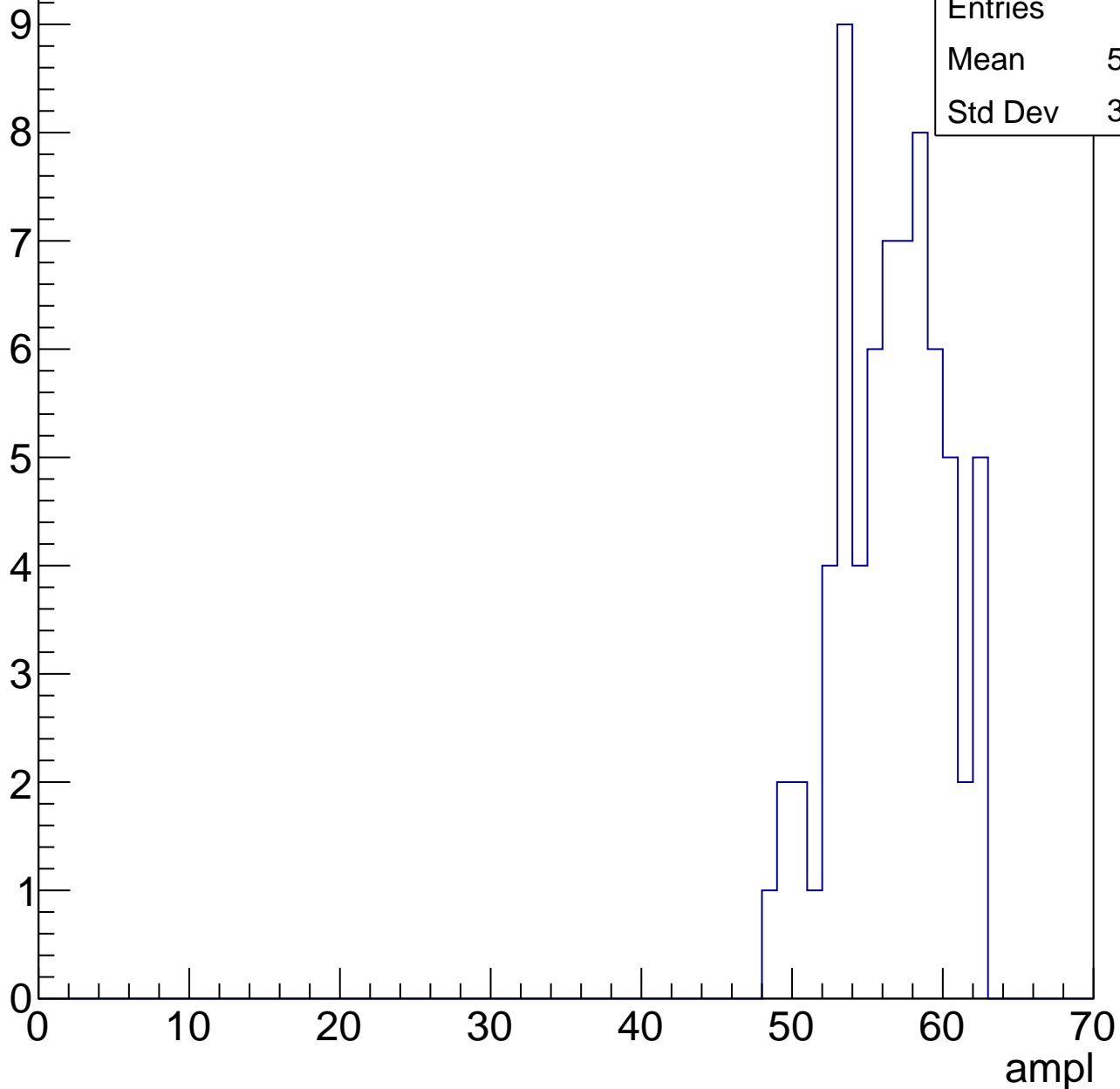
Entries	54
Mean	49.83
Std Dev	3.398



# B1L102S, U12-ch73, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	69
Mean	56.07
Std Dev	3.465

# B1L102S, U12-ch73, adc5

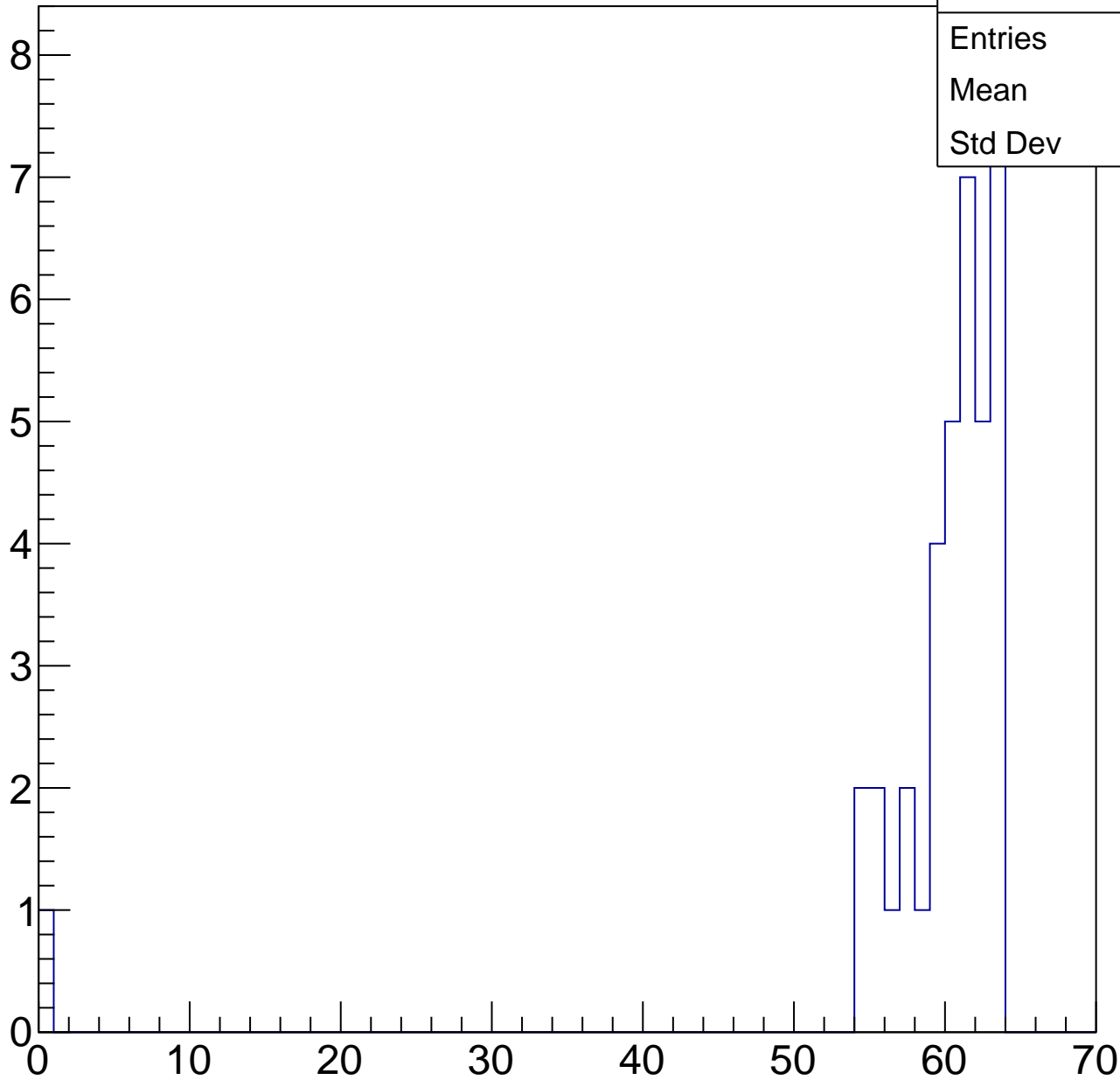
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	38
Mean	58.5
Std Dev	9.97

ampl



# B1L102S, U12-ch73, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U12-ch73, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L102S, U12-ch74, adc0

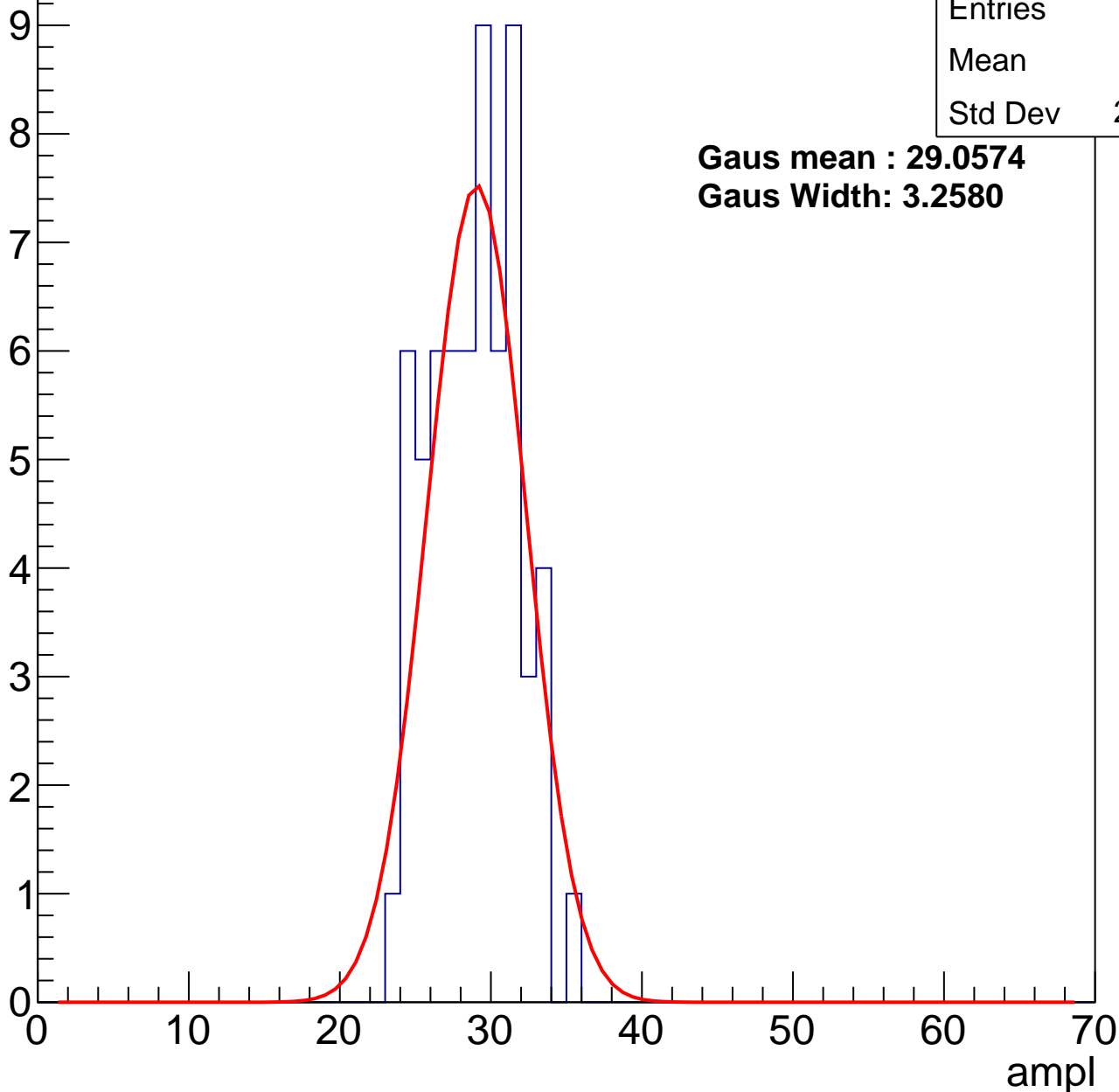
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	62
Mean	28.4
Std Dev	2.831

**Gaus mean : 29.0574**

**Gaus Width: 3.2580**



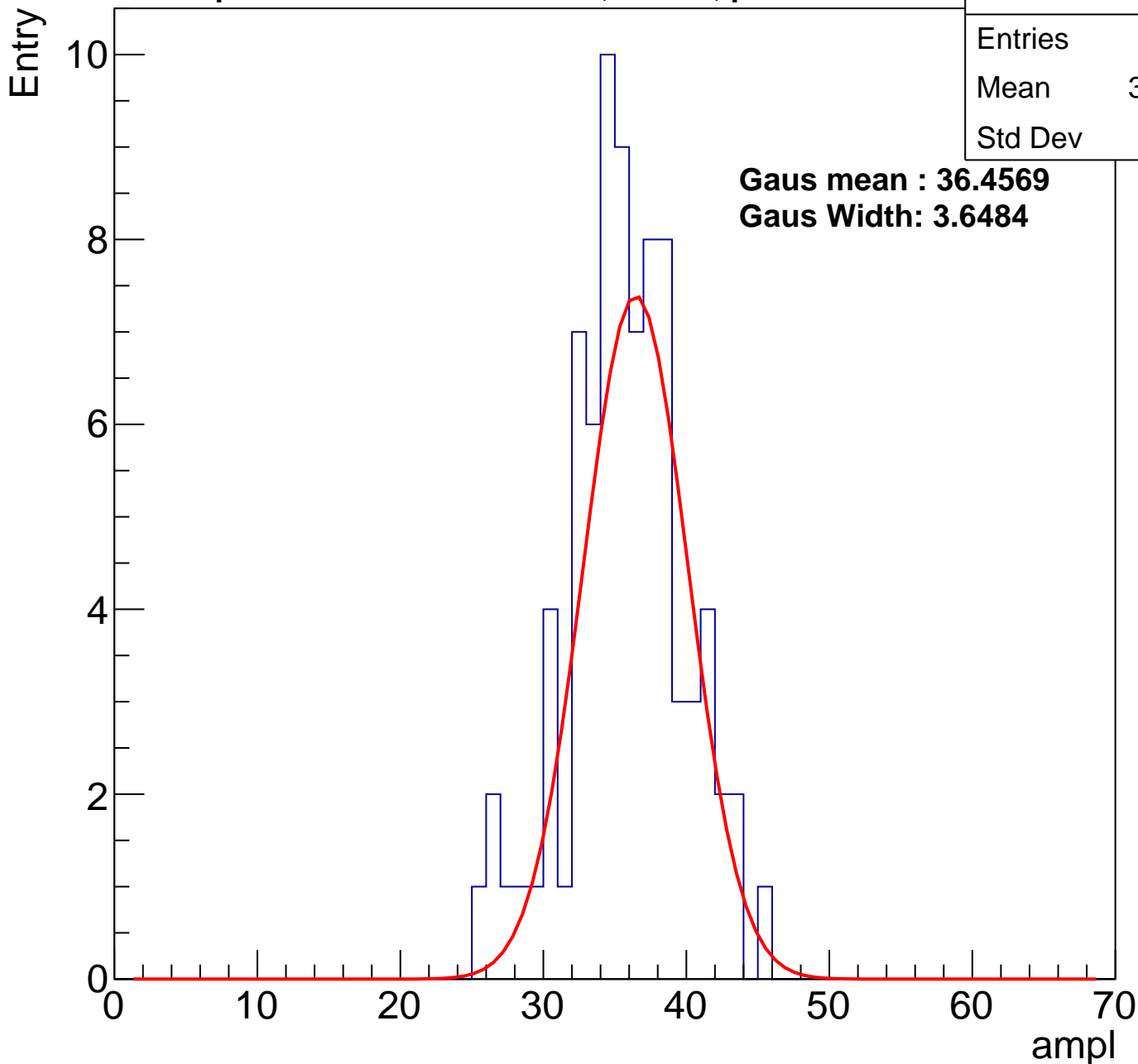
# B1L102S, U12-ch74, adc1

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	81
Mean	35.27
Std Dev	4.04

**Gaus mean : 36.4569**

**Gaus Width: 3.6484**



# B1L102S, U12-ch74, adc2

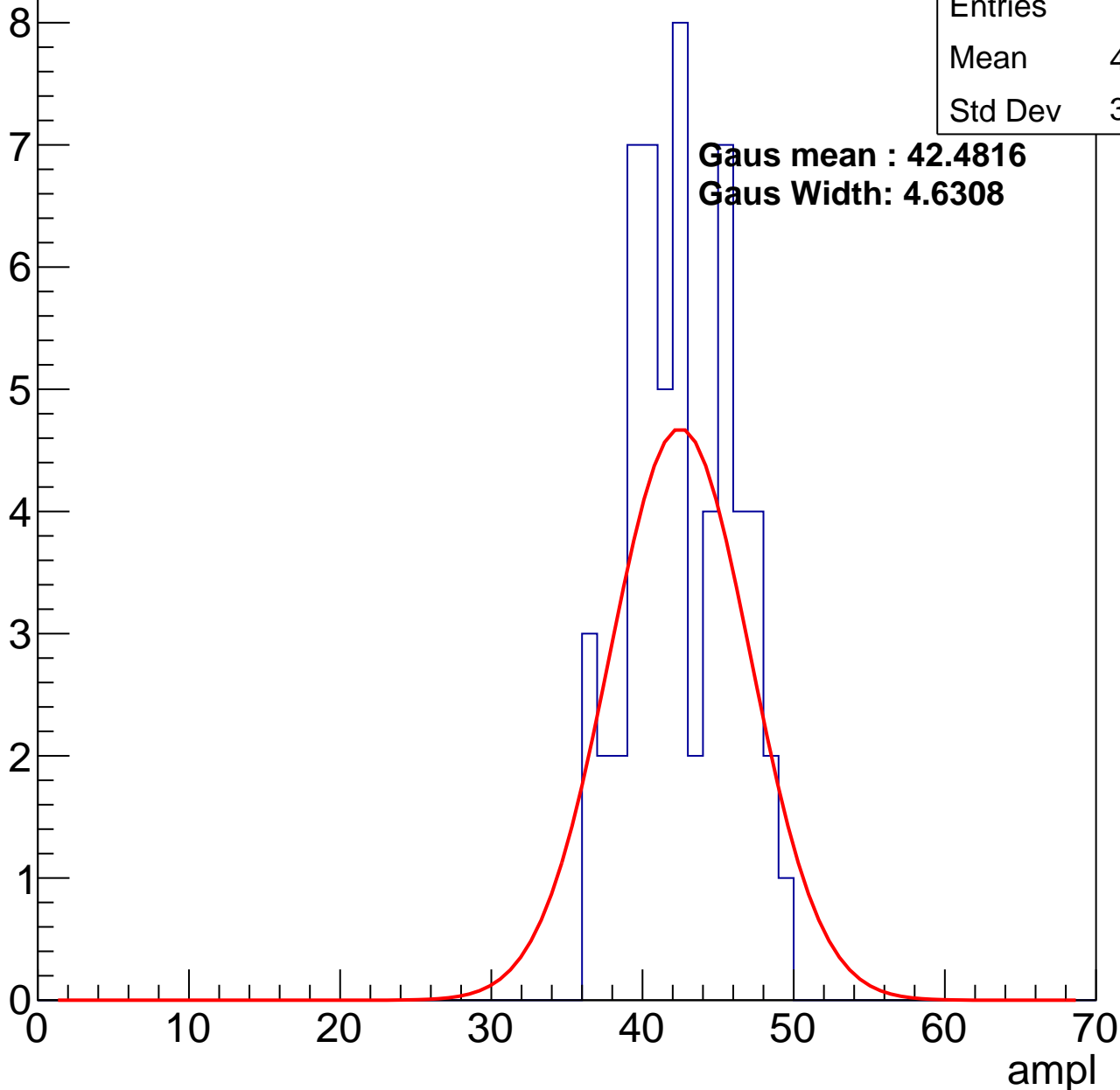
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	58
Mean	42.17
Std Dev	3.348

**Gaus mean : 42.4816**

**Gaus Width: 4.6308**

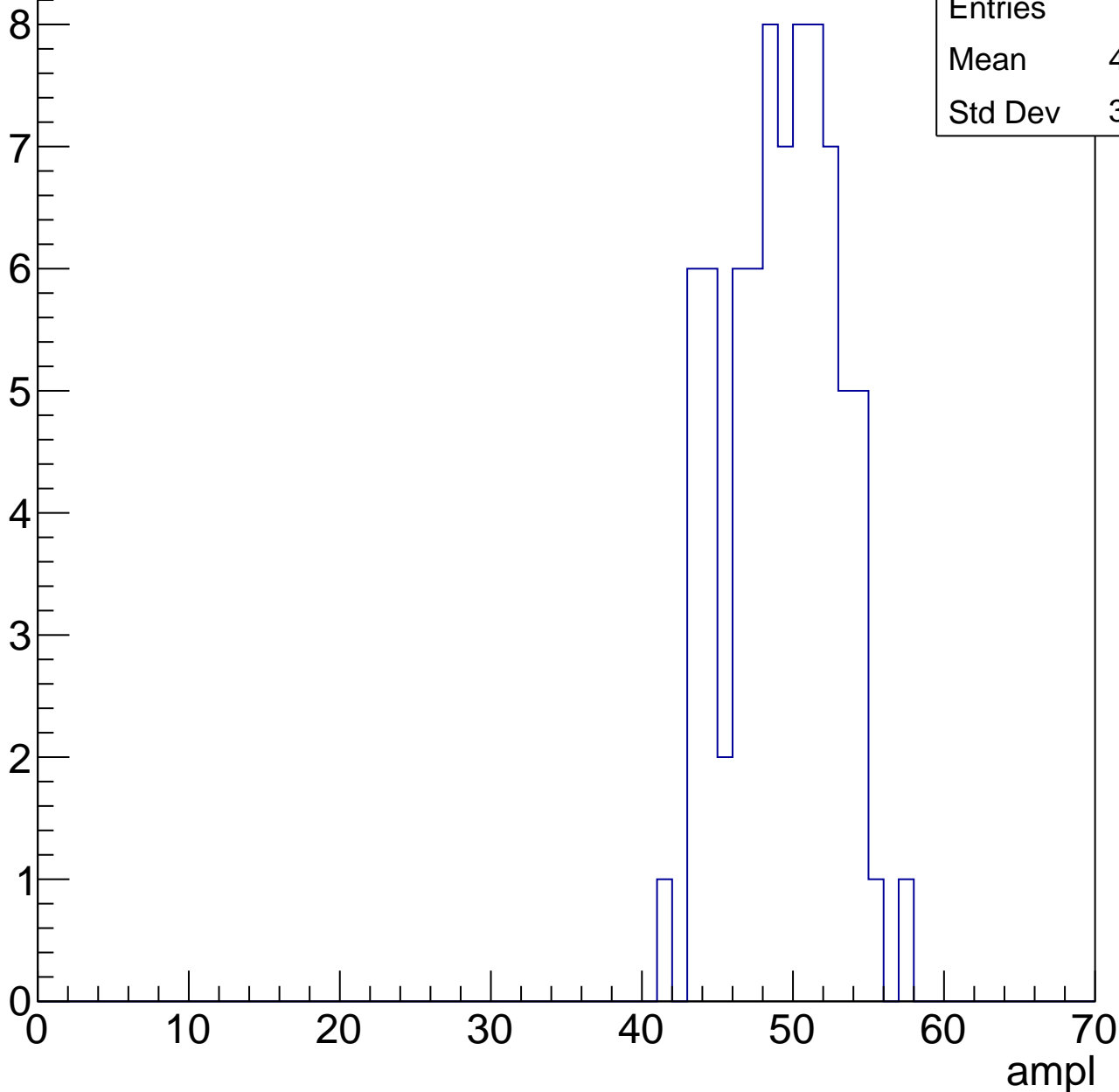


# B1L102S, U12-ch74, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	77
Mean	48.79
Std Dev	3.517



# B1L102S, U12-ch74, adc4

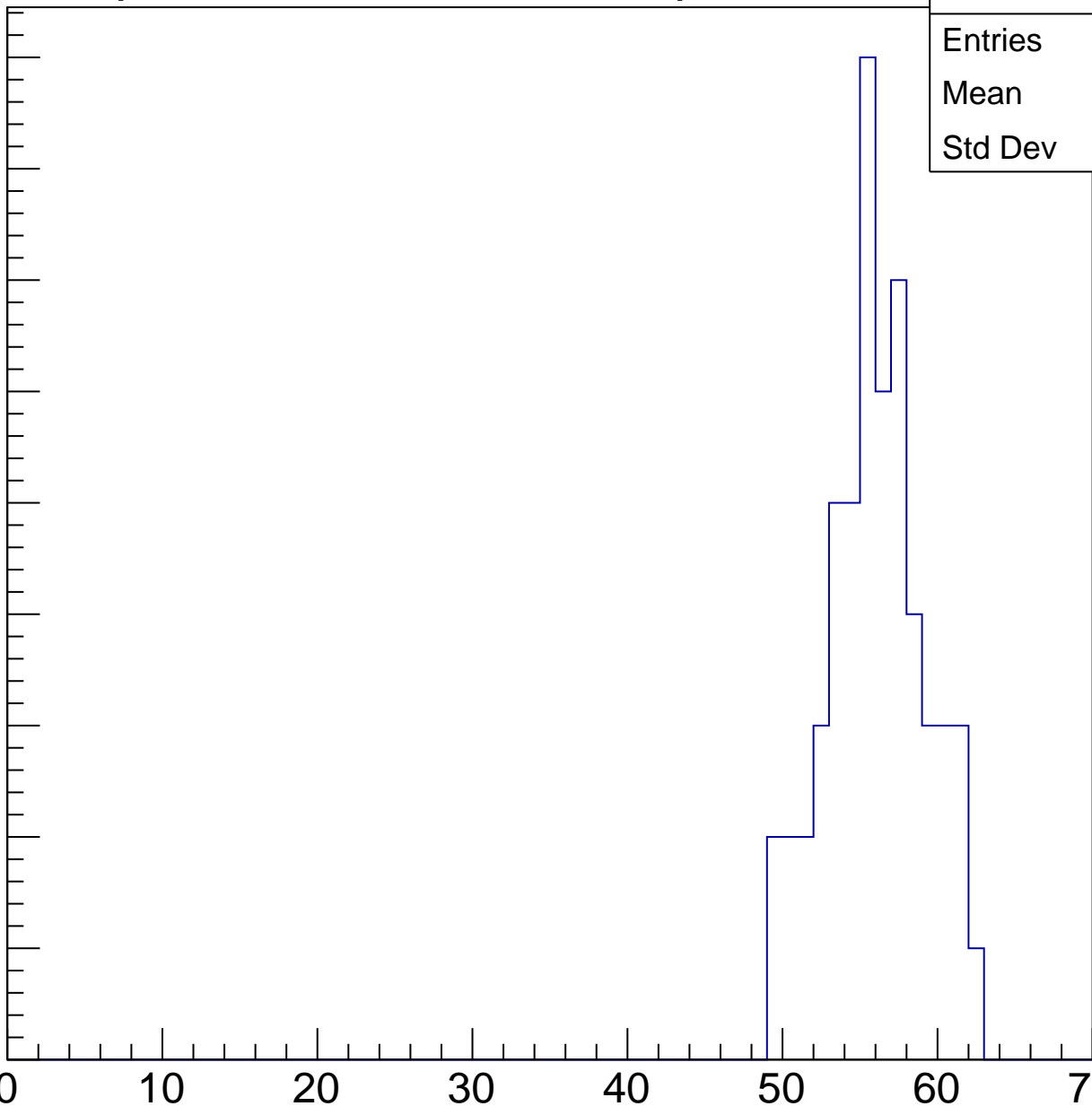
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	55
Mean	55.55
Std Dev	3.132

ampl

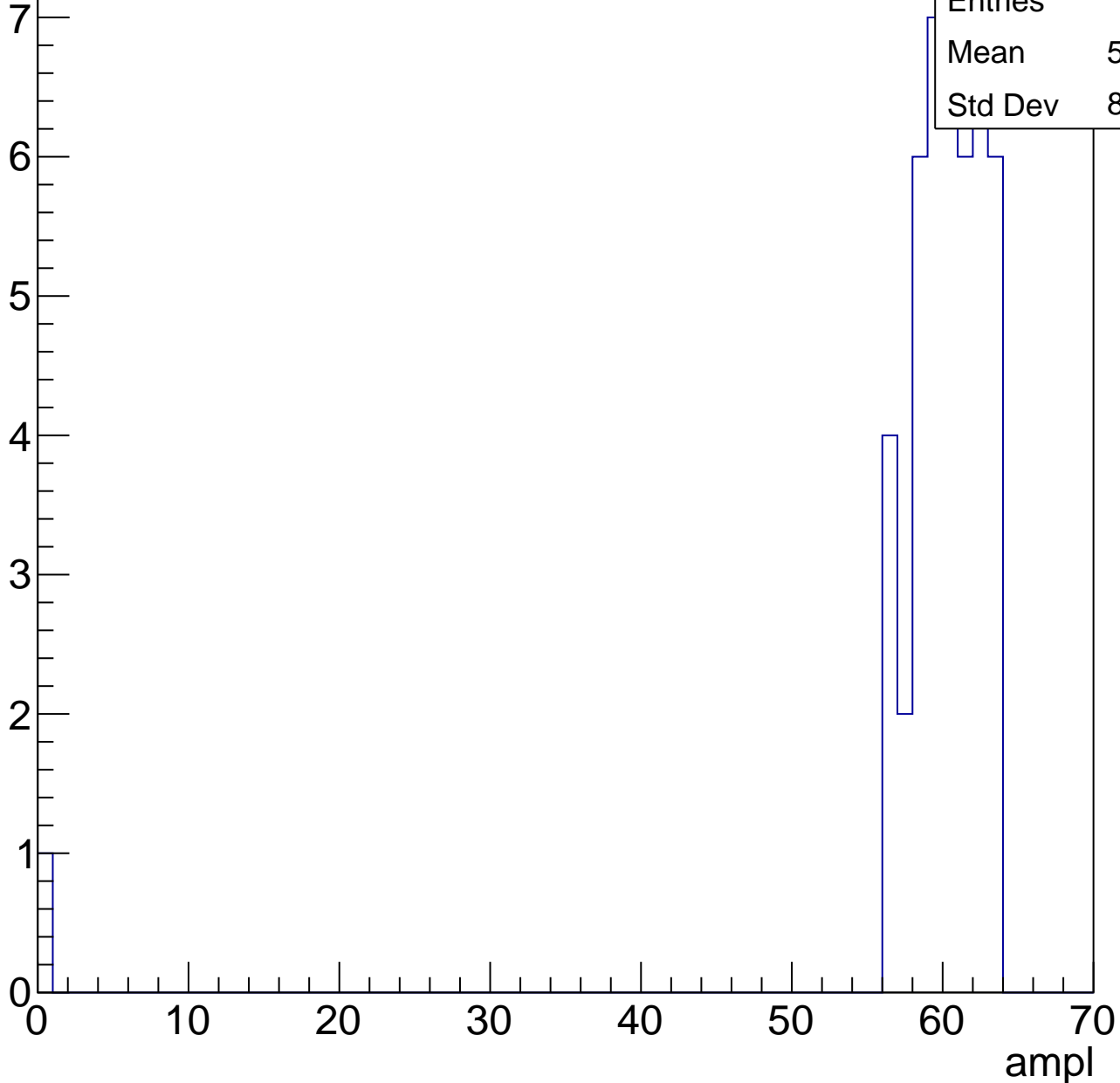


# B1L102S, U12-ch74, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	46
Mean	58.63
Std Dev	8.986



# B1L102S, U12-ch74, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U12-ch74, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U12-ch75, adc0

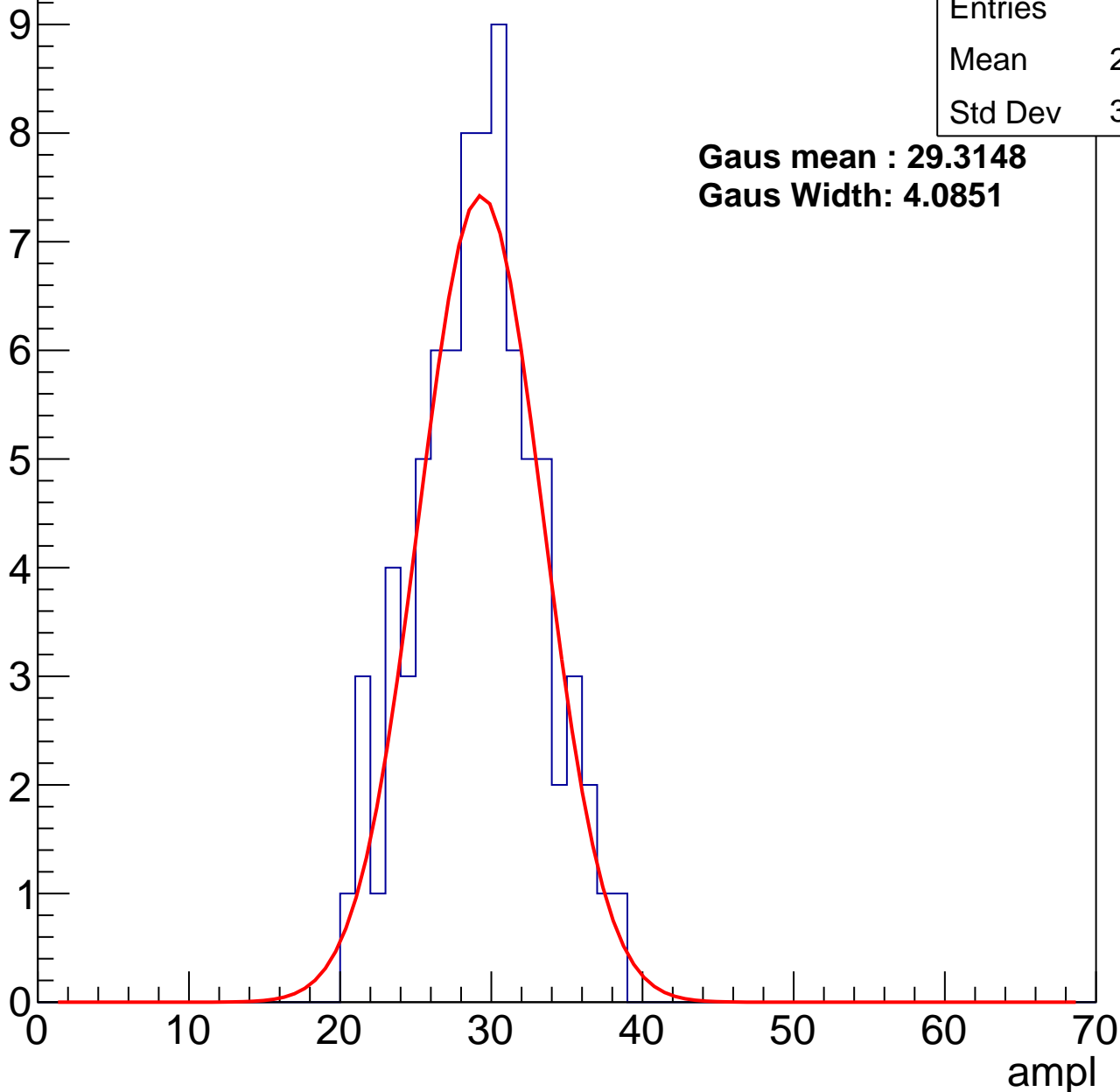
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	79
Mean	28.72
Std Dev	3.993

**Gaus mean : 29.3148**

**Gaus Width: 4.0851**



# B1L102S, U12-ch75, adc1

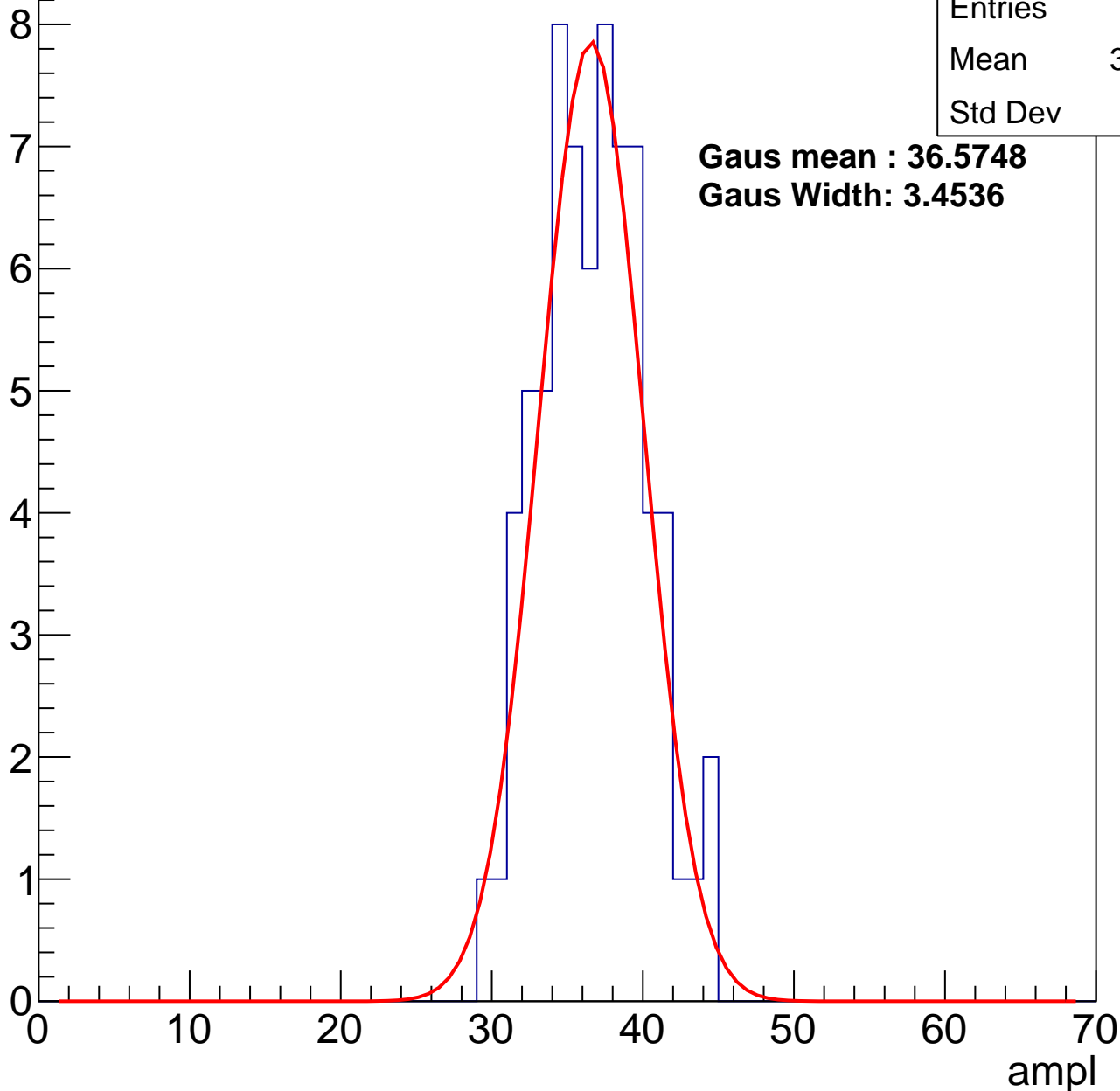
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	71
Mean	36.24
Std Dev	3.4

**Gaus mean : 36.5748**

**Gaus Width: 3.4536**



# B1L102S, U12-ch75, adc2

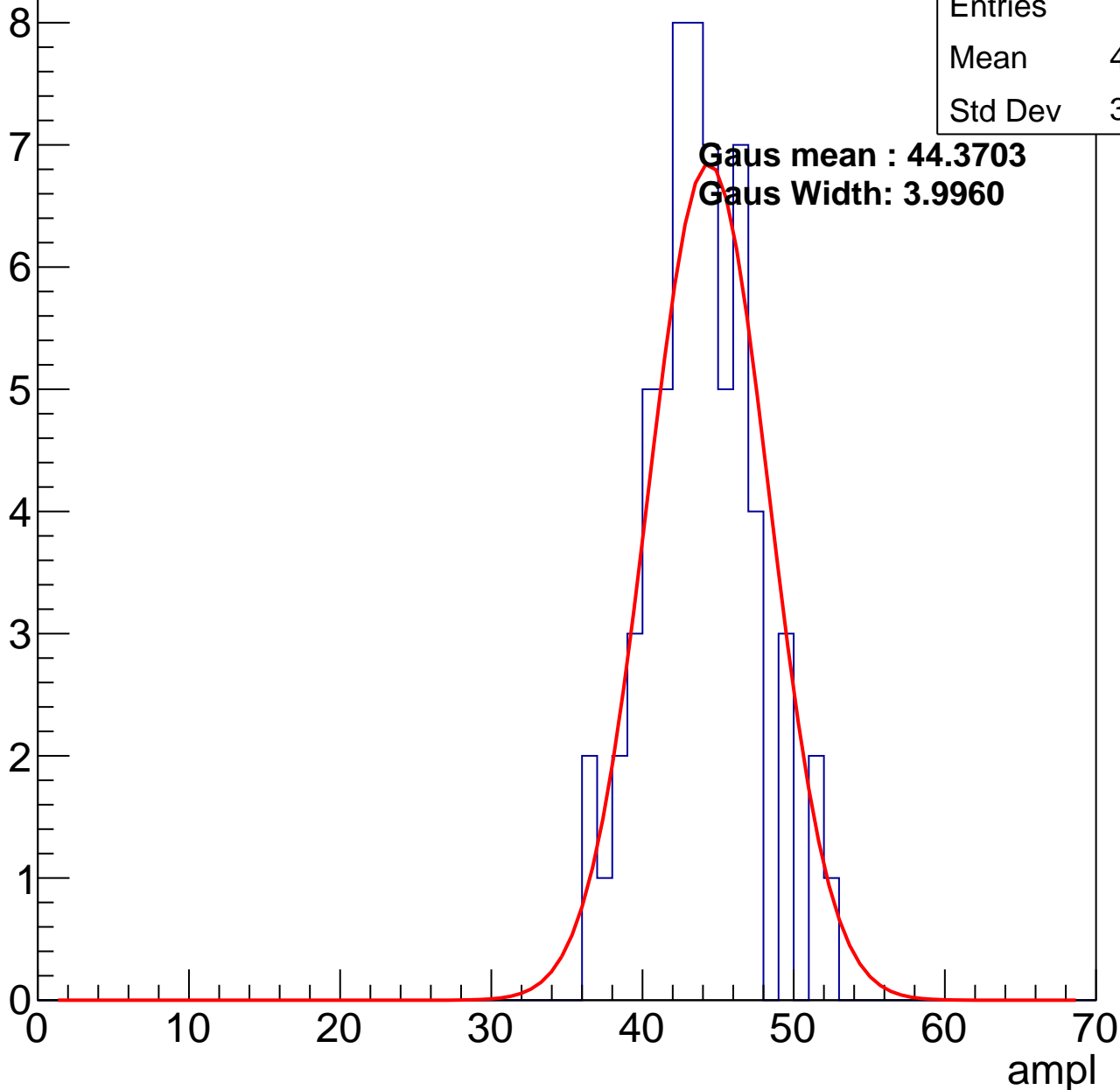
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	63
Mean	43.35
Std Dev	3.492

**Gaus mean : 44.3703**

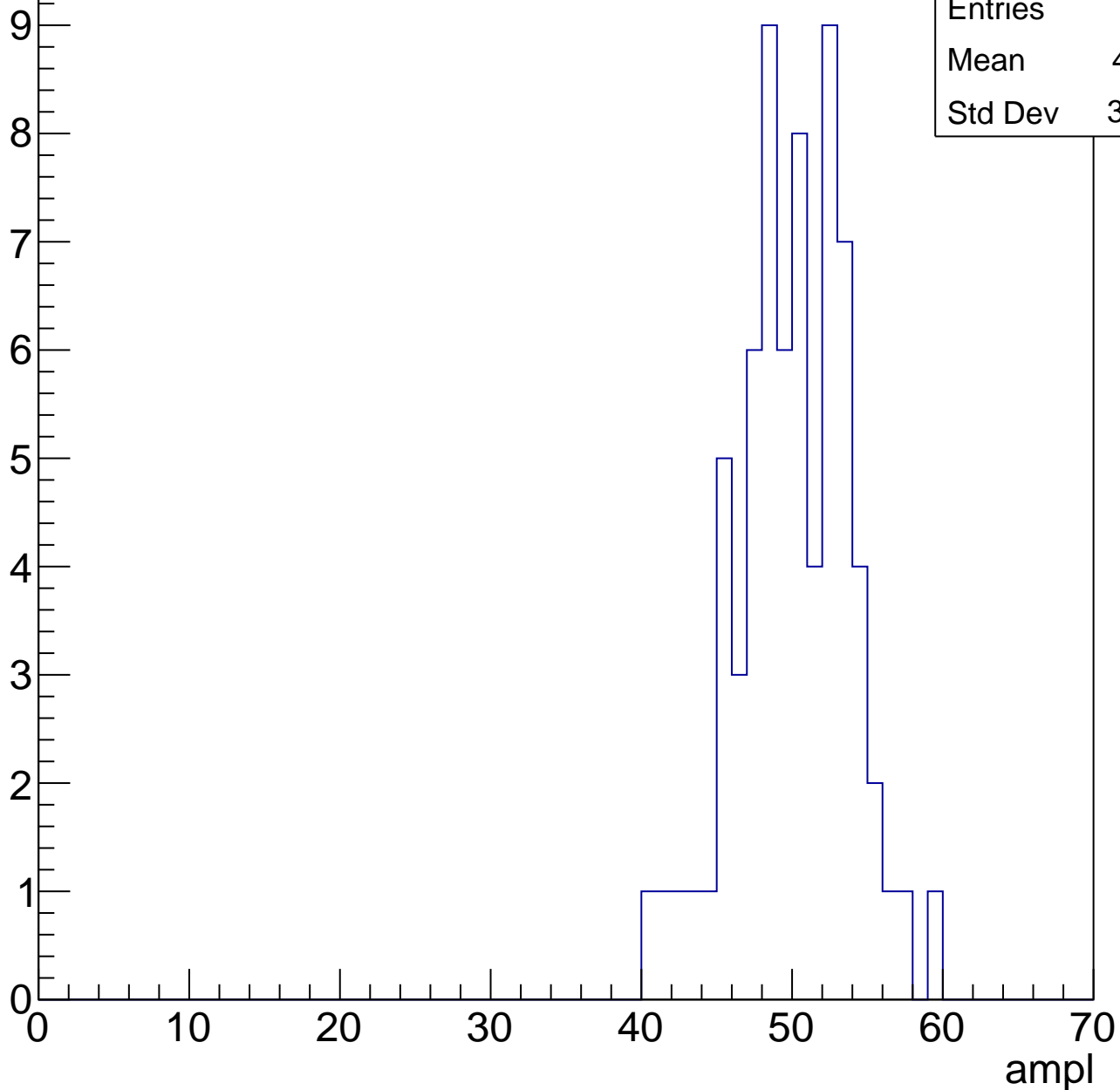
**Gaus Width: 3.9960**



# B1L102S, U12-ch75, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



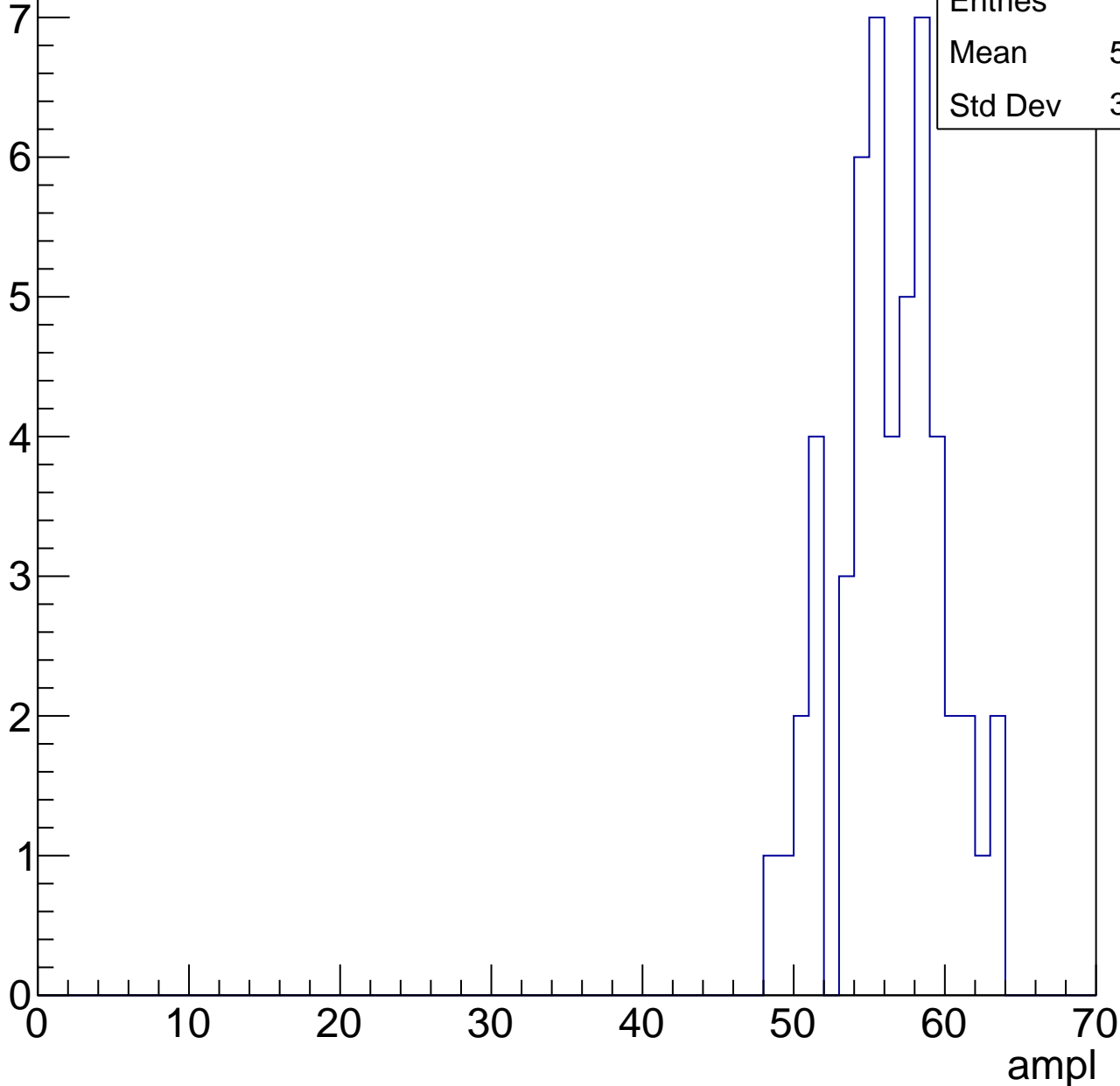
Entries	71
Mean	49.61
Std Dev	3.698

# B1L102S, U12-ch75, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	51
Mean	55.88
Std Dev	3.507

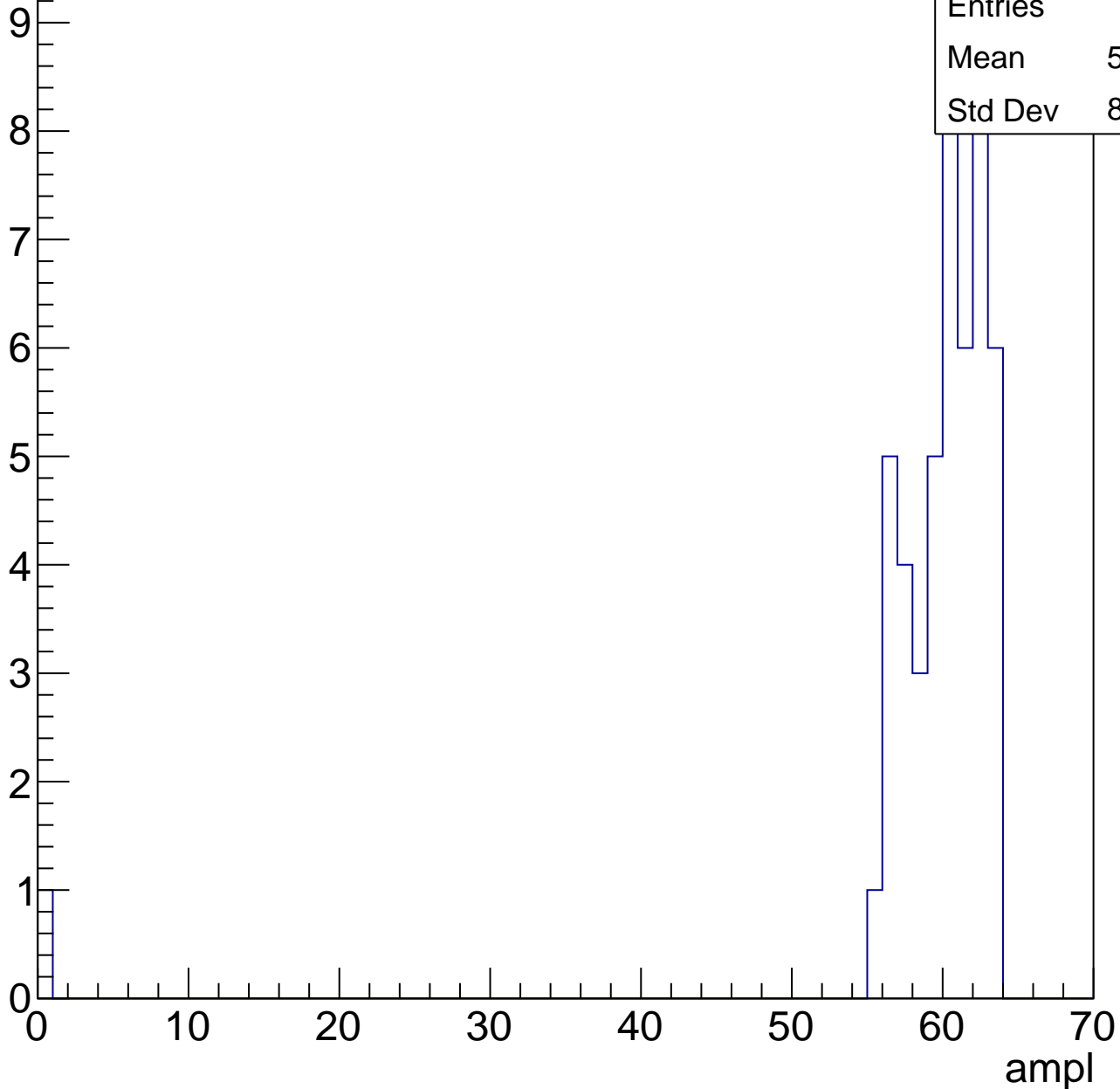


# B1L102S, U12-ch75, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	48
Mean	58.62
Std Dev	8.854



# B1L102S, U12-ch75, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U12-ch75, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U12-ch76, adc0

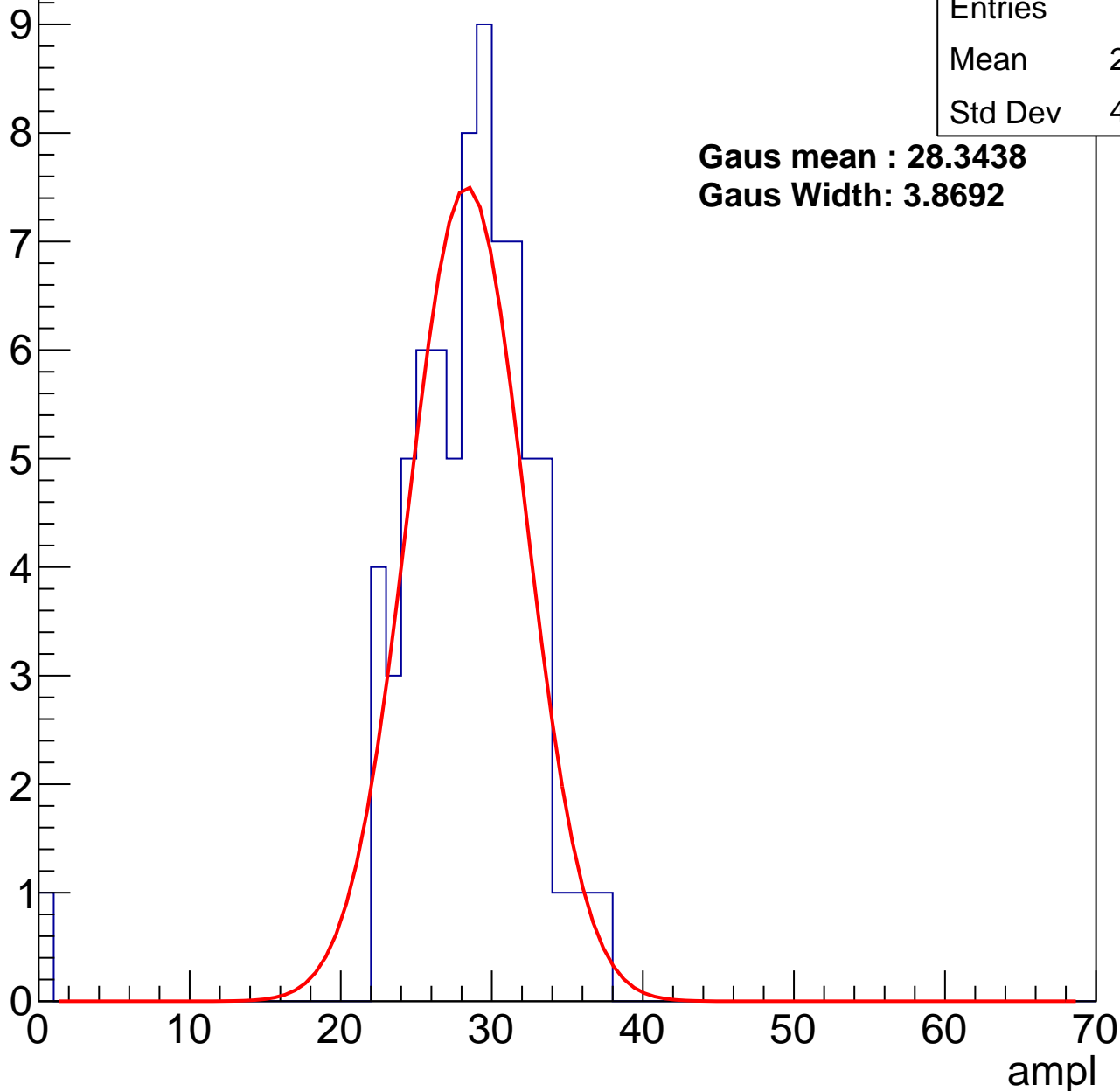
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	75
Mean	27.96
Std Dev	4.762

**Gaus mean : 28.3438**

**Gaus Width: 3.8692**



# B1L102S, U12-ch76, adc1

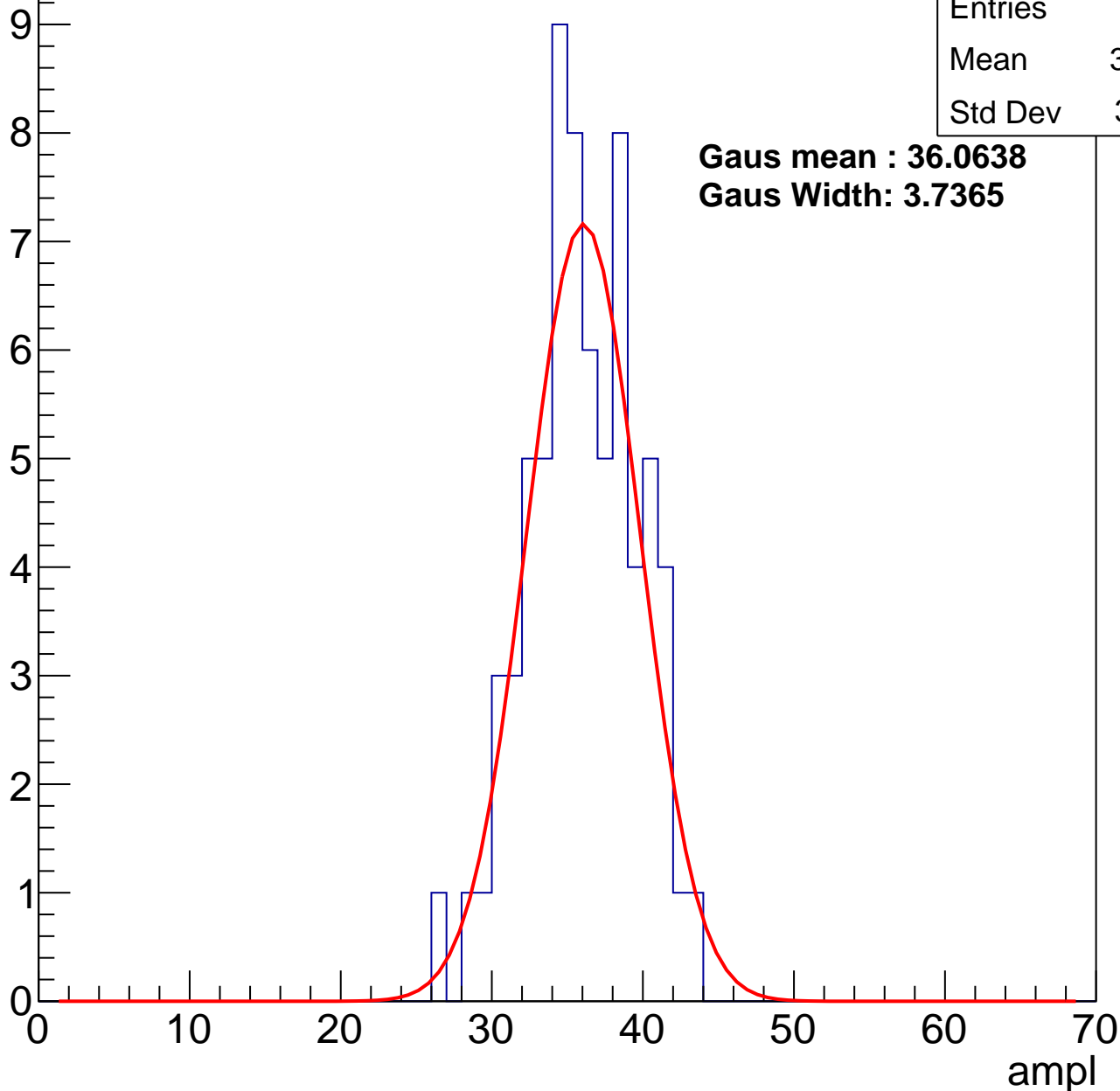
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	70
Mean	35.53
Std Dev	3.561

**Gaus mean : 36.0638**

**Gaus Width: 3.7365**

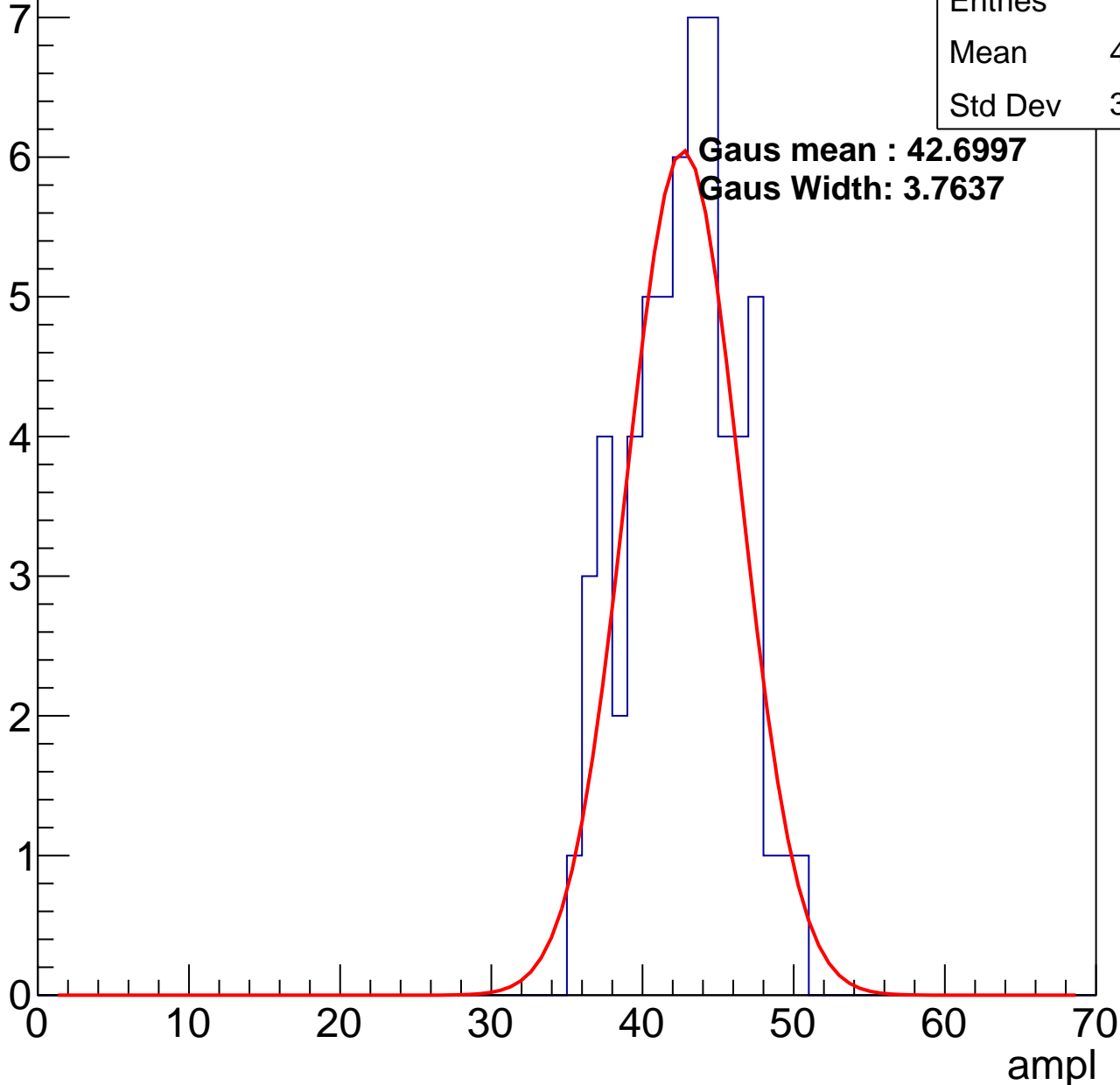


# B1L102S, U12-ch76, adc2

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	60
Mean	42.25
Std Dev	3.548

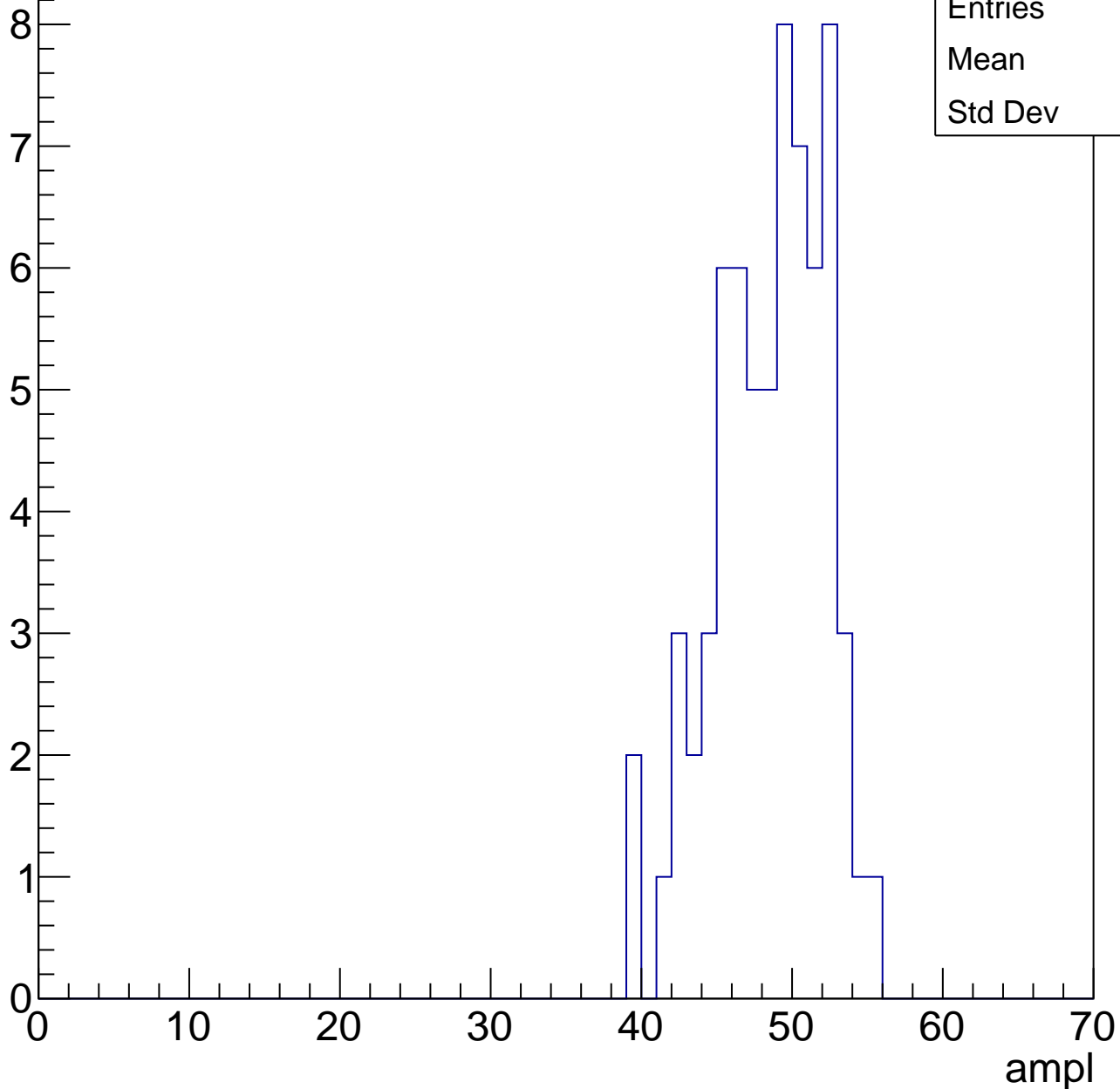


# B1L102S, U12-ch76, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	67
Mean	48
Std Dev	3.62

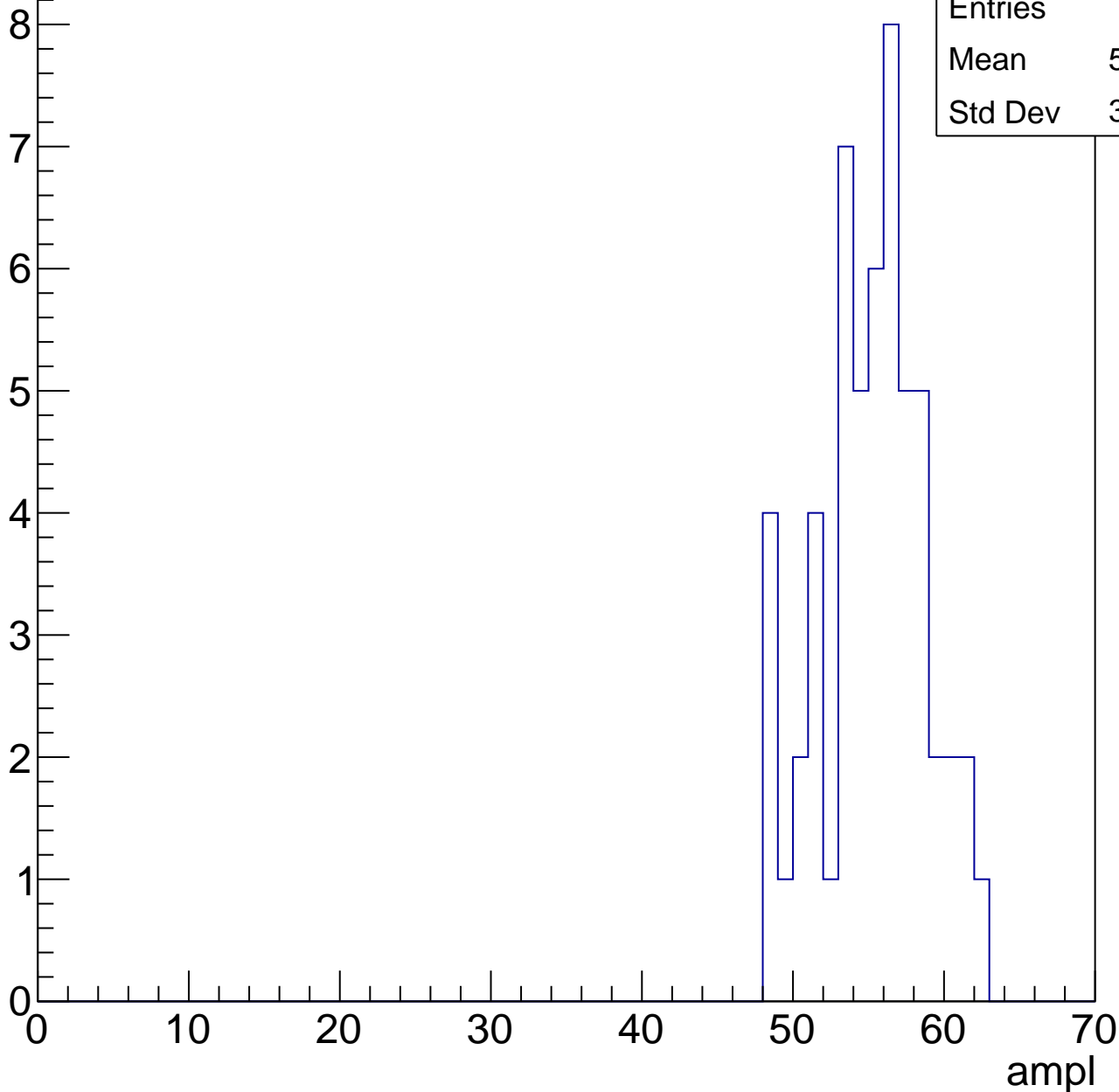


# B1L102S, U12-ch76, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	55
Mean	54.78
Std Dev	3.468

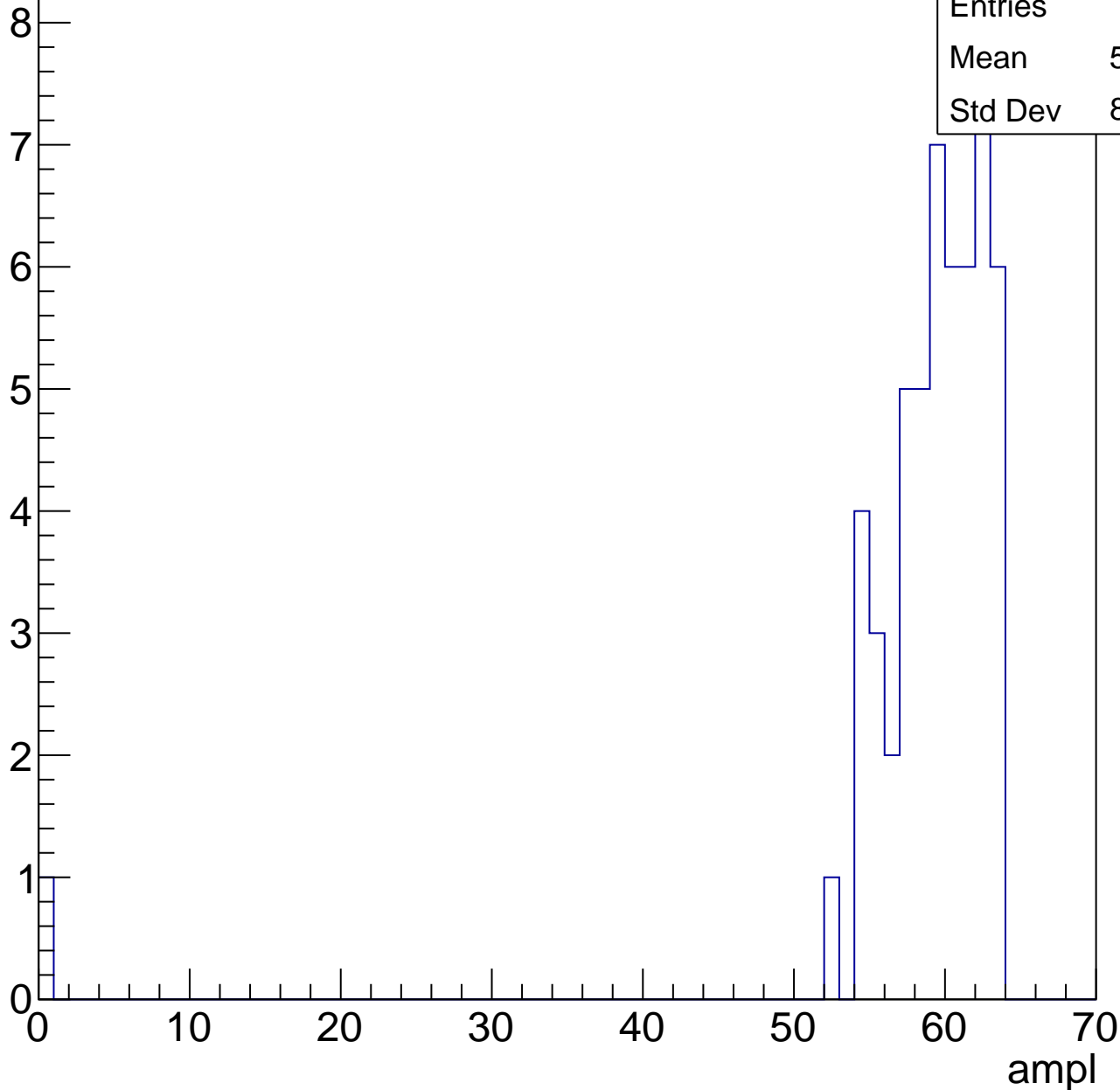


# B1L102S, U12-ch76, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

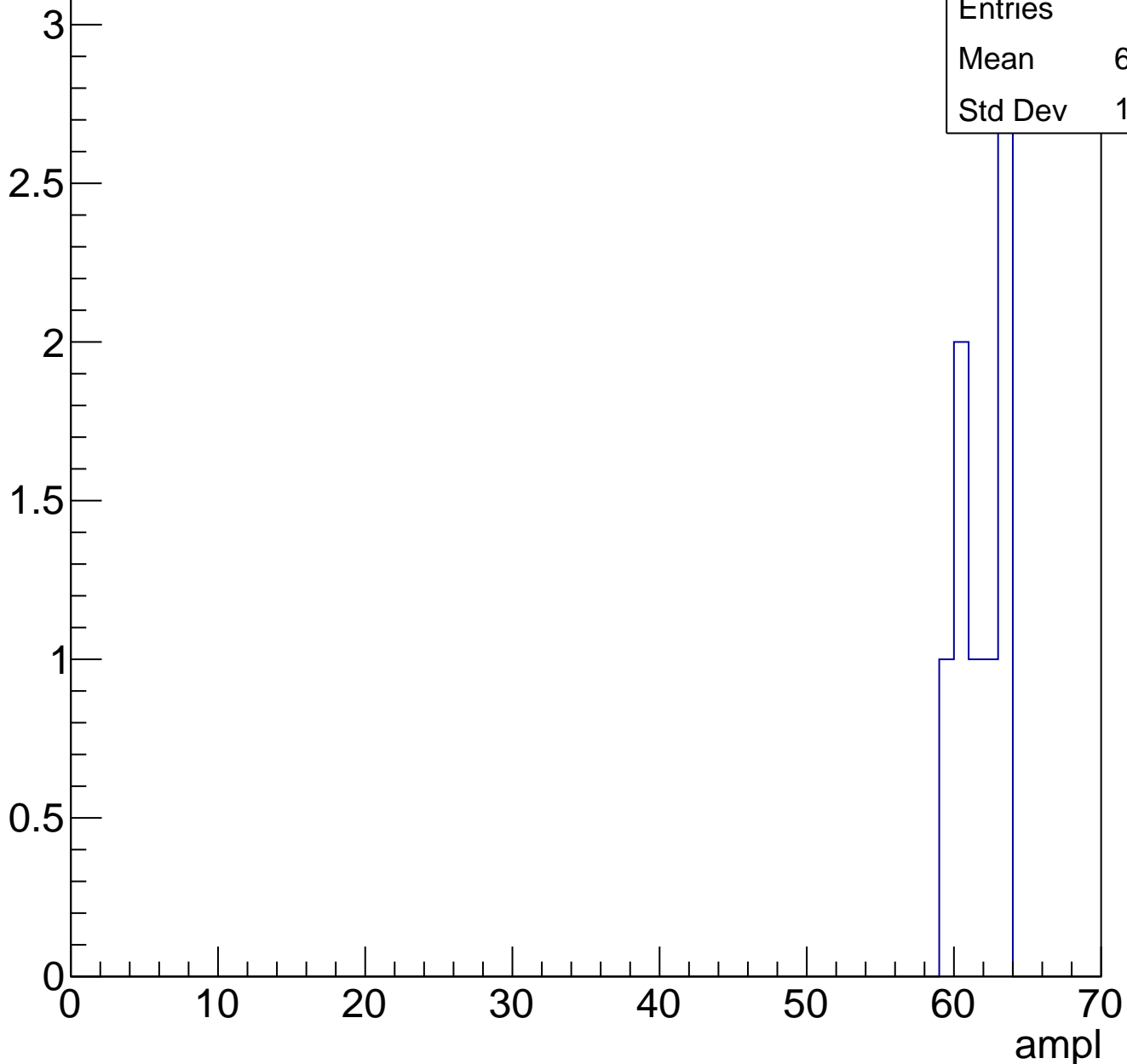
Entries	54
Mean	58.02
Std Dev	8.462



# B1L102S, U12-ch76, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

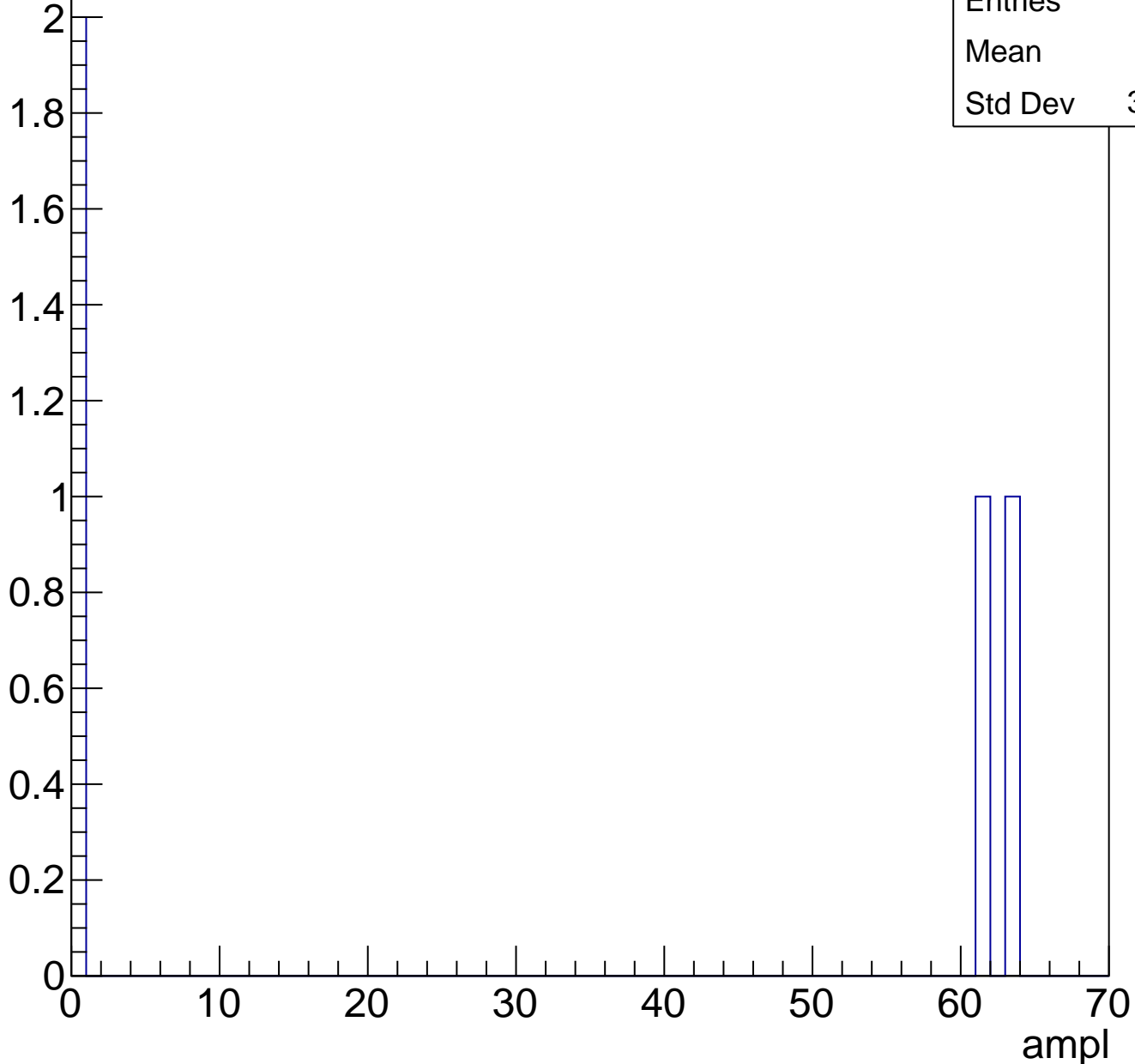




# B1L102S, U12-ch76, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	4
Mean	31
Std Dev	31.01

# B1L102S, U12-ch77, adc0

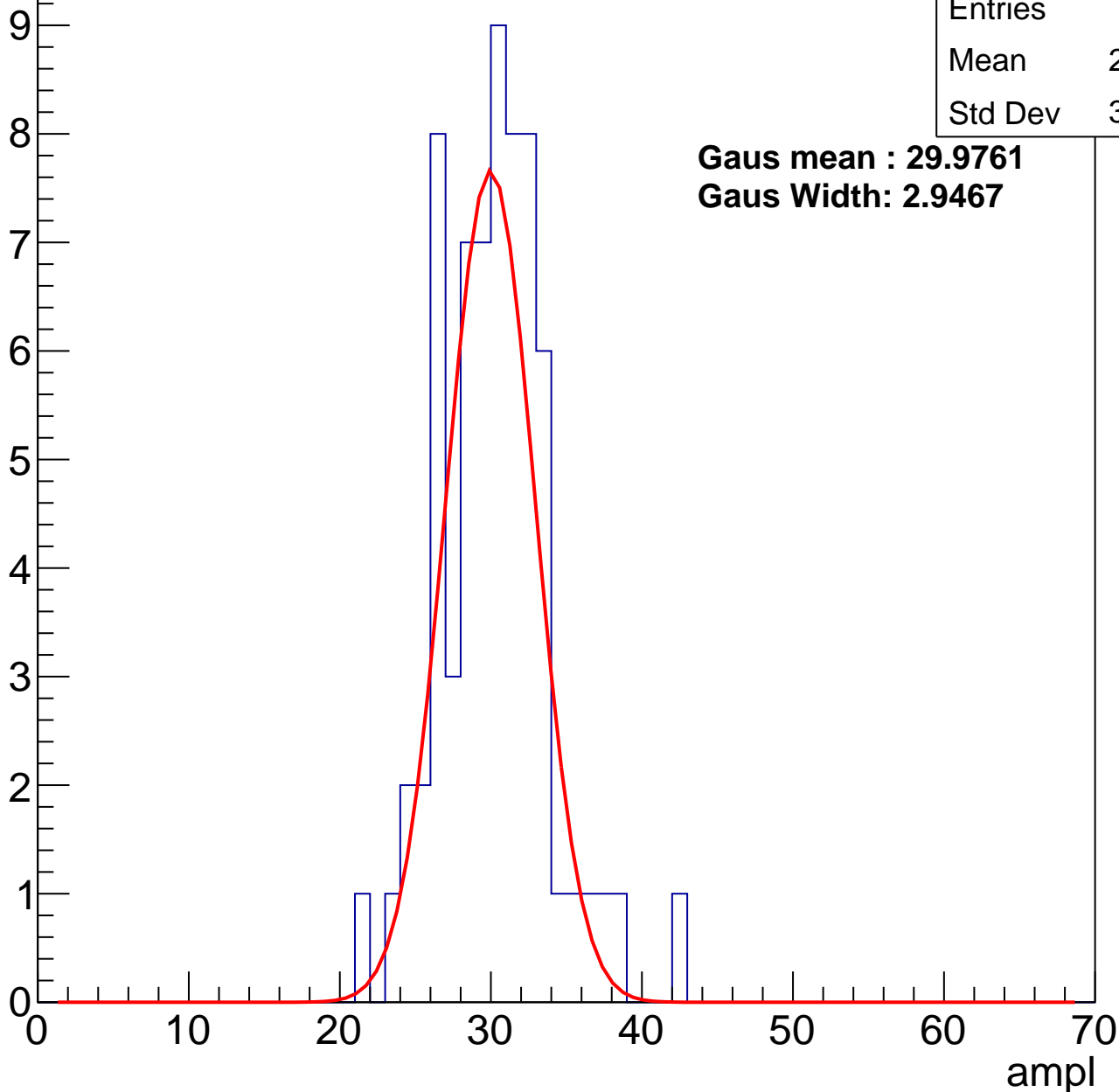
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	29.76
Std Dev	3.569

**Gaus mean : 29.9761**

**Gaus Width: 2.9467**



# B1L102S, U12-ch77, adc1

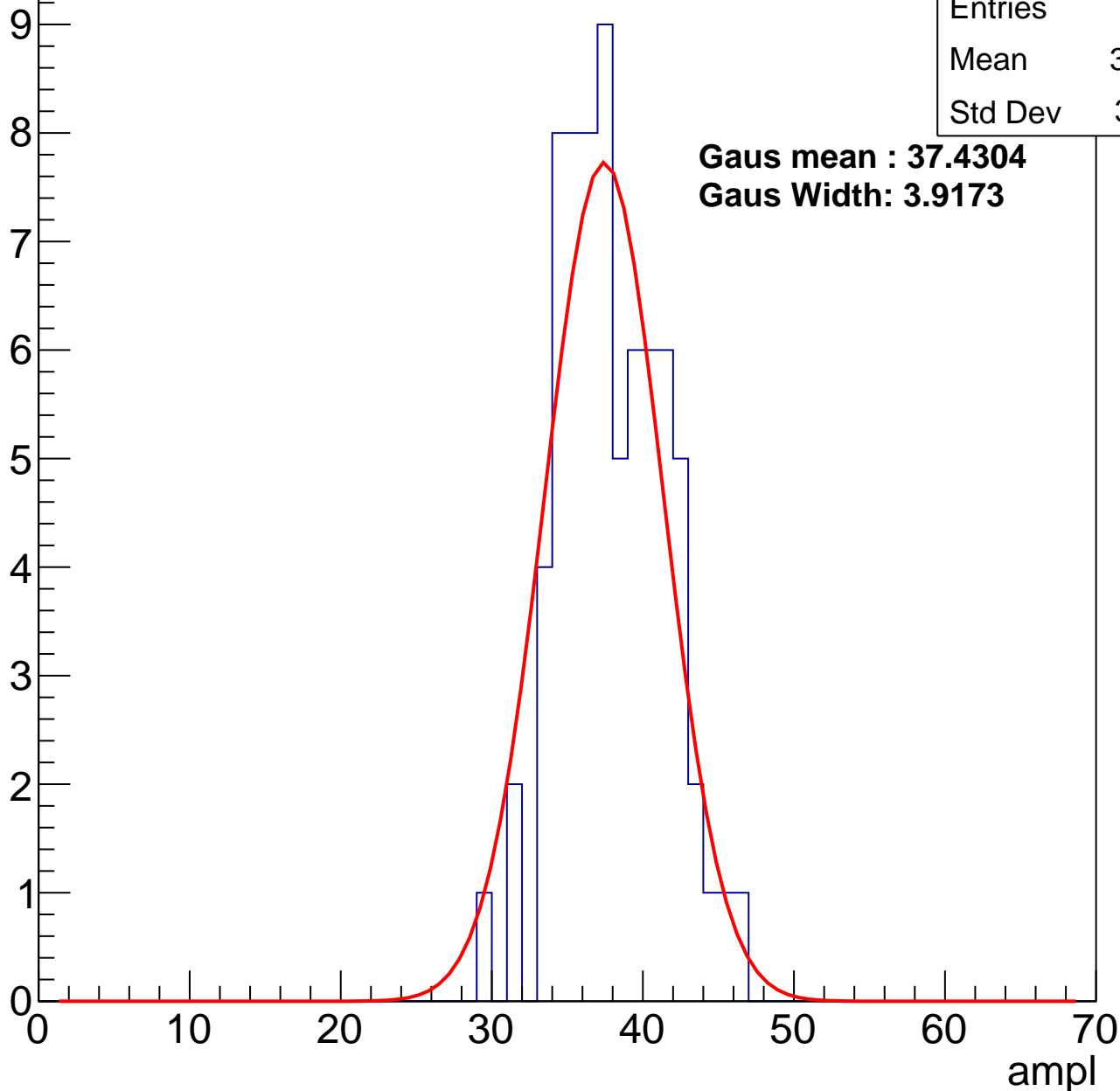
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	73
Mean	37.49
Std Dev	3.441

**Gaus mean : 37.4304**

**Gaus Width: 3.9173**



# B1L102S, U12-ch77, adc2

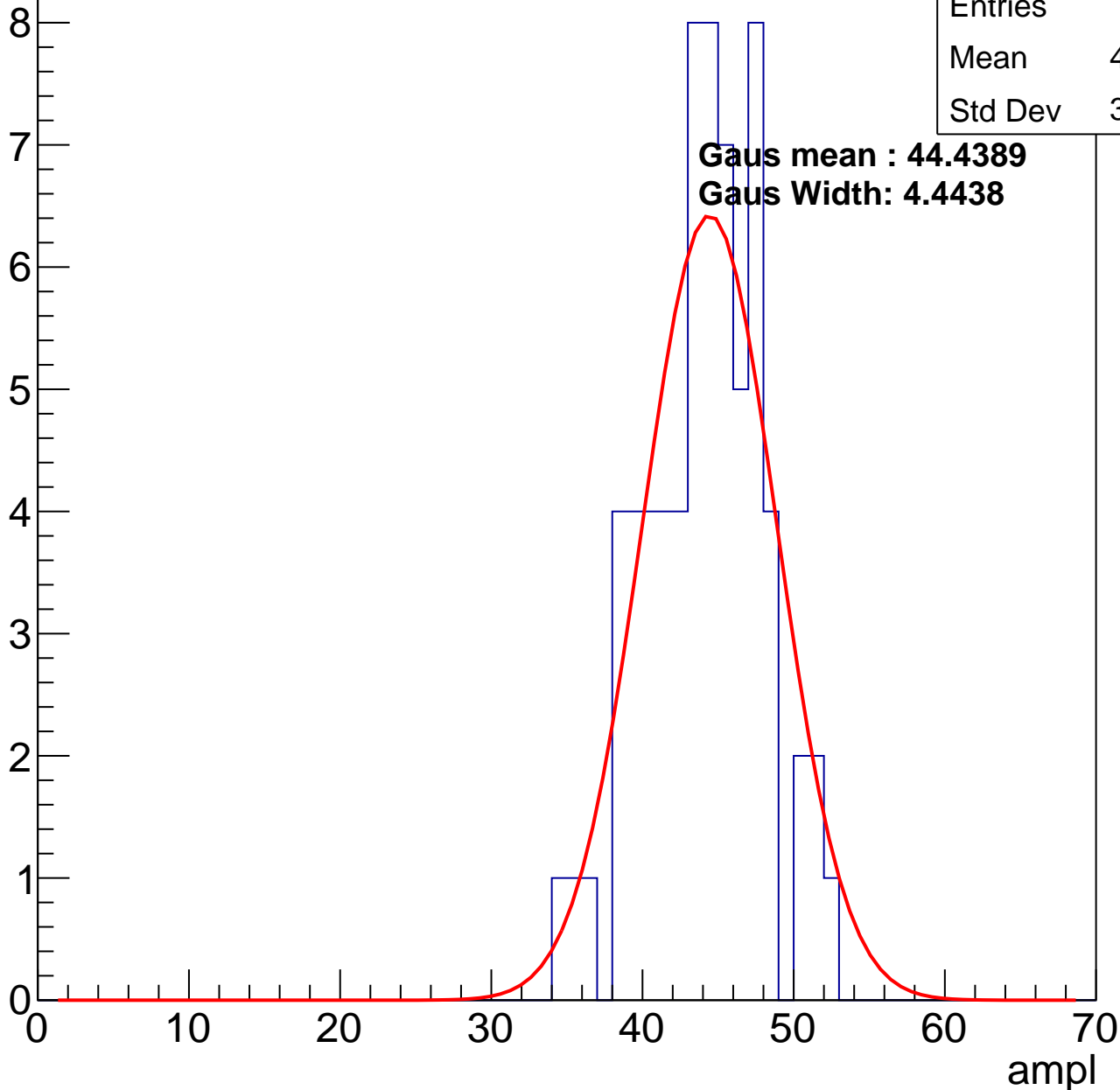
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	43.65
Std Dev	3.838

**Gaus mean : 44.4389**

**Gaus Width: 4.4438**



# B1L102S, U12-ch77, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

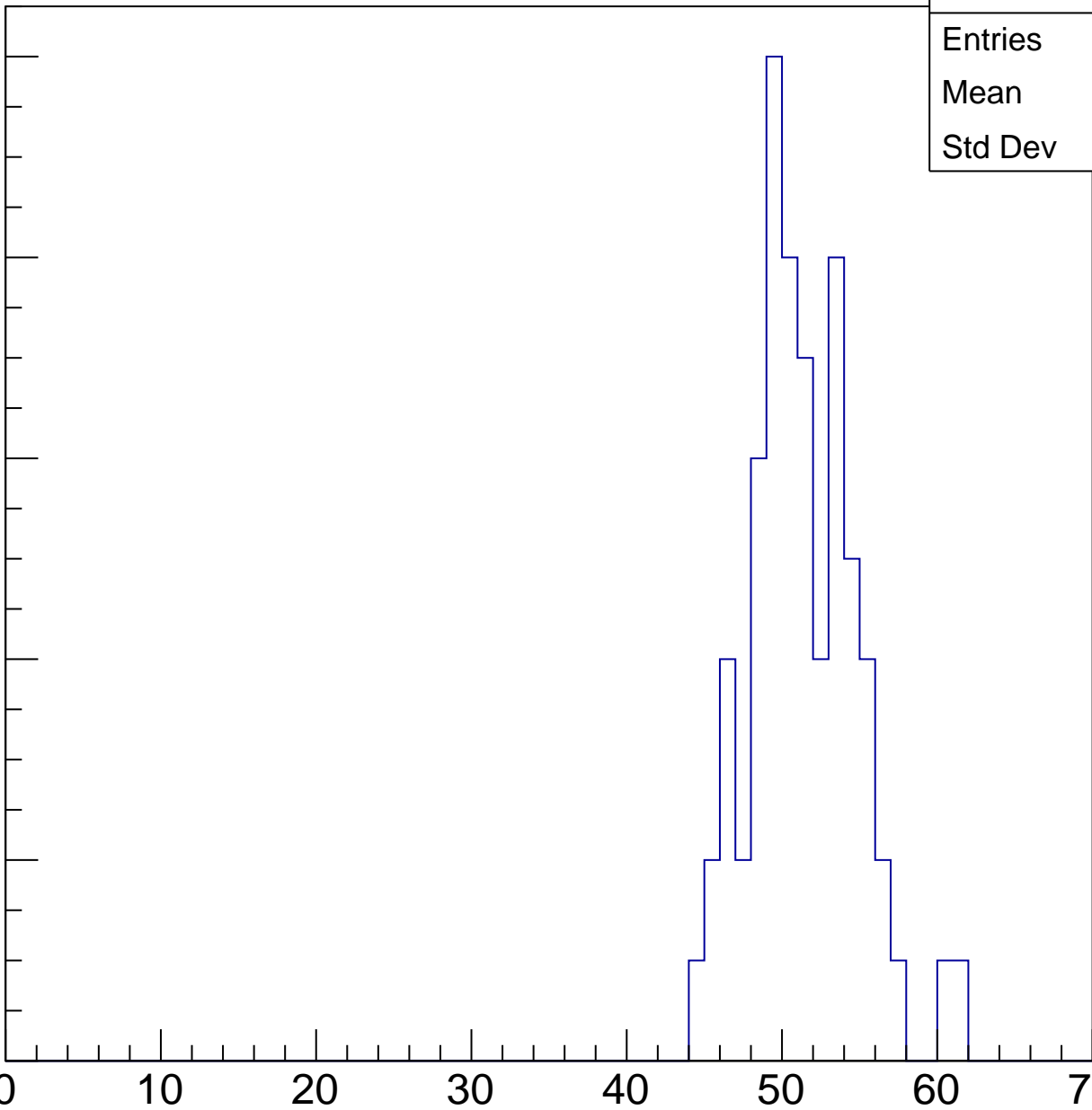
Entries	66
Mean	50.89
Std Dev	3.407

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

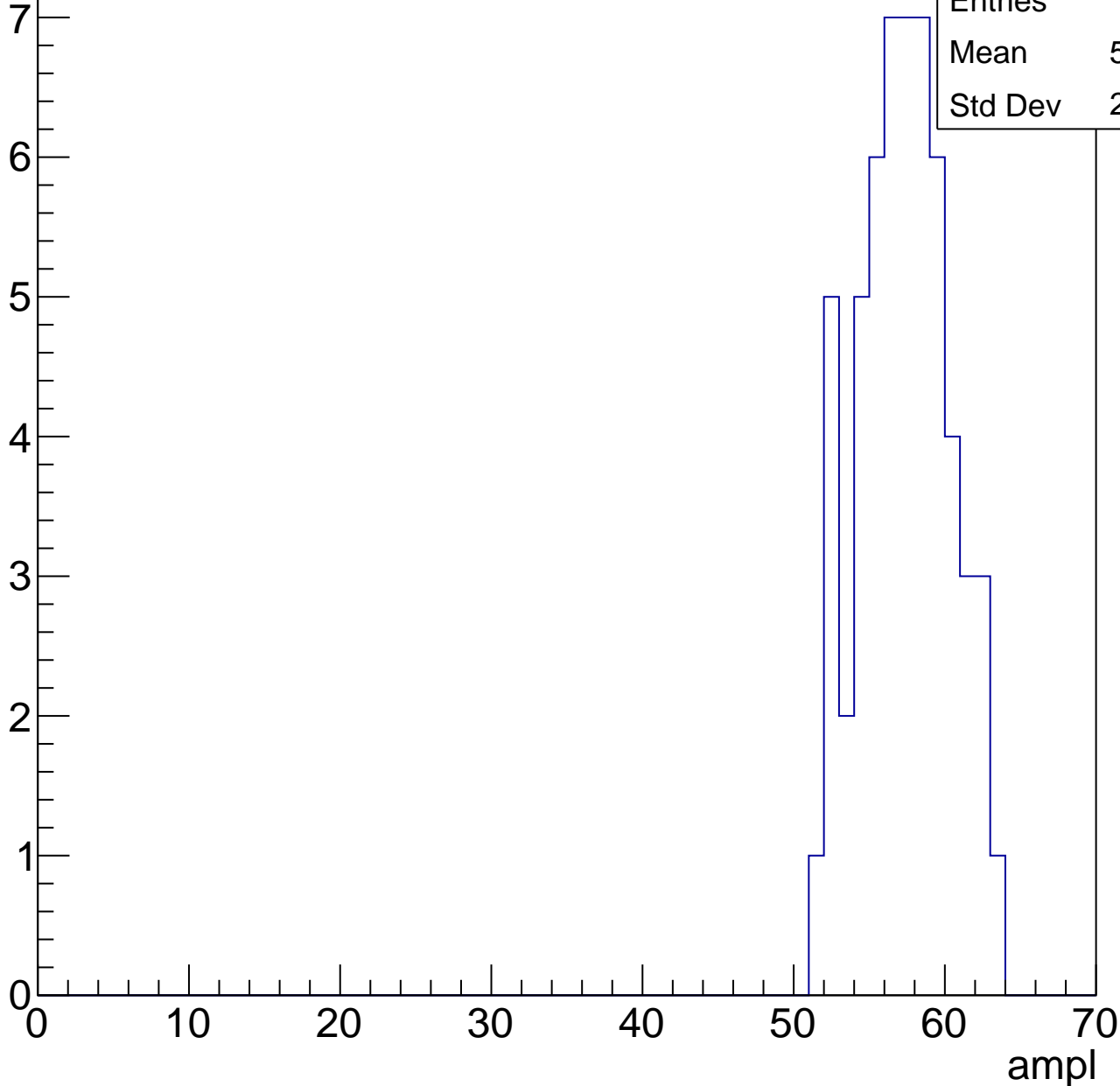


# B1L102S, U12-ch77, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	57
Mean	56.84
Std Dev	2.943

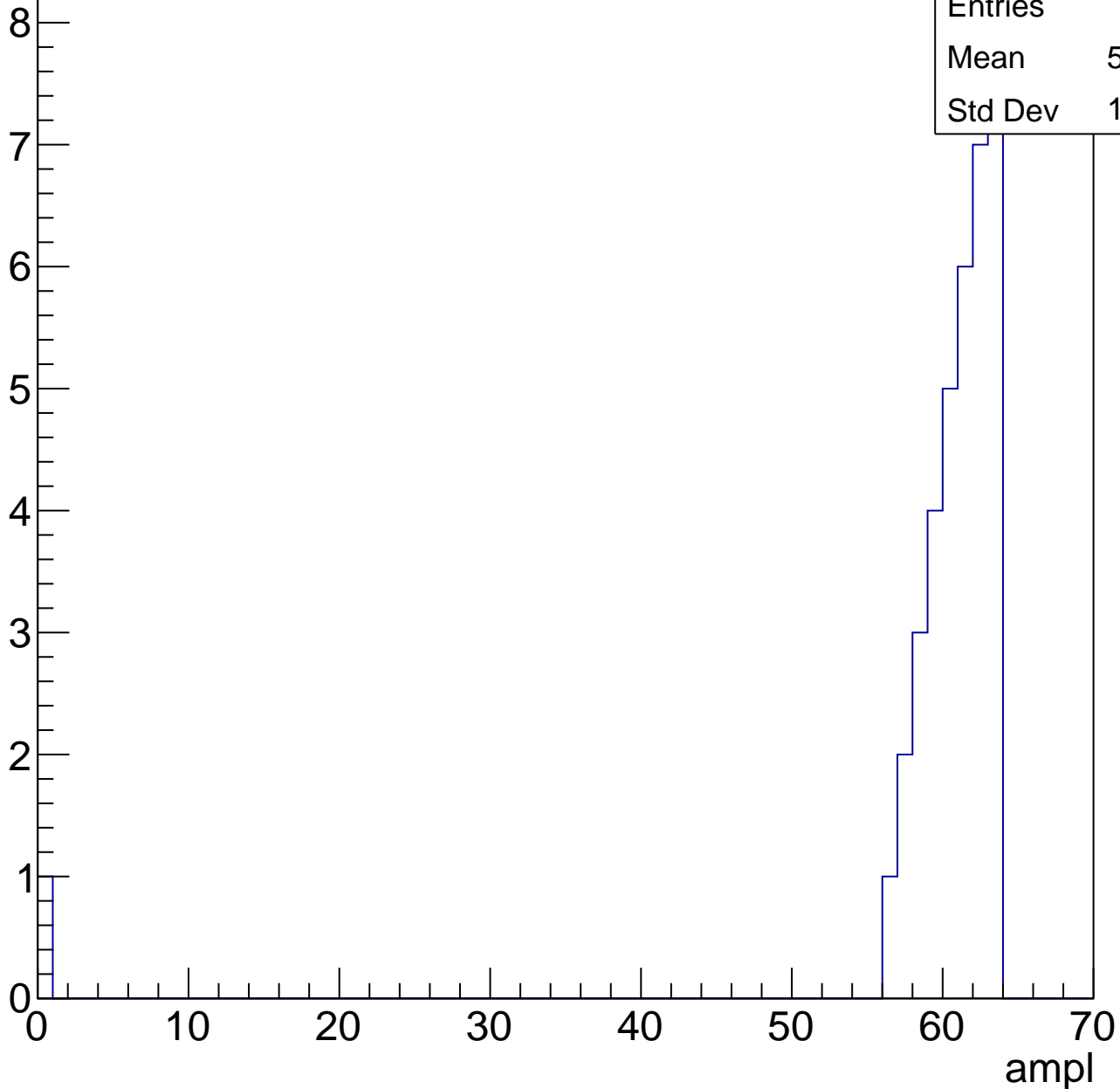


# B1L102S, U12-ch77, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	37
Mean	59.03
Std Dev	10.03



# B1L102S, U12-ch77, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U12-ch77, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L102S, U12-ch78, adc0

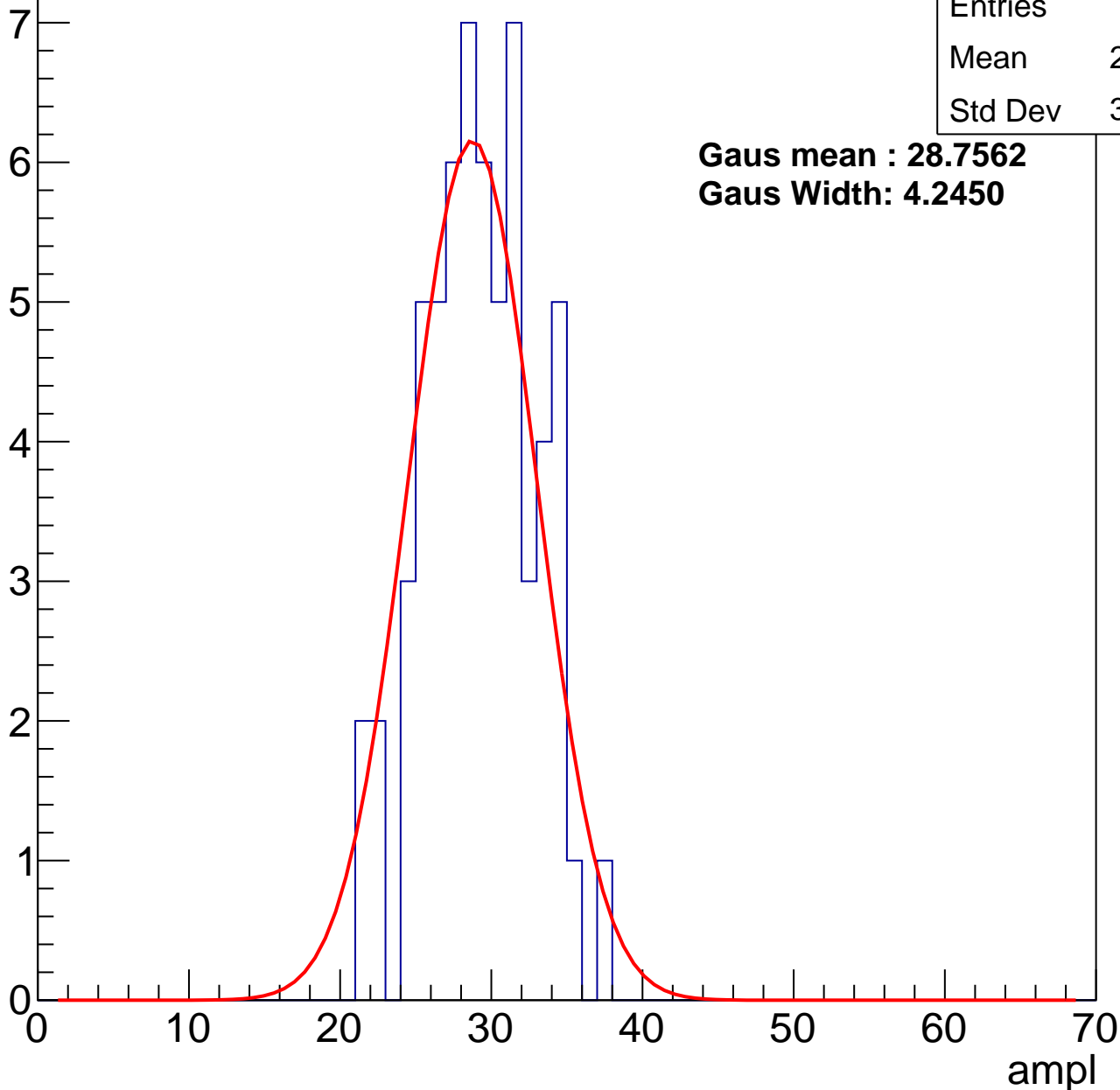
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	62
Mean	28.74
Std Dev	3.596

**Gaus mean : 28.7562**

**Gaus Width: 4.2450**



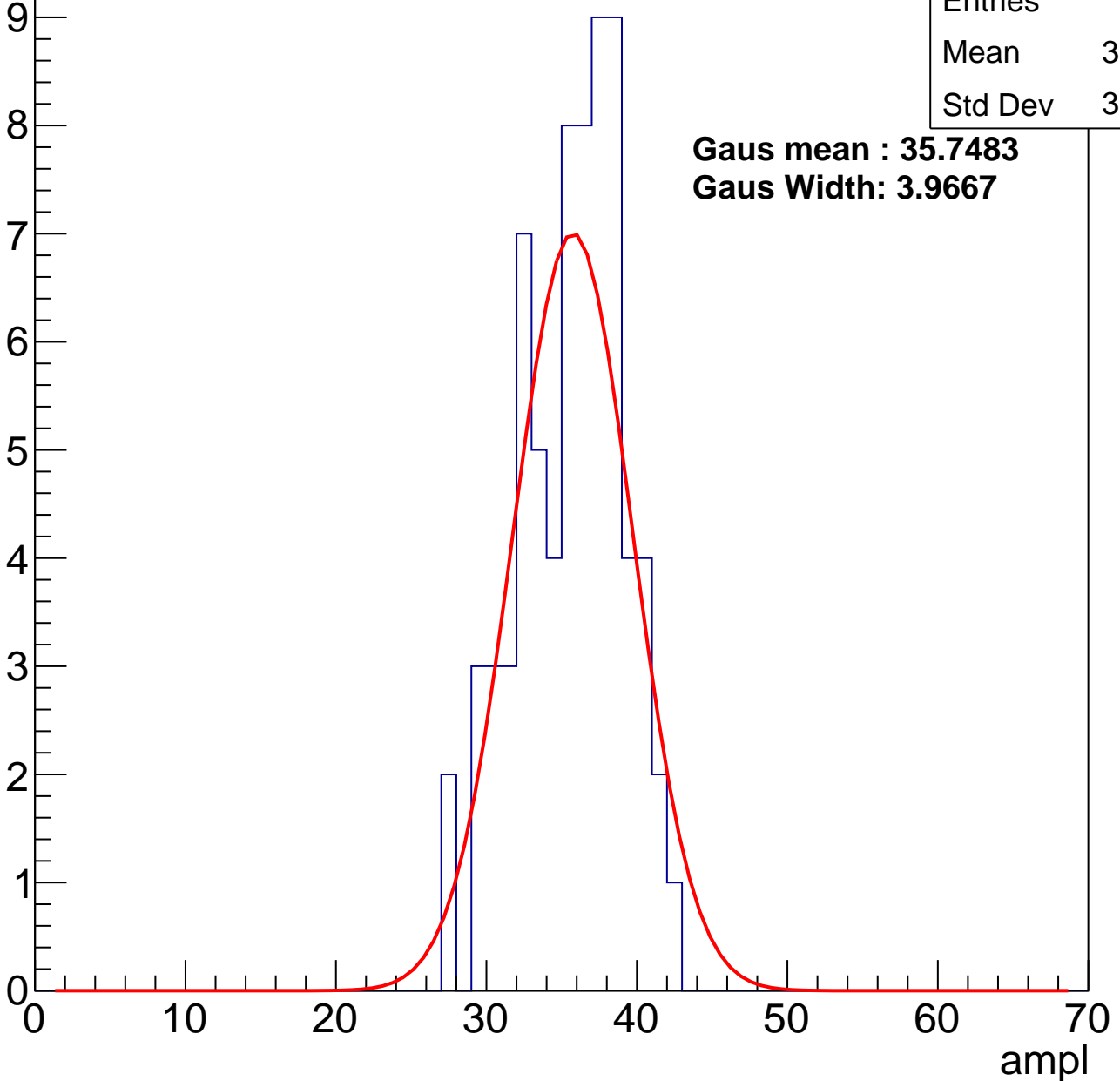
# B1L102S, U12-ch78, adc1

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	72
Mean	35.17
Std Dev	3.444

**Gaus mean : 35.7483**  
**Gaus Width: 3.9667**



# B1L102S, U12-ch78, adc2

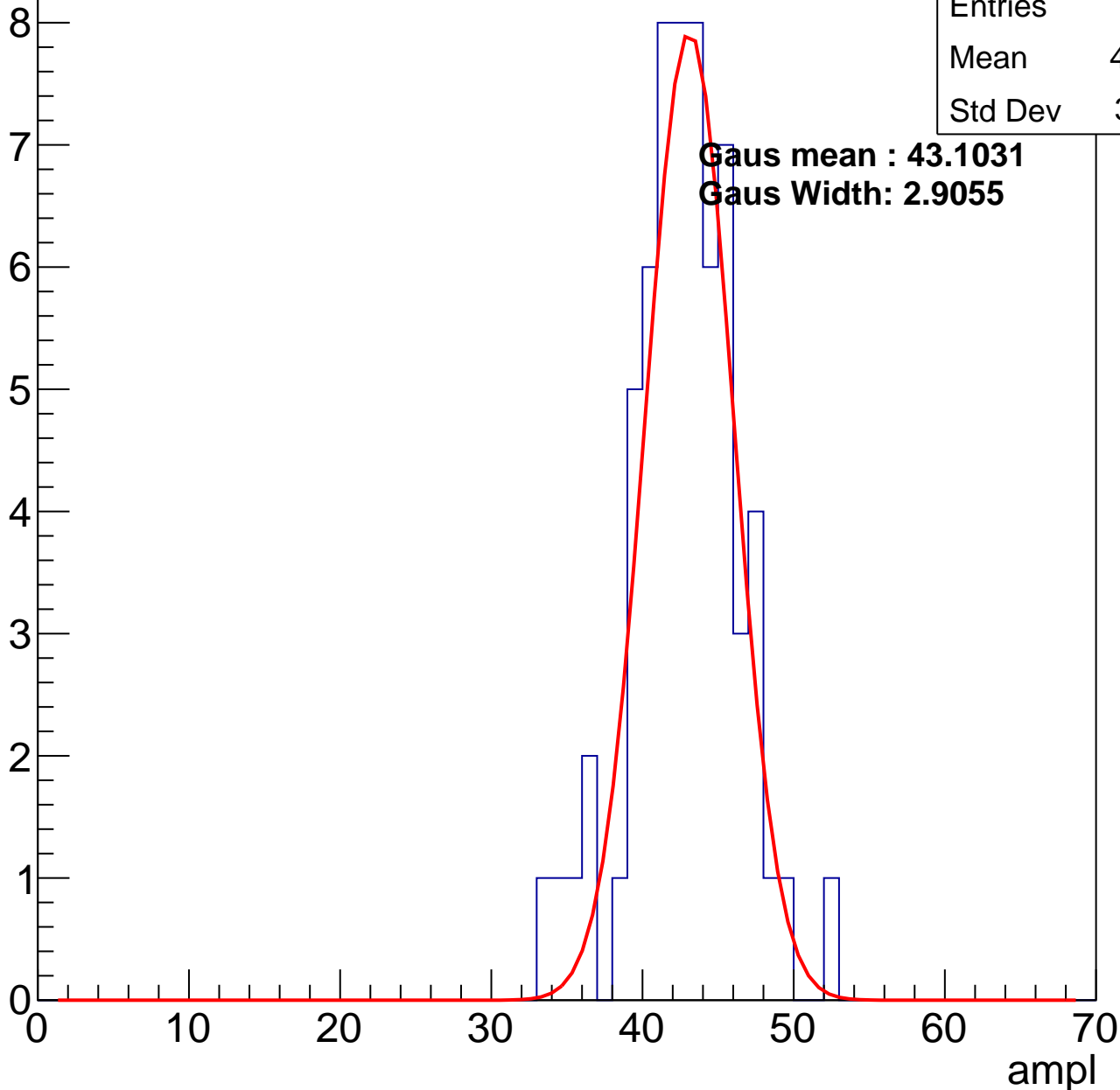
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	42.33
Std Dev	3.491

**Gaus mean : 43.1031**

**Gaus Width: 2.9055**

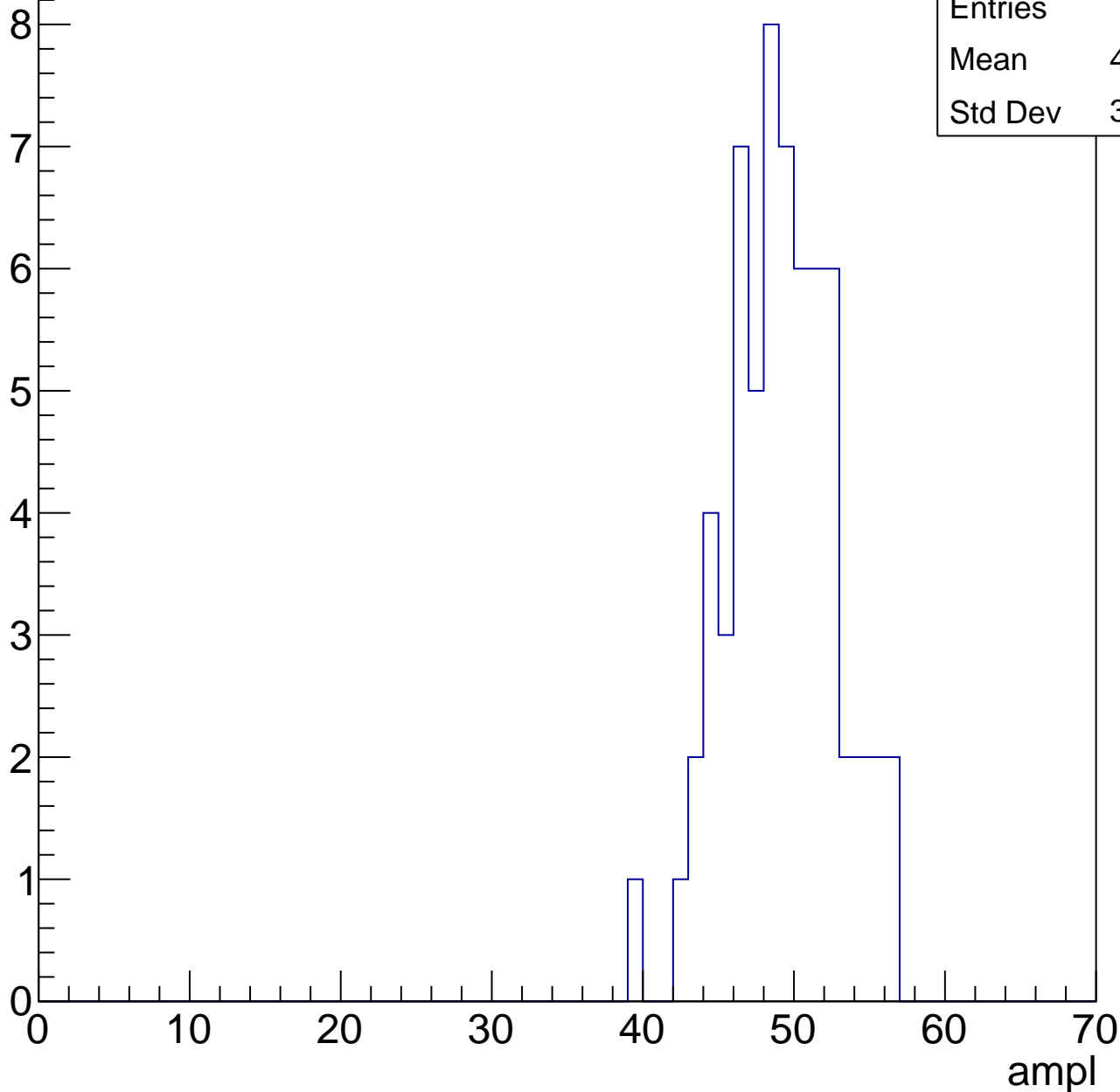


# B1L102S, U12-ch78, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	48.69
Std Dev	3.513

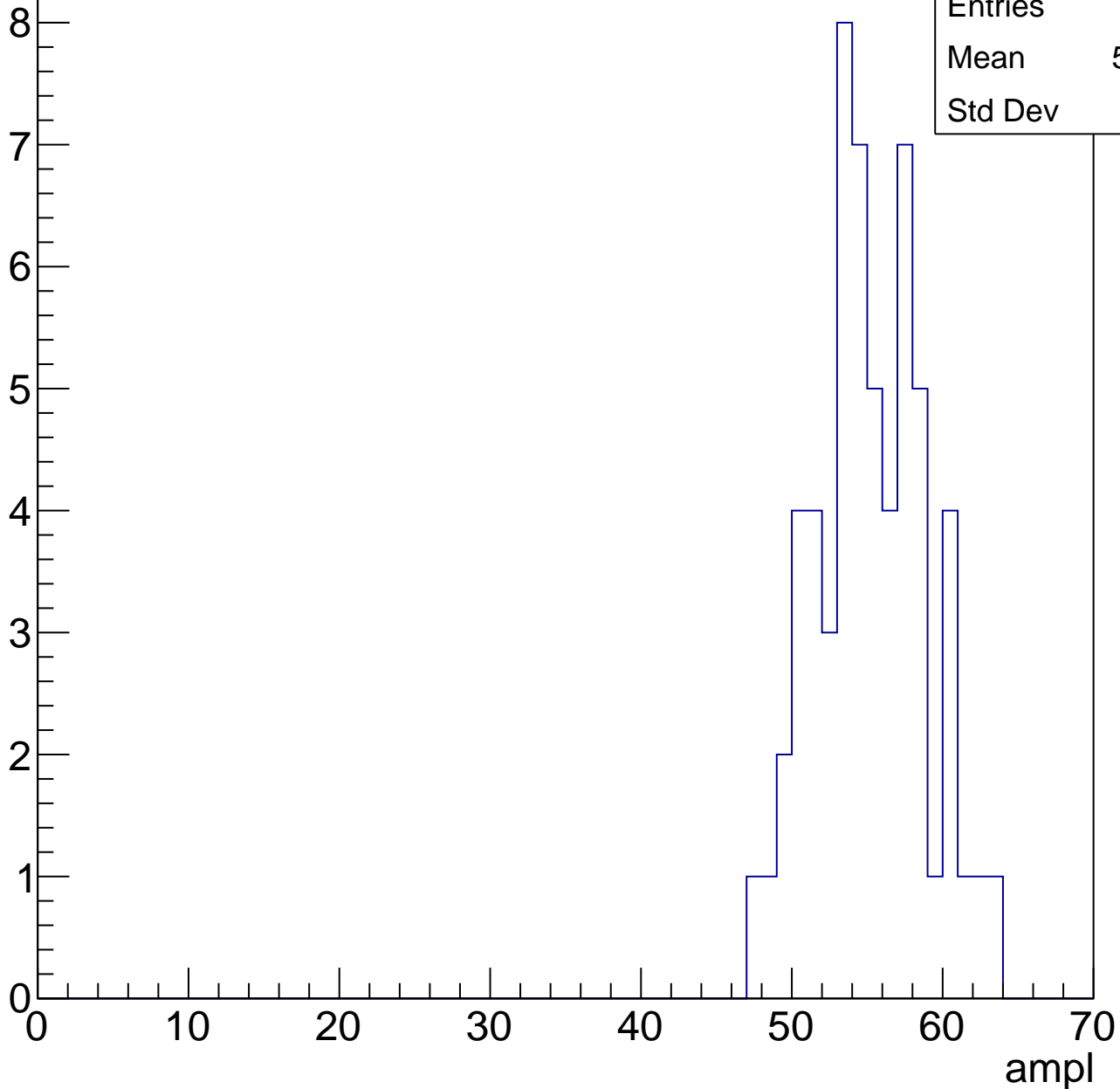


# B1L102S, U12-ch78, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	59
Mean	54.71
Std Dev	3.57

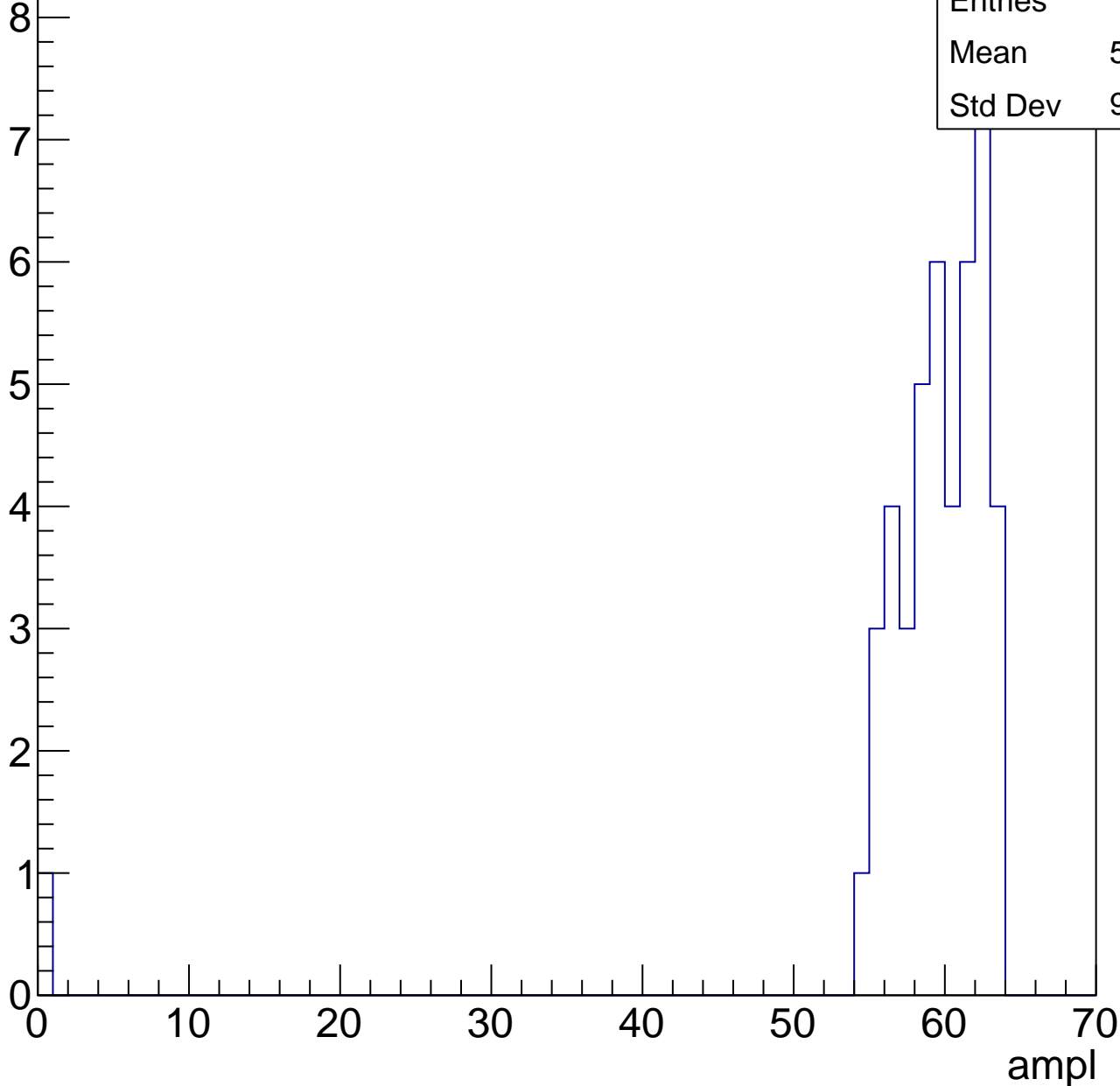


# B1L102S, U12-ch78, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	45
Mean	58.04
Std Dev	9.104

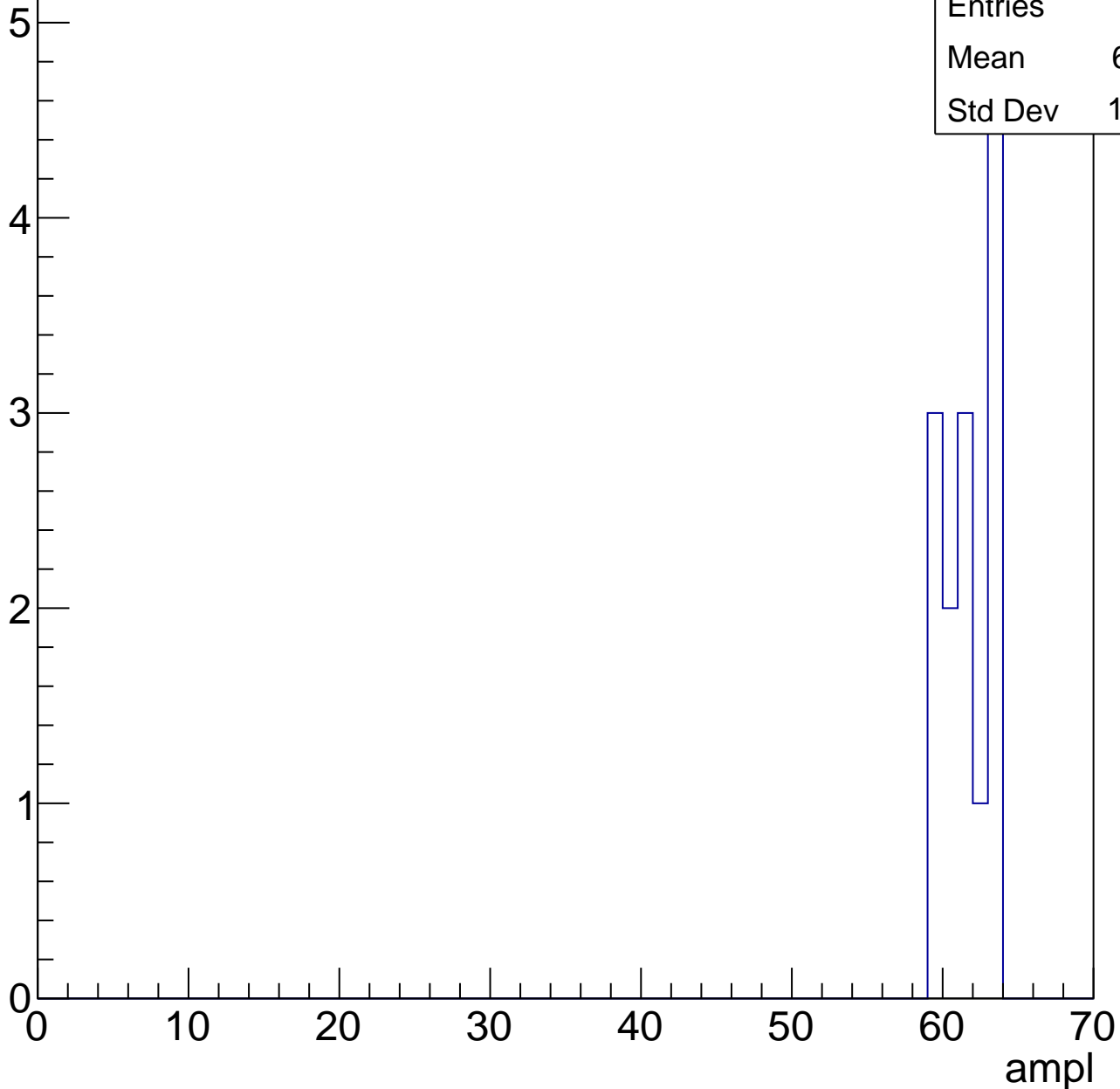


# B1L102S, U12-ch78, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	14
Mean	61.21
Std Dev	1.567





# B1L102S, U12-ch78, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L102S, U12-ch79, adc0

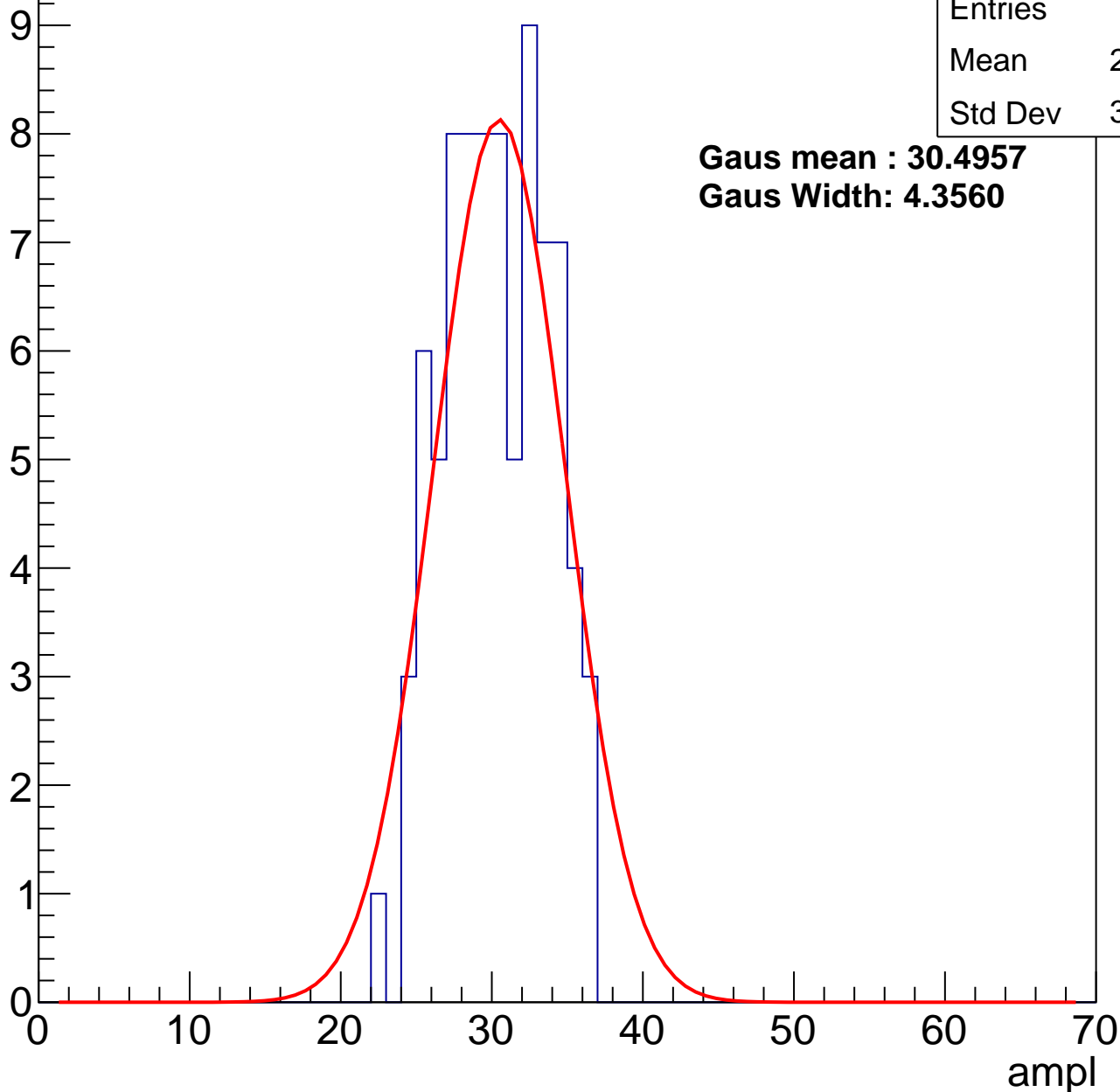
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	82
Mean	29.83
Std Dev	3.378

**Gaus mean : 30.4957**

**Gaus Width: 4.3560**



# B1L102S, U12-ch79, adc1

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	69
Mean	37.12
Std Dev	3.458

**Gaus mean : 38.4530**

**Gaus Width: 3.7637**

Entry

10  
8  
6  
4  
2  
0

ampl

0

10

20

30

40

50

60

70

# B1L102S, U12-ch79, adc2

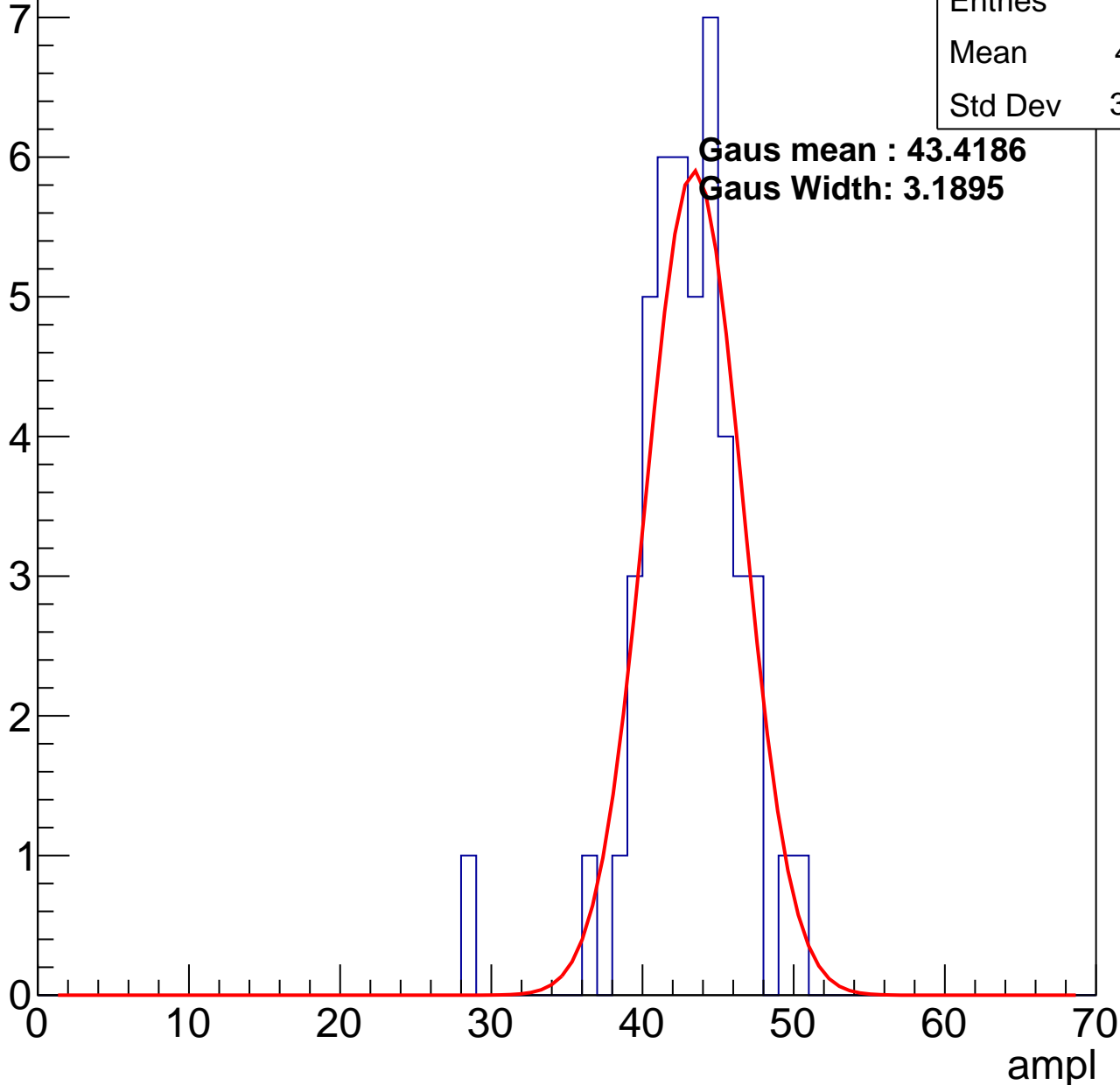
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	47
Mean	42.51
Std Dev	3.554

**Gaus mean : 43.4186**

**Gaus Width: 3.1895**



# B1L102S, U12-ch79, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

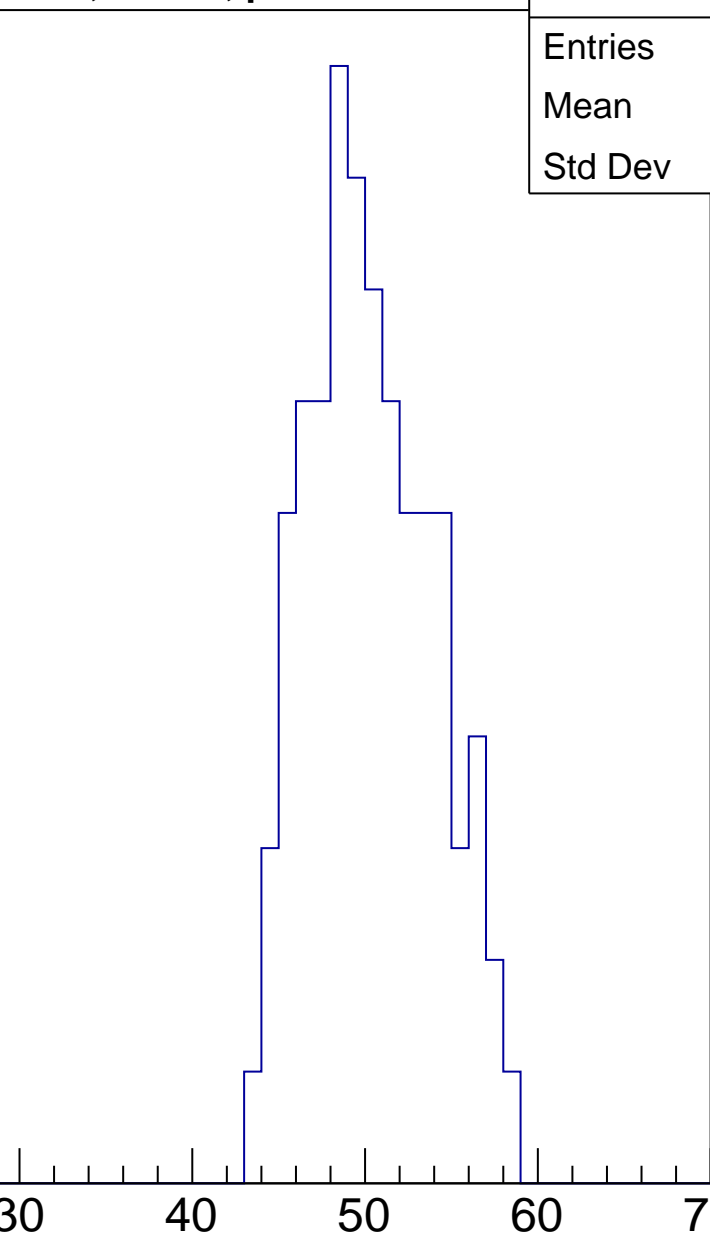
Entries	86
Mean	49.87
Std Dev	3.563

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

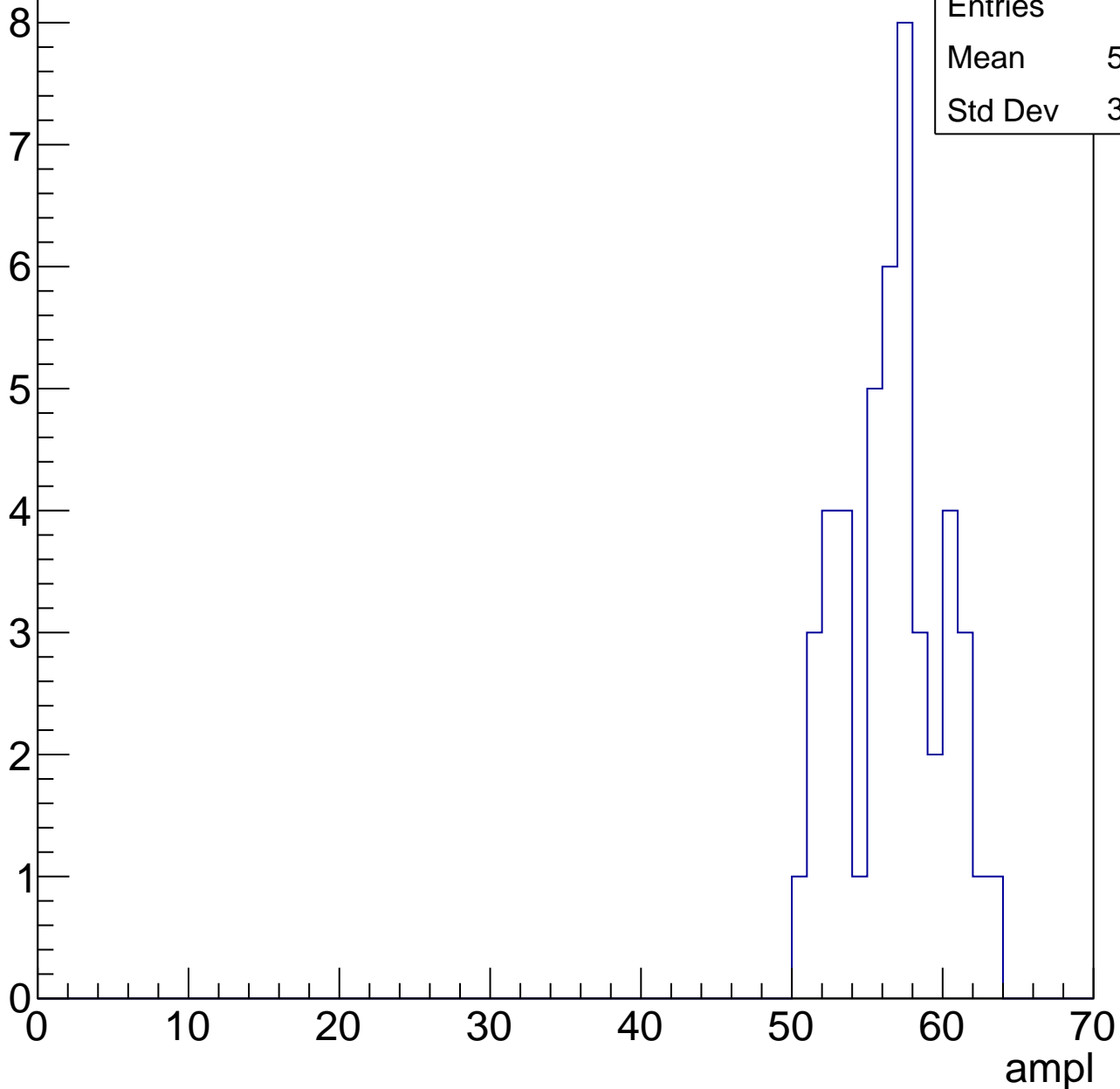


# B1L102S, U12-ch79, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	46
Mean	56.17
Std Dev	3.232

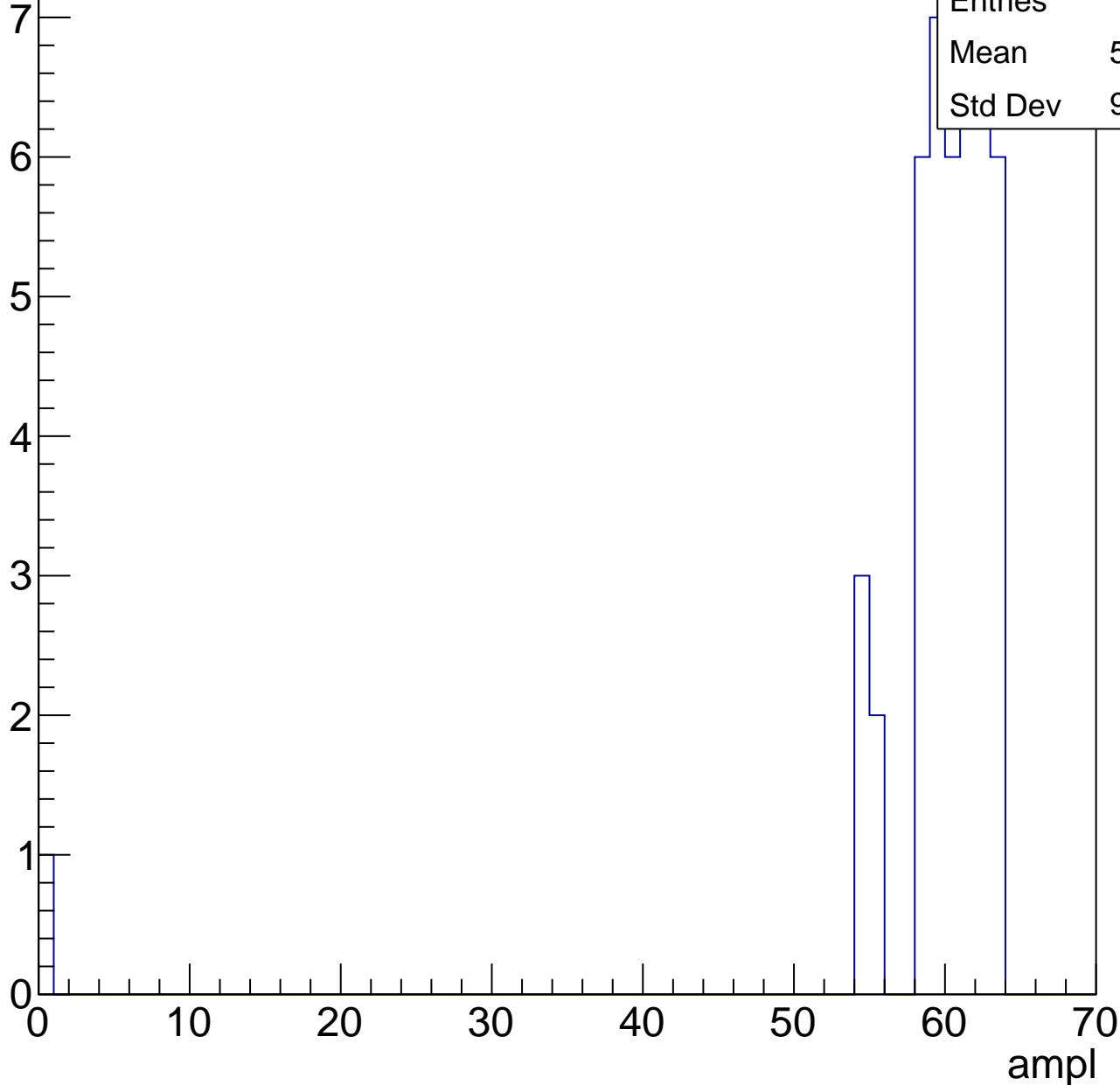


# B1L102S, U12-ch79, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	45
Mean	58.49
Std Dev	9.159



# B1L102S, U12-ch79, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U12-ch79, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U12-ch80, adc0

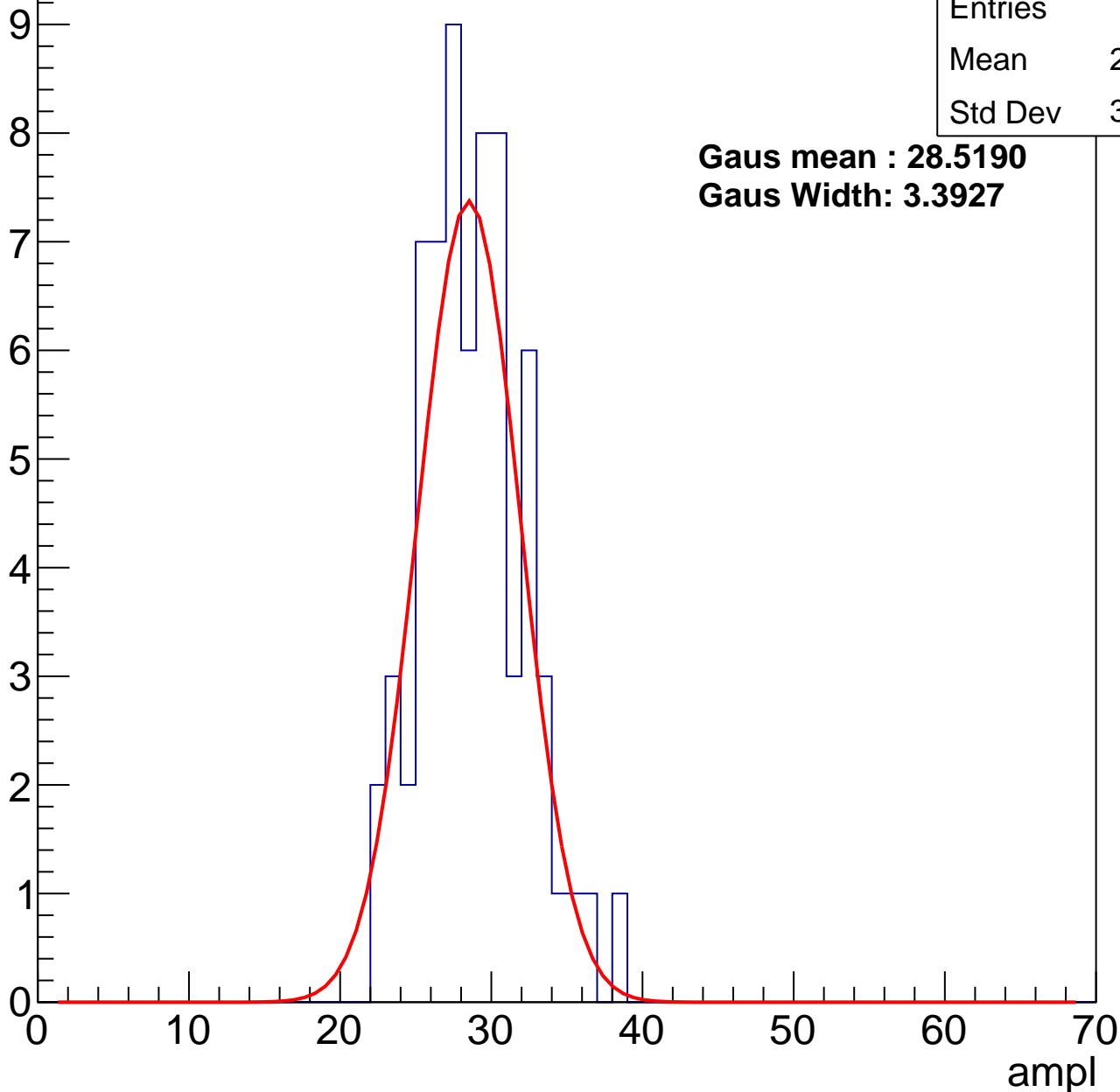
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	28.35
Std Dev	3.338

**Gaus mean : 28.5190**

**Gaus Width: 3.3927**



# B1L102S, U12-ch80, adc1

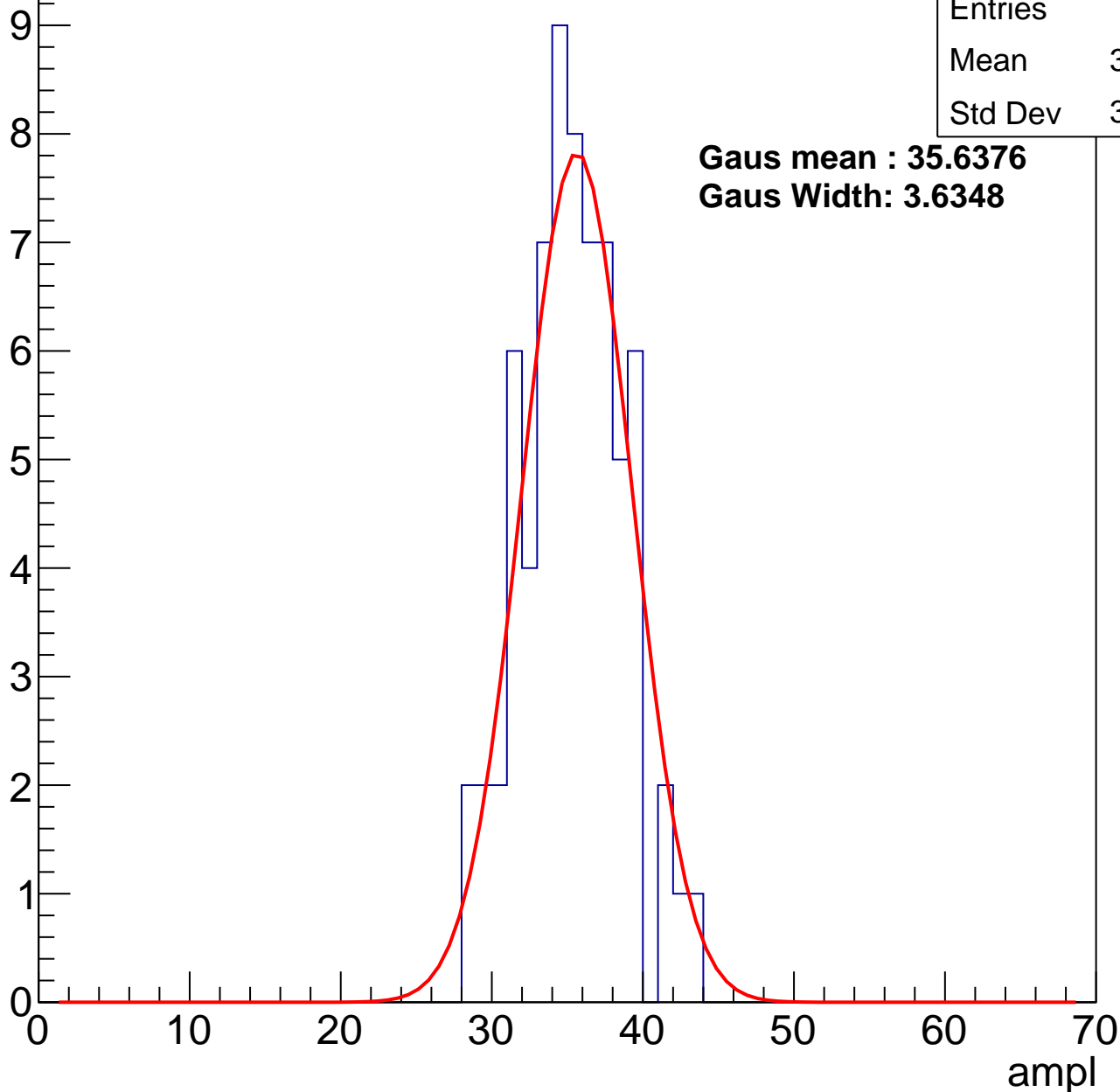
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	34.88
Std Dev	3.295

**Gaus mean : 35.6376**

**Gaus Width: 3.6348**



# B1L102S, U12-ch80, adc2

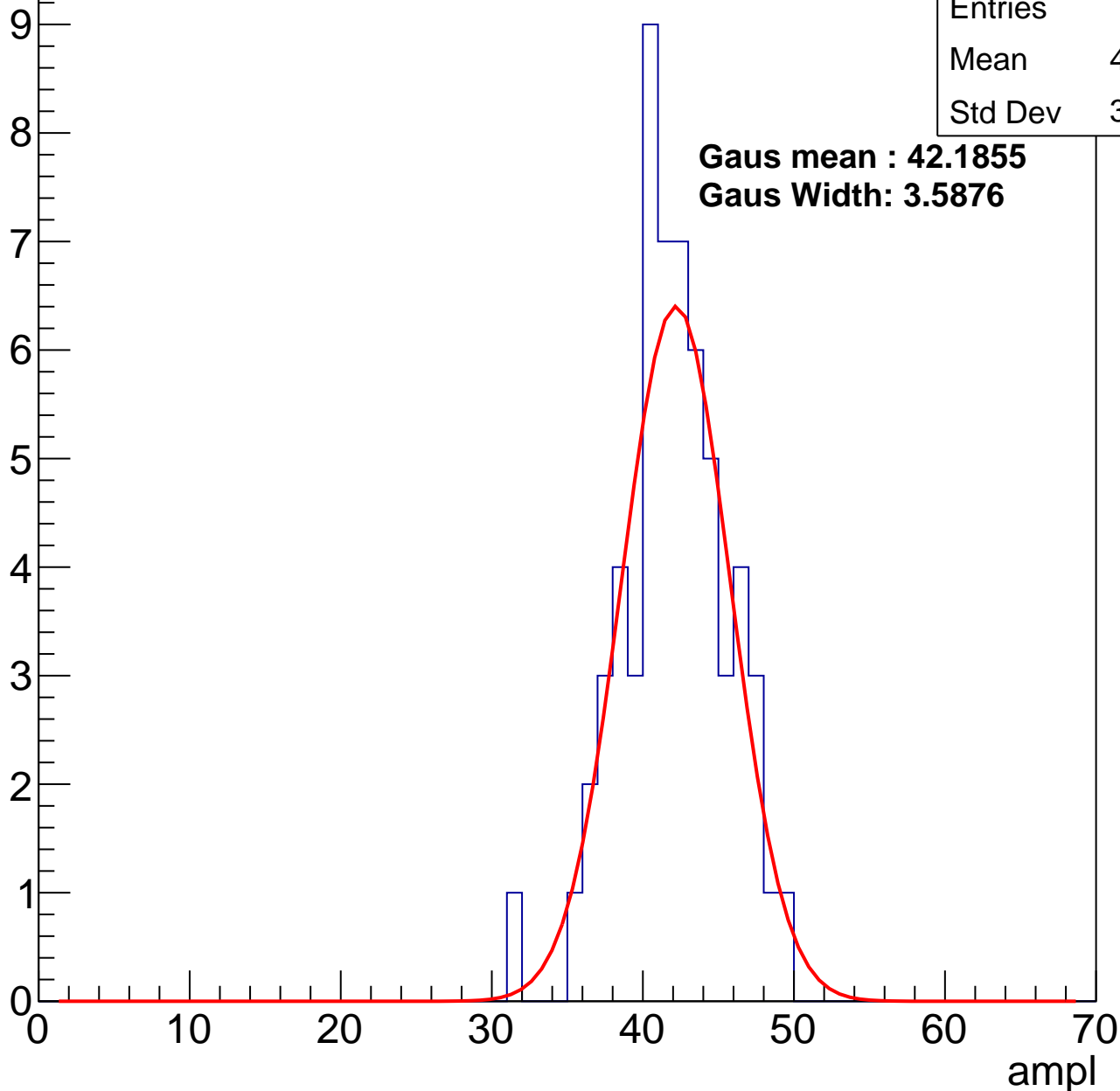
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	60
Mean	41.57
Std Dev	3.456

**Gaus mean : 42.1855**

**Gaus Width: 3.5876**

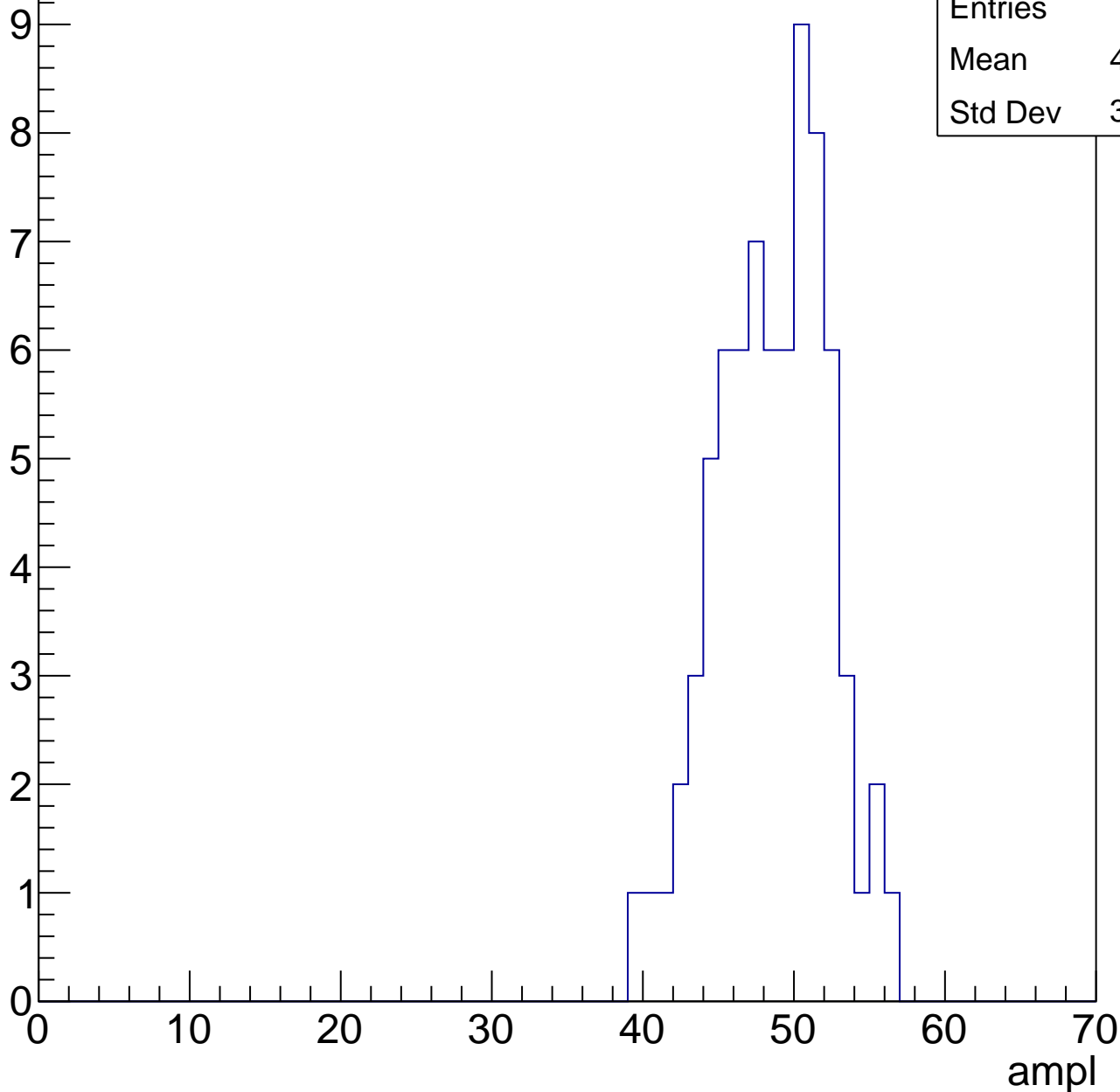


# B1L102S, U12-ch80, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	74
Mean	48.09
Std Dev	3.655

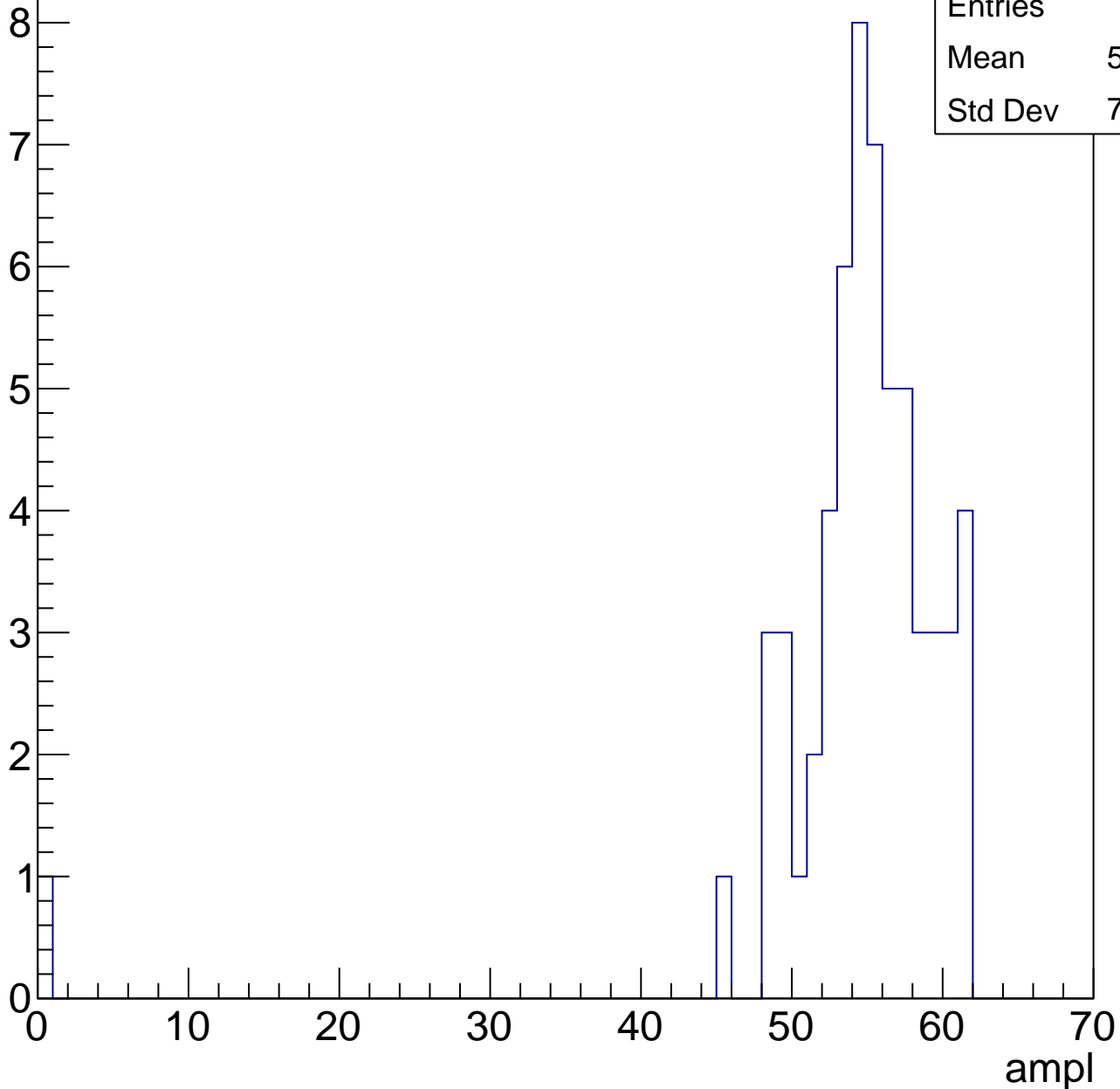


# B1L102S, U12-ch80, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	59
Mean	53.75
Std Dev	7.952

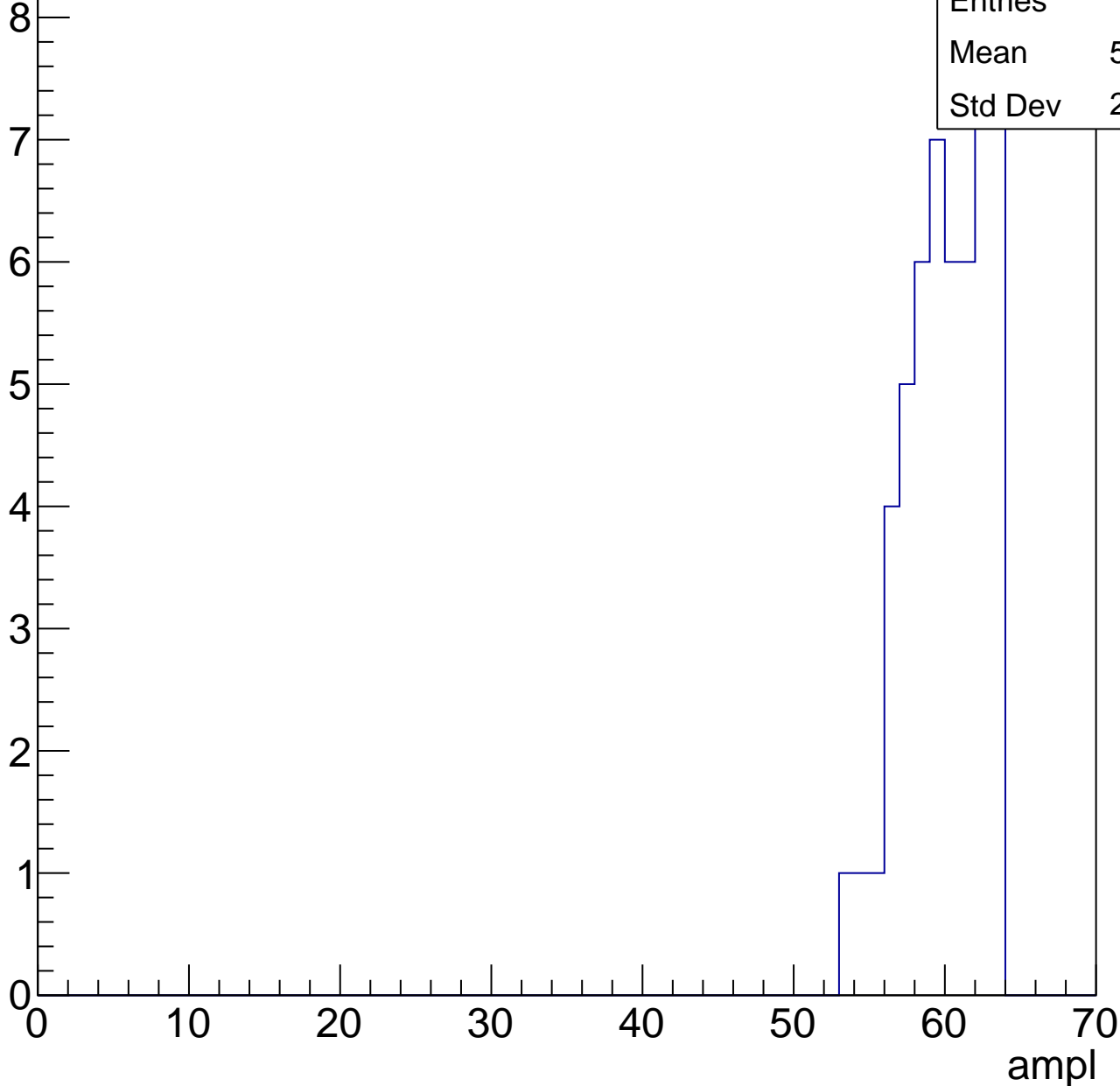


# B1L102S, U12-ch80, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

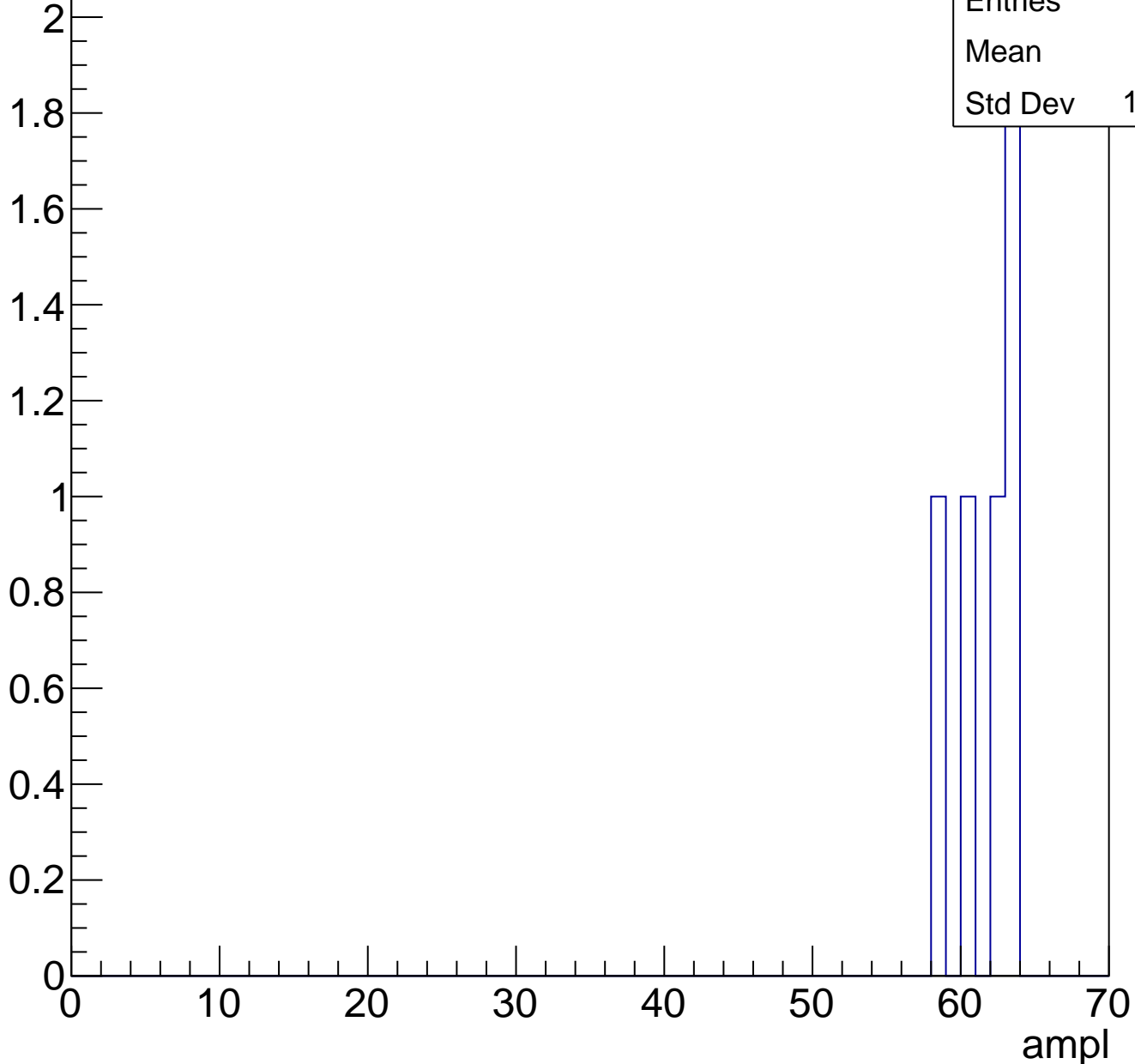
Entries	53
Mean	59.58
Std Dev	2.573



# B1L102S, U12-ch80, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



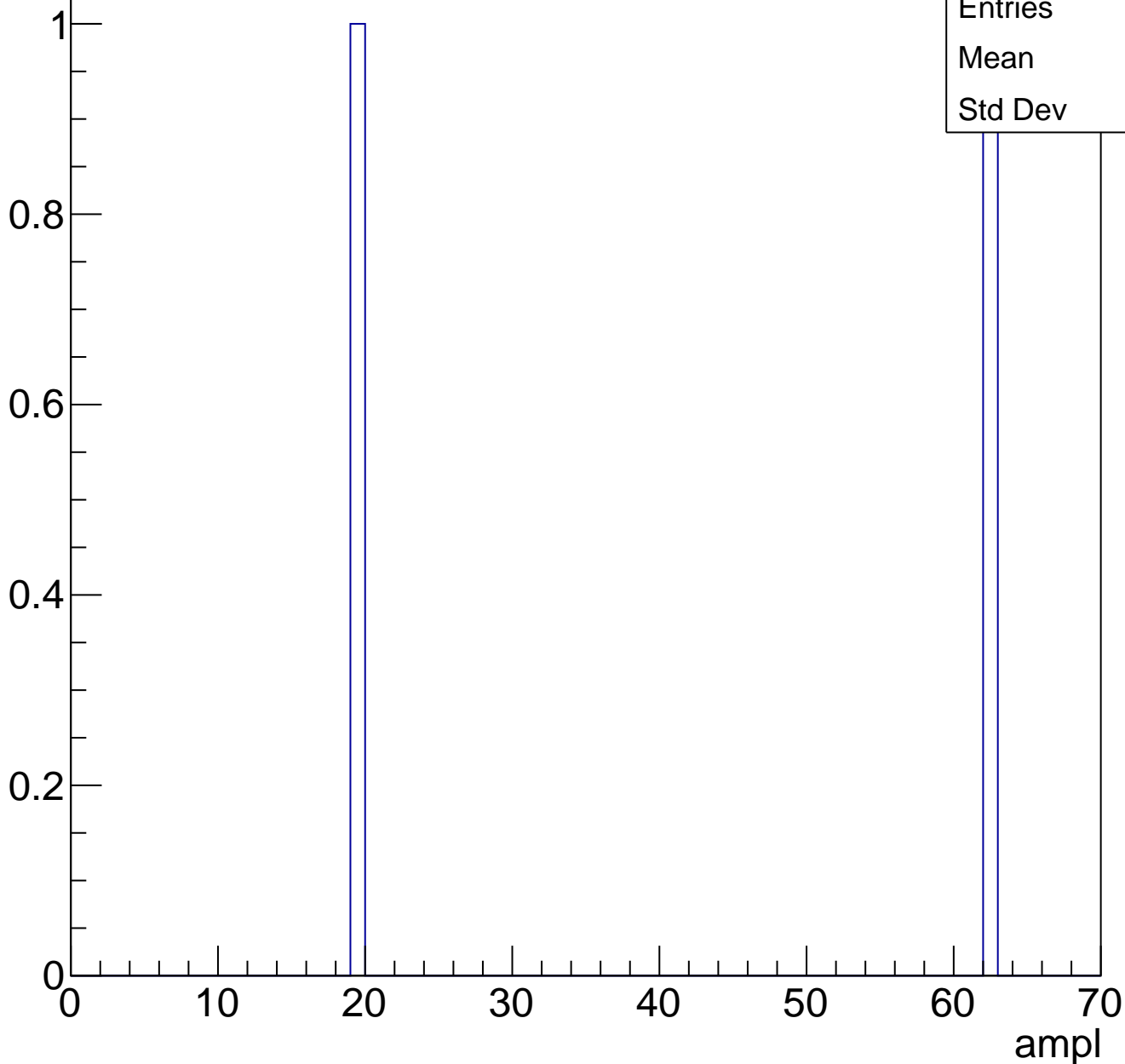
Entries	5
Mean	61.2
Std Dev	1.939



# B1L102S, U12-ch80, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U12-ch81, adc0

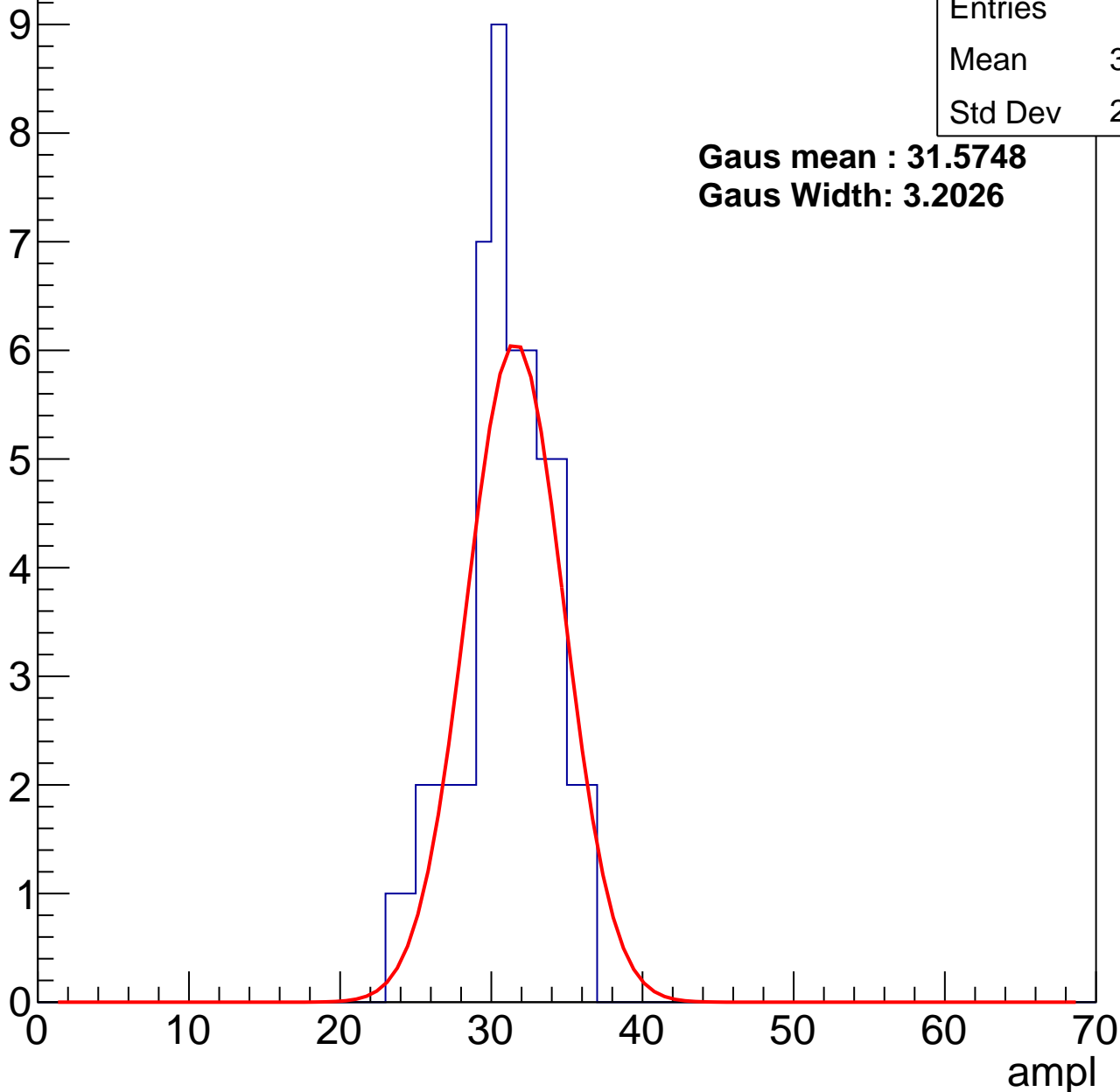
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	52
Mean	30.52
Std Dev	2.984

**Gaus mean : 31.5748**

**Gaus Width: 3.2026**



# B1L102S, U12-ch81, adc1

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	88
Mean	37.4
Std Dev	3.688

**Gaus mean : 37.8709**

**Gaus Width: 4.3702**

10

8

6

4

2

0

0

10

20

30

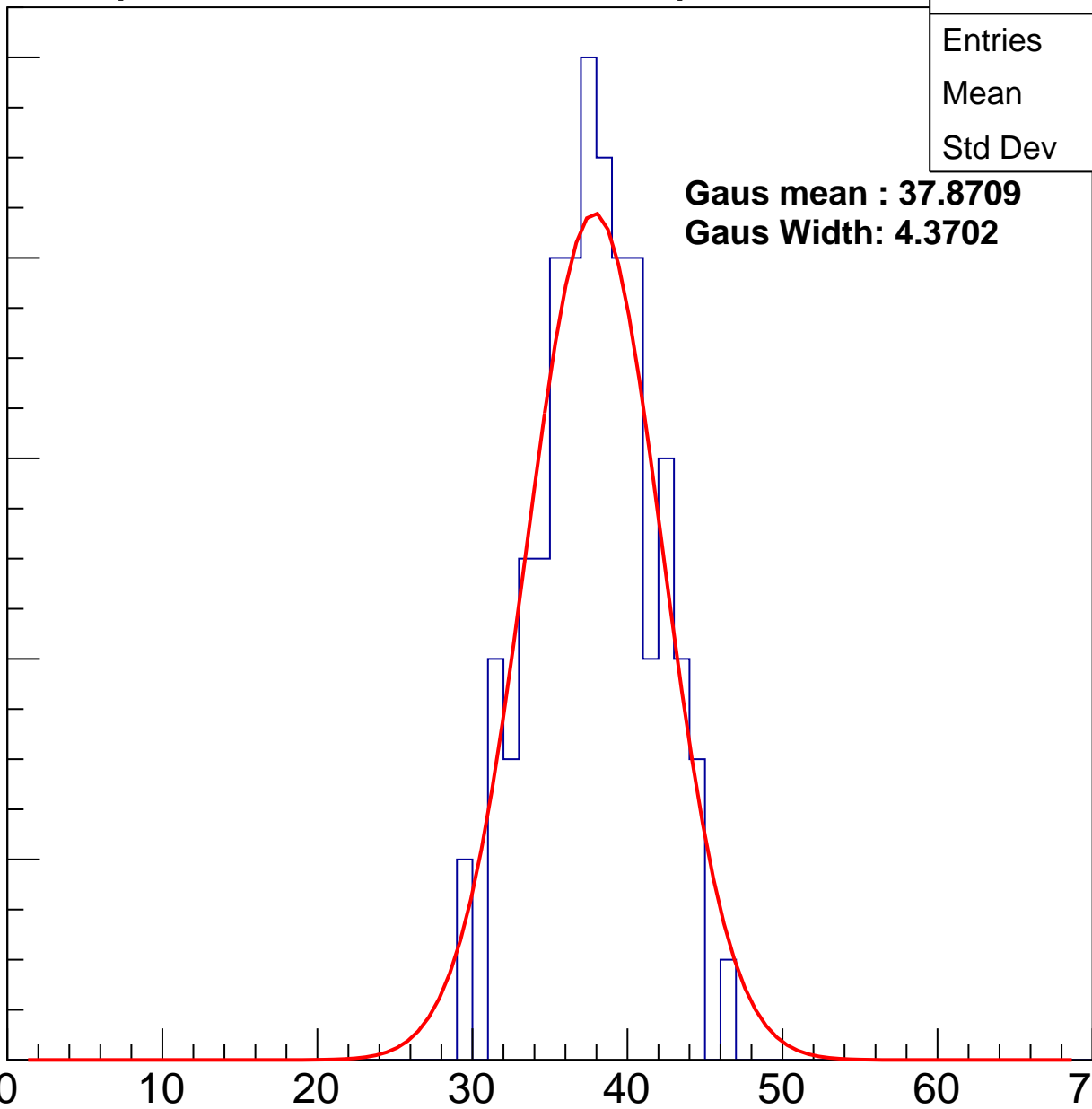
40

50

60

70

ampl



# B1L102S, U12-ch81, adc2

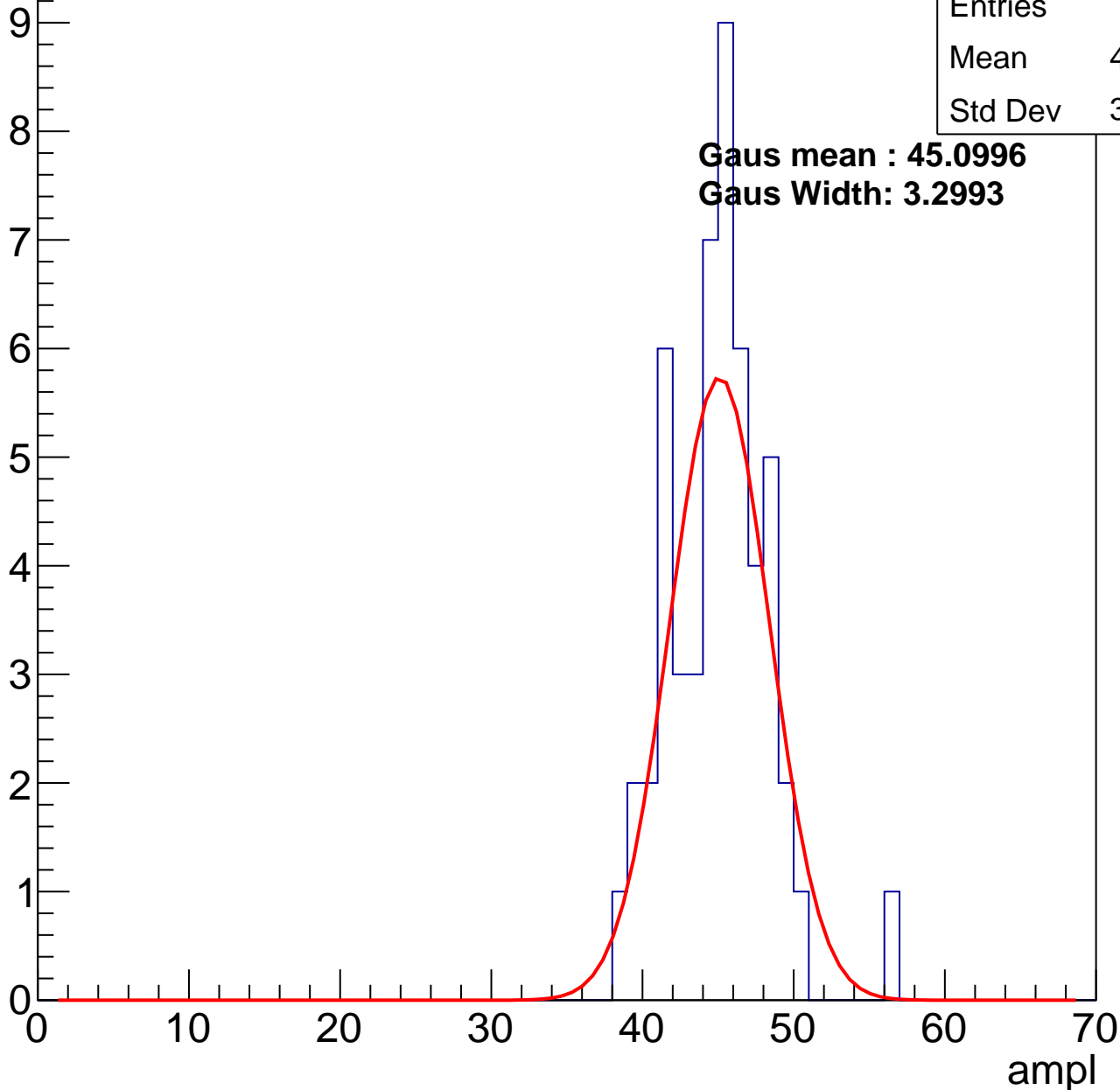
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	52
Mean	44.58
Std Dev	3.248

**Gaus mean : 45.0996**

**Gaus Width: 3.2993**

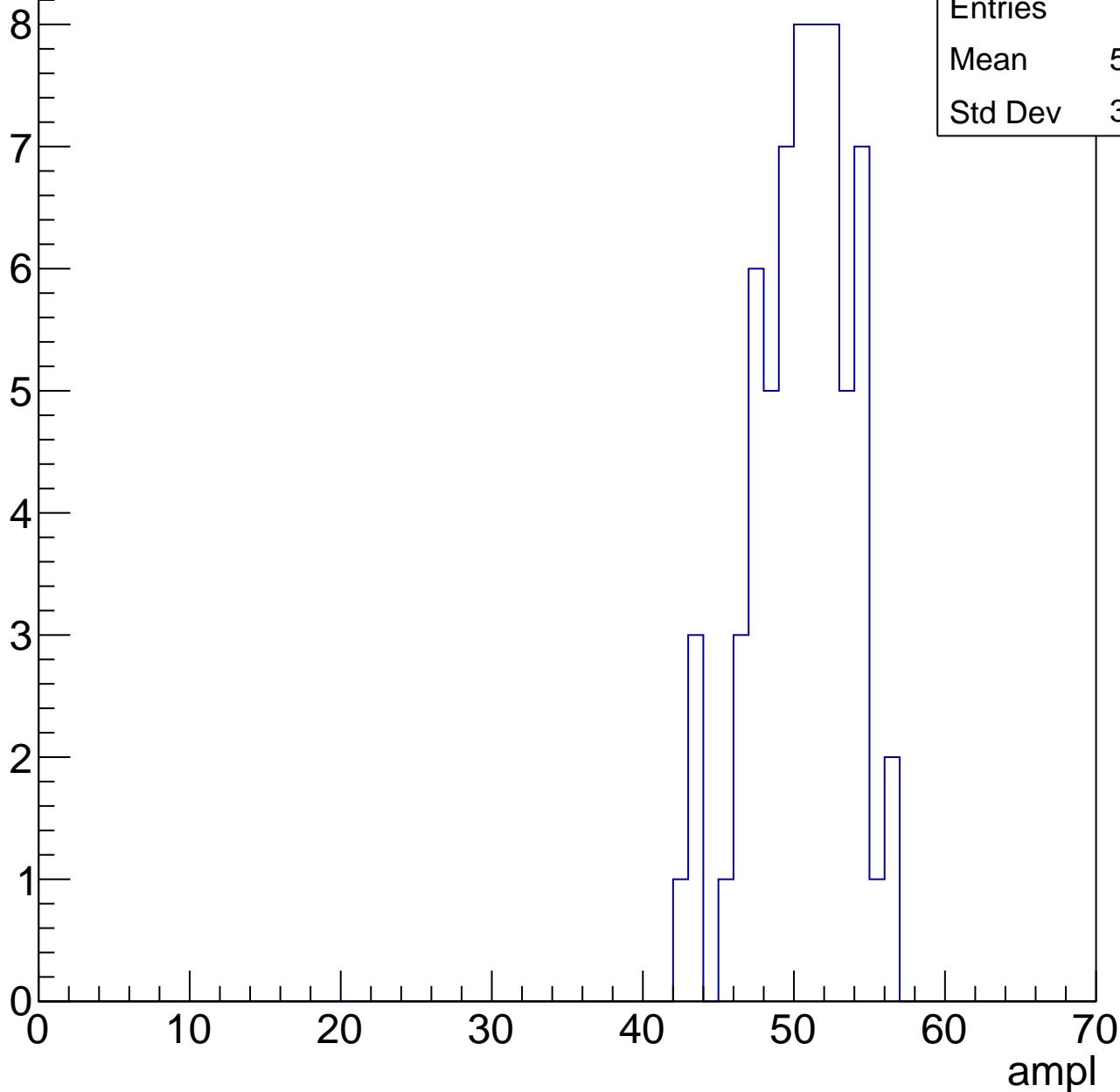


# B1L102S, U12-ch81, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

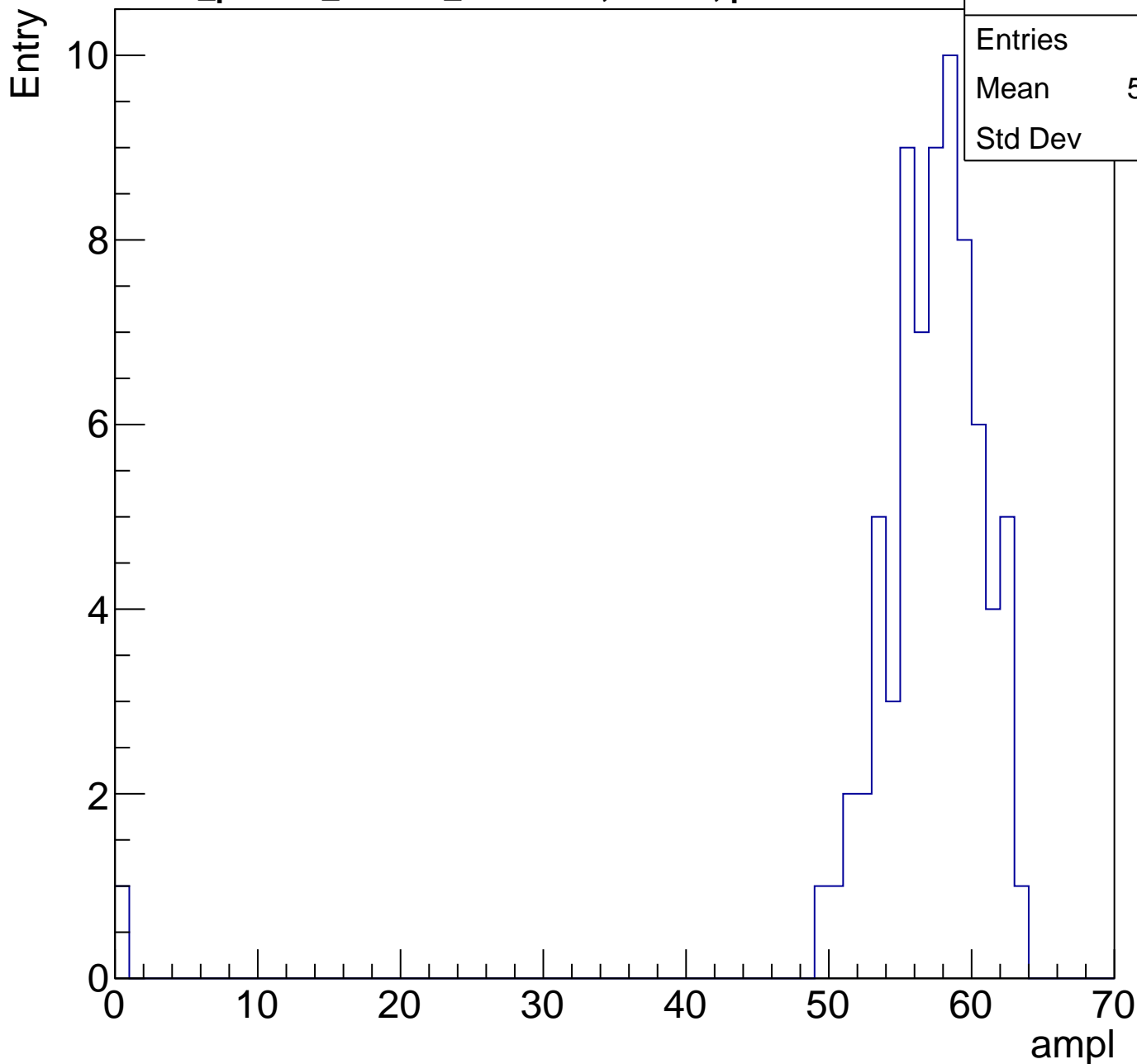
Entries	65
Mean	50.05
Std Dev	3.184



# B1L102S, U12-ch81, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	74
Mean	56.23
Std Dev	7.27

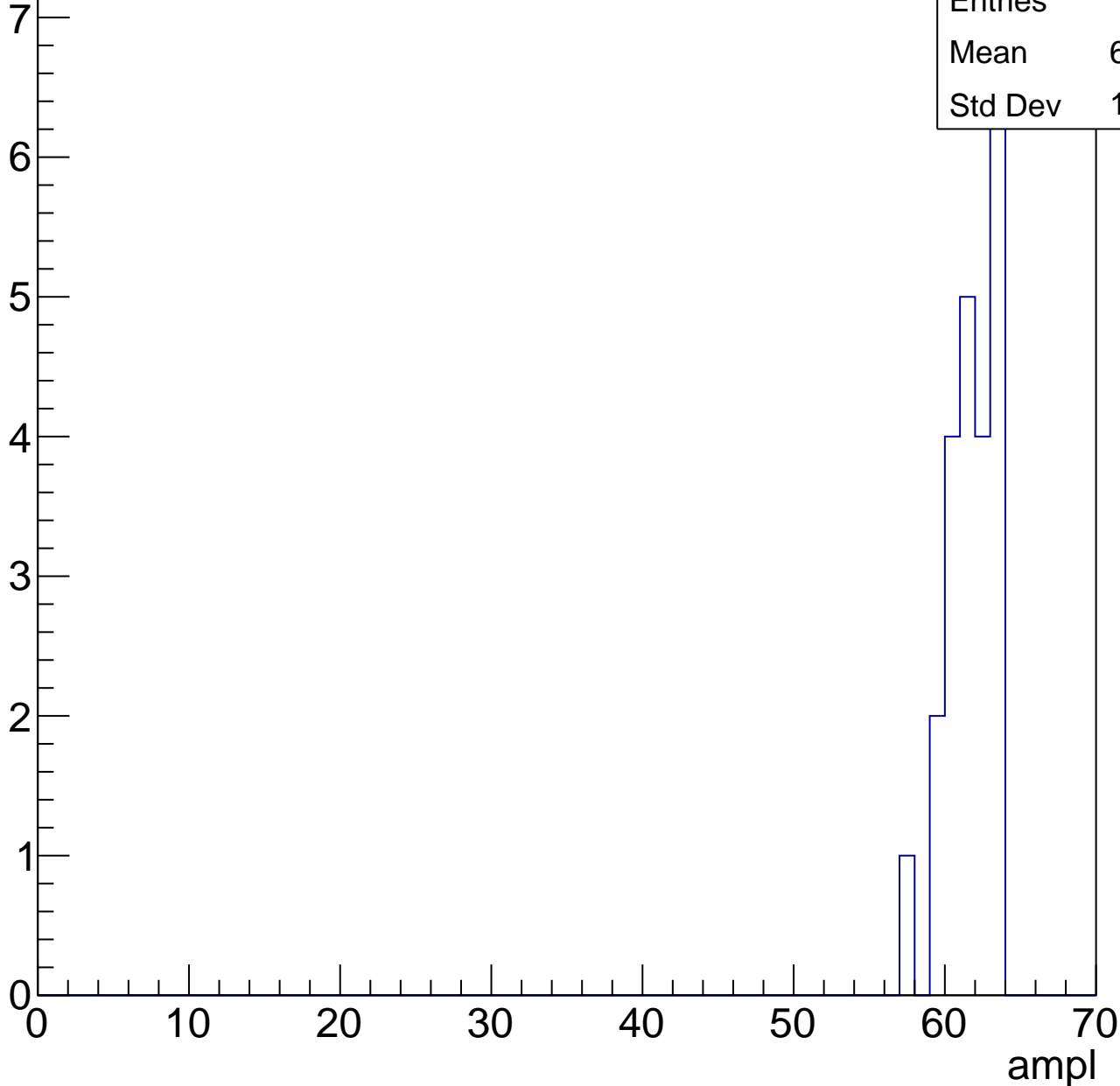


# B1L102S, U12-ch81, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	23
Mean	61.26
Std Dev	1.594



# B1L102S, U12-ch81, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	4
Mean	62.25
Std Dev	0.8292

ampl

0 10 20 30 40 50 60 70



# B1L102S, U12-ch81, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U12-ch82, adc0

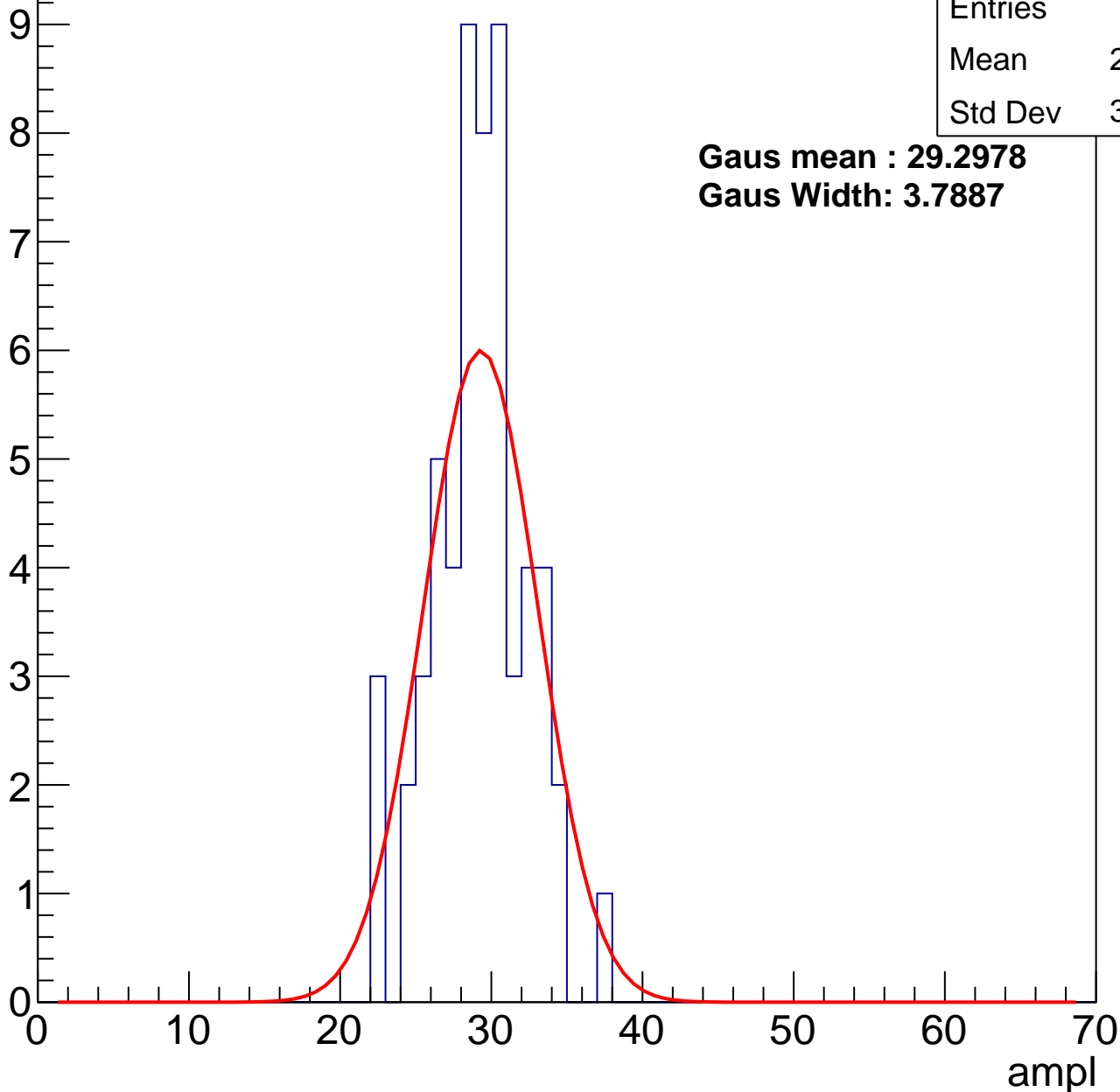
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	57
Mean	28.75
Std Dev	3.097

**Gaus mean : 29.2978**

**Gaus Width: 3.7887**



# B1L102S, U12-ch82, adc1

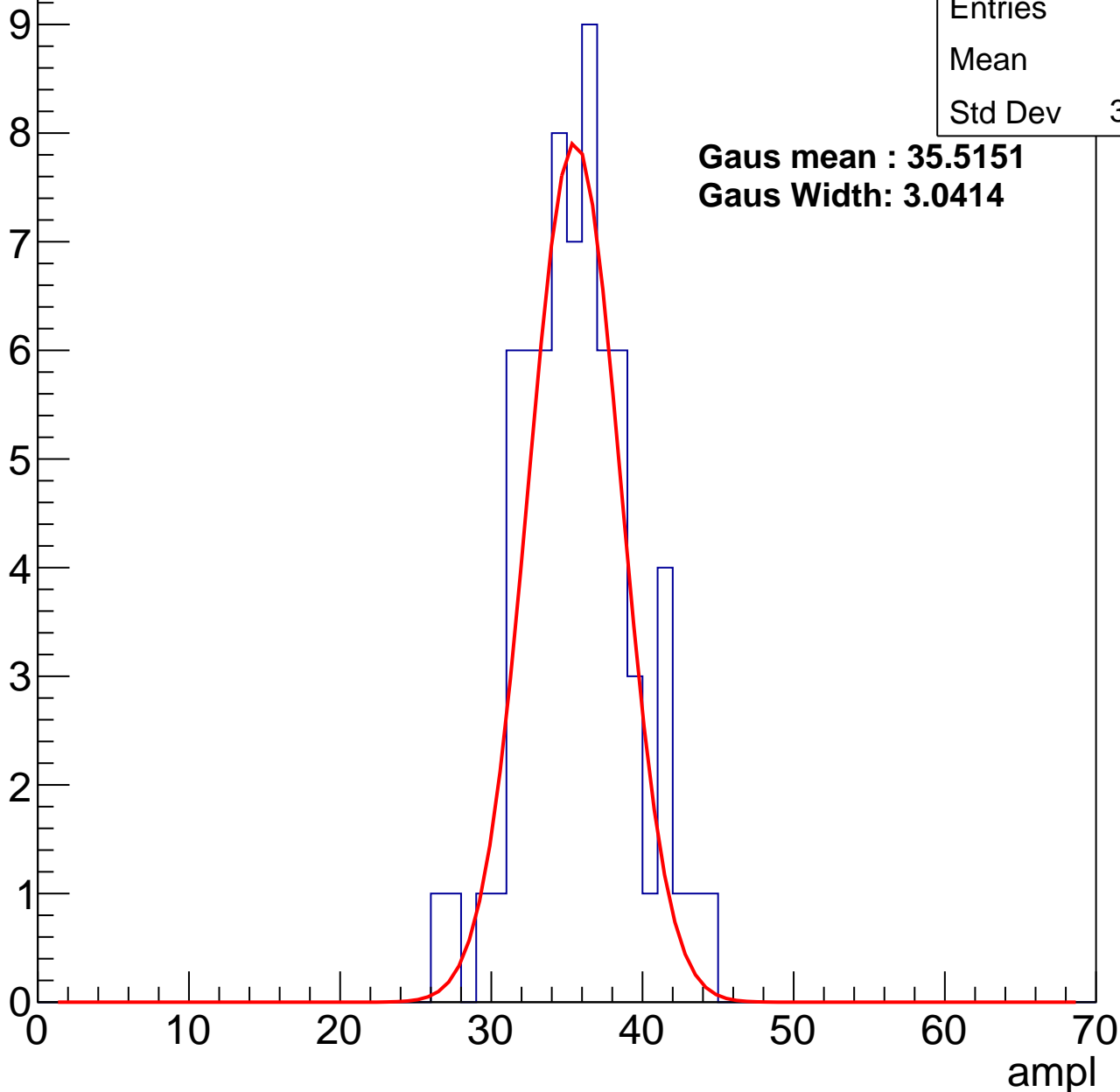
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	35.2
Std Dev	3.578

**Gaus mean : 35.5151**

**Gaus Width: 3.0414**



# B1L102S, U12-ch82, adc2

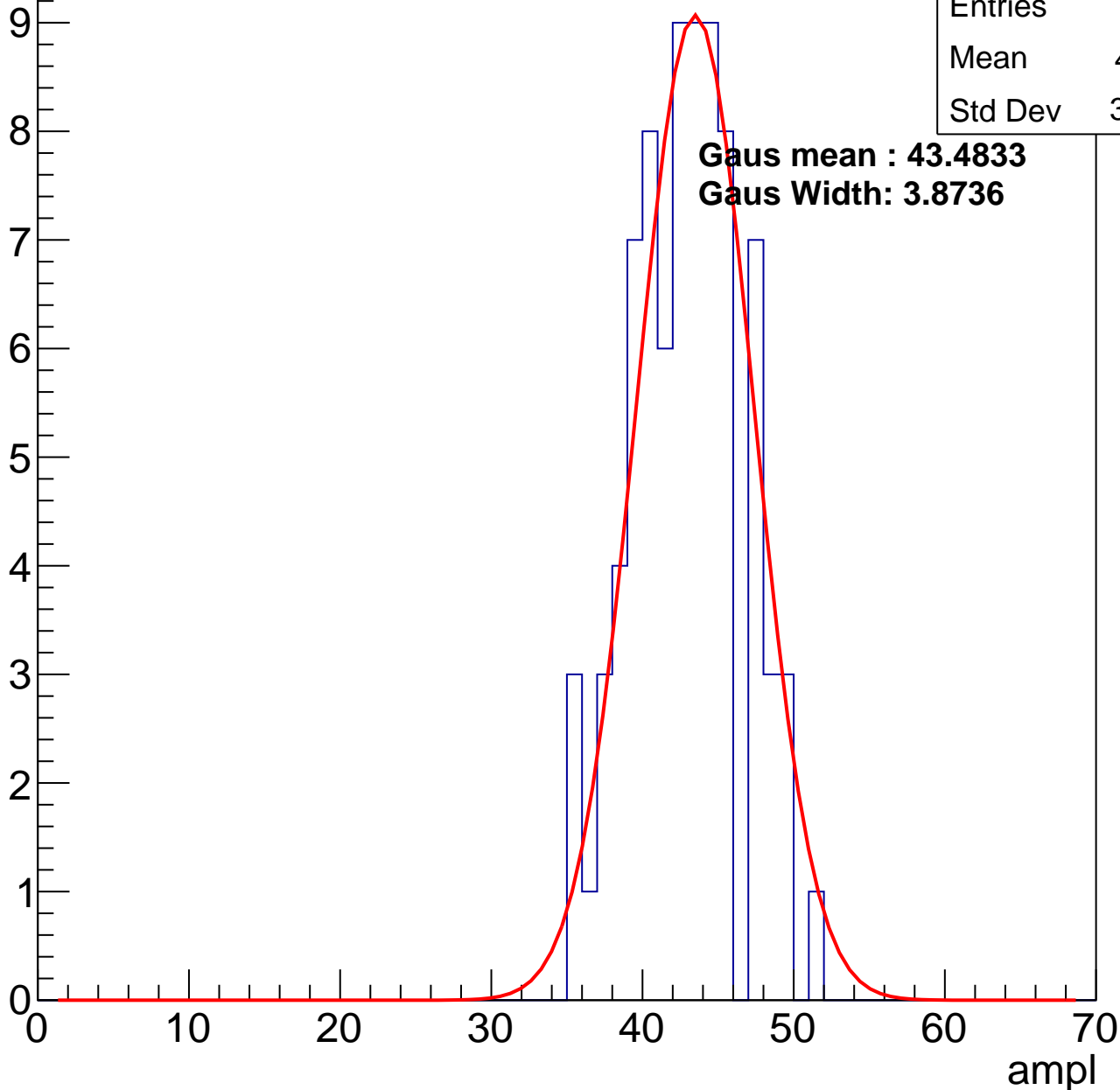
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	81
Mean	42.41
Std Dev	3.579

**Gaus mean : 43.4833**

**Gaus Width: 3.8736**



# B1L102S, U12-ch82, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	65
Mean	49.89
Std Dev	3.287

Entry

10

8

6

4

2

0

0

10

20

30

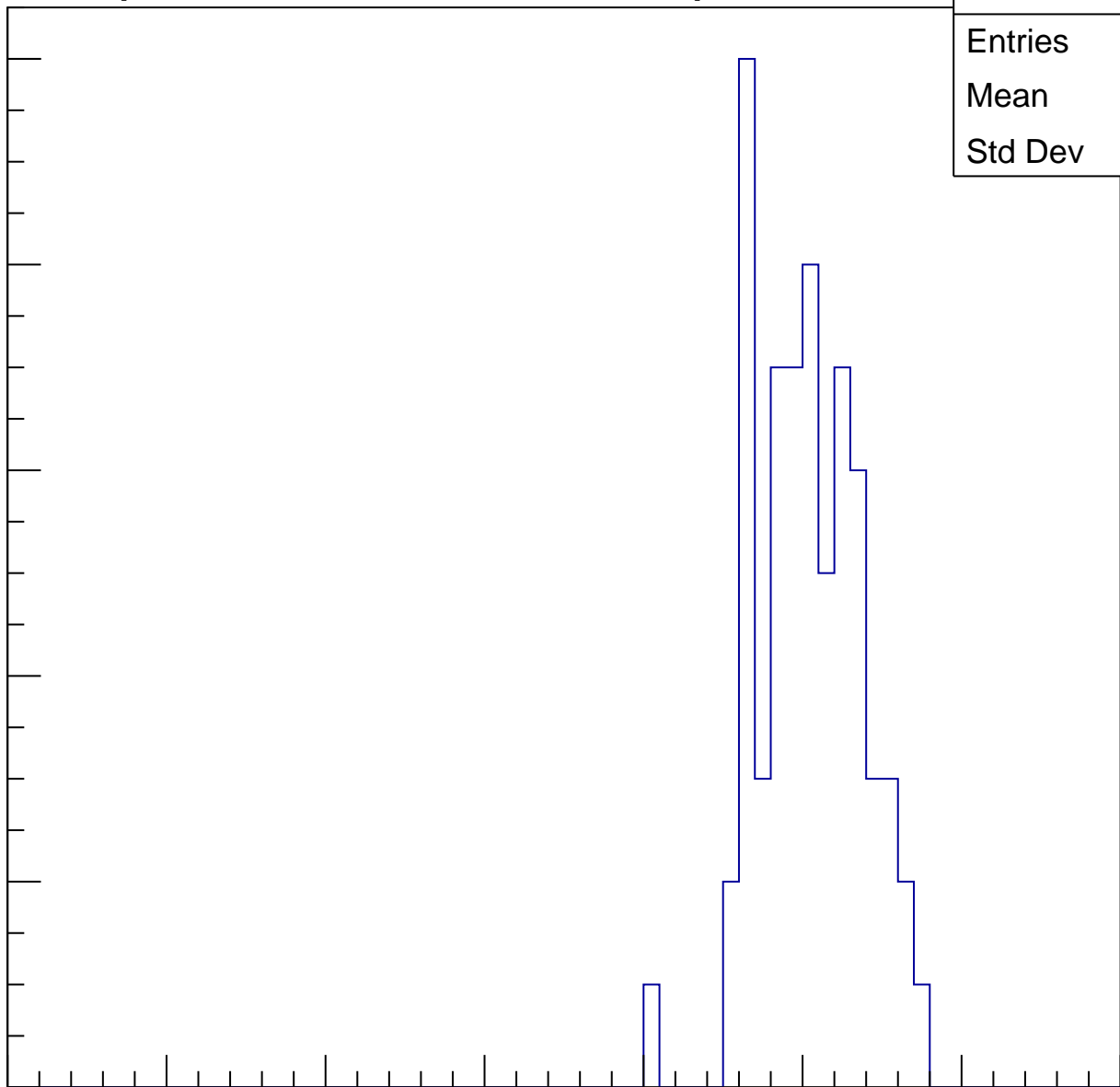
40

50

60

70

ampl

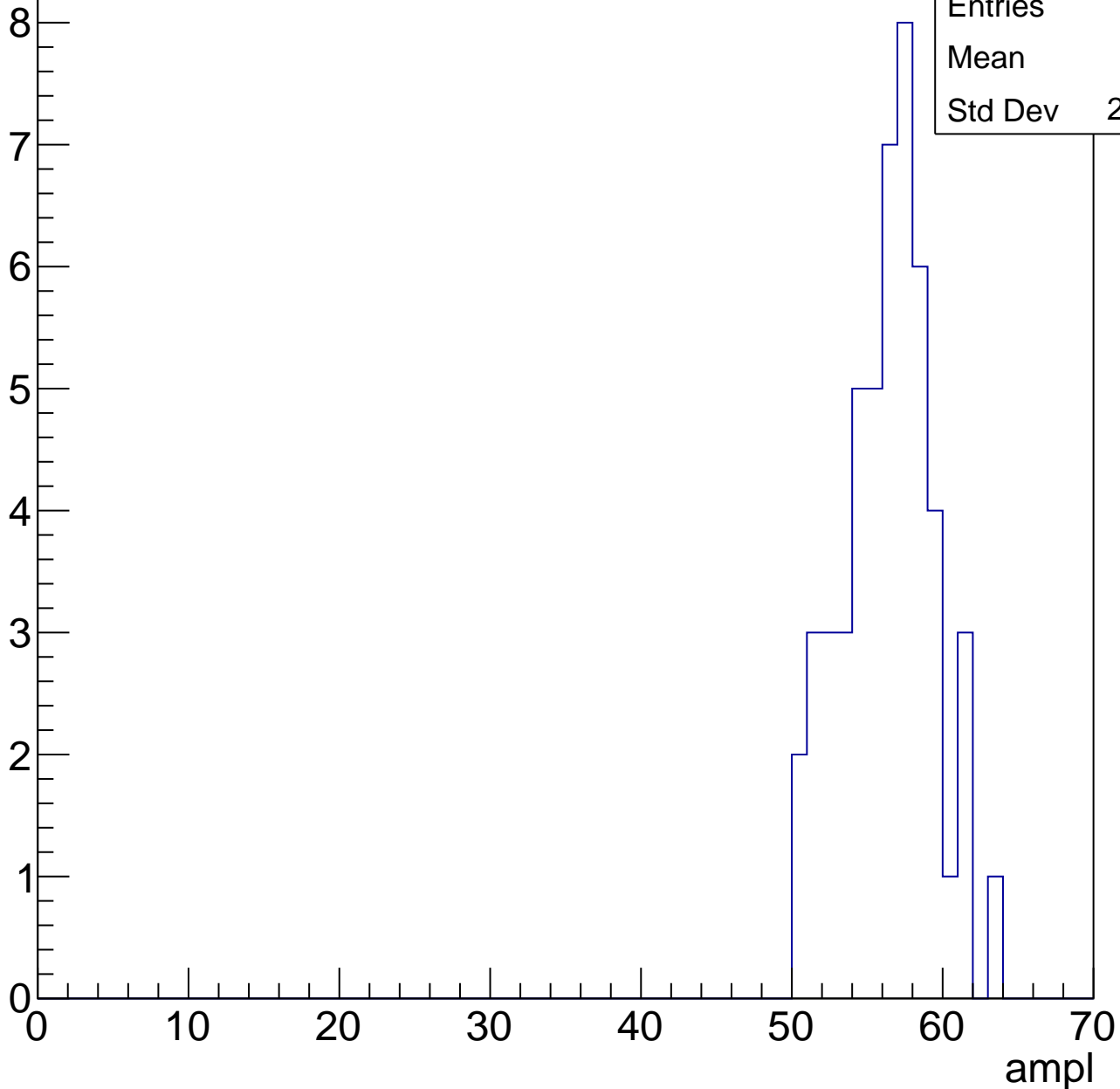


# B1L102S, U12-ch82, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	51
Mean	55.9
Std Dev	2.985

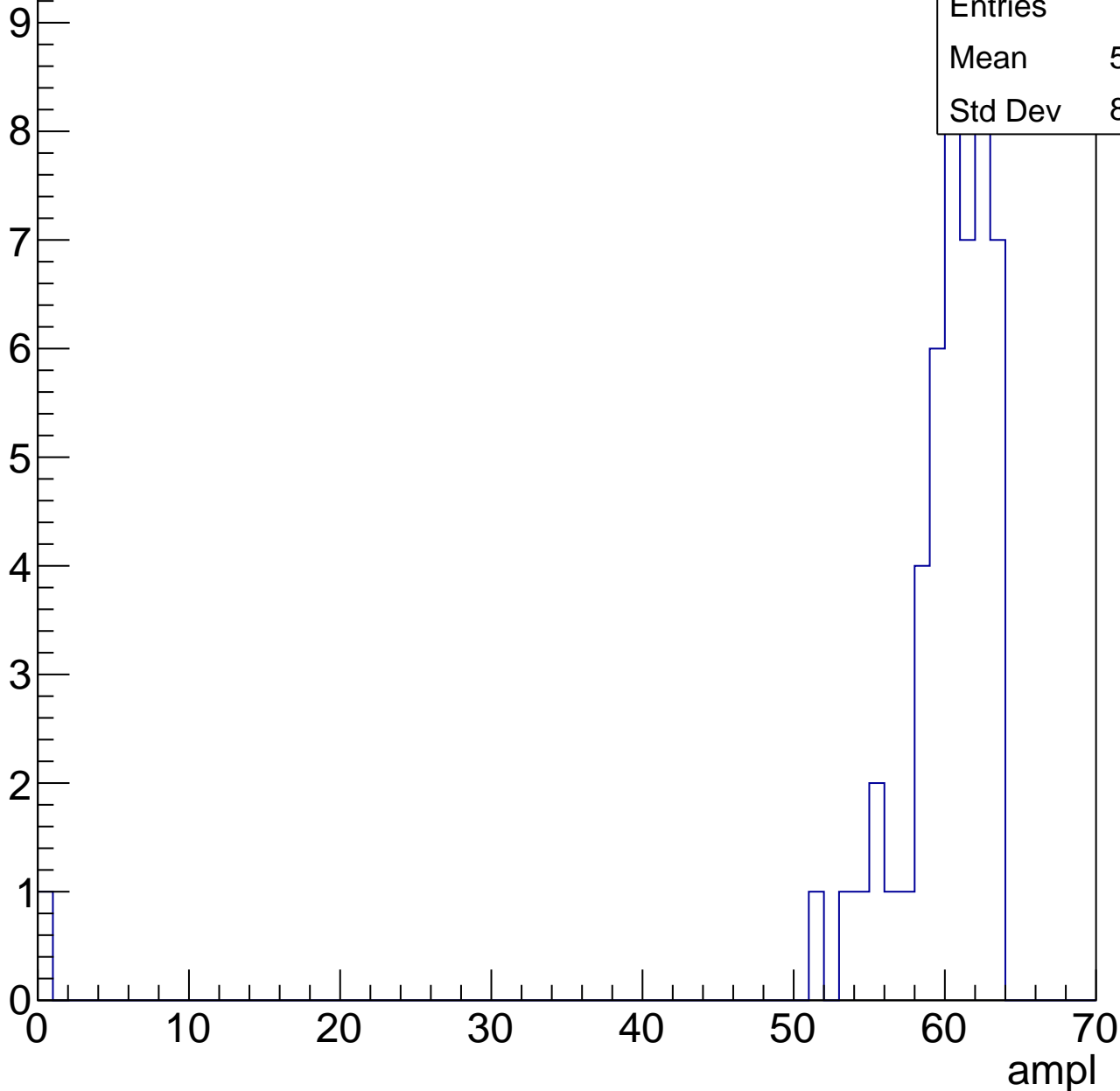


# B1L102S, U12-ch82, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	49
Mean	58.63
Std Dev	8.896



# B1L102S, U12-ch82, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	5
Mean	60.4
Std Dev	3.382

ampl

0 10 20 30 40 50 60 70



# B1L102S, U12-ch82, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L102S, U12-ch83, adc0

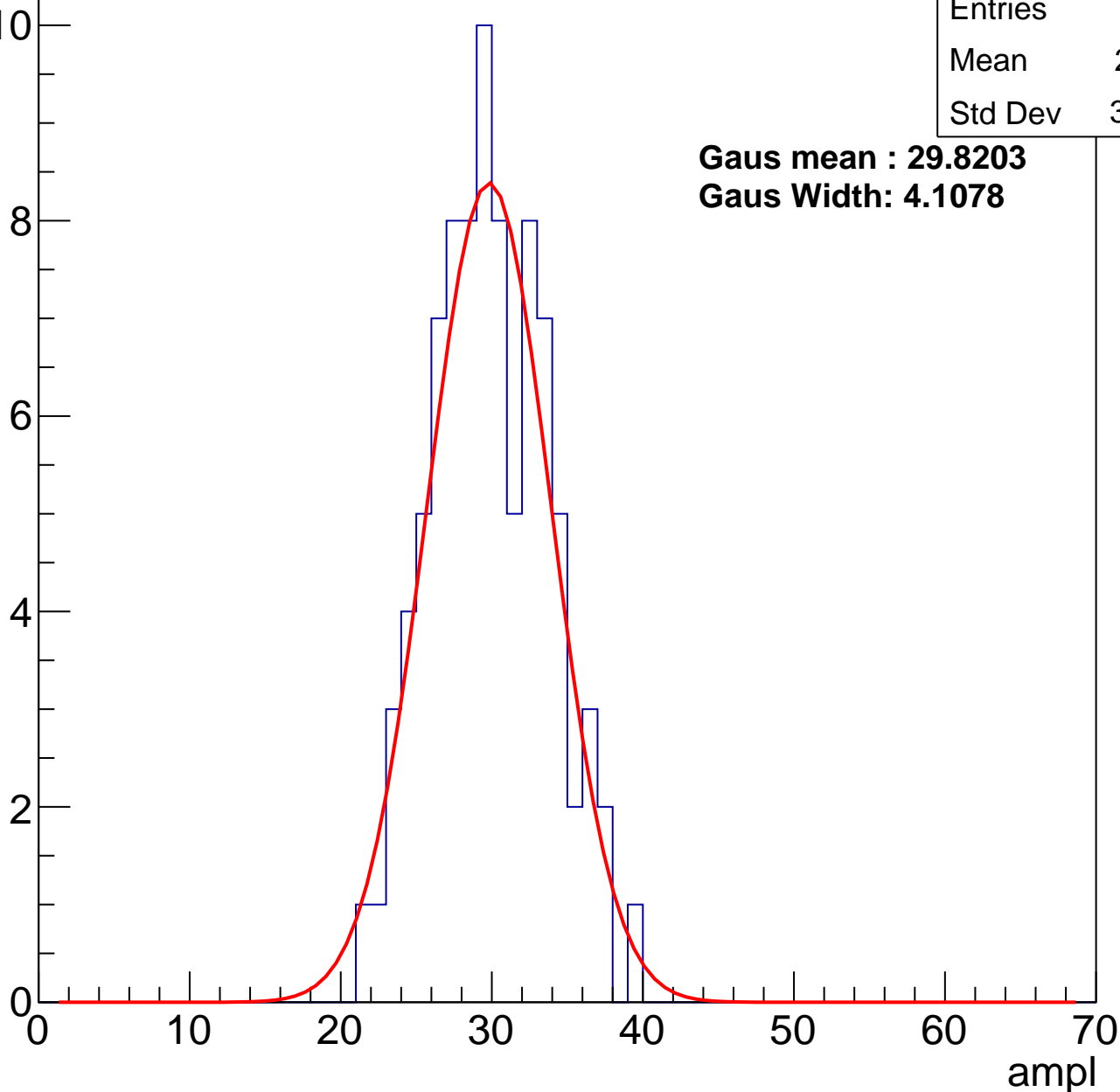
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	88
Mean	29.41
Std Dev	3.804

**Gaus mean : 29.8203**

**Gaus Width: 4.1078**



# B1L102S, U12-ch83, adc1

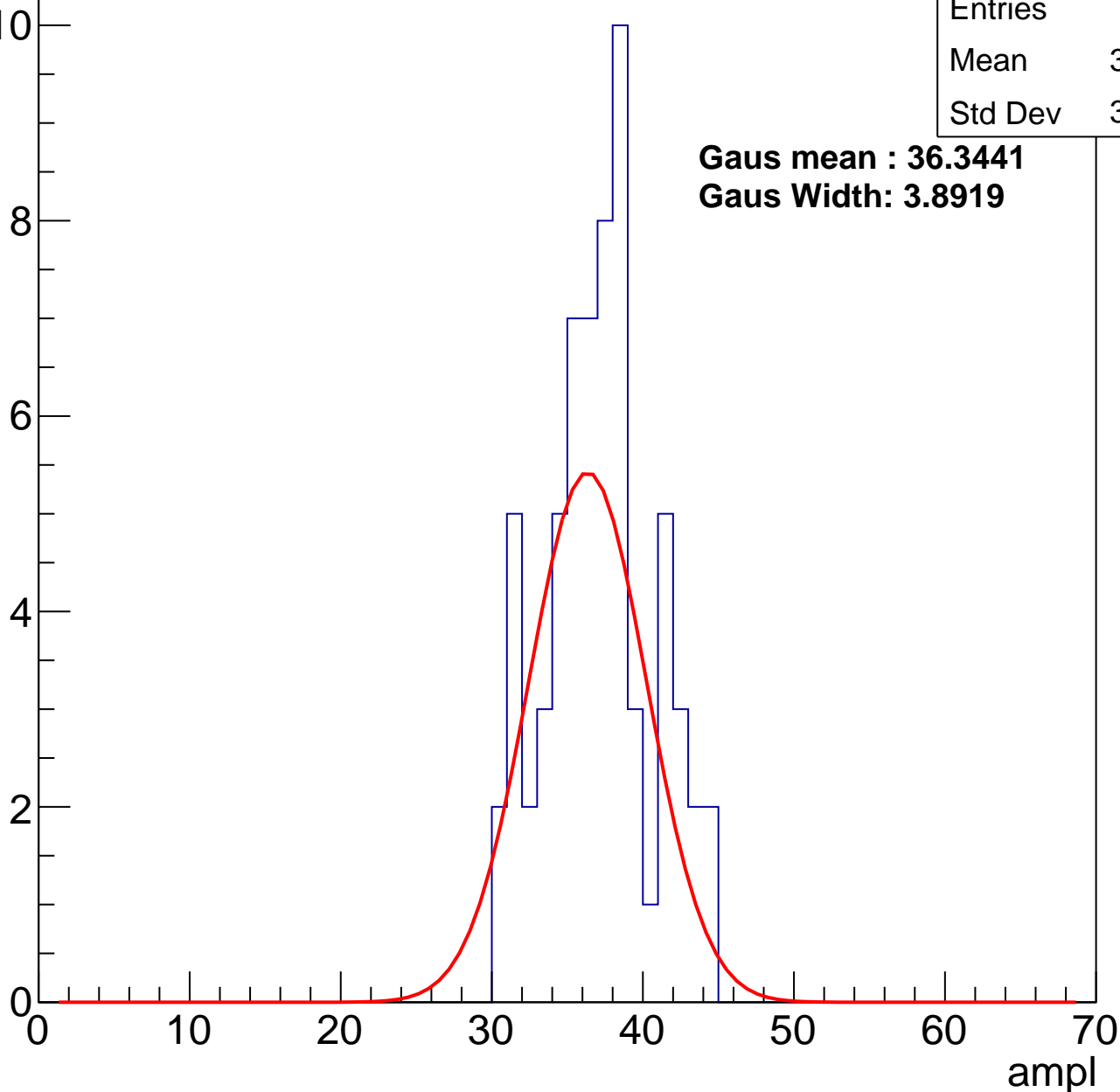
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	65
Mean	36.66
Std Dev	3.518

**Gaus mean : 36.3441**

**Gaus Width: 3.8919**



# B1L102S, U12-ch83, adc2

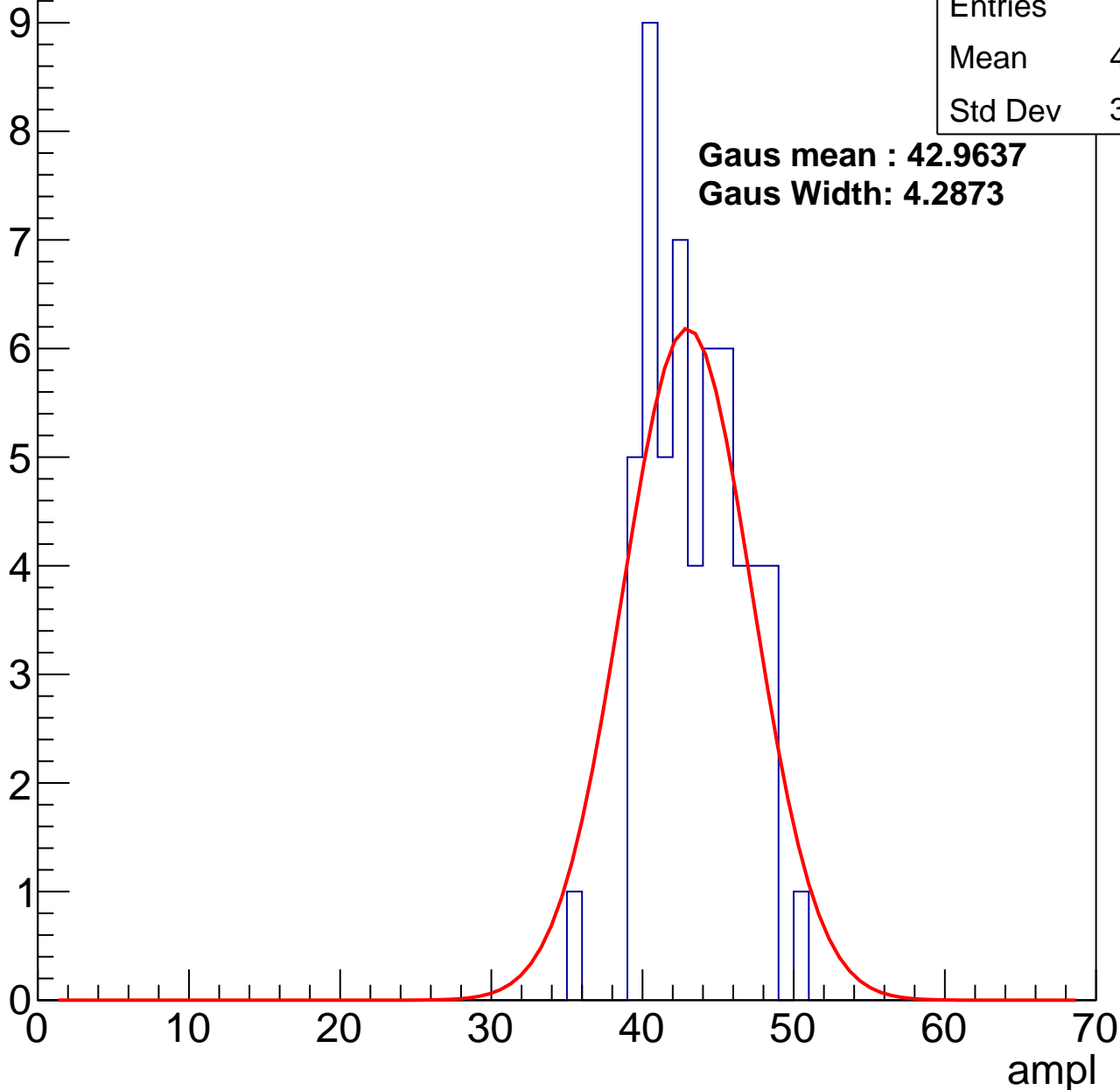
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	56
Mean	43.02
Std Dev	3.079

**Gaus mean : 42.9637**

**Gaus Width: 4.2873**

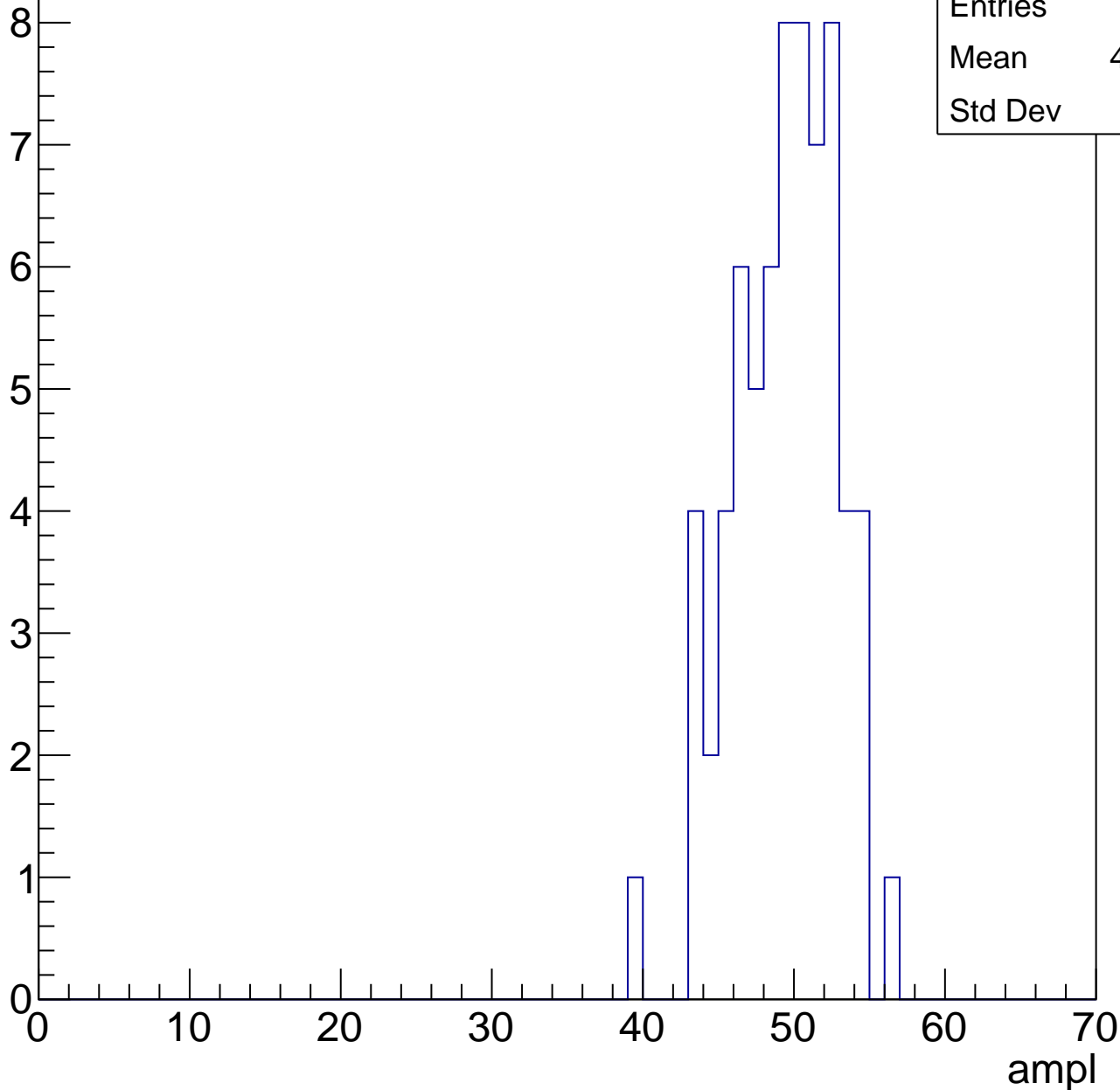


# B1L102S, U12-ch83, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	48.93
Std Dev	3.34

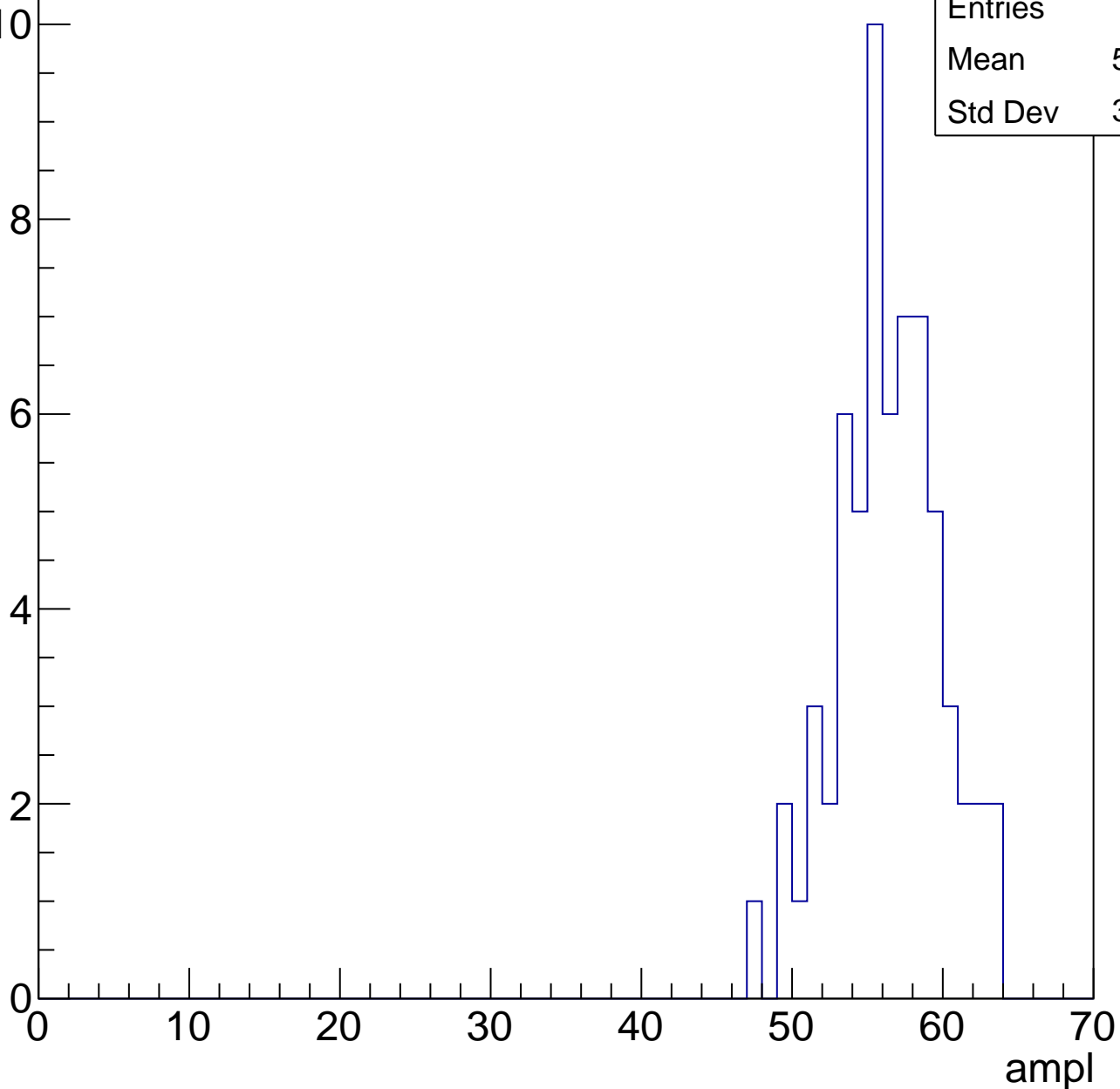


# B1L102S, U12-ch83, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	55.91
Std Dev	3.431



# B1L102S, U12-ch83, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	43
Mean	58.6
Std Dev	9.314

ampl

0 10 20 30 40 50 60 70

1

2

3

4

5

6

7

8

# B1L102S, U12-ch83, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	4
Mean	62.5
Std Dev	0.5



# B1L102S, U12-ch83, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L102S, U12-ch84, adc0

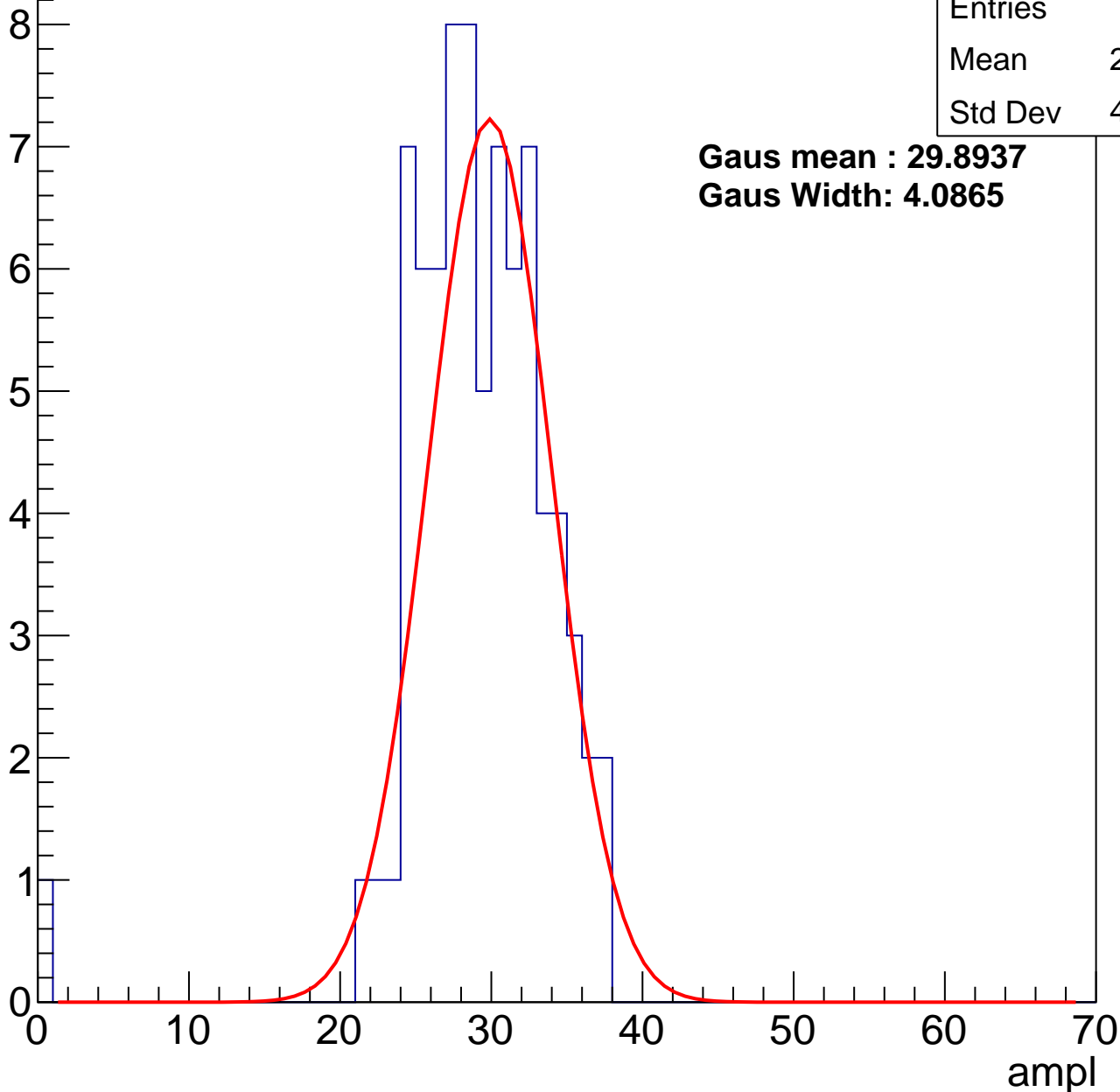
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	79
Mean	28.66
Std Dev	4.953

**Gaus mean : 29.8937**

**Gaus Width: 4.0865**



# B1L102S, U12-ch84, adc1

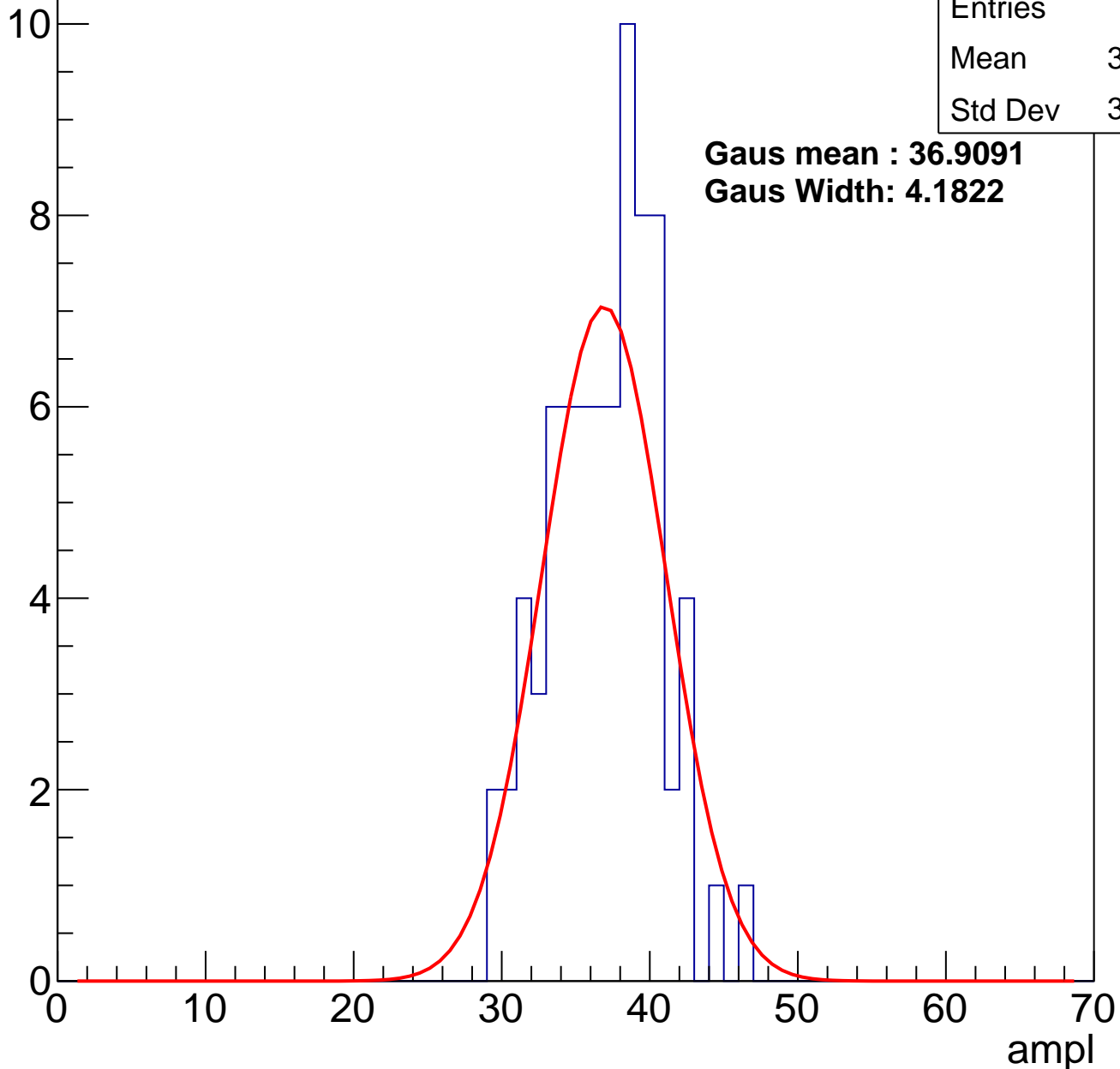
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	75
Mean	36.53
Std Dev	3.623

**Gaus mean : 36.9091**

**Gaus Width: 4.1822**

Entry



# B1L102S, U12-ch84, adc2

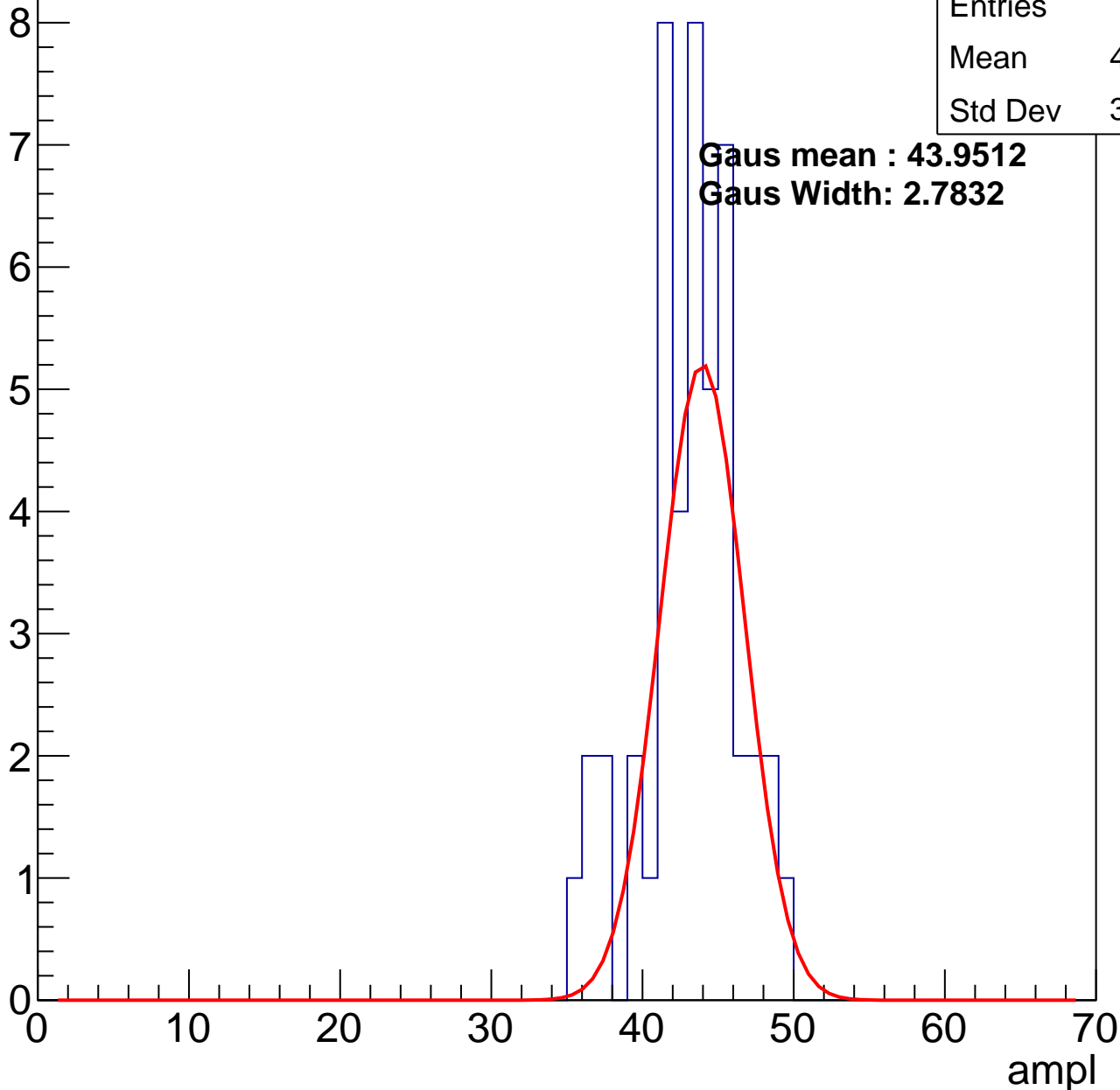
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	47
Mean	42.66
Std Dev	3.178

**Gaus mean : 43.9512**

**Gaus Width: 2.7832**

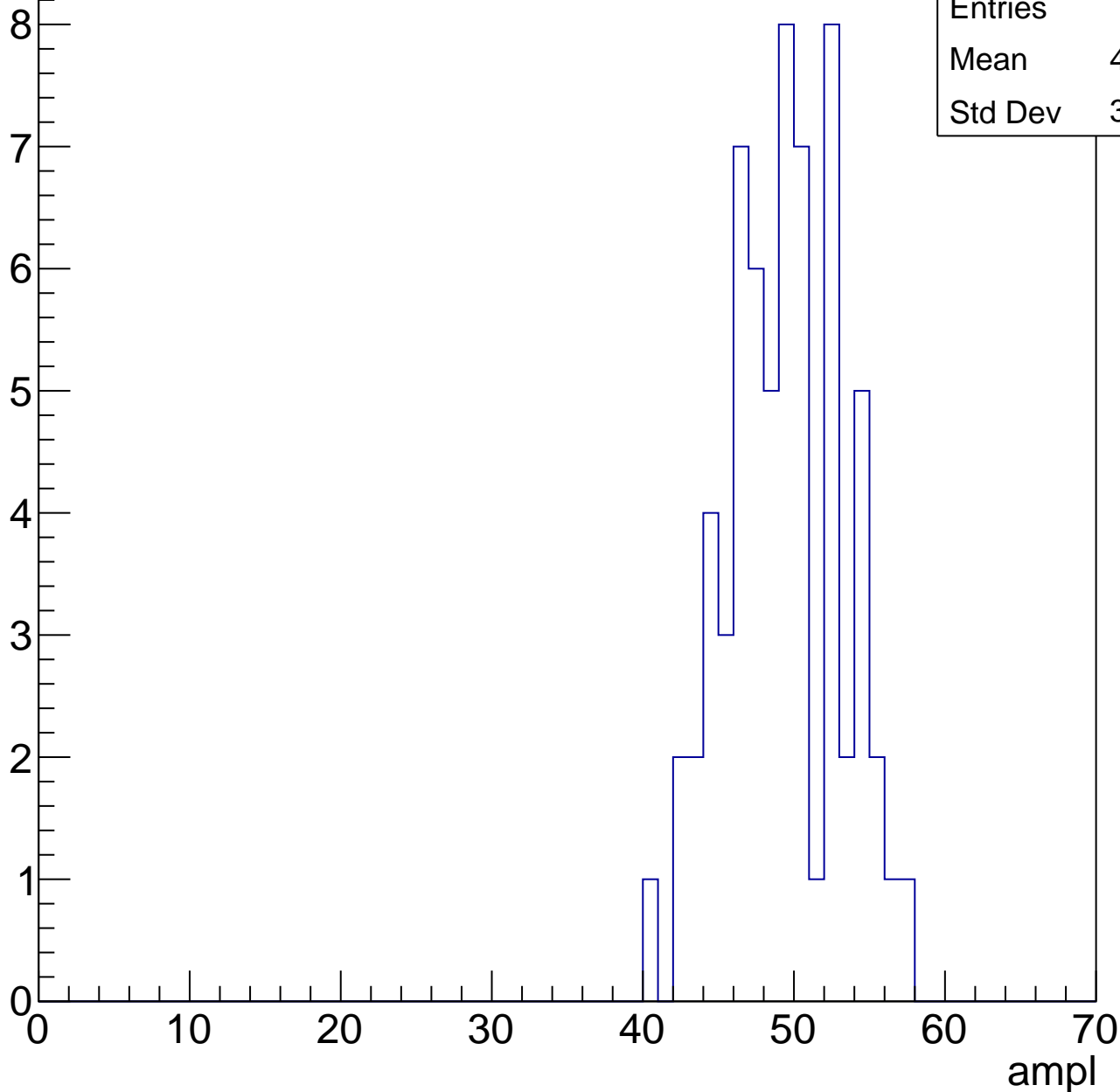


# B1L102S, U12-ch84, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	65
Mean	48.82
Std Dev	3.749

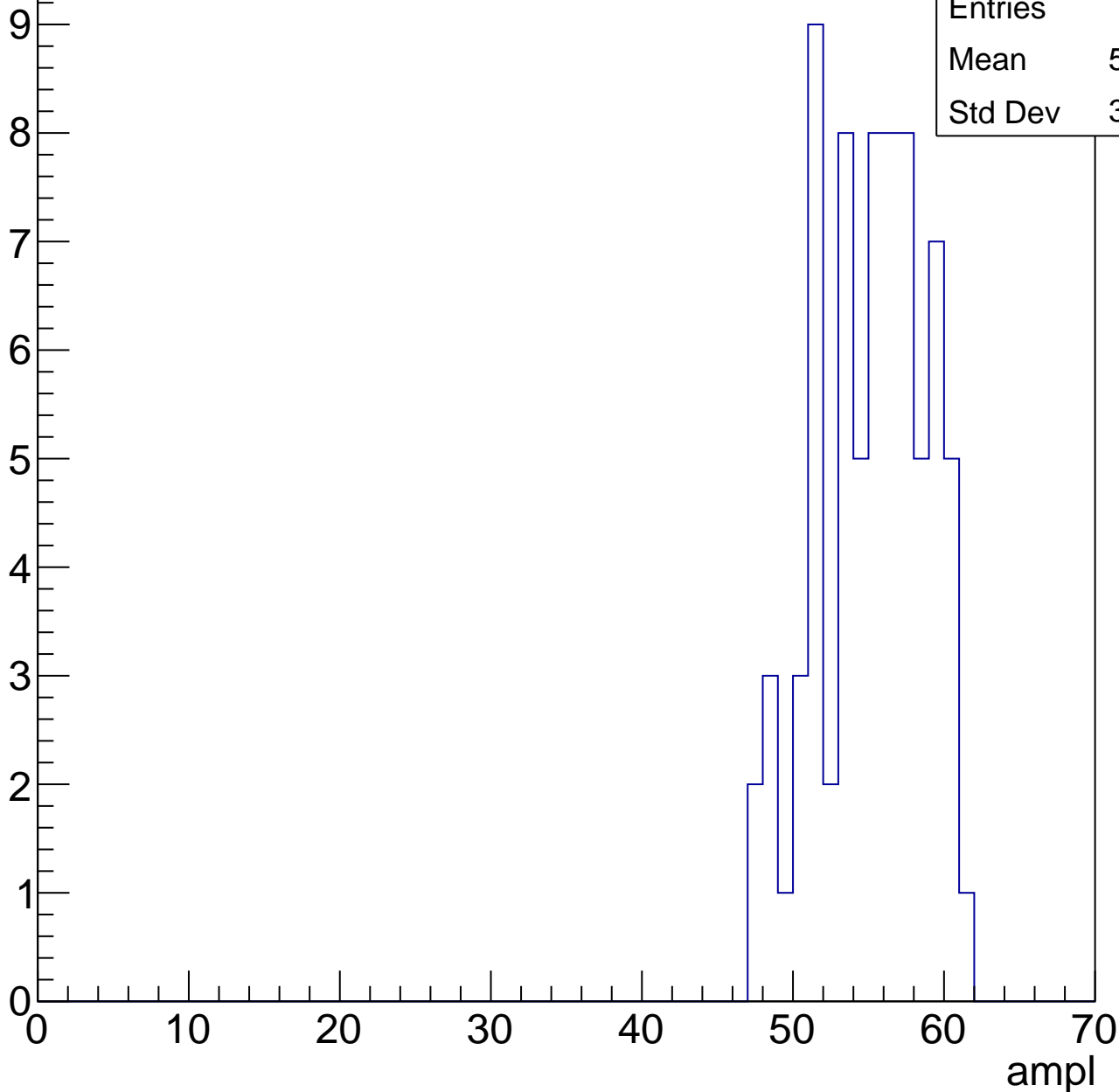


# B1L102S, U12-ch84, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	75
Mean	54.69
Std Dev	3.533

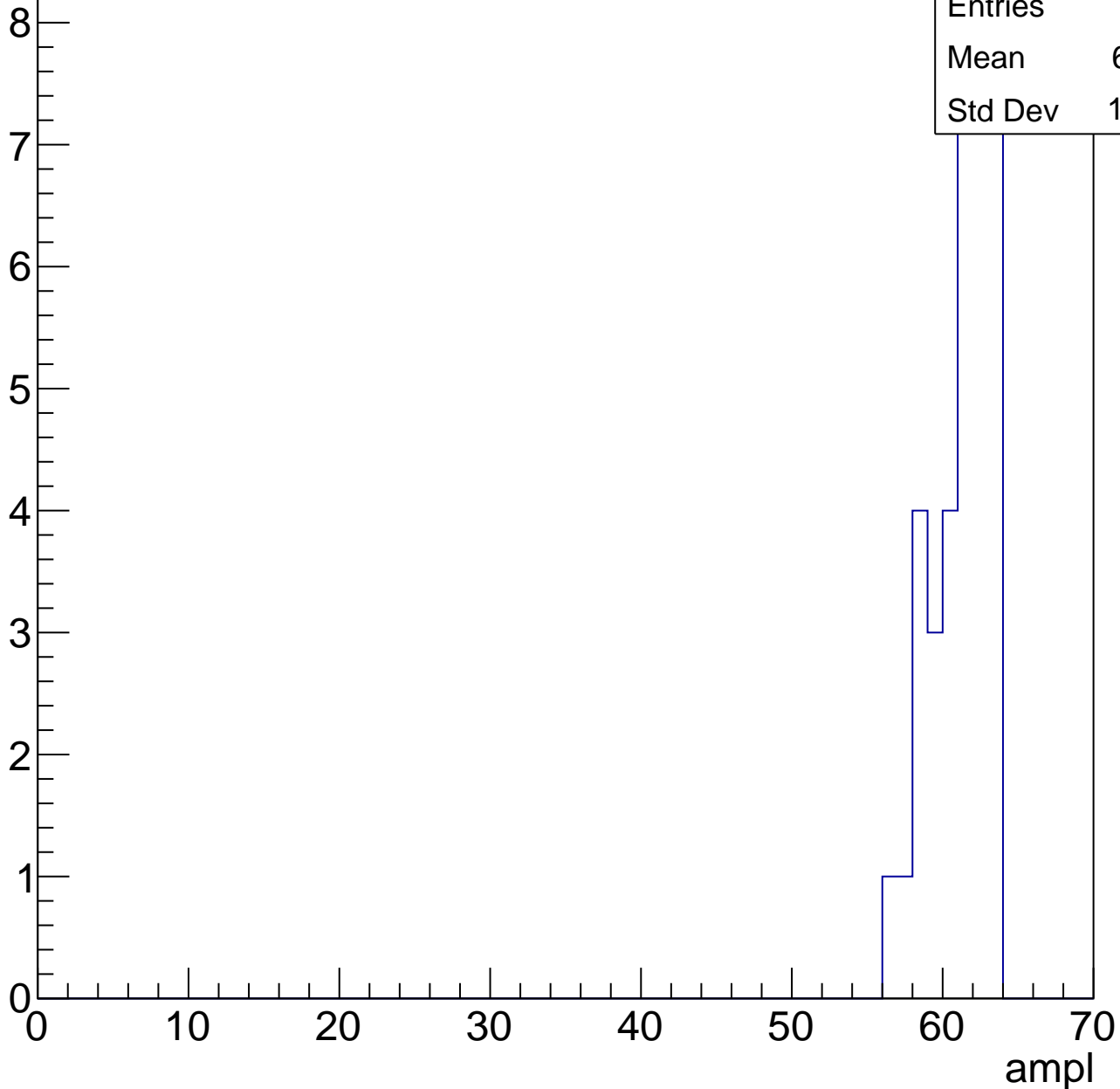


# B1L102S, U12-ch84, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

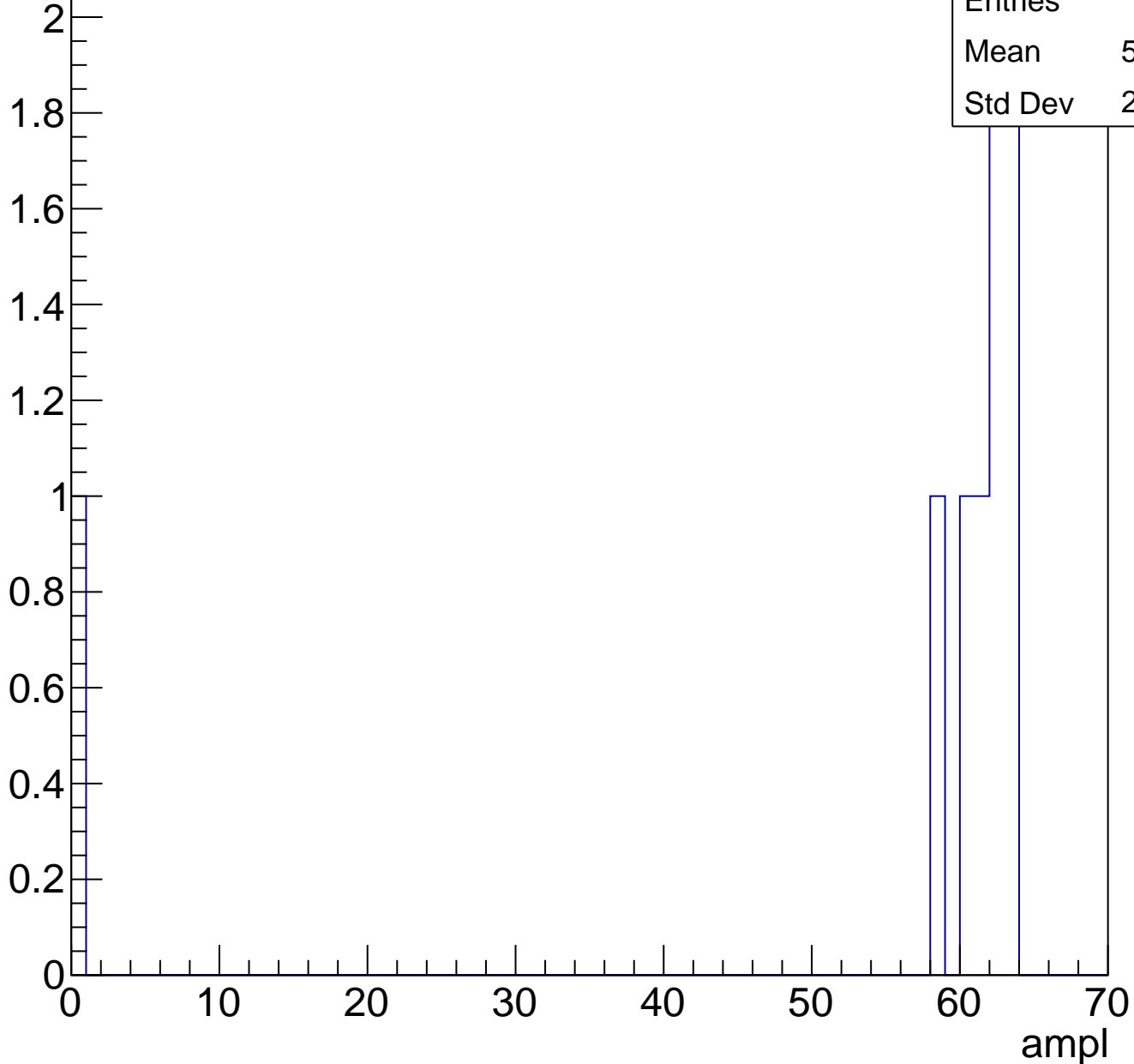
Entries	37
Mean	60.81
Std Dev	1.886



# B1L102S, U12-ch84, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U12-ch84, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U12-ch85, adc0

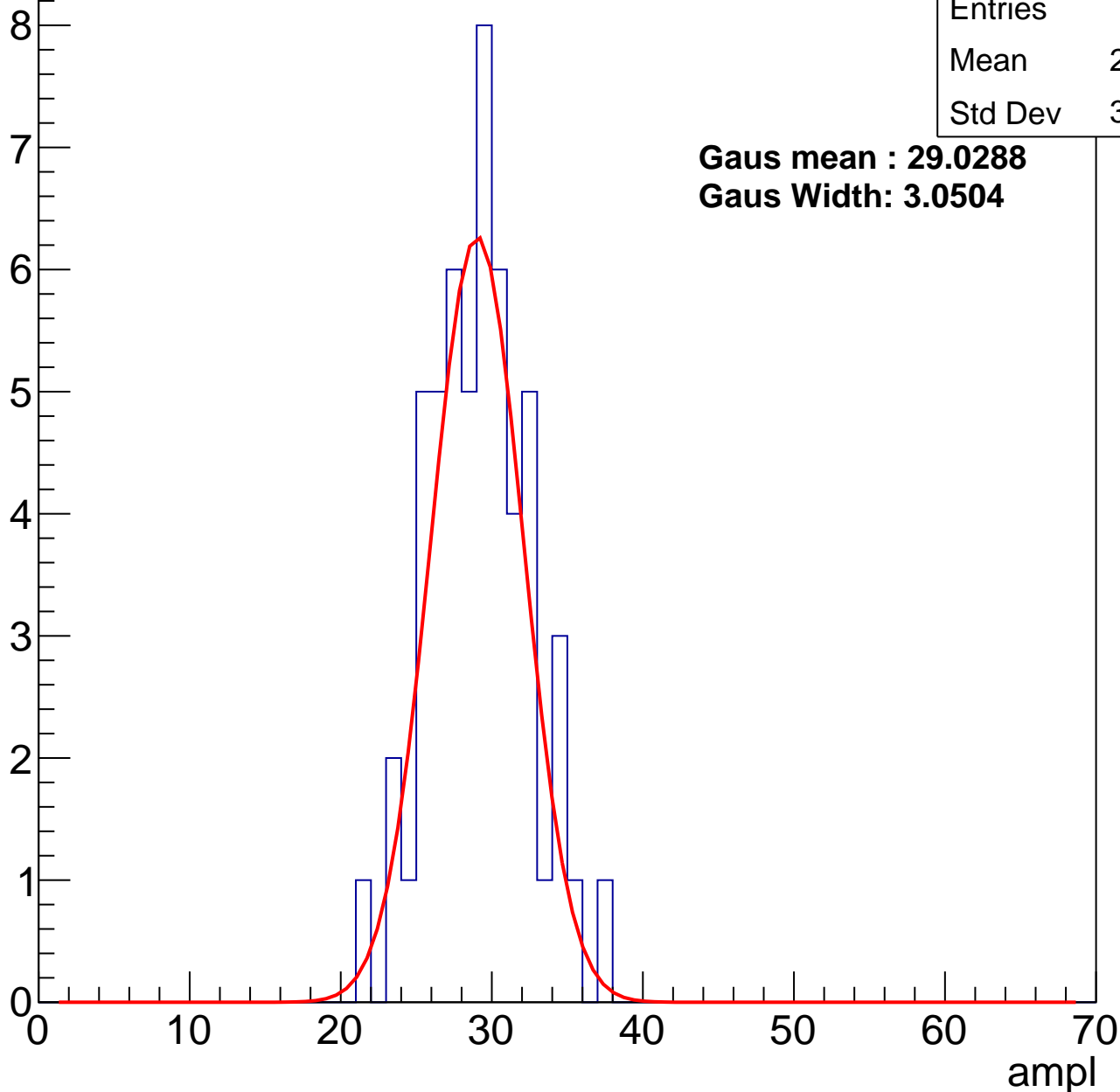
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	54
Mean	28.72
Std Dev	3.246

**Gaus mean : 29.0288**

**Gaus Width: 3.0504**



# B1L102S, U12-ch85, adc1

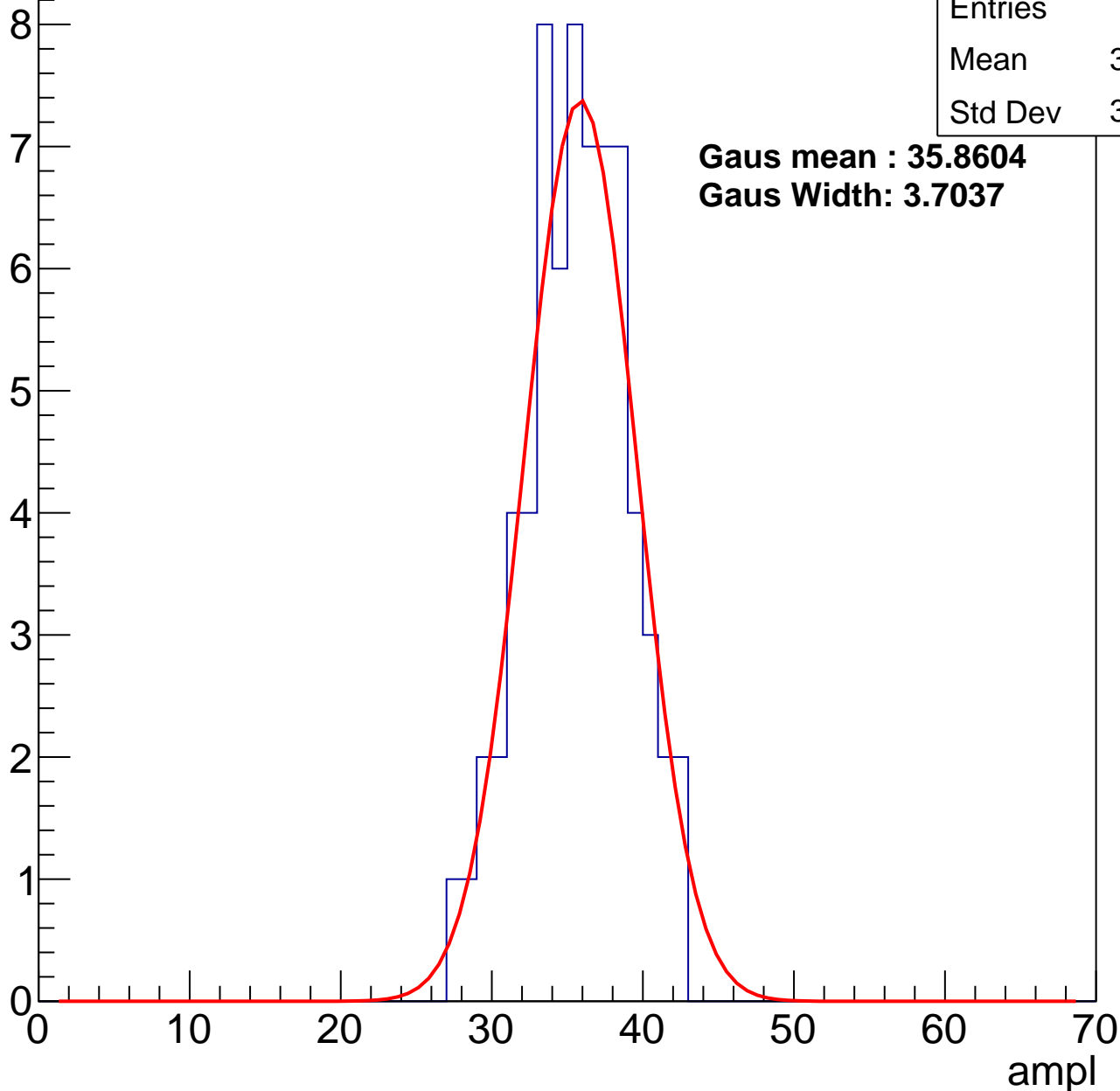
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	35.18
Std Dev	3.382

**Gaus mean : 35.8604**

**Gaus Width: 3.7037**



# B1L102S, U12-ch85, adc2

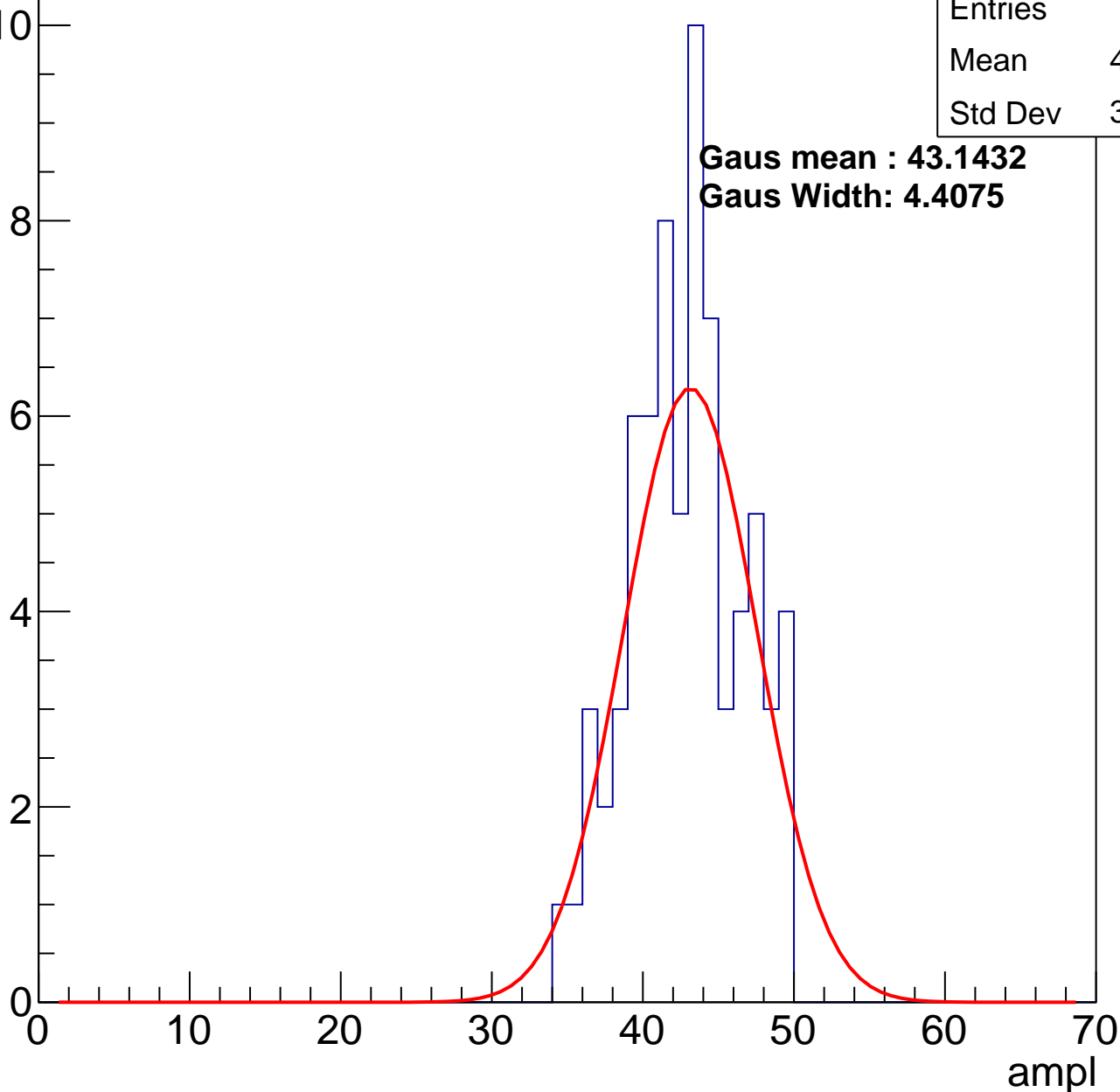
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	71
Mean	42.38
Std Dev	3.663

**Gaus mean : 43.1432**

**Gaus Width: 4.4075**

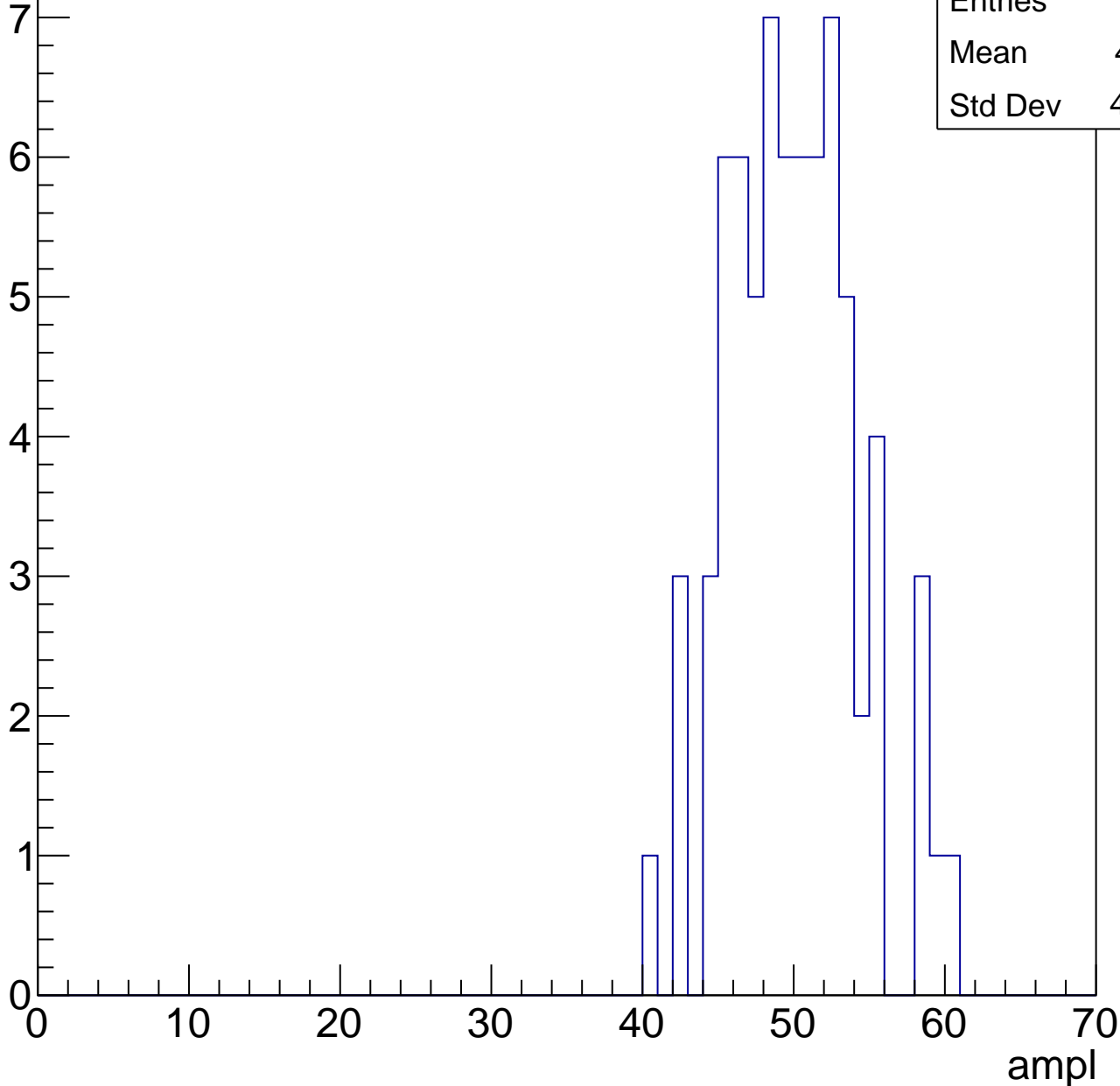


# B1L102S, U12-ch85, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	72
Mean	49.51
Std Dev	4.236

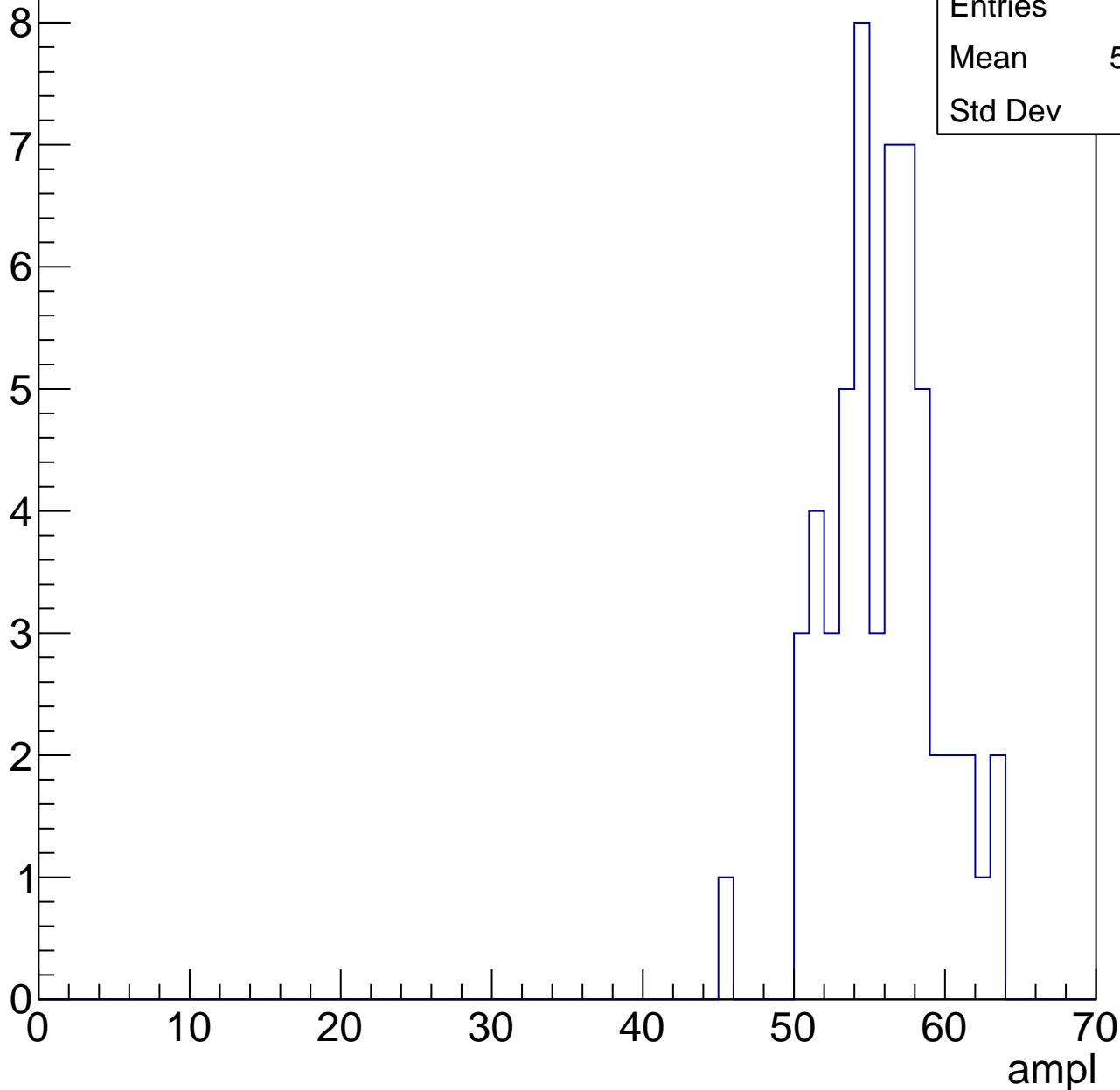


# B1L102S, U12-ch85, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	55
Mean	55.38
Std Dev	3.56

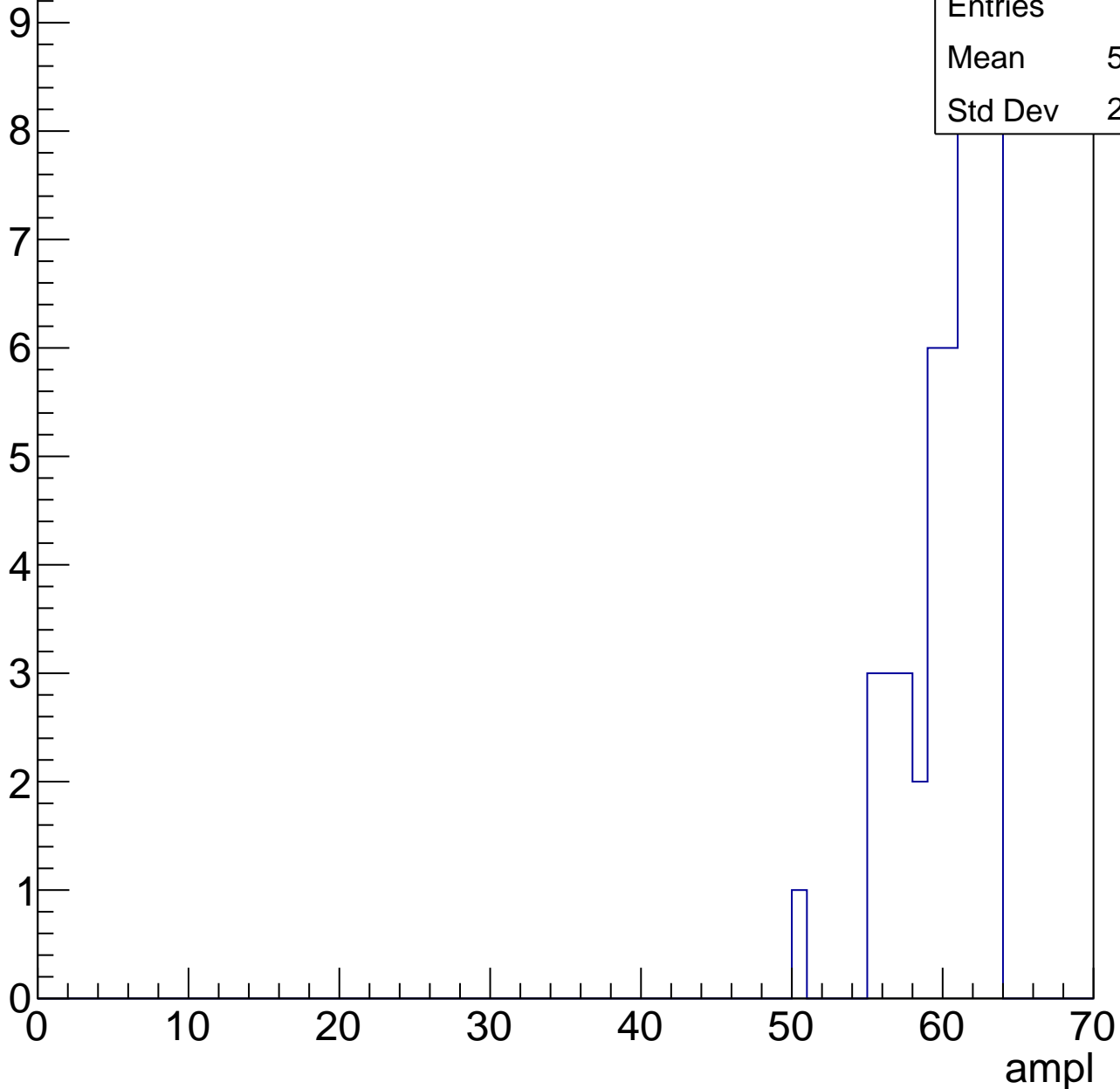


# B1L102S, U12-ch85, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

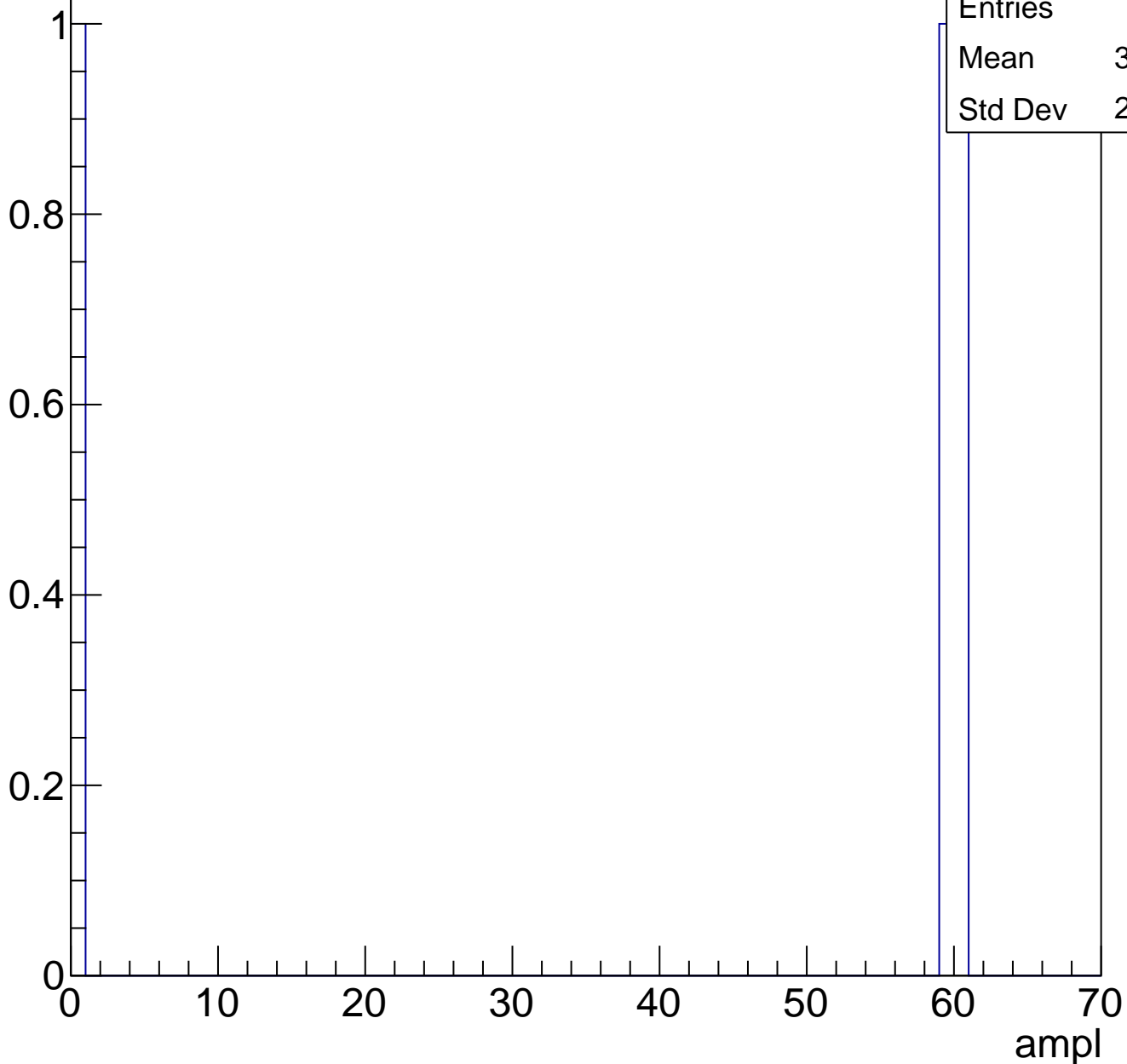
Entries	49
Mean	59.88
Std Dev	2.782



# B1L102S, U12-ch85, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U12-ch85, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L102S, U12-ch86, adc0

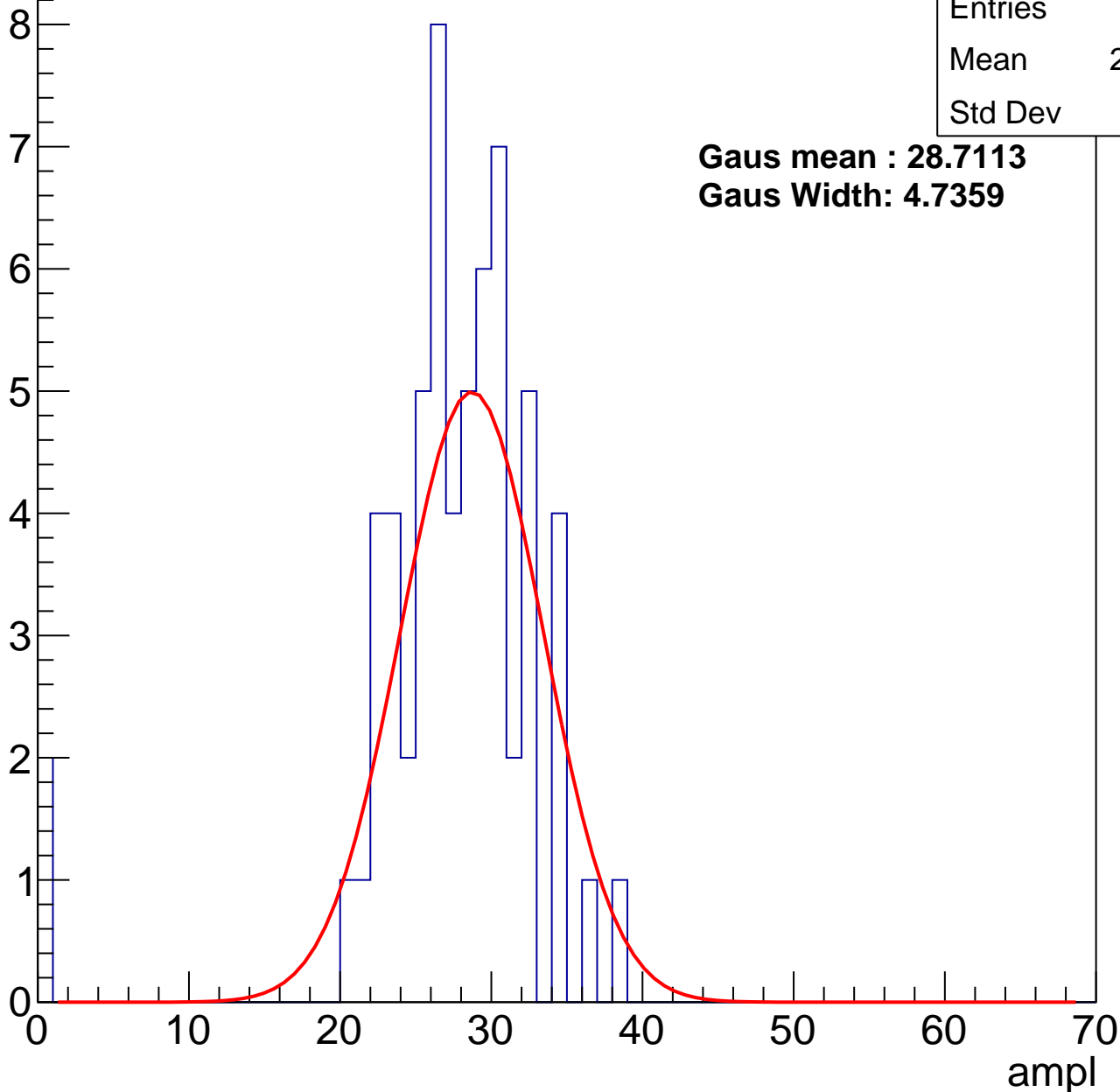
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	62
Mean	26.87
Std Dev	6.22

**Gaus mean : 28.7113**

**Gaus Width: 4.7359**



# B1L102S, U12-ch86, adc1

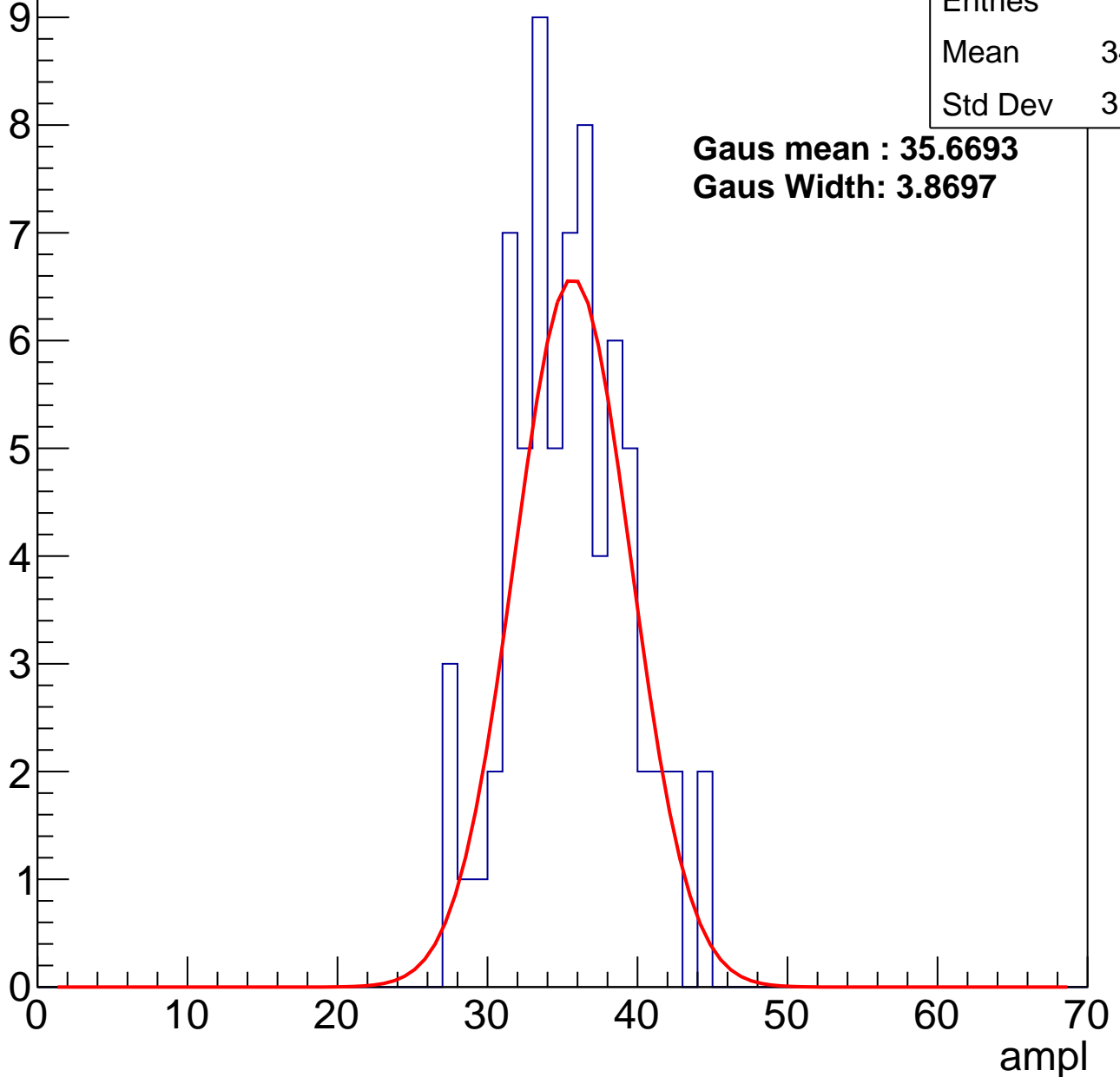
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	71
Mean	34.93
Std Dev	3.872

**Gaus mean : 35.6693**

**Gaus Width: 3.8697**



# B1L102S, U12-ch86, adc2

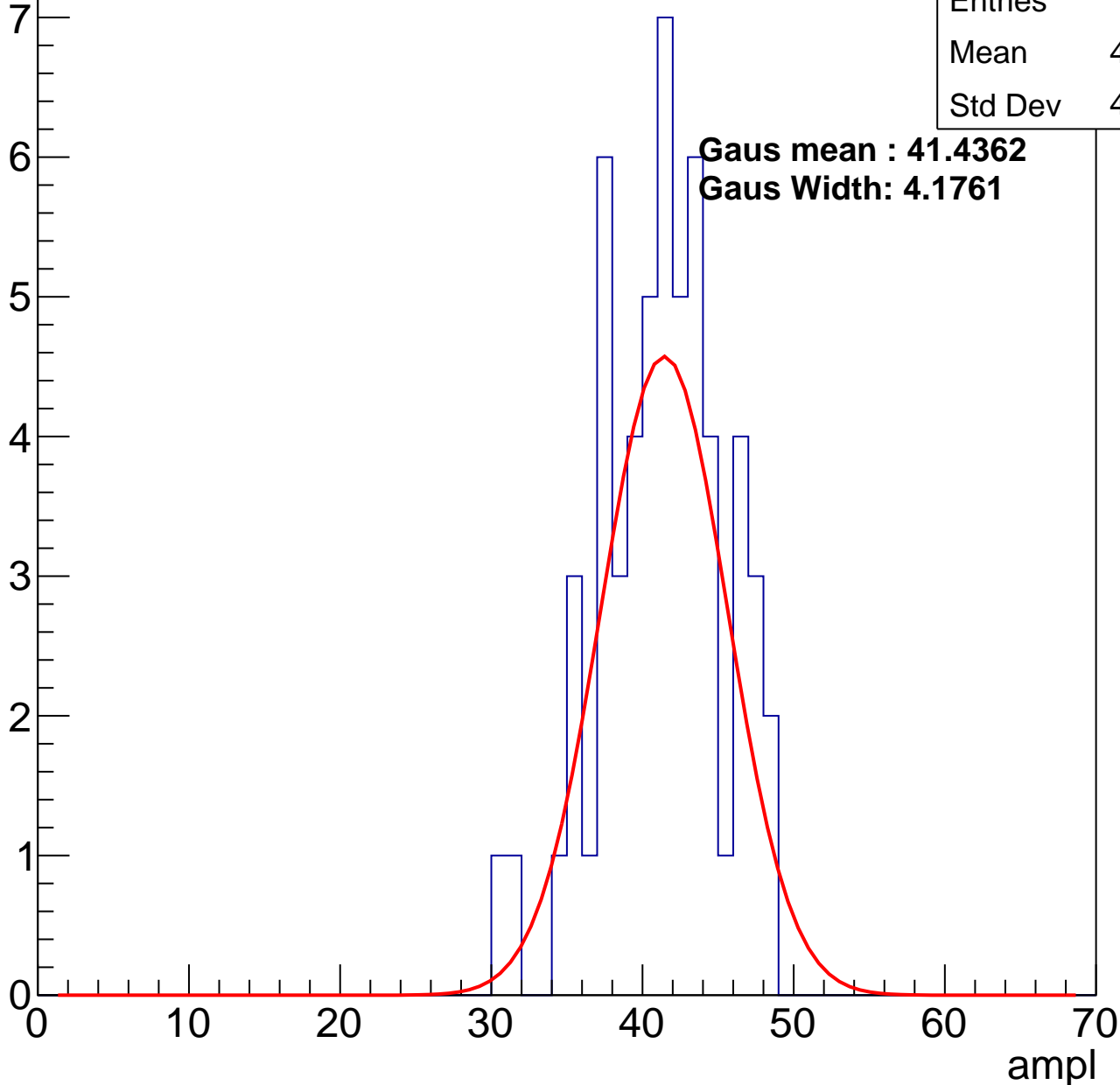
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	57
Mean	40.79
Std Dev	4.042

**Gaus mean : 41.4362**

**Gaus Width: 4.1761**



# B1L102S, U12-ch86, adc3

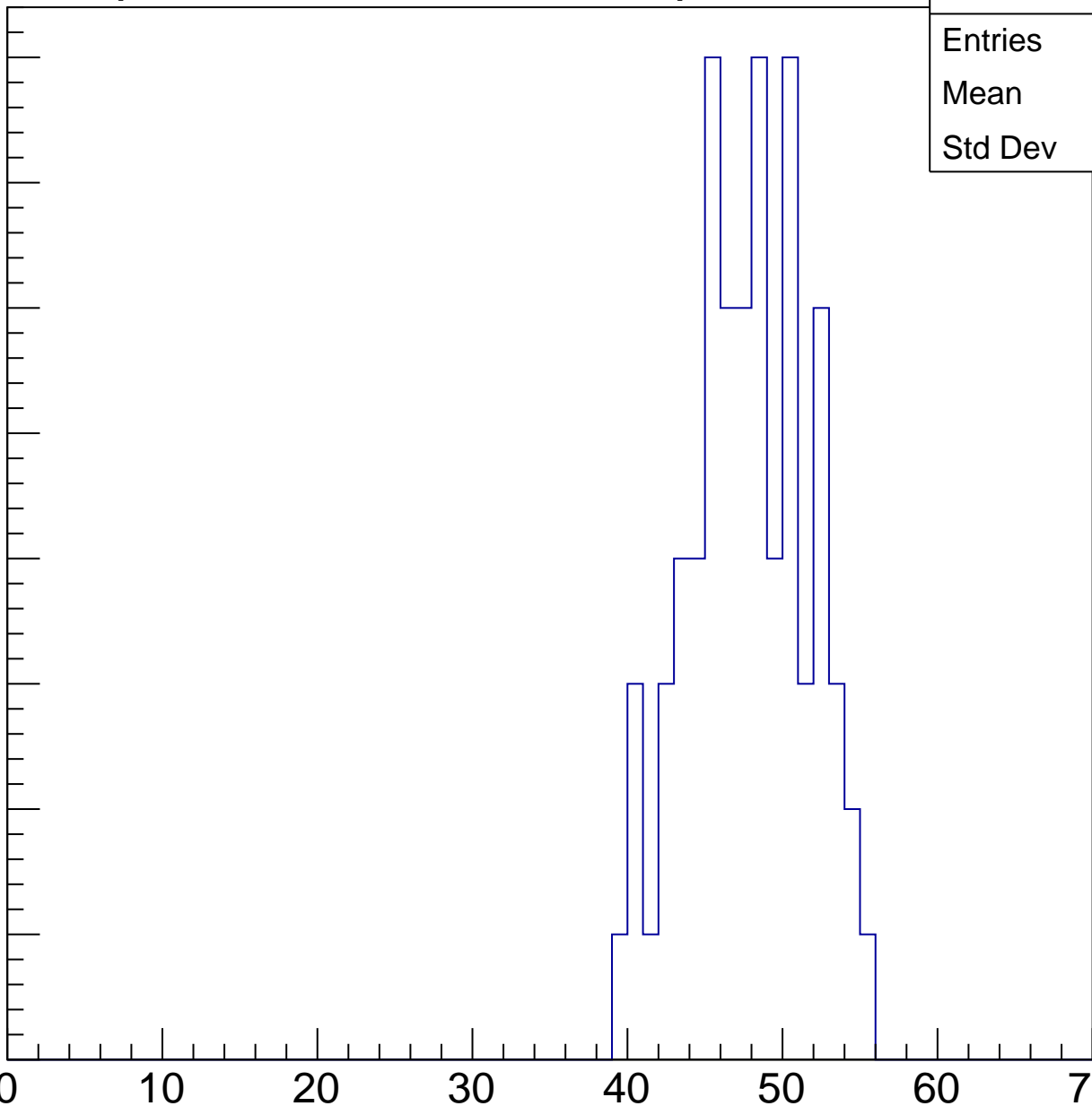
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	71
Mean	47.31
Std Dev	3.785

ampl

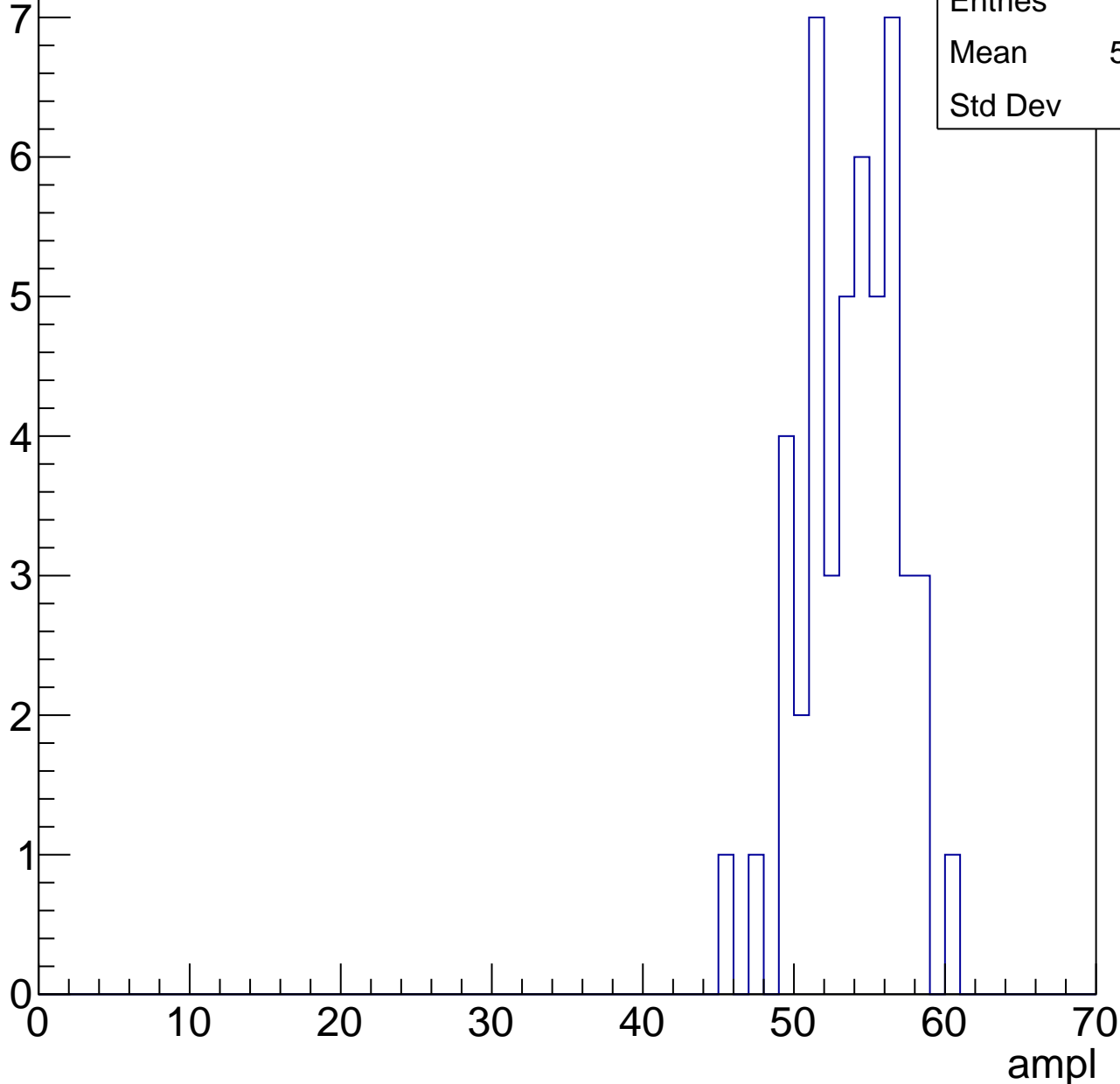


# B1L102S, U12-ch86, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	48
Mean	53.38
Std Dev	3.12



# B1L102S, U12-ch86, adc5

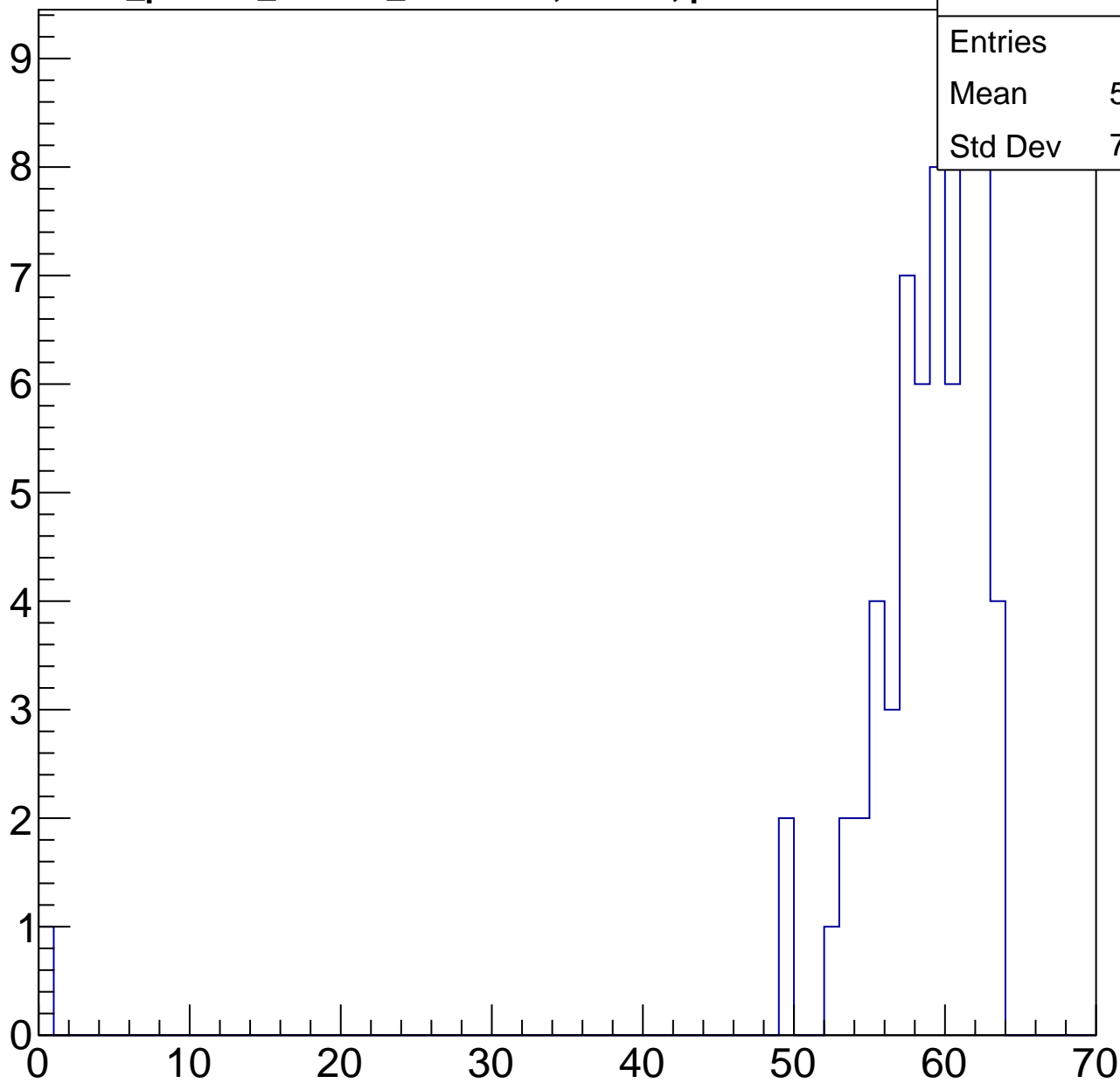
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	63
Mean	57.59
Std Dev	7.997

ampl

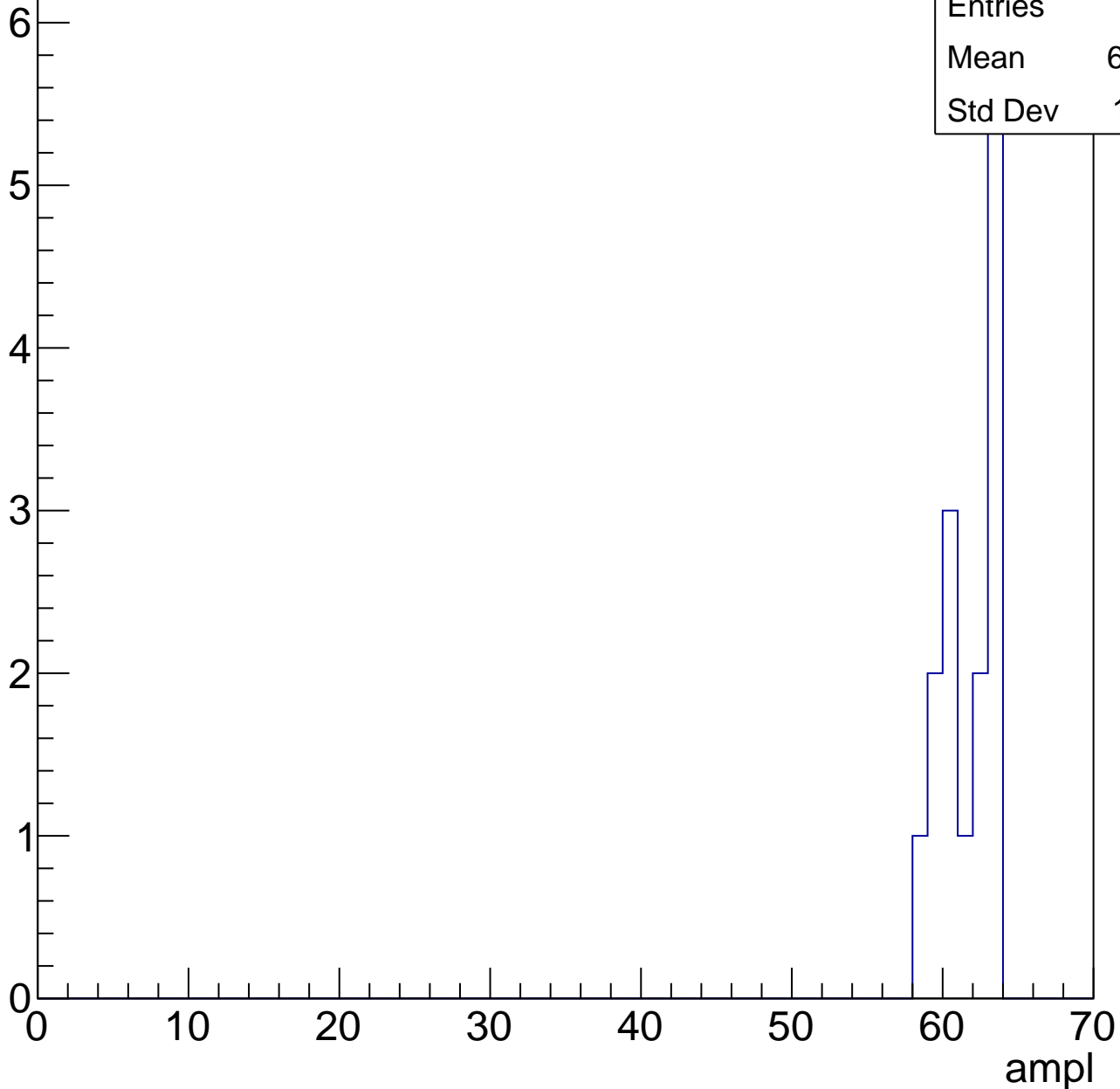


# B1L102S, U12-ch86, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	15
Mean	61.27
Std Dev	1.731





# B1L102S, U12-ch86, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U12-ch87, adc0

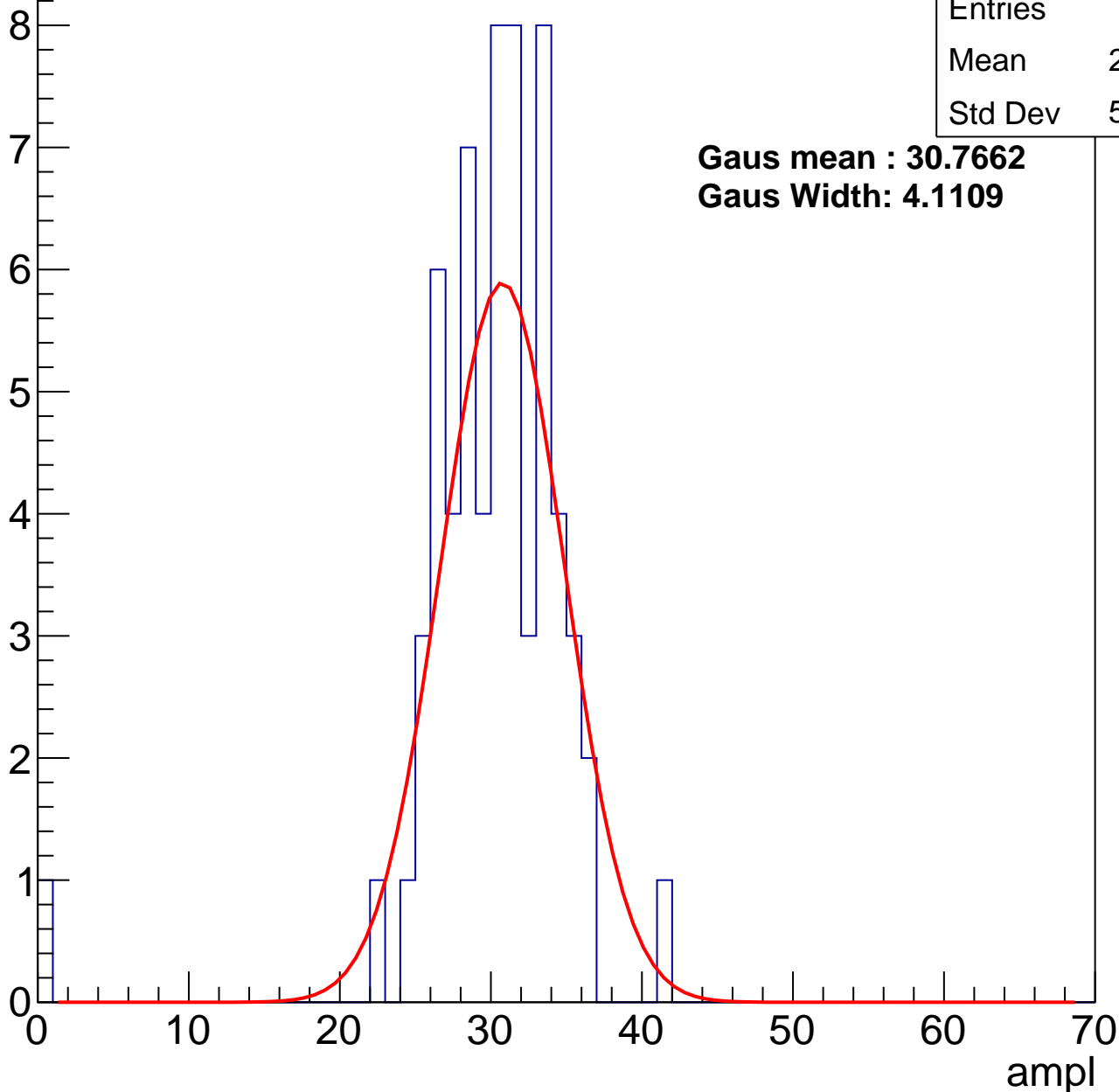
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	29.67
Std Dev	5.087

**Gaus mean : 30.7662**

**Gaus Width: 4.1109**



# B1L102S, U12-ch87, adc1

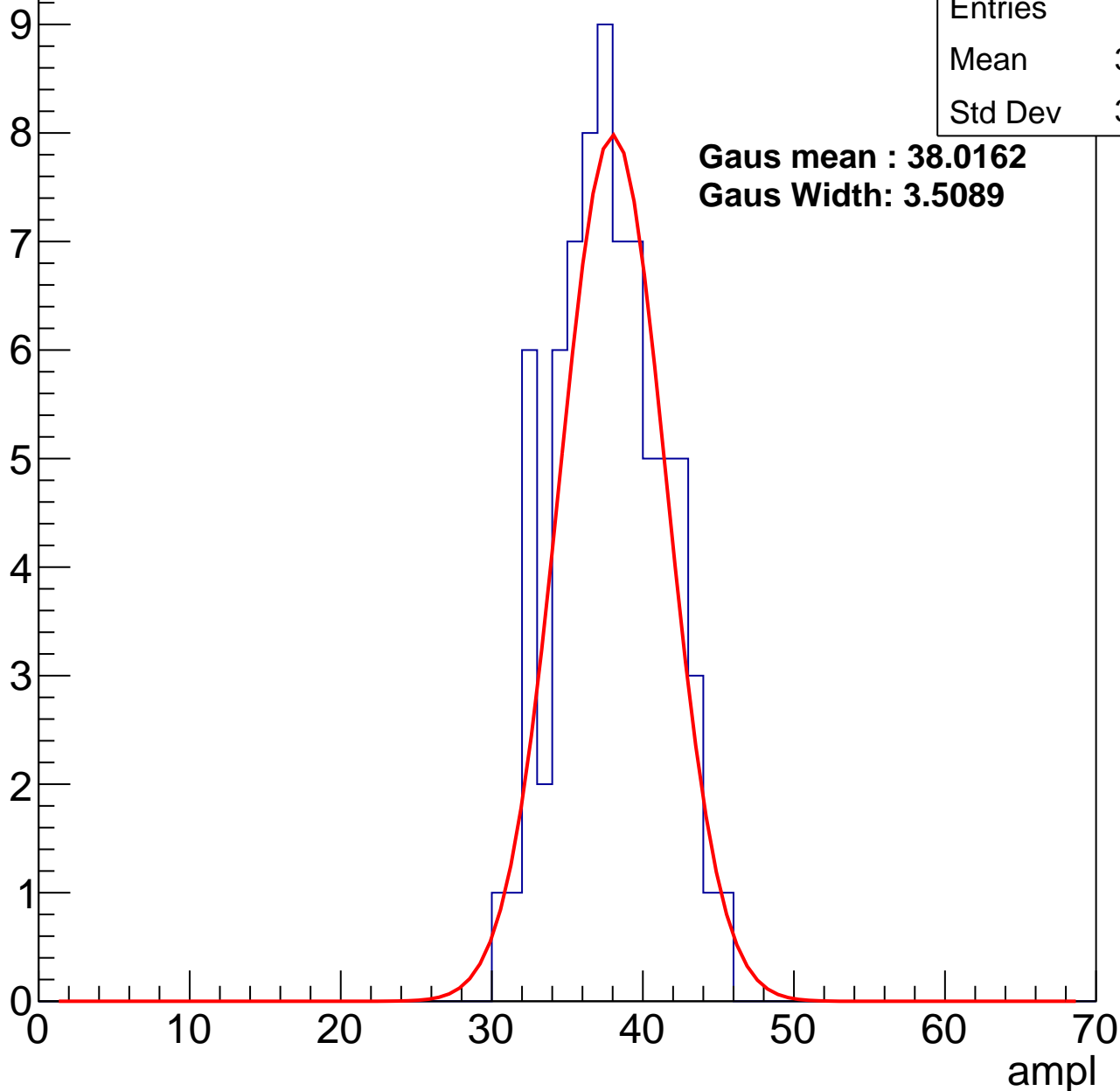
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	74
Mean	37.31
Std Dev	3.401

**Gaus mean : 38.0162**

**Gaus Width: 3.5089**



# B1L102S, U12-ch87, adc2

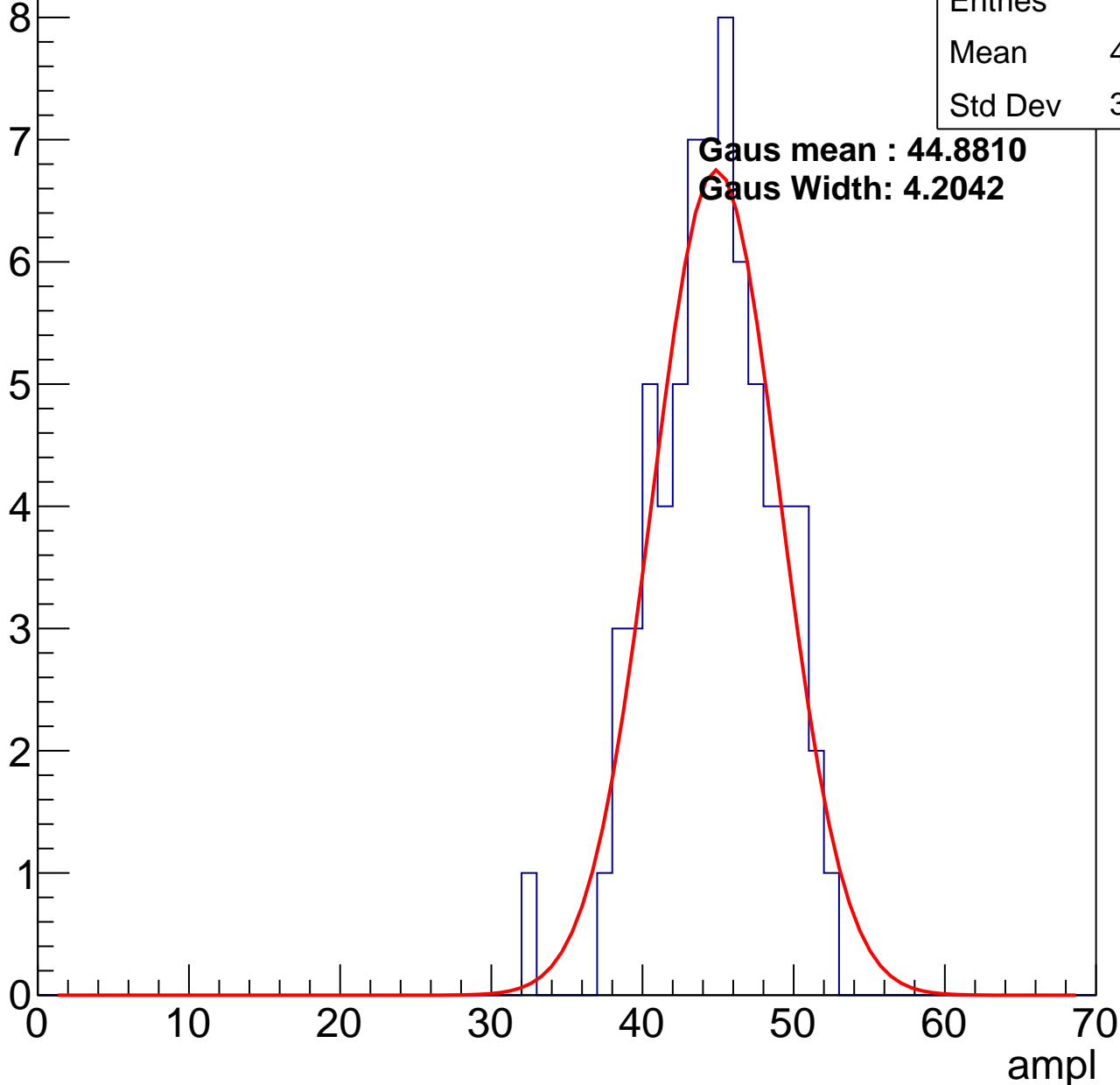
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	70
Mean	44.23
Std Dev	3.896

**Gaus mean : 44.8810**

**Gaus Width: 4.2042**

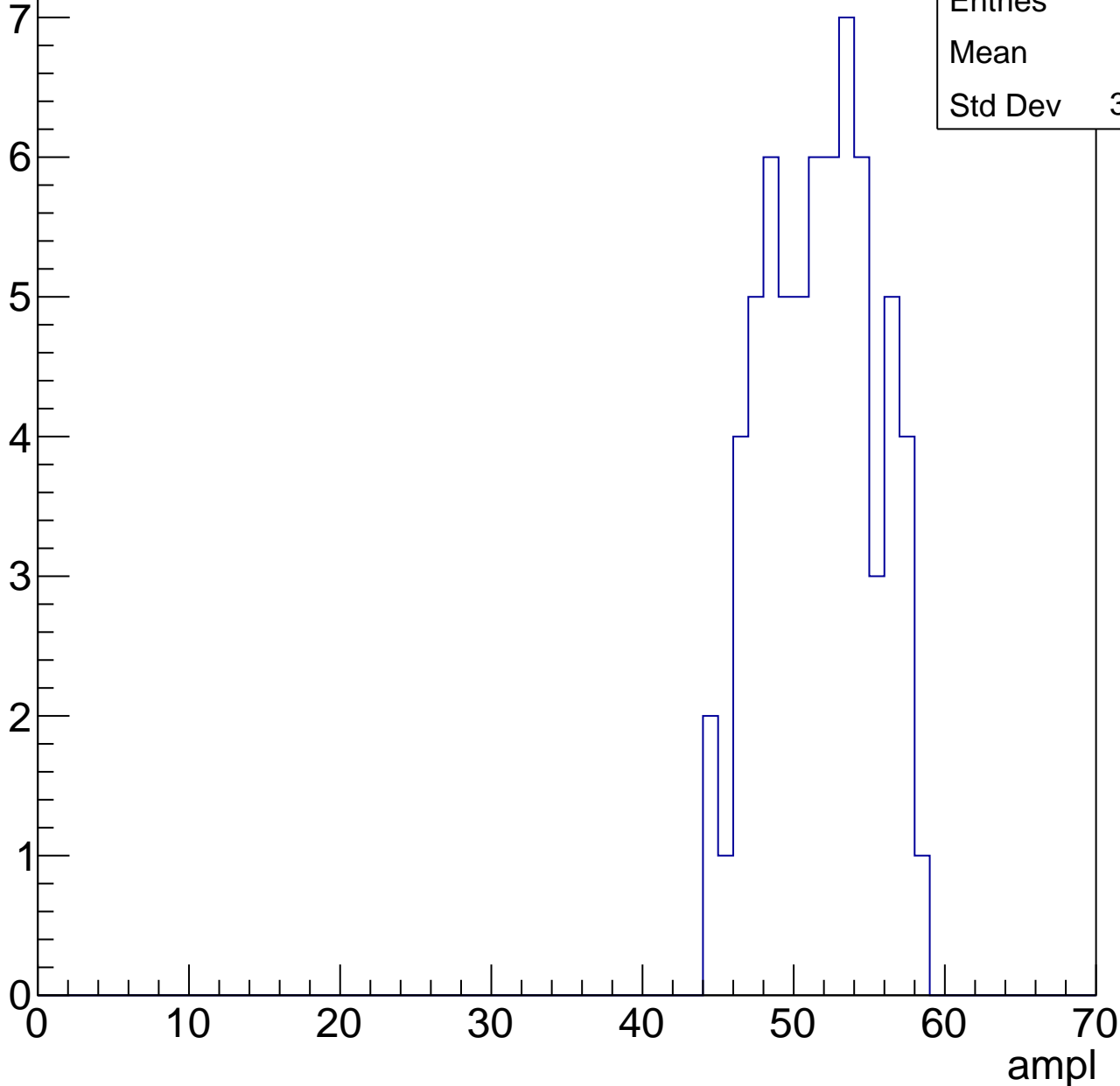


# B1L102S, U12-ch87, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	51.2
Std Dev	3.577

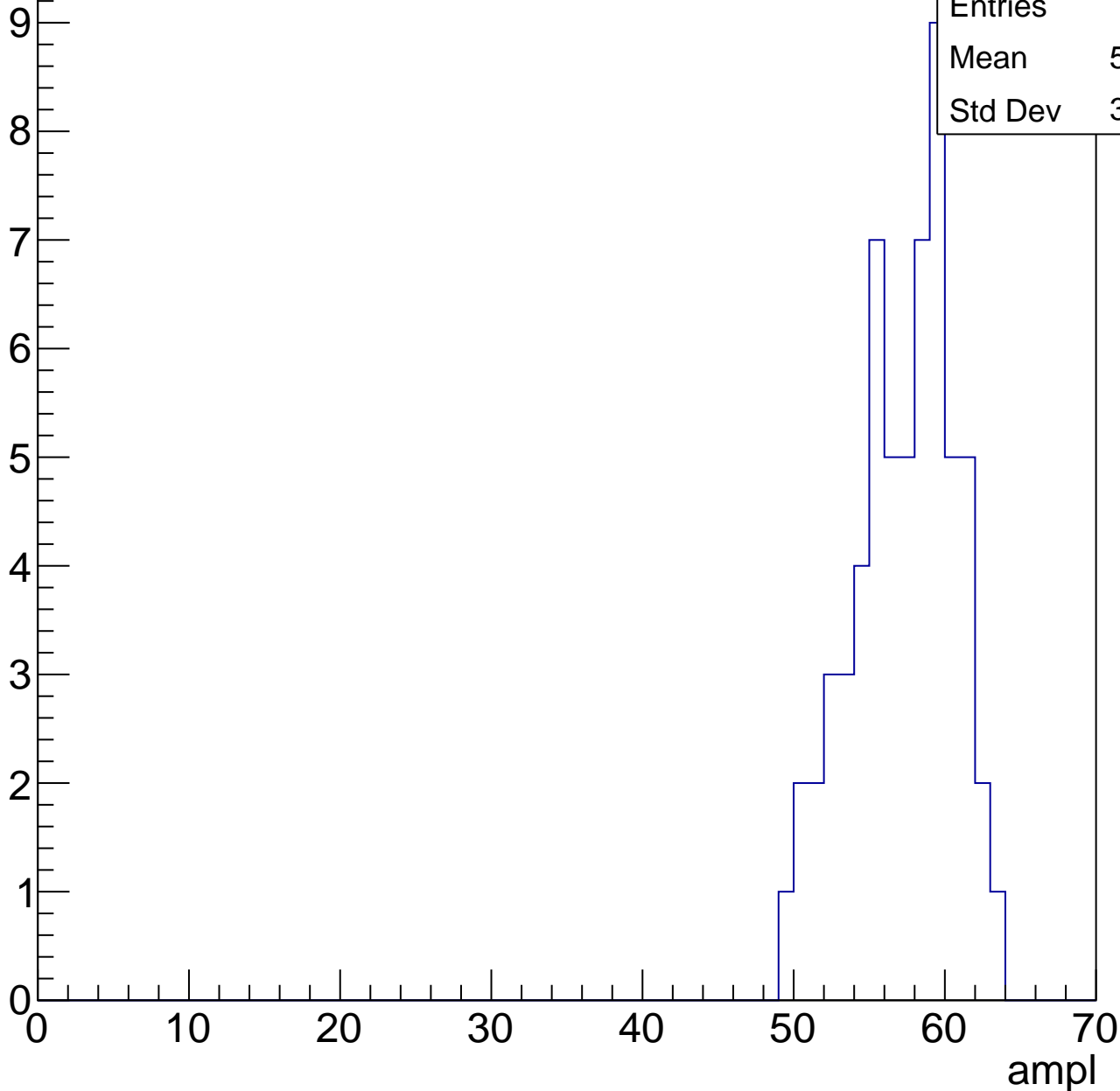


# B1L102S, U12-ch87, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	56.74
Std Dev	3.328

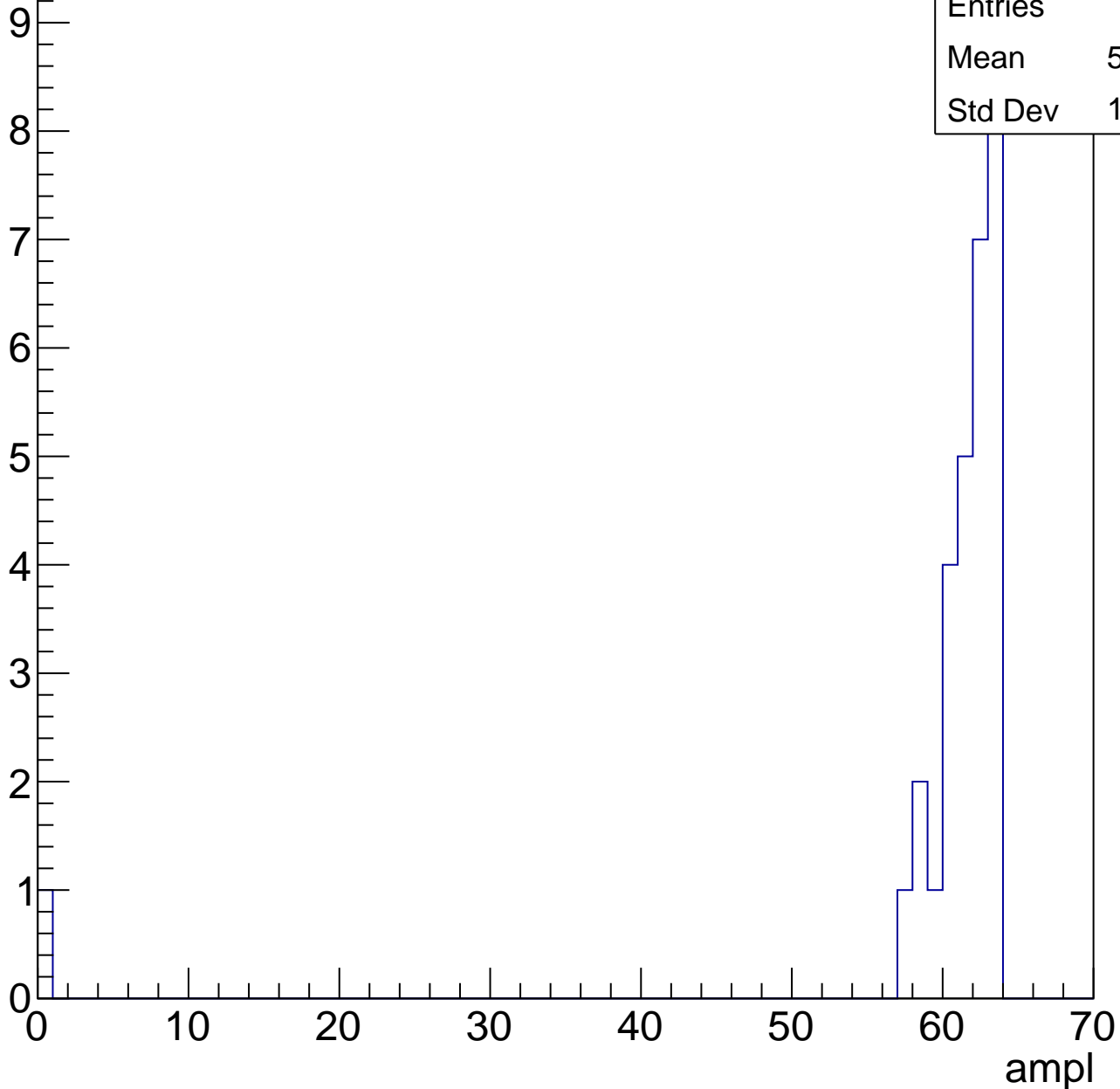


# B1L102S, U12-ch87, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

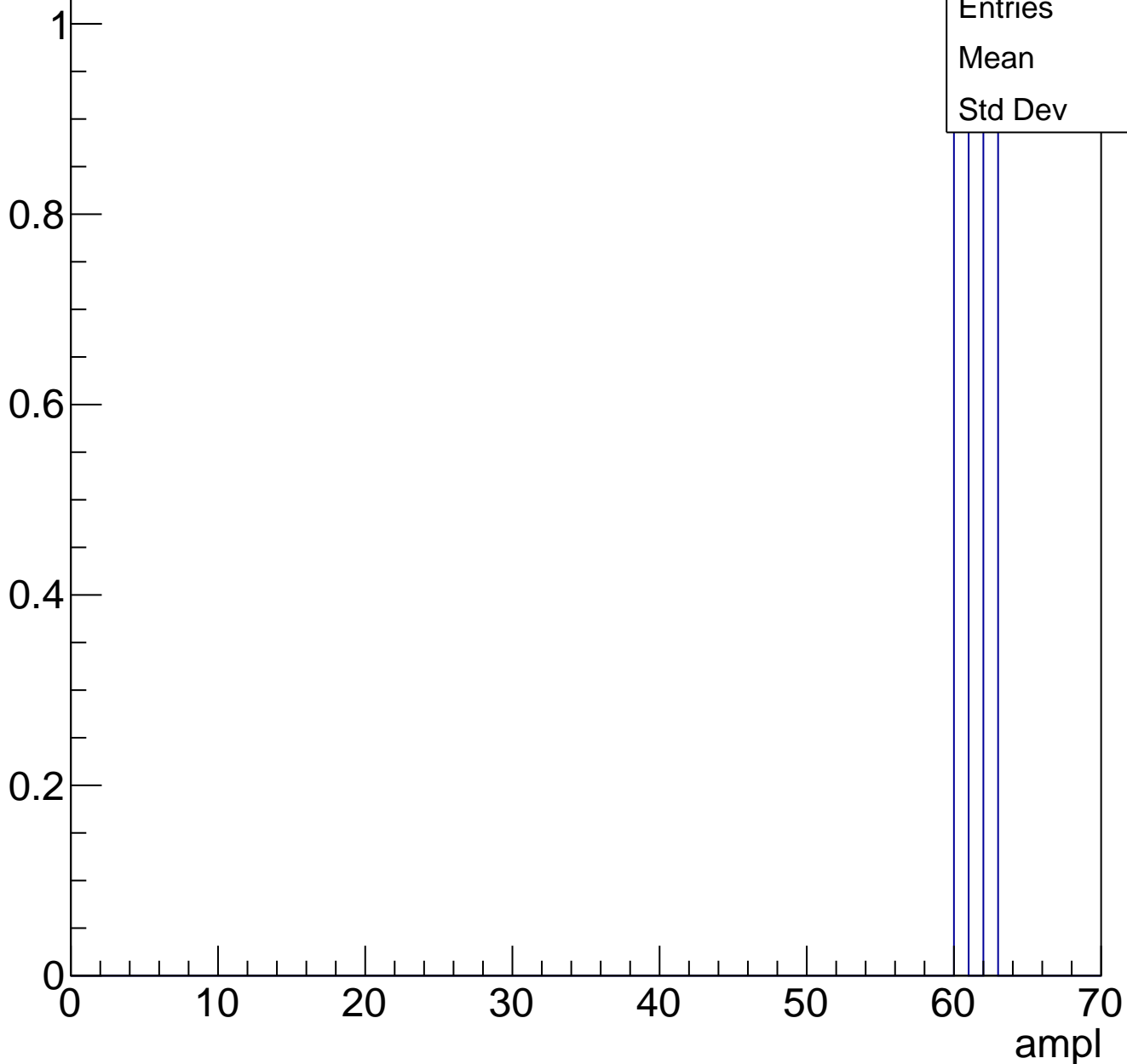
Entries	30
Mean	59.27
Std Dev	11.13



# B1L102S, U12-ch87, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U12-ch87, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U12-ch88, adc0

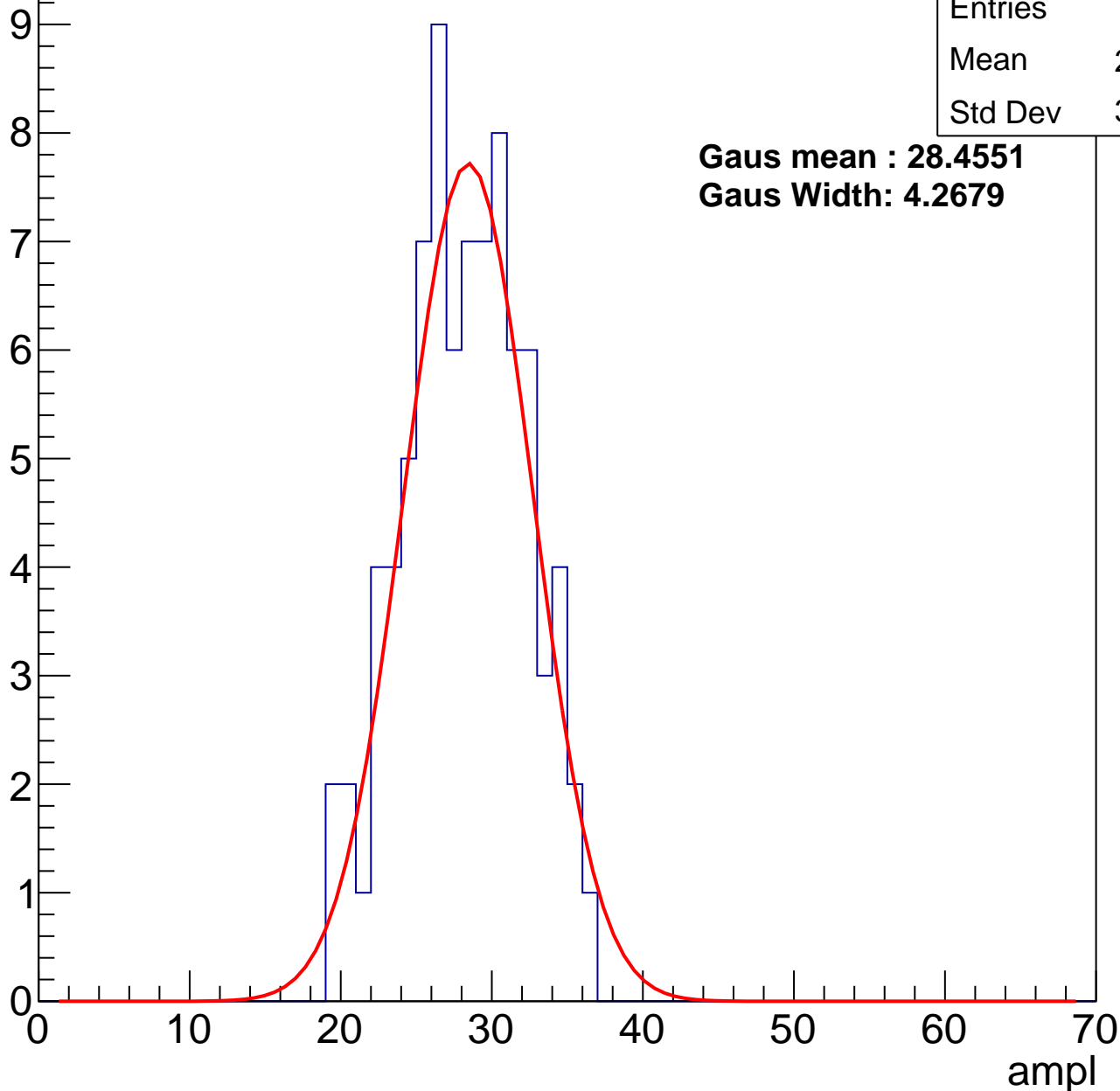
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	84
Mean	27.71
Std Dev	3.981

**Gaus mean : 28.4551**

**Gaus Width: 4.2679**



# B1L102S, U12-ch88, adc1

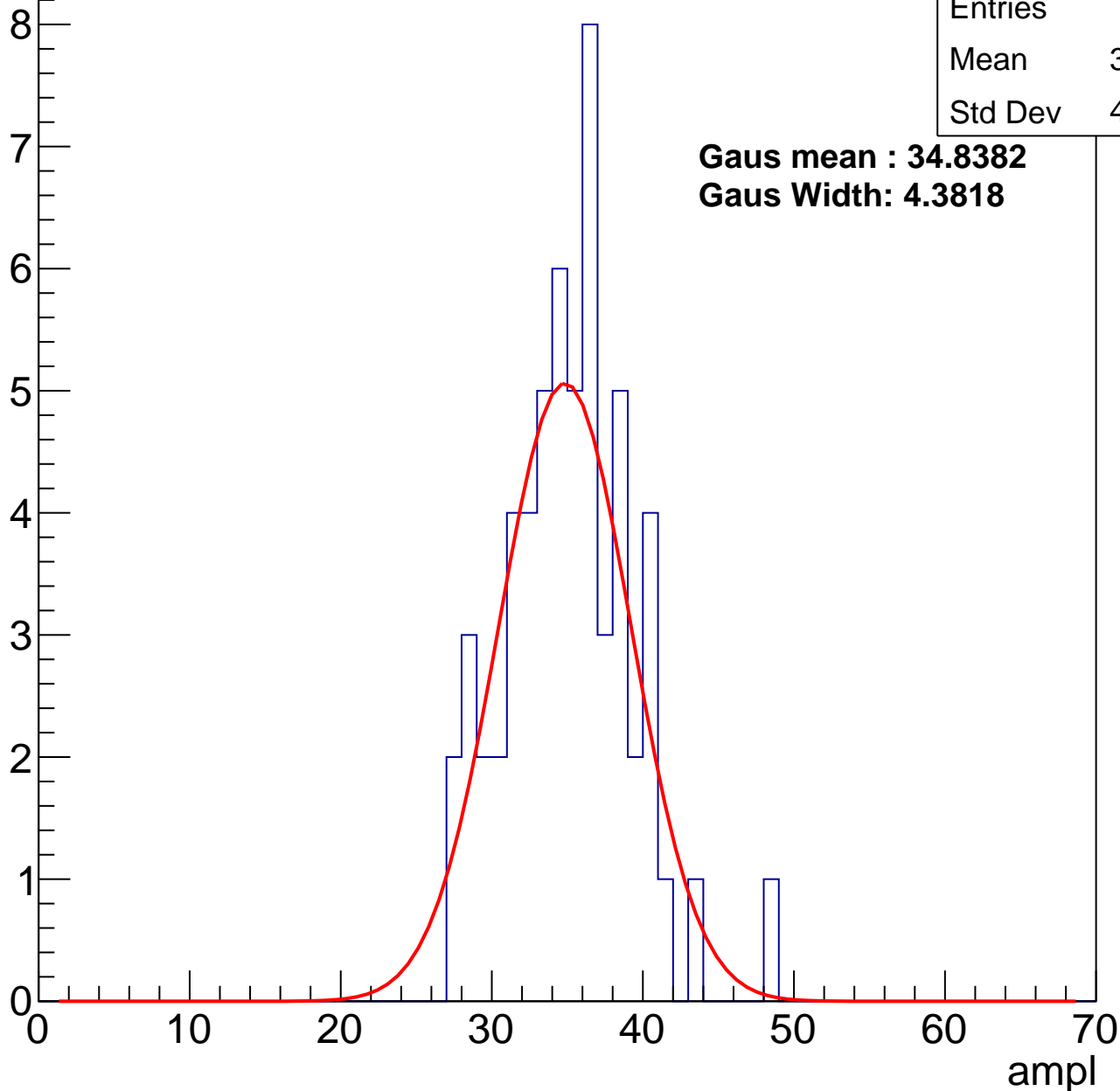
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	58
Mean	34.67
Std Dev	4.116

**Gaus mean : 34.8382**

**Gaus Width: 4.3818**



# B1L102S, U12-ch88, adc2

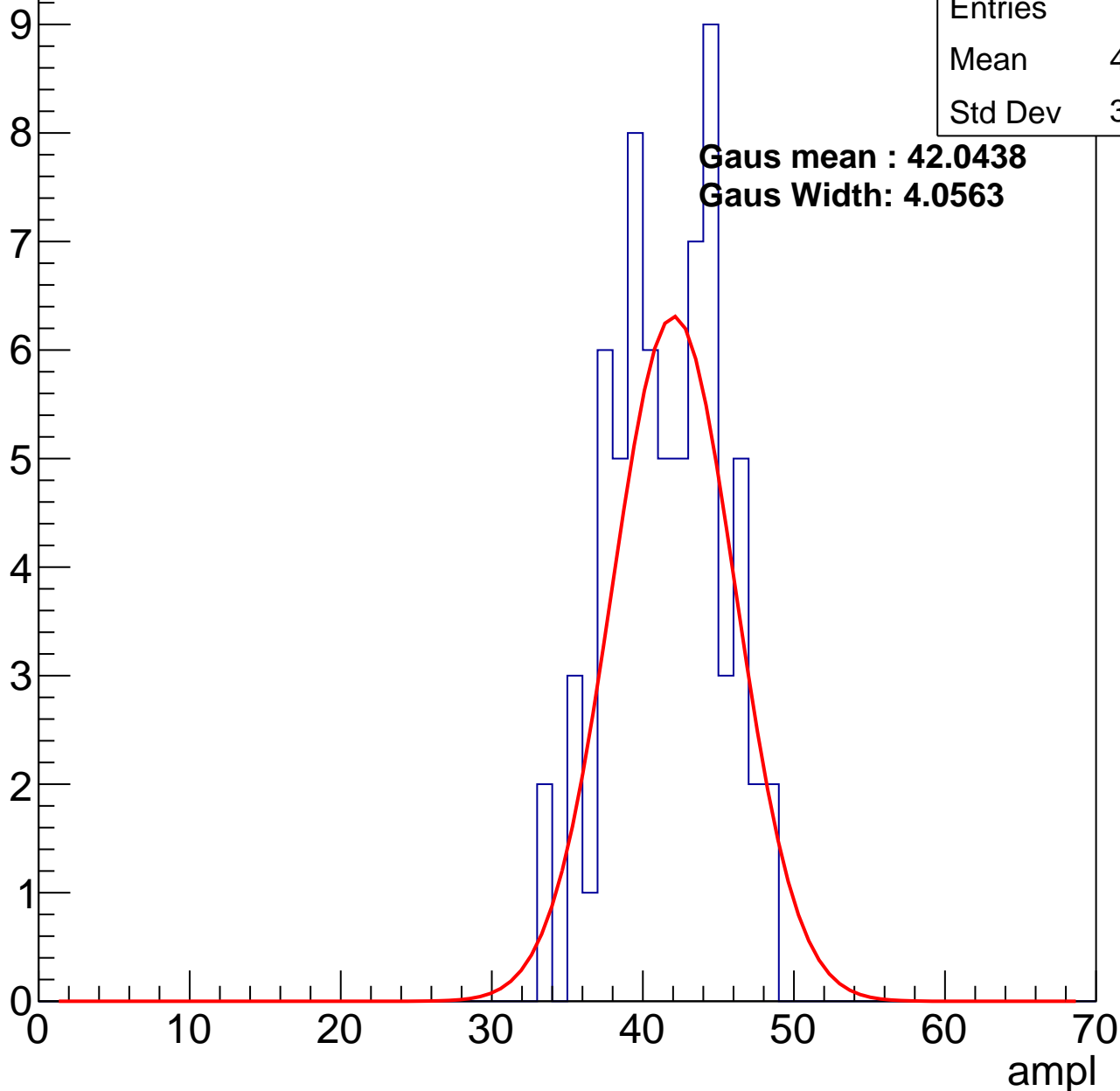
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	41.13
Std Dev	3.603

**Gaus mean : 42.0438**

**Gaus Width: 4.0563**

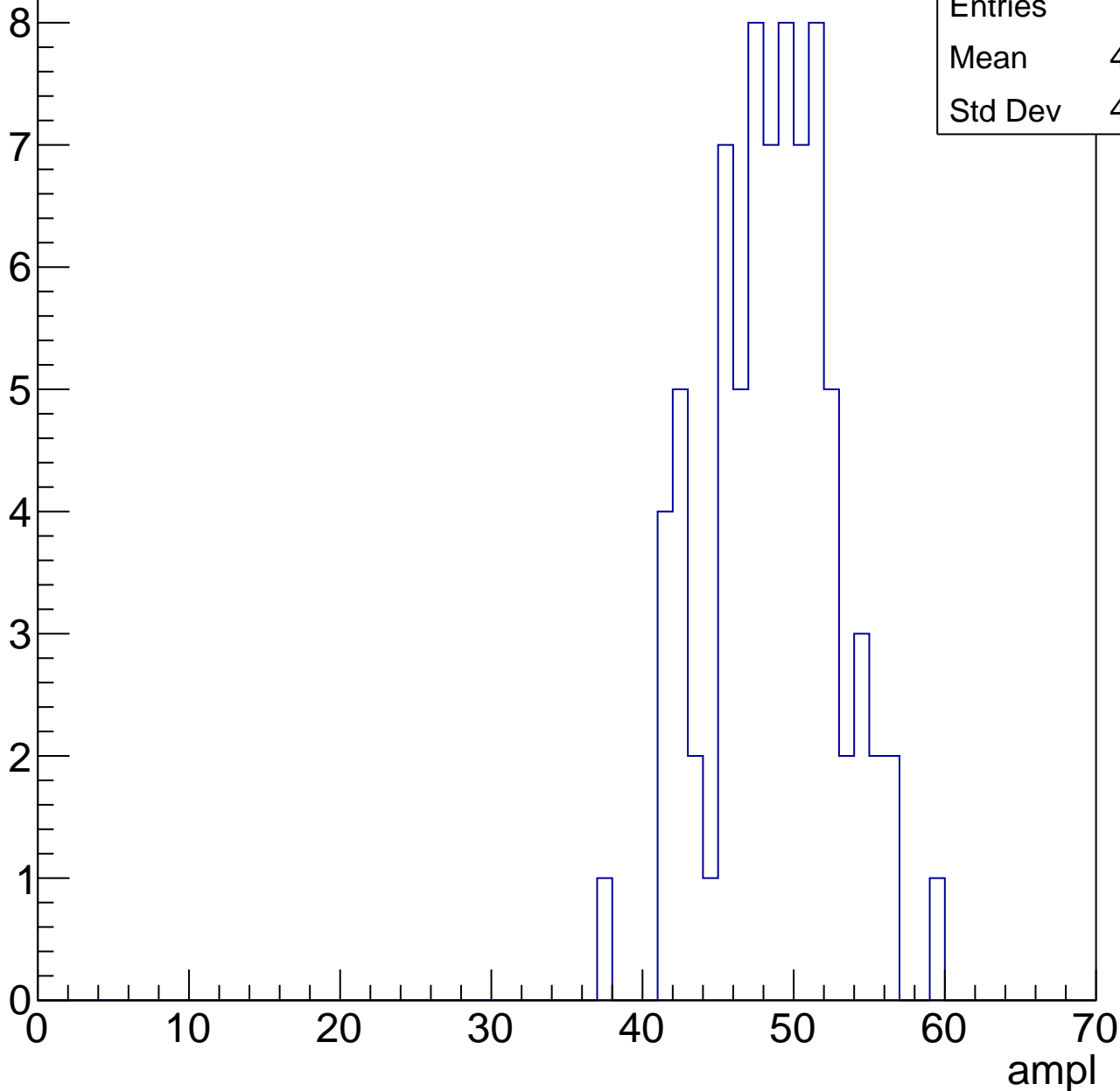


# B1L102S, U12-ch88, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	78
Mean	48.17
Std Dev	4.152

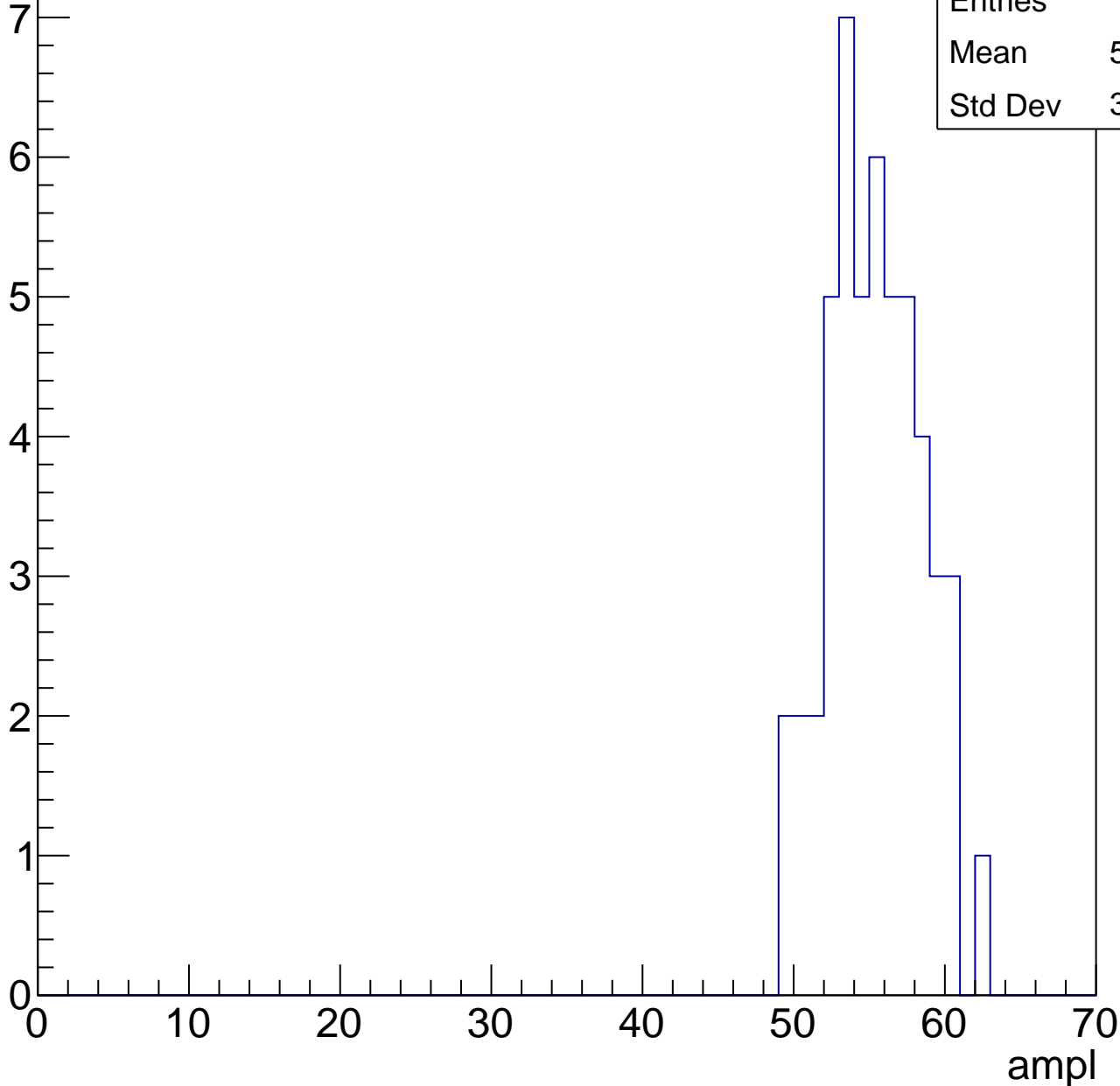


# B1L102S, U12-ch88, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	50
Mean	54.94
Std Dev	3.049

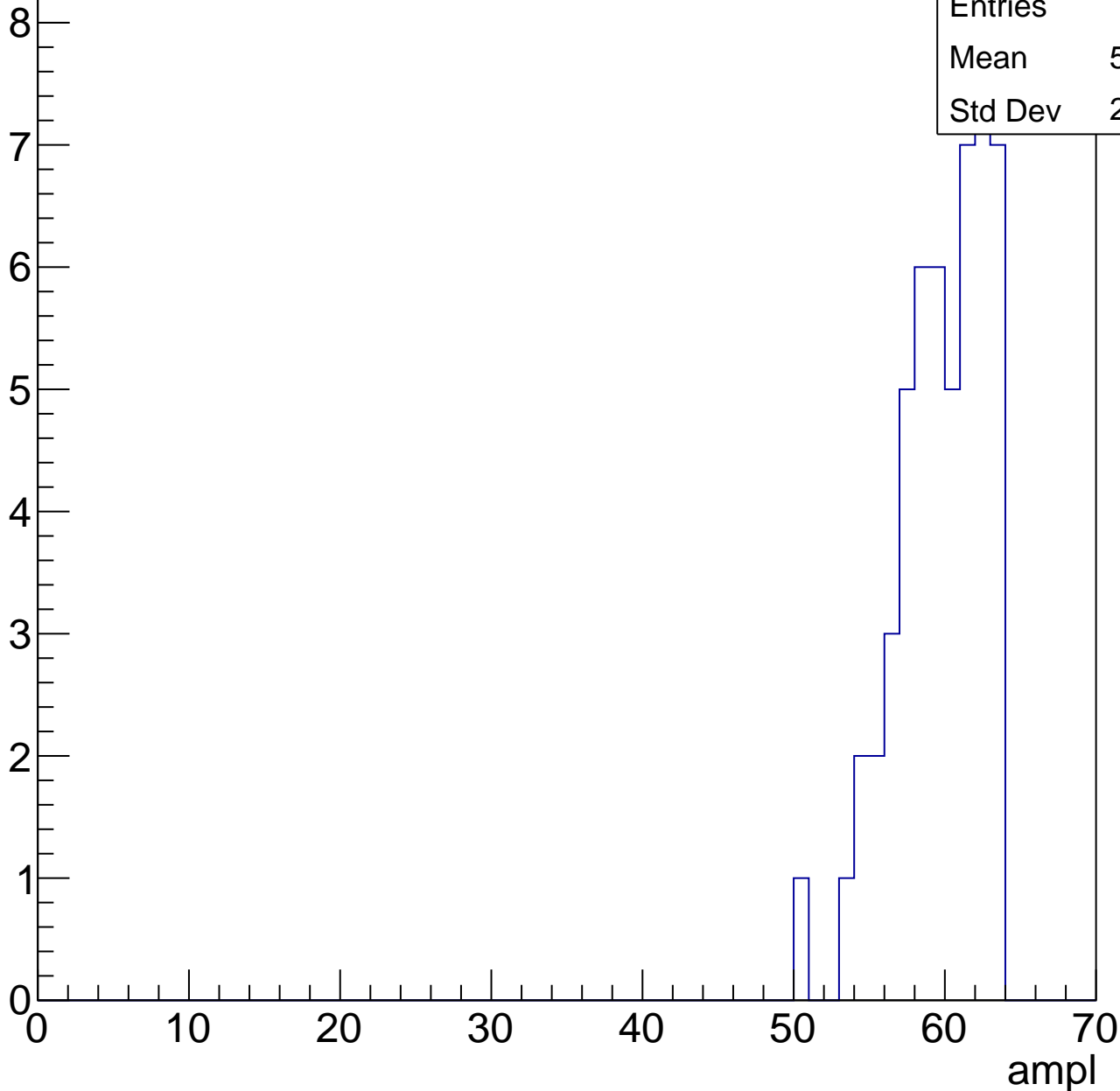


# B1L102S, U12-ch88, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

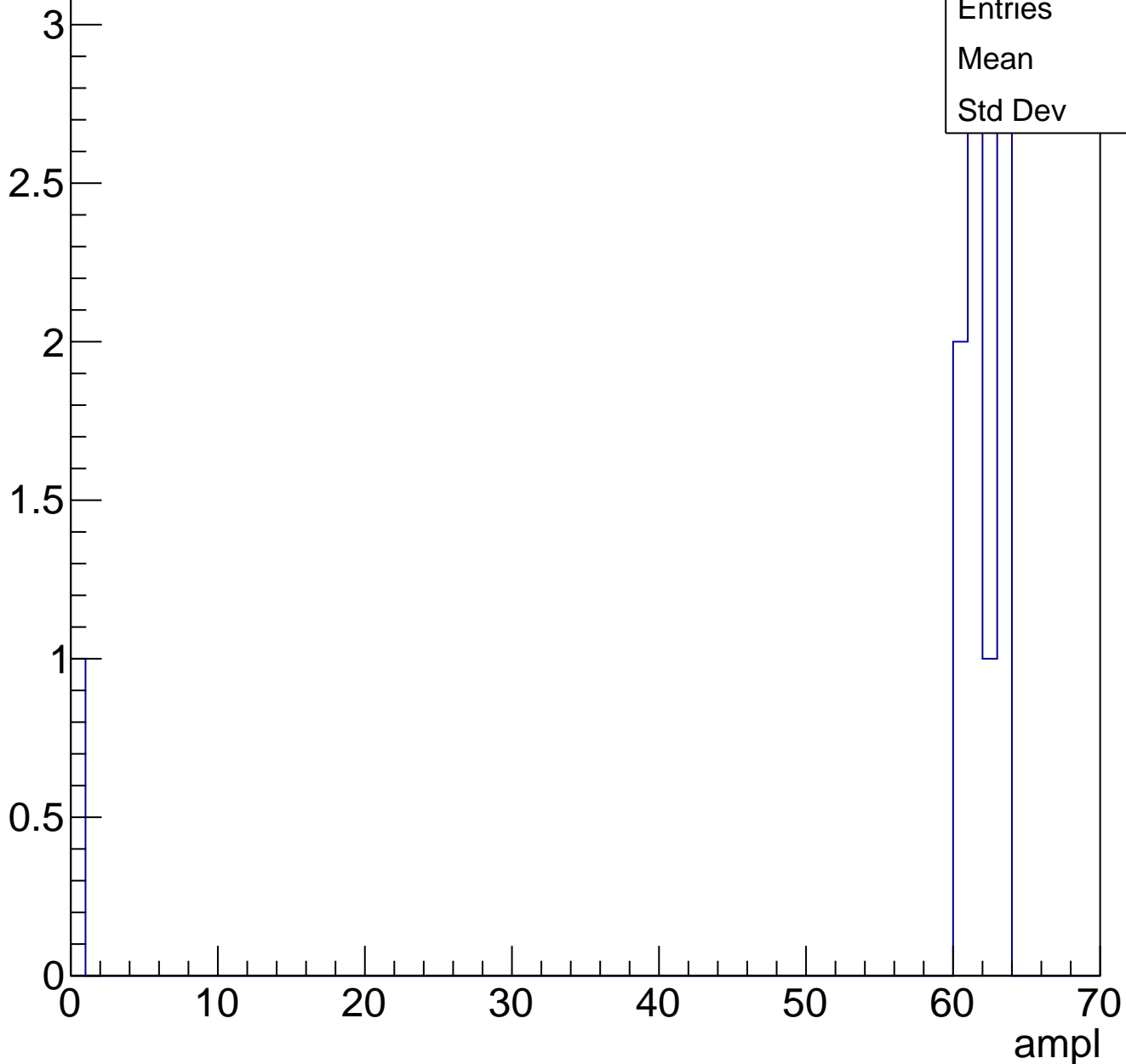
Entries	53
Mean	59.25
Std Dev	2.965



# B1L102S, U12-ch88, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U12-ch88, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U12-ch89, adc0

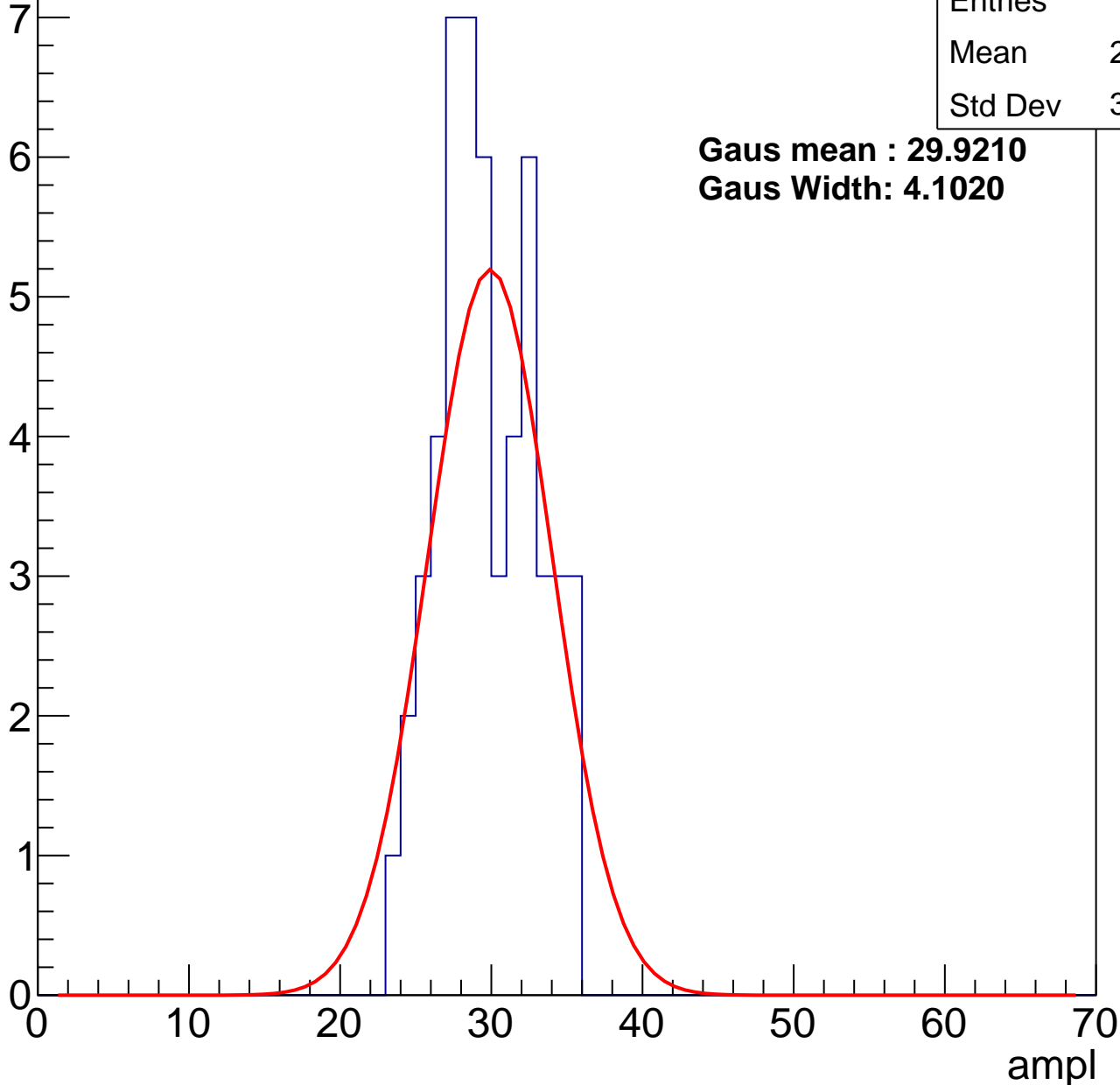
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	52
Mean	29.25
Std Dev	3.119

**Gaus mean : 29.9210**

**Gaus Width: 4.1020**



# B1L102S, U12-ch89, adc1

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	79
Mean	35.9
Std Dev	3.444

**Gaus mean : 36.5659**

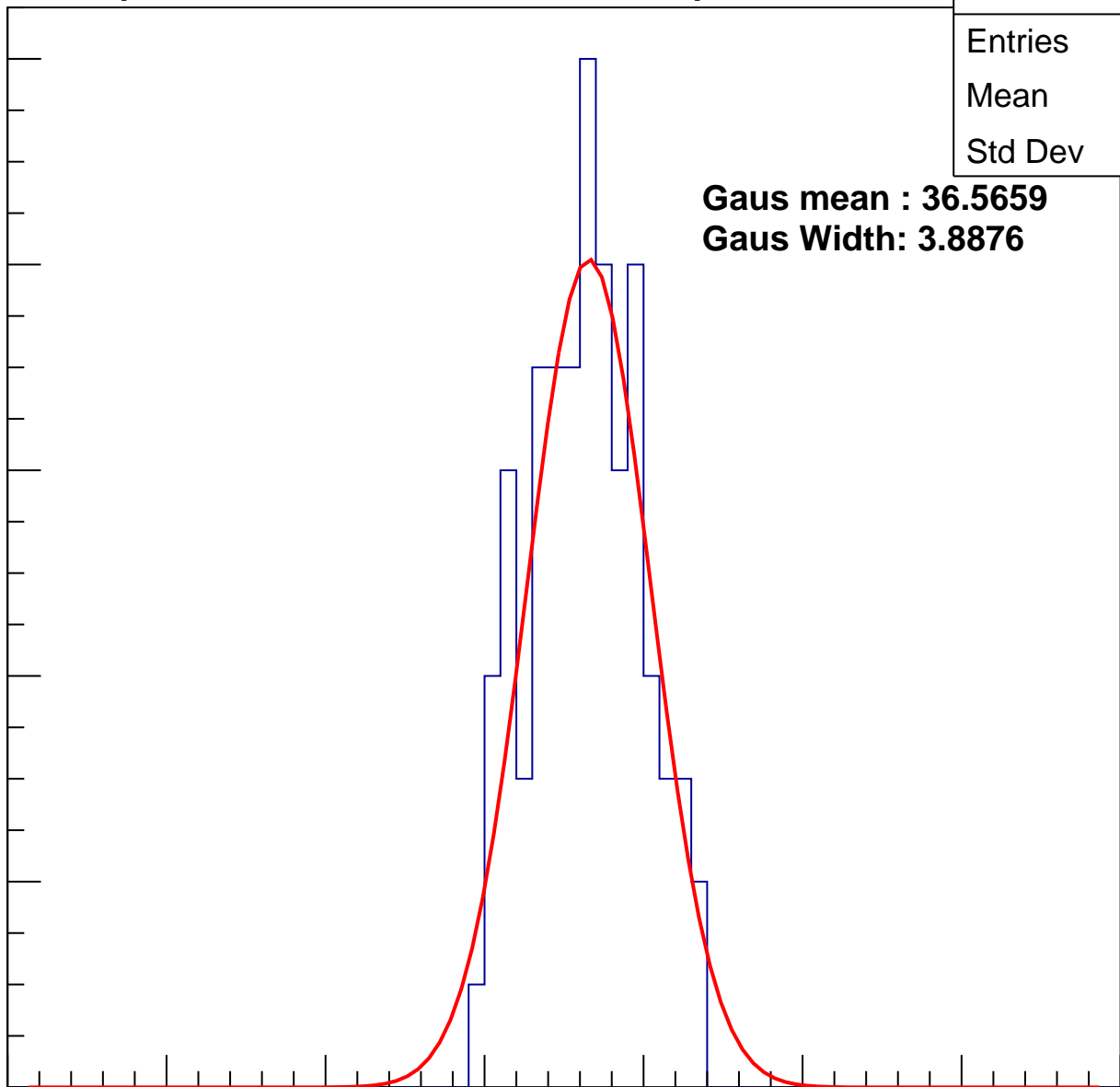
**Gaus Width: 3.8876**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L102S, U12-ch89, adc2

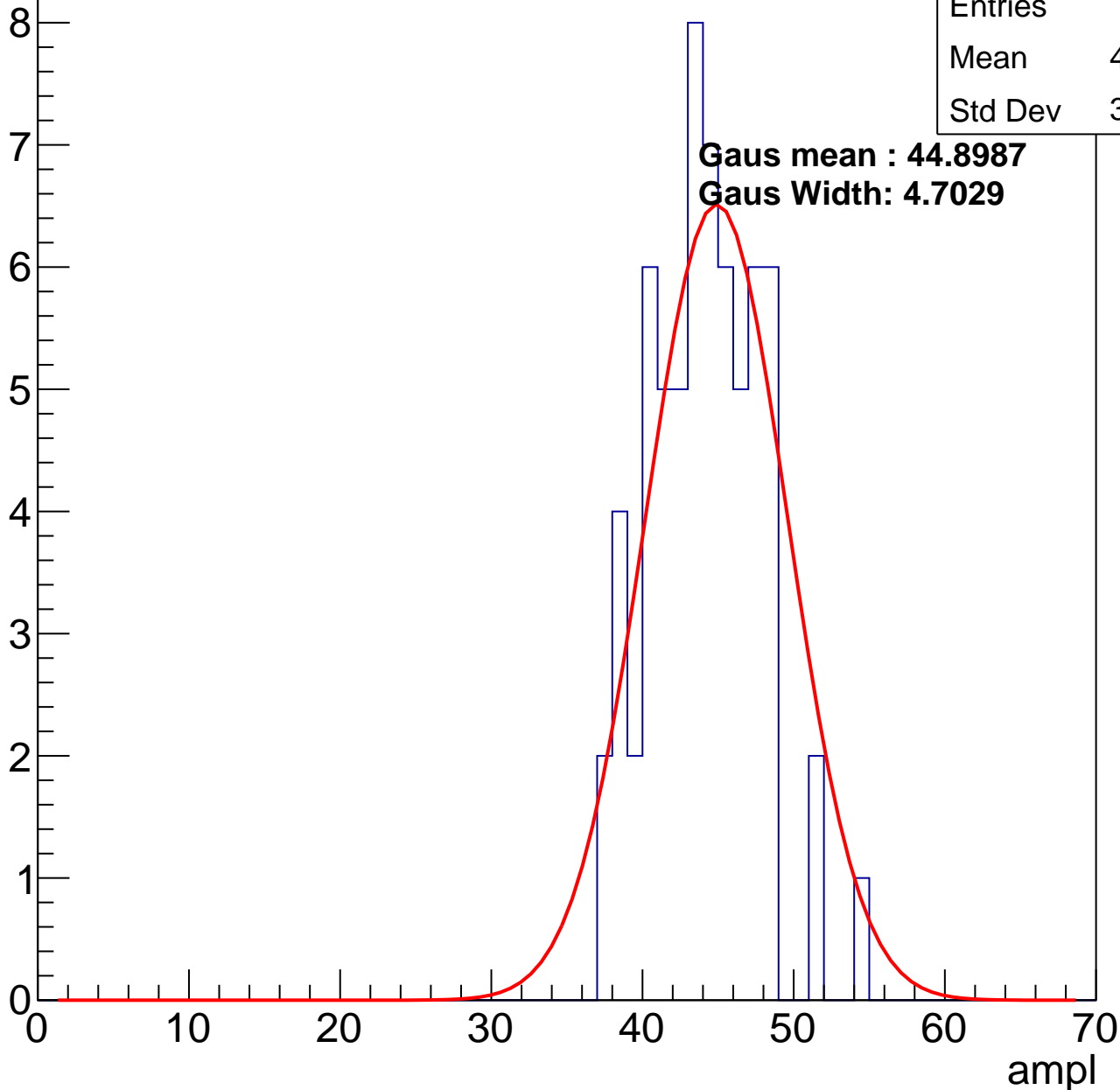
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	65
Mean	43.65
Std Dev	3.567

**Gaus mean : 44.8987**

**Gaus Width: 4.7029**



# B1L102S, U12-ch89, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

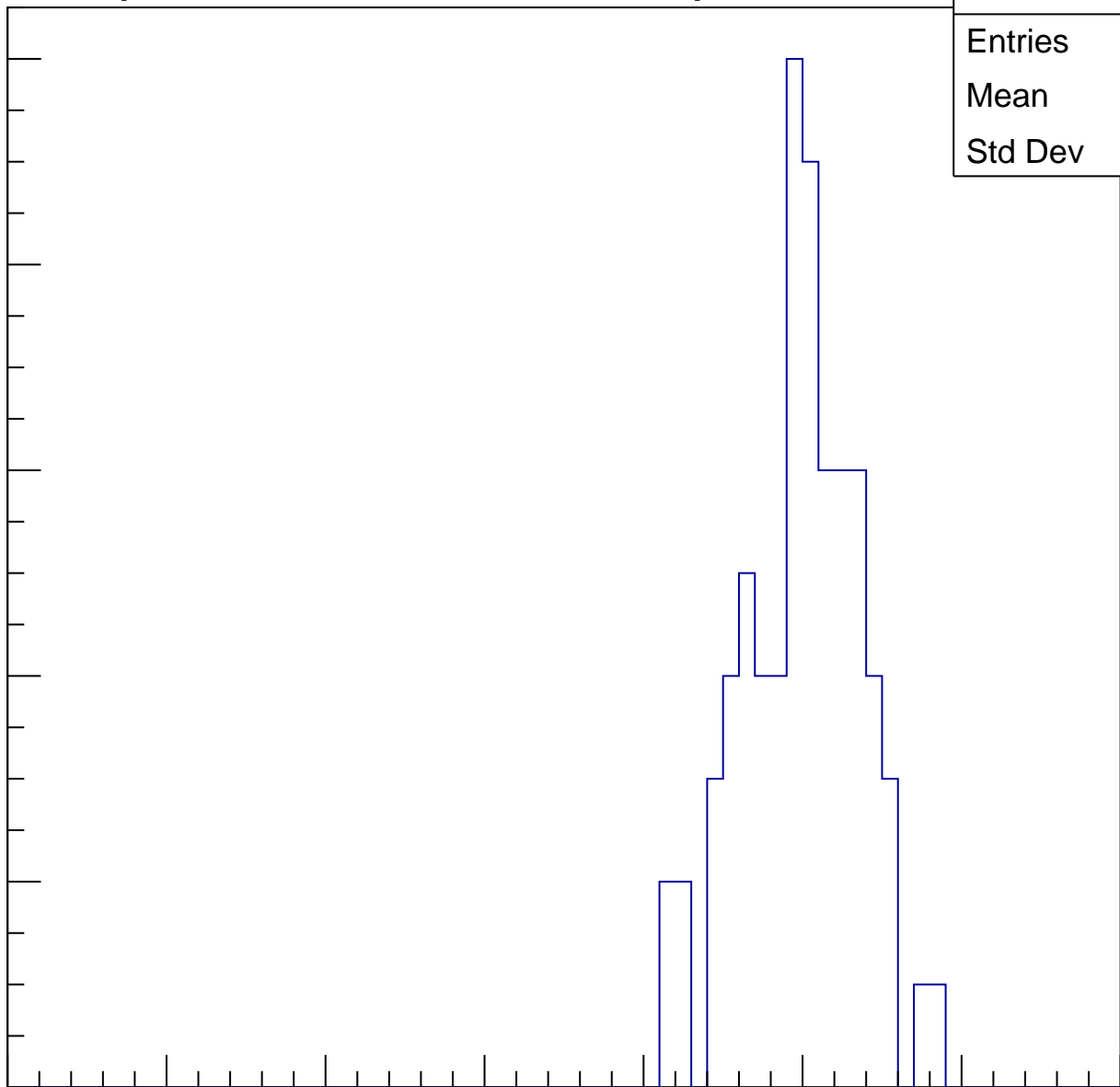
Entries	70
Mean	49.43
Std Dev	3.69

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

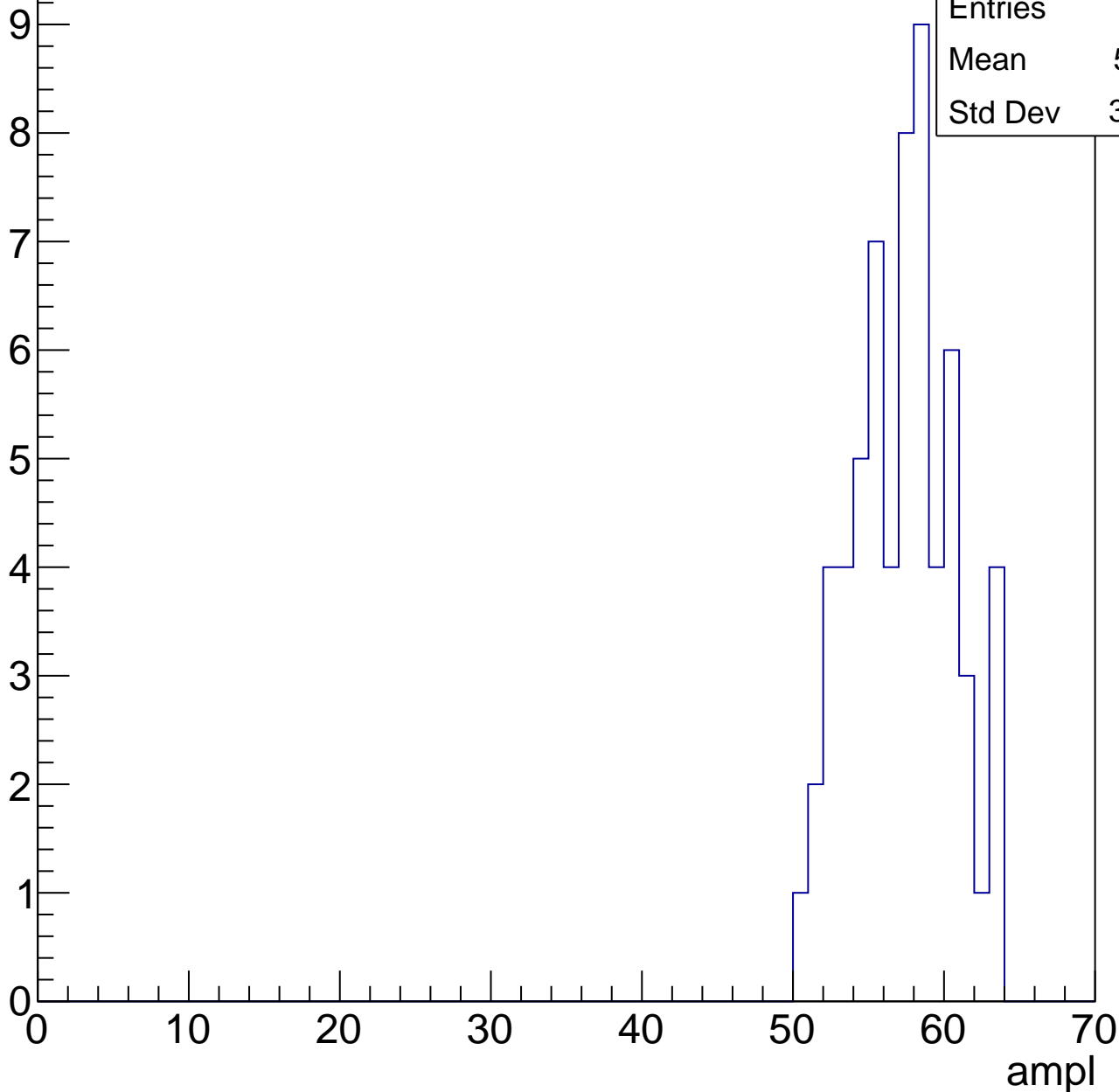


# B1L102S, U12-ch89, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	62
Mean	56.81
Std Dev	3.252

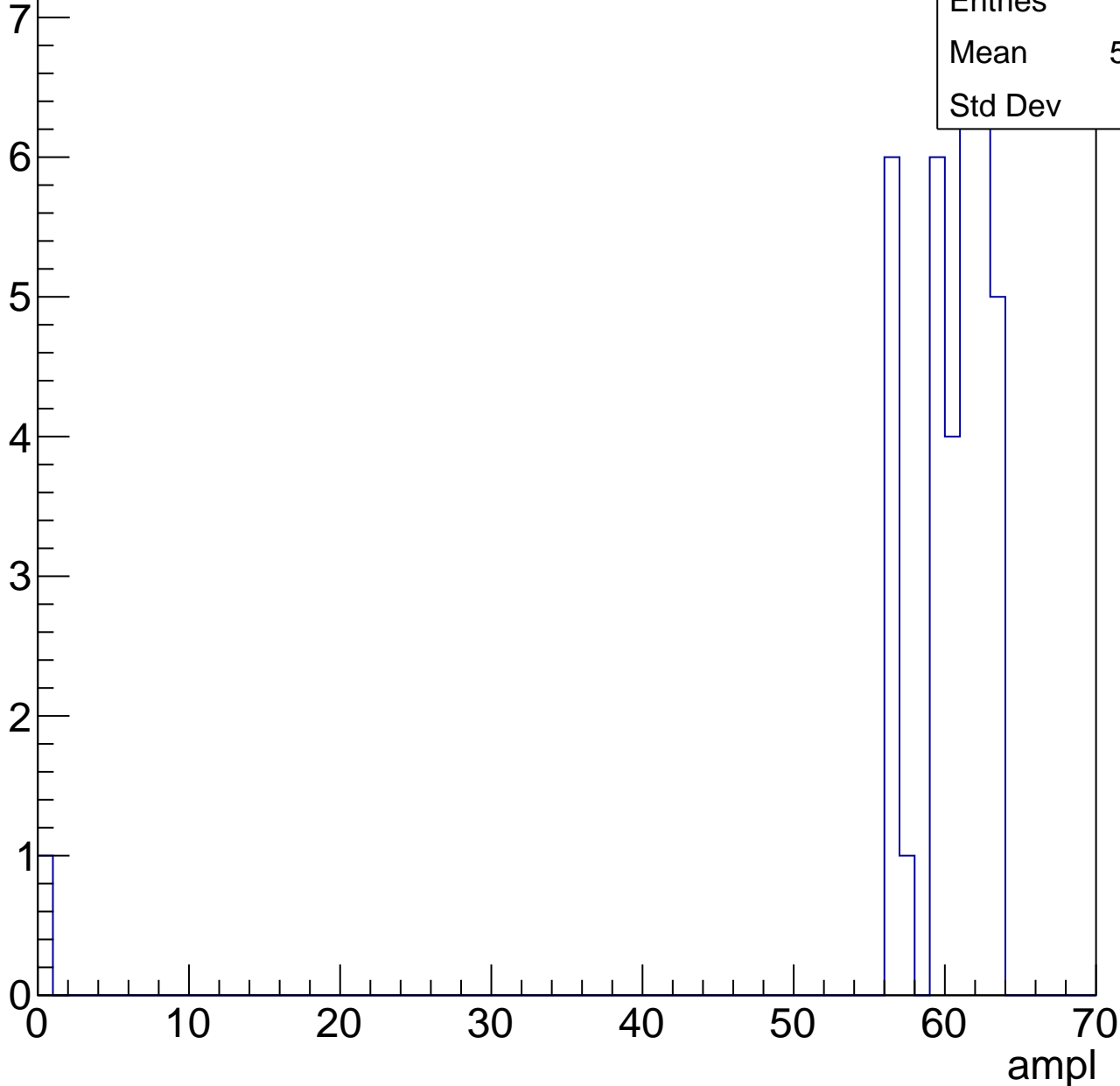


# B1L102S, U12-ch89, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	37
Mean	58.46
Std Dev	10



# B1L102S, U12-ch89, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U12-ch89, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	2
Mean	11
Std Dev	11

# B1L102S, U12-ch90, adc0

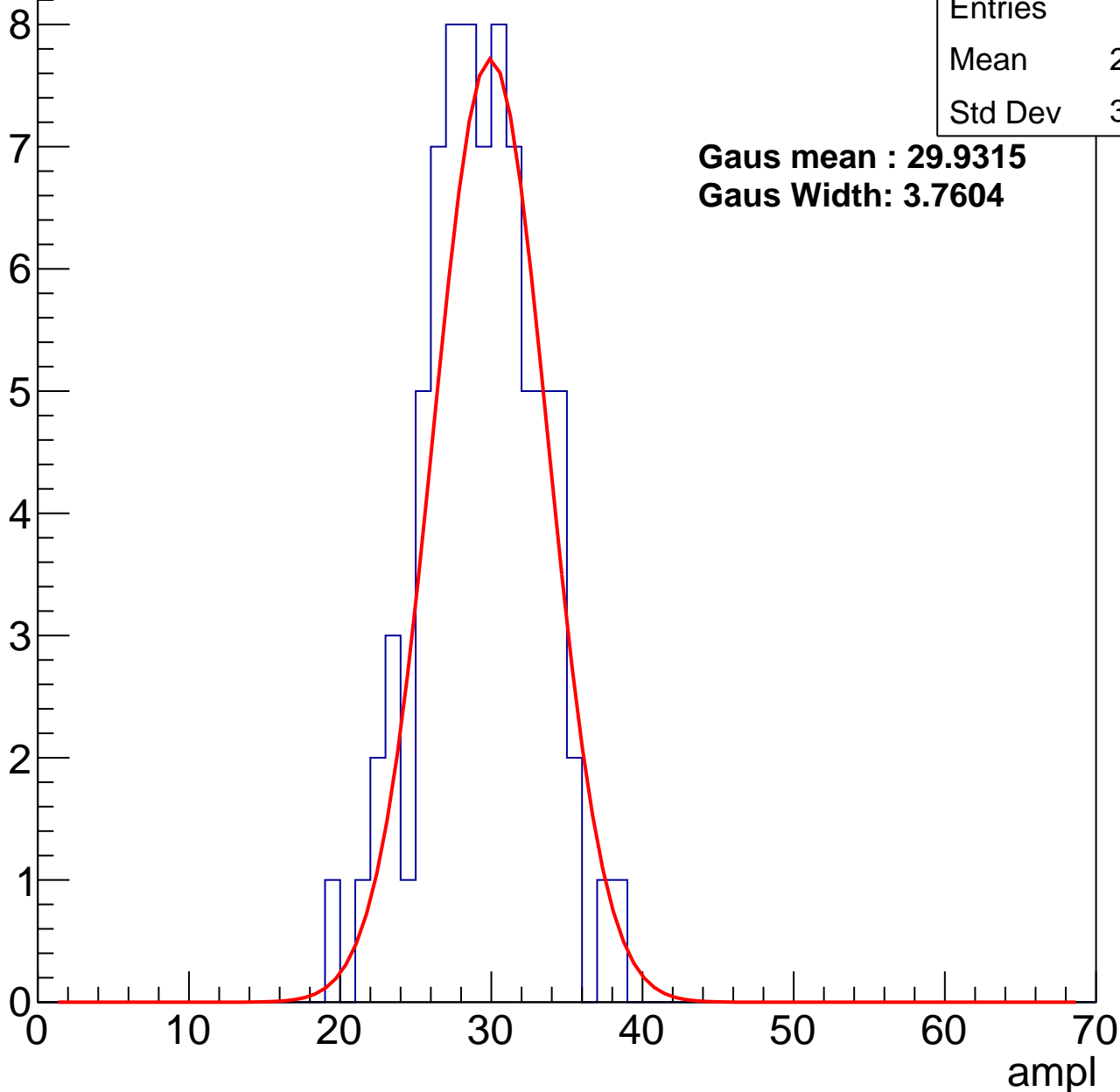
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	77
Mean	28.88
Std Dev	3.745

**Gaus mean : 29.9315**

**Gaus Width: 3.7604**



# B1L102S, U12-ch90, adc1

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	70
Mean	35.7
Std Dev	3.575

**Gaus mean : 36.0690**

**Gaus Width: 3.5931**

Entry

10  
8  
6  
4  
2  
0

ampl

0

10

20

30

40

50

60

70

# B1L102S, U12-ch90, adc2

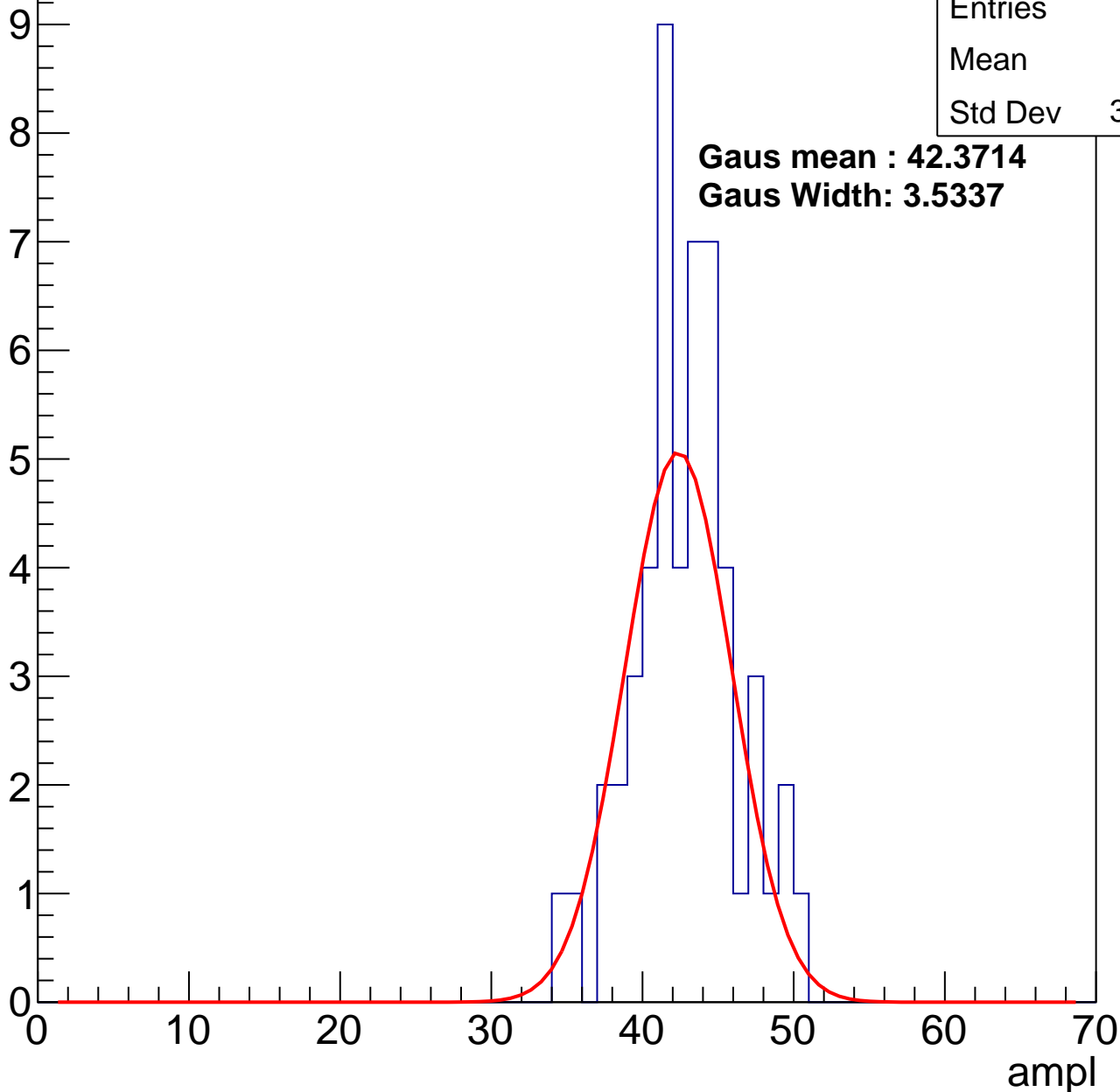
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	52
Mean	42.4
Std Dev	3.393

**Gaus mean : 42.3714**

**Gaus Width: 3.5337**

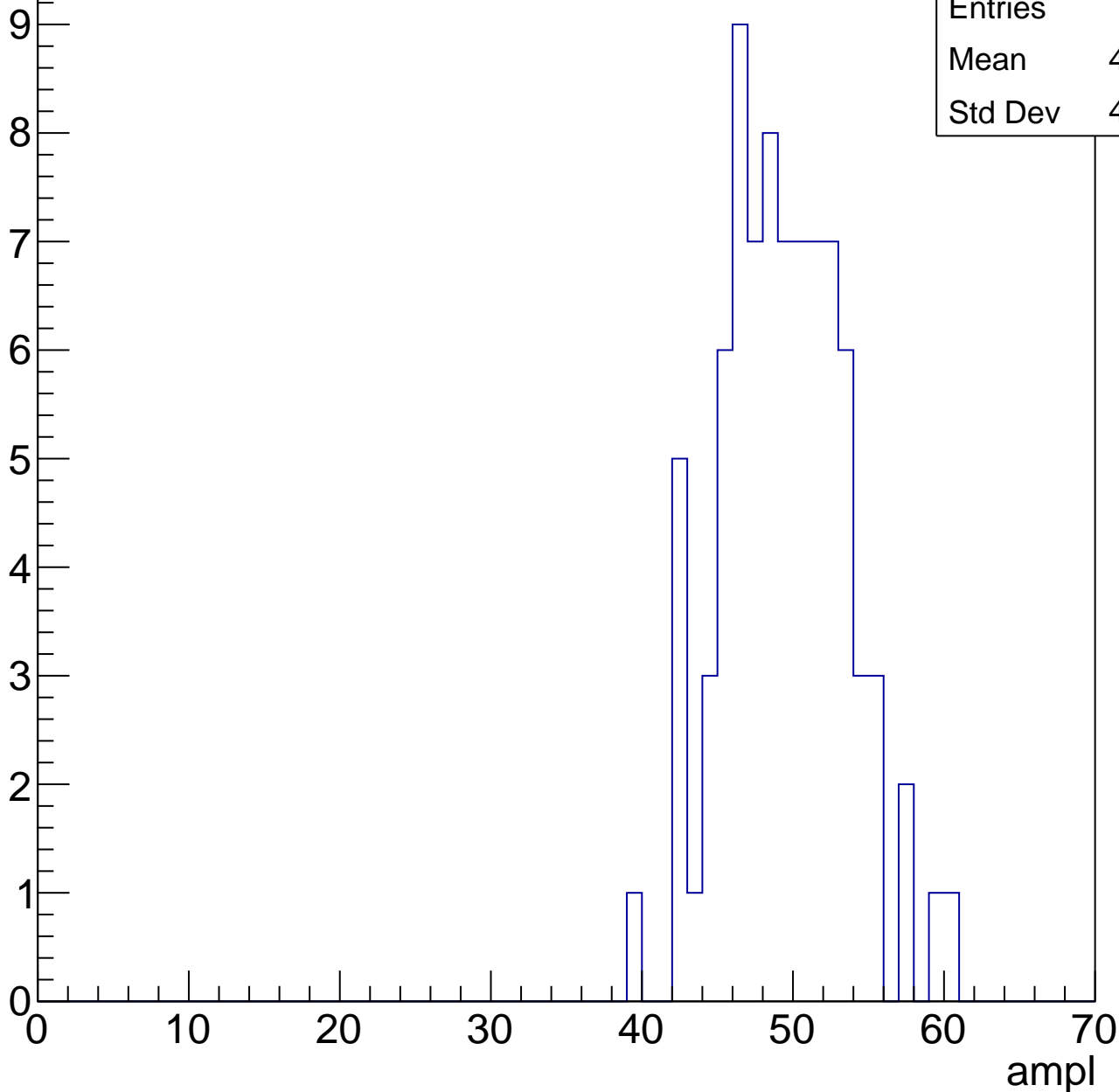


# B1L102S, U12-ch90, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	84
Mean	48.96
Std Dev	4.075

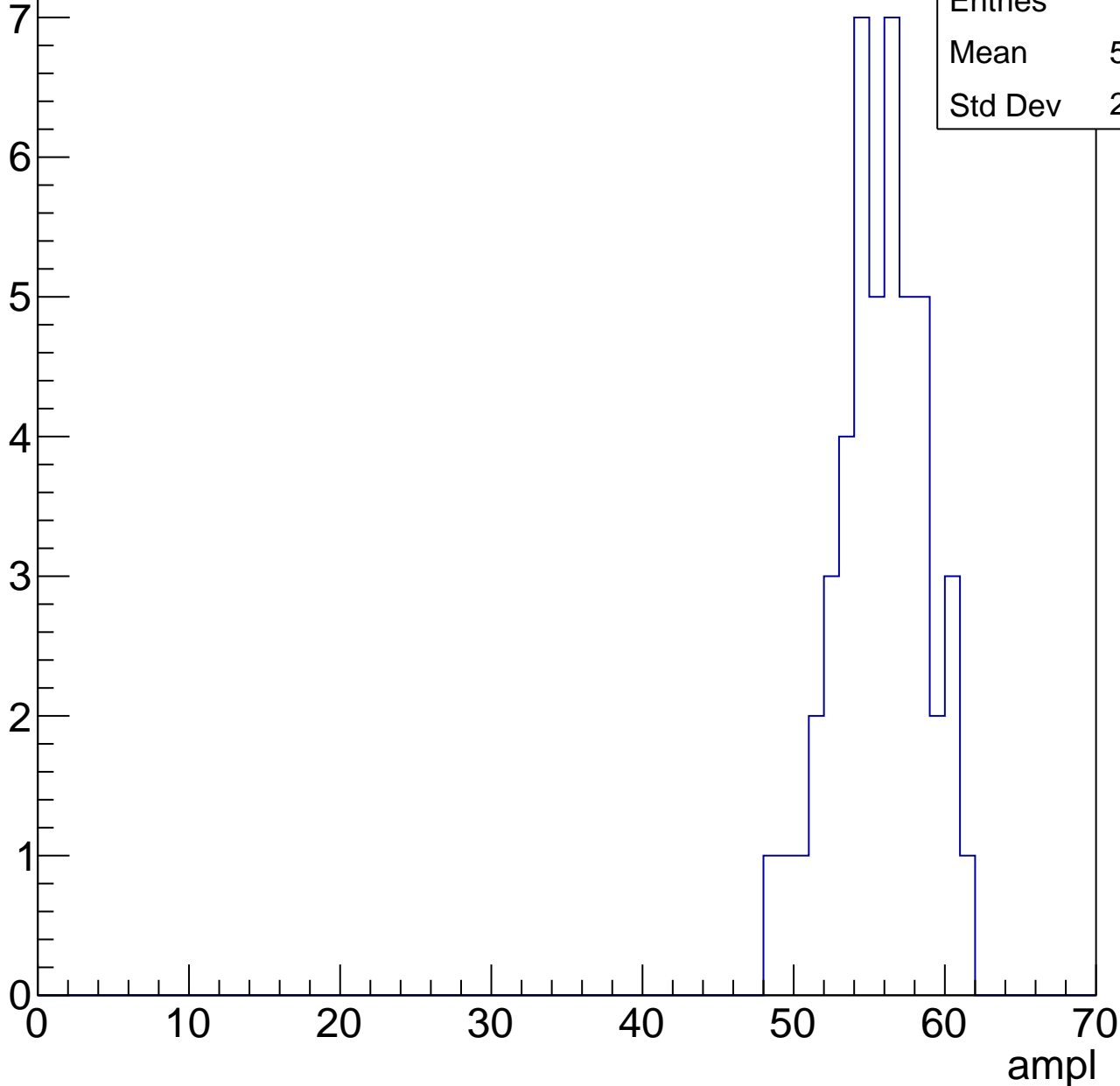


# B1L102S, U12-ch90, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	47
Mean	55.23
Std Dev	2.933

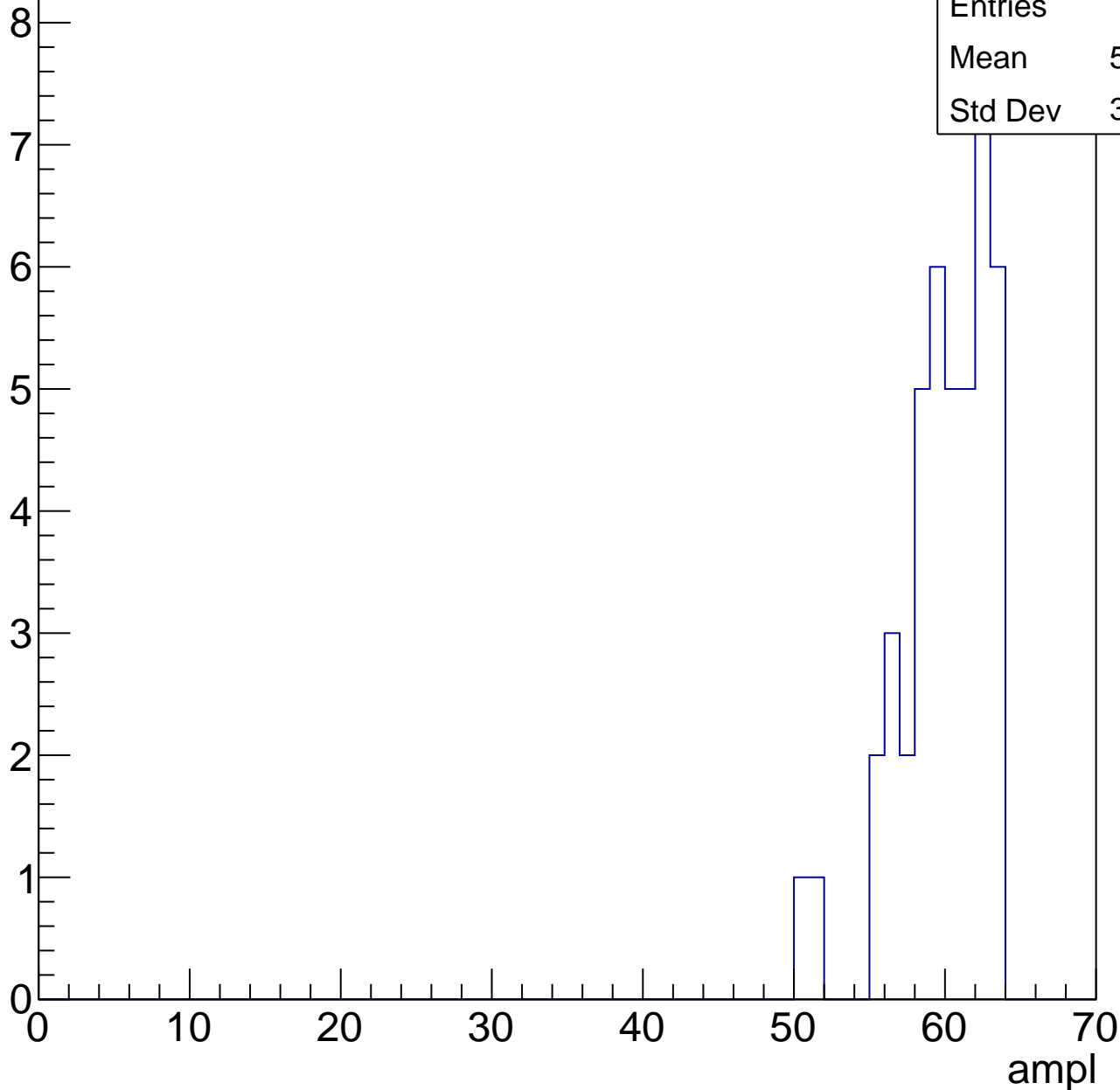


# B1L102S, U12-ch90, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

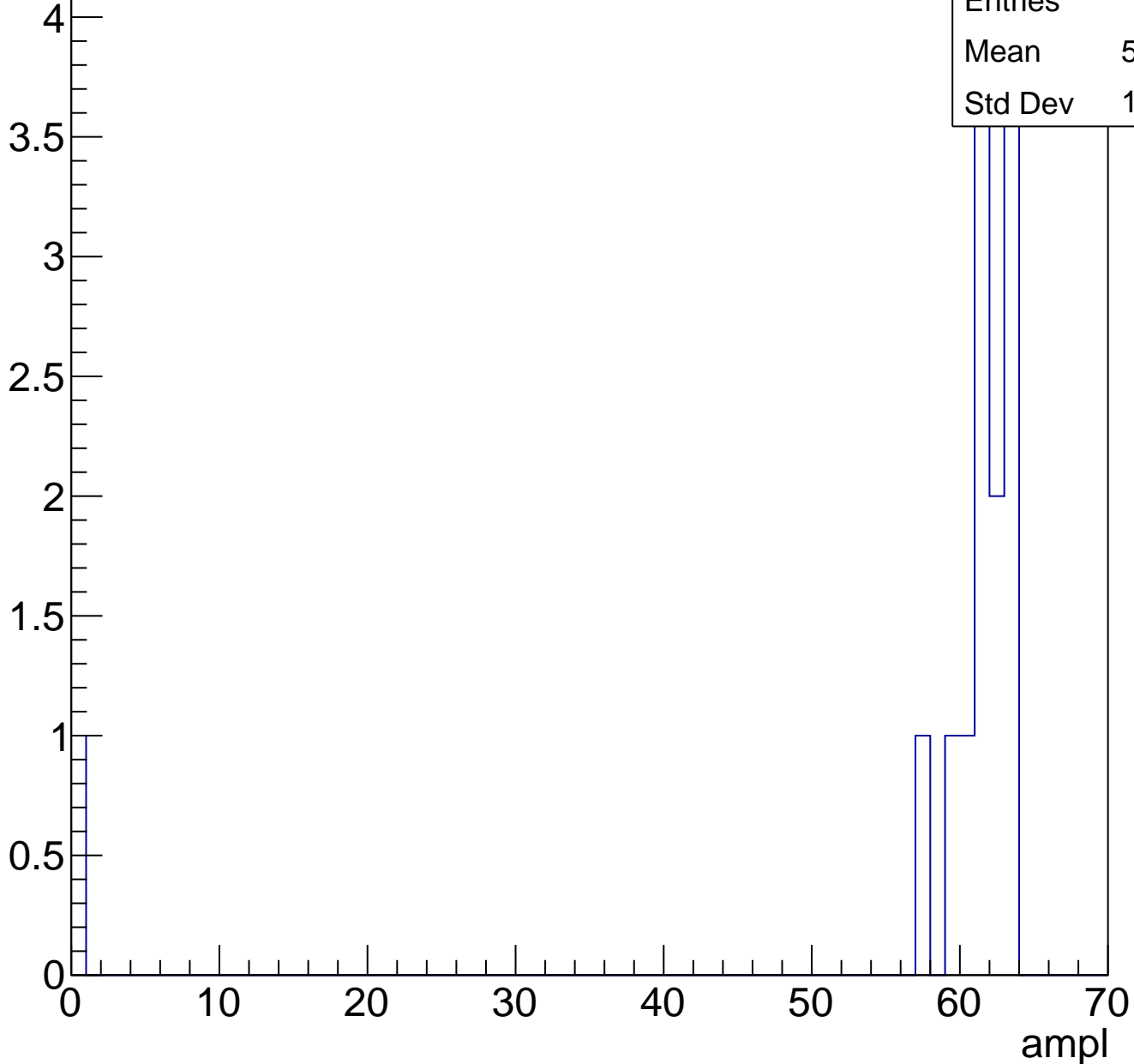
Entries	44
Mean	59.45
Std Dev	3.019



# B1L102S, U12-ch90, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U12-ch90, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	2
Mean	9.5
Std Dev	9.5

# B1L102S, U12-ch91, adc0

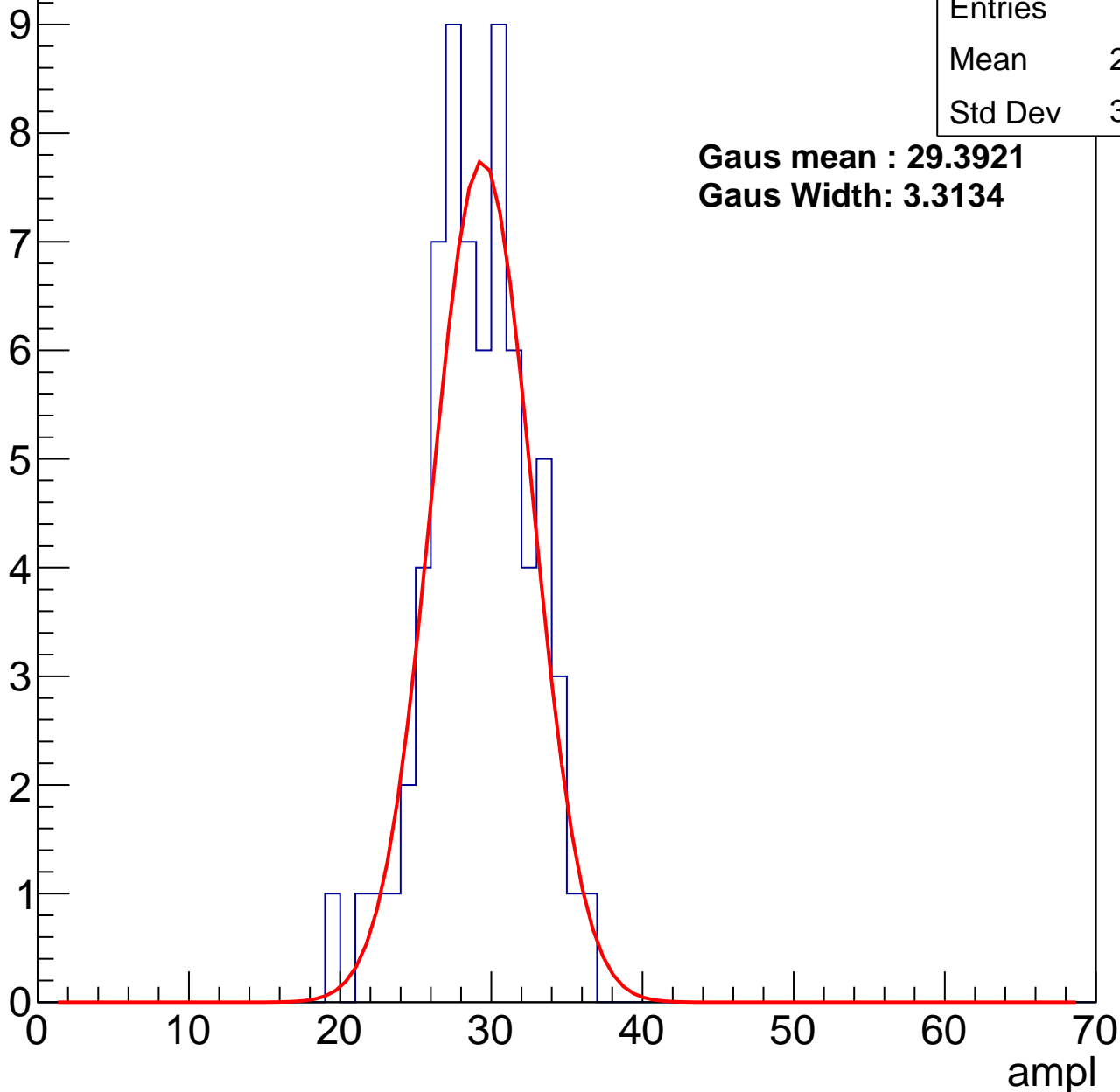
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	28.68
Std Dev	3.367

**Gaus mean : 29.3921**

**Gaus Width: 3.3134**



# B1L102S, U12-ch91, adc1

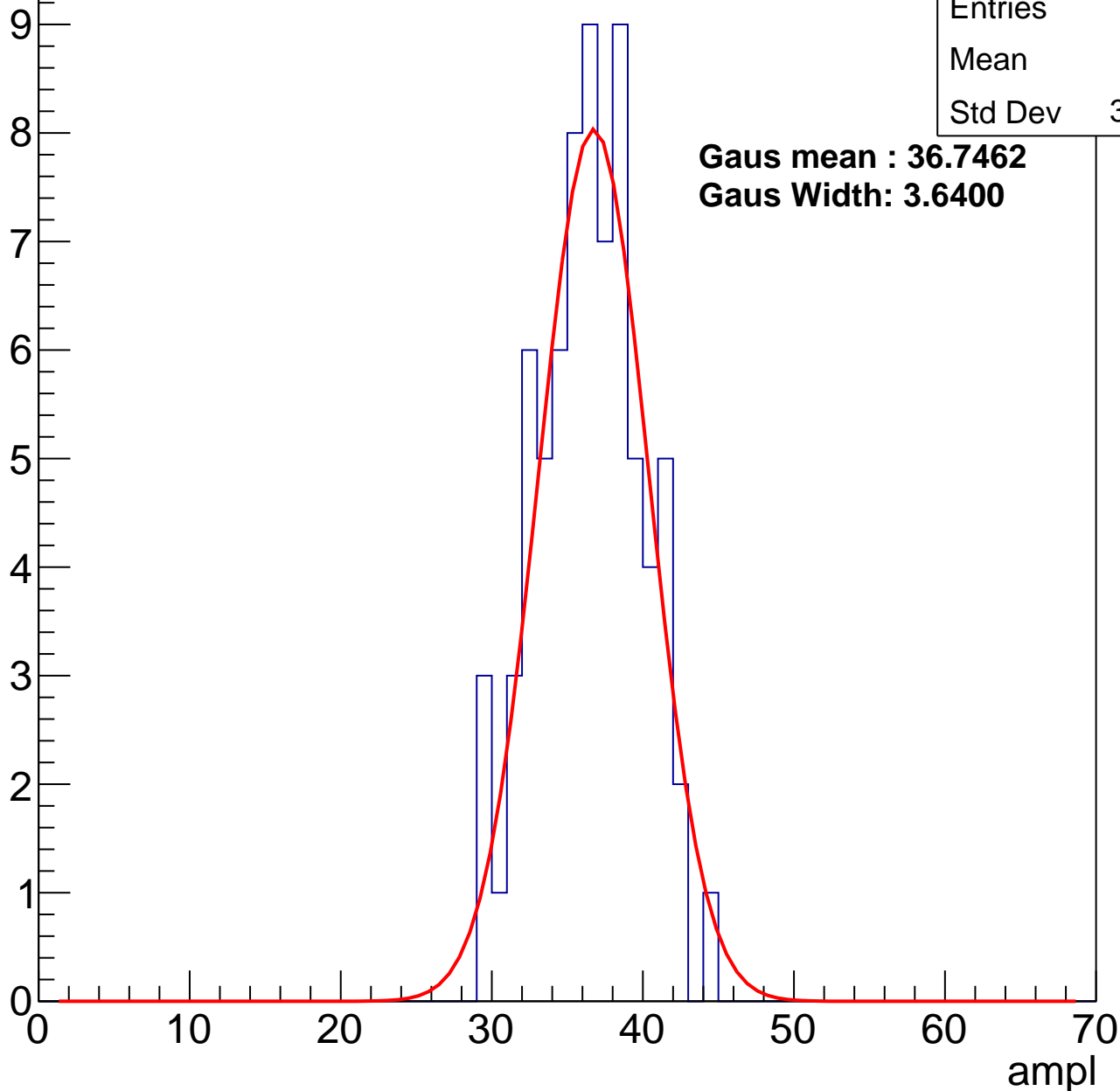
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	74
Mean	36
Std Dev	3.377

**Gaus mean : 36.7462**

**Gaus Width: 3.6400**



# B1L102S, U12-ch91, adc2

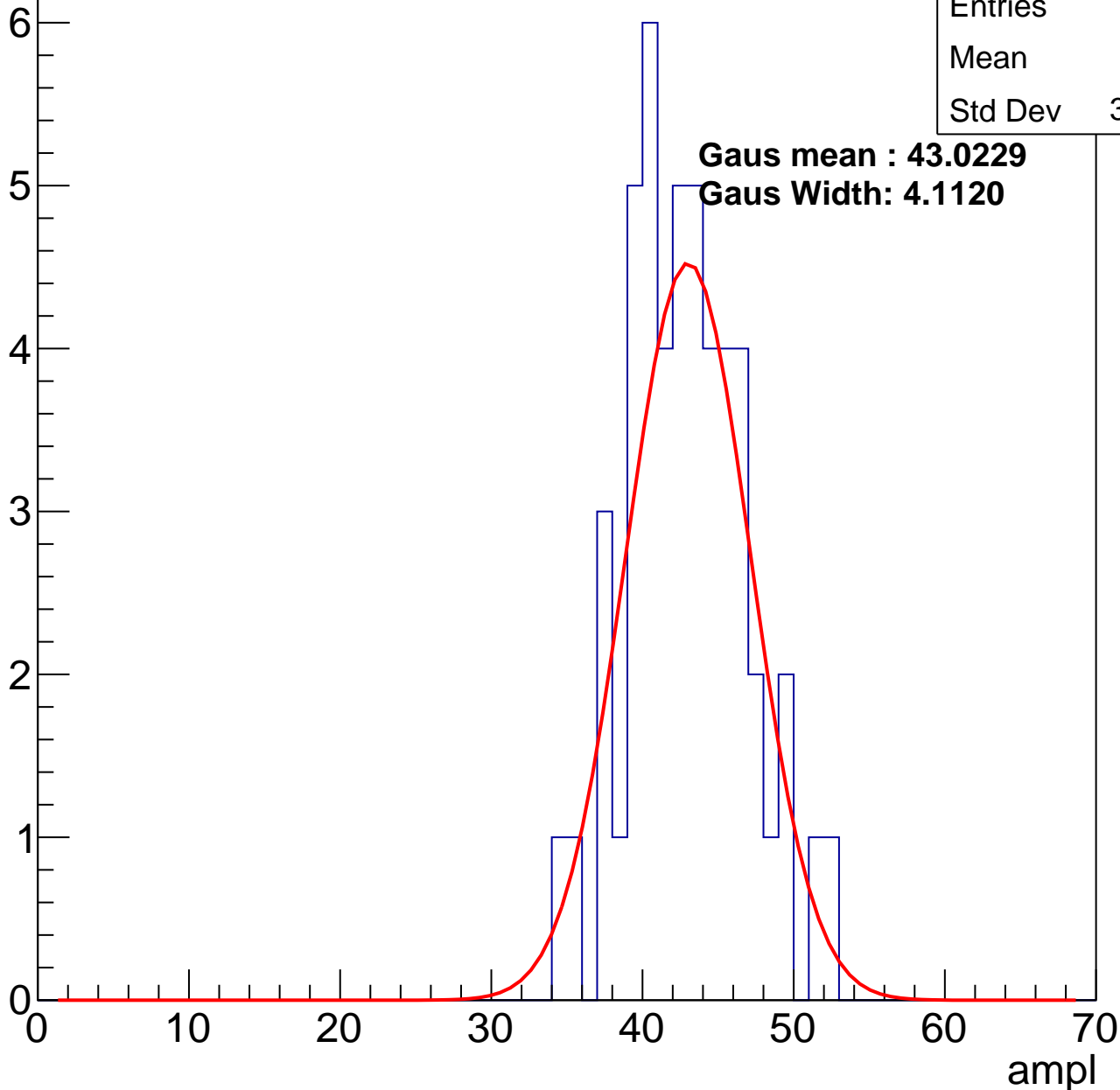
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	50
Mean	42.5
Std Dev	3.874

**Gaus mean : 43.0229**

**Gaus Width: 4.1120**

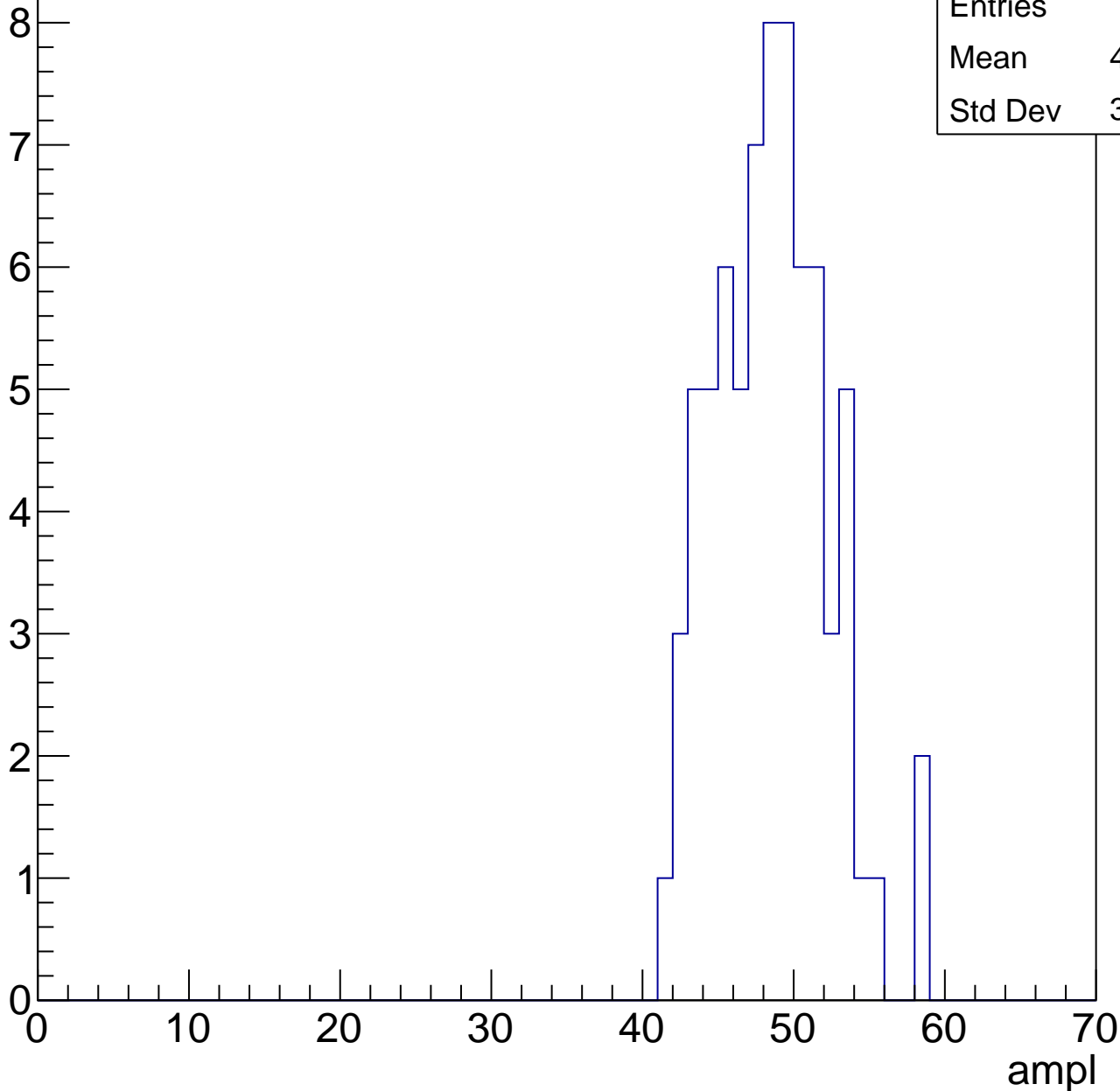


# B1L102S, U12-ch91, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	72
Mean	48.04
Std Dev	3.702

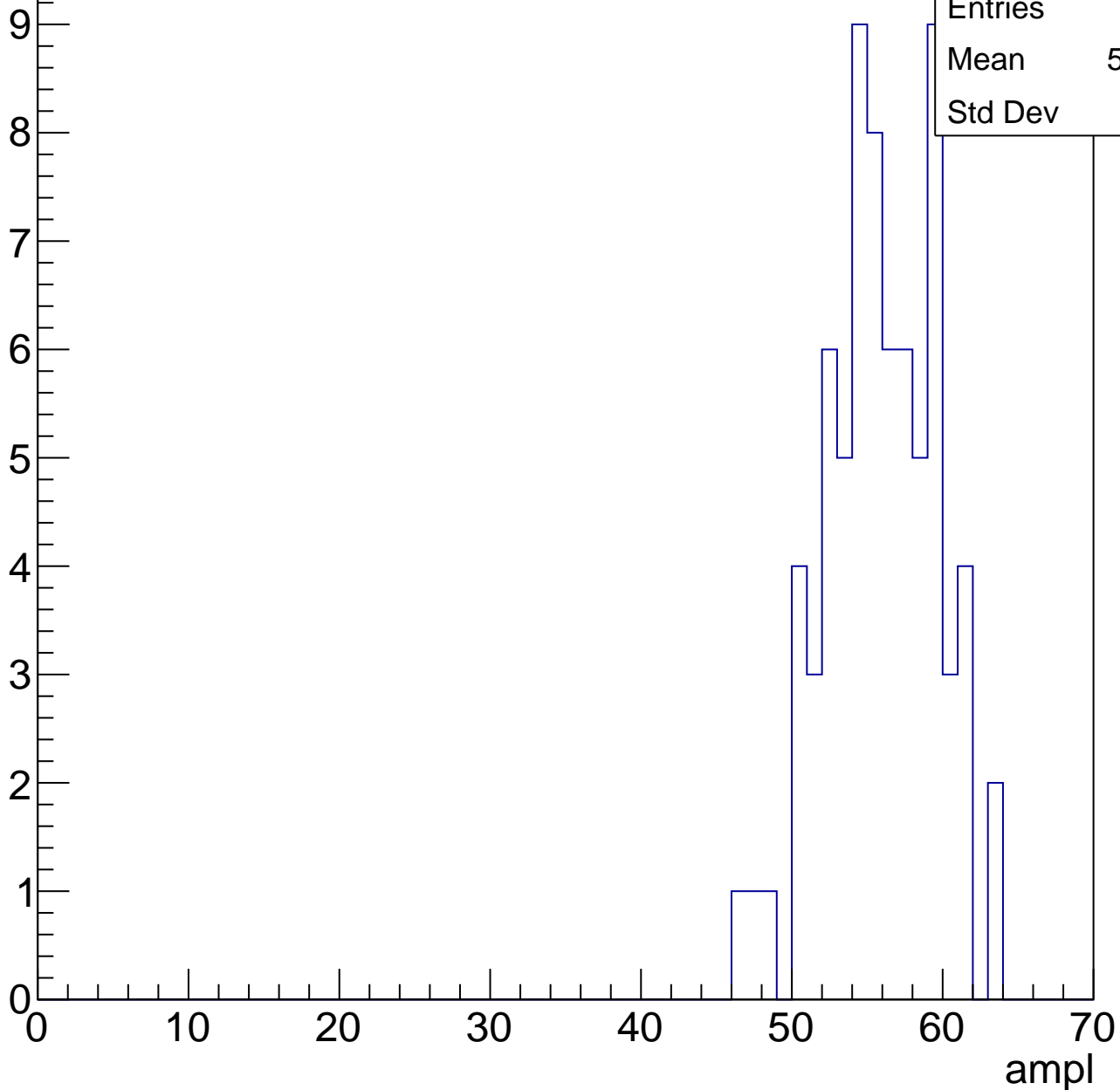


# B1L102S, U12-ch91, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	73
Mean	55.42
Std Dev	3.66

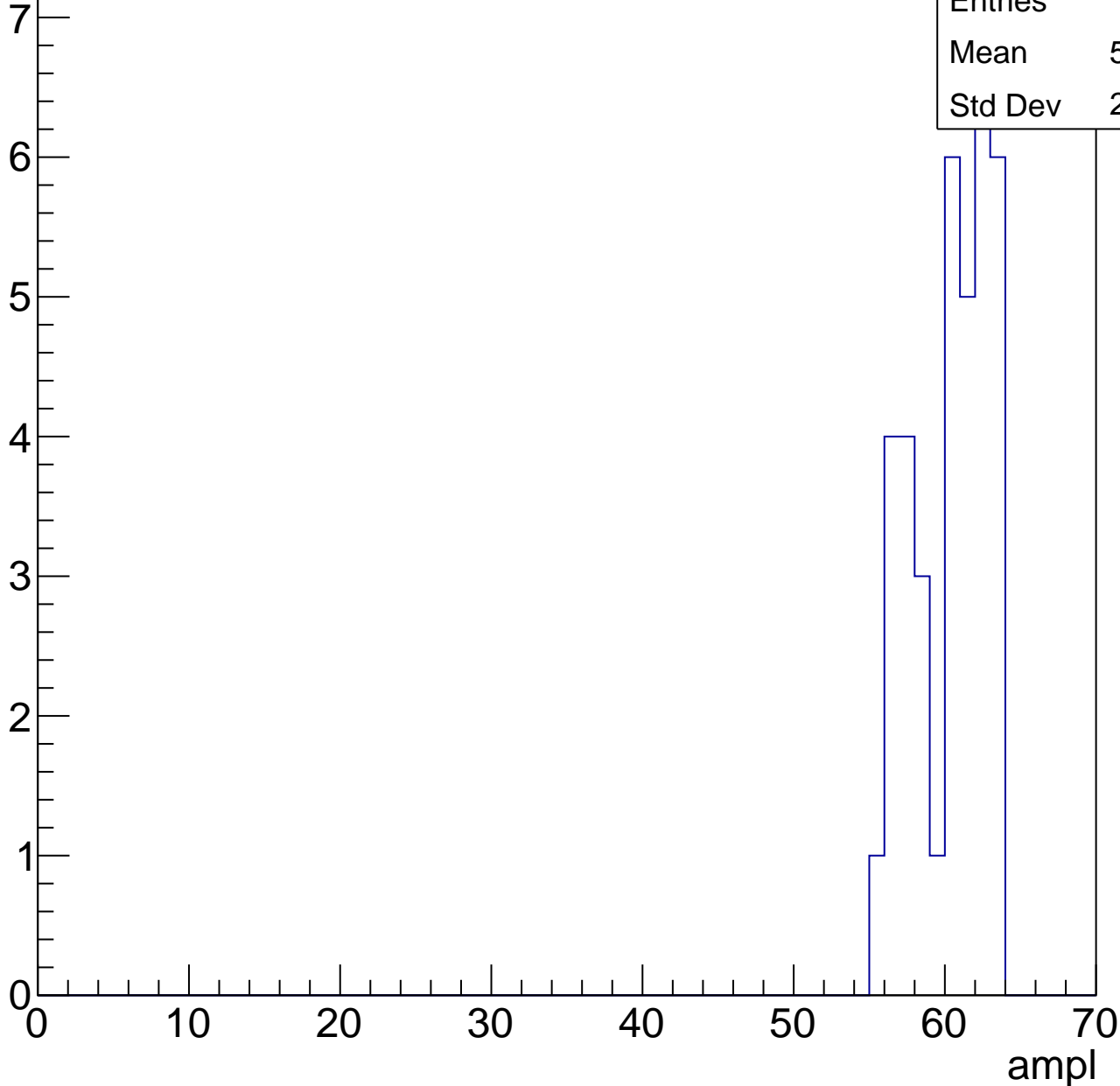


# B1L102S, U12-ch91, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	37
Mean	59.92
Std Dev	2.465



# B1L102S, U12-ch91, adc6

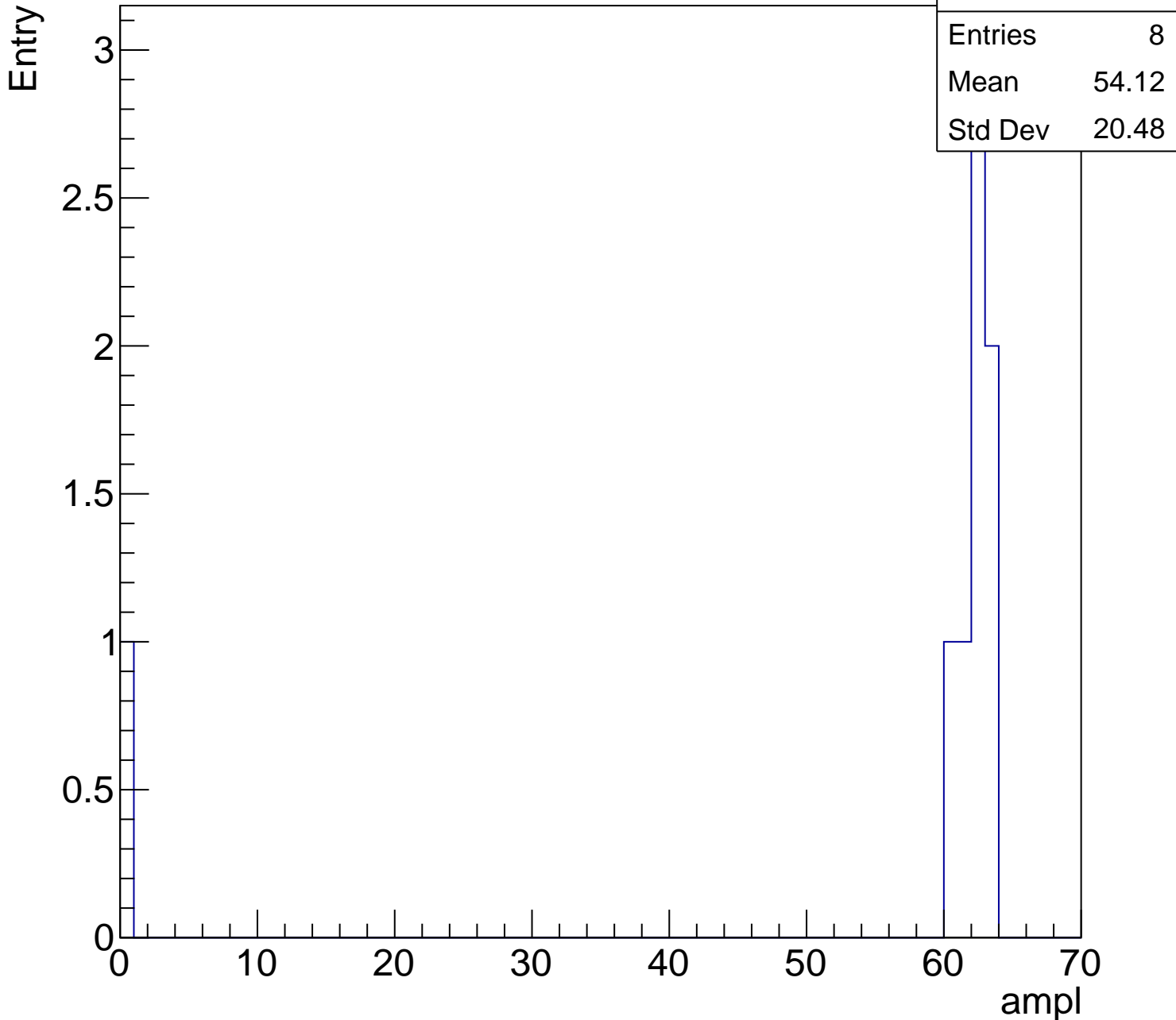
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

3  
2.5  
2  
1.5  
1  
0.5  
0

Entries	8
Mean	54.12
Std Dev	20.48

ampl





# B1L102S, U12-ch91, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L102S, U12-ch92, adc0

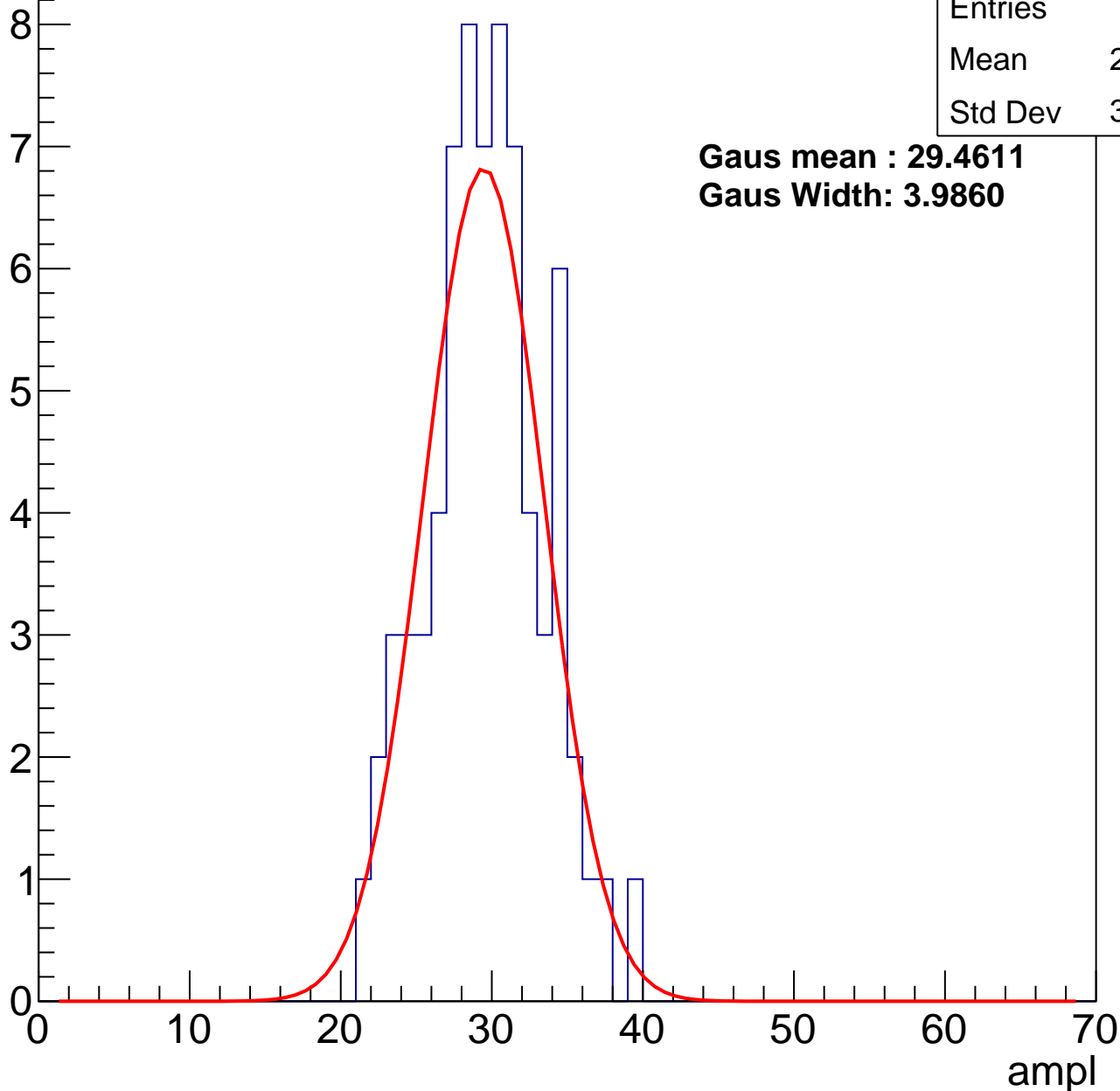
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	71
Mean	29.17
Std Dev	3.787

**Gaus mean : 29.4611**

**Gaus Width: 3.9860**



# B1L102S, U12-ch92, adc1

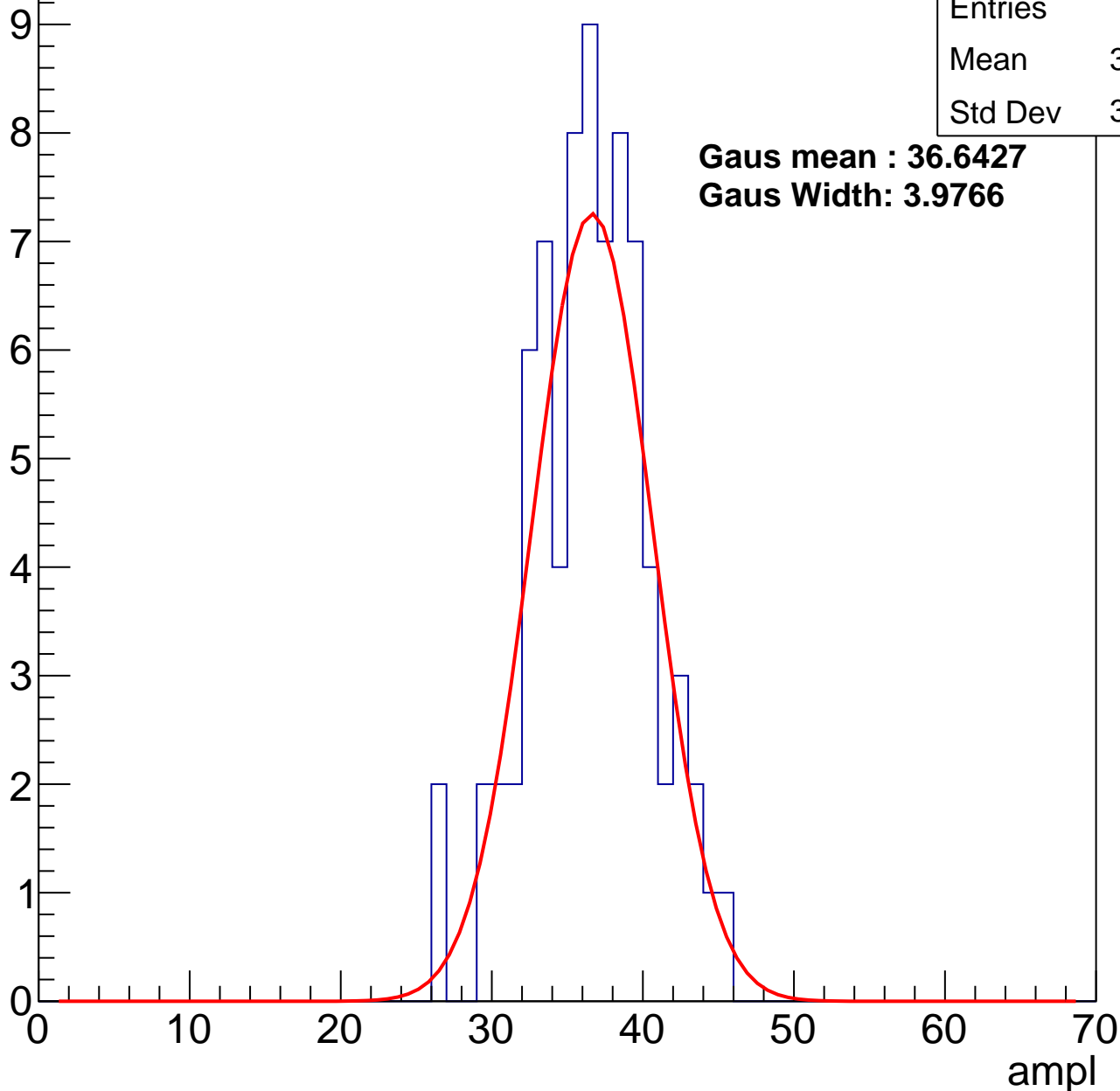
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	77
Mean	36.03
Std Dev	3.898

**Gaus mean : 36.6427**

**Gaus Width: 3.9766**

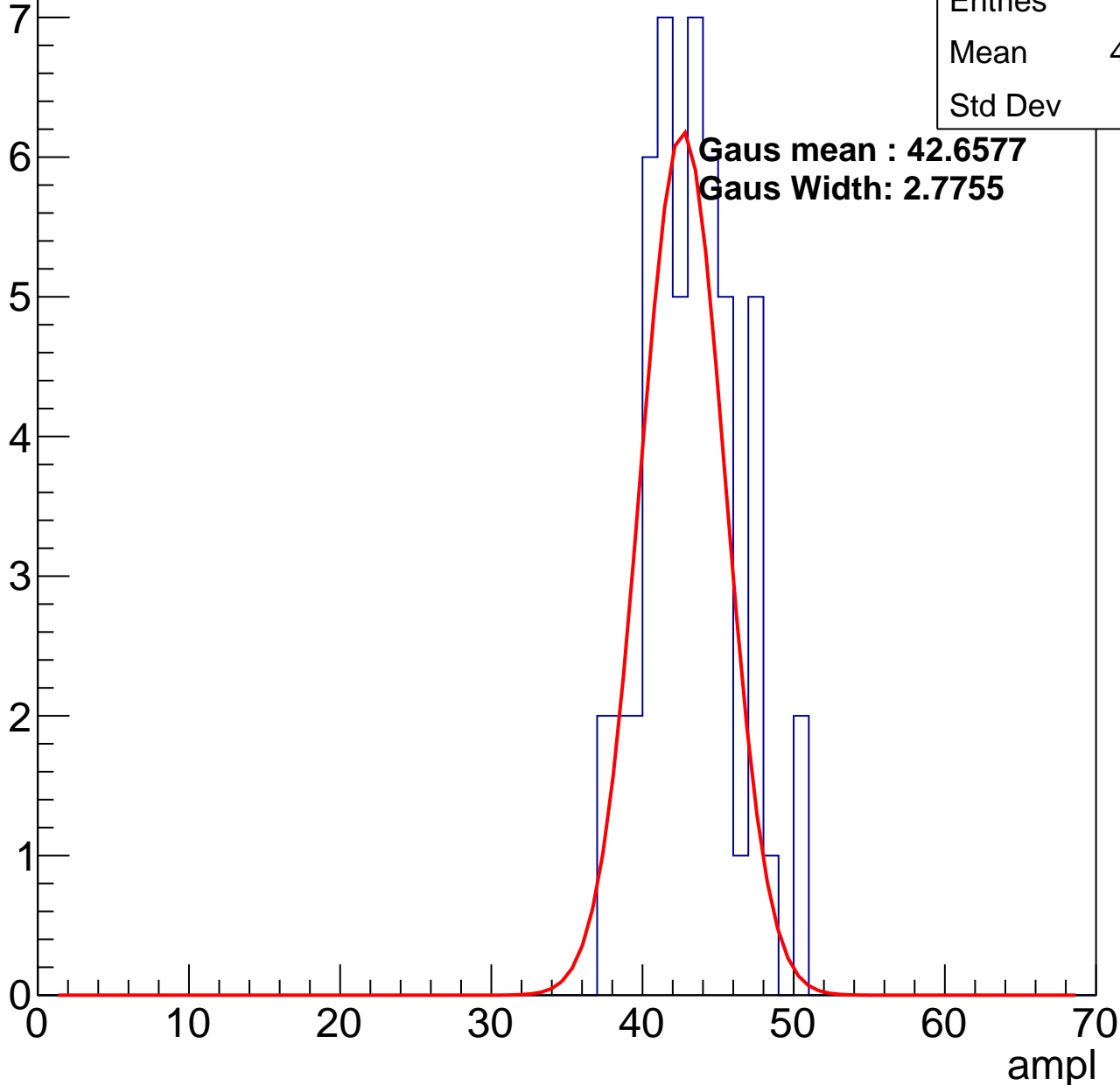


# B1L102S, U12-ch92, adc2

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	51
Mean	42.82
Std Dev	3.06

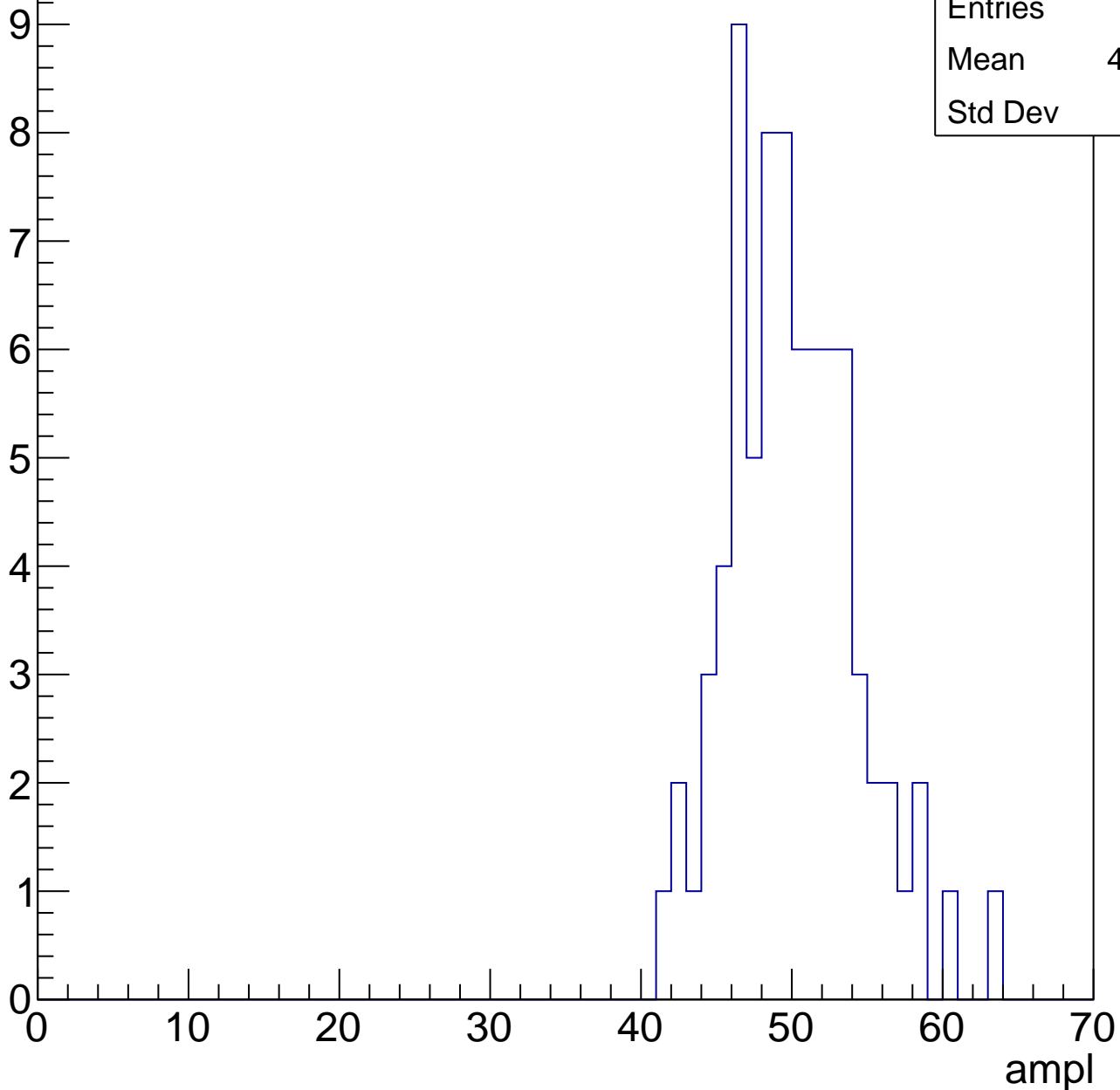


# B1L102S, U12-ch92, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	77
Mean	49.62
Std Dev	4.24

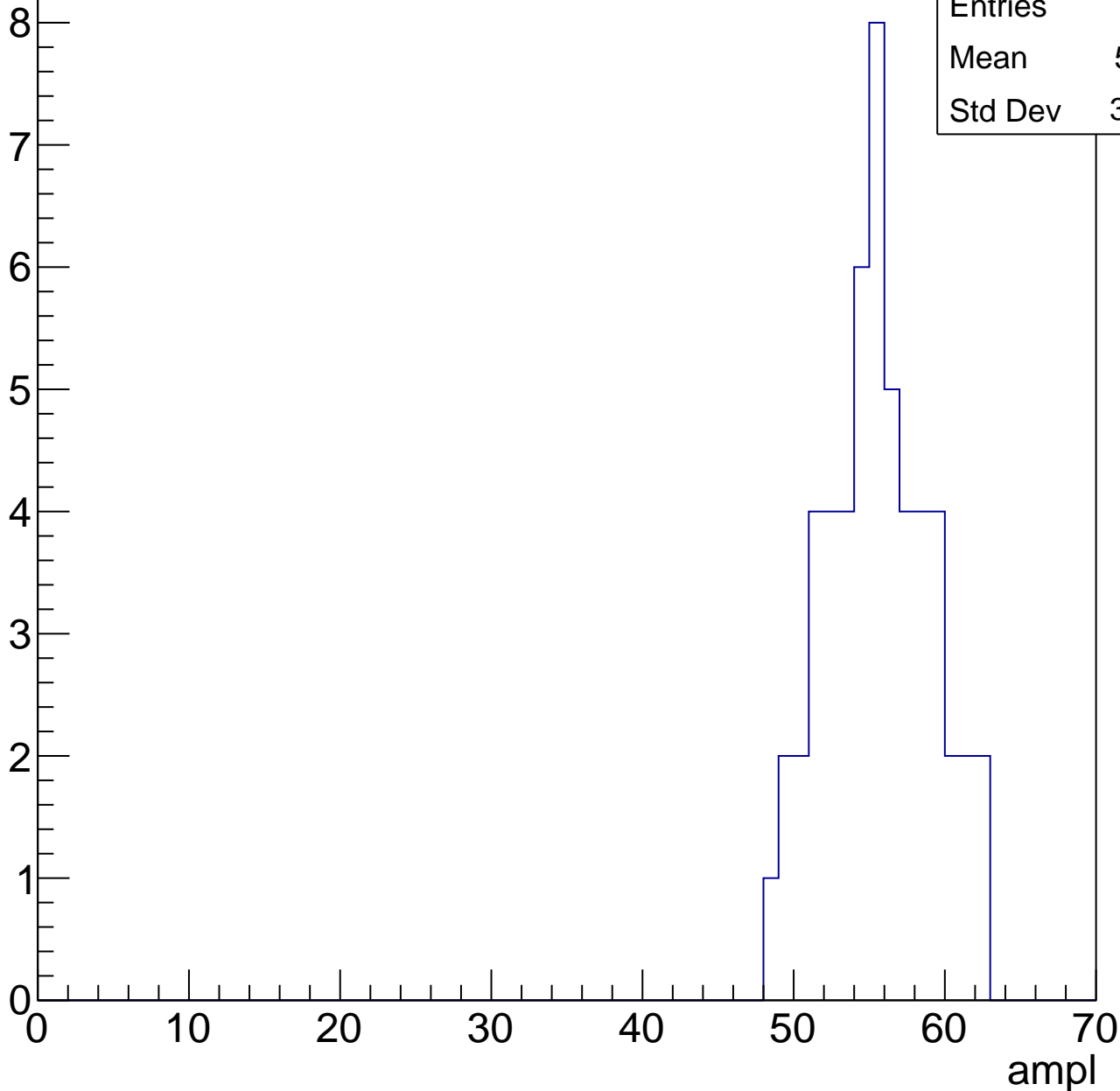


# B1L102S, U12-ch92, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

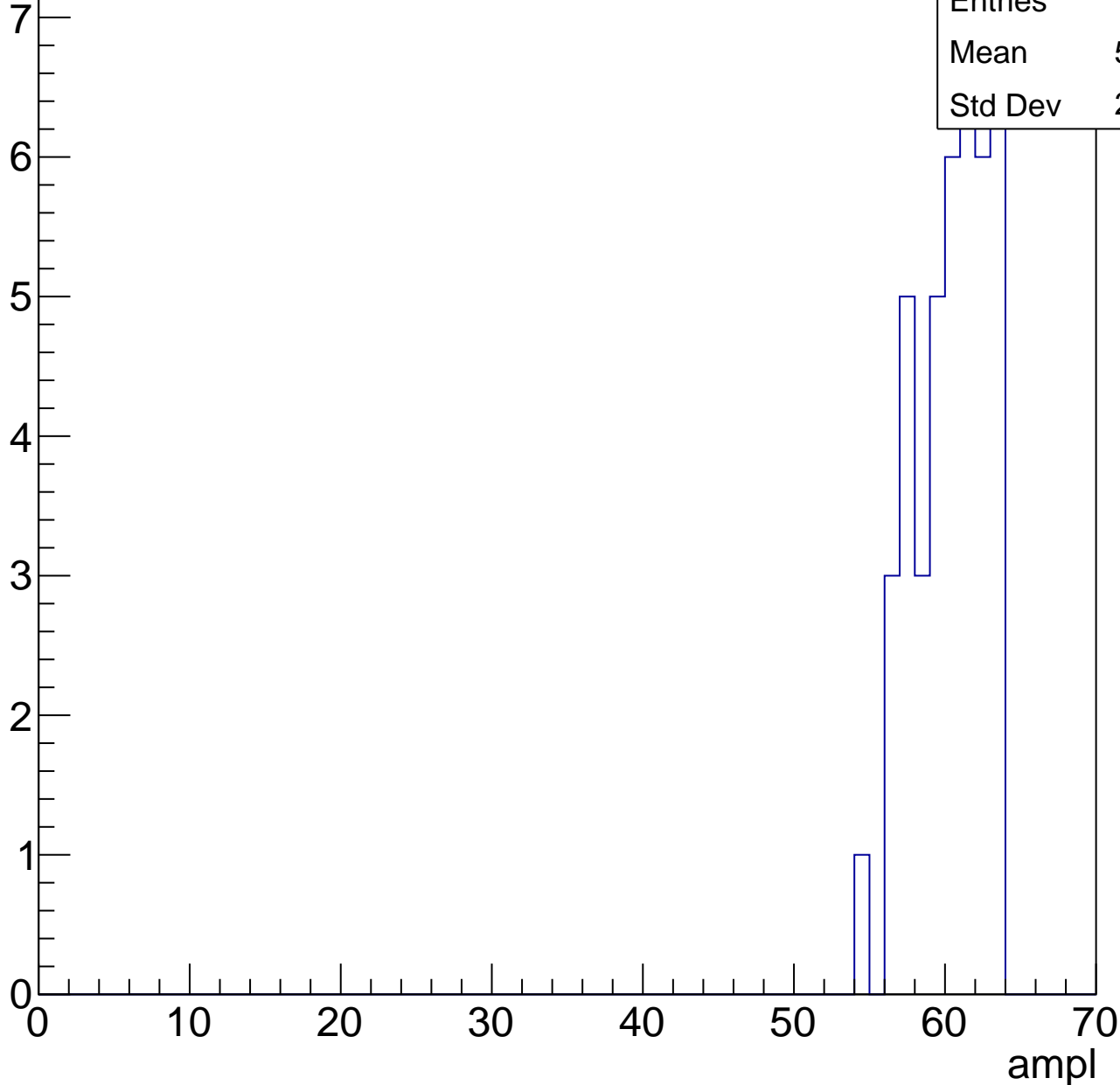
Entries	54
Mean	55.11
Std Dev	3.425



# B1L102S, U12-ch92, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U12-ch92, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

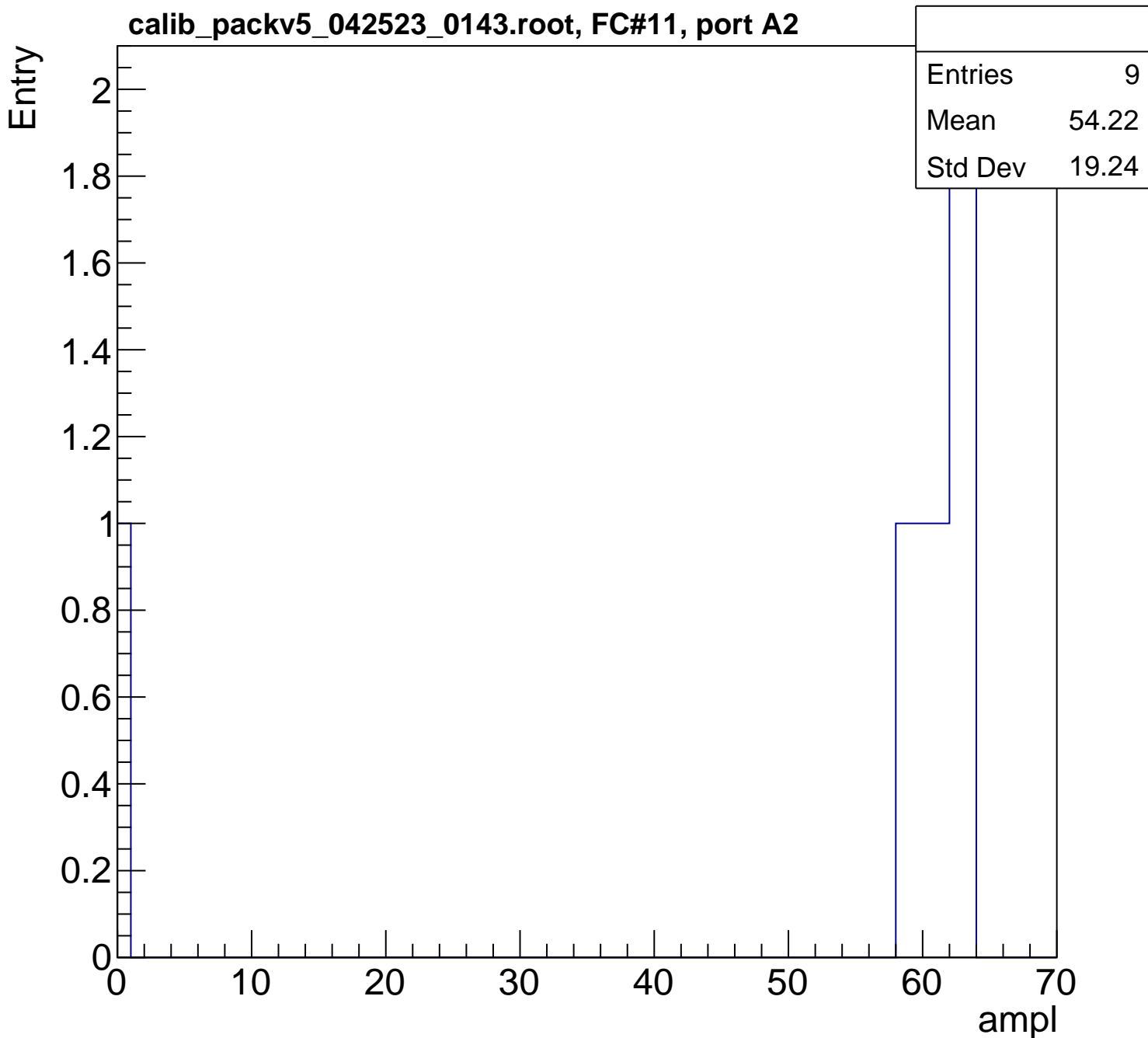
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	9
Mean	54.22
Std Dev	19.24

ampl

0 10 20 30 40 50 60 70





# B1L102S, U12-ch92, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U12-ch93, adc0

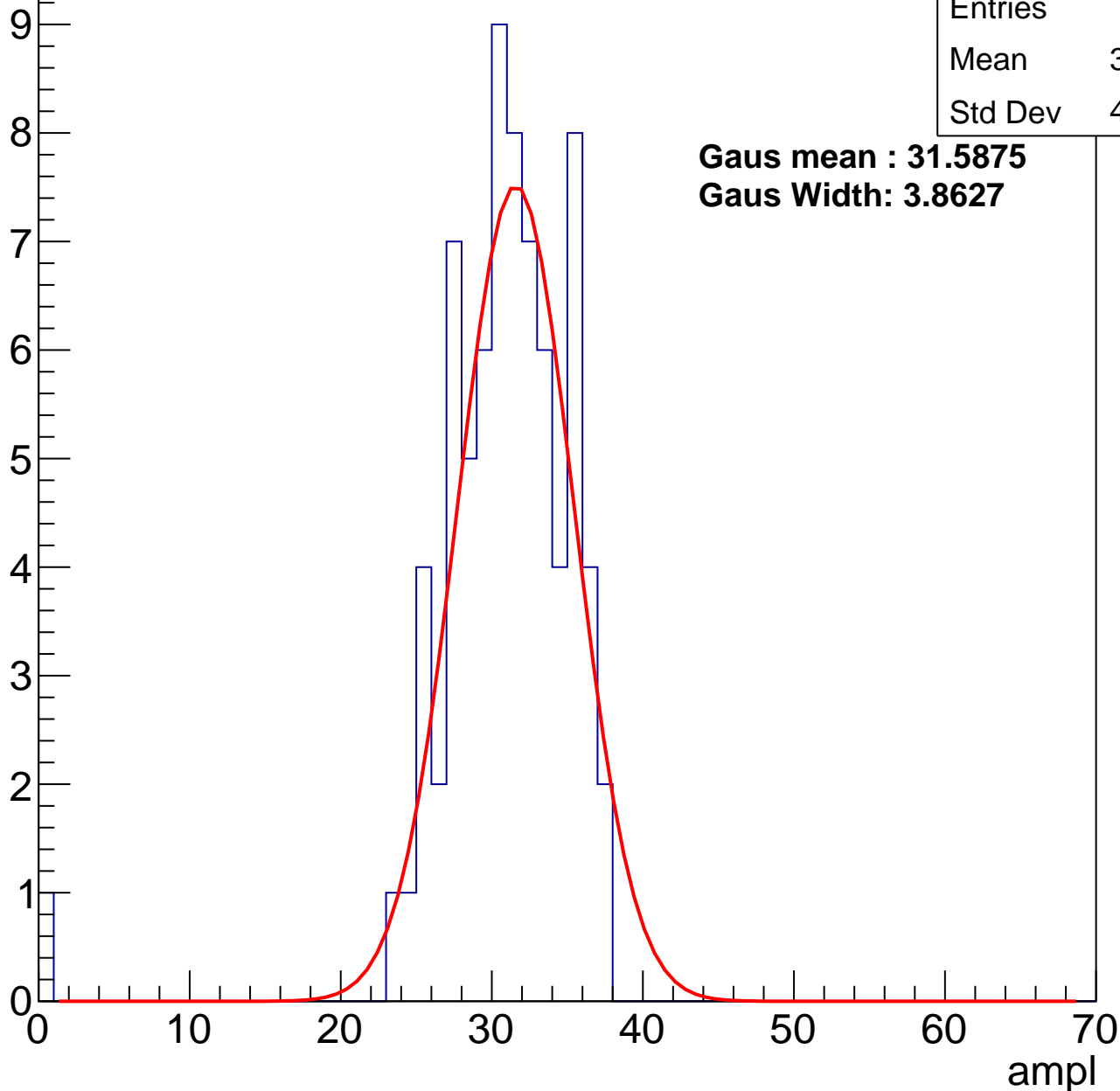
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	75
Mean	30.35
Std Dev	4.889

**Gaus mean : 31.5875**

**Gaus Width: 3.8627**



# B1L102S, U12-ch93, adc1

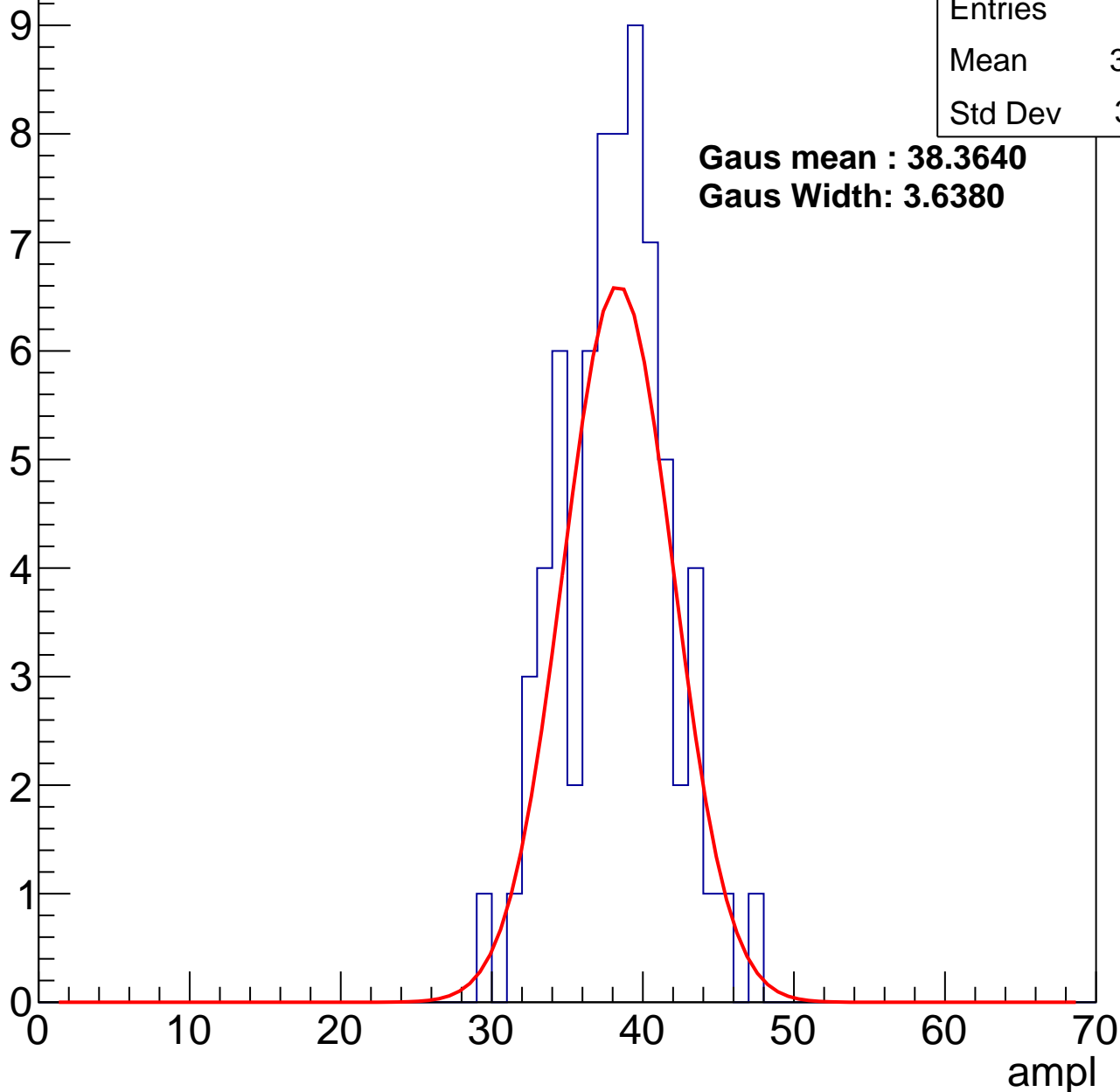
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	37.77
Std Dev	3.531

**Gaus mean : 38.3640**

**Gaus Width: 3.6380**



# B1L102S, U12-ch93, adc2

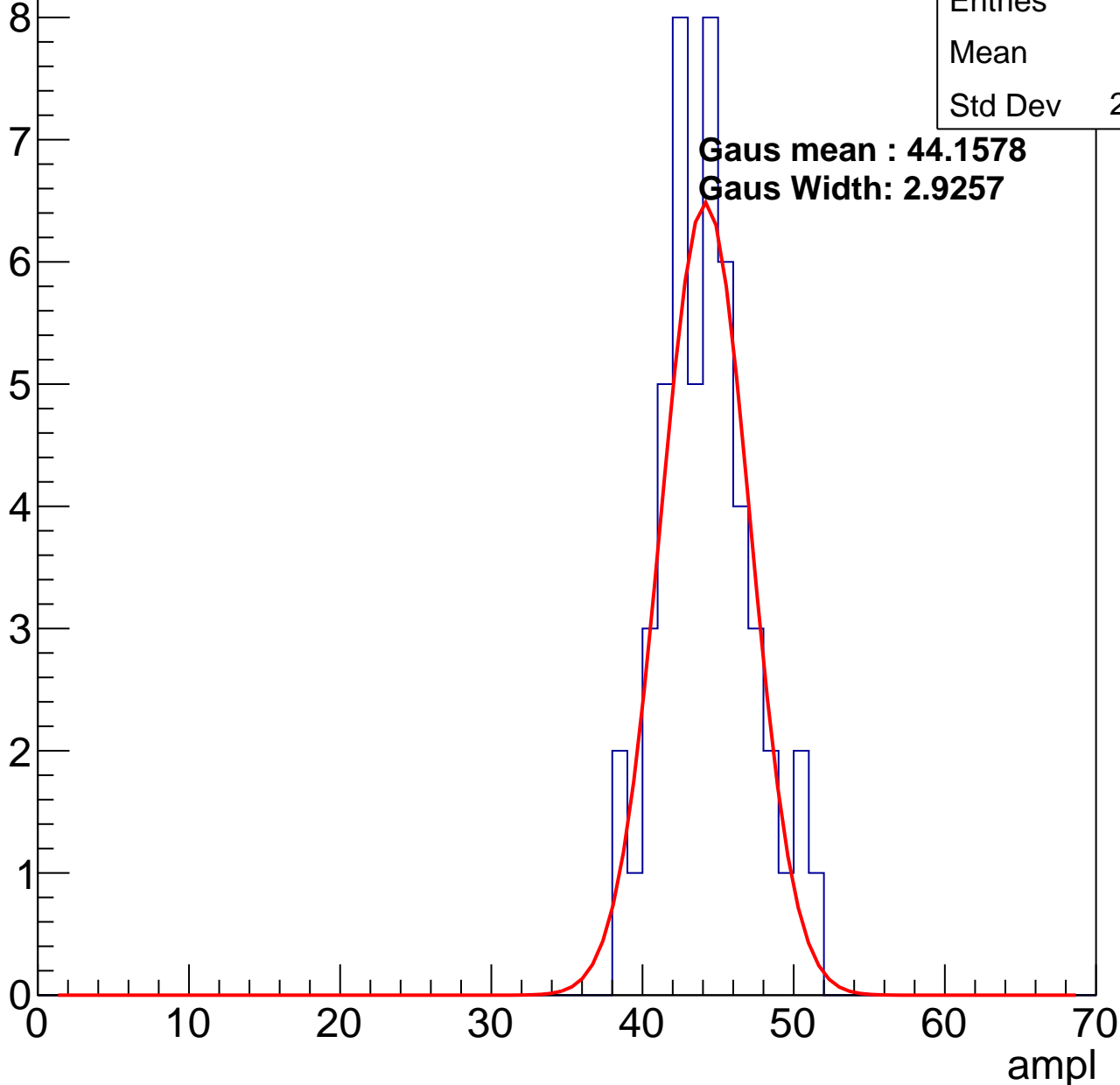
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	51
Mean	43.8
Std Dev	2.977

**Gaus mean : 44.1578**

**Gaus Width: 2.9257**

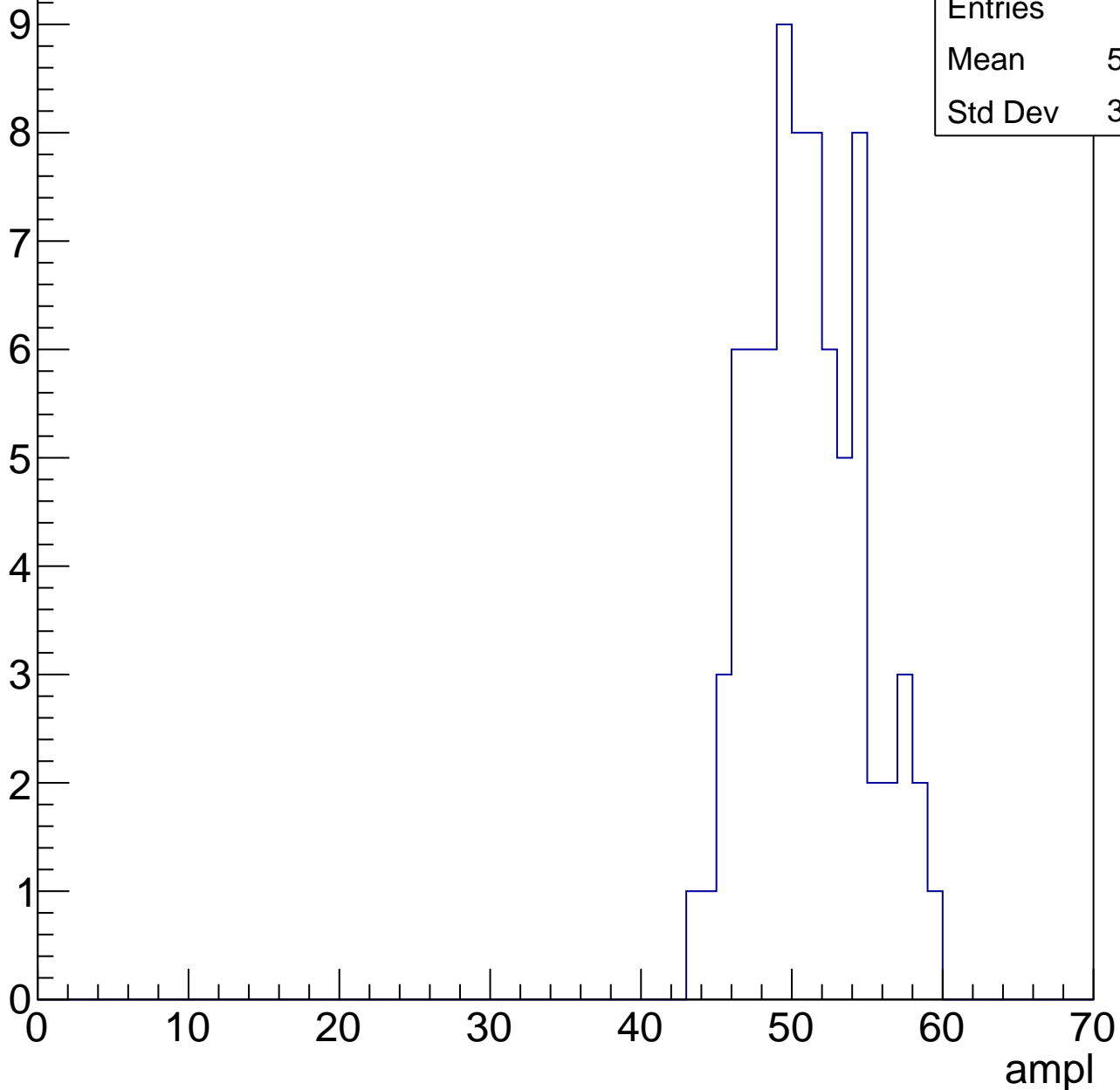


# B1L102S, U12-ch93, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	77
Mean	50.57
Std Dev	3.605

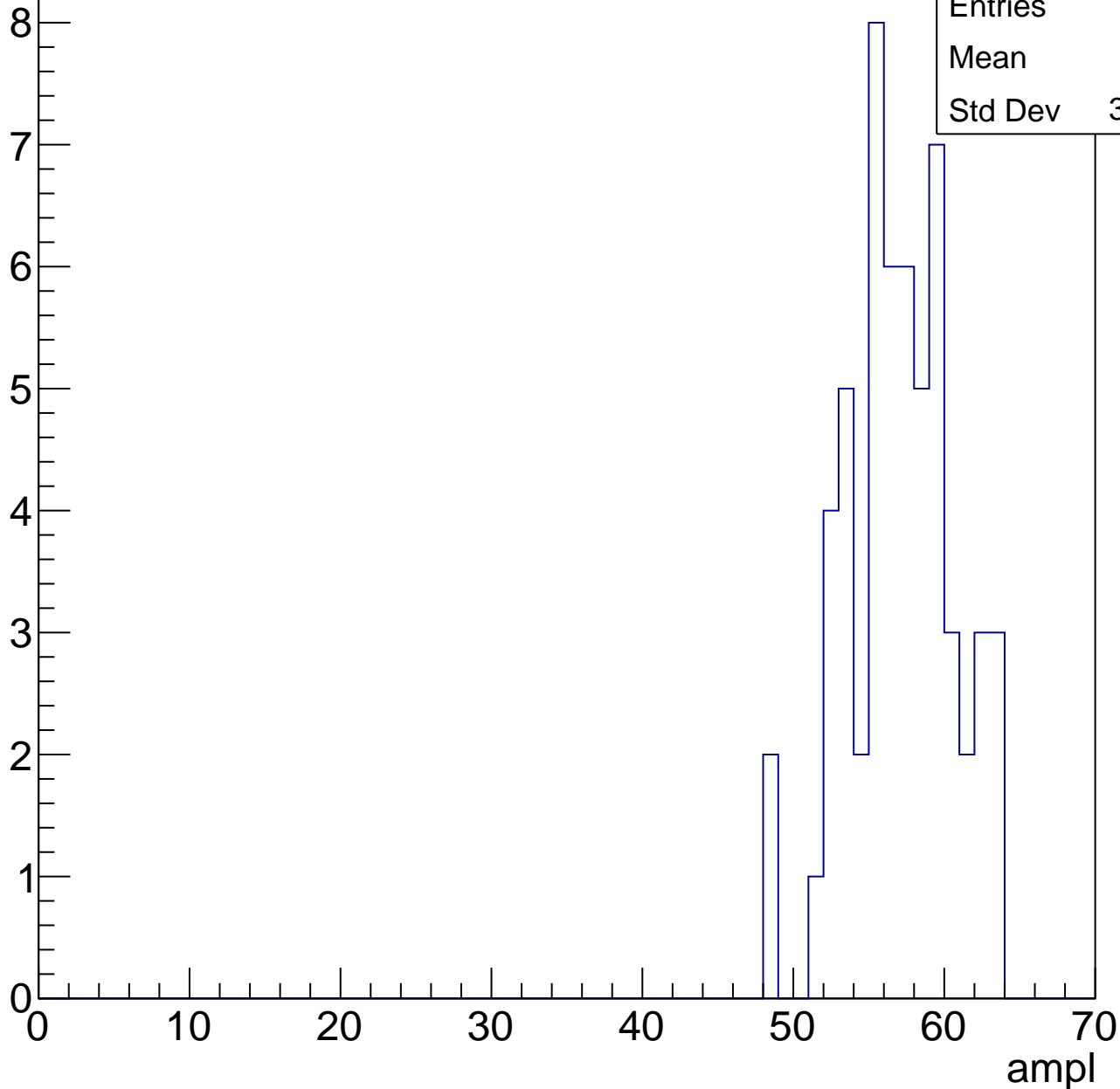


# B1L102S, U12-ch93, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

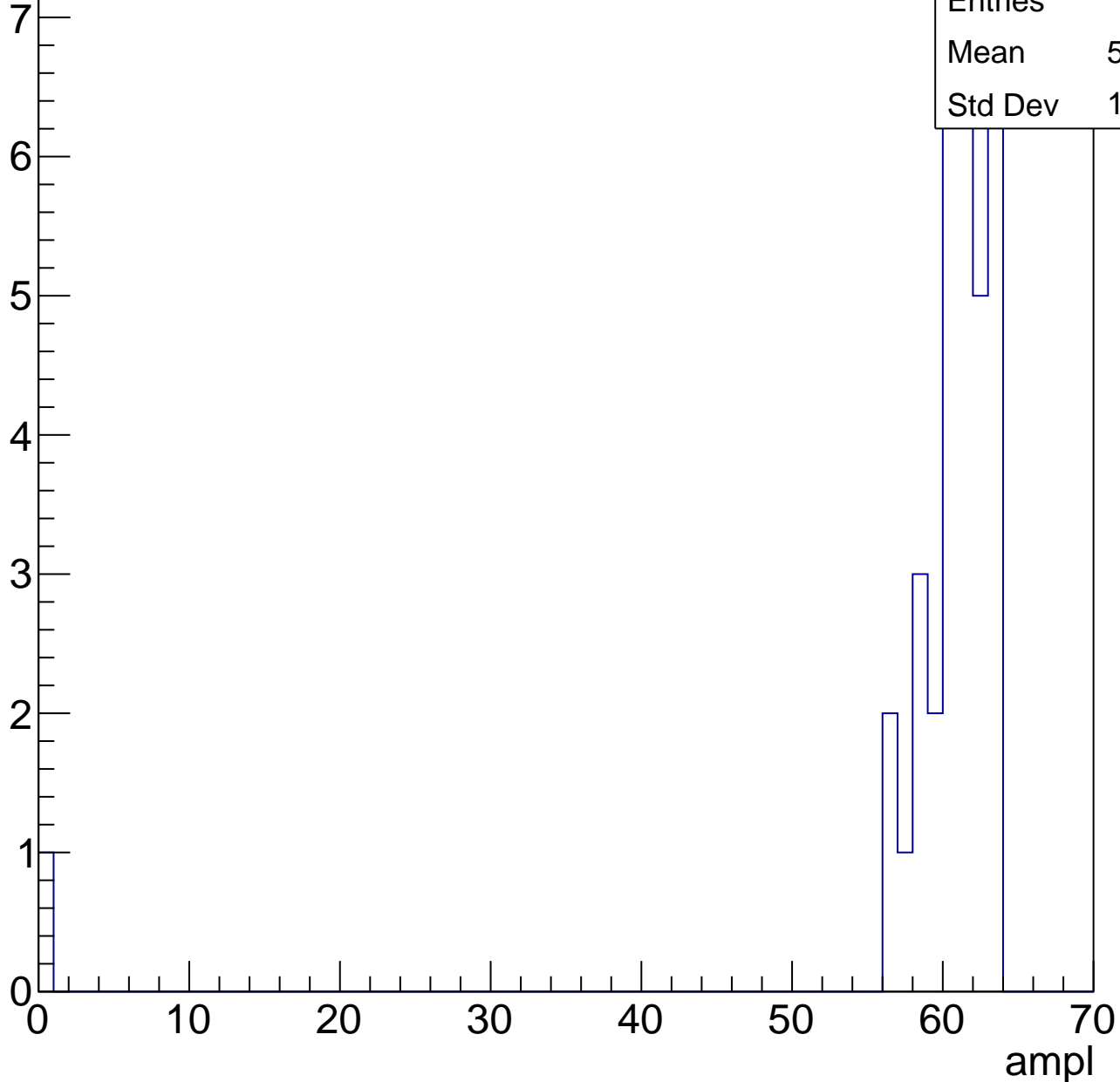
Entries	57
Mean	56.6
Std Dev	3.504



# B1L102S, U12-ch93, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U12-ch93, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	3
Mean	61.67
Std Dev	0.4714

ampl

0 10 20 30 40 50 60 70



# B1L102S, U12-ch93, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U12-ch94, adc0

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	73
Mean	28.3
Std Dev	5.865

**Gaus mean : 29.2270**

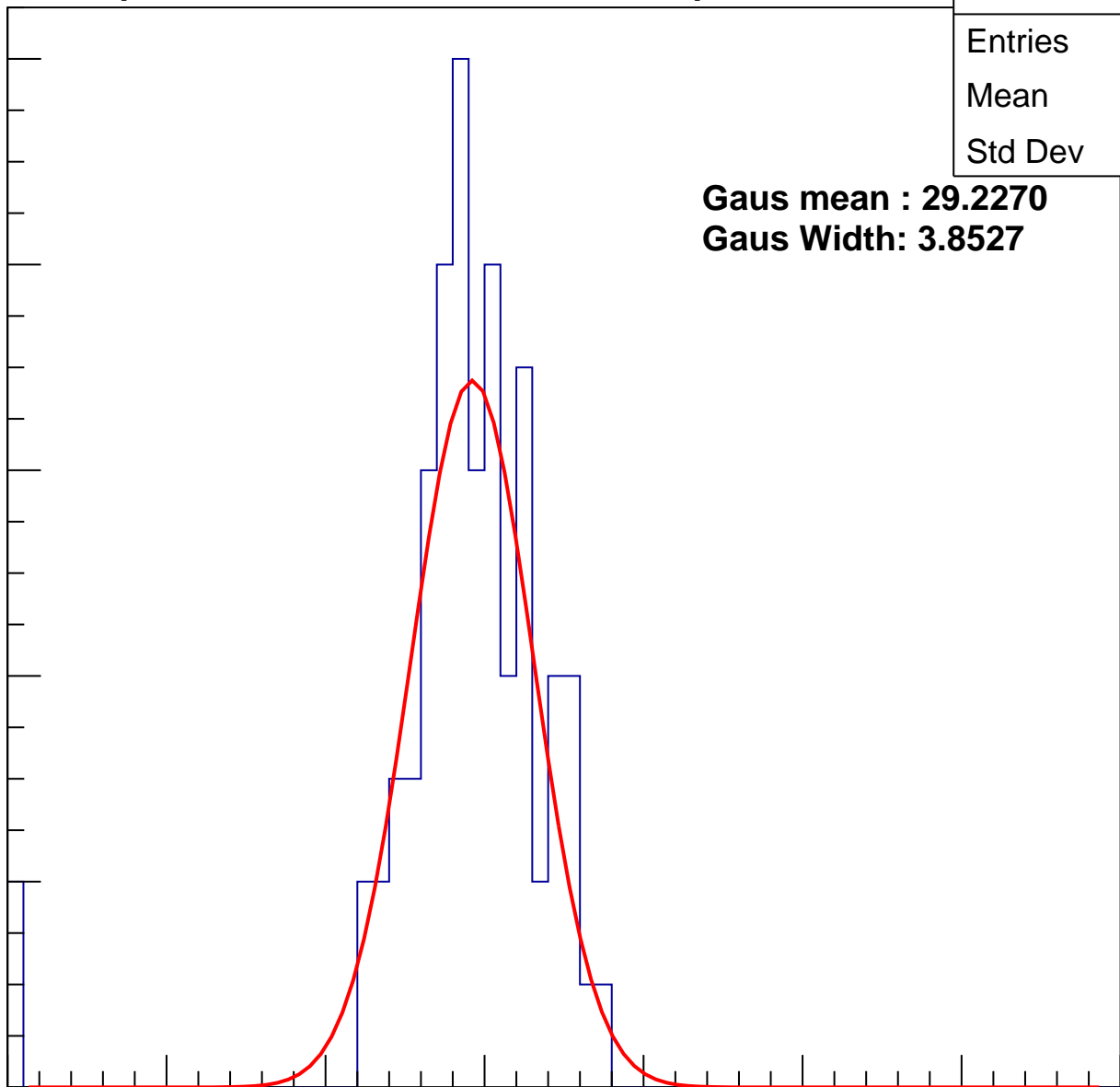
**Gaus Width: 3.8527**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



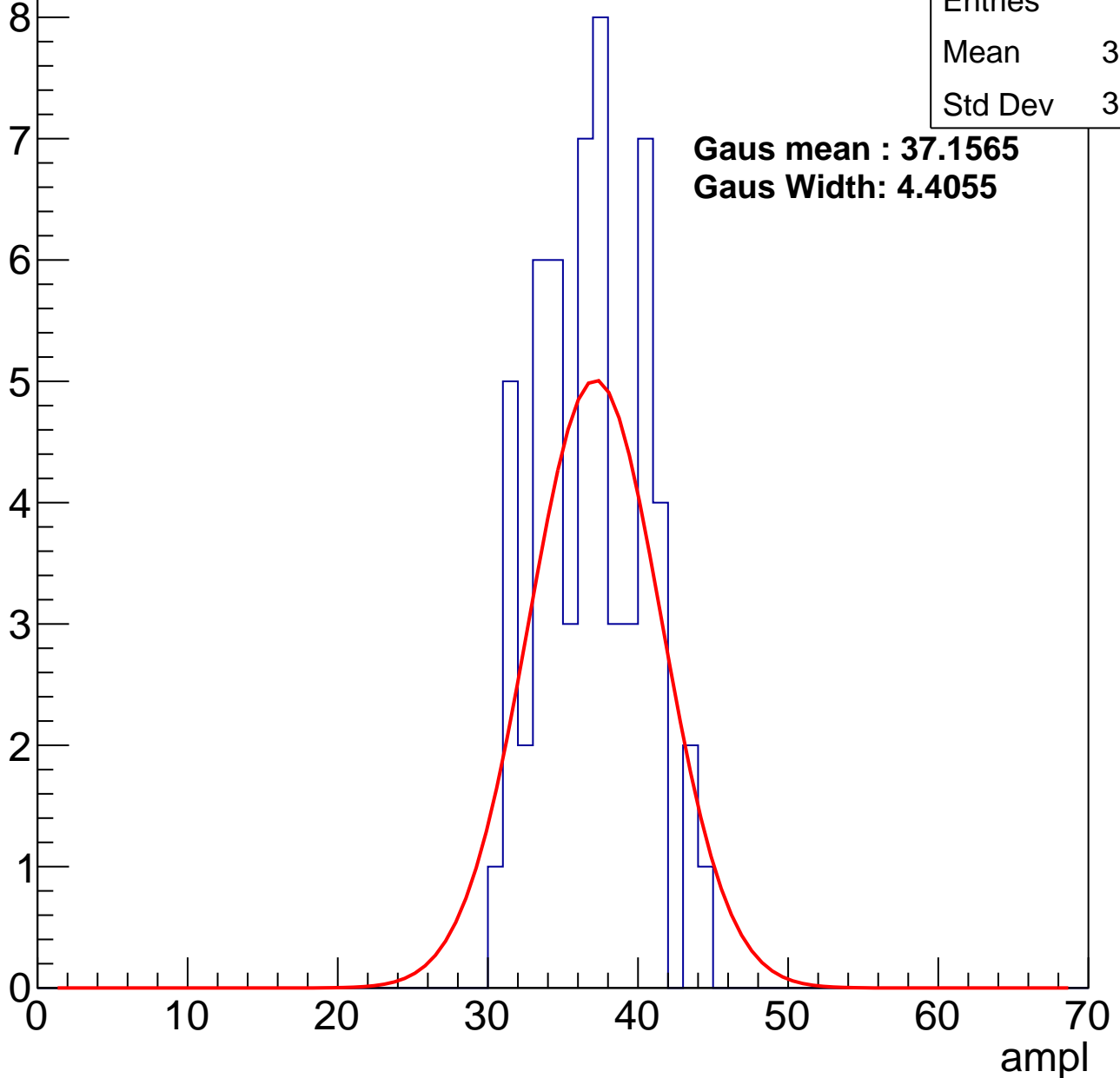
# B1L102S, U12-ch94, adc1

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	58
Mean	36.36
Std Dev	3.443

**Gaus mean : 37.1565**  
**Gaus Width: 4.4055**



# B1L102S, U12-ch94, adc2

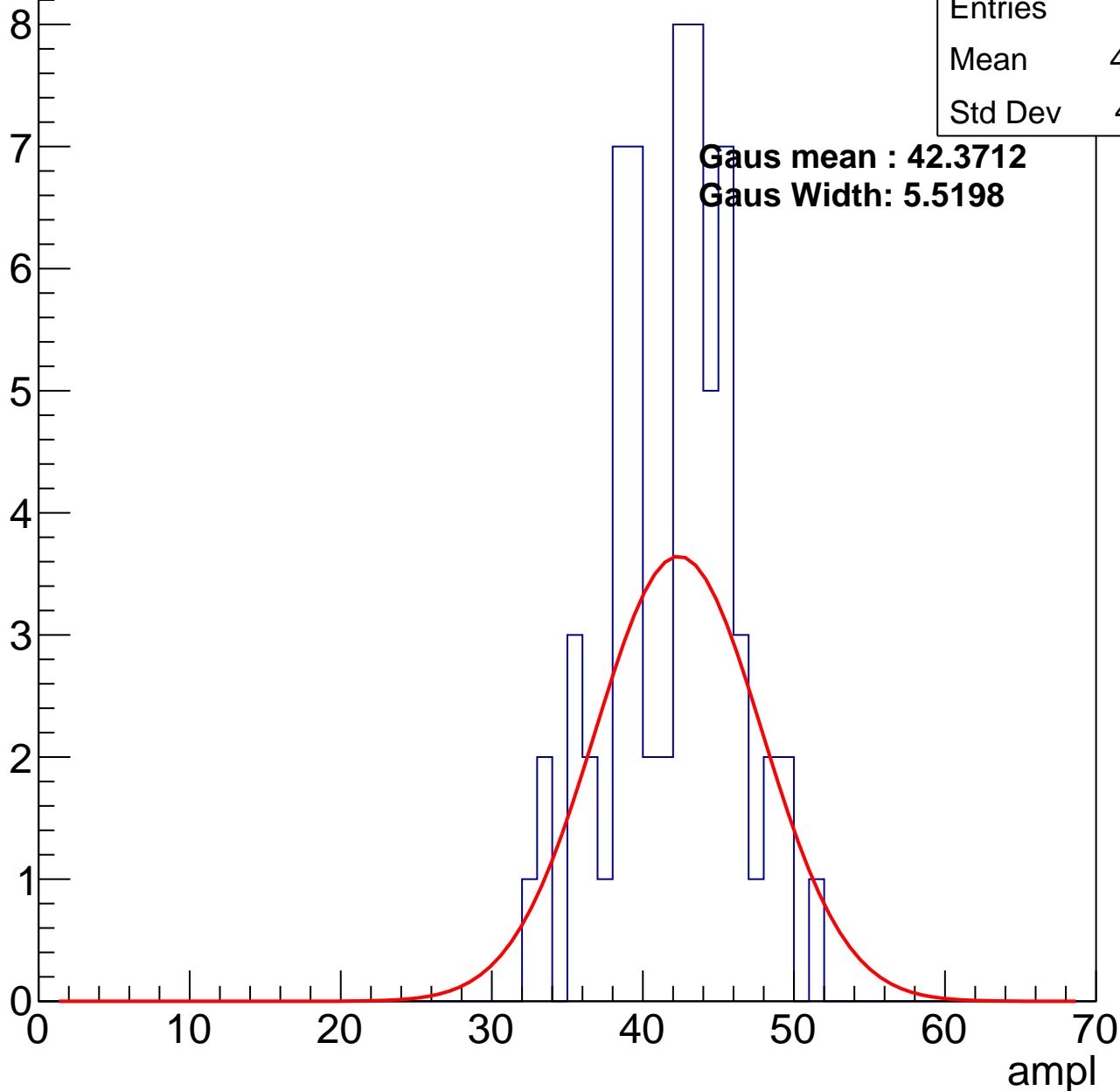
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	41.53
Std Dev	4.131

**Gaus mean : 42.3712**

**Gaus Width: 5.5198**

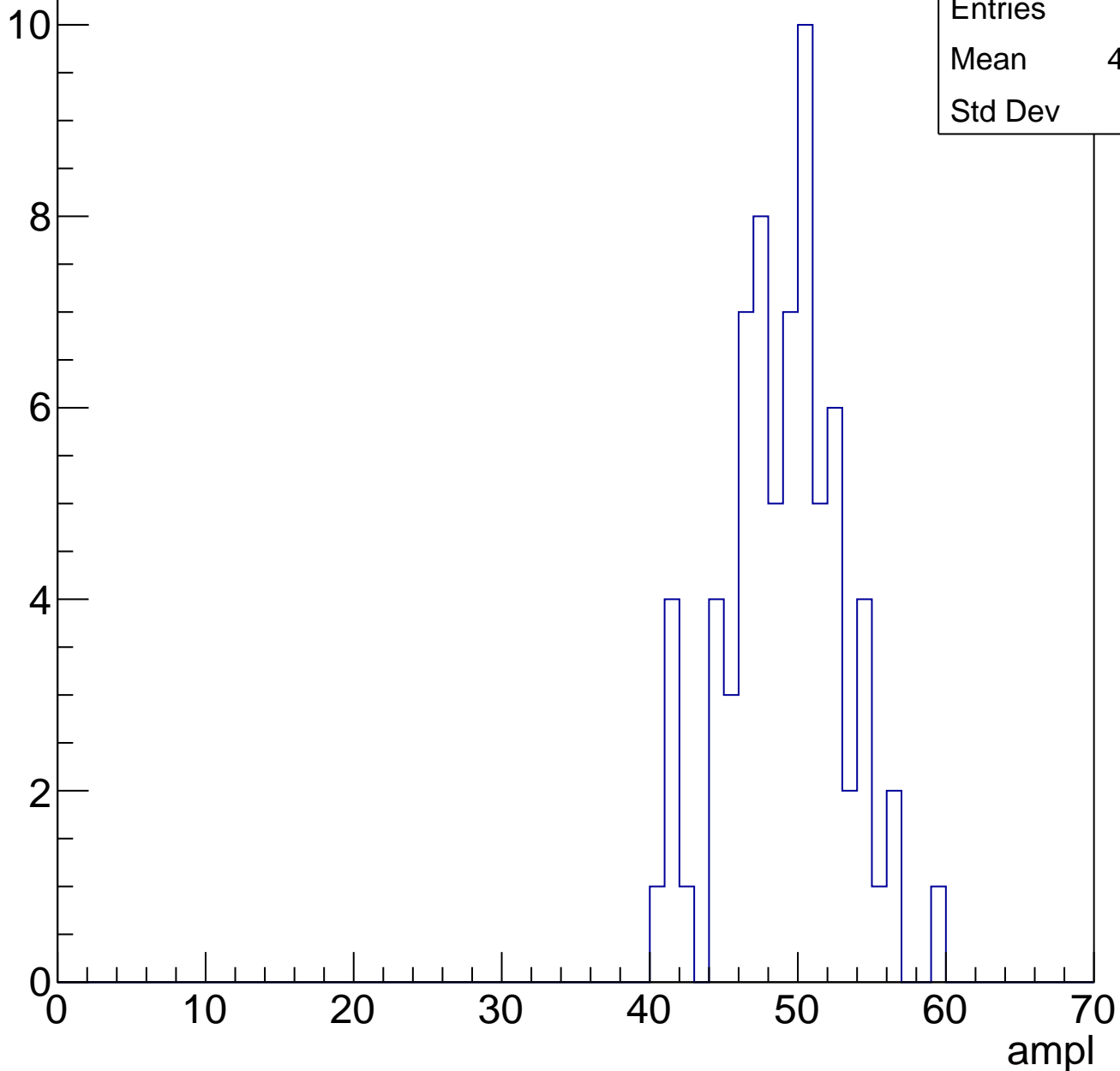


# B1L102S, U12-ch94, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

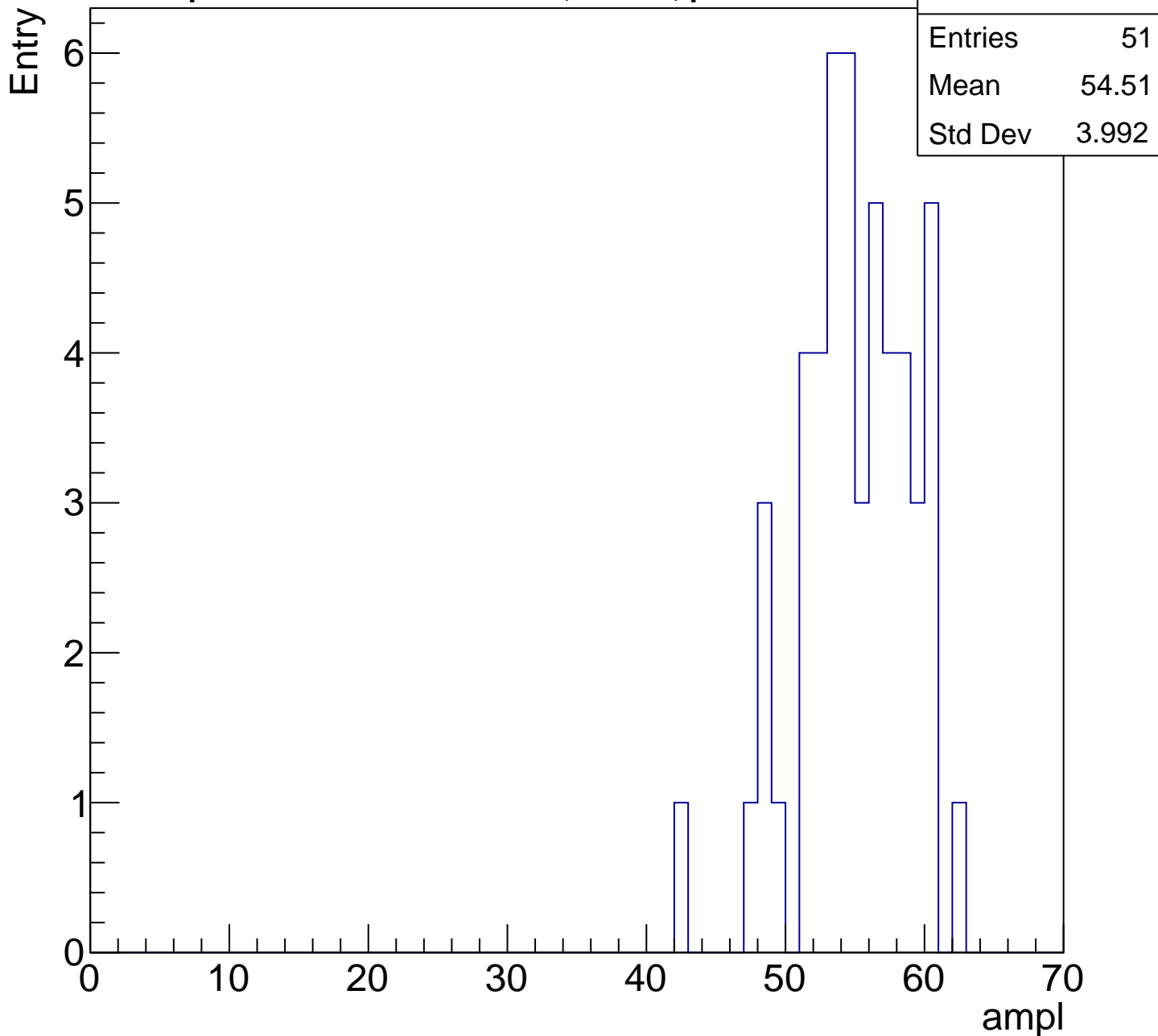
Entries	71
Mean	48.63
Std Dev	3.89

Entry



# B1L102S, U12-ch94, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2



# B1L102S, U12-ch94, adc5

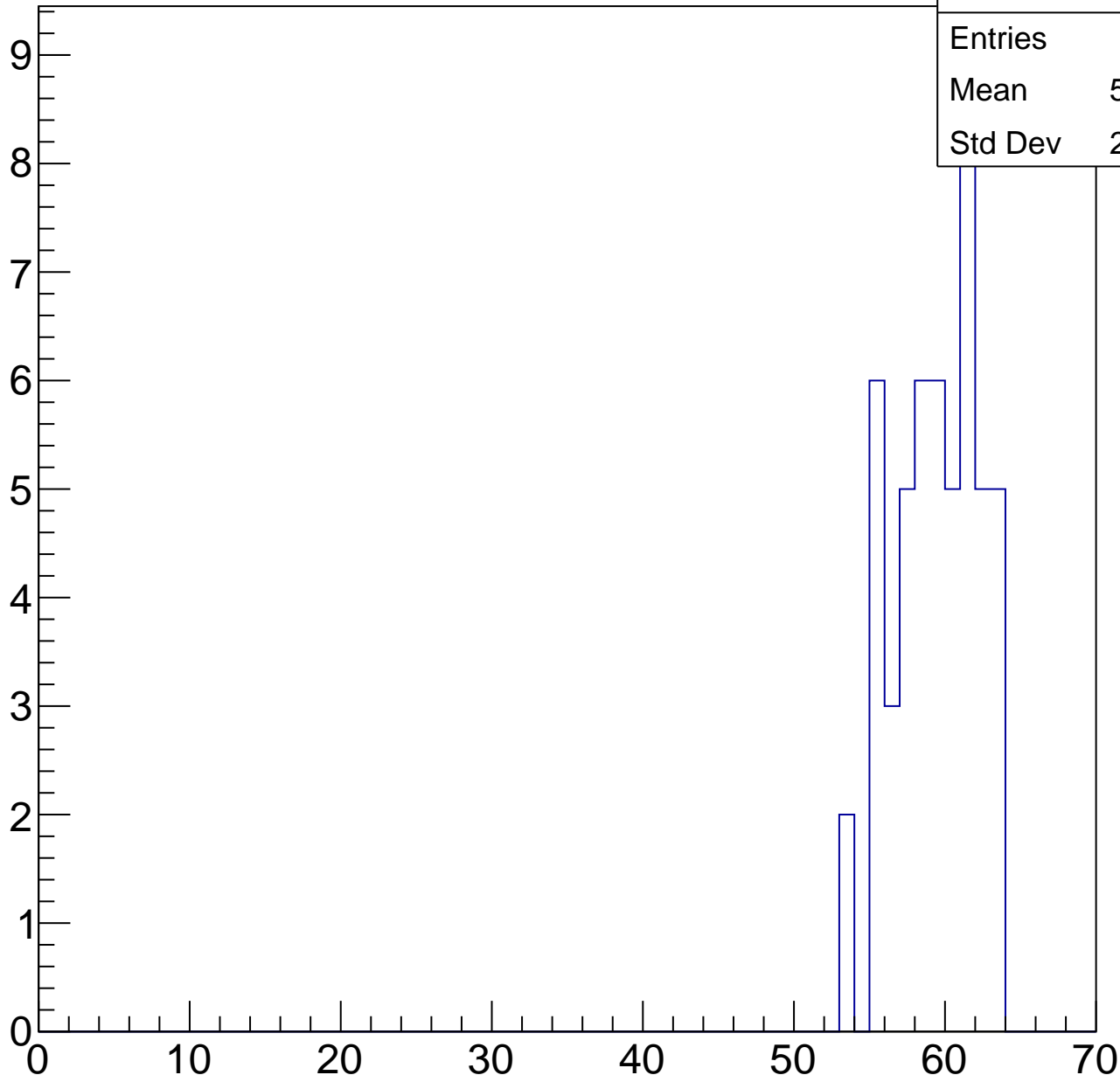
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	52
Mean	58.94
Std Dev	2.727

ampl

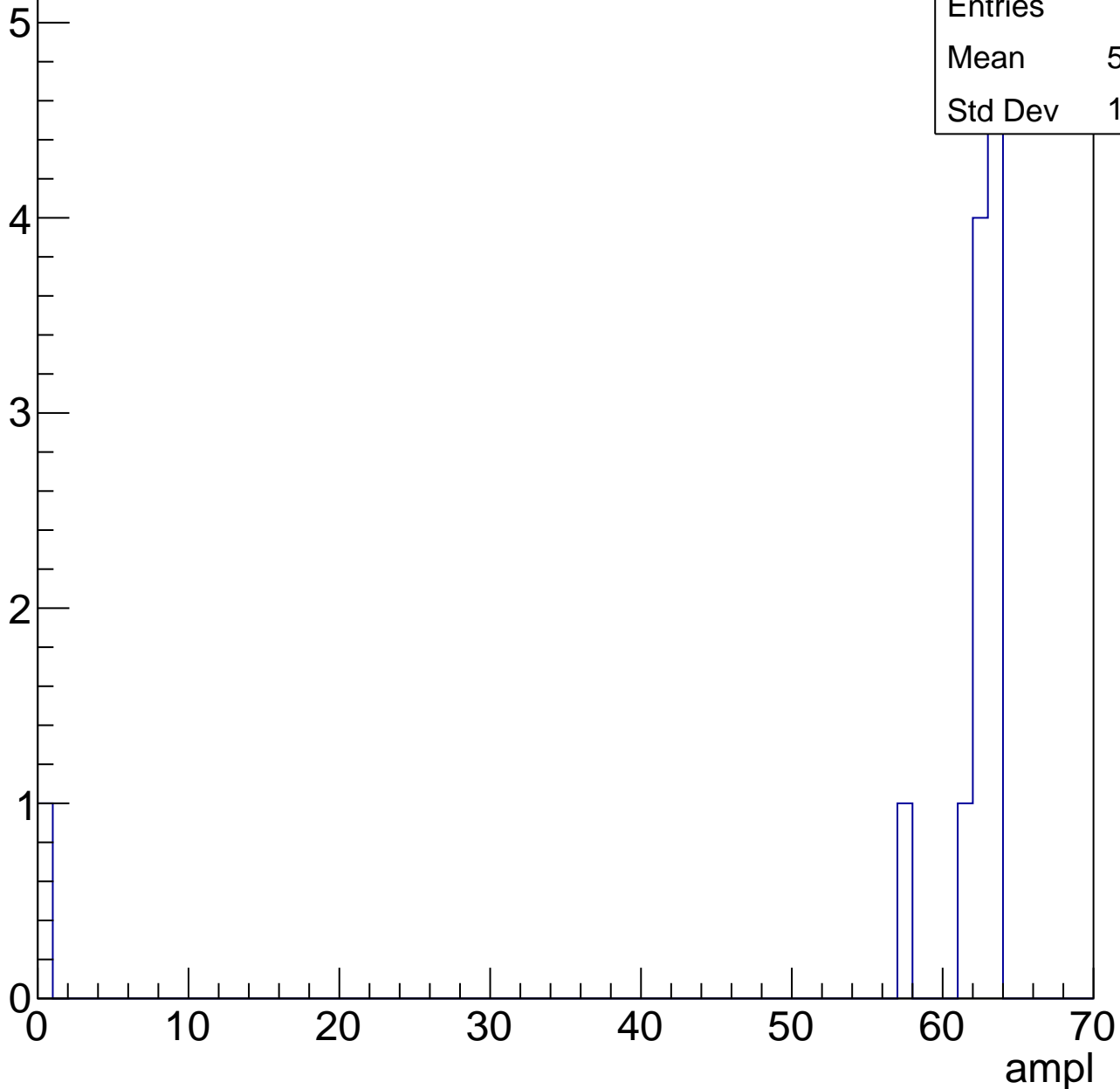


# B1L102S, U12-ch94, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	12
Mean	56.75
Std Dev	17.19





# B1L102S, U12-ch94, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U12-ch95, adc0

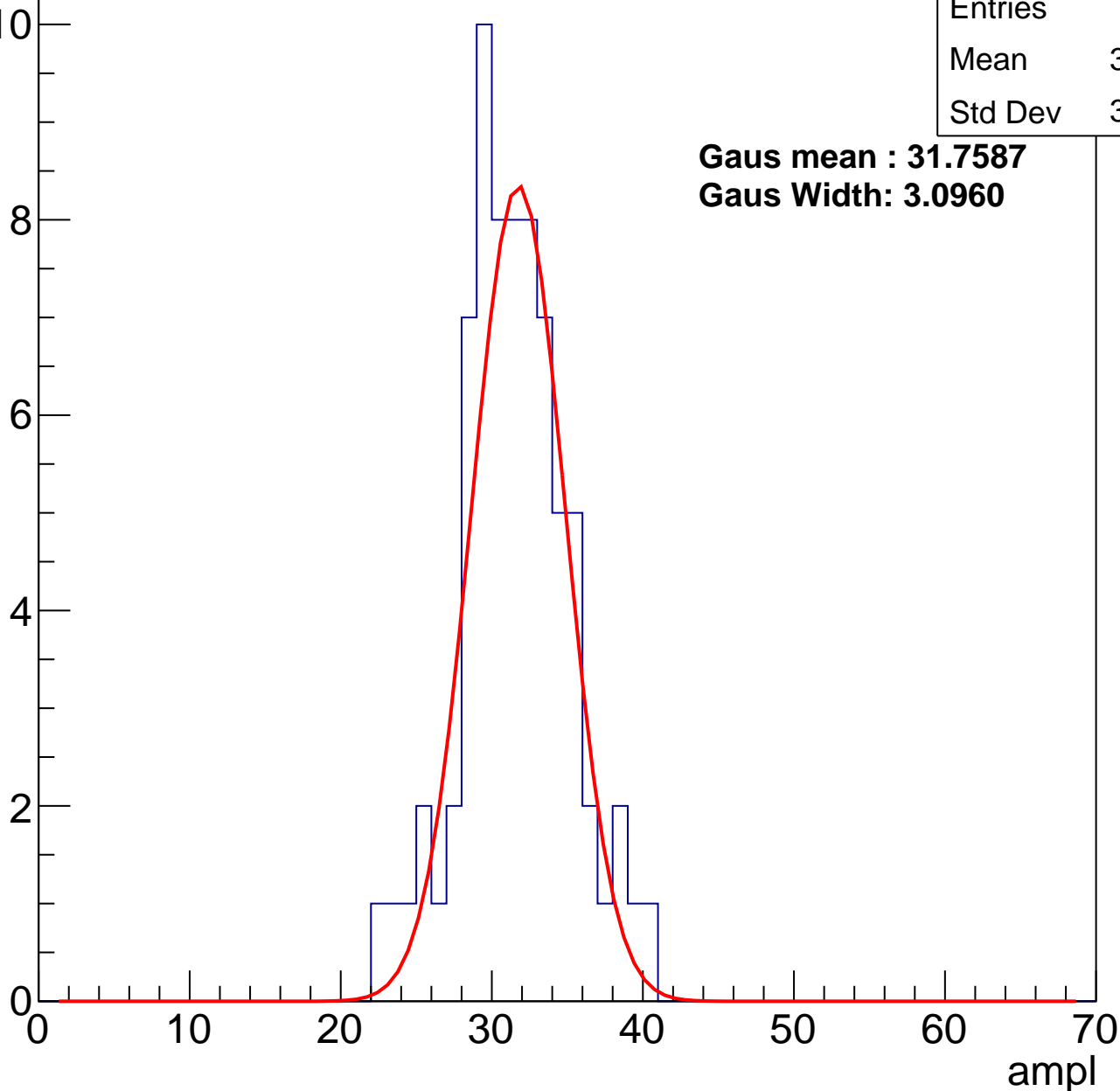
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	73
Mean	31.08
Std Dev	3.557

**Gaus mean : 31.7587**

**Gaus Width: 3.0960**



# B1L102S, U12-ch95, adc1

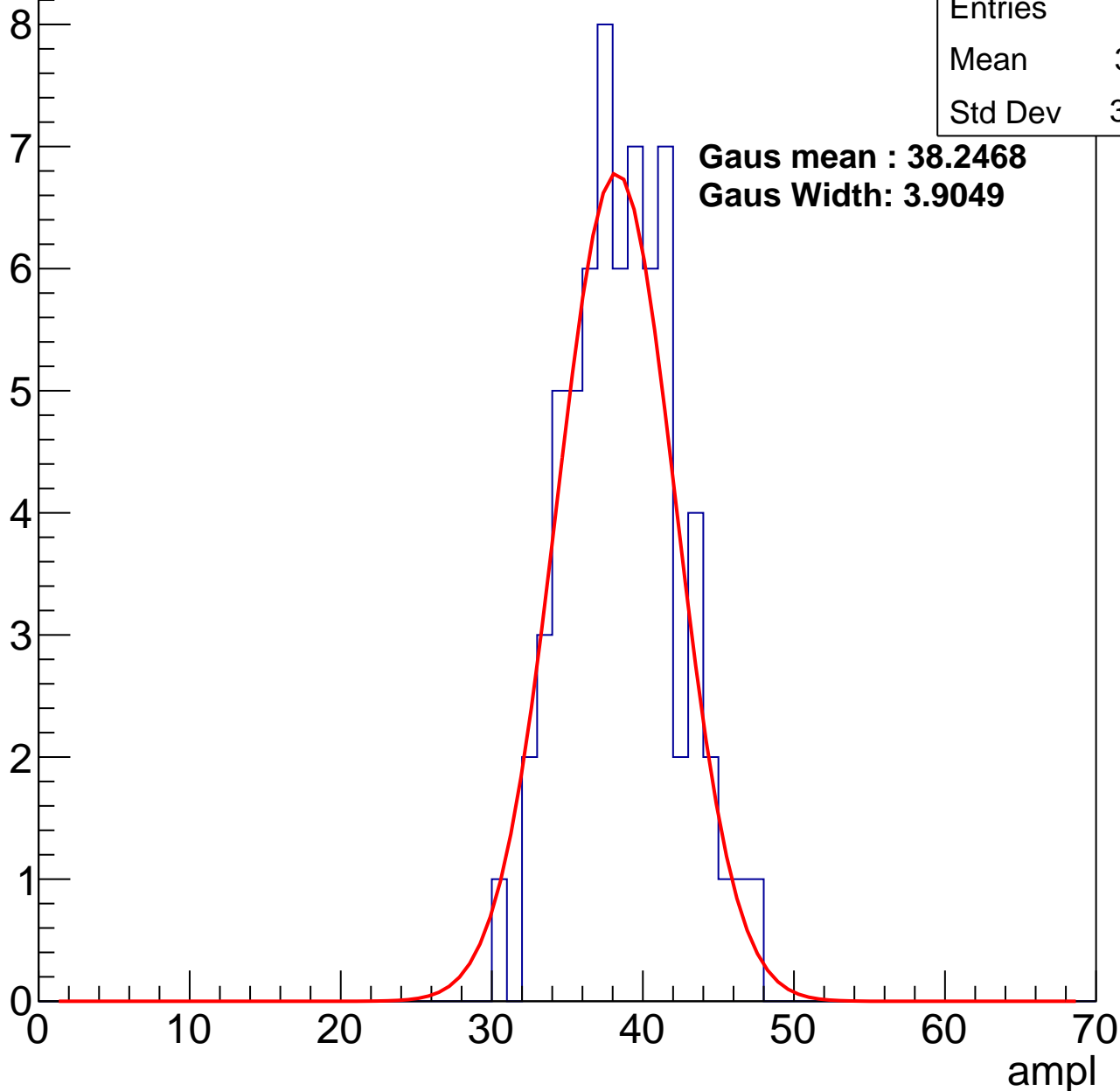
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	67
Mean	38.21
Std Dev	3.577

**Gaus mean : 38.2468**

**Gaus Width: 3.9049**



# B1L102S, U12-ch95, adc2

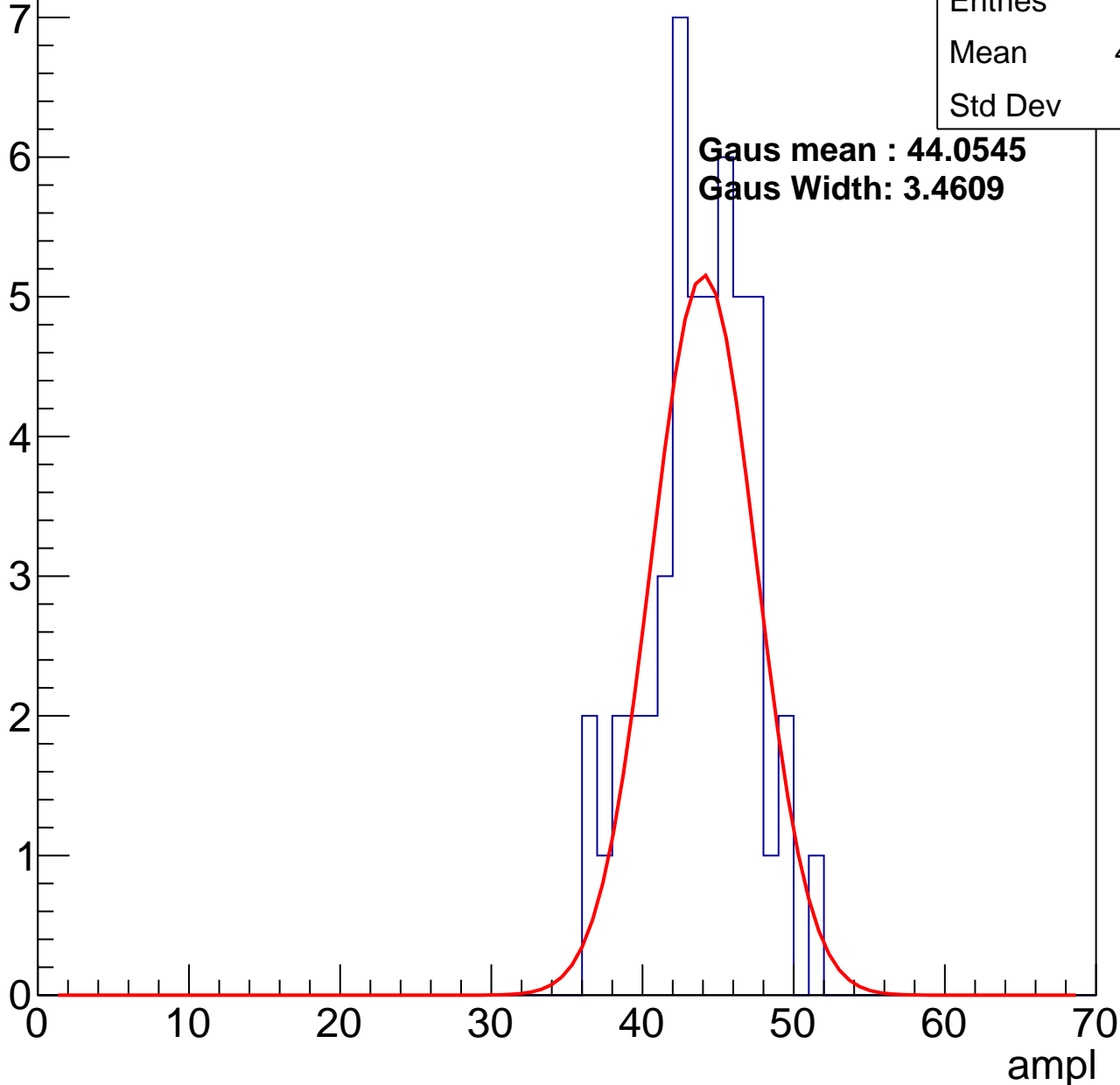
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	49
Mean	43.41
Std Dev	3.38

**Gaus mean : 44.0545**

**Gaus Width: 3.4609**



# B1L102S, U12-ch95, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

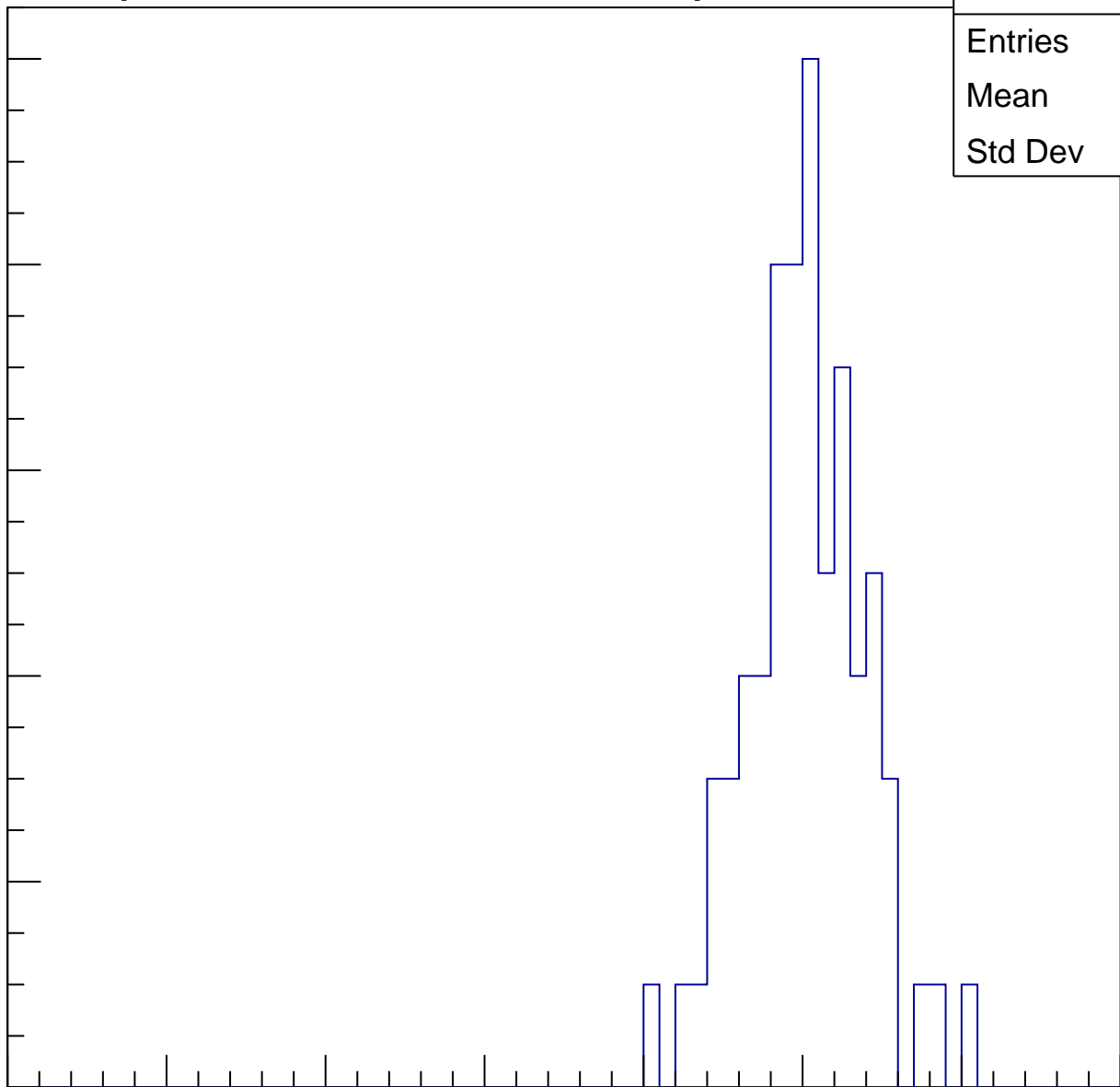
Entries	70
Mean	49.73
Std Dev	3.718

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

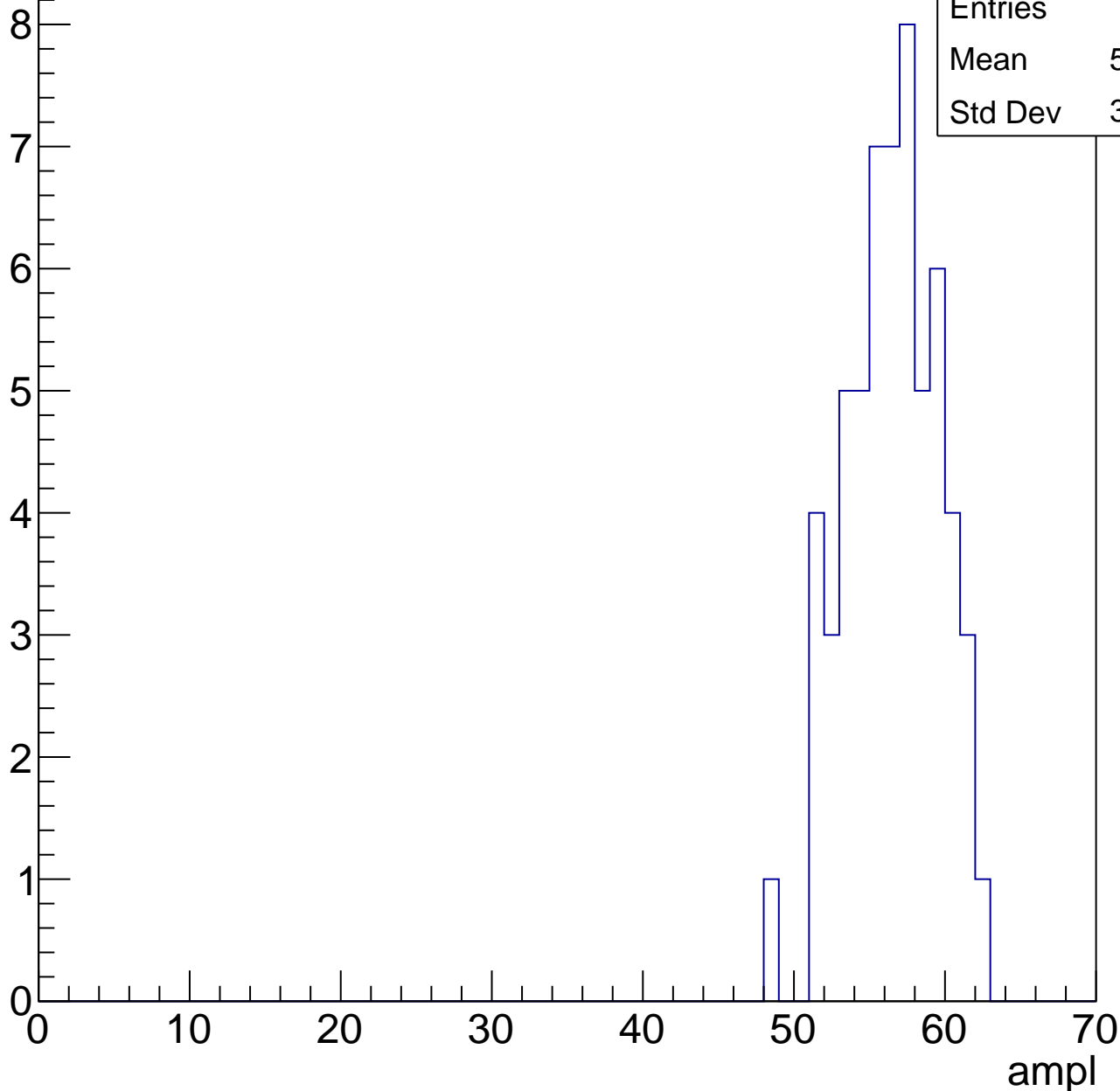


# B1L102S, U12-ch95, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	59
Mean	56.02
Std Dev	3.028

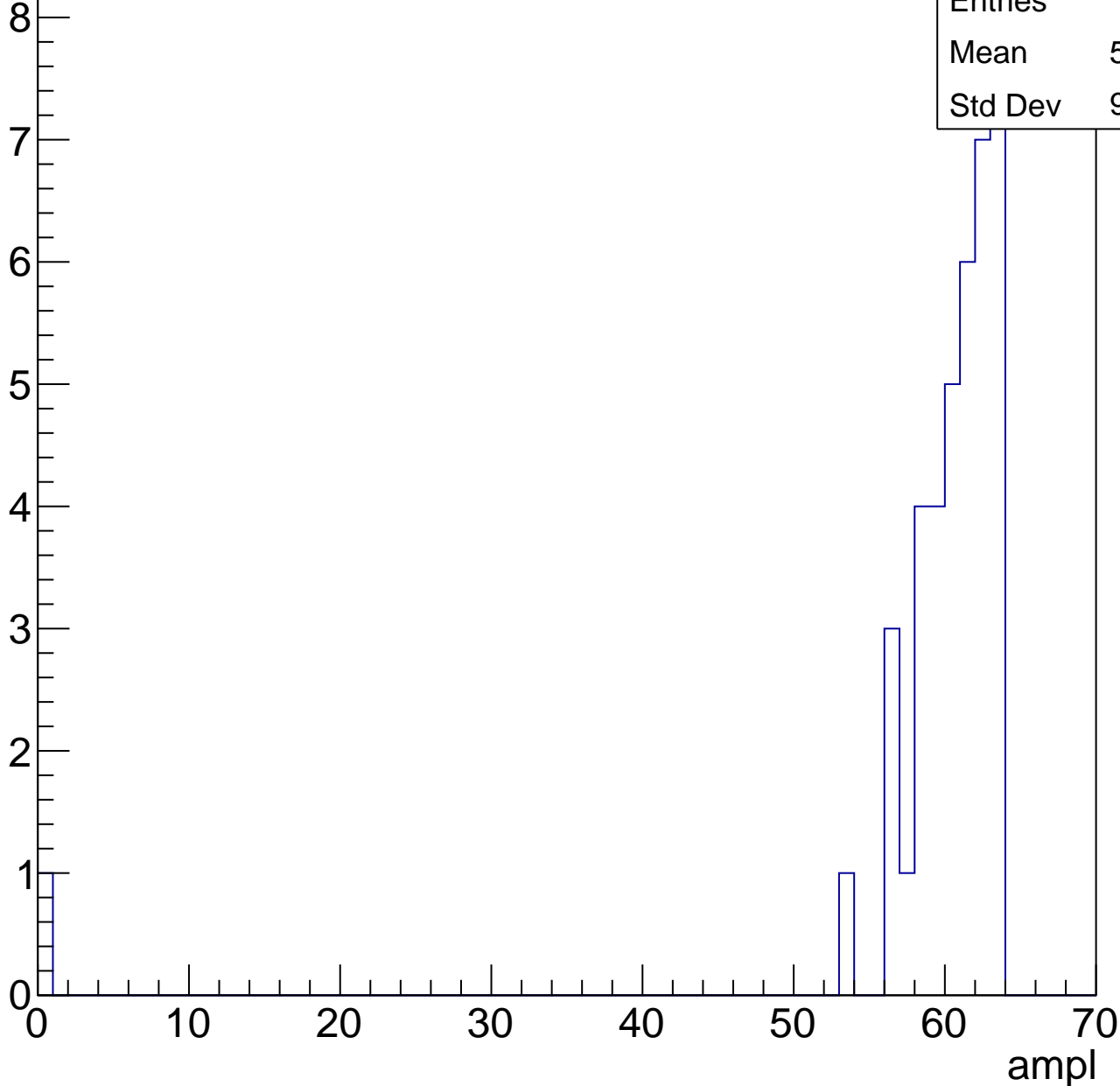


# B1L102S, U12-ch95, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	40
Mean	58.75
Std Dev	9.708



# B1L102S, U12-ch95, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U12-ch95, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U12-ch96, adc0

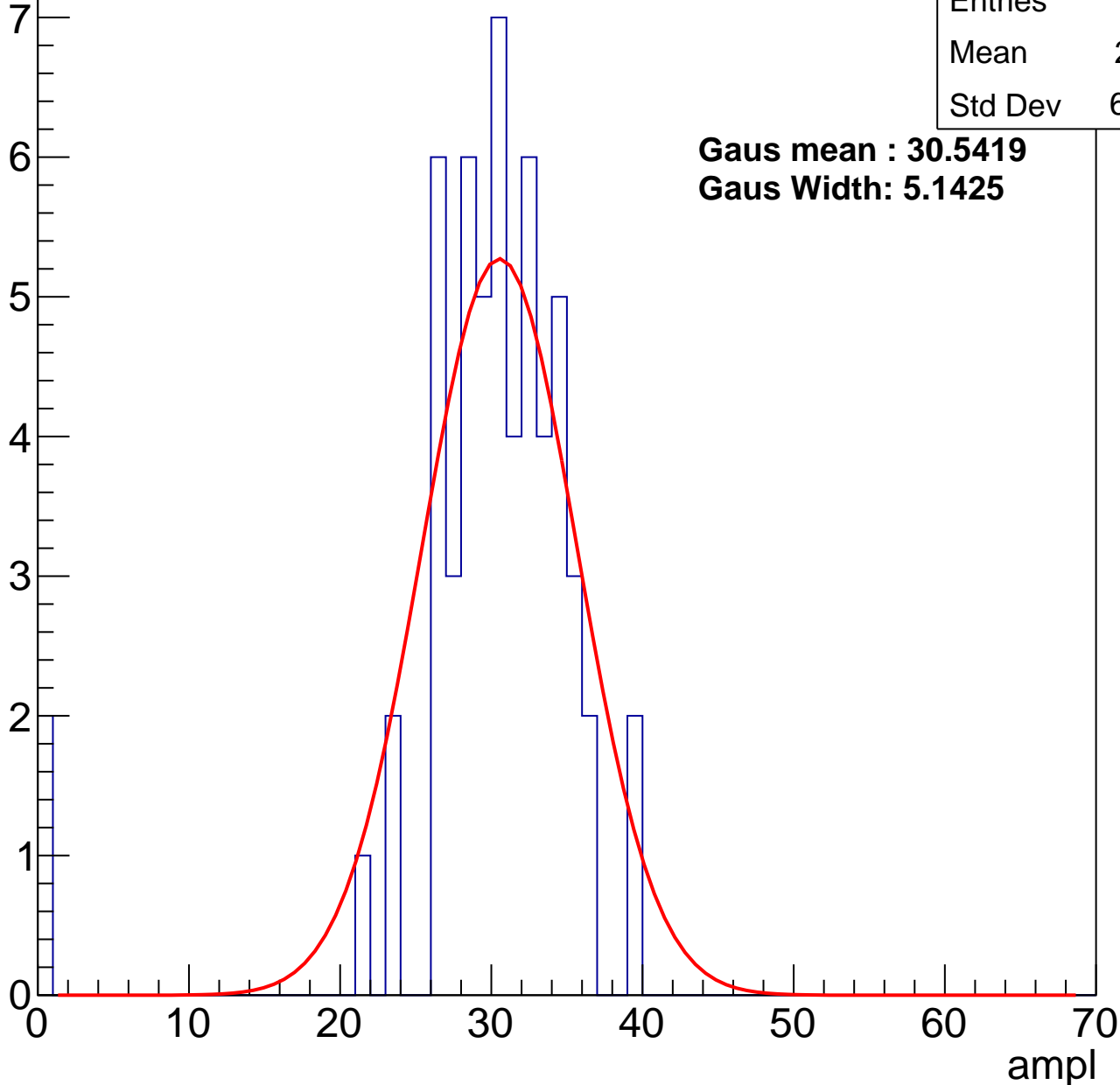
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	58
Mean	29.31
Std Dev	6.639

**Gaus mean : 30.5419**

**Gaus Width: 5.1425**



# B1L102S, U12-ch96, adc1

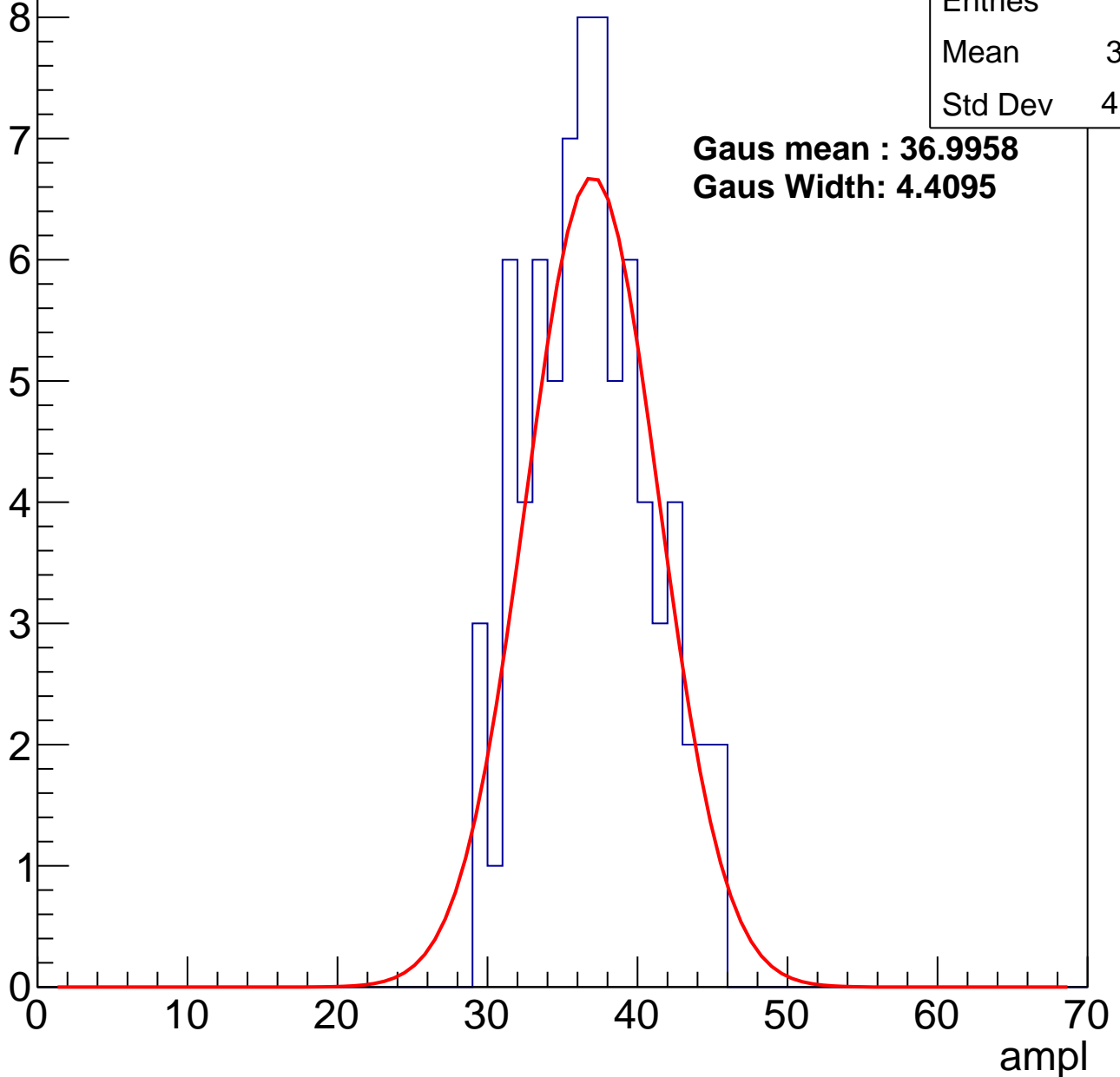
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	76
Mean	36.41
Std Dev	4.004

**Gaus mean : 36.9958**

**Gaus Width: 4.4095**



# B1L102S, U12-ch96, adc2

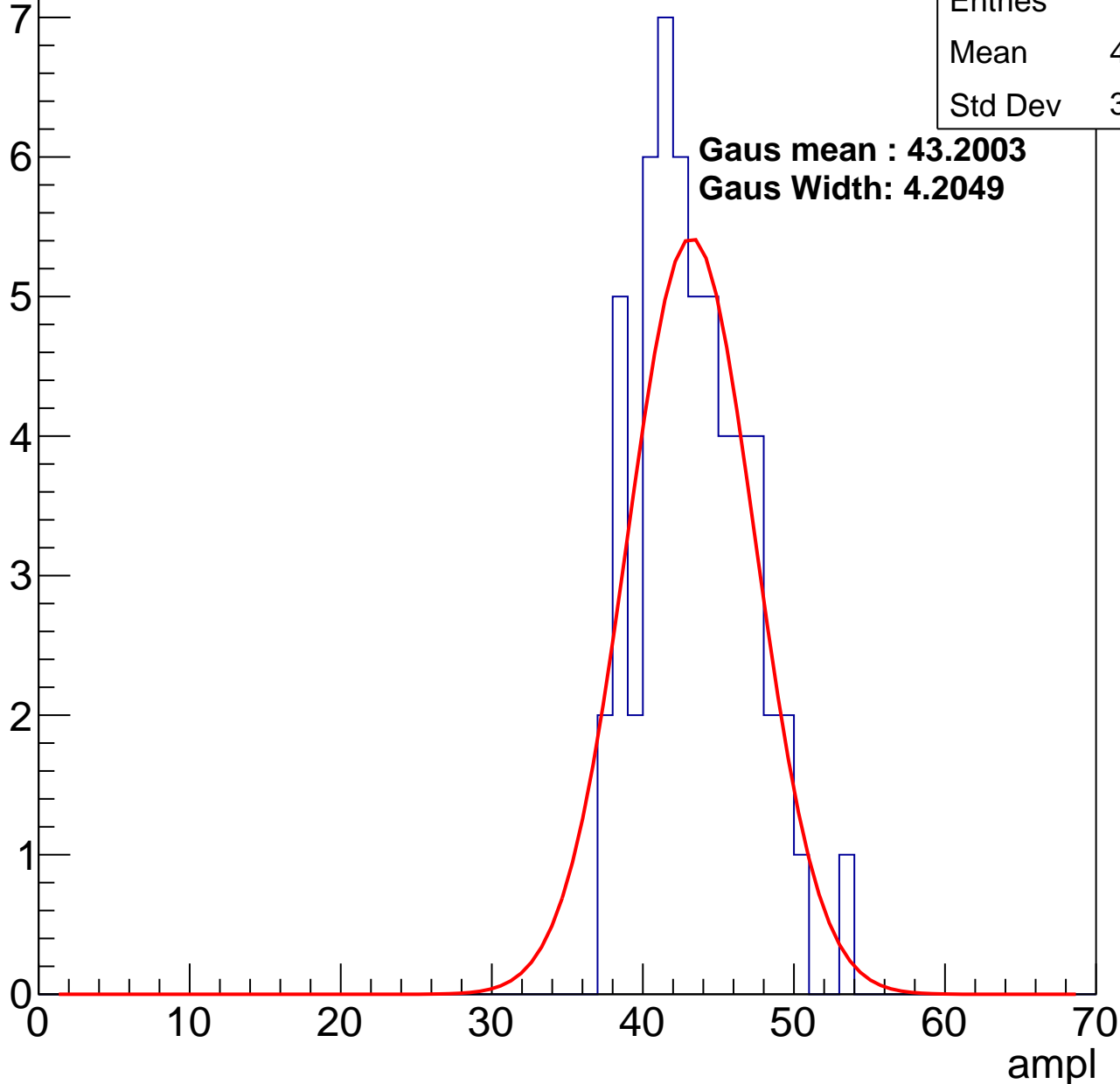
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	56
Mean	42.95
Std Dev	3.558

**Gaus mean : 43.2003**

**Gaus Width: 4.2049**

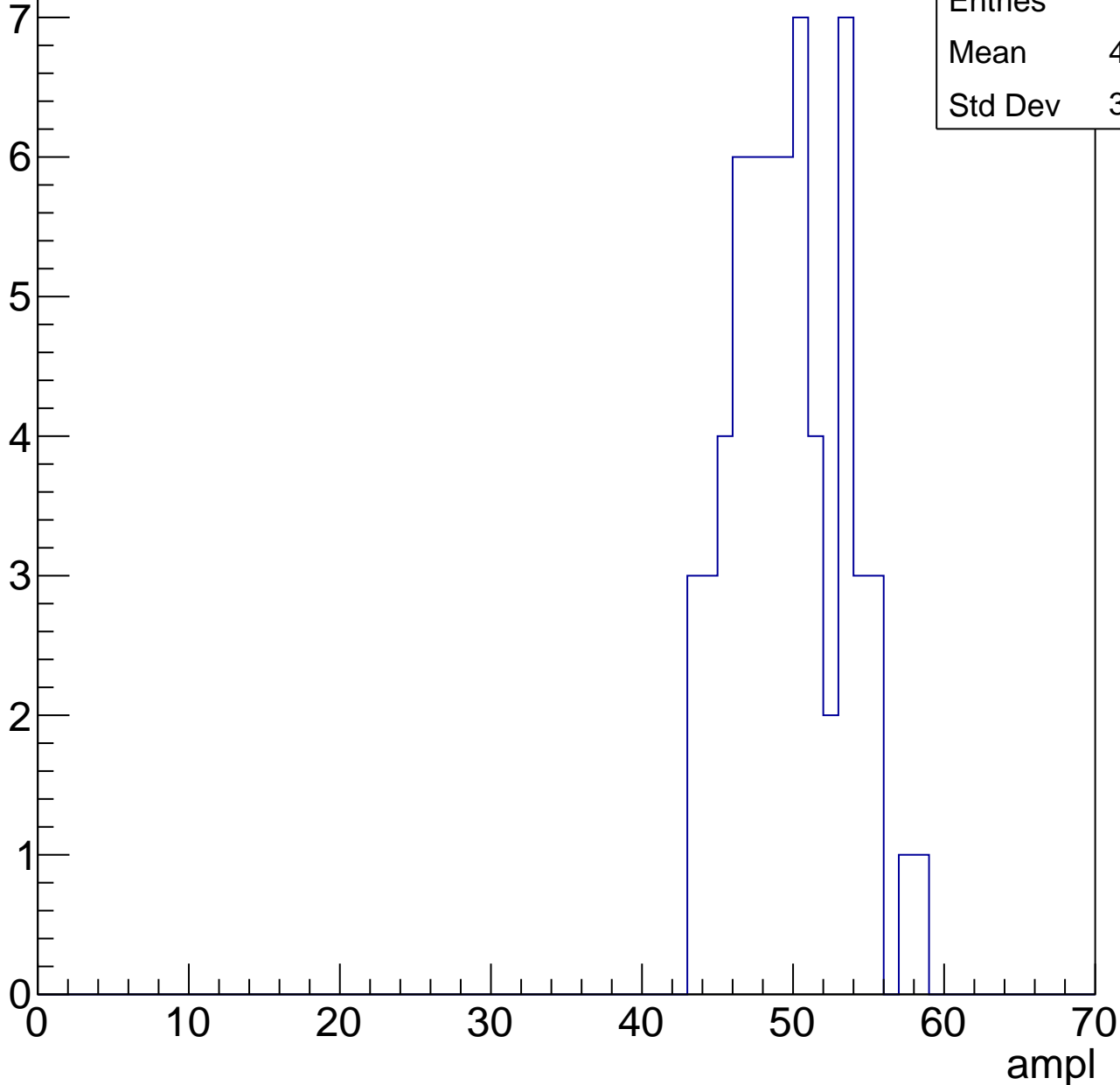


# B1L102S, U12-ch96, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	62
Mean	49.23
Std Dev	3.612

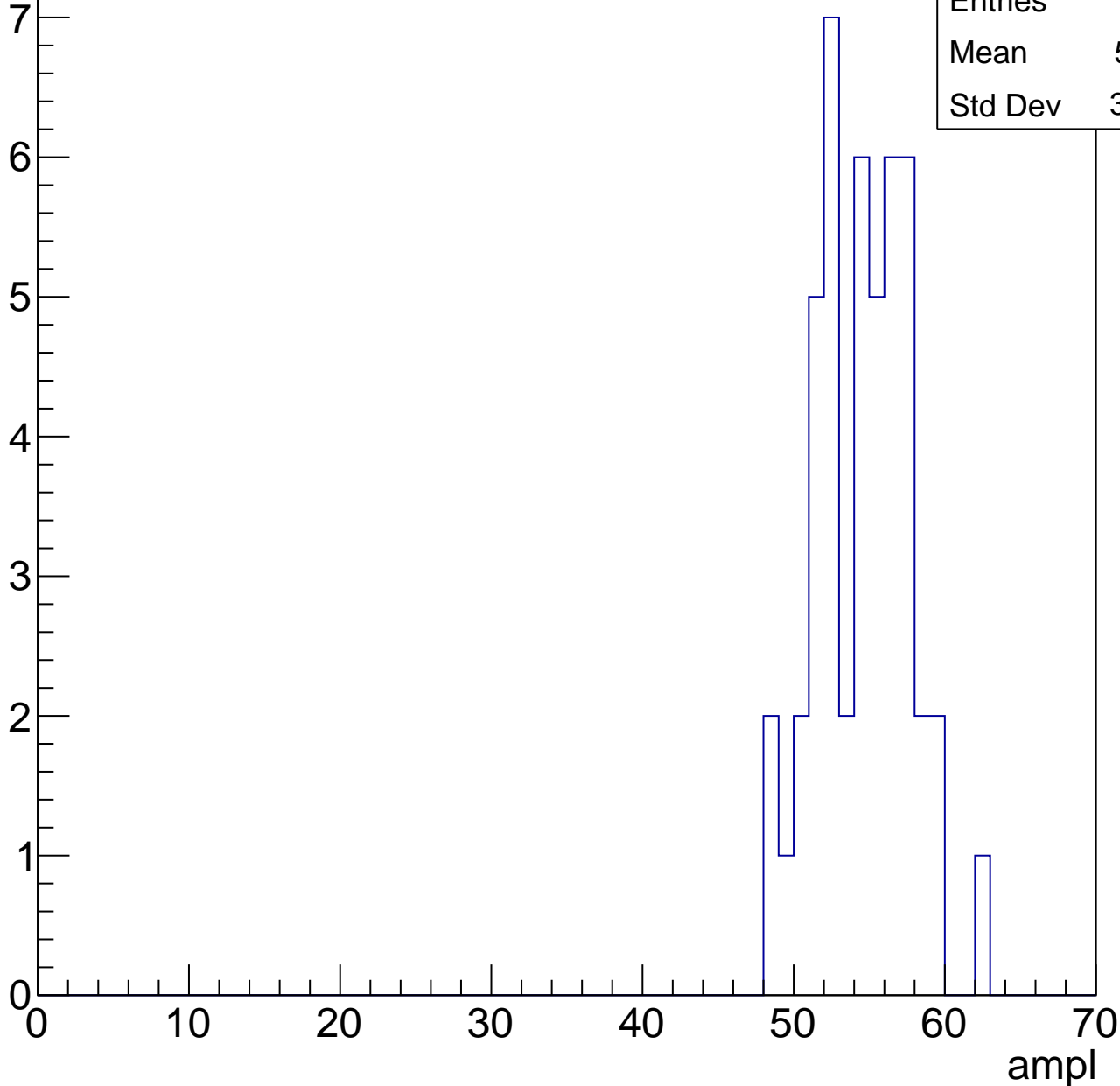


# B1L102S, U12-ch96, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	47
Mean	54.11
Std Dev	3.033

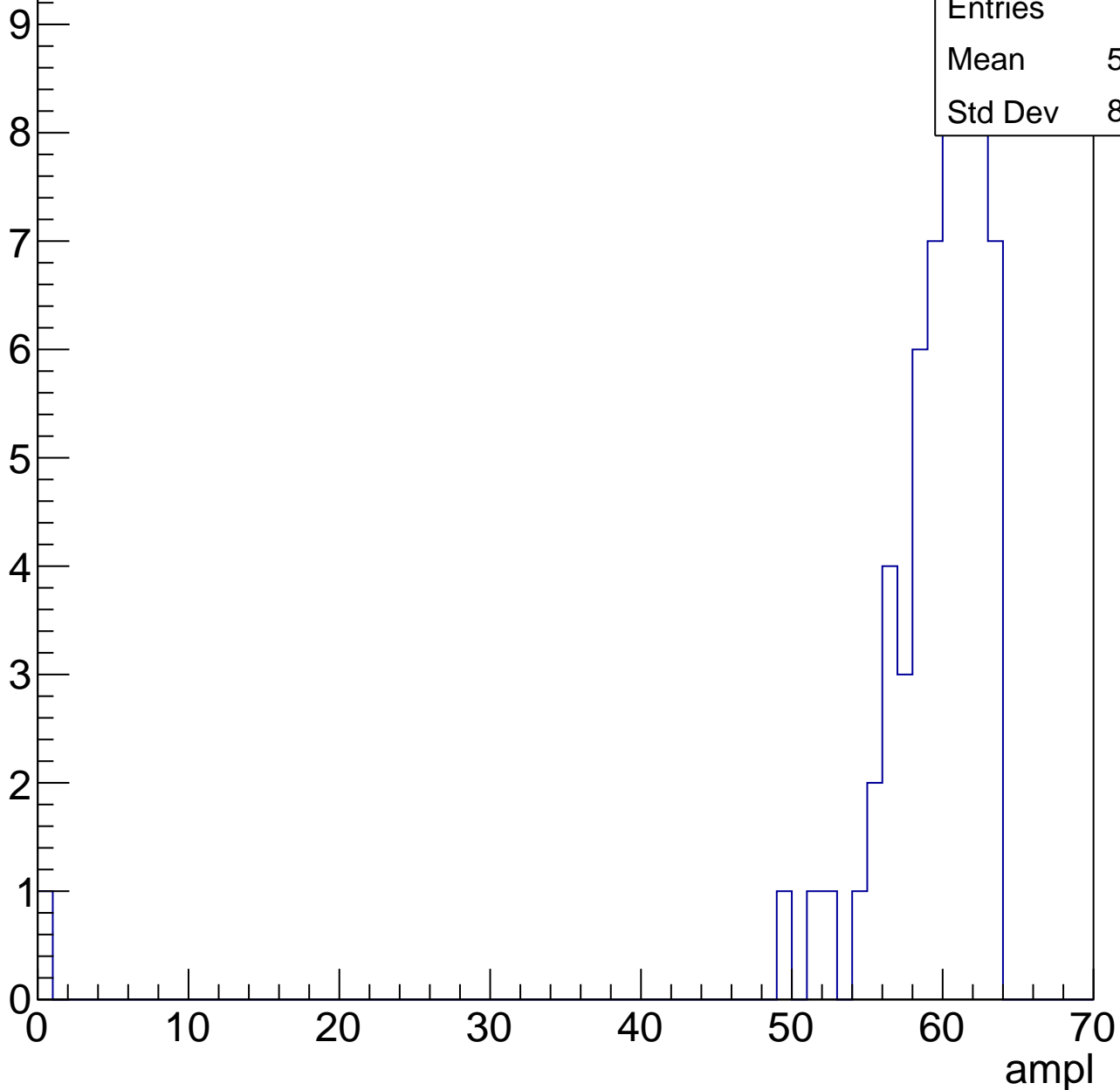


# B1L102S, U12-ch96, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

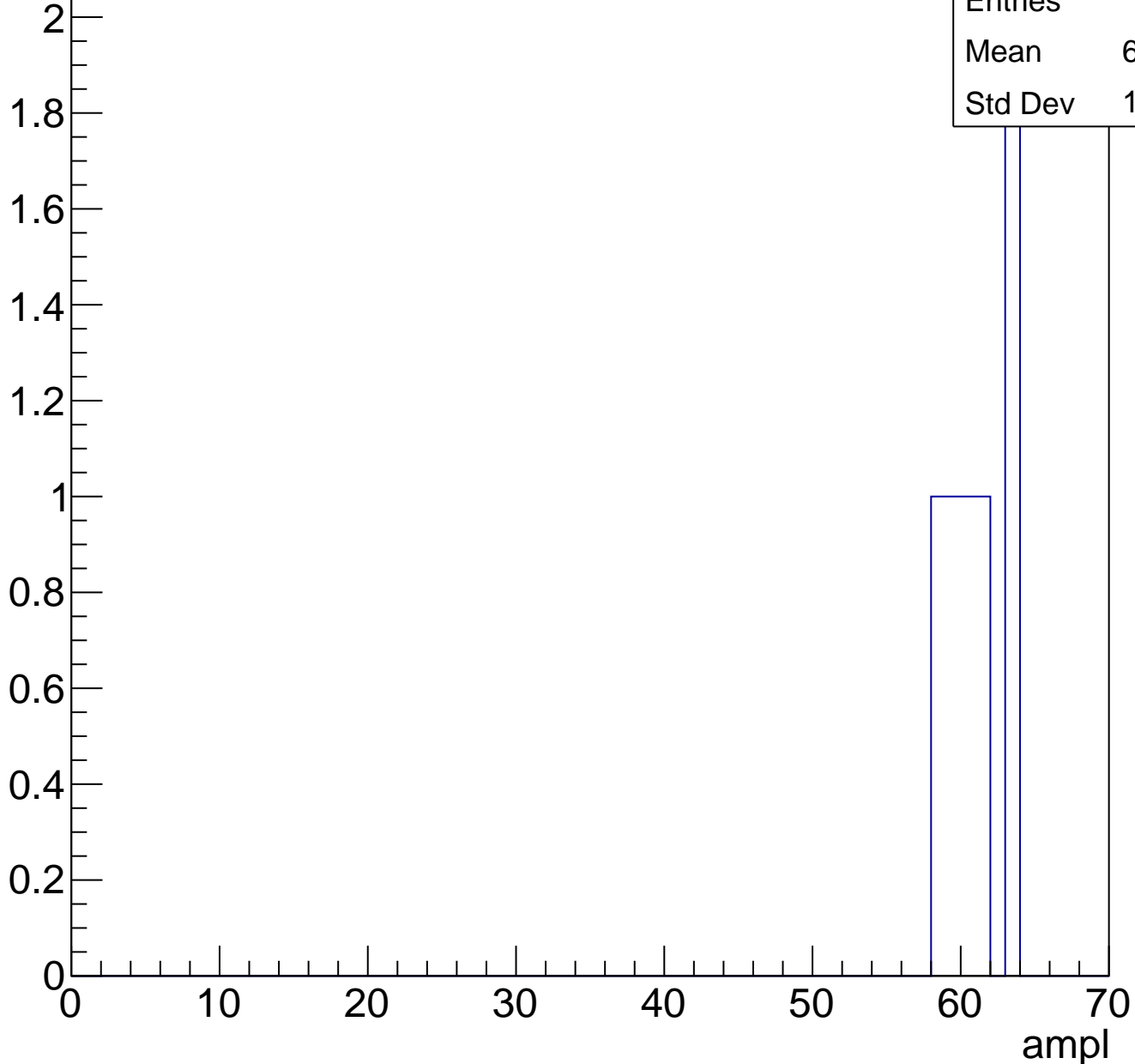
Entries	61
Mean	58.36
Std Dev	8.116



# B1L102S, U12-ch96, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U12-ch96, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U12-ch97, adc0

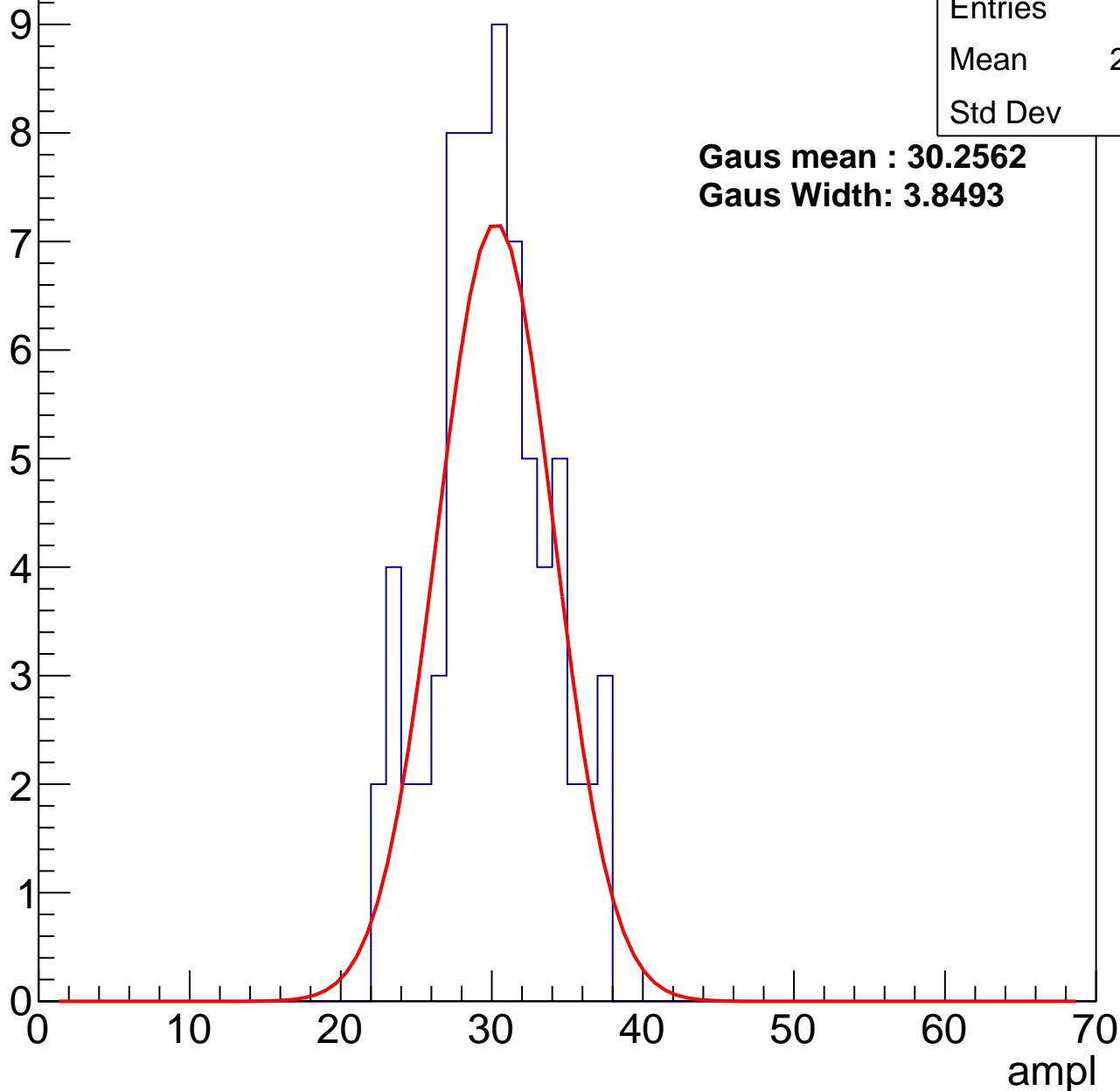
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	74
Mean	29.54
Std Dev	3.68

**Gaus mean : 30.2562**

**Gaus Width: 3.8493**



# B1L102S, U12-ch97, adc1

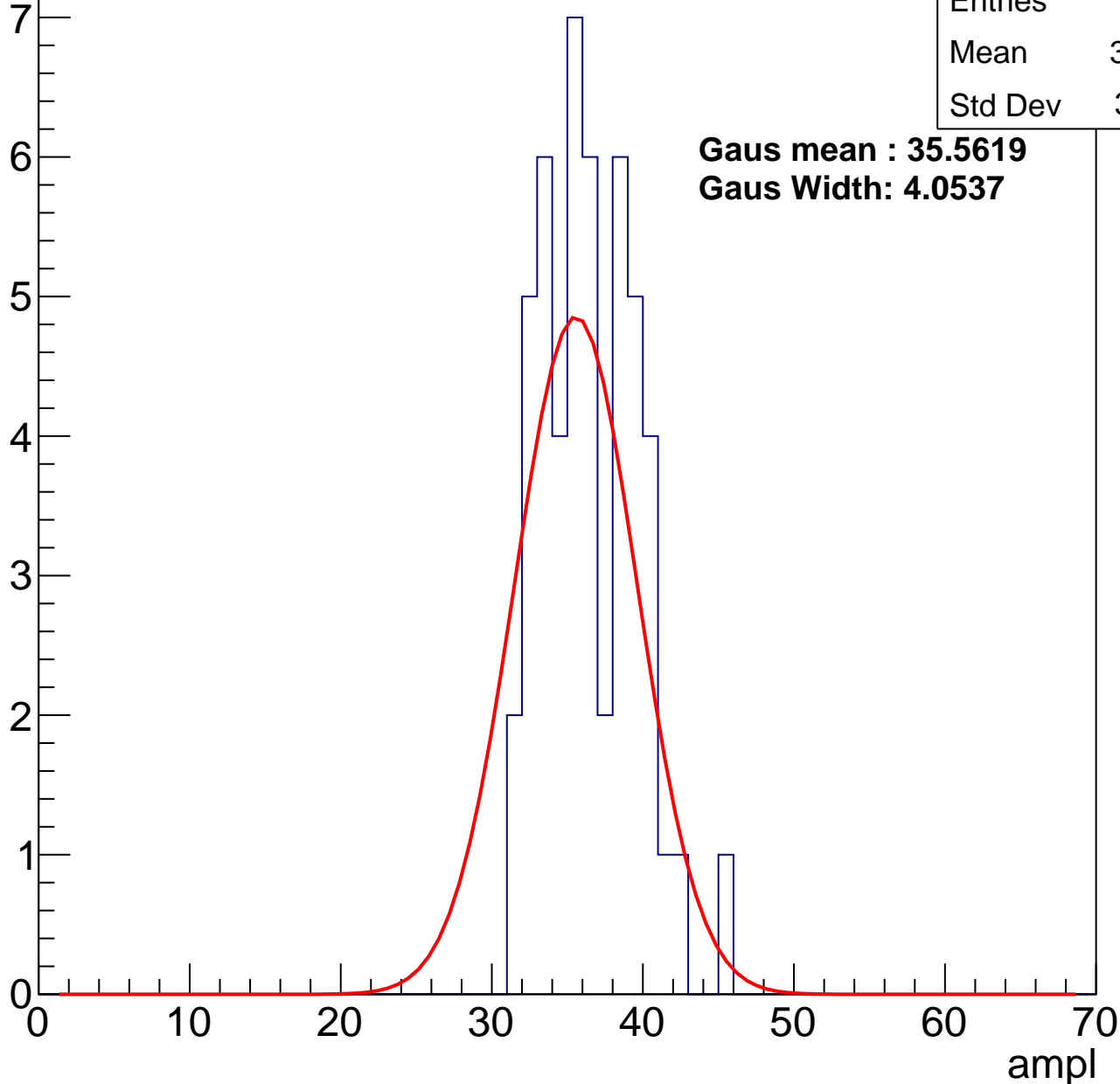
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	50
Mean	36.04
Std Dev	3.111

**Gaus mean : 35.5619**

**Gaus Width: 4.0537**



# B1L102S, U12-ch97, adc2

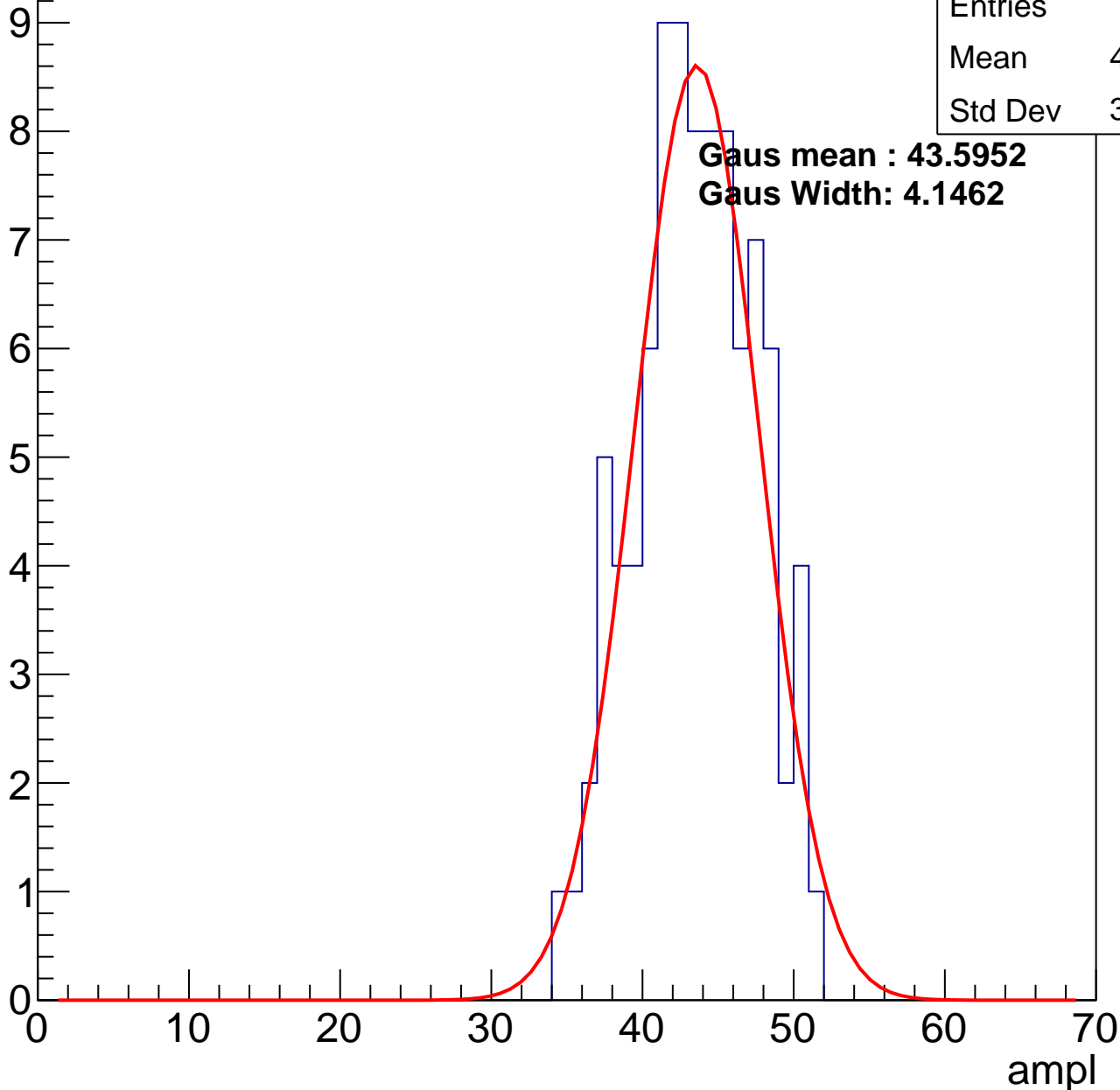
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	91
Mean	43.07
Std Dev	3.885

**Gaus mean : 43.5952**

**Gaus Width: 4.1462**

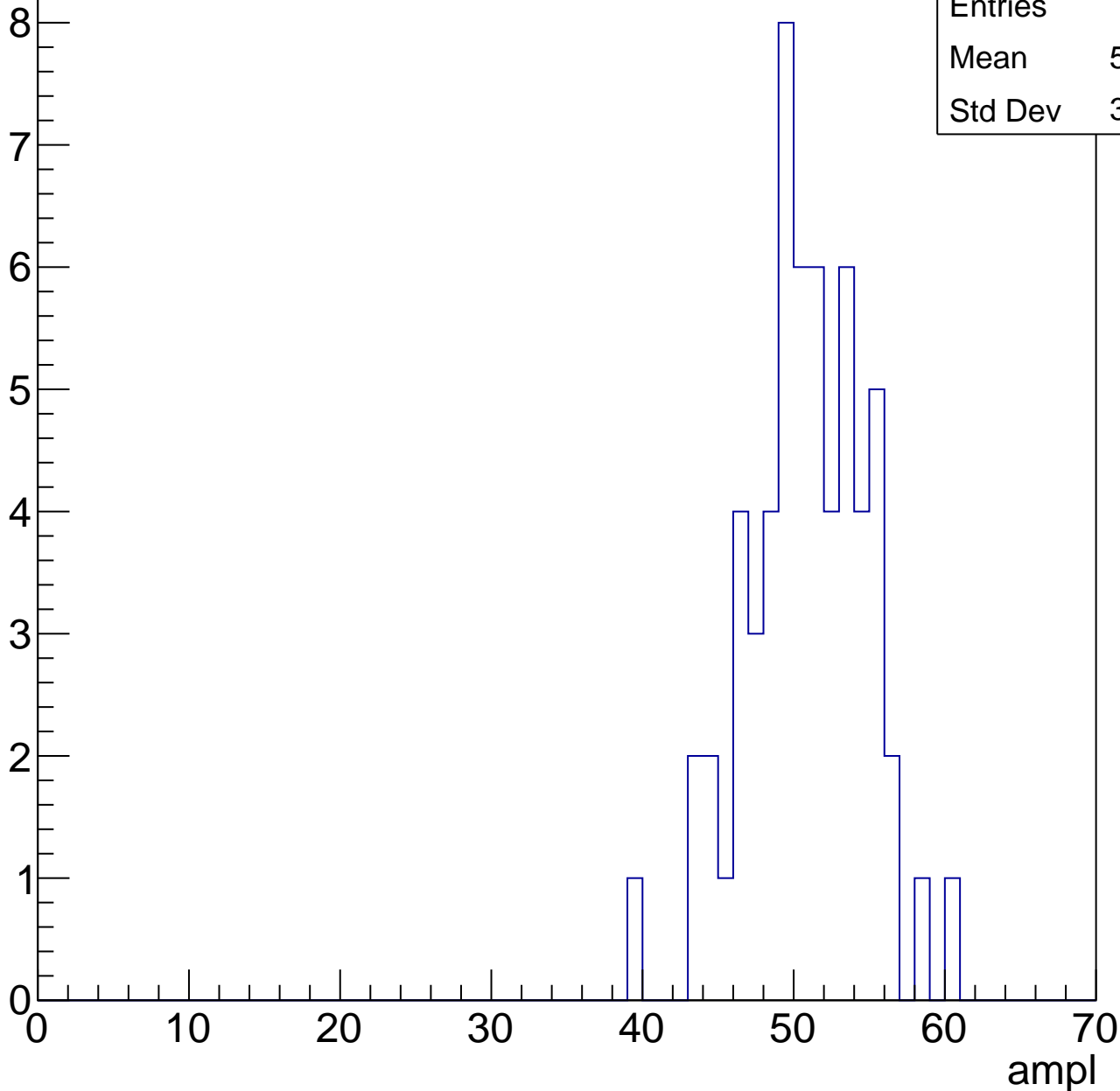


# B1L102S, U12-ch97, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	60
Mean	50.33
Std Dev	3.927

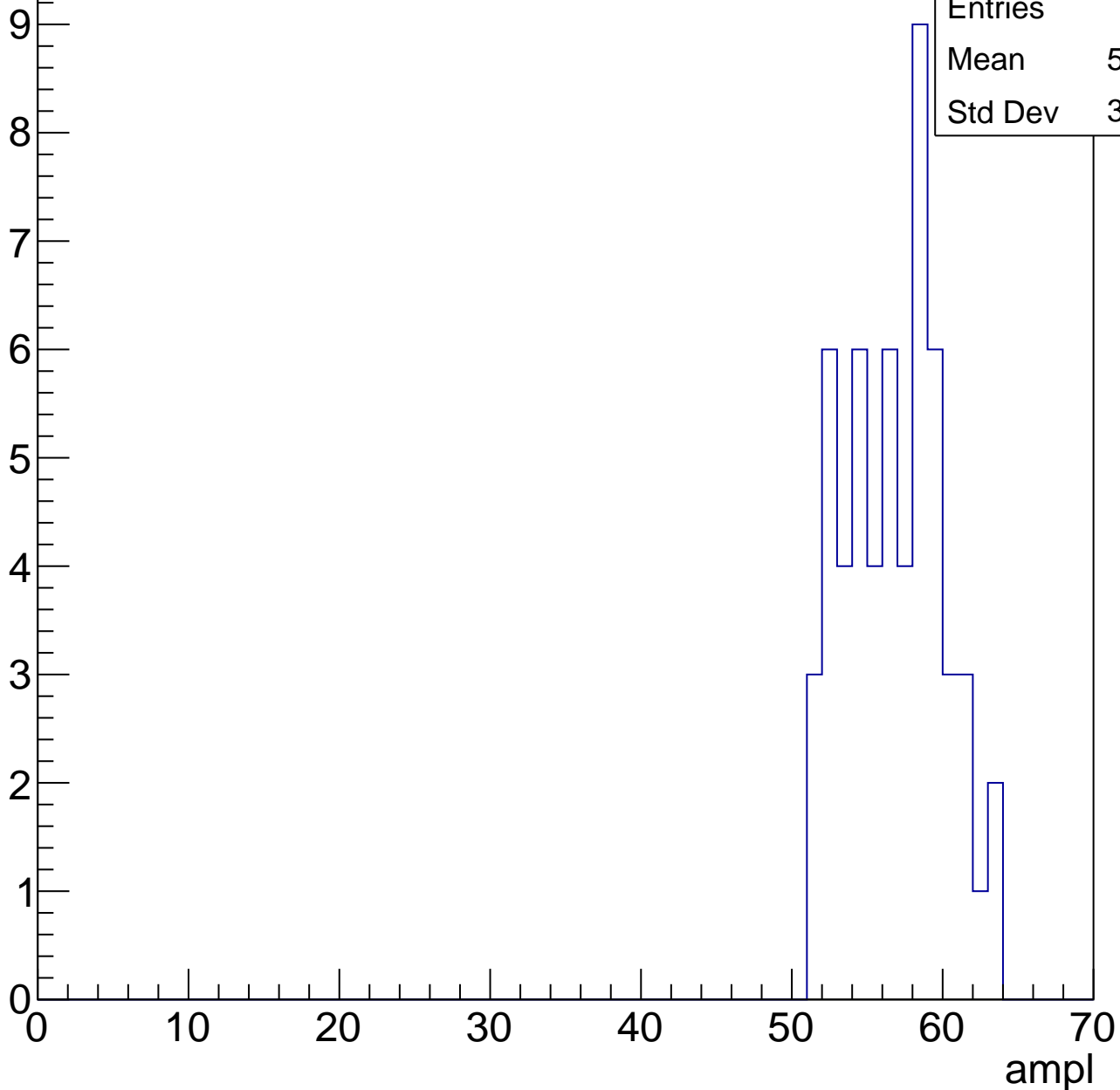


# B1L102S, U12-ch97, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	57
Mean	56.35
Std Dev	3.187

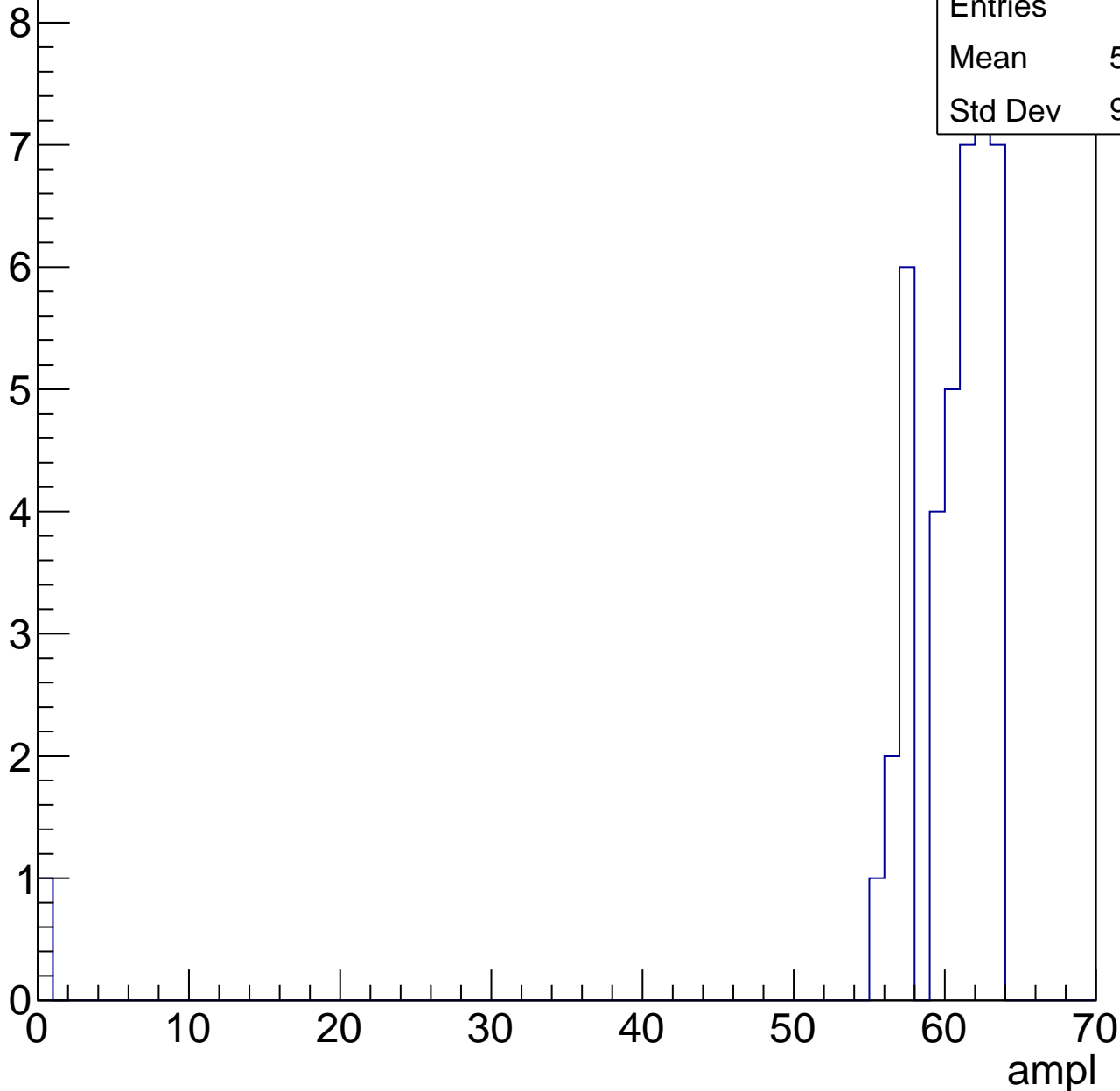


# B1L102S, U12-ch97, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

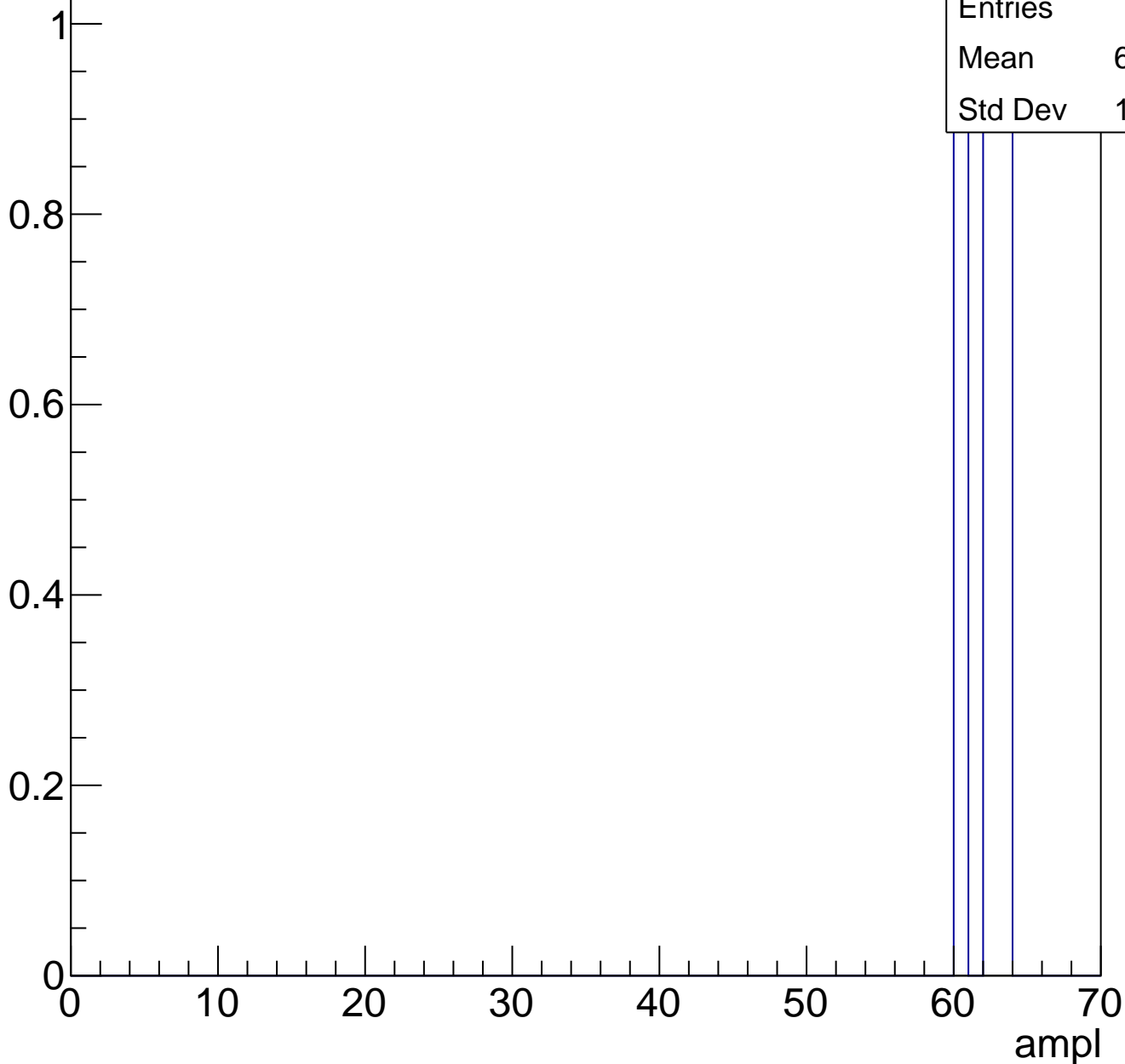
Entries	41
Mean	58.76
Std Dev	9.568



# B1L102S, U12-ch97, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U12-ch97, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L102S, U12-ch98, adc0

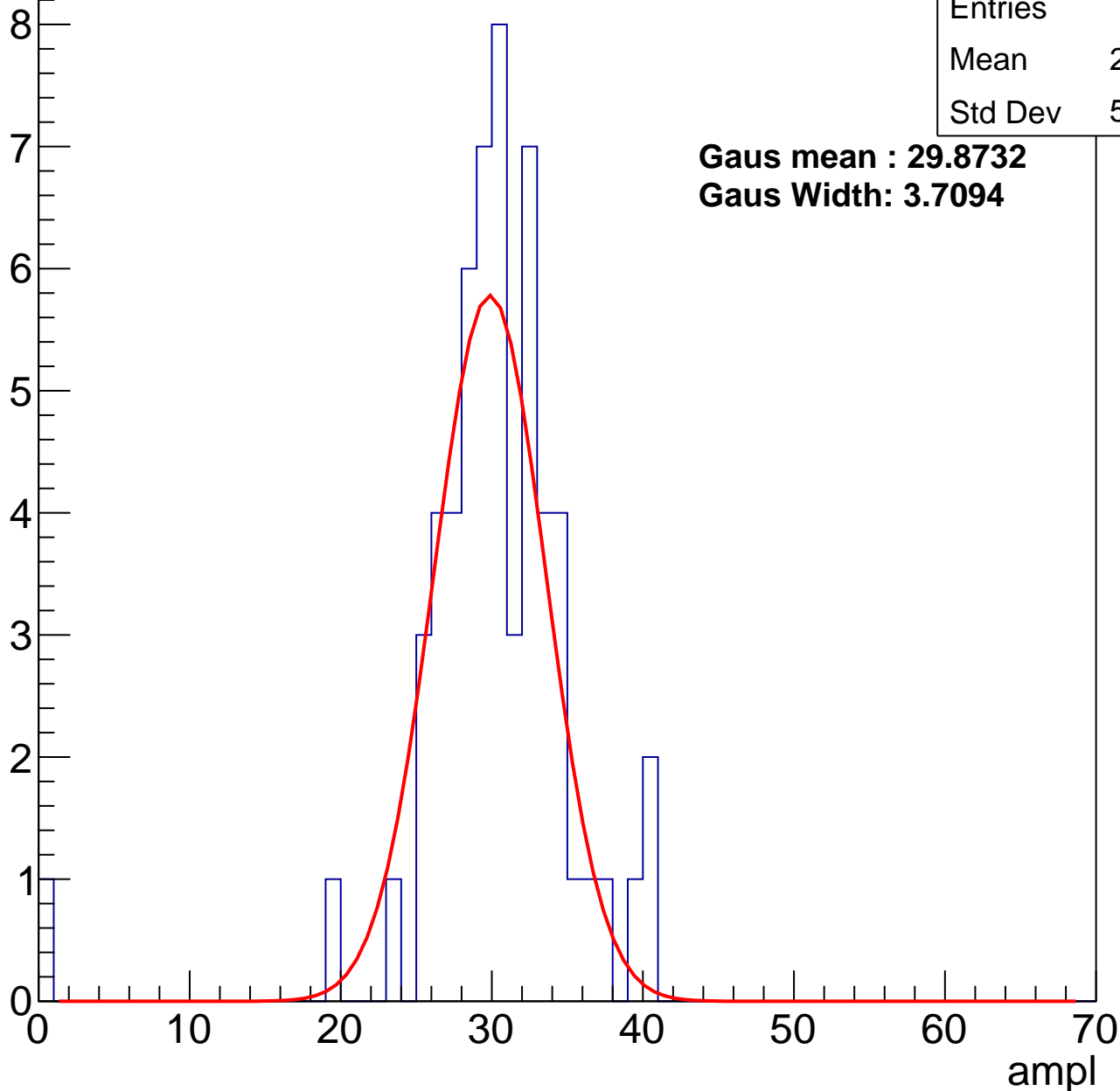
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	59
Mean	29.69
Std Dev	5.512

**Gaus mean : 29.8732**

**Gaus Width: 3.7094**



# B1L102S, U12-ch98, adc1

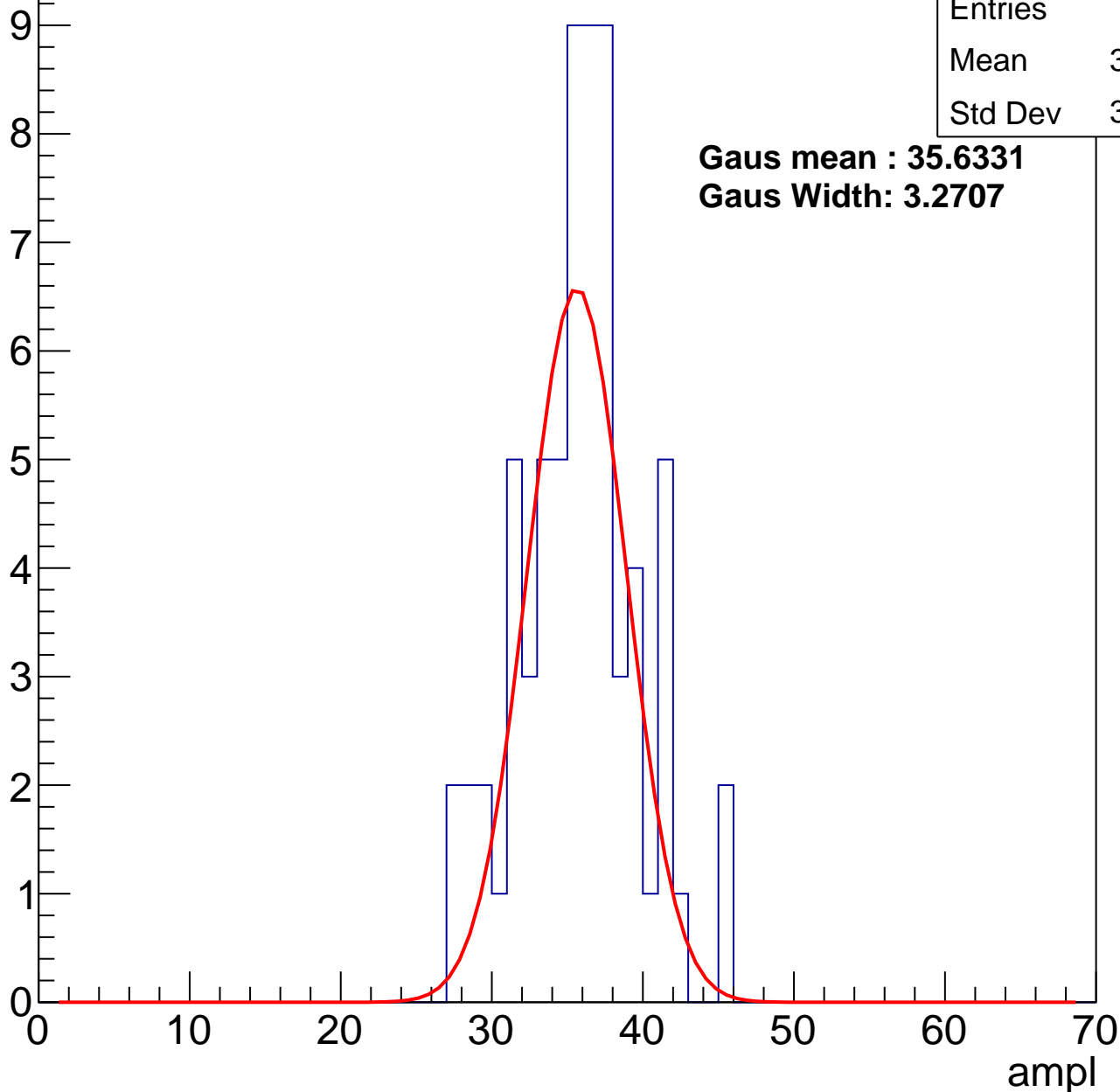
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	35.34
Std Dev	3.906

**Gaus mean : 35.6331**

**Gaus Width: 3.2707**



# B1L102S, U12-ch98, adc2

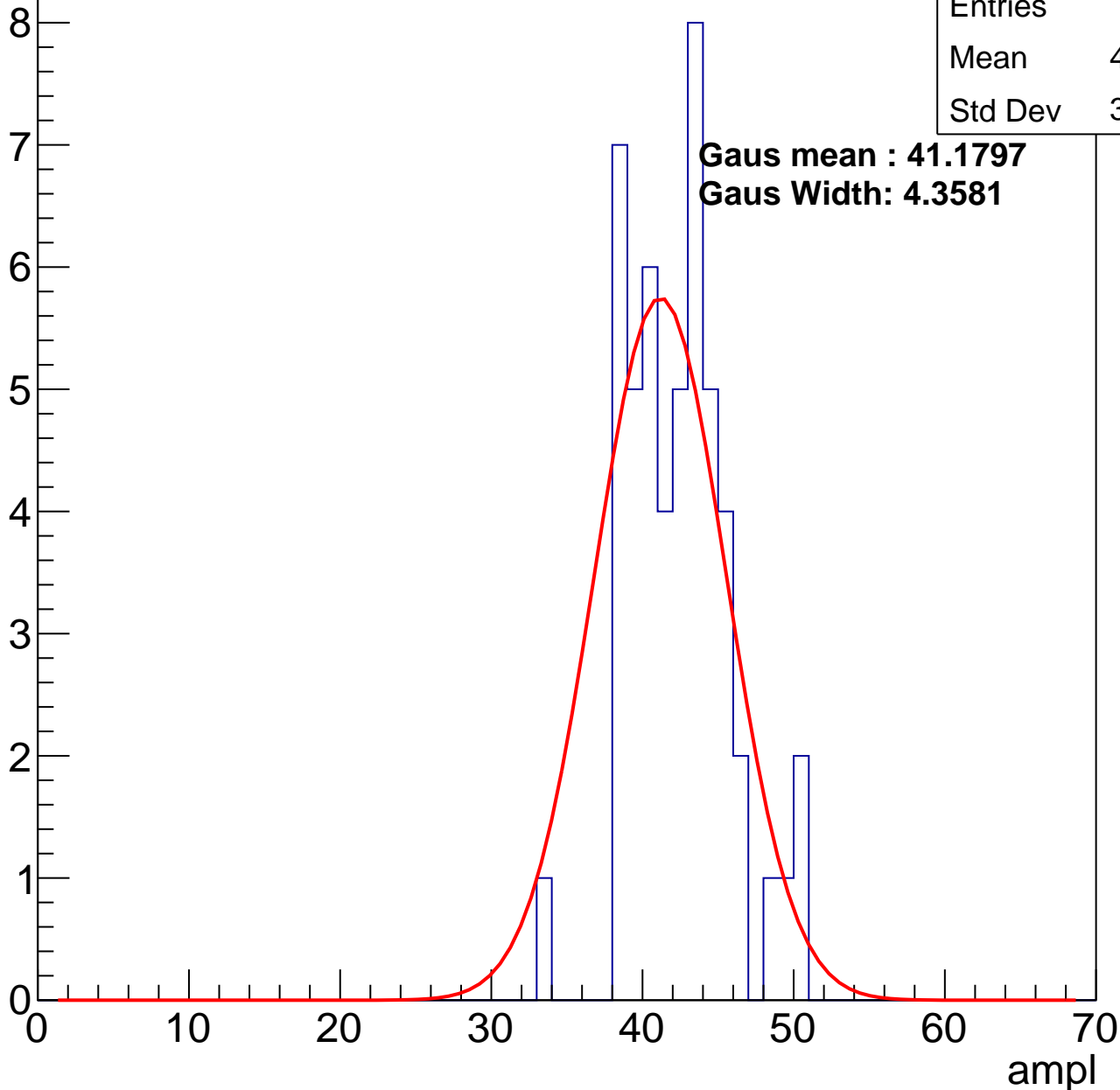
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	51
Mean	41.98
Std Dev	3.358

**Gaus mean : 41.1797**

**Gaus Width: 4.3581**

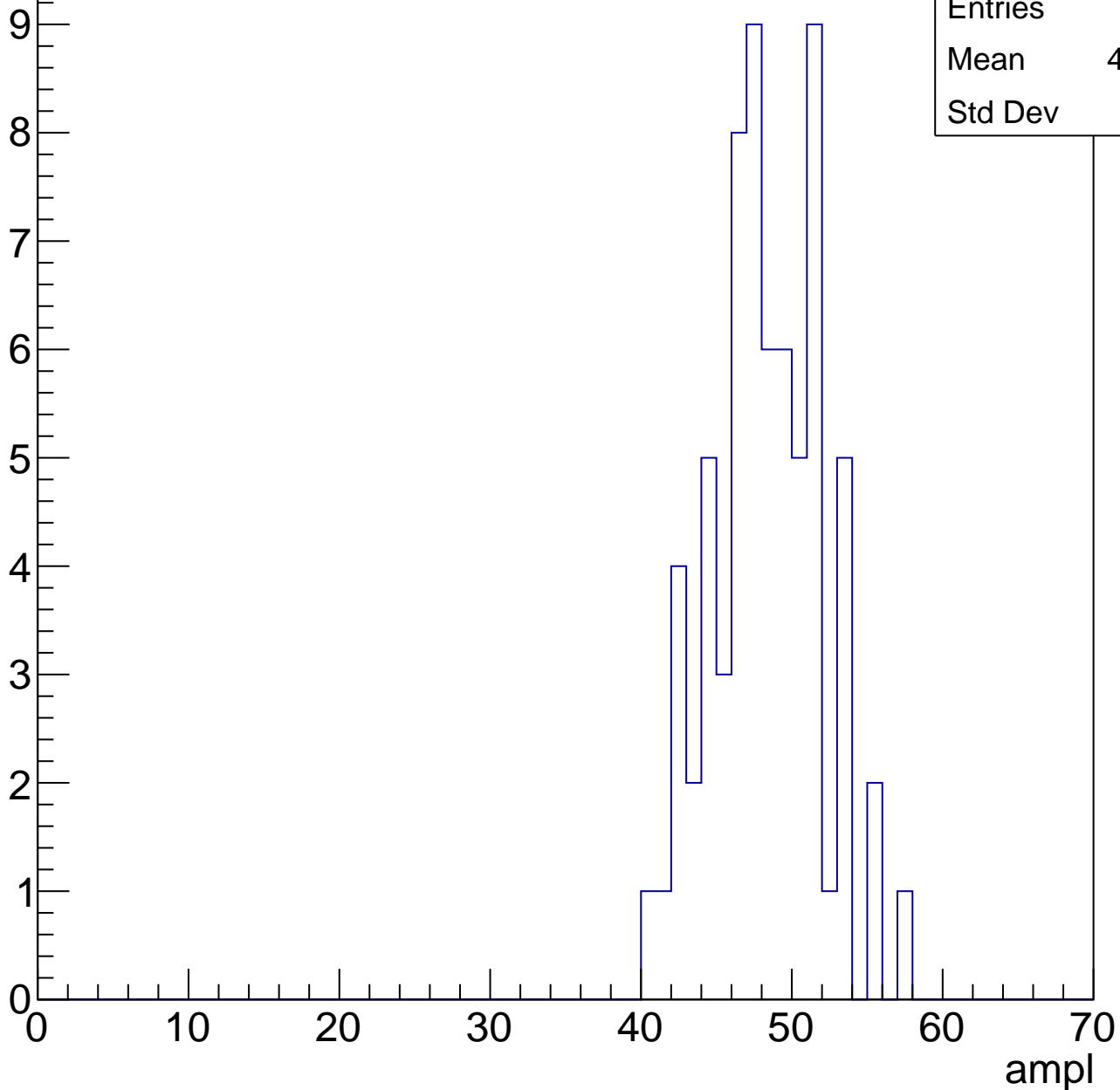


# B1L102S, U12-ch98, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	47.88
Std Dev	3.6

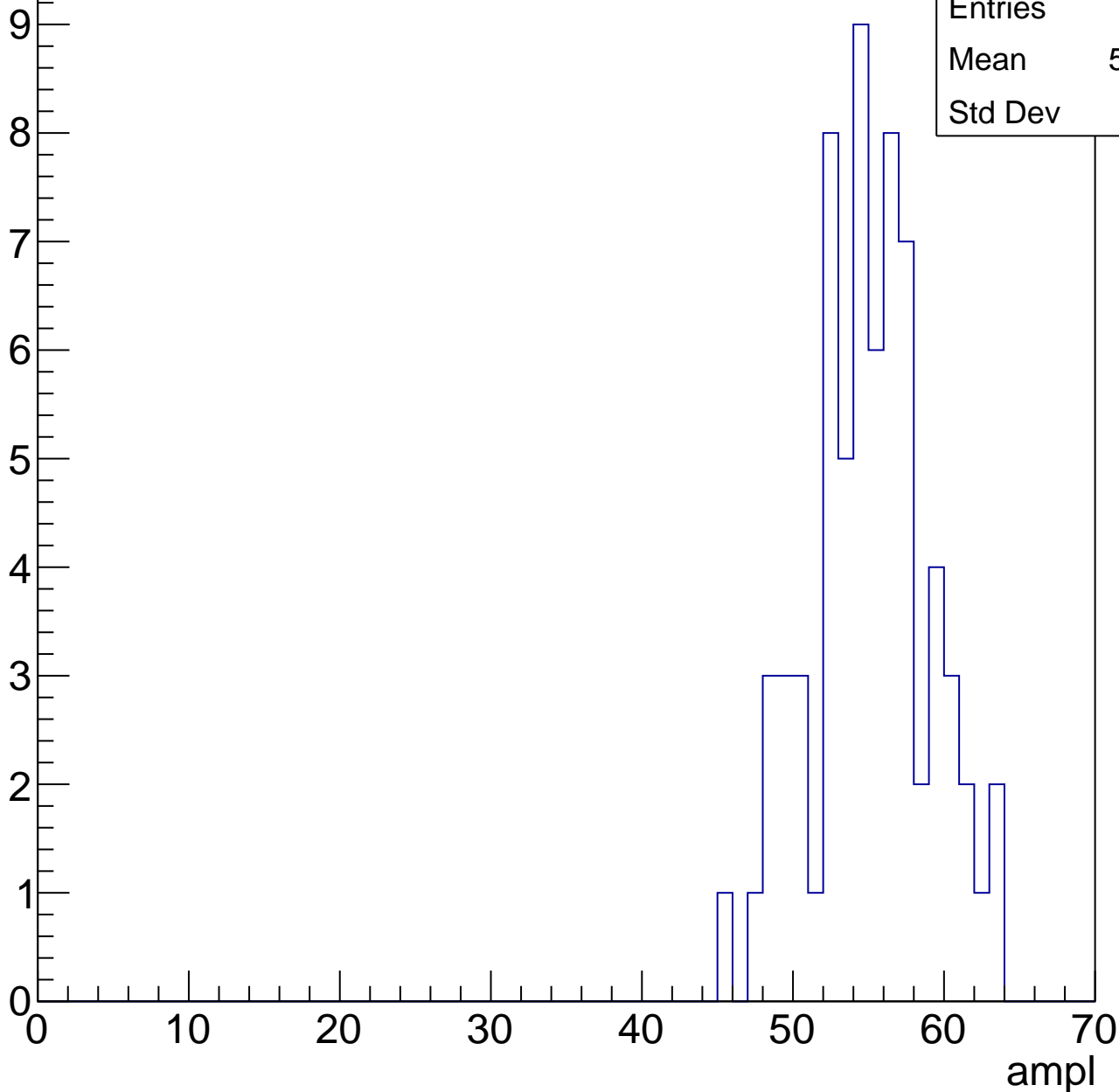


# B1L102S, U12-ch98, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

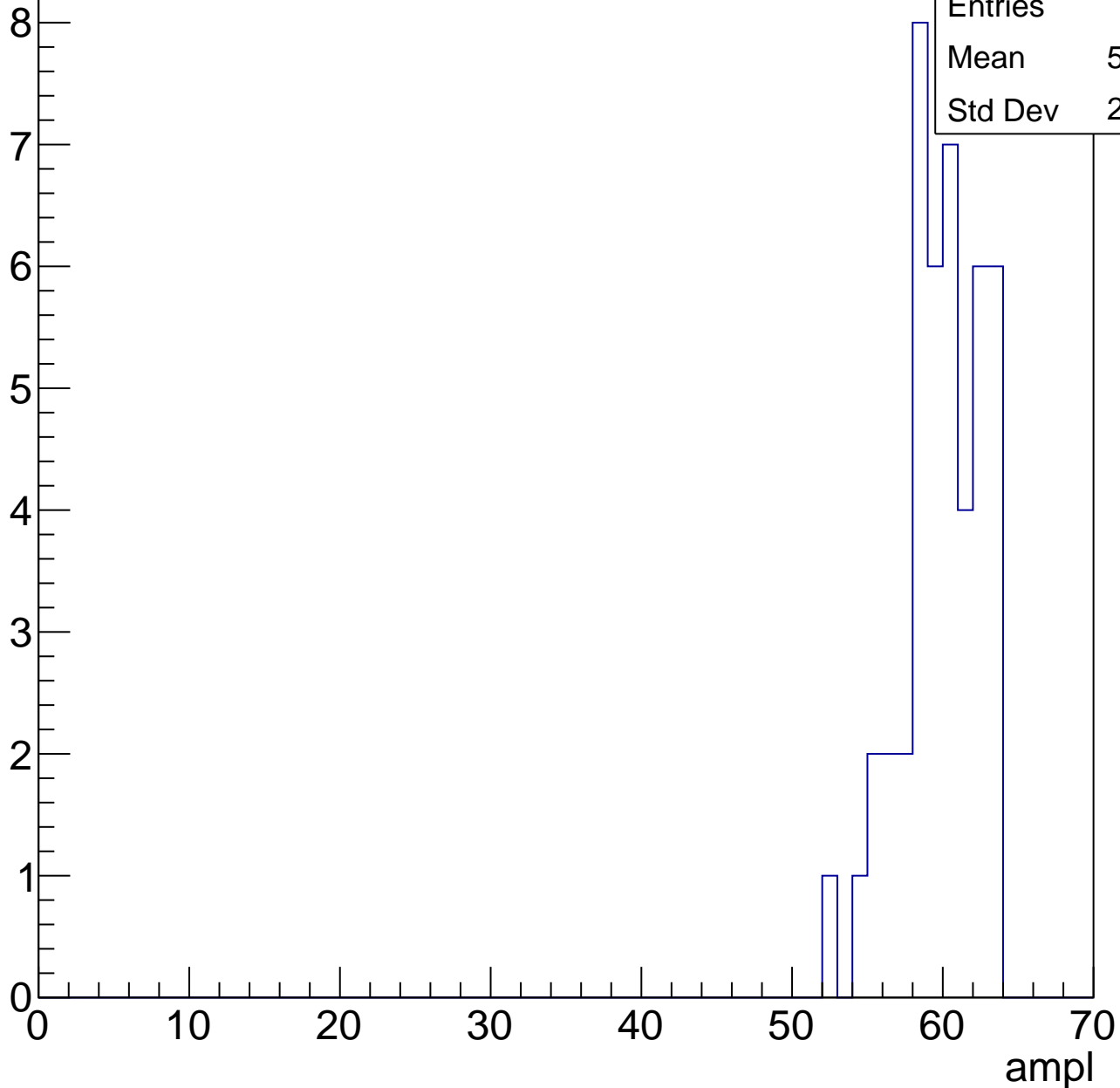
Entries	69
Mean	54.64
Std Dev	3.89



# B1L102S, U12-ch98, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

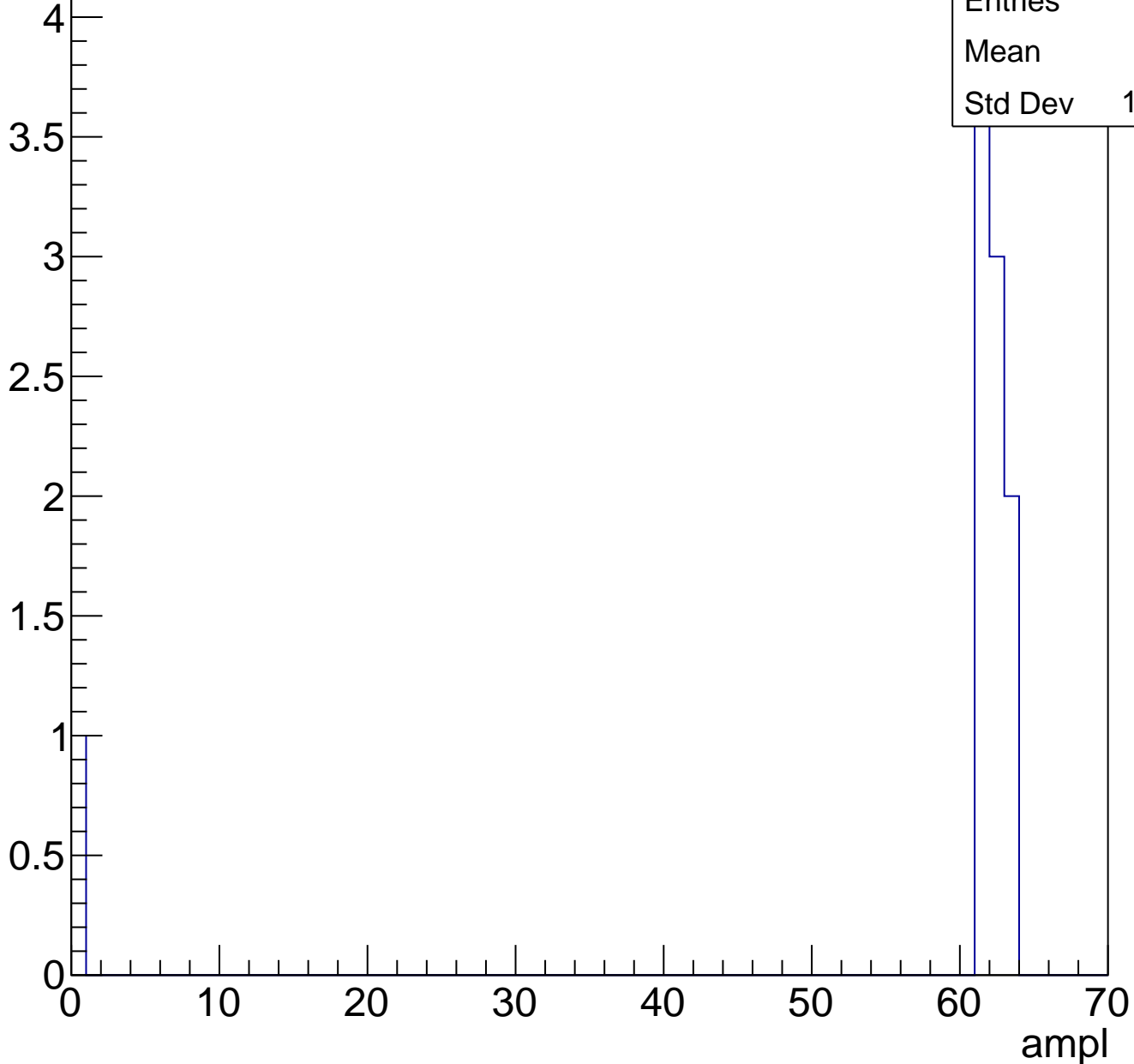
Entry



# B1L102S, U12-ch98, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	10
Mean	55.6
Std Dev	18.55



# B1L102S, U12-ch98, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U12-ch99, adc0

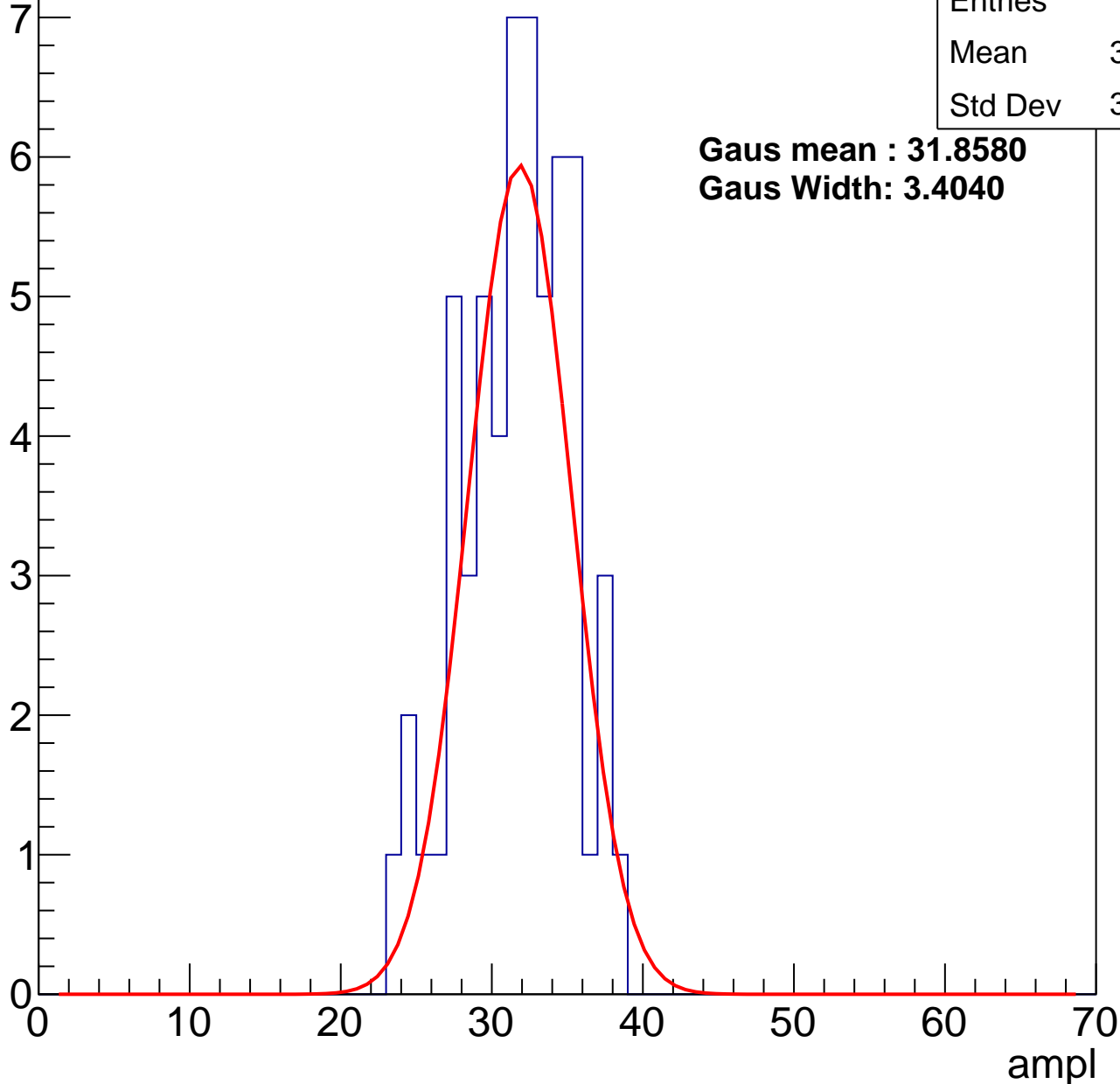
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	58
Mean	31.22
Std Dev	3.499

**Gaus mean : 31.8580**

**Gaus Width: 3.4040**



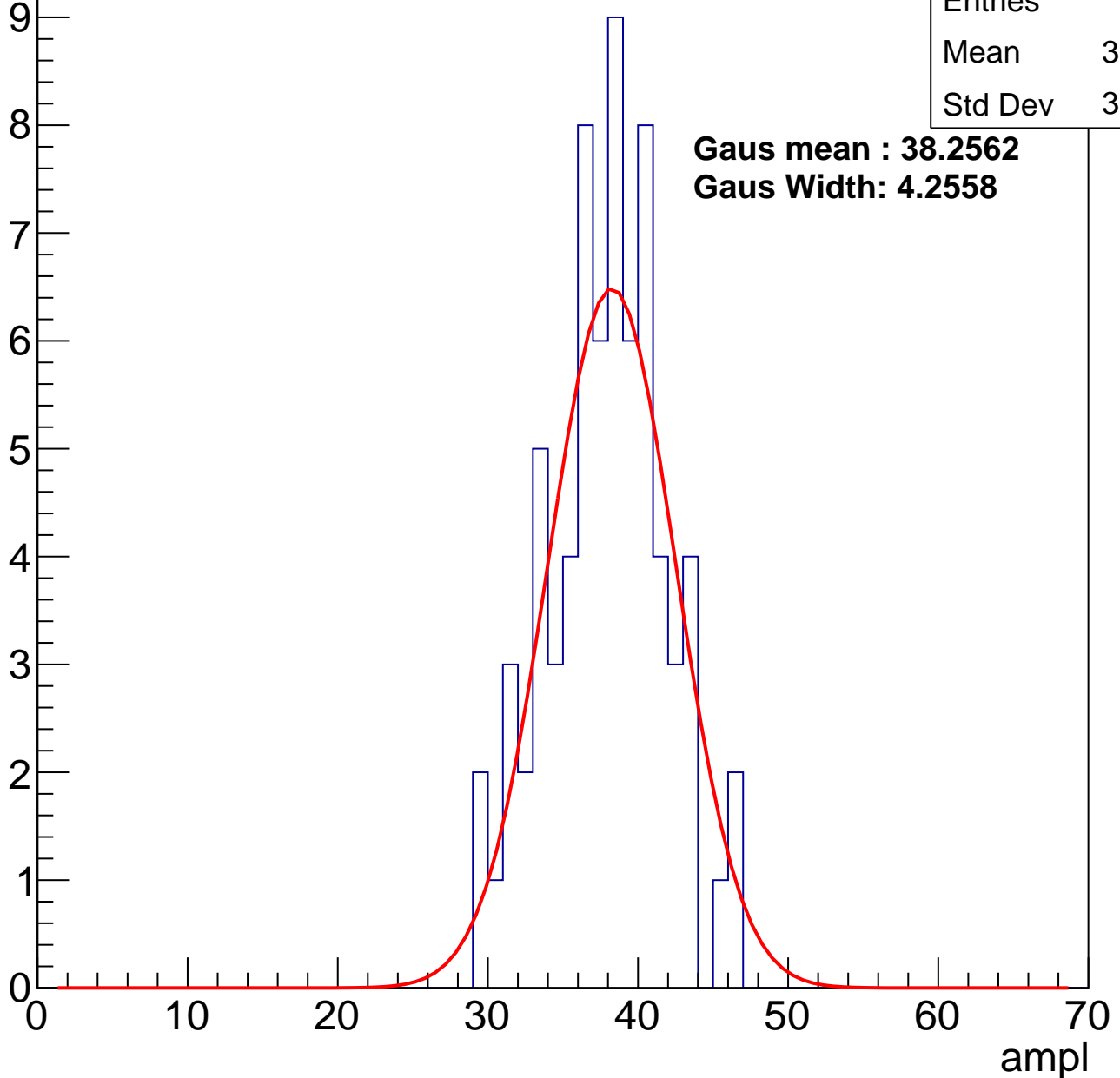
# B1L102S, U12-ch99, adc1

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	71
Mean	37.42
Std Dev	3.877

**Gaus mean : 38.2562**  
**Gaus Width: 4.2558**



# B1L102S, U12-ch99, adc2

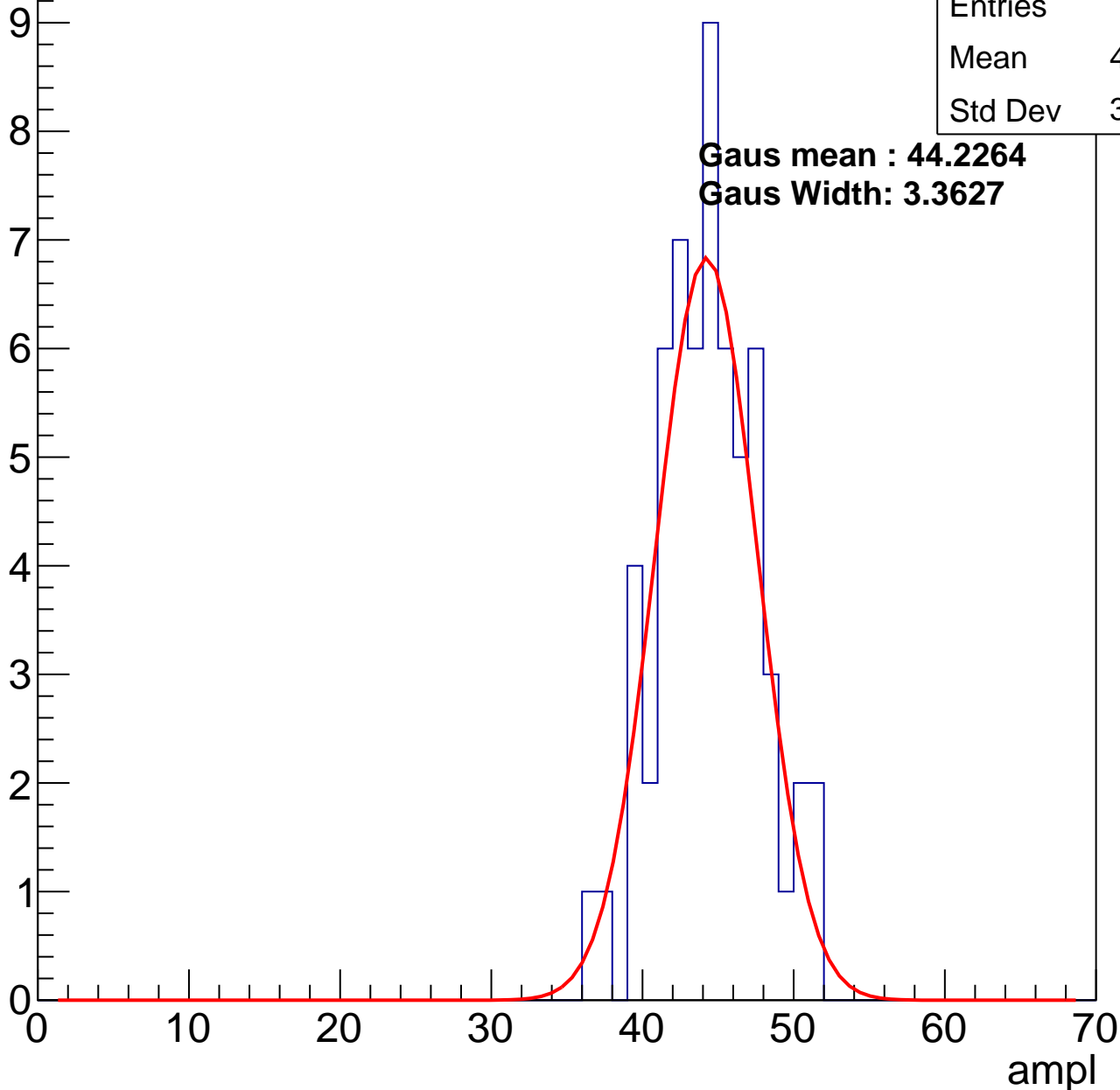
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	43.93
Std Dev	3.279

**Gaus mean : 44.2264**

**Gaus Width: 3.3627**

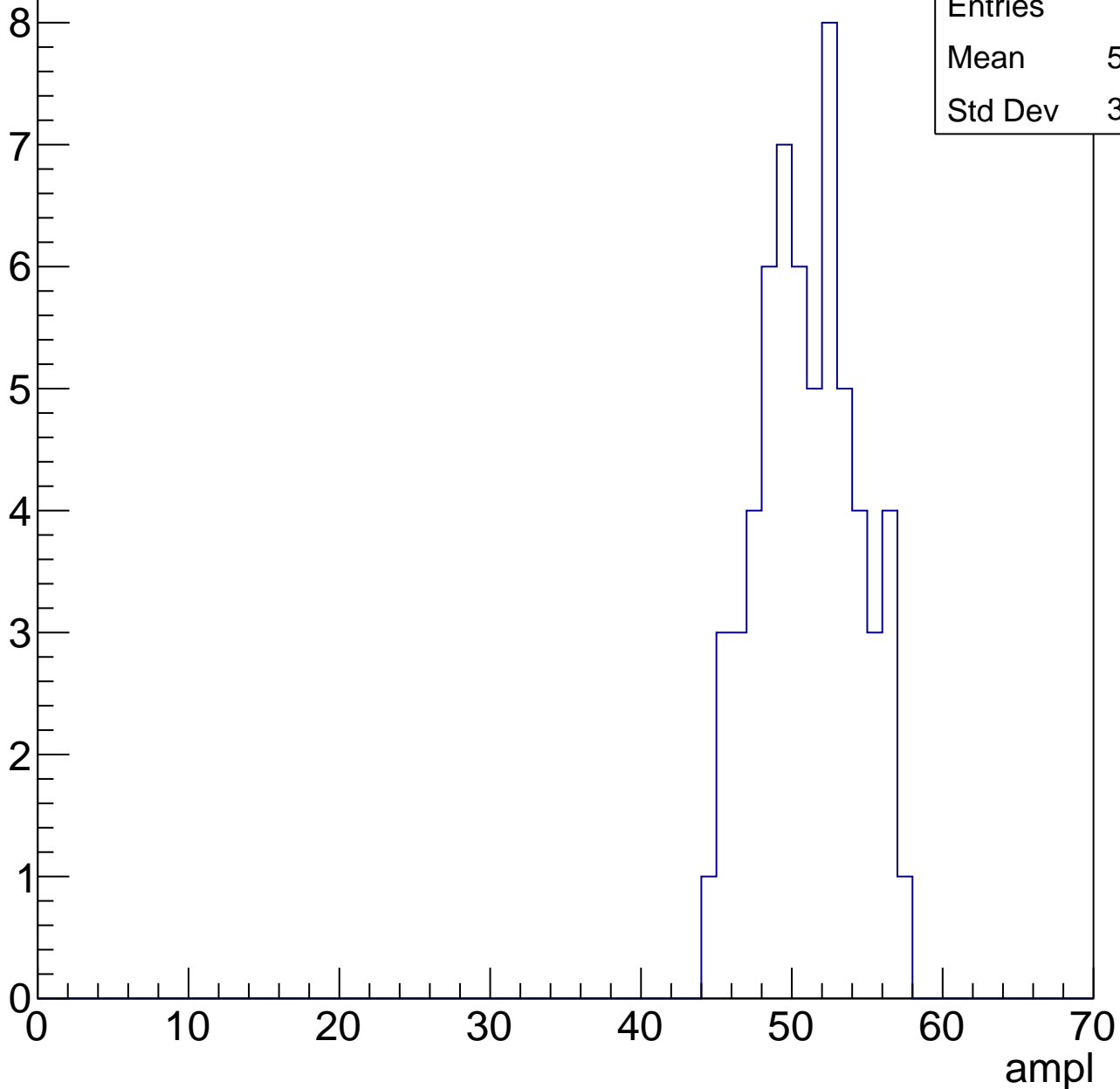


# B1L102S, U12-ch99, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	60
Mean	50.57
Std Dev	3.216

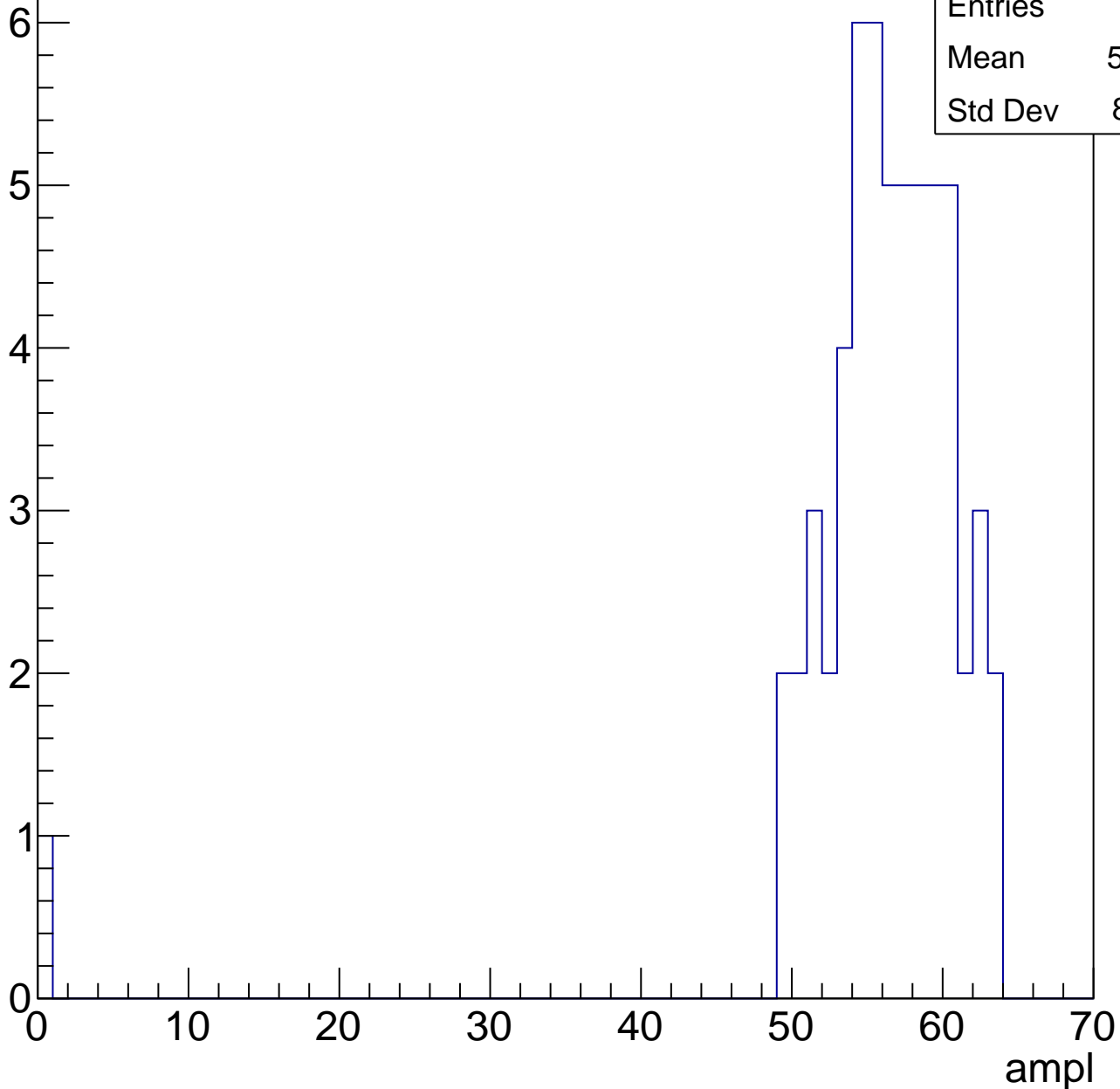


# B1L102S, U12-ch99, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	58
Mean	55.26
Std Dev	8.151

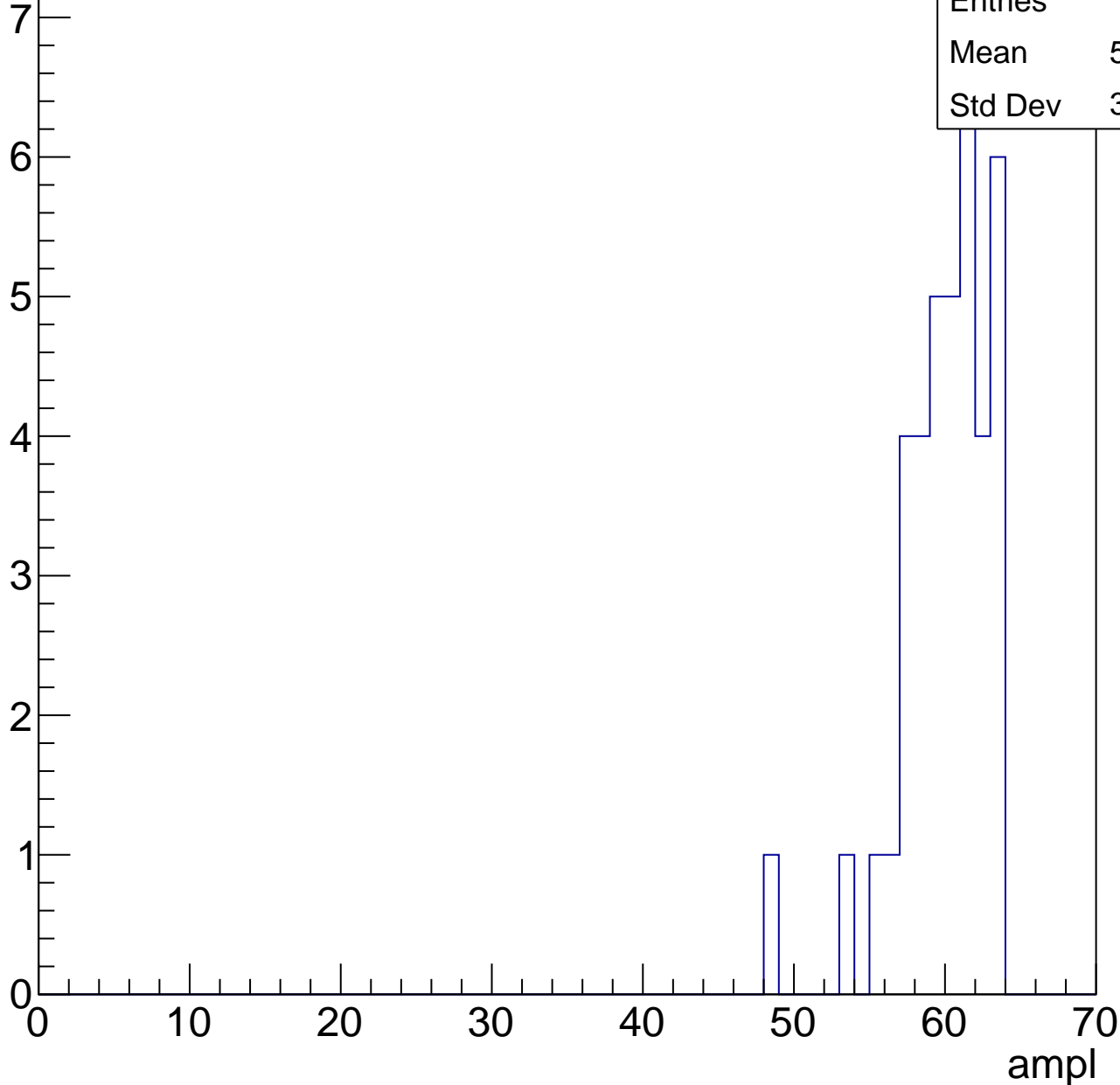


# B1L102S, U12-ch99, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

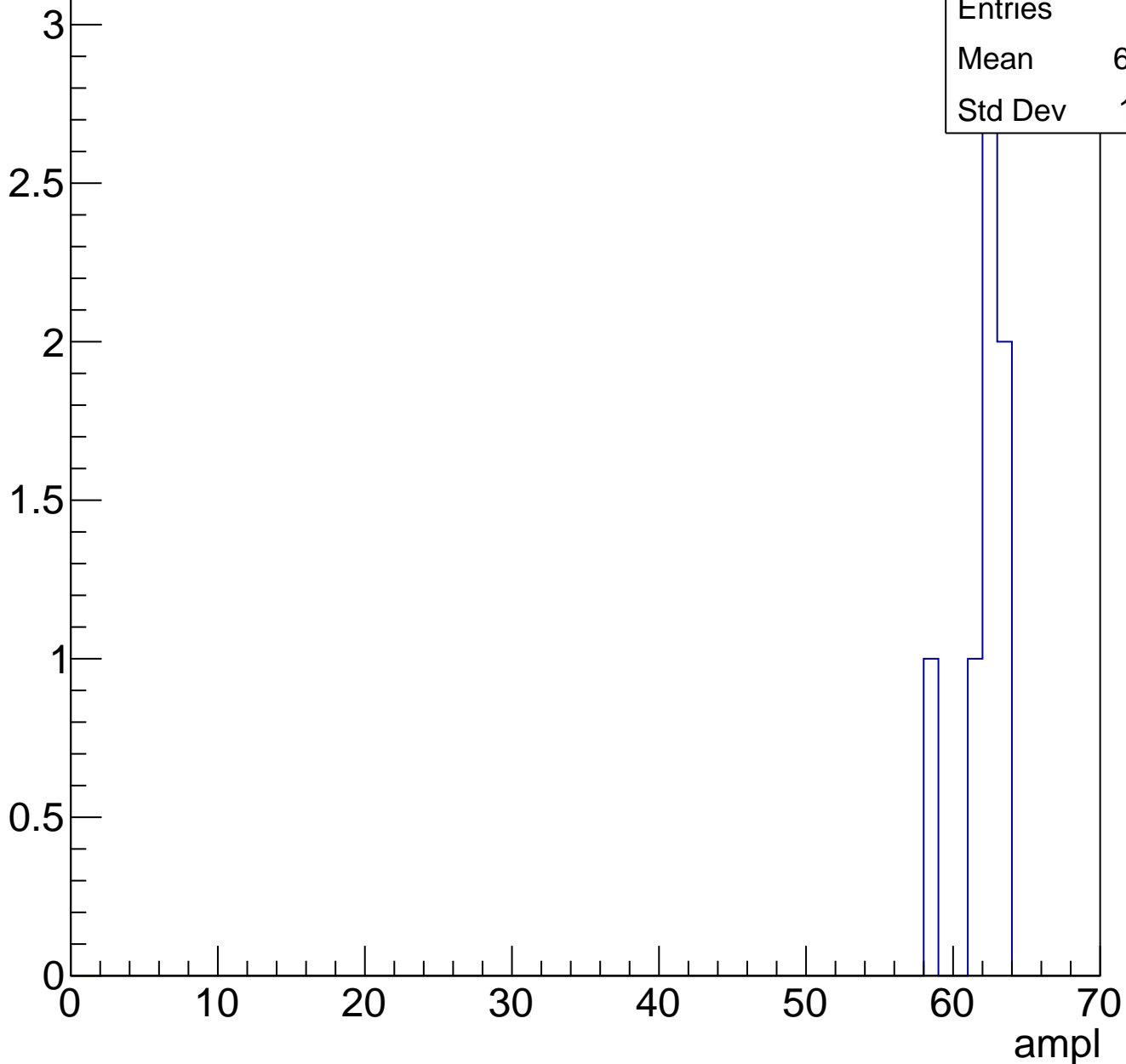
Entries	39
Mean	59.49
Std Dev	3.029



# B1L102S, U12-ch99, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U12-ch99, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

1  
0.8  
0.6  
0.4  
0.2  
0

Entries	1
Mean	23
Std Dev	0

ampl

# B1L102S, U12-ch100, adc0

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	68
Mean	29.63
Std Dev	3.294

**Gaus mean : 30.4324**

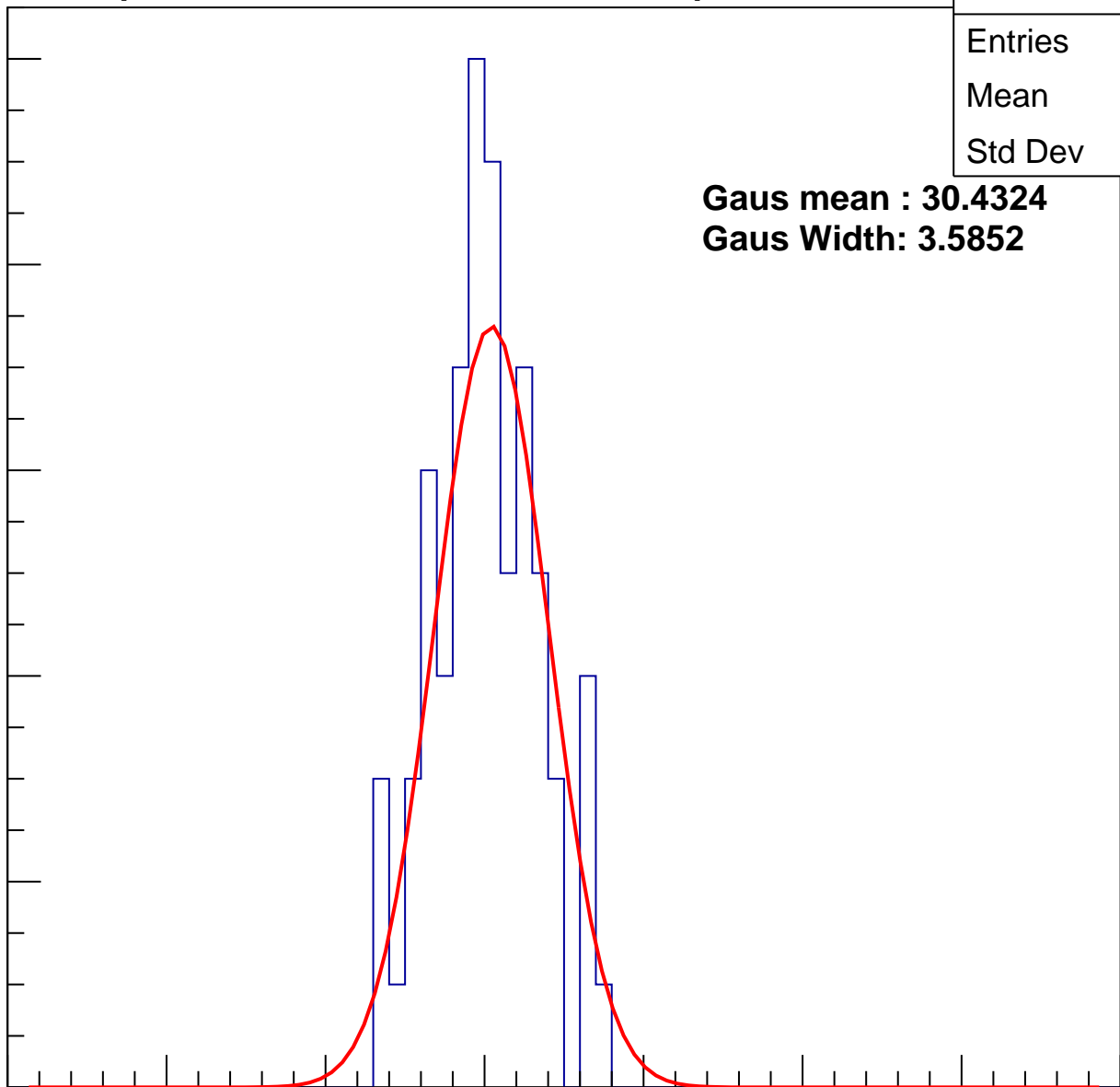
**Gaus Width: 3.5852**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L102S, U12-ch100, adc1

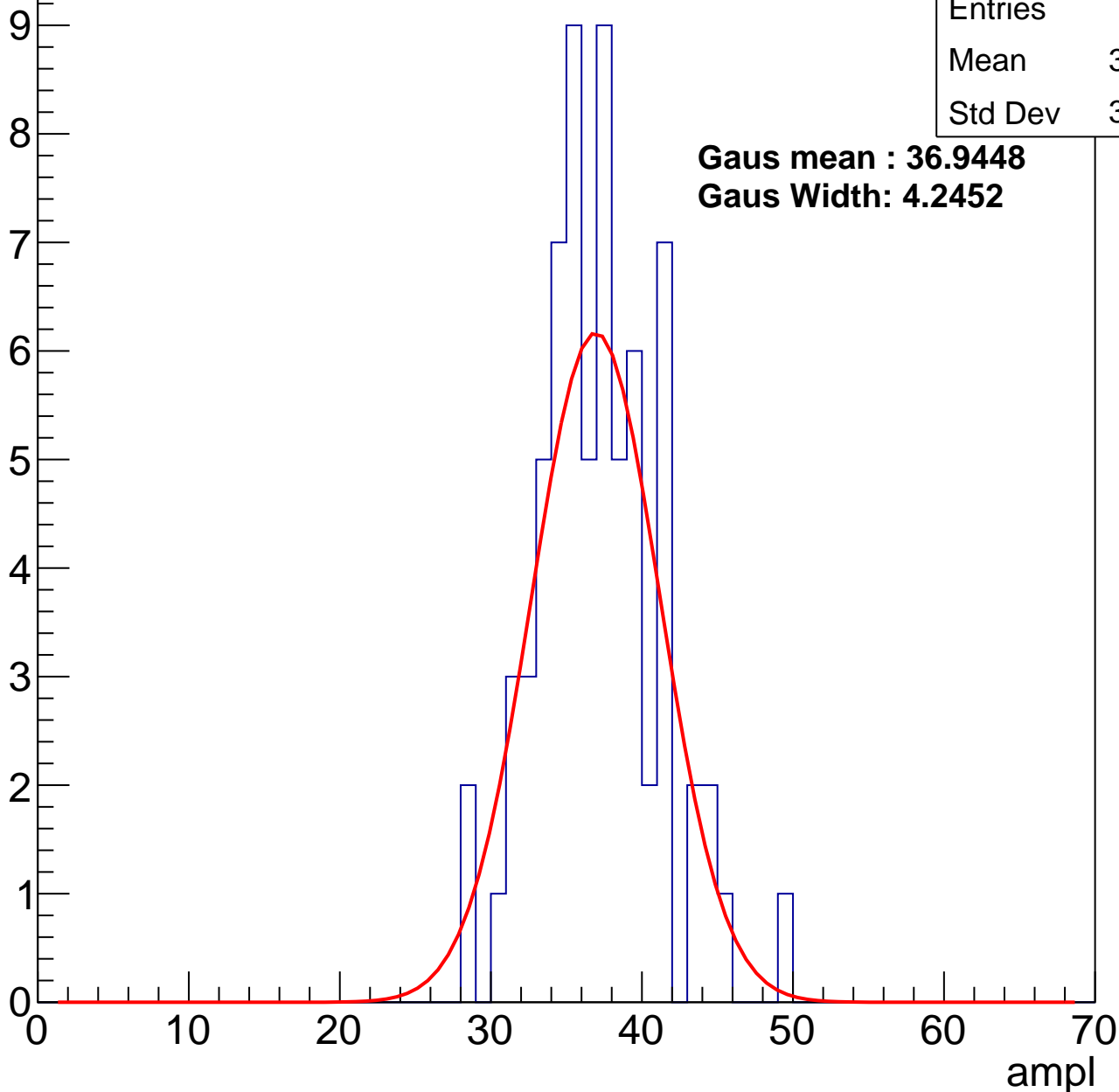
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	70
Mean	36.64
Std Dev	3.975

**Gaus mean : 36.9448**

**Gaus Width: 4.2452**



# B1L102S, U12-ch100, adc2

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	67
Mean	43.04
Std Dev	3.638

**Gaus mean : 43.2087**

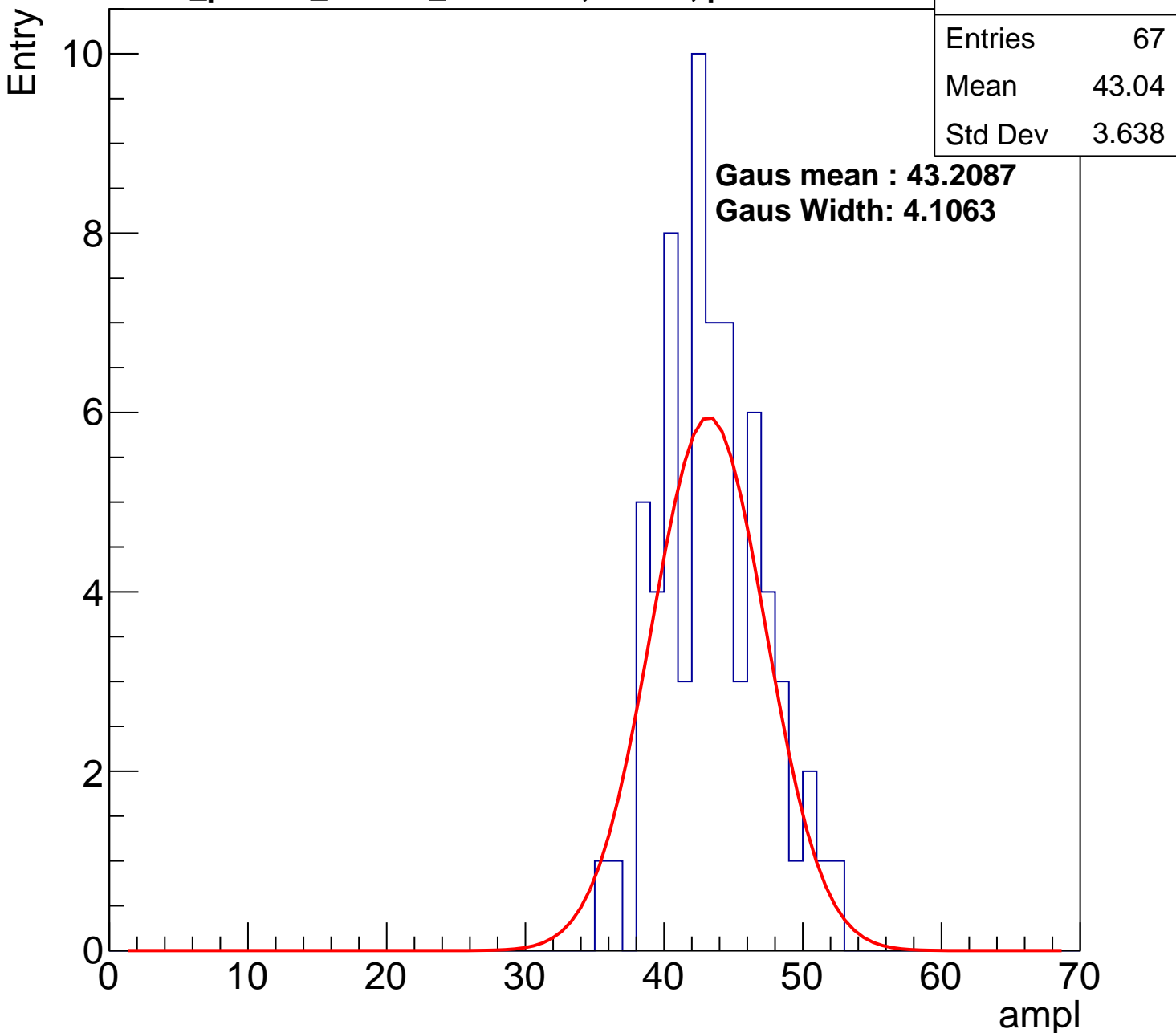
**Gaus Width: 4.1063**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

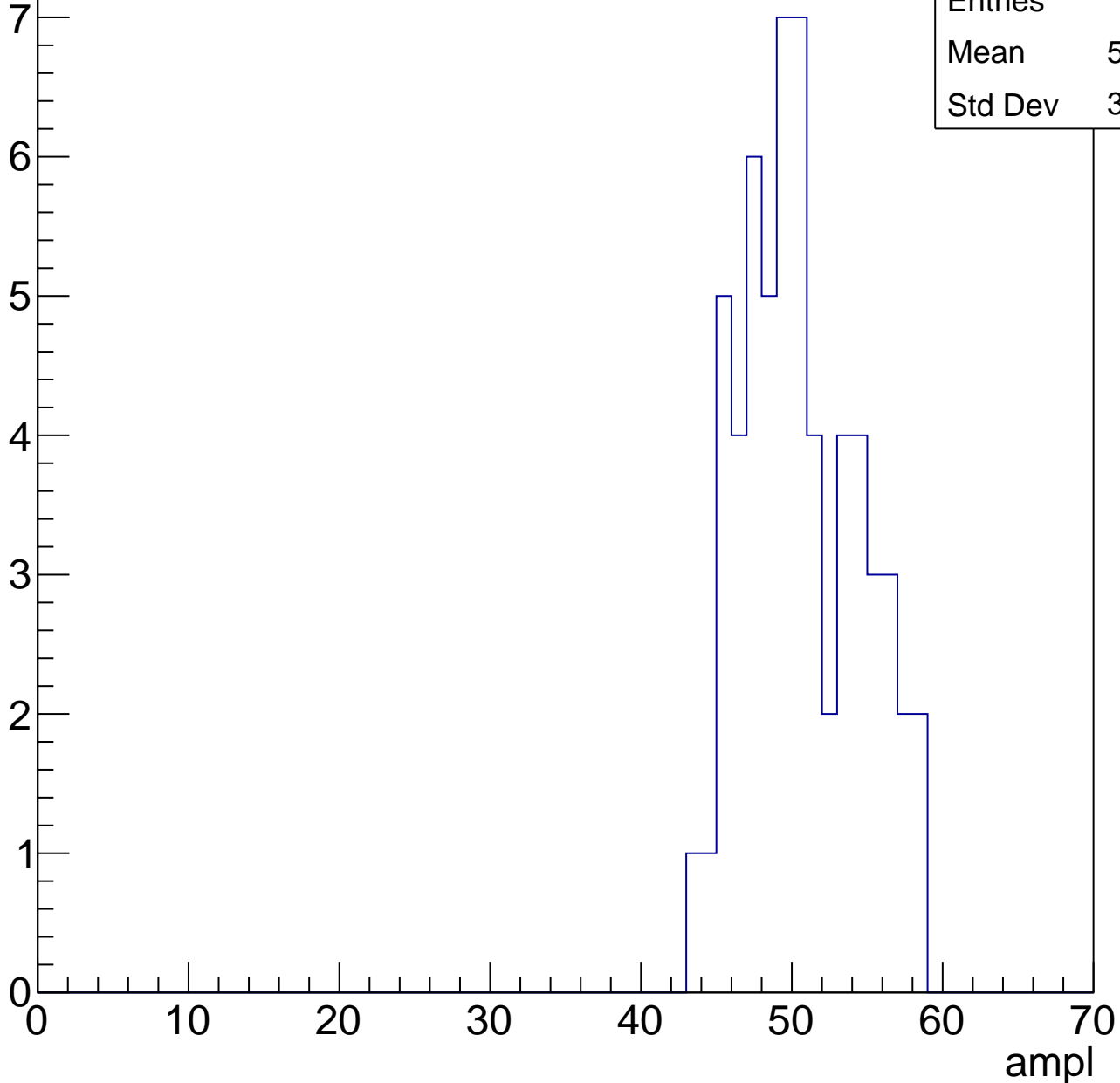


# B1L102S, U12-ch100, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	60
Mean	50.17
Std Dev	3.817

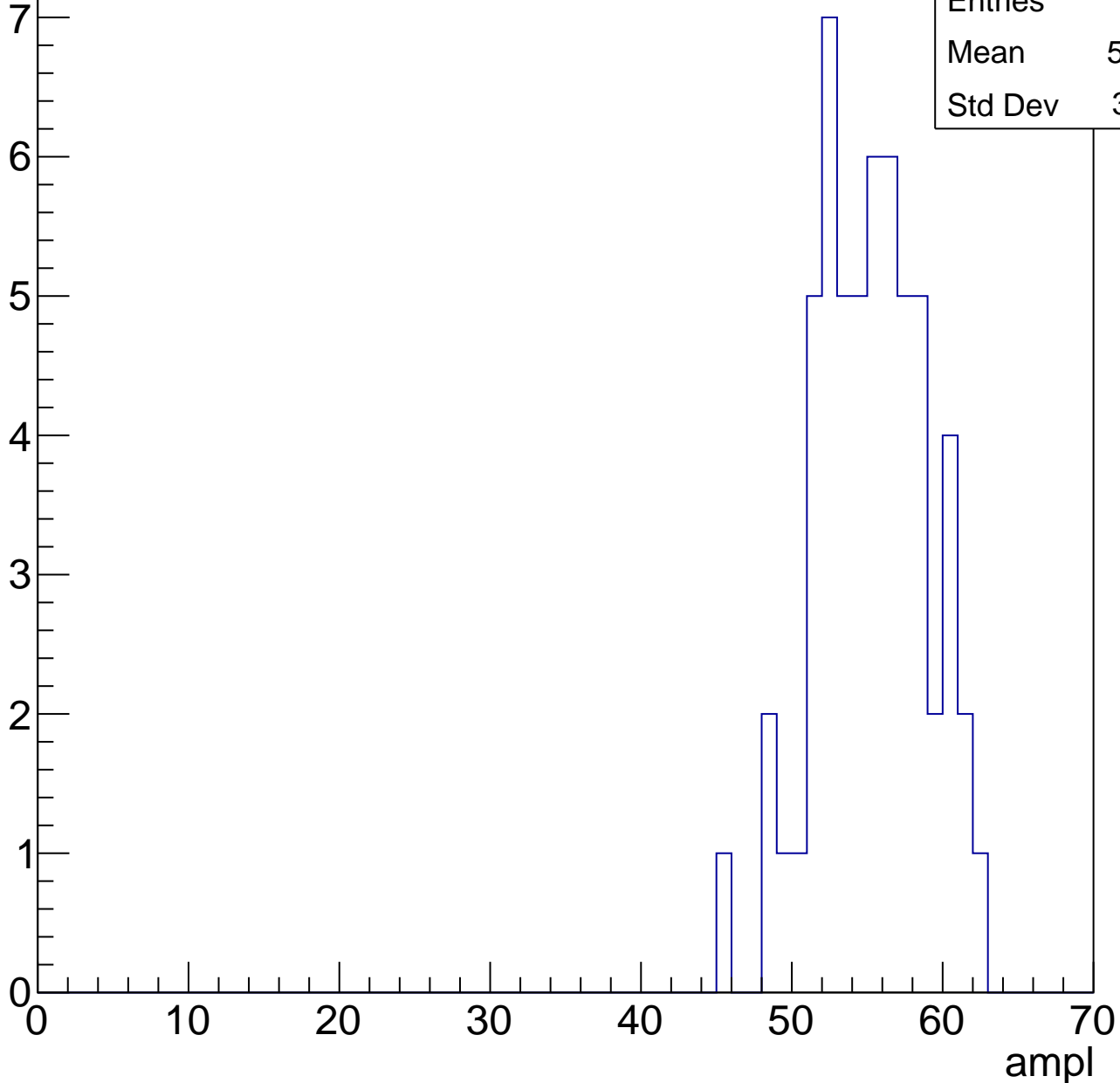


# B1L102S, U12-ch100, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	58
Mean	54.78
Std Dev	3.591



# B1L102S, U12-ch100, adc5

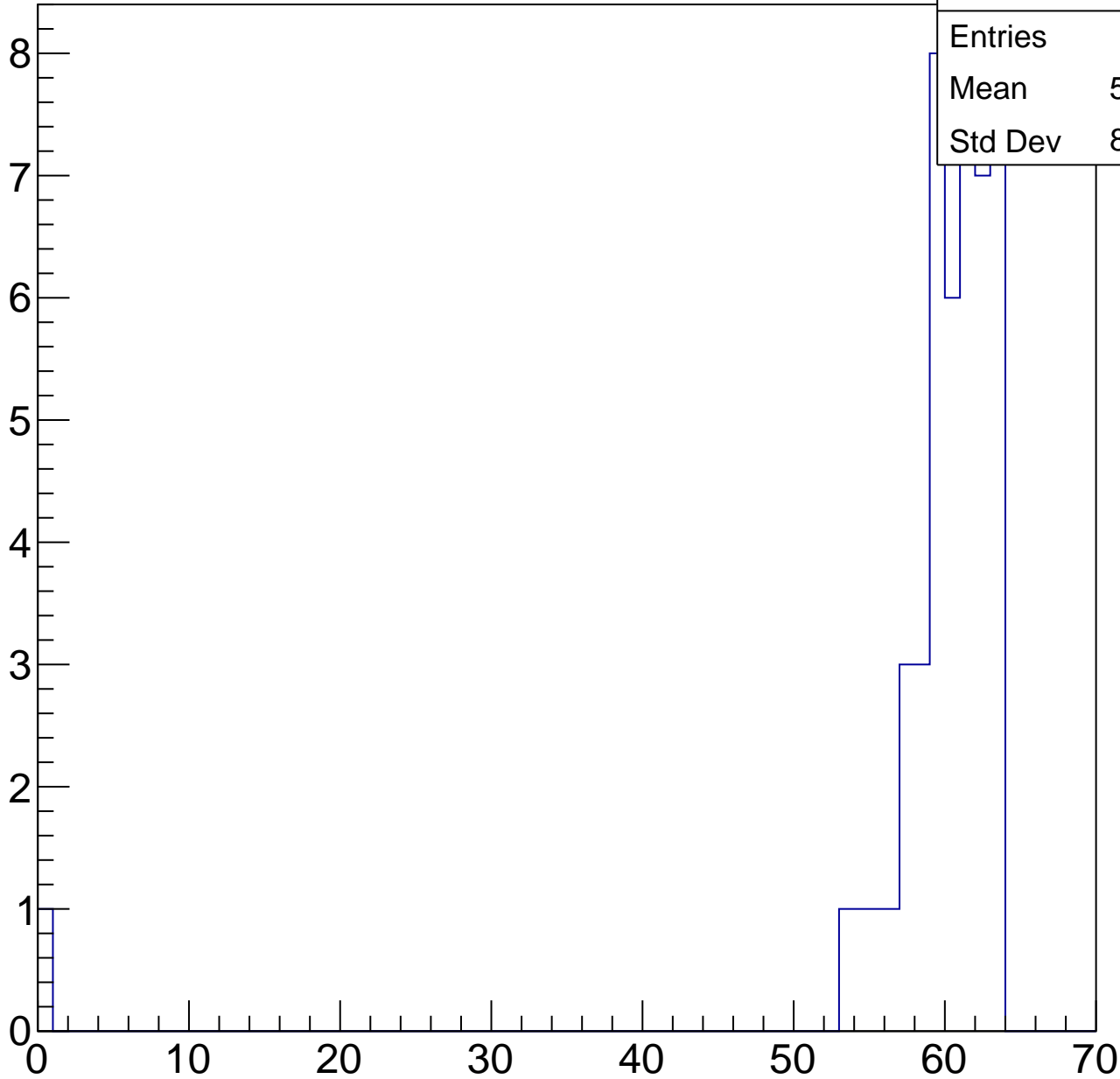
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	48
Mean	58.77
Std Dev	8.907

ampl



# B1L102S, U12-ch100, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U12-ch100, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	2
Mean	11
Std Dev	11

# B1L102S, U12-ch101, adc0

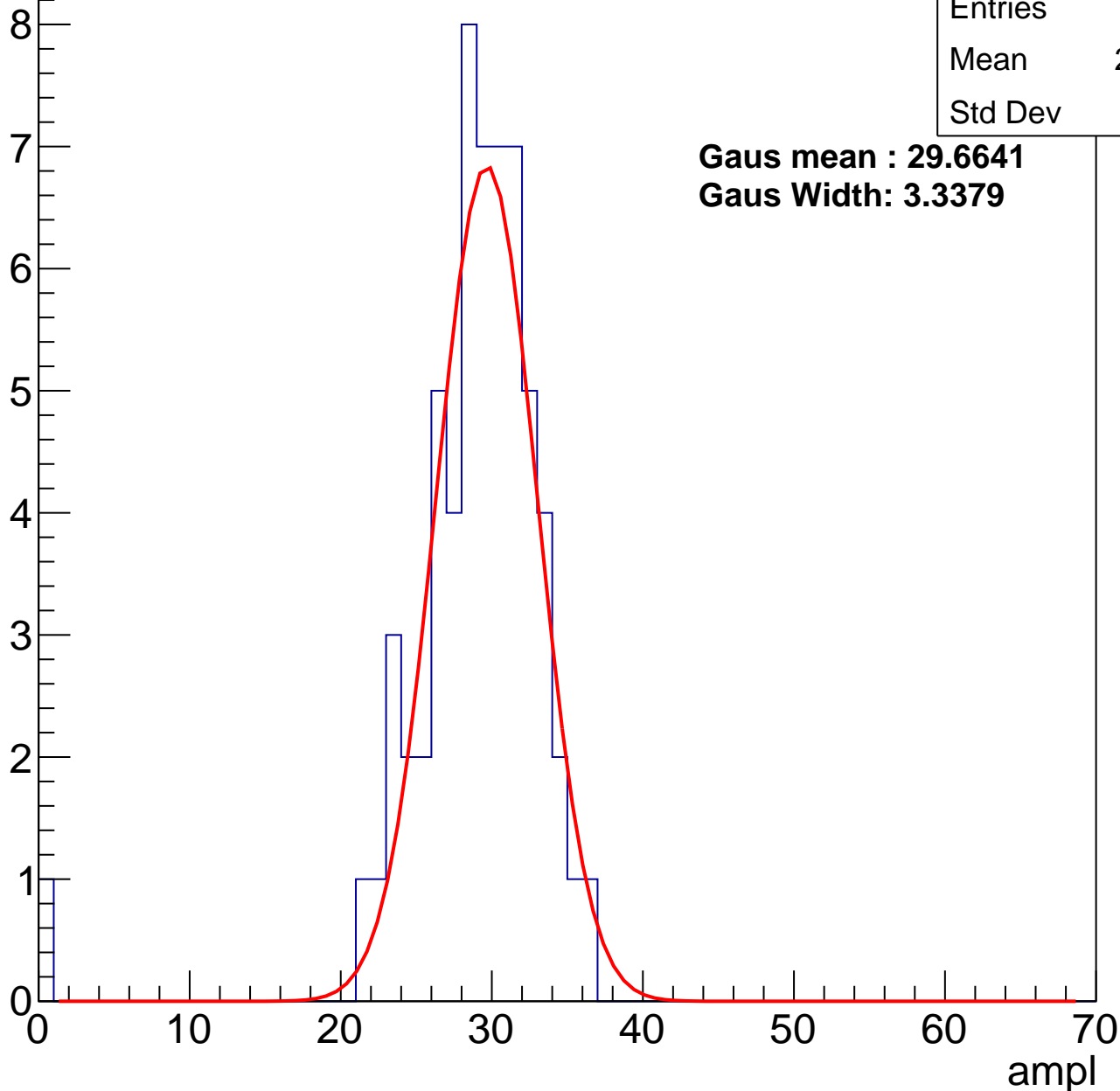
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	28.41
Std Dev	4.91

**Gaus mean : 29.6641**

**Gaus Width: 3.3379**



# B1L102S, U12-ch101, adc1

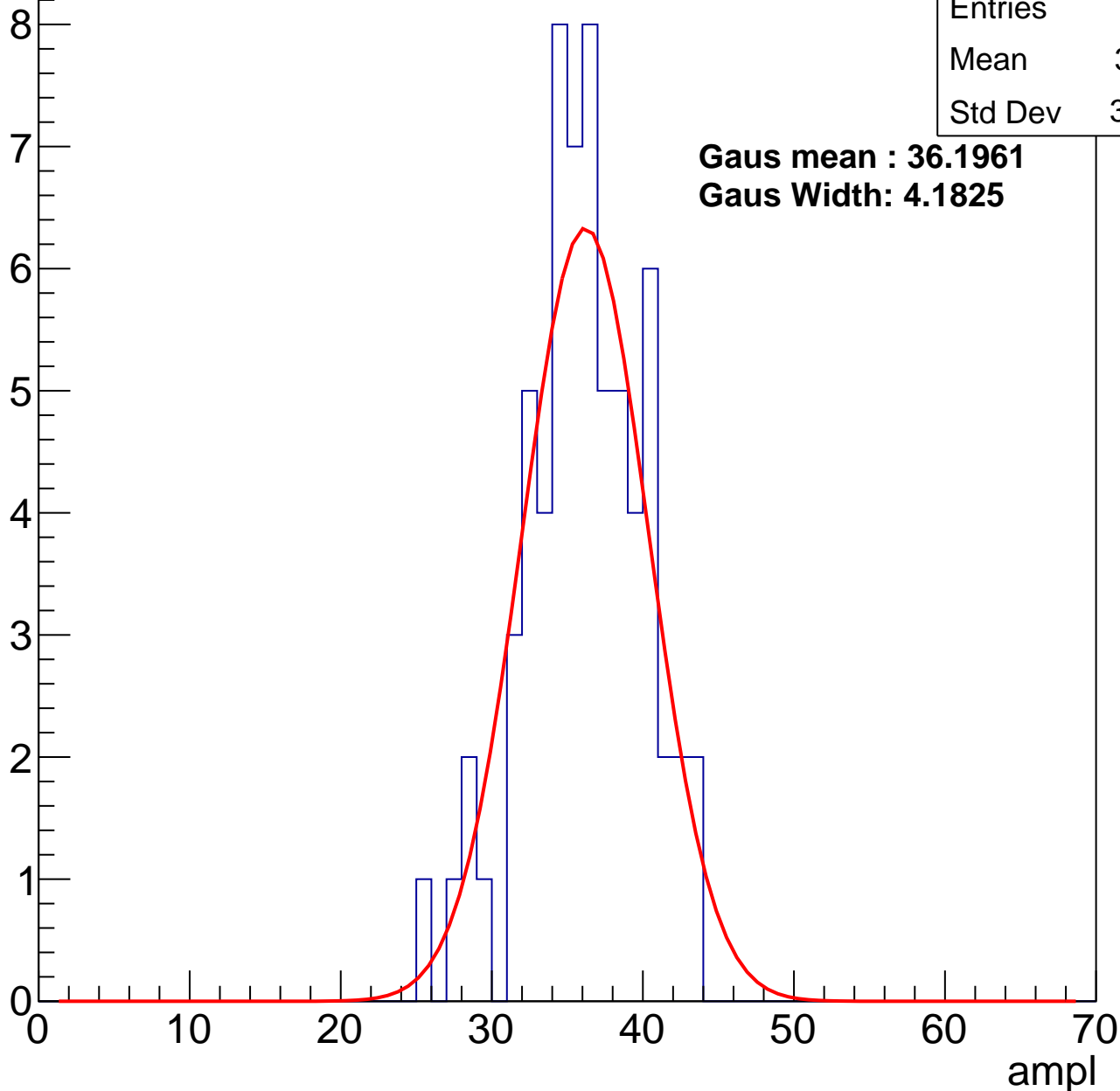
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	35.61
Std Dev	3.845

**Gaus mean : 36.1961**

**Gaus Width: 4.1825**



# B1L102S, U12-ch101, adc2

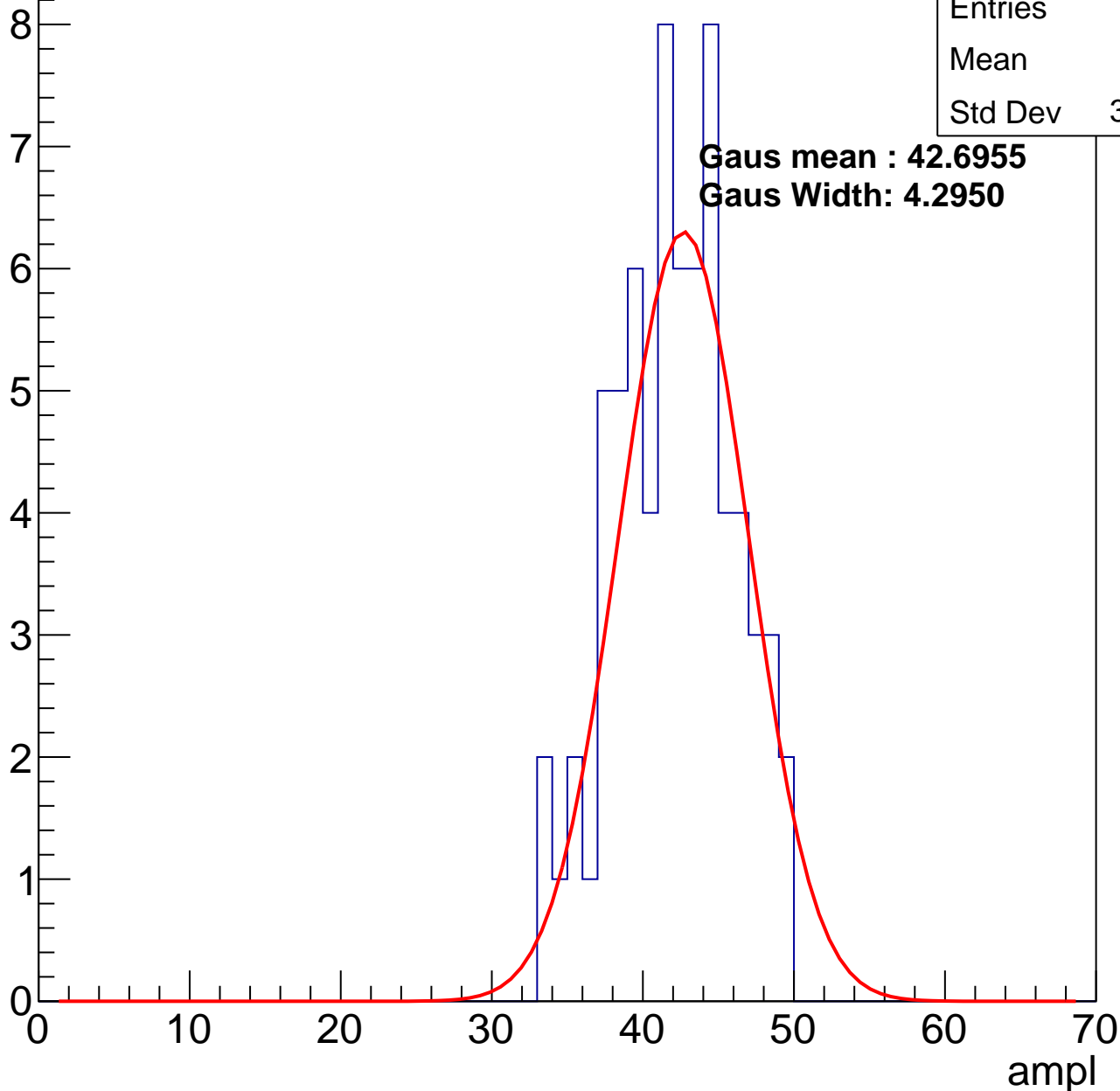
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	70
Mean	41.6
Std Dev	3.874

**Gaus mean : 42.6955**

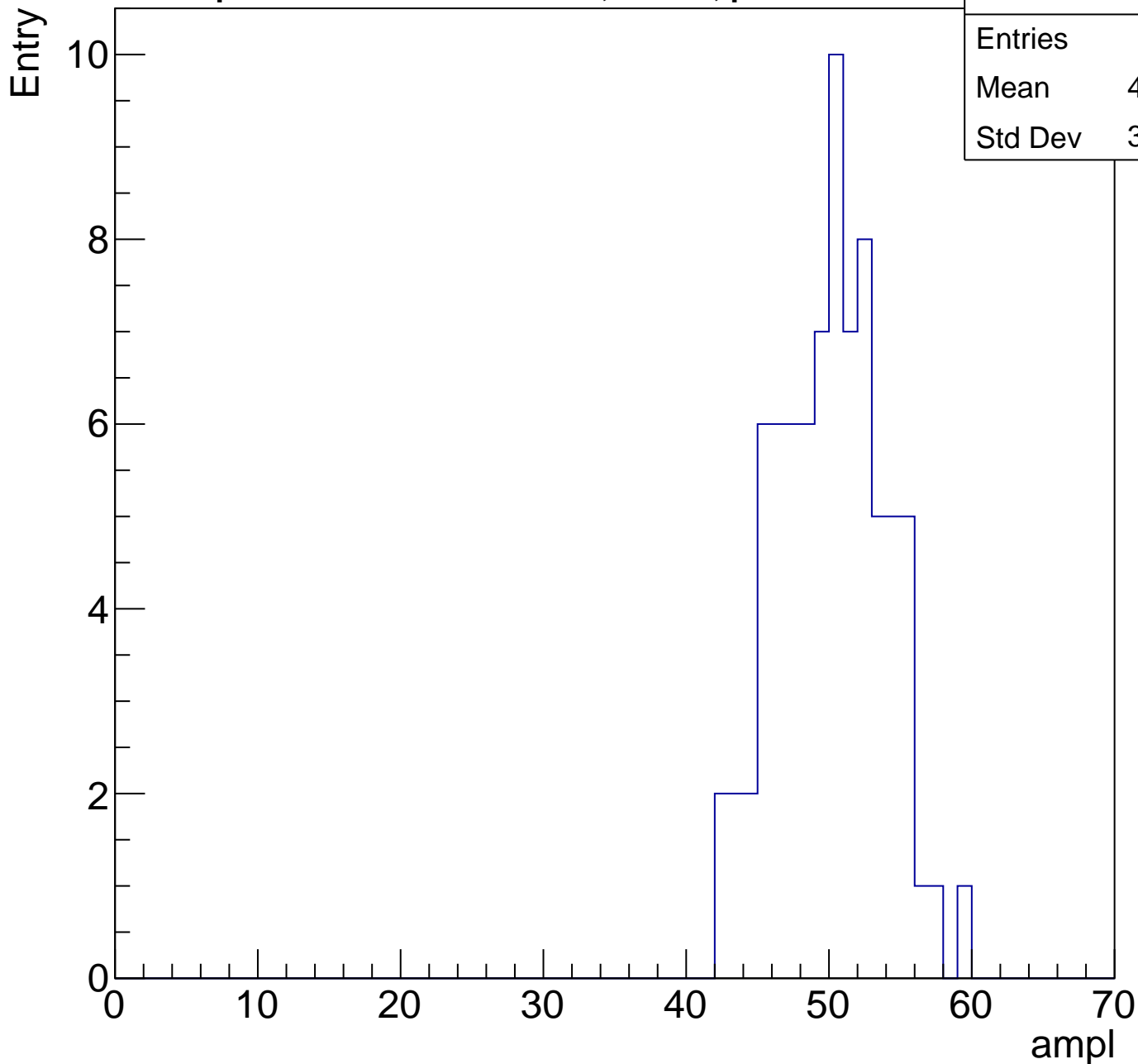
**Gaus Width: 4.2950**



# B1L102S, U12-ch101, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	80
Mean	49.65
Std Dev	3.664

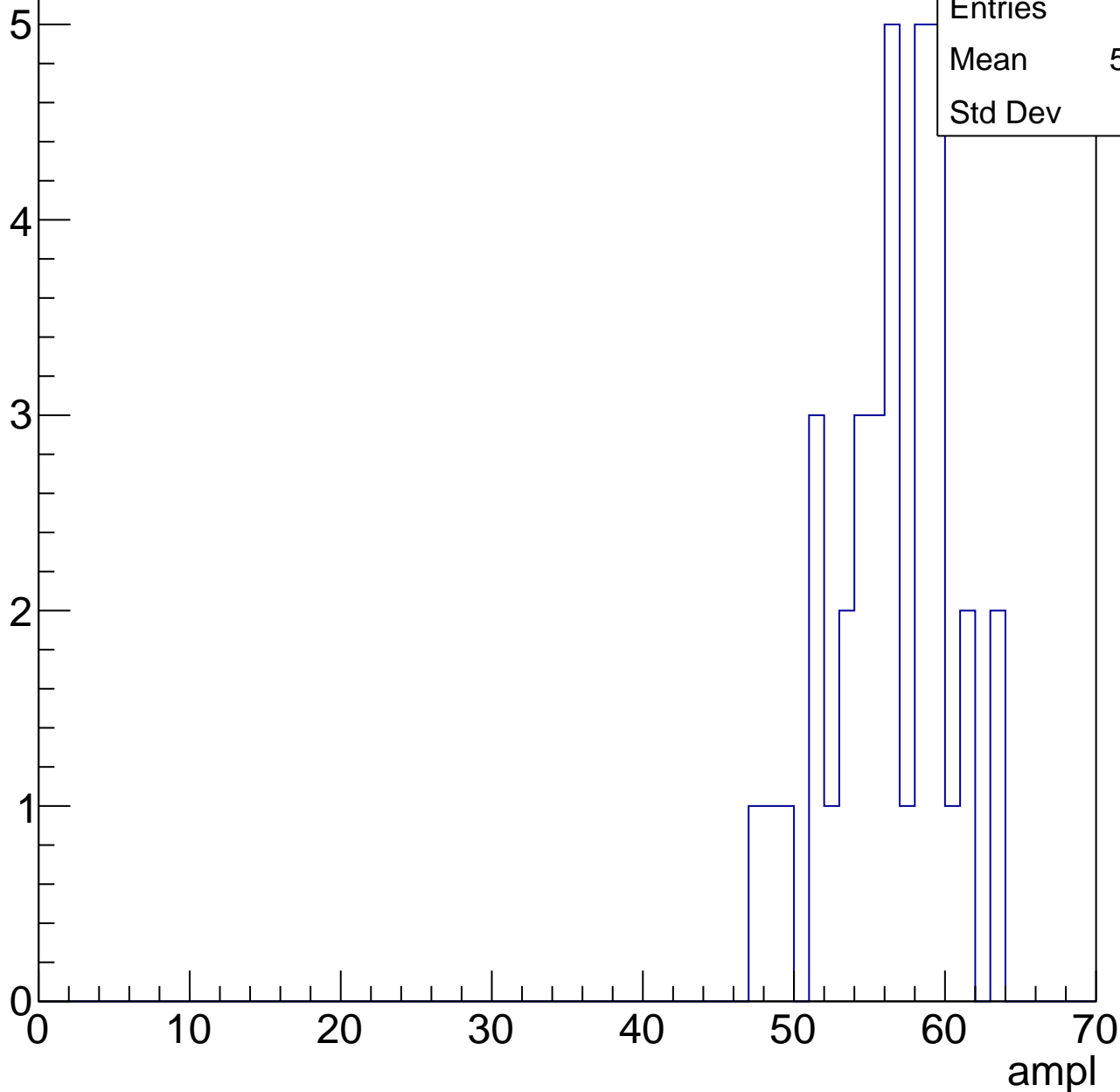


# B1L102S, U12-ch101, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	36
Mean	55.89
Std Dev	3.9

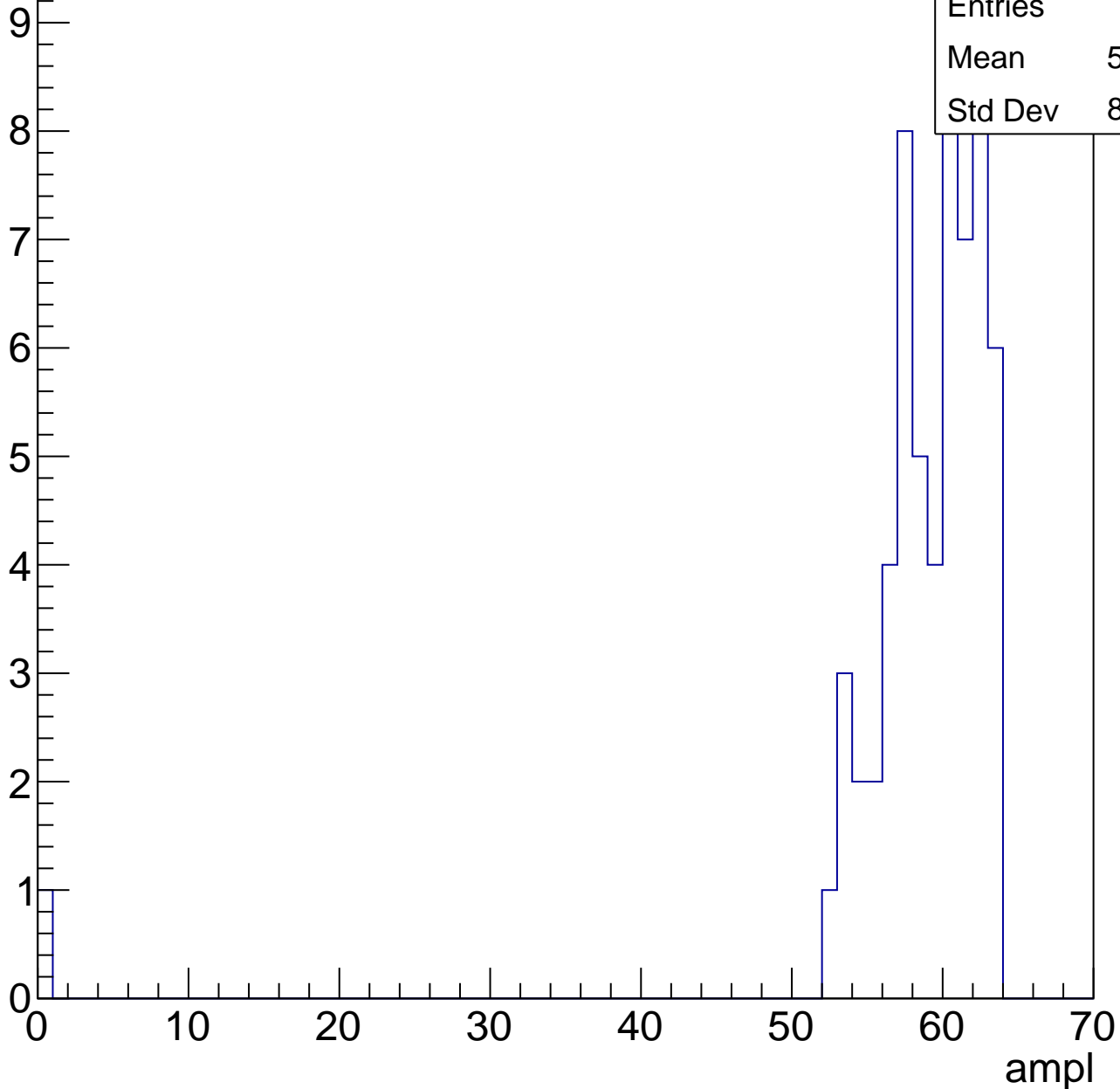


# B1L102S, U12-ch101, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

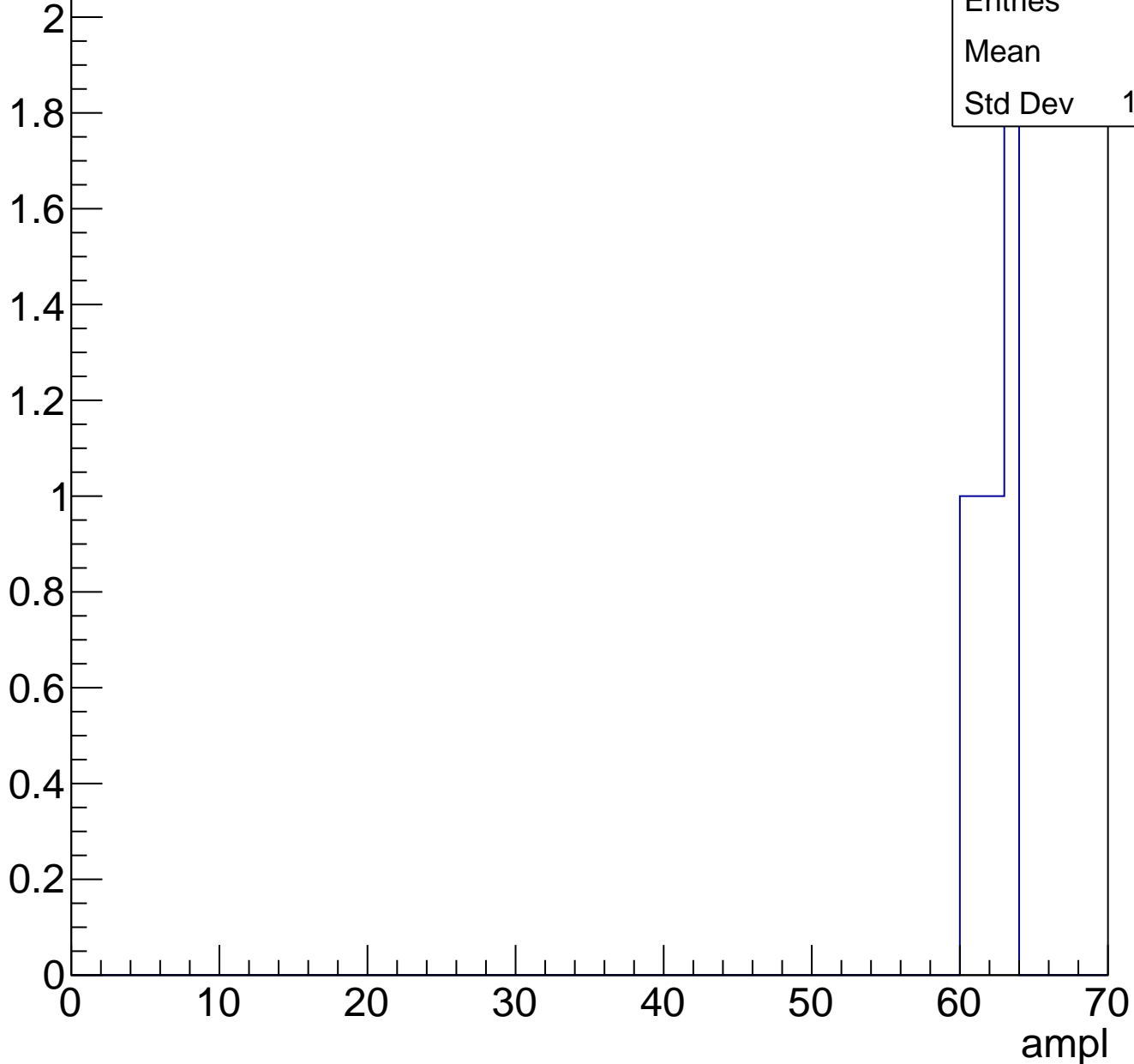
Entries	60
Mean	57.97
Std Dev	8.105



# B1L102S, U12-ch101, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U12-ch101, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

1

0.8

0.6

0.4

0.2

0

0

10

20

30

40

50

60

70

ampl

Entries

0

Mean

0

Std Dev

0

# B1L102S, U12-ch102, adc0

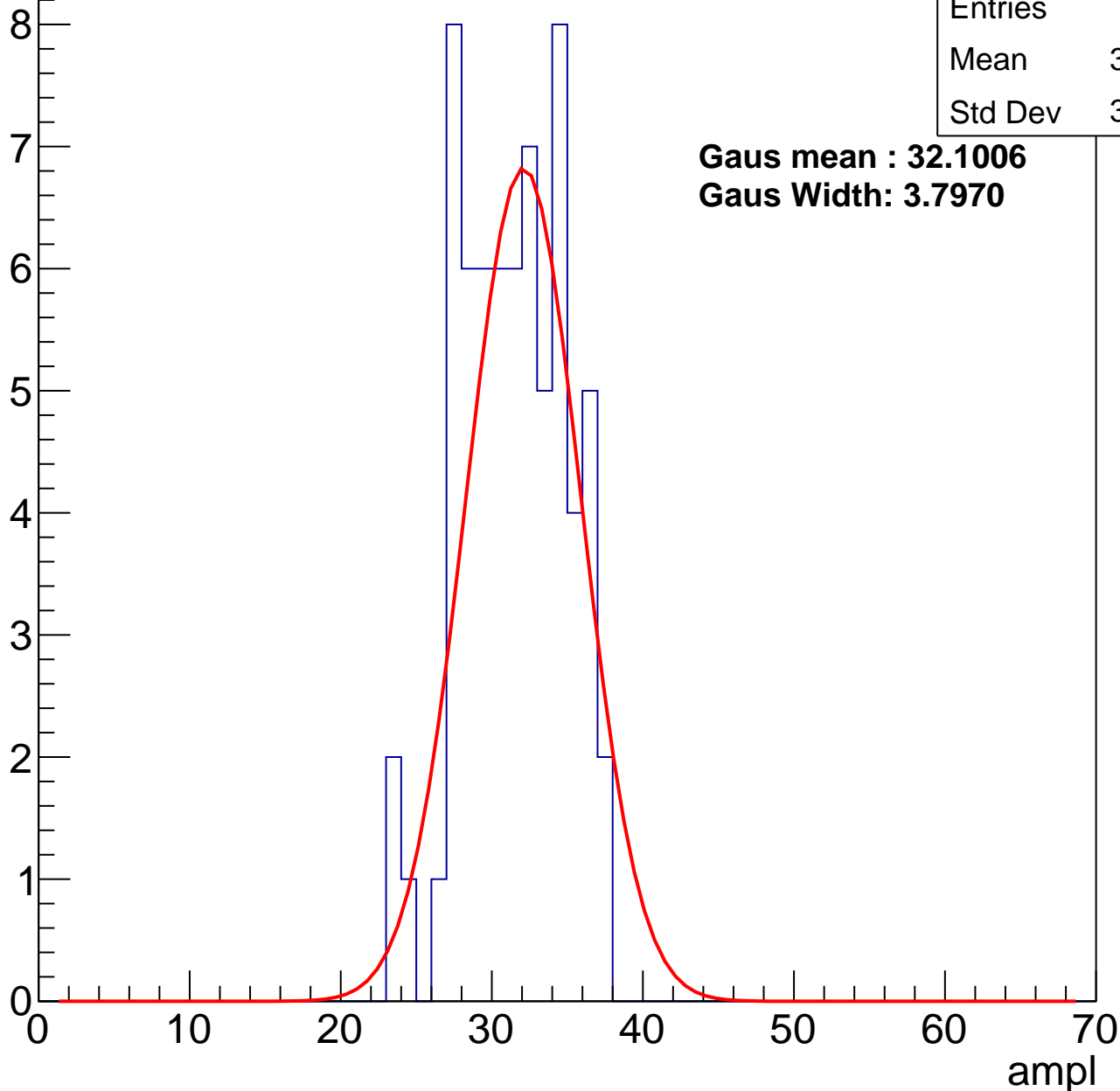
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	67
Mean	30.97
Std Dev	3.399

**Gaus mean : 32.1006**

**Gaus Width: 3.7970**



# B1L102S, U12-ch102, adc1

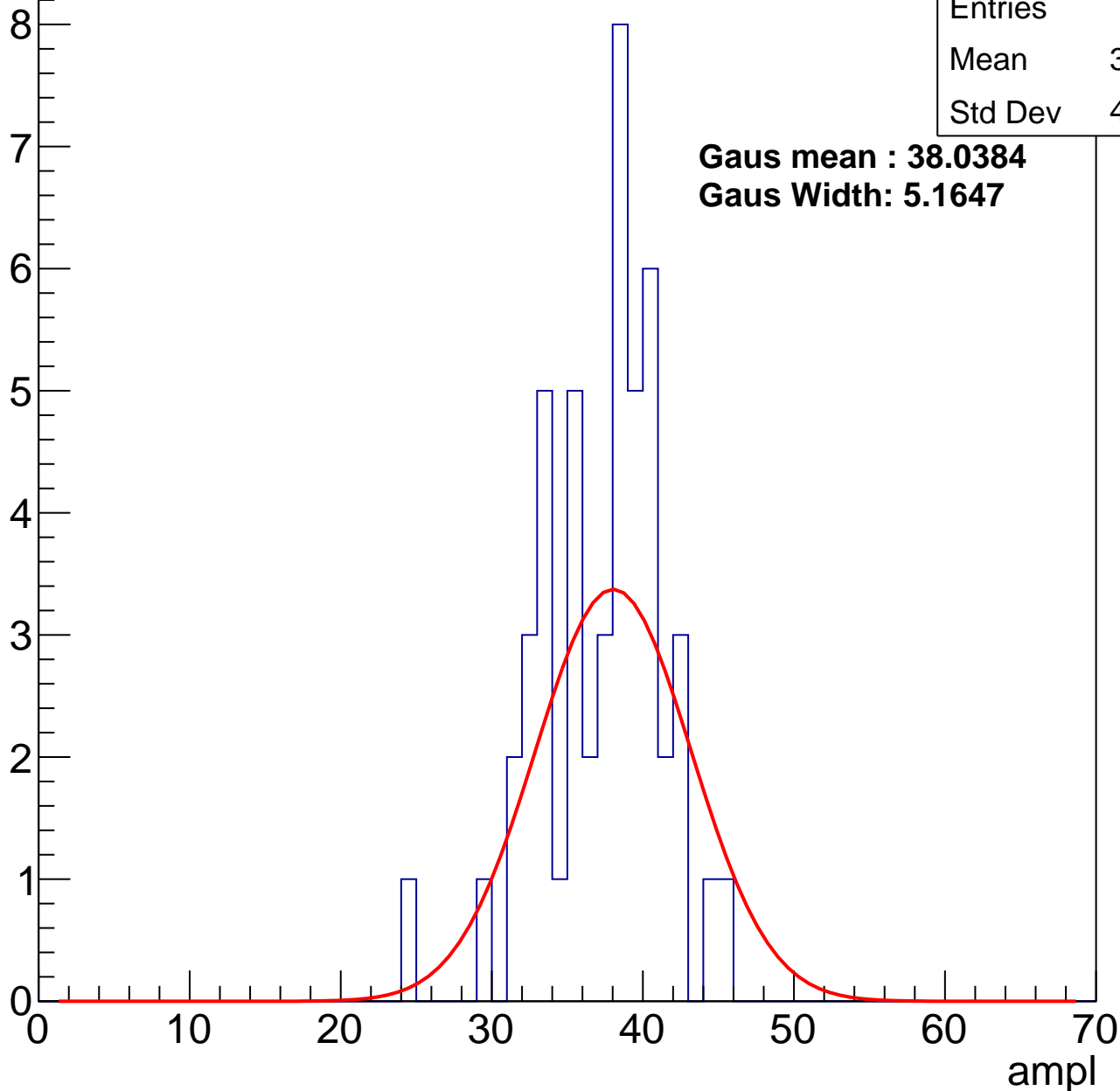
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	49
Mean	36.82
Std Dev	4.019

**Gaus mean : 38.0384**

**Gaus Width: 5.1647**



# B1L102S, U12-ch102, adc2

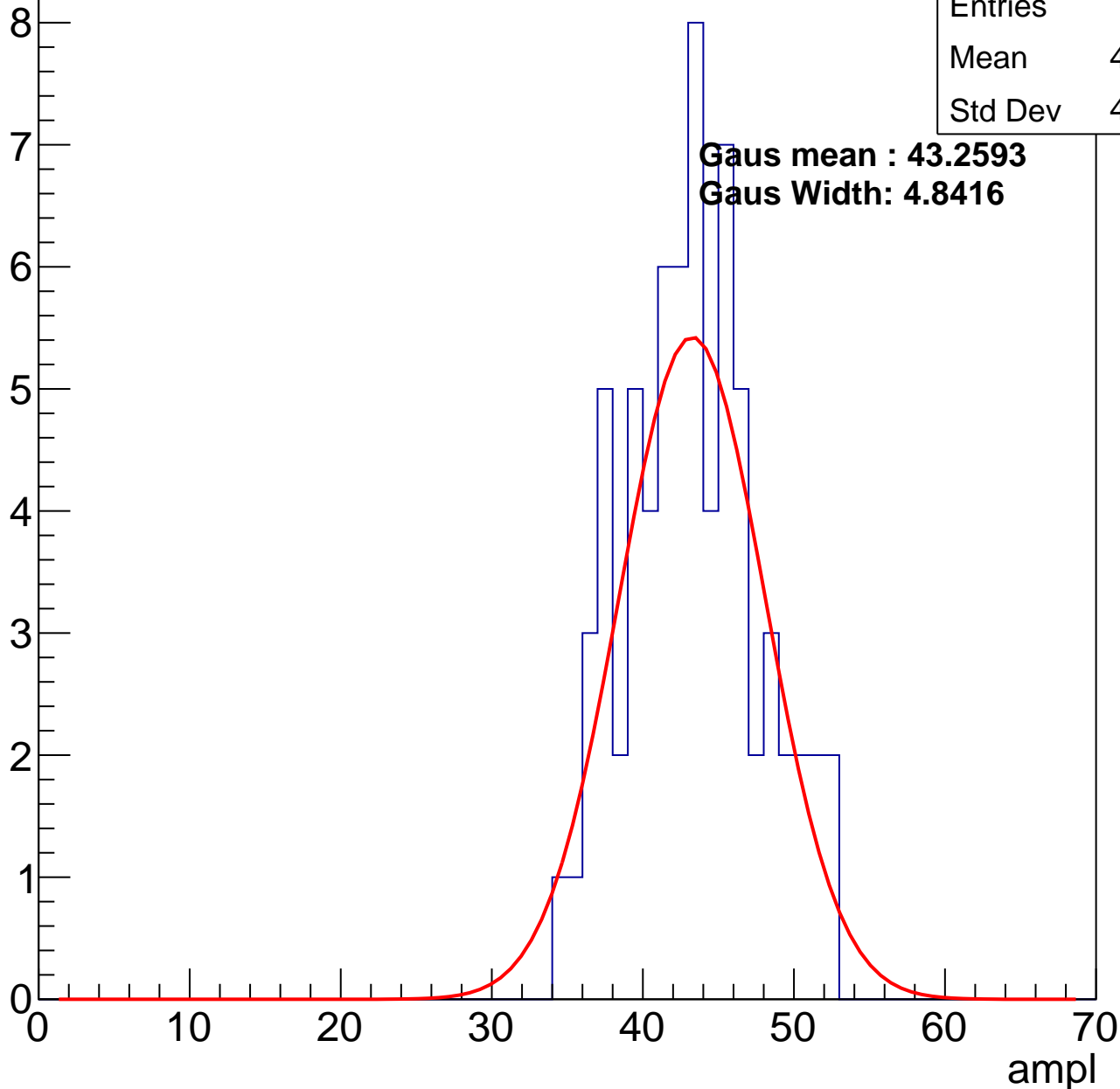
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	70
Mean	42.83
Std Dev	4.326

**Gaus mean : 43.2593**

**Gaus Width: 4.8416**

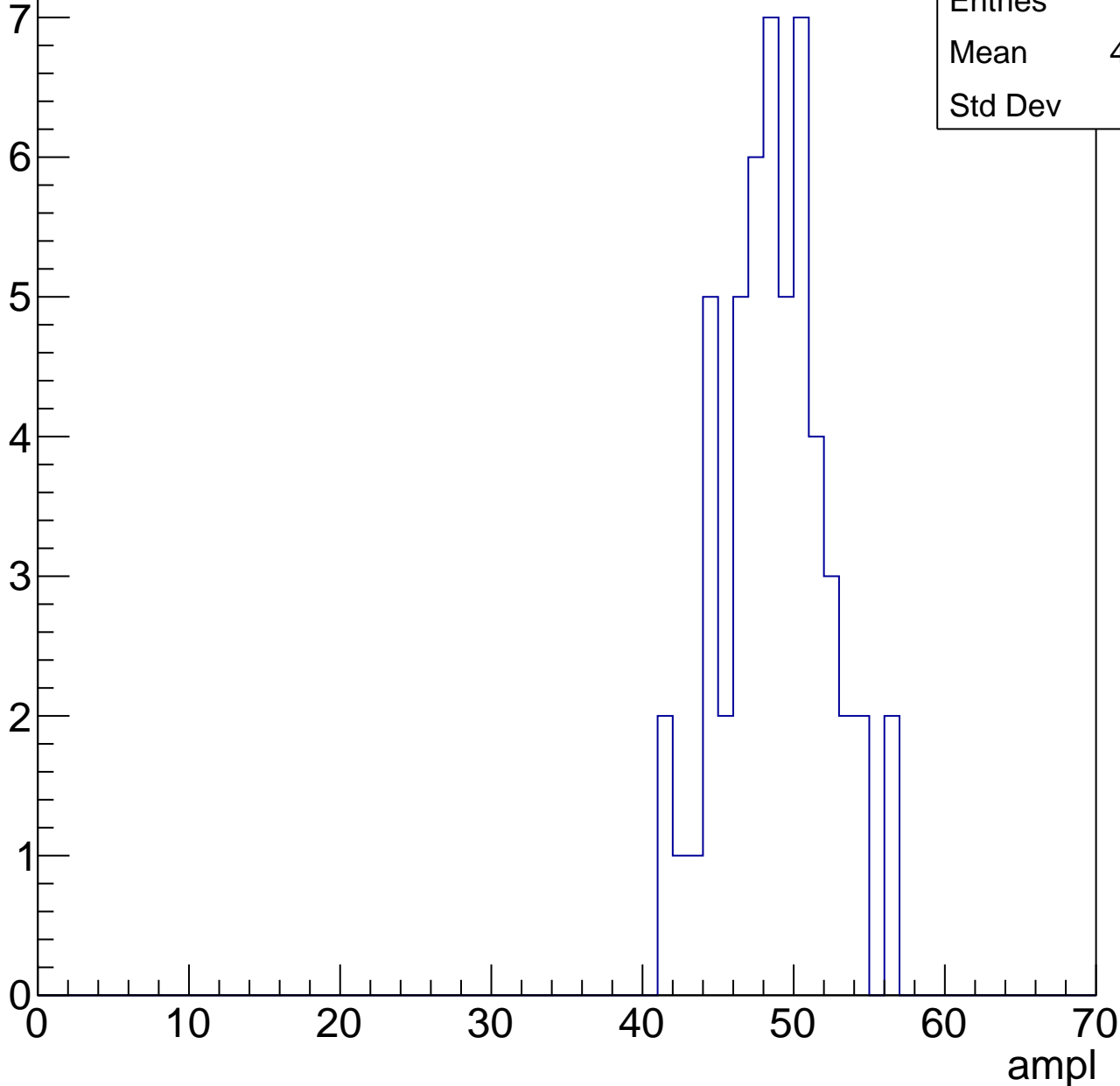


# B1L102S, U12-ch102, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	54
Mean	48.26
Std Dev	3.46

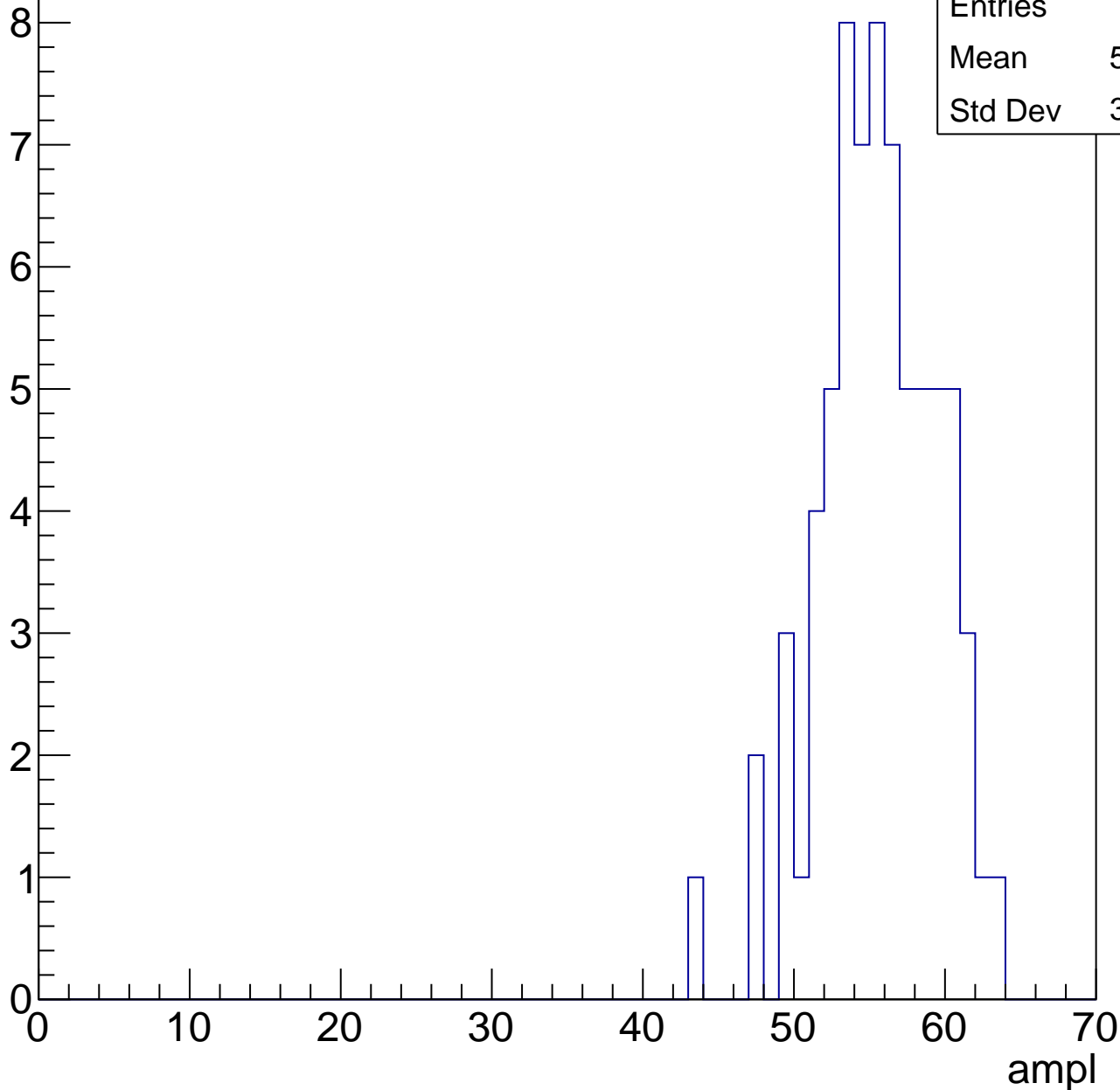


# B1L102S, U12-ch102, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	71
Mean	55.07
Std Dev	3.847

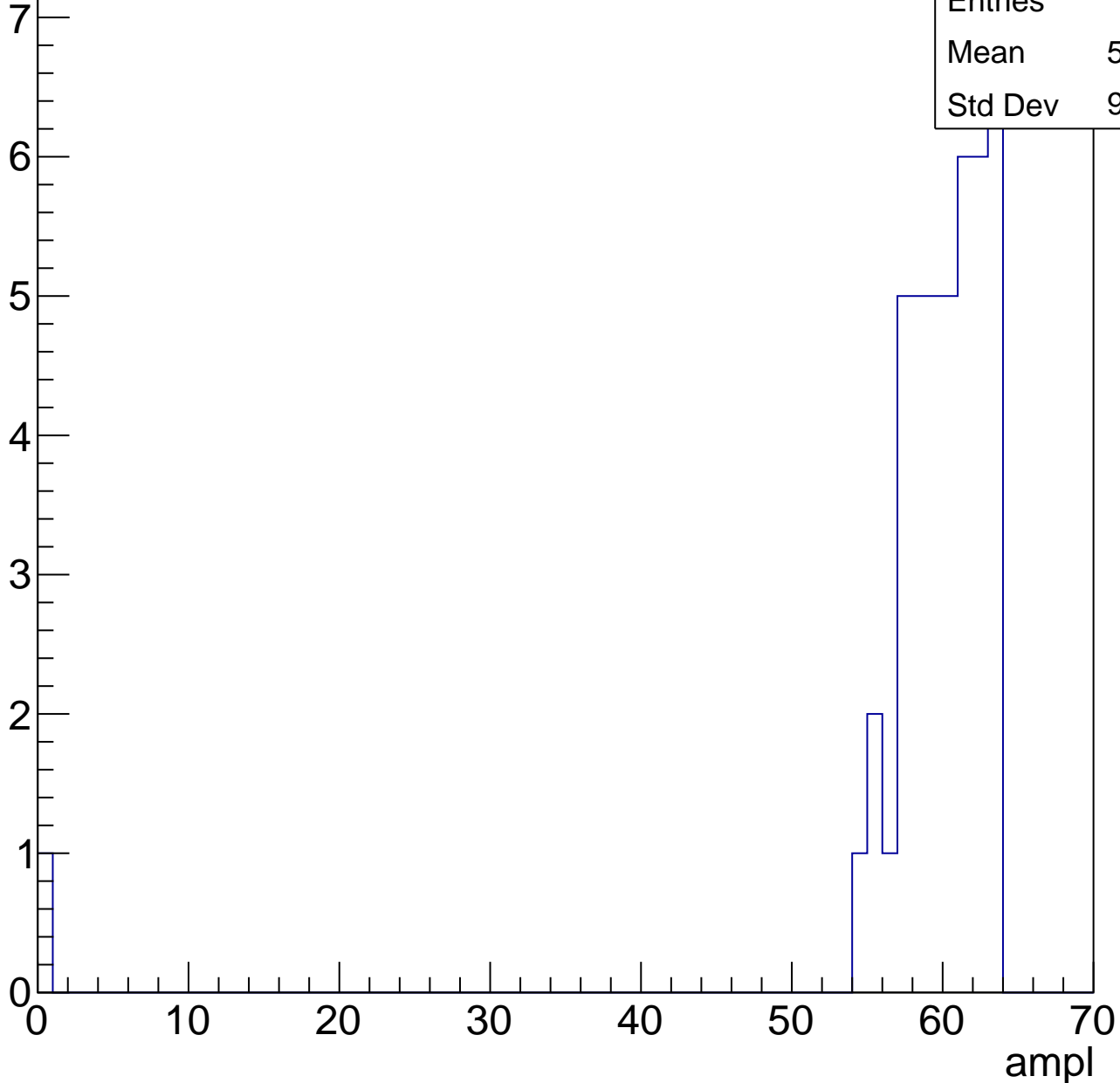


# B1L102S, U12-ch102, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

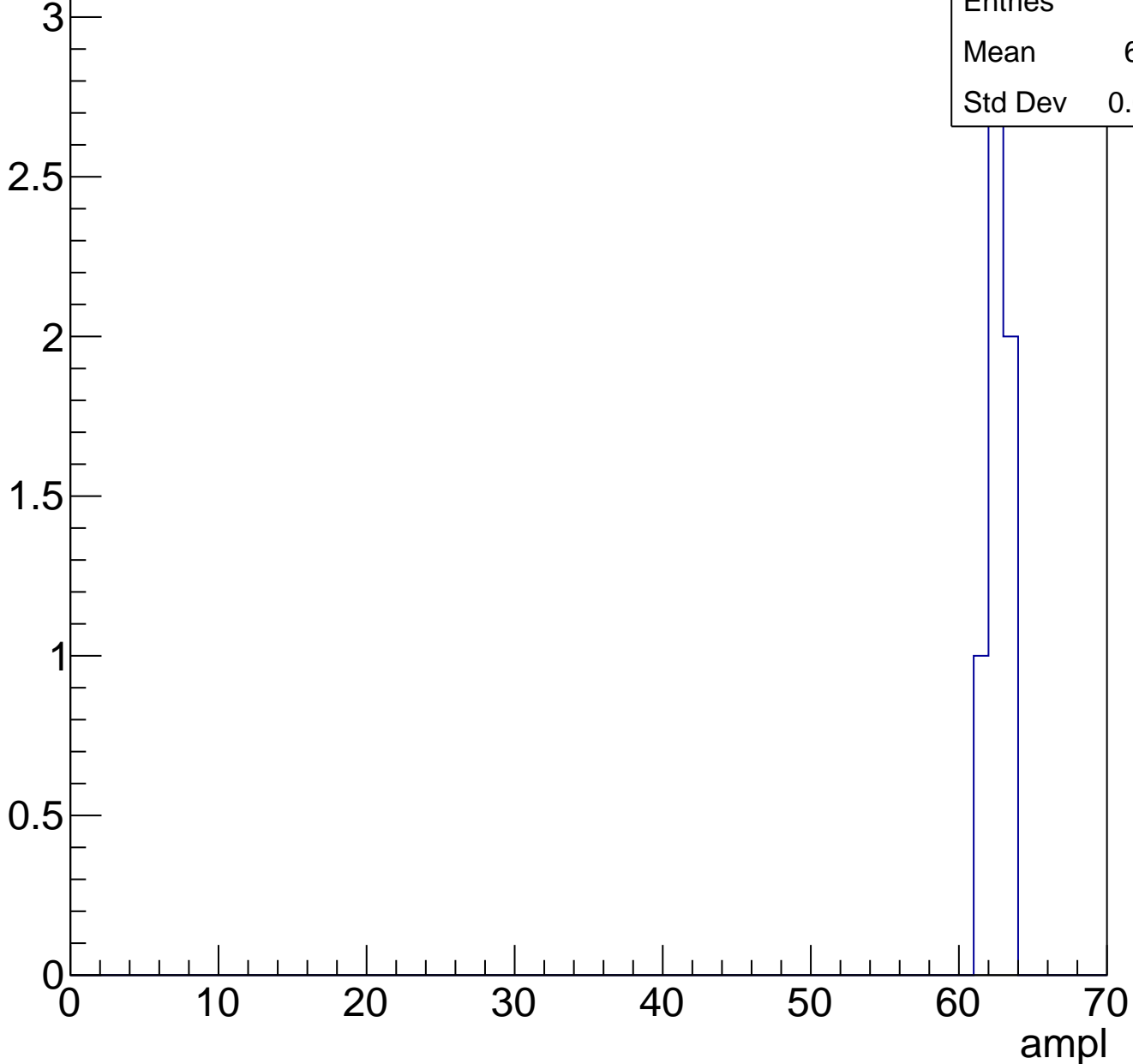
Entries	44
Mean	58.39
Std Dev	9.232



# B1L102S, U12-ch102, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U12-ch102, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

1  
0.8  
0.6  
0.4  
0.2  
0

Entries	1
Mean	22
Std Dev	0

ampl

# B1L102S, U12-ch103, adc0

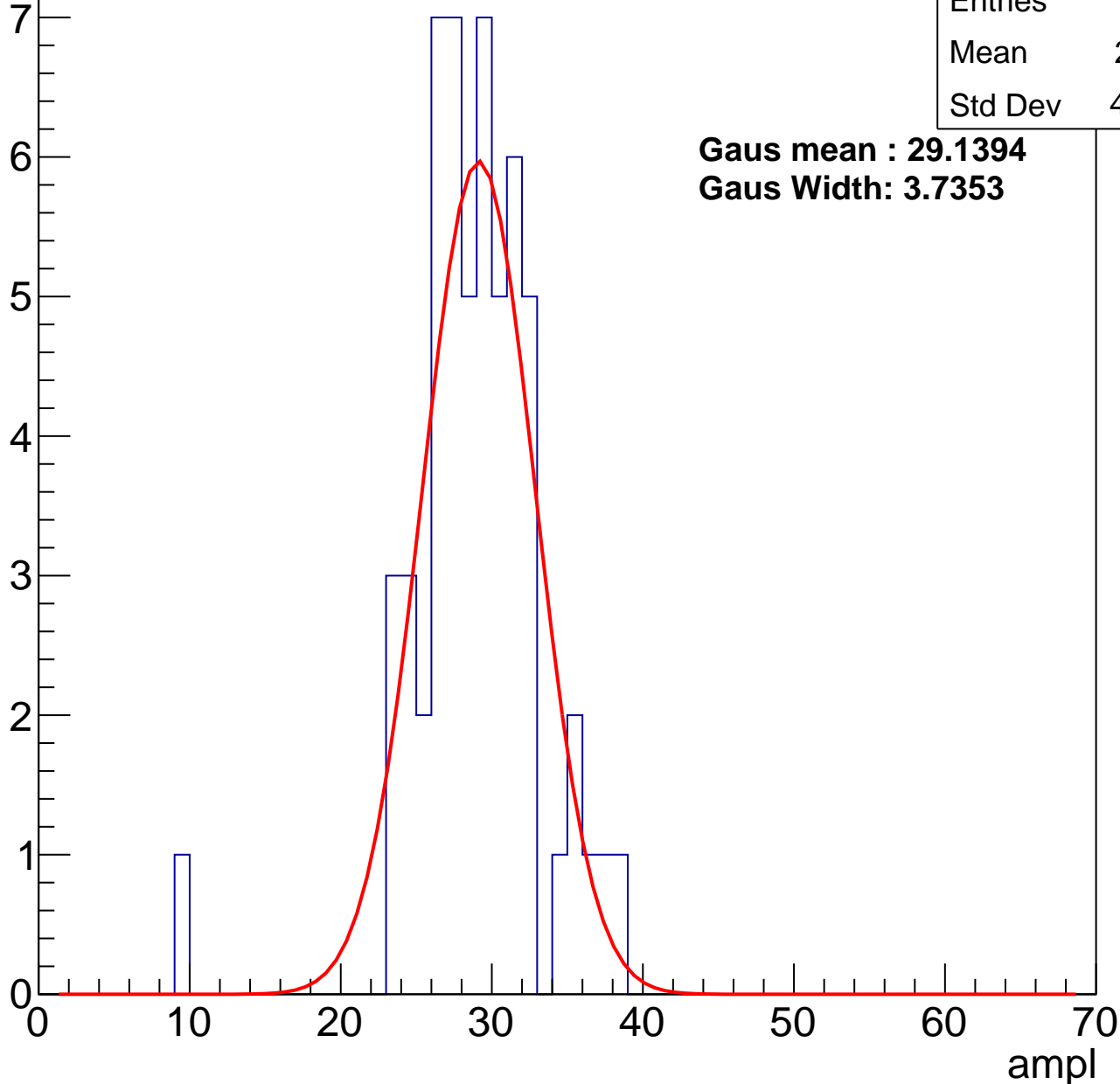
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	57
Mean	28.51
Std Dev	4.317

**Gaus mean : 29.1394**

**Gaus Width: 3.7353**



# B1L102S, U12-ch103, adc1

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	90
Mean	34.51
Std Dev	7.173

**Gaus mean : 36.1595**

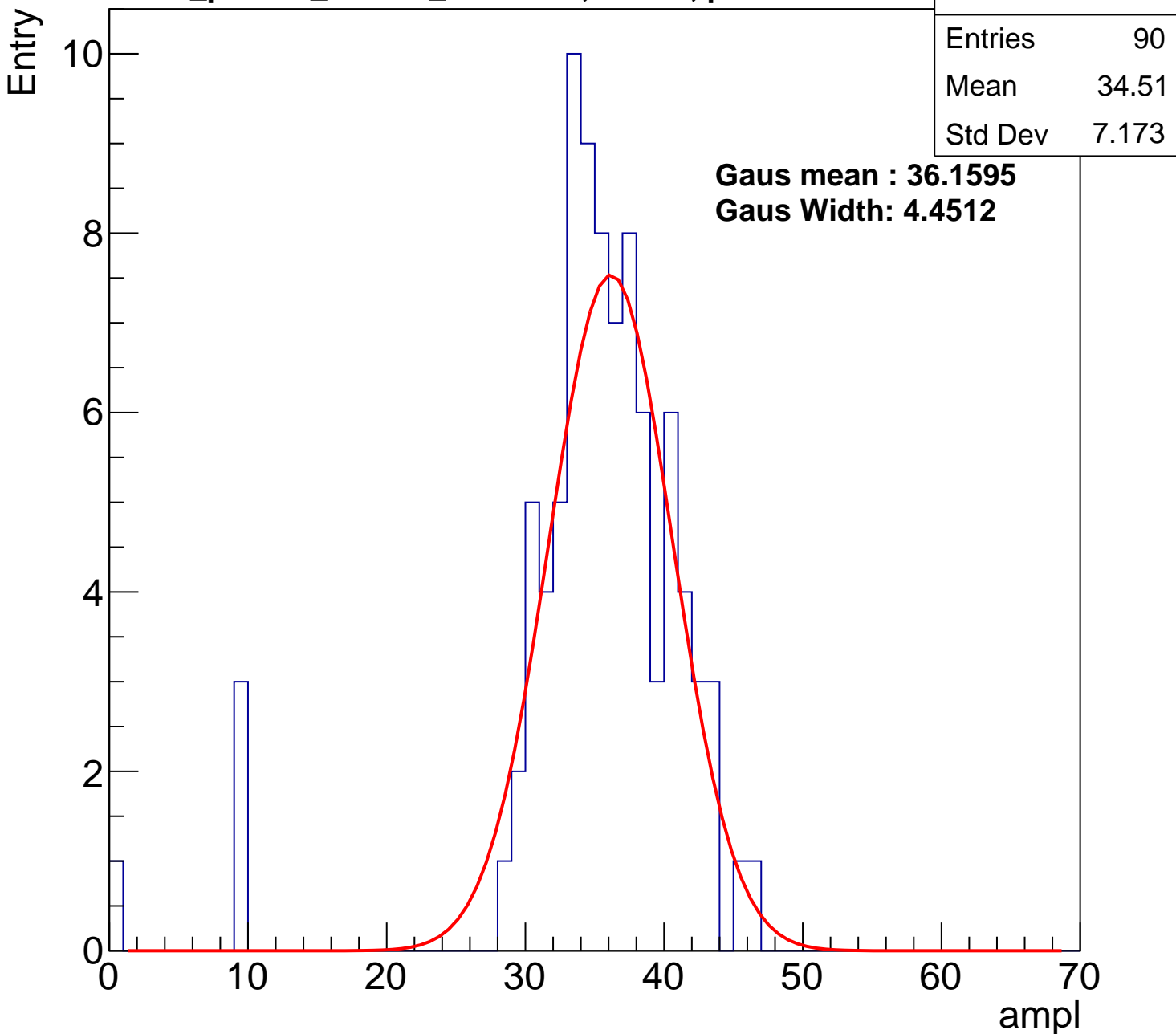
**Gaus Width: 4.4512**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B1L102S, U12-ch103, adc2

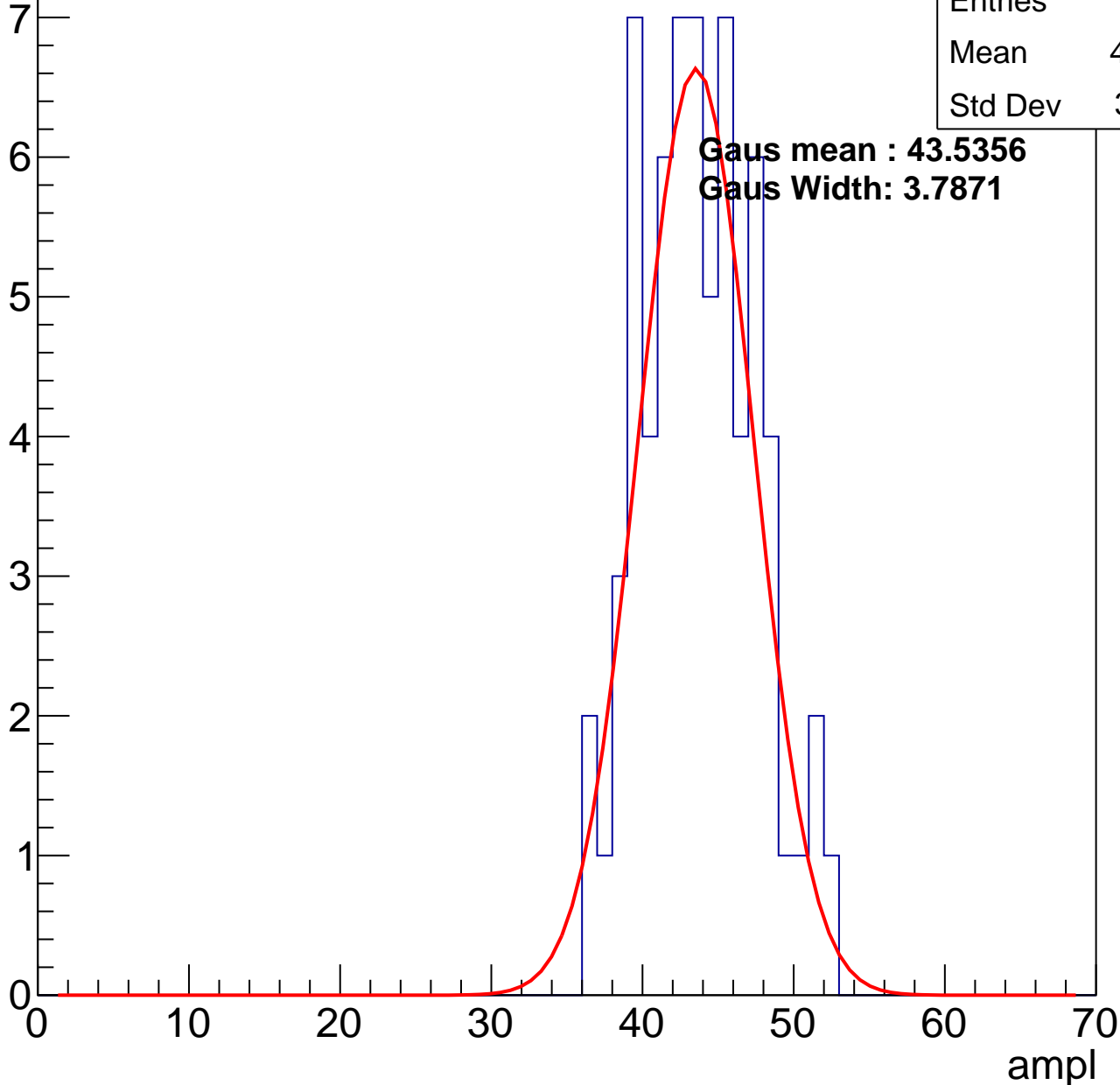
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	43.28
Std Dev	3.721

**Gaus mean : 43.5356**

**Gaus Width: 3.7871**

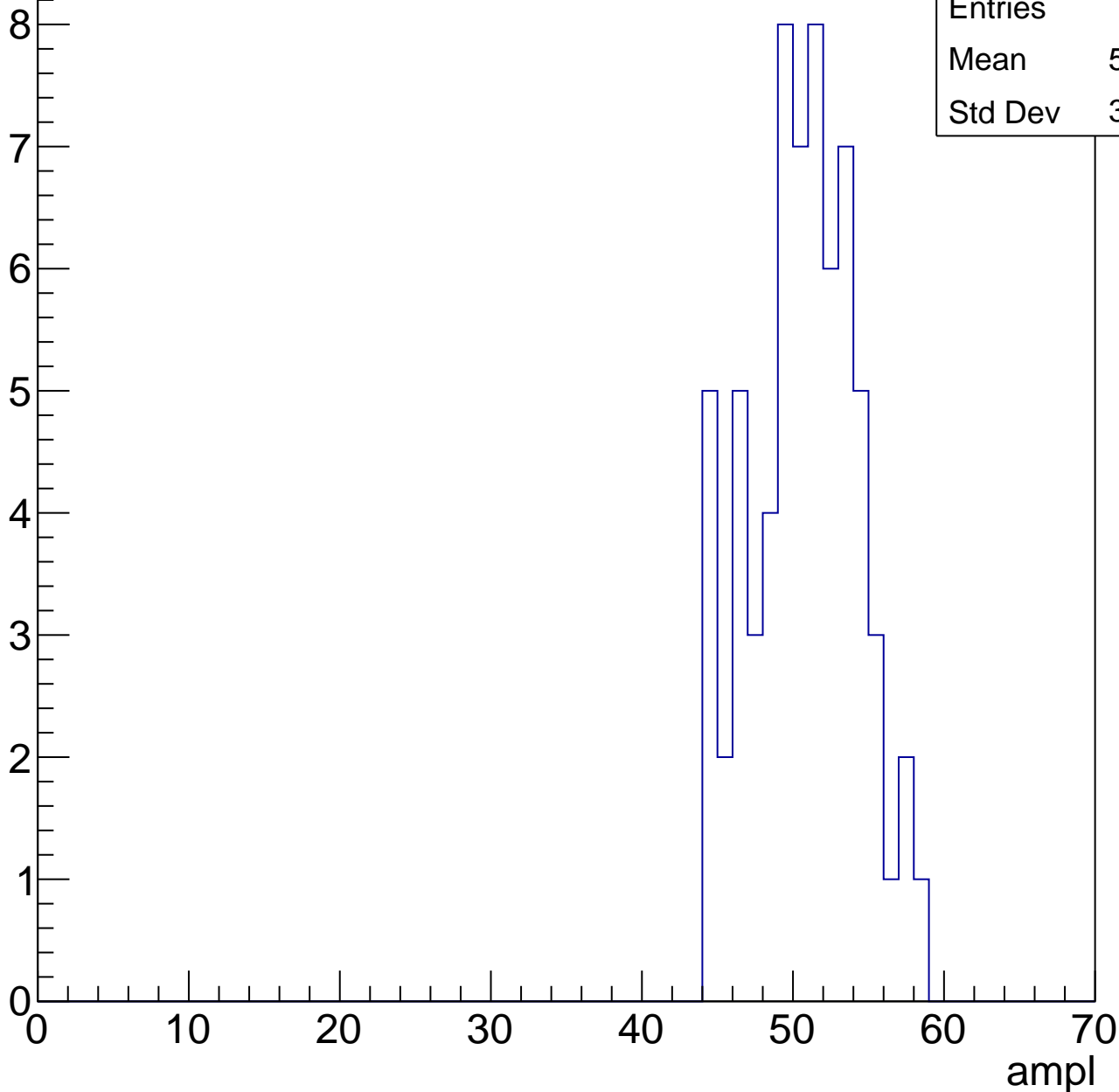


# B1L102S, U12-ch103, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	67
Mean	50.28
Std Dev	3.463

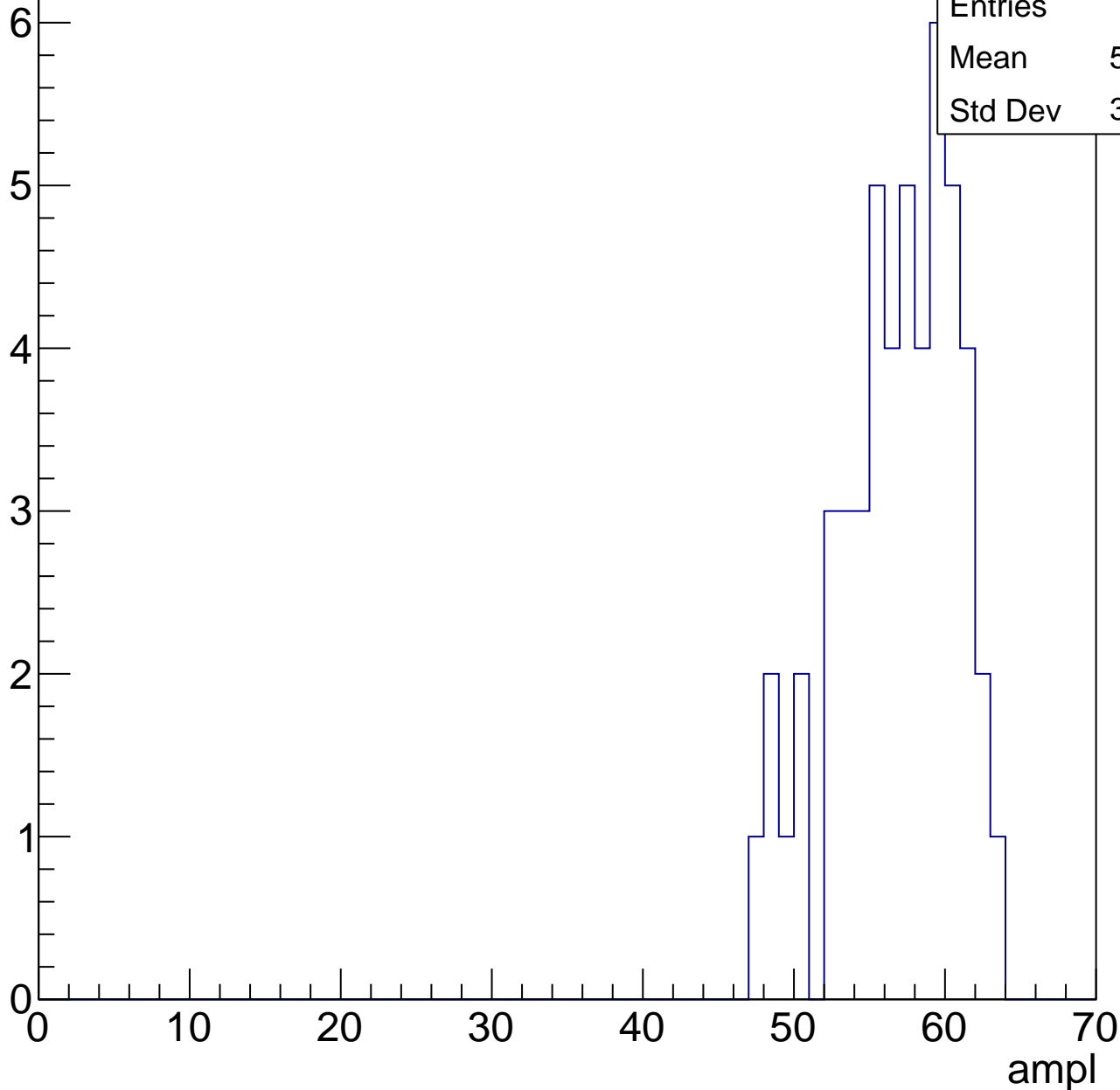


# B1L102S, U12-ch103, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	51
Mean	56.27
Std Dev	3.946

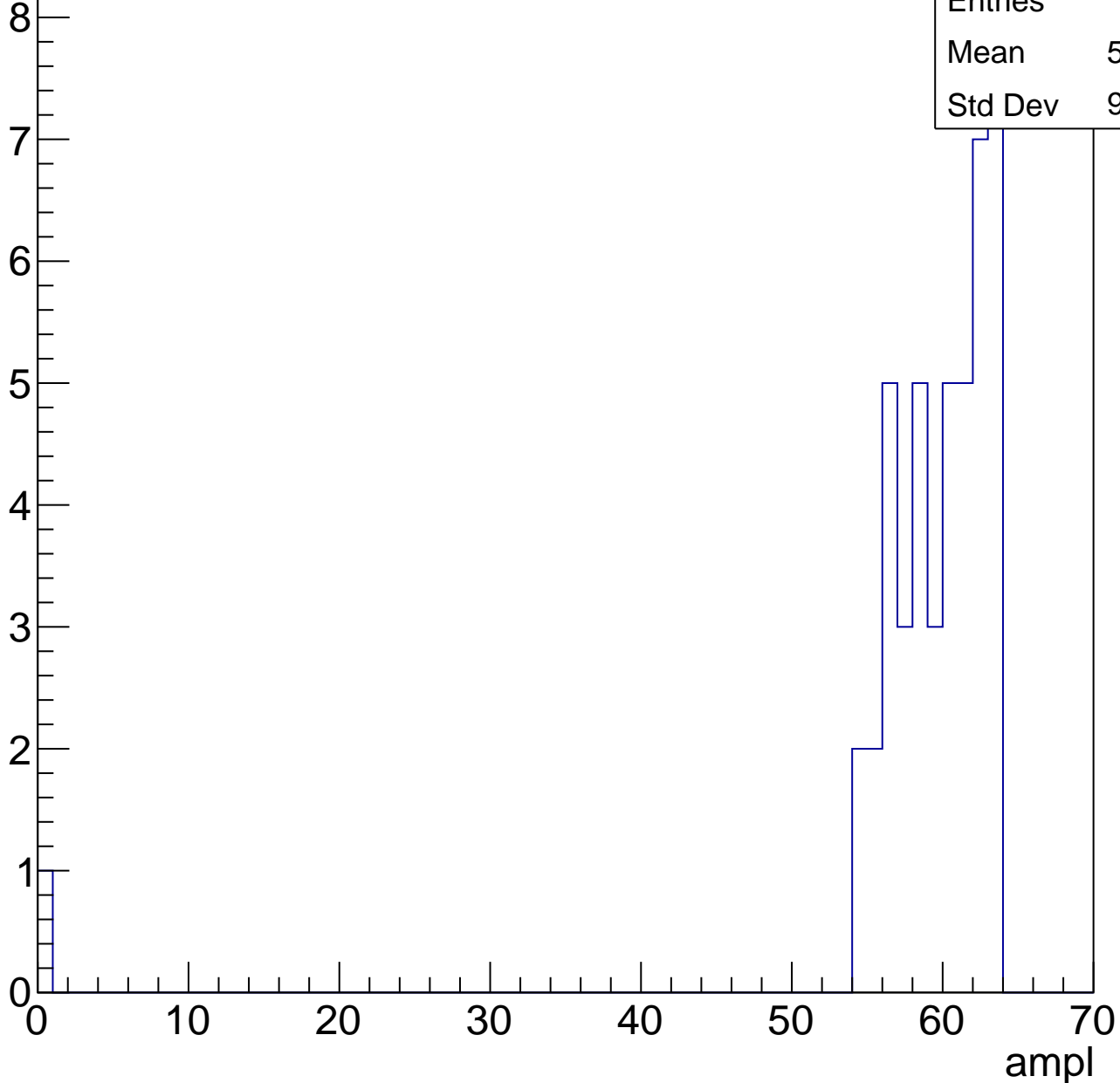


# B1L102S, U12-ch103, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

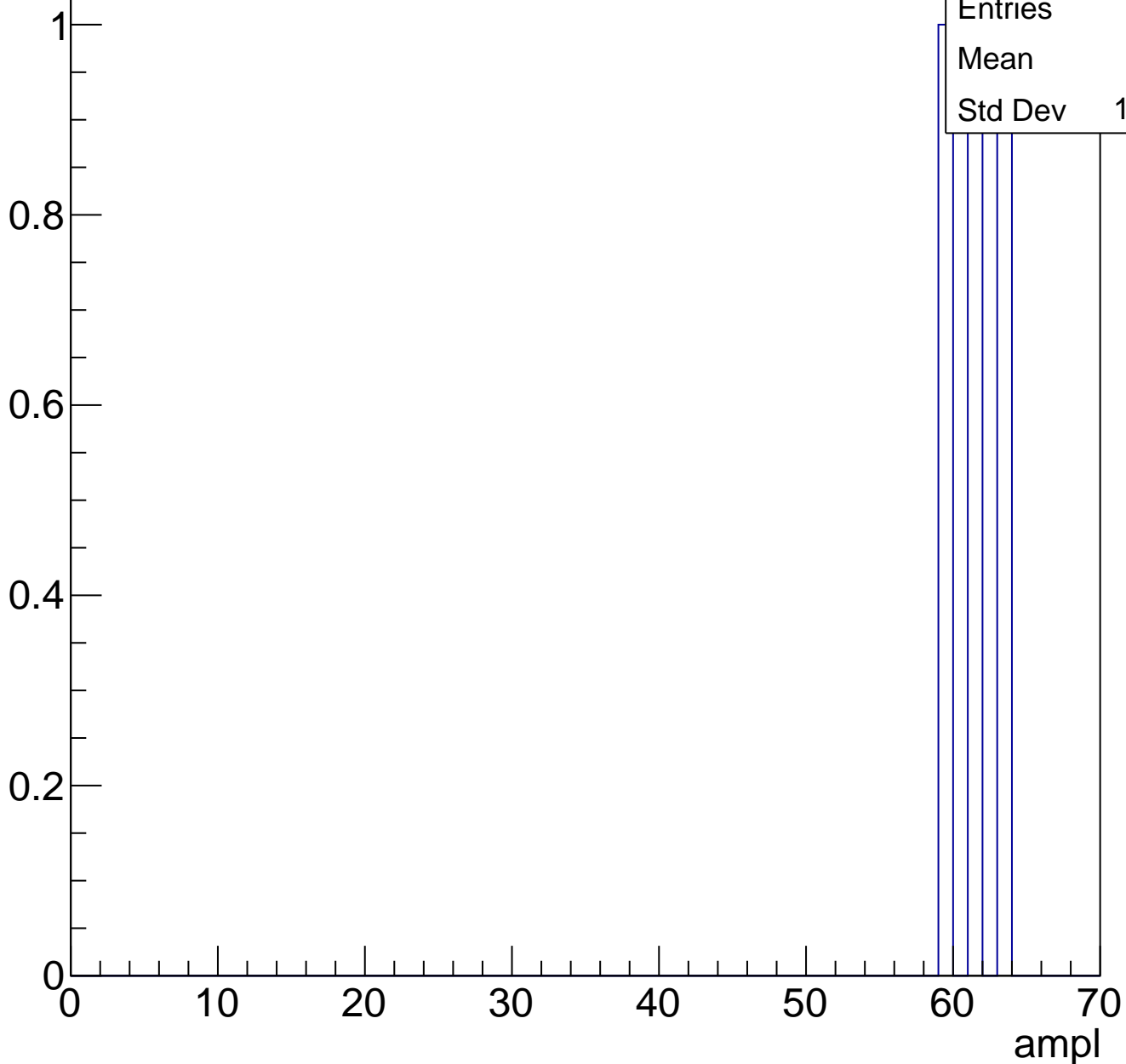
Entries	46
Mean	58.24
Std Dev	9.106



# B1L102S, U12-ch103, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

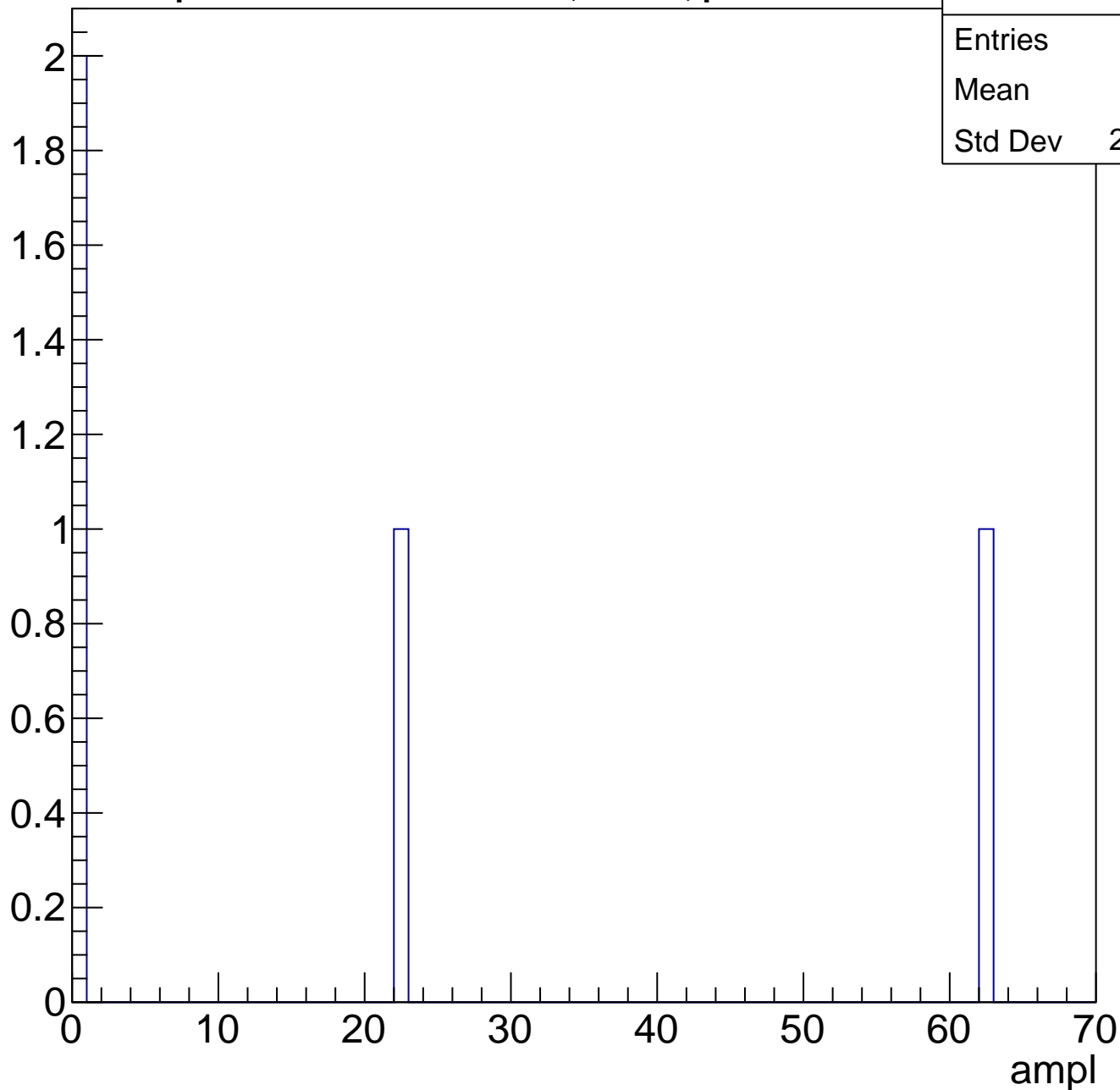




# B1L102S, U12-ch103, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	4
Mean	21
Std Dev	25.32

# B1L102S, U12-ch104, adc0

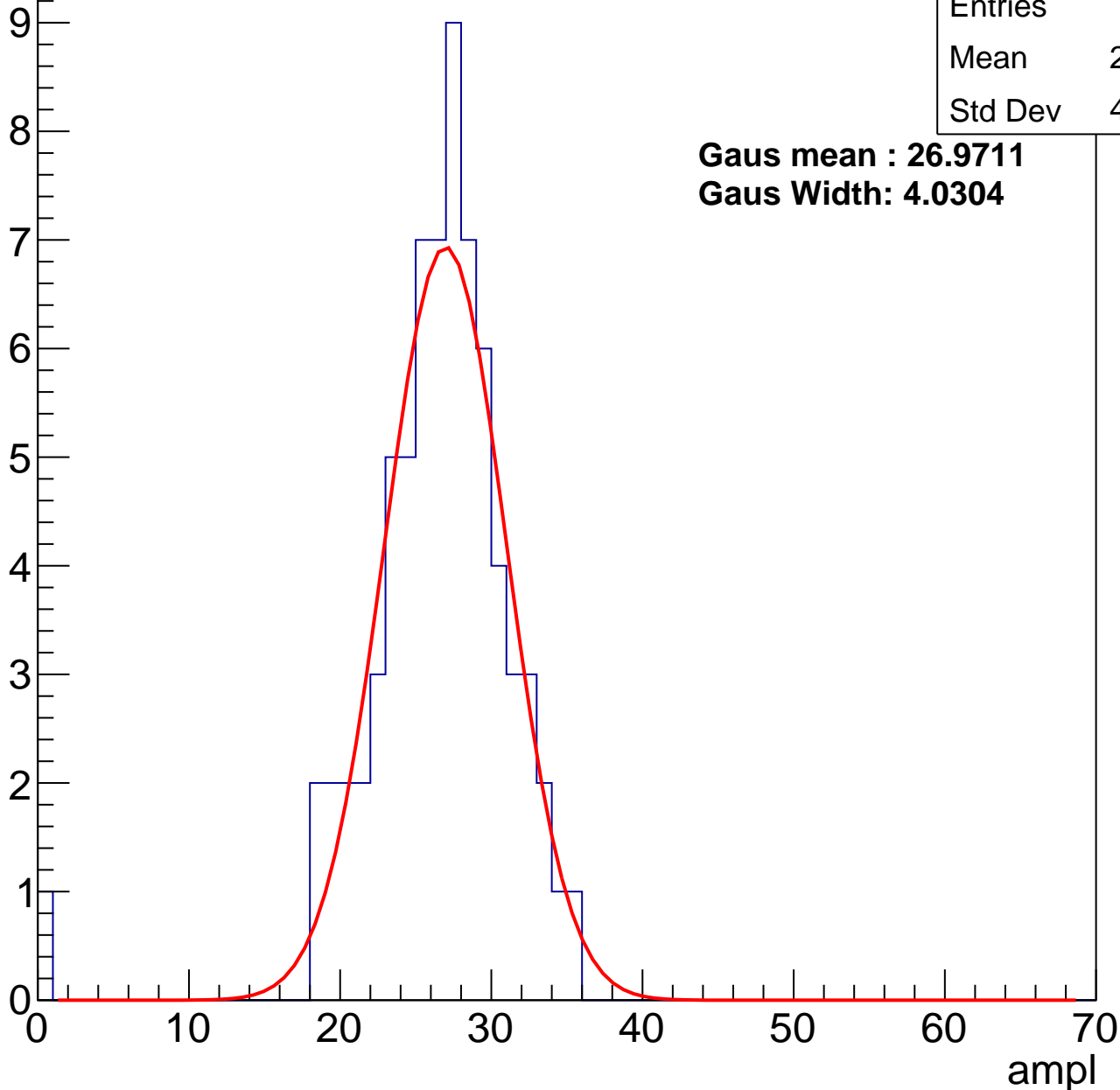
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	72
Mean	25.99
Std Dev	4.895

**Gaus mean : 26.9711**

**Gaus Width: 4.0304**



# B1L102S, U12-ch104, adc1

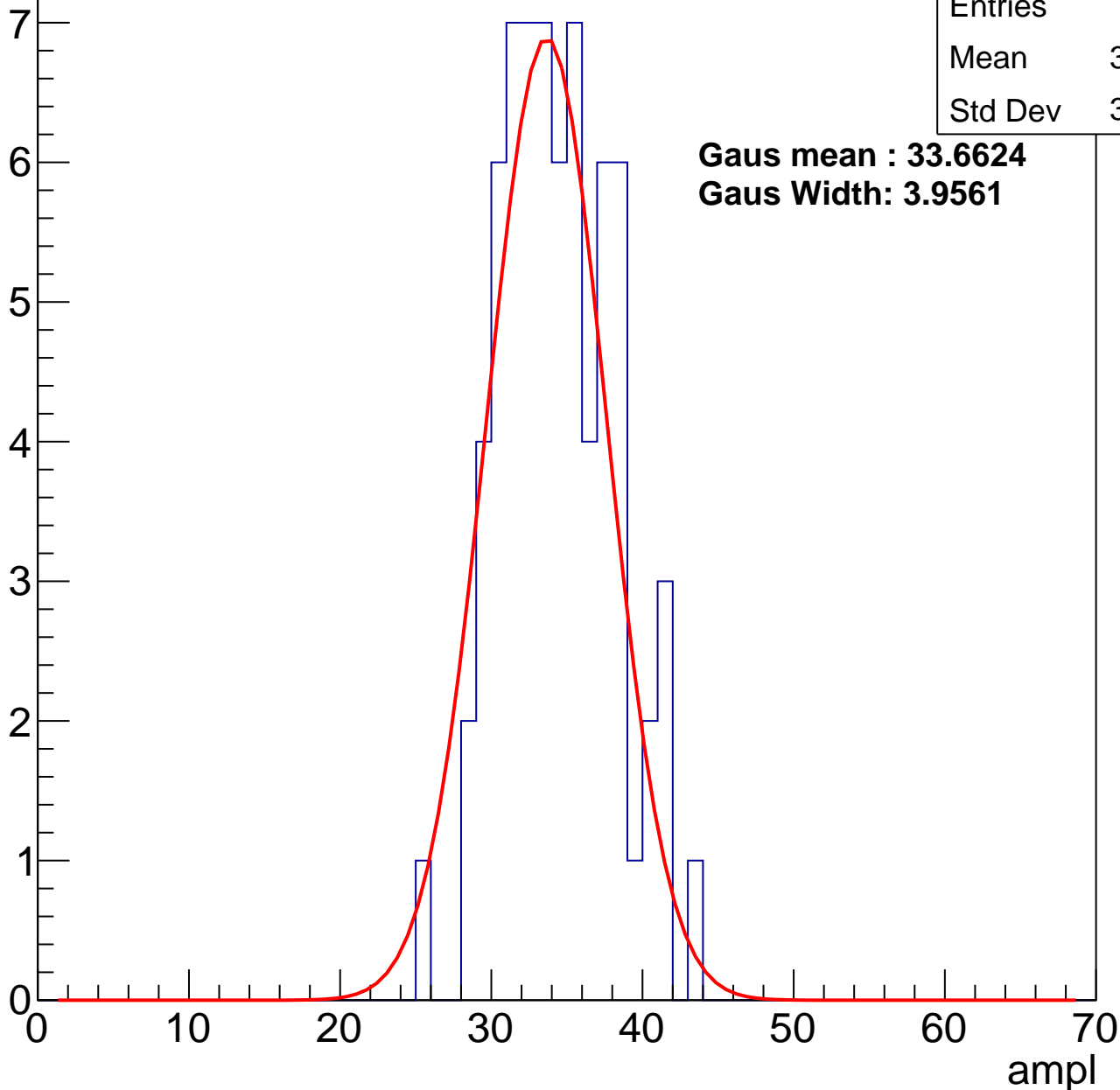
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	70
Mean	33.96
Std Dev	3.674

**Gaus mean : 33.6624**

**Gaus Width: 3.9561**



# B1L102S, U12-ch104, adc2

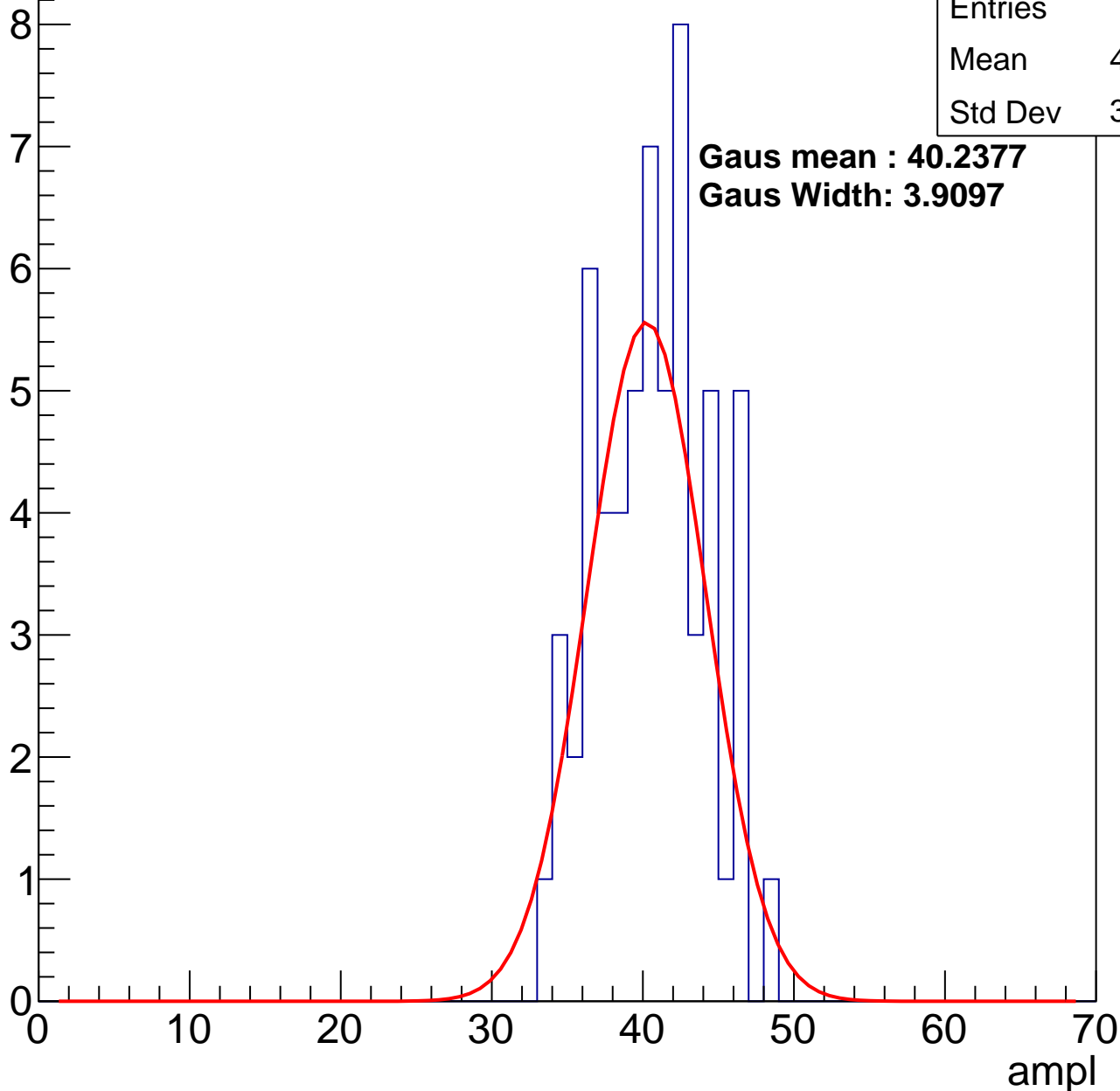
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	60
Mean	40.15
Std Dev	3.586

**Gaus mean : 40.2377**

**Gaus Width: 3.9097**

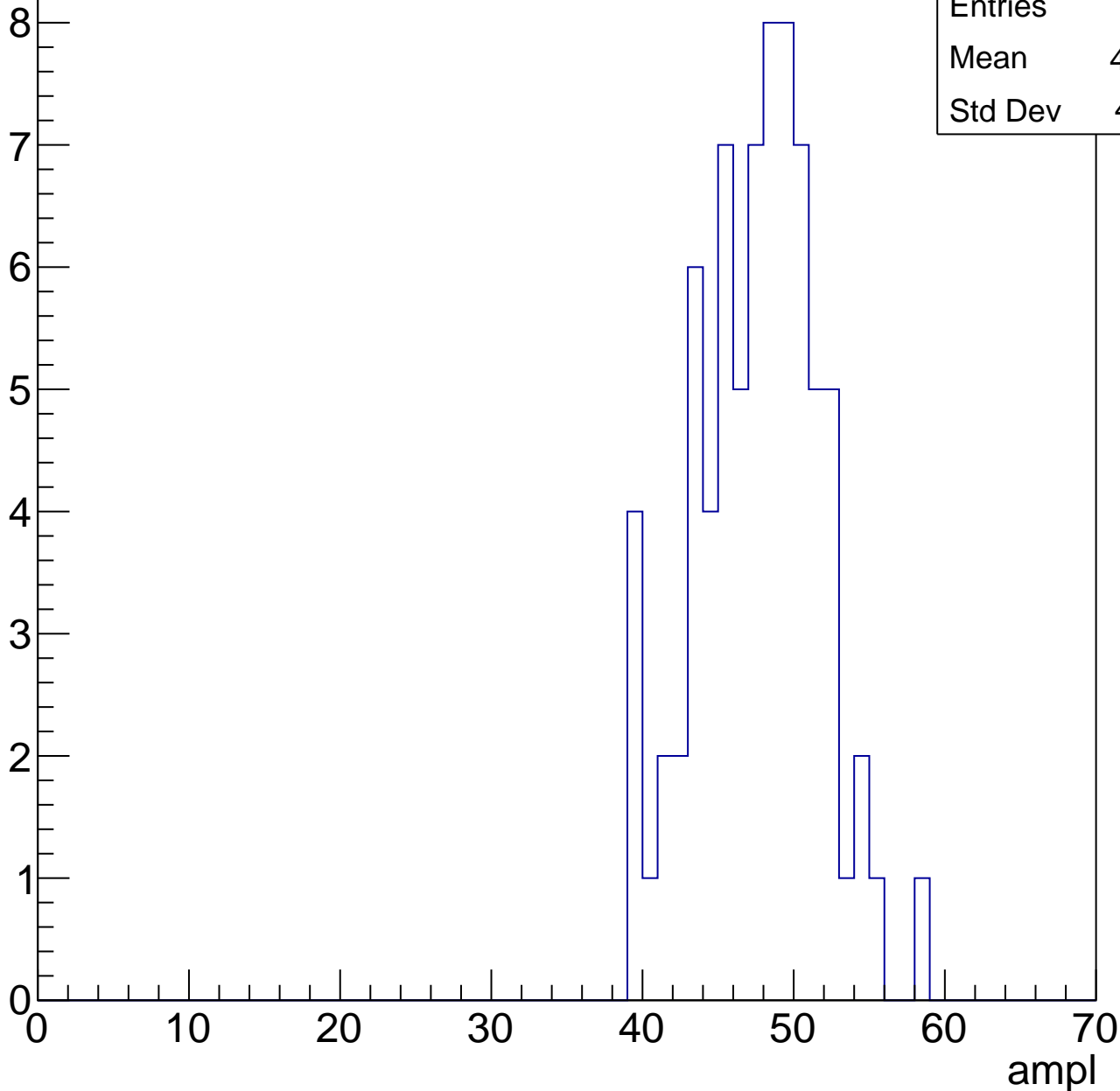


# B1L102S, U12-ch104, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	76
Mean	47.17
Std Dev	4.001

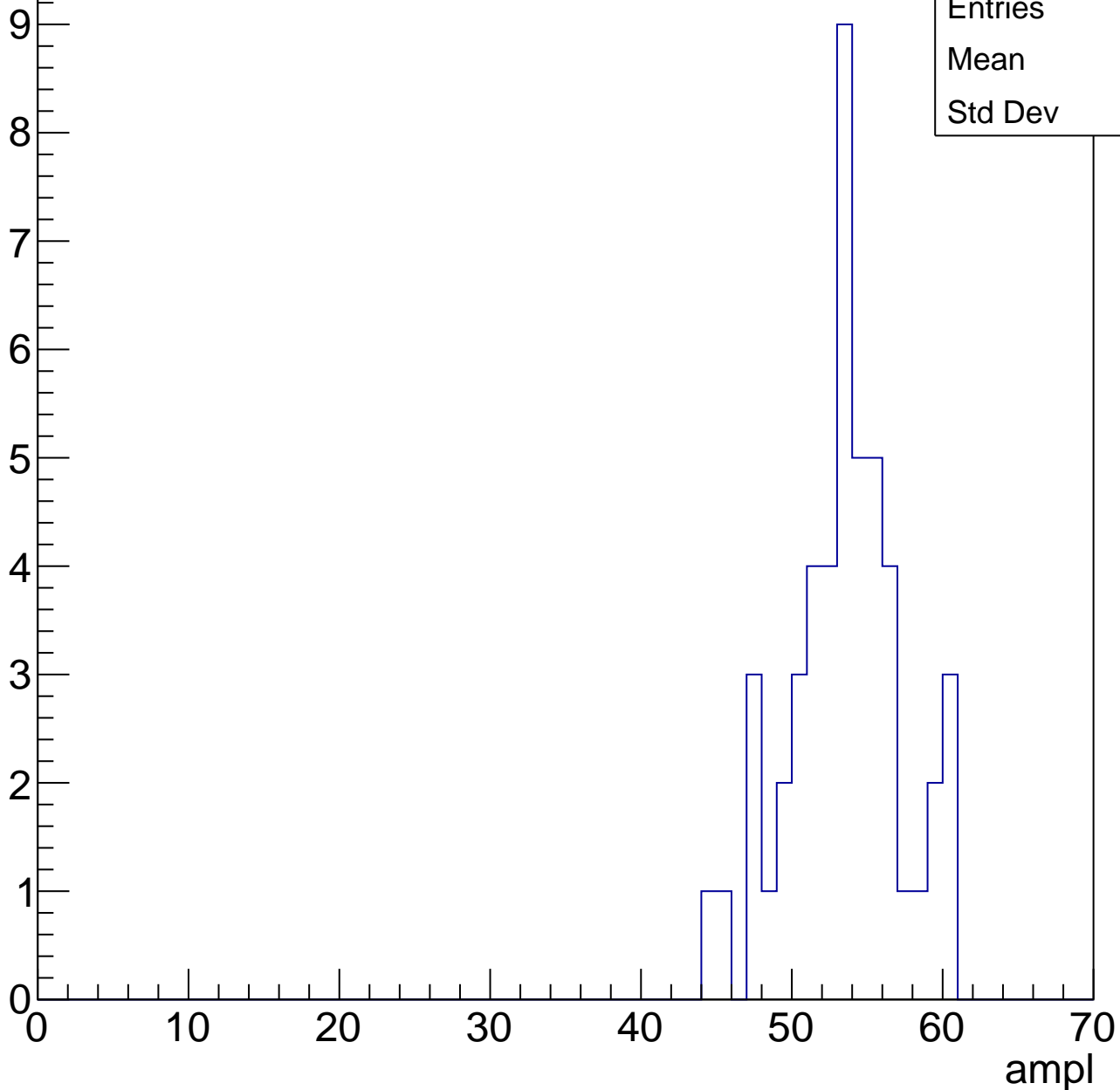


# B1L102S, U12-ch104, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	49
Mean	53
Std Dev	3.72

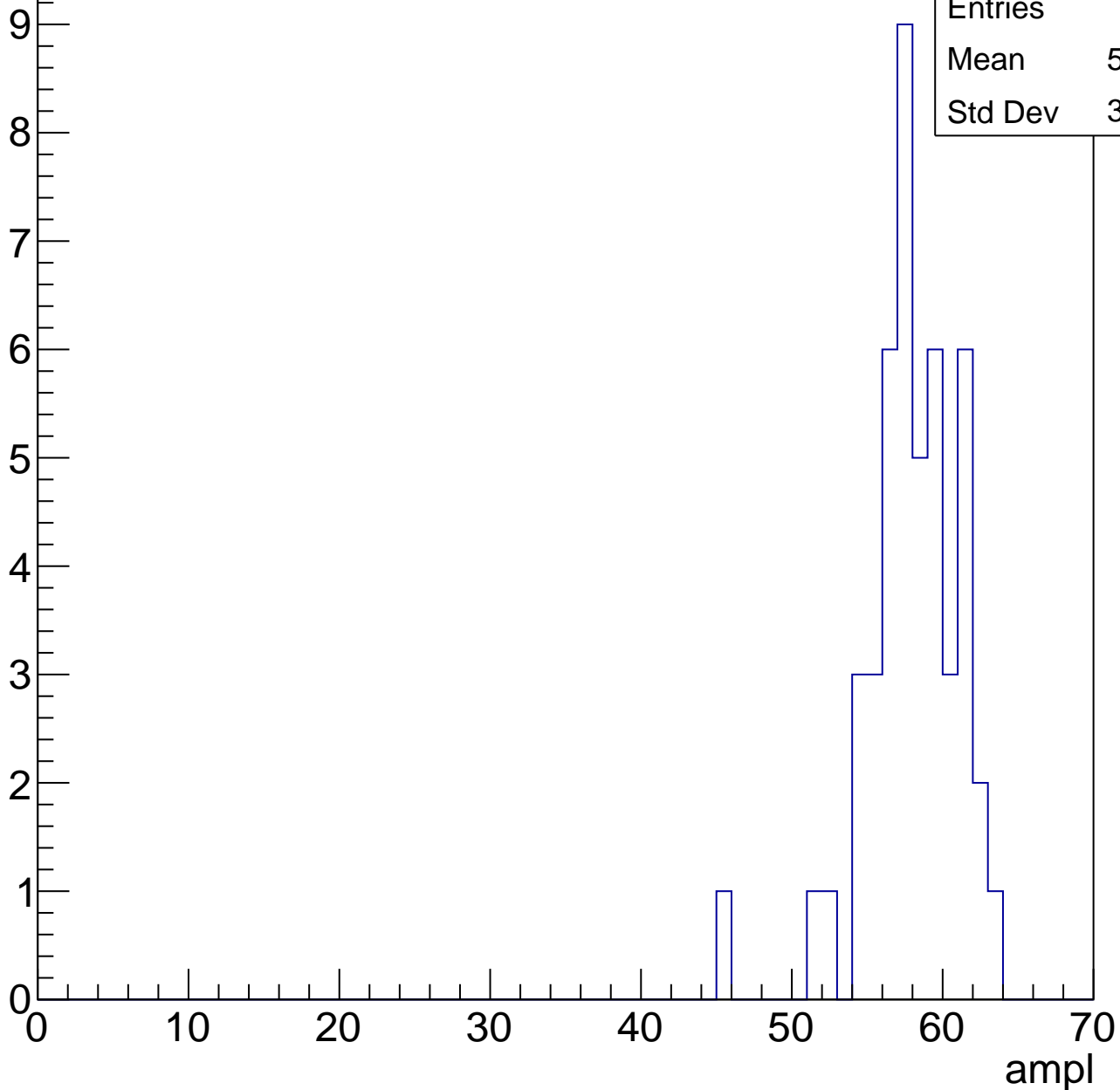


# B1L102S, U12-ch104, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	47
Mean	57.47
Std Dev	3.188

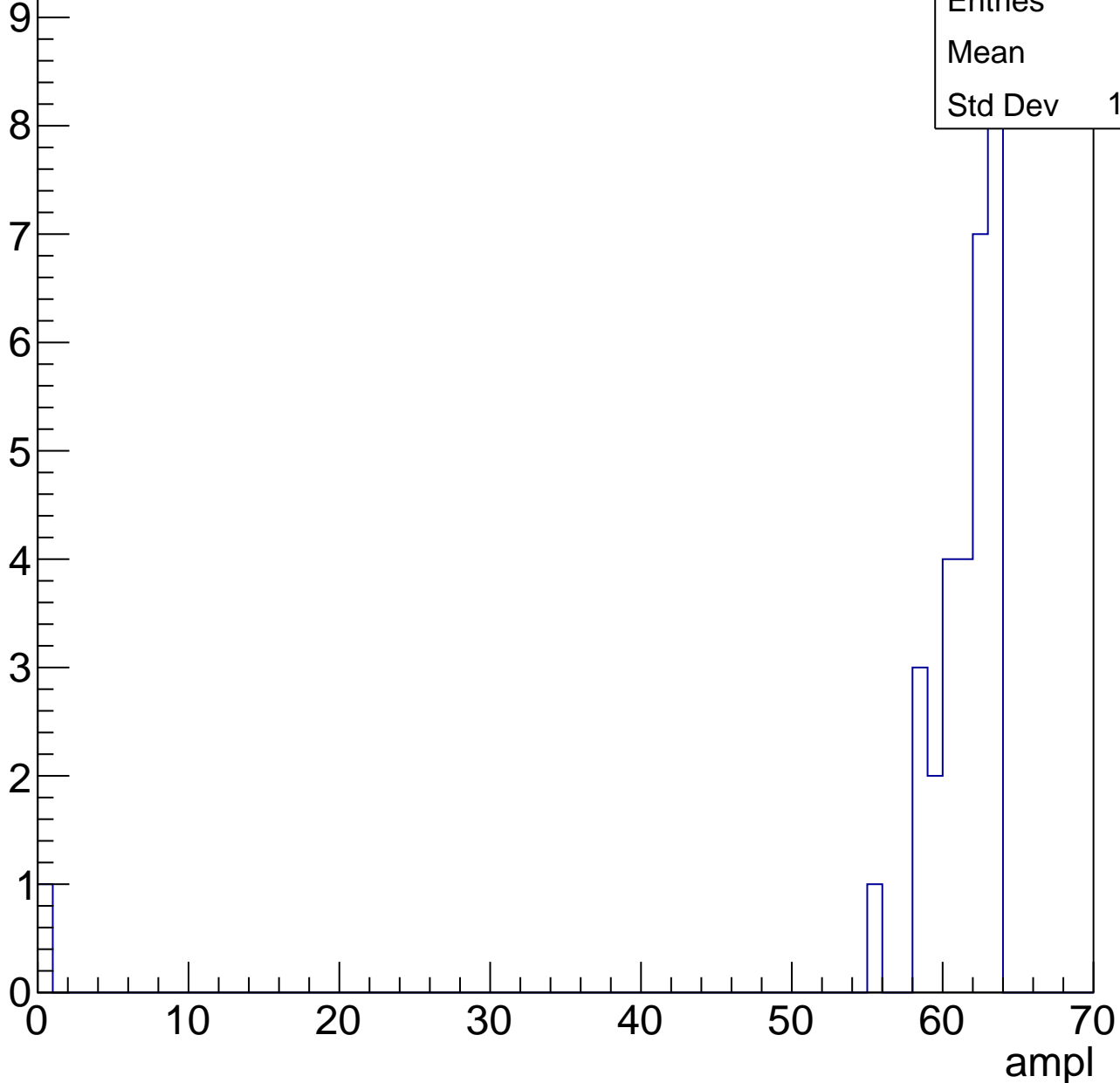


# B1L102S, U12-ch104, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	31
Mean	59.1
Std Dev	10.96





# B1L102S, U12-ch104, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	3
Mean	20.67
Std Dev	29.23

# B1L102S, U12-ch105, adc0

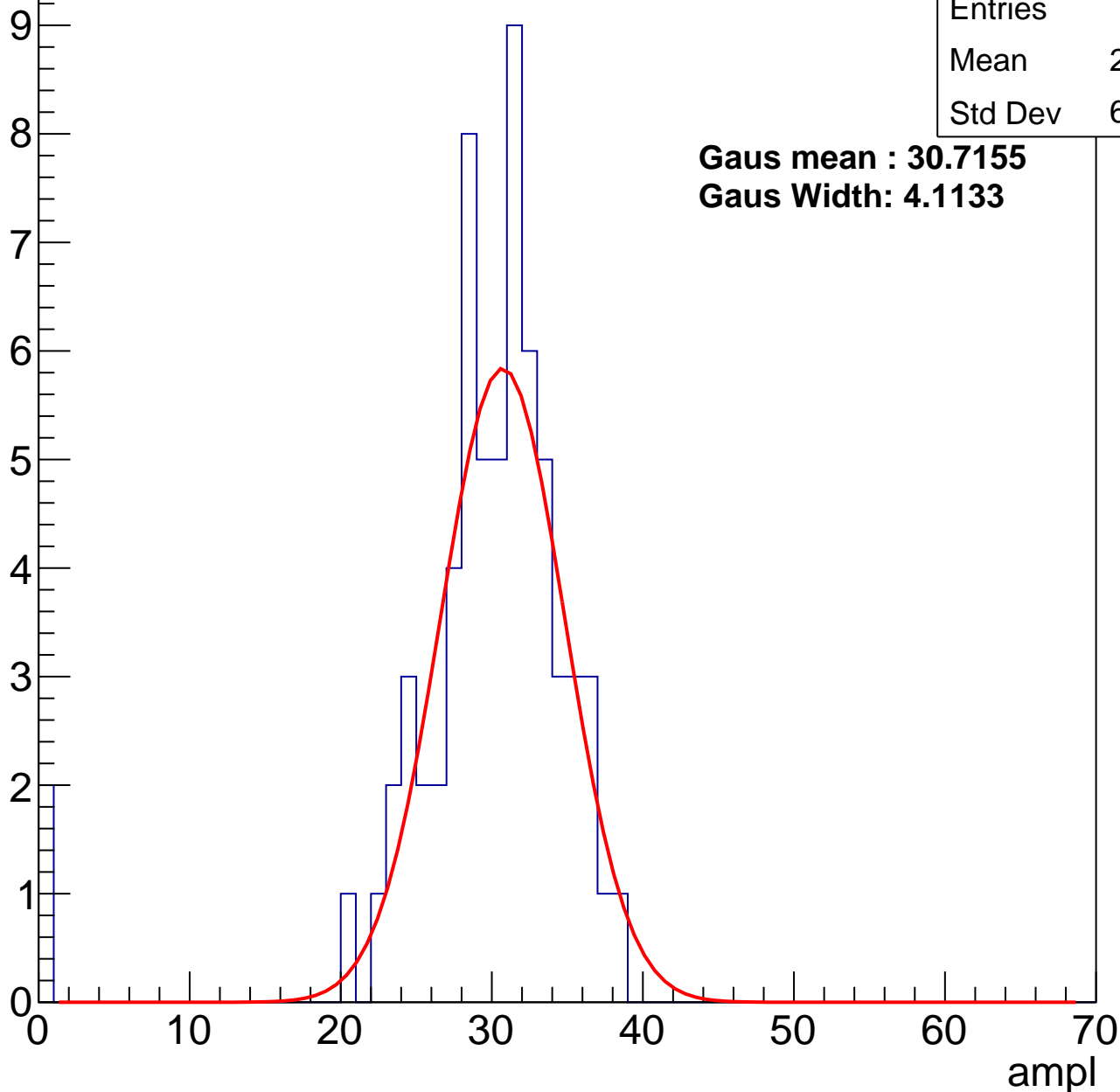
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	29.02
Std Dev	6.376

**Gaus mean : 30.7155**

**Gaus Width: 4.1133**



# B1L102S, U12-ch105, adc1

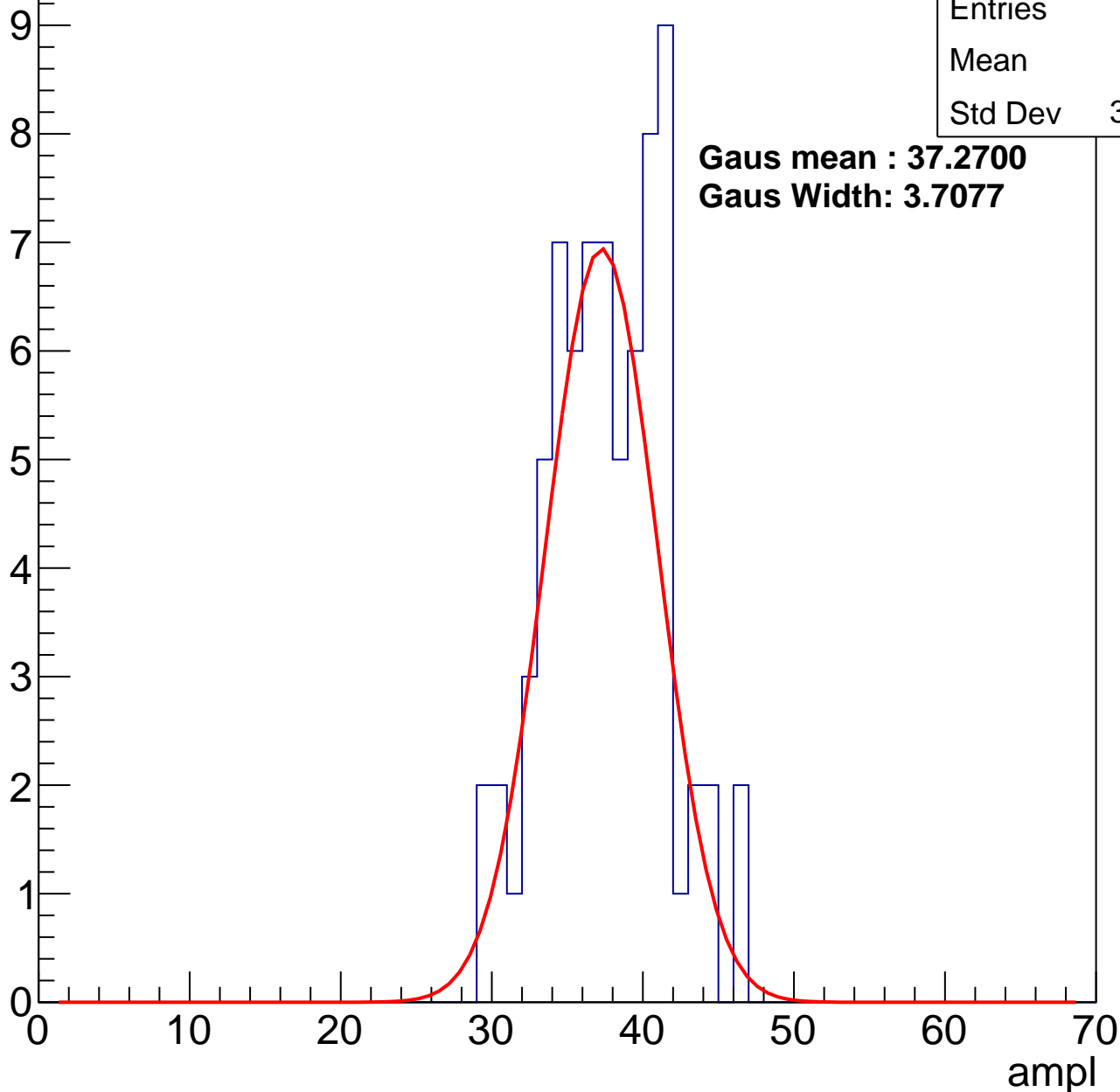
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	75
Mean	37.2
Std Dev	3.847

**Gaus mean : 37.2700**

**Gaus Width: 3.7077**



# B1L102S, U12-ch105, adc2

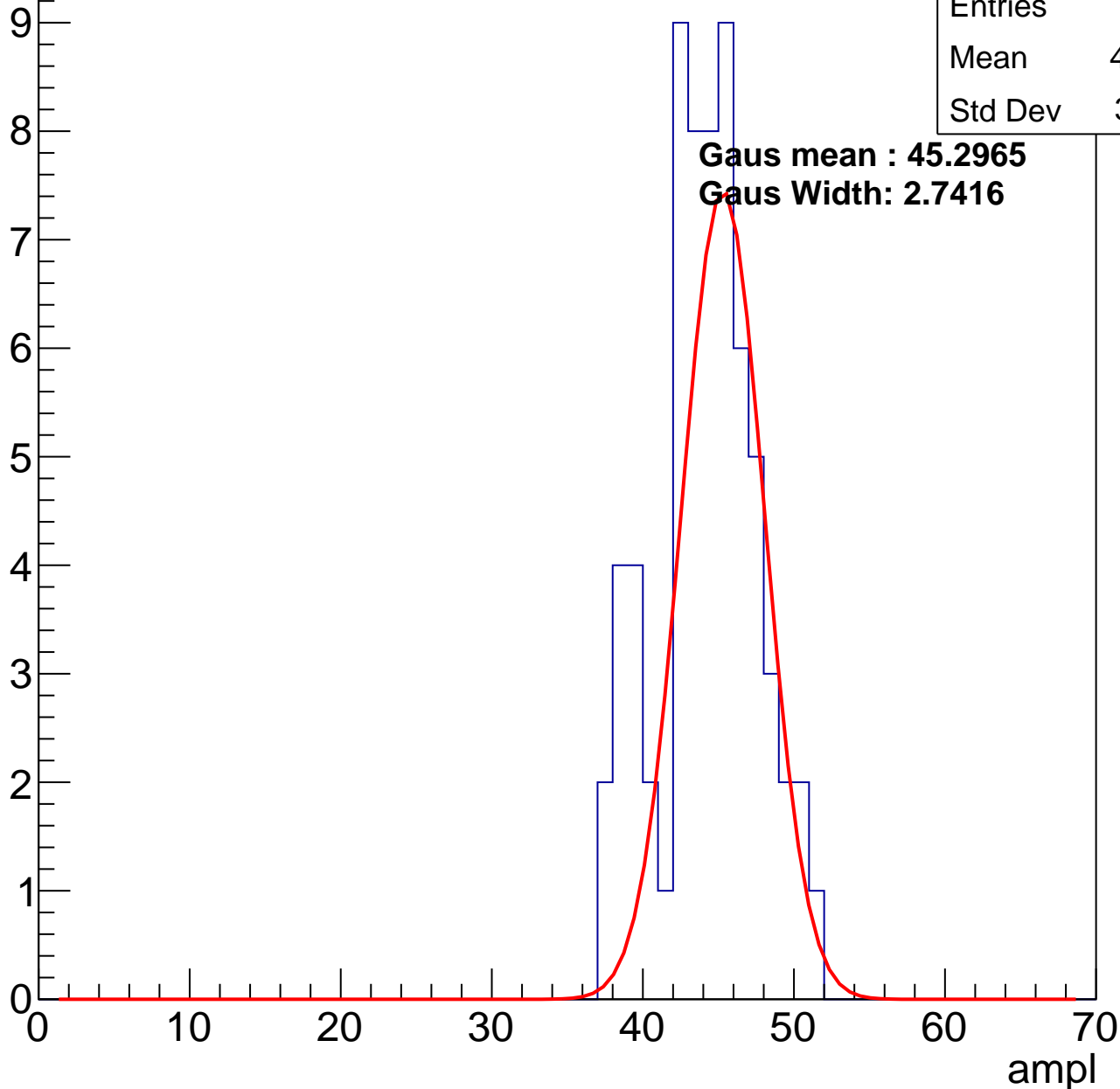
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	43.73
Std Dev	3.301

**Gaus mean : 45.2965**

**Gaus Width: 2.7416**

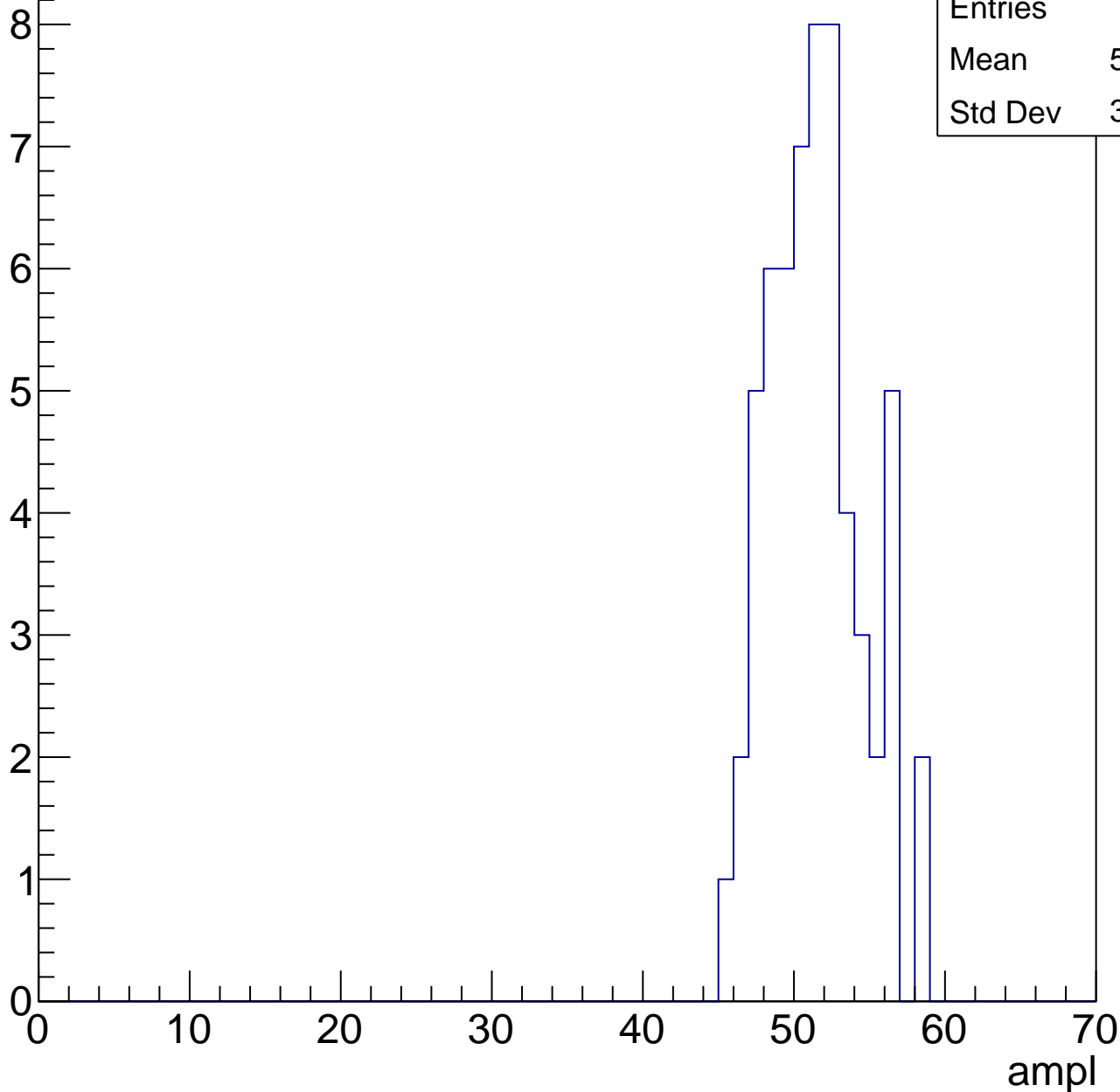


# B1L102S, U12-ch105, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	59
Mean	50.98
Std Dev	3.073

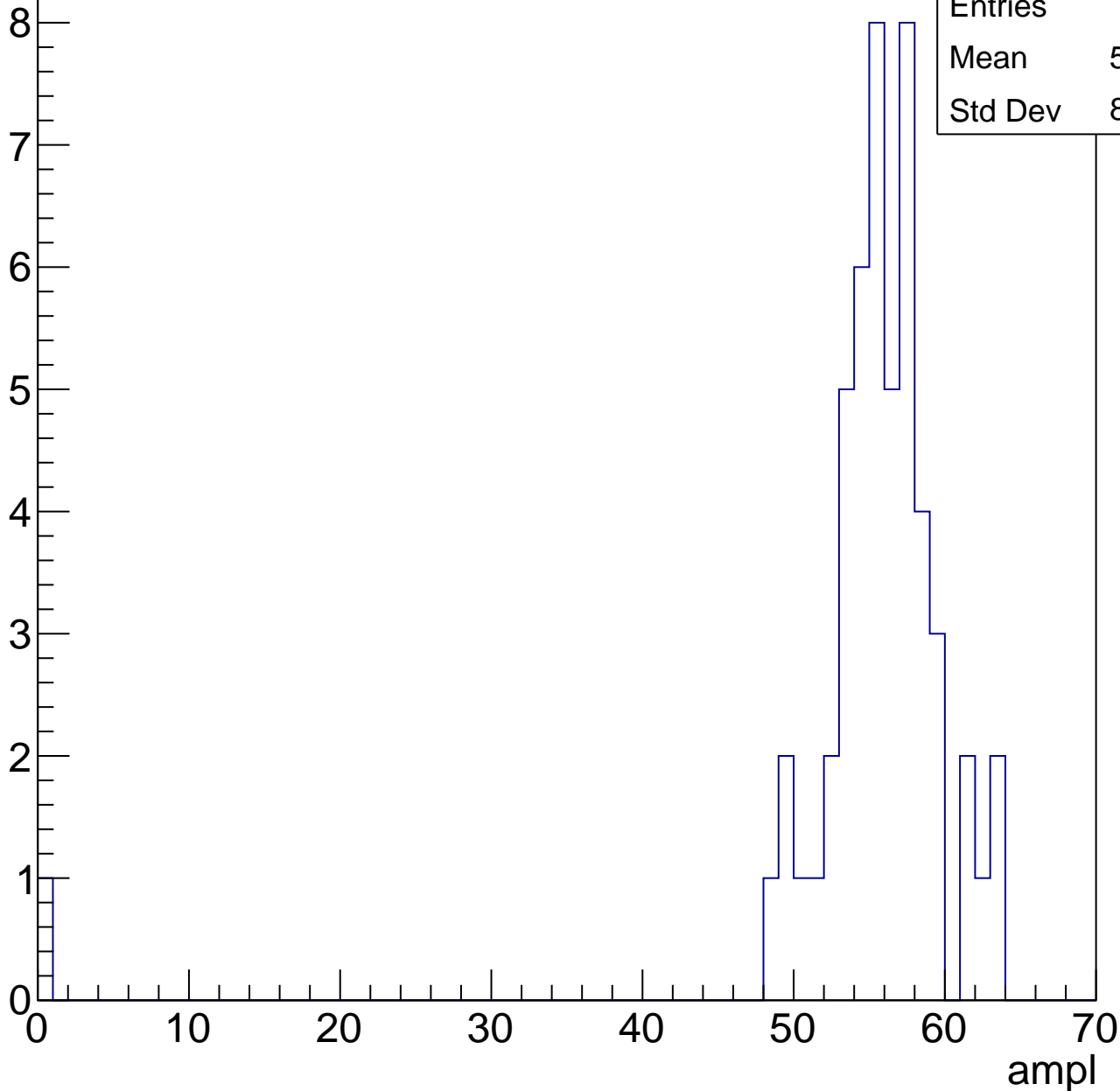


# B1L102S, U12-ch105, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	52
Mean	54.52
Std Dev	8.308

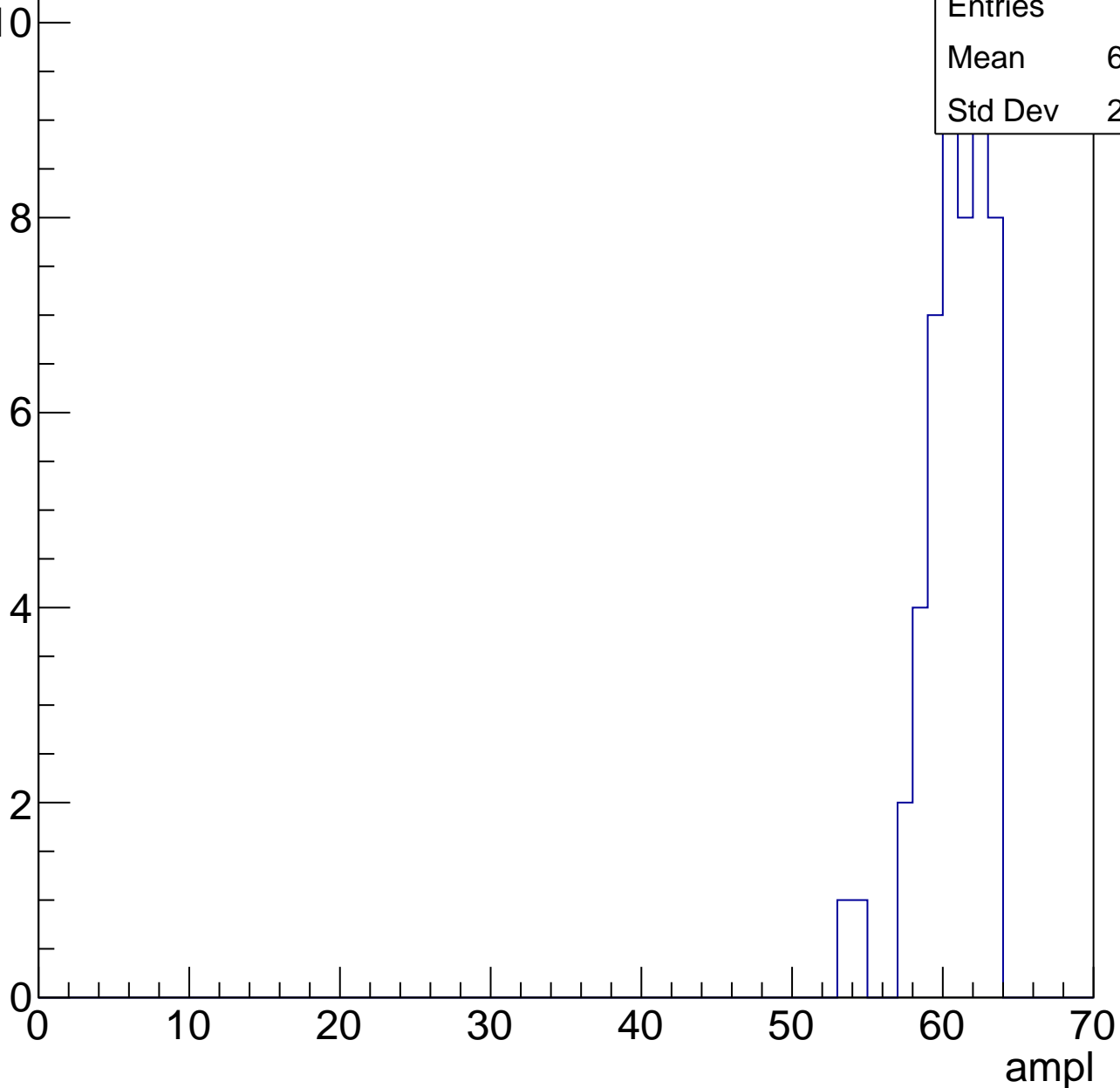


# B1L102S, U12-ch105, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	50
Mean	60.32
Std Dev	2.177



# B1L102S, U12-ch105, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0



# B1L102S, U12-ch105, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L102S, U12-ch106, adc0

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	78
Mean	27.64
Std Dev	4.013

**Gaus mean : 28.1198**

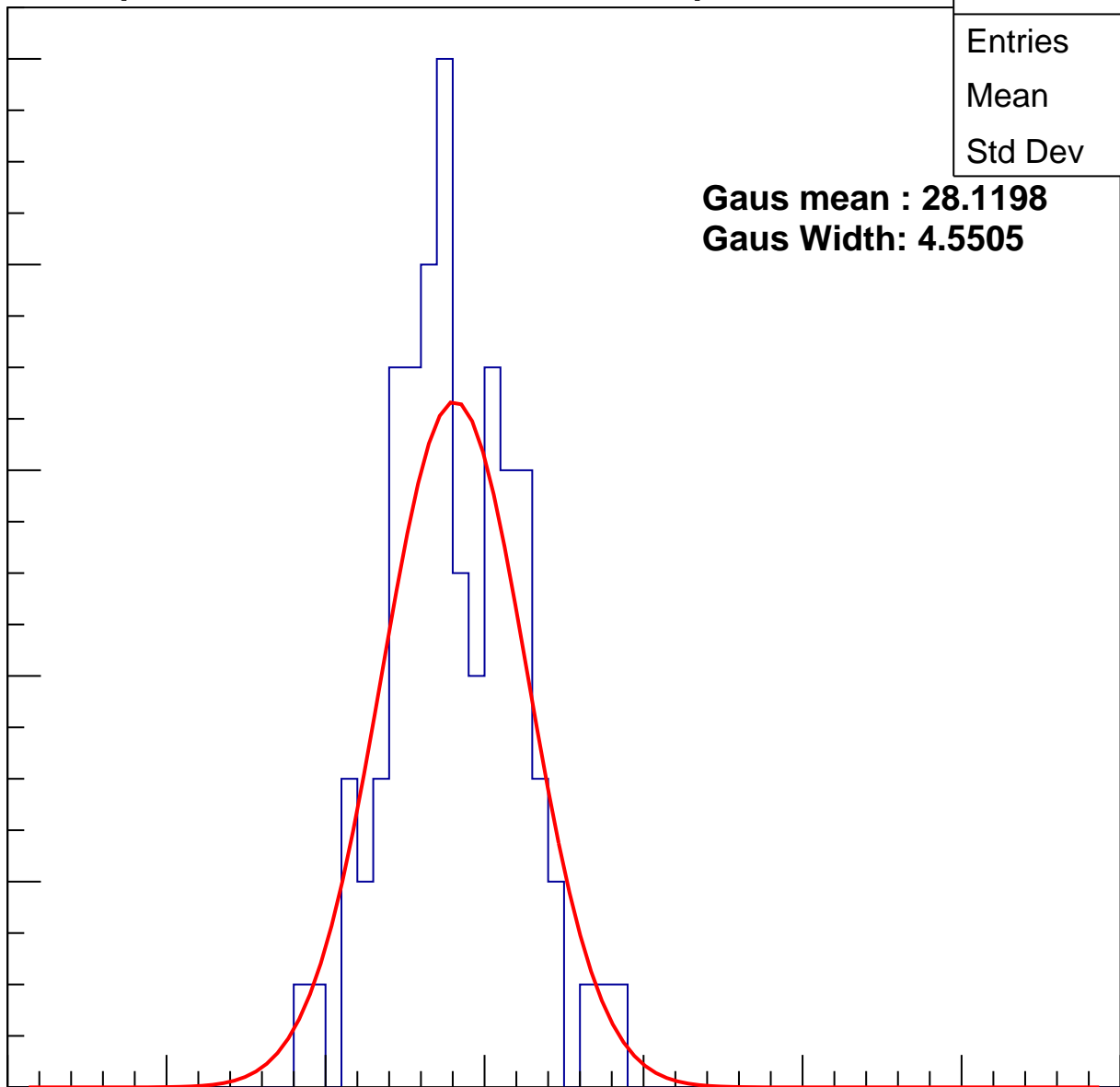
**Gaus Width: 4.5505**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L102S, U12-ch106, adc1

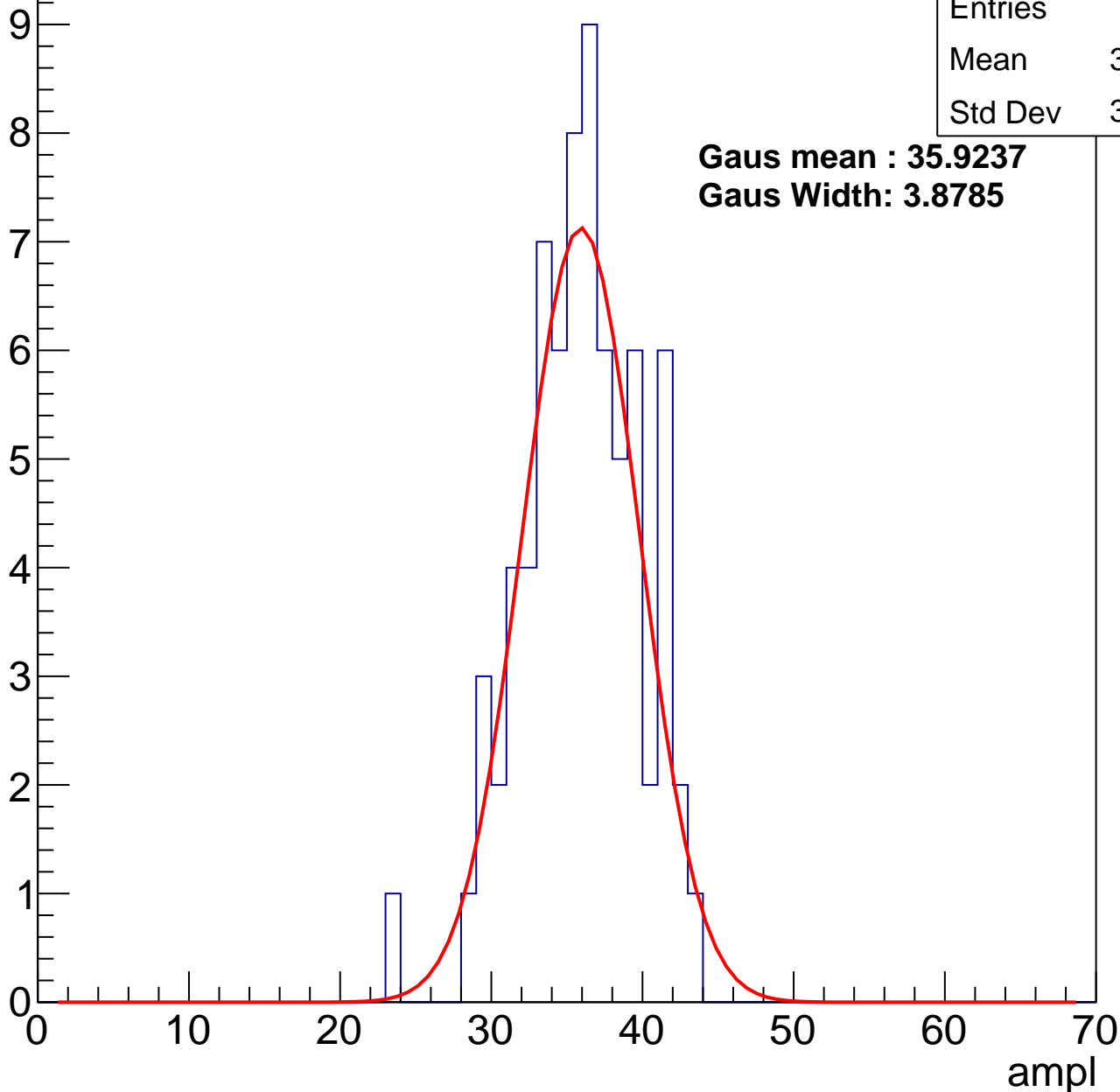
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	73
Mean	35.45
Std Dev	3.832

**Gaus mean : 35.9237**

**Gaus Width: 3.8785**



# B1L102S, U12-ch106, adc2

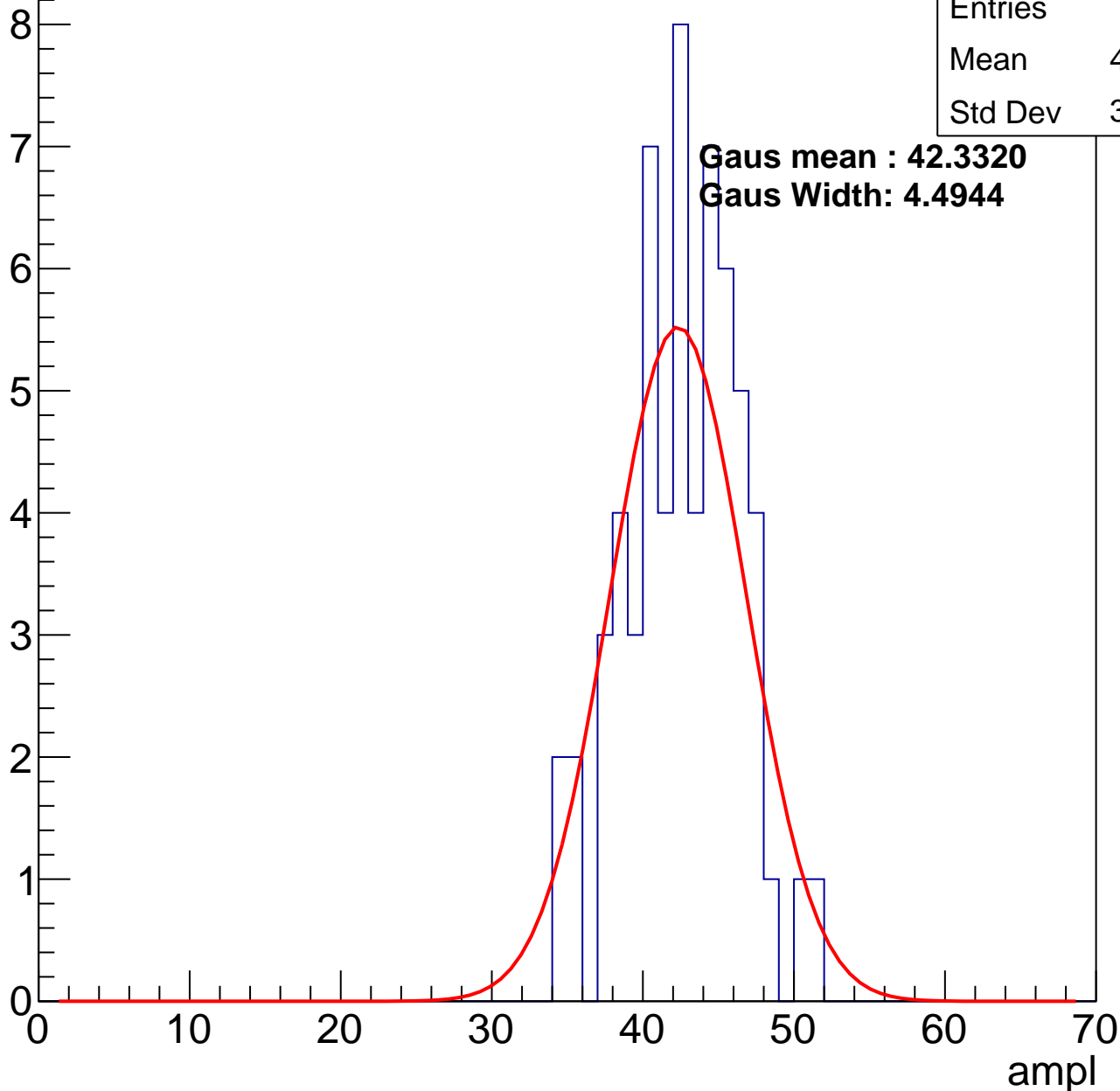
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	62
Mean	42.18
Std Dev	3.744

**Gaus mean : 42.3320**

**Gaus Width: 4.4944**

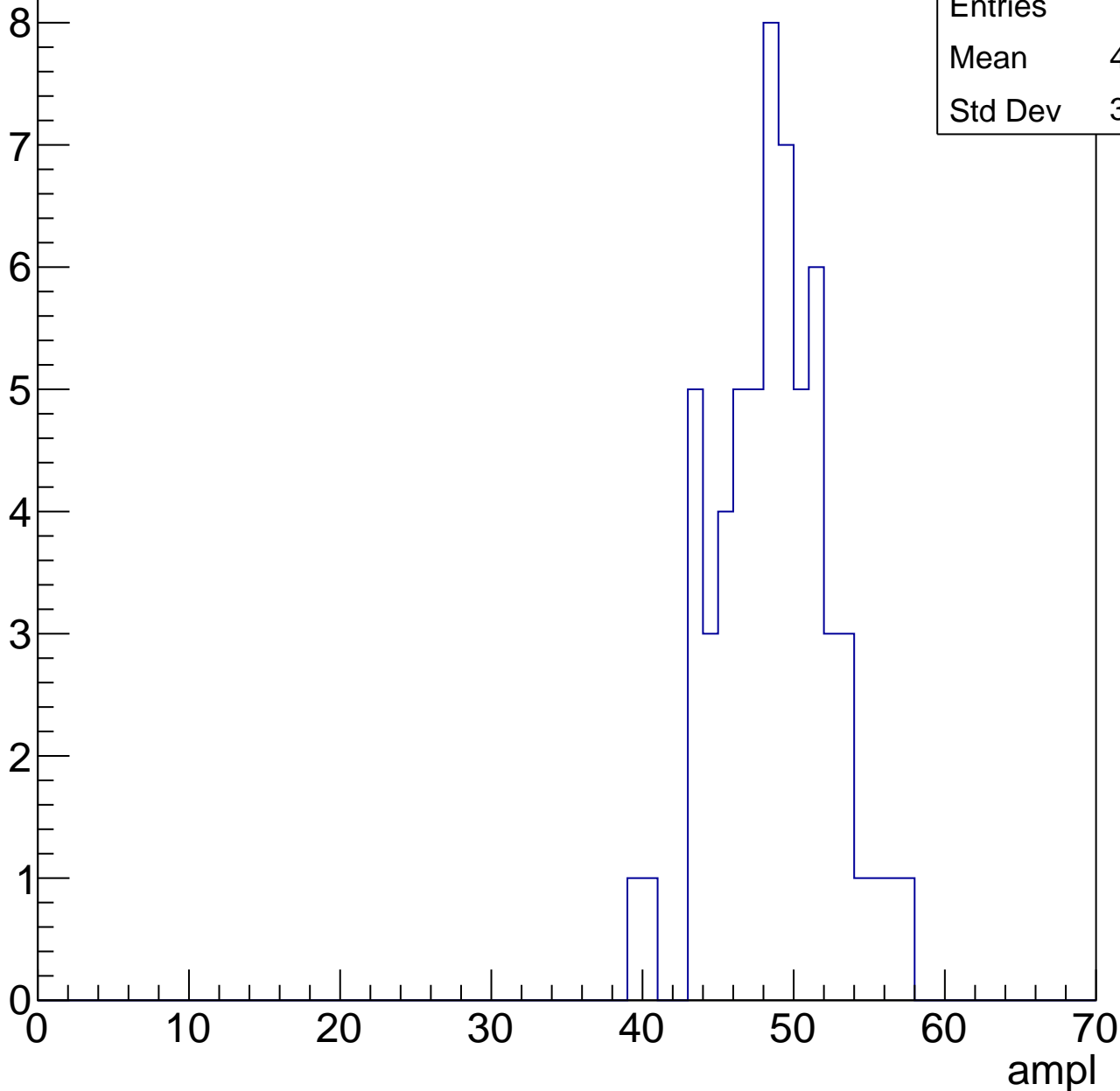


# B1L102S, U12-ch106, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	60
Mean	48.18
Std Dev	3.676

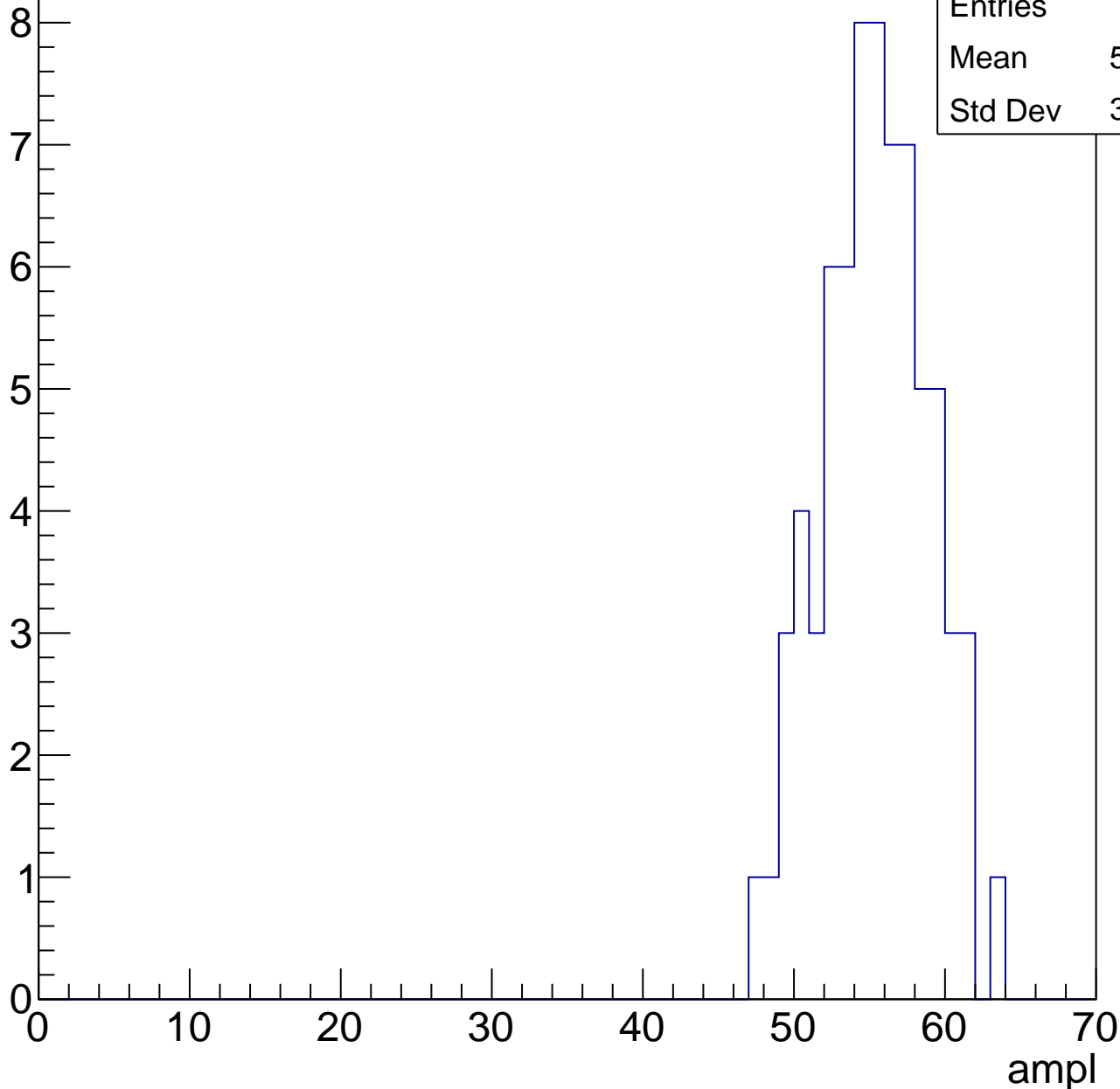


# B1L102S, U12-ch106, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	71
Mean	54.92
Std Dev	3.483

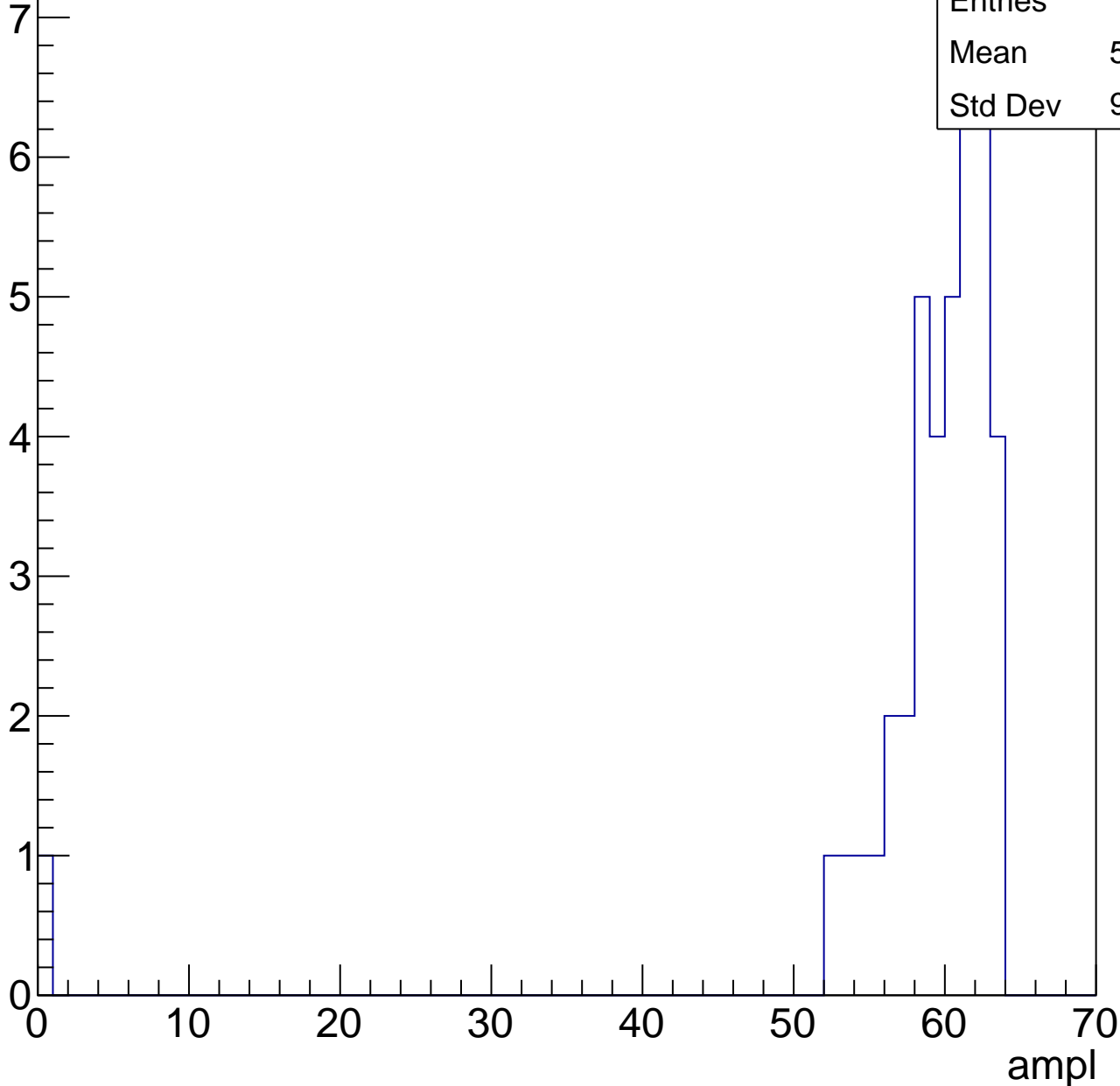


# B1L102S, U12-ch106, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	41
Mean	58.02
Std Dev	9.575

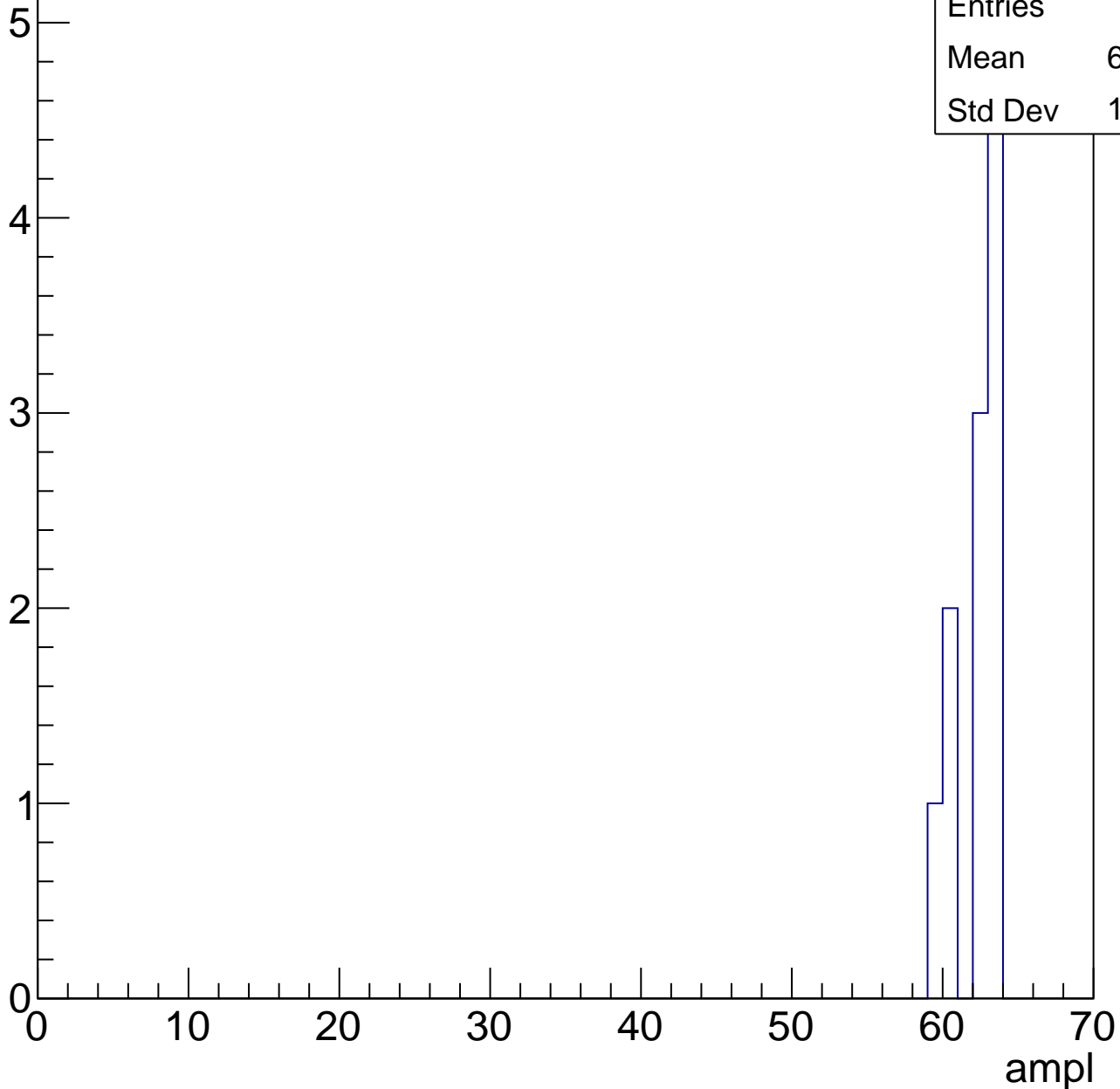


# B1L102S, U12-ch106, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	11
Mean	61.82
Std Dev	1.402





# B1L102S, U12-ch106, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U12-ch107, adc0

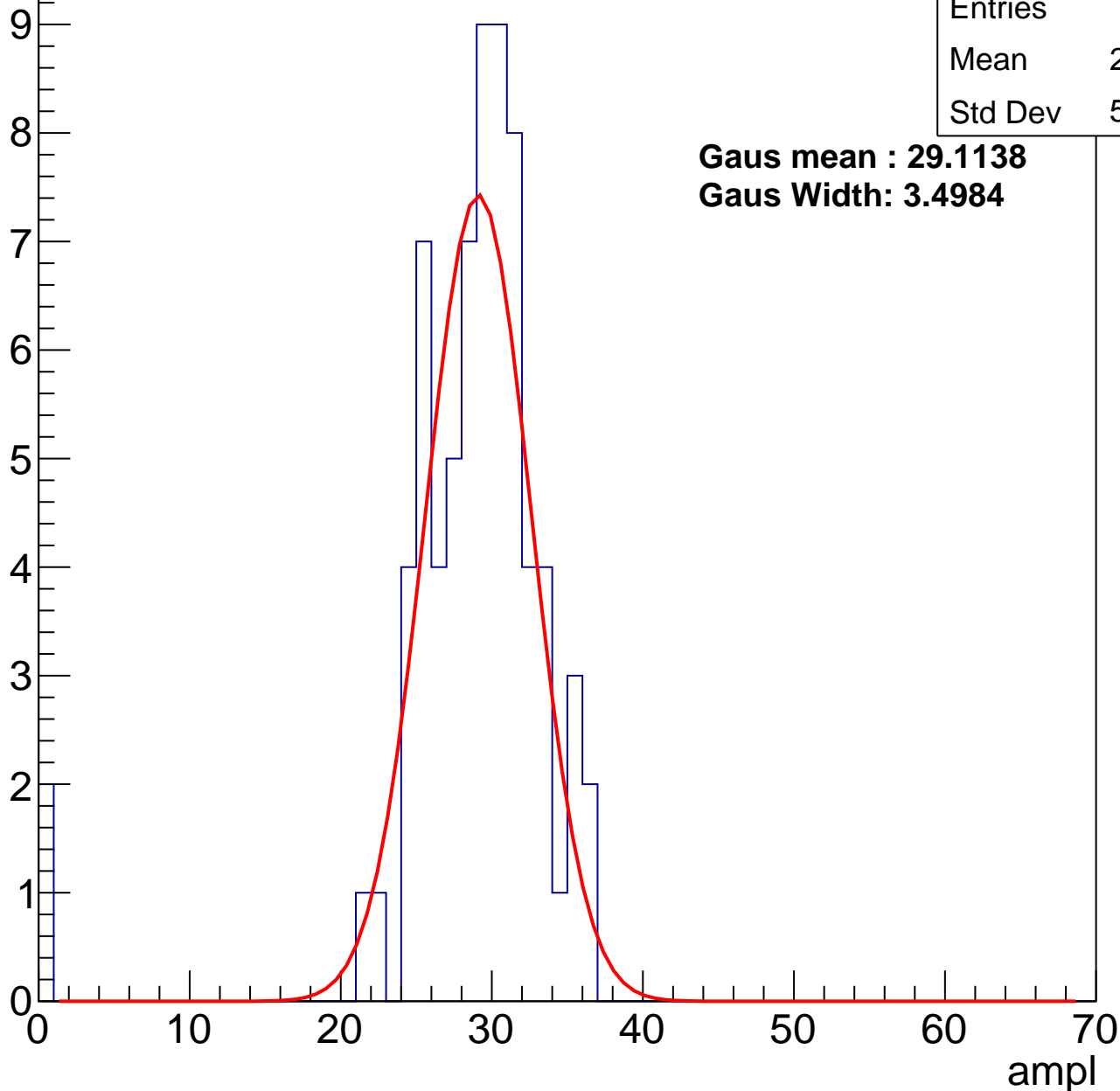
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	71
Mean	28.15
Std Dev	5.803

**Gaus mean : 29.1138**

**Gaus Width: 3.4984**



# B1L102S, U12-ch107, adc1

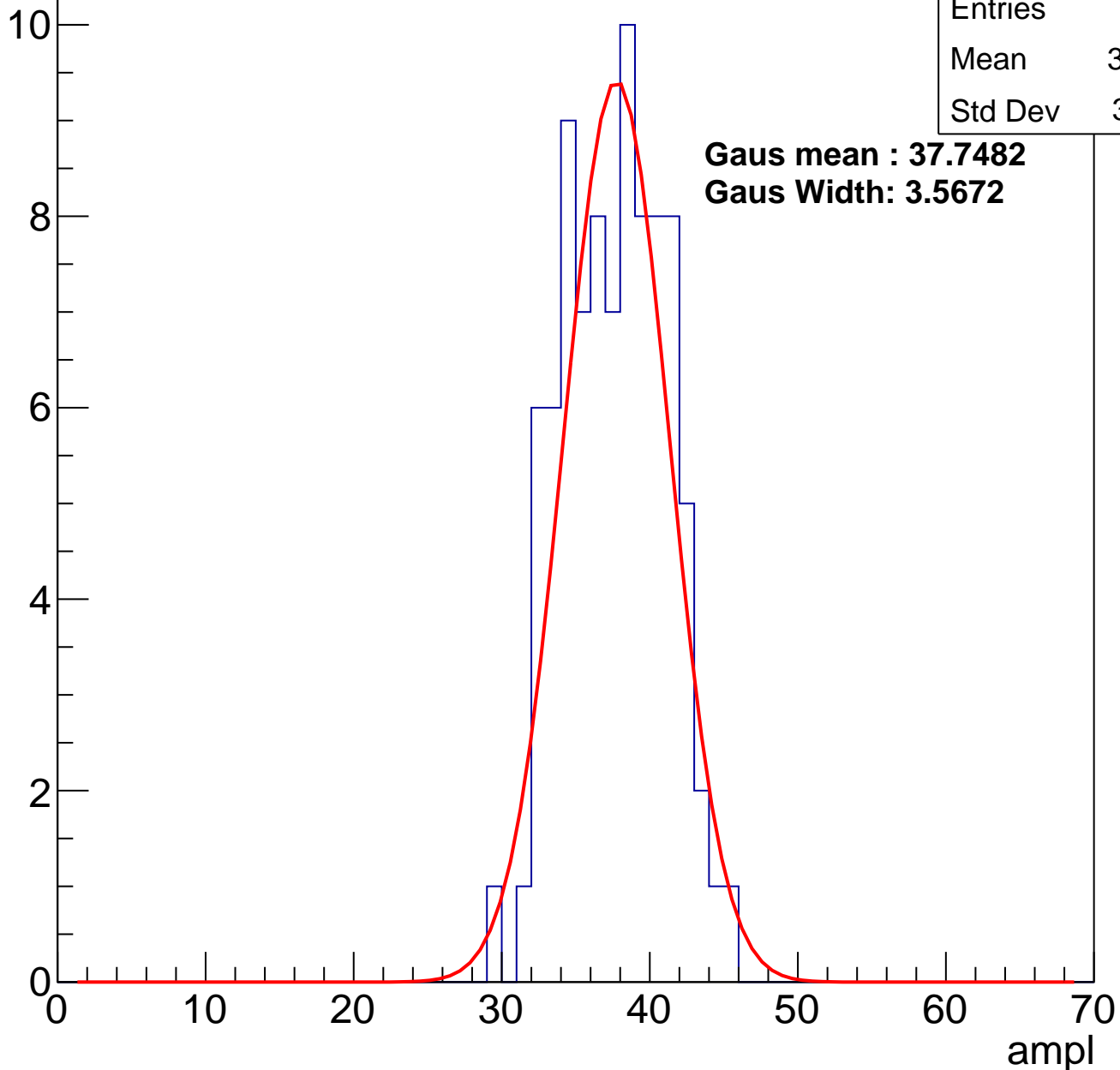
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	88
Mean	37.19
Std Dev	3.391

**Gaus mean : 37.7482**

**Gaus Width: 3.5672**

Entry



# B1L102S, U12-ch107, adc2

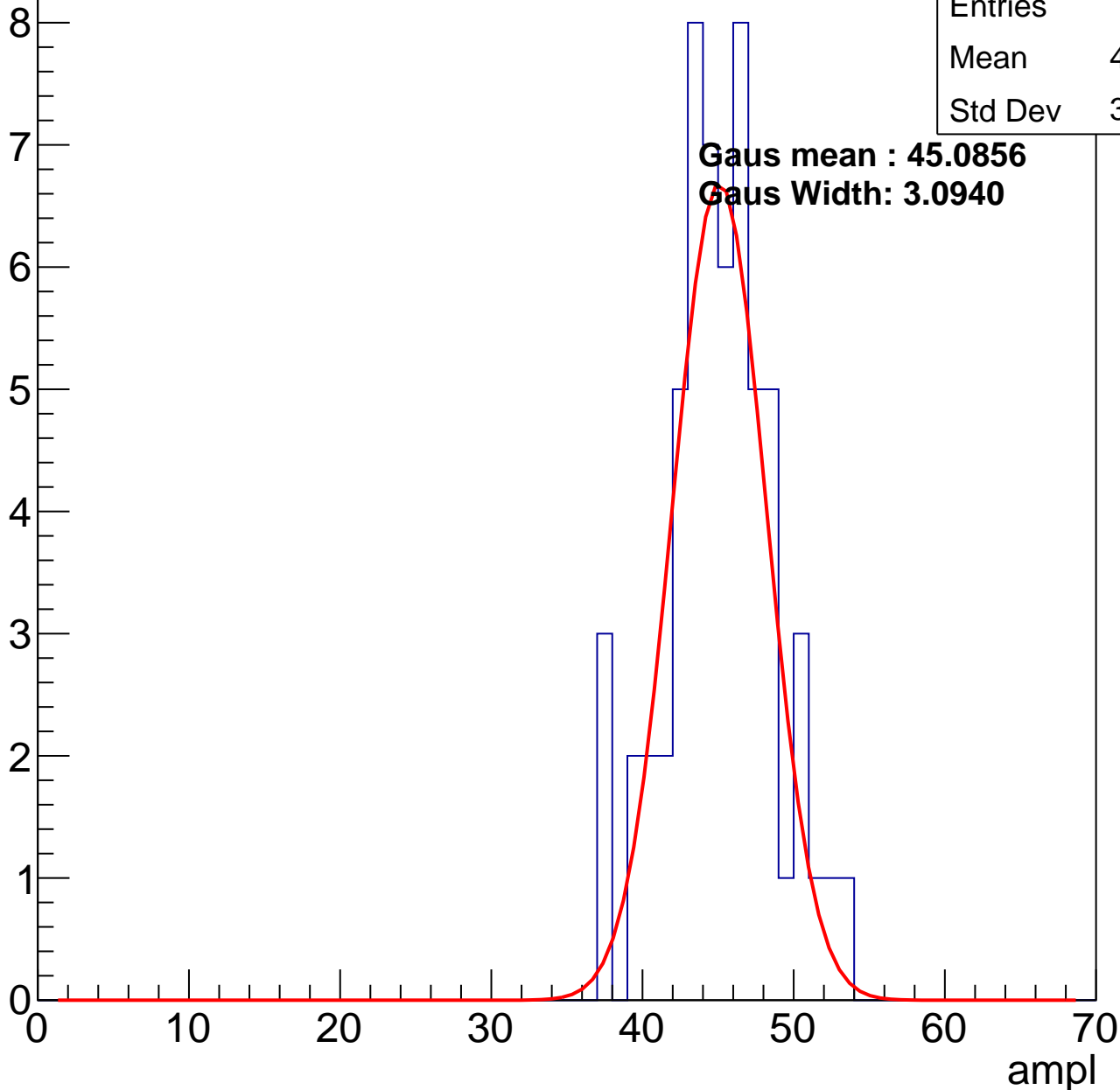
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	60
Mean	44.68
Std Dev	3.505

**Gaus mean : 45.0856**

**Gaus Width: 3.0940**

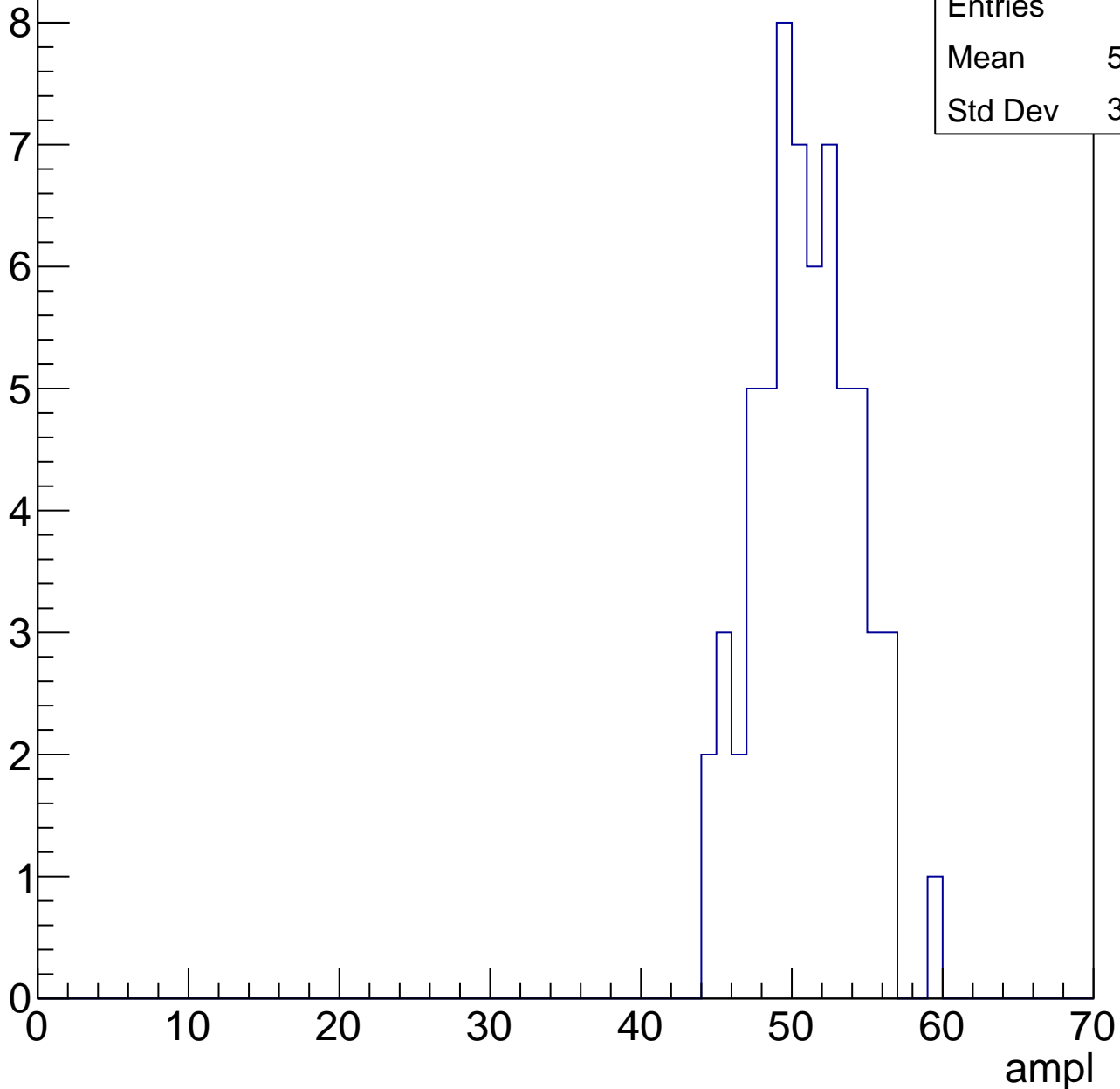


# B1L102S, U12-ch107, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	62
Mean	50.47
Std Dev	3.266

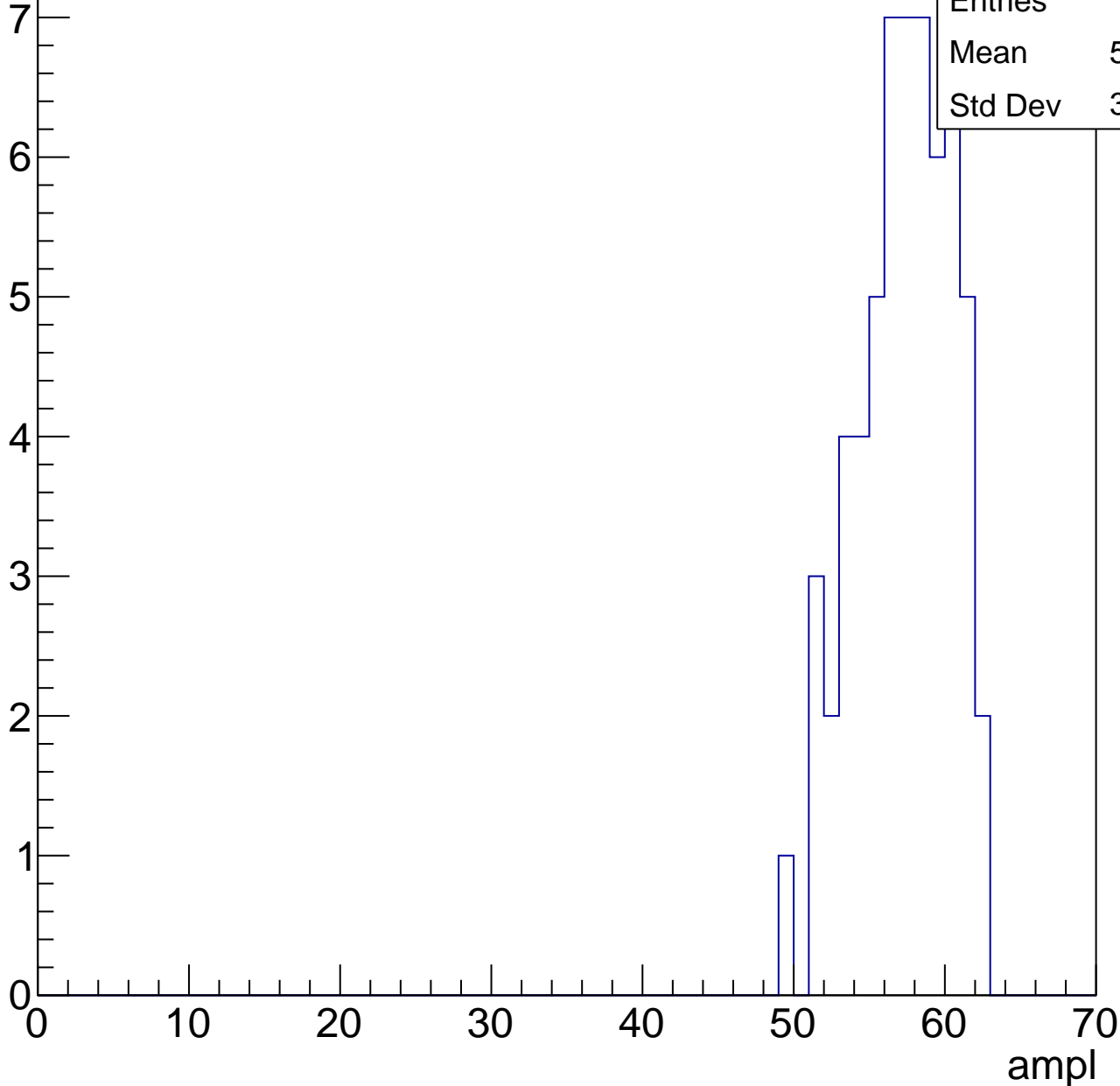


# B1L102S, U12-ch107, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	60
Mean	56.82
Std Dev	3.085

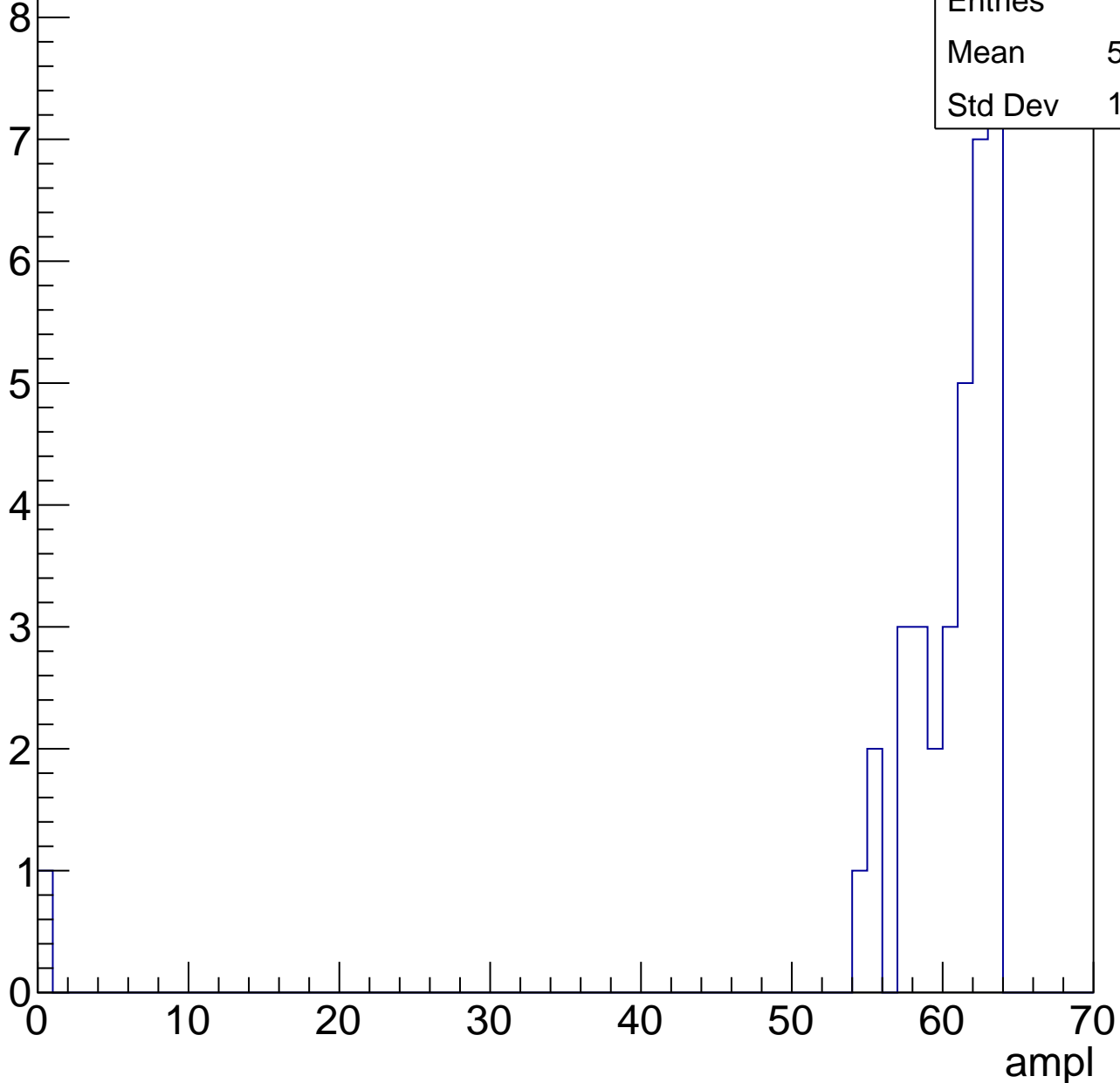


# B1L102S, U12-ch107, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

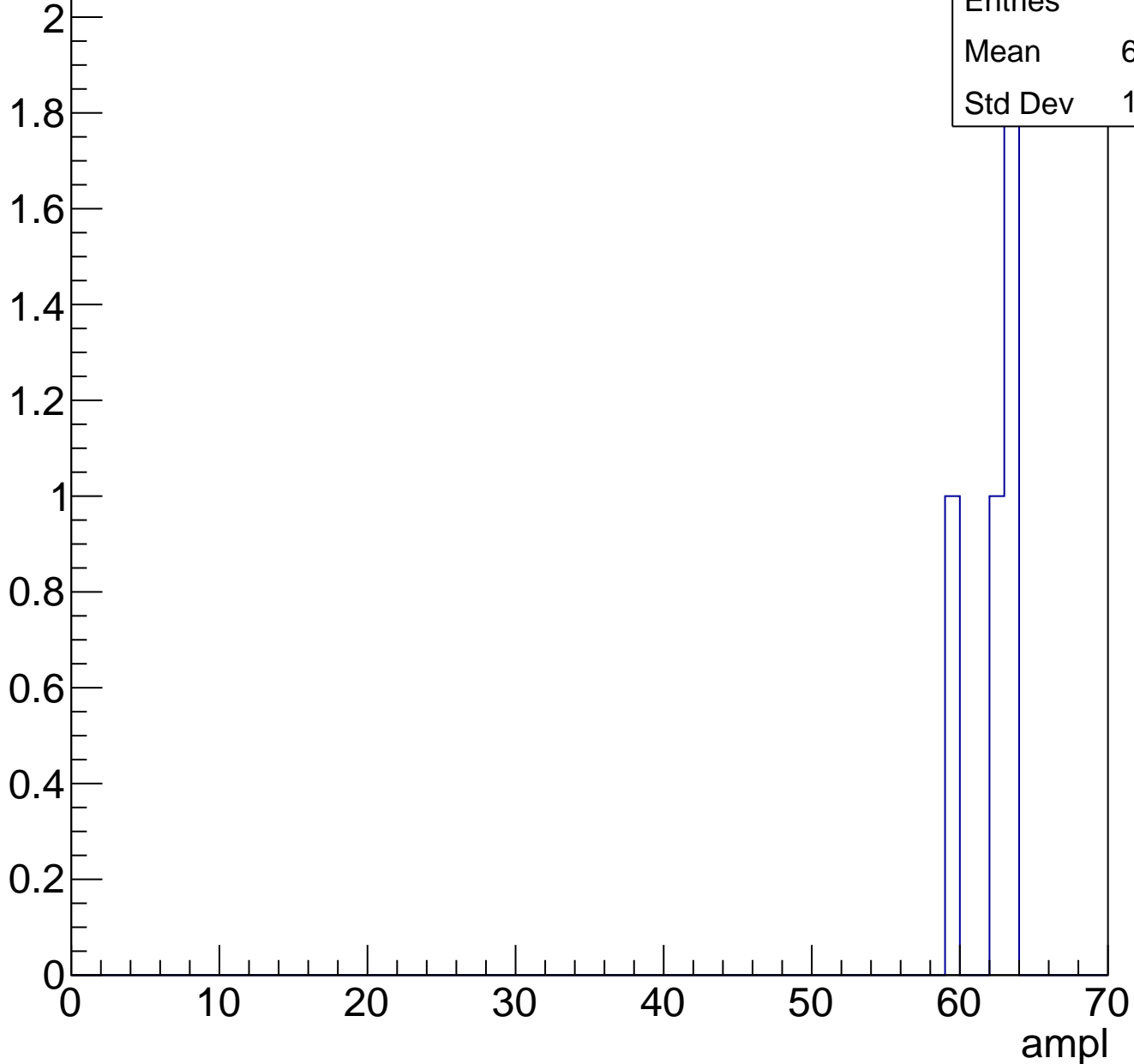
Entries	35
Mean	58.57
Std Dev	10.37



# B1L102S, U12-ch107, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U12-ch107, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U12-ch108, adc0

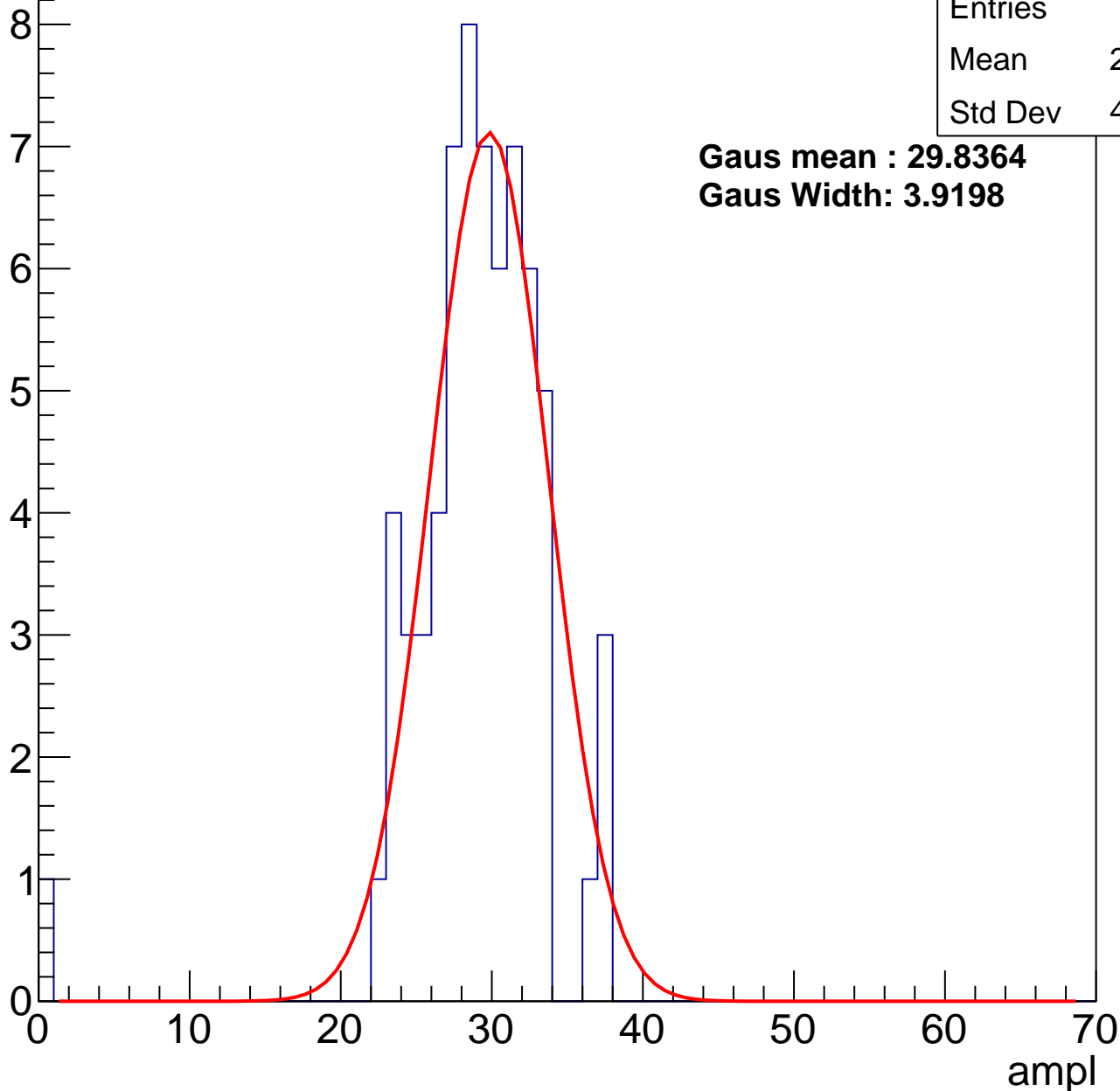
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	28.52
Std Dev	4.958

**Gaus mean : 29.8364**

**Gaus Width: 3.9198**



# B1L102S, U12-ch108, adc1

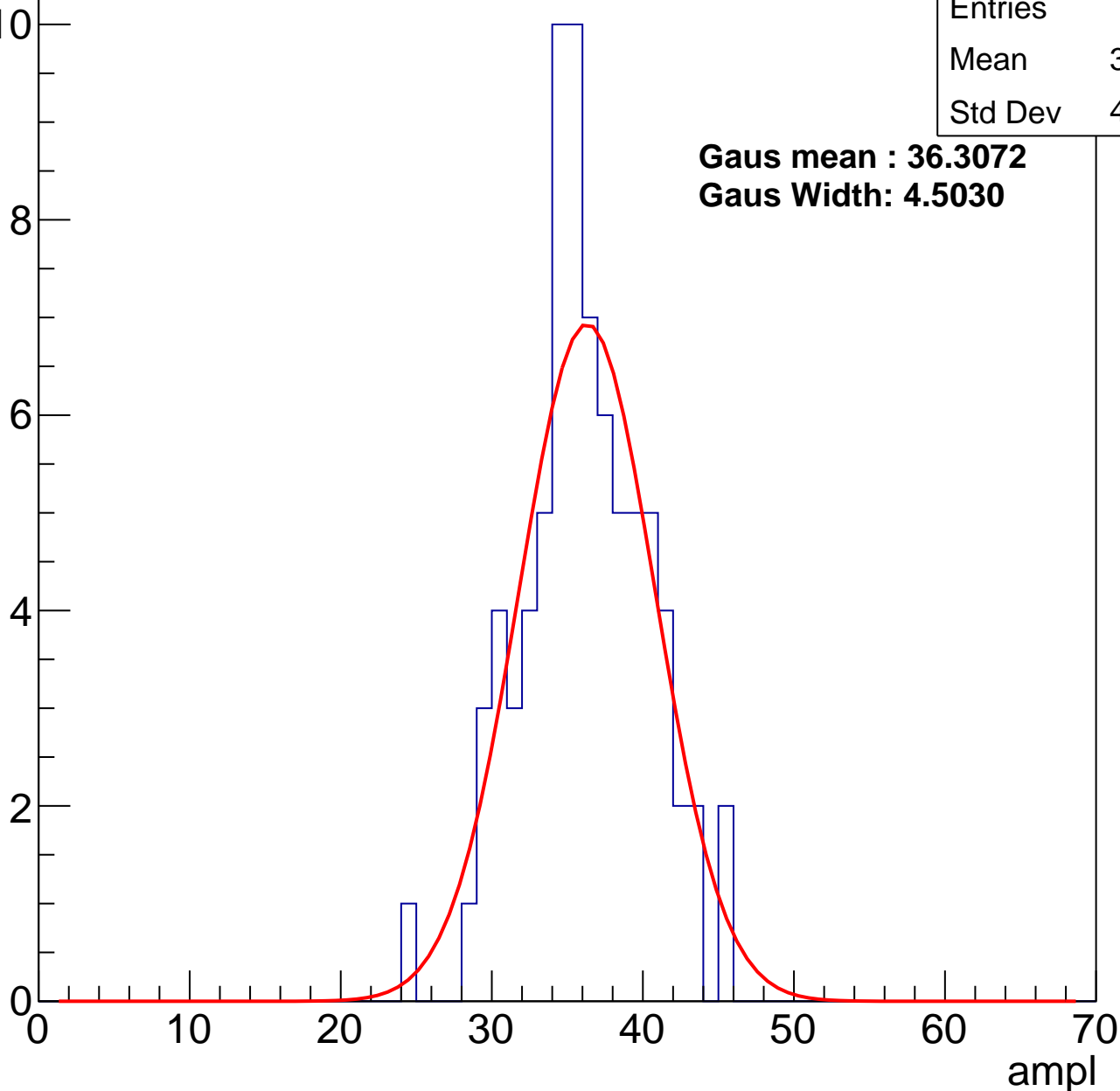
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	79
Mean	35.67
Std Dev	4.068

**Gaus mean : 36.3072**

**Gaus Width: 4.5030**



# B1L102S, U12-ch108, adc2

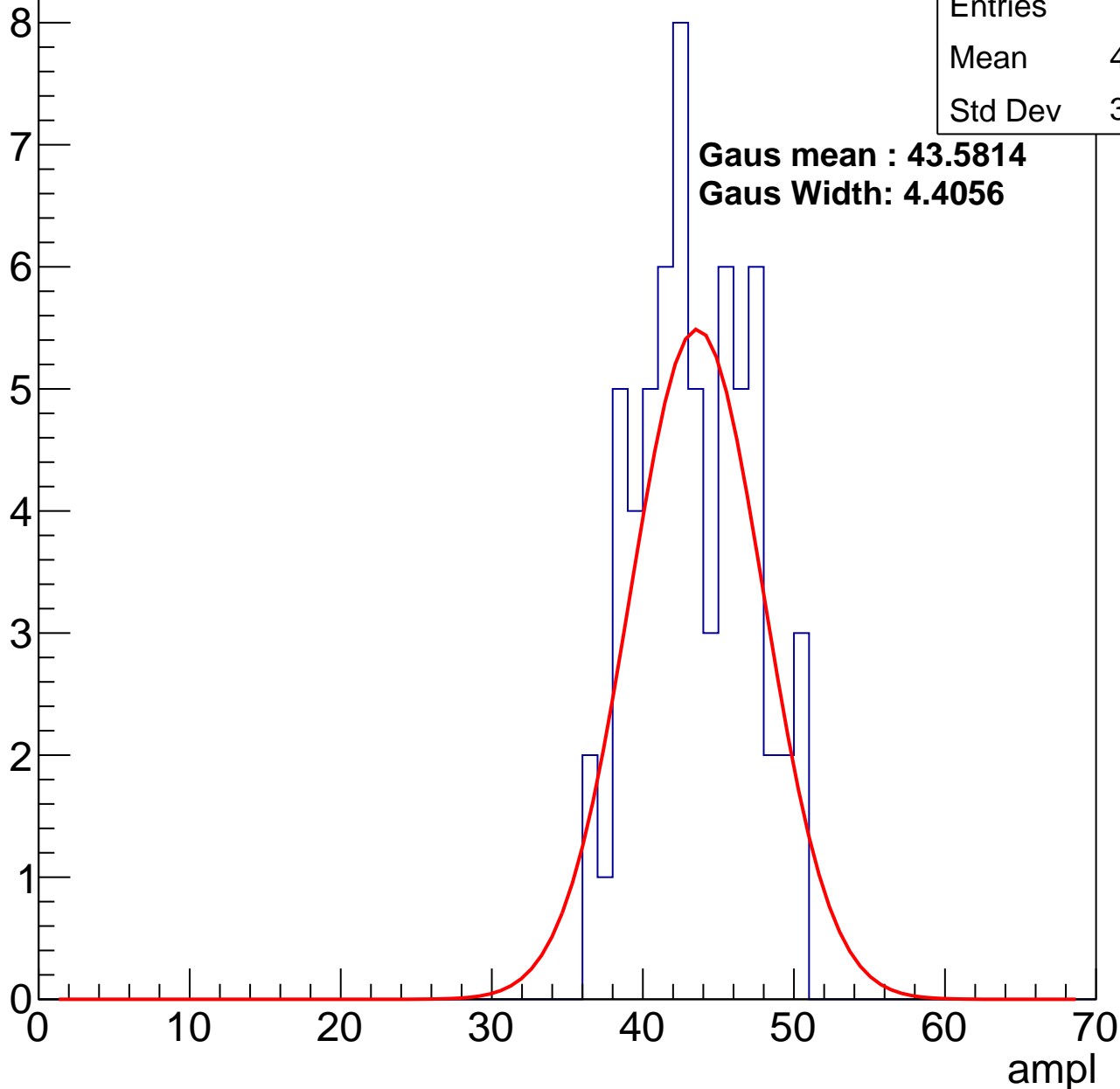
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	63
Mean	43.02
Std Dev	3.645

**Gaus mean : 43.5814**

**Gaus Width: 4.4056**

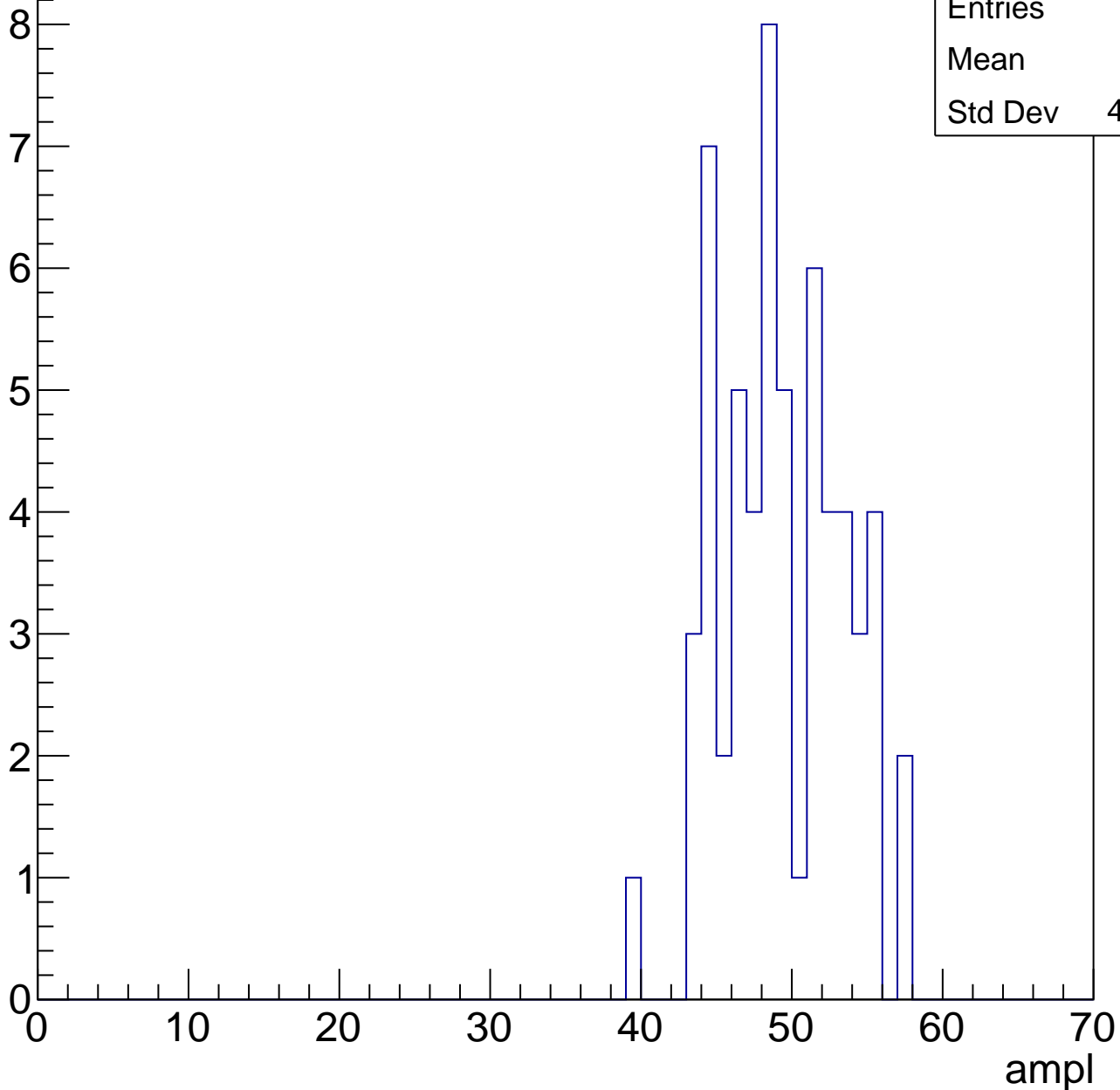


# B1L102S, U12-ch108, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	59
Mean	48.9
Std Dev	4.024

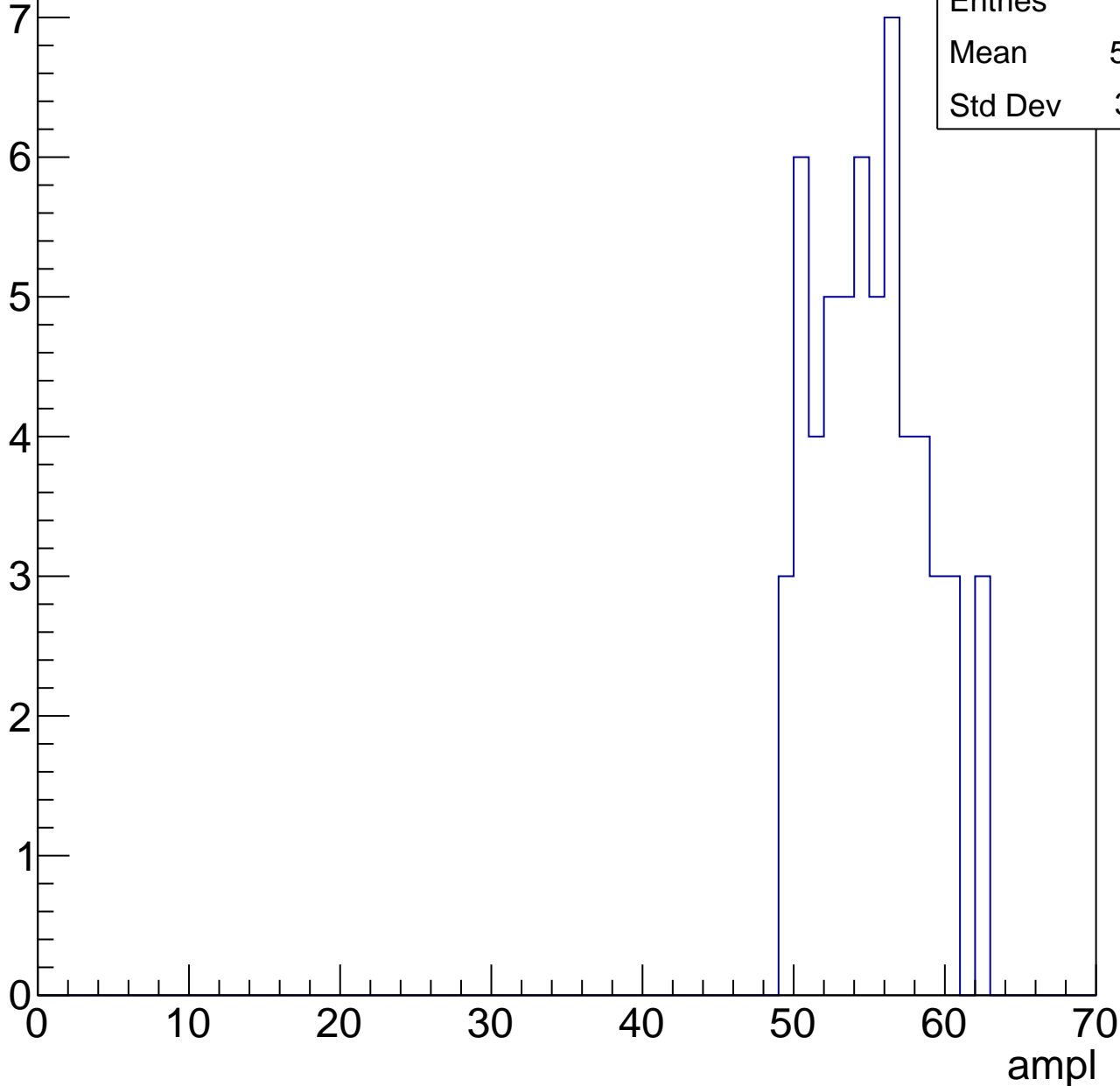


# B1L102S, U12-ch108, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	58
Mean	54.66
Std Dev	3.511

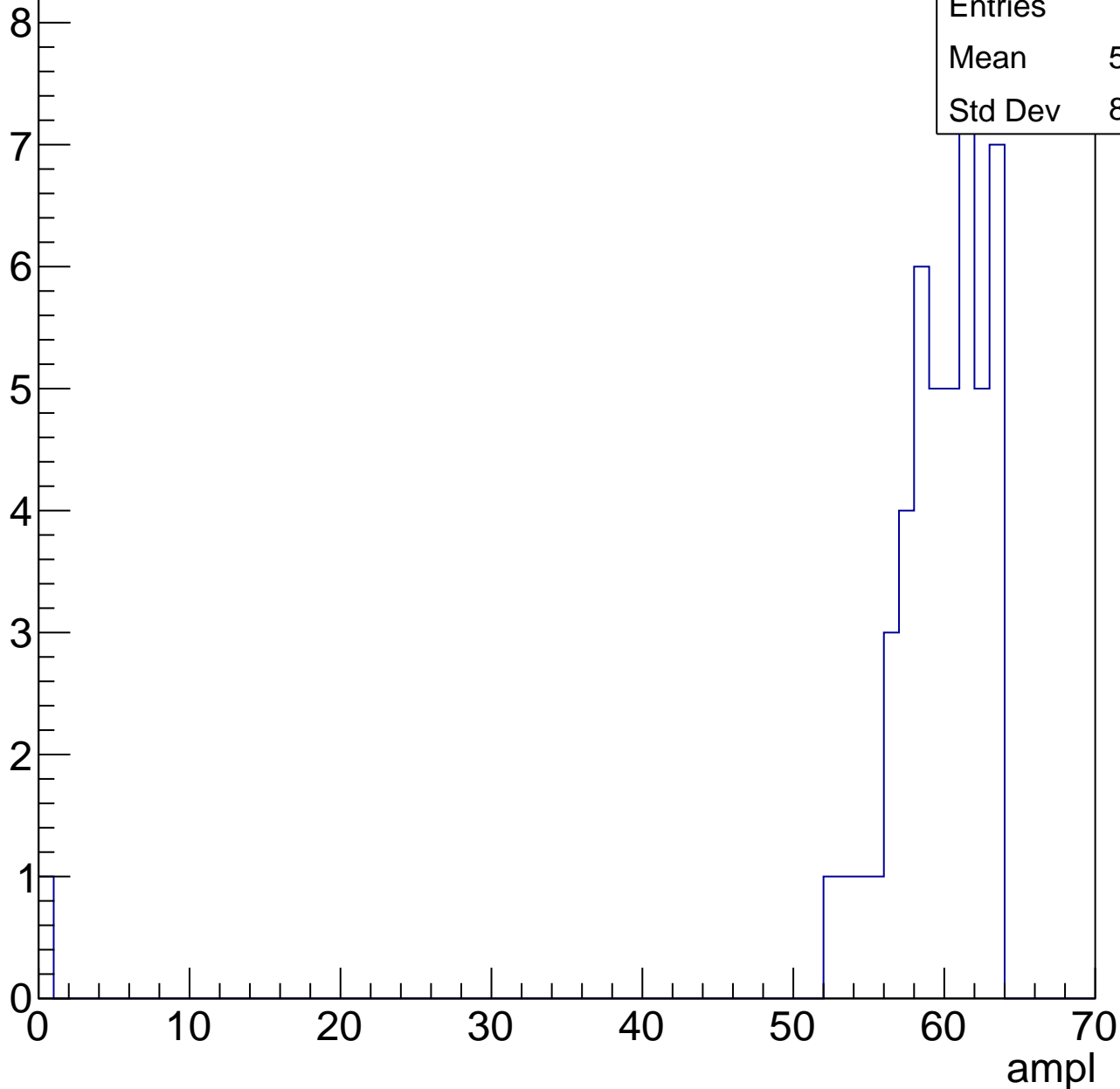


# B1L102S, U12-ch108, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	48
Mean	58.17
Std Dev	8.917



# B1L102S, U12-ch108, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

3

2.5

2

1.5

1

0.5

0

Entries

11

Mean

61.18

Std Dev

1.466

ampl

0

10

20

30

40

50

60

70



# B1L102S, U12-ch108, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U12-ch109, adc0

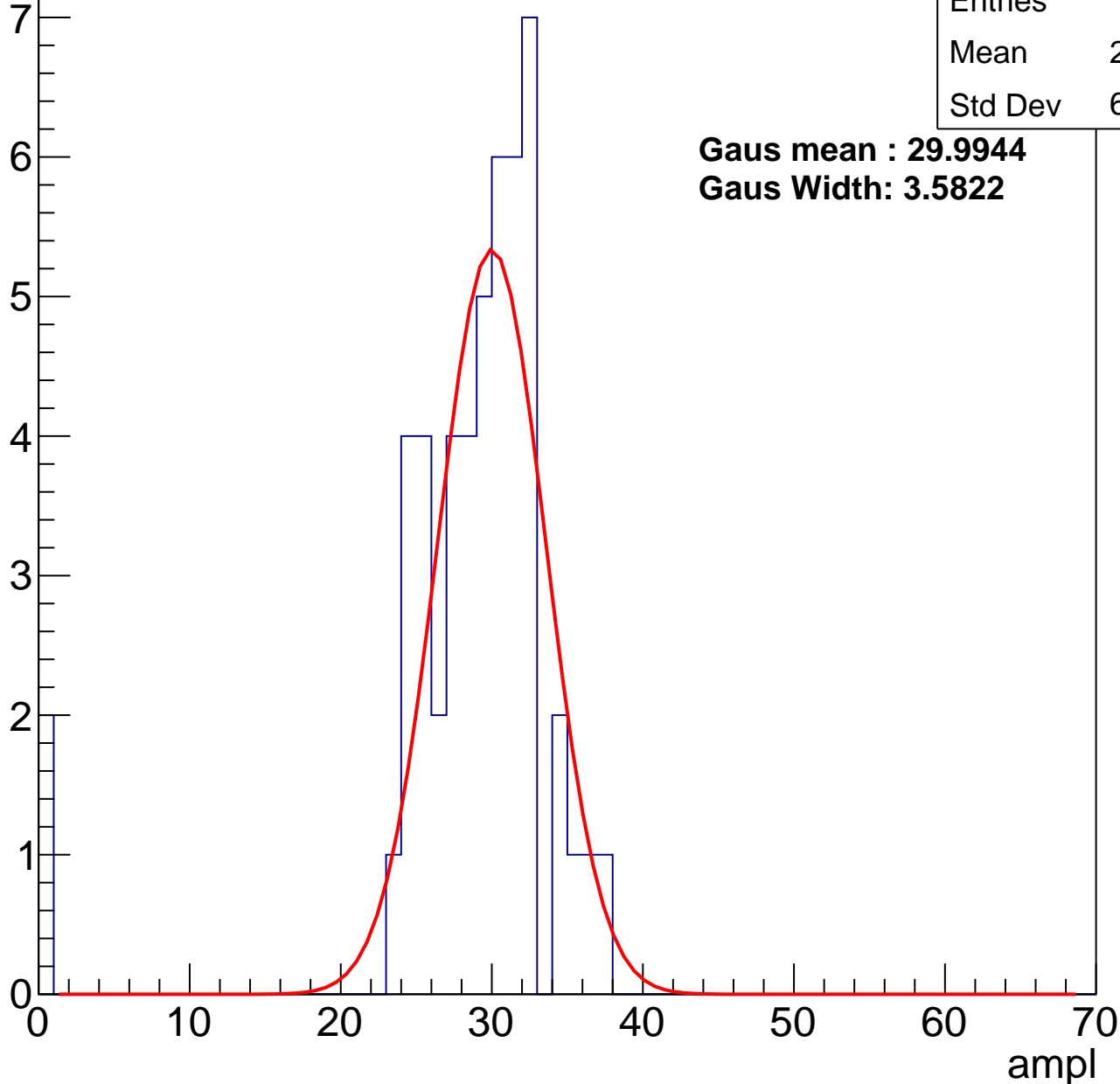
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	50
Mean	28.04
Std Dev	6.582

**Gaus mean : 29.9944**

**Gaus Width: 3.5822**



# B1L102S, U12-ch109, adc1

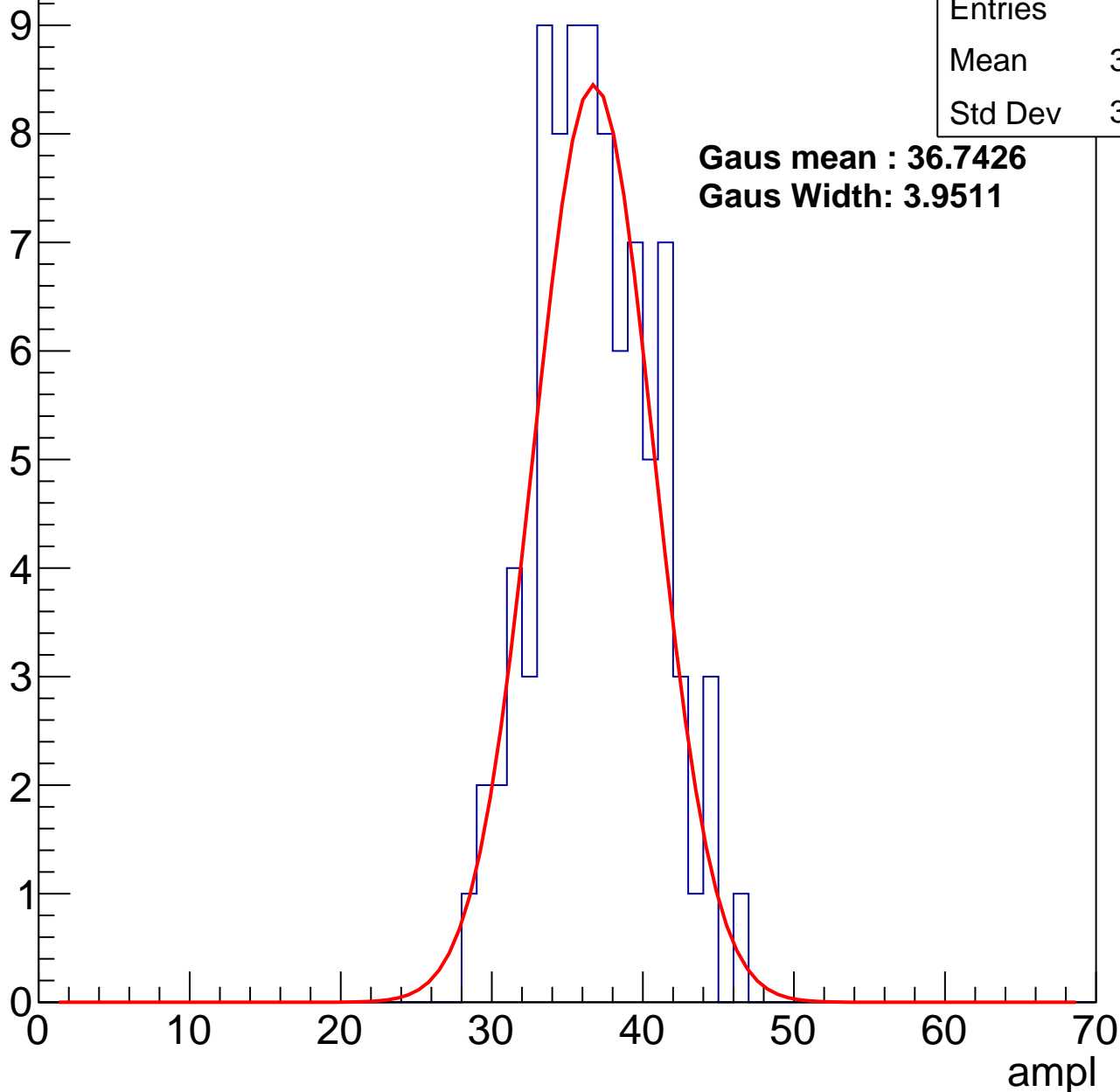
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	88
Mean	36.42
Std Dev	3.825

**Gaus mean : 36.7426**

**Gaus Width: 3.9511**



# B1L102S, U12-ch109, adc2

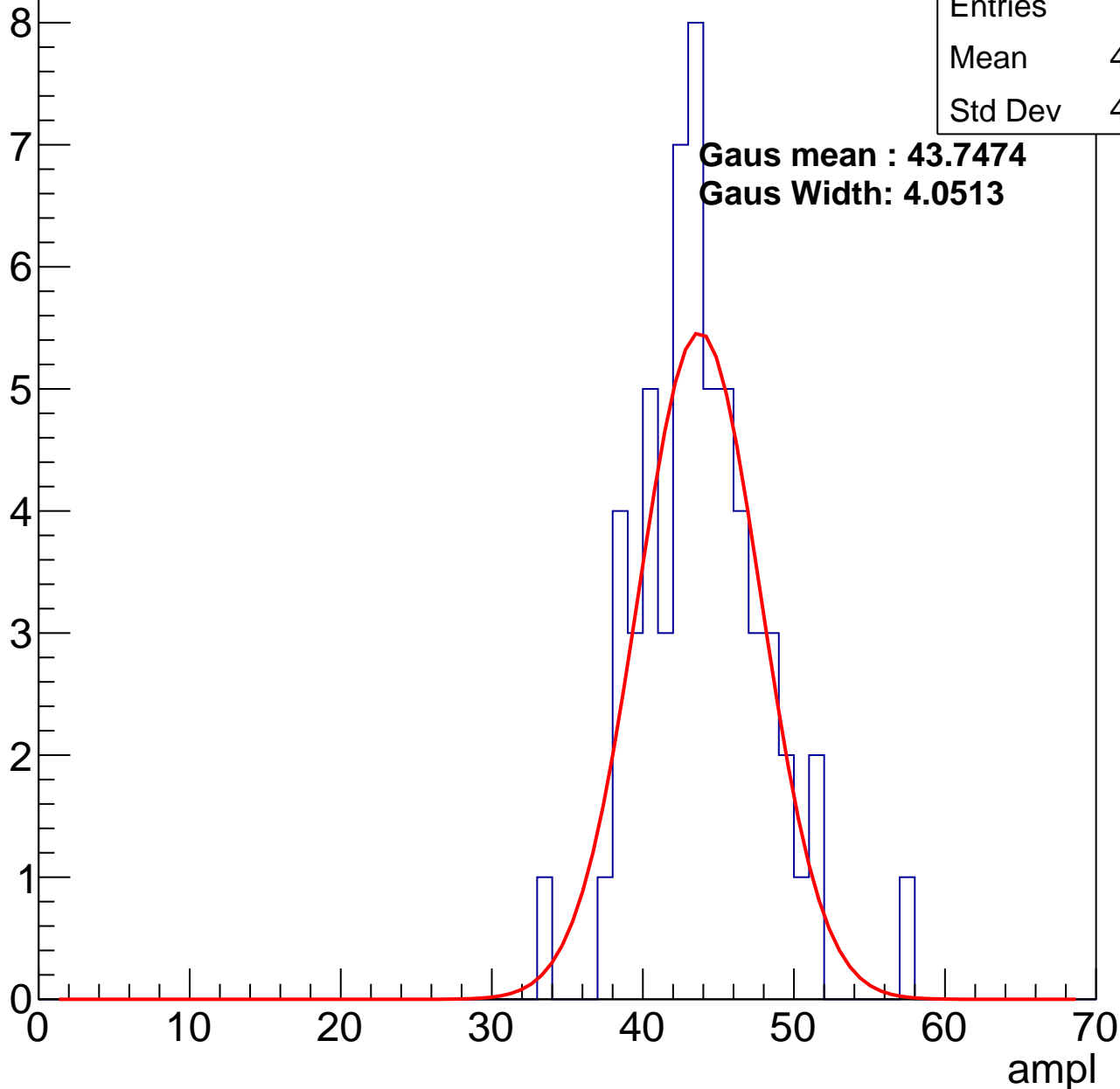
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	58
Mean	43.47
Std Dev	4.078

**Gaus mean : 43.7474**

**Gaus Width: 4.0513**

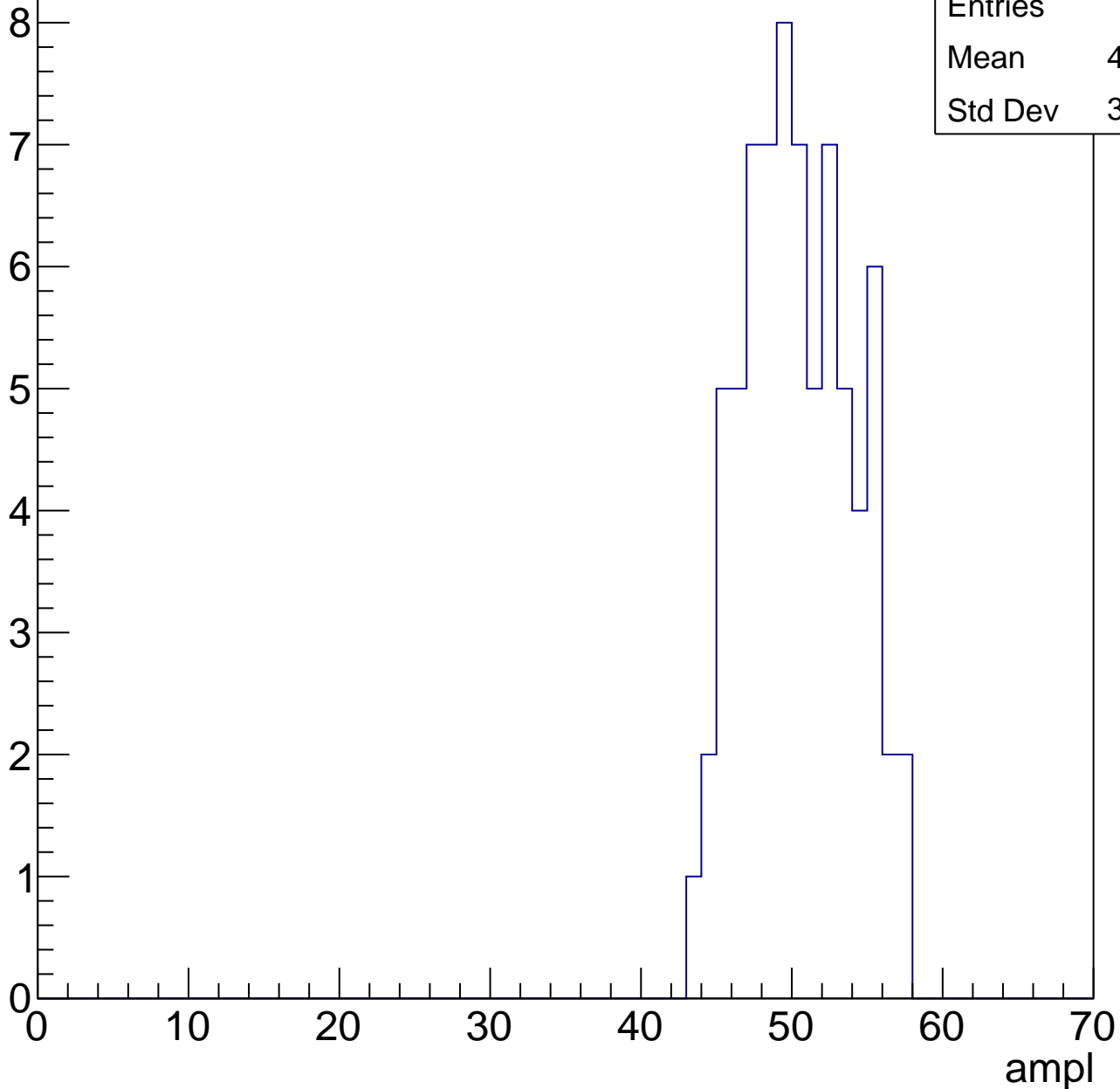


# B1L102S, U12-ch109, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	73
Mean	49.99
Std Dev	3.486

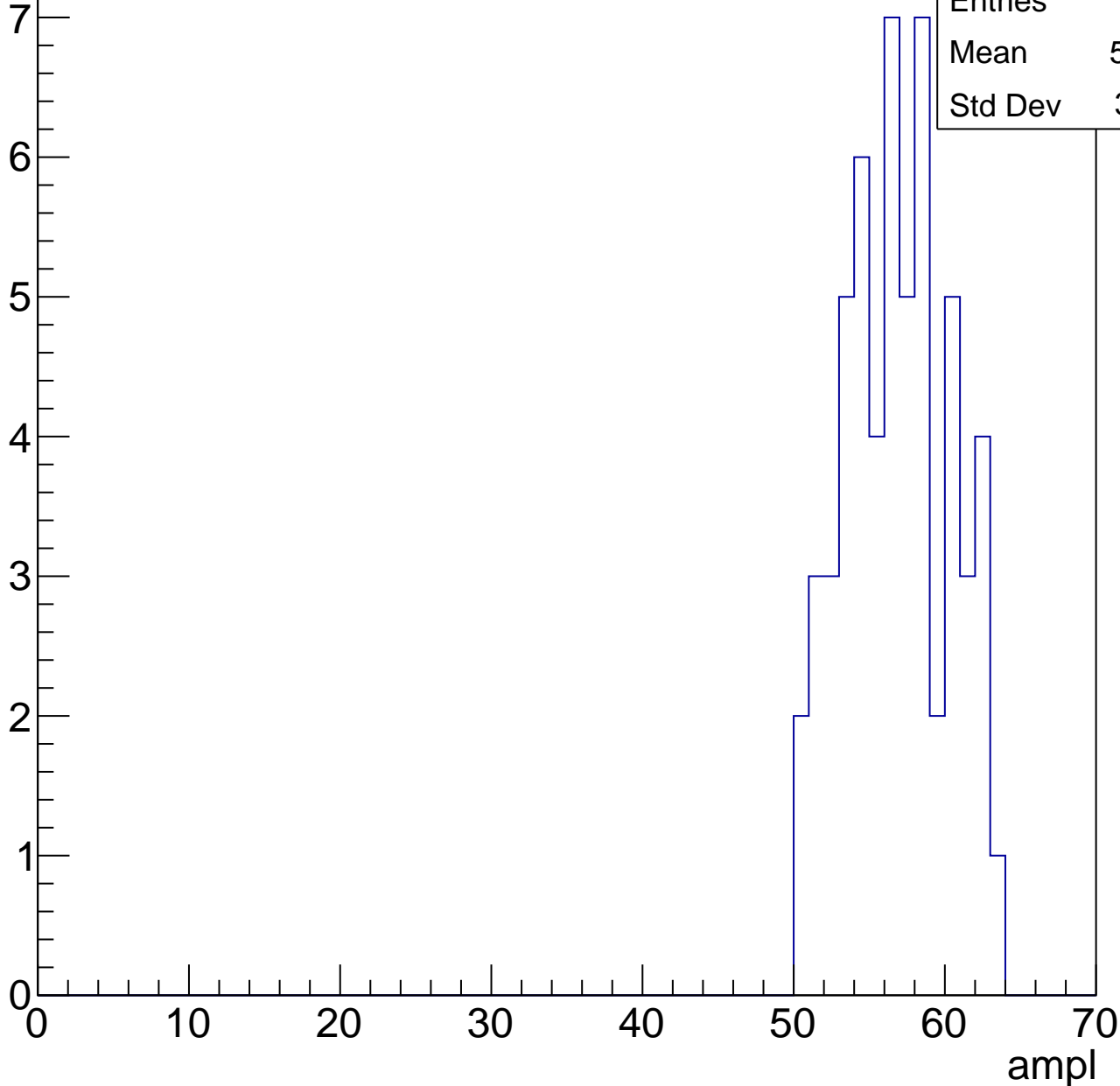


# B1L102S, U12-ch109, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	57
Mean	56.37
Std Dev	3.401

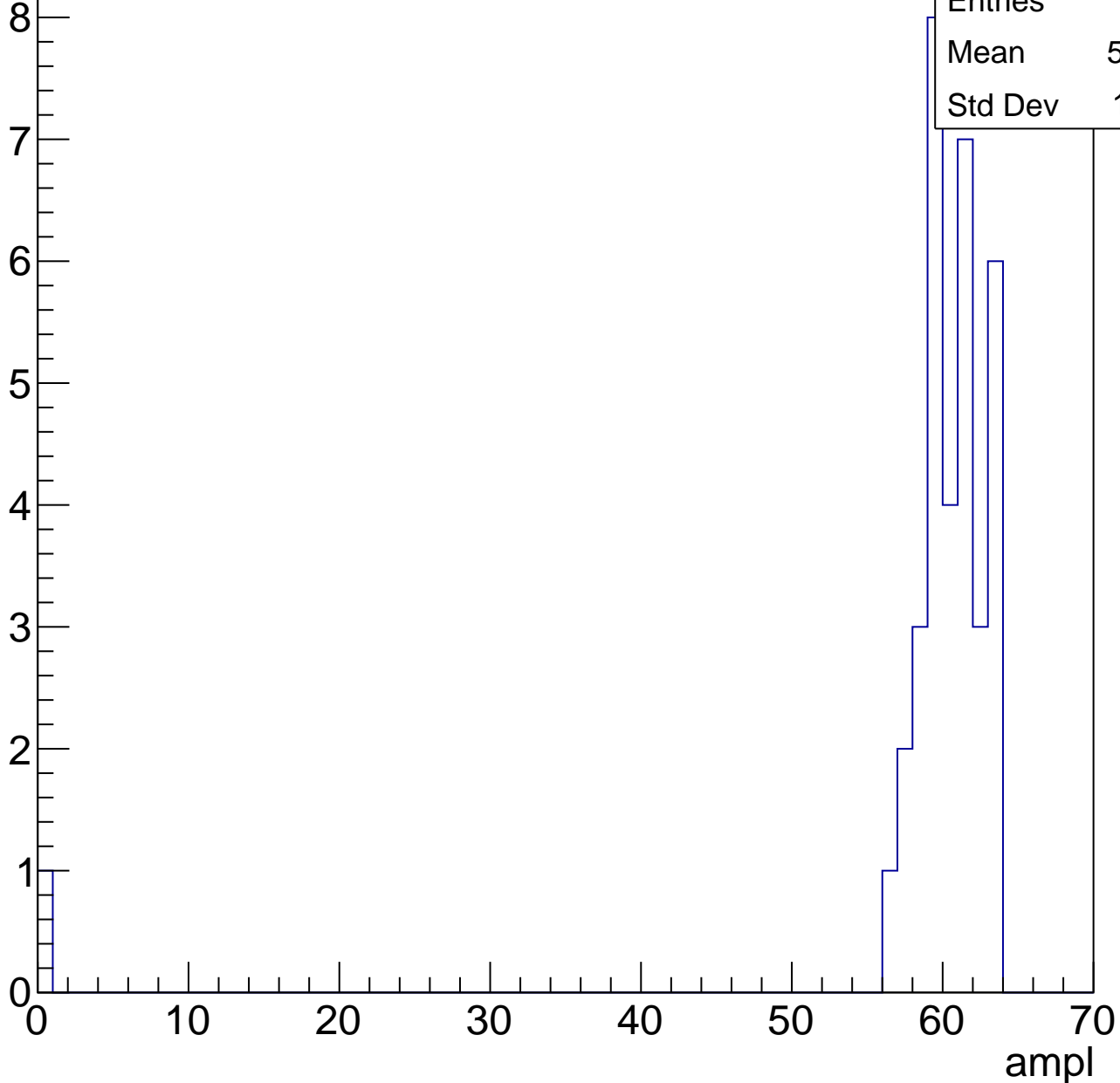


# B1L102S, U12-ch109, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	35
Mean	58.49
Std Dev	10.21



# B1L102S, U12-ch109, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U12-ch109, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U12-ch110, adc0

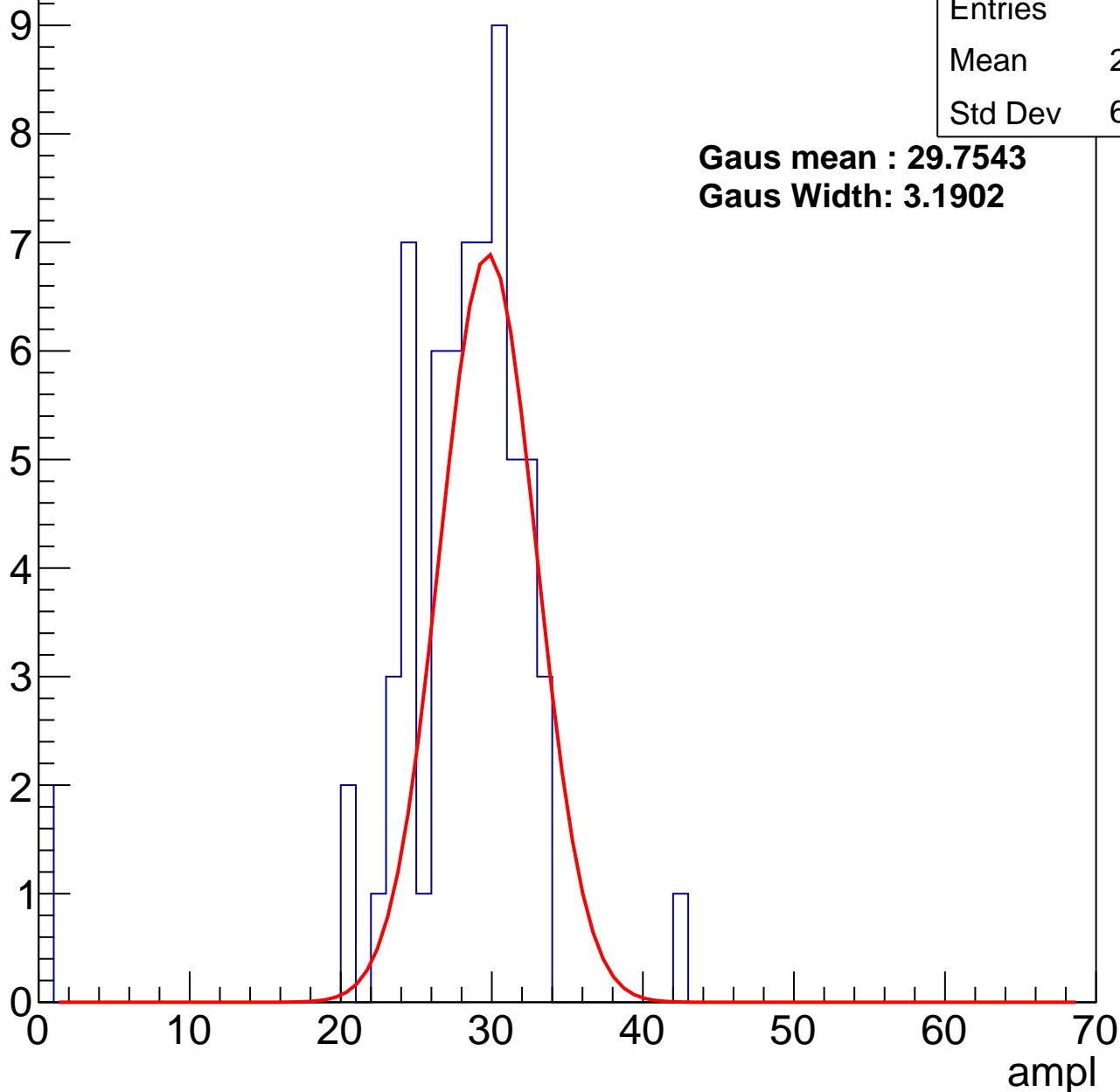
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	65
Mean	27.18
Std Dev	6.018

**Gaus mean : 29.7543**

**Gaus Width: 3.1902**



# B1L102S, U12-ch110, adc1

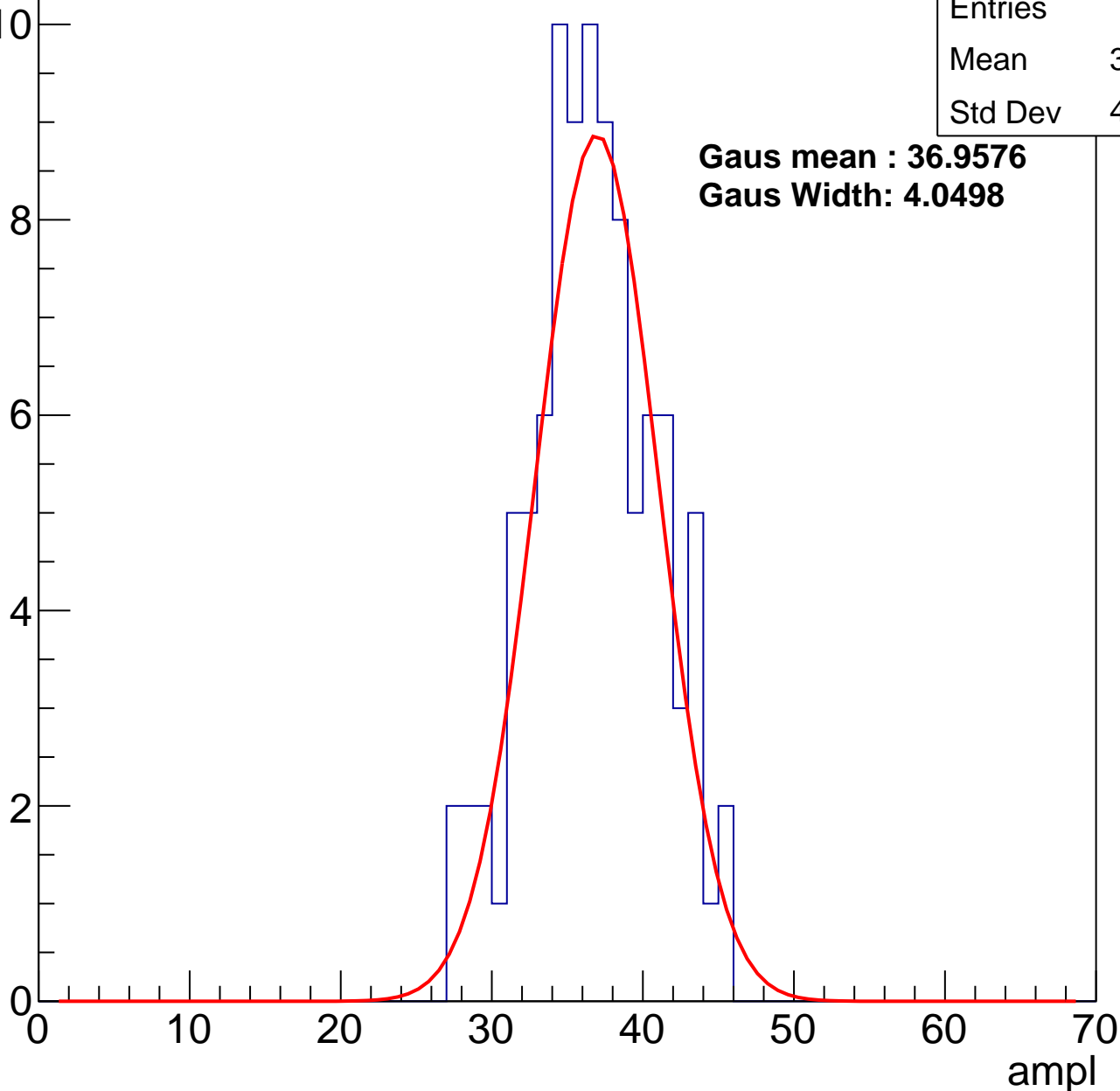
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	97
Mean	36.28
Std Dev	4.106

**Gaus mean : 36.9576**

**Gaus Width: 4.0498**



# B1L102S, U12-ch110, adc2

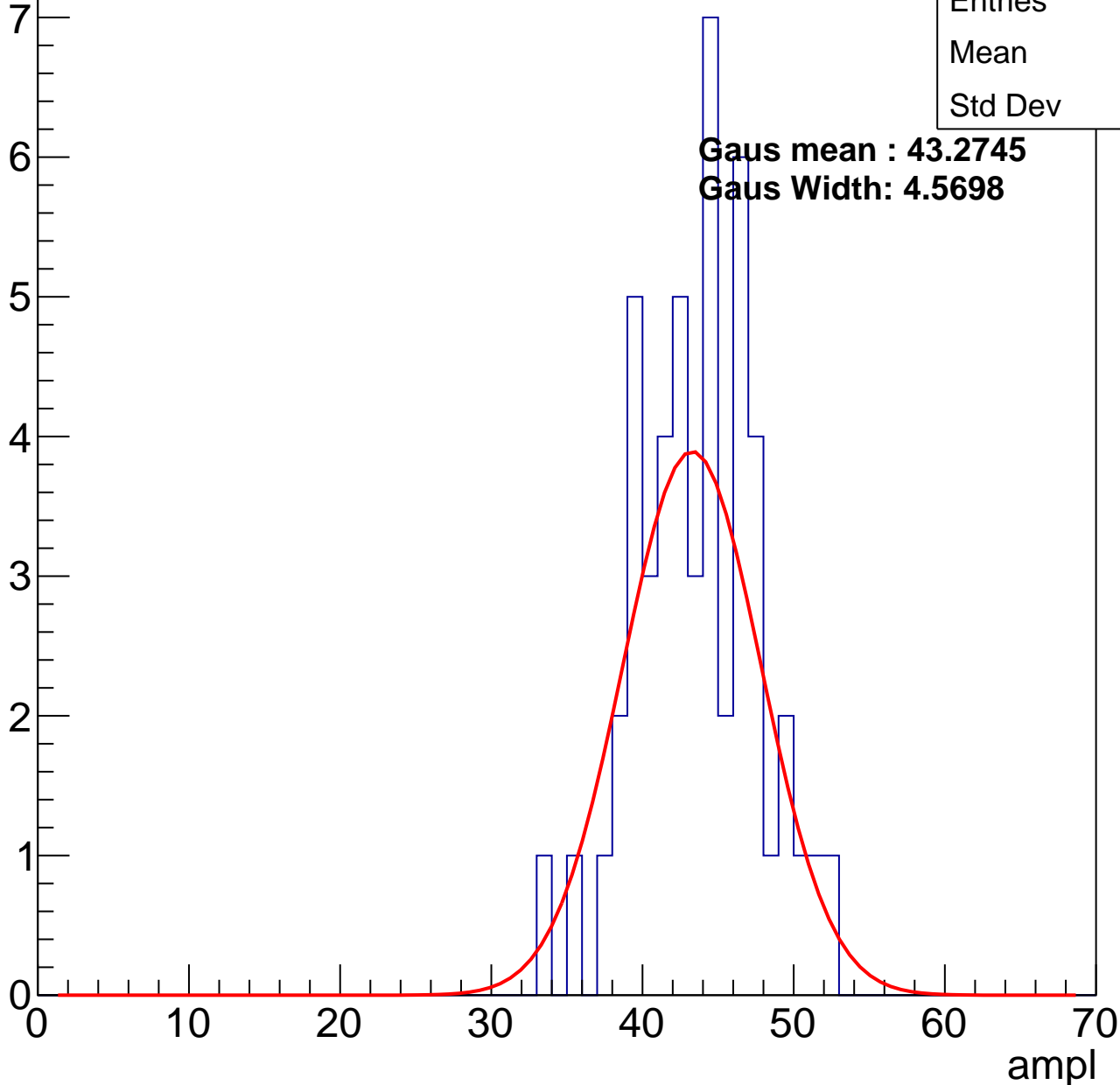
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	50
Mean	43.2
Std Dev	4

**Gaus mean : 43.2745**

**Gaus Width: 4.5698**

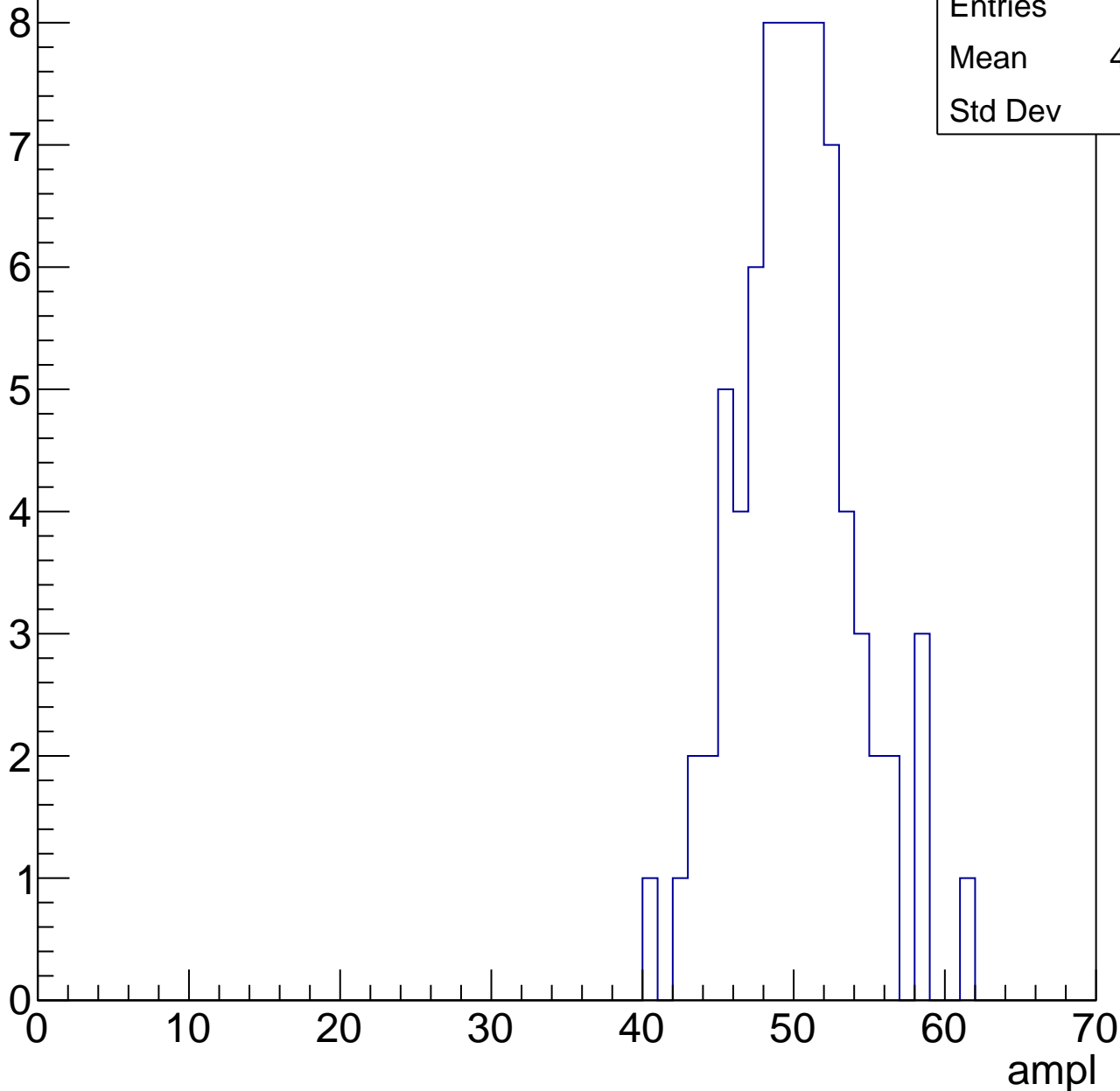


# B1L102S, U12-ch110, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	75
Mean	49.68
Std Dev	3.94



# B1L102S, U12-ch110, adc4

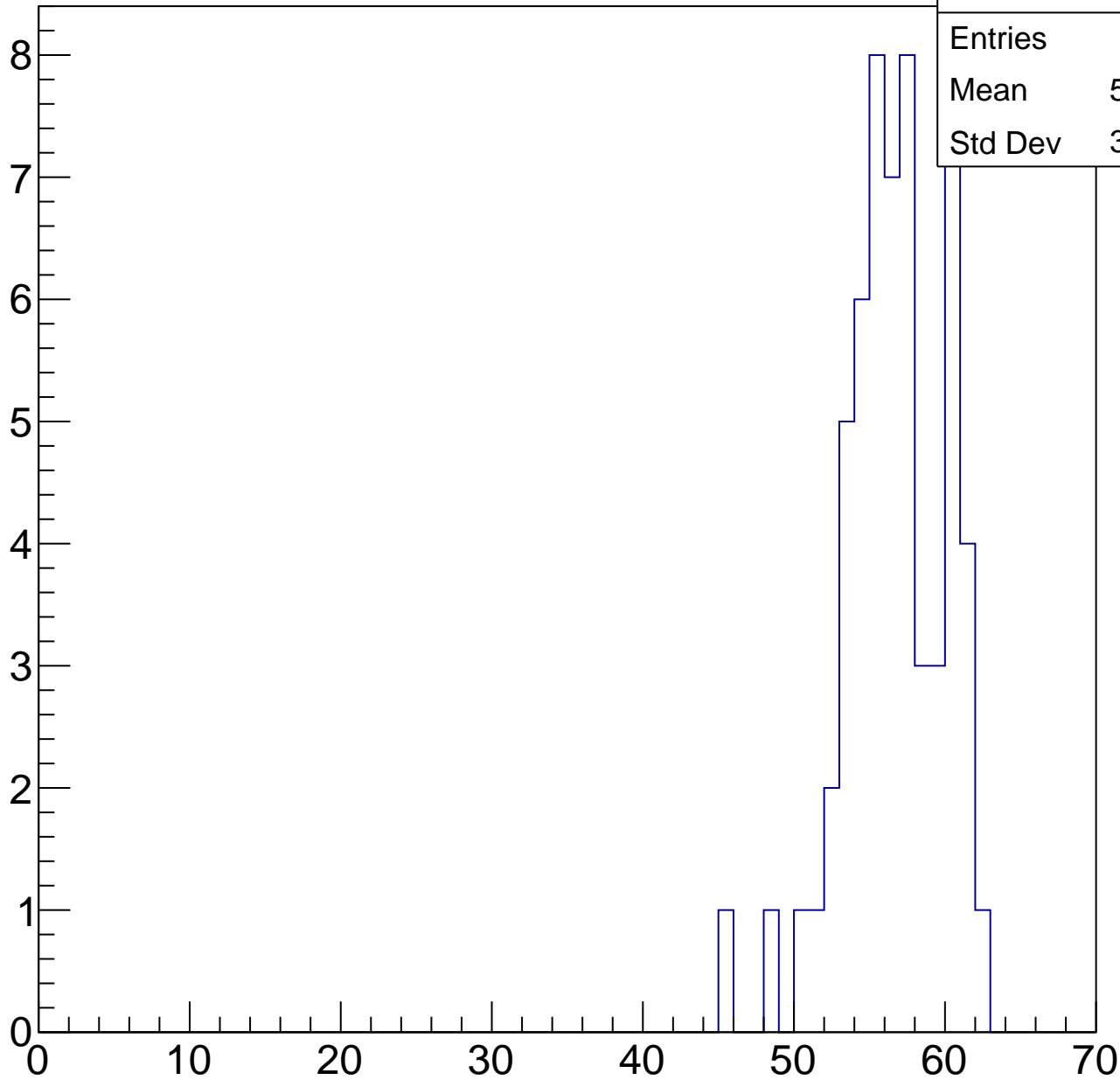
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	59
Mean	56.14
Std Dev	3.357

ampl

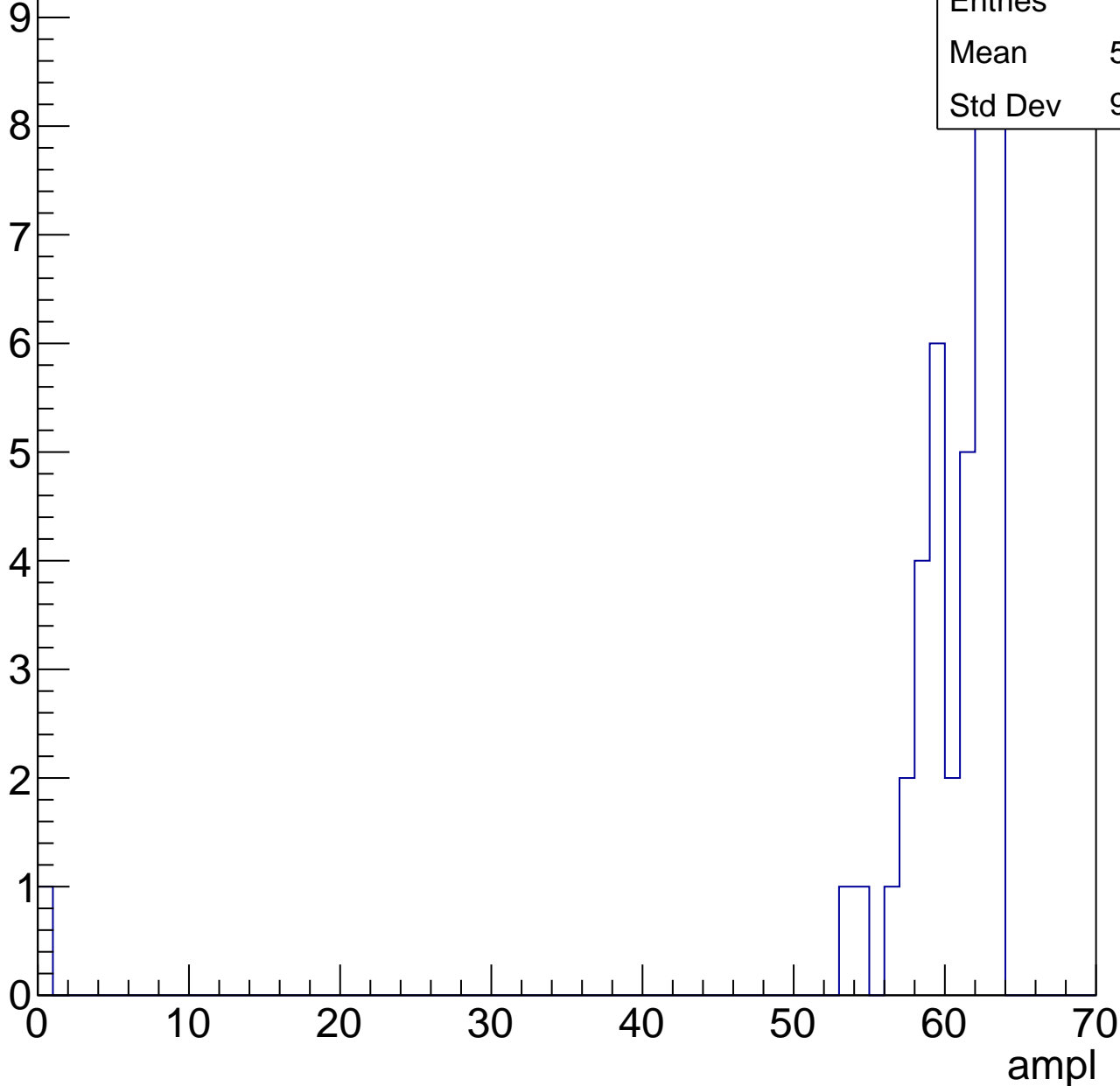


# B1L102S, U12-ch110, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	40
Mean	58.75
Std Dev	9.736



# B1L102S, U12-ch110, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

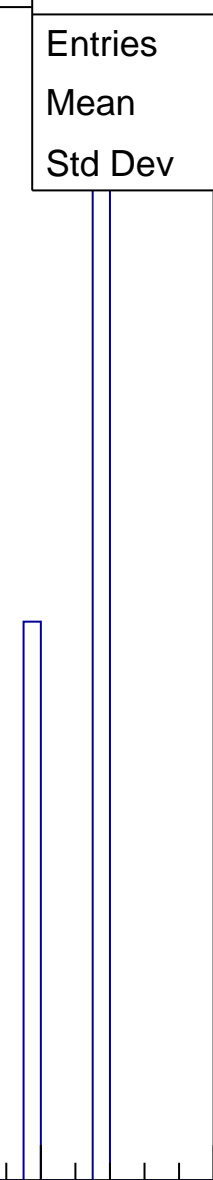
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	3
Mean	61.67
Std Dev	1.886

0 10 20 30 40 50 60 70

ampl





# B1L102S, U12-ch110, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

1

0.8

0.6

0.4

0.2

0

0

10

20

30

40

50

60

70

ampl

Entries

0

Mean

0

Std Dev

0

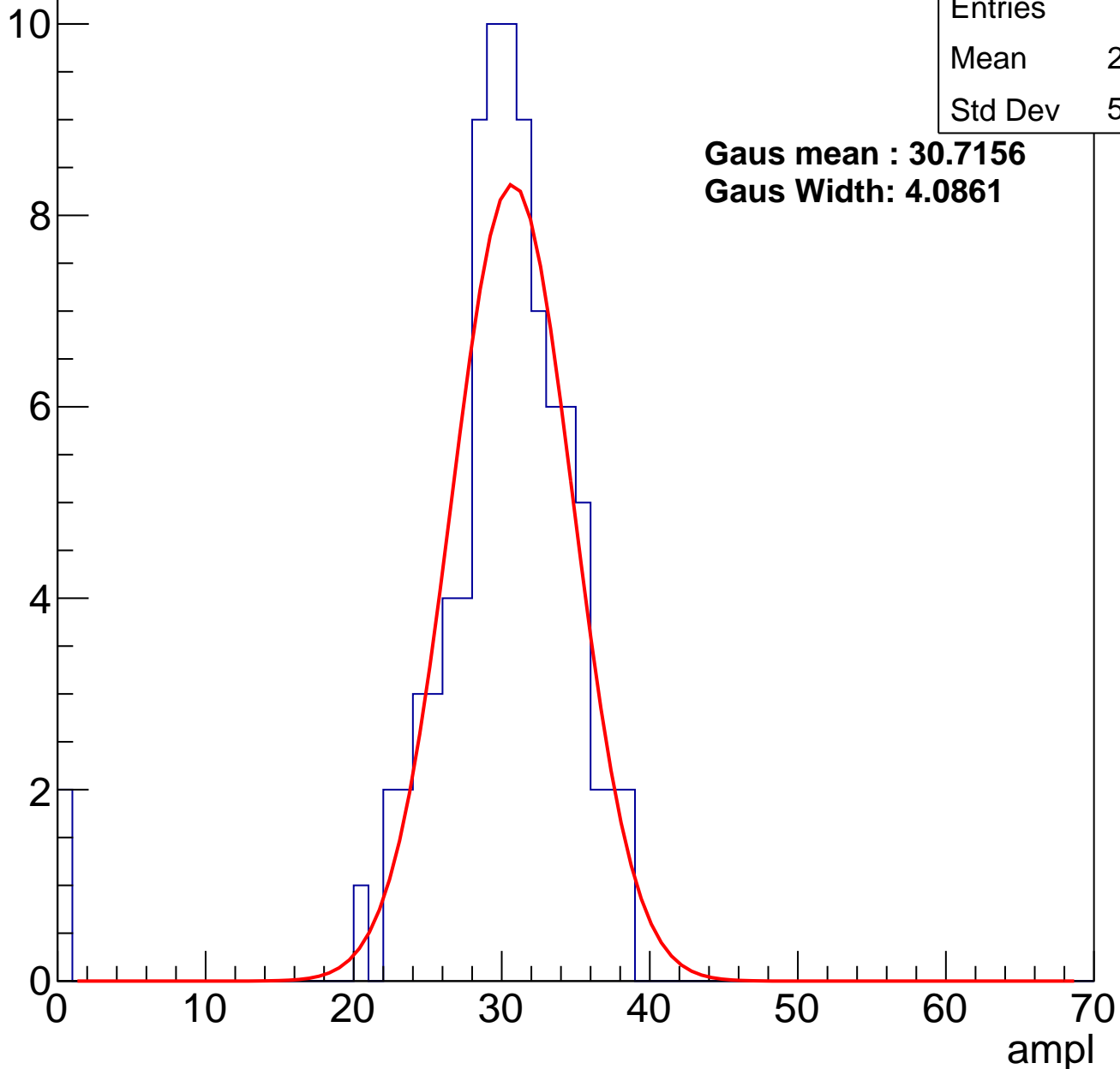
# B1L102S, U12-ch111, adc0

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	89
Mean	29.36
Std Dev	5.833

**Gaus mean : 30.7156**  
**Gaus Width: 4.0861**

Entry



# B1L102S, U12-ch111, adc1

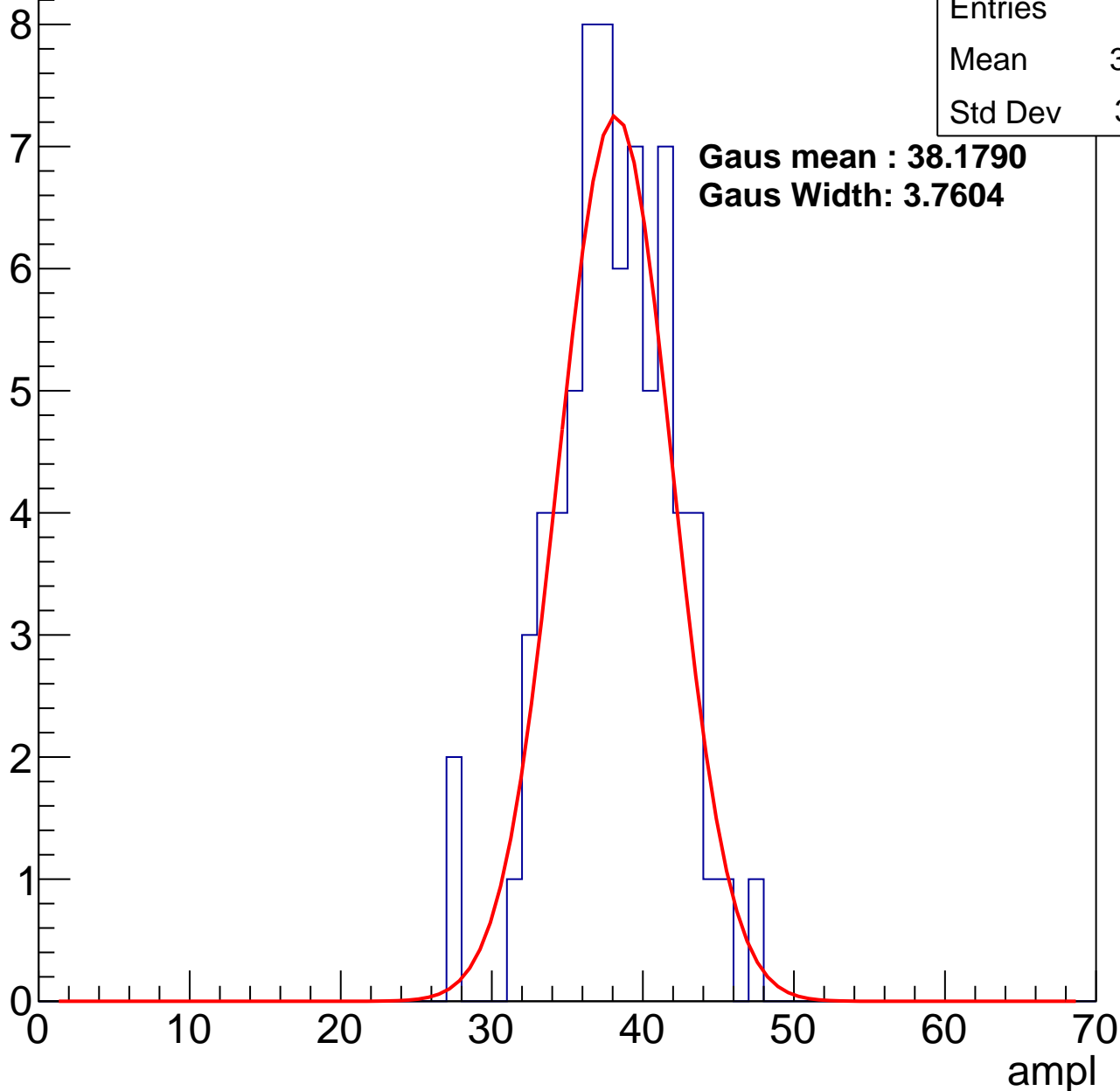
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	71
Mean	37.63
Std Dev	3.861

**Gaus mean : 38.1790**

**Gaus Width: 3.7604**



# B1L102S, U12-ch111, adc2

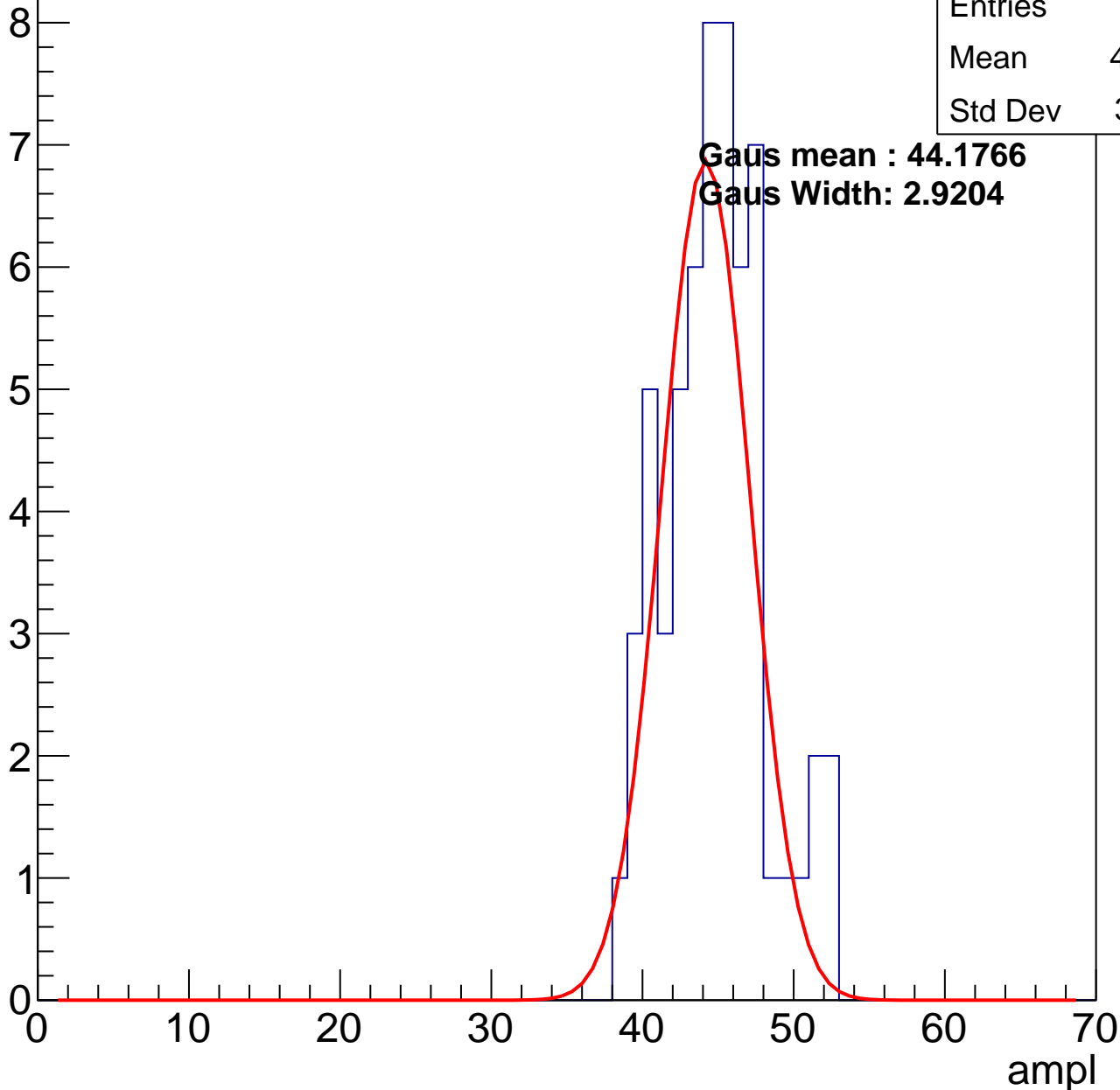
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	59
Mean	44.34
Std Dev	3.281

Gaus mean : 44.1766

Gaus Width: 2.9204

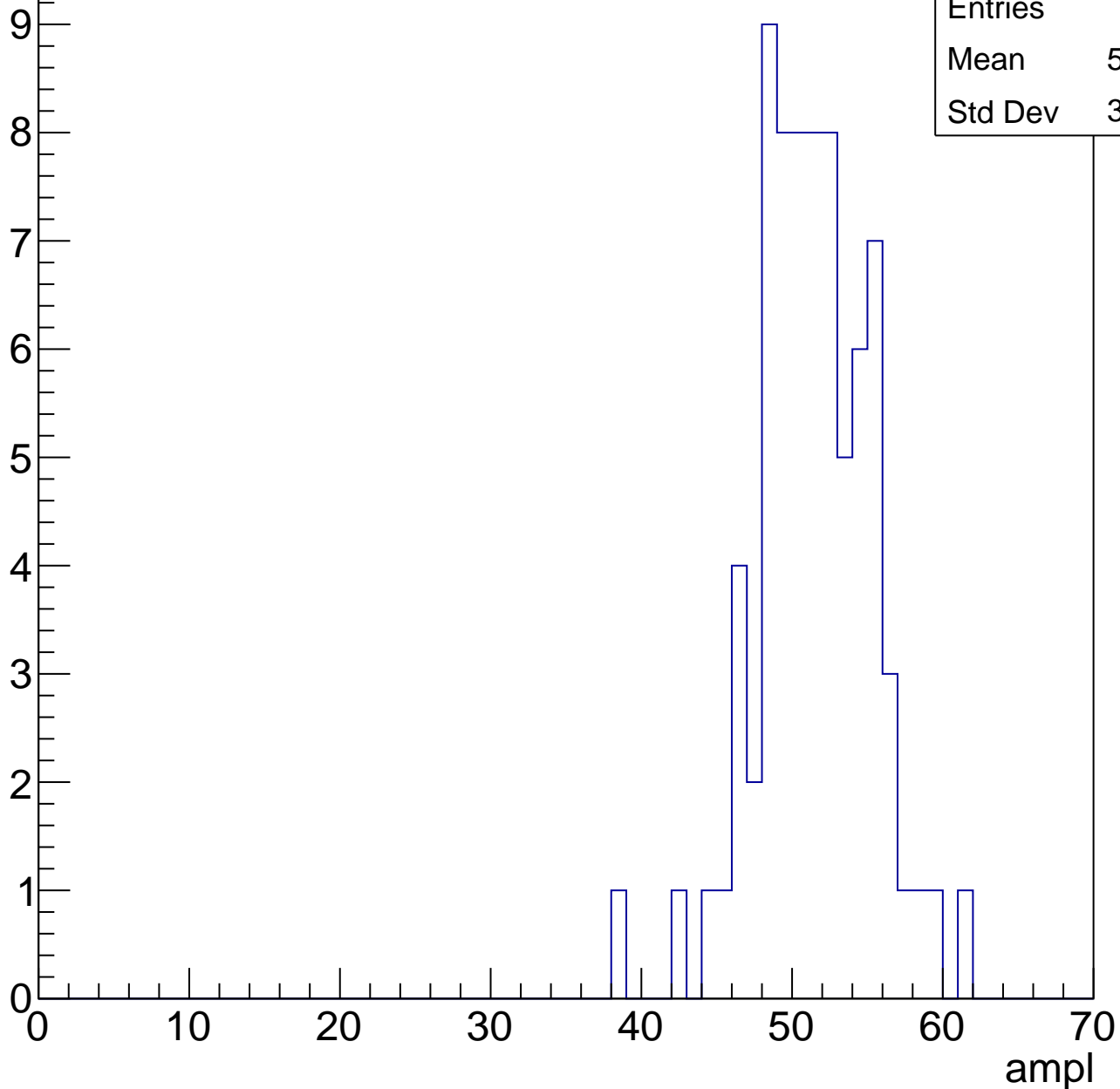


# B1L102S, U12-ch111, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	76
Mean	50.95
Std Dev	3.814

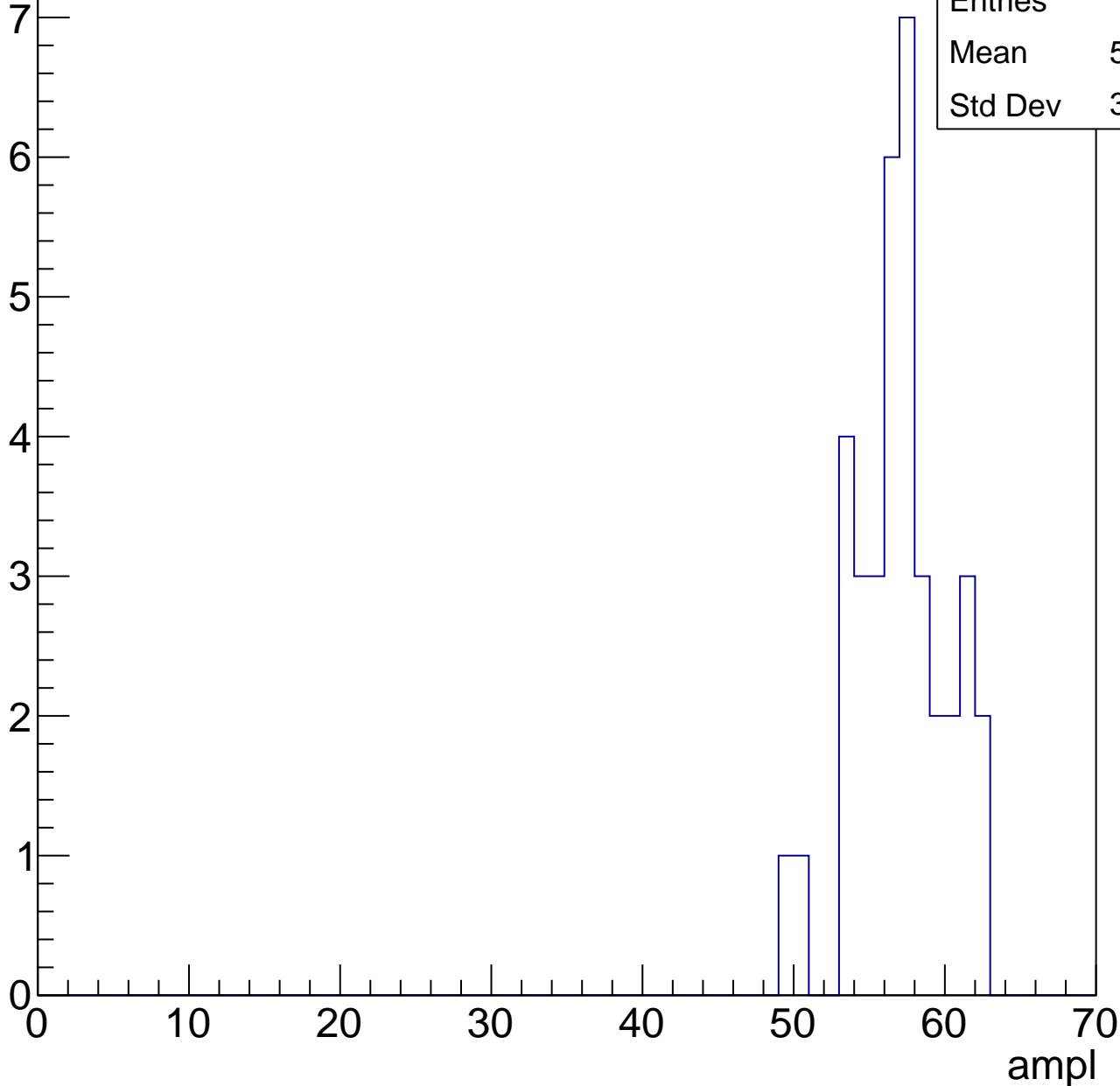


# B1L102S, U12-ch111, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	37
Mean	56.54
Std Dev	3.037

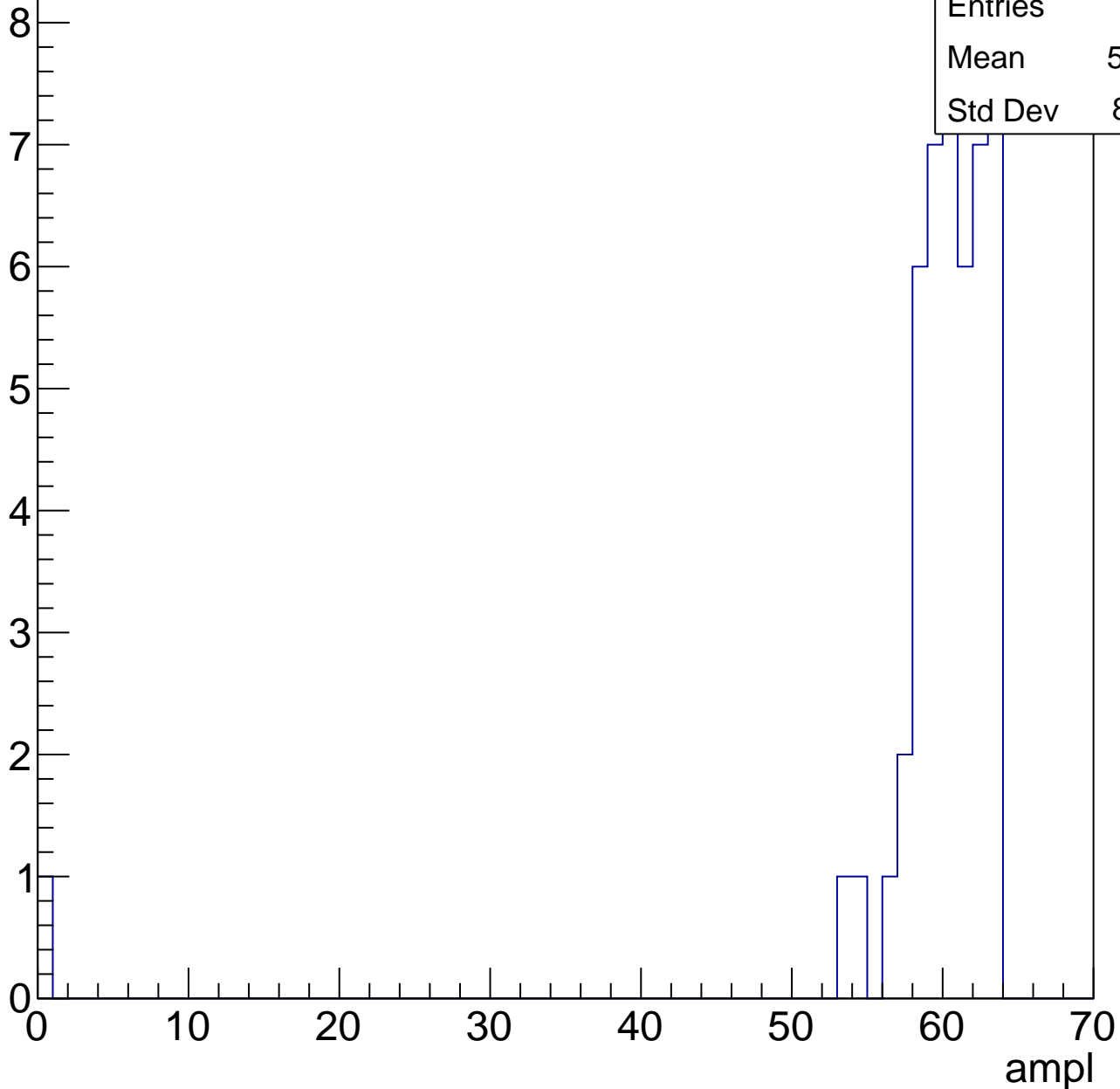


# B1L102S, U12-ch111, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	48
Mean	58.79
Std Dev	8.881



# B1L102S, U12-ch111, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	3
Mean	62.67
Std Dev	0.4714

ampl

0 10 20 30 40 50 60 70



# B1L102S, U12-ch111, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U12-ch112, adc0

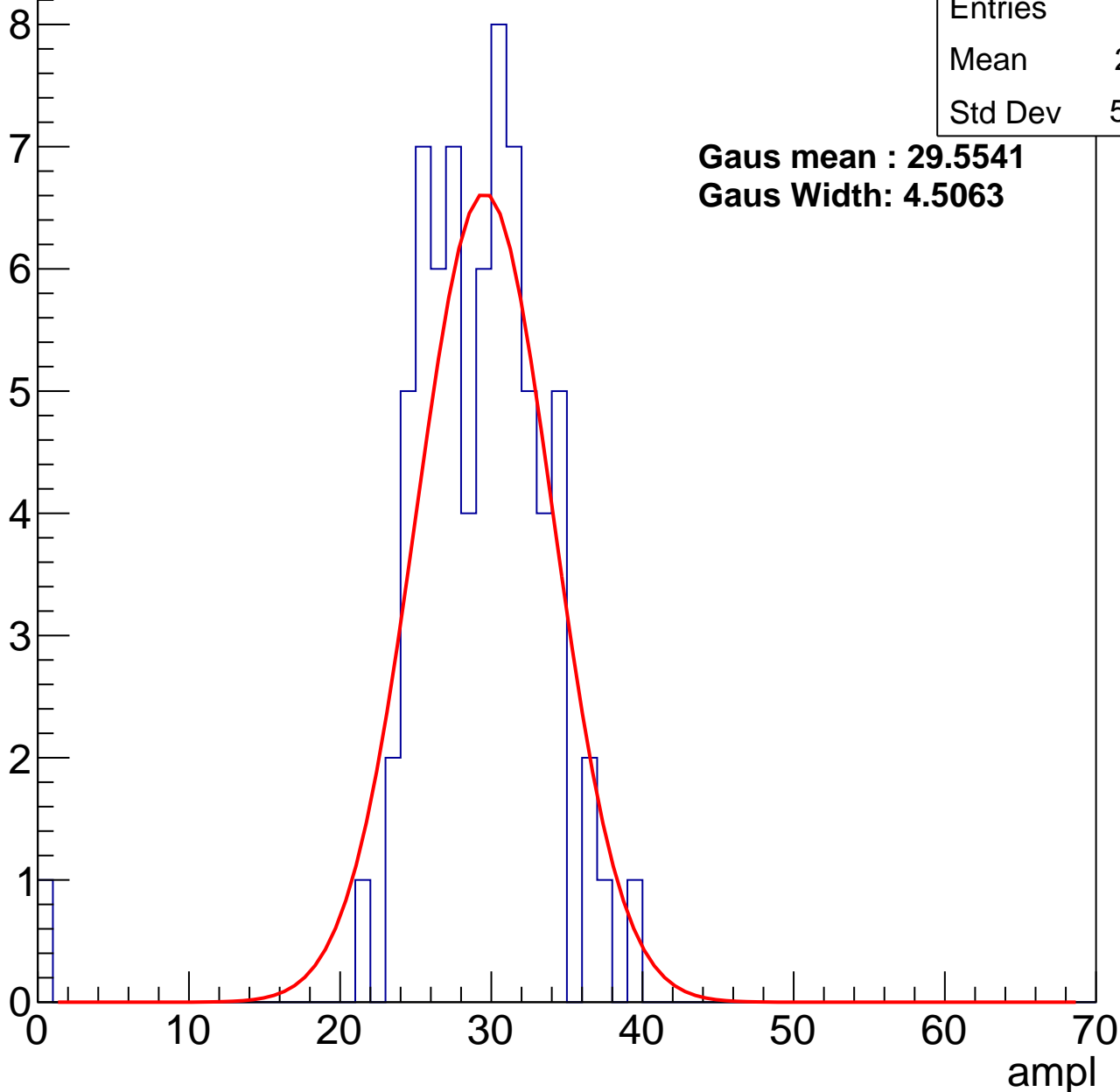
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	72
Mean	28.61
Std Dev	5.029

**Gaus mean : 29.5541**

**Gaus Width: 4.5063**



# B1L102S, U12-ch112, adc1

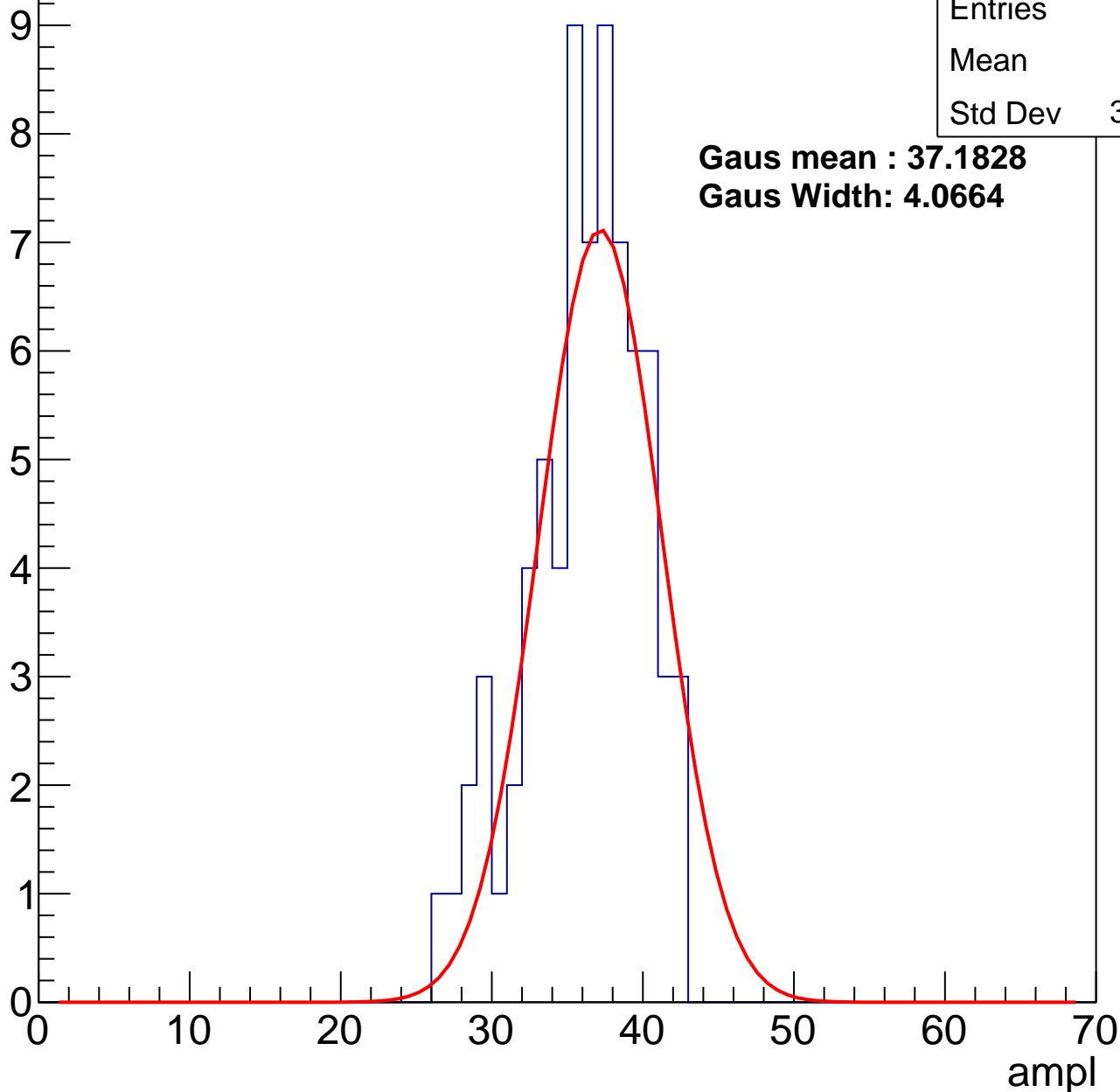
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	73
Mean	35.7
Std Dev	3.773

**Gaus mean : 37.1828**

**Gaus Width: 4.0664**



# B1L102S, U12-ch112, adc2

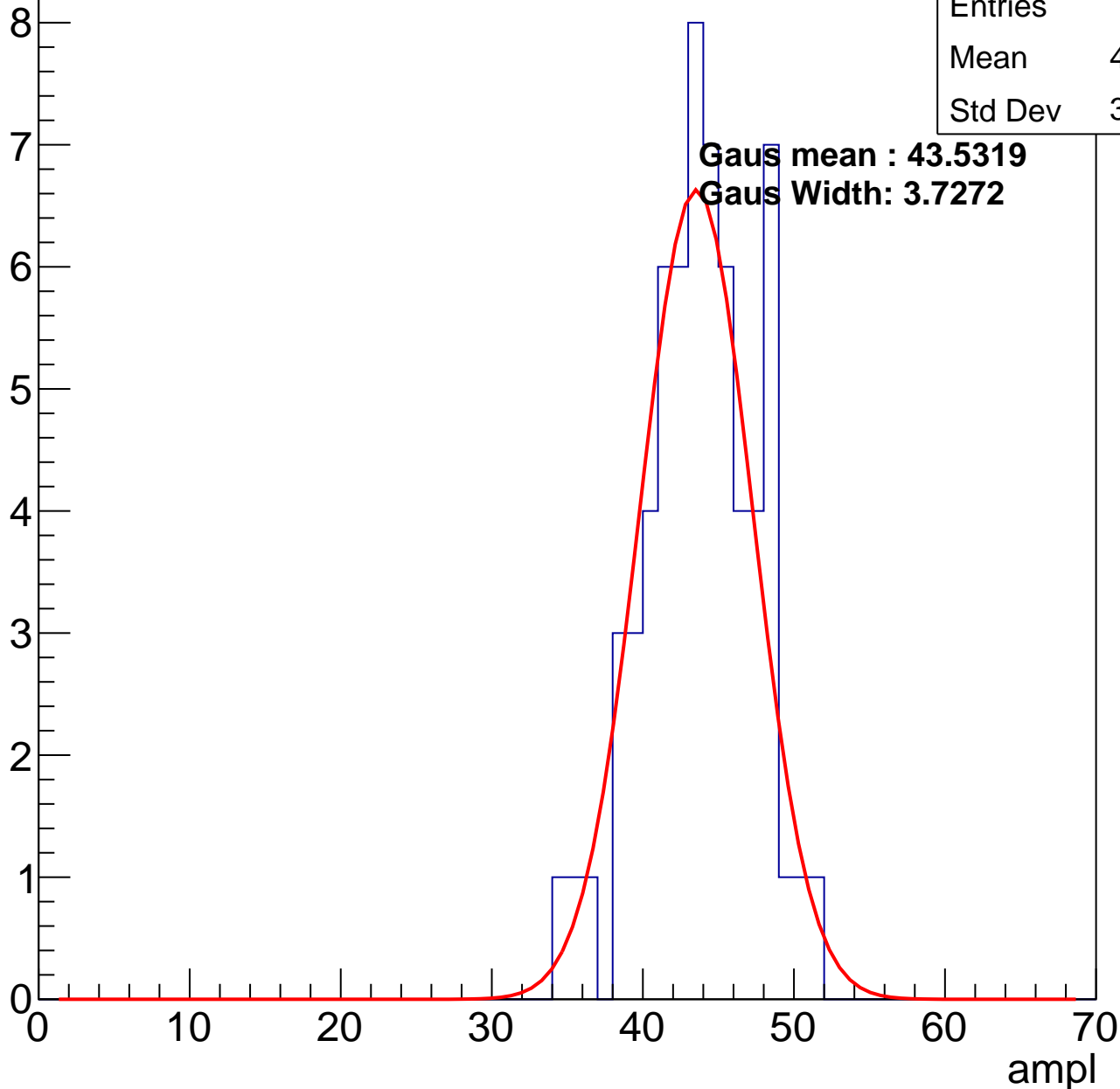
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	43.34
Std Dev	3.602

Gaus mean : 43.5319

Gaus Width: 3.7272

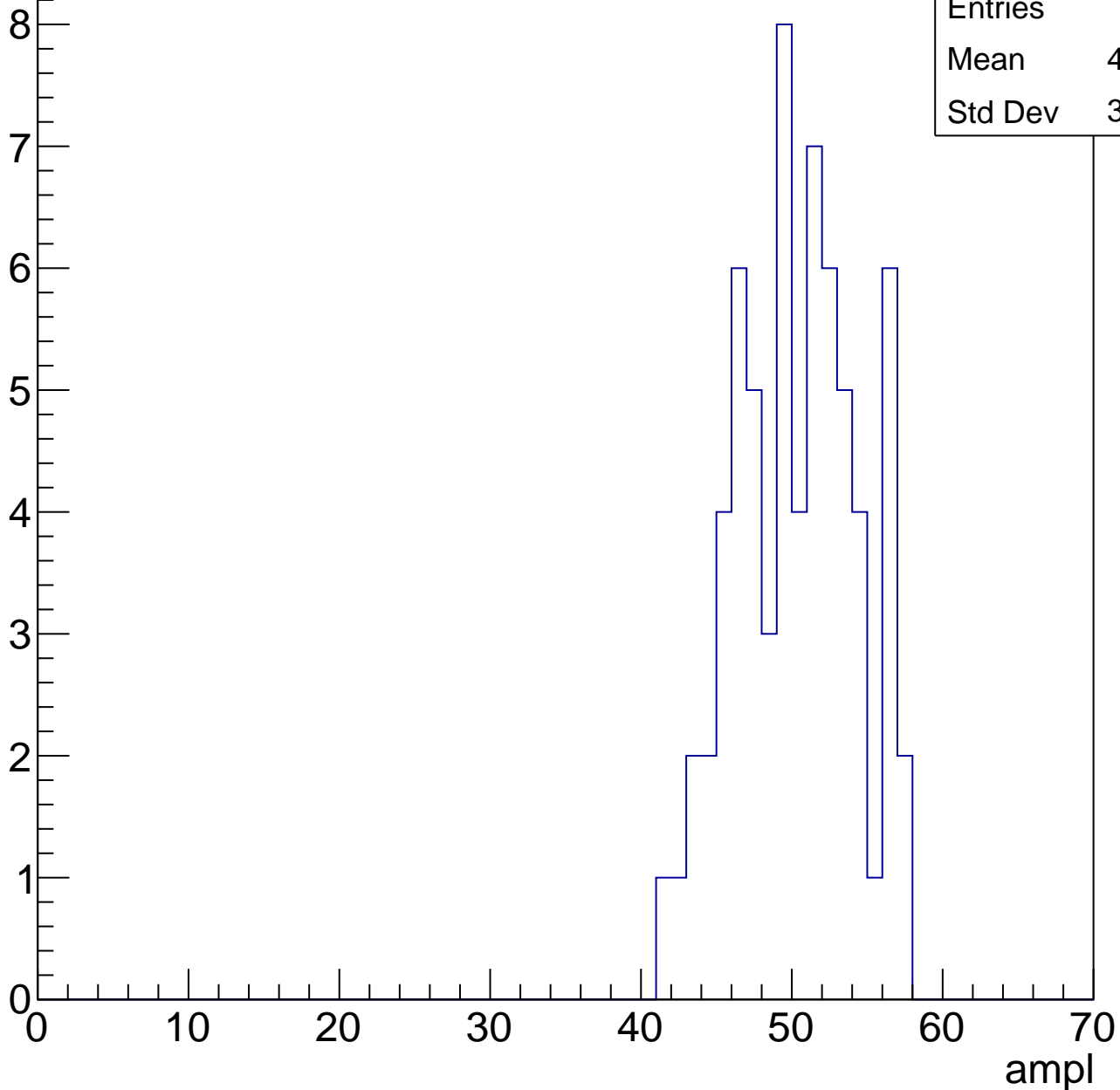


# B1L102S, U12-ch112, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	67
Mean	49.84
Std Dev	3.965



# B1L102S, U12-ch112, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

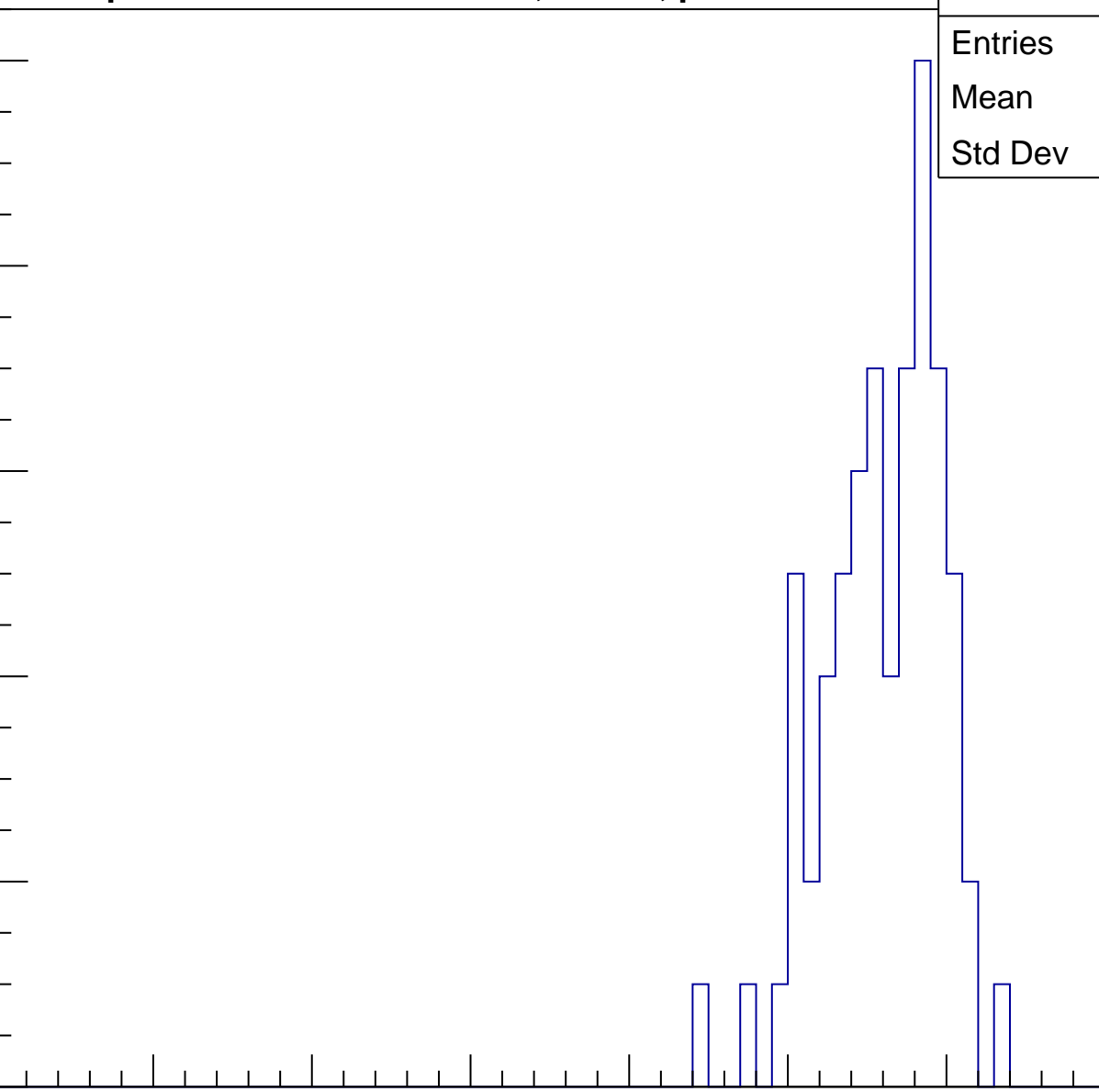
Entries	68
Mean	55.51
Std Dev	3.672

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B1L102S, U12-ch112, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	36
Mean	59.22
Std Dev	10.21

Entry

10

8

6

4

2

0

0

10

20

30

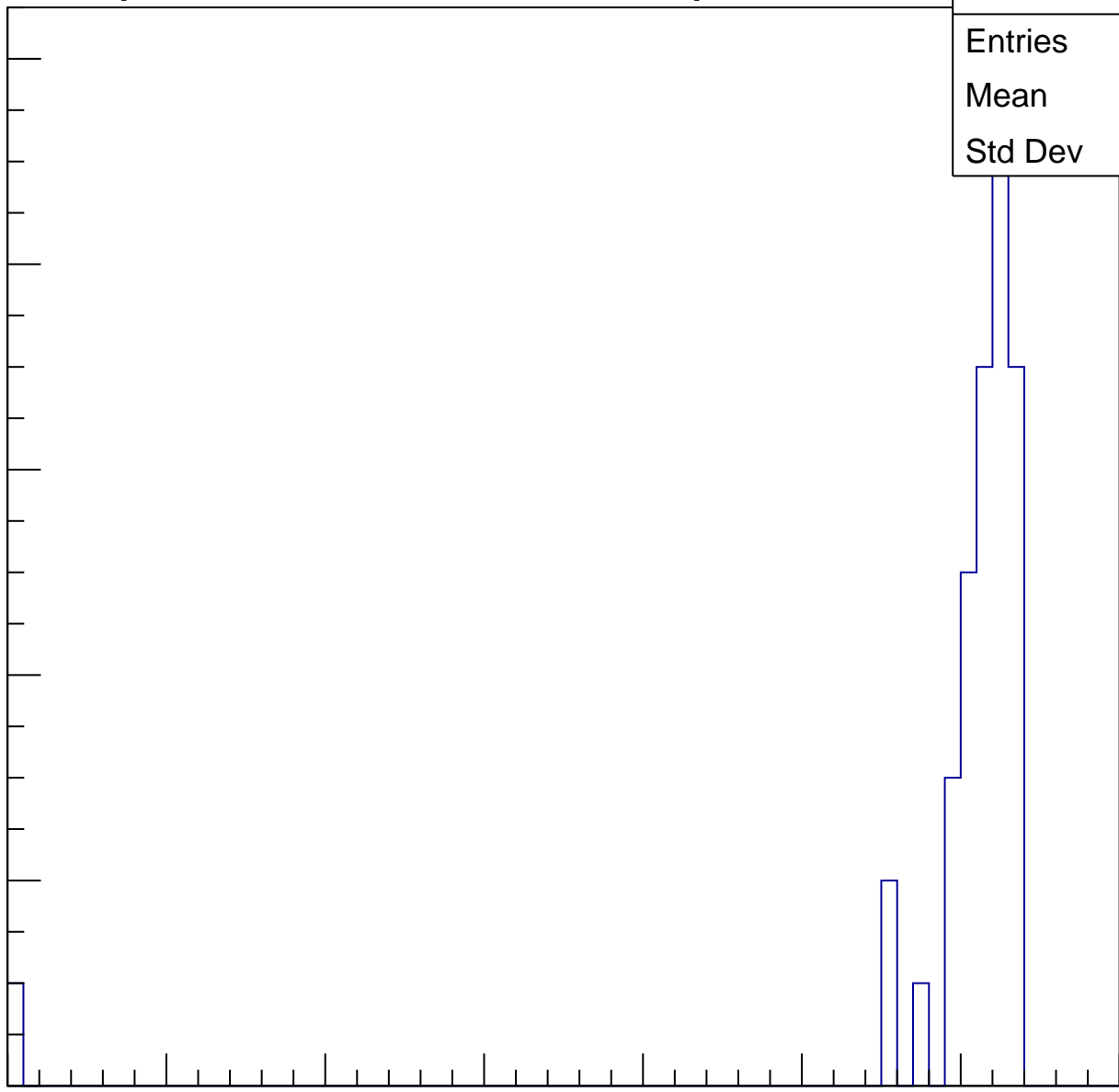
40

50

60

70

ampl



# B1L102S, U12-ch112, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	3
Mean	62.33
Std Dev	0.9428

0 10 20 30 40 50 60 70

ampl





# B1L102S, U12-ch112, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U12-ch113, adc0

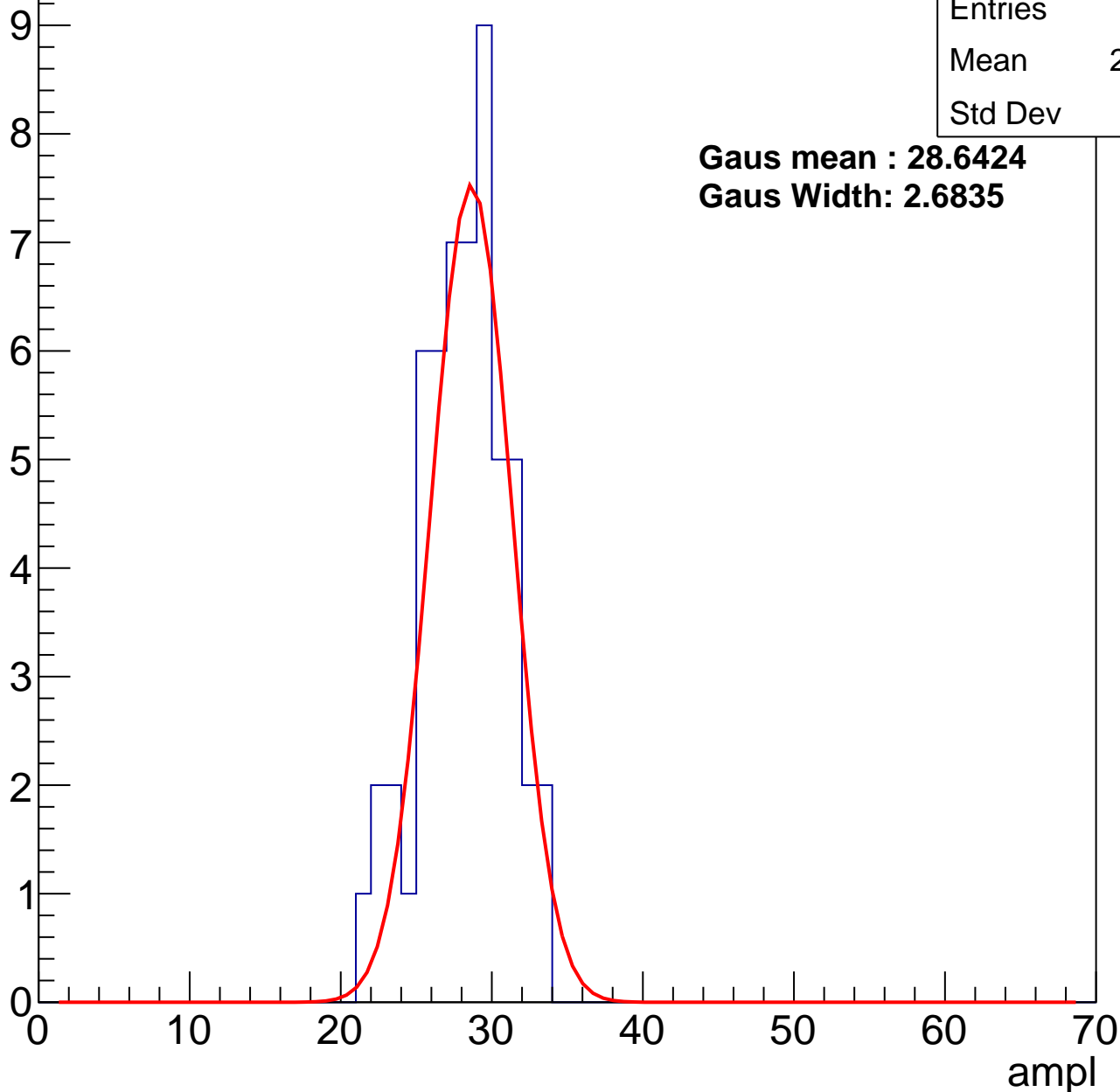
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	55
Mean	27.67
Std Dev	2.77

**Gaus mean : 28.6424**

**Gaus Width: 2.6835**



# B1L102S, U12-ch113, adc1

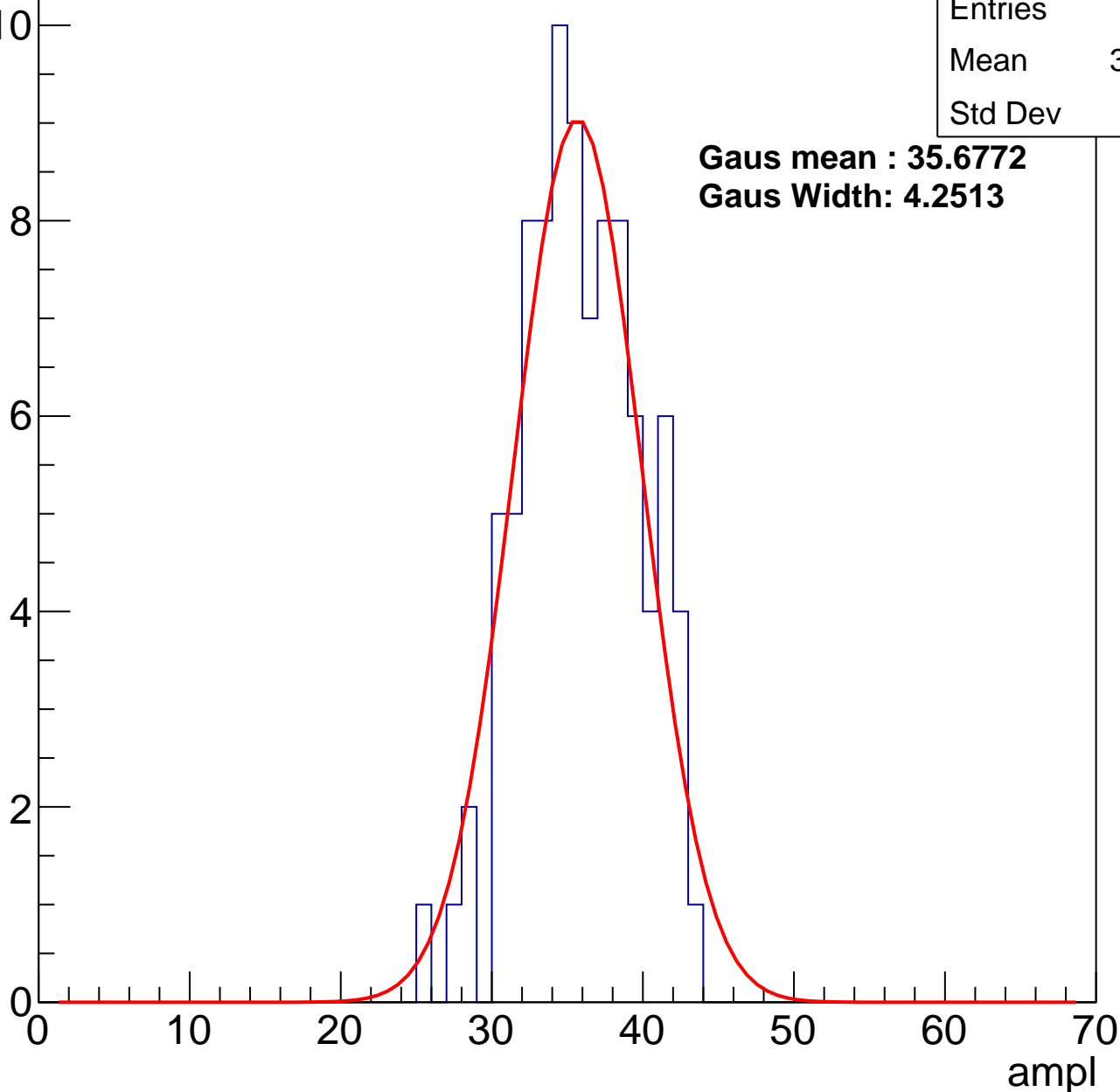
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	93
Mean	35.39
Std Dev	3.81

**Gaus mean : 35.6772**

**Gaus Width: 4.2513**



# B1L102S, U12-ch113, adc2

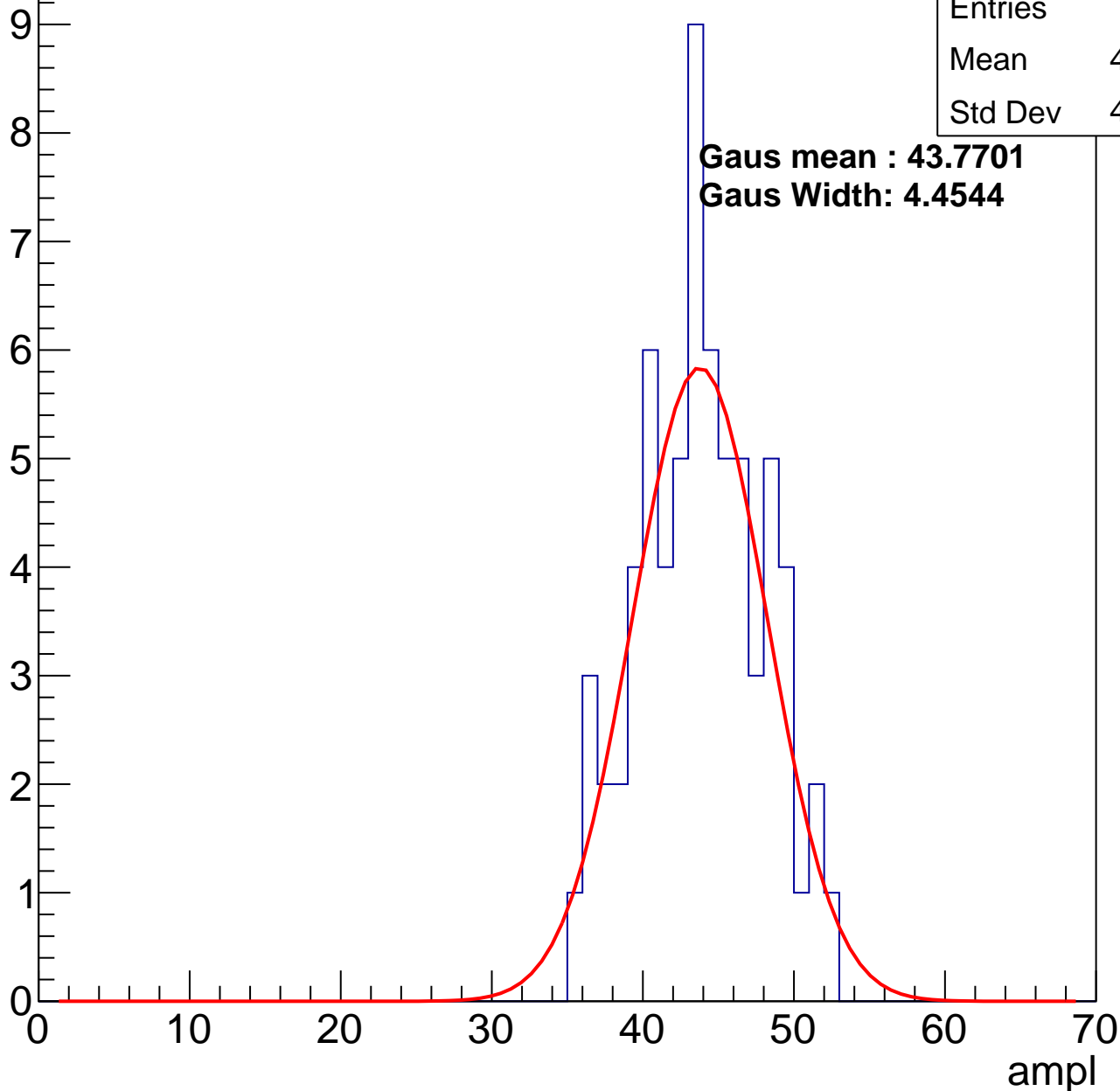
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	43.38
Std Dev	4.037

**Gaus mean : 43.7701**

**Gaus Width: 4.4544**

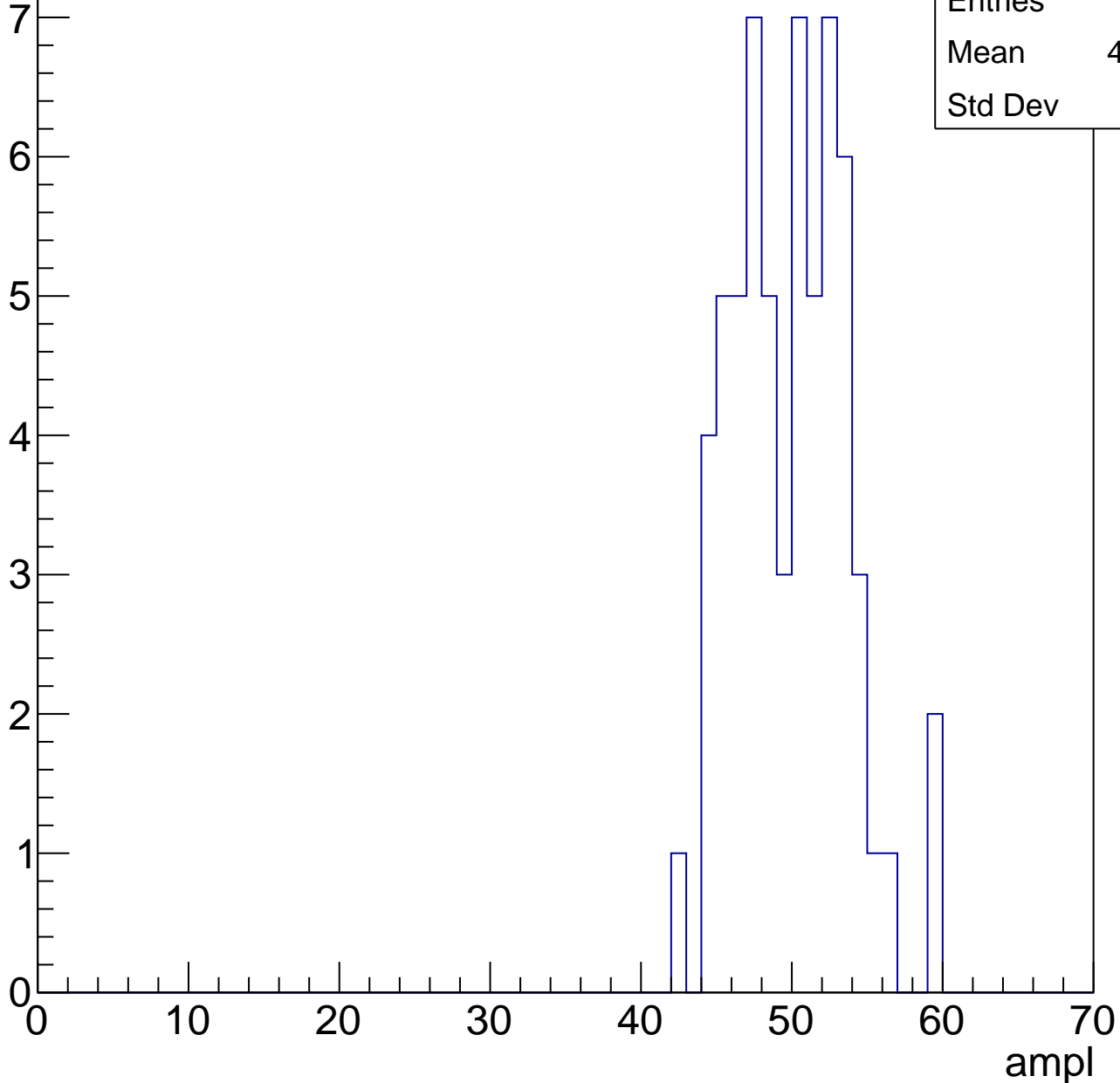


# B1L102S, U12-ch113, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	62
Mean	49.47
Std Dev	3.68

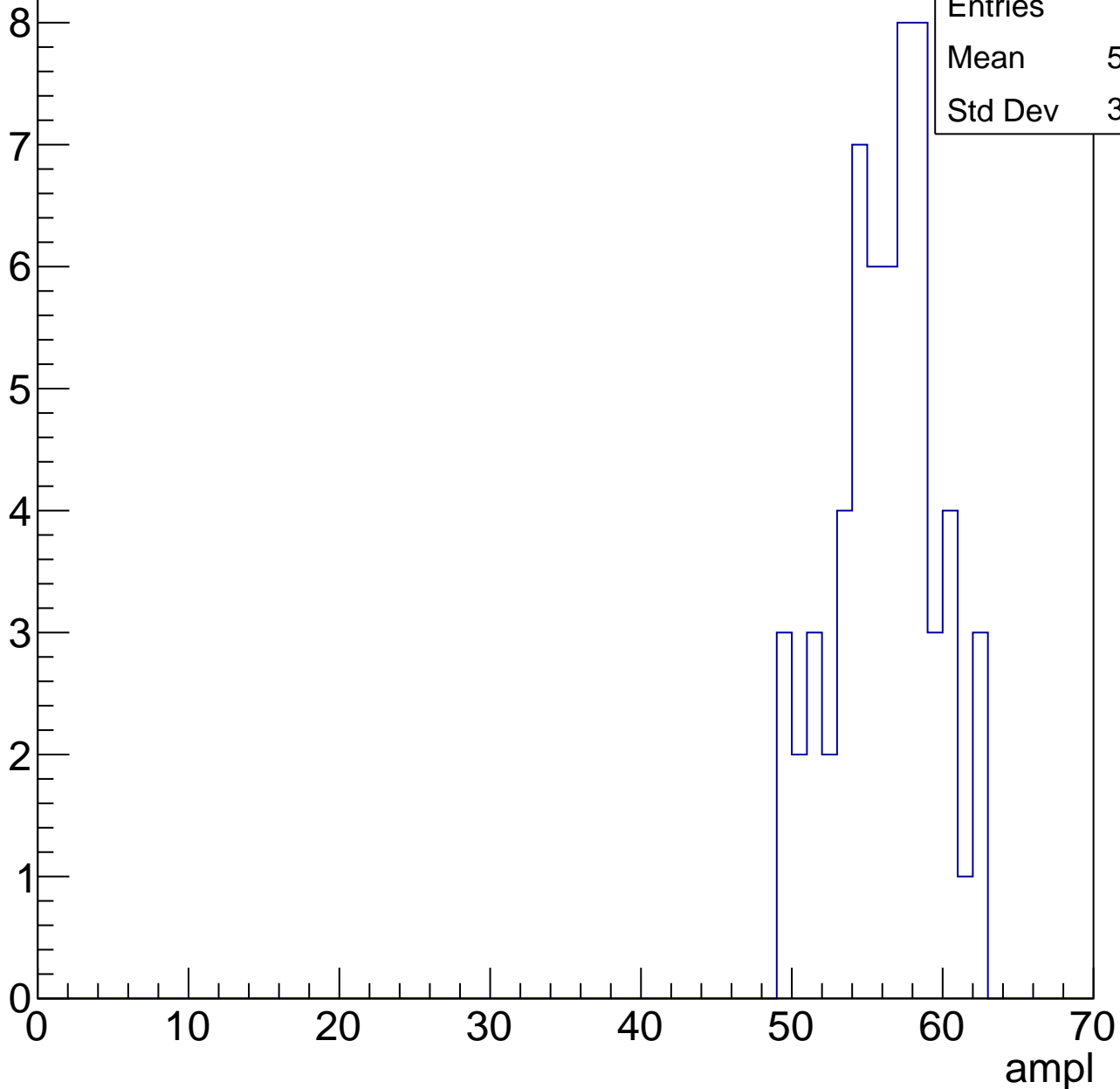


# B1L102S, U12-ch113, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	60
Mean	55.73
Std Dev	3.306

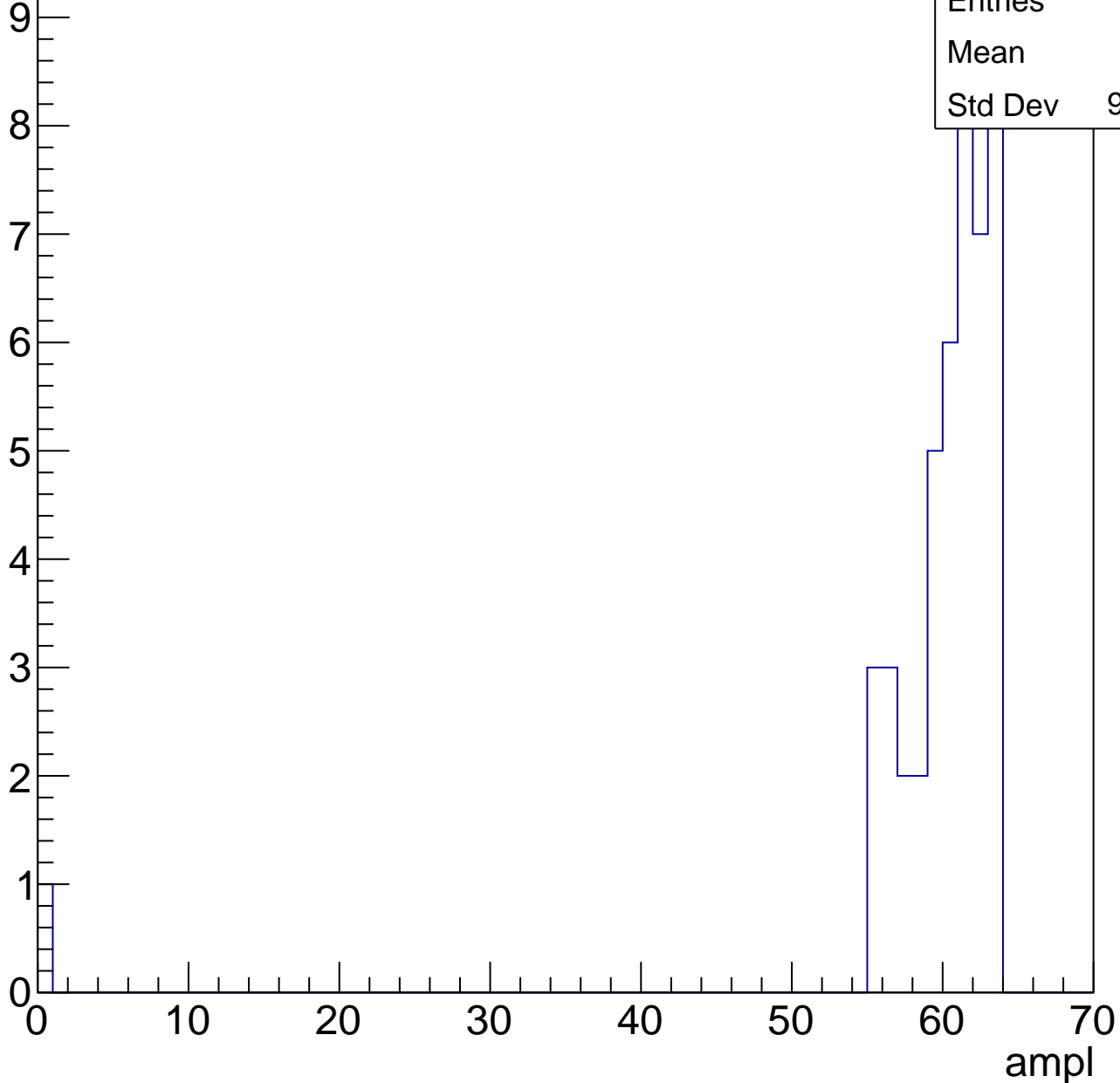


# B1L102S, U12-ch113, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

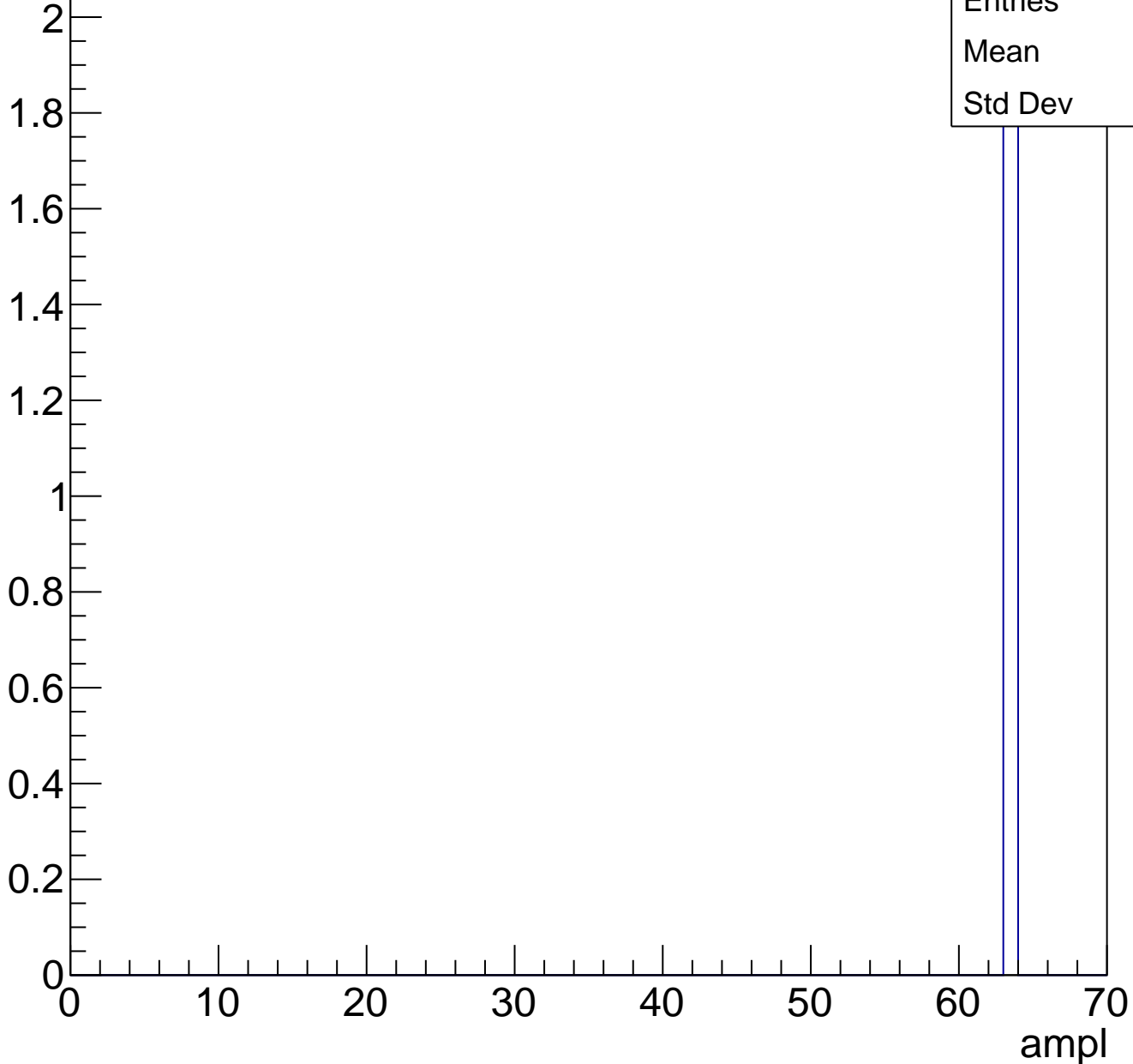
Entries	46
Mean	58.8
Std Dev	9.086



# B1L102S, U12-ch113, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U12-ch113, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U12-ch114, adc0

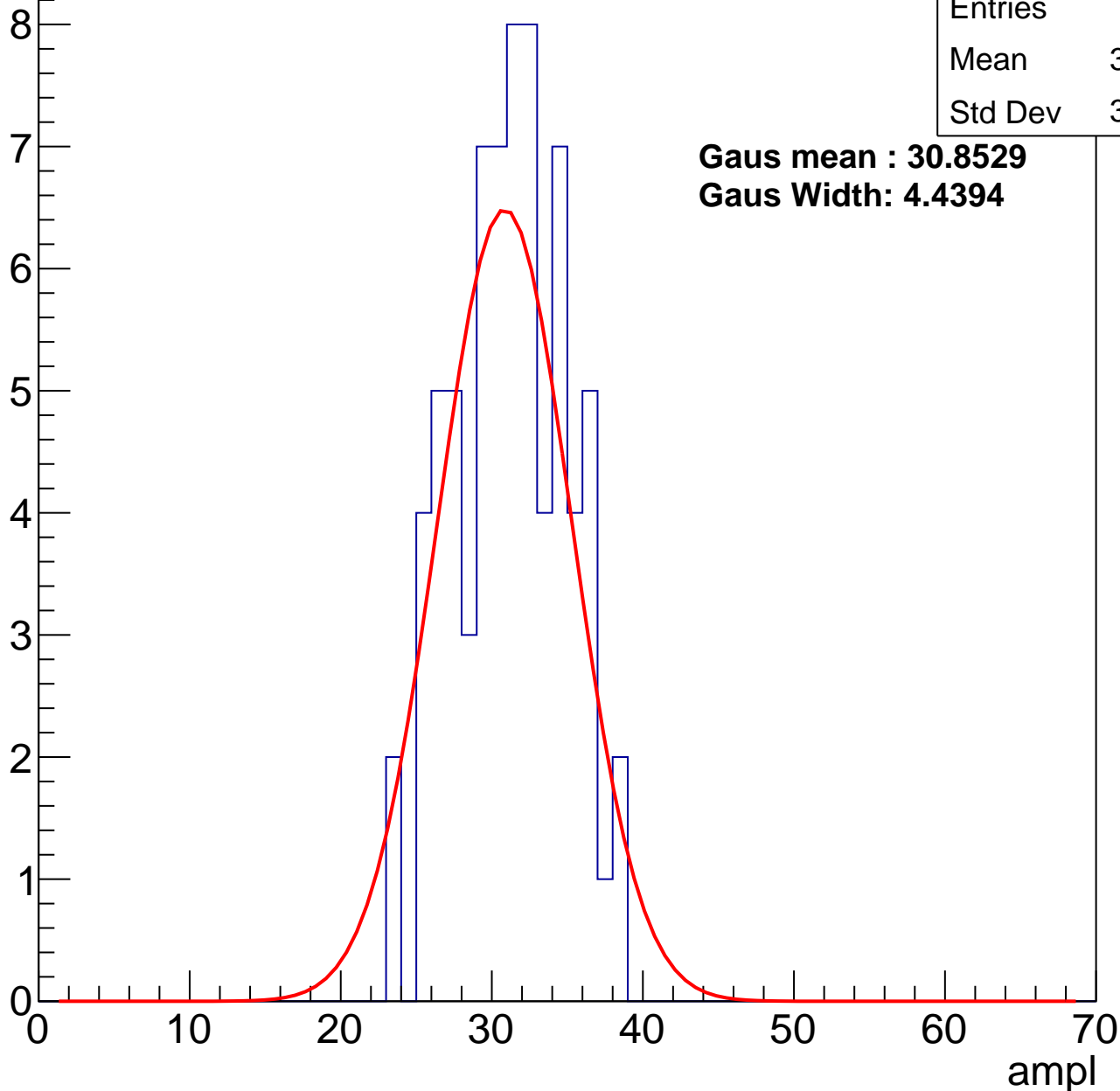
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	72
Mean	30.76
Std Dev	3.623

**Gaus mean : 30.8529**

**Gaus Width: 4.4394**



# B1L102S, U12-ch114, adc1

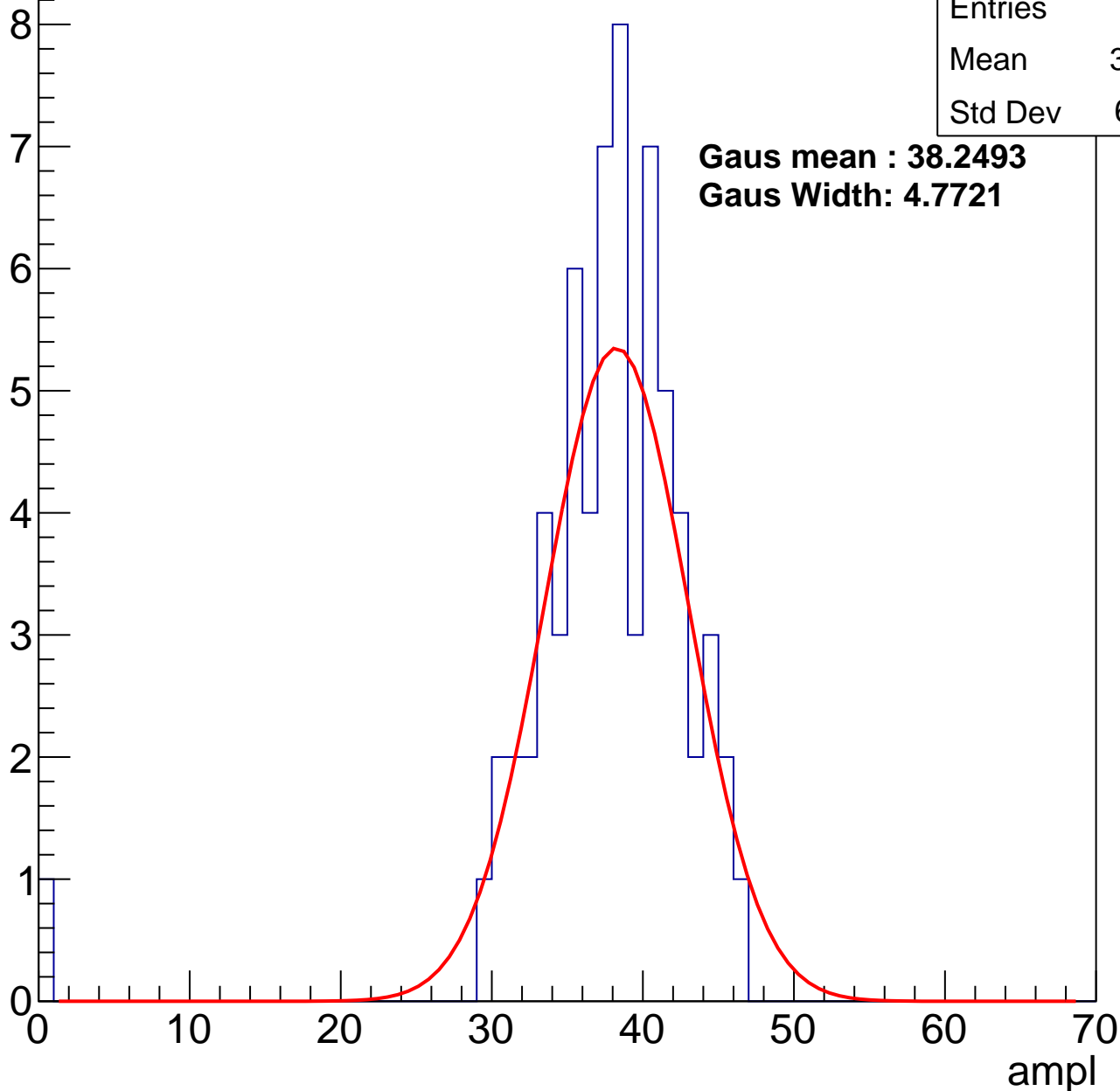
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	67
Mean	37.16
Std Dev	6.061

**Gaus mean : 38.2493**

**Gaus Width: 4.7721**



# B1L102S, U12-ch114, adc2

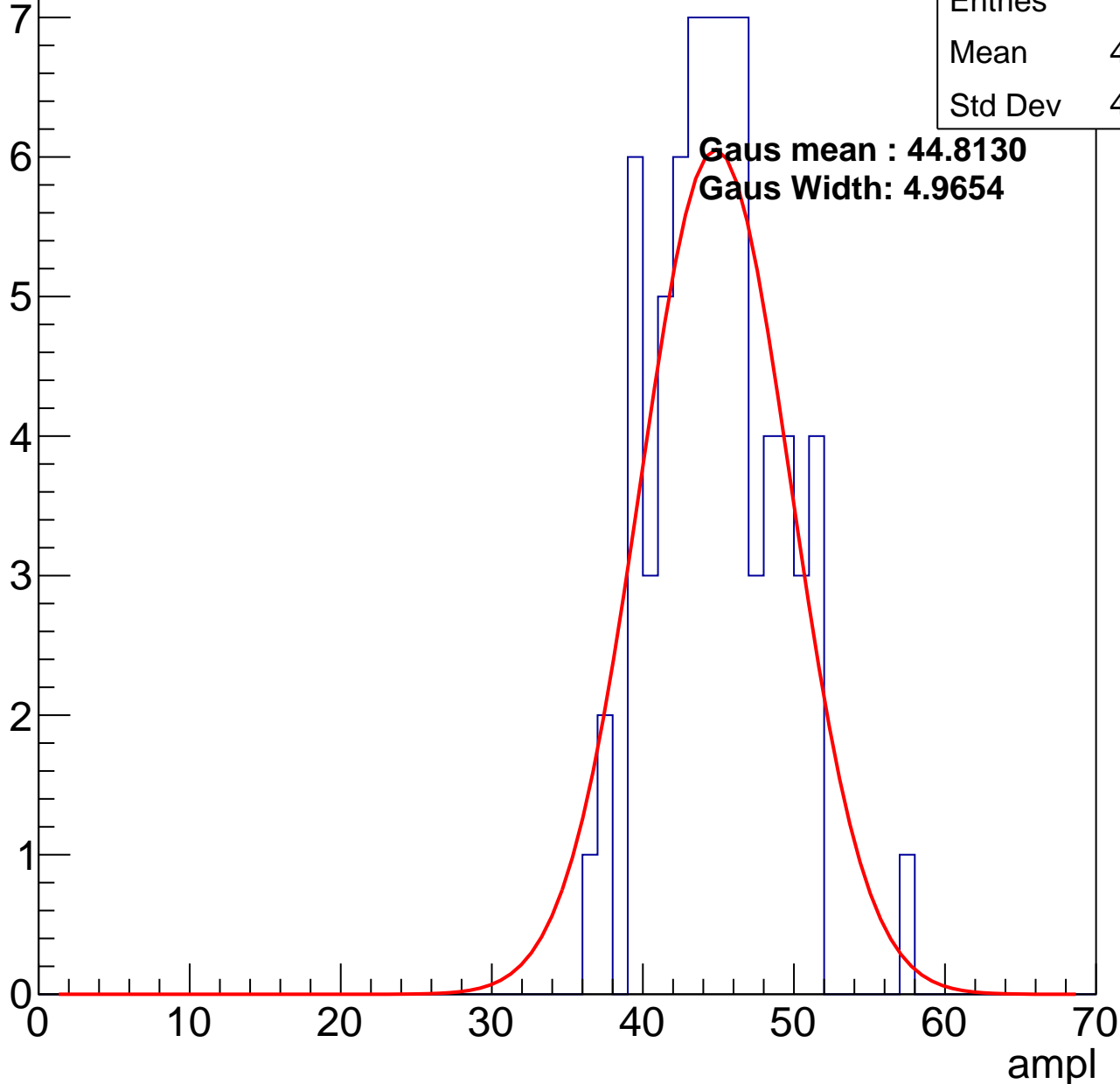
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	70
Mean	44.39
Std Dev	4.008

**Gaus mean : 44.8130**

**Gaus Width: 4.9654**

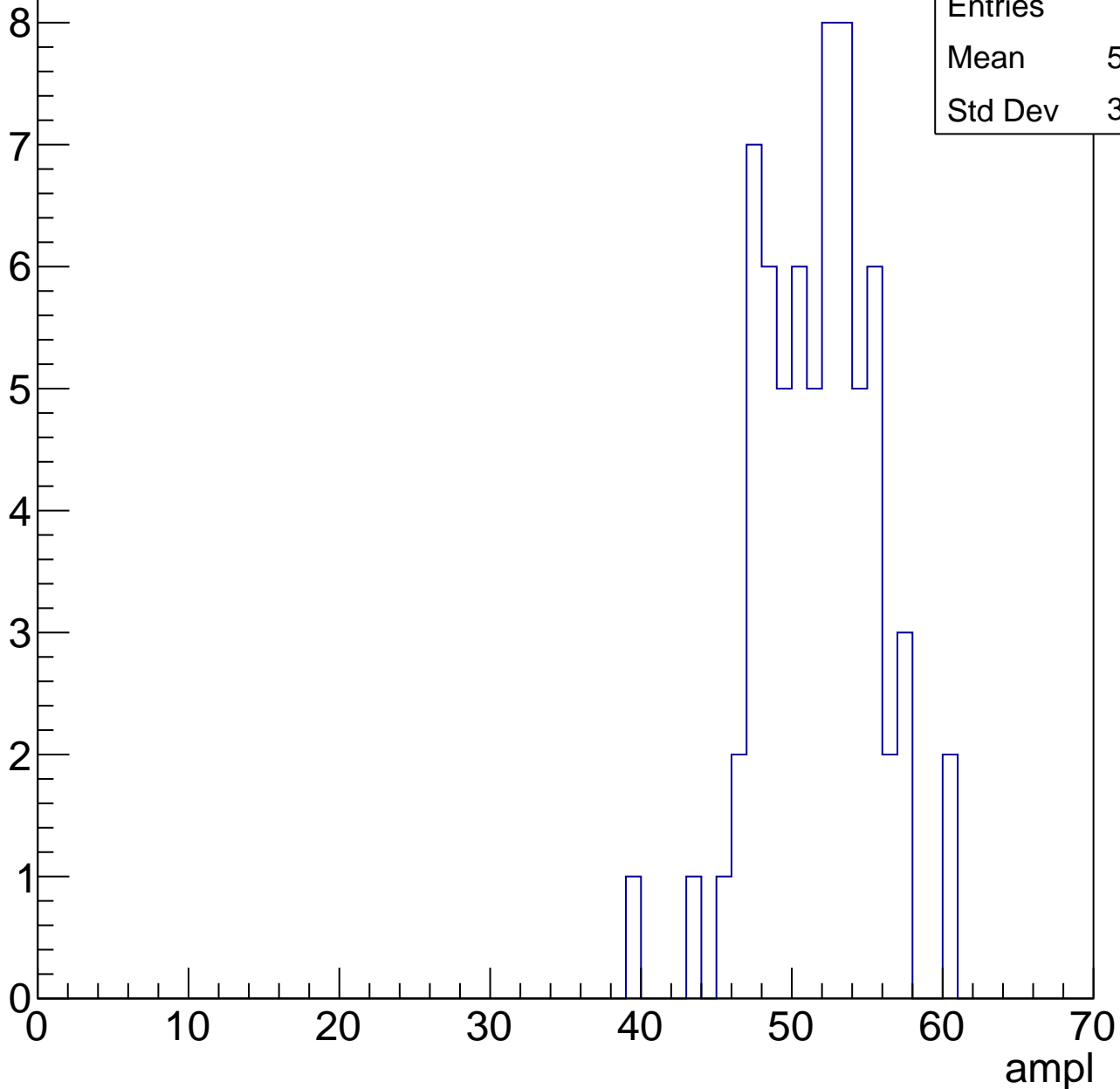


# B1L102S, U12-ch114, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	51.16
Std Dev	3.806

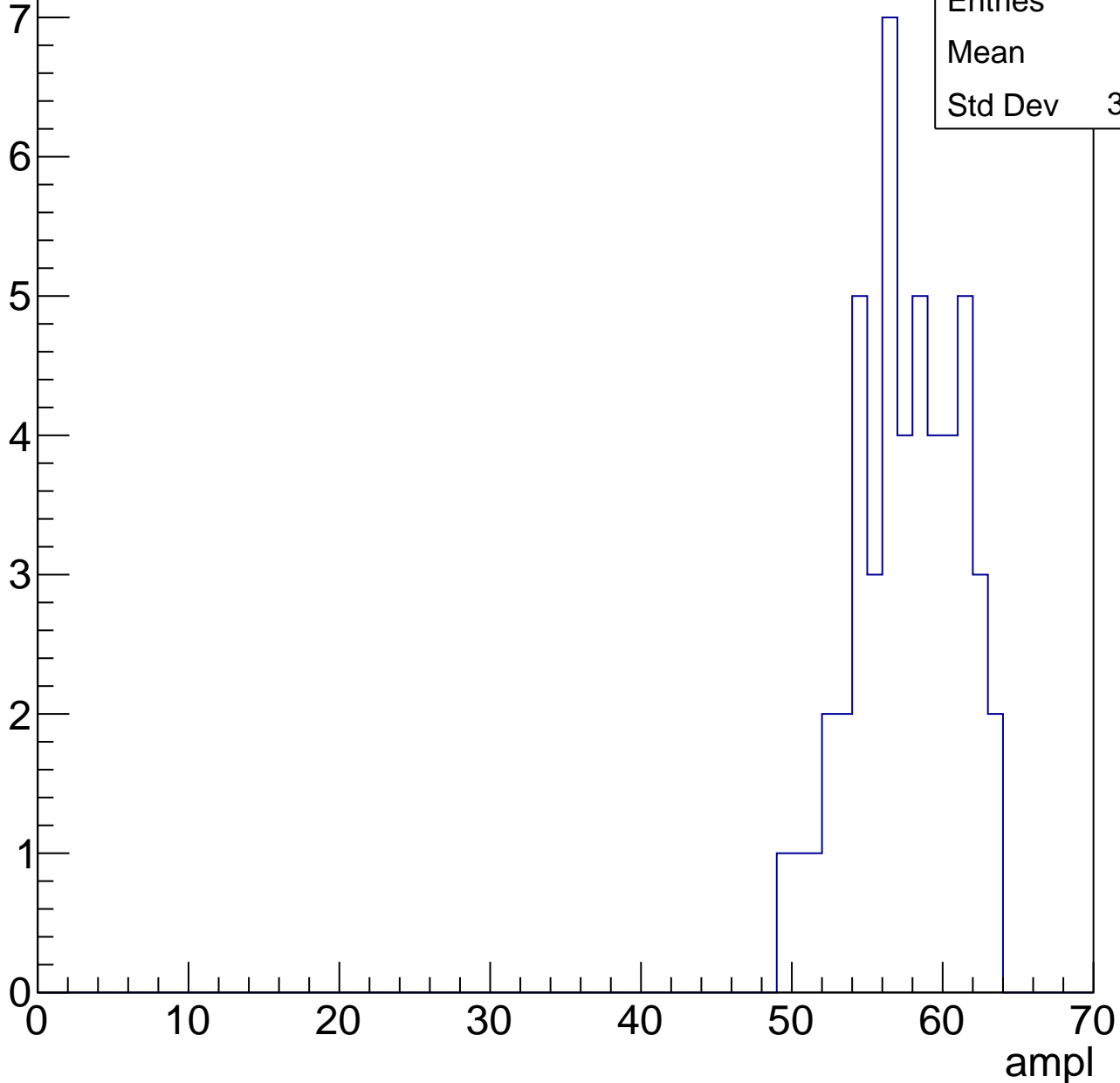


# B1L102S, U12-ch114, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	49
Mean	57.1
Std Dev	3.436

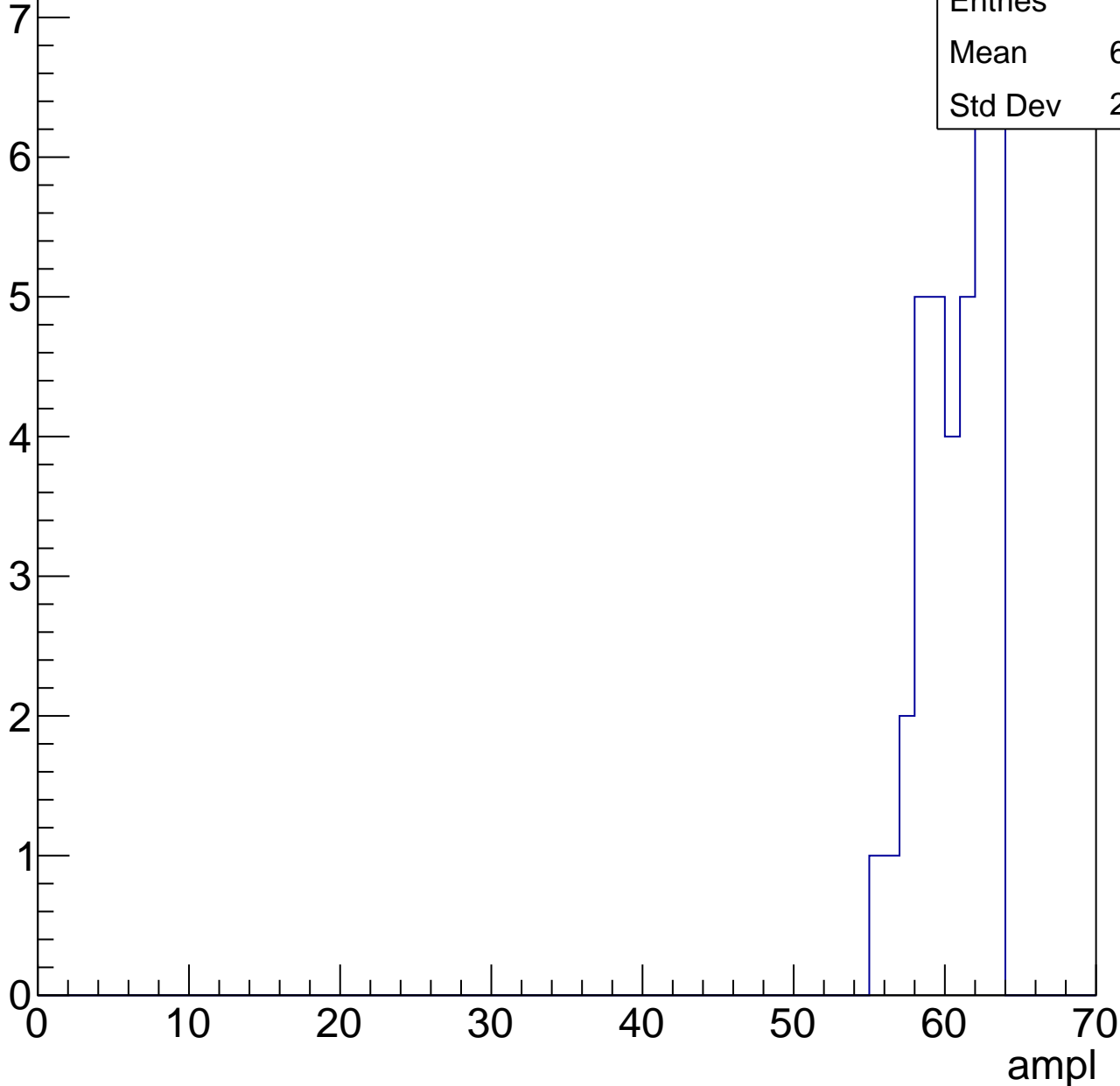


# B1L102S, U12-ch114, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

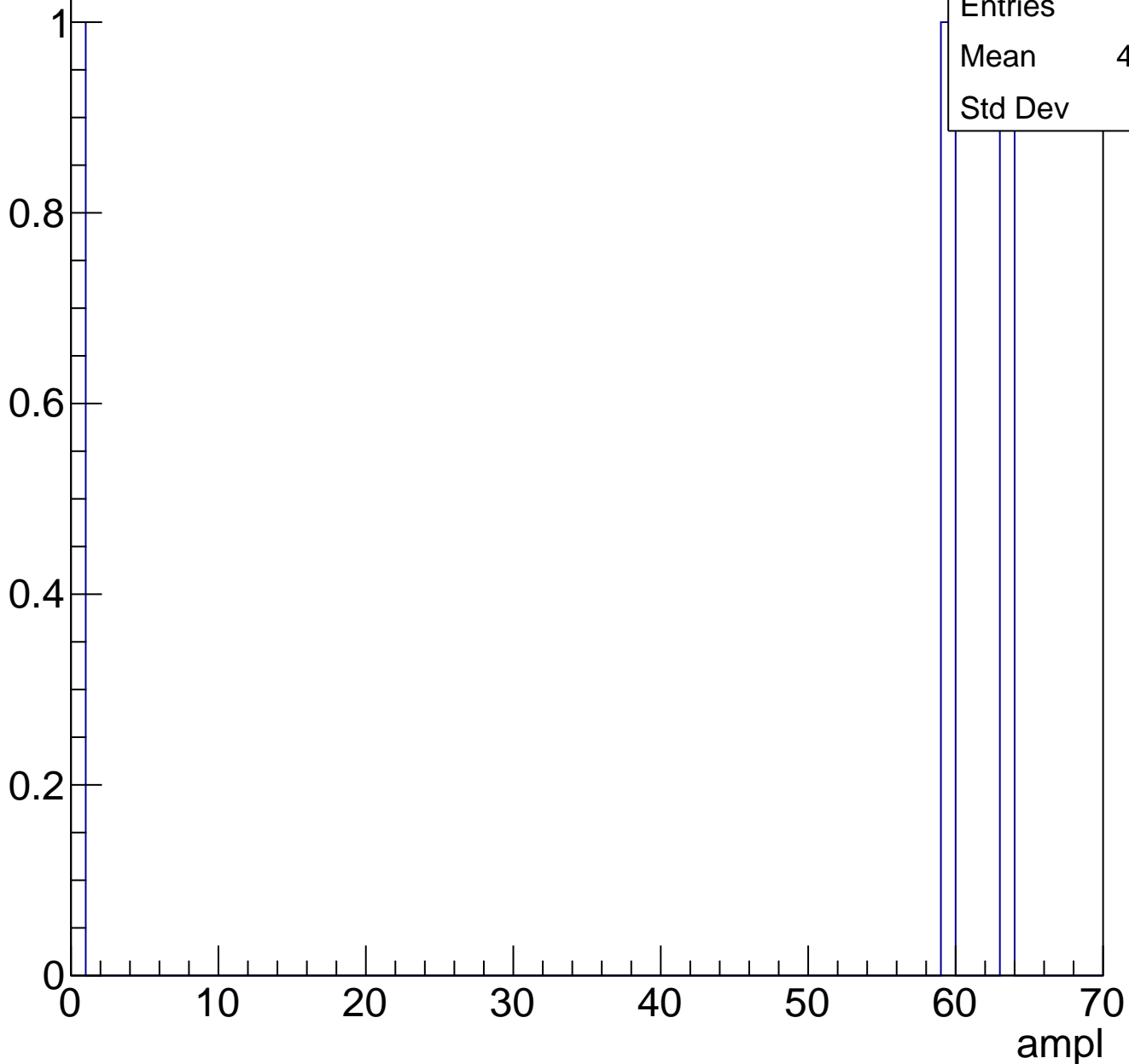
Entries	37
Mean	60.27
Std Dev	2.189



# B1L102S, U12-ch114, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U12-ch114, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U12-ch115, adc0

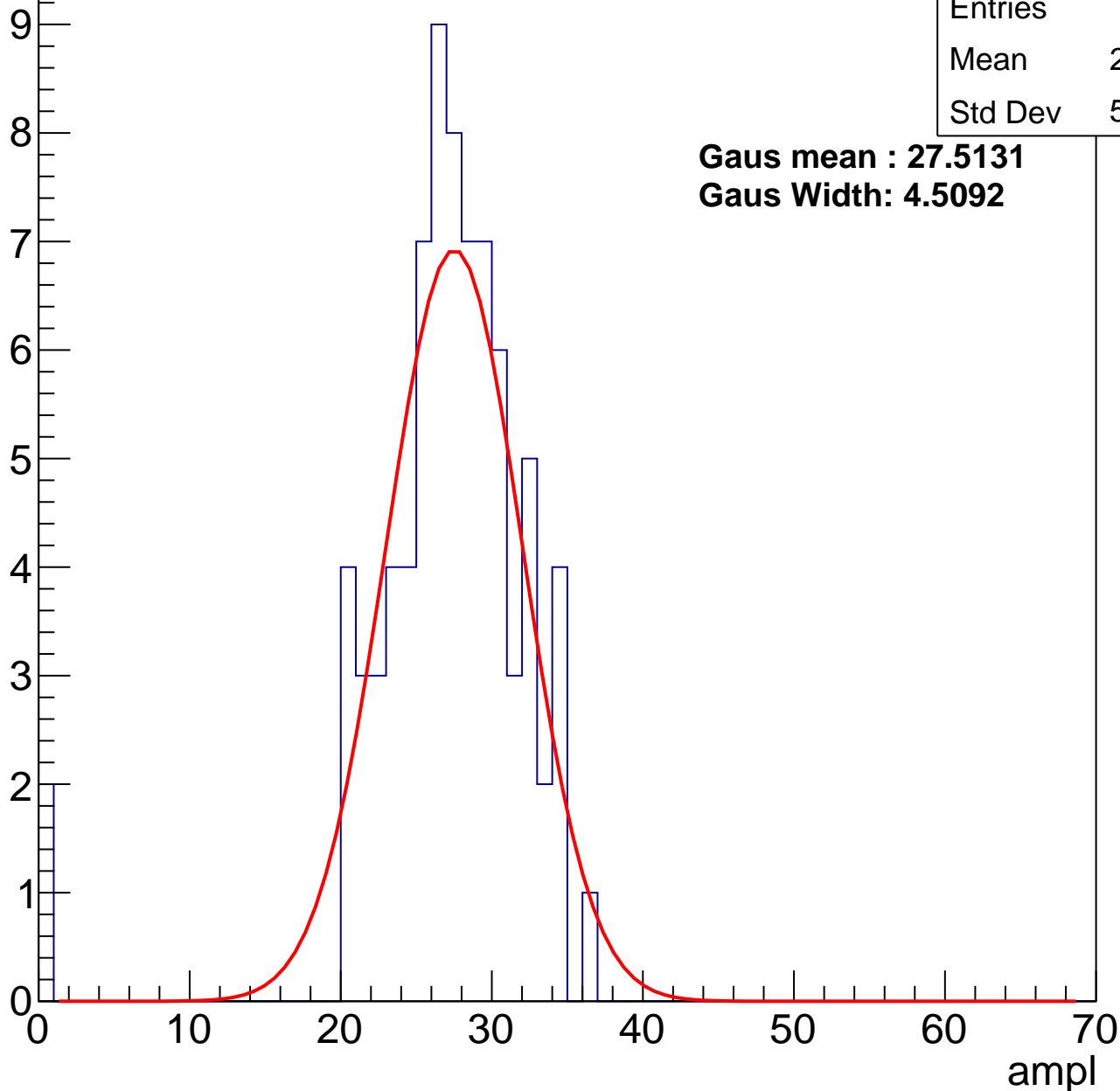
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	79
Mean	26.48
Std Dev	5.697

**Gaus mean : 27.5131**

**Gaus Width: 4.5092**



# B1L102S, U12-ch115, adc1

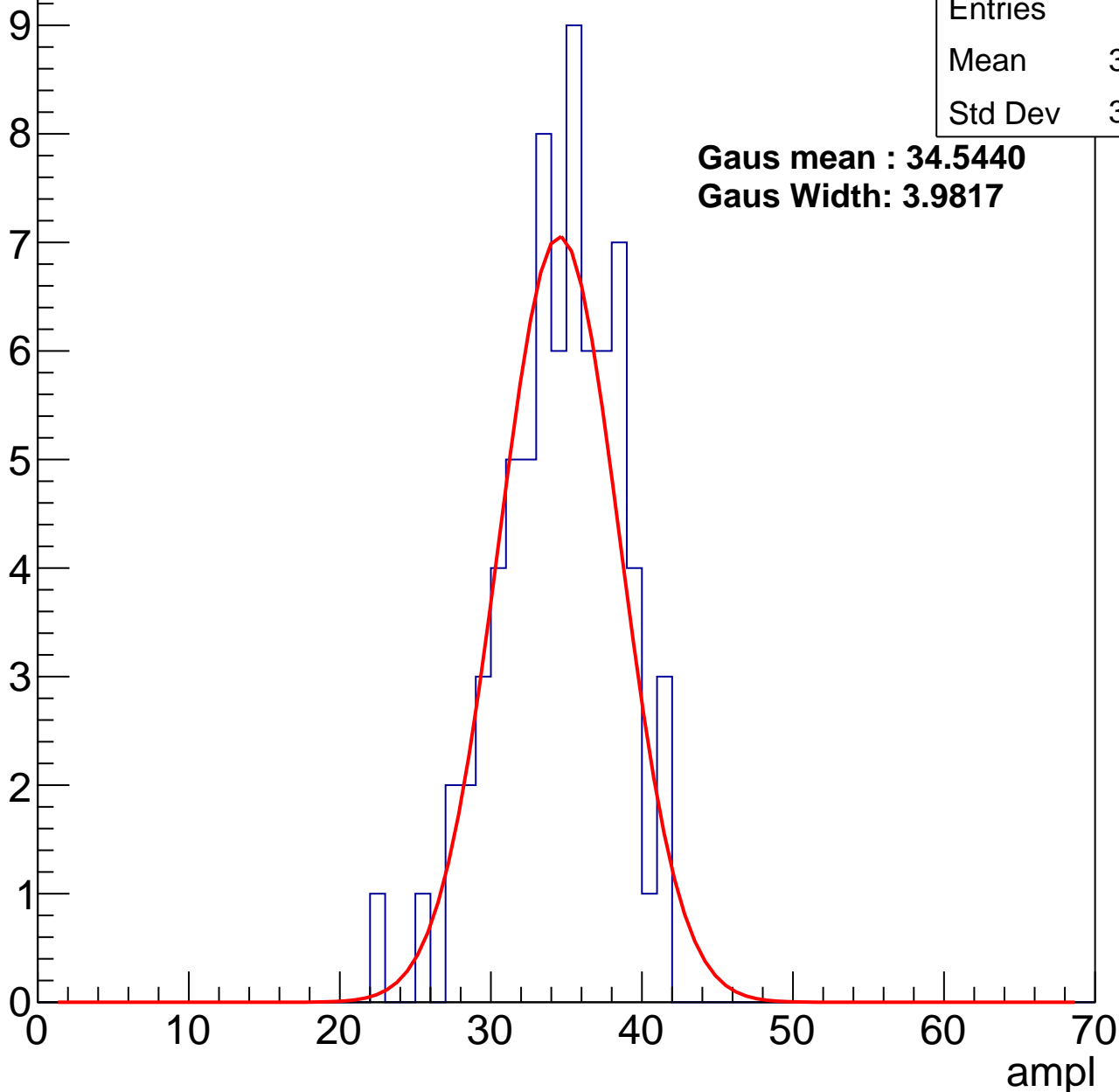
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	73
Mean	34.04
Std Dev	3.862

**Gaus mean : 34.5440**

**Gaus Width: 3.9817**



# B1L102S, U12-ch115, adc2

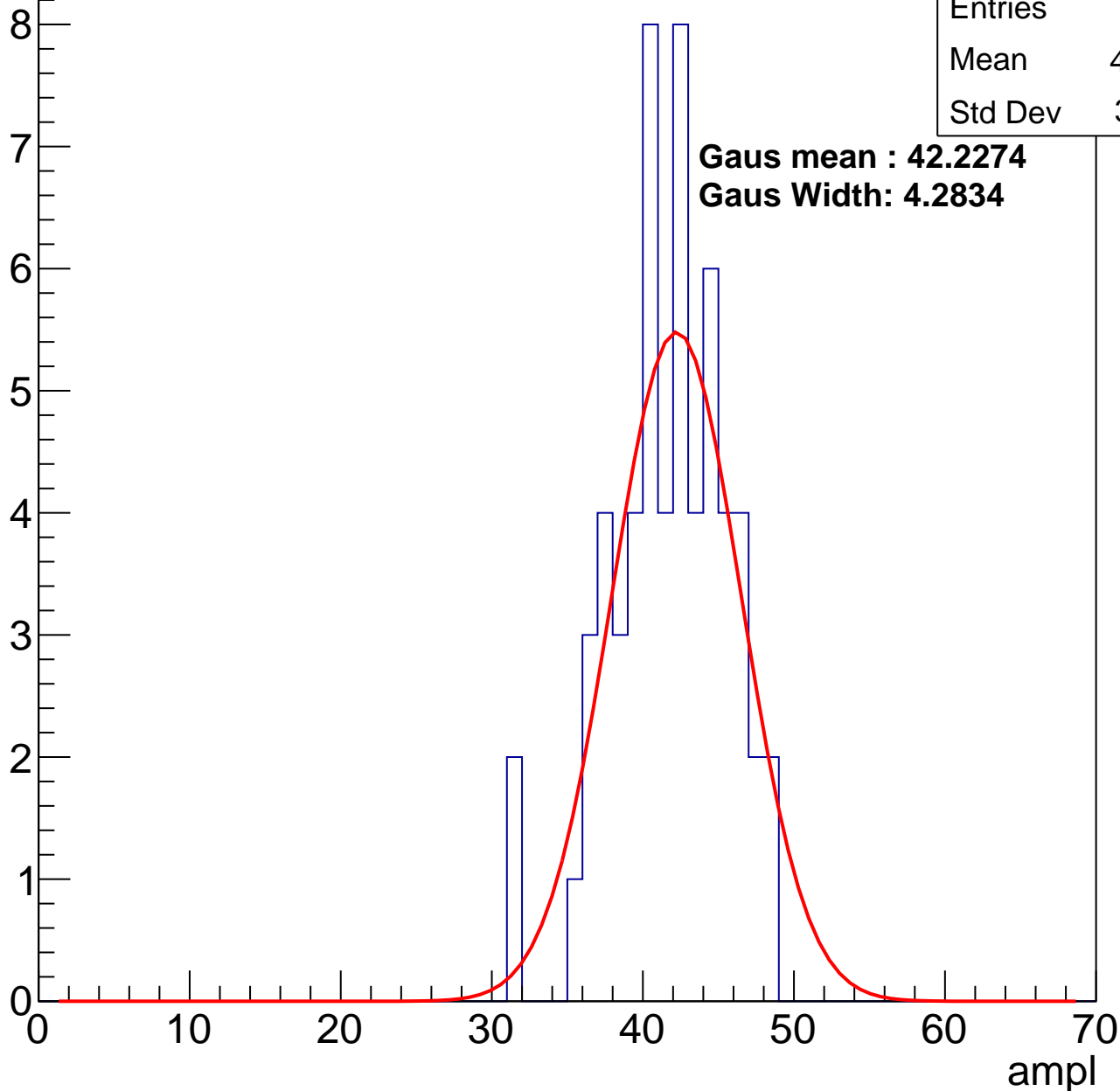
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	59
Mean	41.24
Std Dev	3.761

**Gaus mean : 42.2274**

**Gaus Width: 4.2834**

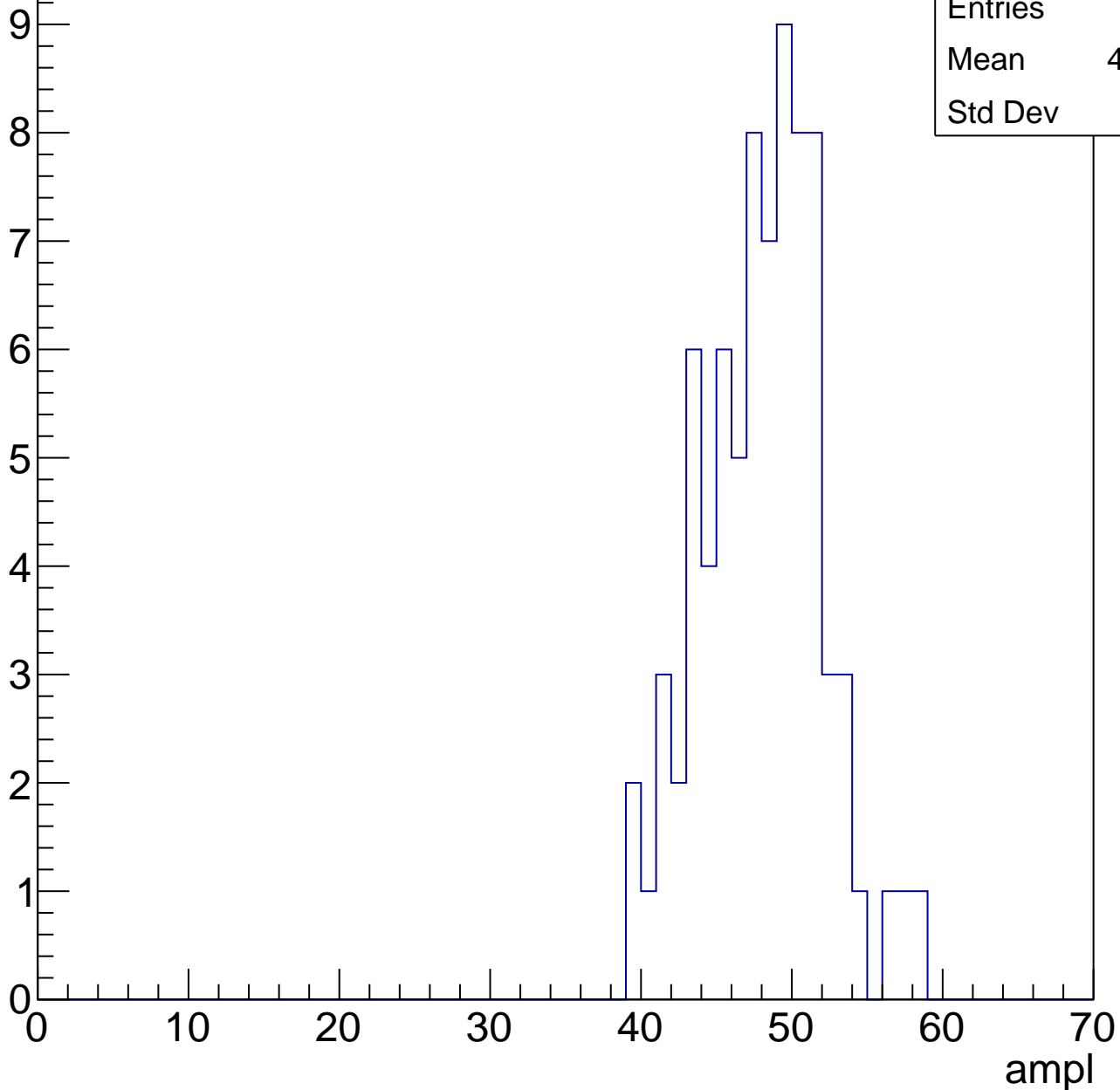


# B1L102S, U12-ch115, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	79
Mean	47.59
Std Dev	3.97

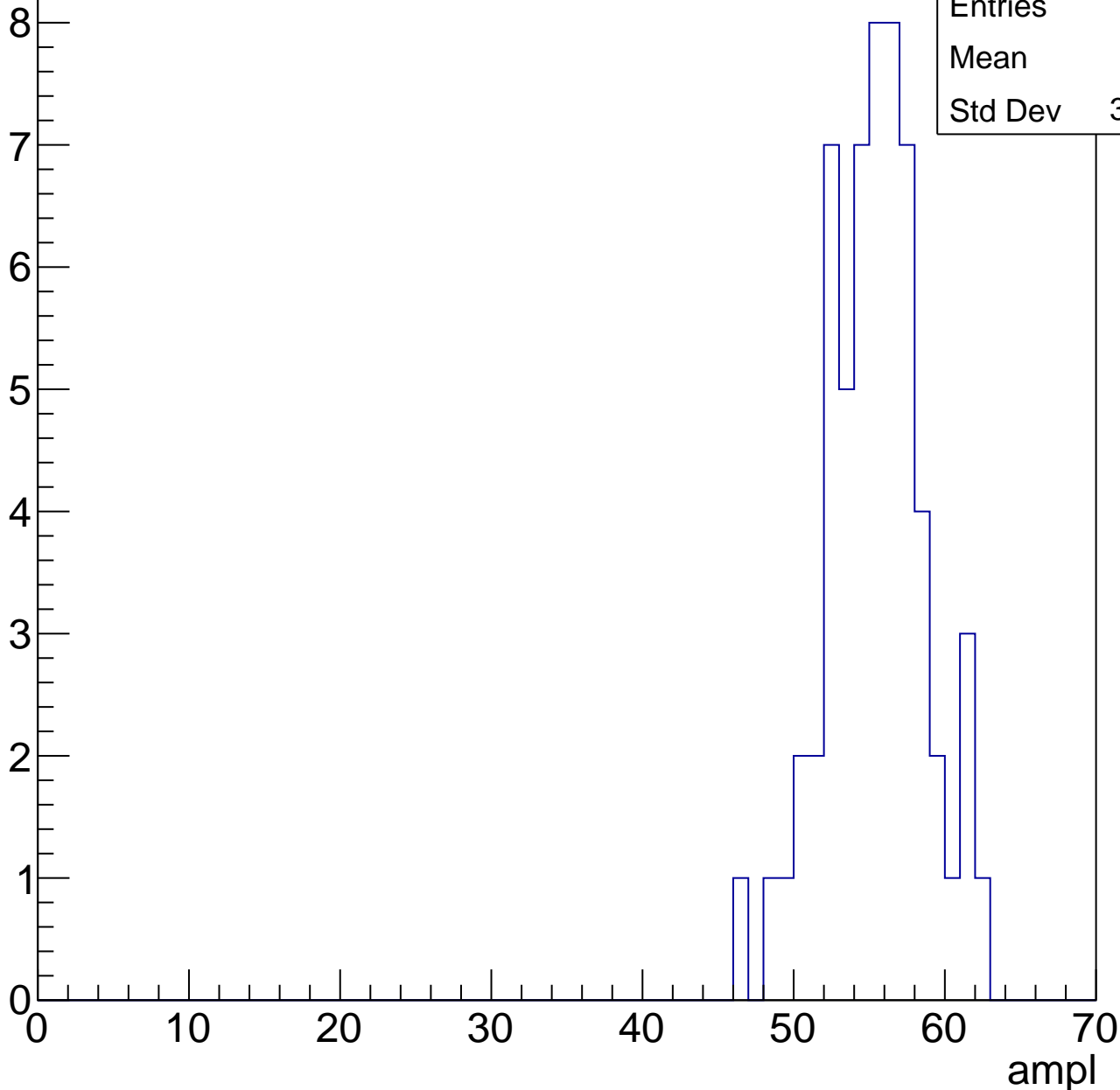


# B1L102S, U12-ch115, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

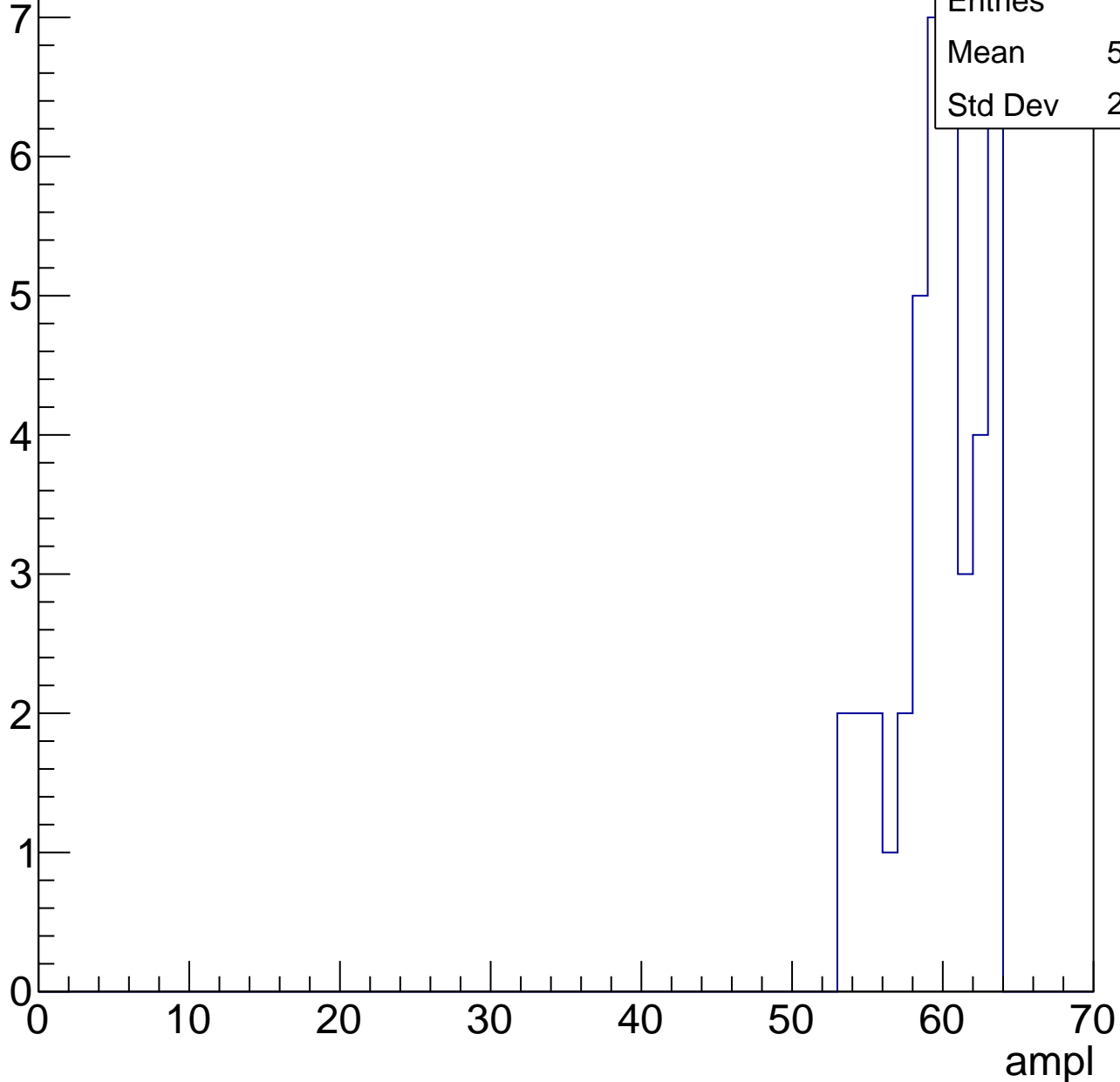
Entries	60
Mean	54.9
Std Dev	3.223



# B1L102S, U12-ch115, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



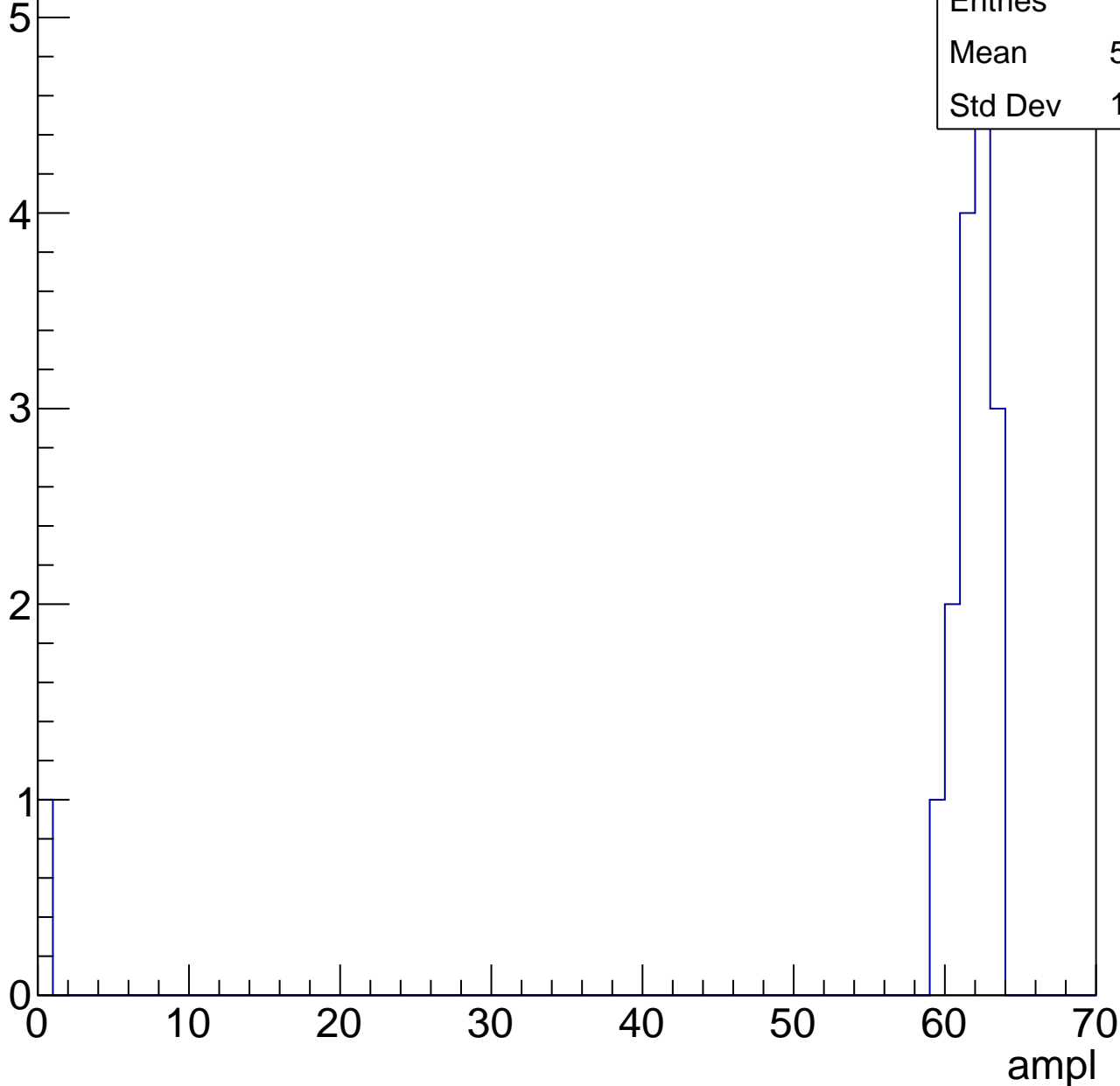
Entries	42
Mean	59.26
Std Dev	2.846

# B1L102S, U12-ch115, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	16
Mean	57.62
Std Dev	14.92

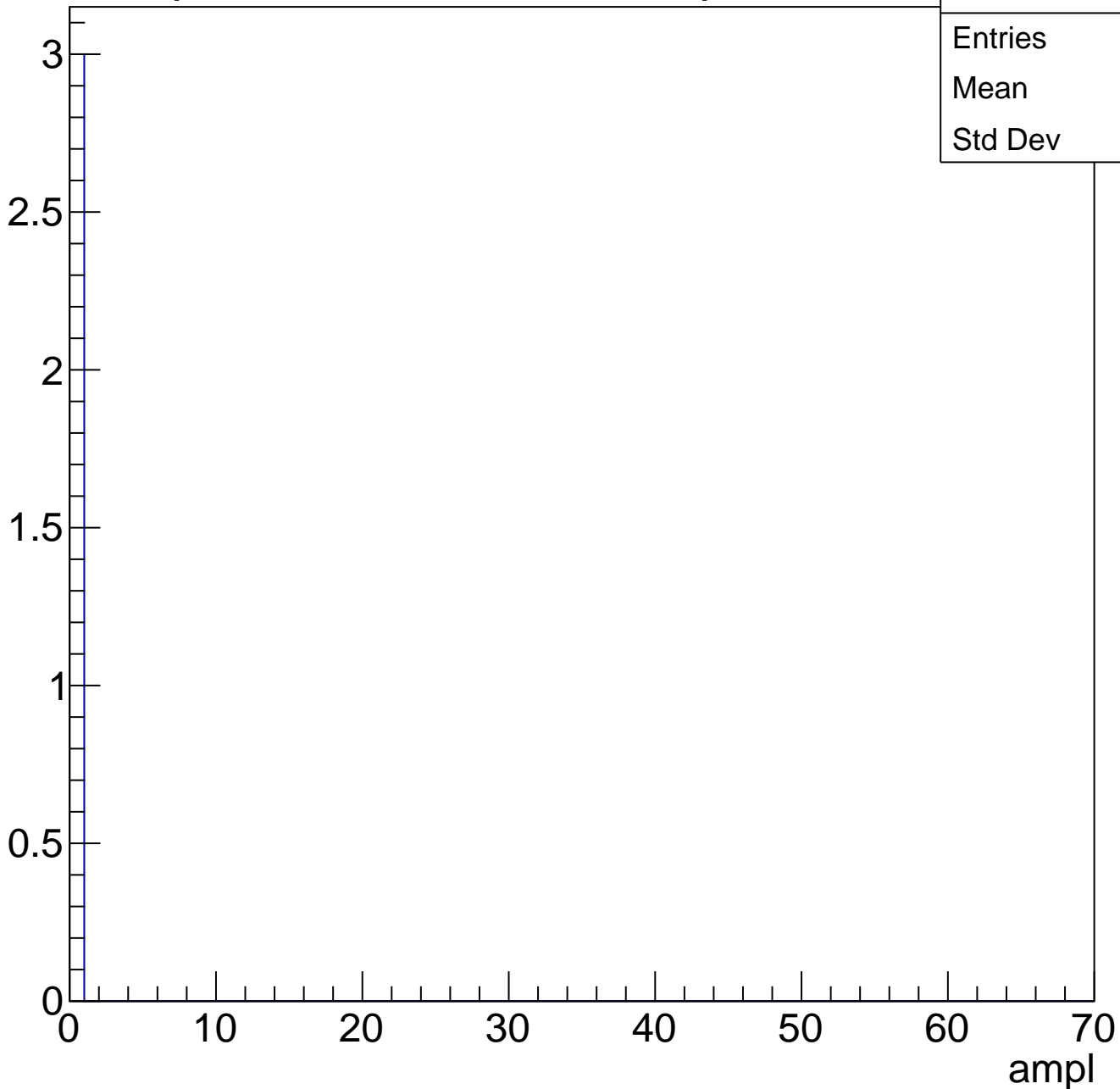




# B1L102S, U12-ch115, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	3
Mean	0
Std Dev	0

# B1L102S, U12-ch116, adc0

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	77
Mean	27.17
Std Dev	4.444

**Gaus mean : 28.1965**

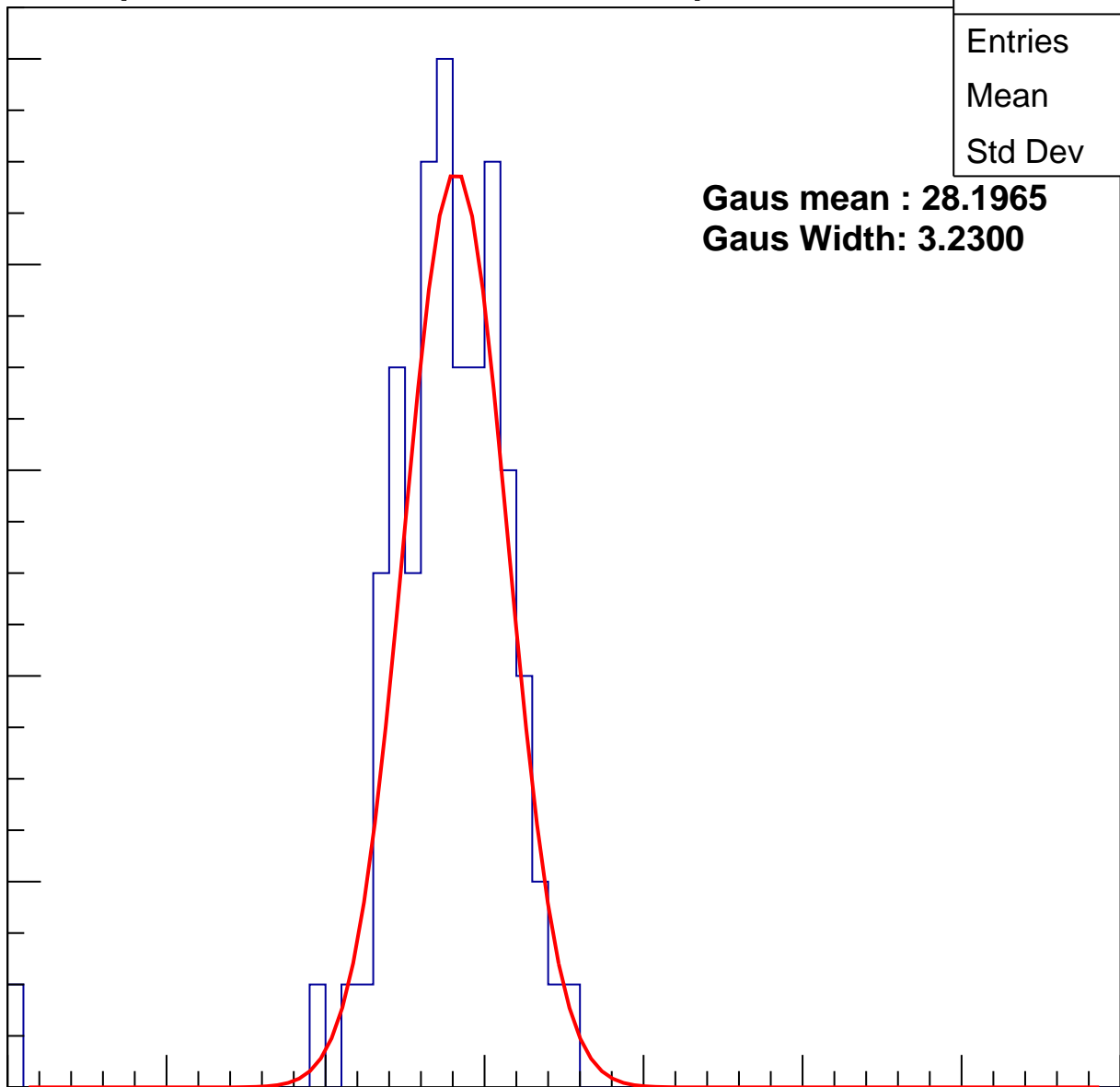
**Gaus Width: 3.2300**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L102S, U12-ch116, adc1

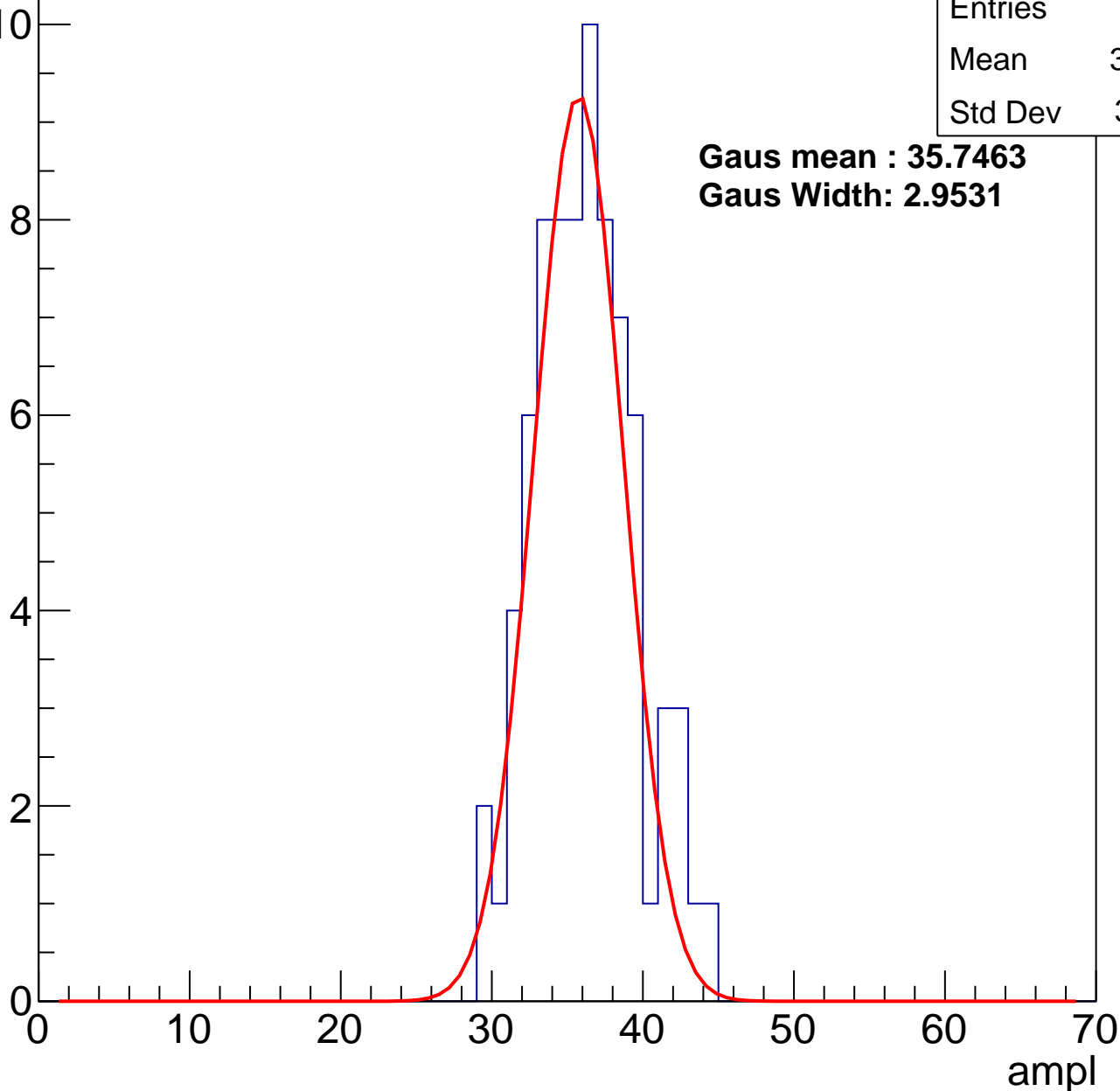
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	77
Mean	35.74
Std Dev	3.301

**Gaus mean : 35.7463**

**Gaus Width: 2.9531**



# B1L102S, U12-ch116, adc2

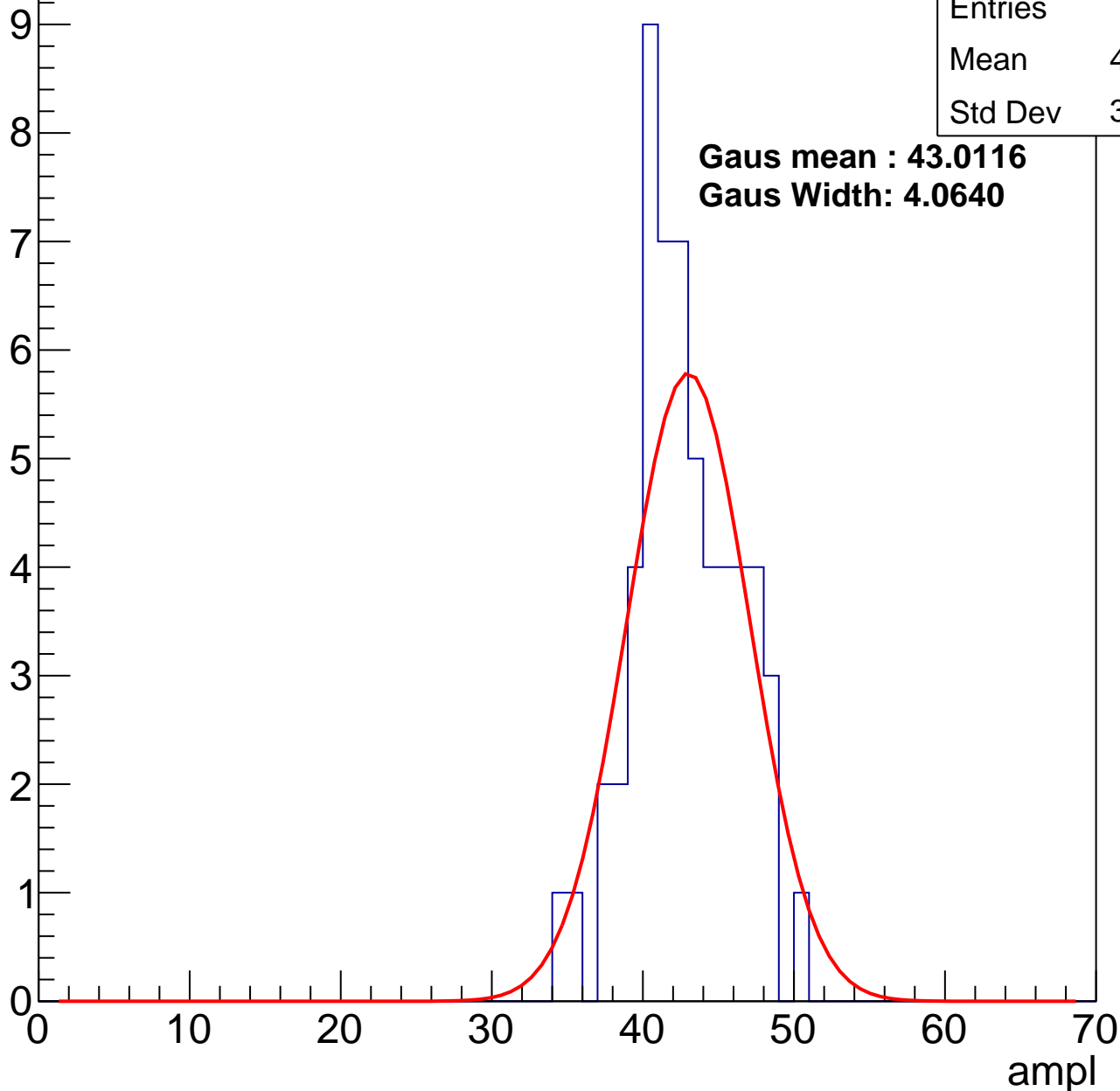
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	58
Mean	42.29
Std Dev	3.378

**Gaus mean : 43.0116**

**Gaus Width: 4.0640**

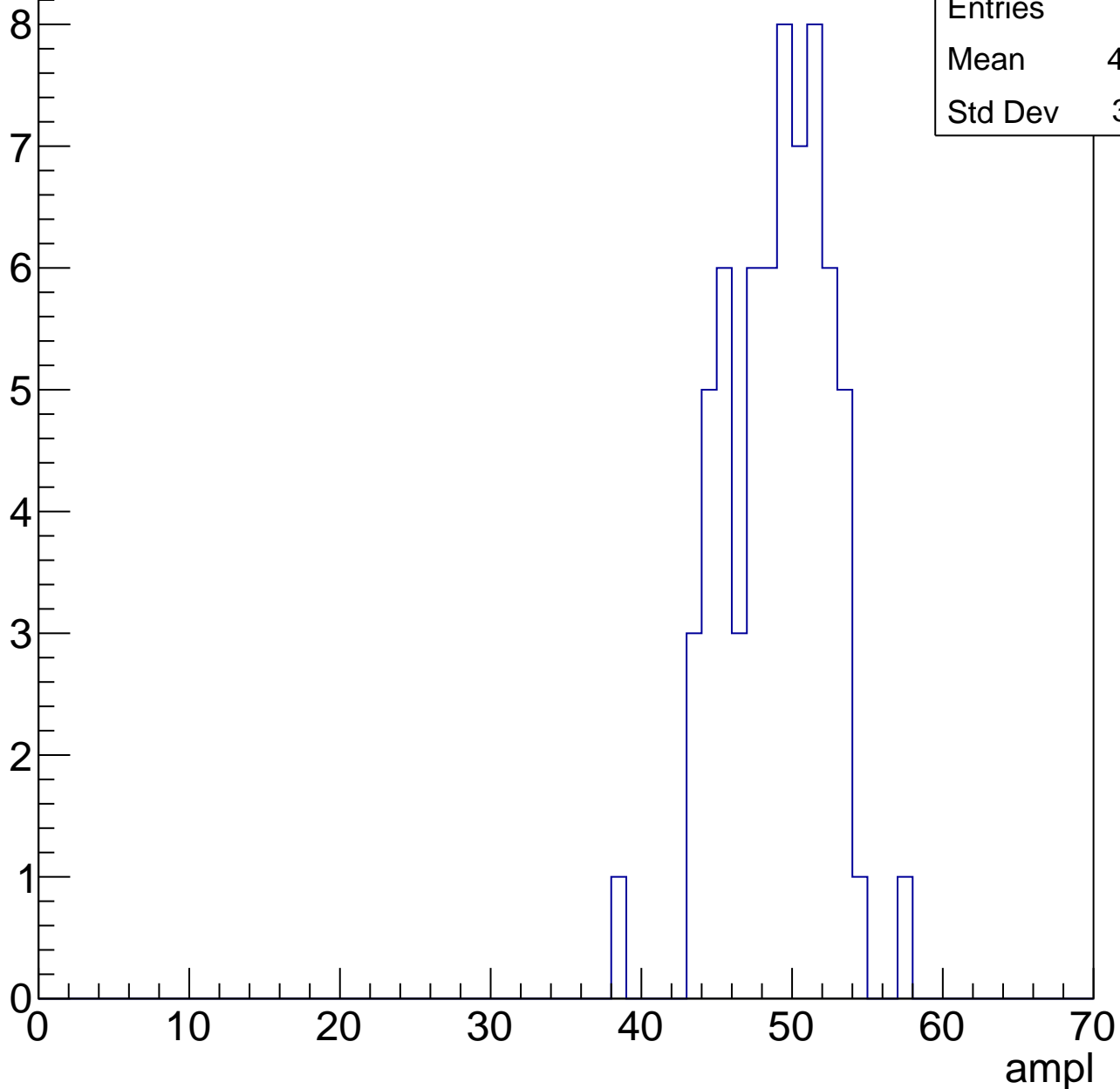


# B1L102S, U12-ch116, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	48.53
Std Dev	3.381

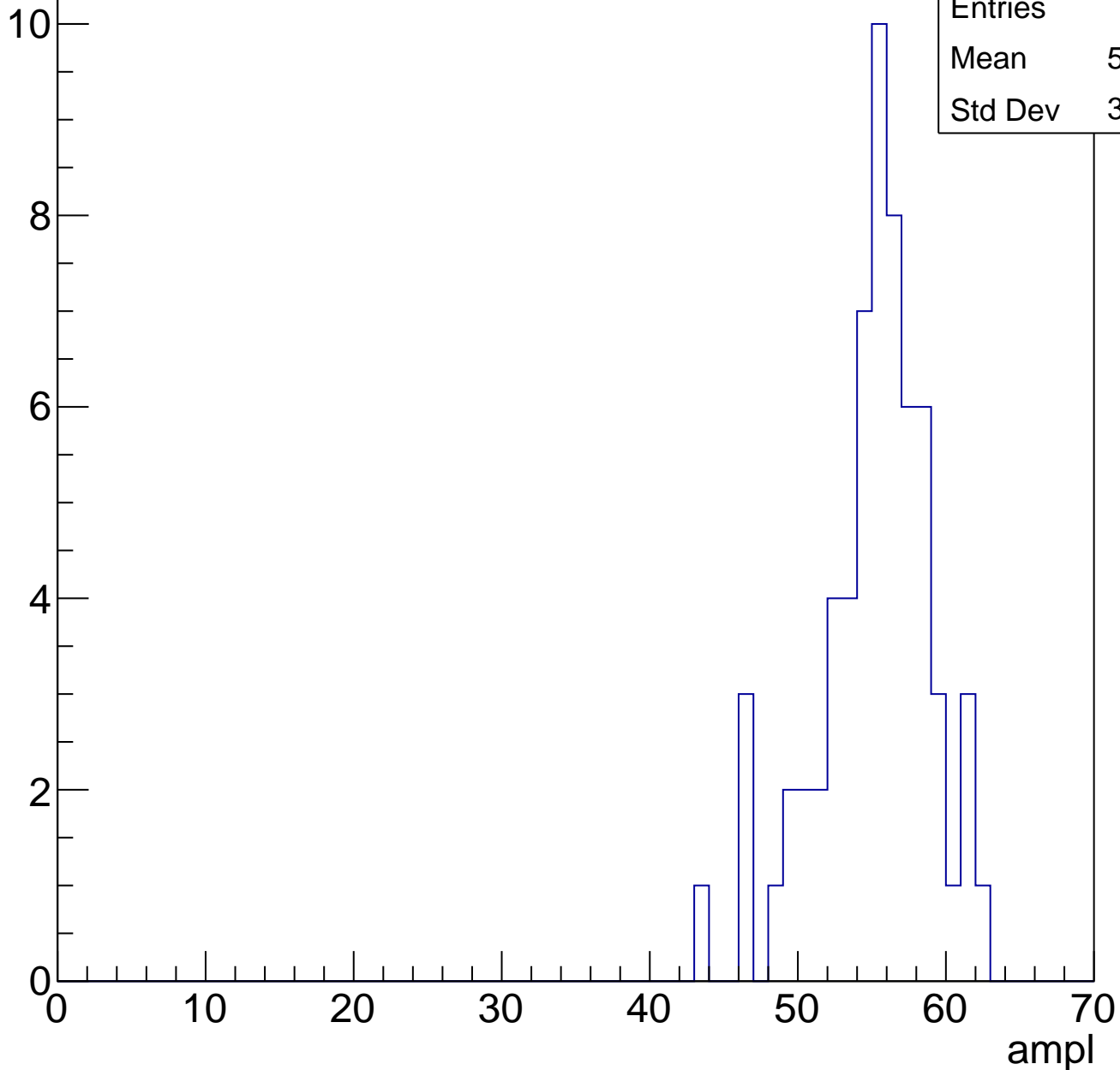


# B1L102S, U12-ch116, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	64
Mean	54.64
Std Dev	3.866

Entry

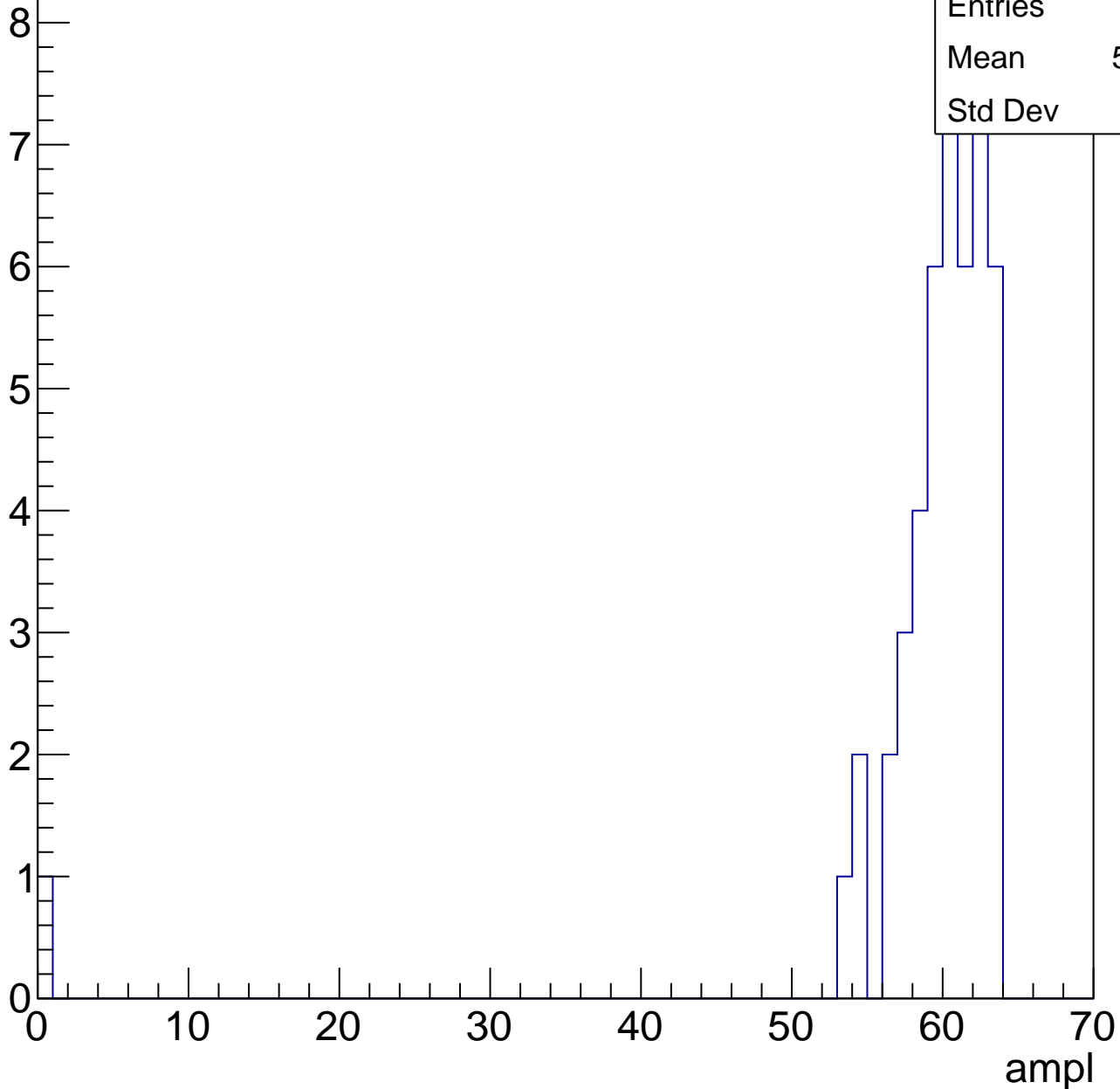


# B1L102S, U12-ch116, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

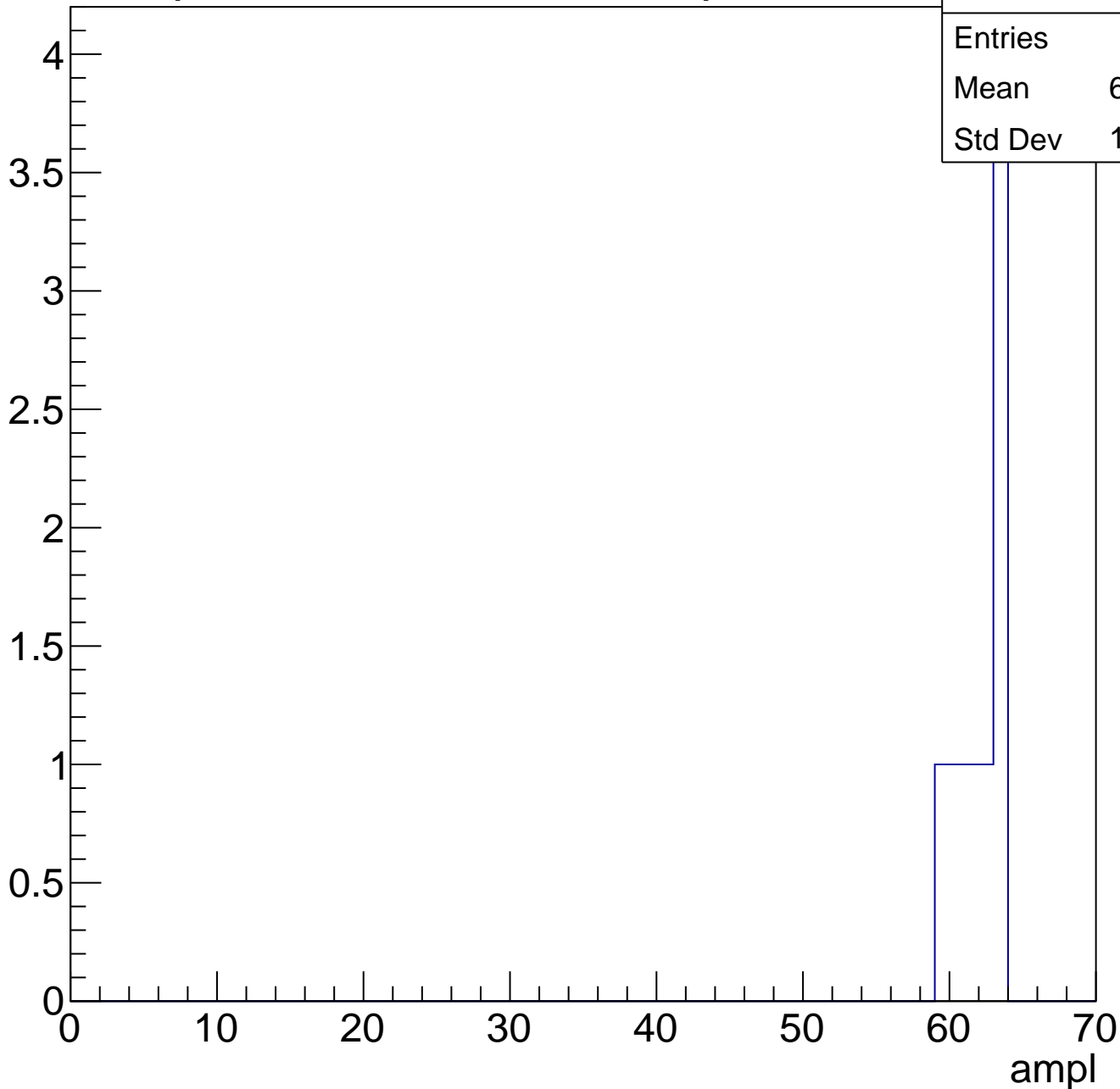
Entries	47
Mean	58.51
Std Dev	8.98



# B1L102S, U12-ch116, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U12-ch116, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U12-ch117, adc0

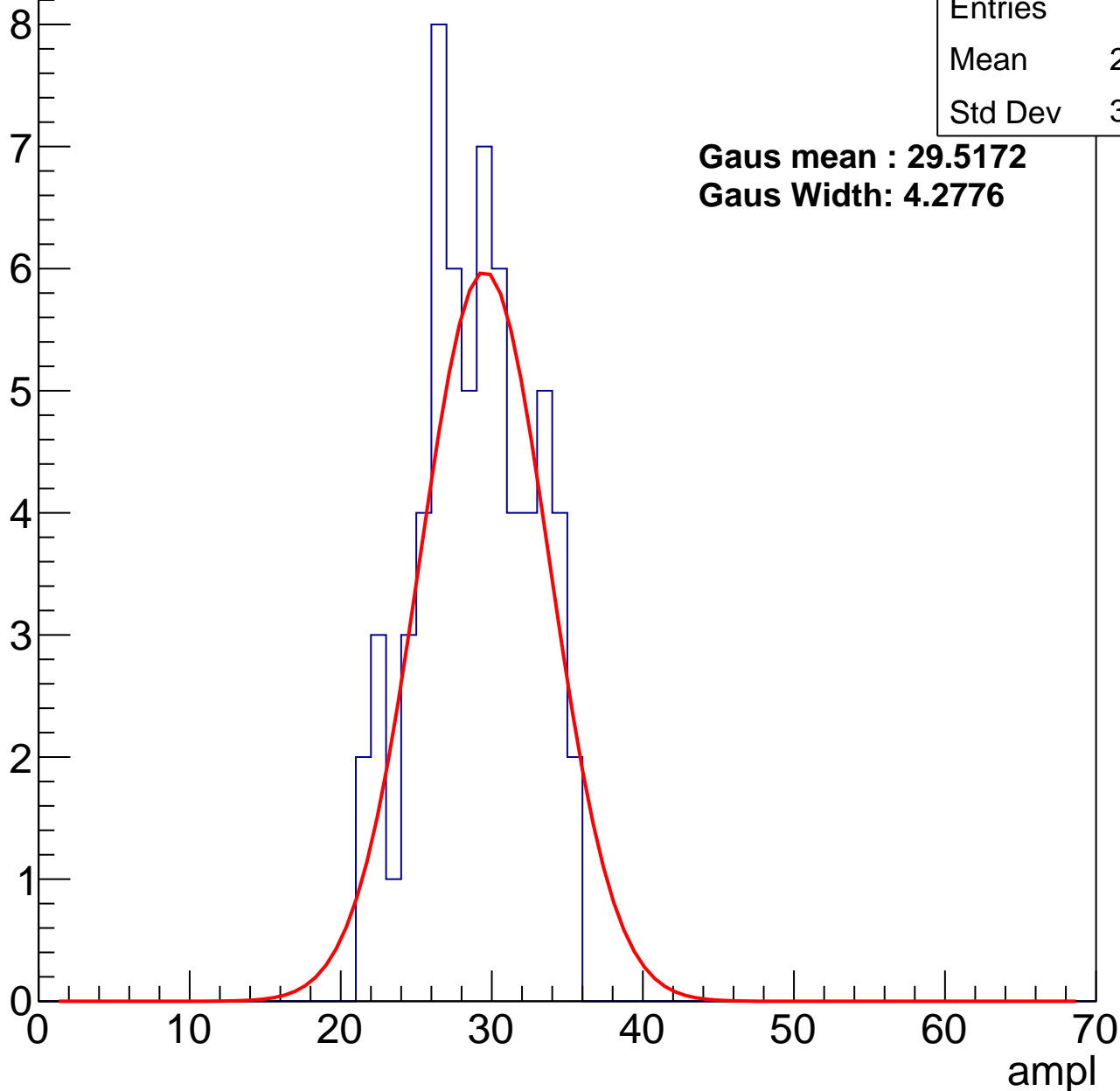
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	28.42
Std Dev	3.622

**Gaus mean : 29.5172**

**Gaus Width: 4.2776**



# B1L102S, U12-ch117, adc1

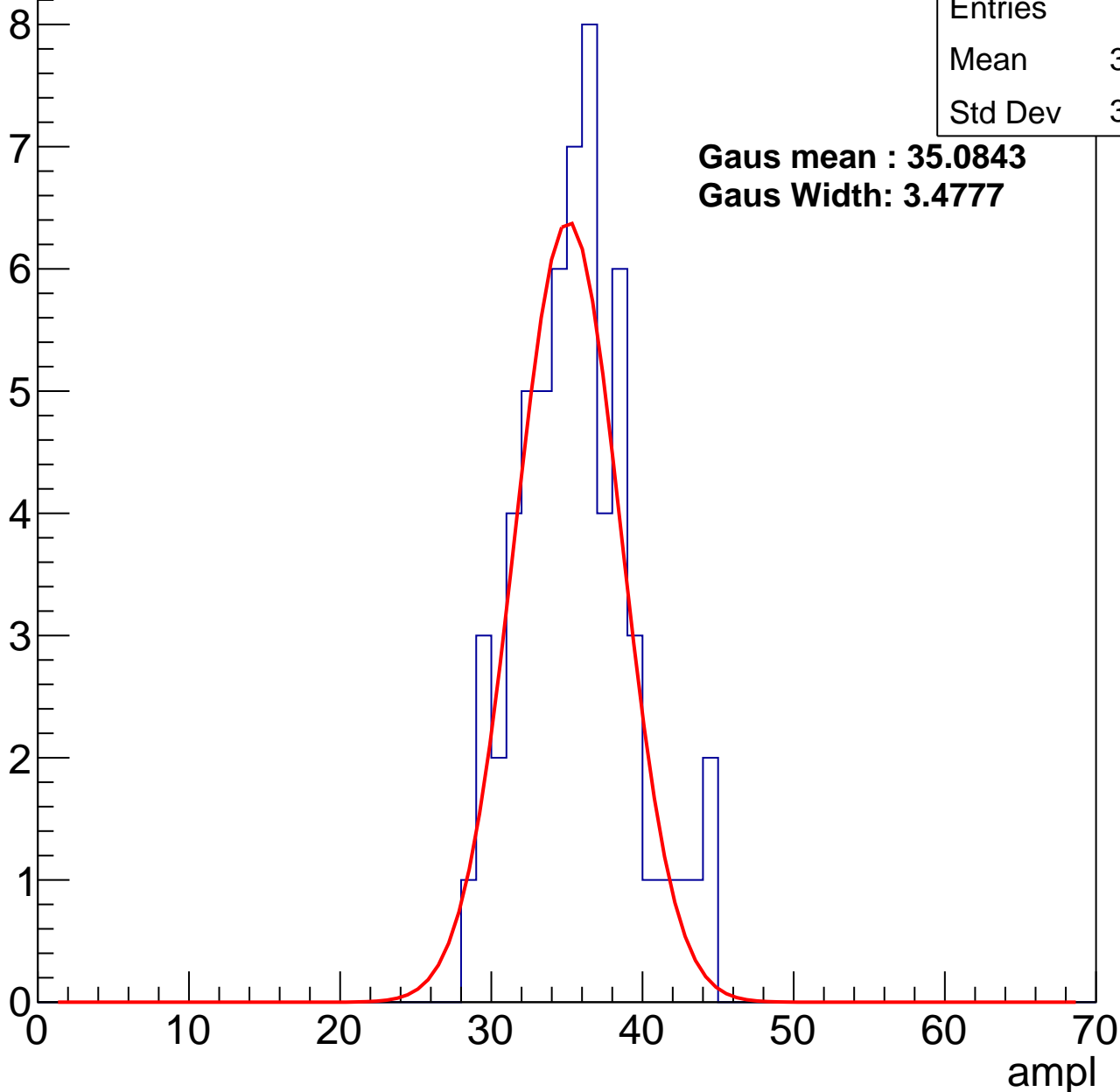
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	60
Mean	35.13
Std Dev	3.658

**Gaus mean : 35.0843**

**Gaus Width: 3.4777**



# B1L102S, U12-ch117, adc2

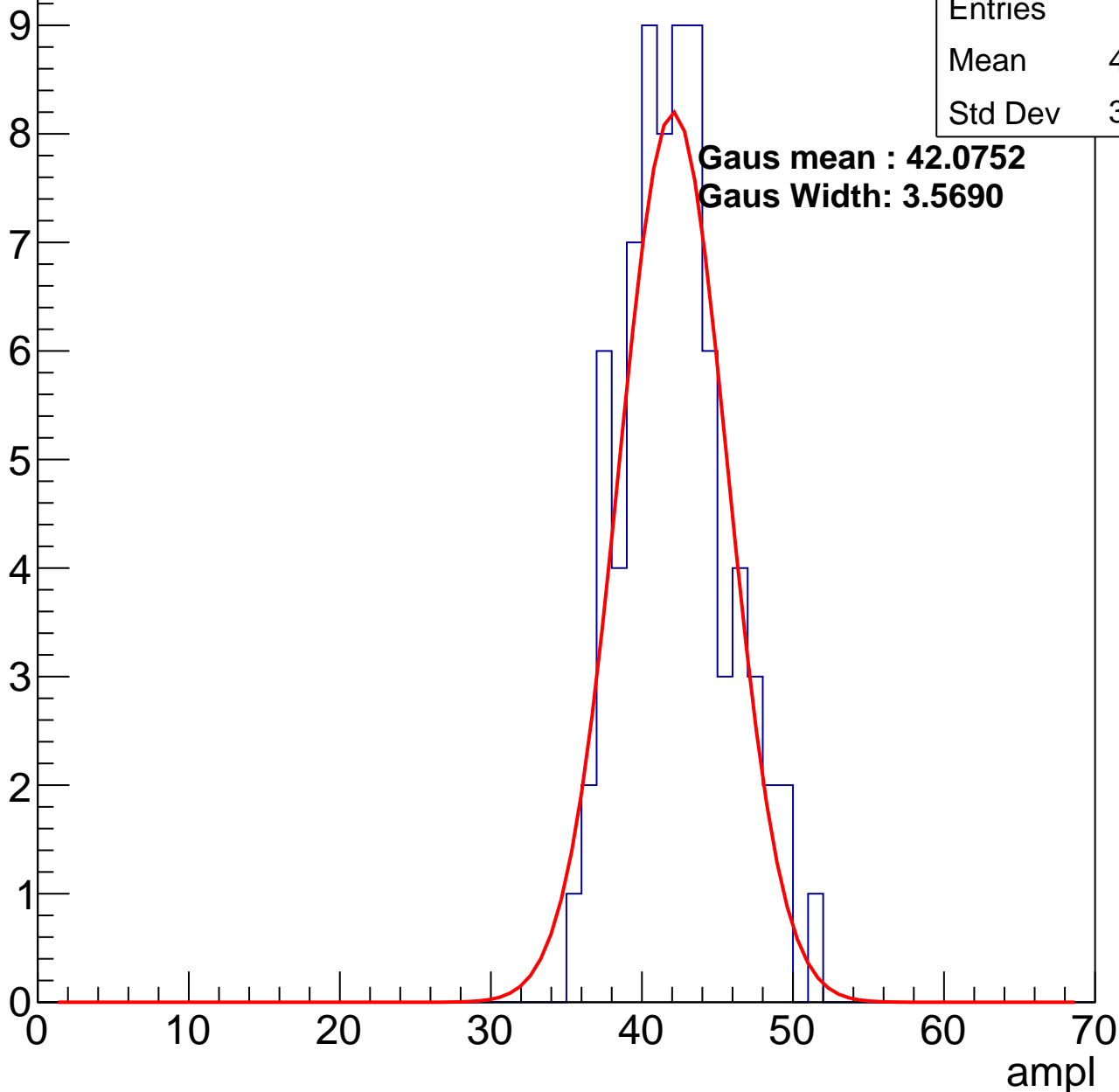
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	76
Mean	41.79
Std Dev	3.419

**Gaus mean : 42.0752**

**Gaus Width: 3.5690**

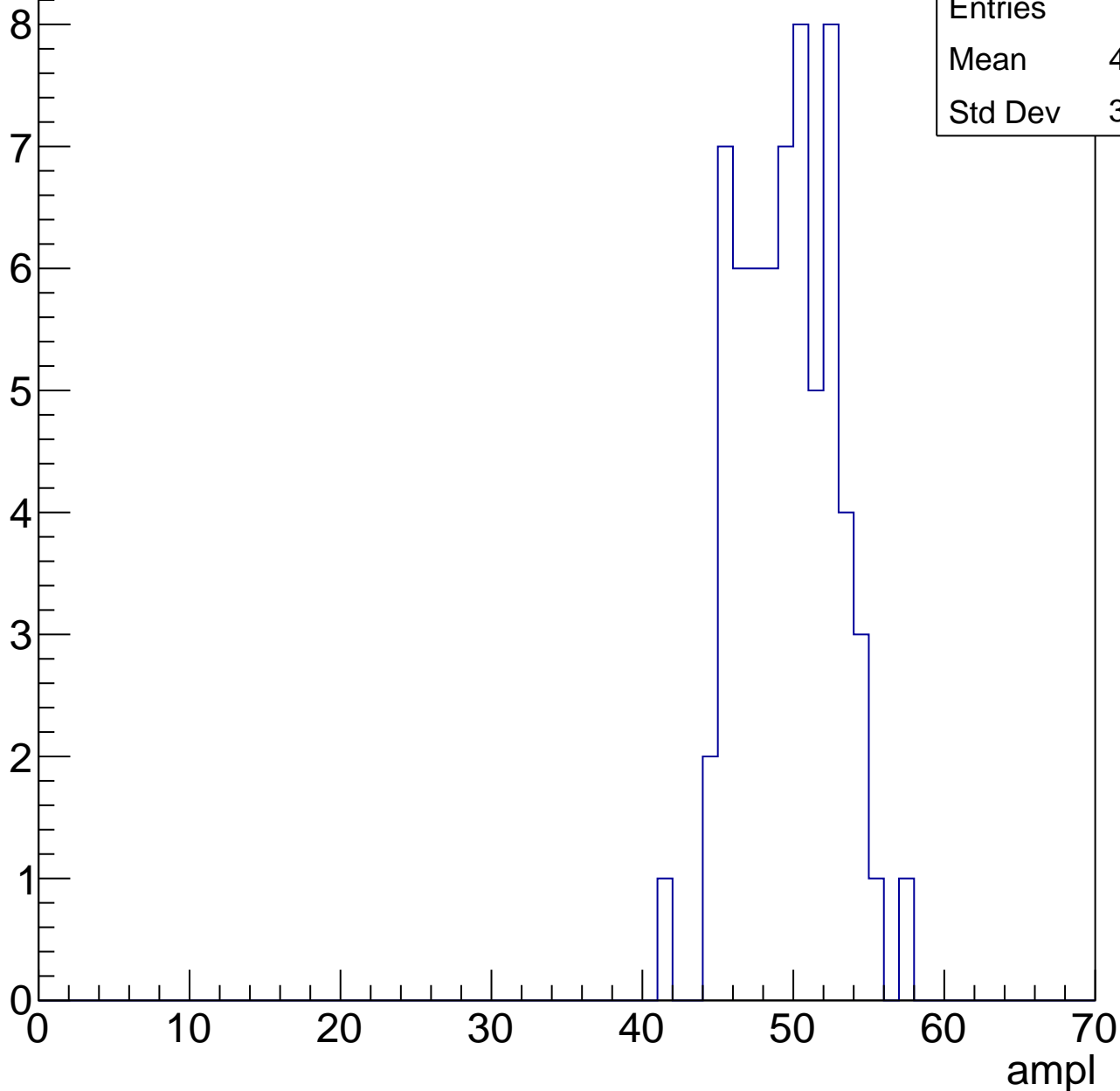


# B1L102S, U12-ch117, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	65
Mean	49.08
Std Dev	3.159

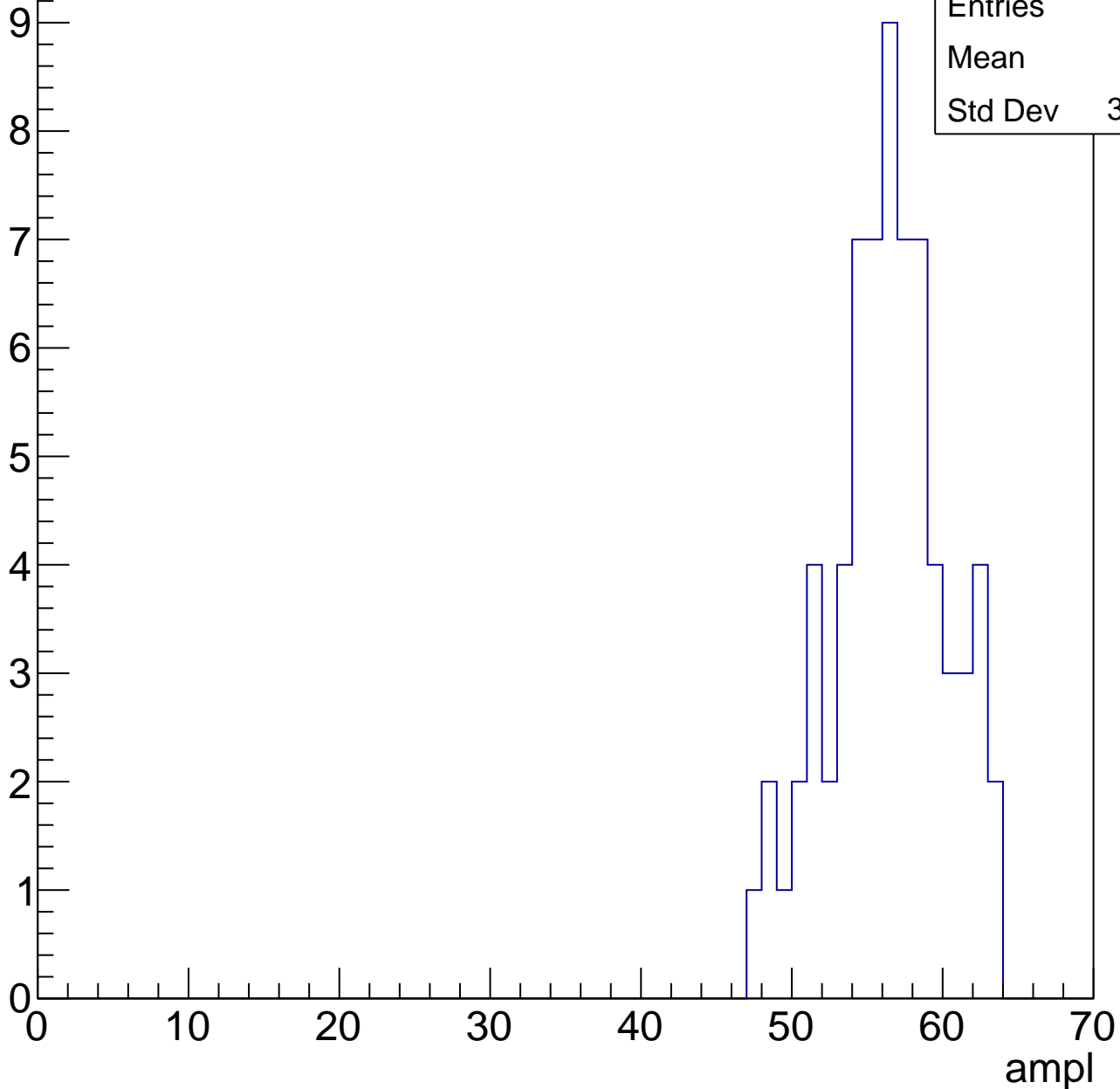


# B1L102S, U12-ch117, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	55.9
Std Dev	3.746

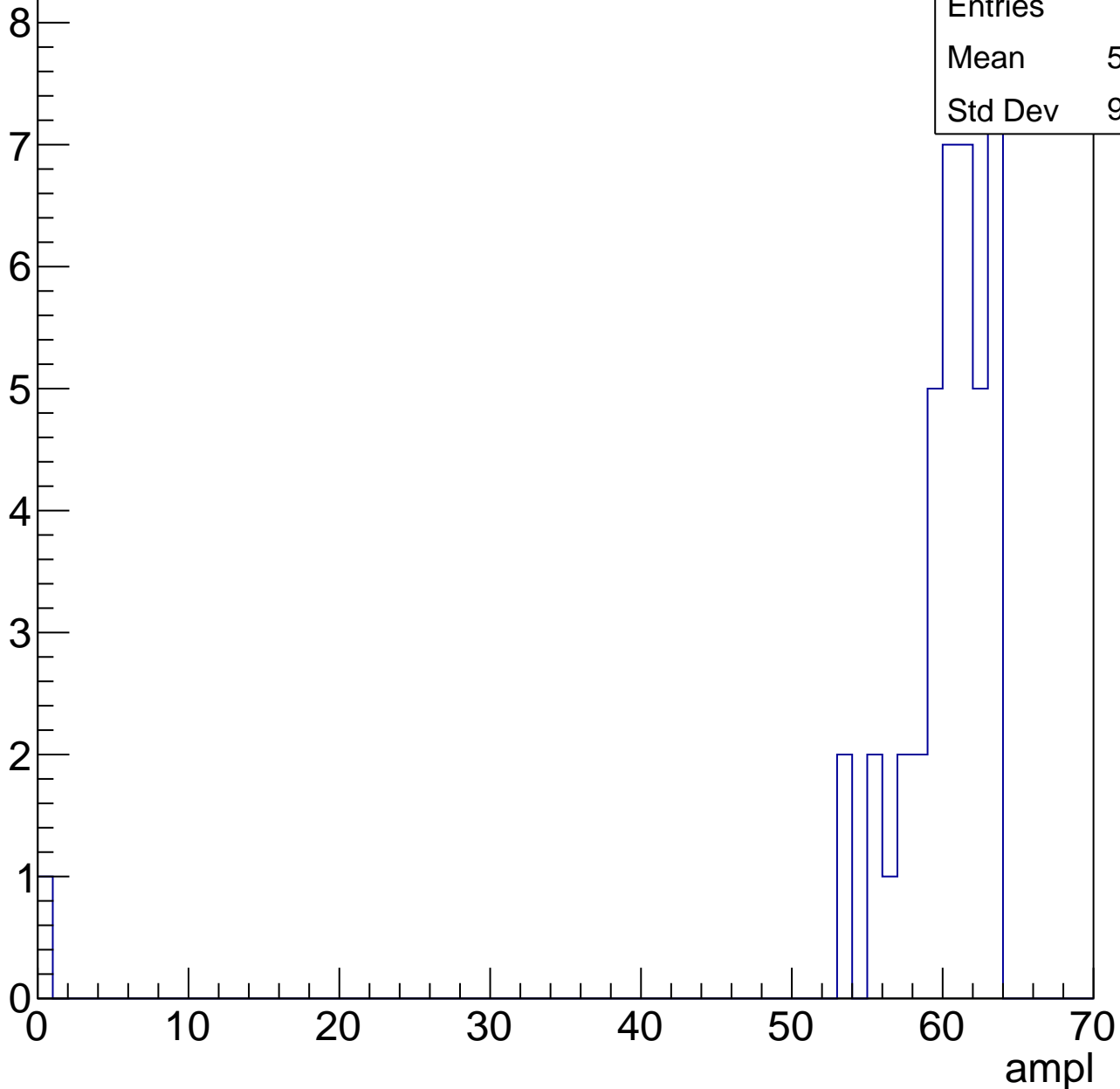


# B1L102S, U12-ch117, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

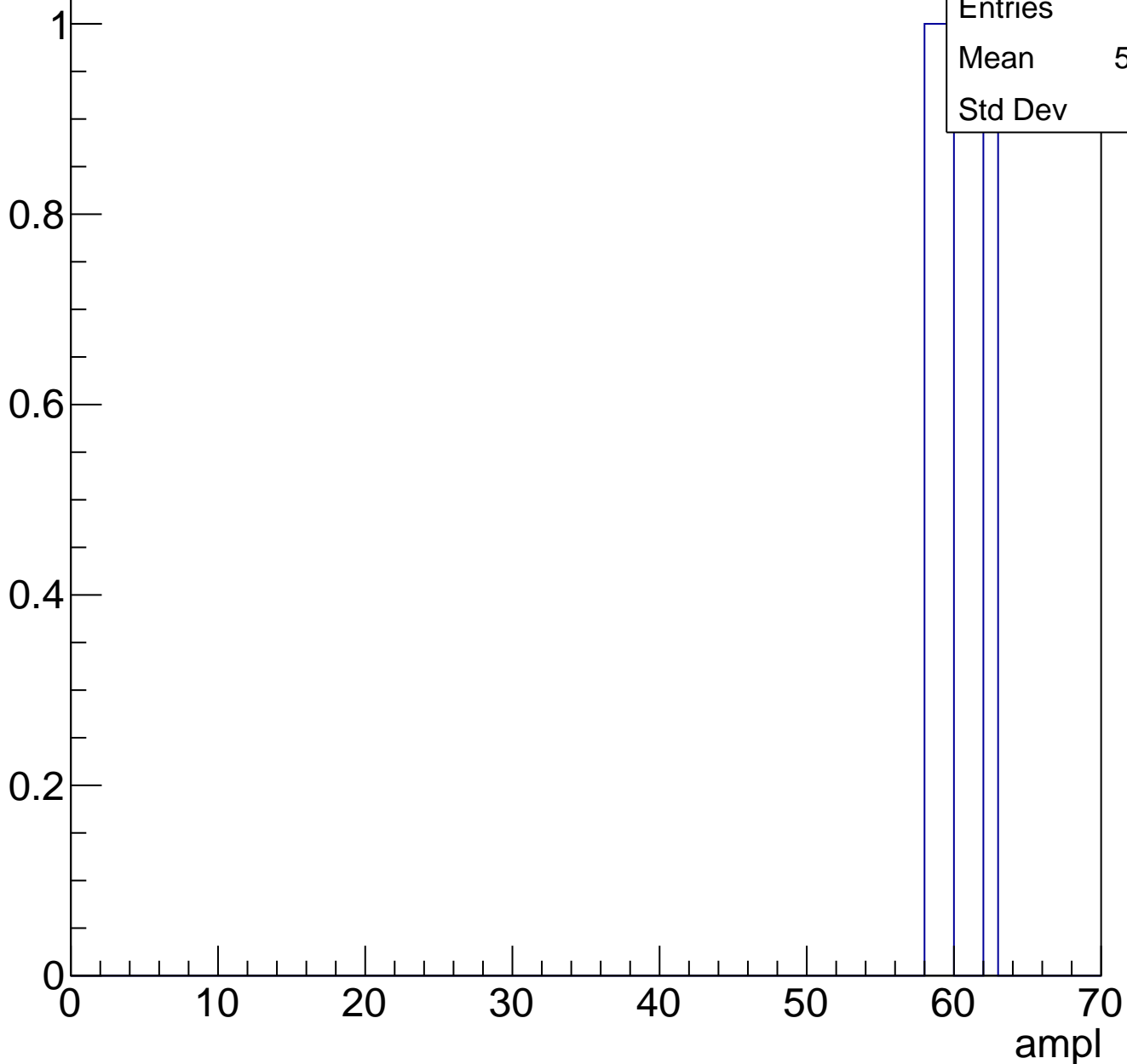
Entries	42
Mean	58.52
Std Dev	9.515



# B1L102S, U12-ch117, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U12-ch117, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

1

0.8

0.6

0.4

0.2

0

0

10

20

30

40

50

60

70

ampl

Entries

0

Mean

0

Std Dev

0

# B1L102S, U12-ch118, adc0

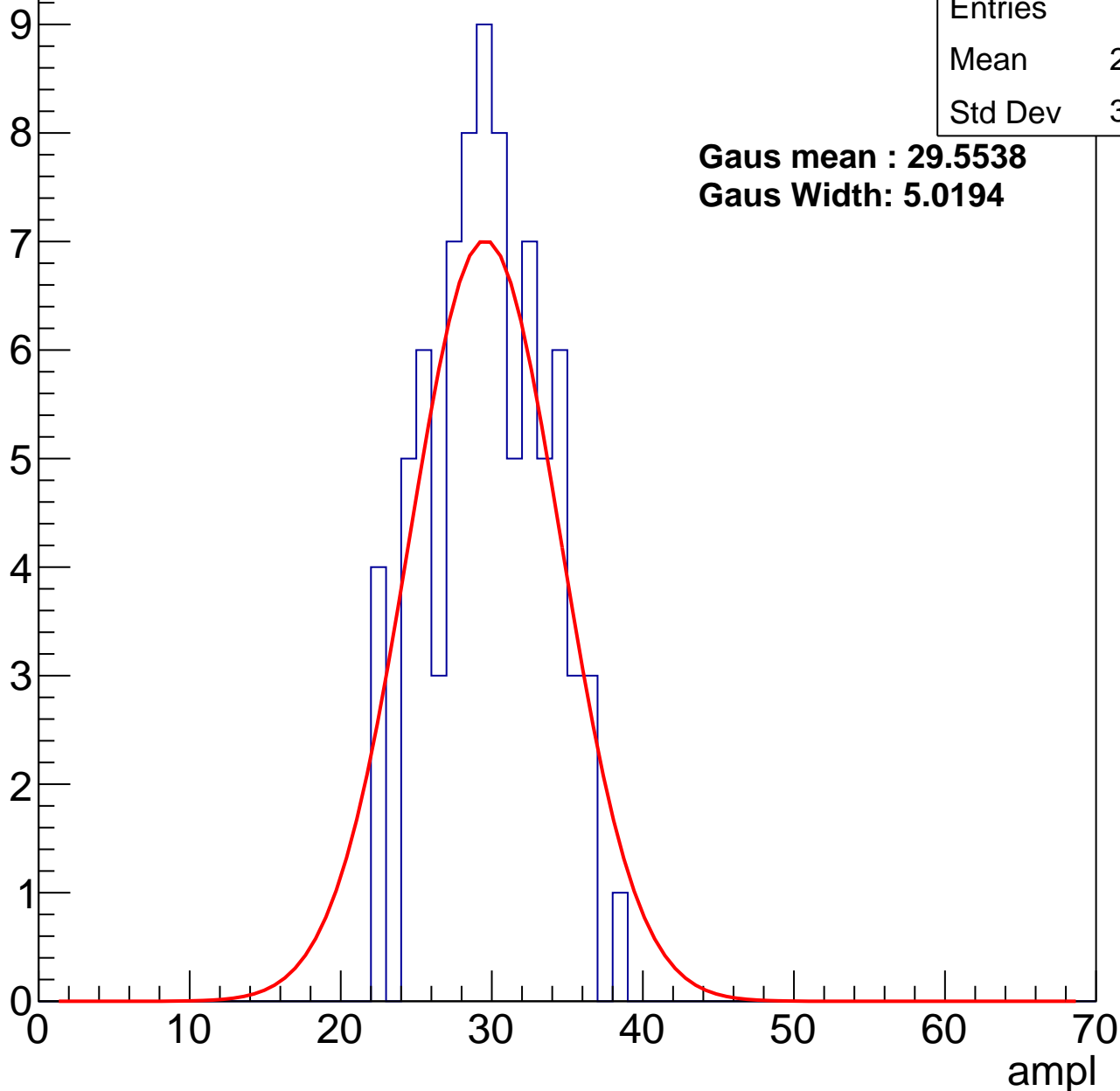
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	80
Mean	29.36
Std Dev	3.752

**Gaus mean : 29.5538**

**Gaus Width: 5.0194**



# B1L102S, U12-ch118, adc1

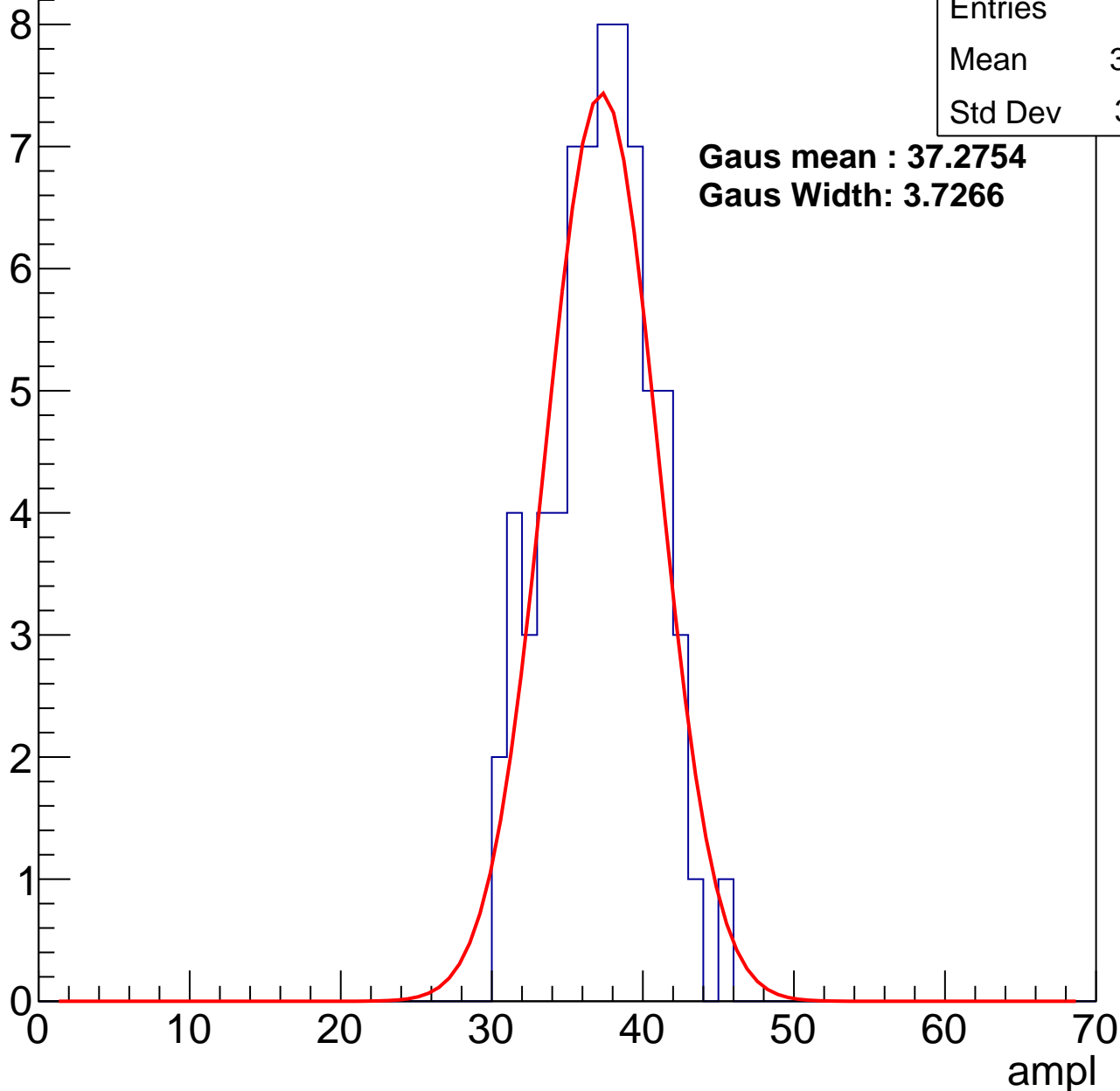
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	36.77
Std Dev	3.371

**Gaus mean : 37.2754**

**Gaus Width: 3.7266**



# B1L102S, U12-ch118, adc2

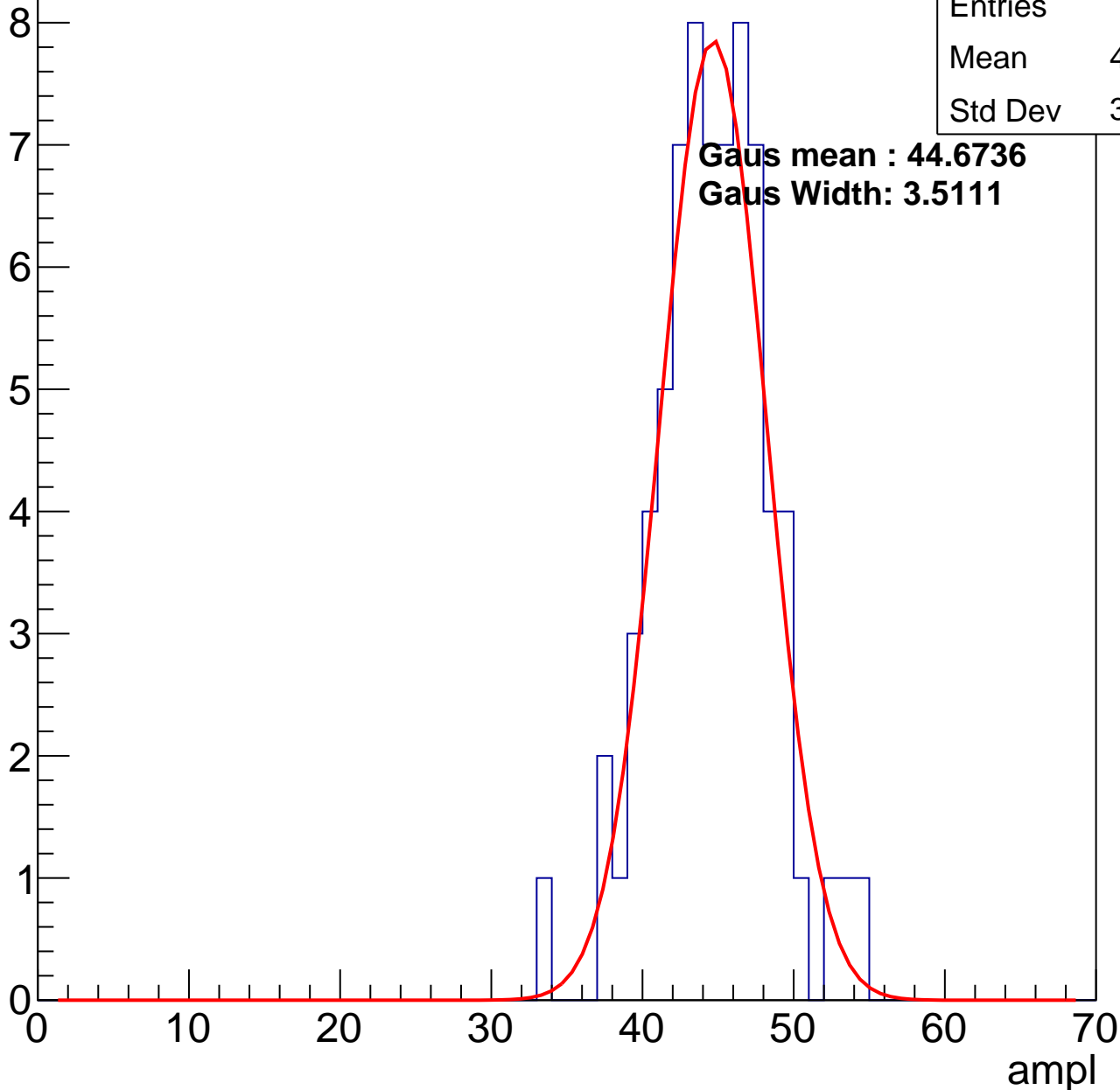
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	72
Mean	44.19
Std Dev	3.763

**Gaus mean : 44.6736**

**Gaus Width: 3.5111**

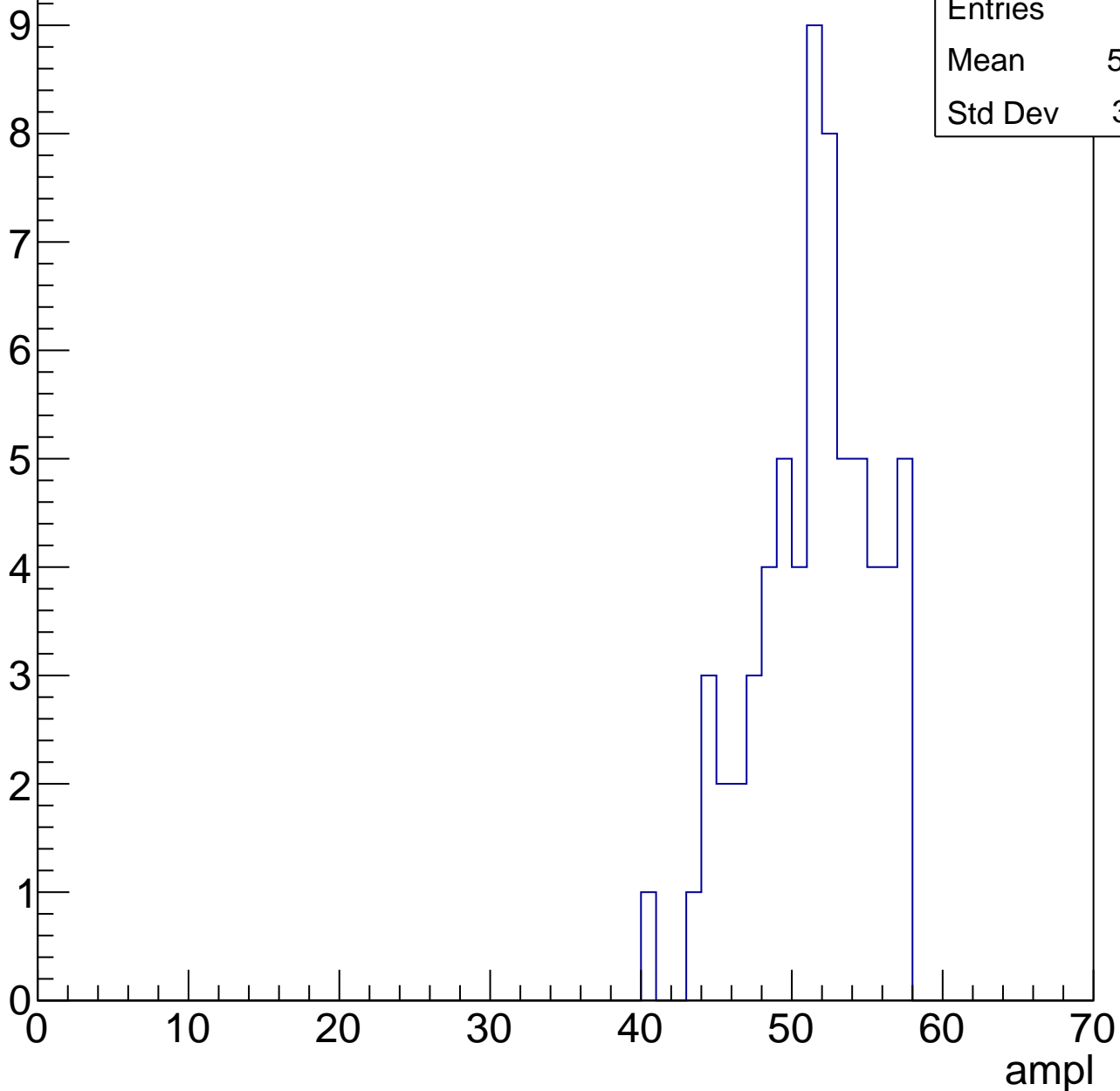


# B1L102S, U12-ch118, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	65
Mean	50.98
Std Dev	3.881

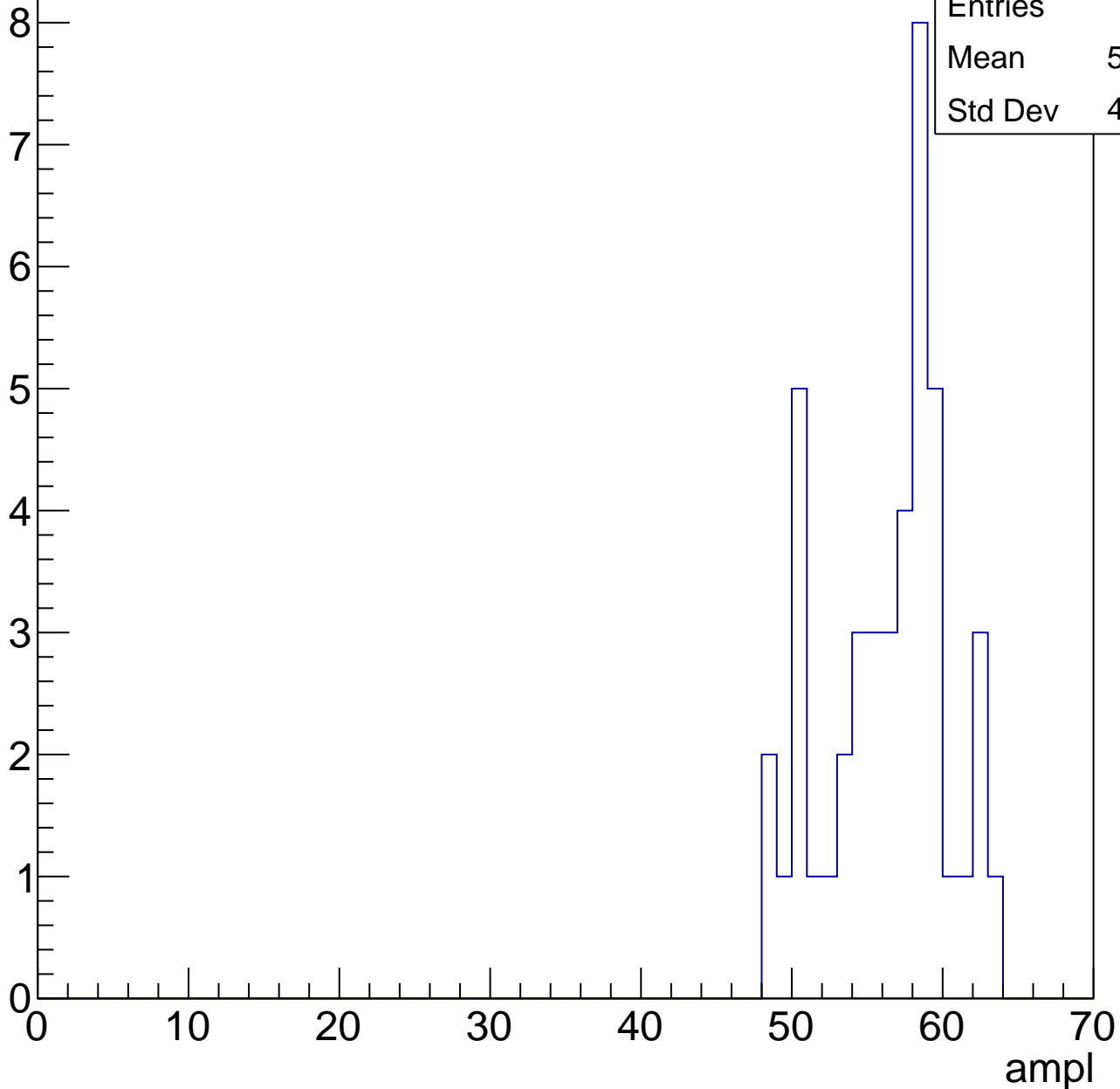


# B1L102S, U12-ch118, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	44
Mean	55.82
Std Dev	4.013

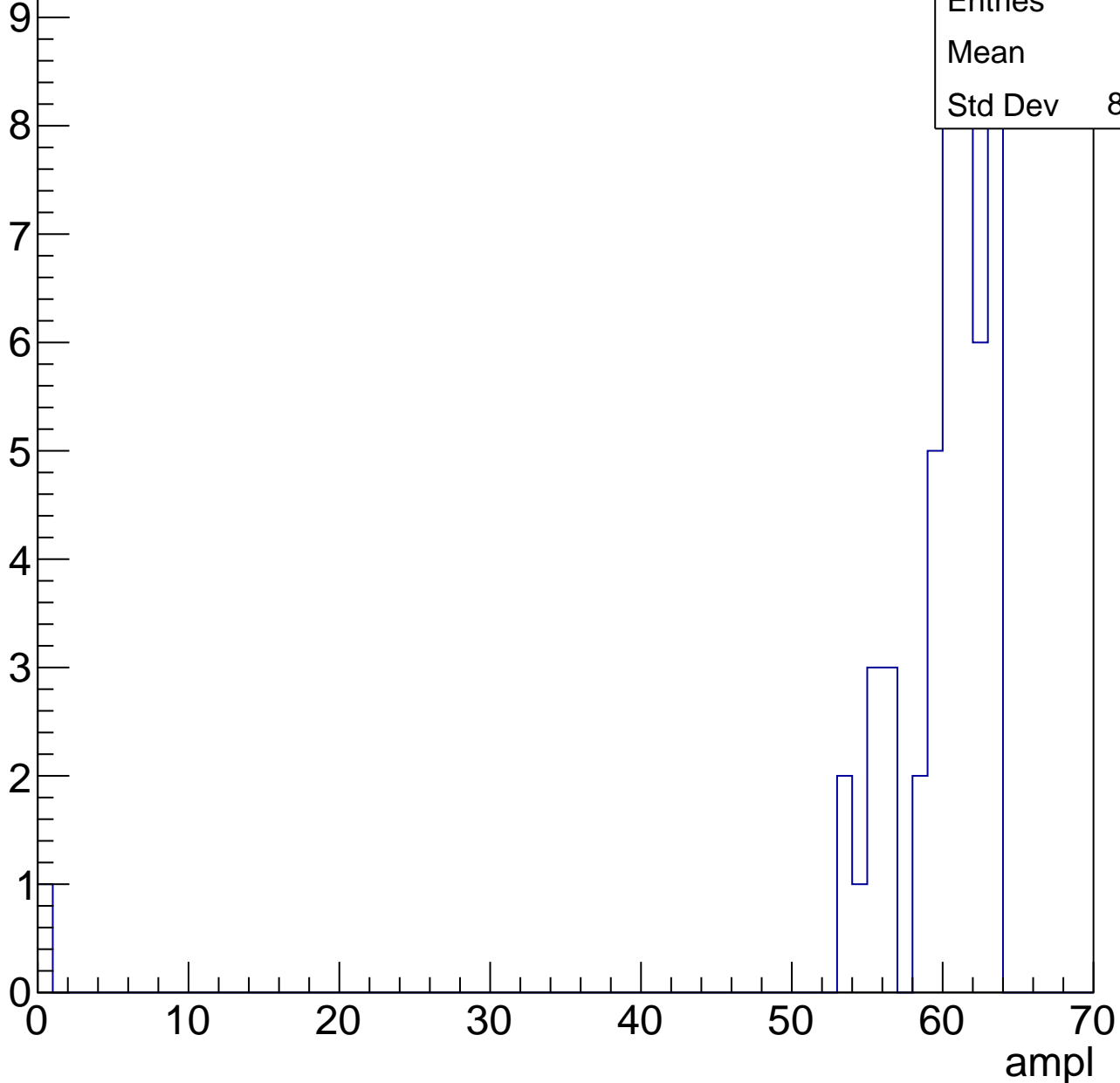


# B1L102S, U12-ch118, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

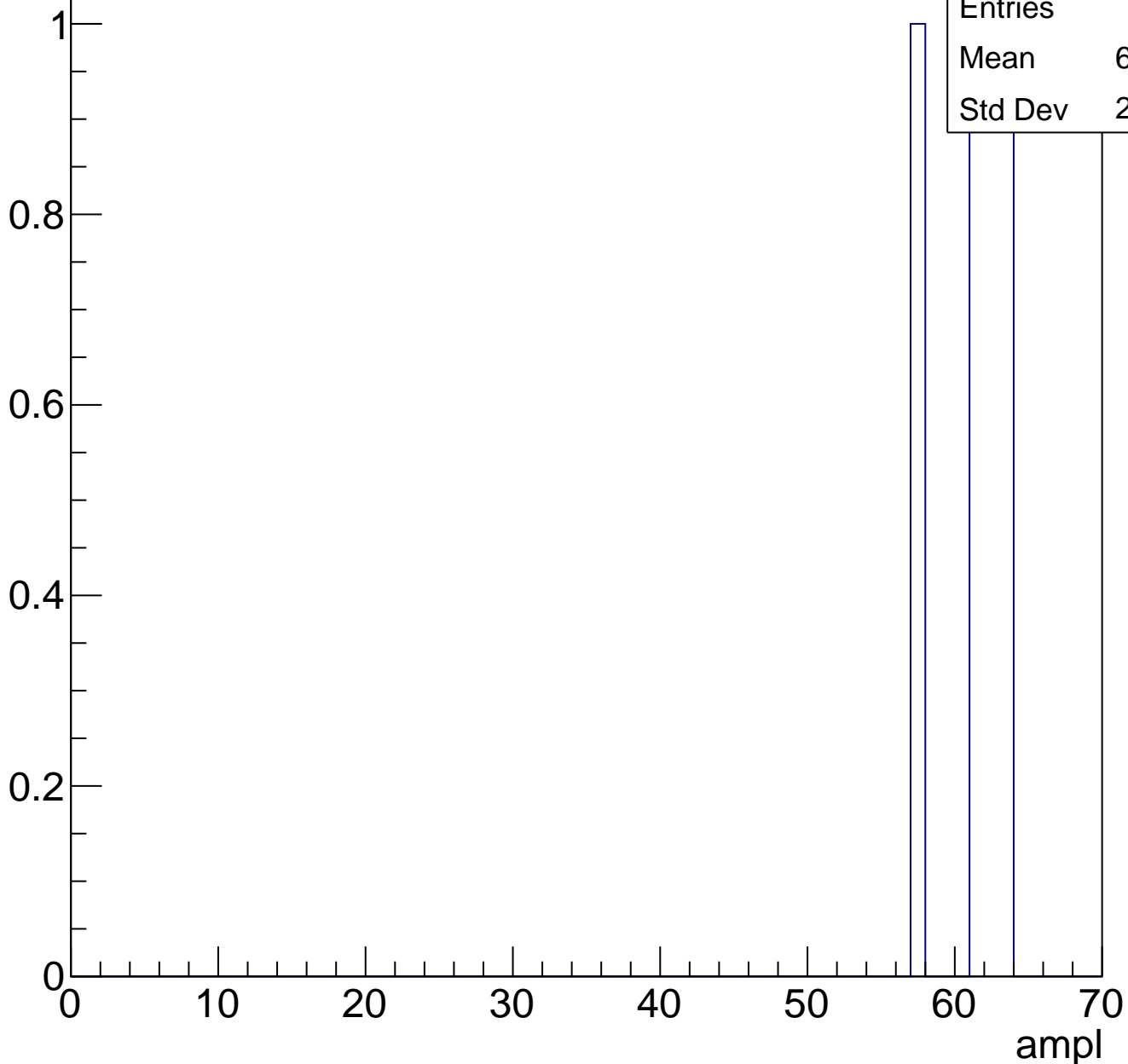
Entries	48
Mean	58.5
Std Dev	8.975



# B1L102S, U12-ch118, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	4
Mean	60.75
Std Dev	2.278



# B1L102S, U12-ch118, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	2
Mean	10
Std Dev	10

# B1L102S, U12-ch119, adc0

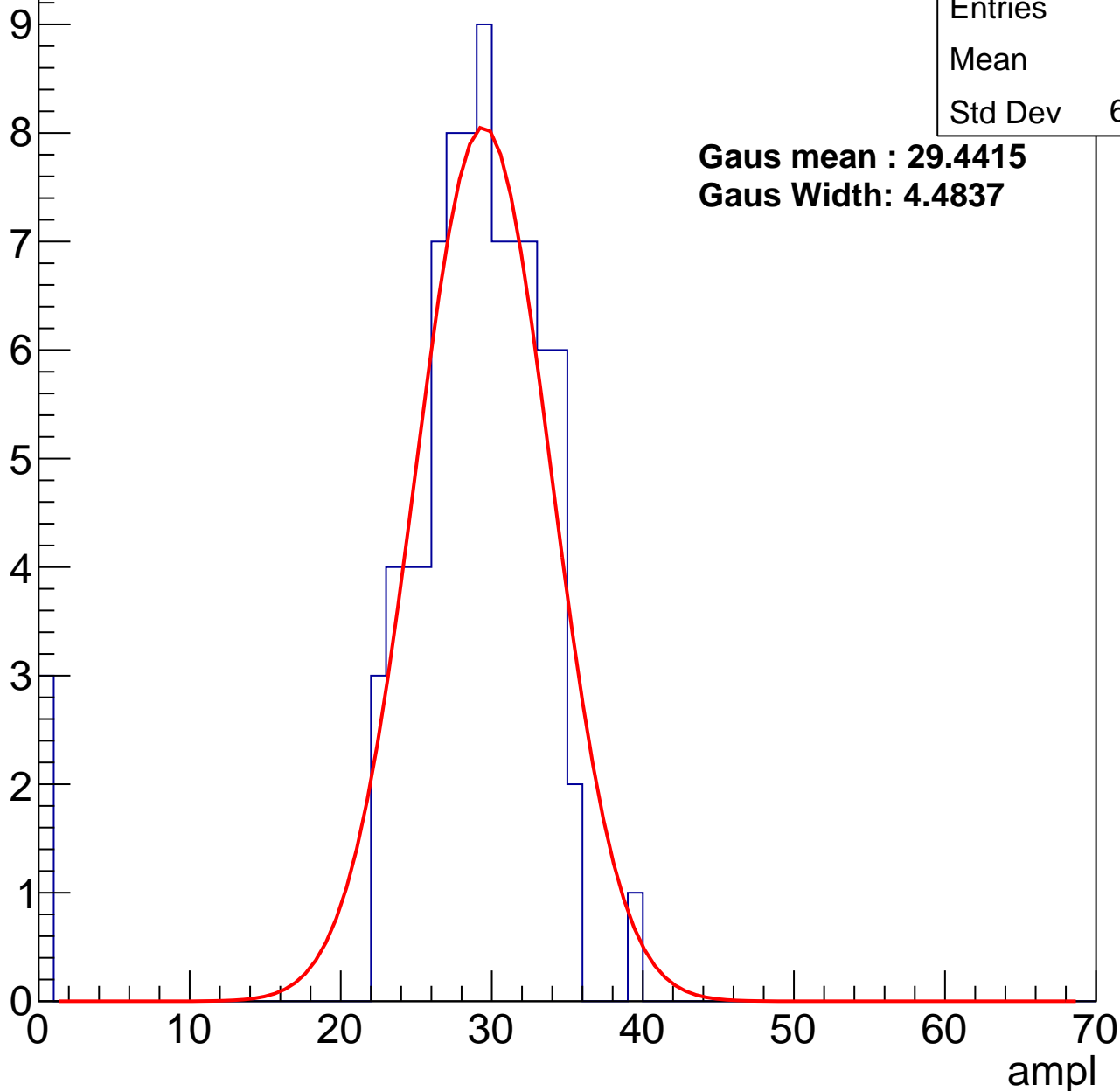
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	86
Mean	27.9
Std Dev	6.372

**Gaus mean : 29.4415**

**Gaus Width: 4.4837**



# B1L102S, U12-ch119, adc1

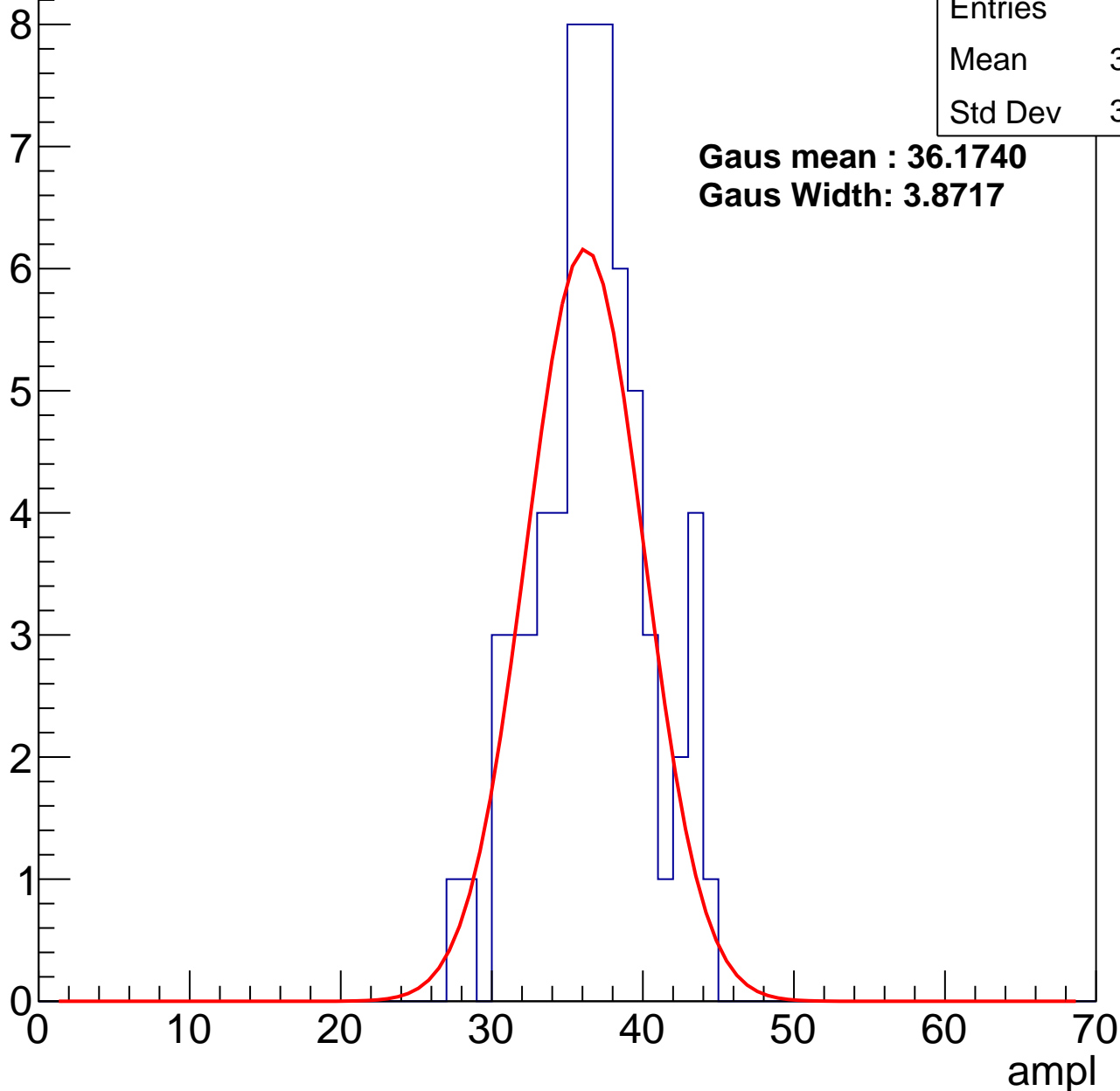
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	65
Mean	36.15
Std Dev	3.755

**Gaus mean : 36.1740**

**Gaus Width: 3.8717**



# B1L102S, U12-ch119, adc2

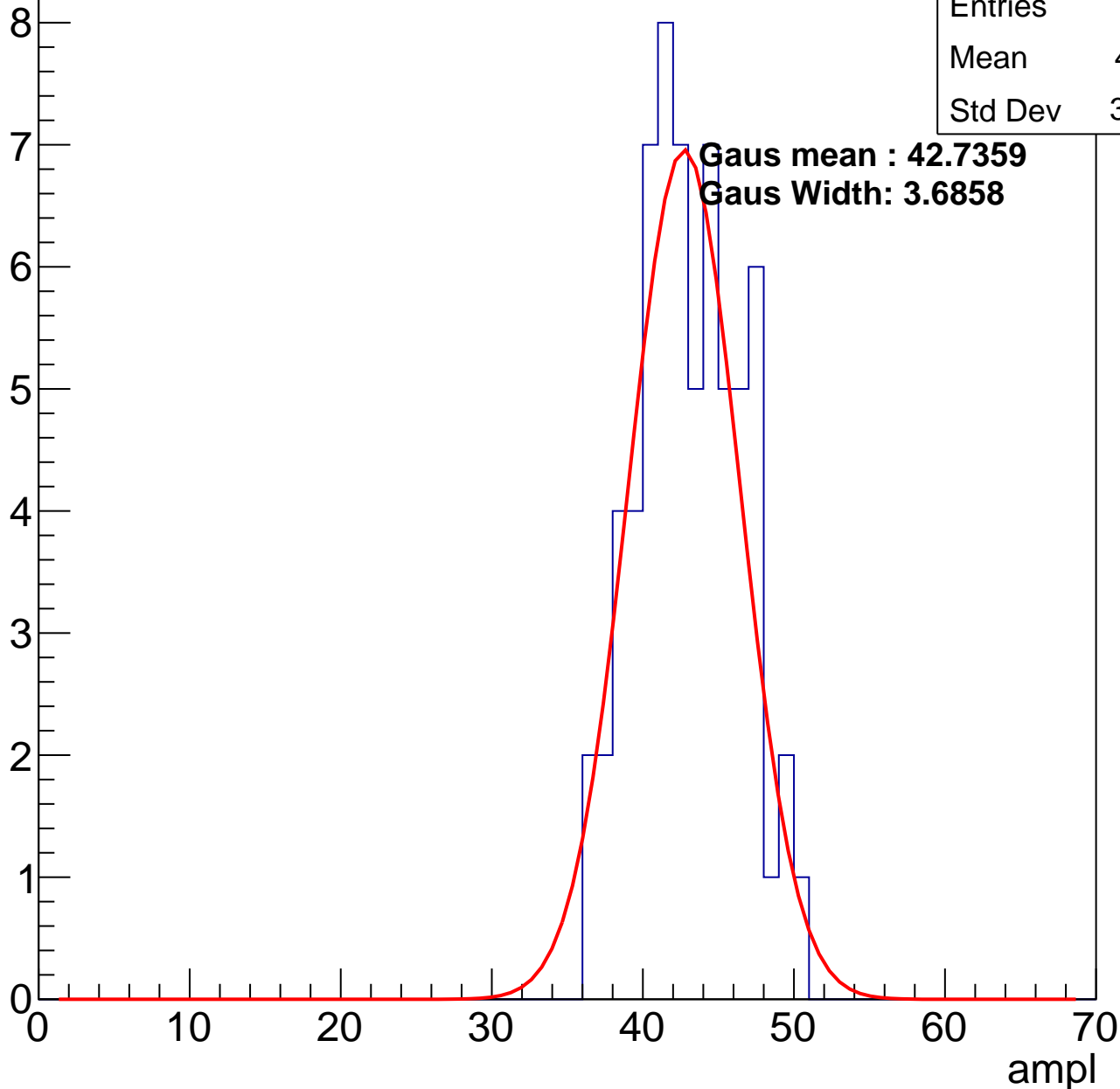
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	42.61
Std Dev	3.348

**Gaus mean : 42.7359**

**Gaus Width: 3.6858**

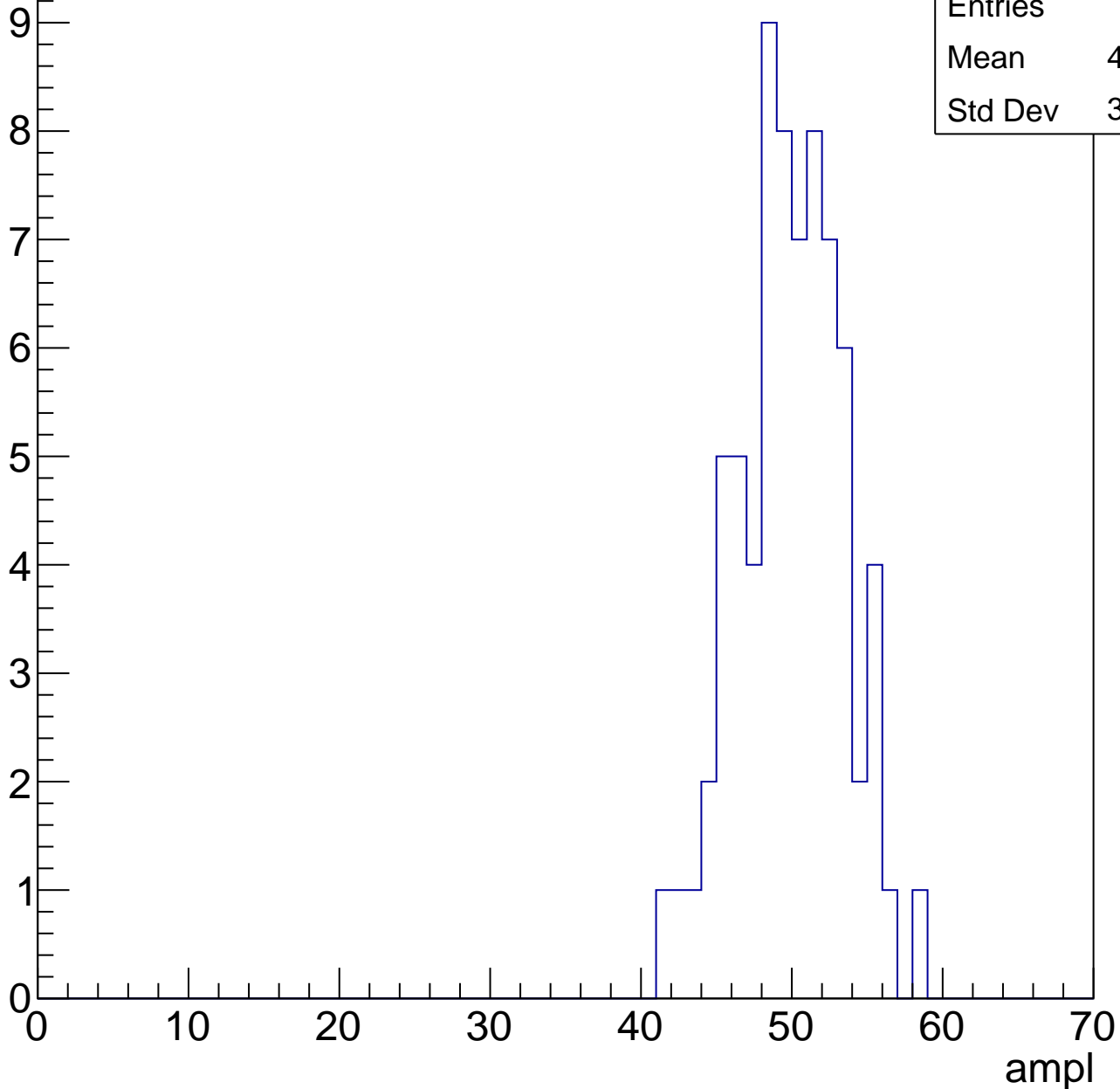


# B1L102S, U12-ch119, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	72
Mean	49.49
Std Dev	3.444

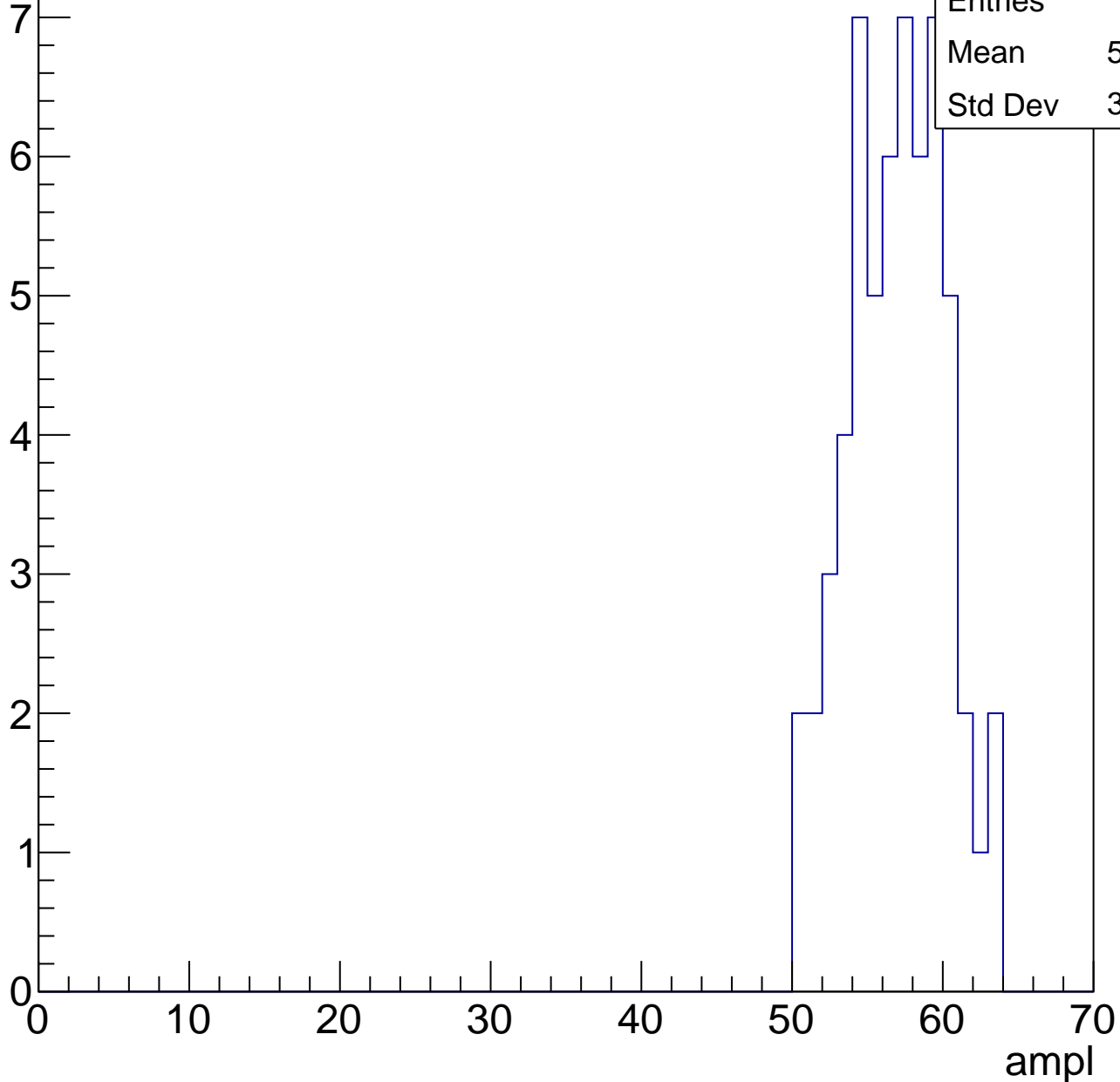


# B1L102S, U12-ch119, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	59
Mean	56.42
Std Dev	3.153

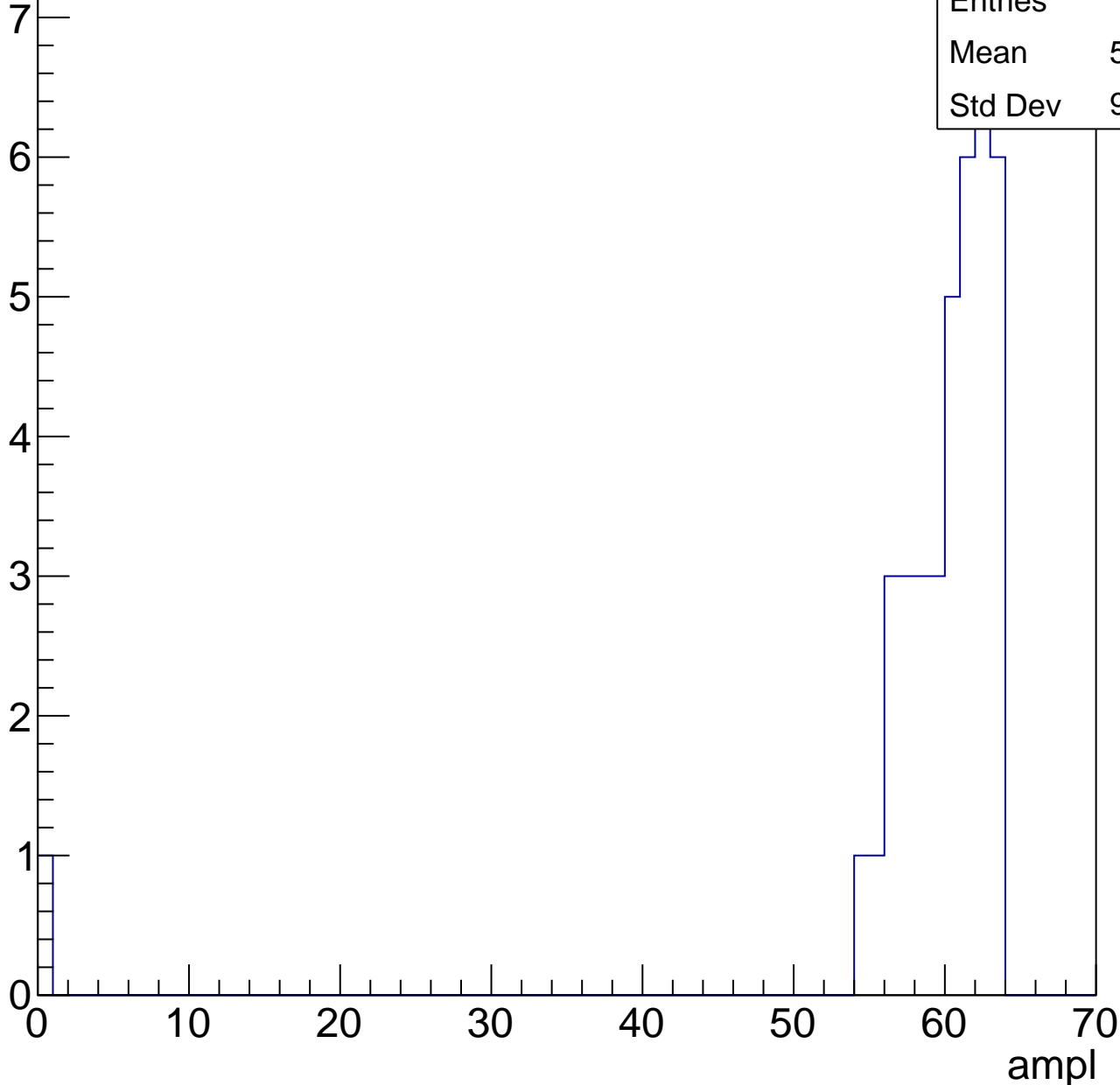


# B1L102S, U12-ch119, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	39
Mean	58.38
Std Dev	9.789



# B1L102S, U12-ch119, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	6
Mean	62
Std Dev	0.8165

ampl



# B1L102S, U12-ch119, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U12-ch120, adc0

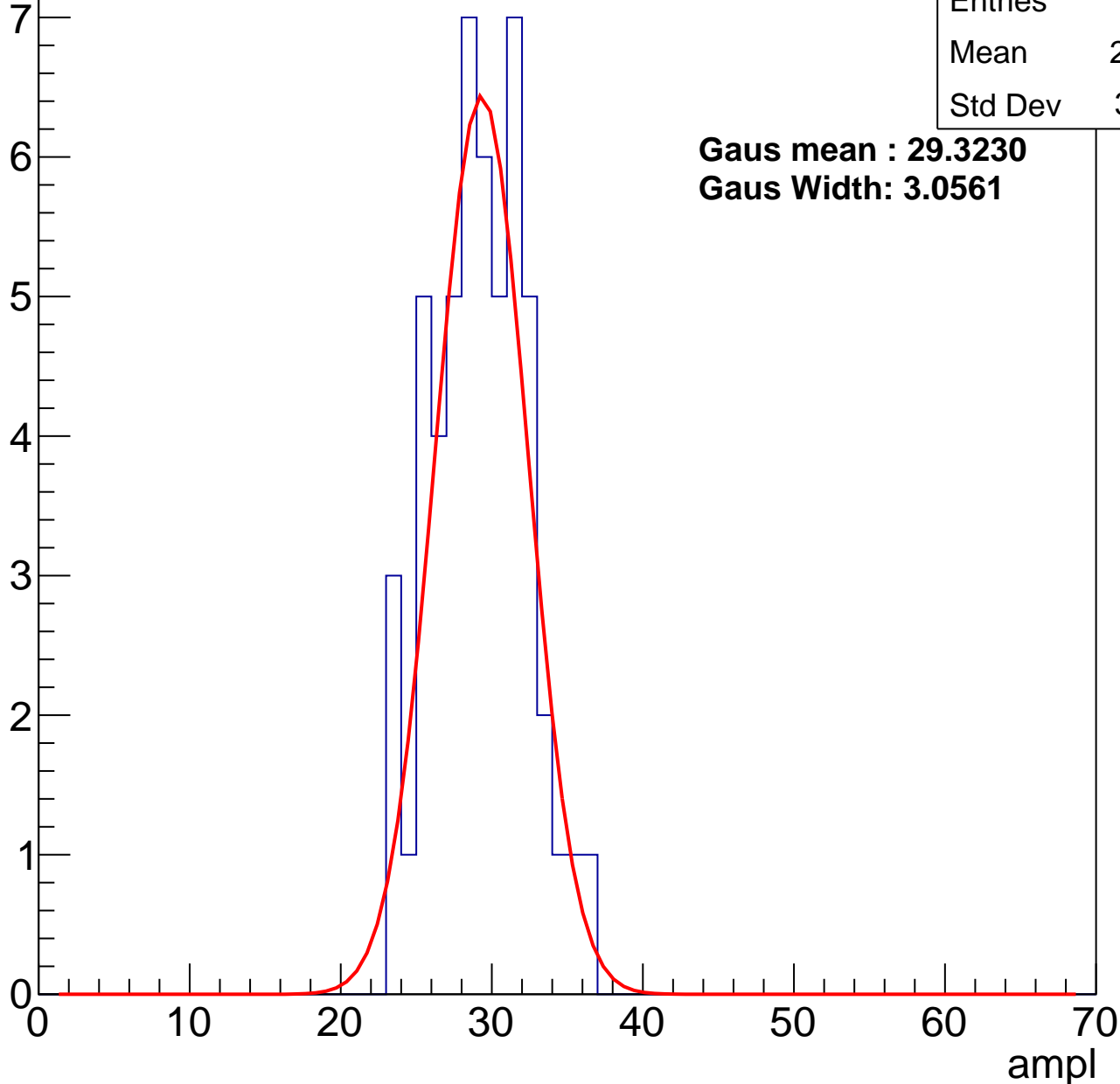
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	53
Mean	28.77
Std Dev	3.051

**Gaus mean : 29.3230**

**Gaus Width: 3.0561**



# B1L102S, U12-ch120, adc1

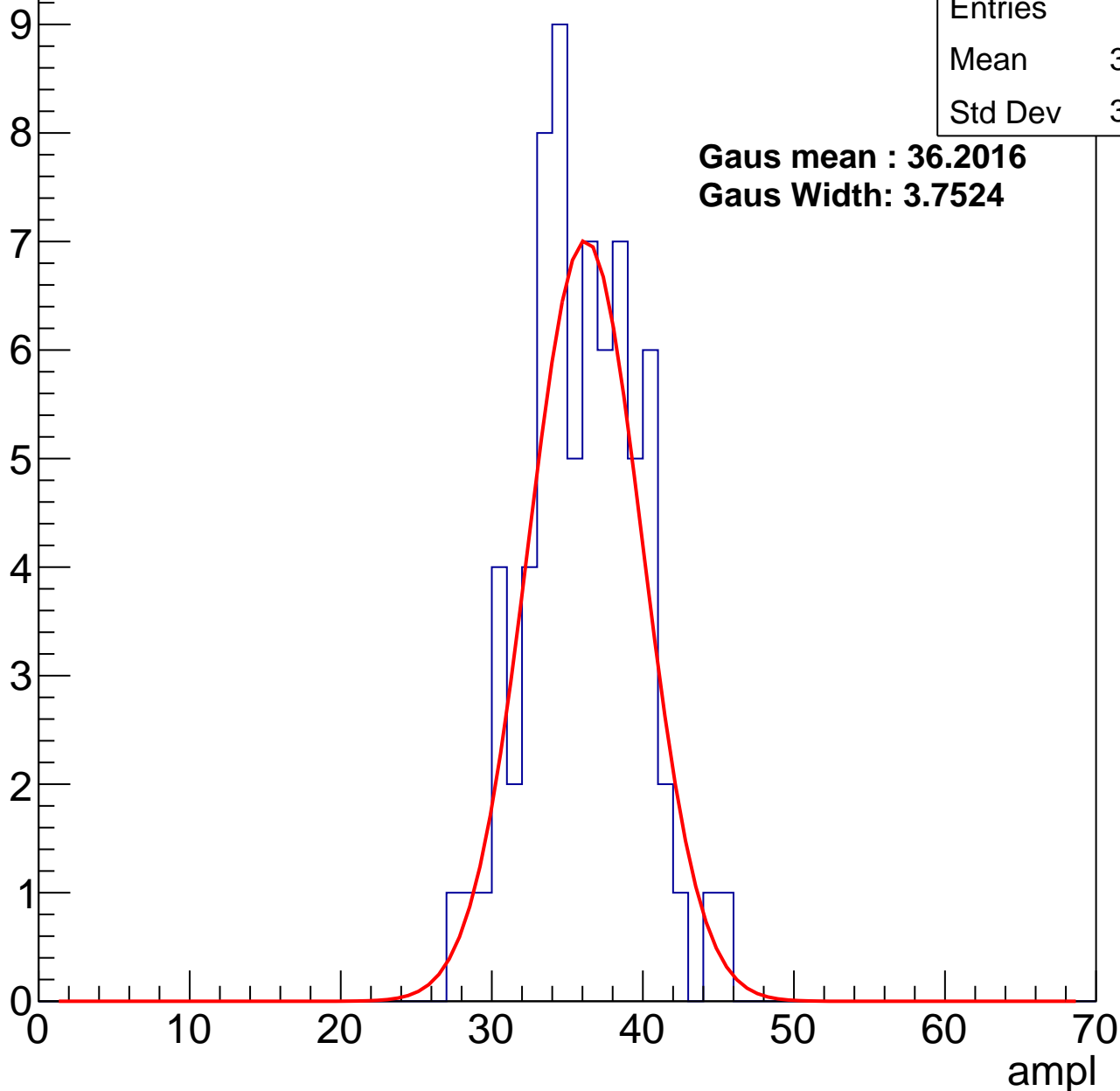
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	71
Mean	35.59
Std Dev	3.675

**Gaus mean : 36.2016**

**Gaus Width: 3.7524**



# B1L102S, U12-ch120, adc2

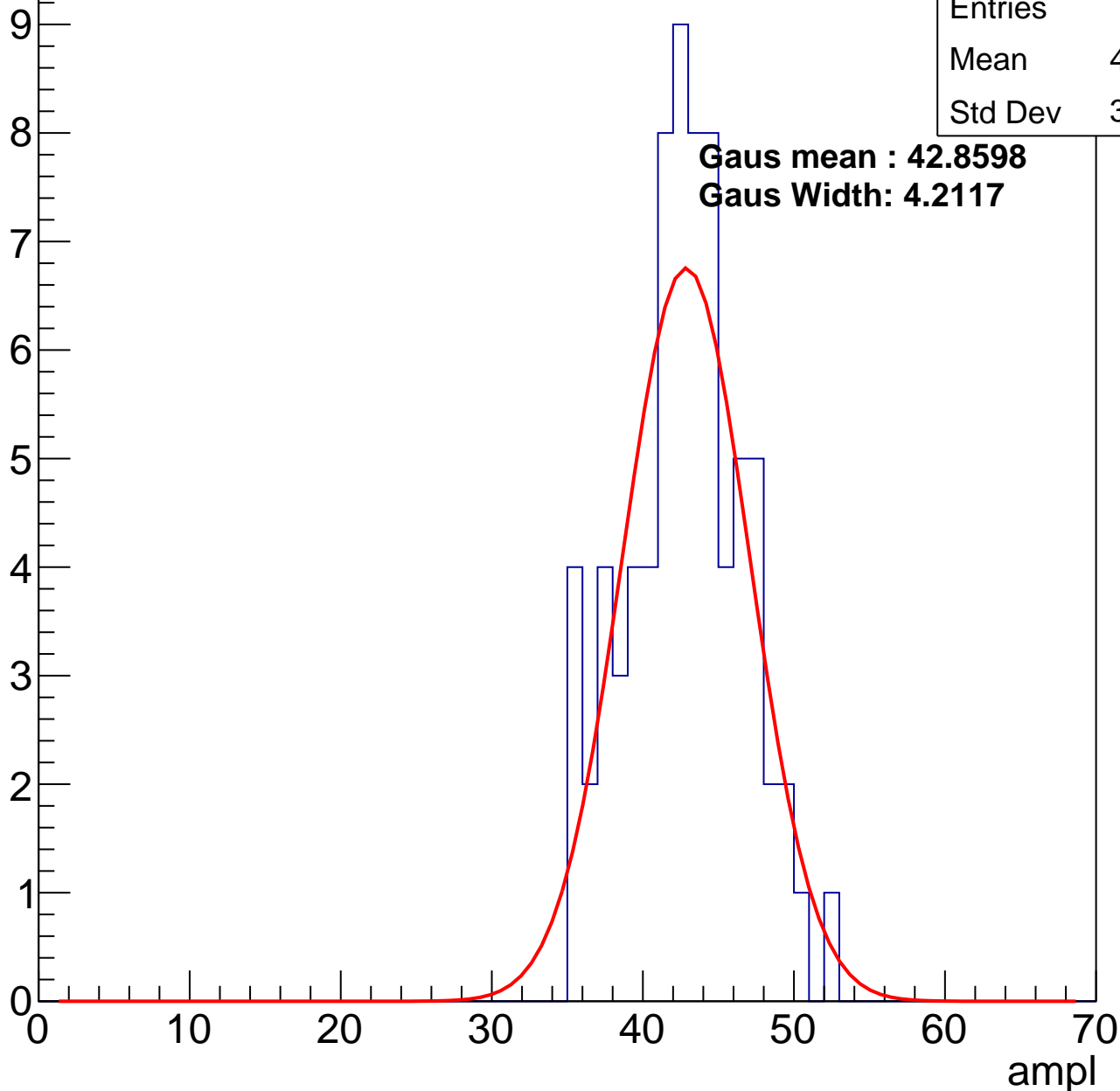
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	74
Mean	42.34
Std Dev	3.825

**Gaus mean : 42.8598**

**Gaus Width: 4.2117**

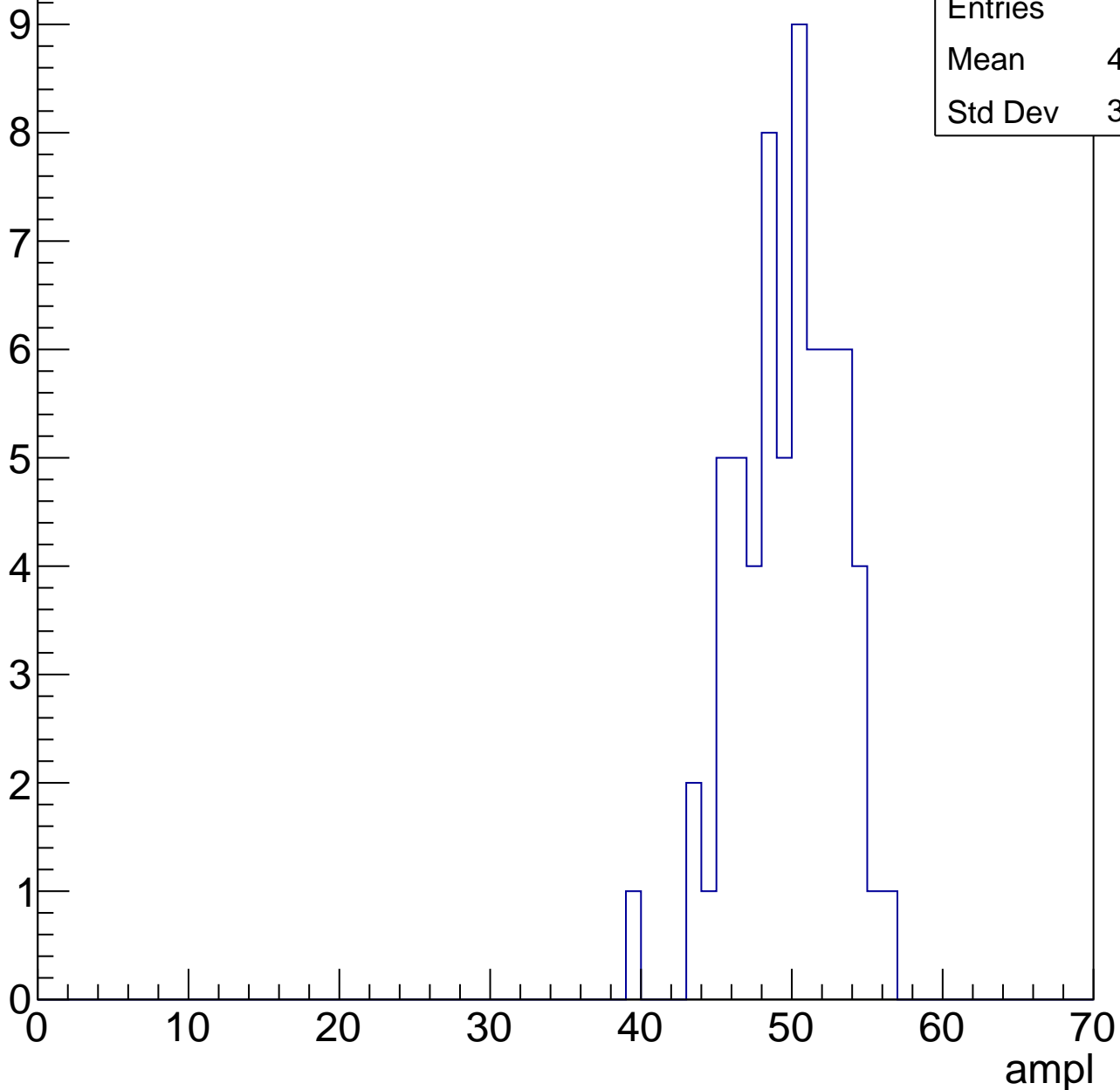


# B1L102S, U12-ch120, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	49.28
Std Dev	3.328

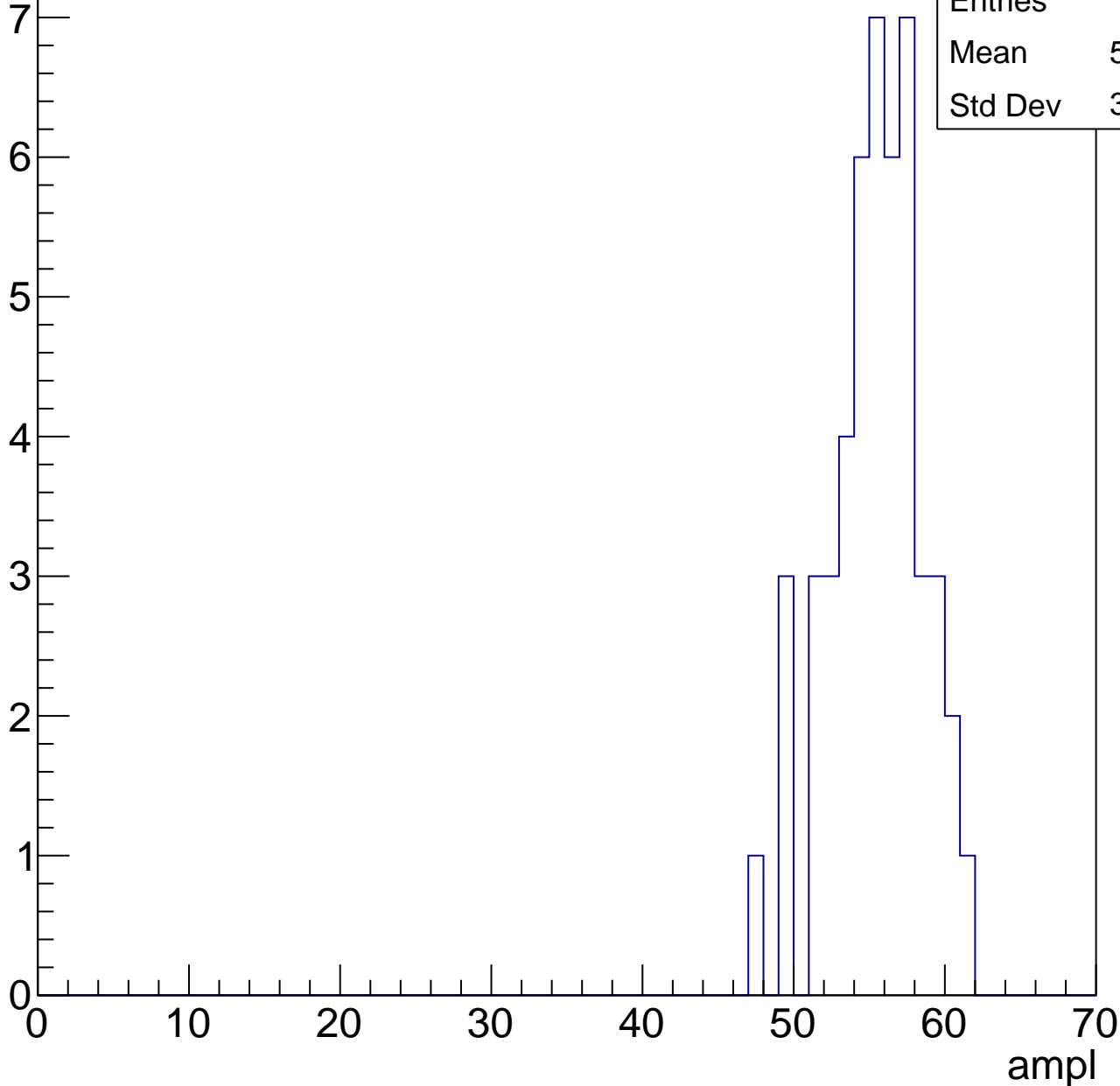


# B1L102S, U12-ch120, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	49
Mean	54.92
Std Dev	3.076

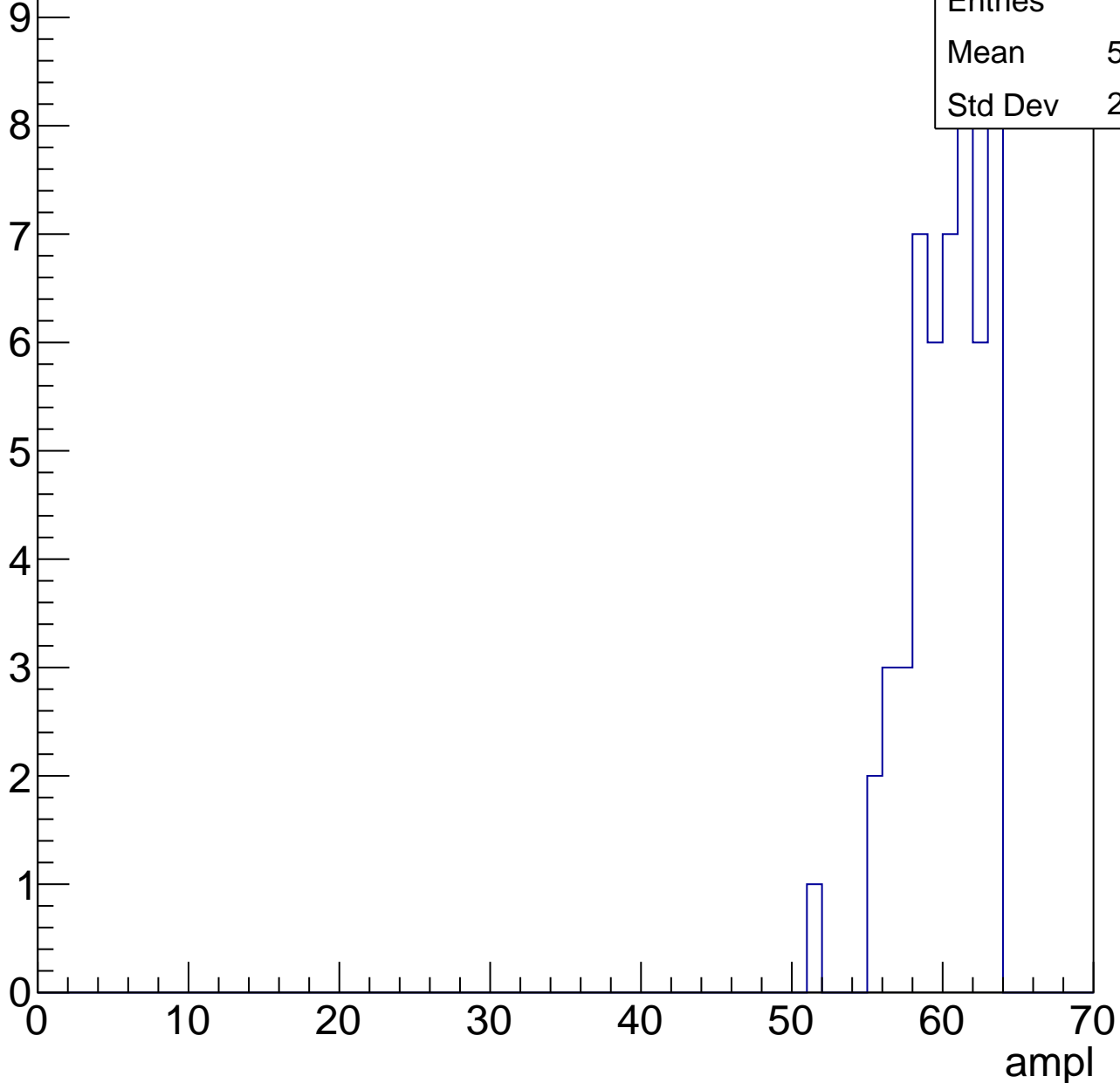


# B1L102S, U12-ch120, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

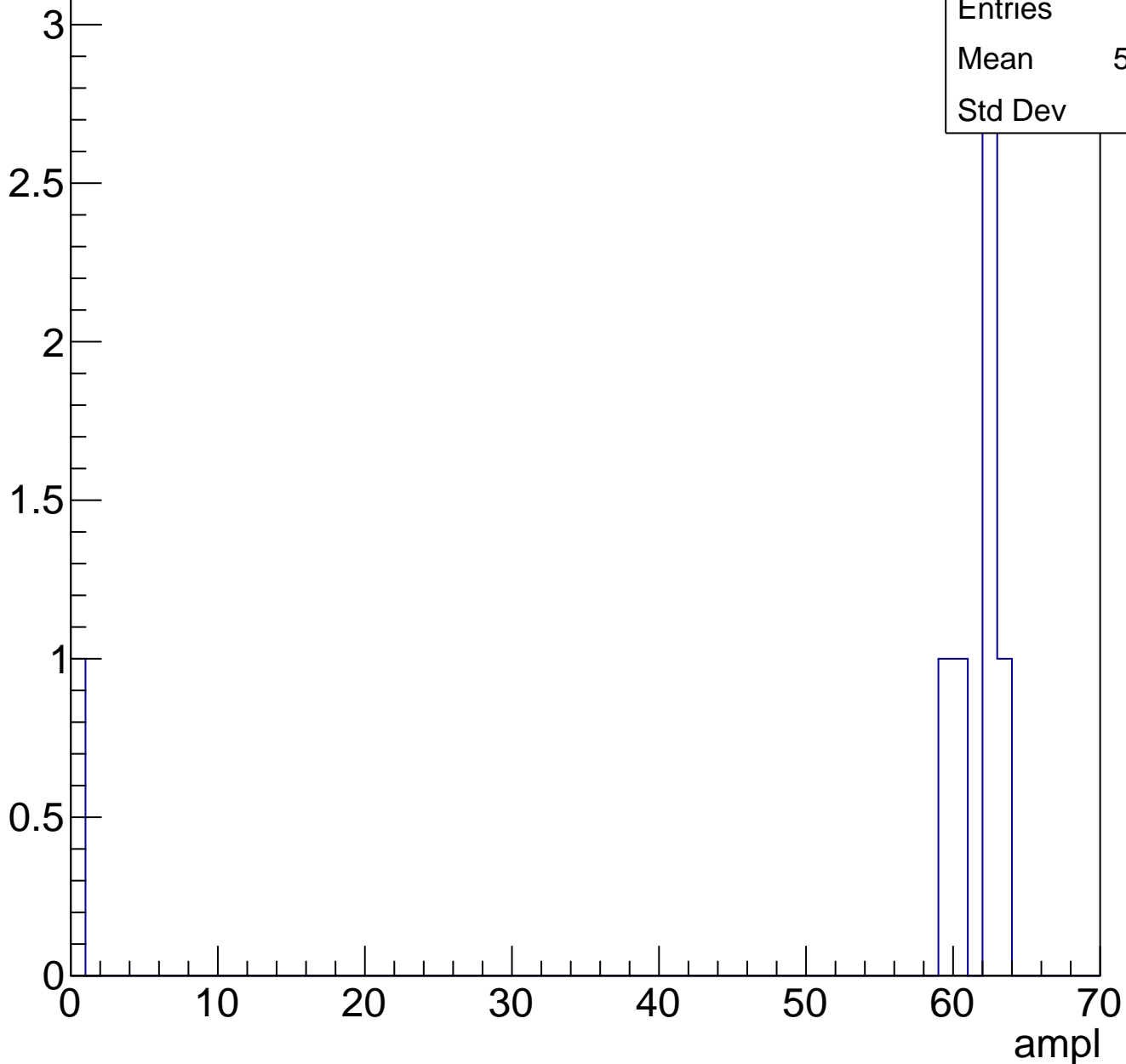
Entries	53
Mean	59.77
Std Dev	2.574



# B1L102S, U12-ch120, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



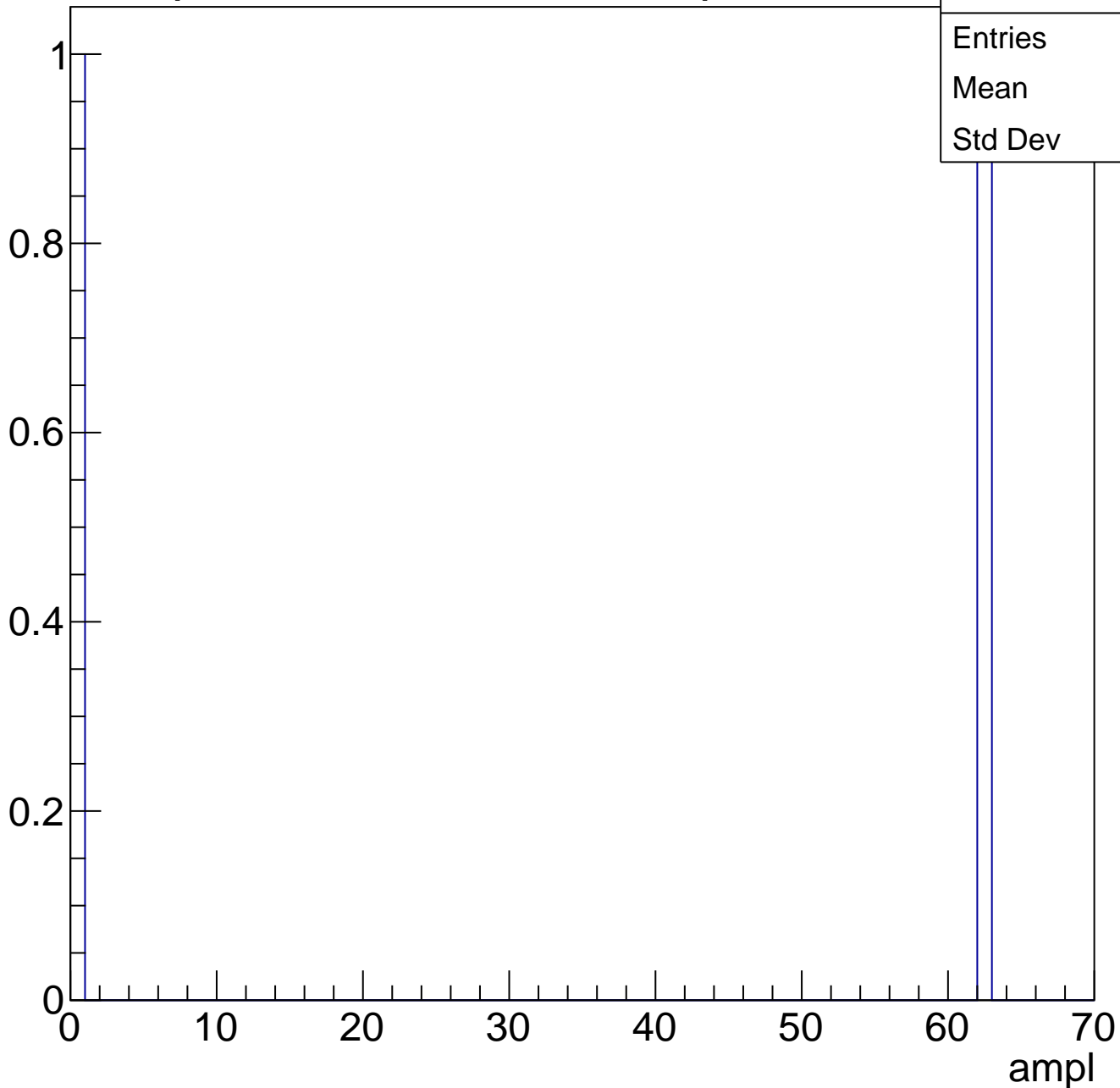
Entries	7
Mean	52.57
Std Dev	21.5



# B1L102S, U12-ch120, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U12-ch121, adc0

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	74
Mean	30.04
Std Dev	5.039

**Gaus mean : 31.3203**

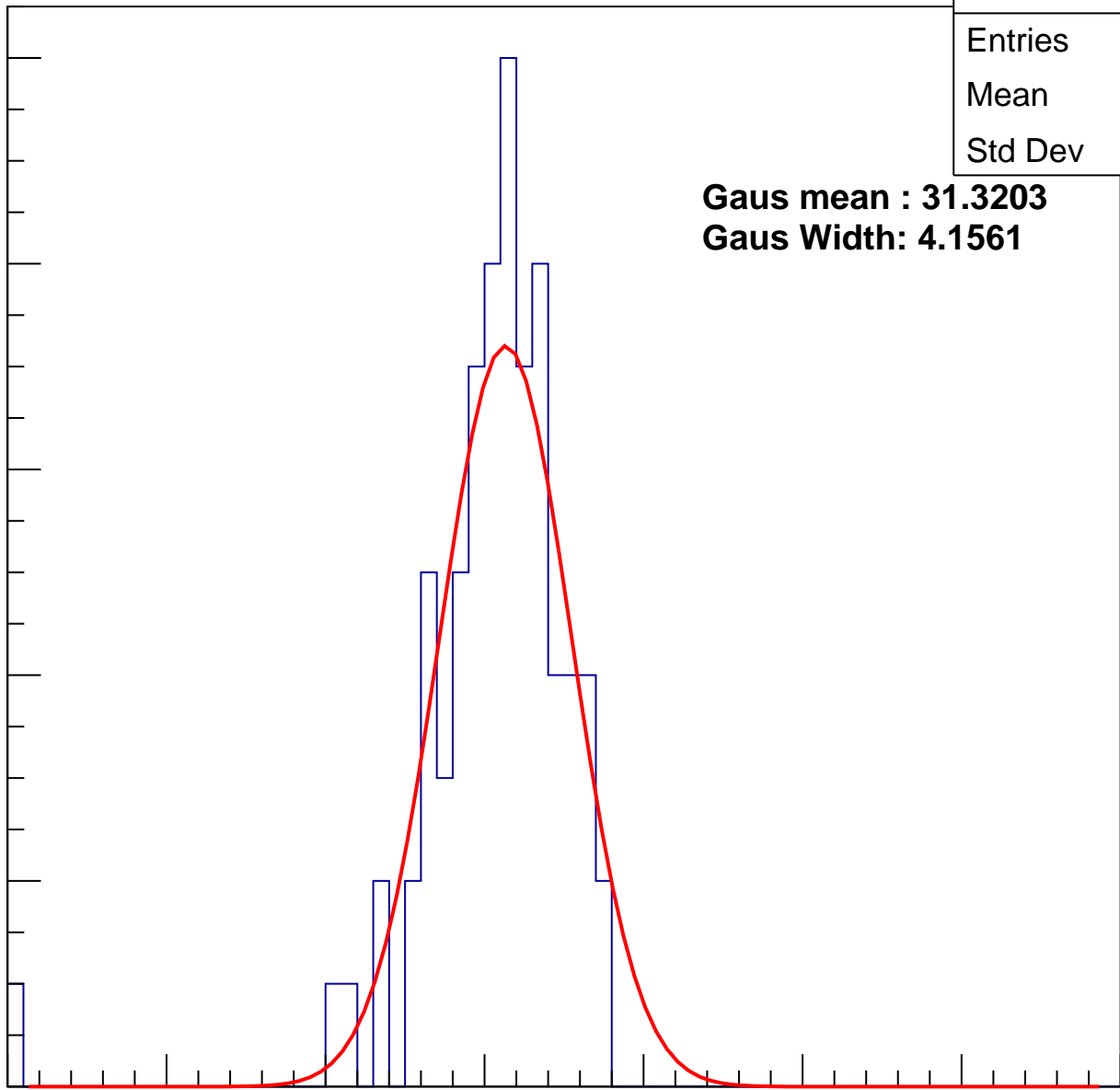
**Gaus Width: 4.1561**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L102S, U12-ch121, adc1

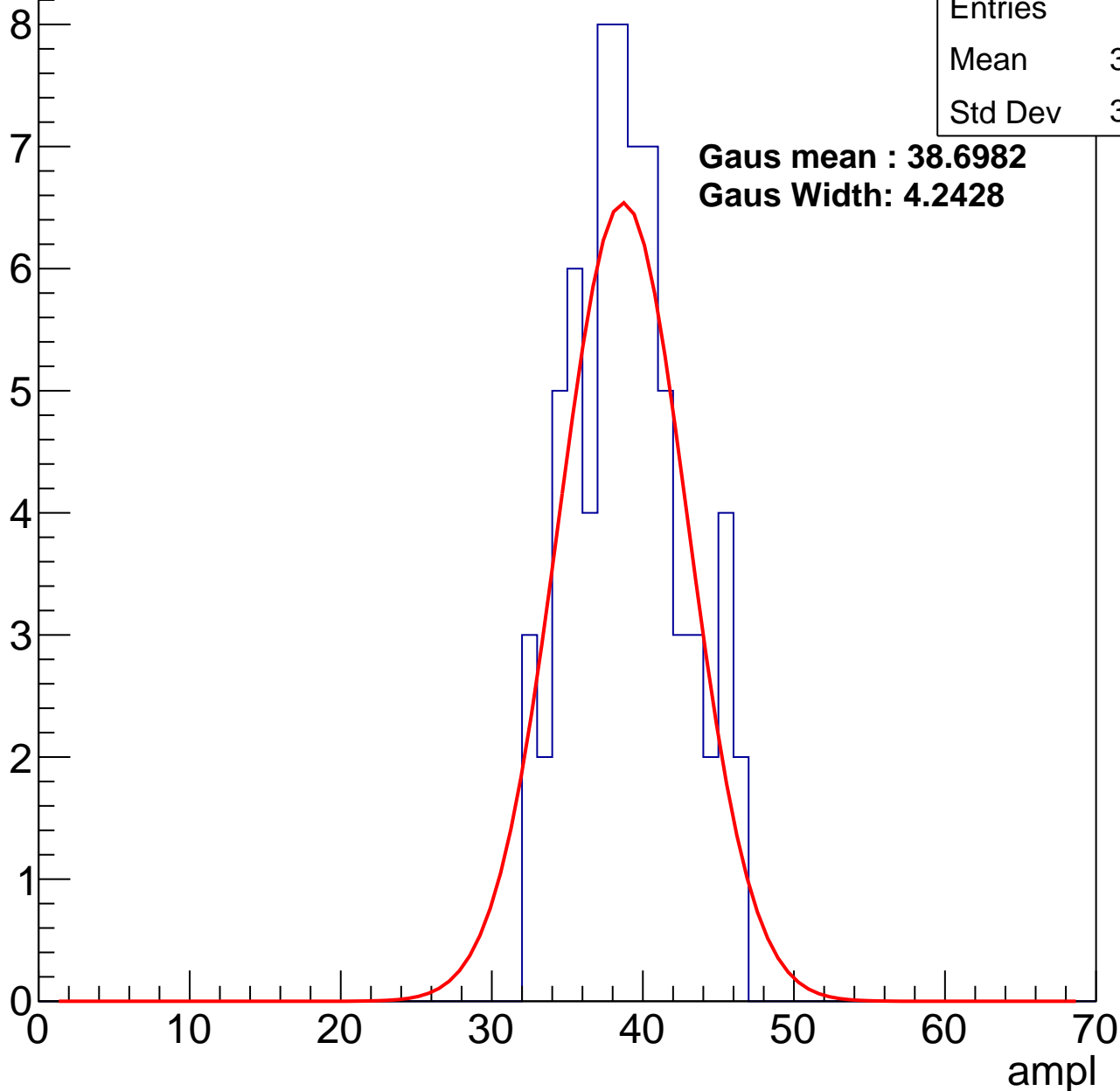
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	38.54
Std Dev	3.602

**Gaus mean : 38.6982**

**Gaus Width: 4.2428**



# B1L102S, U12-ch121, adc2

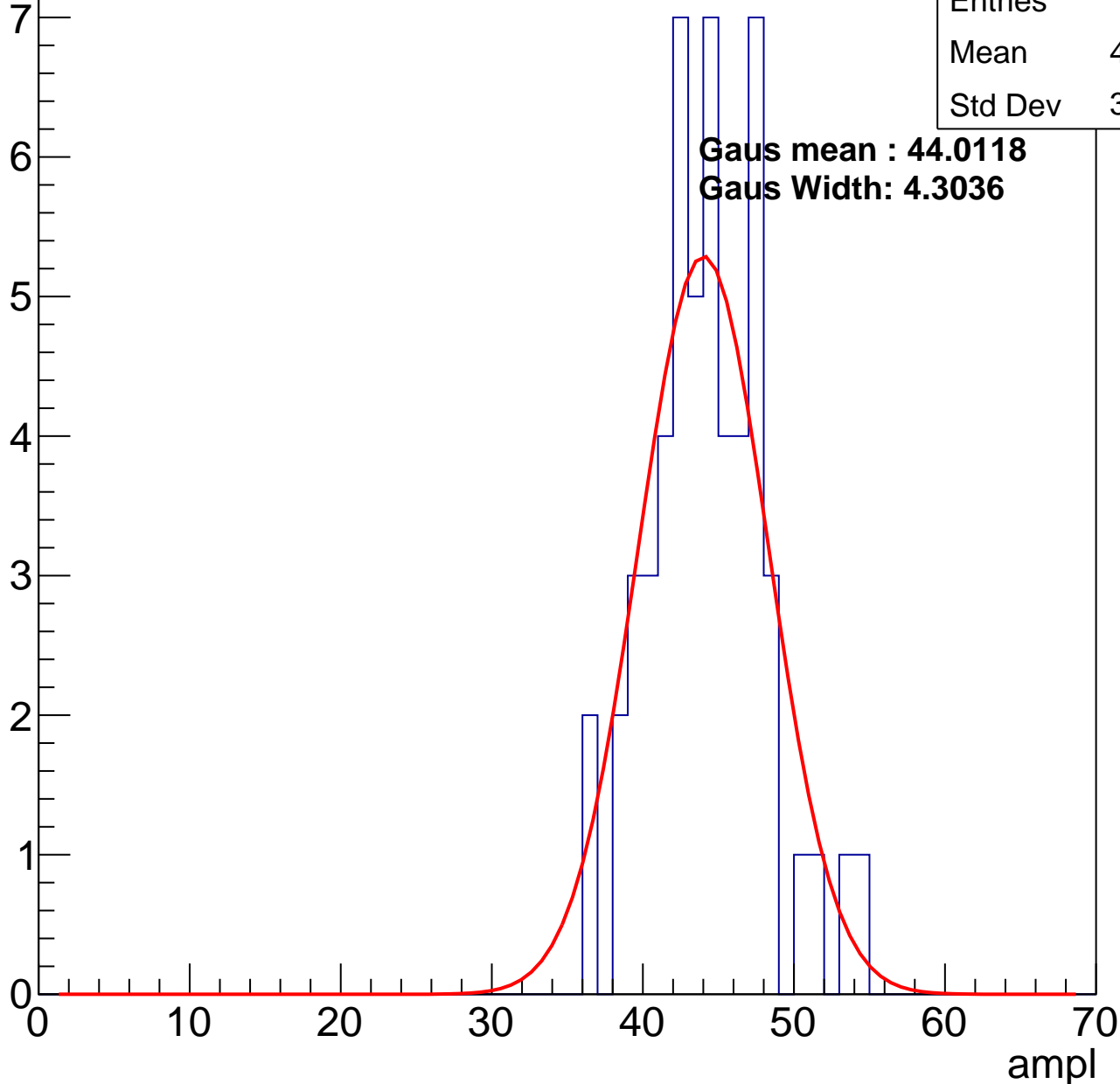
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	55
Mean	43.84
Std Dev	3.784

**Gaus mean : 44.0118**

**Gaus Width: 4.3036**

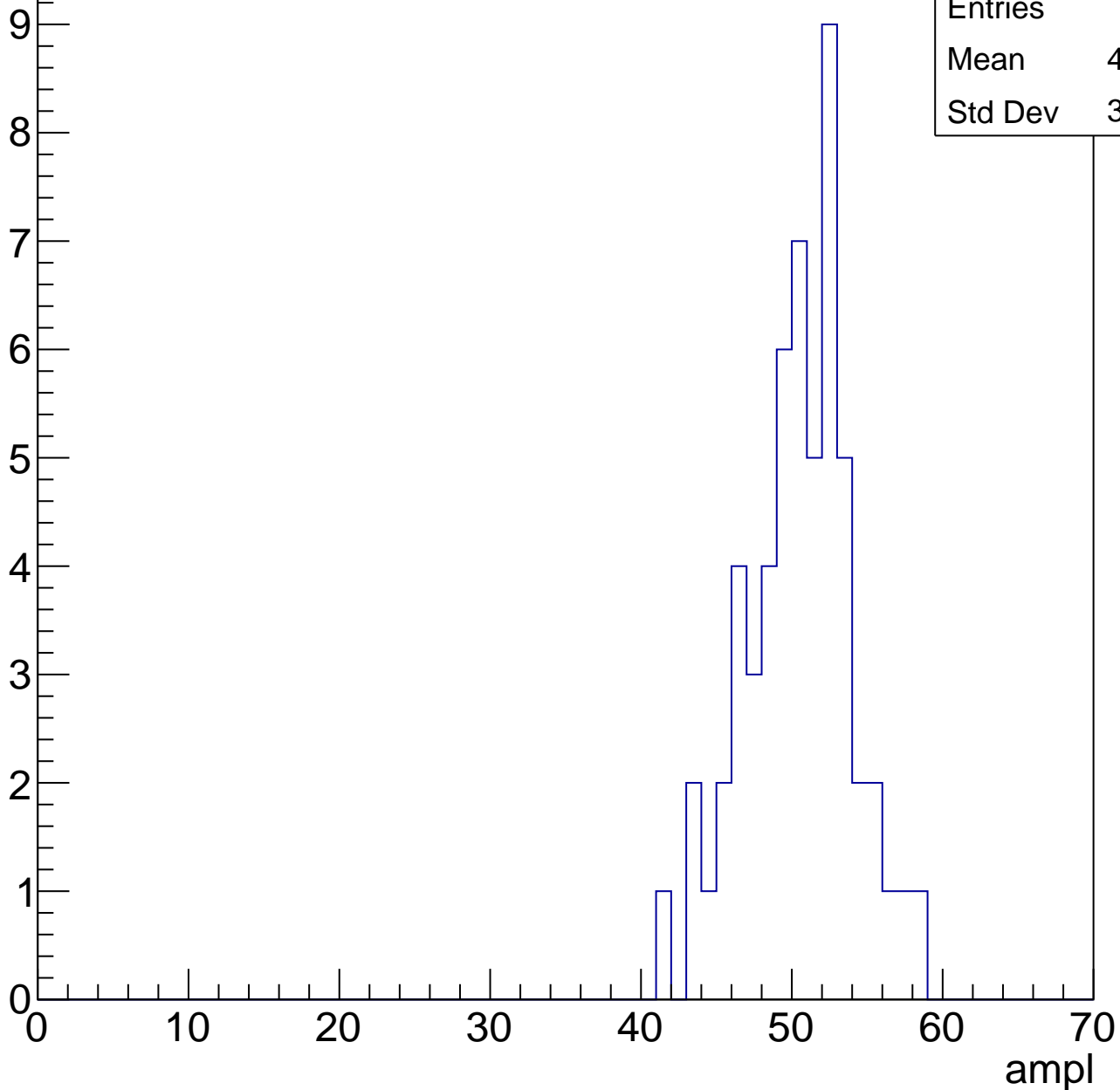


# B1L102S, U12-ch121, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	56
Mean	49.98
Std Dev	3.523

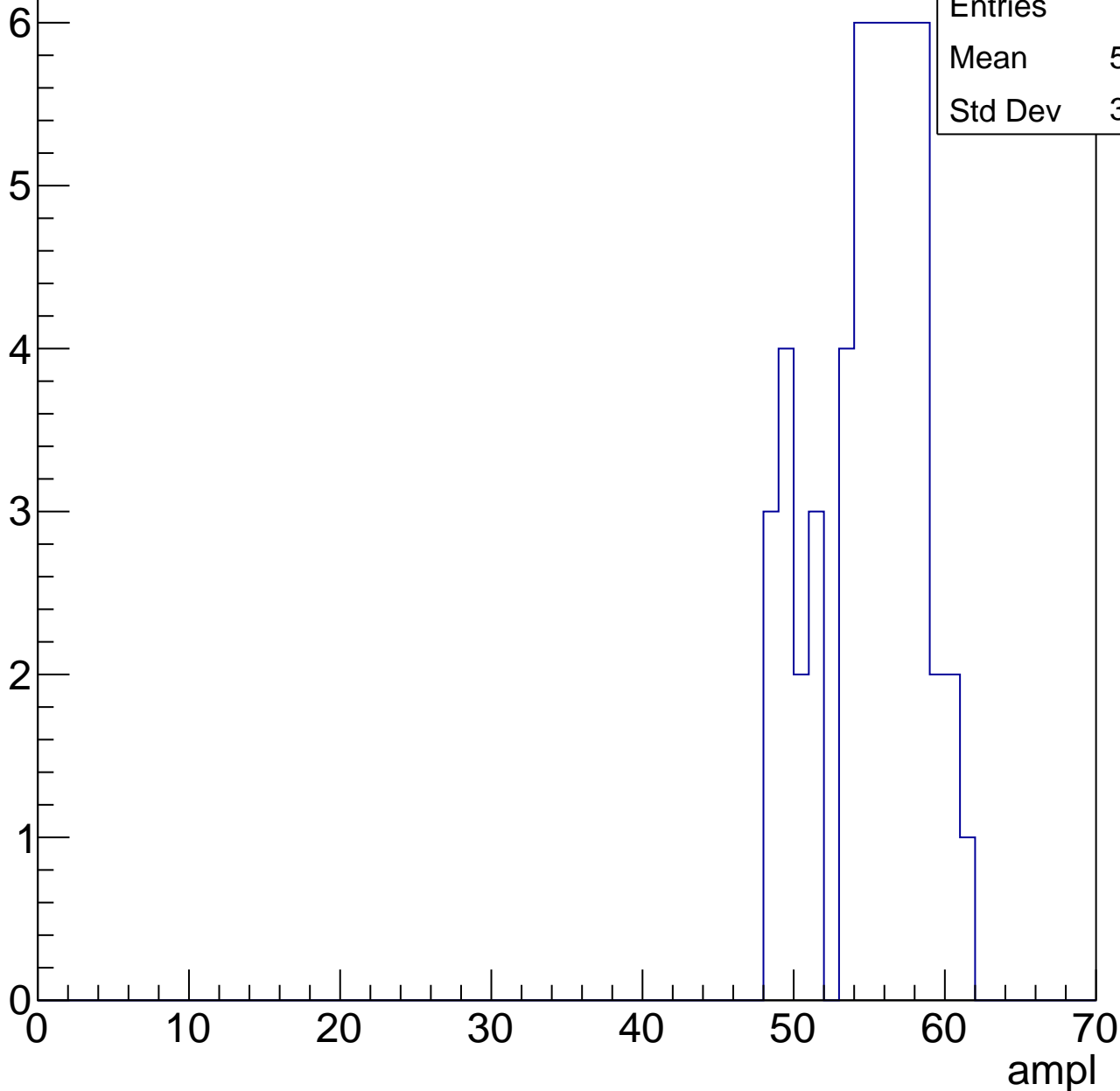


# B1L102S, U12-ch121, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	51
Mean	54.59
Std Dev	3.442



# B1L102S, U12-ch121, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	56
Mean	58.64
Std Dev	8.391

Entry

10

8

6

4

2

0

ampl

0

10

20

30

40

50

60

70

# B1L102S, U12-ch121, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

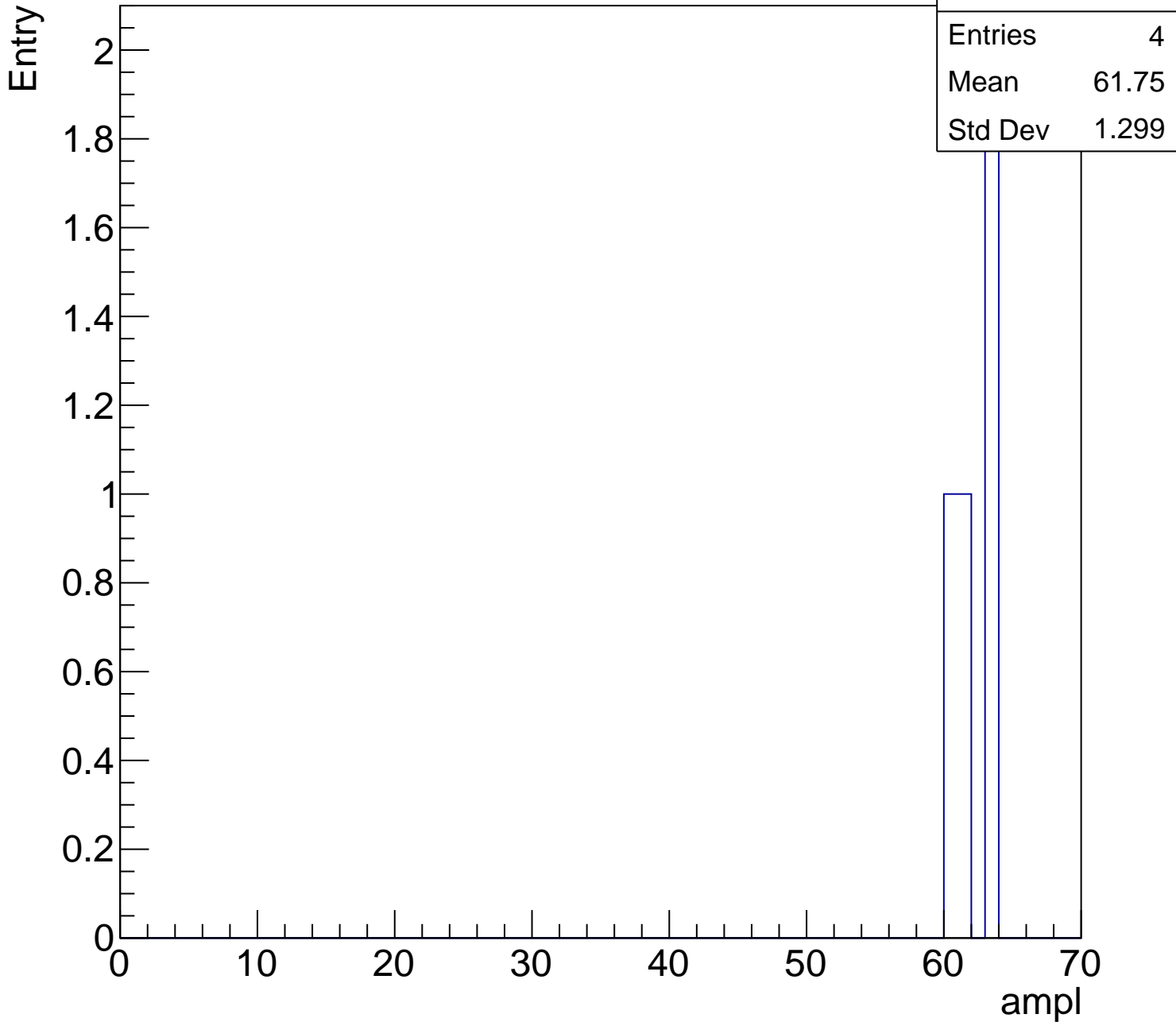
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	4
Mean	61.75
Std Dev	1.299

ampl

0 10 20 30 40 50 60 70





# B1L102S, U12-ch121, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U12-ch122, adc0

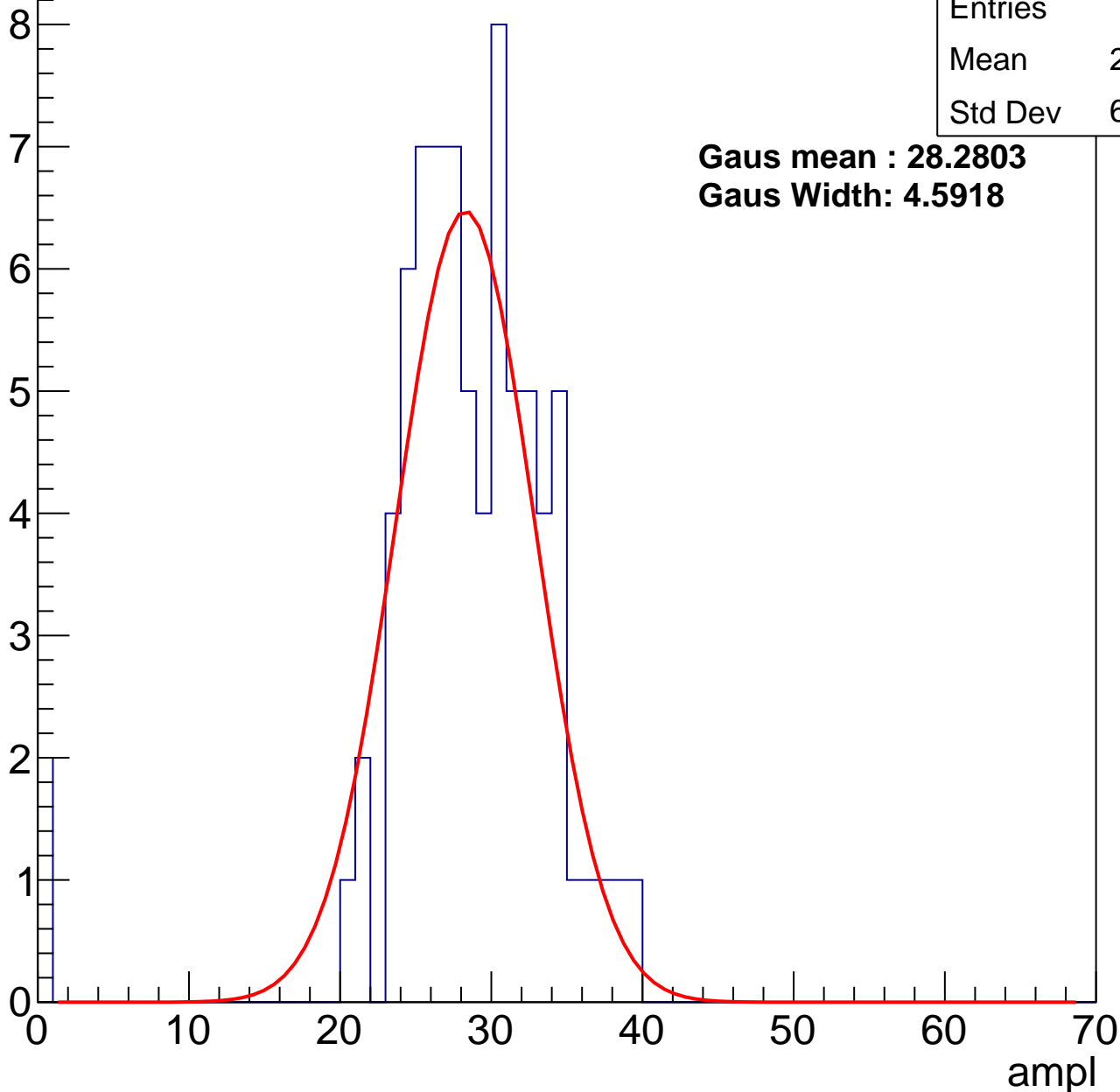
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	77
Mean	27.82
Std Dev	6.113

**Gaus mean : 28.2803**

**Gaus Width: 4.5918**



# B1L102S, U12-ch122, adc1

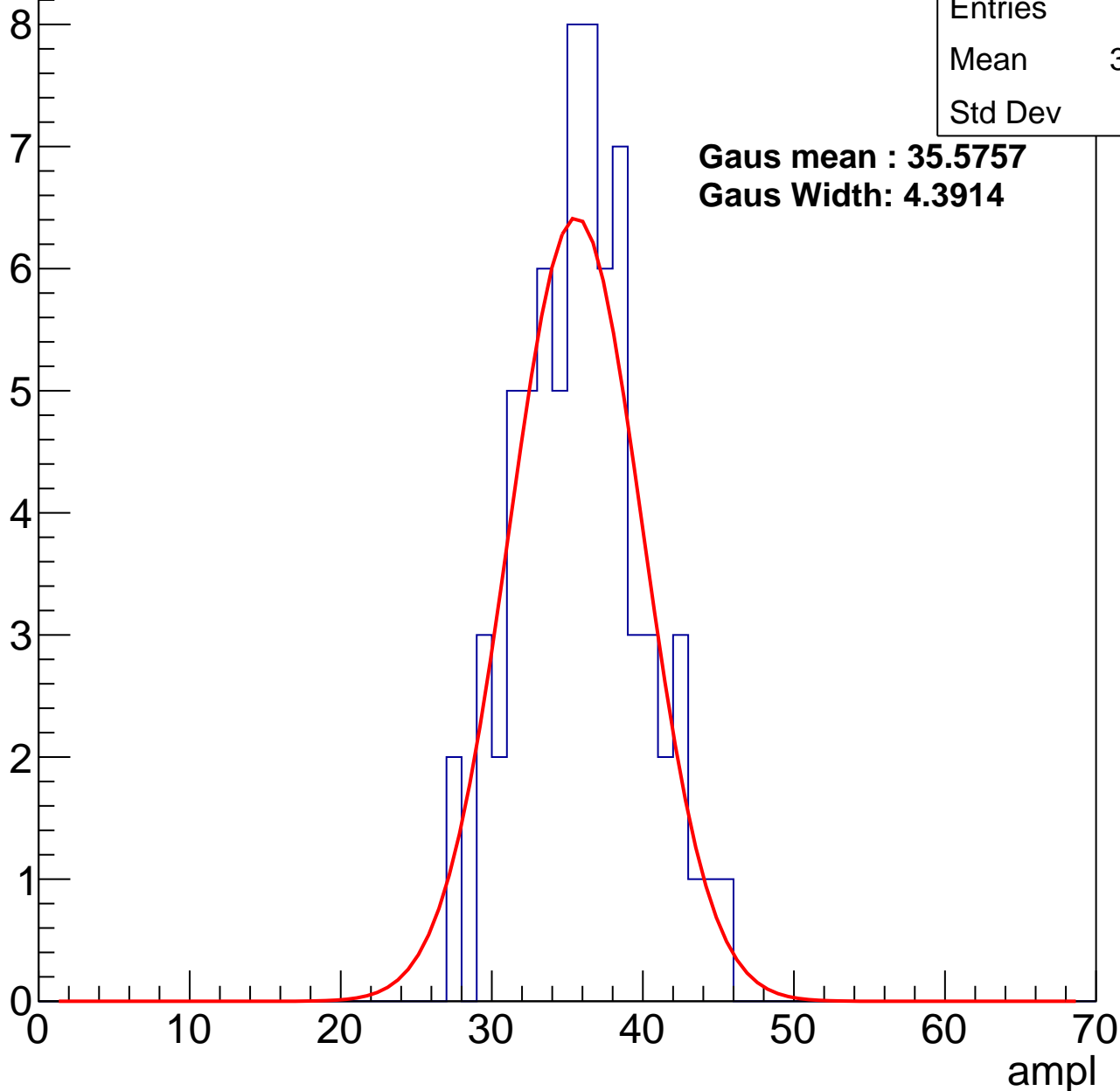
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	71
Mean	35.45
Std Dev	3.95

**Gaus mean : 35.5757**

**Gaus Width: 4.3914**



# B1L102S, U12-ch122, adc2

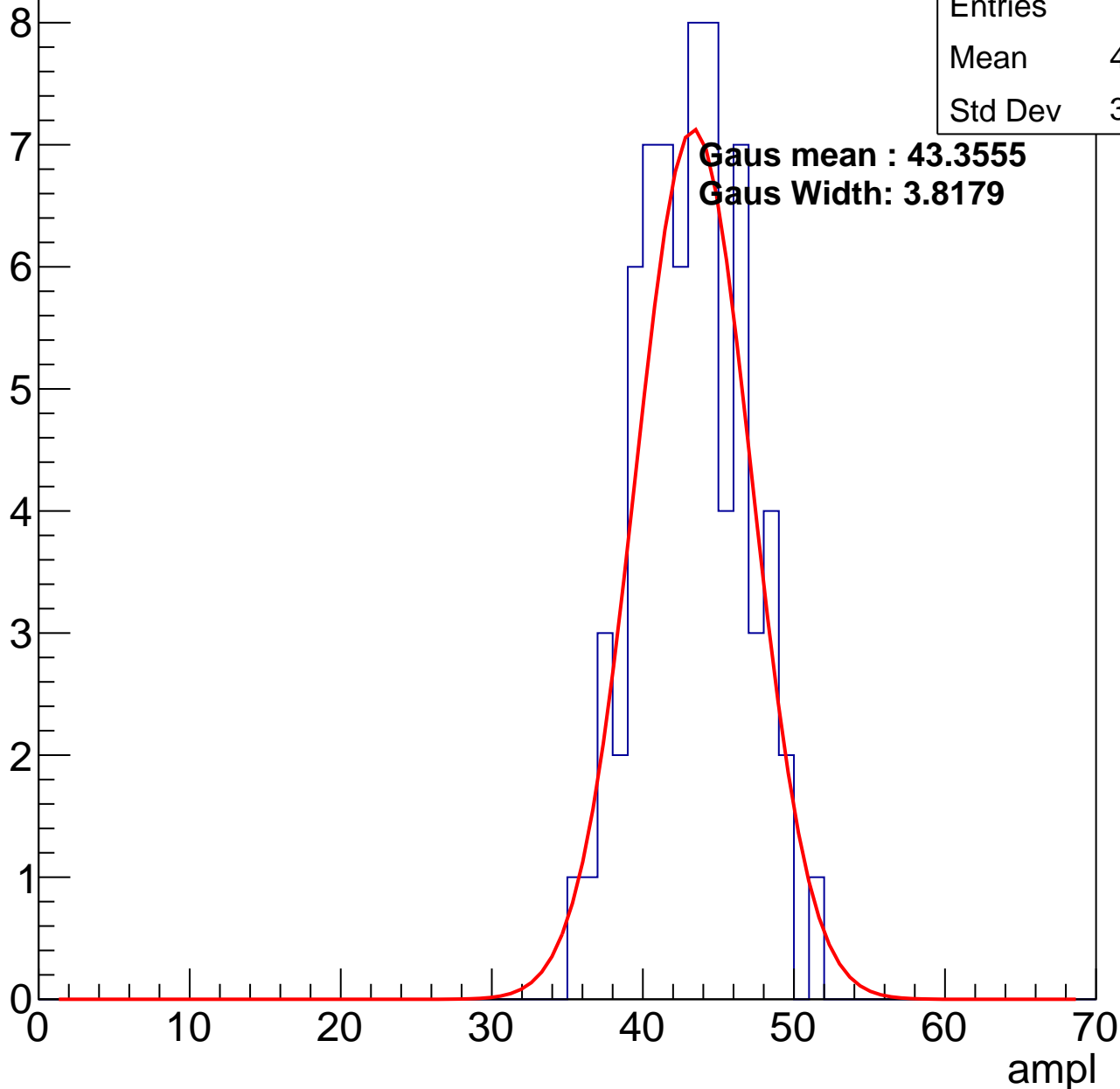
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	70
Mean	42.73
Std Dev	3.443

**Gaus mean : 43.3555**

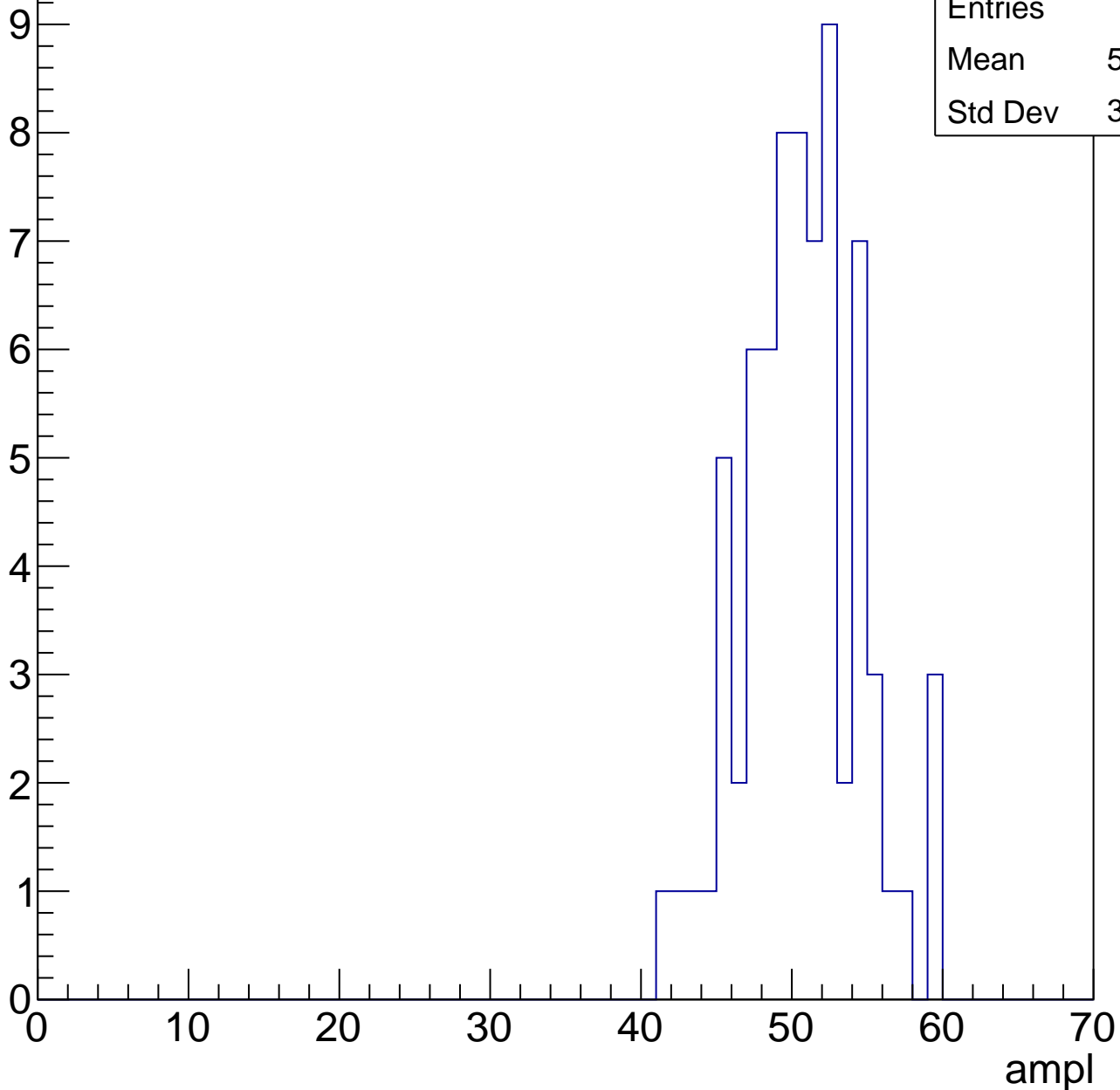
**Gaus Width: 3.8179**



# B1L102S, U12-ch122, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

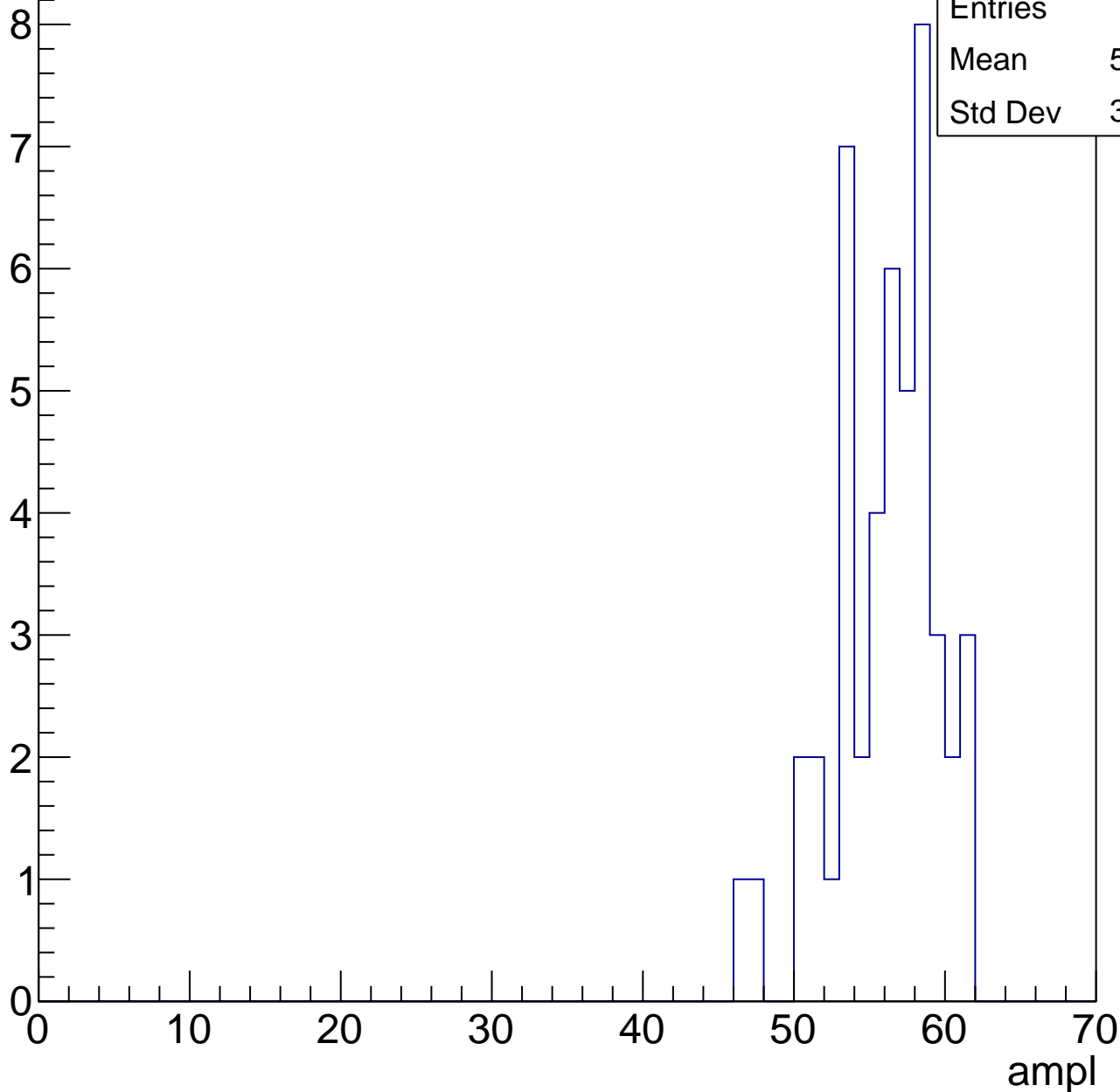


# B1L102S, U12-ch122, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	47
Mean	55.55
Std Dev	3.438

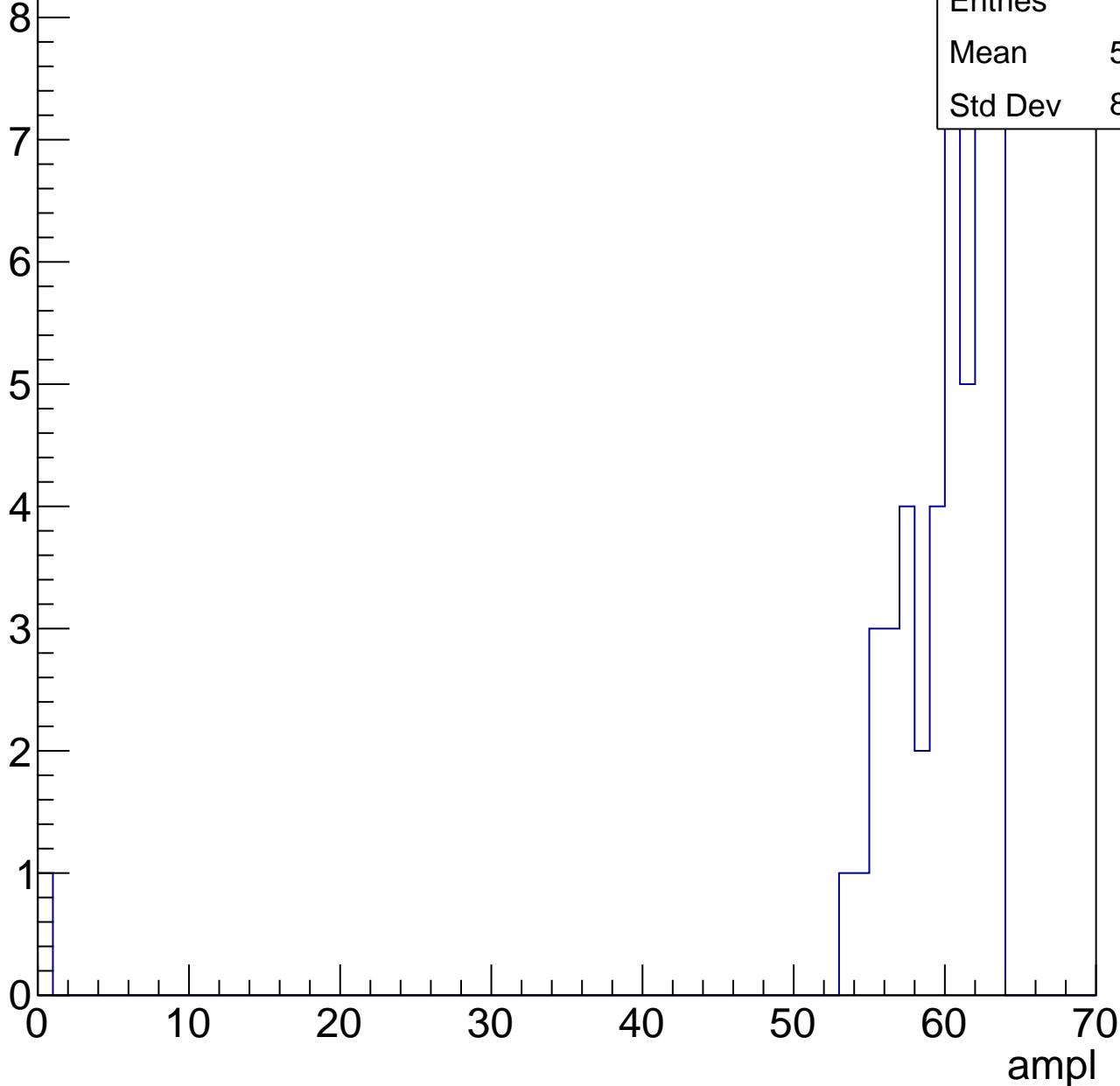


# B1L102S, U12-ch122, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	48
Mean	58.44
Std Dev	8.953



# B1L102S, U12-ch122, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	6
Mean	62
Std Dev	0.8165

ampl



# B1L102S, U12-ch122, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

1

0.8

0.6

0.4

0.2

0

0

10

20

30

40

50

60

70

ampl

Entries

0

Mean

0

Std Dev

0

# B1L102S, U12-ch123, adc0

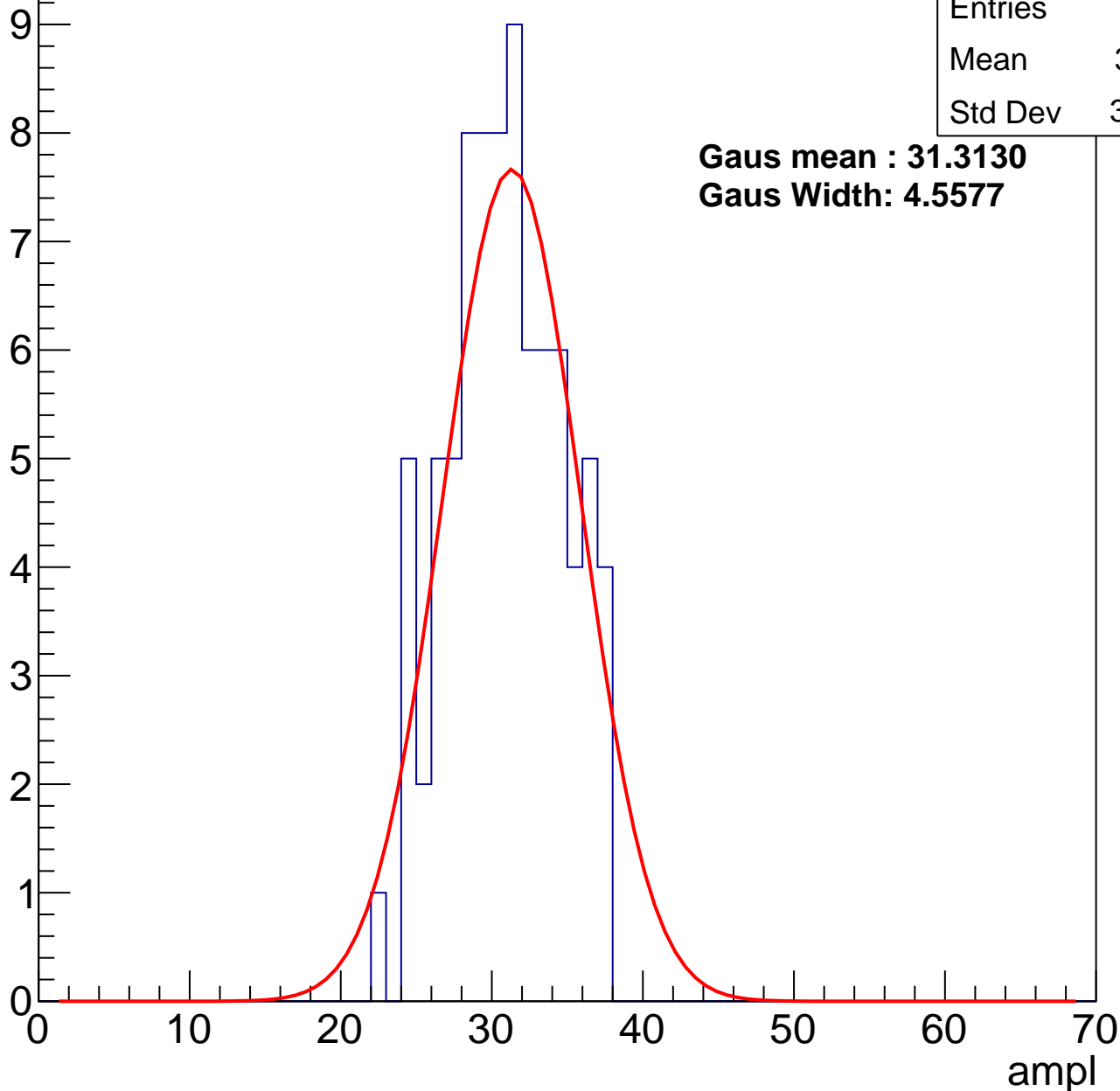
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	82
Mean	30.41
Std Dev	3.669

**Gaus mean : 31.3130**

**Gaus Width: 4.5577**



# B1L102S, U12-ch123, adc1

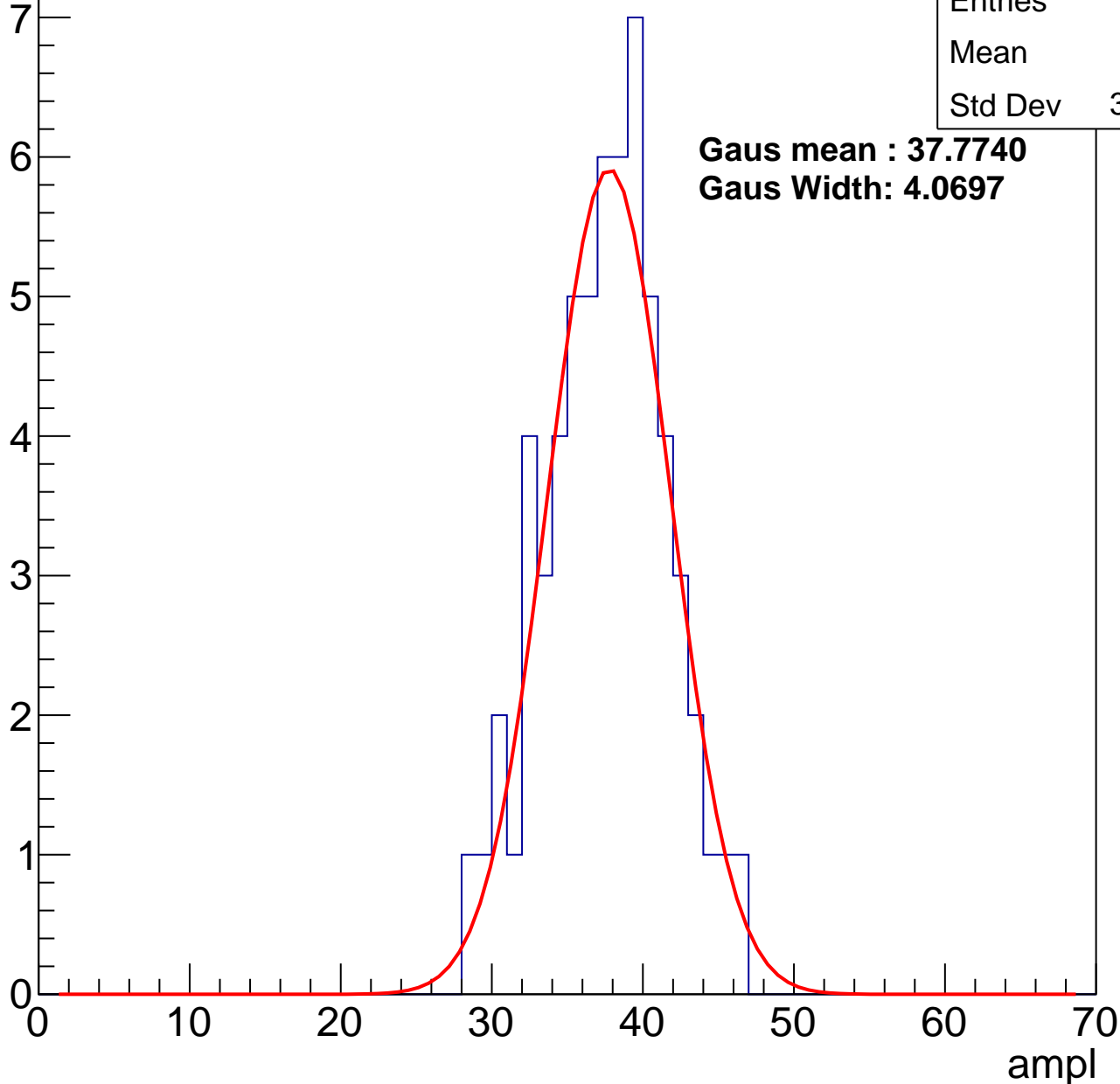
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	62
Mean	37.1
Std Dev	3.958

**Gaus mean : 37.7740**

**Gaus Width: 4.0697**



# B1L102S, U12-ch123, adc2

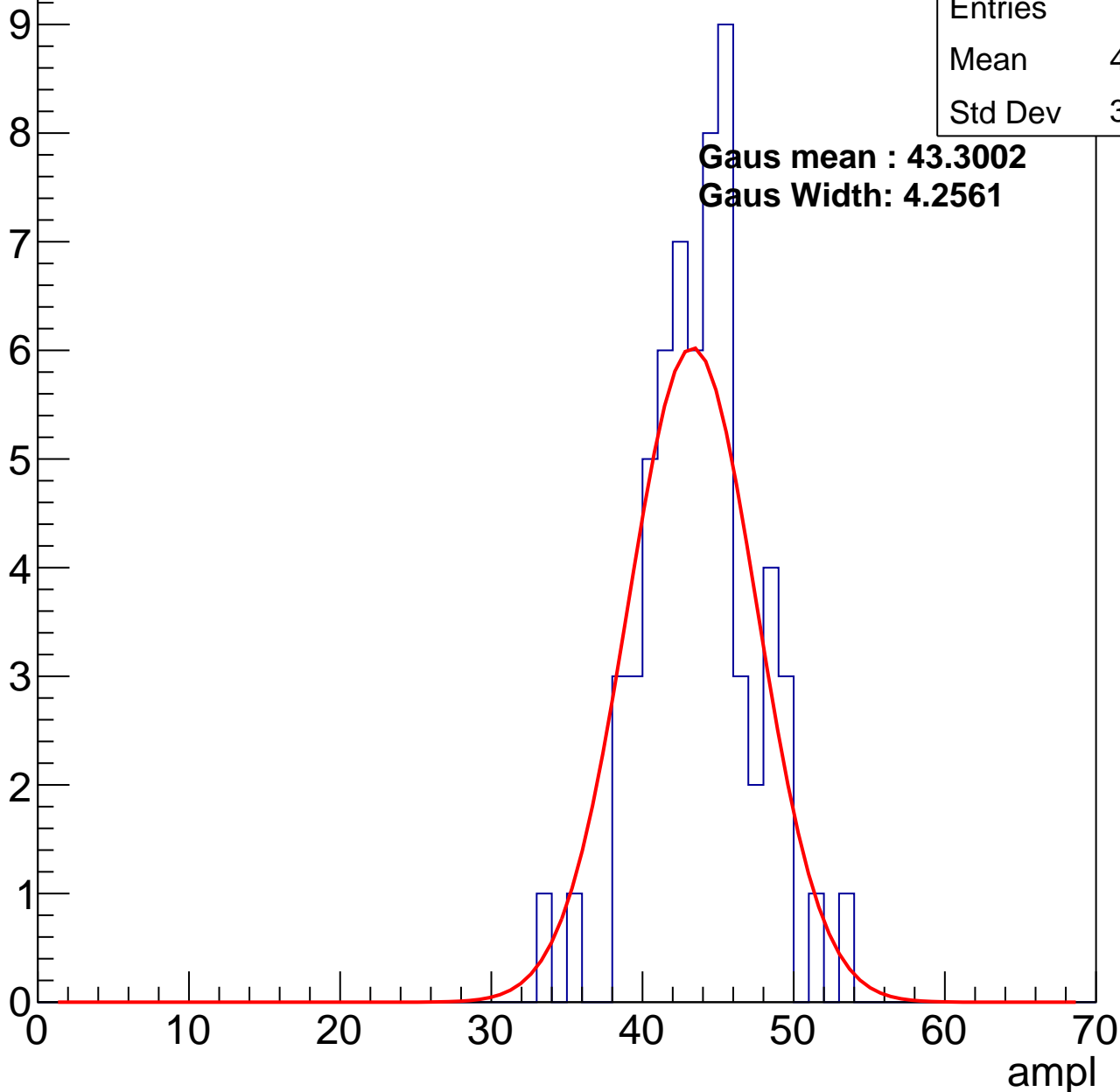
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	63
Mean	43.32
Std Dev	3.633

**Gaus mean : 43.3002**

**Gaus Width: 4.2561**

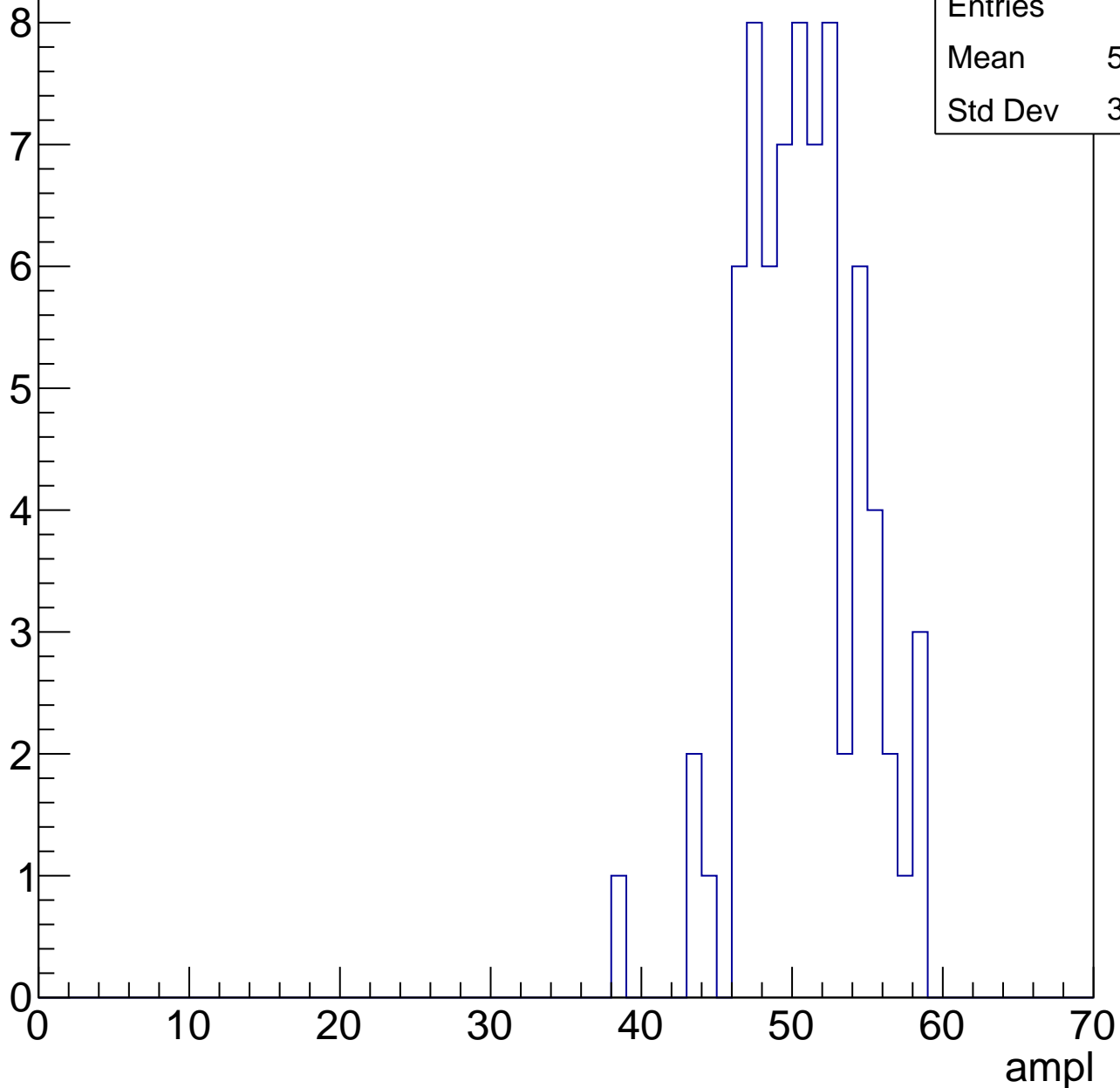


# B1L102S, U12-ch123, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

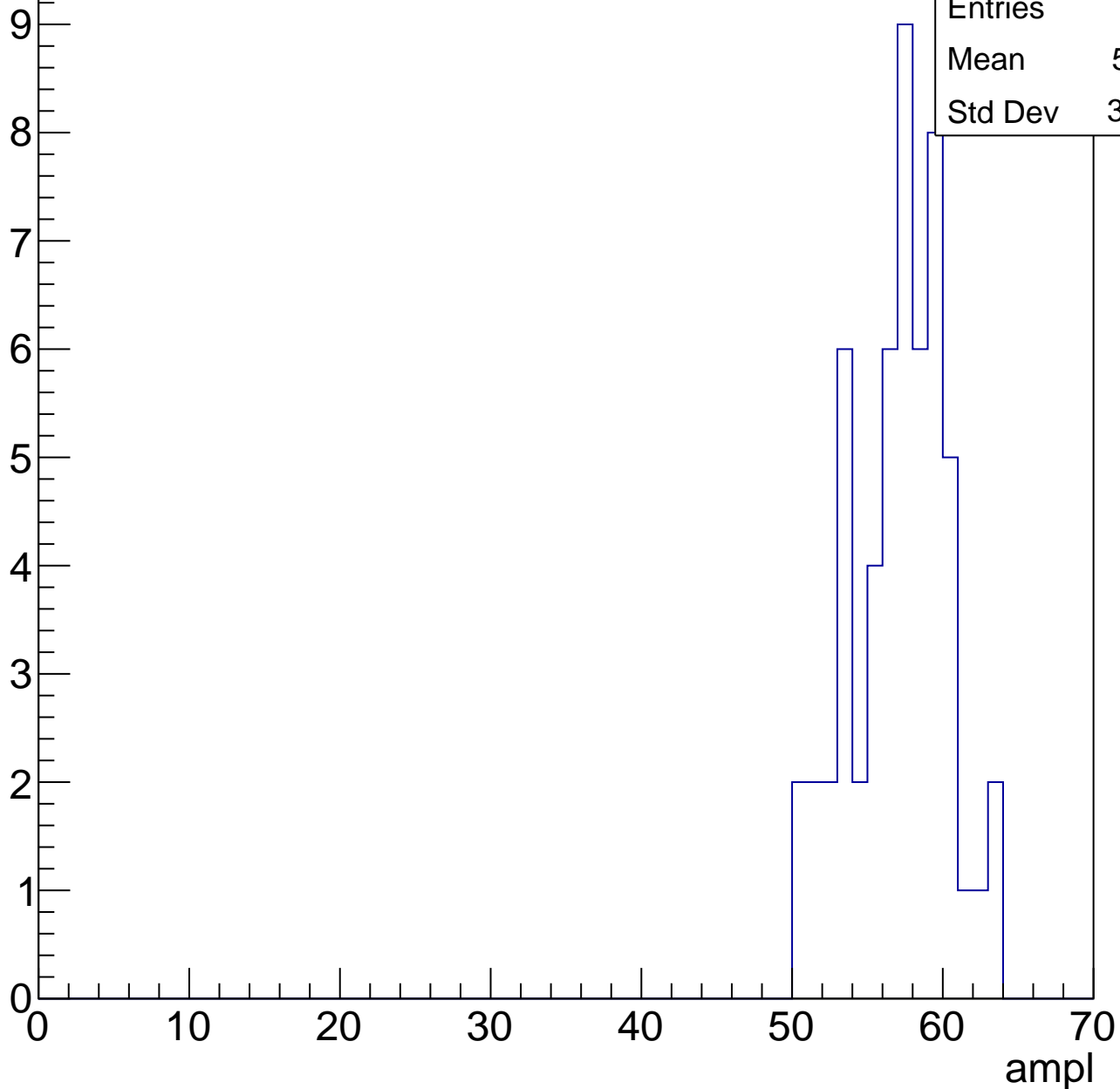
Entries	72
Mean	50.24
Std Dev	3.799



# B1L102S, U12-ch123, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

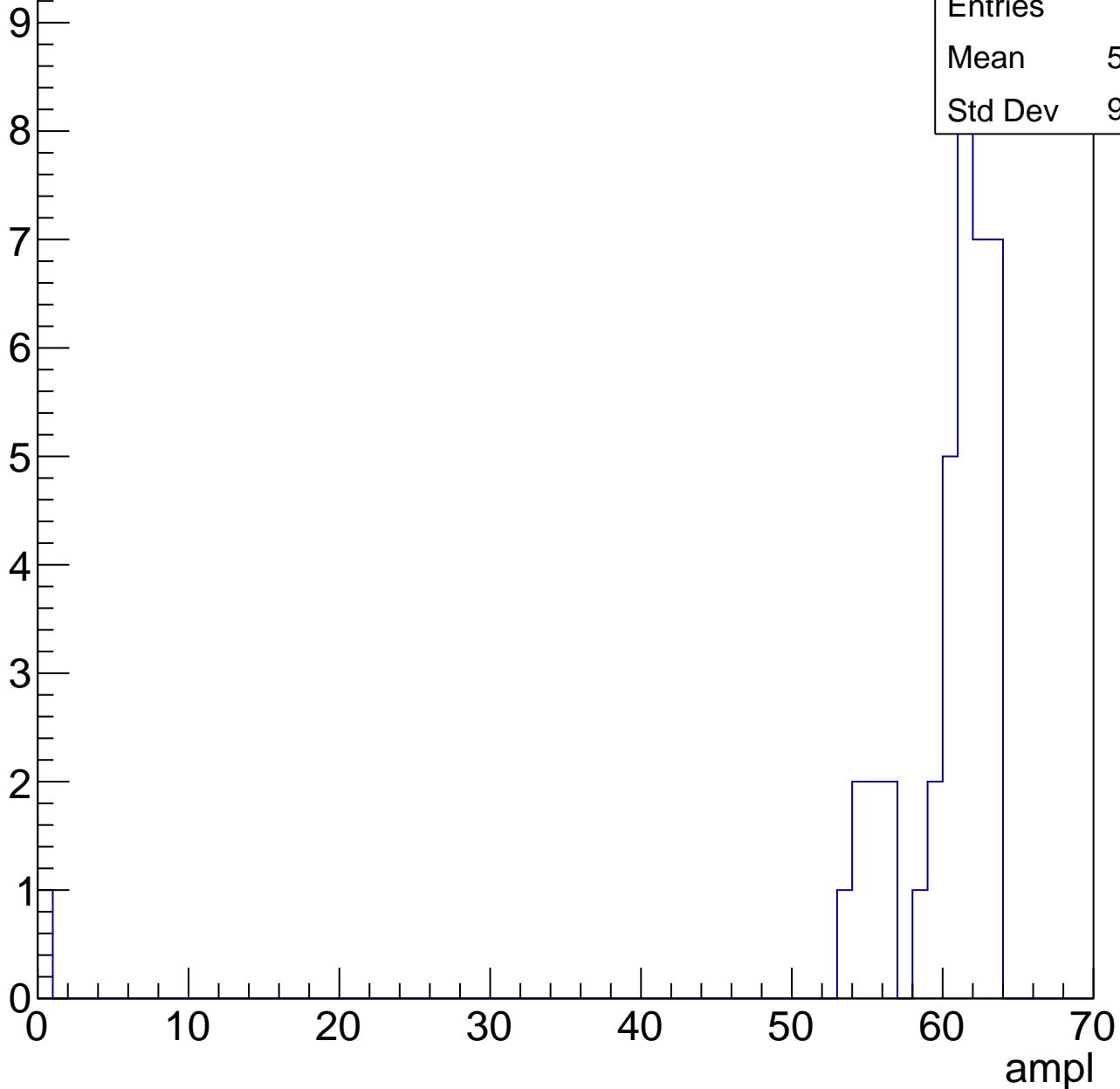


# B1L102S, U12-ch123, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	39
Mean	58.54
Std Dev	9.904



# B1L102S, U12-ch123, adc6

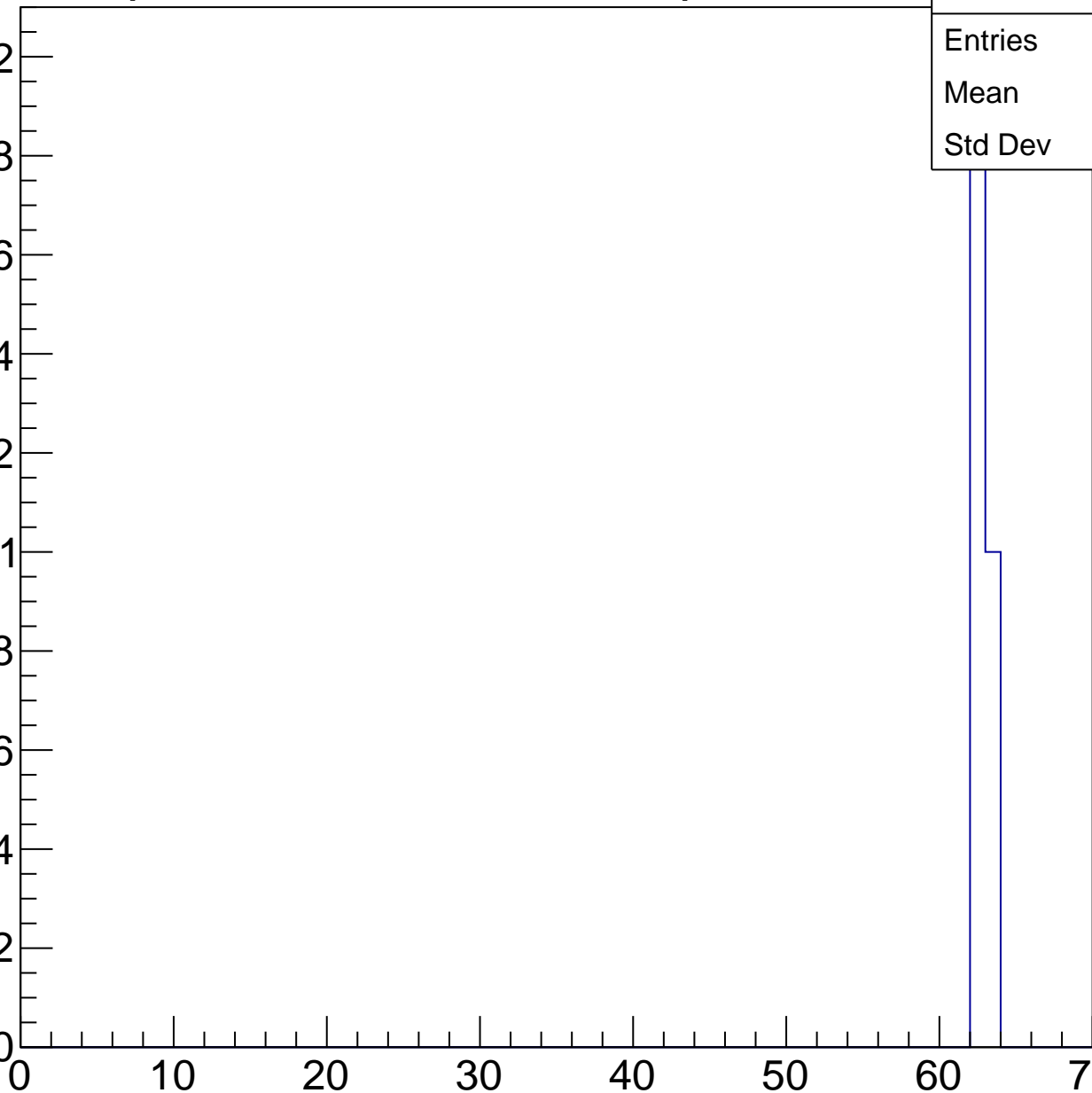
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	3
Mean	62.33
Std Dev	0.4714

ampl

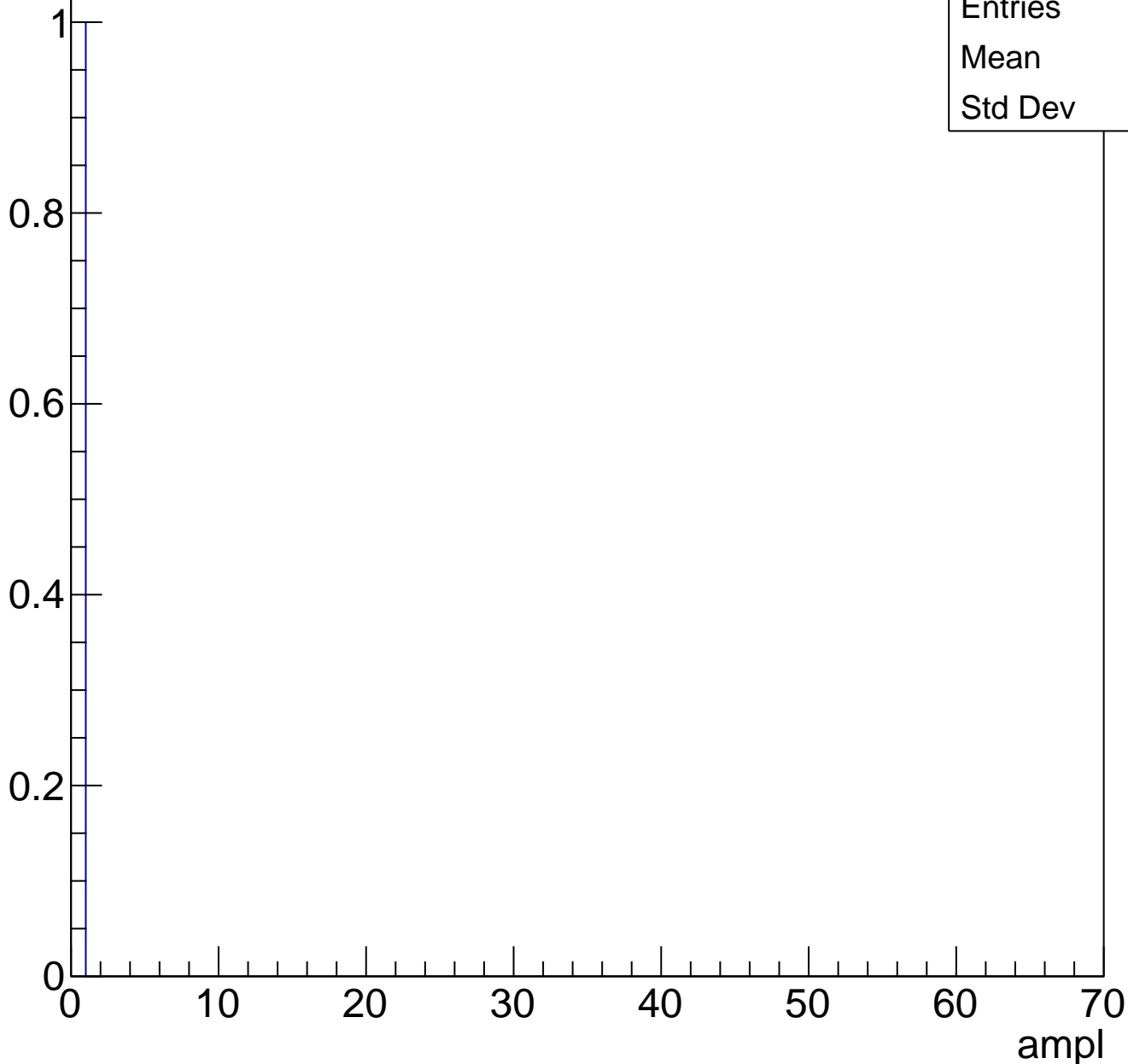




# B1L102S, U12-ch123, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U12-ch124, adc0

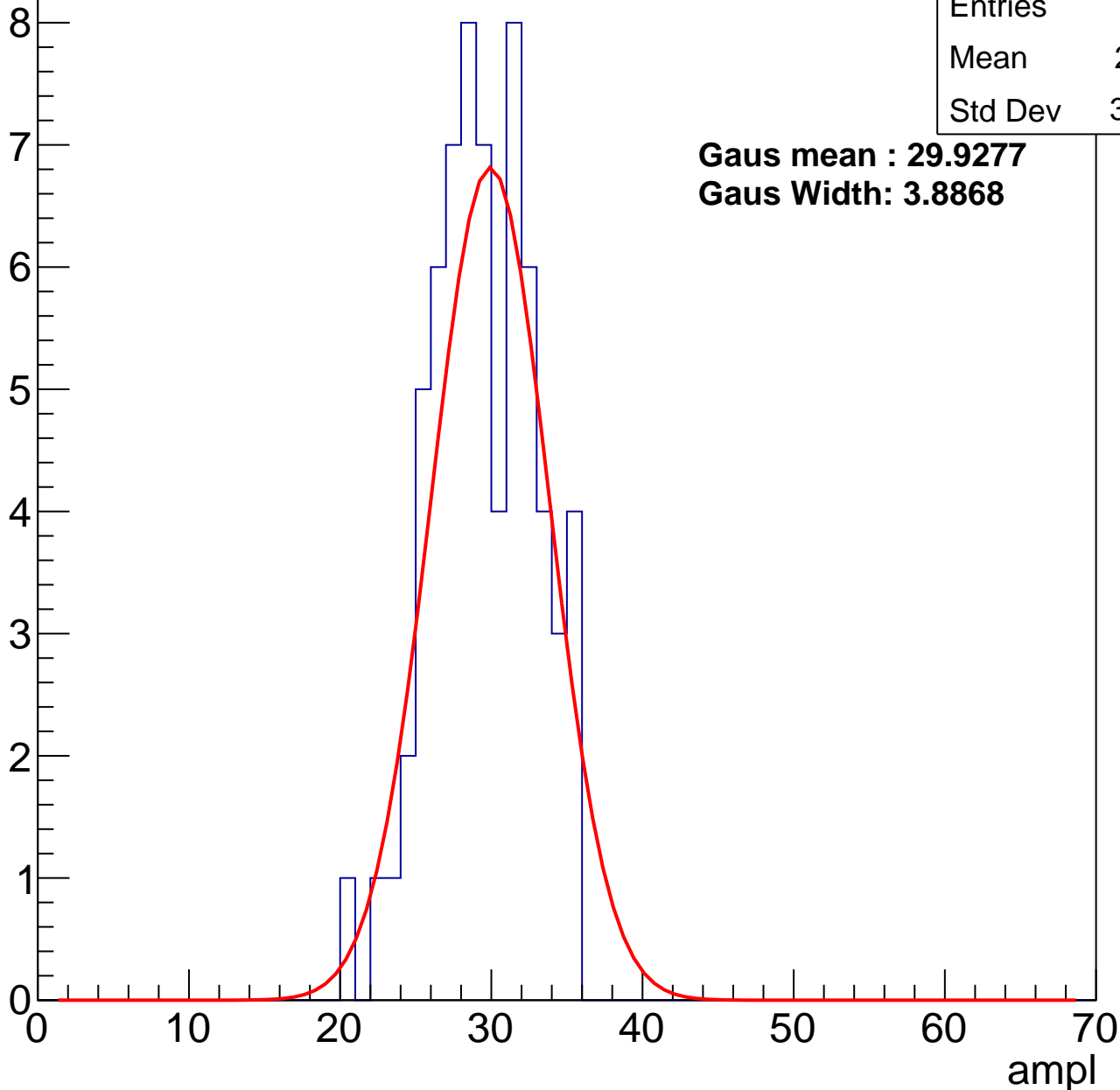
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	67
Mean	29.01
Std Dev	3.366

**Gaus mean : 29.9277**

**Gaus Width: 3.8868**



# B1L102S, U12-ch124, adc1

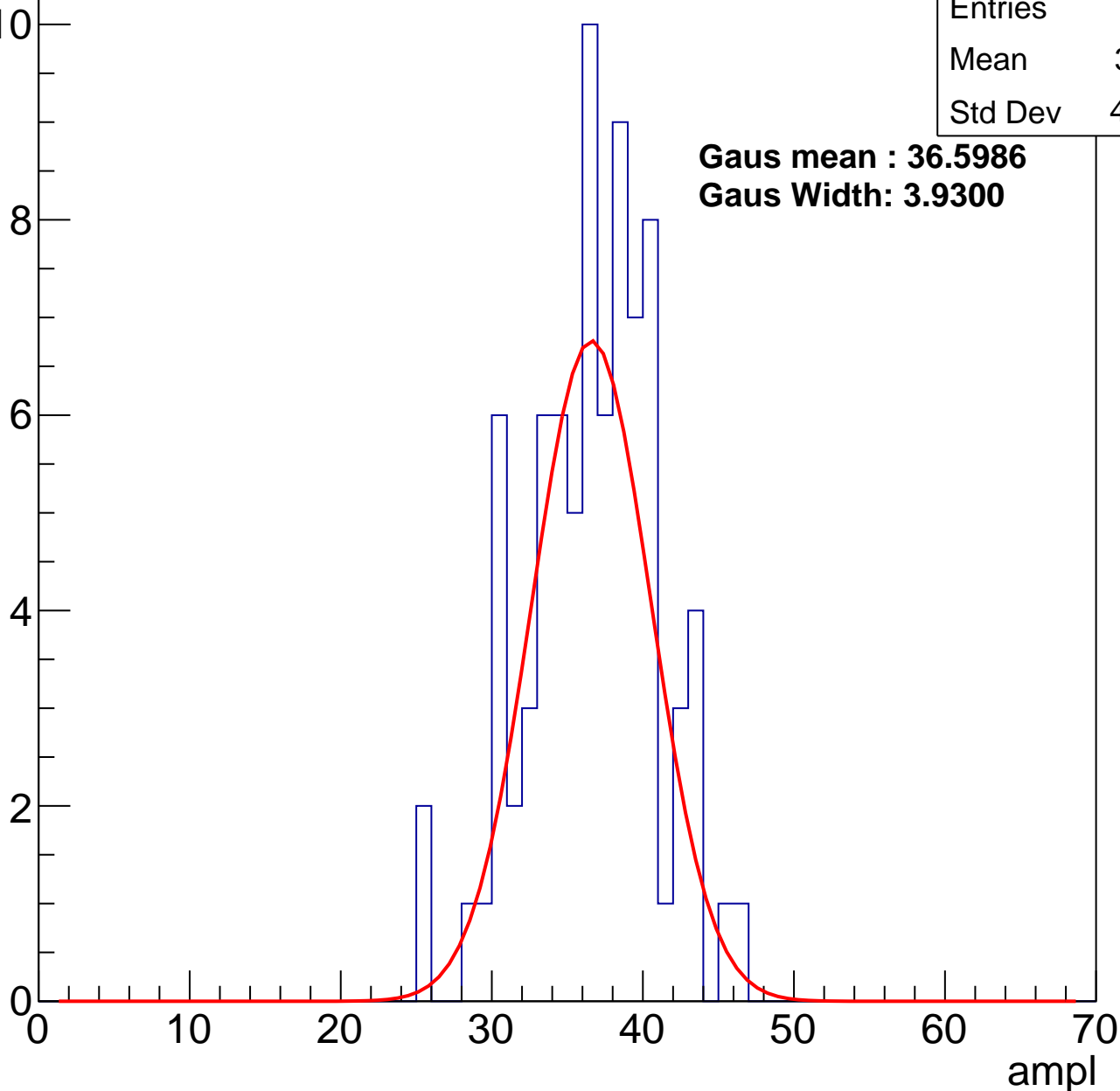
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	82
Mean	36.21
Std Dev	4.265

**Gaus mean : 36.5986**

**Gaus Width: 3.9300**



# B1L102S, U12-ch124, adc2

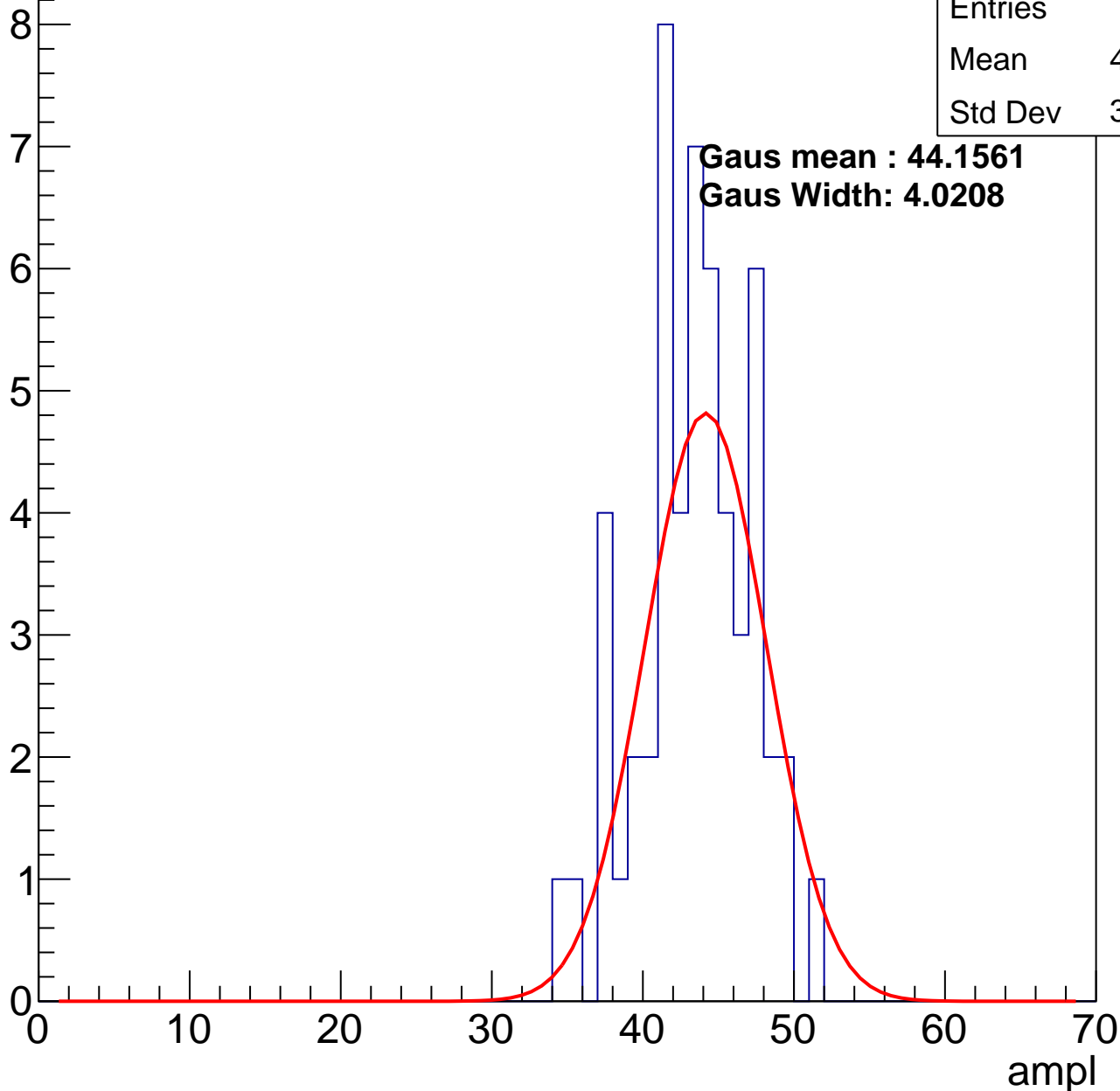
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	54
Mean	42.94
Std Dev	3.679

**Gaus mean : 44.1561**

**Gaus Width: 4.0208**

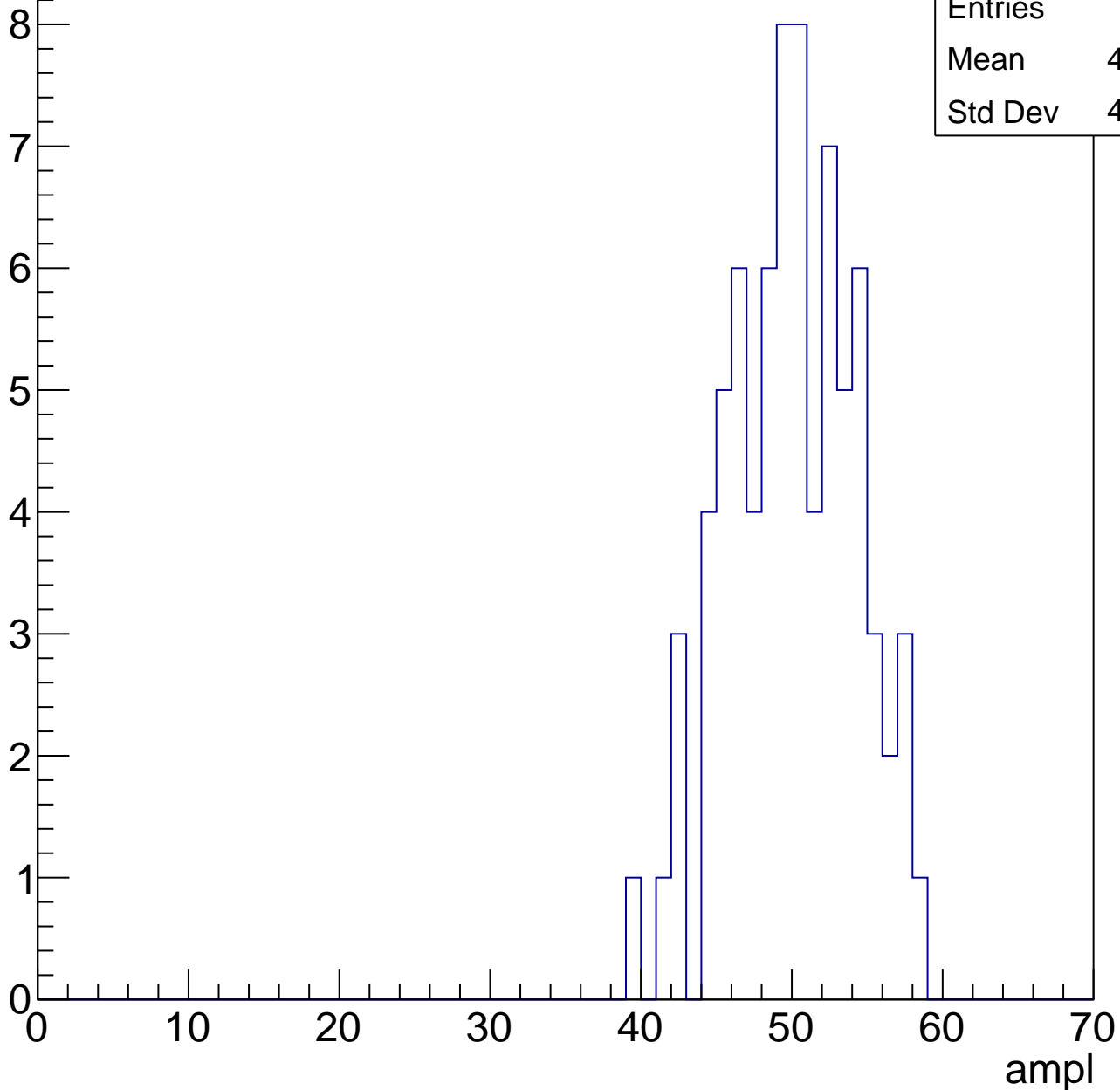


# B1L102S, U12-ch124, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	77
Mean	49.53
Std Dev	4.173

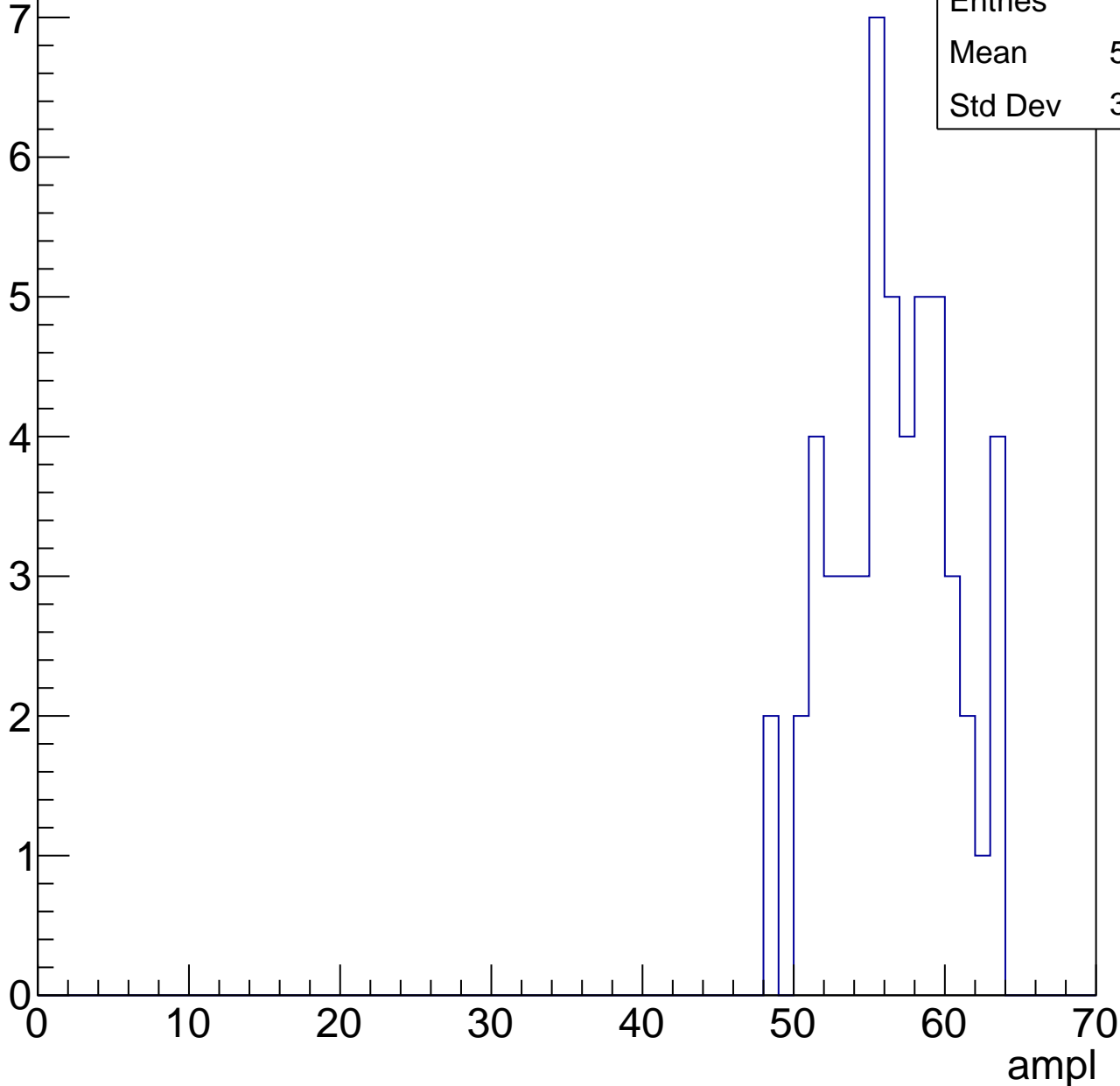


# B1L102S, U12-ch124, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	53
Mean	56.06
Std Dev	3.868

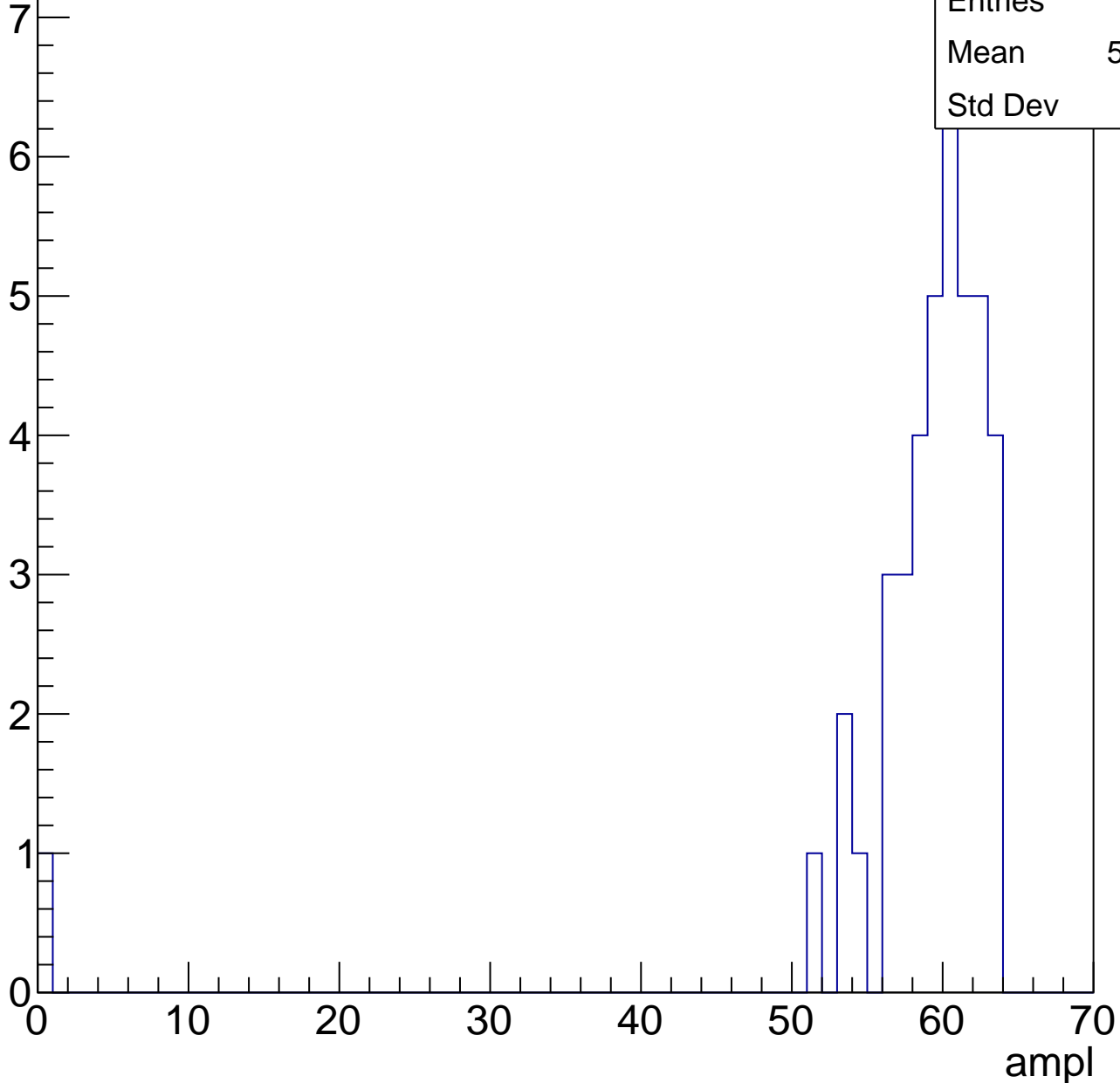


# B1L102S, U12-ch124, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

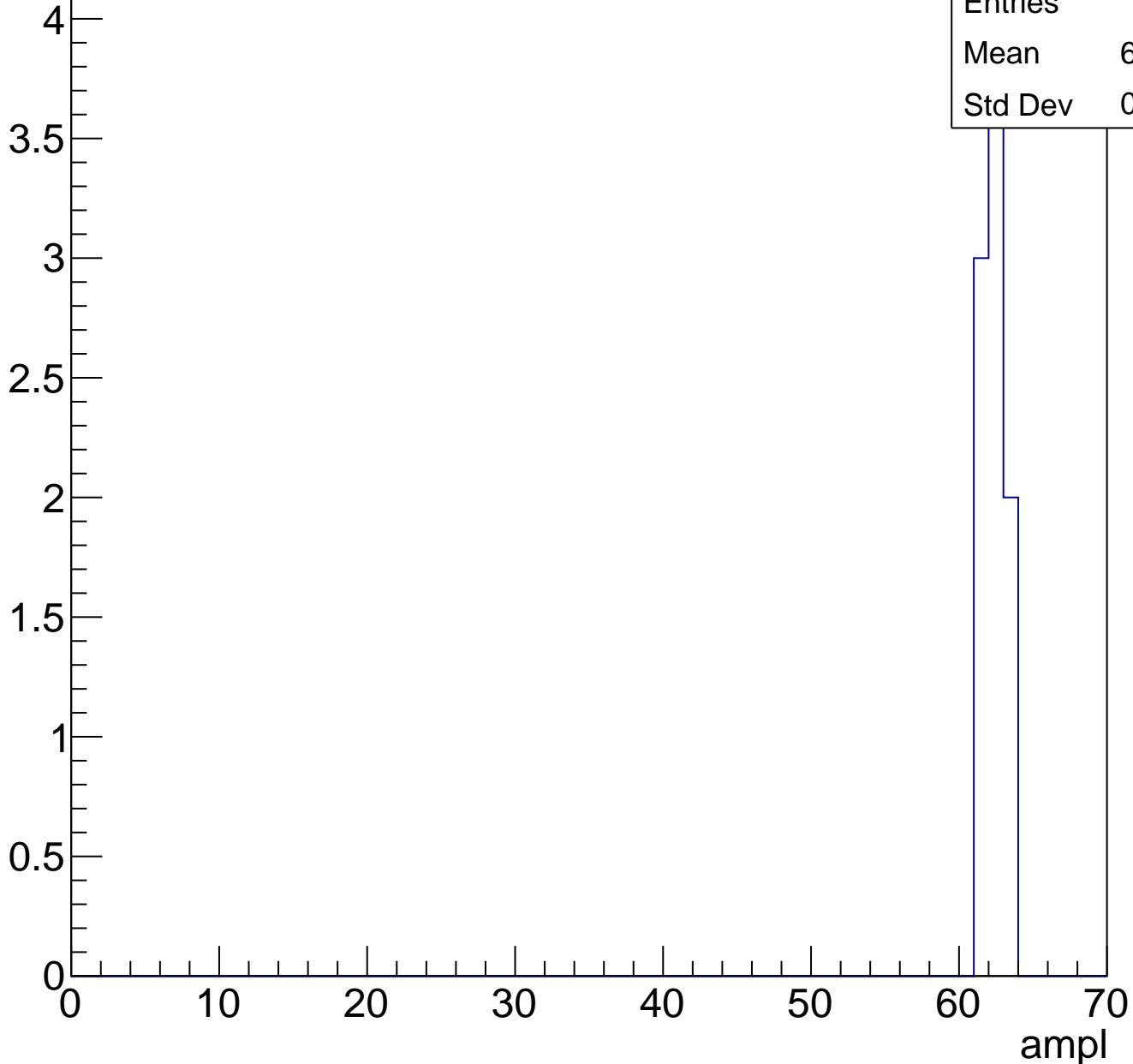
Entries	41
Mean	57.66
Std Dev	9.56



# B1L102S, U12-ch124, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



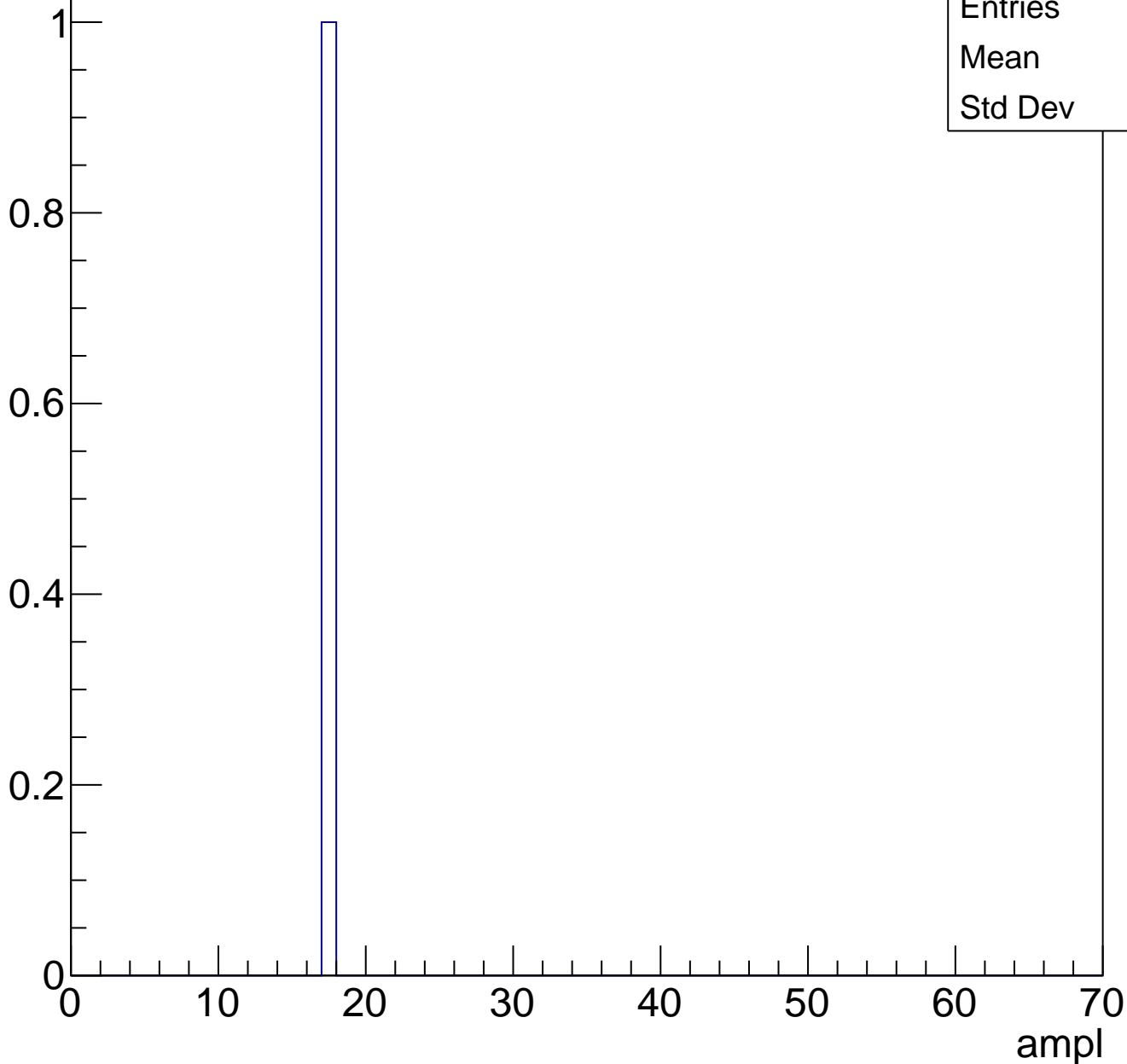
Entries	9
Mean	61.89
Std Dev	0.737



# B1L102S, U12-ch124, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U12-ch125, adc0

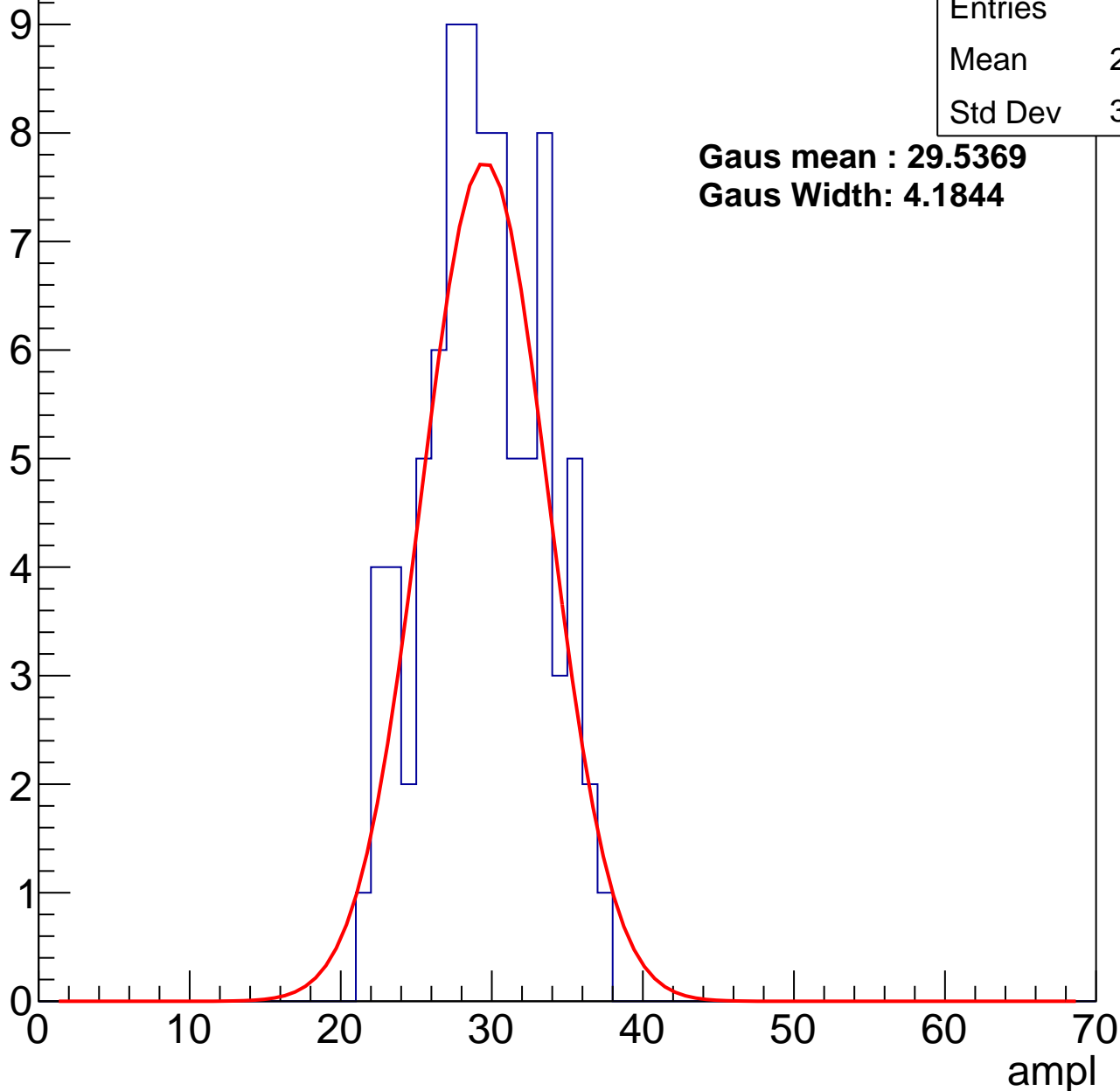
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	85
Mean	28.96
Std Dev	3.836

**Gaus mean : 29.5369**

**Gaus Width: 4.1844**



# B1L102S, U12-ch125, adc1

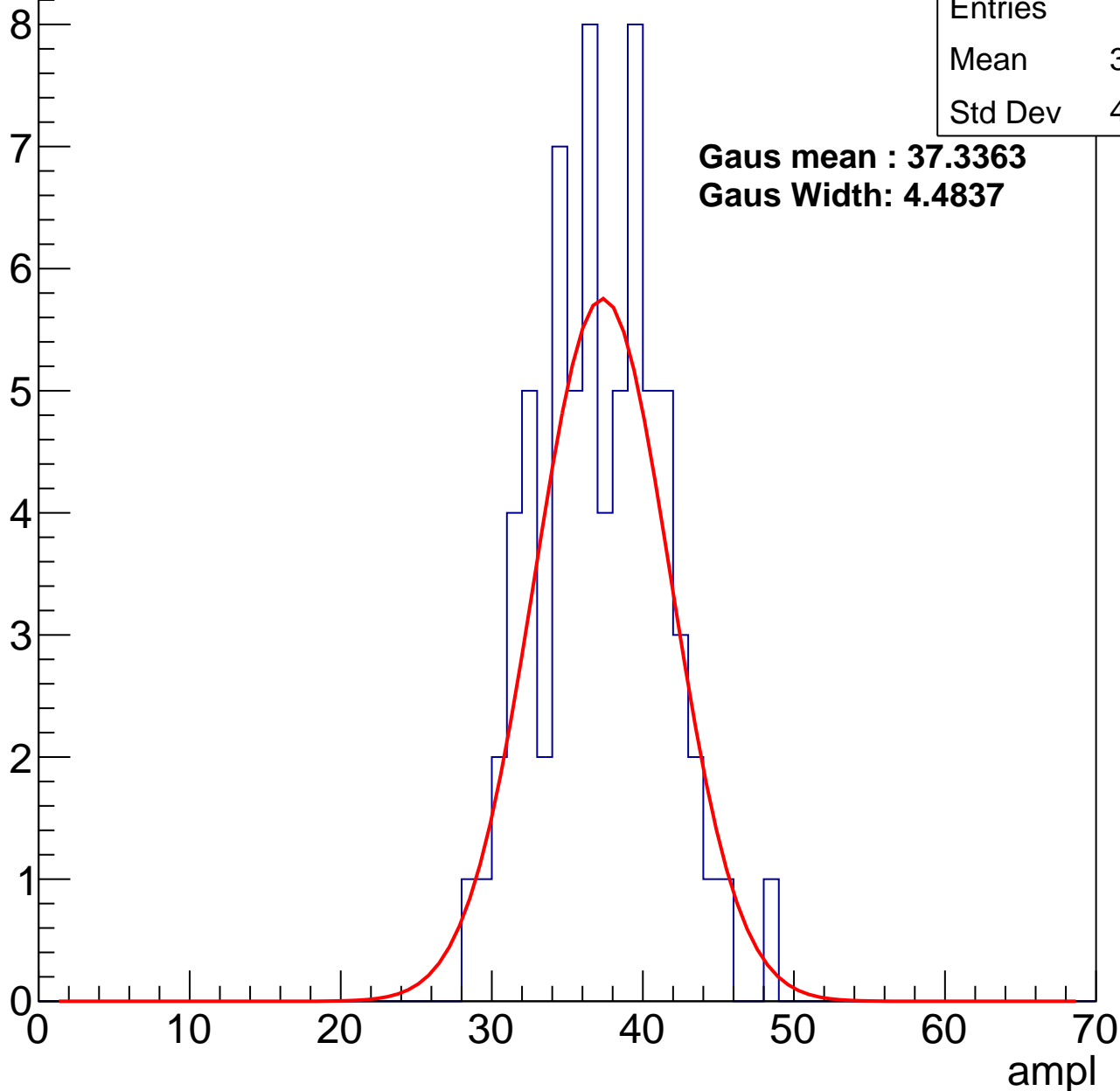
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	70
Mean	36.74
Std Dev	4.094

**Gaus mean : 37.3363**

**Gaus Width: 4.4837**



# B1L102S, U12-ch125, adc2

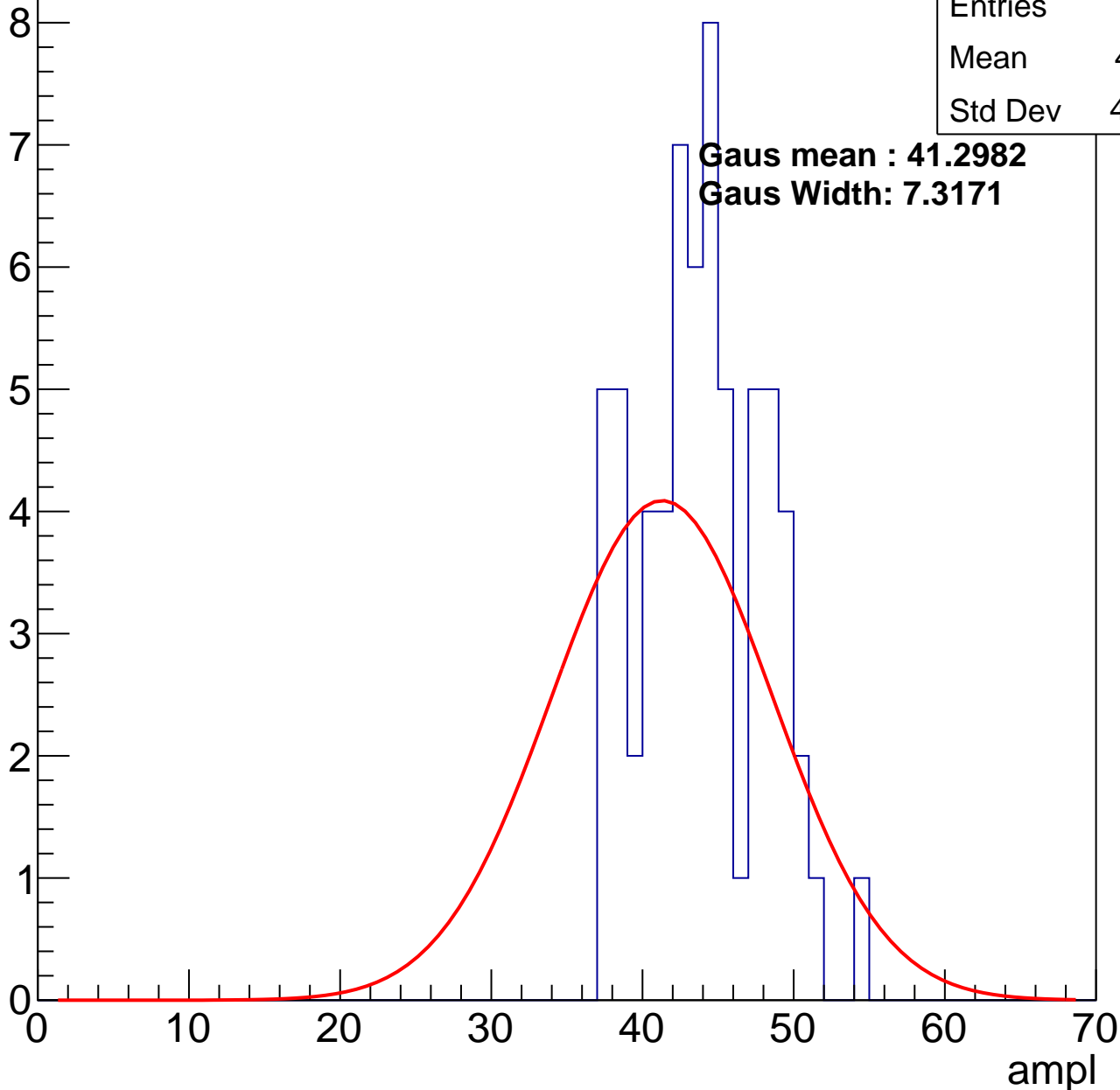
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	65
Mean	43.51
Std Dev	4.016

**Gaus mean : 41.2982**

**Gaus Width: 7.3171**

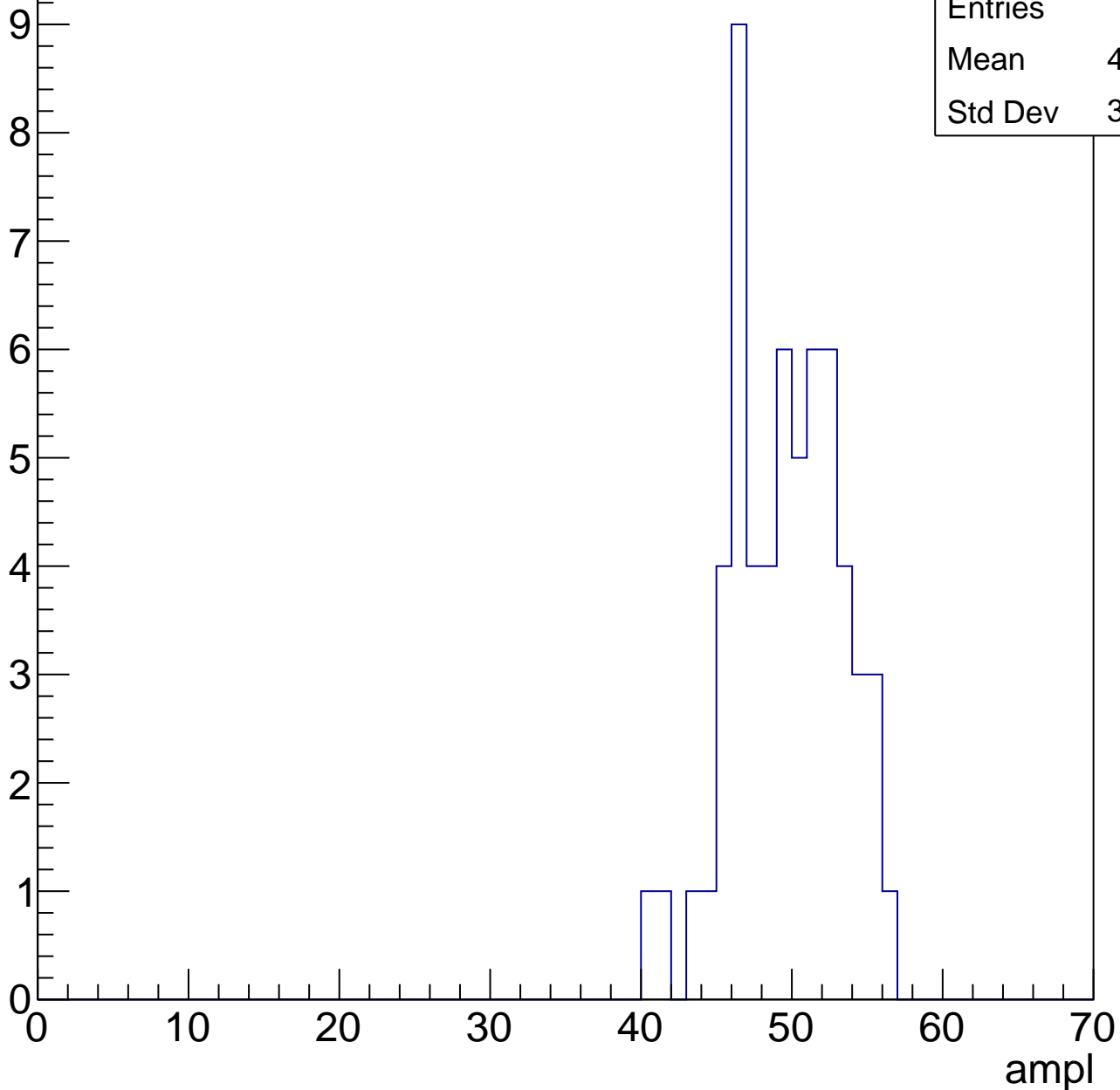


# B1L102S, U12-ch125, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	59
Mean	49.14
Std Dev	3.563

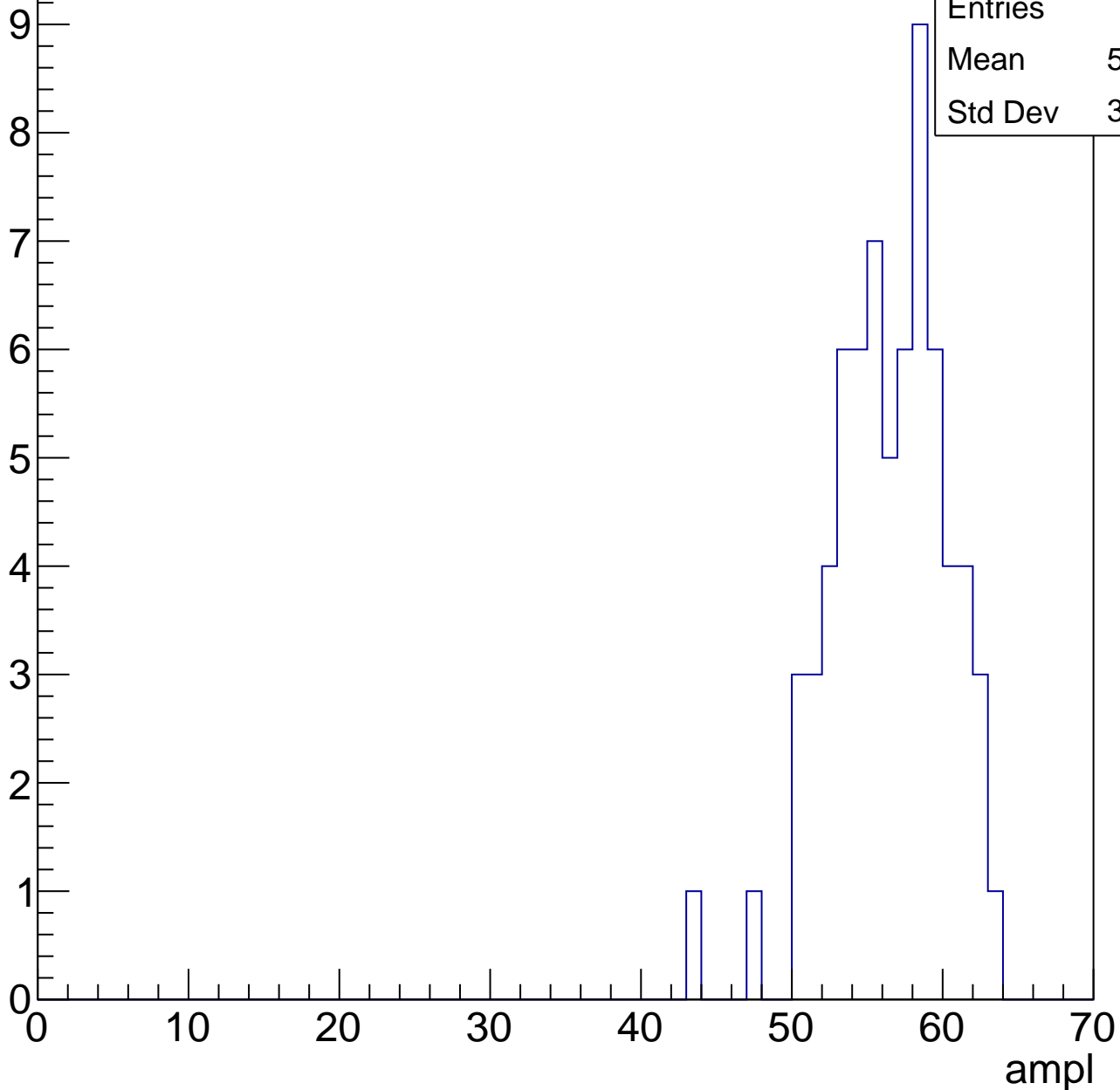


# B1L102S, U12-ch125, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	55.93
Std Dev	3.804

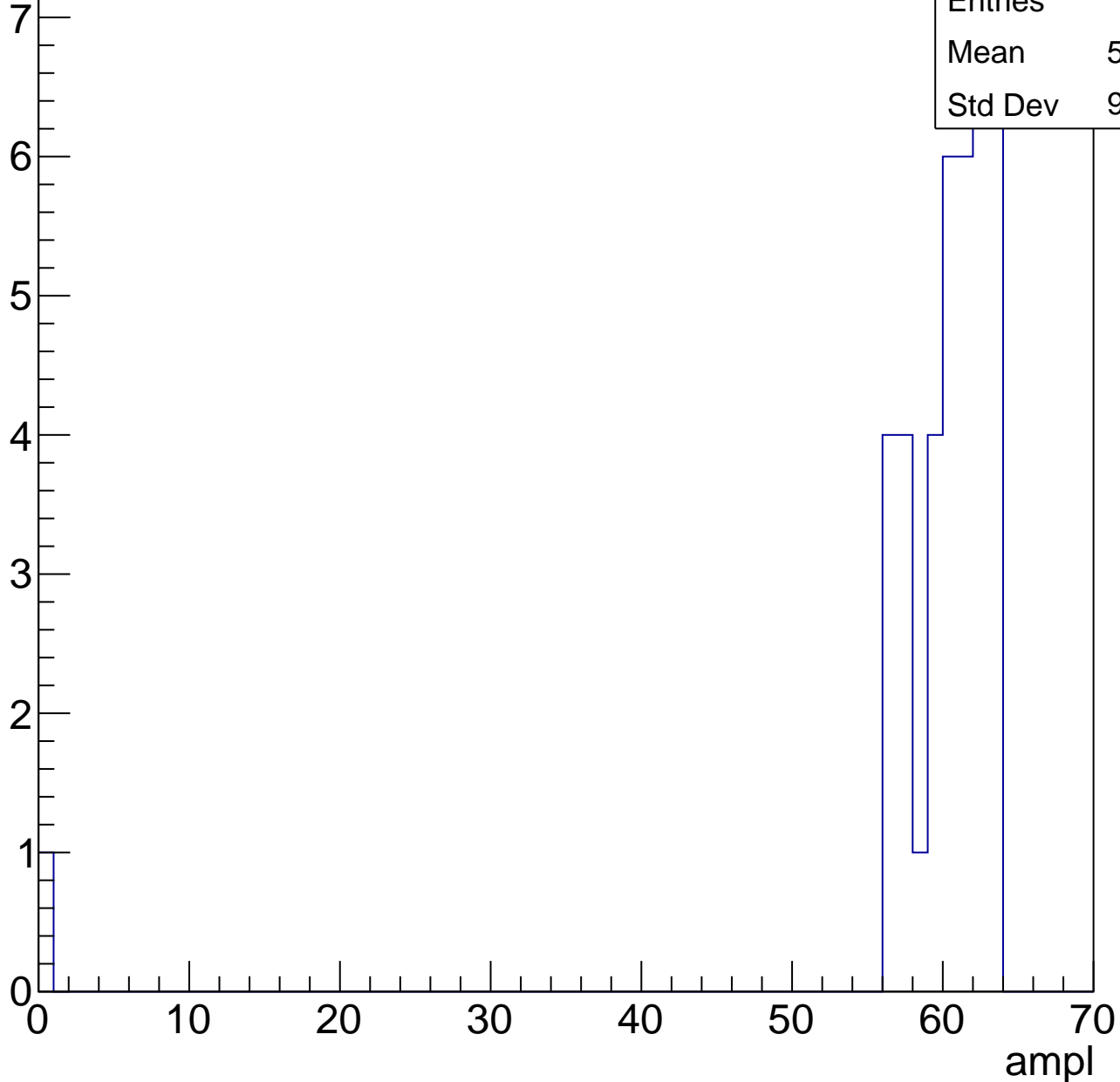


# B1L102S, U12-ch125, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	40
Mean	58.67
Std Dev	9.663



# B1L102S, U12-ch125, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U12-ch125, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U12-ch126, adc0

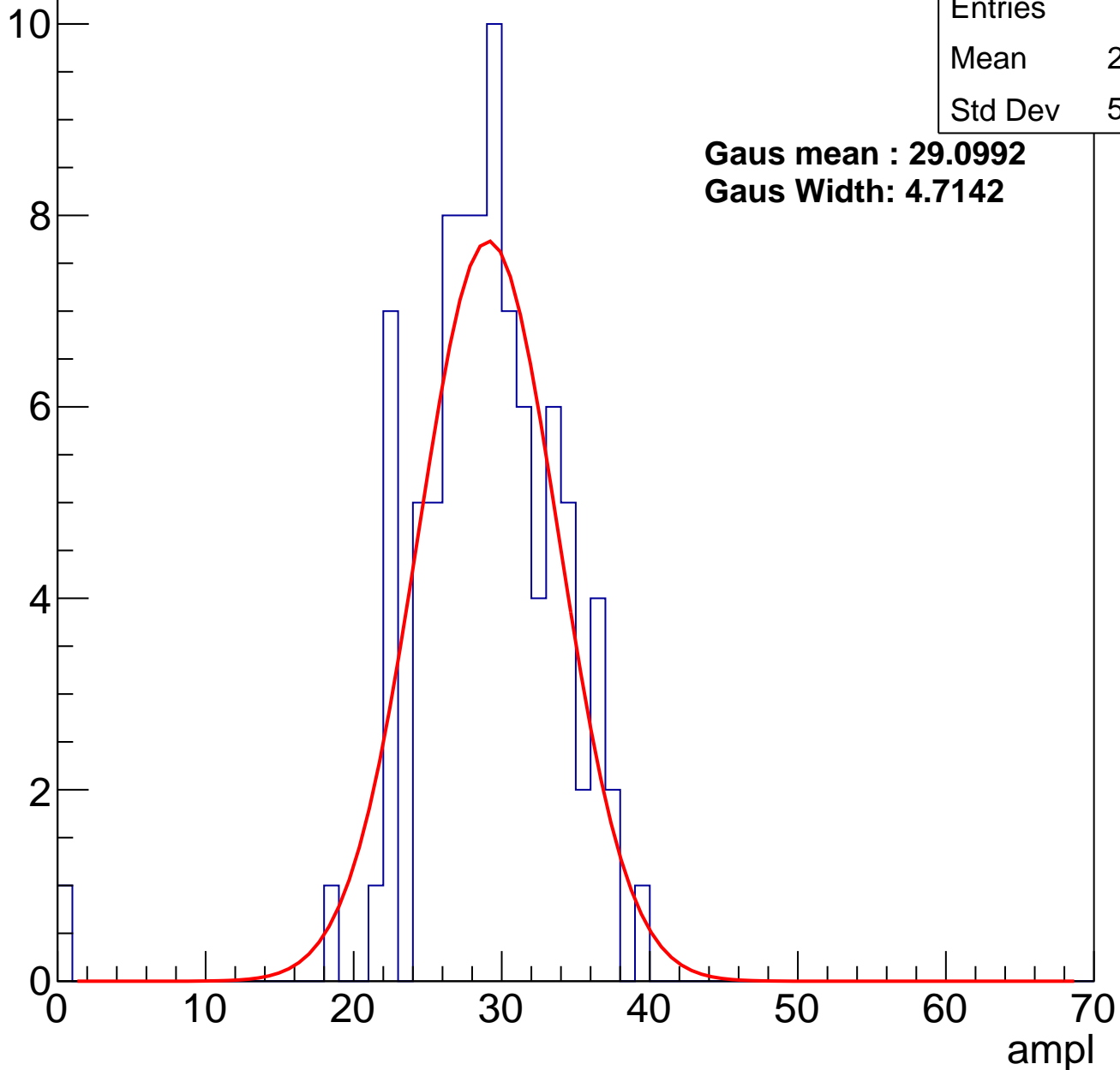
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	91
Mean	28.52
Std Dev	5.187

**Gaus mean : 29.0992**

**Gaus Width: 4.7142**

Entry



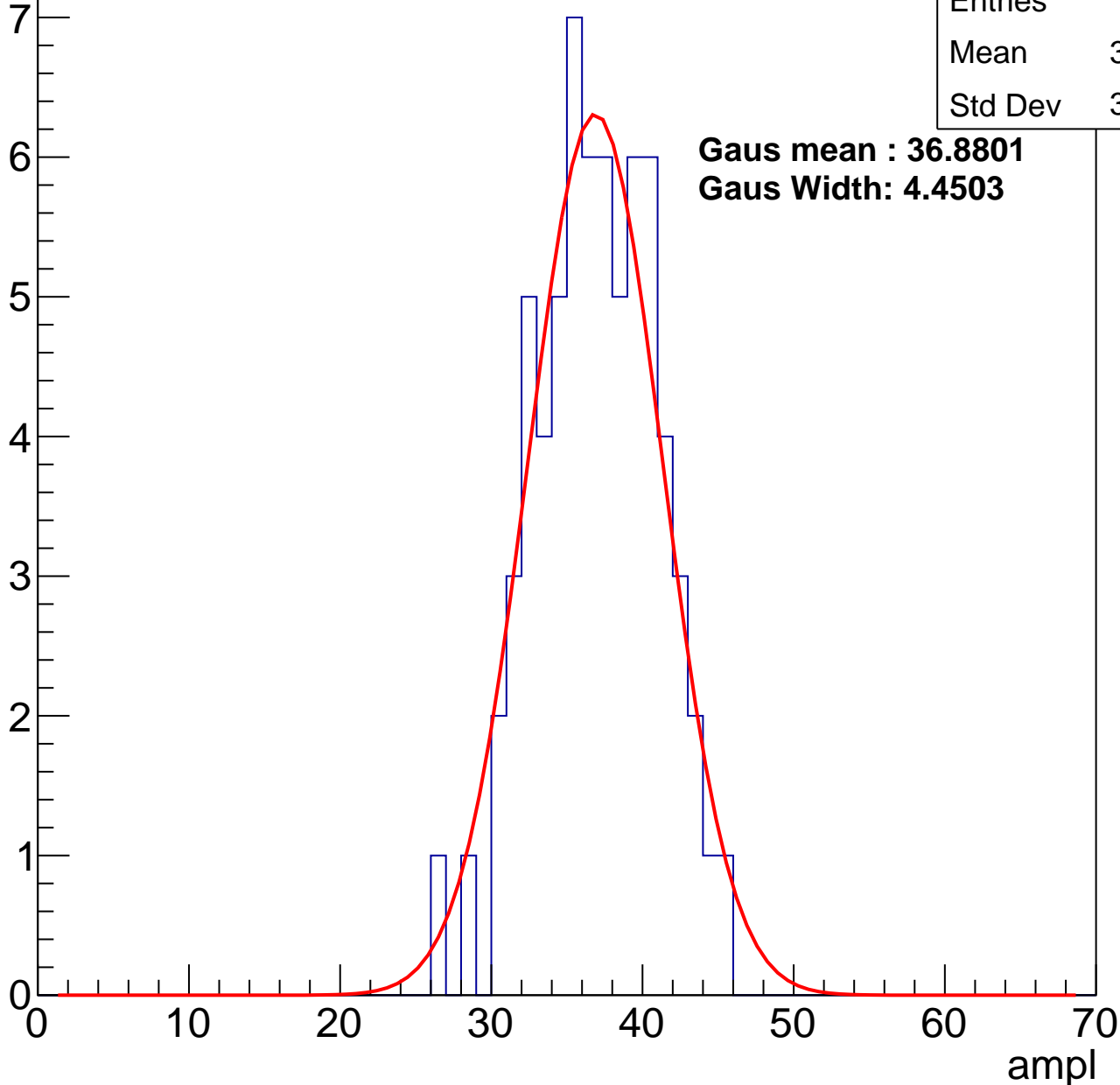
# B1L102S, U12-ch126, adc1

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	36.49
Std Dev	3.957

**Gaus mean : 36.8801**  
**Gaus Width: 4.4503**



# B1L102S, U12-ch126, adc2

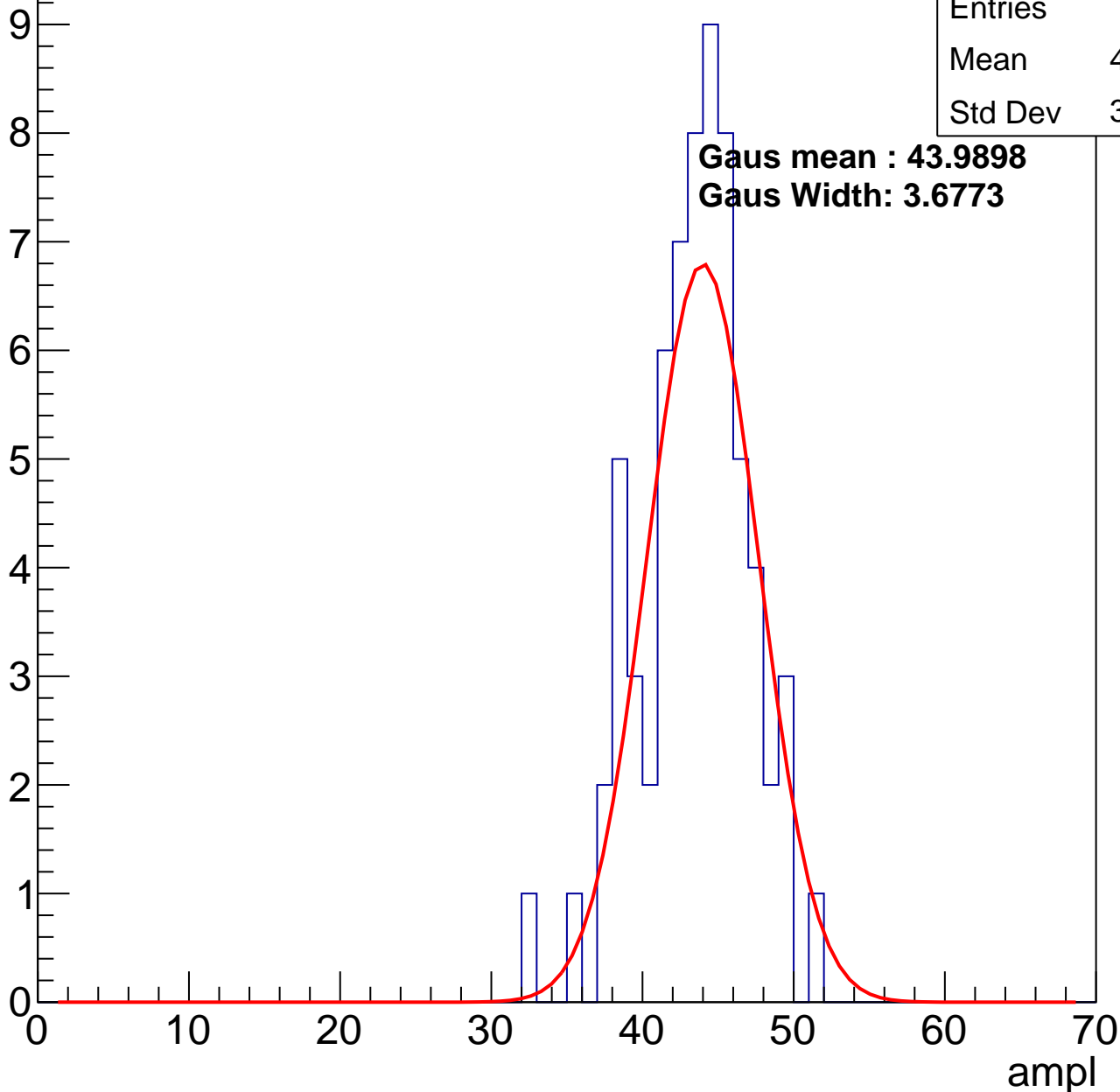
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	67
Mean	42.99
Std Dev	3.564

**Gaus mean : 43.9898**

**Gaus Width: 3.6773**

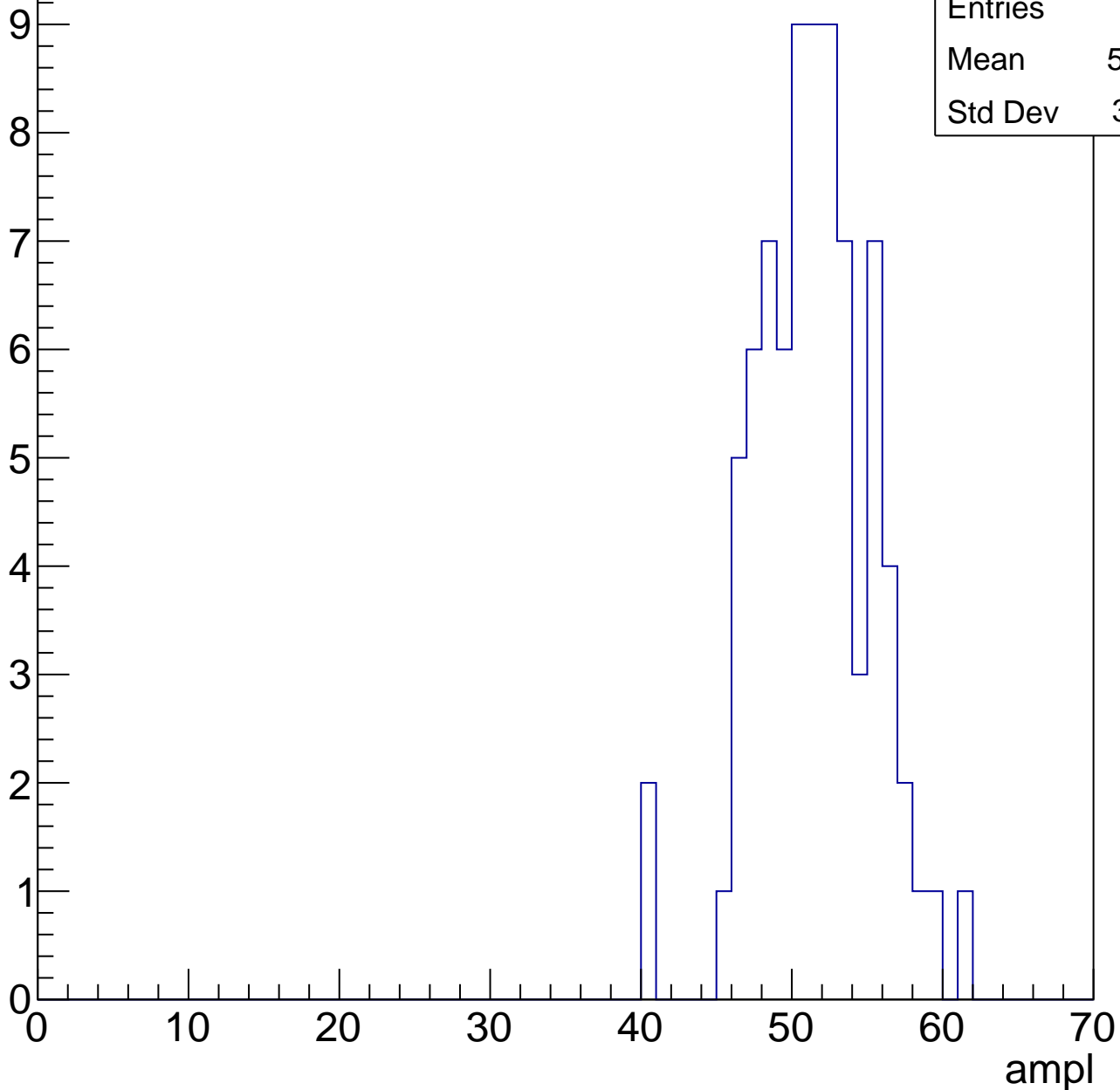


# B1L102S, U12-ch126, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	80
Mean	50.98
Std Dev	3.801

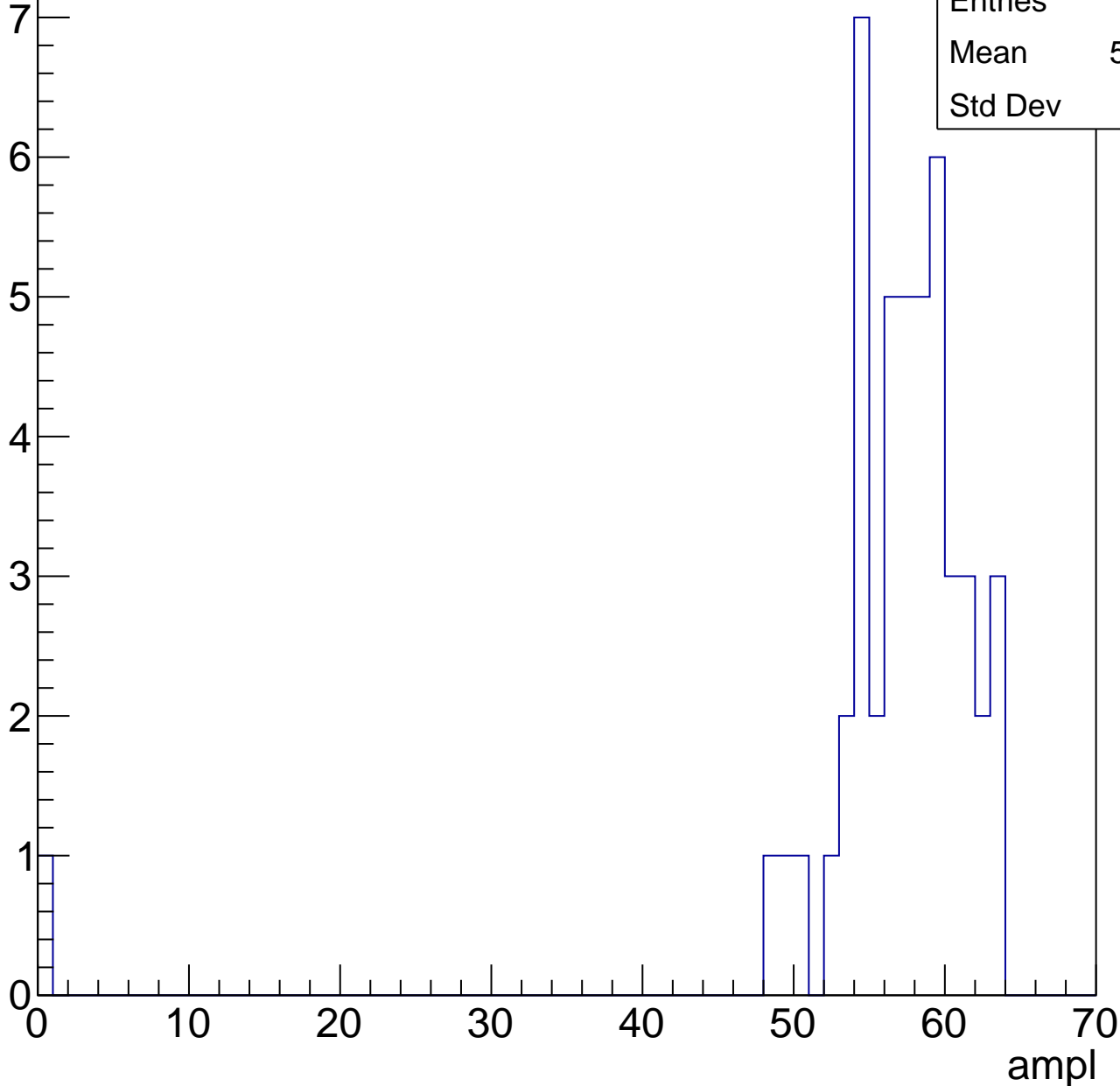


# B1L102S, U12-ch126, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	48
Mean	55.79
Std Dev	8.86

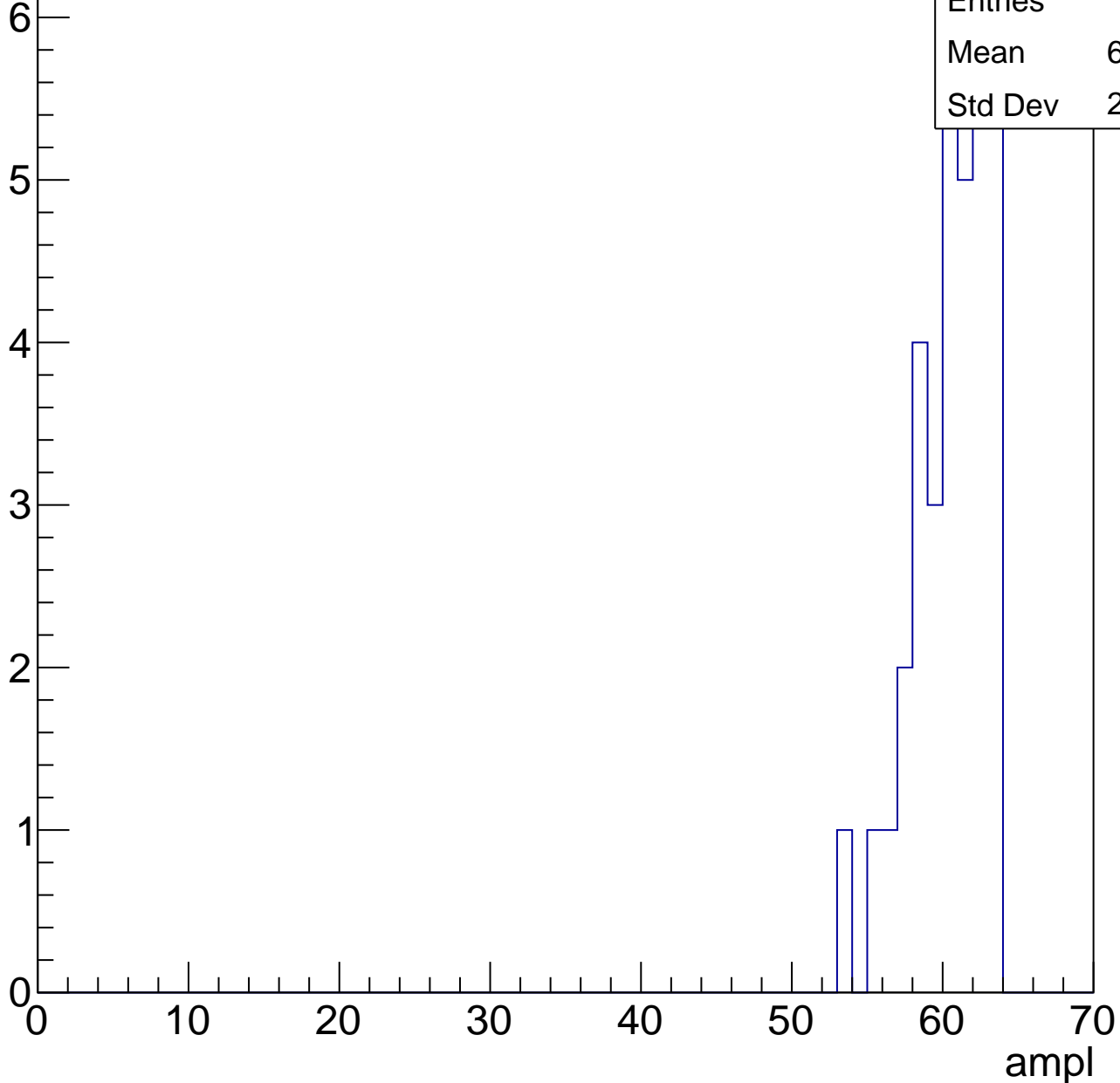


# B1L102S, U12-ch126, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	35
Mean	60.06
Std Dev	2.449



# B1L102S, U12-ch126, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	6
Mean	60.83
Std Dev	1.951

ampl

0 10 20 30 40 50 60 70



# B1L102S, U12-ch126, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L102S, U12-ch127, adc0

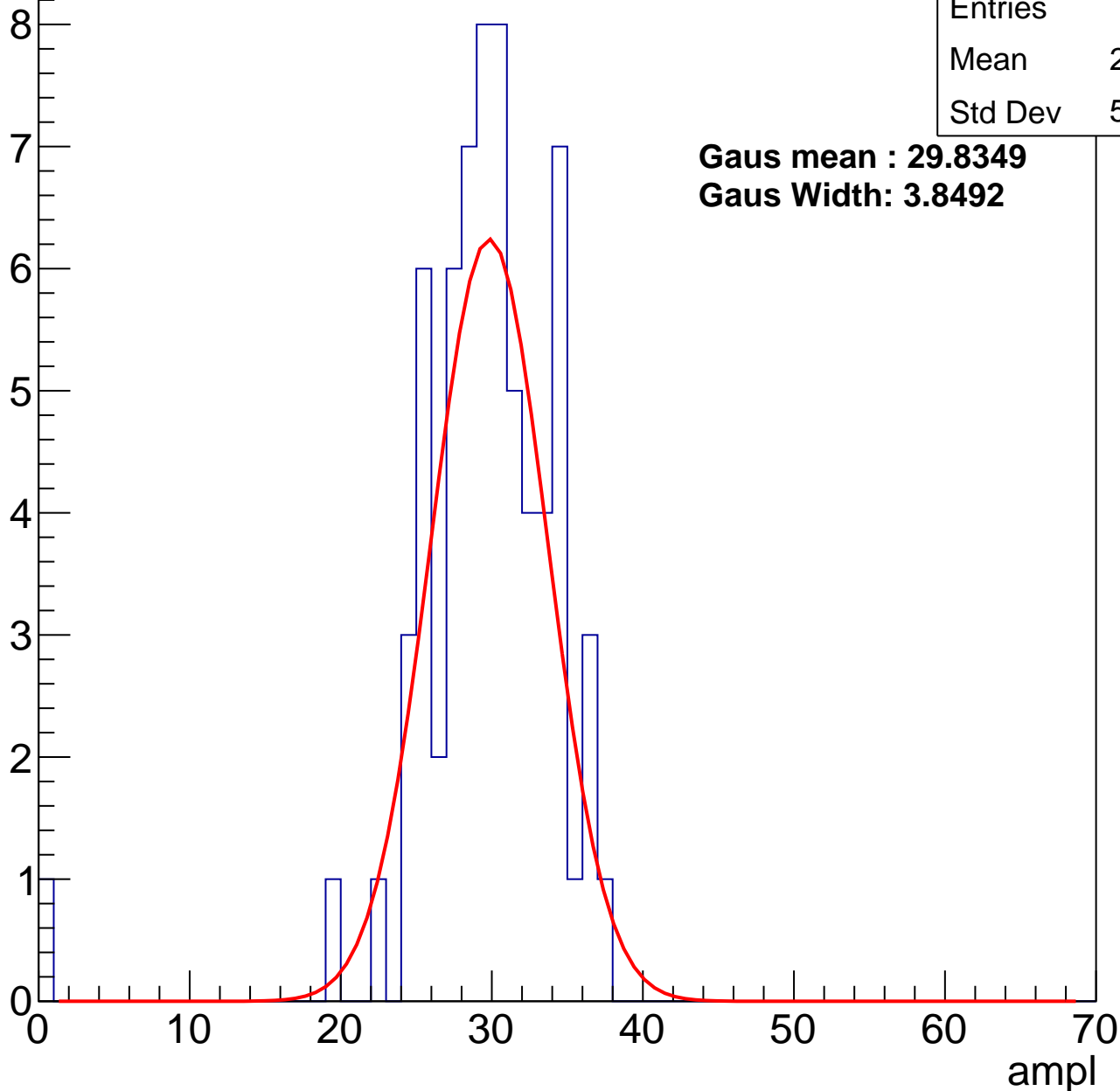
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	29.09
Std Dev	5.087

**Gaus mean : 29.8349**

**Gaus Width: 3.8492**



# B1L102S, U12-ch127, adc1

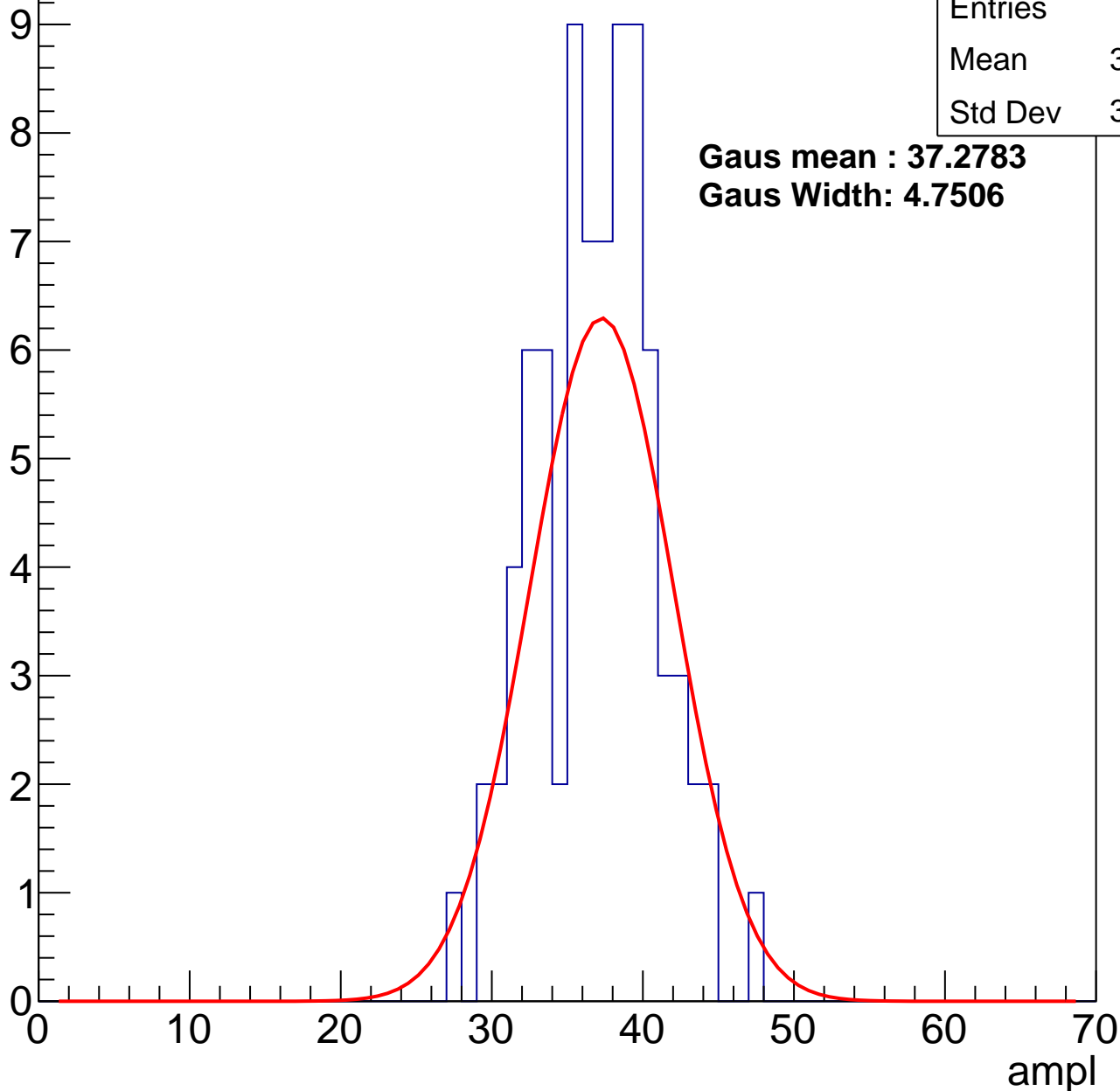
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	81
Mean	36.49
Std Dev	3.926

**Gaus mean : 37.2783**

**Gaus Width: 4.7506**



# B1L102S, U12-ch127, adc2

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	71
Mean	44.31
Std Dev	3.598

**Gaus mean : 44.9660**

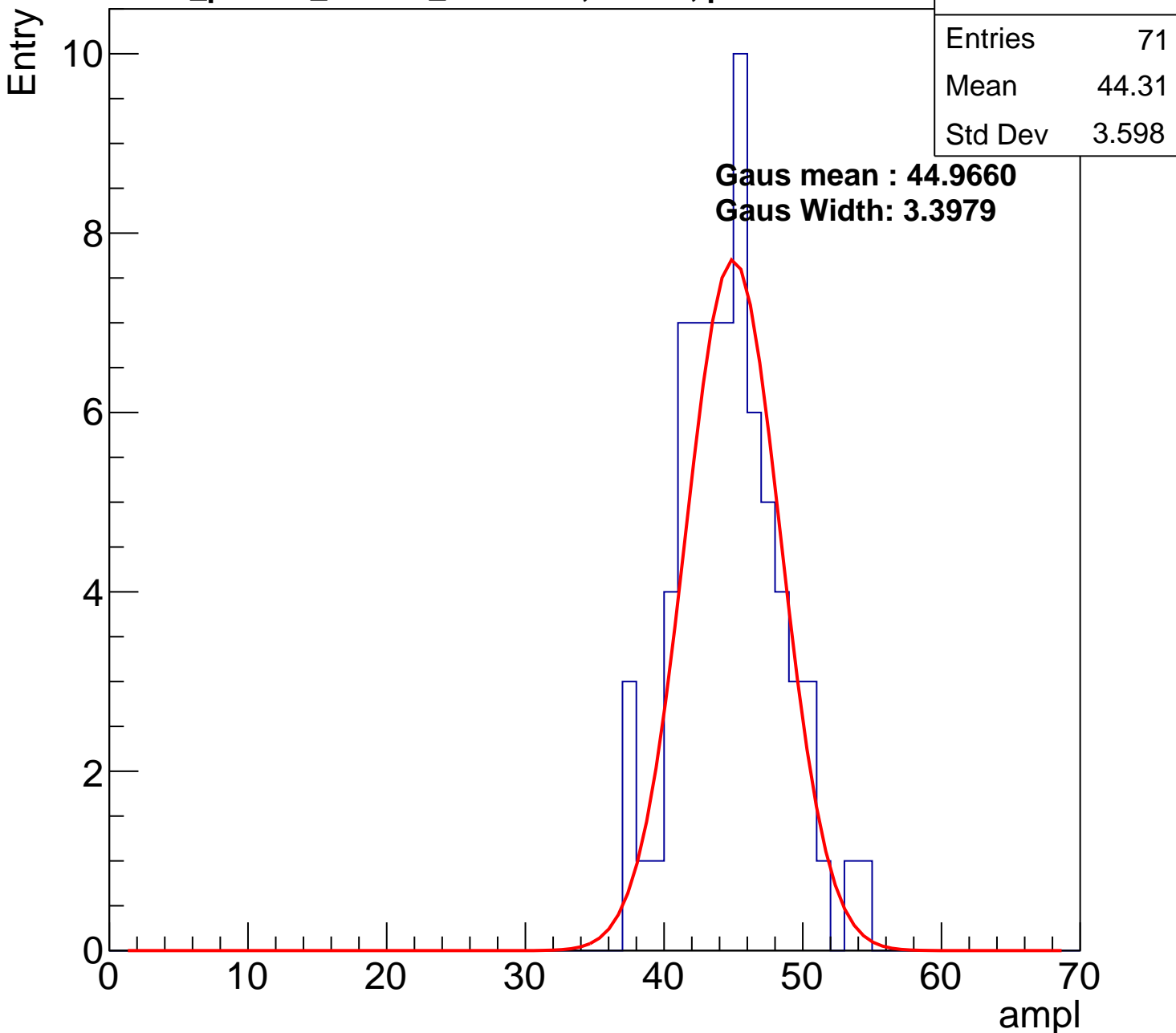
**Gaus Width: 3.3979**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

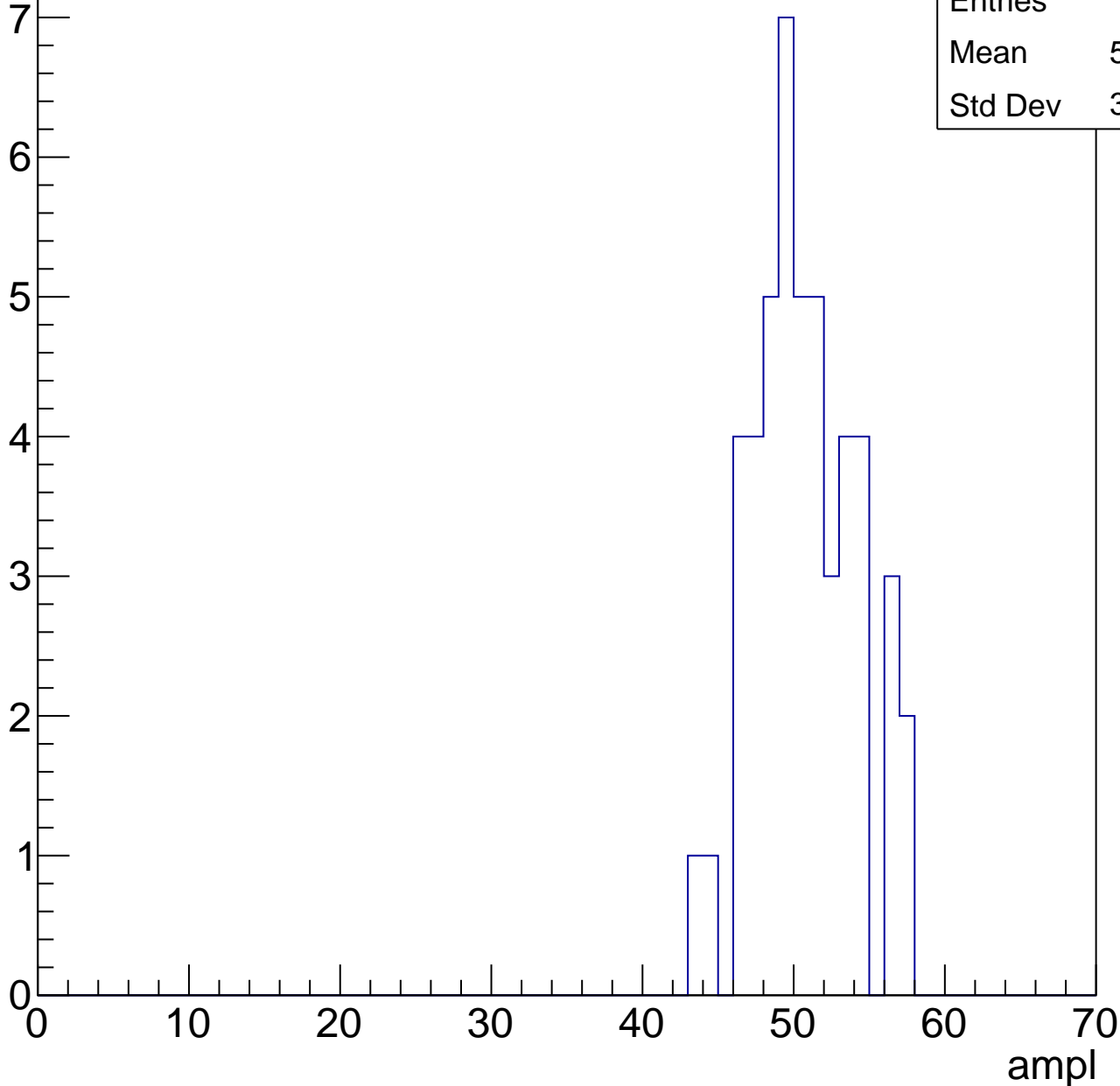


# B1L102S, U12-ch127, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	48
Mean	50.27
Std Dev	3.328



# B1L102S, U12-ch127, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

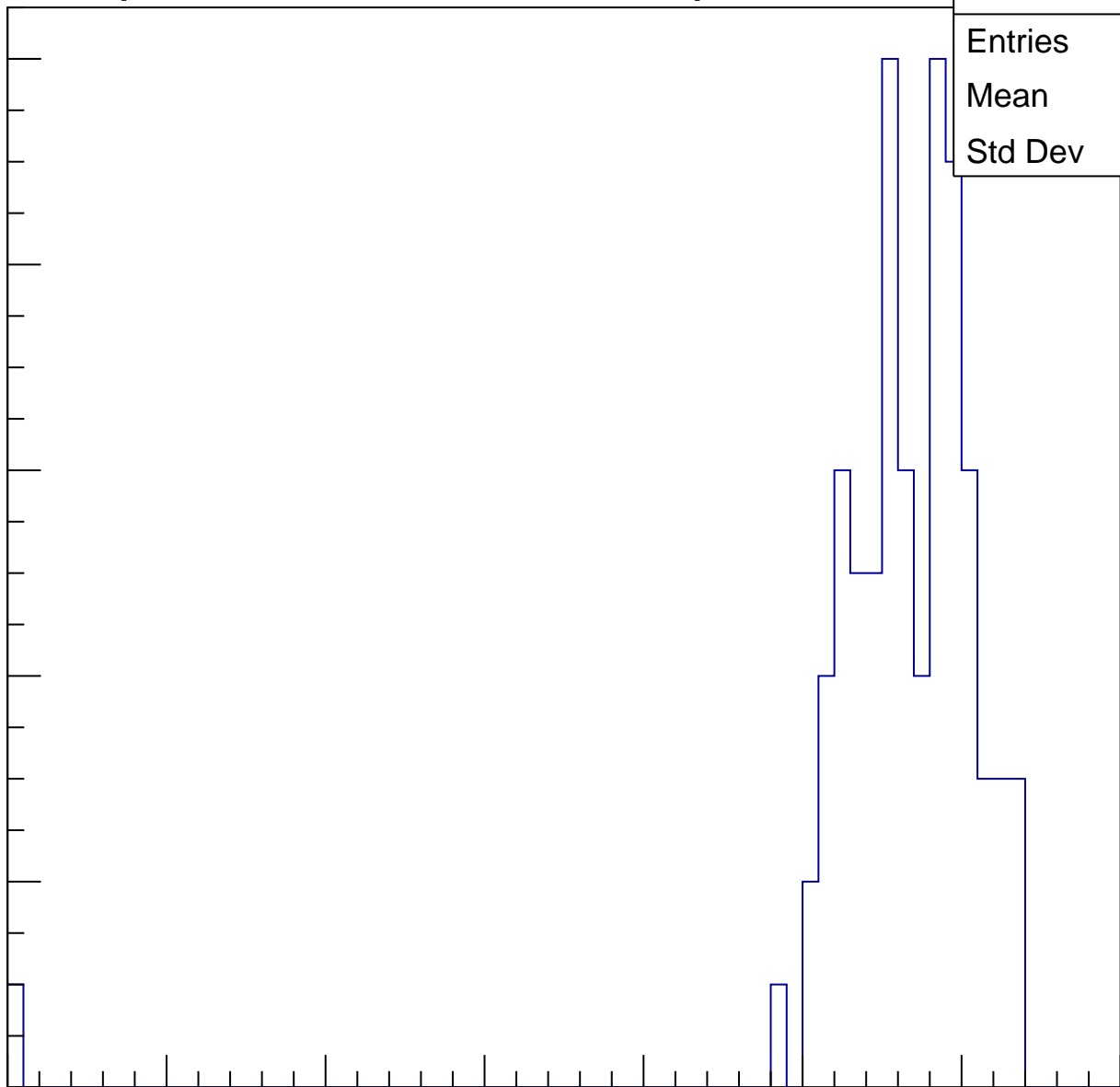
Entries	78
Mean	55.67
Std Dev	7.237

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

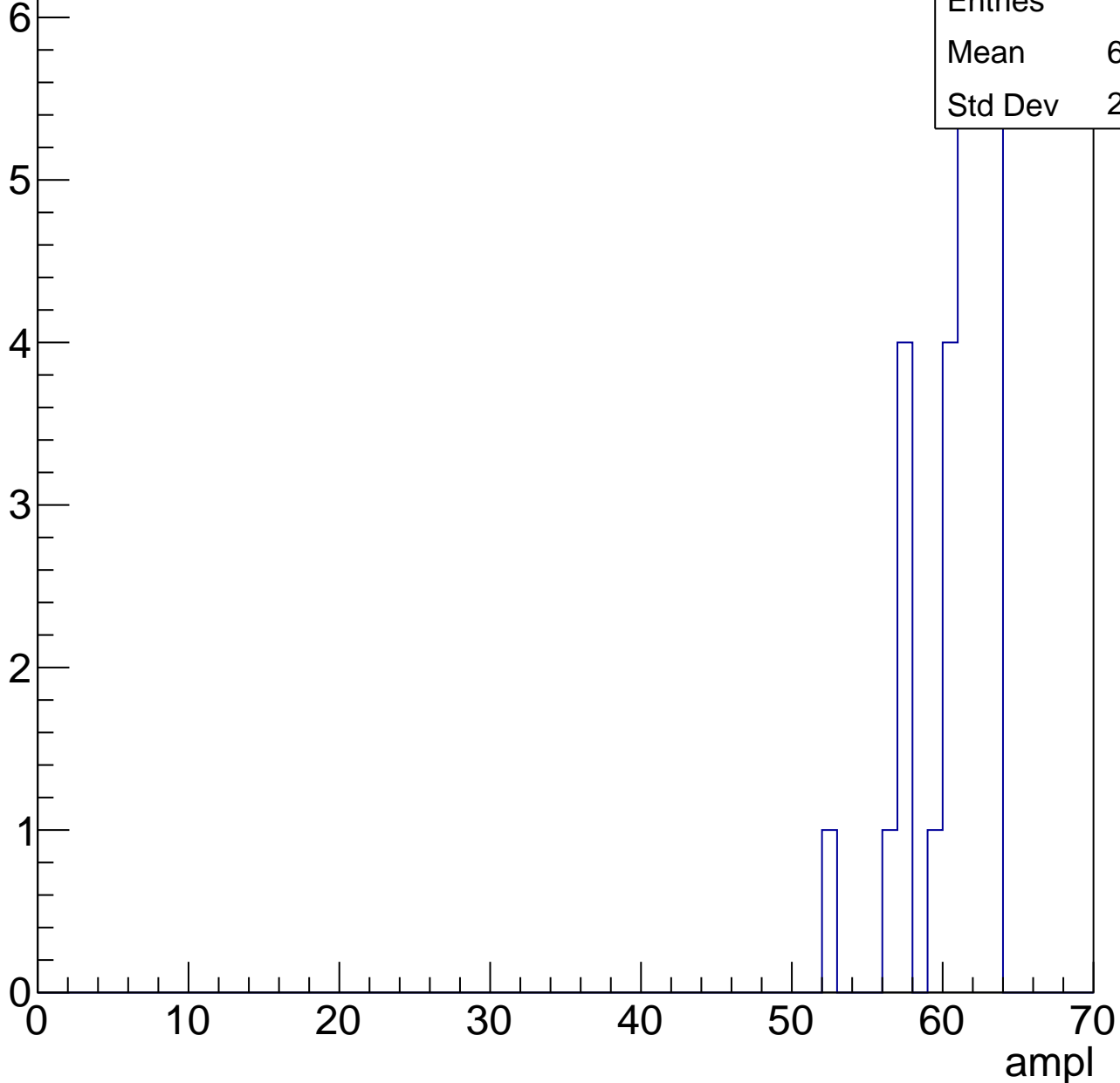


# B1L102S, U12-ch127, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	29
Mean	60.38
Std Dev	2.605



# B1L102S, U12-ch127, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U12-ch127, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U12-ch127, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0