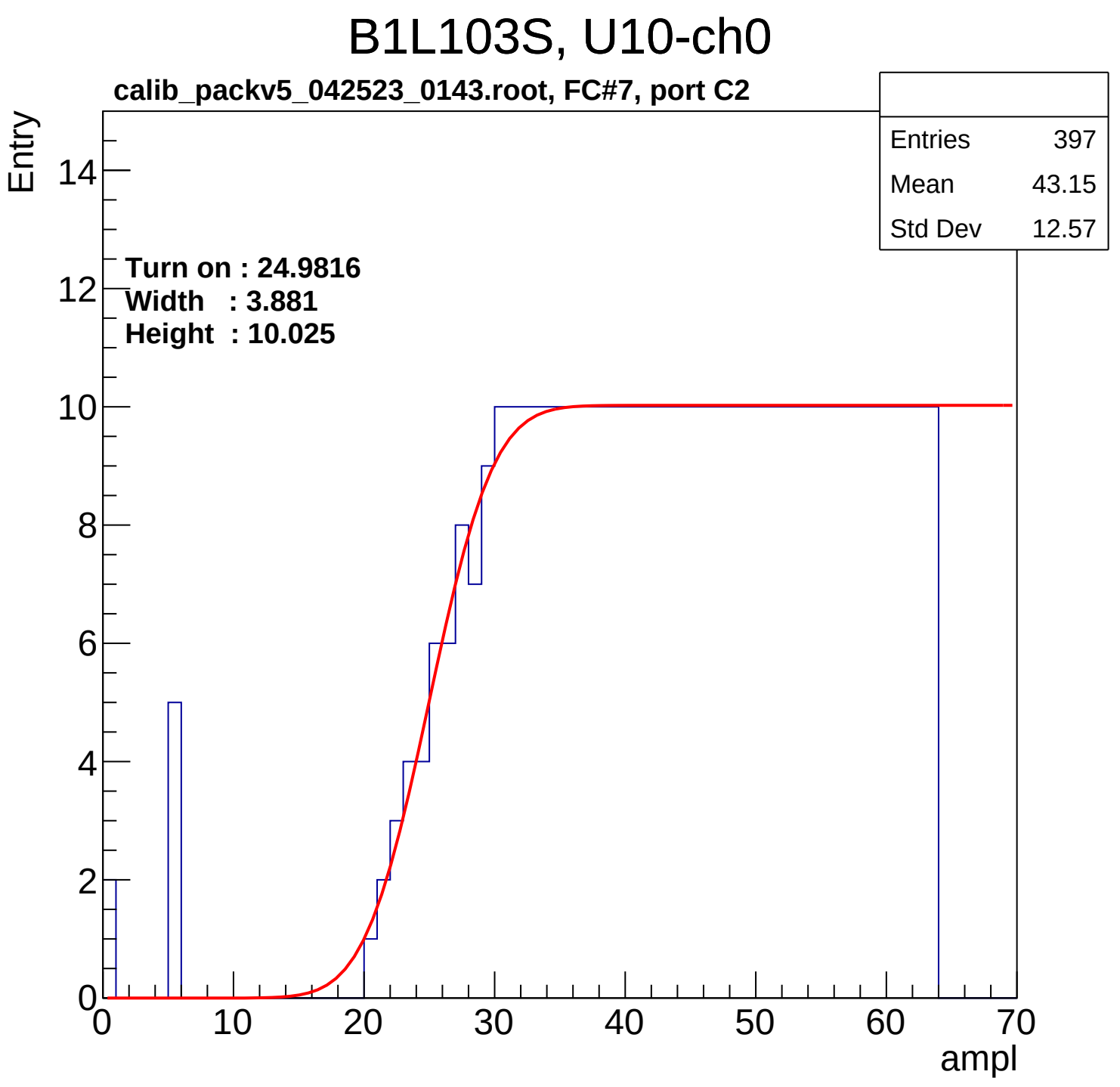
B1L103S, U10-ch0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 397
Mean 43.15
Std Dev 12.57
Turn on : 24.9816
Width : 3.881
Height : 10.025
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ampl
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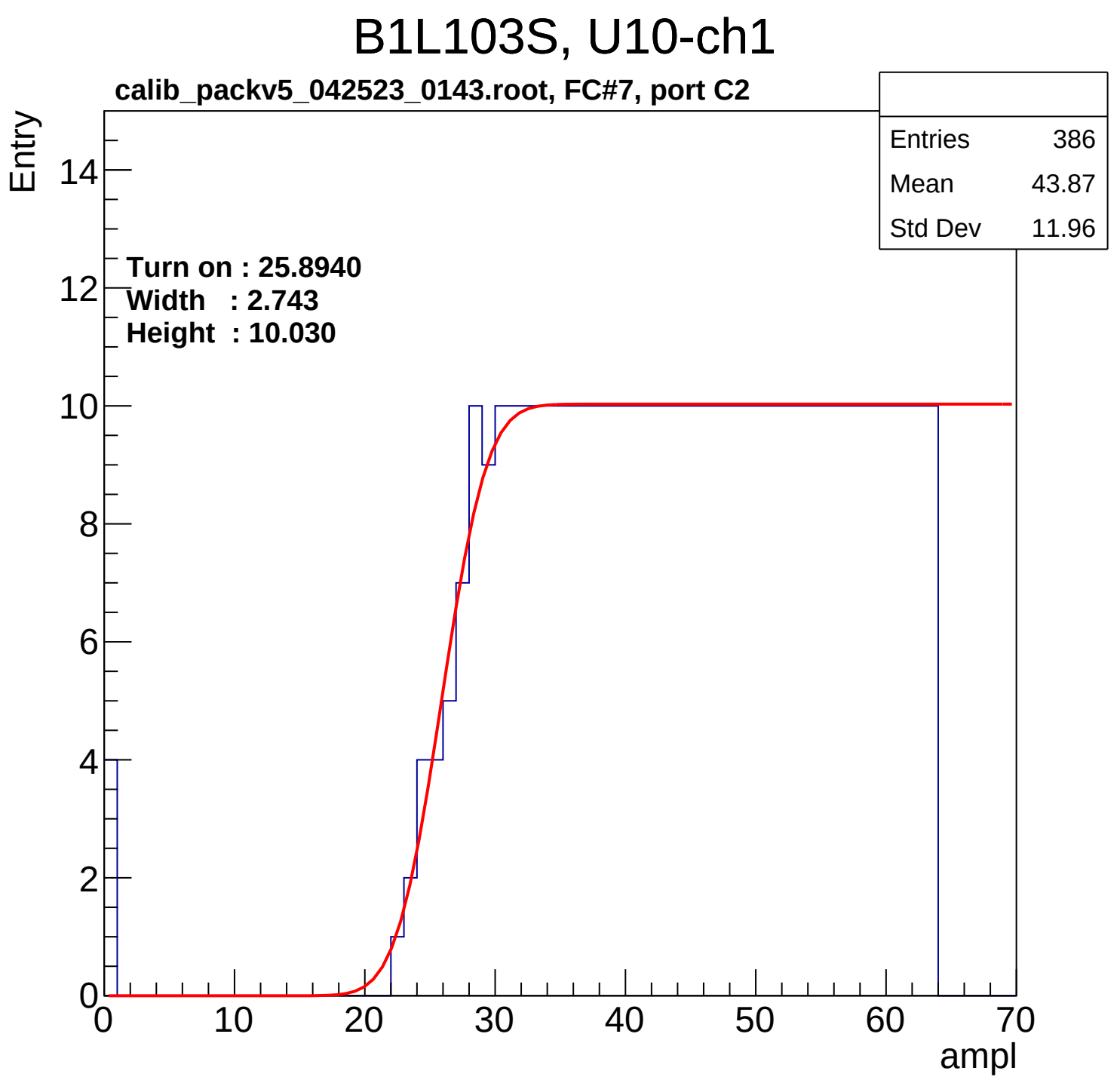
B1L103S, U10-ch1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 386
Mean 43.87
Std Dev 11.96
Turn on : 25.8940
Width : 2.743
Height : 10.030
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ampl
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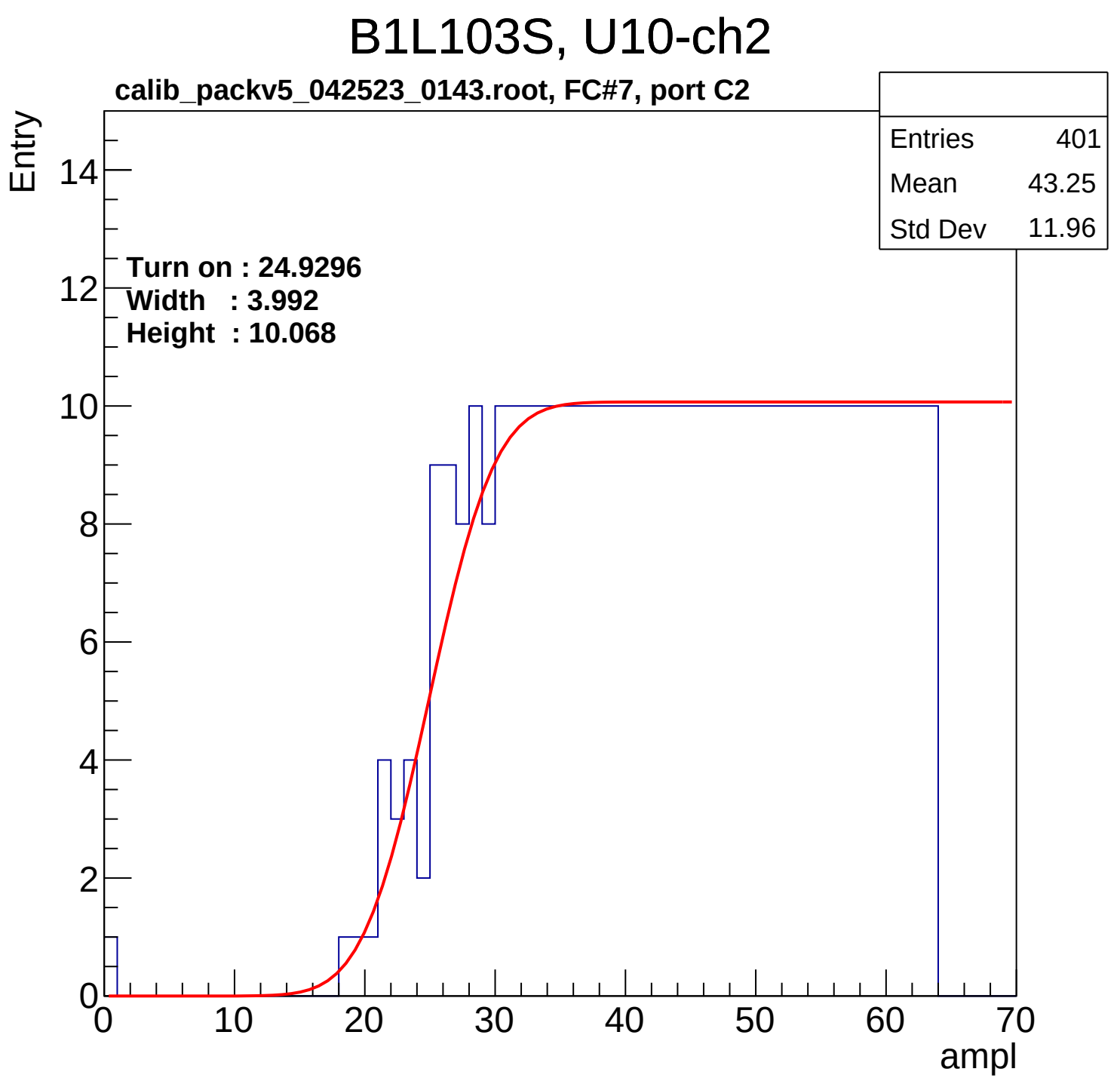
B1L103S, U10-ch2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 401
Mean 43.25
Std Dev 11.96
Turn on : 24.9296
Width : 3.992
Height : 10.068
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ampl
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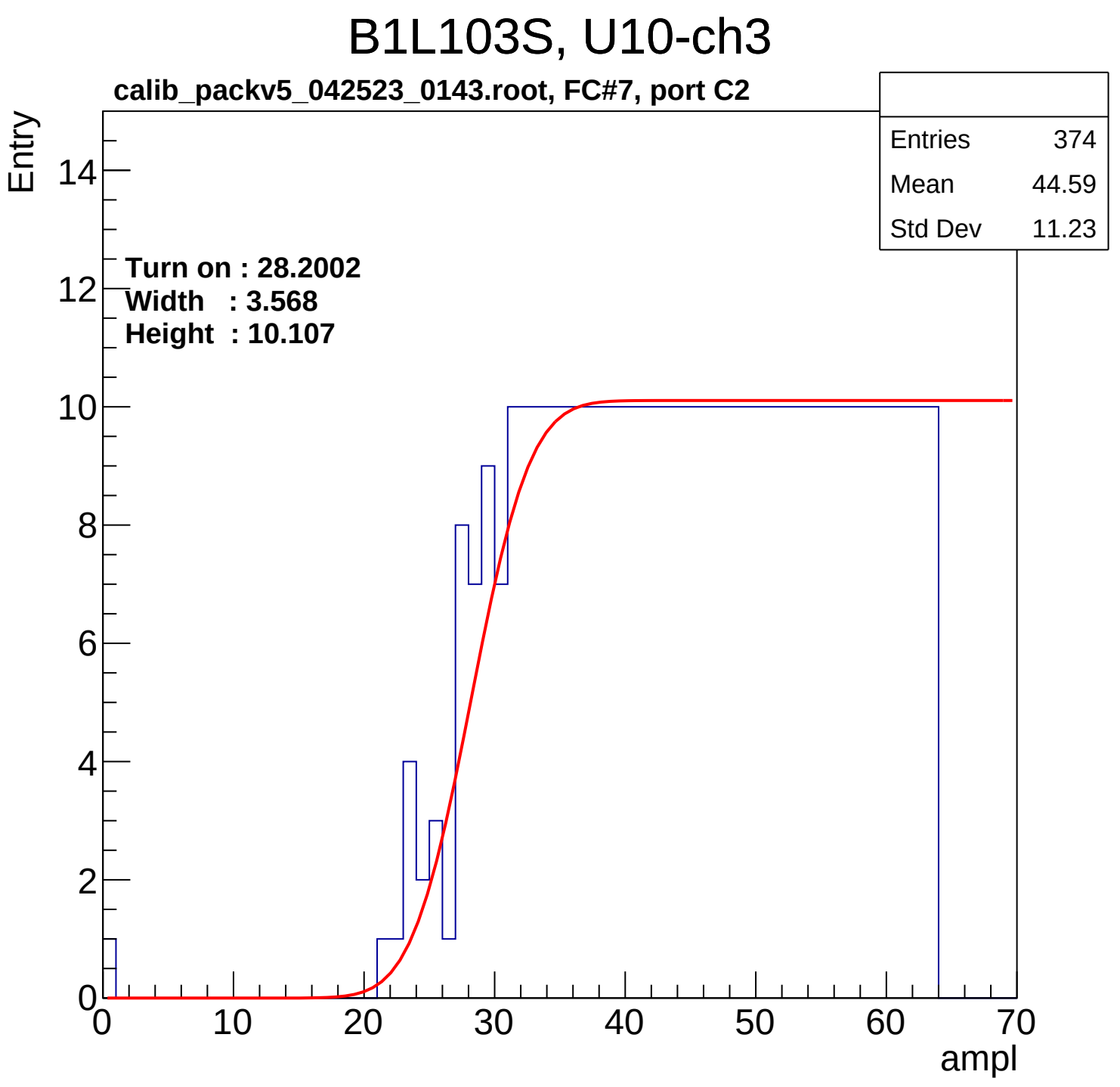
B1L103S, U10-ch3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 374
Mean 44.59
Std Dev 11.23
Turn on : 28.2002
Width : 3.568
Height : 10.107
Entry
ampl
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2
4
6
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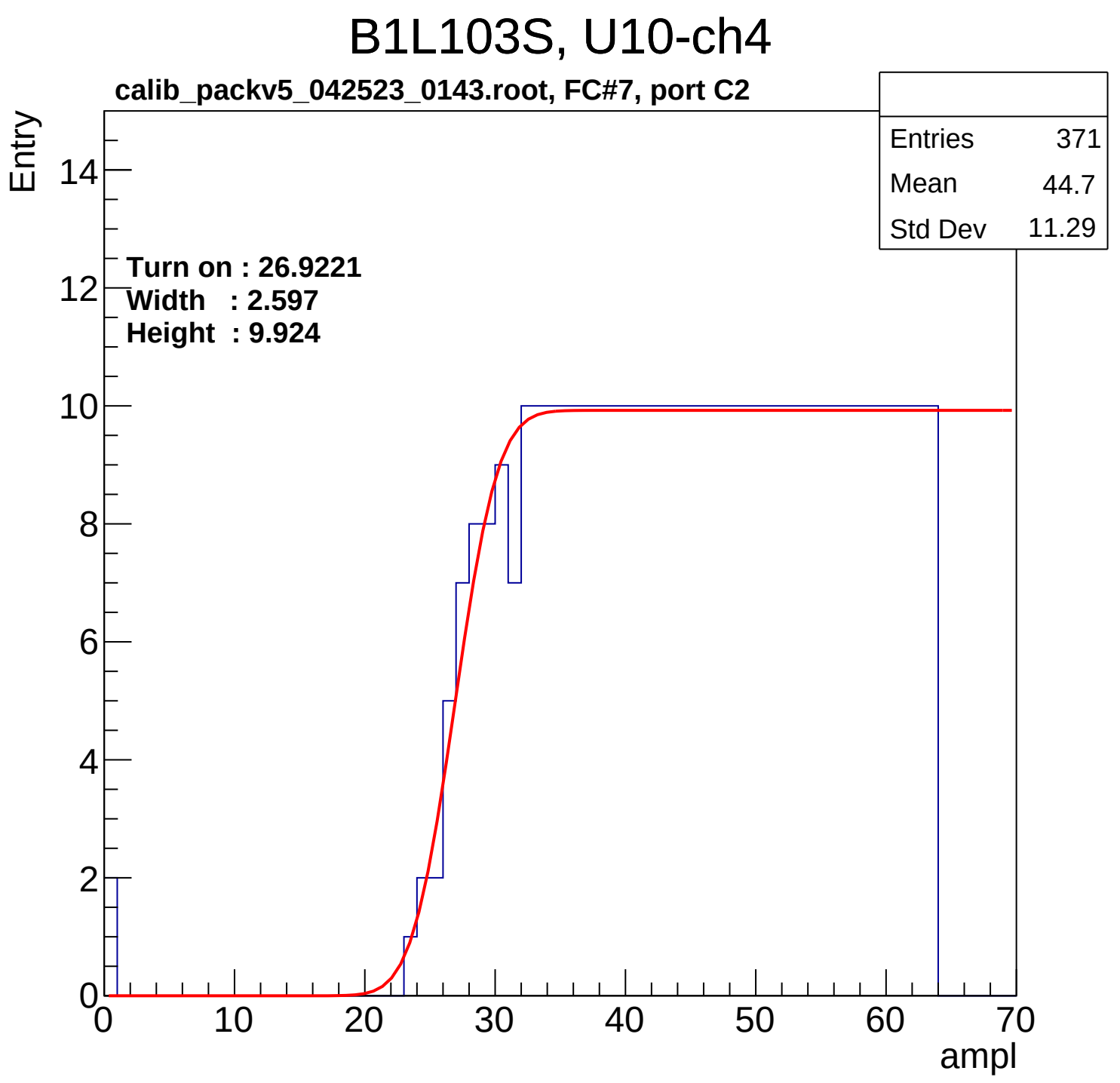
B1L103S, U10-ch4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 371
Mean 44.7
Std Dev 11.29
Turn on : 26.9221
Width : 2.597
Height : 9.924
Entry
ampl
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2
4
6
8
10
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0
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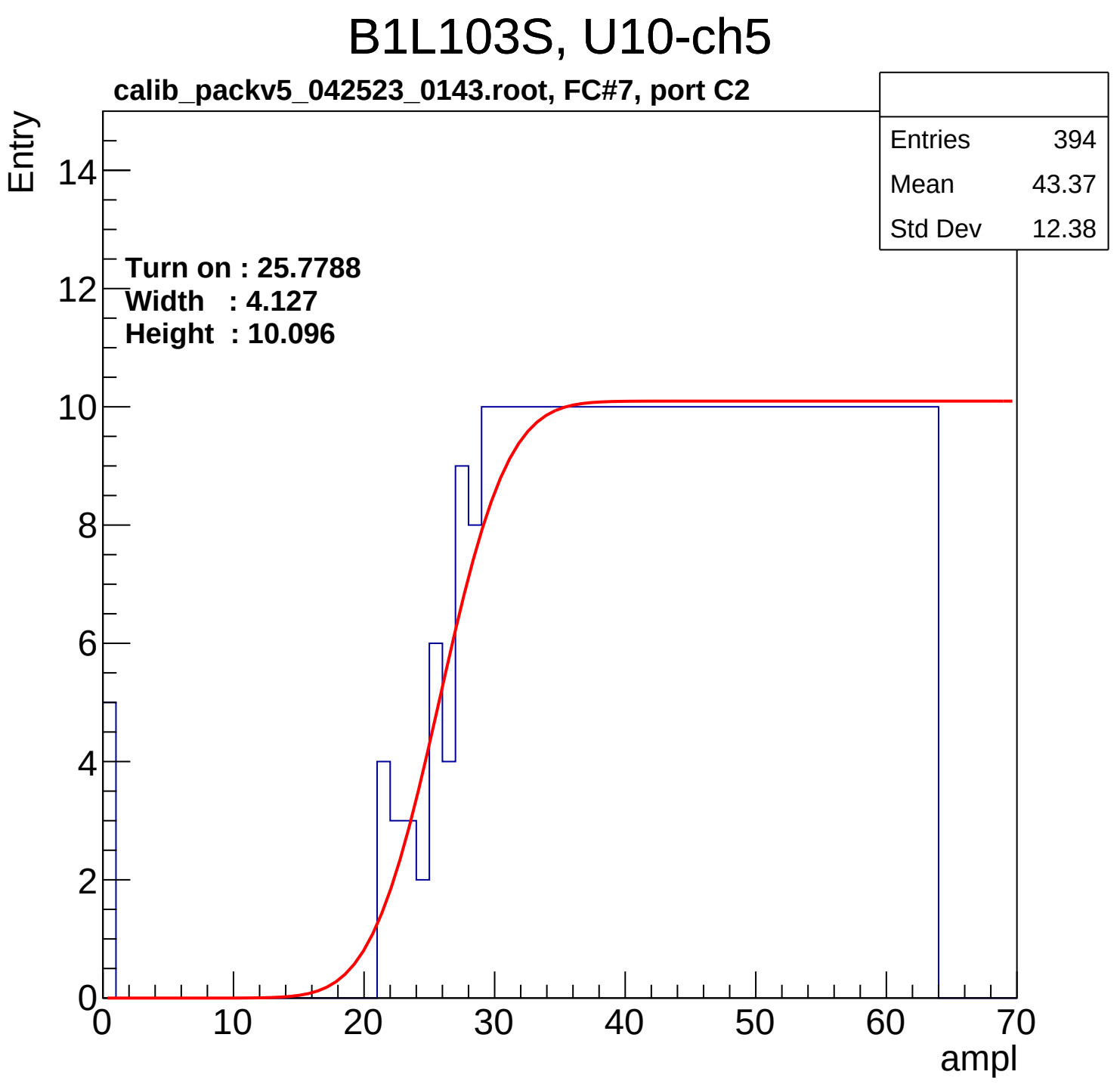
B1L103S, U10-ch5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 394
Mean 43.37
Std Dev 12.38
Turn on : 25.7788
Width : 4.127
Height : 10.096
Entry
ampl
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2
4
6
8
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0
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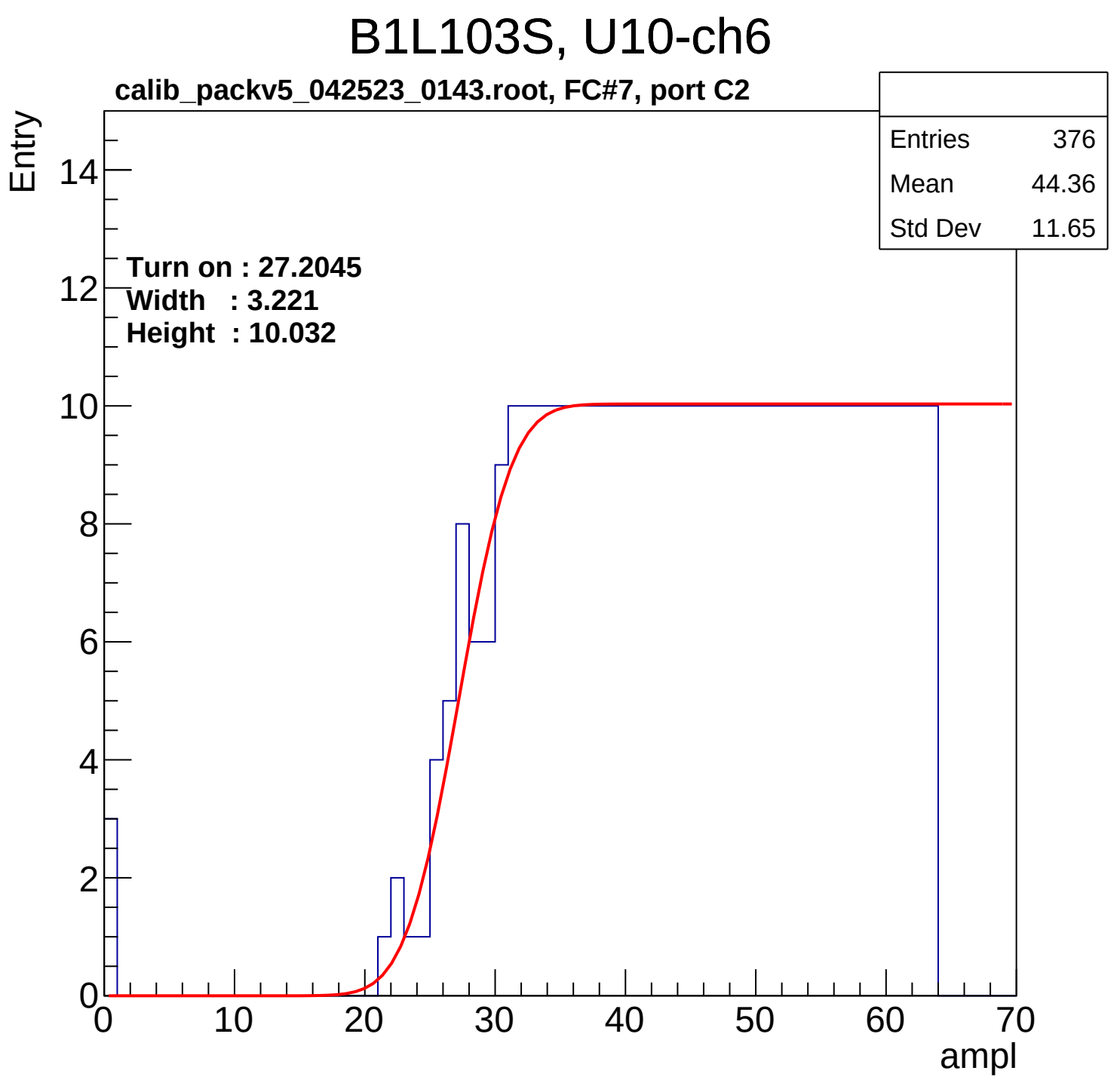
B1L103S, U10-ch6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 376
Mean 44.36
Std Dev 11.65
Turn on : 27.2045
Width : 3.221
Height : 10.032
Entry
ampl
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4
6
8
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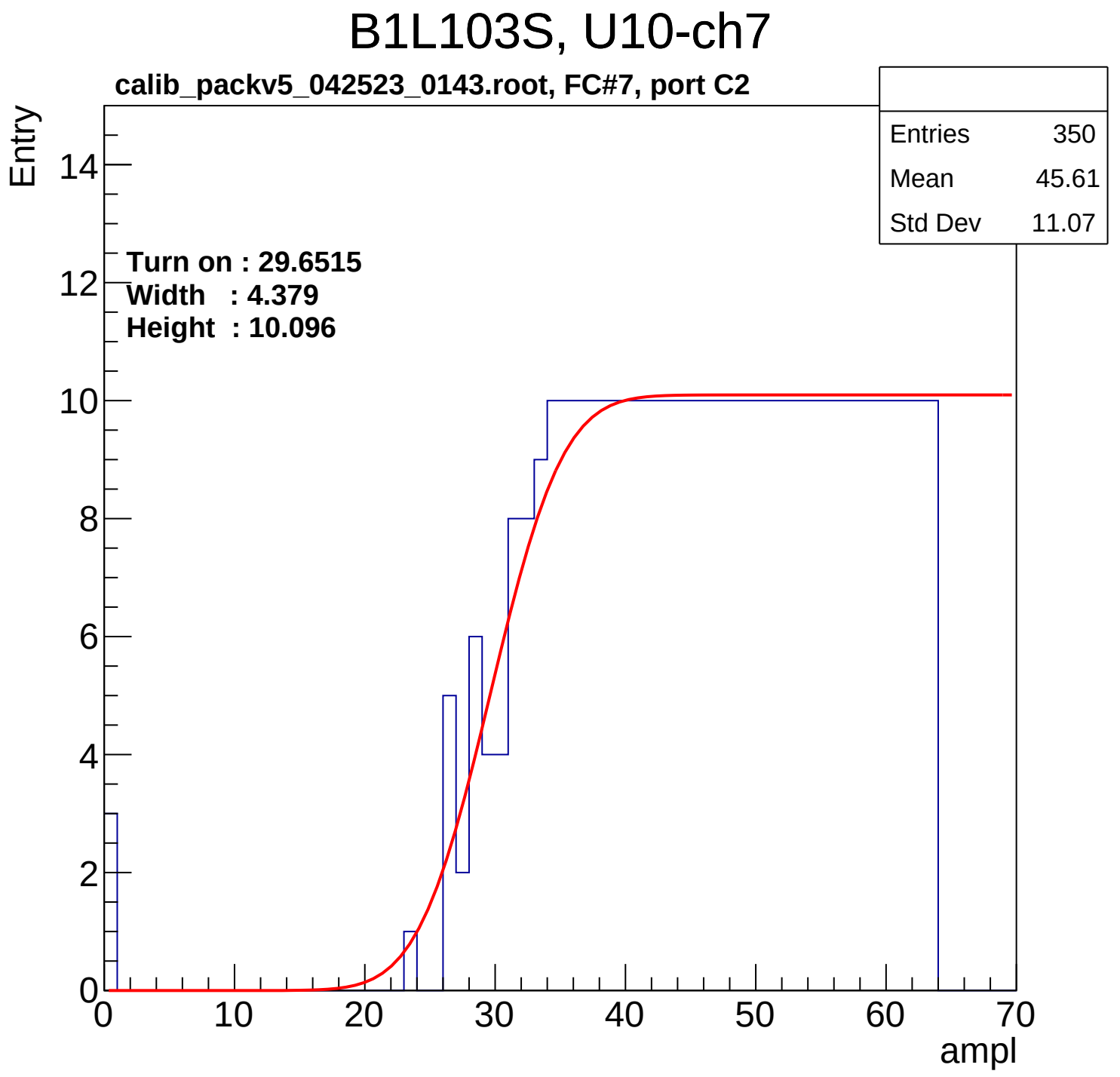
B1L103S, U10-ch7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 350
Mean 45.61
Std Dev 11.07
Turn on : 29.6515
Width : 4.379
Height : 10.096
Entry
ampl
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4
6
8
10
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60
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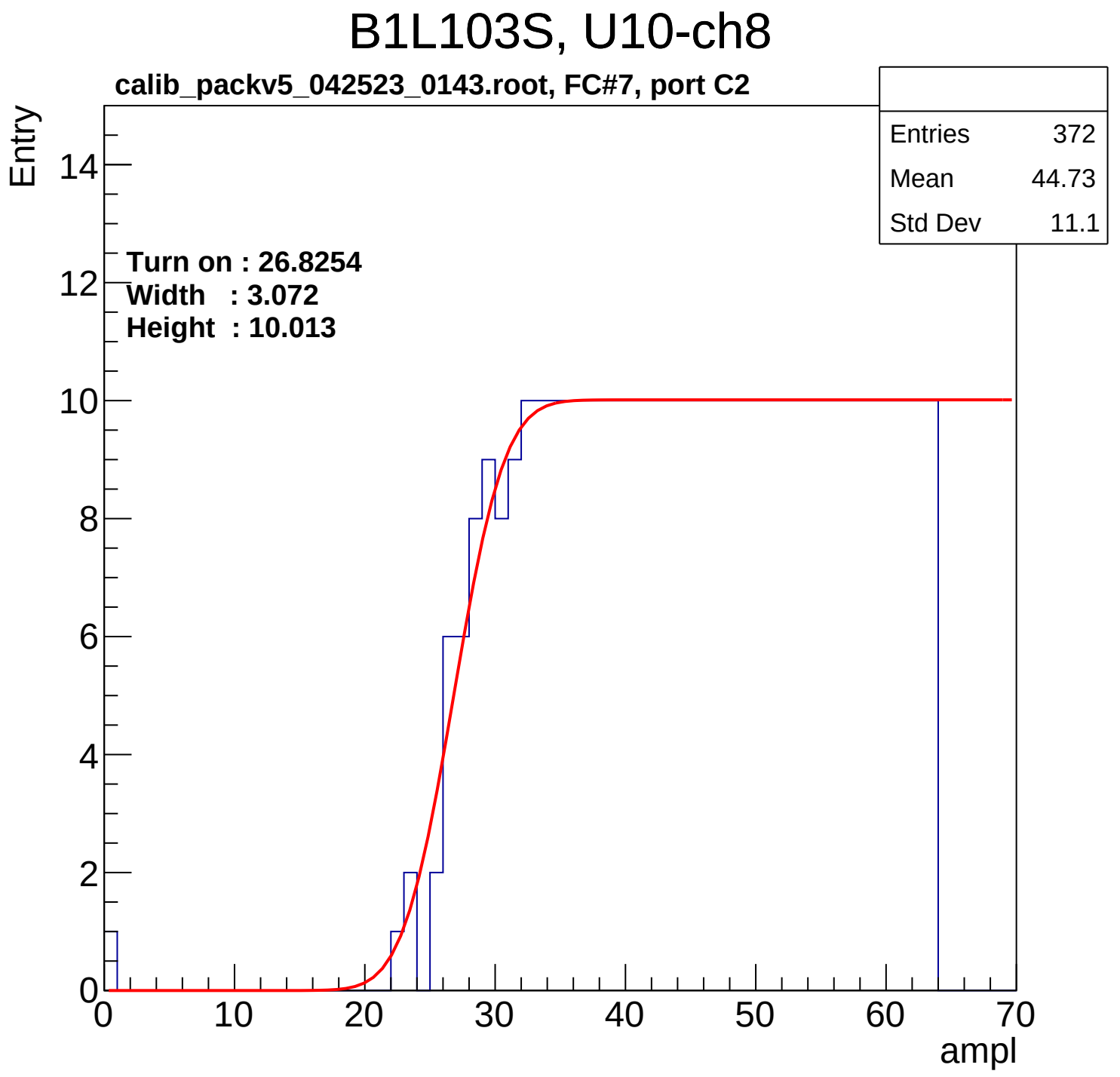
B1L103S, U10-ch8
calib_packv5_042523_0143.root, FC#7, port C2
Entries 372
Mean 44.73
Std Dev 11.1
Turn on : 26.8254
Width : 3.072
Height : 10.013
Entry
ampl
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6
8
10
12
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60
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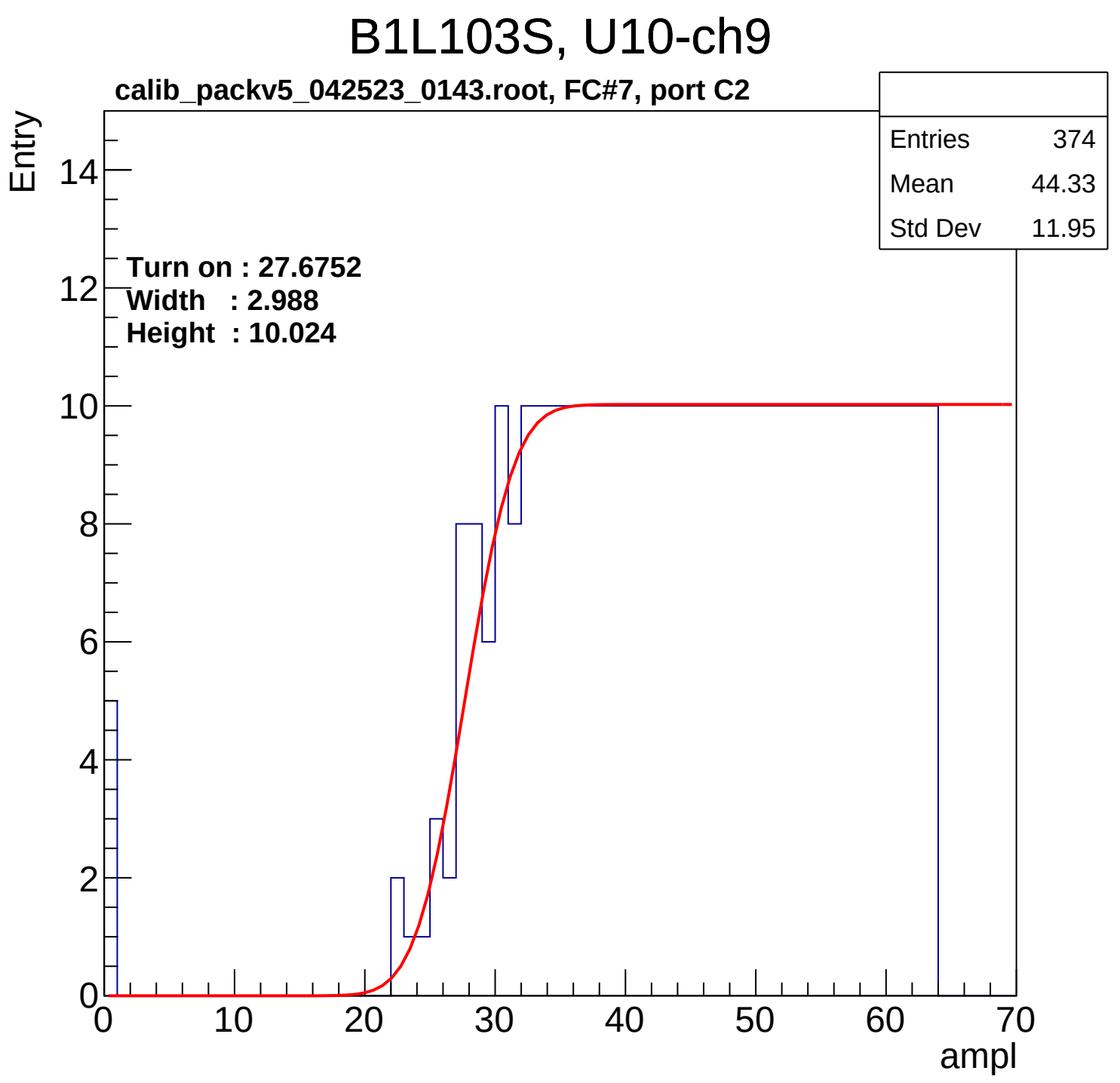
B1L103S, U10-ch9
calib_packv5_042523_0143.root, FC#7, port C2
Entries 374
Mean 44.33
Std Dev 11.95
Turn on : 27.6752
Width : 2.988
Height : 10.024
Entry
ampl
0
2
4
6
8
10
12
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0
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20
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60
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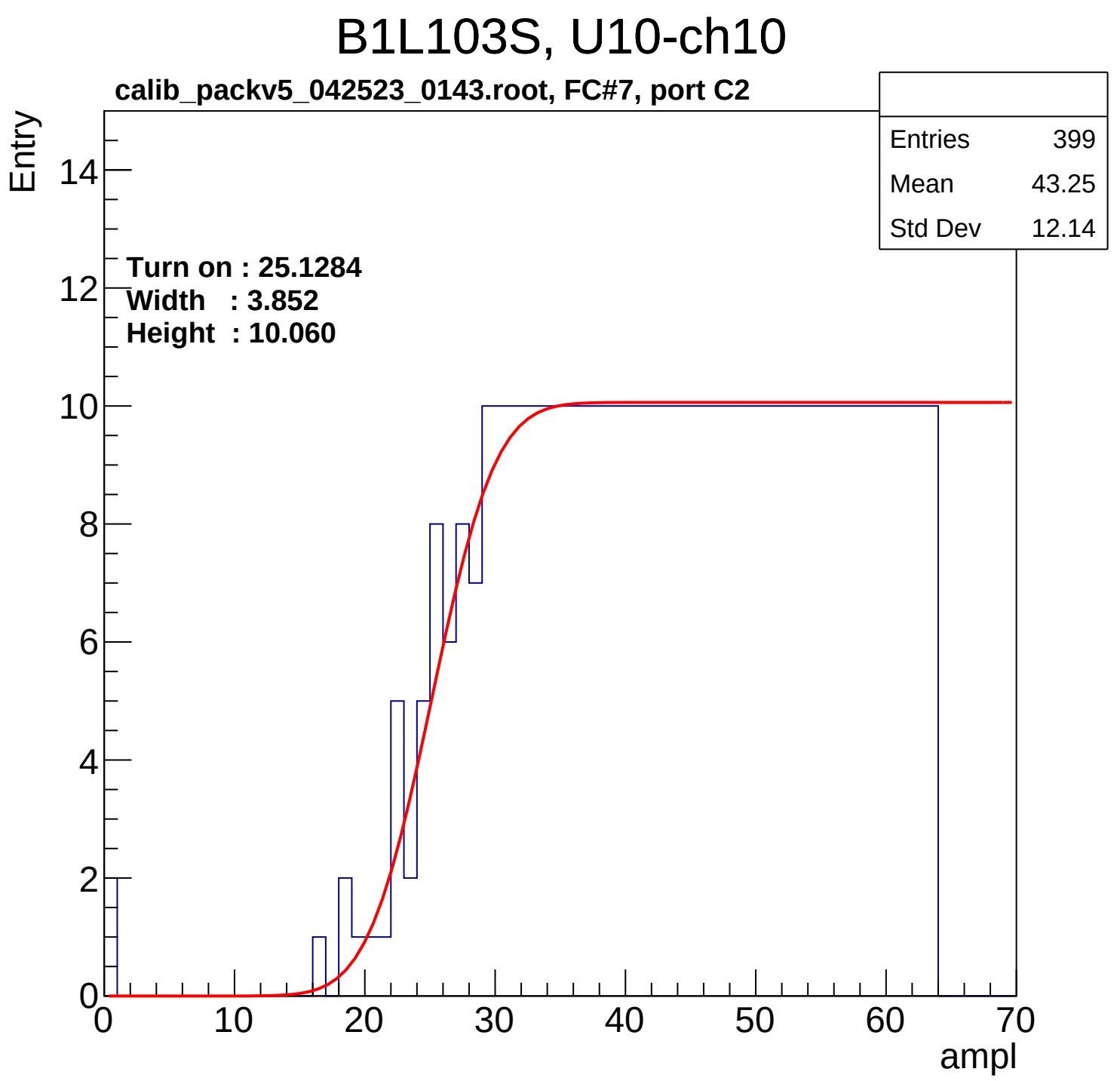
B1L103S, U10-ch10
calib_packv5_042523_0143.root, FC#7, port C2
Entries 399
Mean 43.25
Std Dev 12.14
Turn on : 25.1284
Width : 3.852
Height : 10.060
Entry
ampl
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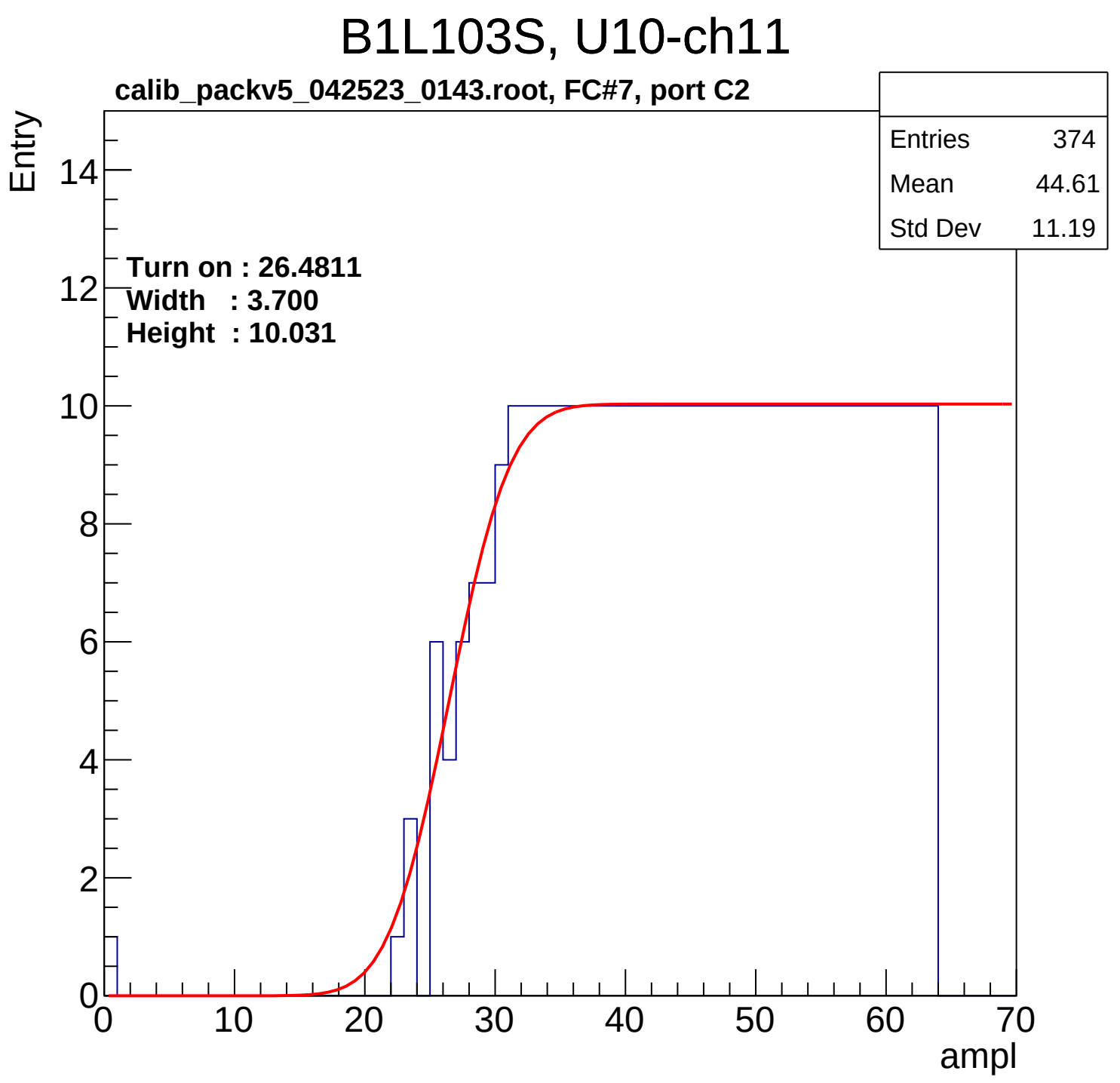
B1L103S, U10-ch11
calib_packv5_042523_0143.root, FC#7, port C2
Entries 374
Mean 44.61
Std Dev 11.19
Turn on : 26.4811
Width : 3.700
Height : 10.031
Entry
ampl
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6
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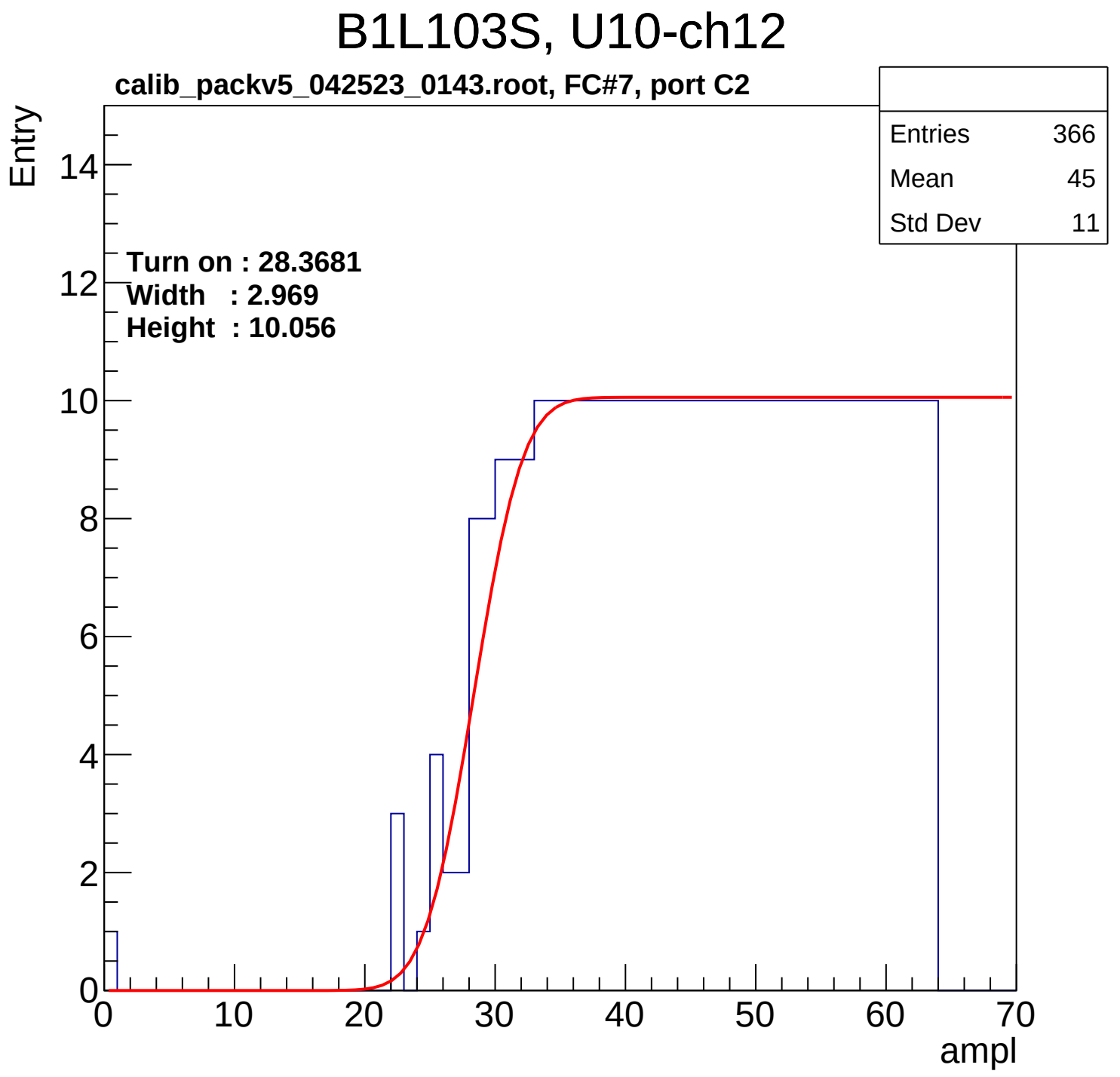
B1L103S, U10-ch12
calib_packv5_042523_0143.root, FC#7, port C2
Entries 366
Mean 45
Std Dev 11
Turn on : 28.3681
Width : 2.969
Height : 10.056
Entry
ampl
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2
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6
8
10
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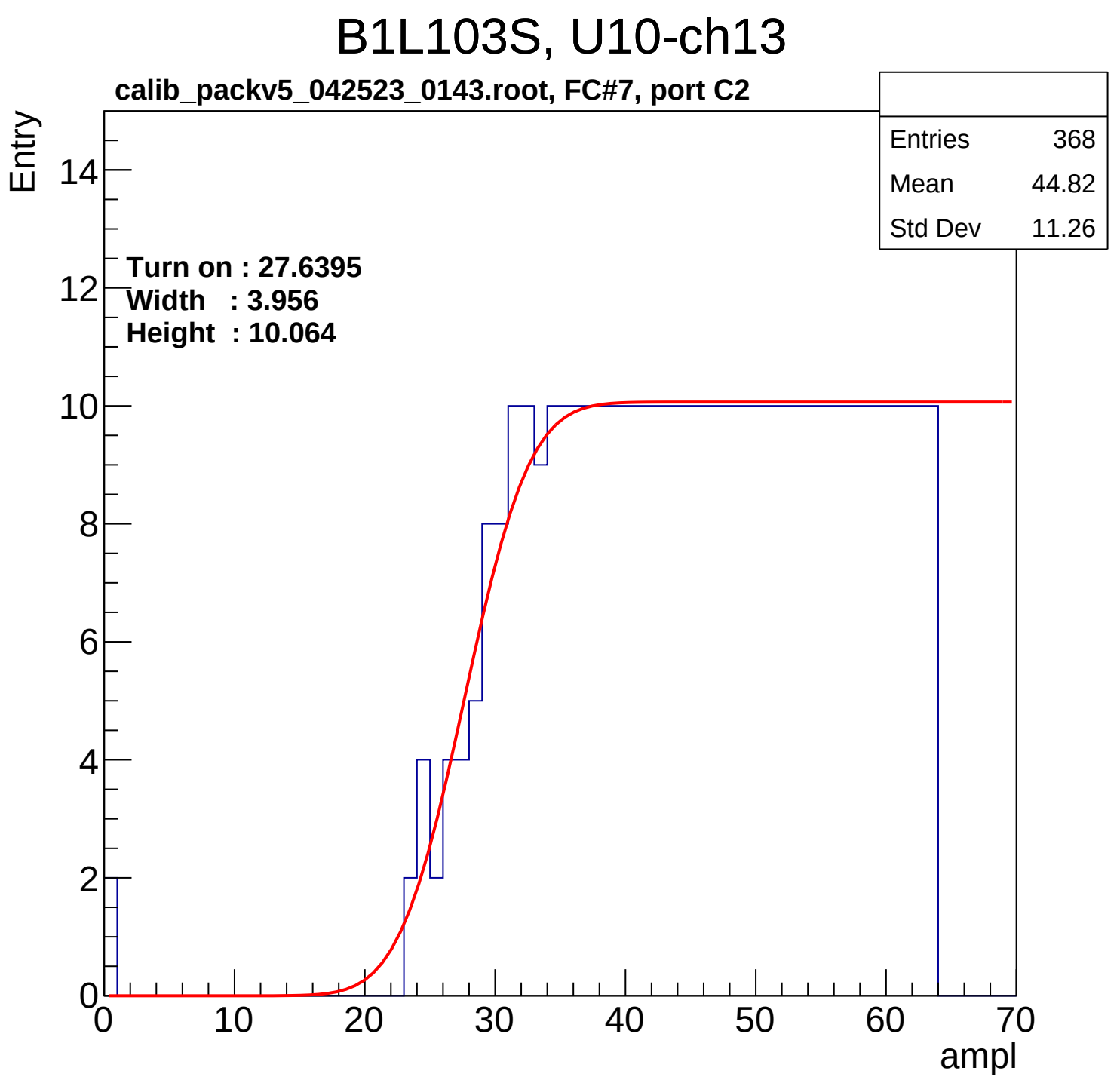
B1L103S, U10-ch13
calib_packv5_042523_0143.root, FC#7, port C2
Entries 368
Mean 44.82
Std Dev 11.26
Turn on : 27.6395
Width : 3.956
Height : 10.064
Entry
ampl
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6
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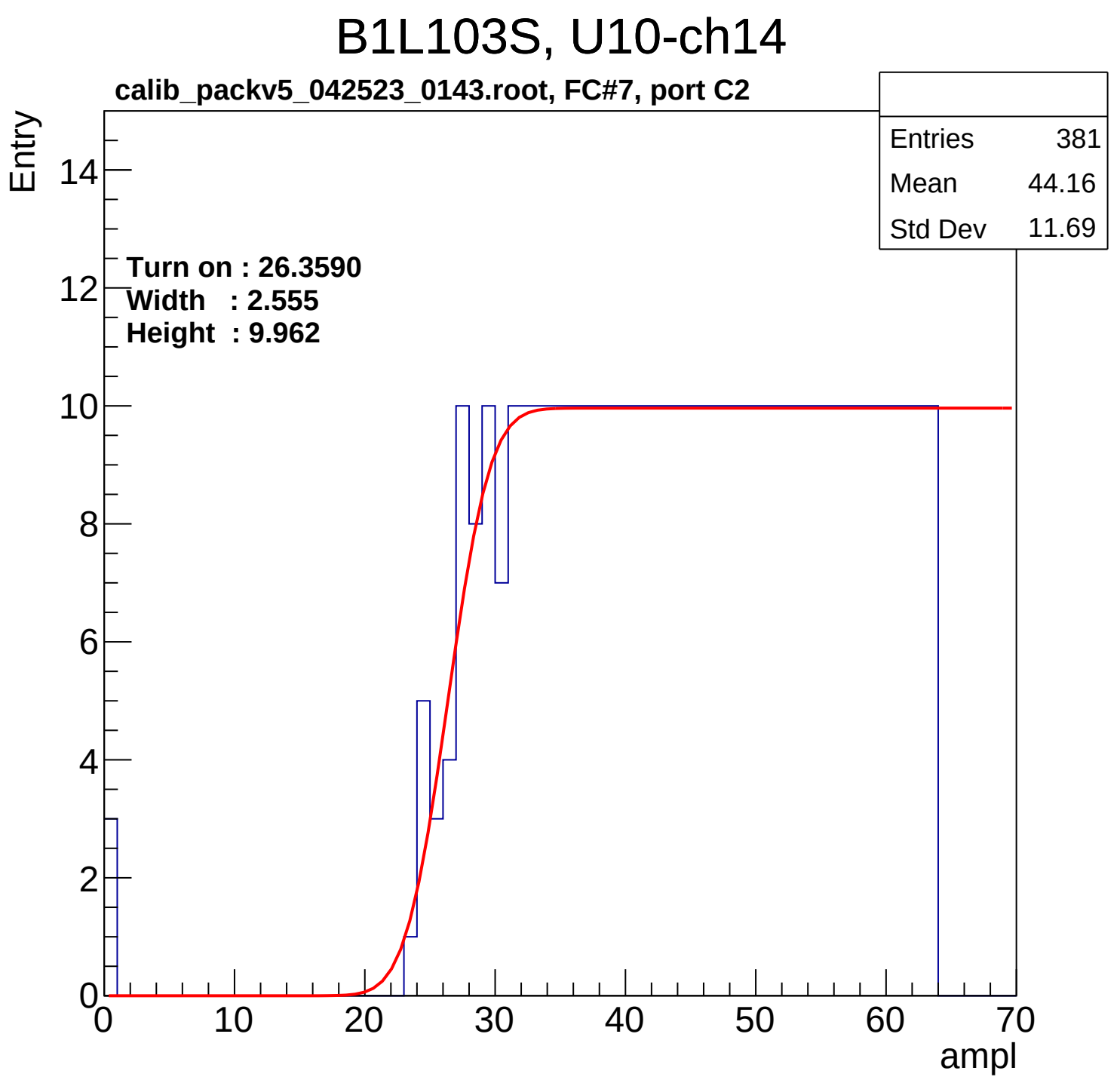
B1L103S, U10-ch14
calib_packv5_042523_0143.root, FC#7, port C2
Entries 381
Mean 44.16
Std Dev 11.69
Turn on : 26.3590
Width : 2.555
Height : 9.962
Entry
ampl
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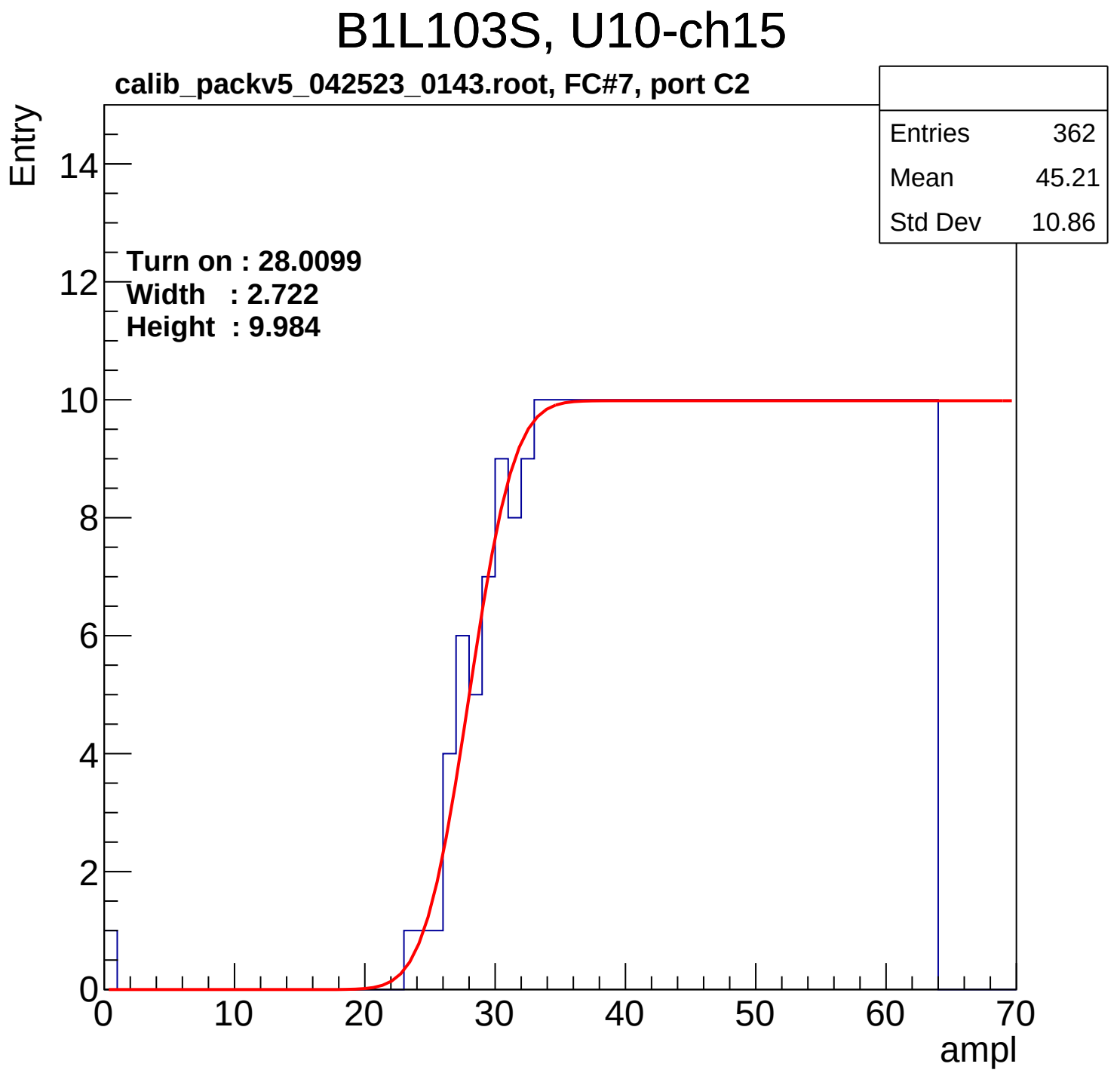
B1L103S, U10-ch15
calib_packv5_042523_0143.root, FC#7, port C2
Entries 362
Mean 45.21
Std Dev 10.86
Turn on : 28.0099
Width : 2.722
Height : 9.984
Entry
ampl
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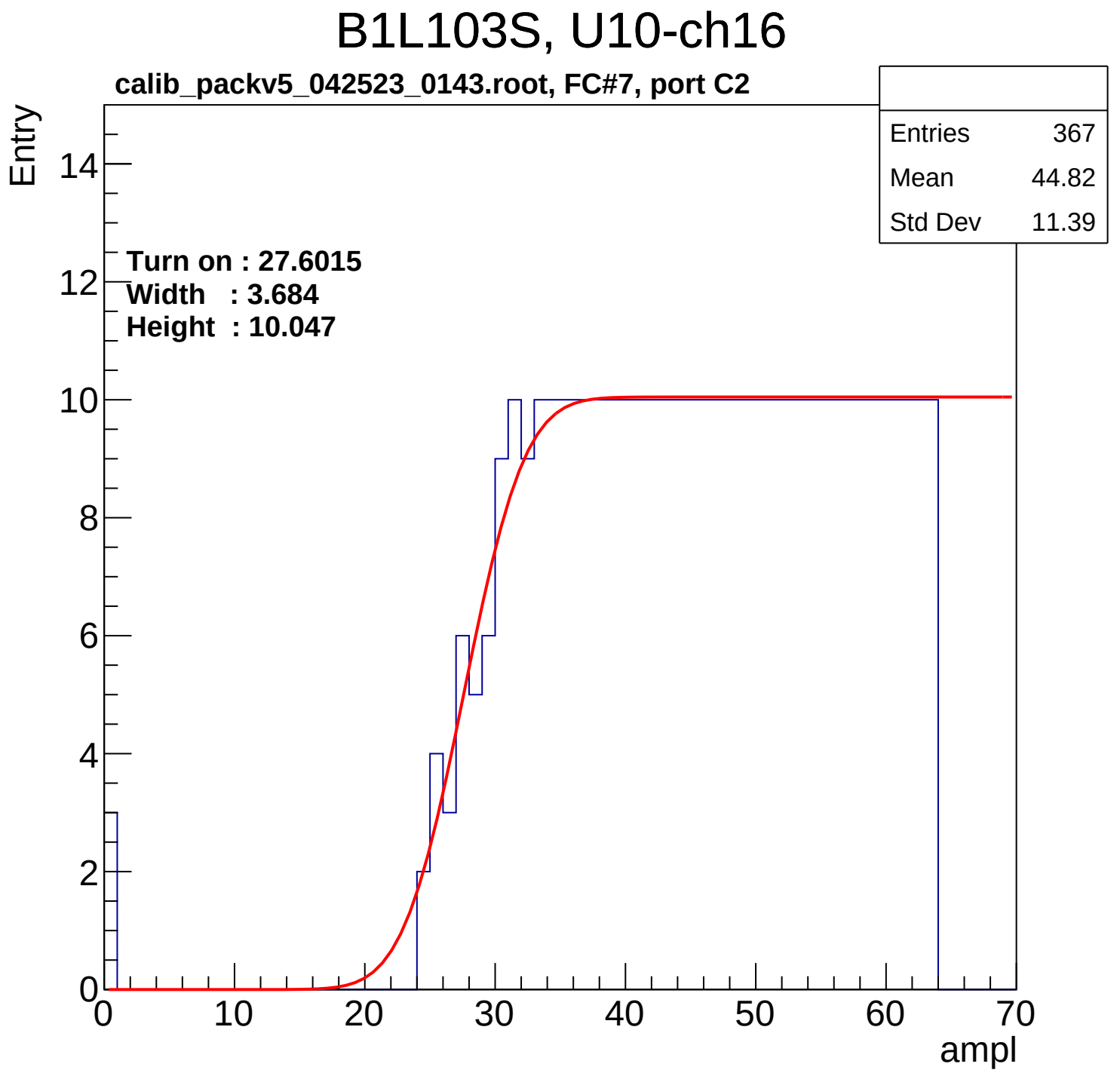
B1L103S, U10-ch16
calib_packv5_042523_0143.root, FC#7, port C2
Entries 367
Mean 44.82
Std Dev 11.39
Turn on : 27.6015
Width : 3.684
Height : 10.047
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ampl
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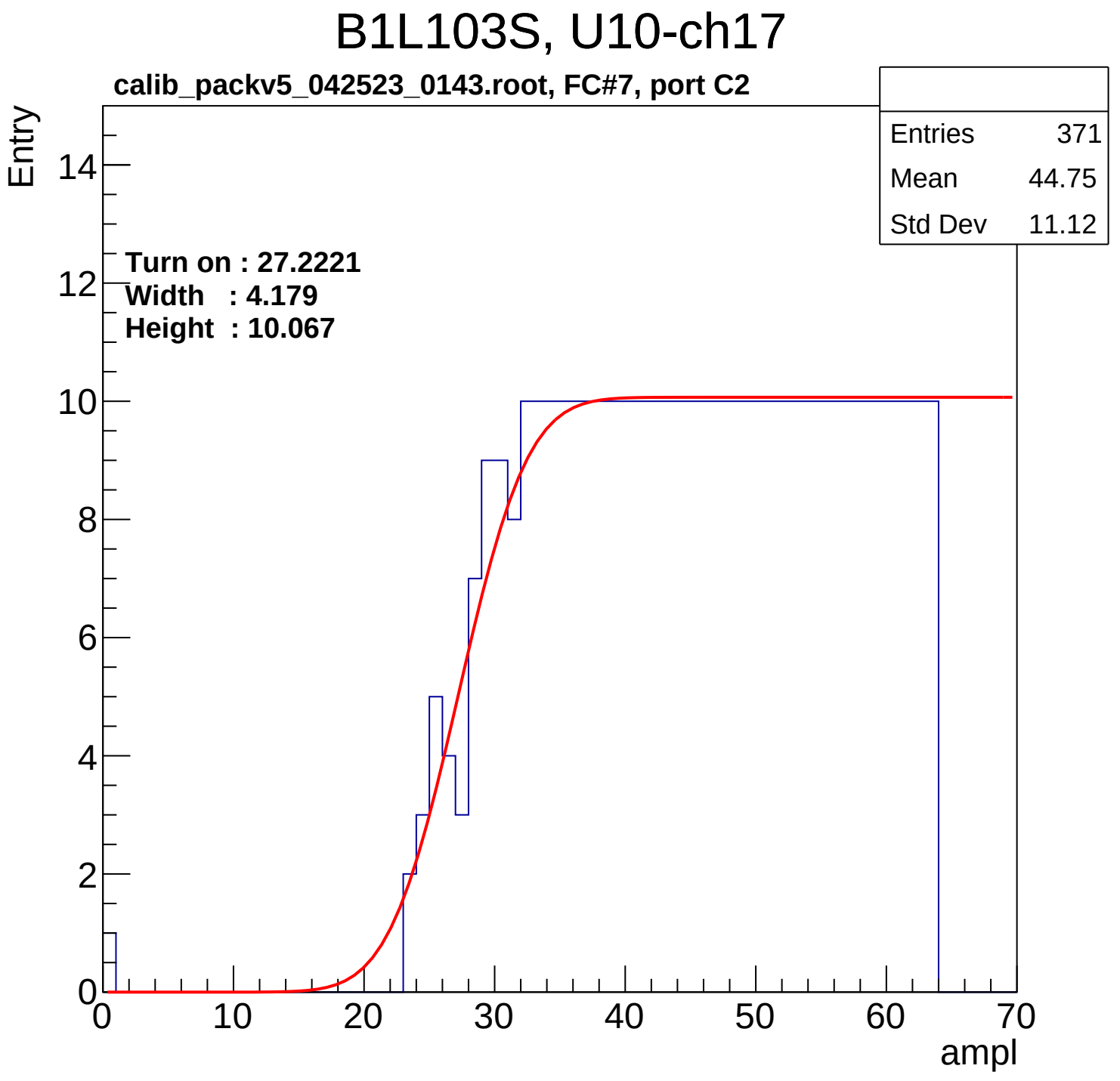
B1L103S, U10-ch17
calib_packv5_042523_0143.root, FC#7, port C2
Entries 371
Mean 44.75
Std Dev 11.12
Turn on : 27.2221
Width : 4.179
Height : 10.067
Entry
ampl
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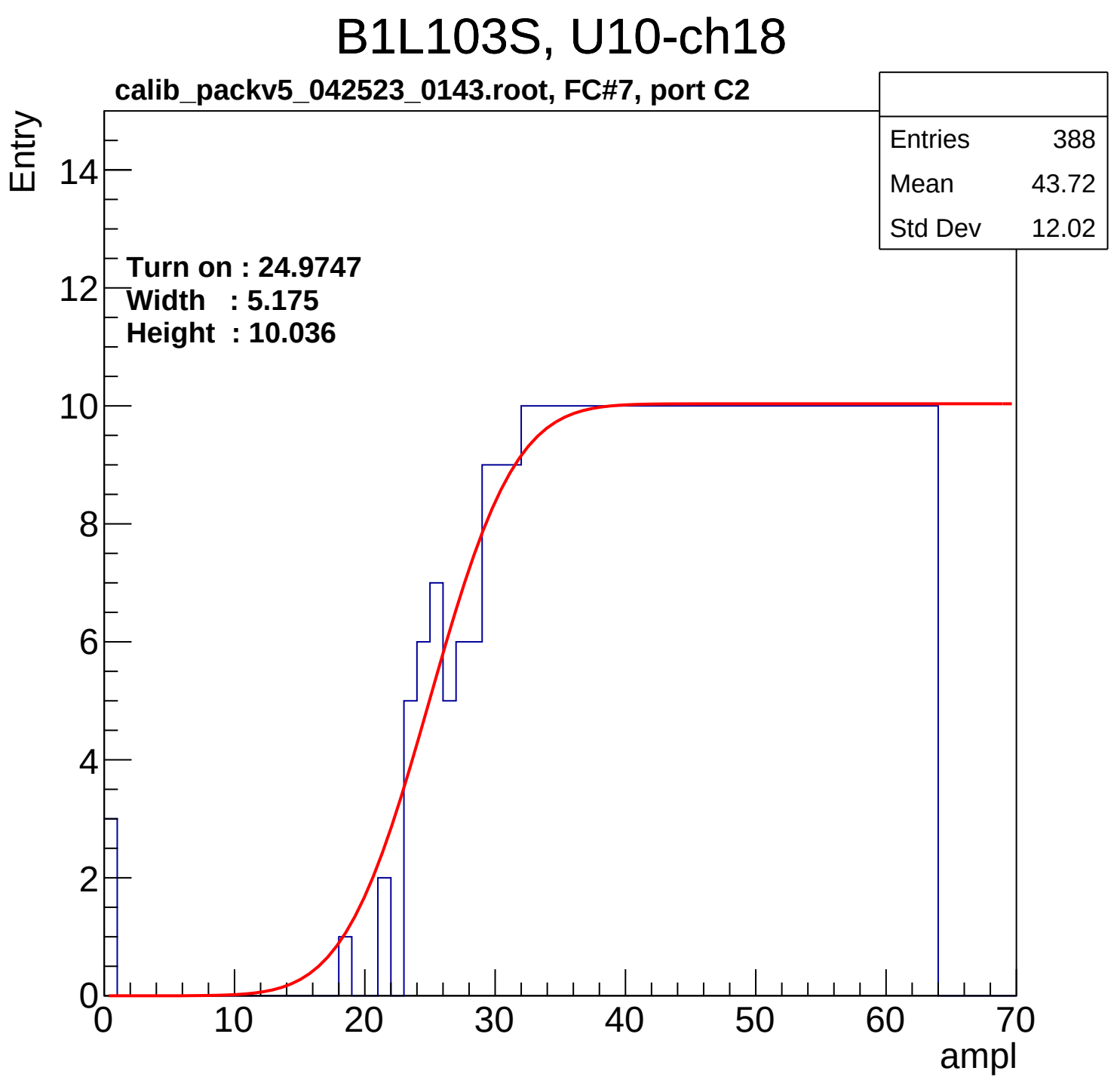
B1L103S, U10-ch18
calib_packv5_042523_0143.root, FC#7, port C2
Entries 388
Mean 43.72
Std Dev 12.02
Turn on : 24.9747
Width : 5.175
Height : 10.036
Entry
ampl
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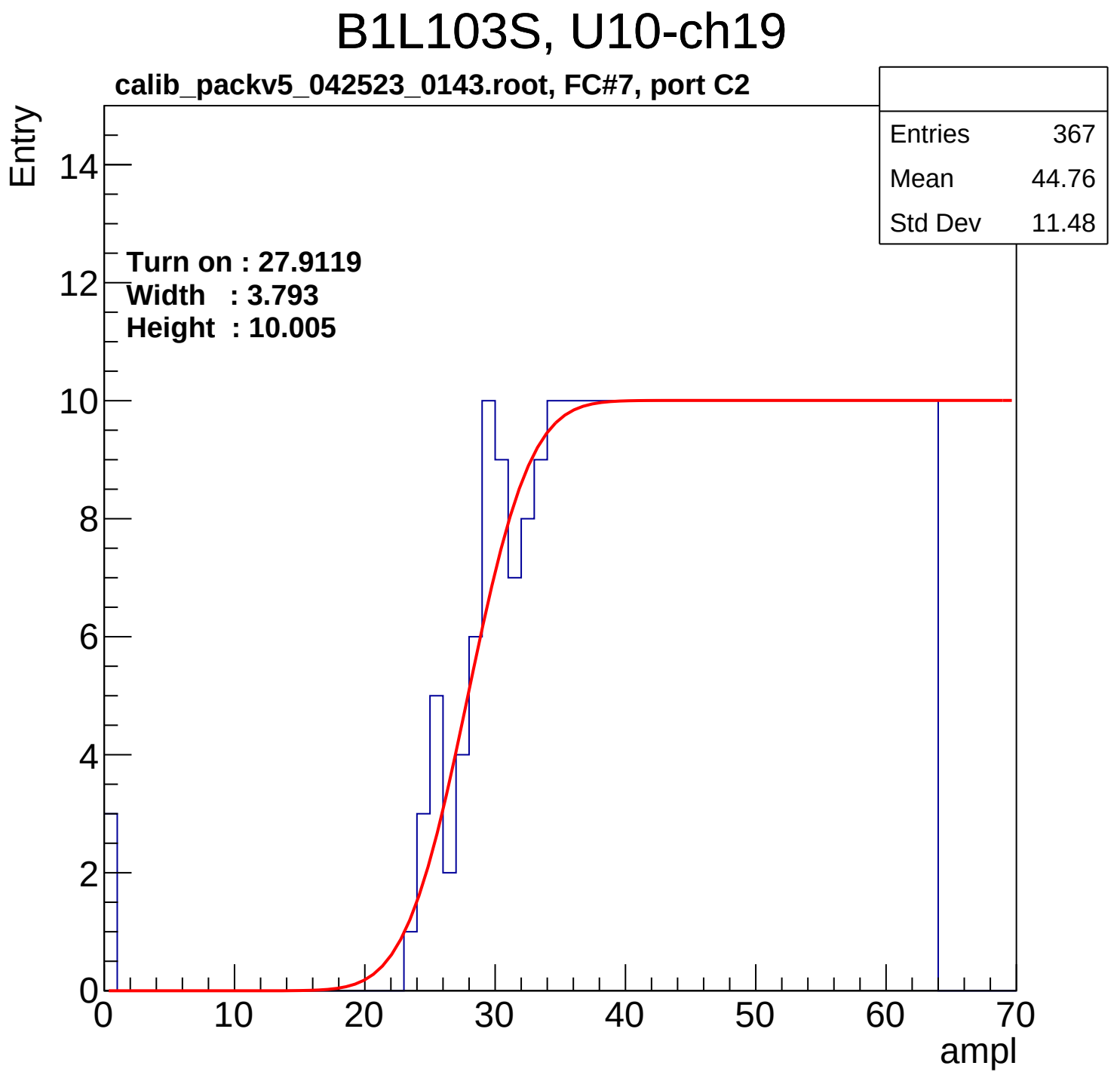
B1L103S, U10-ch19
calib_packv5_042523_0143.root, FC#7, port C2
Entries 367
Mean 44.76
Std Dev 11.48
Turn on : 27.9119
Width : 3.793
Height : 10.005
Entry
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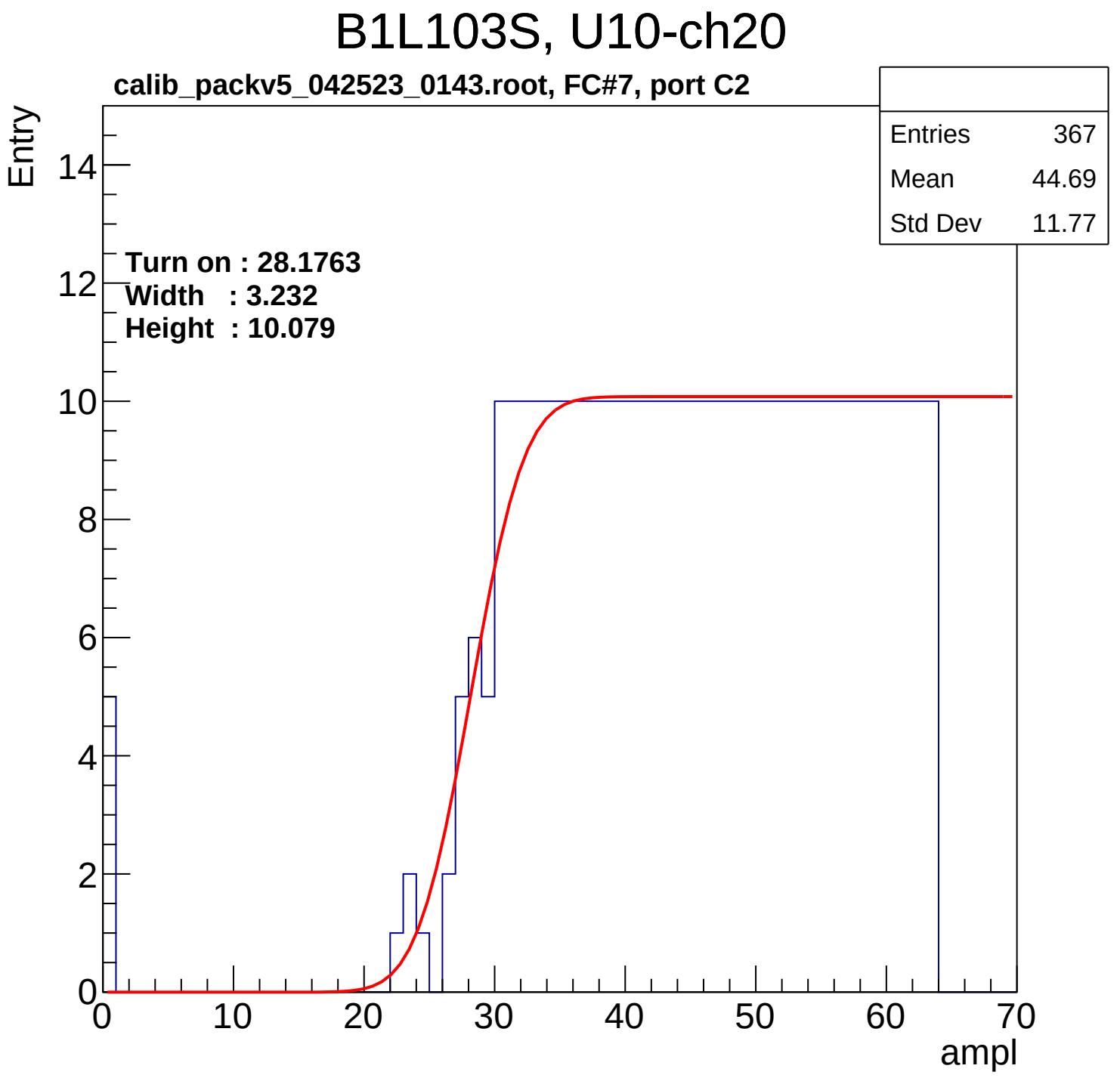
B1L103S, U10-ch20
calib_packv5_042523_0143.root, FC#7, port C2
Entries 367
Mean 44.69
Std Dev 11.77
Turn on : 28.1763
Width : 3.232
Height : 10.079
Entry
ampl
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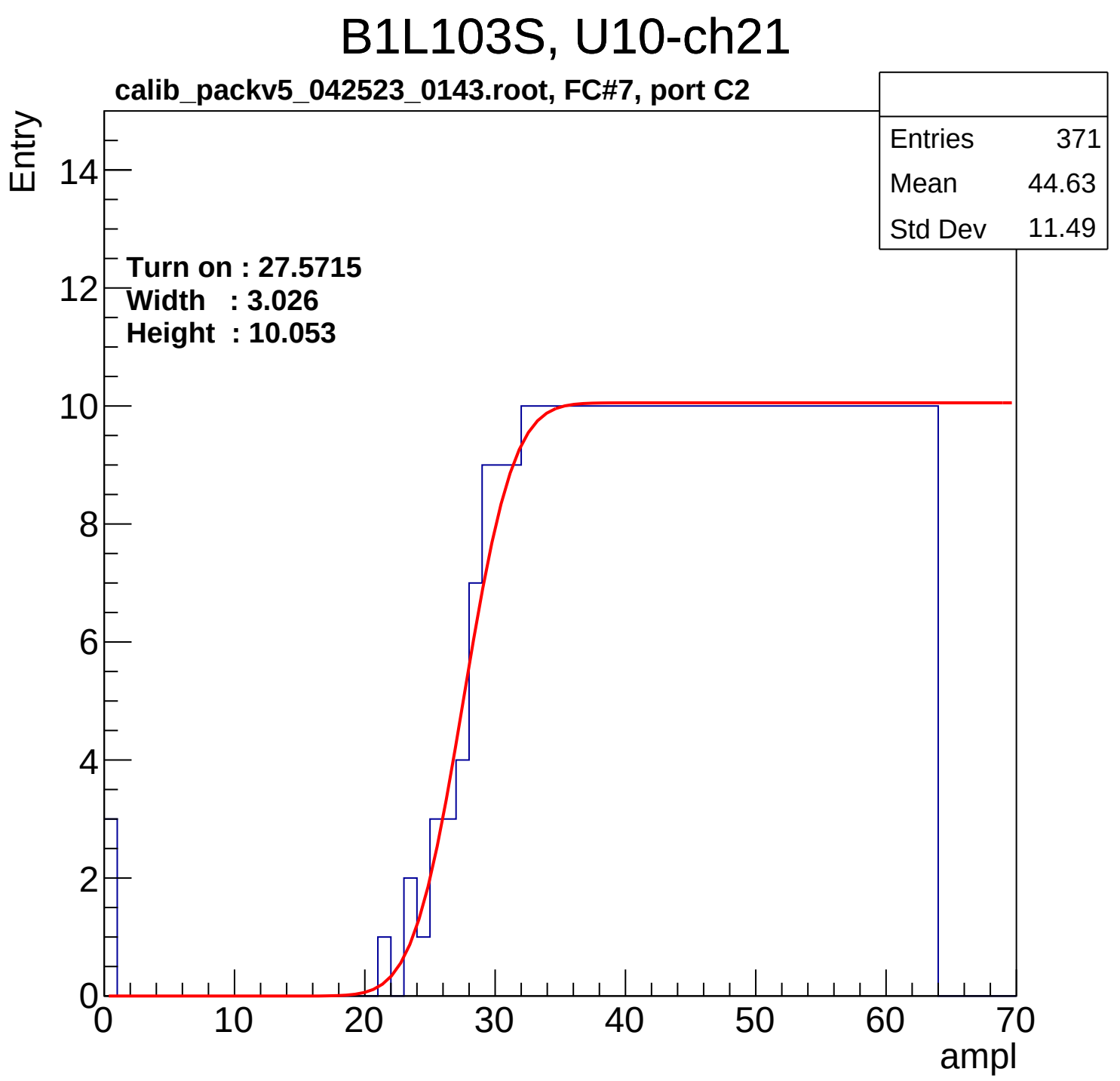
B1L103S, U10-ch21
calib_packv5_042523_0143.root, FC#7, port C2
Entries 371
Mean 44.63
Std Dev 11.49
Turn on : 27.5715
Width : 3.026
Height : 10.053
Entry
ampl
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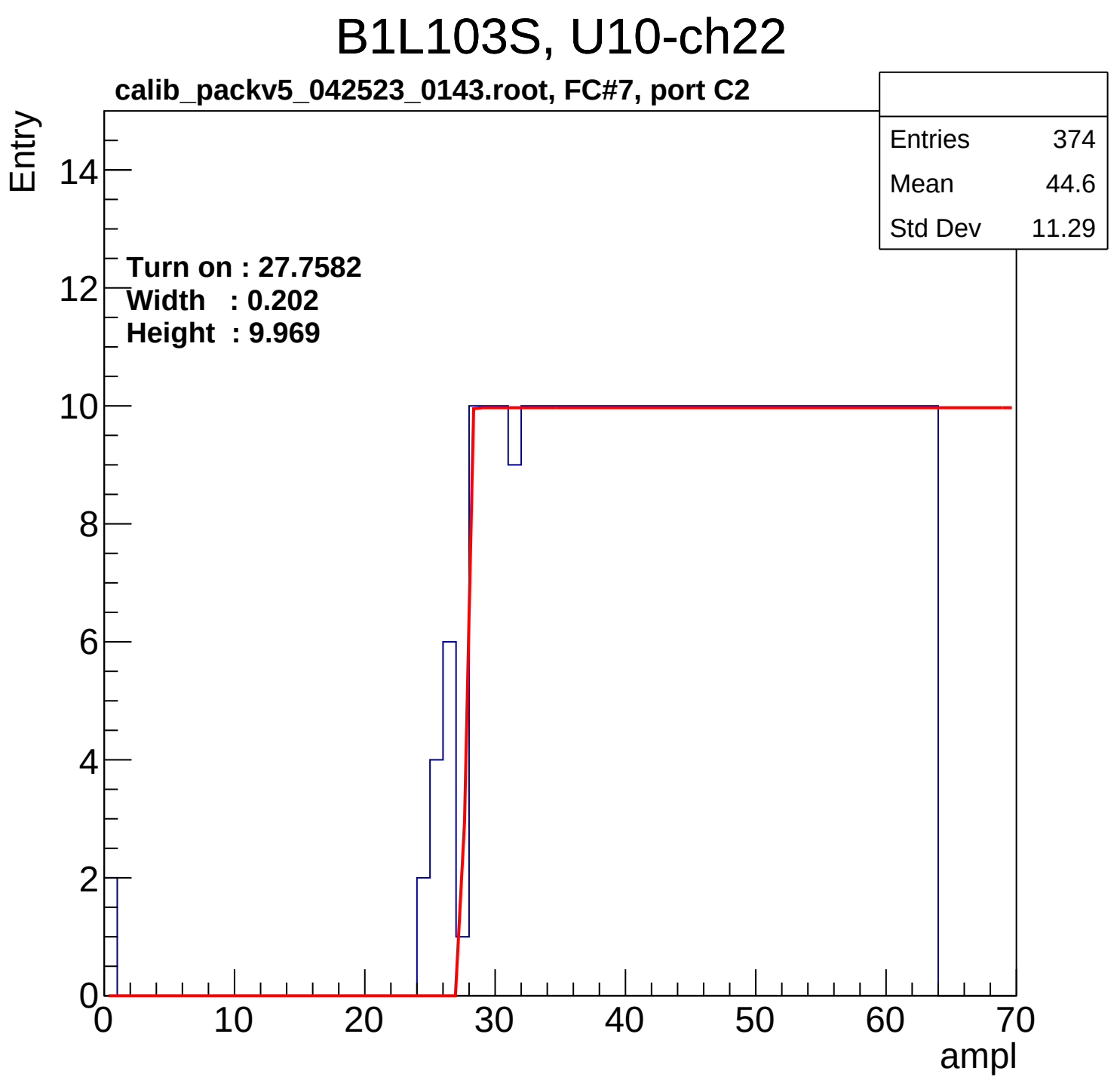
B1L103S, U10-ch22
calib_packv5_042523_0143.root, FC#7, port C2
Entries 374
Mean 44.6
Std Dev 11.29
Turn on : 27.7582
Width : 0.202
Height : 9.969
Entry
ampl
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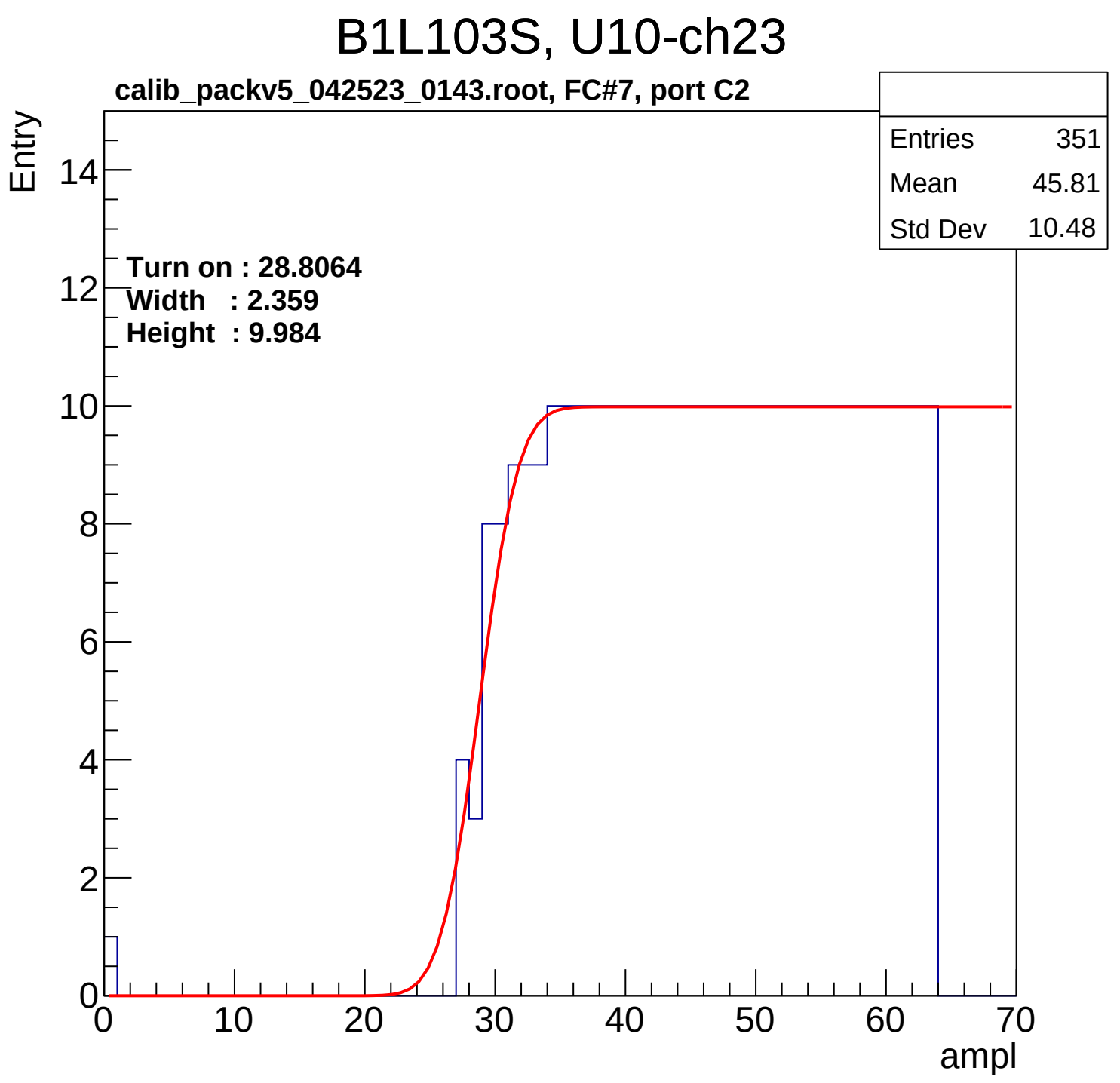
B1L103S, U10-ch23
calib_packv5_042523_0143.root, FC#7, port C2
Entries 351
Mean 45.81
Std Dev 10.48
Turn on : 28.8064
Width : 2.359
Height : 9.984
Entry
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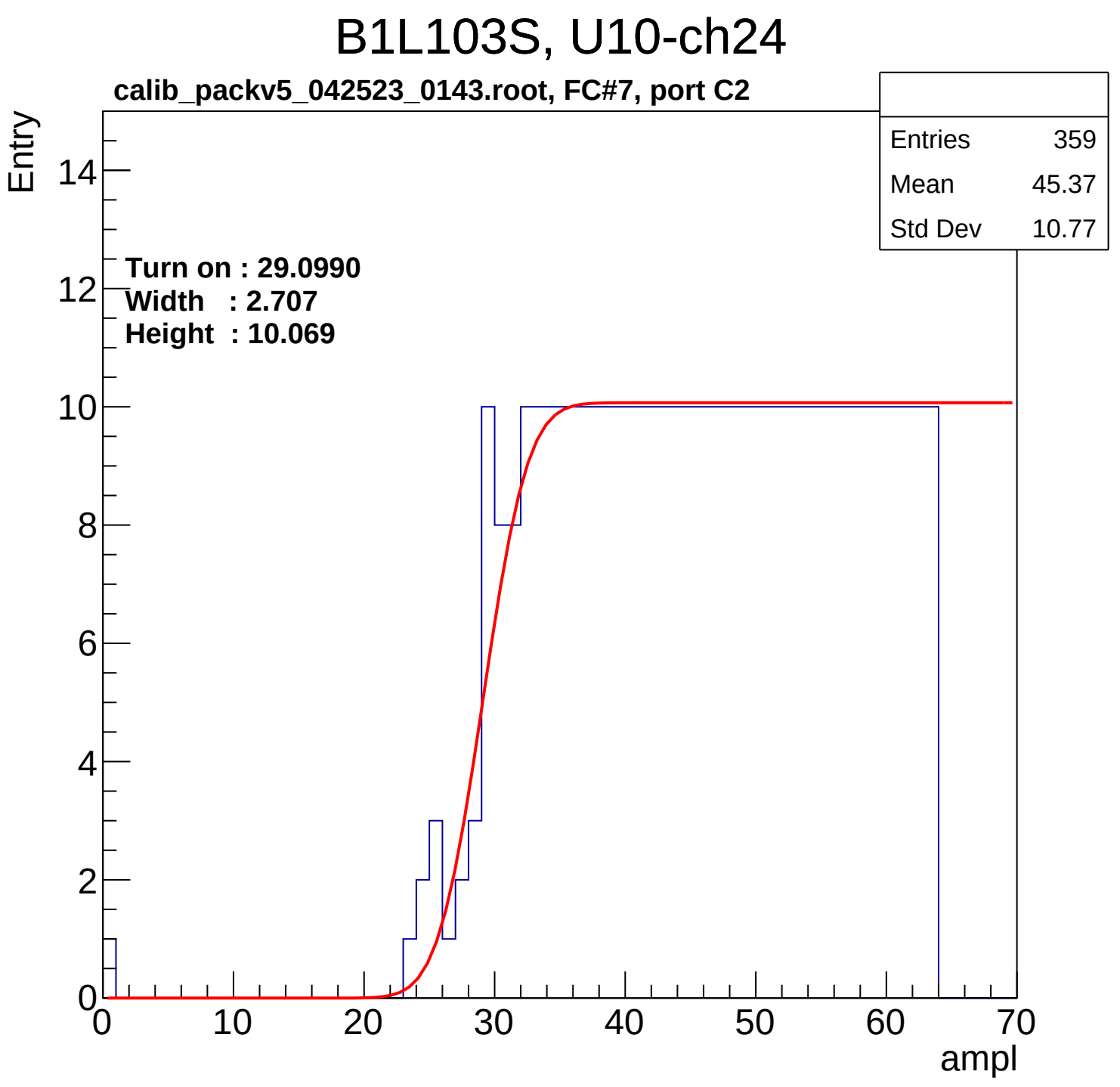
B1L103S, U10-ch24
calib_packv5_042523_0143.root, FC#7, port C2
Entries 359
Mean 45.37
Std Dev 10.77
Turn on : 29.0990
Width : 2.707
Height : 10.069
Entry
ampl
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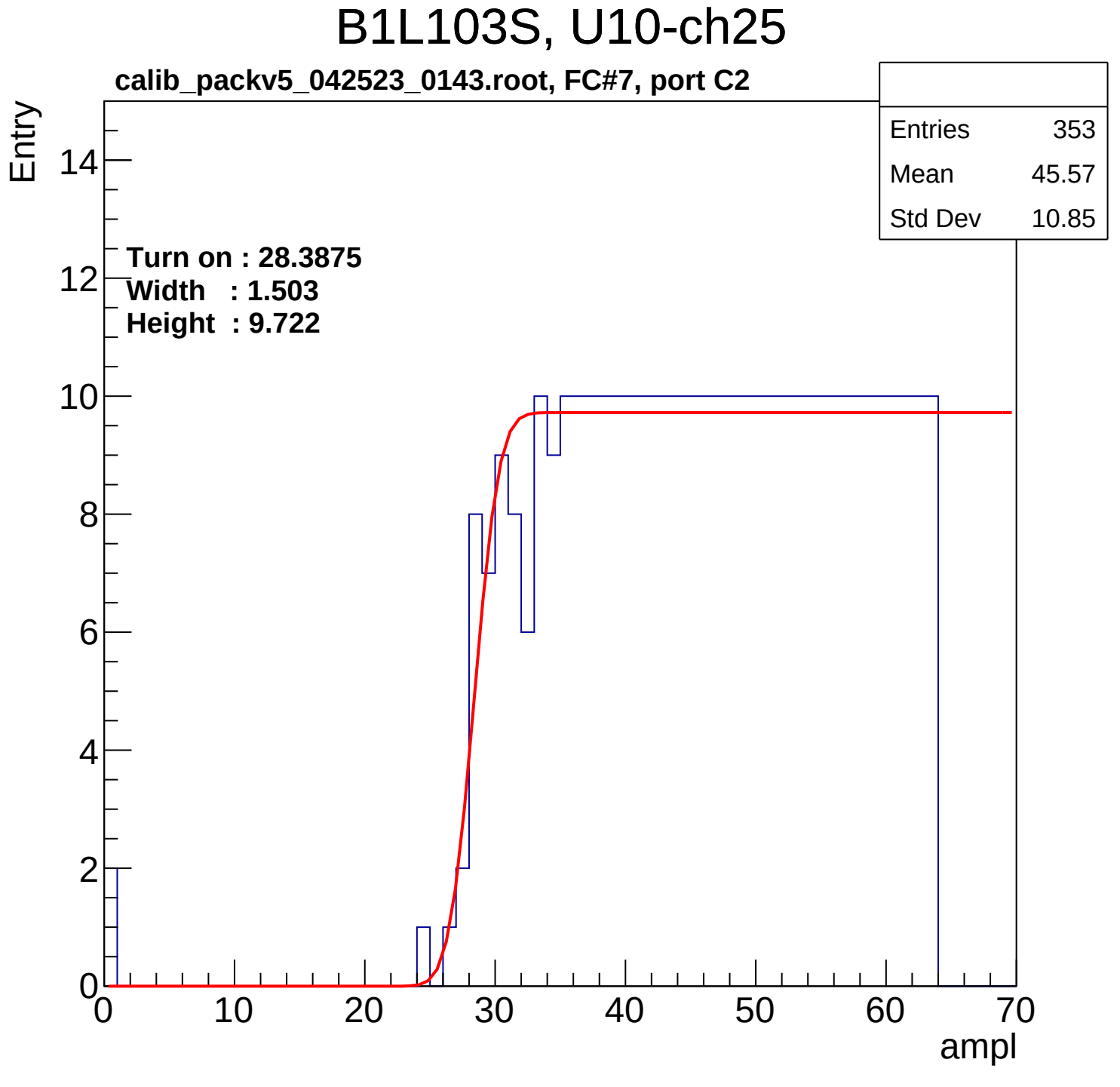
B1L103S, U10-ch25
calib_packv5_042523_0143.root, FC#7, port C2
Entries 353
Mean 45.57
Std Dev 10.85
Turn on : 28.3875
Width : 1.503
Height : 9.722
Entry
ampl
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6
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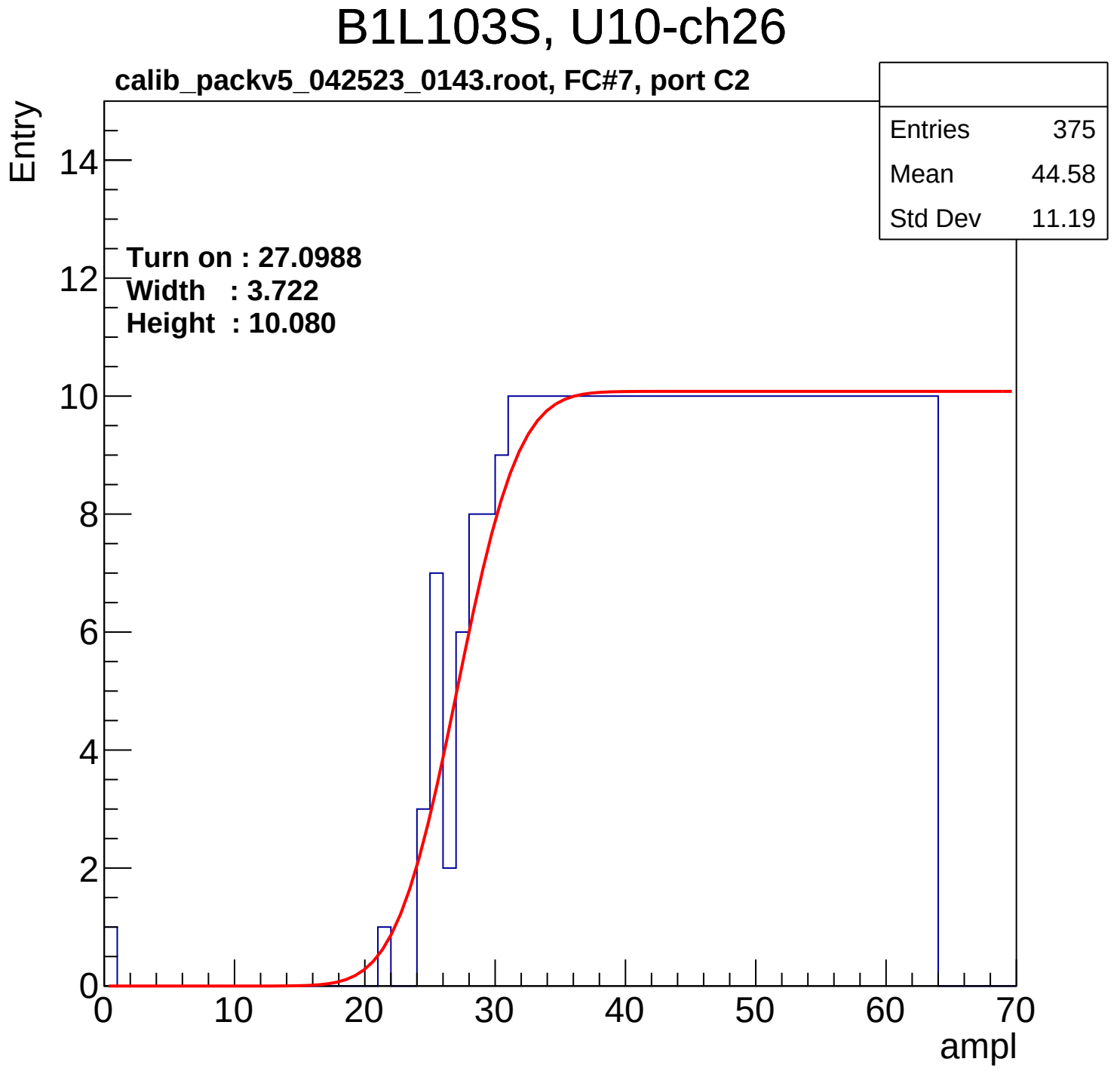
B1L103S, U10-ch26
calib_packv5_042523_0143.root, FC#7, port C2
Entries 375
Mean 44.58
Std Dev 11.19
Turn on : 27.0988
Width : 3.722
Height : 10.080
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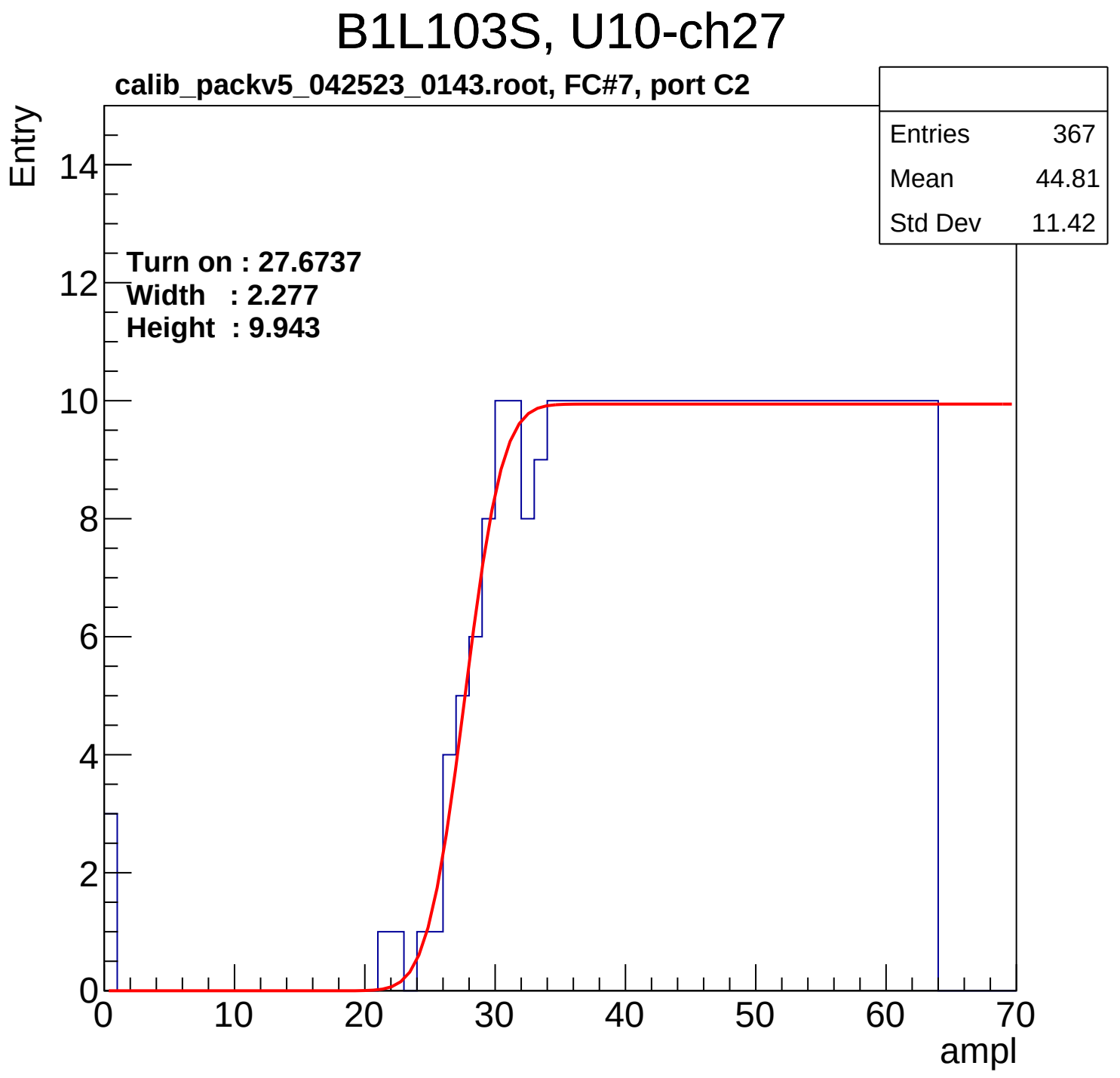
B1L103S, U10-ch27
calib_packv5_042523_0143.root, FC#7, port C2
Entries 367
Mean 44.81
Std Dev 11.42
Turn on : 27.6737
Width : 2.277
Height : 9.943
Entry
ampl
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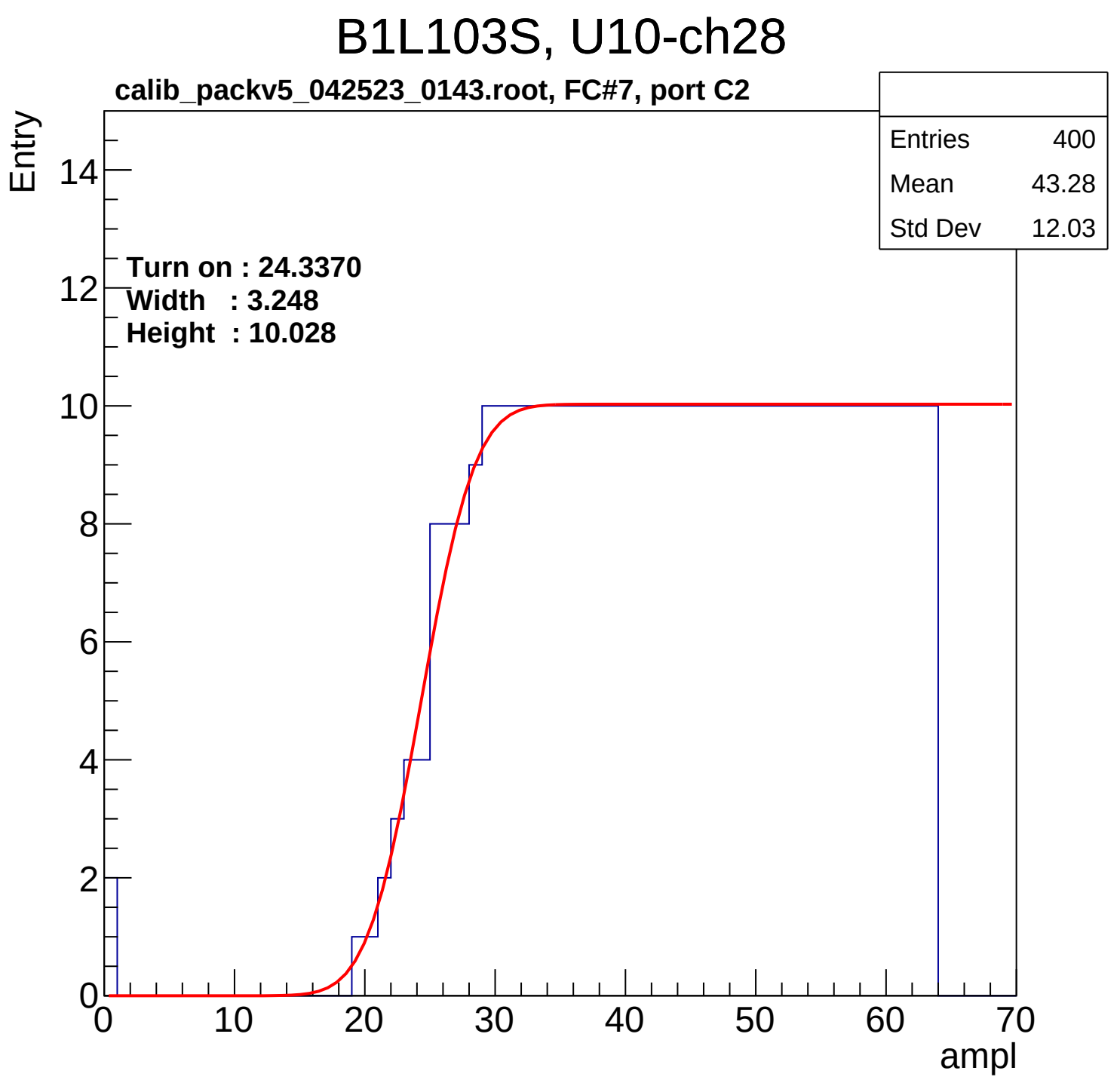
B1L103S, U10-ch28
calib_packv5_042523_0143.root, FC#7, port C2
Entries 400
Mean 43.28
Std Dev 12.03
Turn on : 24.3370
Width : 3.248
Height : 10.028
Entry
ampl
0
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4
6
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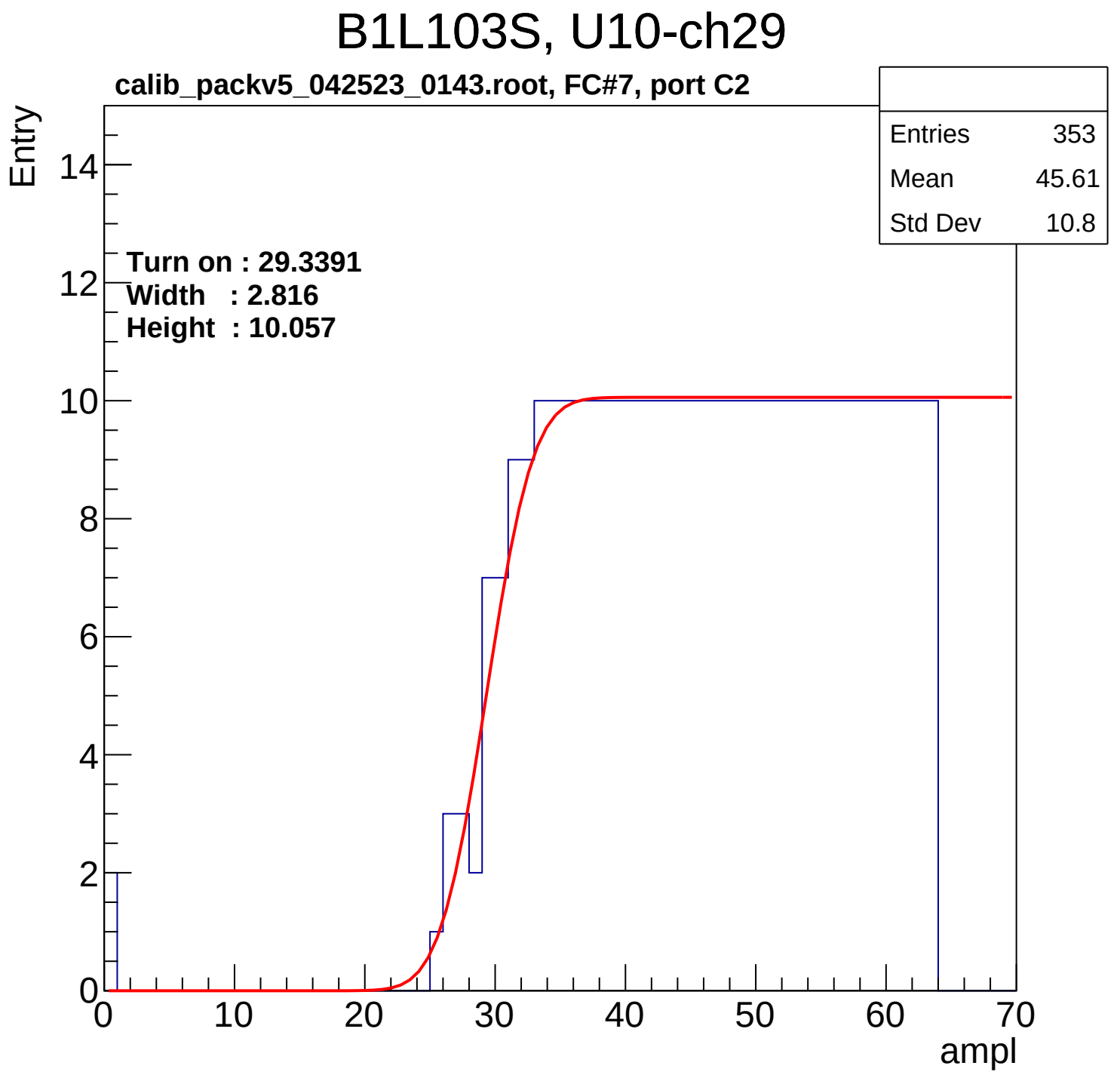
B1L103S, U10-ch29
calib_packv5_042523_0143.root, FC#7, port C2
Entries 353
Mean 45.61
Std Dev 10.8
Turn on : 29.3391
Width : 2.816
Height : 10.057
Entry
ampl
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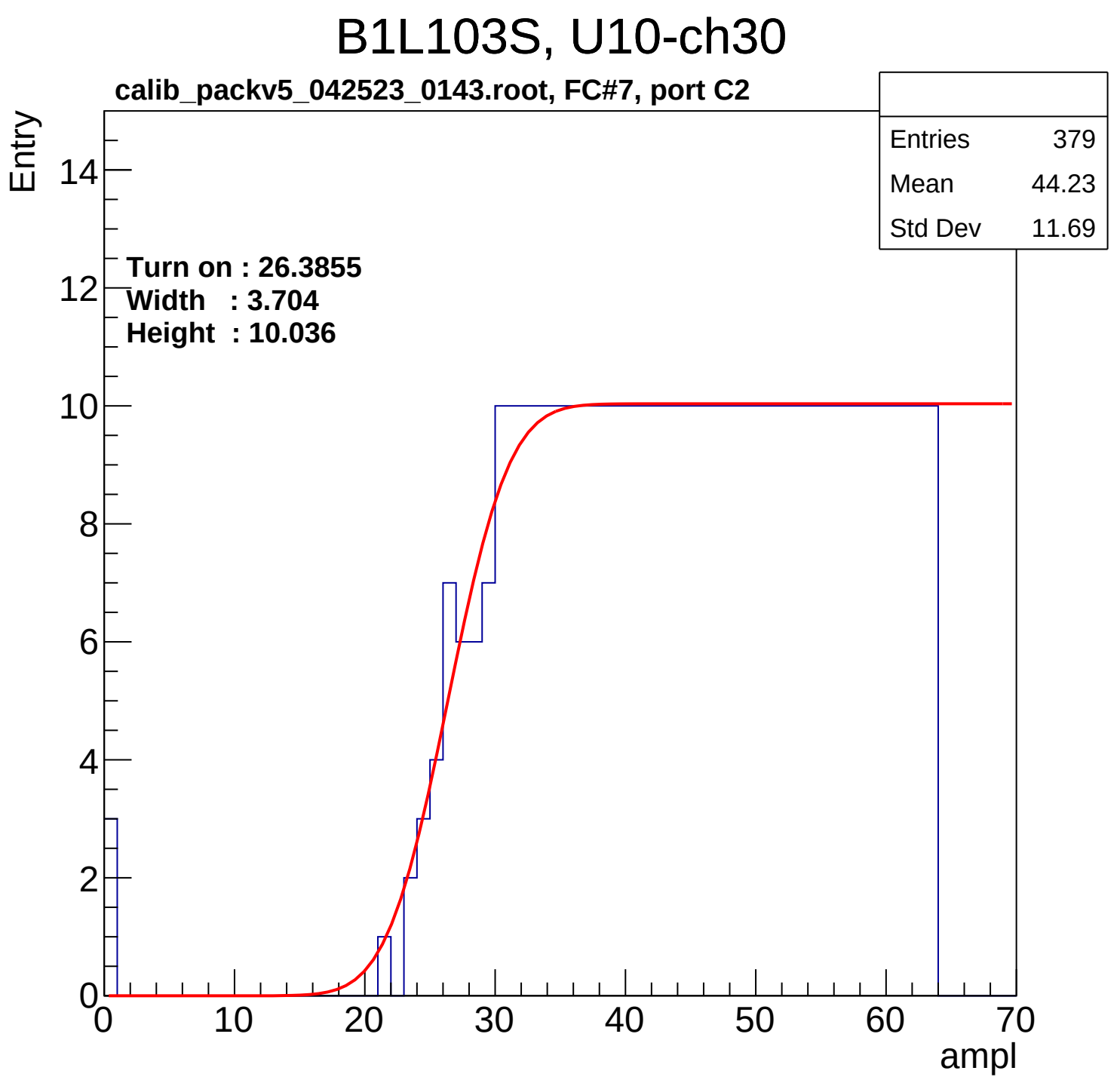
B1L103S, U10-ch30
calib_packv5_042523_0143.root, FC#7, port C2
Entries 379
Mean 44.23
Std Dev 11.69
Turn on : 26.3855
Width : 3.704
Height : 10.036
Entry
ampl
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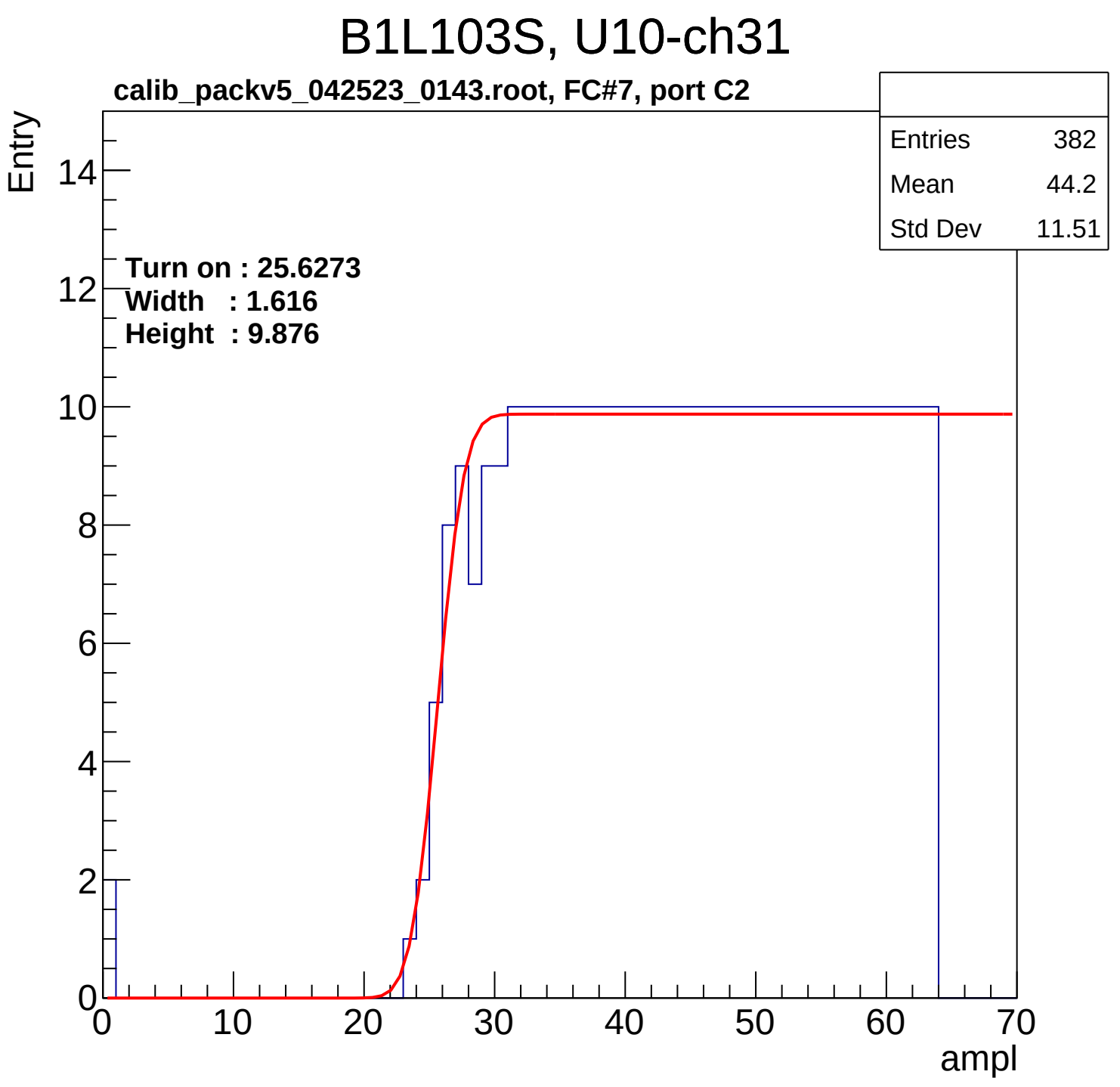
B1L103S, U10-ch31
calib_packv5_042523_0143.root, FC#7, port C2
Entries 382
Mean 44.2
Std Dev 11.51
Turn on : 25.6273
Width : 1.616
Height : 9.876
Entry
ampl
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2
4
6
8
10
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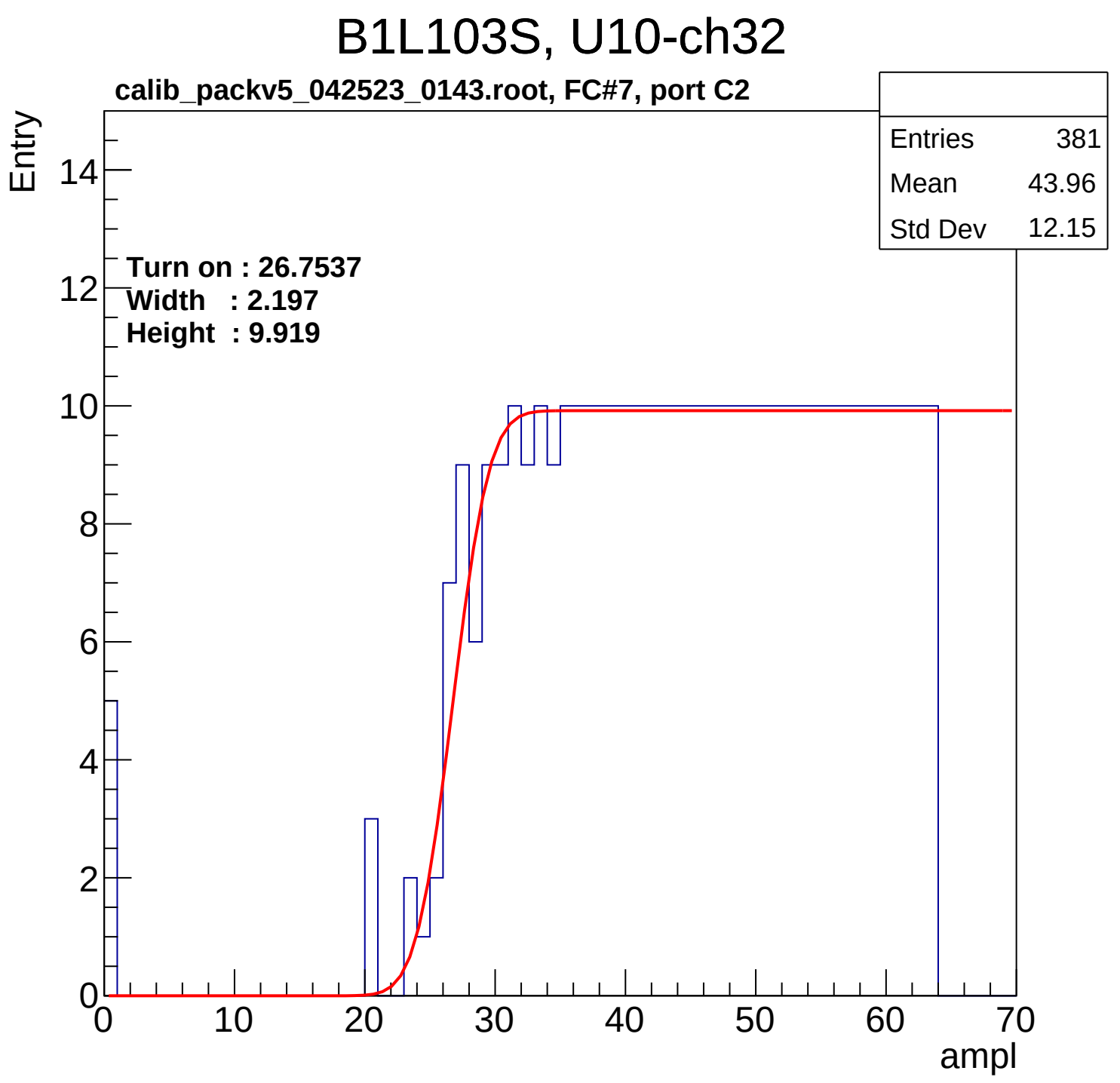
B1L103S, U10-ch32
calib_packv5_042523_0143.root, FC#7, port C2
Entries 381
Mean 43.96
Std Dev 12.15
Turn on : 26.7537
Width : 2.197
Height : 9.919
Entry
ampl
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2
4
6
8
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0
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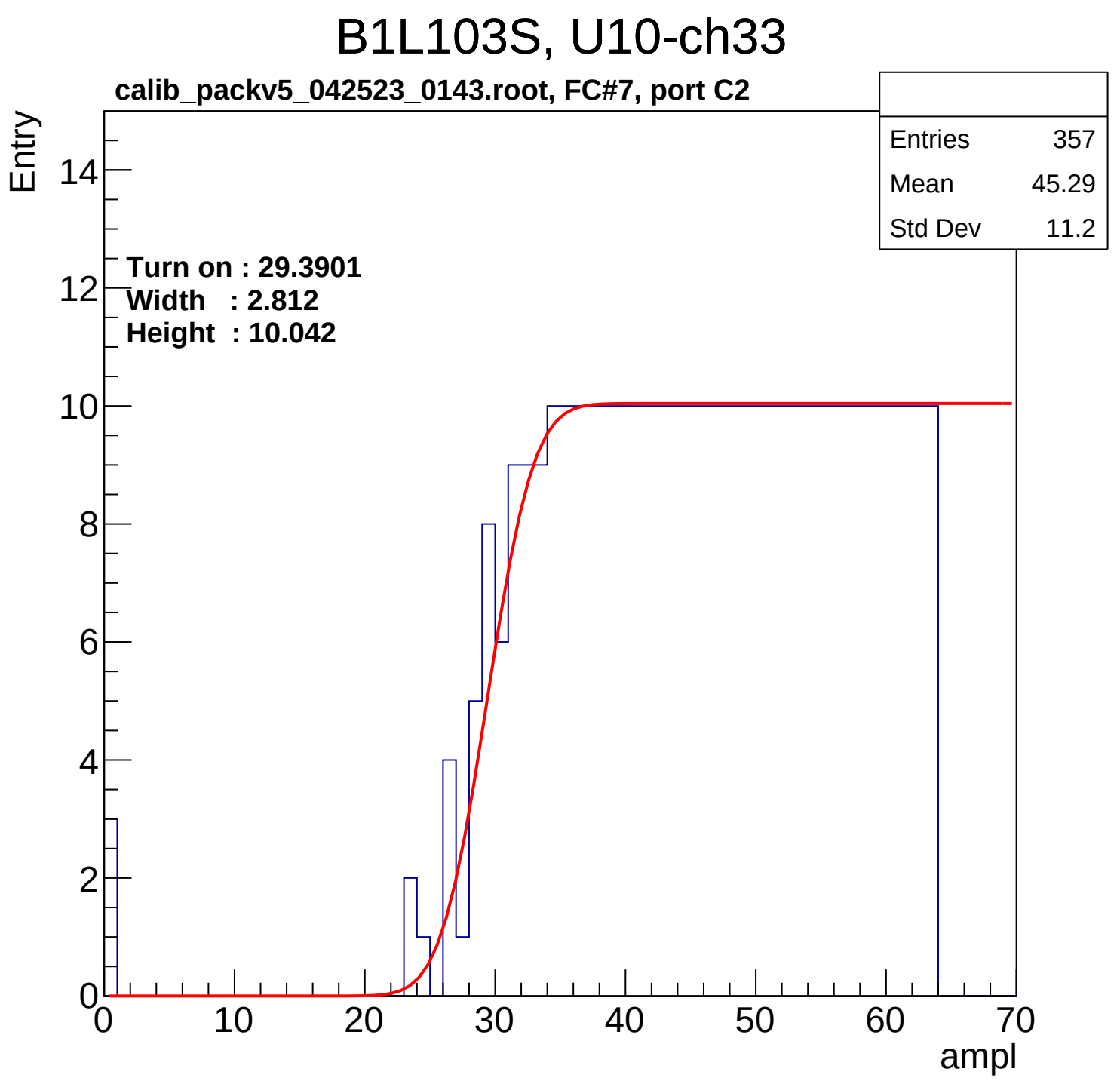
B1L103S, U10-ch33
calib_packv5_042523_0143.root, FC#7, port C2
Entries 357
Mean 45.29
Std Dev 11.2
Turn on : 29.3901
Width : 2.812
Height : 10.042
Entry
ampl
0
2
4
6
8
10
12
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0
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60
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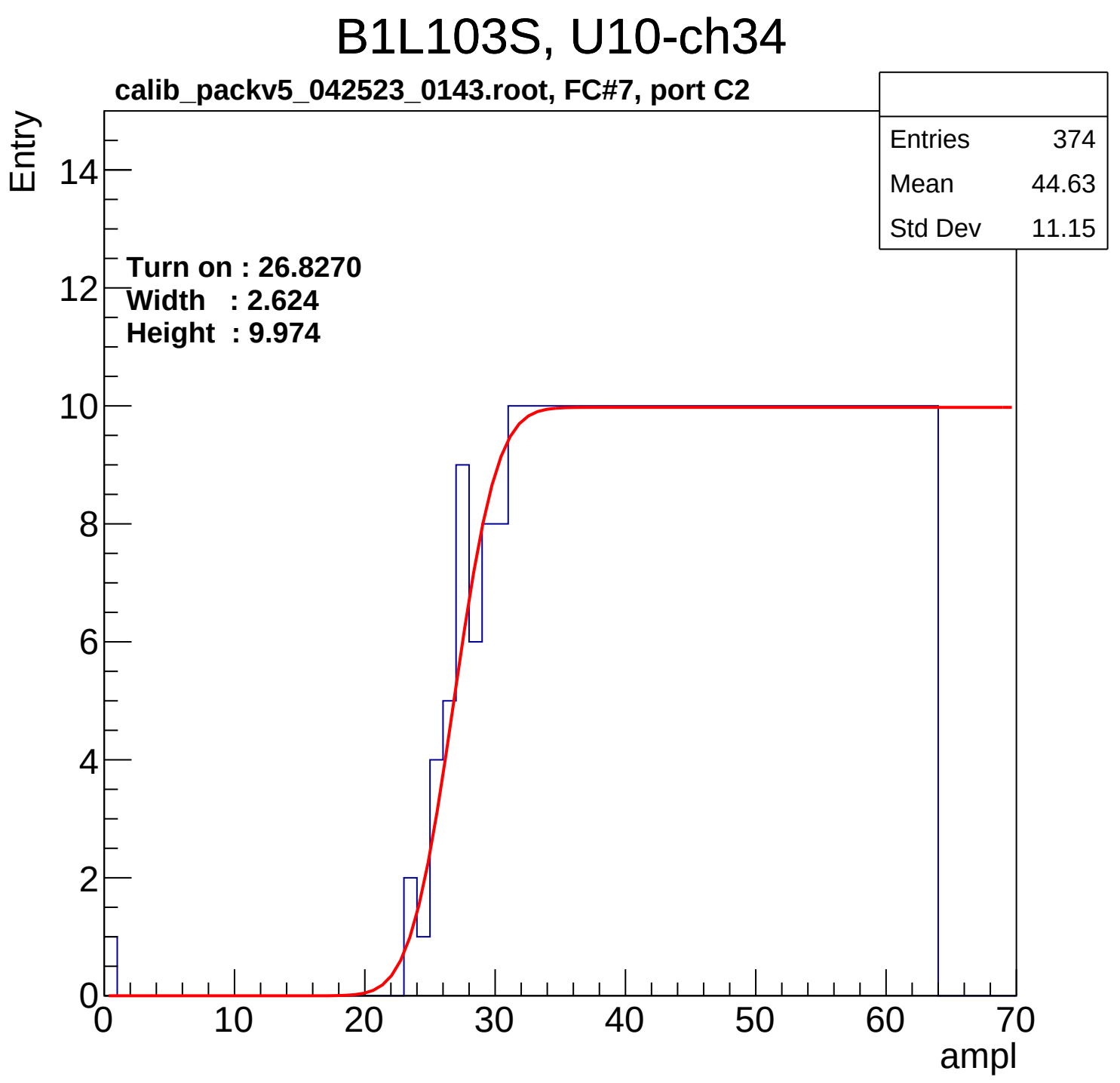
B1L103S, U10-ch34
calib_packv5_042523_0143.root, FC#7, port C2
Entries 374
Mean 44.63
Std Dev 11.15
Turn on : 26.8270
Width : 2.624
Height : 9.974
Entry
ampl
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2
4
6
8
10
12
14
0
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60
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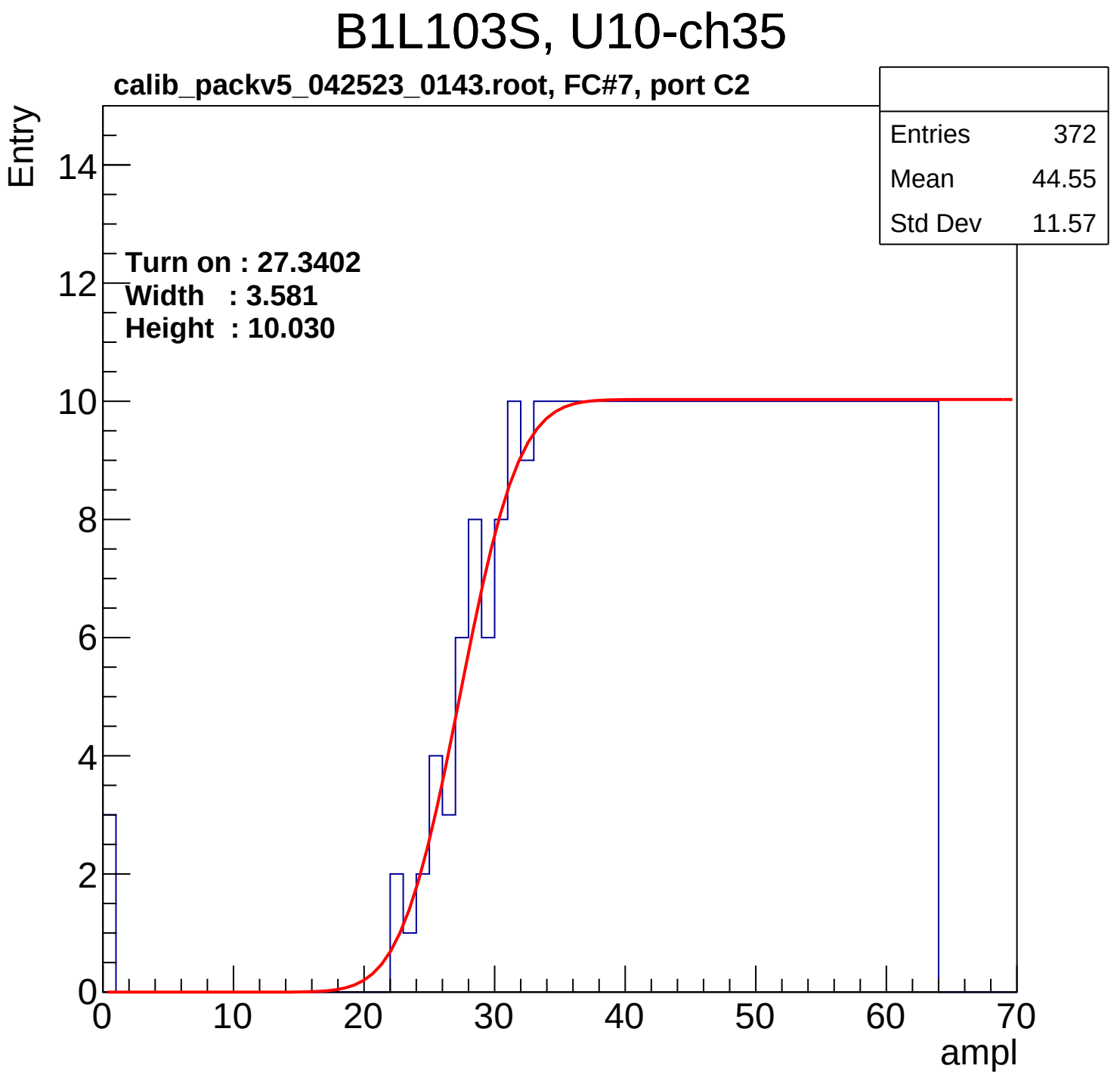
B1L103S, U10-ch35
calib_packv5_042523_0143.root, FC#7, port C2
Entries 372
Mean 44.55
Std Dev 11.57
Turn on : 27.3402
Width : 3.581
Height : 10.030
Entry
ampl
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2
4
6
8
10
12
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0
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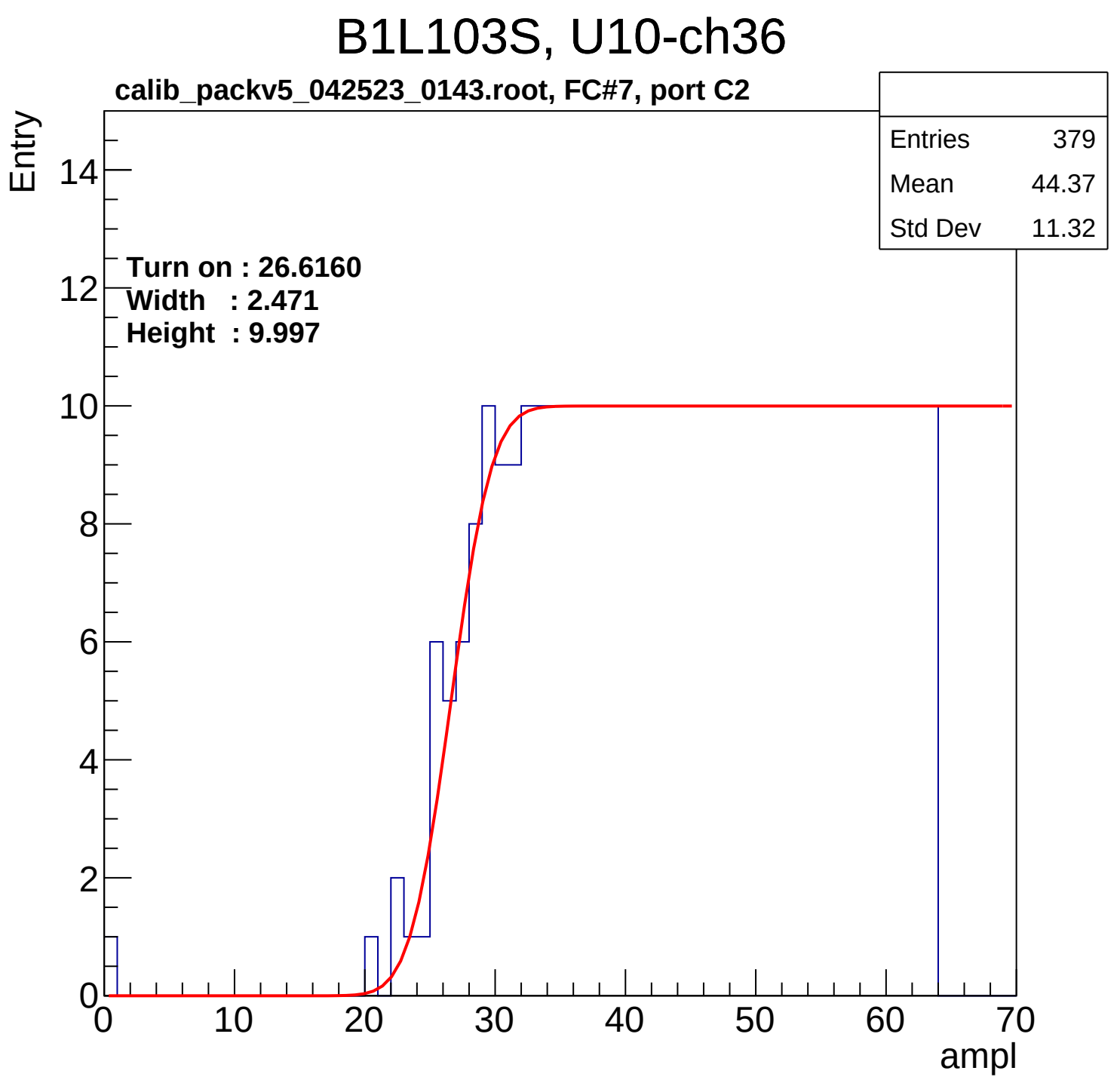
B1L103S, U10-ch36
calib_packv5_042523_0143.root, FC#7, port C2
Entries 379
Mean 44.37
Std Dev 11.32
Turn on : 26.6160
Width : 2.471
Height : 9.997
Entry
ampl
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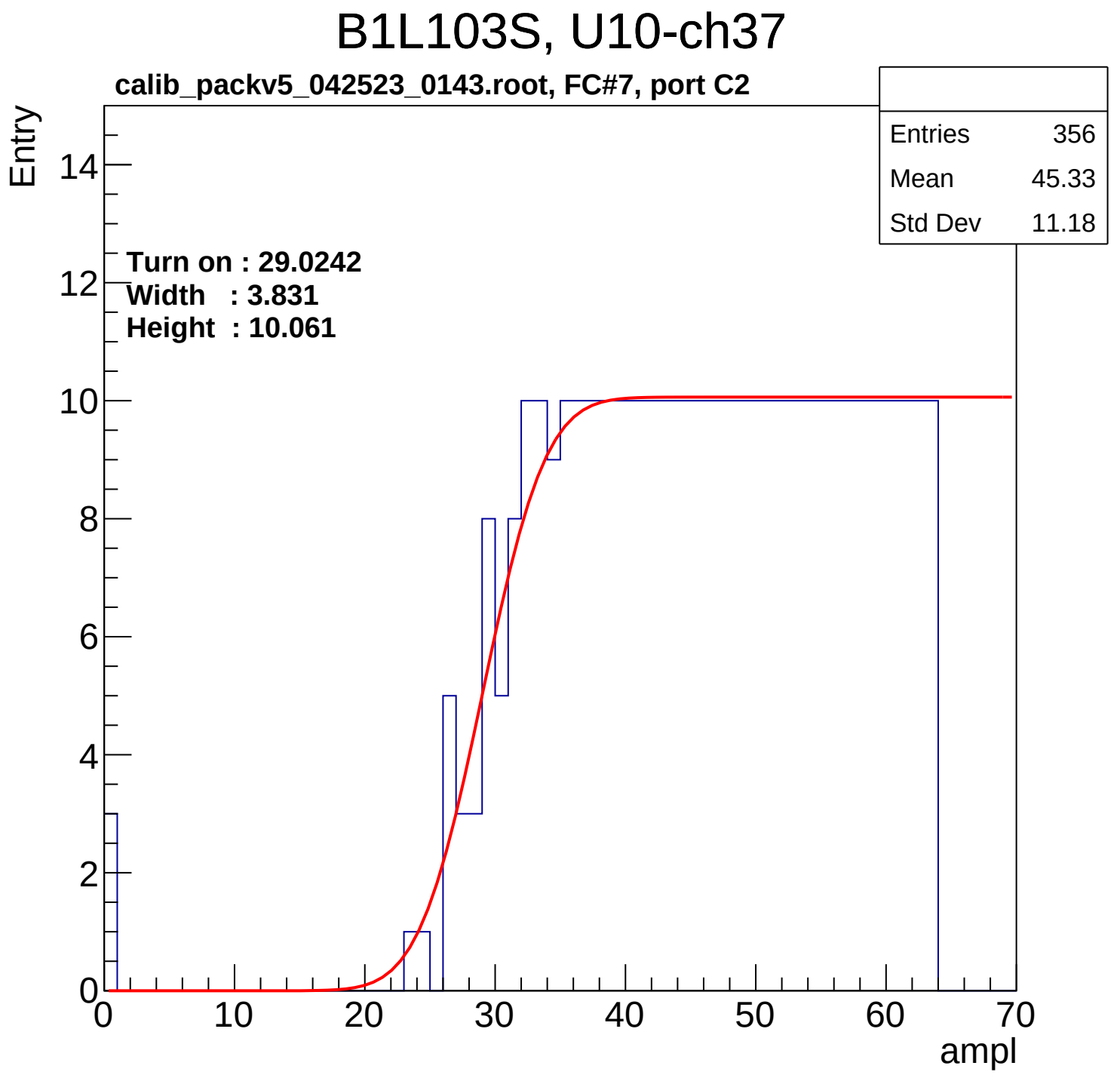
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L103S, U10-ch37
calib_packv5_042523_0143.root, FC#7, port C2
Entries 356
Mean 45.33
Std Dev 11.18
Turn on : 29.0242
Width : 3.831
Height : 10.061
Entry
ampl
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4
6
8
10
12
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60
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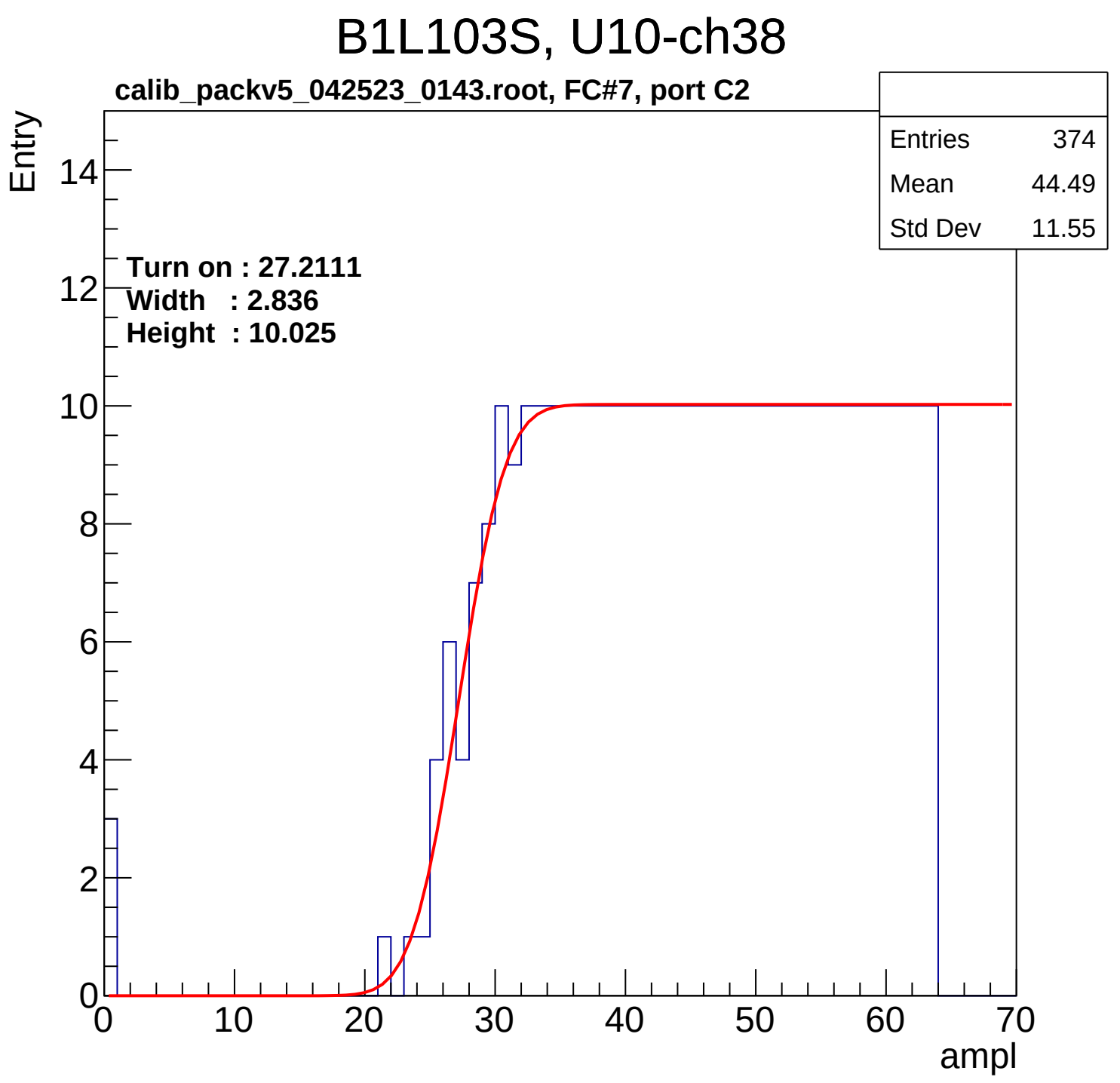
B1L103S, U10-ch38
calib_packv5_042523_0143.root, FC#7, port C2
Entries 374
Mean 44.49
Std Dev 11.55
Turn on : 27.2111
Width : 2.836
Height : 10.025
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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40
50
60
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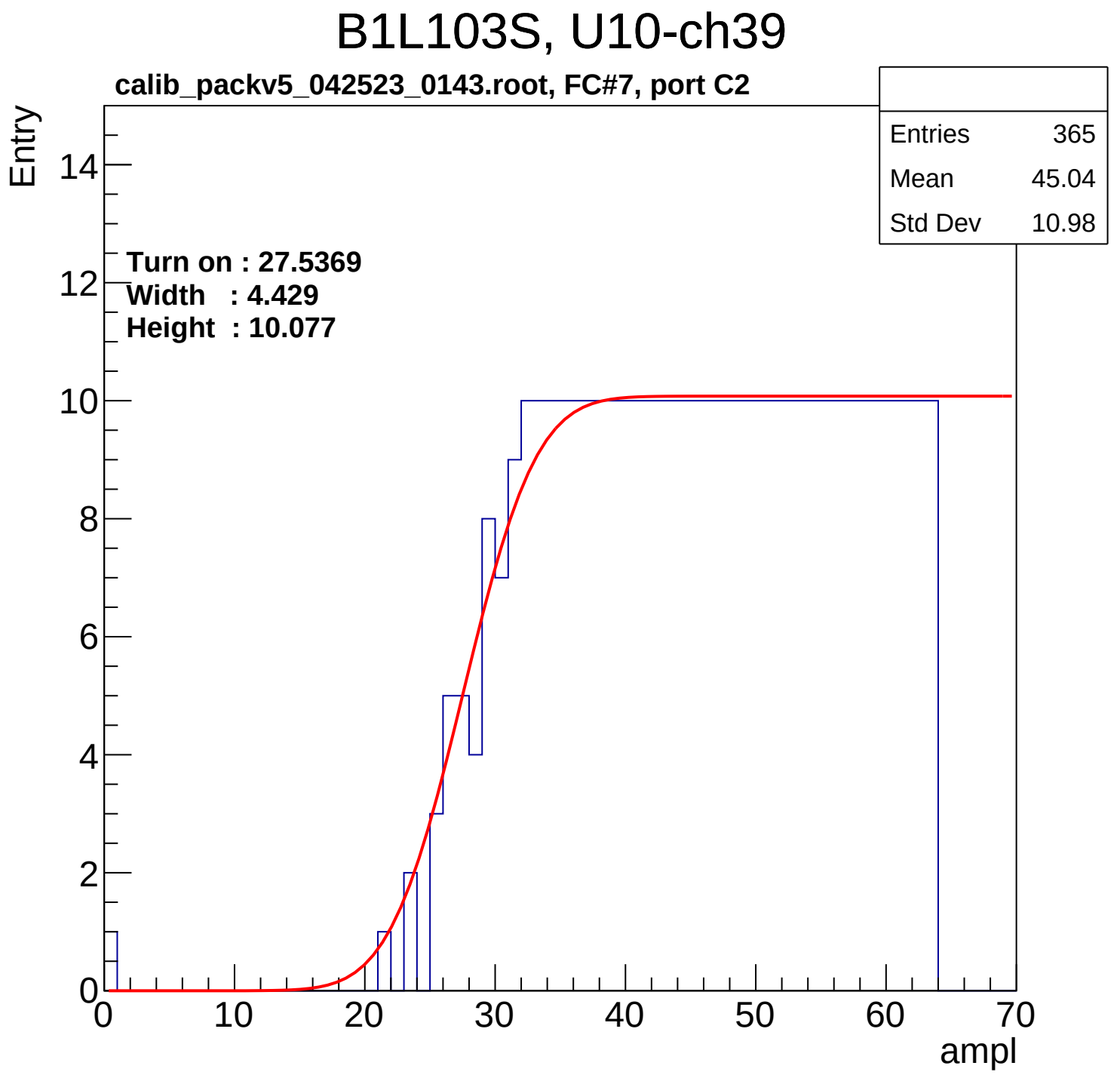
B1L103S, U10-ch39
calib_packv5_042523_0143.root, FC#7, port C2
Entries 365
Mean 45.04
Std Dev 10.98
Turn on : 27.5369
Width : 4.429
Height : 10.077
Entry
ampl
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2
4
6
8
10
12
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0
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60
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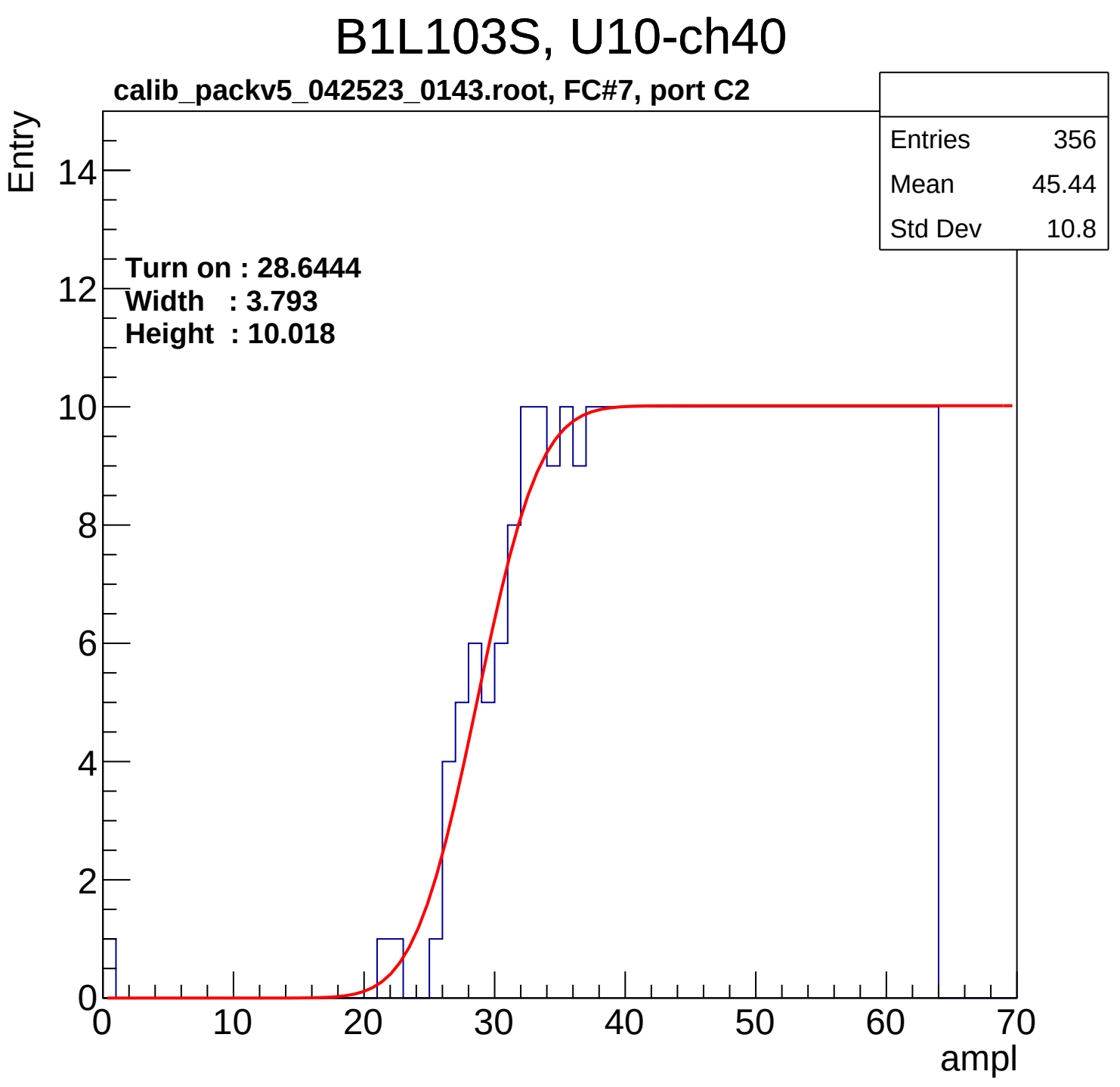
B1L103S, U10-ch40
calib_packv5_042523_0143.root, FC#7, port C2
Entries 356
Mean 45.44
Std Dev 10.8
Turn on : 28.6444
Width : 3.793
Height : 10.018
Entry
ampl
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6
8
10
12
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0
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60
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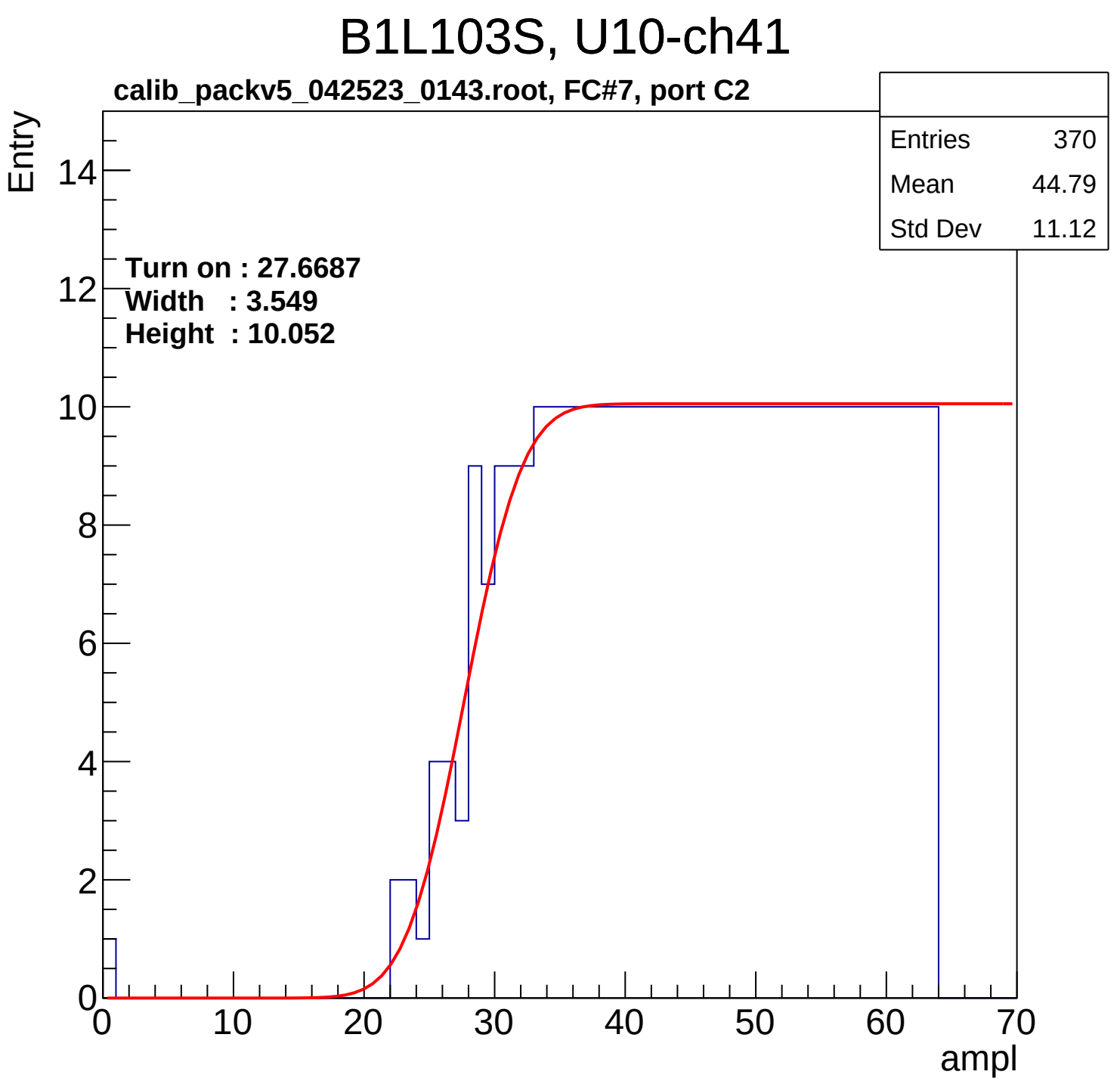
B1L103S, U10-ch41
calib_packv5_042523_0143.root, FC#7, port C2
Entries 370
Mean 44.79
Std Dev 11.12
Turn on : 27.6687
Width : 3.549
Height : 10.052
Entry
ampl
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6
8
10
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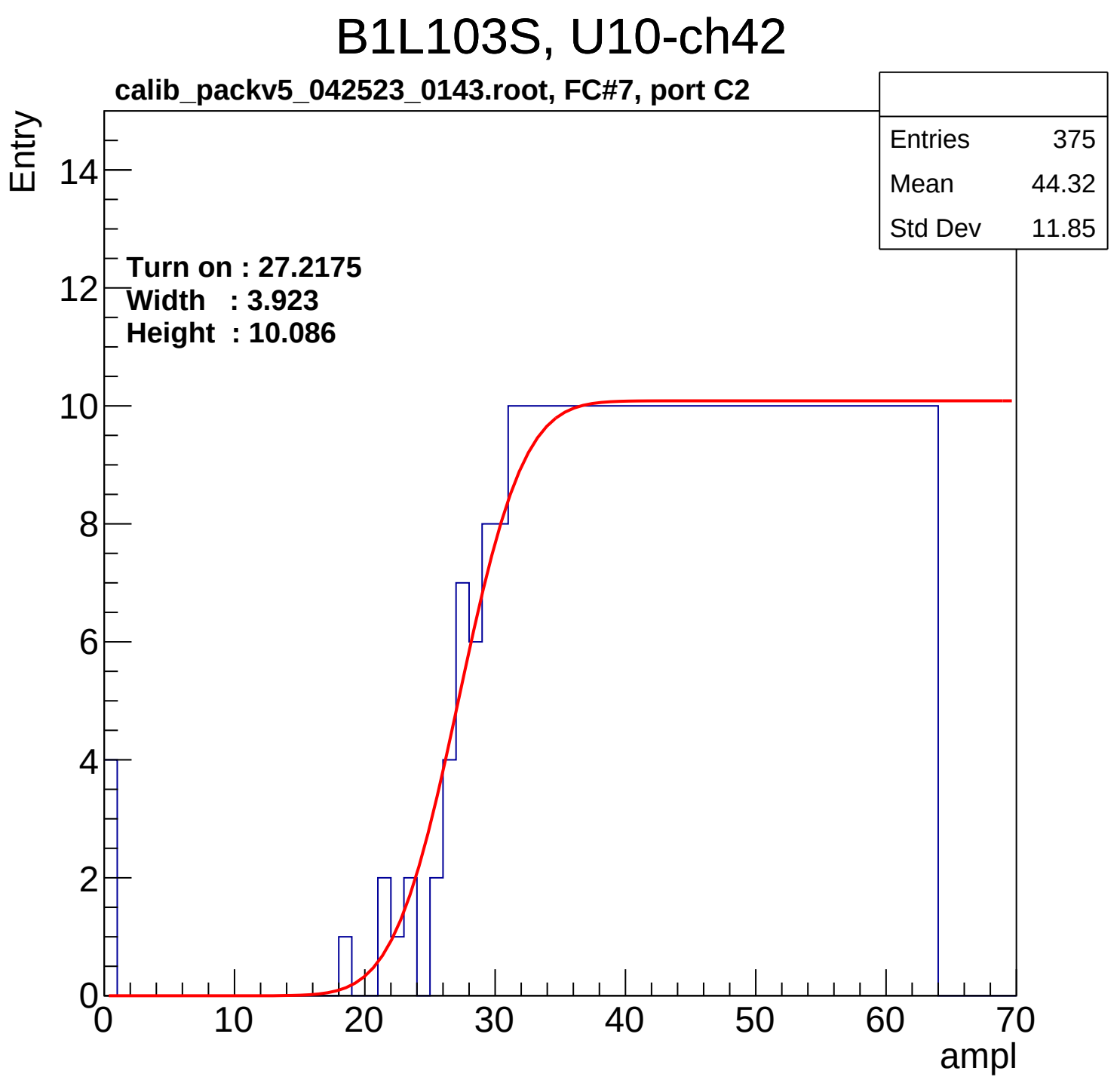
B1L103S, U10-ch42
calib_packv5_042523_0143.root, FC#7, port C2
Entries 375
Mean 44.32
Std Dev 11.85
Turn on : 27.2175
Width : 3.923
Height : 10.086
Entry
ampl
0
2
4
6
8
10
12
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0
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60
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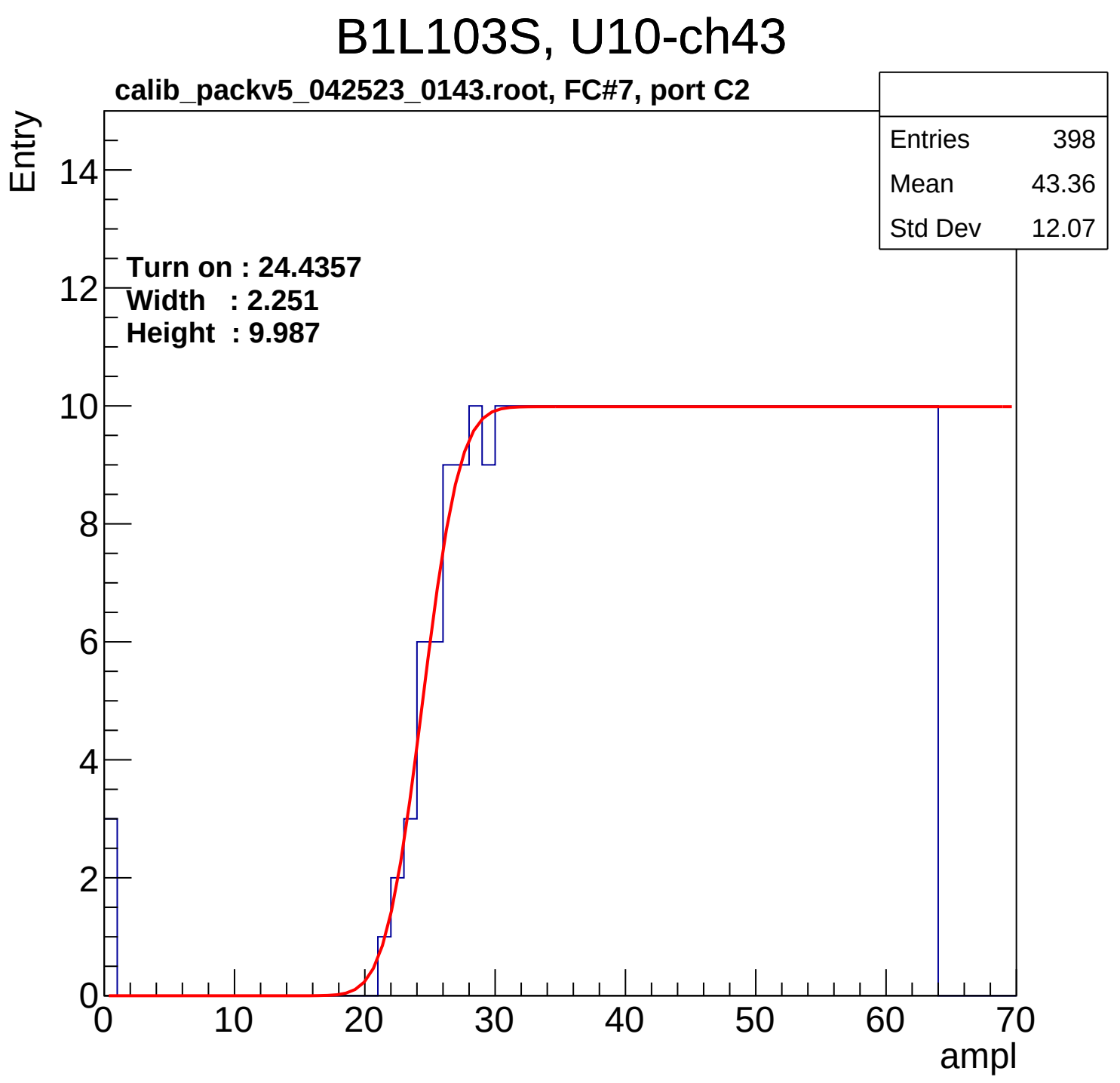
B1L103S, U10-ch43
calib_packv5_042523_0143.root, FC#7, port C2
Entries 398
Mean 43.36
Std Dev 12.07
Turn on : 24.4357
Width : 2.251
Height : 9.987
Entry
ampl
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6
8
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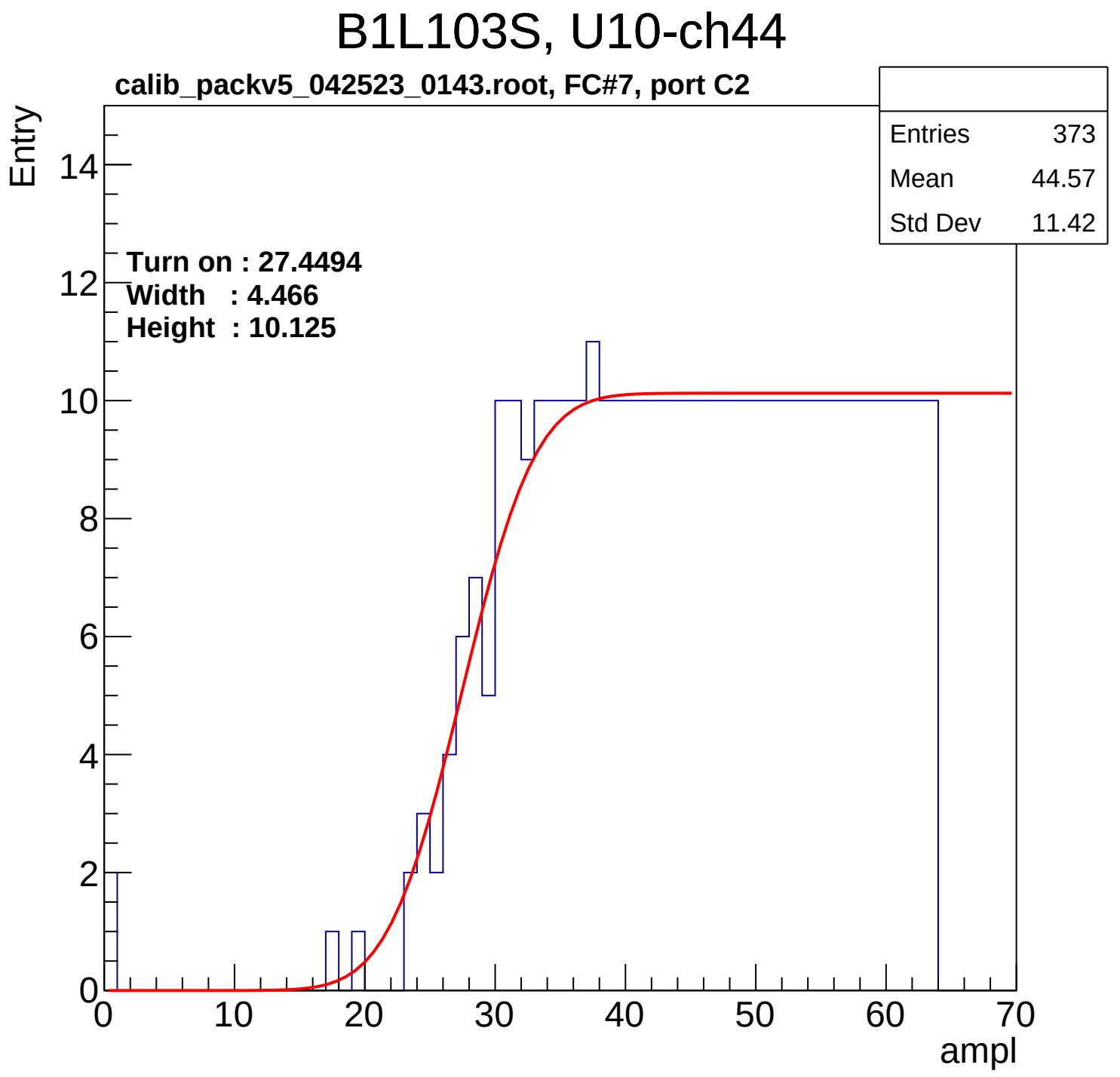
B1L103S, U10-ch44
calib_packv5_042523_0143.root, FC#7, port C2
Entries 373
Mean 44.57
Std Dev 11.42
Turn on : 27.4494
Width : 4.466
Height : 10.125
Entry
ampl
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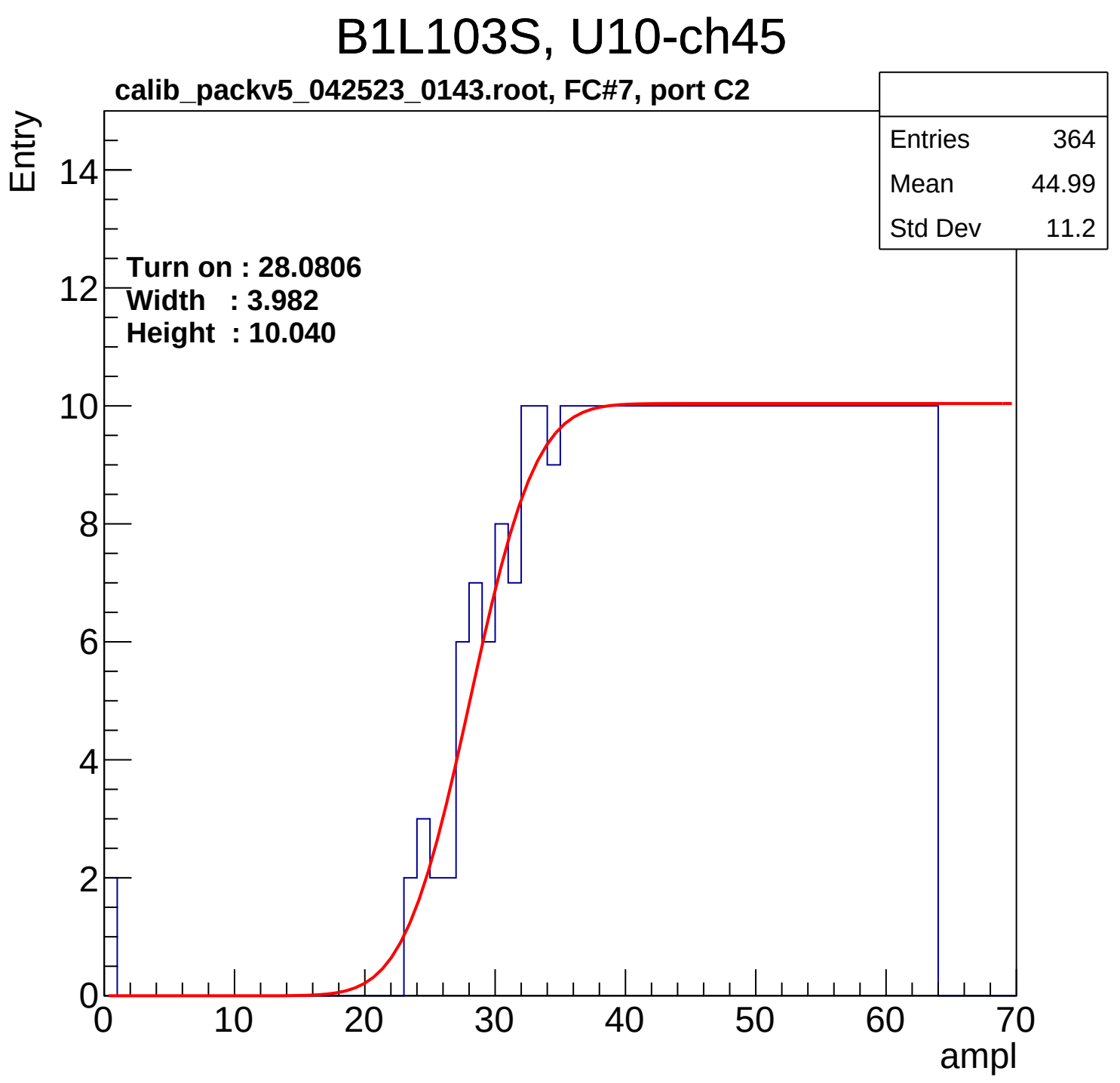
B1L103S, U10-ch45
calib_packv5_042523_0143.root, FC#7, port C2
Entries 364
Mean 44.99
Std Dev 11.2
Turn on : 28.0806
Width : 3.982
Height : 10.040
Entry
ampl
0
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4
6
8
10
12
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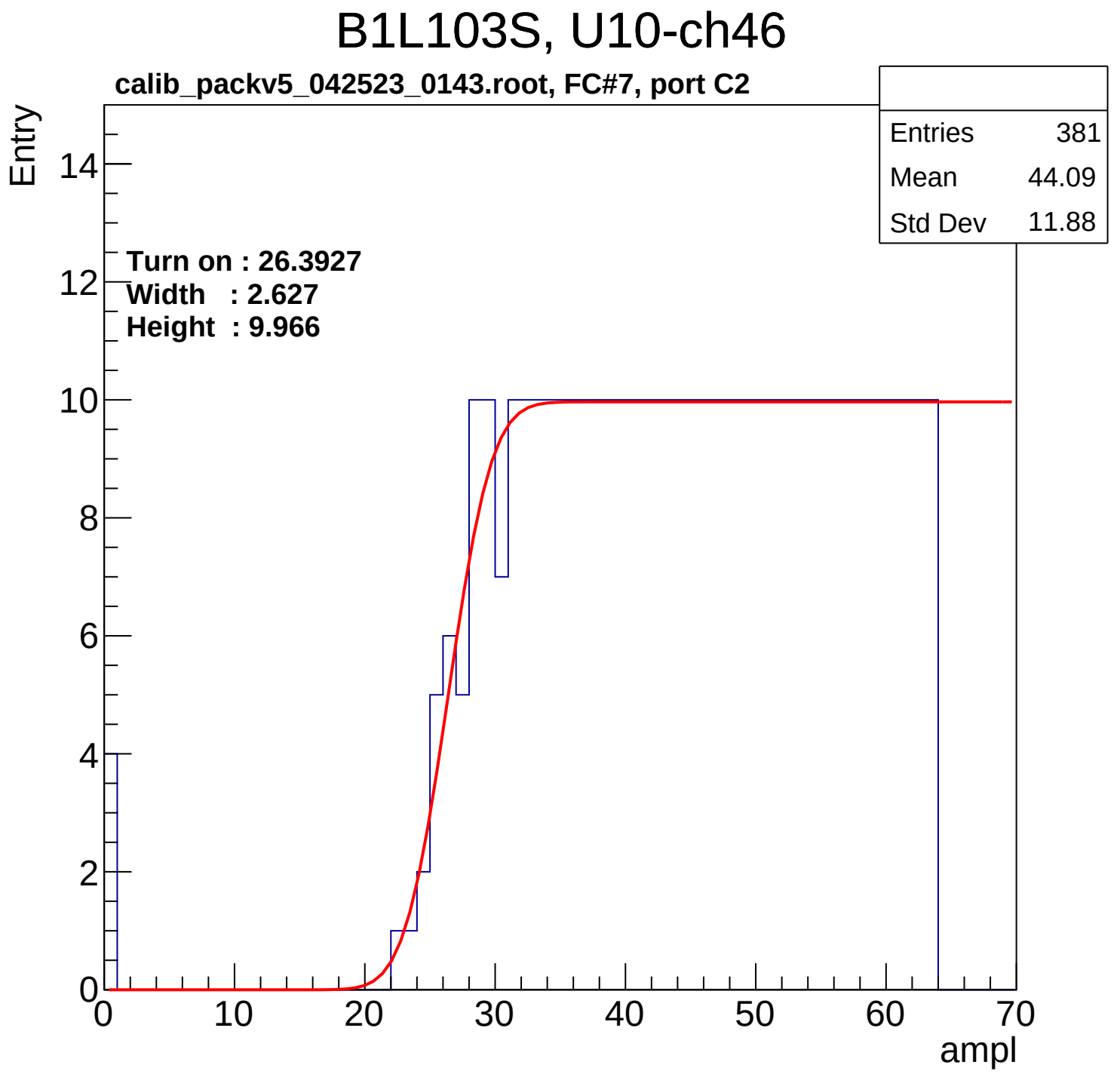
B1L103S, U10-ch46
calib_packv5_042523_0143.root, FC#7, port C2
Entries 381
Mean 44.09
Std Dev 11.88
Turn on : 26.3927
Width : 2.627
Height : 9.966
Entry
ampl
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6
8
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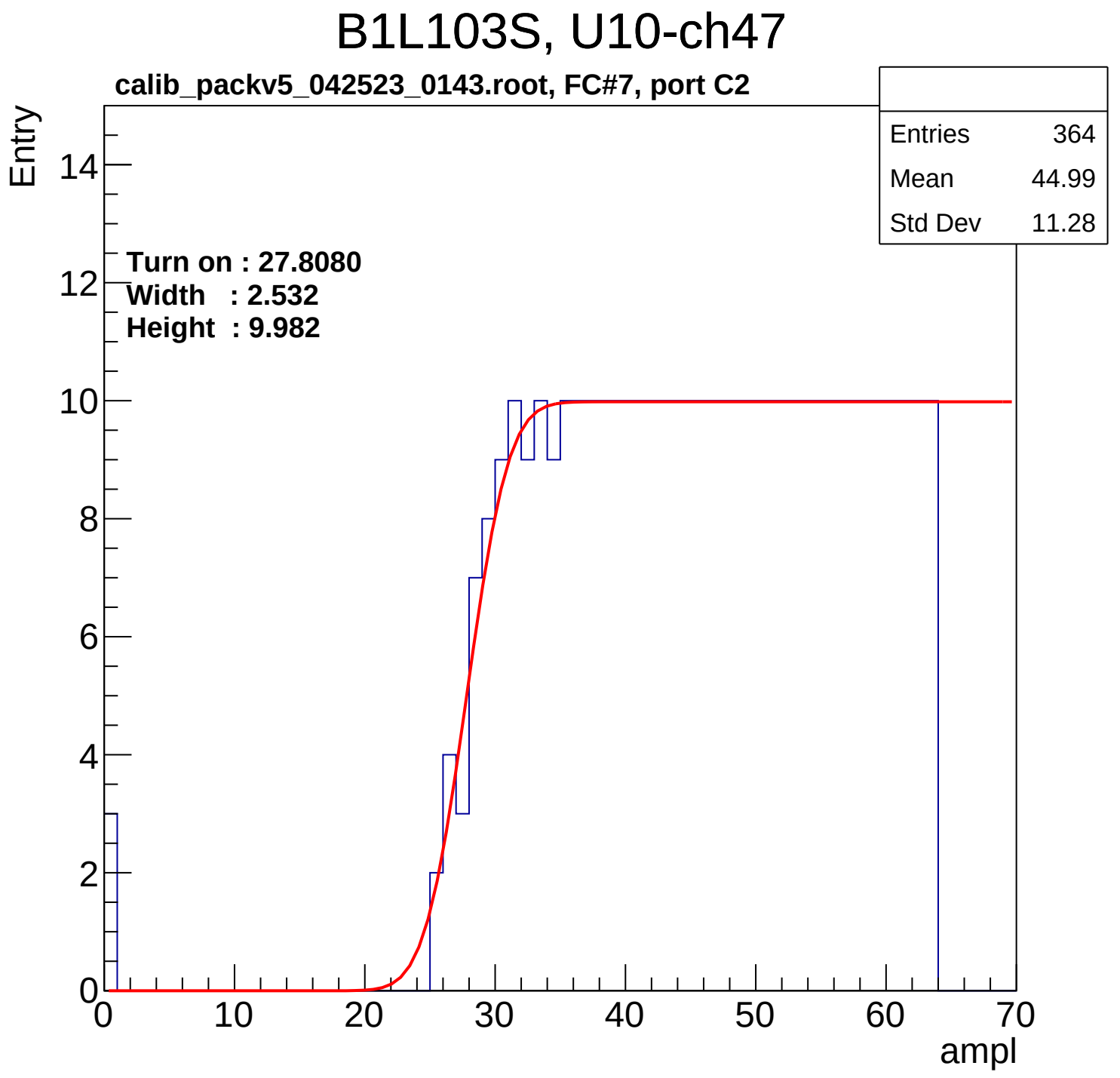
B1L103S, U10-ch47
calib_packv5_042523_0143.root, FC#7, port C2
Entries 364
Mean 44.99
Std Dev 11.28
Turn on : 27.8080
Width : 2.532
Height : 9.982
Entry
ampl
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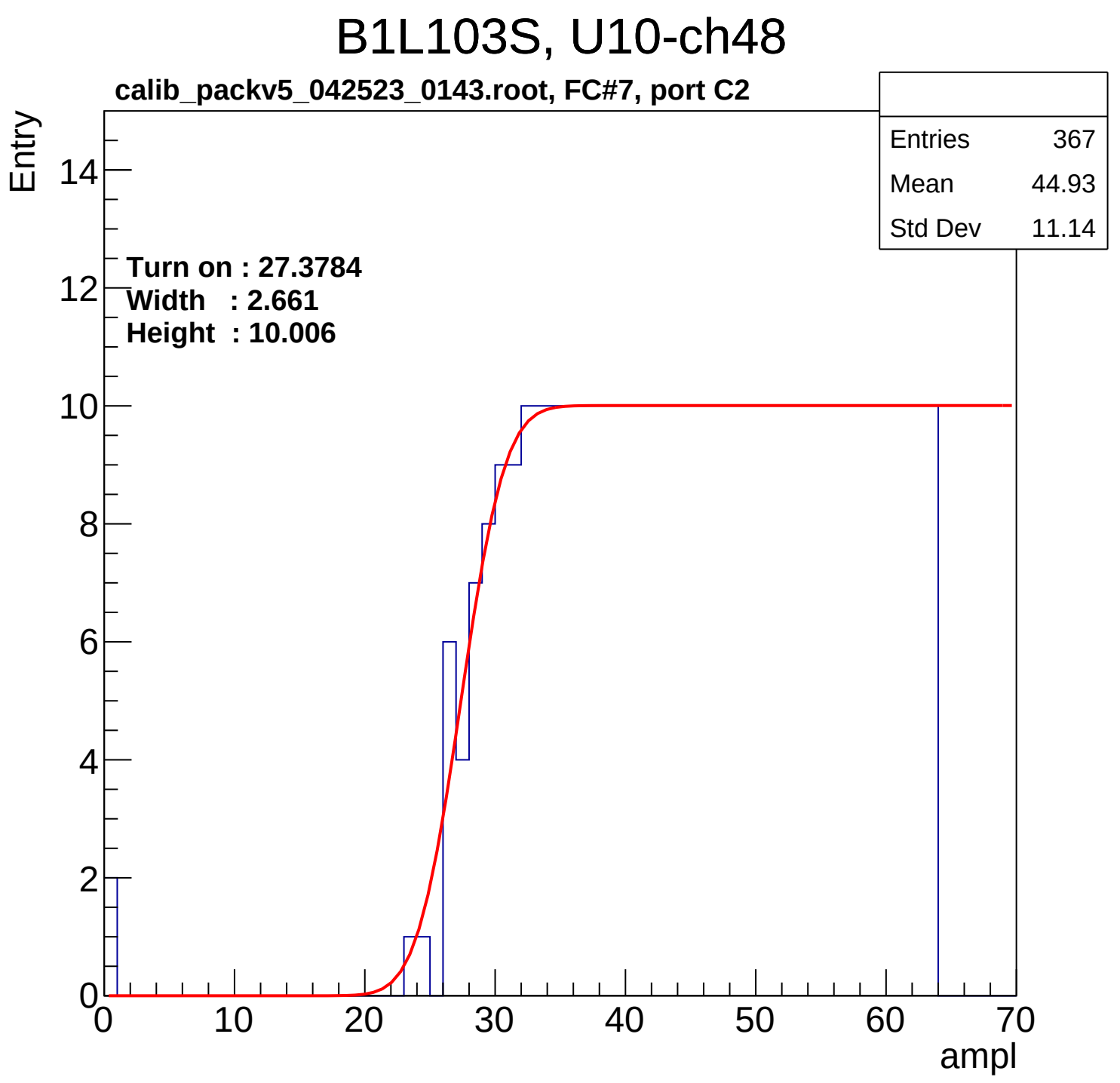
B1L103S, U10-ch48
calib_packv5_042523_0143.root, FC#7, port C2
Entries 367
Mean 44.93
Std Dev 11.14
Turn on : 27.3784
Width : 2.661
Height : 10.006
Entry
ampl
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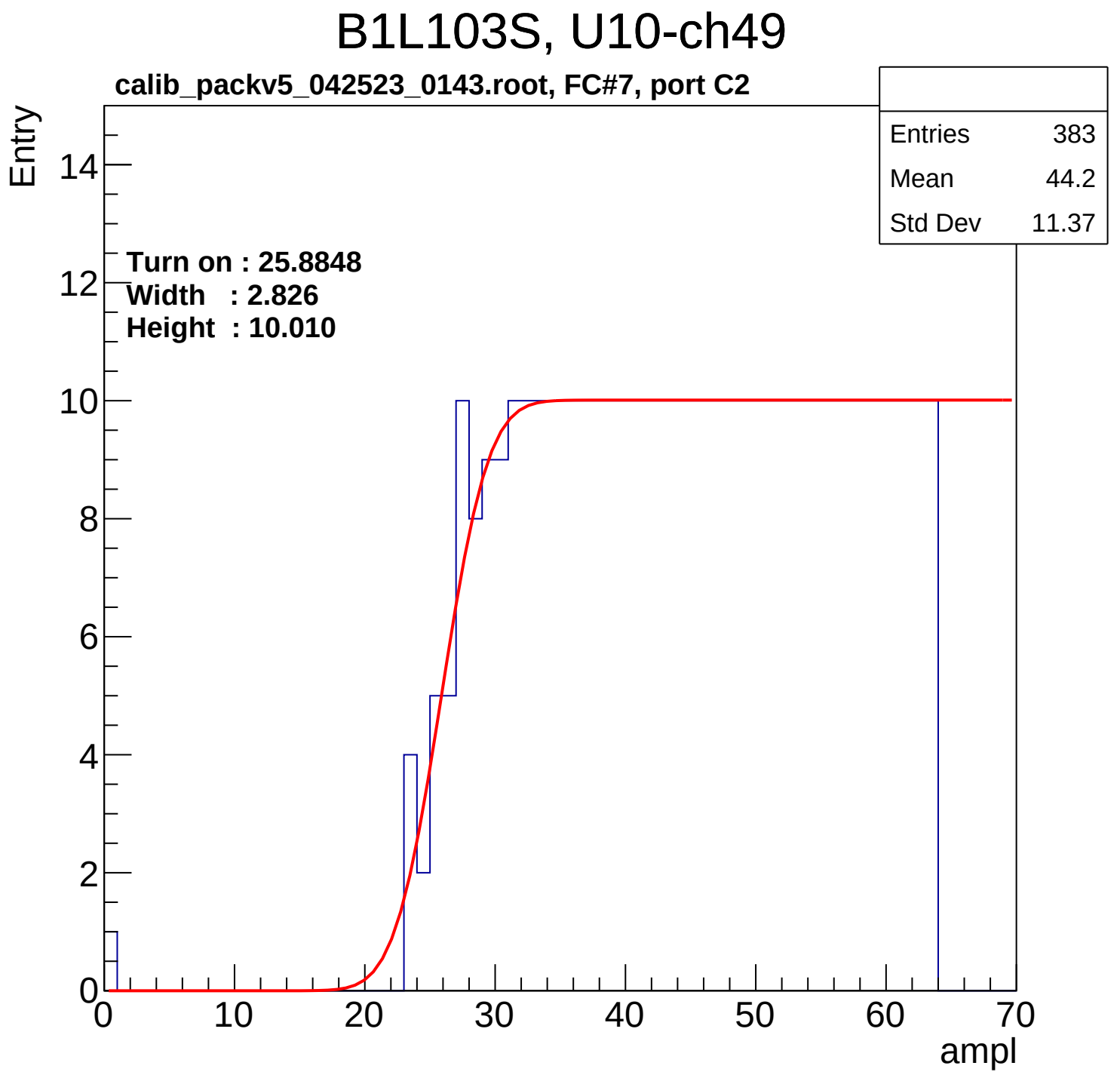
B1L103S, U10-ch49
calib_packv5_042523_0143.root, FC#7, port C2
Entries 383
Mean 44.2
Std Dev 11.37
Turn on : 25.8848
Width : 2.826
Height : 10.010
Entry
ampl
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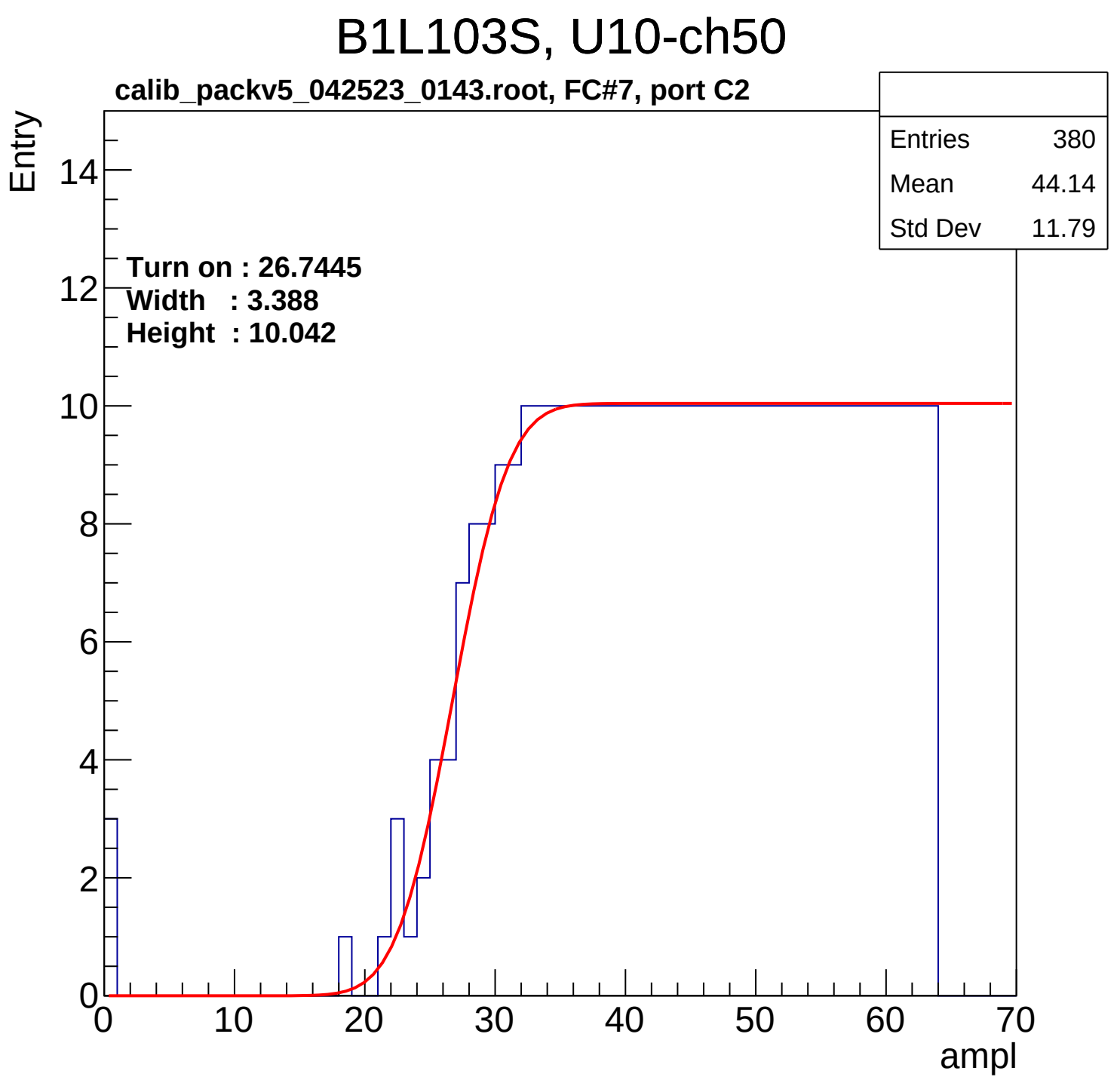
B1L103S, U10-ch50
calib_packv5_042523_0143.root, FC#7, port C2
Entries 380
Mean 44.14
Std Dev 11.79
Turn on : 26.7445
Width : 3.388
Height : 10.042
Entry
ampl
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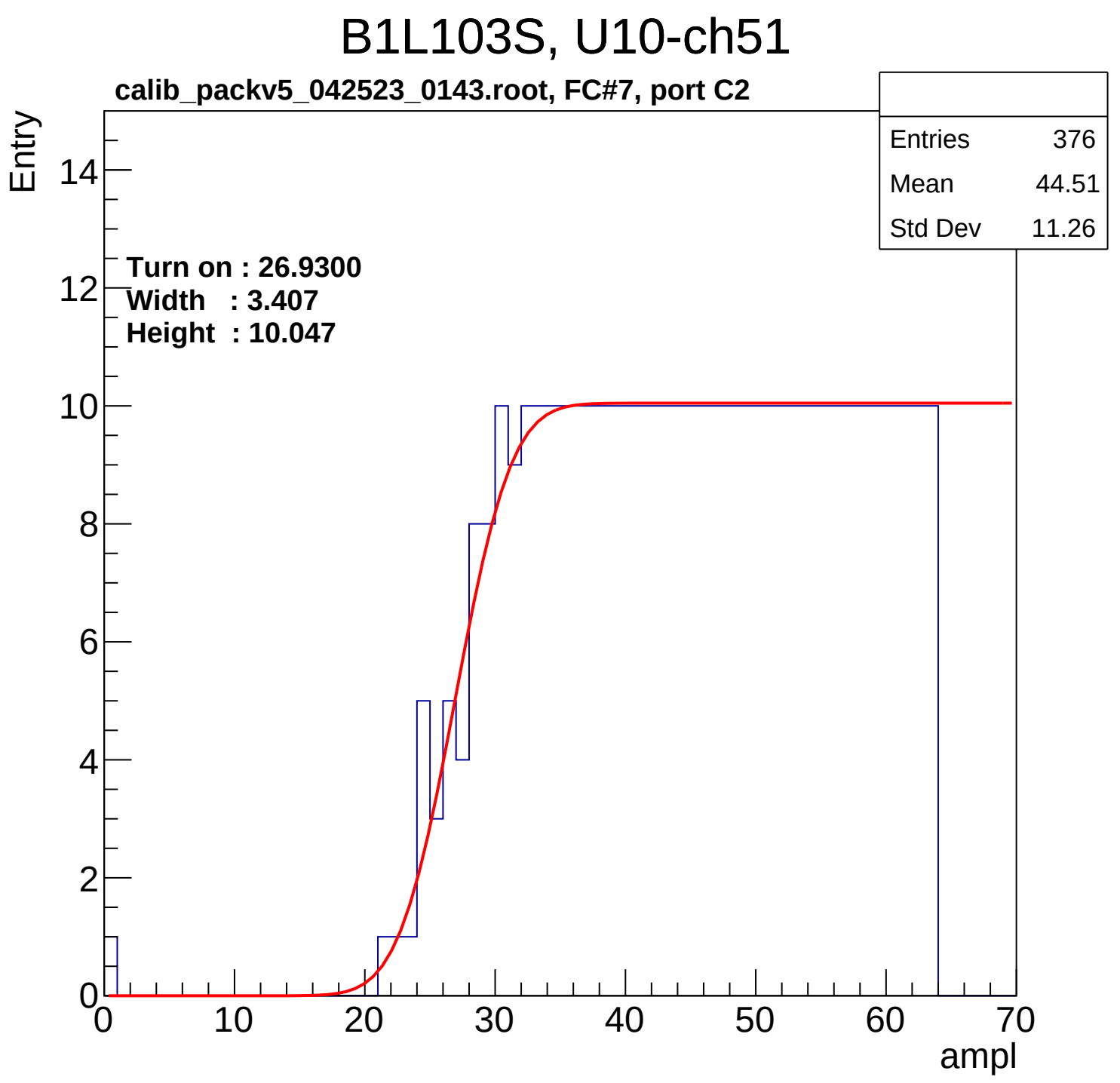
B1L103S, U10-ch51
calib_packv5_042523_0143.root, FC#7, port C2
Entries 376
Mean 44.51
Std Dev 11.26
Turn on : 26.9300
Width : 3.407
Height : 10.047
Entry
ampl
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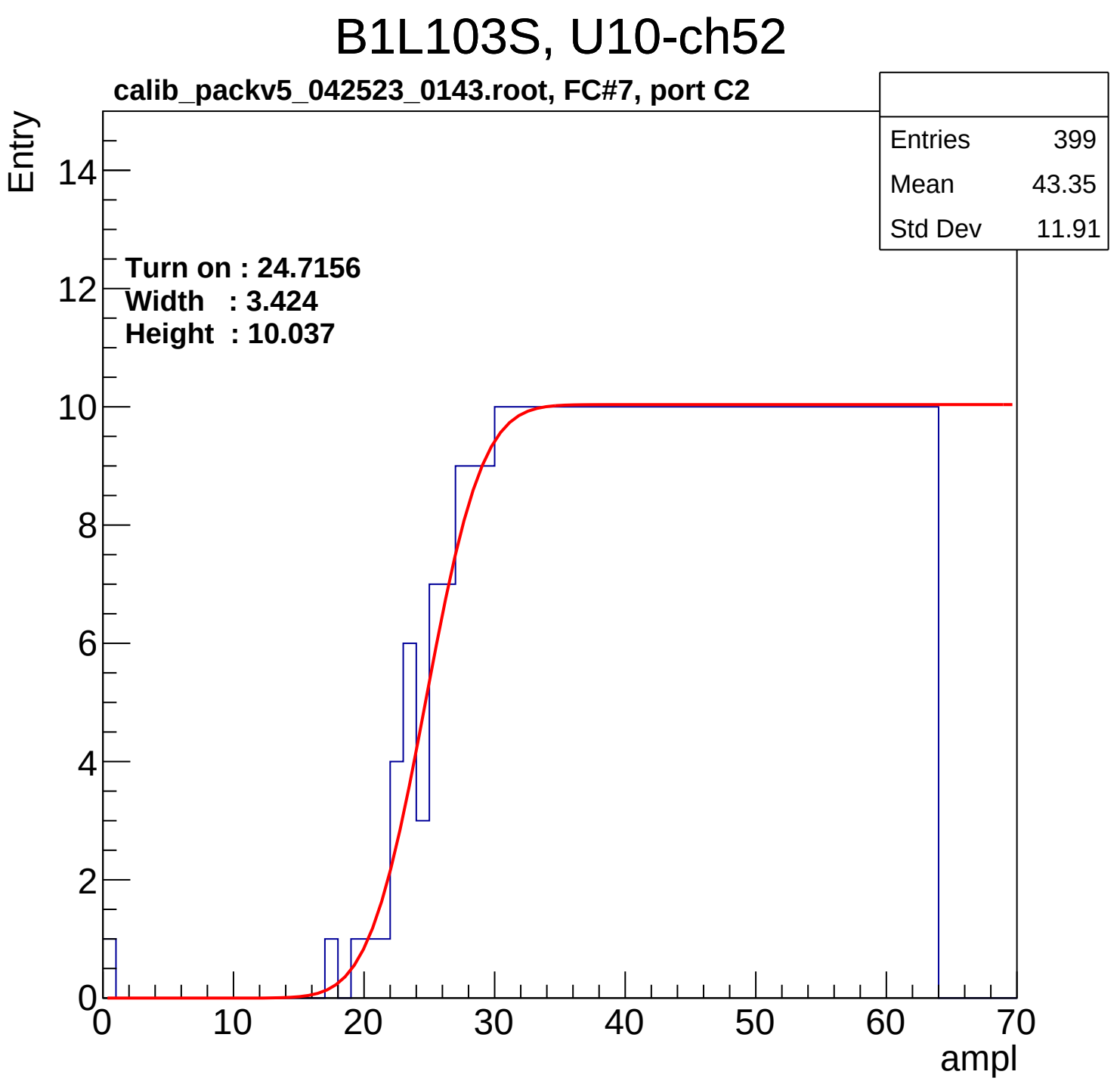
B1L103S, U10-ch52
calib_packv5_042523_0143.root, FC#7, port C2
Entries 399
Mean 43.35
Std Dev 11.91
Turn on : 24.7156
Width : 3.424
Height : 10.037
Entry
ampl
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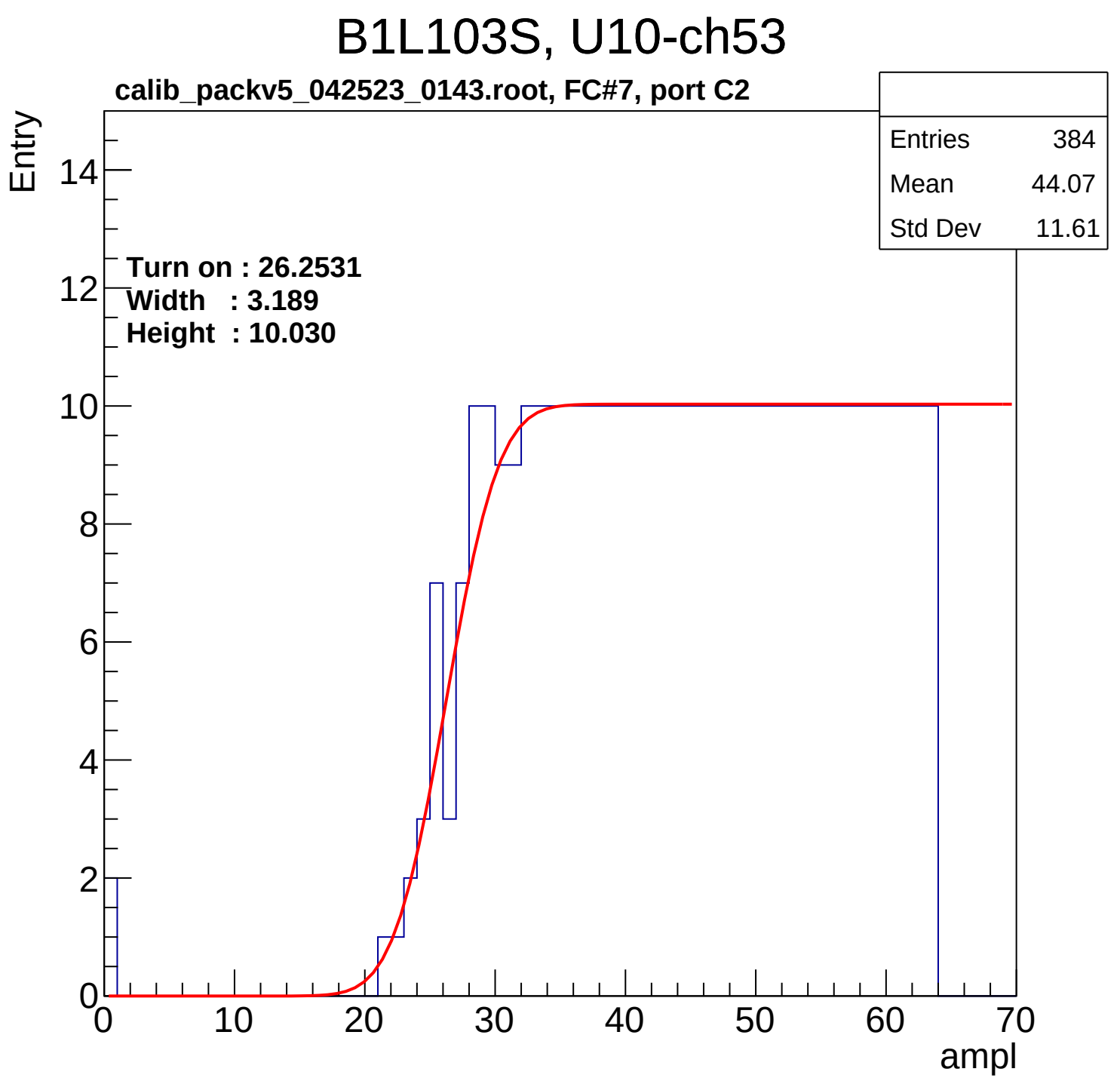
B1L103S, U10-ch53
calib_packv5_042523_0143.root, FC#7, port C2
Entries 384
Mean 44.07
Std Dev 11.61
Turn on : 26.2531
Width : 3.189
Height : 10.030
Entry
ampl
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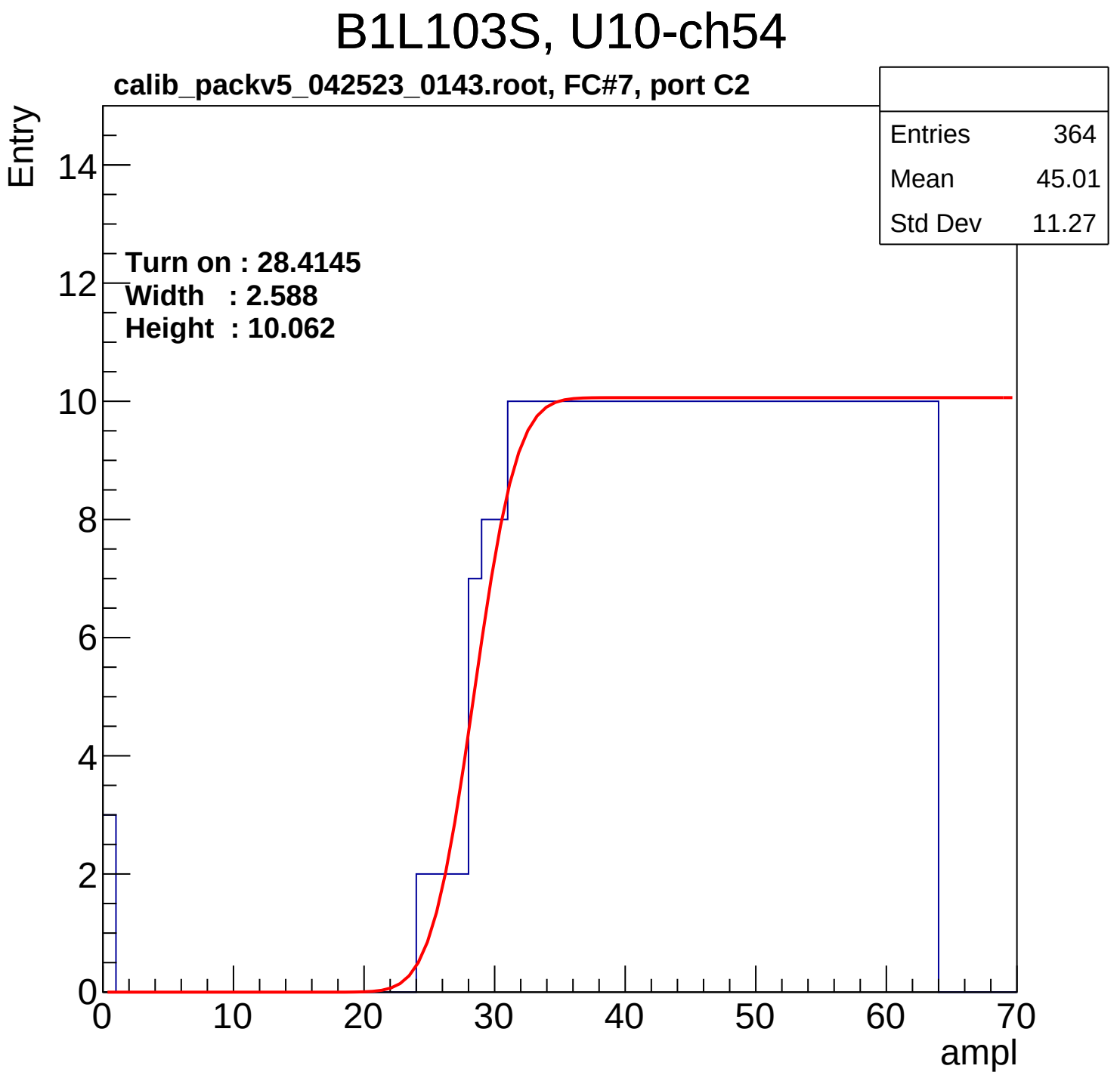
B1L103S, U10-ch54
calib_packv5_042523_0143.root, FC#7, port C2
Entries 364
Mean 45.01
Std Dev 11.27
Turn on : 28.4145
Width : 2.588
Height : 10.062
Entry
ampl
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4
6
8
10
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0
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60
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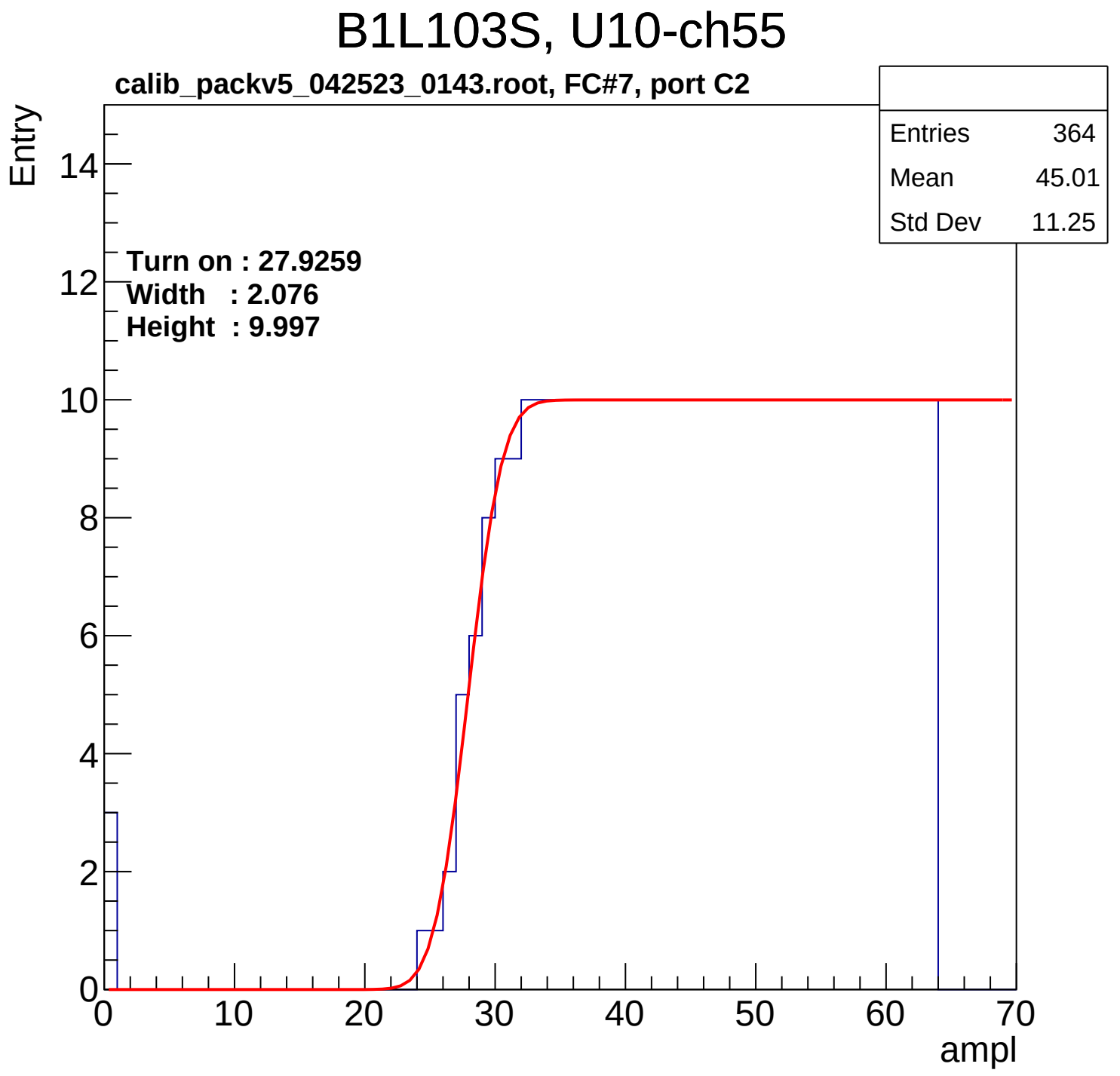
B1L103S, U10-ch55
calib_packv5_042523_0143.root, FC#7, port C2
Entries 364
Mean 45.01
Std Dev 11.25
Turn on : 27.9259
Width : 2.076
Height : 9.997
Entry
ampl
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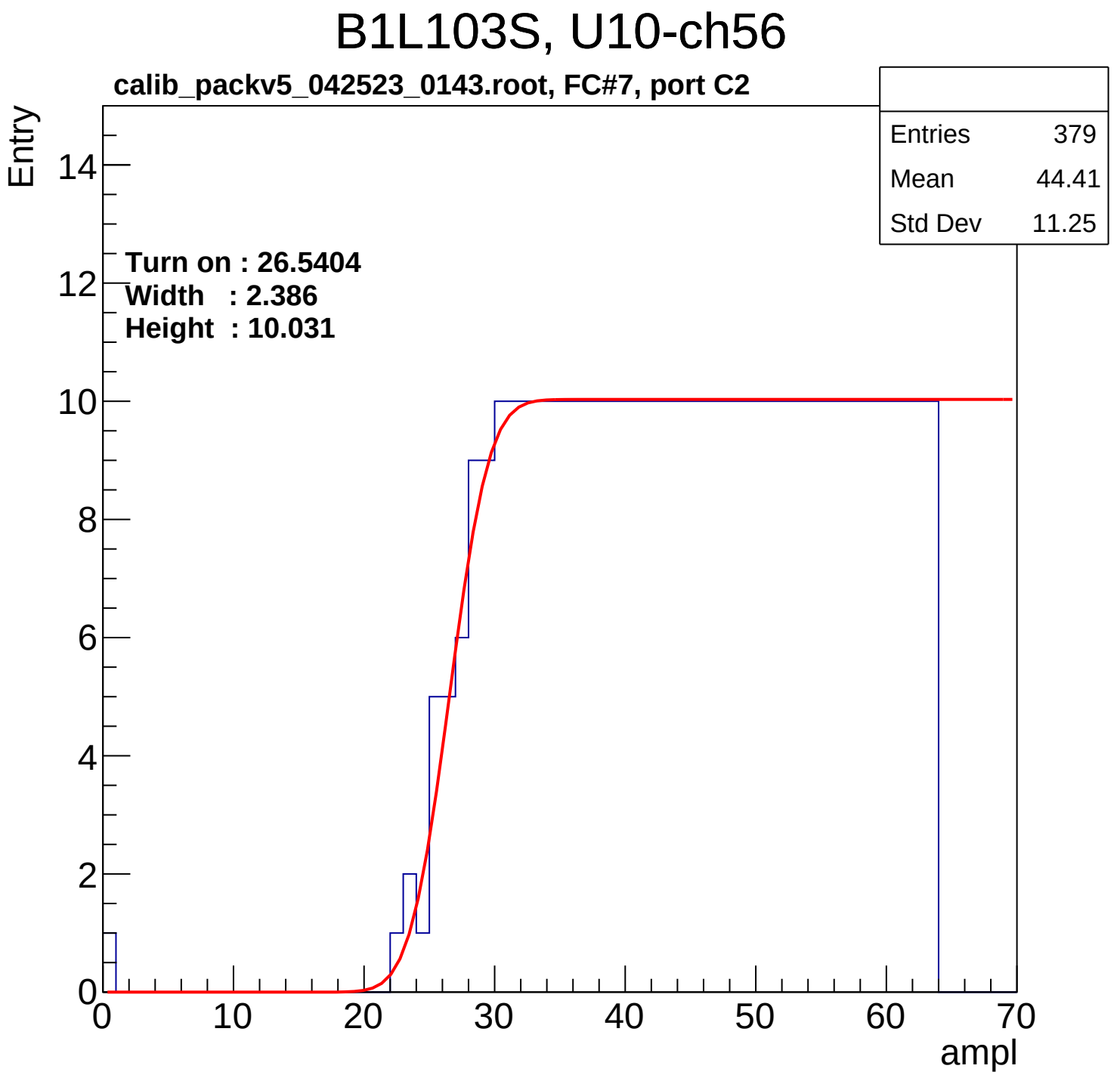
B1L103S, U10-ch56
calib_packv5_042523_0143.root, FC#7, port C2
Entries 379
Mean 44.41
Std Dev 11.25
Turn on : 26.5404
Width : 2.386
Height : 10.031
Entry
ampl
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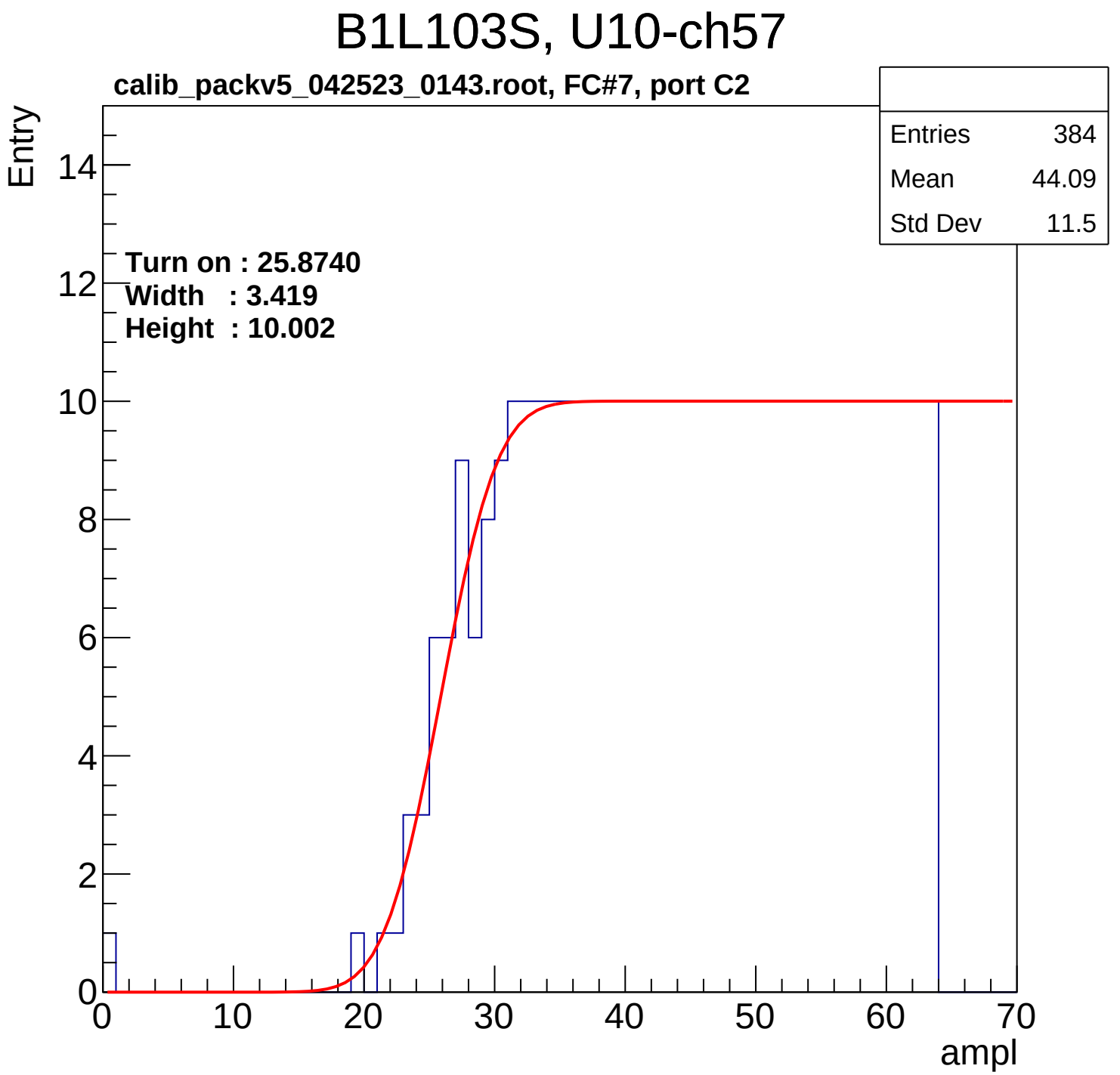
B1L103S, U10-ch57
calib_packv5_042523_0143.root, FC#7, port C2
Entries 384
Mean 44.09
Std Dev 11.5
Turn on : 25.8740
Width : 3.419
Height : 10.002
Entry
ampl
0
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4
6
8
10
12
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0
10
20
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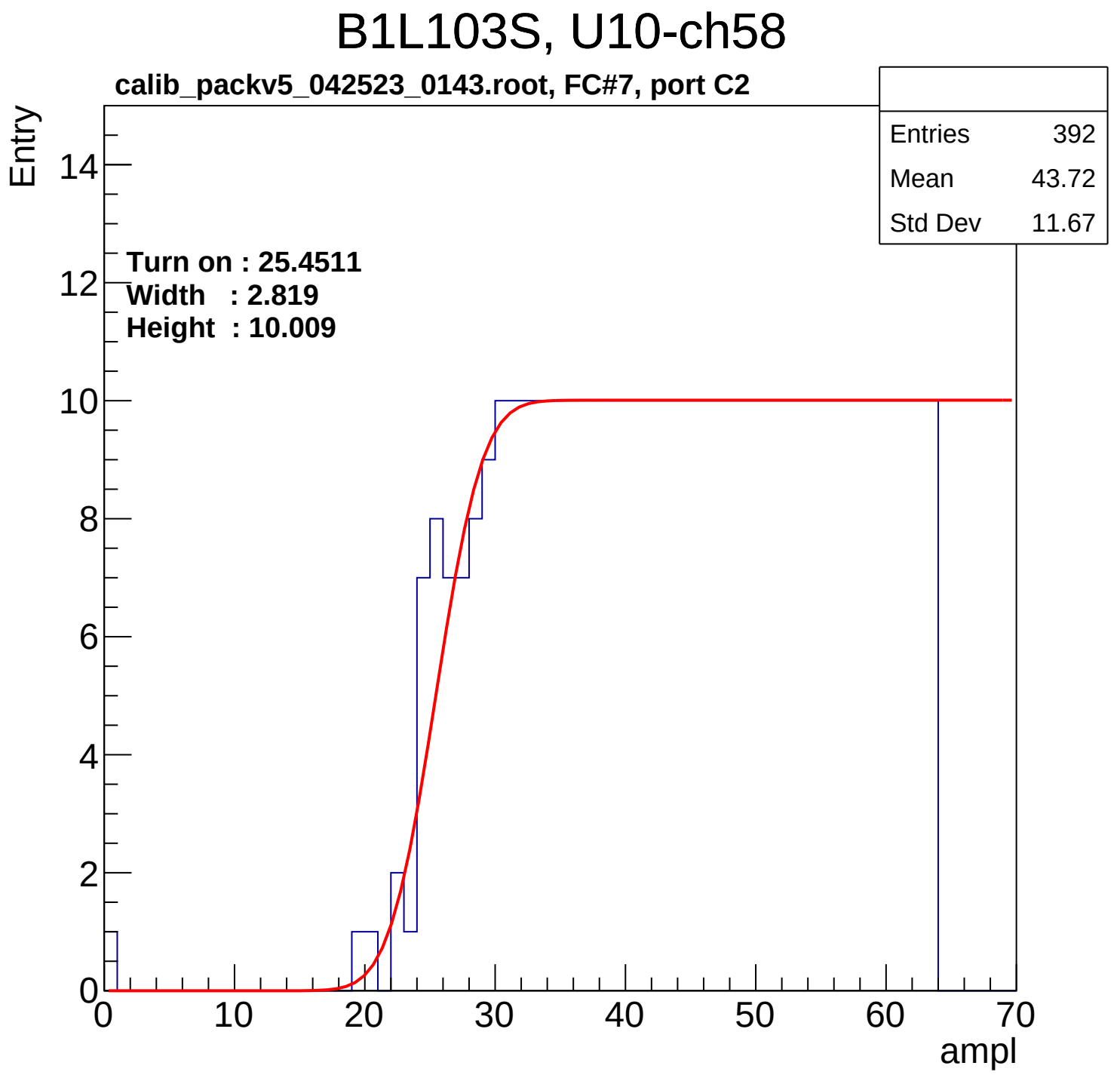
B1L103S, U10-ch58
calib_packv5_042523_0143.root, FC#7, port C2
Entries 392
Mean 43.72
Std Dev 11.67
Turn on : 25.4511
Width : 2.819
Height : 10.009
Entry
ampl
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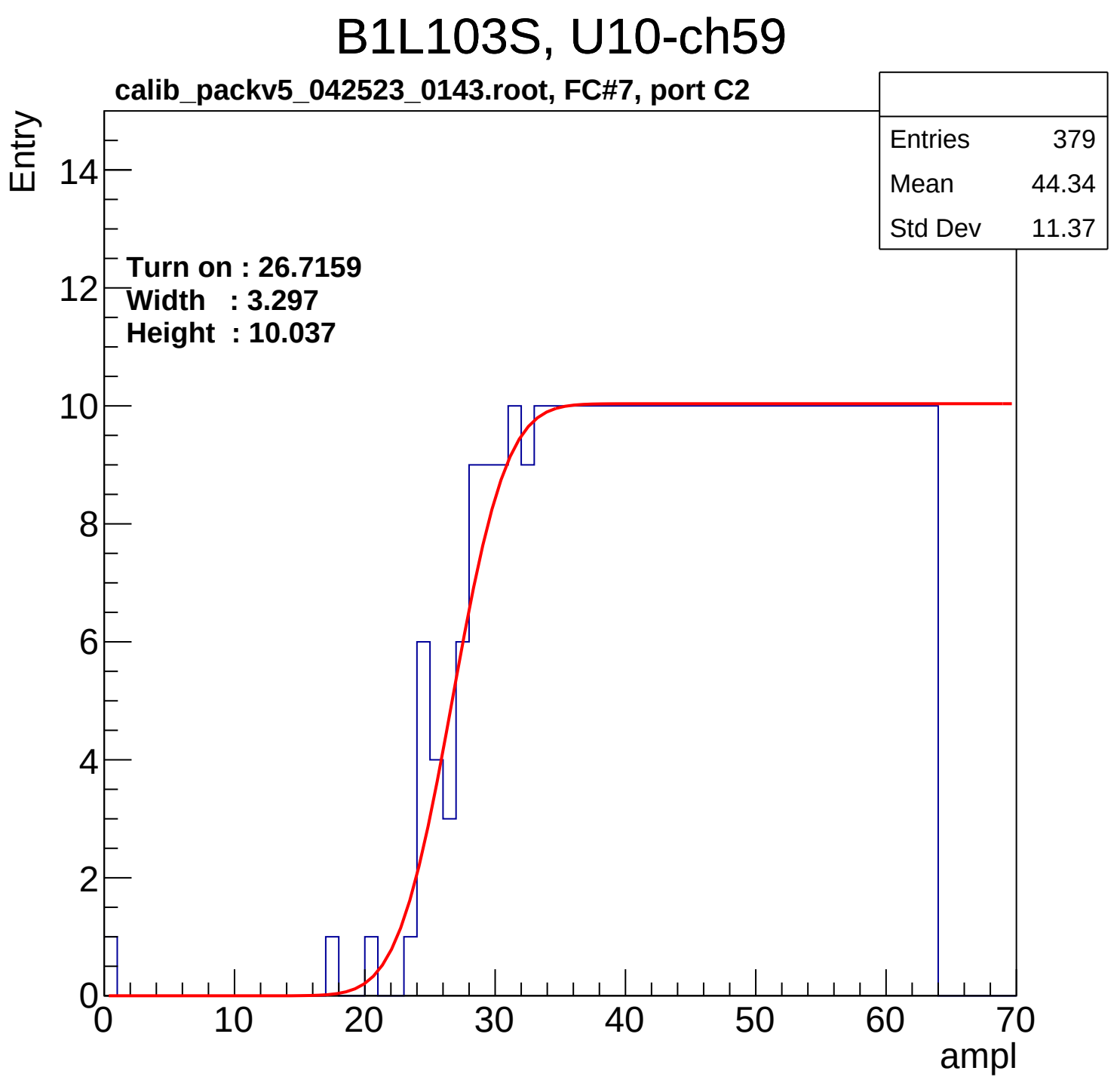
B1L103S, U10-ch59
calib_packv5_042523_0143.root, FC#7, port C2
Entries 379
Mean 44.34
Std Dev 11.37
Turn on : 26.7159
Width : 3.297
Height : 10.037
Entry
ampl
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2
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6
8
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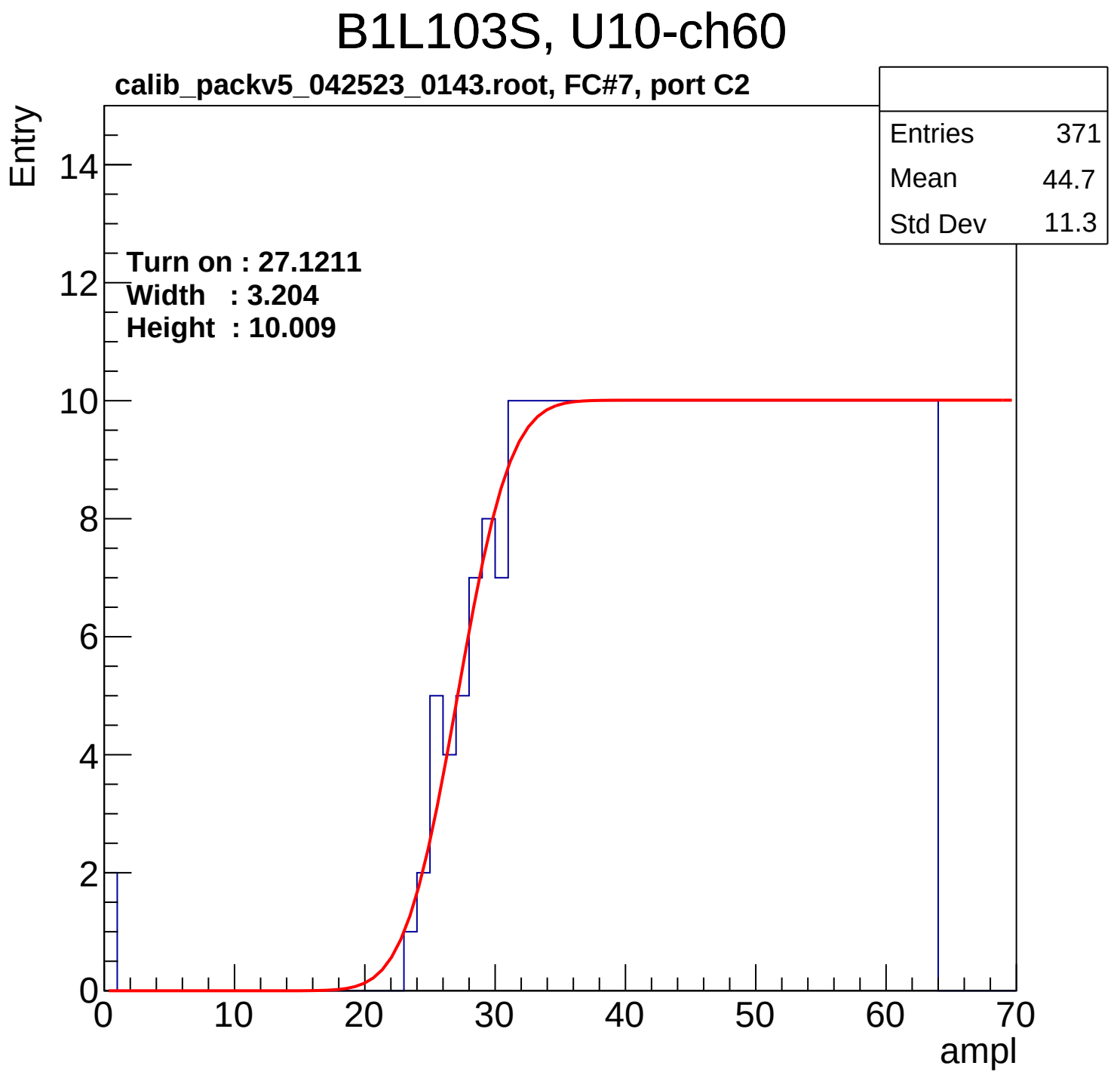
B1L103S, U10-ch60
calib_packv5_042523_0143.root, FC#7, port C2
Entries 371
Mean 44.7
Std Dev 11.3
Turn on : 27.1211
Width : 3.204
Height : 10.009
Entry
ampl
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2
4
6
8
10
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0
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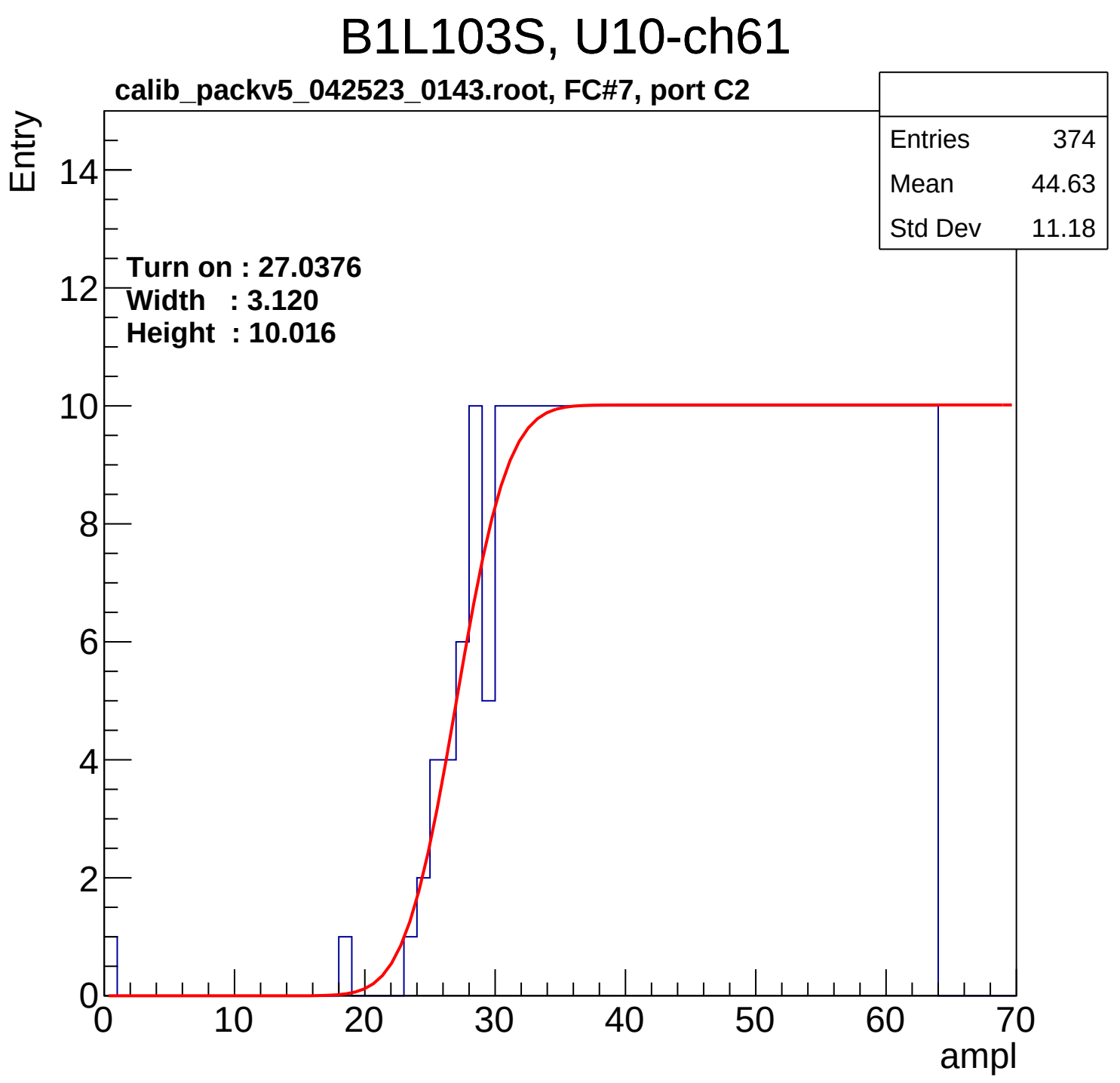
B1L103S, U10-ch61
calib_packv5_042523_0143.root, FC#7, port C2
Entries 374
Mean 44.63
Std Dev 11.18
Turn on : 27.0376
Width : 3.120
Height : 10.016
Entry
ampl
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2
4
6
8
10
12
14
0
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20
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60
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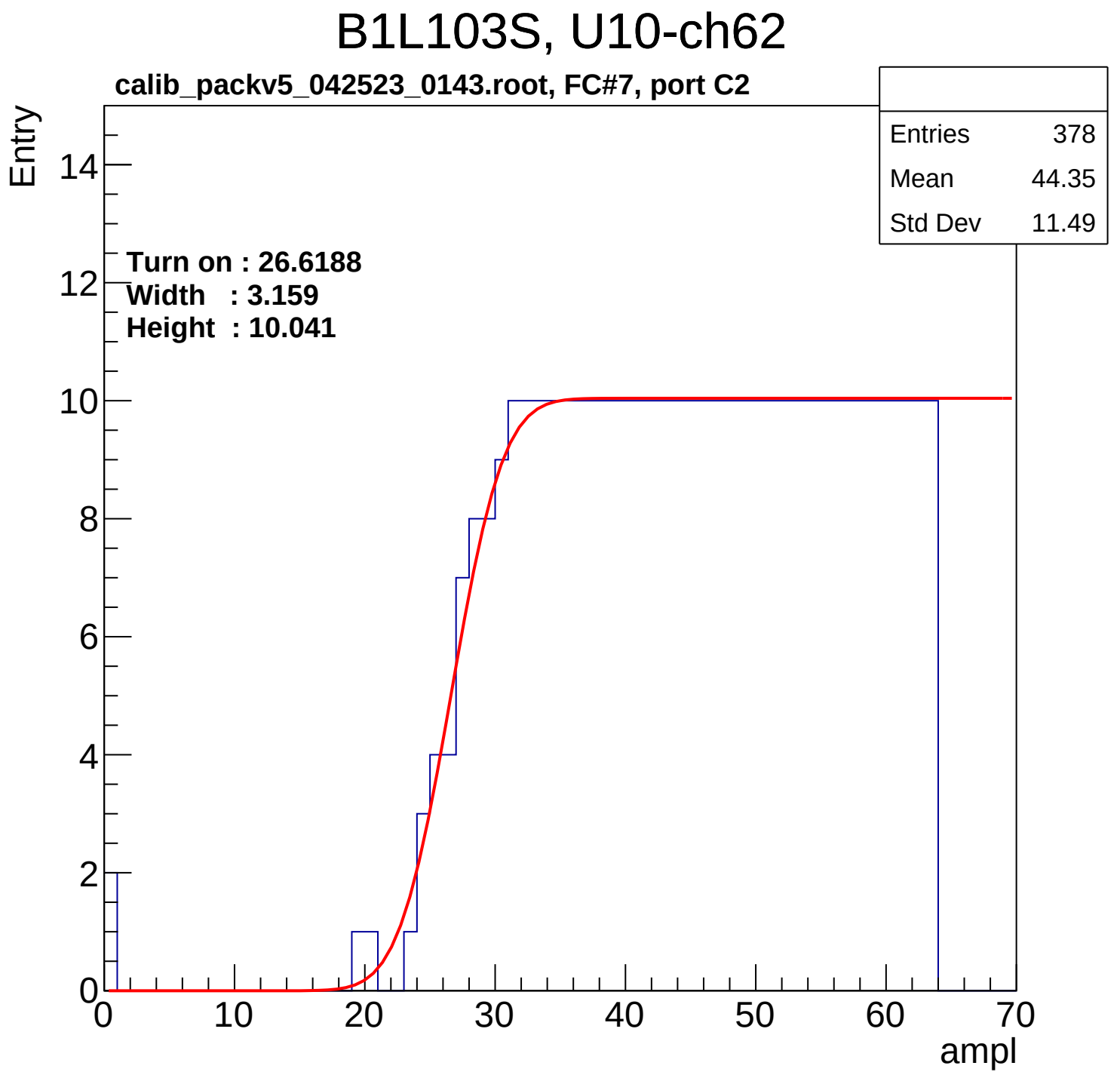
B1L103S, U10-ch62
calib_packv5_042523_0143.root, FC#7, port C2
Entries 378
Mean 44.35
Std Dev 11.49
Turn on : 26.6188
Width : 3.159
Height : 10.041
Entry
ampl
0
2
4
6
8
10
12
14
0
10
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40
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60
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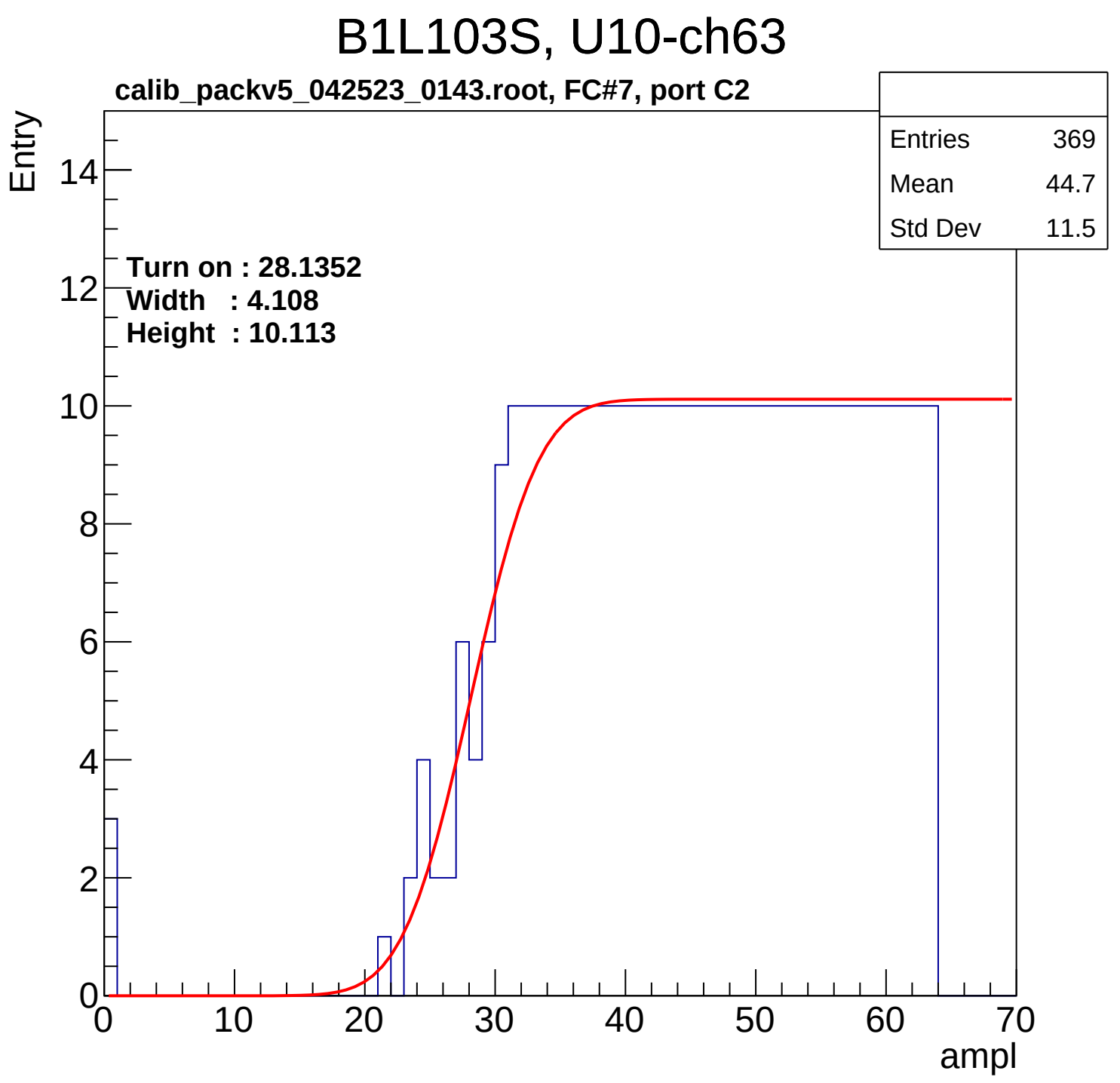
B1L103S, U10-ch63
calib_packv5_042523_0143.root, FC#7, port C2
Entries 369
Mean 44.7
Std Dev 11.5
Turn on : 28.1352
Width : 4.108
Height : 10.113
Entry
ampl
0
2
4
6
8
10
12
14
0
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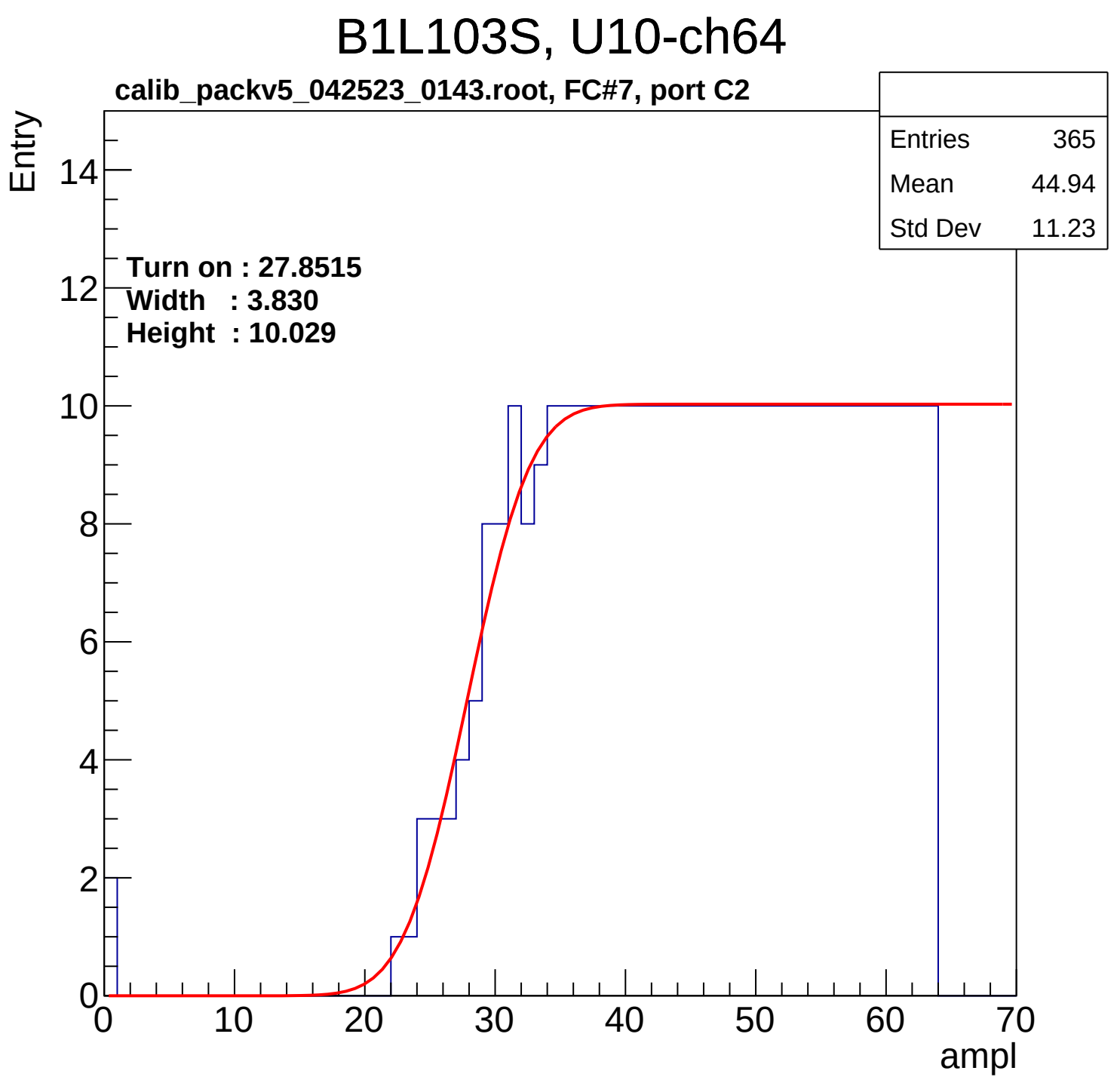
B1L103S, U10-ch64
calib_packv5_042523_0143.root, FC#7, port C2
Entries 365
Mean 44.94
Std Dev 11.23
Turn on : 27.8515
Width : 3.830
Height : 10.029
Entry
ampl
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4
6
8
10
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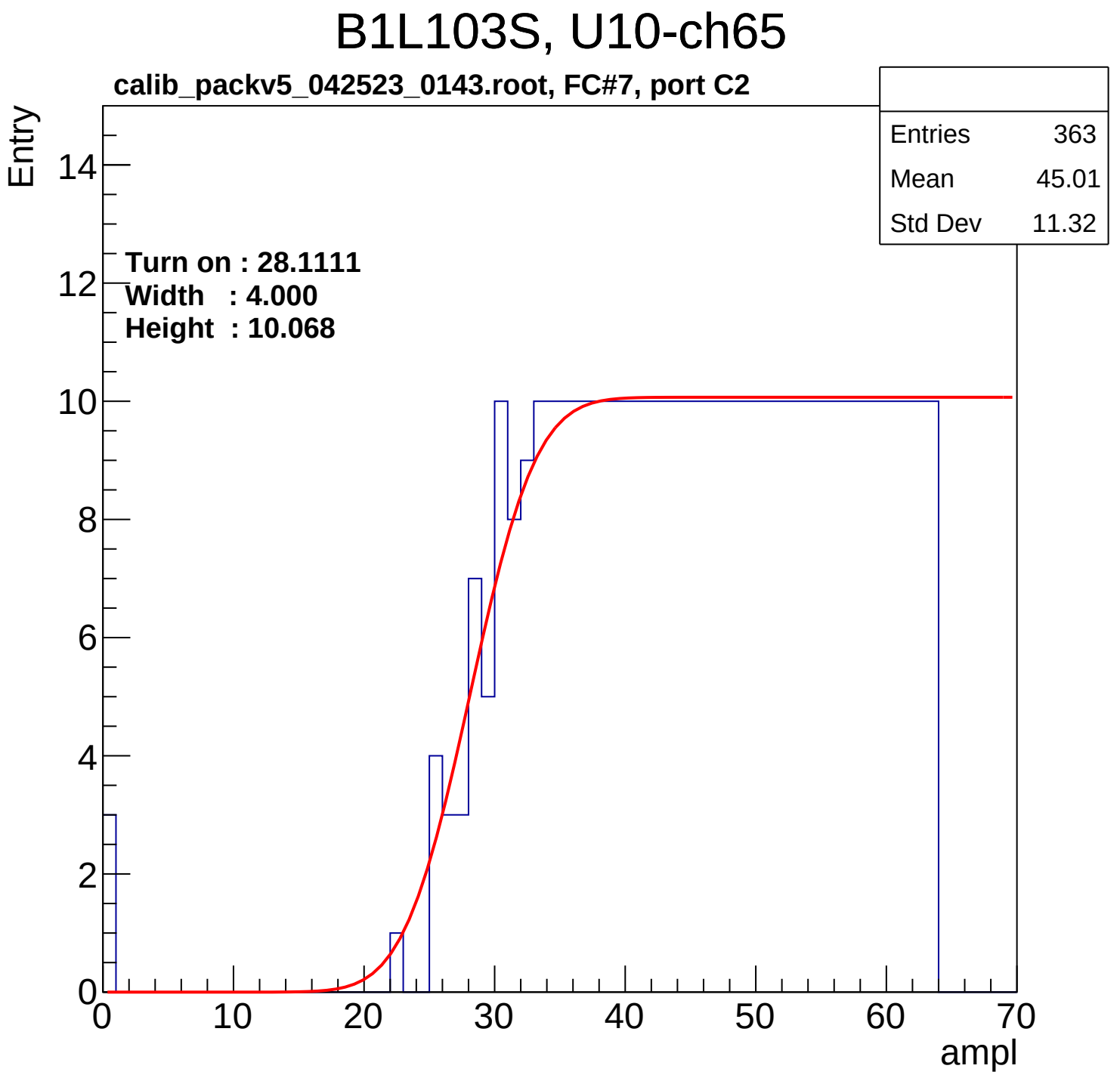
B1L103S, U10-ch65
calib_packv5_042523_0143.root, FC#7, port C2
Entries 363
Mean 45.01
Std Dev 11.32
Turn on : 28.1111
Width : 4.000
Height : 10.068
Entry
ampl
0
2
4
6
8
10
12
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0
10
20
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40
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60
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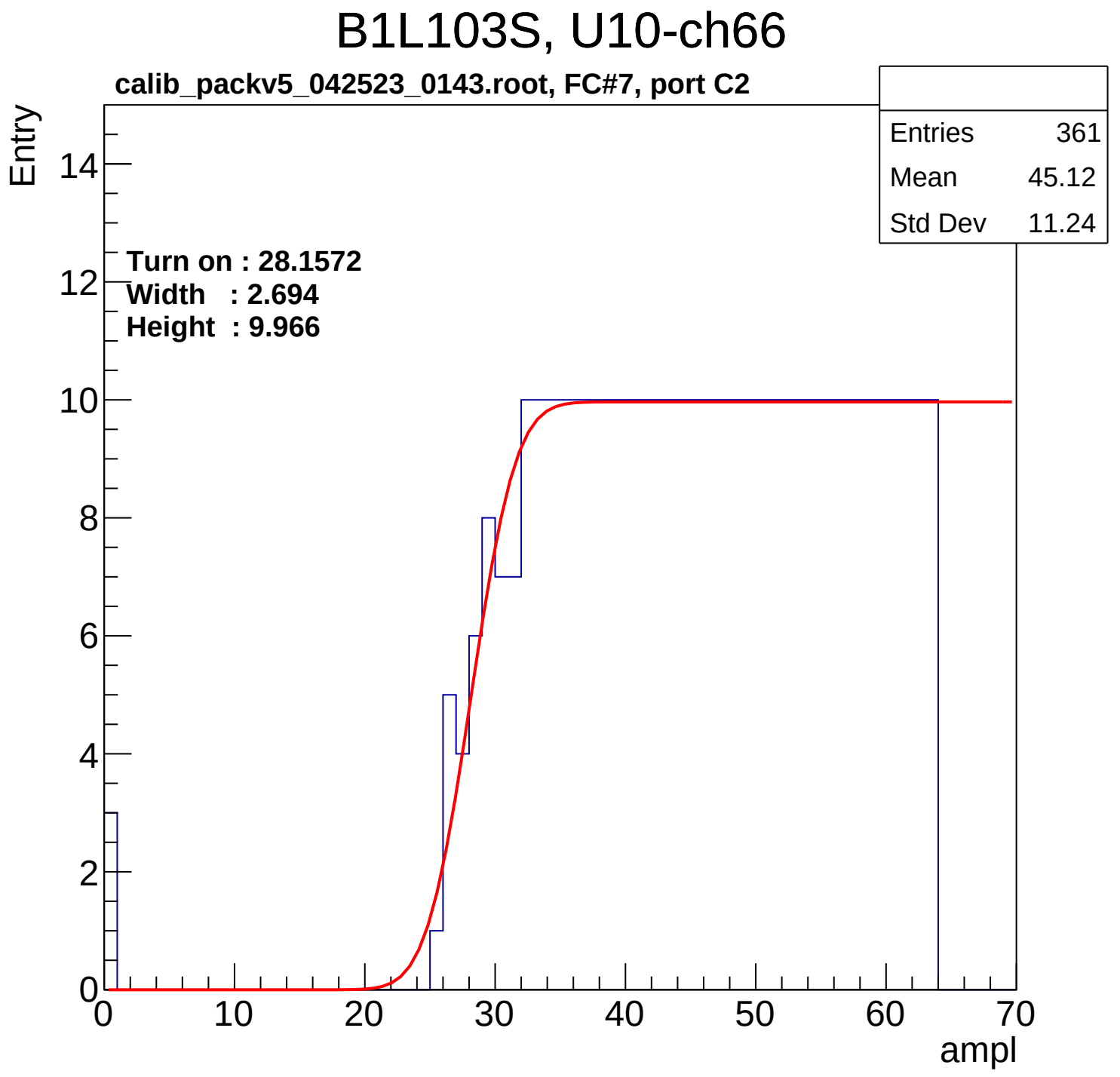
B1L103S, U10-ch66
calib_packv5_042523_0143.root, FC#7, port C2
Entries 361
Mean 45.12
Std Dev 11.24
Turn on : 28.1572
Width : 2.694
Height : 9.966
Entry
ampl
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4
6
8
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0
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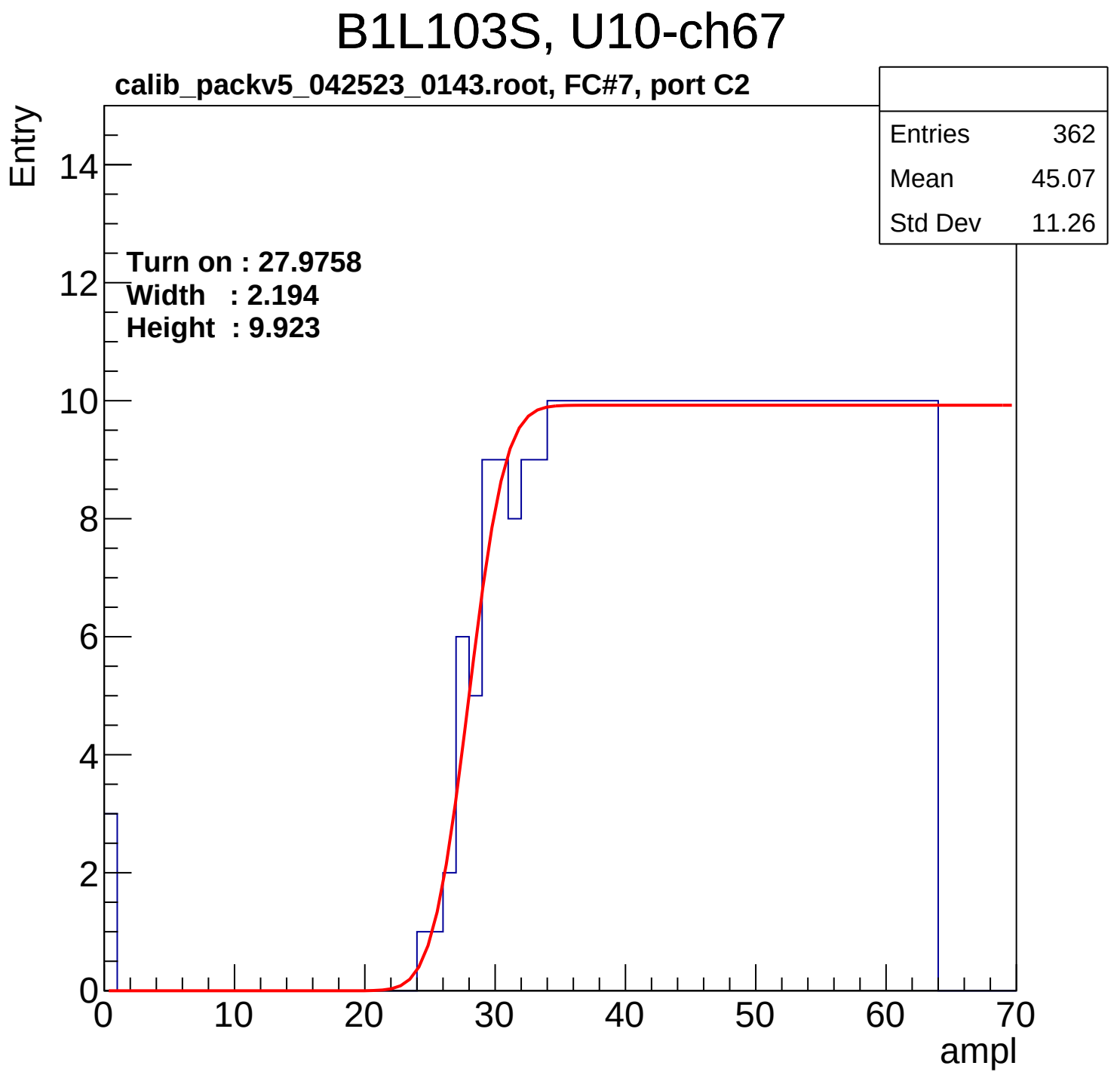
B1L103S, U10-ch67
calib_packv5_042523_0143.root, FC#7, port C2
Entries 362
Mean 45.07
Std Dev 11.26
Turn on : 27.9758
Width : 2.194
Height : 9.923
Entry
ampl
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2
4
6
8
10
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0
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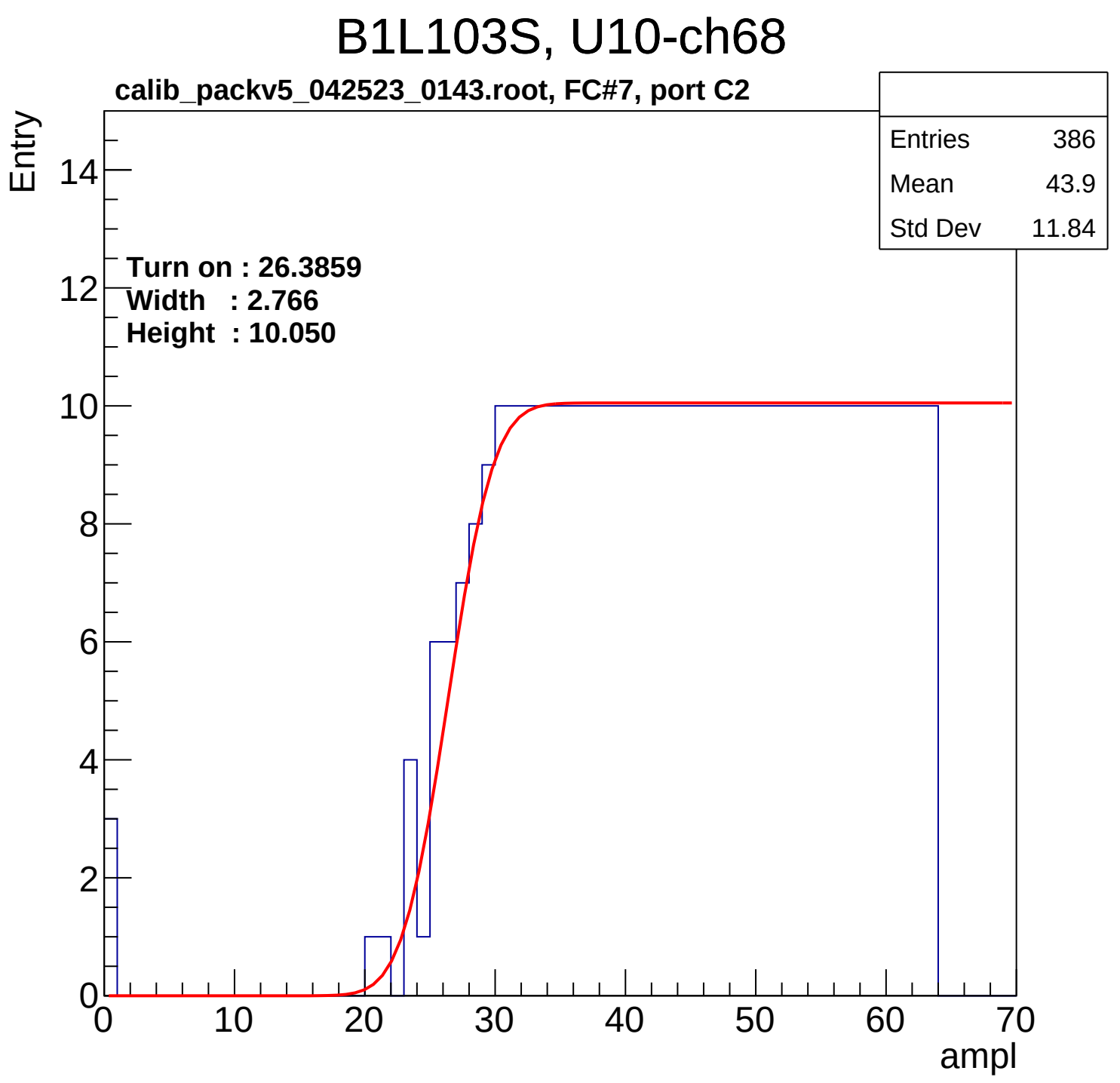
B1L103S, U10-ch68
calib_packv5_042523_0143.root, FC#7, port C2
Entries 386
Mean 43.9
Std Dev 11.84
Turn on : 26.3859
Width : 2.766
Height : 10.050
Entry
ampl
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2
4
6
8
10
12
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0
10
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60
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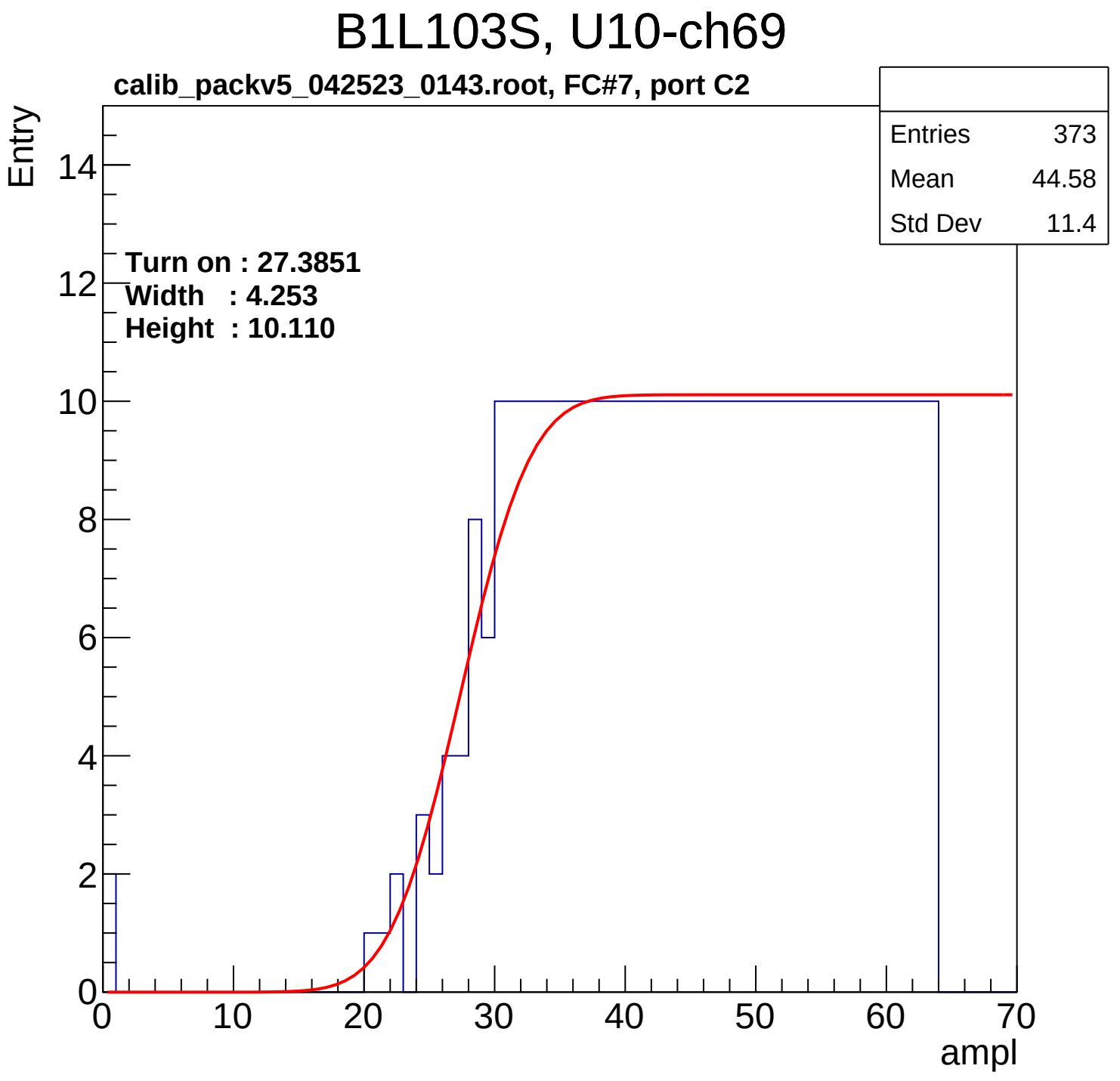
B1L103S, U10-ch69
calib_packv5_042523_0143.root, FC#7, port C2
Entries 373
Mean 44.58
Std Dev 11.4
Turn on : 27.3851
Width : 4.253
Height : 10.110
Entry
ampl
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6
8
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0
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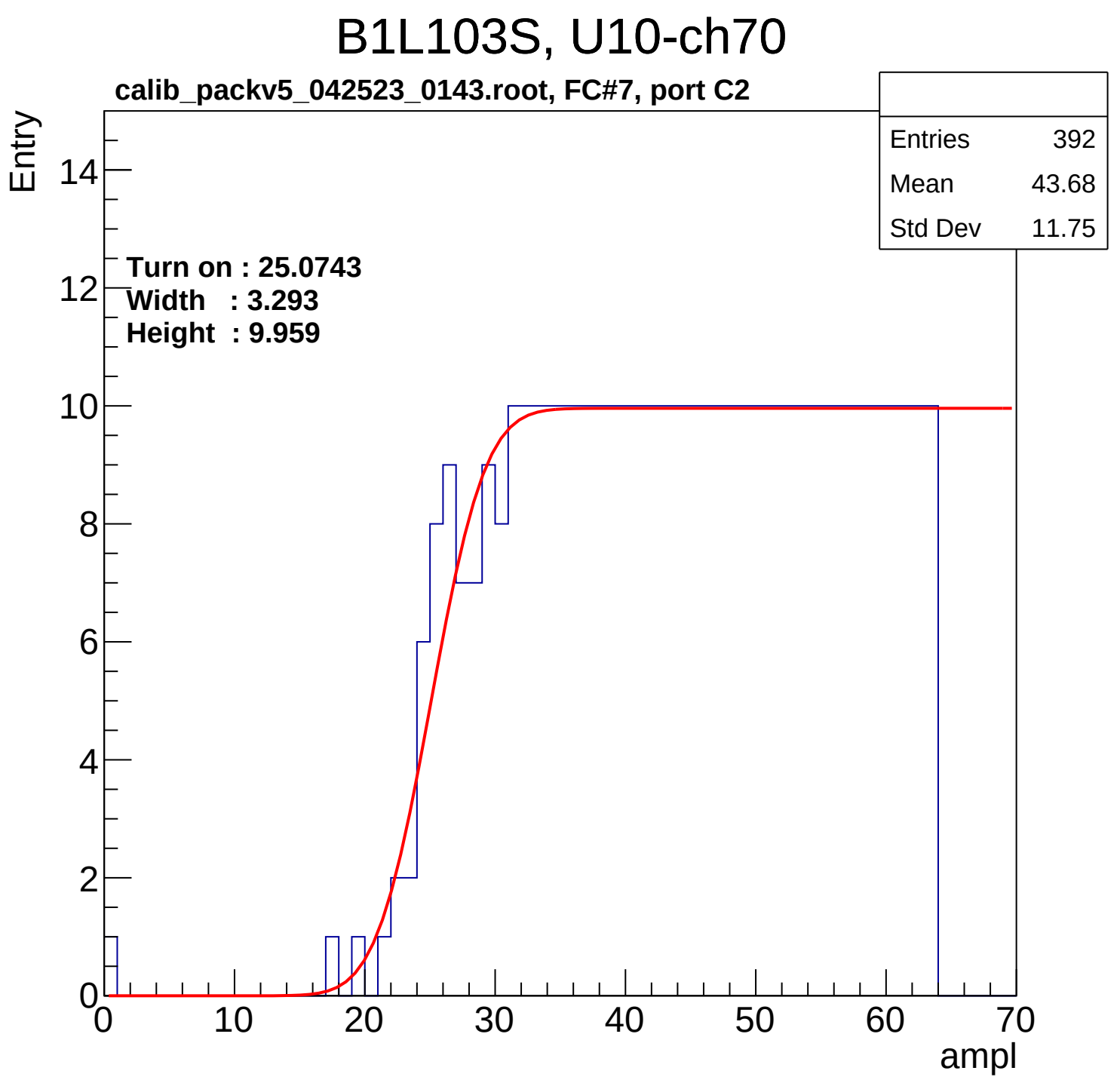
B1L103S, U10-ch70
calib_packv5_042523_0143.root, FC#7, port C2
Entries 392
Mean 43.68
Std Dev 11.75
Turn on : 25.0743
Width : 3.293
Height : 9.959
Entry
ampl
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6
8
10
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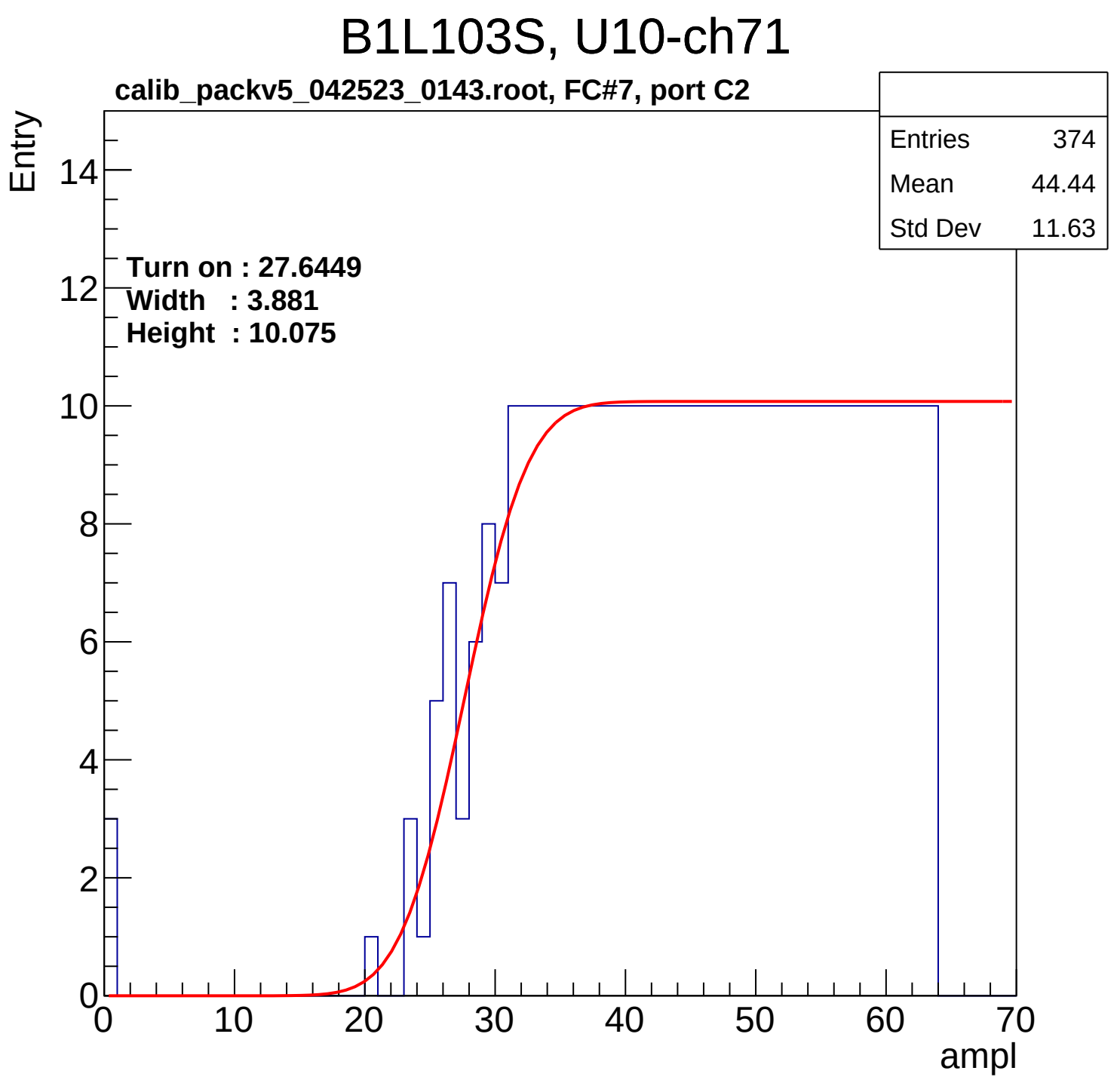
B1L103S, U10-ch71
calib_packv5_042523_0143.root, FC#7, port C2
Entries 374
Mean 44.44
Std Dev 11.63
Turn on : 27.6449
Width : 3.881
Height : 10.075
Entry
ampl
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6
8
10
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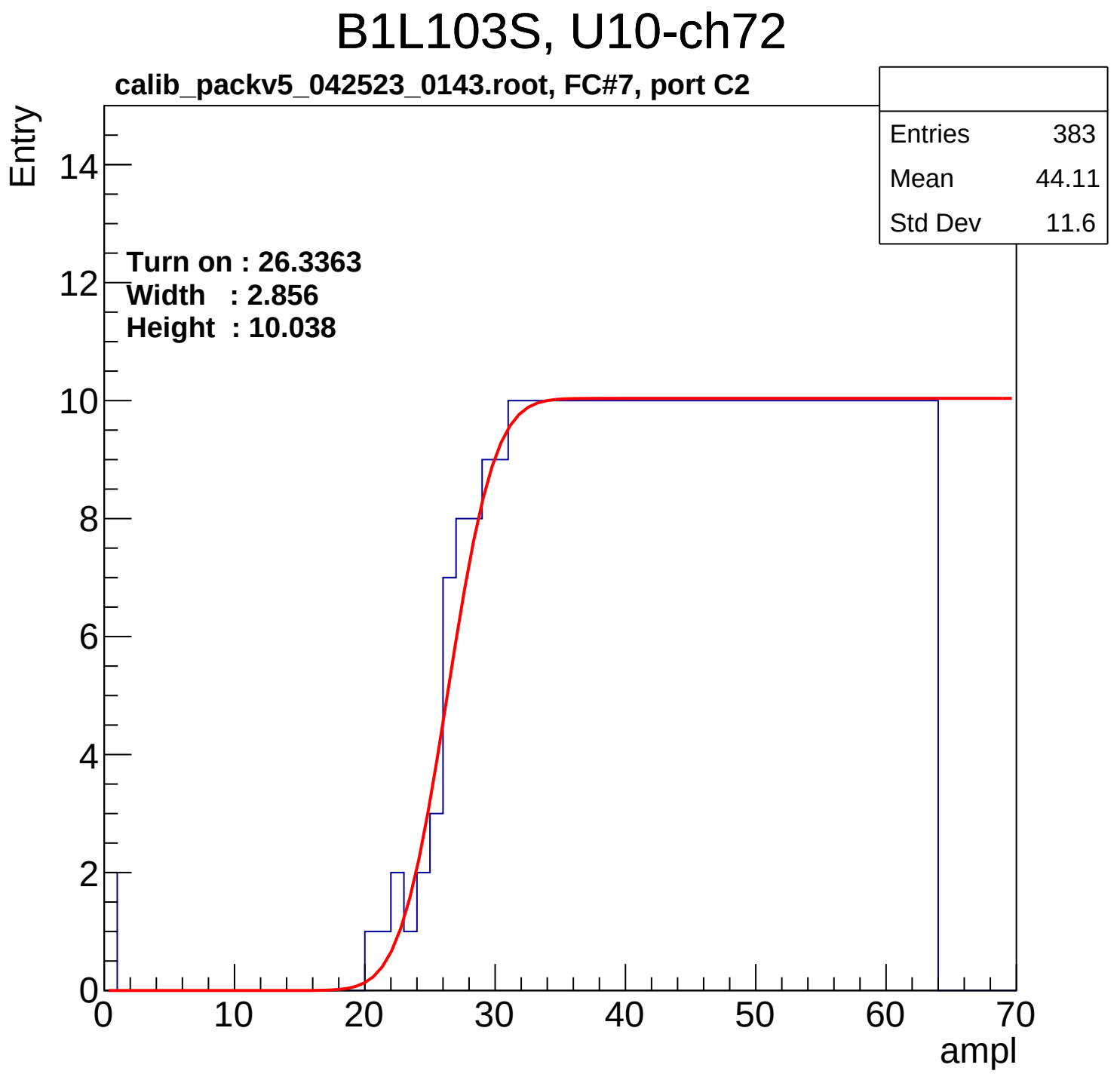
B1L103S, U10-ch72
calib_packv5_042523_0143.root, FC#7, port C2
Entries 383
Mean 44.11
Std Dev 11.6
Turn on : 26.3363
Width : 2.856
Height : 10.038
Entry
ampl
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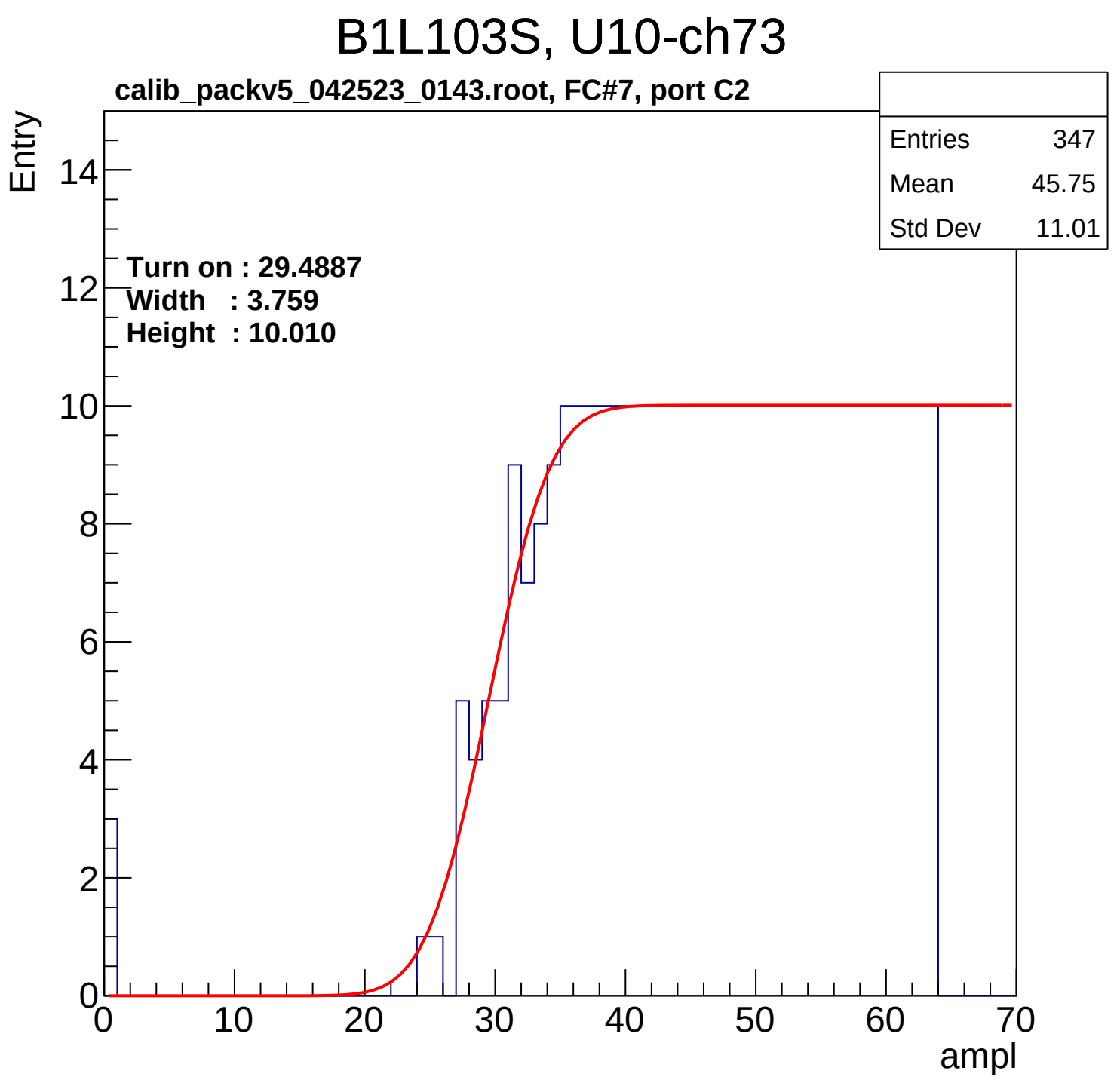
B1L103S, U10-ch73
calib_packv5_042523_0143.root, FC#7, port C2
Entries 347
Mean 45.75
Std Dev 11.01
Turn on : 29.4887
Width : 3.759
Height : 10.010
Entry
ampl
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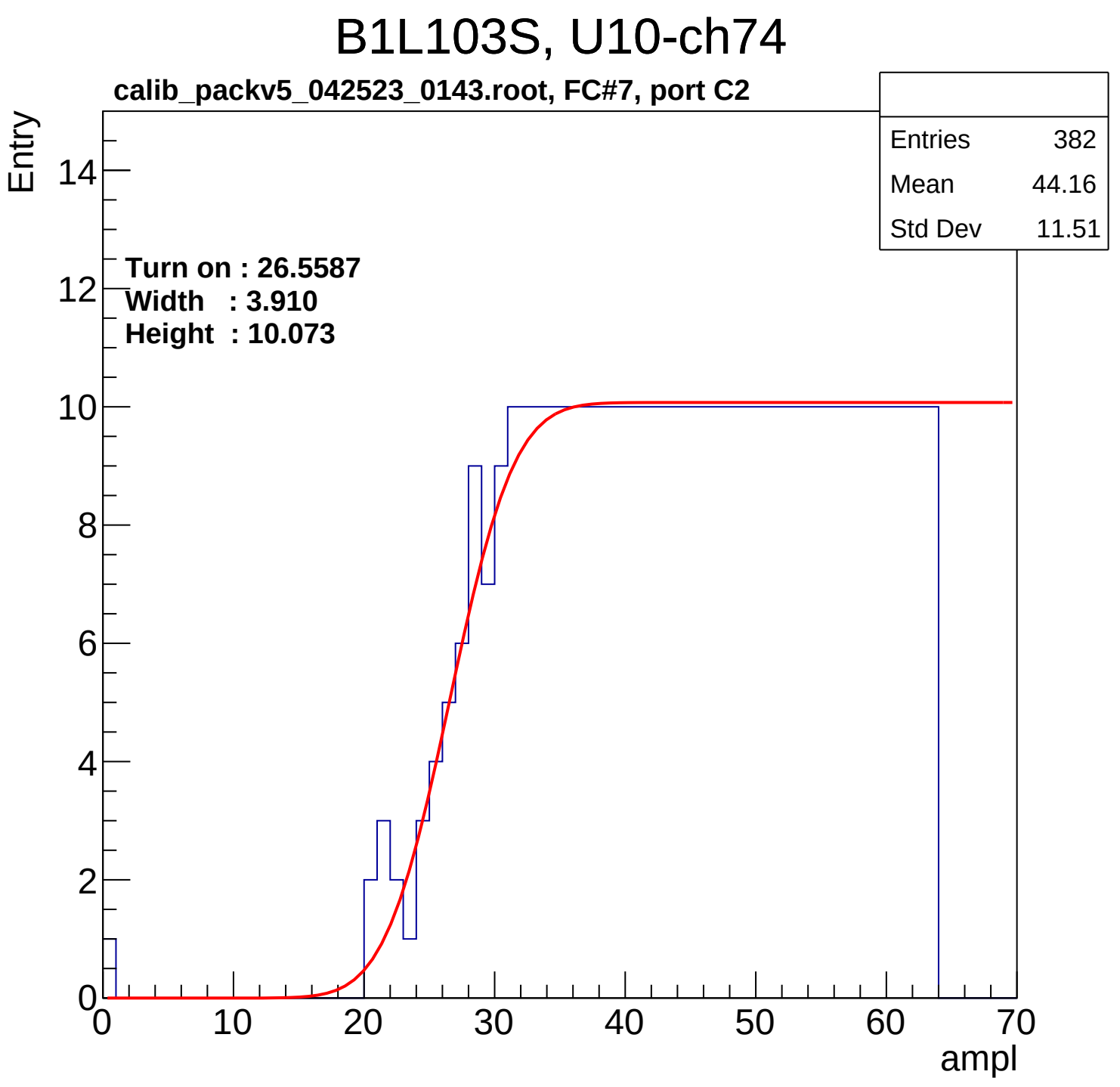
B1L103S, U10-ch74
calib_packv5_042523_0143.root, FC#7, port C2
Entries 382
Mean 44.16
Std Dev 11.51
Turn on : 26.5587
Width : 3.910
Height : 10.073
Entry
ampl
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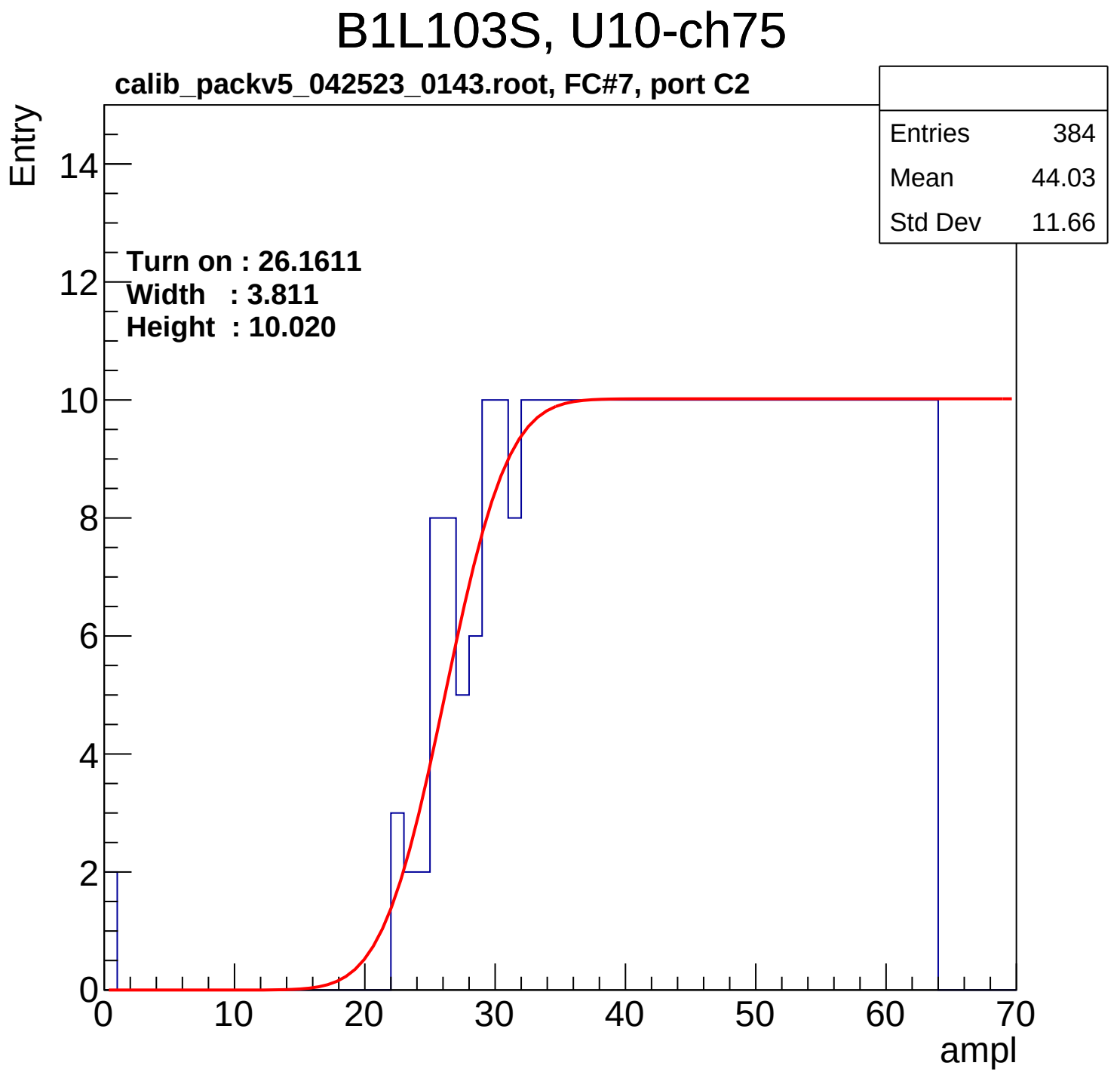
B1L103S, U10-ch75
calib_packv5_042523_0143.root, FC#7, port C2
Entries 384
Mean 44.03
Std Dev 11.66
Turn on : 26.1611
Width : 3.811
Height : 10.020
Entry
ampl
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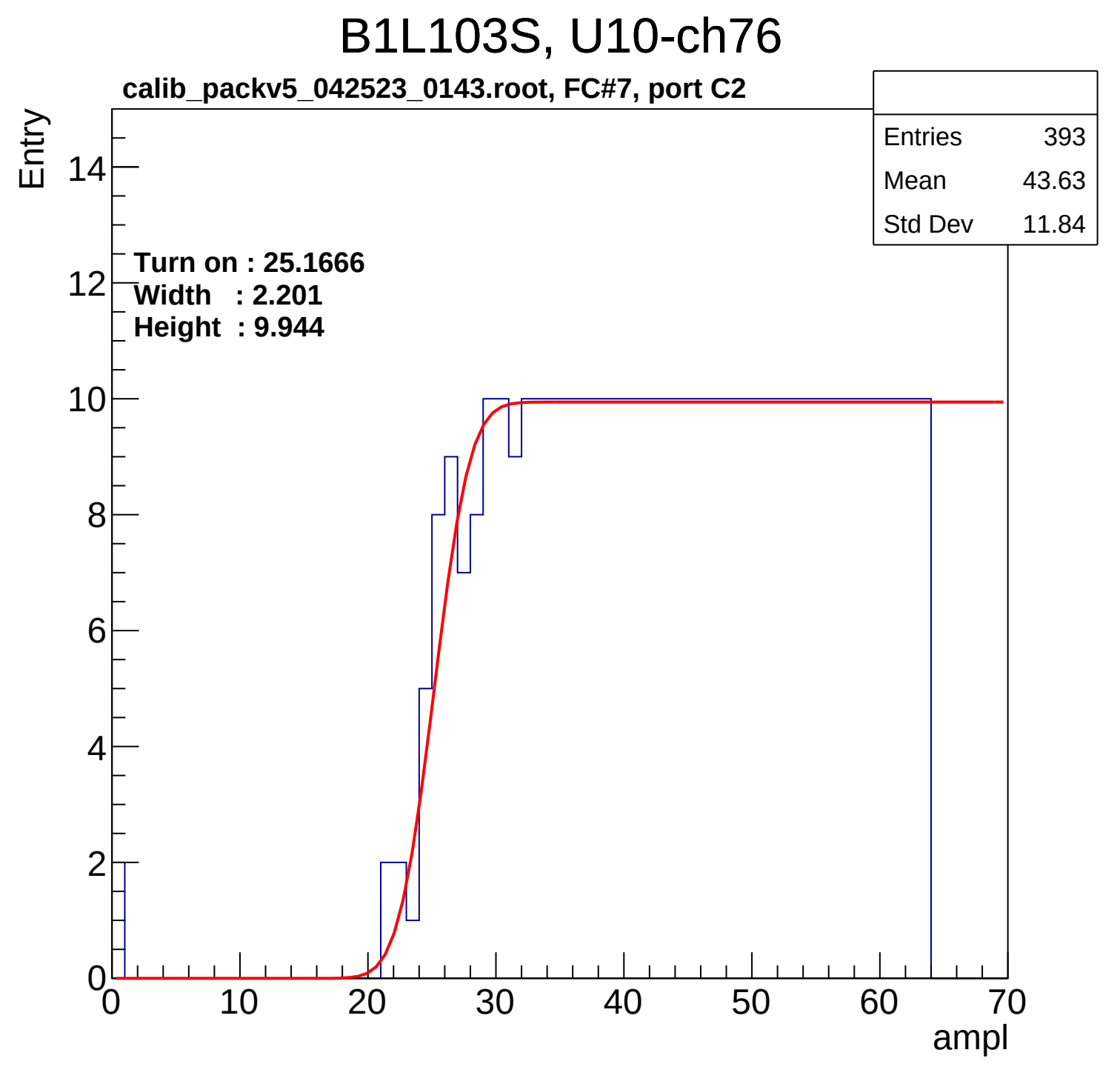
B1L103S, U10-ch76
calib_packv5_042523_0143.root, FC#7, port C2
Entries 393
Mean 43.63
Std Dev 11.84
Turn on : 25.1666
Width : 2.201
Height : 9.944
Entry
ampl
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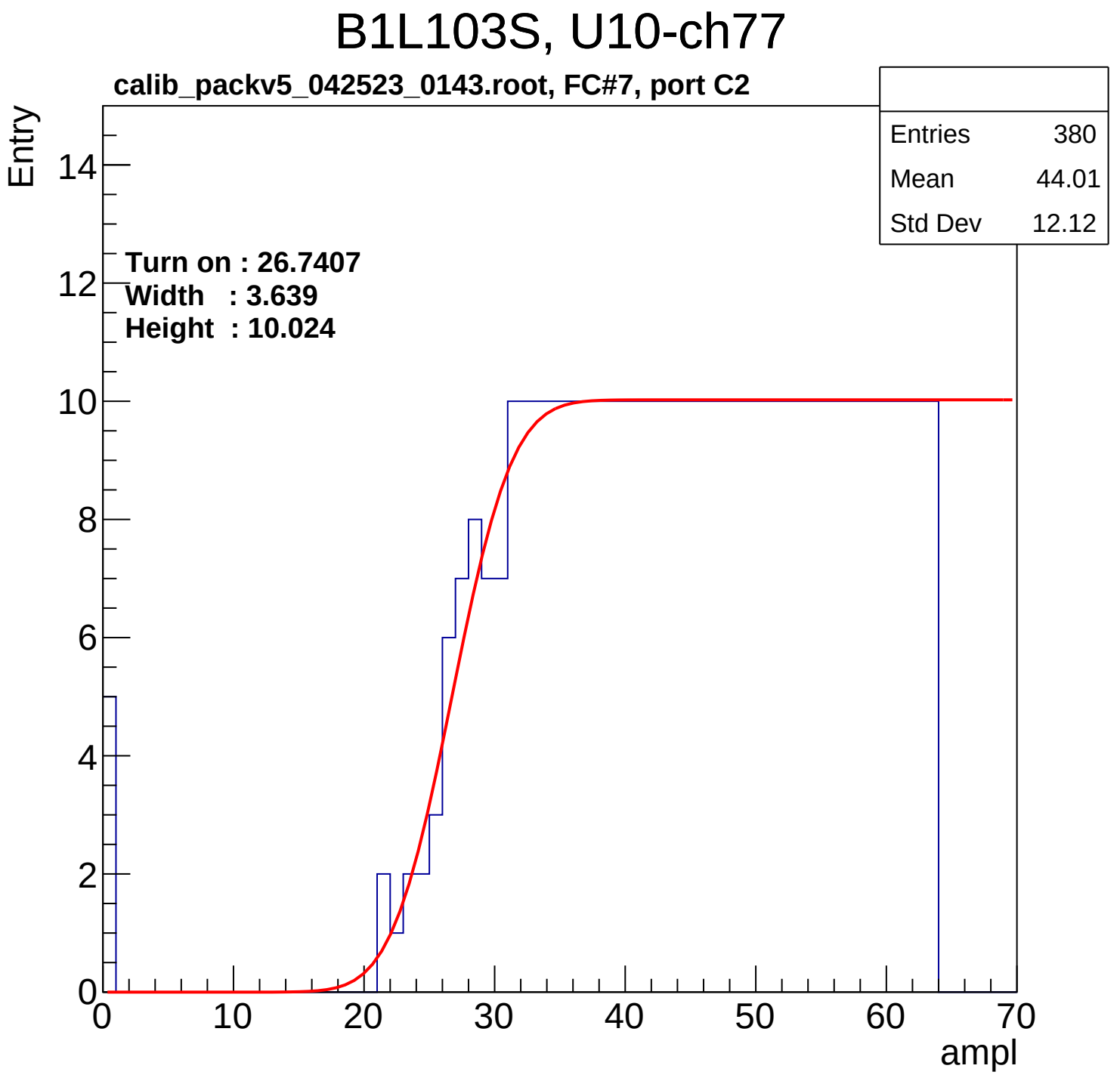
B1L103S, U10-ch77
calib_packv5_042523_0143.root, FC#7, port C2
Entries 380
Mean 44.01
Std Dev 12.12
Turn on : 26.7407
Width : 3.639
Height : 10.024
Entry
ampl
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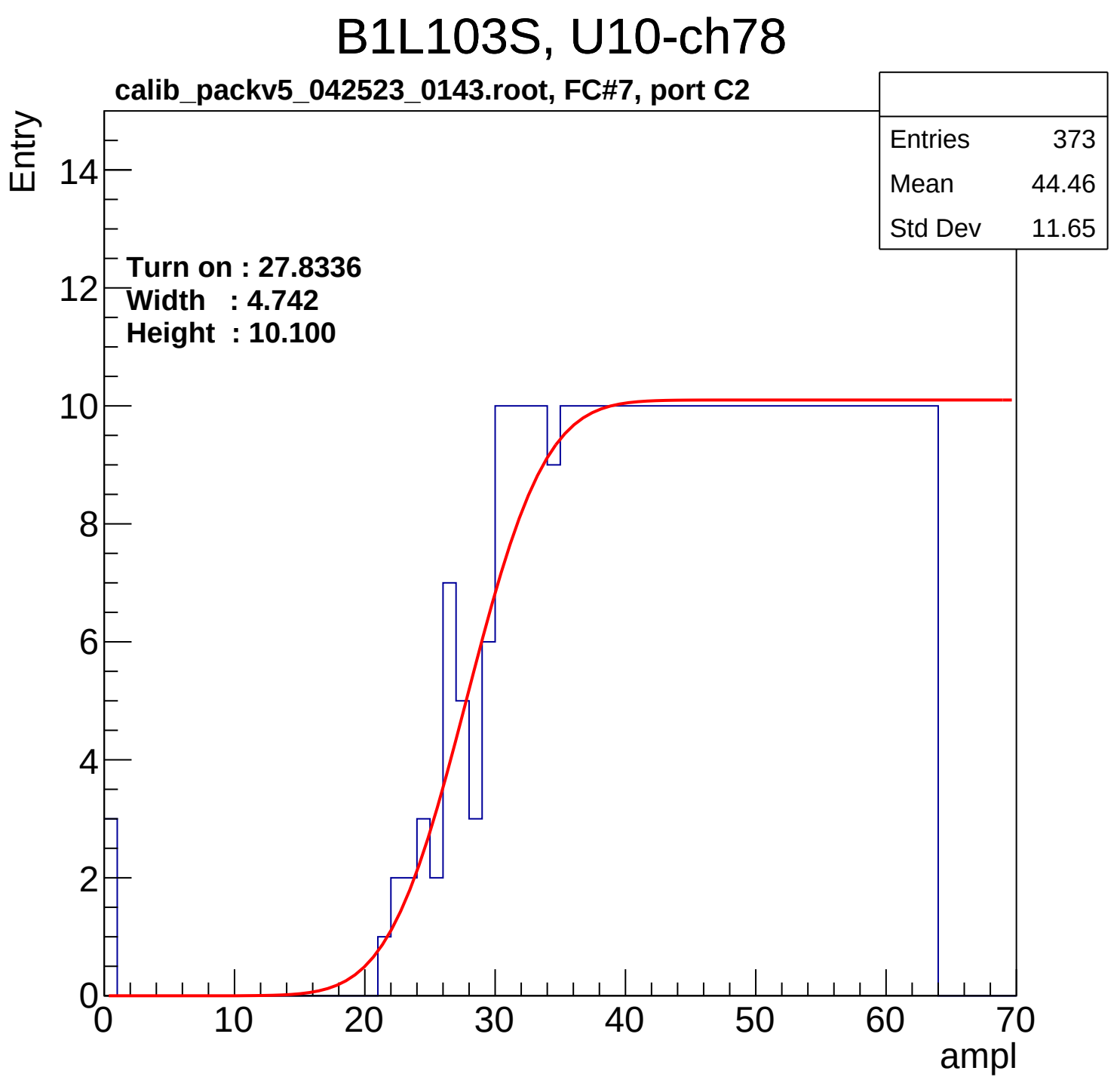
B1L103S, U10-ch78
calib_packv5_042523_0143.root, FC#7, port C2
Entries 373
Mean 44.46
Std Dev 11.65
Turn on : 27.8336
Width : 4.742
Height : 10.100
Entry
ampl
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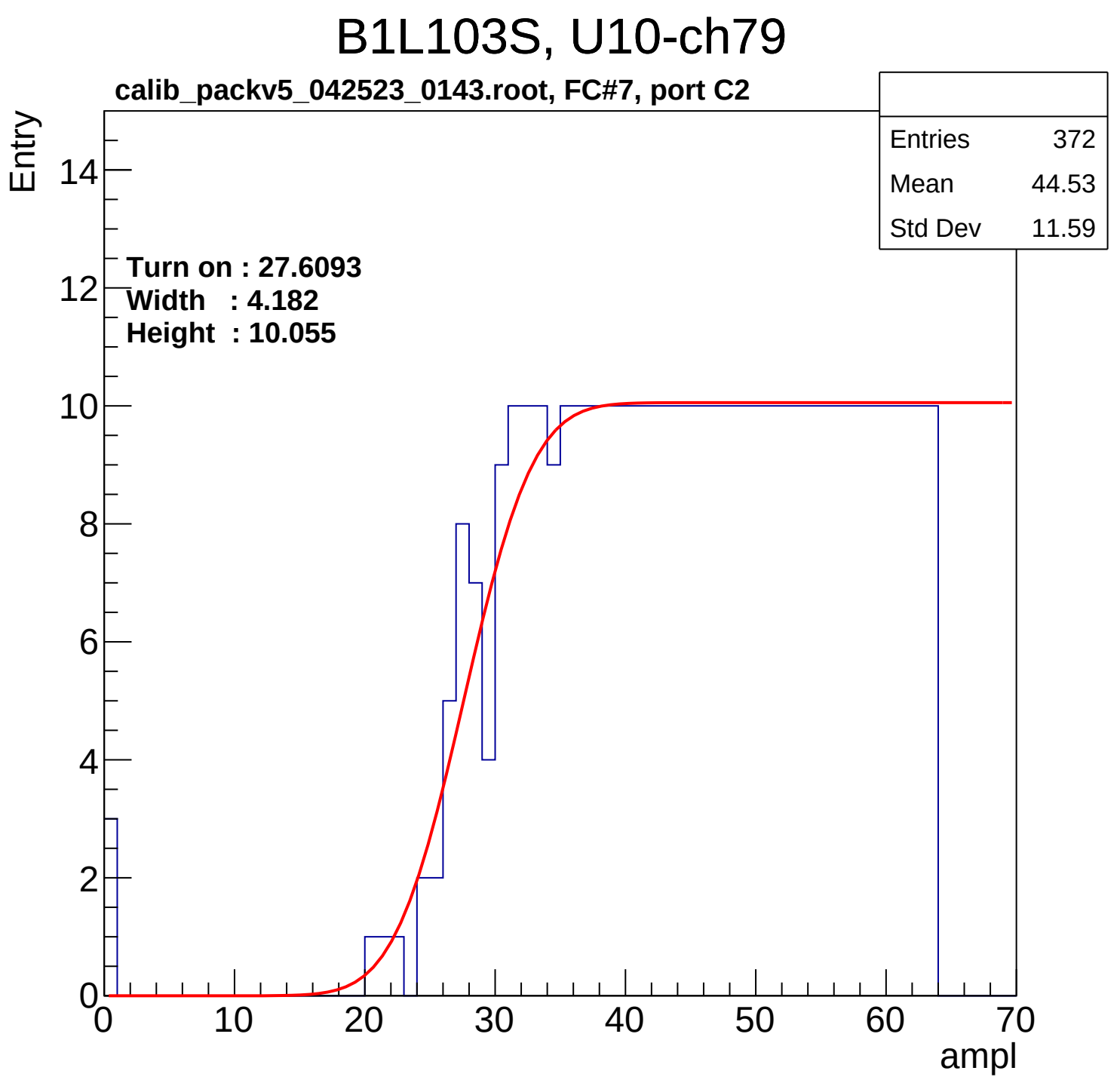
B1L103S, U10-ch79
calib_packv5_042523_0143.root, FC#7, port C2
Entries 372
Mean 44.53
Std Dev 11.59
Turn on : 27.6093
Width : 4.182
Height : 10.055
Entry
ampl
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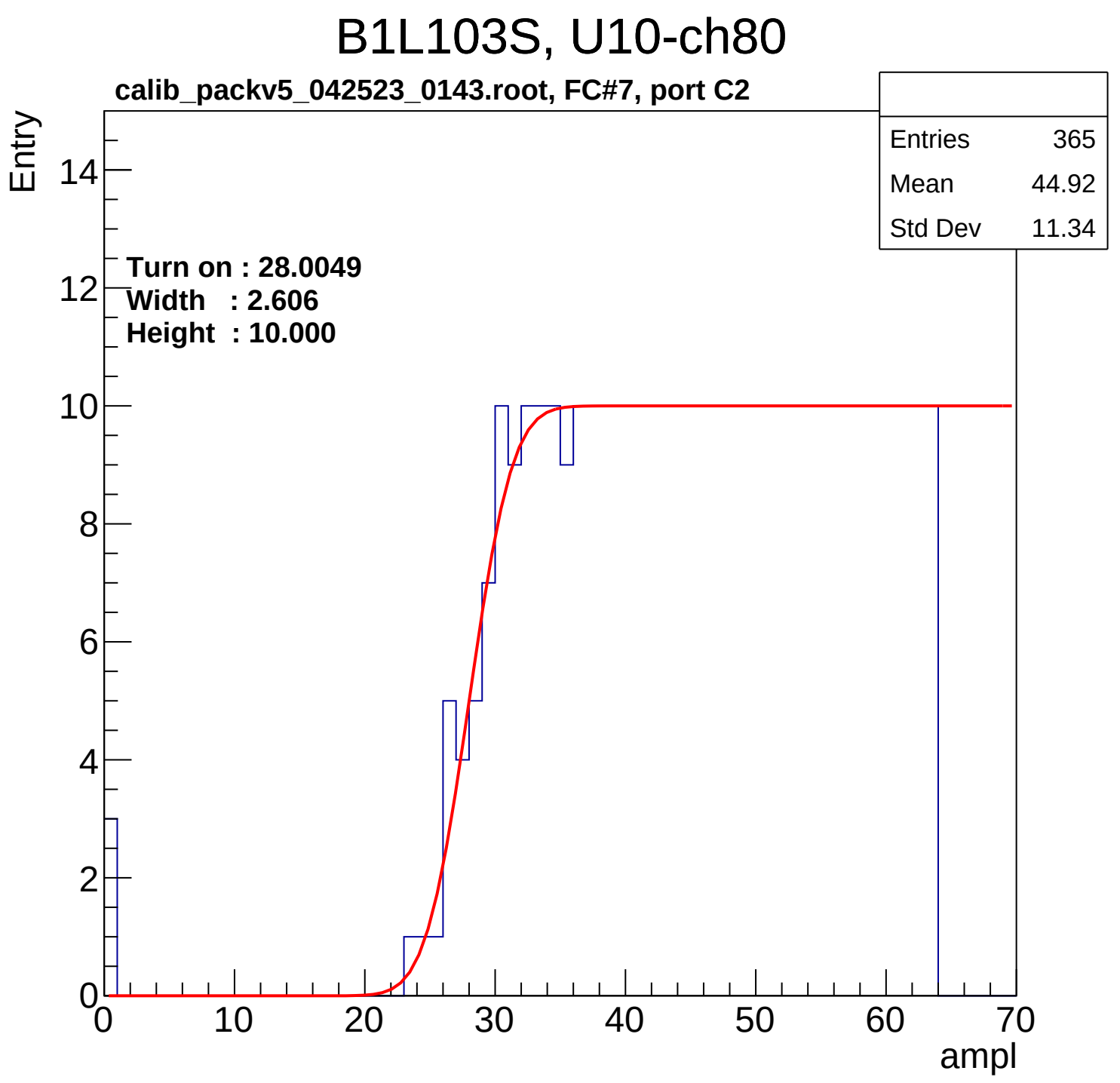
B1L103S, U10-ch80
calib_packv5_042523_0143.root, FC#7, port C2
Entries 365
Mean 44.92
Std Dev 11.34
Turn on : 28.0049
Width : 2.606
Height : 10.000
Entry
ampl
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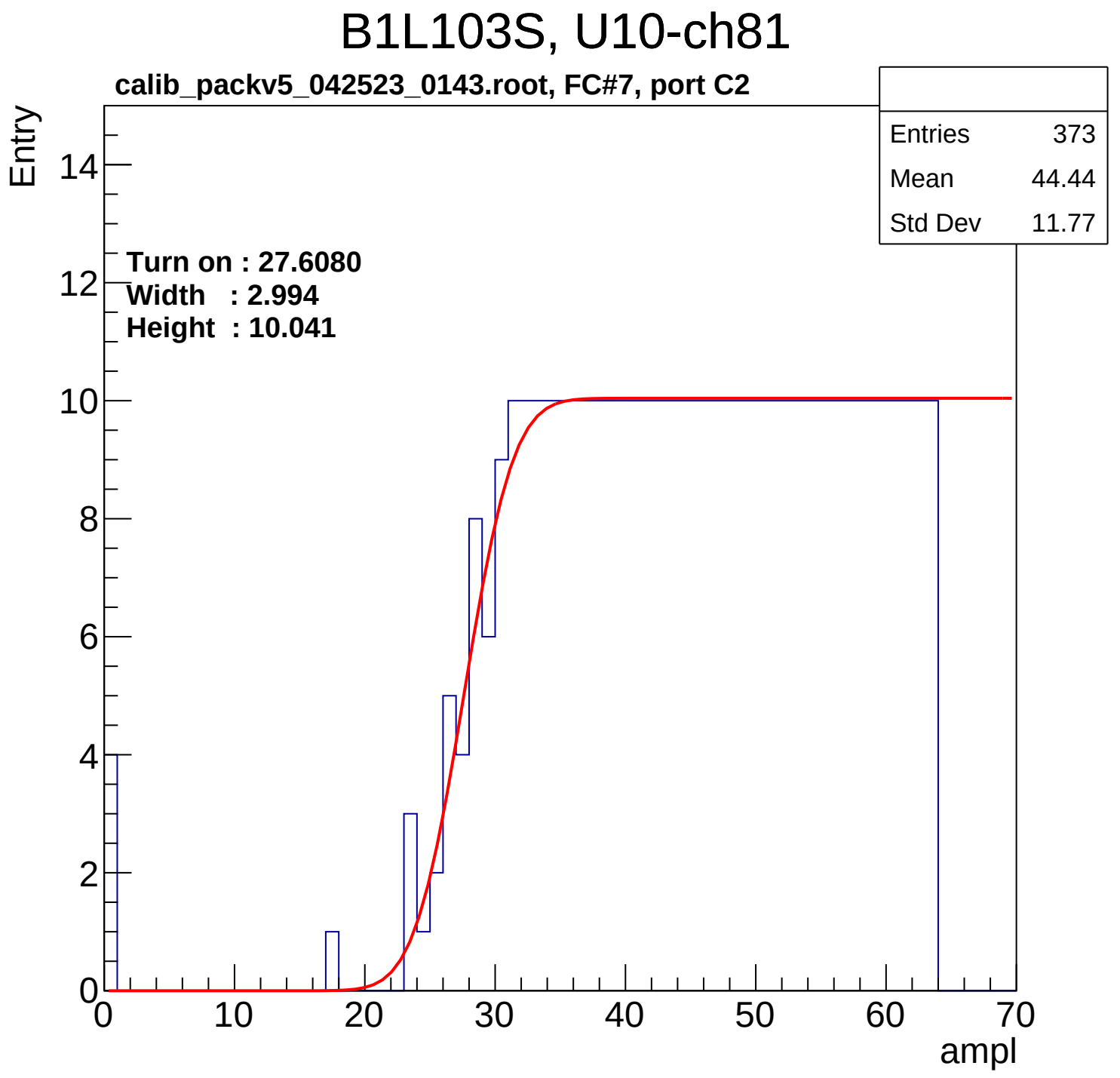
B1L103S, U10-ch81
calib_packv5_042523_0143.root, FC#7, port C2
Entries 373
Mean 44.44
Std Dev 11.77
Turn on : 27.6080
Width : 2.994
Height : 10.041
Entry
ampl
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4
6
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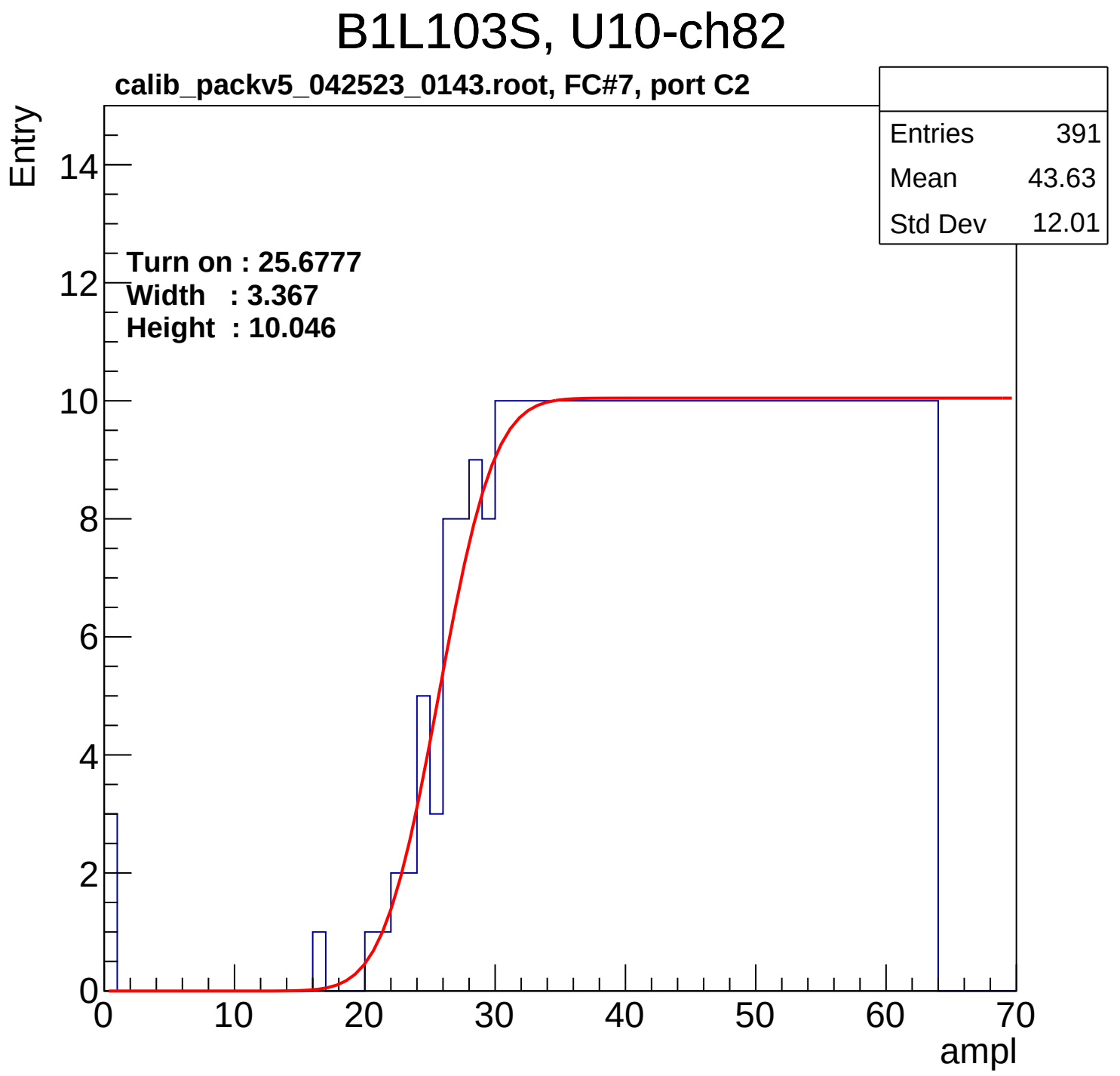
B1L103S, U10-ch82
calib_packv5_042523_0143.root, FC#7, port C2
Entries 391
Mean 43.63
Std Dev 12.01
Turn on : 25.6777
Width : 3.367
Height : 10.046
Entry
ampl
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4
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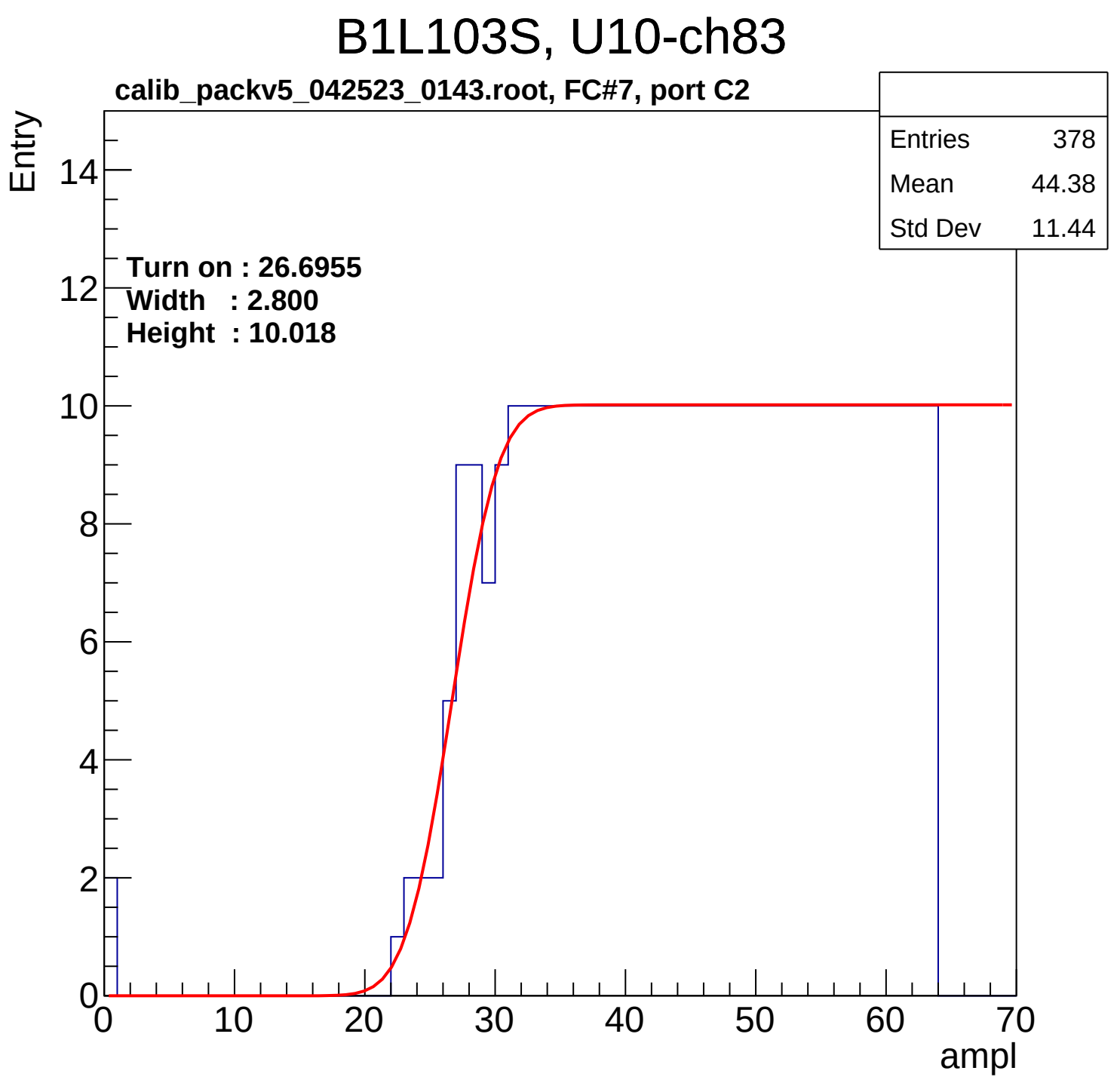
B1L103S, U10-ch83
calib_packv5_042523_0143.root, FC#7, port C2
Entries 378
Mean 44.38
Std Dev 11.44
Turn on : 26.6955
Width : 2.800
Height : 10.018
Entry
ampl
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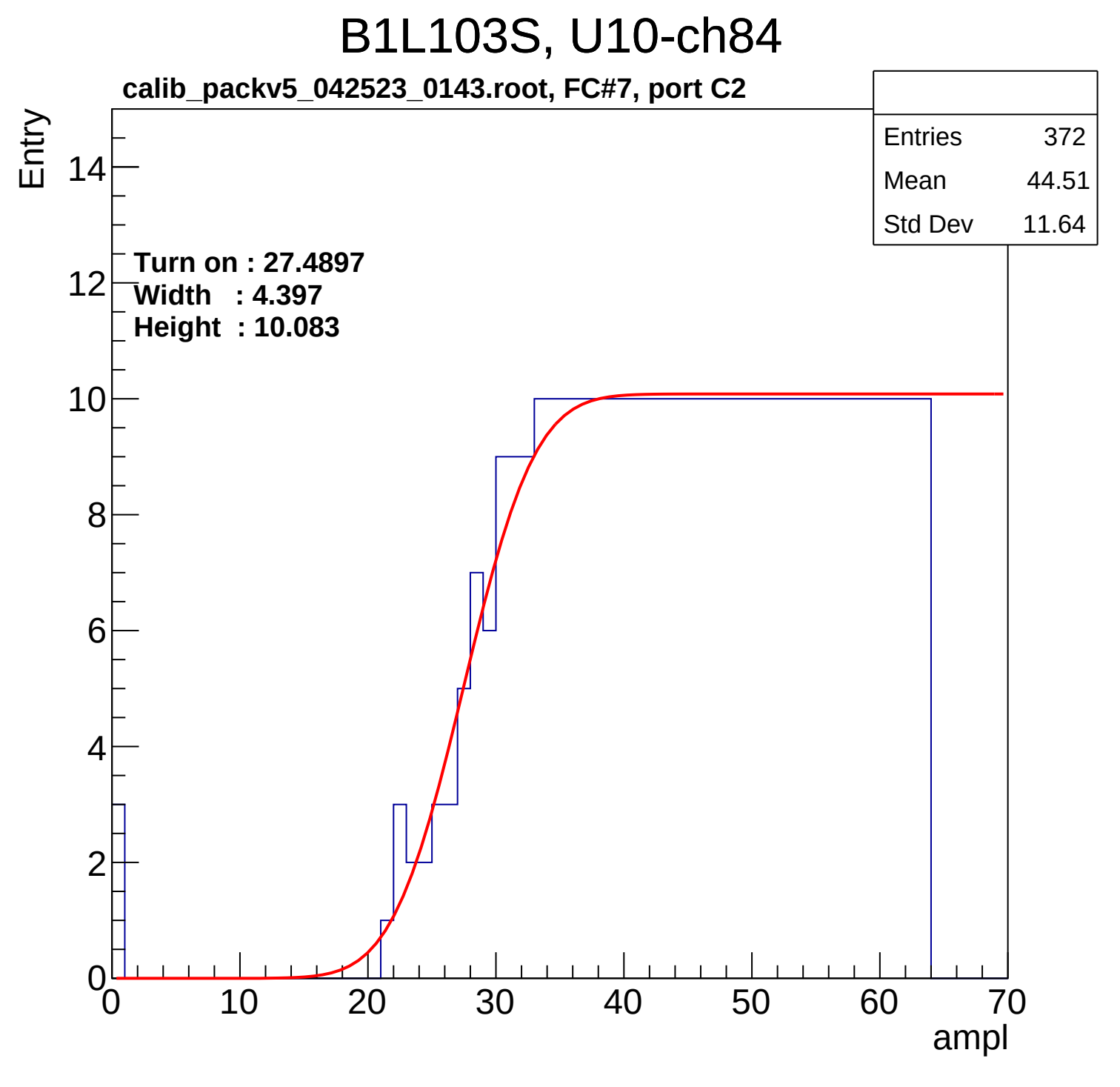
B1L103S, U10-ch84
calib_packv5_042523_0143.root, FC#7, port C2
Entries 372
Mean 44.51
Std Dev 11.64
Turn on : 27.4897
Width : 4.397
Height : 10.083
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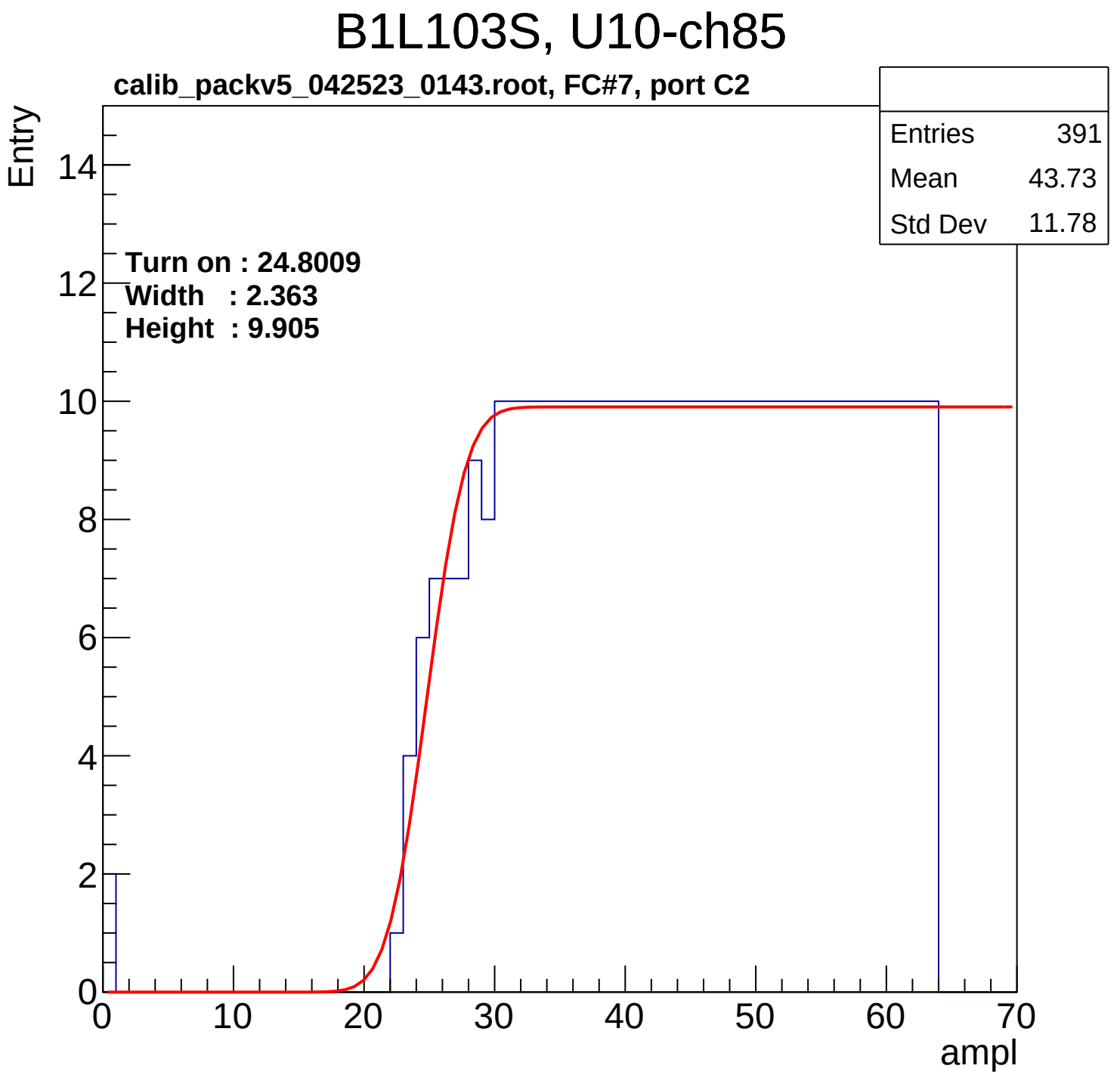
B1L103S, U10-ch85
calib_packv5_042523_0143.root, FC#7, port C2
Entries 391
Mean 43.73
Std Dev 11.78
Turn on : 24.8009
Width : 2.363
Height : 9.905
Entry
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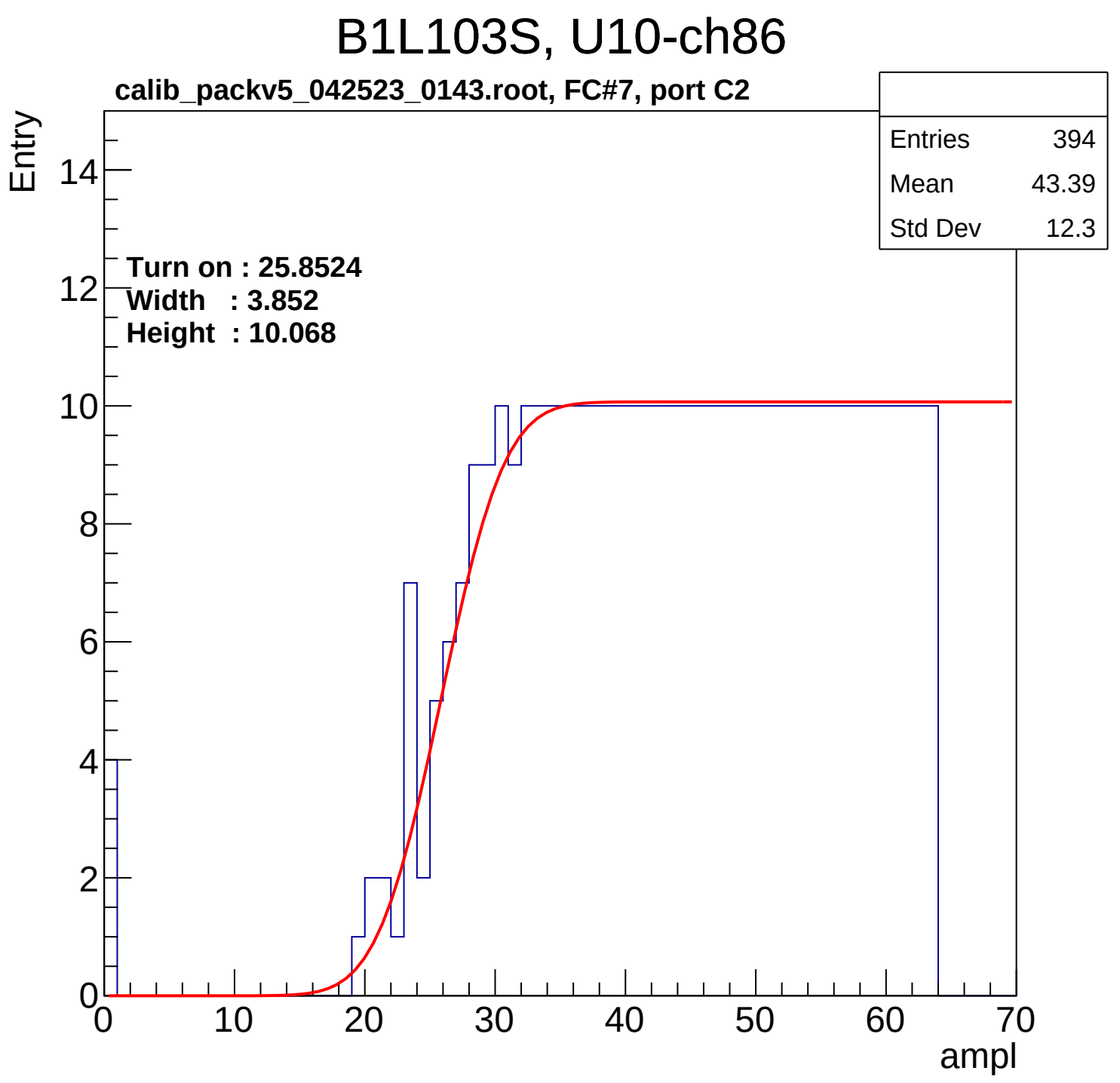
B1L103S, U10-ch86
calib_packv5_042523_0143.root, FC#7, port C2
Entries 394
Mean 43.39
Std Dev 12.3
Turn on : 25.8524
Width : 3.852
Height : 10.068
Entry
ampl
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4
6
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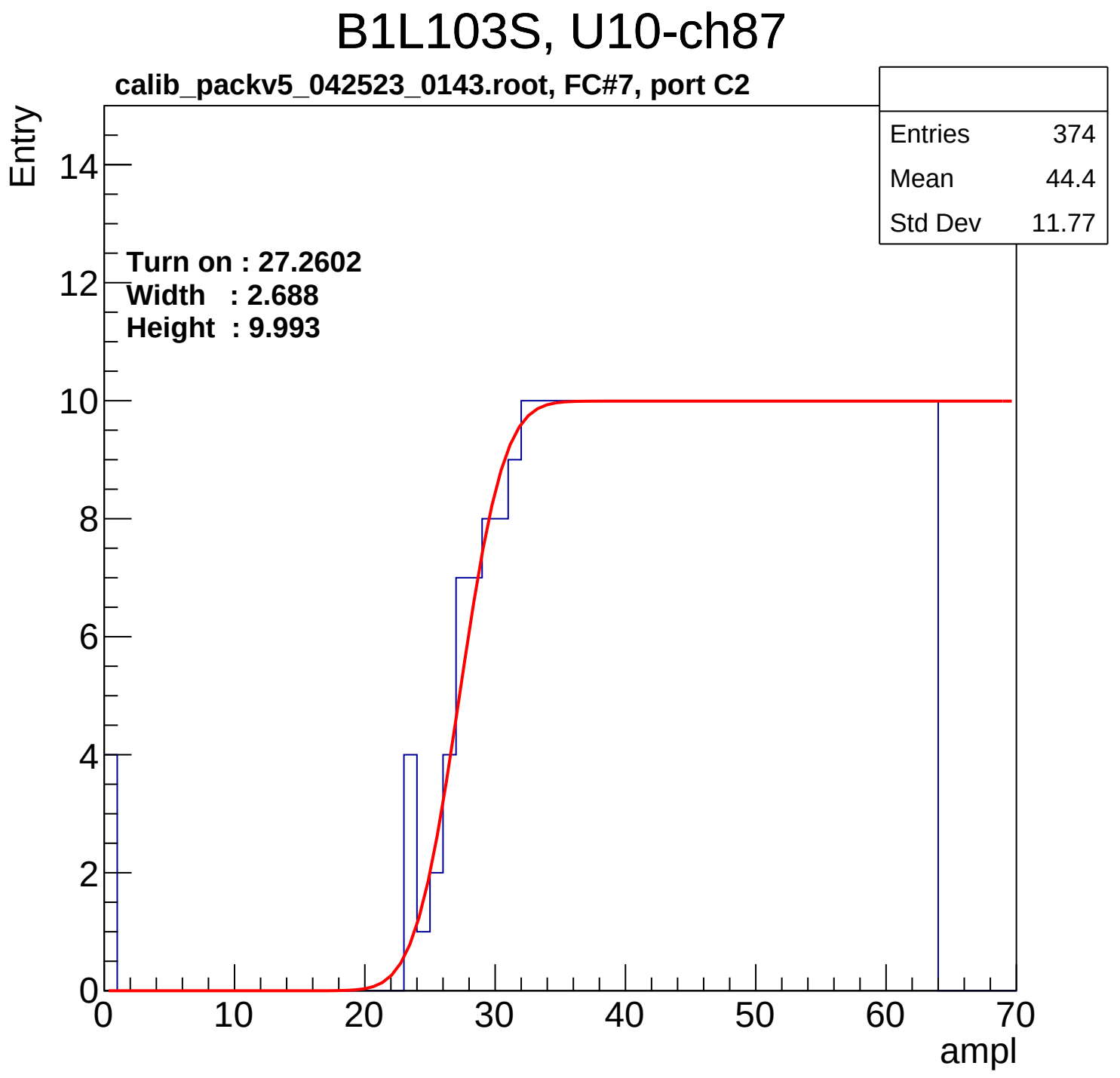
B1L103S, U10-ch87
calib_packv5_042523_0143.root, FC#7, port C2
Entries 374
Mean 44.4
Std Dev 11.77
Turn on : 27.2602
Width : 2.688
Height : 9.993
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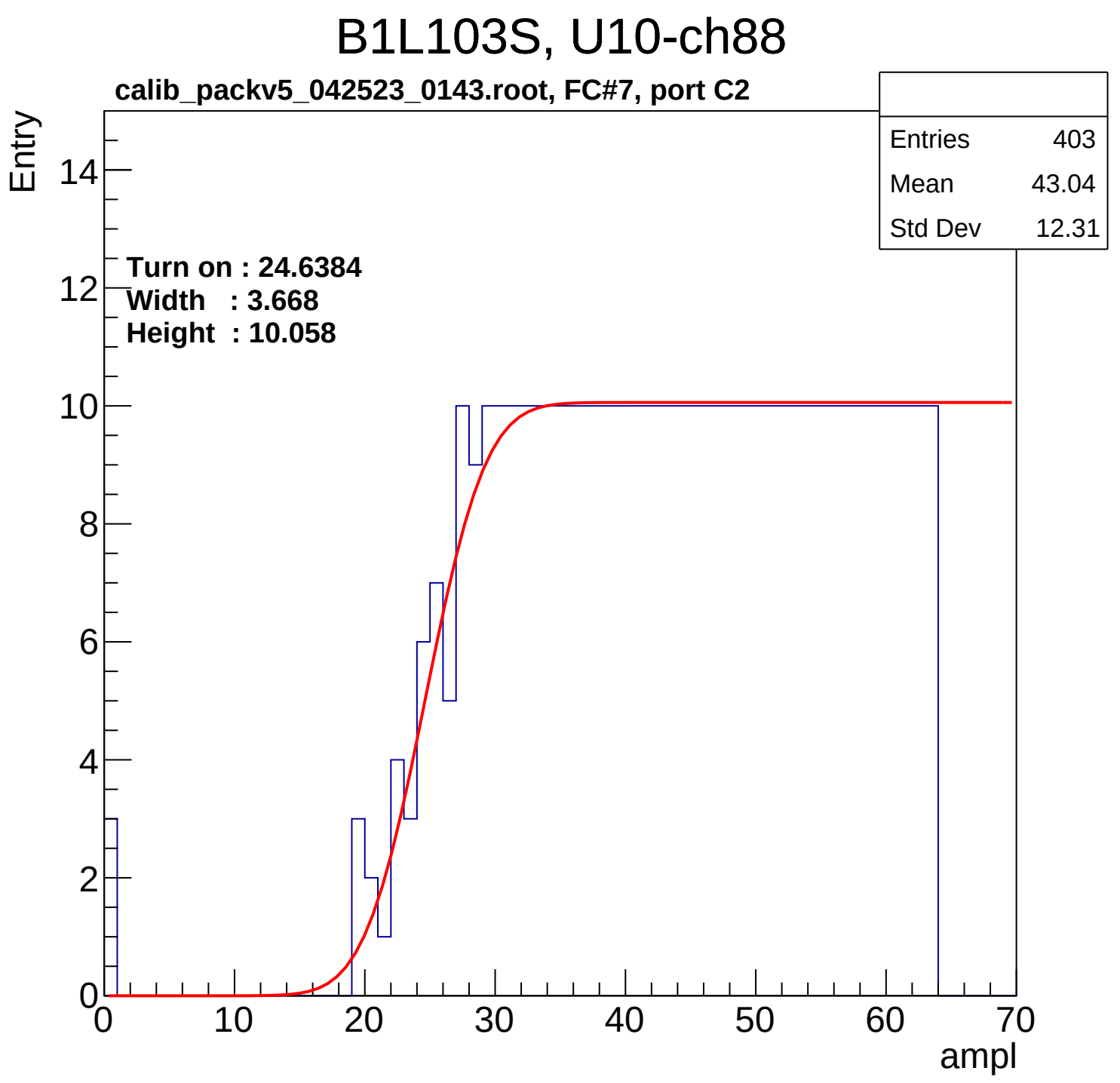
B1L103S, U10-ch88
calib_packv5_042523_0143.root, FC#7, port C2
Entries 403
Mean 43.04
Std Dev 12.31
Turn on : 24.6384
Width : 3.668
Height : 10.058
Entry
ampl
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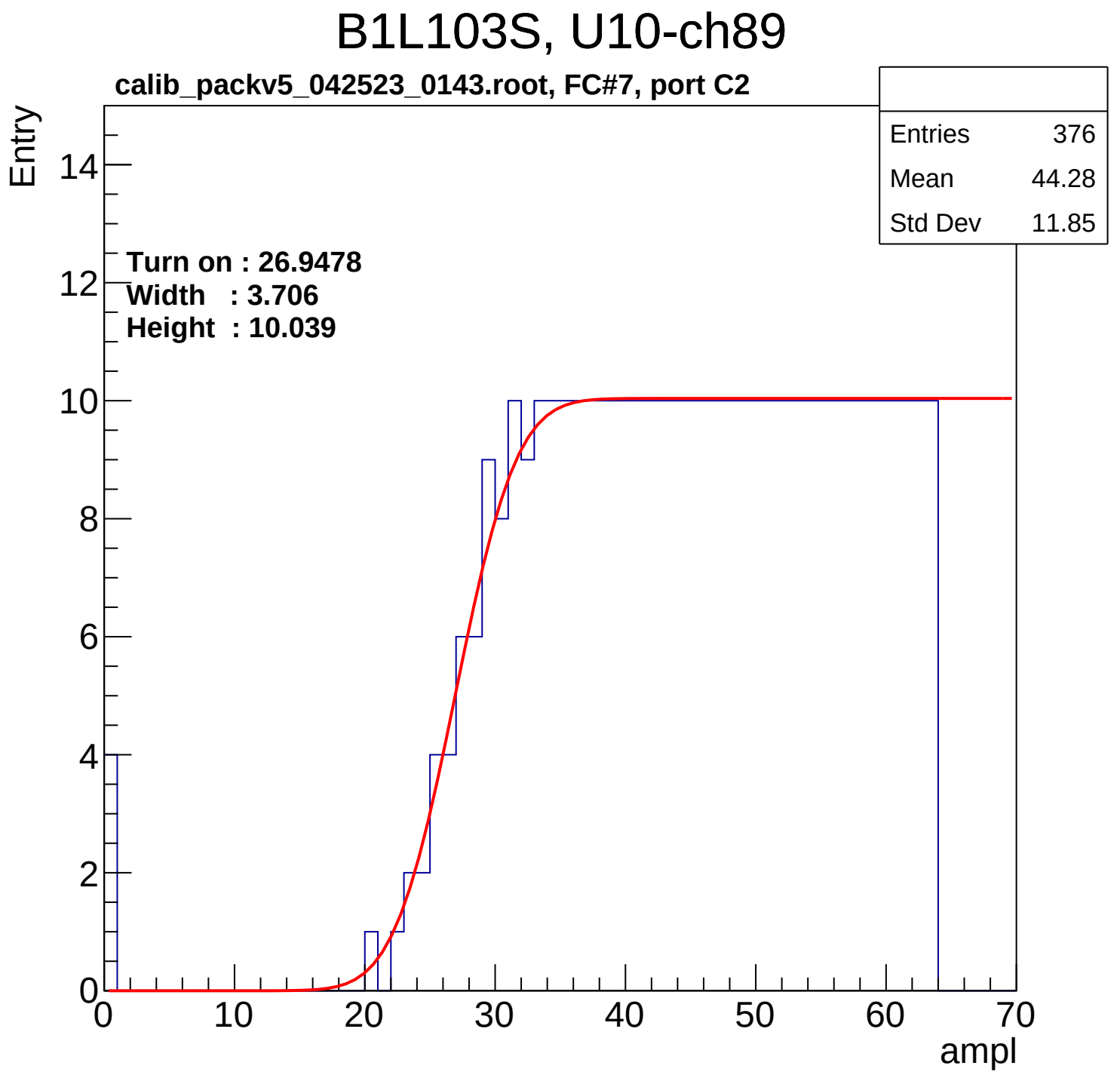
B1L103S, U10-ch89
calib_packv5_042523_0143.root, FC#7, port C2
Entries 376
Mean 44.28
Std Dev 11.85
Turn on : 26.9478
Width : 3.706
Height : 10.039
Entry
ampl
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4
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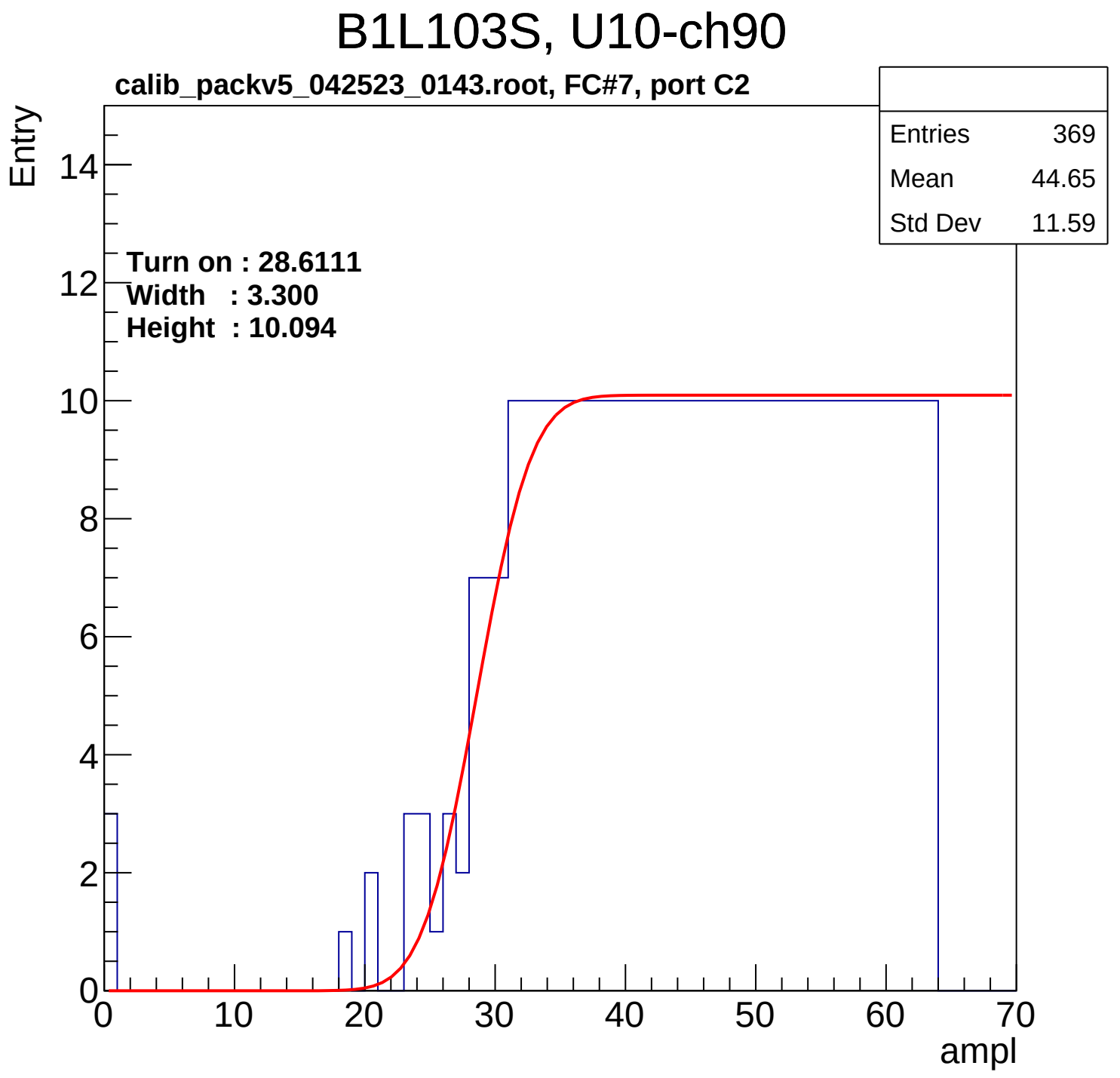
B1L103S, U10-ch90
calib_packv5_042523_0143.root, FC#7, port C2
Entries 369
Mean 44.65
Std Dev 11.59
Turn on : 28.6111
Width : 3.300
Height : 10.094
Entry
ampl
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2
4
6
8
10
12
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0
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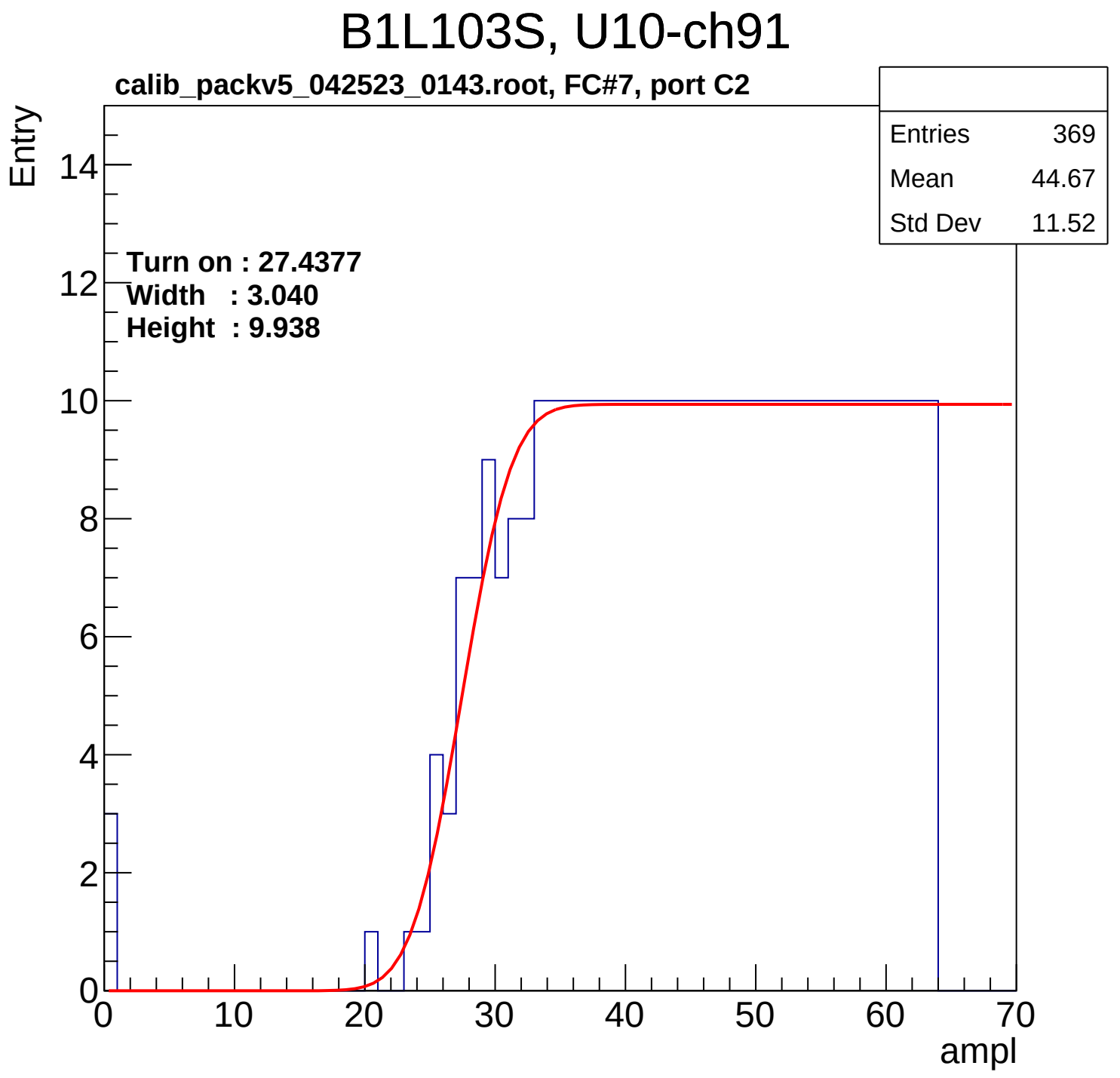
B1L103S, U10-ch91
calib_packv5_042523_0143.root, FC#7, port C2
Entries 369
Mean 44.67
Std Dev 11.52
Turn on : 27.4377
Width : 3.040
Height : 9.938
Entry
ampl
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4
6
8
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0
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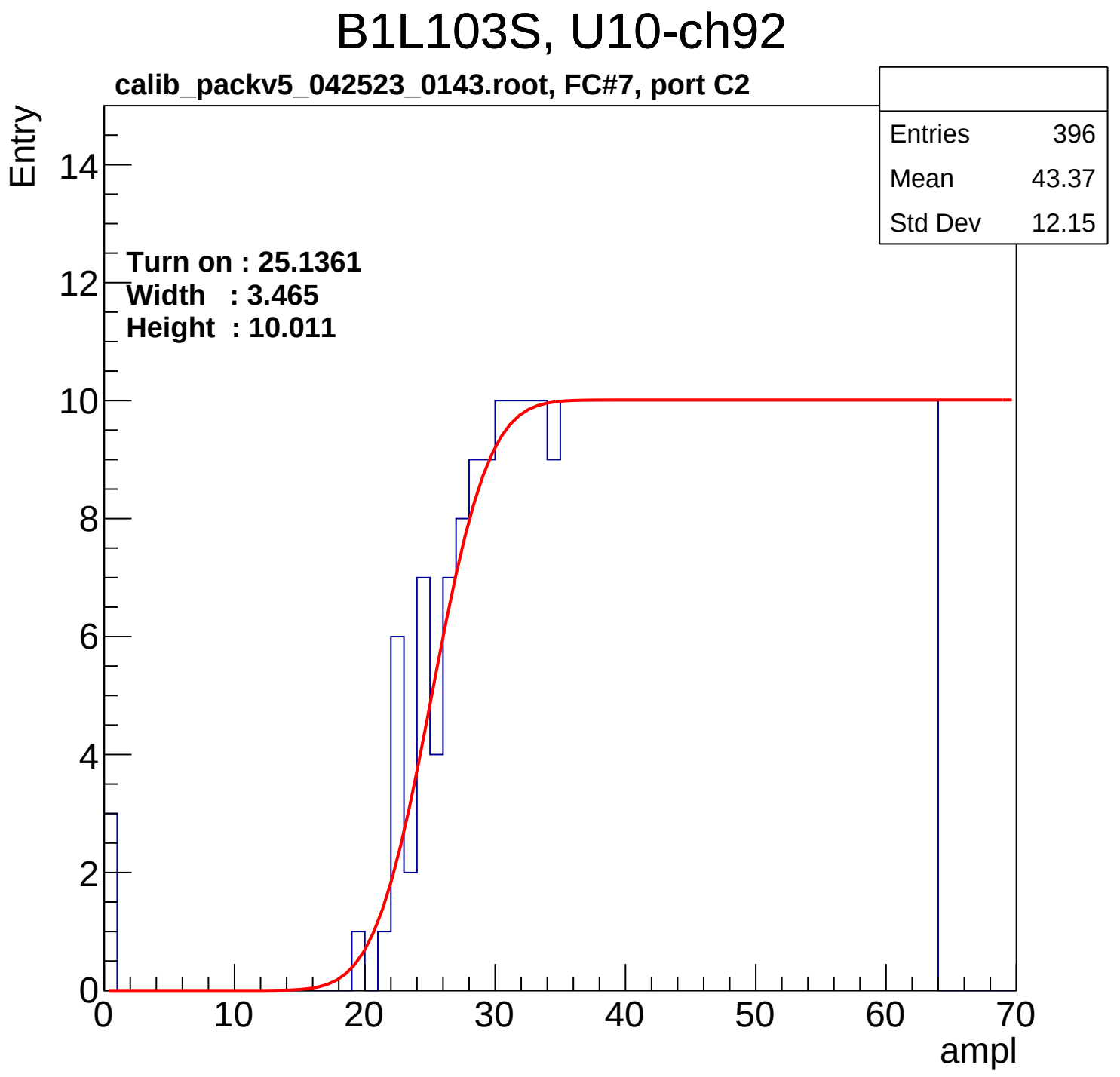
B1L103S, U10-ch92
calib_packv5_042523_0143.root, FC#7, port C2
Entries 396
Mean 43.37
Std Dev 12.15
Turn on : 25.1361
Width : 3.465
Height : 10.011
Entry
ampl
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2
4
6
8
10
12
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0
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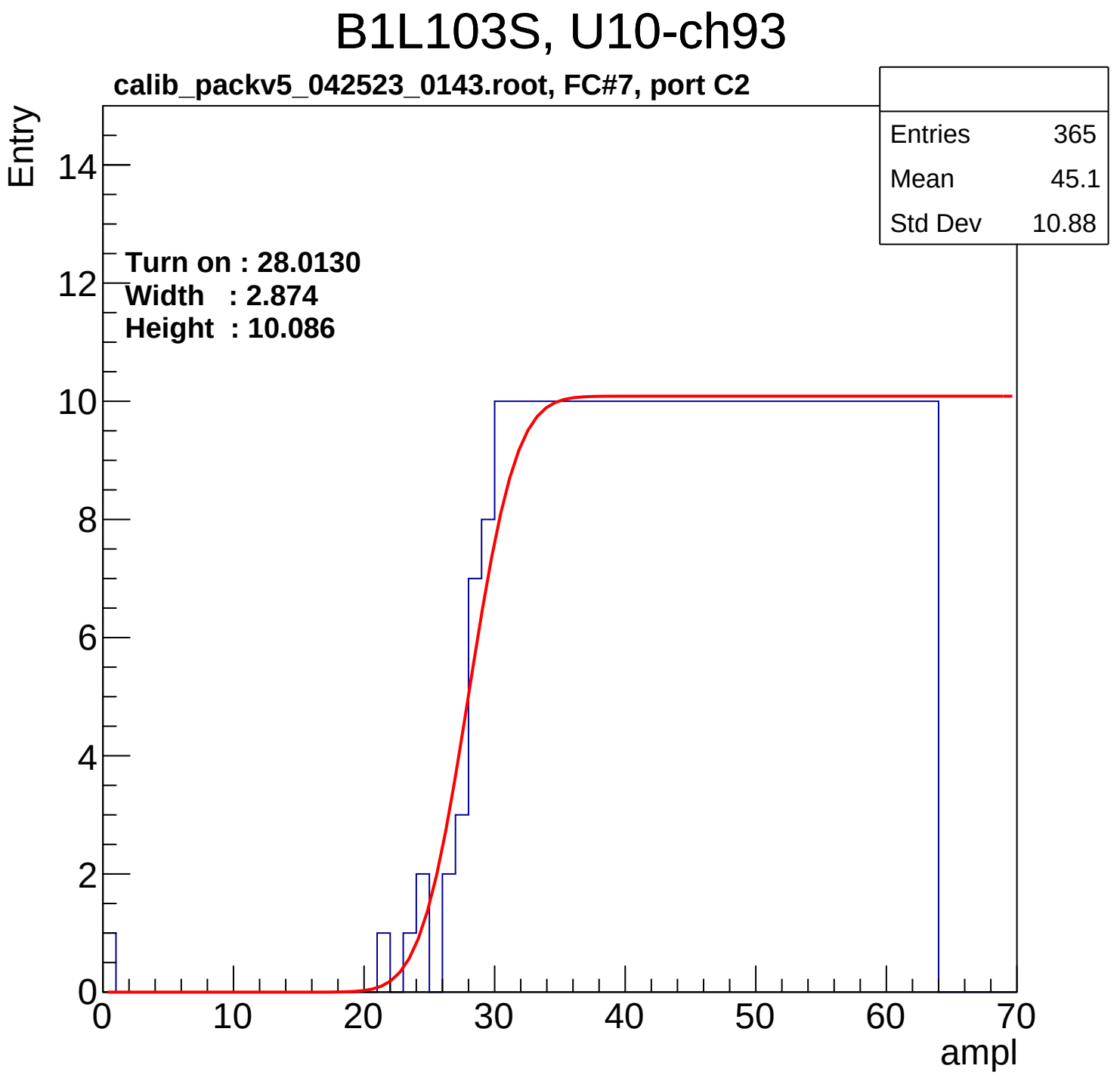
B1L103S, U10-ch93
calib_packv5_042523_0143.root, FC#7, port C2
Entries 365
Mean 45.1
Std Dev 10.88
Turn on : 28.0130
Width : 2.874
Height : 10.086
Entry
ampl
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2
4
6
8
10
12
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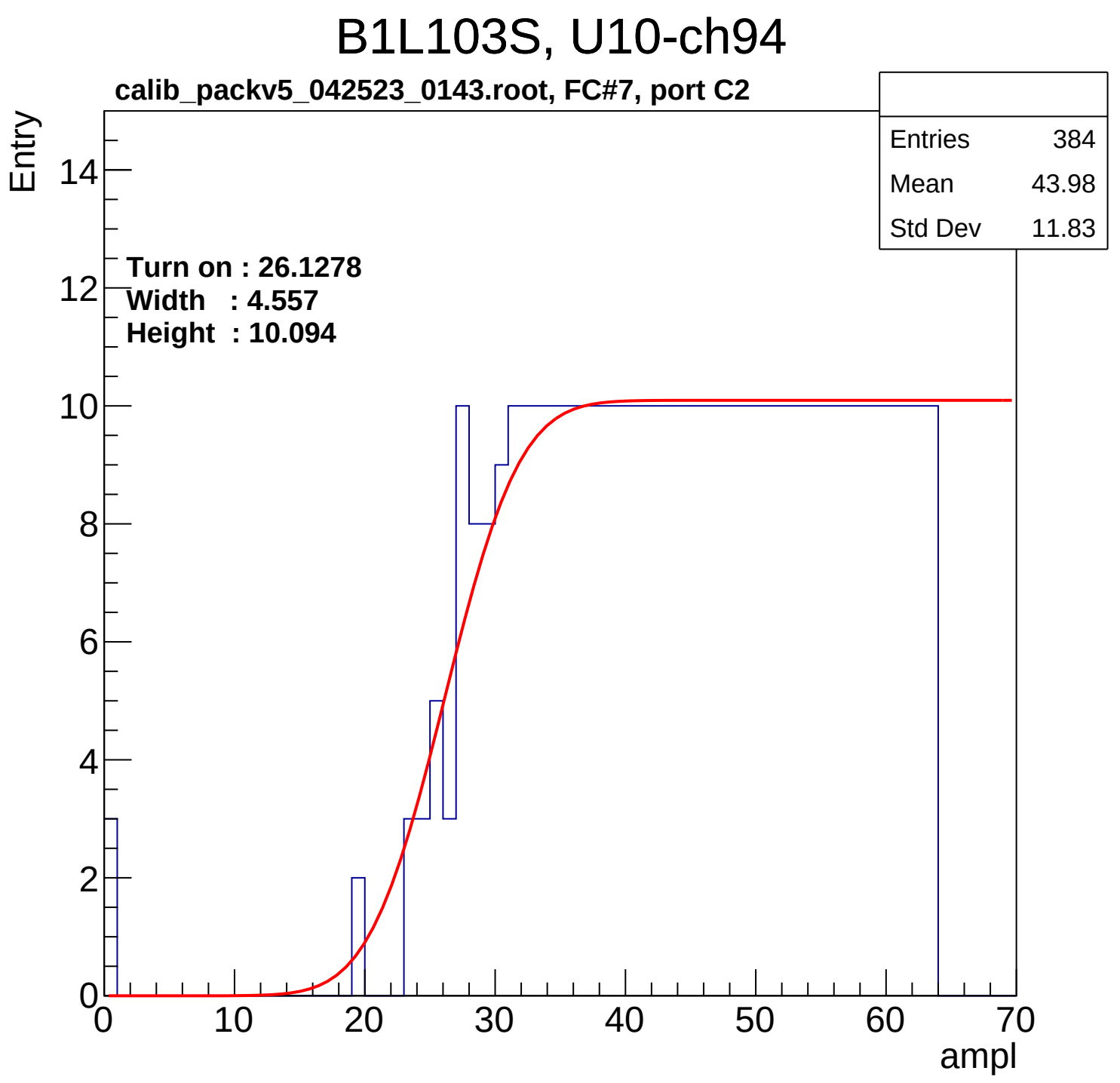
B1L103S, U10-ch94
calib_packv5_042523_0143.root, FC#7, port C2
Entries 384
Mean 43.98
Std Dev 11.83
Turn on : 26.1278
Width : 4.557
Height : 10.094
Entry
ampl
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2
4
6
8
10
12
14
0
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20
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40
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60
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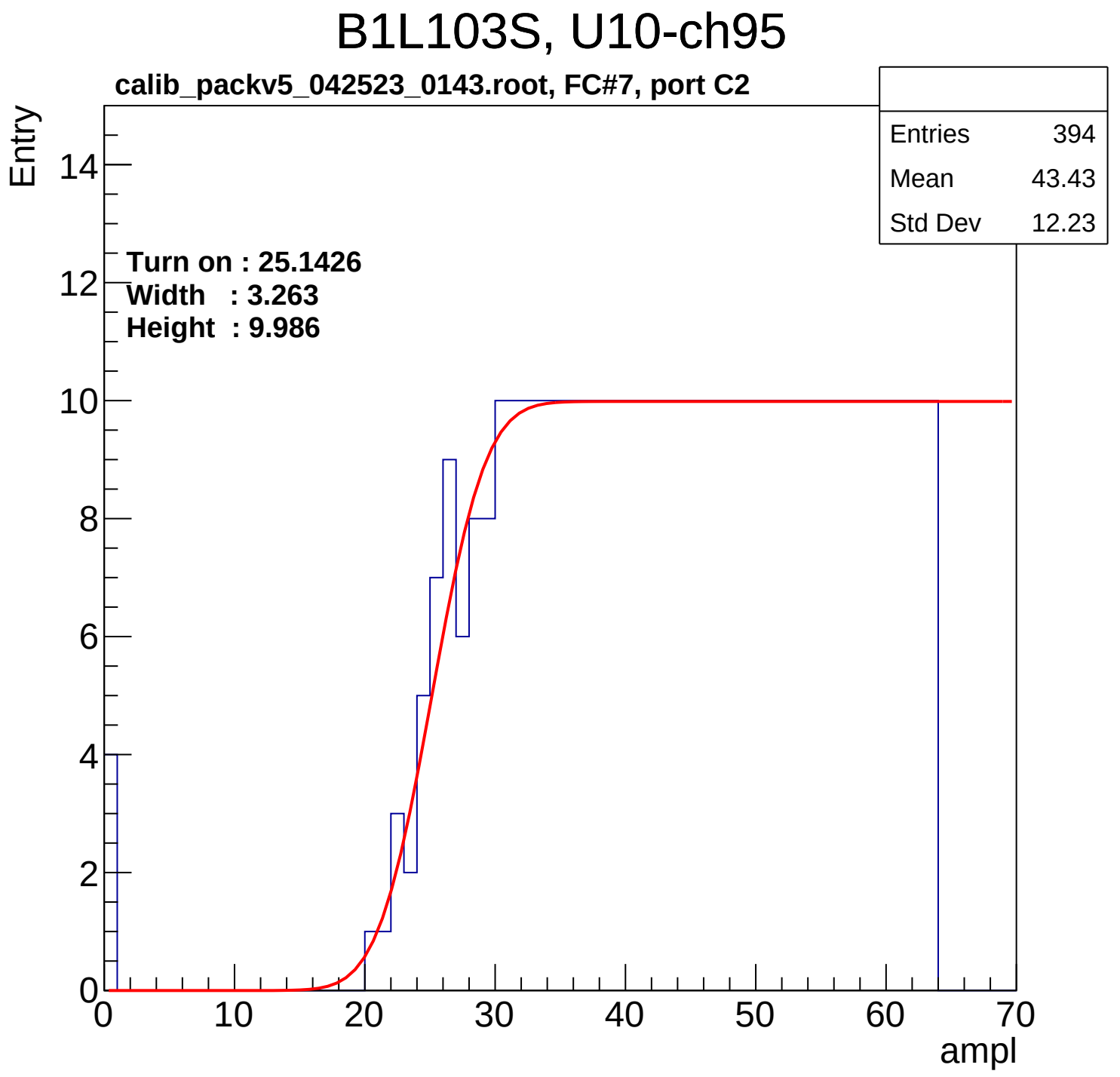
B1L103S, U10-ch95
calib_packv5_042523_0143.root, FC#7, port C2
Entries 394
Mean 43.43
Std Dev 12.23
Turn on : 25.1426
Width : 3.263
Height : 9.986
Entry
ampl
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2
4
6
8
10
12
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0
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60
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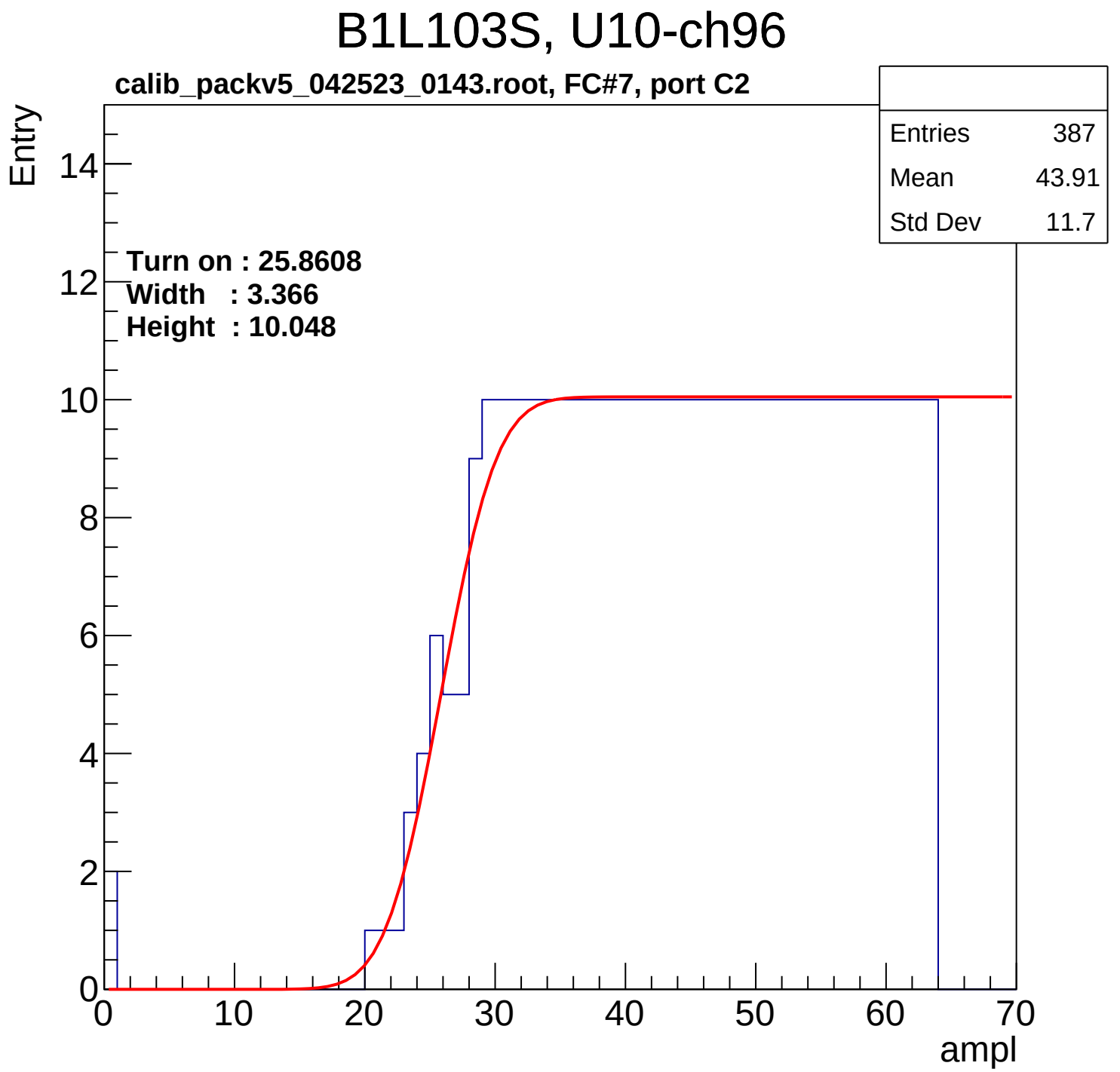
B1L103S, U10-ch96
calib_packv5_042523_0143.root, FC#7, port C2
Entries 387
Mean 43.91
Std Dev 11.7
Turn on : 25.8608
Width : 3.366
Height : 10.048
Entry
ampl
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2
4
6
8
10
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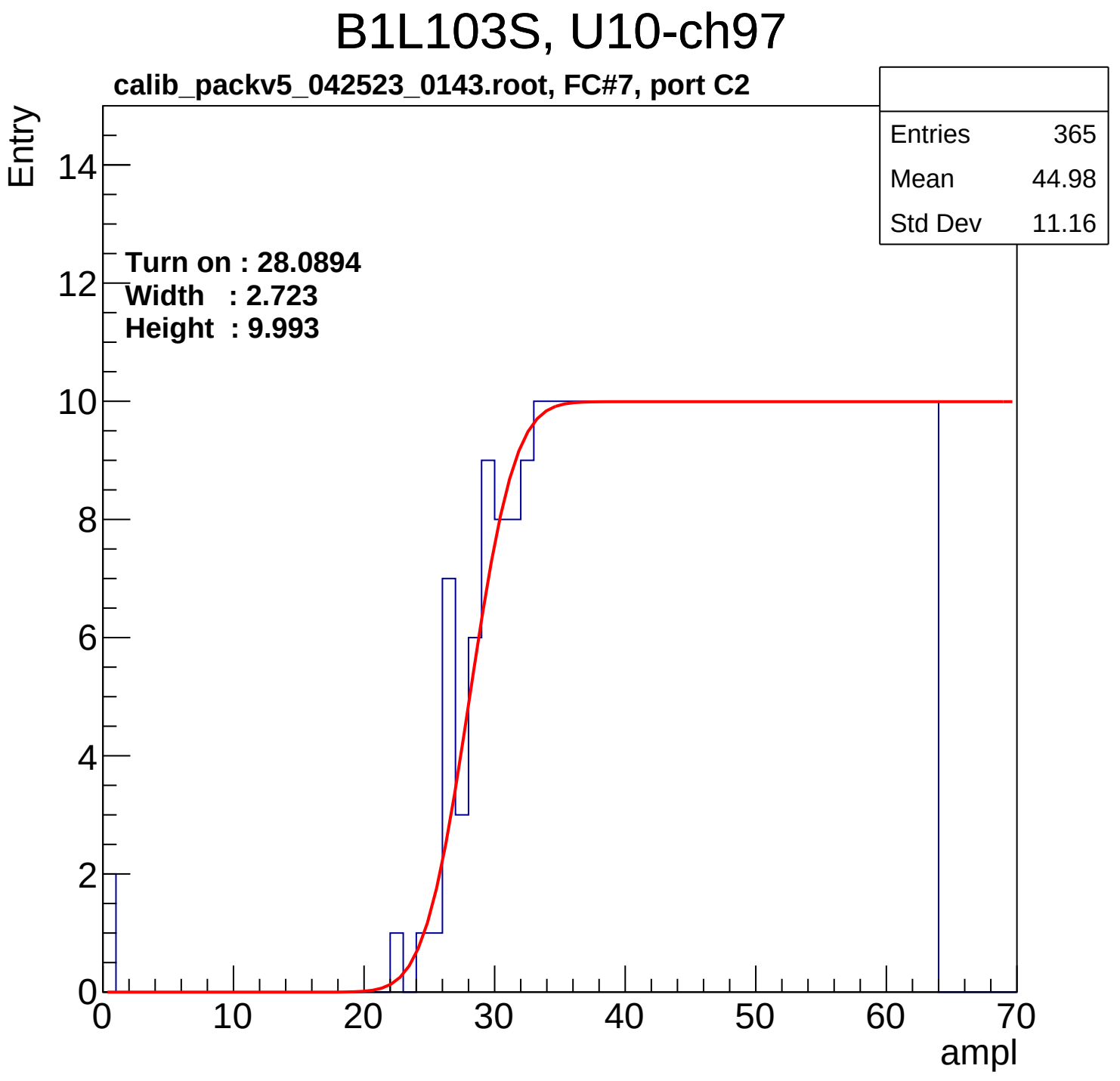
B1L103S, U10-ch97
calib_packv5_042523_0143.root, FC#7, port C2
Entries 365
Mean 44.98
Std Dev 11.16
Turn on : 28.0894
Width : 2.723
Height : 9.993
Entry
ampl
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4
6
8
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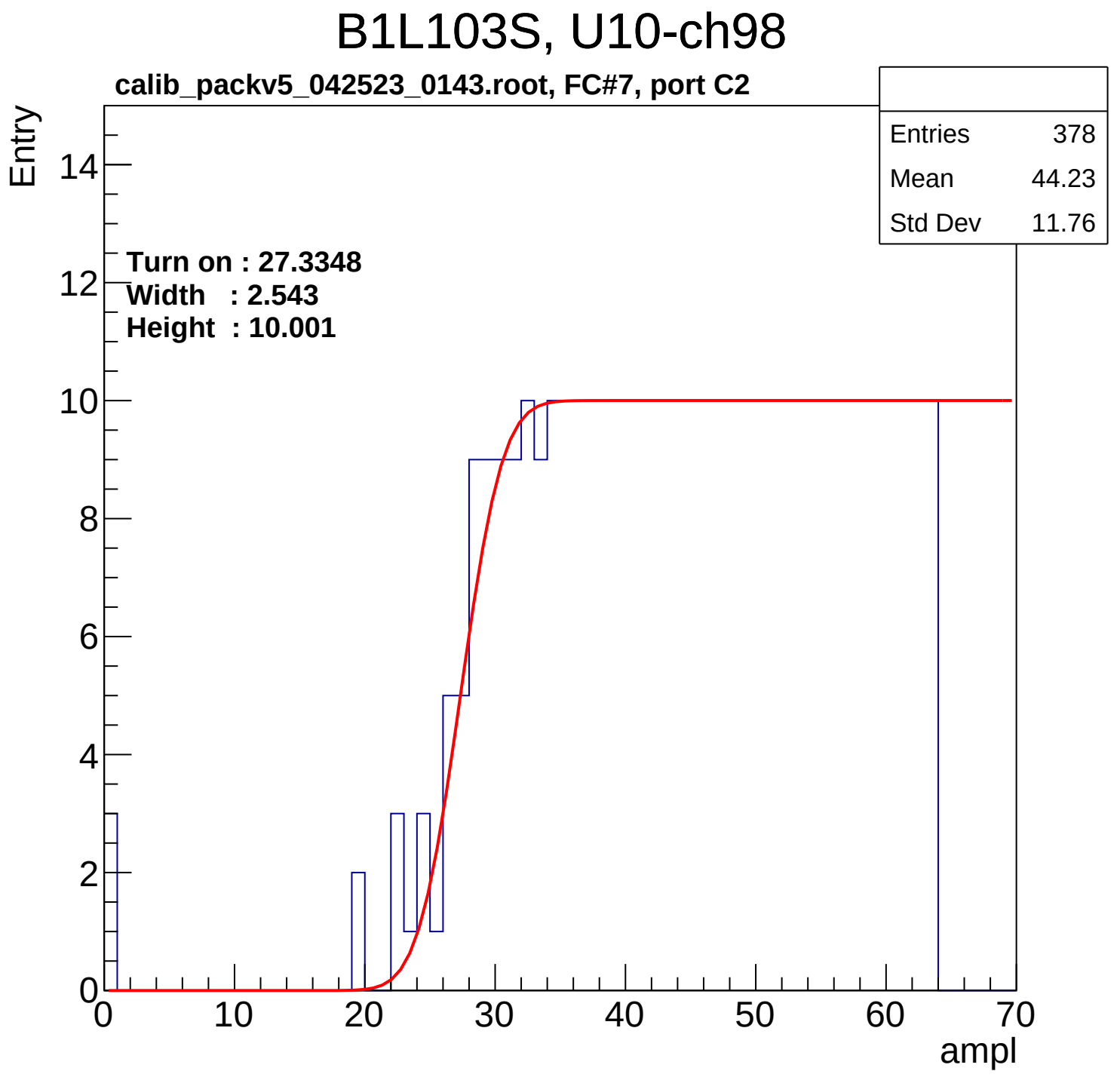
B1L103S, U10-ch98
calib_packv5_042523_0143.root, FC#7, port C2
Entries 378
Mean 44.23
Std Dev 11.76
Turn on : 27.3348
Width : 2.543
Height : 10.001
Entry
ampl
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6
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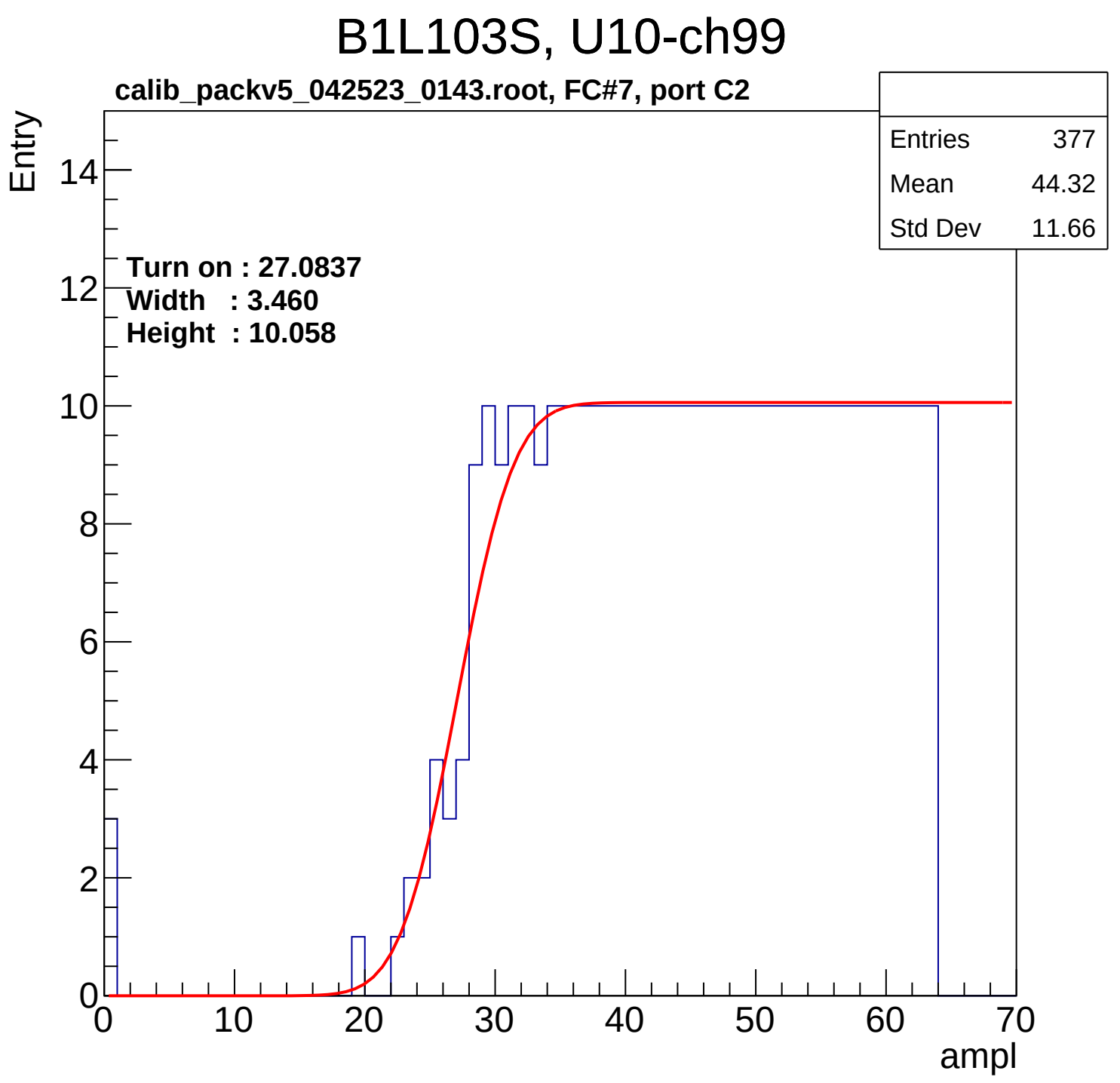
B1L103S, U10-ch99
calib_packv5_042523_0143.root, FC#7, port C2
Entries 377
Mean 44.32
Std Dev 11.66
Turn on : 27.0837
Width : 3.460
Height : 10.058
Entry
ampl
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8
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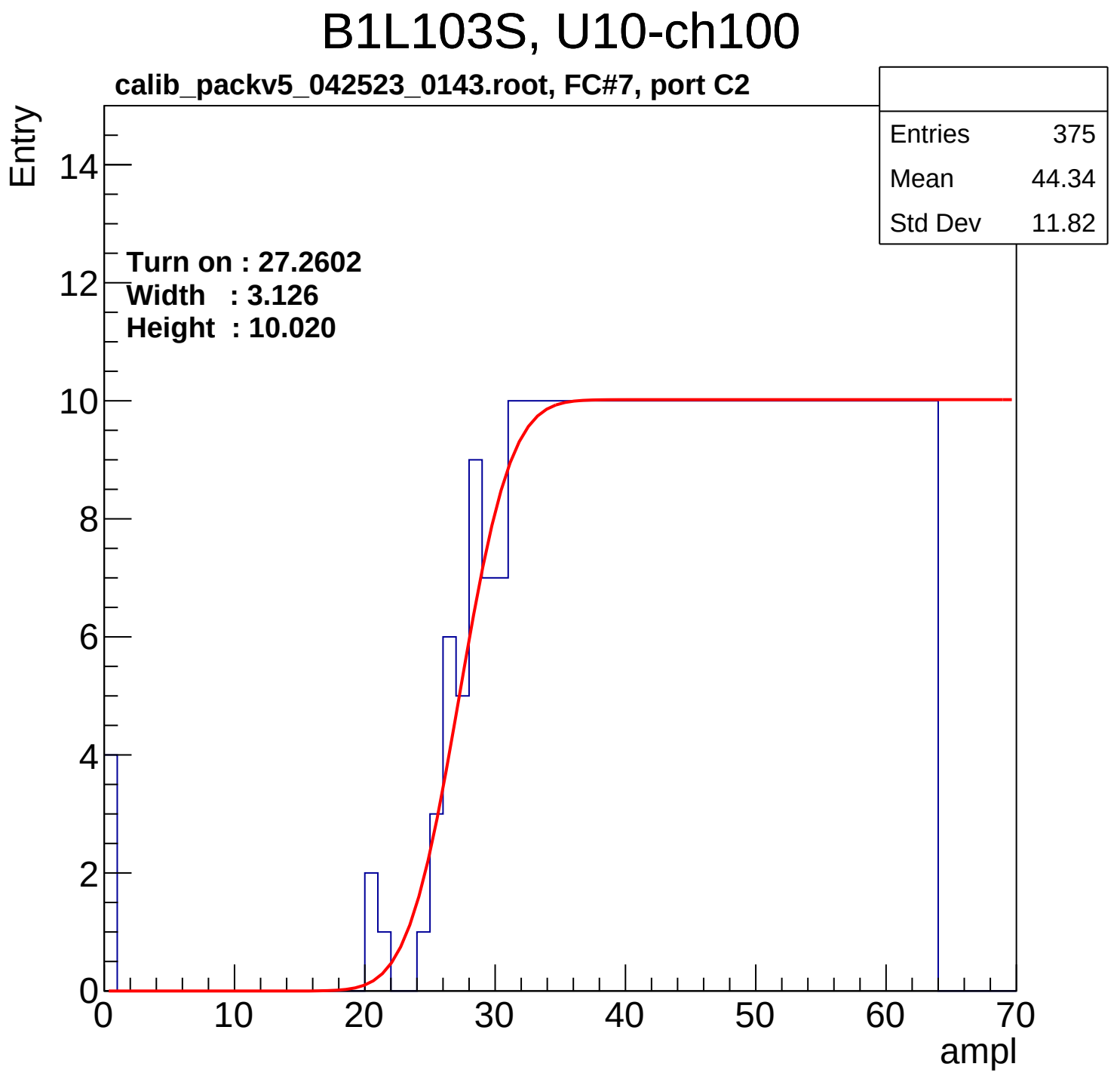
B1L103S, U10-ch100
calib_packv5_042523_0143.root, FC#7, port C2
Entries 375
Mean 44.34
Std Dev 11.82
Turn on : 27.2602
Width : 3.126
Height : 10.020
Entry
ampl
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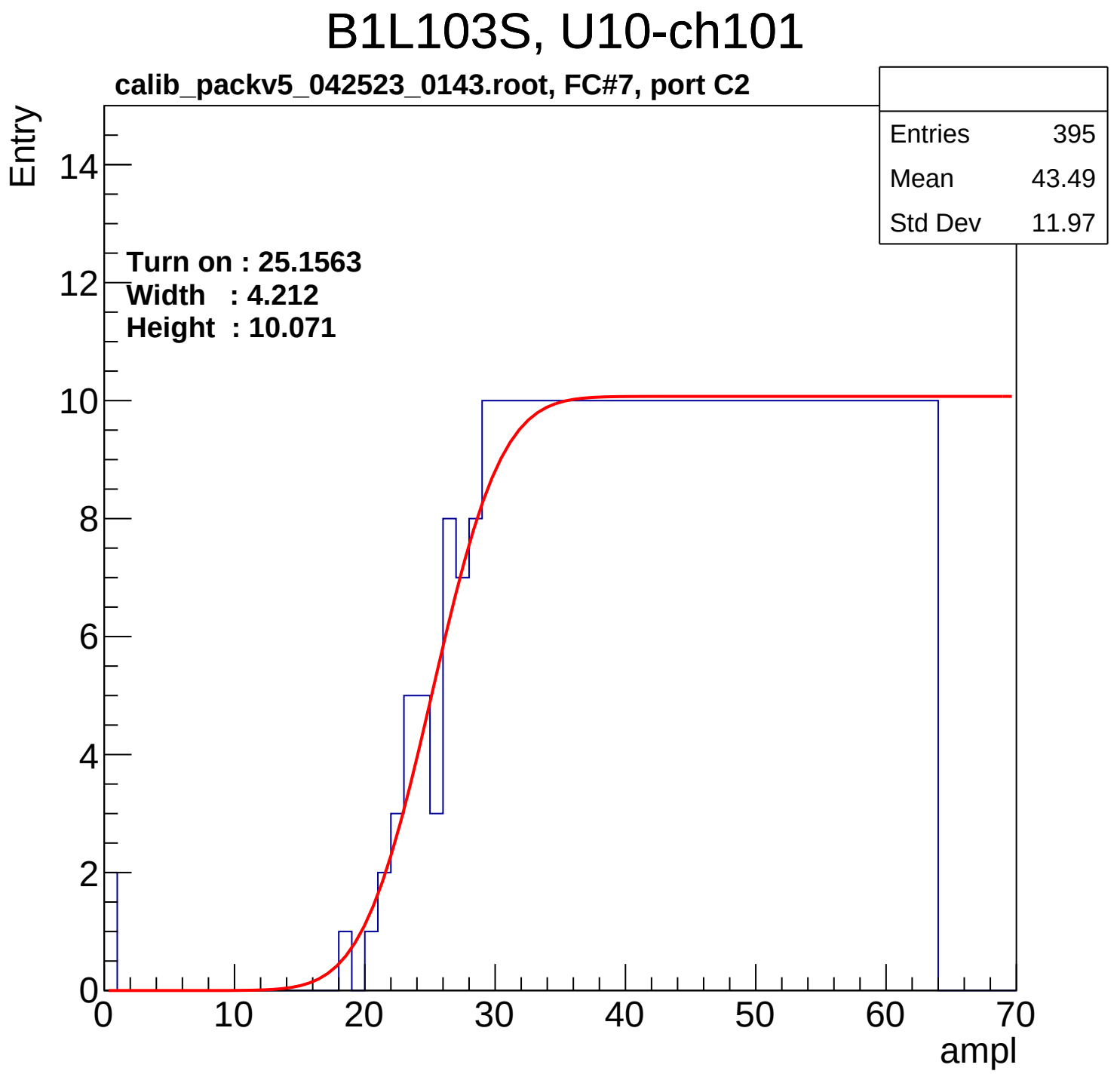
B1L103S, U10-ch101
calib_packv5_042523_0143.root, FC#7, port C2
Entries 395
Mean 43.49
Std Dev 11.97
Turn on : 25.1563
Width : 4.212
Height : 10.071
Entry
ampl
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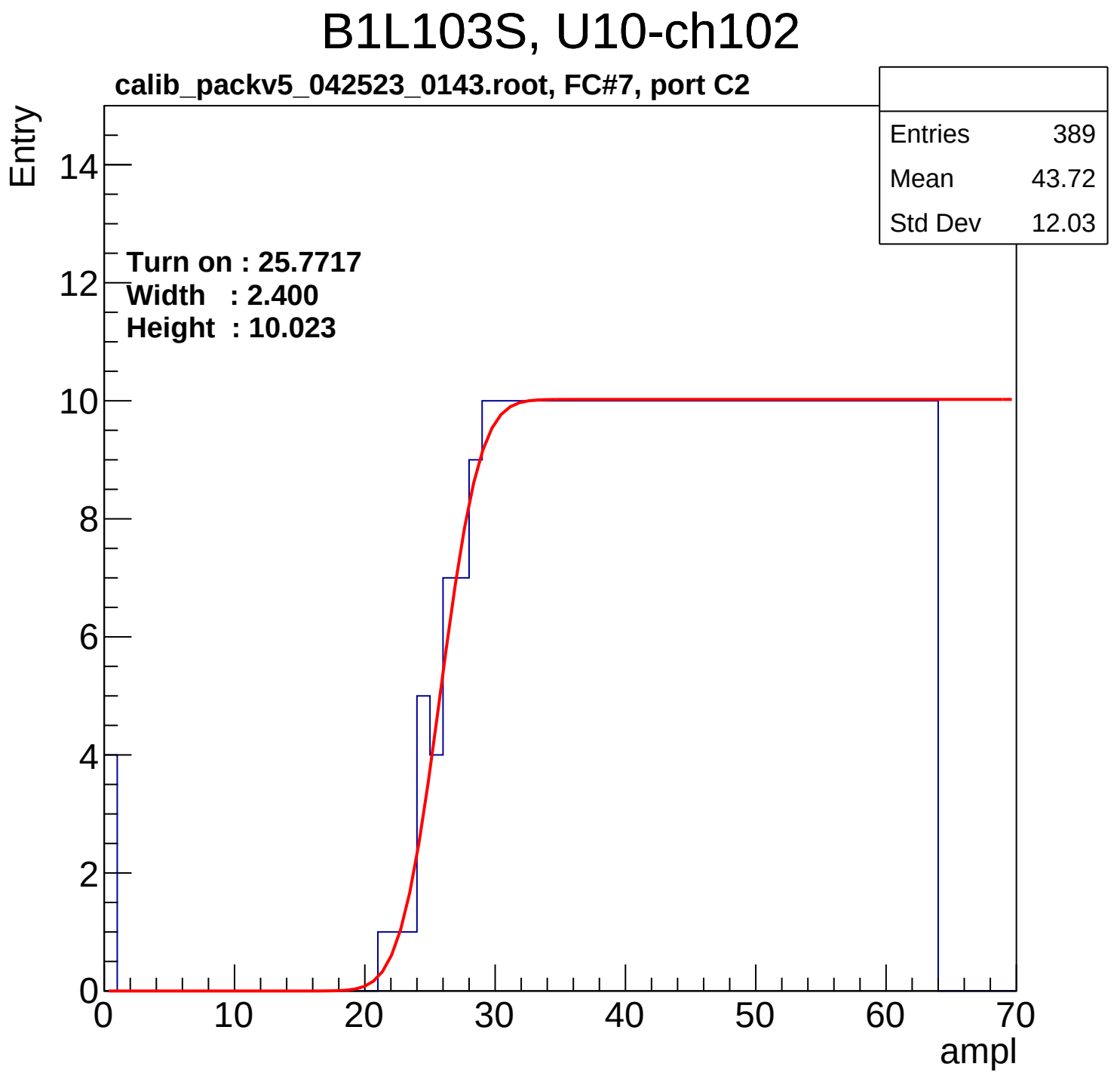
B1L103S, U10-ch102
calib_packv5_042523_0143.root, FC#7, port C2
Entries 389
Mean 43.72
Std Dev 12.03
Turn on : 25.7717
Width : 2.400
Height : 10.023
Entry
ampl
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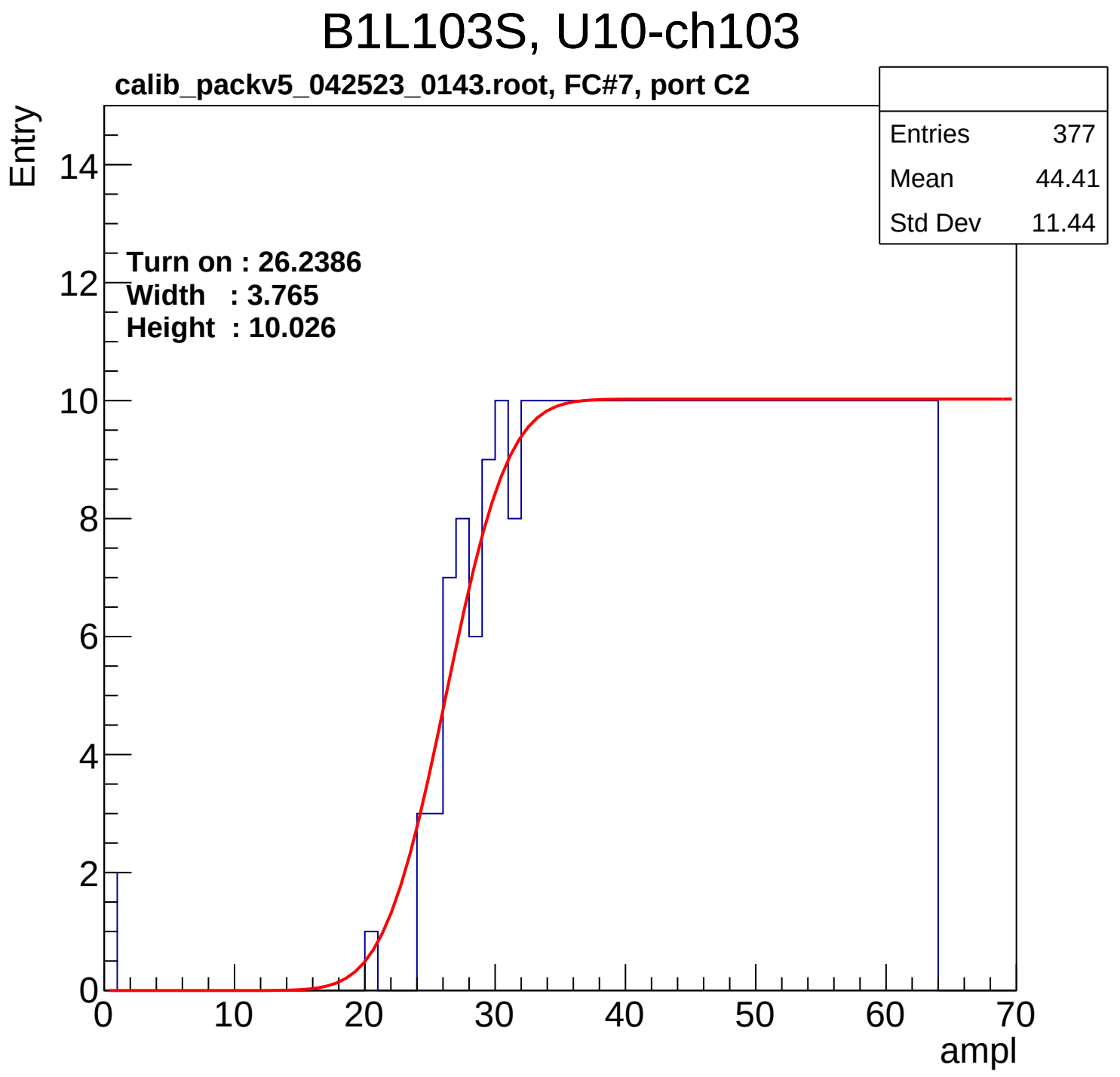
B1L103S, U10-ch103
calib_packv5_042523_0143.root, FC#7, port C2
Entries 377
Mean 44.41
Std Dev 11.44
Turn on : 26.2386
Width : 3.765
Height : 10.026
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ampl
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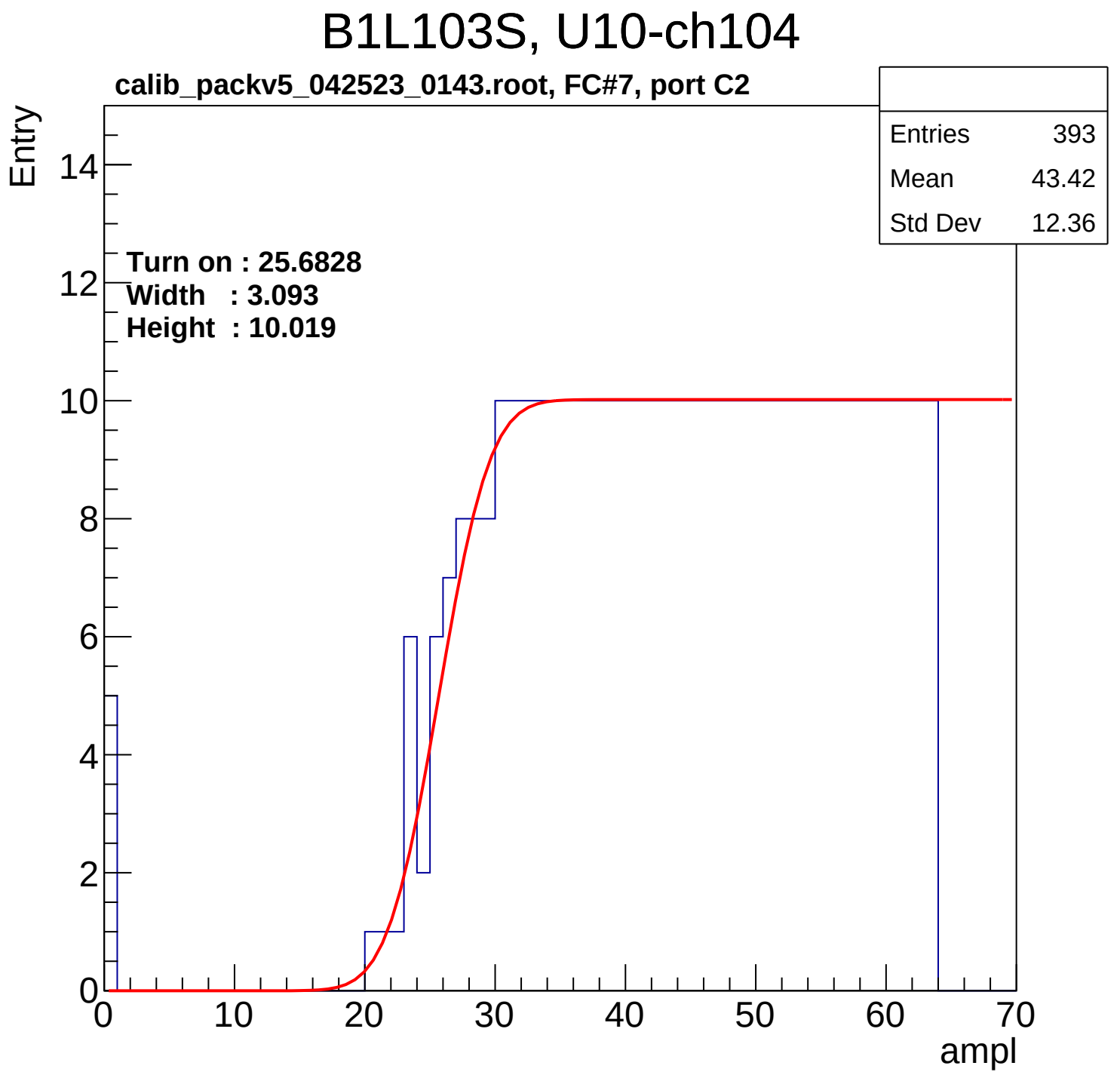
B1L103S, U10-ch104
calib_packv5_042523_0143.root, FC#7, port C2
Entries 393
Mean 43.42
Std Dev 12.36
Turn on : 25.6828
Width : 3.093
Height : 10.019
Entry
ampl
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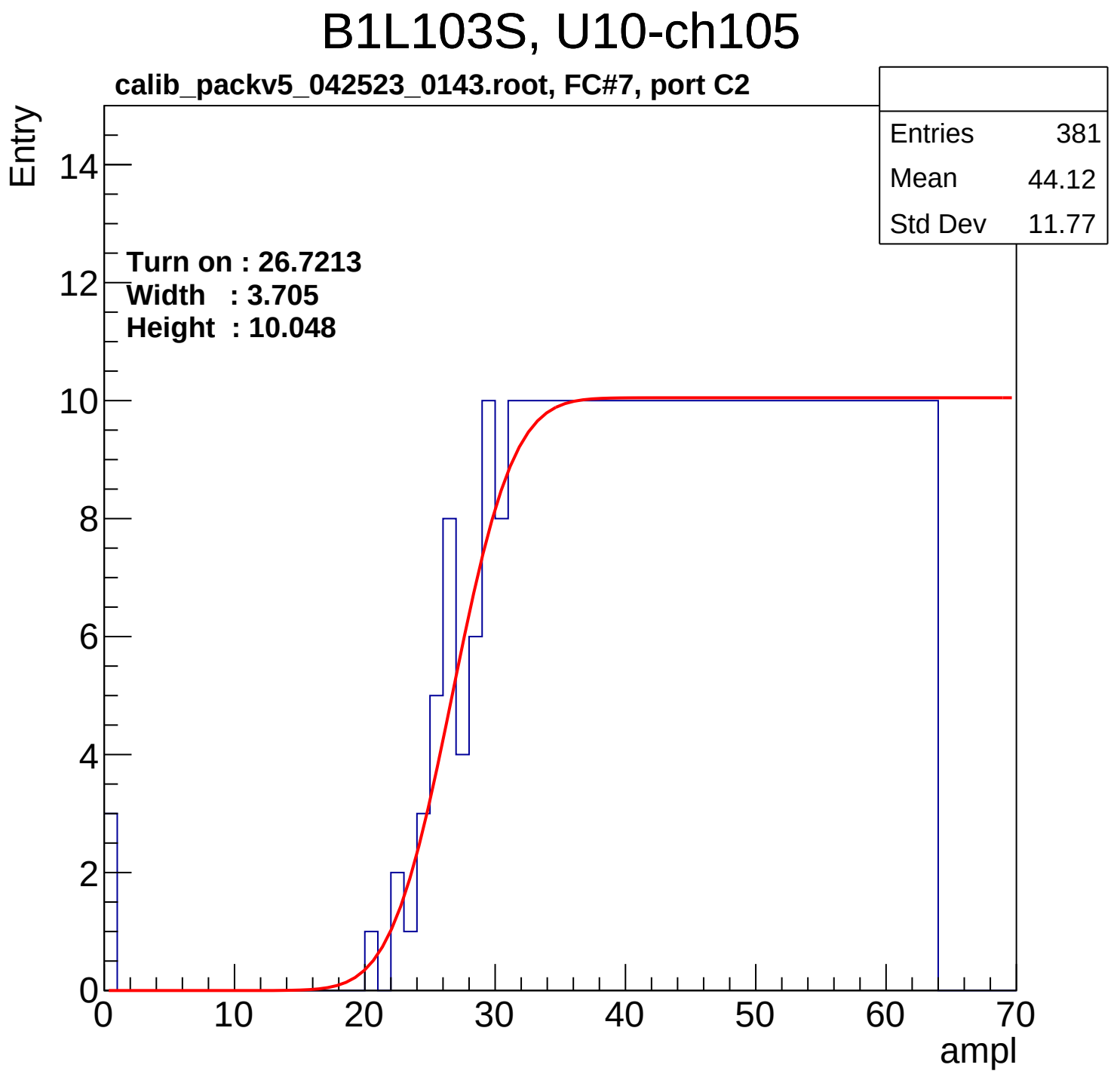
B1L103S, U10-ch105
calib_packv5_042523_0143.root, FC#7, port C2
Entries 381
Mean 44.12
Std Dev 11.77
Turn on : 26.7213
Width : 3.705
Height : 10.048
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ampl
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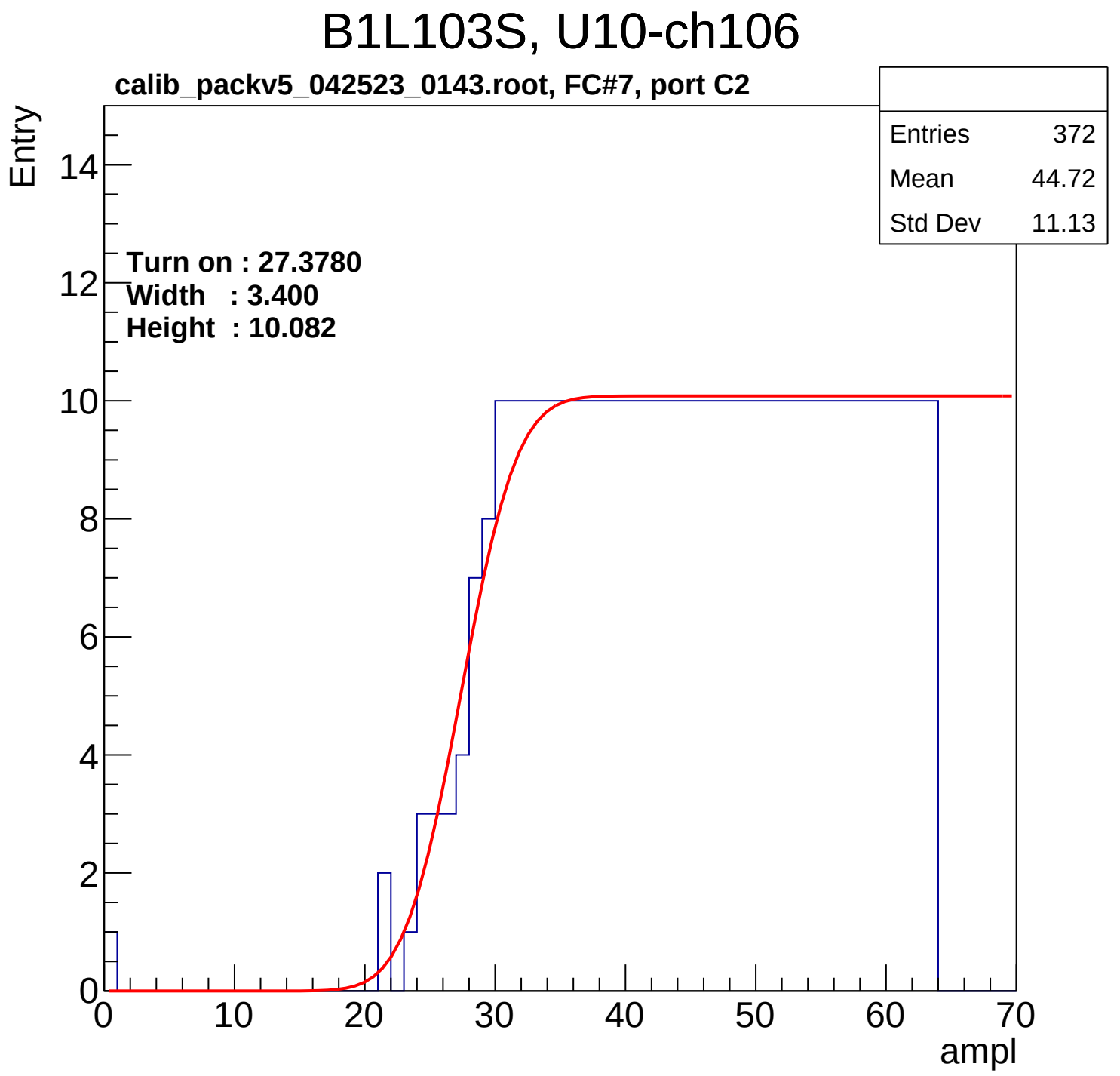
B1L103S, U10-ch106
calib_packv5_042523_0143.root, FC#7, port C2
Entries 372
Mean 44.72
Std Dev 11.13
Turn on : 27.3780
Width : 3.400
Height : 10.082
Entry
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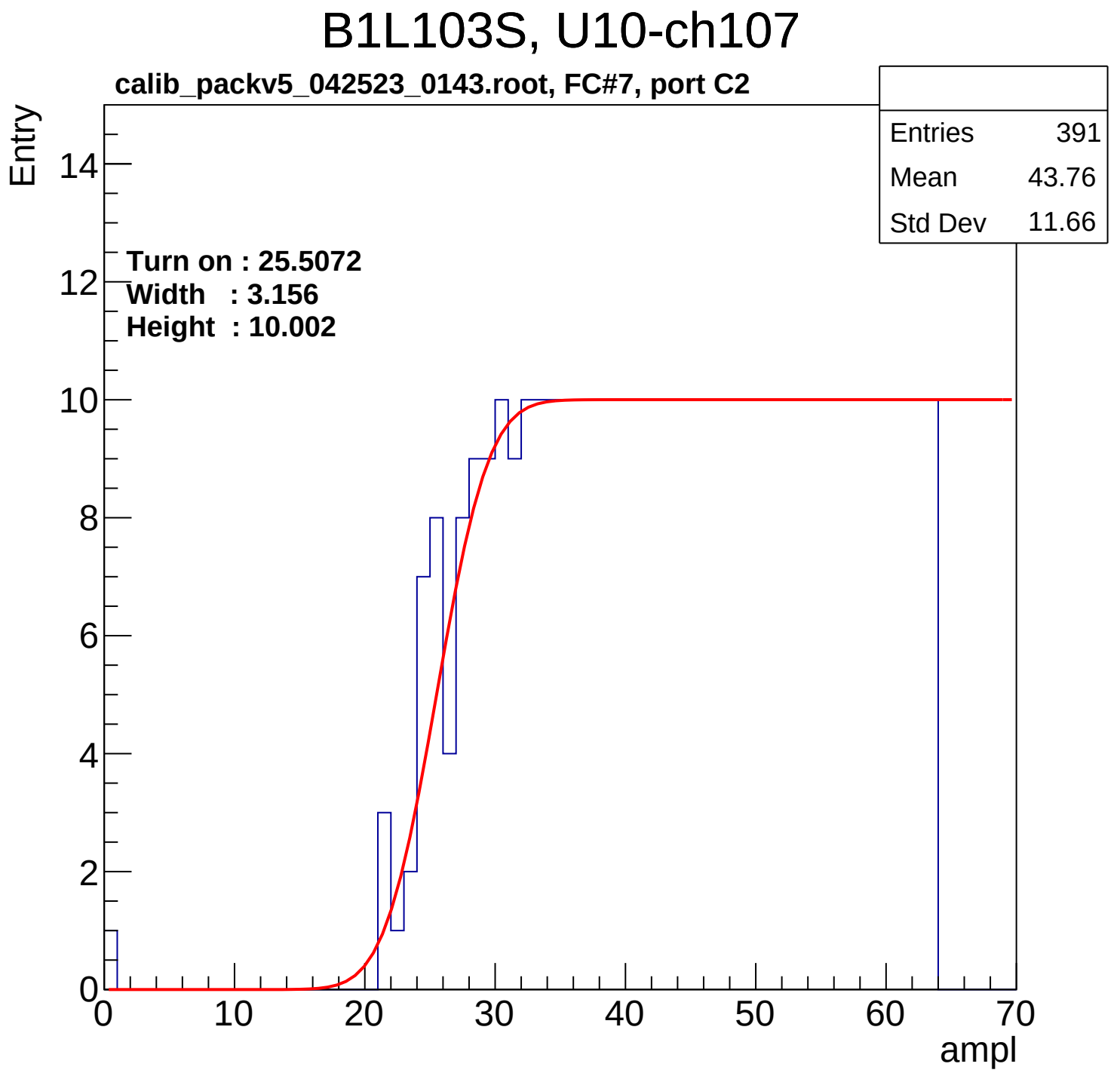
B1L103S, U10-ch107
calib_packv5_042523_0143.root, FC#7, port C2
Entries 391
Mean 43.76
Std Dev 11.66
Turn on : 25.5072
Width : 3.156
Height : 10.002
Entry
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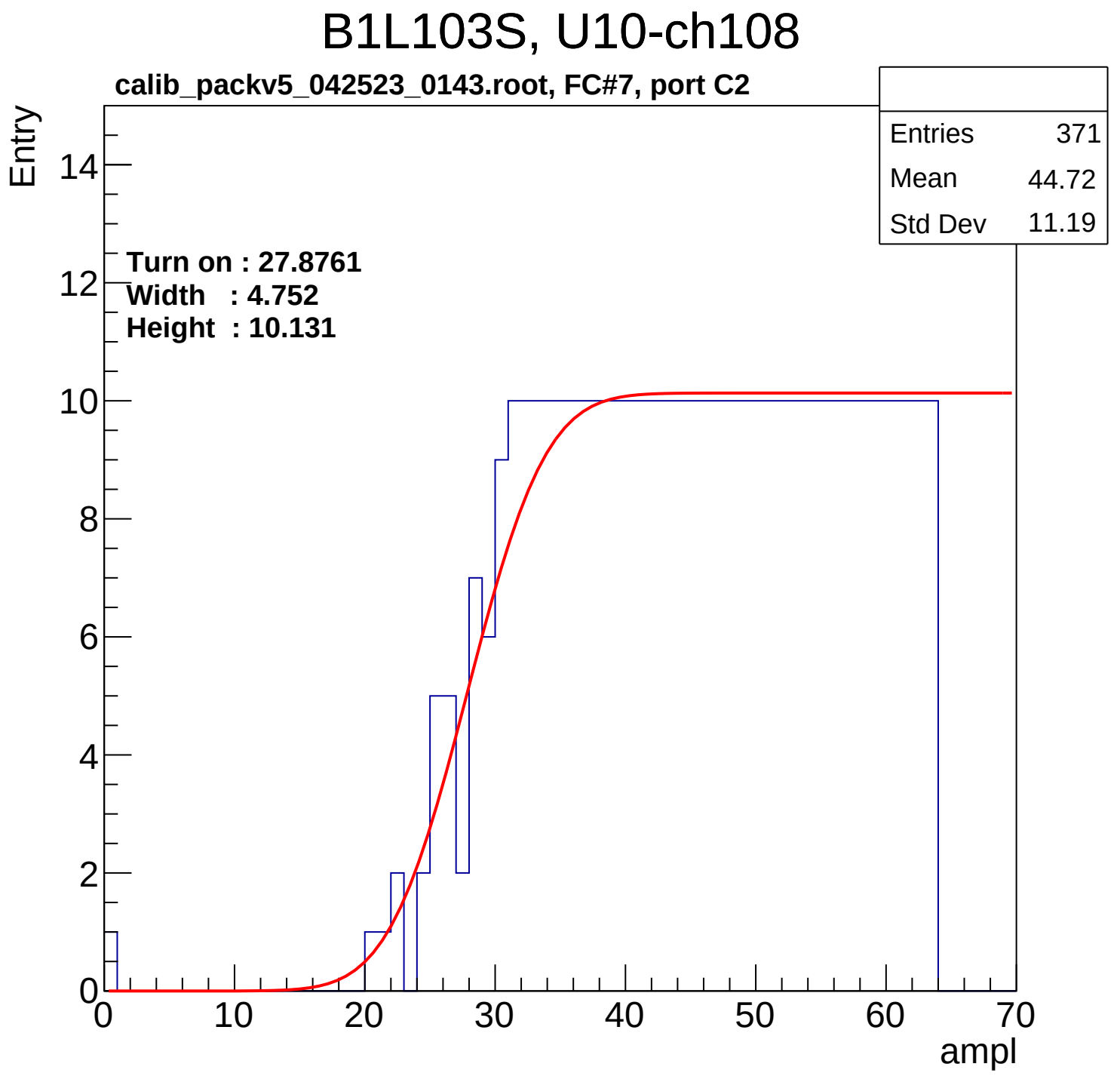
B1L103S, U10-ch108
calib_packv5_042523_0143.root, FC#7, port C2
Entries 371
Mean 44.72
Std Dev 11.19
Turn on : 27.8761
Width : 4.752
Height : 10.131
Entry
ampl
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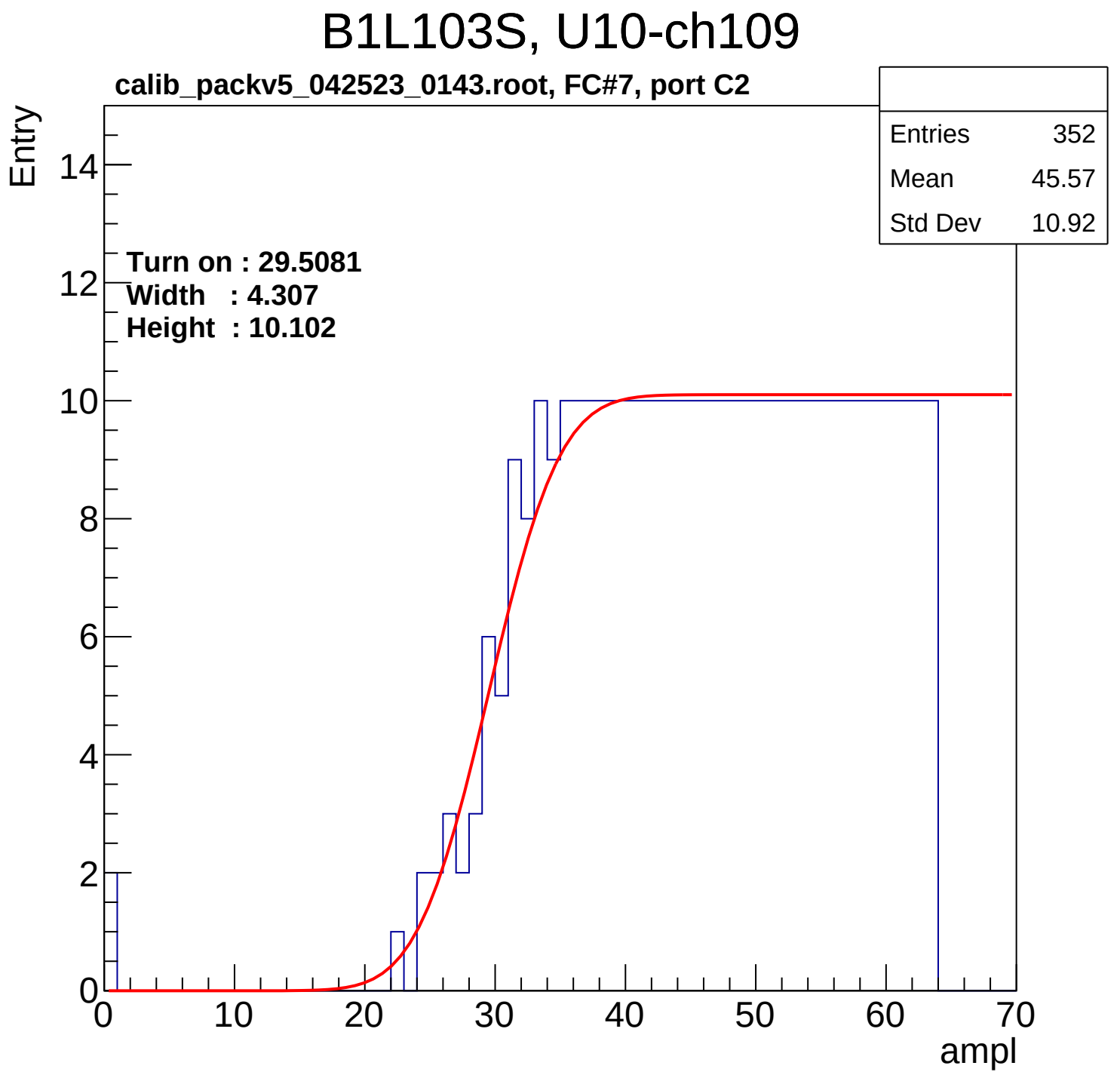
B1L103S, U10-ch109
calib_packv5_042523_0143.root, FC#7, port C2
Entries 352
Mean 45.57
Std Dev 10.92
Turn on : 29.5081
Width : 4.307
Height : 10.102
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ampl
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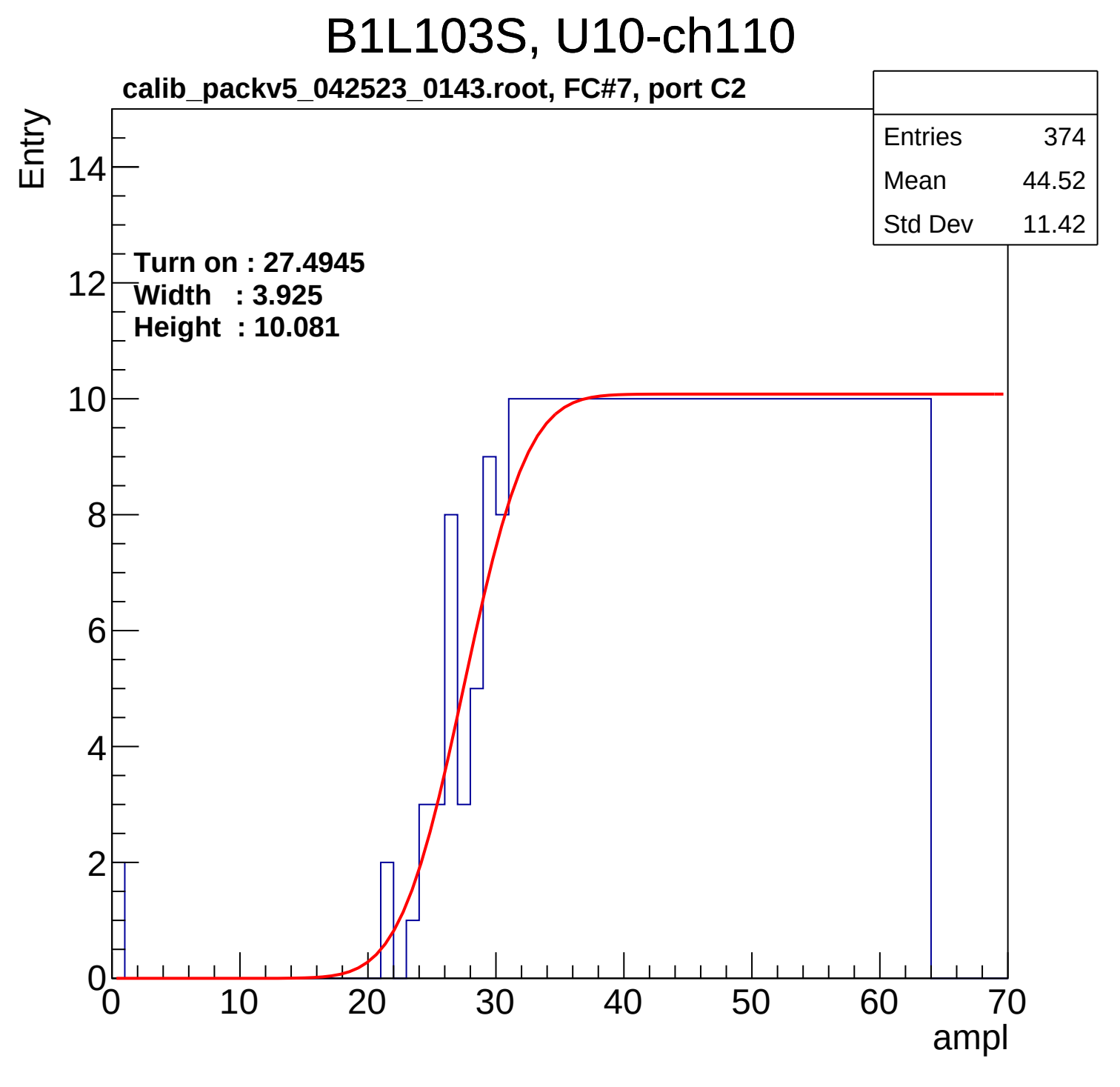
B1L103S, U10-ch110
calib_packv5_042523_0143.root, FC#7, port C2
Entries 374
Mean 44.52
Std Dev 11.42
Turn on : 27.4945
Width : 3.925
Height : 10.081
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ampl
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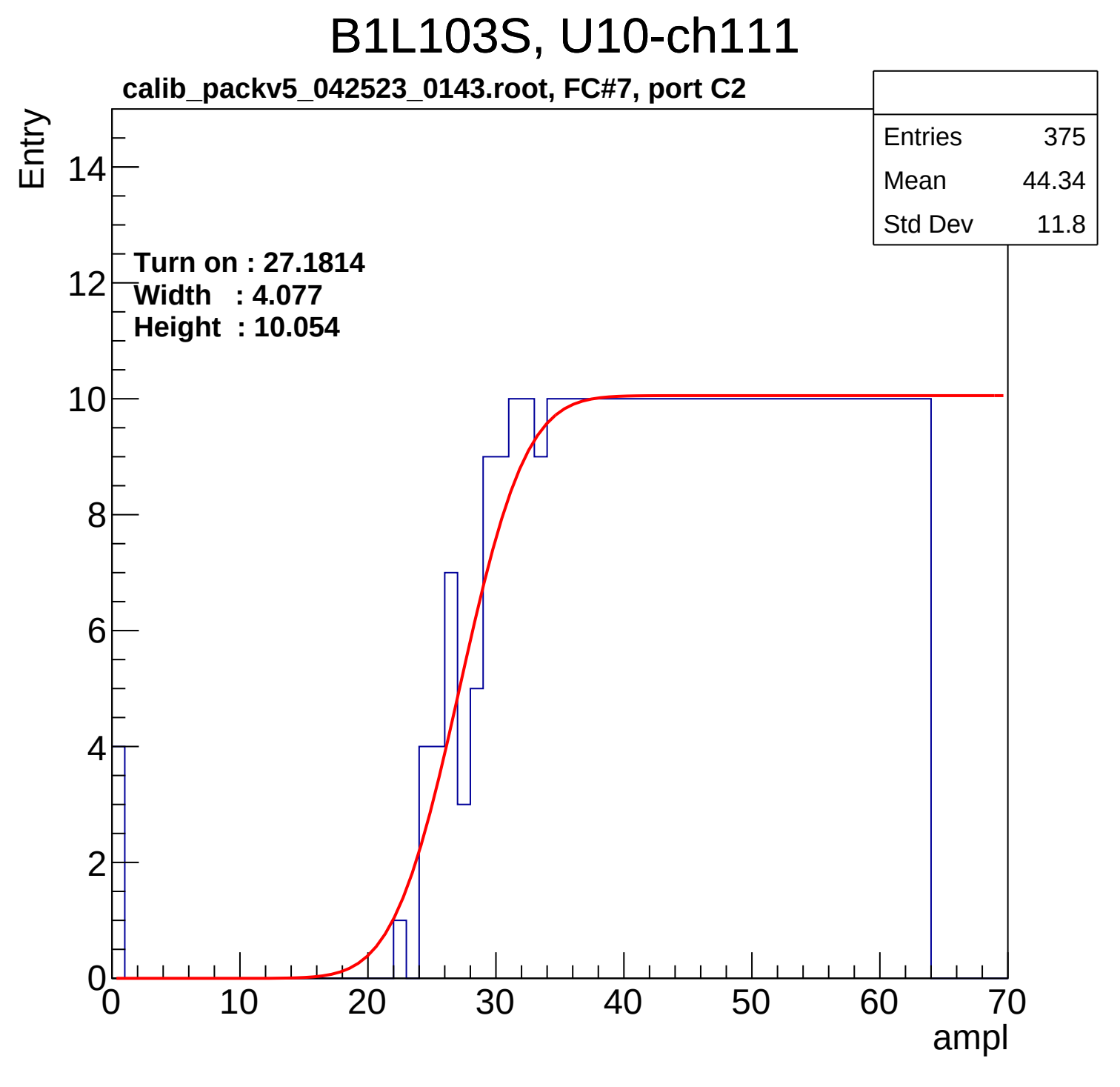
B1L103S, U10-ch111
calib_packv5_042523_0143.root, FC#7, port C2
Entries 375
Mean 44.34
Std Dev 11.8
Turn on : 27.1814
Width : 4.077
Height : 10.054
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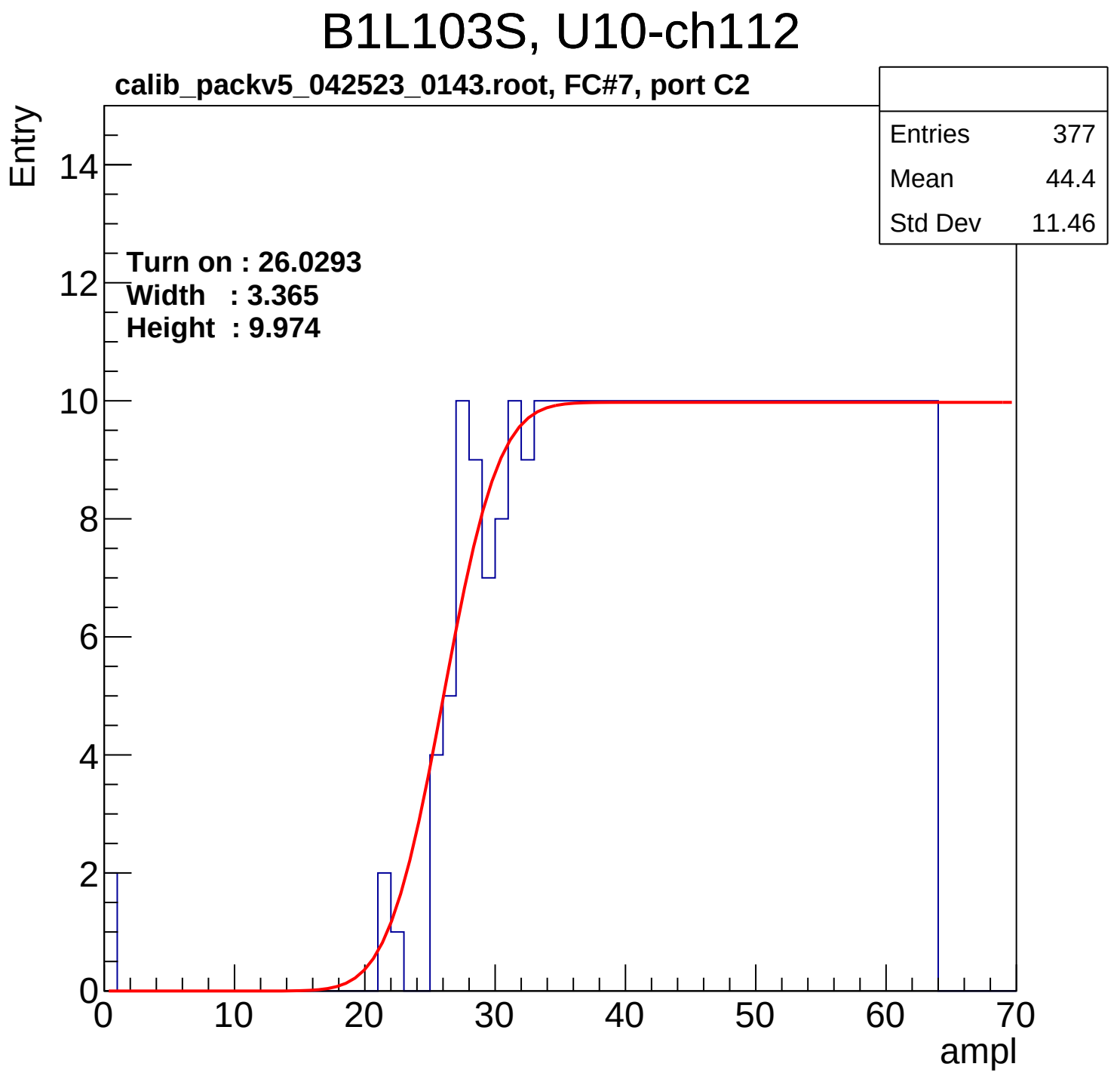
B1L103S, U10-ch112
calib_packv5_042523_0143.root, FC#7, port C2
Entries 377
Mean 44.4
Std Dev 11.46
Turn on : 26.0293
Width : 3.365
Height : 9.974
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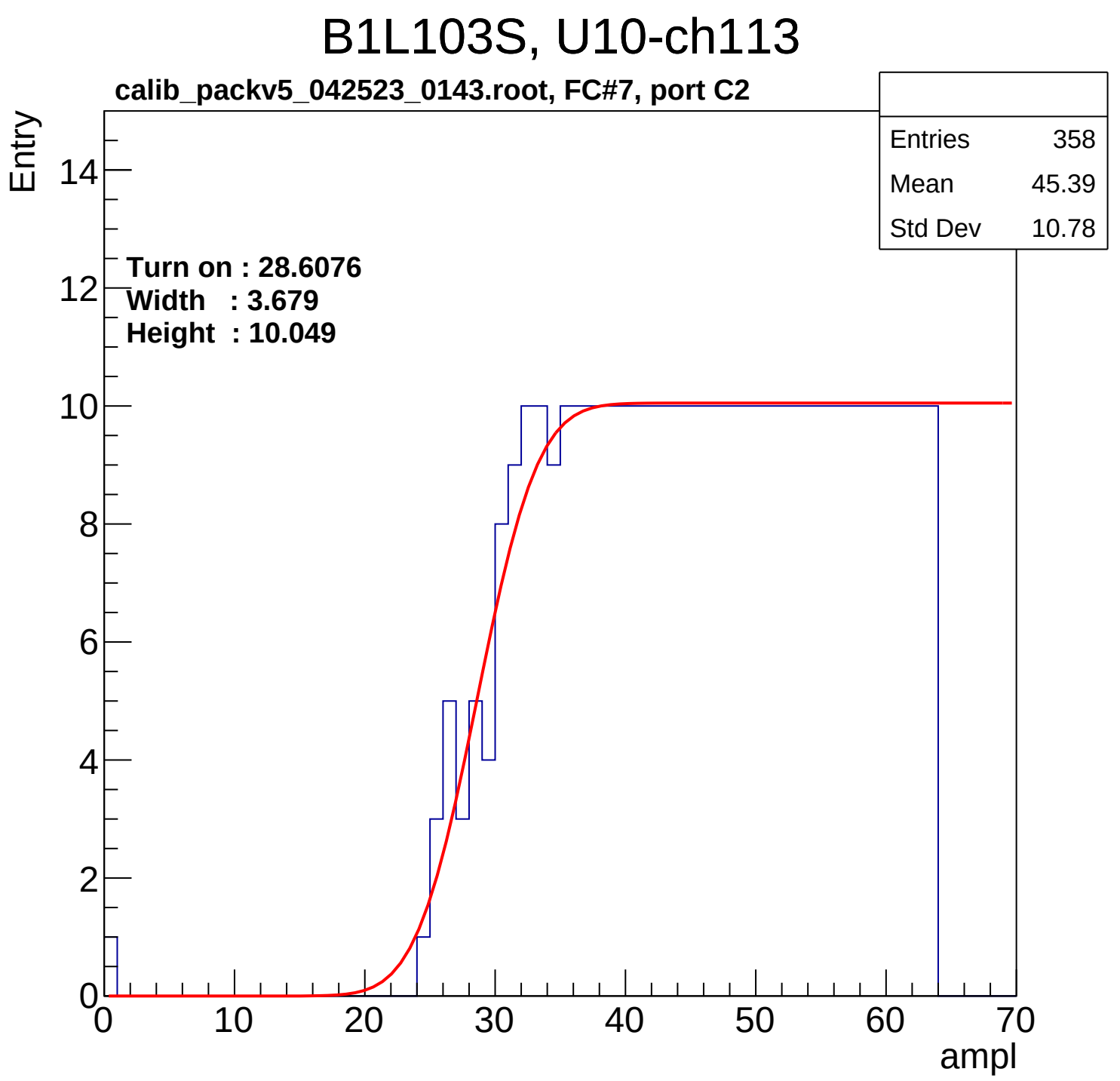
B1L103S, U10-ch113
calib_packv5_042523_0143.root, FC#7, port C2
Entries 358
Mean 45.39
Std Dev 10.78
Turn on : 28.6076
Width : 3.679
Height : 10.049
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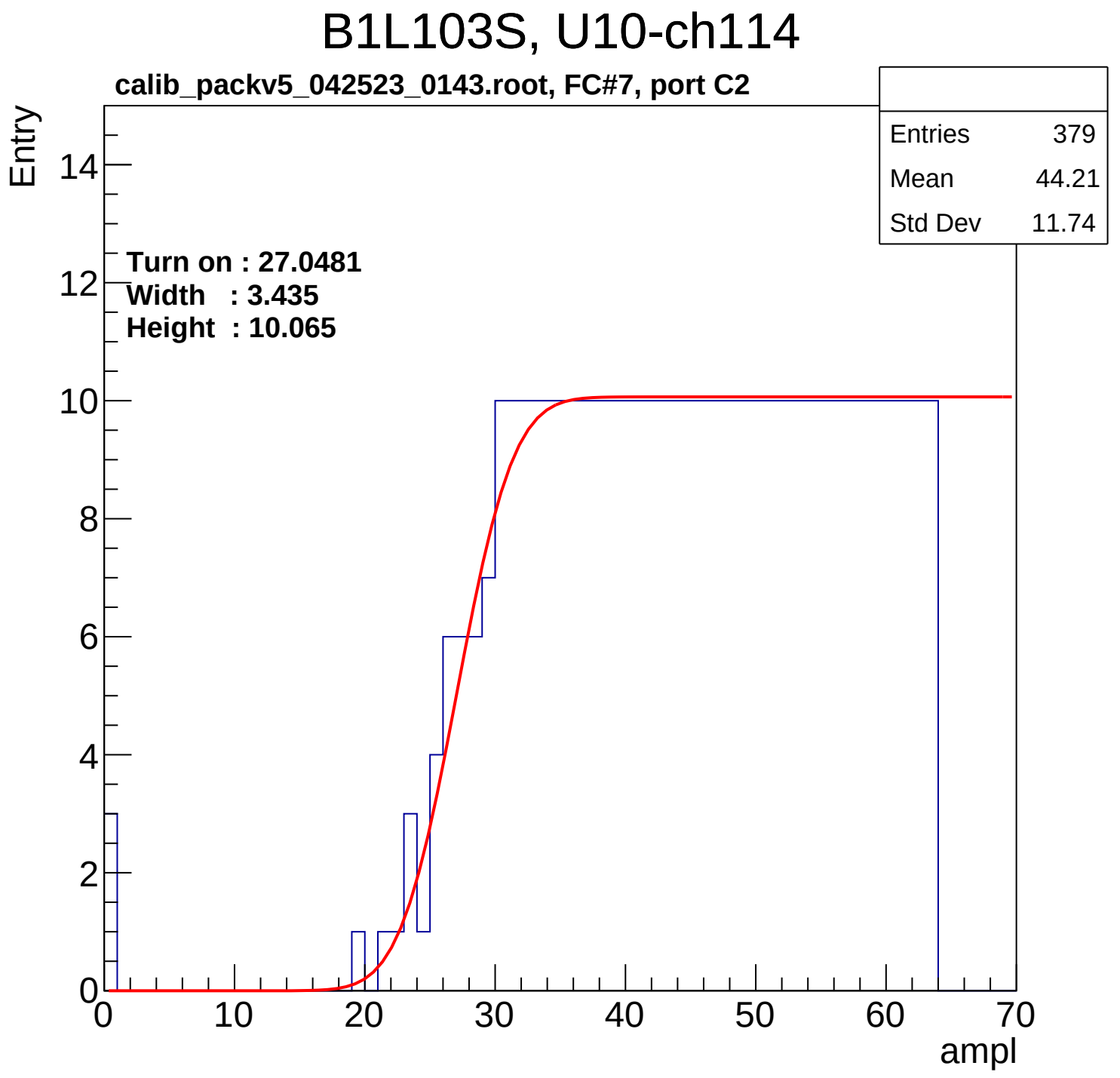
B1L103S, U10-ch114
calib_packv5_042523_0143.root, FC#7, port C2
Entries 379
Mean 44.21
Std Dev 11.74
Turn on : 27.0481
Width : 3.435
Height : 10.065
Entry
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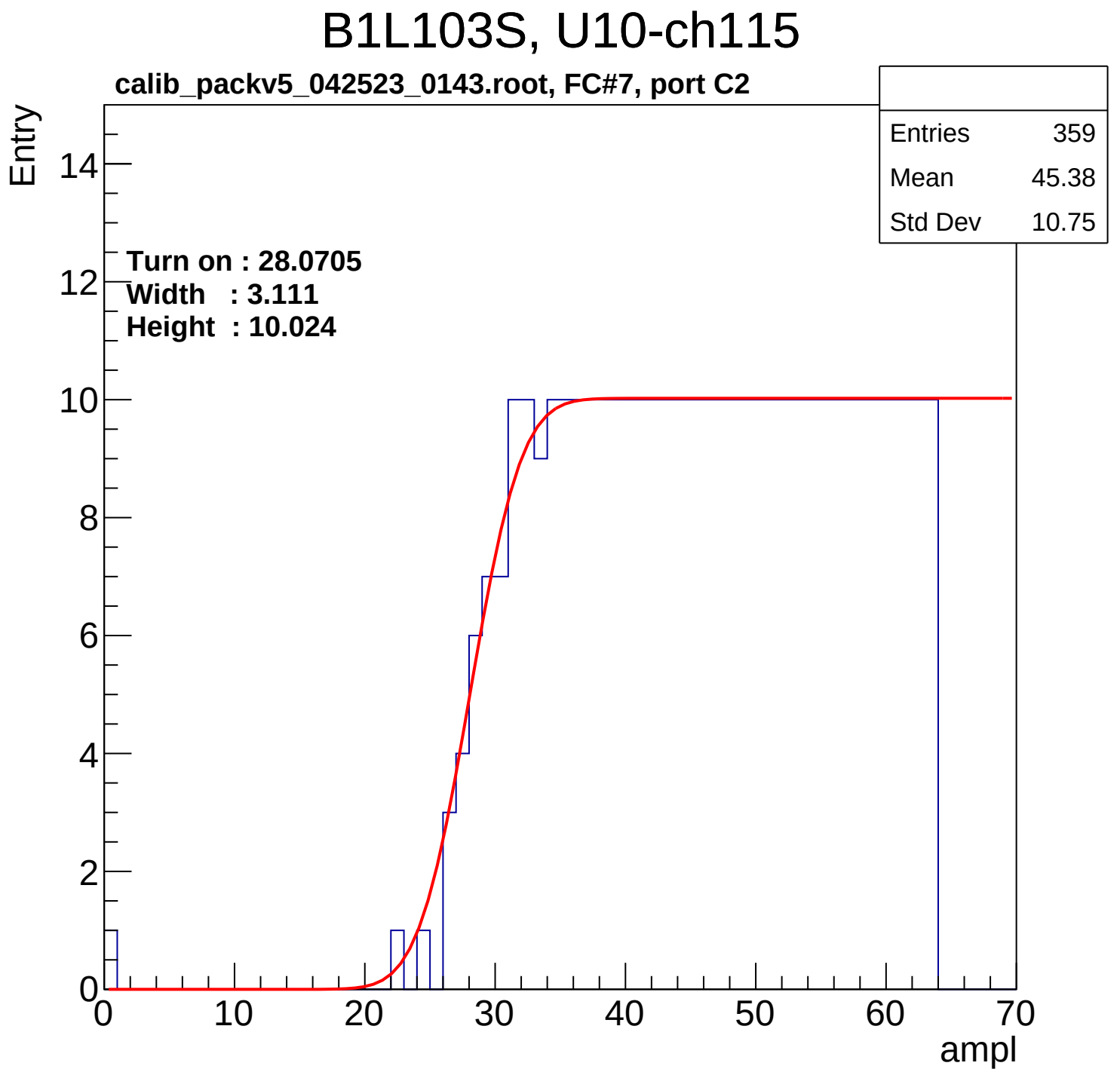
B1L103S, U10-ch115
calib_packv5_042523_0143.root, FC#7, port C2
Entries 359
Mean 45.38
Std Dev 10.75
Turn on : 28.0705
Width : 3.111
Height : 10.024
Entry
ampl
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4
6
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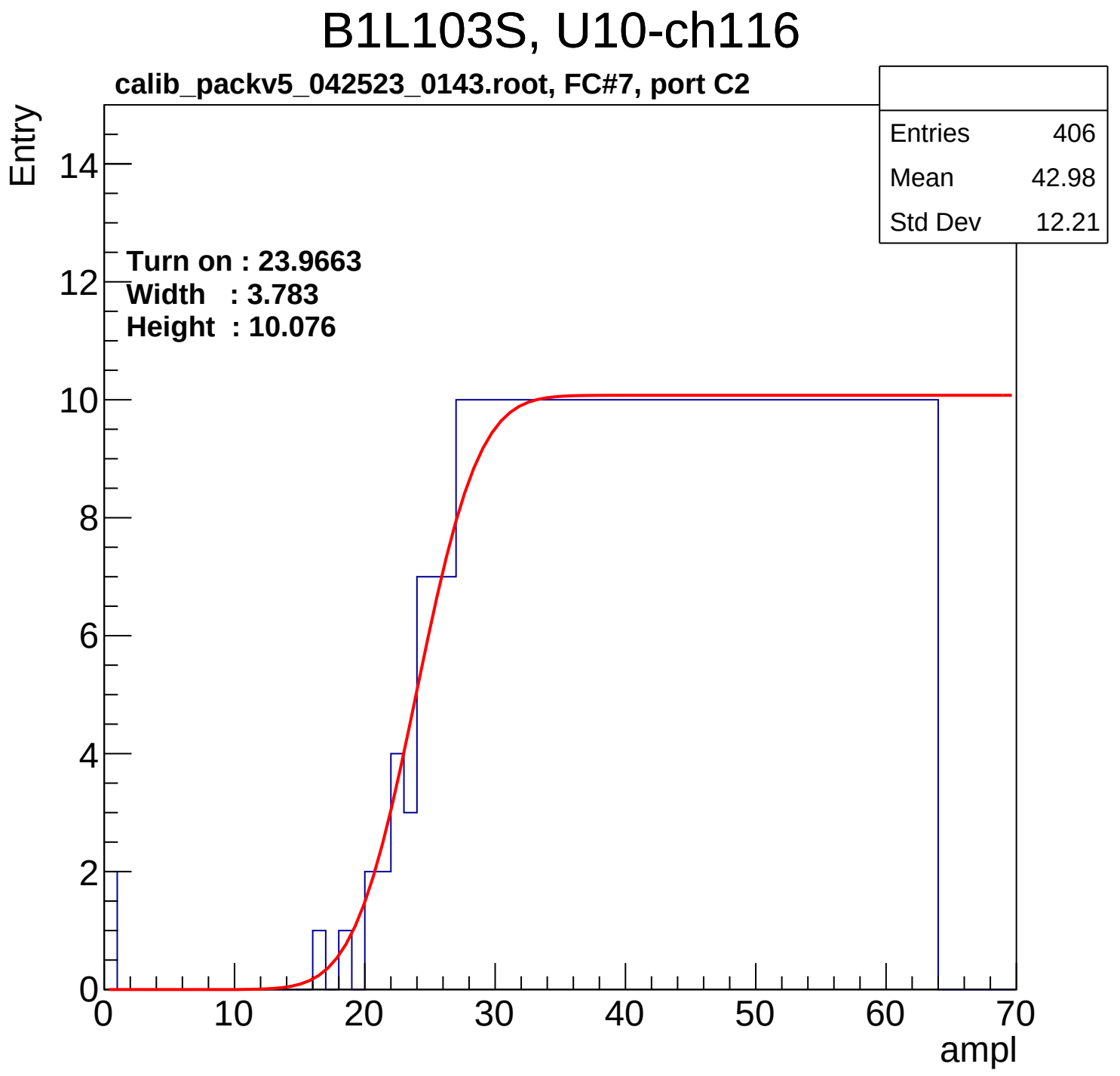
B1L103S, U10-ch116
calib_packv5_042523_0143.root, FC#7, port C2
Entries 406
Mean 42.98
Std Dev 12.21
Turn on : 23.9663
Width : 3.783
Height : 10.076
Entry
ampl
0
2
4
6
8
10
12
14
0
10
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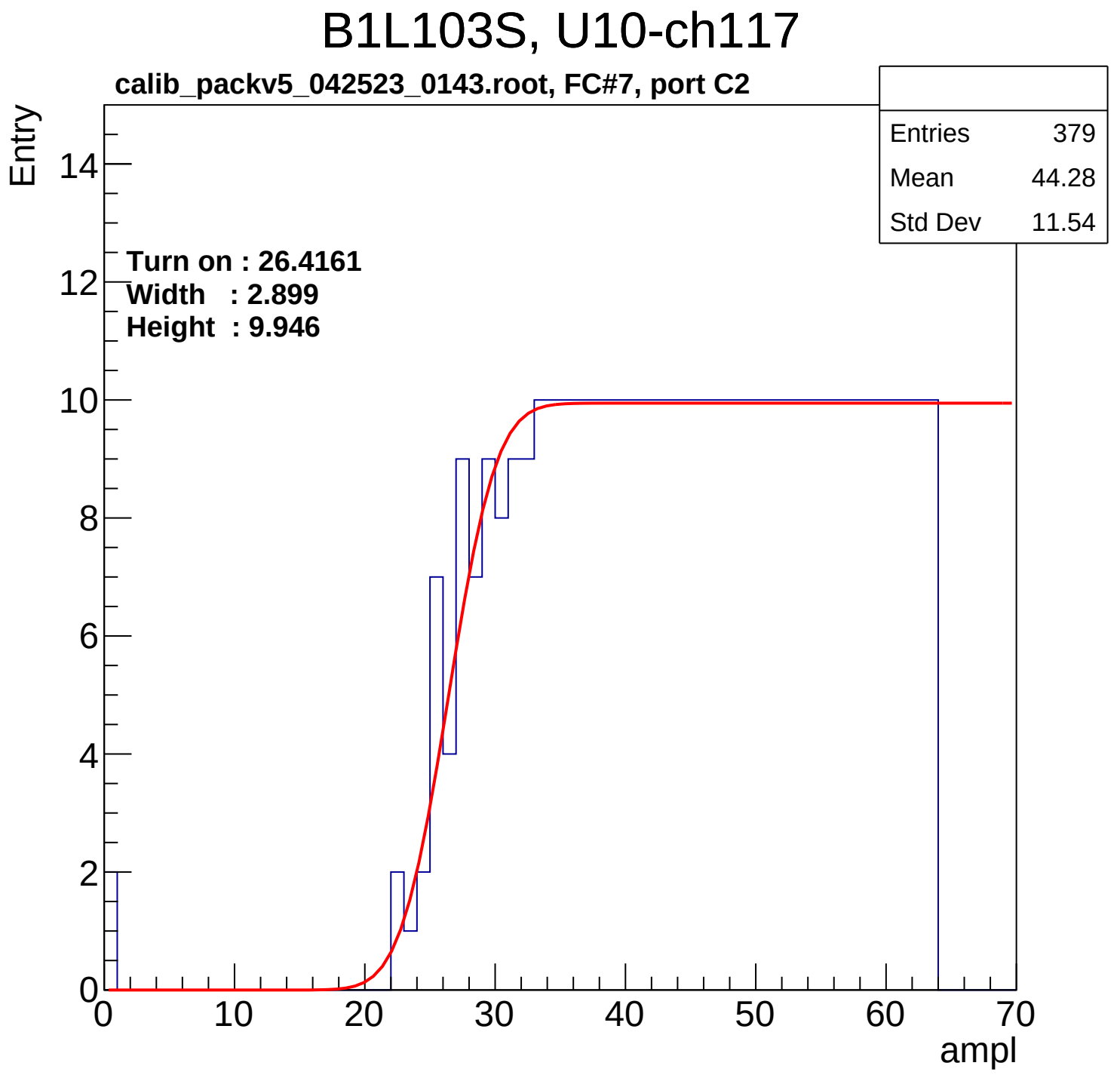
B1L103S, U10-ch117
calib_packv5_042523_0143.root, FC#7, port C2
Entries 379
Mean 44.28
Std Dev 11.54
Turn on : 26.4161
Width : 2.899
Height : 9.946
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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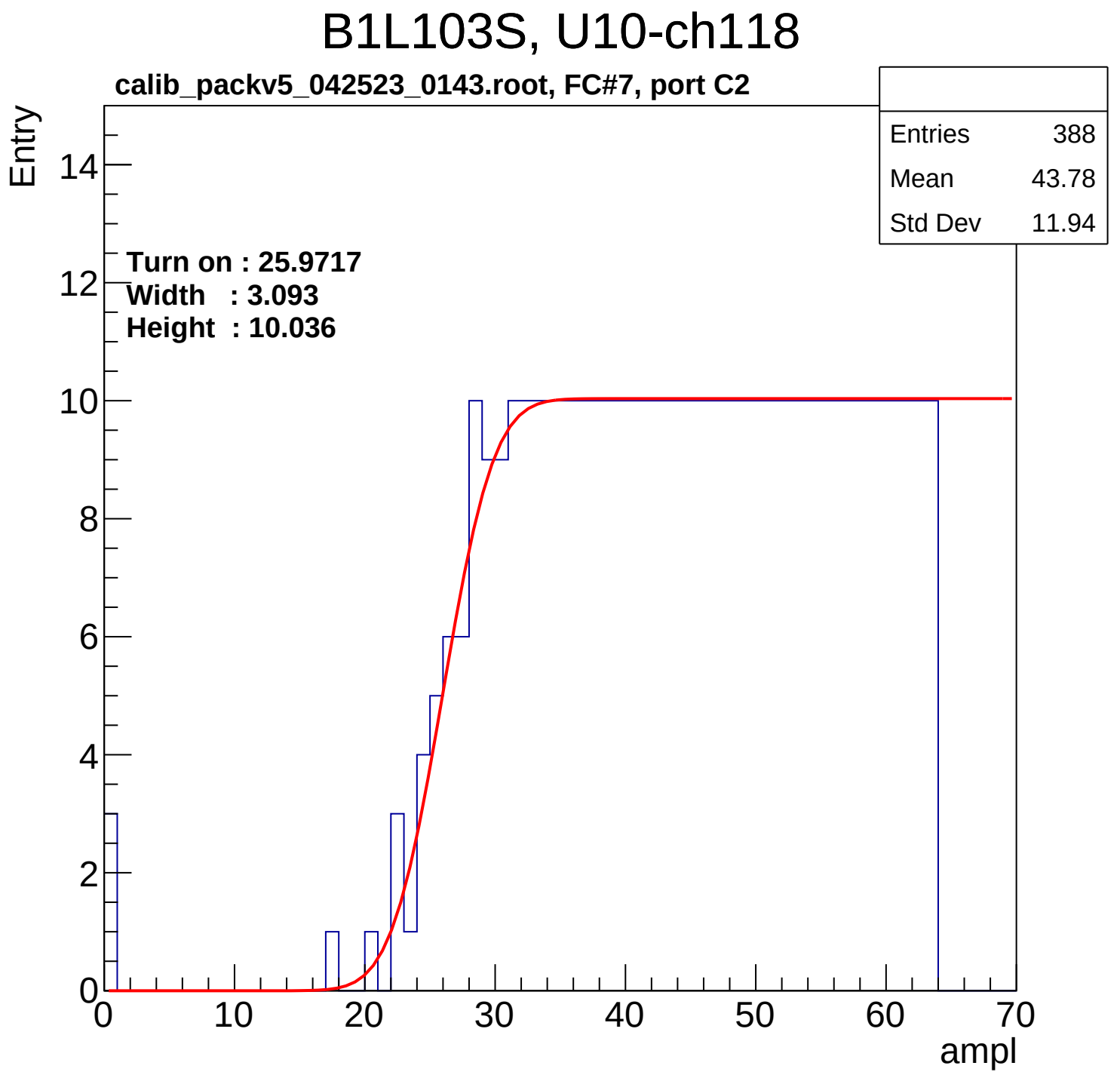
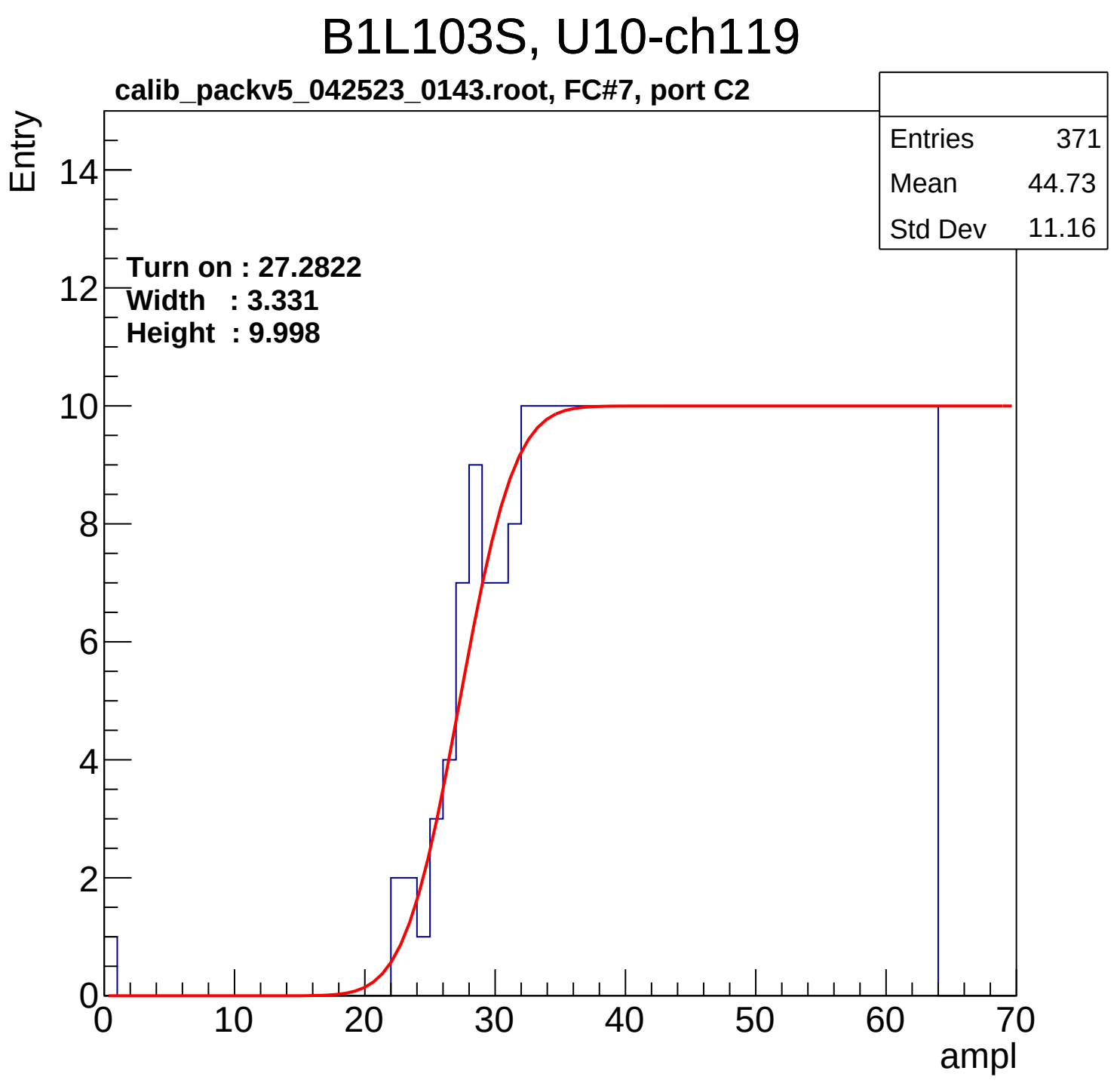
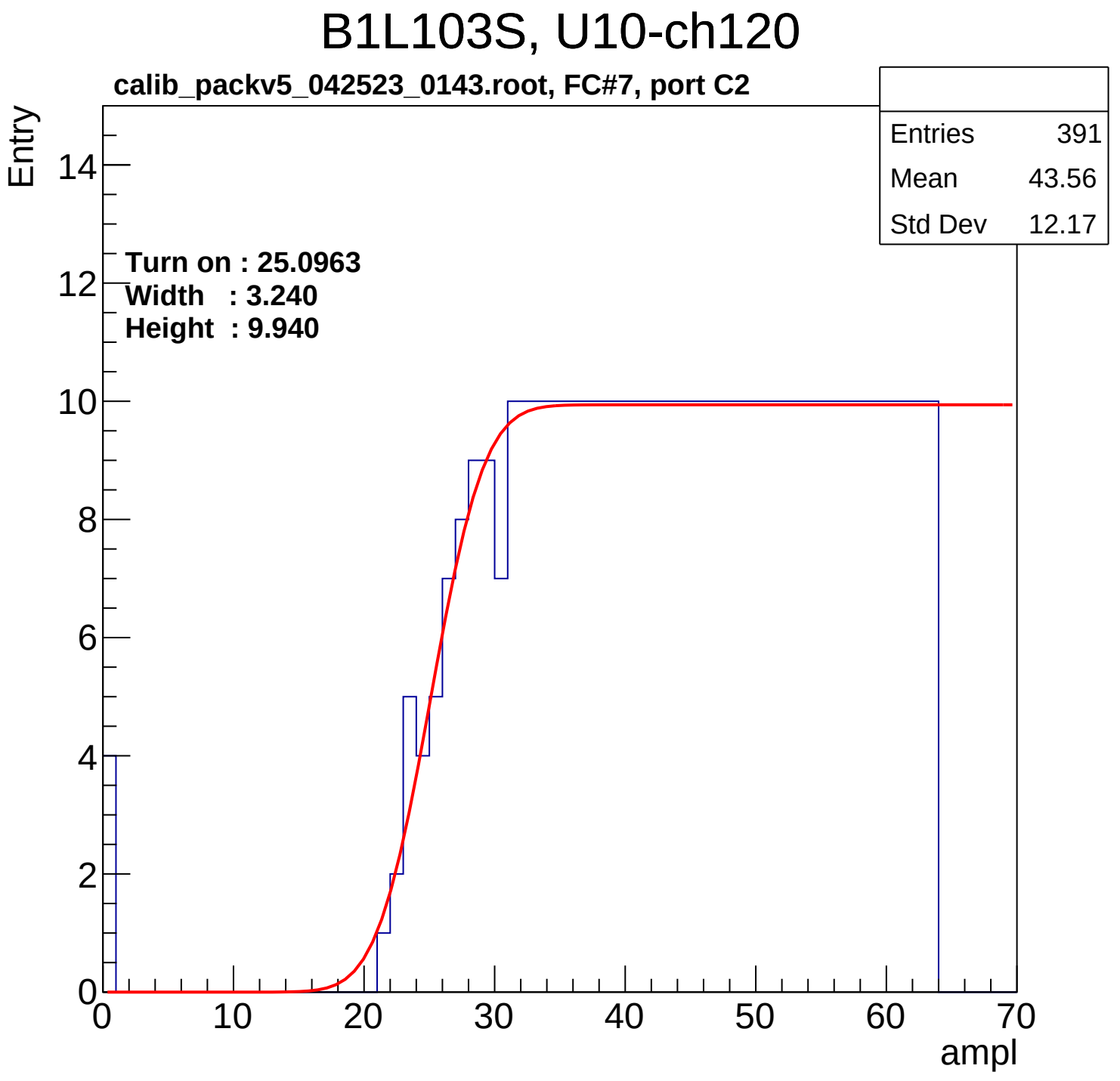

B1L103S, U10-ch118
calib_packv5_042523_0143.root, FC#7, port C2
Entries 388
Mean 43.78
Std Dev 11.94
Turn on : 25.9717
Width : 3.093
Height : 10.036
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L103S, U10-ch119
calib_packv5_042523_0143.root, FC#7, port C2
Entries 371
Mean 44.73
Std Dev 11.16
Turn on : 27.2822
Width : 3.331
Height : 9.998
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L103S, U10-ch120
calib_packv5_042523_0143.root, FC#7, port C2
Entries 391
Mean 43.56
Std Dev 12.17
Turn on : 25.0963
Width : 3.240
Height : 9.940
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
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60
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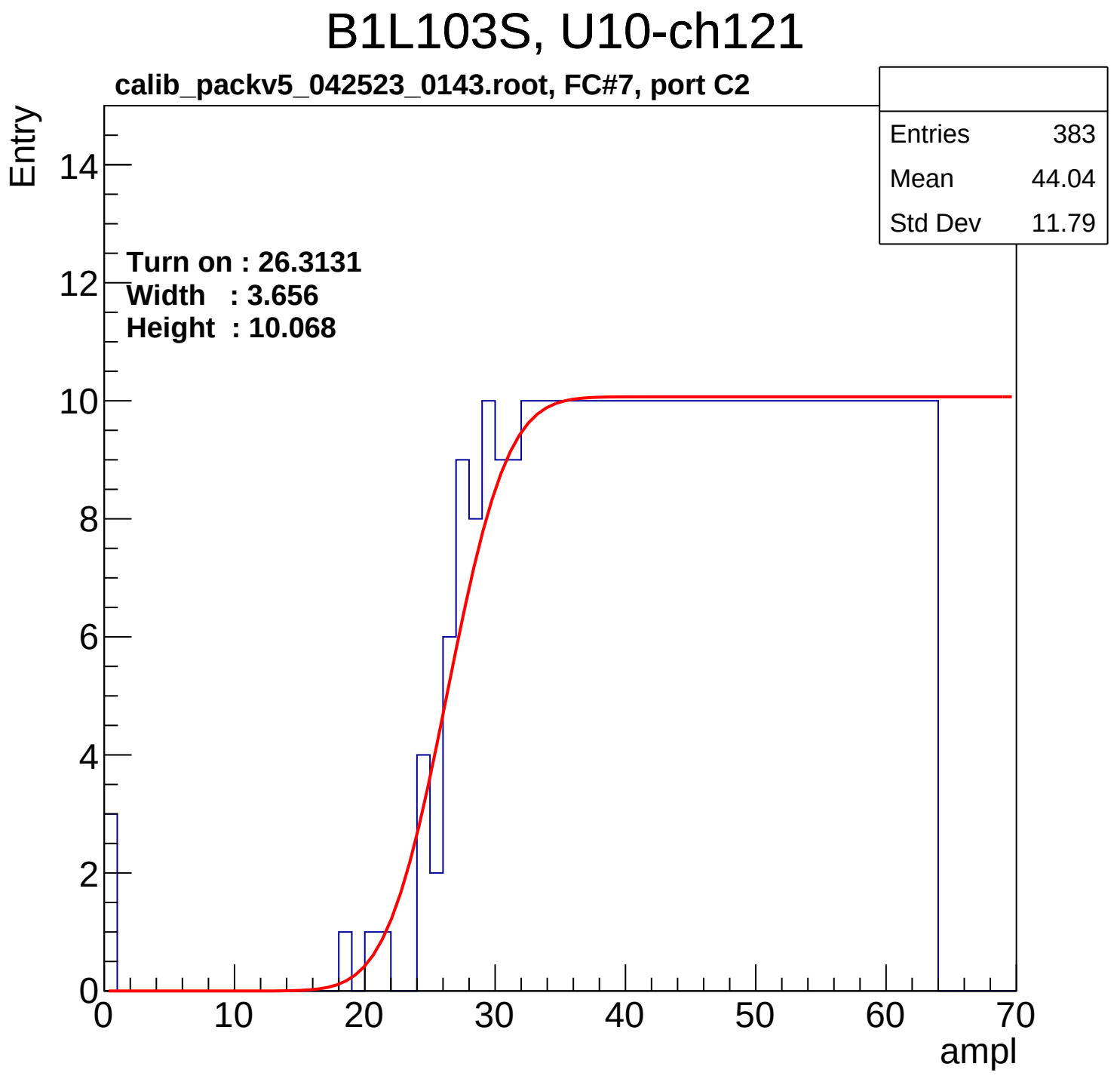
B1L103S, U10-ch121
calib_packv5_042523_0143.root, FC#7, port C2
Entries 383
Mean 44.04
Std Dev 11.79
Turn on : 26.3131
Width : 3.656
Height : 10.068
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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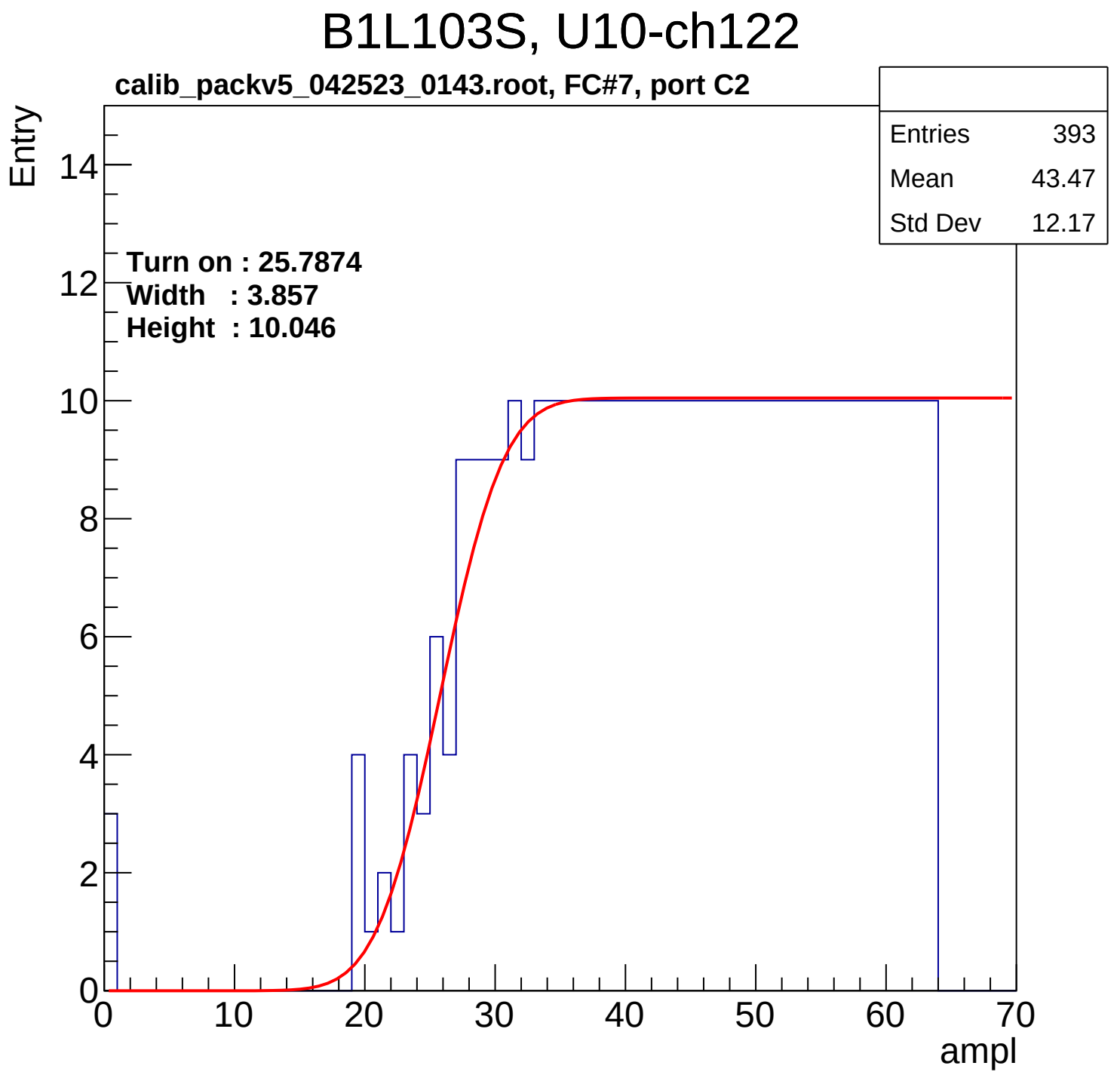
B1L103S, U10-ch122
calib_packv5_042523_0143.root, FC#7, port C2
Entries 393
Mean 43.47
Std Dev 12.17
Turn on : 25.7874
Width : 3.857
Height : 10.046
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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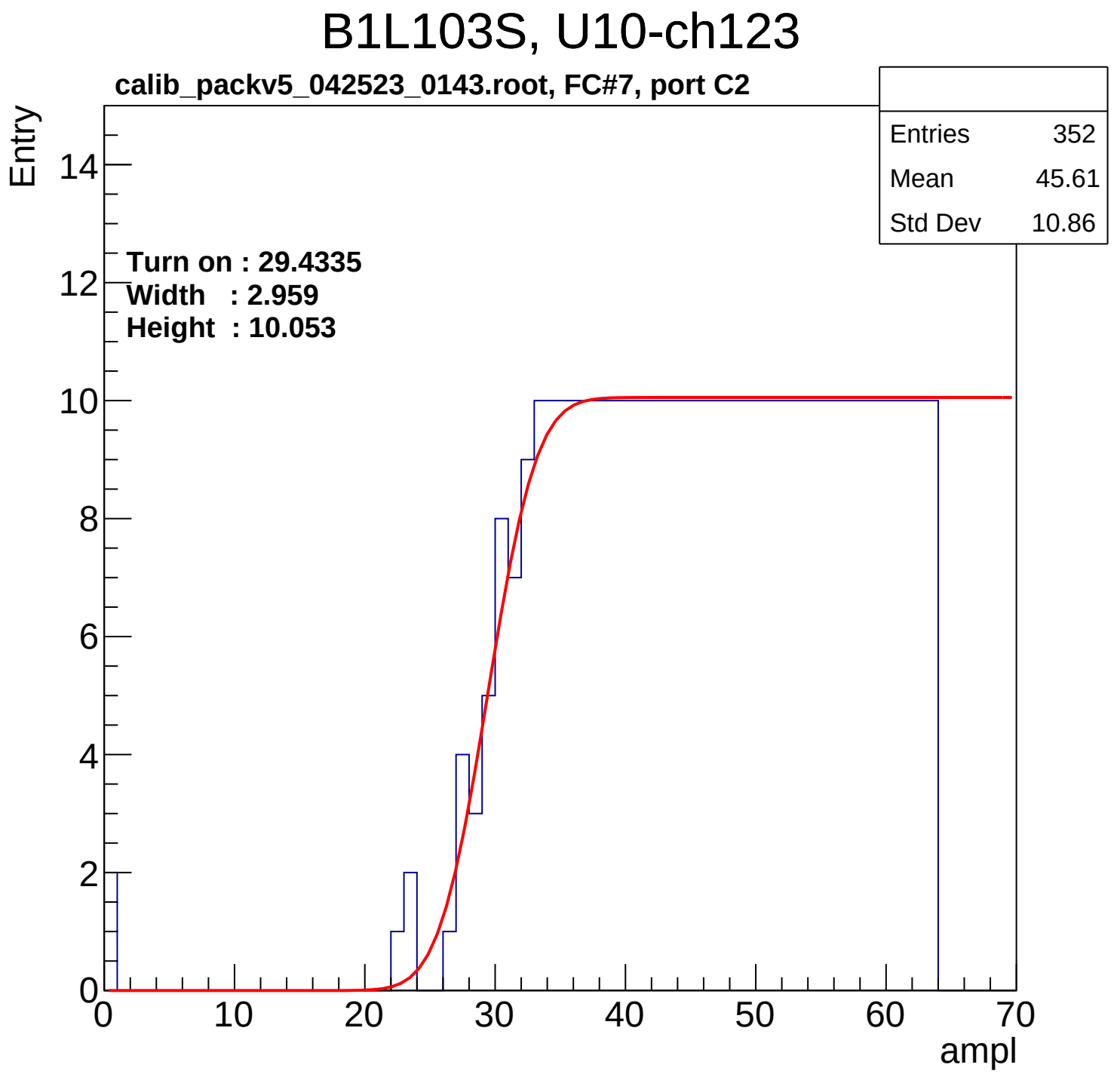
B1L103S, U10-ch123
calib_packv5_042523_0143.root, FC#7, port C2
Entries 352
Mean 45.61
Std Dev 10.86
Turn on : 29.4335
Width : 2.959
Height : 10.053
Entry
ampl
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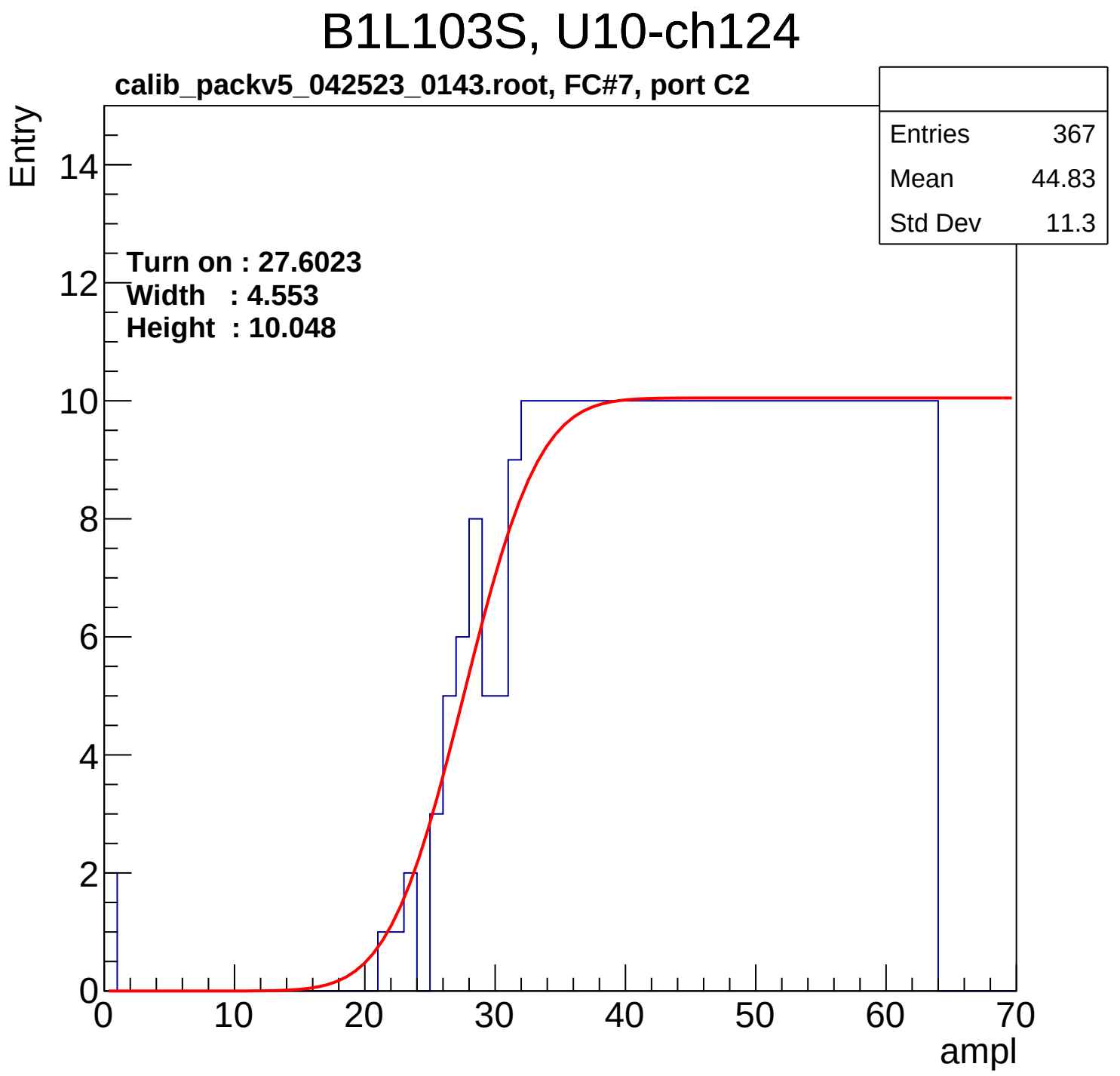
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L103S, U10-ch124
calib_packv5_042523_0143.root, FC#7, port C2
Entries 367
Mean 44.83
Std Dev 11.3
Turn on : 27.6023
Width : 4.553
Height : 10.048
Entry
ampl
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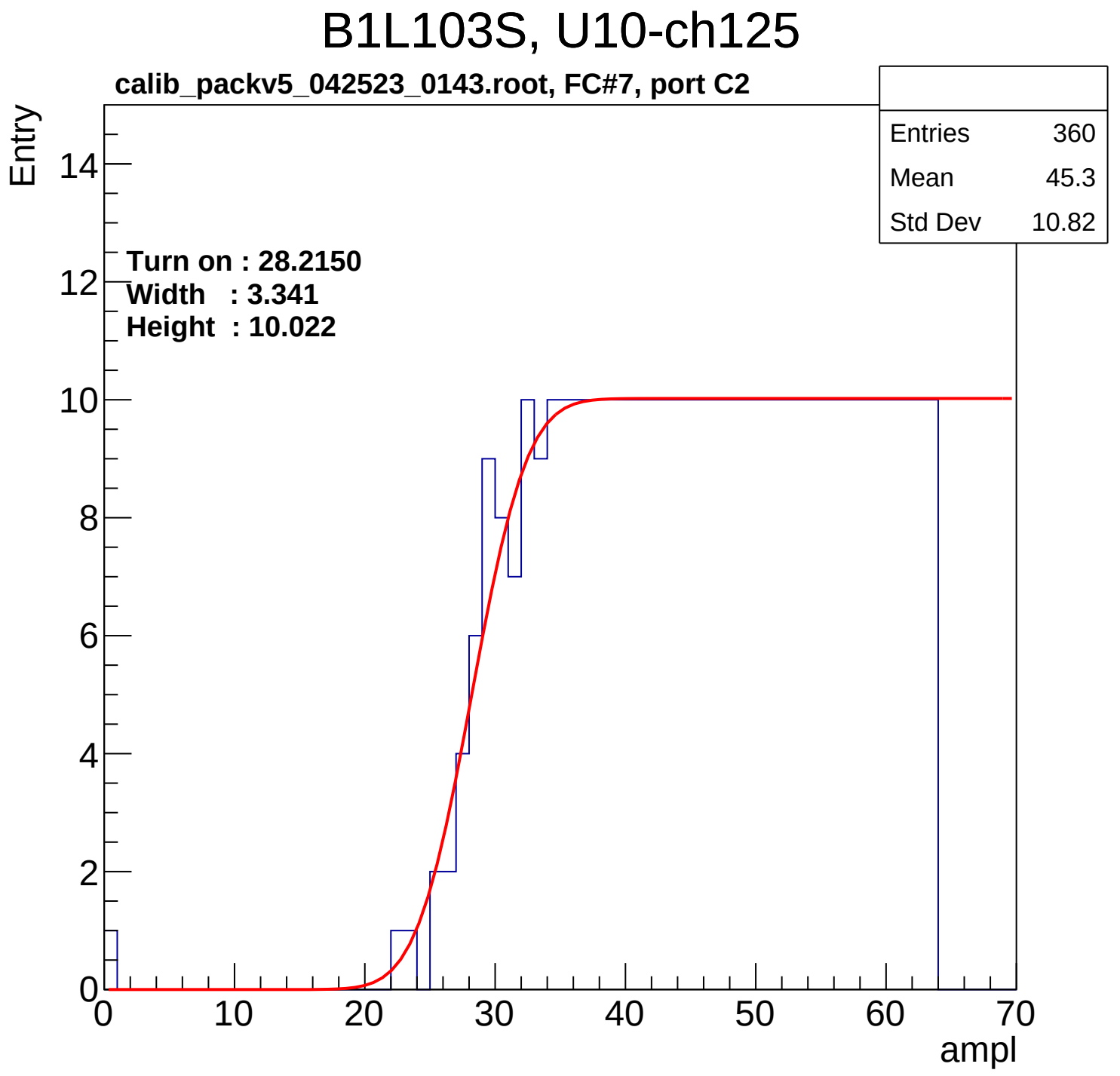
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L103S, U10-ch125
calib_packv5_042523_0143.root, FC#7, port C2
Entries 360
Mean 45.3
Std Dev 10.82
Turn on : 28.2150
Width : 3.341
Height : 10.022
Entry
ampl
0
2
4
6
8
10
12
14
0
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20
30
40
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60
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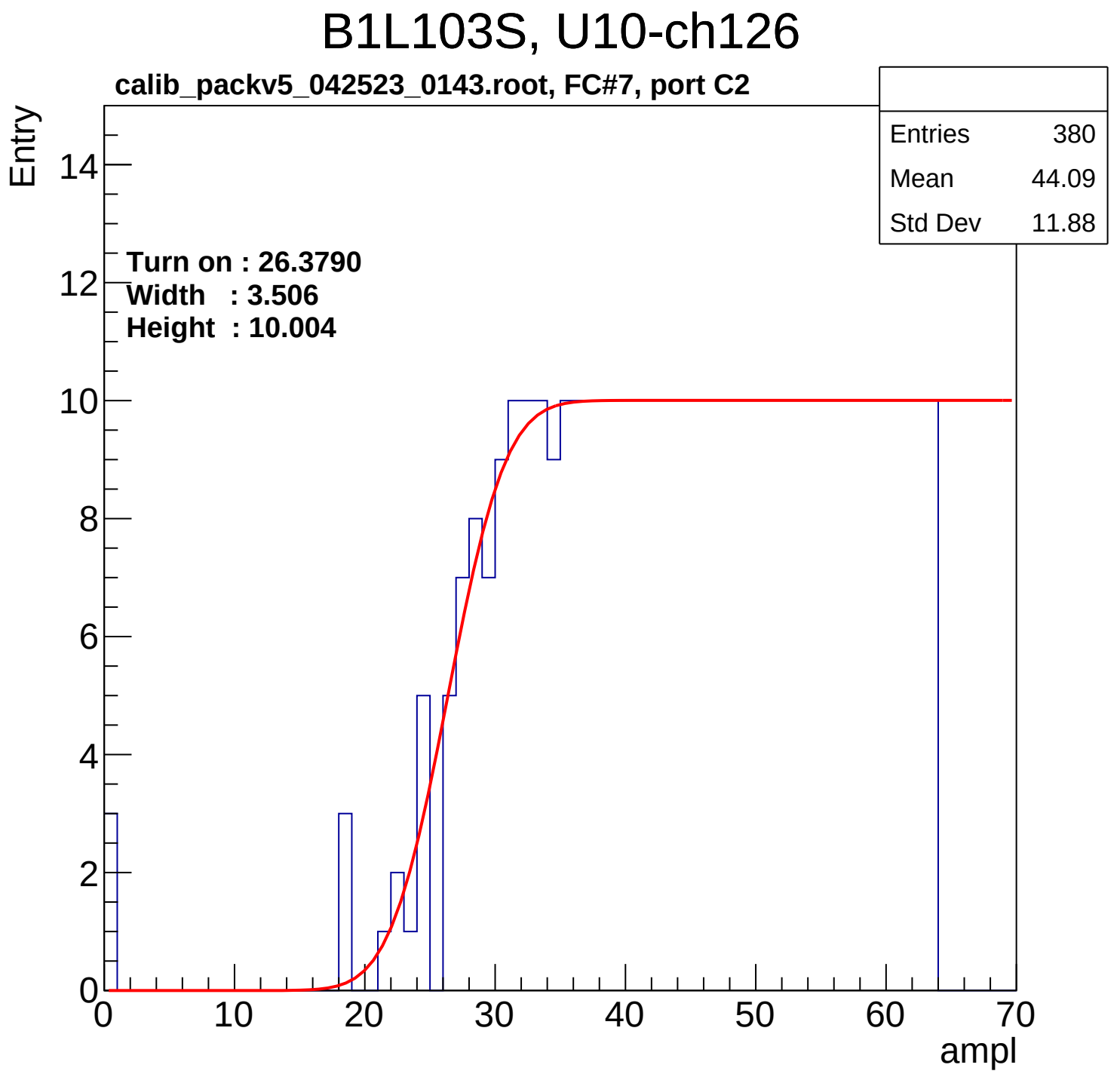
B1L103S, U10-ch126
calib_packv5_042523_0143.root, FC#7, port C2
Entries 380
Mean 44.09
Std Dev 11.88
Turn on : 26.3790
Width : 3.506
Height : 10.004
Entry
ampl
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2
4
6
8
10
12
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0
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20
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40
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60
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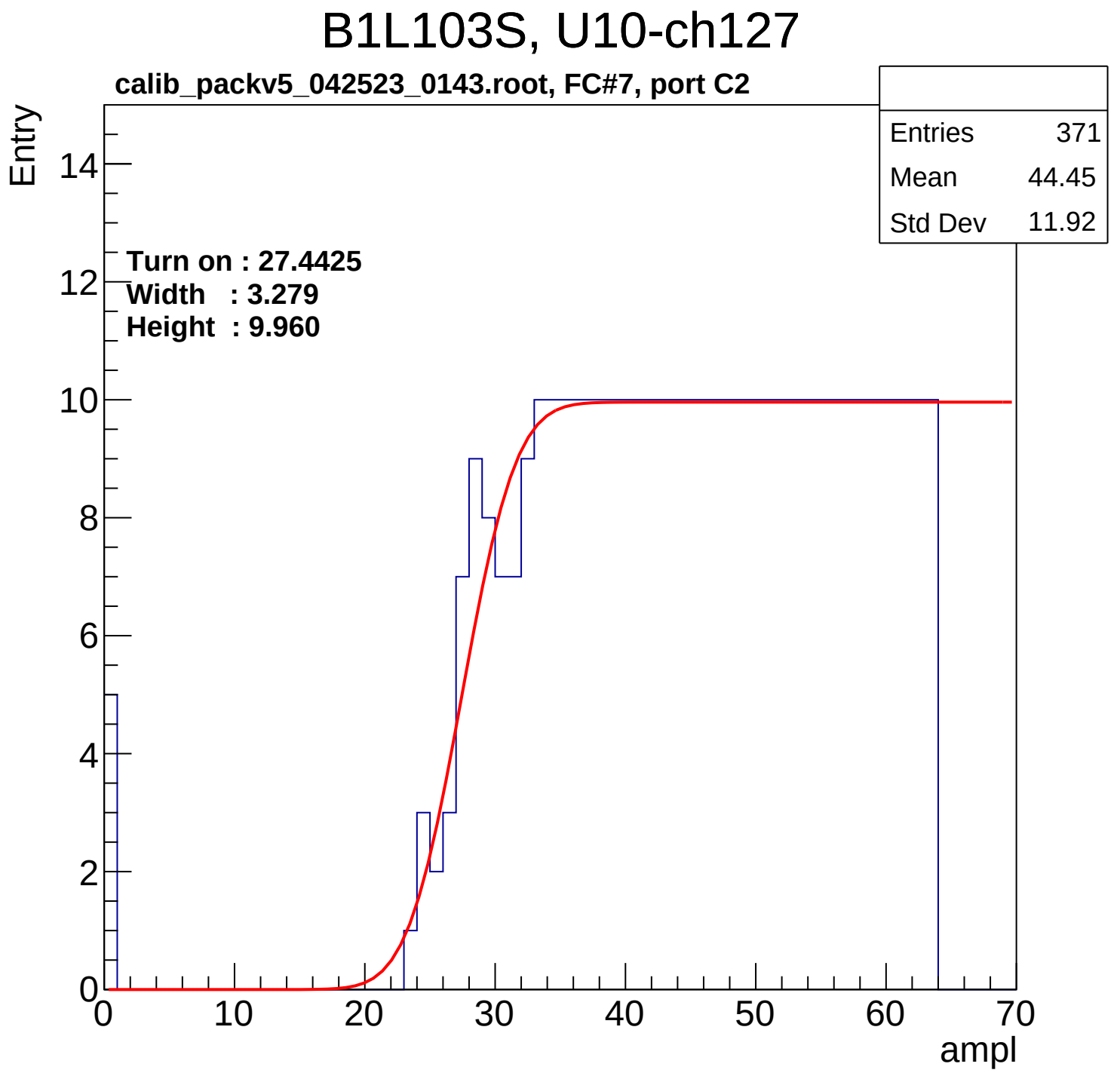
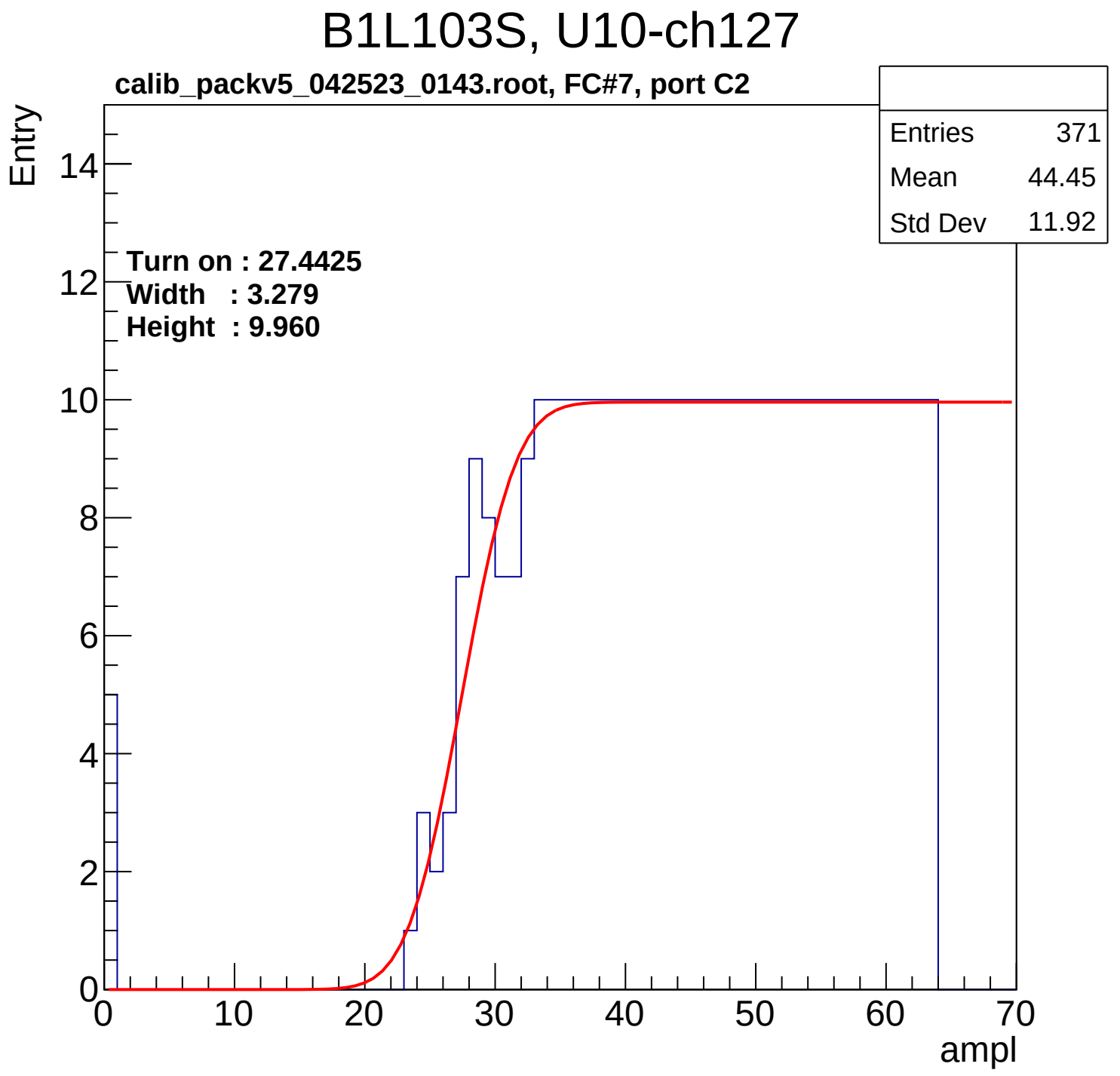

B1L103S, U10-ch127
calib_packv5_042523_0143.root, FC#7, port C2
Entries 371
Mean 44.45
Std Dev 11.92
Turn on : 27.4425
Width : 3.279
Height : 9.960
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L103S, U10-ch127
calib_packv5_042523_0143.root, FC#7, port C2
Entries 371
Mean 44.45
Std Dev 11.92
Turn on : 27.4425
Width : 3.279
Height : 9.960
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70