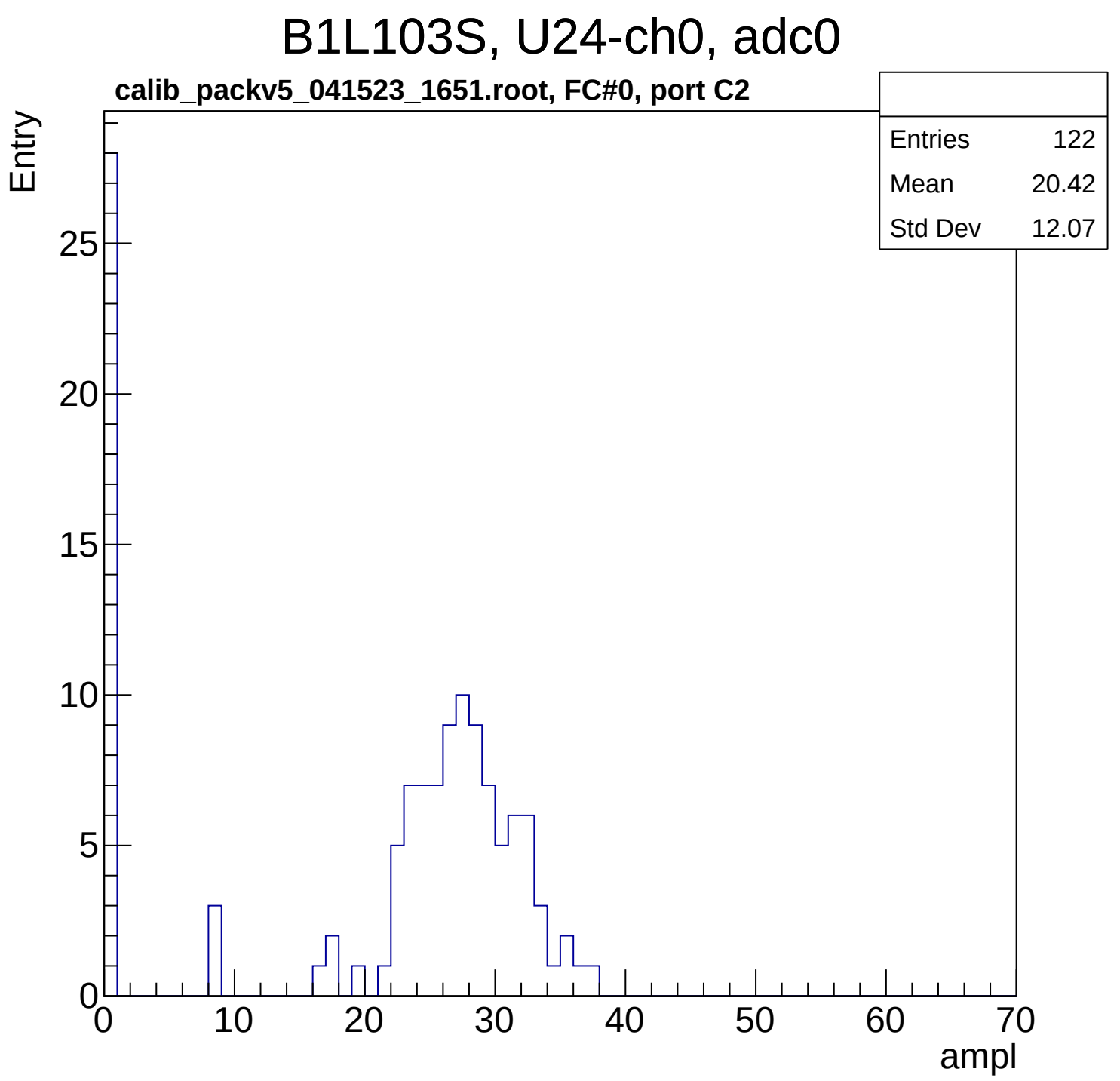
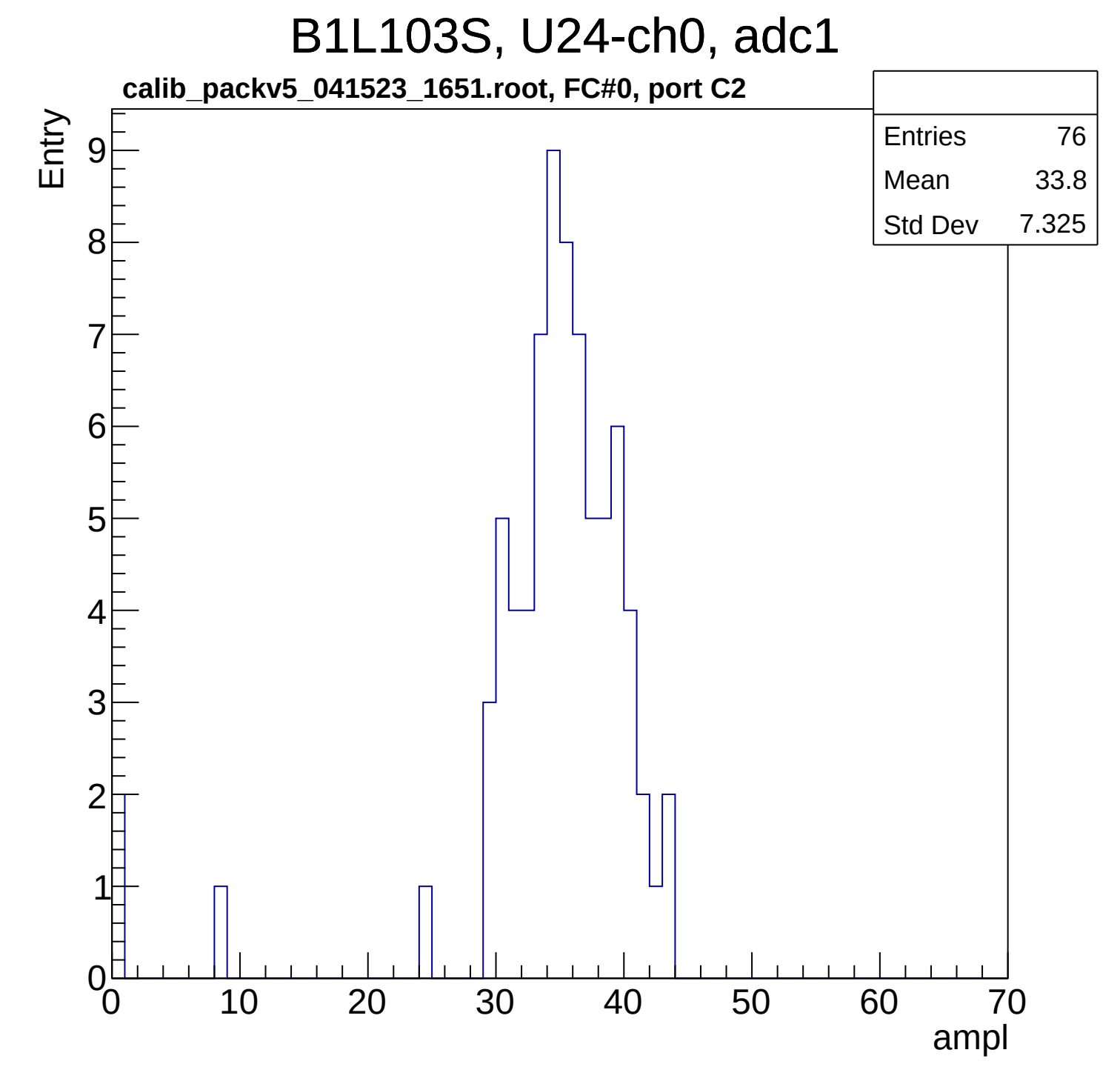

B1L103S, U24-ch0, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 122
Mean 20.42
Std Dev 12.07
Entry
0
5
10
15
20
25
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch0, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 33.8
Std Dev 7.325
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
50
60
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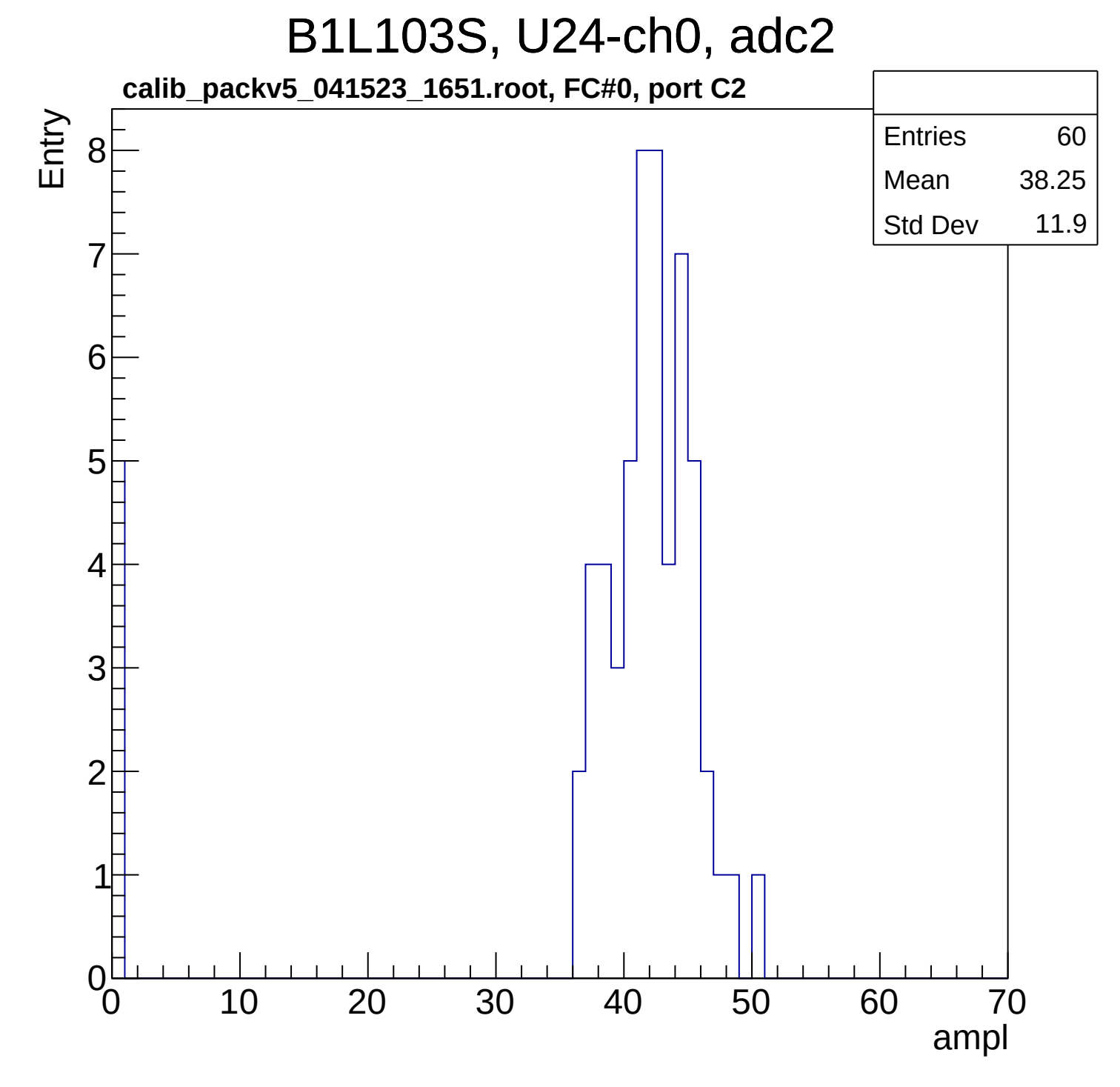
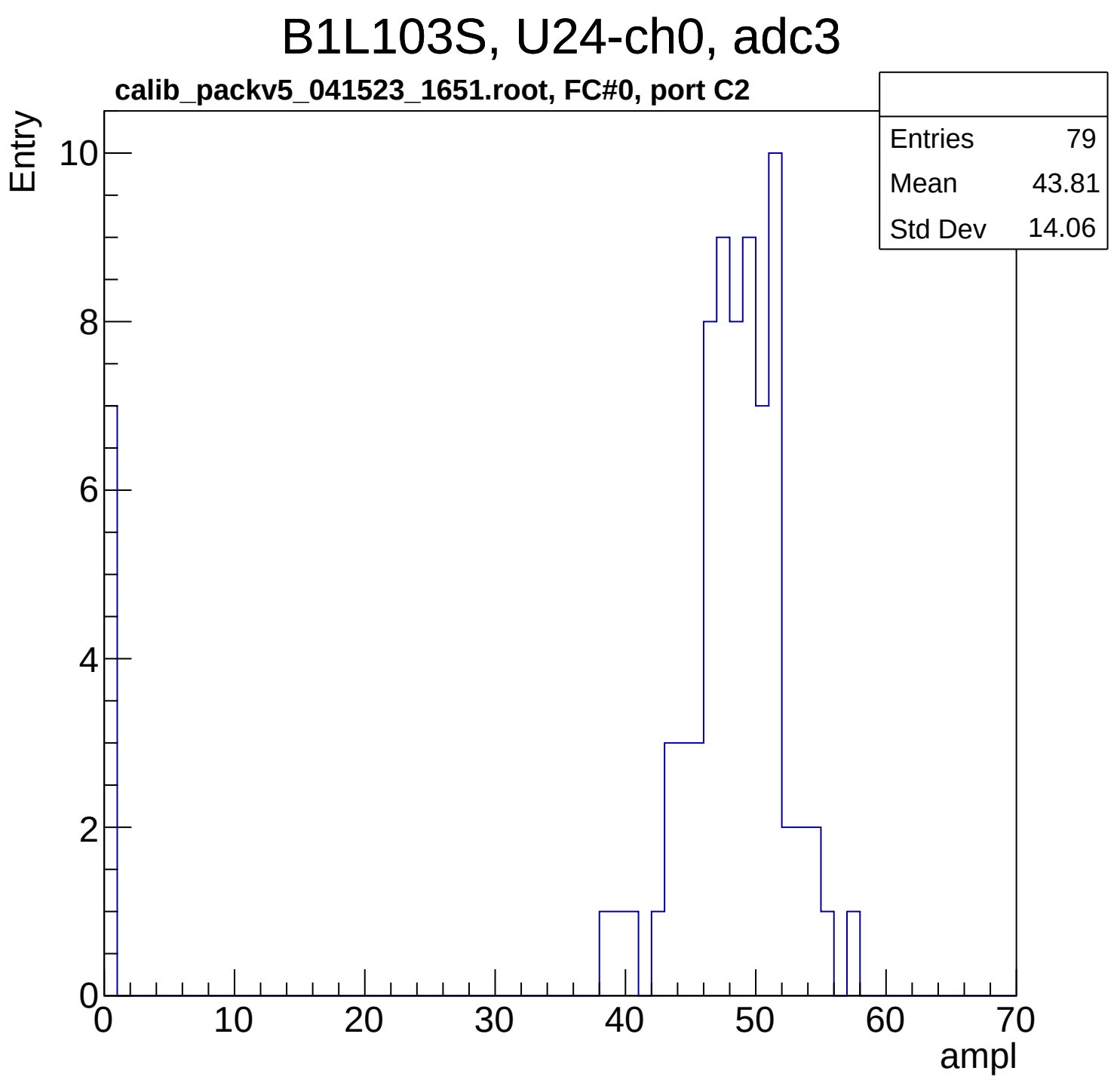
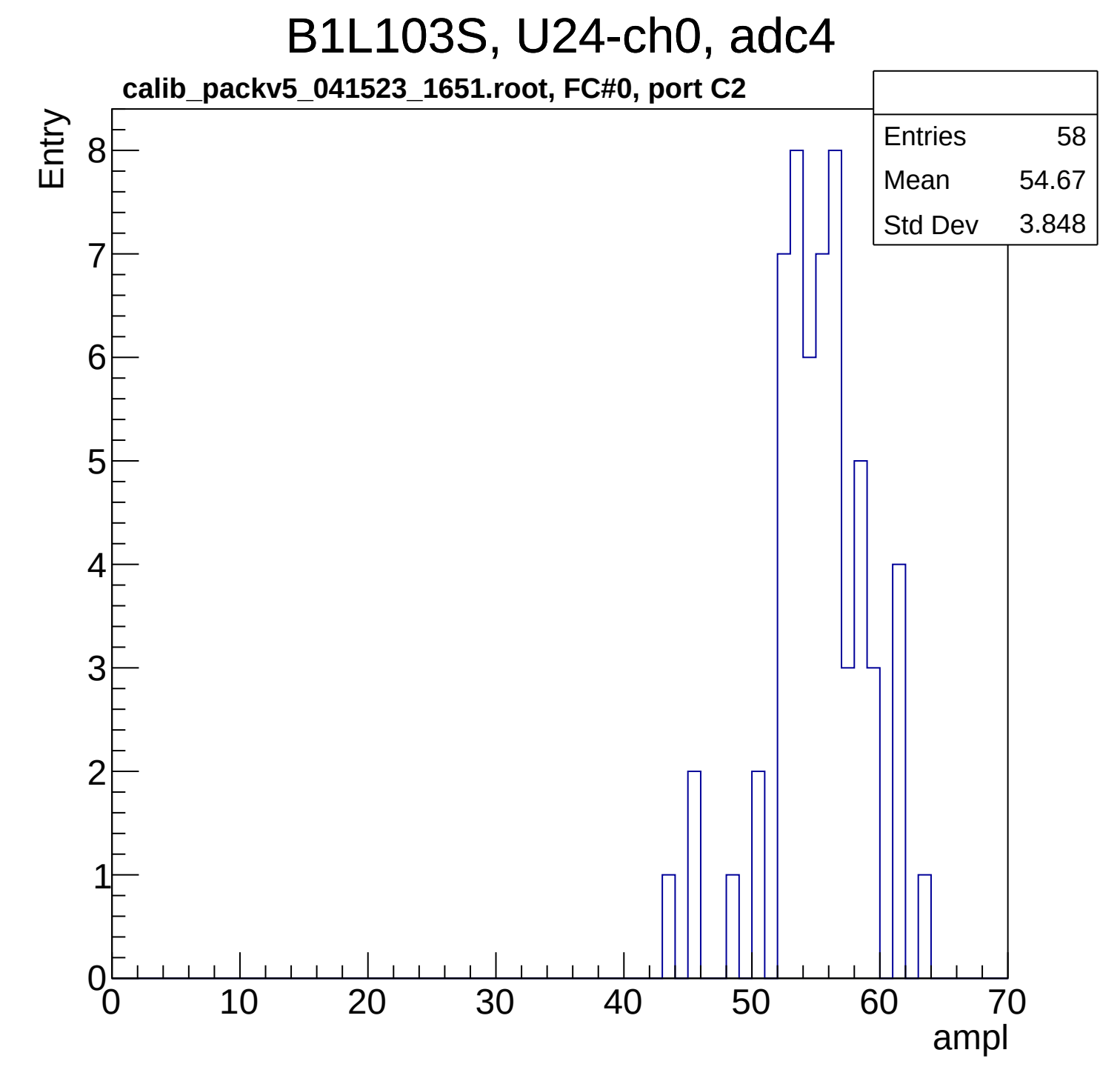

B1L103S, U24-ch0, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 38.25
Std Dev 11.9
Entry
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch0, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 43.81
Std Dev 14.06
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U24-ch0, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 54.67
Std Dev 3.848
Entry
ampl
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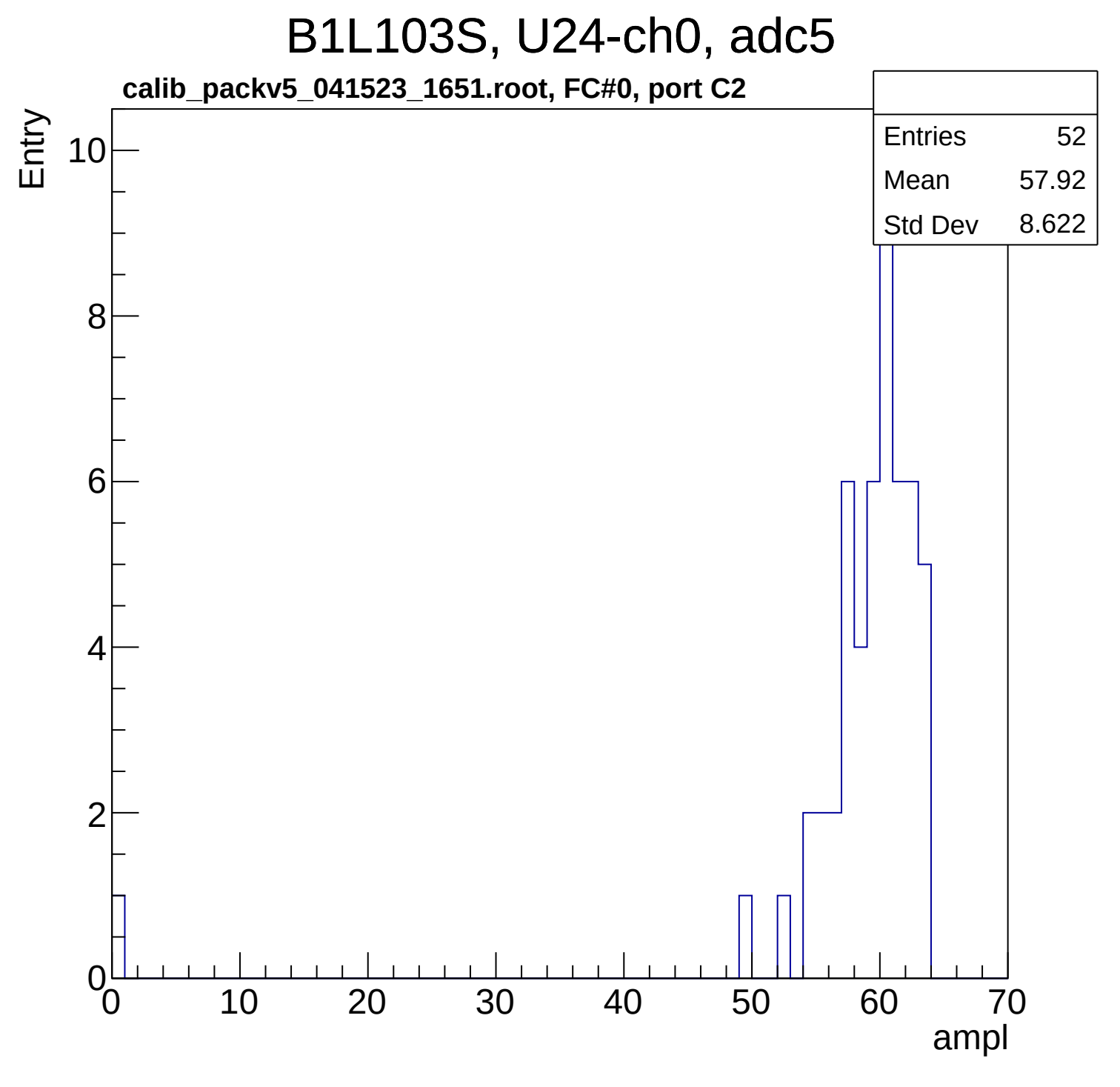
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U24-ch0, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 57.92
Std Dev 8.622
Entry
ampl
0
2
4
6
8
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0
10
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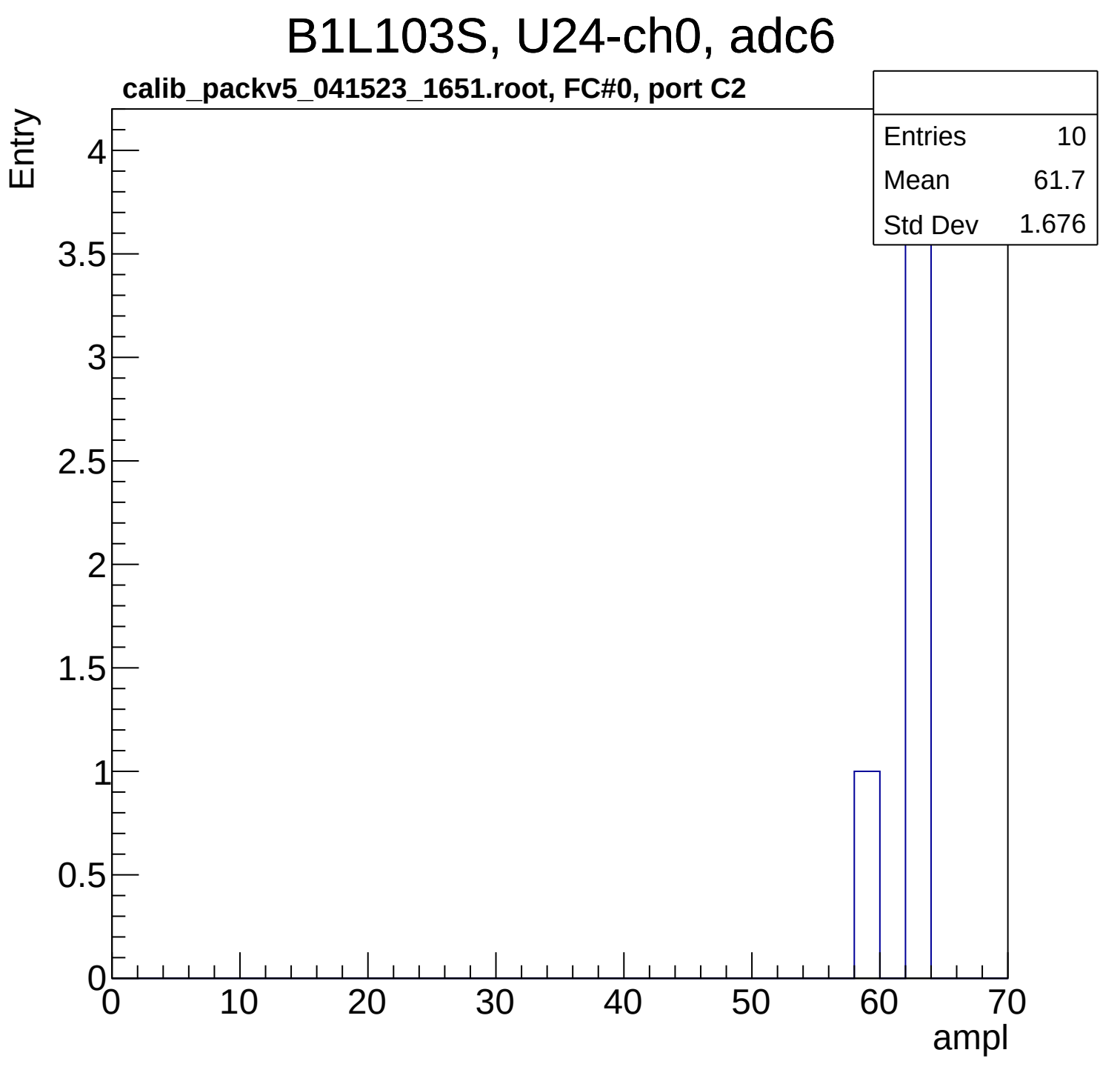
30
40
50
60
70


B1L103S, U24-ch0, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 61.7
Std Dev 1.676
Entry
ampl
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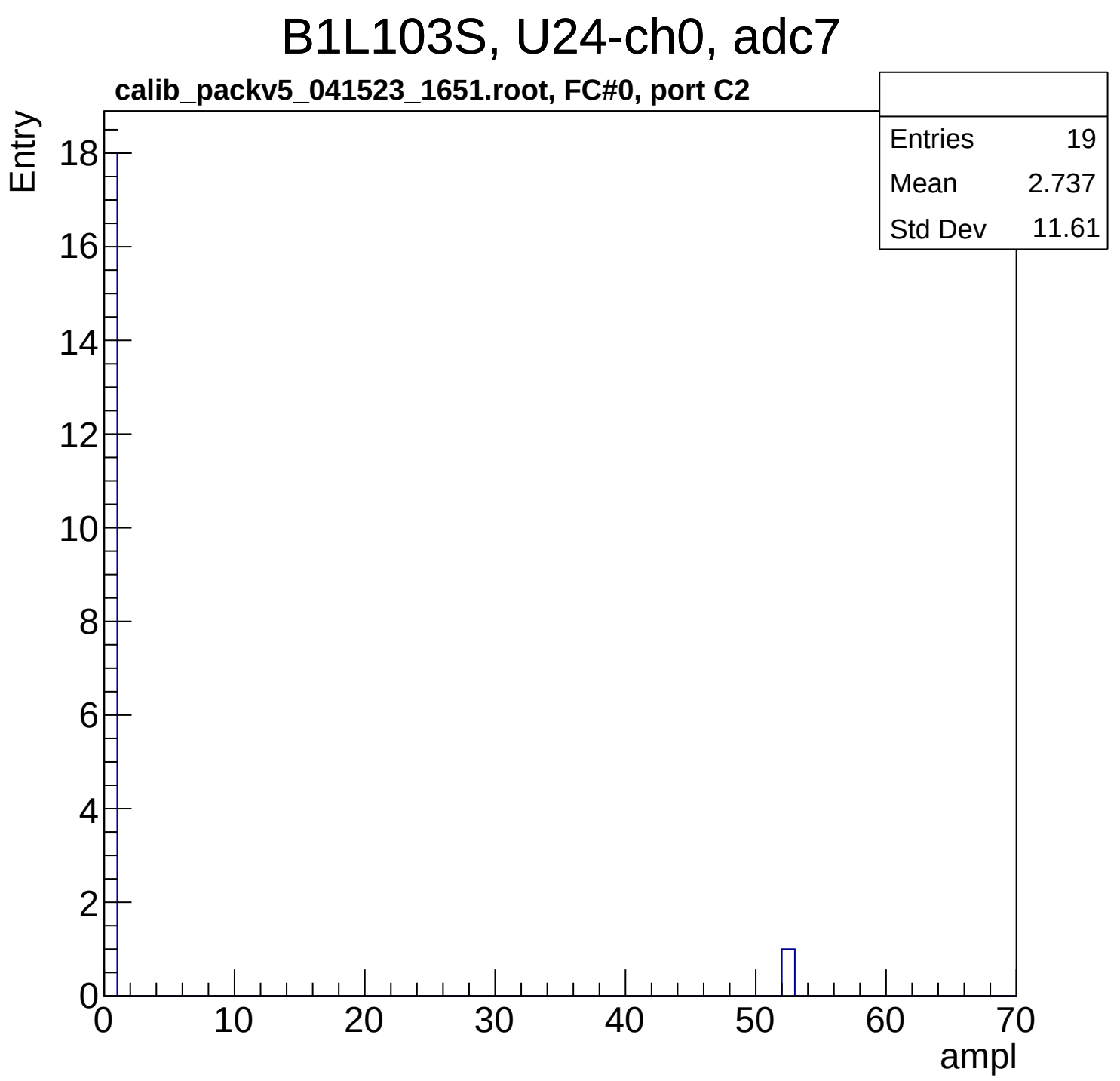
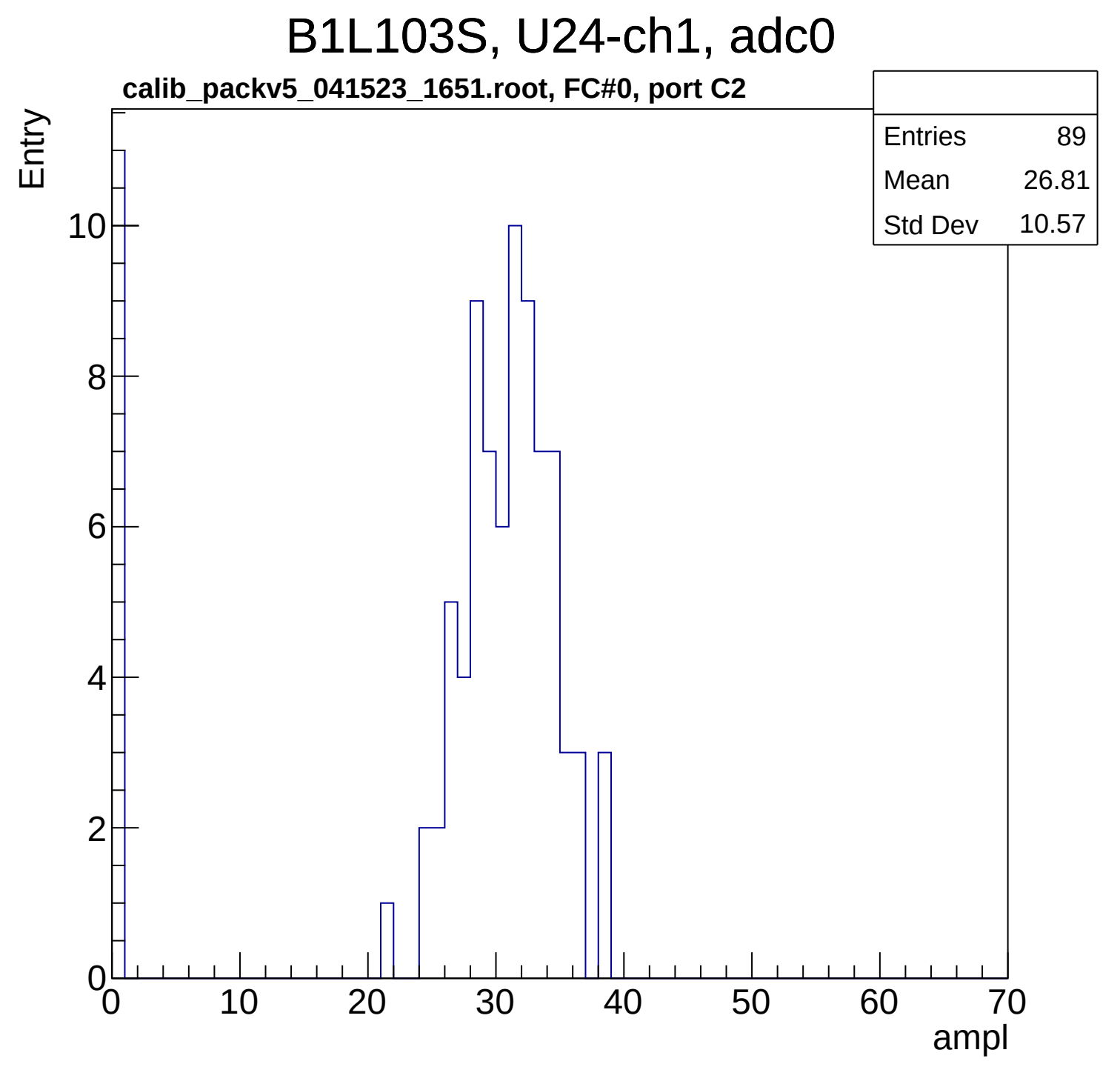
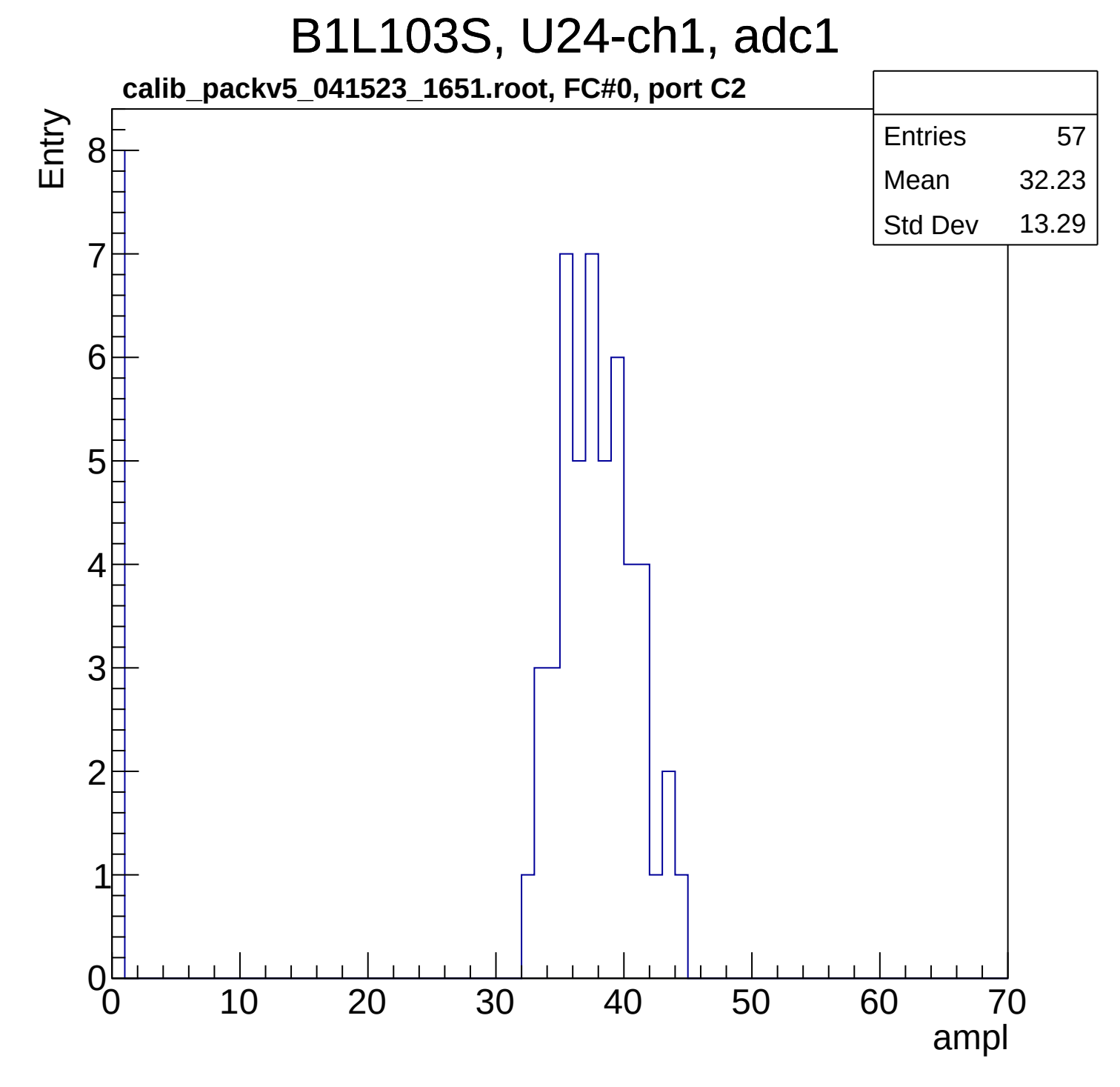
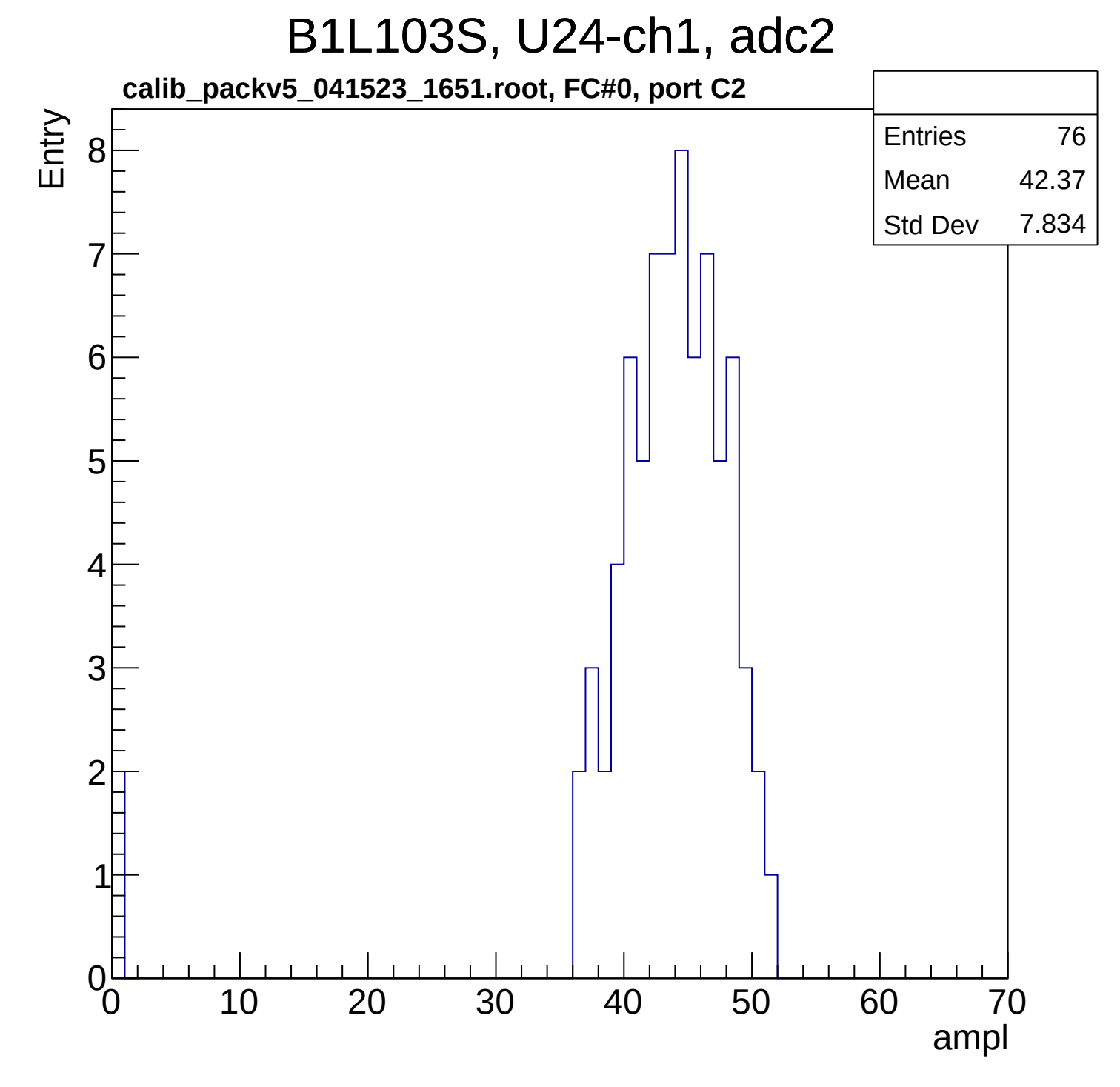
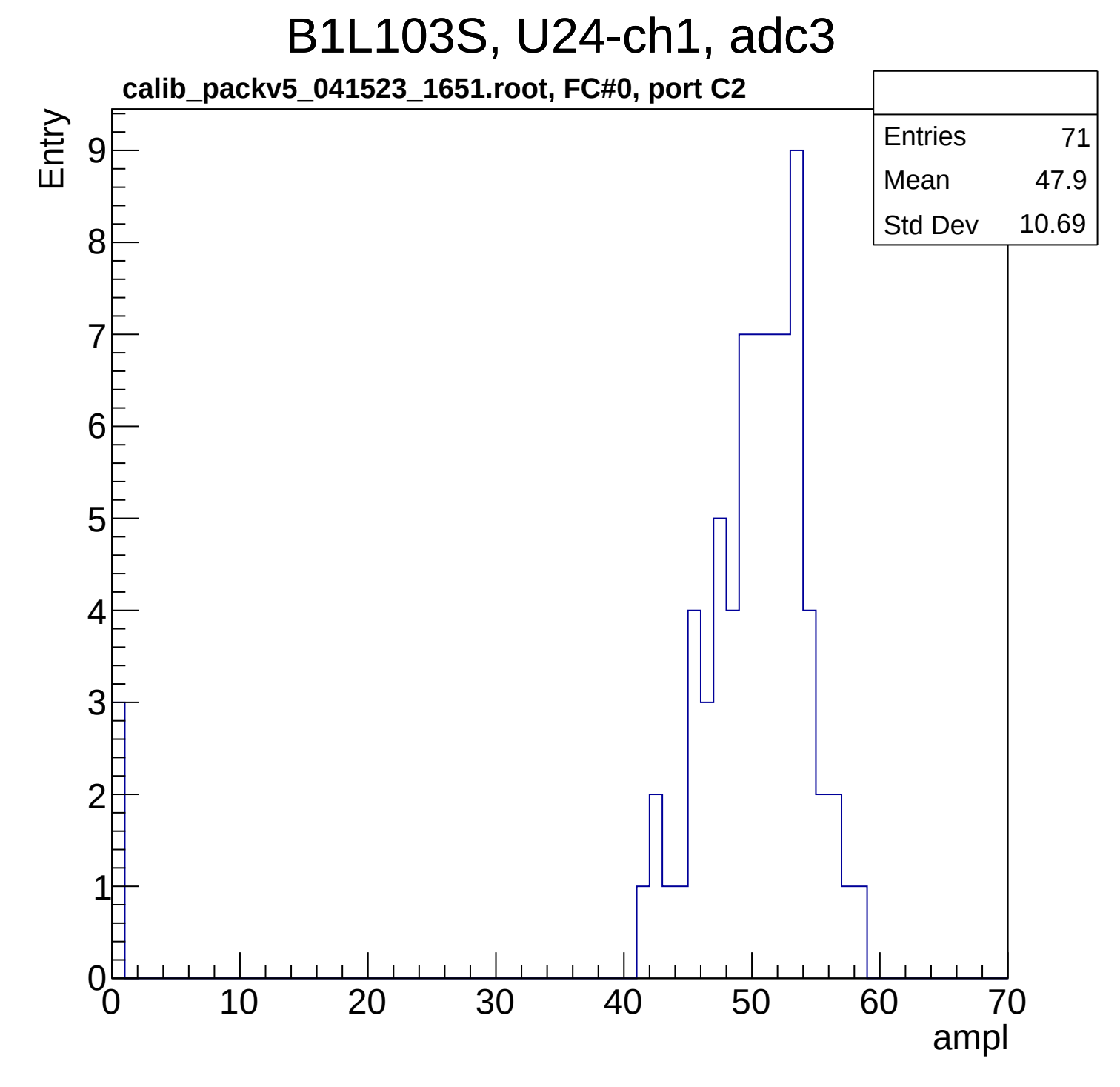
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

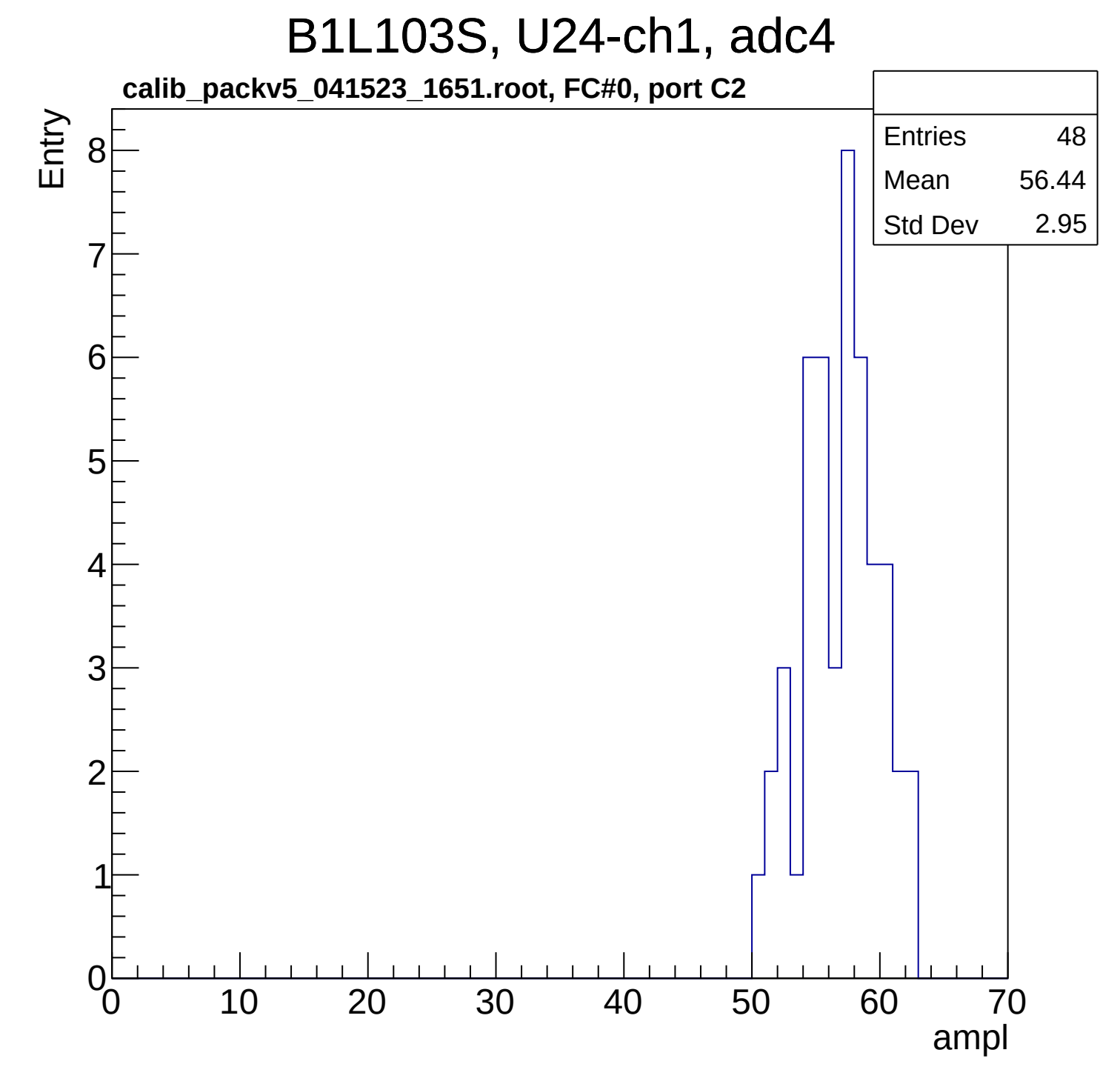

B1L103S, U24-ch0, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 2.737
Std Dev 11.61
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

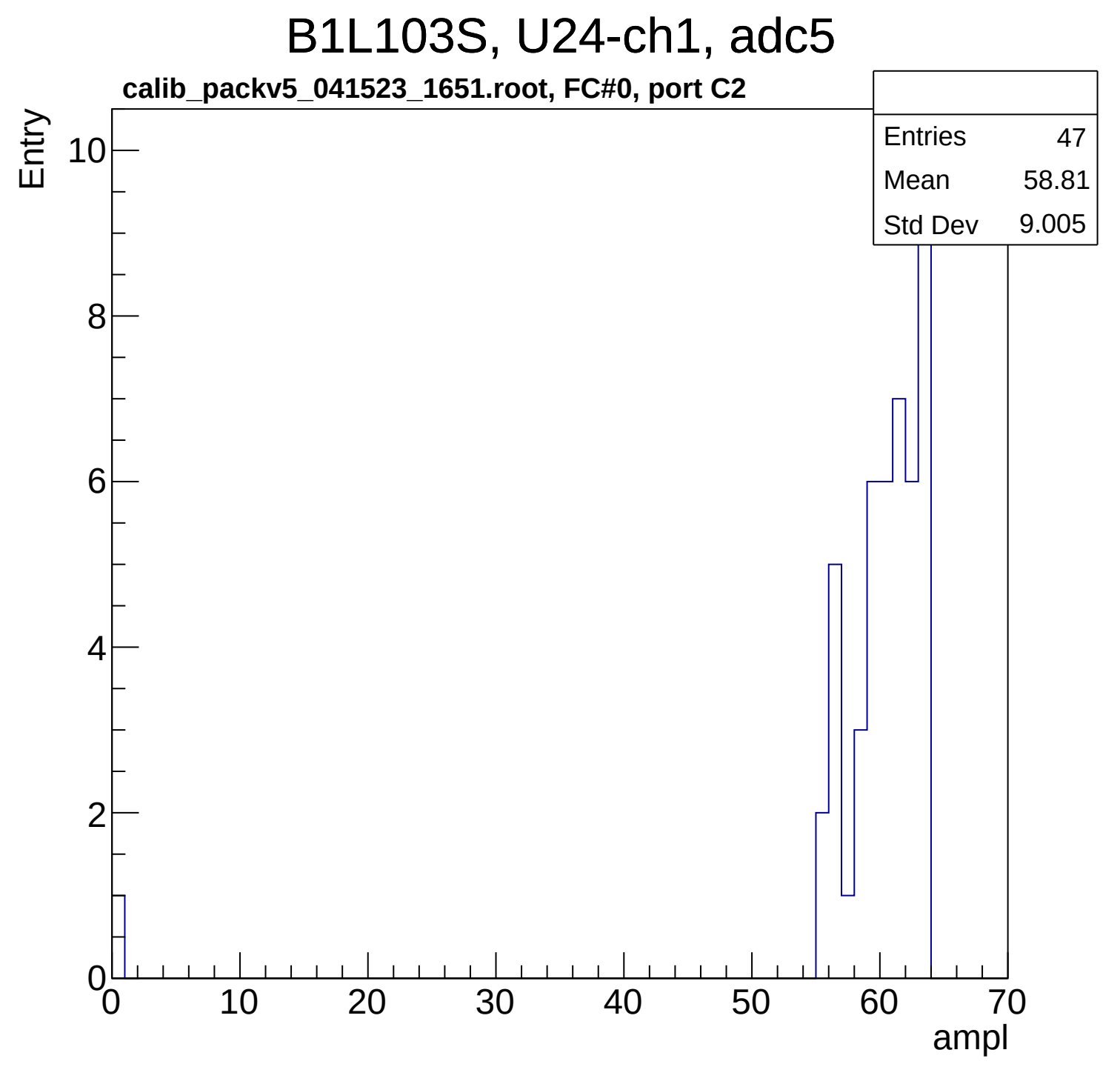

B1L103S, U24-ch1, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 89
Mean 26.81
Std Dev 10.57
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

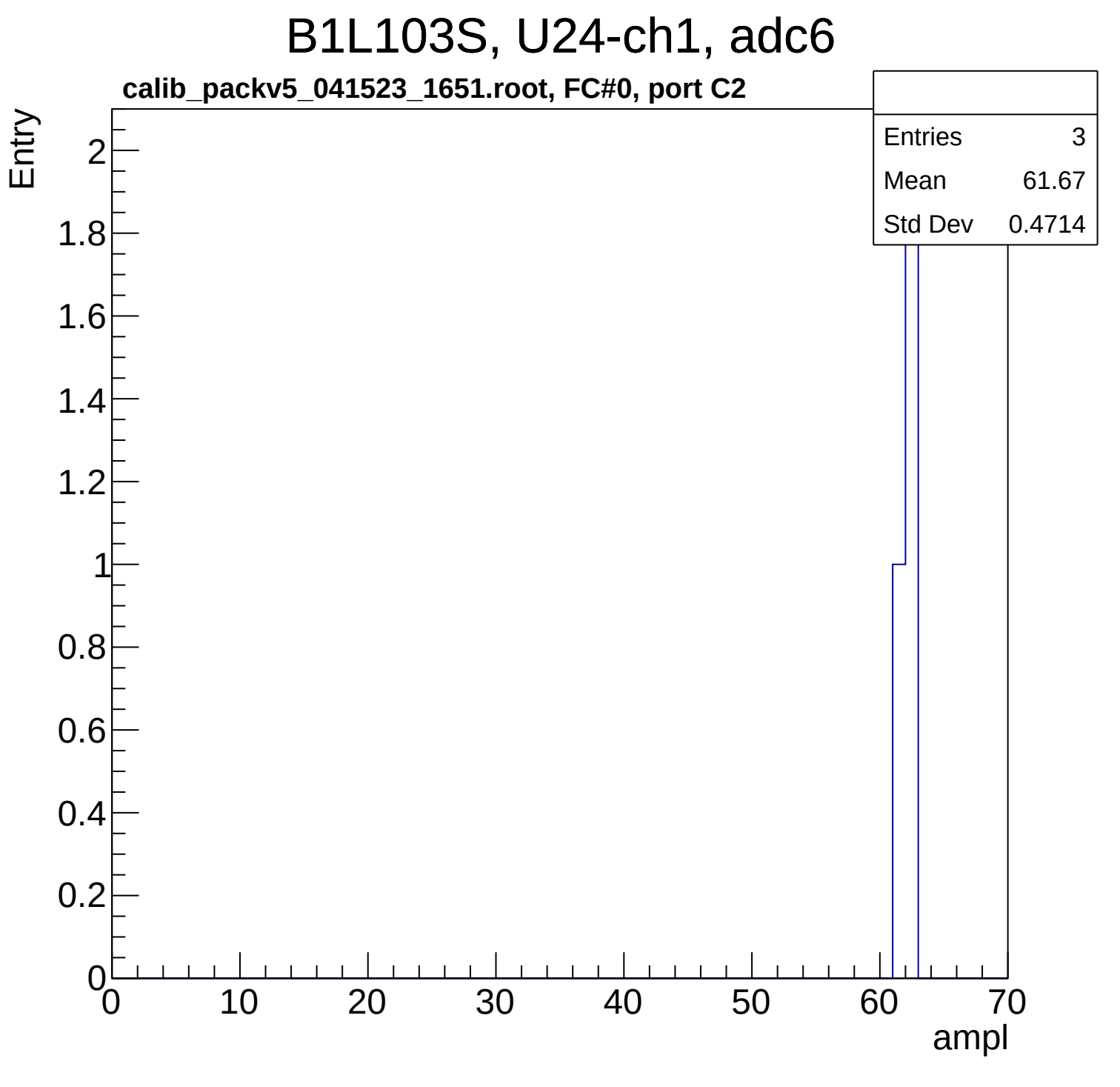

B1L103S, U24-ch1, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 32.23
Std Dev 13.29
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

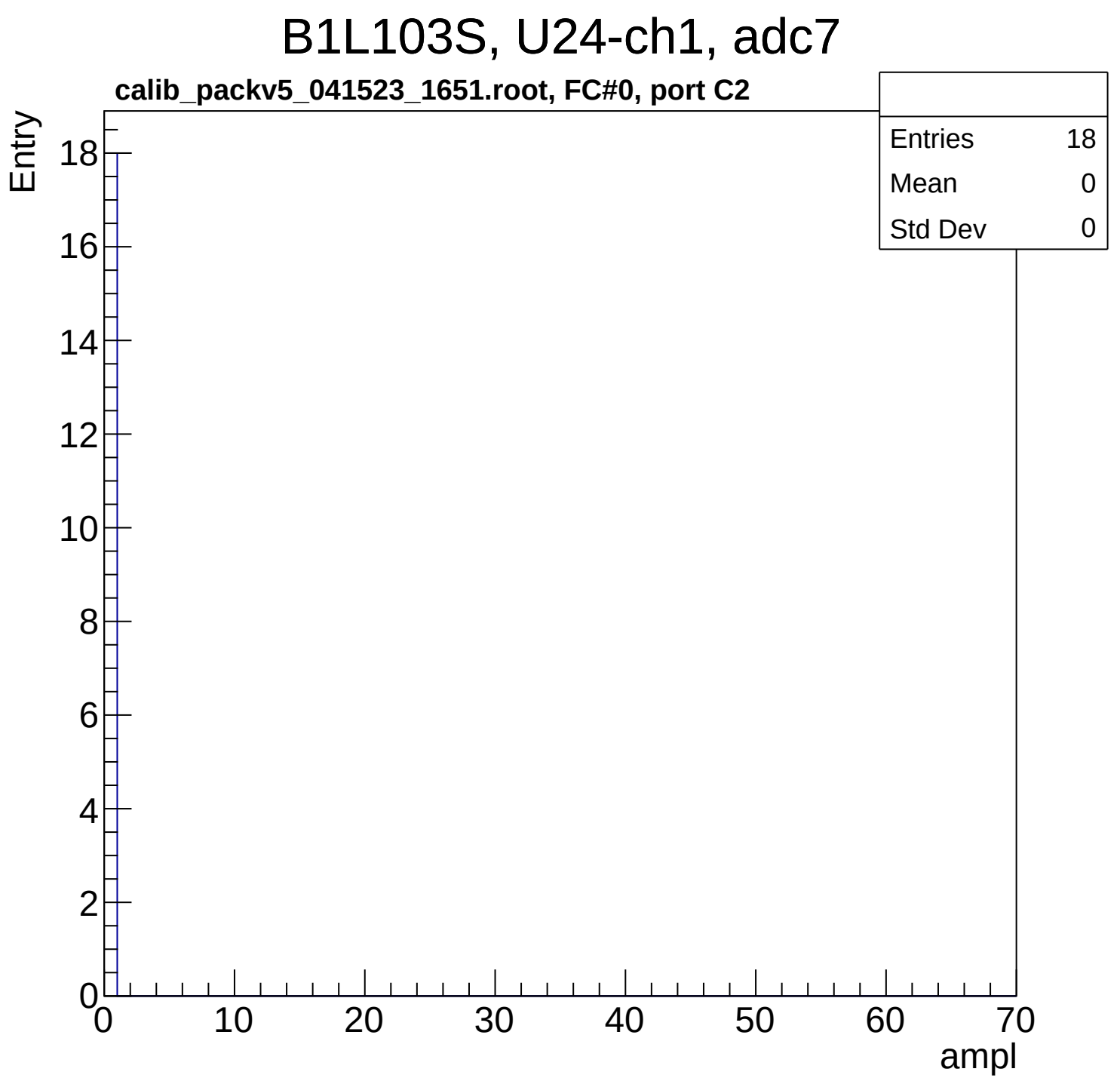

B1L103S, U24-ch1, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 42.37
Std Dev 7.834
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

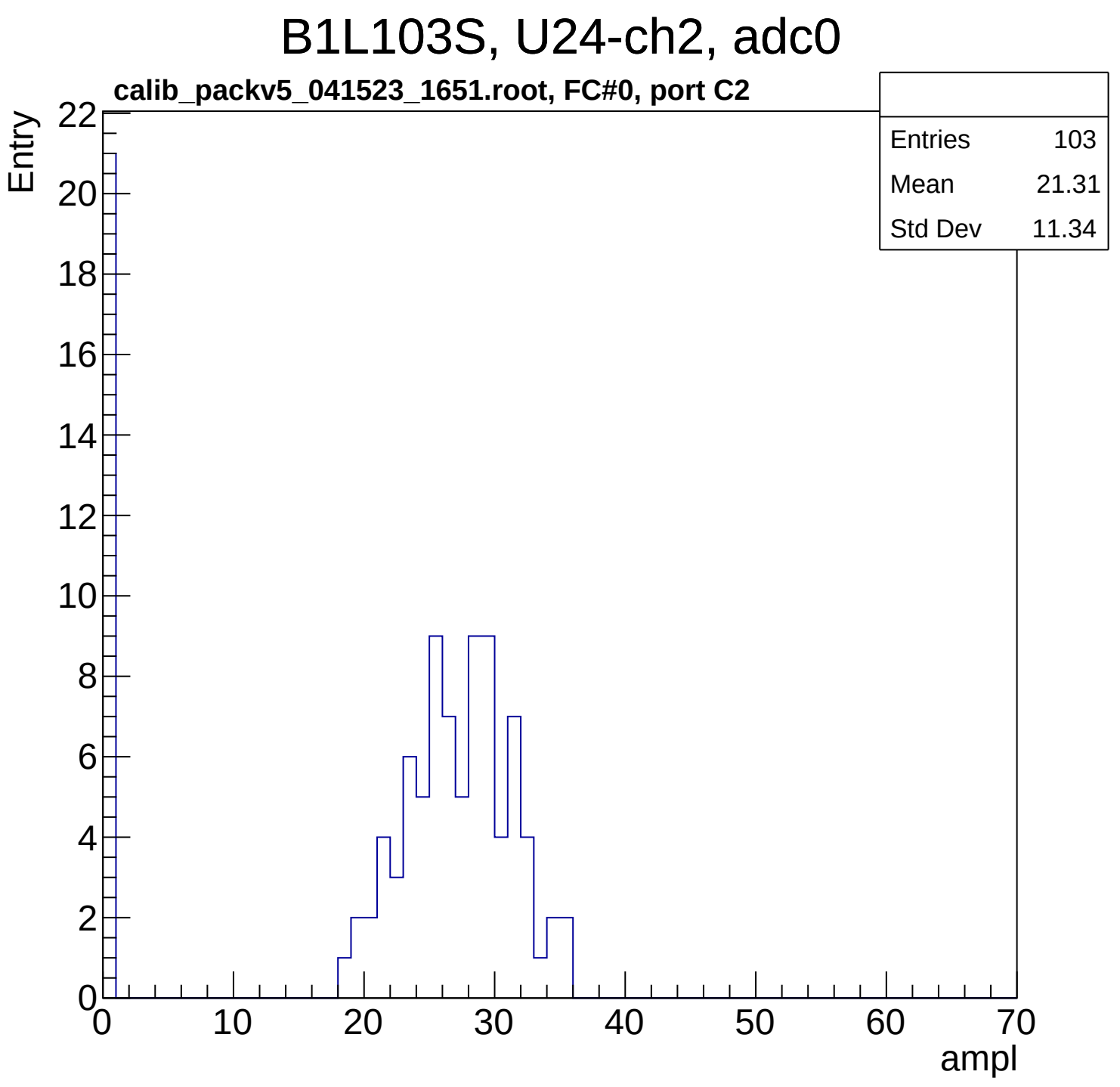

B1L103S, U24-ch1, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 47.9
Std Dev 10.69
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

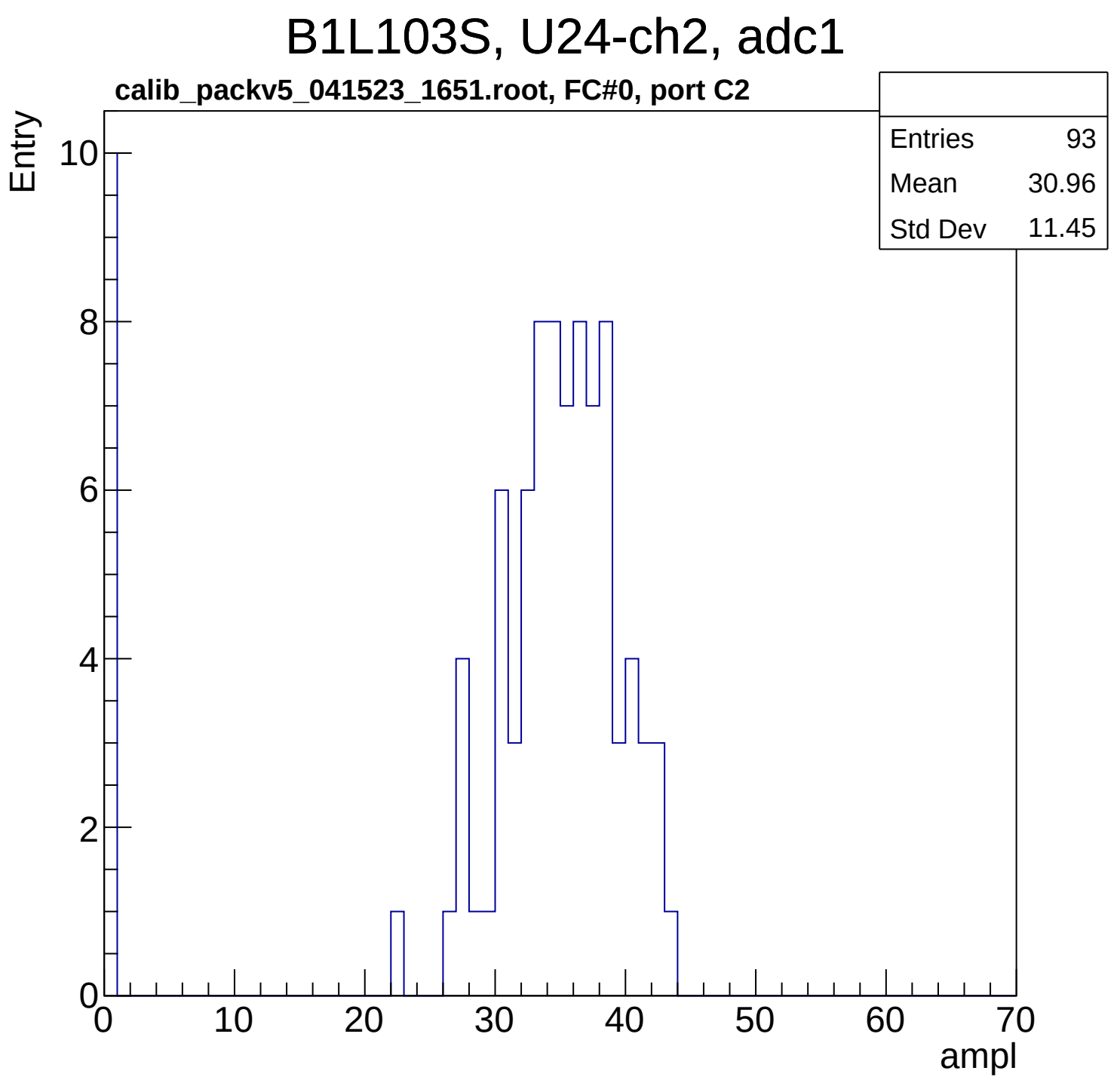

B1L103S, U24-ch1, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 56.44
Std Dev 2.95
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

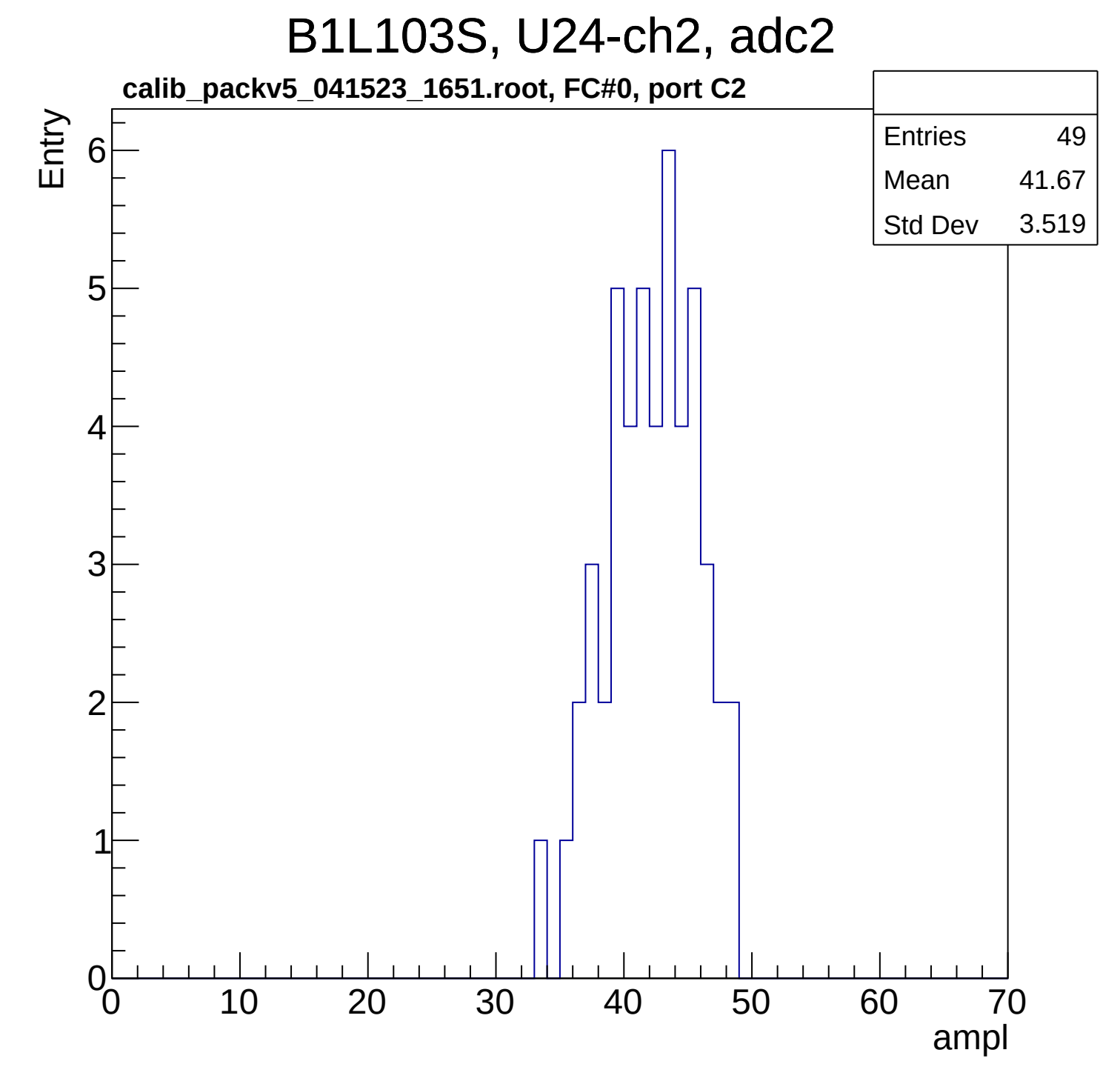

B1L103S, U24-ch1, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 58.81
Std Dev 9.005
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

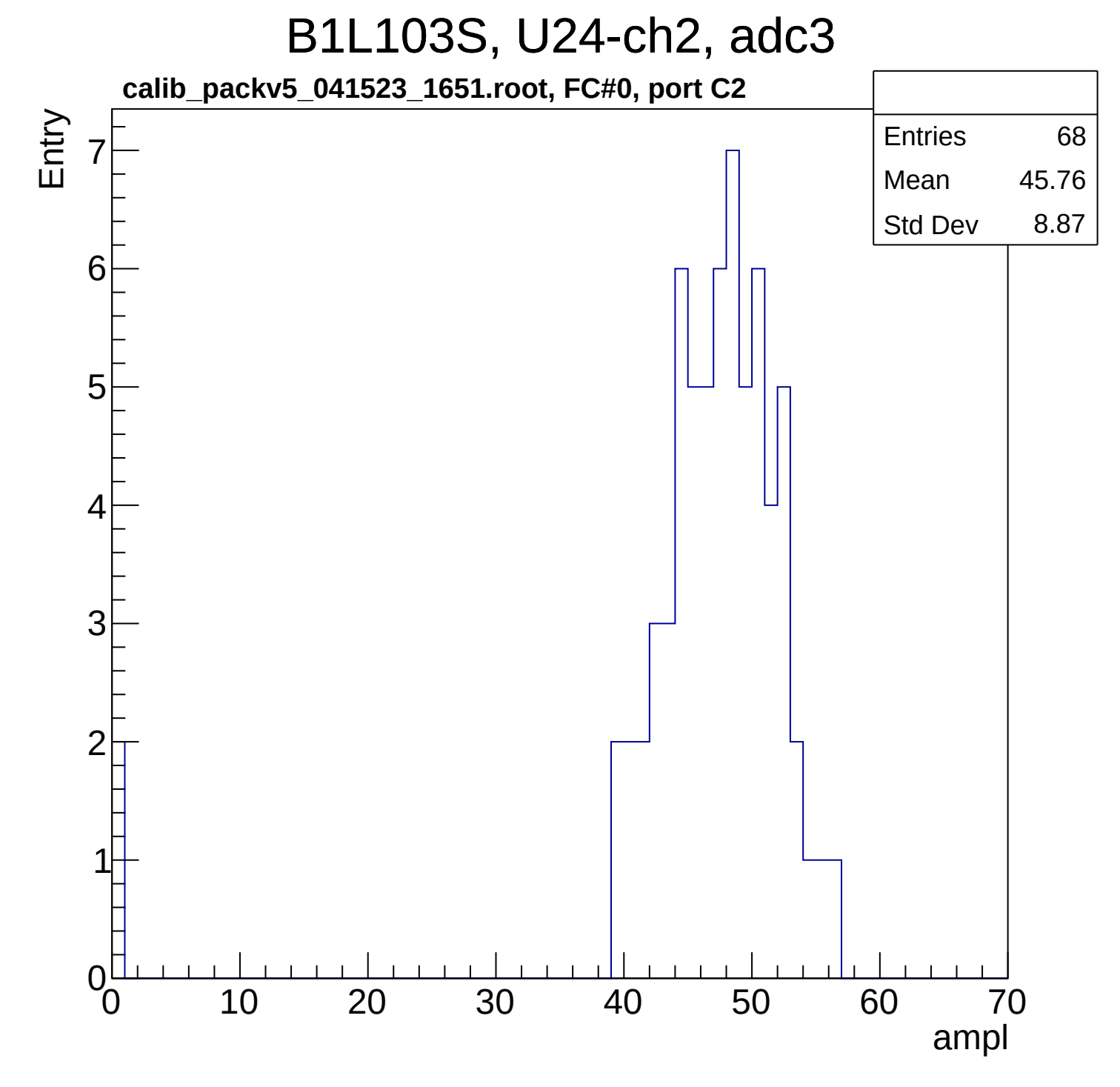

B1L103S, U24-ch1, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 3
Mean 61.67
Std Dev 0.4714
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

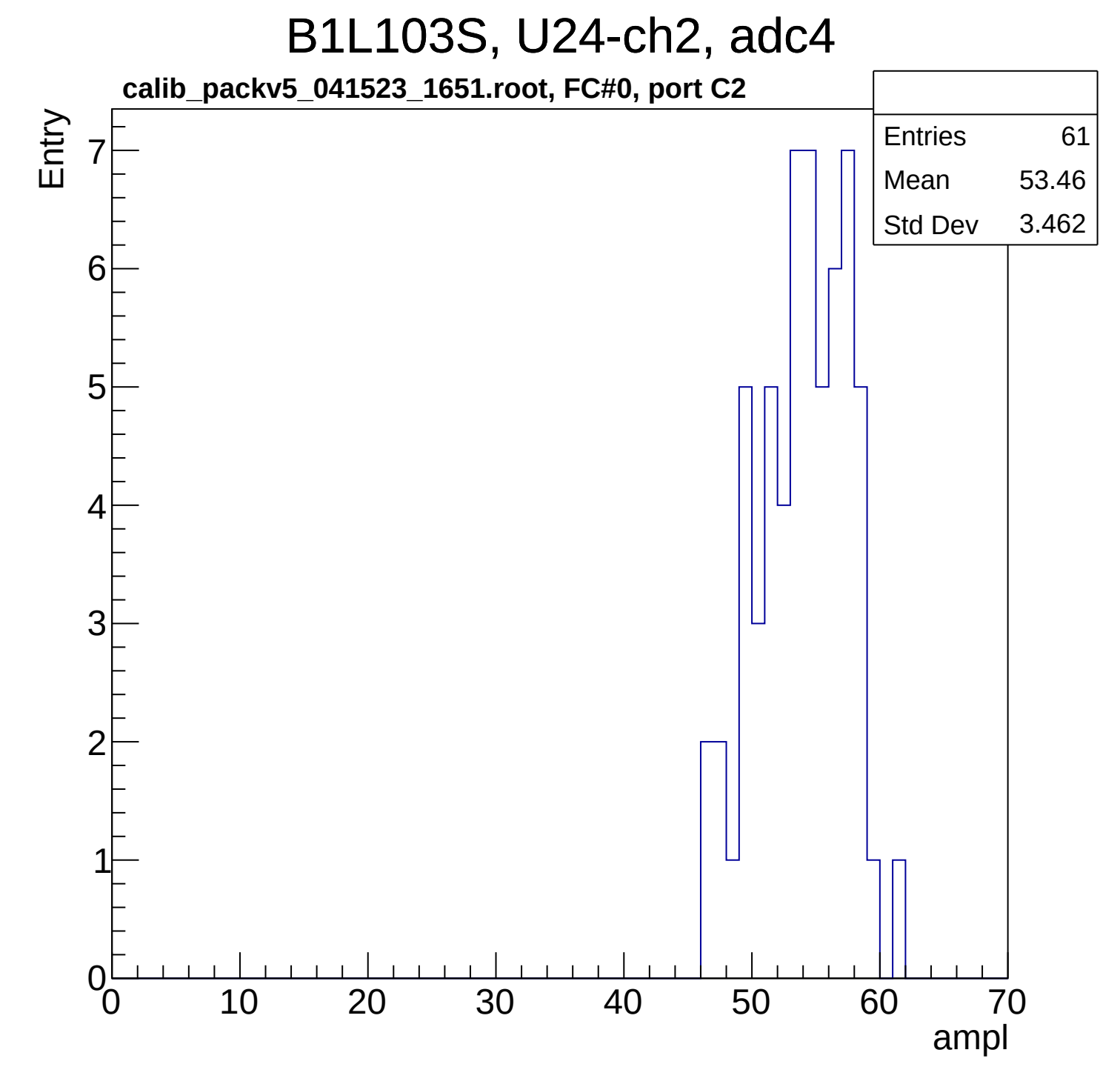

B1L103S, U24-ch1, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

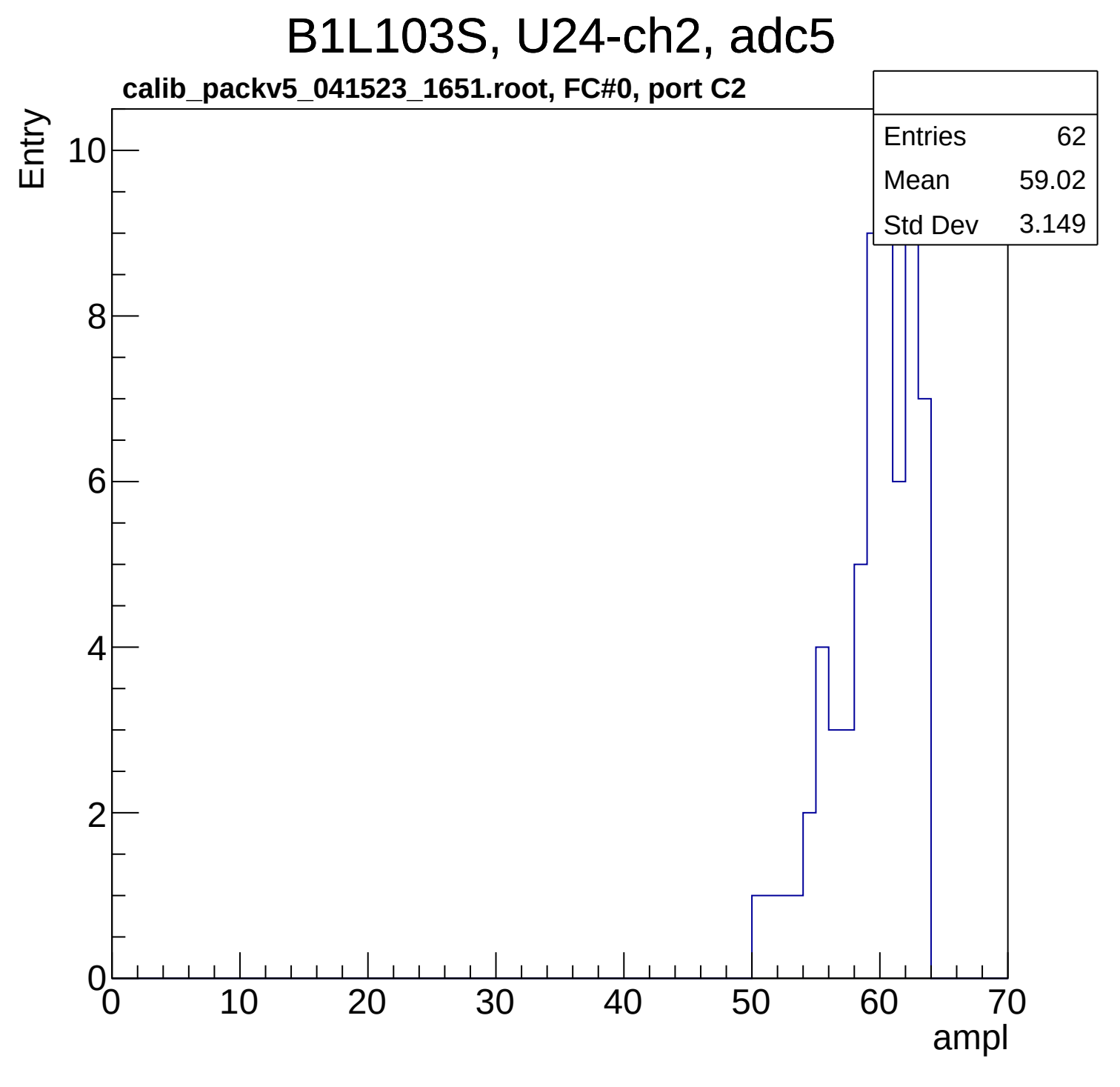

B1L103S, U24-ch2, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 103
Mean 21.31
Std Dev 11.34
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
22
0
10
20
30
40
50
60
70

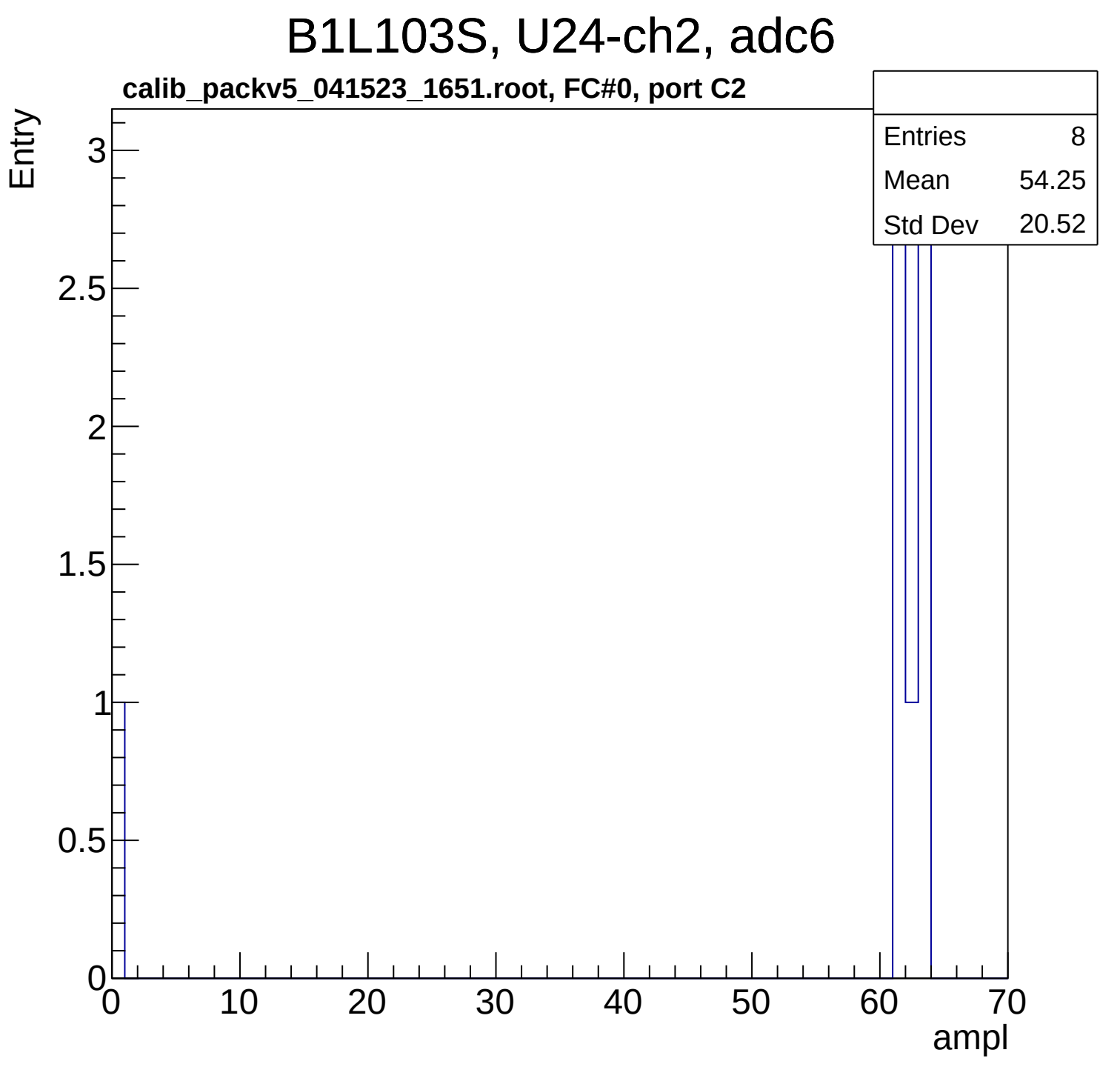

B1L103S, U24-ch2, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 93
Mean 30.96
Std Dev 11.45
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch2, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 41.67
Std Dev 3.519
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U24-ch2, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 45.76
Std Dev 8.87
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U24-ch2, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 53.46
Std Dev 3.462
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U24-ch2, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 59.02
Std Dev 3.149
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U24-ch2, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 54.25
Std Dev 20.52
Entry
ampl
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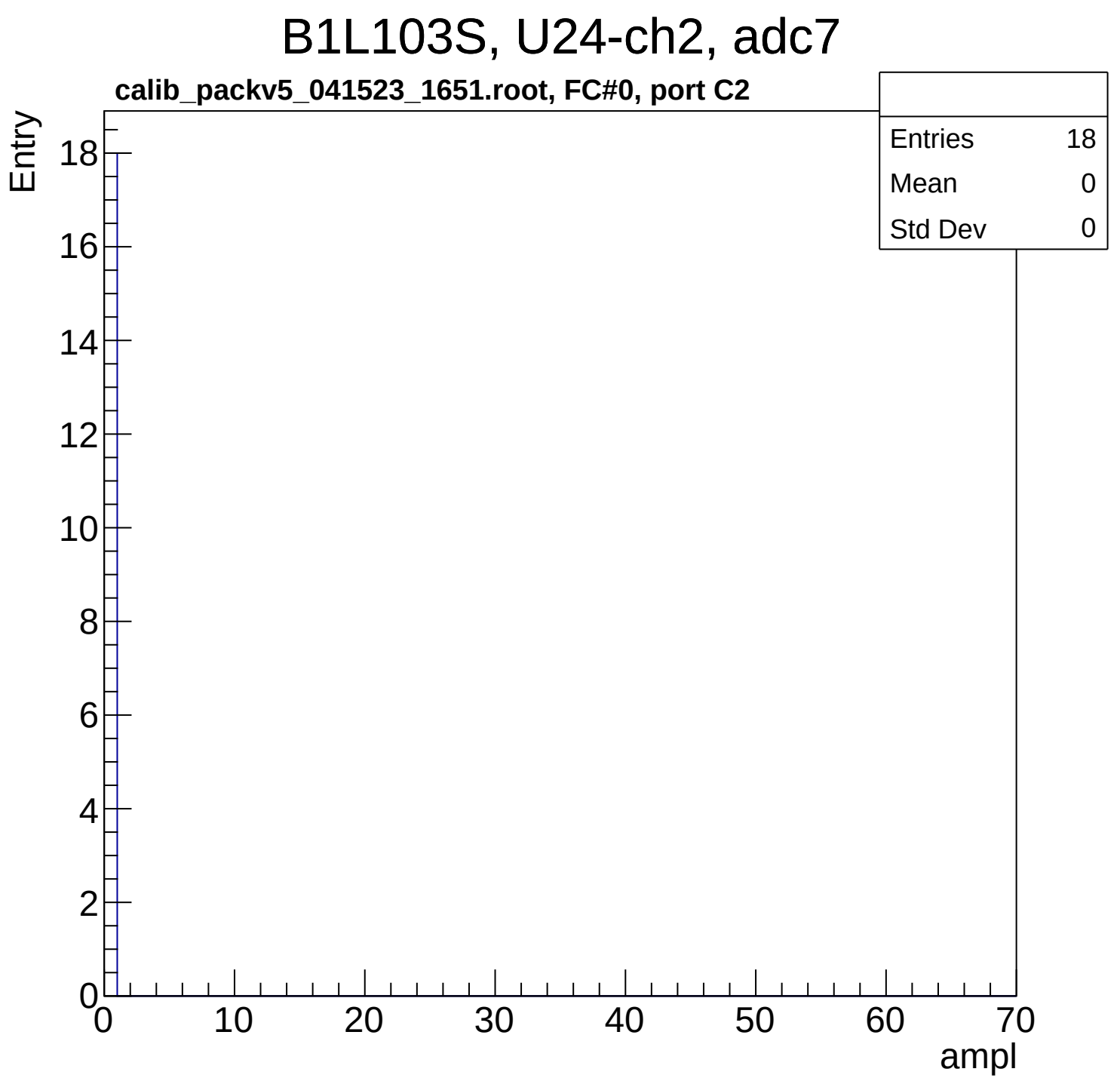
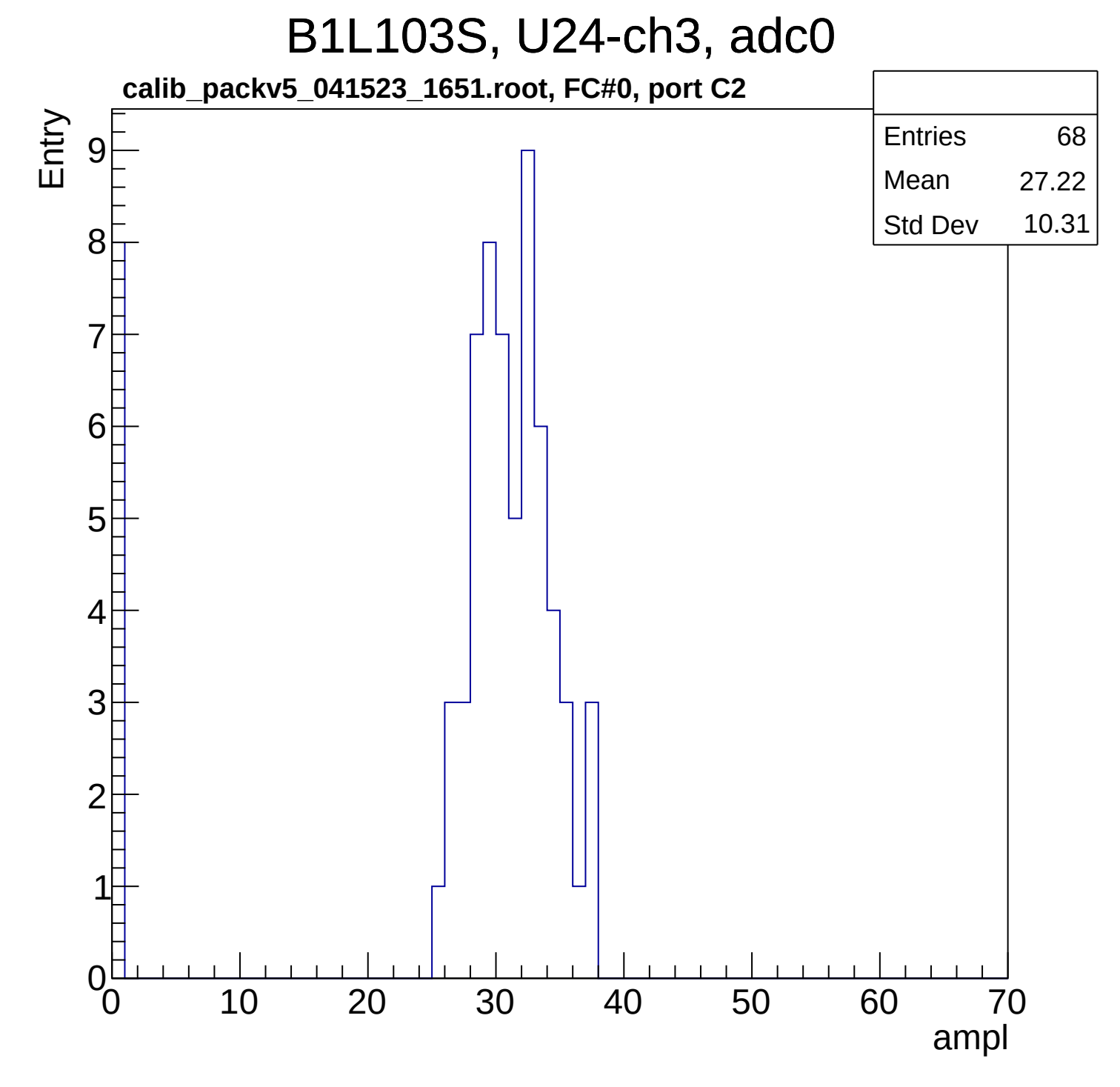
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U24-ch2, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch3, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 27.22
Std Dev 10.31
Entry
ampl
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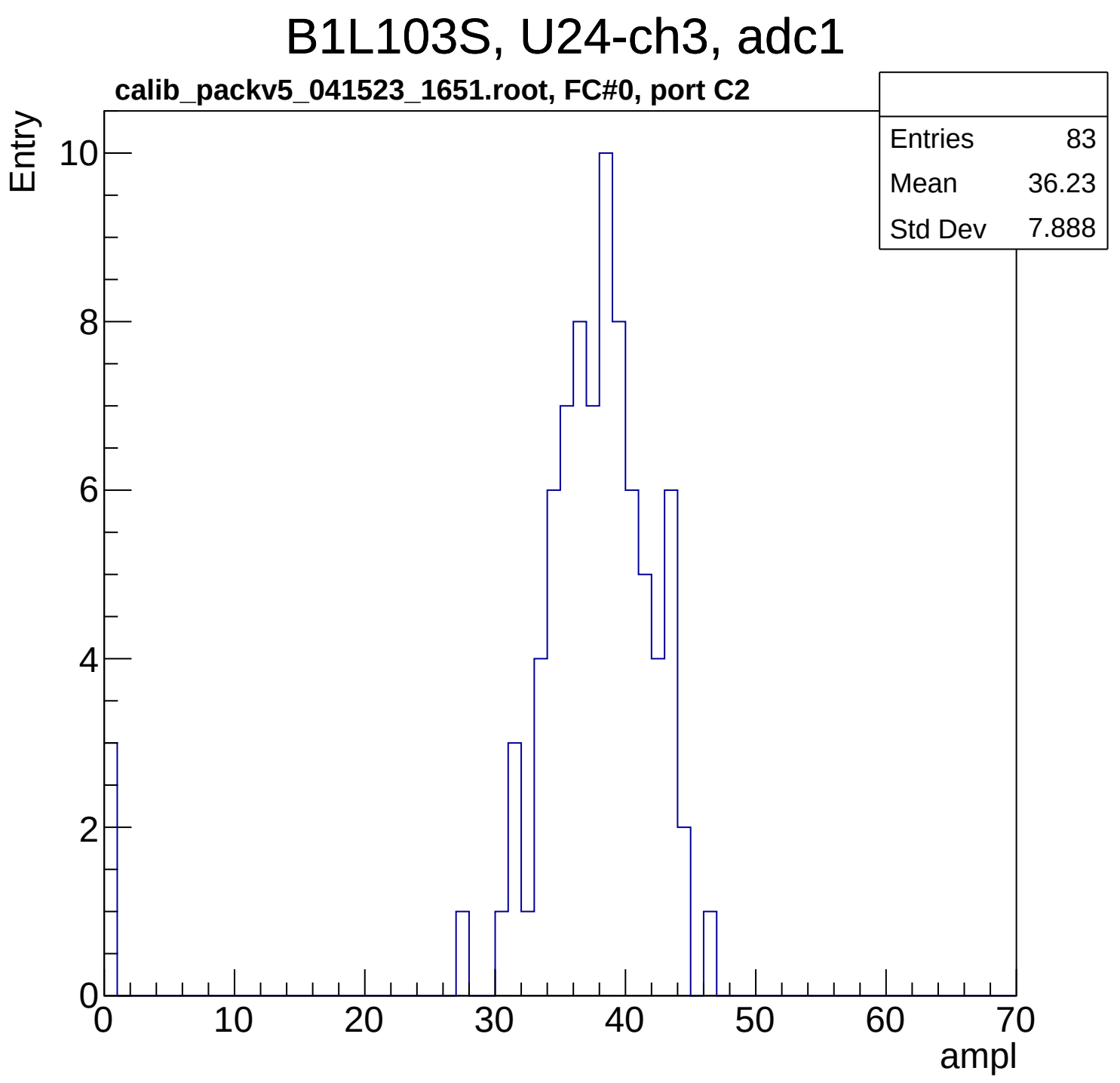
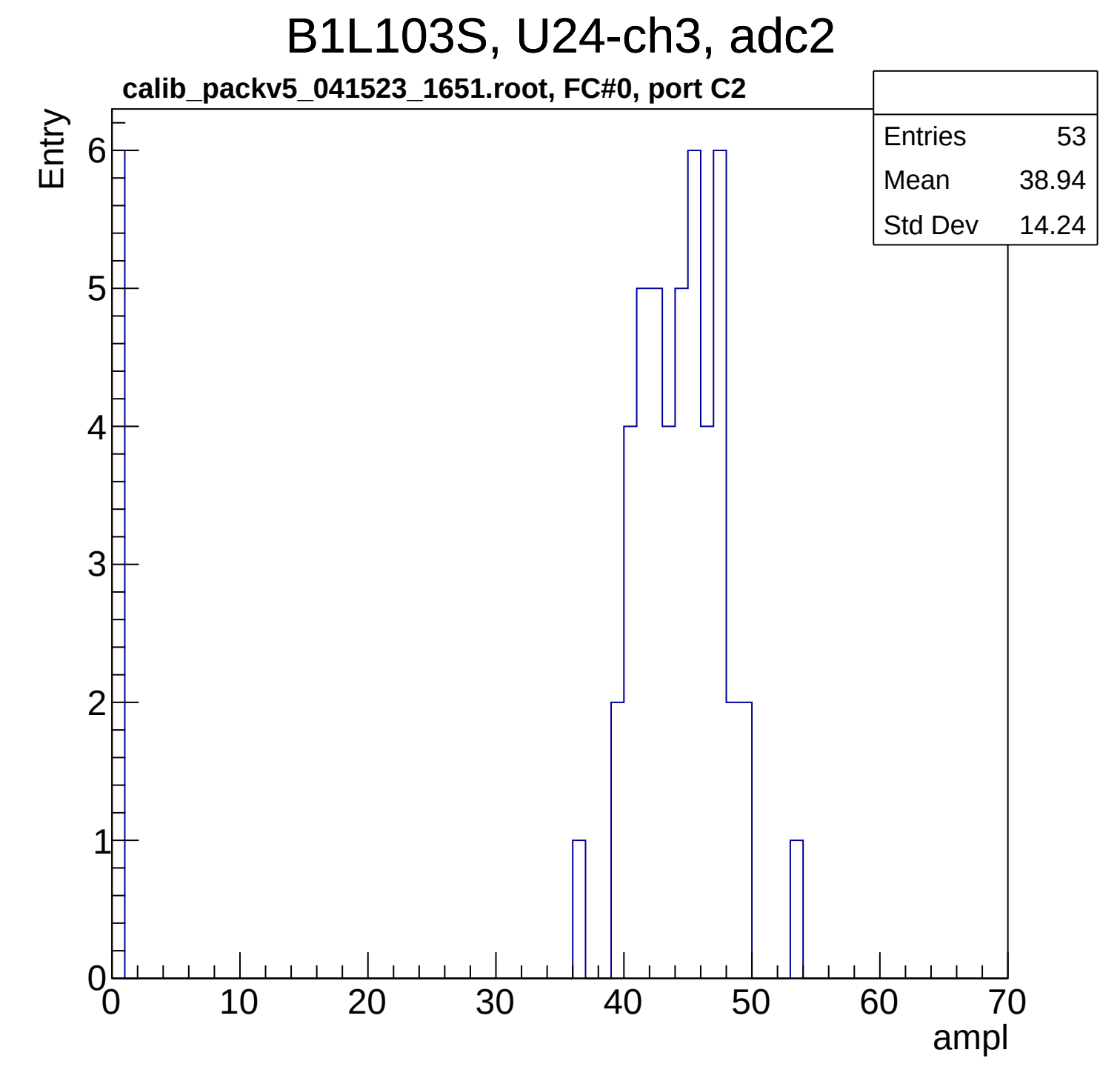
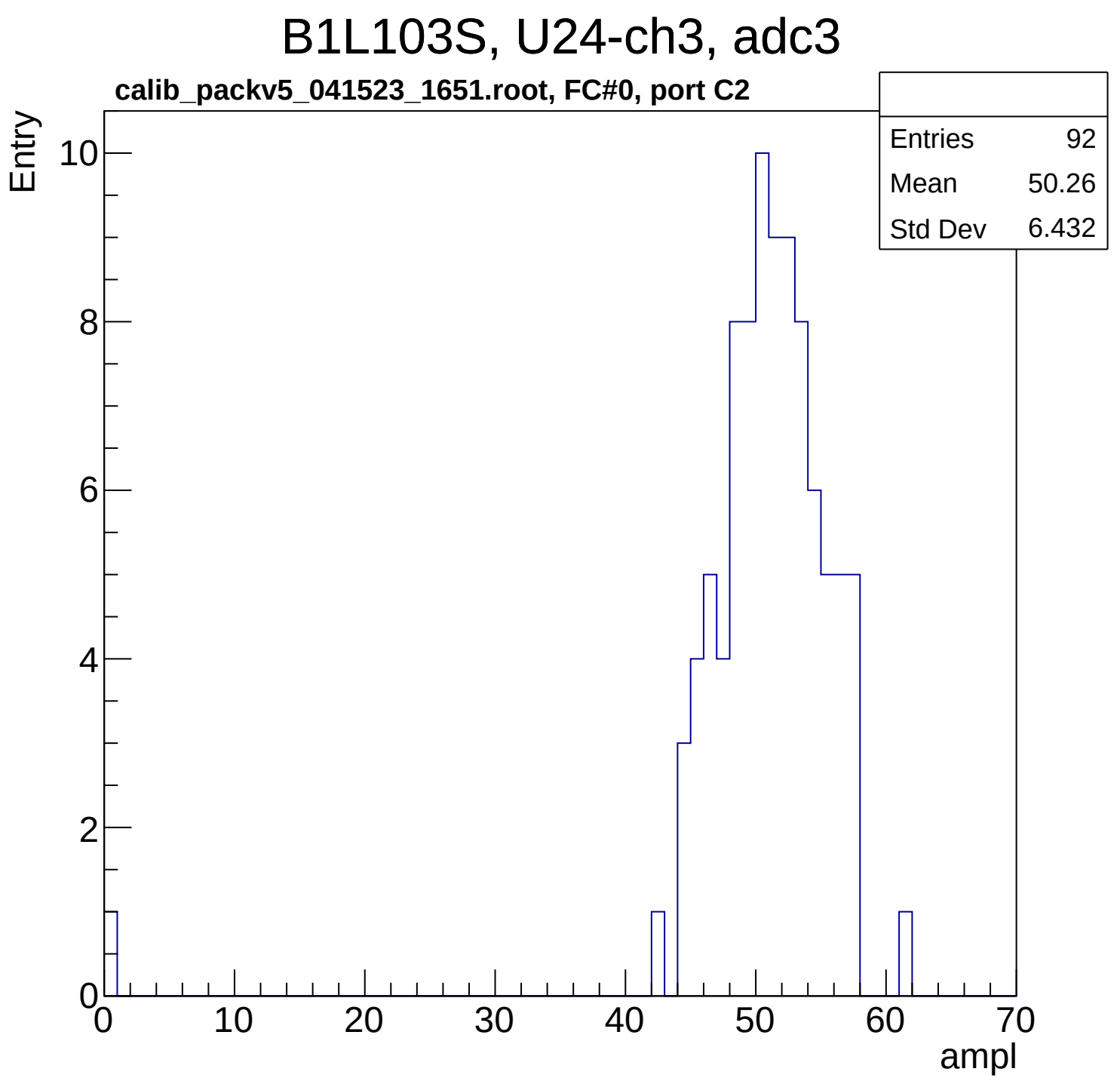
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U24-ch3, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 36.23
Std Dev 7.888
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U24-ch3, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 38.94
Std Dev 14.24
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch3, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 92
Mean 50.26
Std Dev 6.432
Entry
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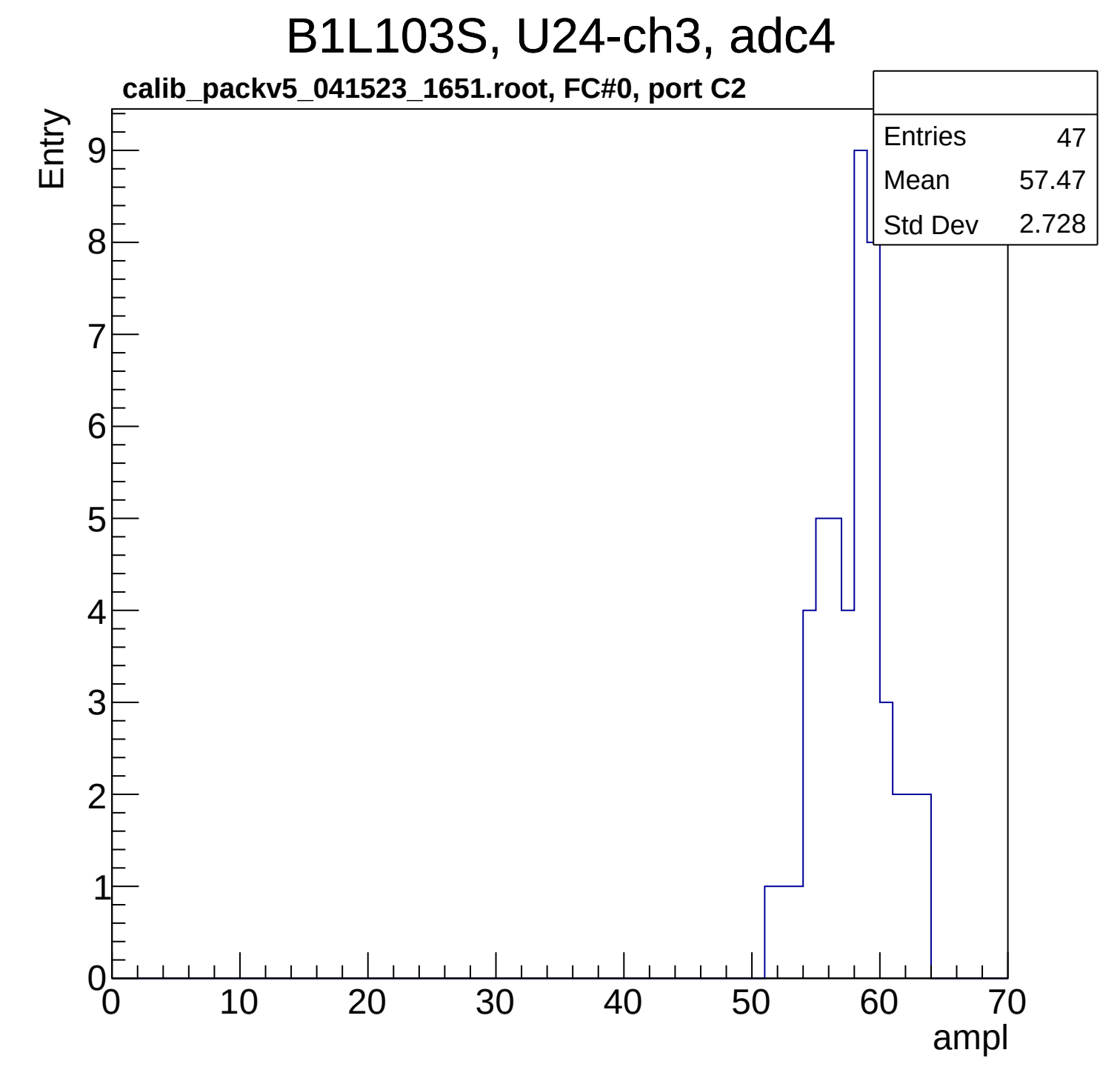
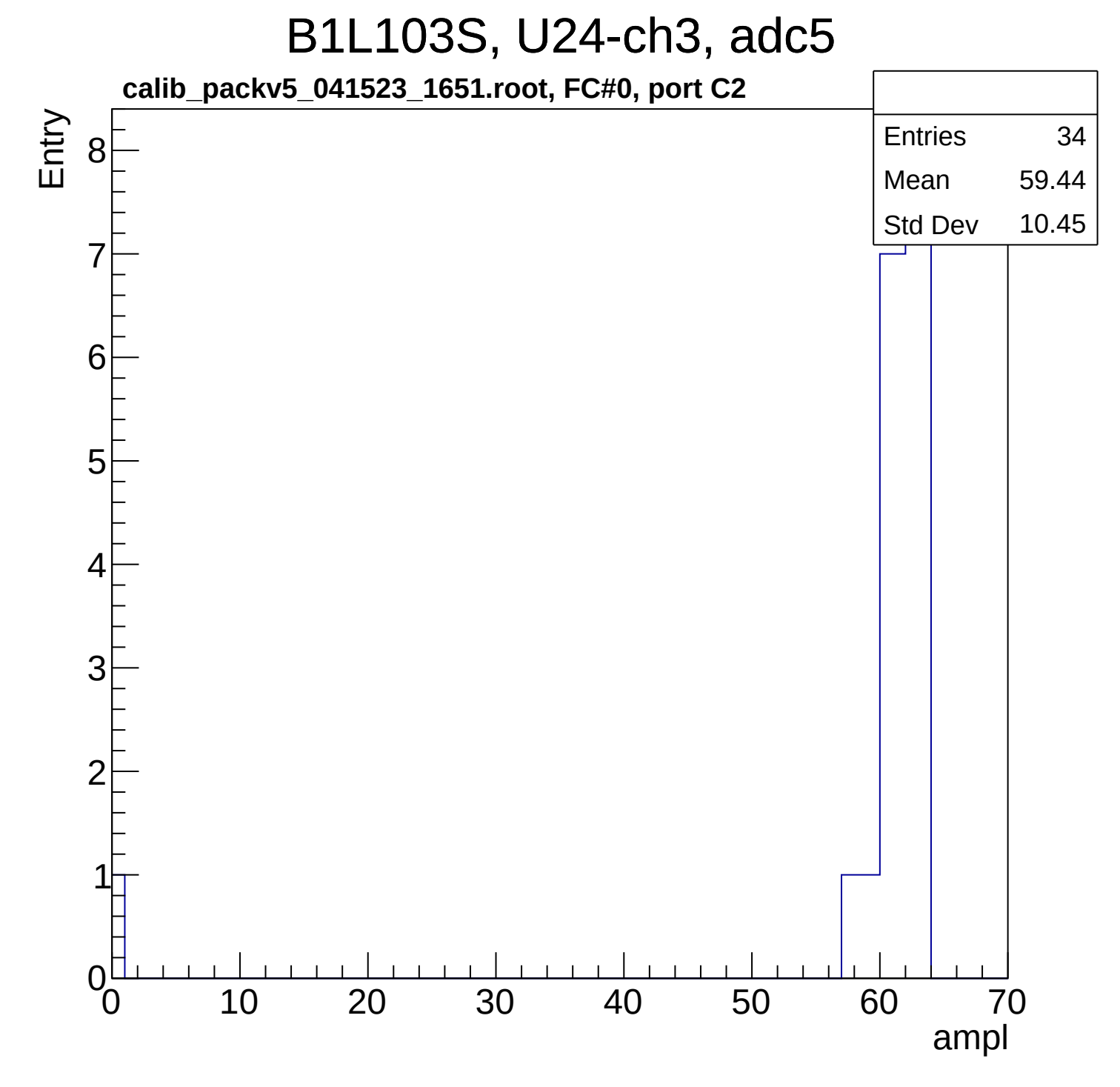
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch3, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 57.47
Std Dev 2.728
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U24-ch3, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 34
Mean 59.44
Std Dev 10.45
Entry
ampl
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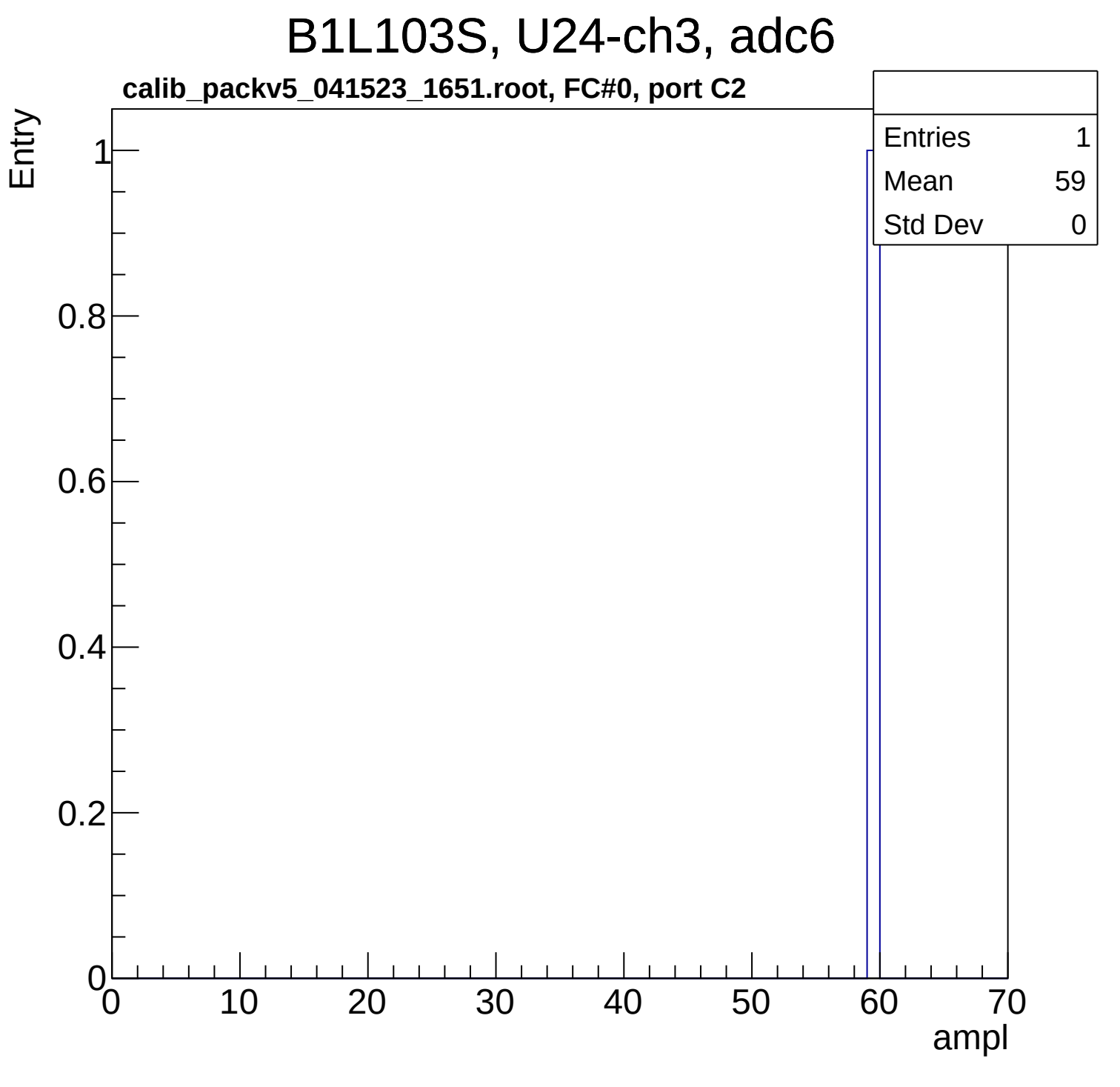
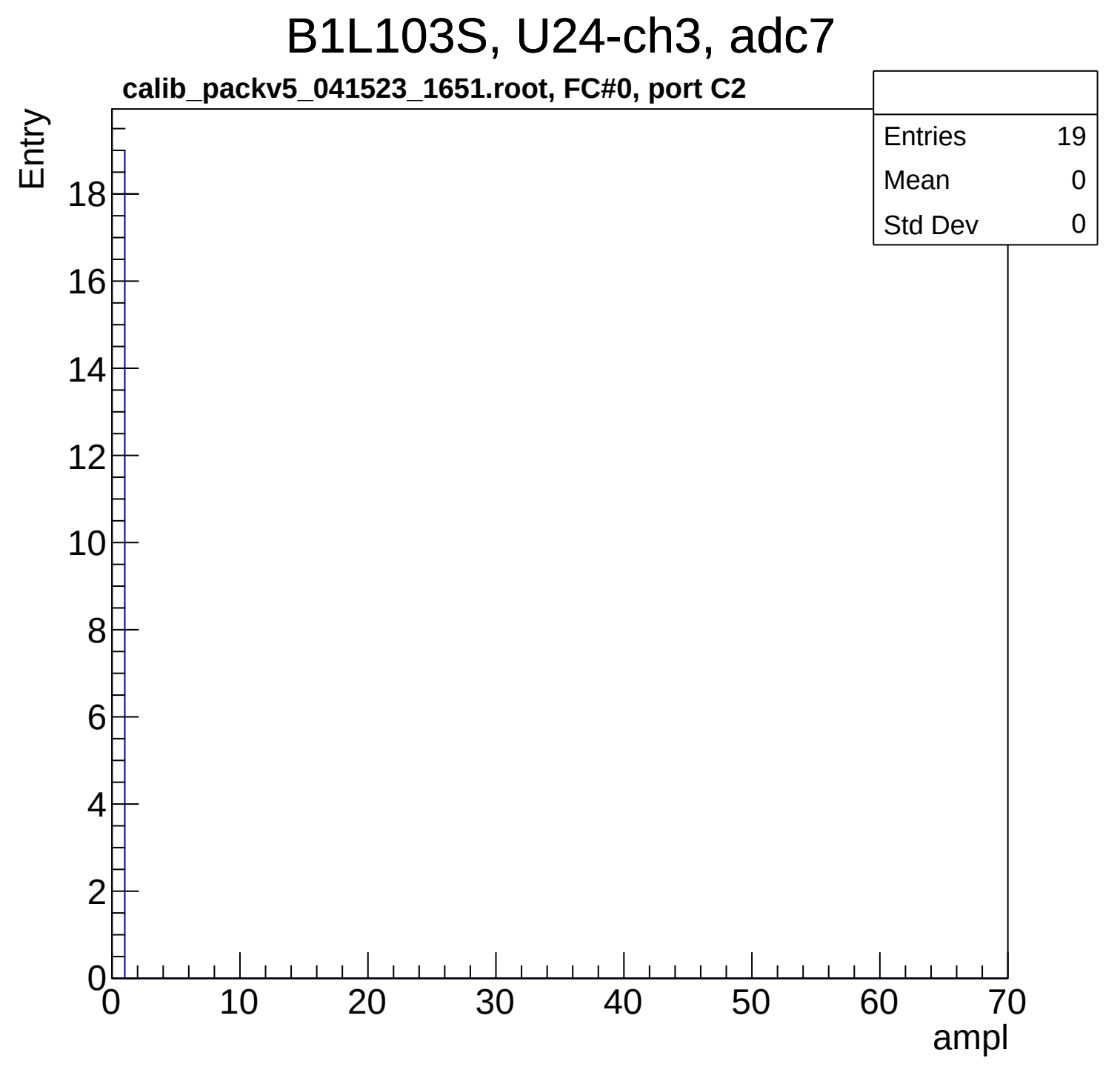
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U24-ch3, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 1
Mean 59
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70


B1L103S, U24-ch3, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
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6
8
10
12
14
16
18
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10
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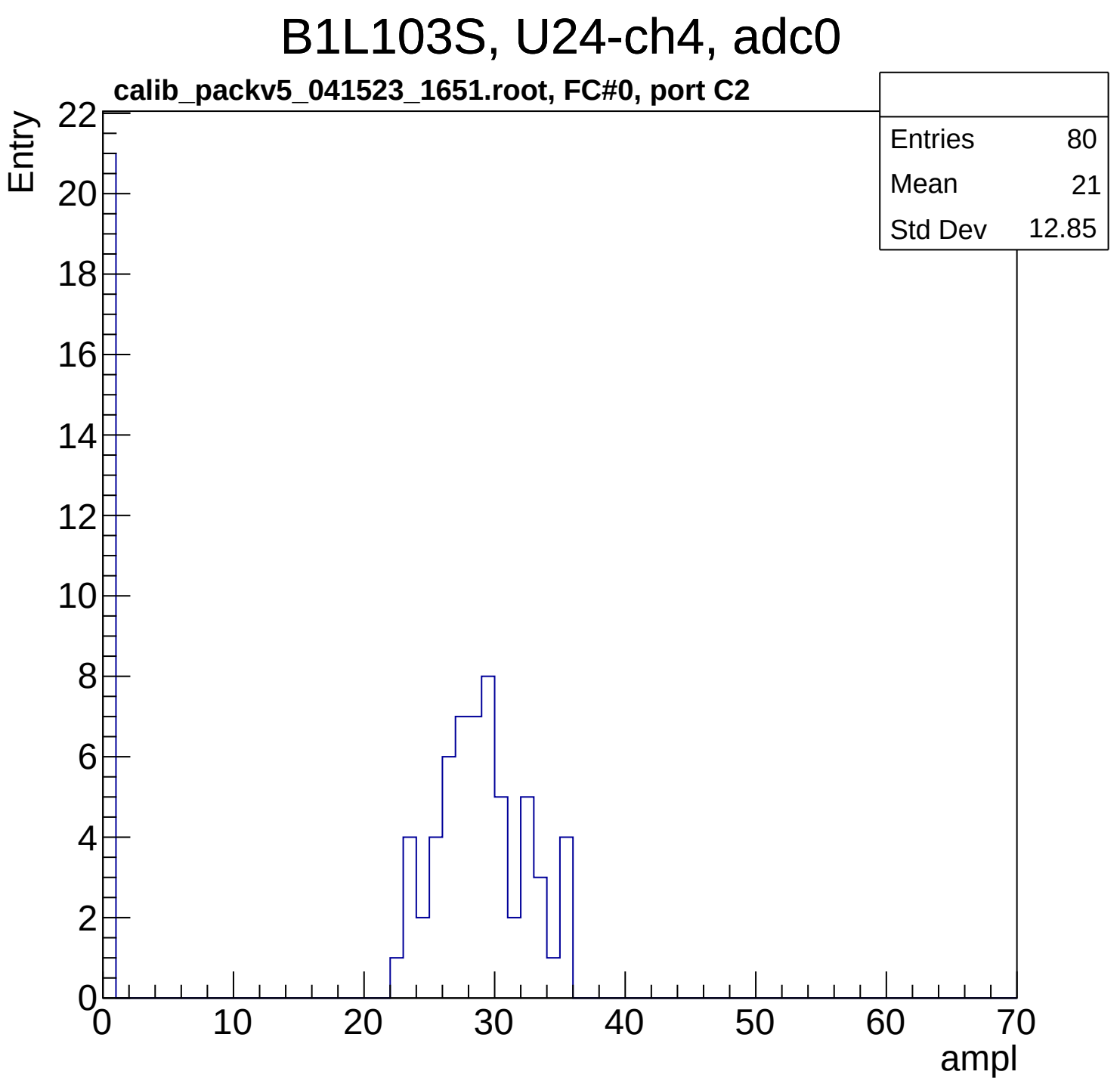
50
60
70
ampl


B1L103S, U24-ch4, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 21
Std Dev 12.85
Entry
ampl
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8
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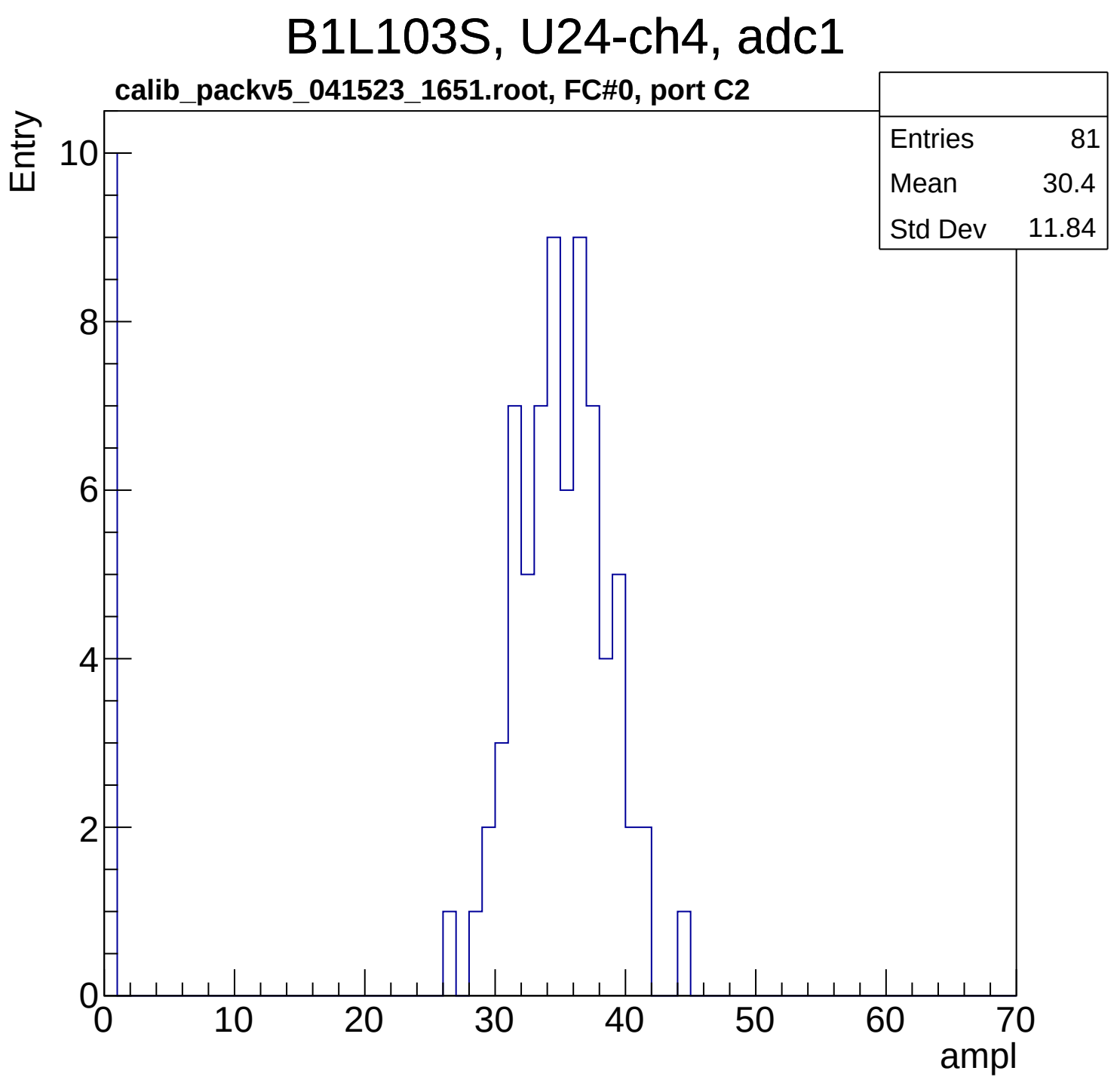
B1L103S, U24-ch4, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 30.4
Std Dev 11.84
Entry
ampl
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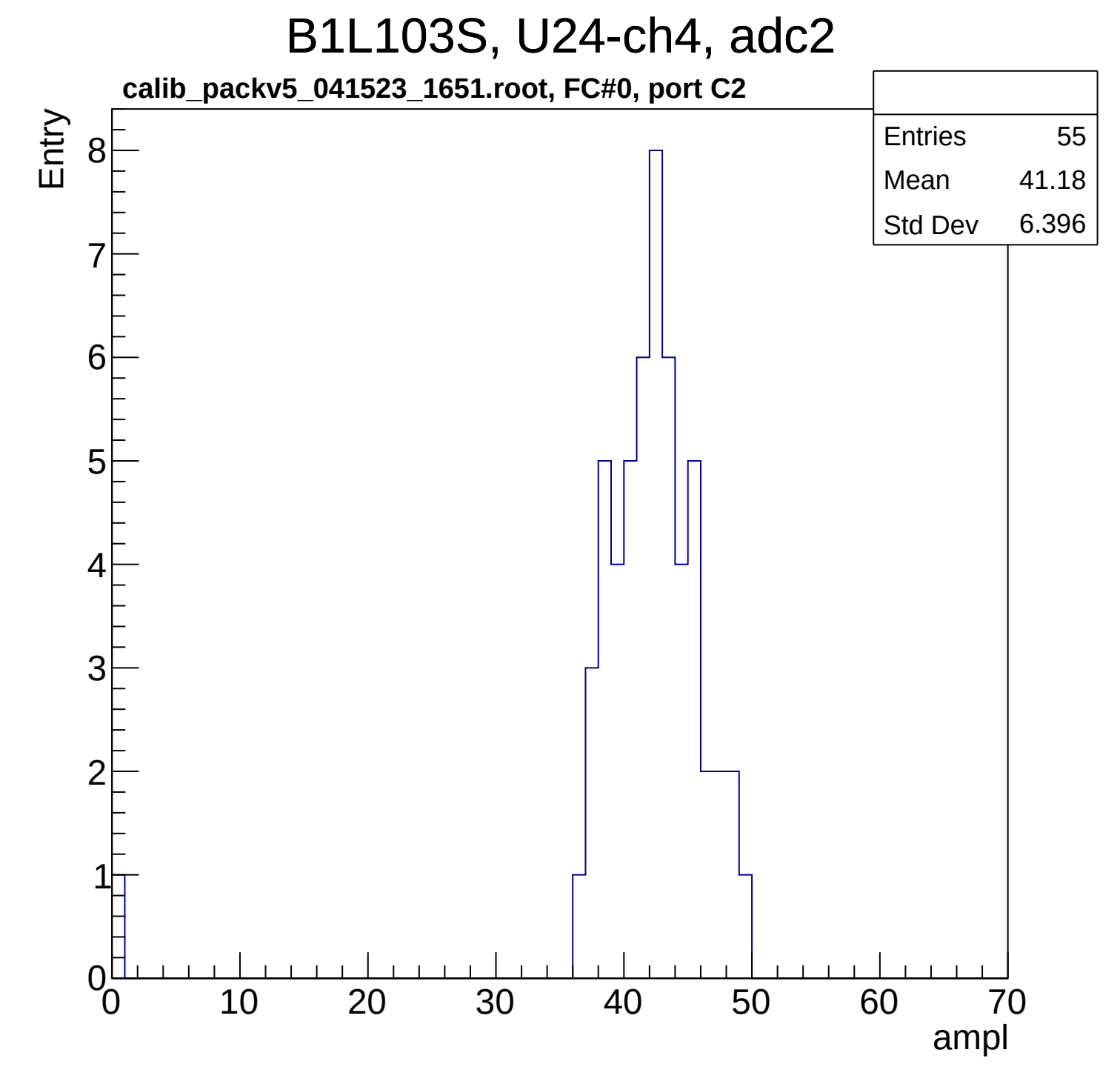
B1L103S, U24-ch4, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 41.18
Std Dev 6.396
Entry
ampl
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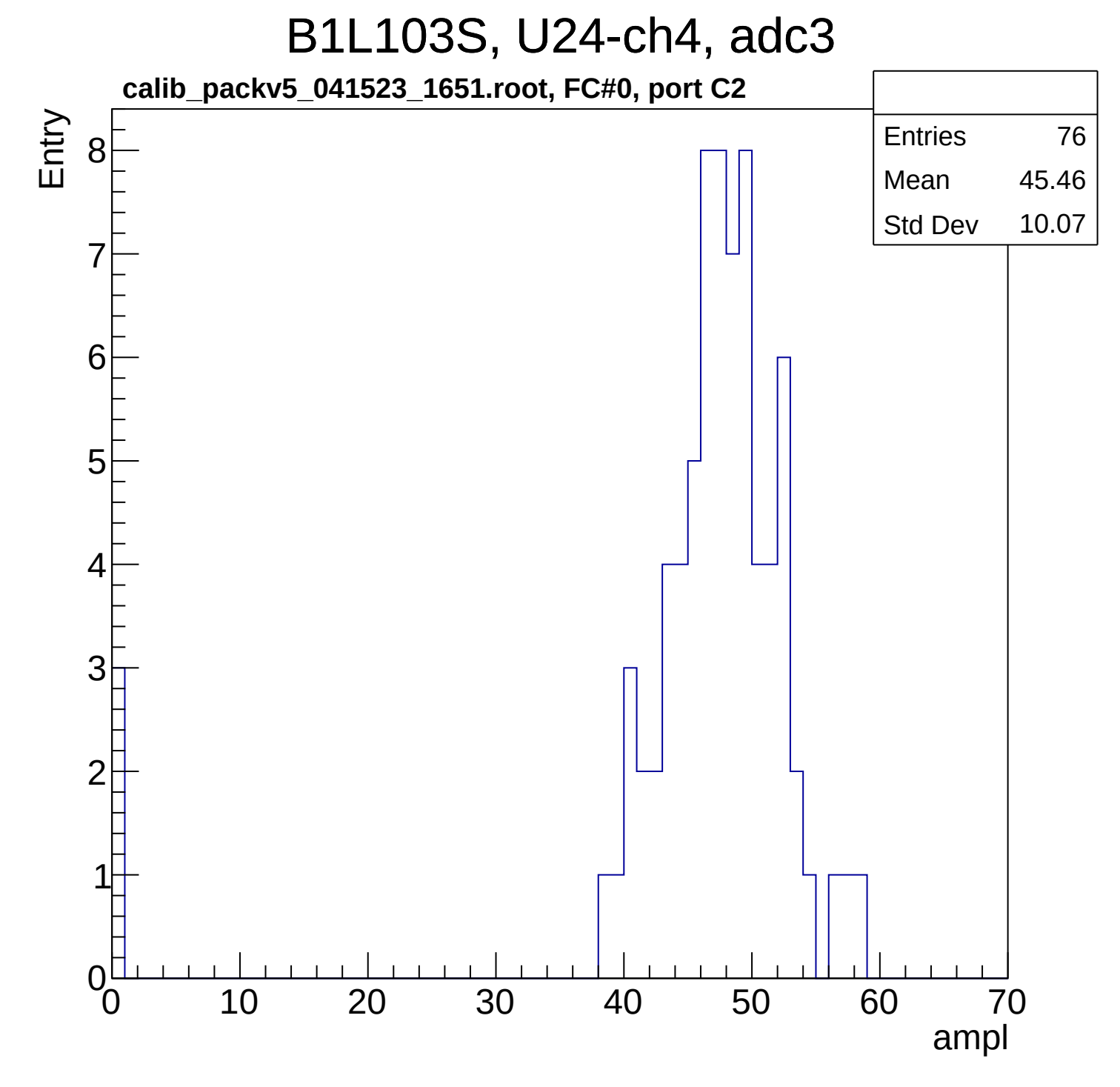
B1L103S, U24-ch4, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 45.46
Std Dev 10.07
Entry
ampl
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2
3
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7
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0
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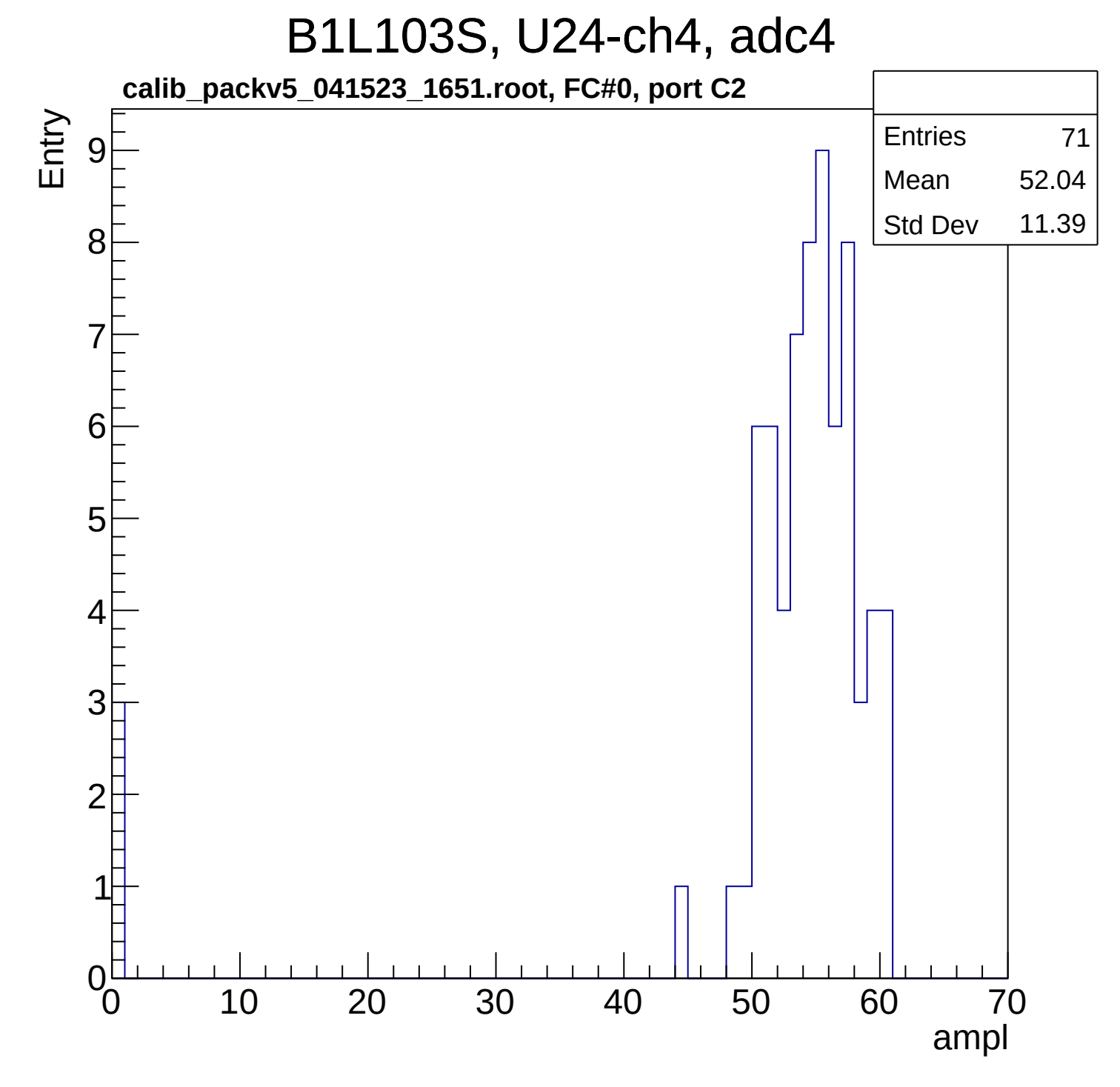
B1L103S, U24-ch4, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 52.04
Std Dev 11.39
Entry
ampl
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3
4
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7
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0
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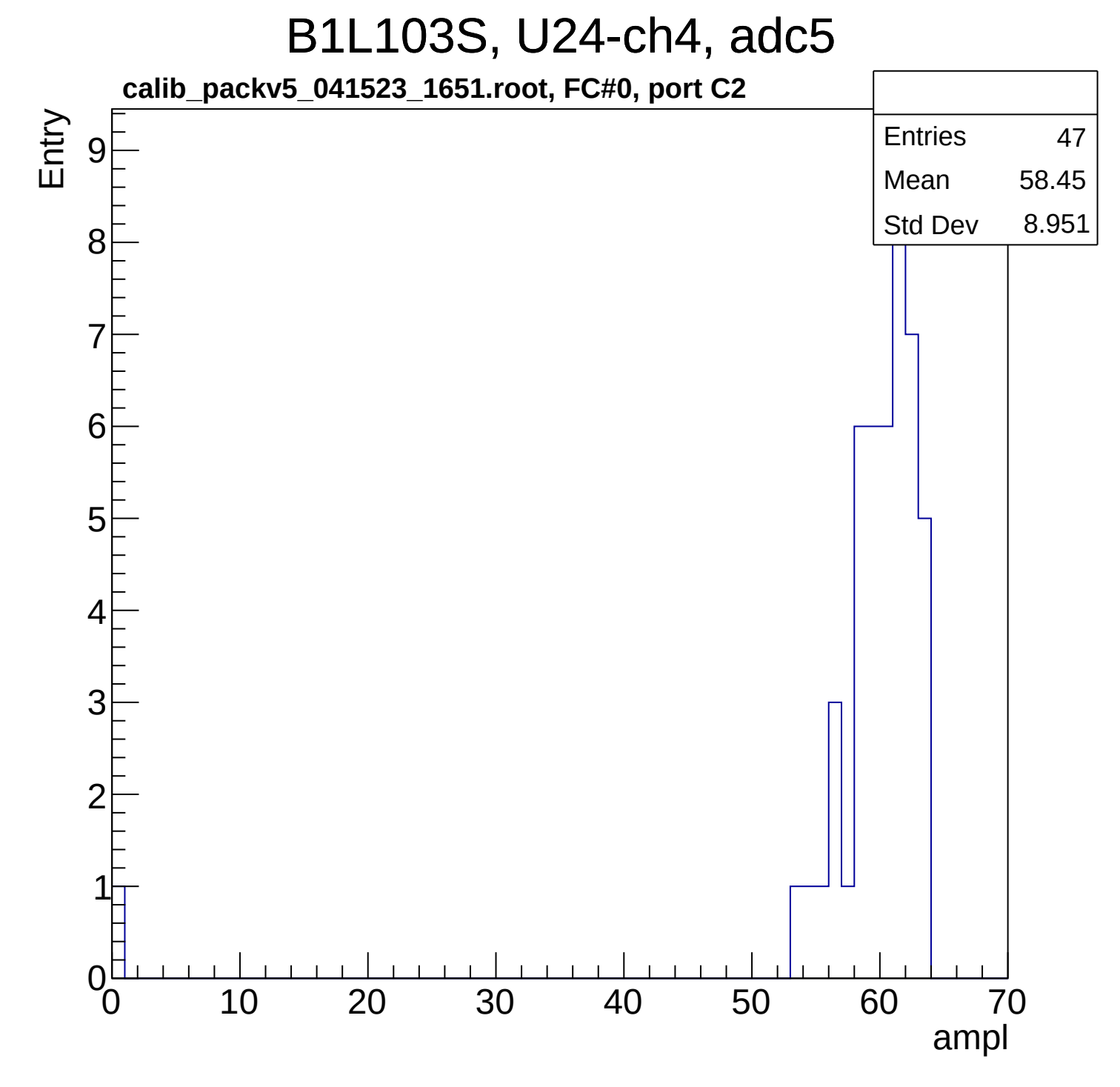
B1L103S, U24-ch4, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 58.45
Std Dev 8.951
Entry
ampl
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2
3
4
5
6
7
8
9
0
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60
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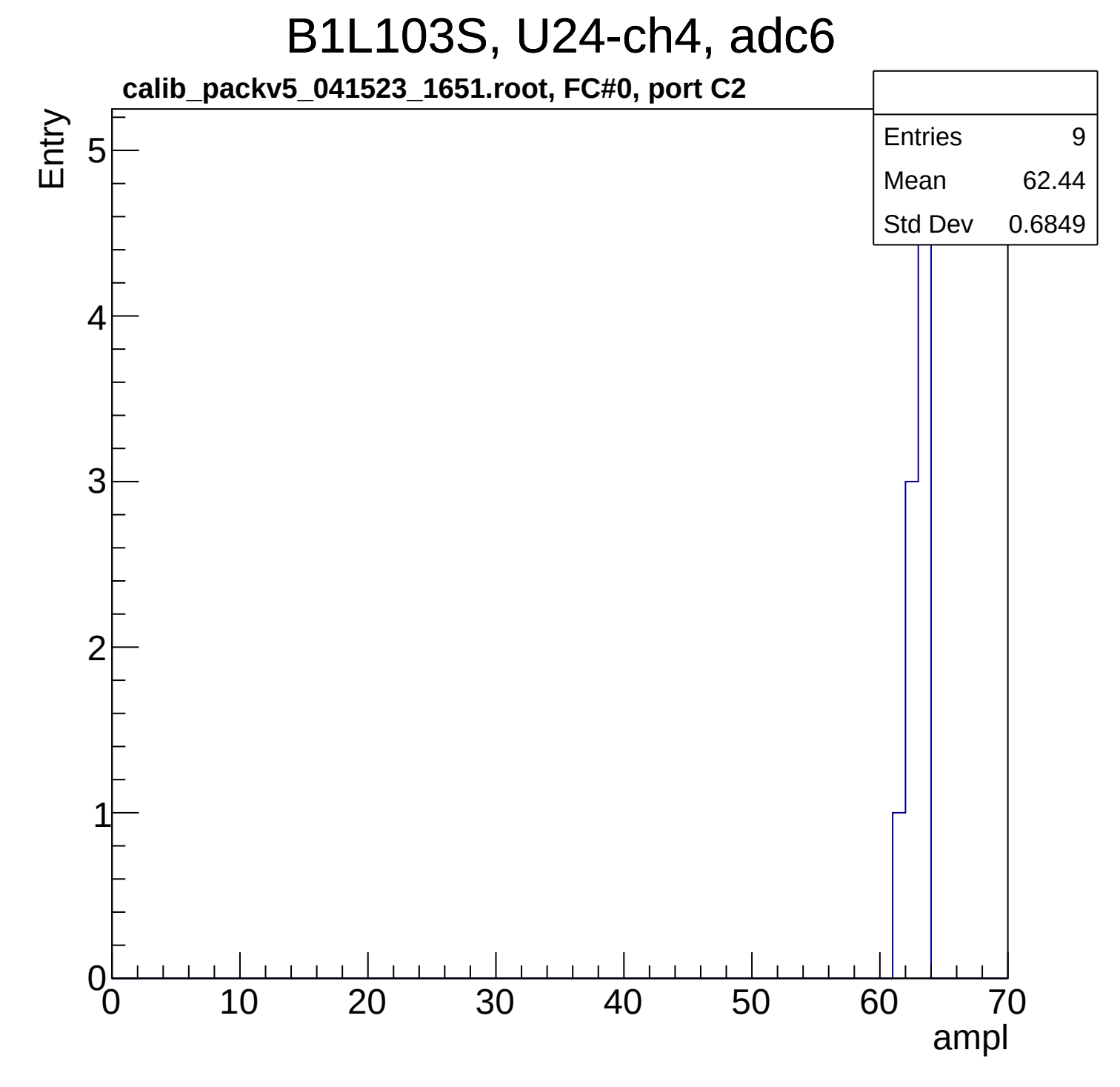
B1L103S, U24-ch4, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 9
Mean 62.44
Std Dev 0.6849
Entry
ampl
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3
4
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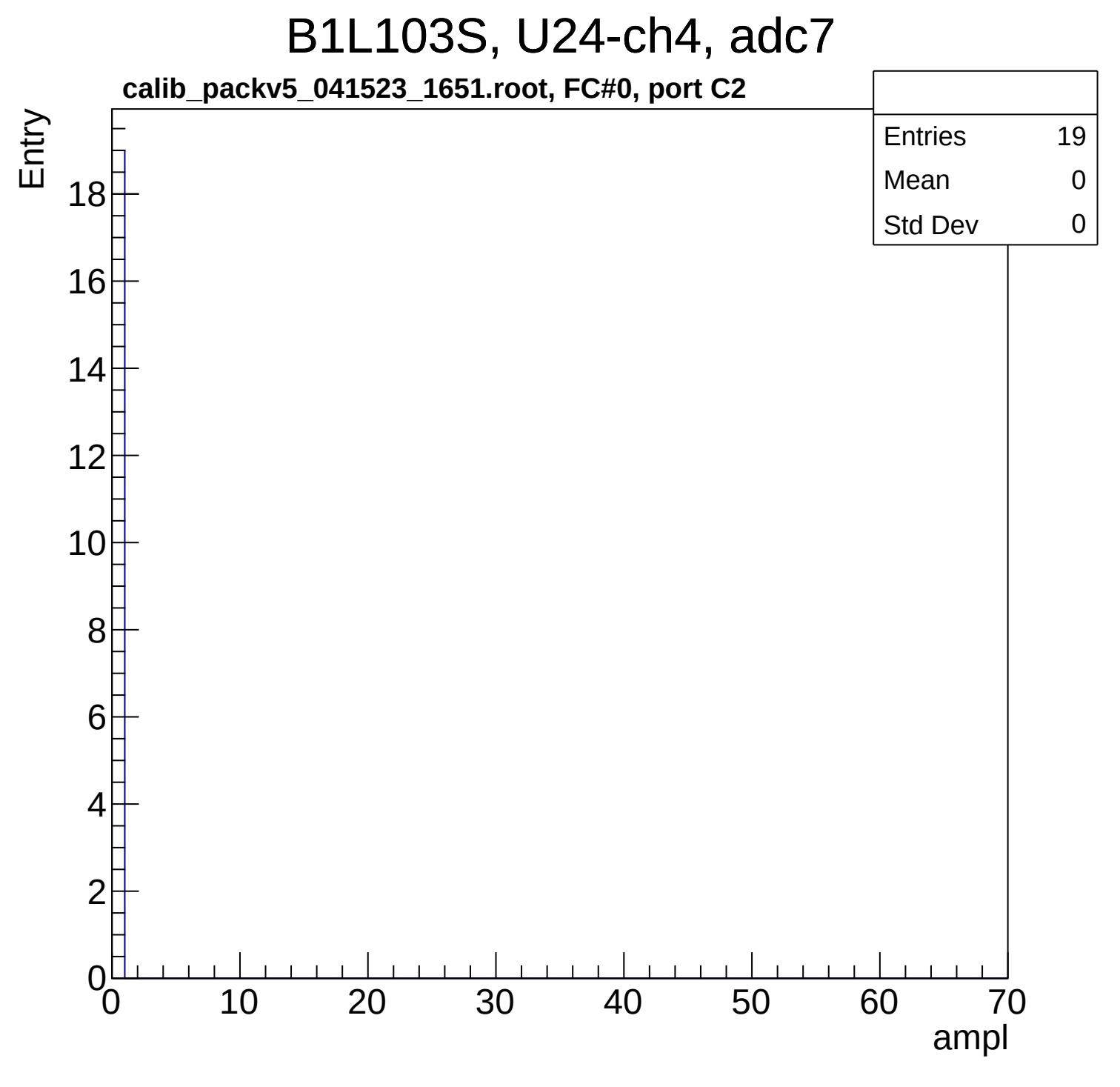
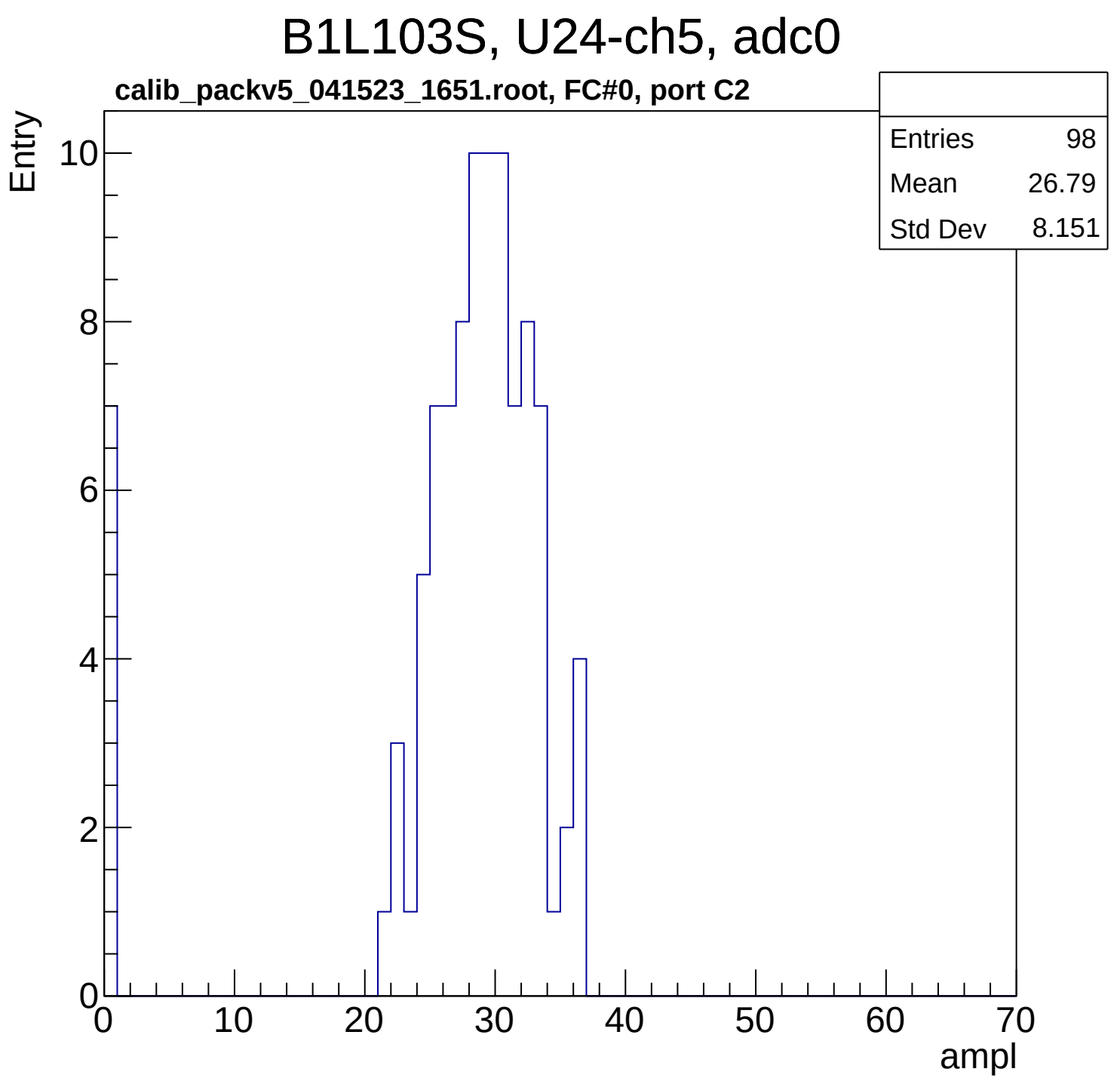
0
10
20
30
40
50
60
70


B1L103S, U24-ch4, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch5, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 98
Mean 26.79
Std Dev 8.151
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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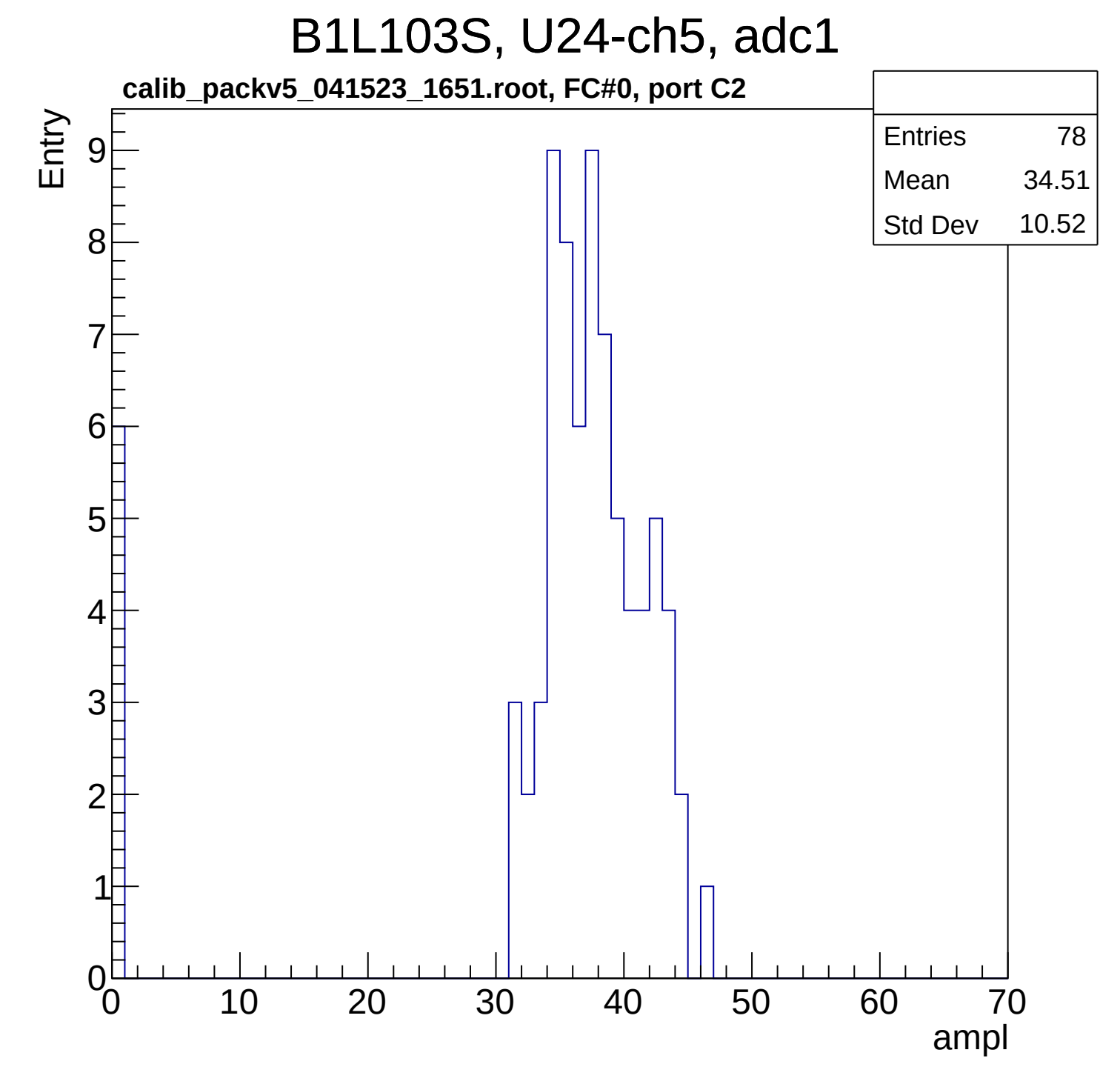
B1L103S, U24-ch5, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 34.51
Std Dev 10.52
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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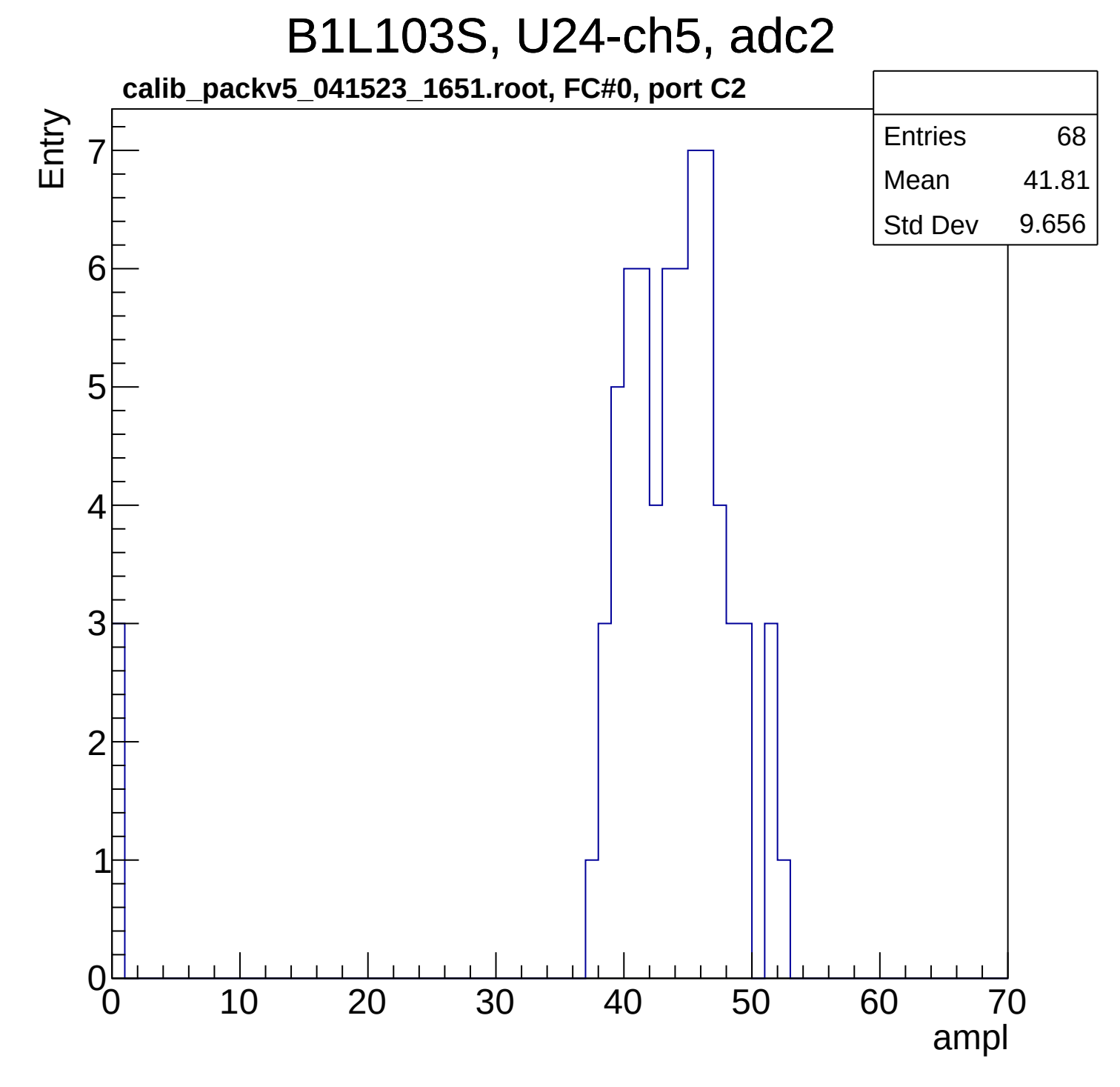
B1L103S, U24-ch5, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 41.81
Std Dev 9.656
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
30
40
50
60
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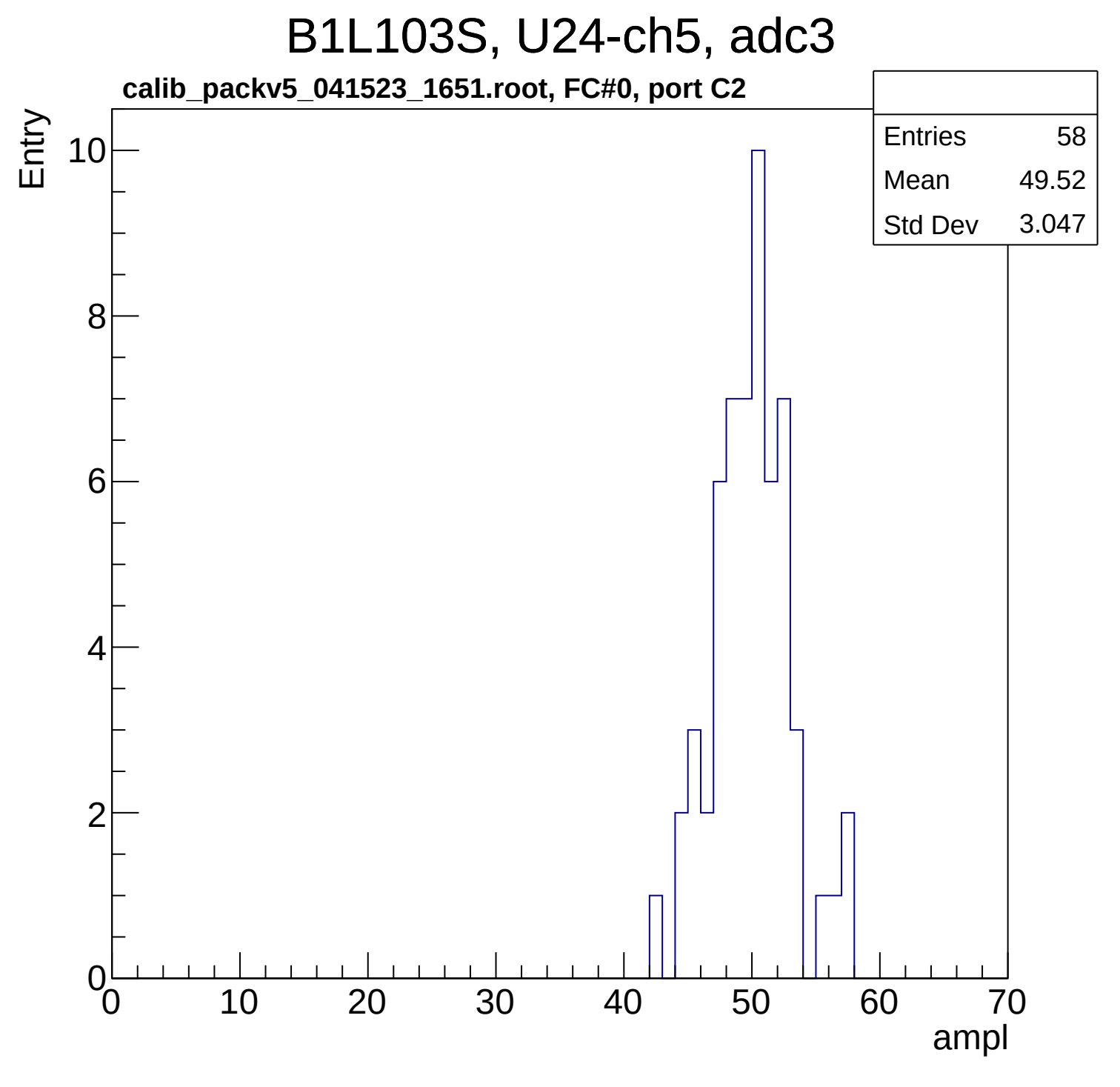
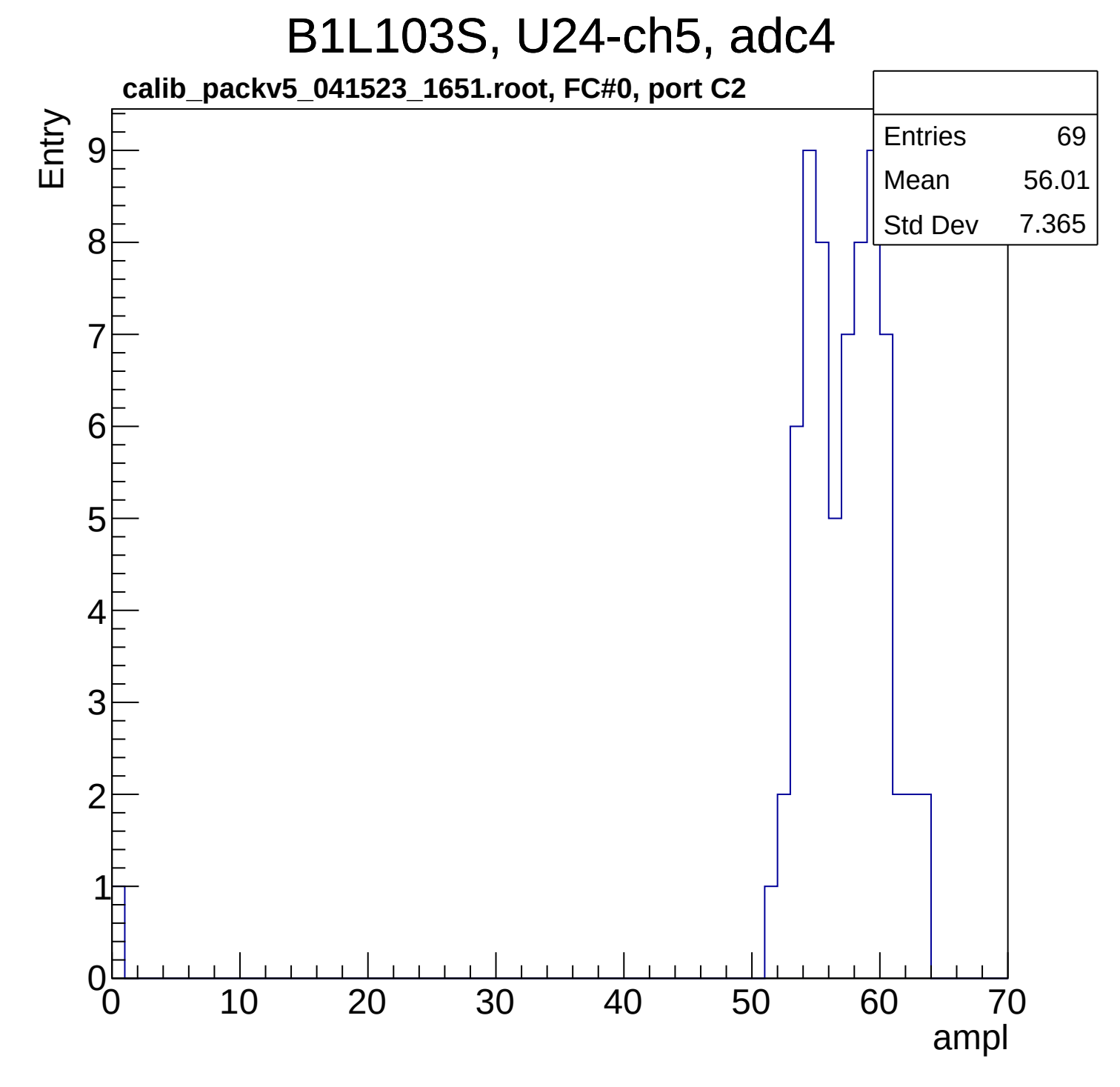

B1L103S, U24-ch5, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 49.52
Std Dev 3.047
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U24-ch5, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 56.01
Std Dev 7.365
Entry
ampl
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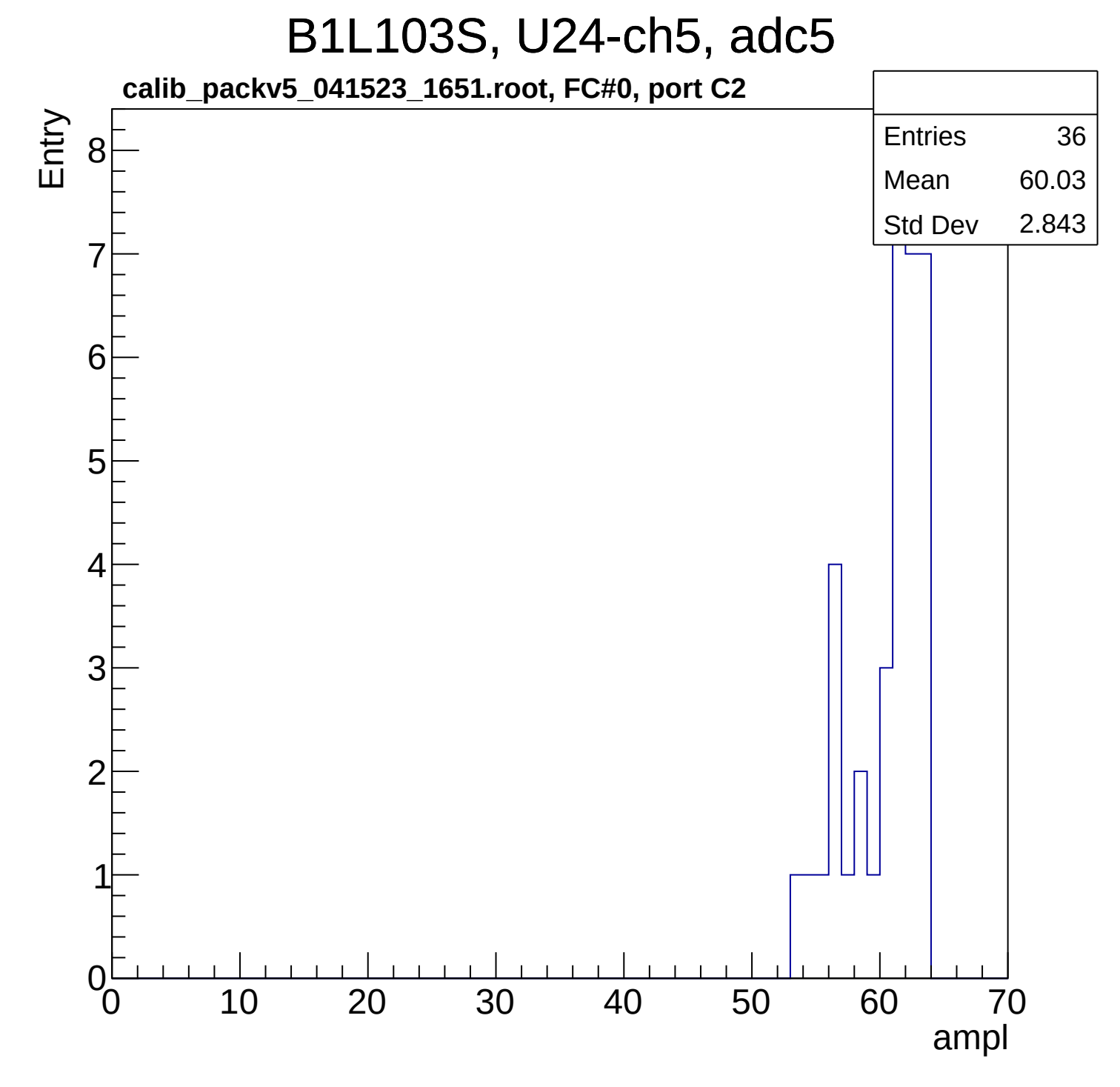
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U24-ch5, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 36
Mean 60.03
Std Dev 2.843
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
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40
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60
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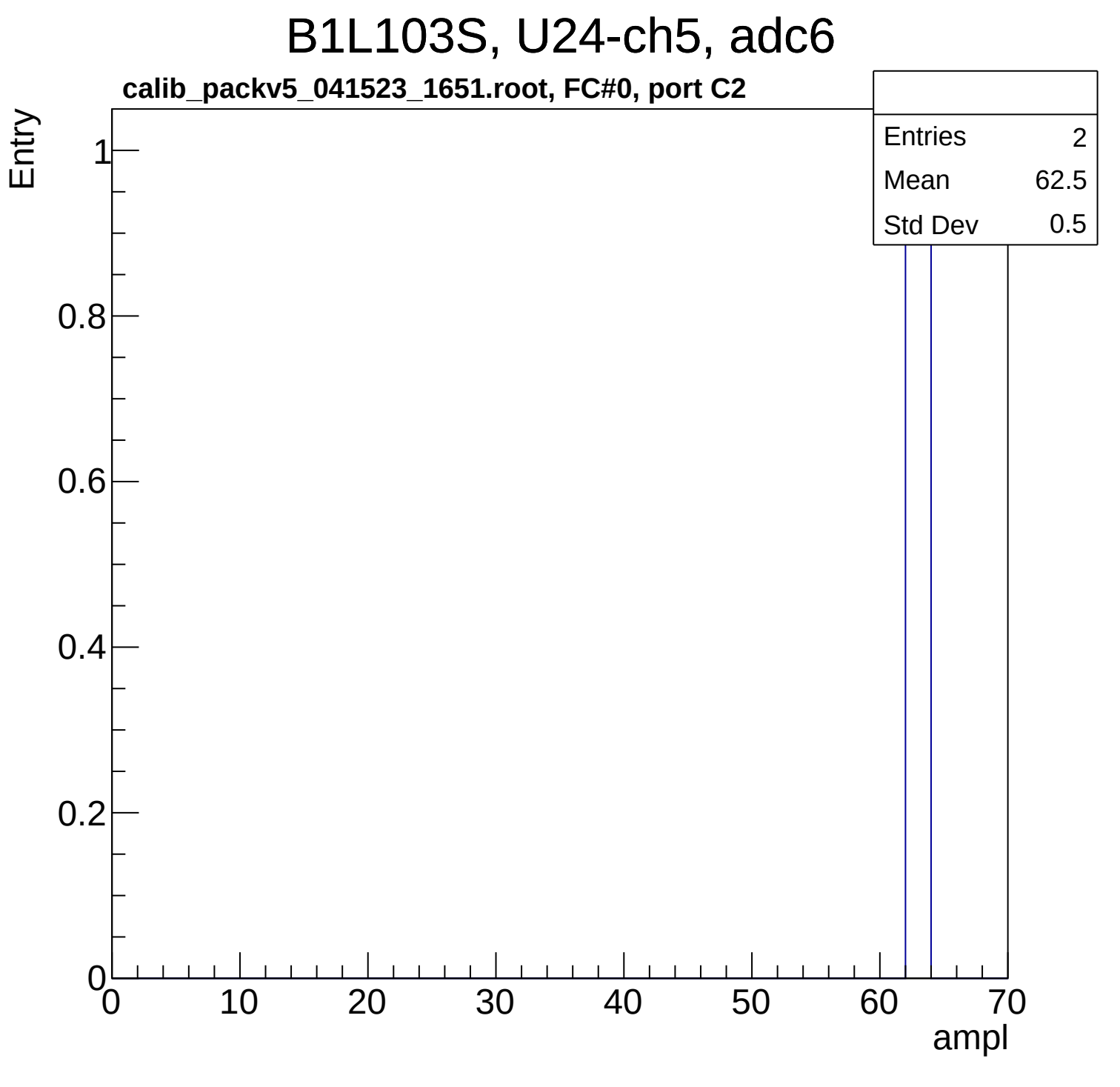
B1L103S, U24-ch5, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 2
Mean 62.5
Std Dev 0.5
Entry
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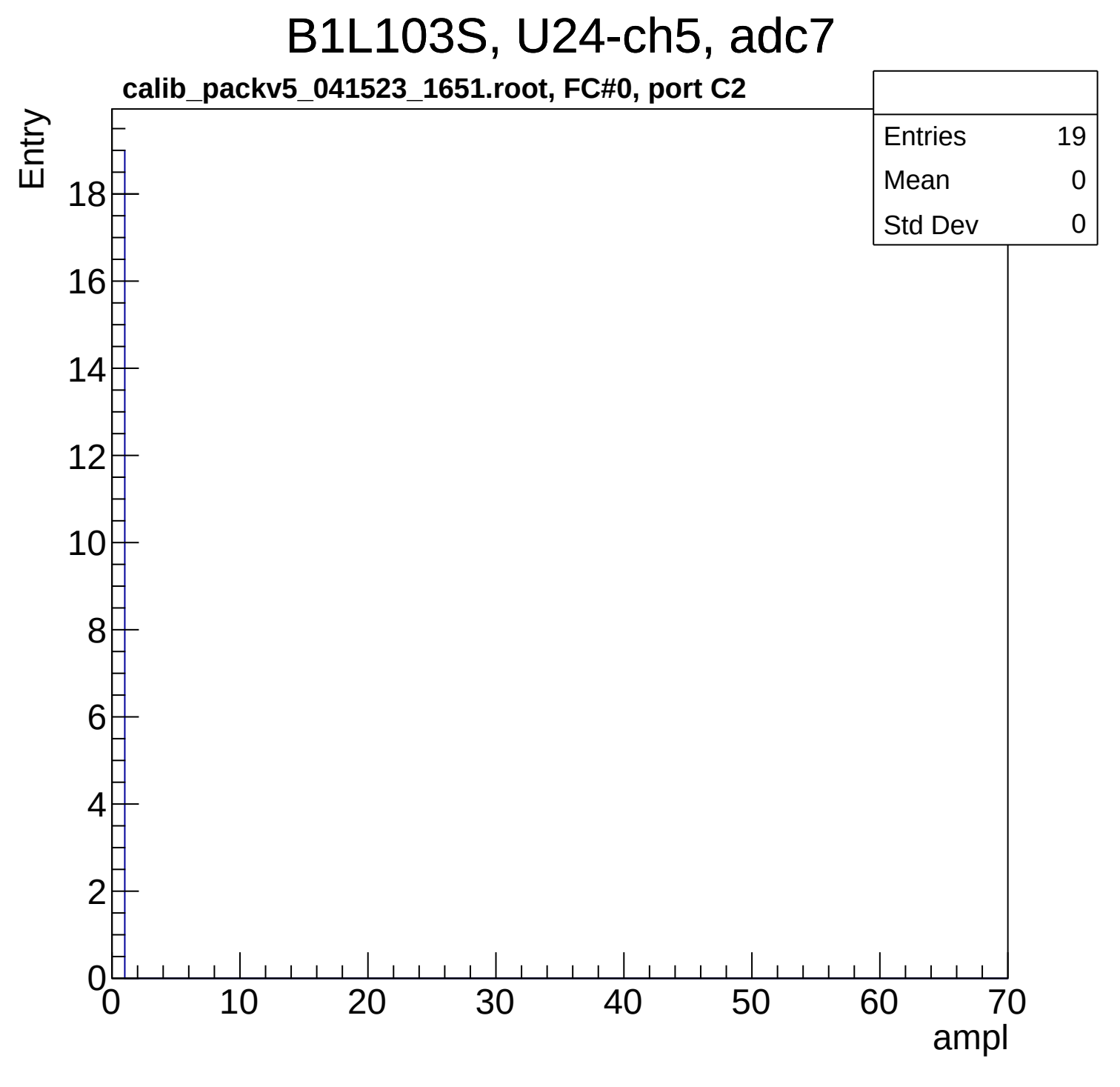
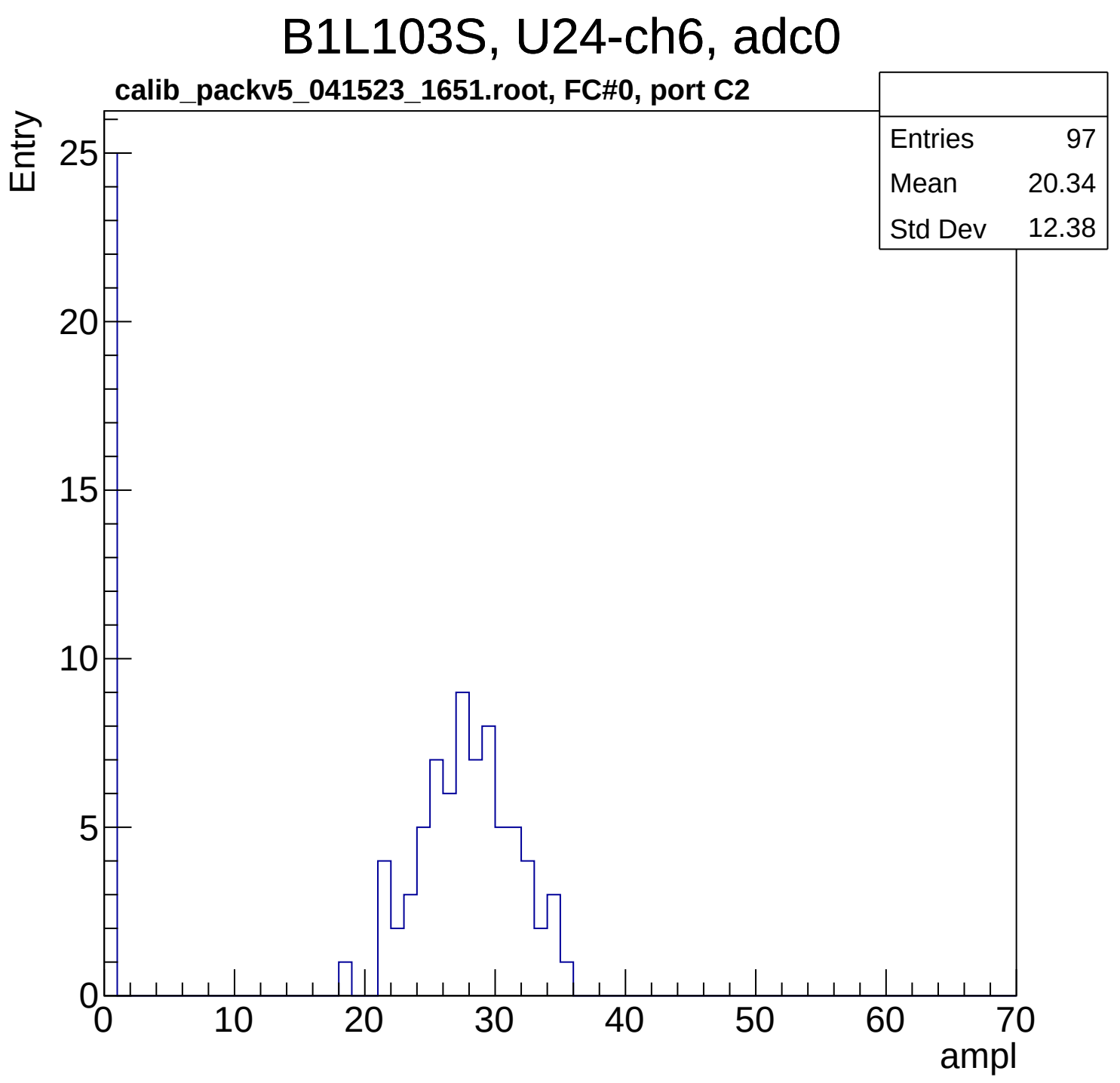
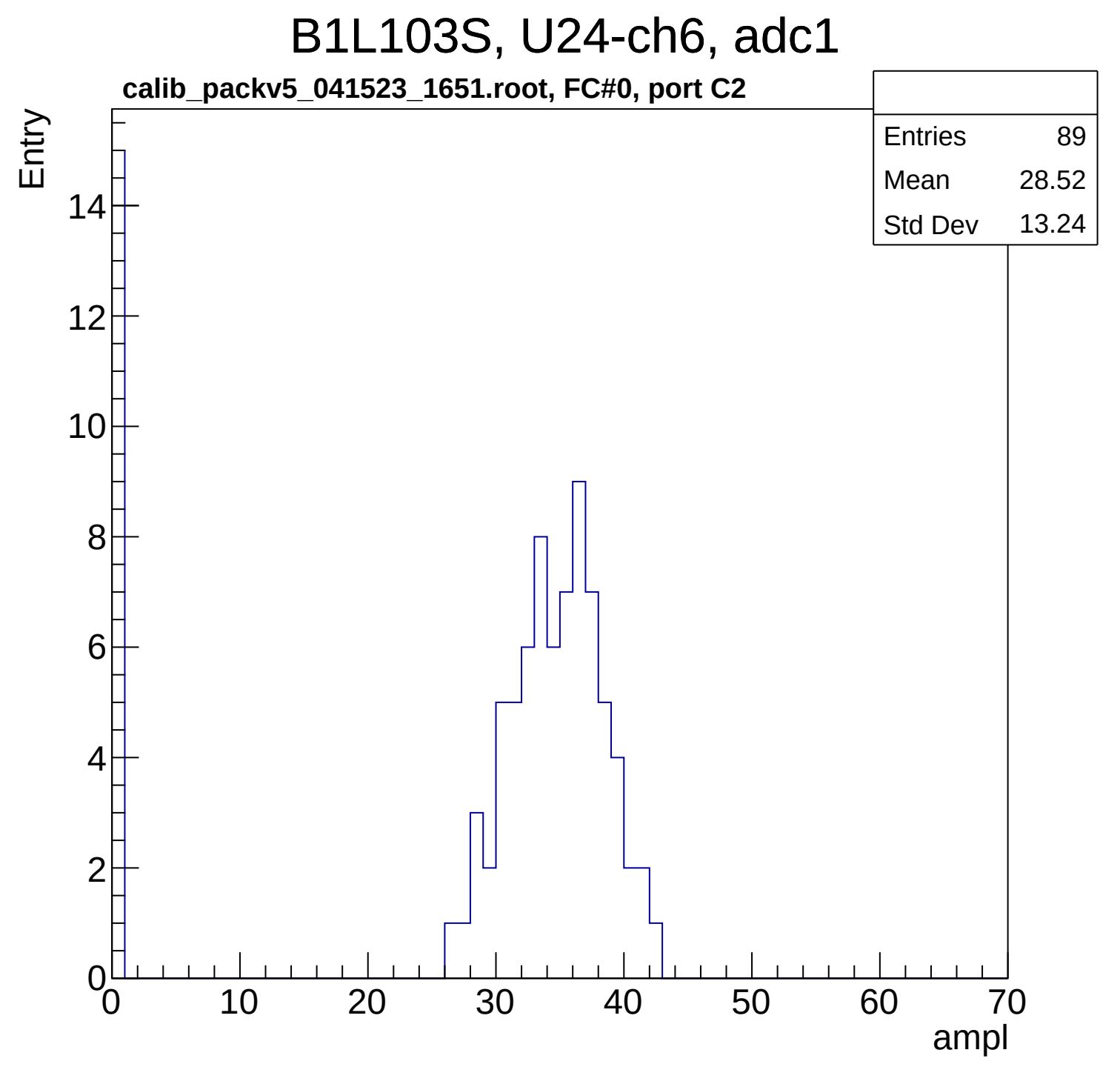
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch5, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch6, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 97
Mean 20.34
Std Dev 12.38
Entry
0
5
10
15
20
25
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch6, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 89
Mean 28.52
Std Dev 13.24
Entry
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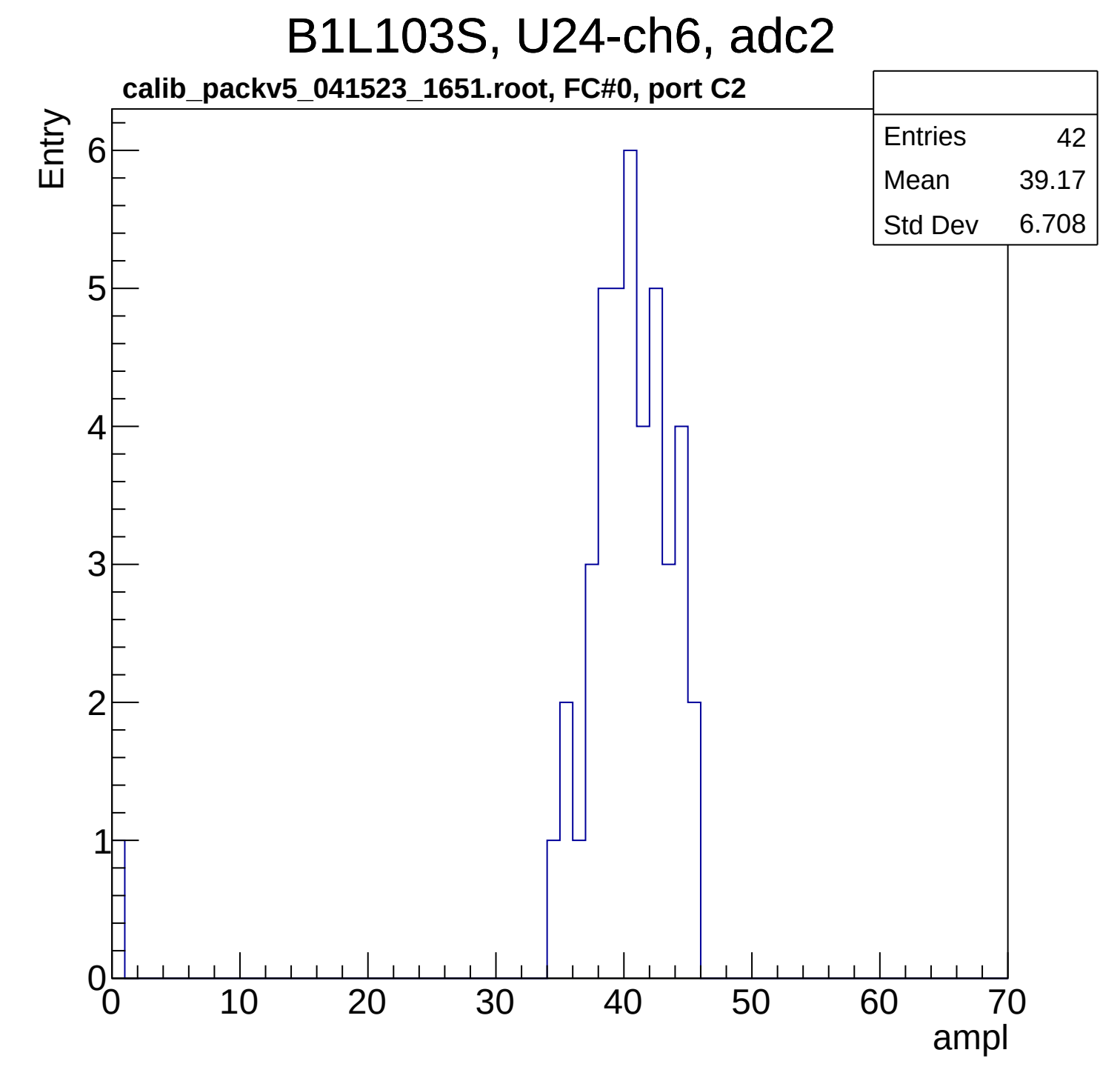
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch6, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 42
Mean 39.17
Std Dev 6.708
Entry
ampl
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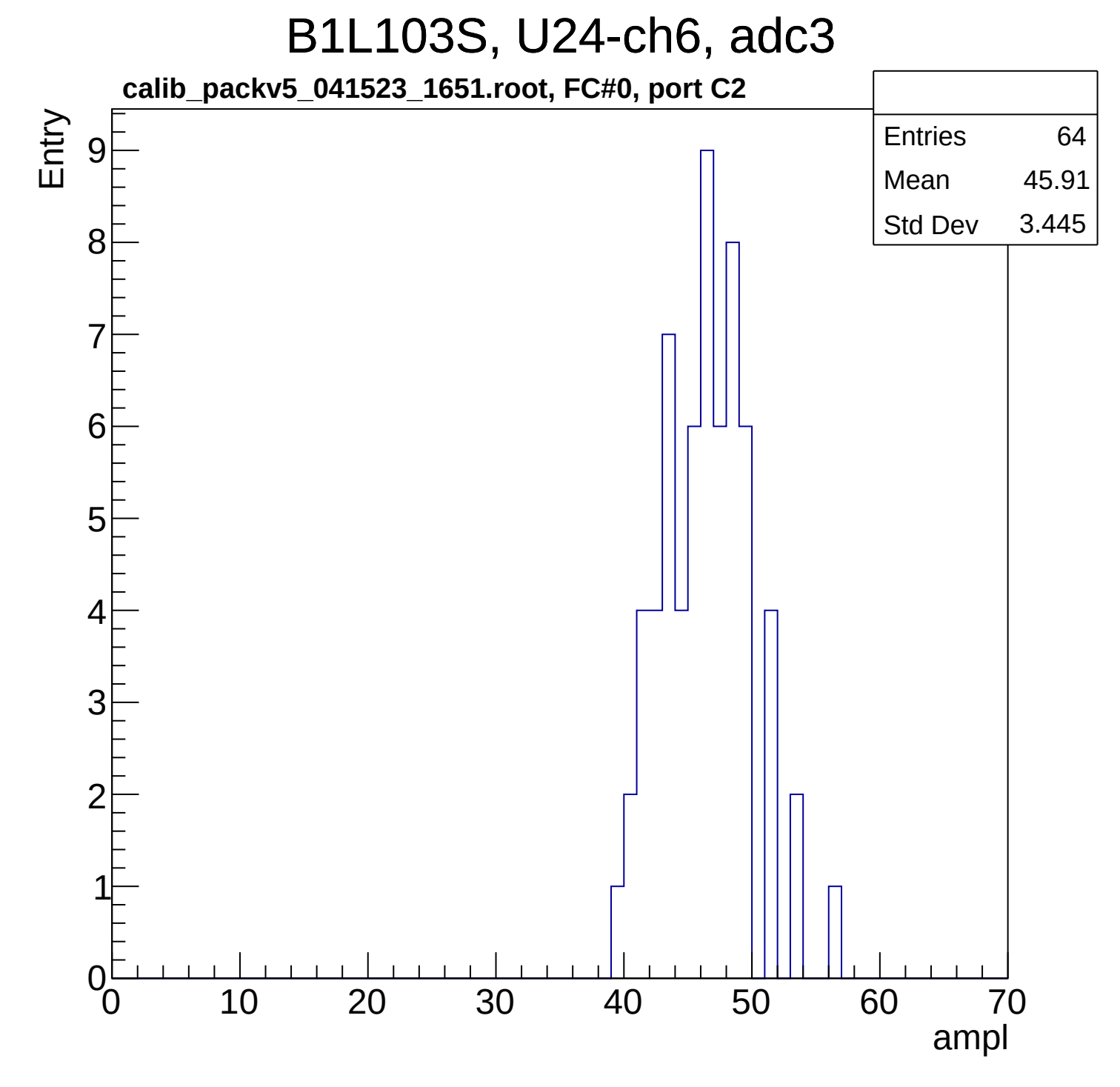
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U24-ch6, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 45.91
Std Dev 3.445
Entry
ampl
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3
4
5
6
7
8
9
0
10
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60
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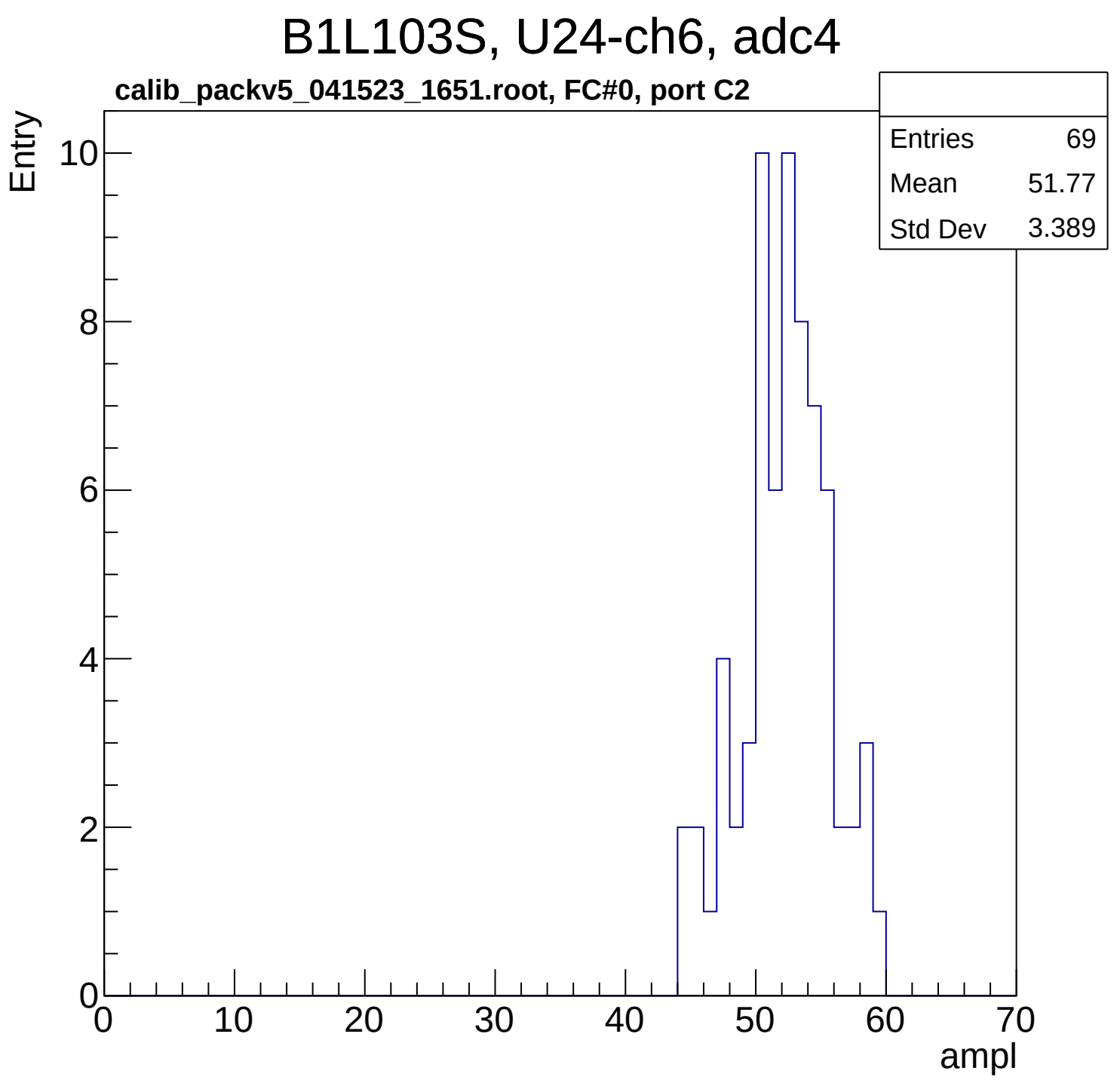
B1L103S, U24-ch6, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 51.77
Std Dev 3.389
Entry
ampl
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4
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8
10
0
10
20
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40
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60
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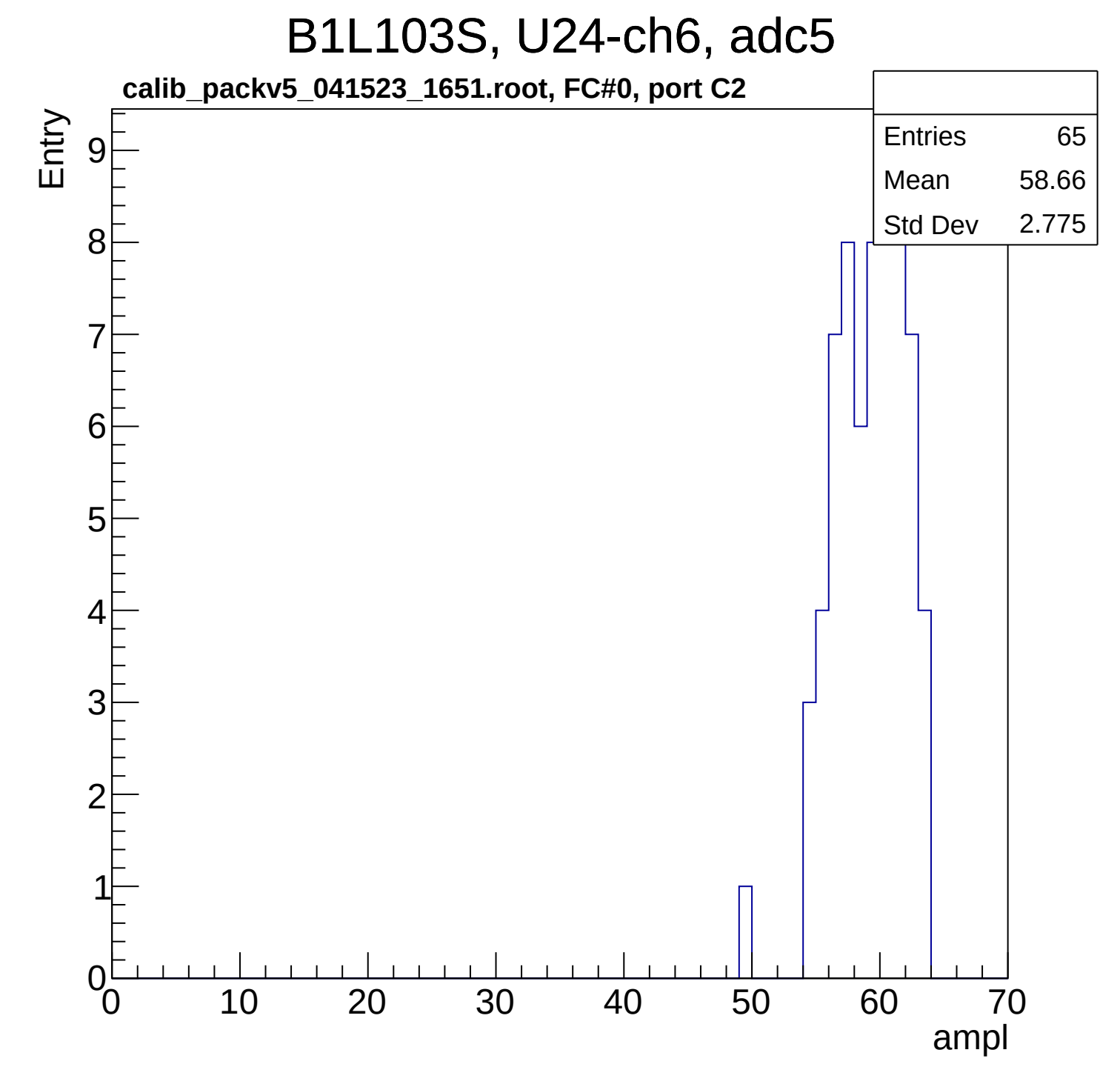
B1L103S, U24-ch6, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 58.66
Std Dev 2.775
Entry
ampl
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2
3
4
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6
7
8
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0
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60
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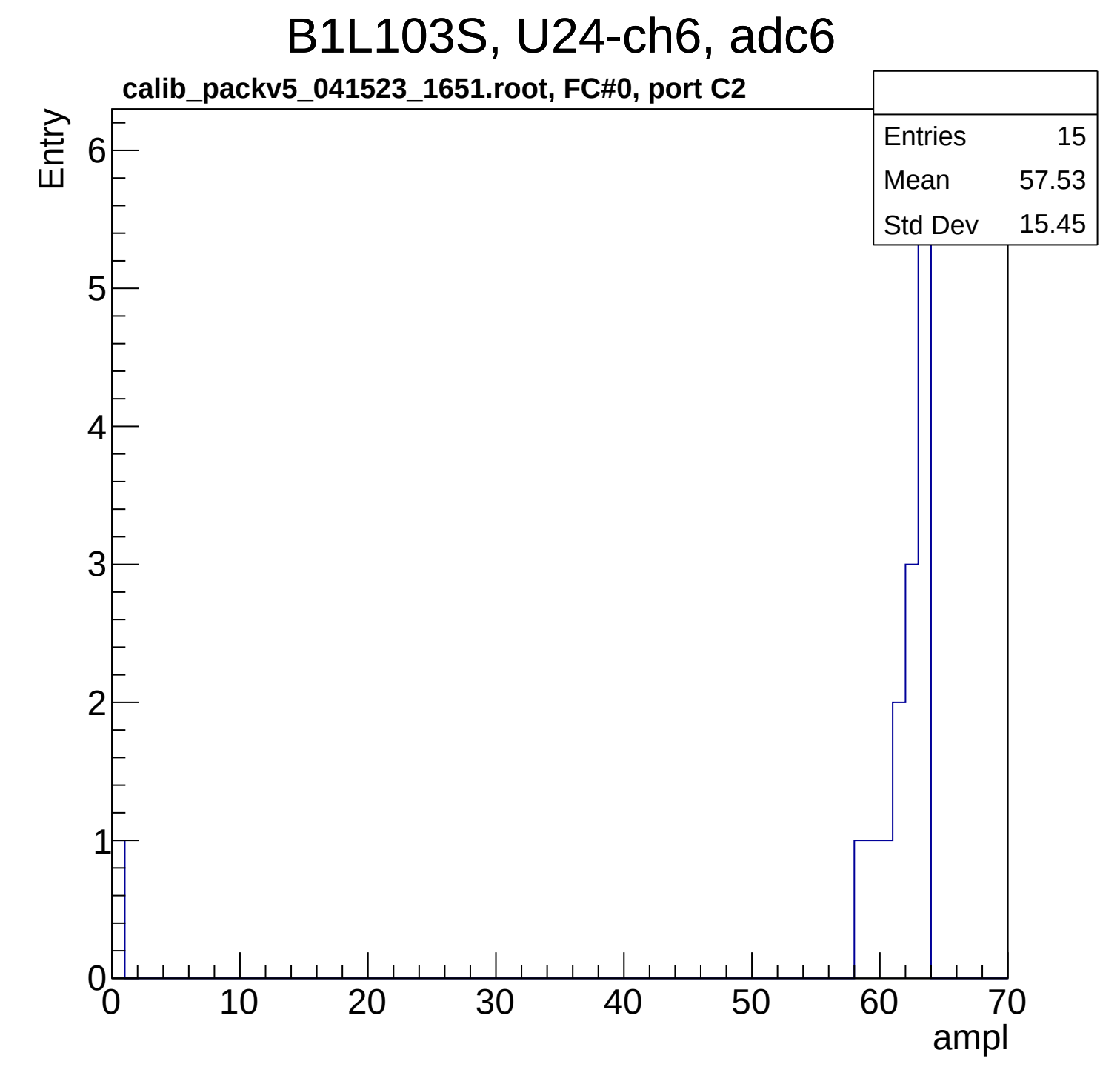
B1L103S, U24-ch6, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 15
Mean 57.53
Std Dev 15.45
Entry
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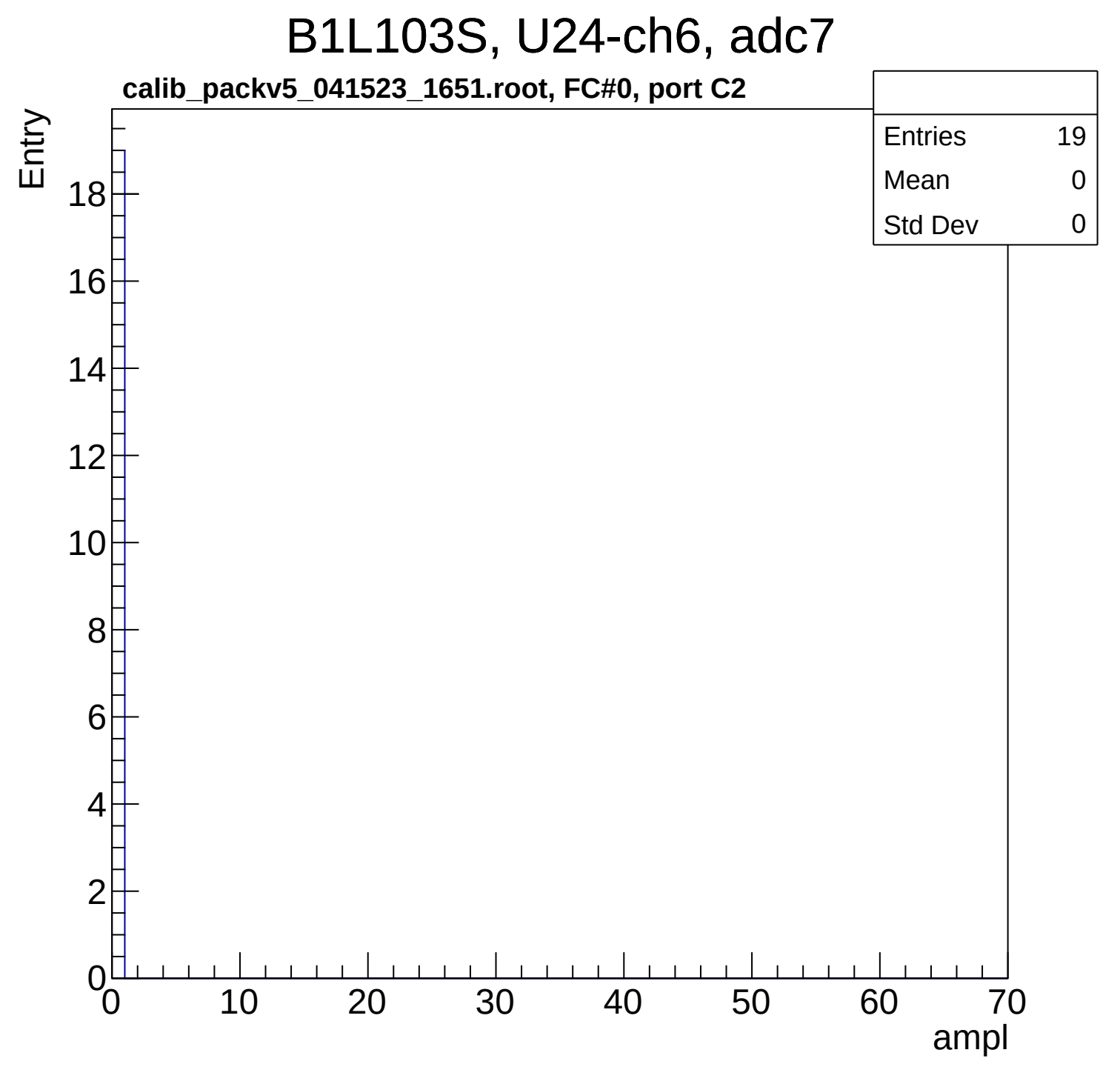
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch6, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
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2
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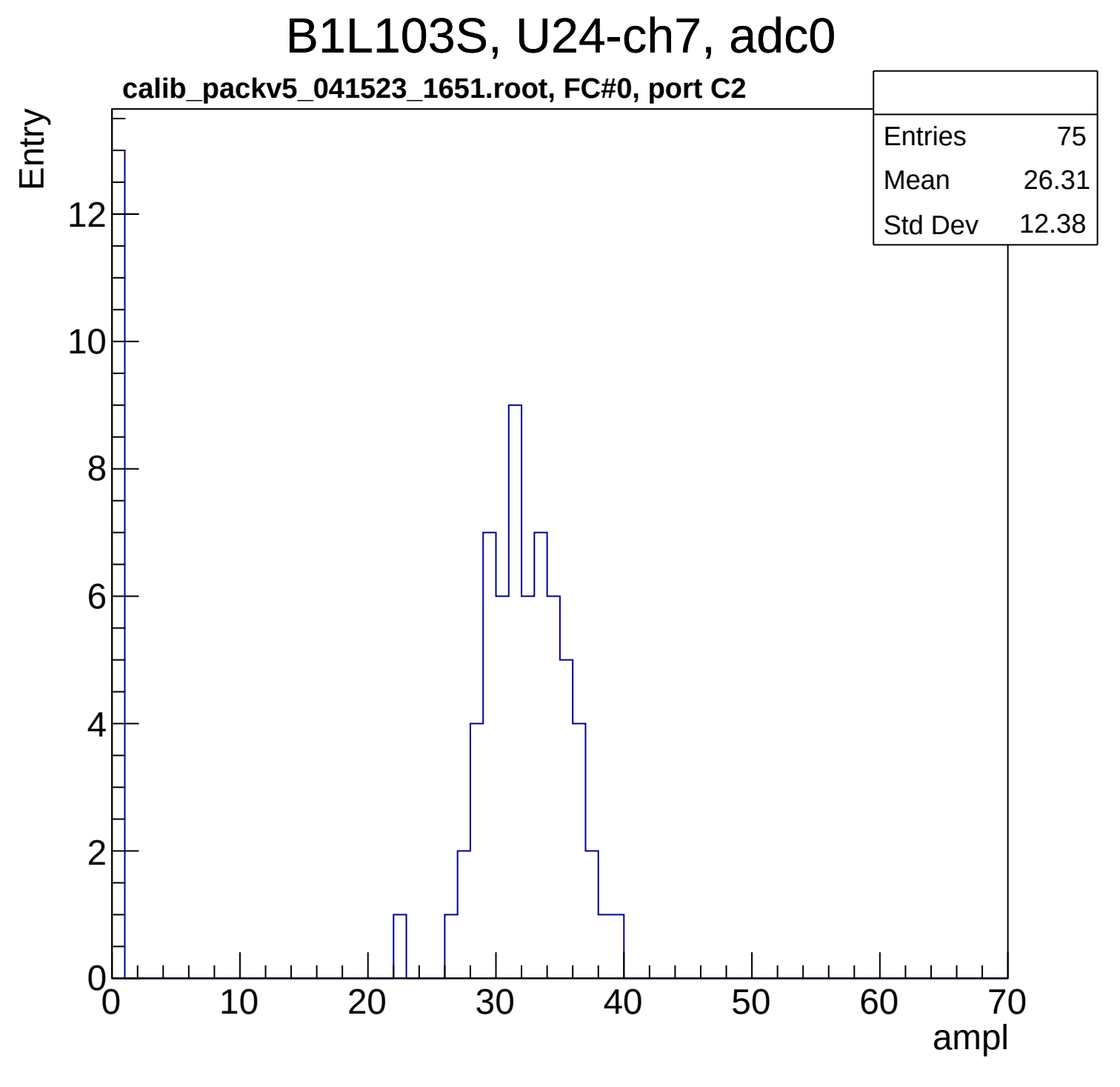
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch7, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 26.31
Std Dev 12.38
Entry
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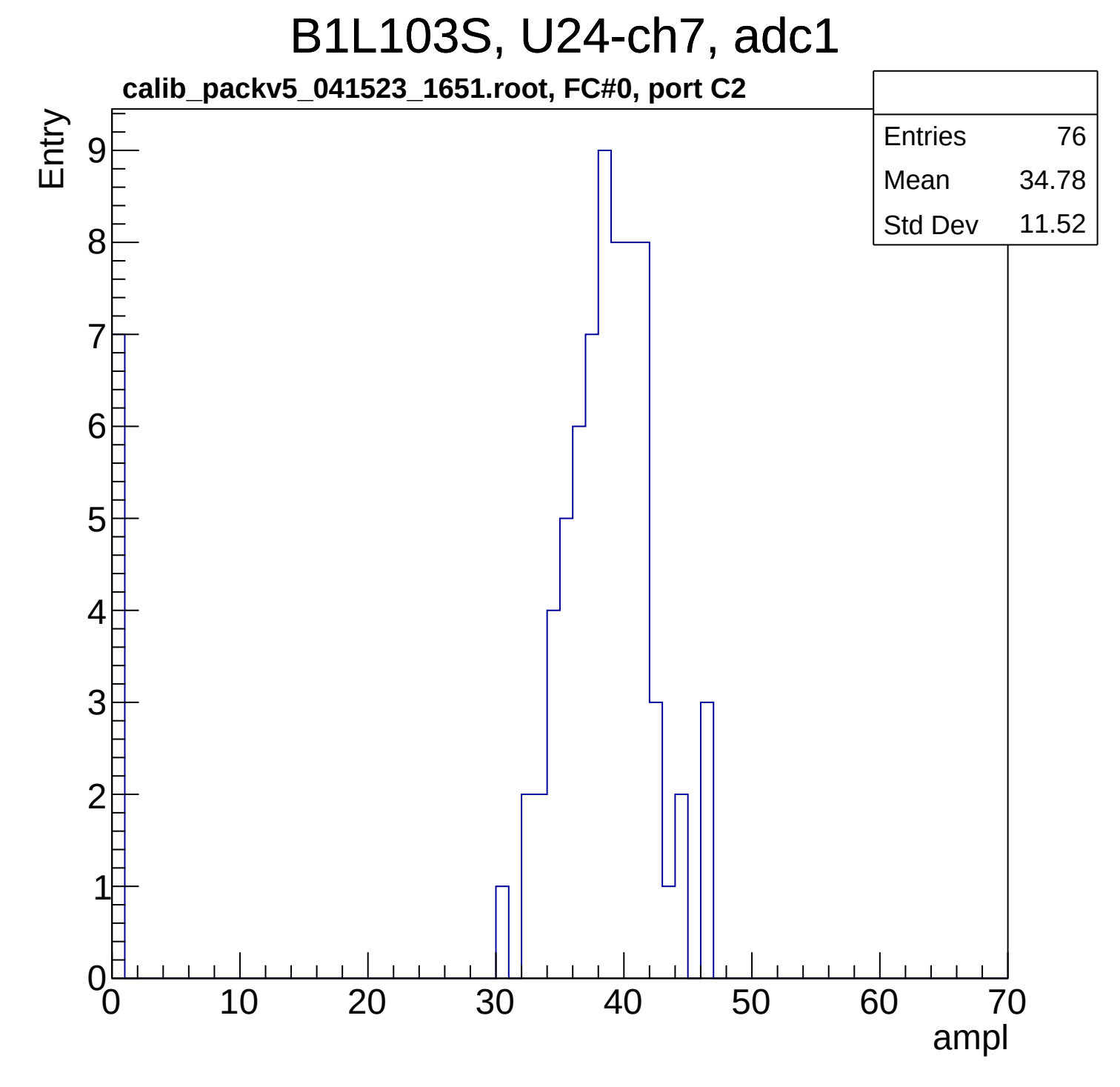
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch7, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 34.78
Std Dev 11.52
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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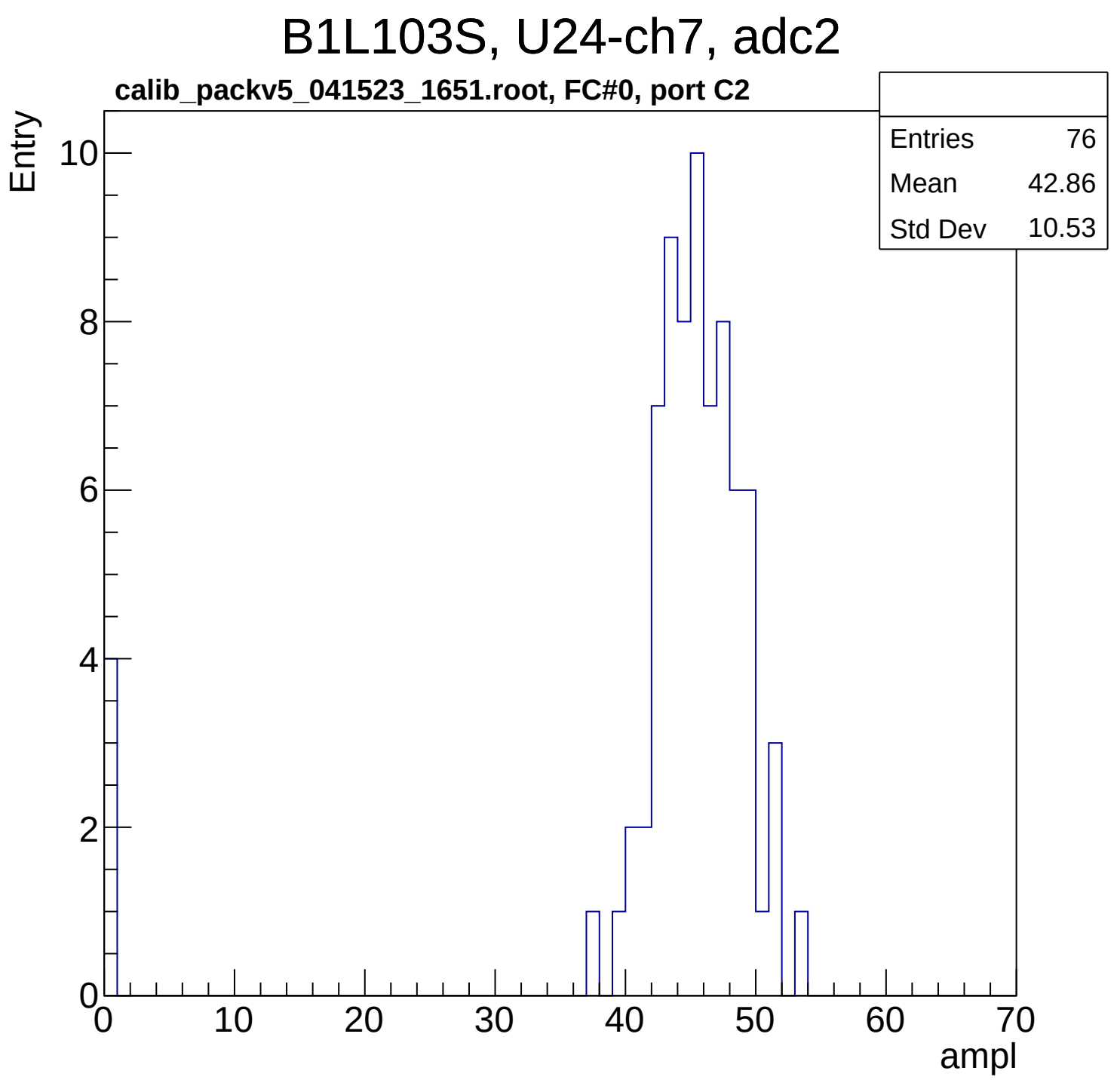
40
50
60
70


B1L103S, U24-ch7, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 42.86
Std Dev 10.53
Entry
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8
10
0
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20
30
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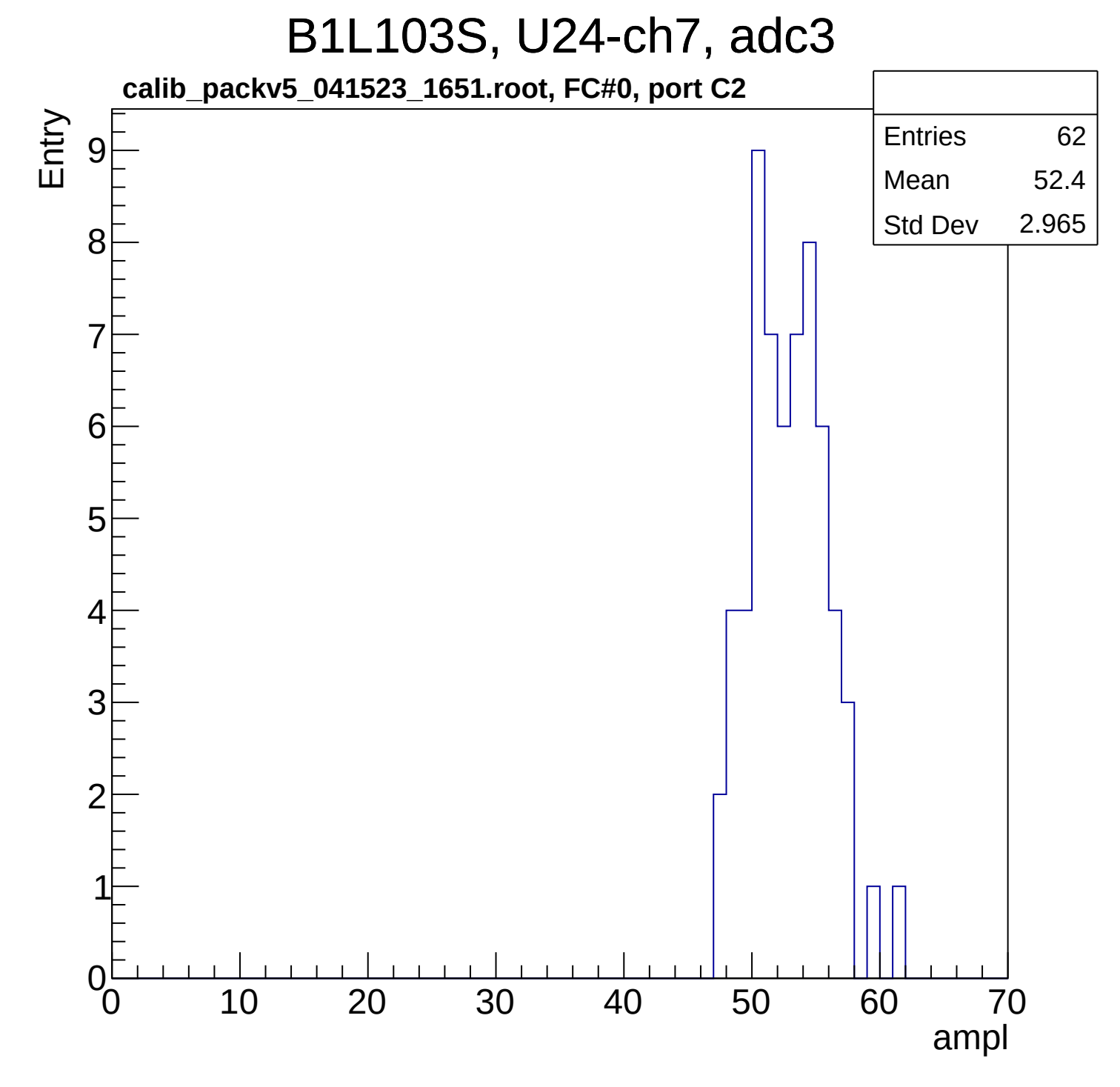
50
60
70
ampl


B1L103S, U24-ch7, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 52.4
Std Dev 2.965
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
50
60
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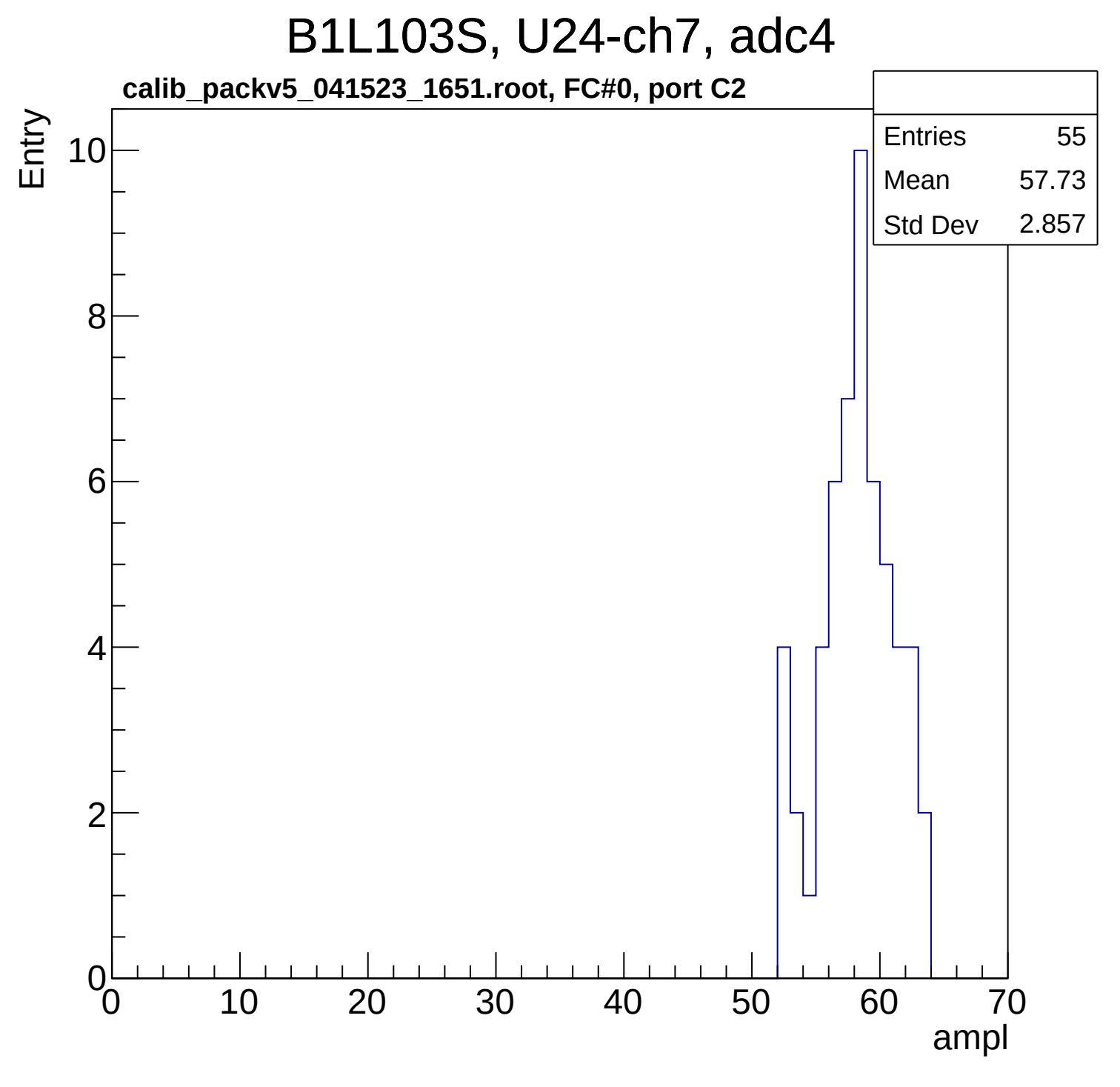
B1L103S, U24-ch7, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 57.73
Std Dev 2.857
Entry
ampl
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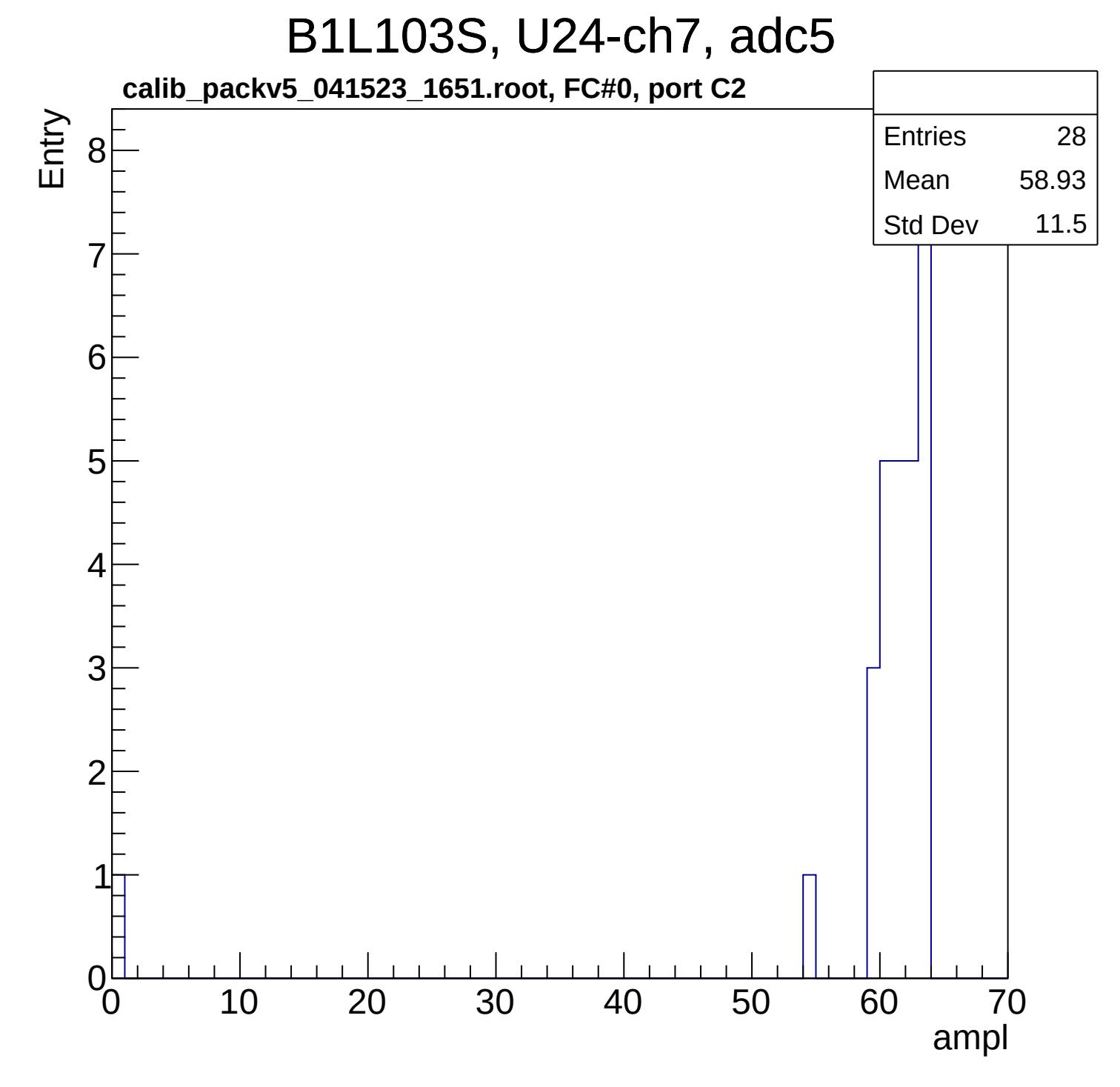
30
40
50
60
70


B1L103S, U24-ch7, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 28
Mean 58.93
Std Dev 11.5
Entry
ampl
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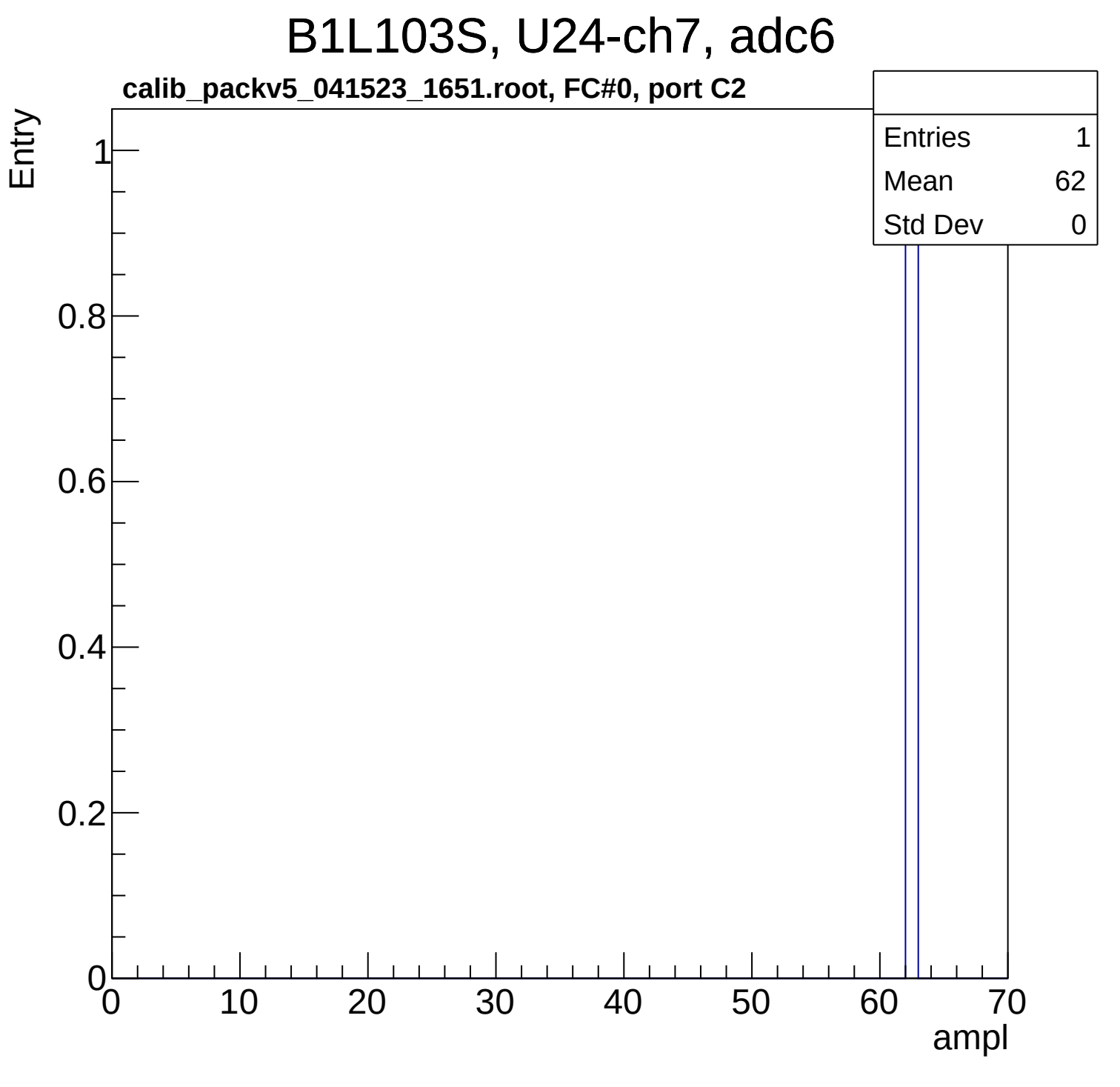
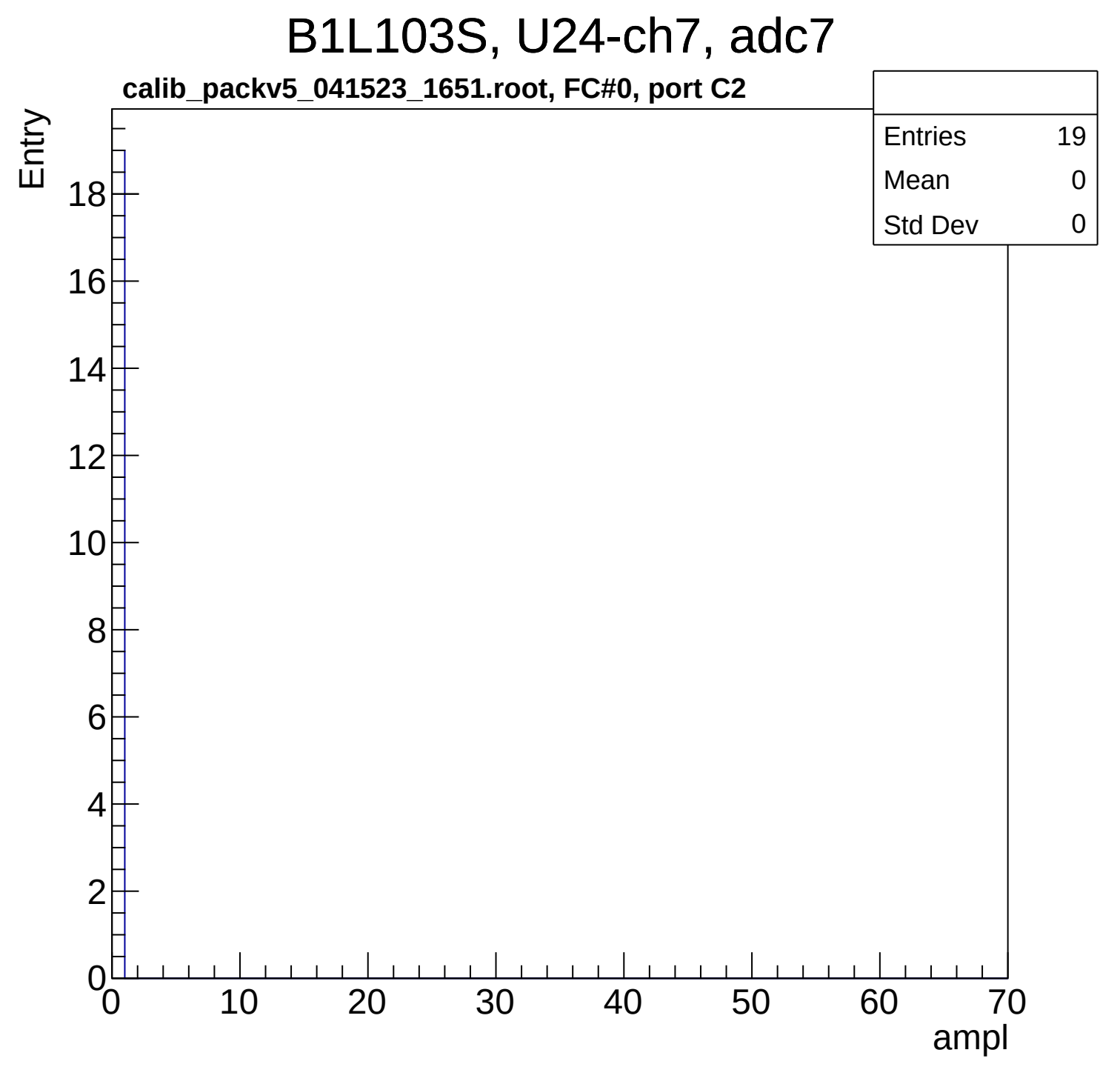
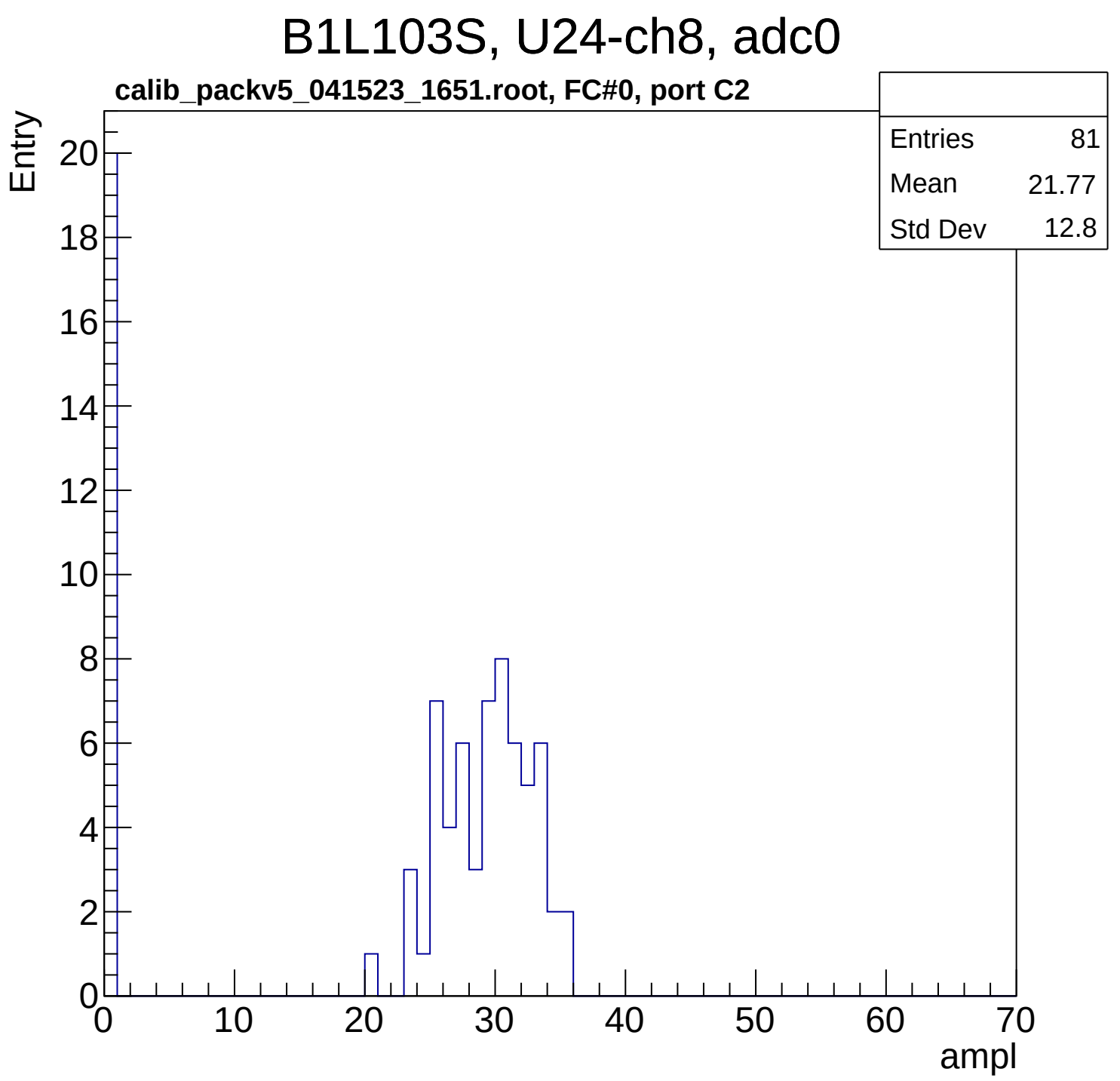
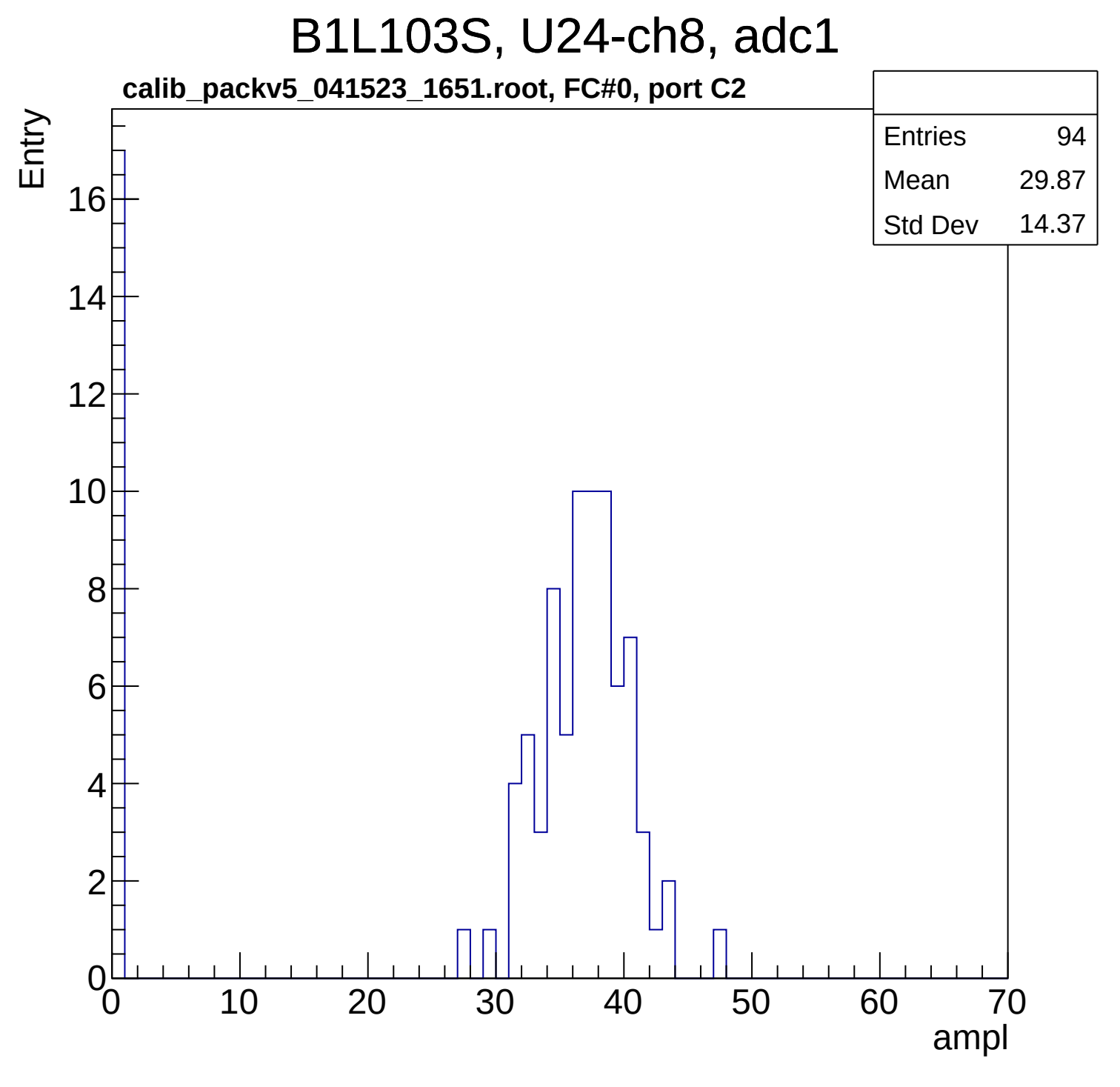
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U24-ch7, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 1
Mean 62
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch7, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch8, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 21.77
Std Dev 12.8
Entry
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch8, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 94
Mean 29.87
Std Dev 14.37
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
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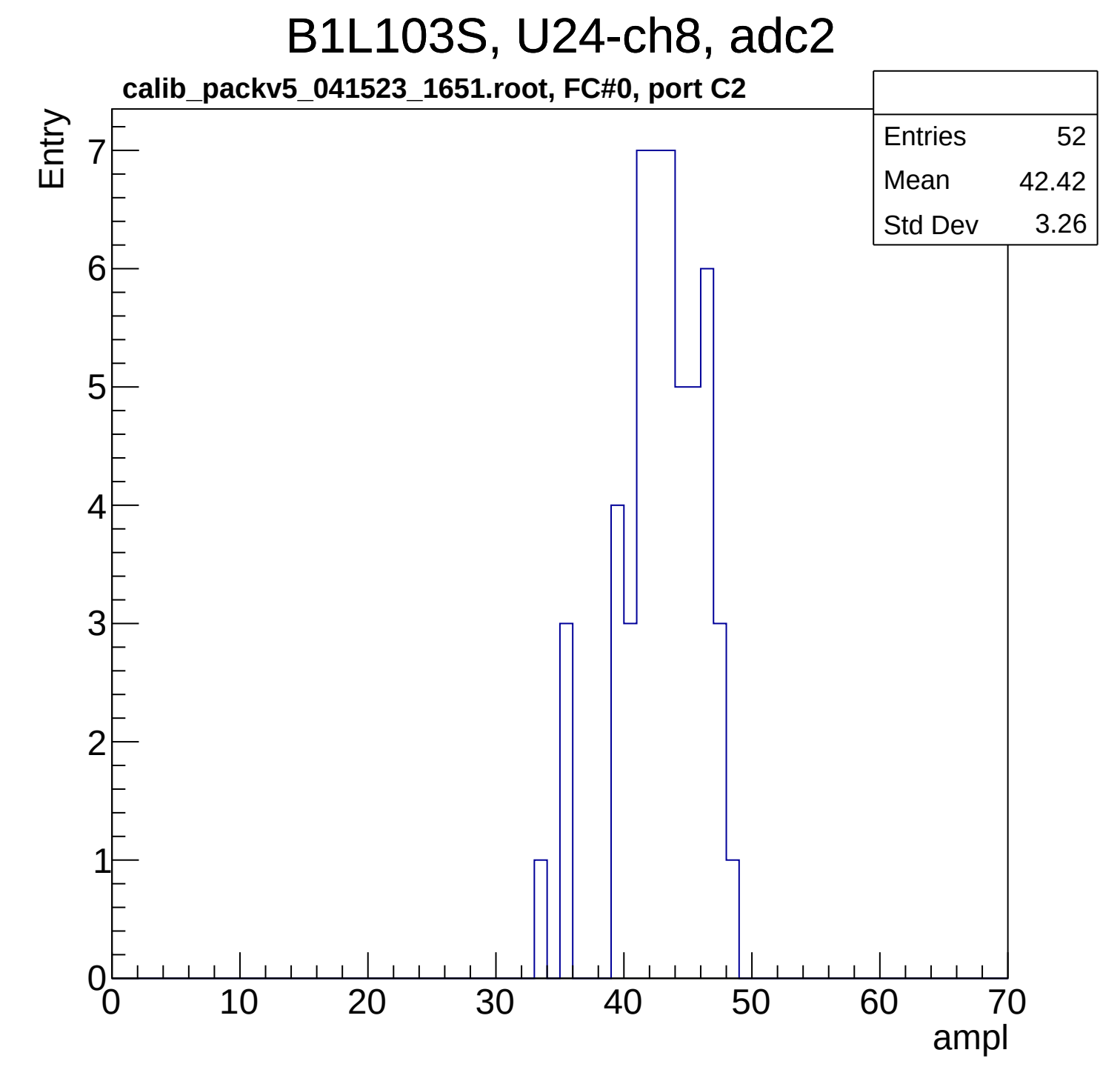
60
70


B1L103S, U24-ch8, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 42.42
Std Dev 3.26
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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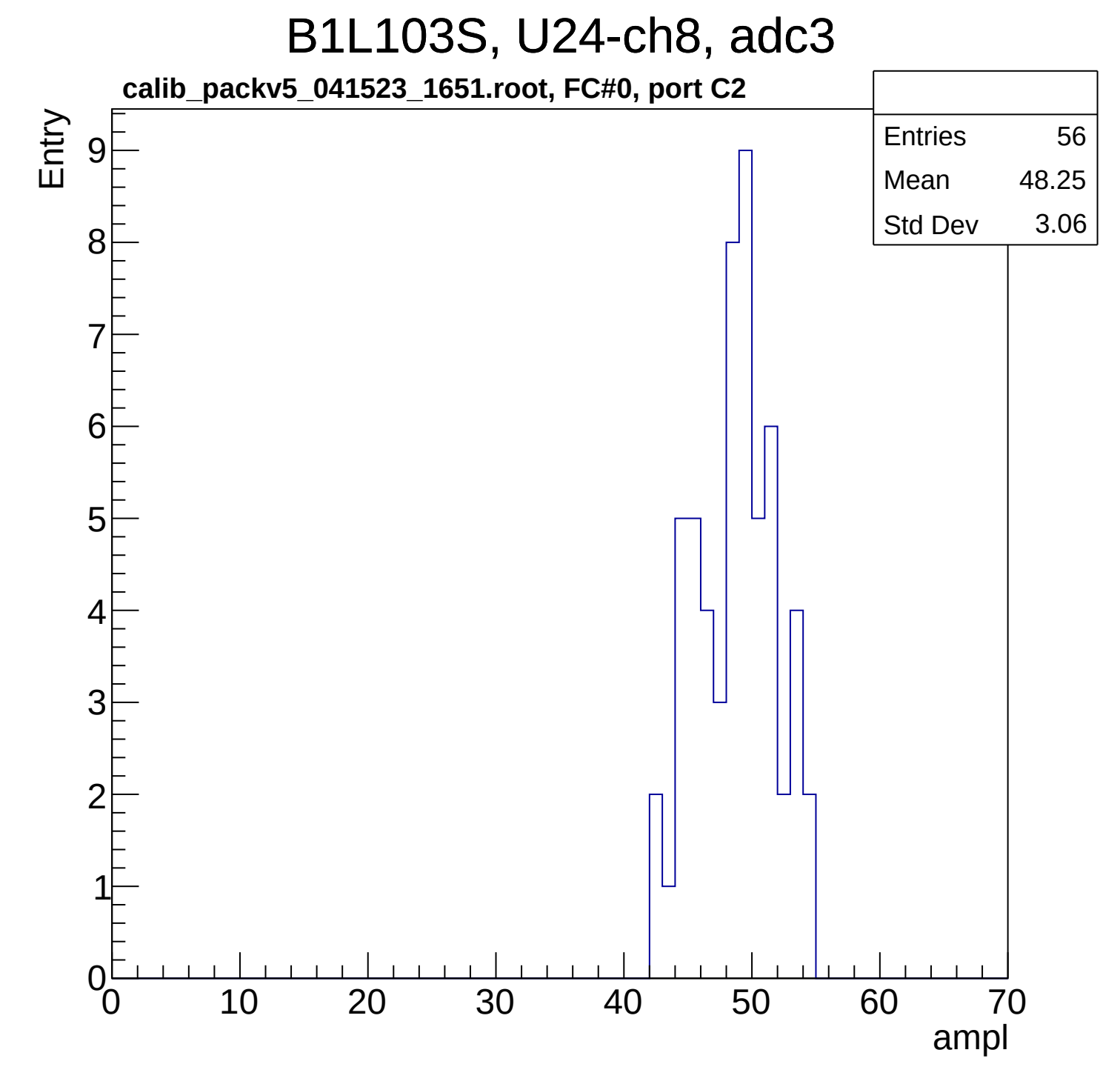
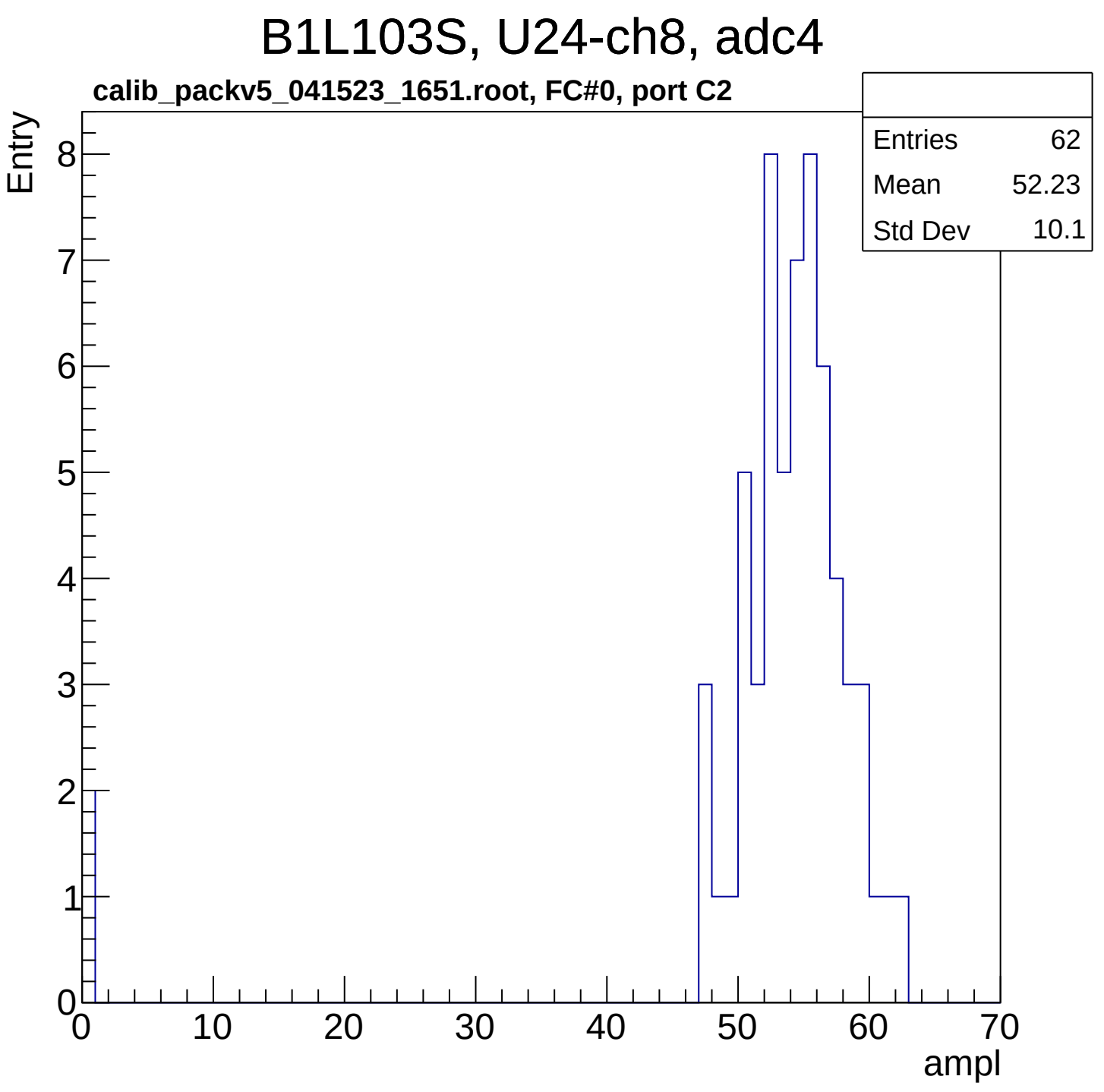
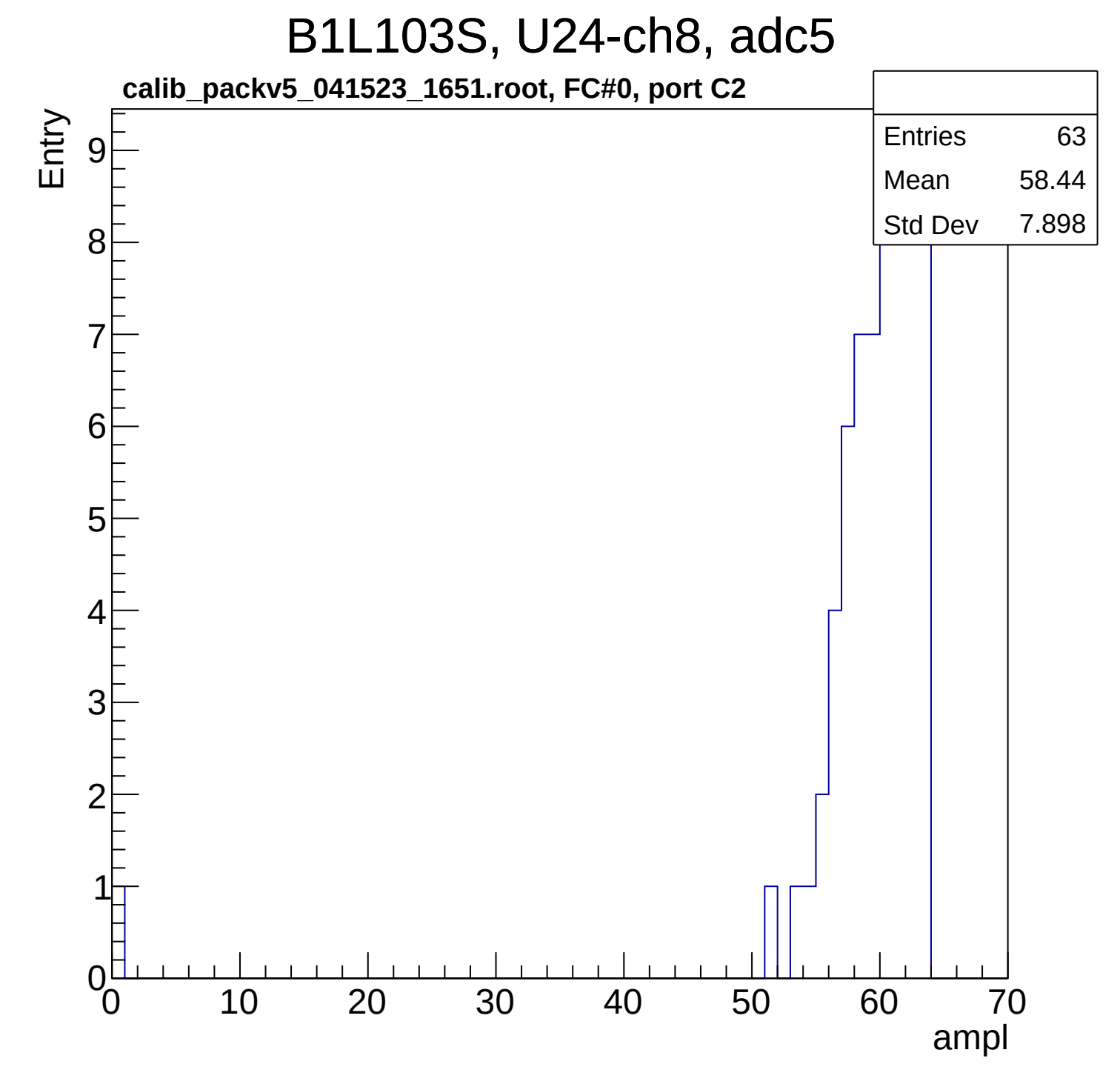
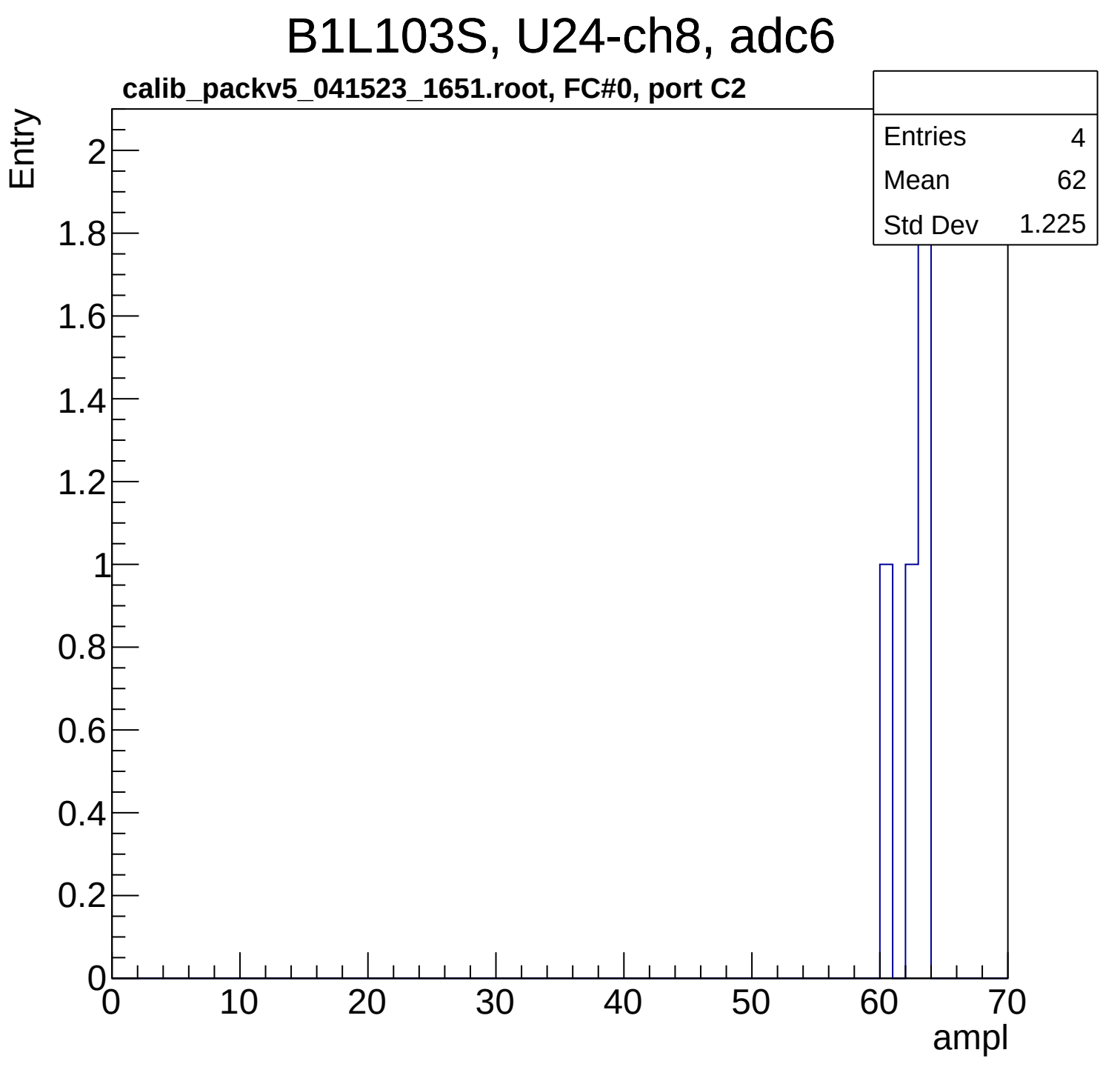
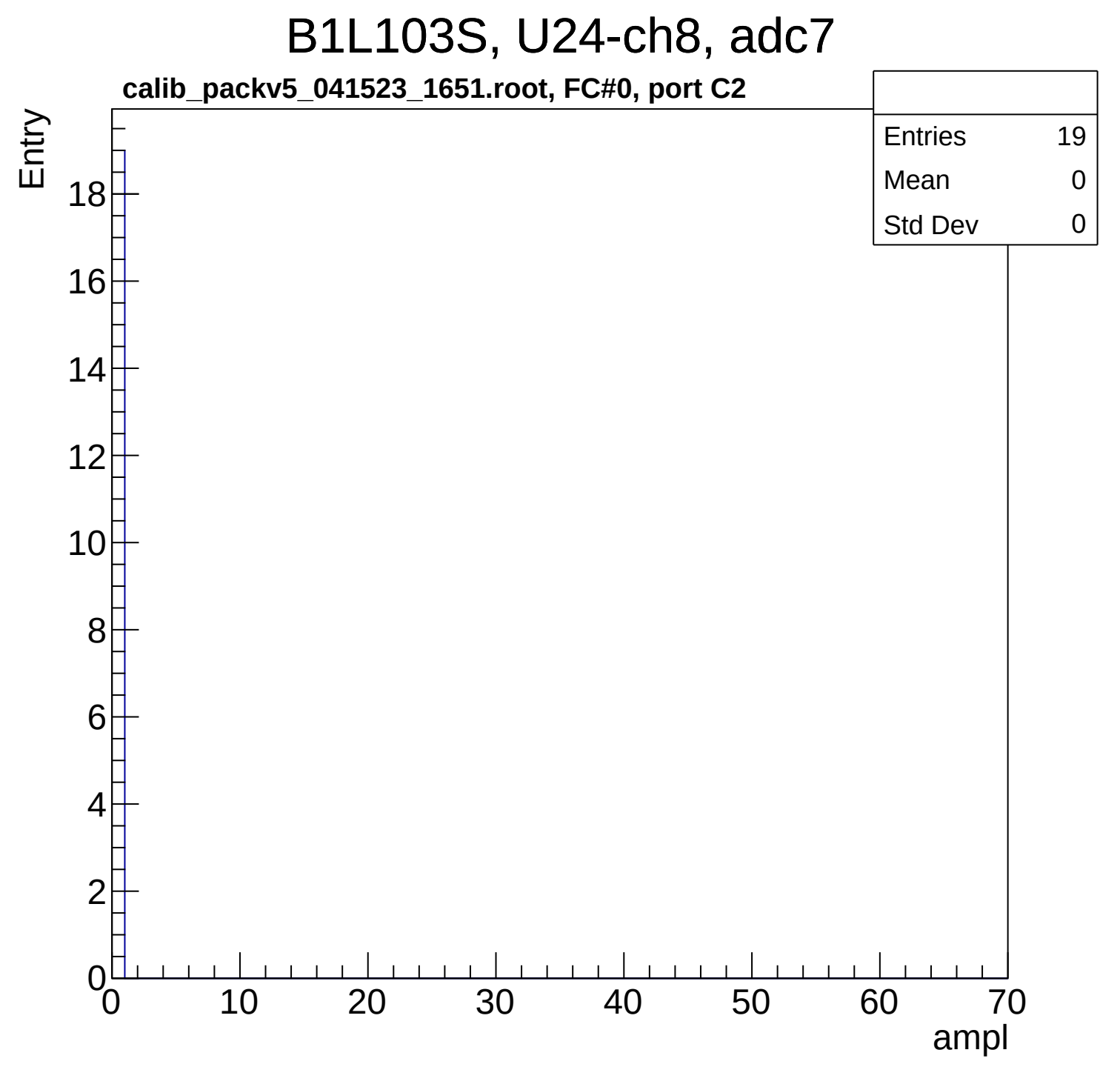
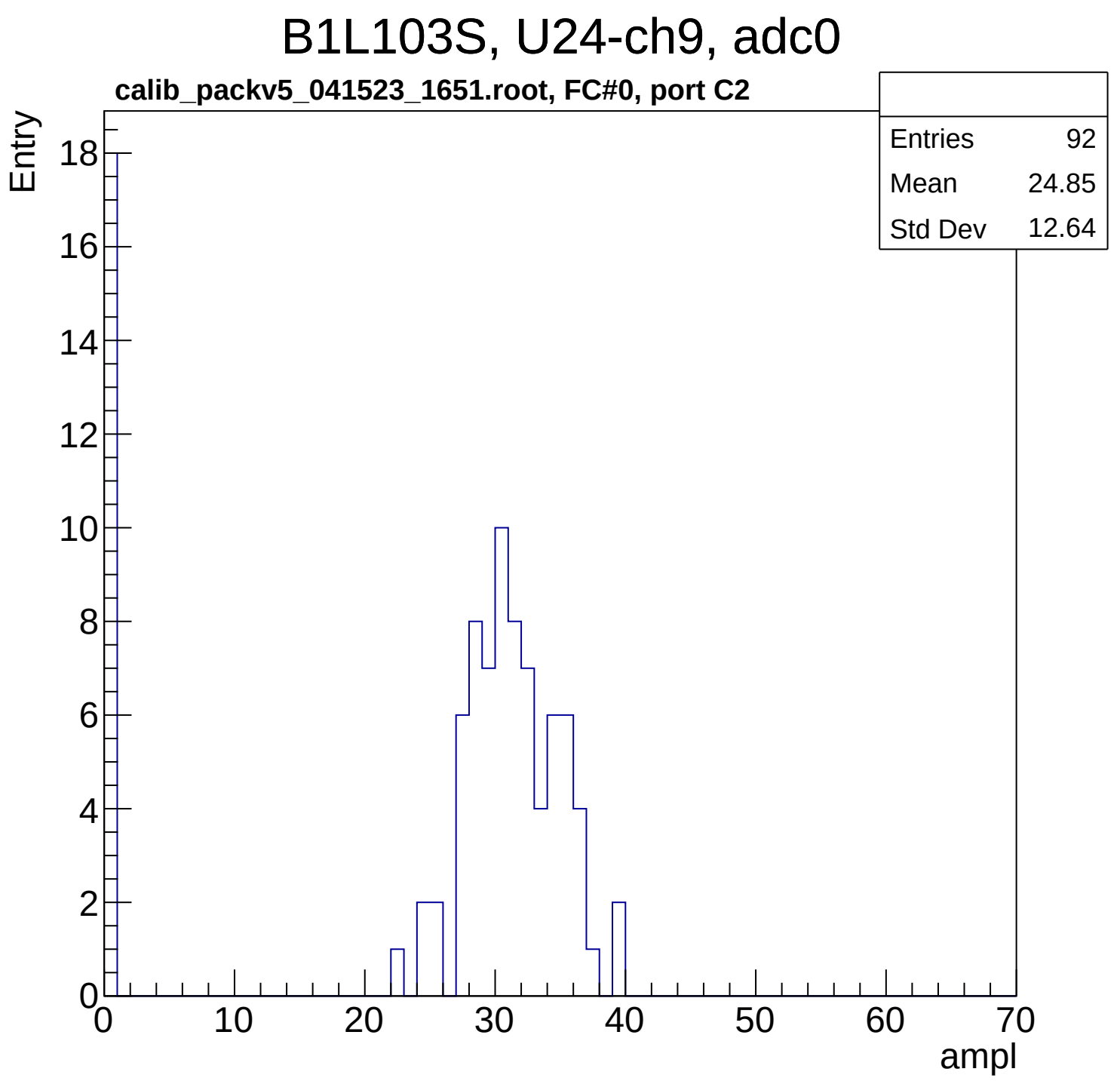

B1L103S, U24-ch8, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 48.25
Std Dev 3.06
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

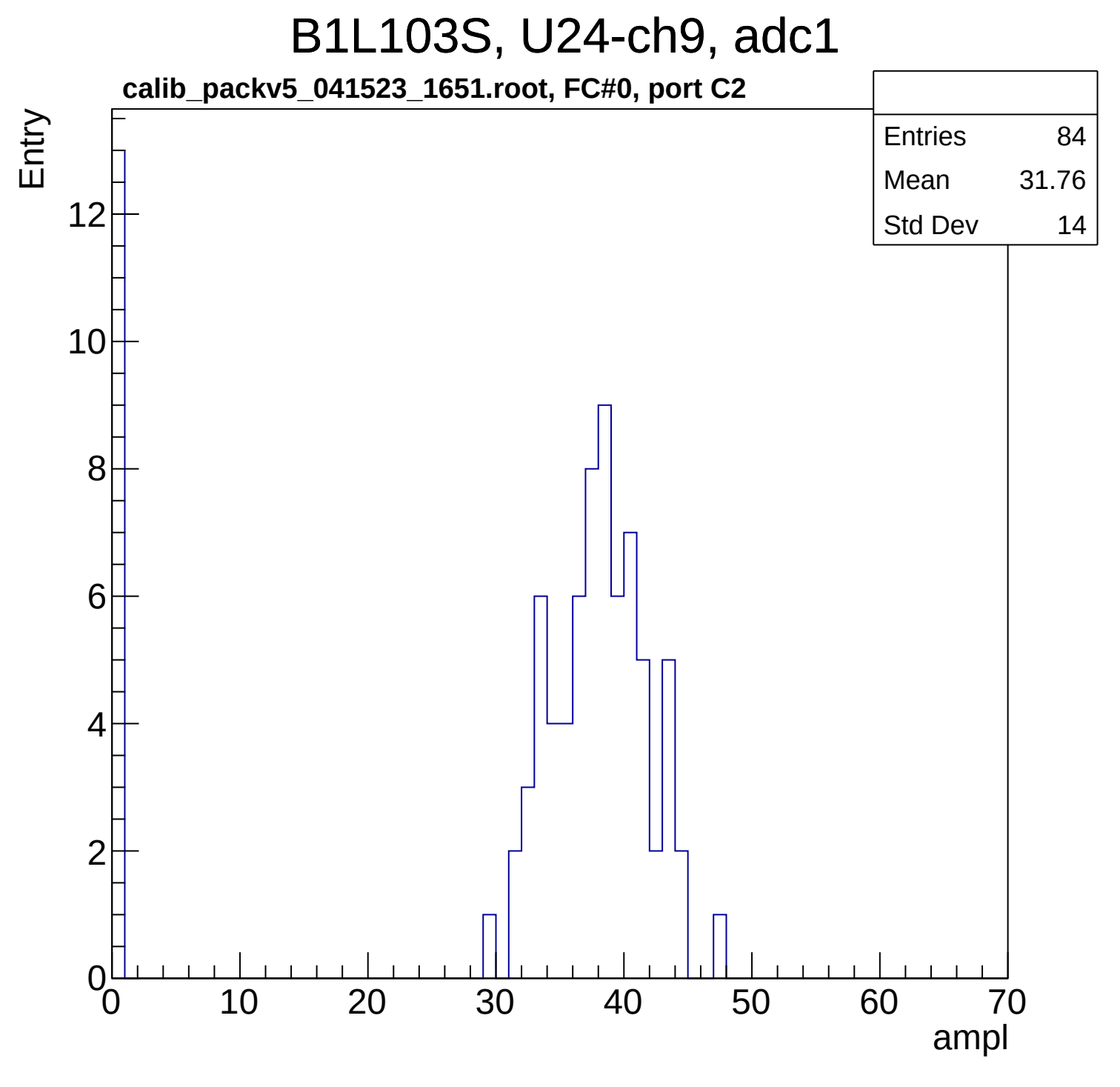

B1L103S, U24-ch8, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 52.23
Std Dev 10.1
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

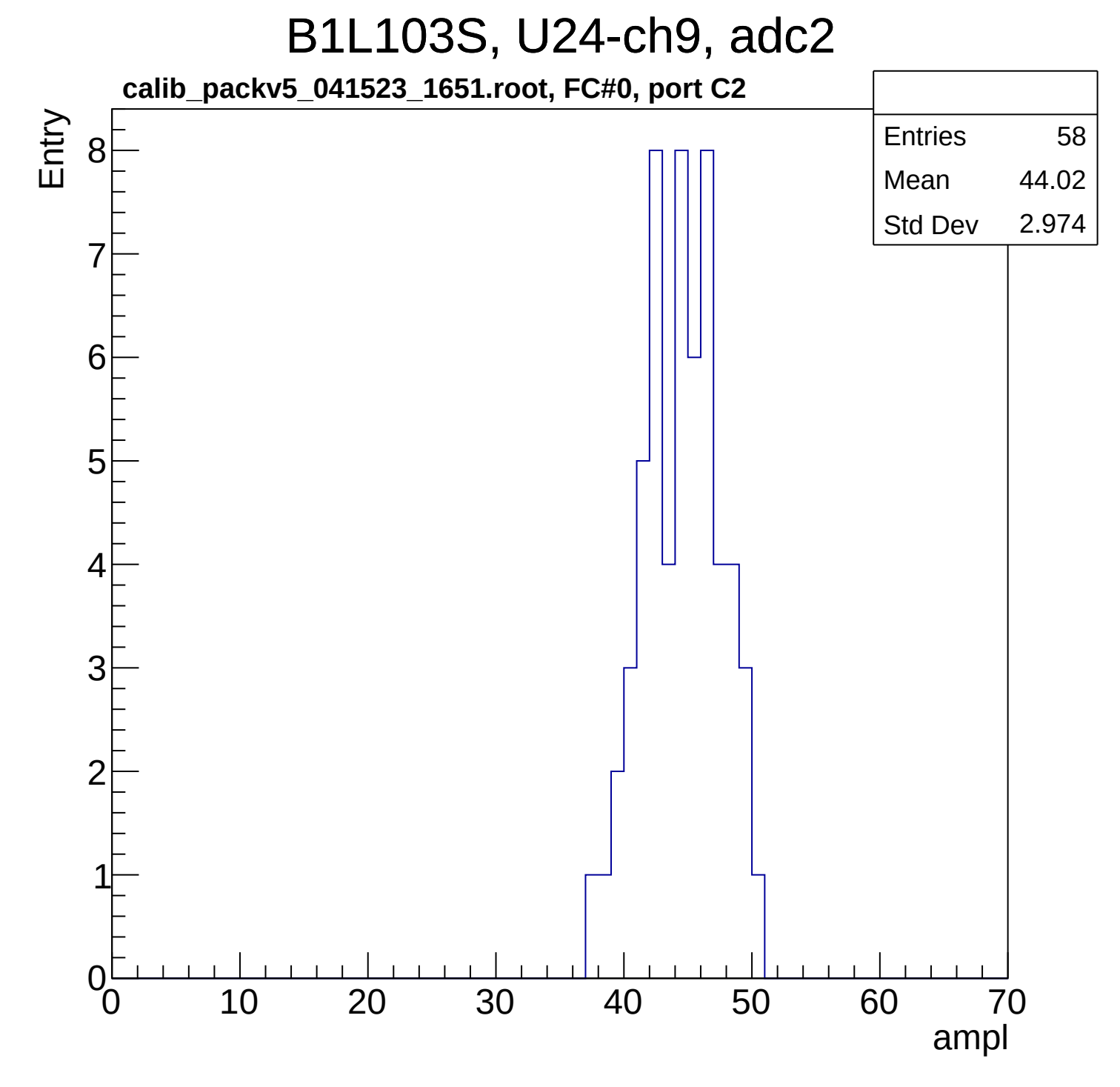

B1L103S, U24-ch8, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 58.44
Std Dev 7.898
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

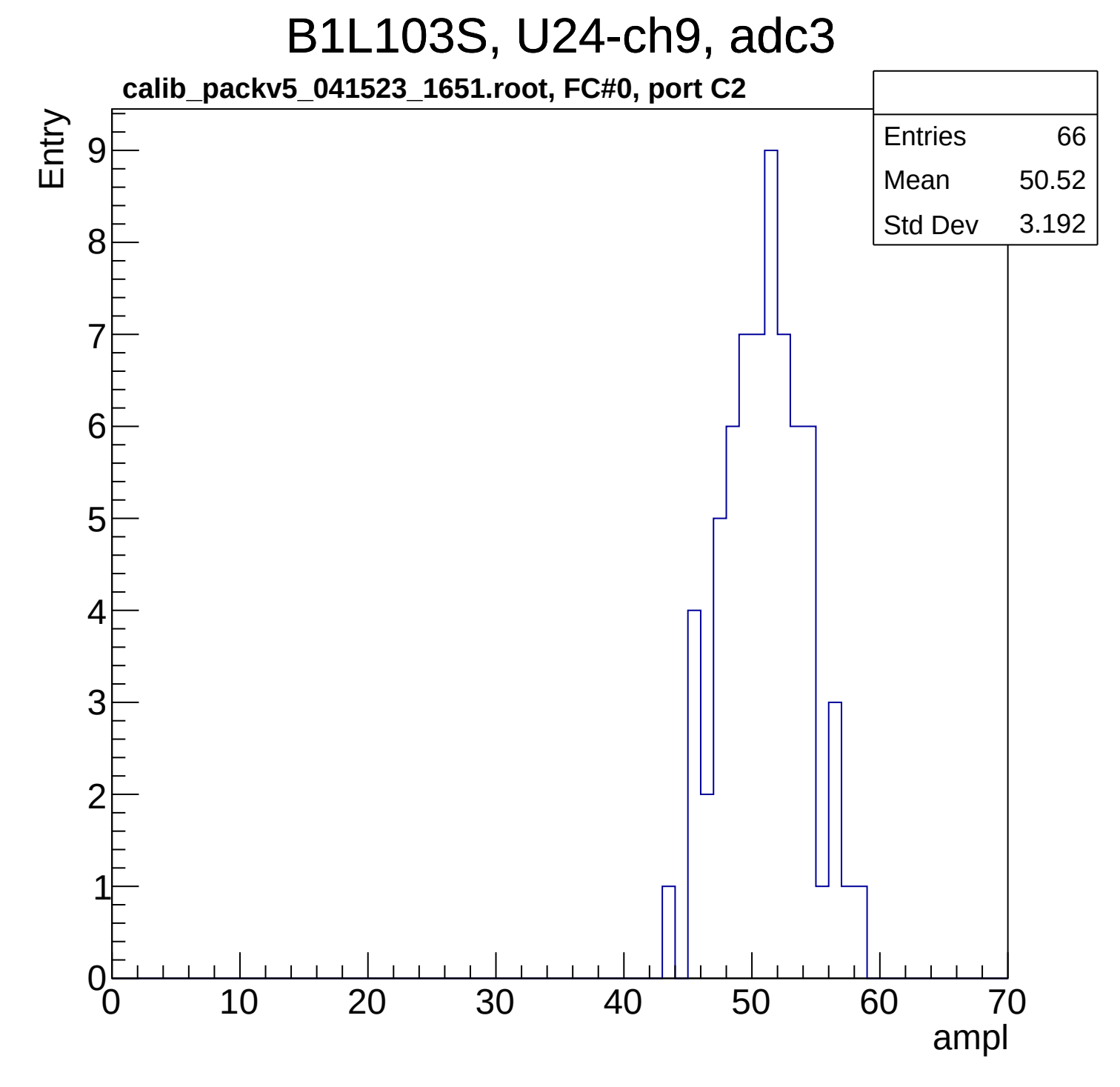

B1L103S, U24-ch8, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 4
Mean 62
Std Dev 1.225
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

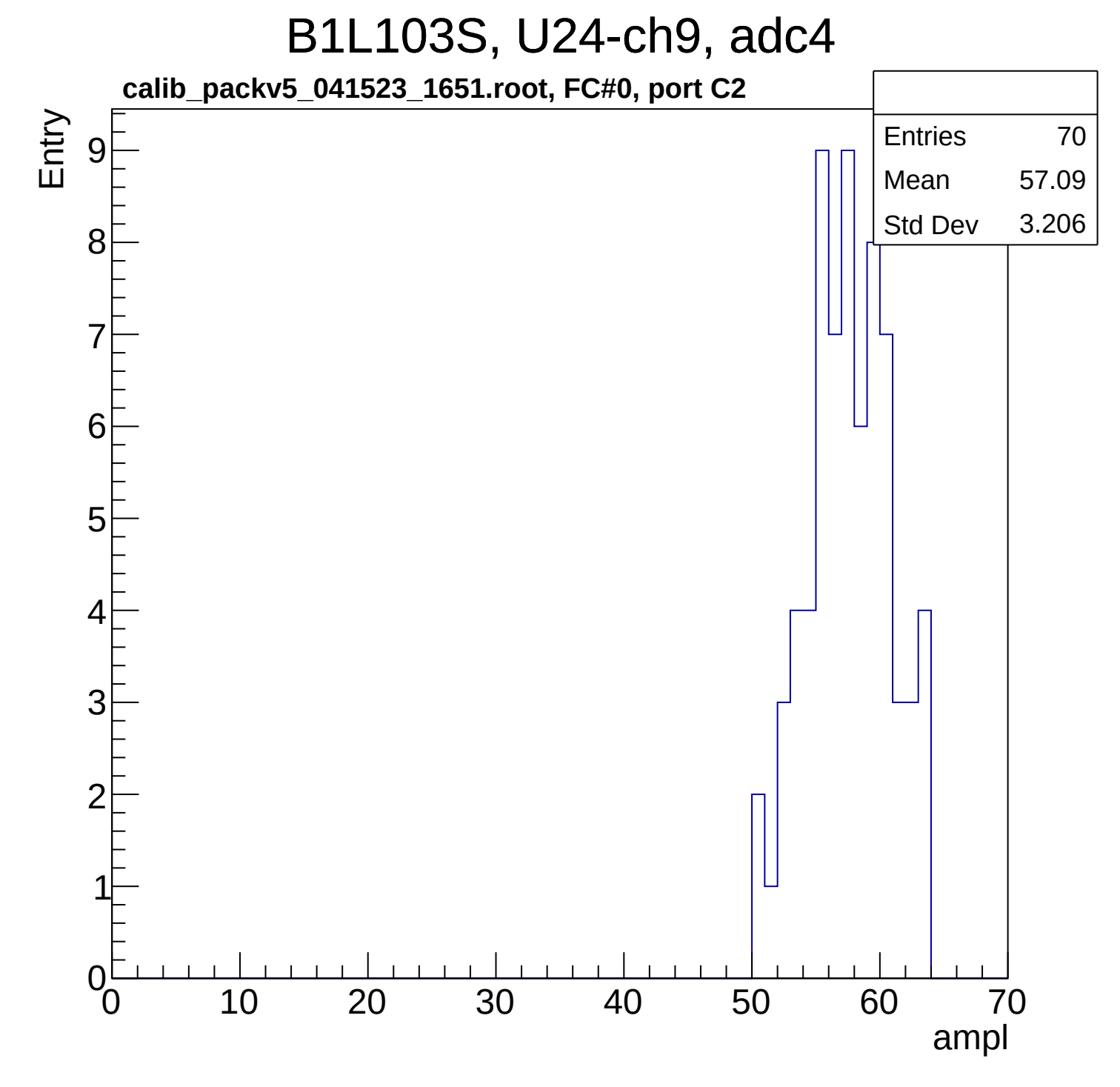

B1L103S, U24-ch8, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

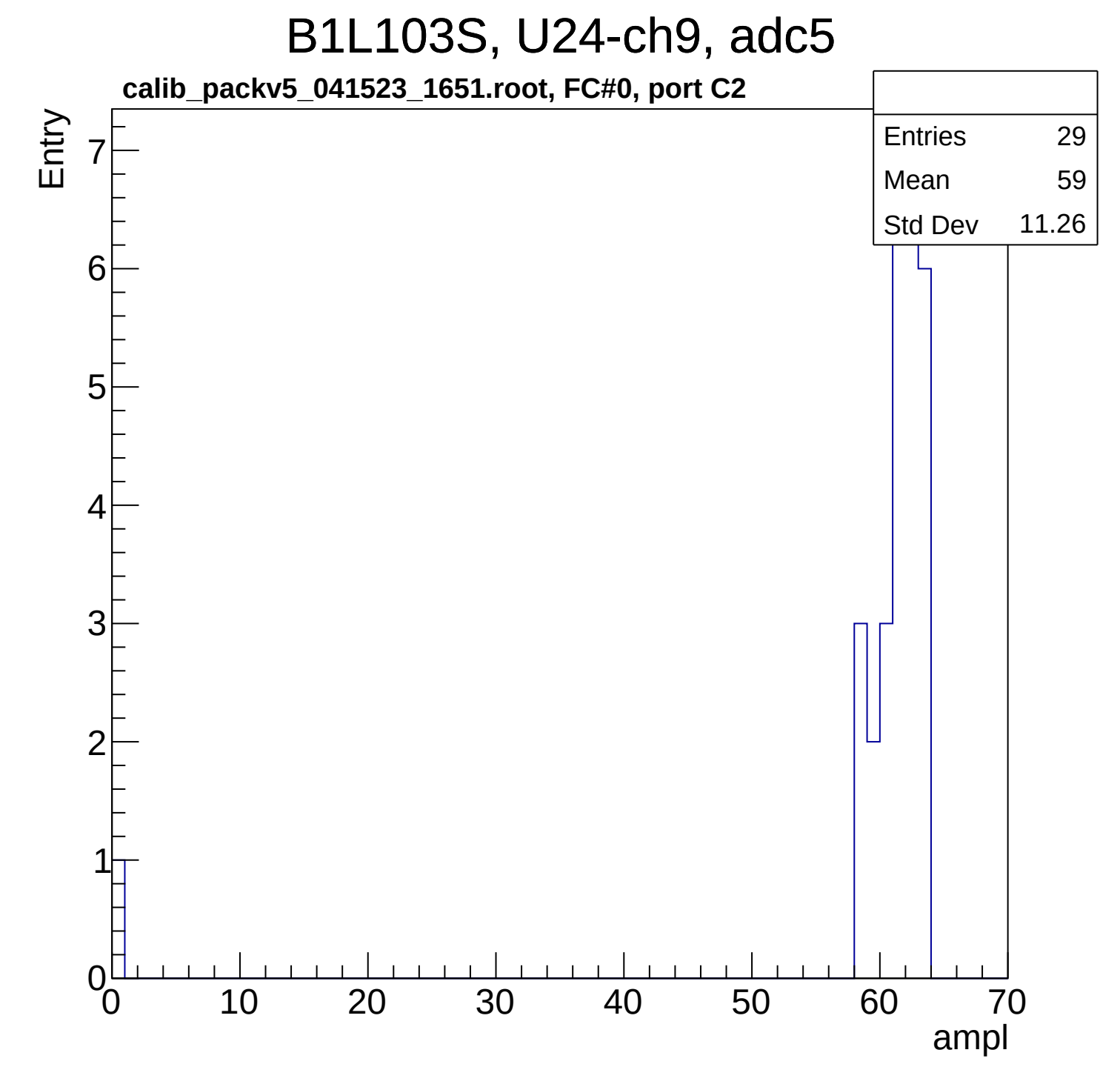

B1L103S, U24-ch9, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 92
Mean 24.85
Std Dev 12.64
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

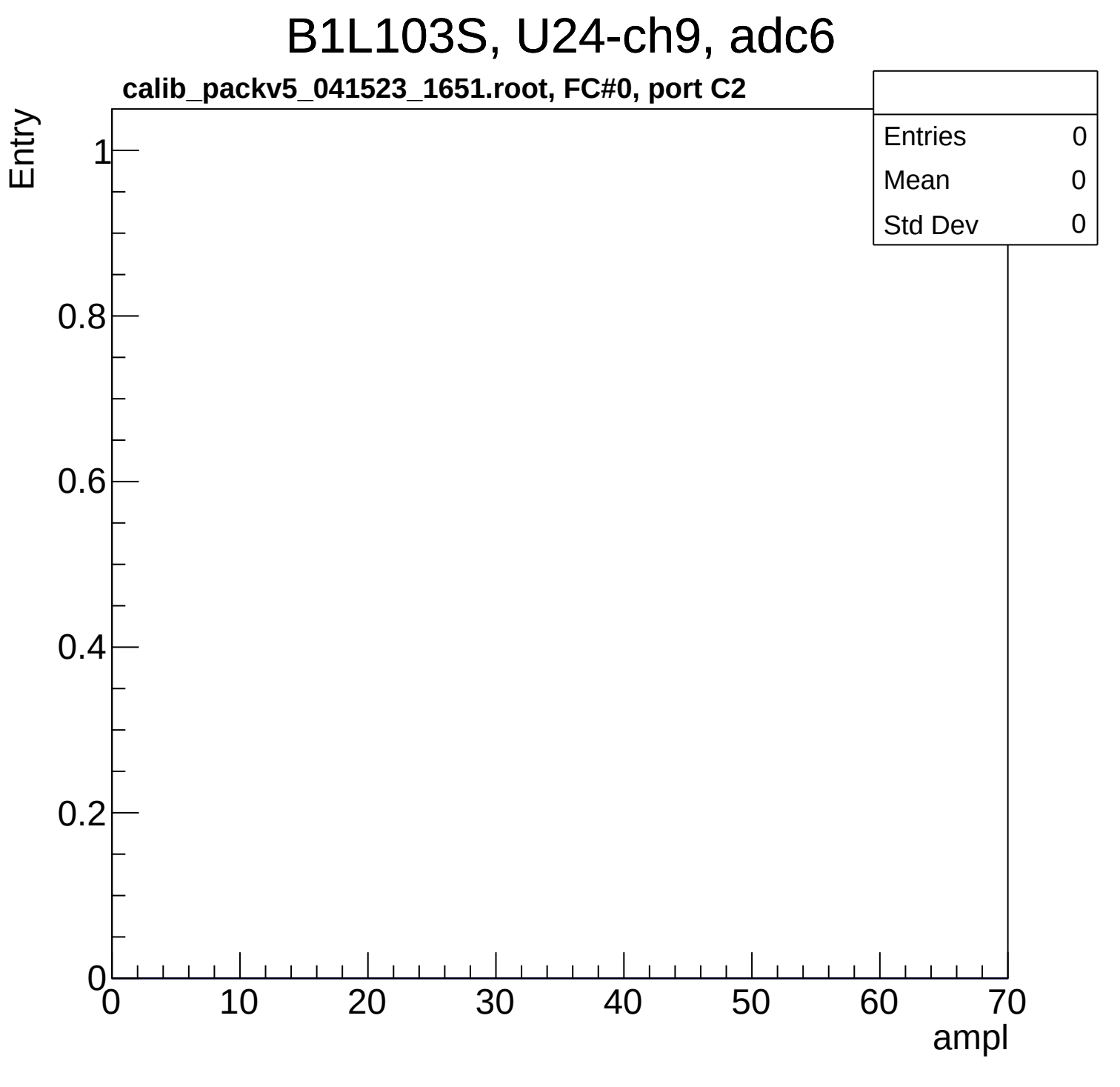

B1L103S, U24-ch9, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 31.76
Std Dev 14
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70

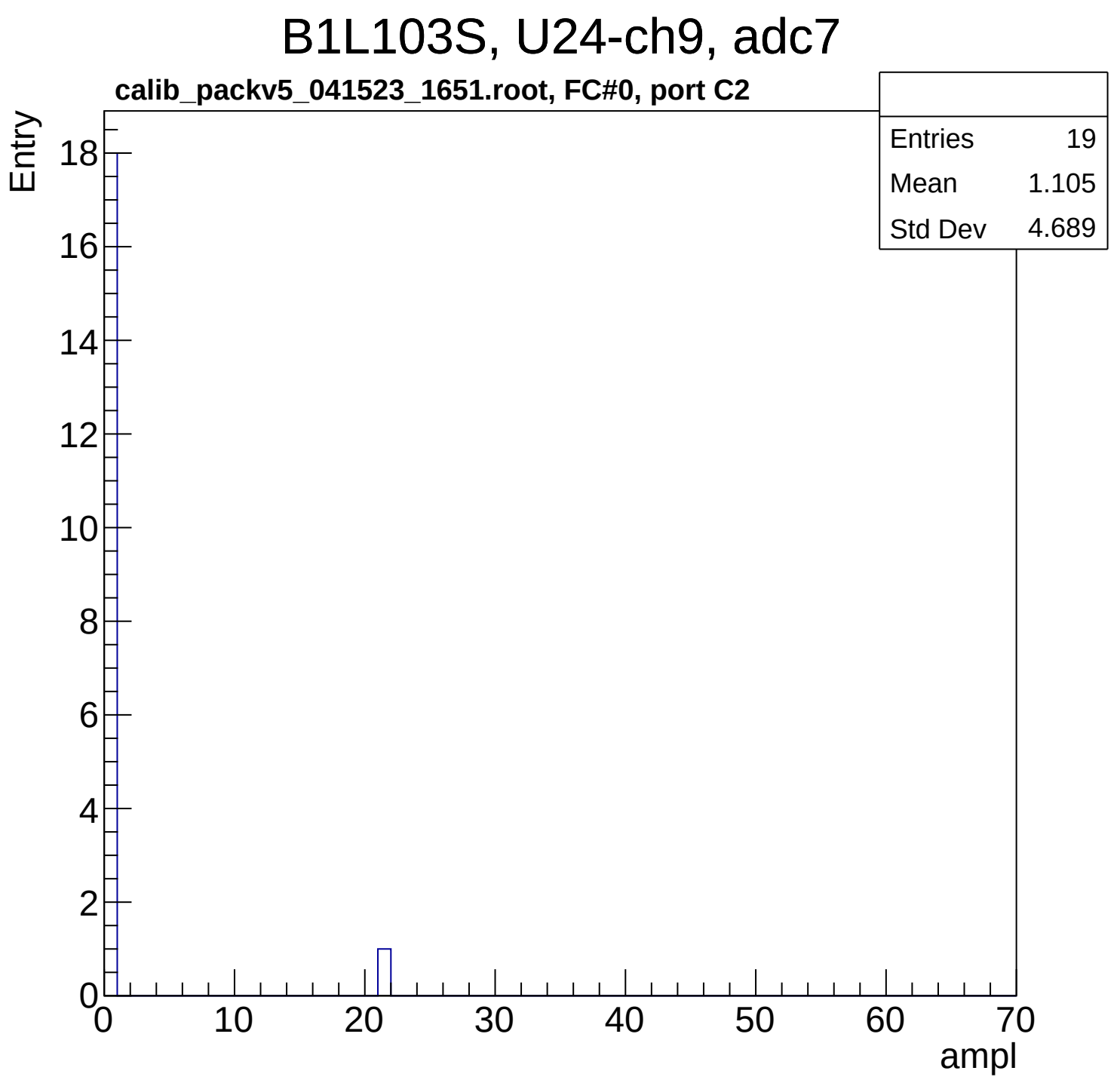

B1L103S, U24-ch9, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 44.02
Std Dev 2.974
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

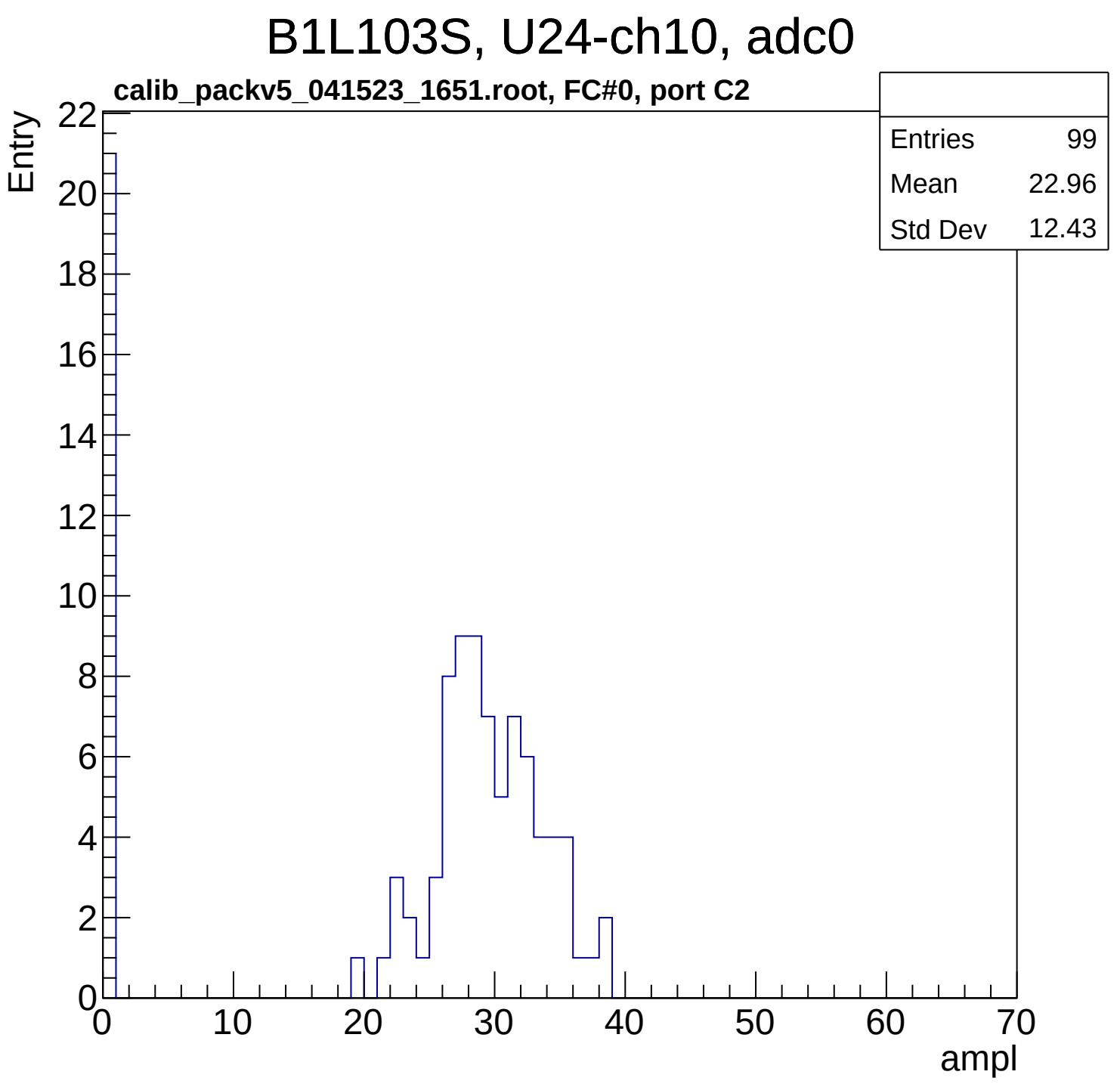

B1L103S, U24-ch9, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 50.52
Std Dev 3.192
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

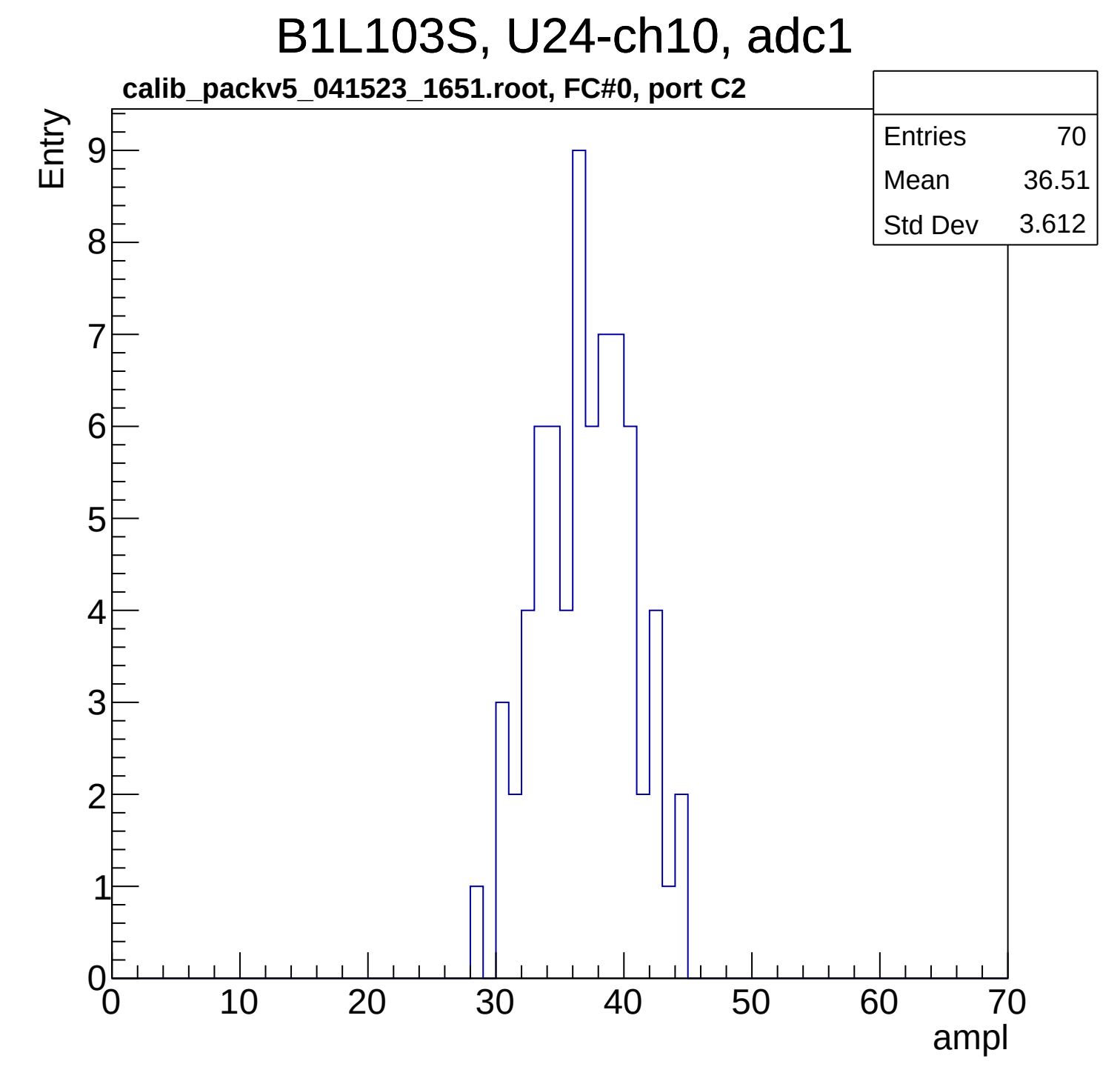

B1L103S, U24-ch9, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 57.09
Std Dev 3.206
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U24-ch9, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 29
Mean 59
Std Dev 11.26
Entry
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch9, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch9, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.105
Std Dev 4.689
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch10, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 99
Mean 22.96
Std Dev 12.43
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
22
0
10
20
30
40
50
60
70


B1L103S, U24-ch10, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 36.51
Std Dev 3.612
Entry
ampl
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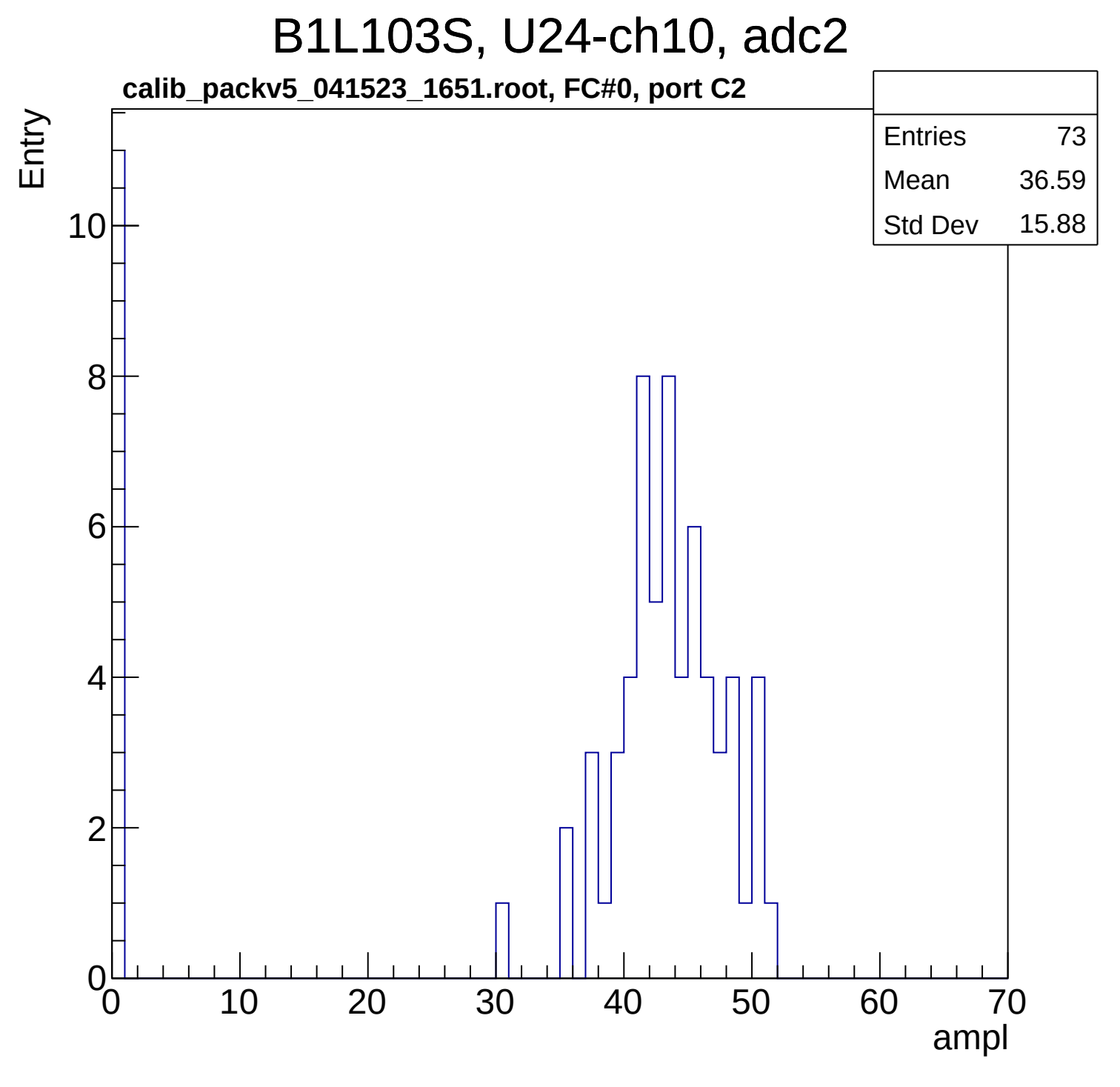
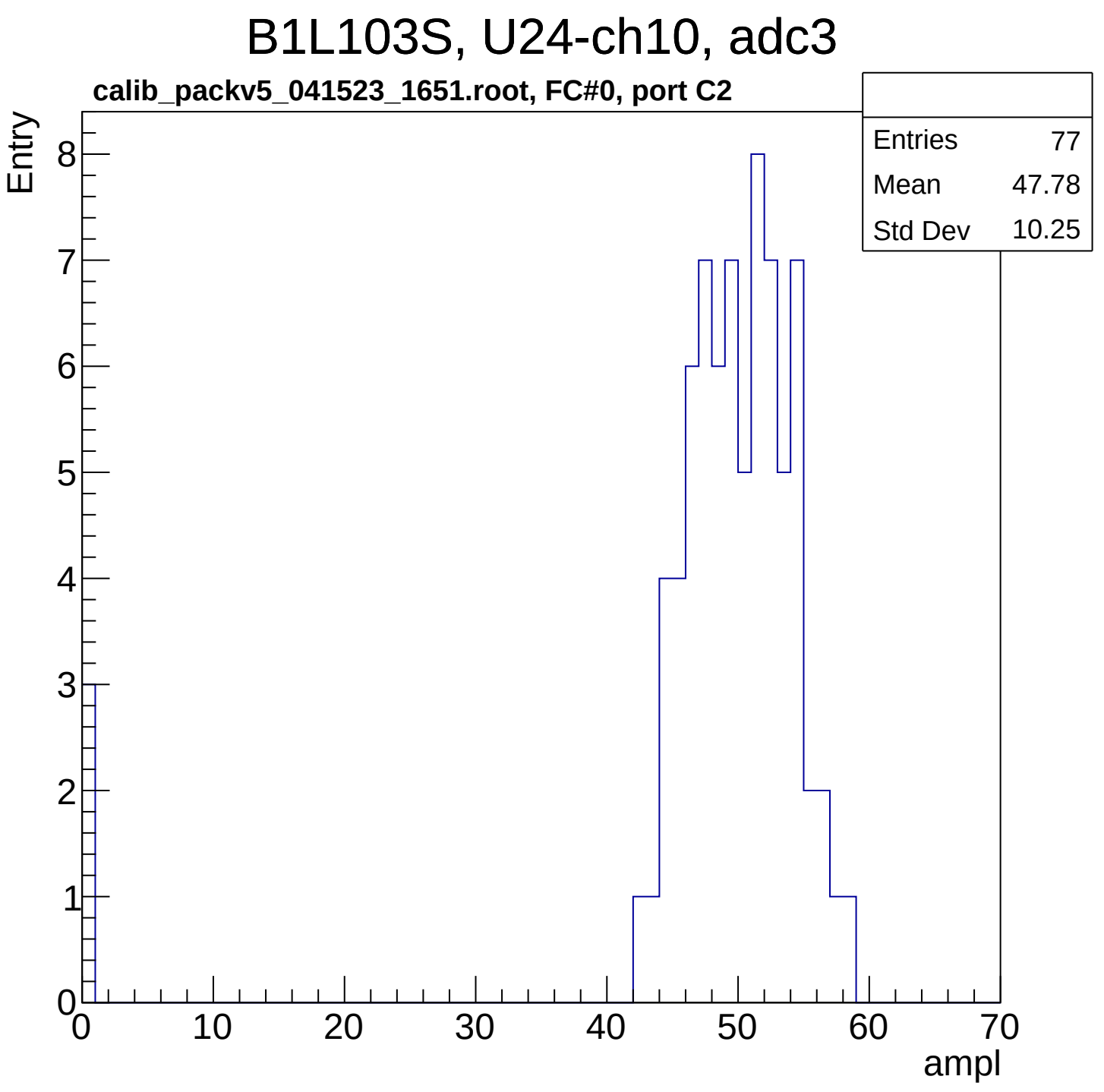
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U24-ch10, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 36.59
Std Dev 15.88
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch10, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 47.78
Std Dev 10.25
Entry
ampl
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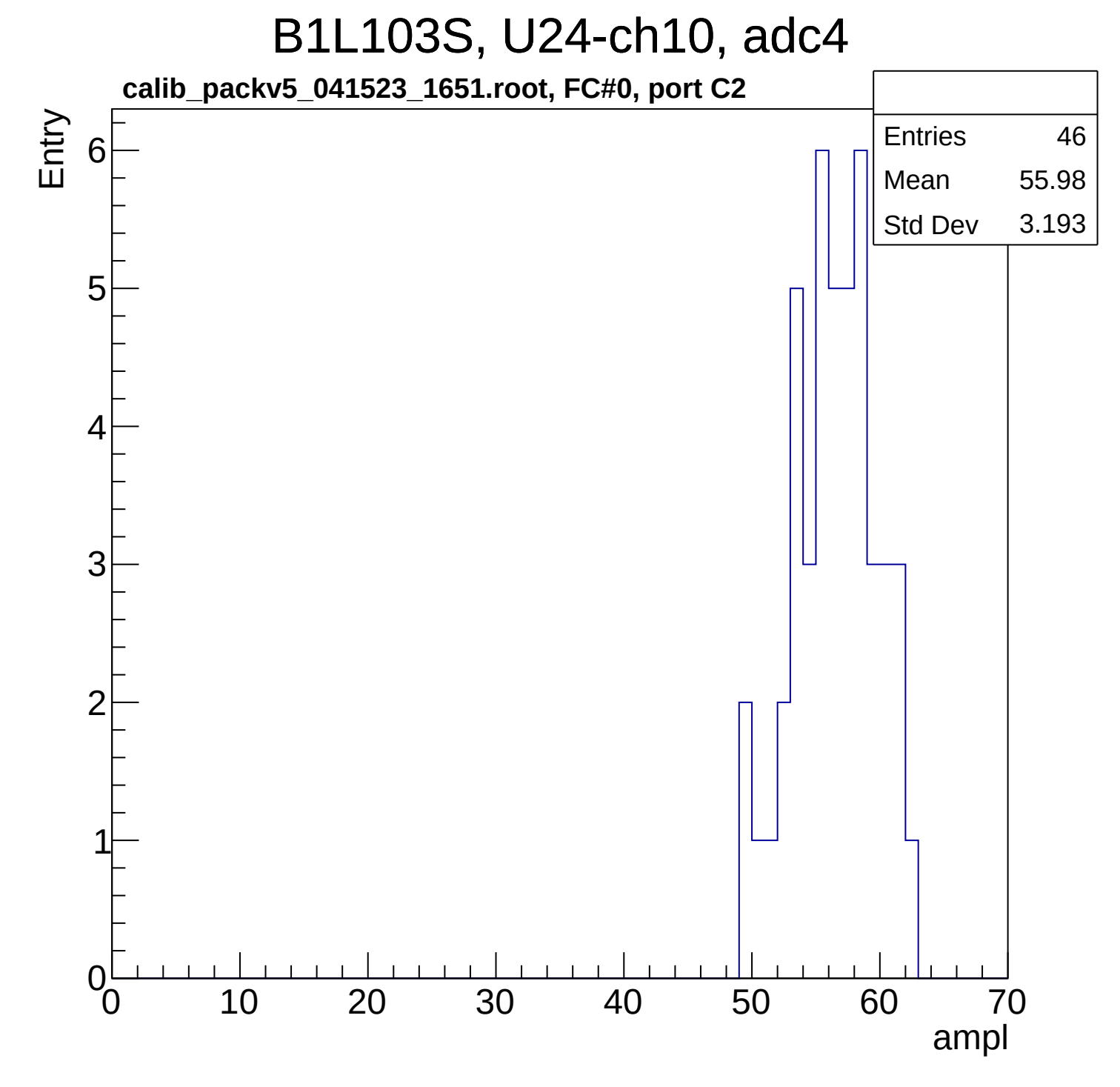
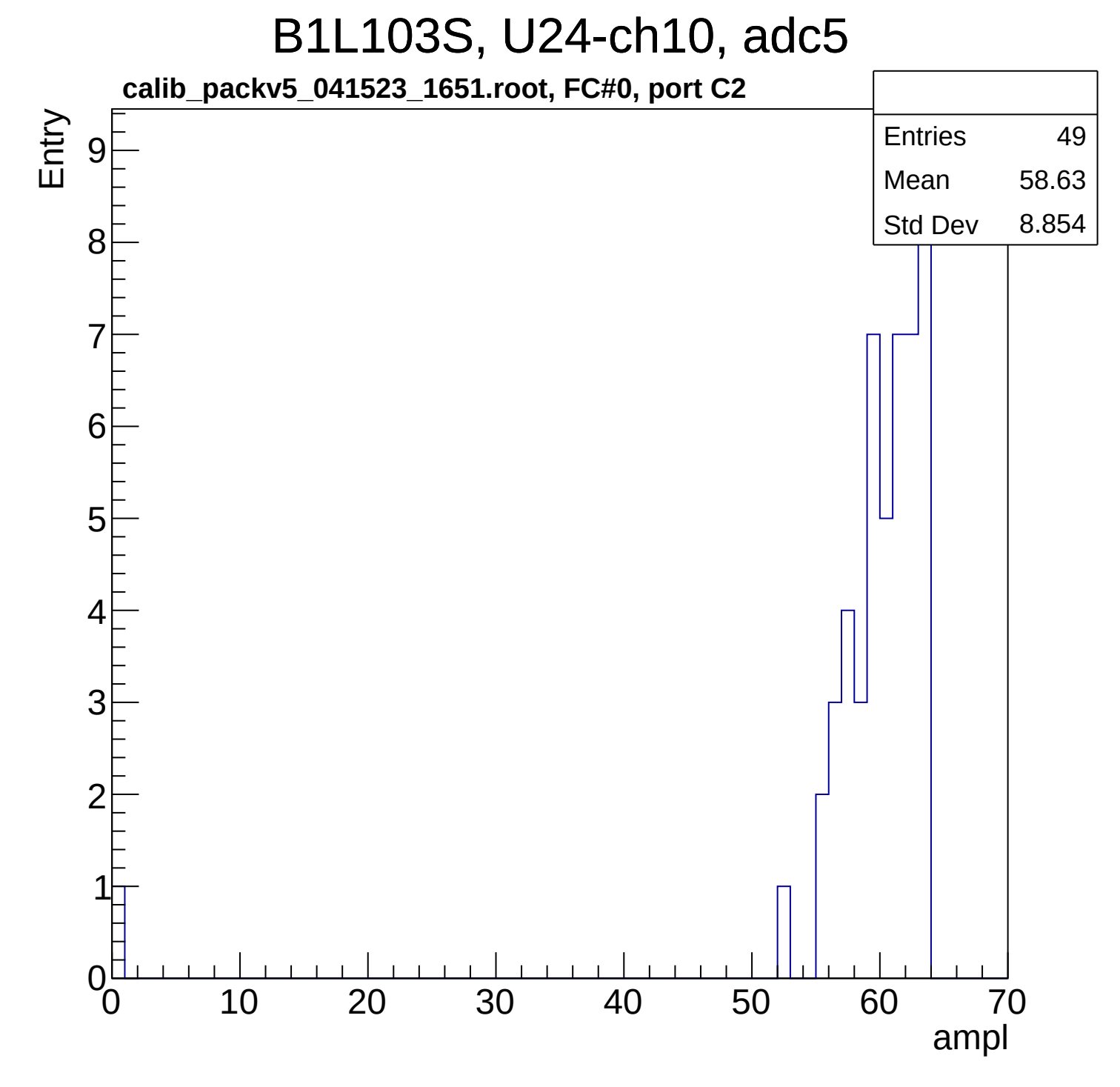
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U24-ch10, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 55.98
Std Dev 3.193
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U24-ch10, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 58.63
Std Dev 8.854
Entry
ampl
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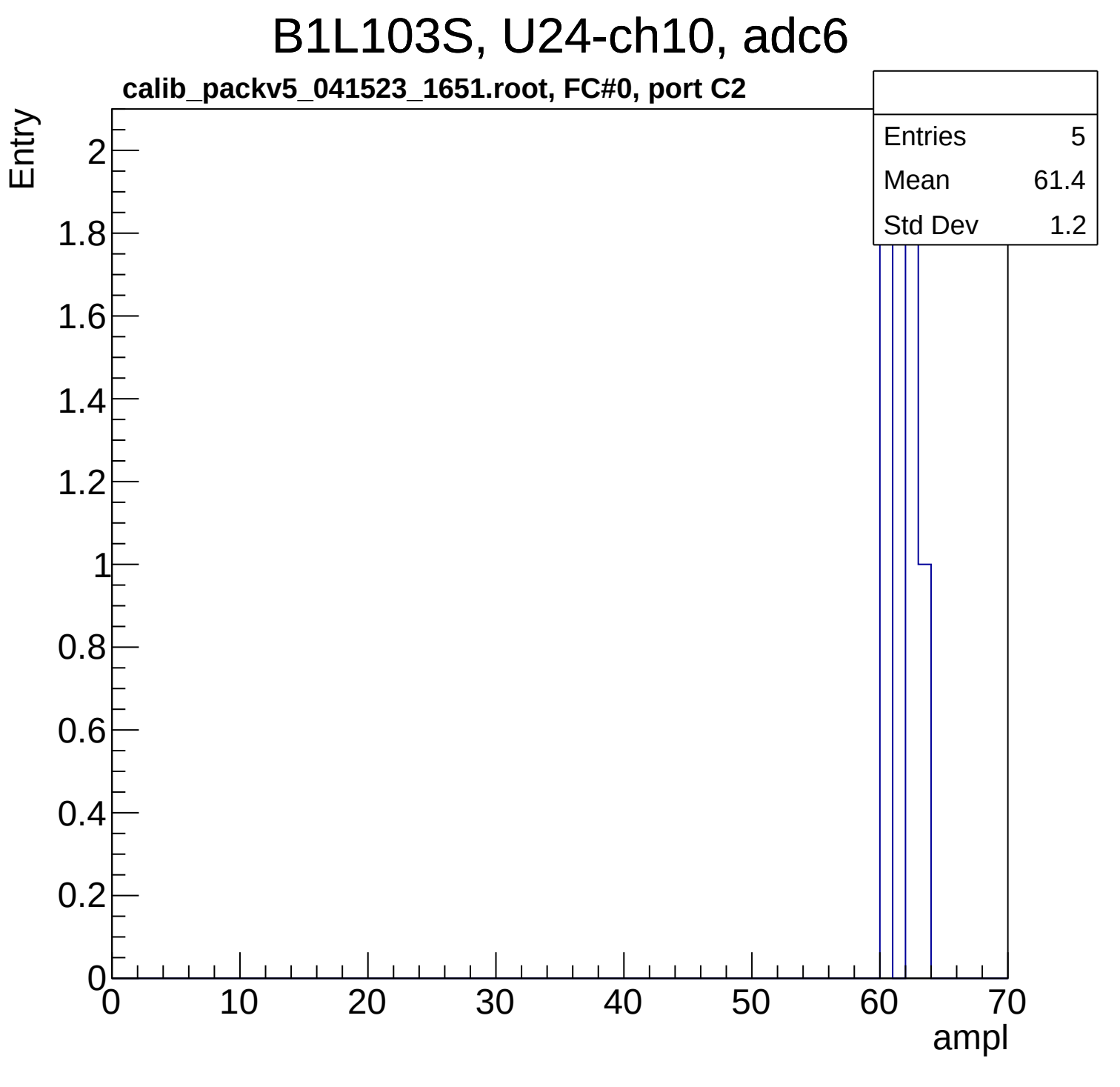
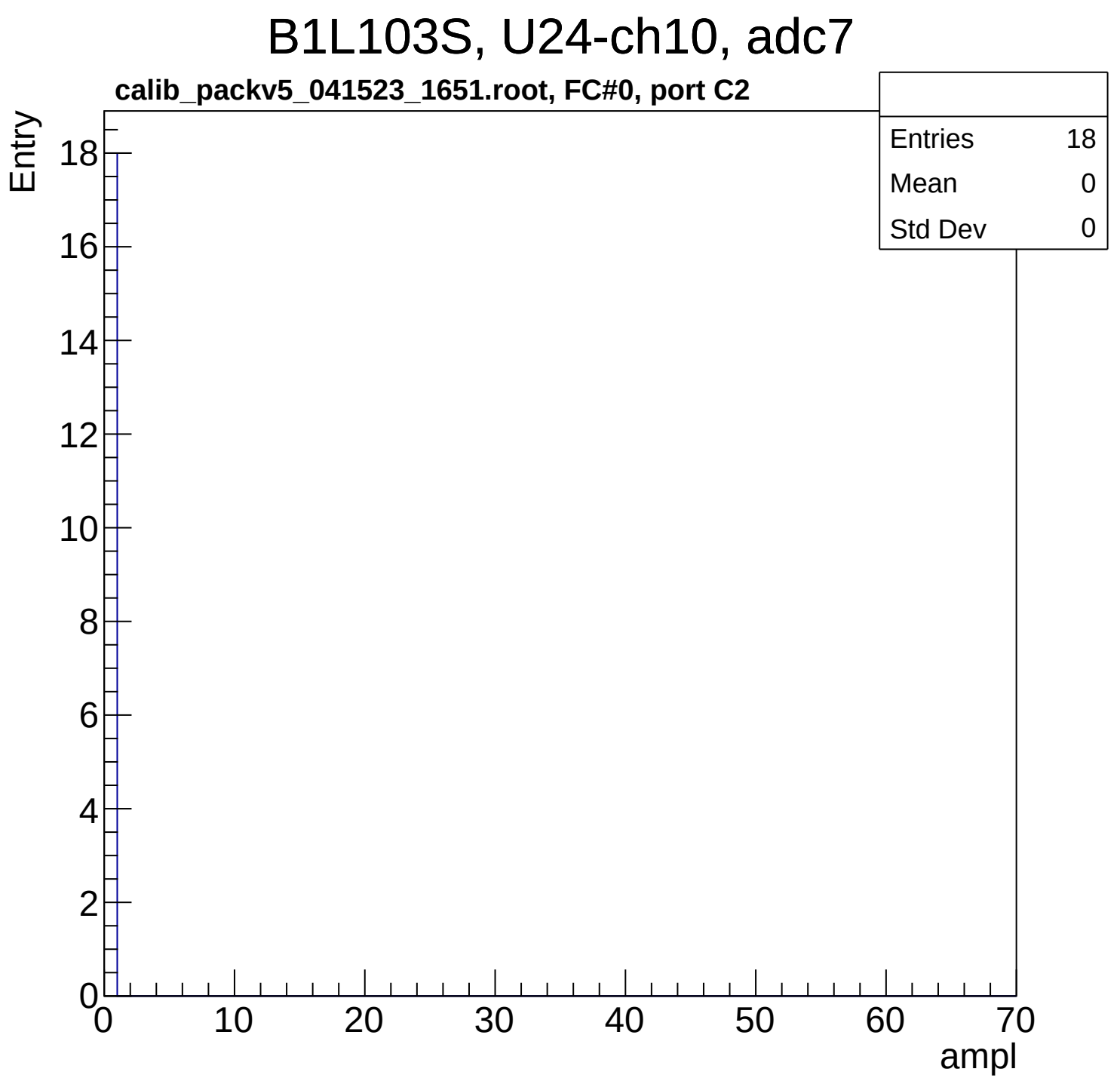
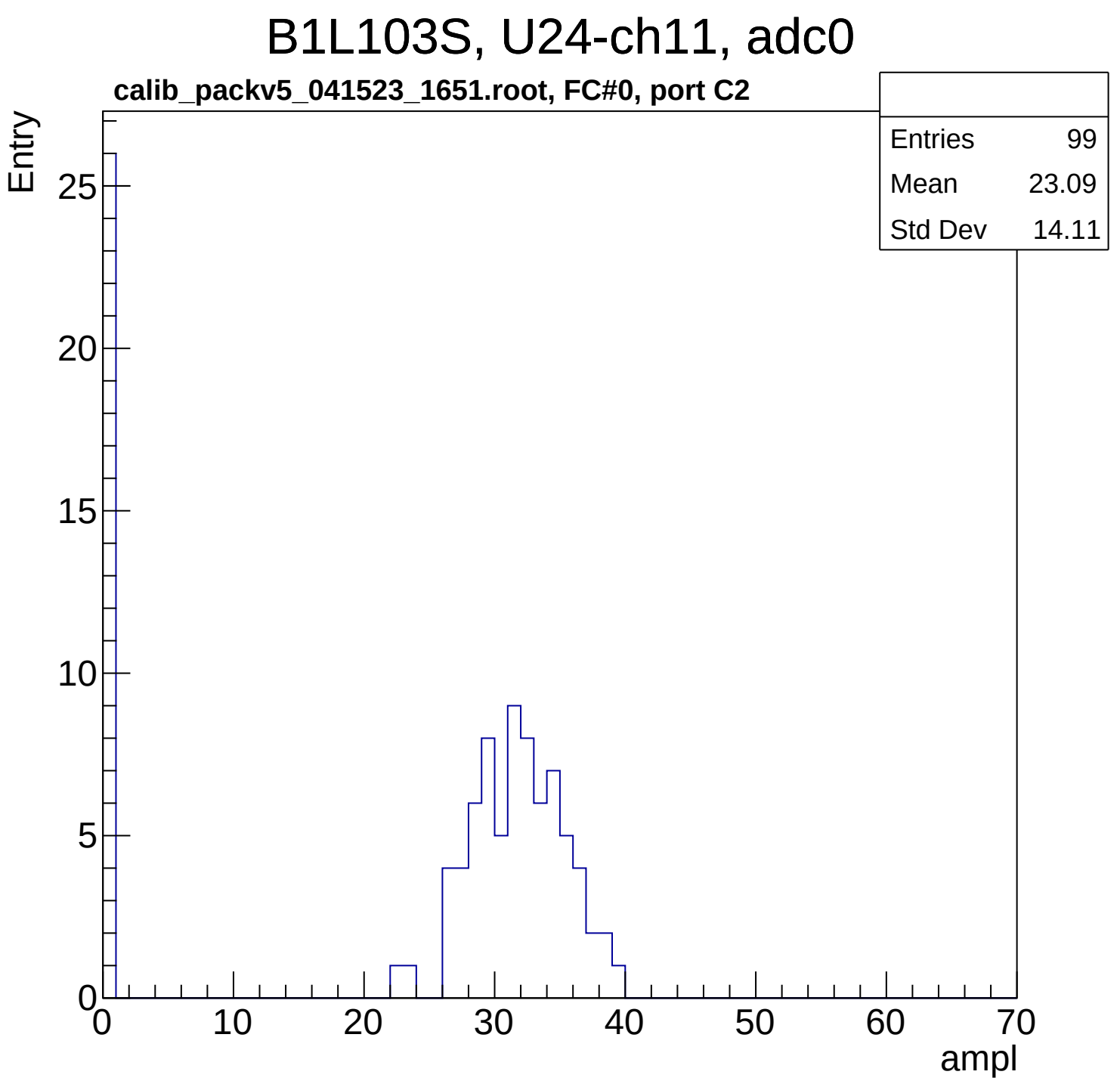
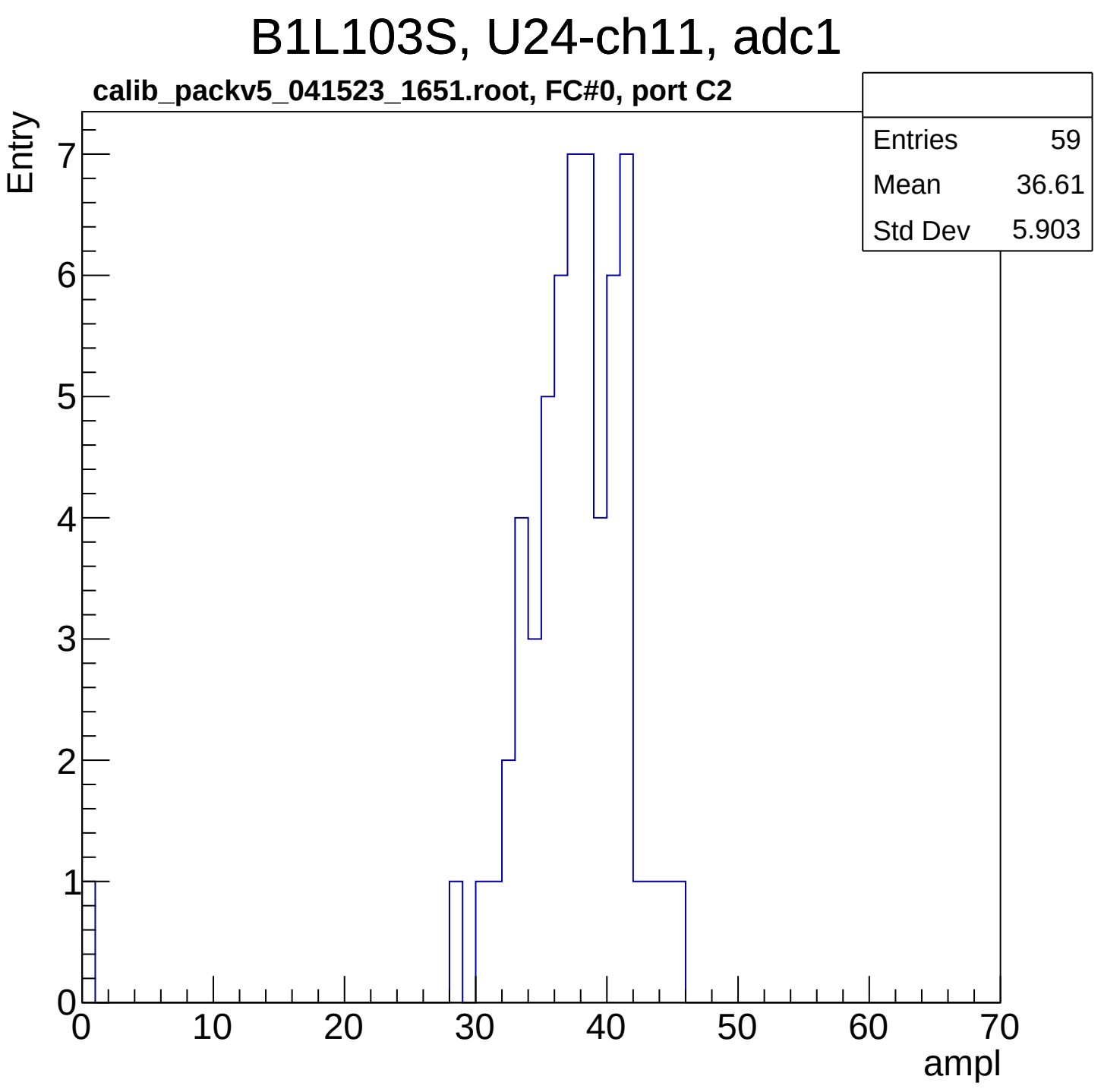
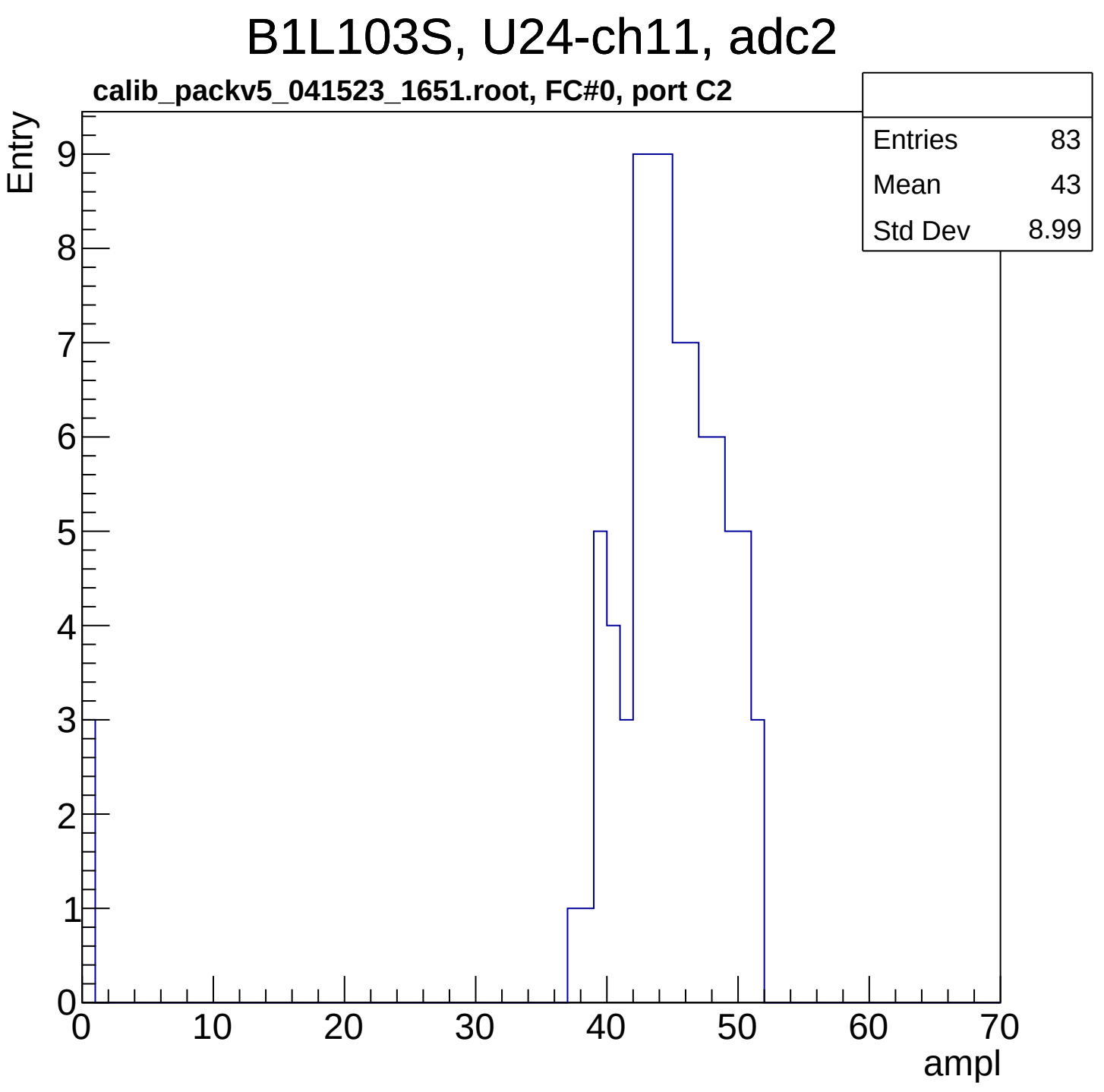
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U24-ch10, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 5
Mean 61.4
Std Dev 1.2
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U24-ch10, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch11, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 99
Mean 23.09
Std Dev 14.11
Entry
0
5
10
15
20
25
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch11, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 36.61
Std Dev 5.903
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U24-ch11, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 43
Std Dev 8.99
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
50
60
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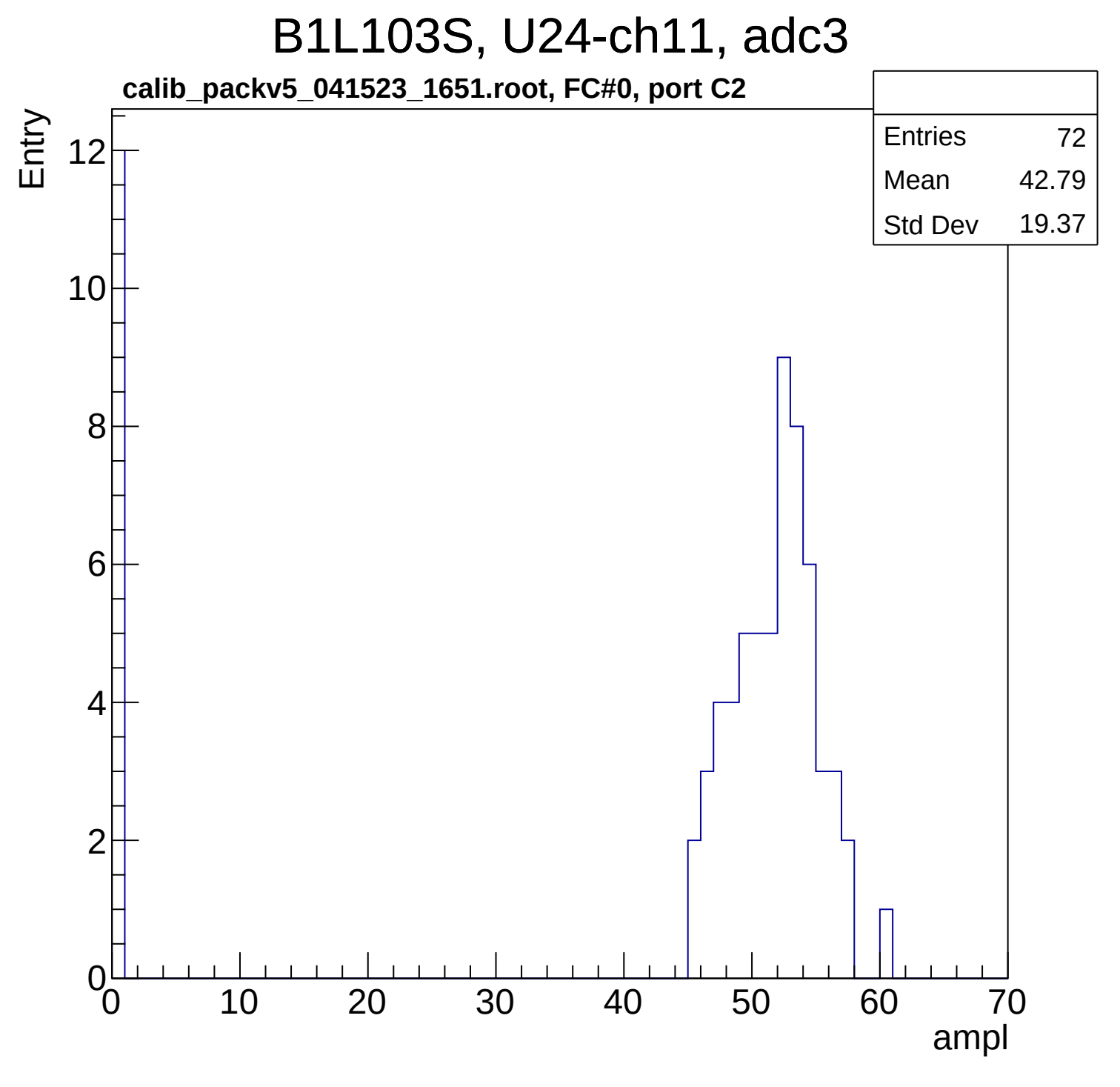
B1L103S, U24-ch11, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 42.79
Std Dev 19.37
Entry
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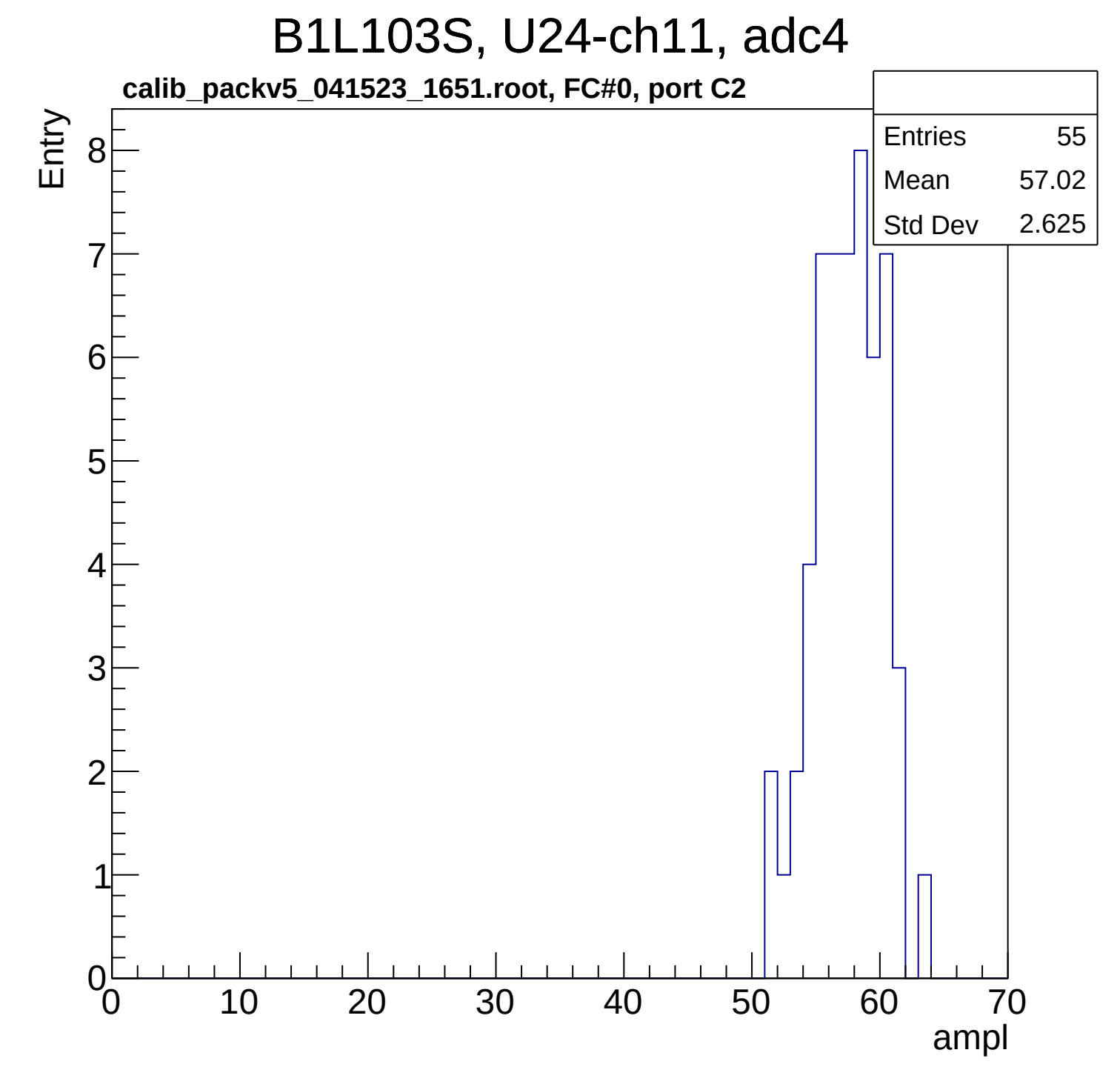
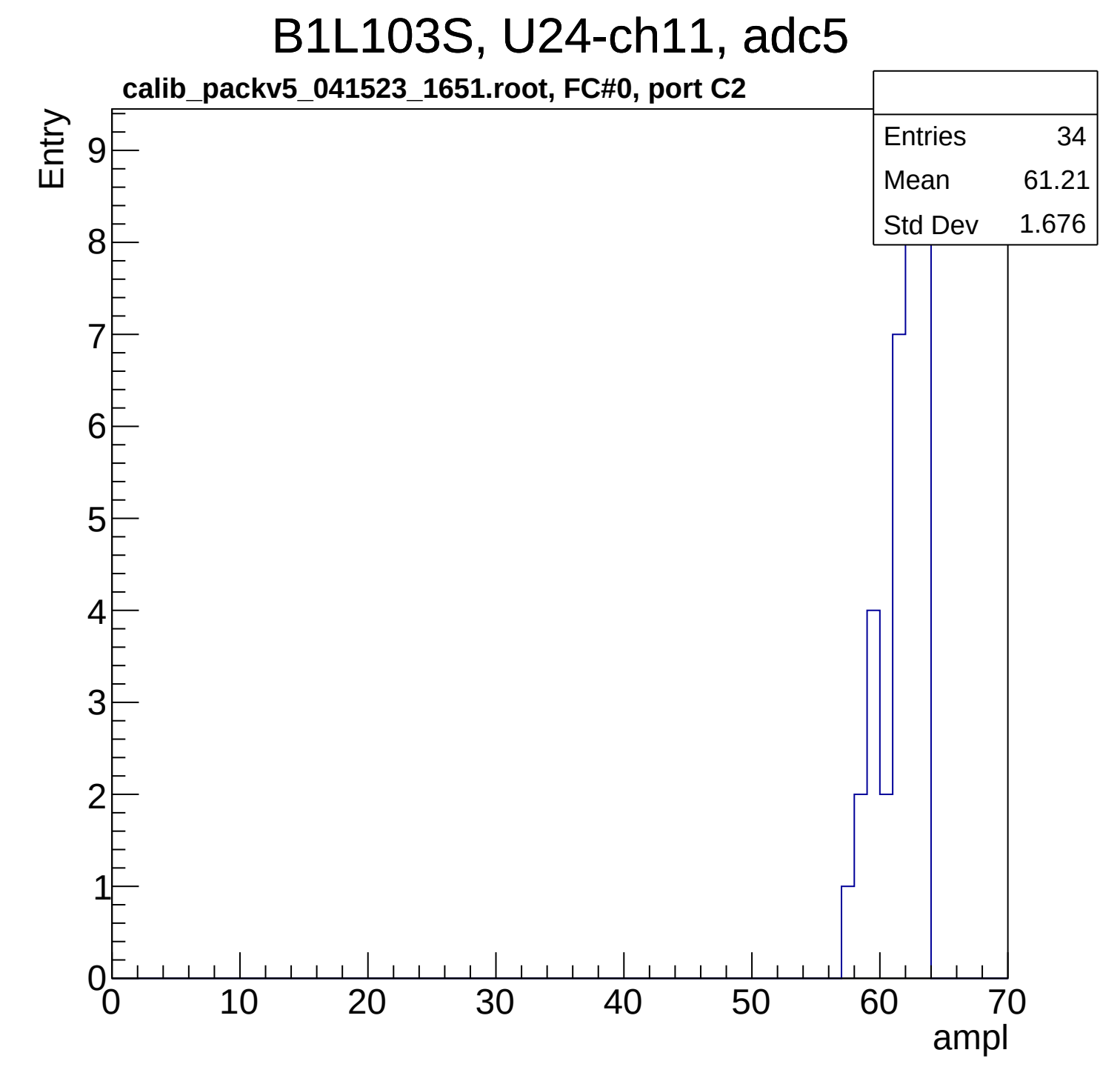
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch11, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 57.02
Std Dev 2.625
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U24-ch11, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 34
Mean 61.21
Std Dev 1.676
Entry
ampl
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2
3
4
5
6
7
8
9
0
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60
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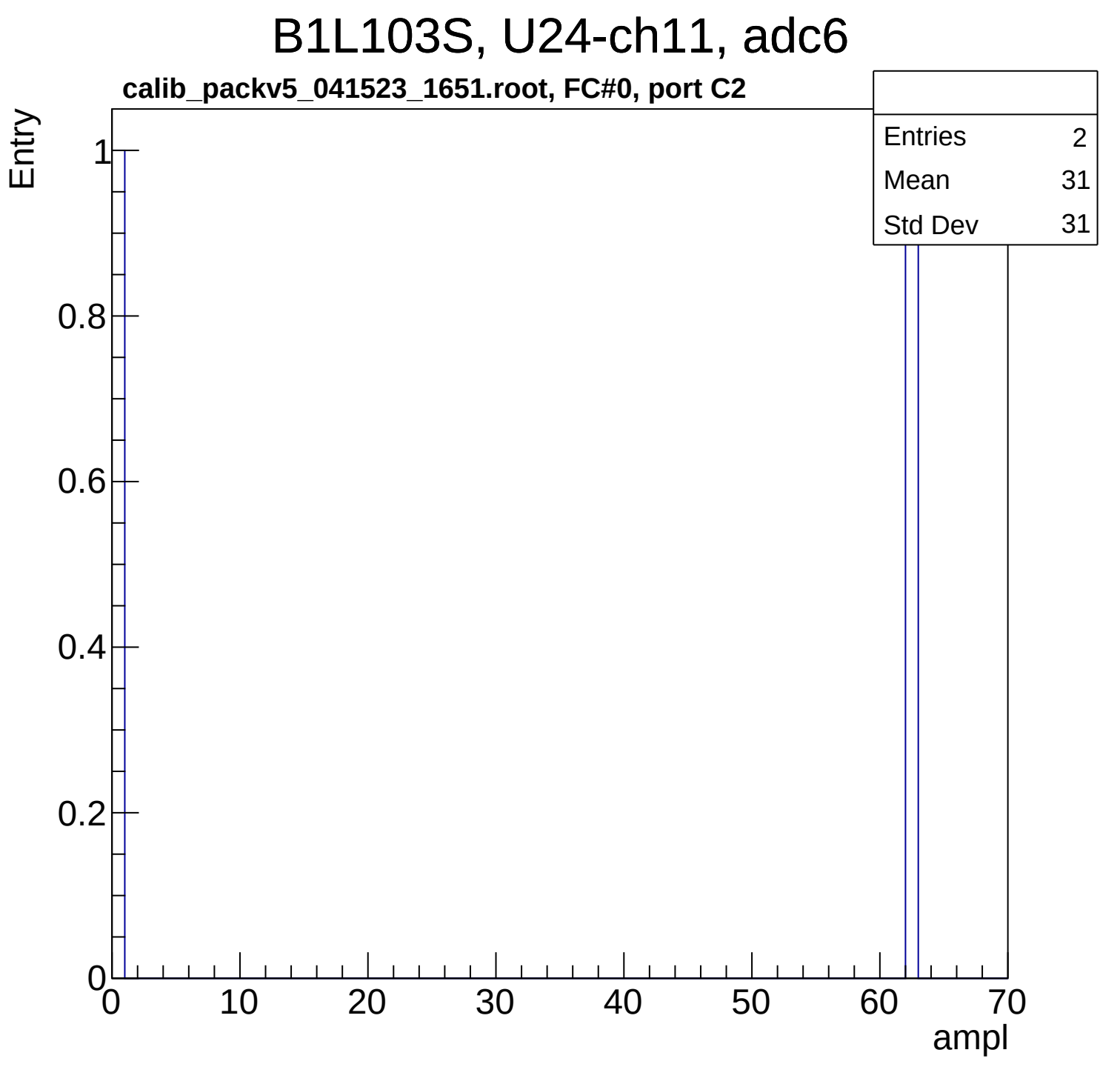
B1L103S, U24-ch11, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 2
Mean 31
Std Dev 31
Entry
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0.8
0.6
0.4
0.2
0
0
10
20
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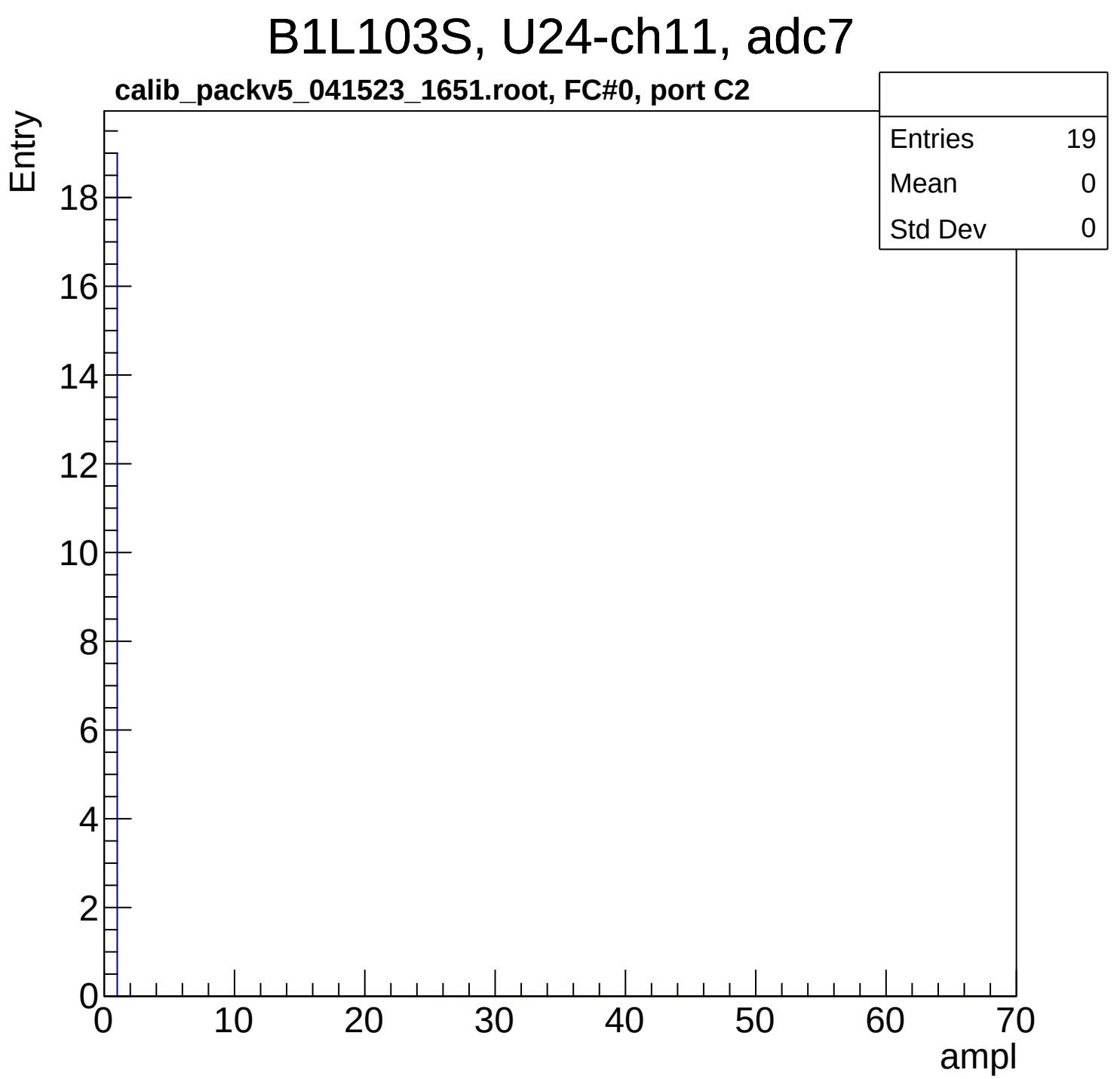
40
50
60
70
ampl


B1L103S, U24-ch11, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
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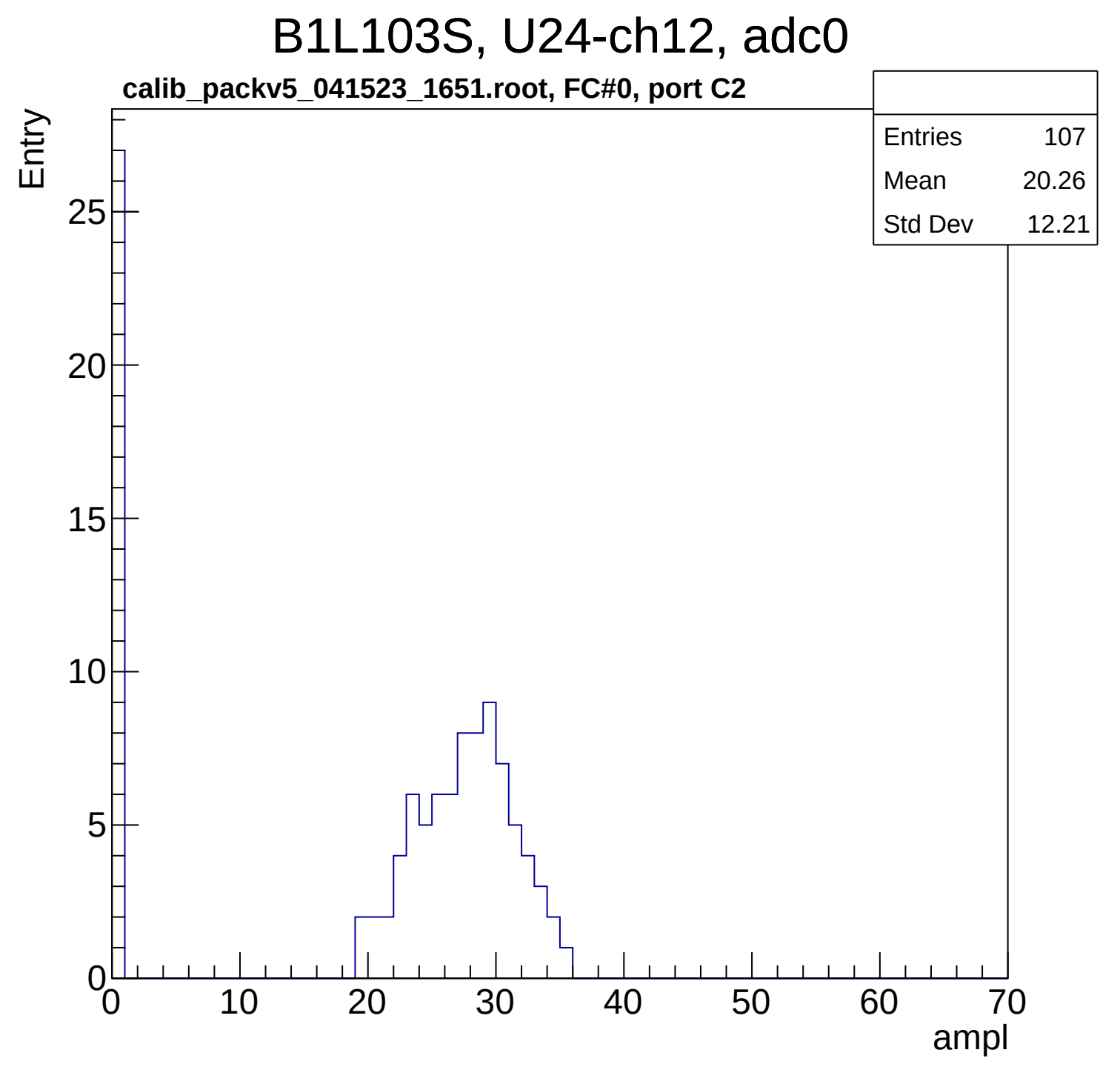
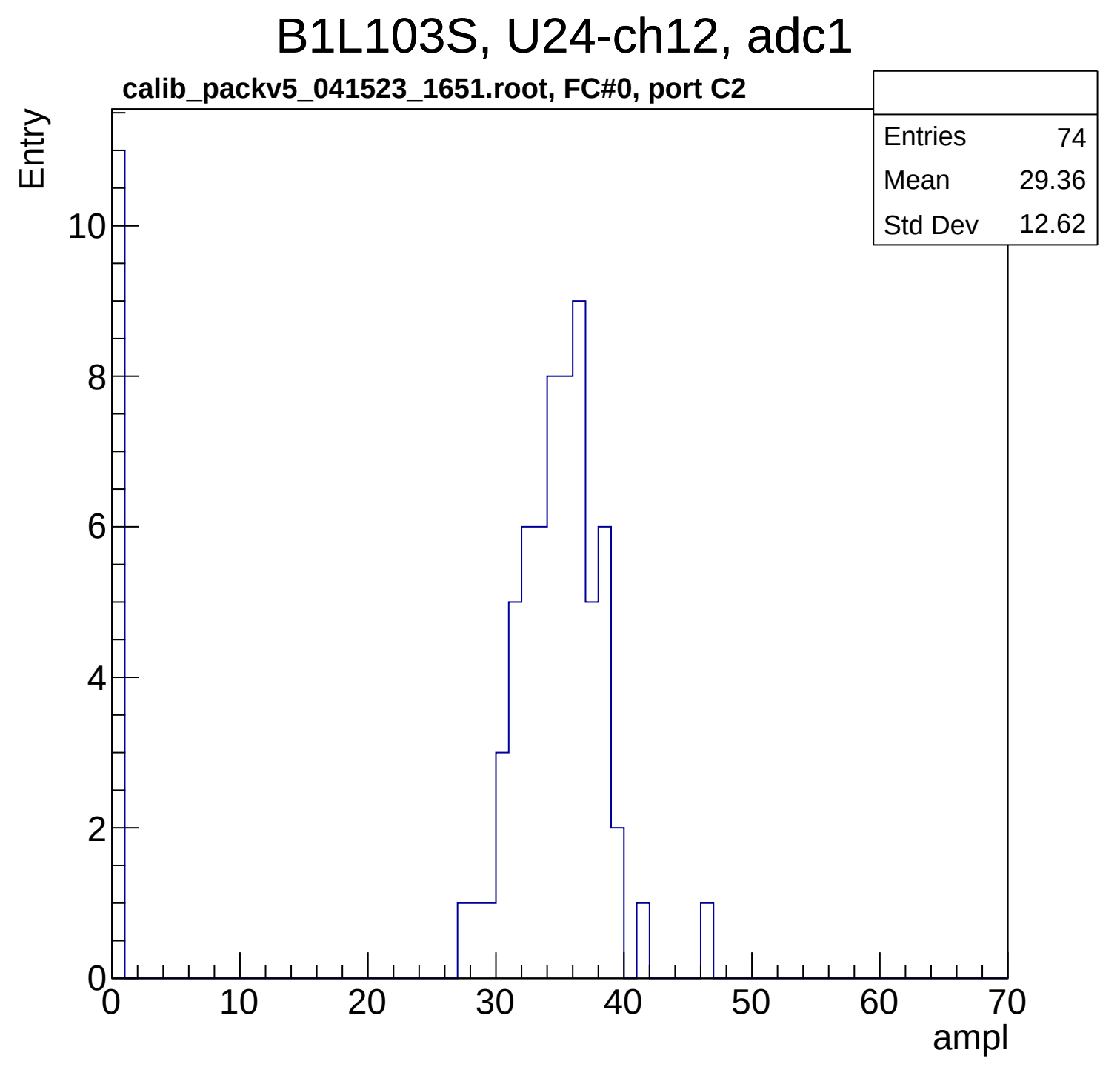
50
60
70
ampl


B1L103S, U24-ch12, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 107
Mean 20.26
Std Dev 12.21
Entry
0
5
10
15
20
25
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch12, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 29.36
Std Dev 12.62
Entry
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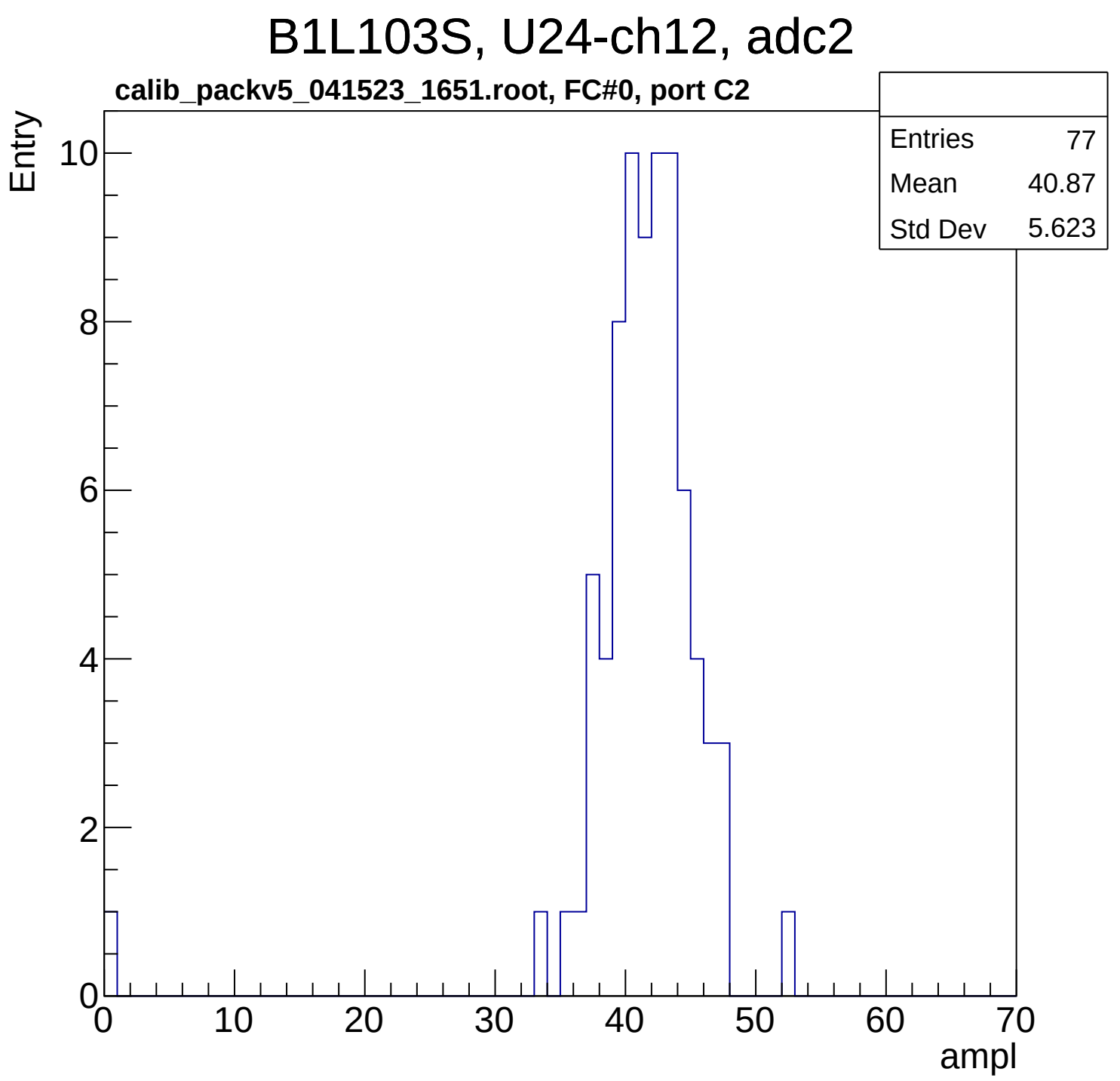
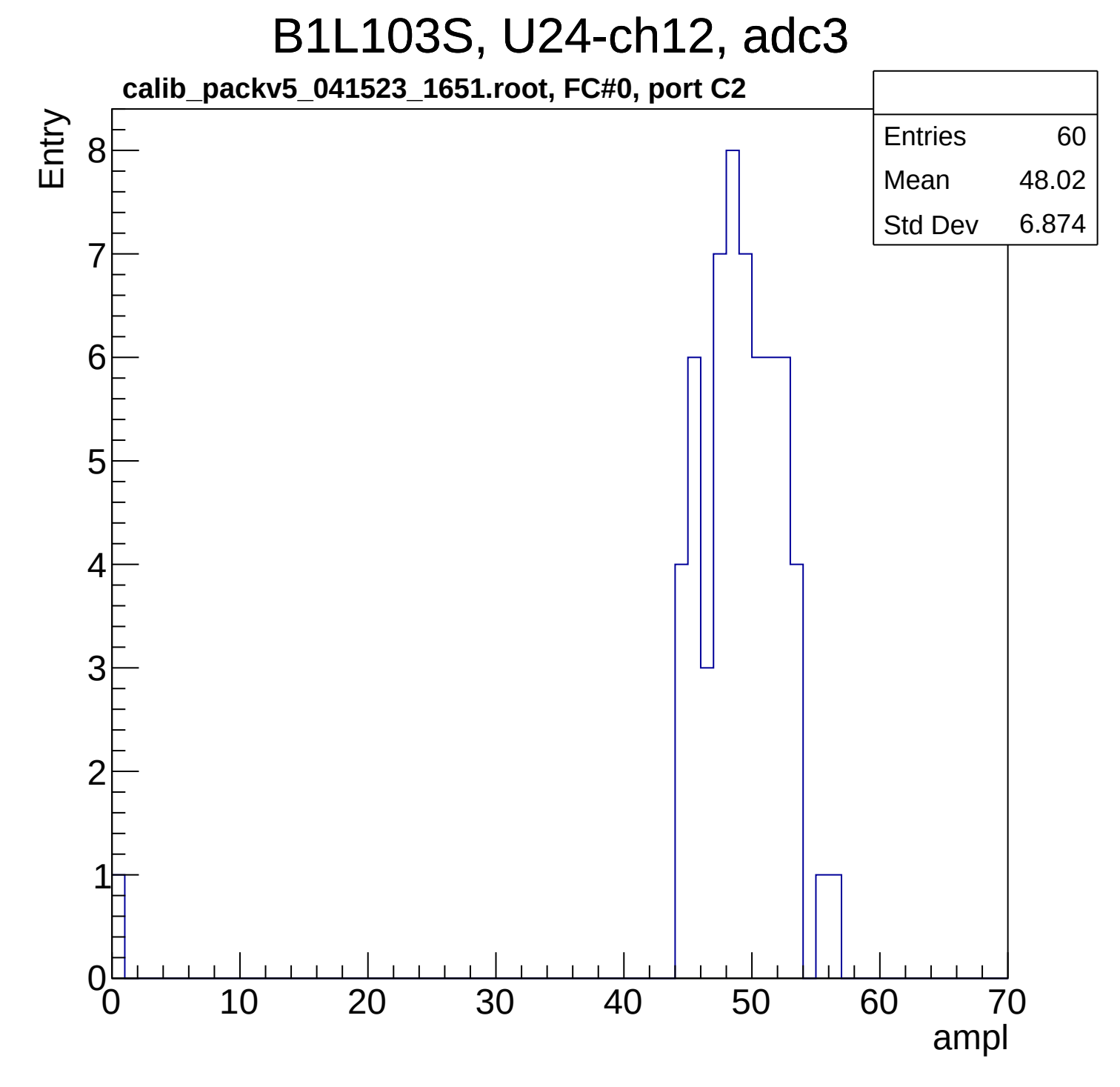
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch12, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 40.87
Std Dev 5.623
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch12, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 48.02
Std Dev 6.874
Entry
ampl
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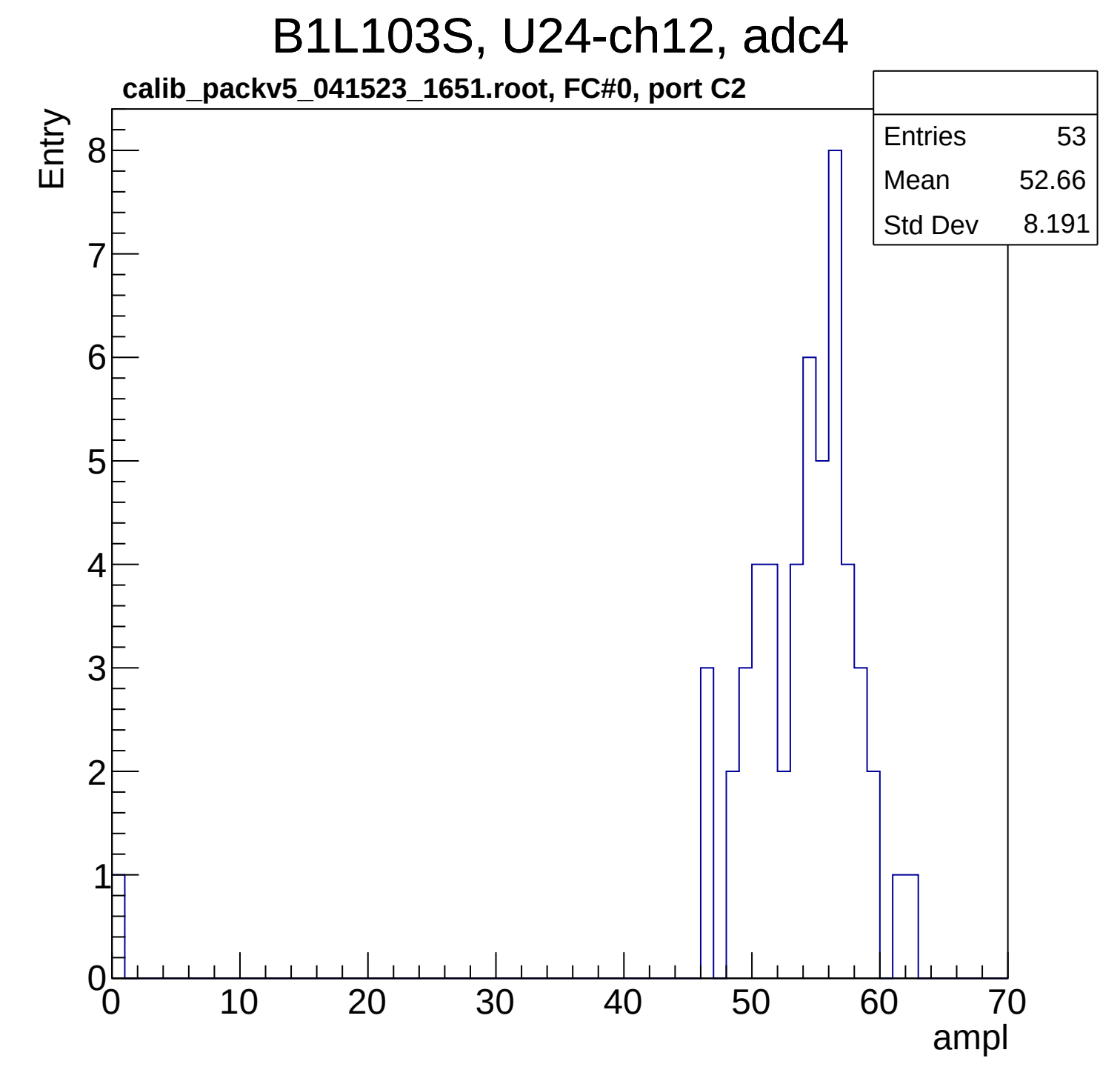
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U24-ch12, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 52.66
Std Dev 8.191
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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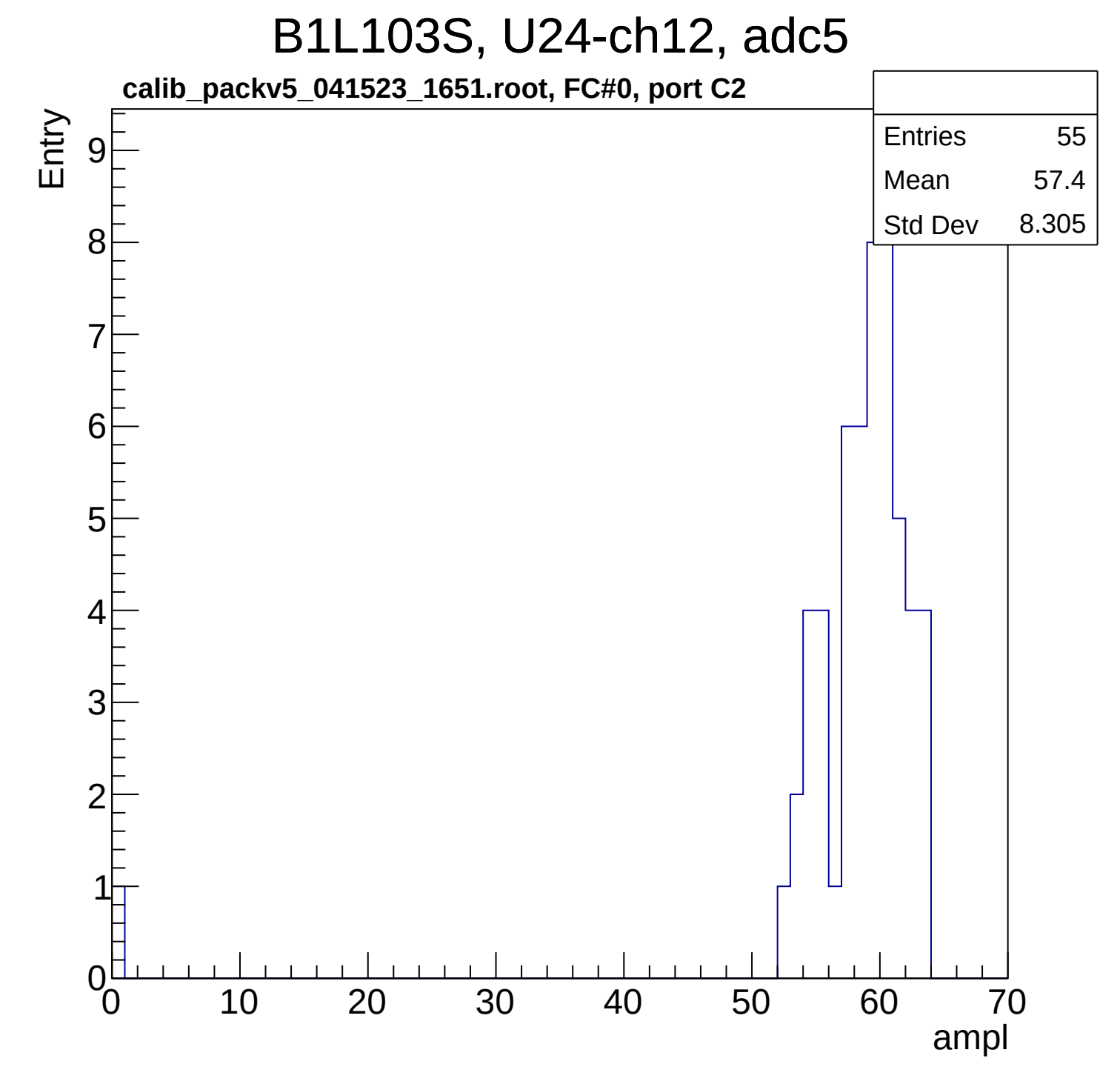
B1L103S, U24-ch12, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 57.4
Std Dev 8.305
Entry
ampl
0
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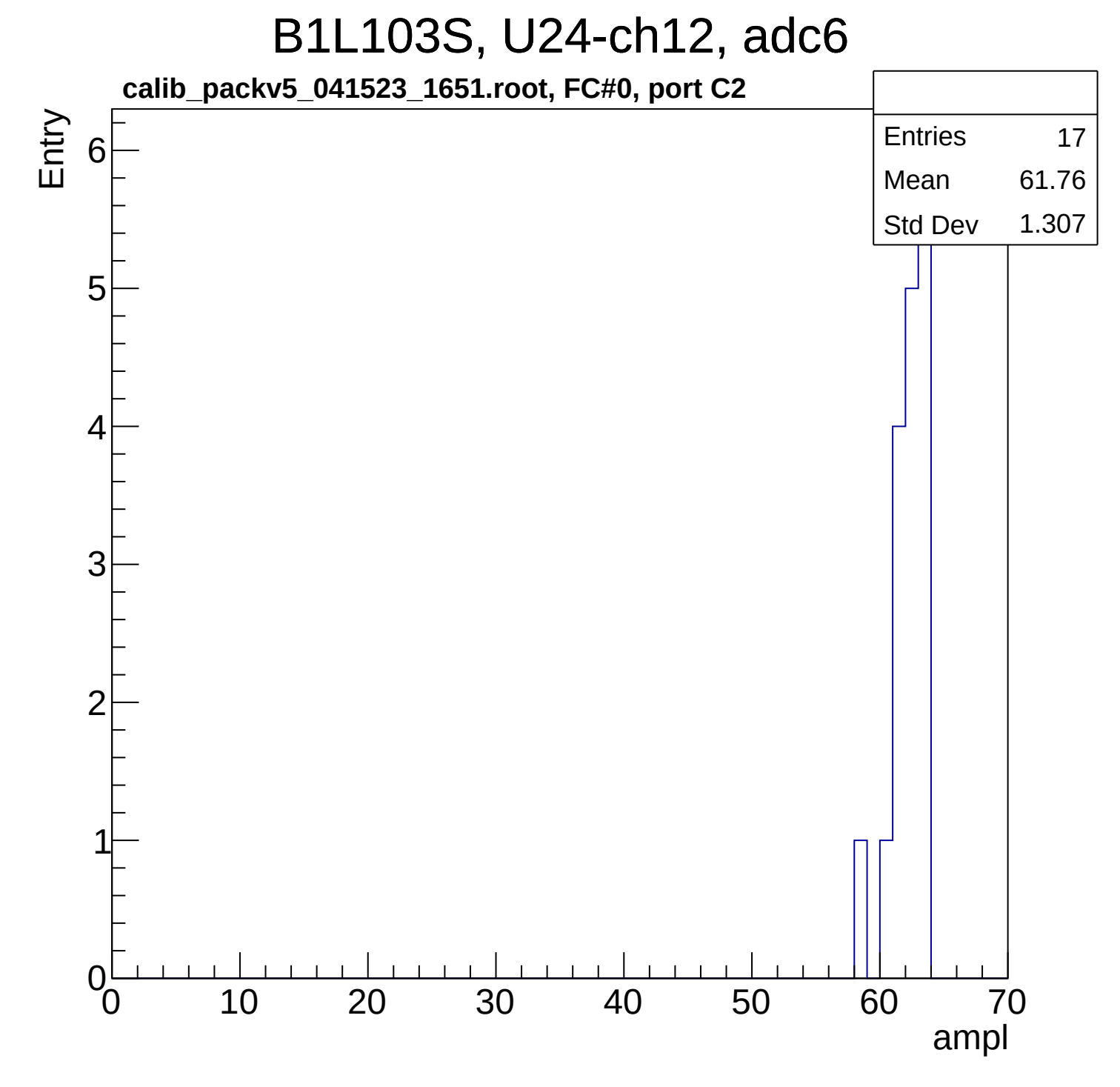
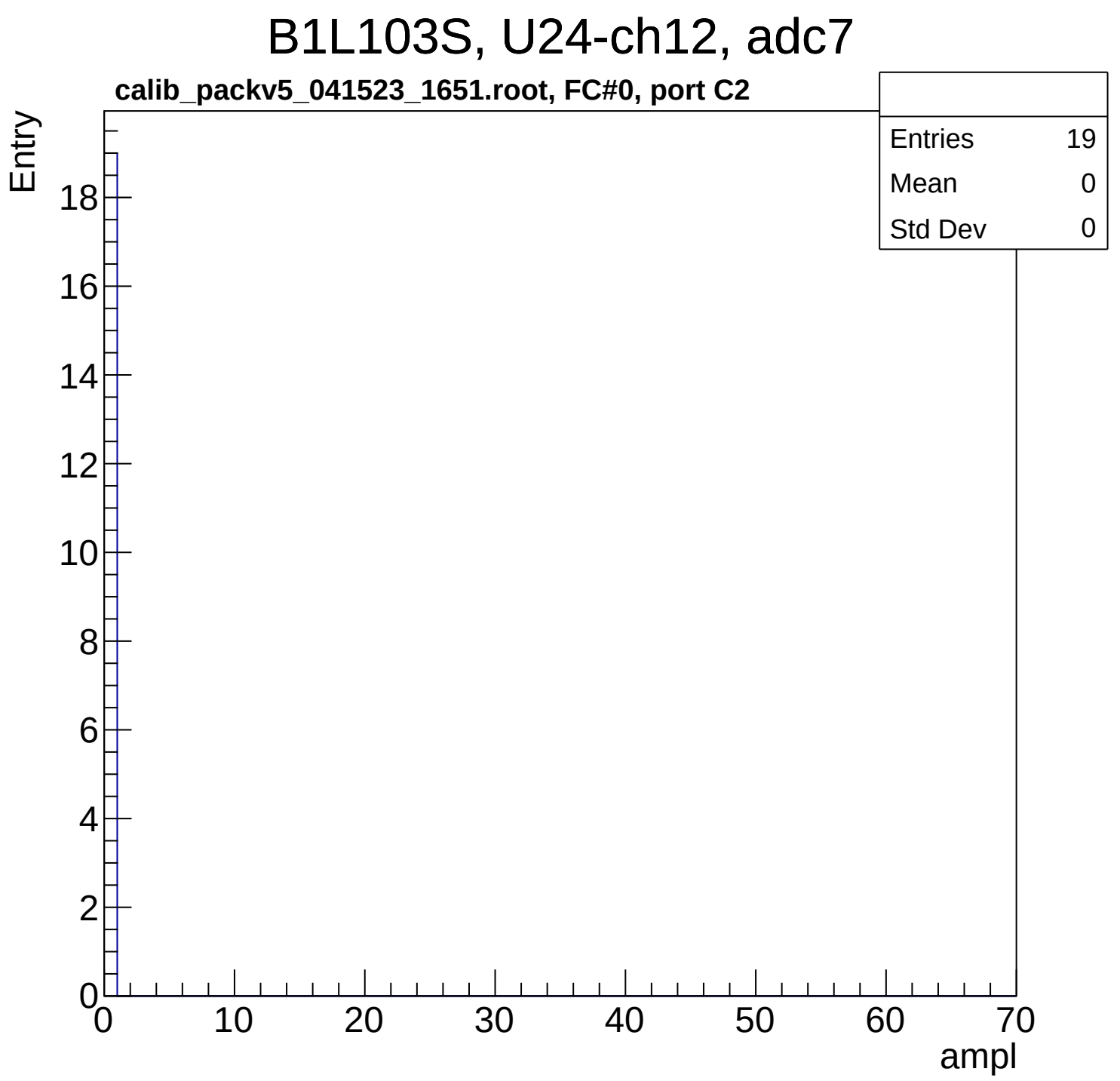
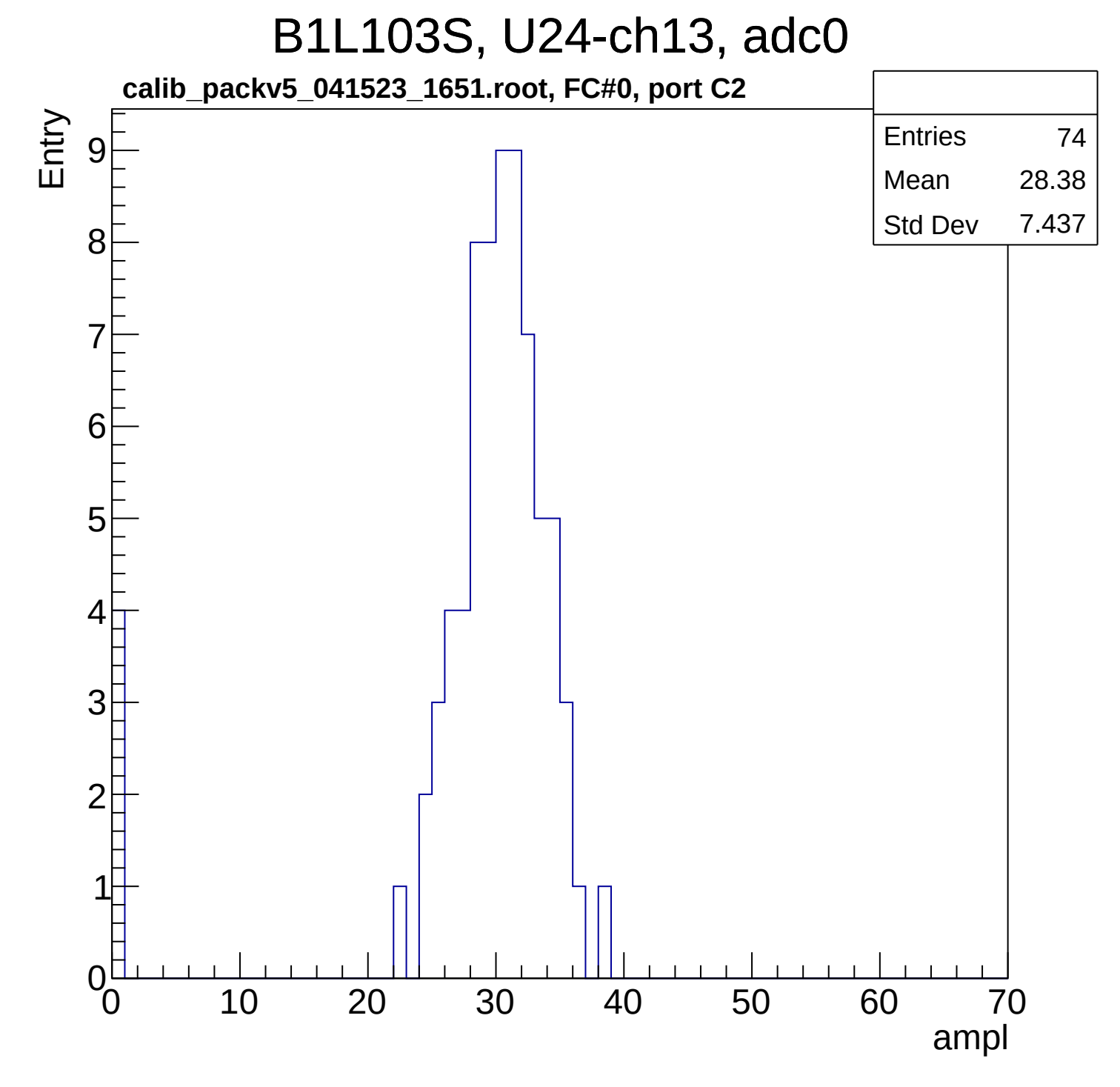
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U24-ch12, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 17
Mean 61.76
Std Dev 1.307
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U24-ch12, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch13, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 28.38
Std Dev 7.437
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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30
40
50
60
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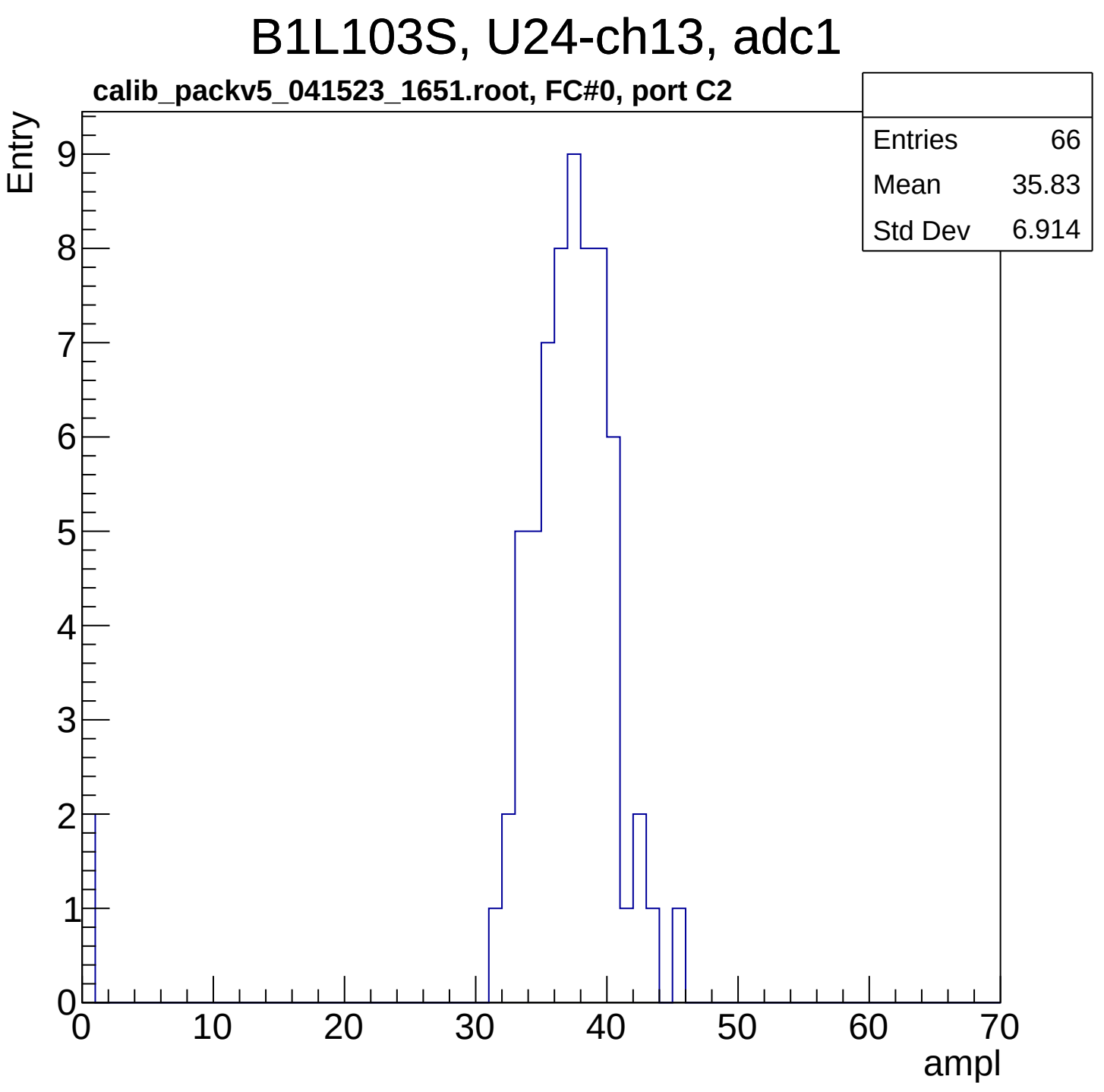
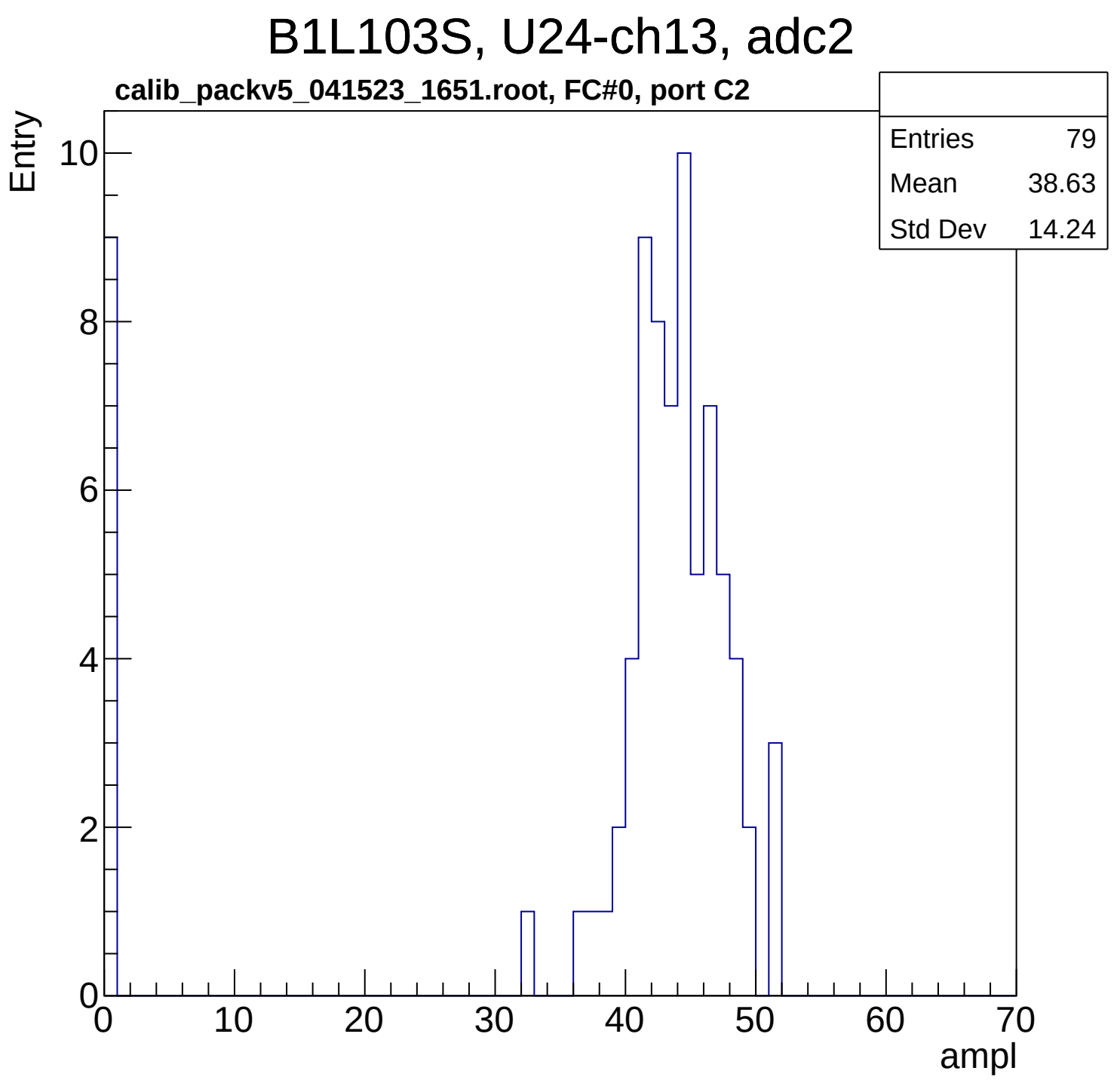
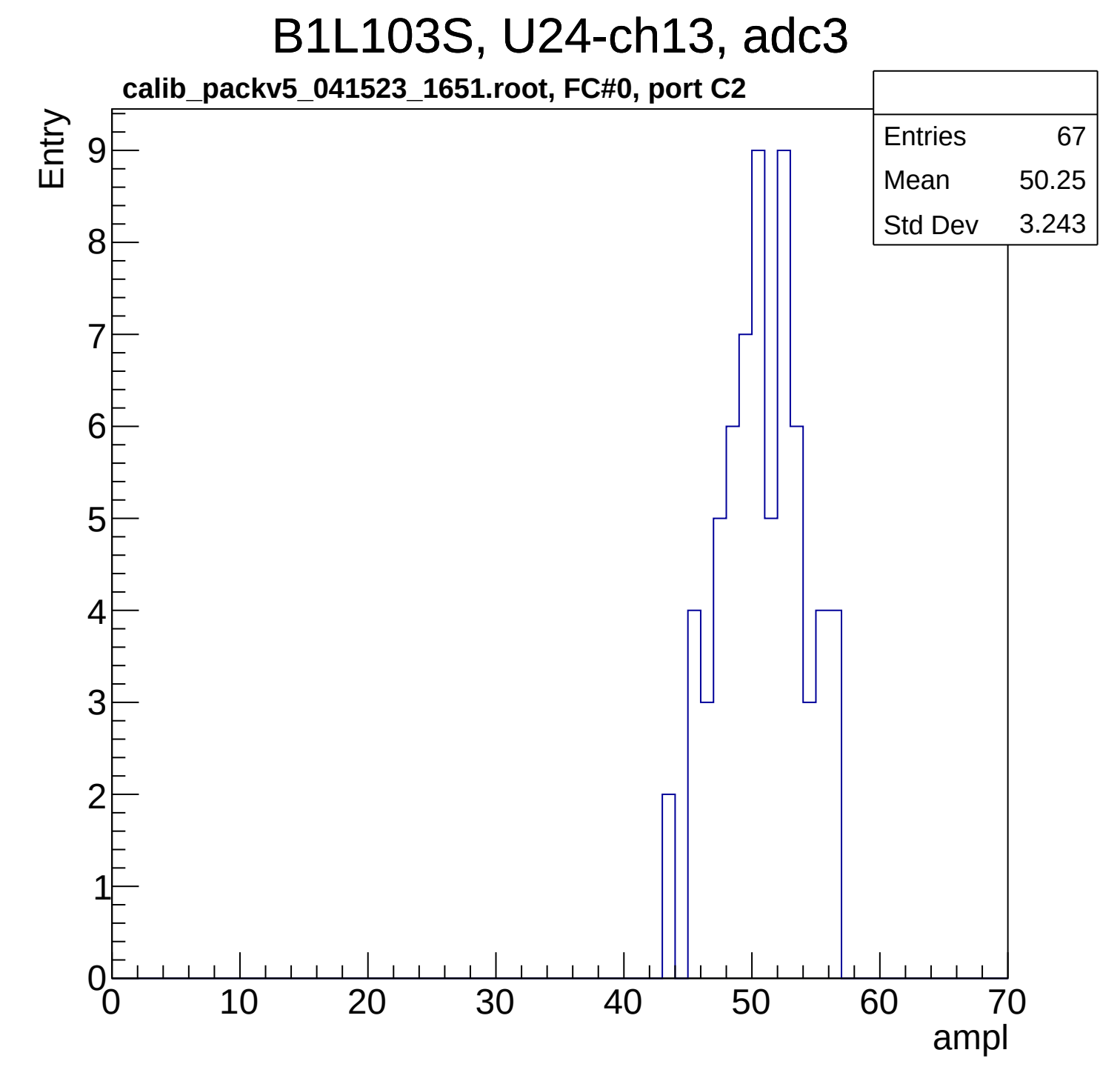

B1L103S, U24-ch13, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 35.83
Std Dev 6.914
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U24-ch13, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 38.63
Std Dev 14.24
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U24-ch13, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 50.25
Std Dev 3.243
Entry
ampl
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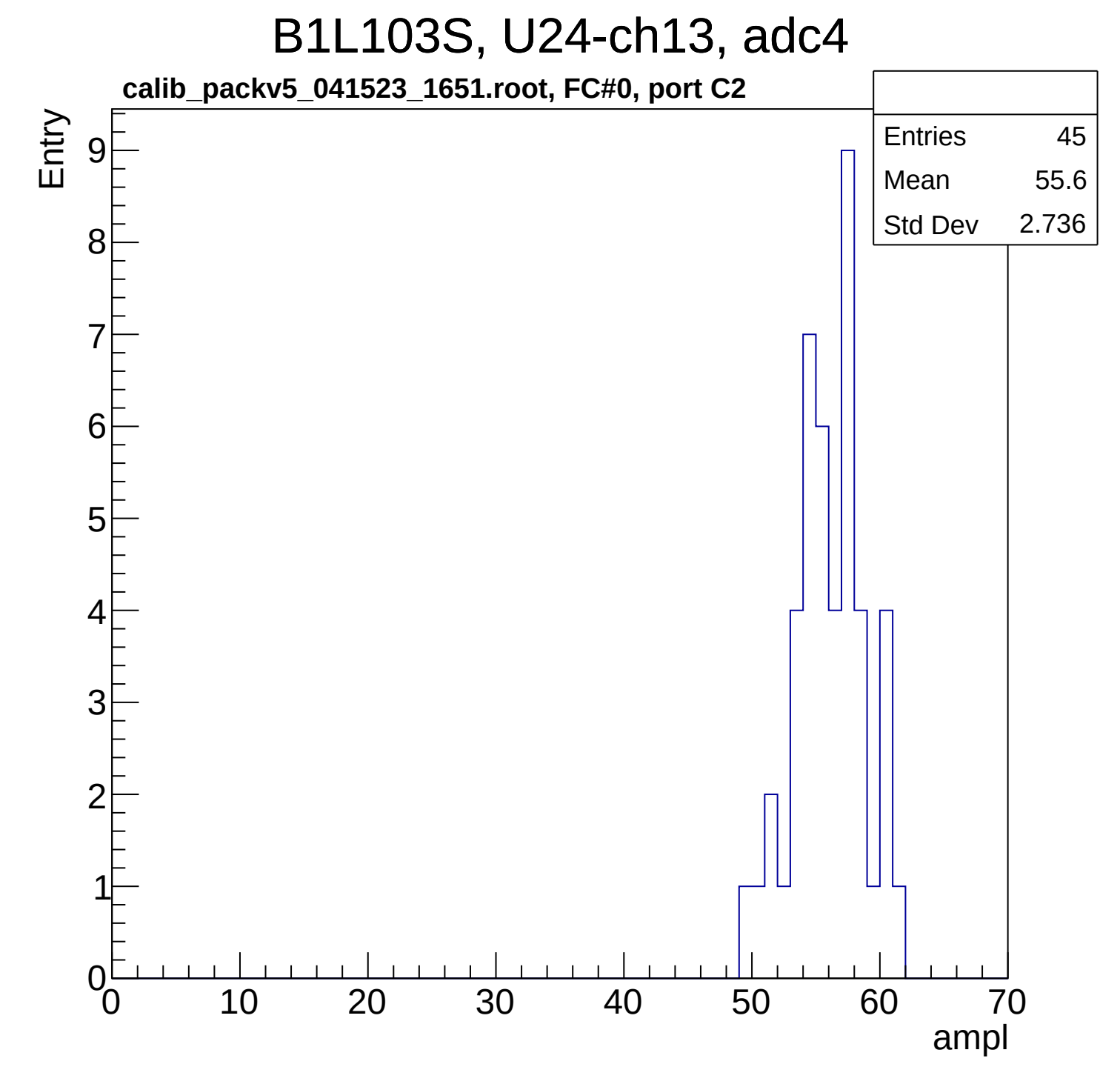
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U24-ch13, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 55.6
Std Dev 2.736
Entry
ampl
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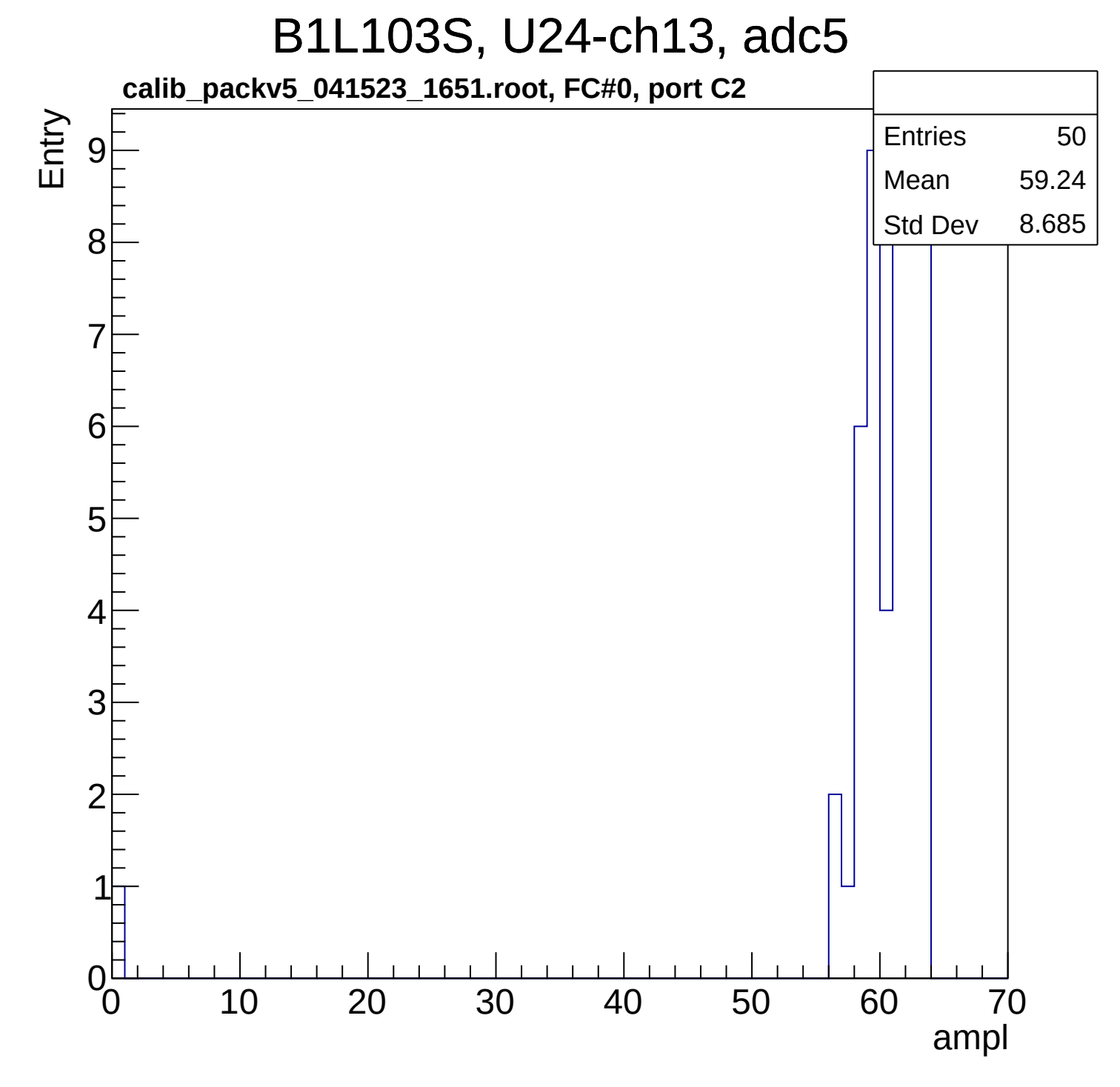
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U24-ch13, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 59.24
Std Dev 8.685
Entry
ampl
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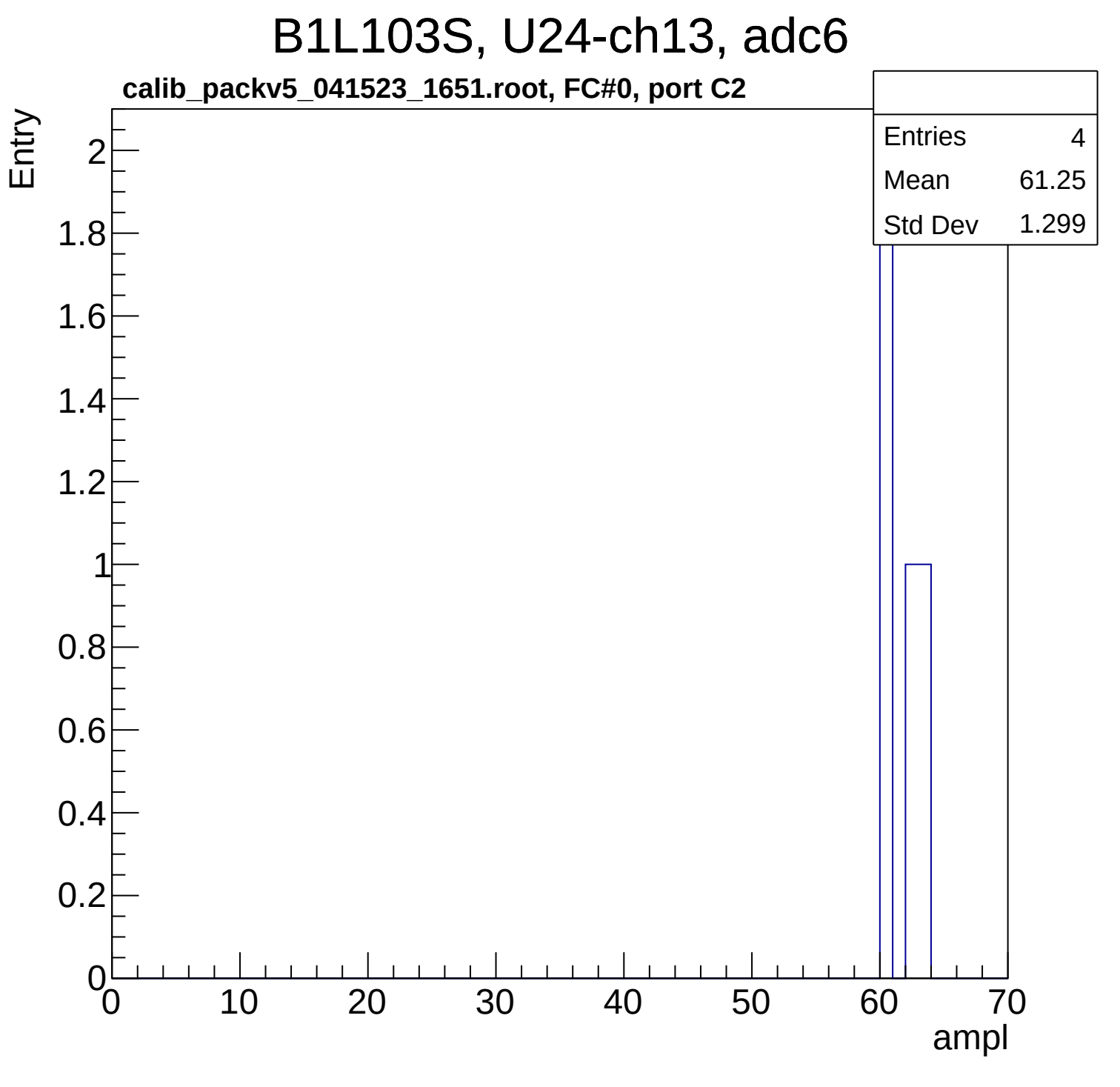
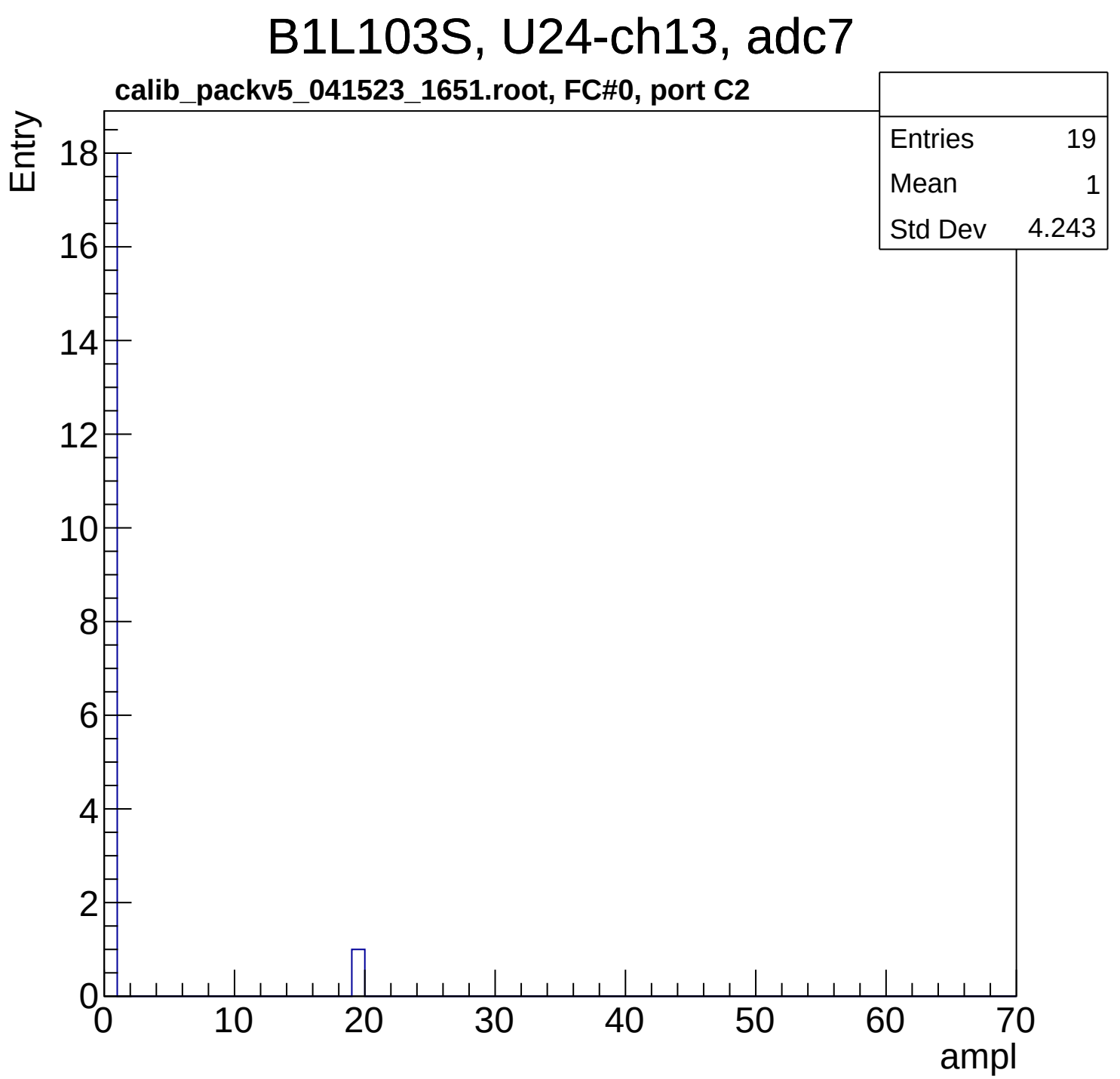
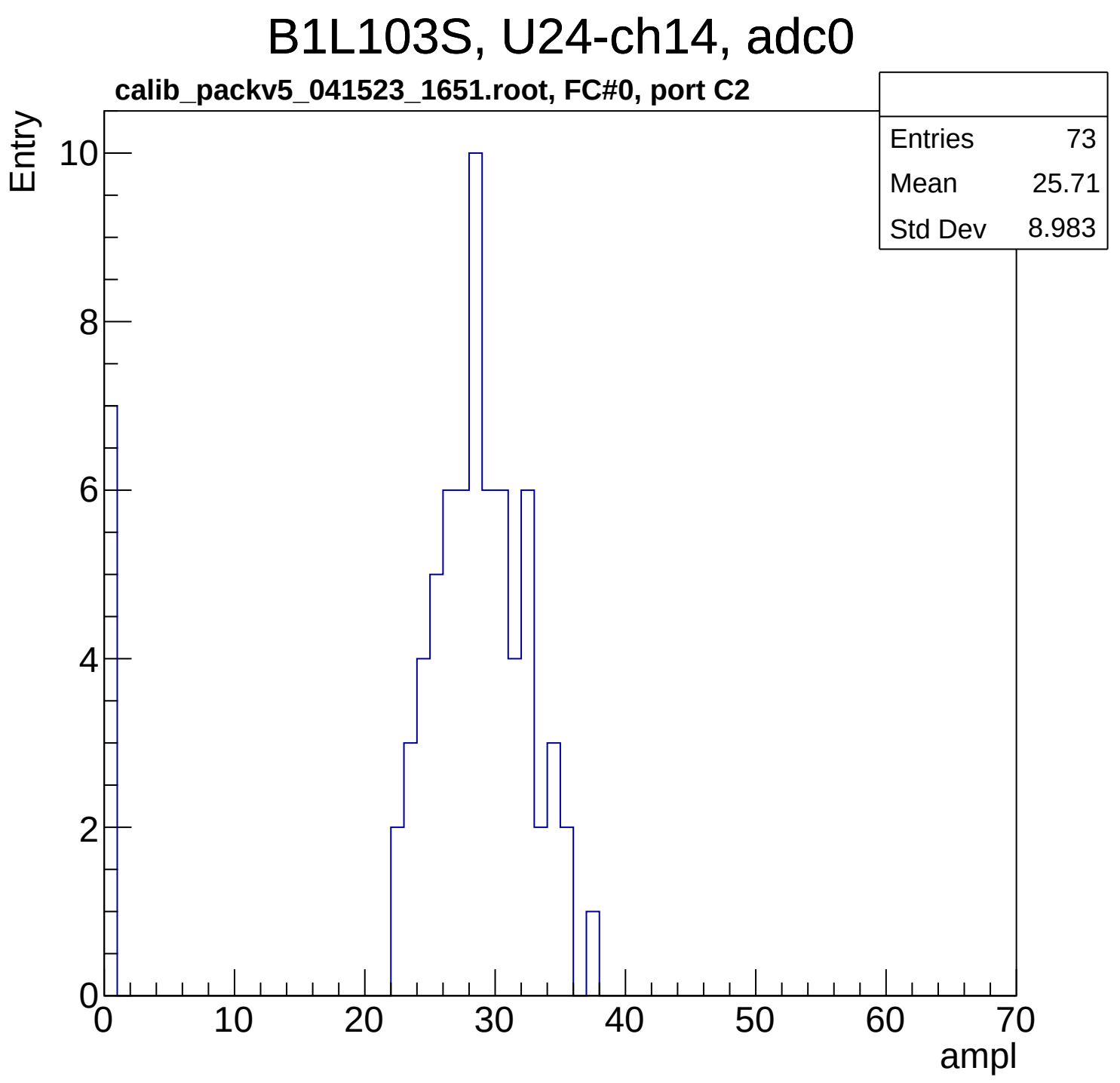
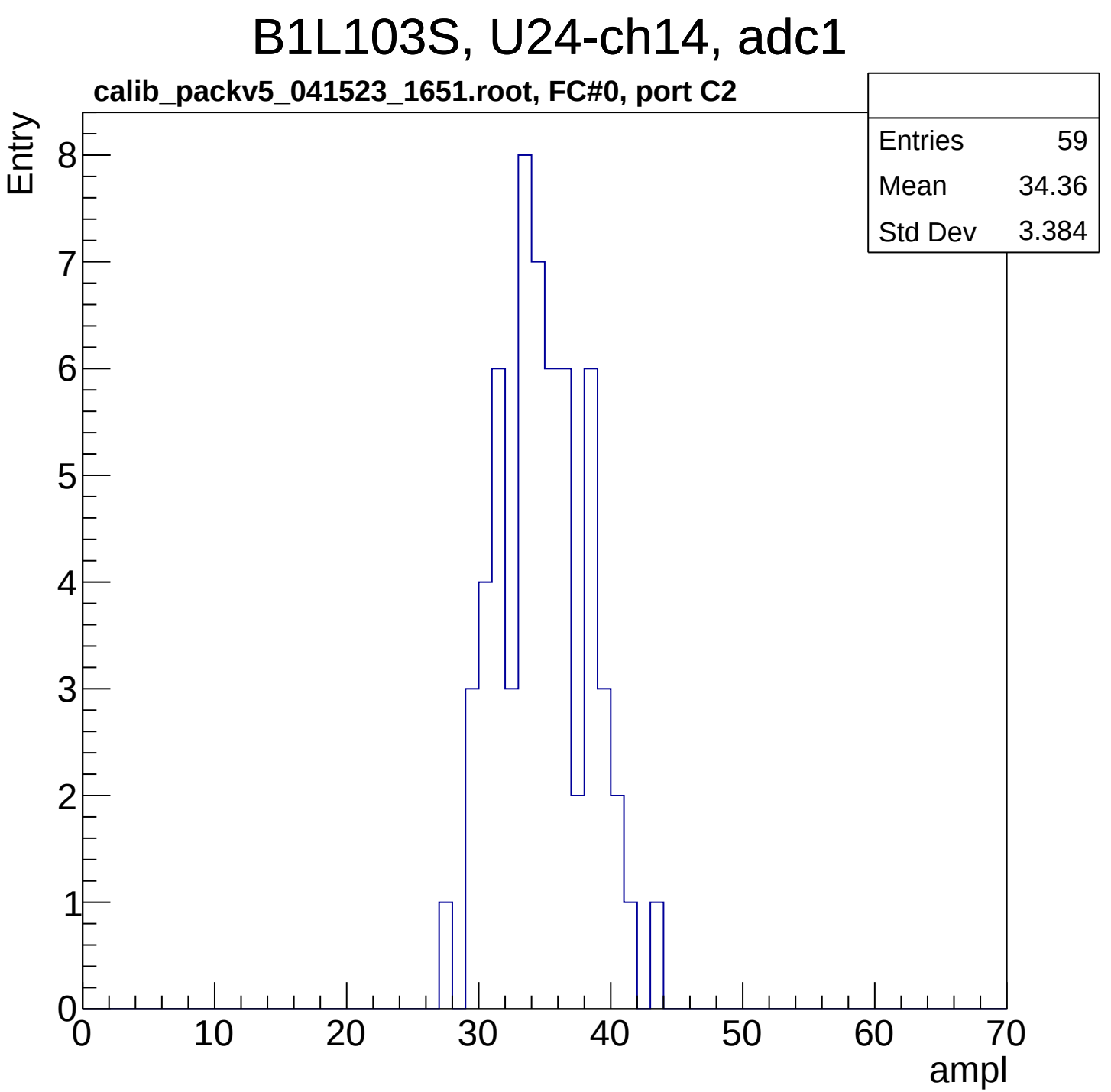
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U24-ch13, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 4
Mean 61.25
Std Dev 1.299
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U24-ch13, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1
Std Dev 4.243
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch14, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 25.71
Std Dev 8.983
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch14, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 34.36
Std Dev 3.384
Entry
ampl
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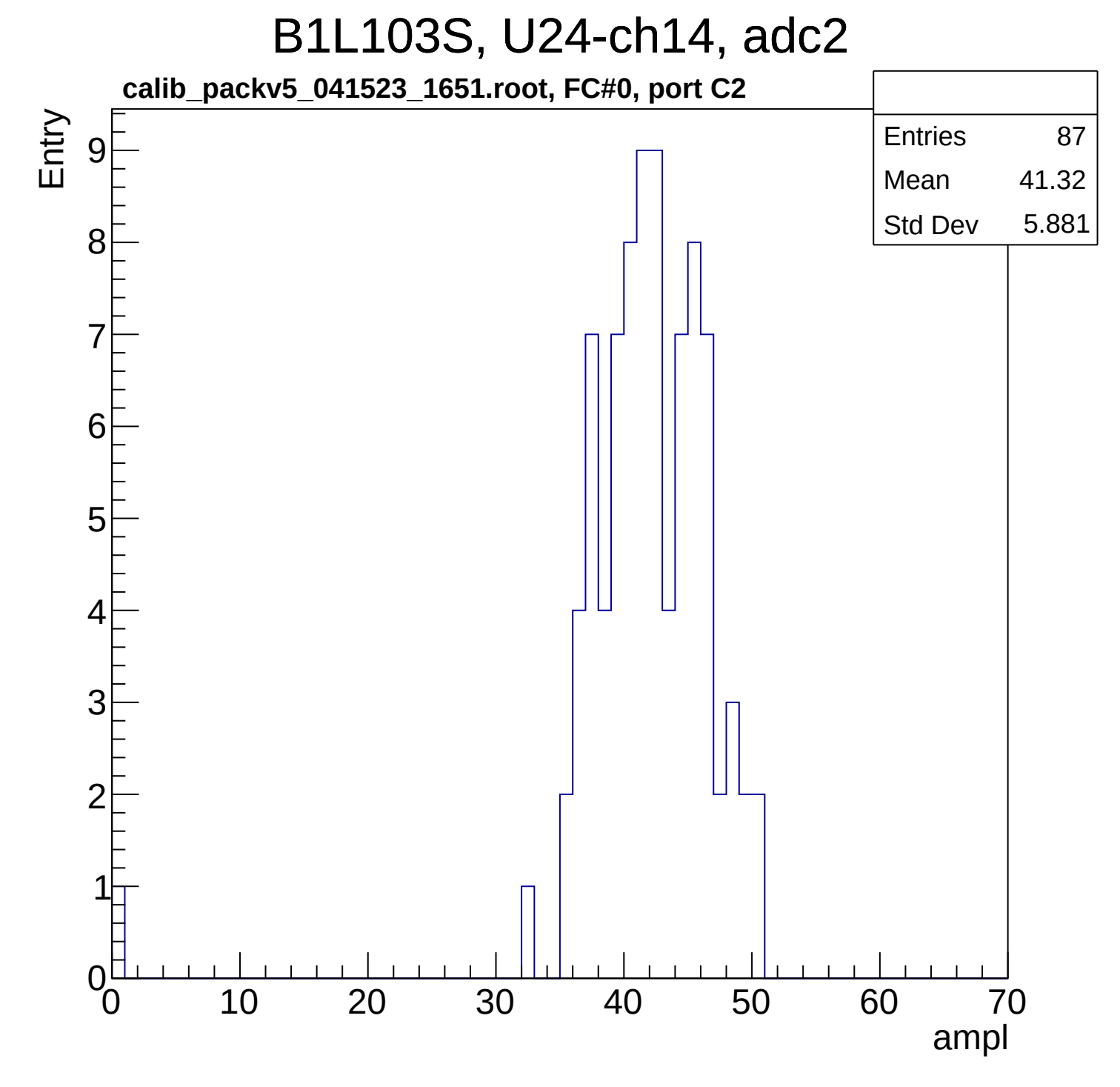
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U24-ch14, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 87
Mean 41.32
Std Dev 5.881
Entry
ampl
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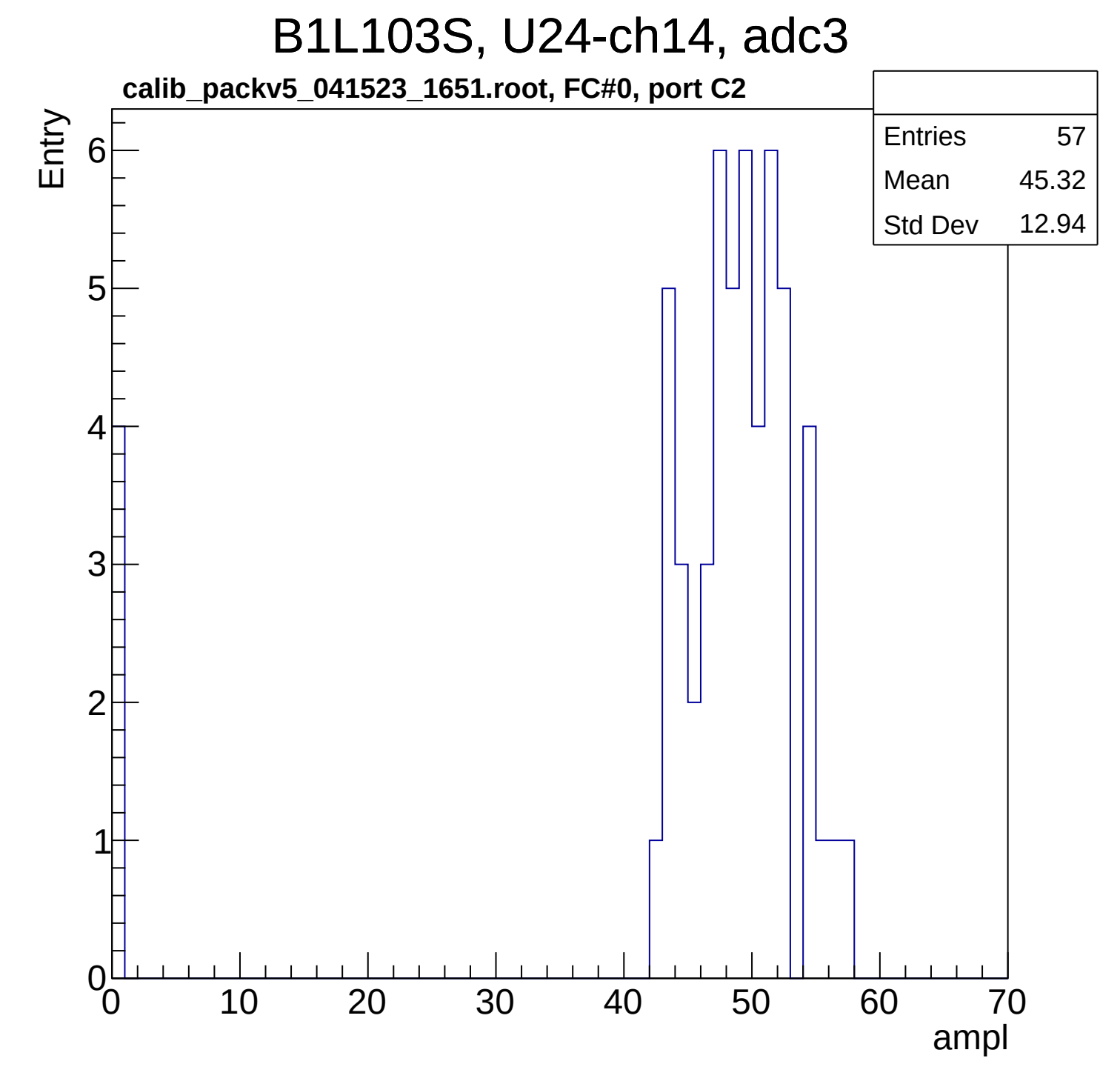
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U24-ch14, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 45.32
Std Dev 12.94
Entry
ampl
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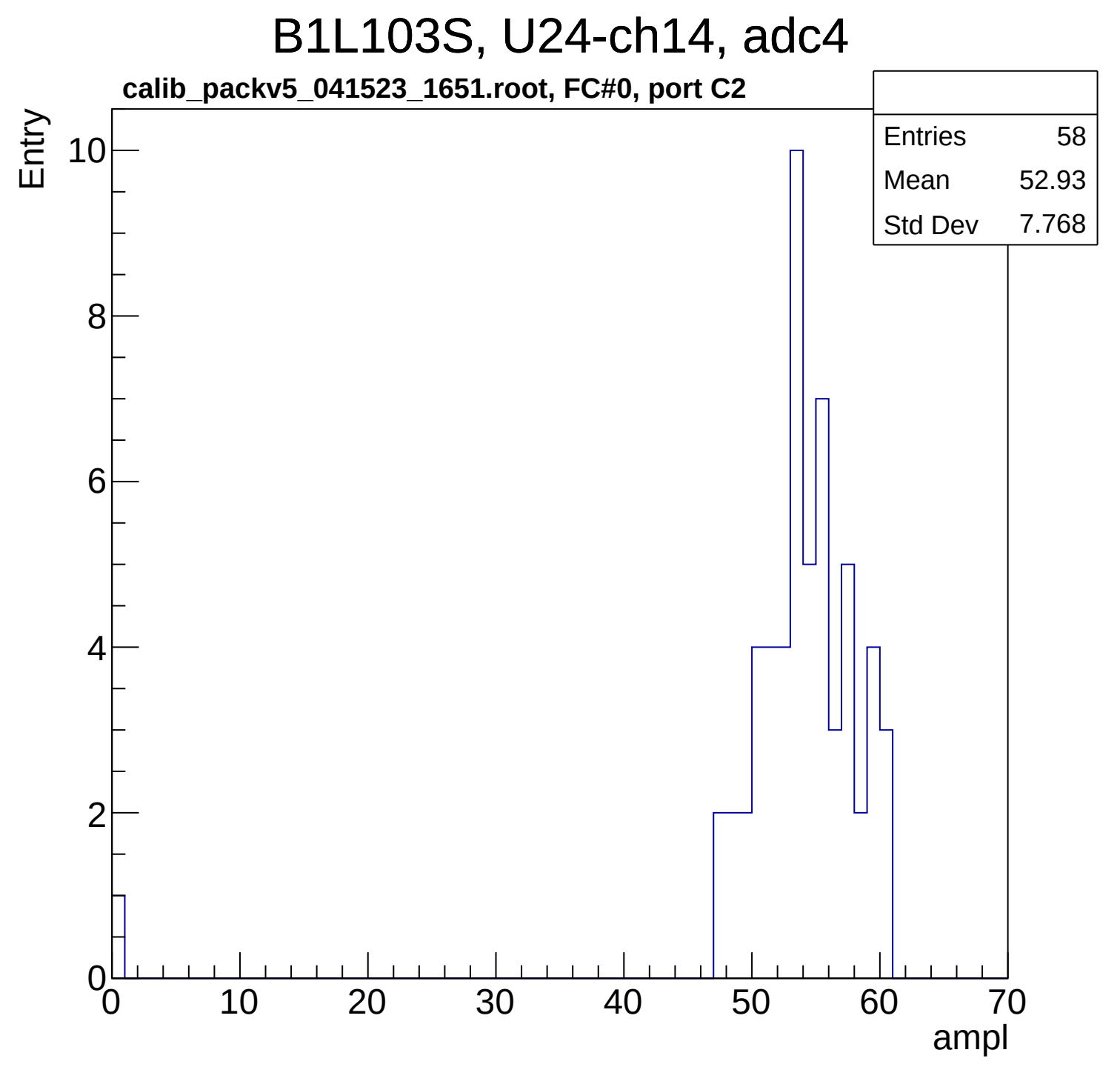
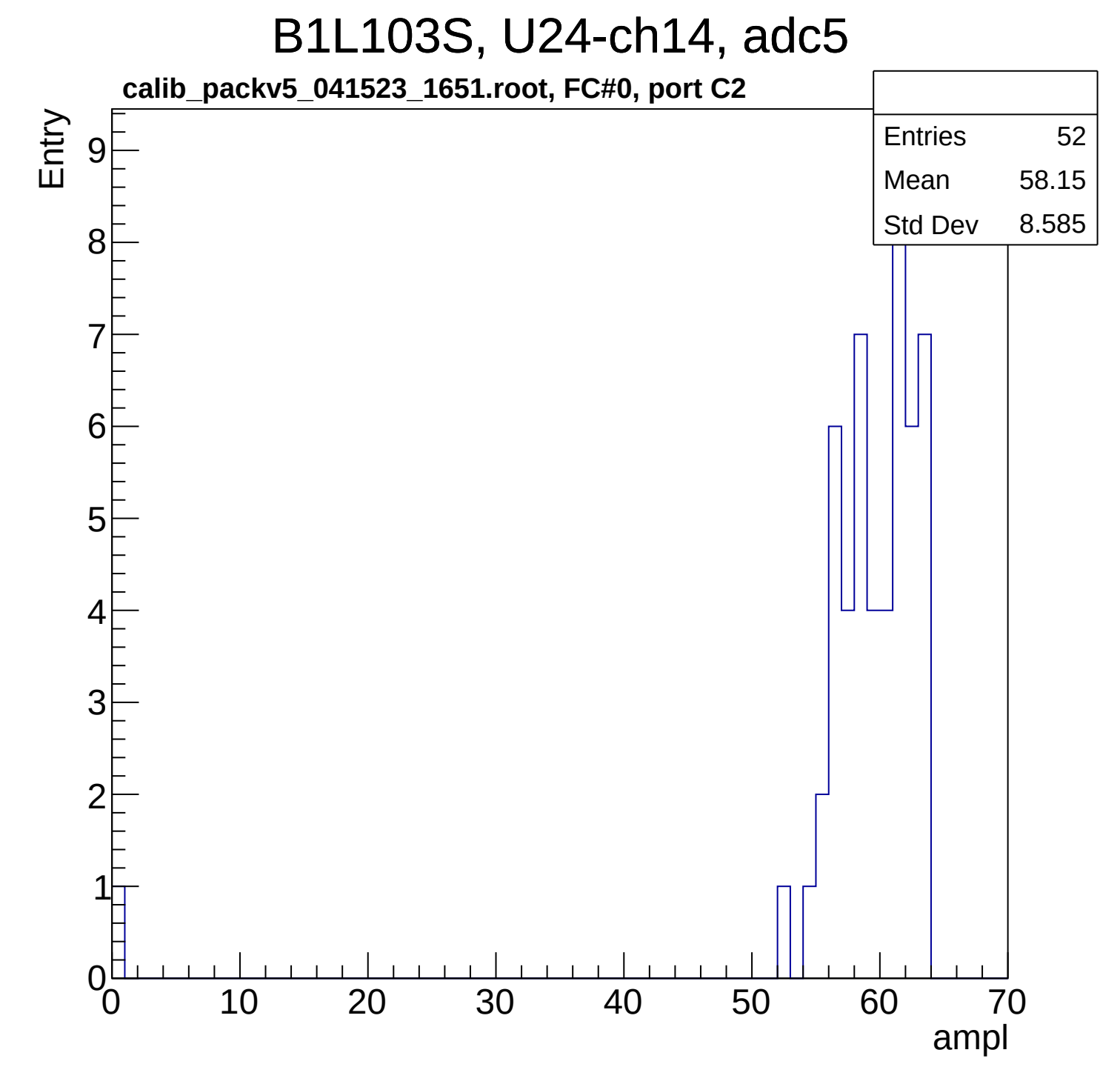
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U24-ch14, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 52.93
Std Dev 7.768
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U24-ch14, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 58.15
Std Dev 8.585
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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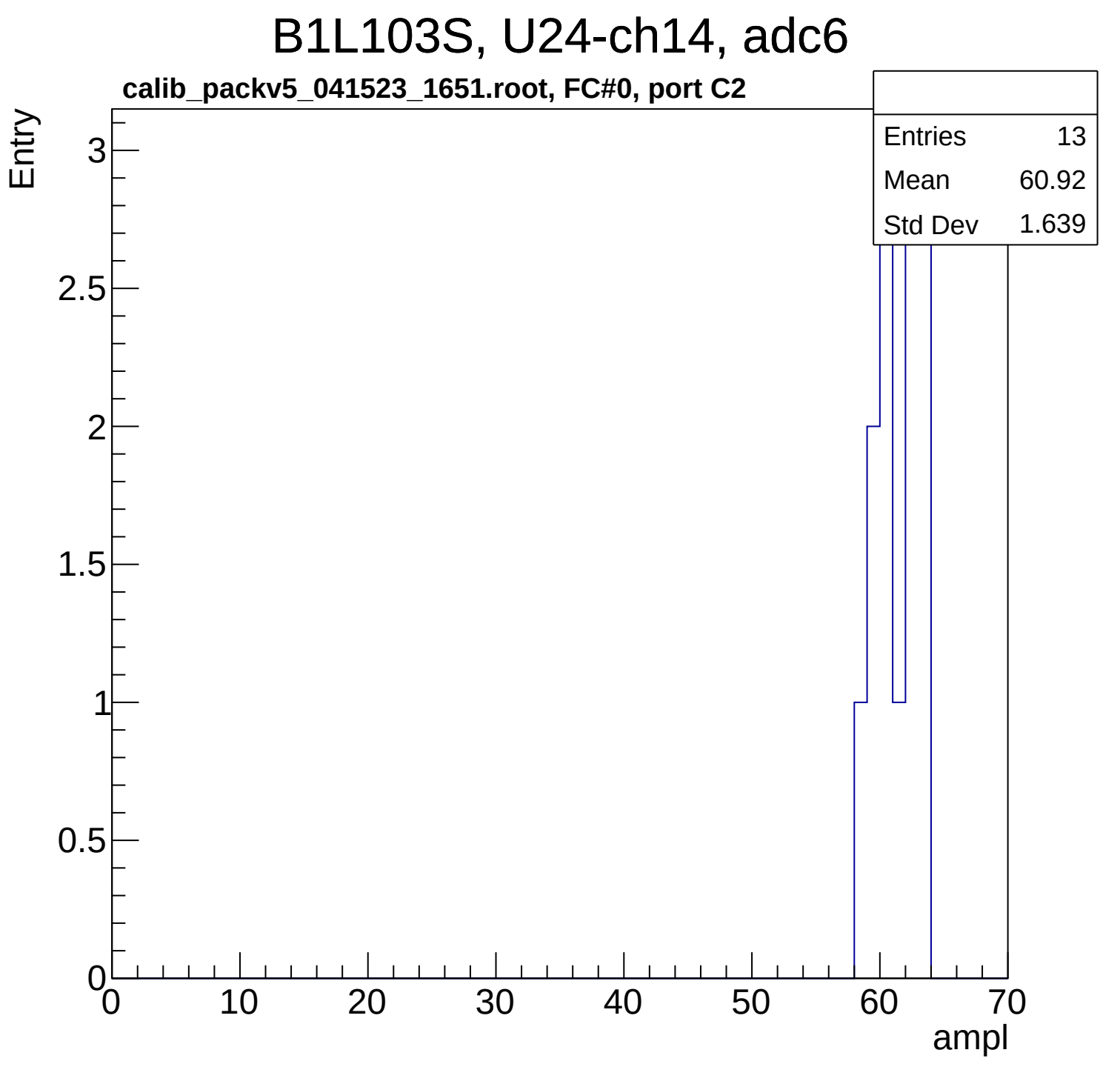
40
50
60
70


B1L103S, U24-ch14, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 13
Mean 60.92
Std Dev 1.639
Entry
ampl
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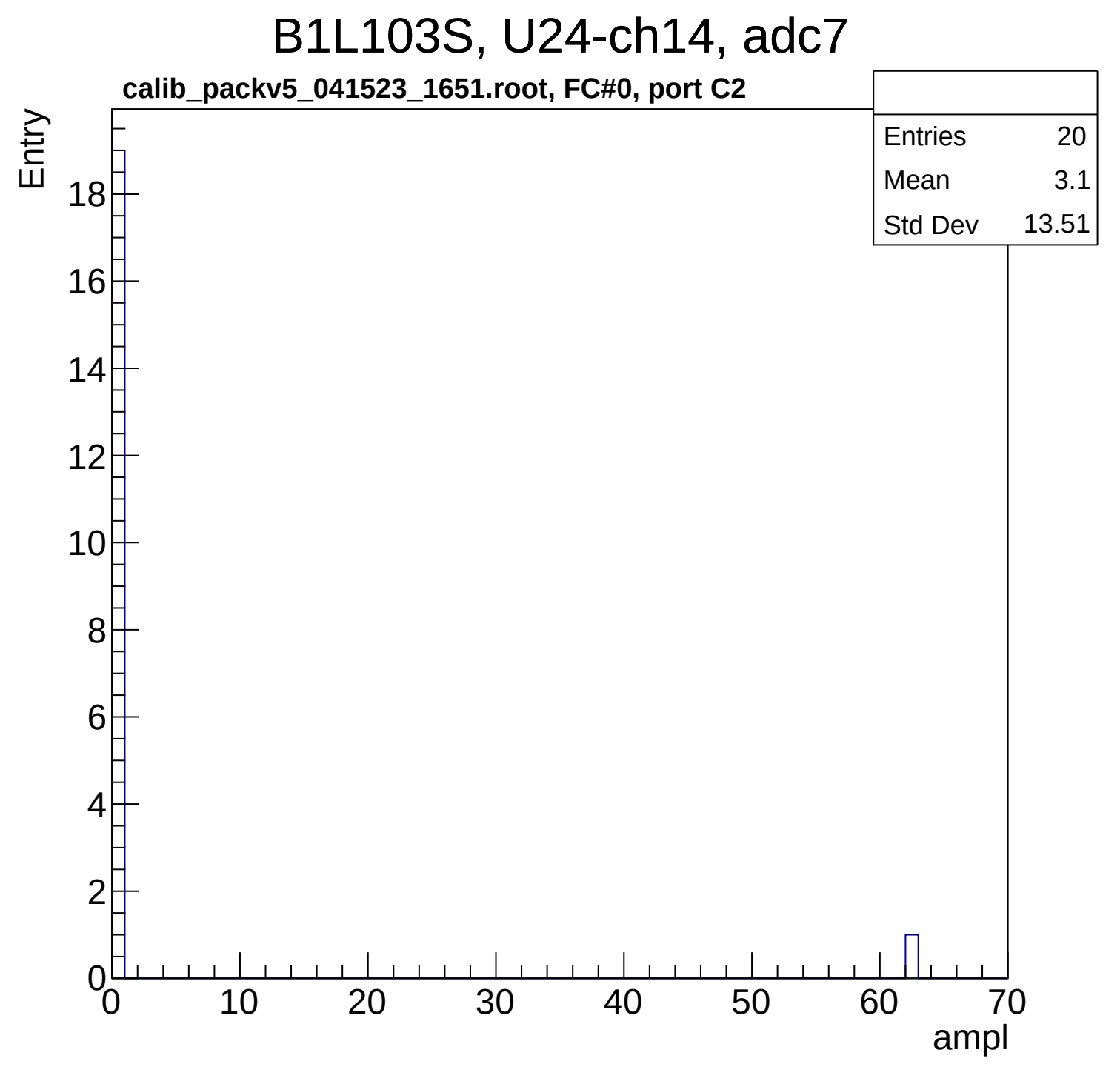
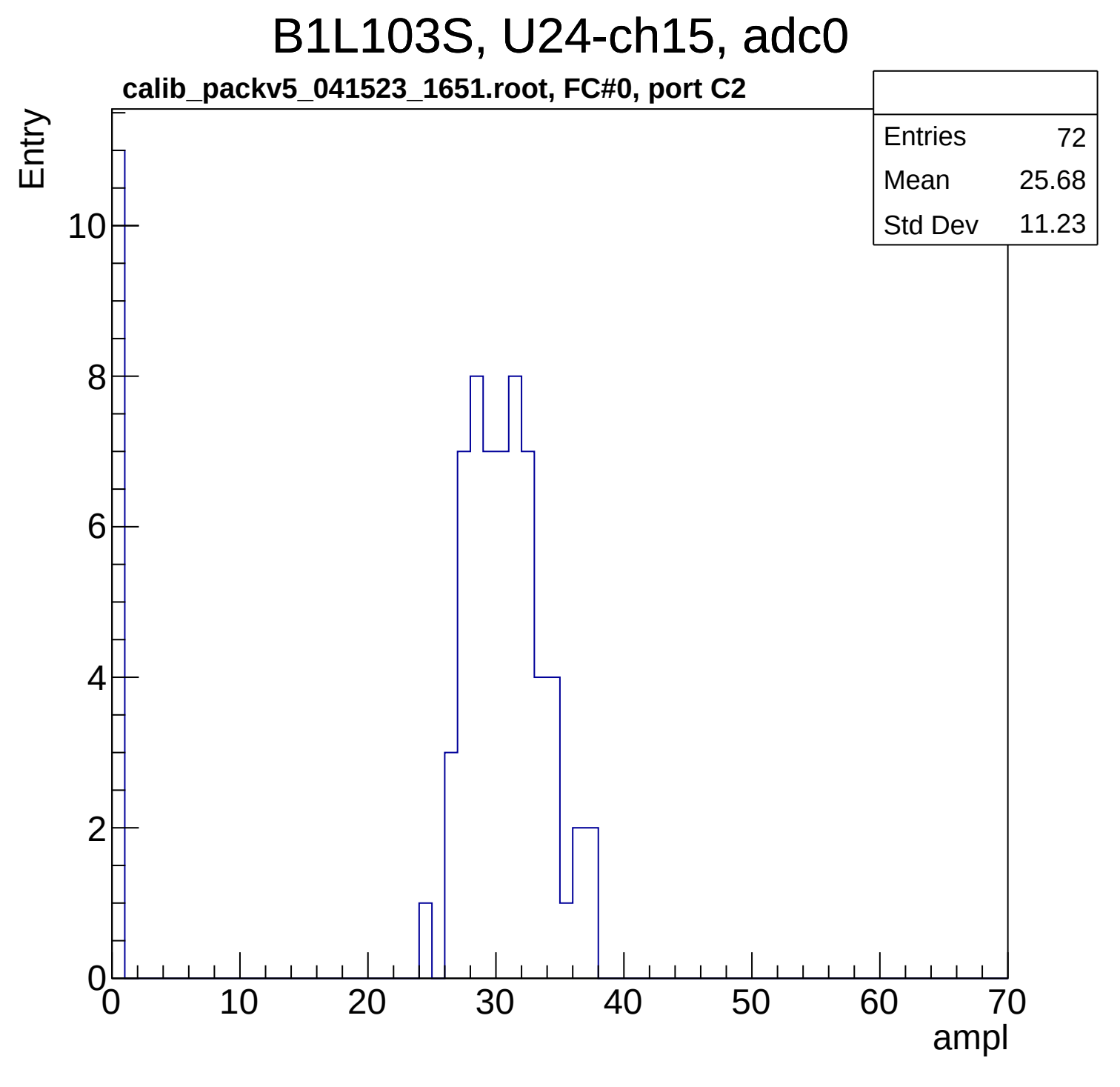
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U24-ch14, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.1
Std Dev 13.51
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch15, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 25.68
Std Dev 11.23
Entry
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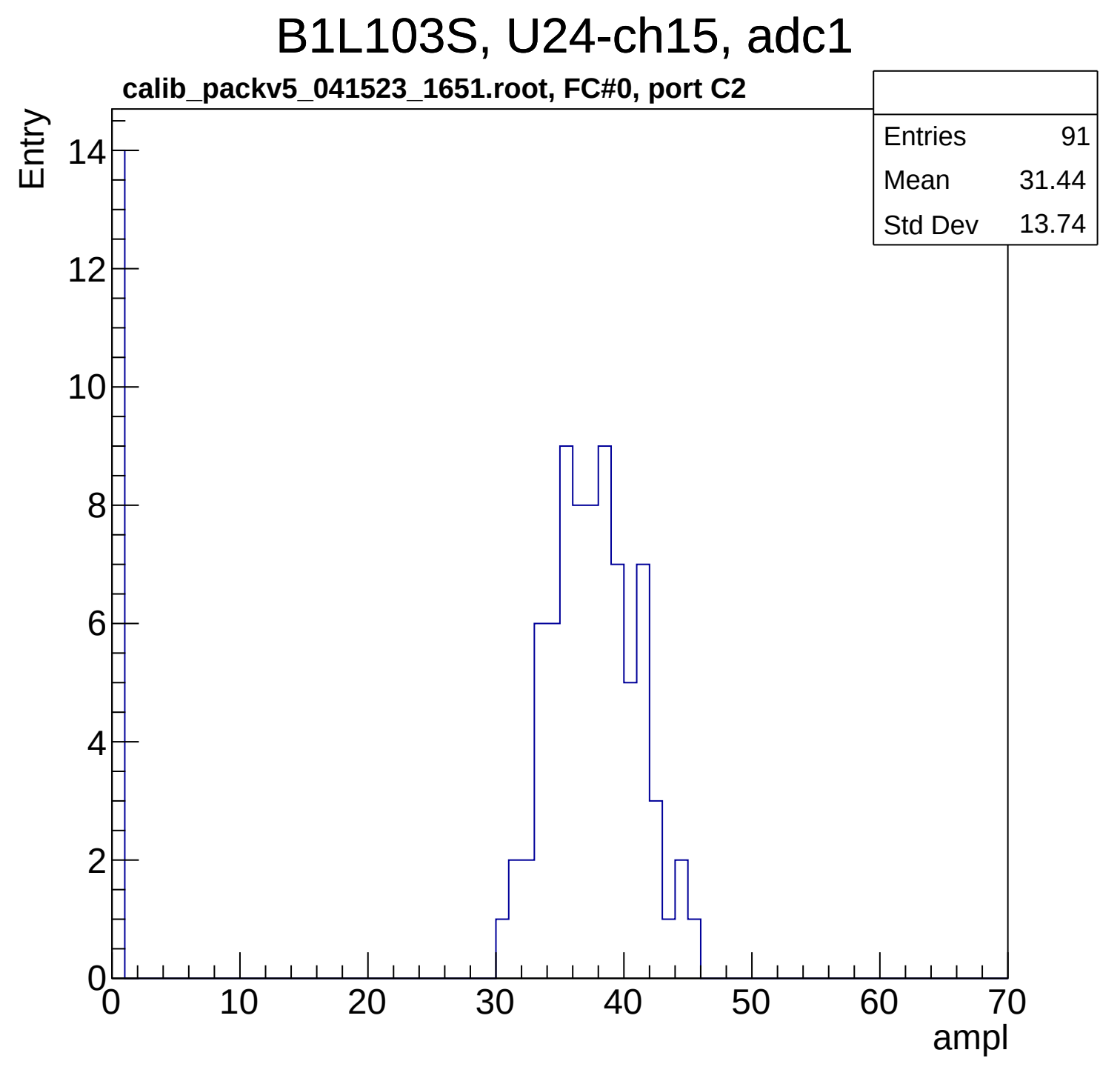
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch15, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 91
Mean 31.44
Std Dev 13.74
Entry
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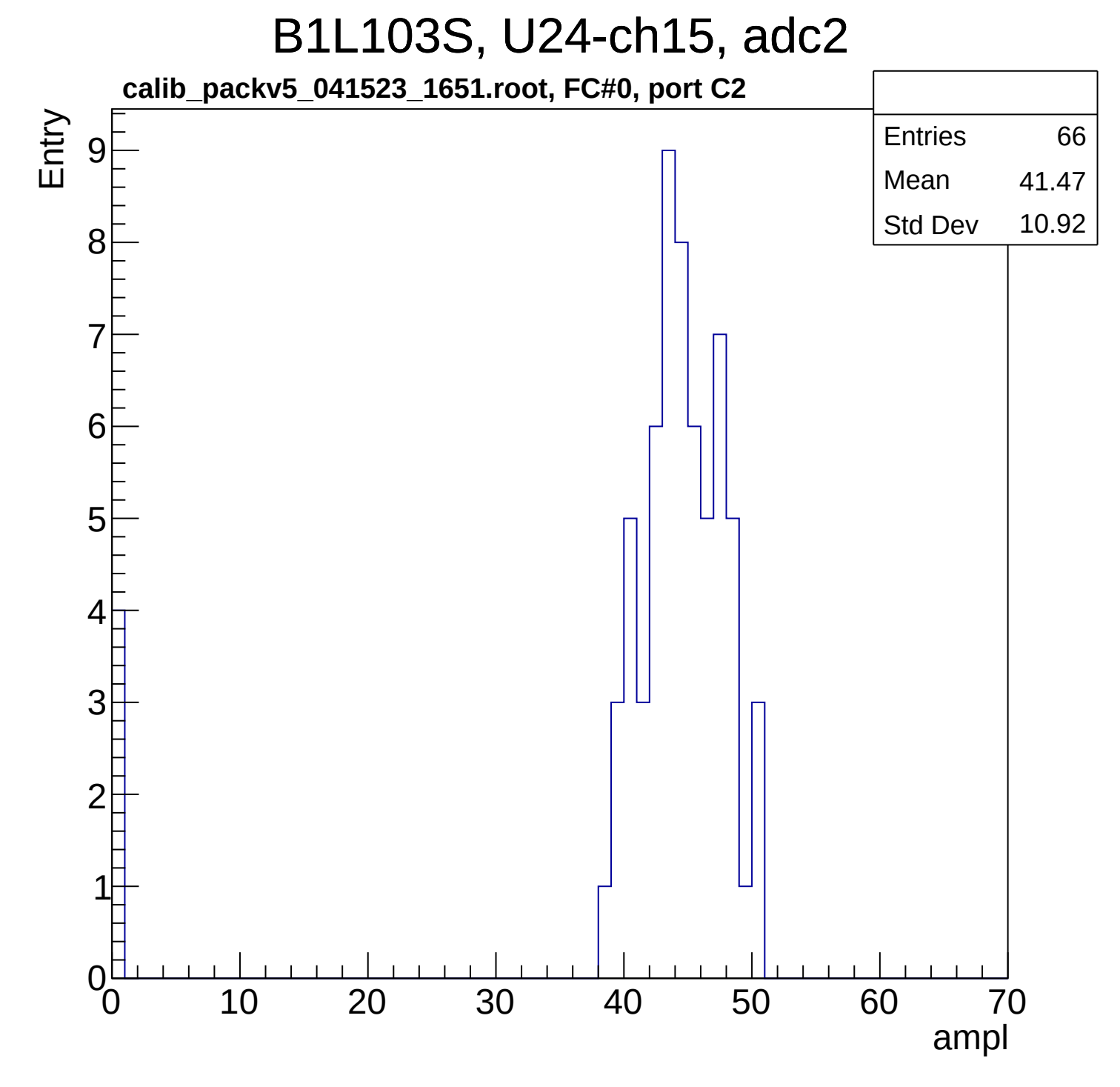
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch15, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 41.47
Std Dev 10.92
Entry
ampl
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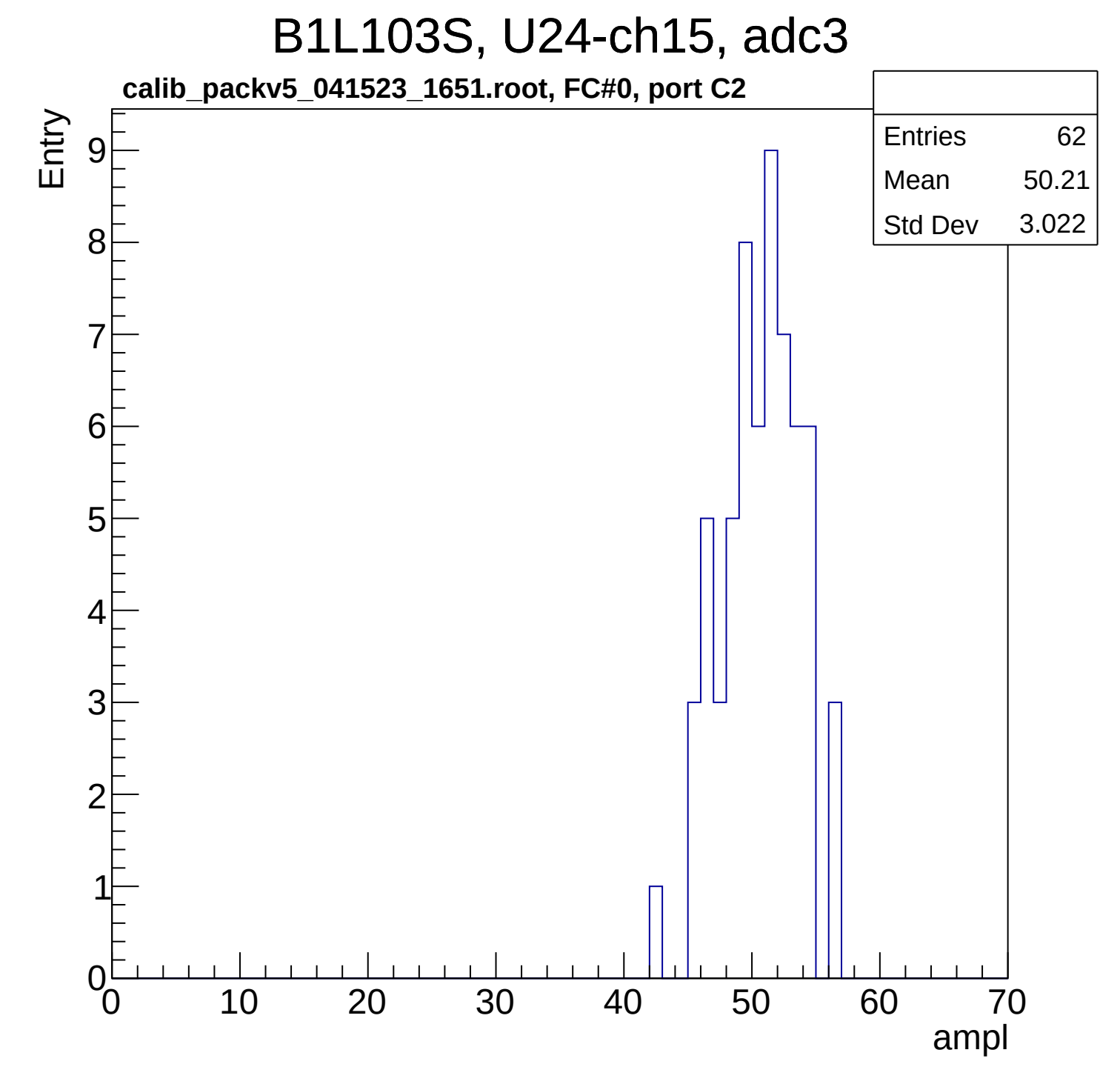
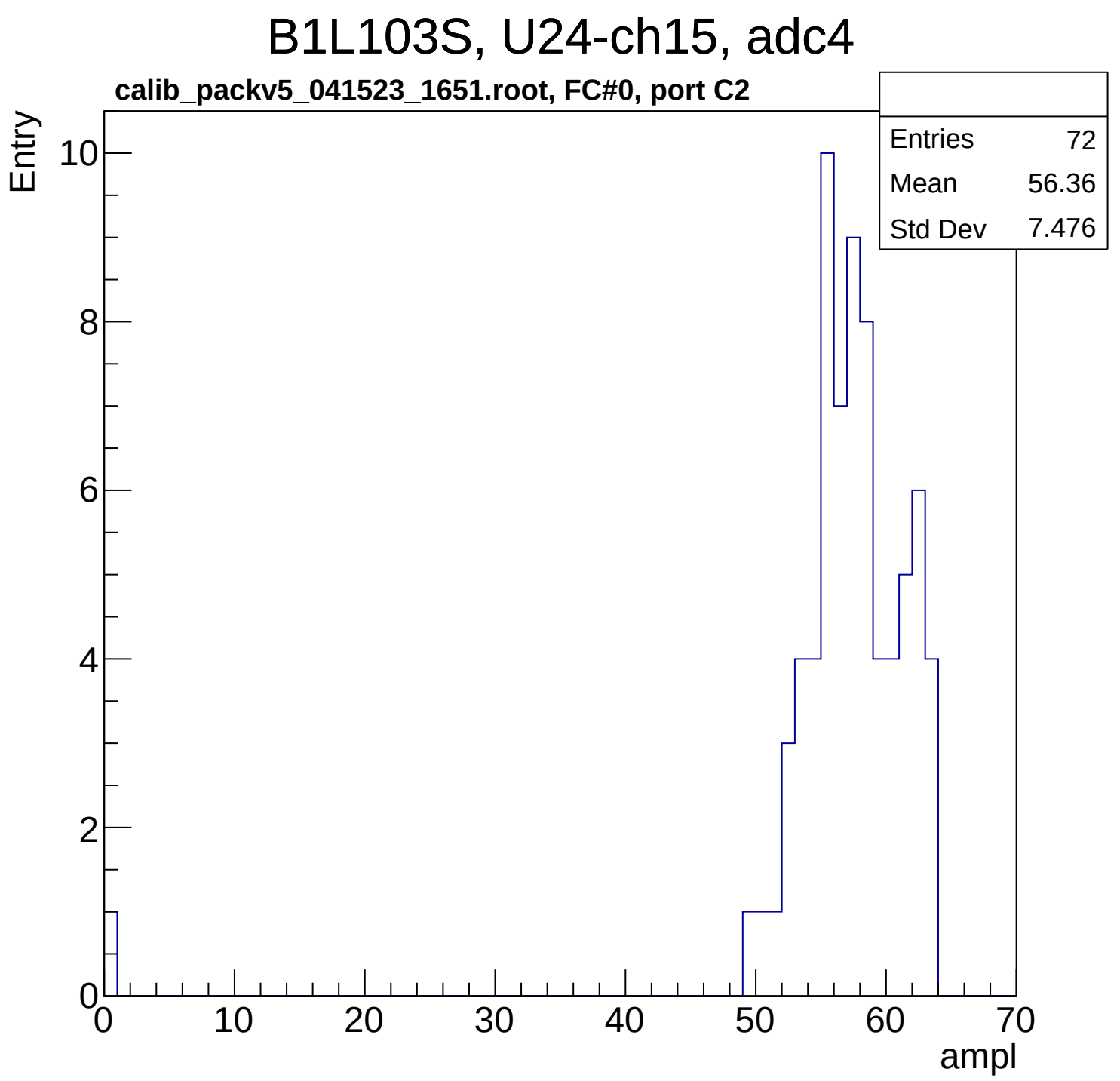
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U24-ch15, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 50.21
Std Dev 3.022
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U24-ch15, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 56.36
Std Dev 7.476
Entry
0
2
4
6
8
10
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10
20
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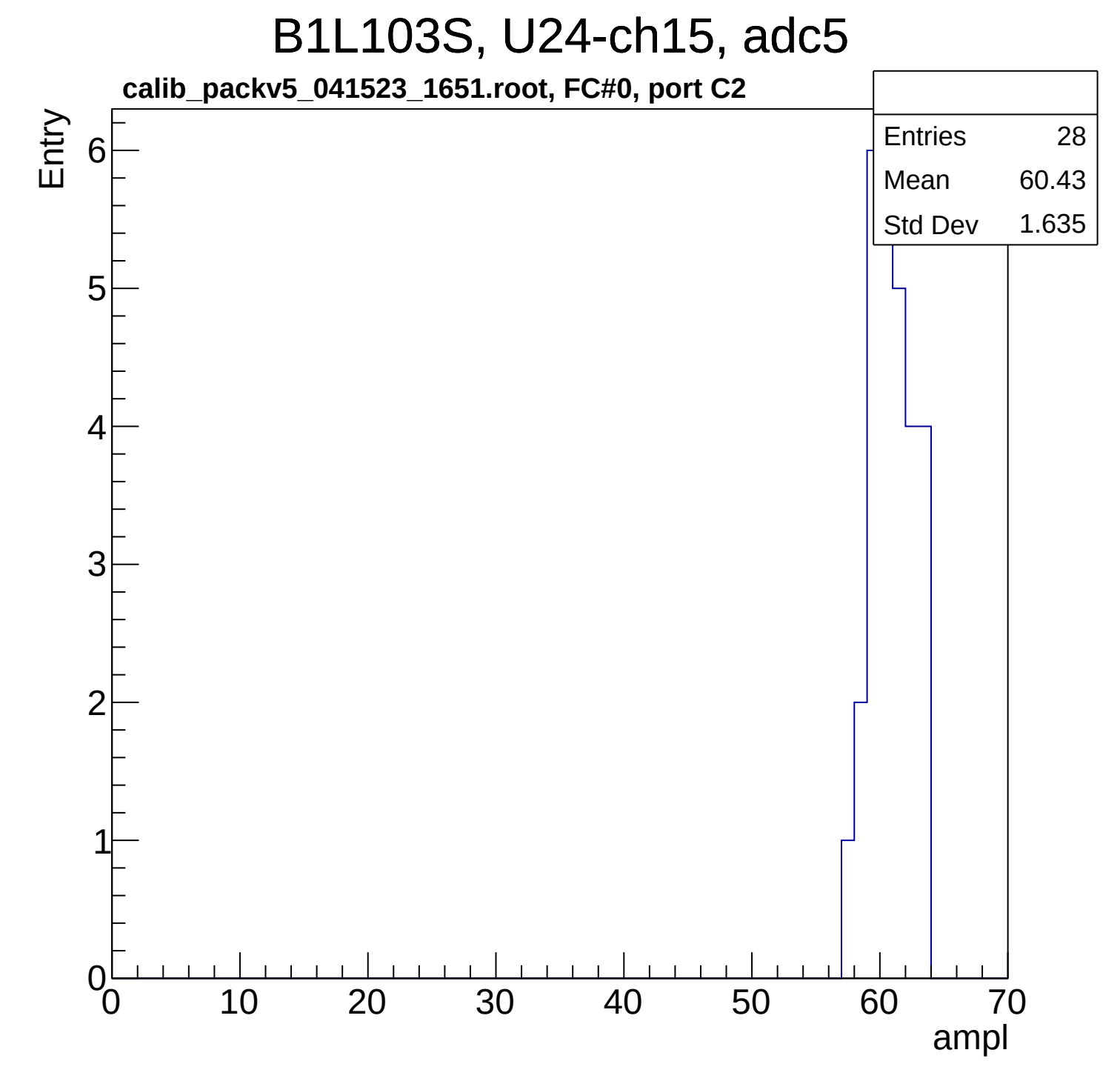
50
60
70
ampl


B1L103S, U24-ch15, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 28
Mean 60.43
Std Dev 1.635
Entry
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2
3
4
5
6
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10
20
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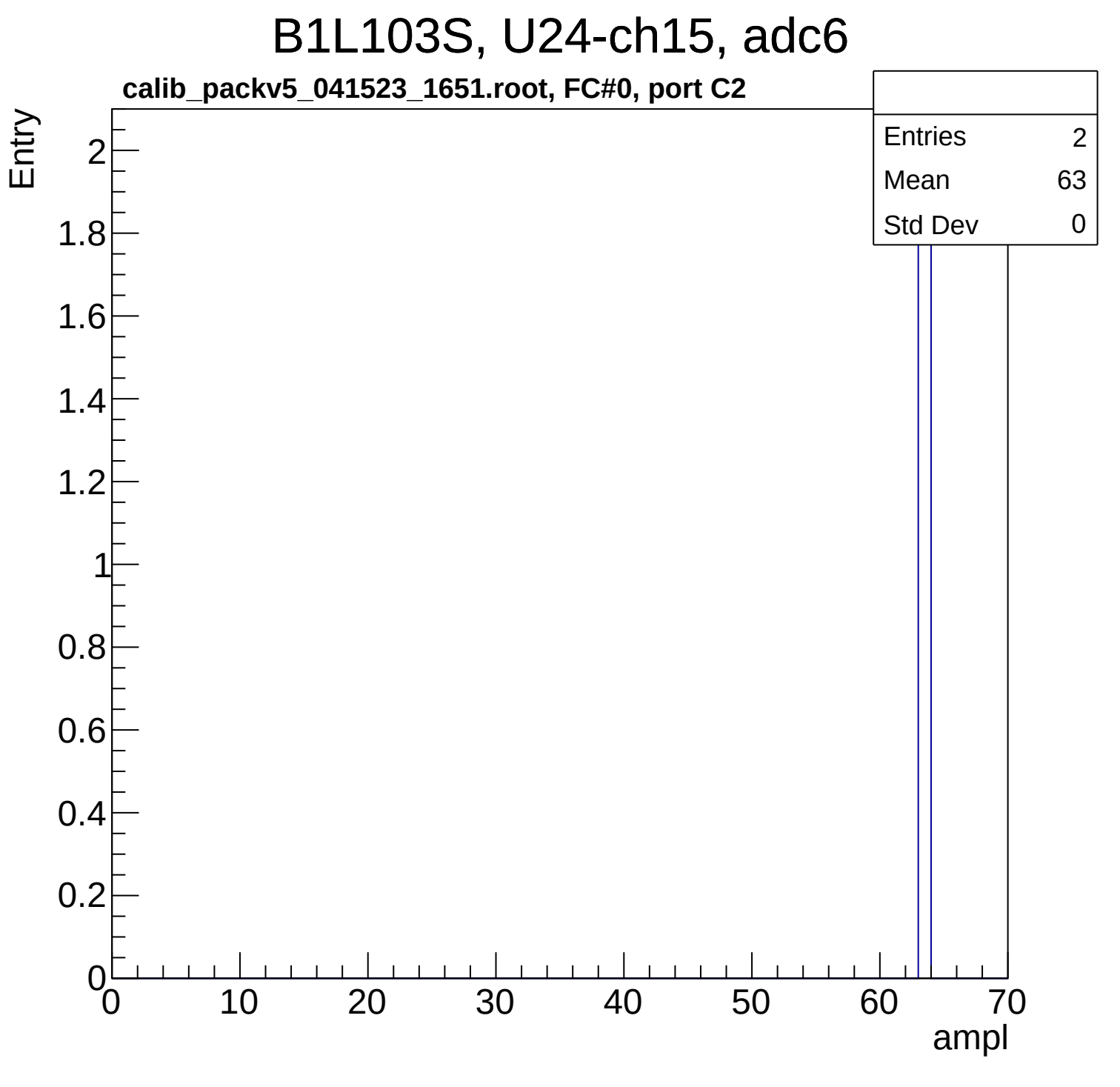
50
60
70
ampl


B1L103S, U24-ch15, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 2
Mean 63
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
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40
50
60
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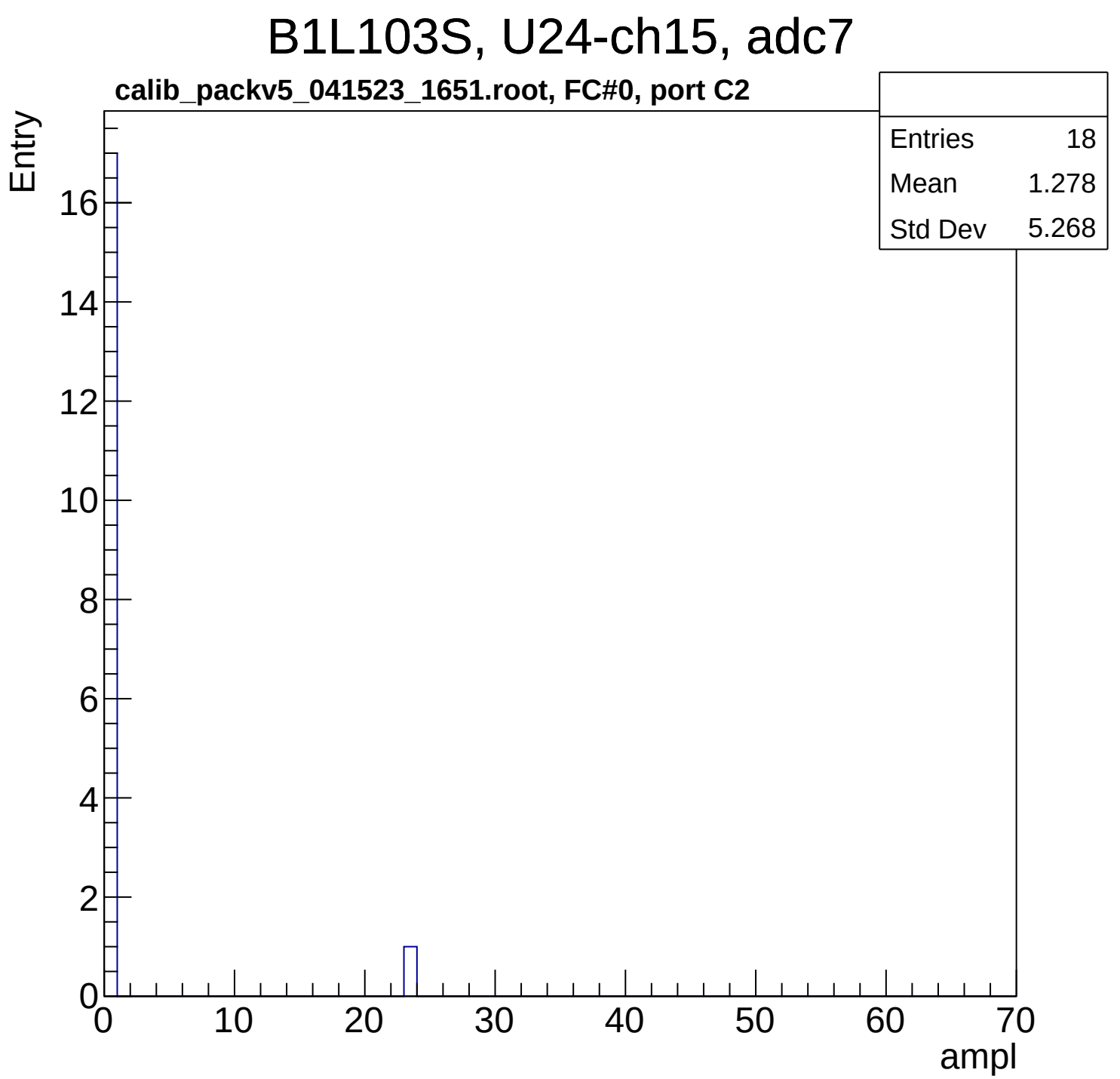
B1L103S, U24-ch15, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 1.278
Std Dev 5.268
Entry
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8
10
12
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16
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10
20
30
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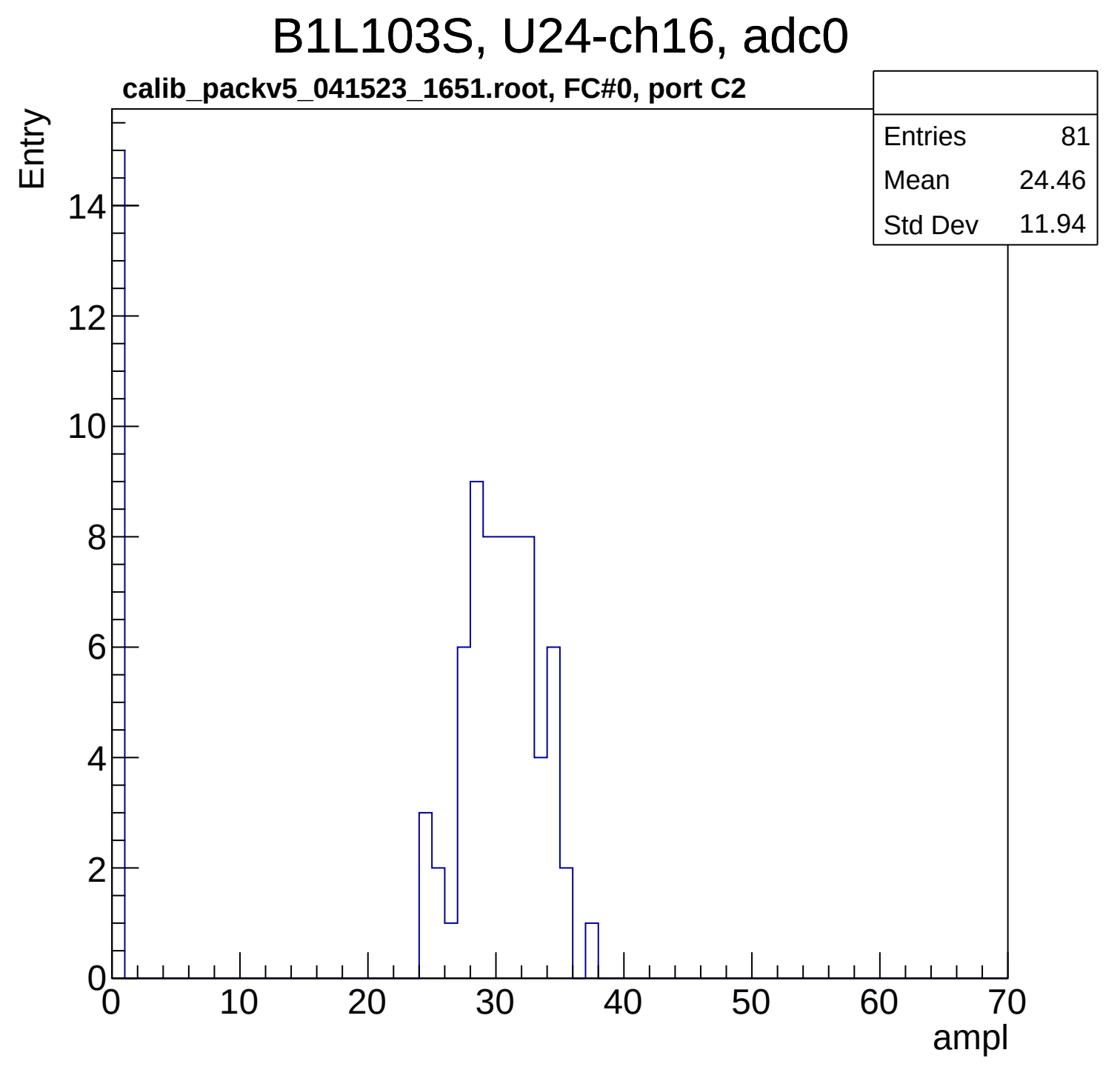
50
60
70
ampl


B1L103S, U24-ch16, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 24.46
Std Dev 11.94
Entry
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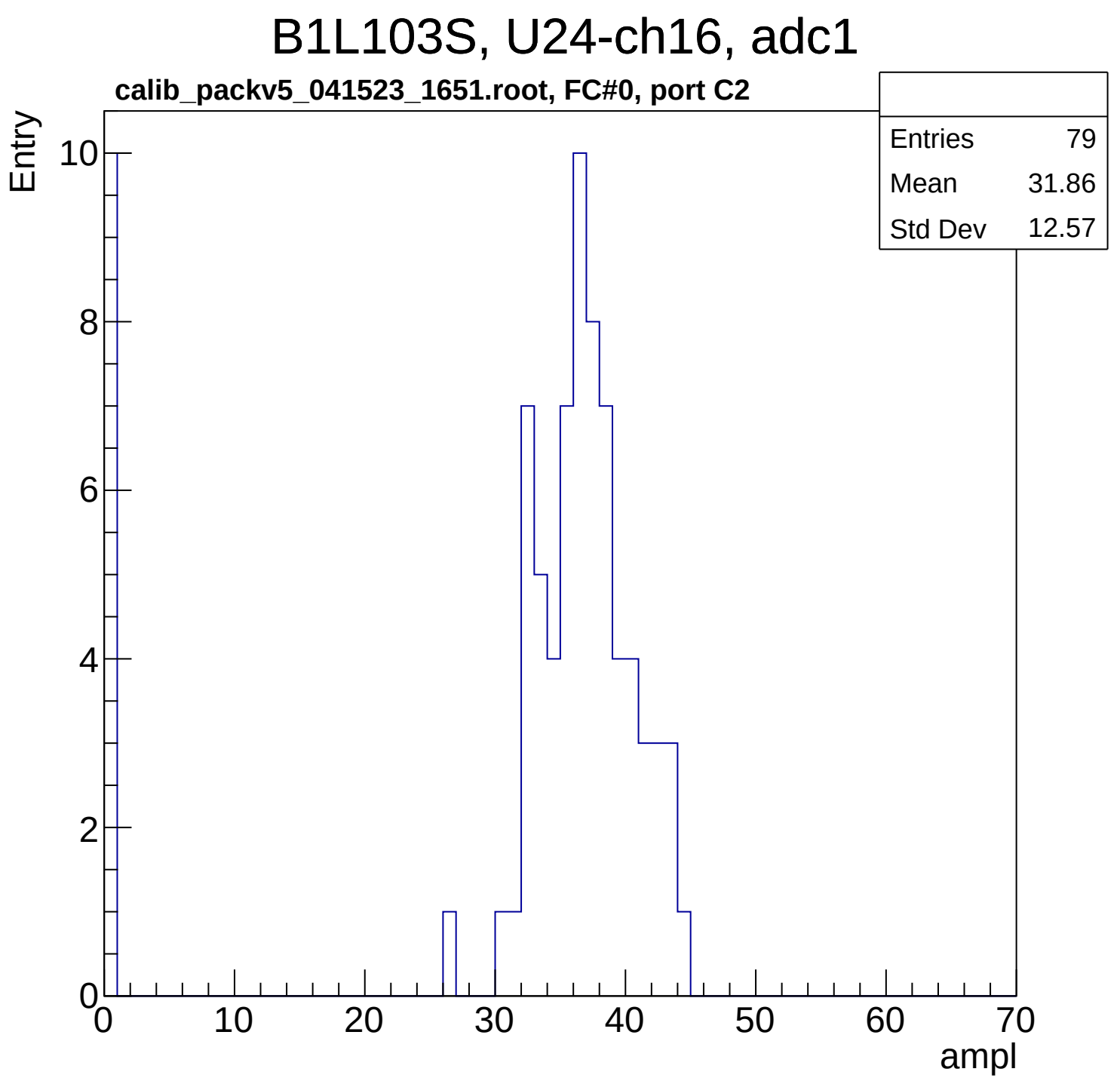
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch16, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 31.86
Std Dev 12.57
Entry
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6
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10
0
10
20
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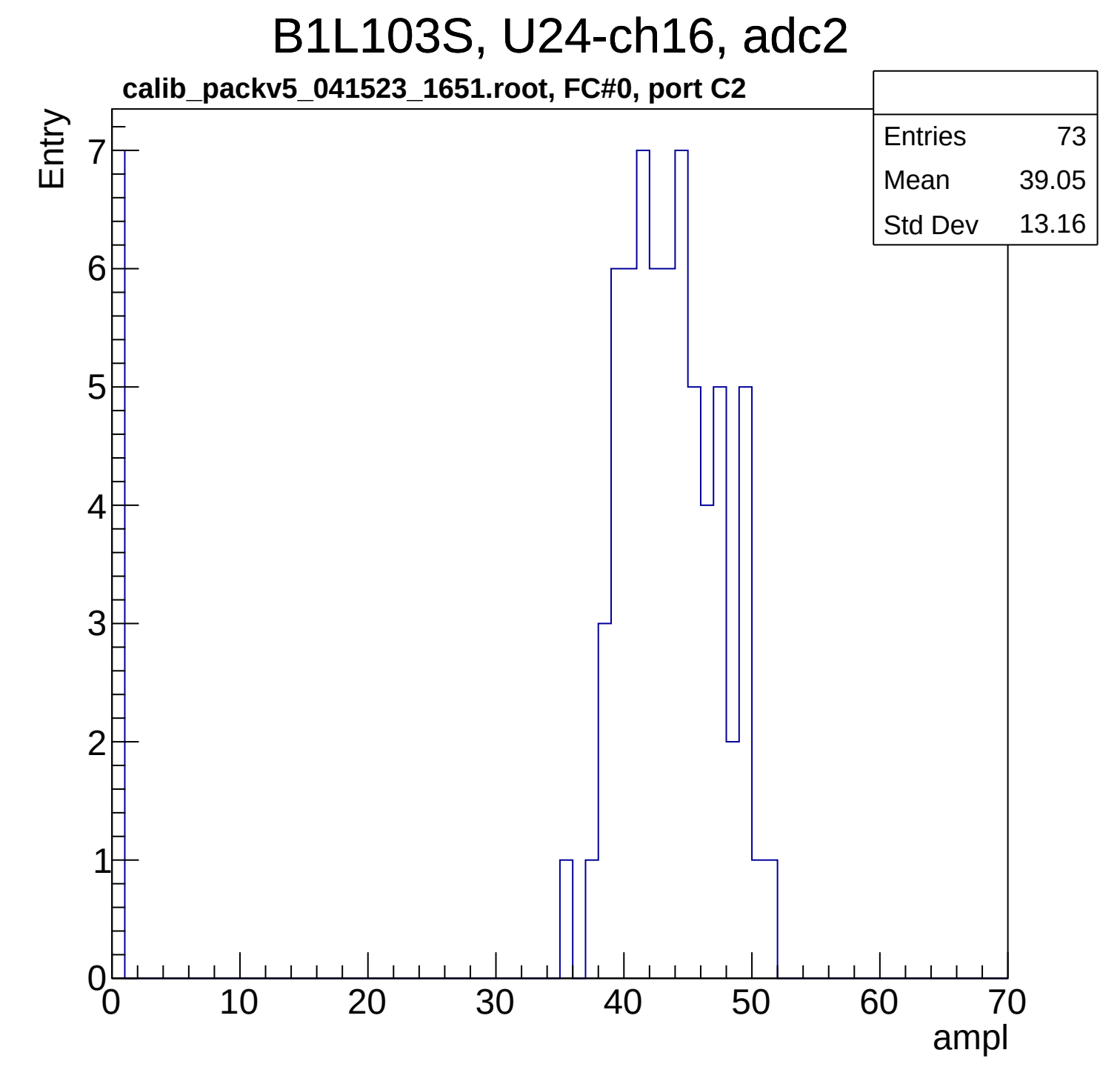
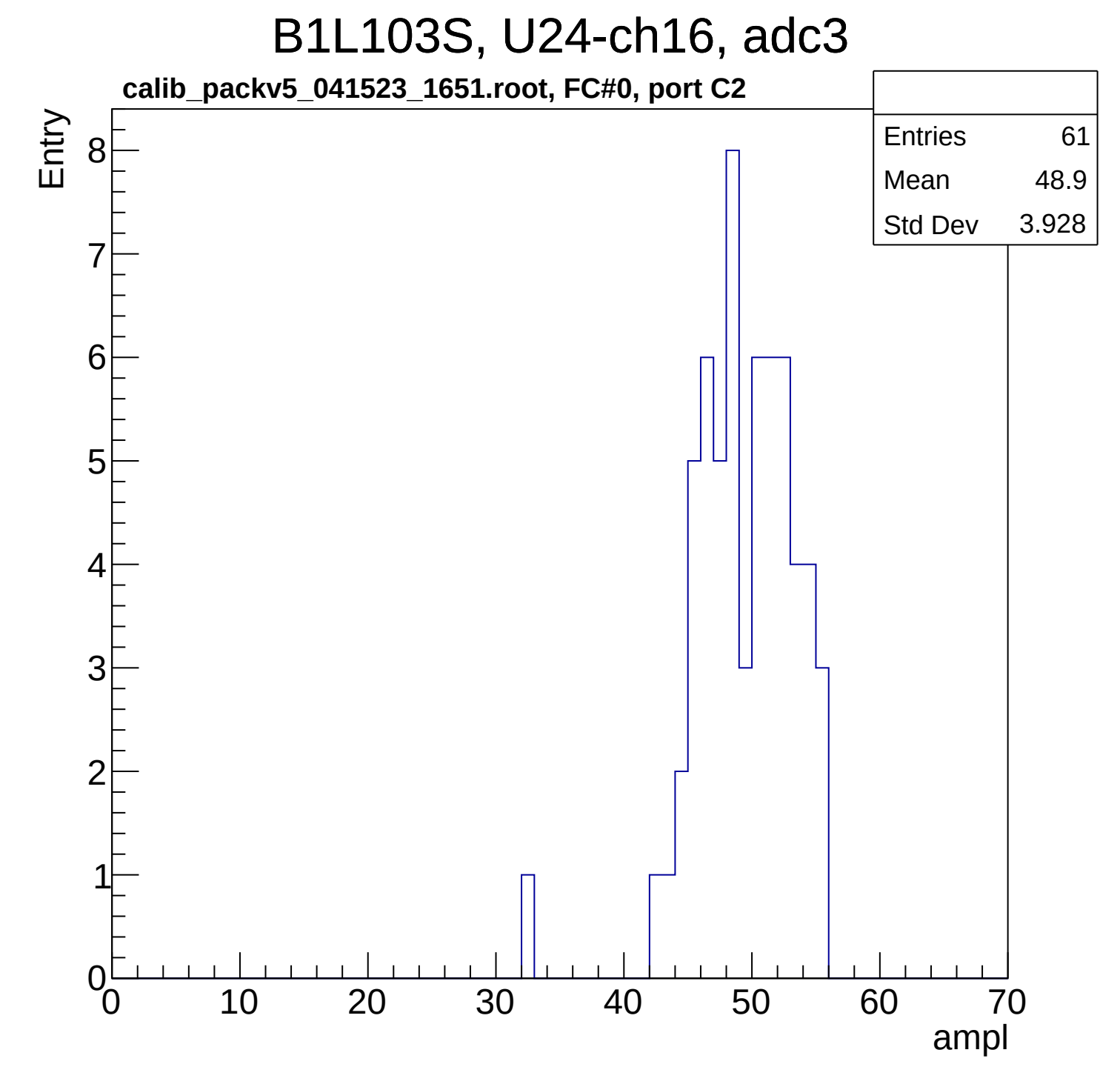
50
60
70
ampl


B1L103S, U24-ch16, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 39.05
Std Dev 13.16
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U24-ch16, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 48.9
Std Dev 3.928
Entry
ampl
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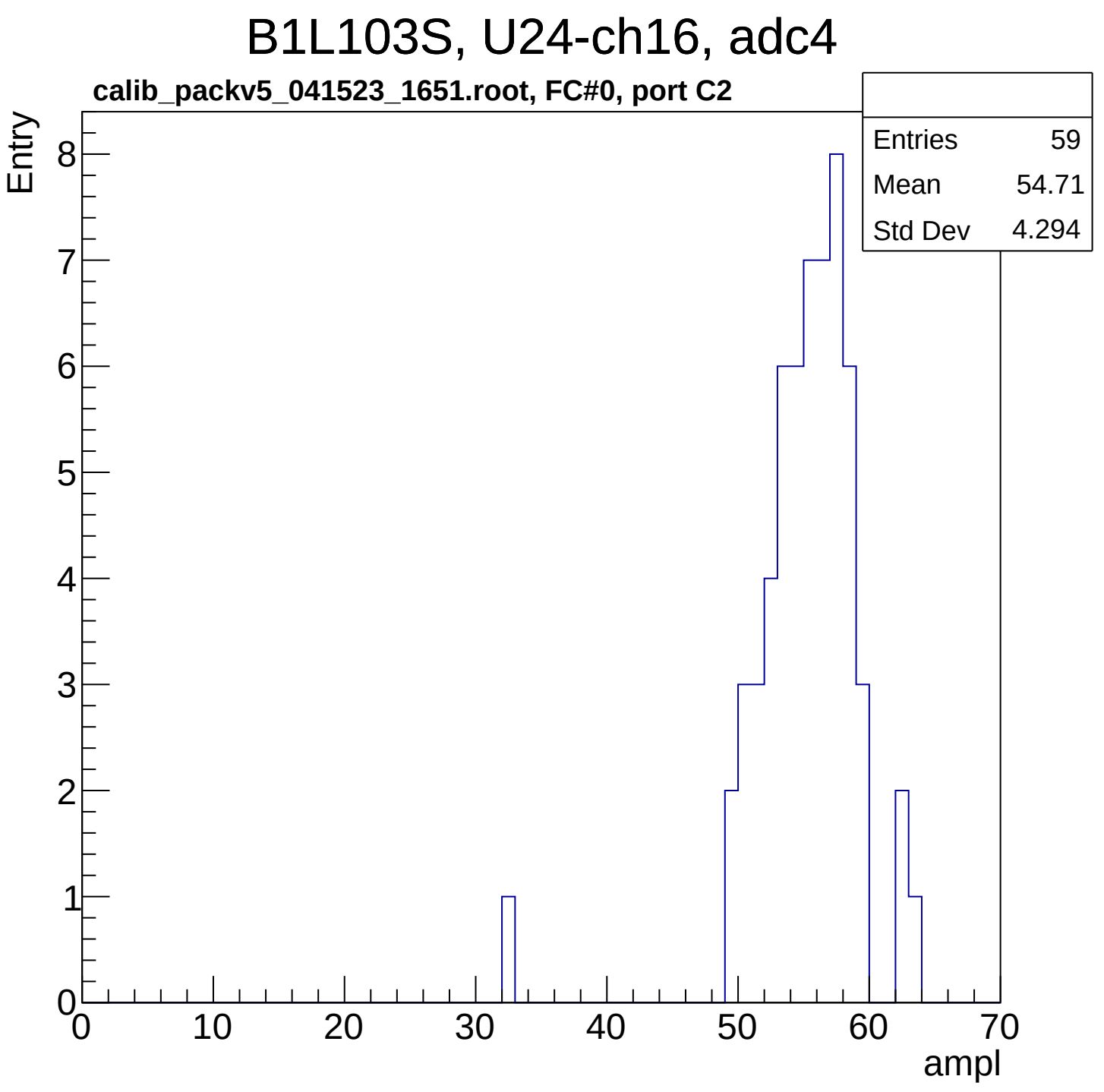
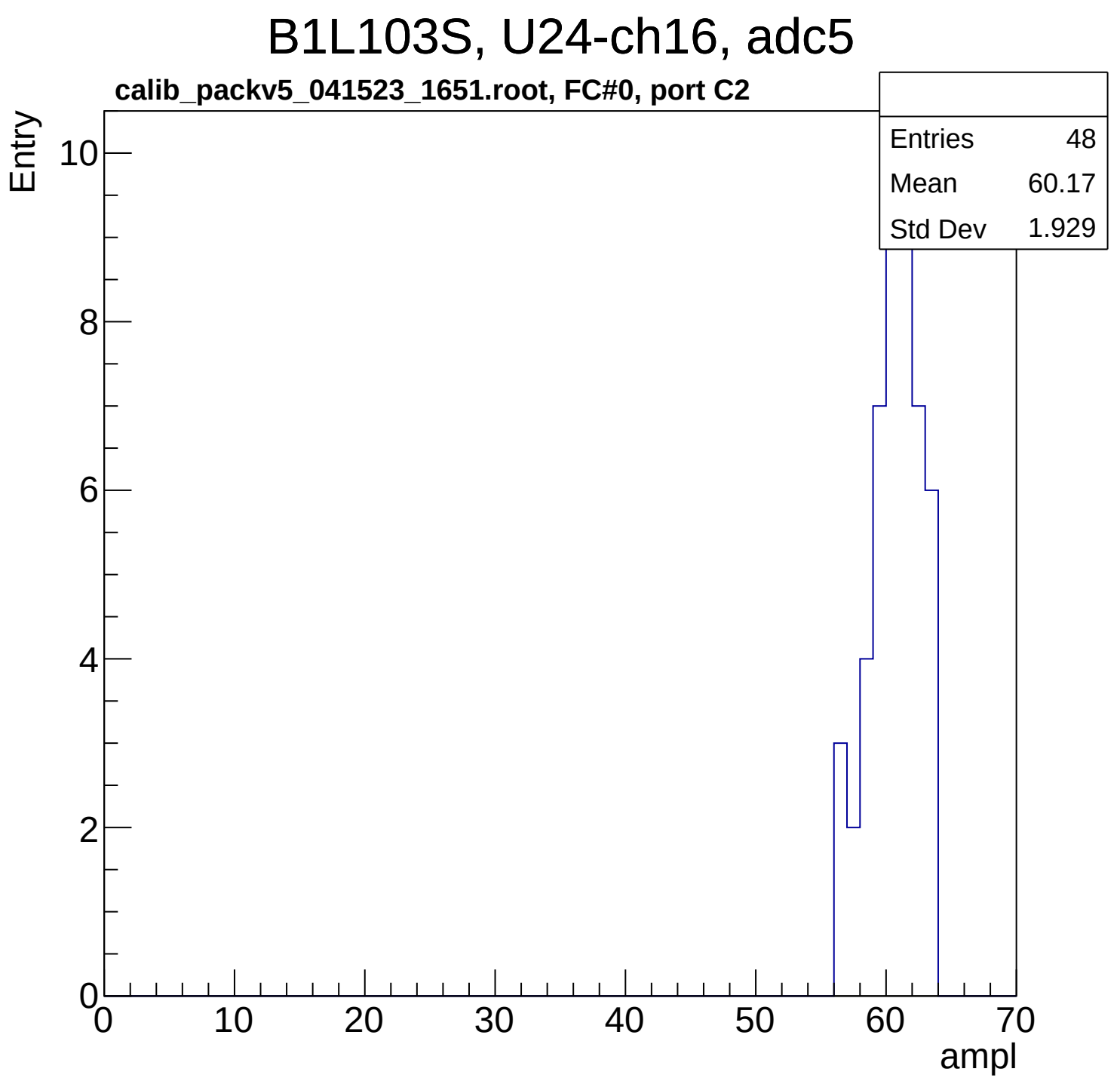
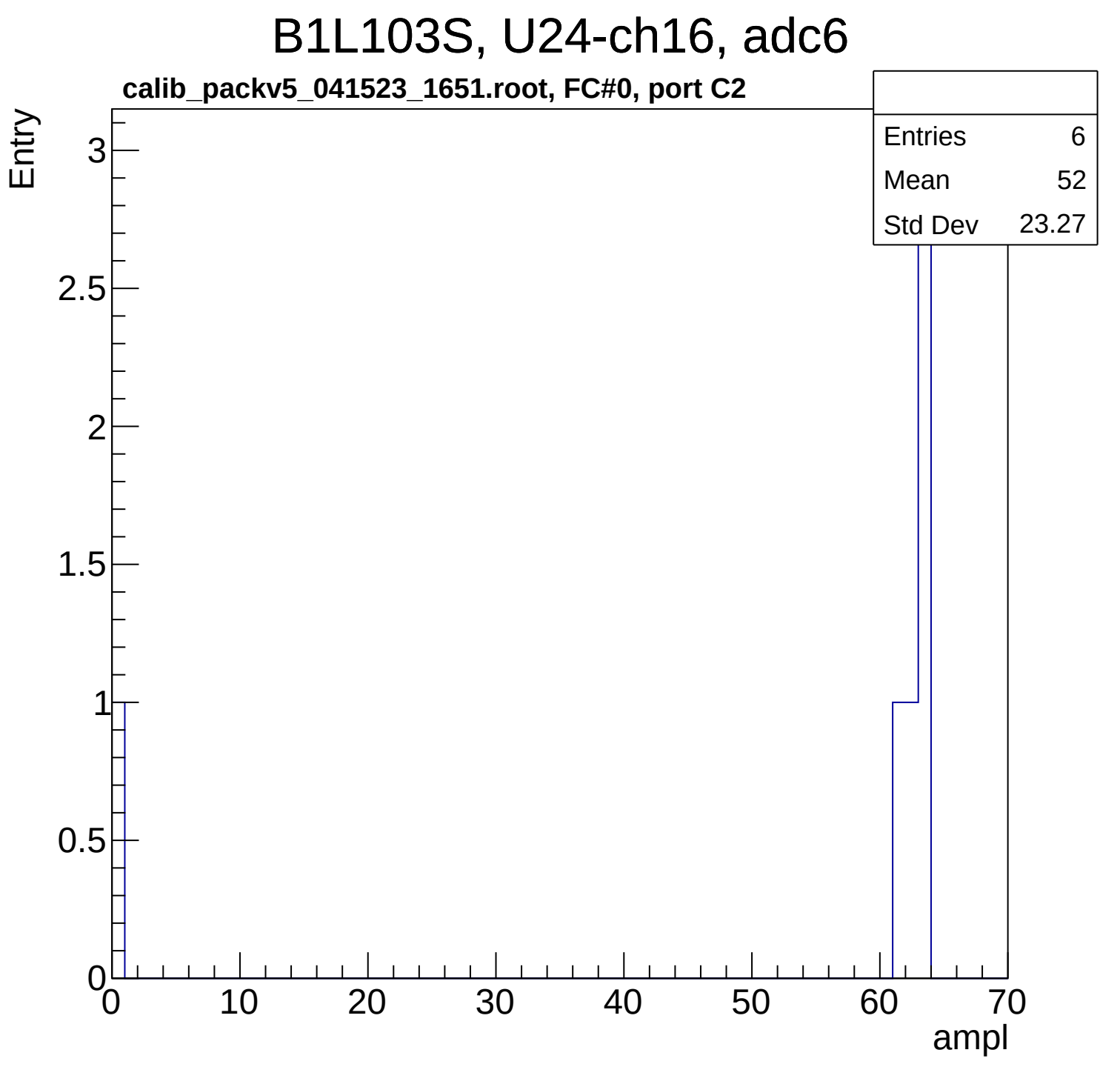
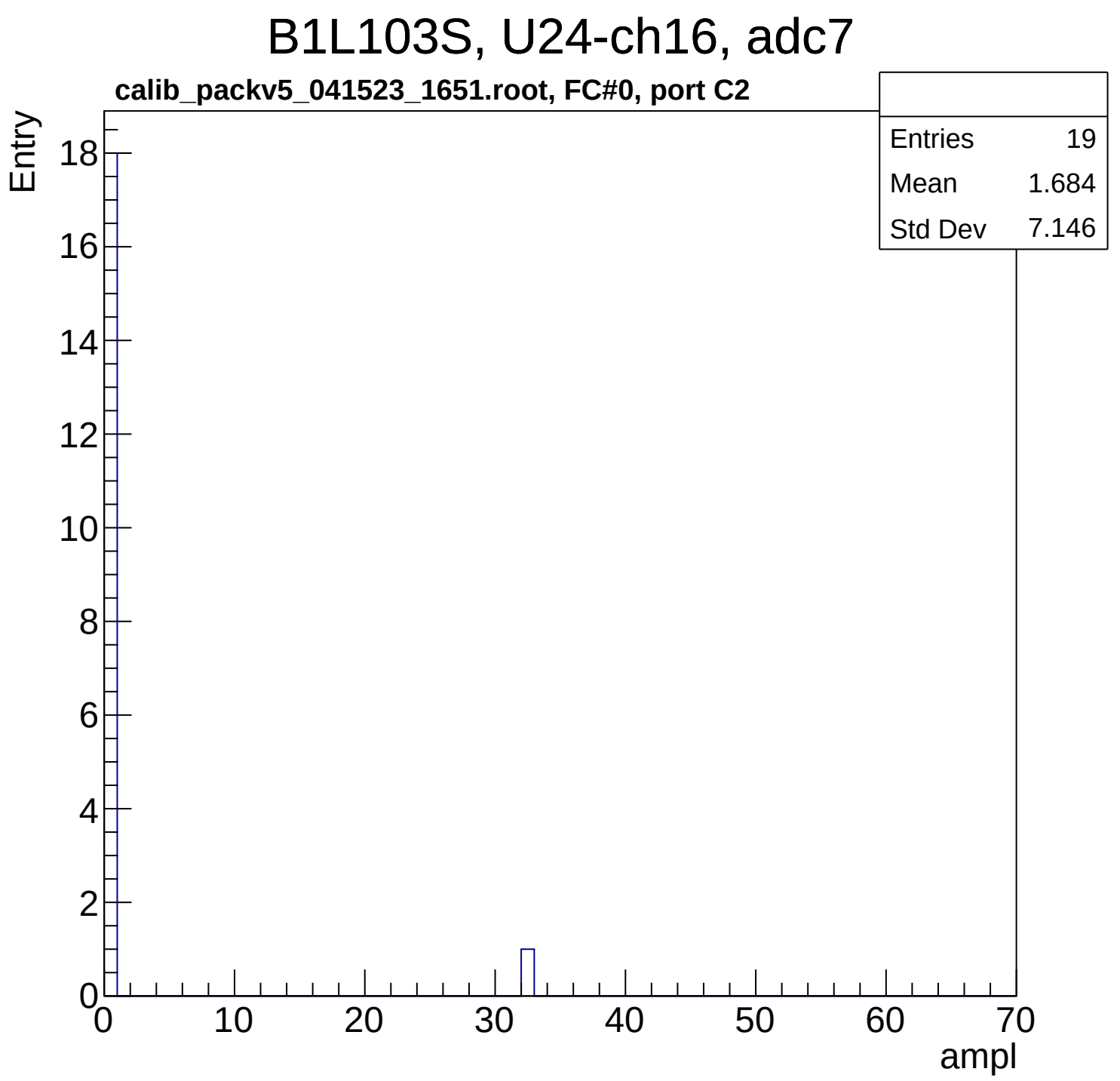
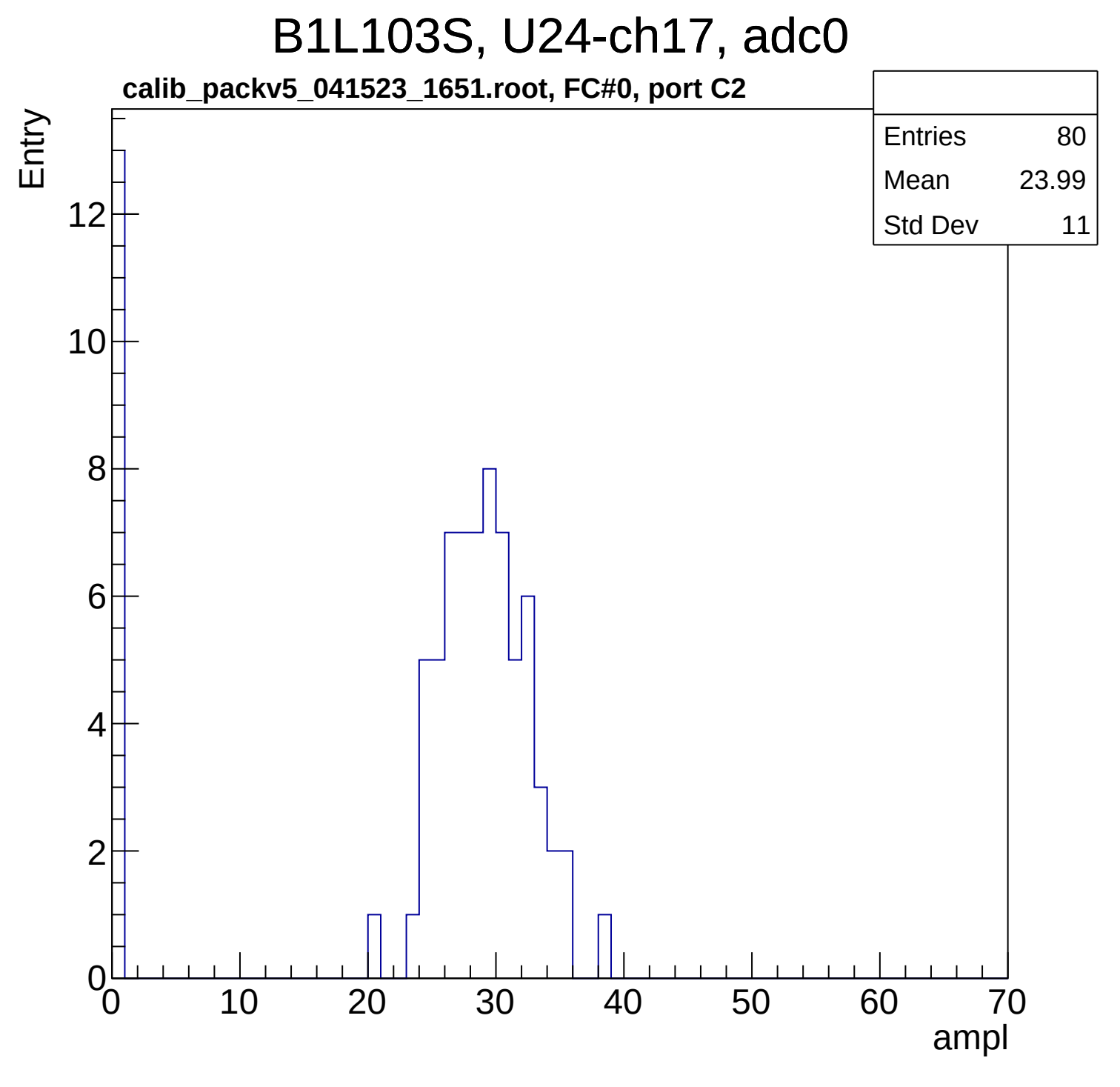
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

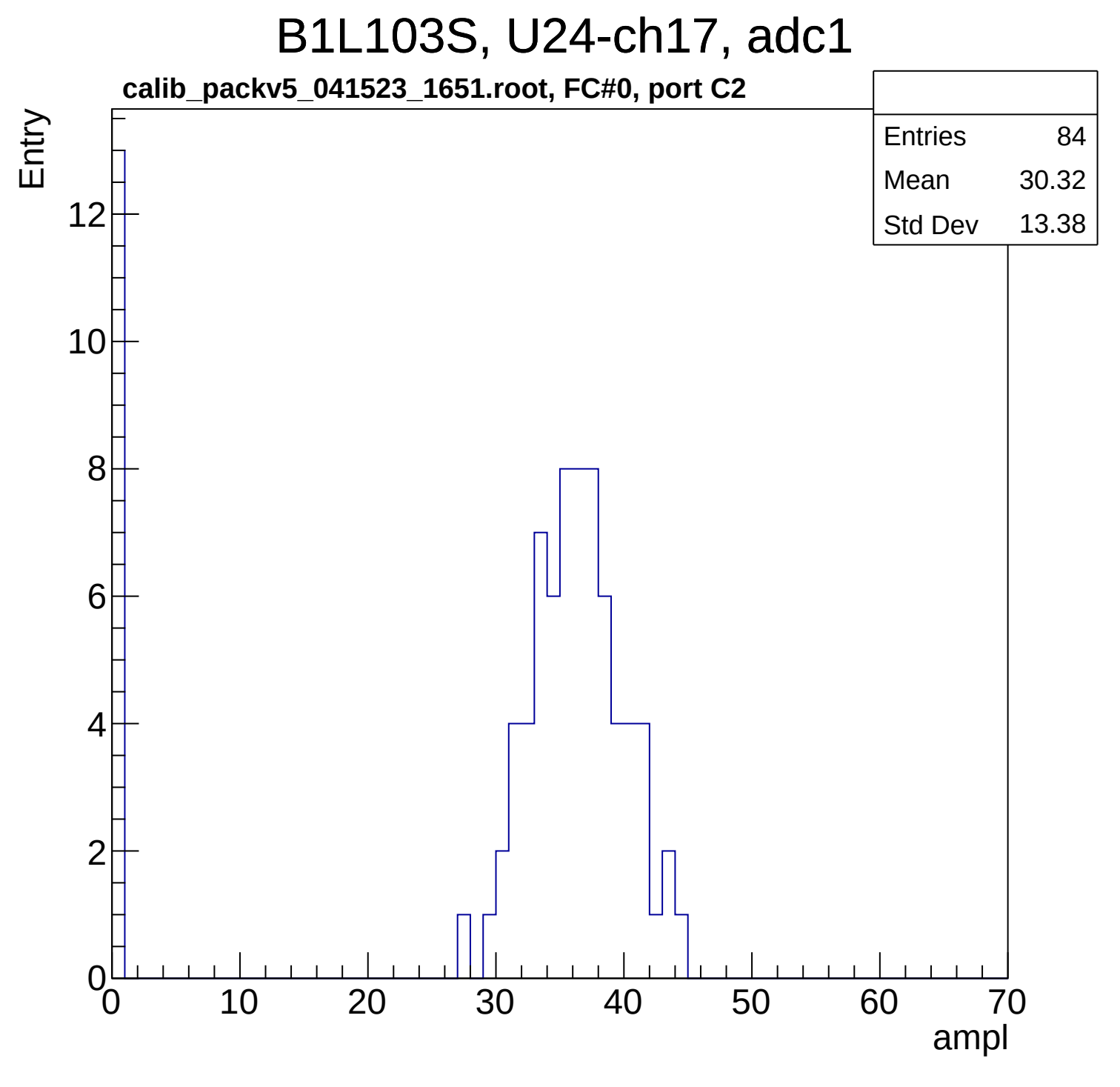

B1L103S, U24-ch16, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 54.71
Std Dev 4.294
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

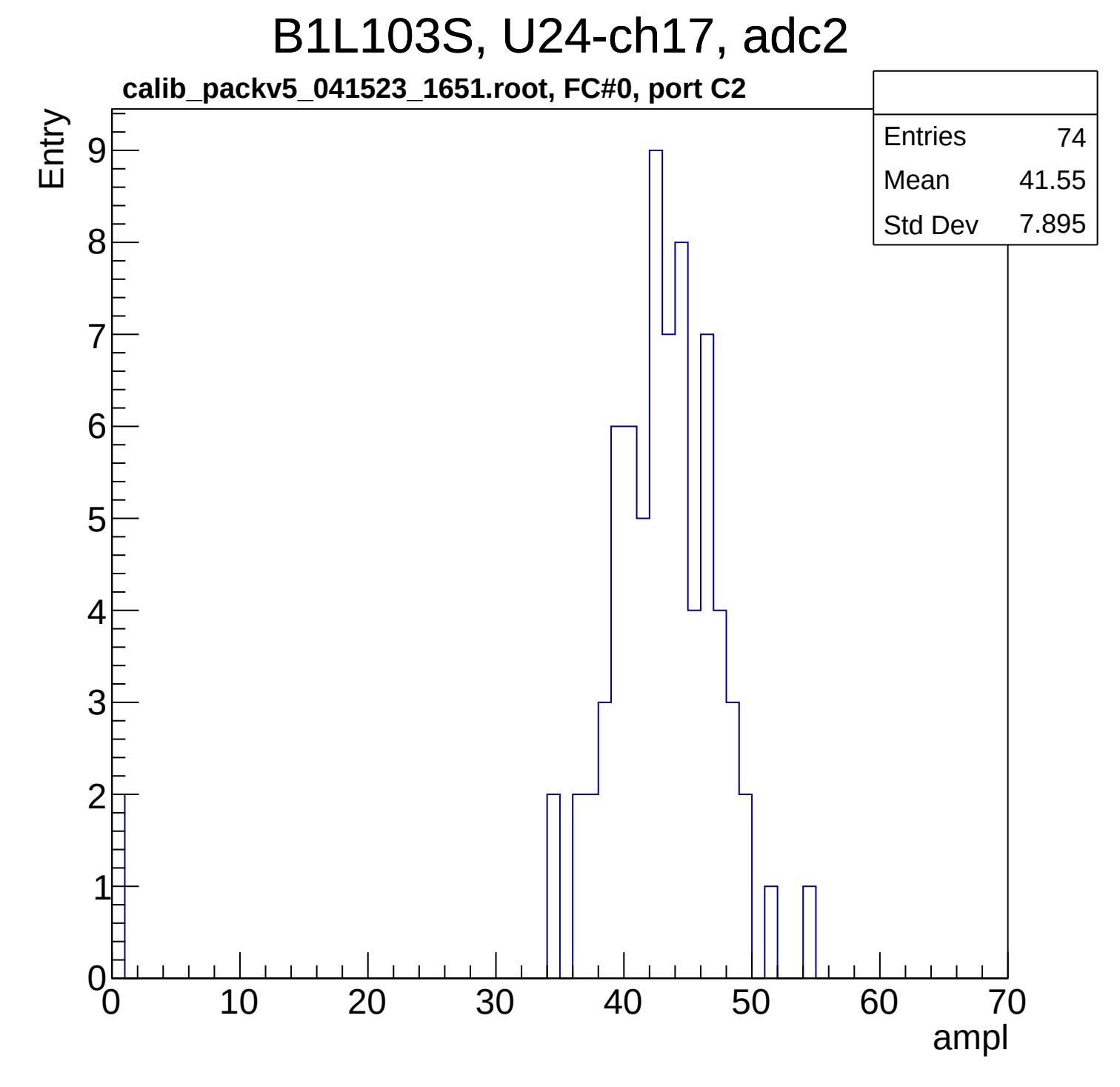

B1L103S, U24-ch16, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 60.17
Std Dev 1.929
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

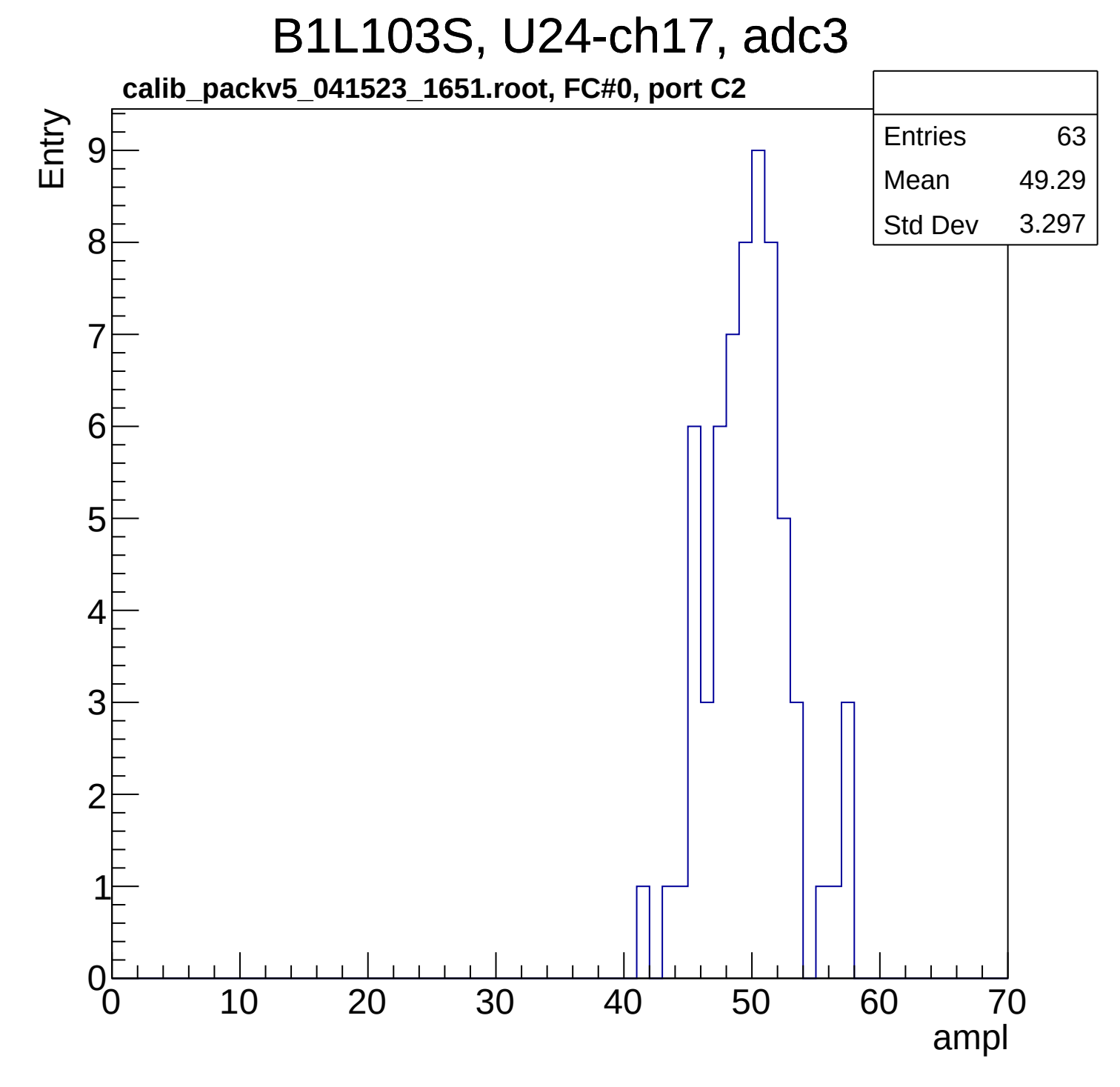

B1L103S, U24-ch16, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 52
Std Dev 23.27
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U24-ch16, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.684
Std Dev 7.146
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch17, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 23.99
Std Dev 11
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch17, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 30.32
Std Dev 13.38
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch17, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 41.55
Std Dev 7.895
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U24-ch17, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 49.29
Std Dev 3.297
Entry
ampl
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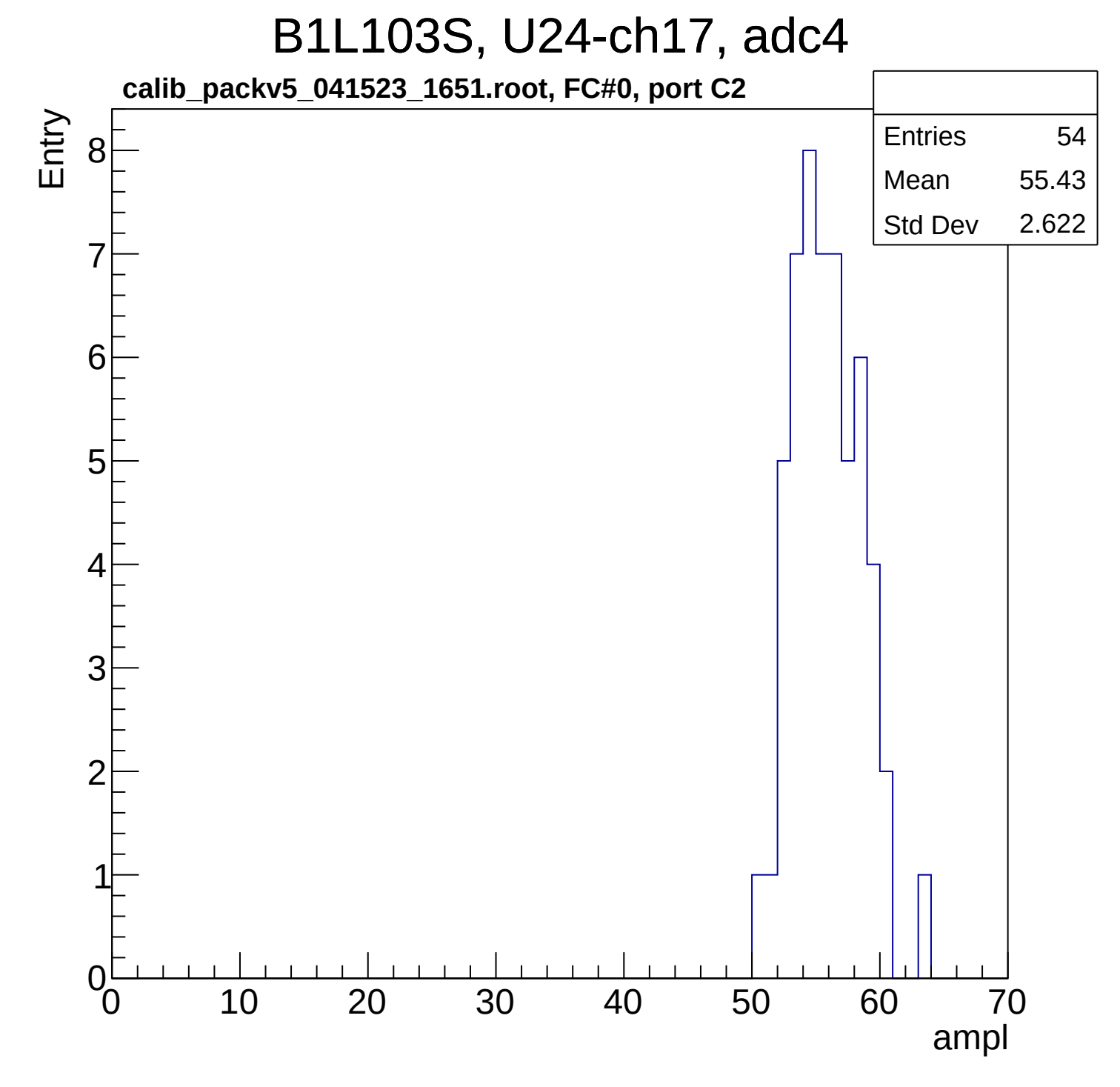
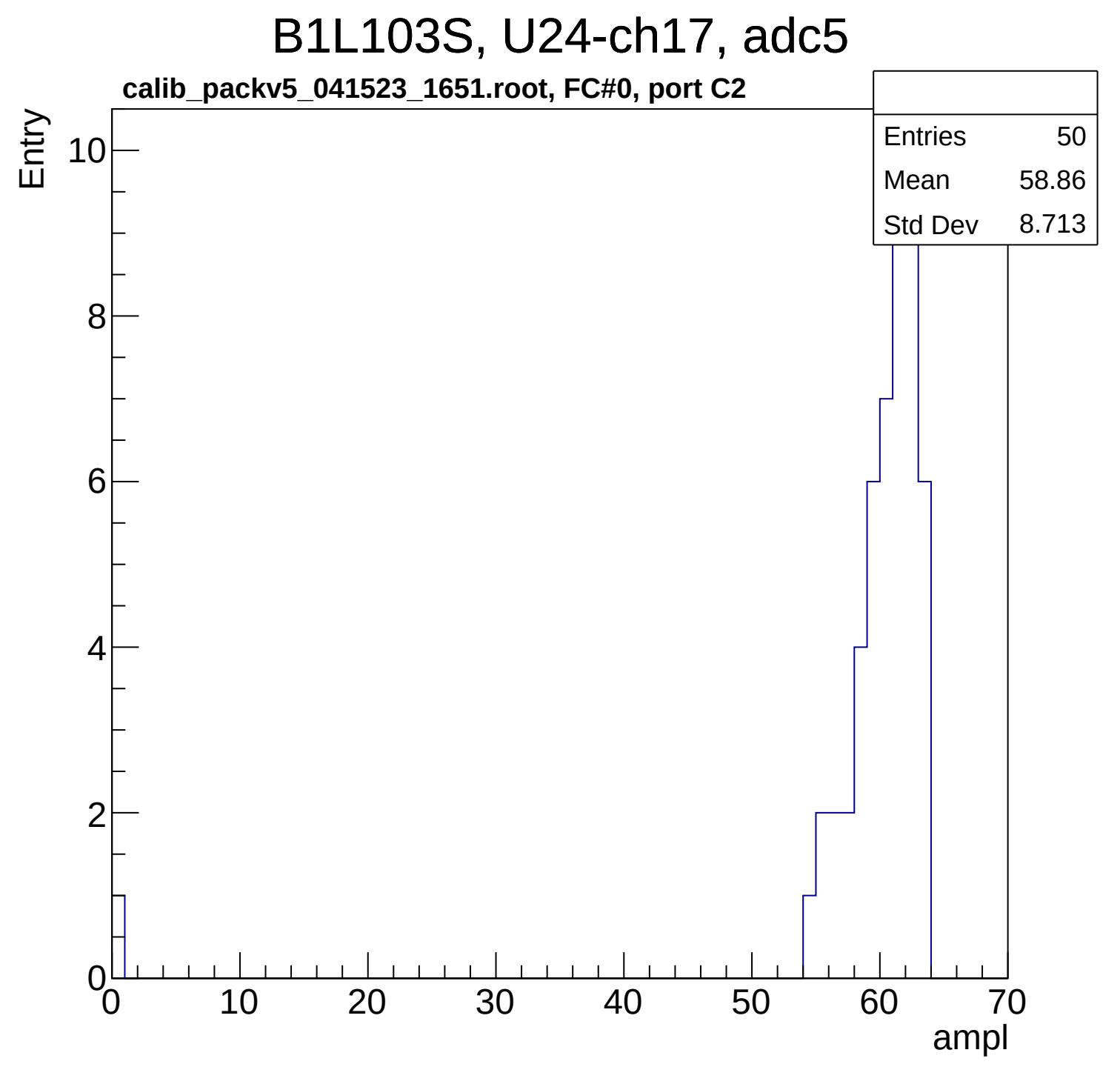
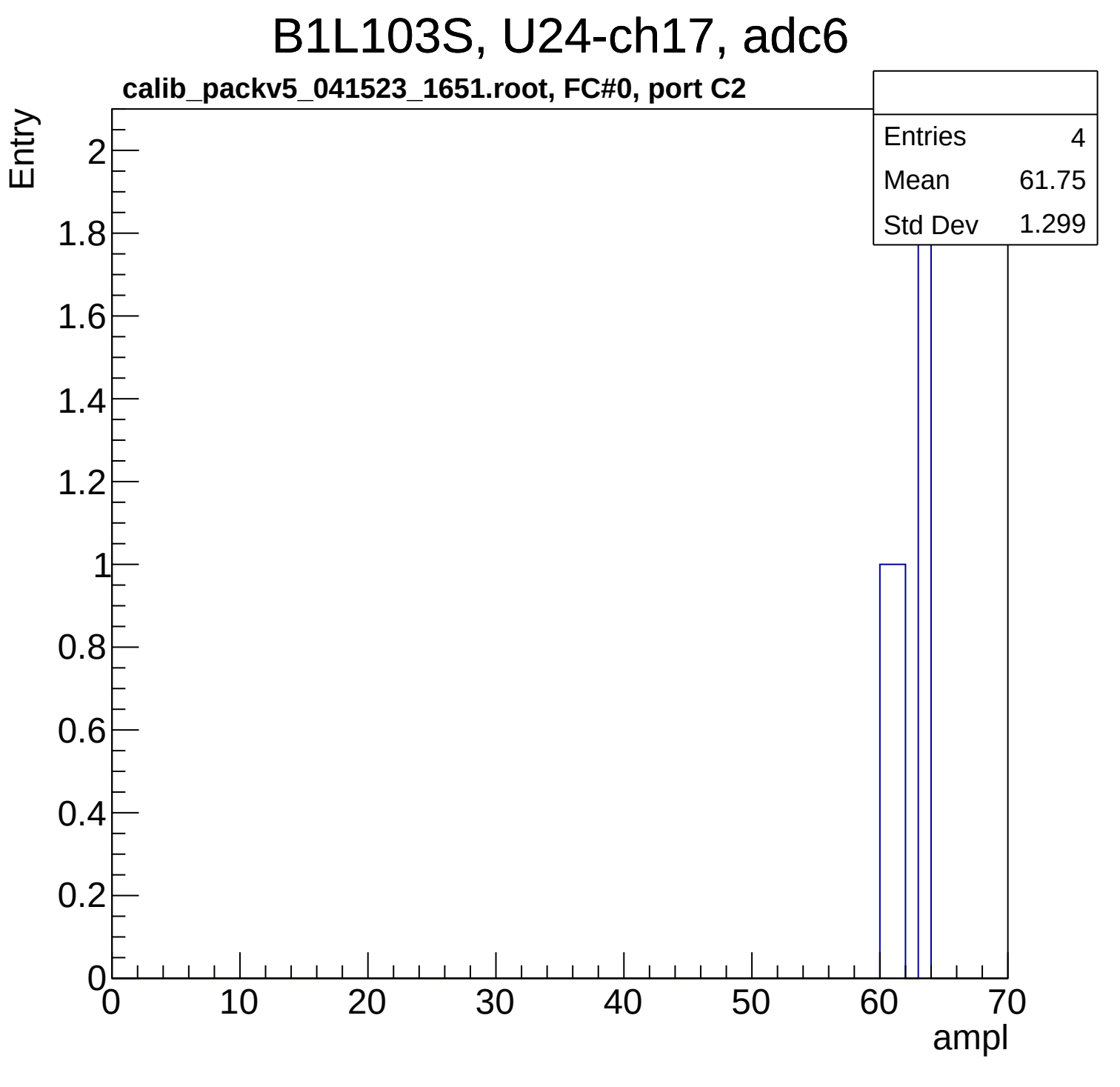
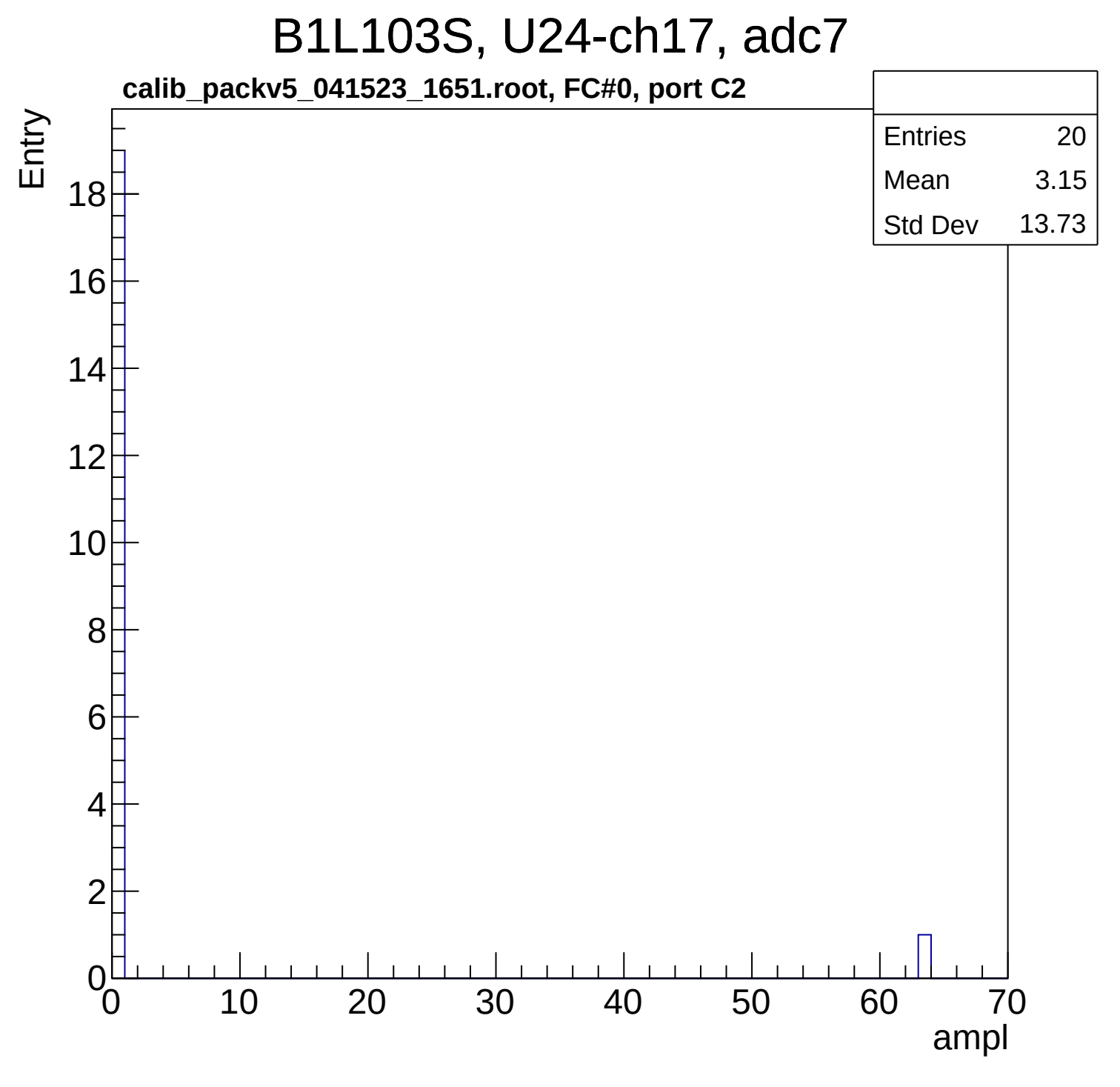
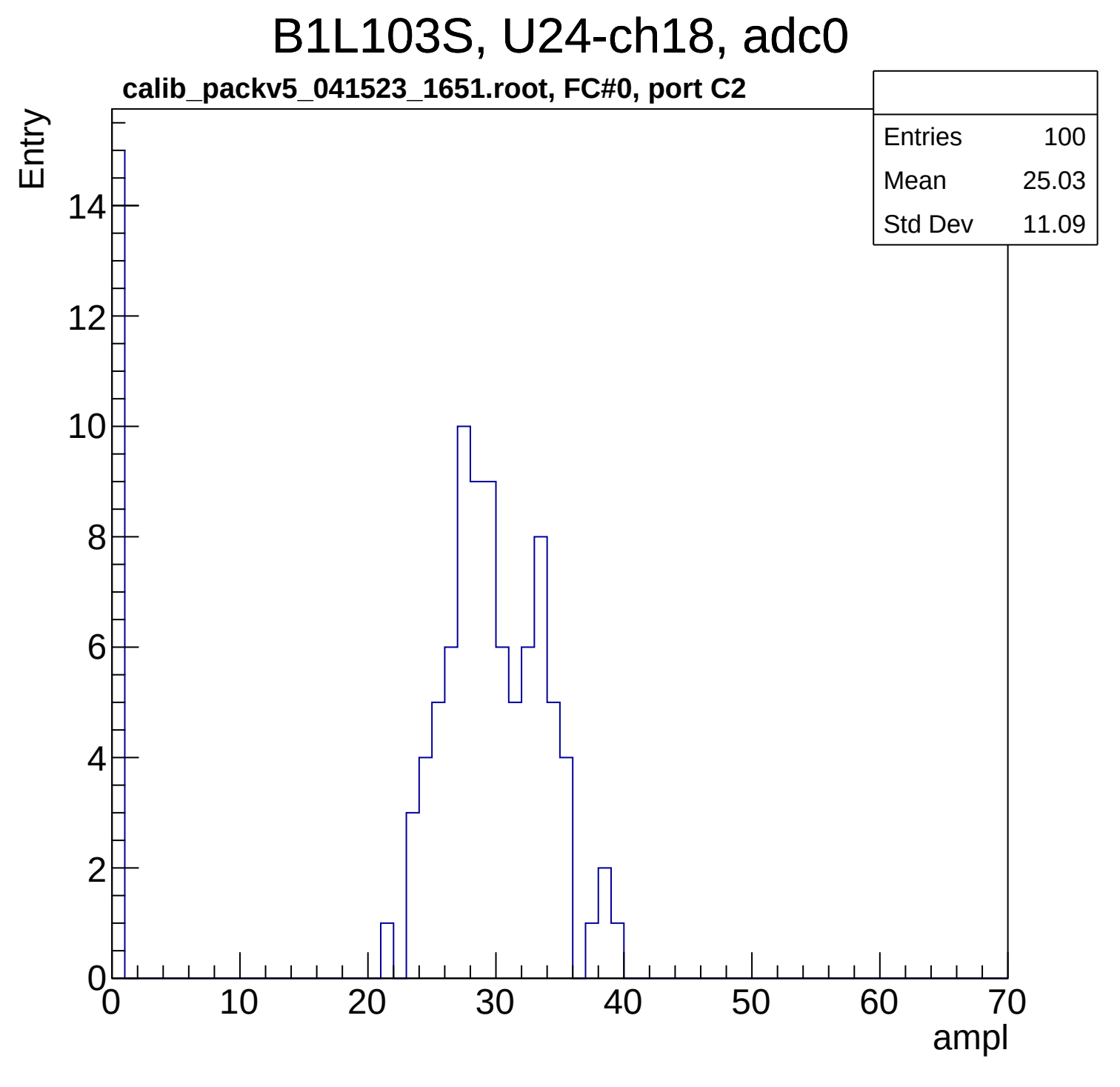
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U24-ch17, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 55.43
Std Dev 2.622
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U24-ch17, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 58.86
Std Dev 8.713
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch17, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 4
Mean 61.75
Std Dev 1.299
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U24-ch17, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch18, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 100
Mean 25.03
Std Dev 11.09
Entry
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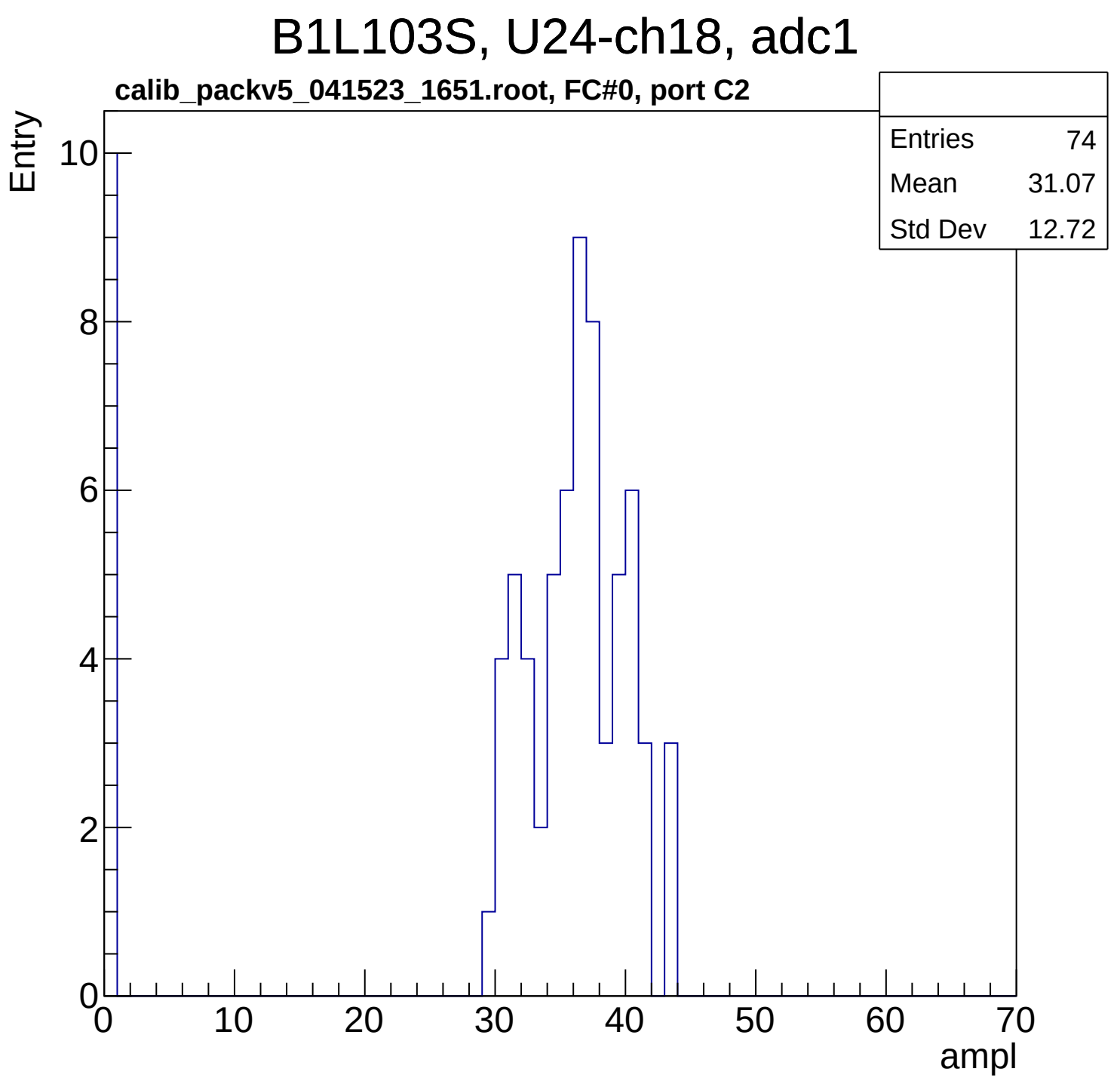
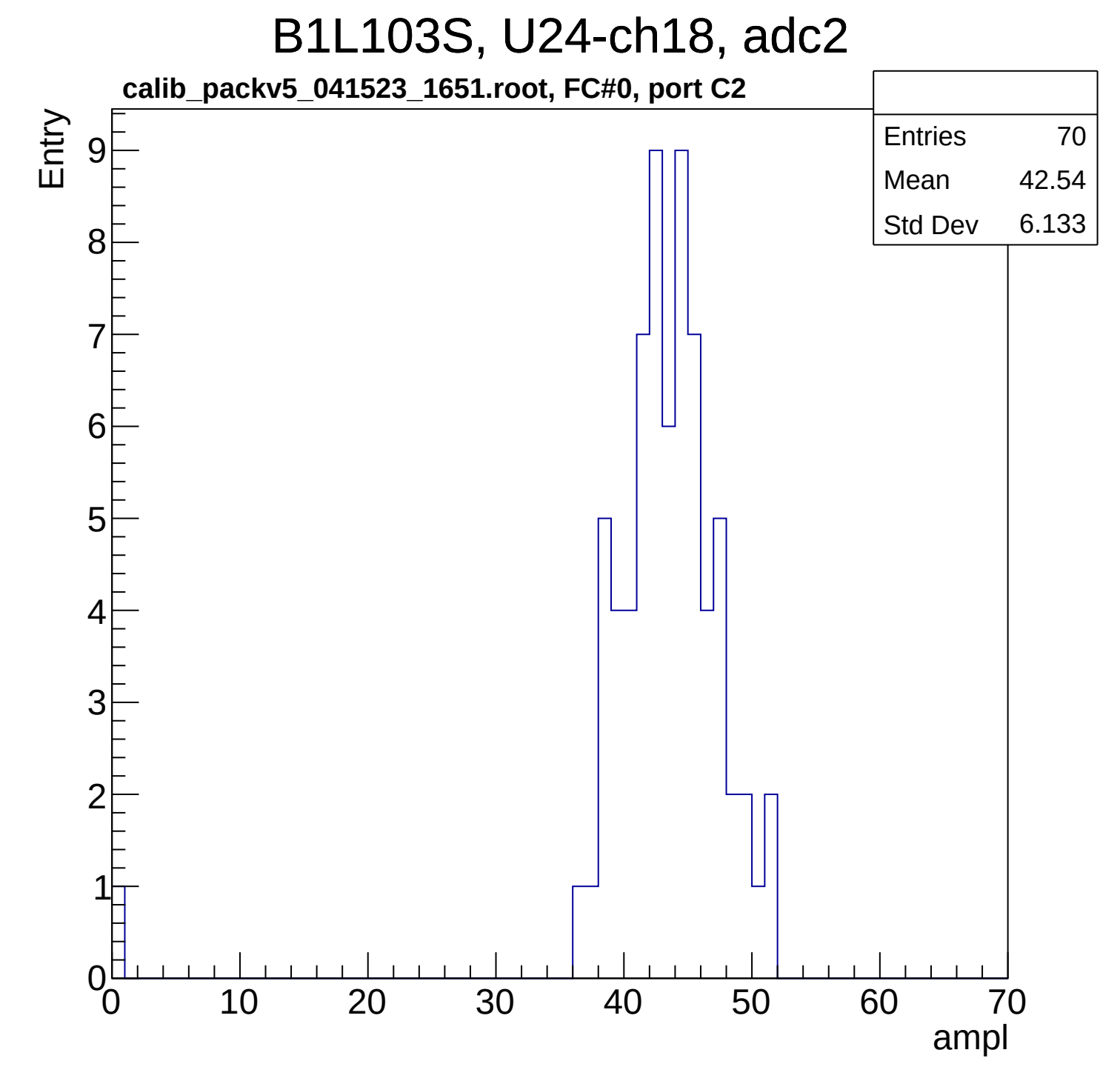
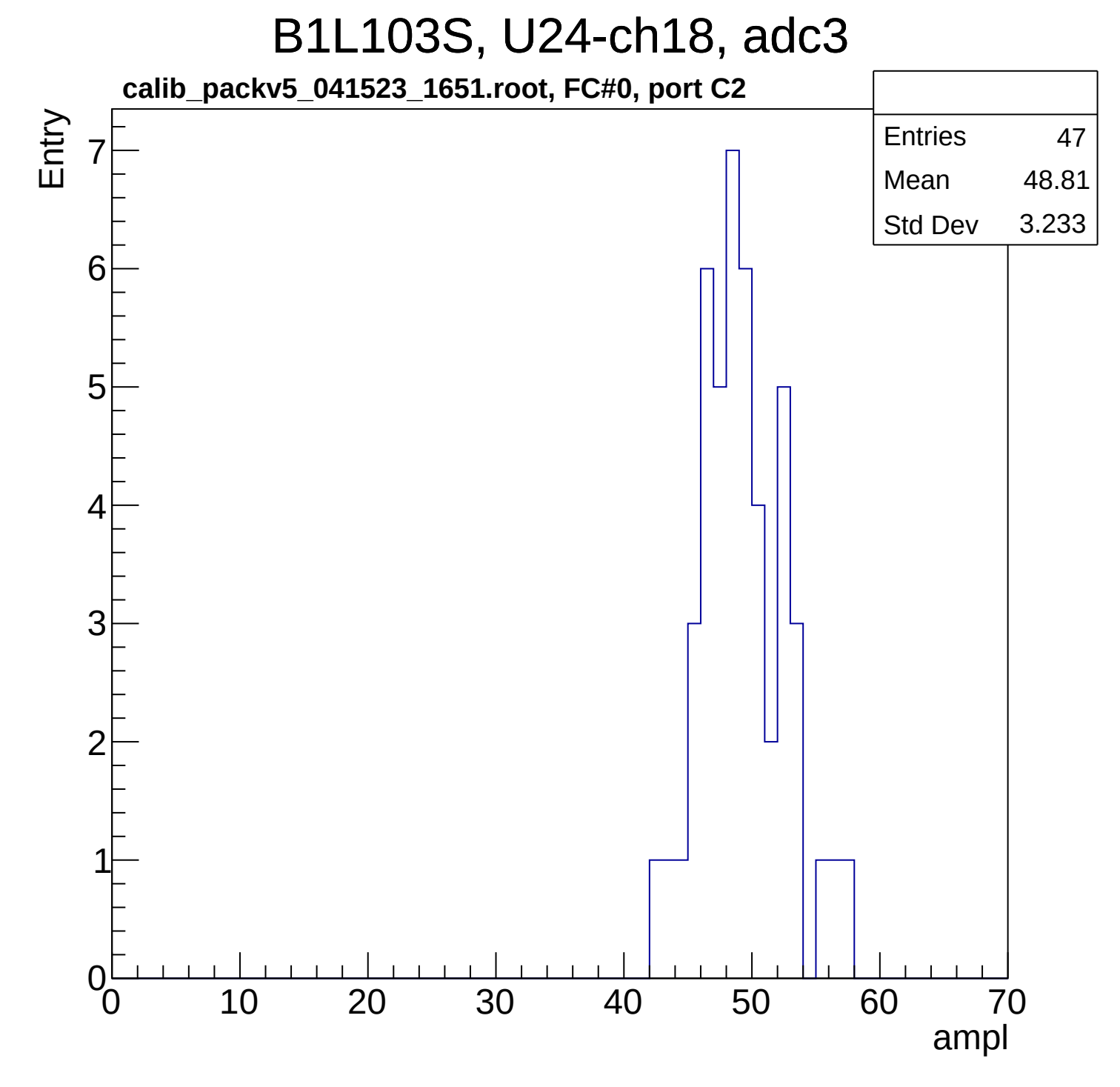
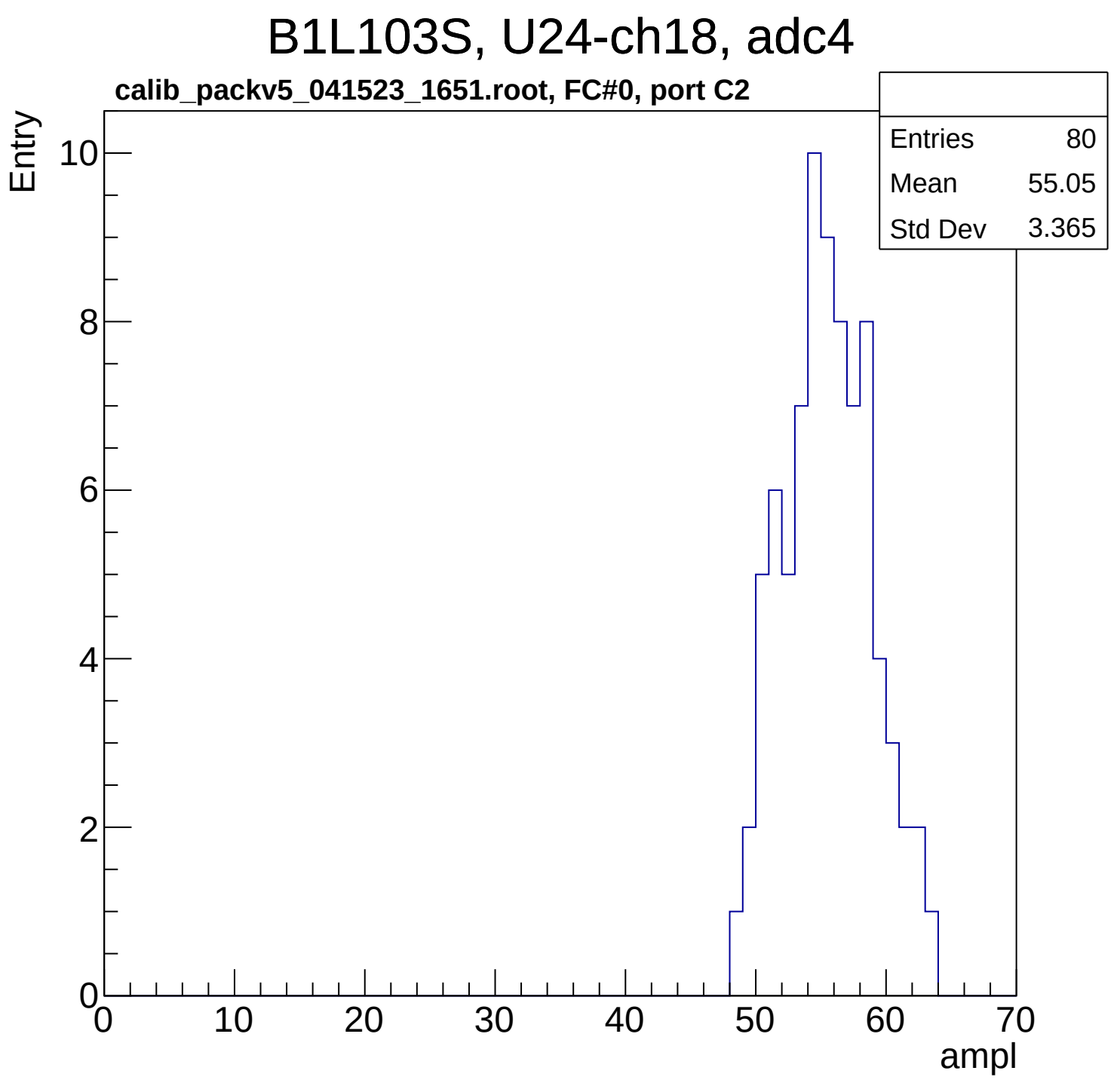
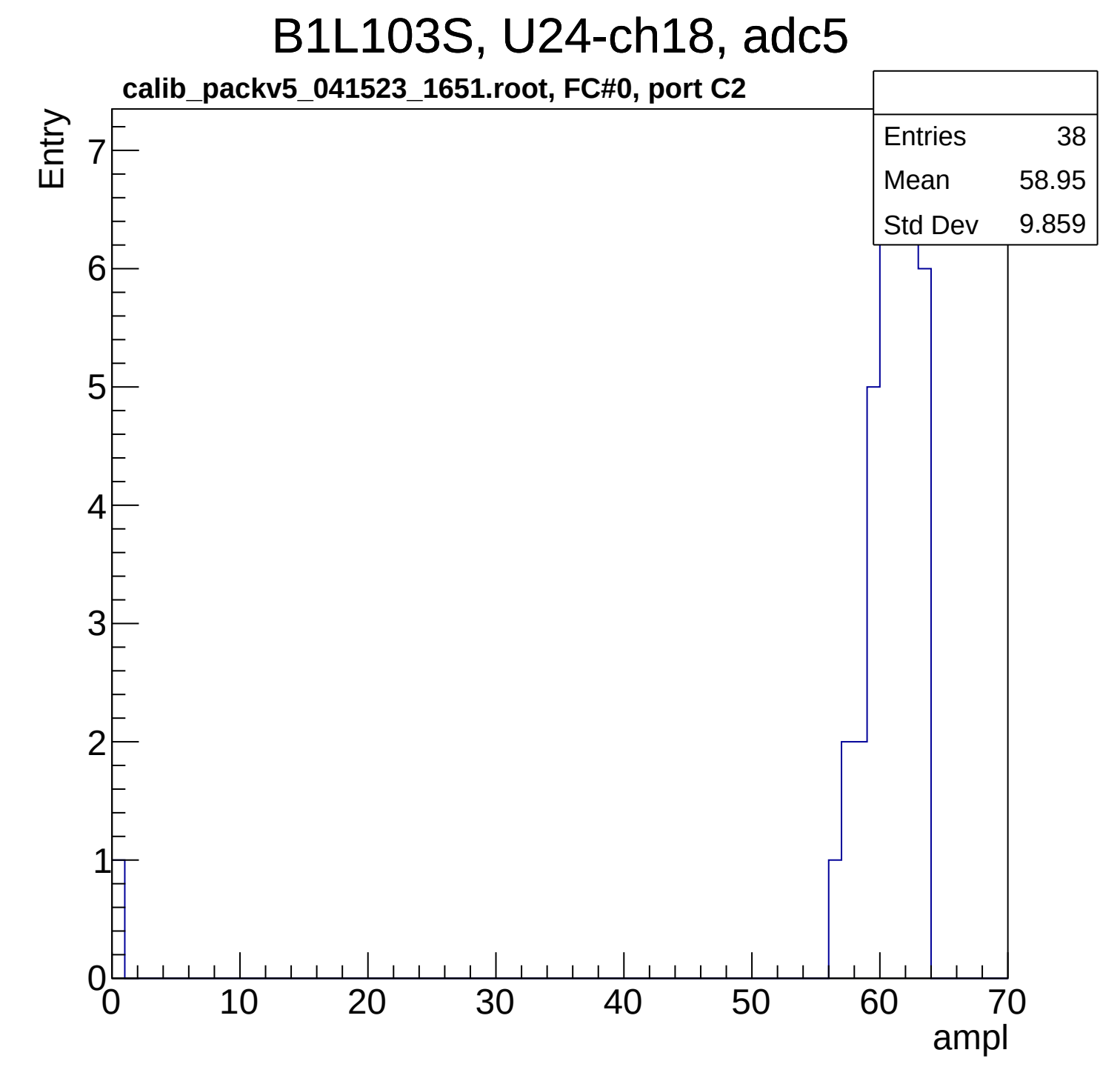
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch18, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 31.07
Std Dev 12.72
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch18, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 42.54
Std Dev 6.133
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U24-ch18, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 48.81
Std Dev 3.233
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U24-ch18, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 55.05
Std Dev 3.365
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch18, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 38
Mean 58.95
Std Dev 9.859
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
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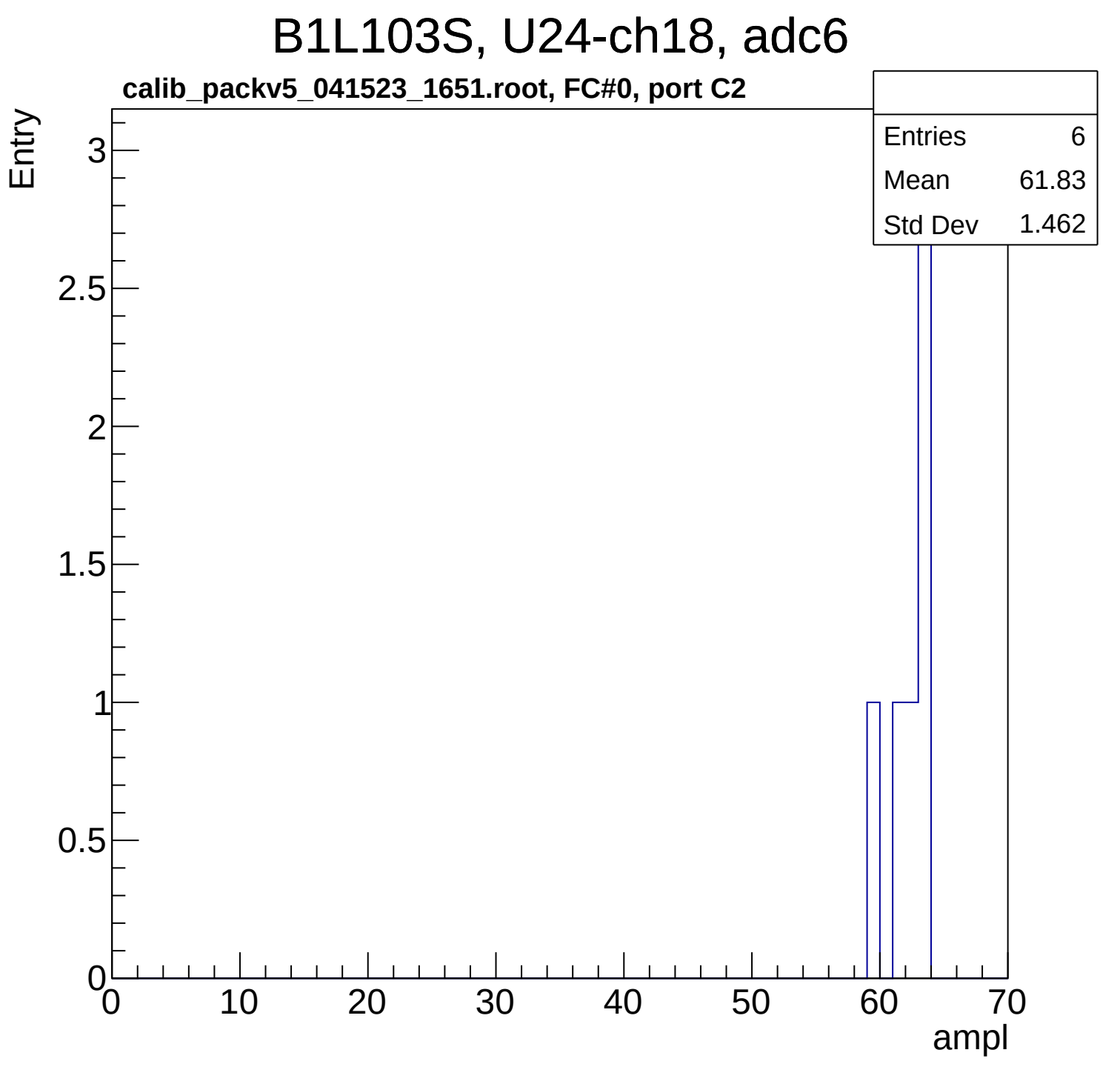
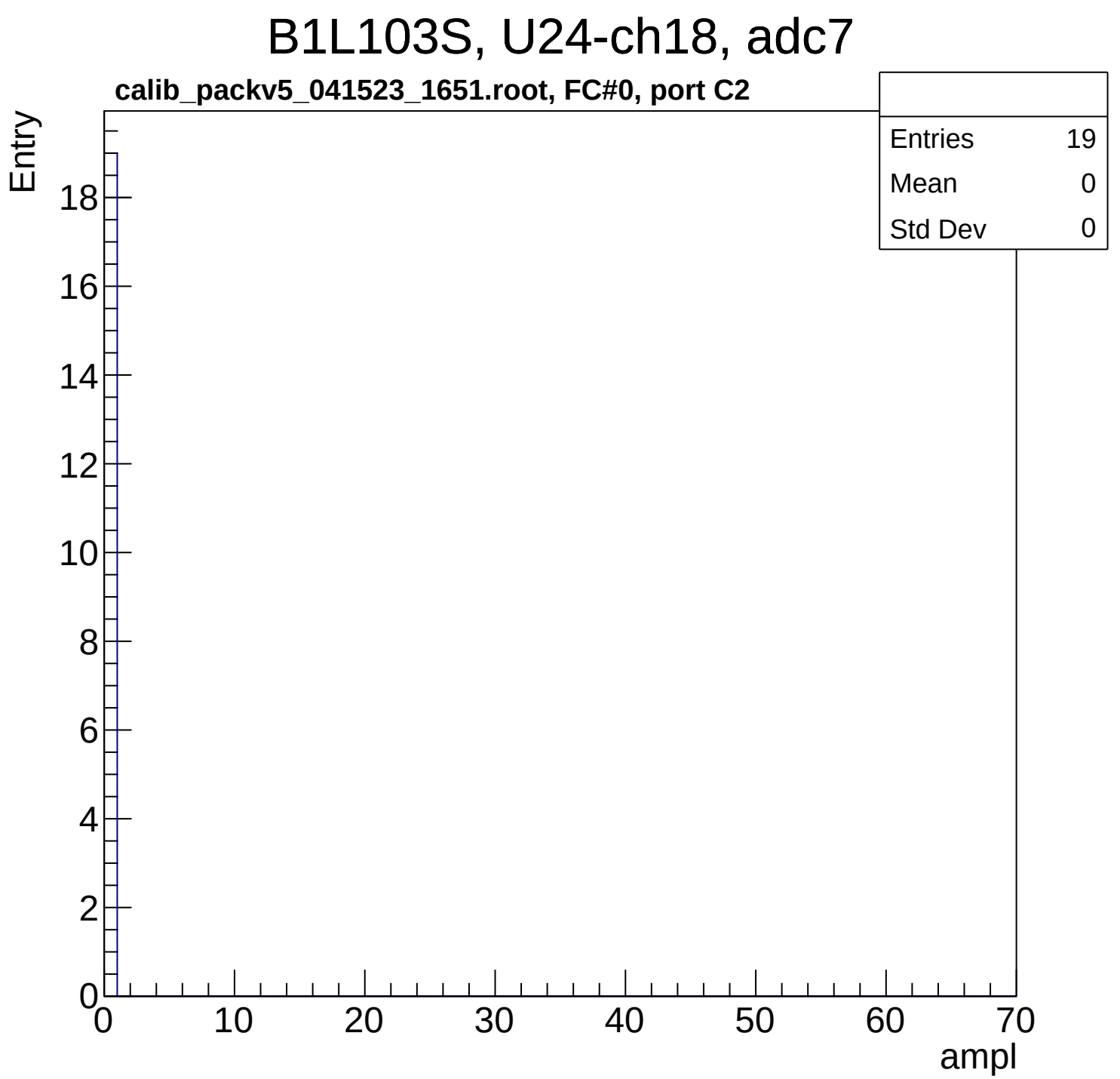
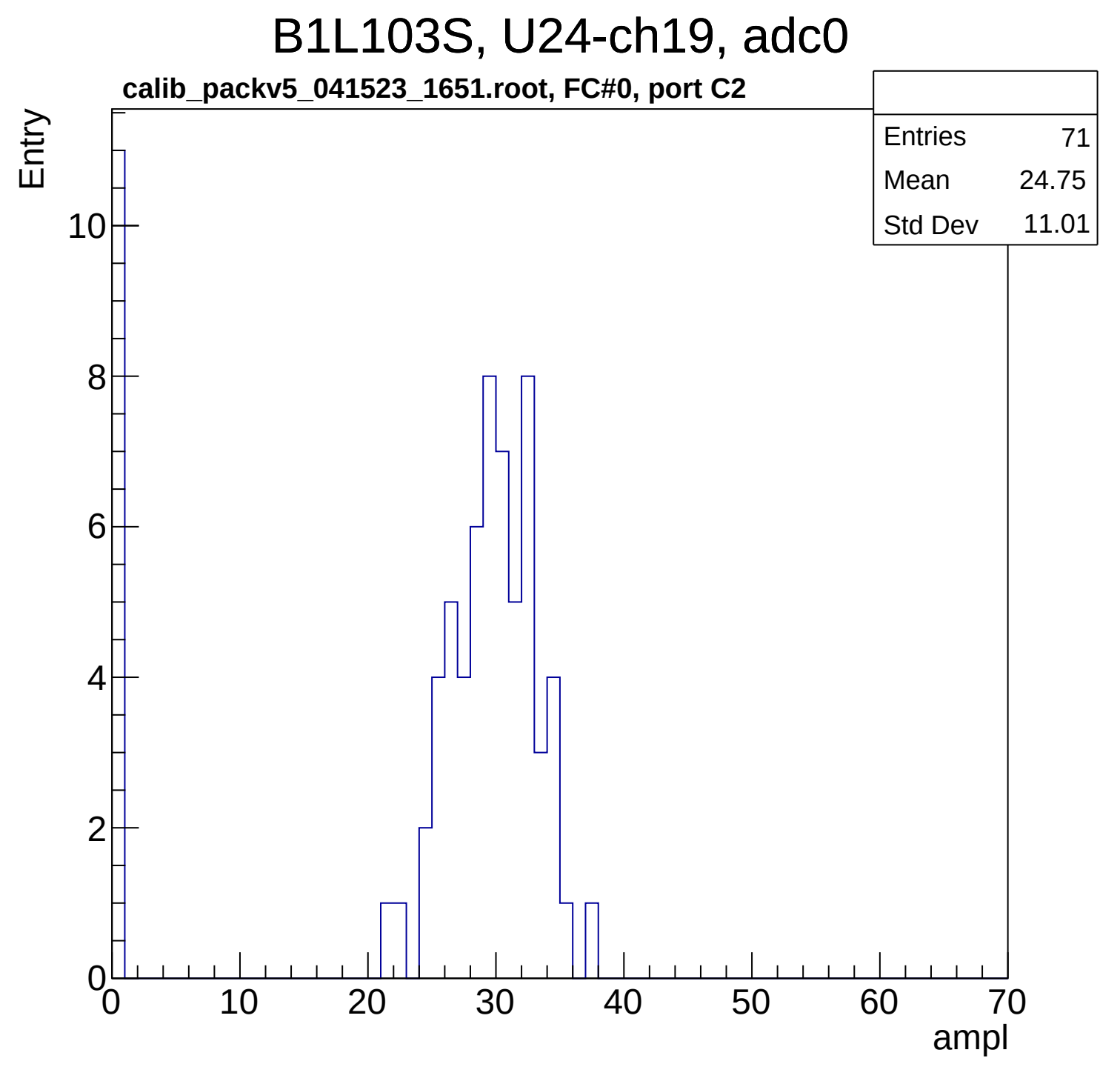
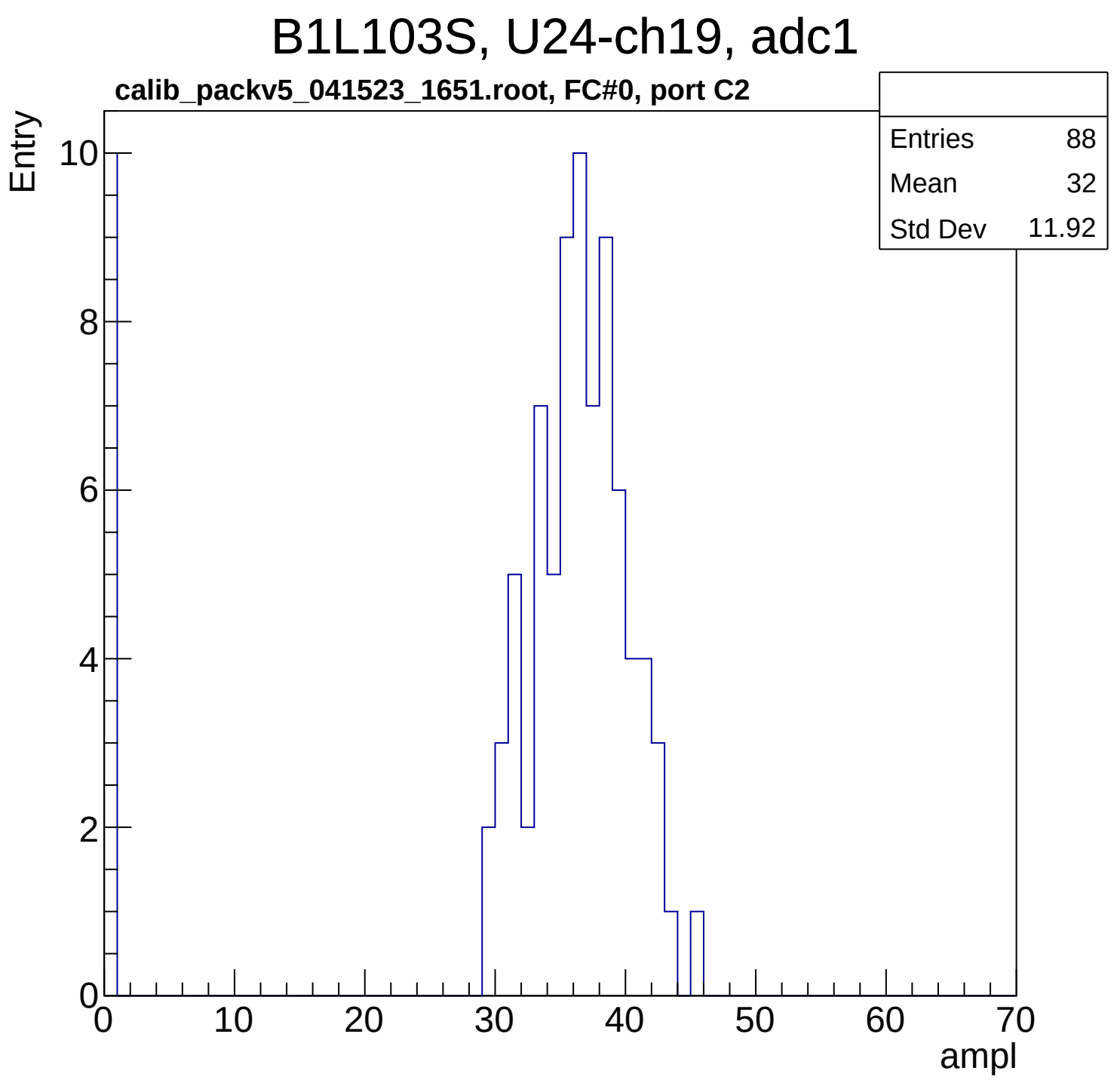
40
50
60
70


B1L103S, U24-ch18, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 61.83
Std Dev 1.462
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U24-ch18, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch19, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 24.75
Std Dev 11.01
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch19, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 88
Mean 32
Std Dev 11.92
Entry
ampl
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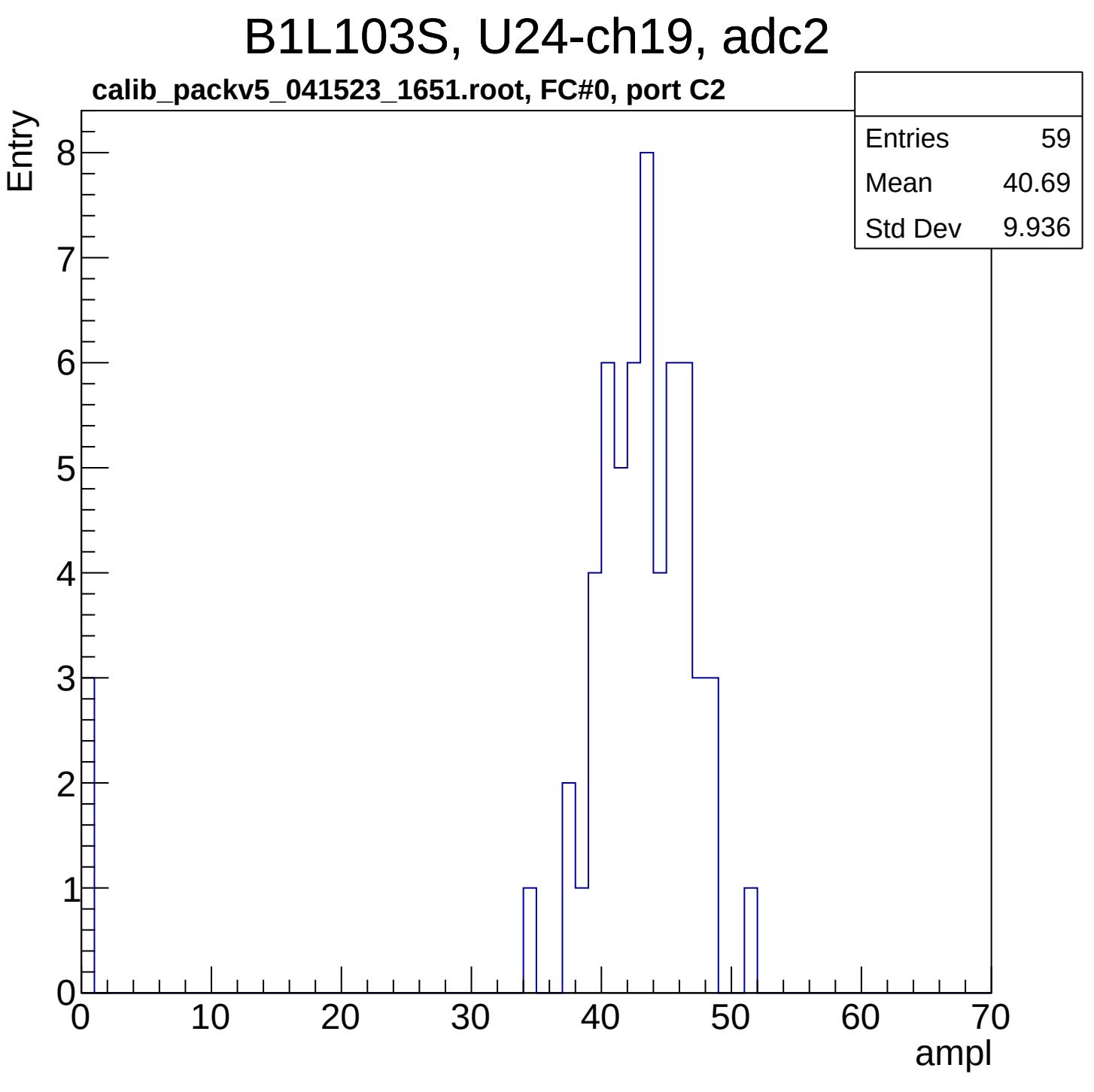
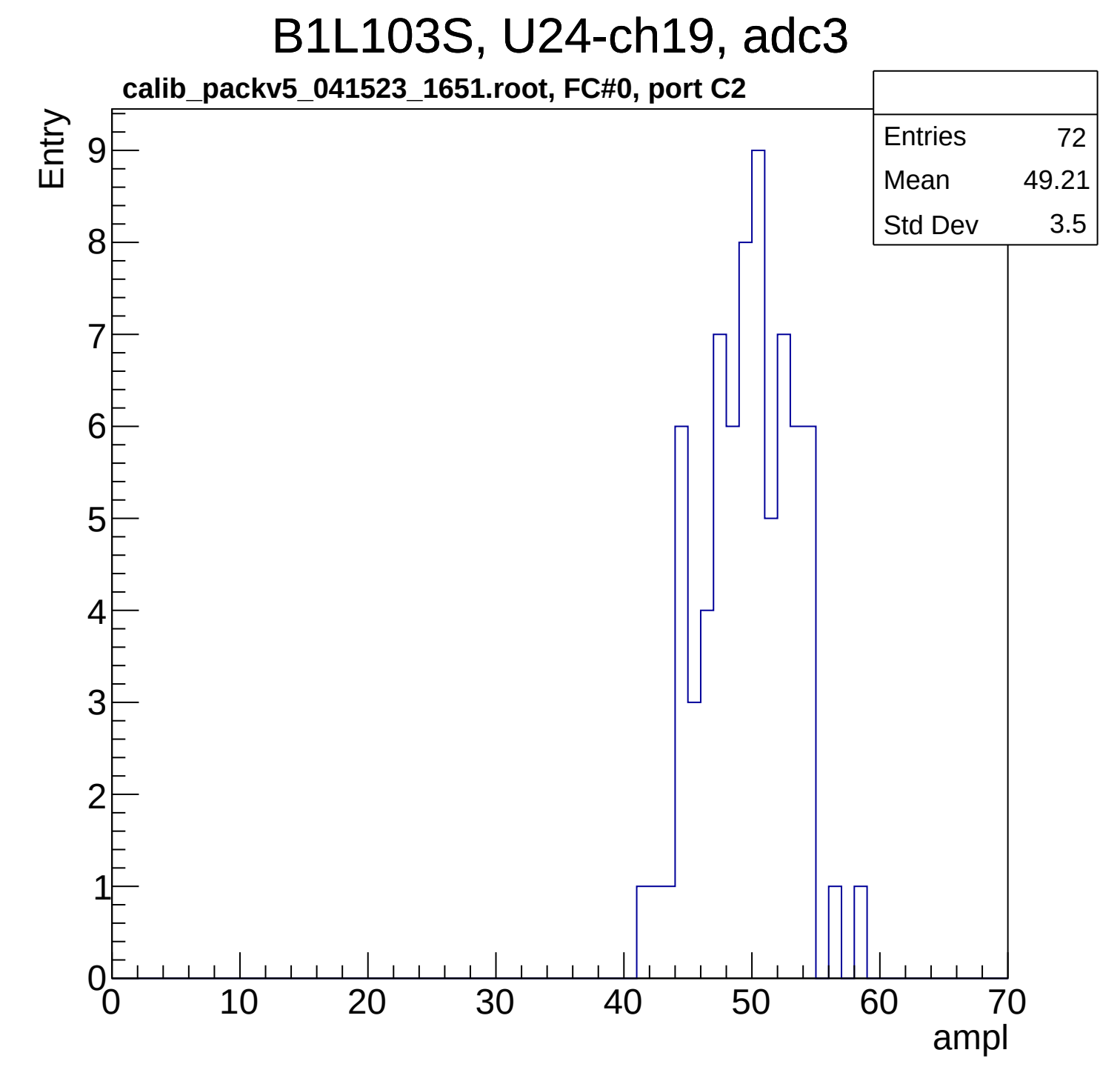
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U24-ch19, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 40.69
Std Dev 9.936
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U24-ch19, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 49.21
Std Dev 3.5
Entry
ampl
0
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2
3
4
5
6
7
8
9
0
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20
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40
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60
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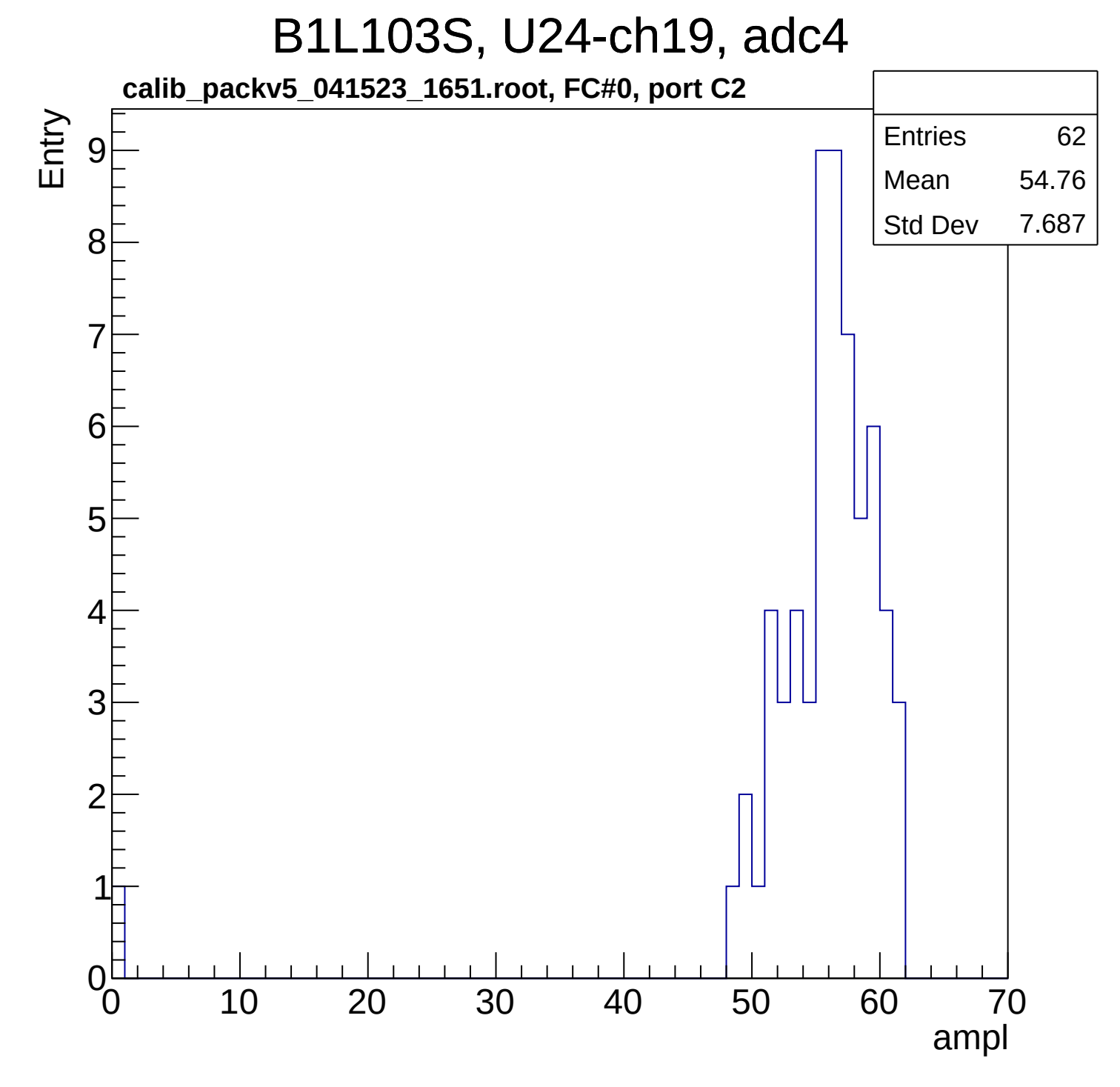
B1L103S, U24-ch19, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 54.76
Std Dev 7.687
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
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40
50
60
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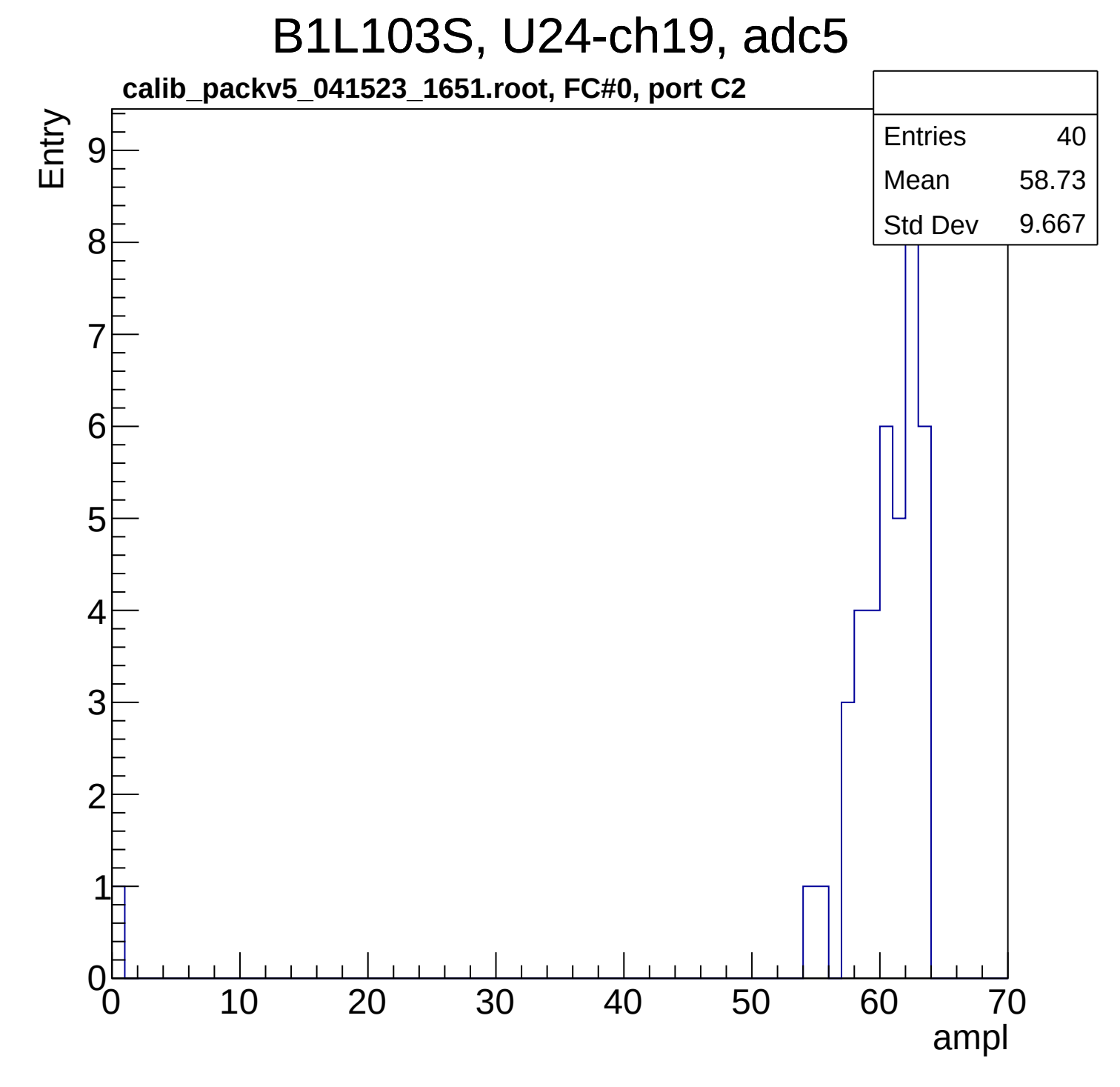
B1L103S, U24-ch19, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 40
Mean 58.73
Std Dev 9.667
Entry
ampl
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2
3
4
5
6
7
8
9
0
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40
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60
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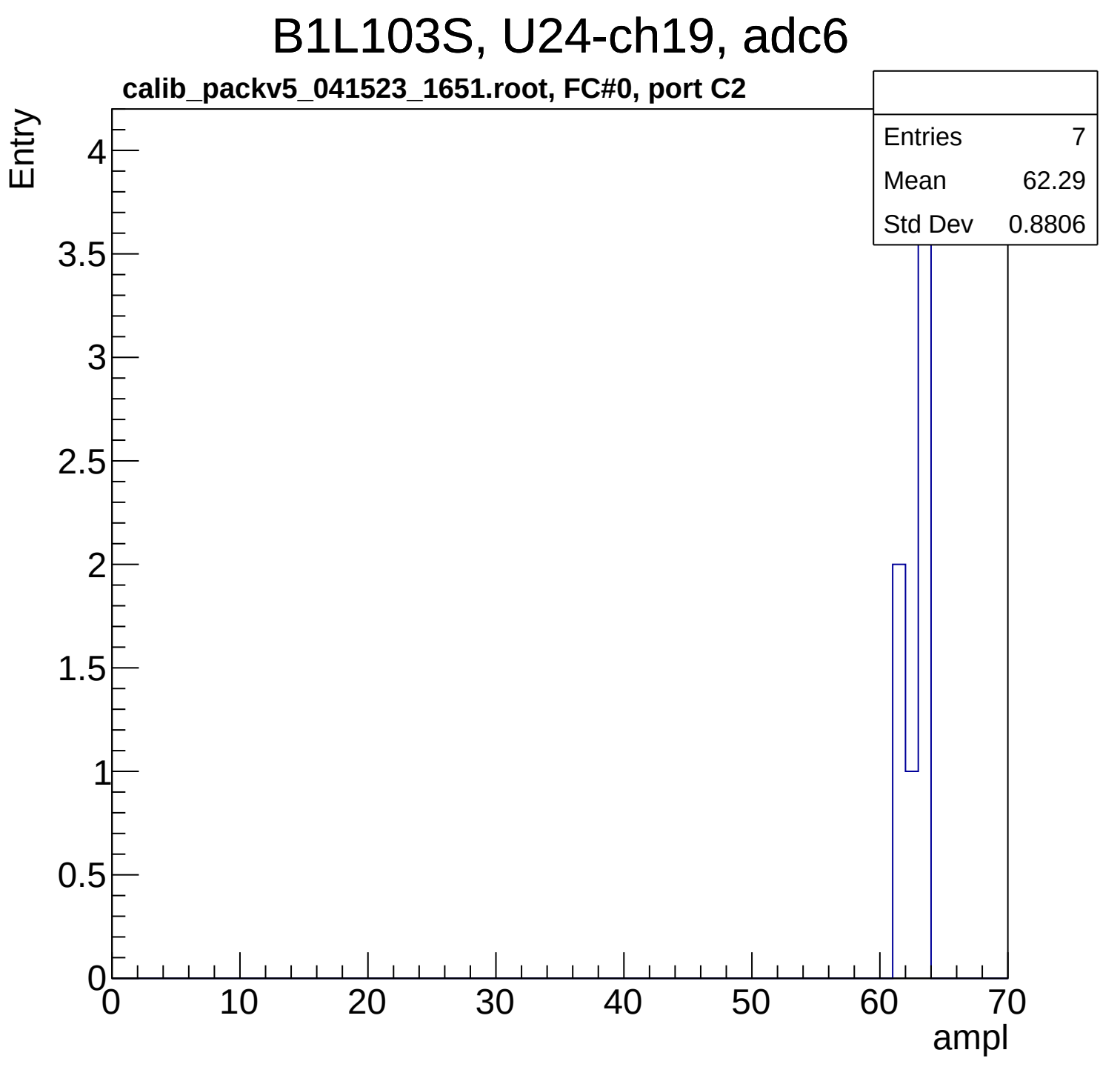
B1L103S, U24-ch19, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 62.29
Std Dev 0.8806
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
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40
50
60
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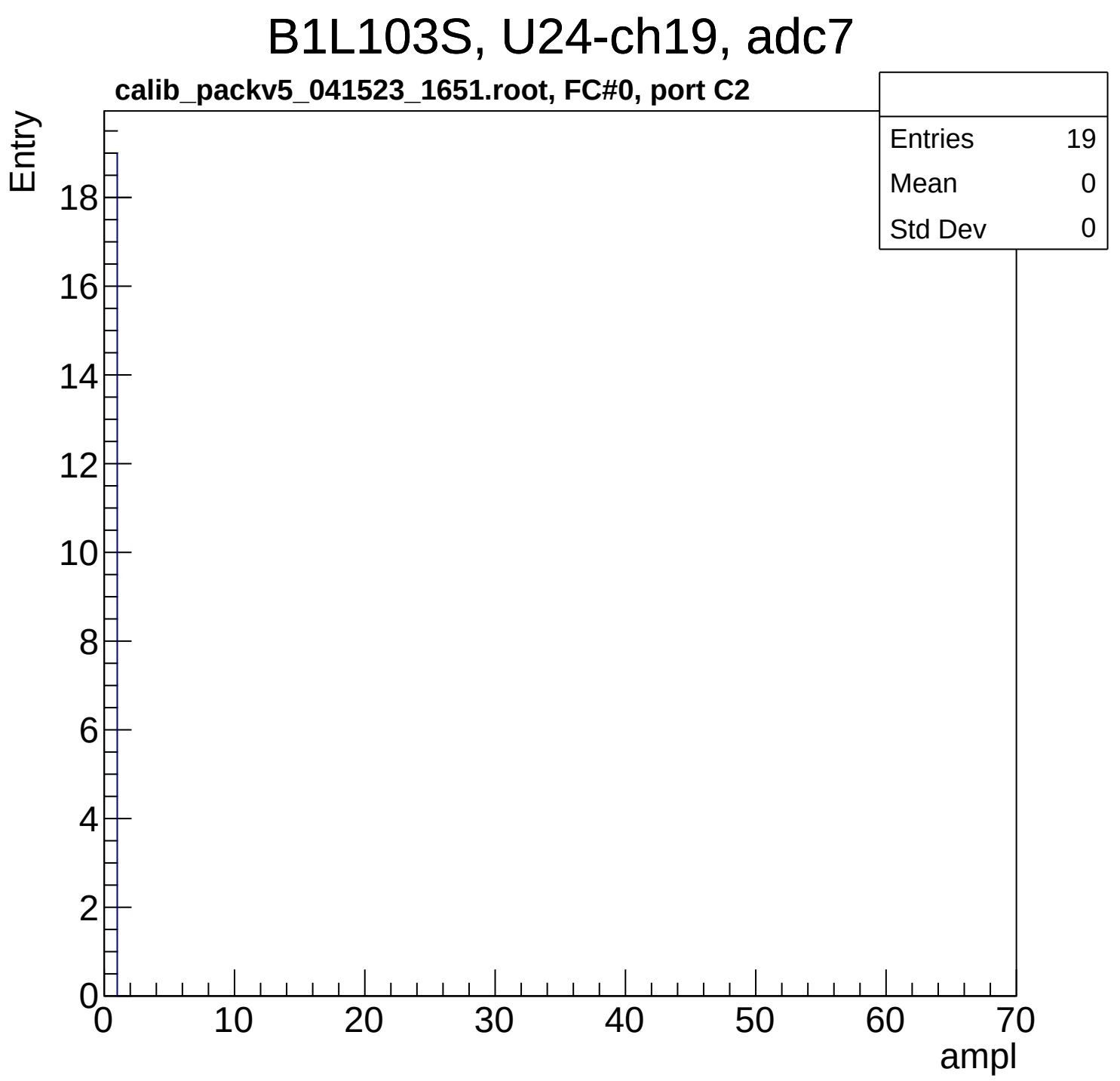
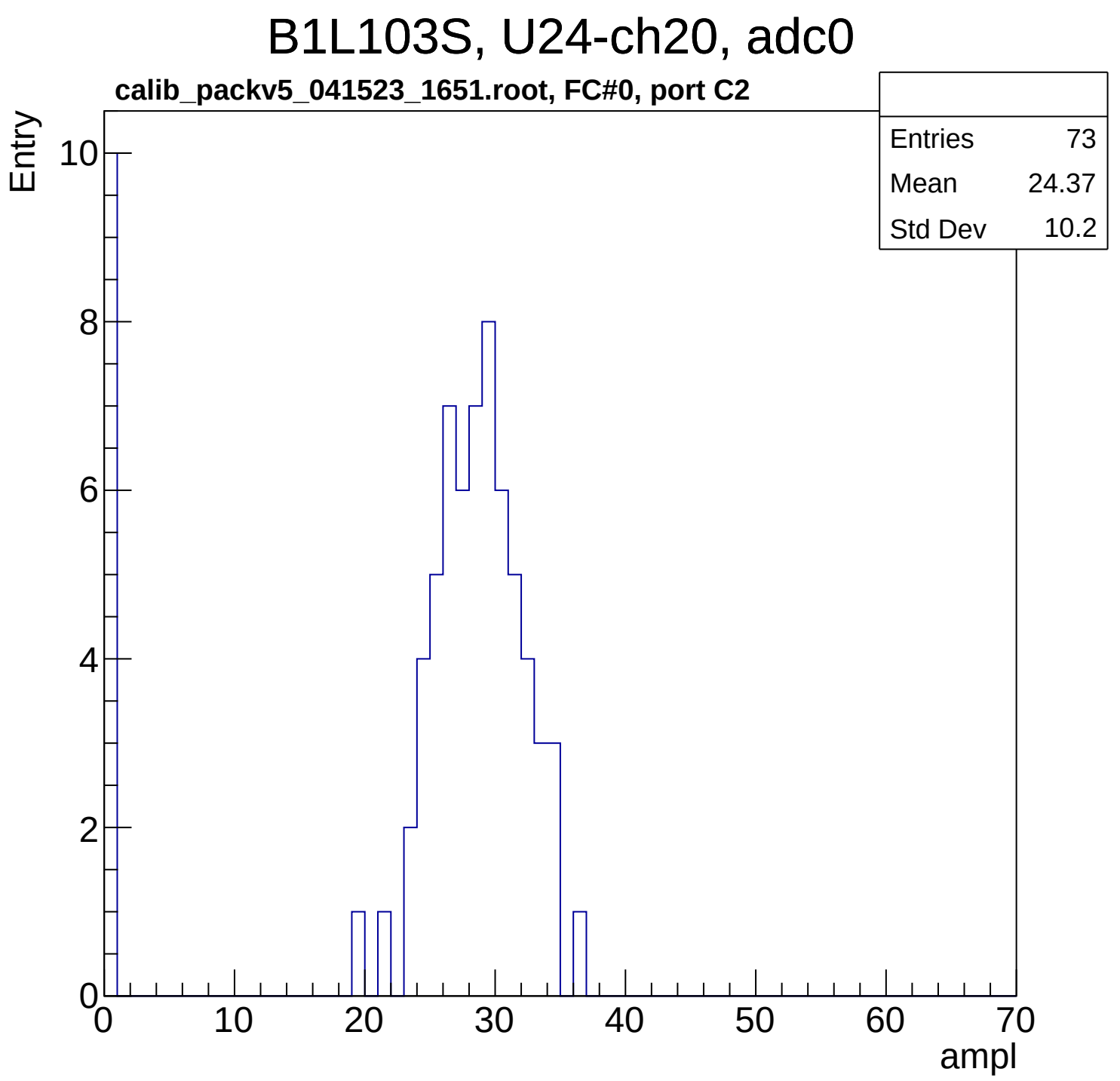
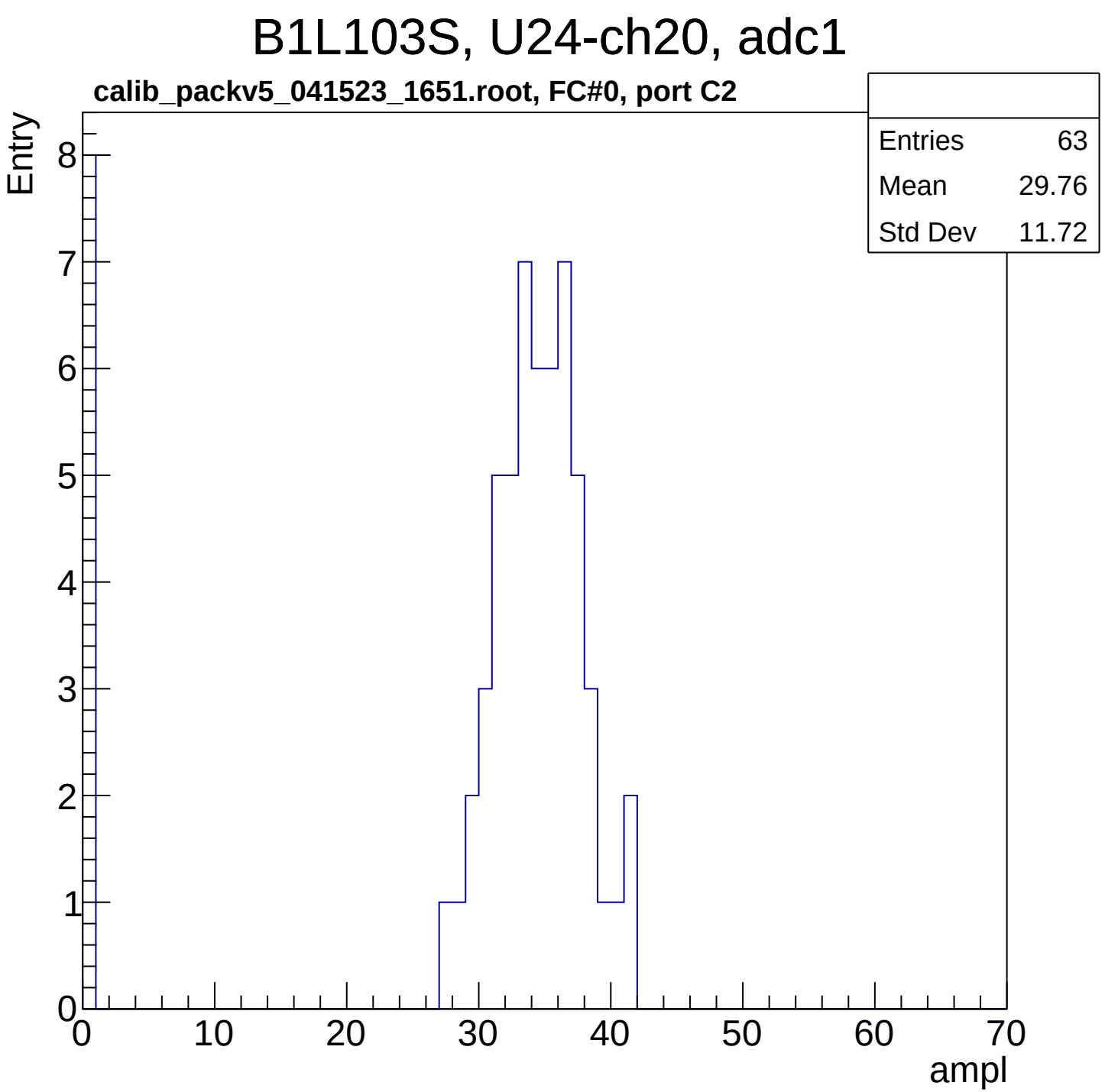
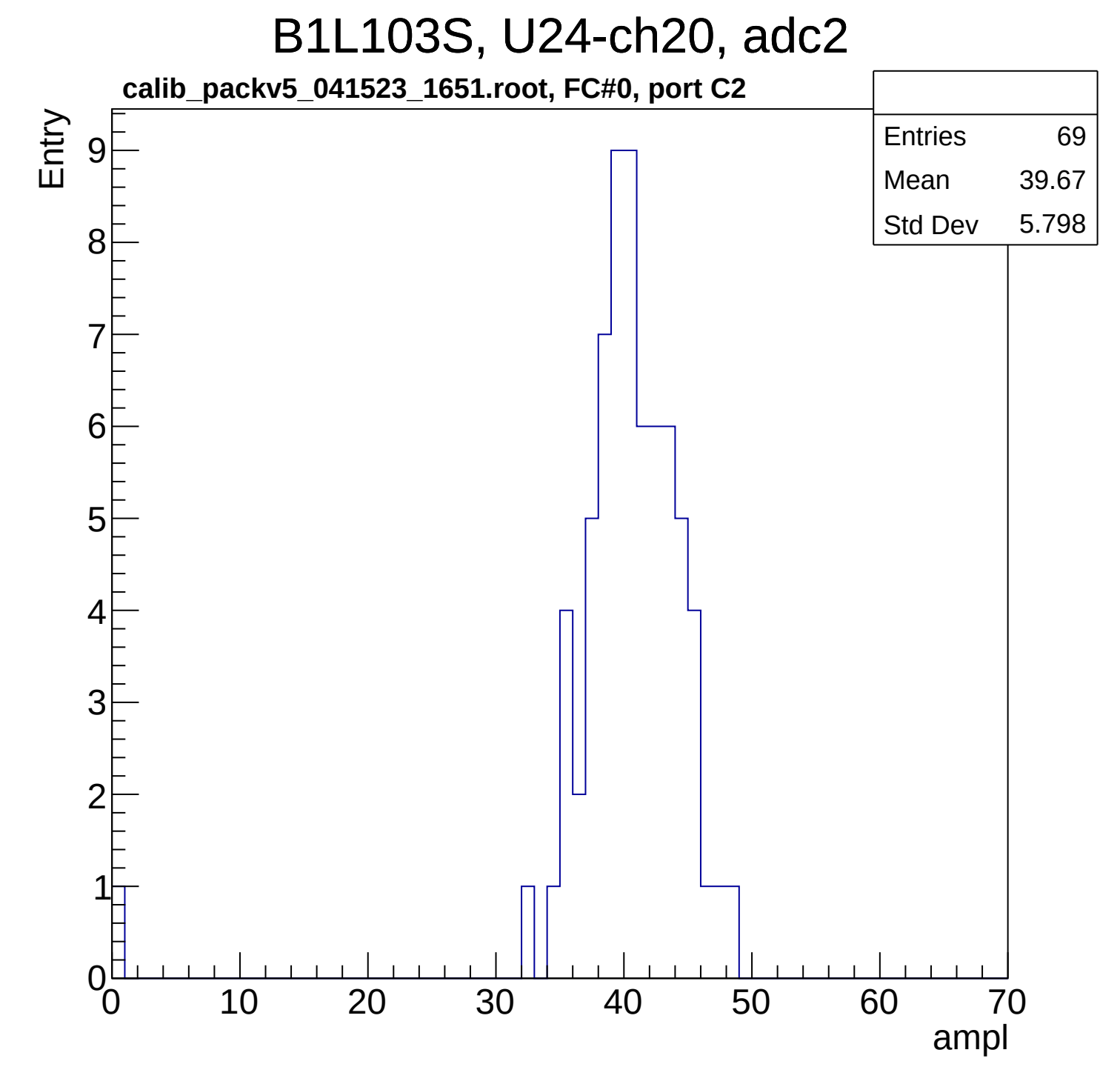

B1L103S, U24-ch19, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch20, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 24.37
Std Dev 10.2
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch20, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 29.76
Std Dev 11.72
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U24-ch20, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 39.67
Std Dev 5.798
Entry
ampl
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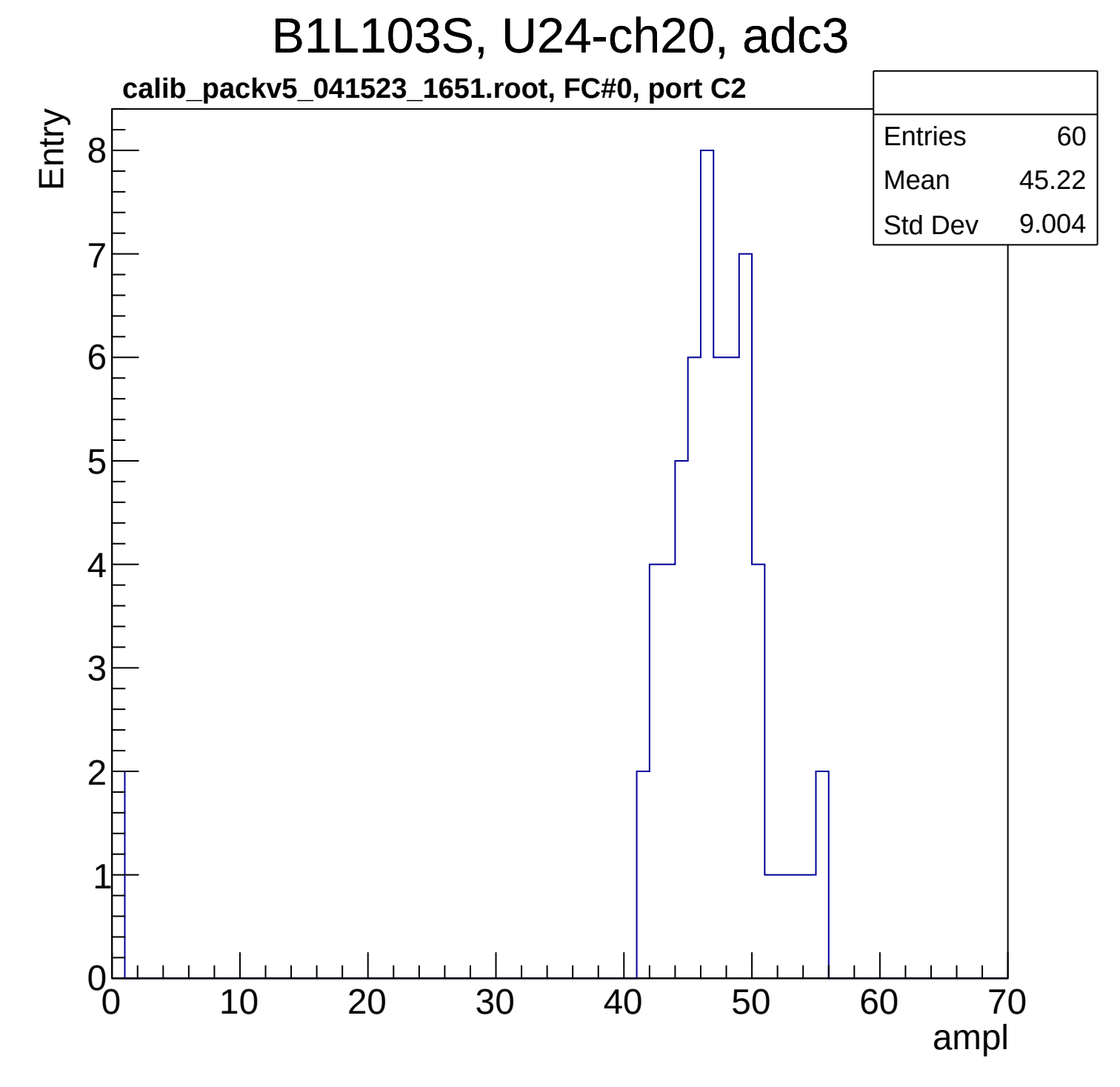
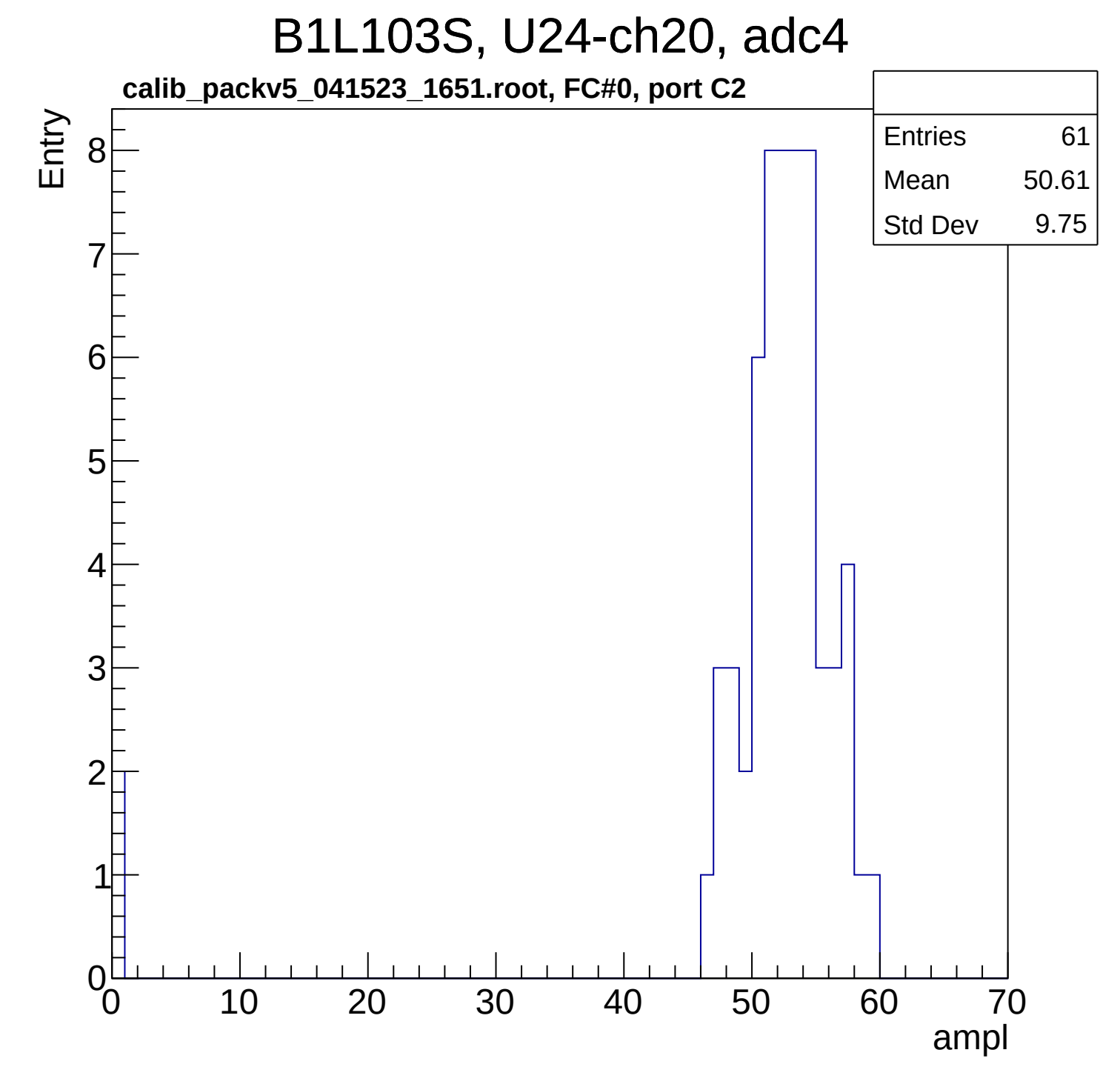
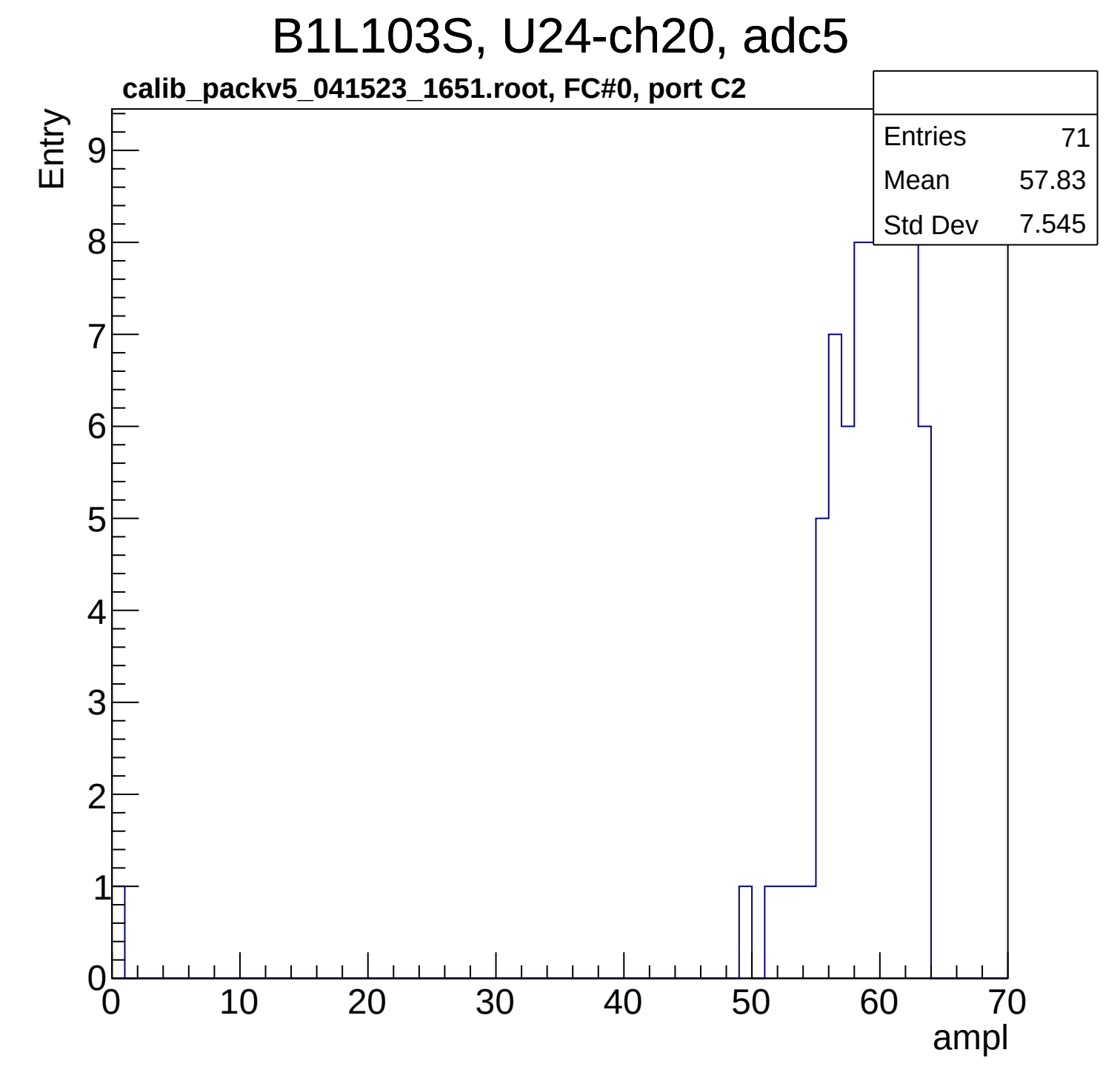
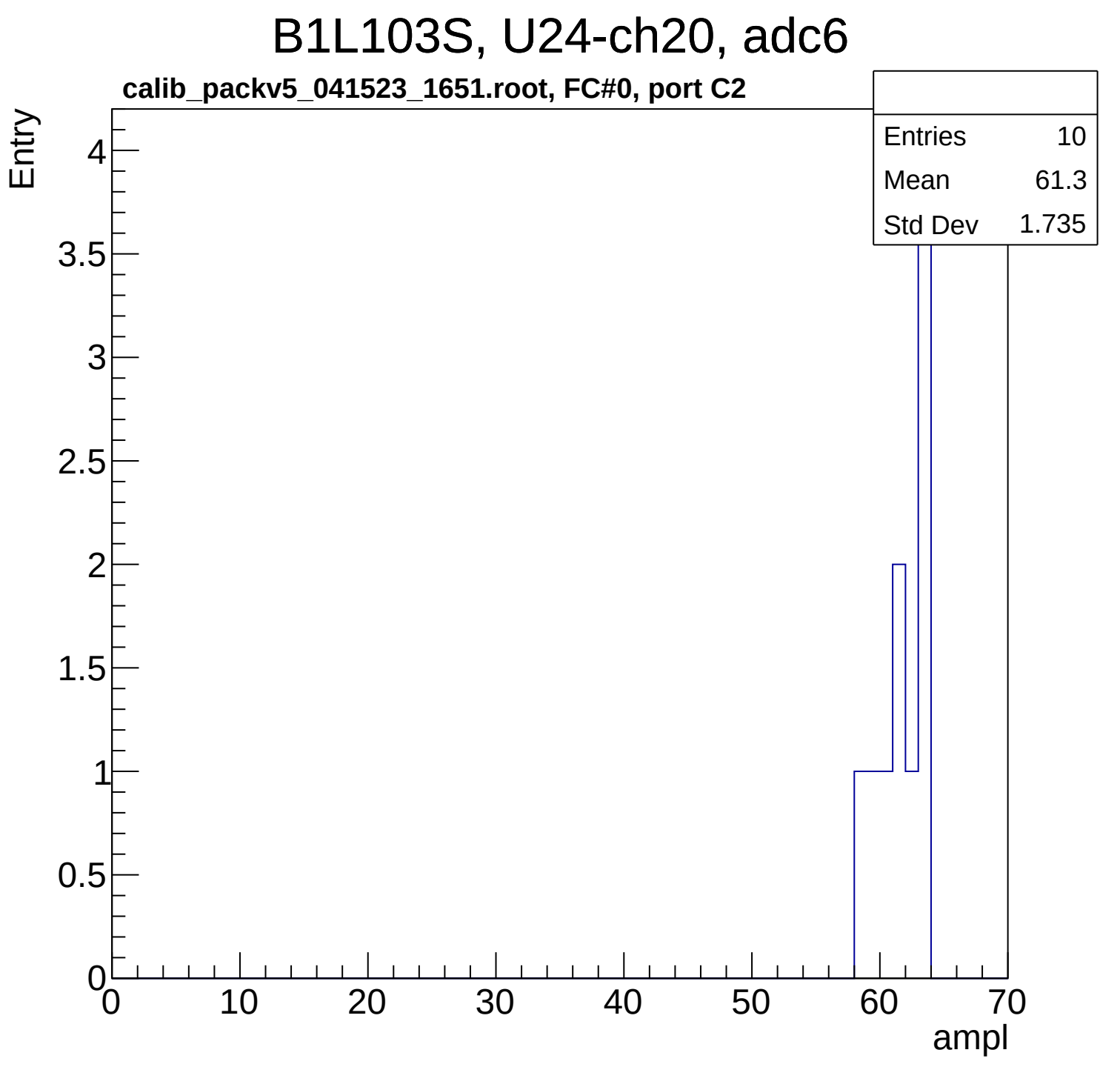
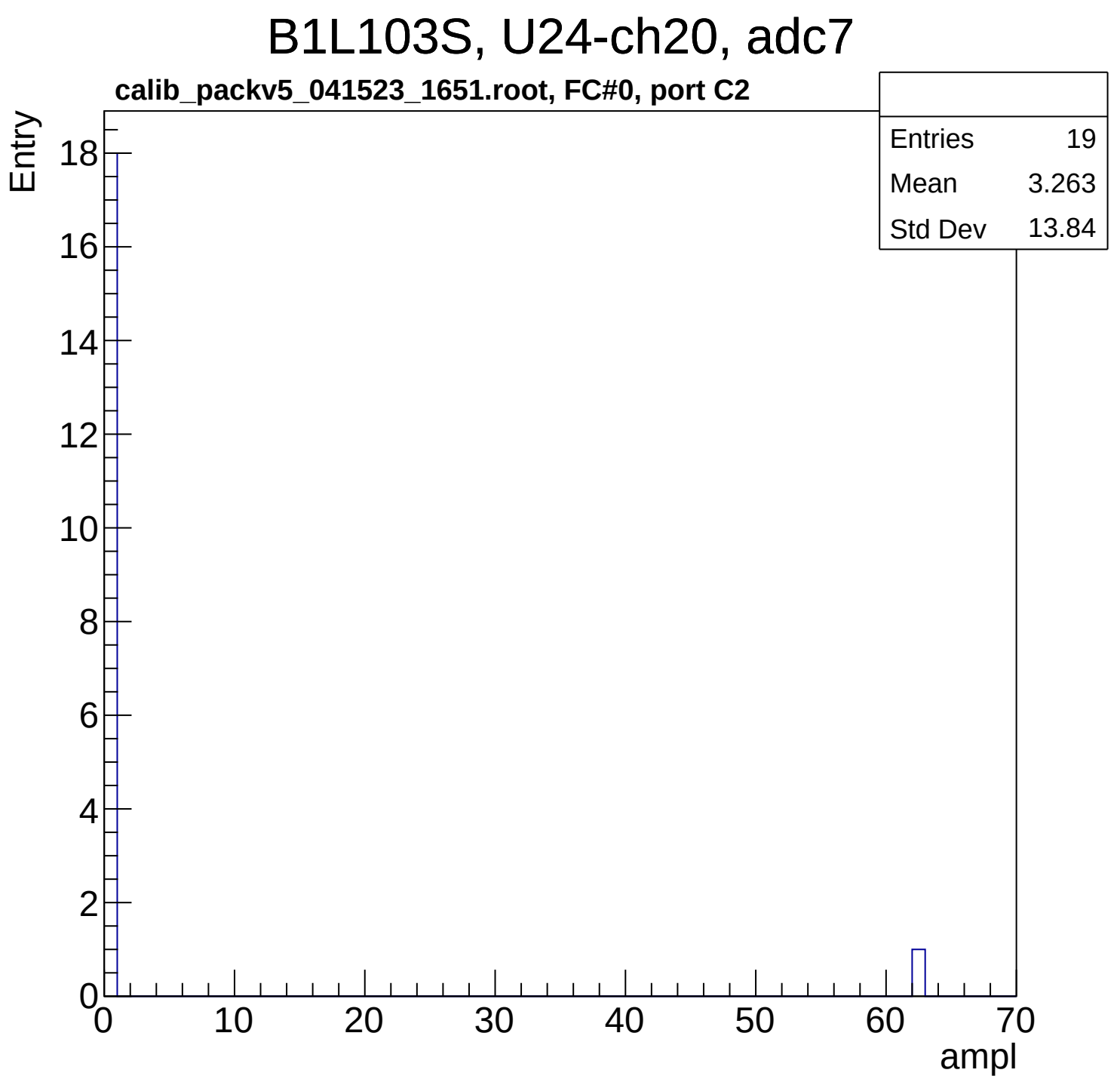
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

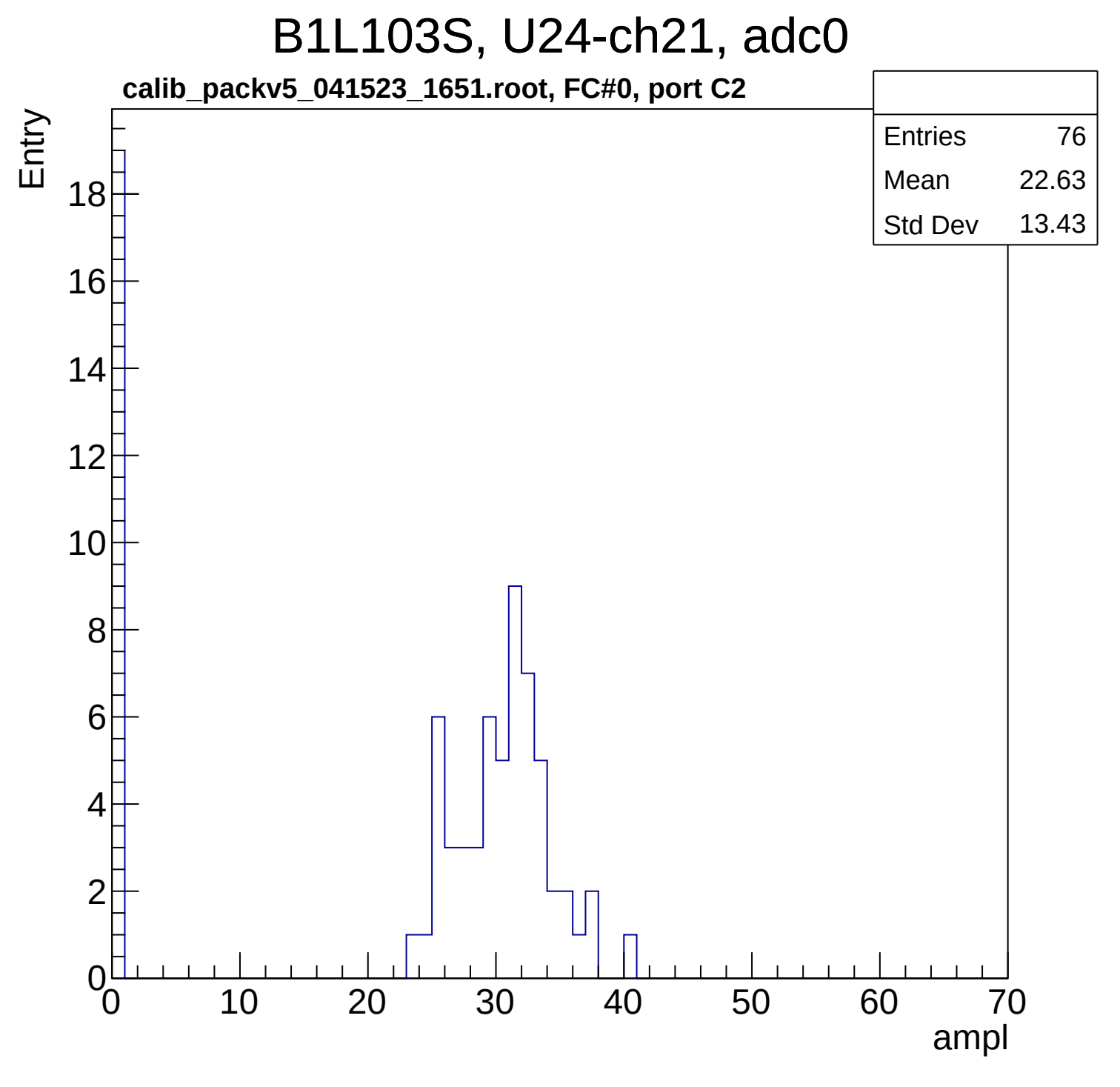

B1L103S, U24-ch20, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 45.22
Std Dev 9.004
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

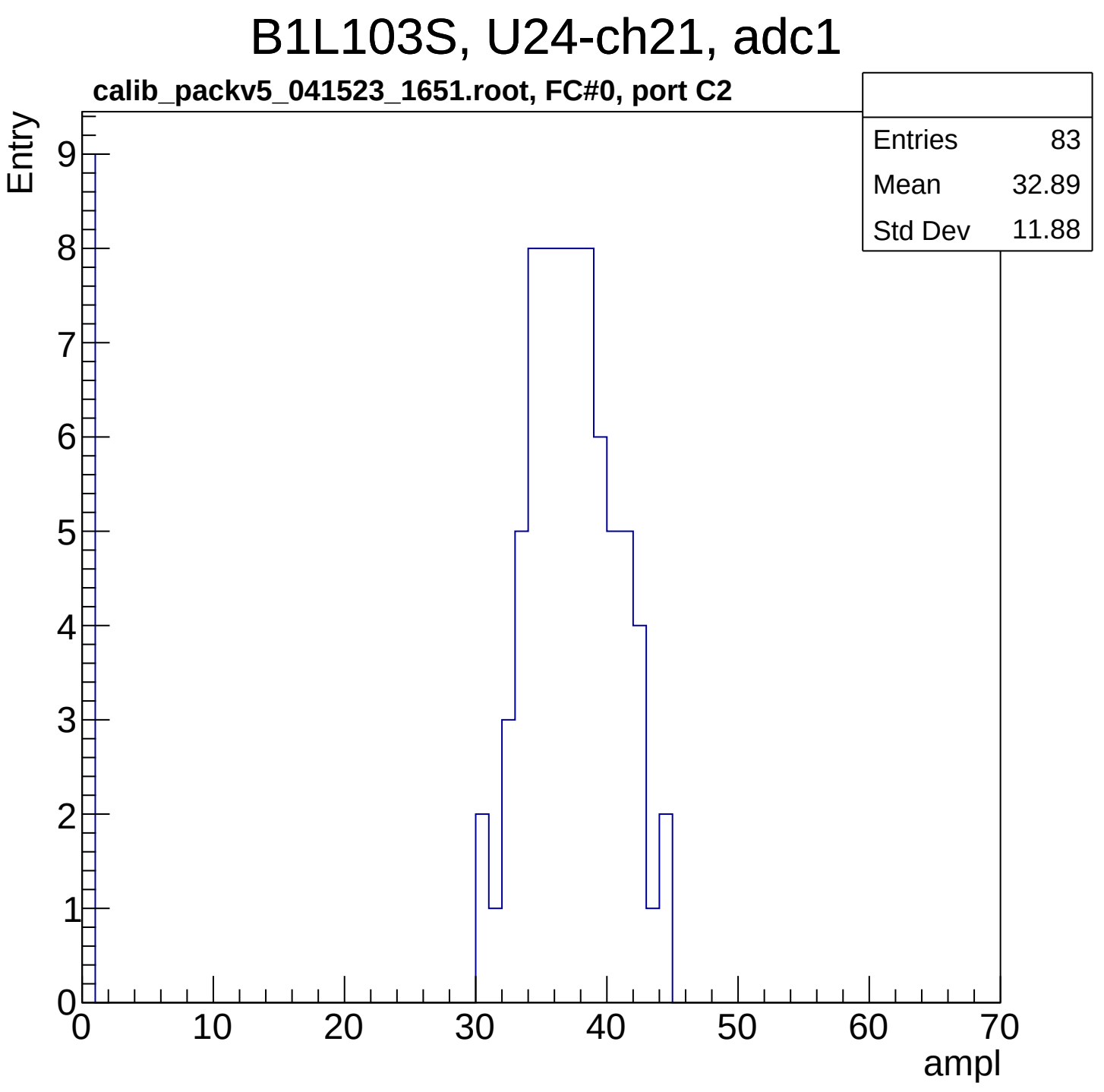

B1L103S, U24-ch20, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 50.61
Std Dev 9.75
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U24-ch20, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 57.83
Std Dev 7.545
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U24-ch20, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 61.3
Std Dev 1.735
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U24-ch20, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 3.263
Std Dev 13.84
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch21, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 22.63
Std Dev 13.43
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch21, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 32.89
Std Dev 11.88
Entry
ampl
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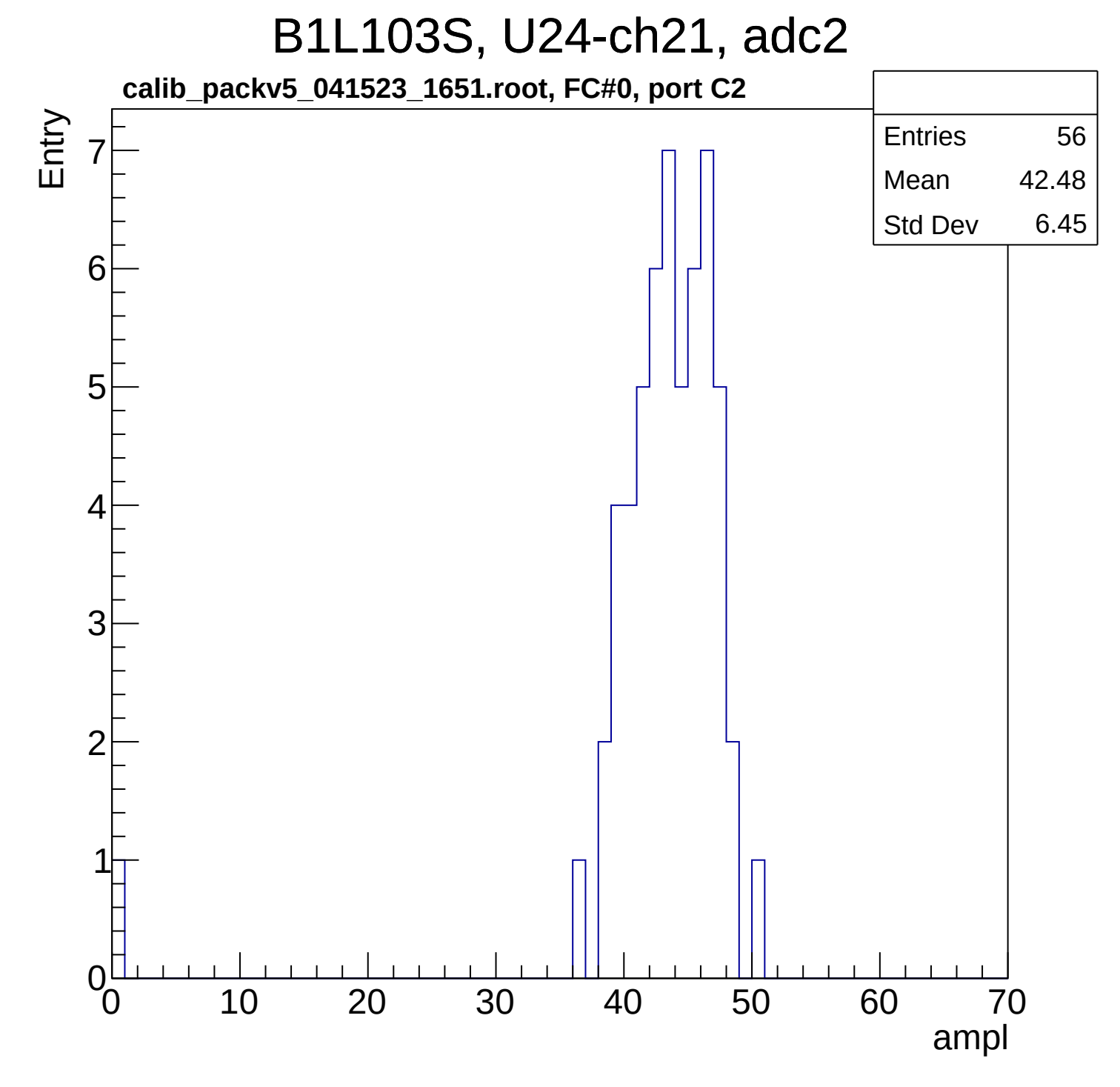
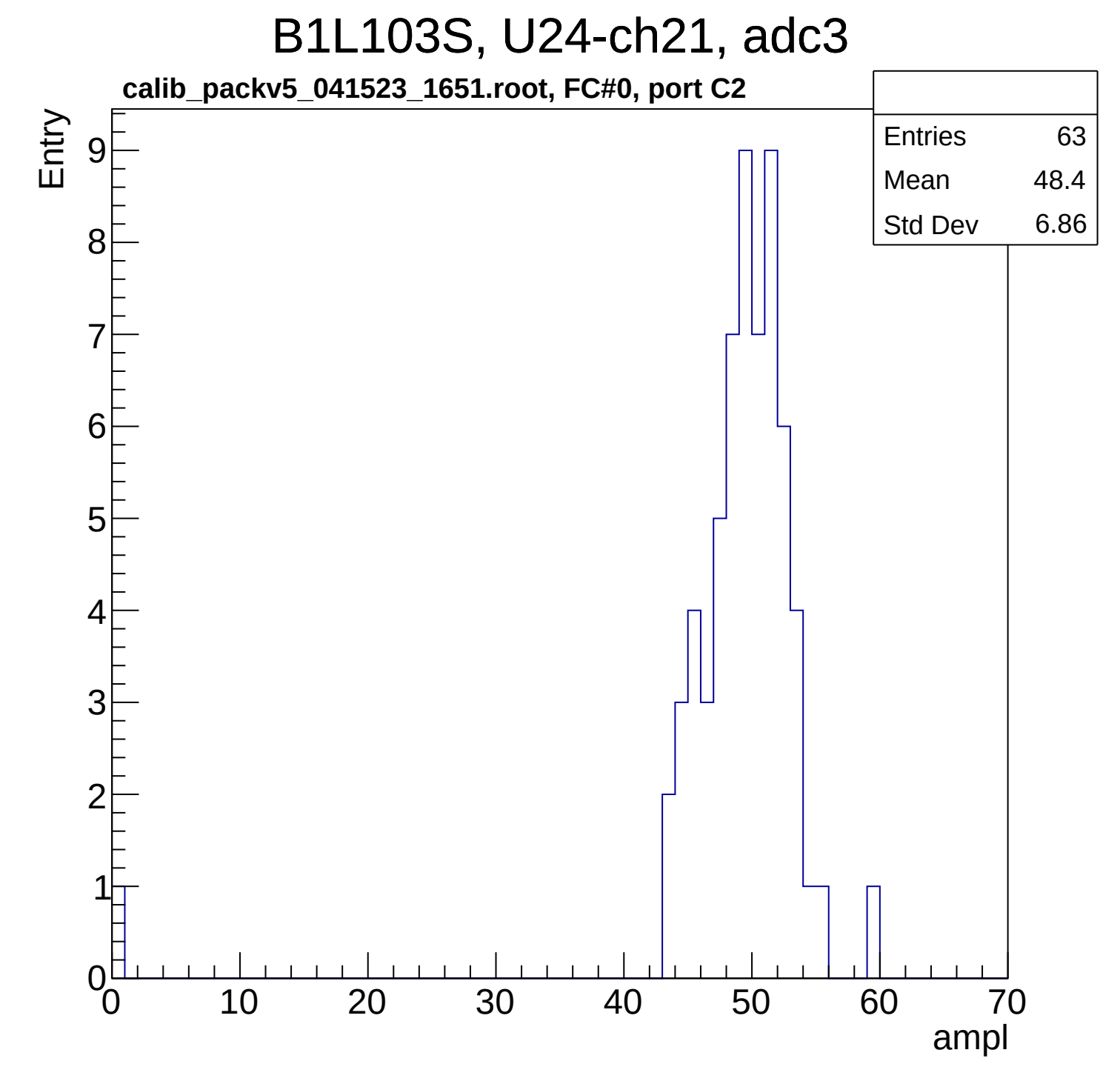
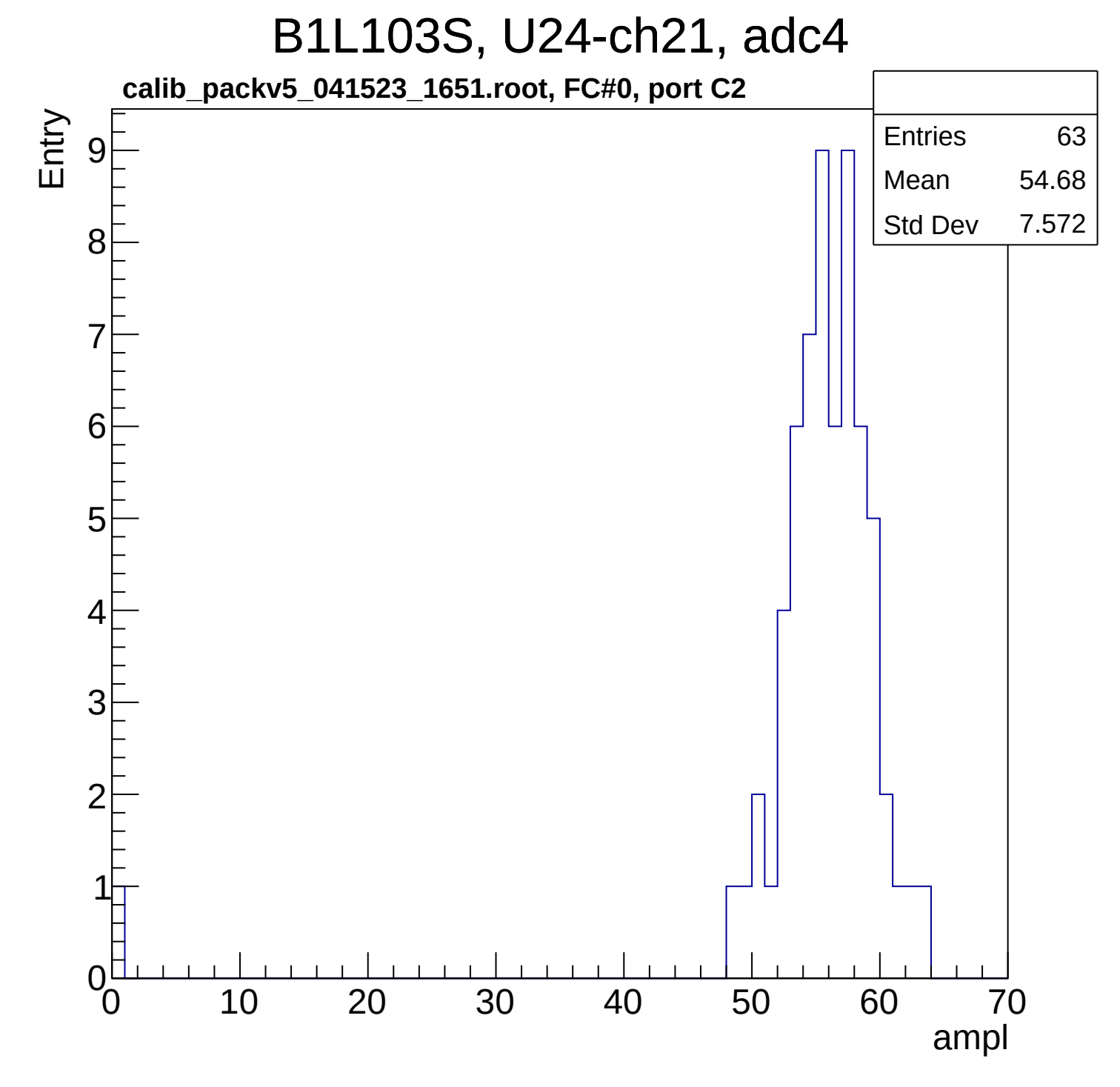
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U24-ch21, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 42.48
Std Dev 6.45
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U24-ch21, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 48.4
Std Dev 6.86
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U24-ch21, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 54.68
Std Dev 7.572
Entry
ampl
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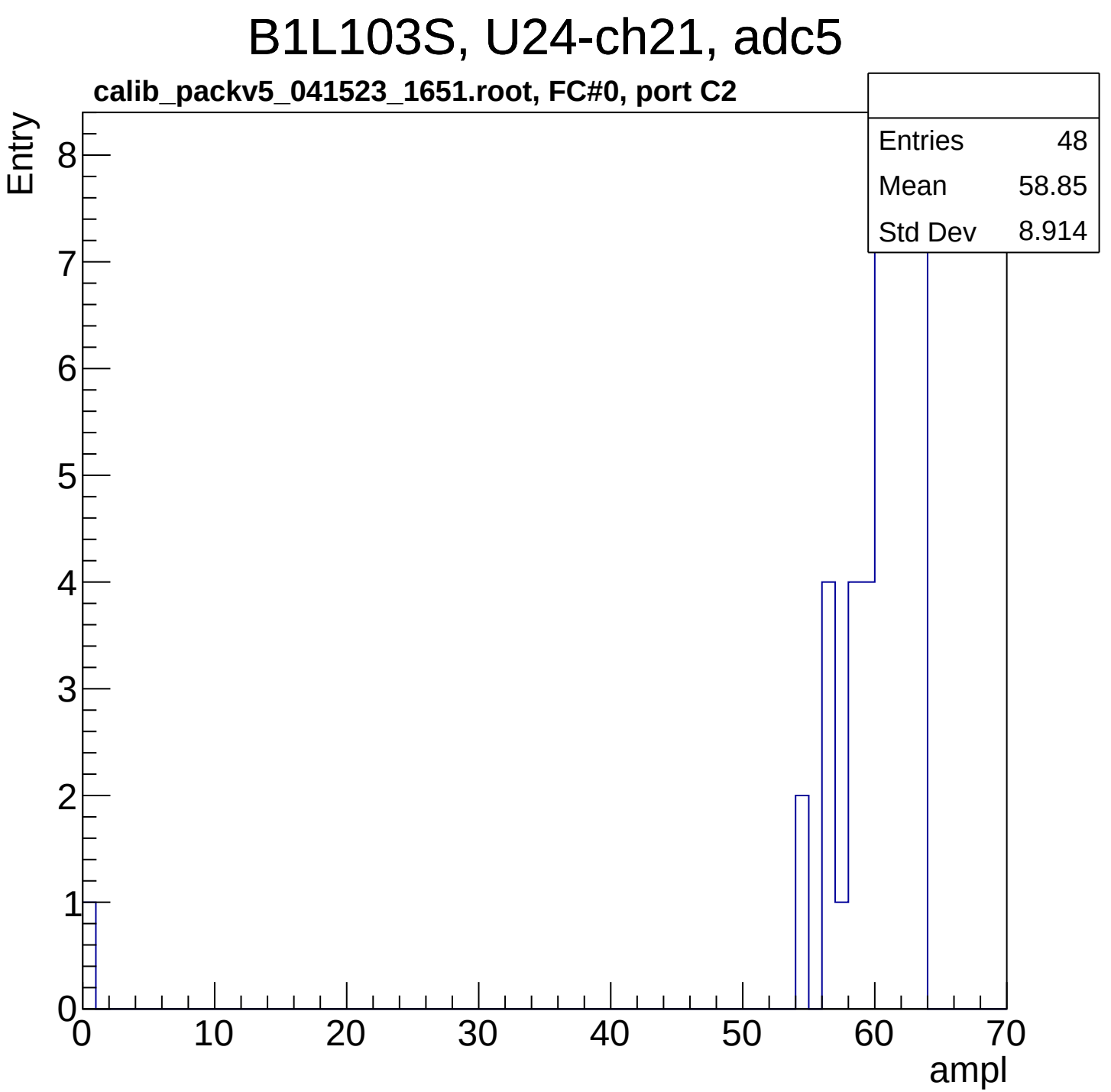
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U24-ch21, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 58.85
Std Dev 8.914
Entry
ampl
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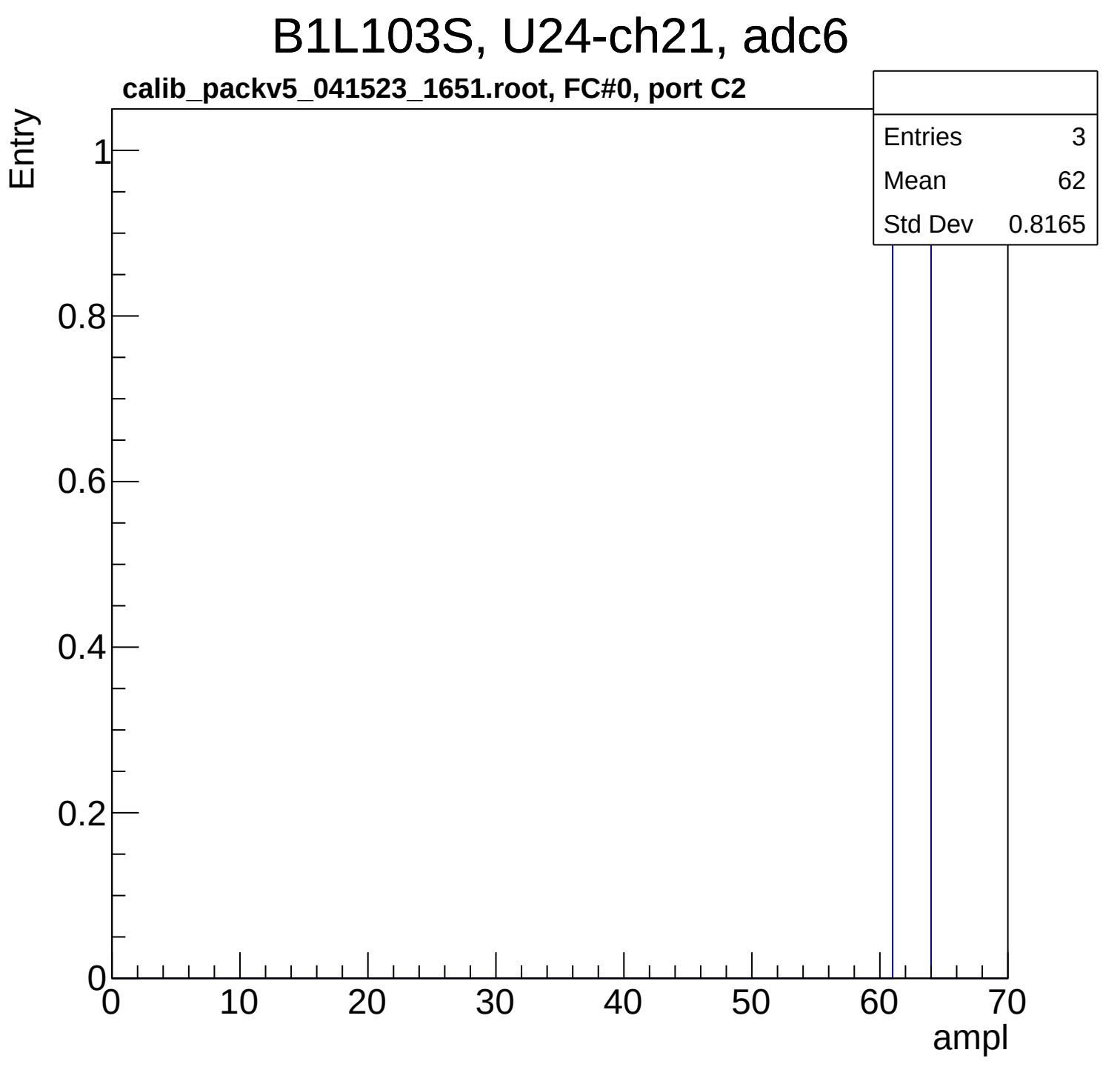
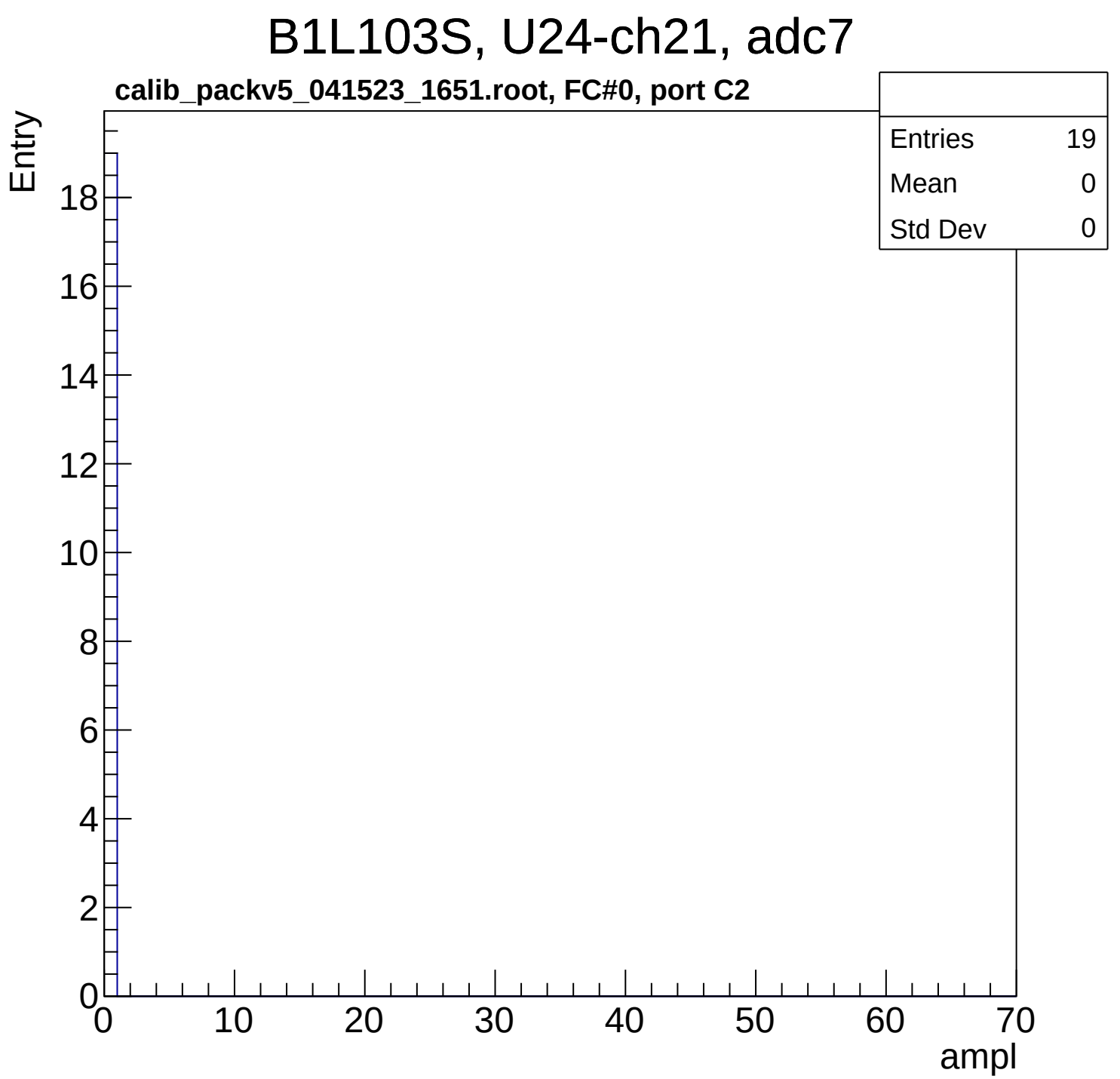
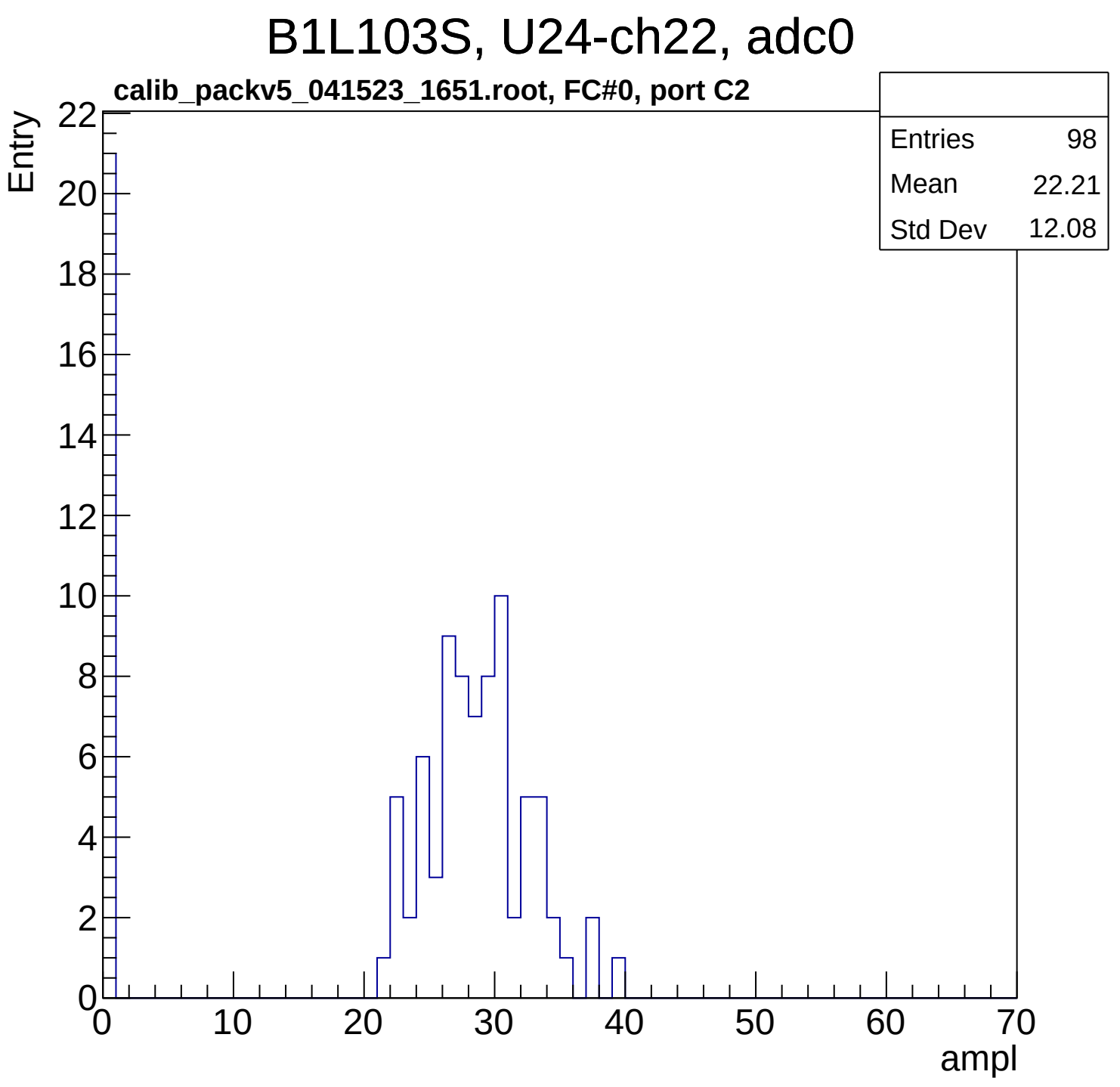
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U24-ch21, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 3
Mean 62
Std Dev 0.8165
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch21, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch22, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 98
Mean 22.21
Std Dev 12.08
Entry
ampl
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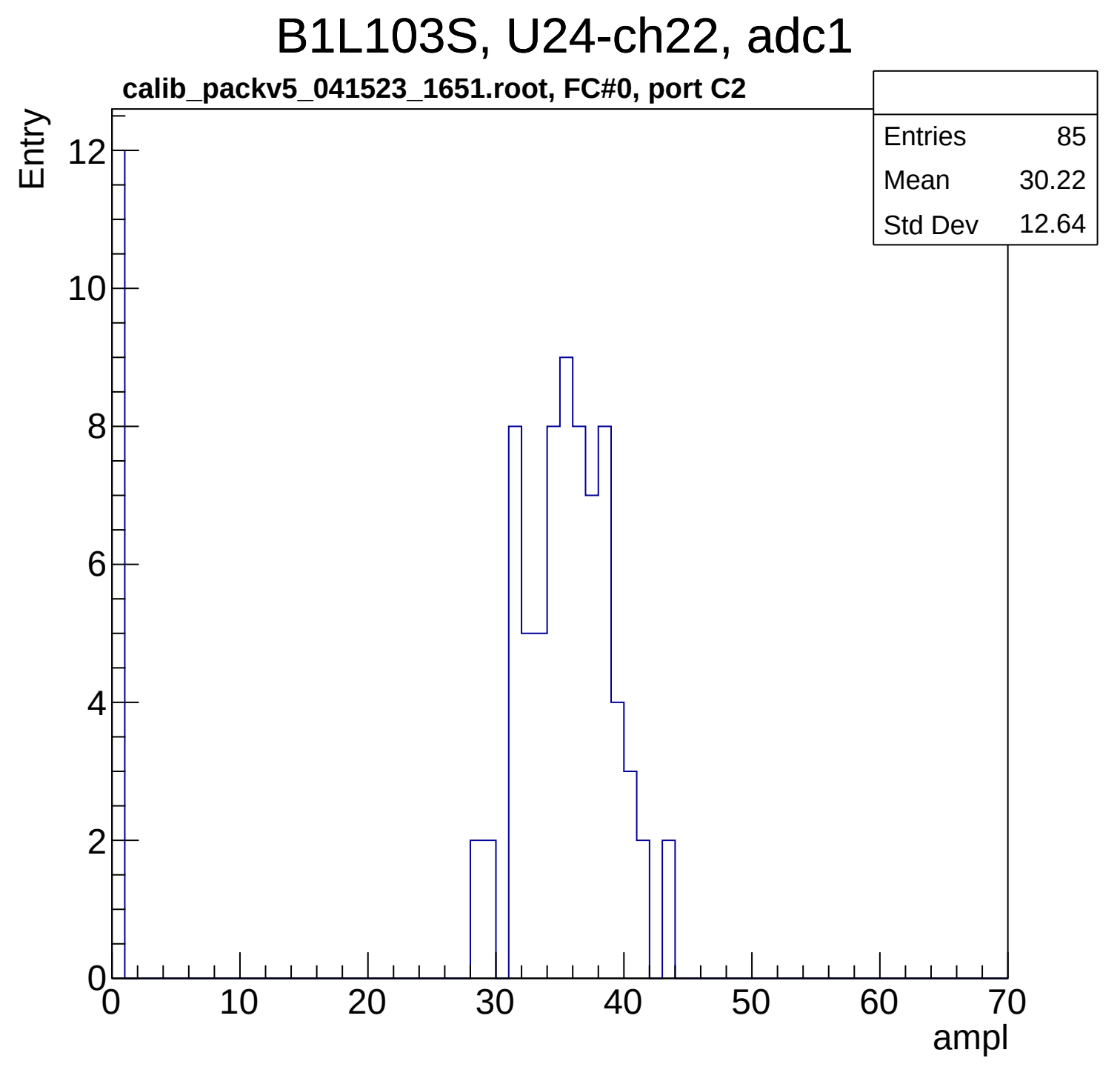
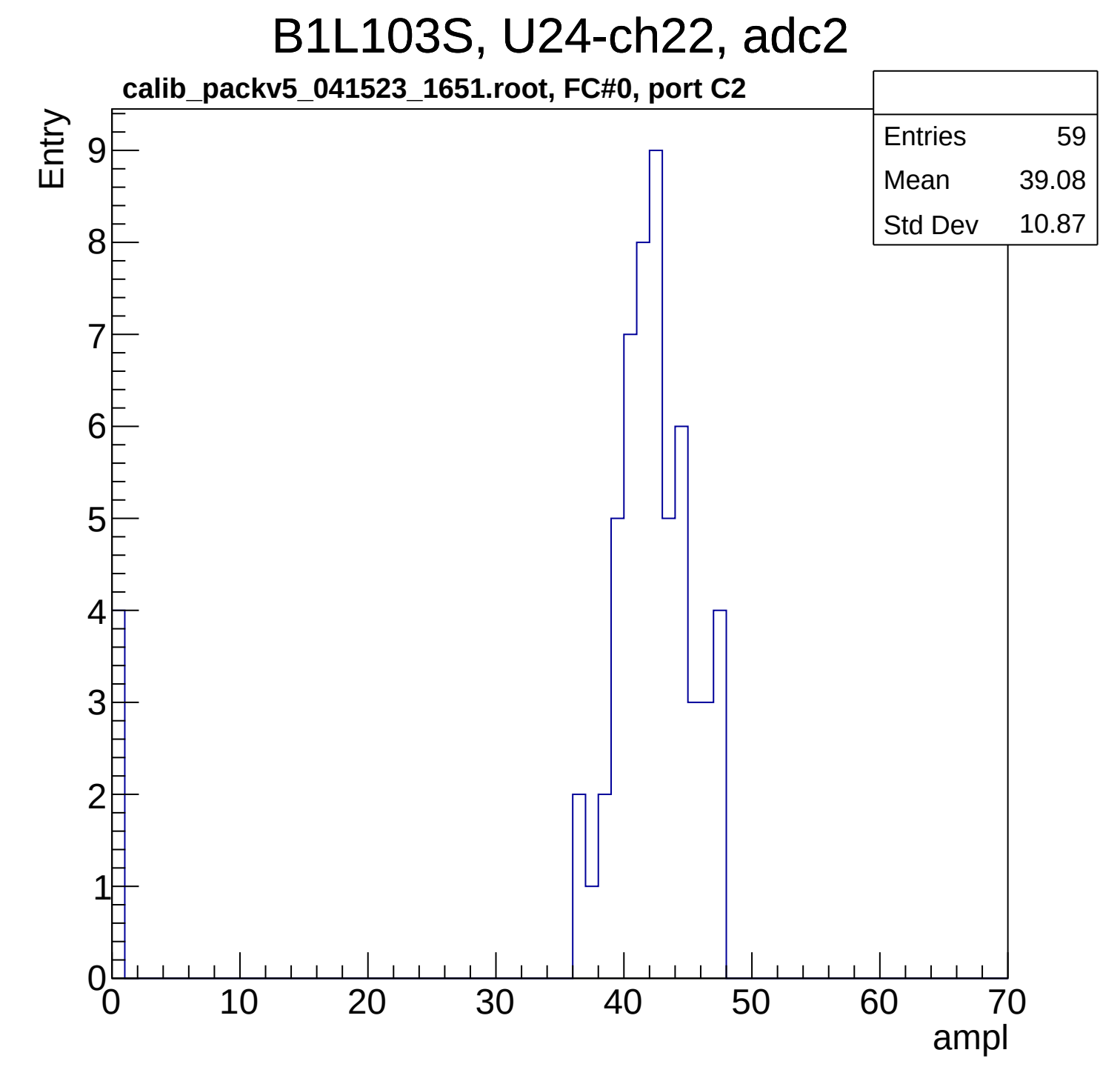
8
10
12
14
16
18
20
22
0
10
20
30
40
50
60
70


B1L103S, U24-ch22, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 30.22
Std Dev 12.64
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch22, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 39.08
Std Dev 10.87
Entry
ampl
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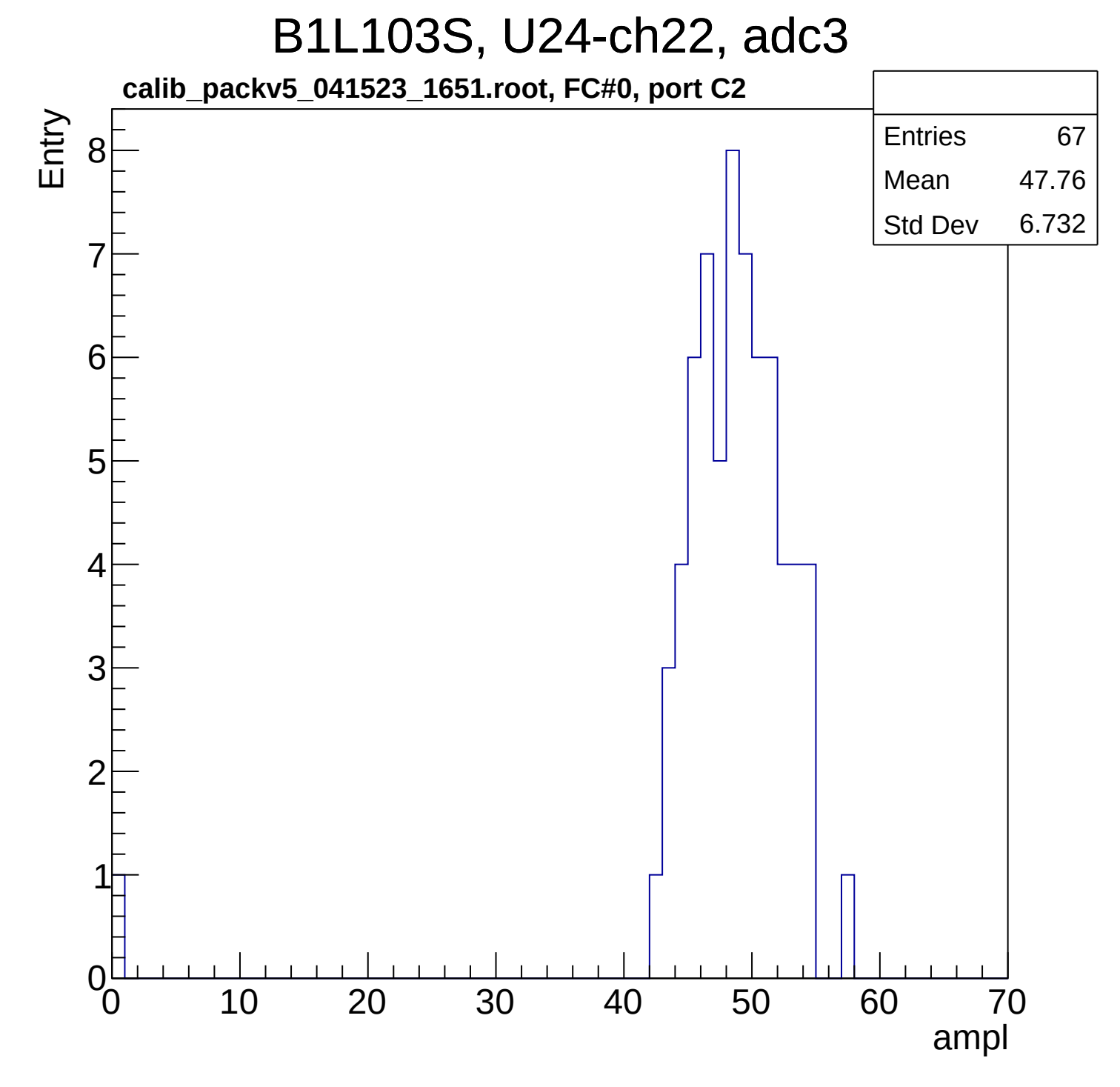
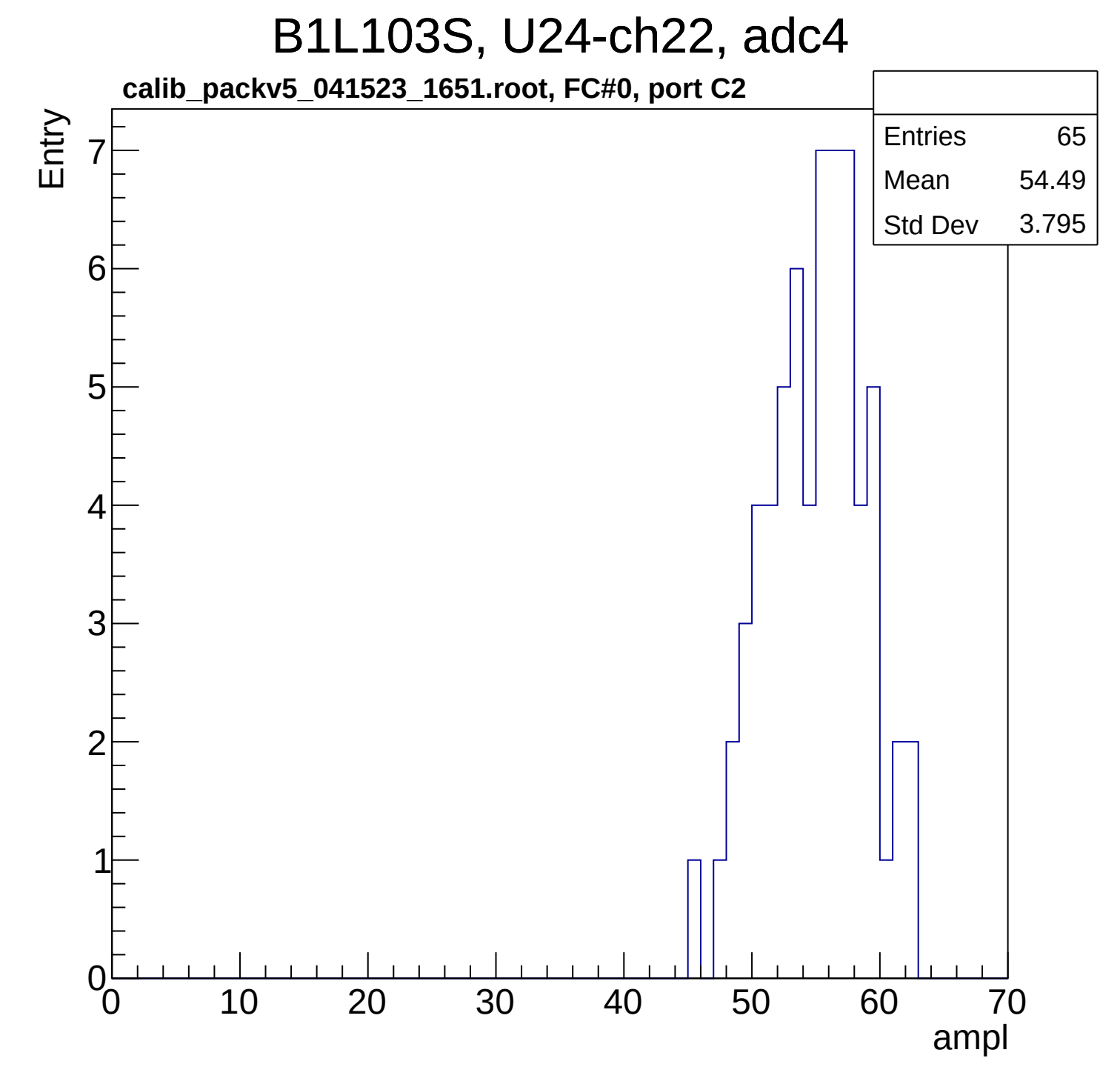
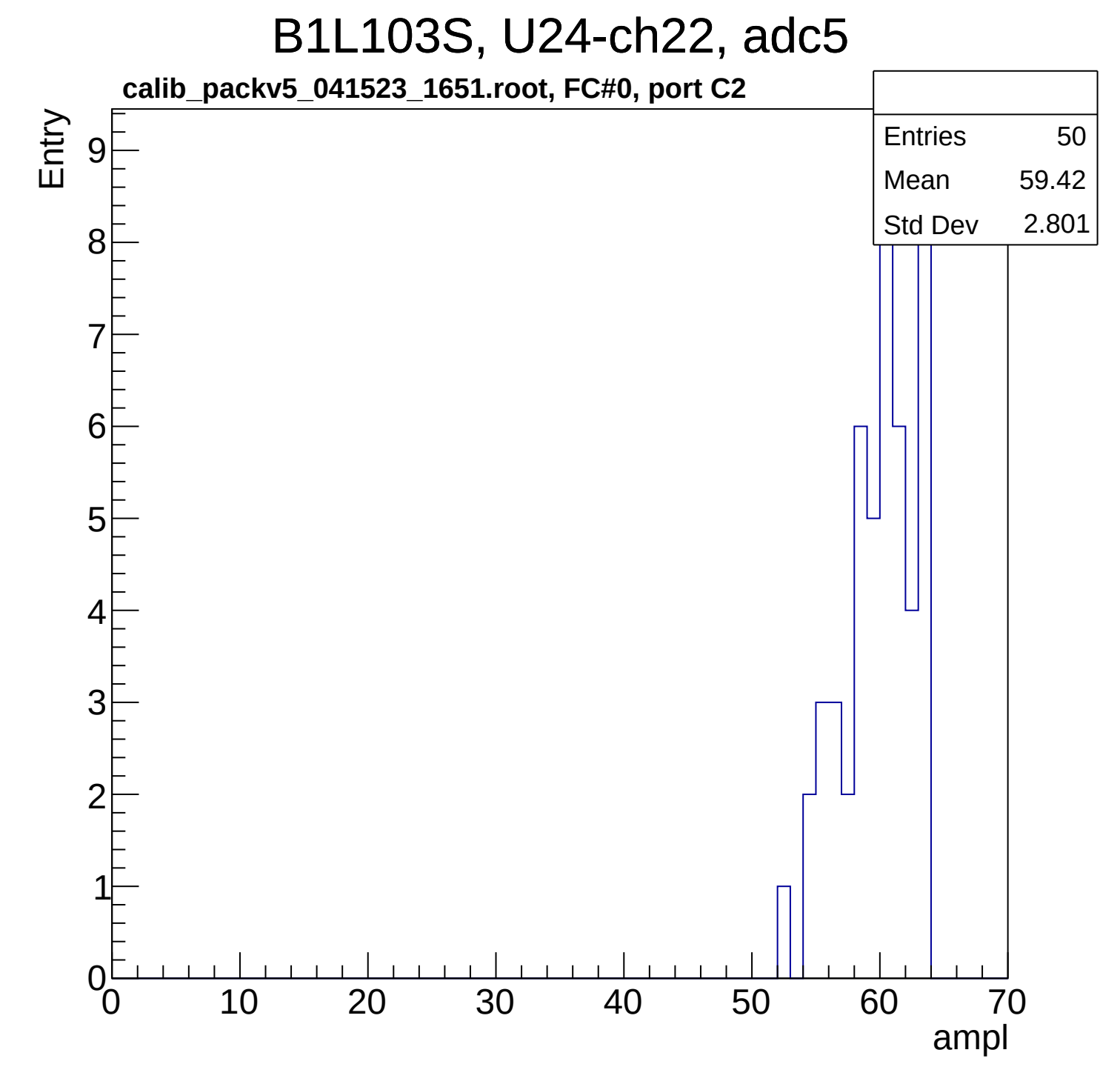
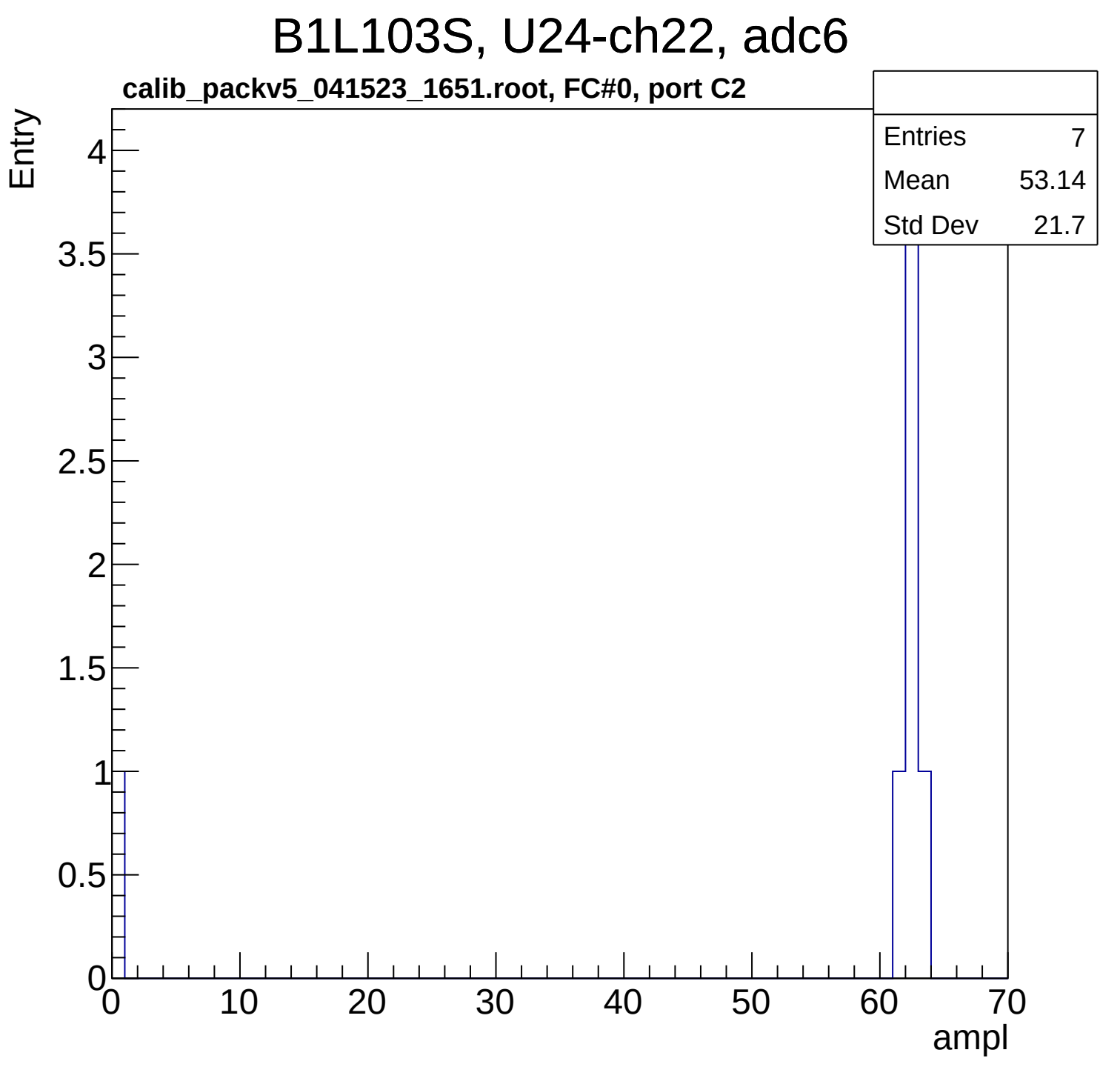
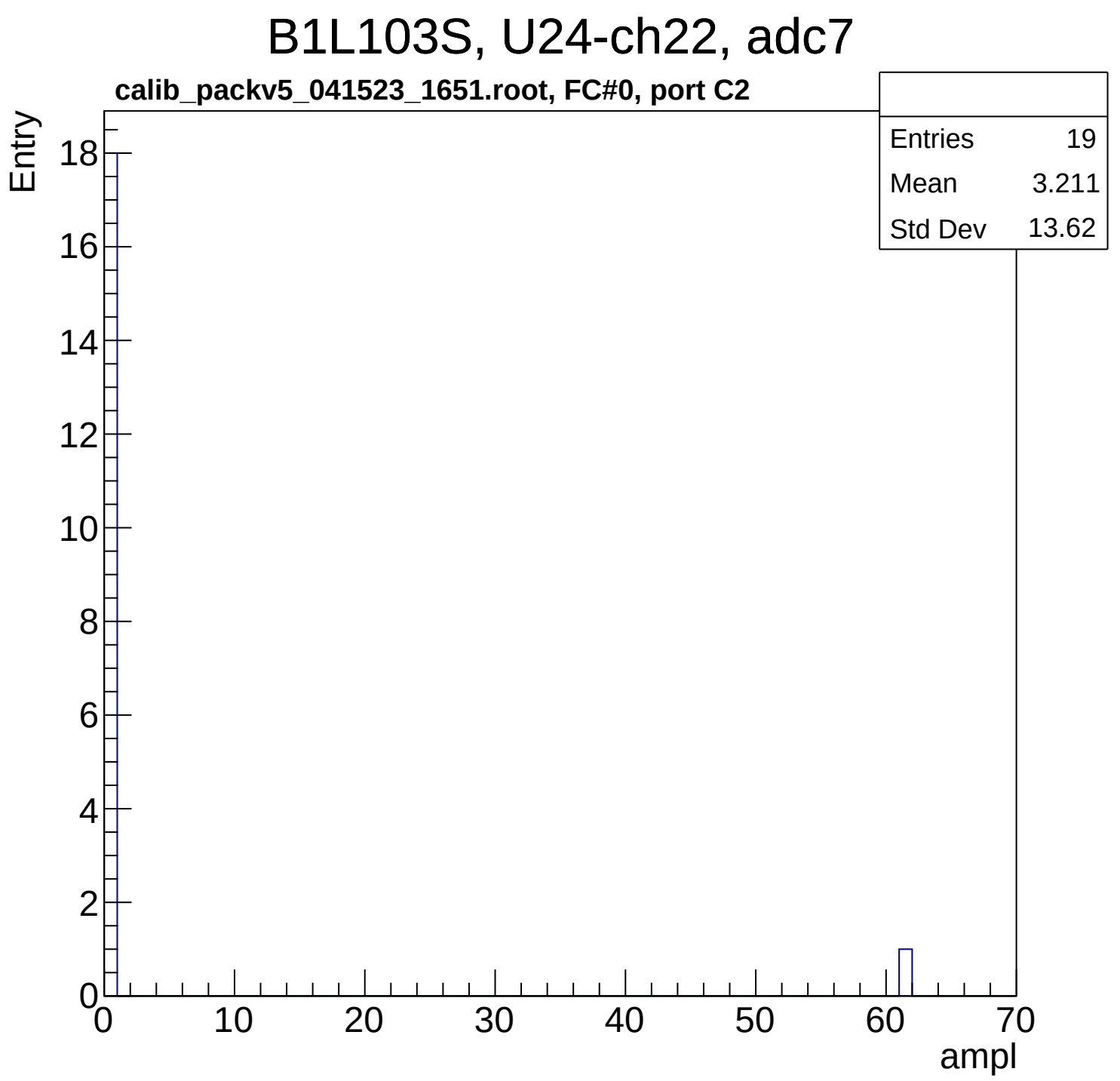
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U24-ch22, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 47.76
Std Dev 6.732
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U24-ch22, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 54.49
Std Dev 3.795
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U24-ch22, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 59.42
Std Dev 2.801
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U24-ch22, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 53.14
Std Dev 21.7
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U24-ch22, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 3.211
Std Dev 13.62
Entry
0
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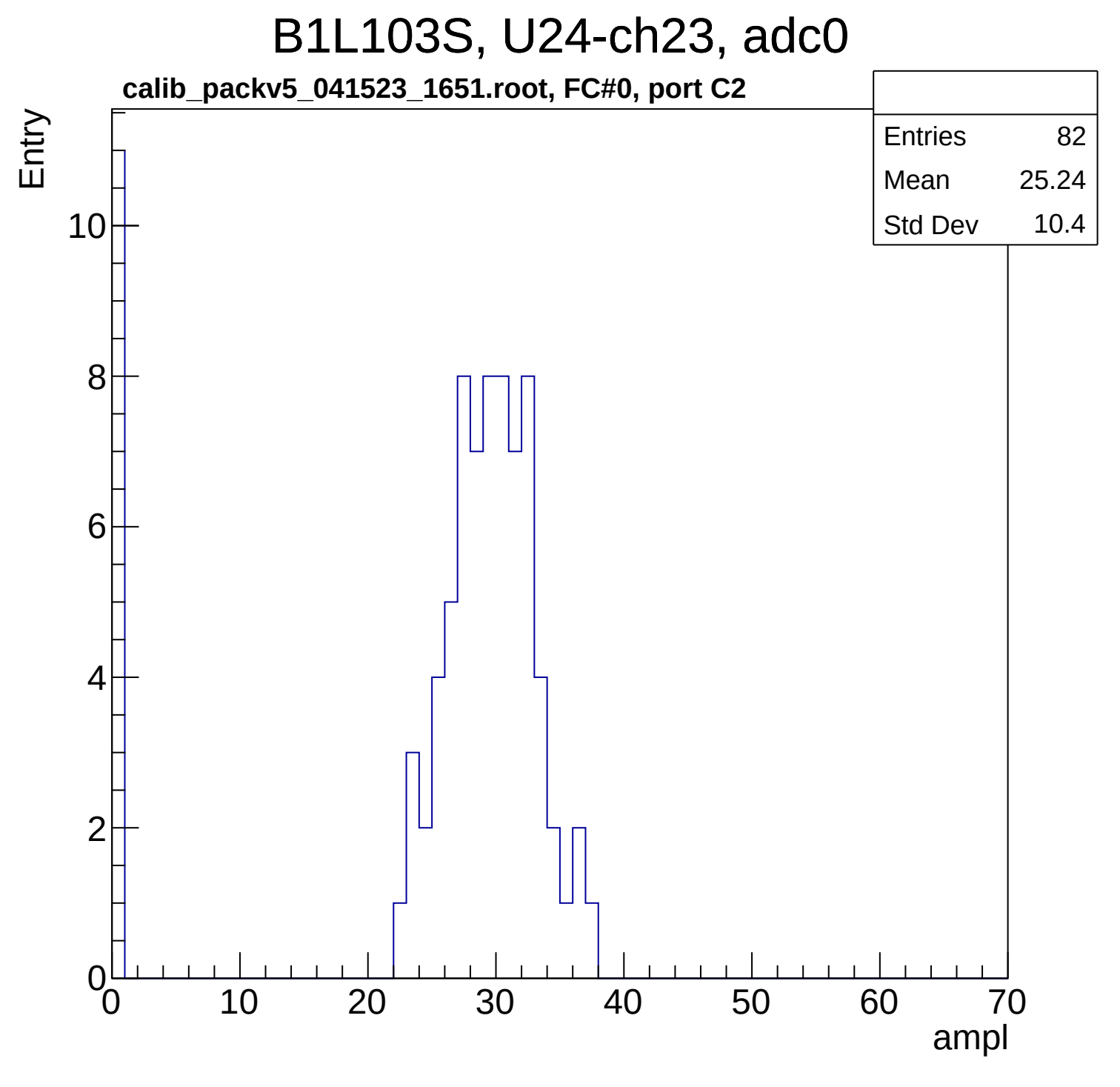
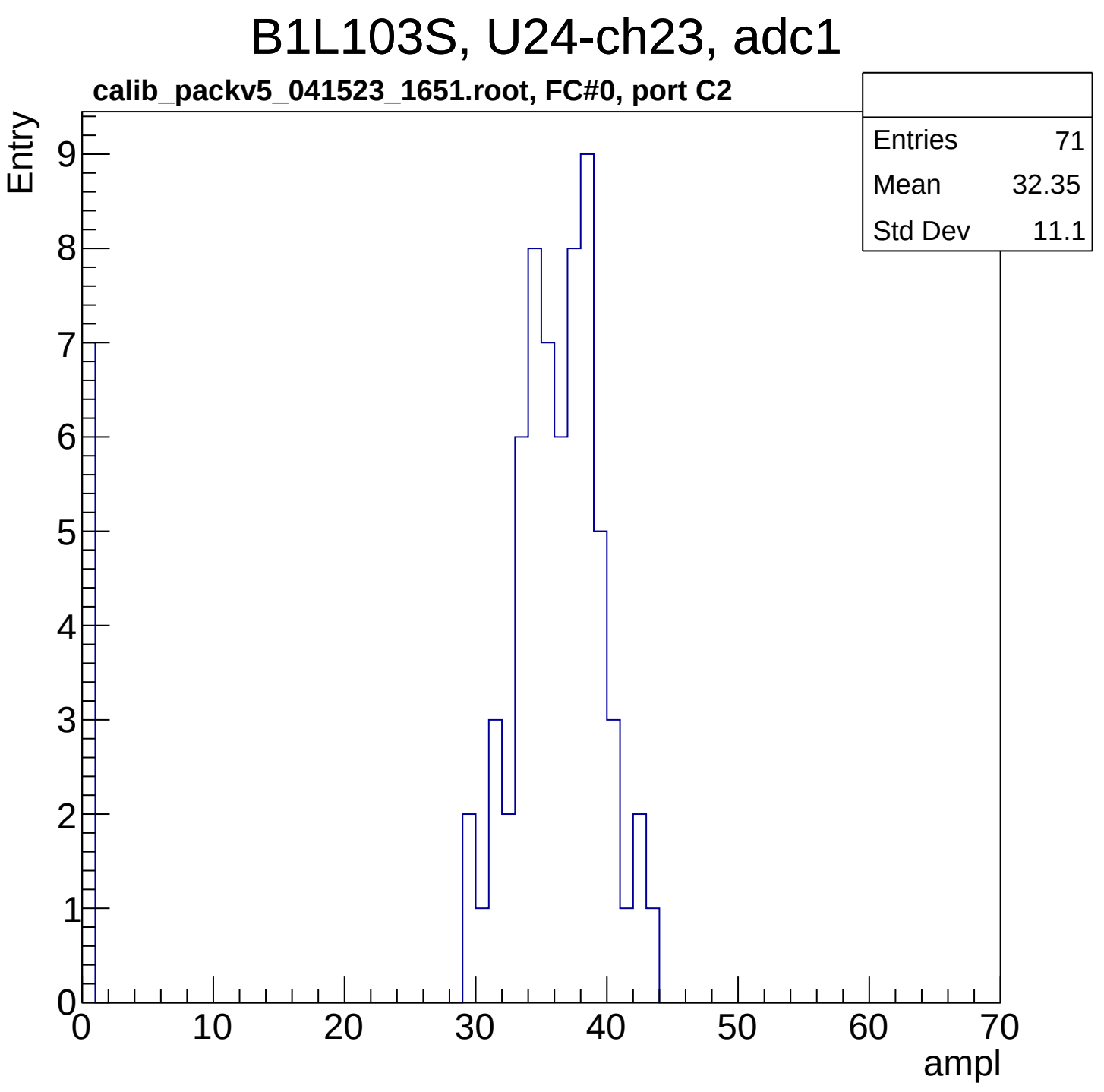
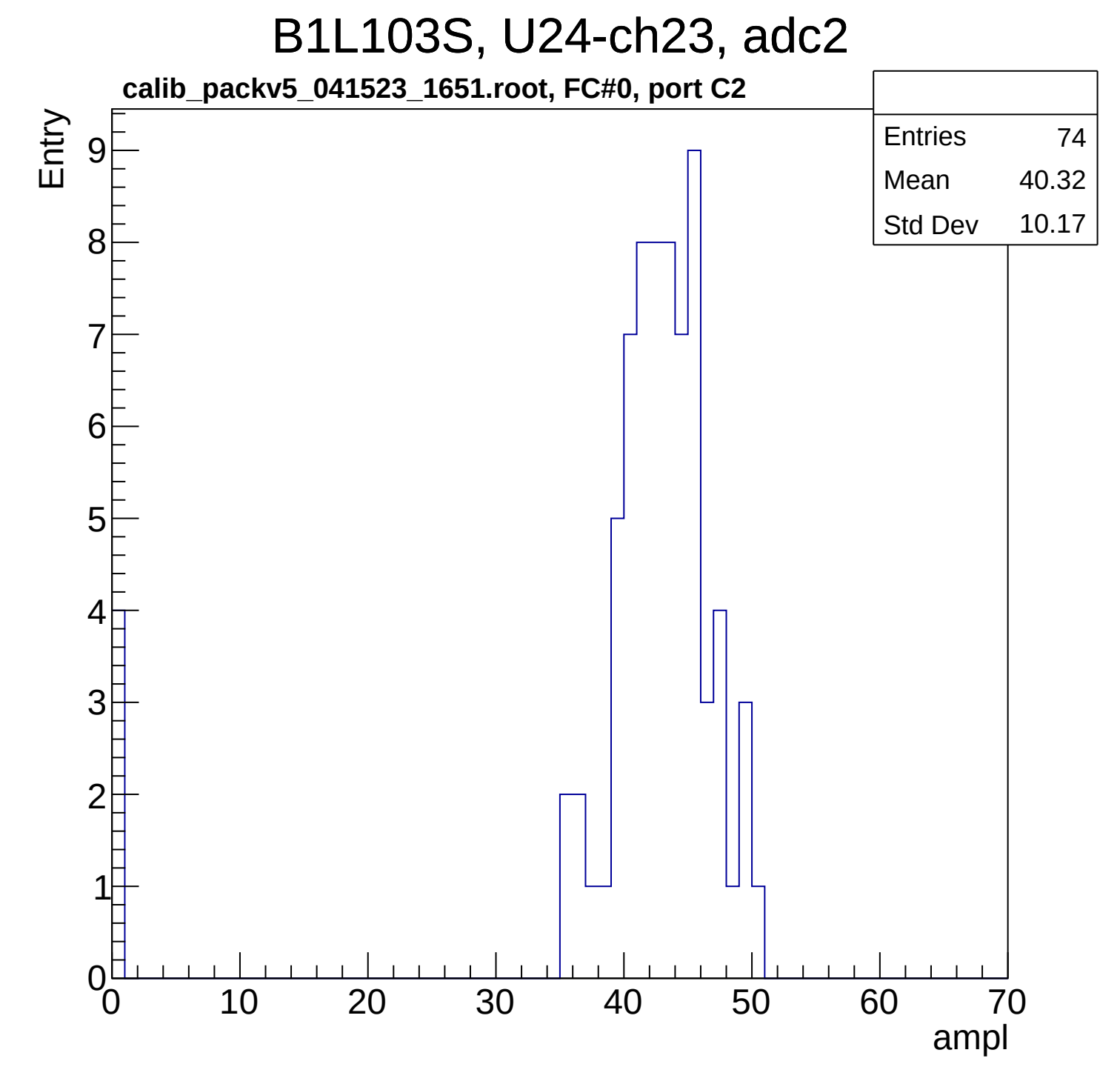
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch23, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 25.24
Std Dev 10.4
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch23, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 32.35
Std Dev 11.1
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U24-ch23, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 40.32
Std Dev 10.17
Entry
ampl
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2
3
4
5
6
7
8
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0
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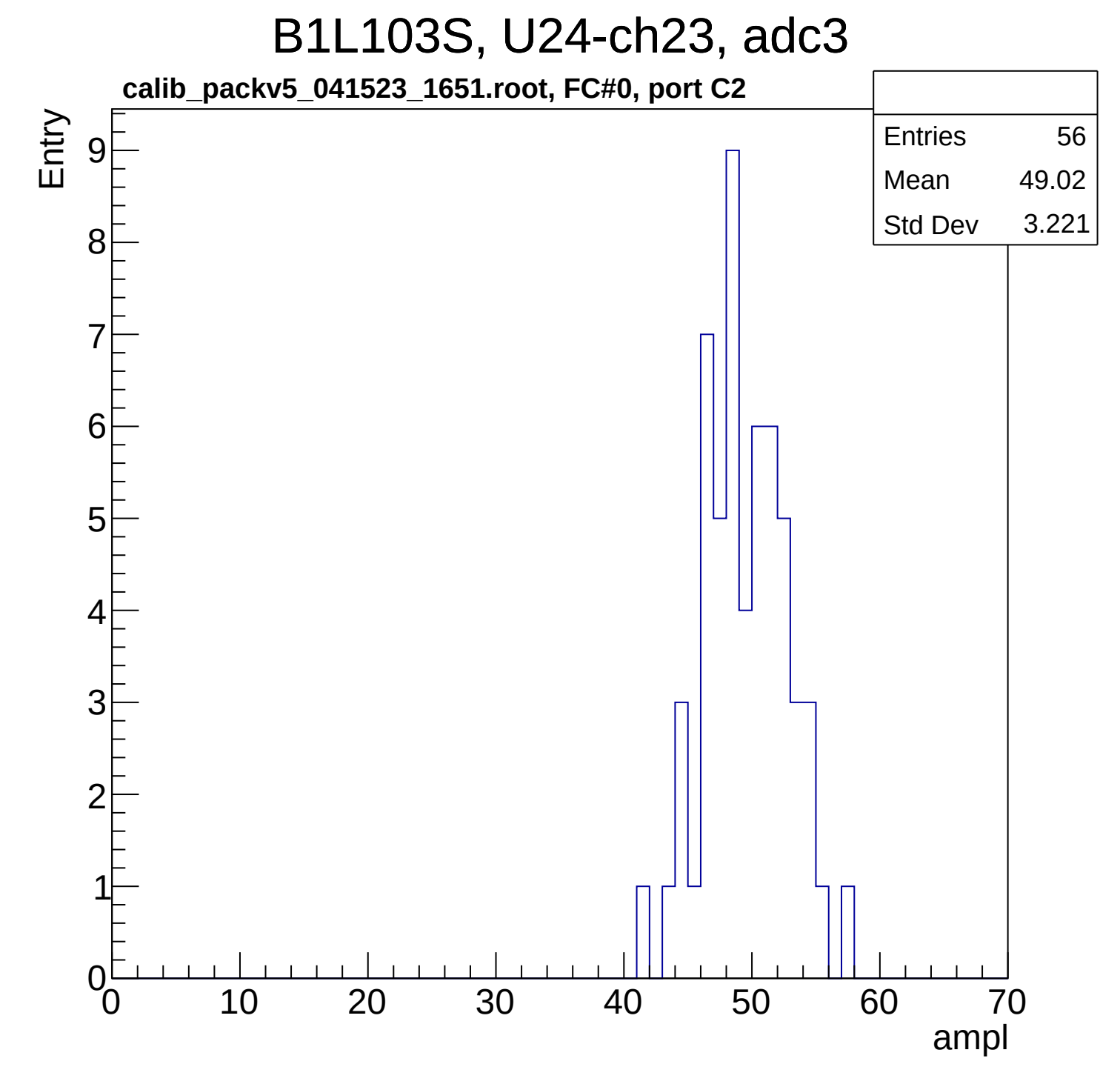
B1L103S, U24-ch23, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 49.02
Std Dev 3.221
Entry
ampl
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0
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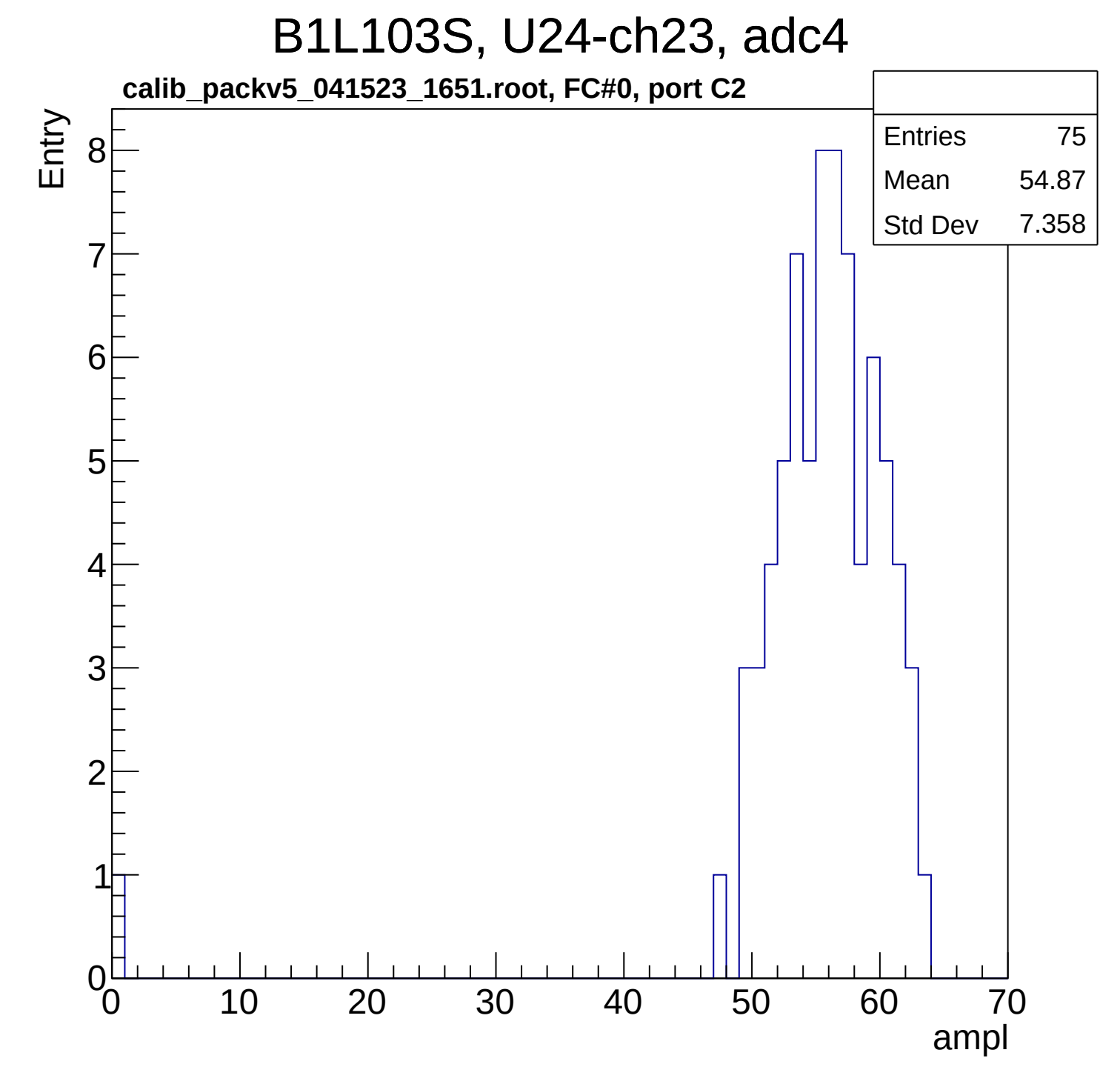
B1L103S, U24-ch23, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 54.87
Std Dev 7.358
Entry
ampl
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2
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4
5
6
7
8
0
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40
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60
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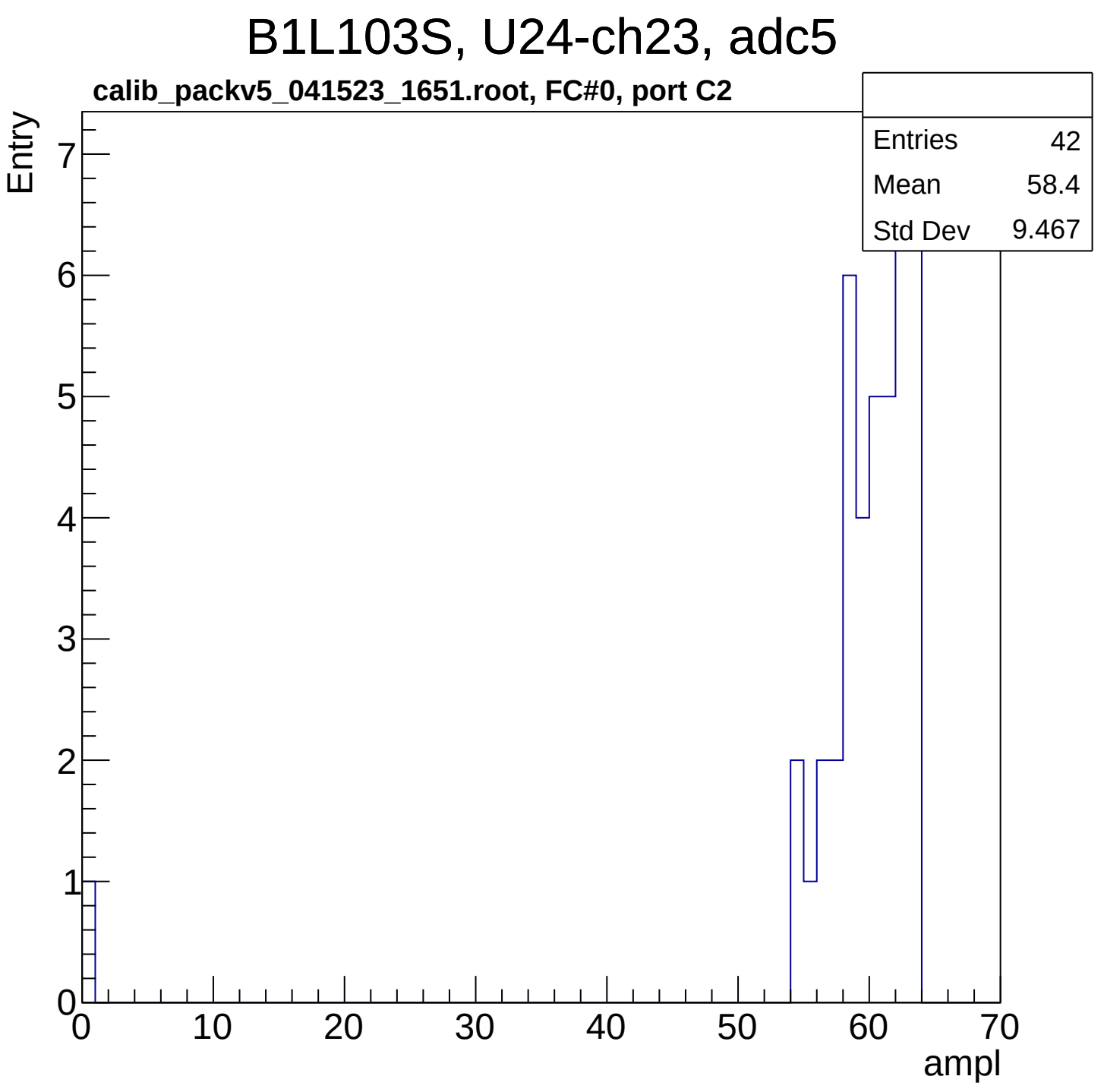
B1L103S, U24-ch23, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 42
Mean 58.4
Std Dev 9.467
Entry
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7
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50
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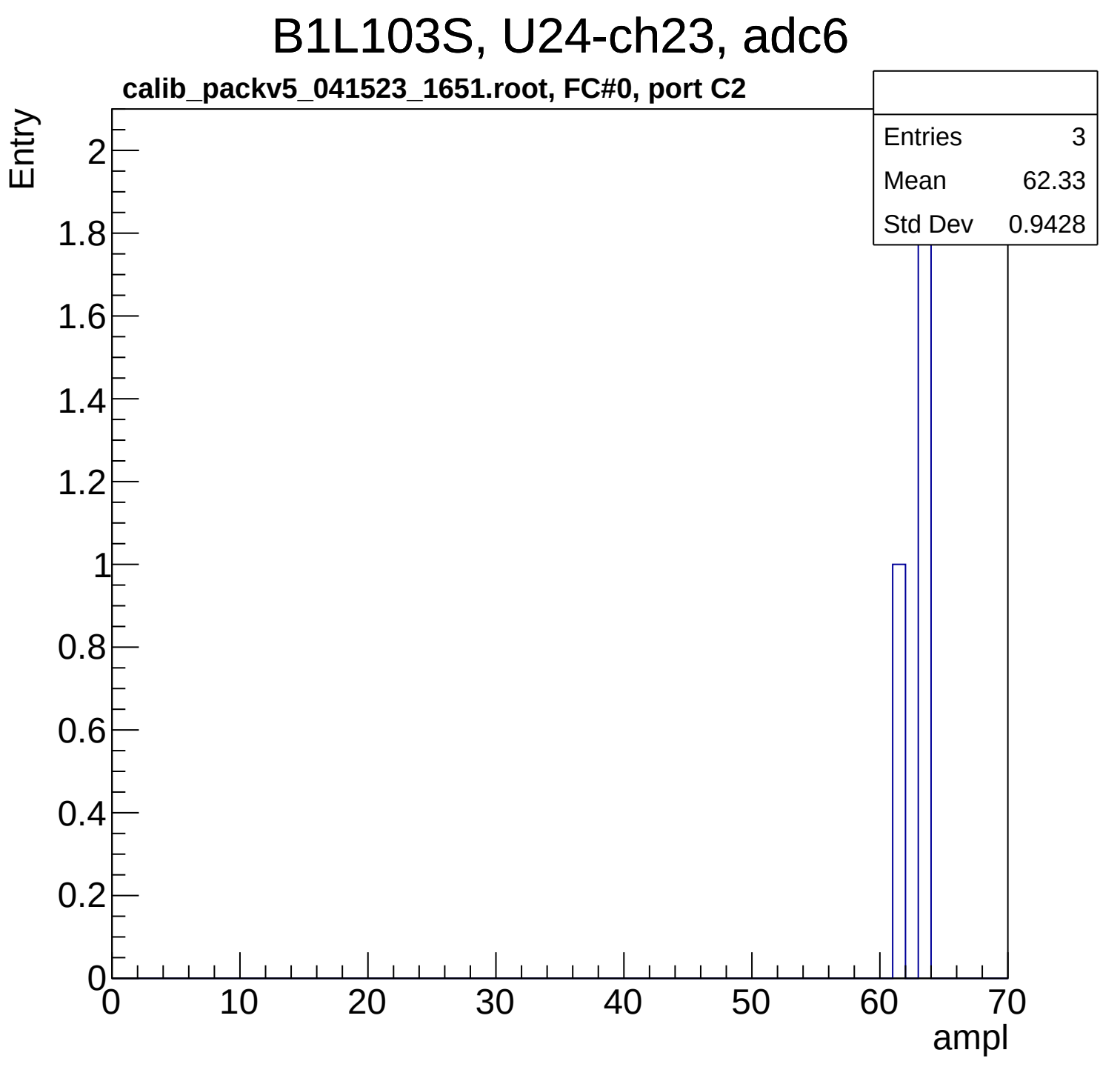
70
ampl


B1L103S, U24-ch23, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 3
Mean 62.33
Std Dev 0.9428
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
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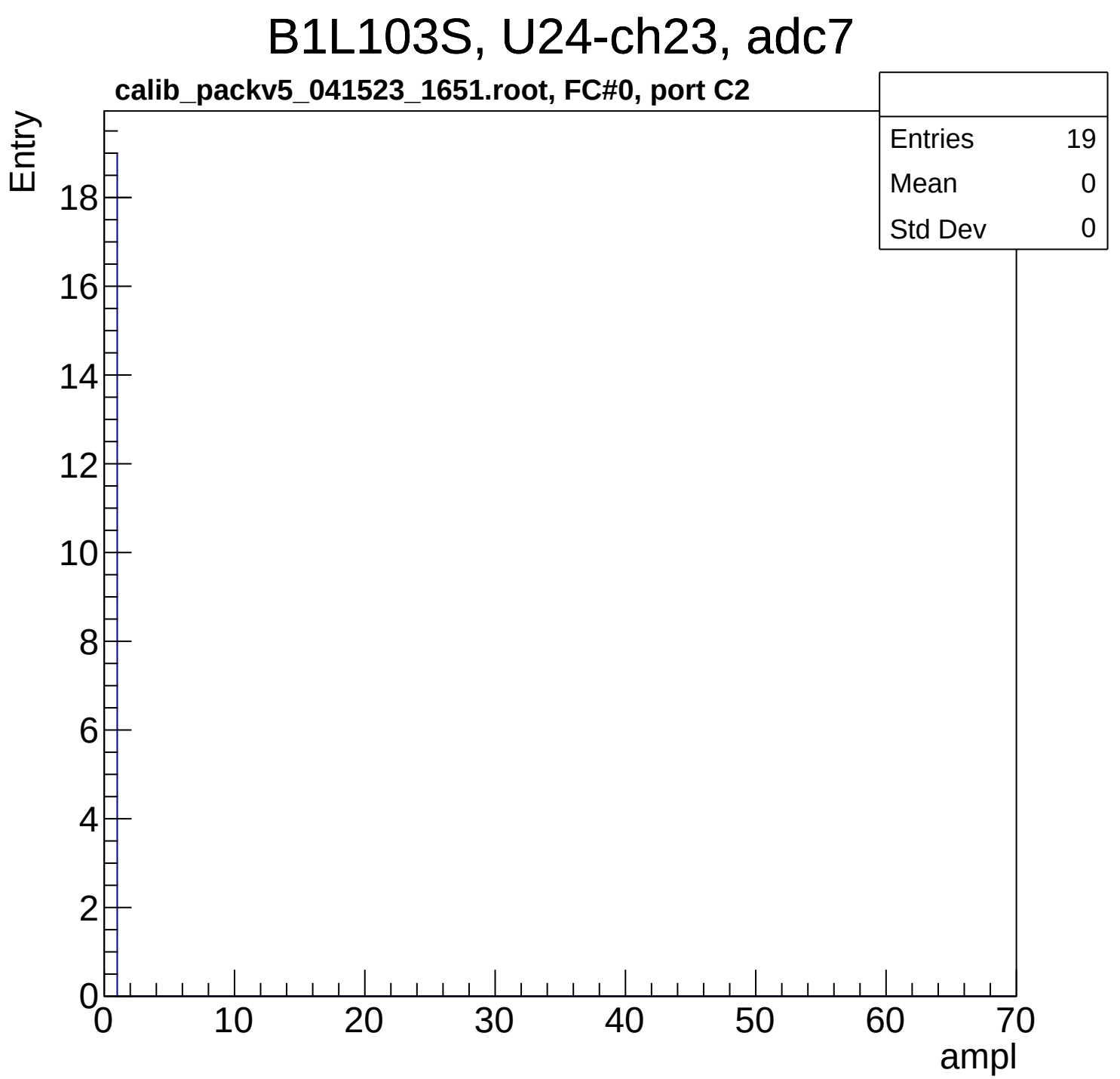
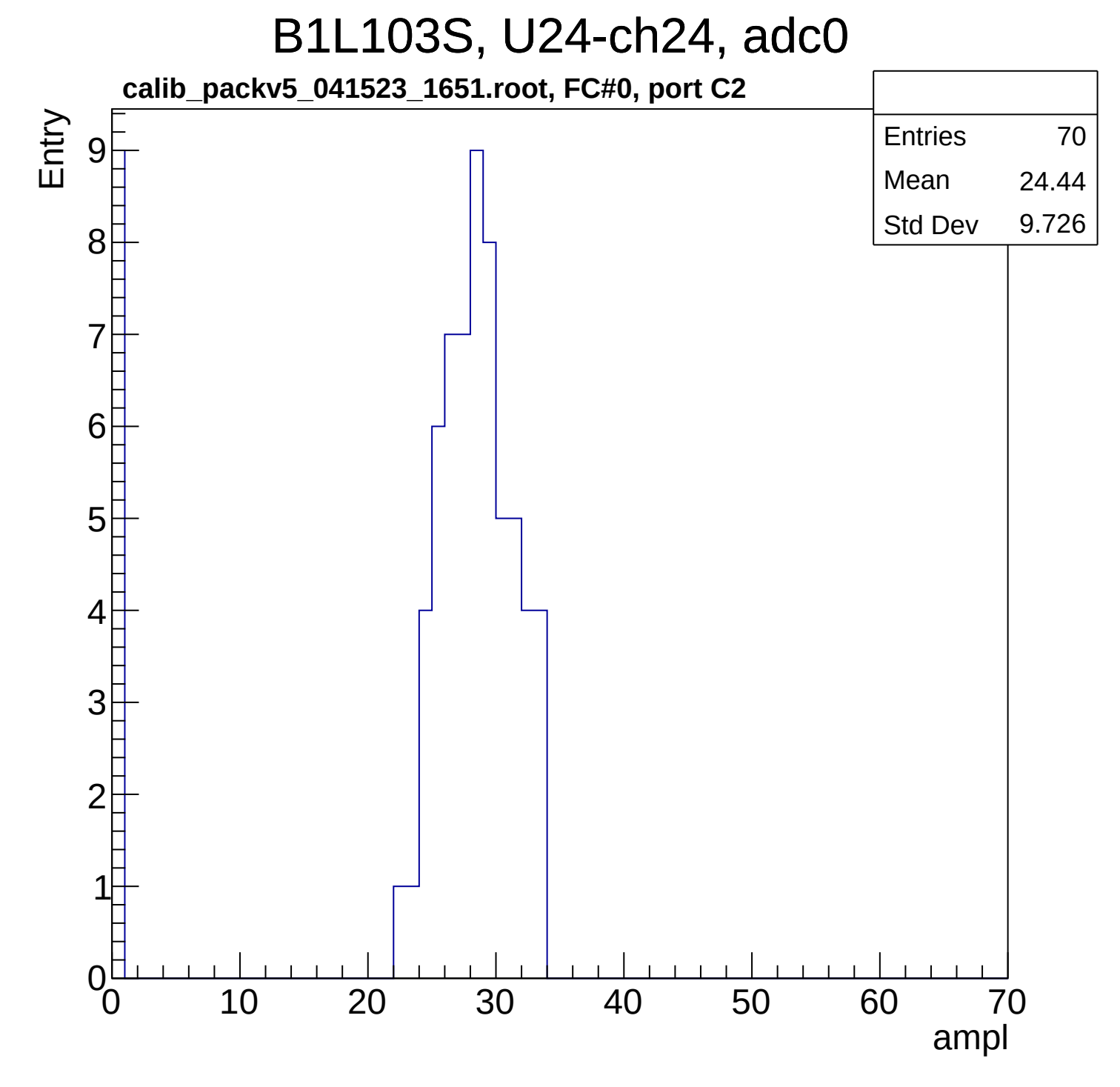

B1L103S, U24-ch23, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch24, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 24.44
Std Dev 9.726
Entry
ampl
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2
3
4
5
6
7
8
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0
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40
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60
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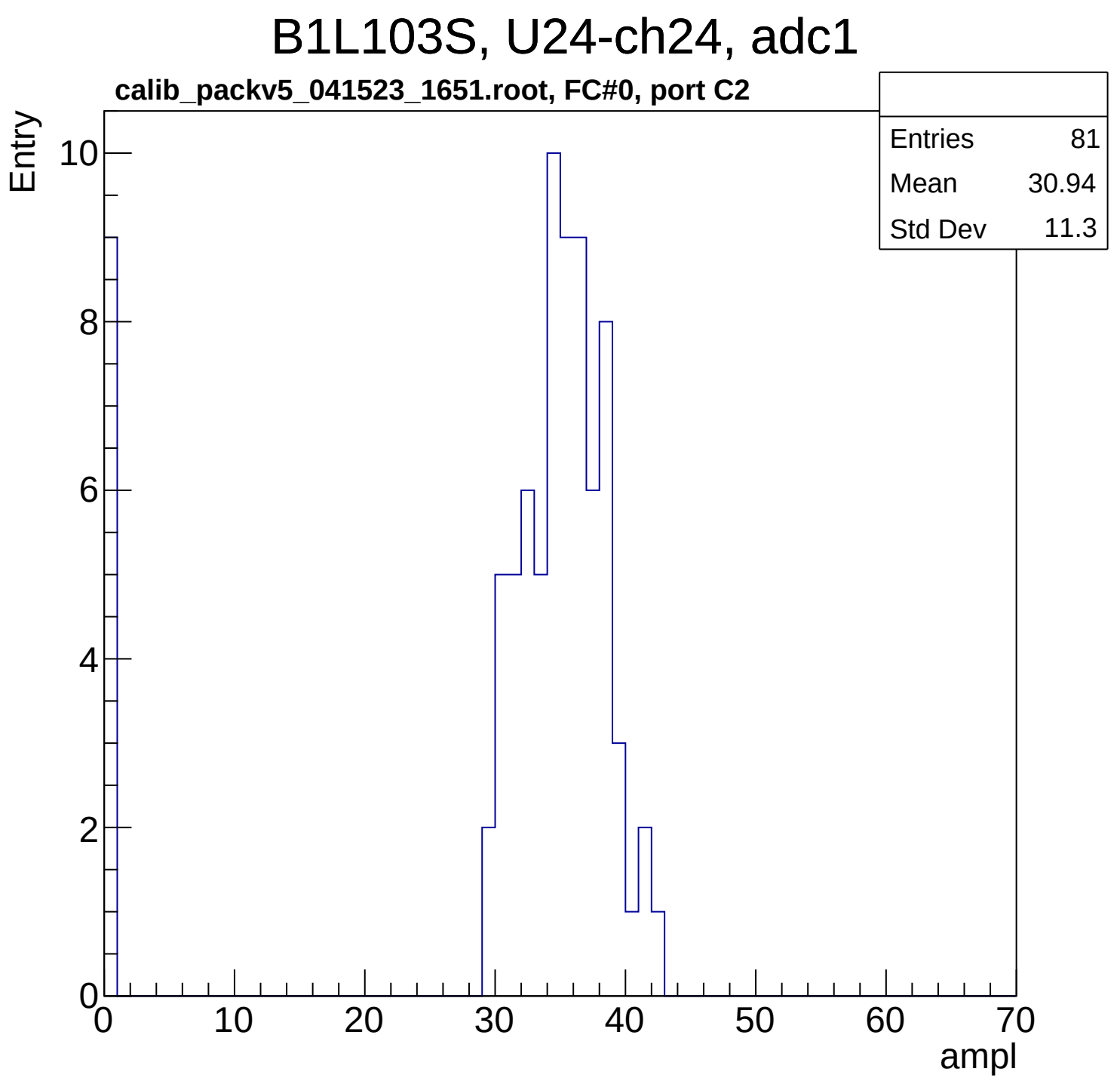
B1L103S, U24-ch24, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 30.94
Std Dev 11.3
Entry
ampl
0
2
4
6
8
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0
10
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30
40
50
60
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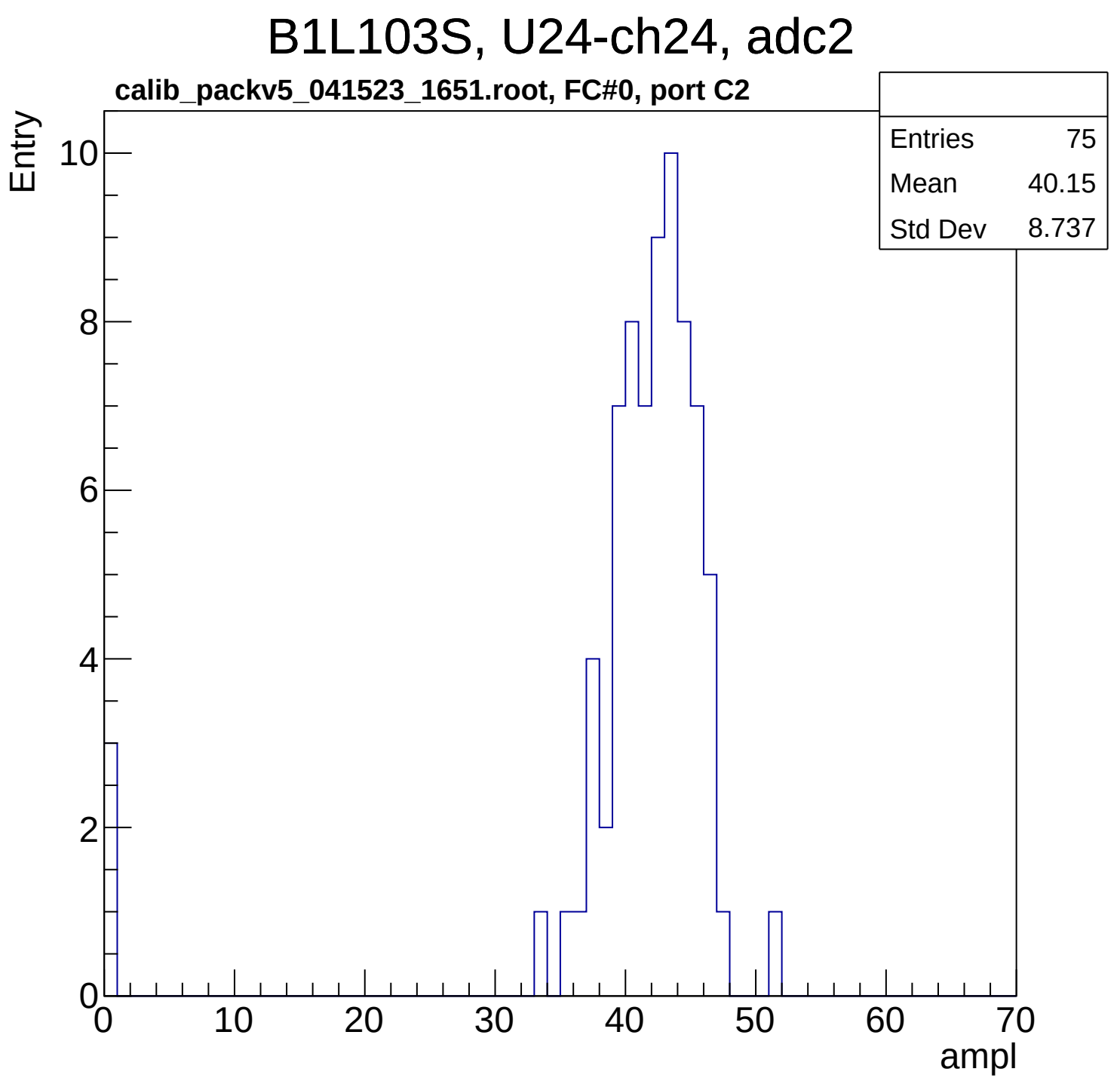
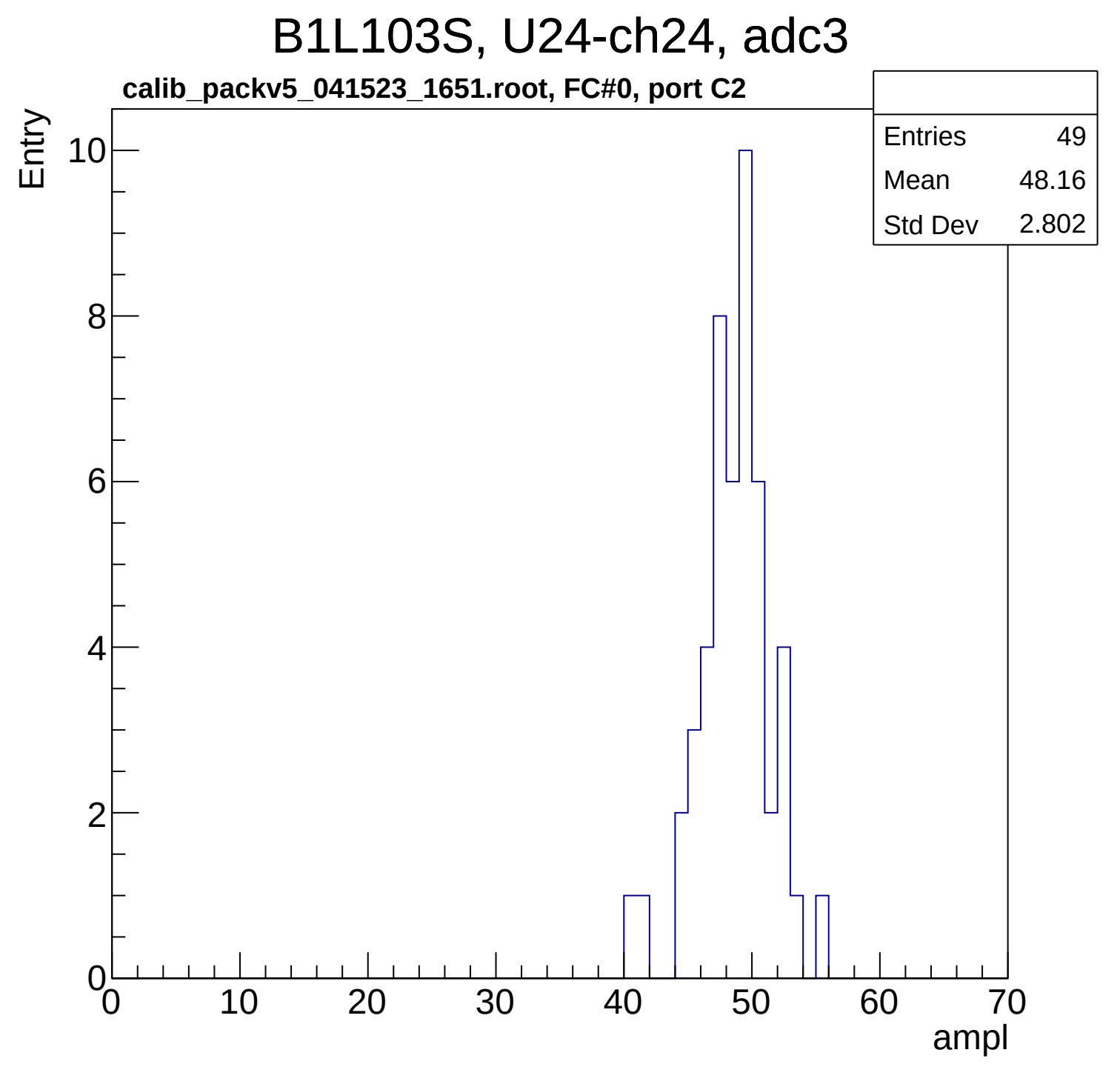
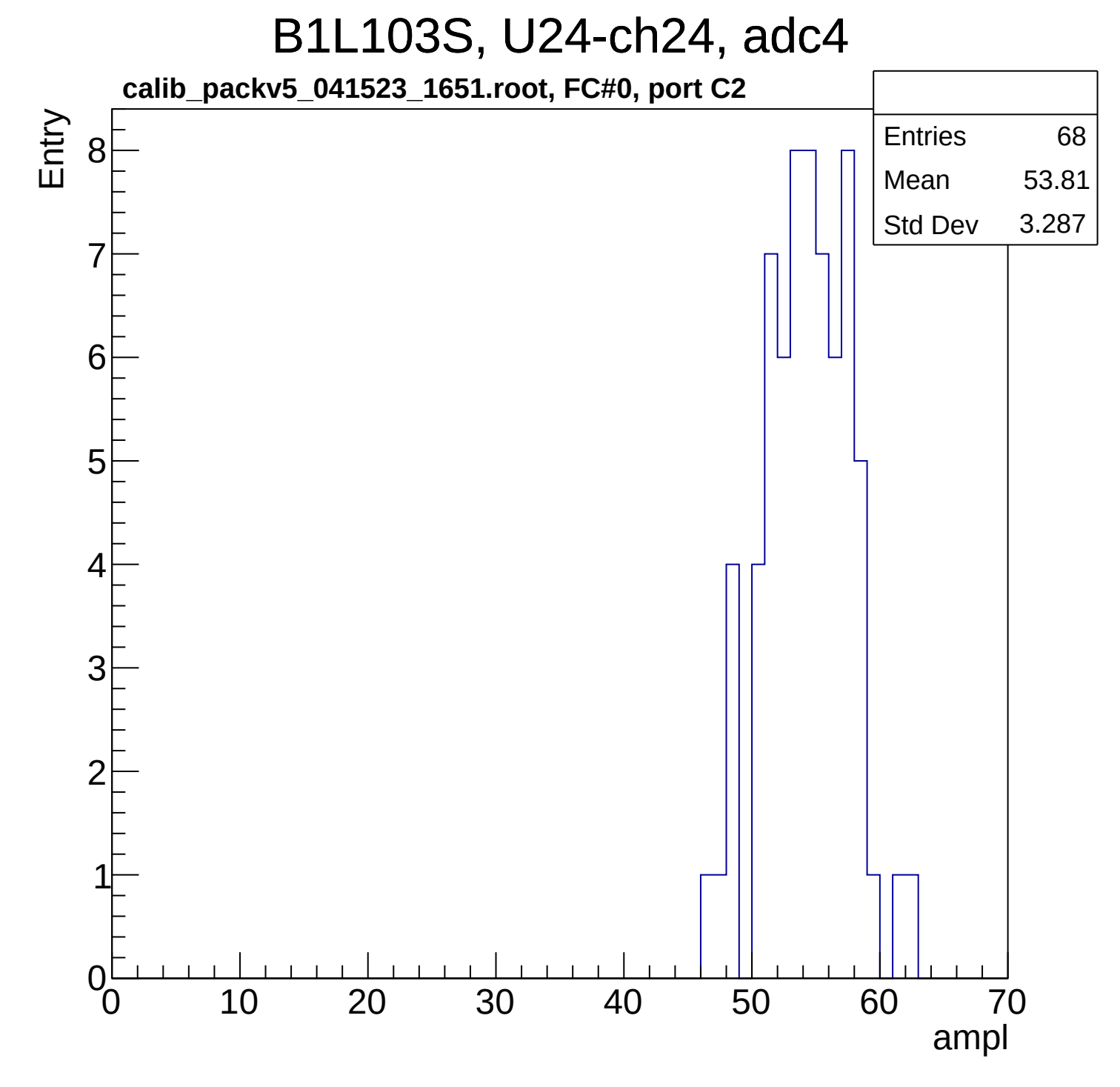

B1L103S, U24-ch24, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 40.15
Std Dev 8.737
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch24, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 48.16
Std Dev 2.802
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U24-ch24, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 53.81
Std Dev 3.287
Entry
ampl
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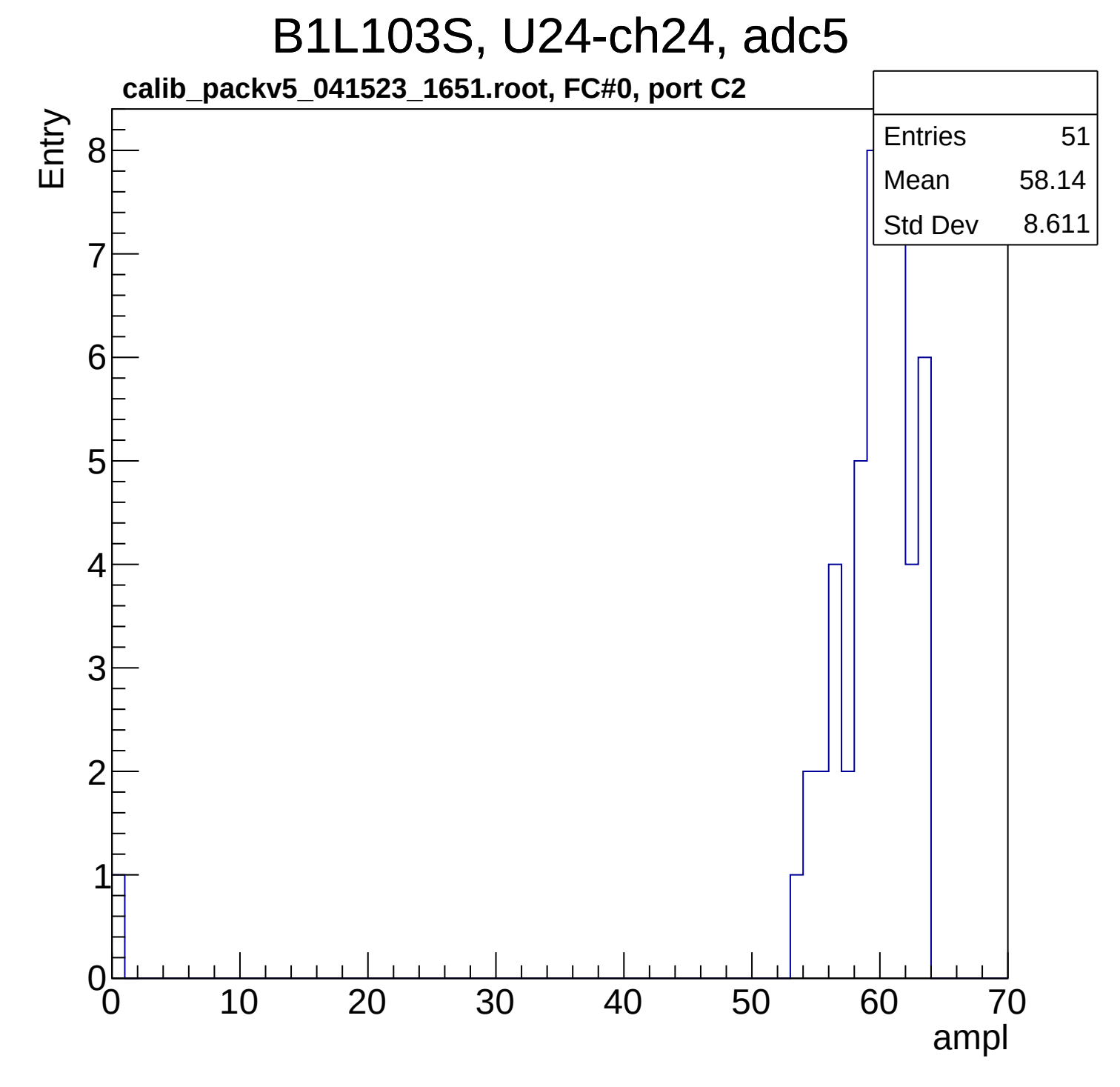
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U24-ch24, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 58.14
Std Dev 8.611
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
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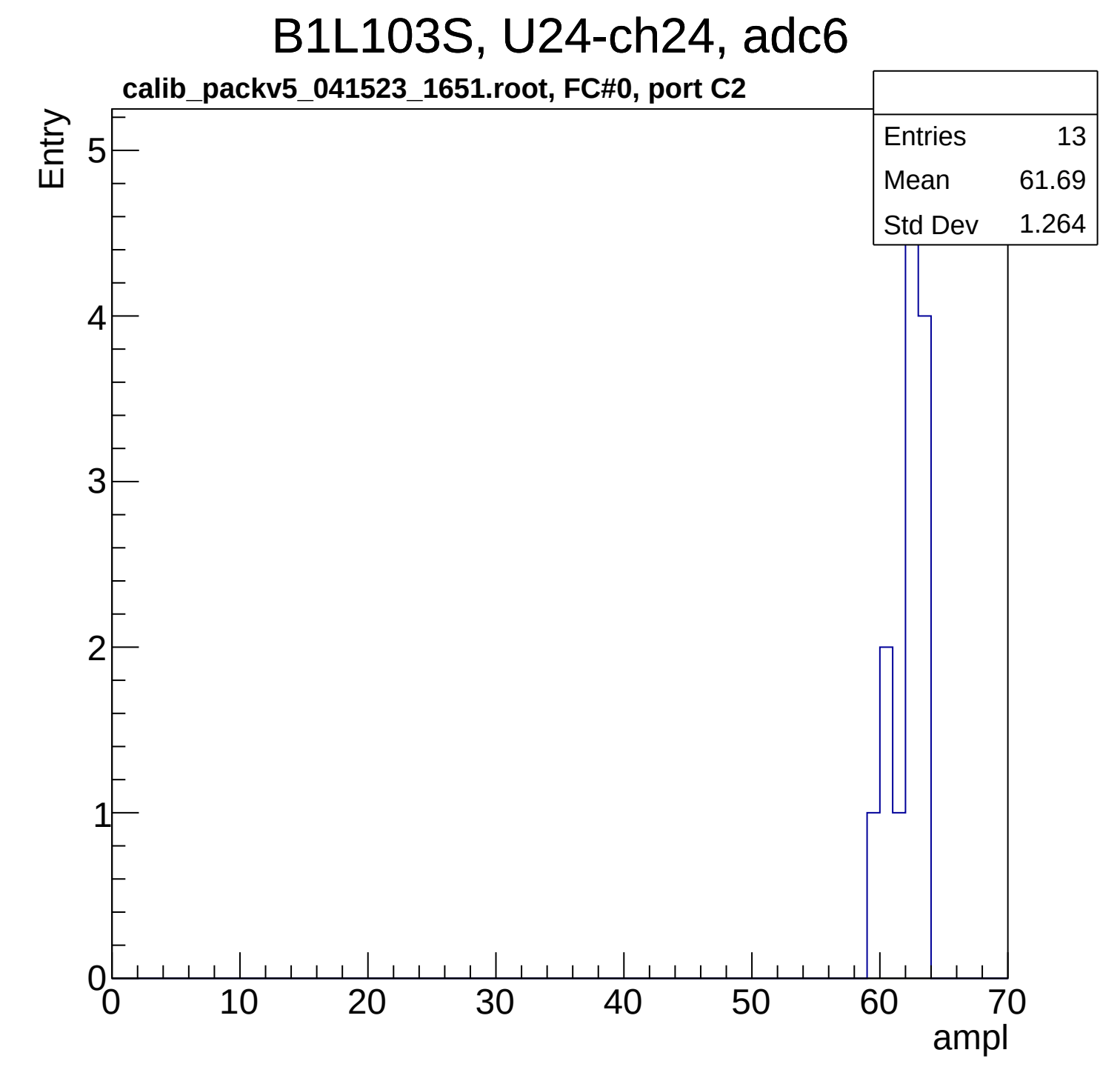
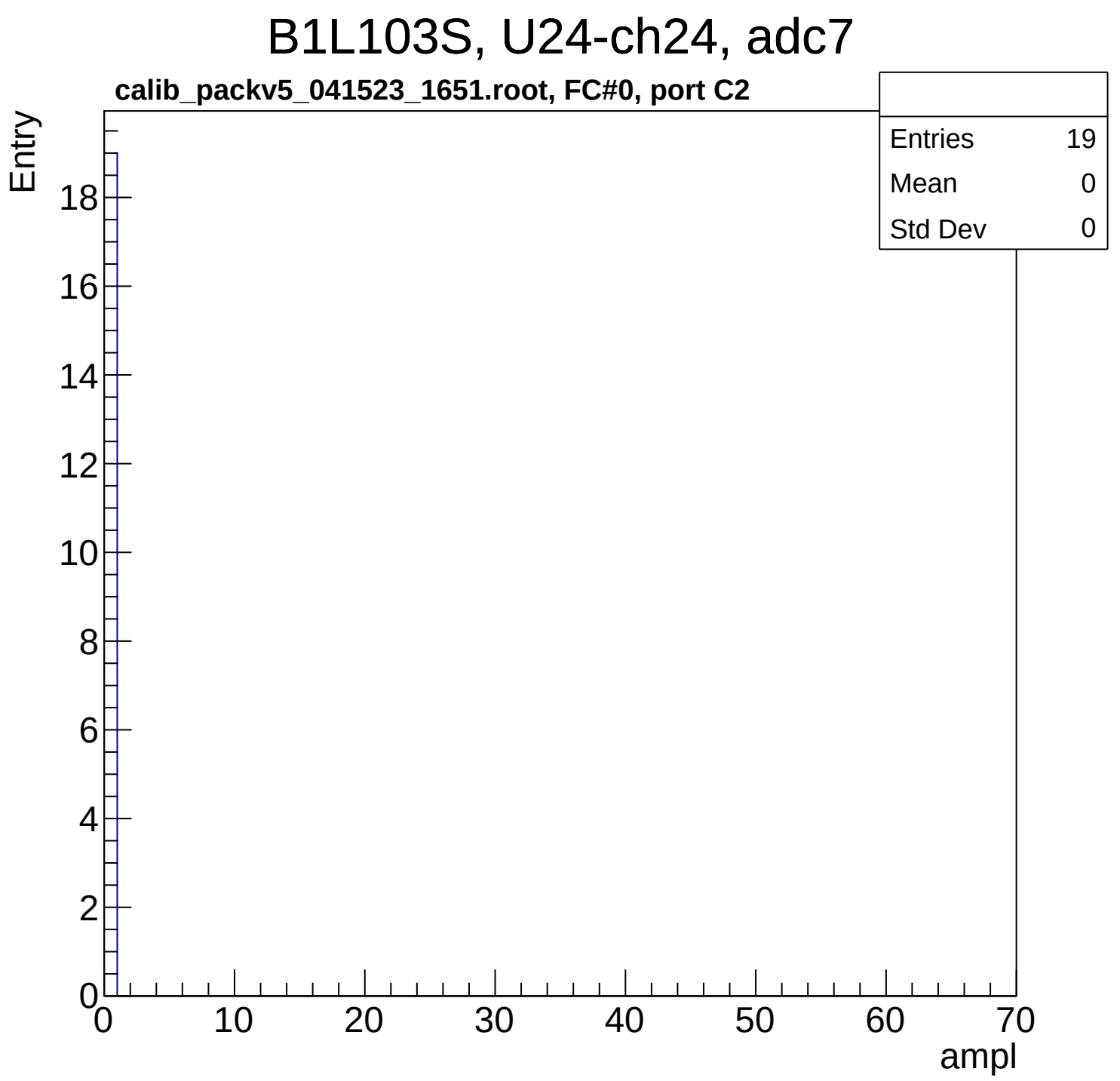
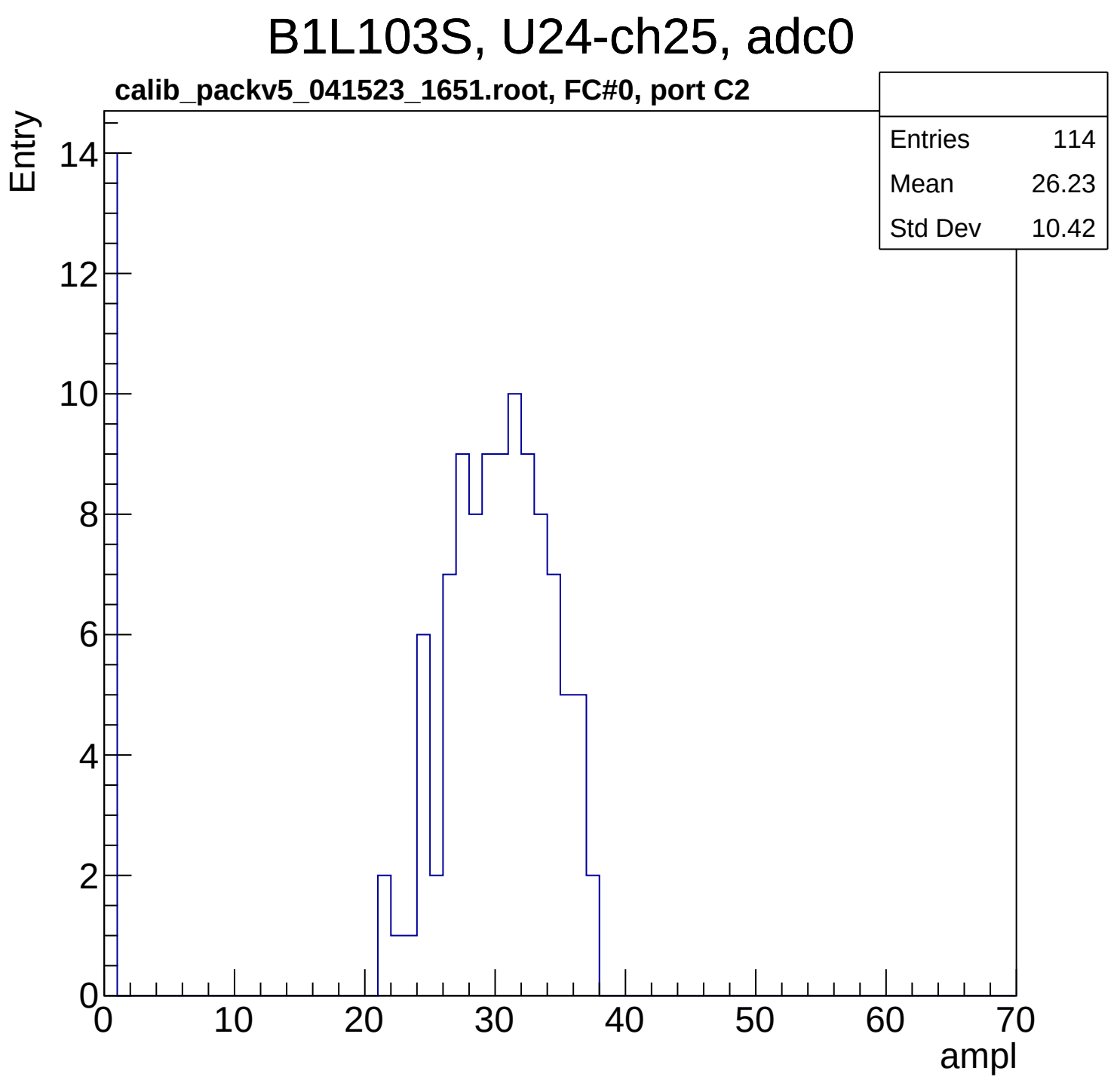
60
70


B1L103S, U24-ch24, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 13
Mean 61.69
Std Dev 1.264
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U24-ch24, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch25, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 114
Mean 26.23
Std Dev 10.42
Entry
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4
6
8
10
12
14
0
10
20
30
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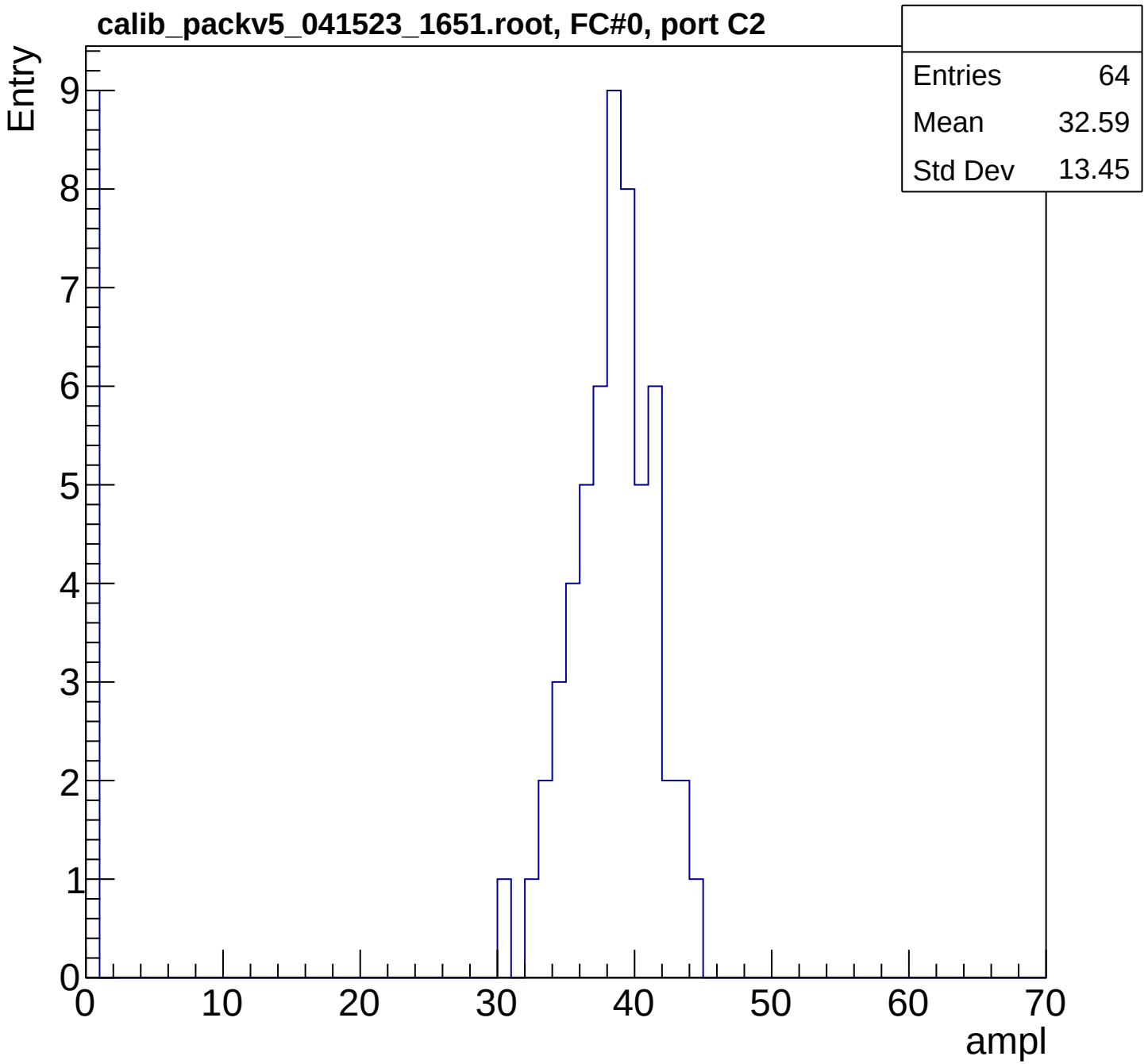
50
60
70
ampl


B1L103S, U24-ch25, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 32.59
Std Dev 13.45
Entry
ampl
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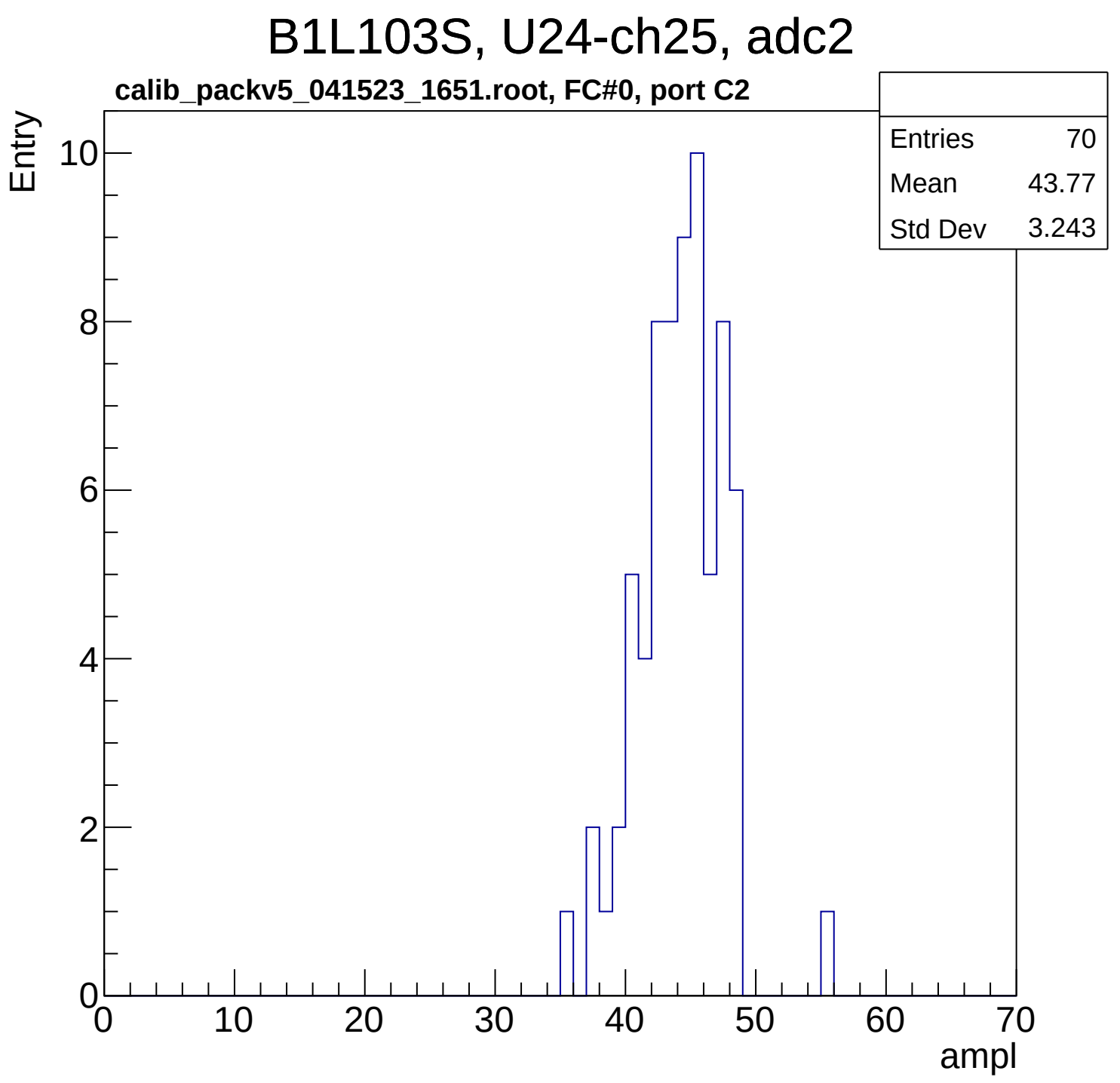
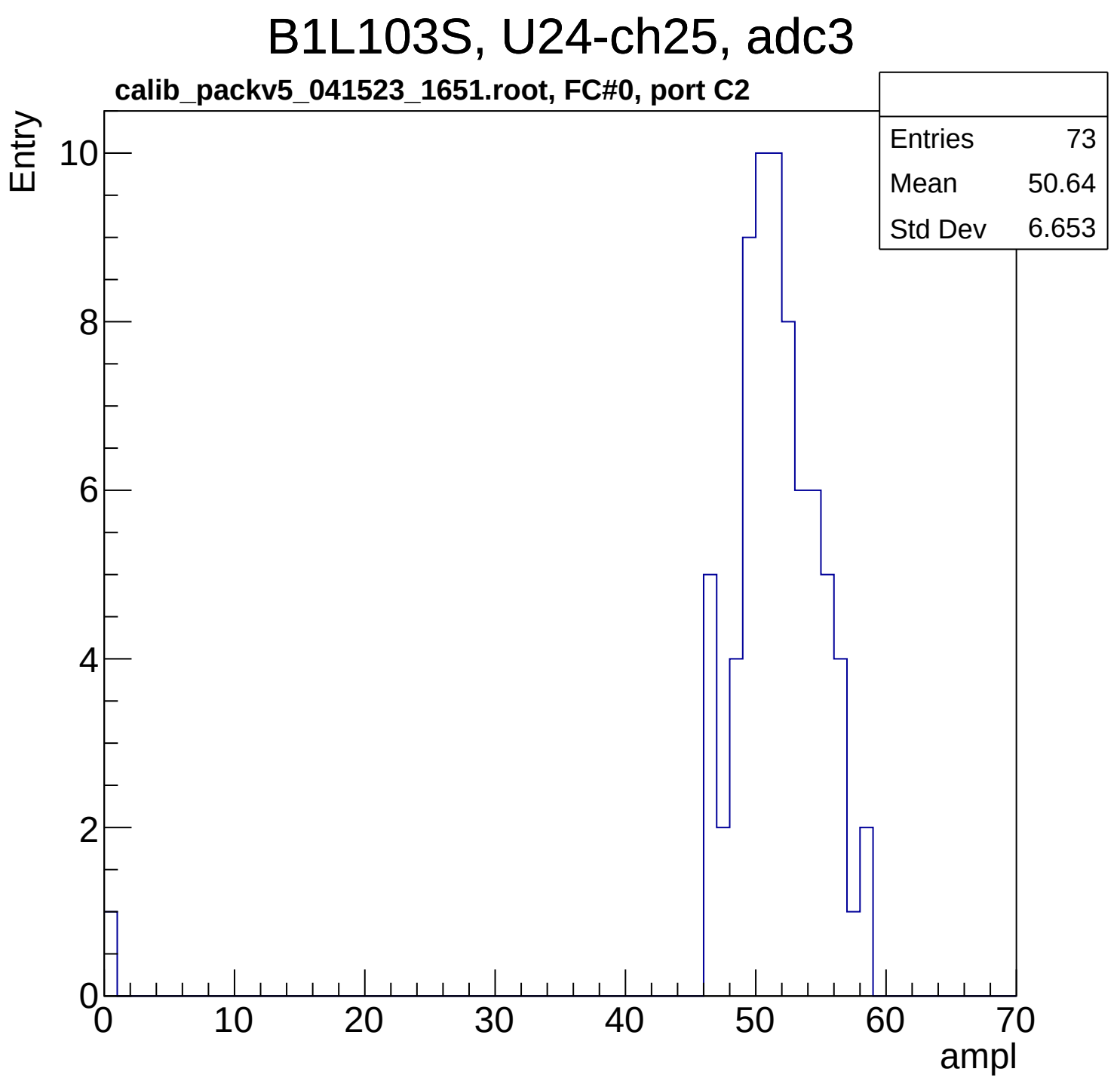
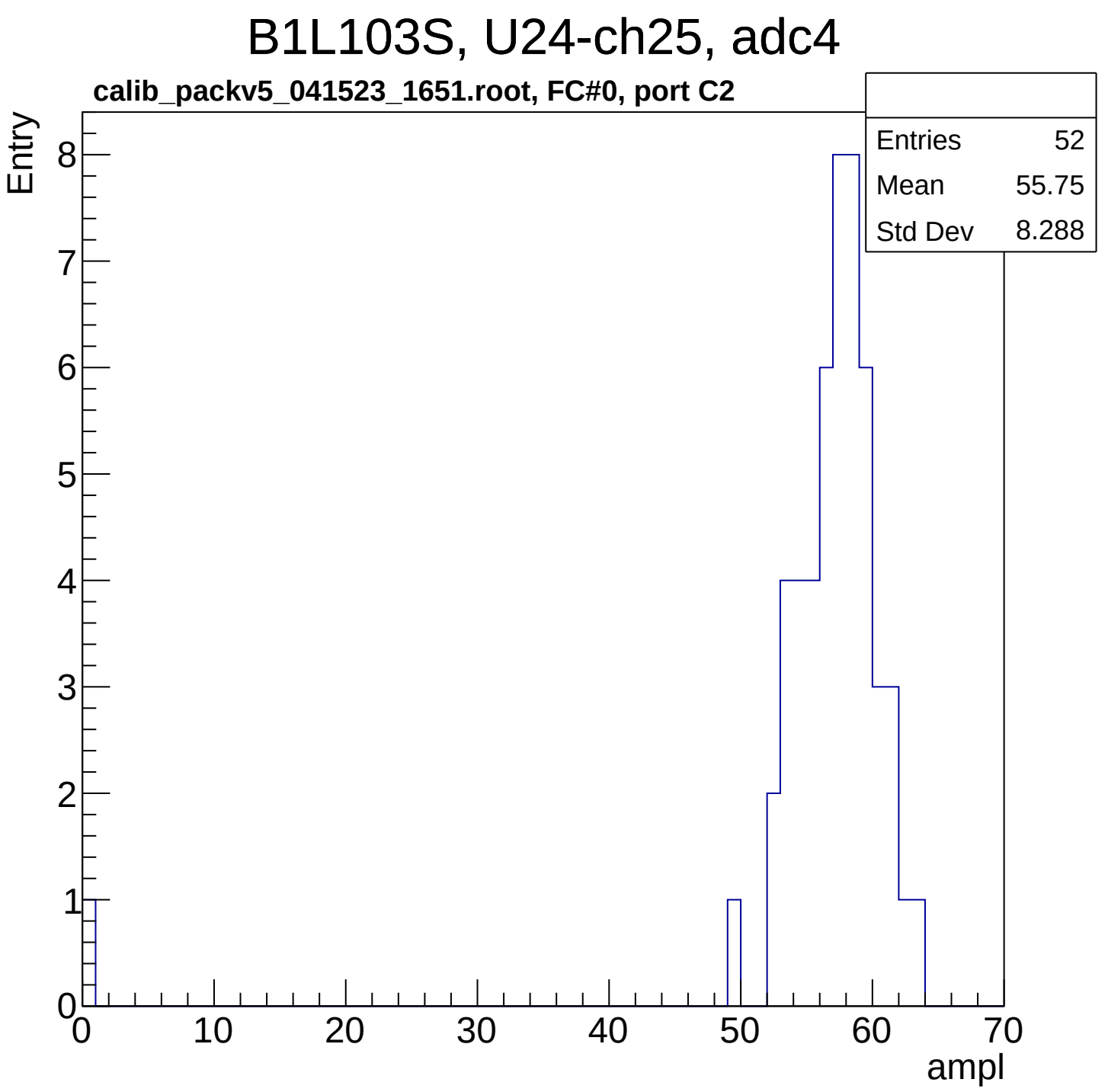
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U24-ch25, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 43.77
Std Dev 3.243
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U24-ch25, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 50.64
Std Dev 6.653
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch25, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 55.75
Std Dev 8.288
Entry
ampl
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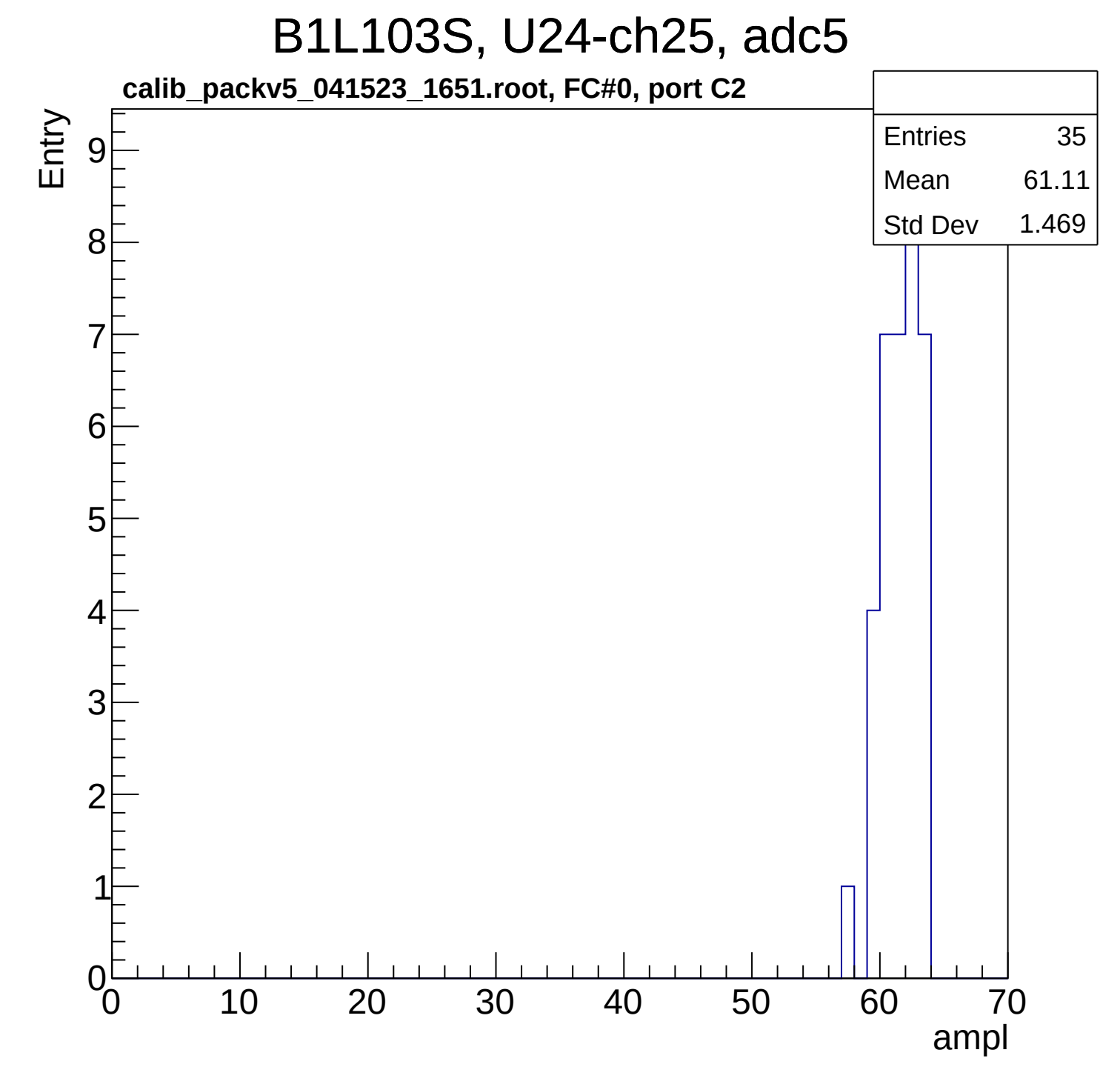
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U24-ch25, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 35
Mean 61.11
Std Dev 1.469
Entry
ampl
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3
4
5
6
7
8
9
0
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20
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60
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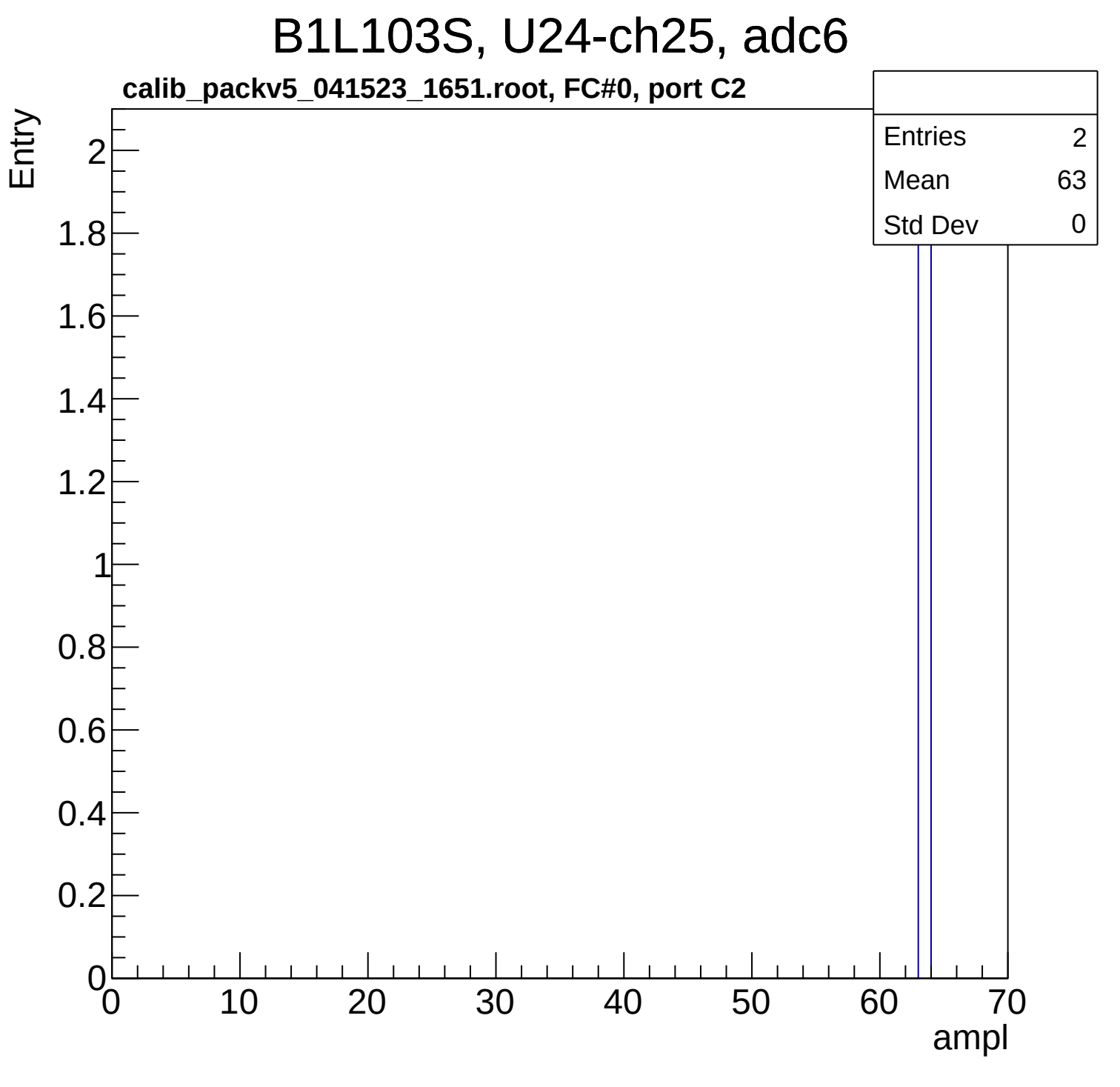
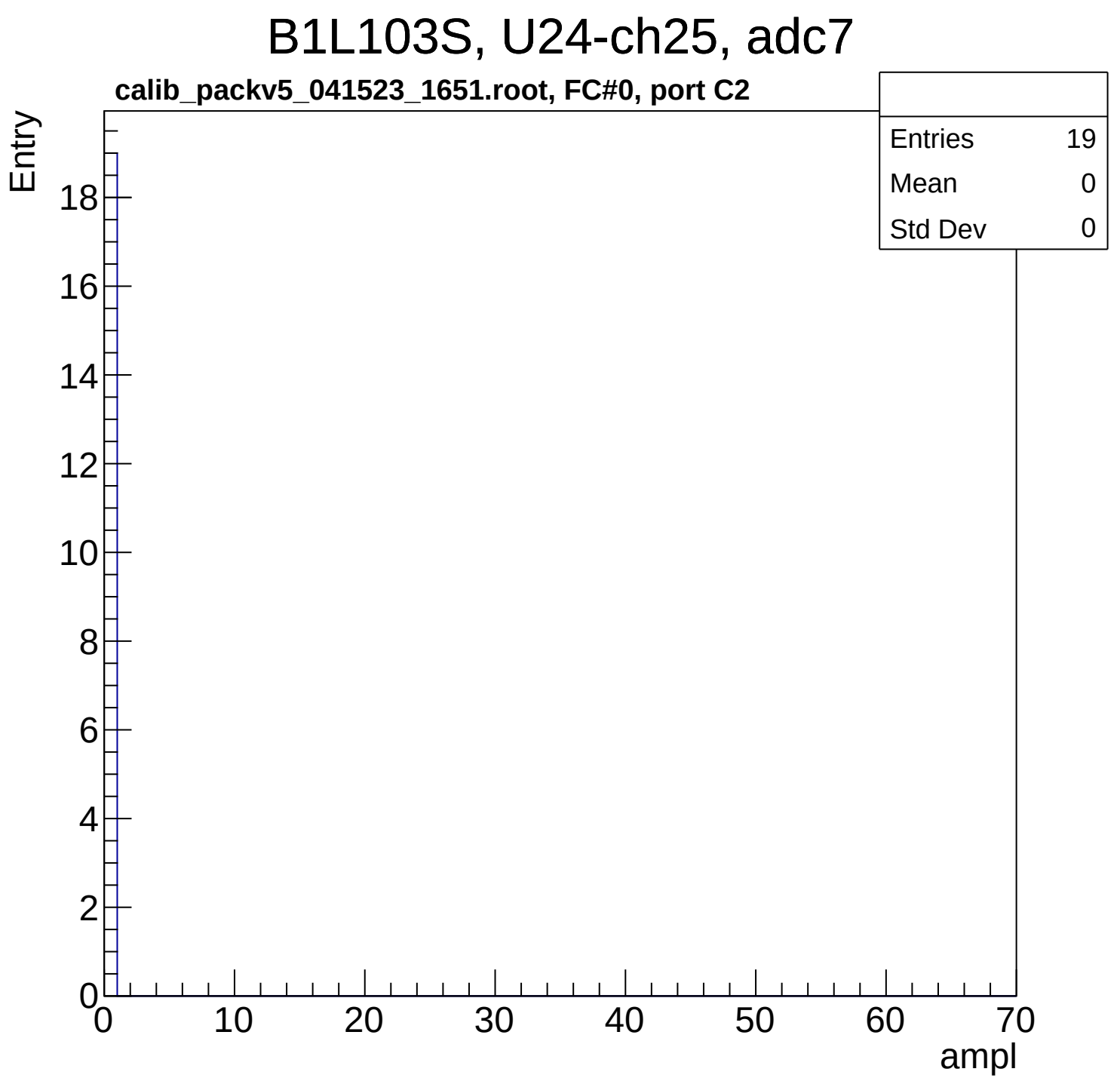
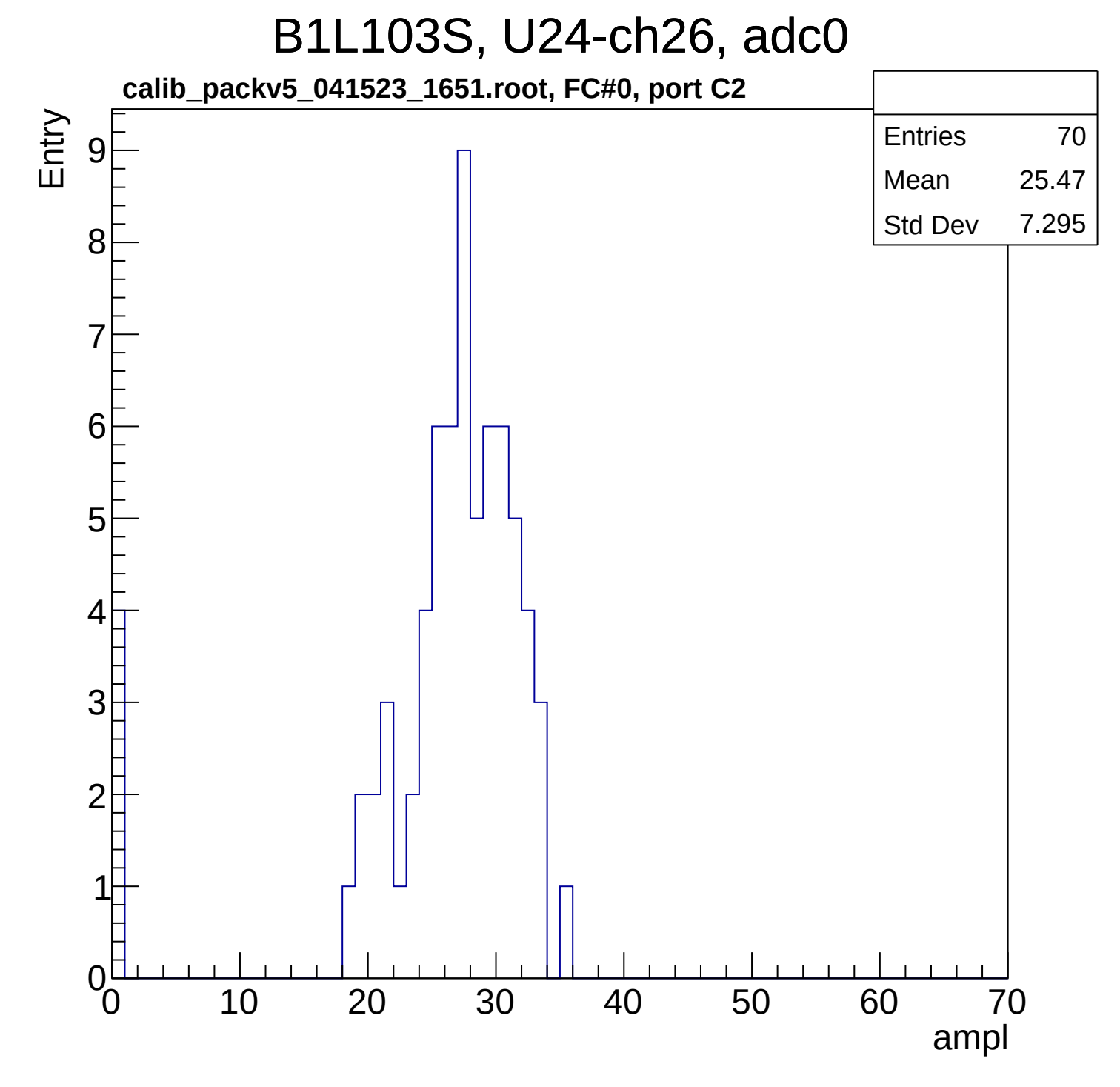

B1L103S, U24-ch25, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 2
Mean 63
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U24-ch25, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch26, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 25.47
Std Dev 7.295
Entry
ampl
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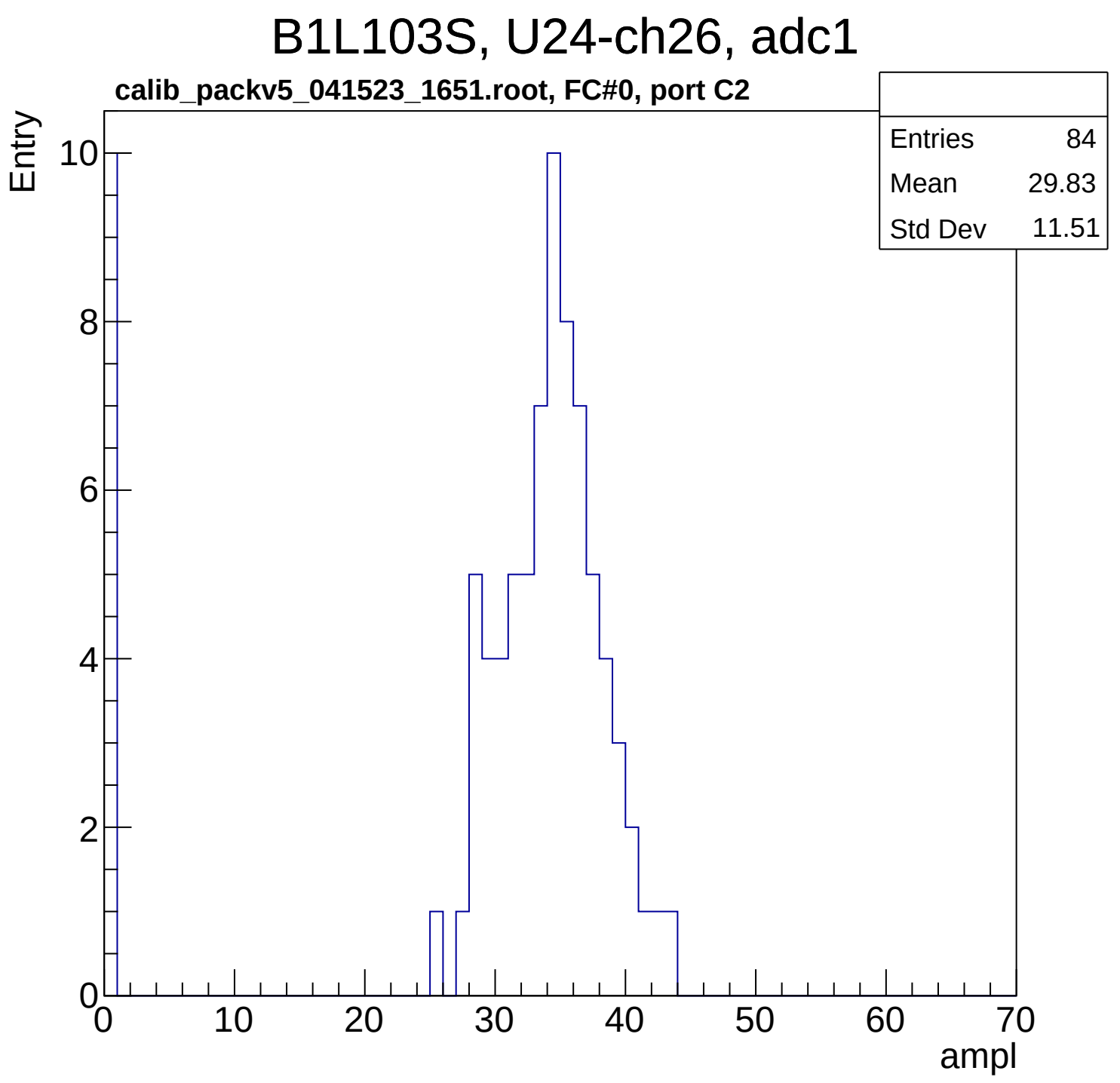
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U24-ch26, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 29.83
Std Dev 11.51
Entry
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4
6
8
10
0
10
20
30
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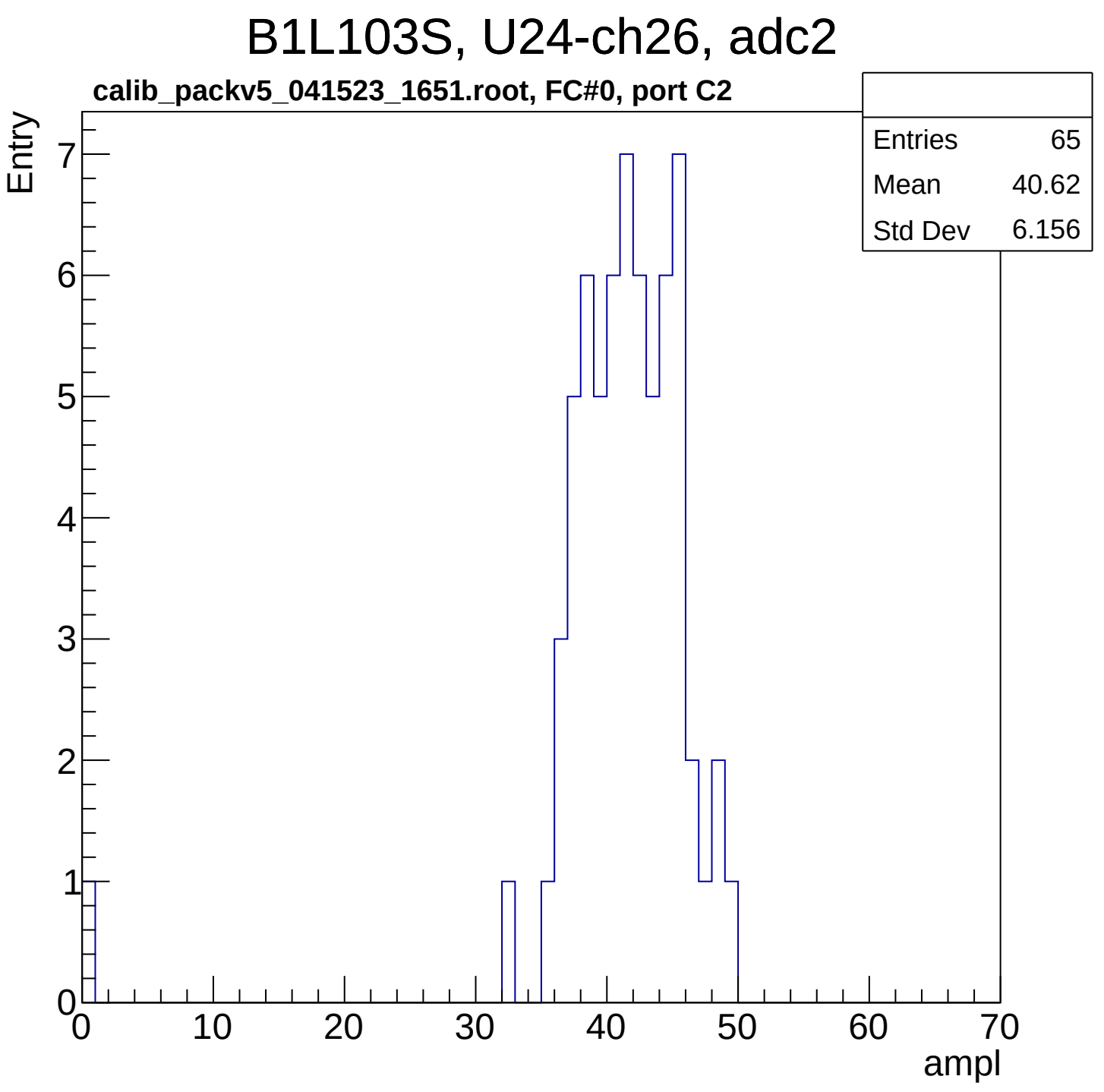
50
60
70
ampl


B1L103S, U24-ch26, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 40.62
Std Dev 6.156
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
30
40
50
60
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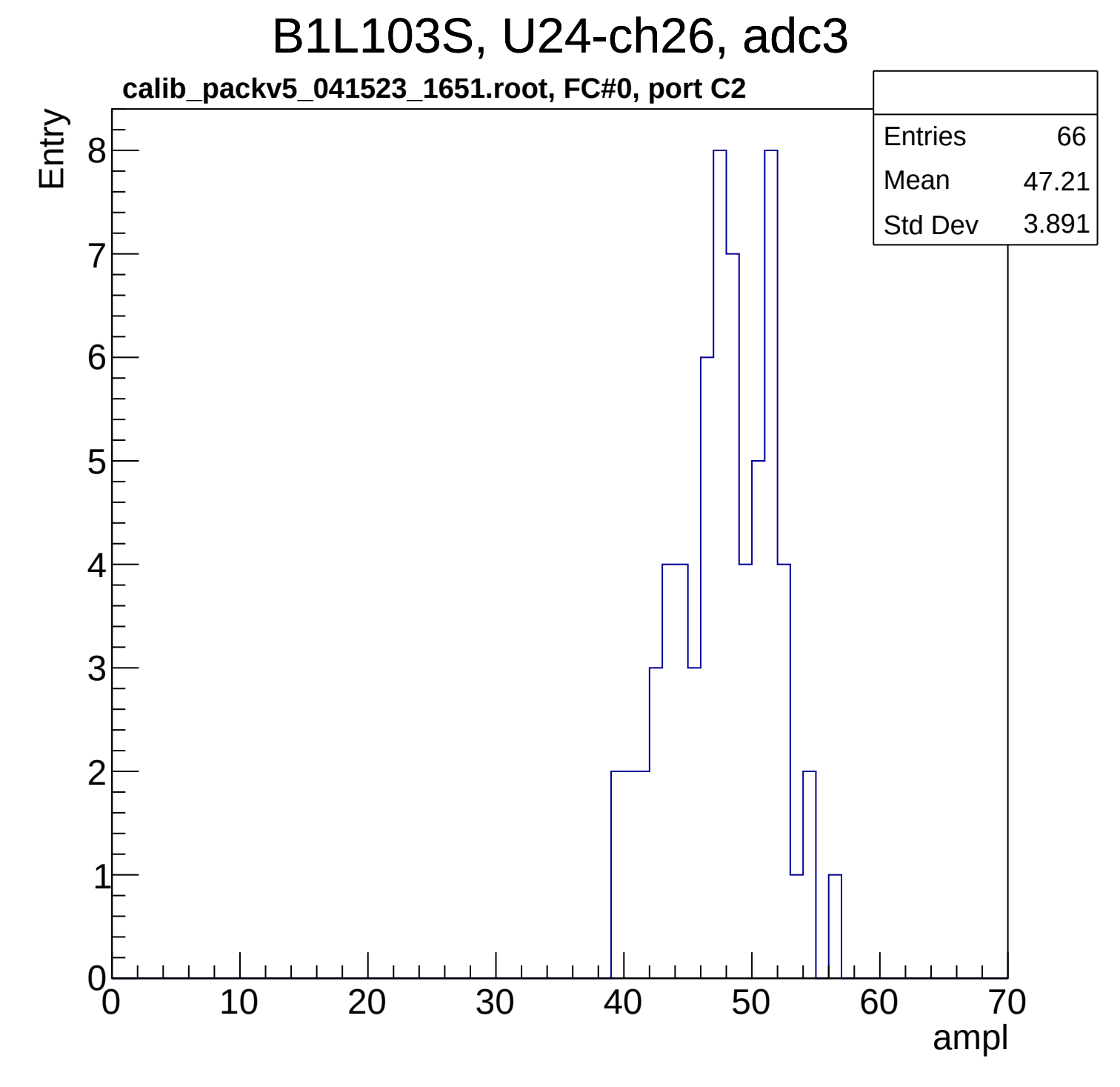
B1L103S, U24-ch26, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 47.21
Std Dev 3.891
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
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40
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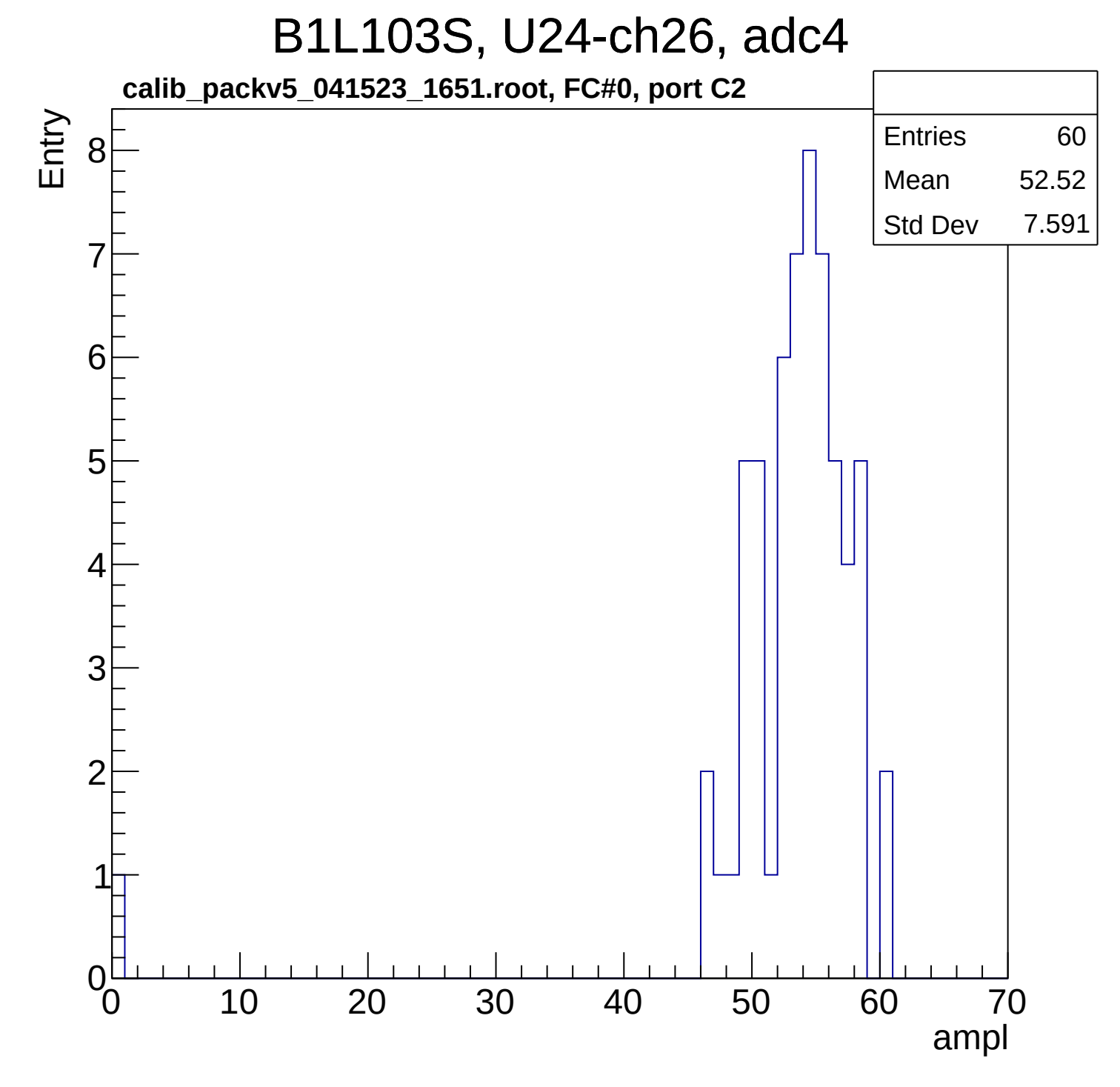
60
70


B1L103S, U24-ch26, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 52.52
Std Dev 7.591
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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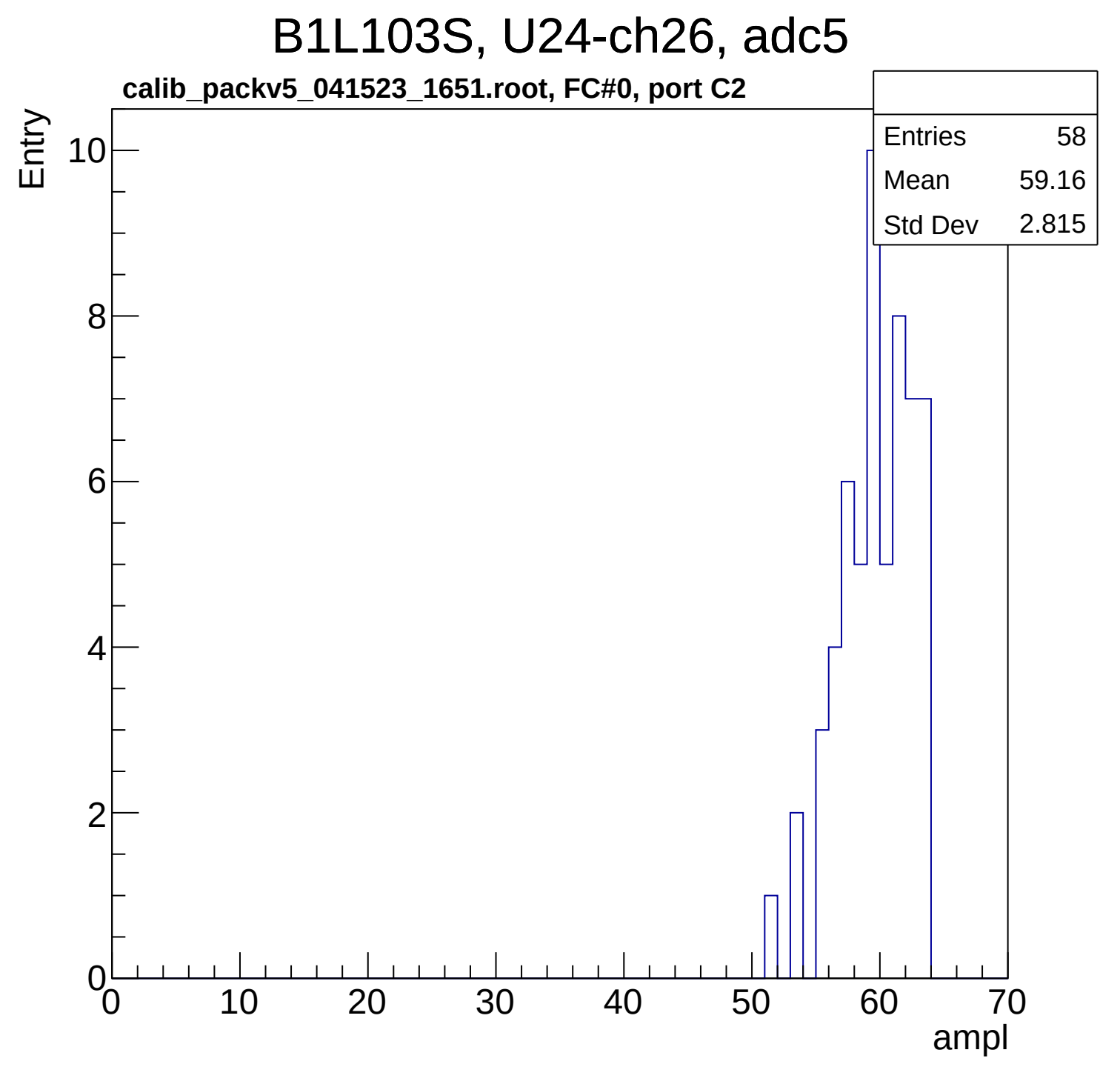
B1L103S, U24-ch26, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 59.16
Std Dev 2.815
Entry
ampl
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4
6
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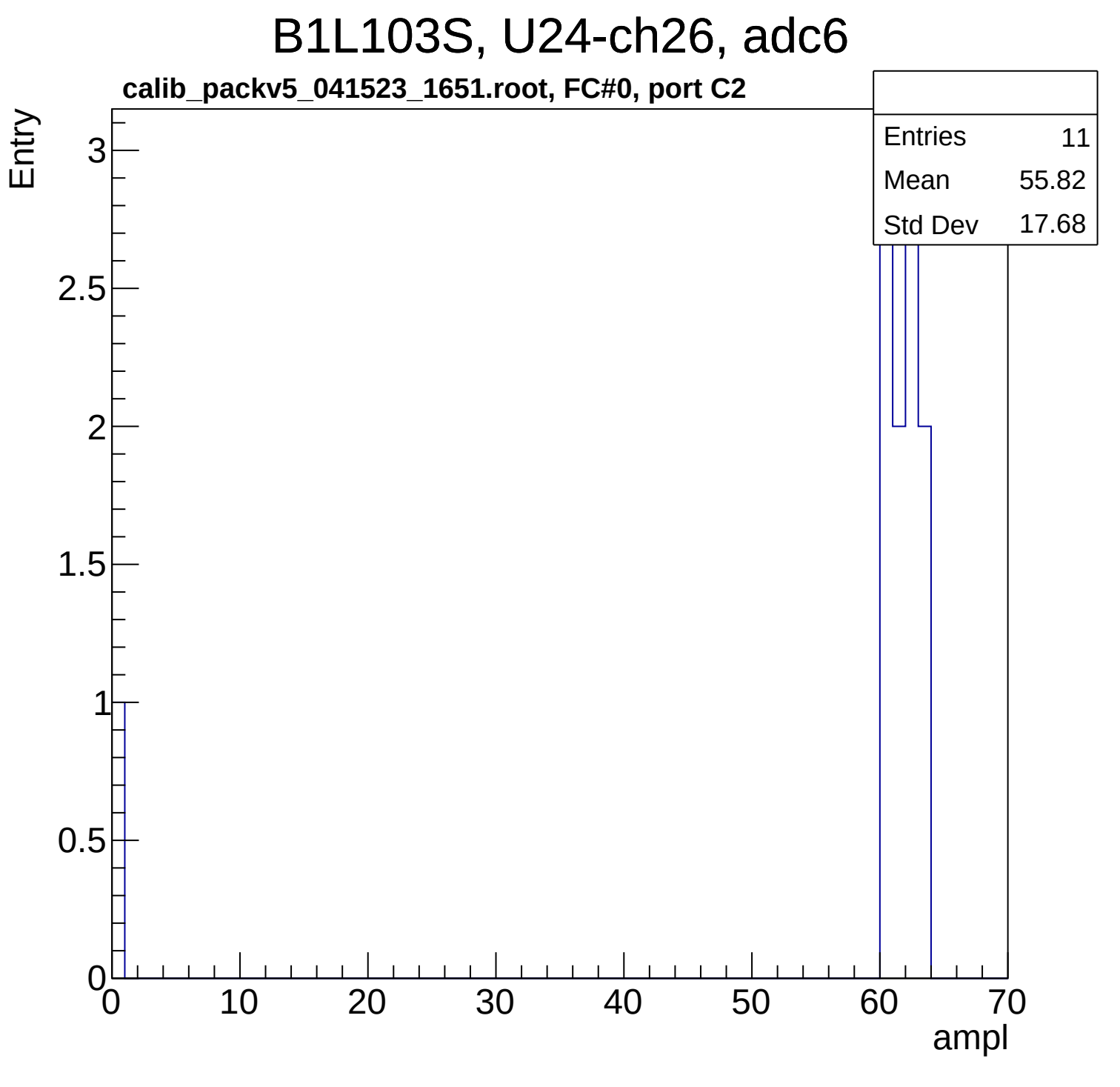
10
0
10
20
30
40
50
60
70


B1L103S, U24-ch26, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 55.82
Std Dev 17.68
Entry
ampl
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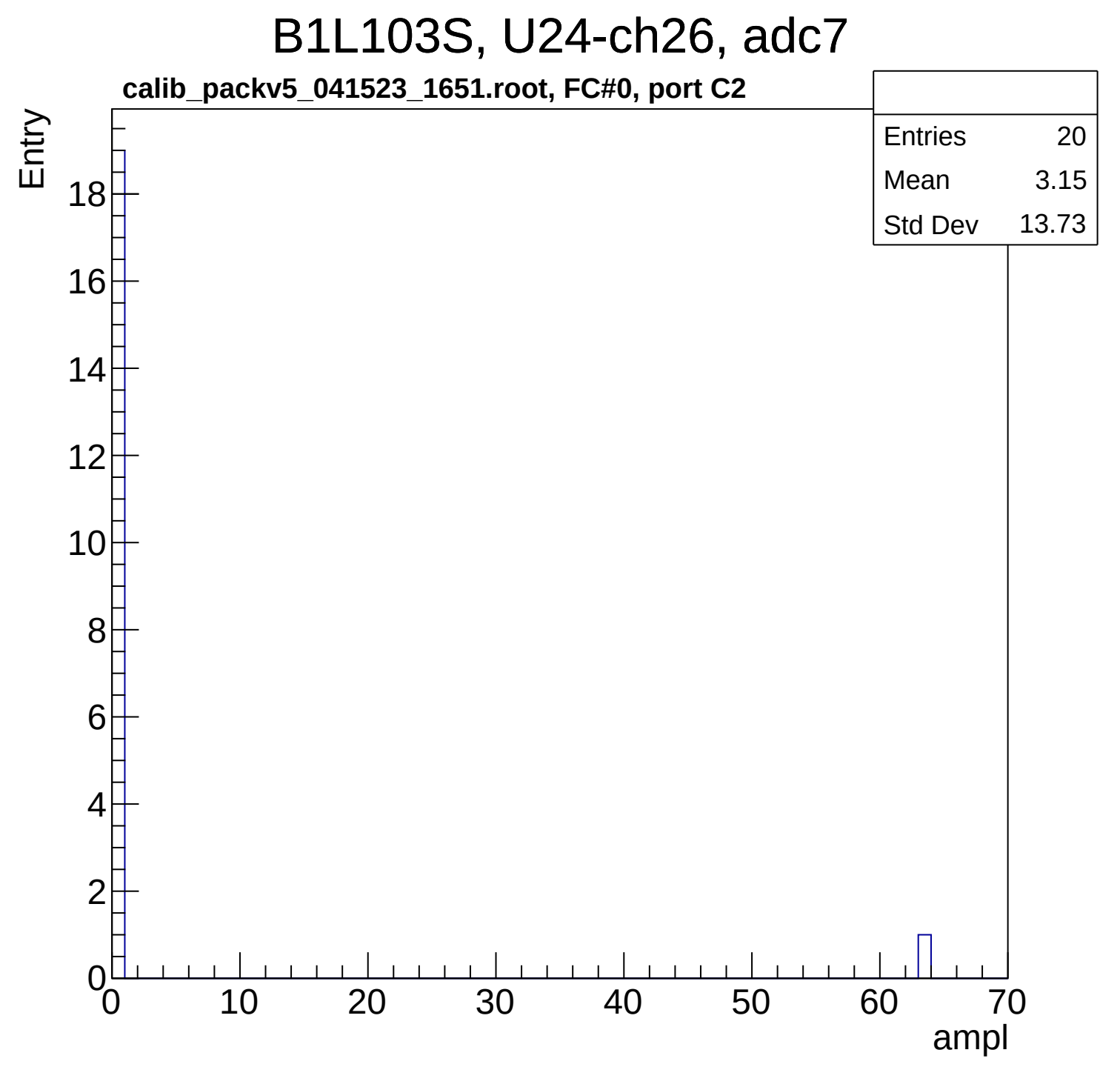
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U24-ch26, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
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6
8
10
12
14
16
18
0
10
20
30
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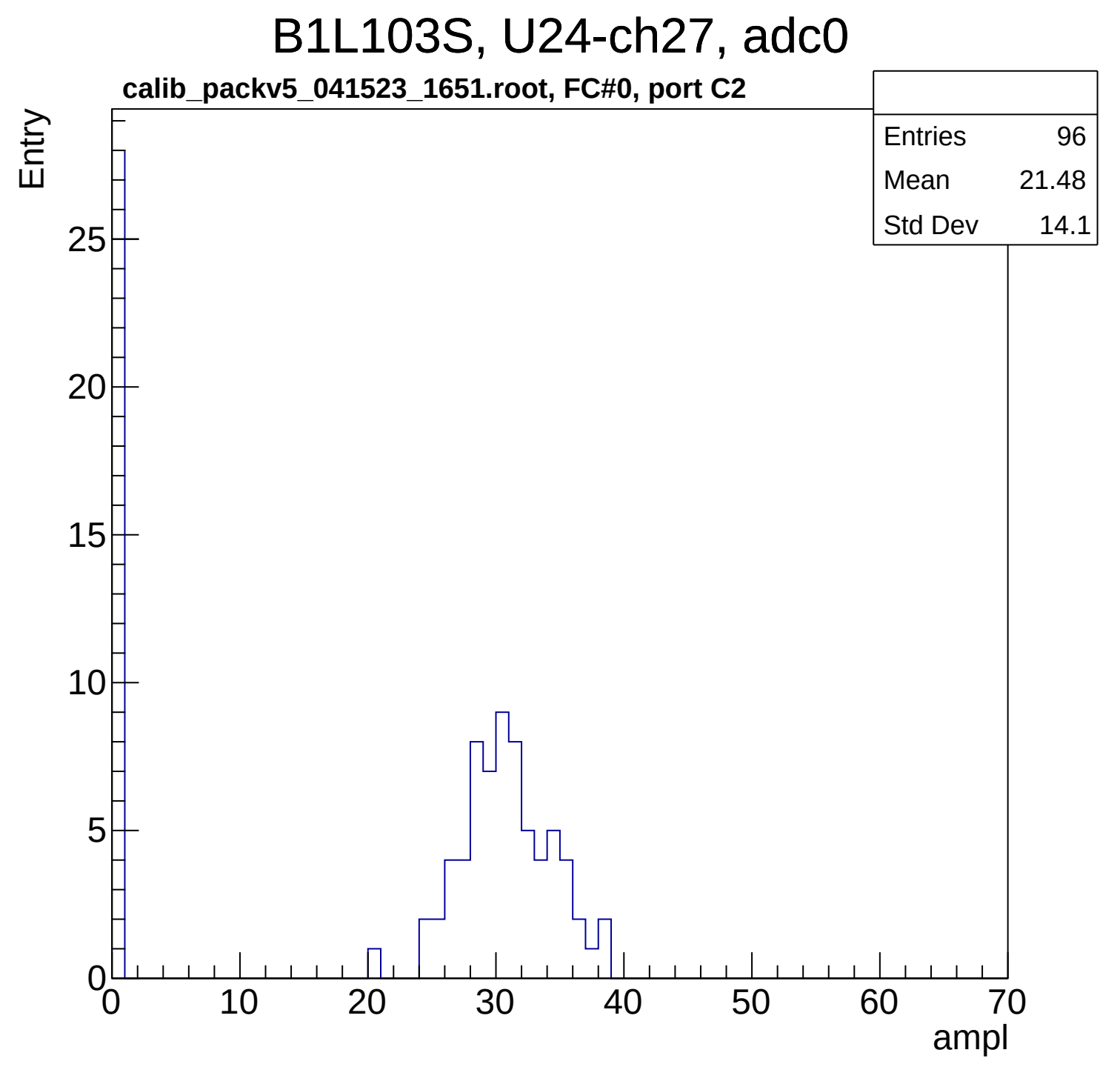
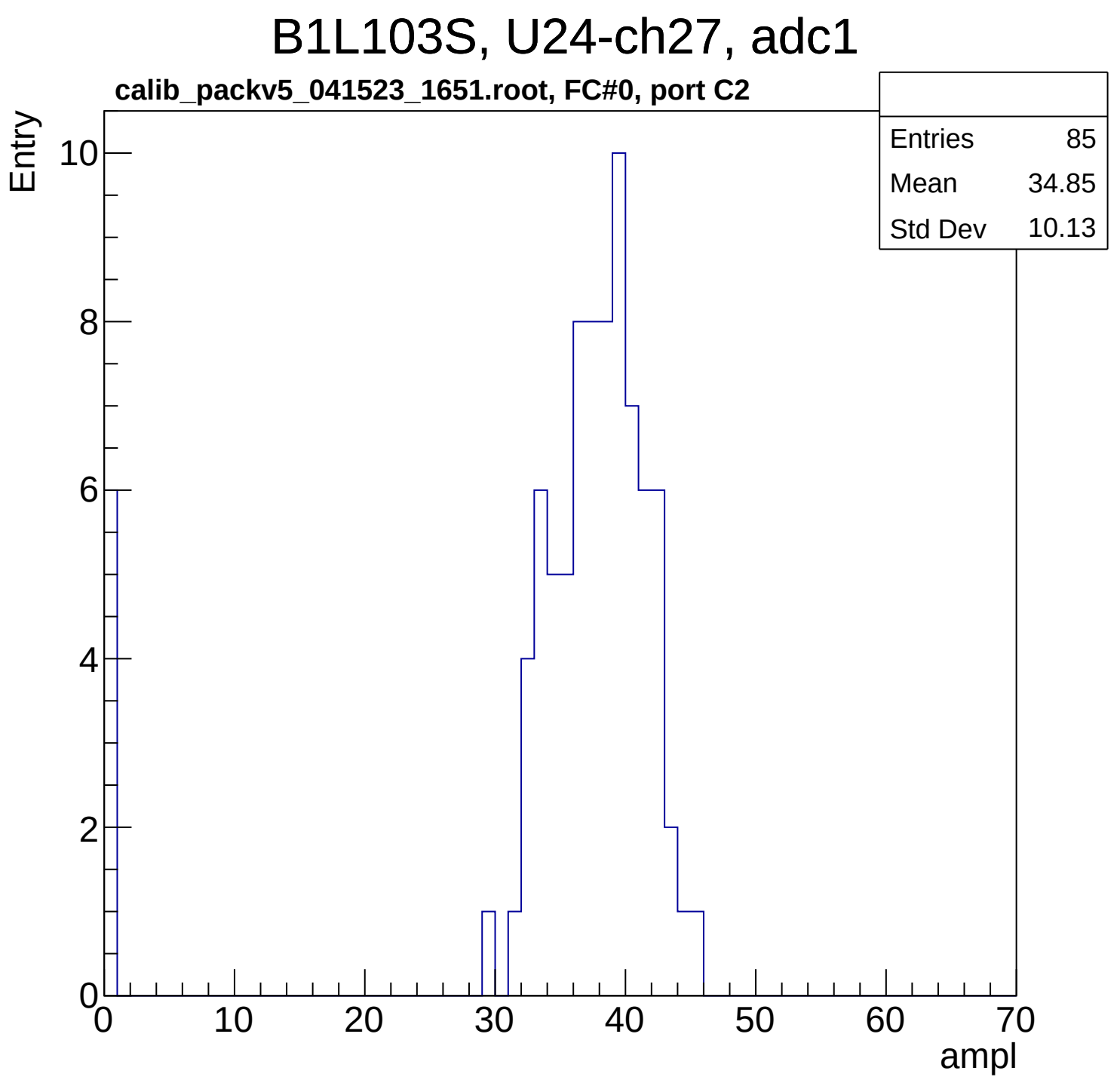
50
60
70
ampl


B1L103S, U24-ch27, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 96
Mean 21.48
Std Dev 14.1
Entry
0
5
10
15
20
25
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch27, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 34.85
Std Dev 10.13
Entry
ampl
0
2
4
6
8
10
0
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20
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40
50
60
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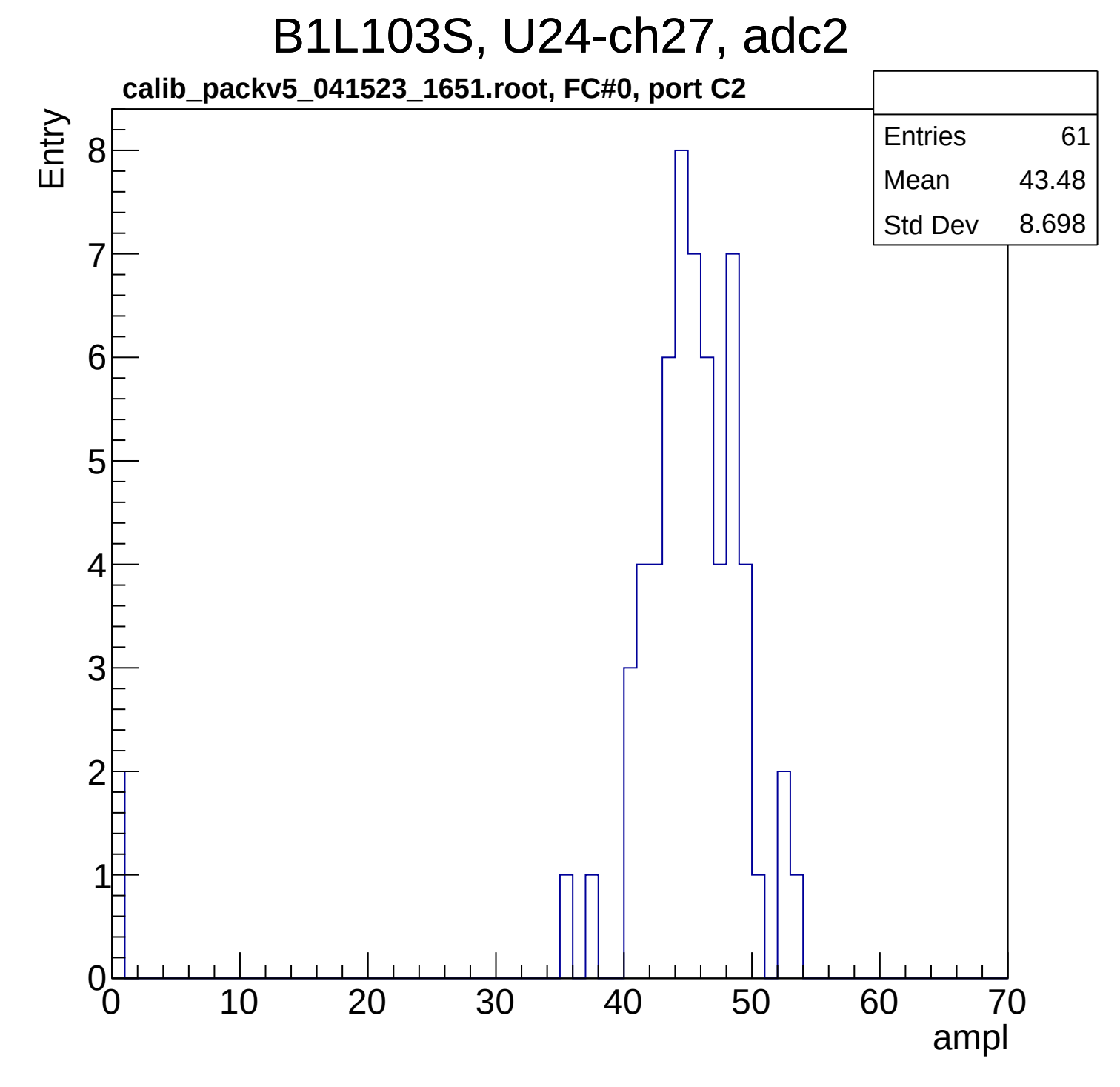
B1L103S, U24-ch27, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 43.48
Std Dev 8.698
Entry
ampl
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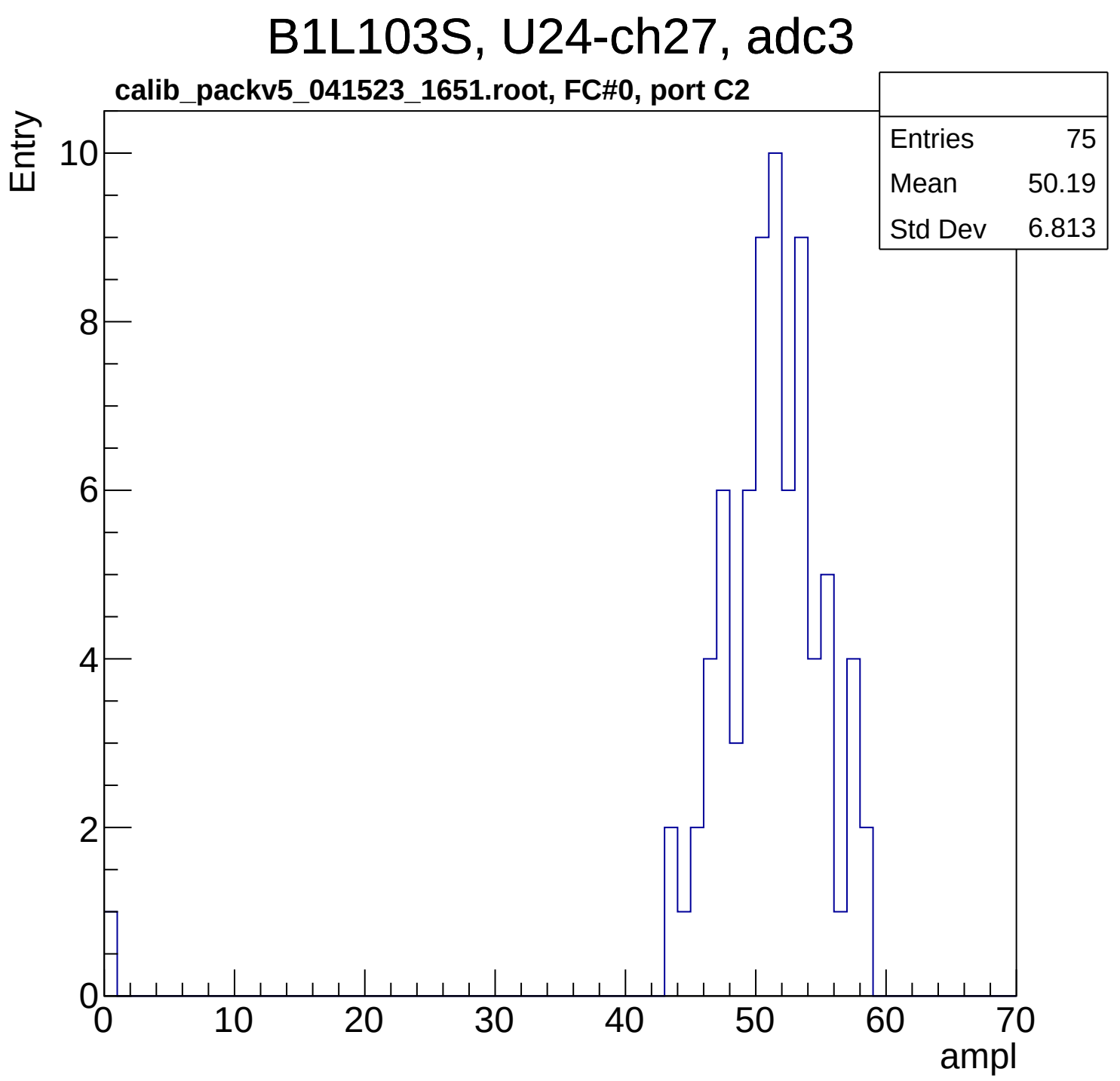
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U24-ch27, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 50.19
Std Dev 6.813
Entry
0
2
4
6
8
10
0
10
20
30
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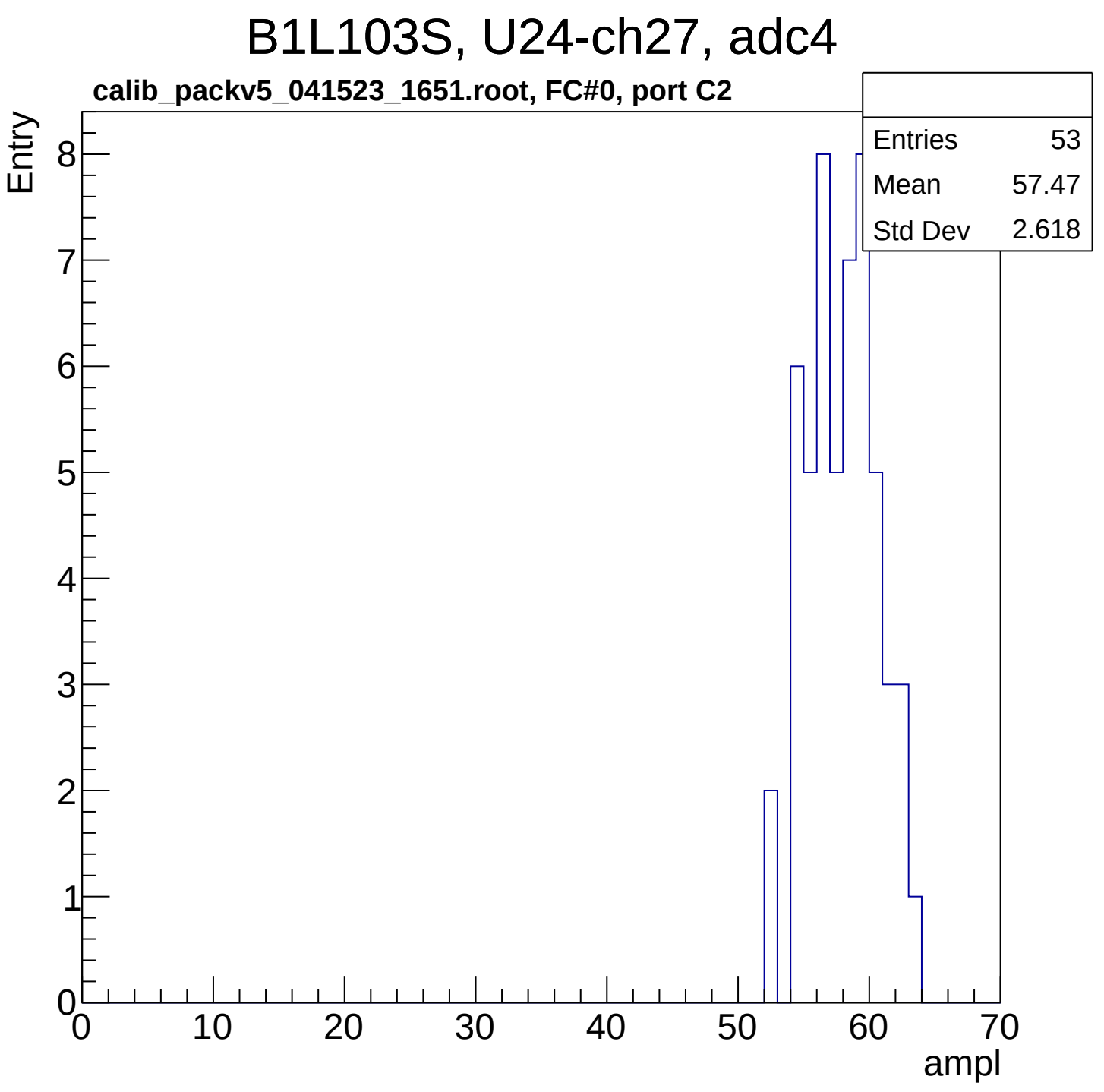
50
60
70
ampl


B1L103S, U24-ch27, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 57.47
Std Dev 2.618
Entry
ampl
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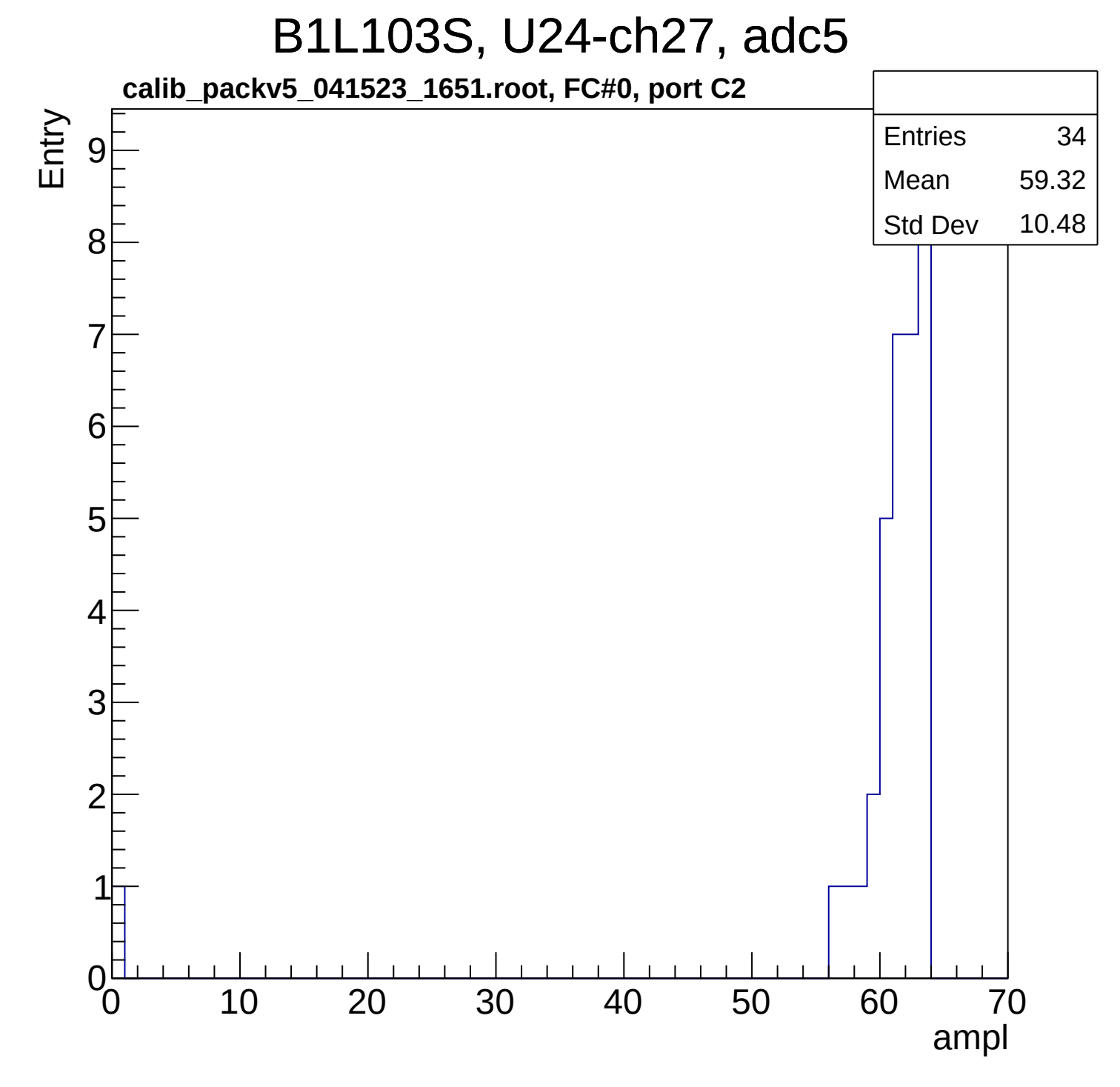
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U24-ch27, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 34
Mean 59.32
Std Dev 10.48
Entry
ampl
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2
3
4
5
6
7
8
9
0
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60
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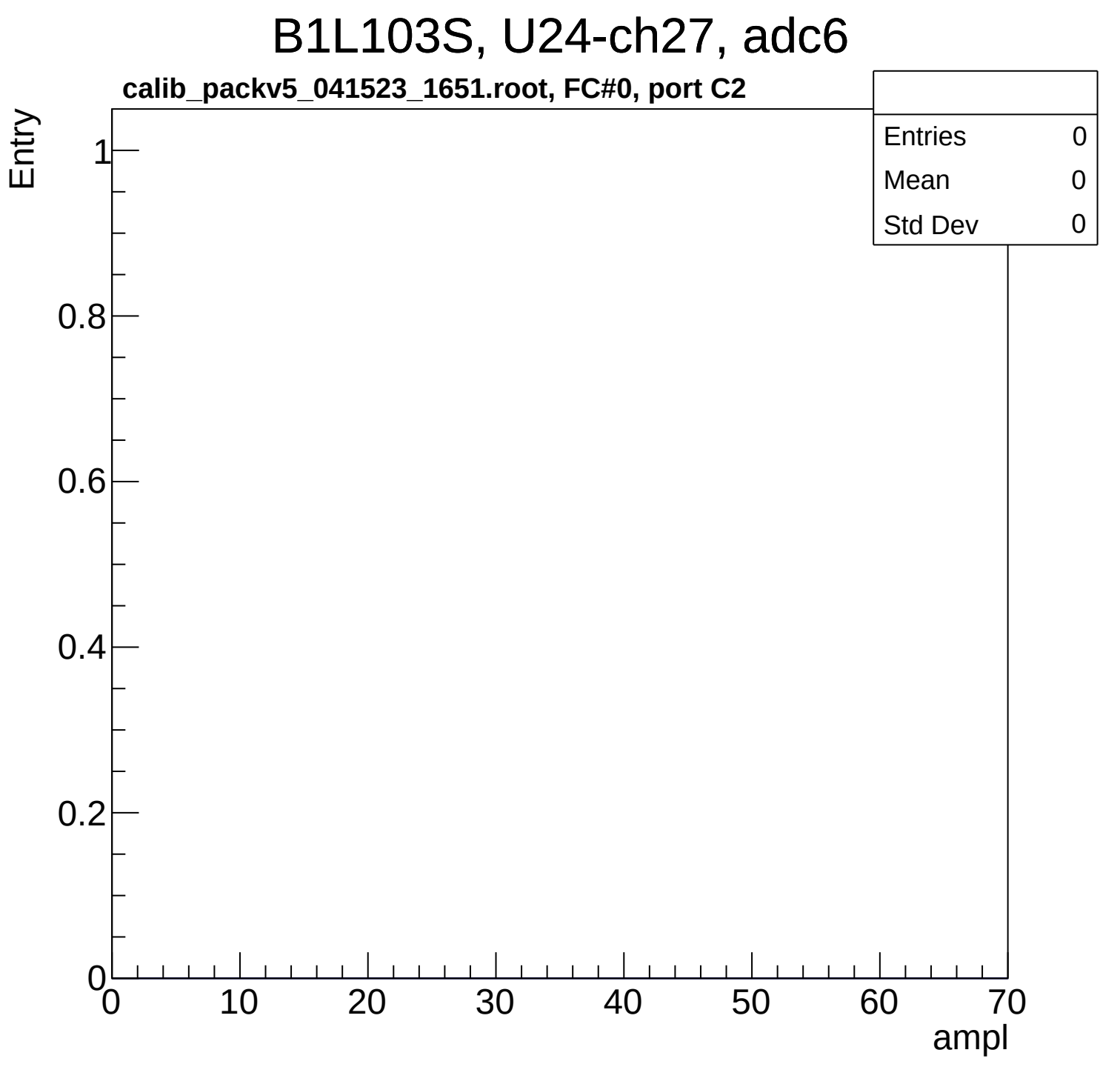
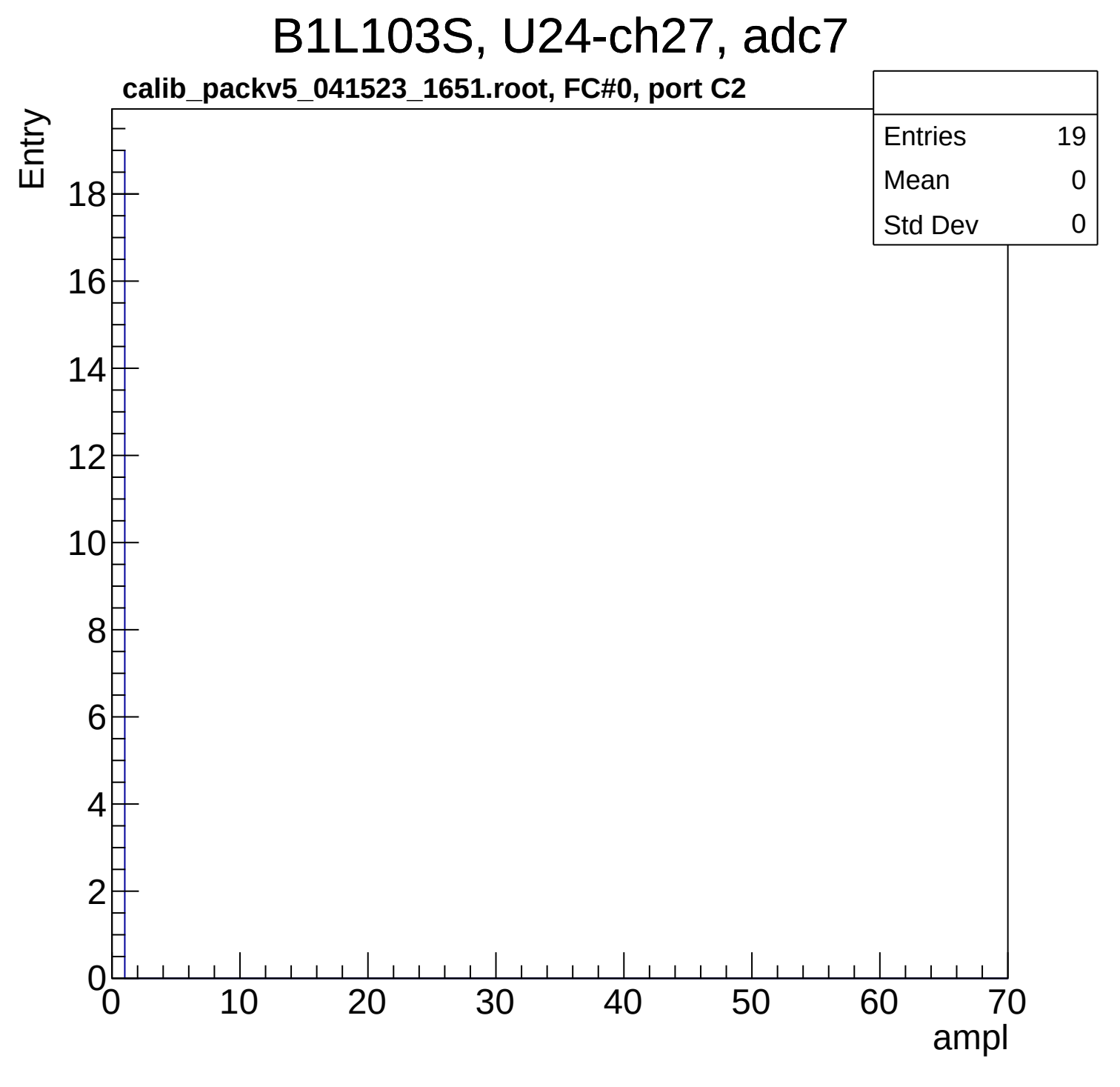
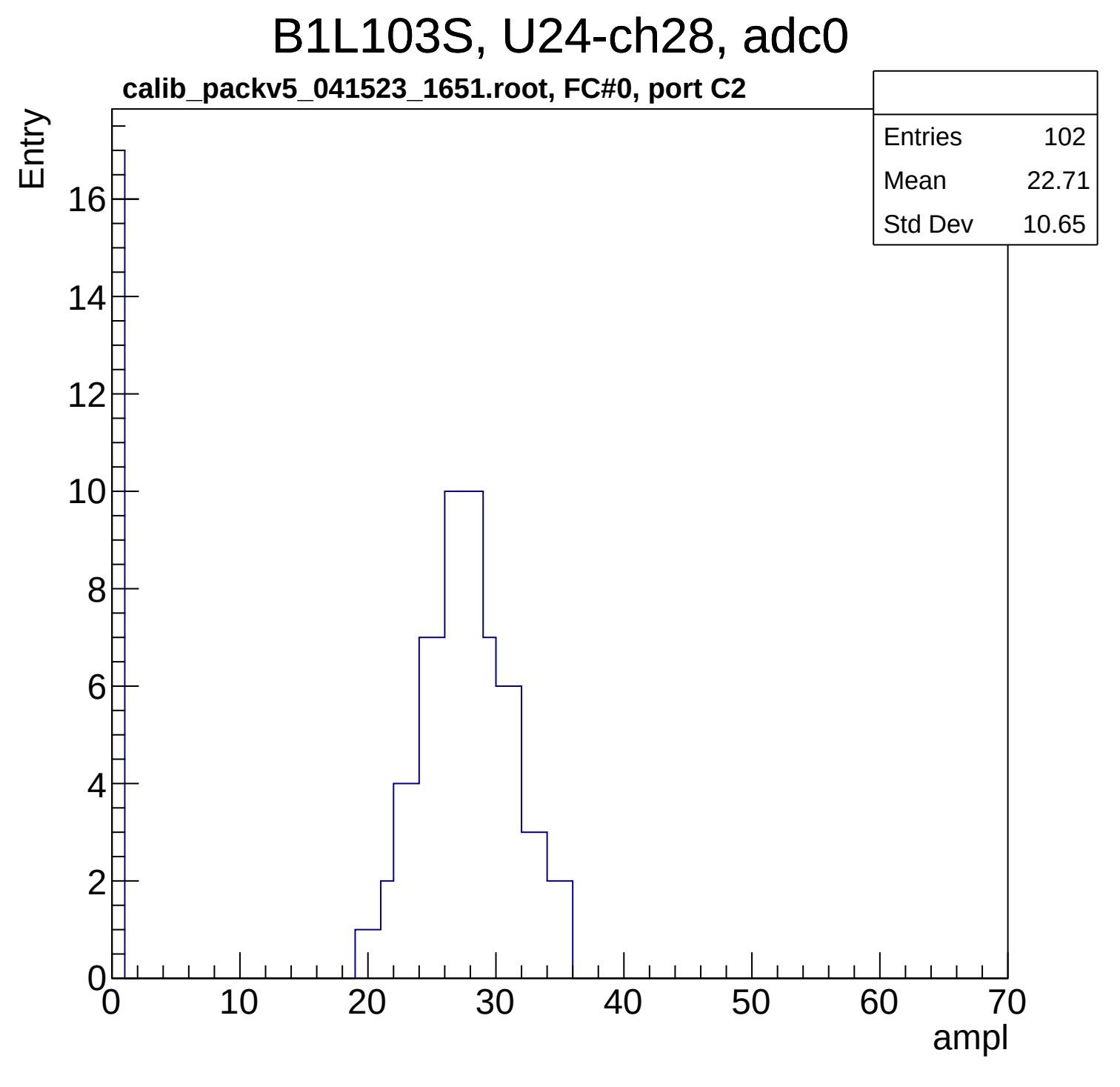
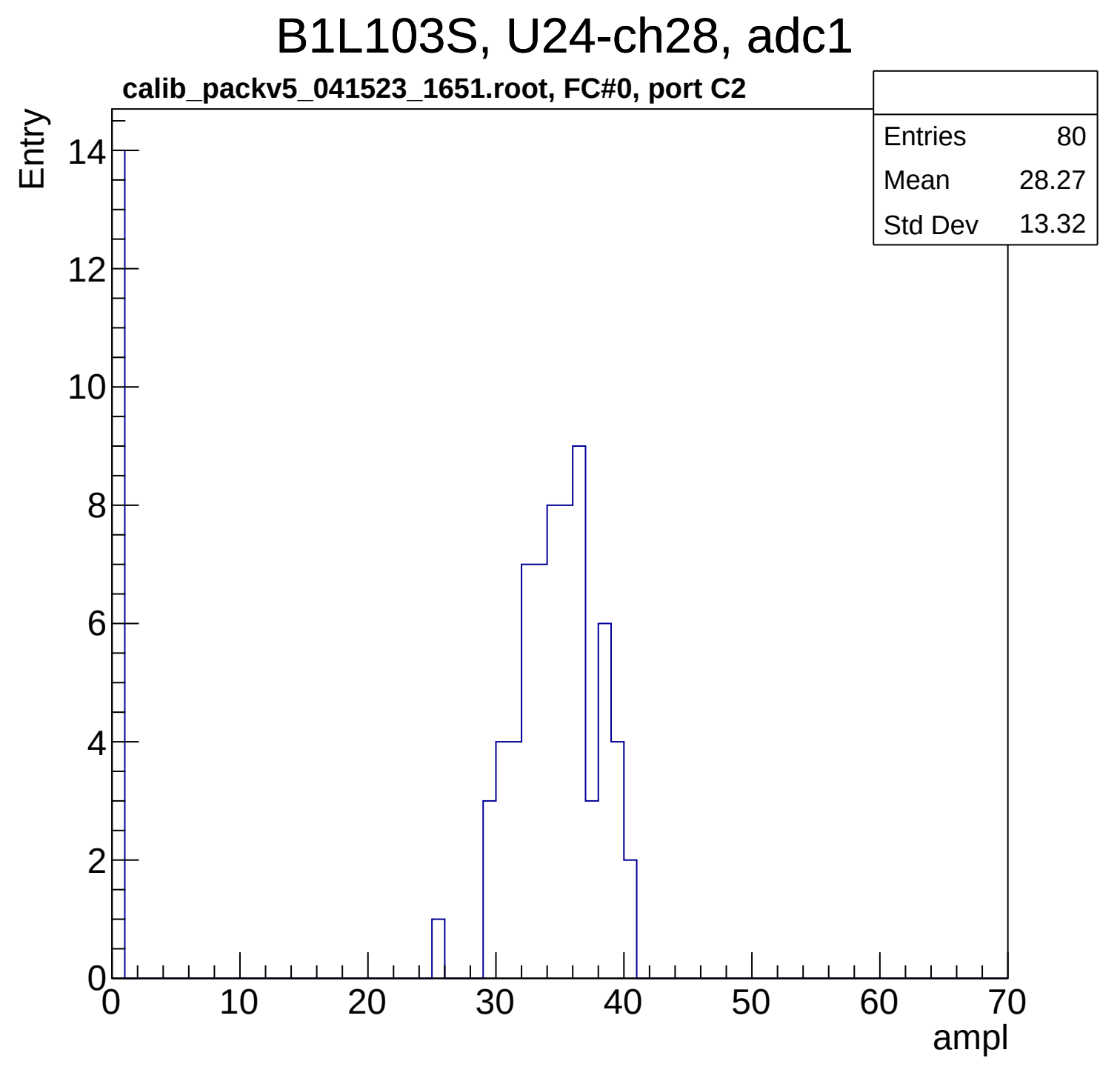
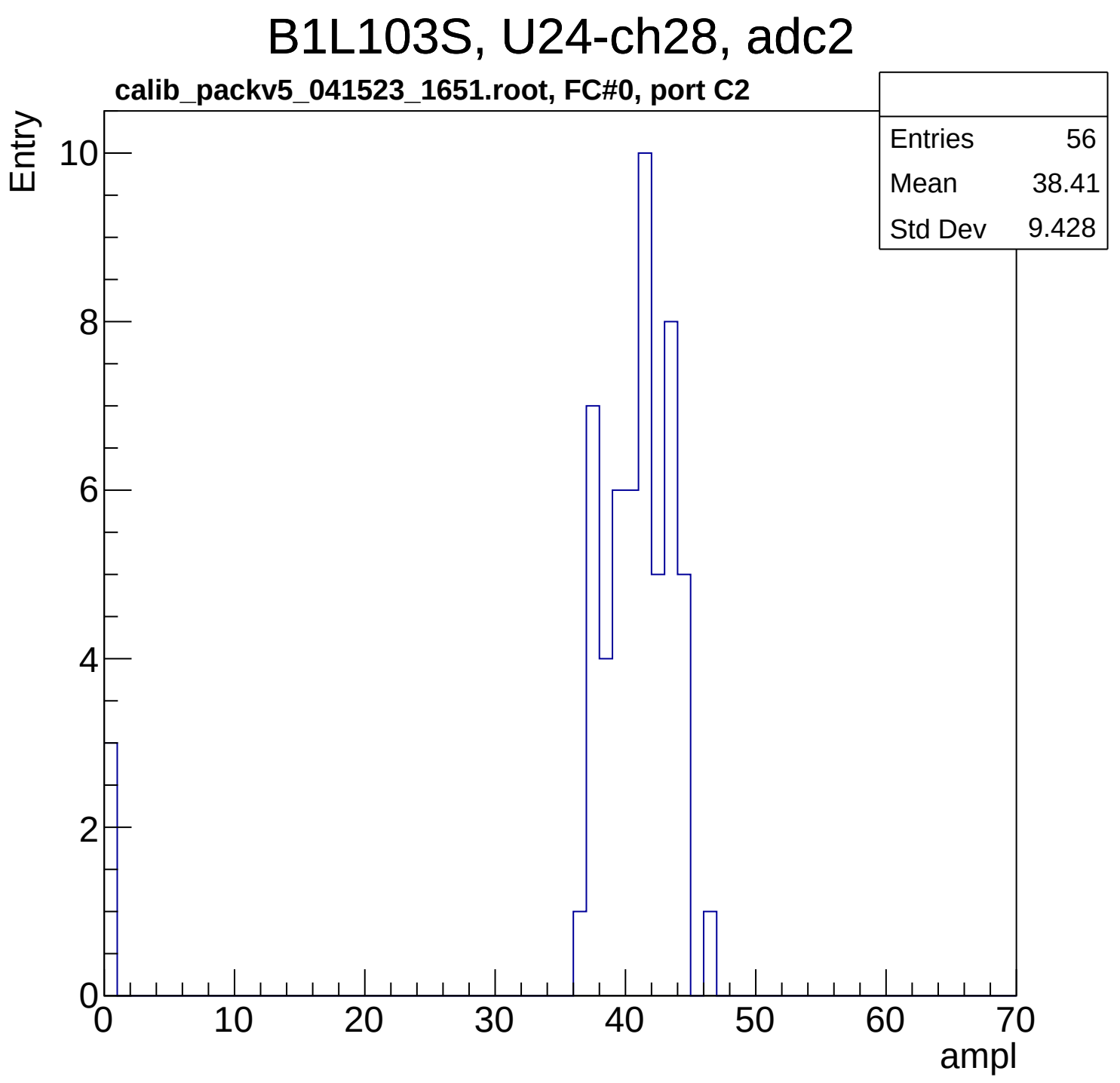
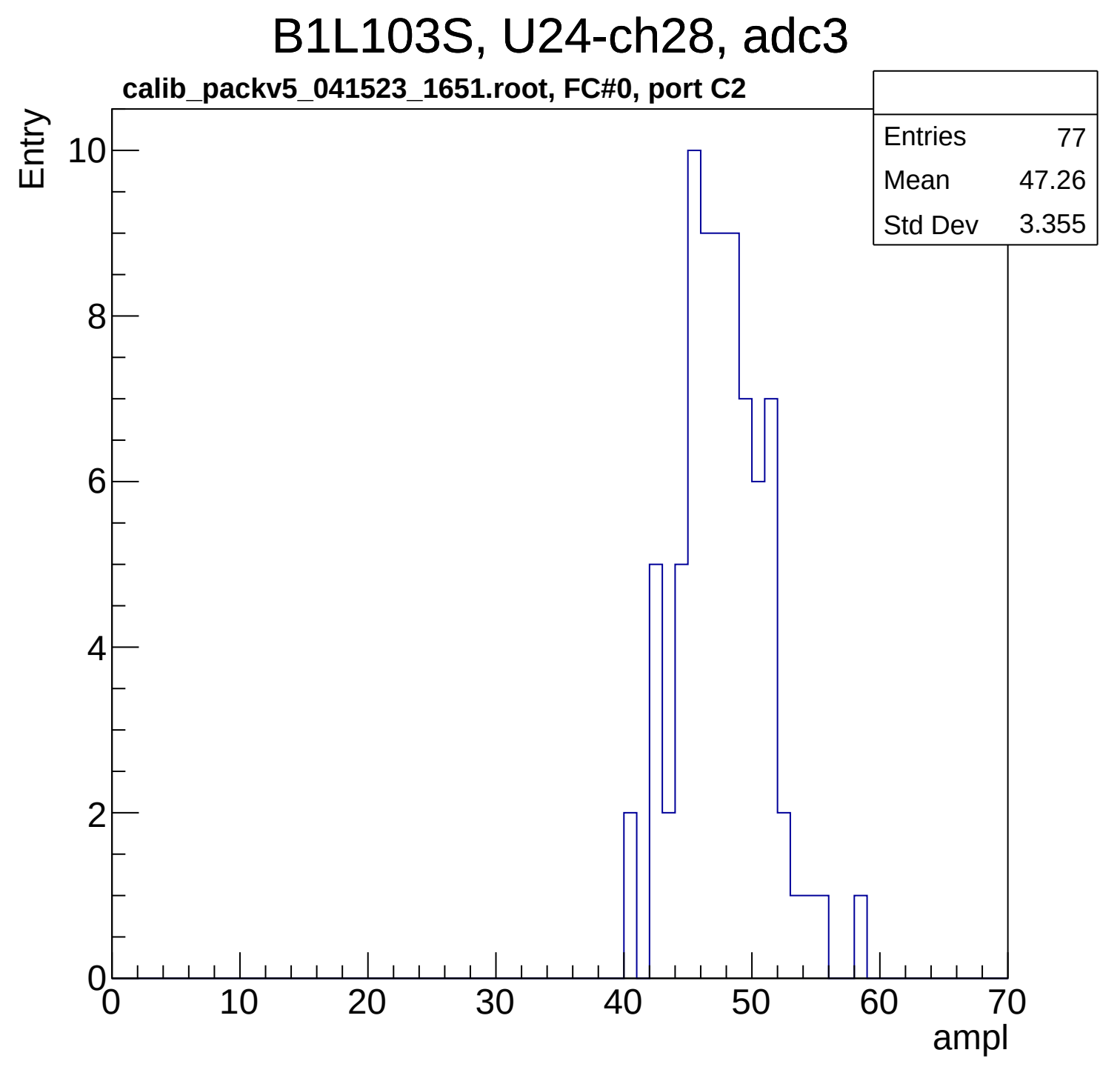

B1L103S, U24-ch27, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

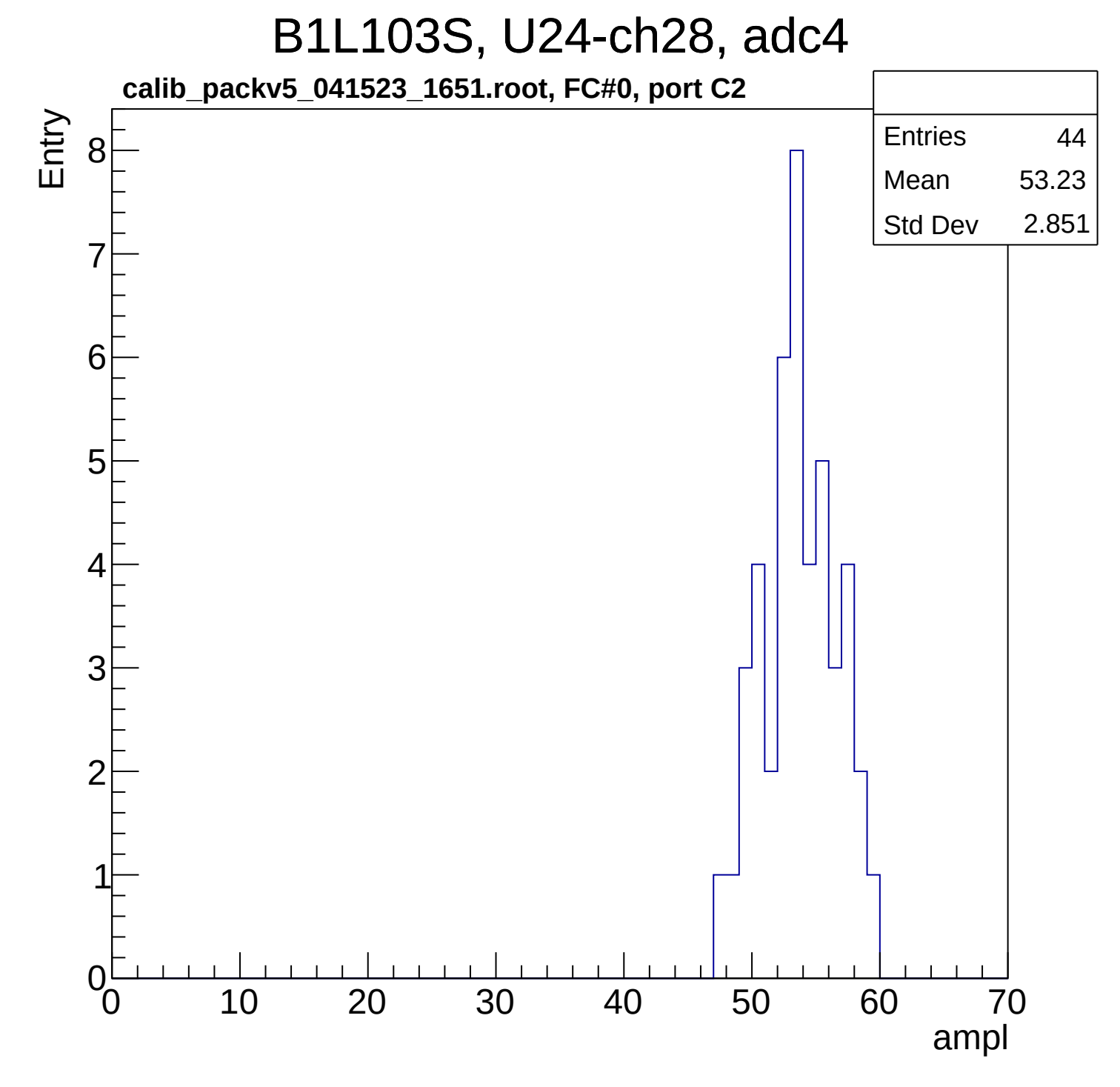

B1L103S, U24-ch27, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch28, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 102
Mean 22.71
Std Dev 10.65
Entry
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch28, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 28.27
Std Dev 13.32
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch28, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 38.41
Std Dev 9.428
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U24-ch28, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 47.26
Std Dev 3.355
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U24-ch28, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 53.23
Std Dev 2.851
Entry
ampl
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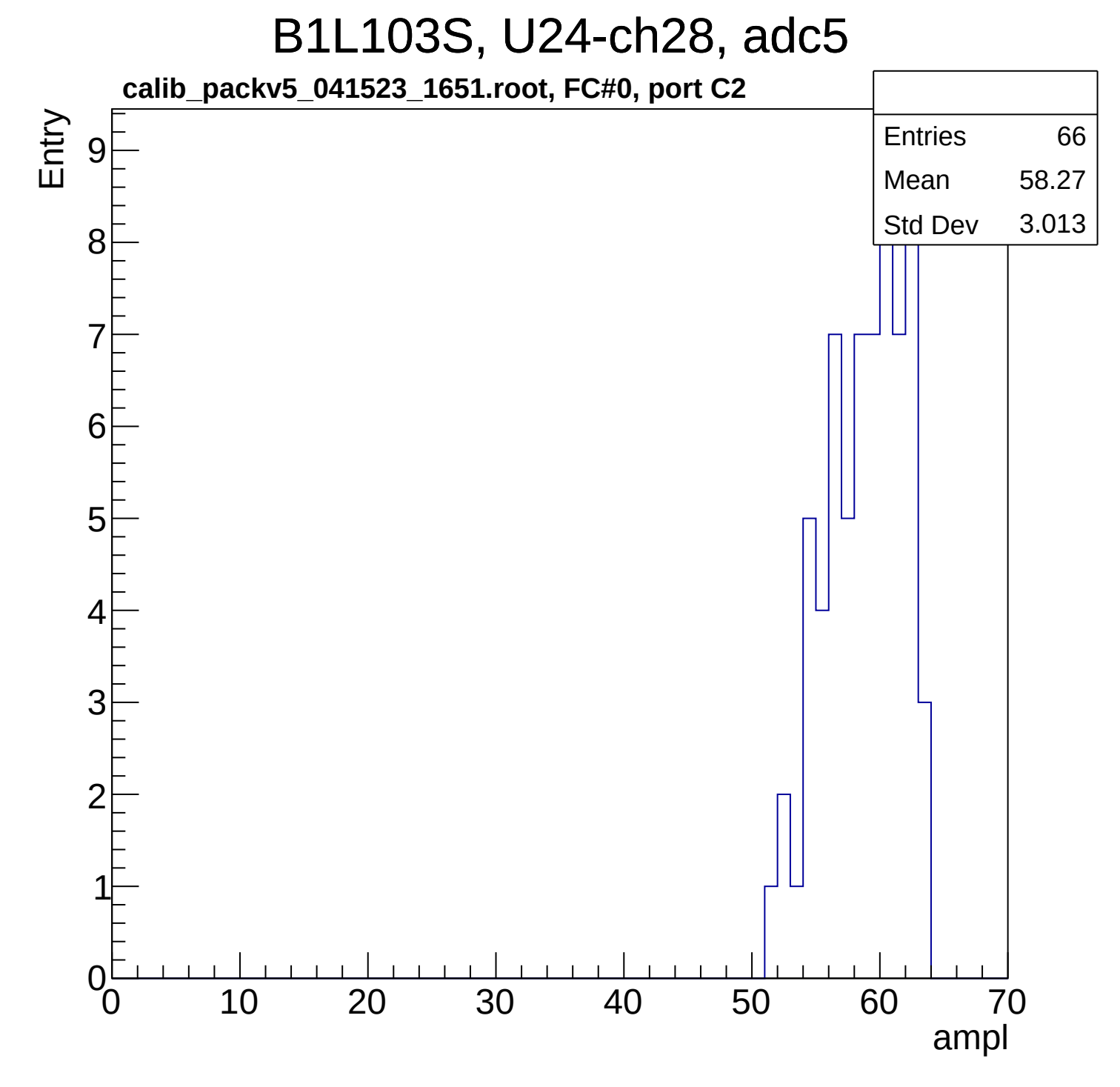
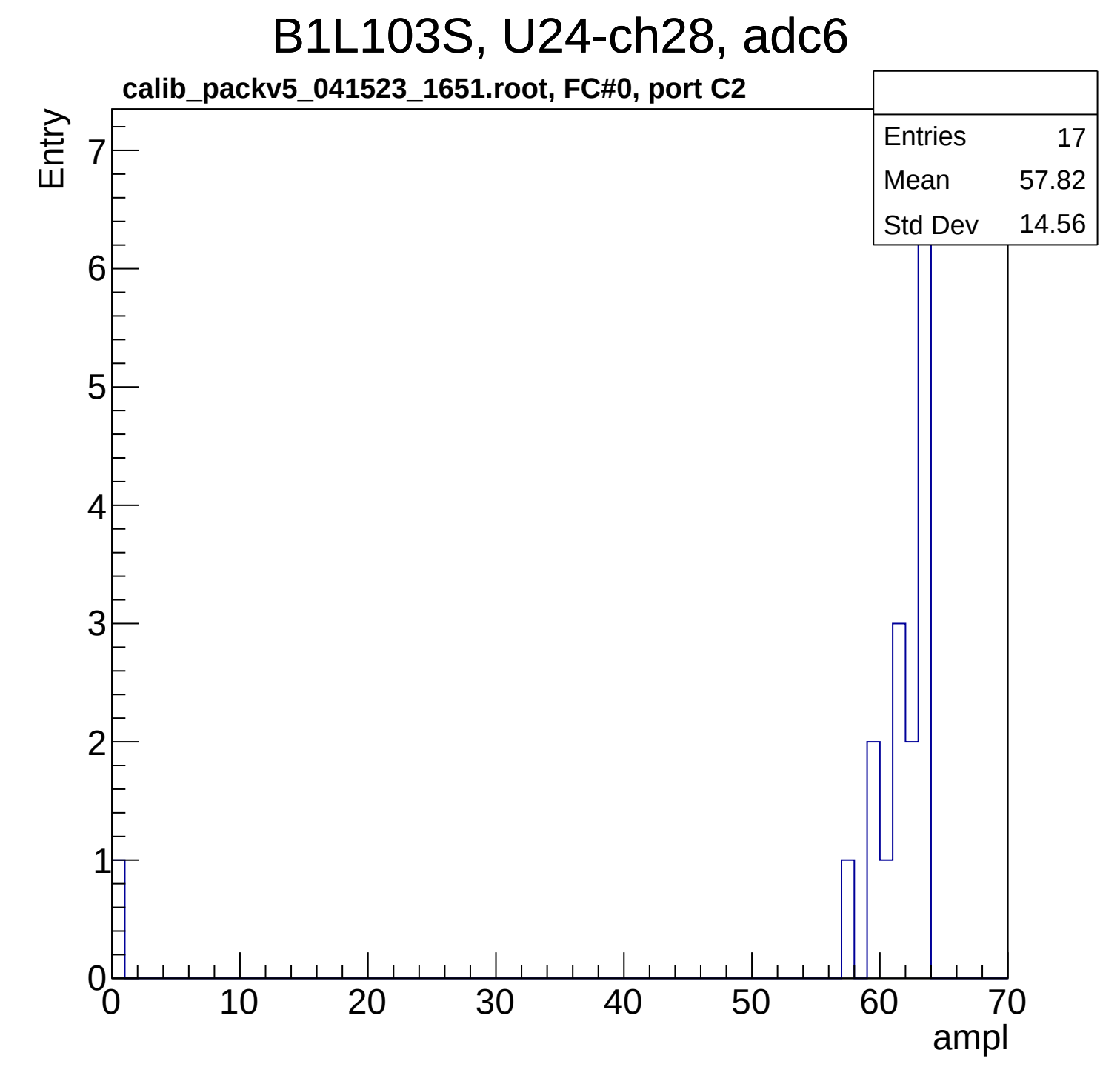
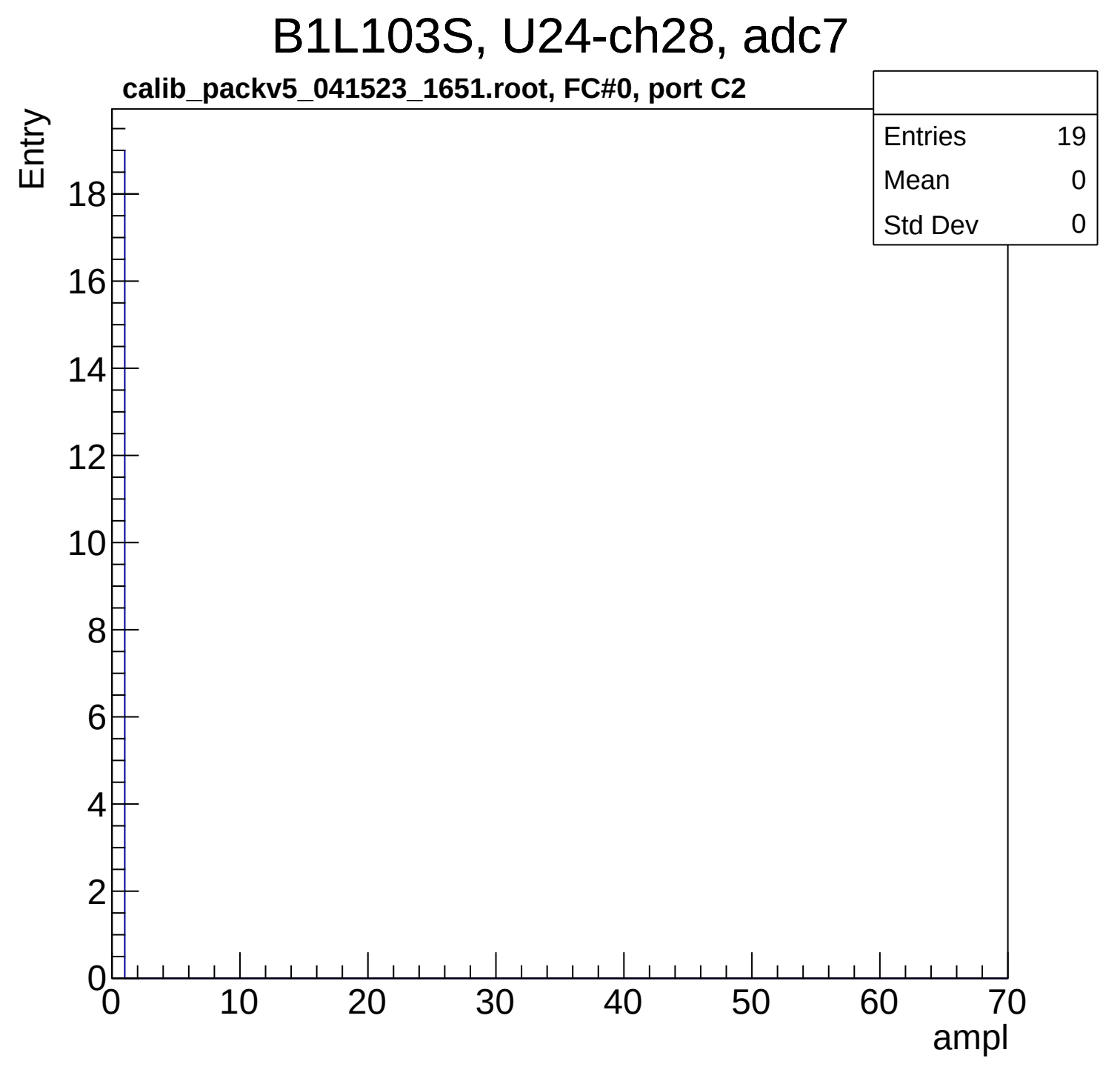
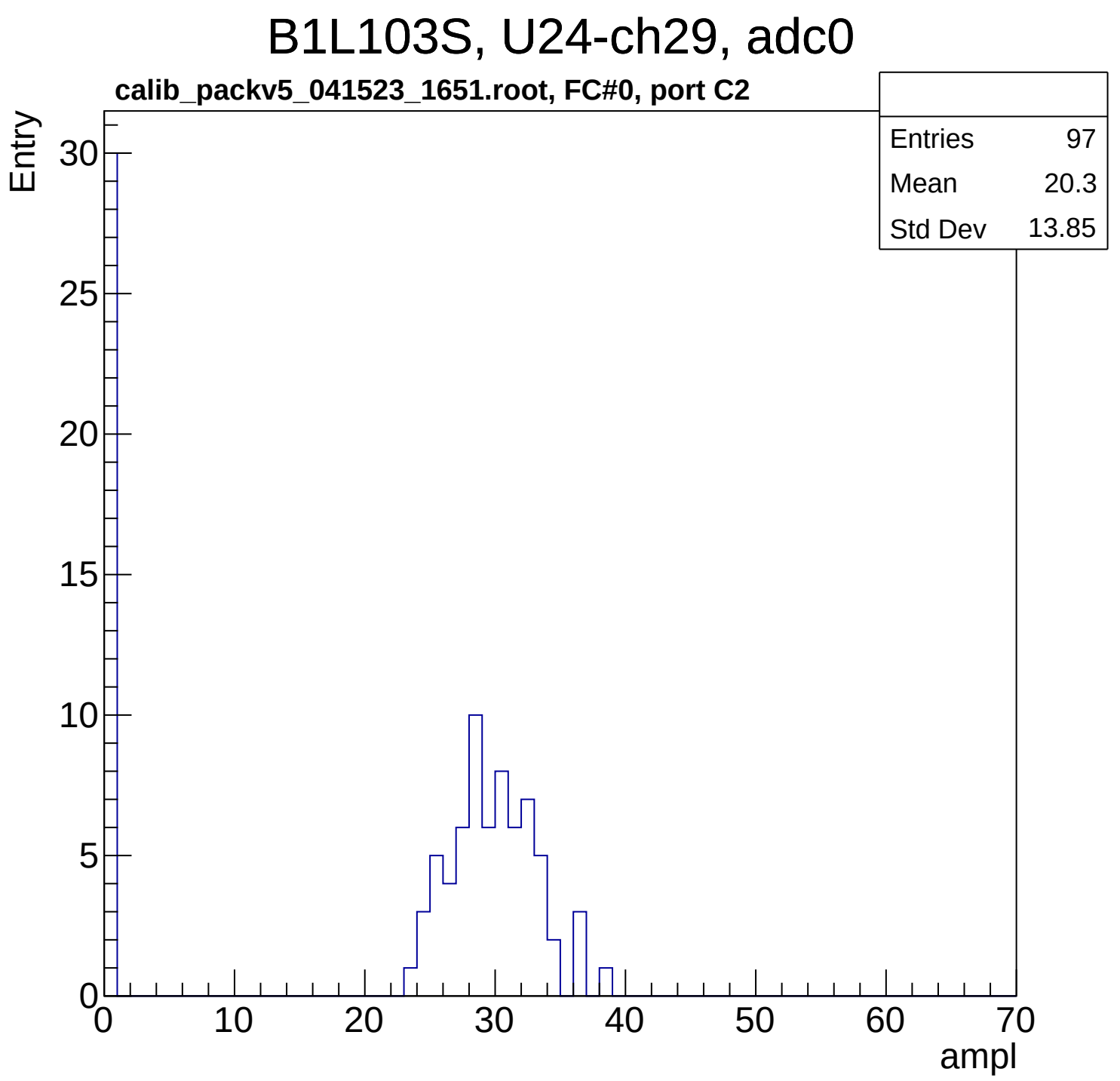
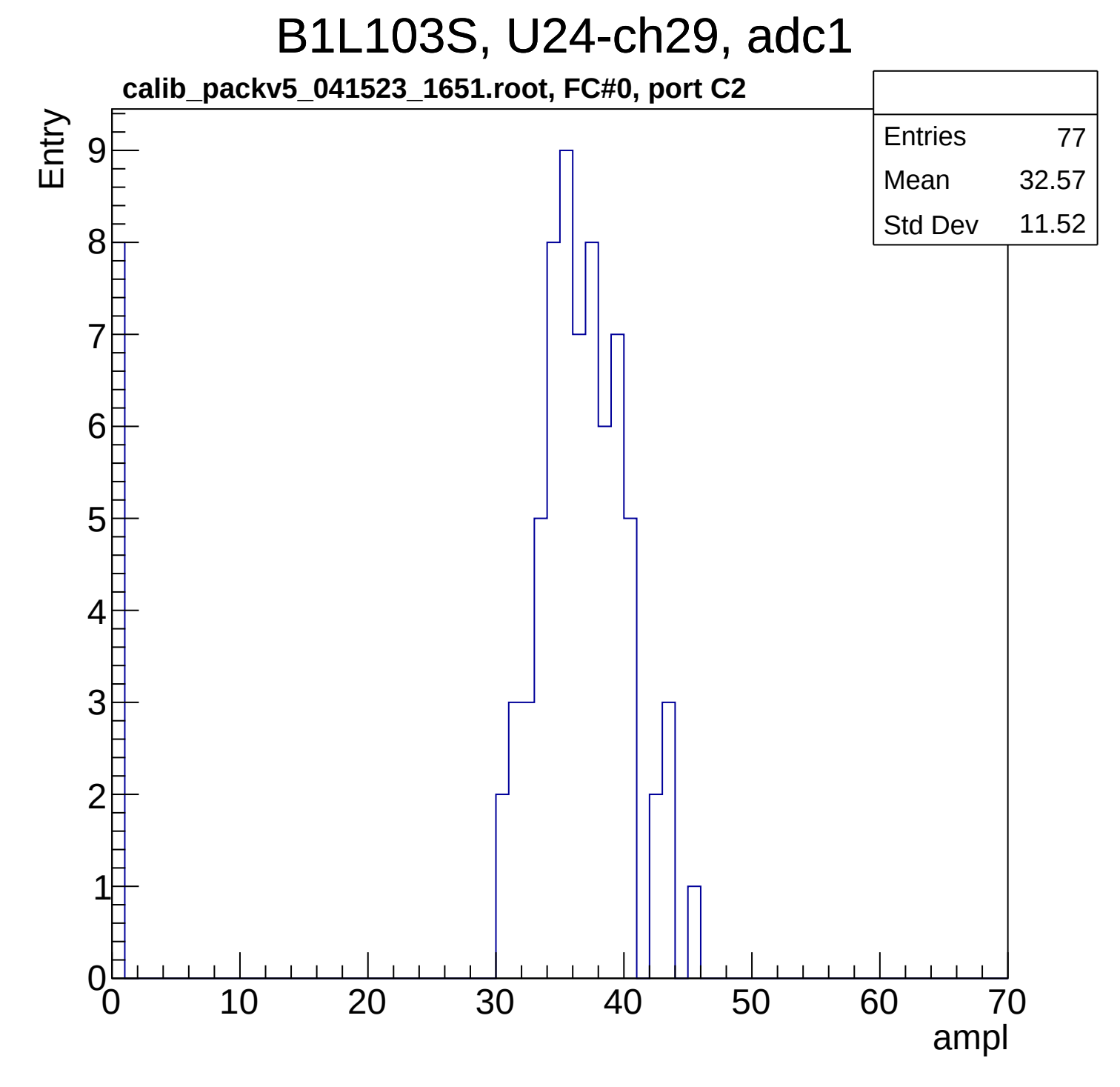
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

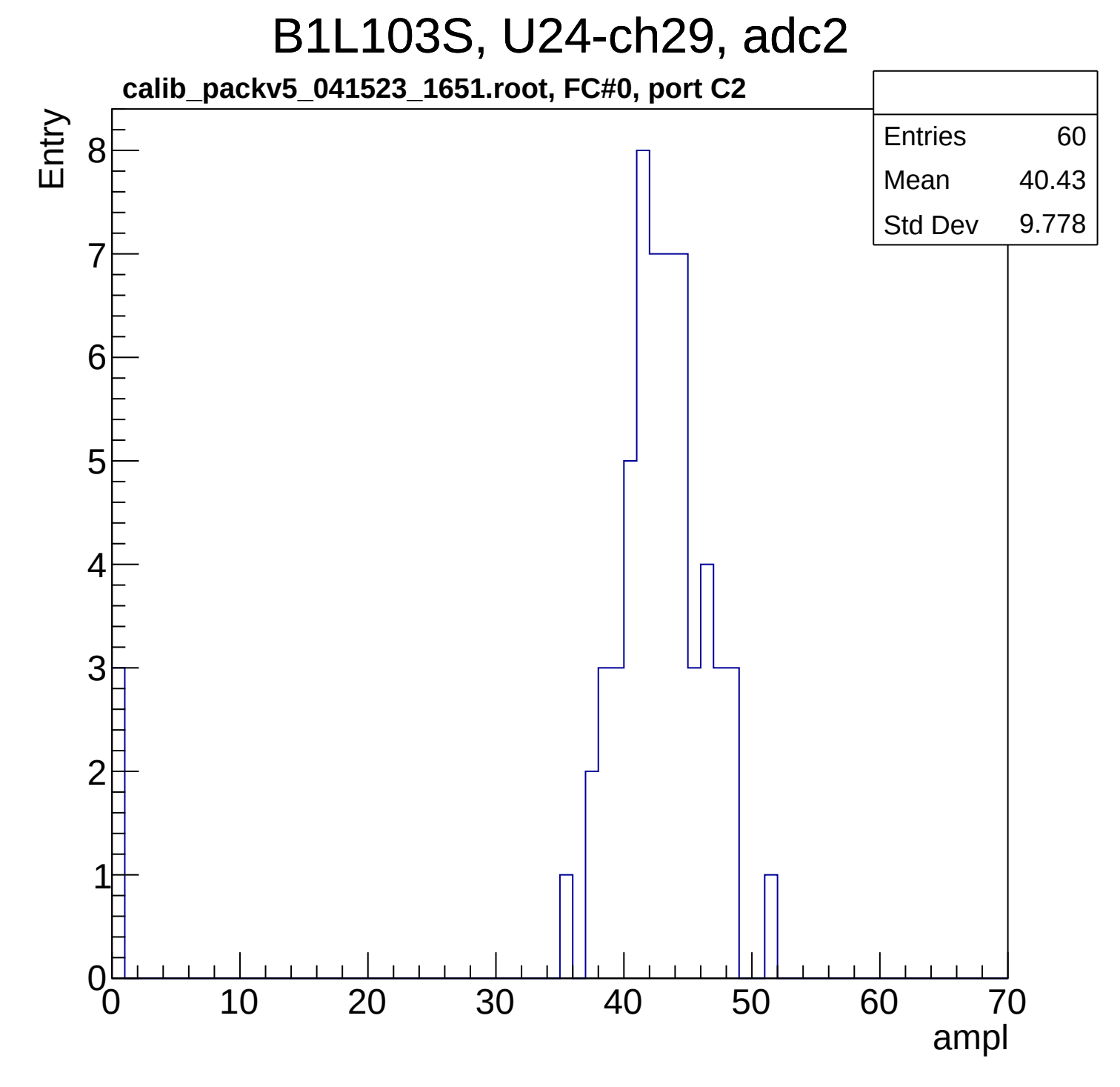

B1L103S, U24-ch28, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 58.27
Std Dev 3.013
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

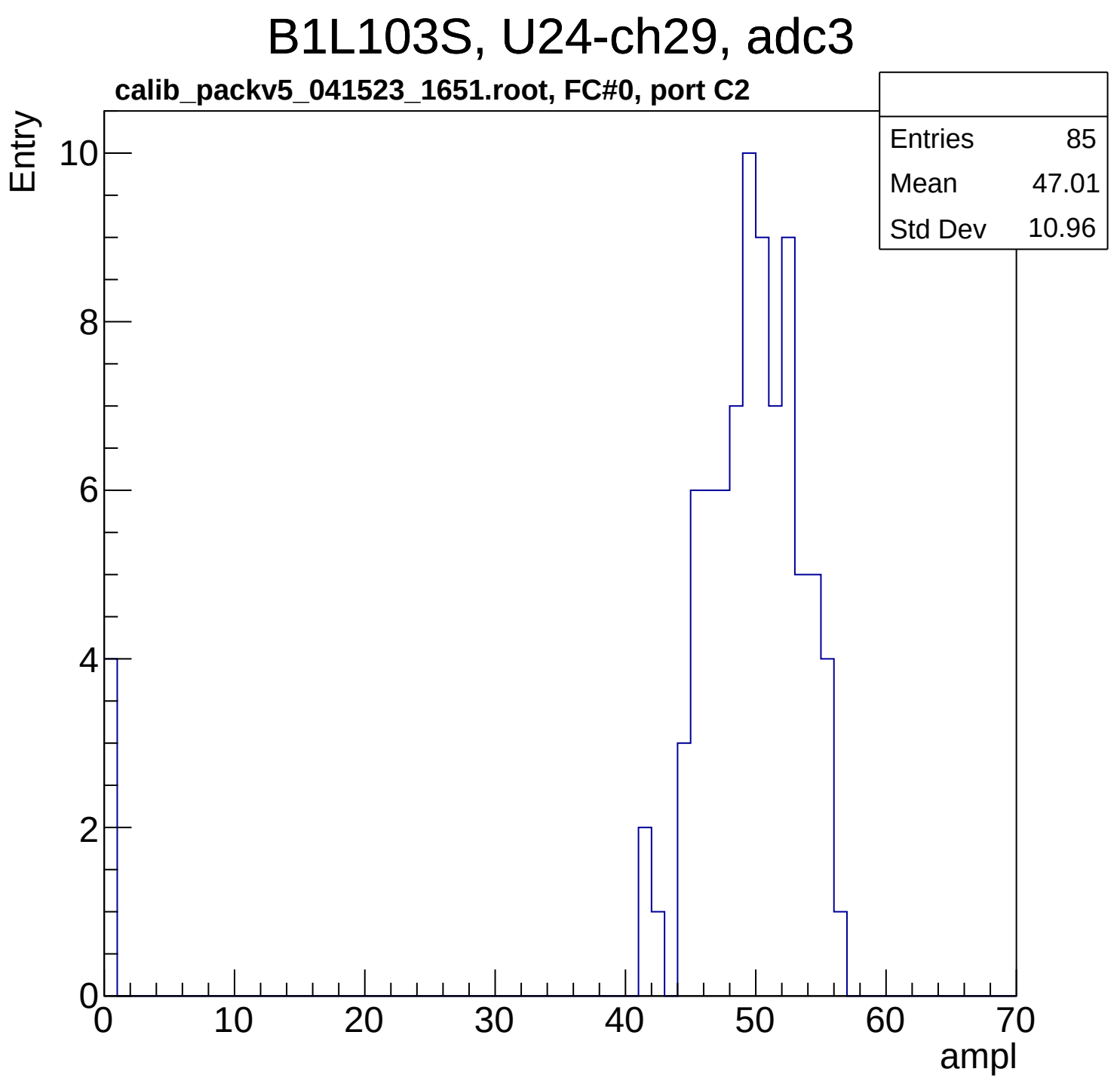

B1L103S, U24-ch28, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 17
Mean 57.82
Std Dev 14.56
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

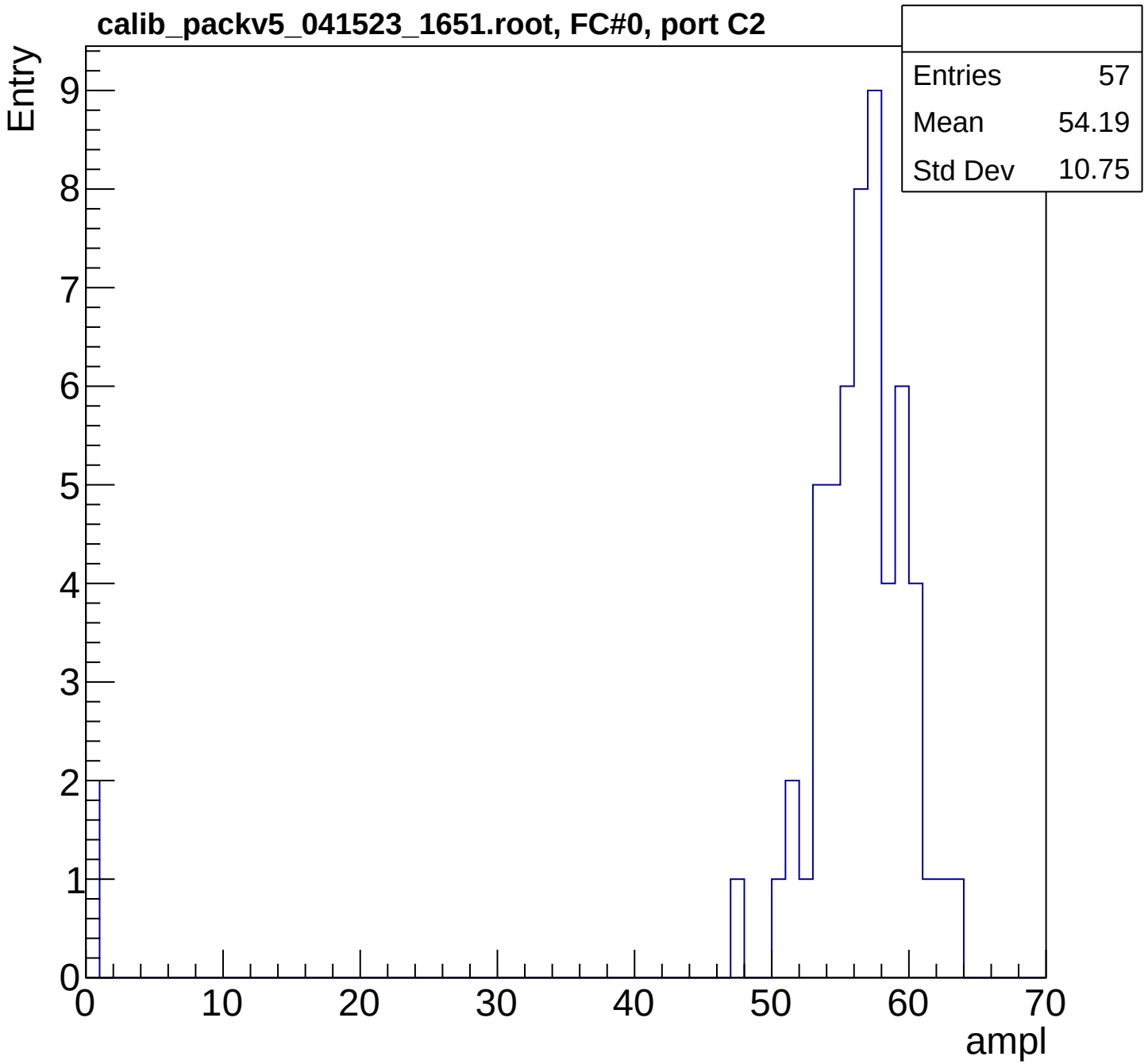

B1L103S, U24-ch28, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch29, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 97
Mean 20.3
Std Dev 13.85
Entry
0
5
10
15
20
25
30
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch29, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 32.57
Std Dev 11.52
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U24-ch29, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 40.43
Std Dev 9.778
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U24-ch29, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 47.01
Std Dev 10.96
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U24-ch29, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 54.19
Std Dev 10.75
Entry
ampl
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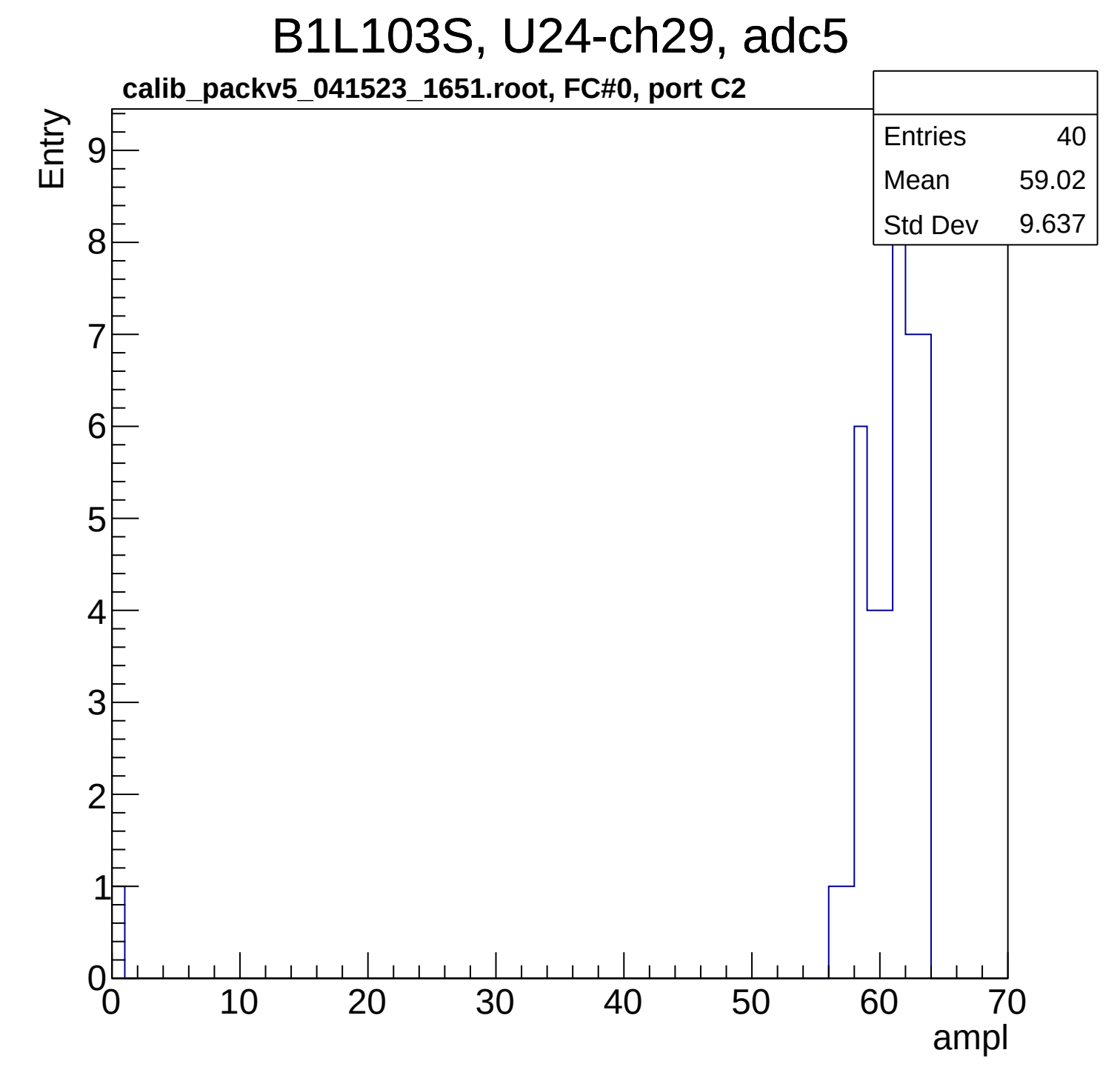
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U24-ch29, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 40
Mean 59.02
Std Dev 9.637
Entry
ampl
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2
3
4
5
6
7
8
9
0
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40
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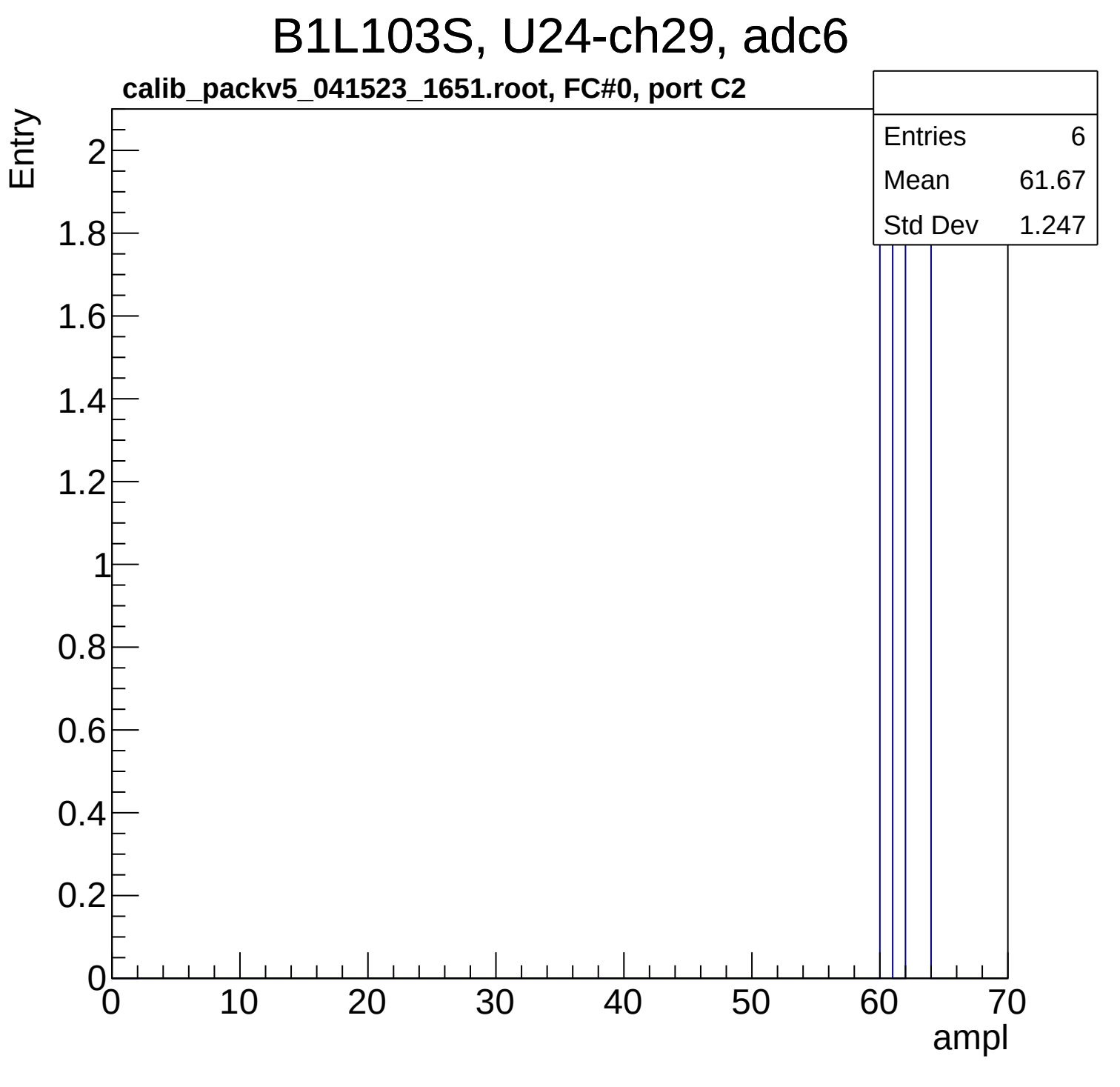
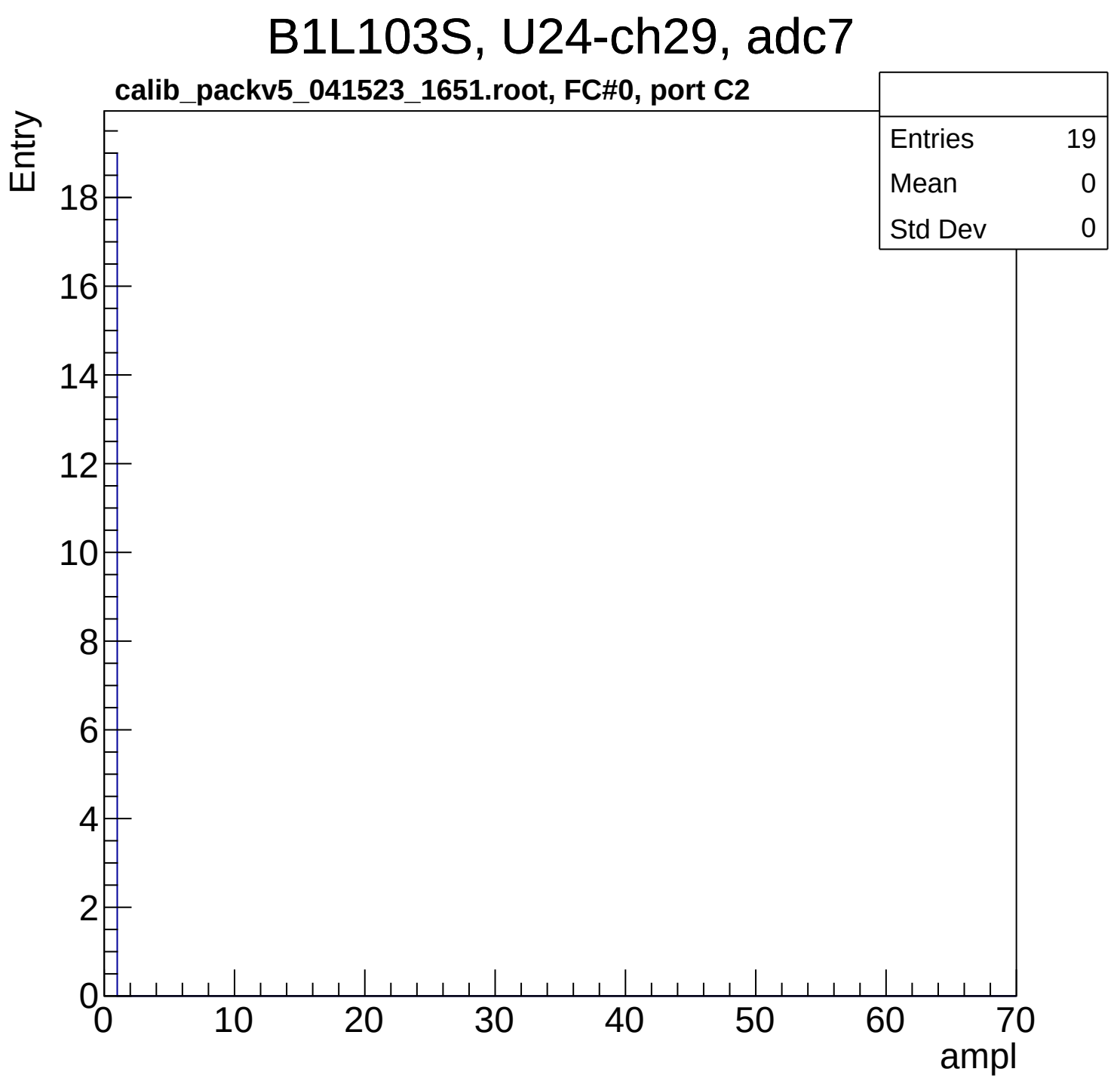
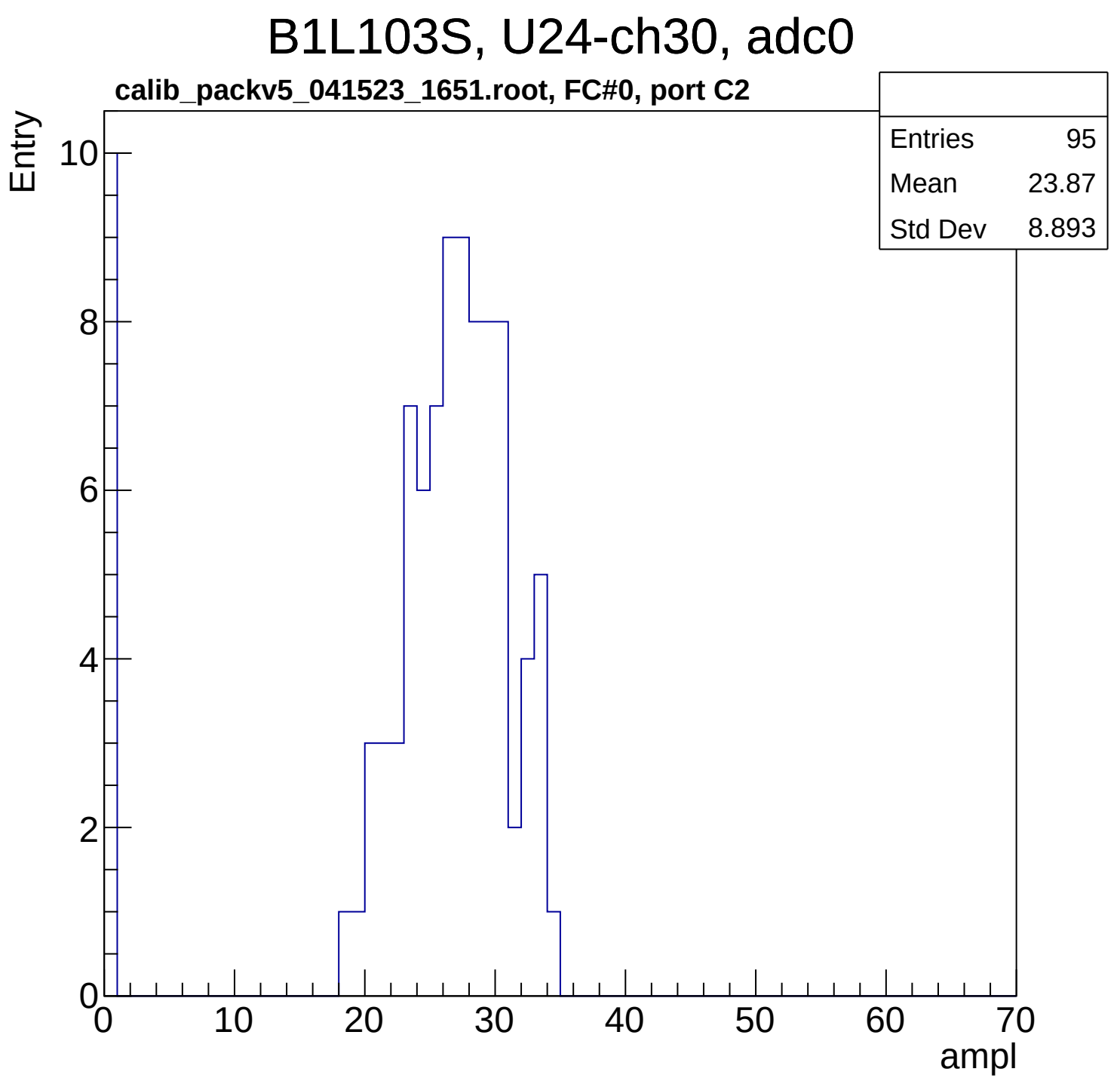
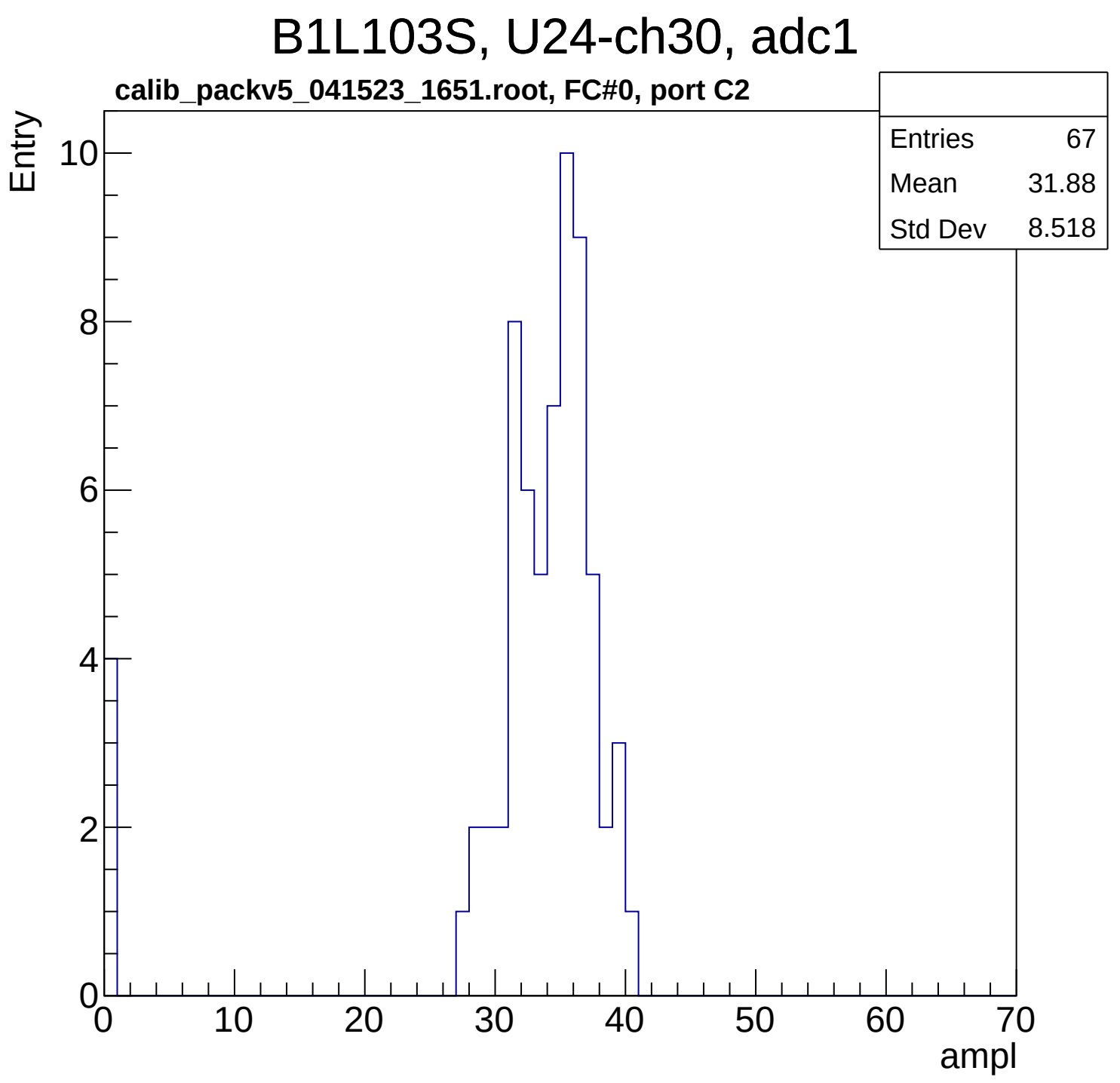
60
70


B1L103S, U24-ch29, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 61.67
Std Dev 1.247
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U24-ch29, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch30, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 95
Mean 23.87
Std Dev 8.893
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U24-ch30, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 31.88
Std Dev 8.518
Entry
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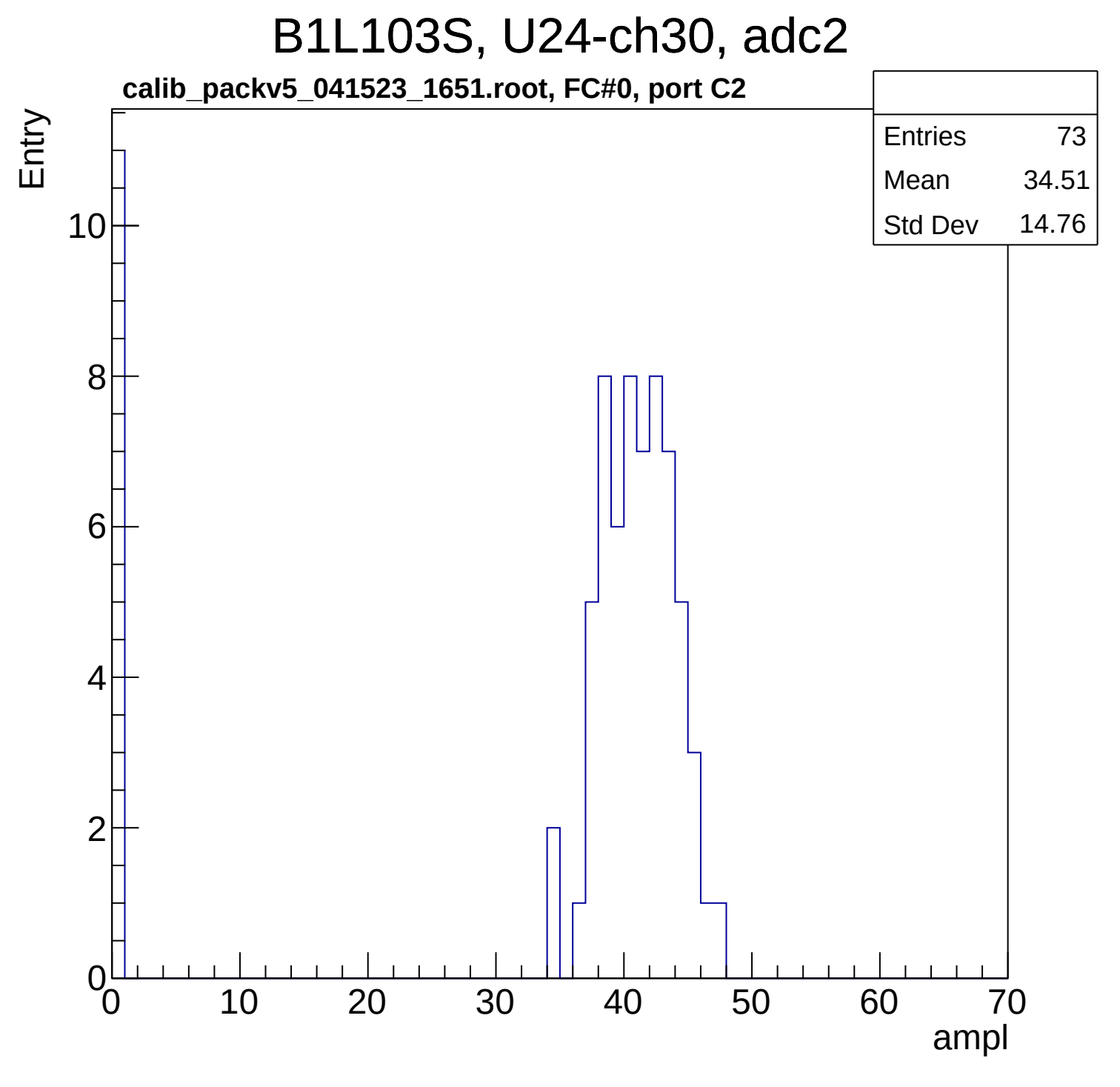
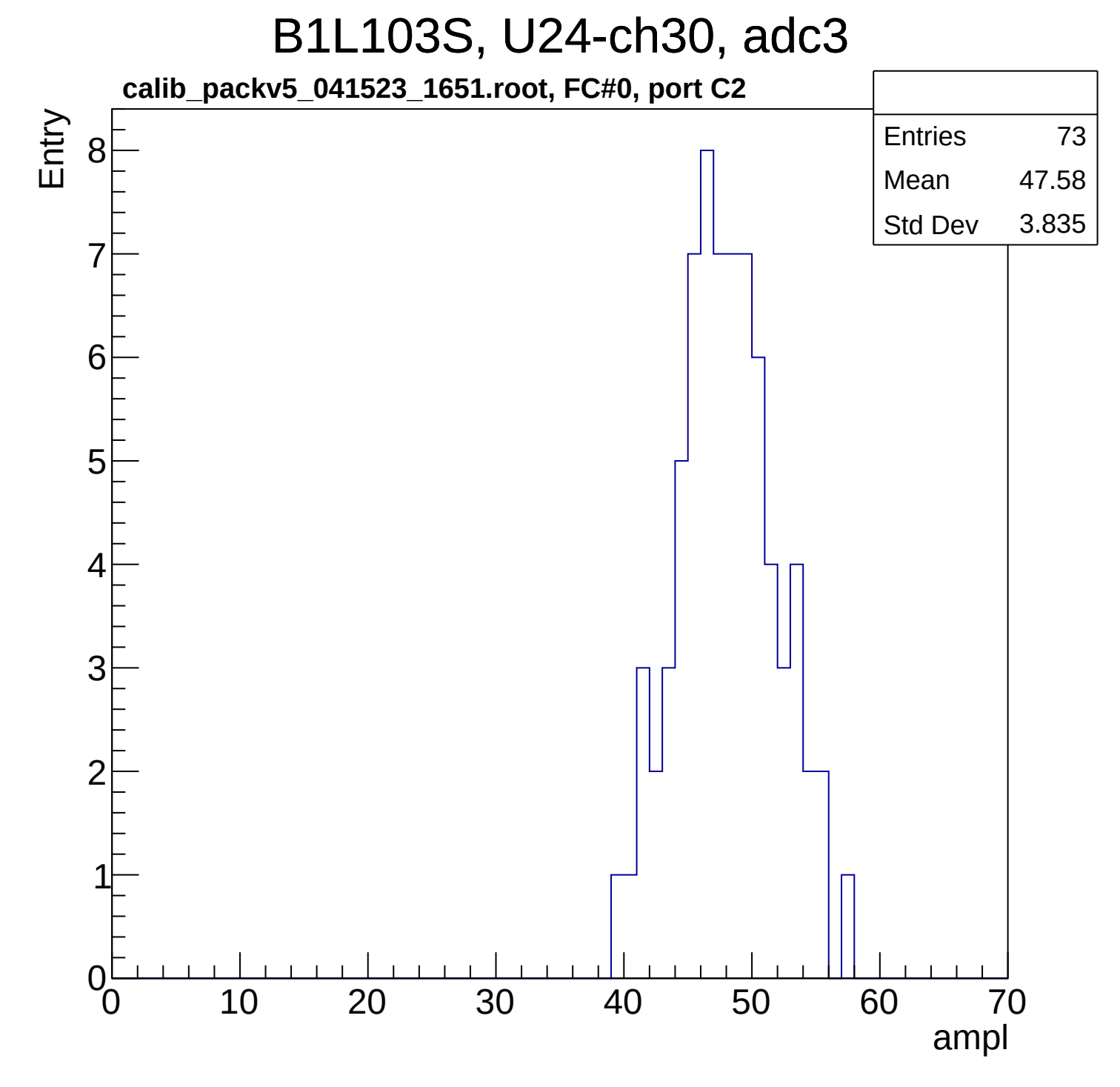
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch30, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 34.51
Std Dev 14.76
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch30, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 47.58
Std Dev 3.835
Entry
ampl
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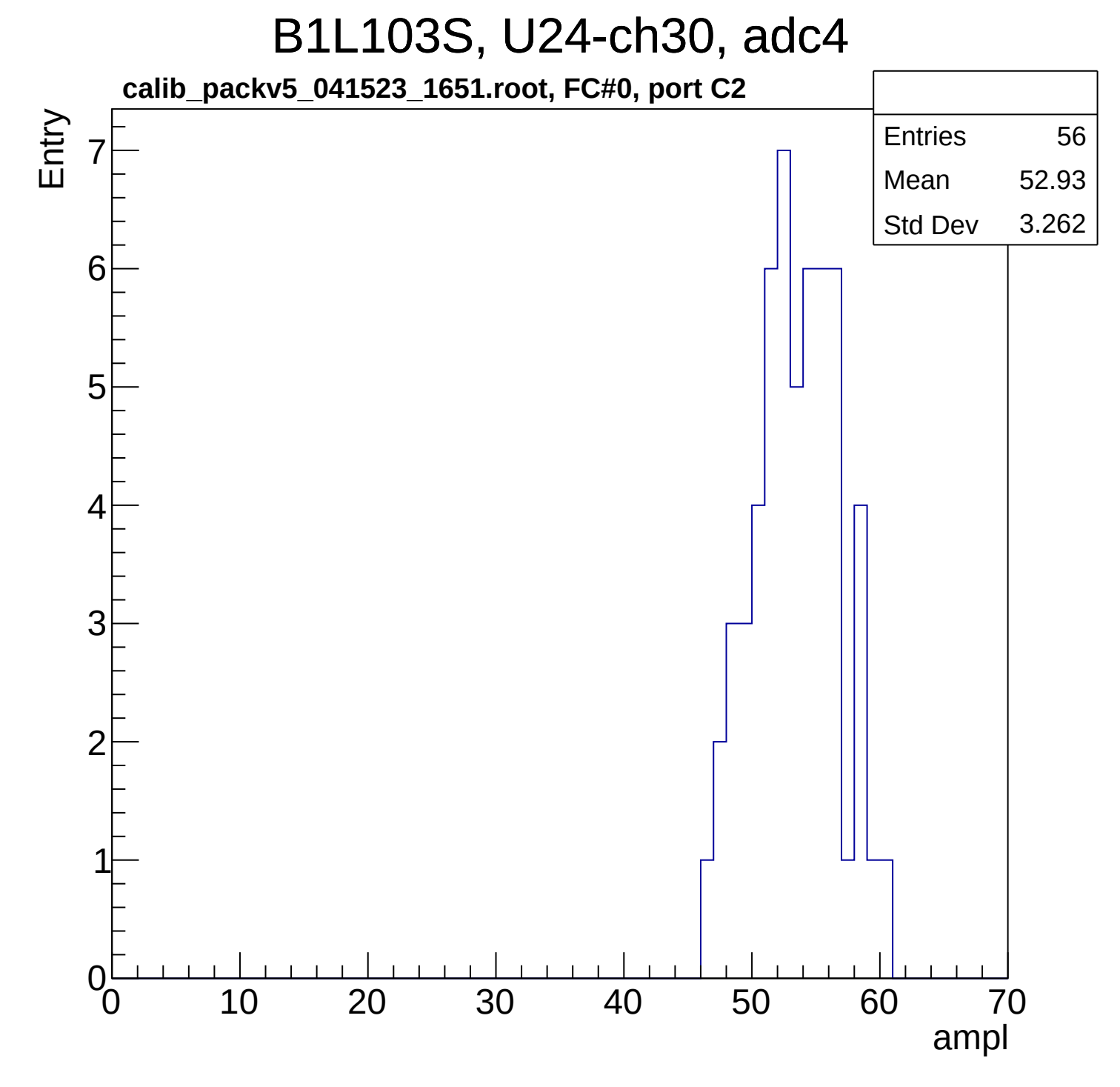
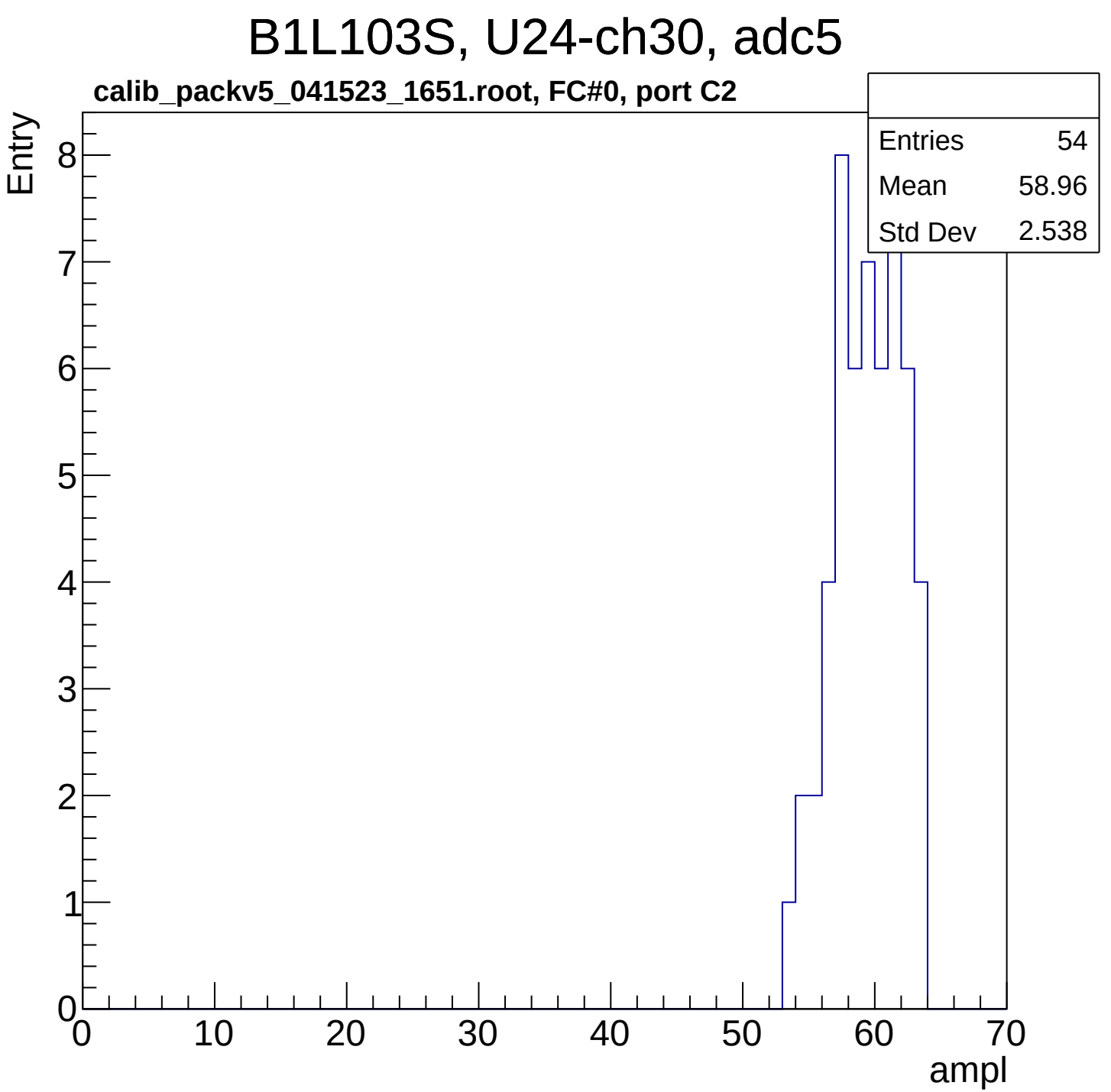
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U24-ch30, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 52.93
Std Dev 3.262
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U24-ch30, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 58.96
Std Dev 2.538
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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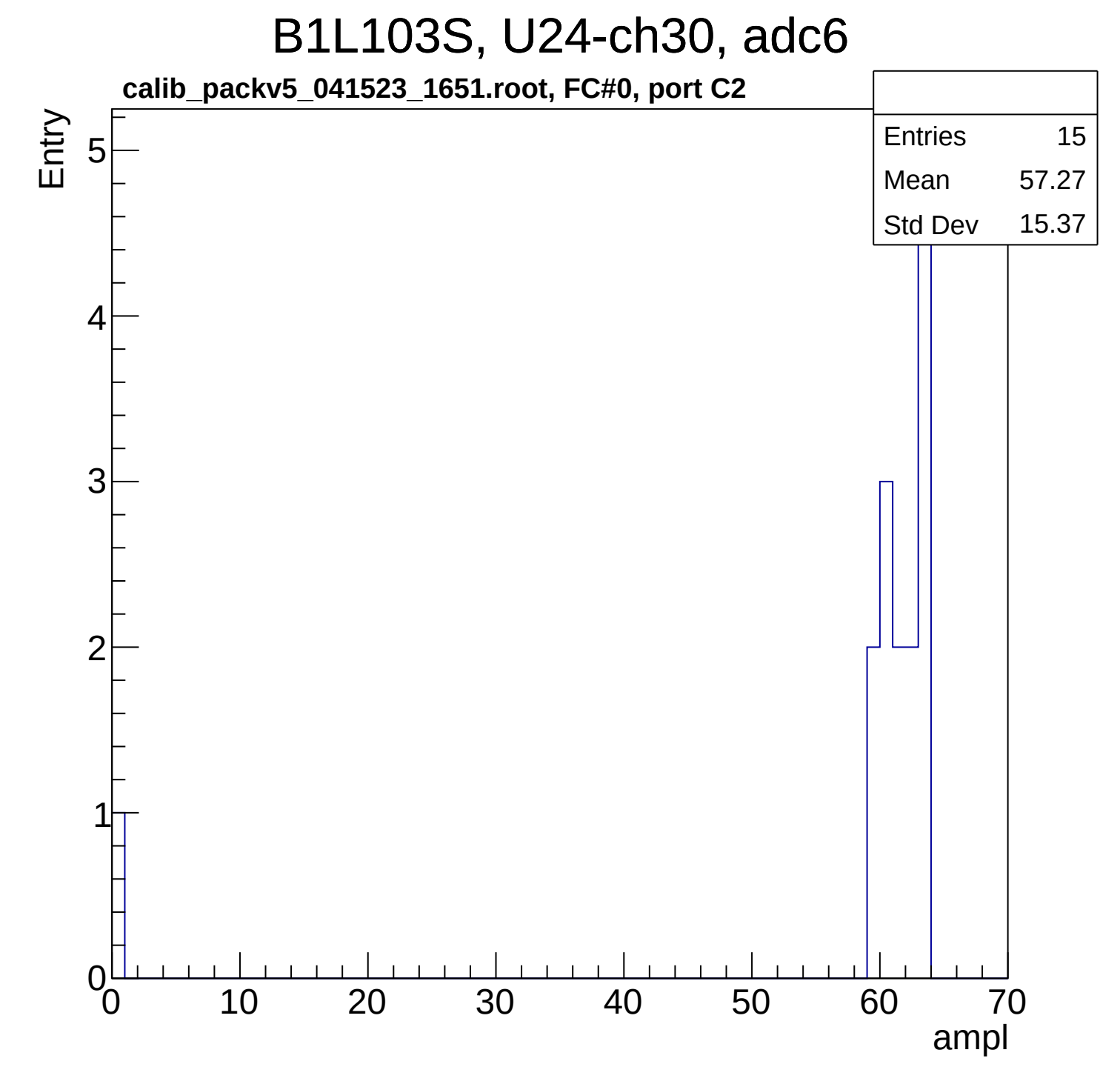
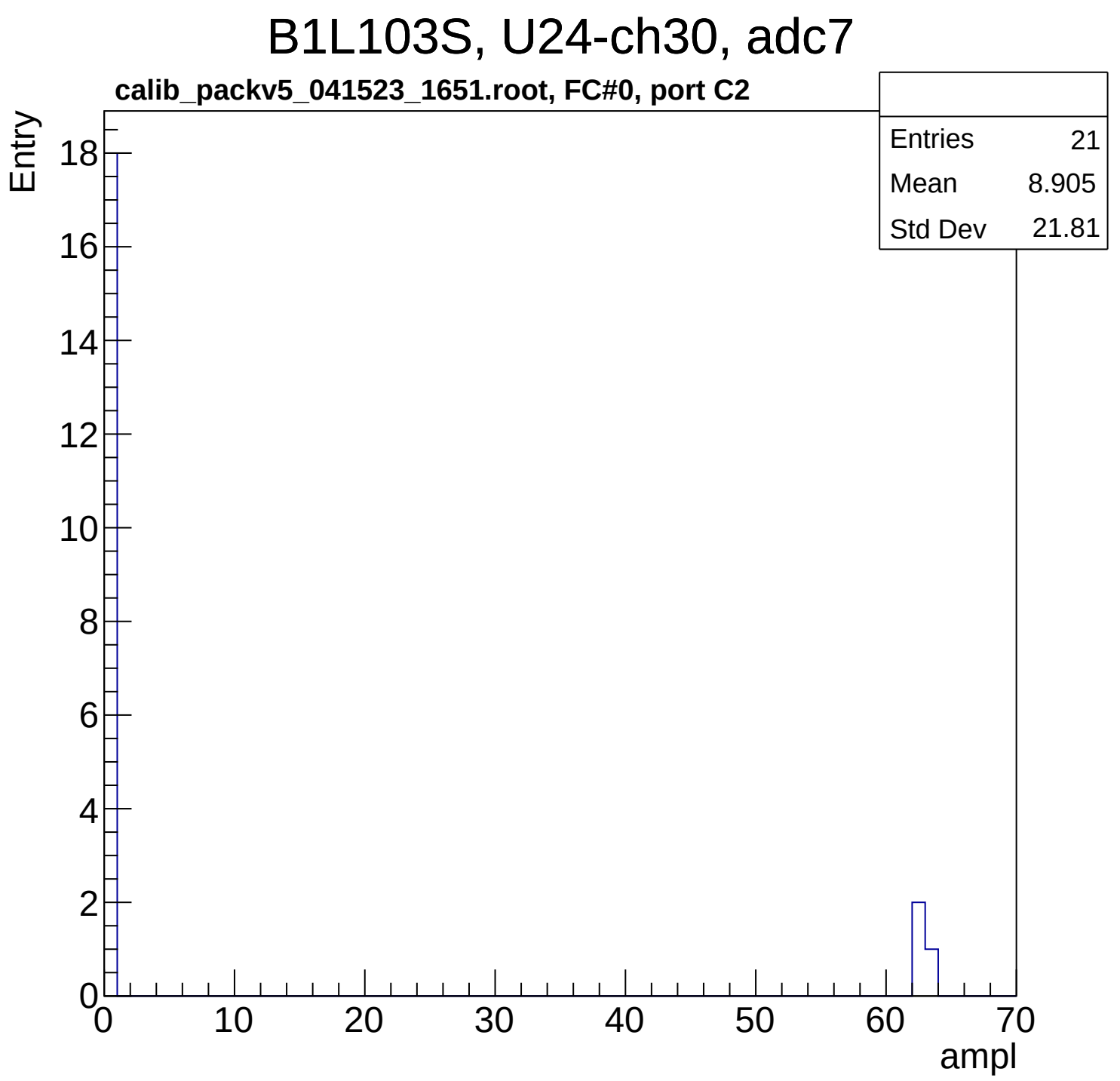
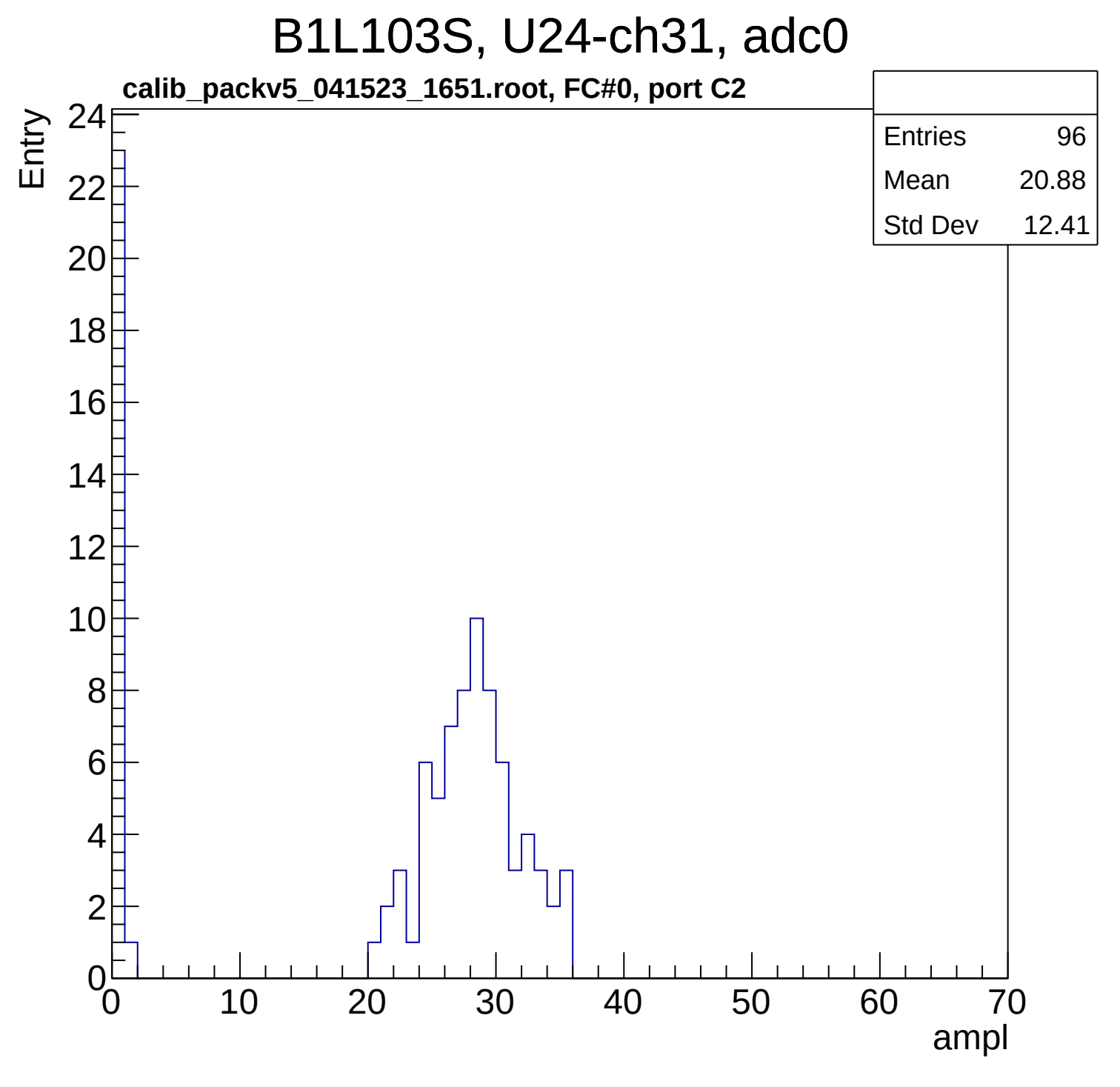

B1L103S, U24-ch30, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 15
Mean 57.27
Std Dev 15.37
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch30, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 8.905
Std Dev 21.81
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch31, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 96
Mean 20.88
Std Dev 12.41
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
22
24
0
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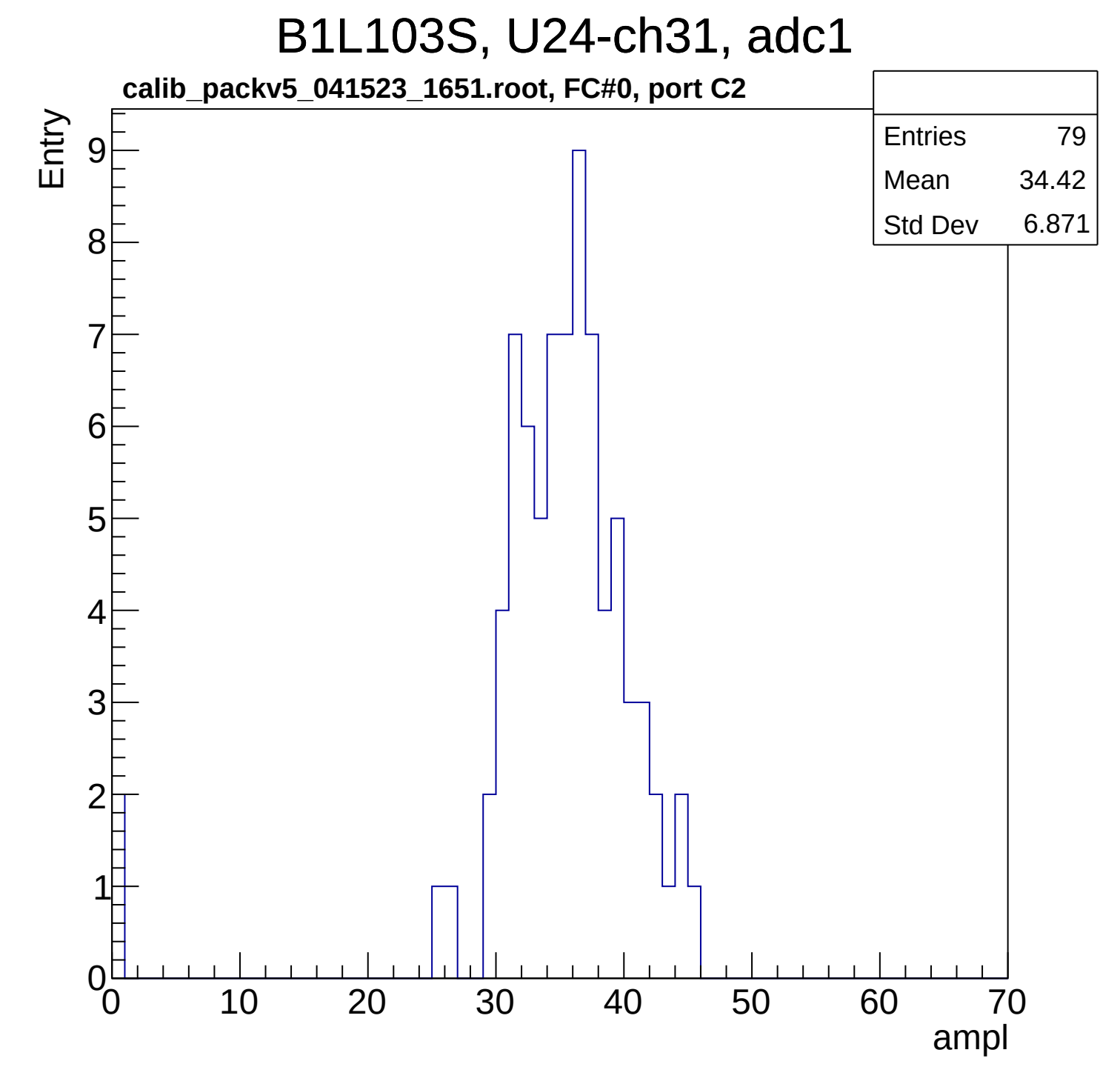
B1L103S, U24-ch31, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 34.42
Std Dev 6.871
Entry
ampl
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2
3
4
5
6
7
8
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0
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40
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60
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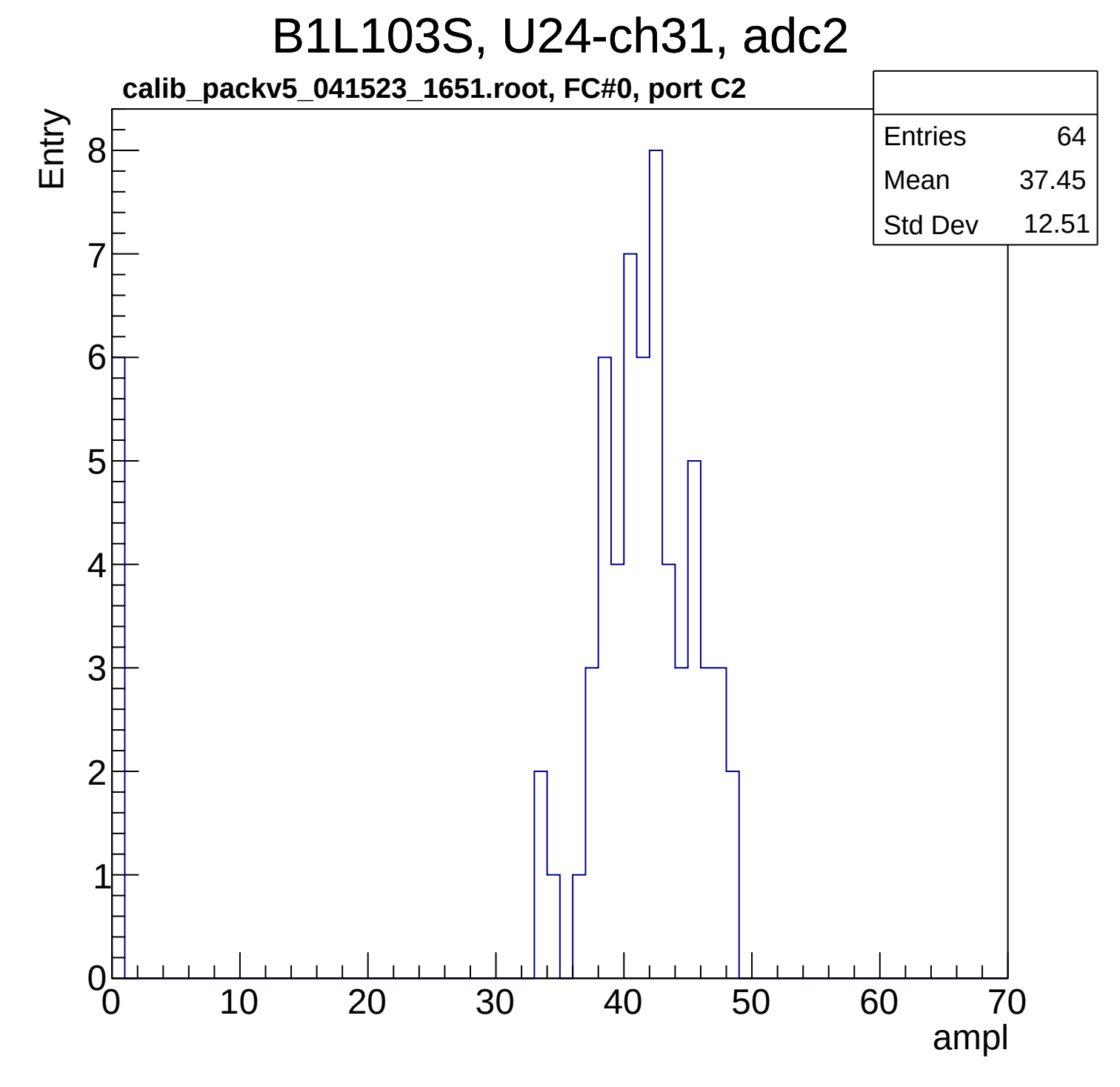
B1L103S, U24-ch31, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 37.45
Std Dev 12.51
Entry
ampl
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1
2
3
4
5
6
7
8
0
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40
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60
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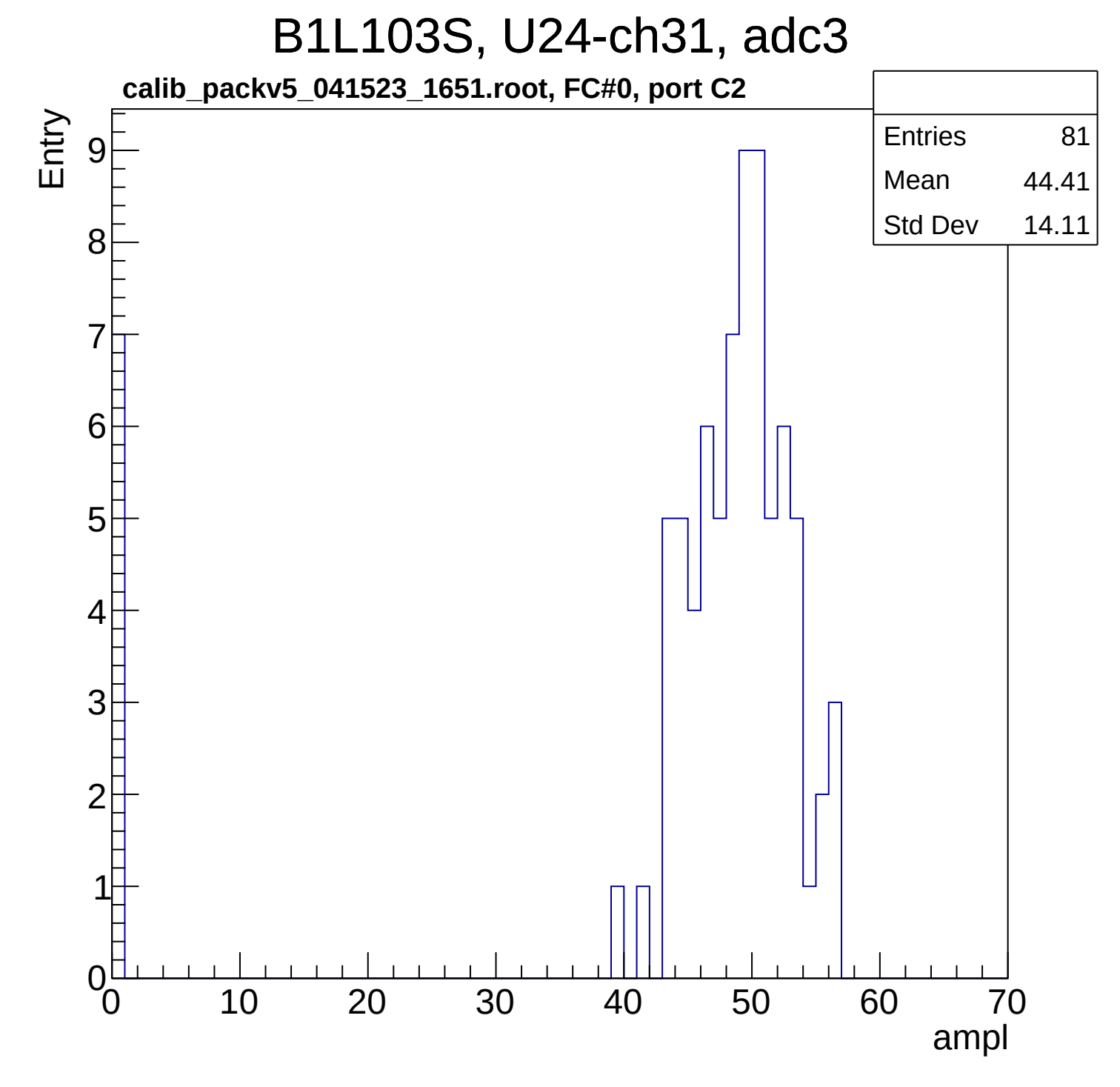
B1L103S, U24-ch31, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 44.41
Std Dev 14.11
Entry
ampl
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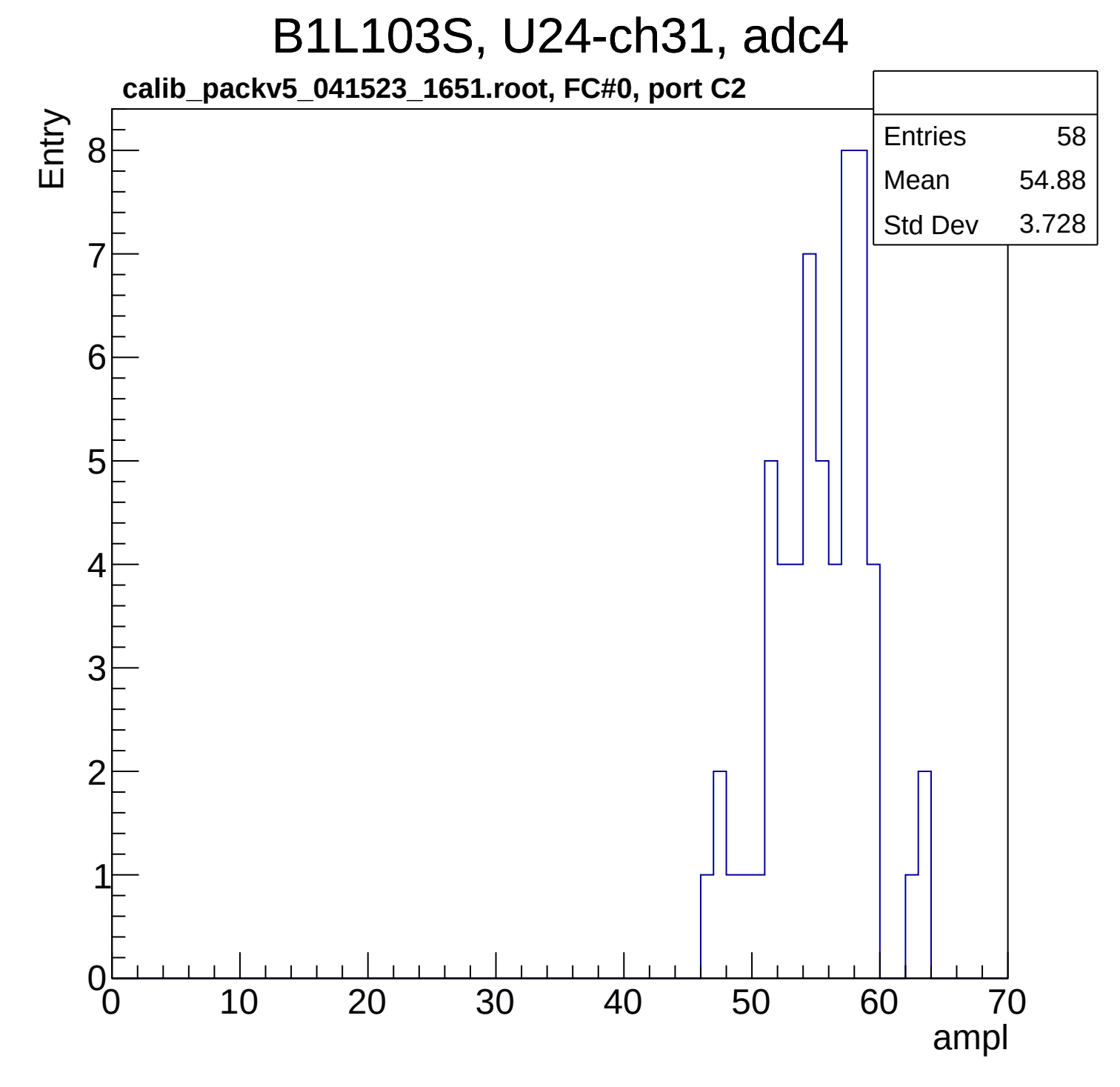
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9


B1L103S, U24-ch31, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 54.88
Std Dev 3.728
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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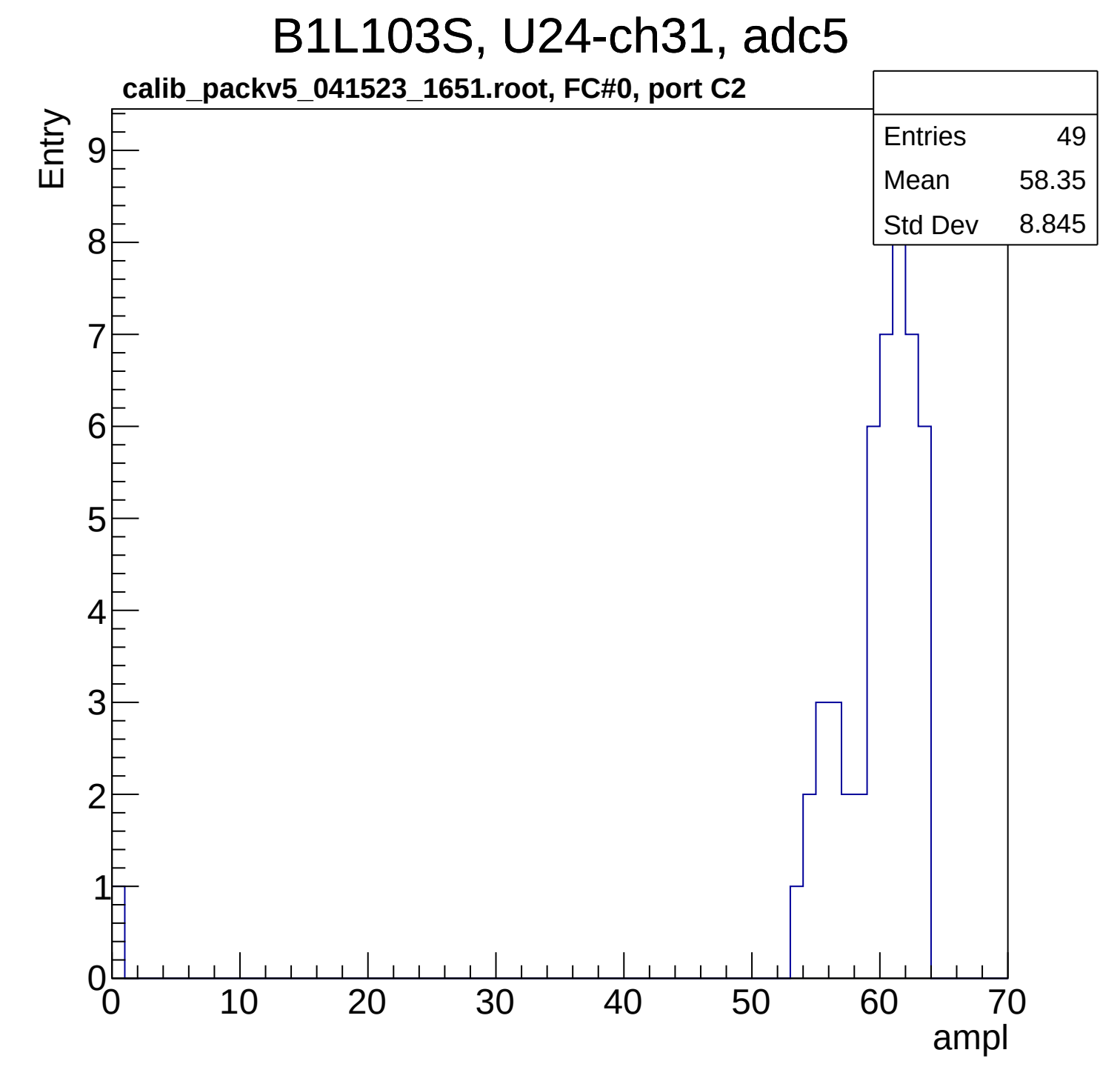
B1L103S, U24-ch31, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 58.35
Std Dev 8.845
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
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40
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60
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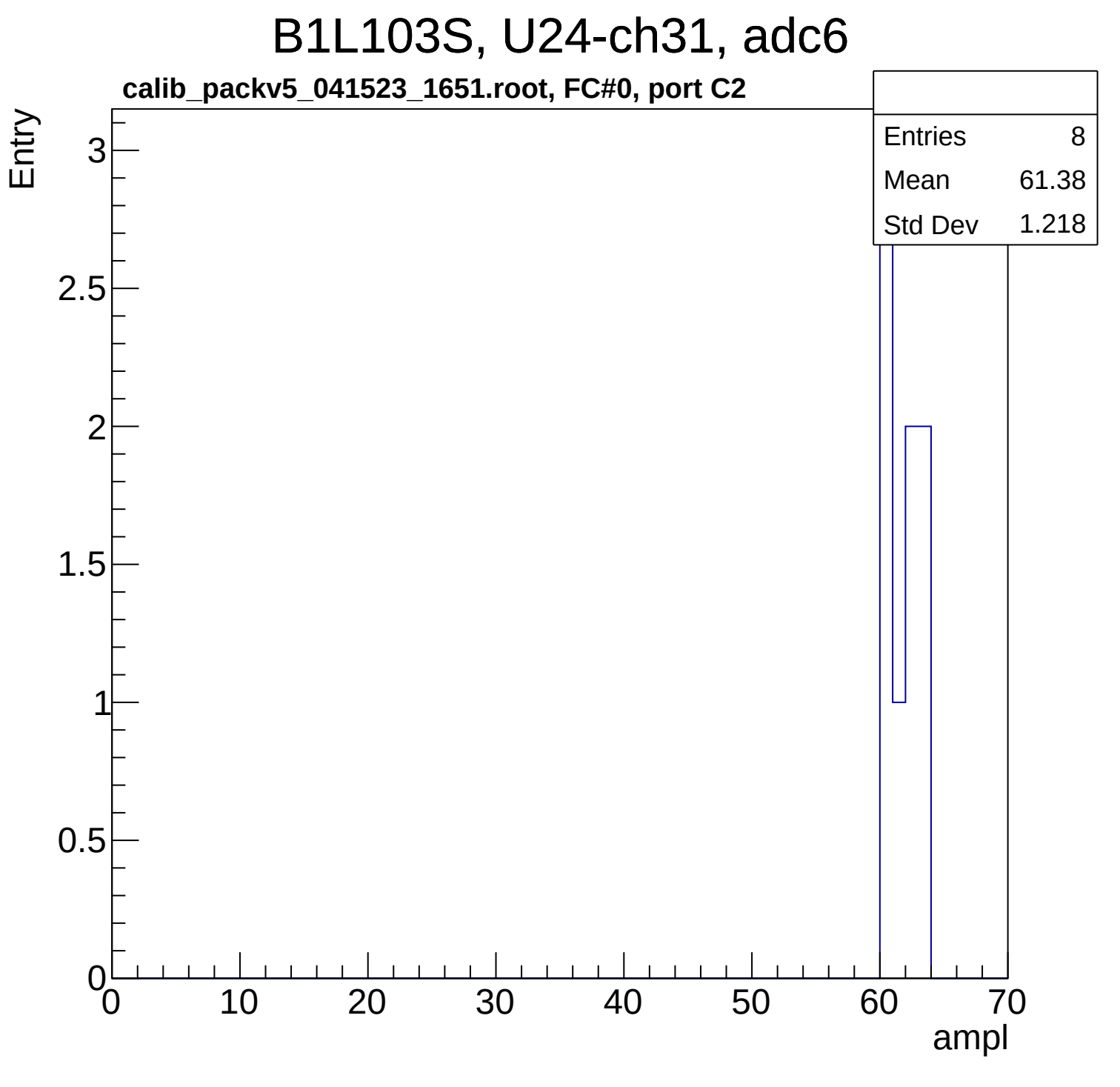
B1L103S, U24-ch31, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 61.38
Std Dev 1.218
Entry
ampl
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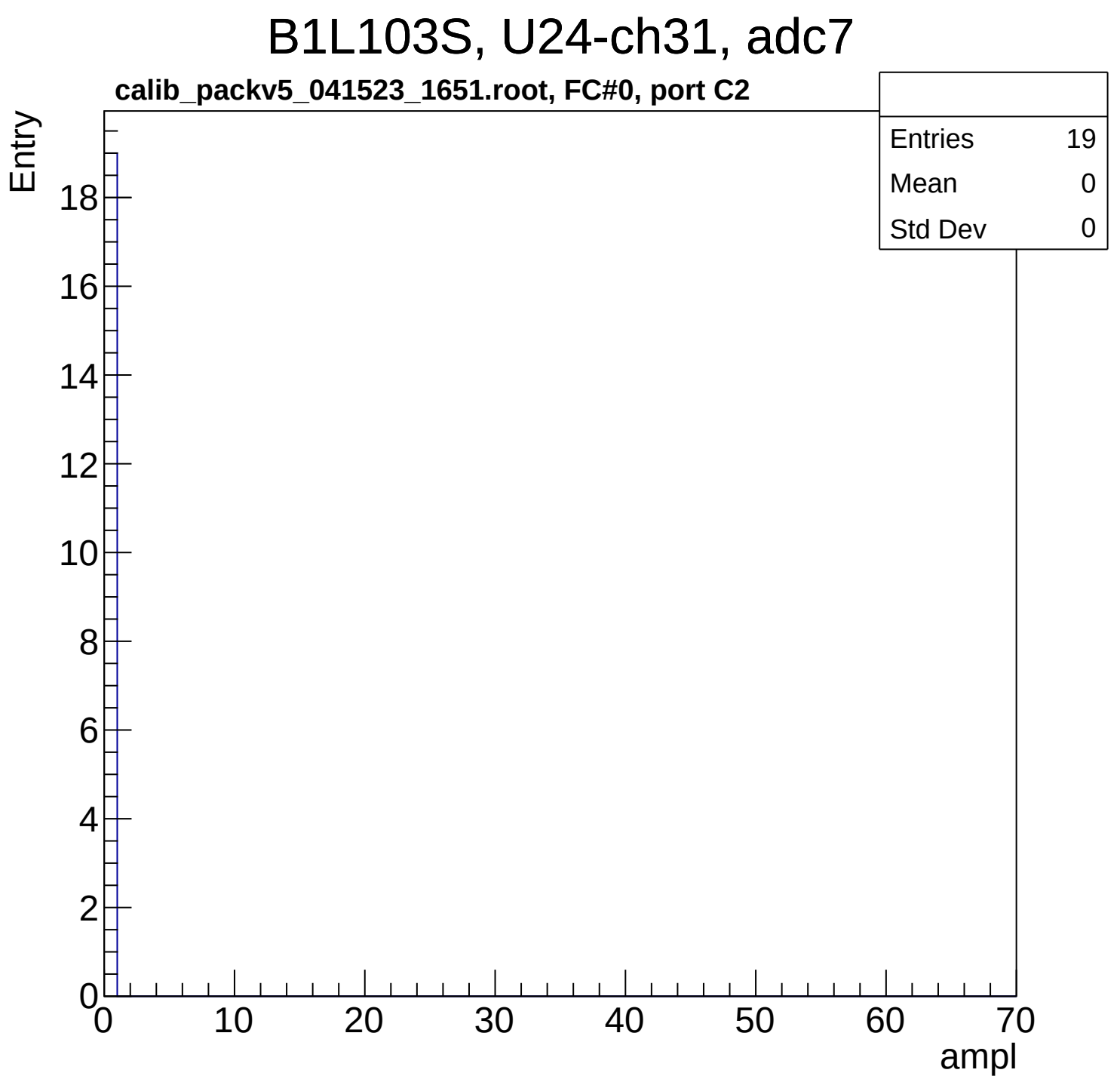
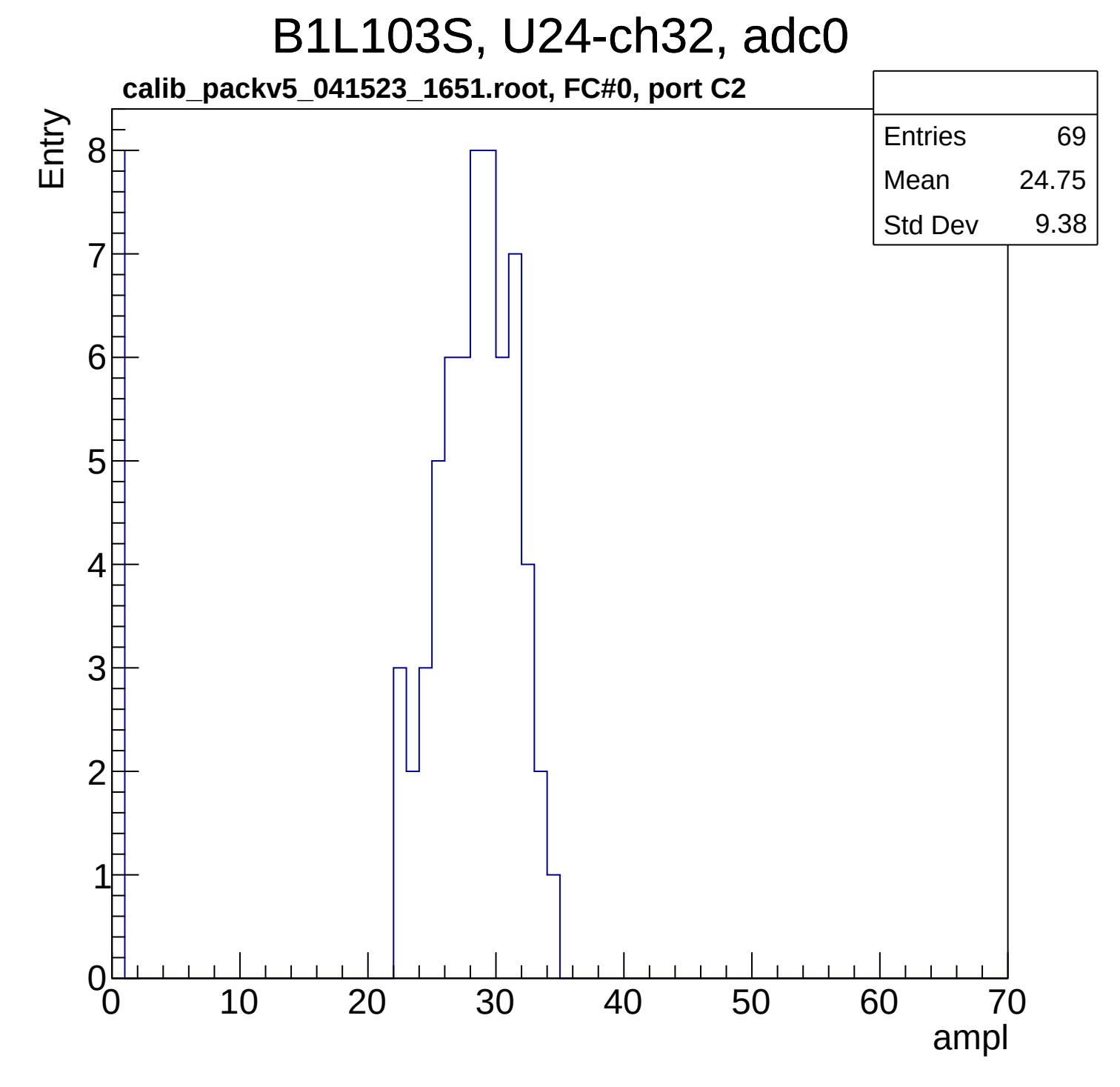
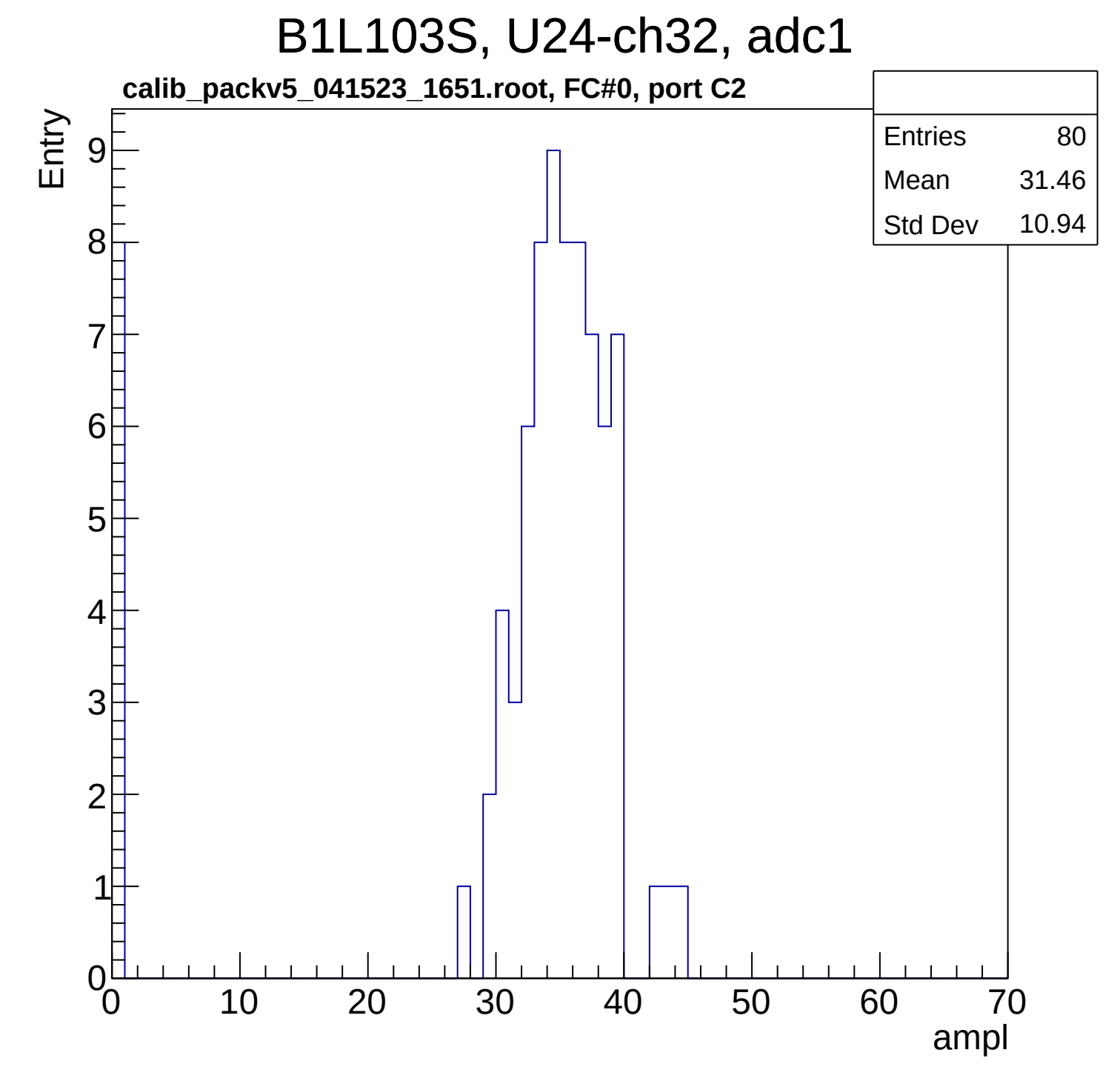
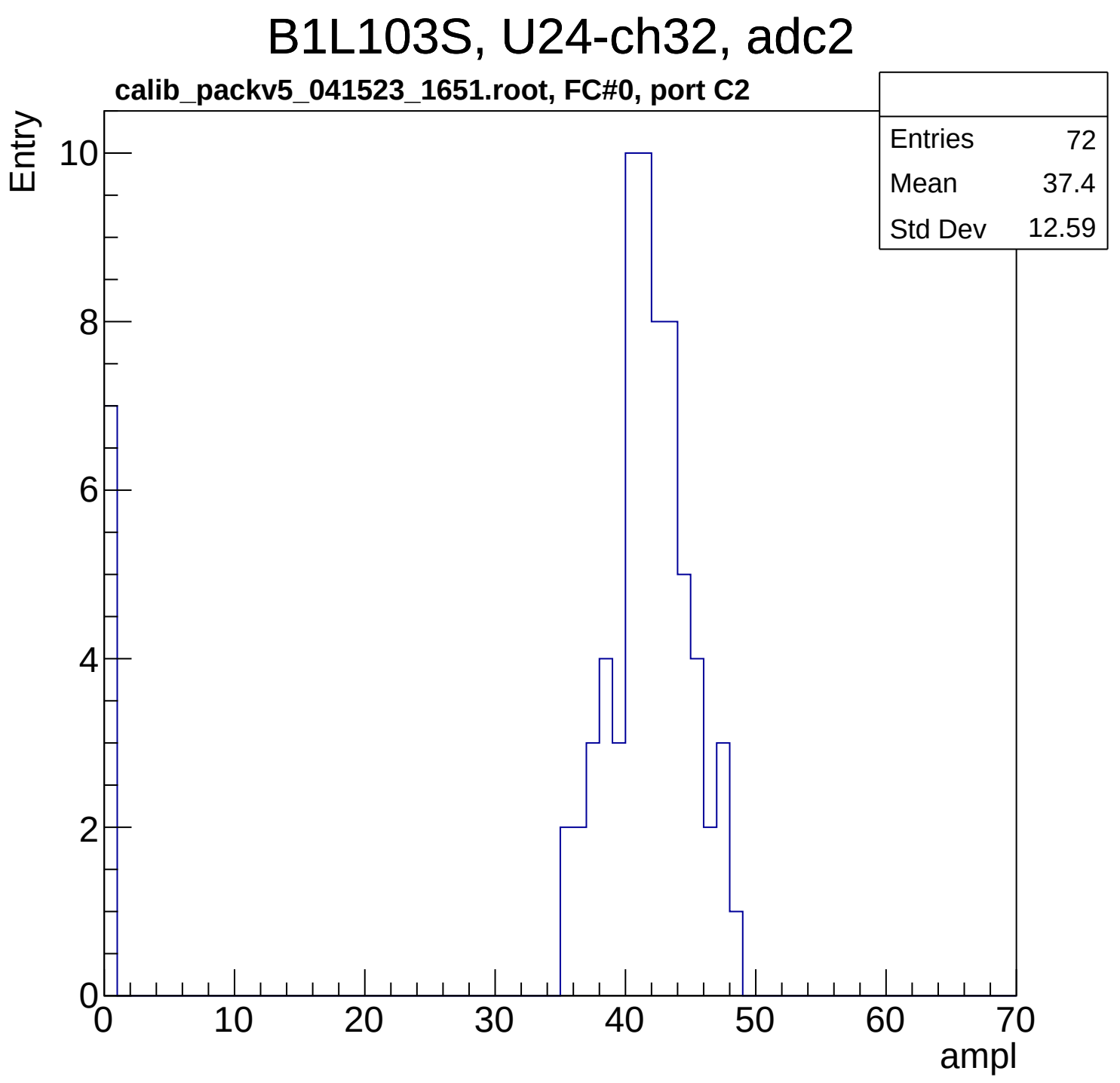
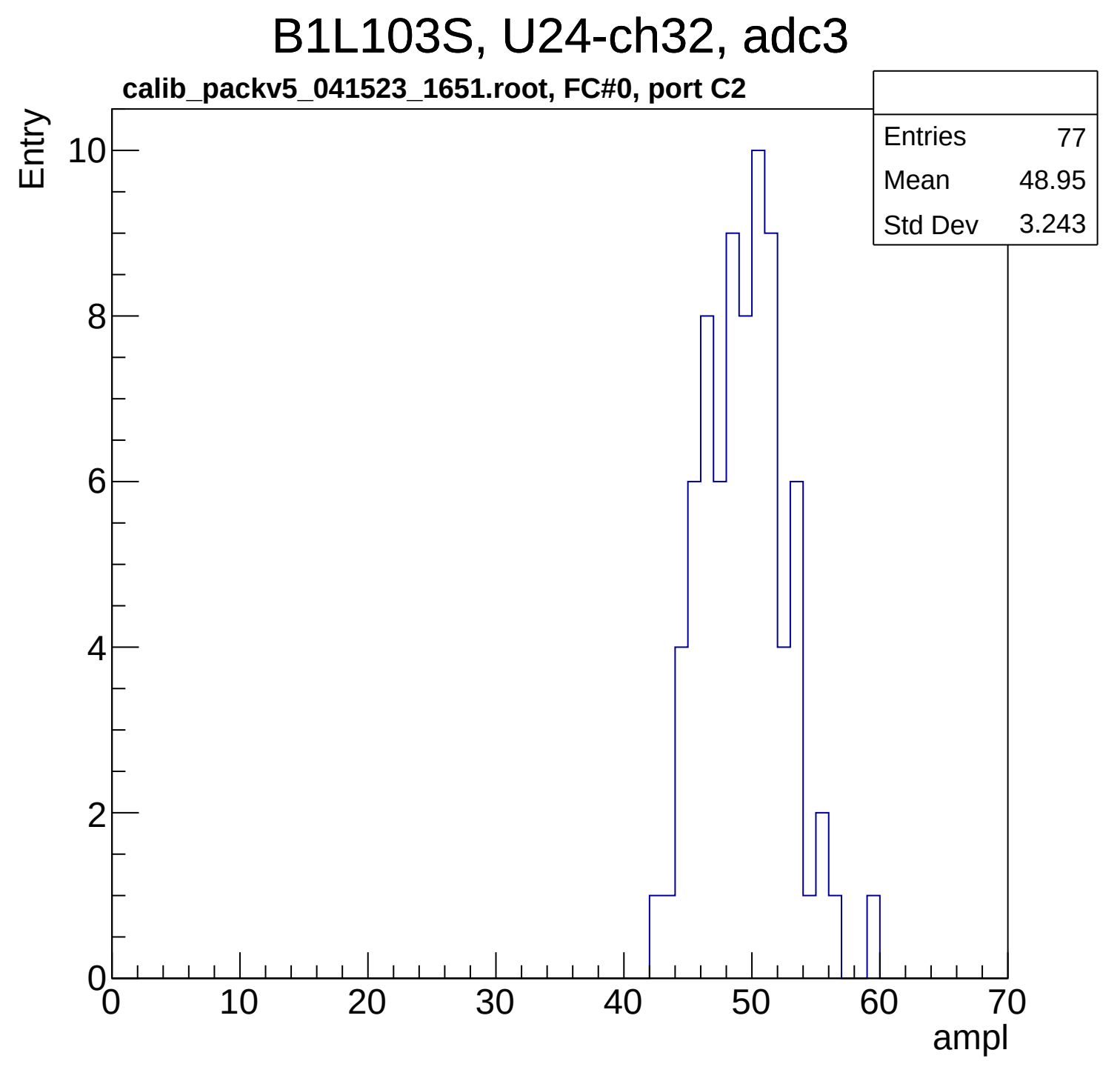
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

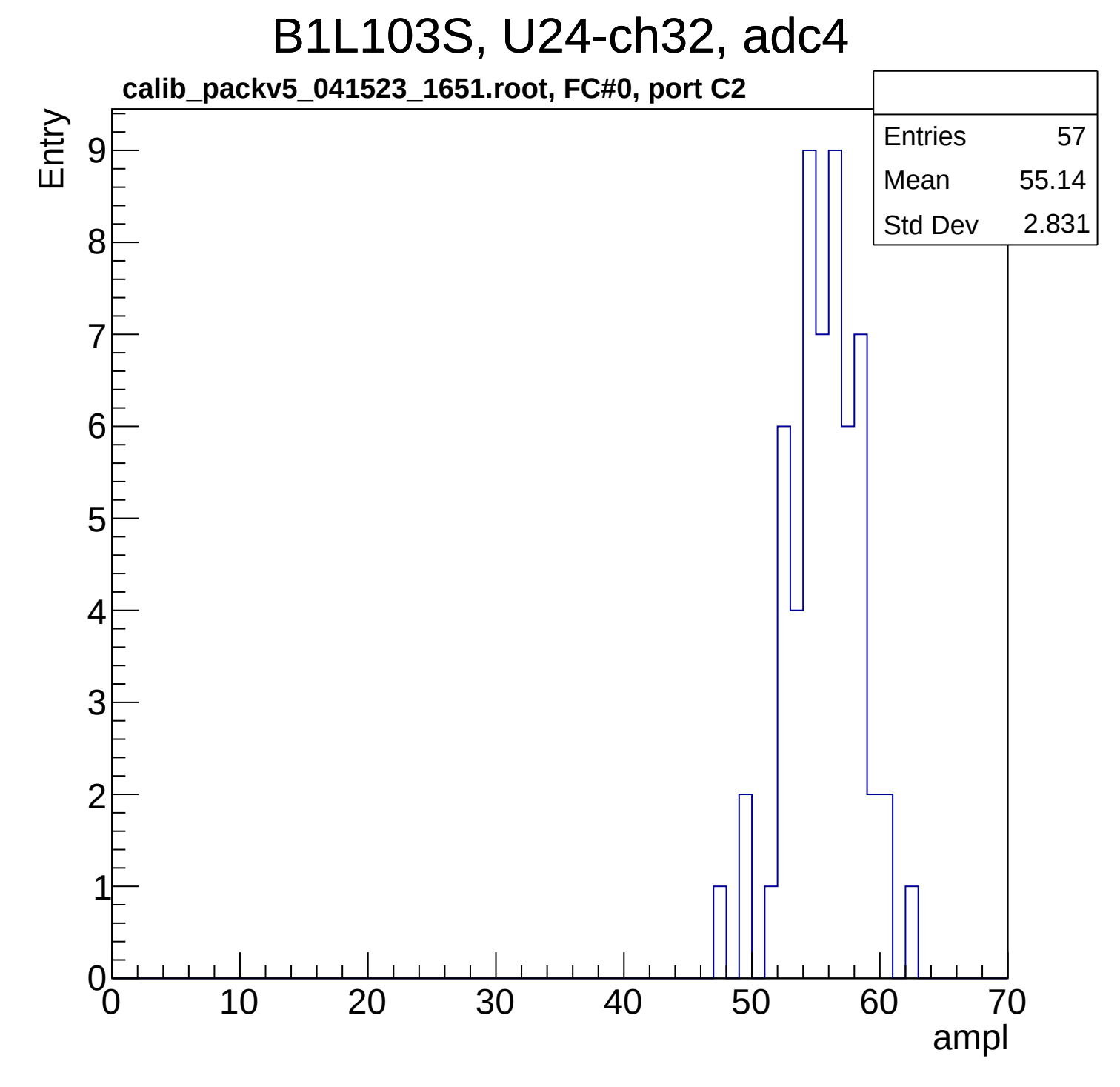

B1L103S, U24-ch31, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch32, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 24.75
Std Dev 9.38
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U24-ch32, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 31.46
Std Dev 10.94
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U24-ch32, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 37.4
Std Dev 12.59
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch32, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 48.95
Std Dev 3.243
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U24-ch32, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 55.14
Std Dev 2.831
Entry
ampl
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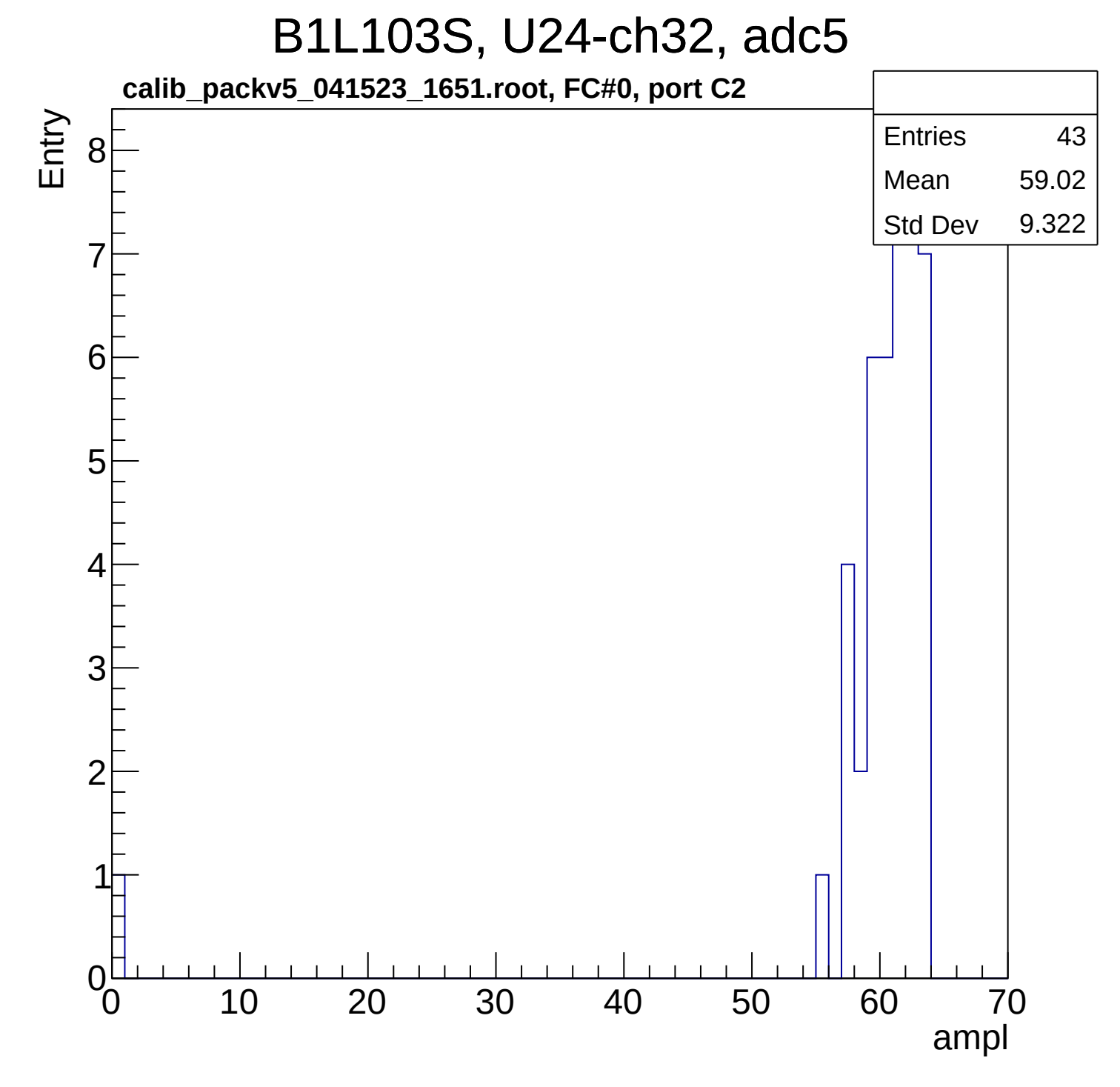
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U24-ch32, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 43
Mean 59.02
Std Dev 9.322
Entry
ampl
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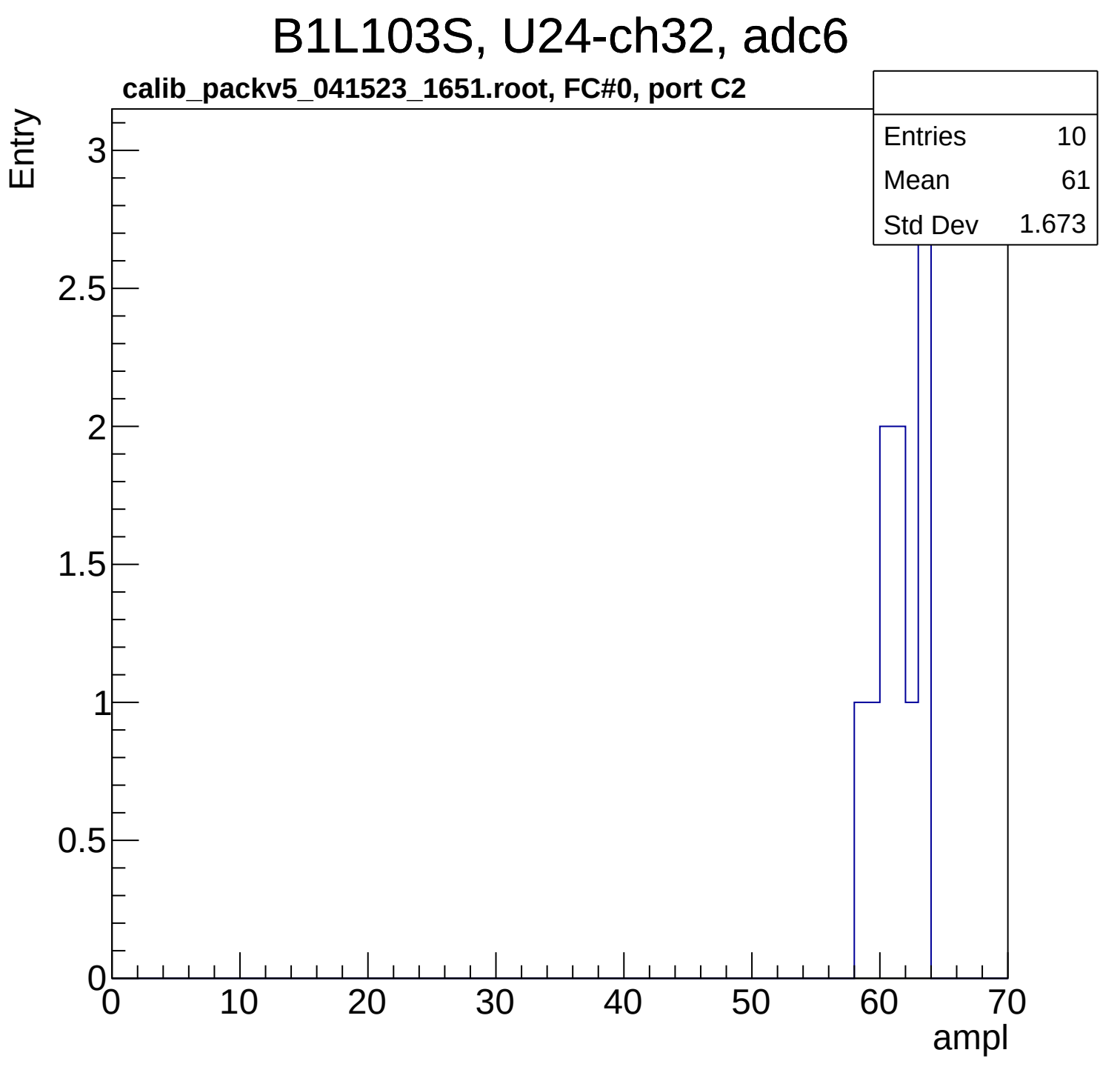
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U24-ch32, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 61
Std Dev 1.673
Entry
ampl
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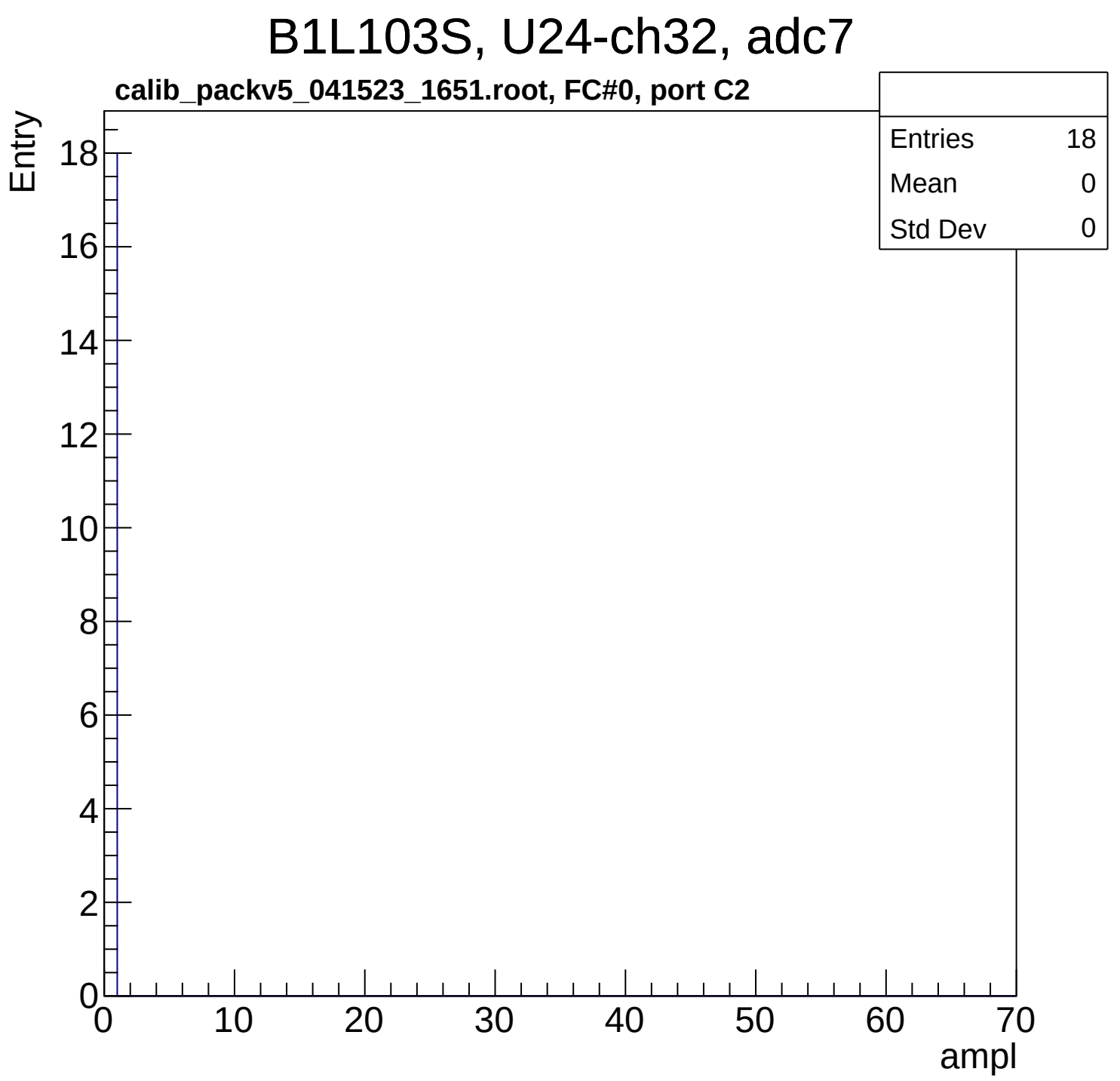
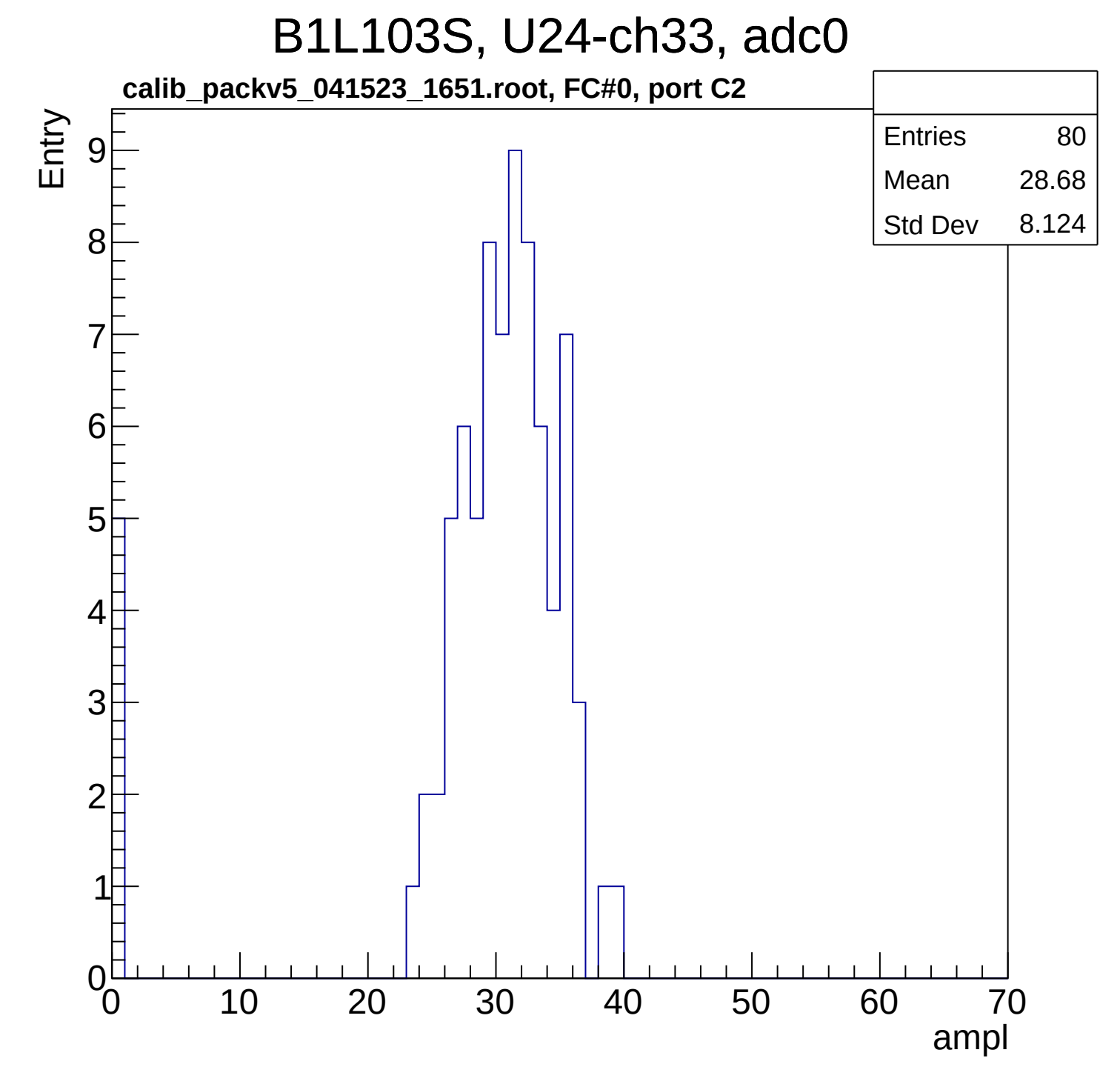
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U24-ch32, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch33, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 28.68
Std Dev 8.124
Entry
ampl
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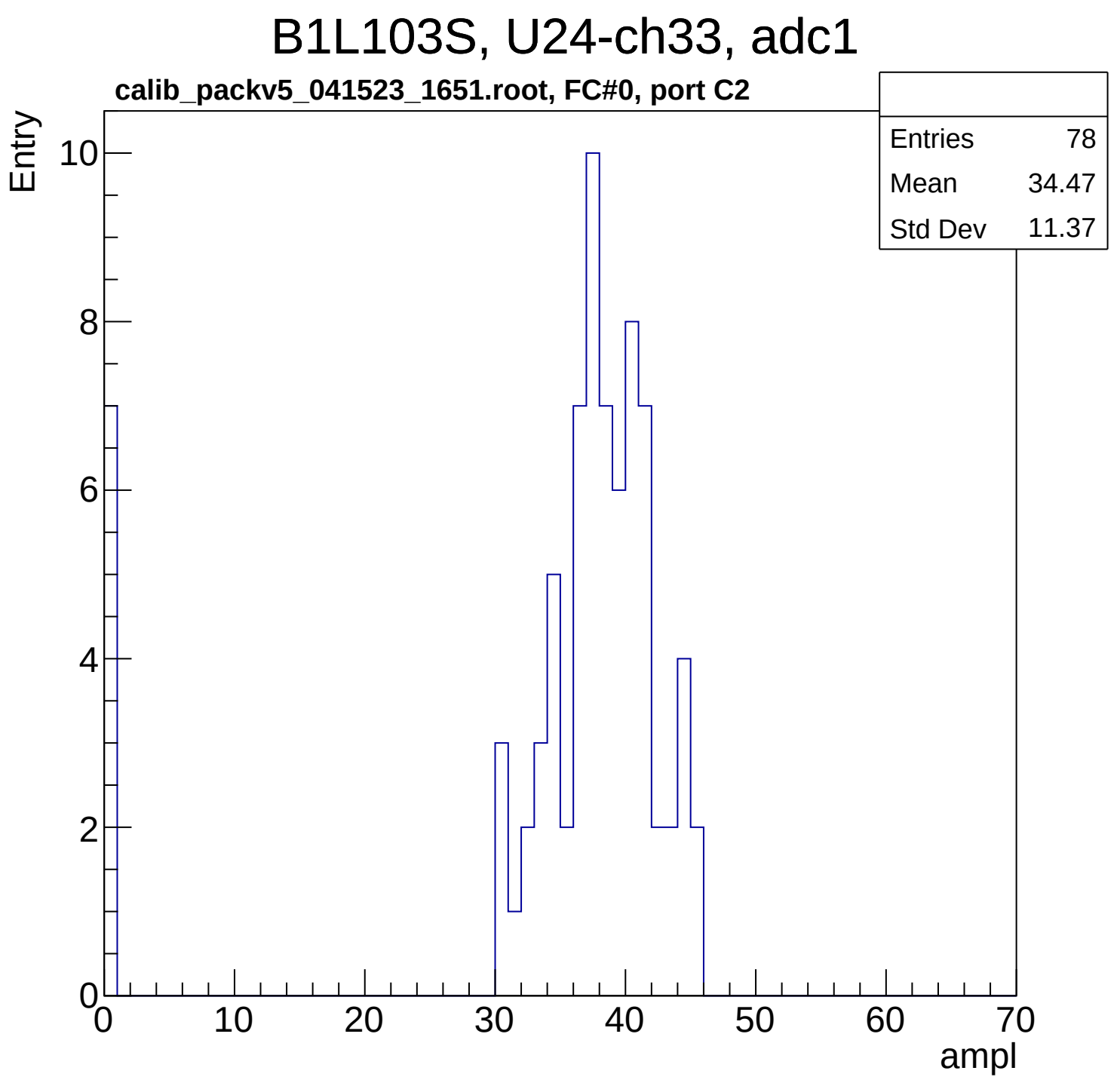
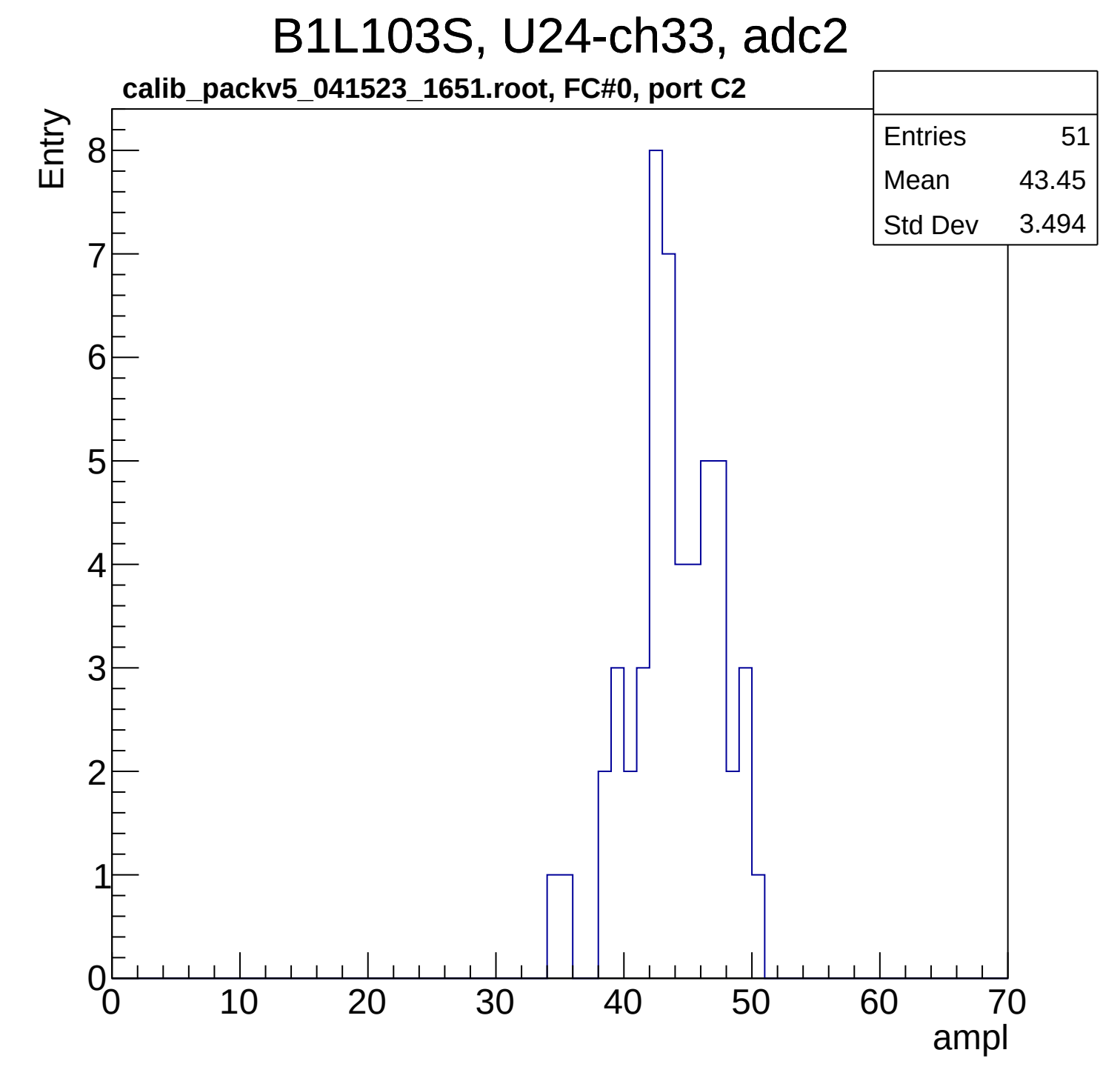
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U24-ch33, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 34.47
Std Dev 11.37
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U24-ch33, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 43.45
Std Dev 3.494
Entry
ampl
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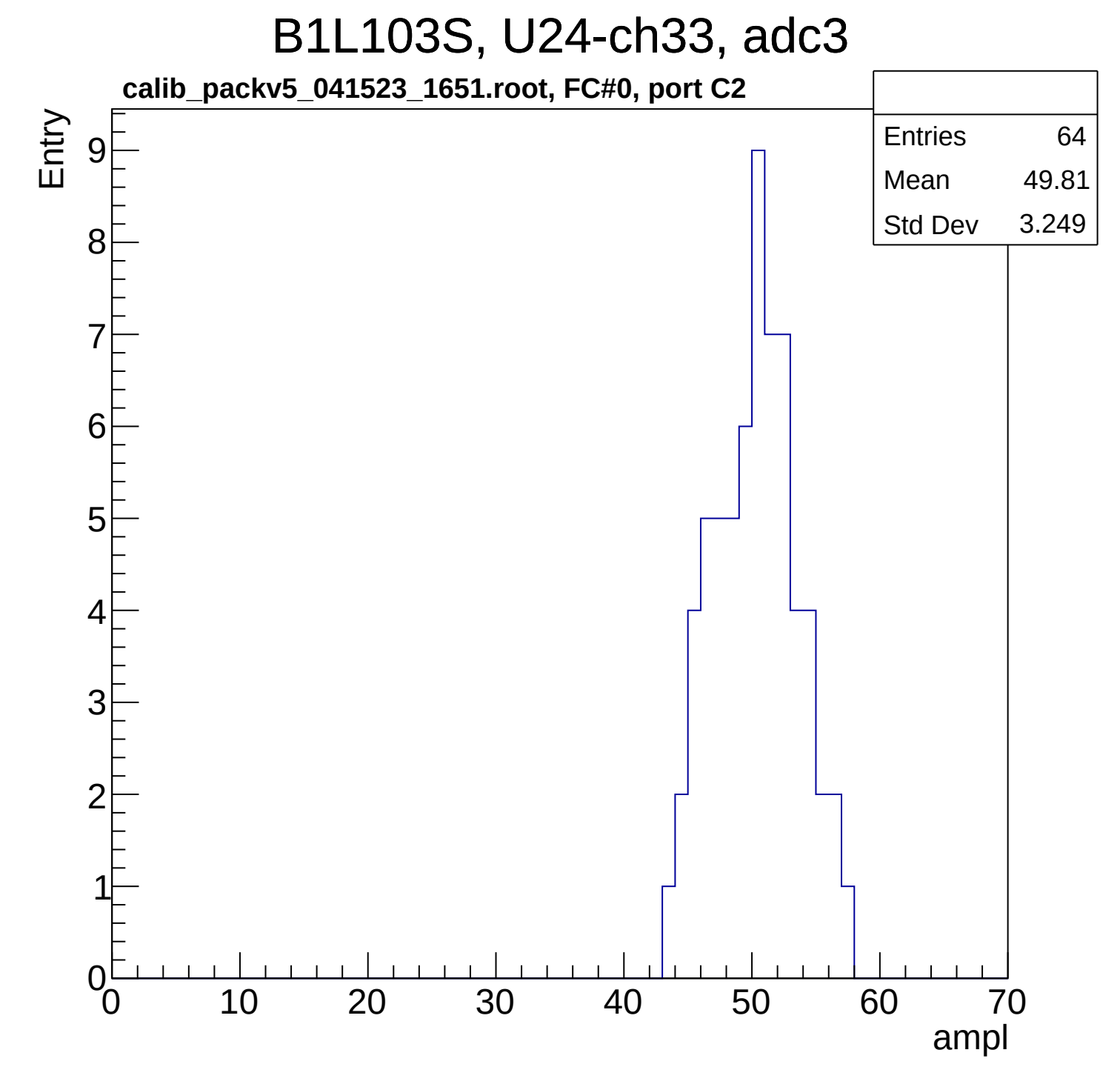
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U24-ch33, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 49.81
Std Dev 3.249
Entry
ampl
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2
3
4
5
6
7
8
9
0
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60
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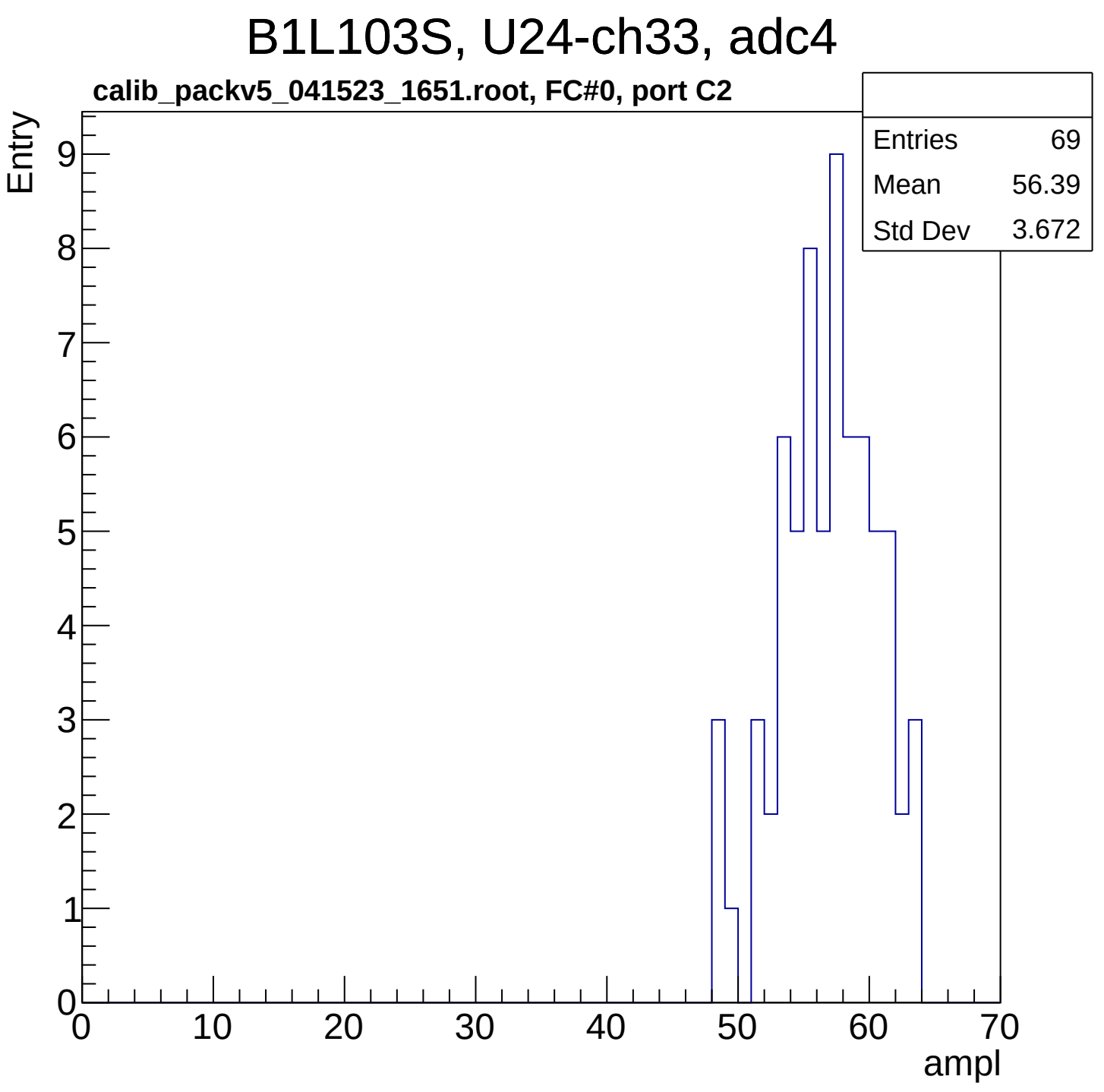
B1L103S, U24-ch33, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 56.39
Std Dev 3.672
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
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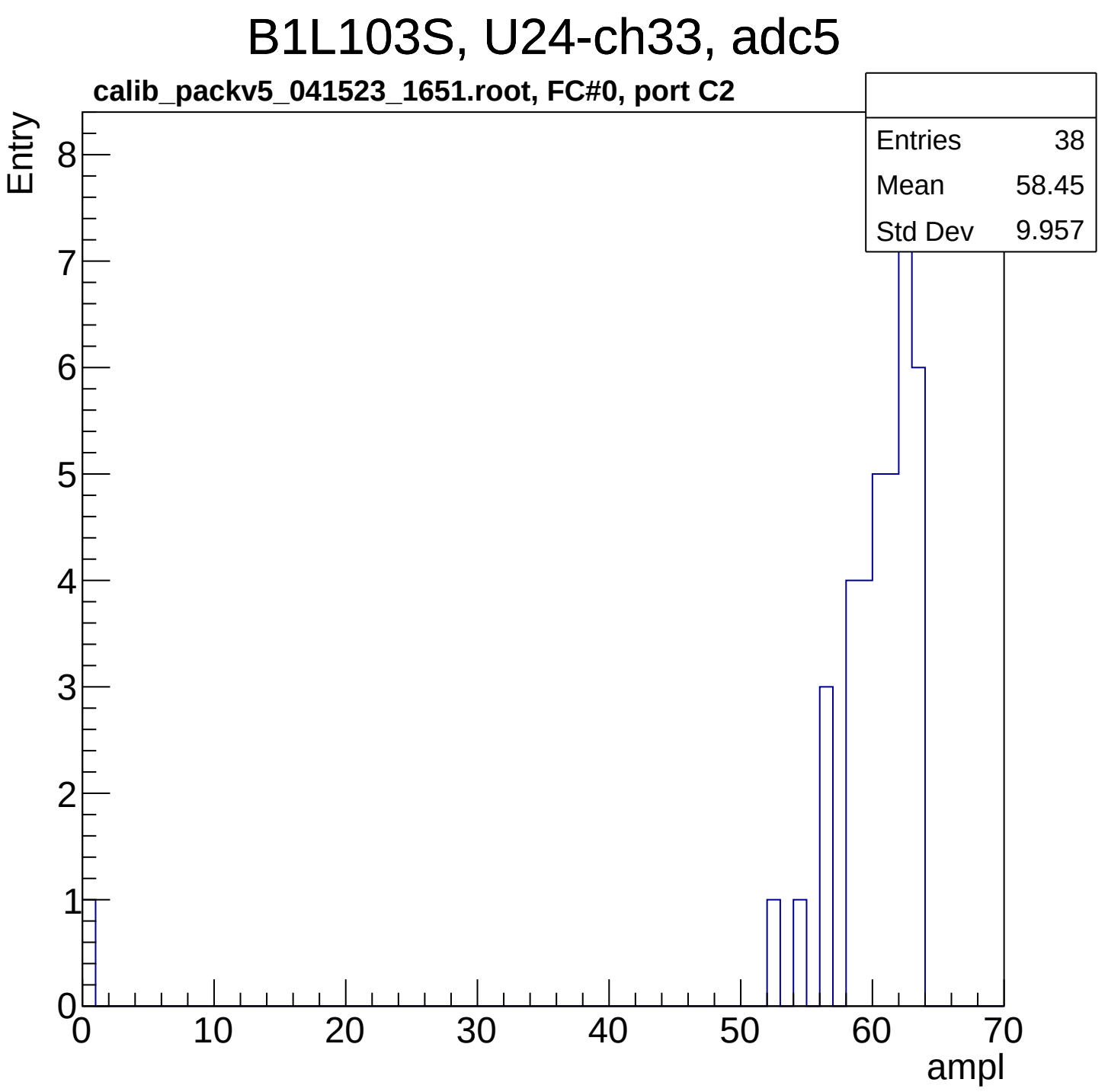
60
70


B1L103S, U24-ch33, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 38
Mean 58.45
Std Dev 9.957
Entry
ampl
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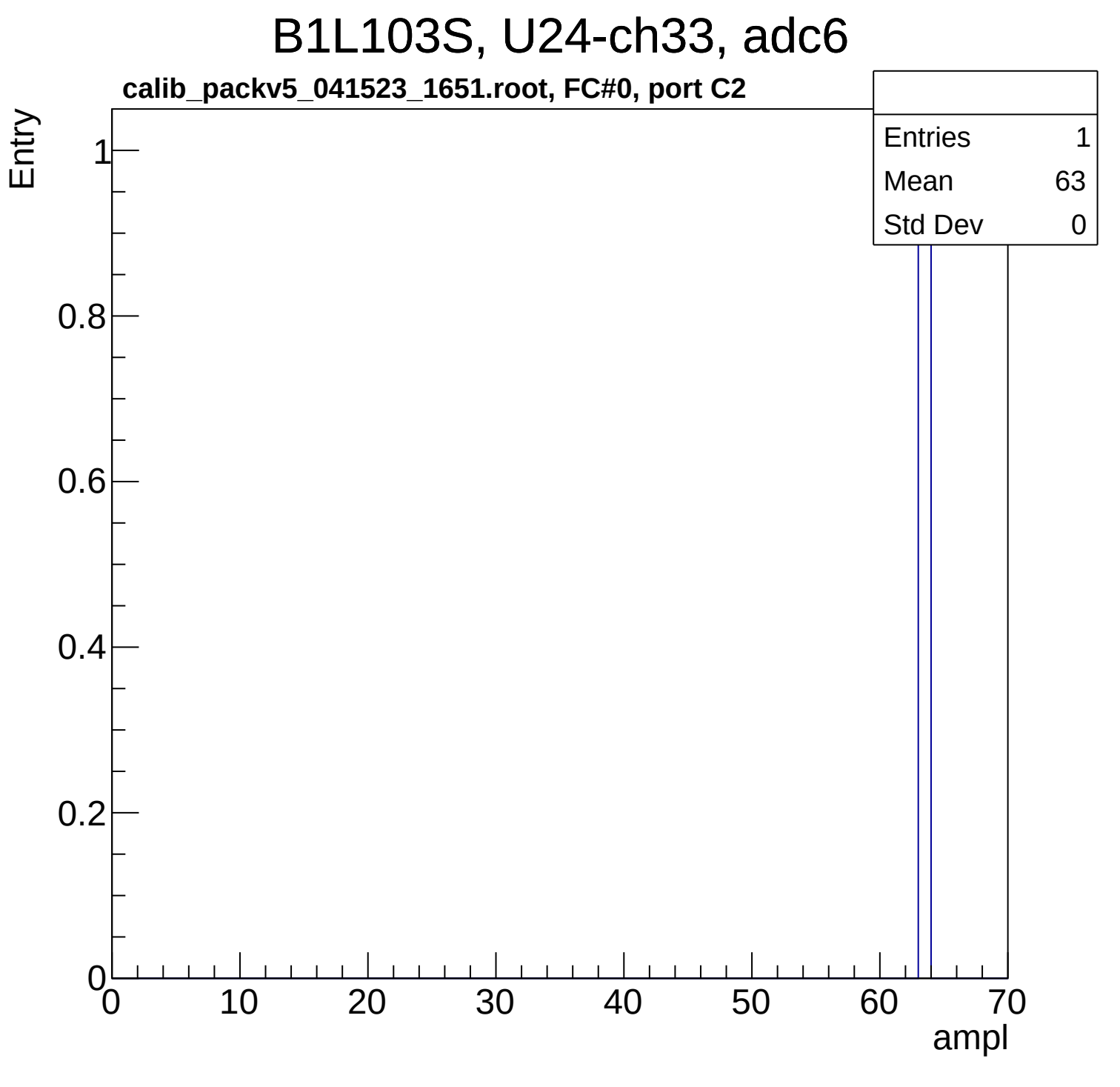
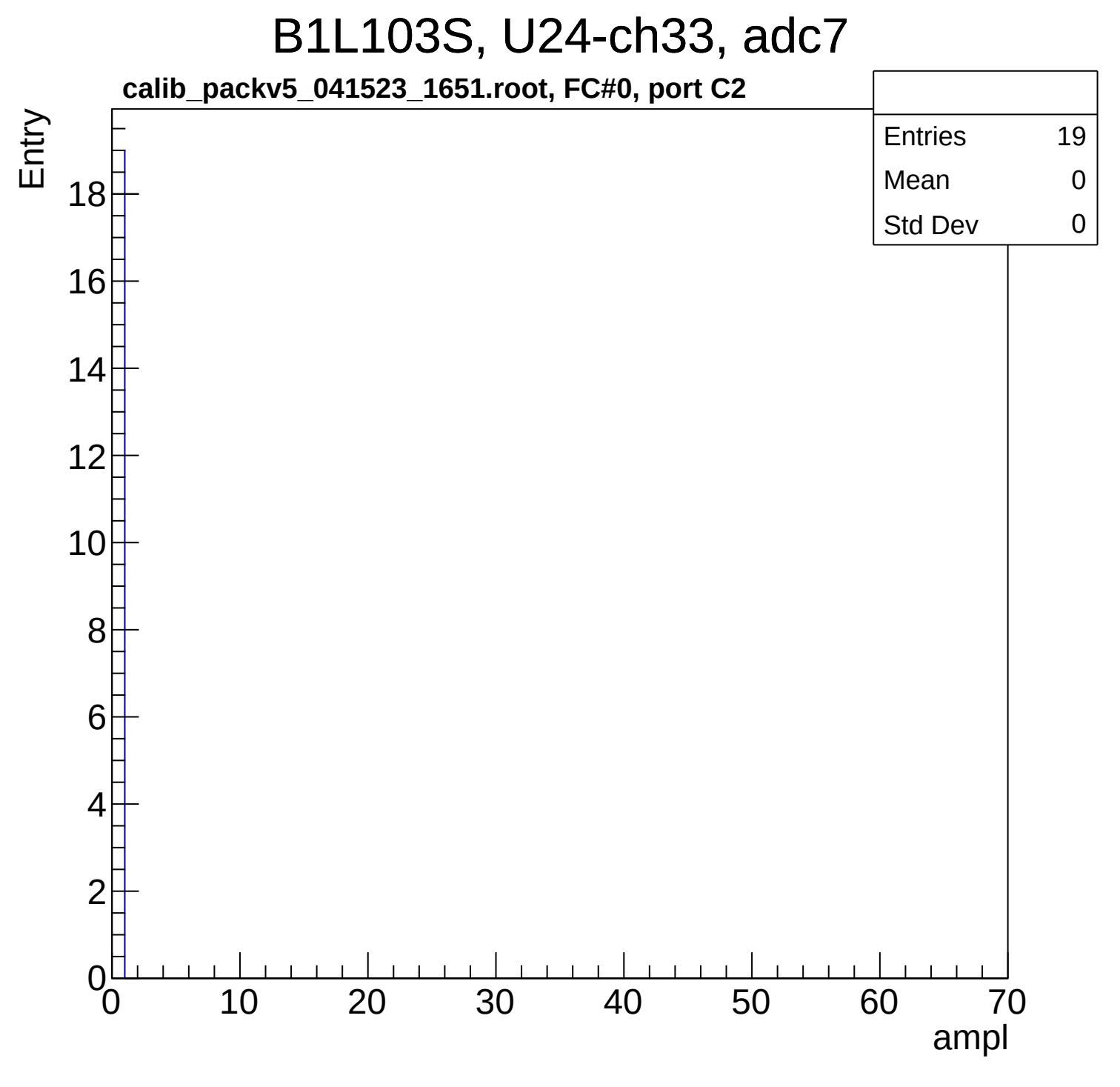
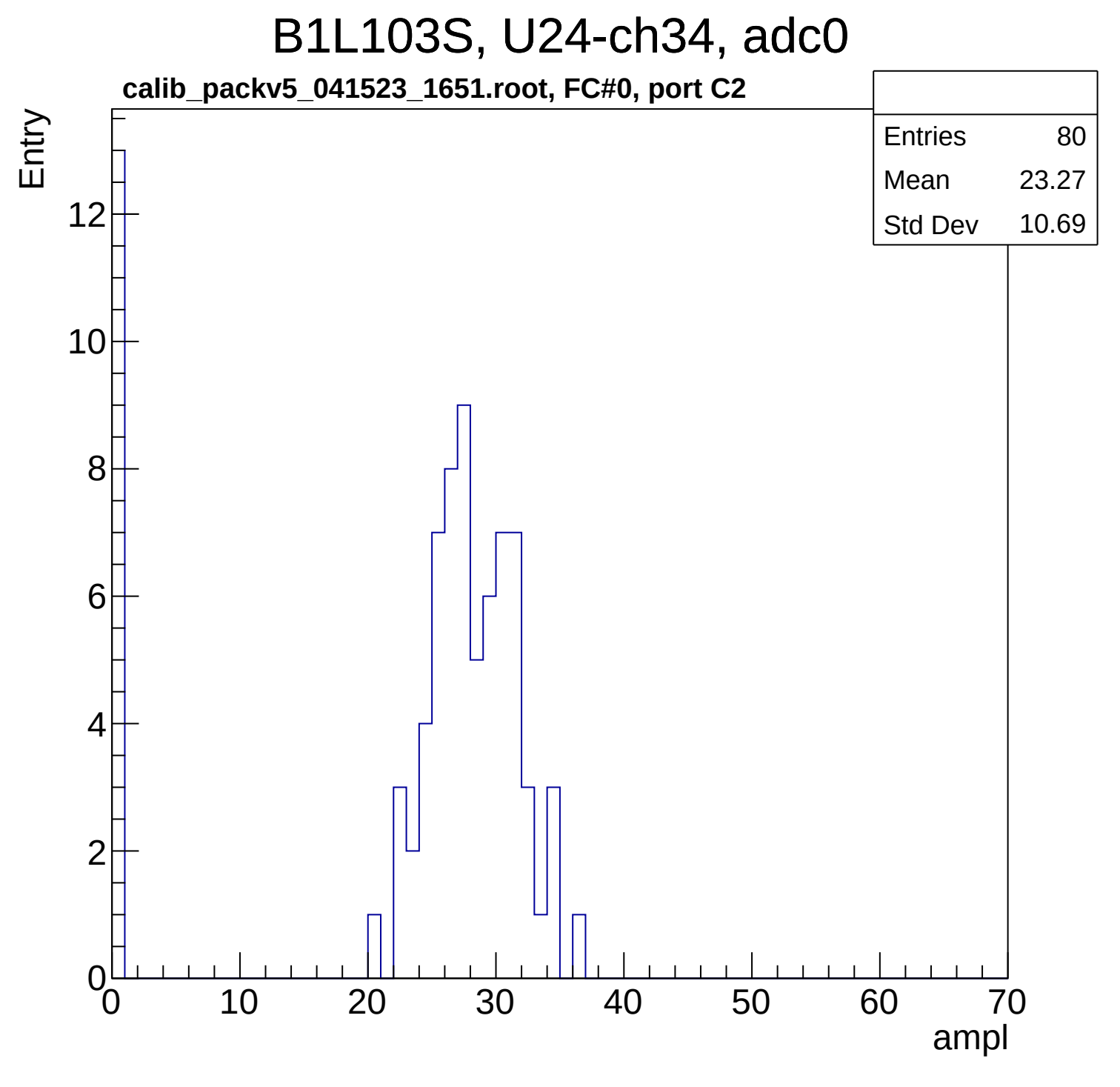
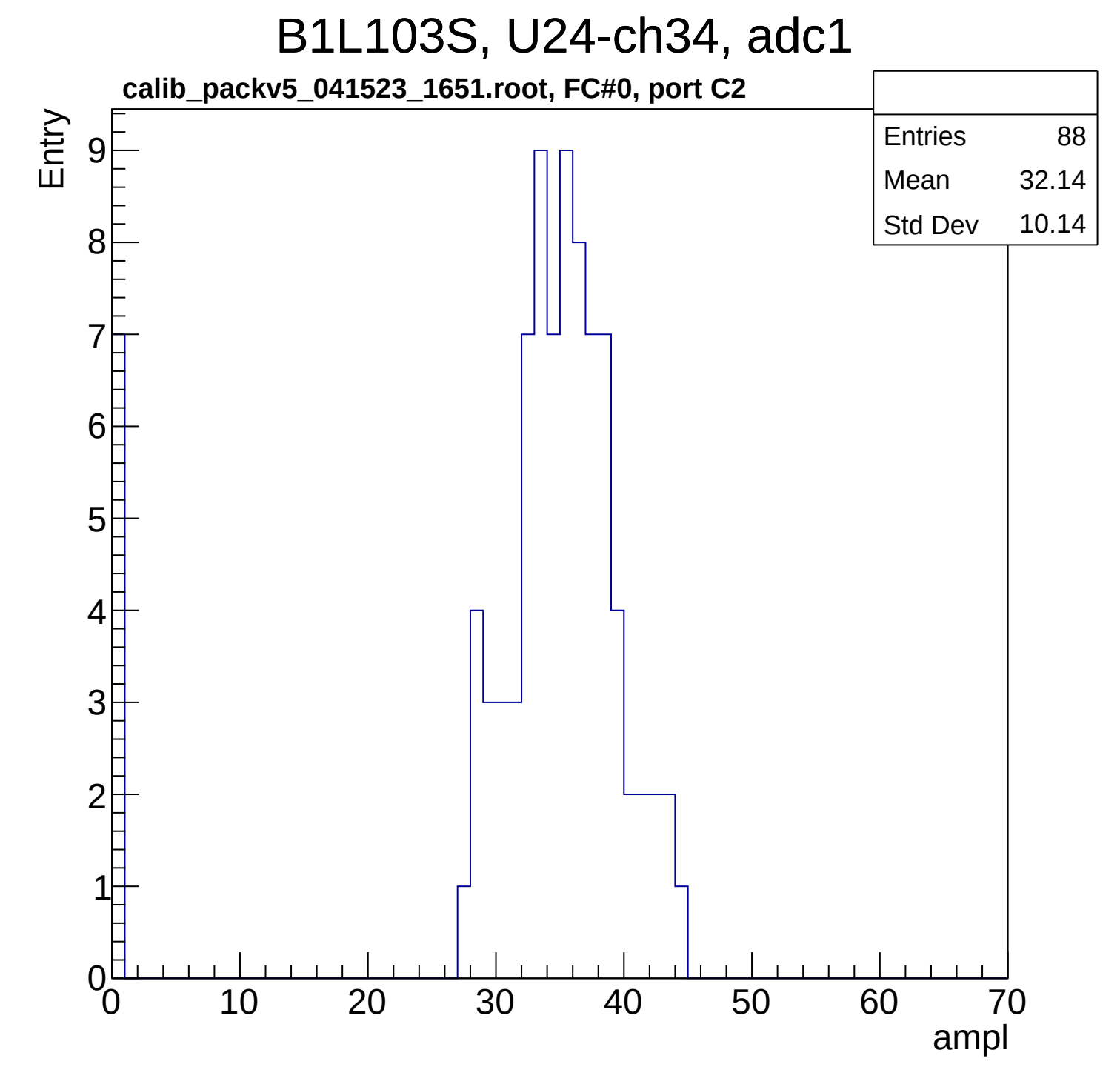
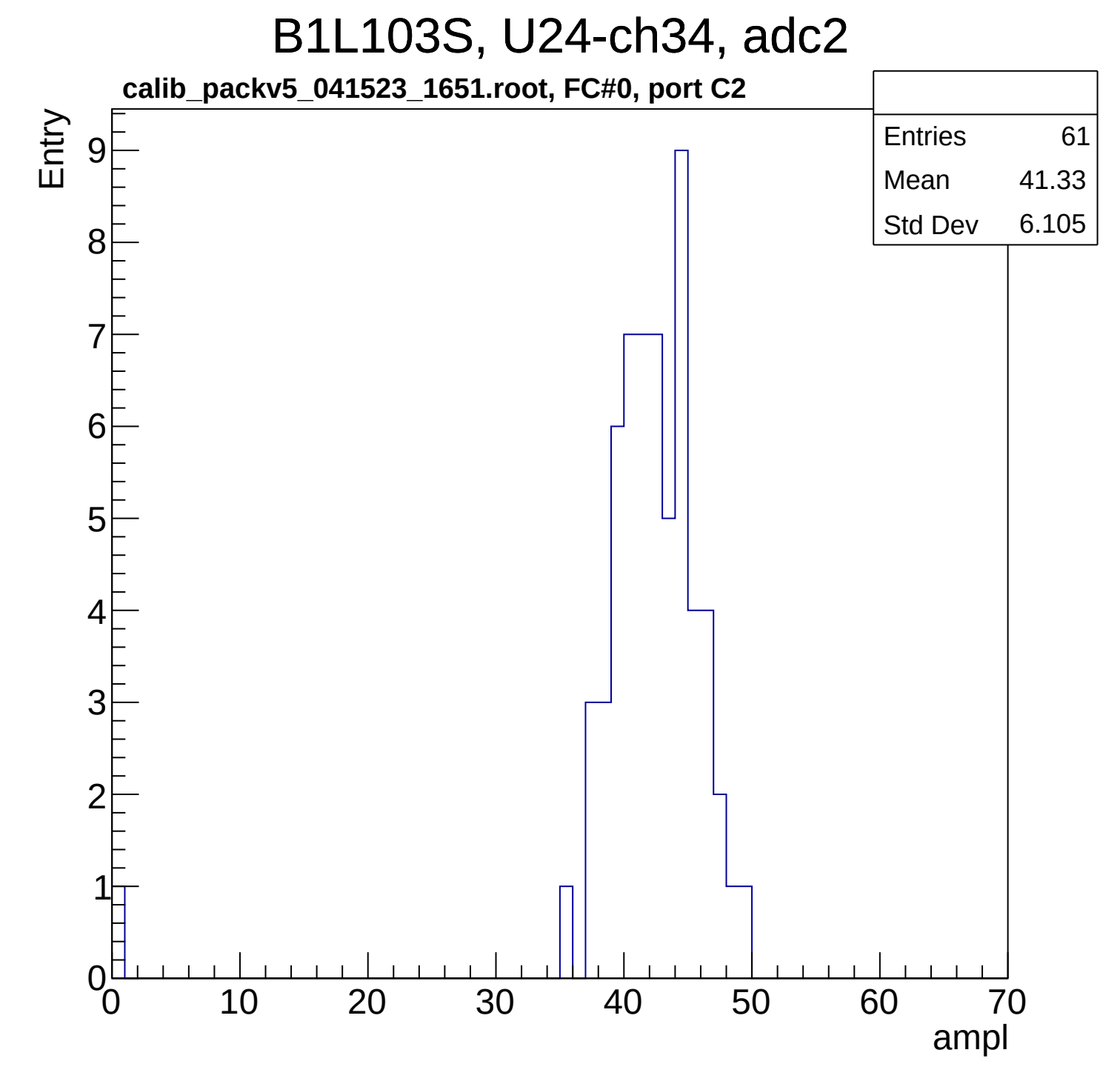
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

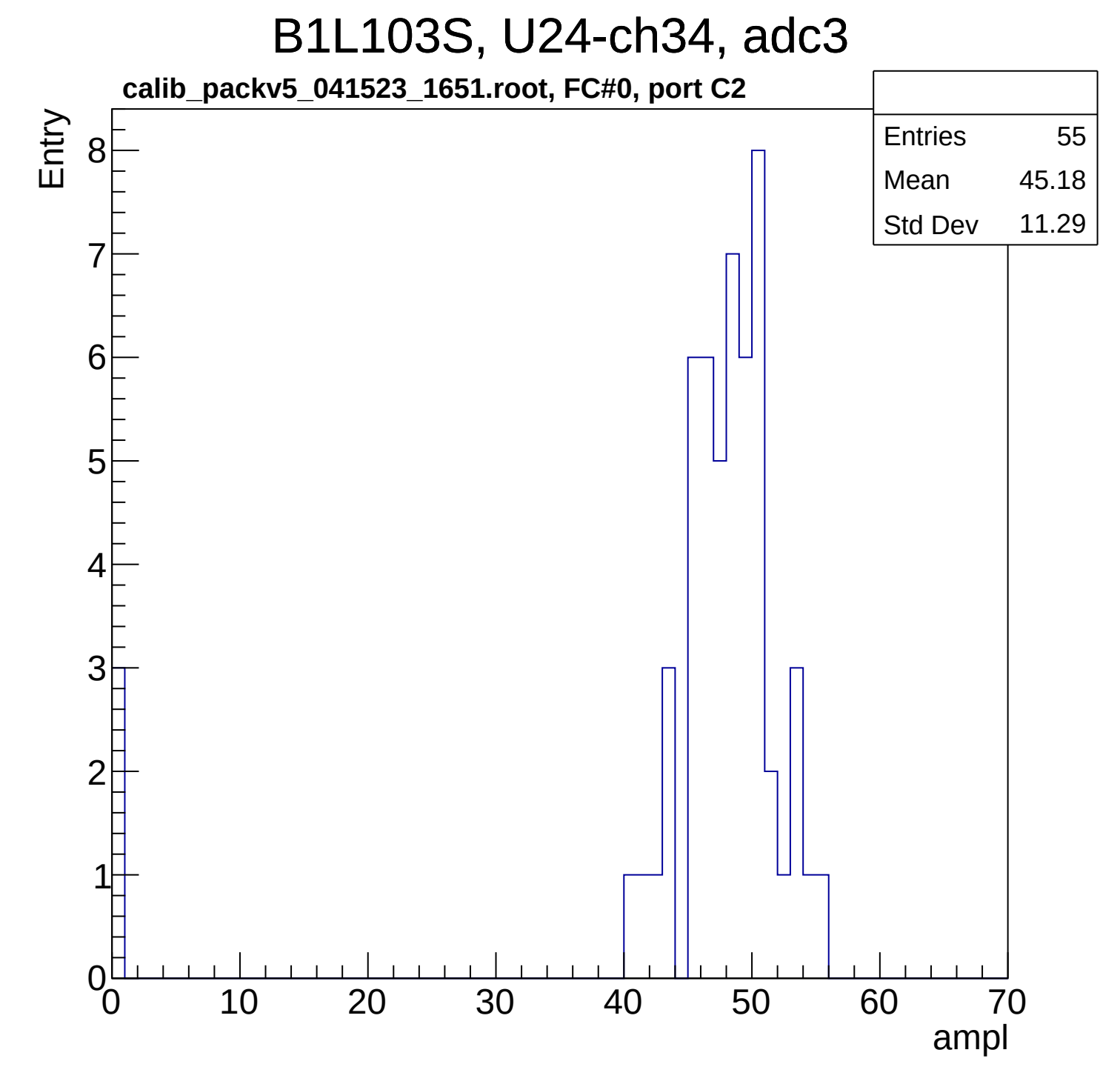

B1L103S, U24-ch33, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 1
Mean 63
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

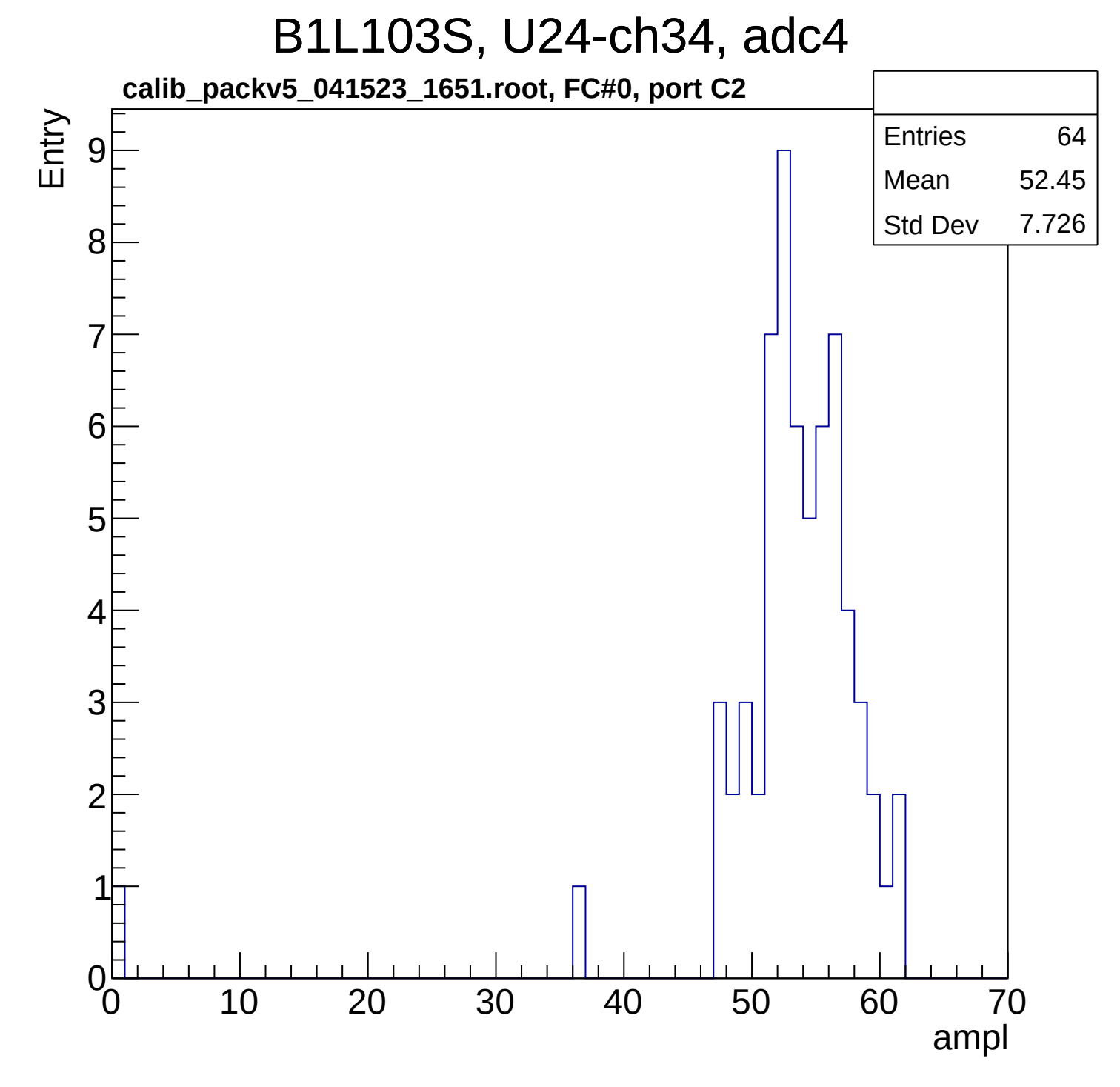

B1L103S, U24-ch33, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch34, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 23.27
Std Dev 10.69
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70


B1L103S, U24-ch34, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 88
Mean 32.14
Std Dev 10.14
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U24-ch34, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 41.33
Std Dev 6.105
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U24-ch34, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 45.18
Std Dev 11.29
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U24-ch34, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 52.45
Std Dev 7.726
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
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40
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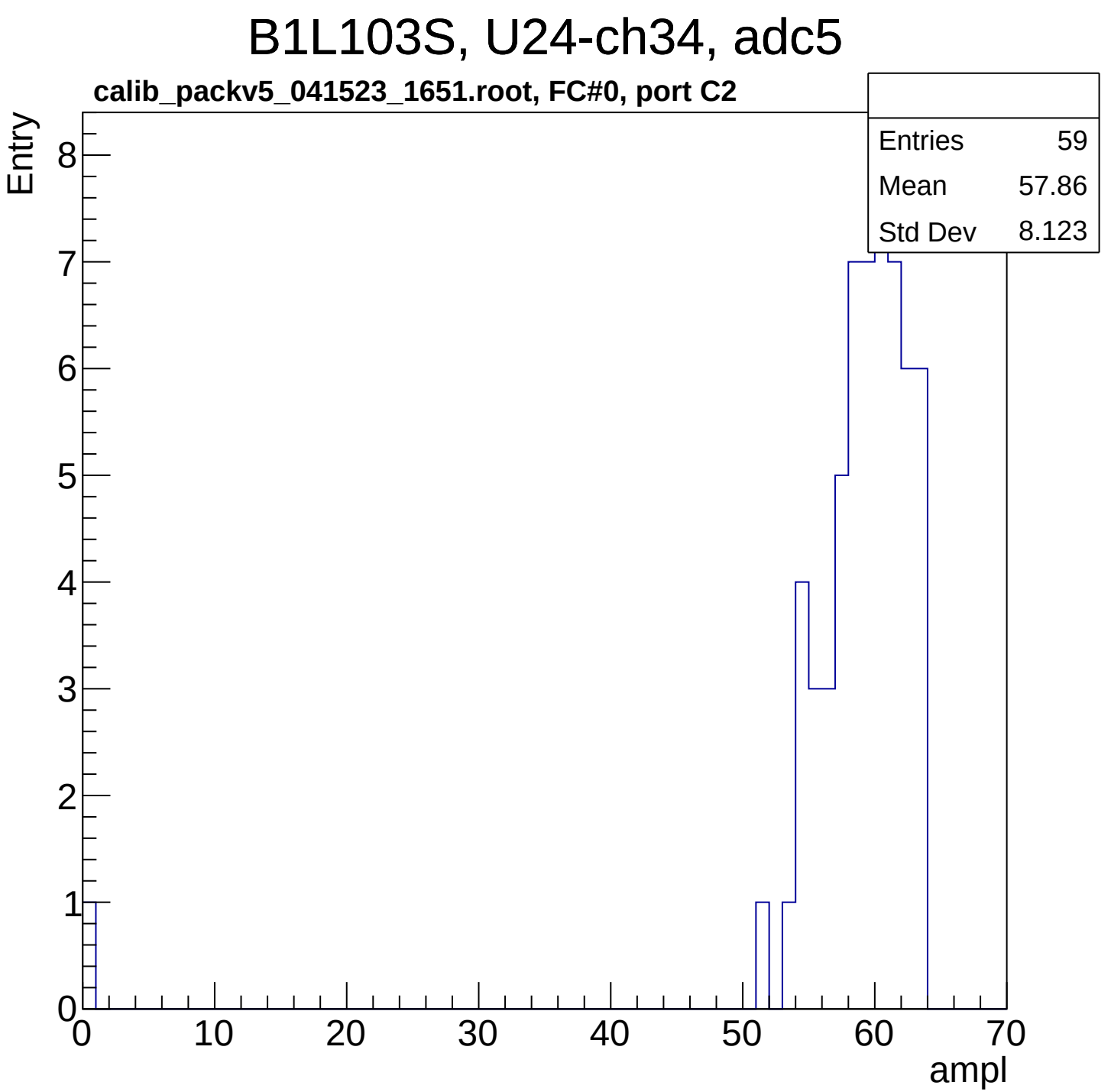
B1L103S, U24-ch34, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 57.86
Std Dev 8.123
Entry
ampl
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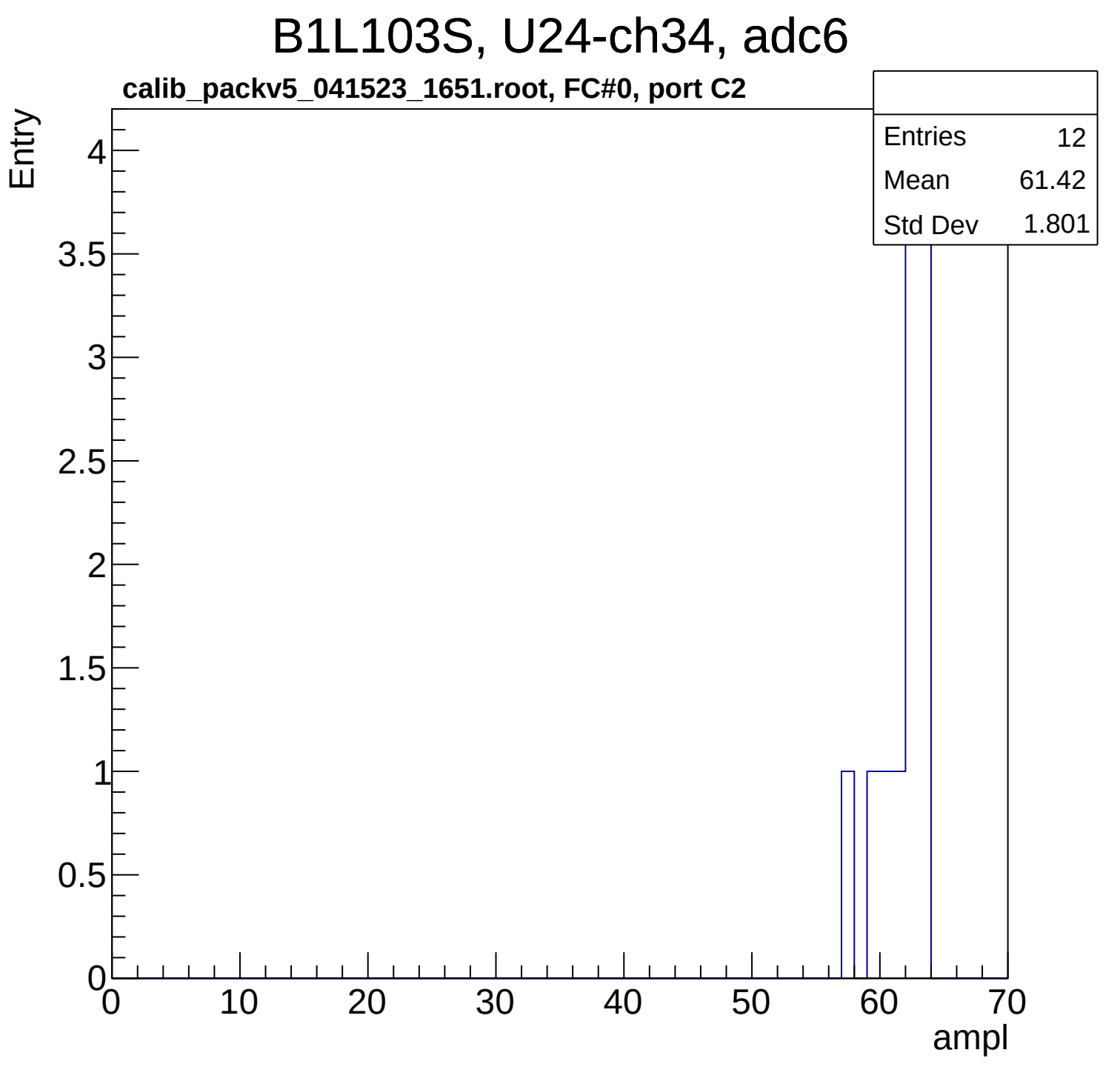
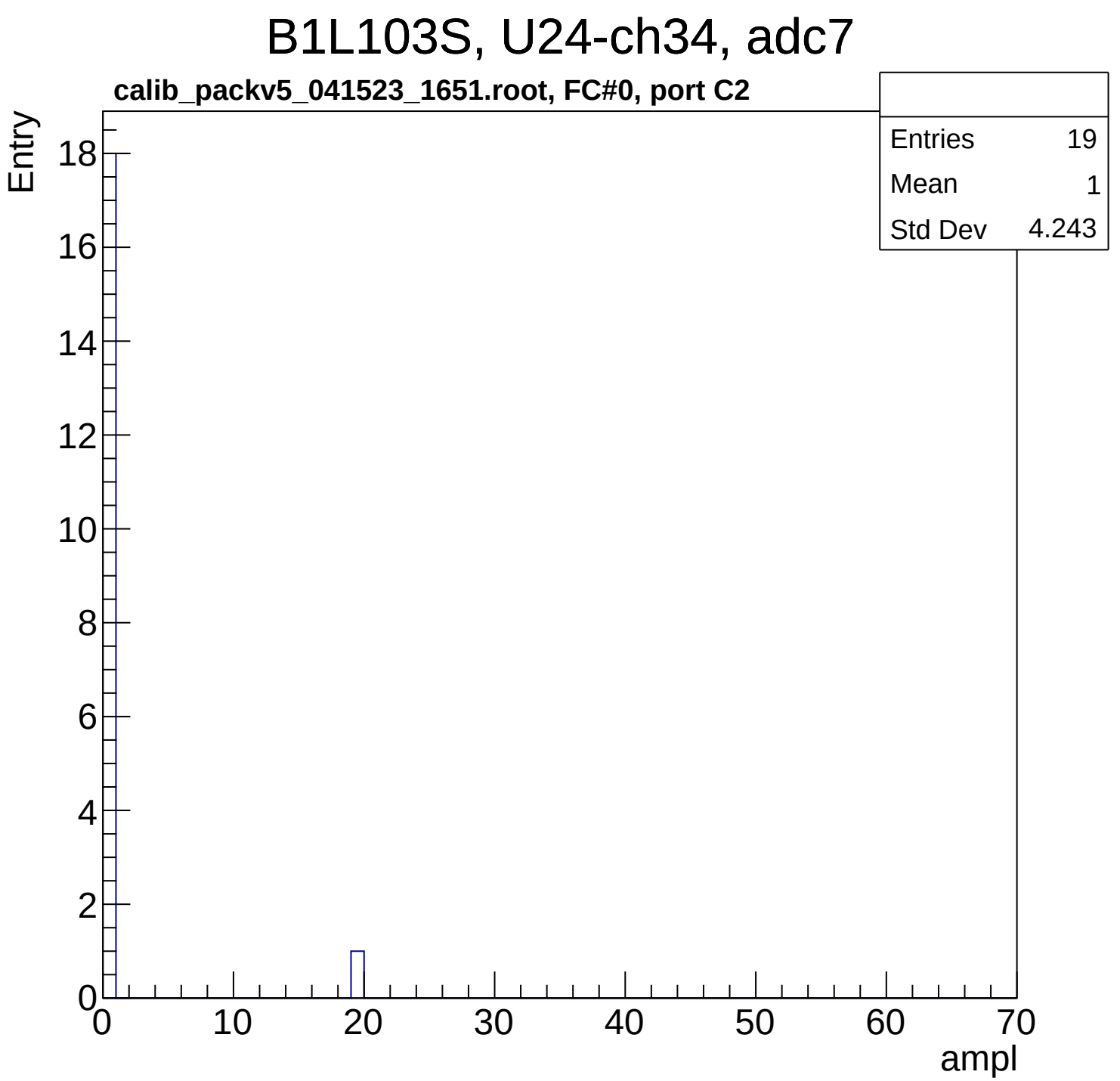
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U24-ch34, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 61.42
Std Dev 1.801
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U24-ch34, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1
Std Dev 4.243
Entry
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6
8
10
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14
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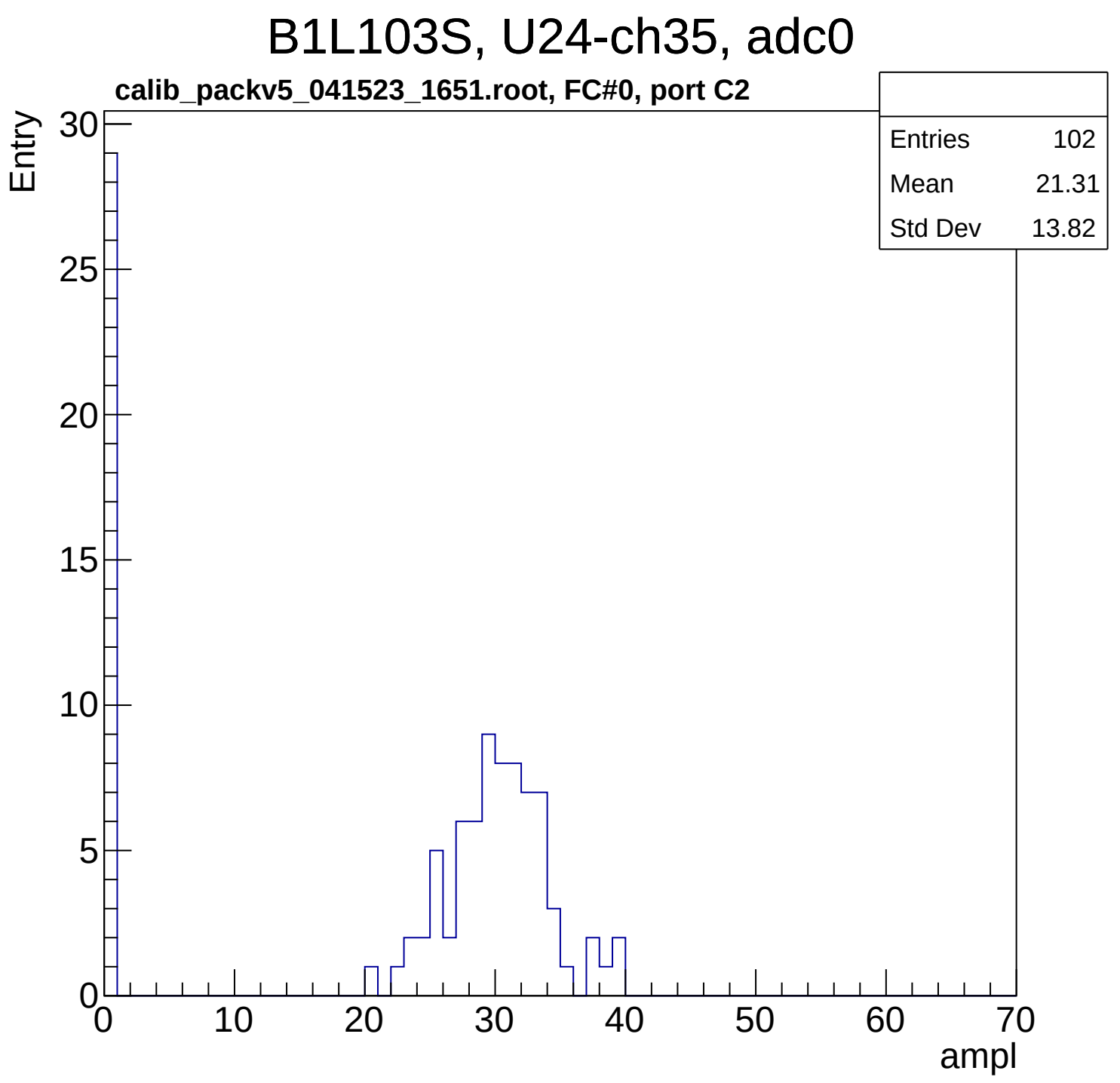
ampl


B1L103S, U24-ch35, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 102
Mean 21.31
Std Dev 13.82
Entry
ampl
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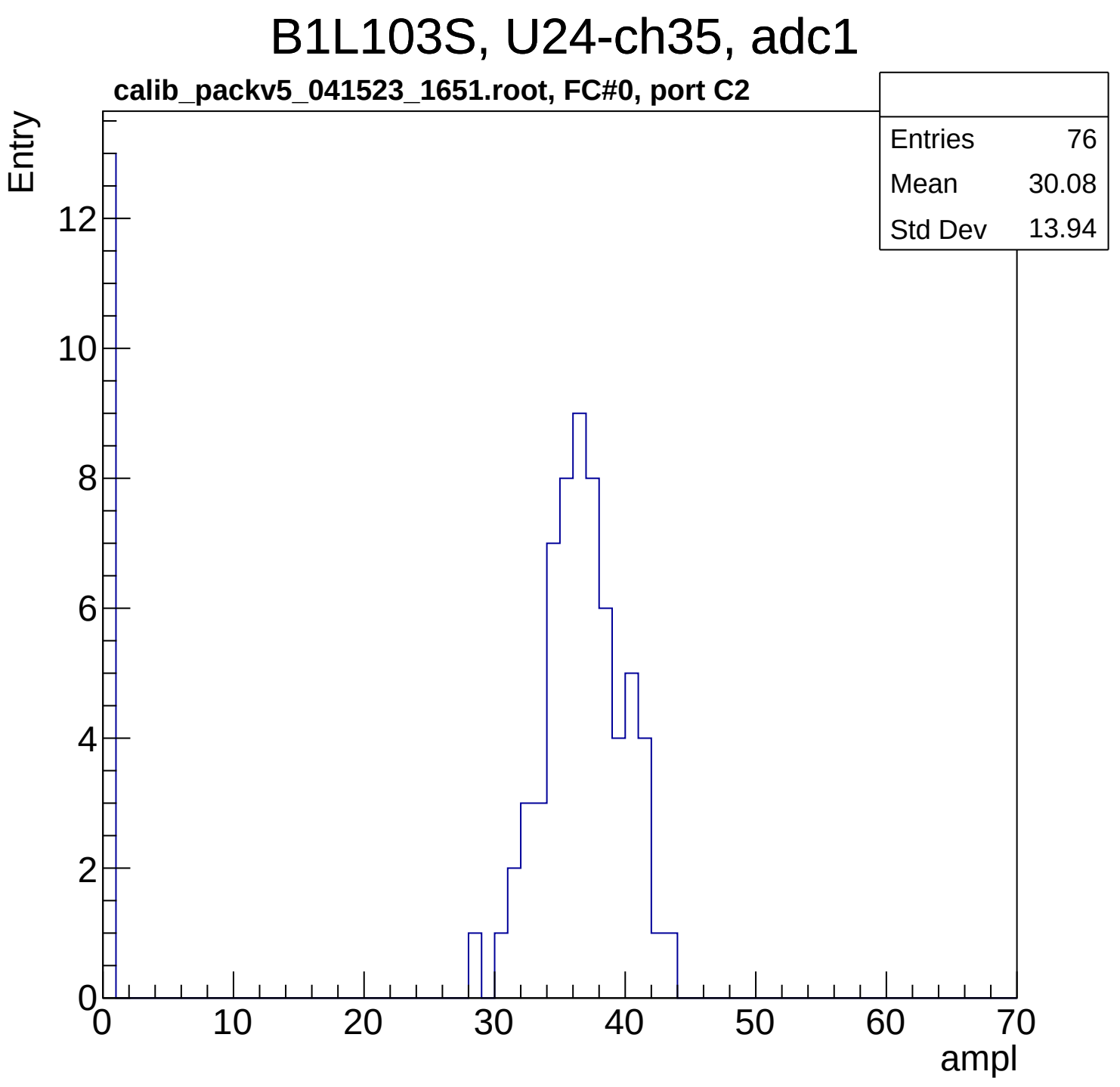
B1L103S, U24-ch35, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 30.08
Std Dev 13.94
Entry
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10
12
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10
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50
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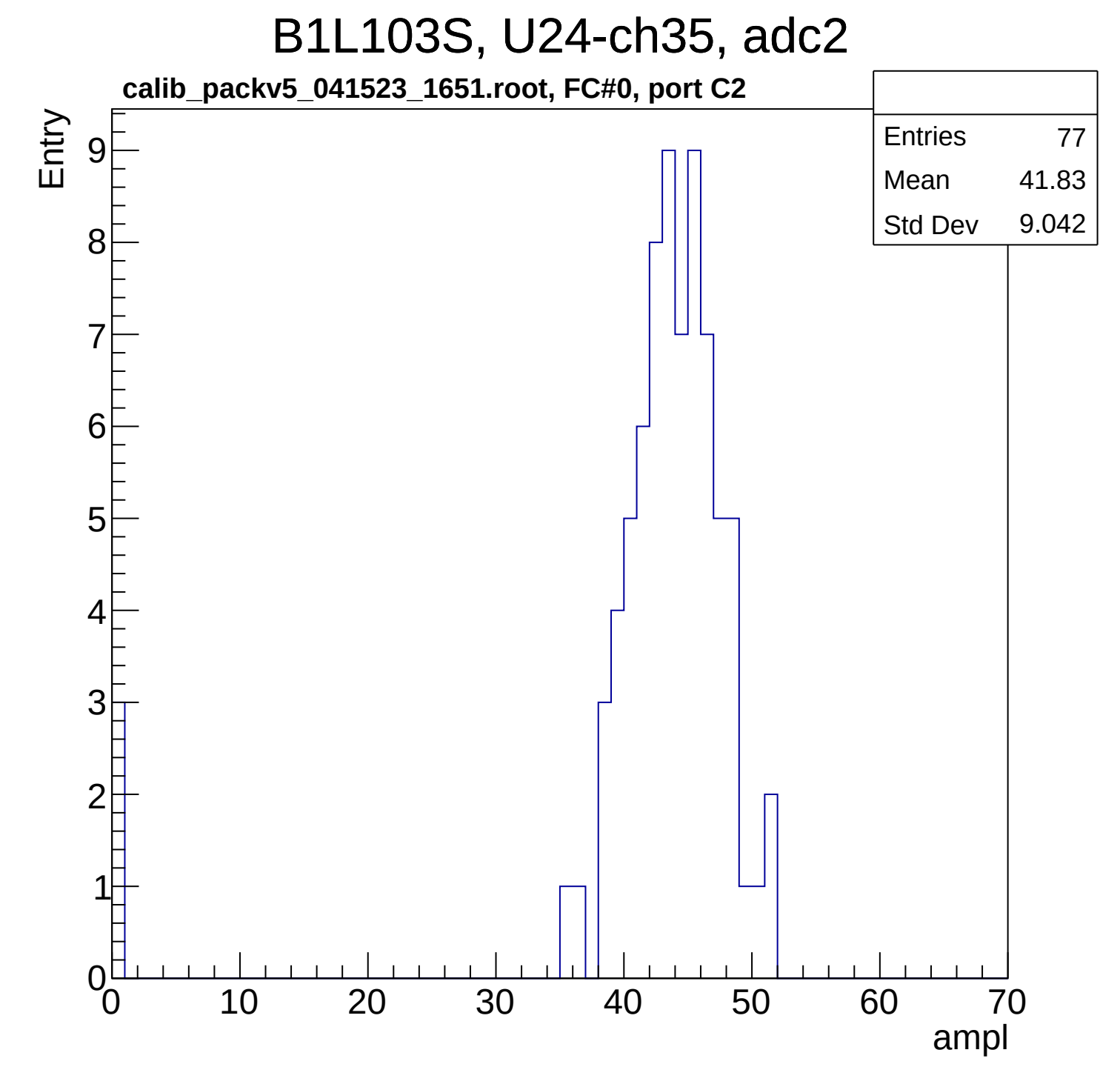
70
ampl


B1L103S, U24-ch35, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 41.83
Std Dev 9.042
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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40
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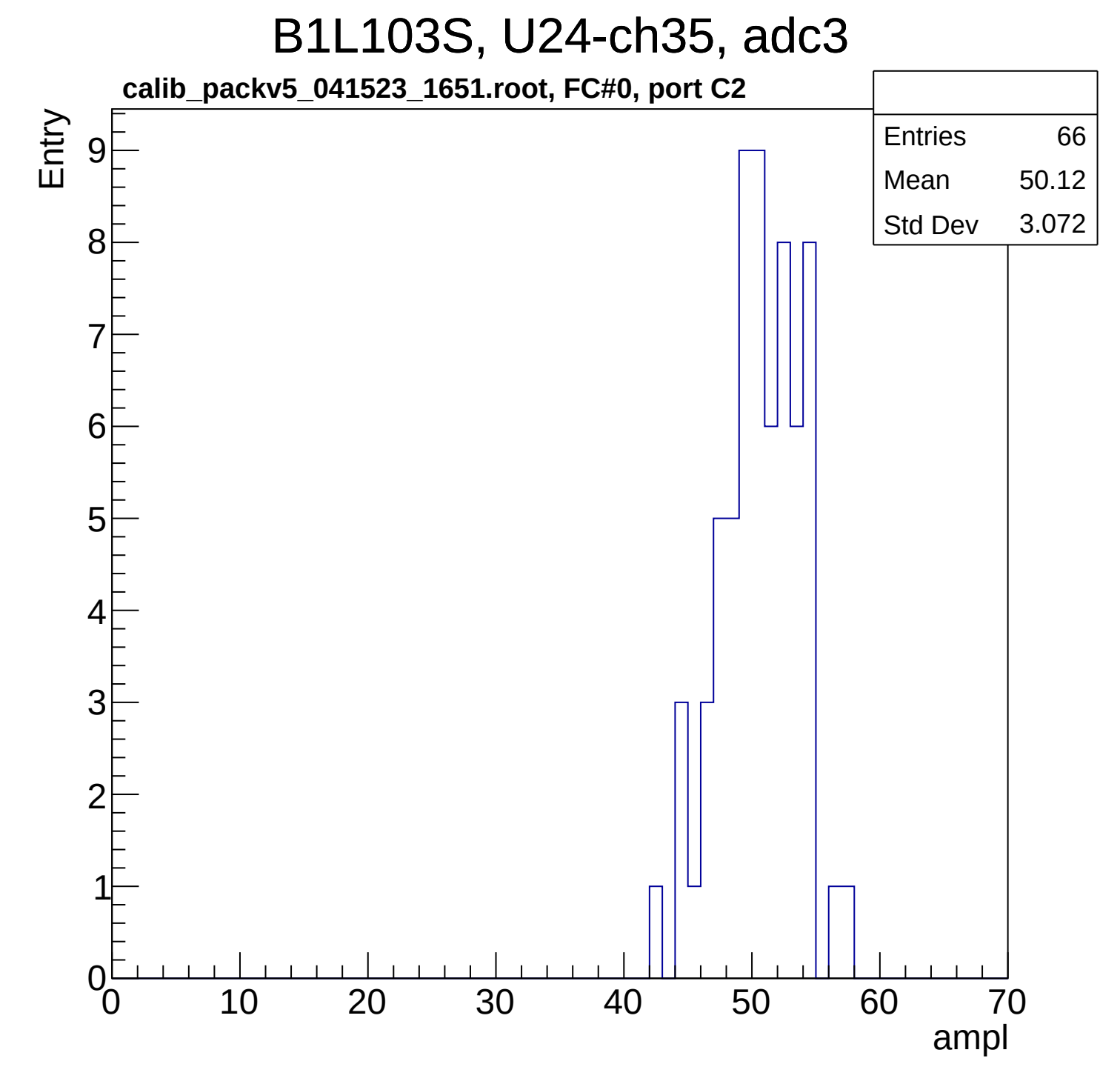
B1L103S, U24-ch35, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 50.12
Std Dev 3.072
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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60
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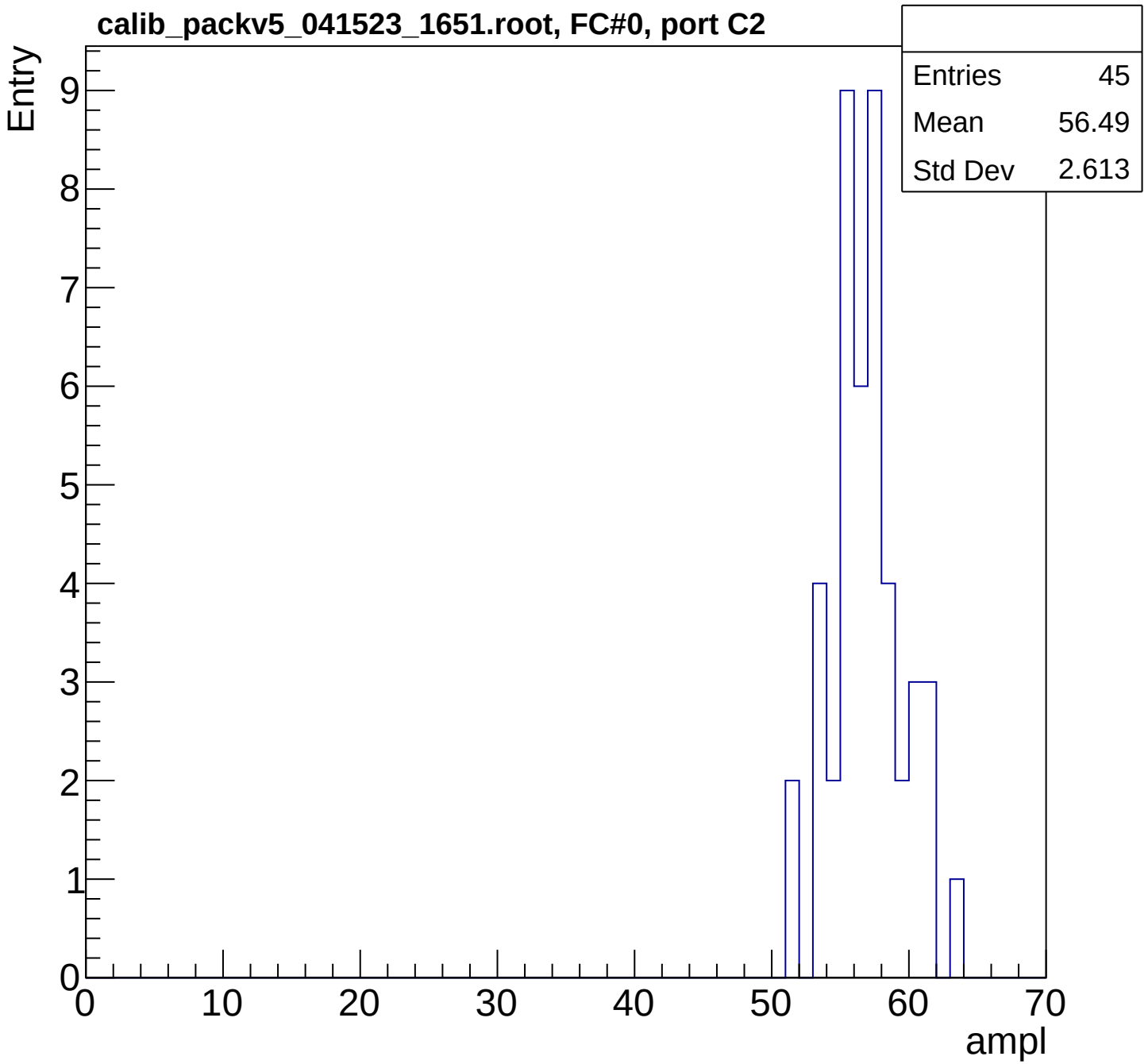
B1L103S, U24-ch35, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 56.49
Std Dev 2.613
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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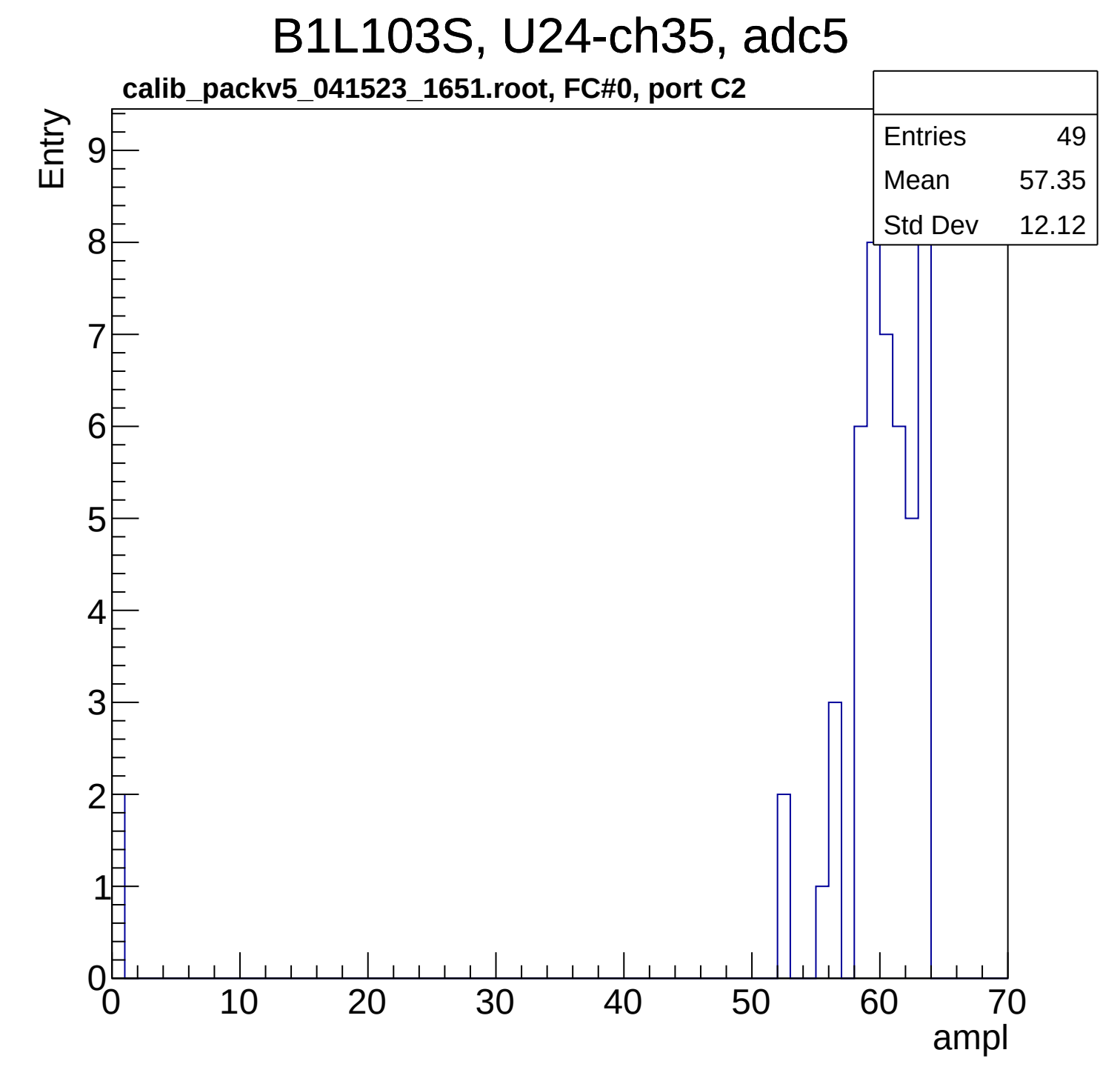
B1L103S, U24-ch35, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 57.35
Std Dev 12.12
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
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40
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60
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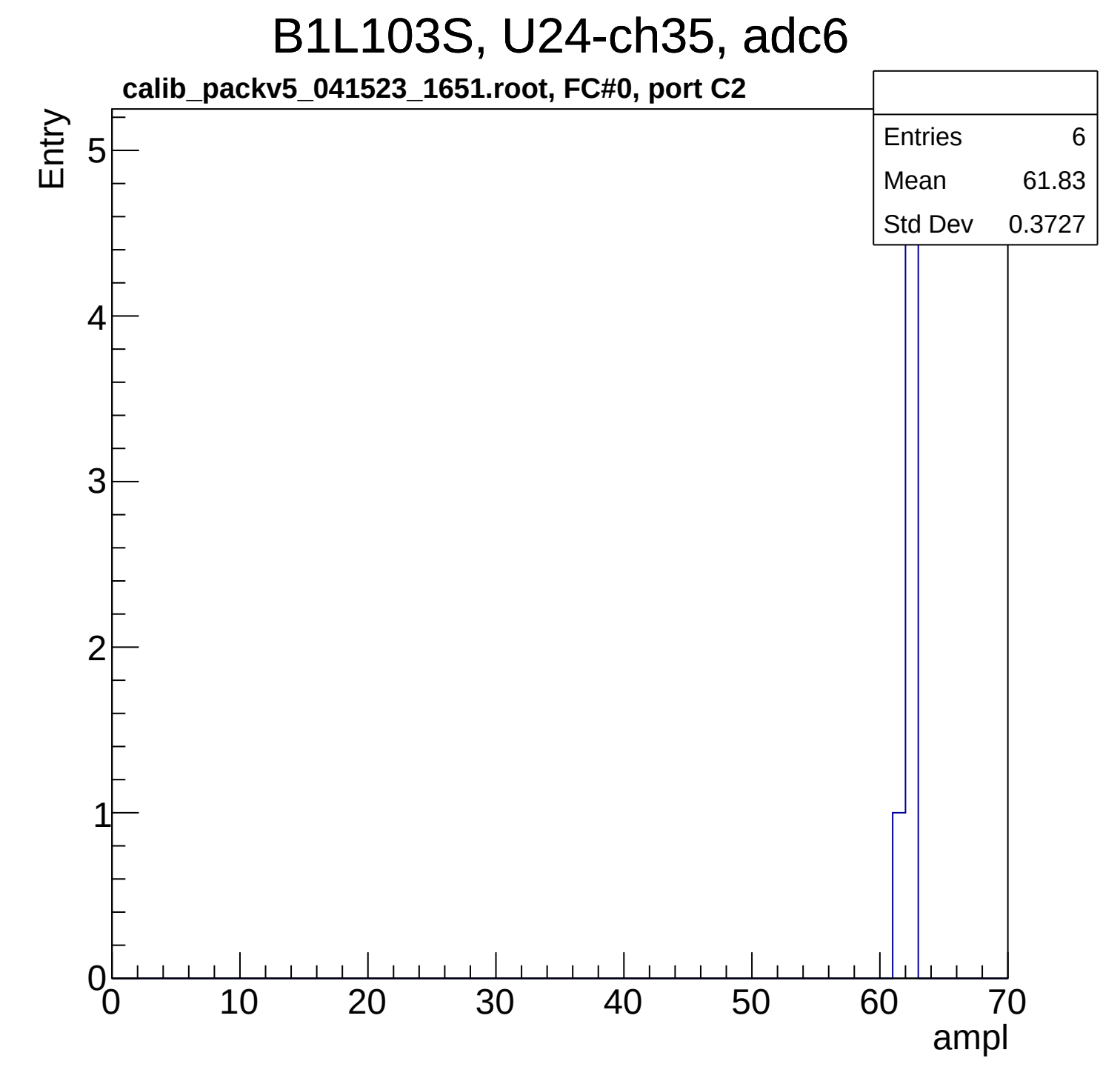
B1L103S, U24-ch35, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 61.83
Std Dev 0.3727
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
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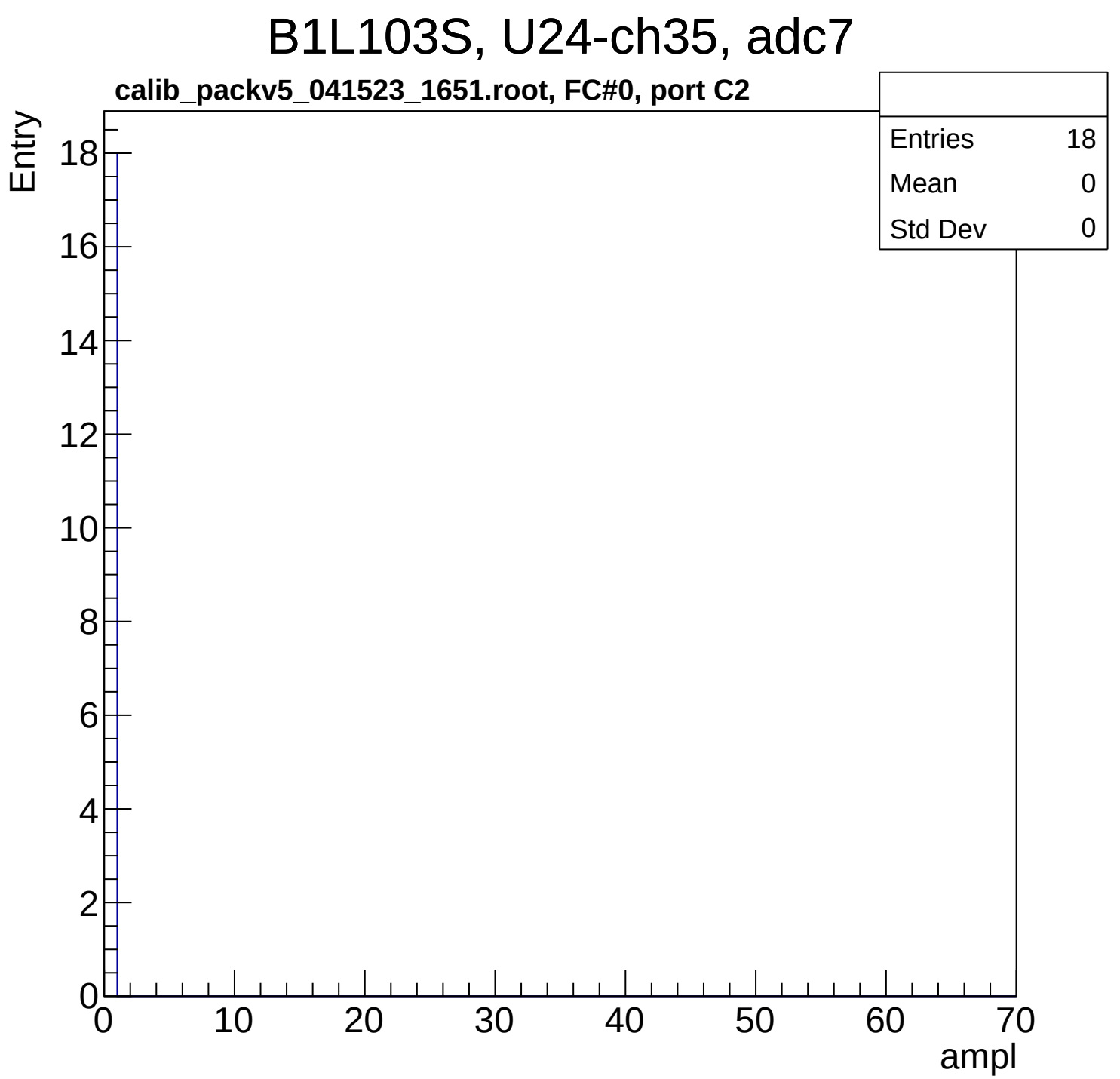
B1L103S, U24-ch35, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
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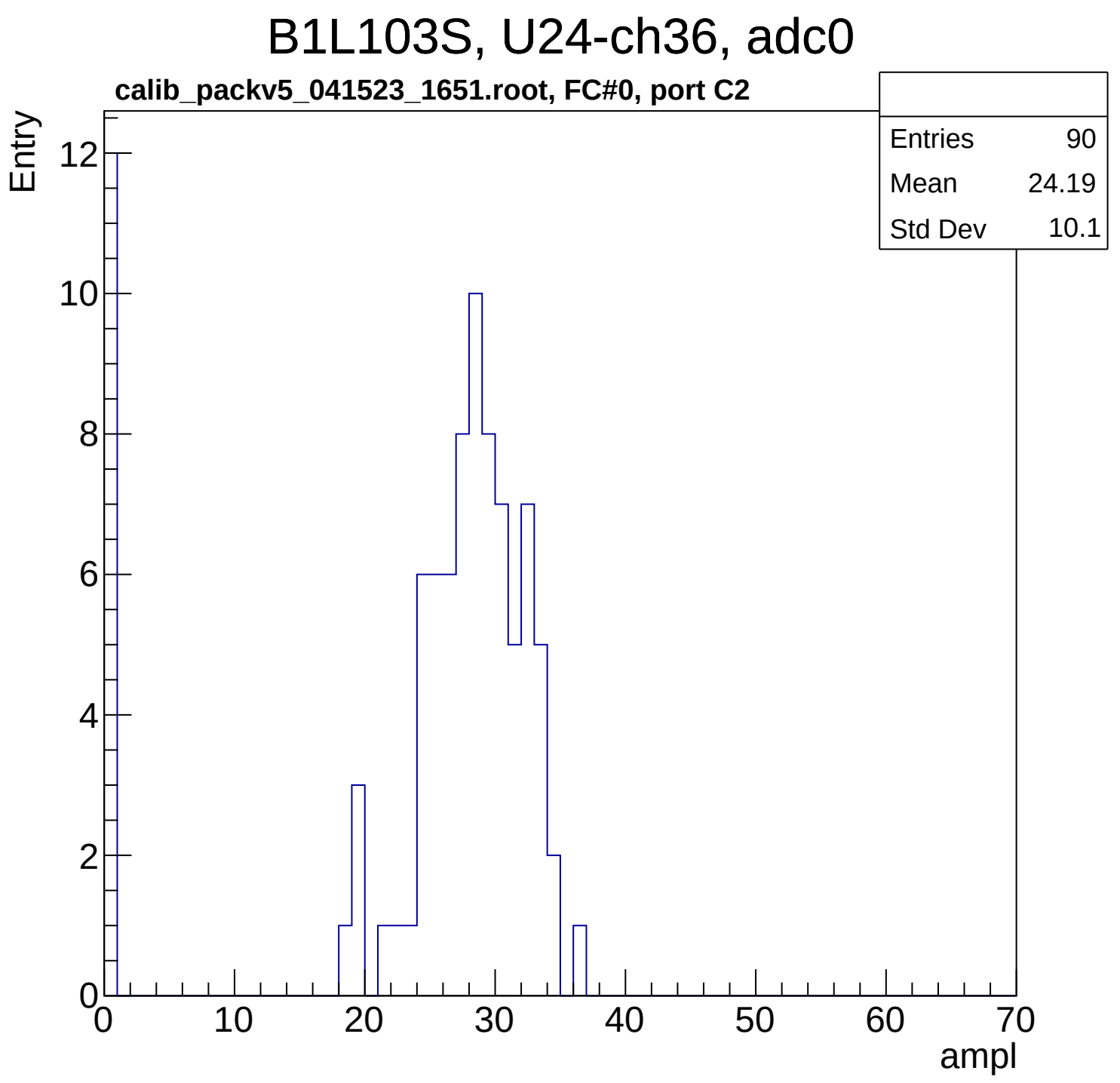
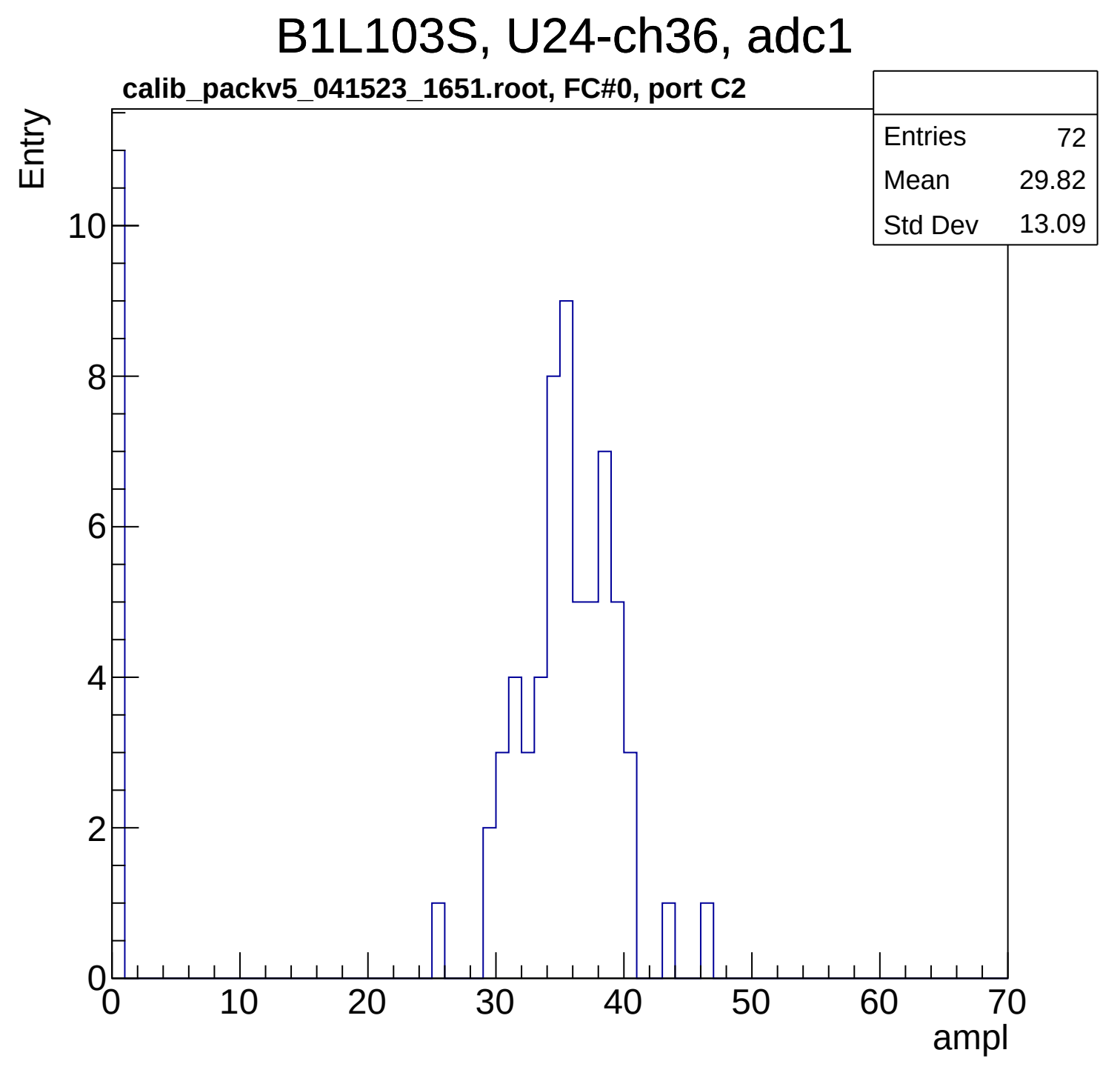
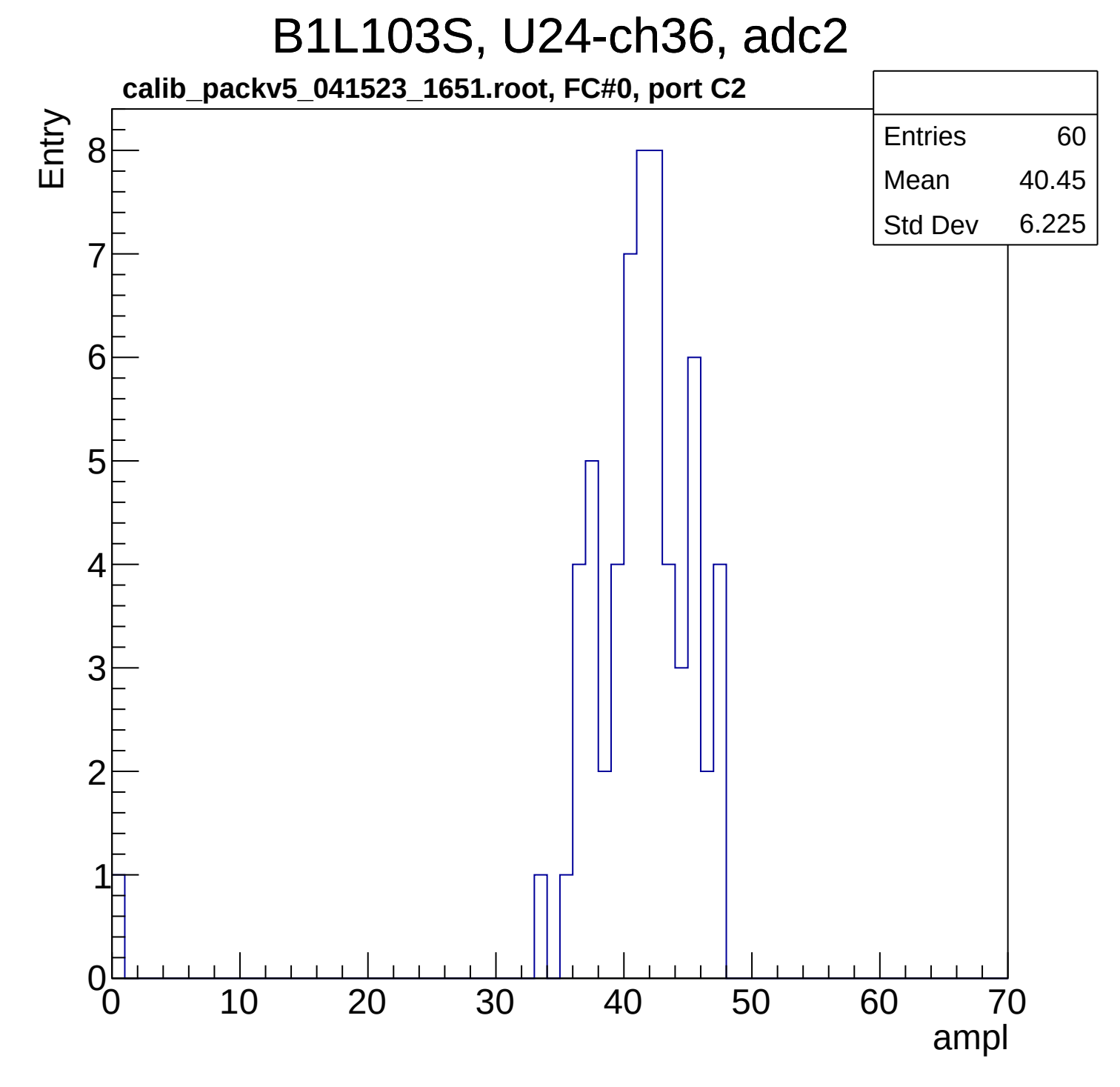
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch36, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 90
Mean 24.19
Std Dev 10.1
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch36, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 29.82
Std Dev 13.09
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch36, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 40.45
Std Dev 6.225
Entry
ampl
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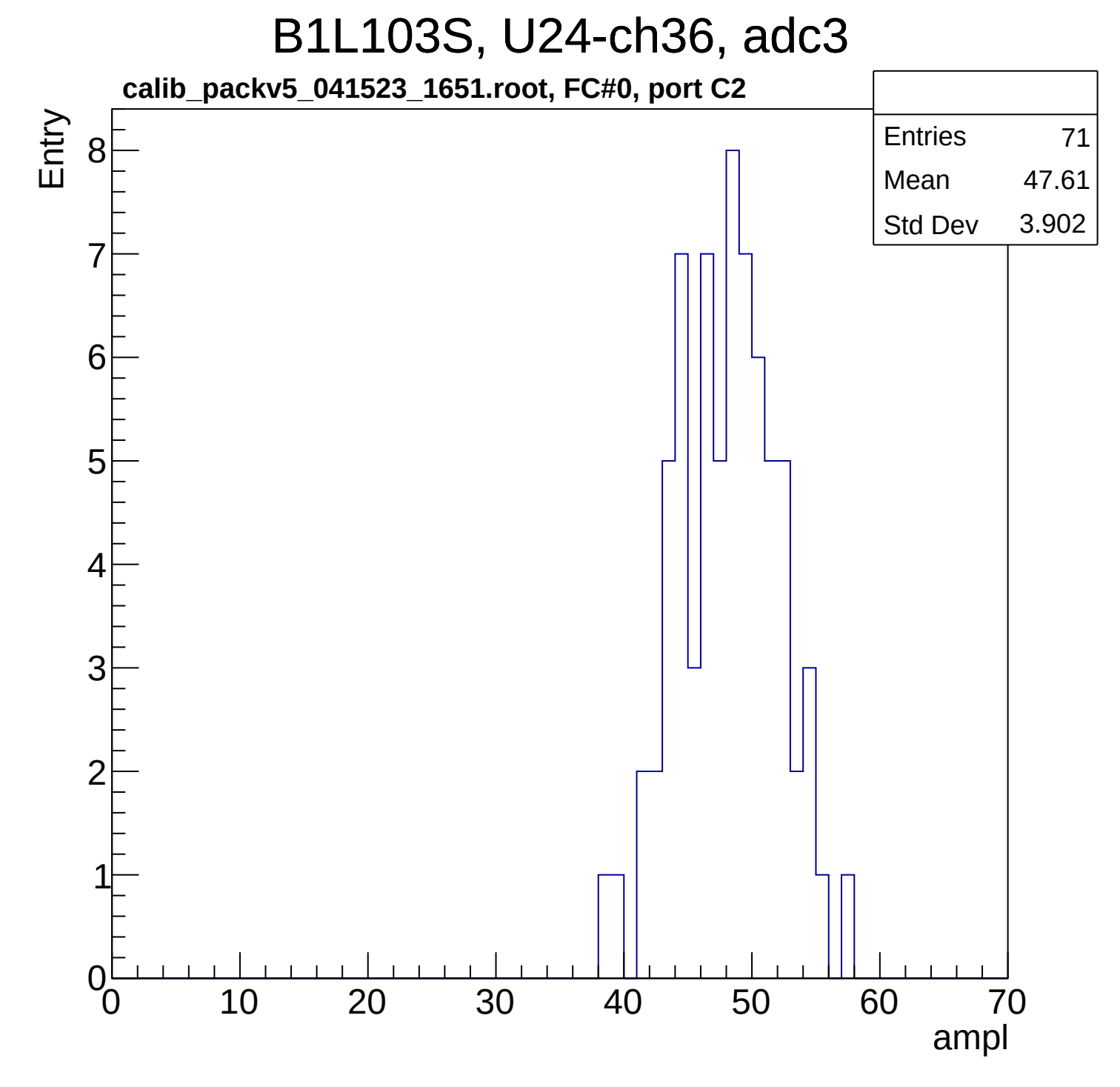
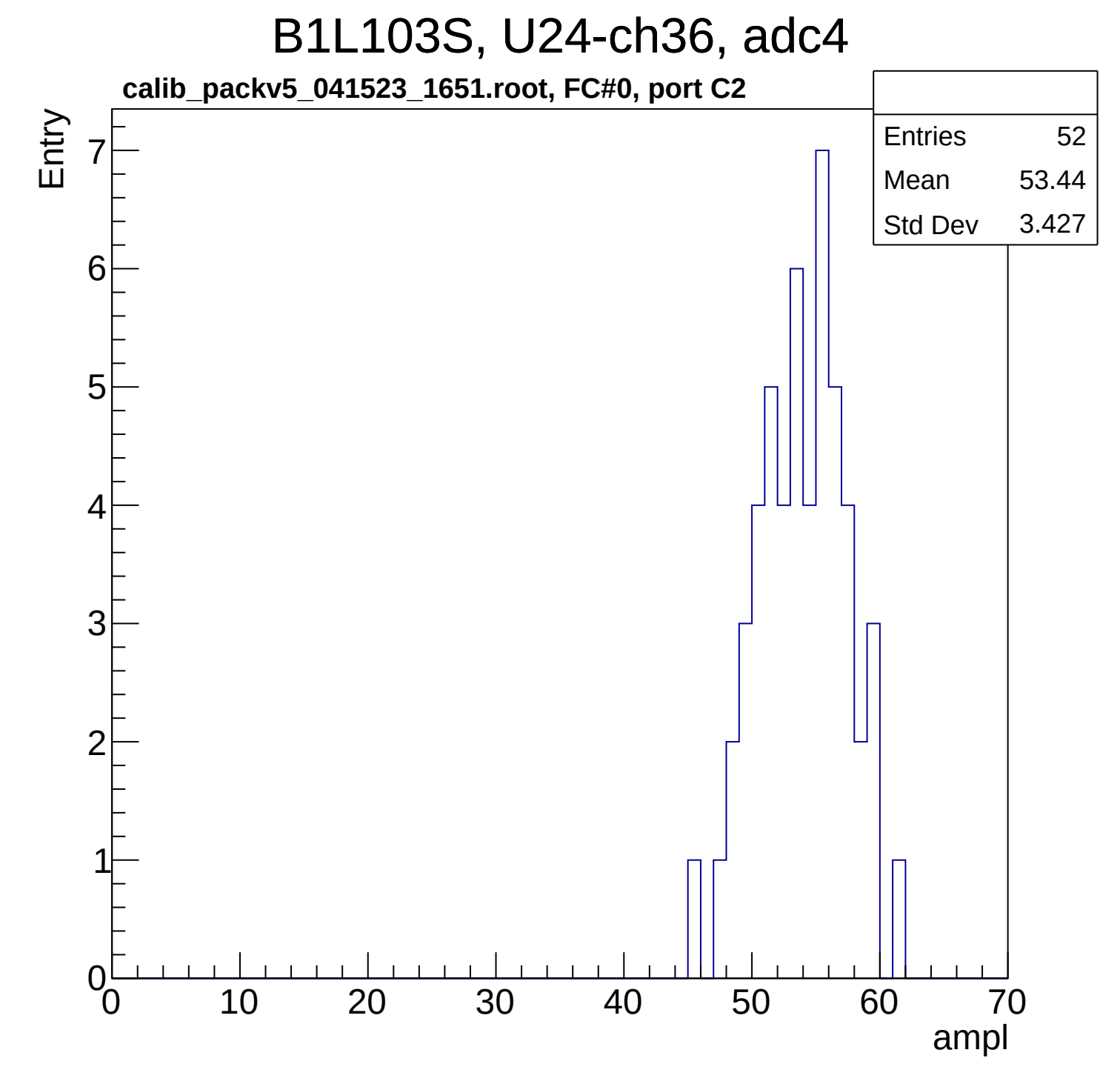
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U24-ch36, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 47.61
Std Dev 3.902
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U24-ch36, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 53.44
Std Dev 3.427
Entry
ampl
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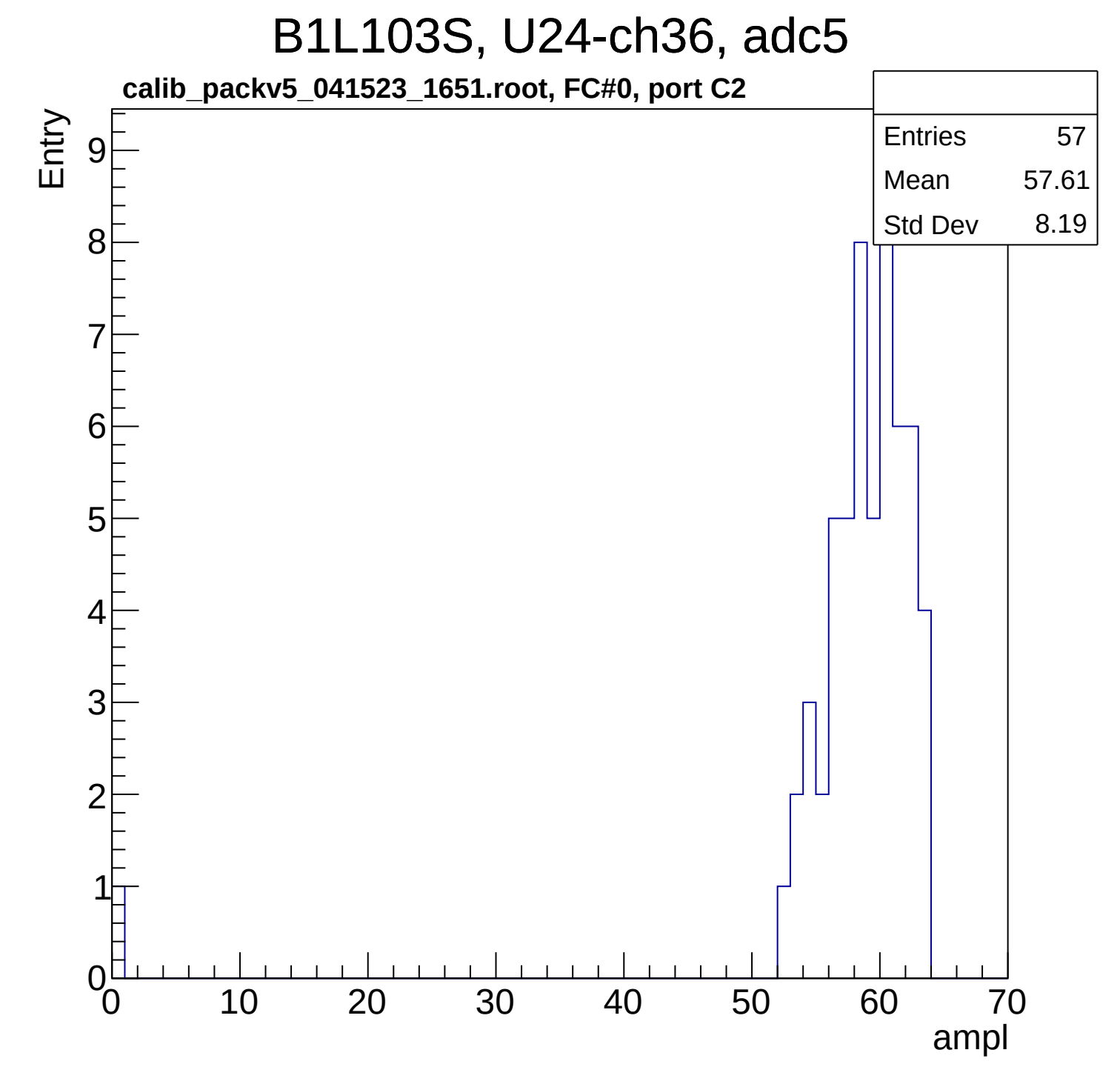
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U24-ch36, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 57.61
Std Dev 8.19
Entry
ampl
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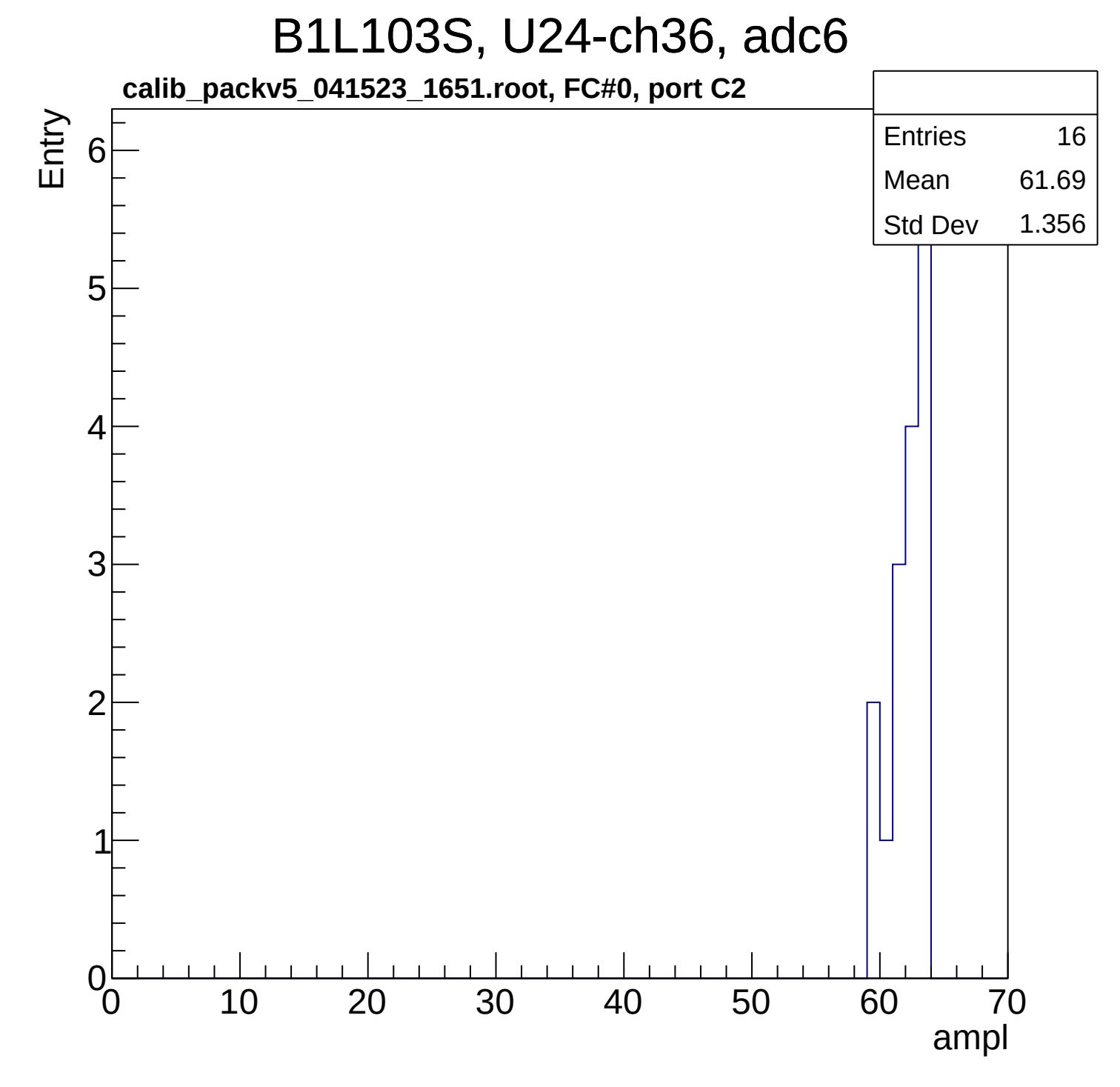
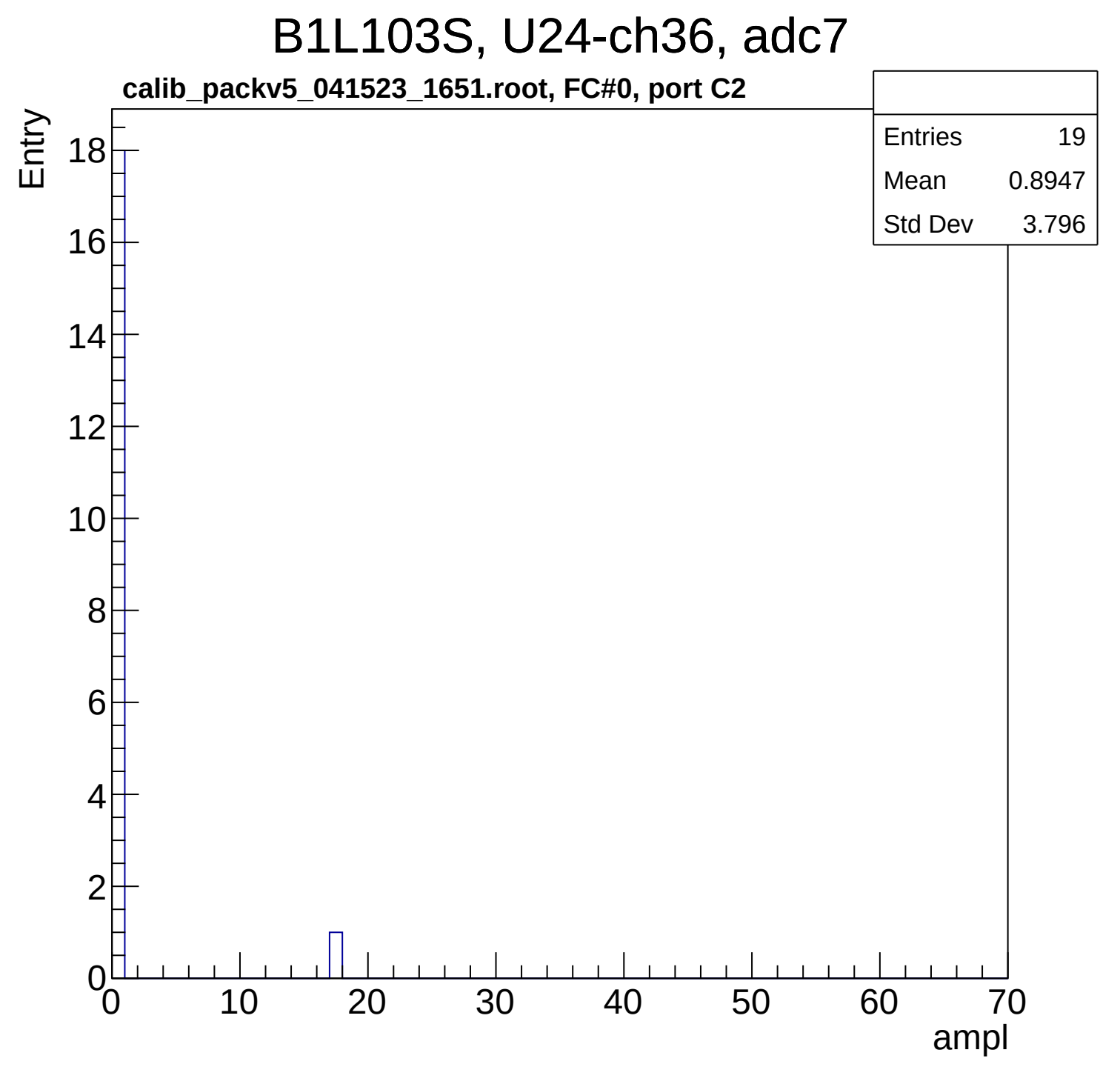
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U24-ch36, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 16
Mean 61.69
Std Dev 1.356
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U24-ch36, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0.8947
Std Dev 3.796
Entry
ampl
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4
6
8
10
12
14
16
18
0
10
20
30
40
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60
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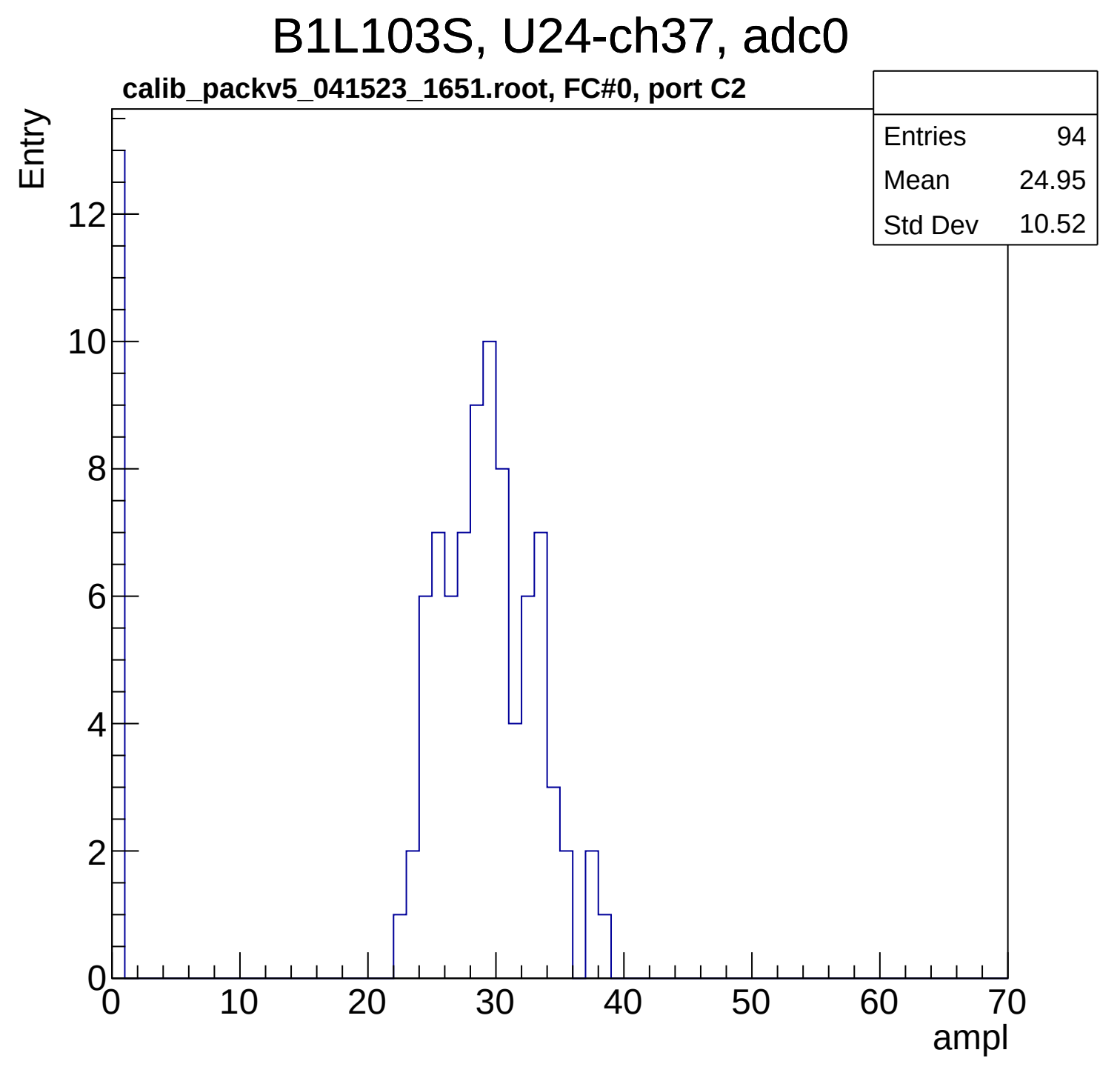
B1L103S, U24-ch37, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 94
Mean 24.95
Std Dev 10.52
Entry
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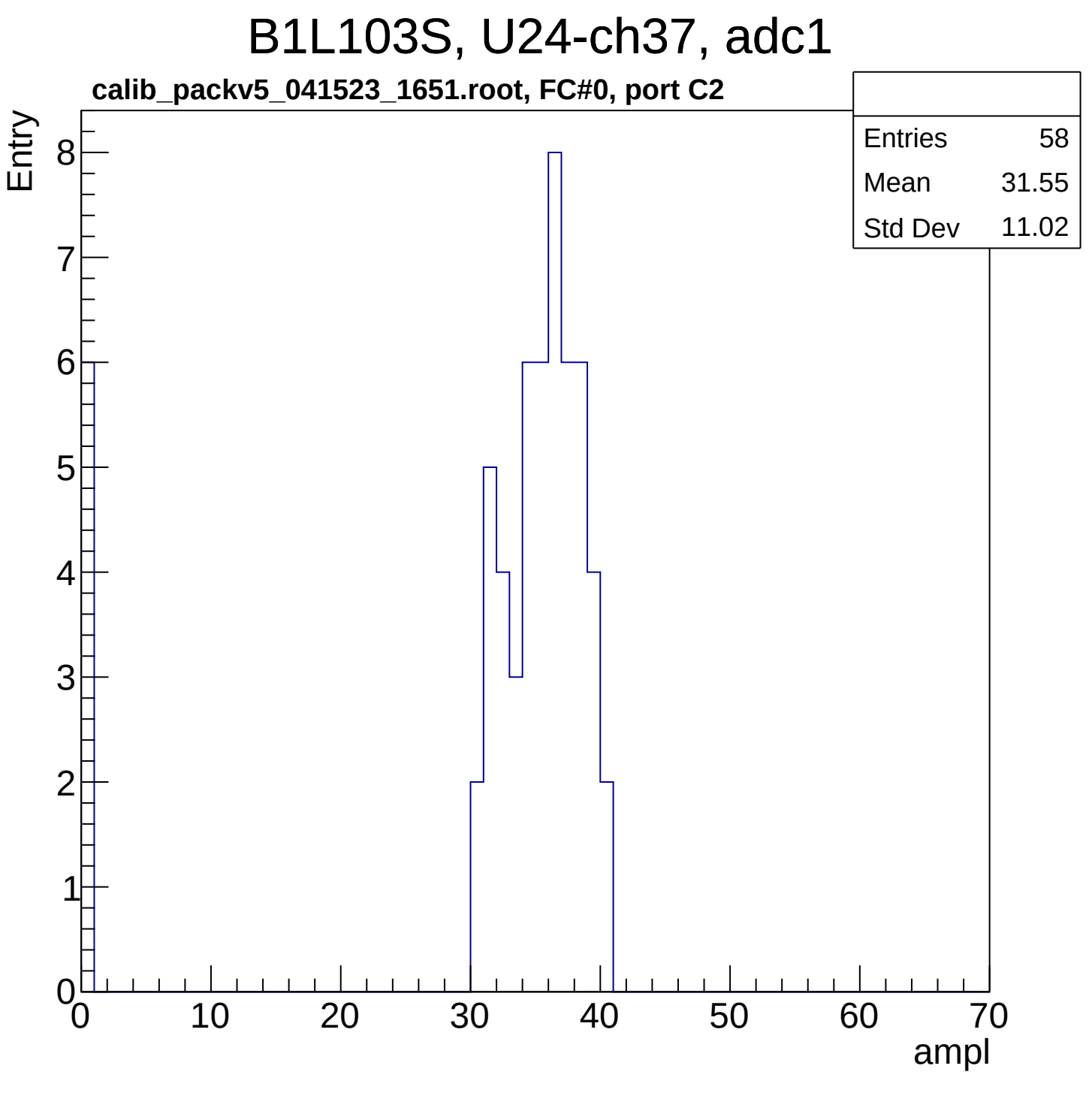
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch37, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 31.55
Std Dev 11.02
Entry
ampl
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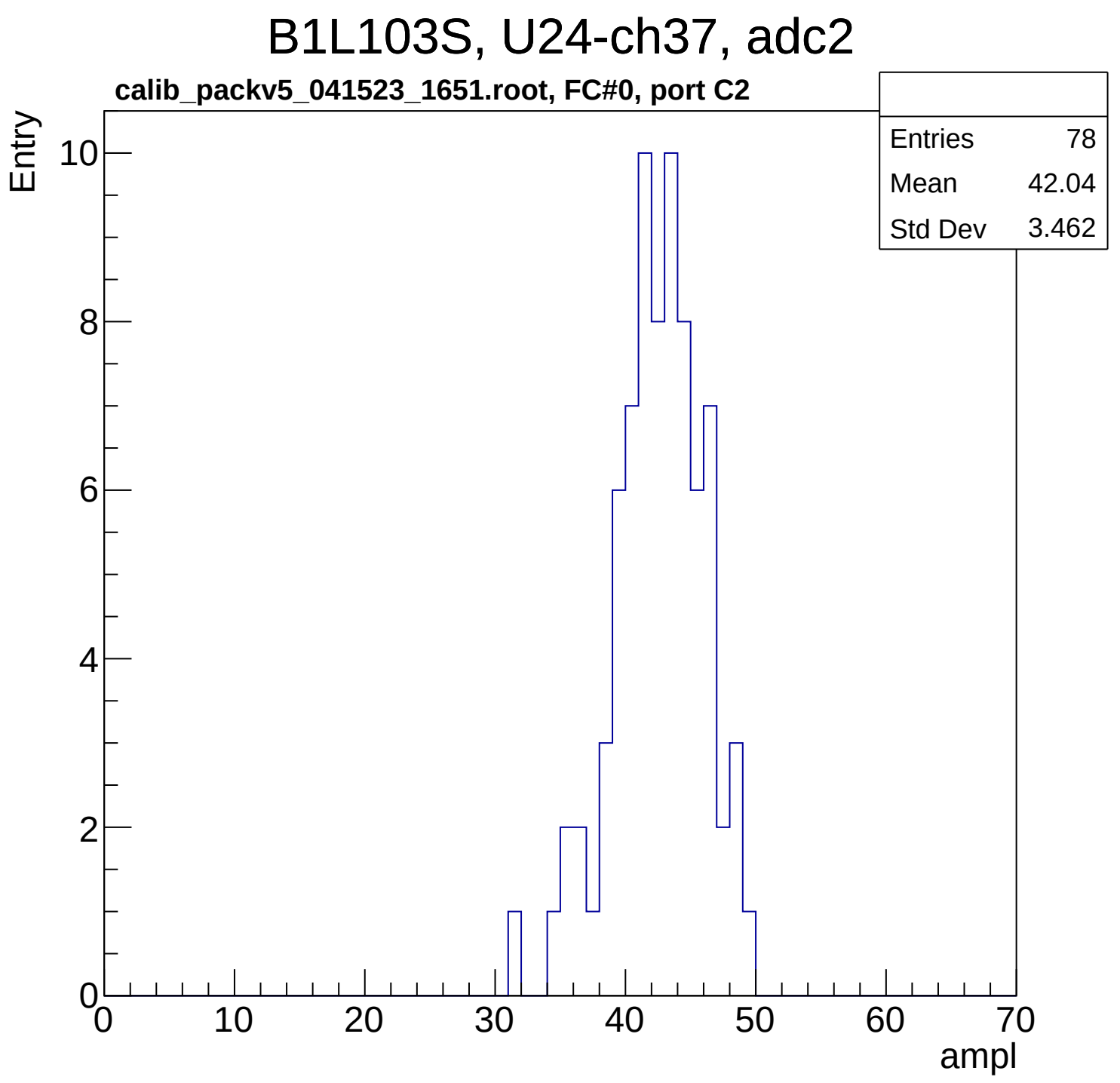
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U24-ch37, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 42.04
Std Dev 3.462
Entry
ampl
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2
4
6
8
10
0
10
20
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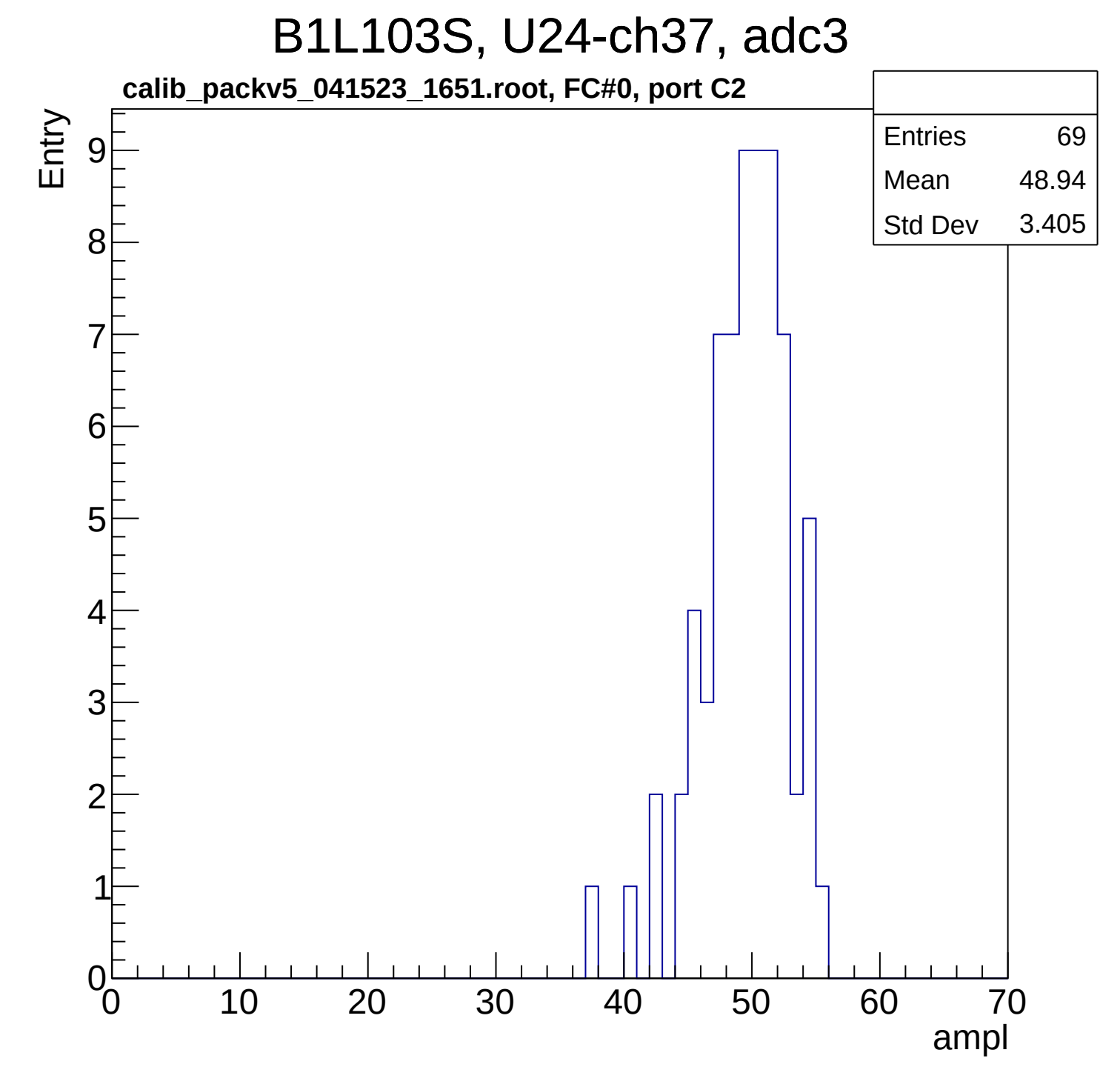
40
50
60
70


B1L103S, U24-ch37, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 48.94
Std Dev 3.405
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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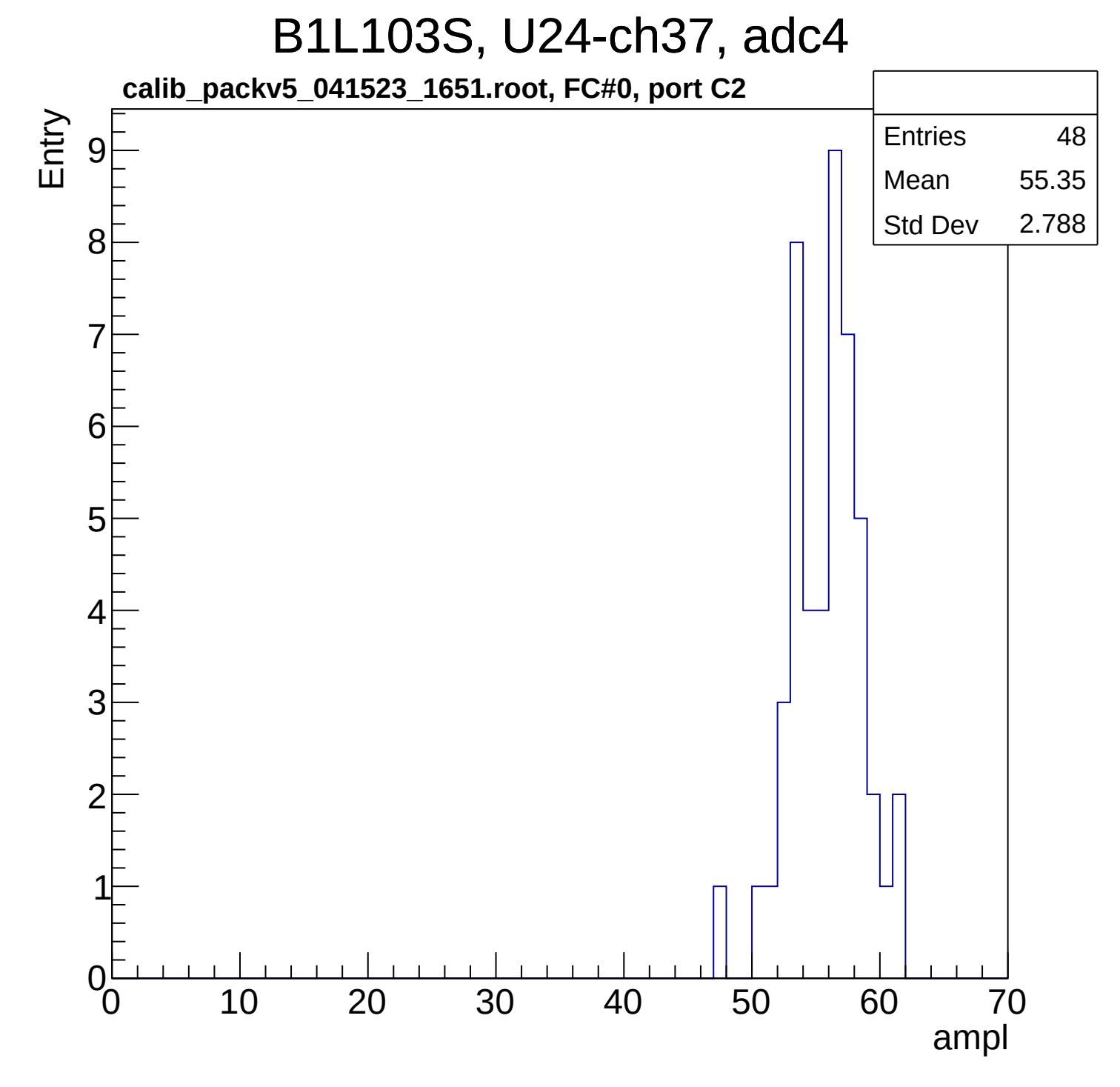
40
50
60
70


B1L103S, U24-ch37, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 55.35
Std Dev 2.788
Entry
ampl
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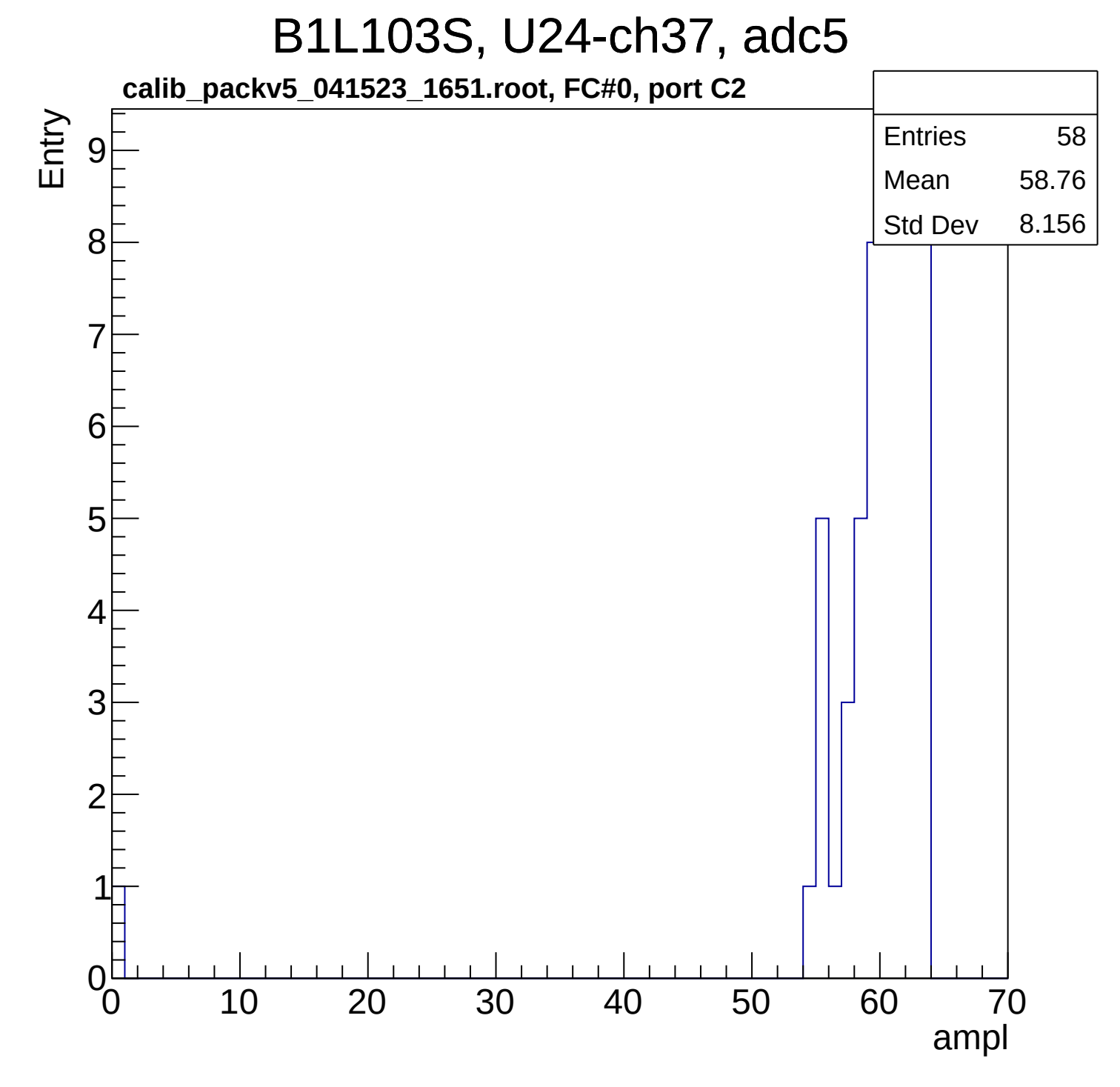
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U24-ch37, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 58.76
Std Dev 8.156
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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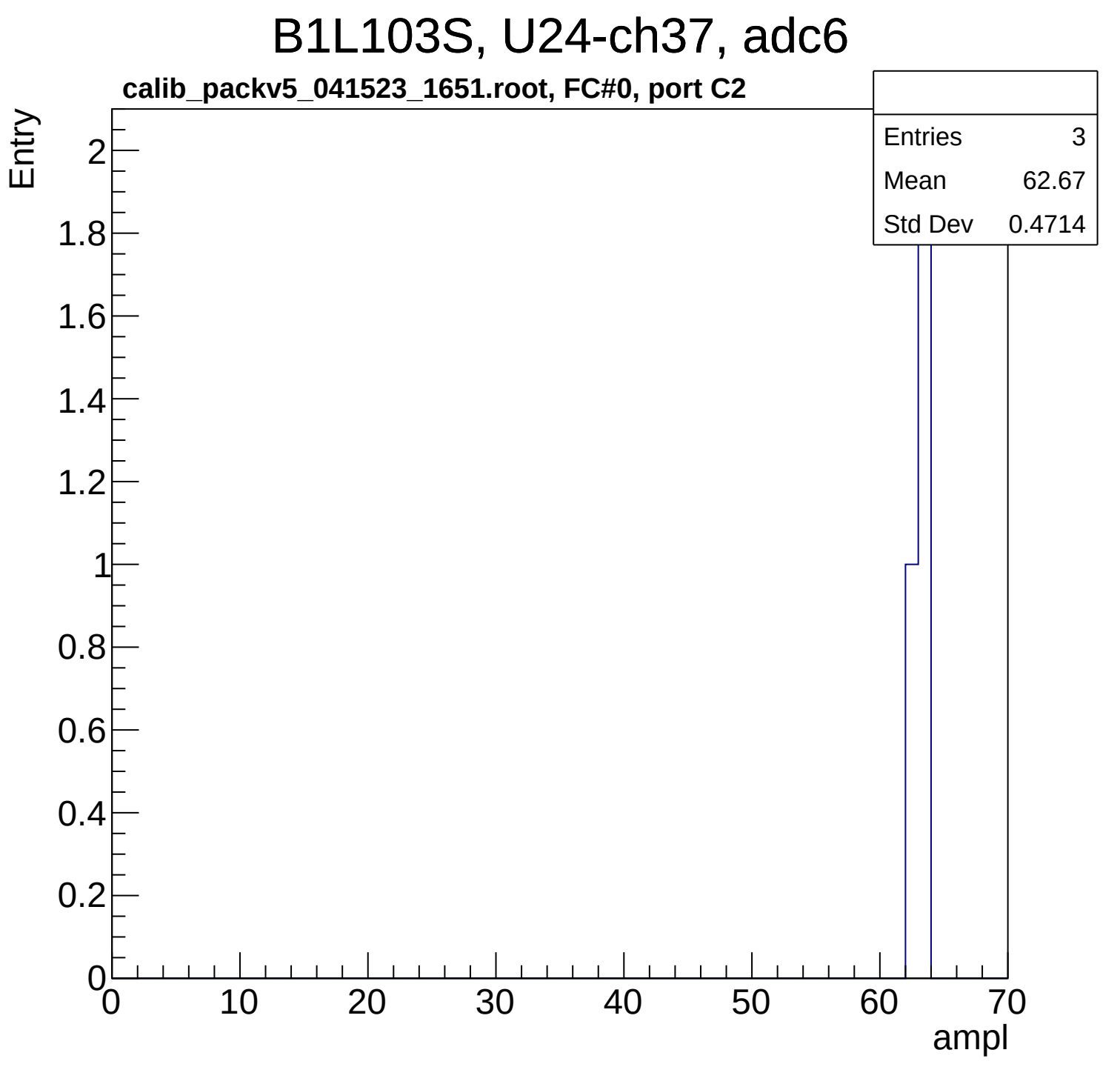
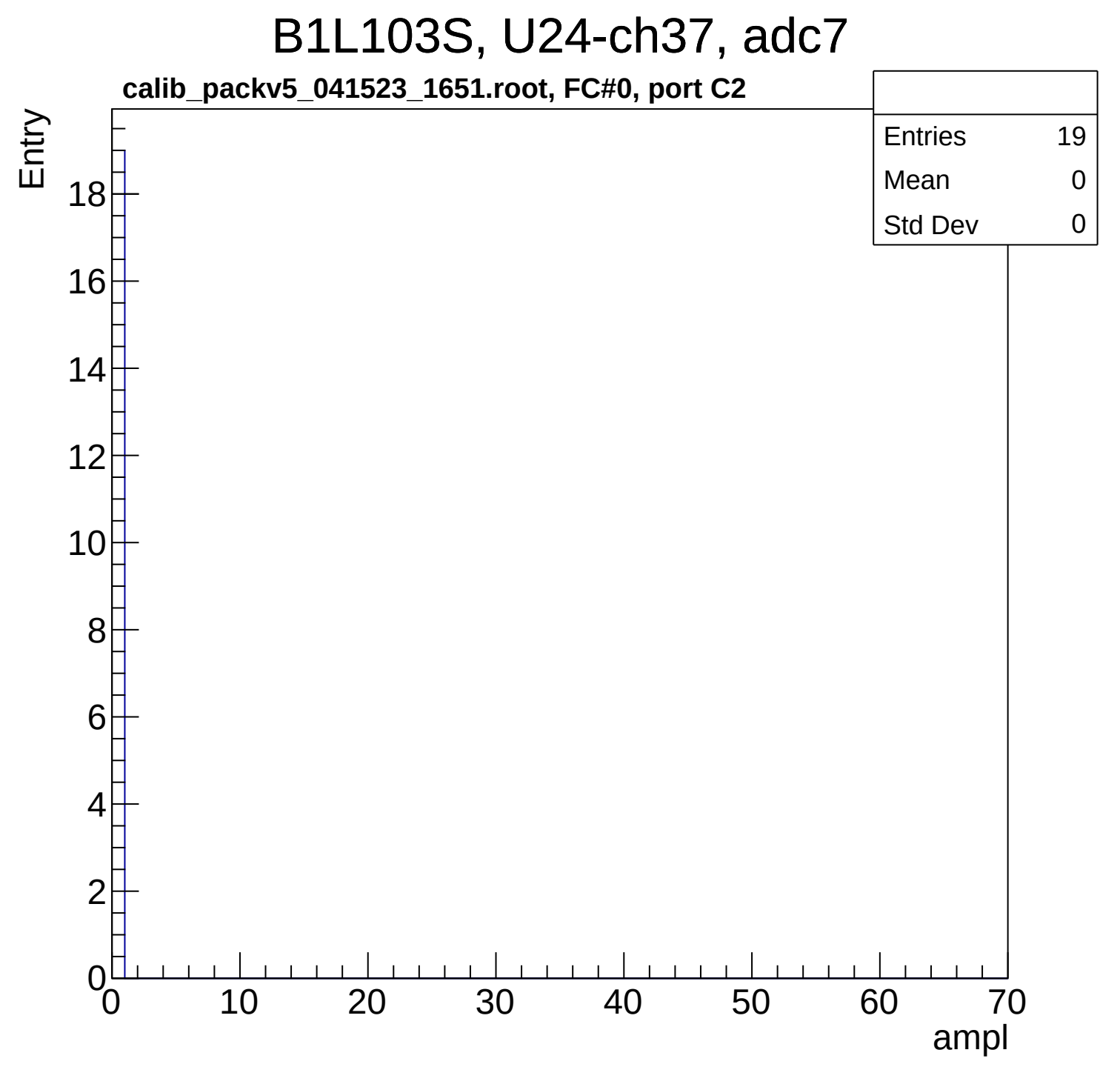
60
70


B1L103S, U24-ch37, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 3
Mean 62.67
Std Dev 0.4714
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U24-ch37, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
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10
20
30
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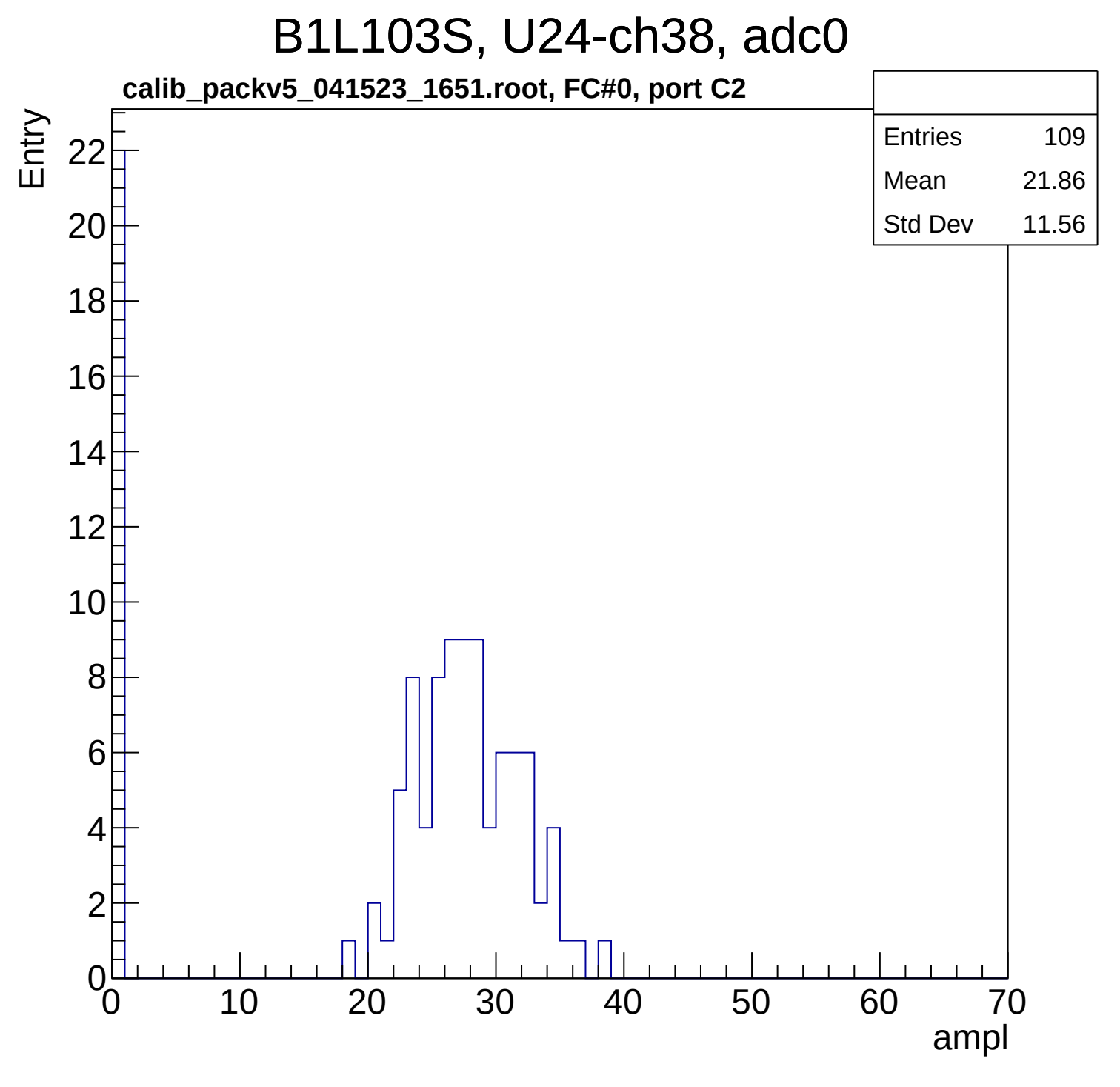
50
60
70
ampl


B1L103S, U24-ch38, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 109
Mean 21.86
Std Dev 11.56
Entry
0
2
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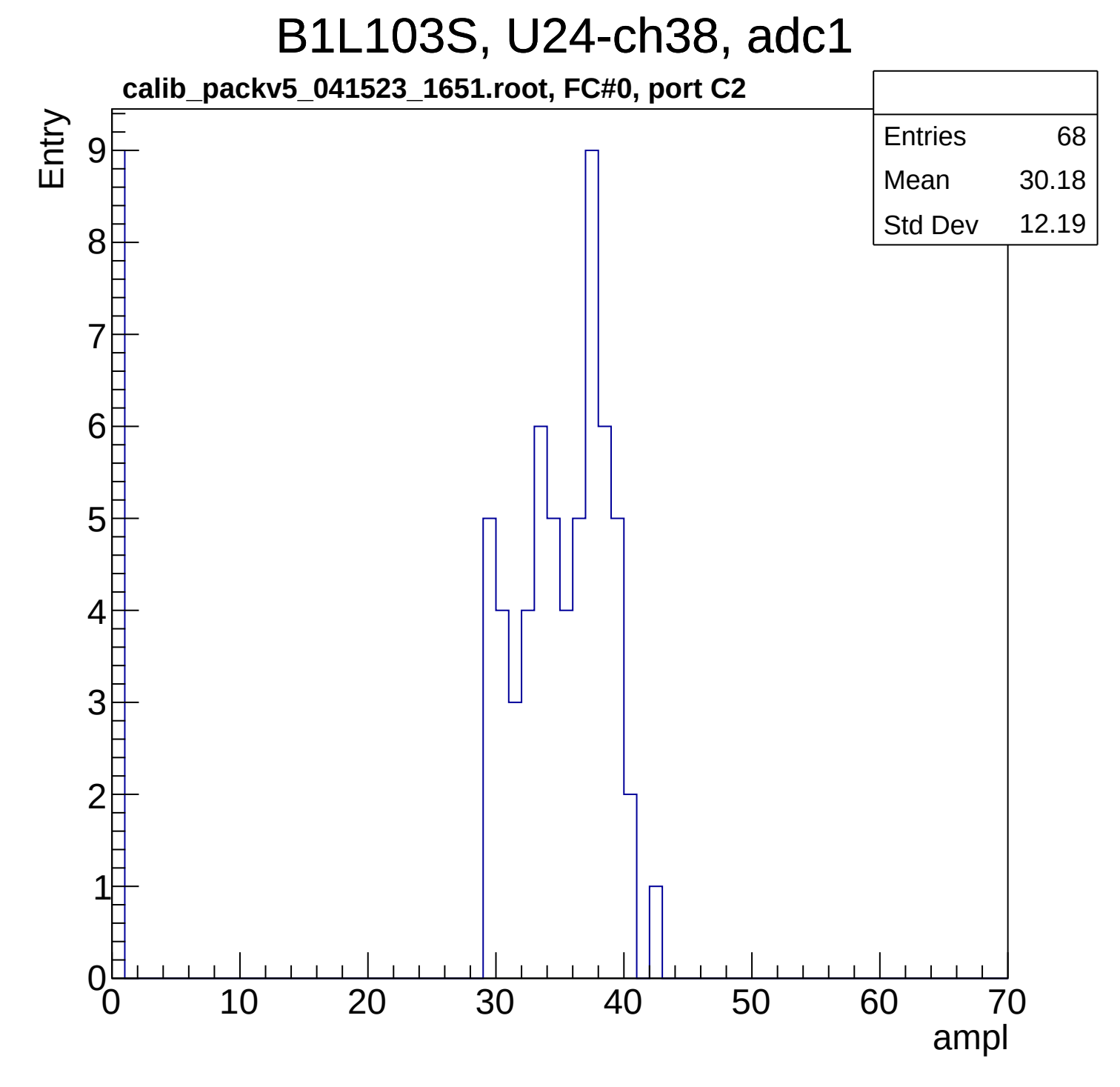
10
12
14
16
18
20
22
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch38, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 30.18
Std Dev 12.19
Entry
ampl
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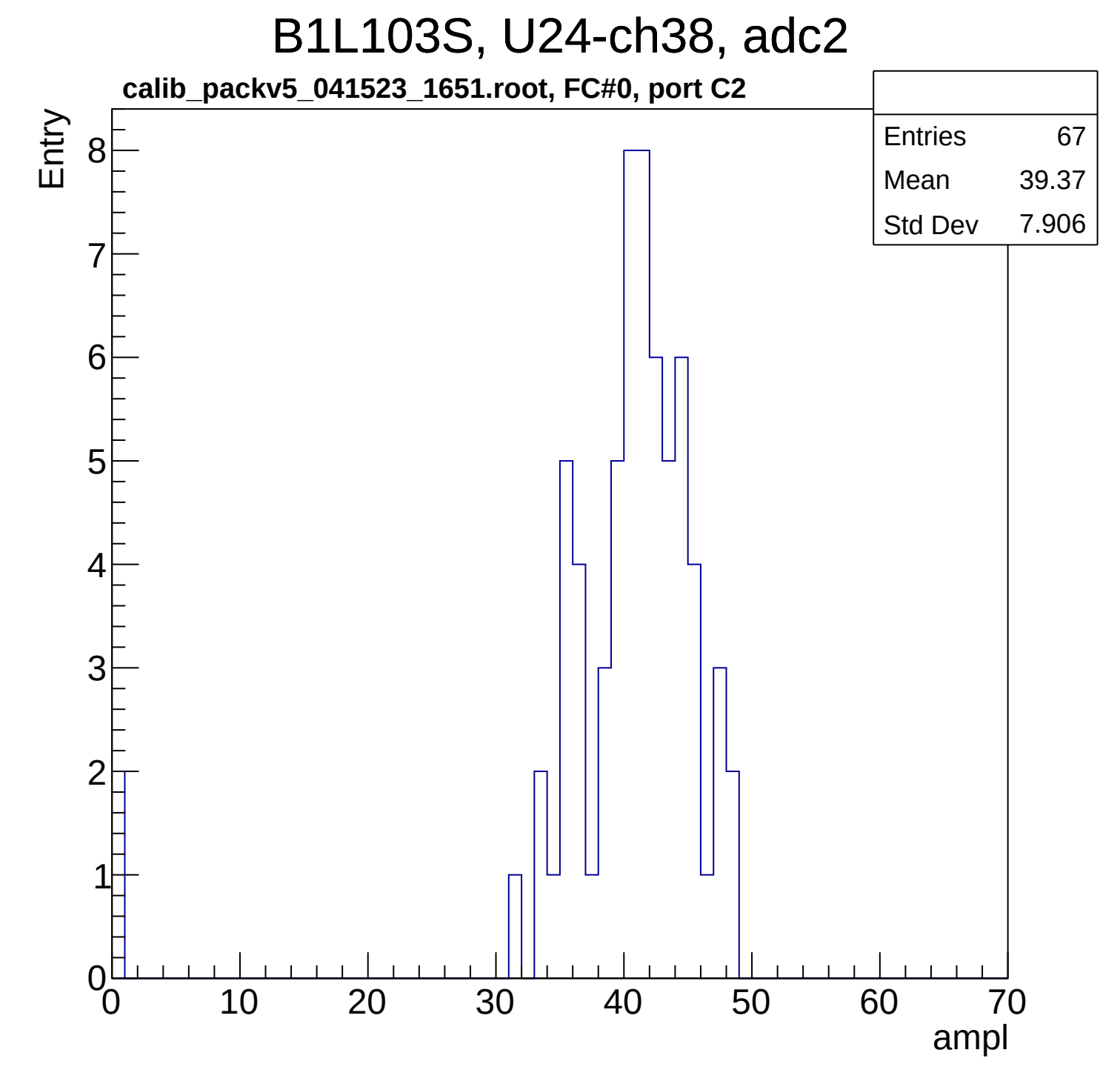
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U24-ch38, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 39.37
Std Dev 7.906
Entry
ampl
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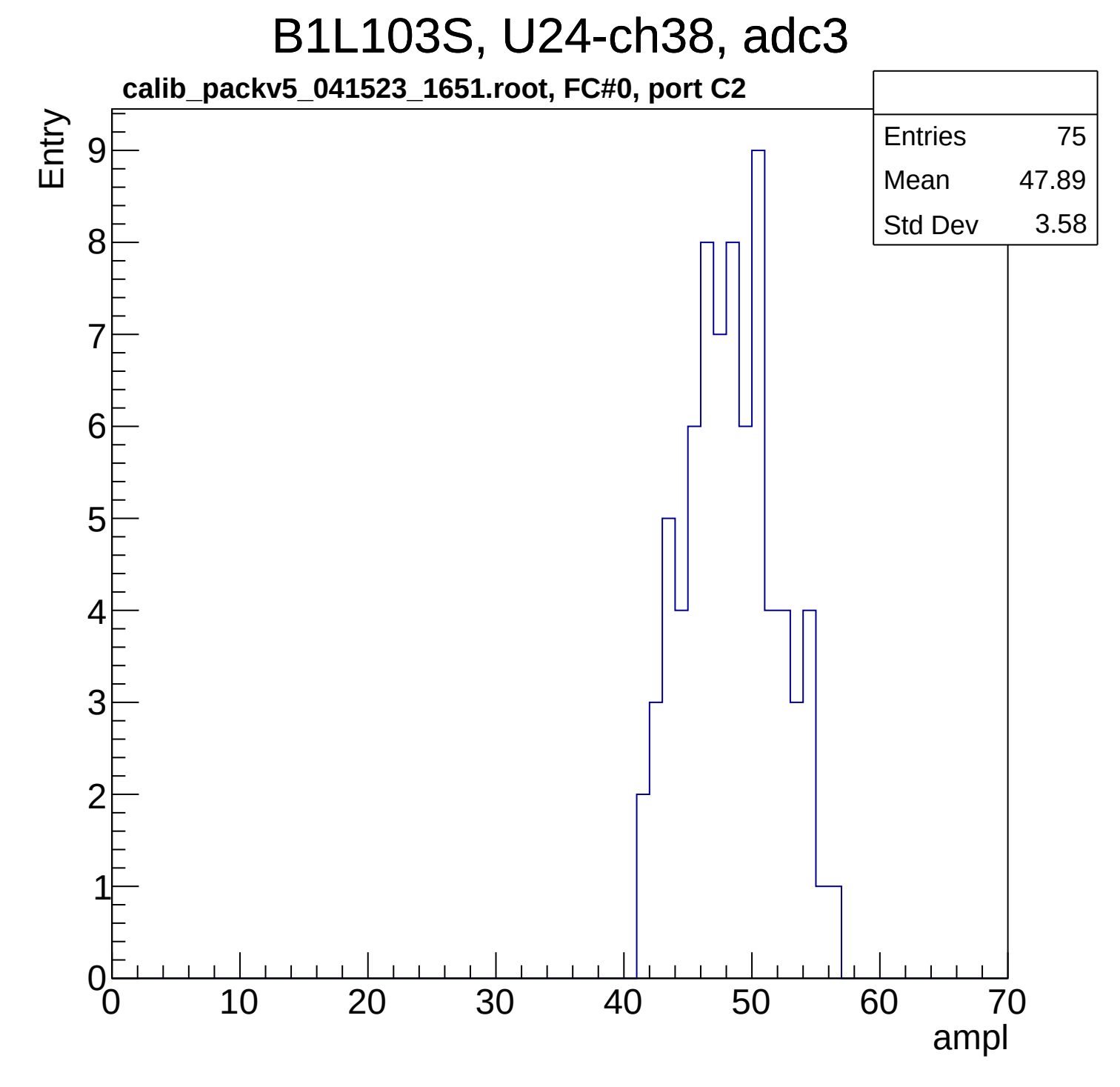
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U24-ch38, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 47.89
Std Dev 3.58
Entry
ampl
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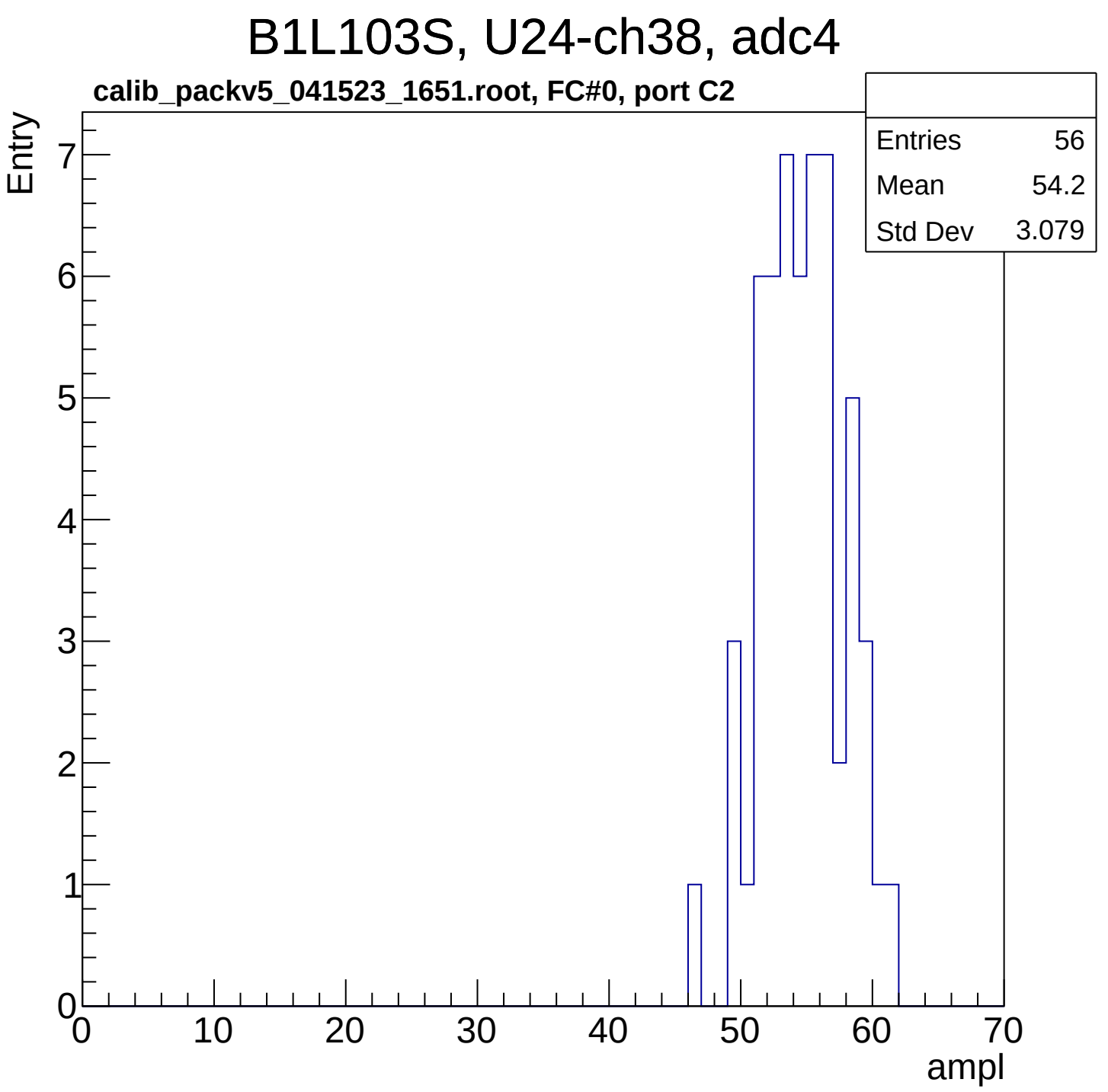
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U24-ch38, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 54.2
Std Dev 3.079
Entry
ampl
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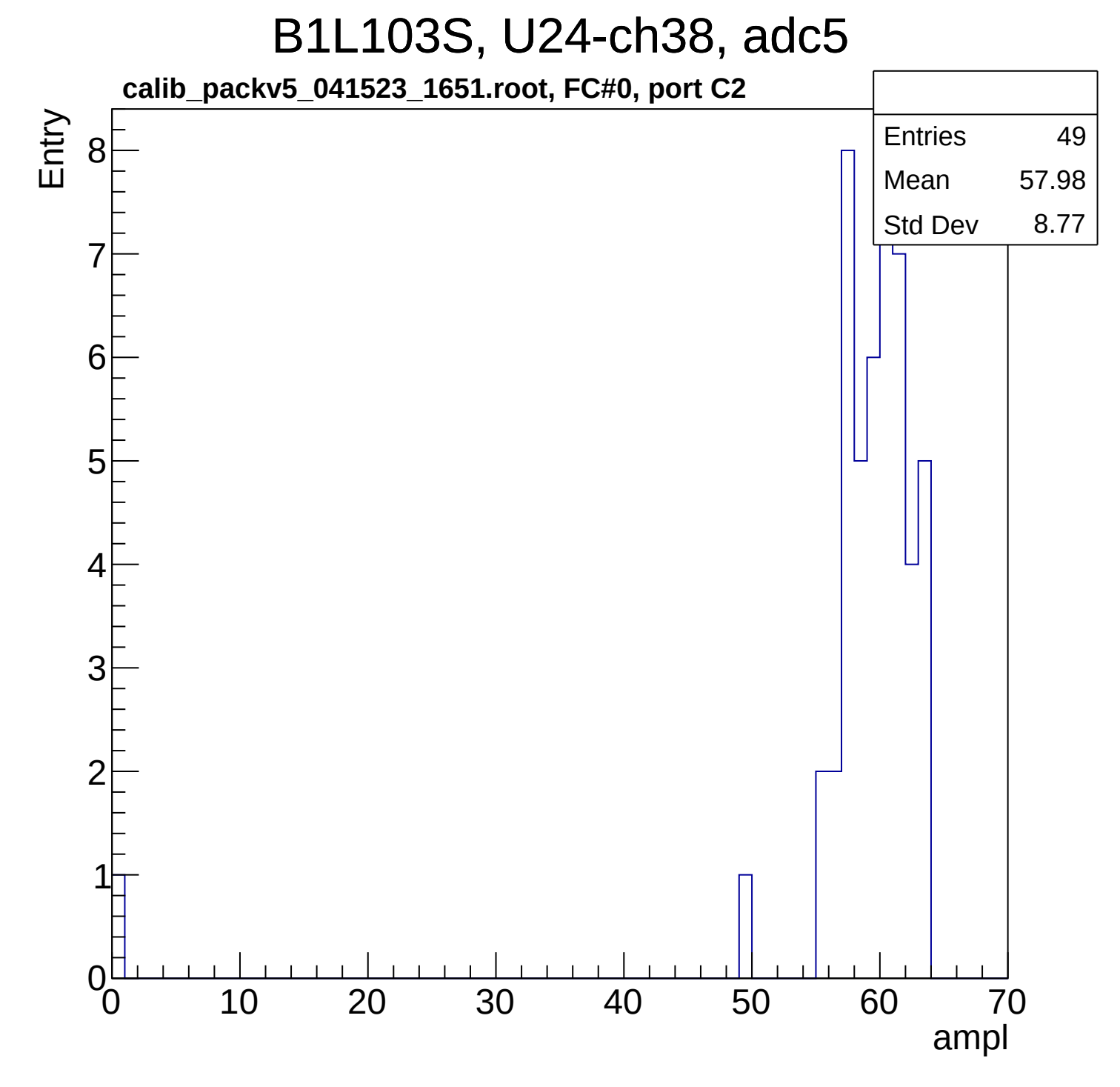
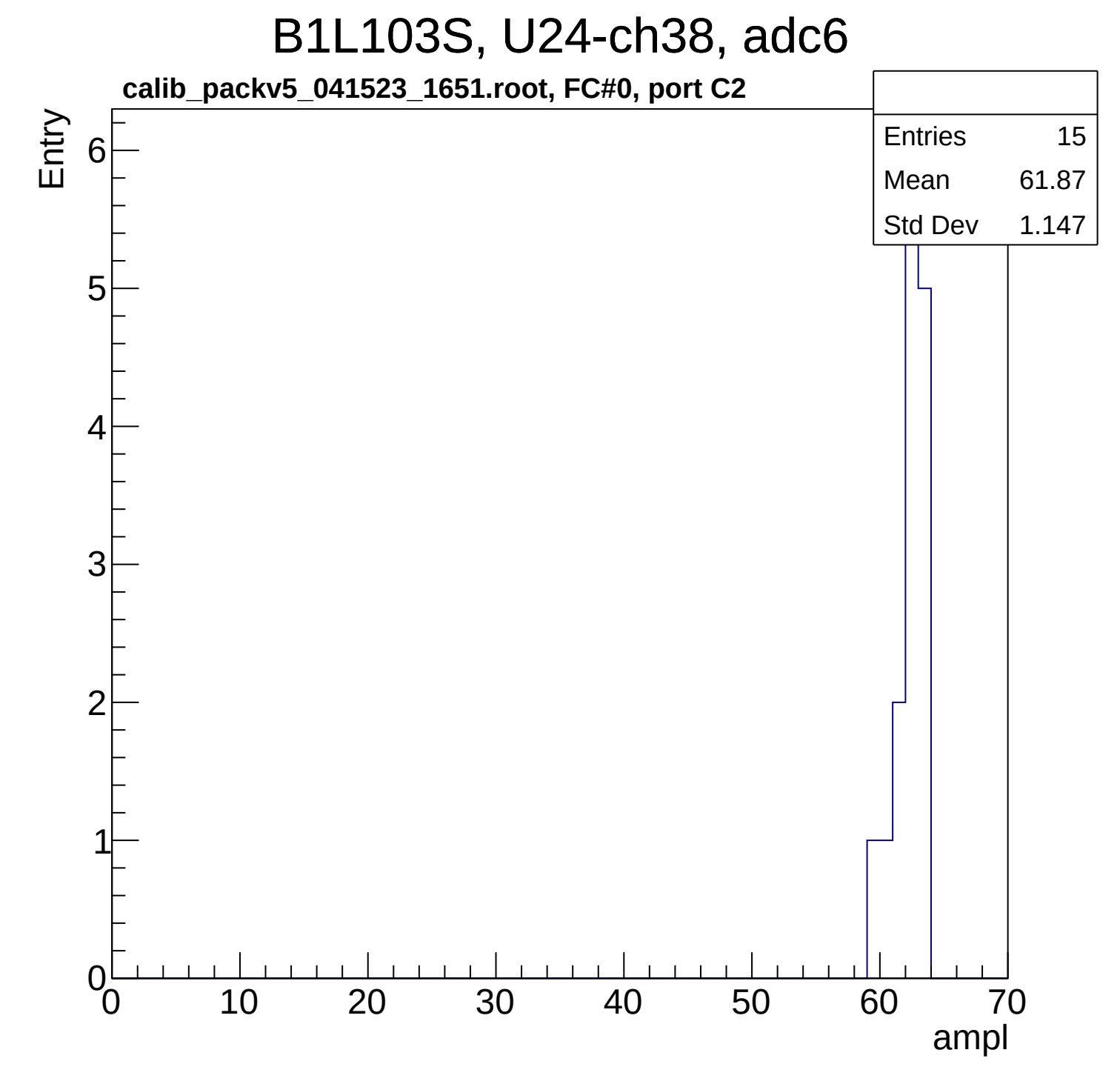
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U24-ch38, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 57.98
Std Dev 8.77
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U24-ch38, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 15
Mean 61.87
Std Dev 1.147
Entry
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1
2
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4
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6
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10
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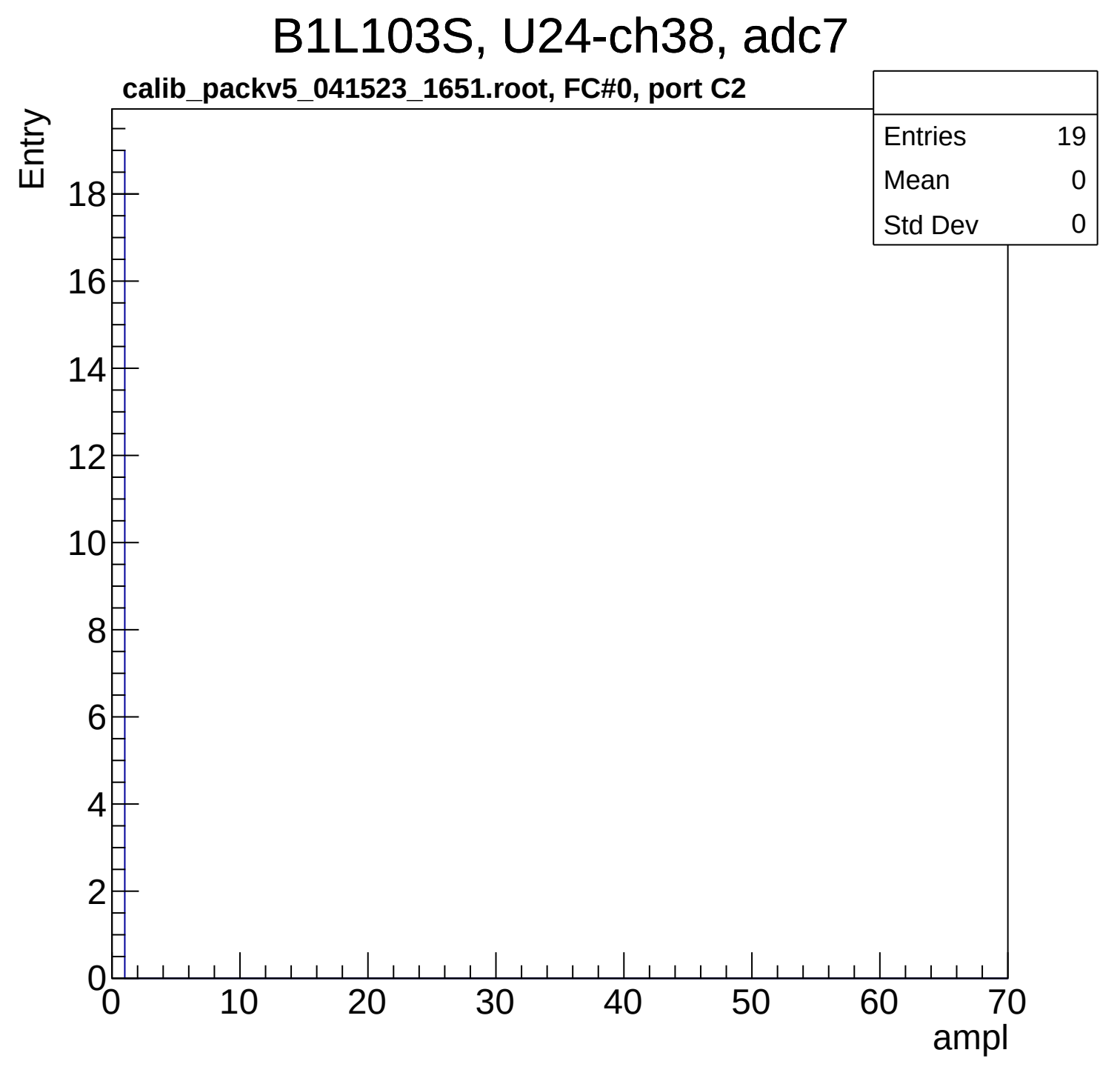
70
ampl


B1L103S, U24-ch38, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
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10
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10
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50
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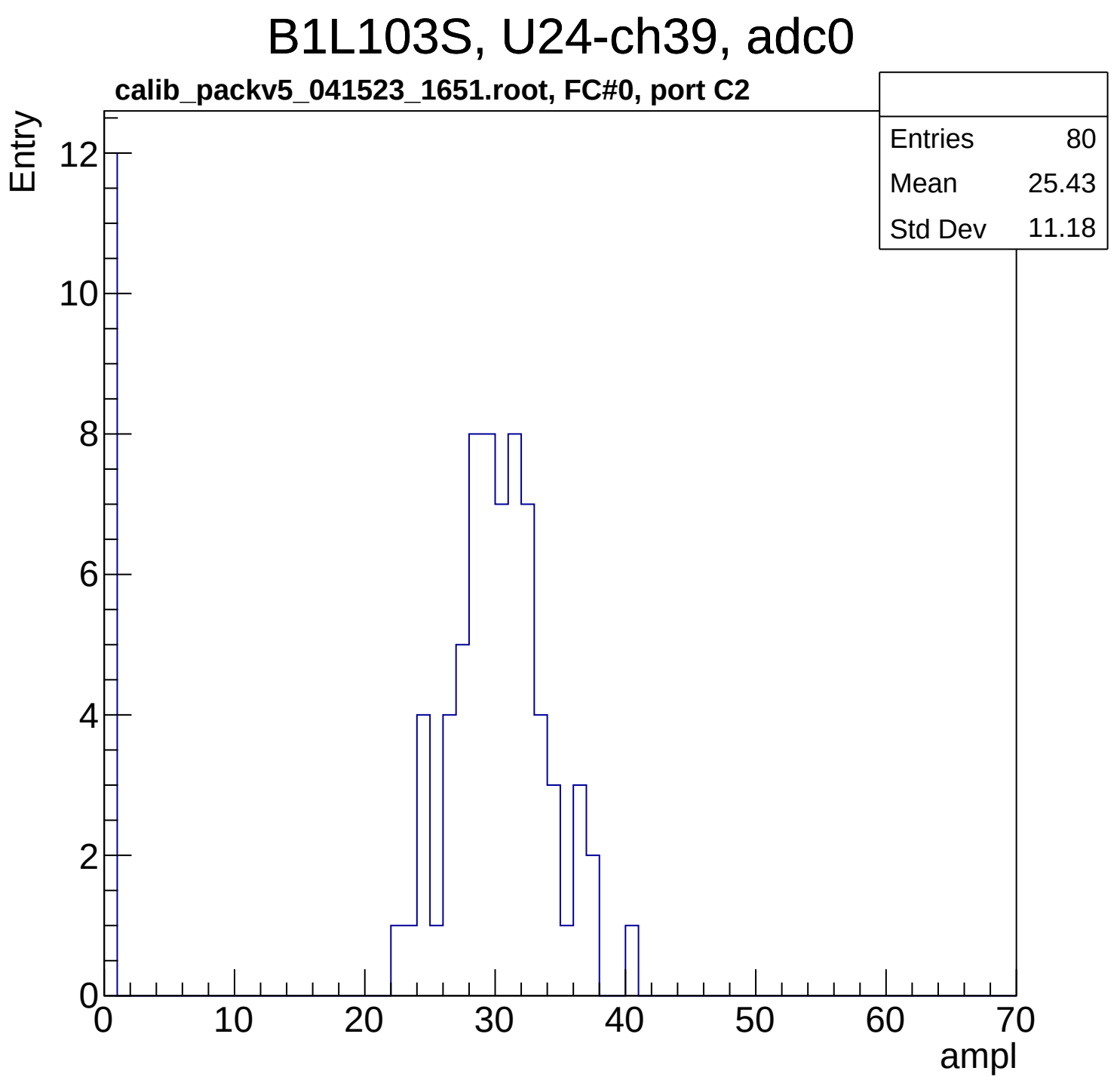
ampl


B1L103S, U24-ch39, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 25.43
Std Dev 11.18
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2
4
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8
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12
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10
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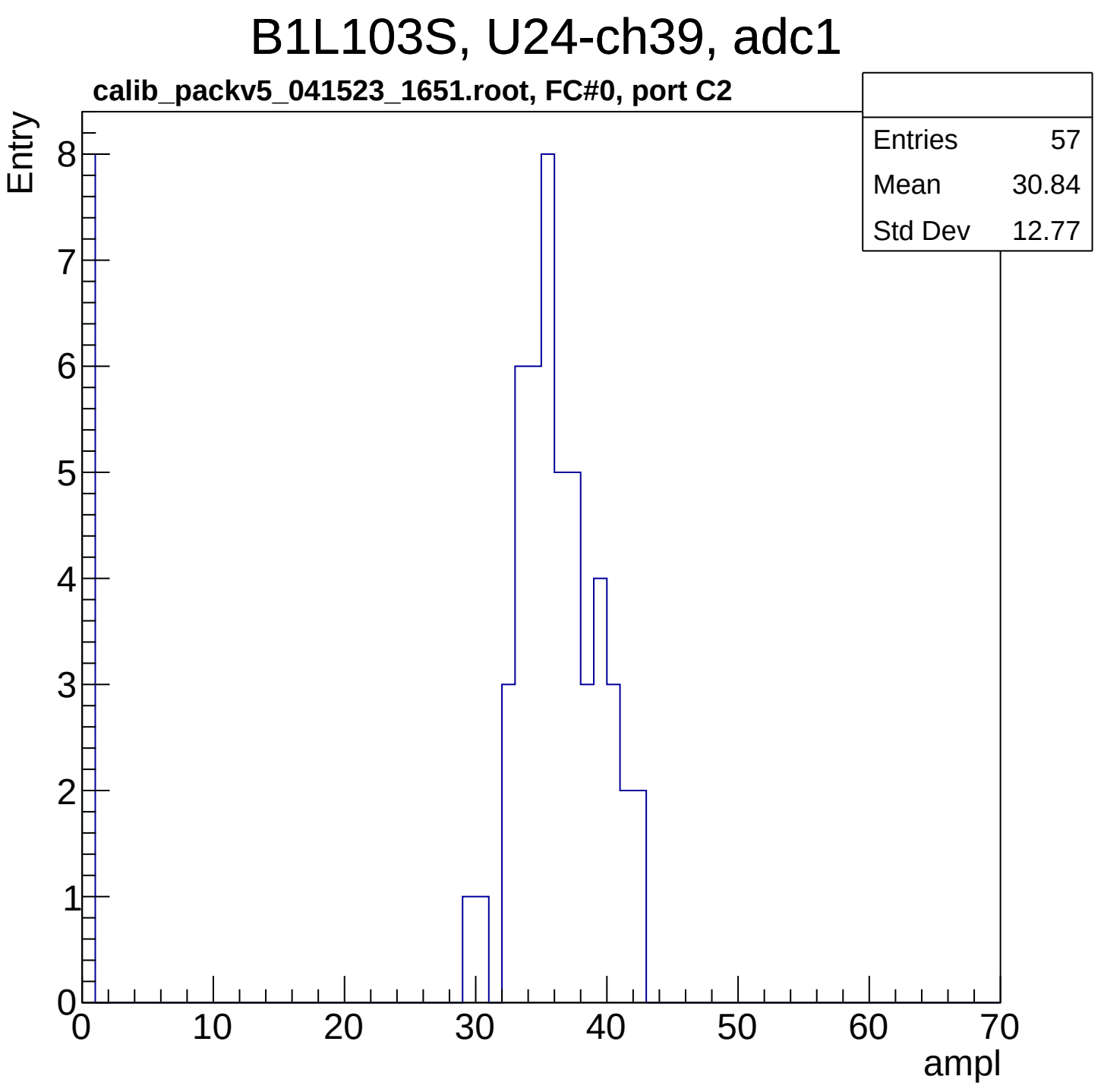
70
ampl


B1L103S, U24-ch39, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 30.84
Std Dev 12.77
Entry
ampl
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3
4
5
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7
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0
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40
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60
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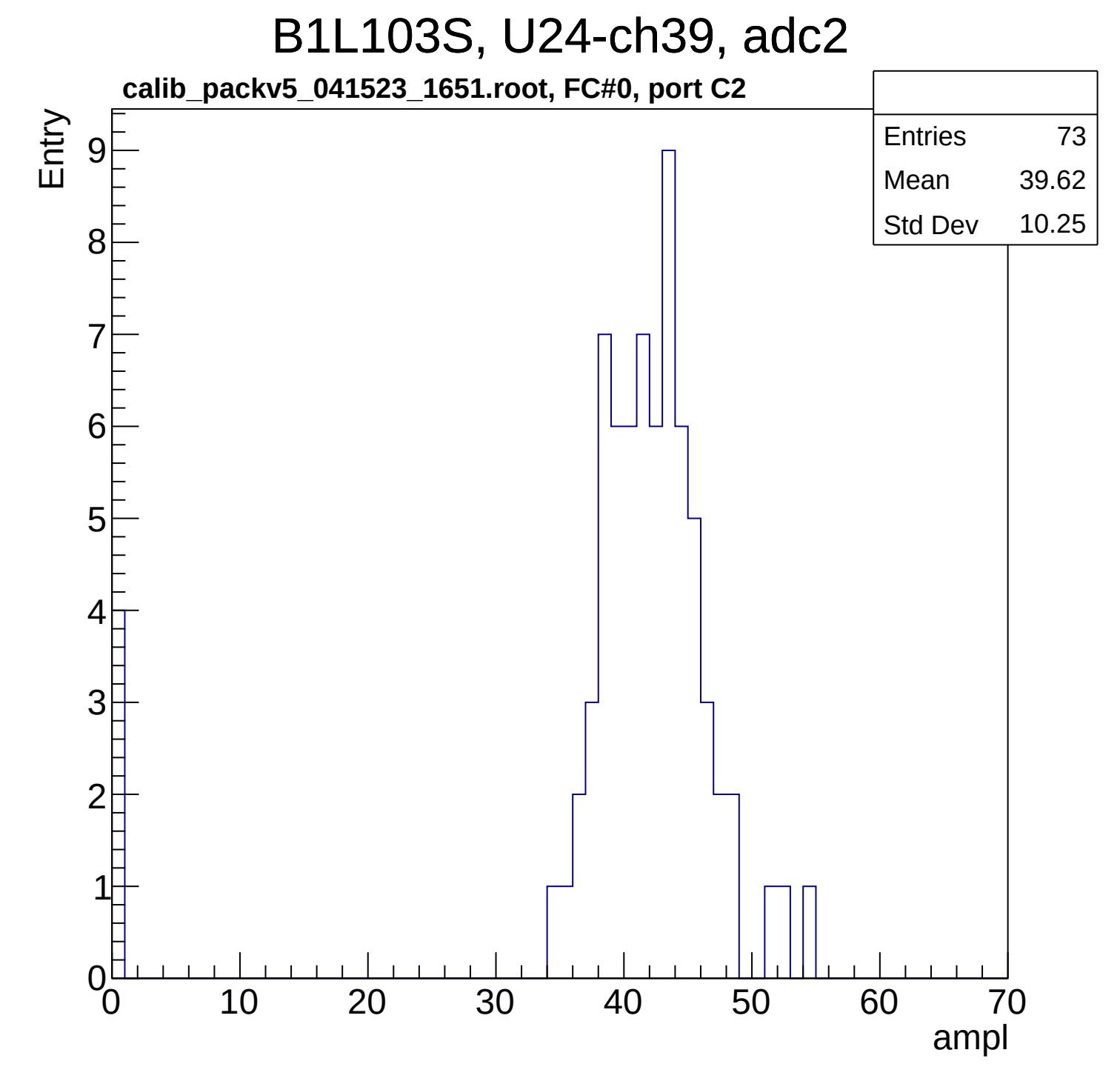
B1L103S, U24-ch39, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 39.62
Std Dev 10.25
Entry
ampl
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2
3
4
5
6
7
8
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0
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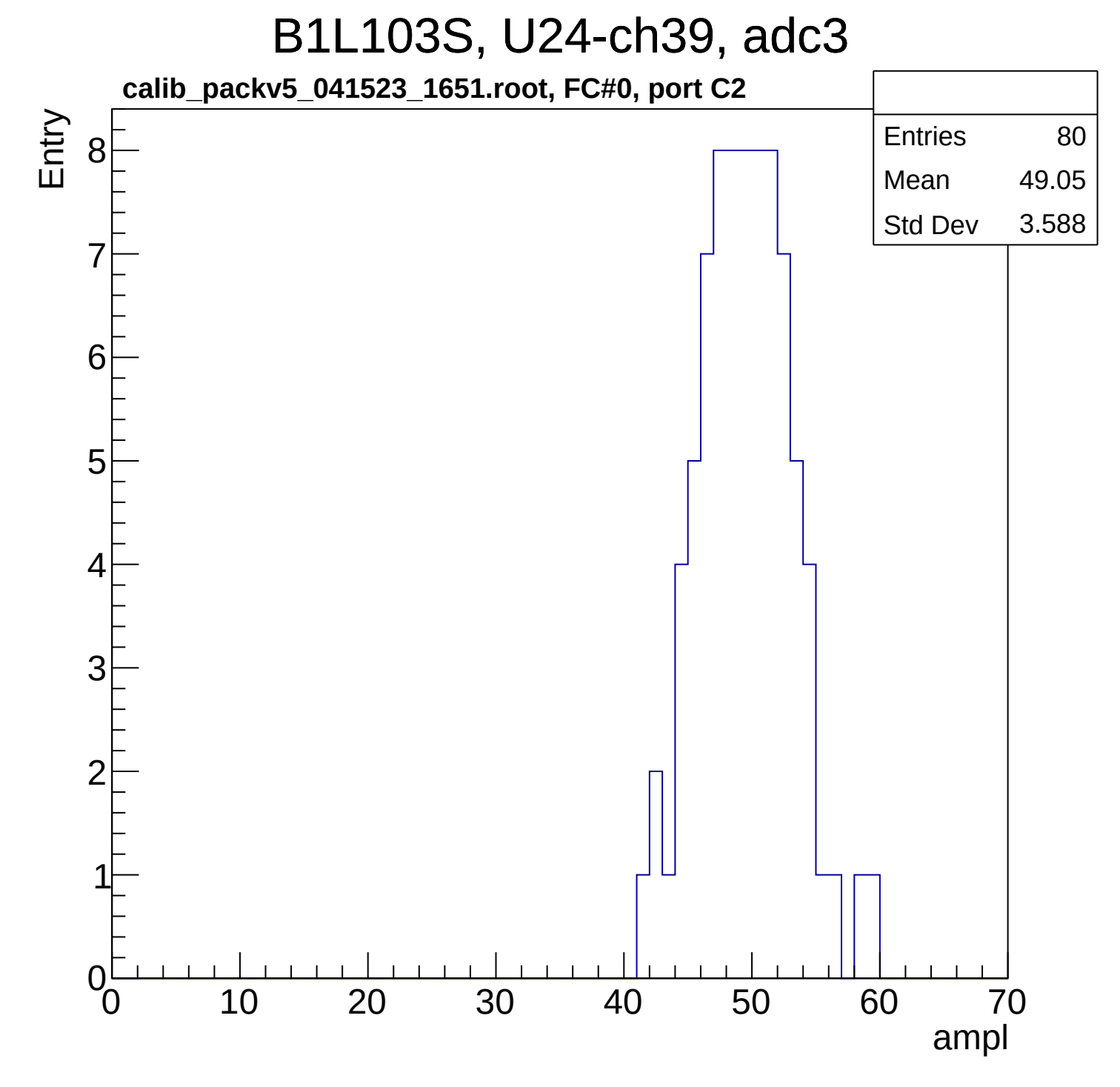
B1L103S, U24-ch39, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 49.05
Std Dev 3.588
Entry
ampl
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7
8
0
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40
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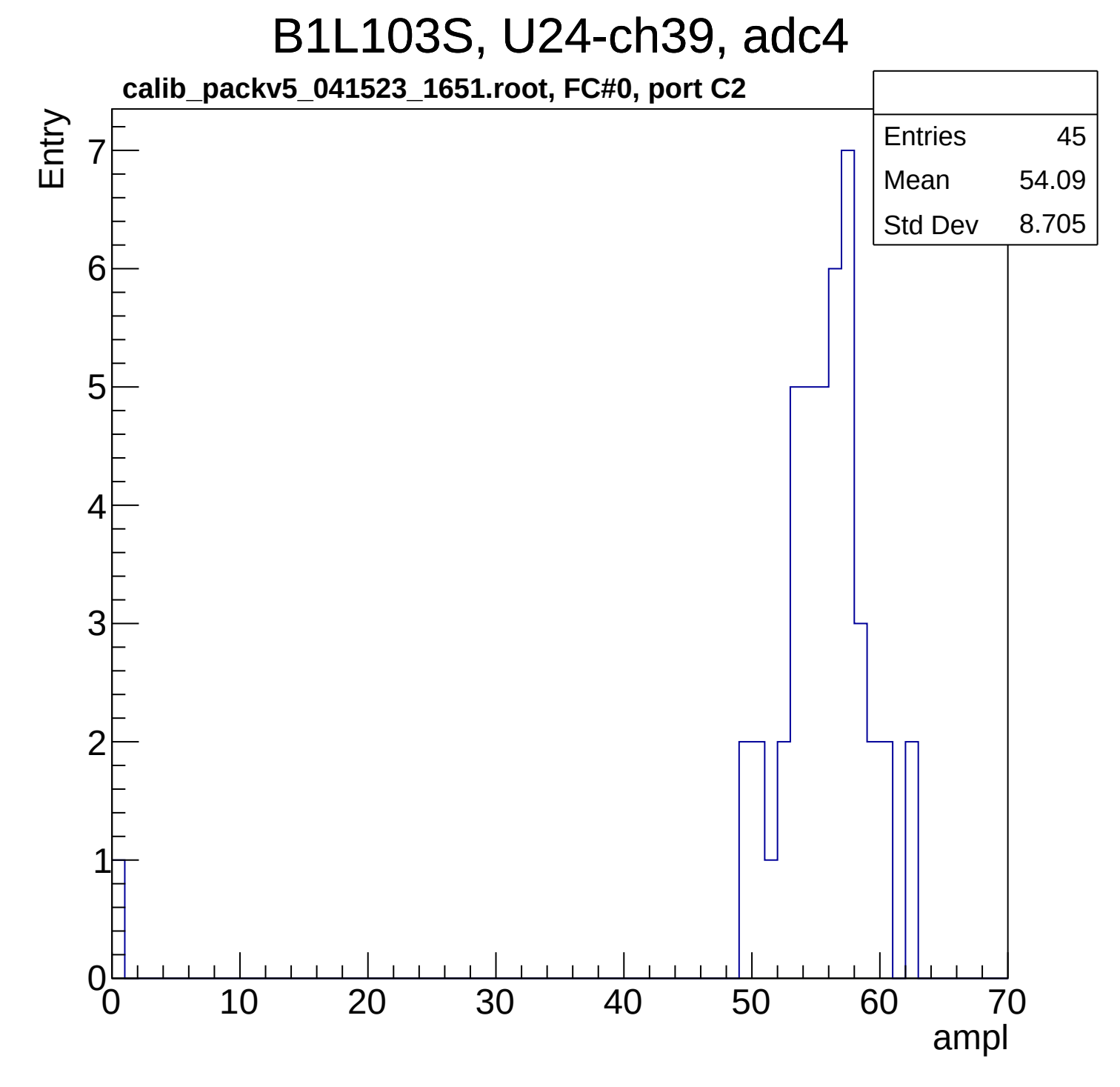
B1L103S, U24-ch39, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 54.09
Std Dev 8.705
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
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40
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60
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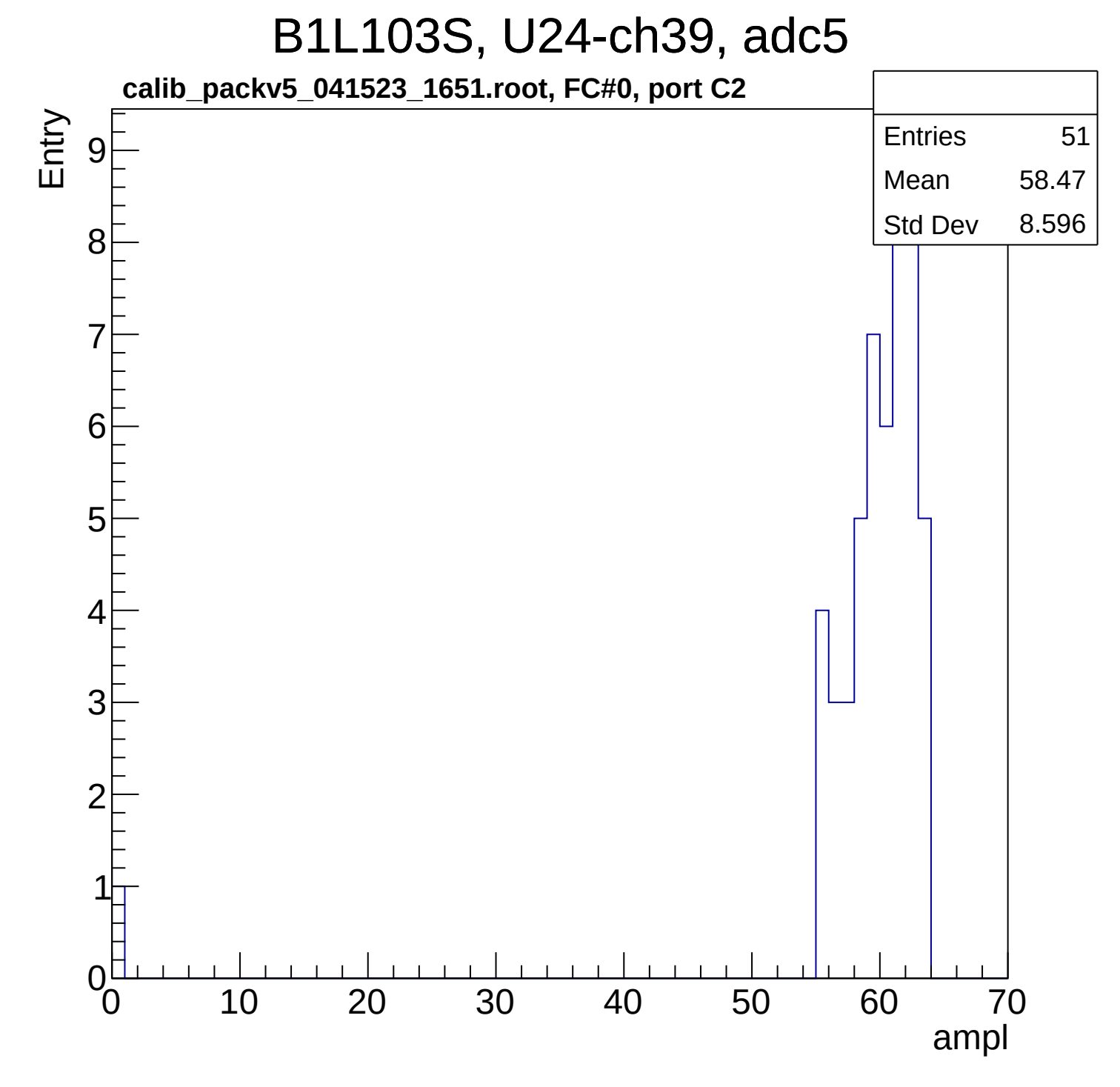
B1L103S, U24-ch39, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 58.47
Std Dev 8.596
Entry
ampl
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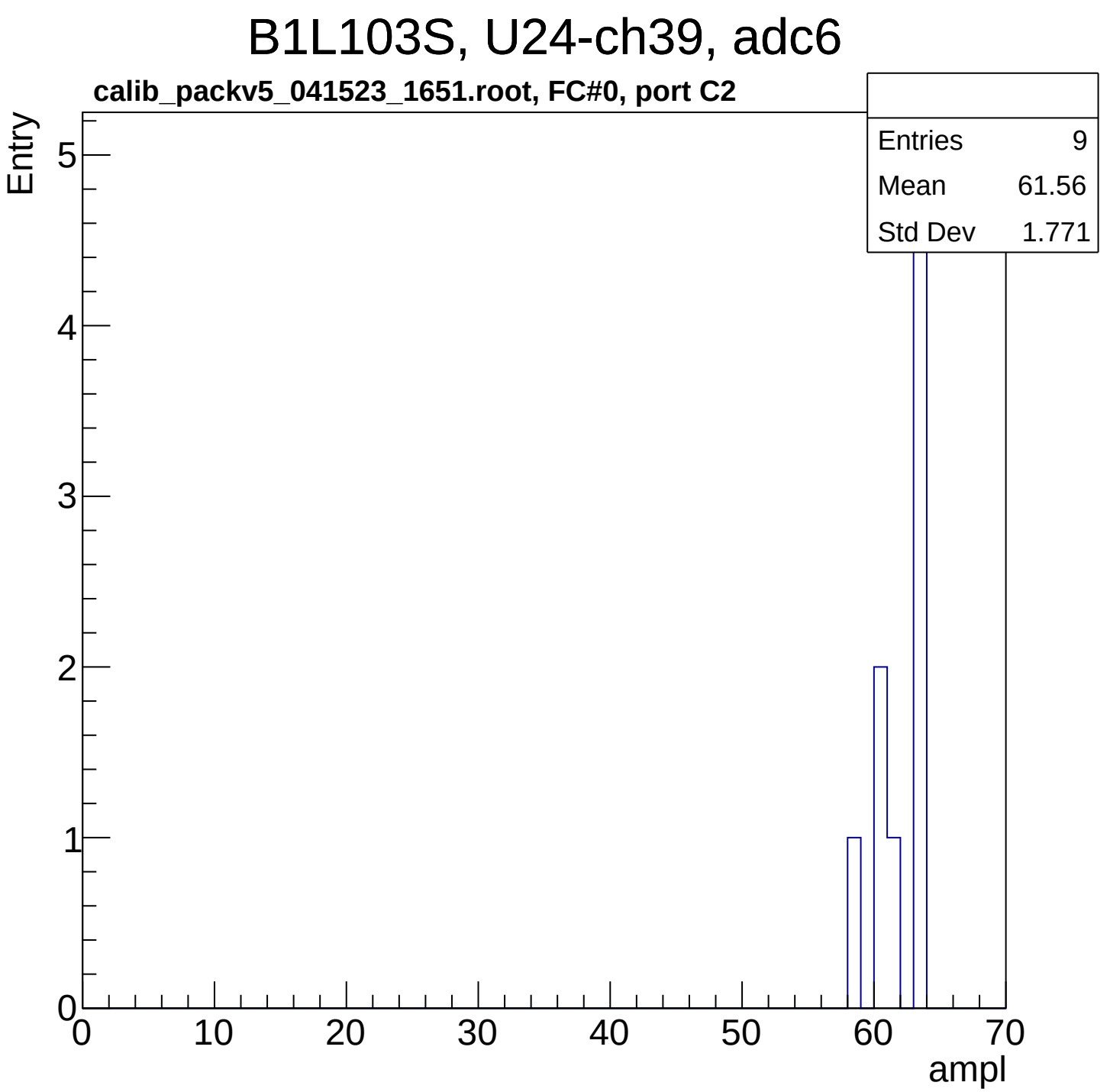
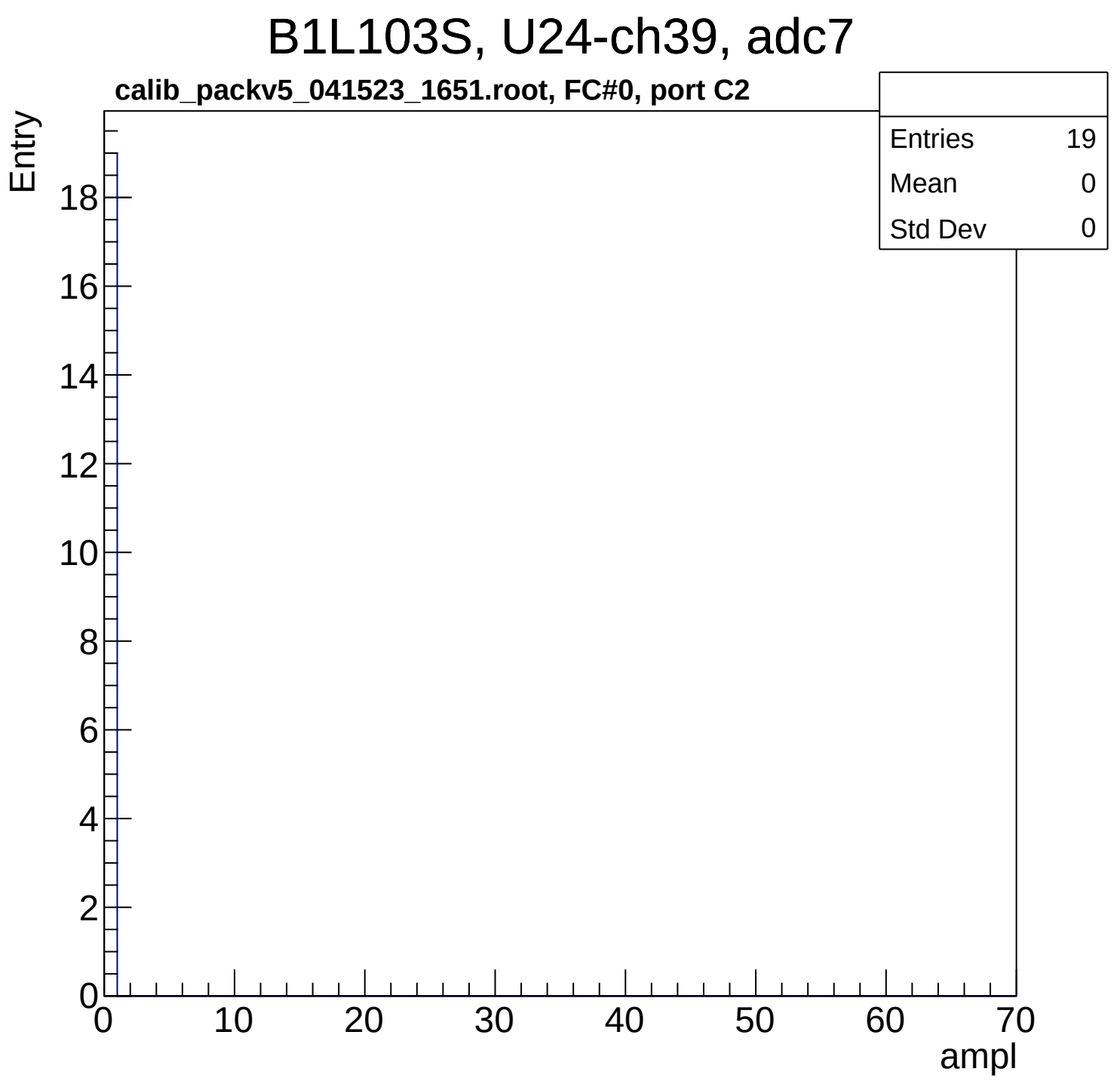
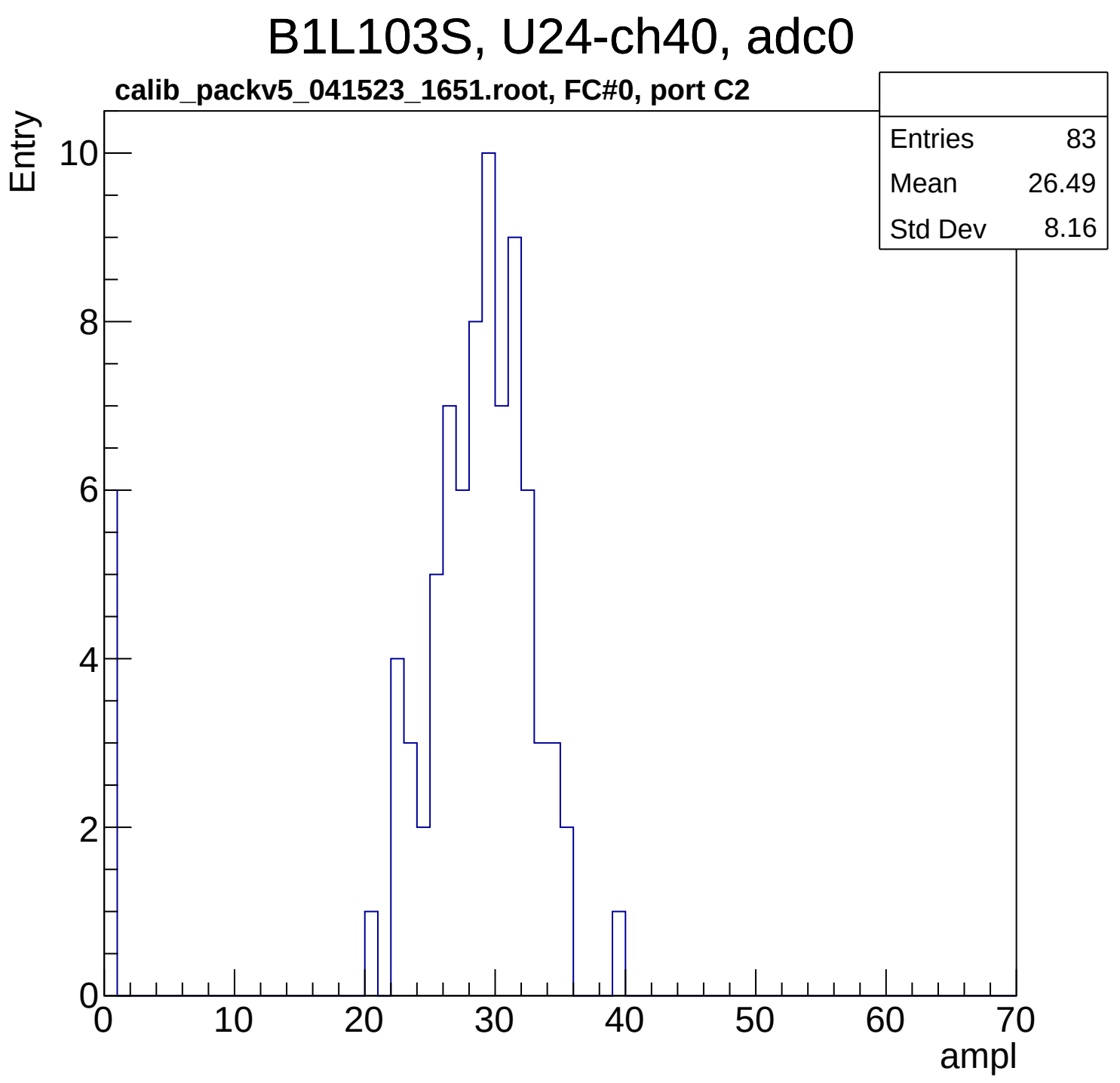
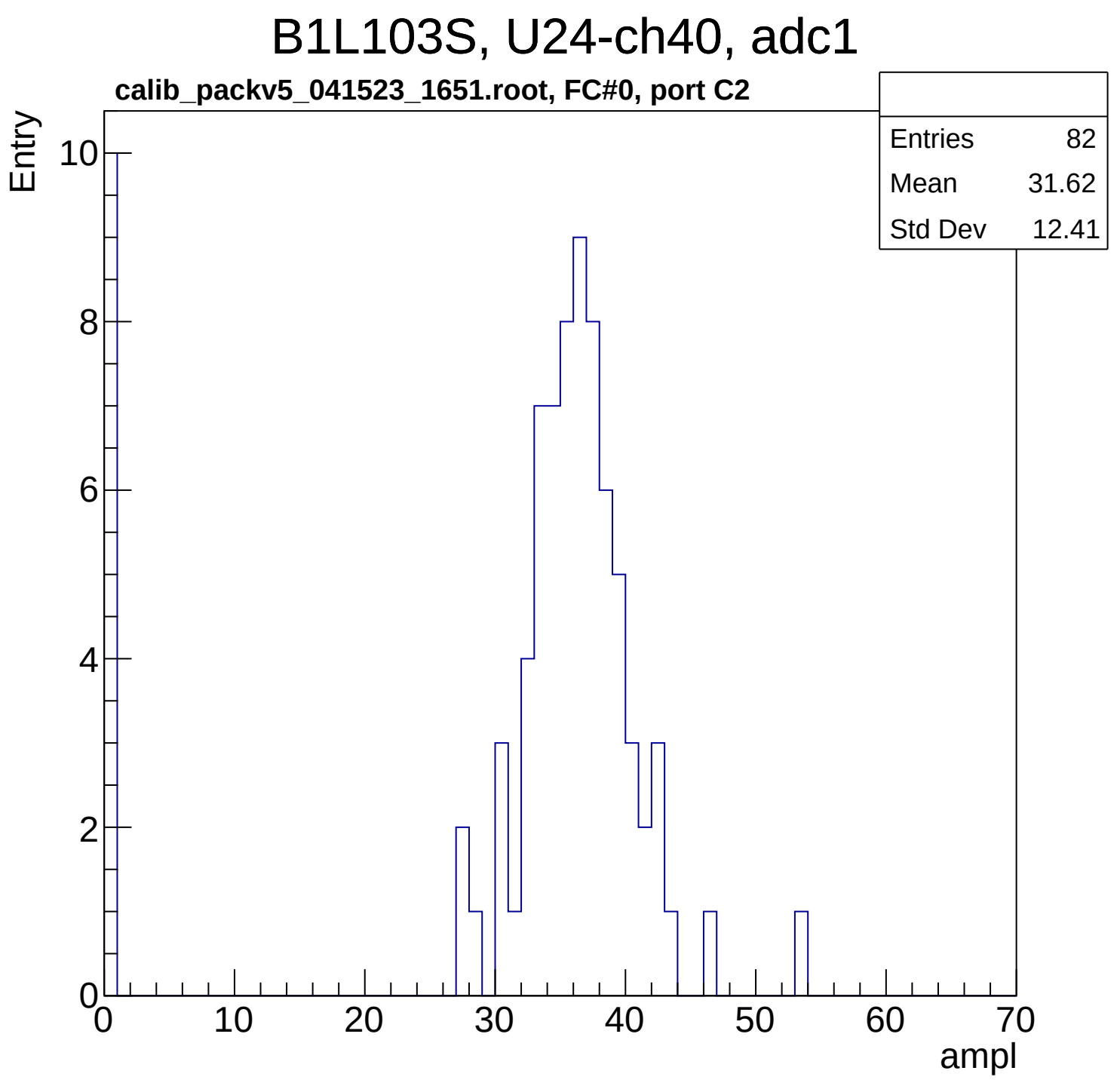
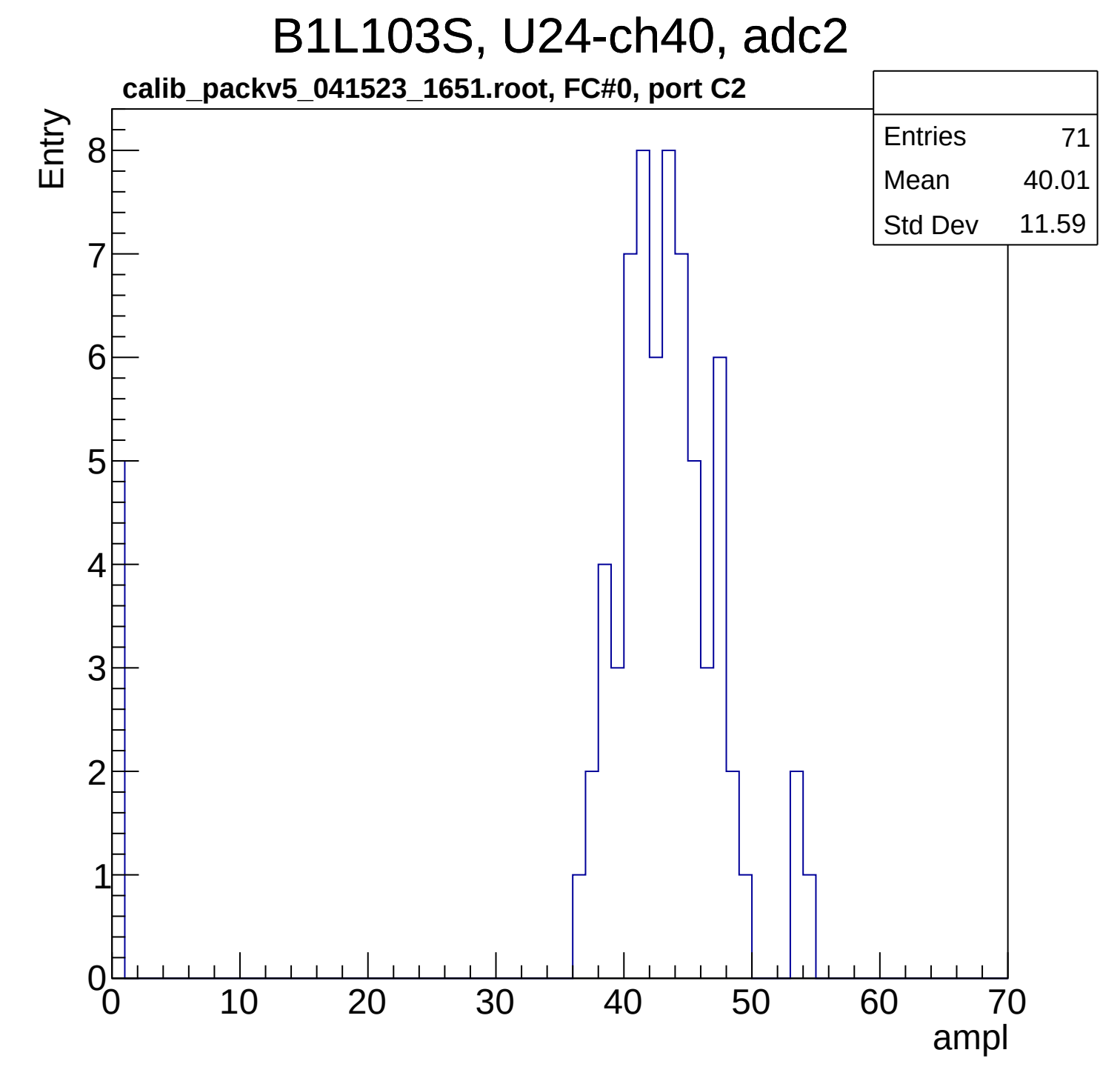

B1L103S, U24-ch39, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 9
Mean 61.56
Std Dev 1.771
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch39, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch40, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 26.49
Std Dev 8.16
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U24-ch40, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 31.62
Std Dev 12.41
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U24-ch40, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 40.01
Std Dev 11.59
Entry
ampl
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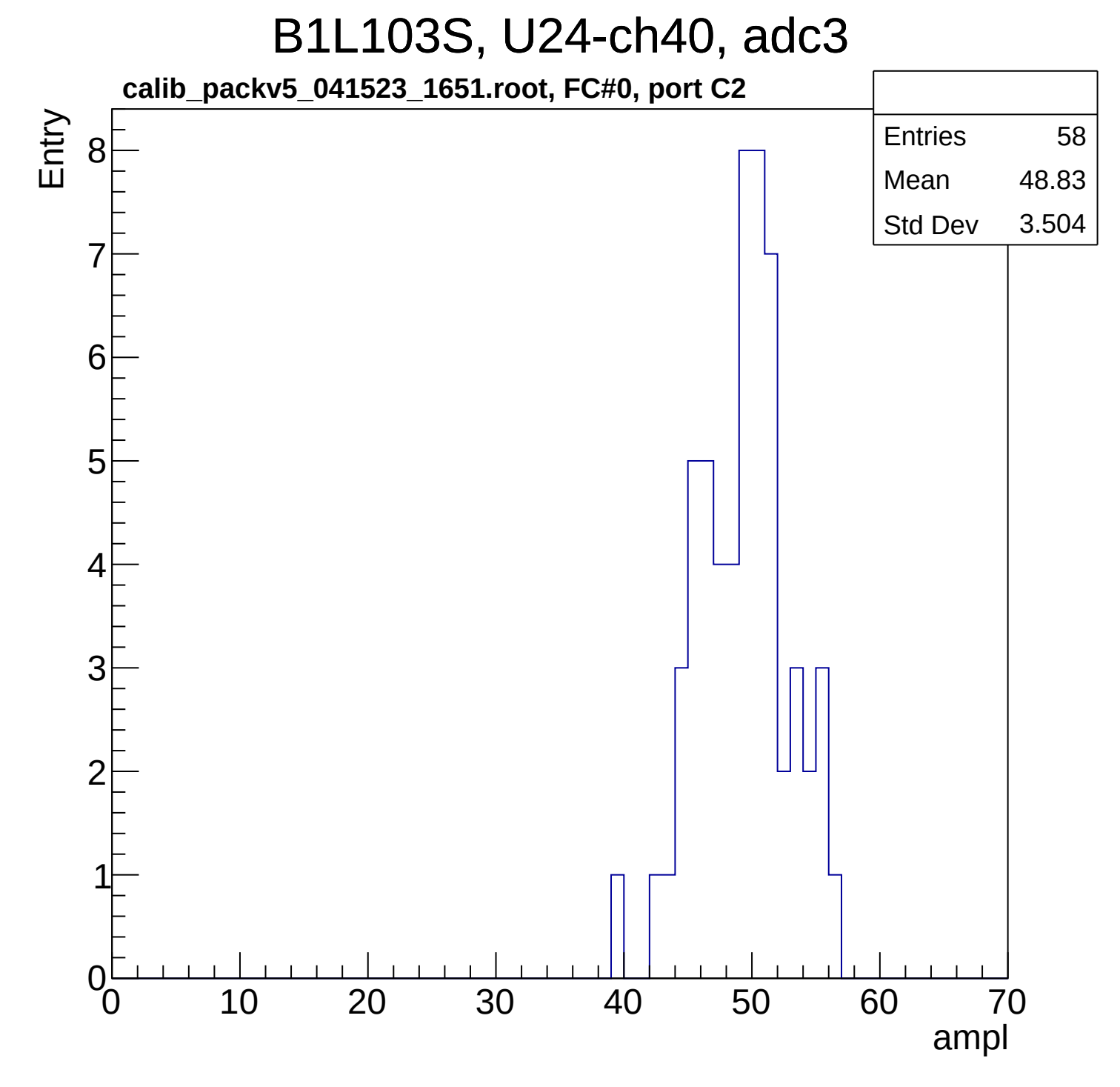
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U24-ch40, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 48.83
Std Dev 3.504
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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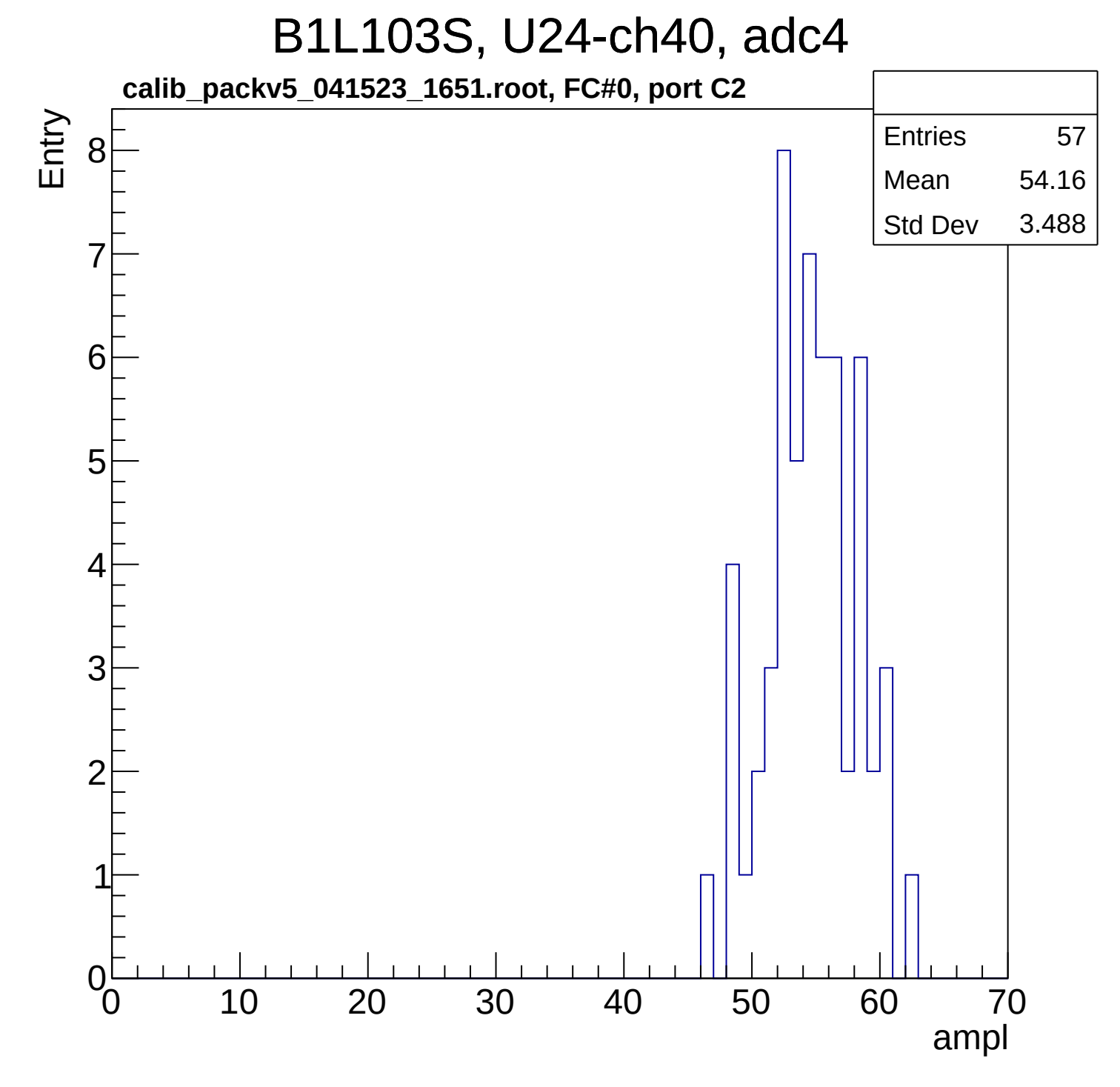
40
50
60
70


B1L103S, U24-ch40, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 54.16
Std Dev 3.488
Entry
ampl
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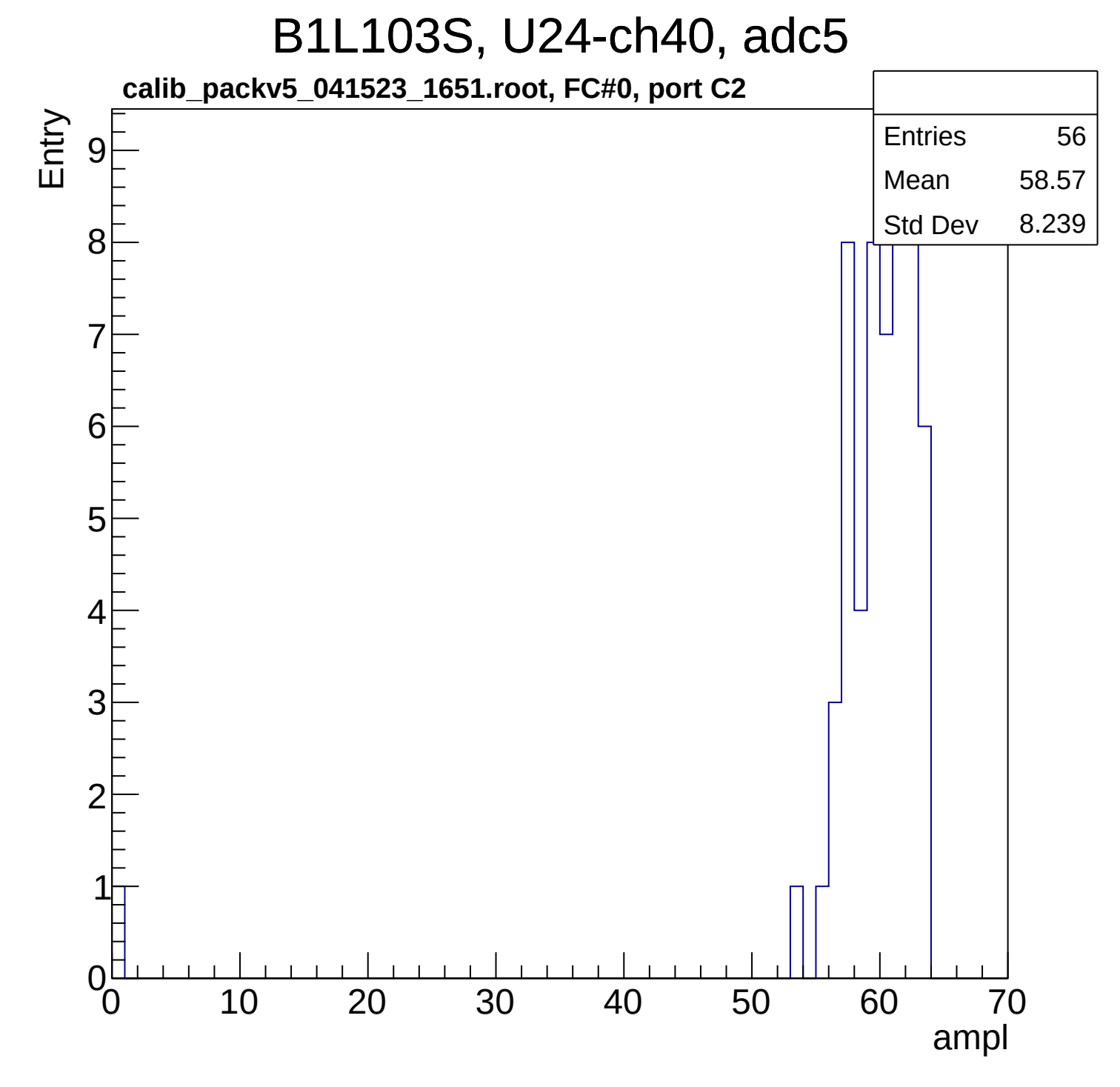
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U24-ch40, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 58.57
Std Dev 8.239
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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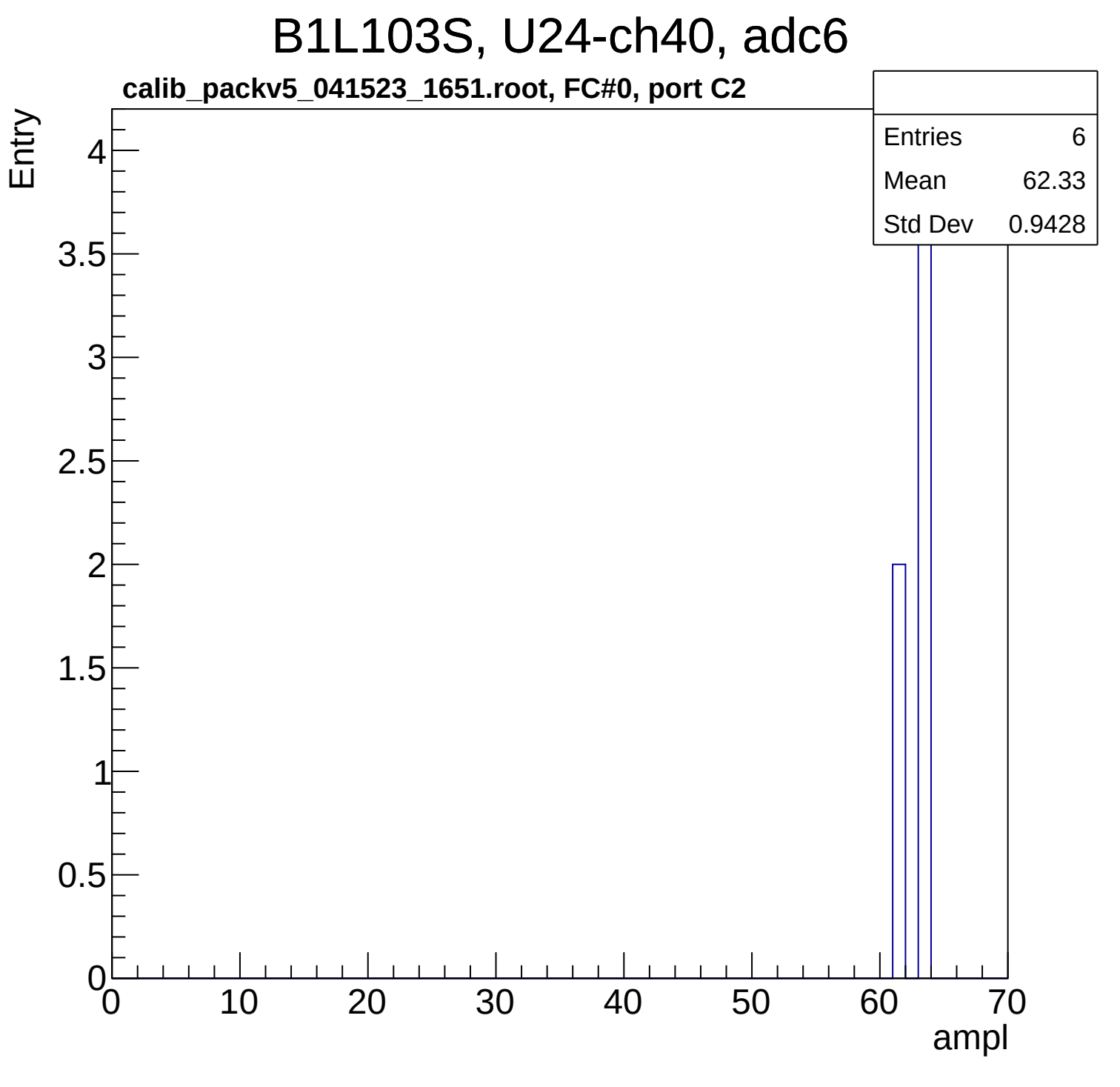
40
50
60
70


B1L103S, U24-ch40, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 62.33
Std Dev 0.9428
Entry
ampl
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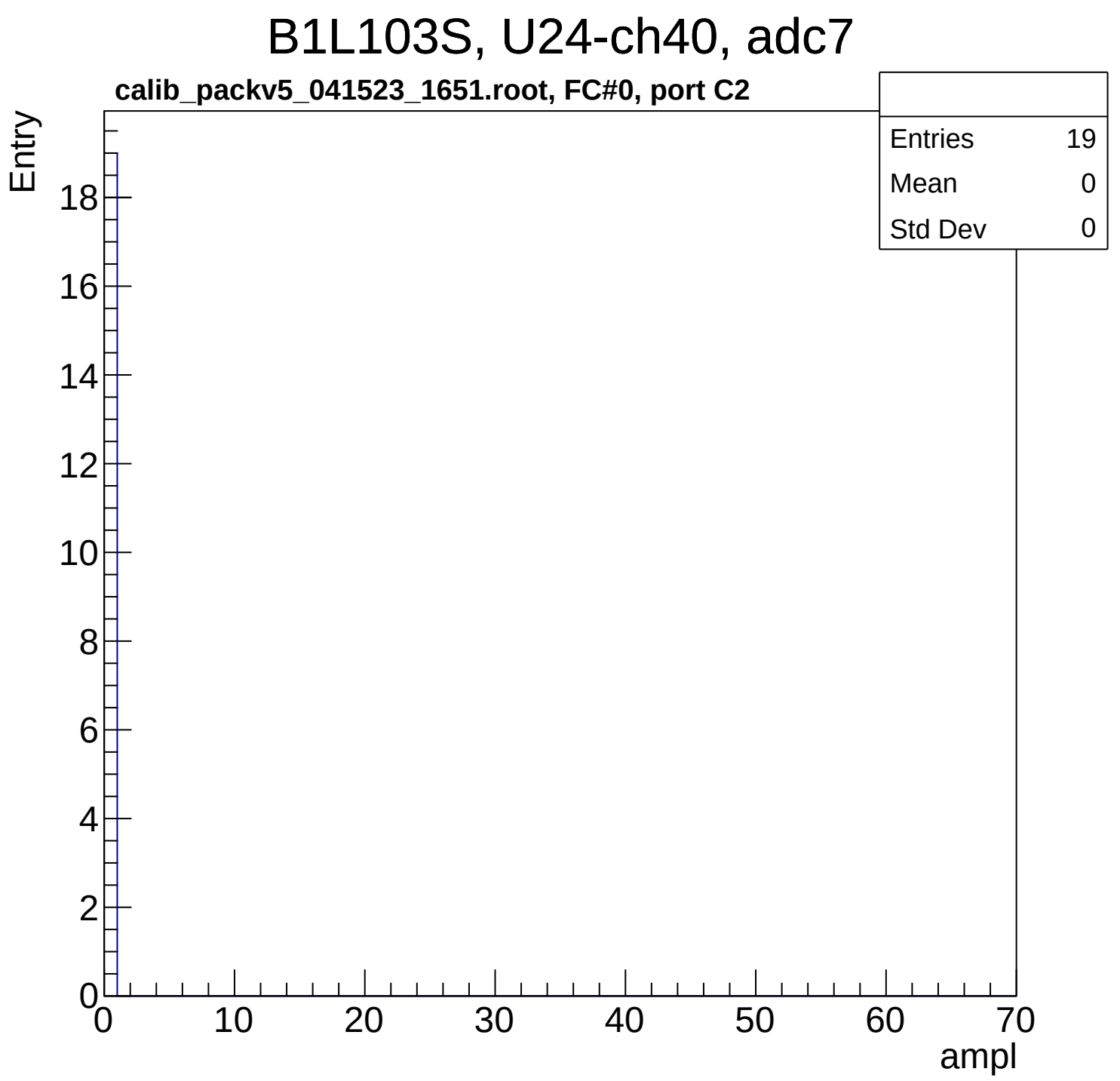
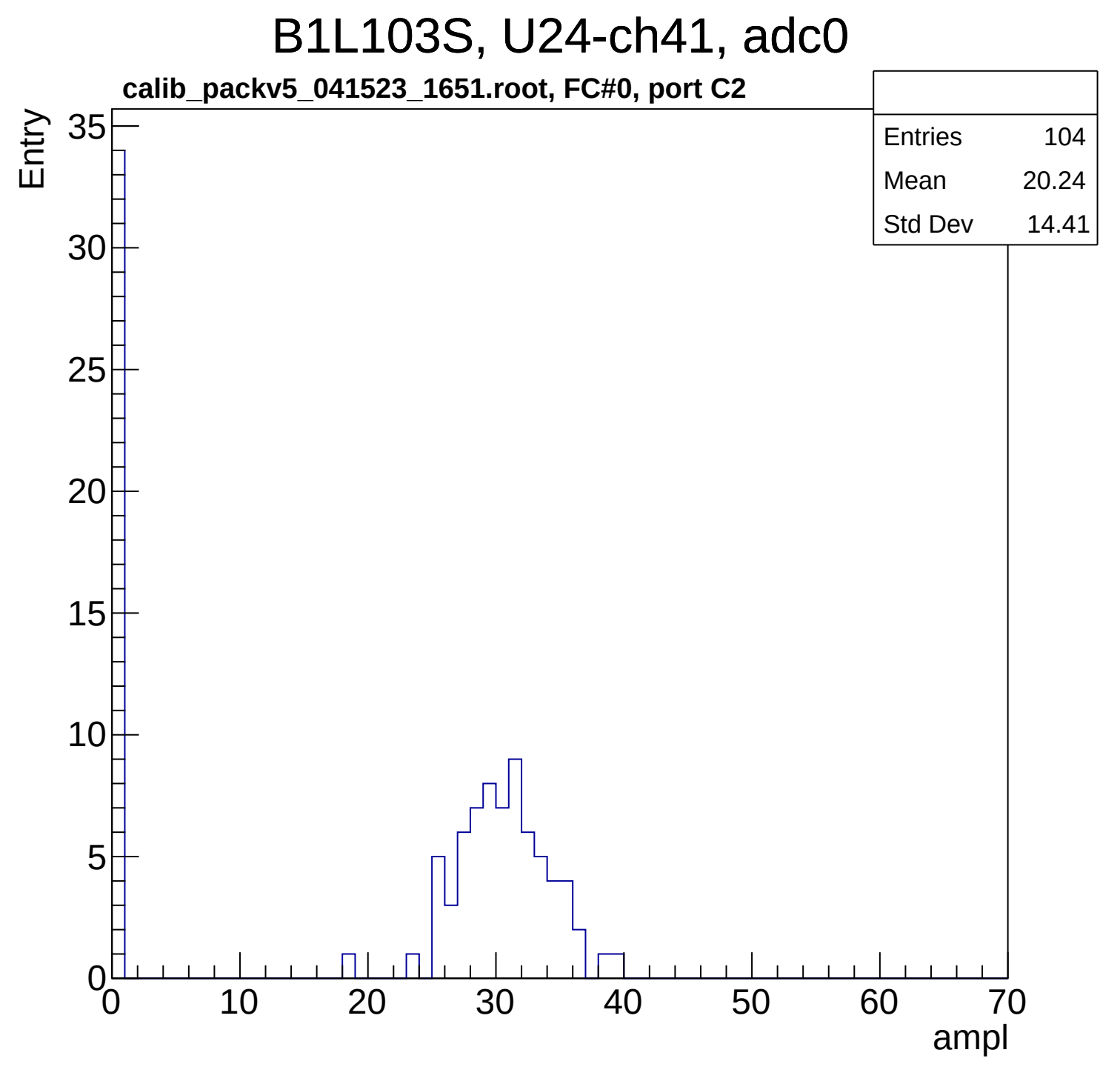
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U24-ch40, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch41, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 104
Mean 20.24
Std Dev 14.41
Entry
ampl
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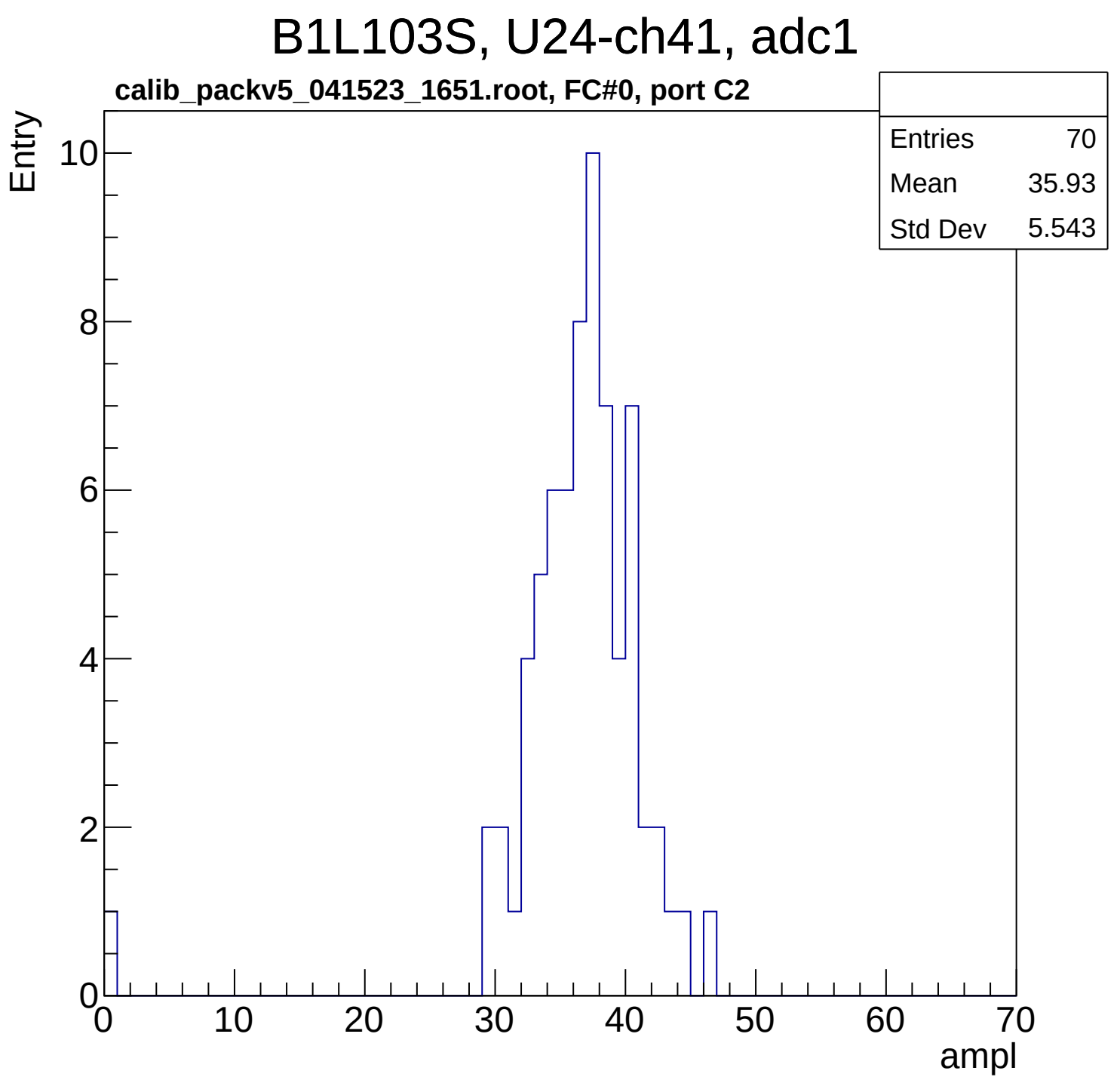
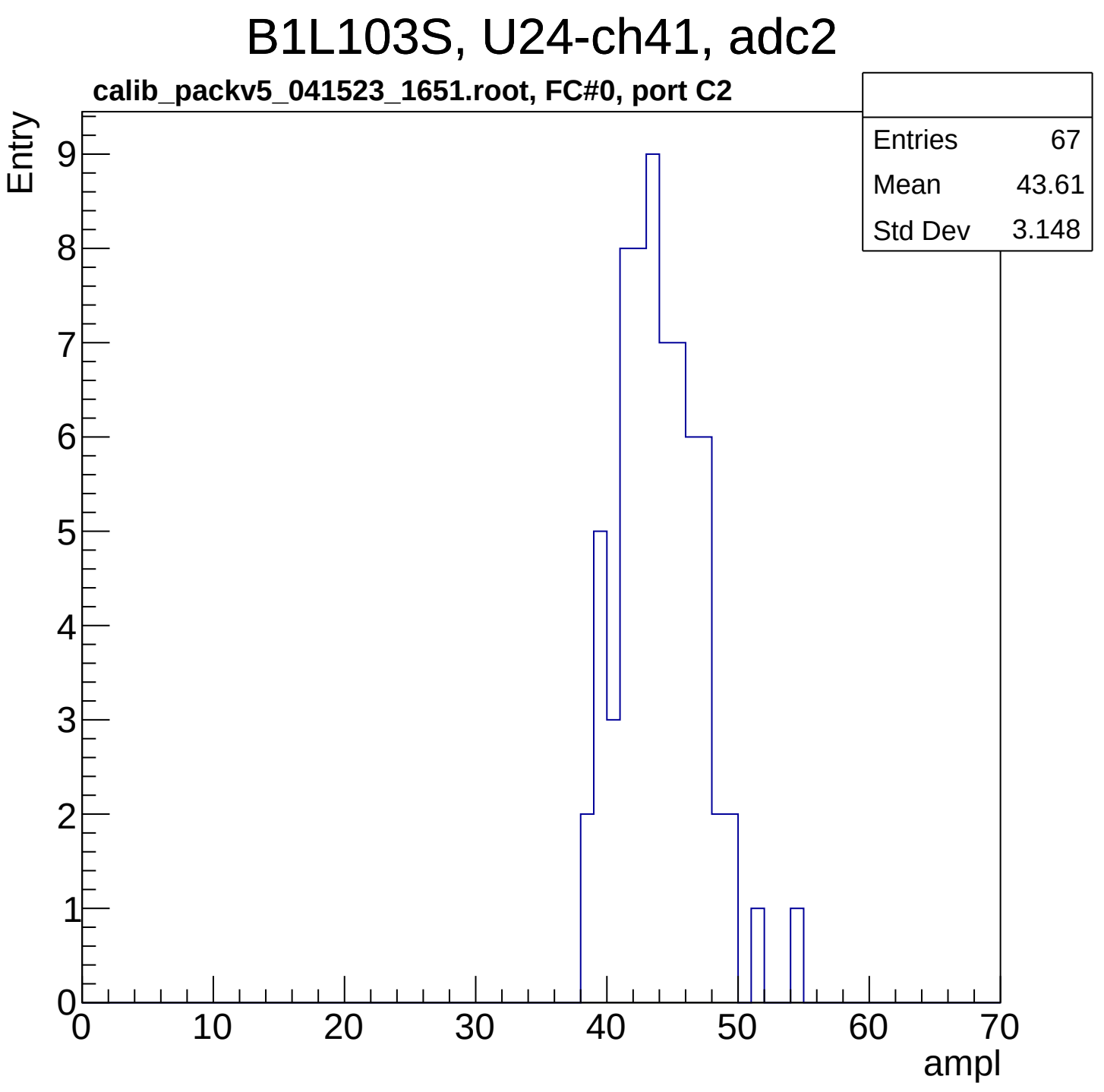
5
10
15
20
25
30
35
0
10
20
30
40
50
60
70


B1L103S, U24-ch41, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 35.93
Std Dev 5.543
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch41, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 43.61
Std Dev 3.148
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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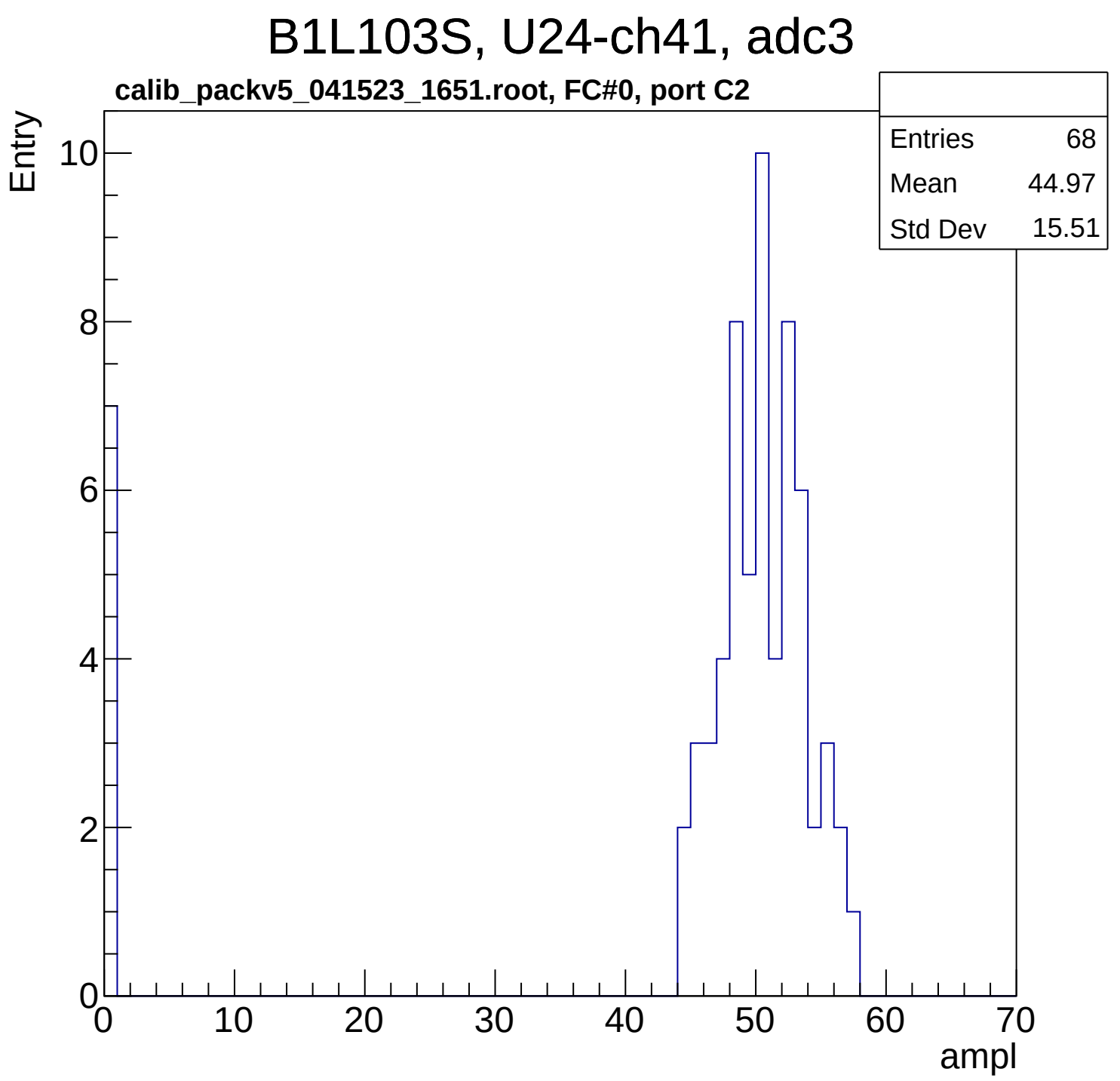
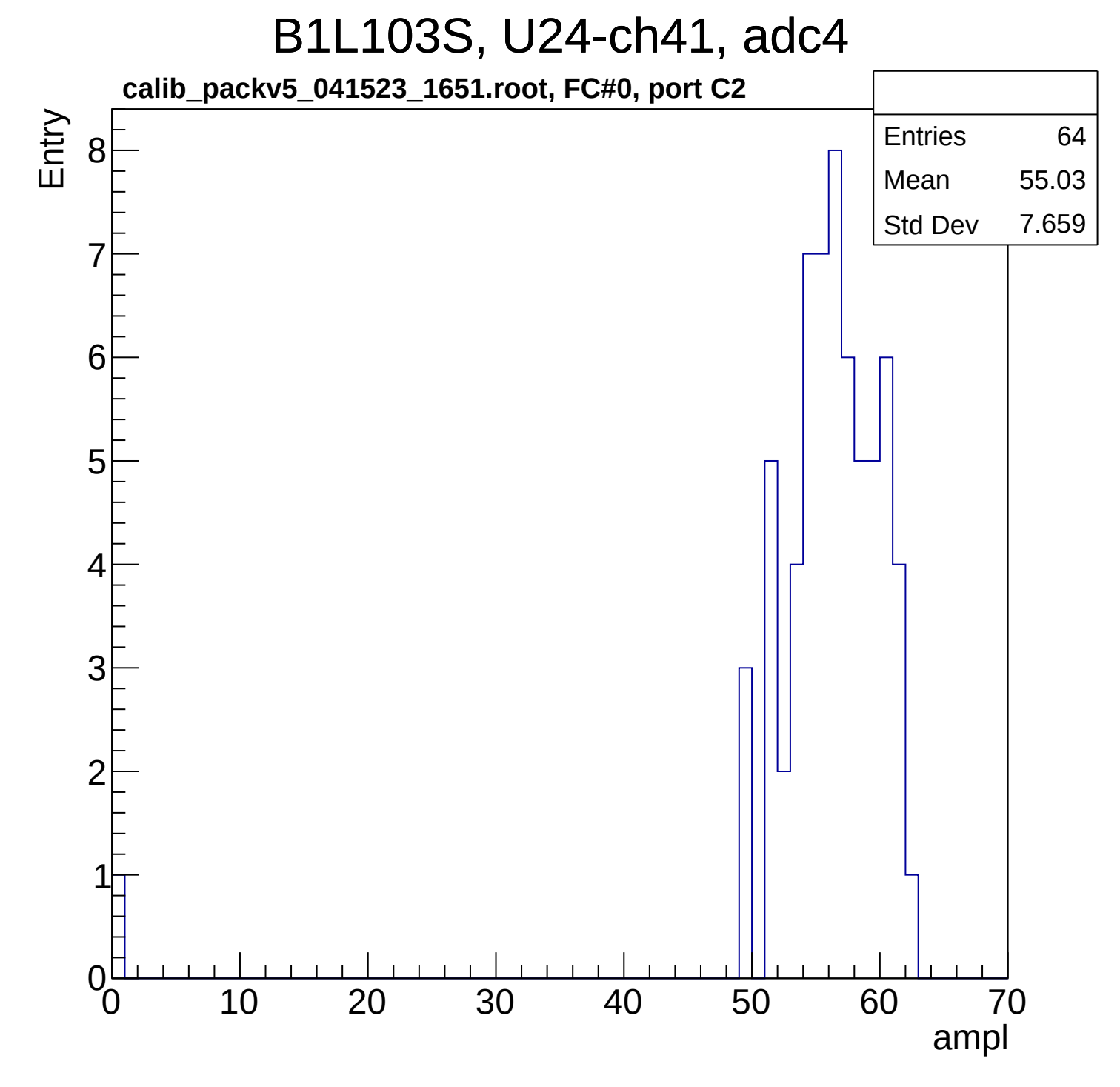

B1L103S, U24-ch41, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 44.97
Std Dev 15.51
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U24-ch41, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 55.03
Std Dev 7.659
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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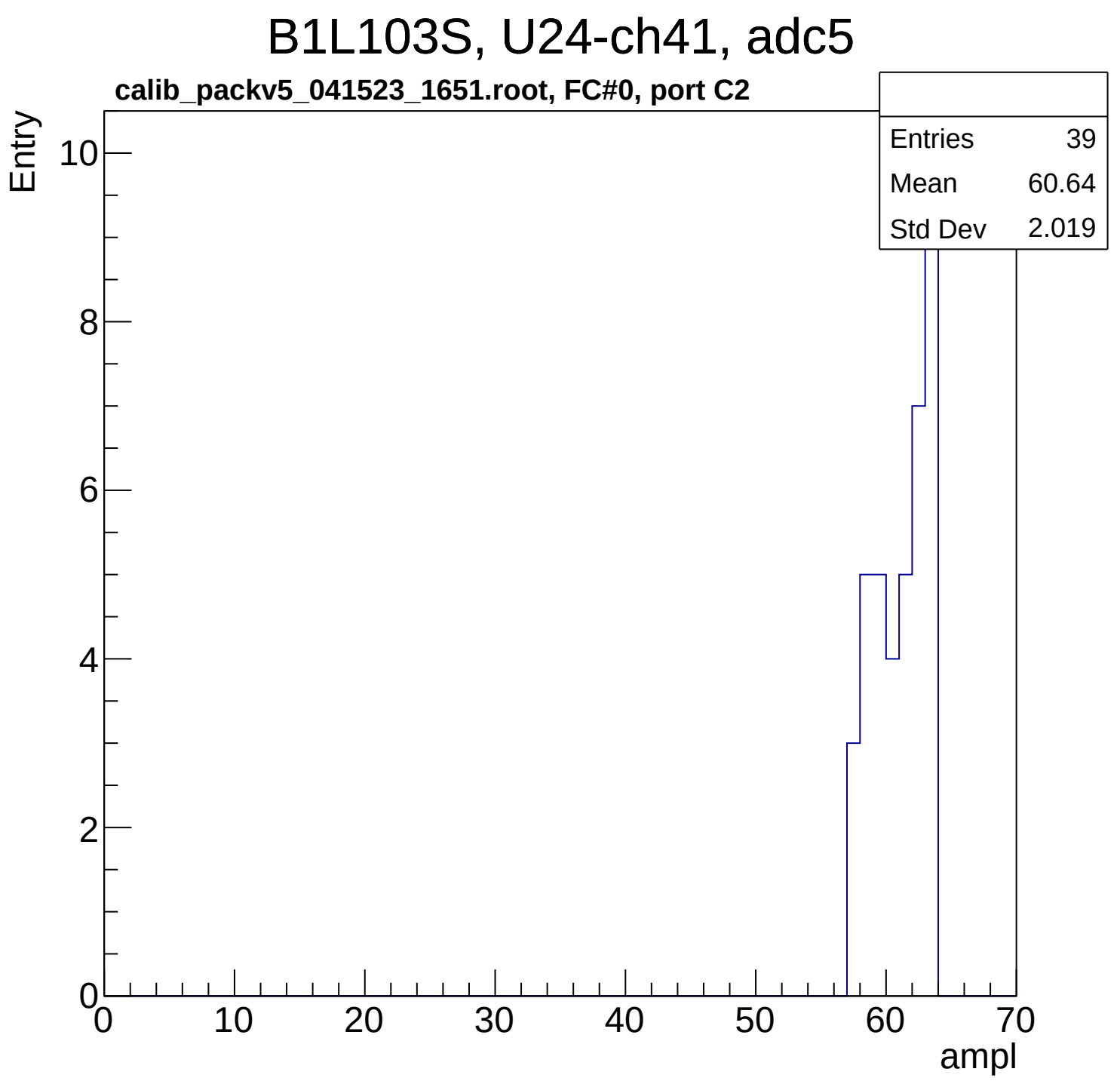
40
50
60
70


B1L103S, U24-ch41, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 39
Mean 60.64
Std Dev 2.019
Entry
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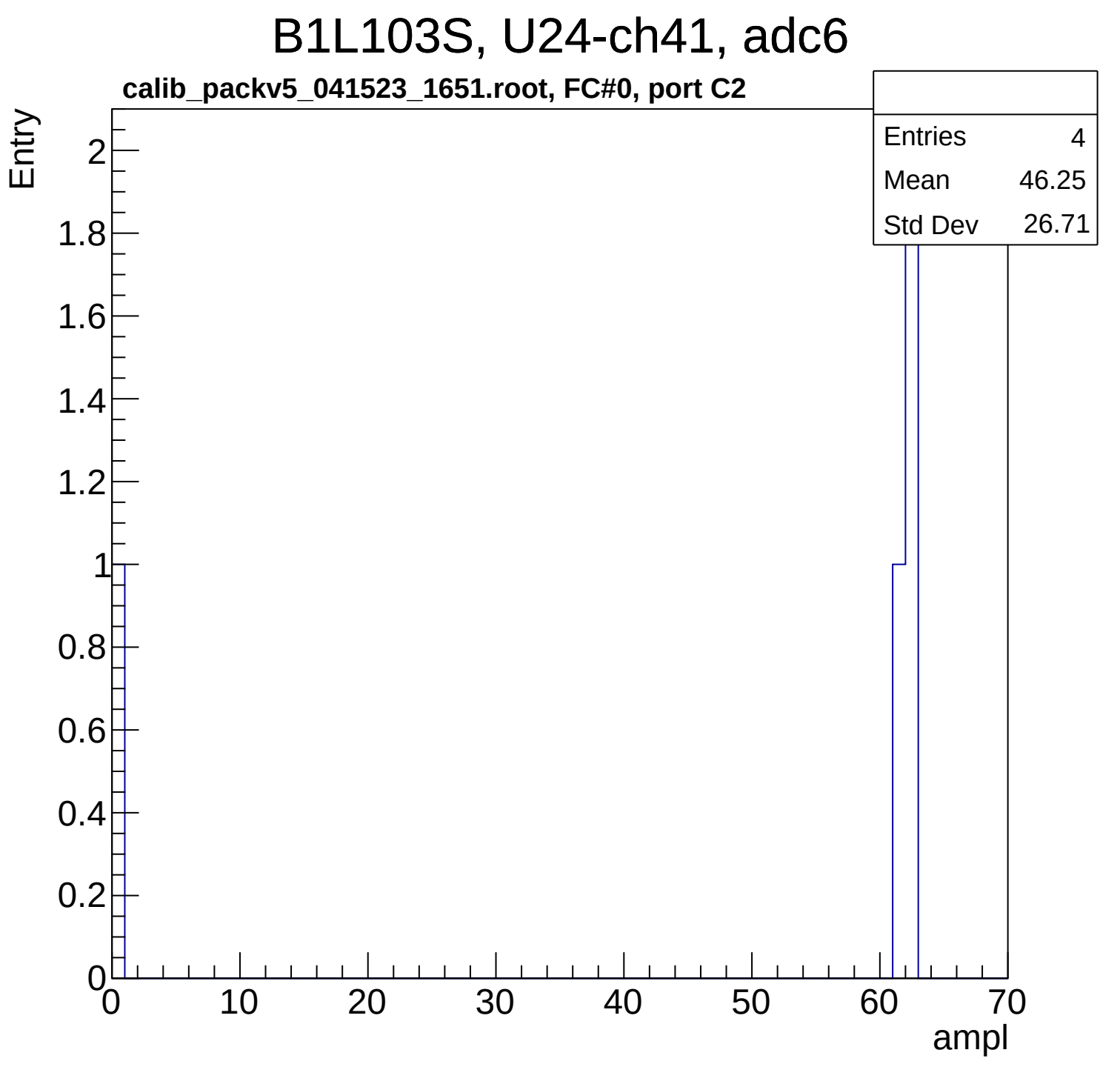
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch41, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 4
Mean 46.25
Std Dev 26.71
Entry
ampl
0
0.2
0.4
0.6
0.8
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1.2
1.4
1.6
1.8
2
0
10
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60
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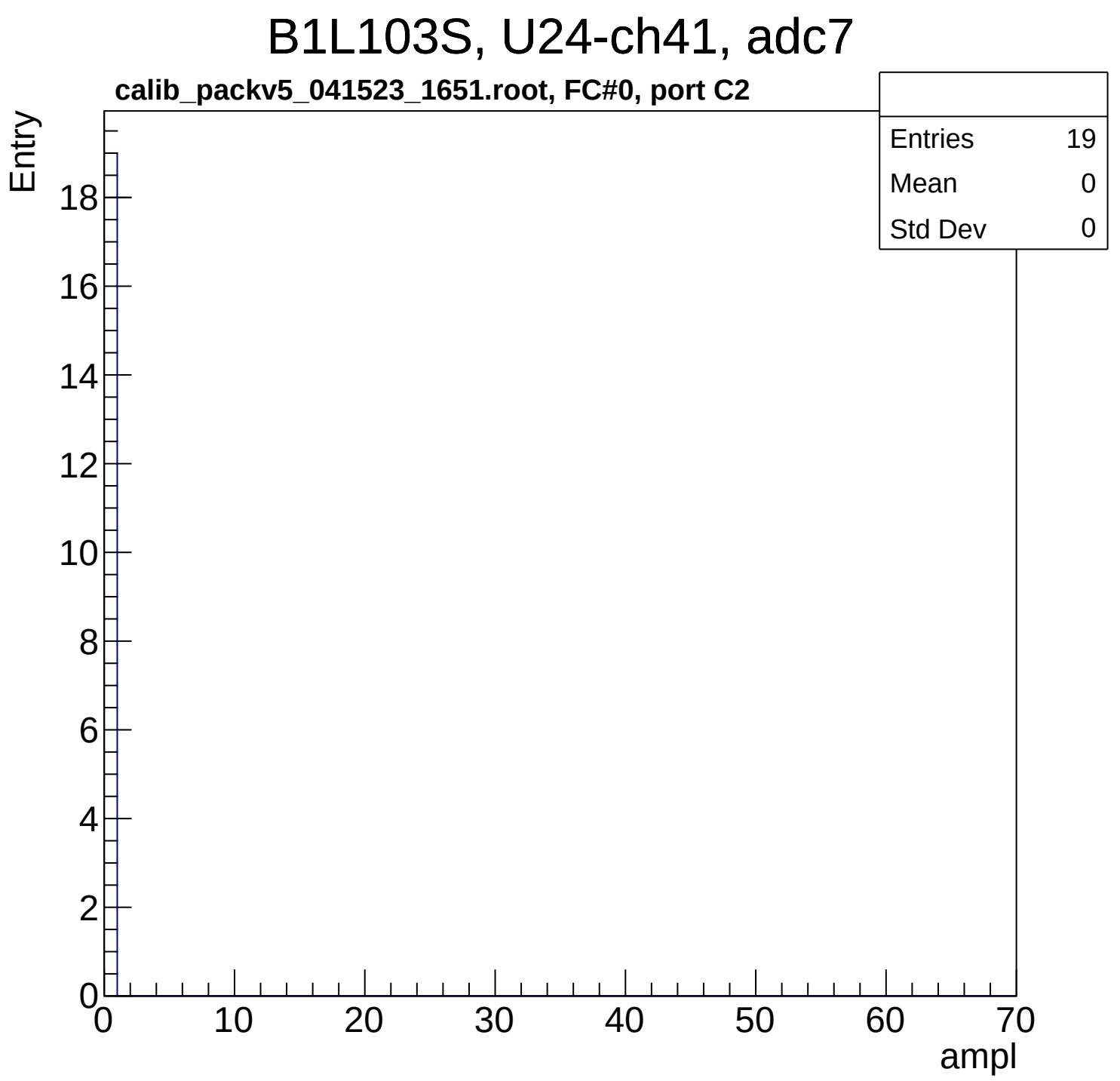
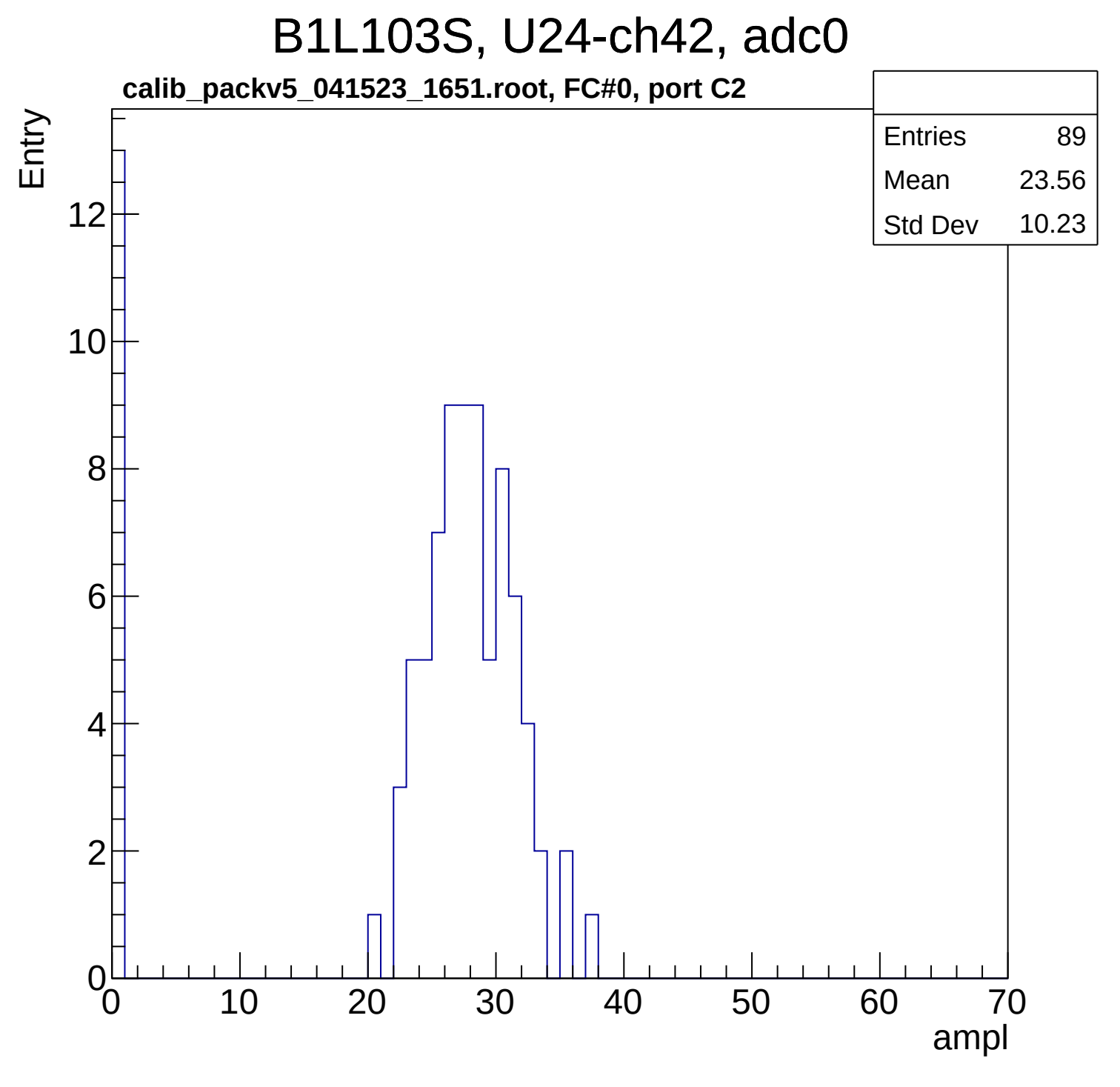
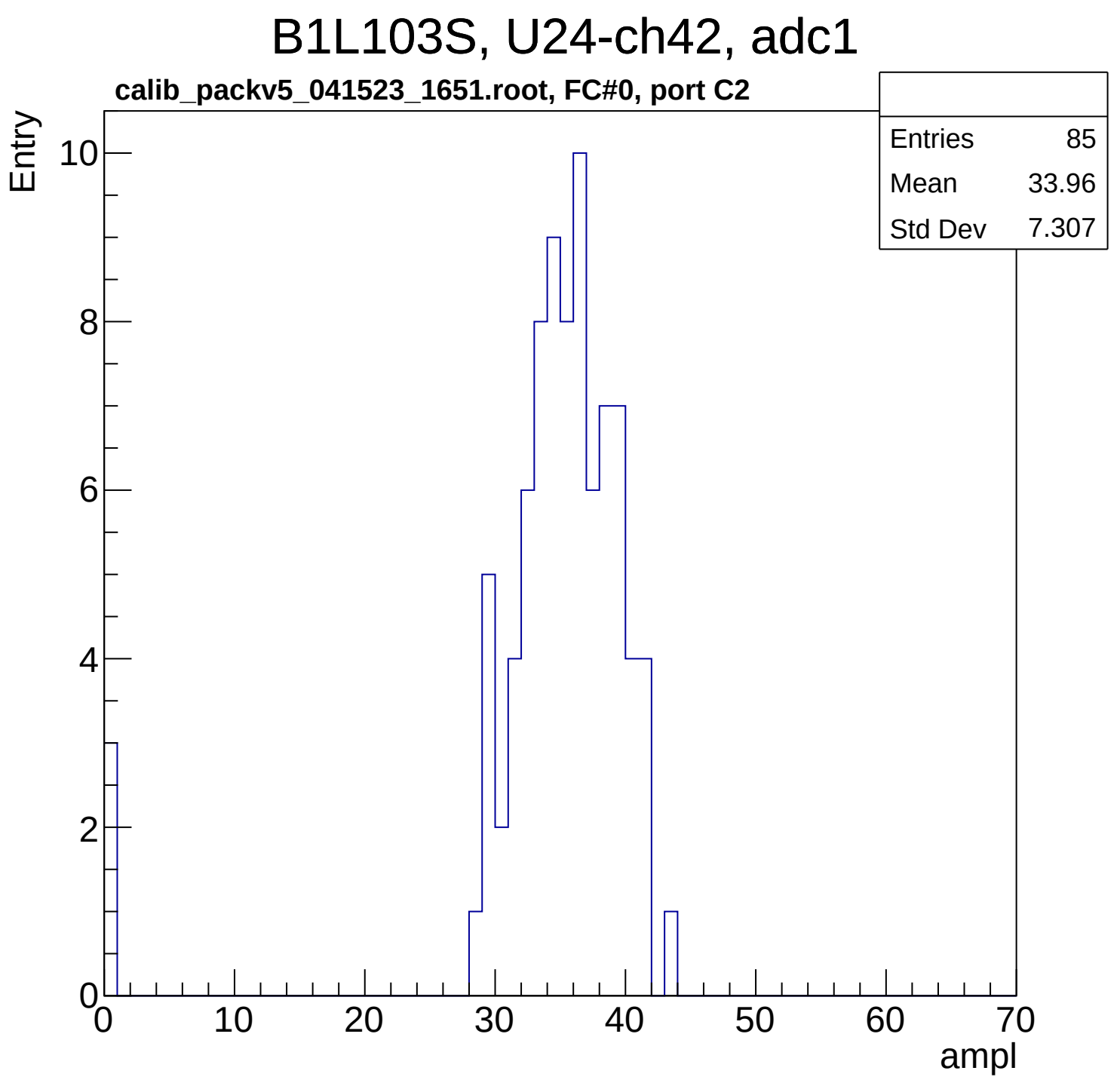
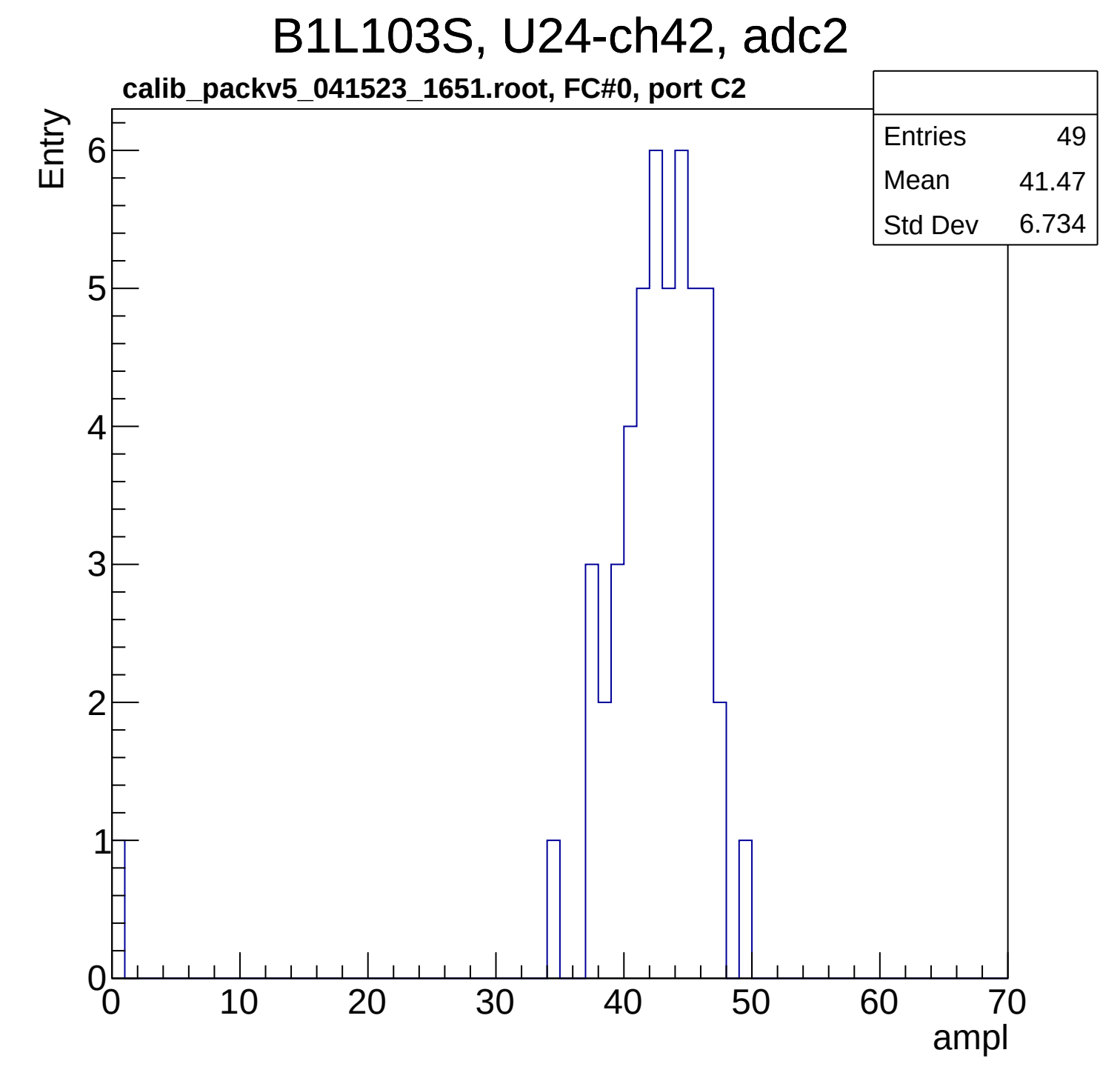

B1L103S, U24-ch41, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch42, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 89
Mean 23.56
Std Dev 10.23
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch42, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 33.96
Std Dev 7.307
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U24-ch42, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 41.47
Std Dev 6.734
Entry
ampl
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1
2
3
4
5
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0
10
20
30
40
50
60
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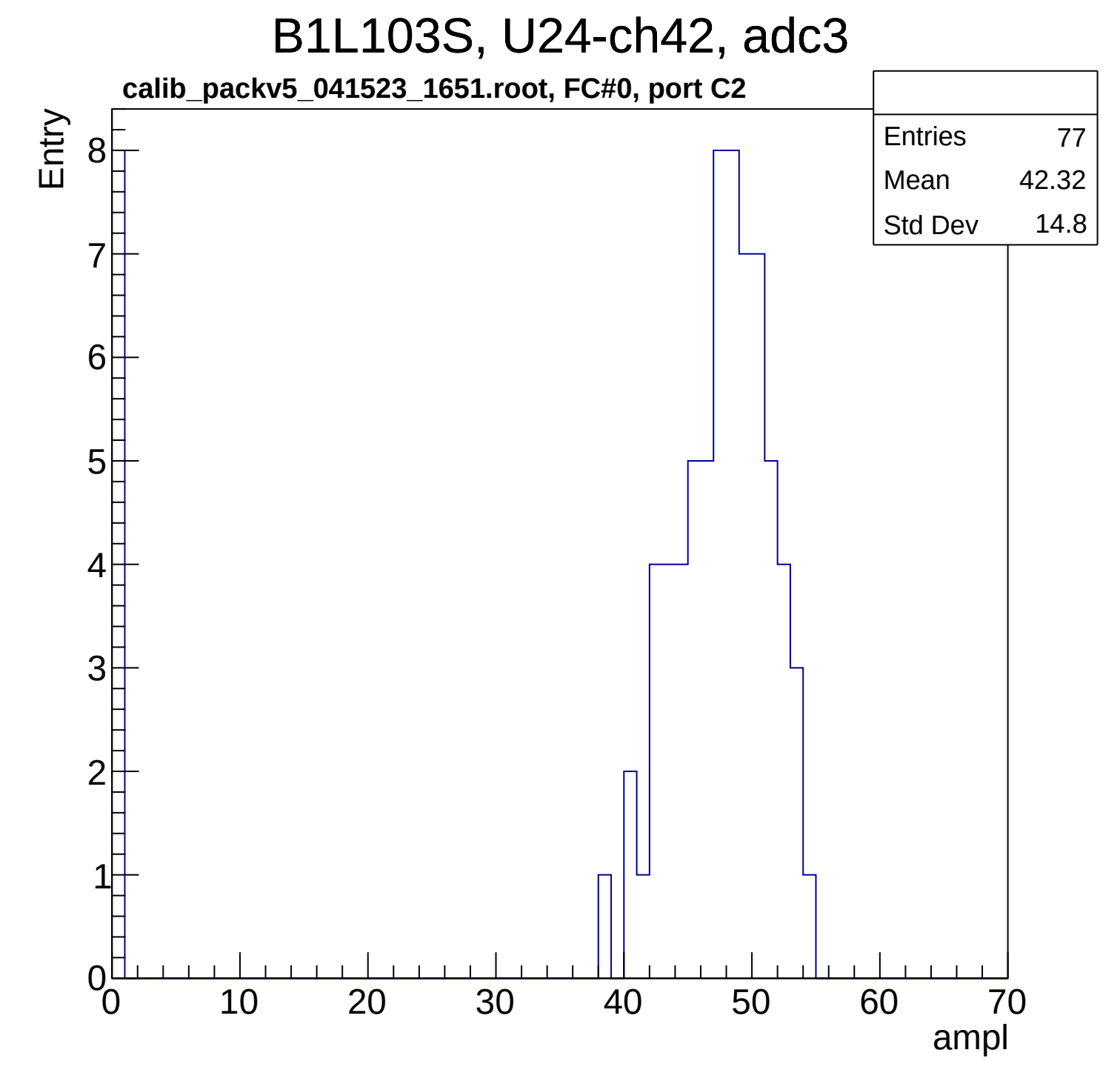
B1L103S, U24-ch42, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 42.32
Std Dev 14.8
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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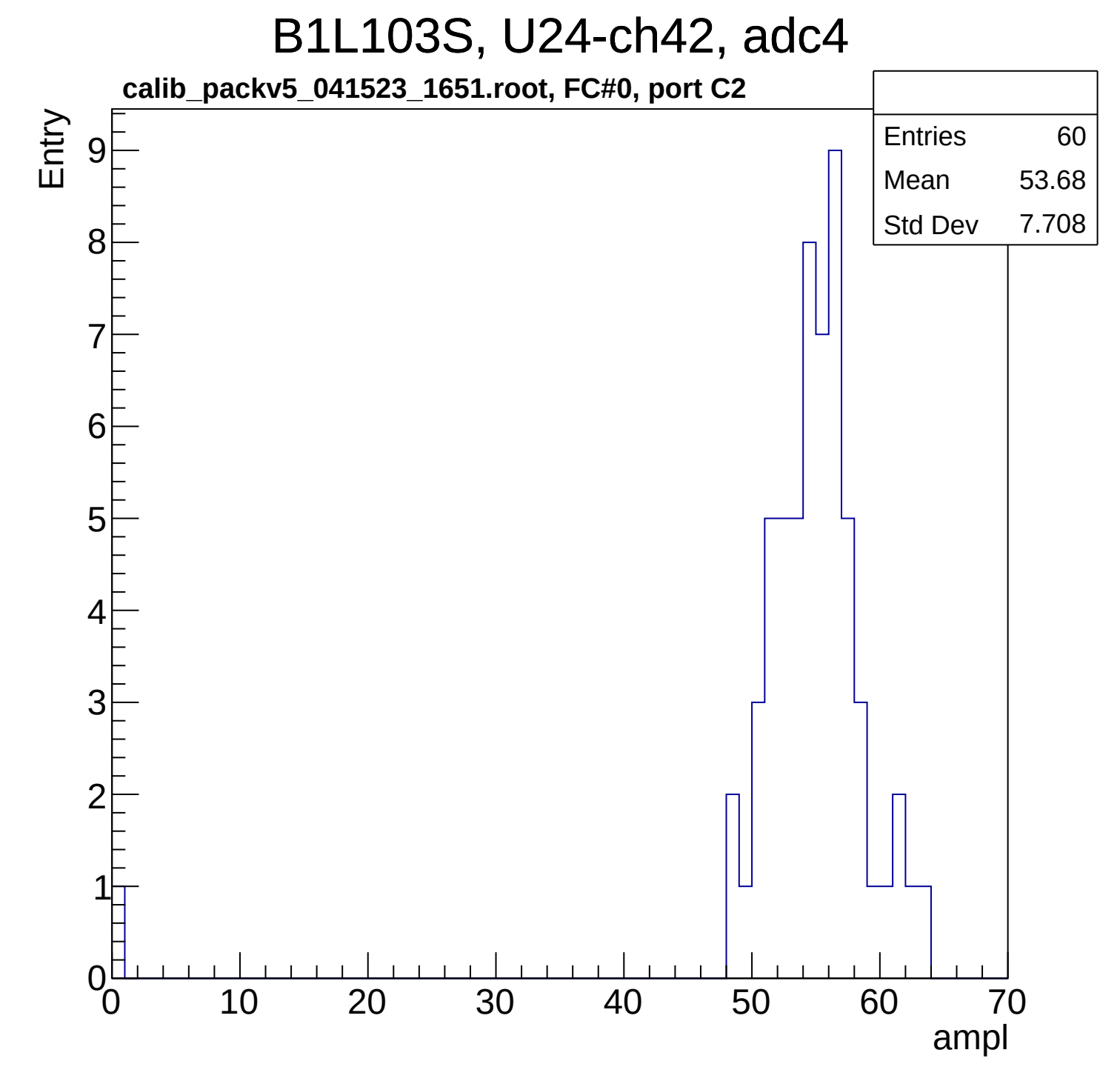
B1L103S, U24-ch42, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 53.68
Std Dev 7.708
Entry
ampl
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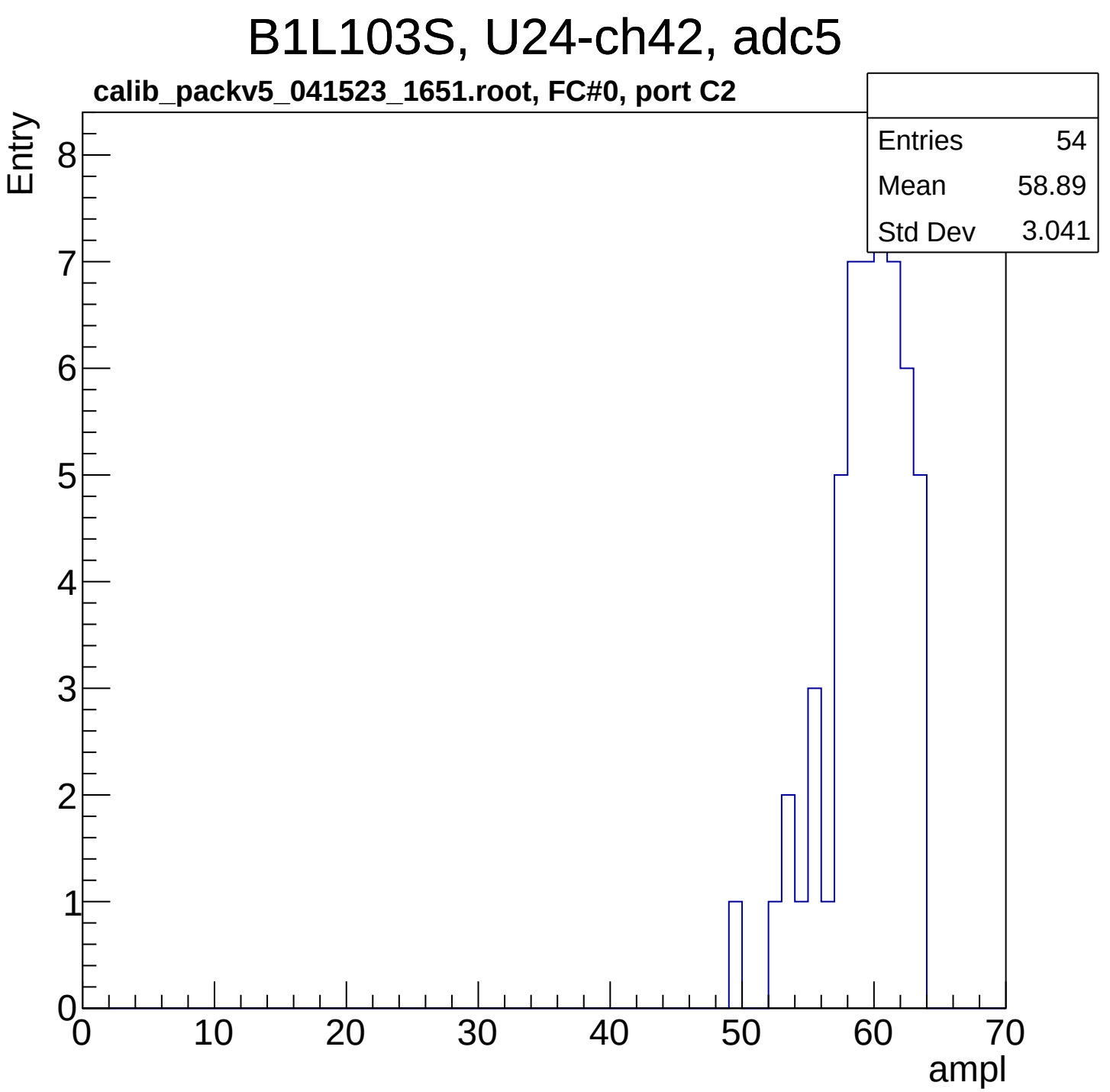
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U24-ch42, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 58.89
Std Dev 3.041
Entry
ampl
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2
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7
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0
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60
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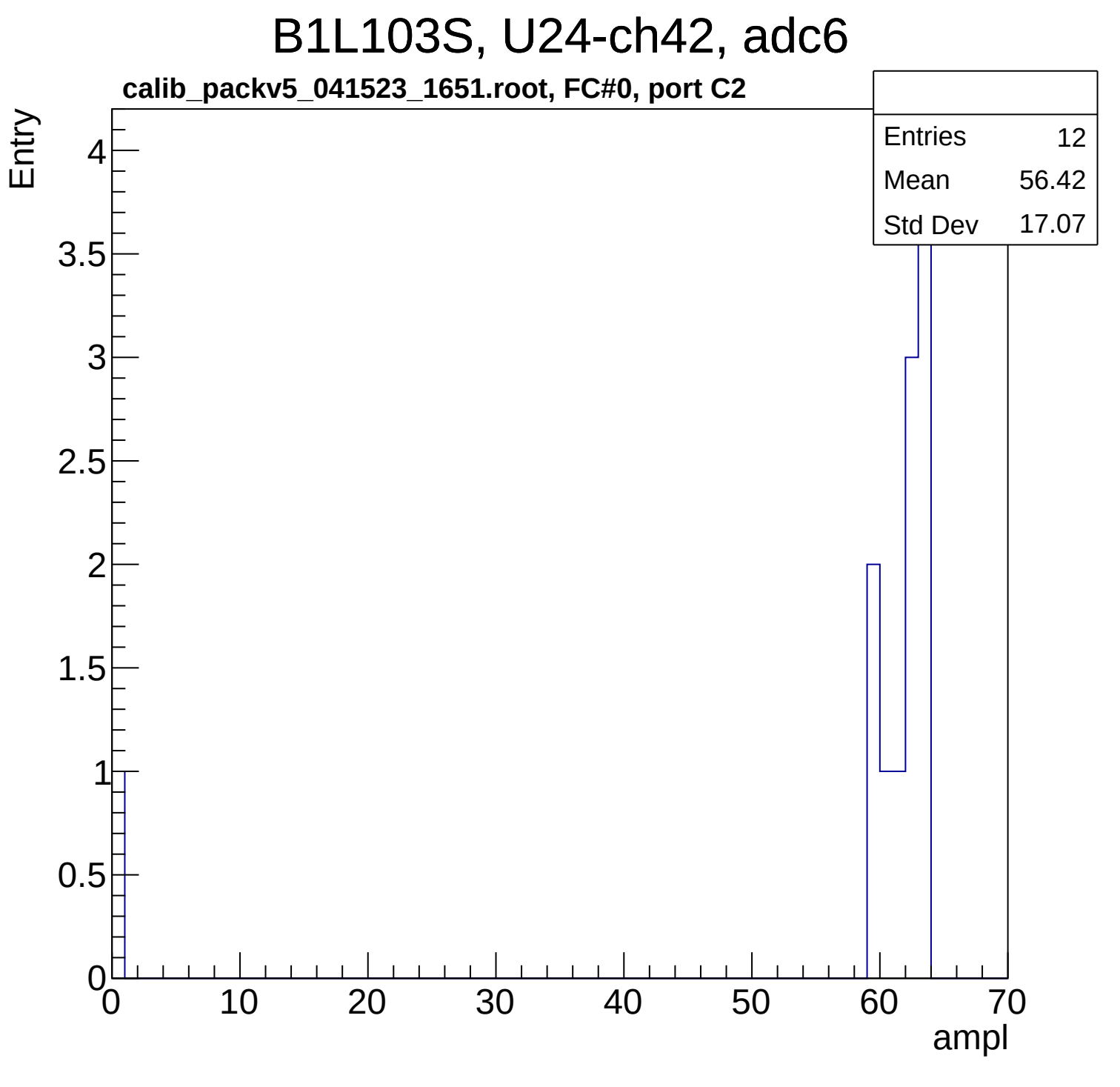
B1L103S, U24-ch42, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 56.42
Std Dev 17.07
Entry
ampl
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1.5
2
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3
3.5
4
0
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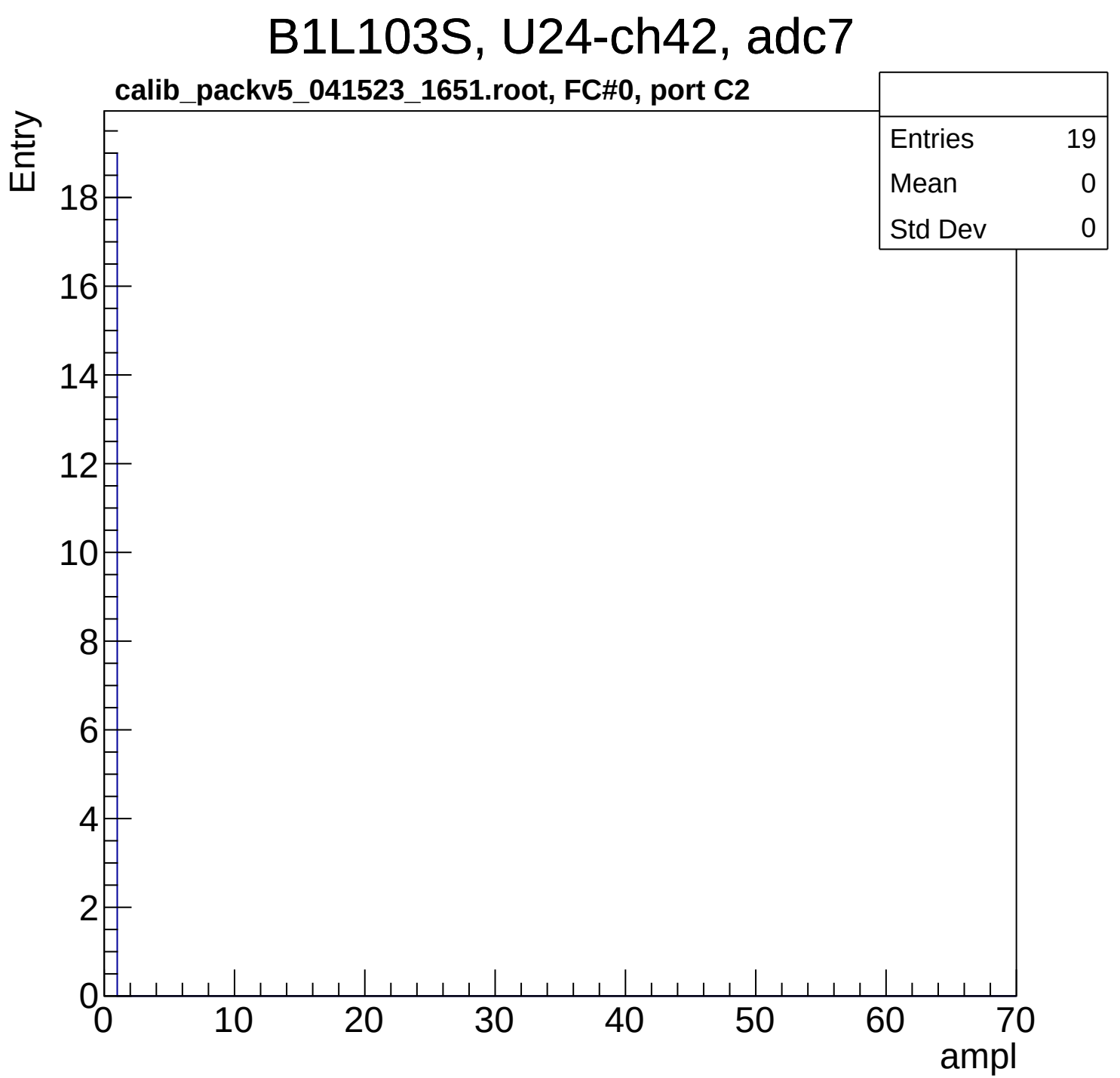
B1L103S, U24-ch42, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
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6
8
10
12
14
16
18
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50
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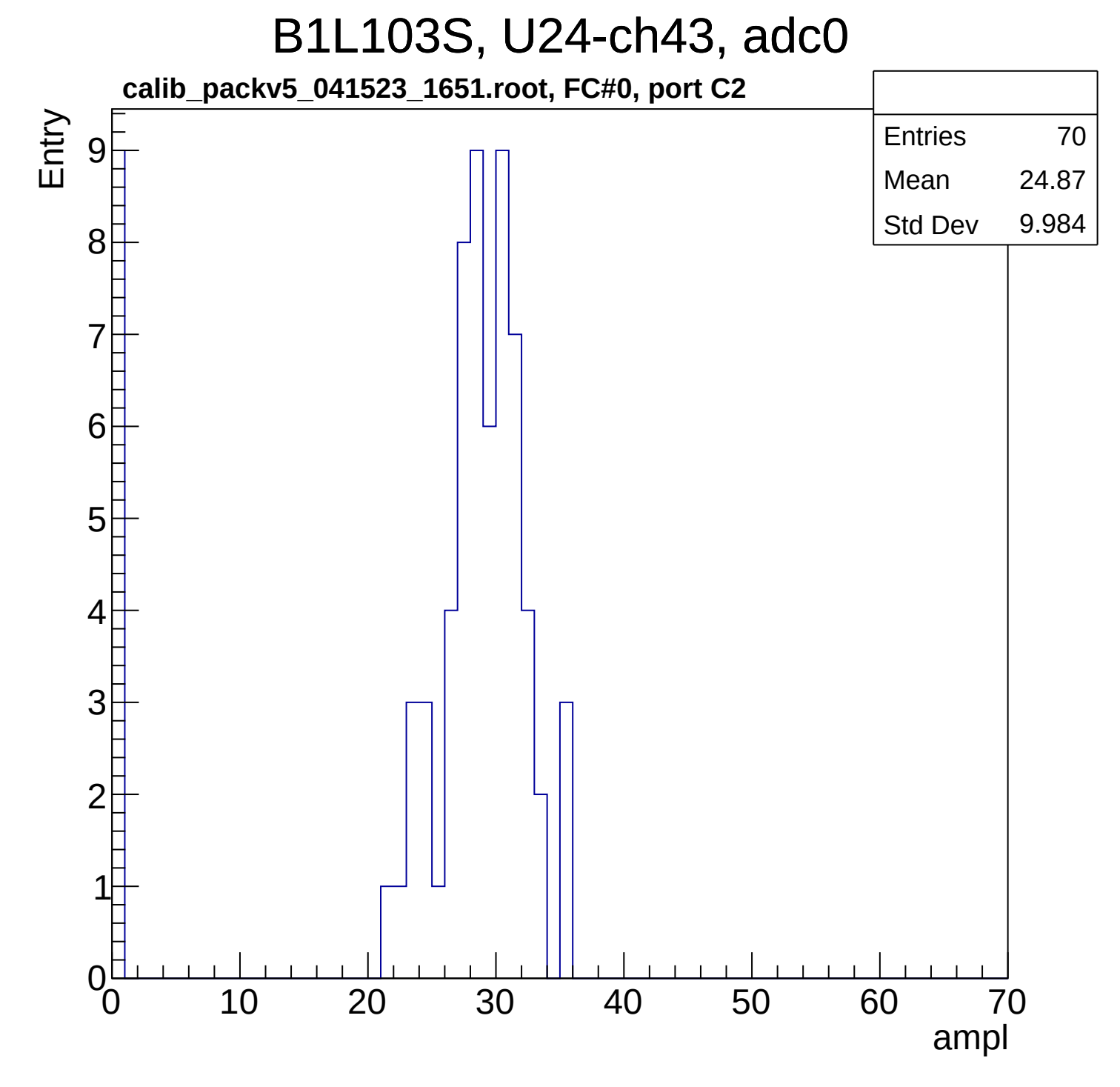
70
ampl


B1L103S, U24-ch43, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 24.87
Std Dev 9.984
Entry
ampl
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0
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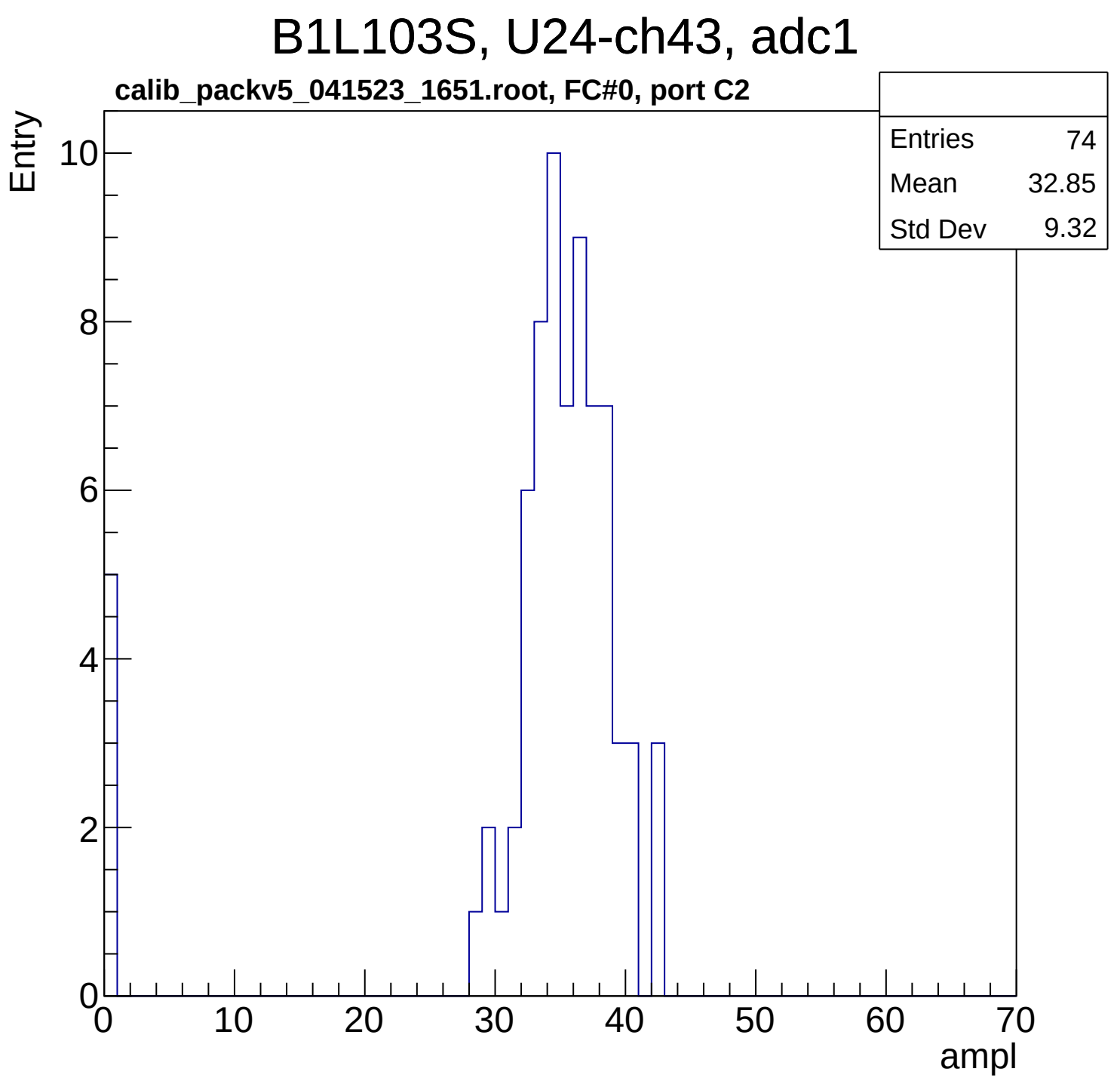
B1L103S, U24-ch43, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 32.85
Std Dev 9.32
Entry
ampl
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60
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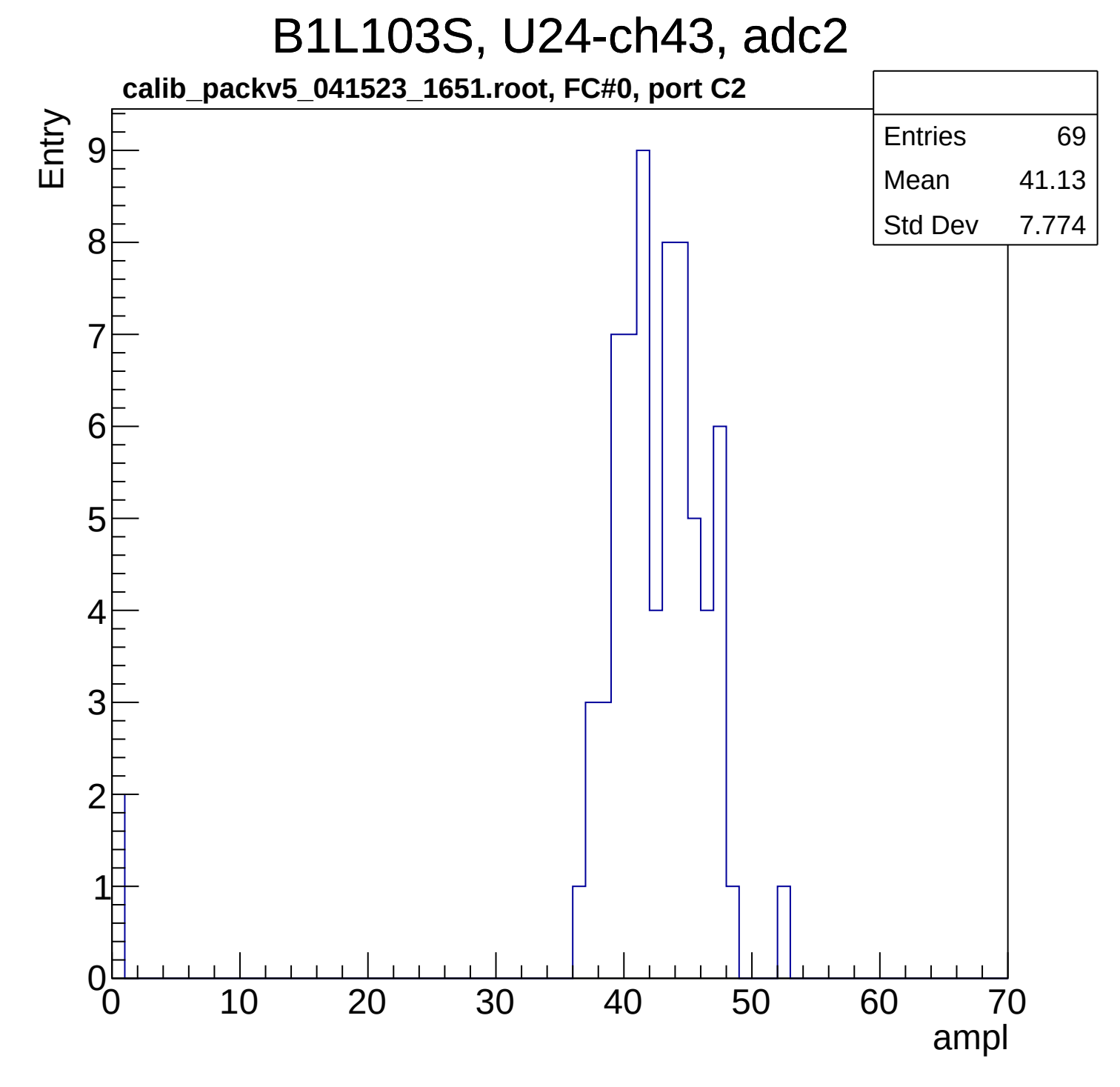
B1L103S, U24-ch43, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 41.13
Std Dev 7.774
Entry
ampl
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8
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0
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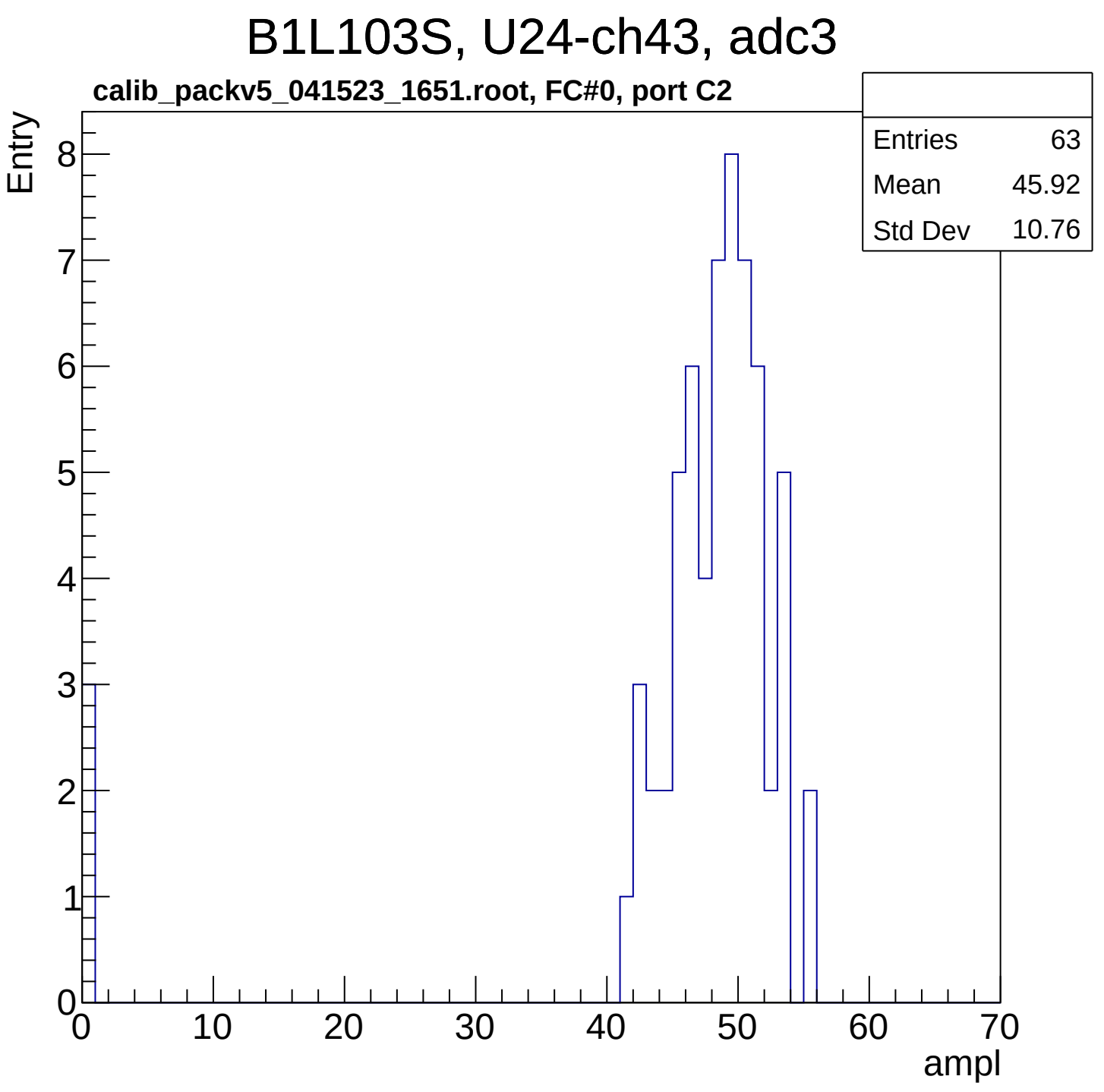
B1L103S, U24-ch43, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 45.92
Std Dev 10.76
Entry
ampl
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40
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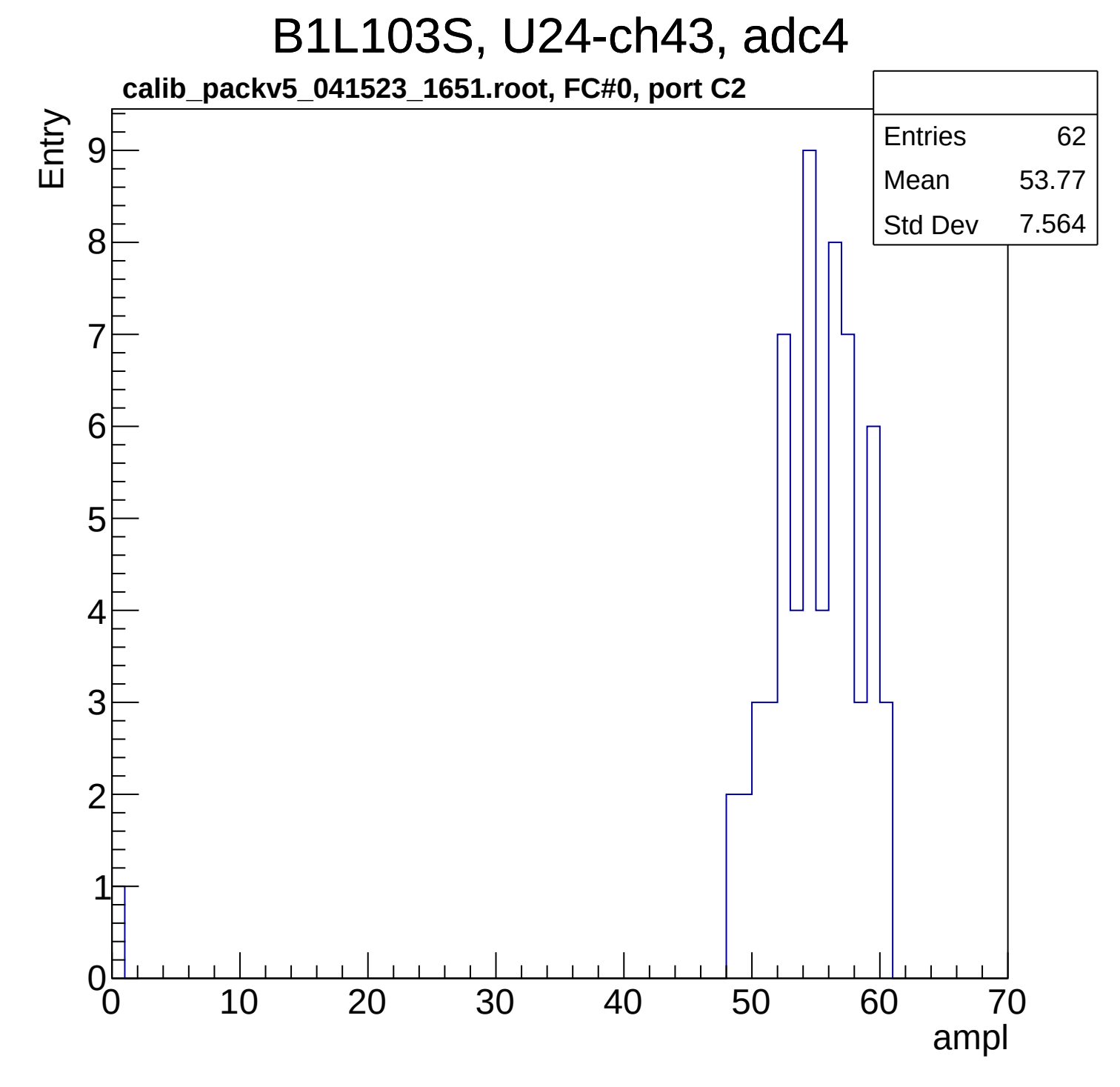
B1L103S, U24-ch43, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 53.77
Std Dev 7.564
Entry
ampl
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2
3
4
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6
7
8
9
0
10
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50
60
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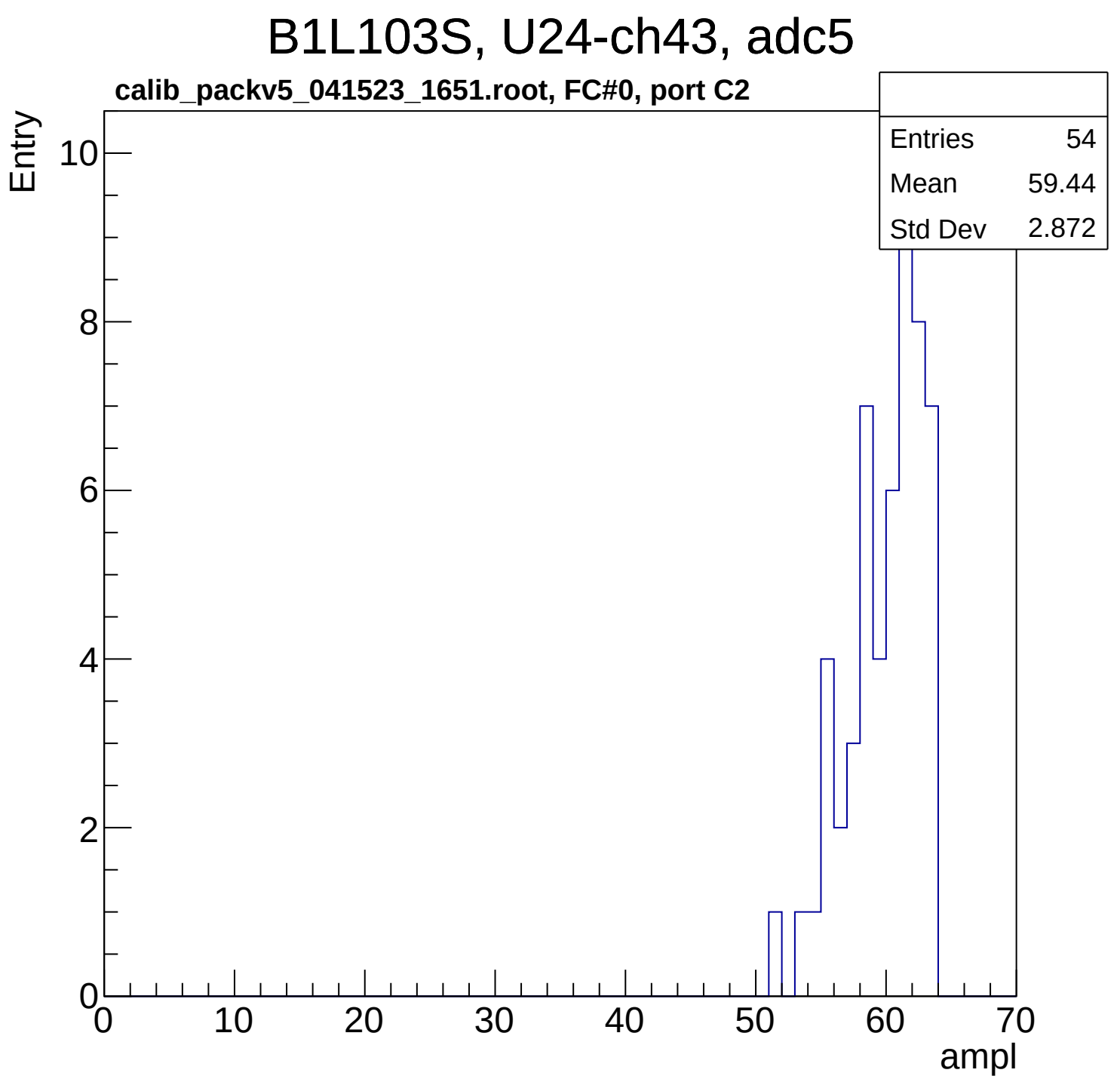
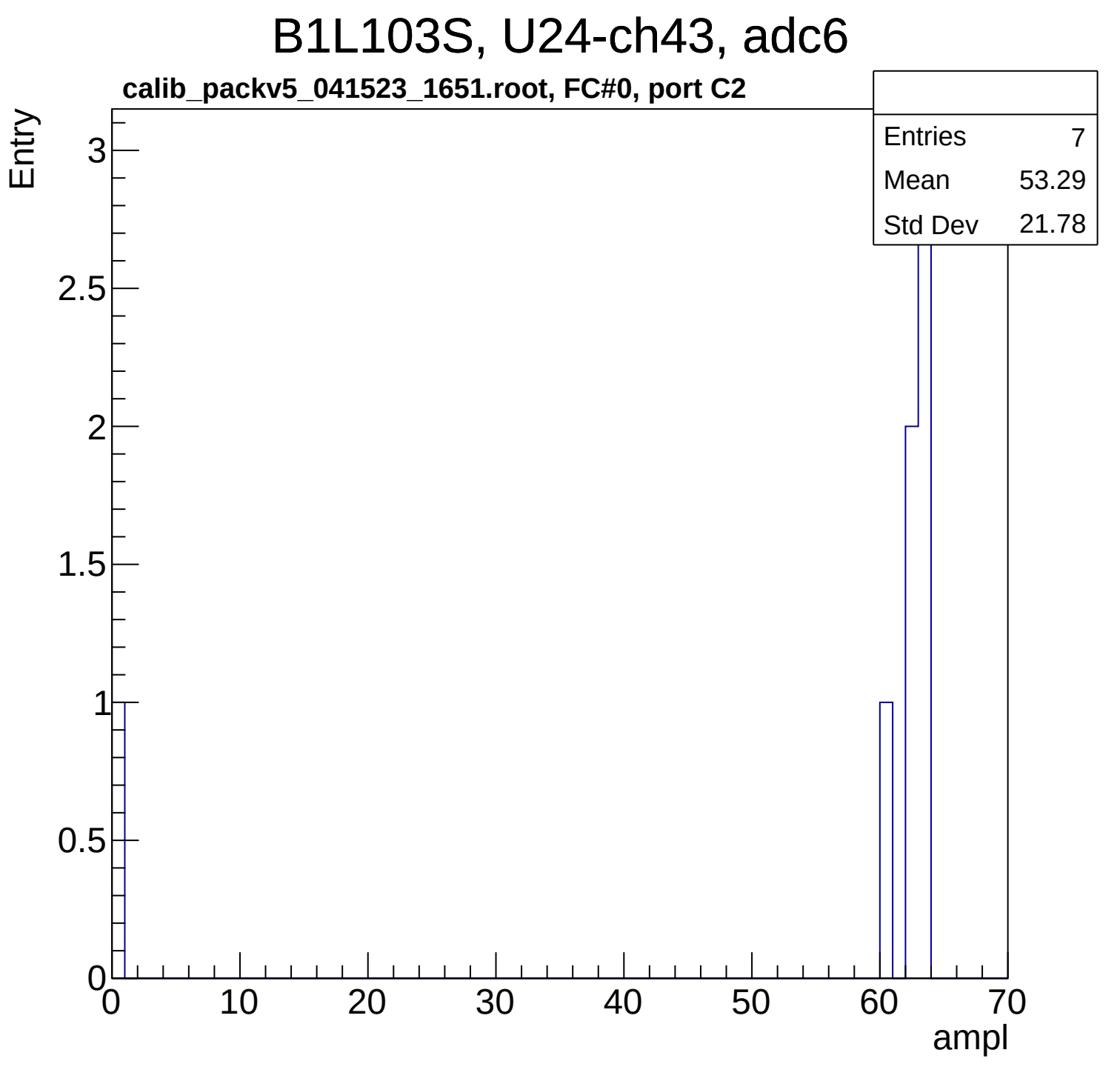

B1L103S, U24-ch43, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 59.44
Std Dev 2.872
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch43, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 53.29
Std Dev 21.78
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
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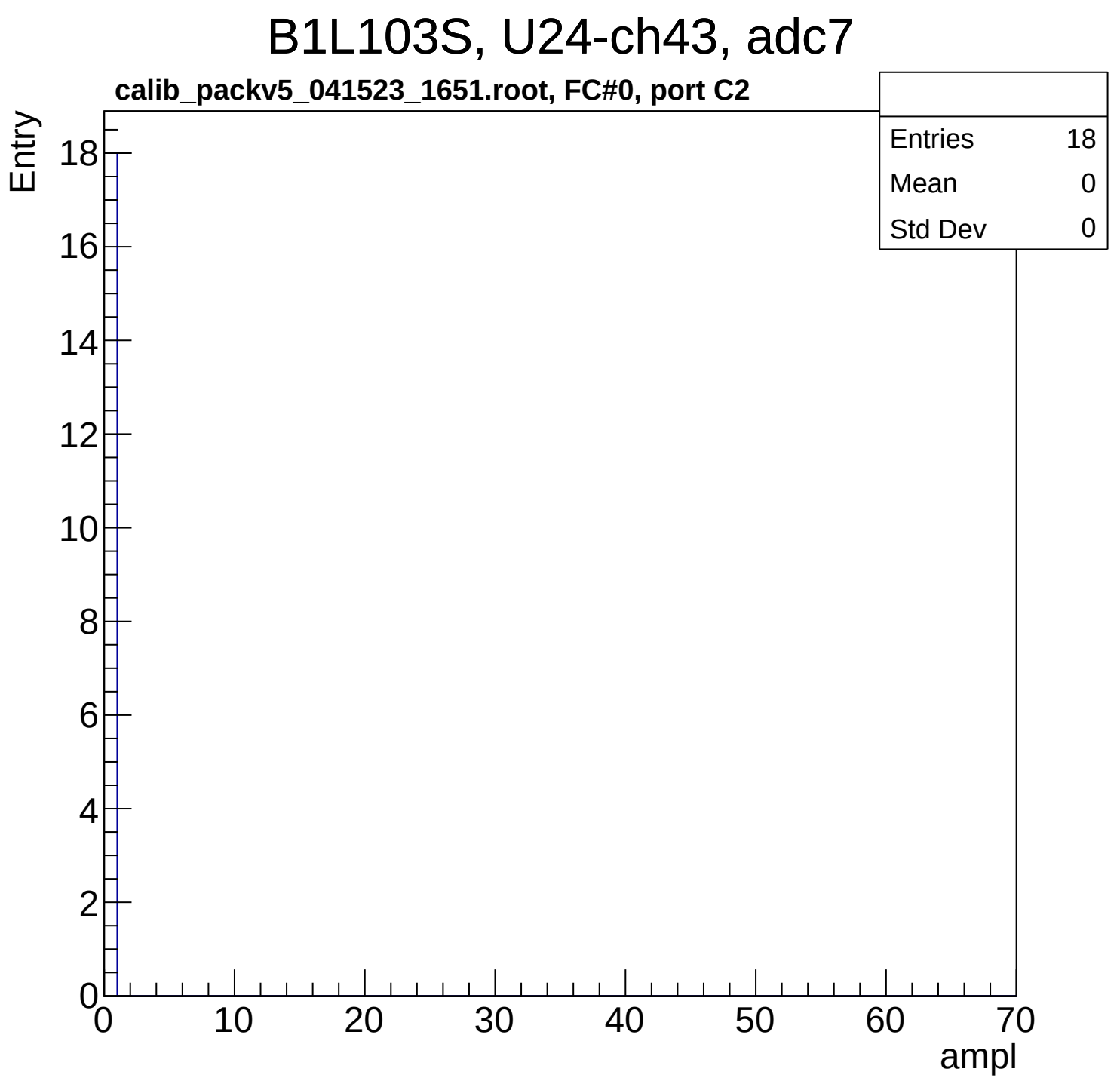
B1L103S, U24-ch43, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
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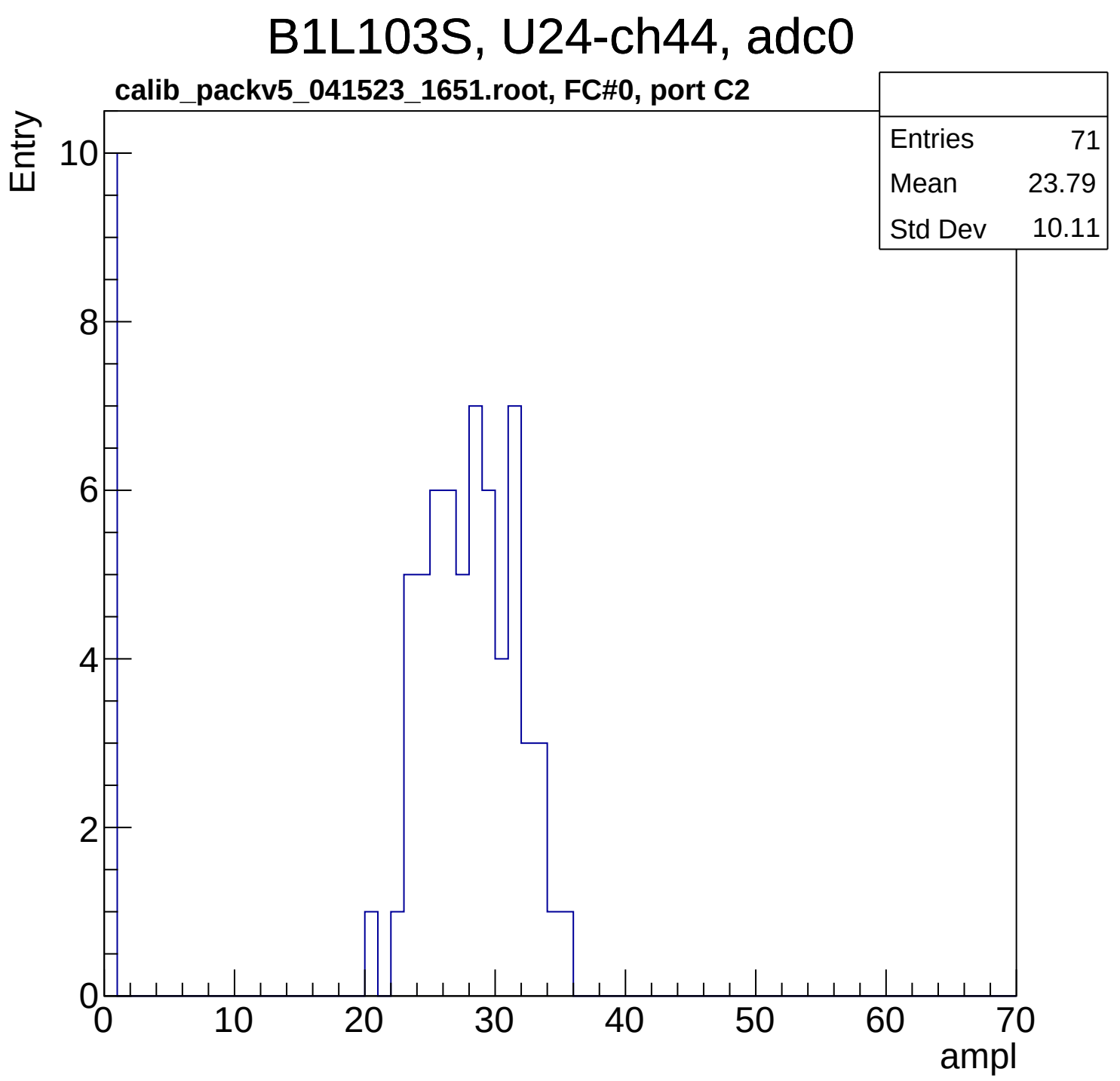
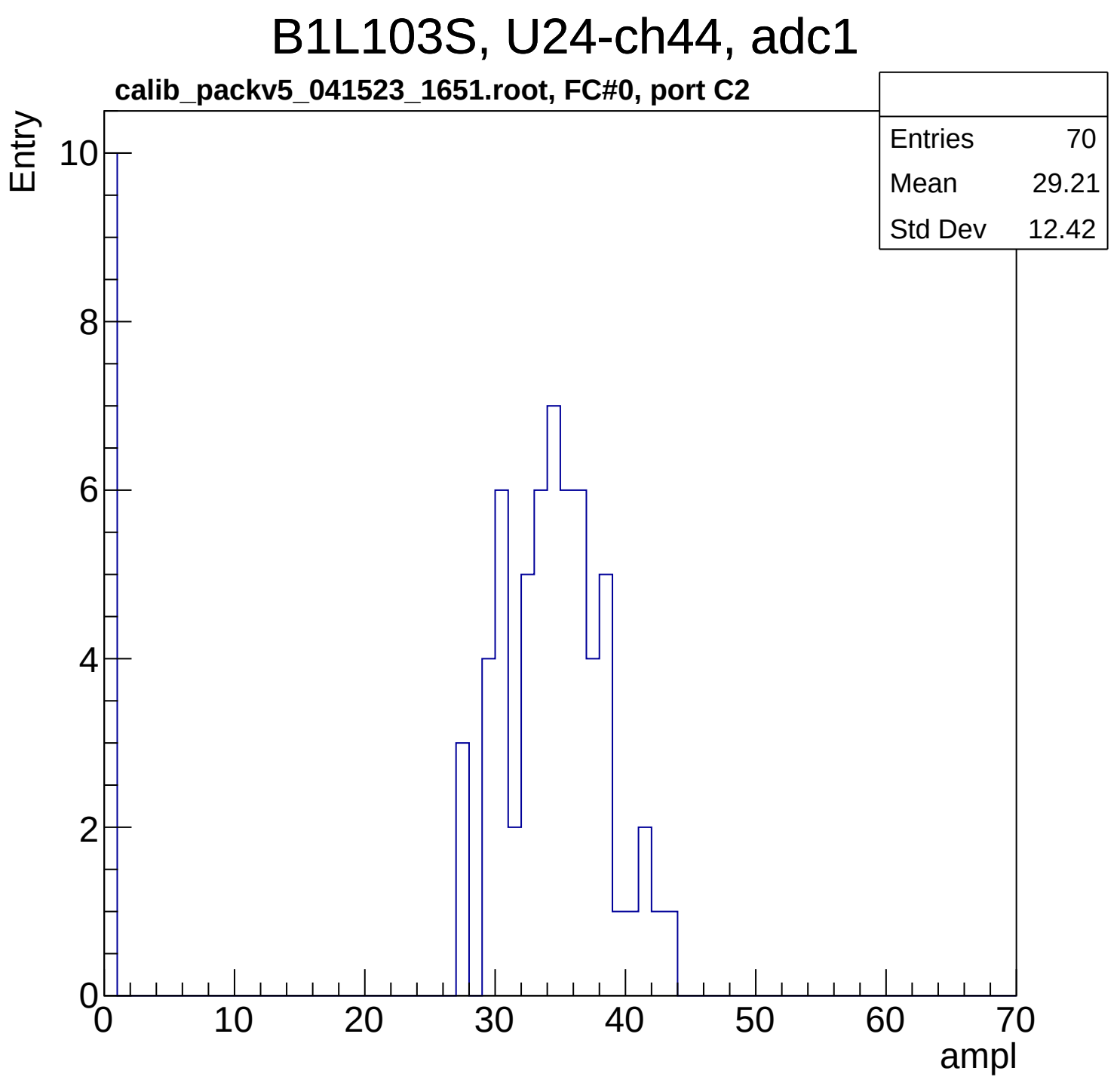
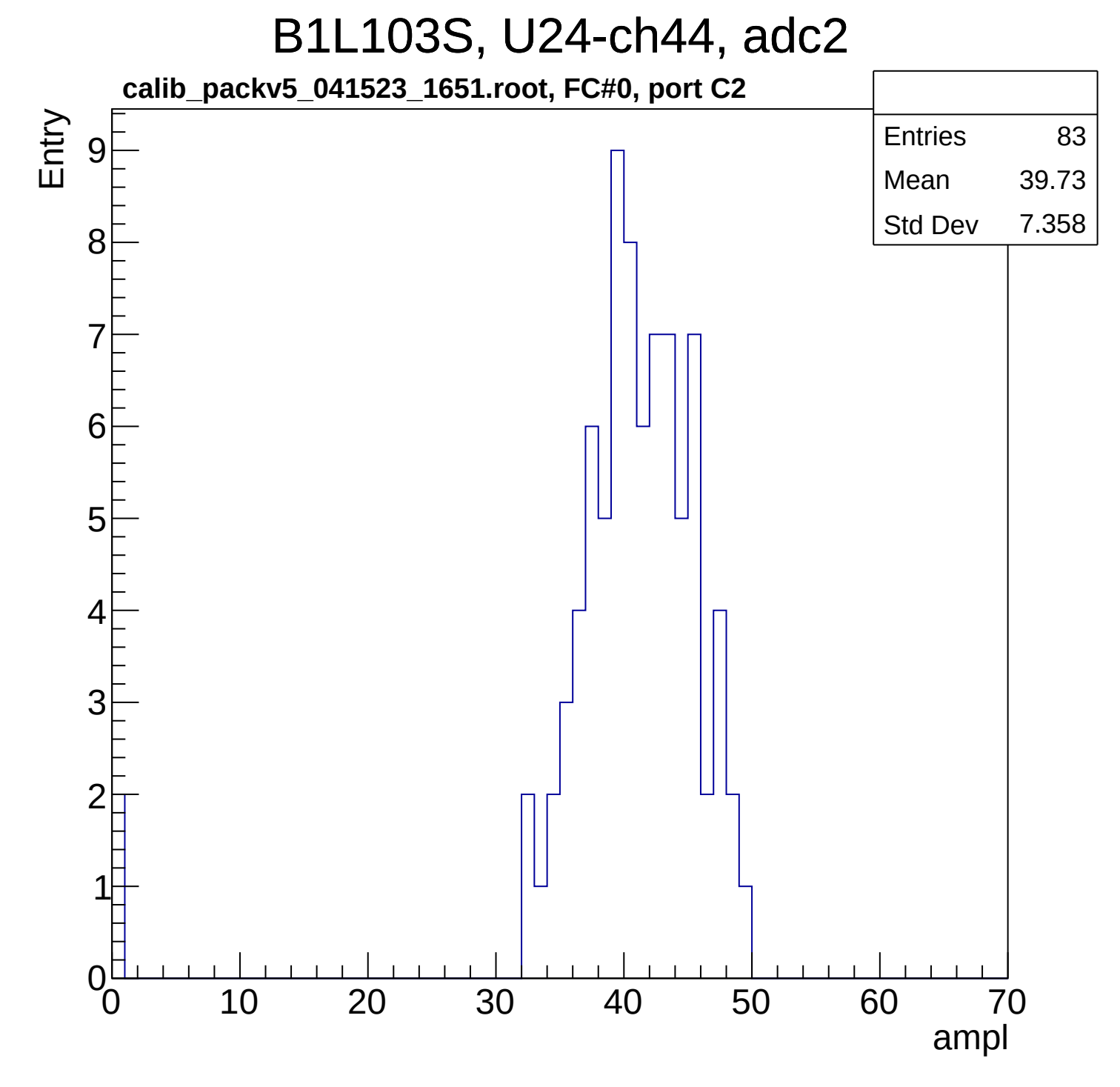
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch44, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 23.79
Std Dev 10.11
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch44, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 29.21
Std Dev 12.42
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch44, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 39.73
Std Dev 7.358
Entry
ampl
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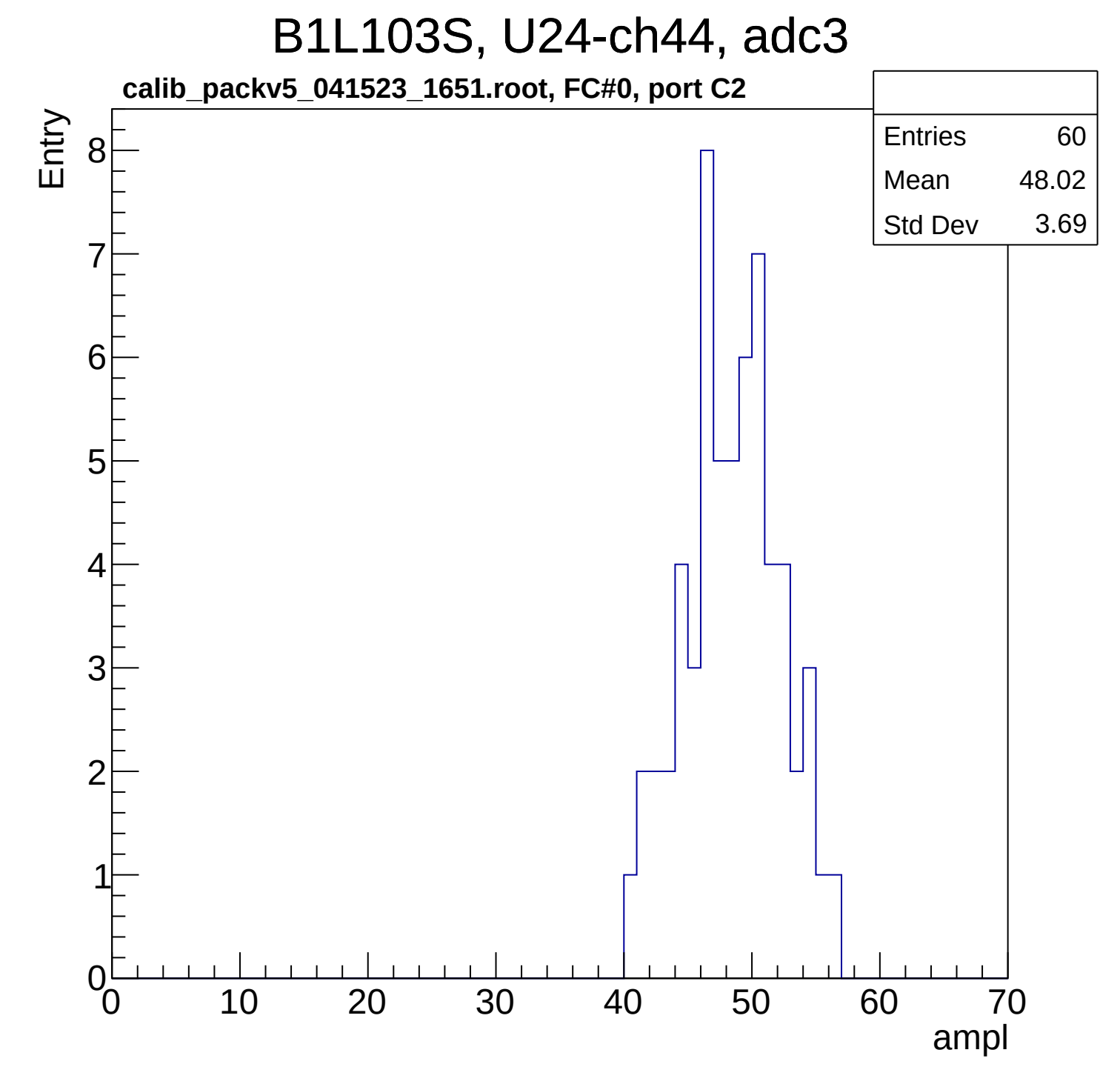
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U24-ch44, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 48.02
Std Dev 3.69
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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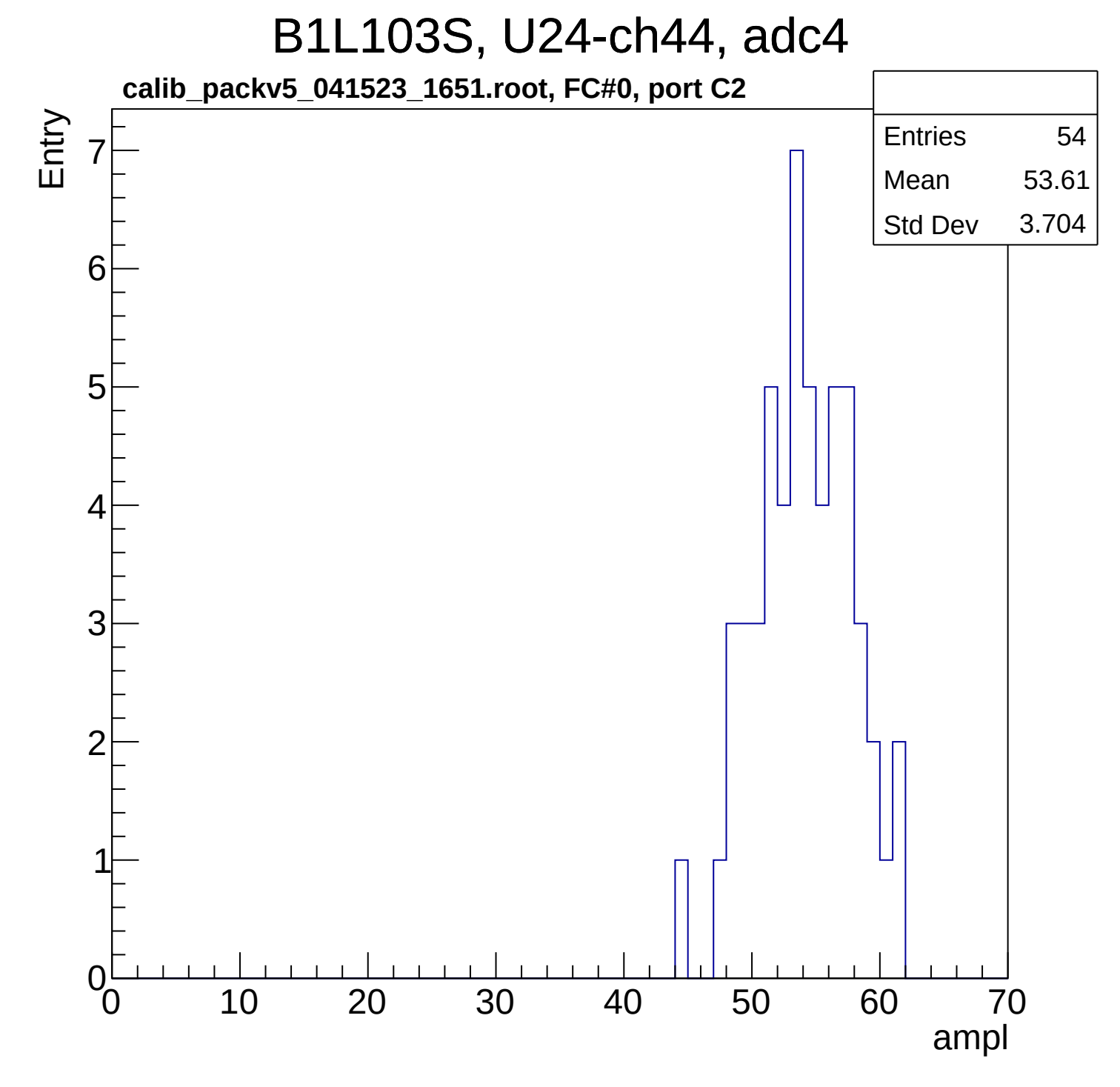
B1L103S, U24-ch44, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 53.61
Std Dev 3.704
Entry
ampl
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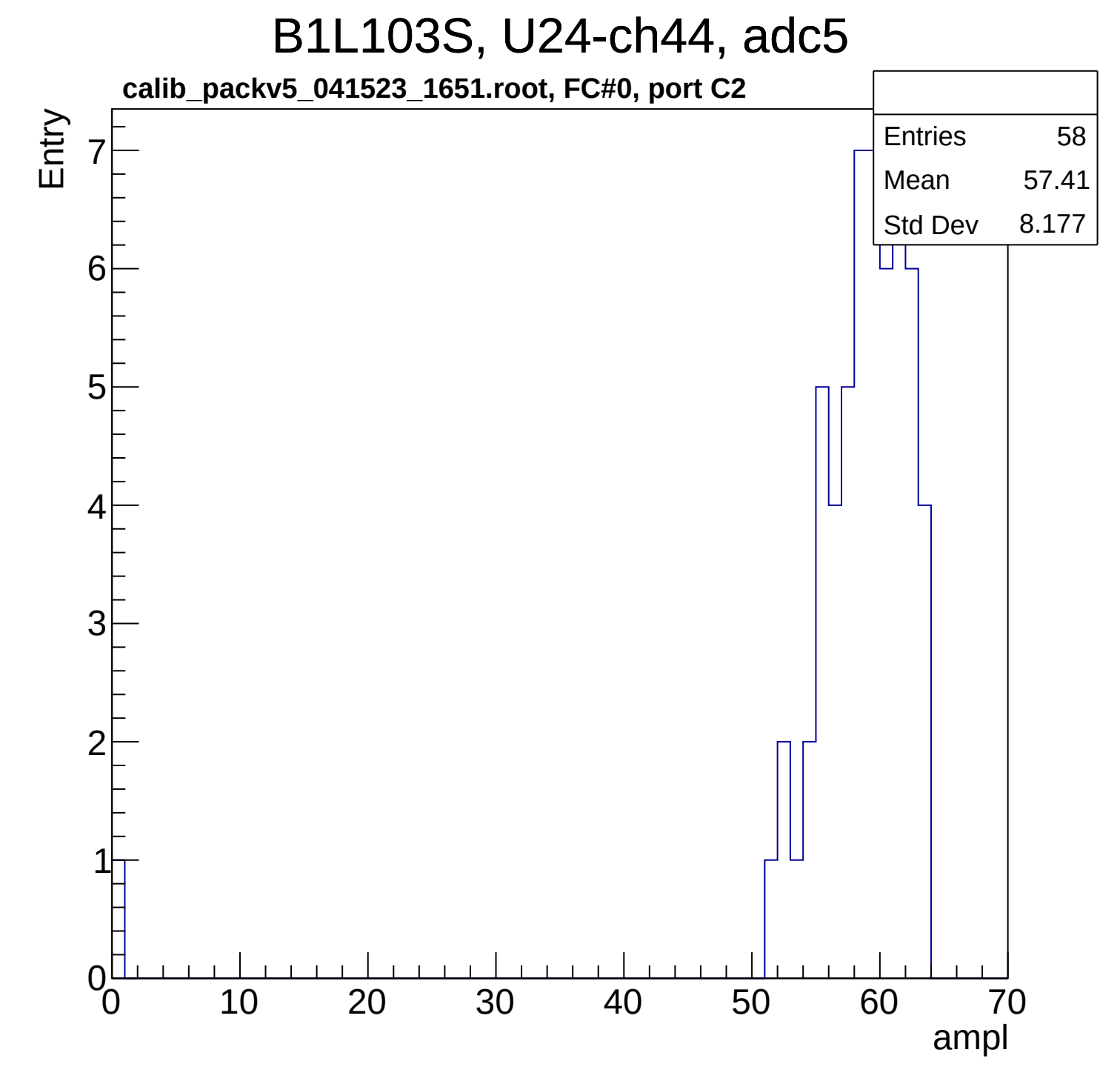
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U24-ch44, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 57.41
Std Dev 8.177
Entry
ampl
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3
4
5
6
7
0
10
20
30
40
50
60
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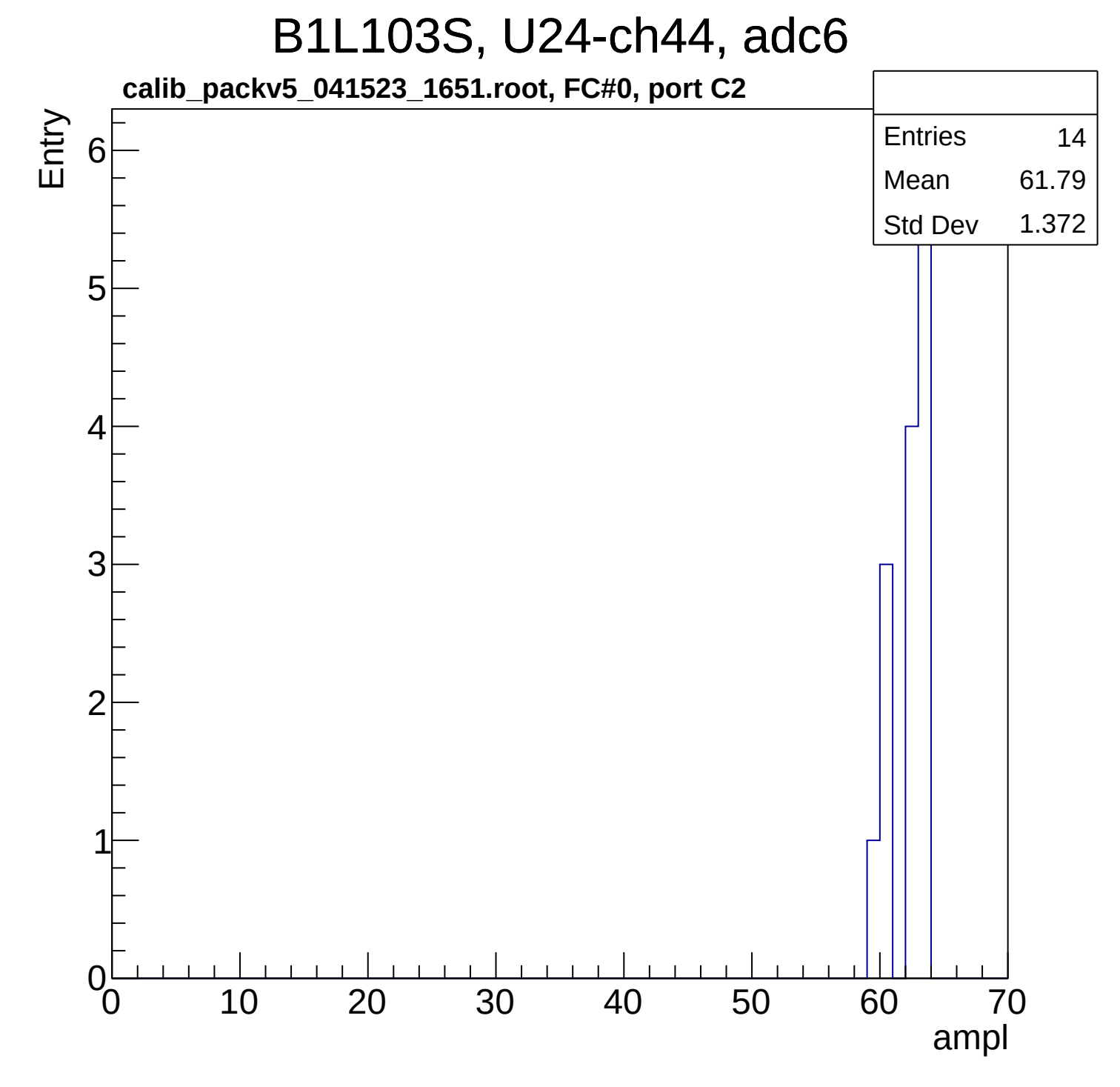
B1L103S, U24-ch44, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 14
Mean 61.79
Std Dev 1.372
Entry
ampl
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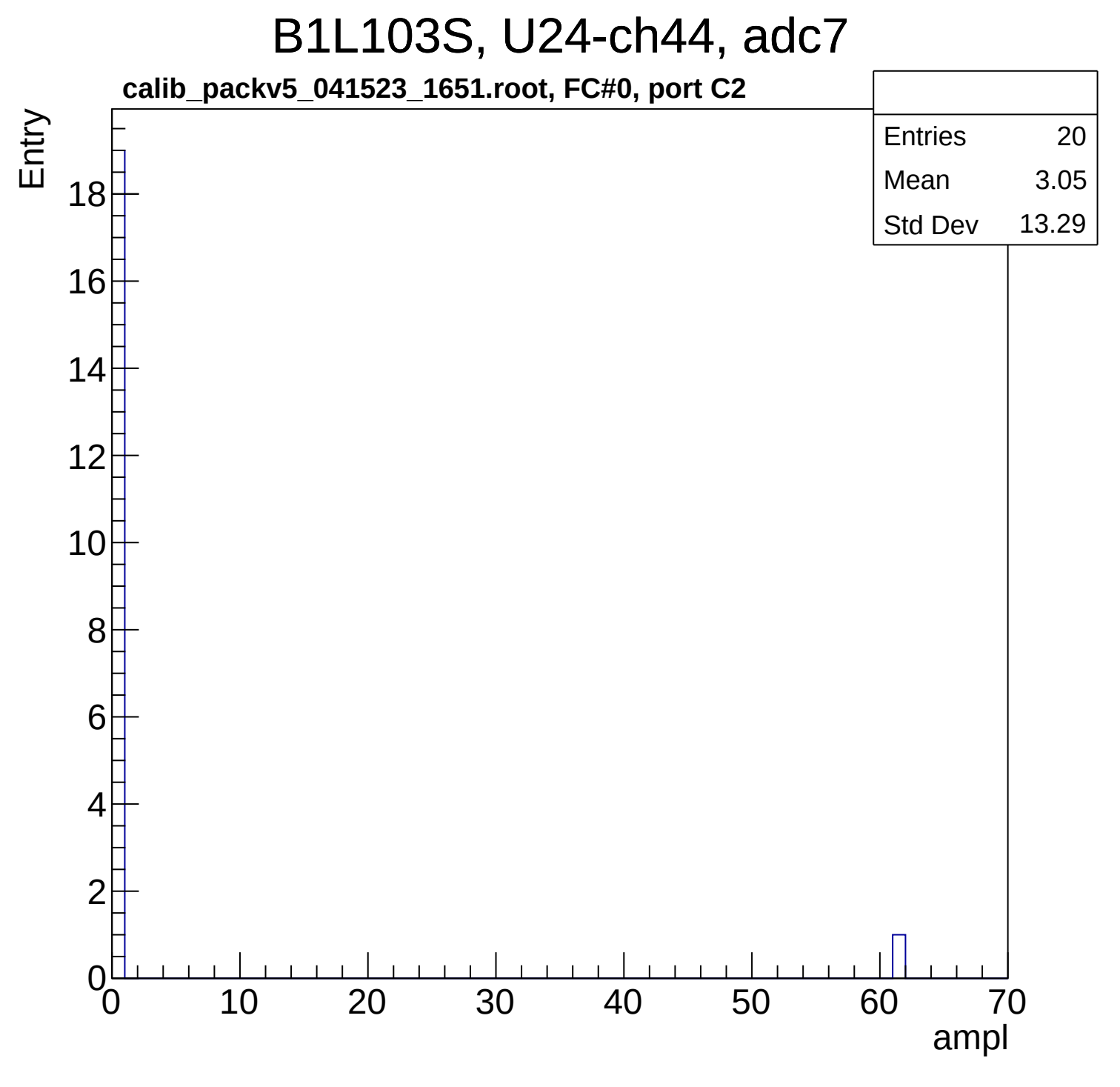
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U24-ch44, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.05
Std Dev 13.29
Entry
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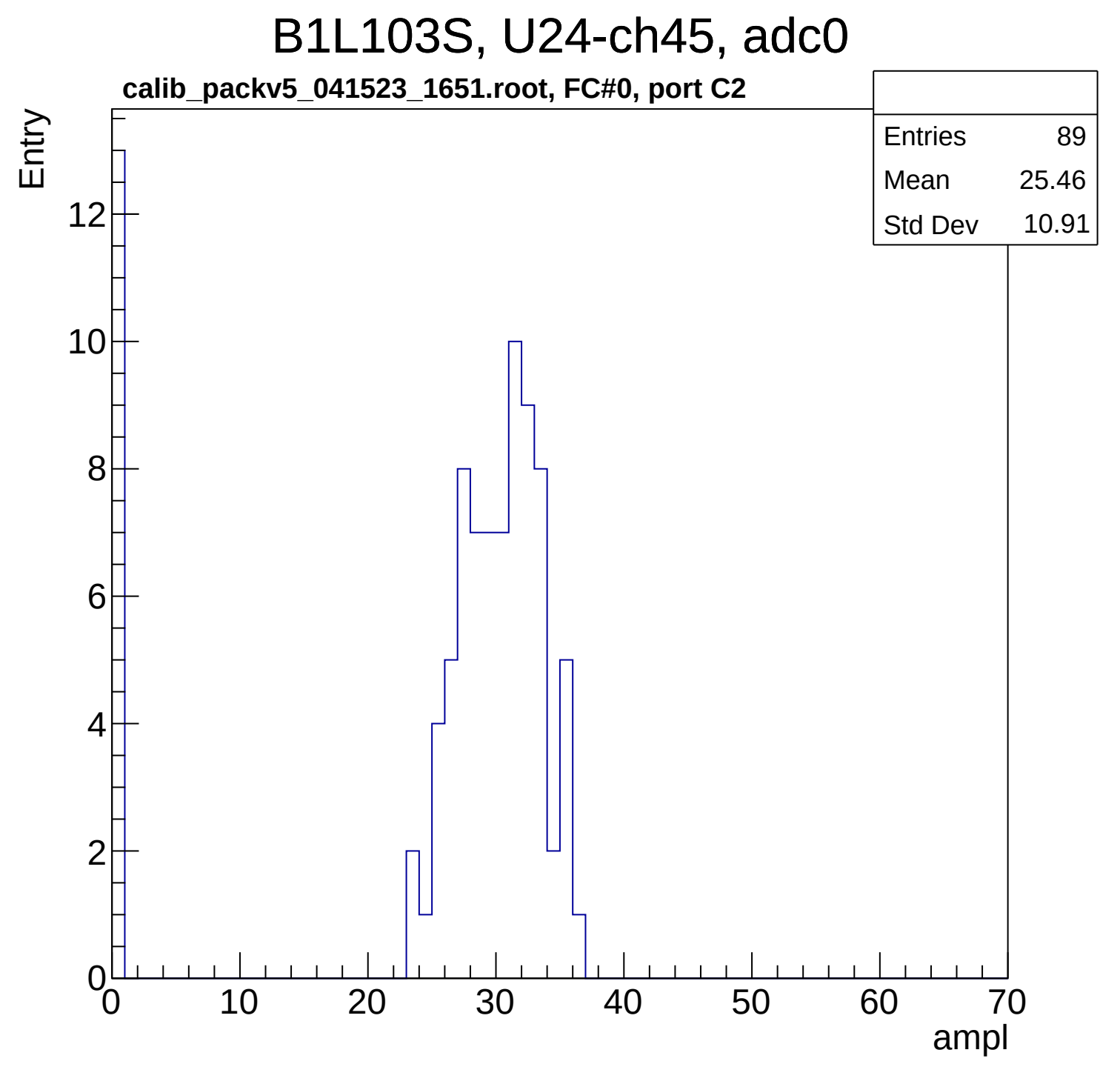
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch45, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 89
Mean 25.46
Std Dev 10.91
Entry
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8
10
12
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20
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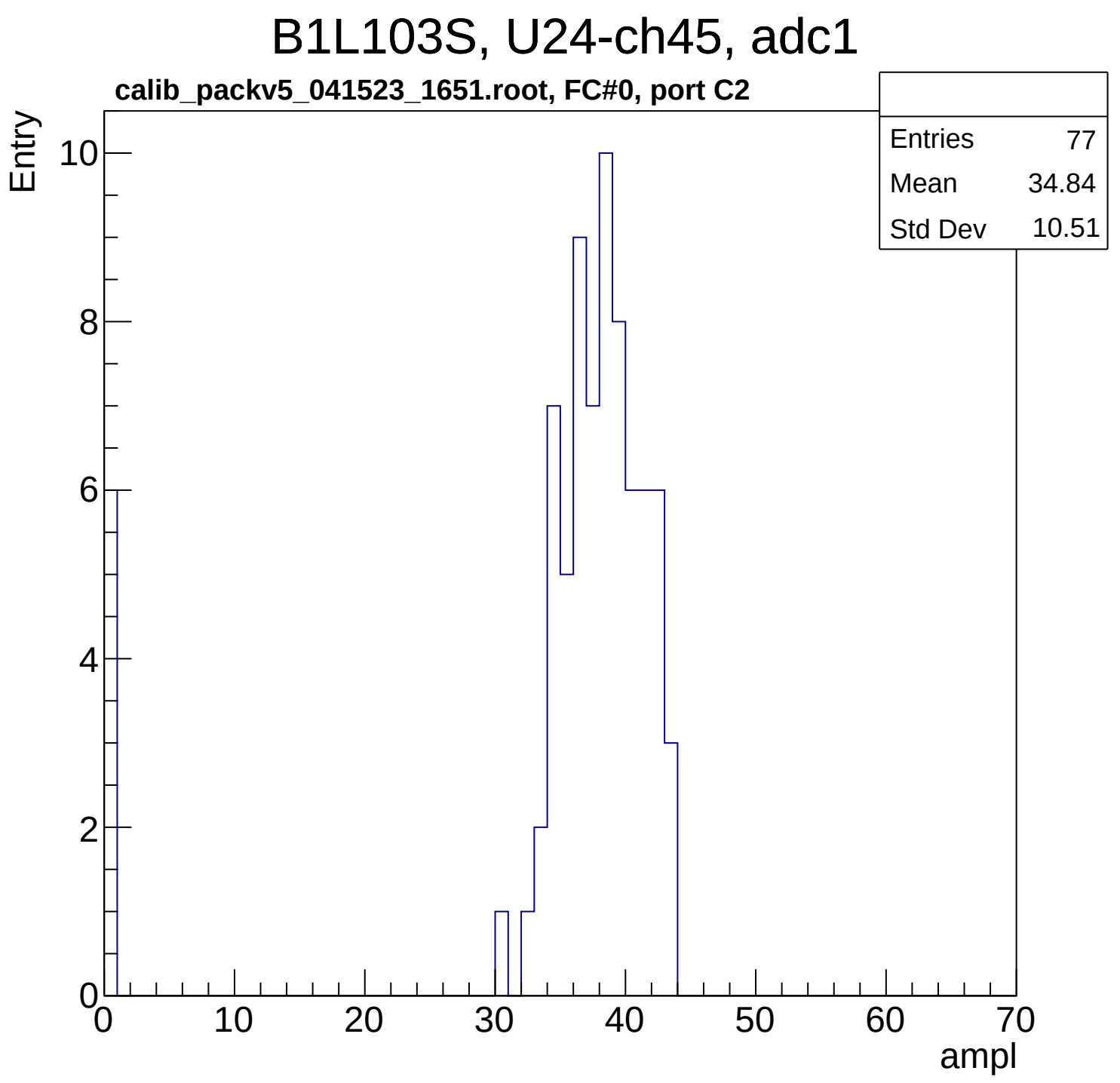
60
70
ampl


B1L103S, U24-ch45, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 34.84
Std Dev 10.51
Entry
ampl
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4
6
8
10
0
10
20
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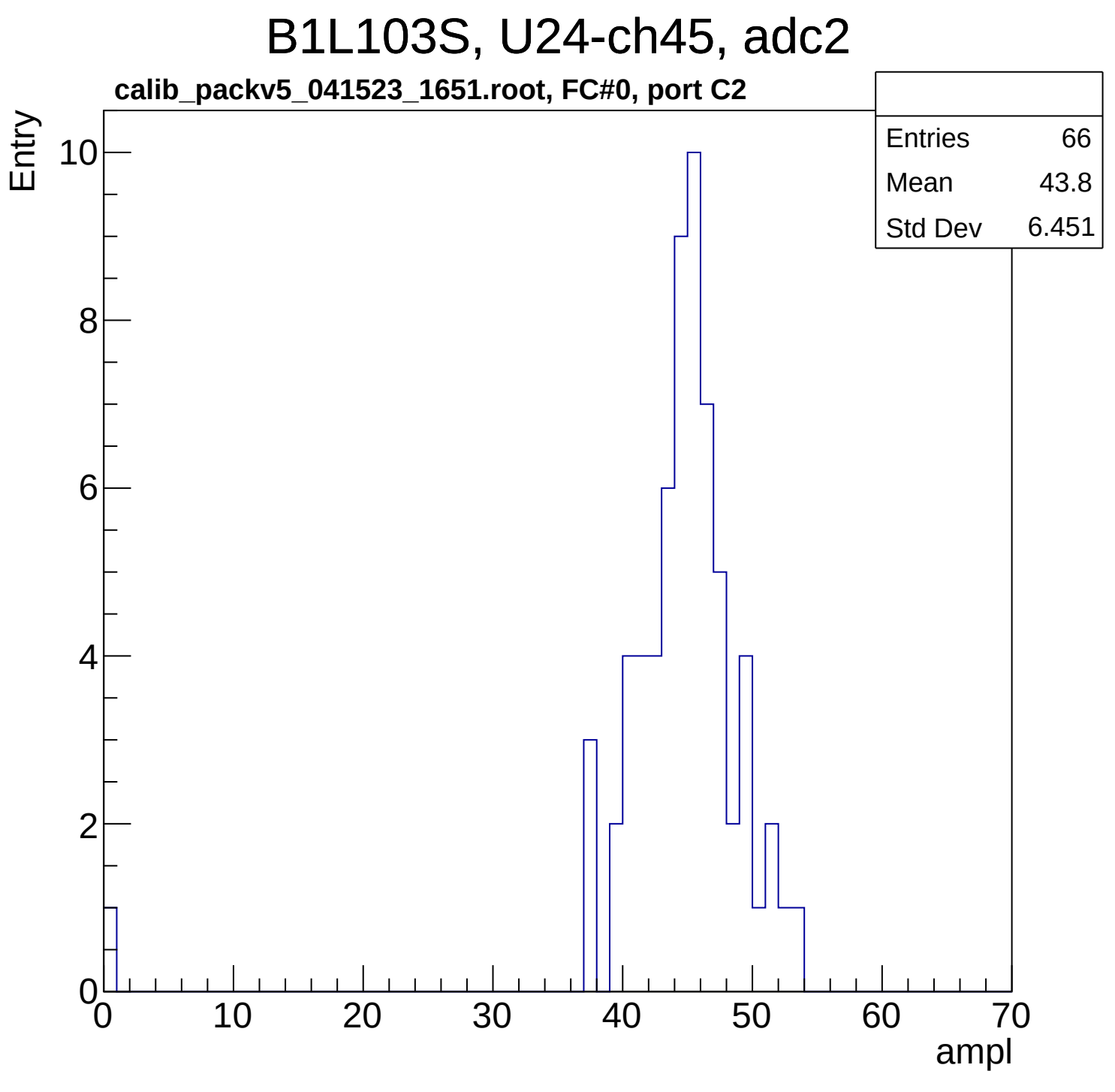
40
50
60
70


B1L103S, U24-ch45, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 43.8
Std Dev 6.451
Entry
ampl
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4
6
8
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0
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60
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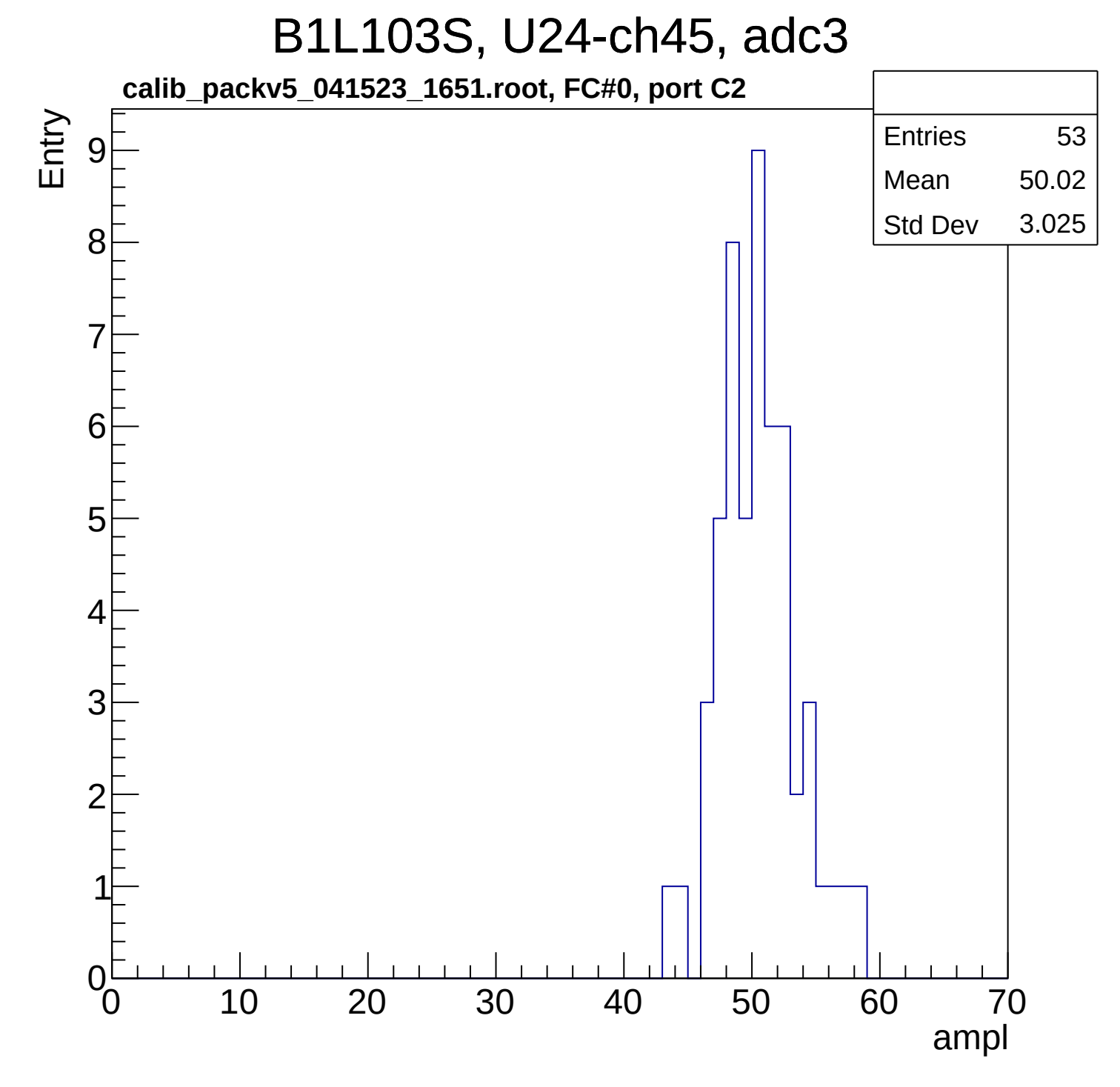
B1L103S, U24-ch45, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 50.02
Std Dev 3.025
Entry
ampl
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2
3
4
5
6
7
8
9
0
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60
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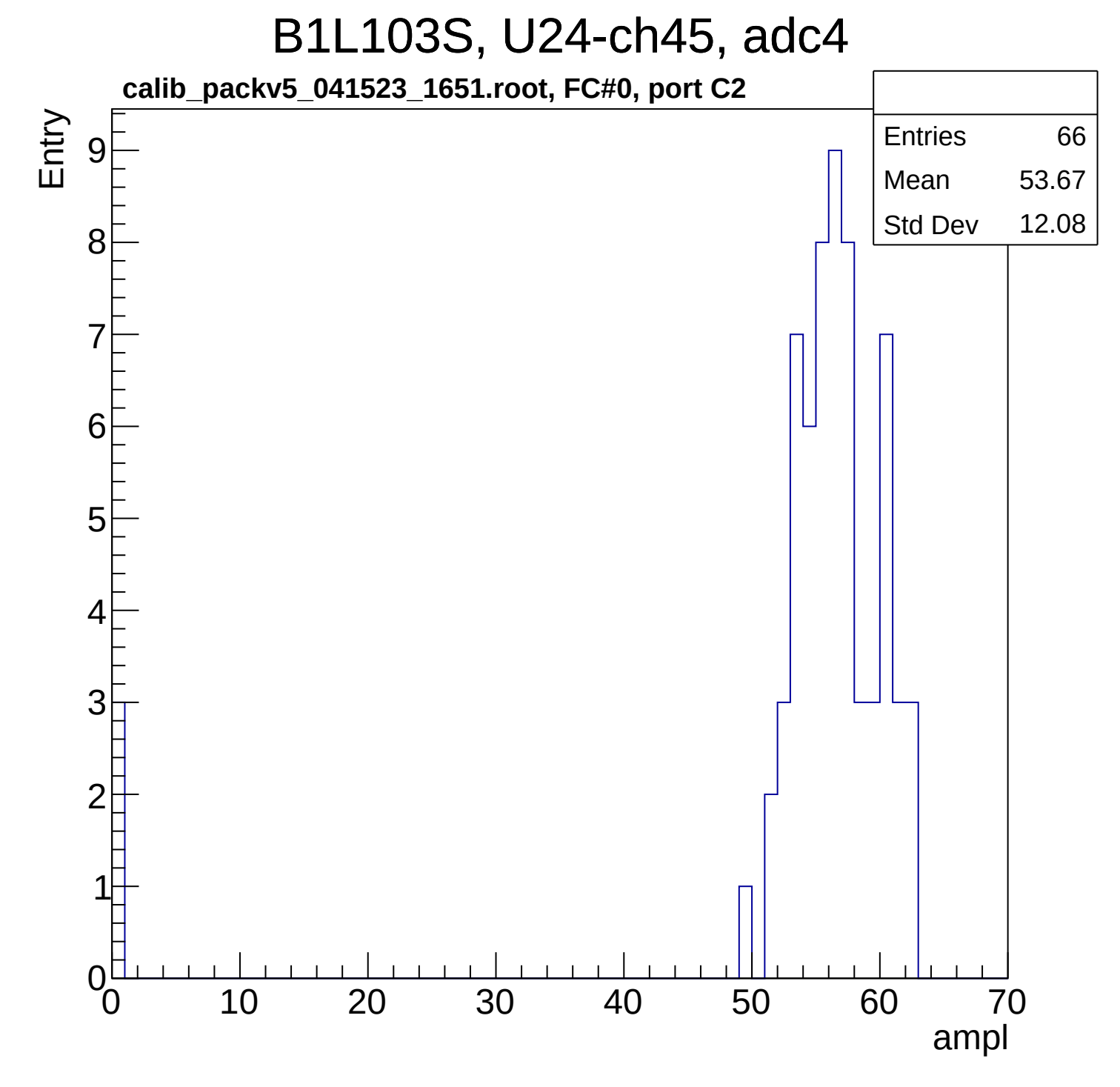
B1L103S, U24-ch45, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 53.67
Std Dev 12.08
Entry
ampl
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2
3
4
5
6
7
8
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0
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20
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40
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60
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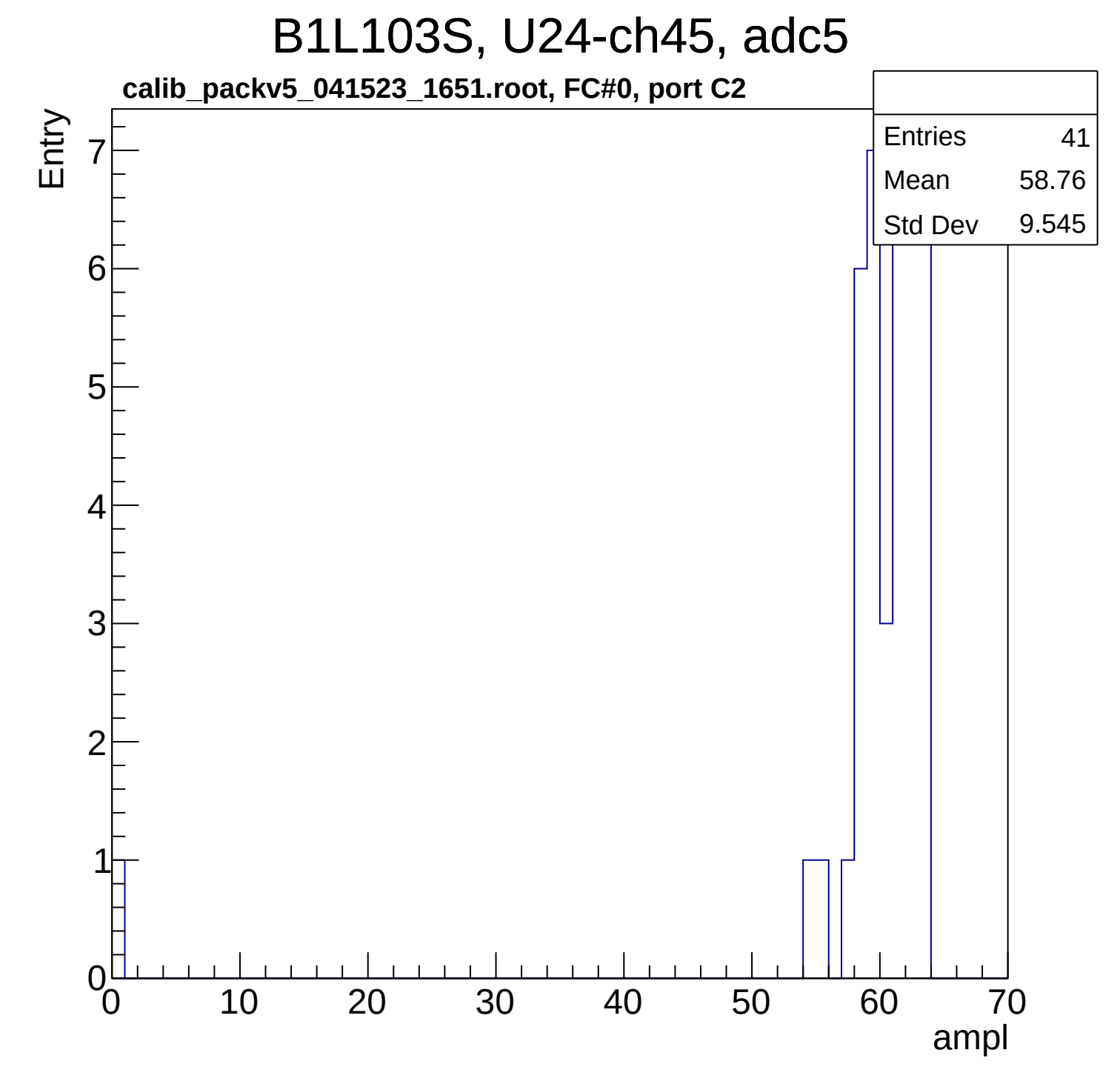
B1L103S, U24-ch45, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 41
Mean 58.76
Std Dev 9.545
Entry
ampl
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2
3
4
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0
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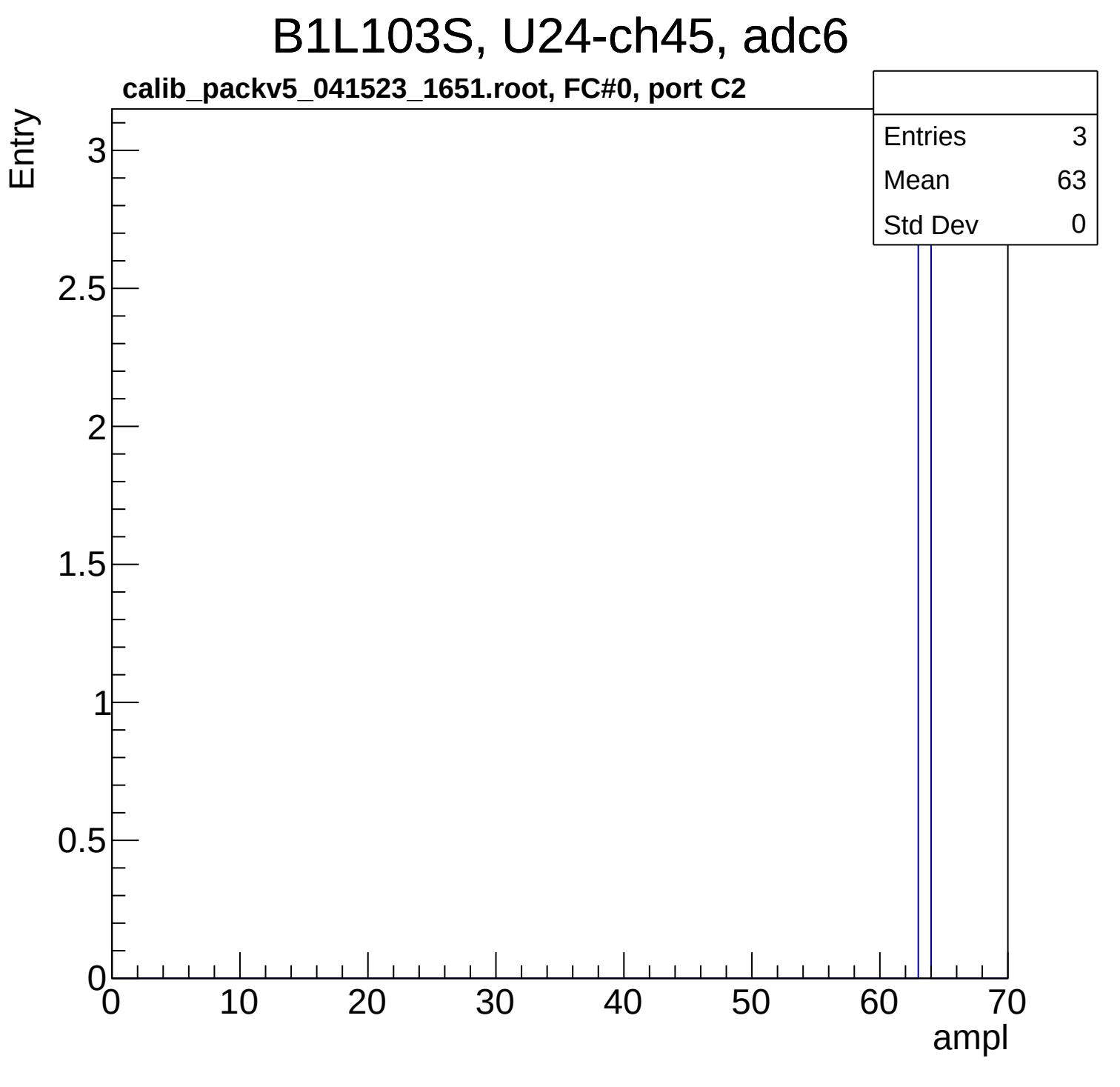
B1L103S, U24-ch45, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 3
Mean 63
Std Dev 0
Entry
ampl
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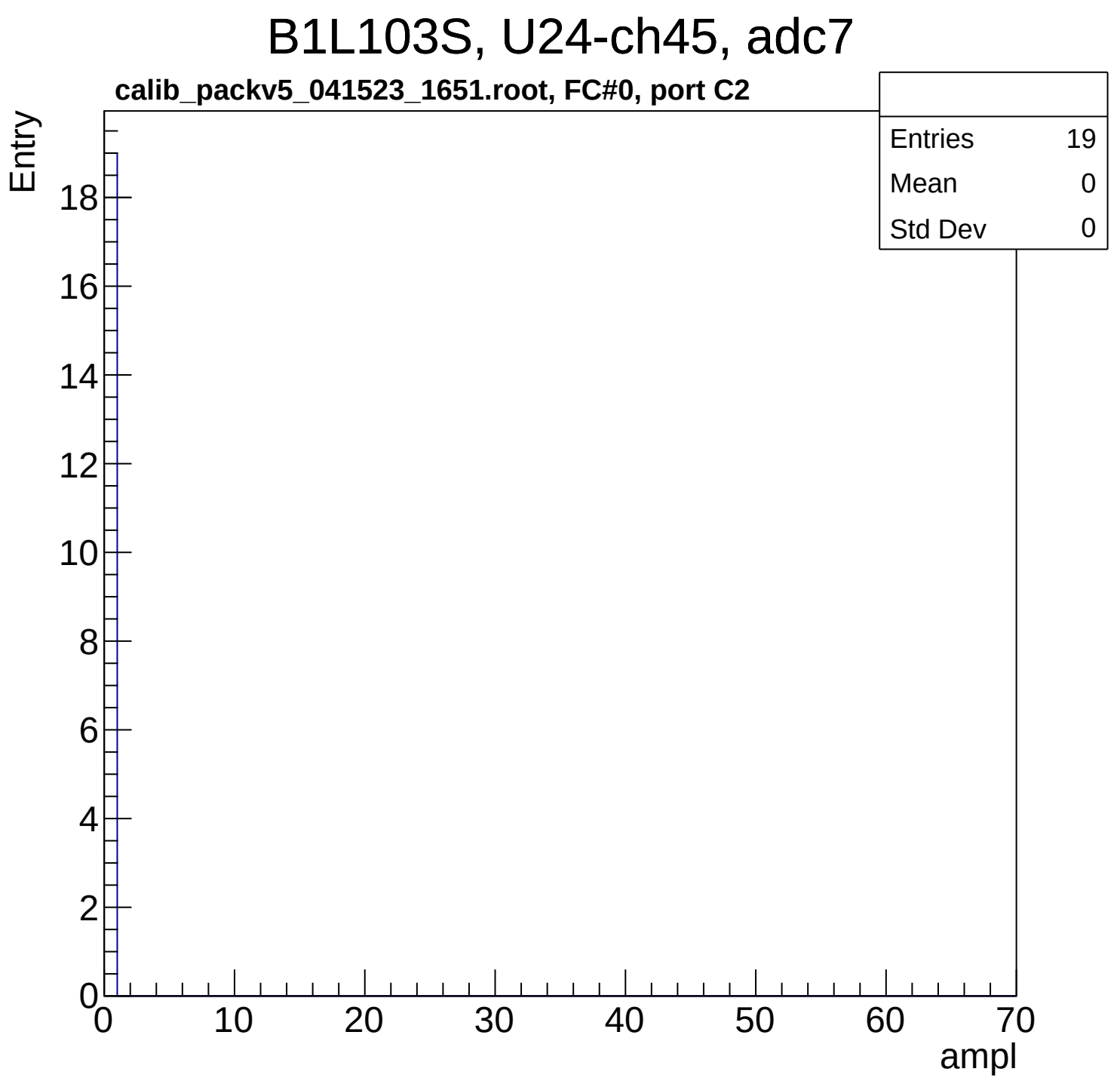
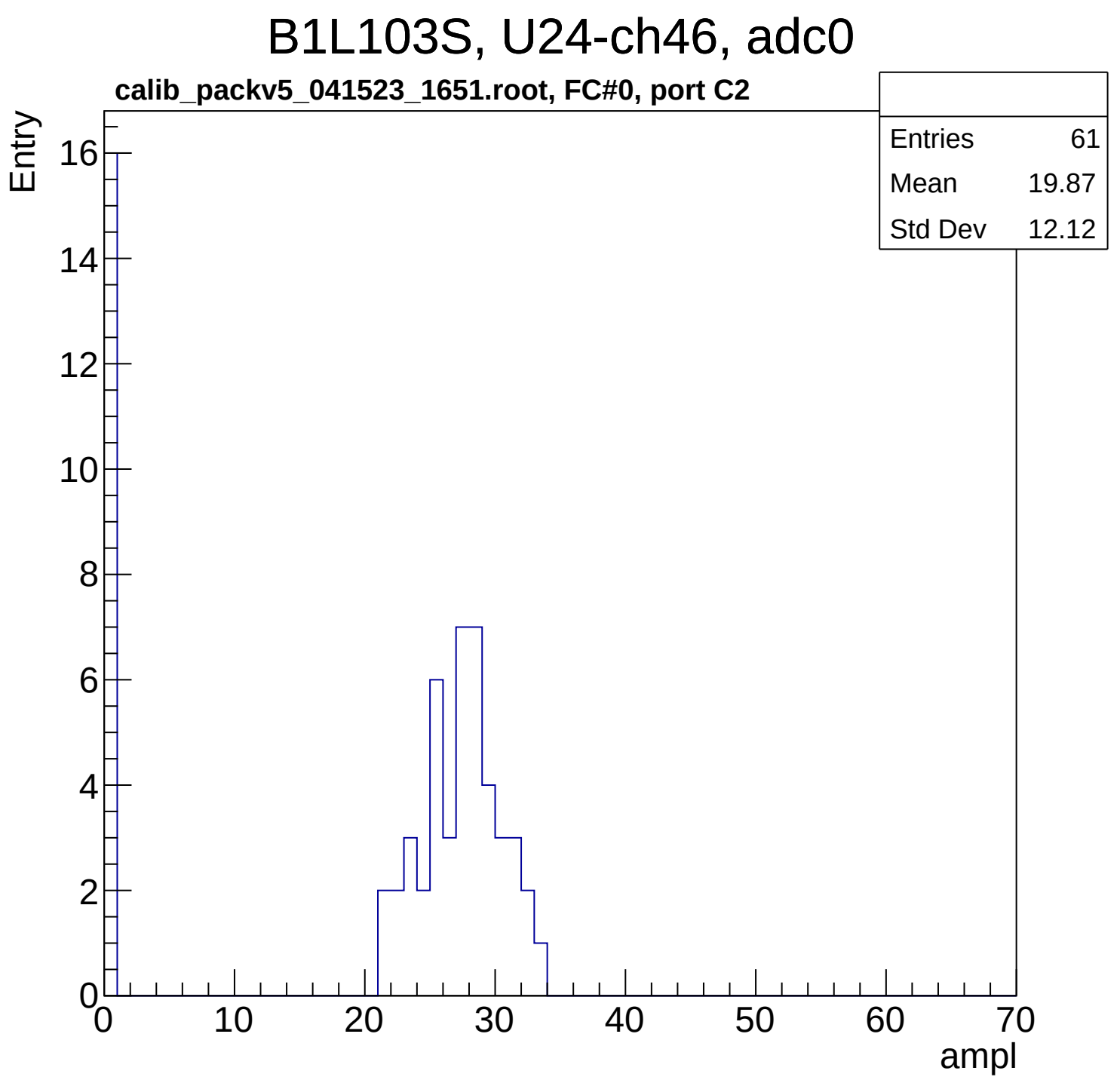
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U24-ch45, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch46, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 19.87
Std Dev 12.12
Entry
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6
8
10
12
14
16
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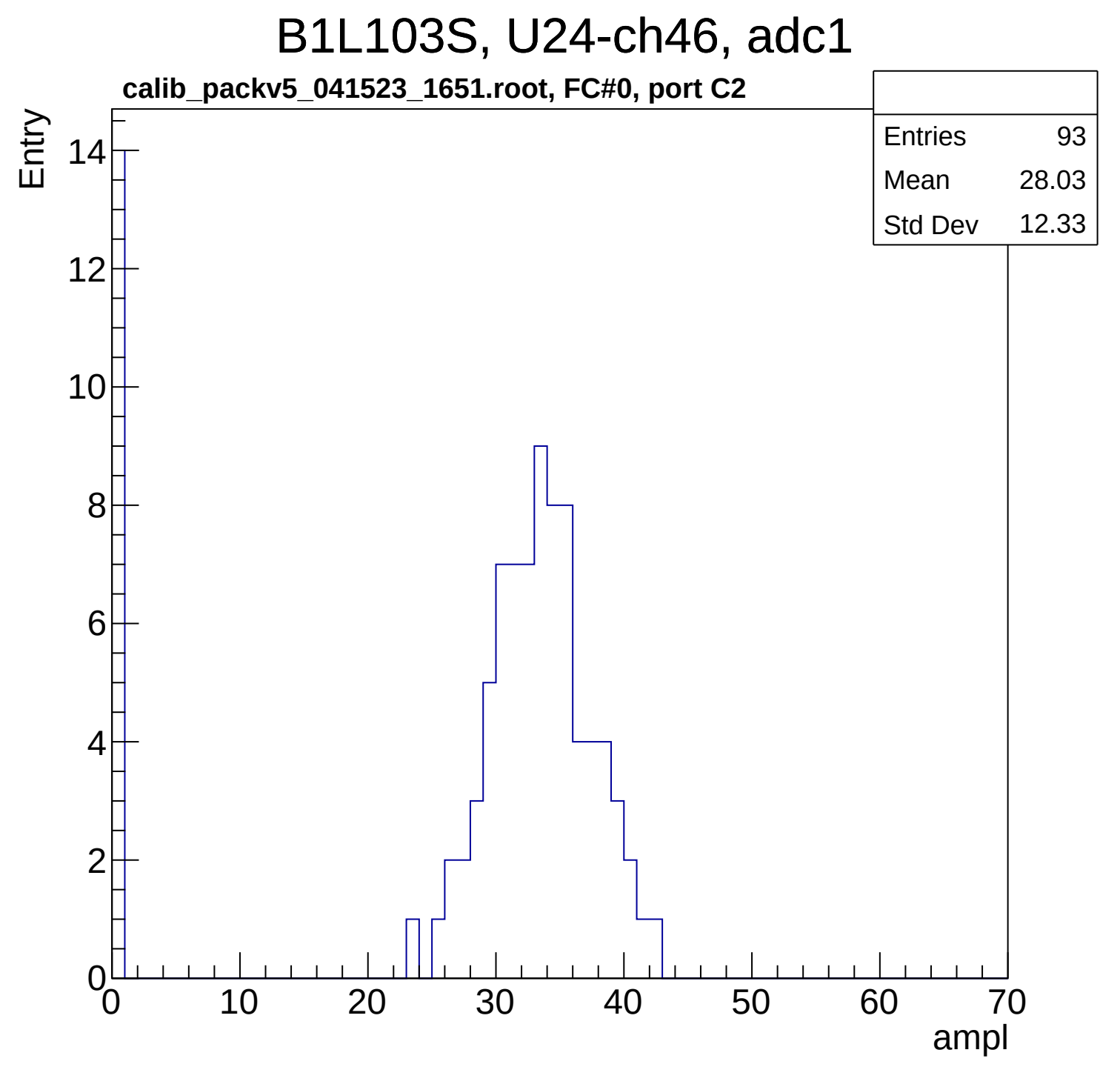
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch46, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 93
Mean 28.03
Std Dev 12.33
Entry
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6
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10
12
14
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10
20
30
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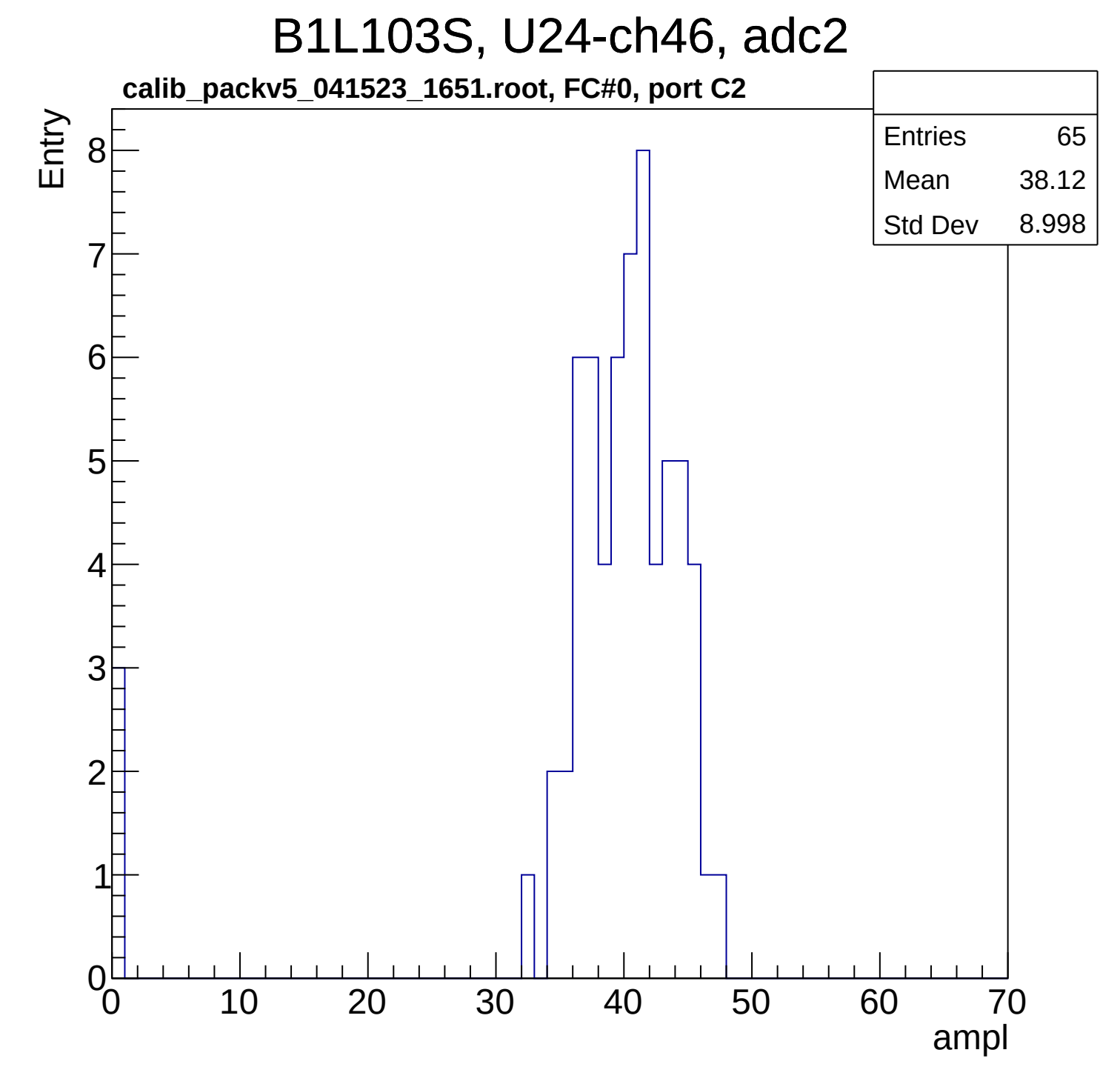
50
60
70
ampl


B1L103S, U24-ch46, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 38.12
Std Dev 8.998
Entry
ampl
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2
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4
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6
7
8
0
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20
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40
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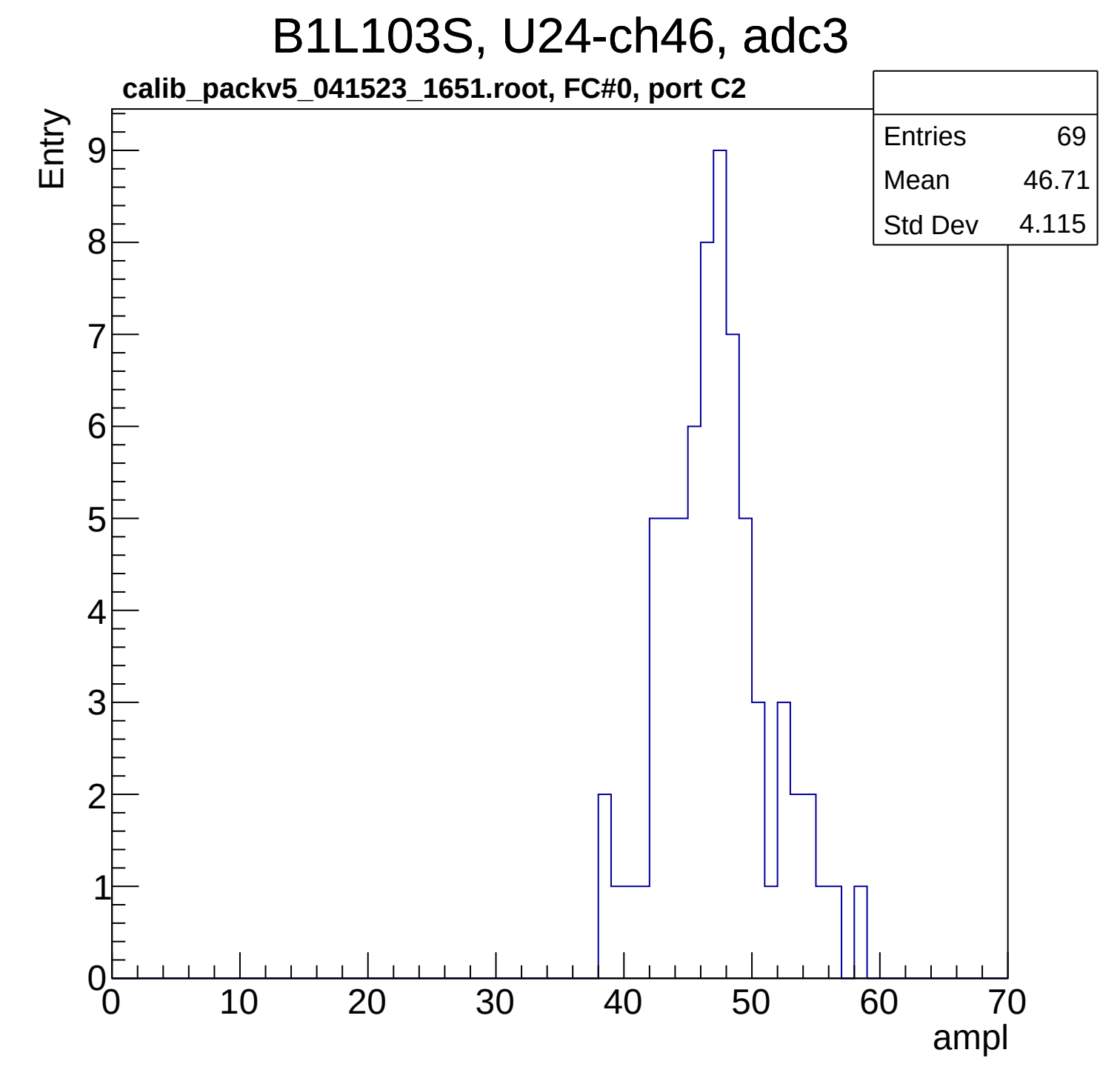
60
70


B1L103S, U24-ch46, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 46.71
Std Dev 4.115
Entry
ampl
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3
4
5
6
7
8
9
0
10
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40
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60
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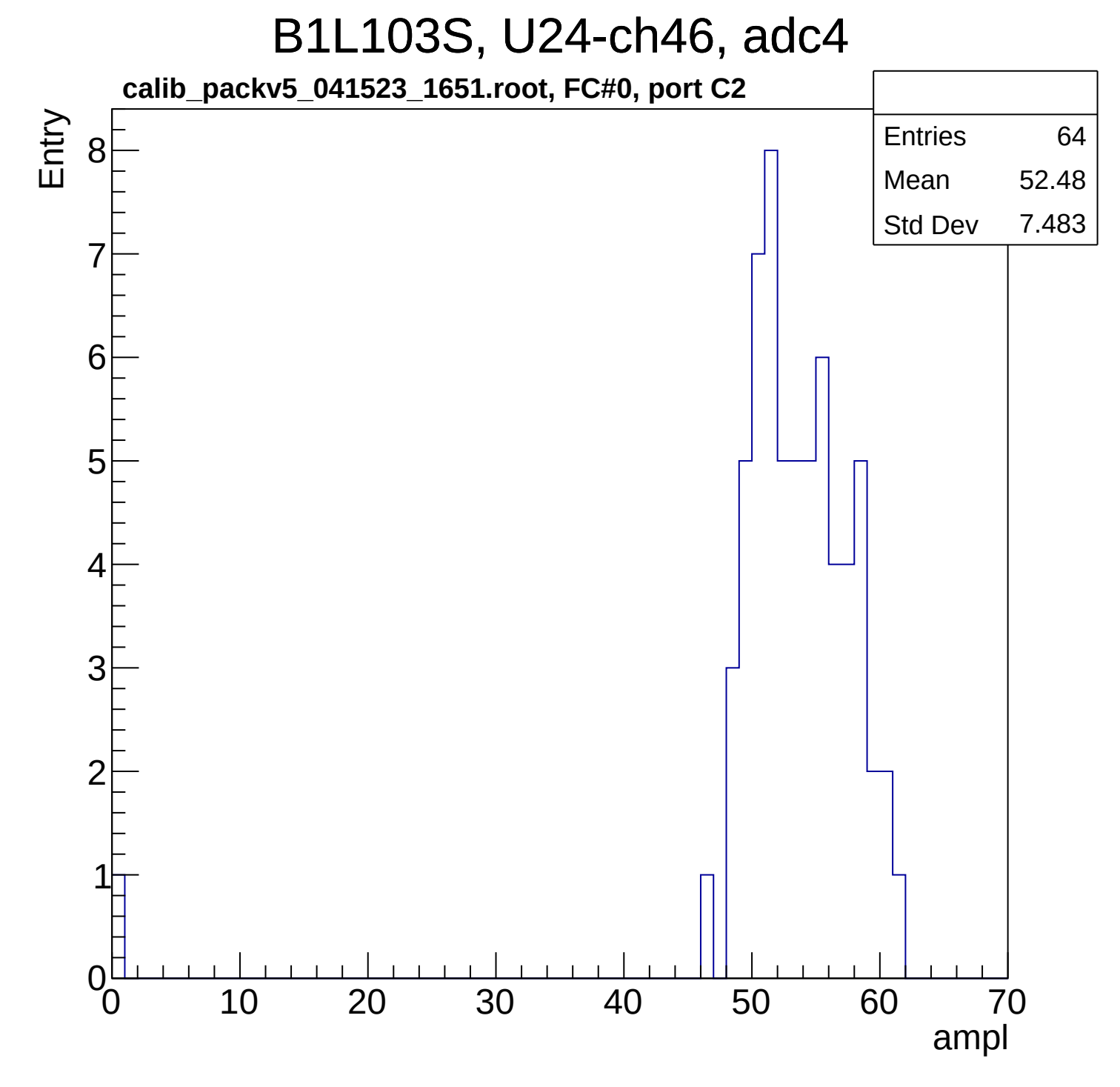
B1L103S, U24-ch46, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 52.48
Std Dev 7.483
Entry
ampl
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5
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0
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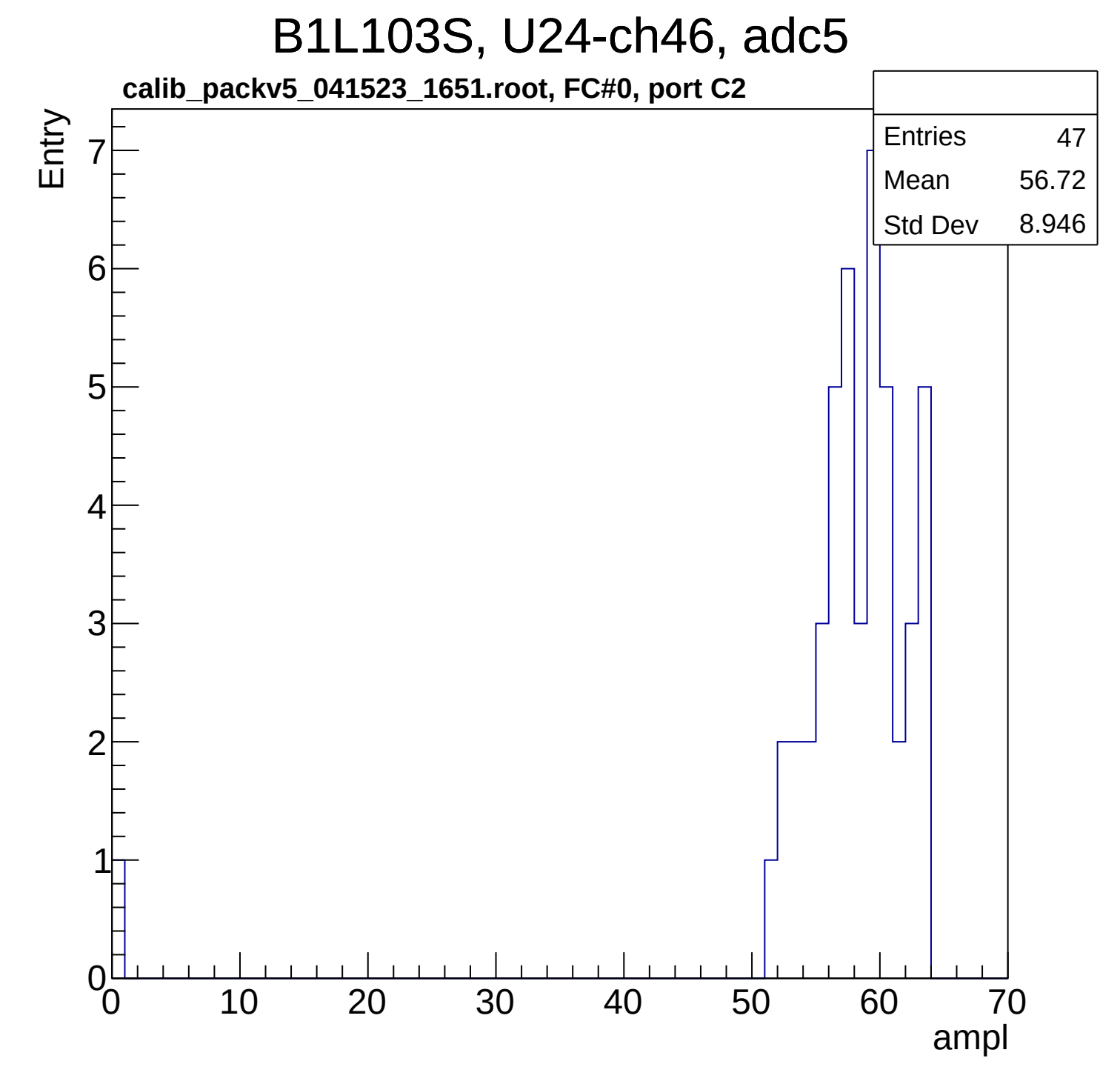
B1L103S, U24-ch46, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 56.72
Std Dev 8.946
Entry
ampl
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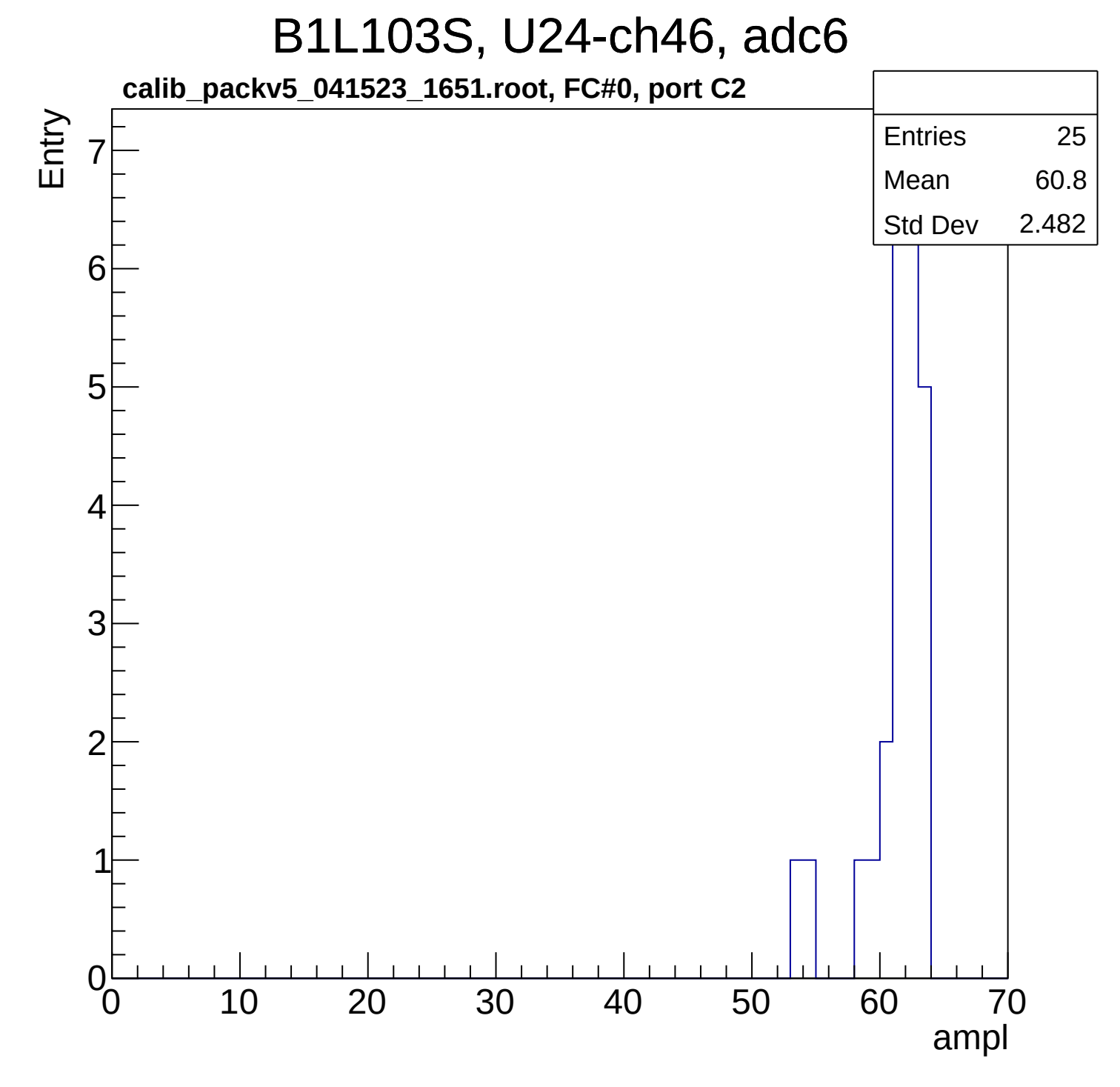
B1L103S, U24-ch46, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 25
Mean 60.8
Std Dev 2.482
Entry
ampl
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1
2
3
4
5
6
7
0
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40
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60
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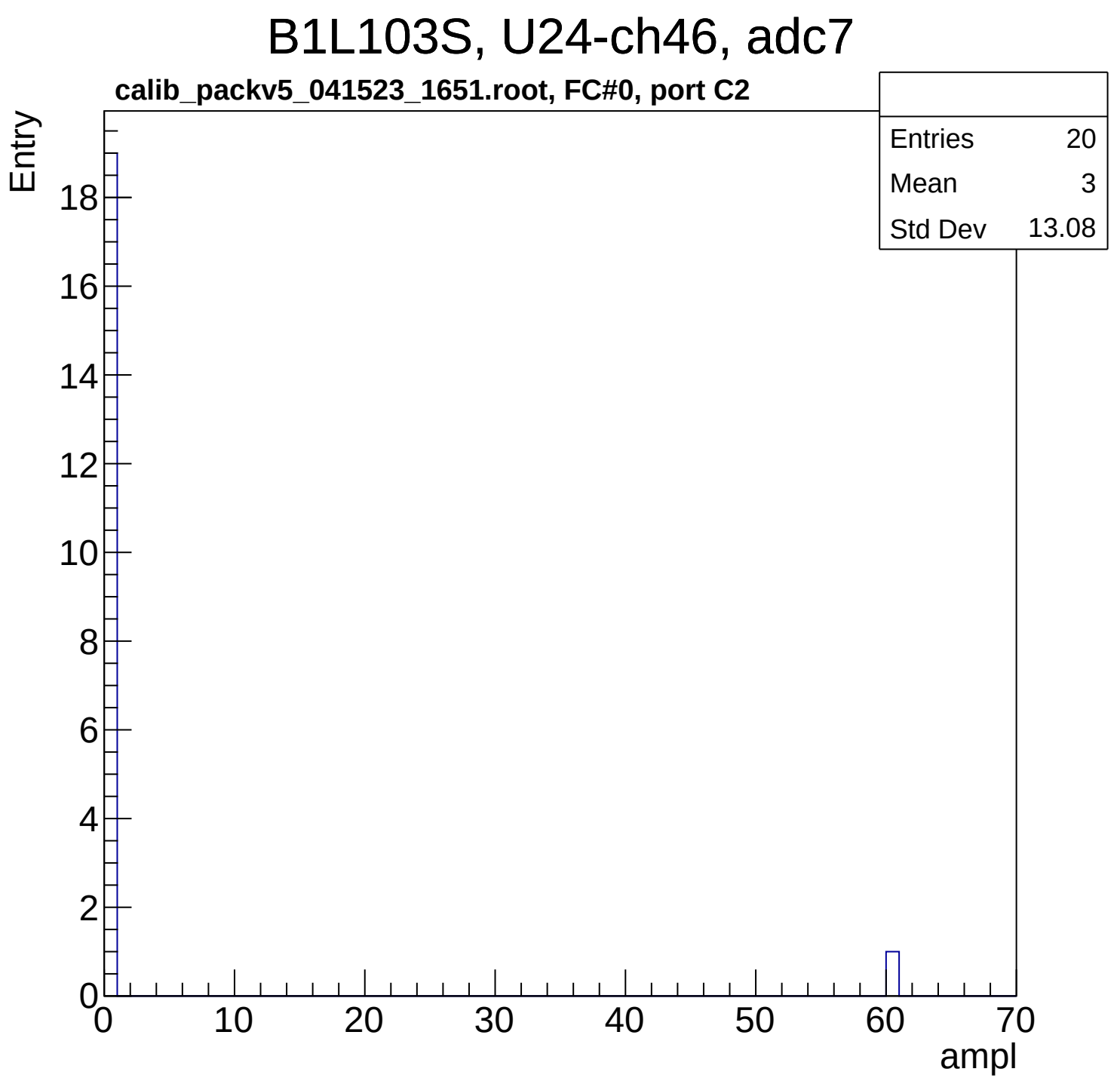
B1L103S, U24-ch46, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3
Std Dev 13.08
Entry
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6
8
10
12
14
16
18
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10
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50
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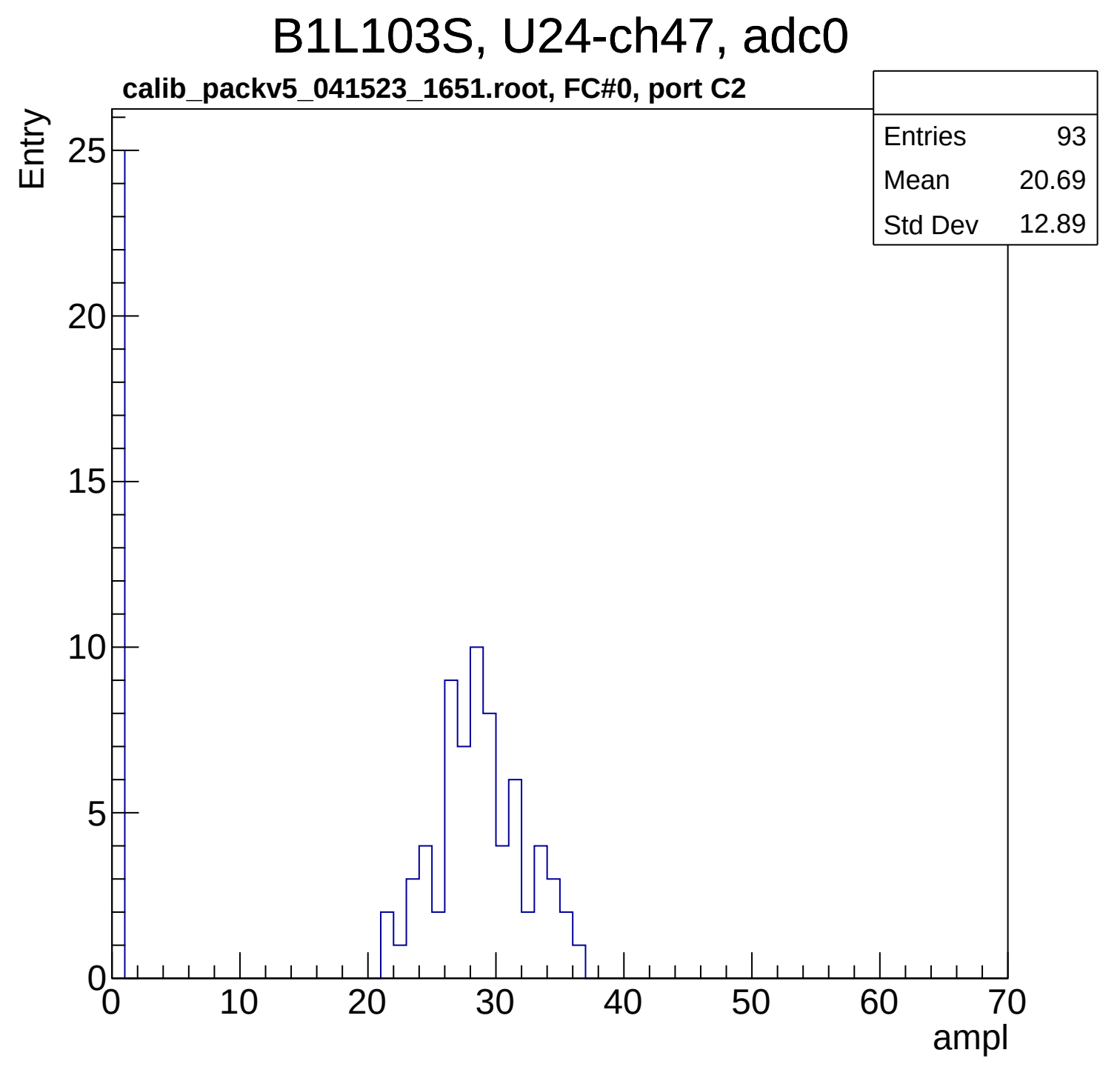
70
ampl


B1L103S, U24-ch47, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 93
Mean 20.69
Std Dev 12.89
Entry
ampl
0
5
10
15
20
25
0
10
20
30
40
50
60
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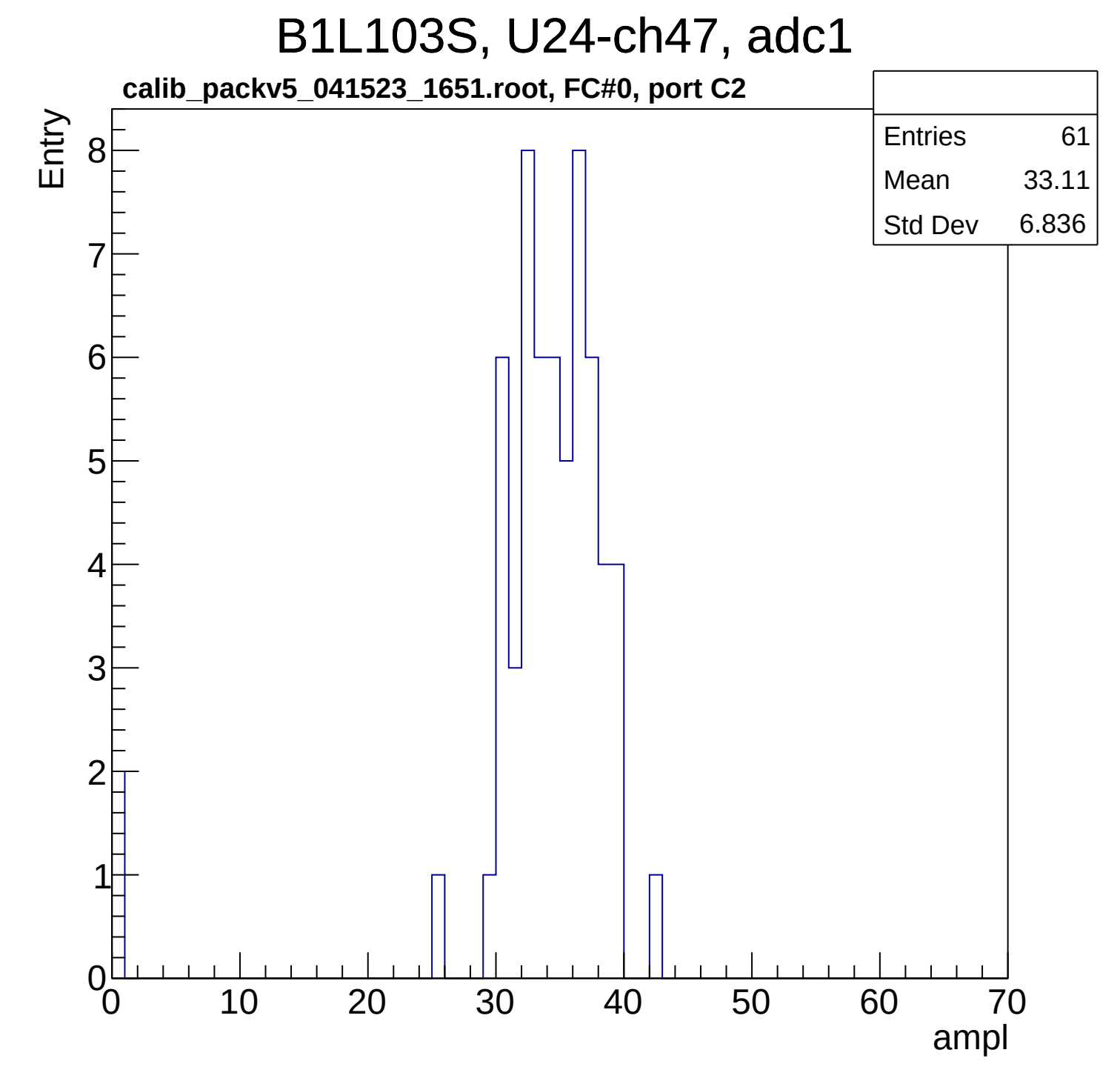
B1L103S, U24-ch47, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 33.11
Std Dev 6.836
Entry
ampl
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3
4
5
6
7
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0
10
20
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40
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60
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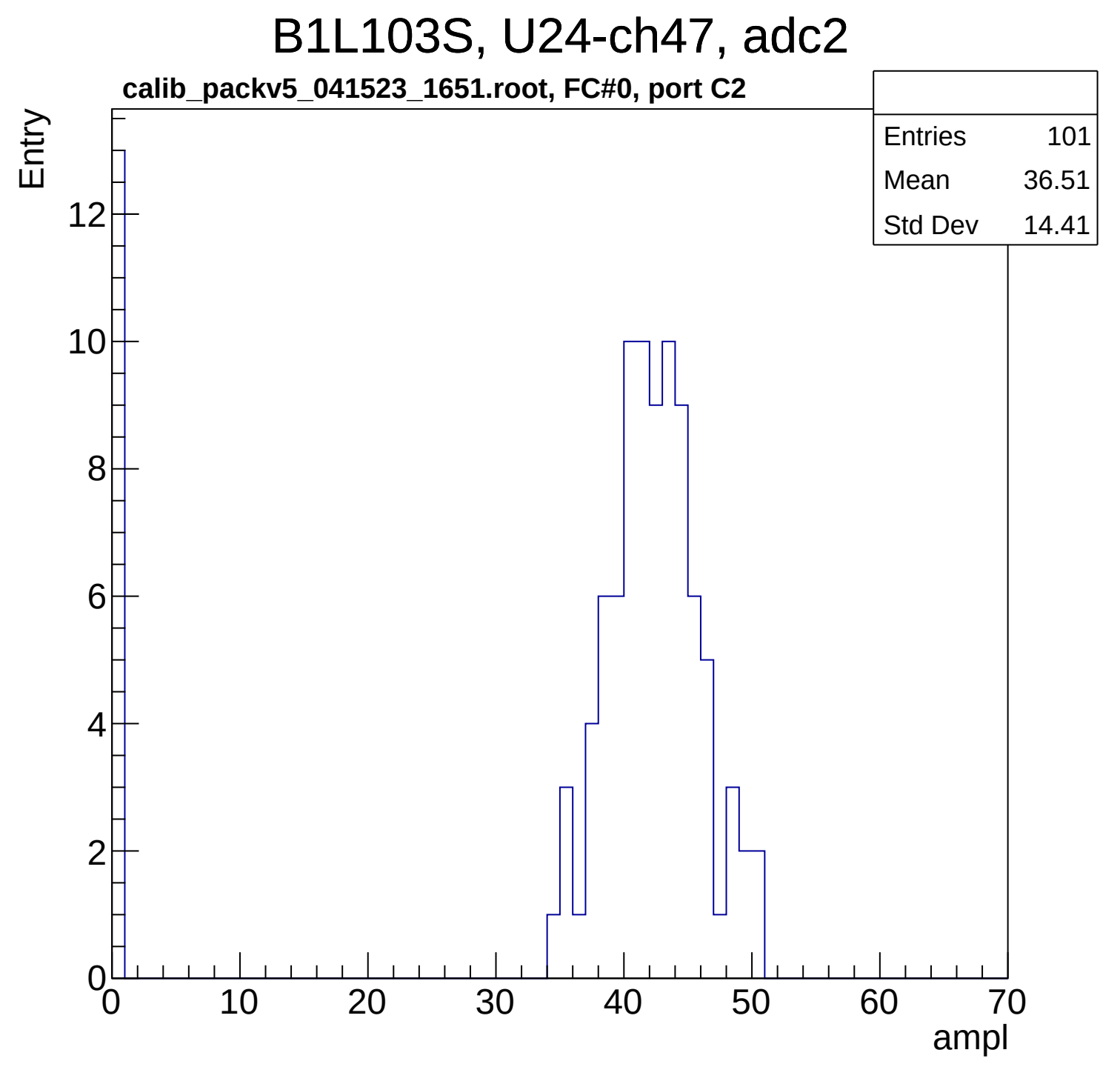
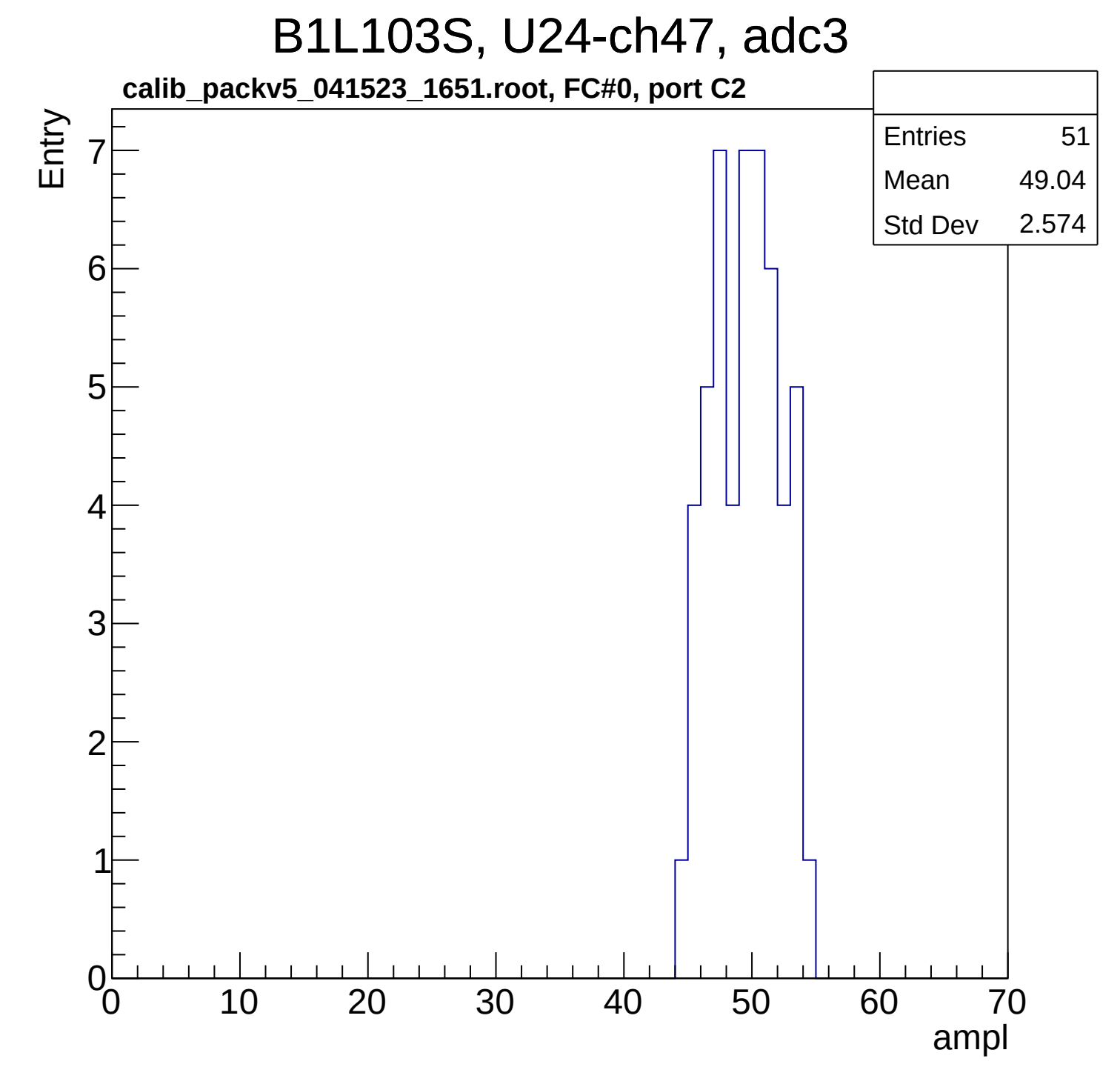
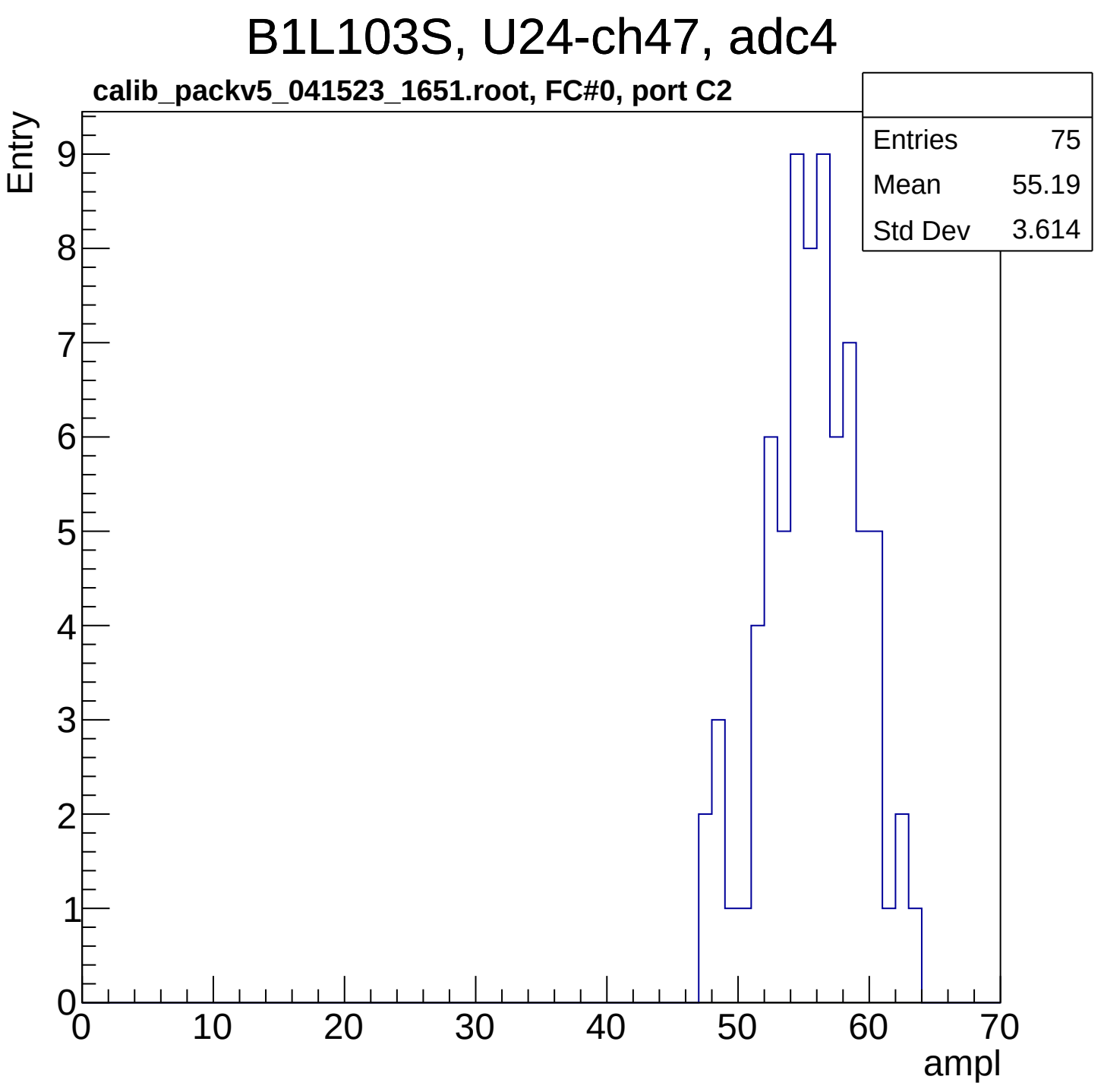

B1L103S, U24-ch47, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 101
Mean 36.51
Std Dev 14.41
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch47, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 49.04
Std Dev 2.574
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U24-ch47, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 55.19
Std Dev 3.614
Entry
ampl
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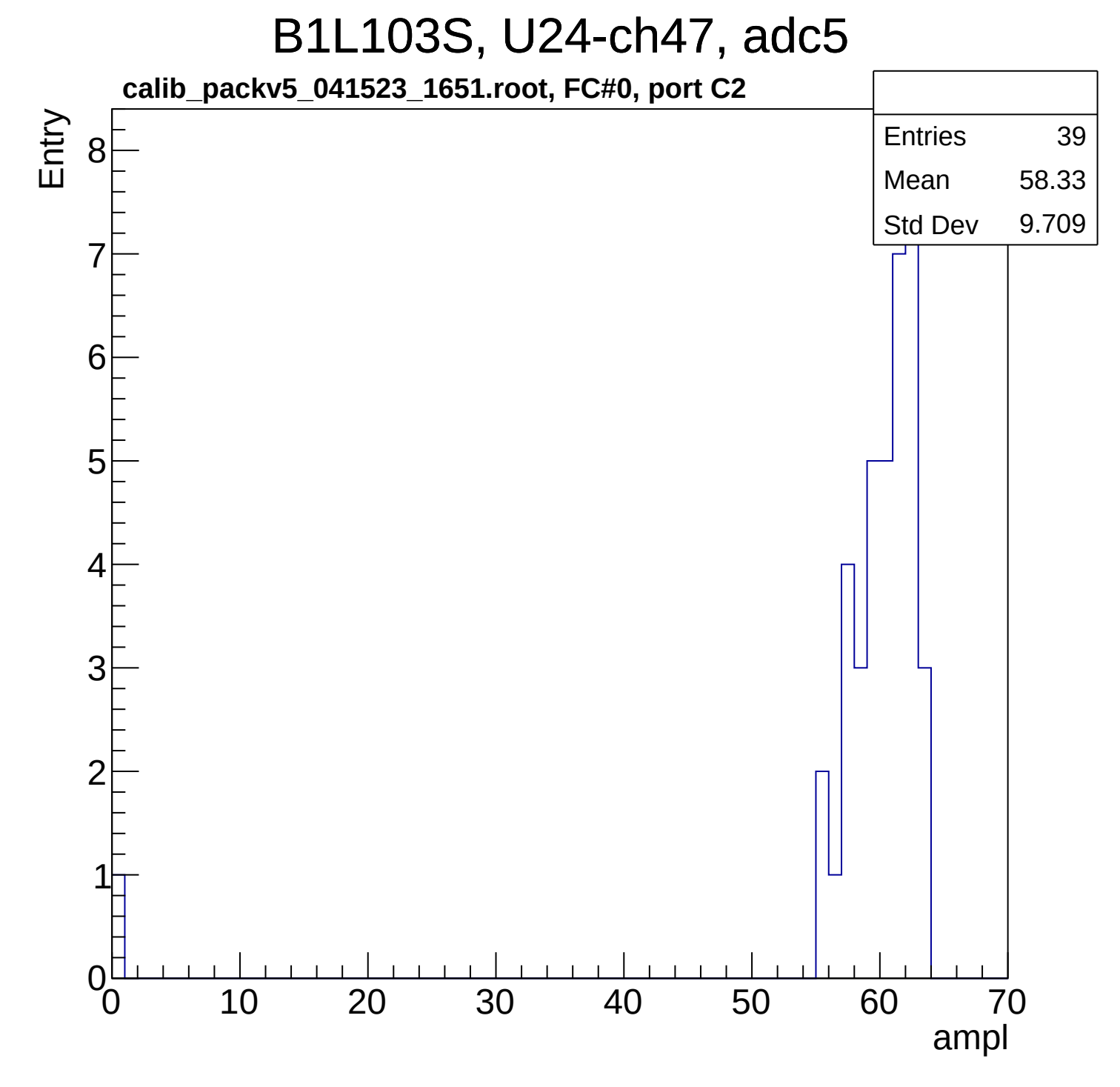
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U24-ch47, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 39
Mean 58.33
Std Dev 9.709
Entry
ampl
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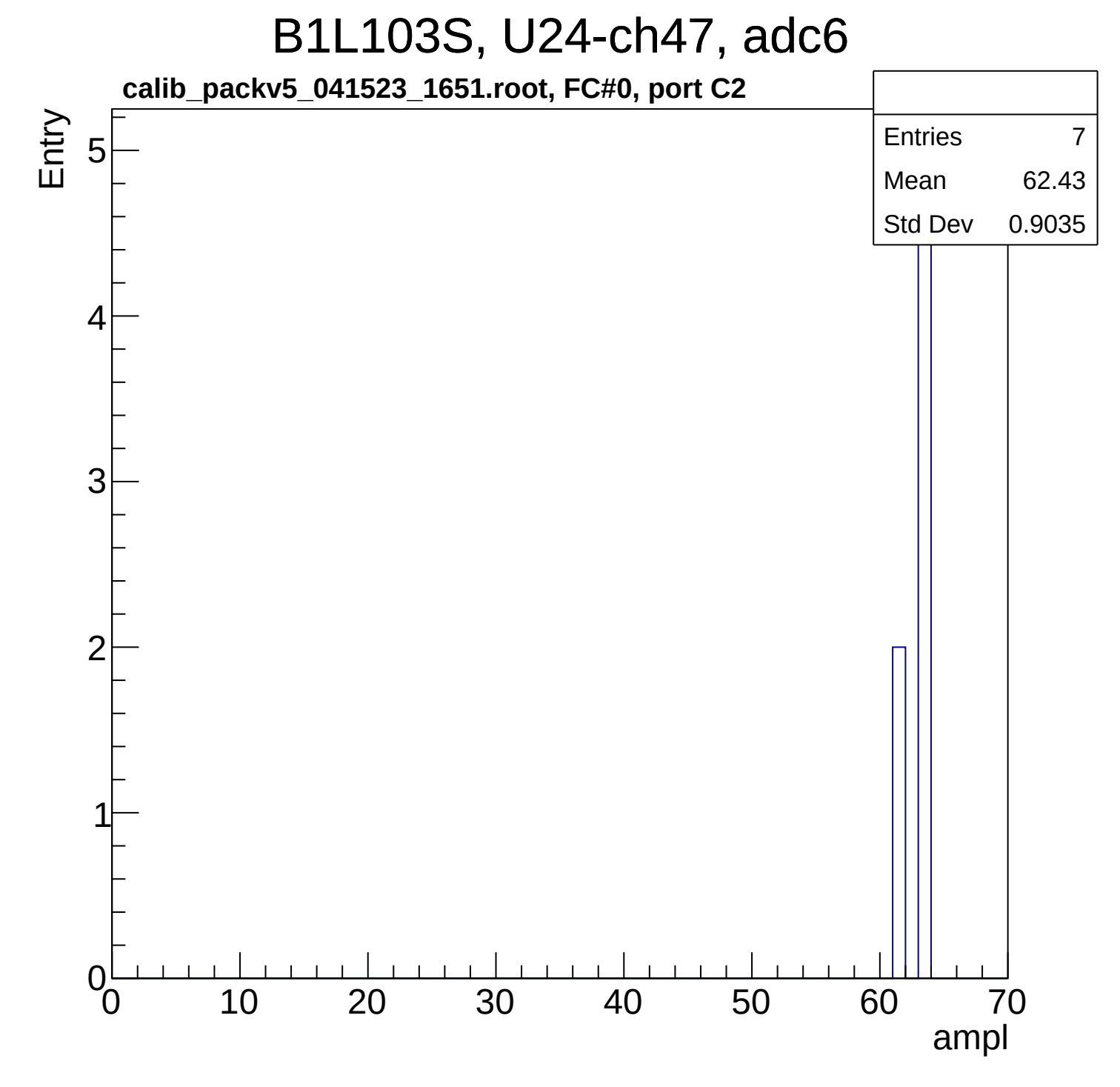
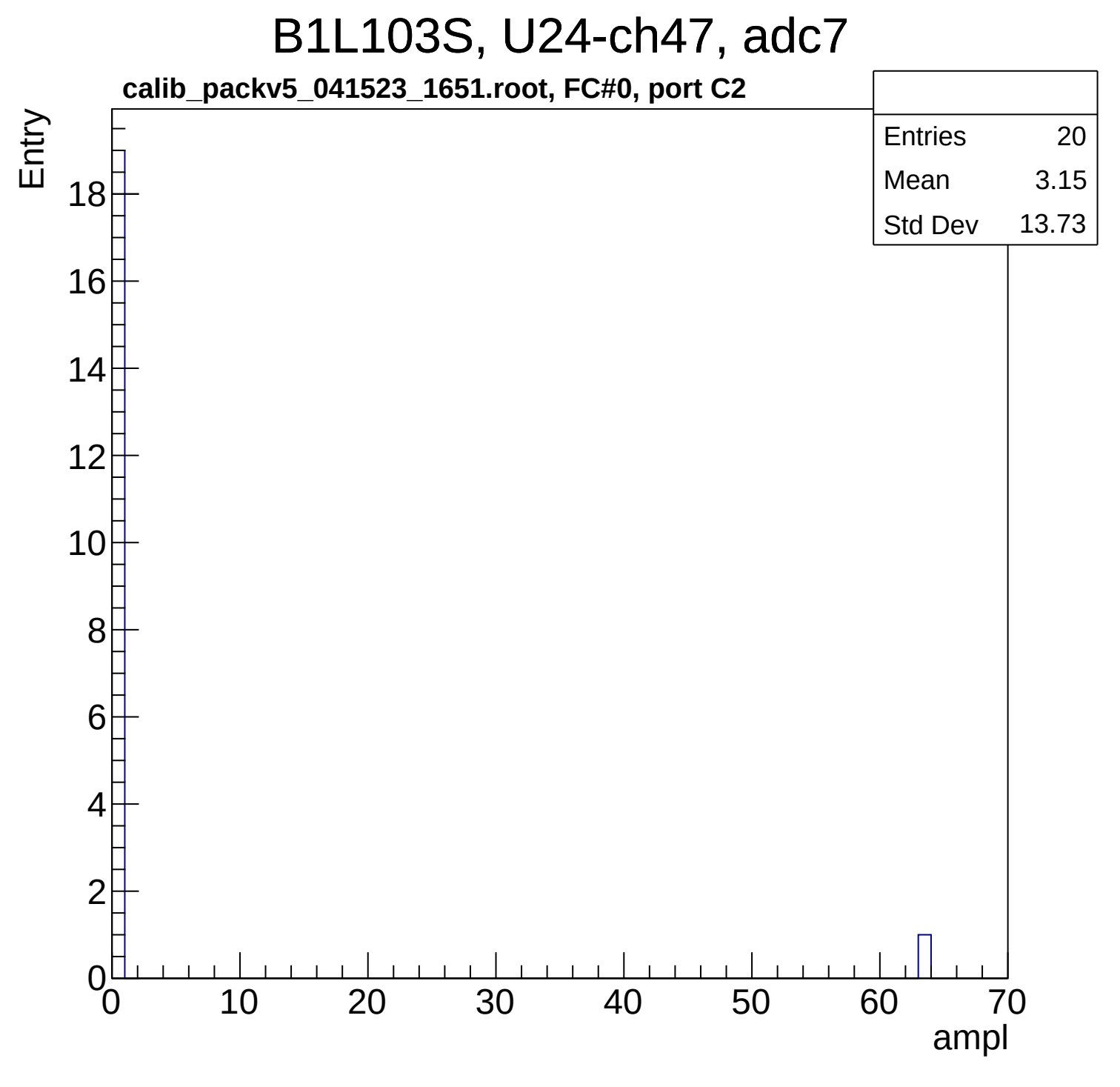
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U24-ch47, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 62.43
Std Dev 0.9035
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U24-ch47, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
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6
8
10
12
14
16
18
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10
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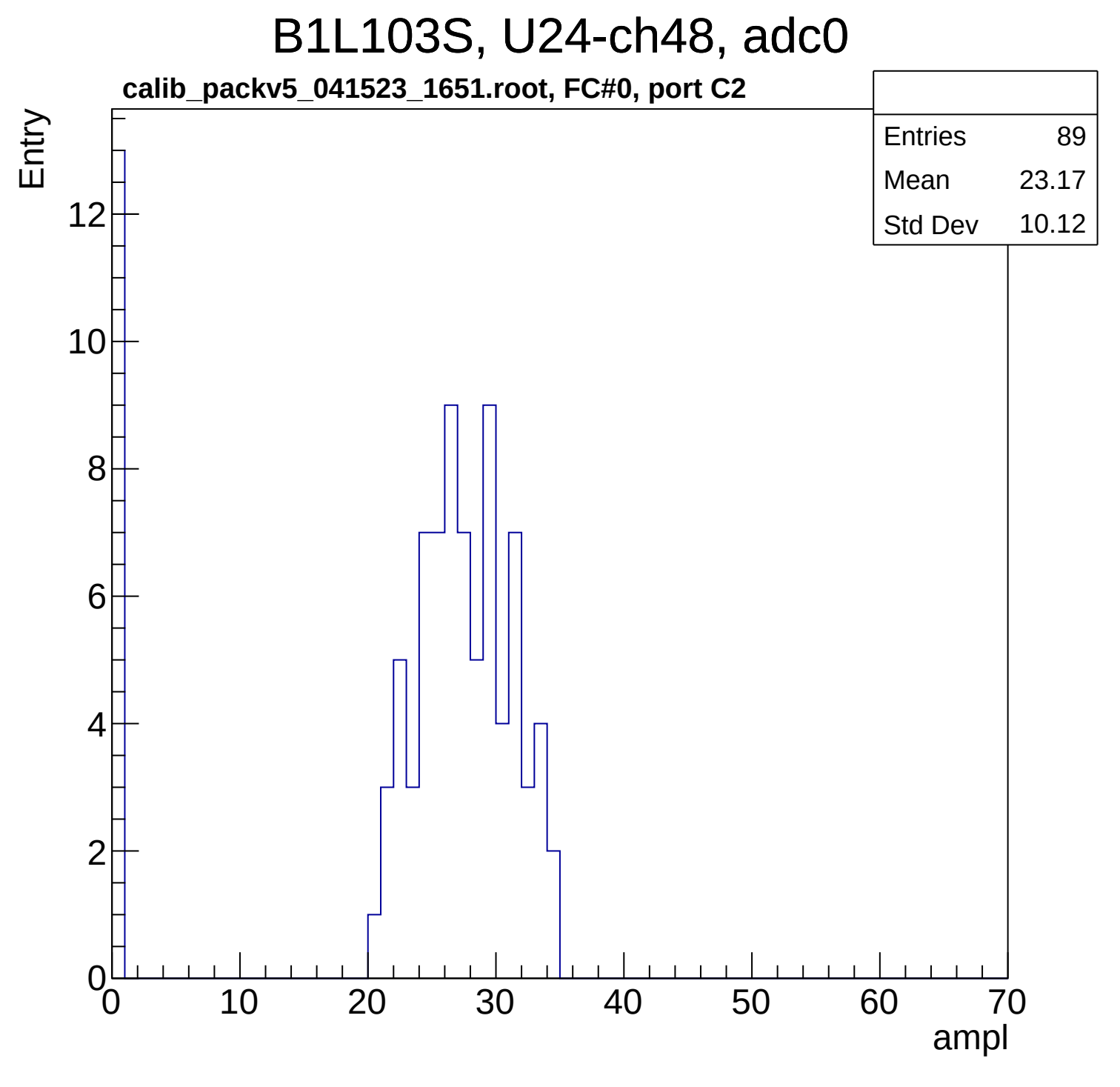
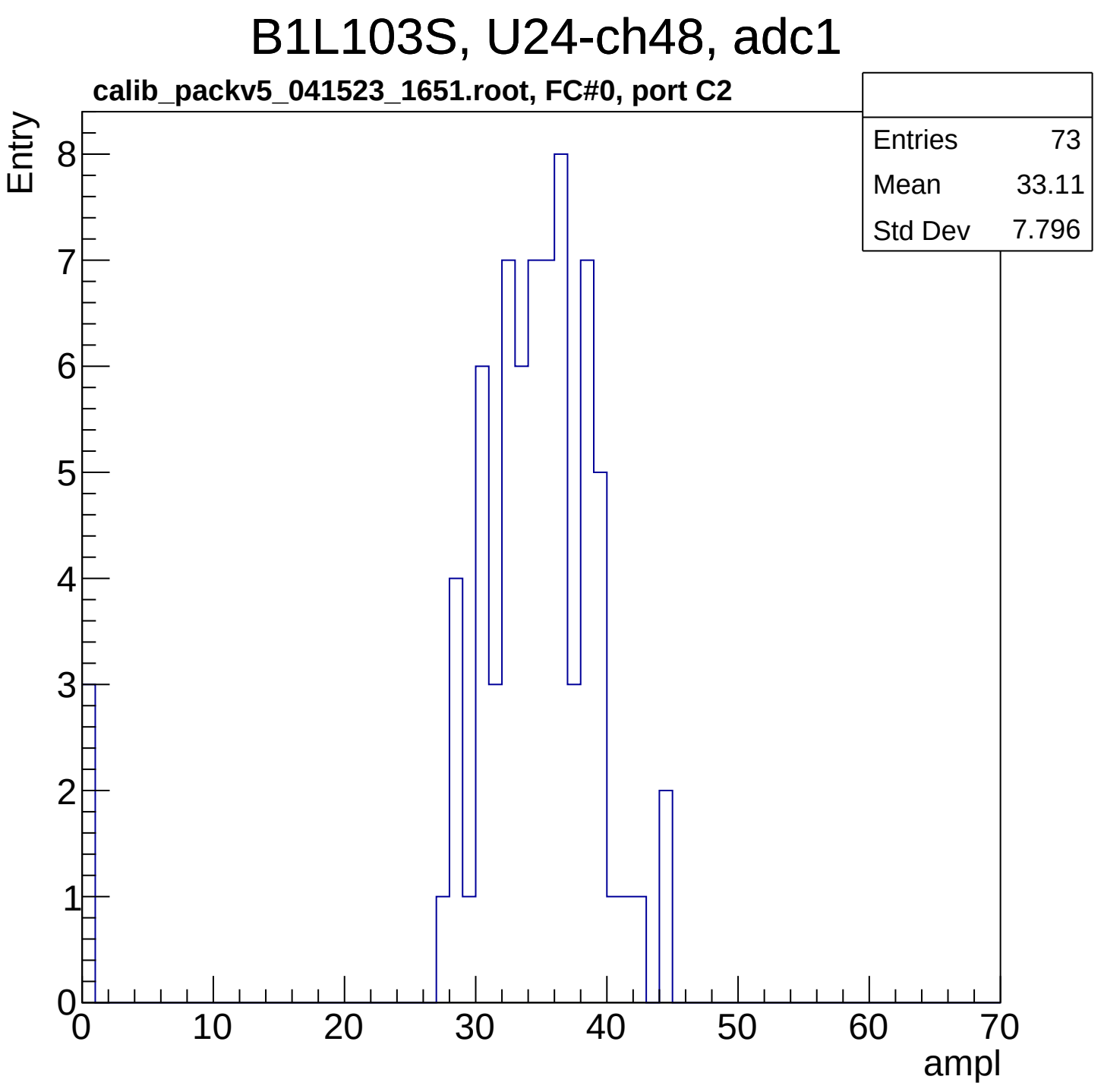
50
60
70
ampl


B1L103S, U24-ch48, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 89
Mean 23.17
Std Dev 10.12
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70


B1L103S, U24-ch48, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 33.11
Std Dev 7.796
Entry
ampl
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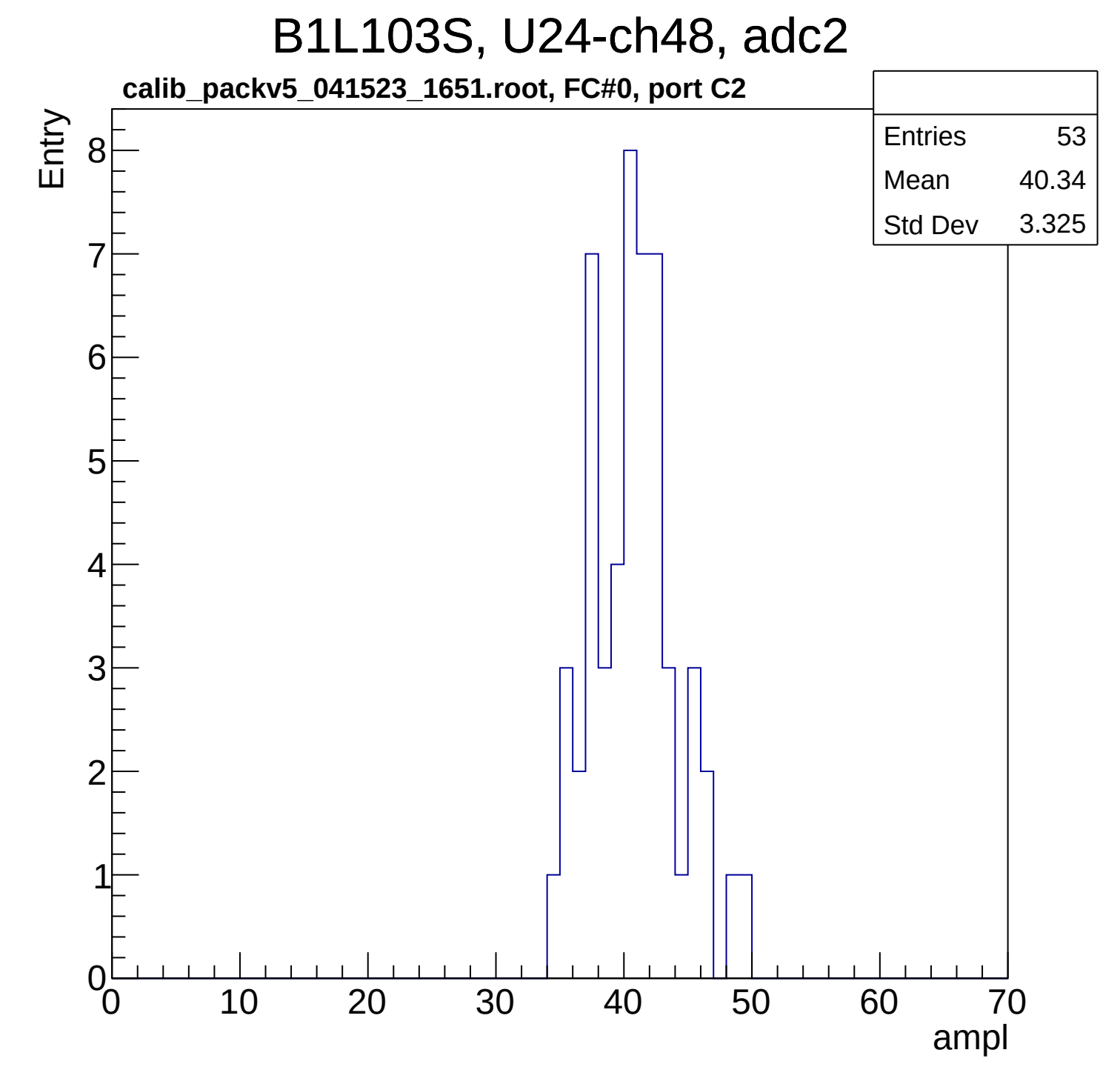
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U24-ch48, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 40.34
Std Dev 3.325
Entry
ampl
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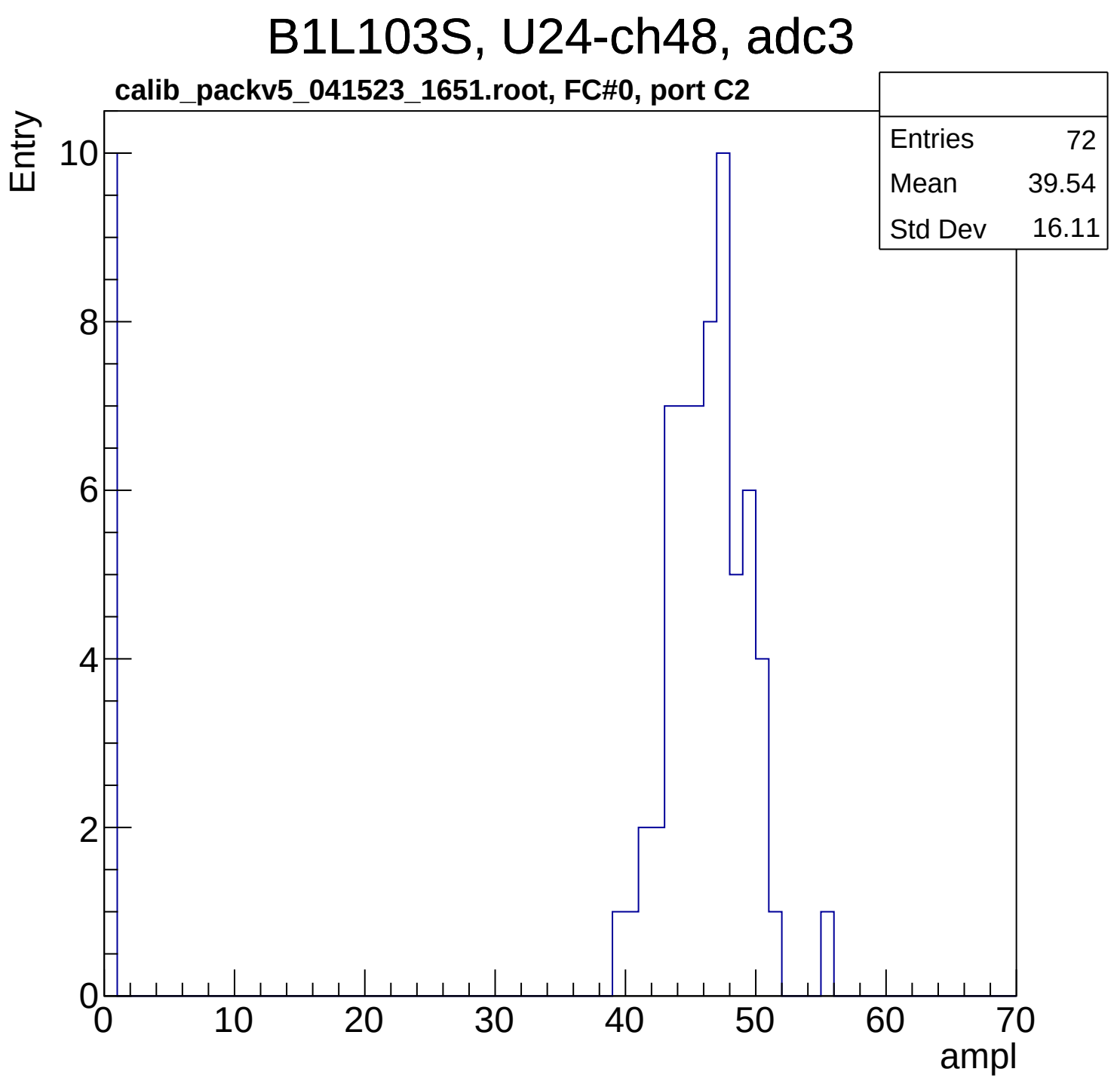
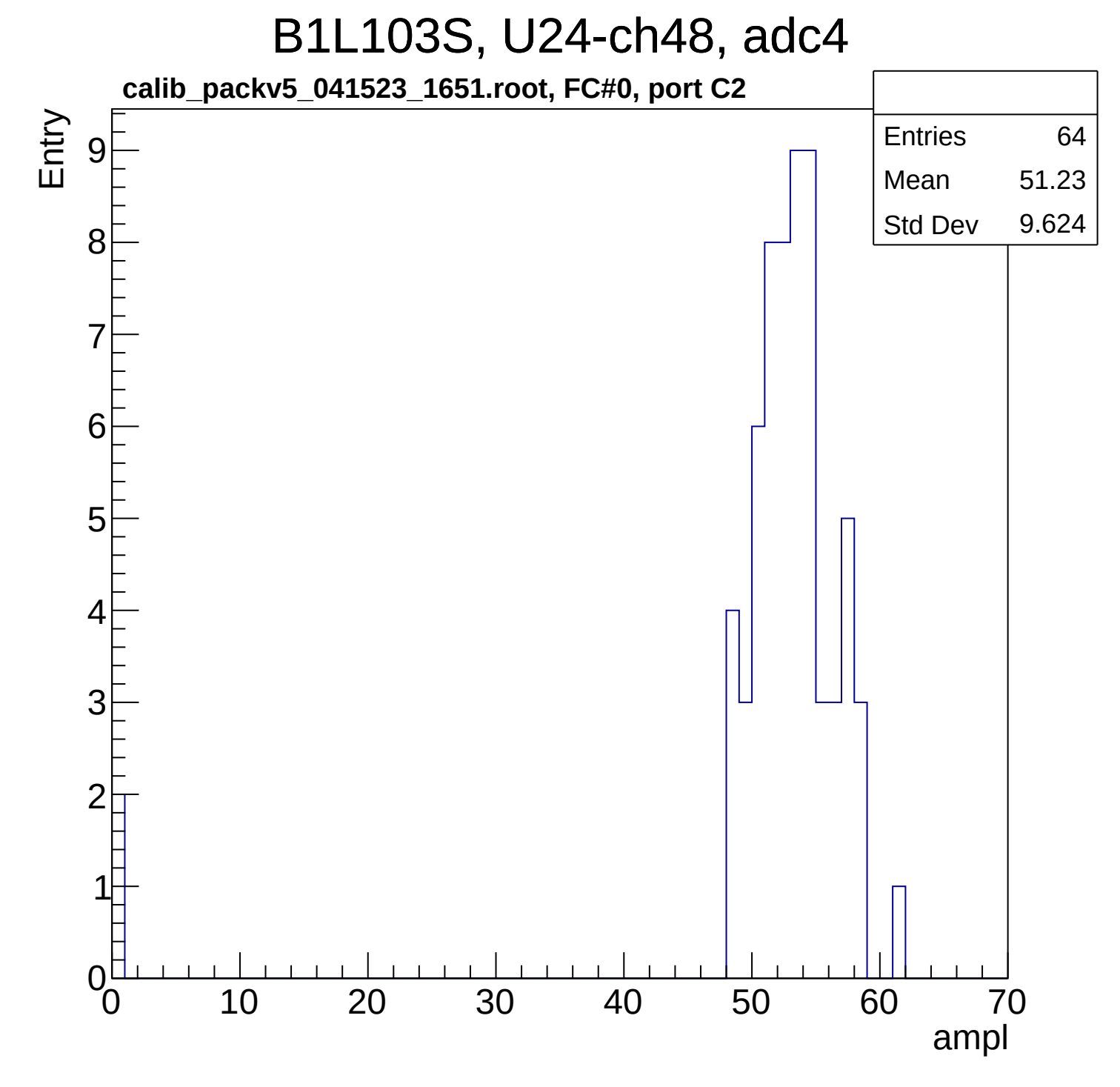
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U24-ch48, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 39.54
Std Dev 16.11
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch48, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 51.23
Std Dev 9.624
Entry
ampl
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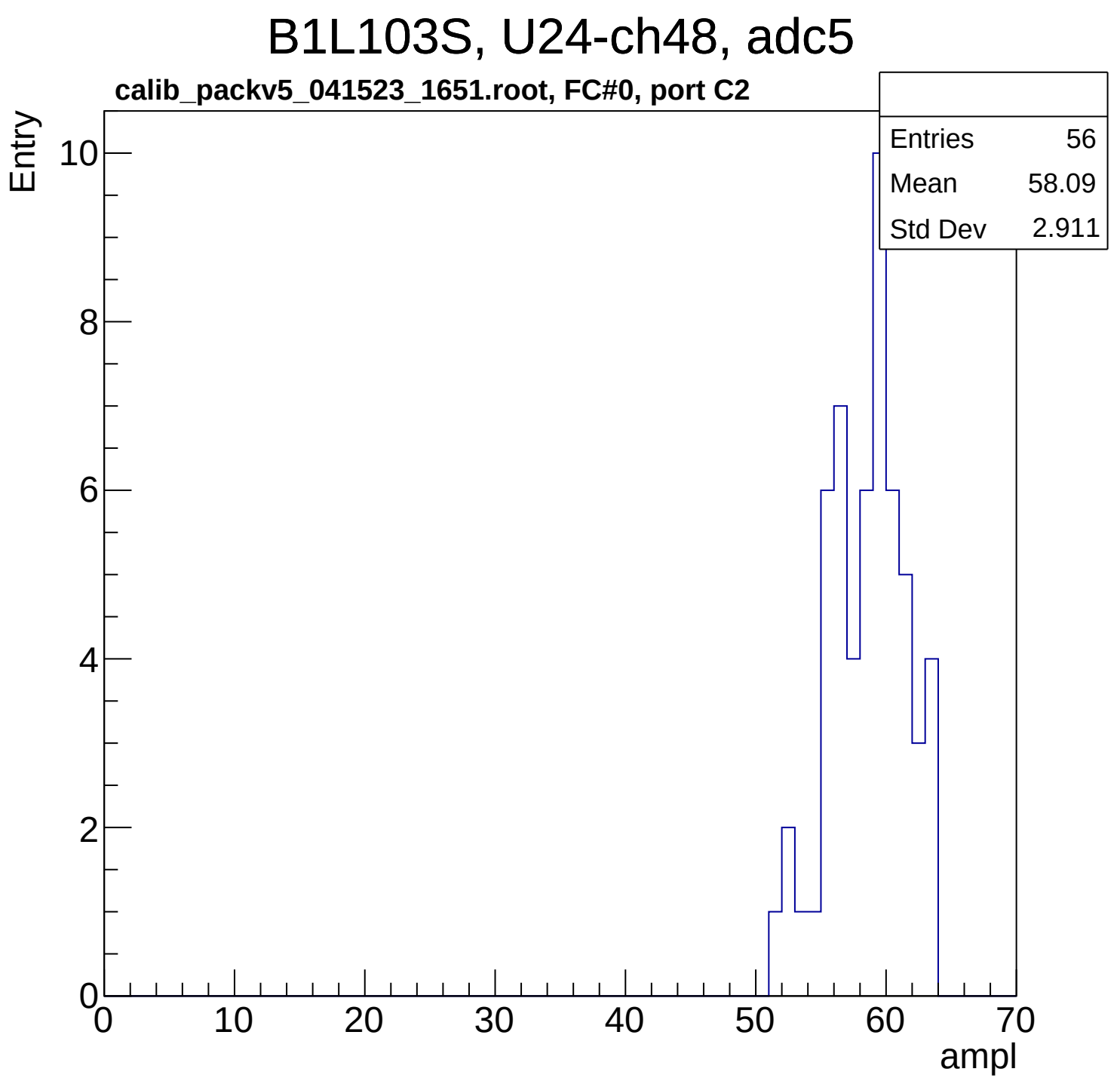
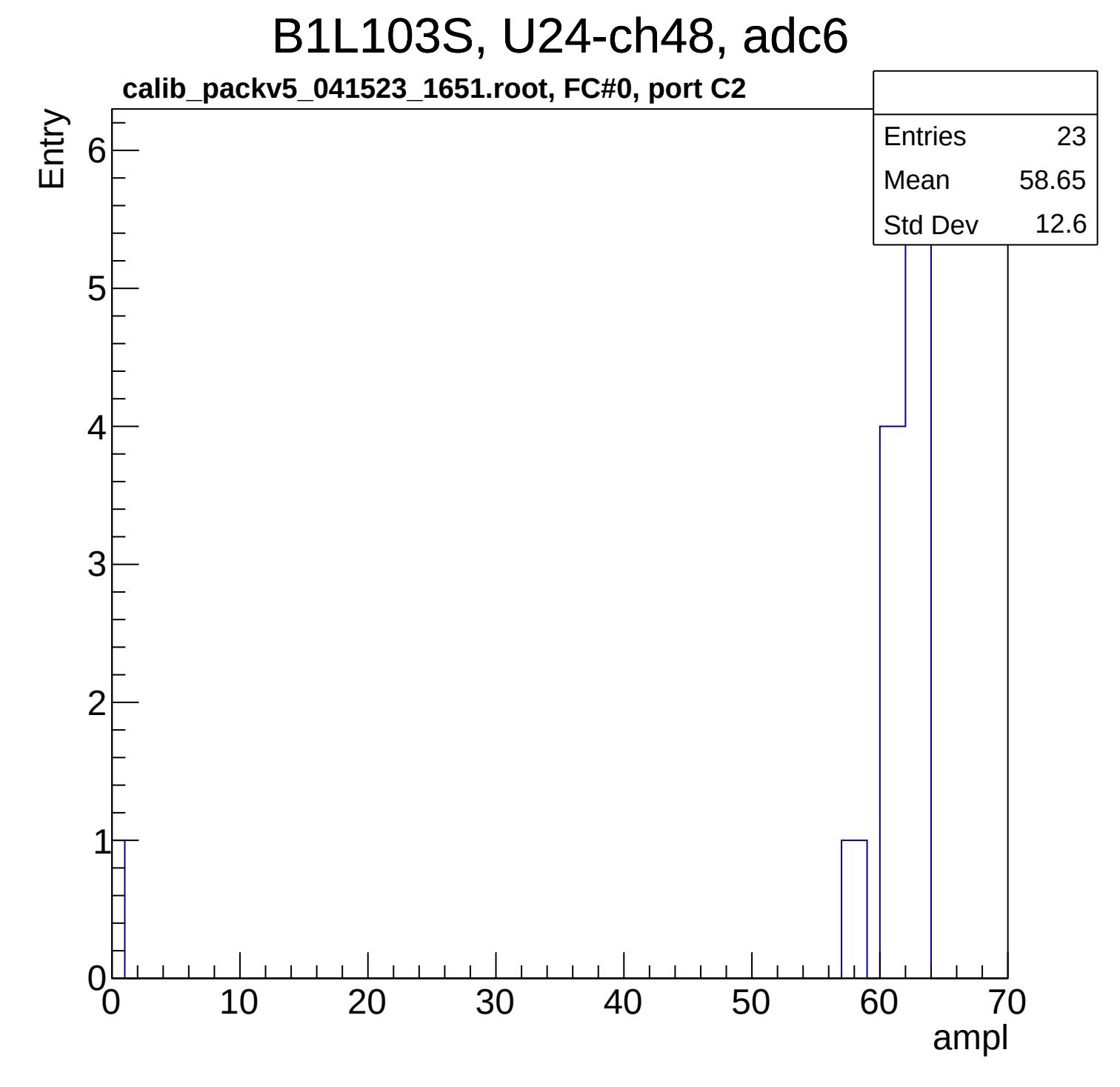
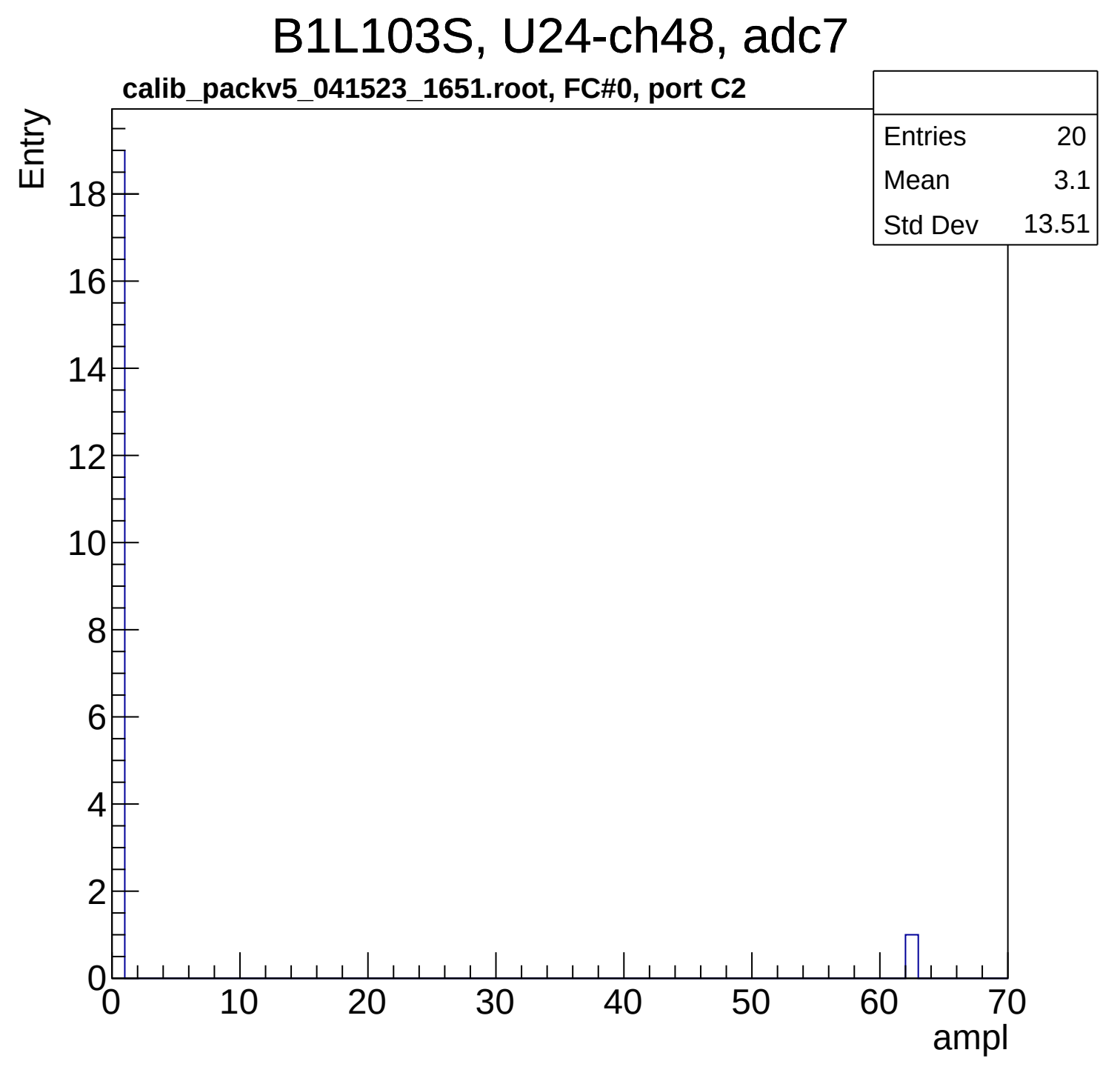
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U24-ch48, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 58.09
Std Dev 2.911
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch48, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 23
Mean 58.65
Std Dev 12.6
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U24-ch48, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.1
Std Dev 13.51
Entry
0
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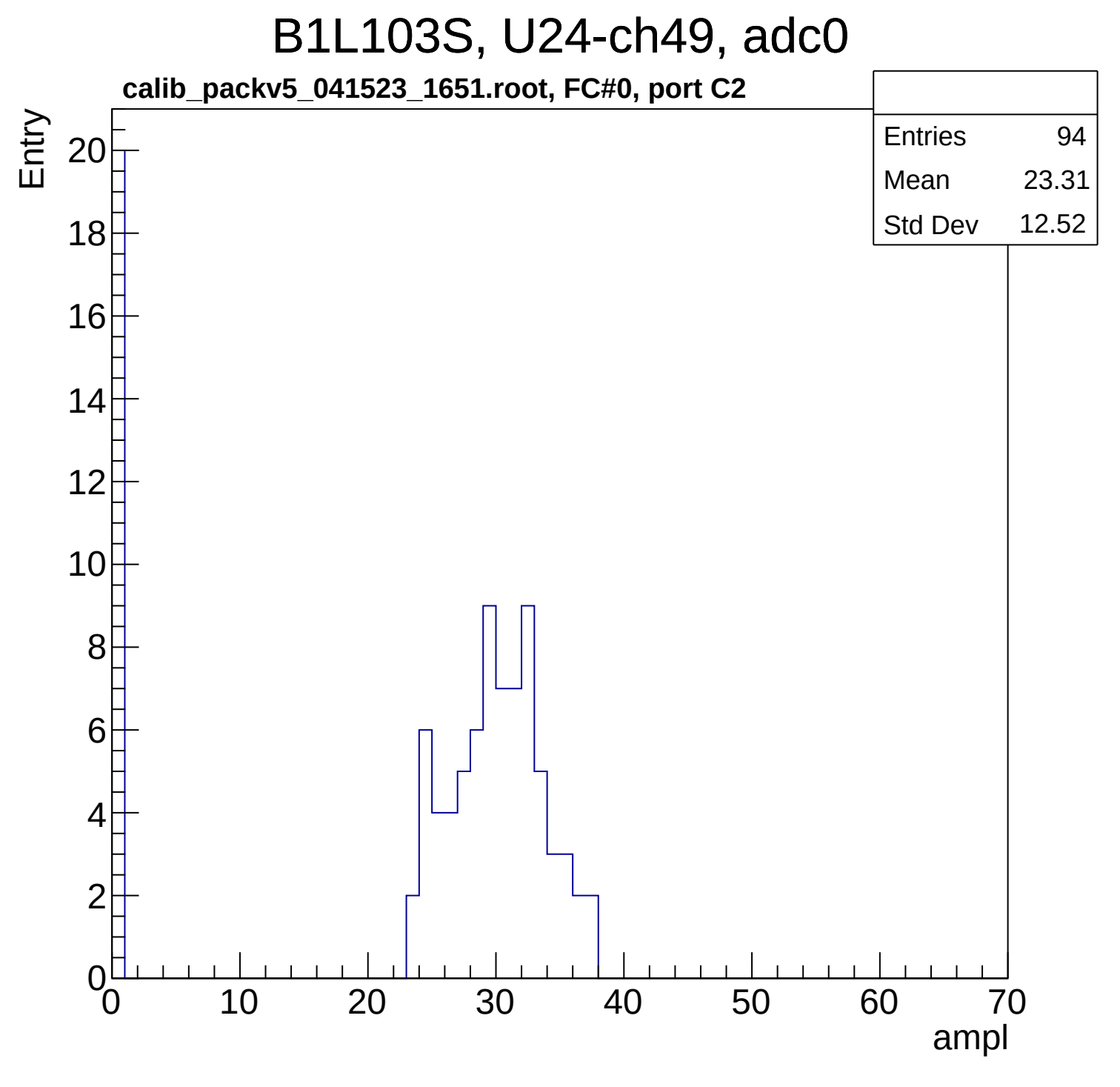
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch49, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 94
Mean 23.31
Std Dev 12.52
Entry
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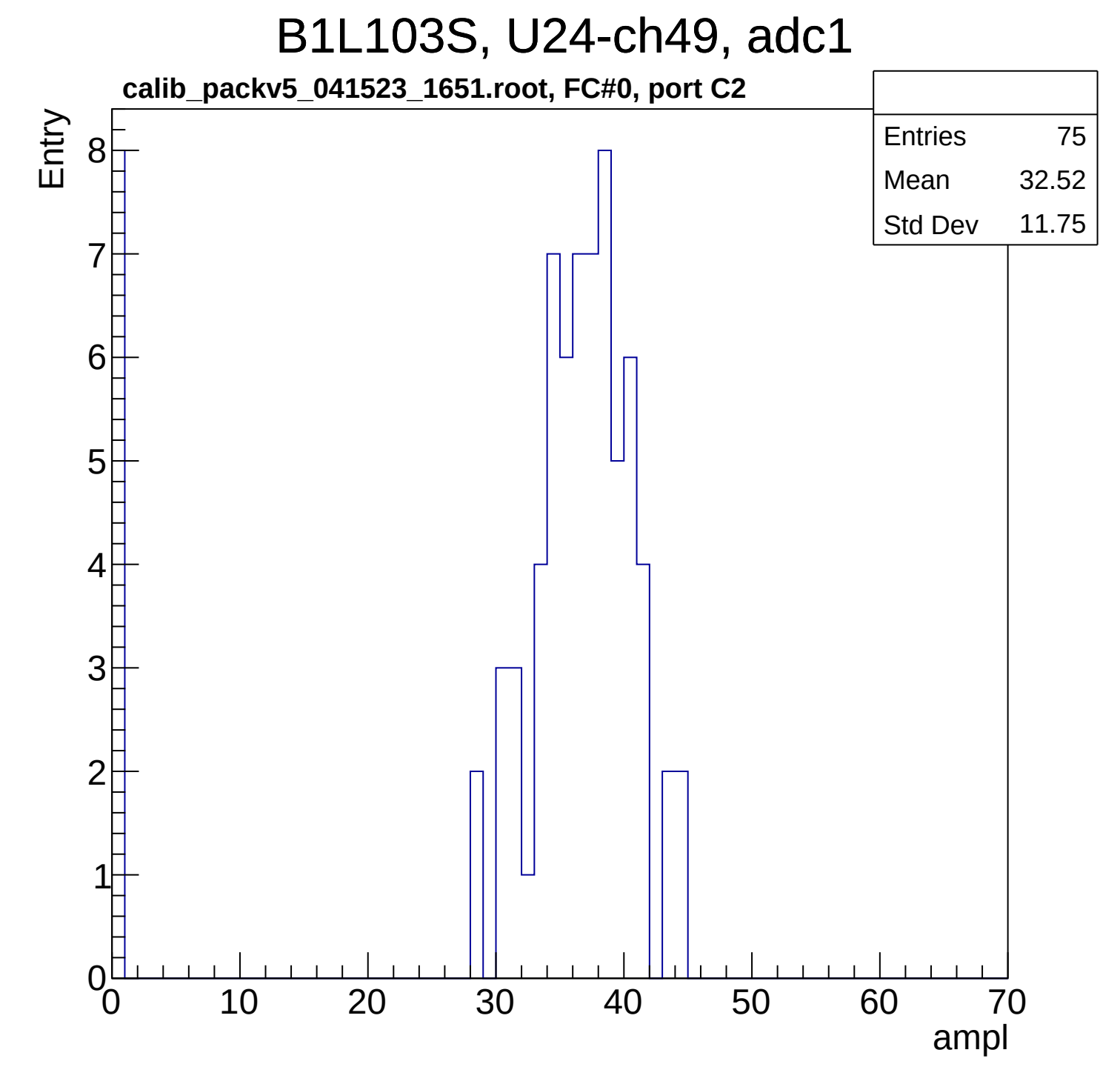
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch49, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 32.52
Std Dev 11.75
Entry
ampl
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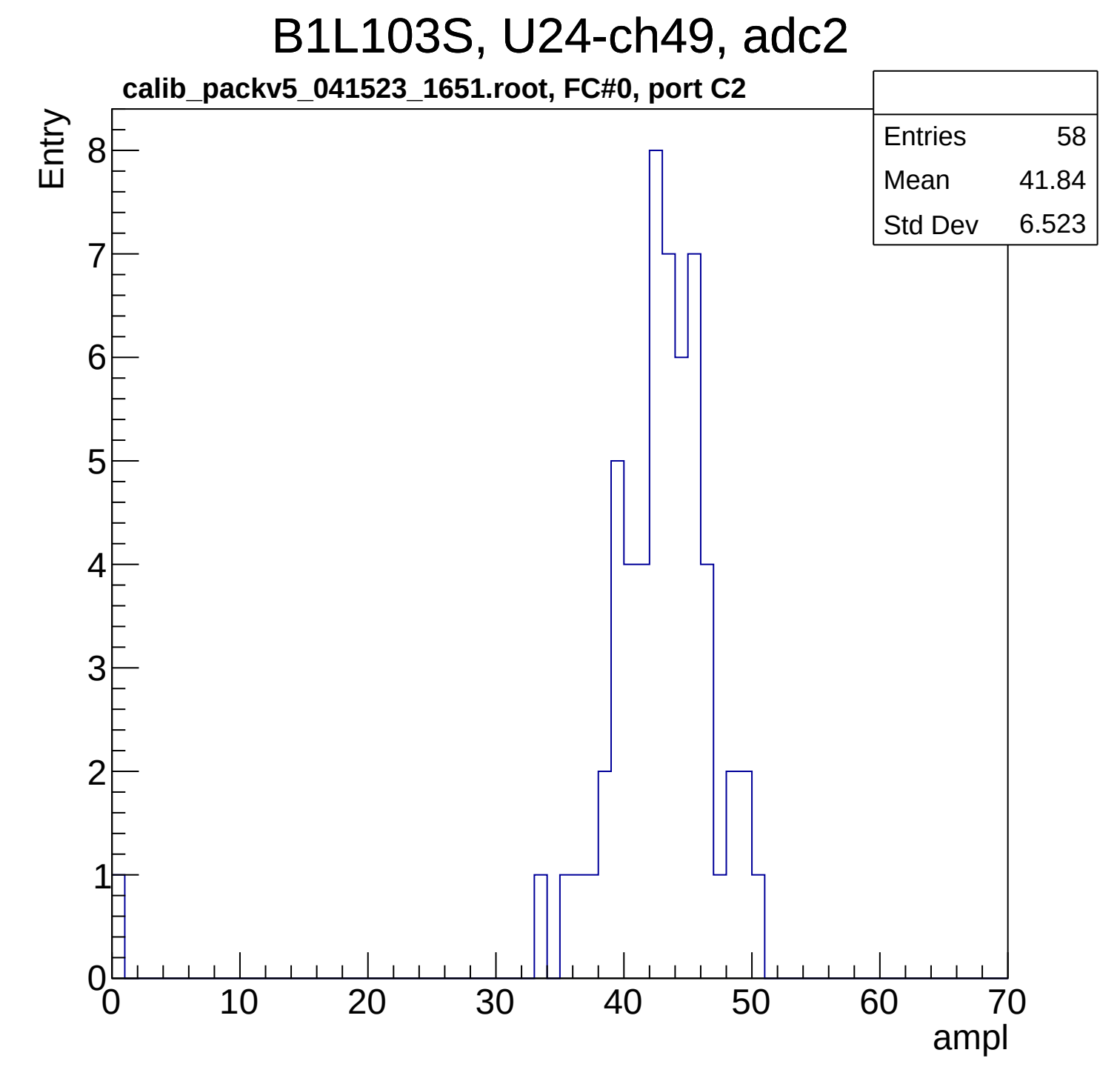
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U24-ch49, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 41.84
Std Dev 6.523
Entry
ampl
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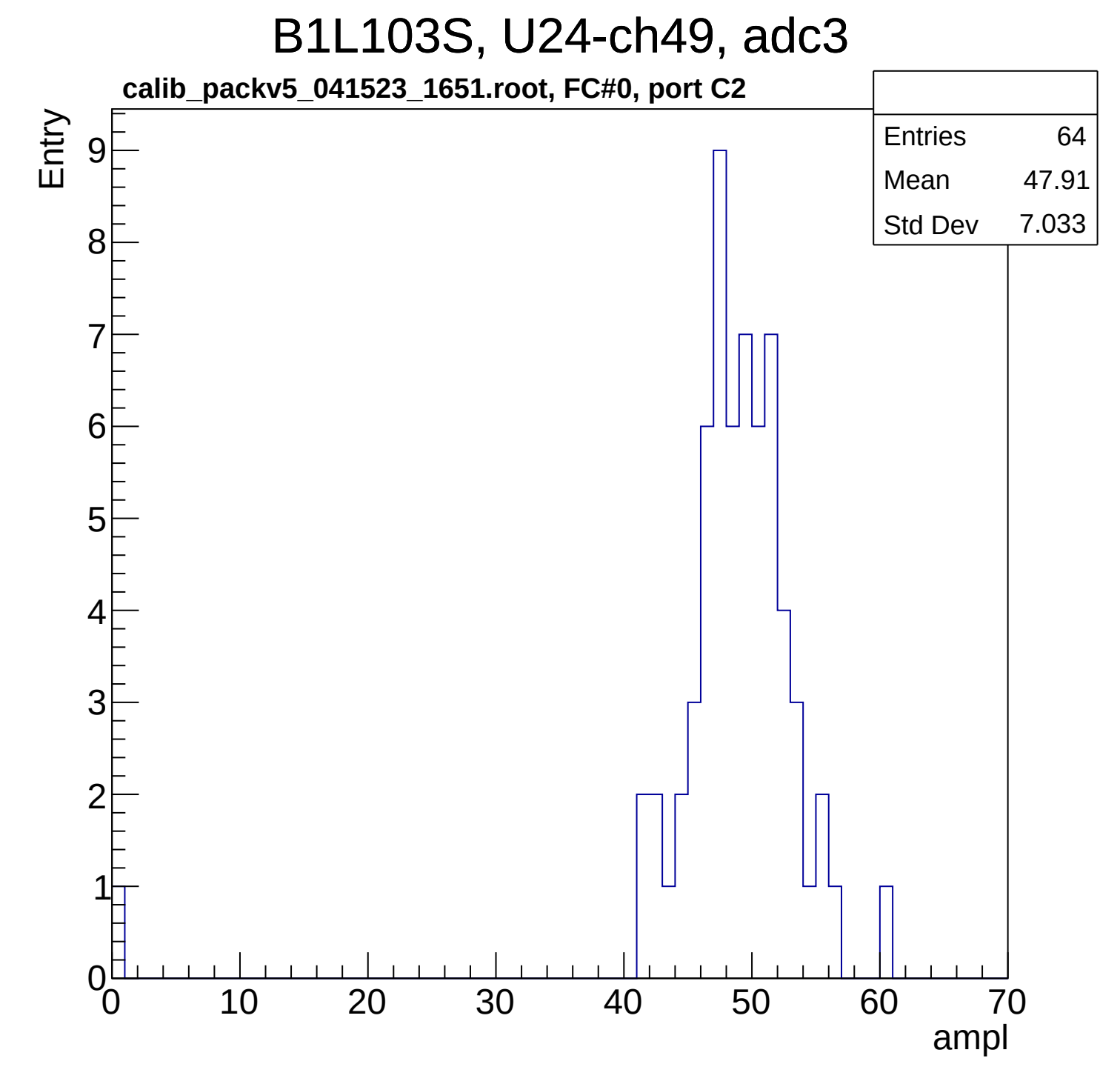
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U24-ch49, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 47.91
Std Dev 7.033
Entry
ampl
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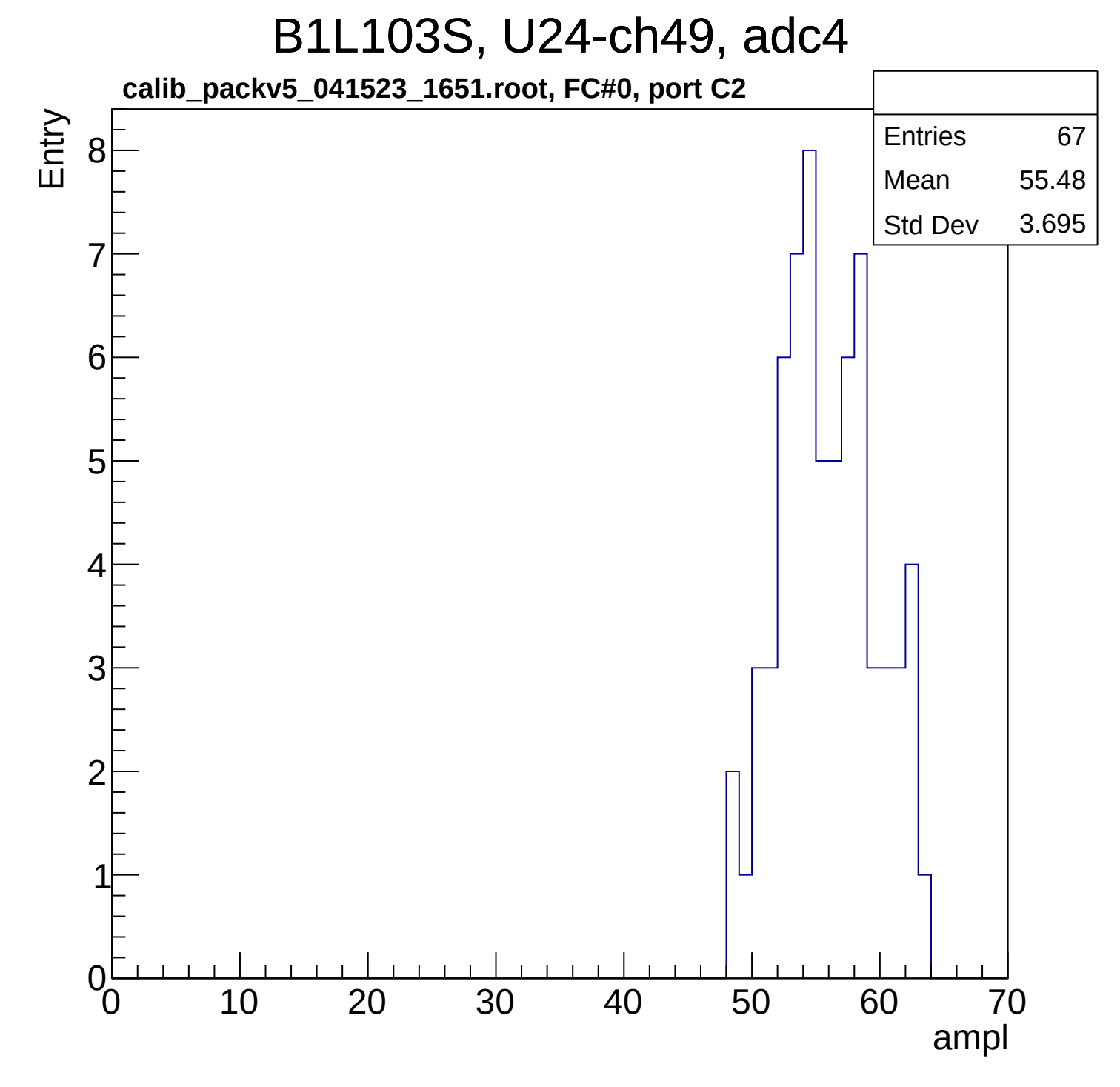
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U24-ch49, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 55.48
Std Dev 3.695
Entry
ampl
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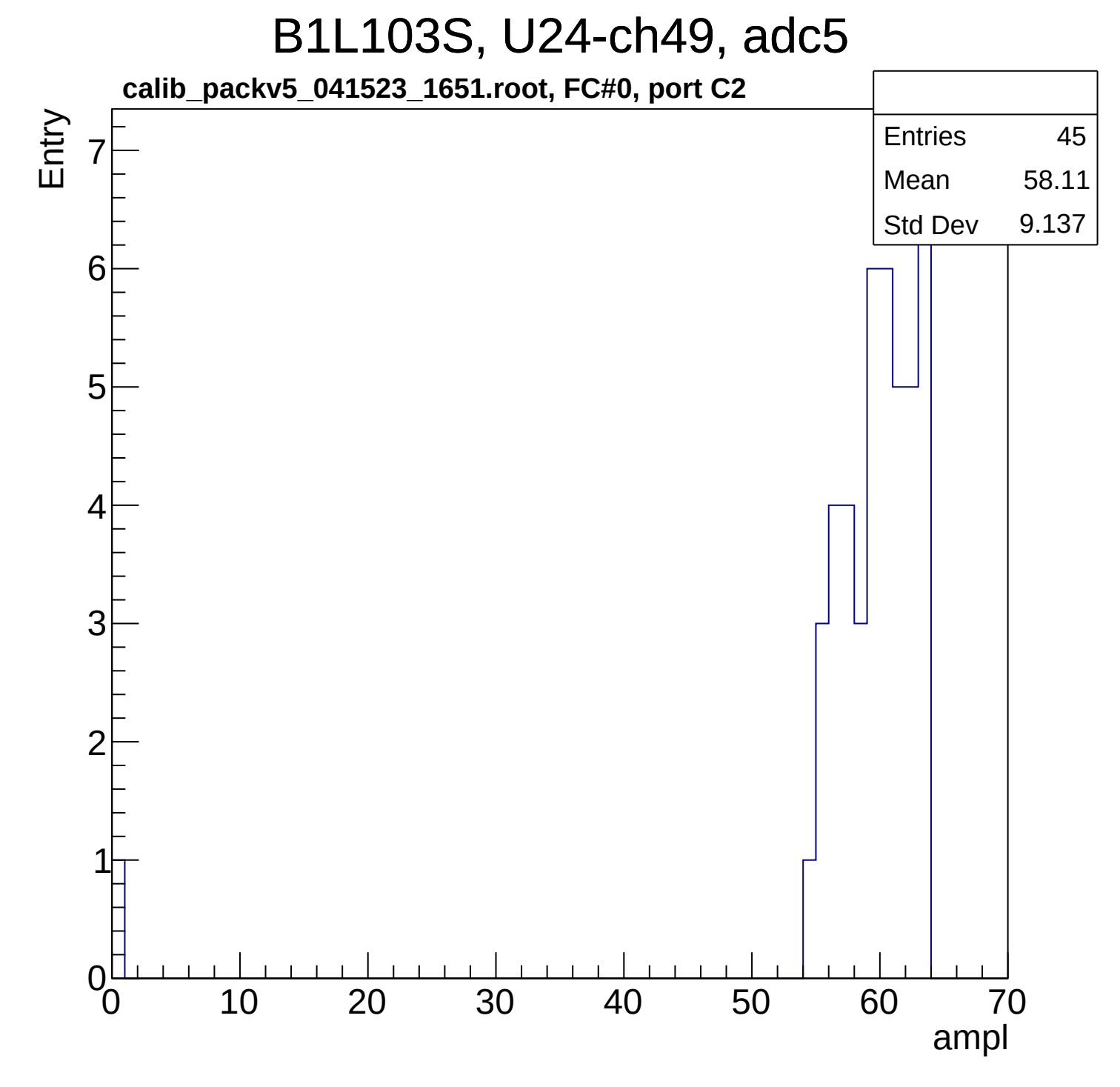
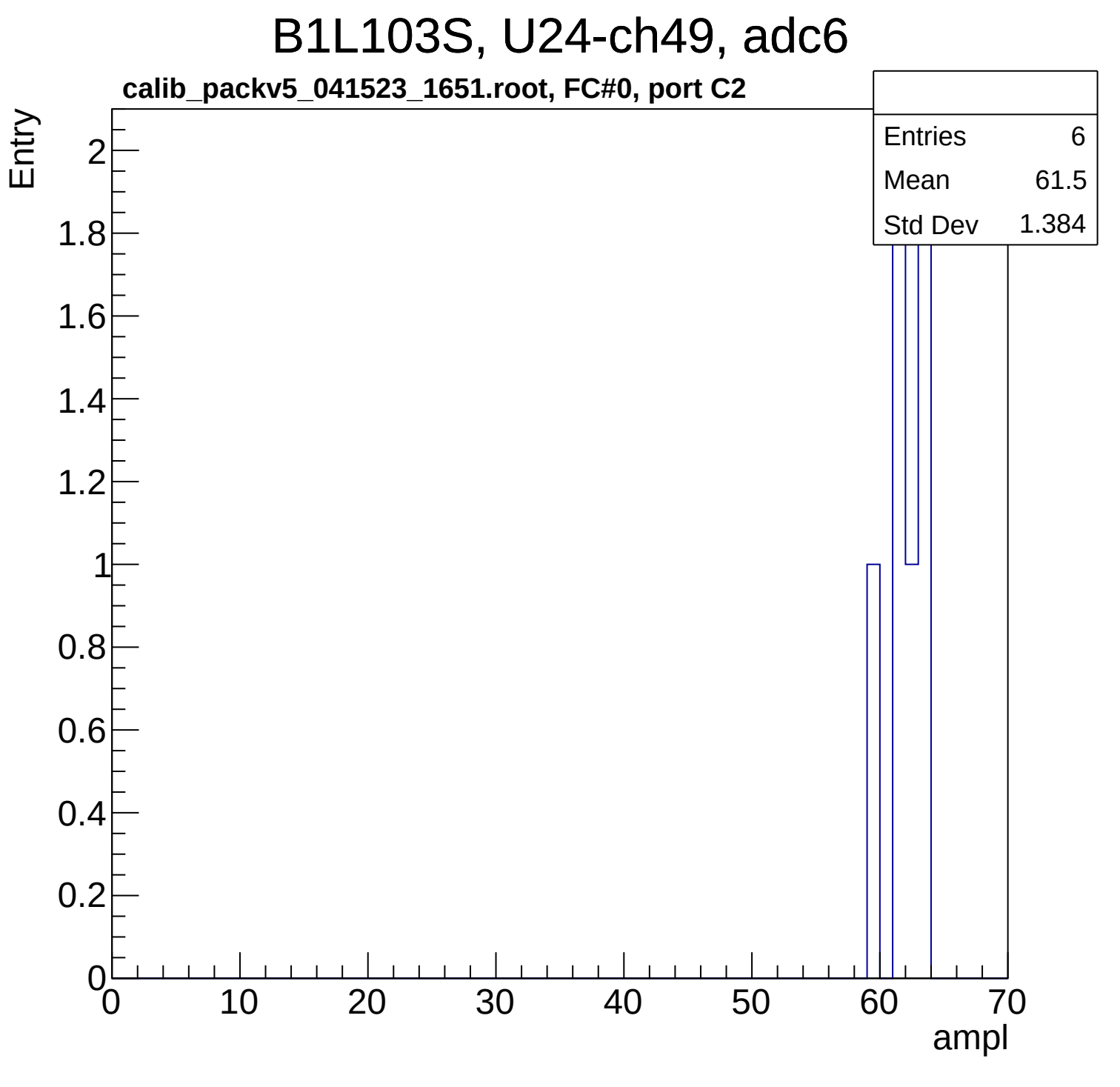
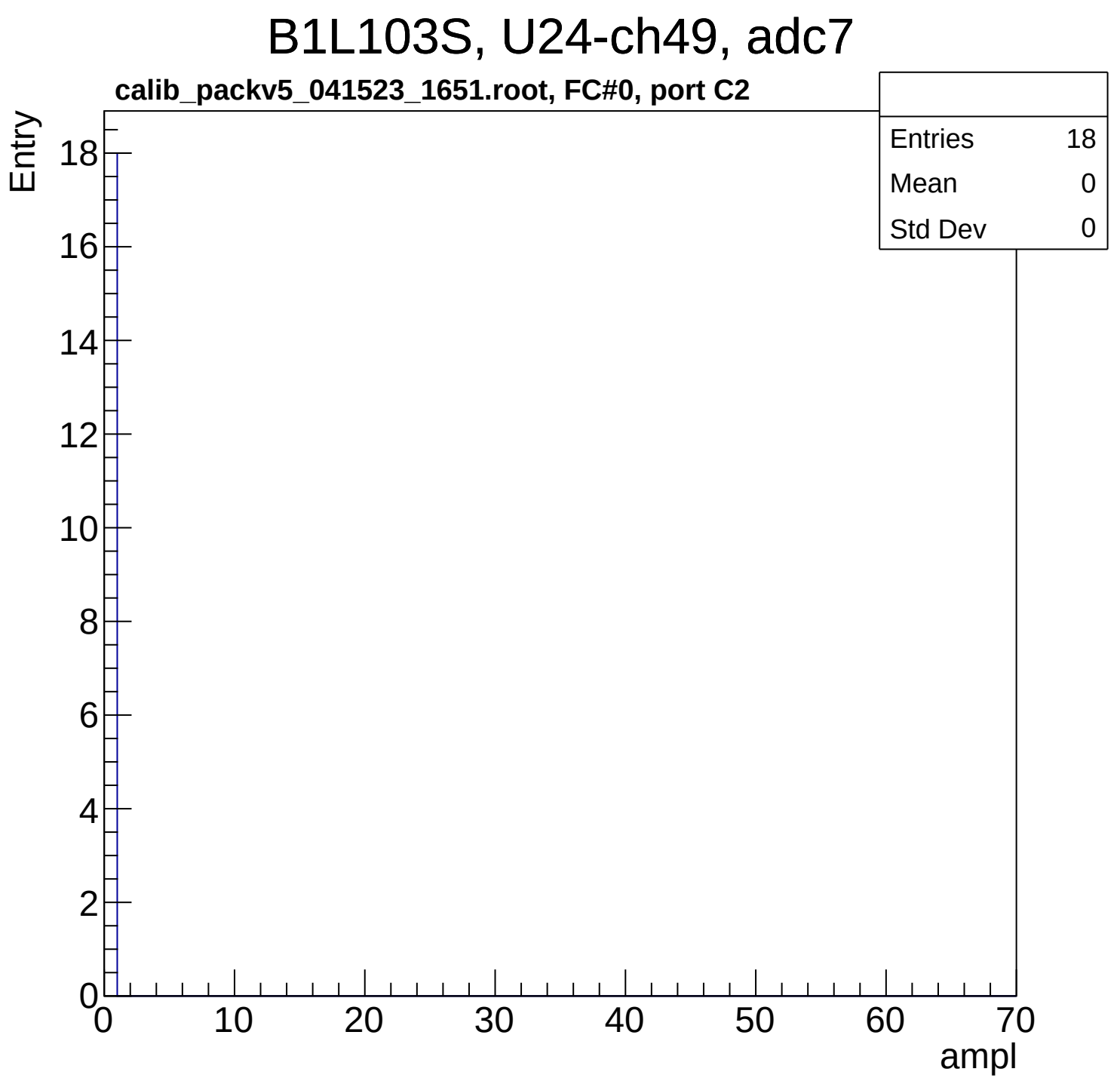
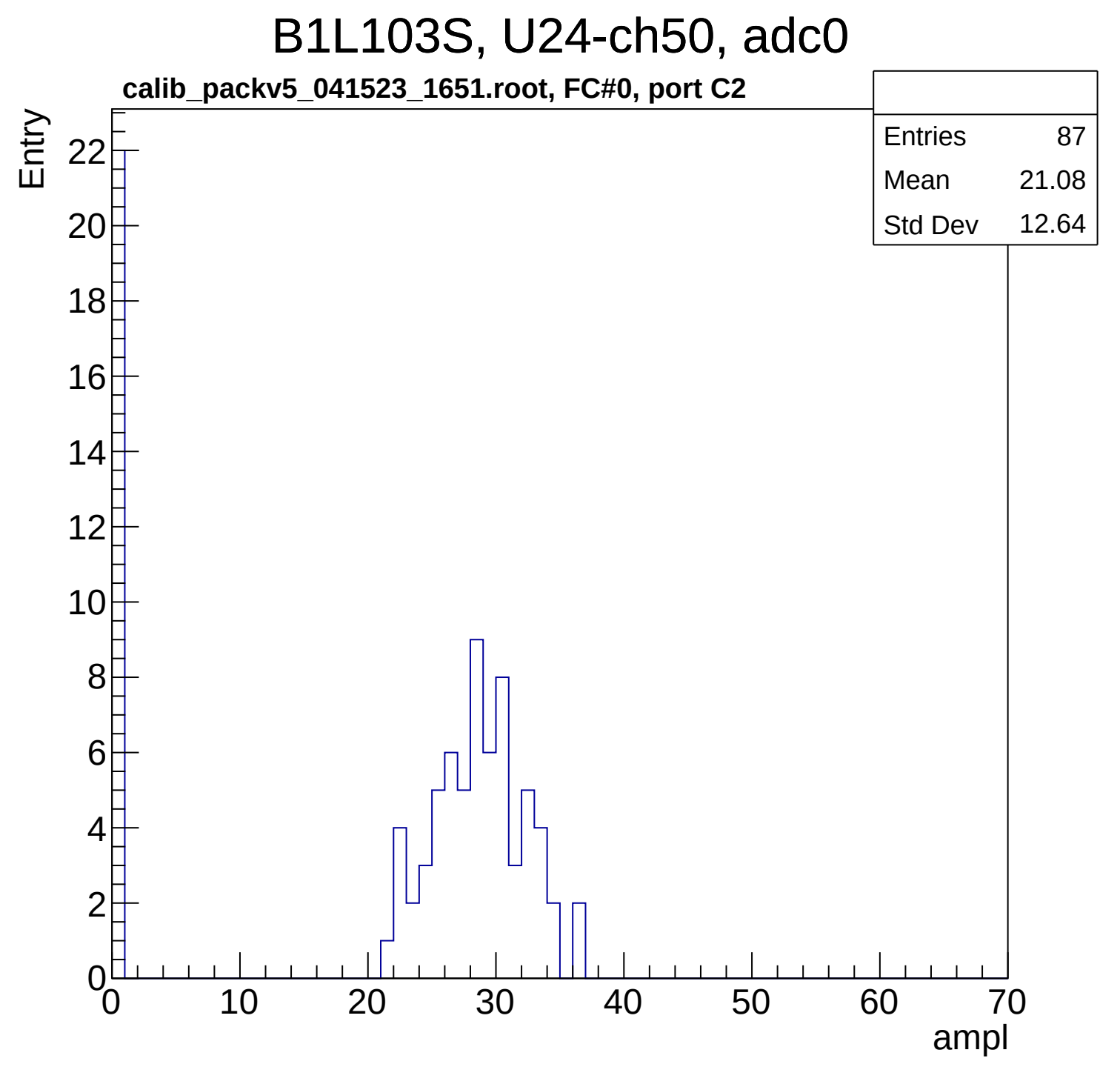
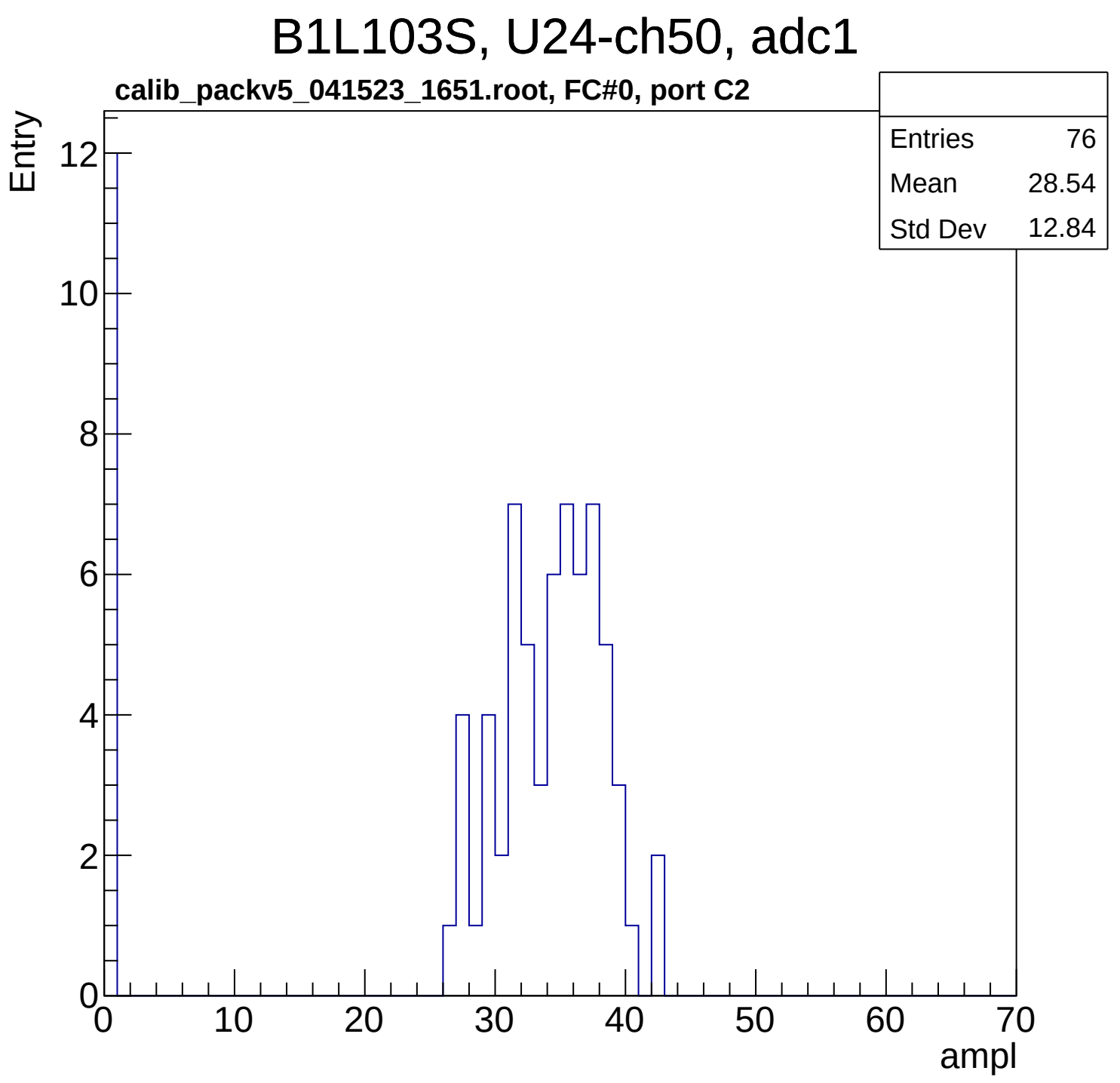
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

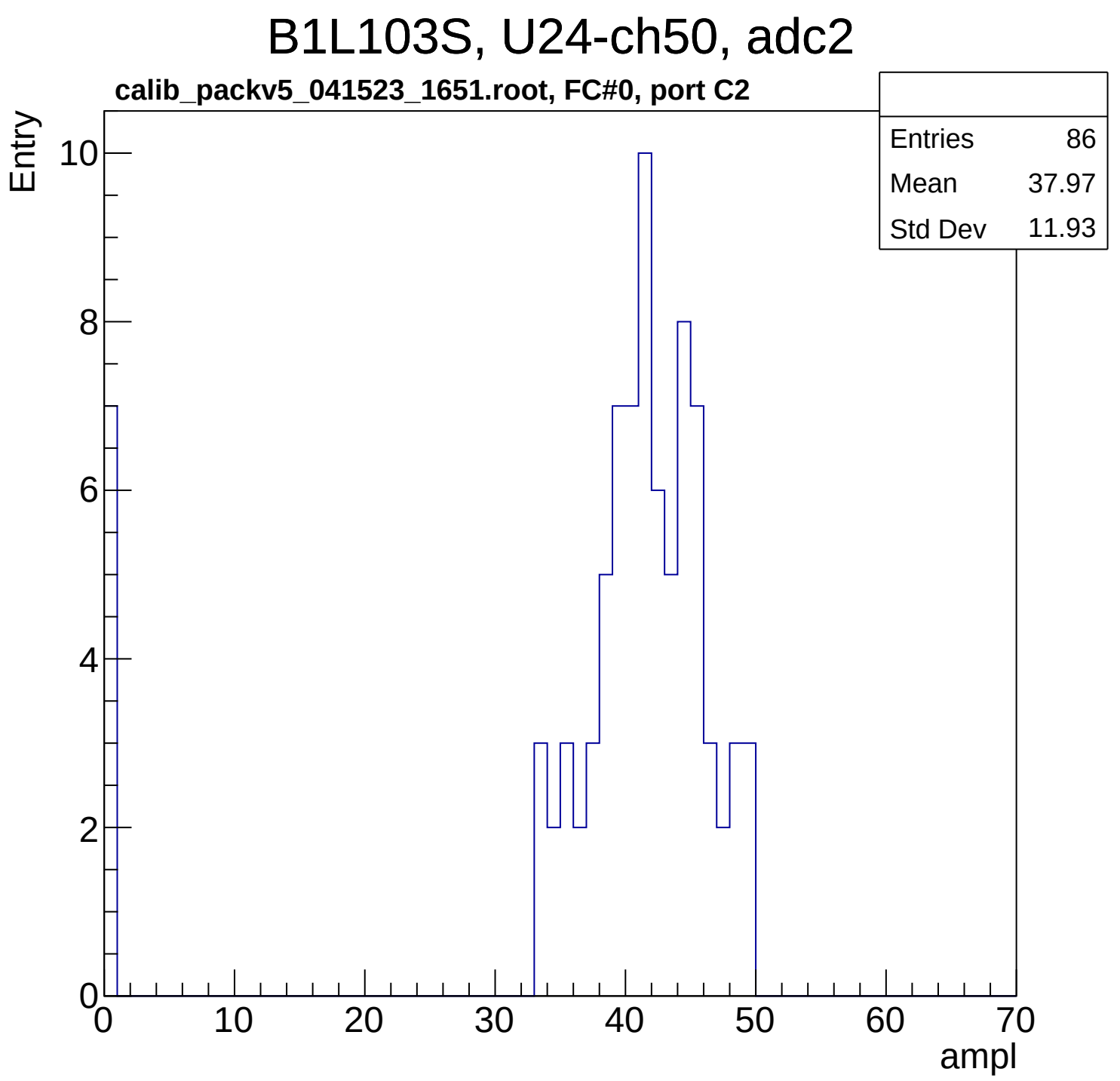

B1L103S, U24-ch49, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 58.11
Std Dev 9.137
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

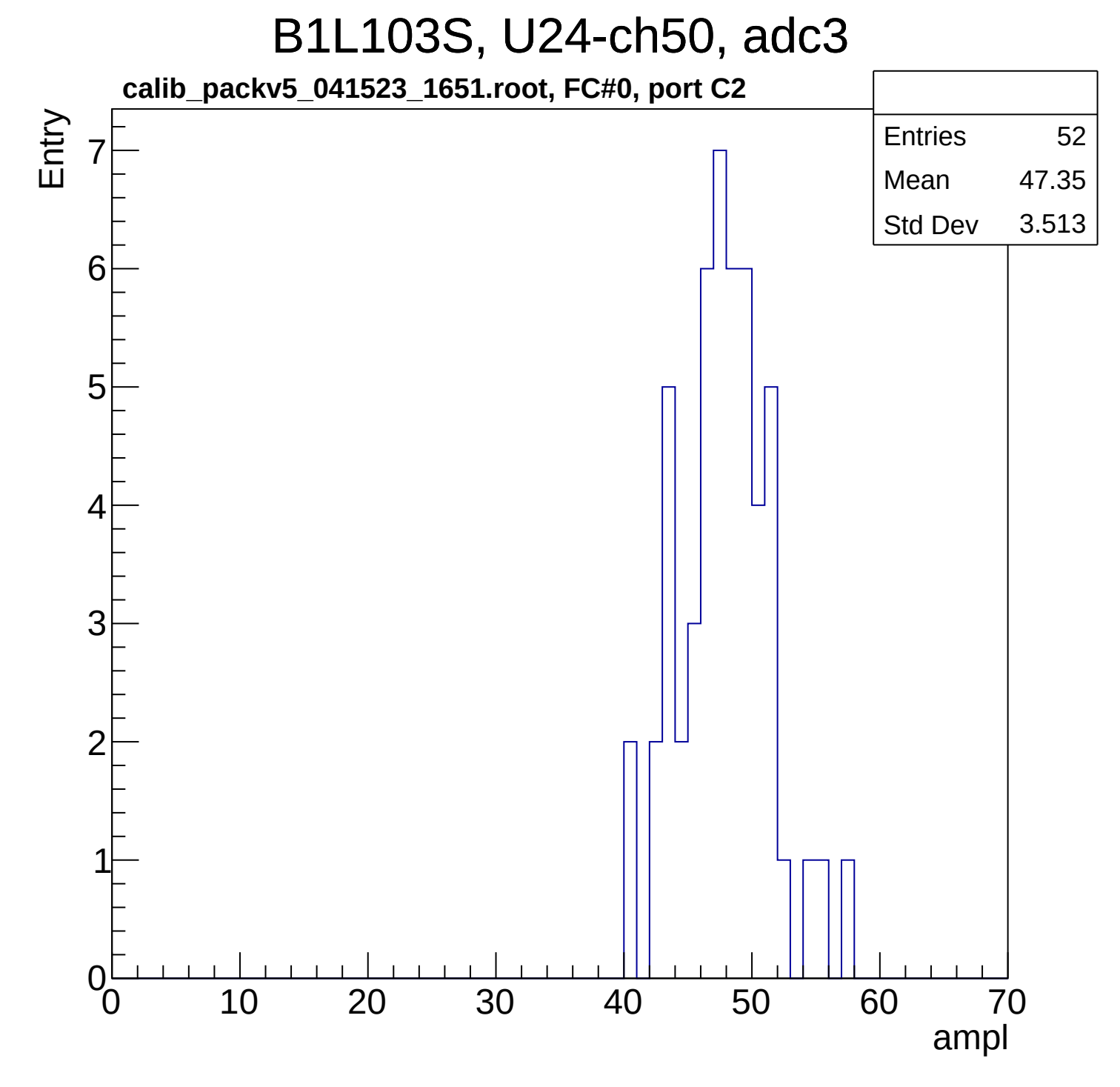

B1L103S, U24-ch49, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 61.5
Std Dev 1.384
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U24-ch49, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch50, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 87
Mean 21.08
Std Dev 12.64
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
22
0
10
20
30
40
50
60
70


B1L103S, U24-ch50, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 28.54
Std Dev 12.84
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch50, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 37.97
Std Dev 11.93
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U24-ch50, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 47.35
Std Dev 3.513
Entry
ampl
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4
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60
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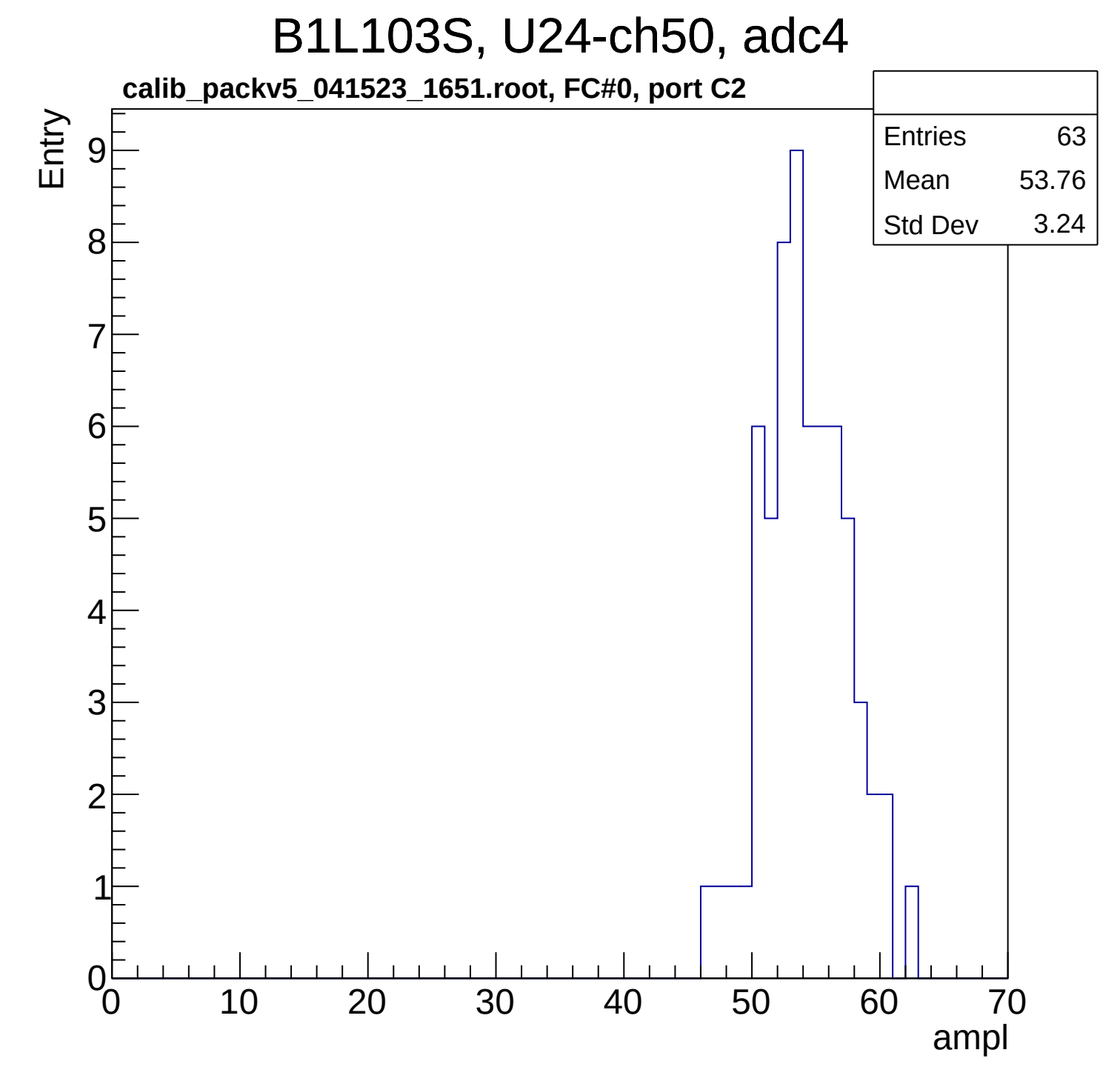
B1L103S, U24-ch50, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 53.76
Std Dev 3.24
Entry
ampl
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3
4
5
6
7
8
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0
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40
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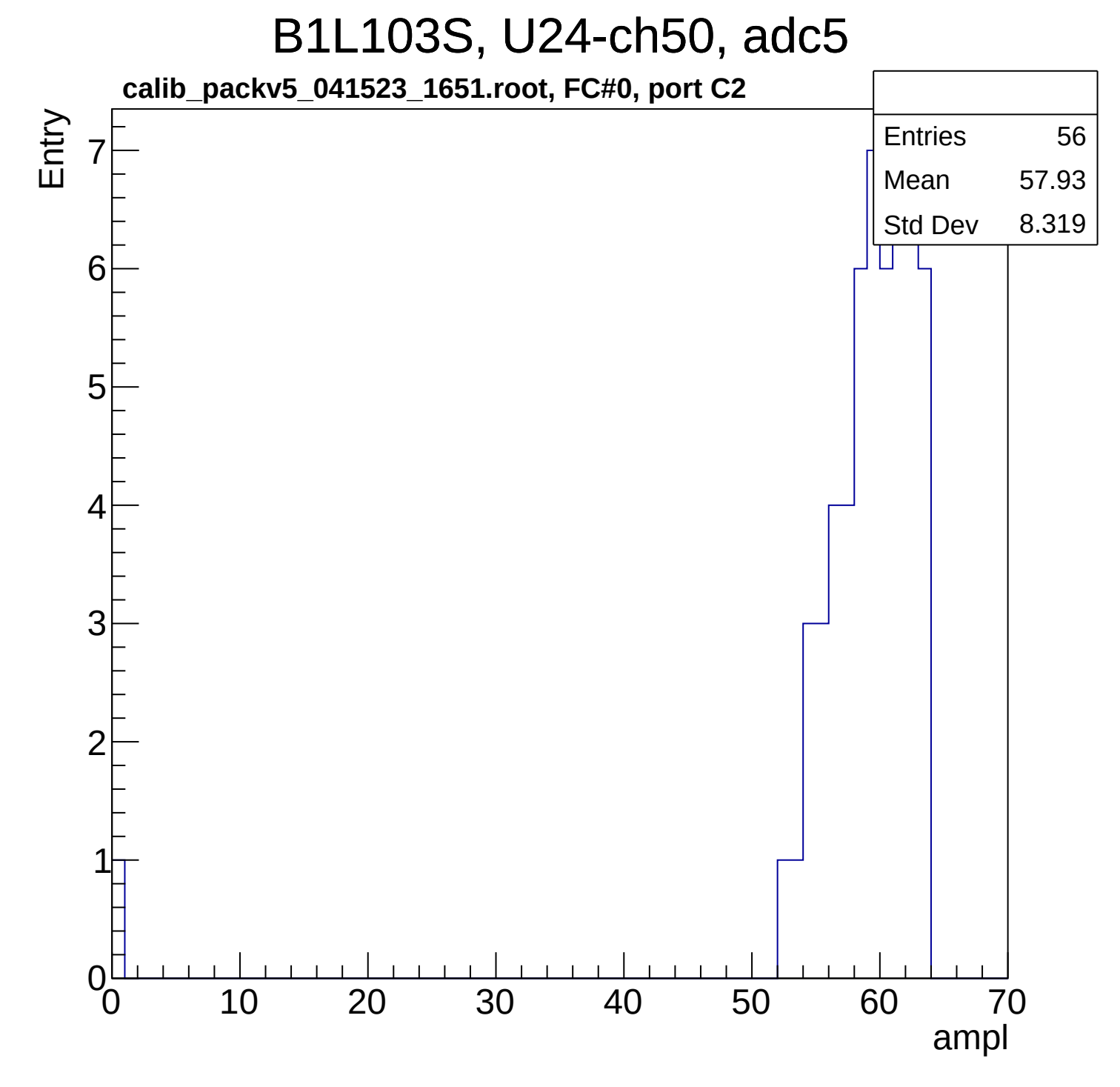
B1L103S, U24-ch50, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 57.93
Std Dev 8.319
Entry
ampl
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4
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0
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40
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60
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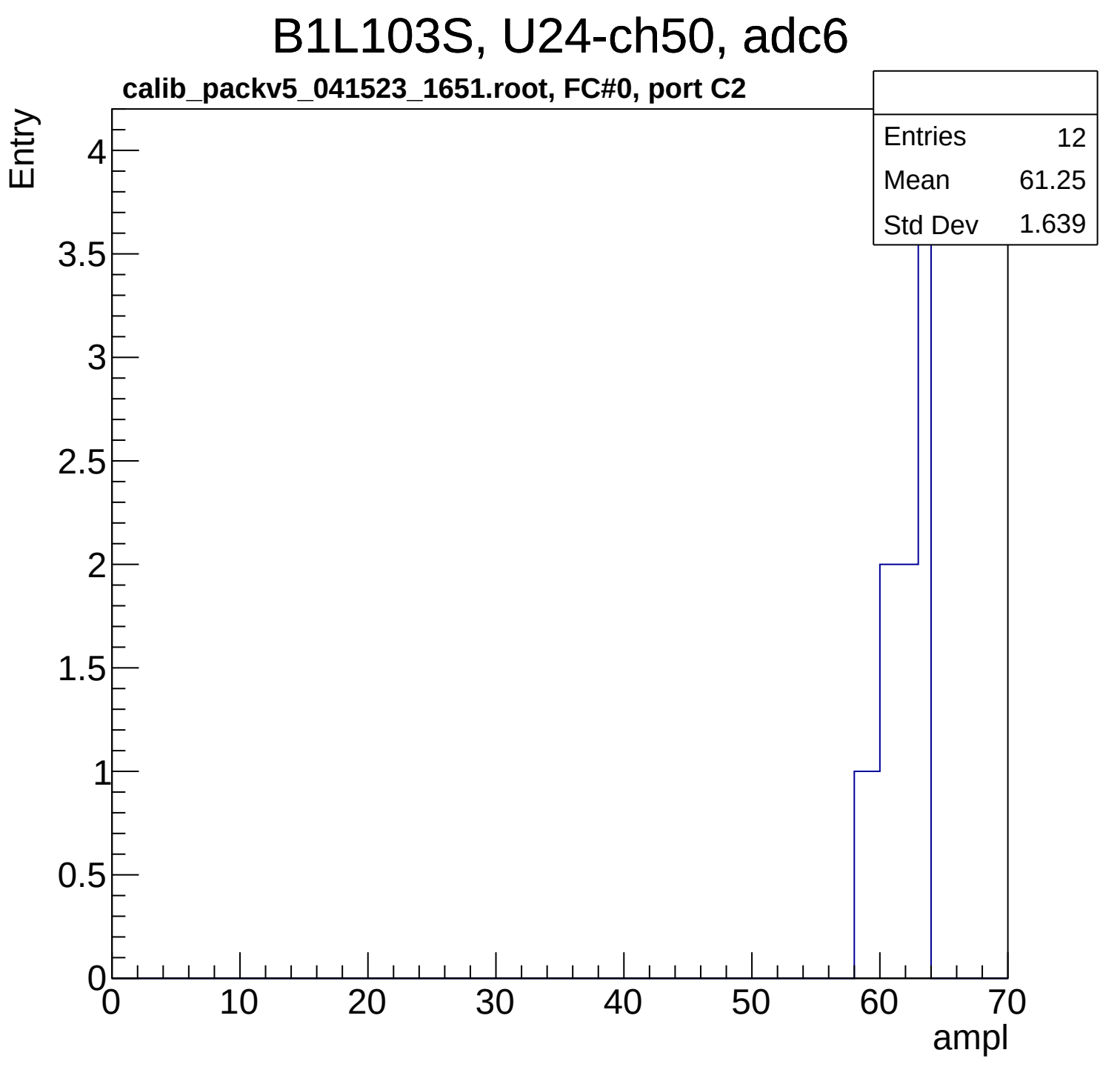
B1L103S, U24-ch50, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 61.25
Std Dev 1.639
Entry
ampl
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0.5
1
1.5
2
2.5
3
3.5
4
0
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40
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60
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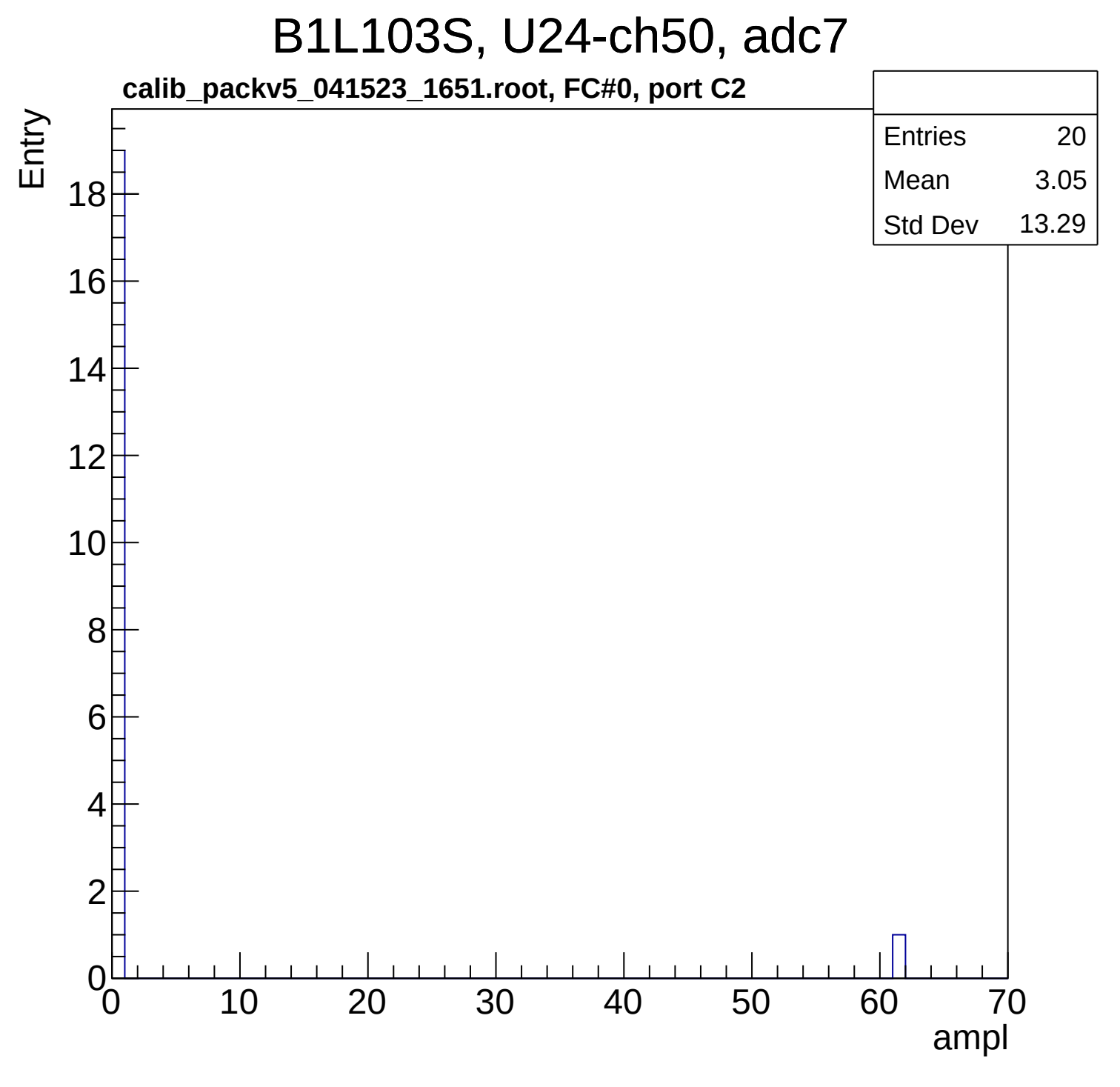
B1L103S, U24-ch50, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.05
Std Dev 13.29
Entry
0
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6
8
10
12
14
16
18
0
10
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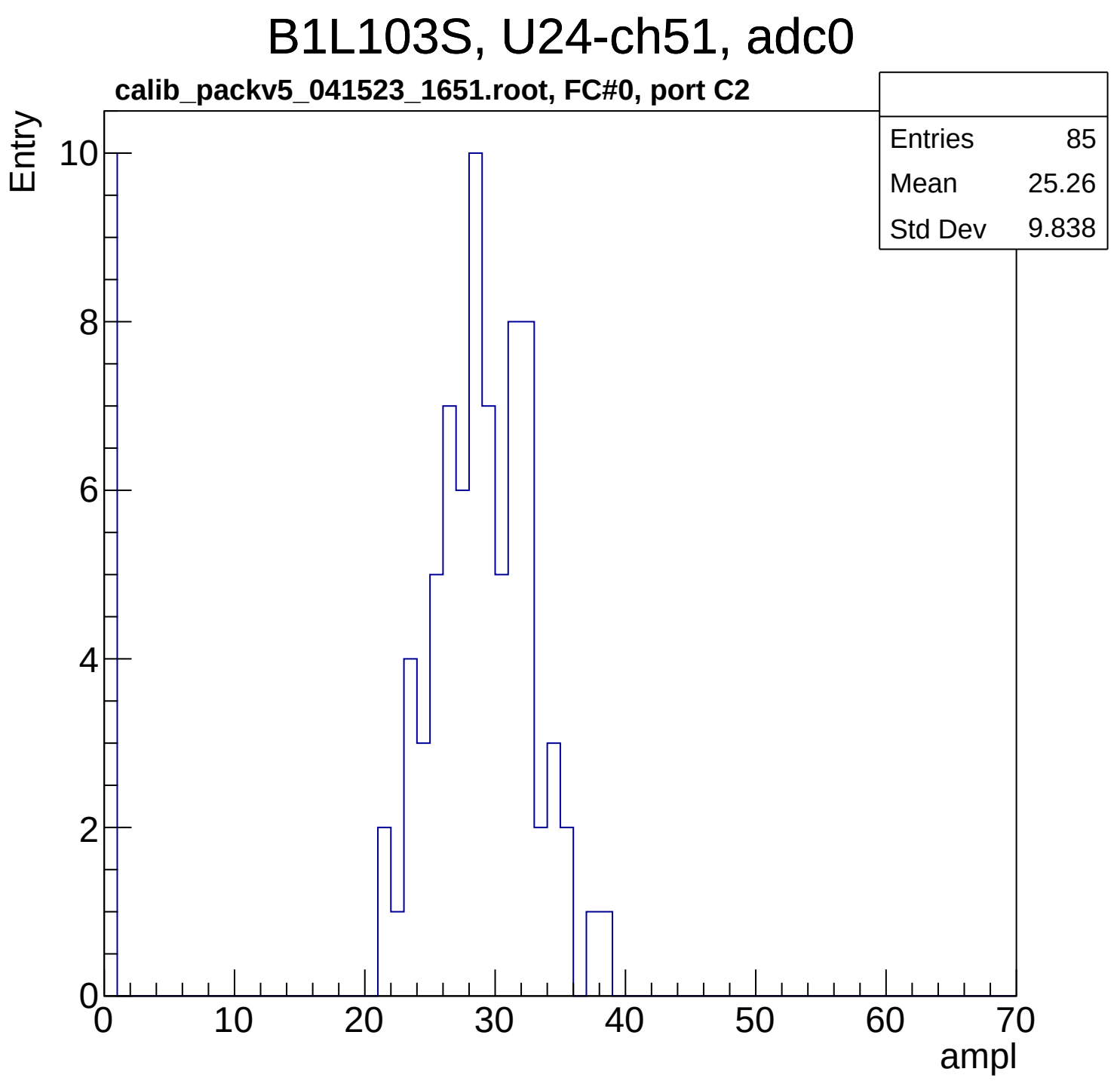
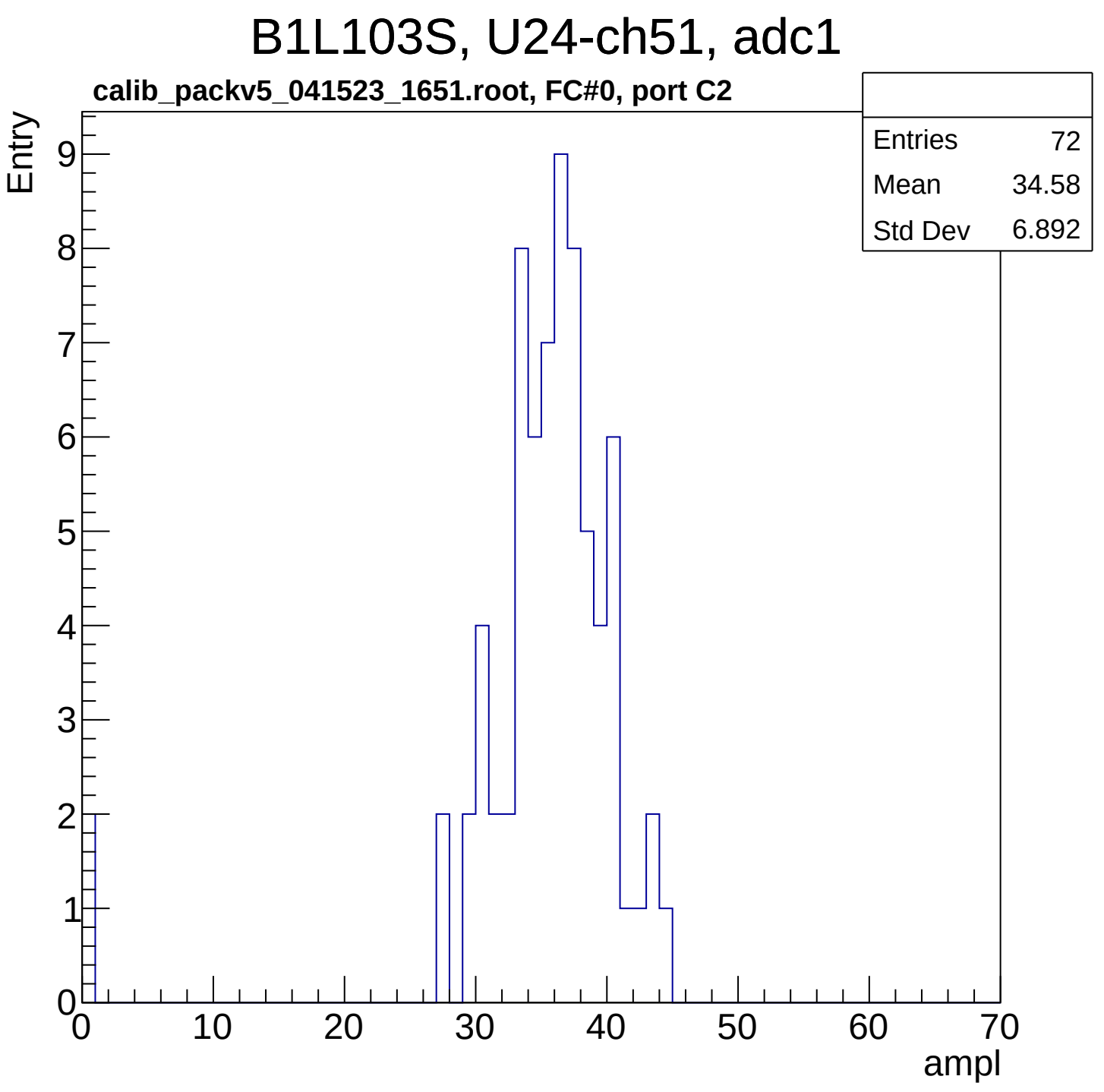
50
60
70
ampl


B1L103S, U24-ch51, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 25.26
Std Dev 9.838
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch51, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 34.58
Std Dev 6.892
Entry
ampl
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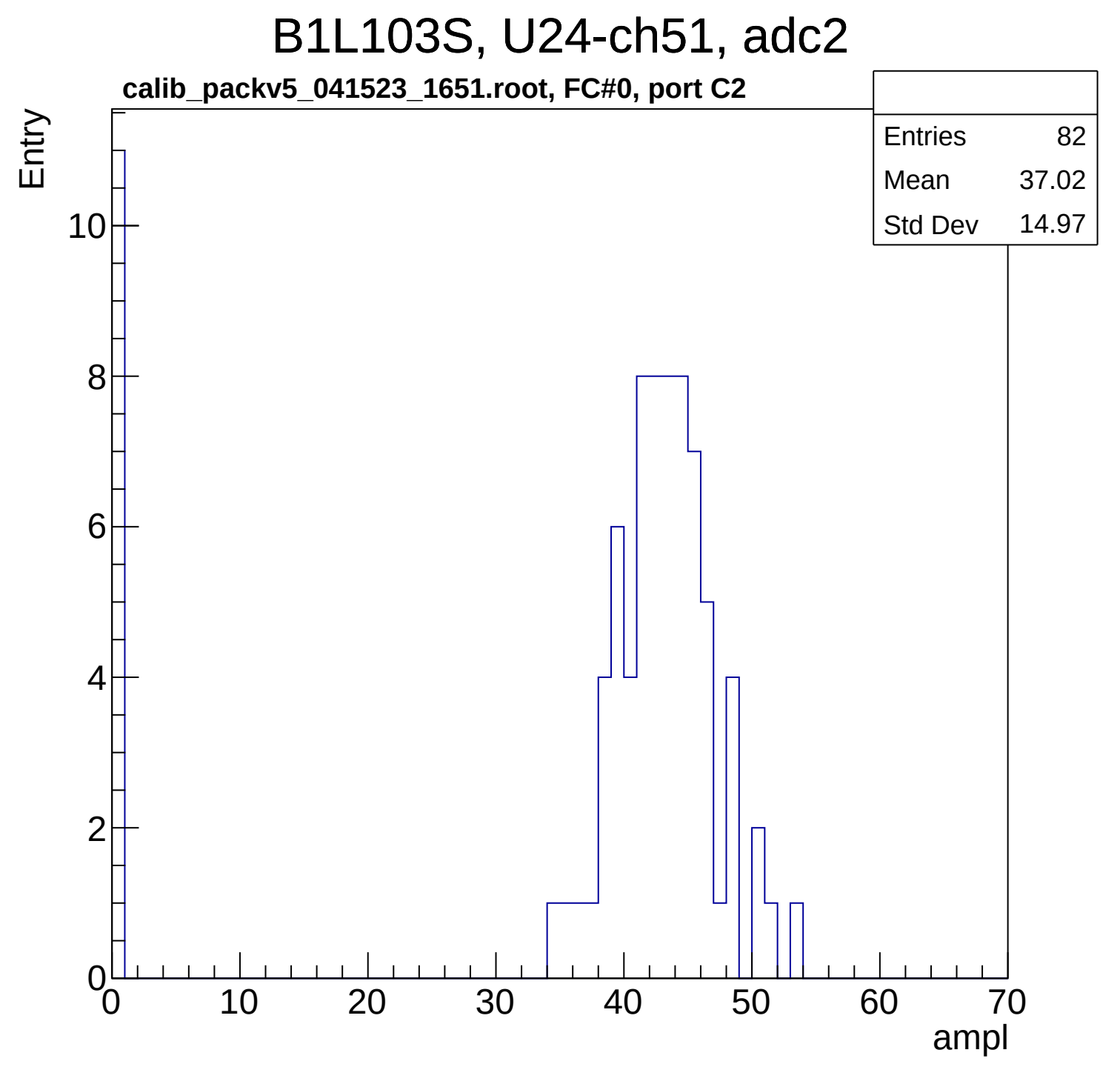
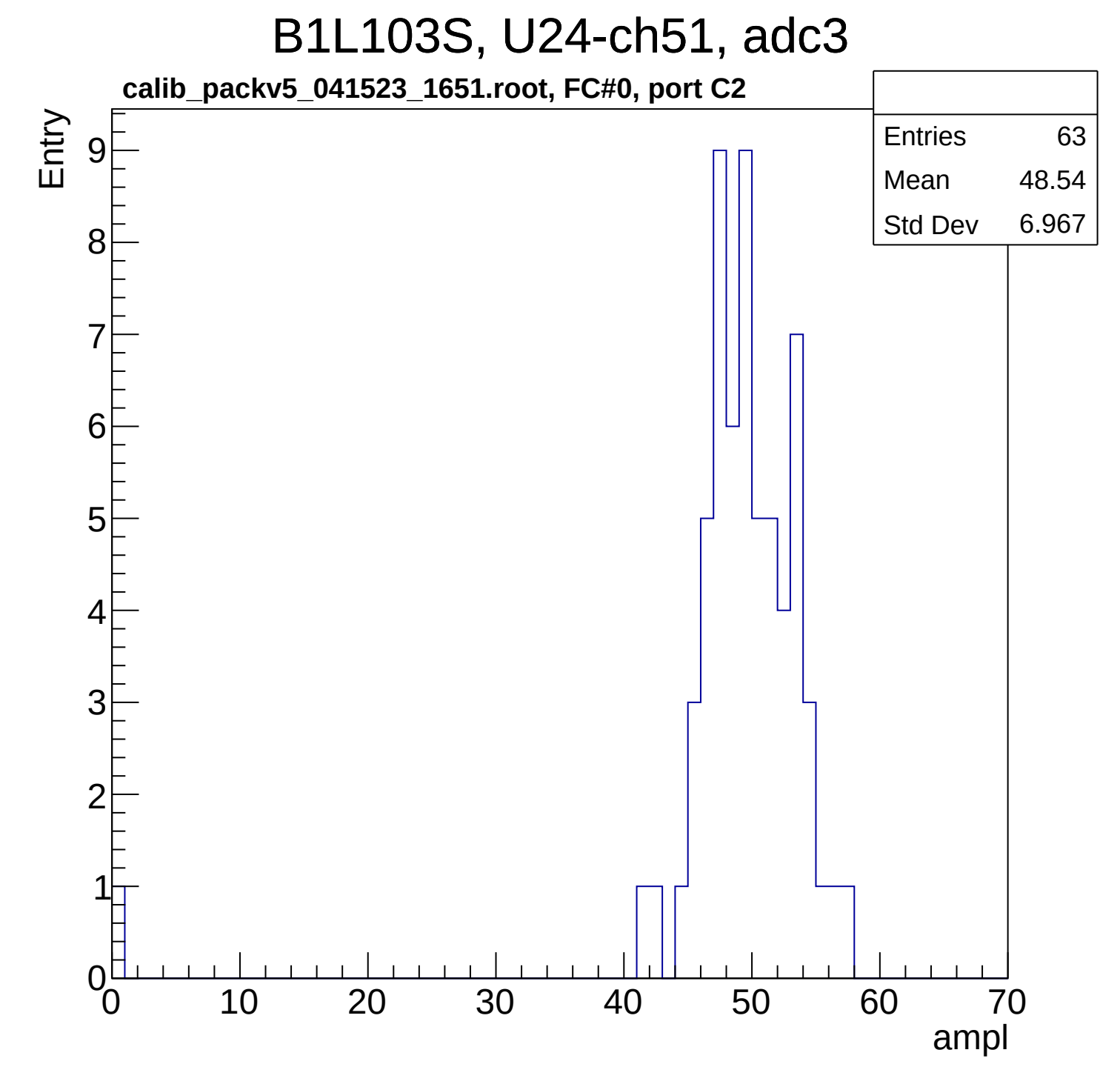
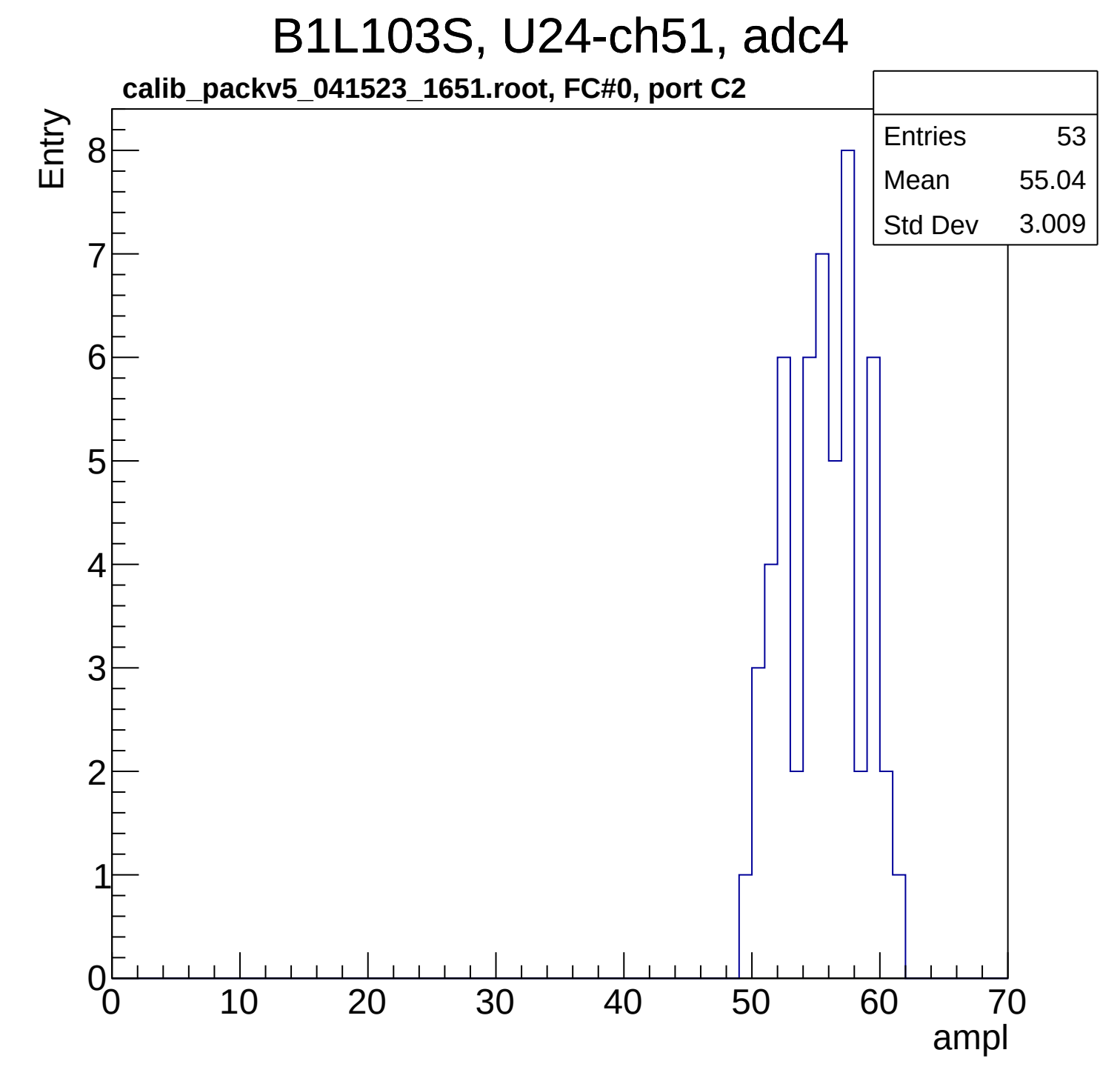
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U24-ch51, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 37.02
Std Dev 14.97
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch51, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 48.54
Std Dev 6.967
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U24-ch51, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 55.04
Std Dev 3.009
Entry
ampl
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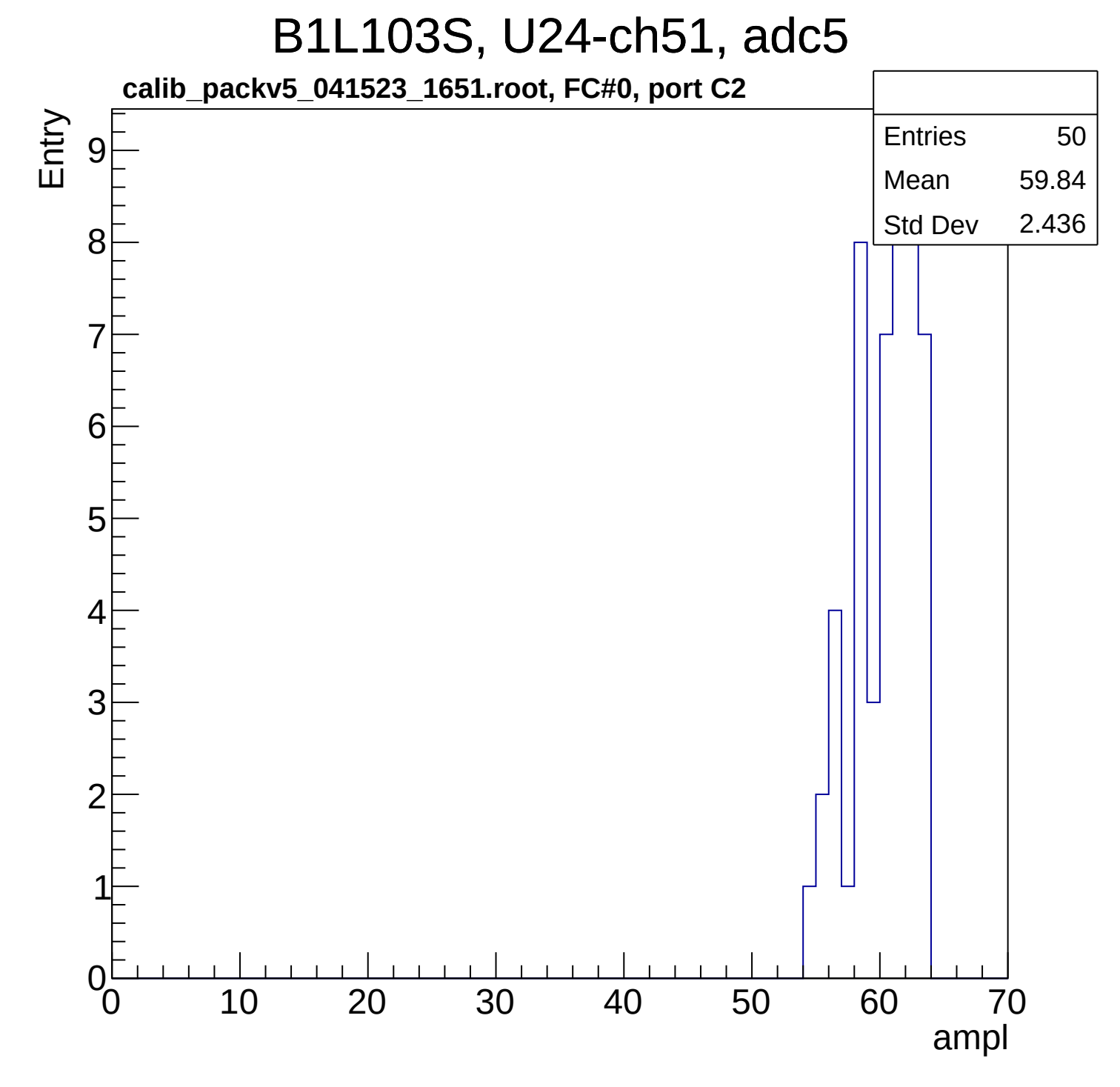
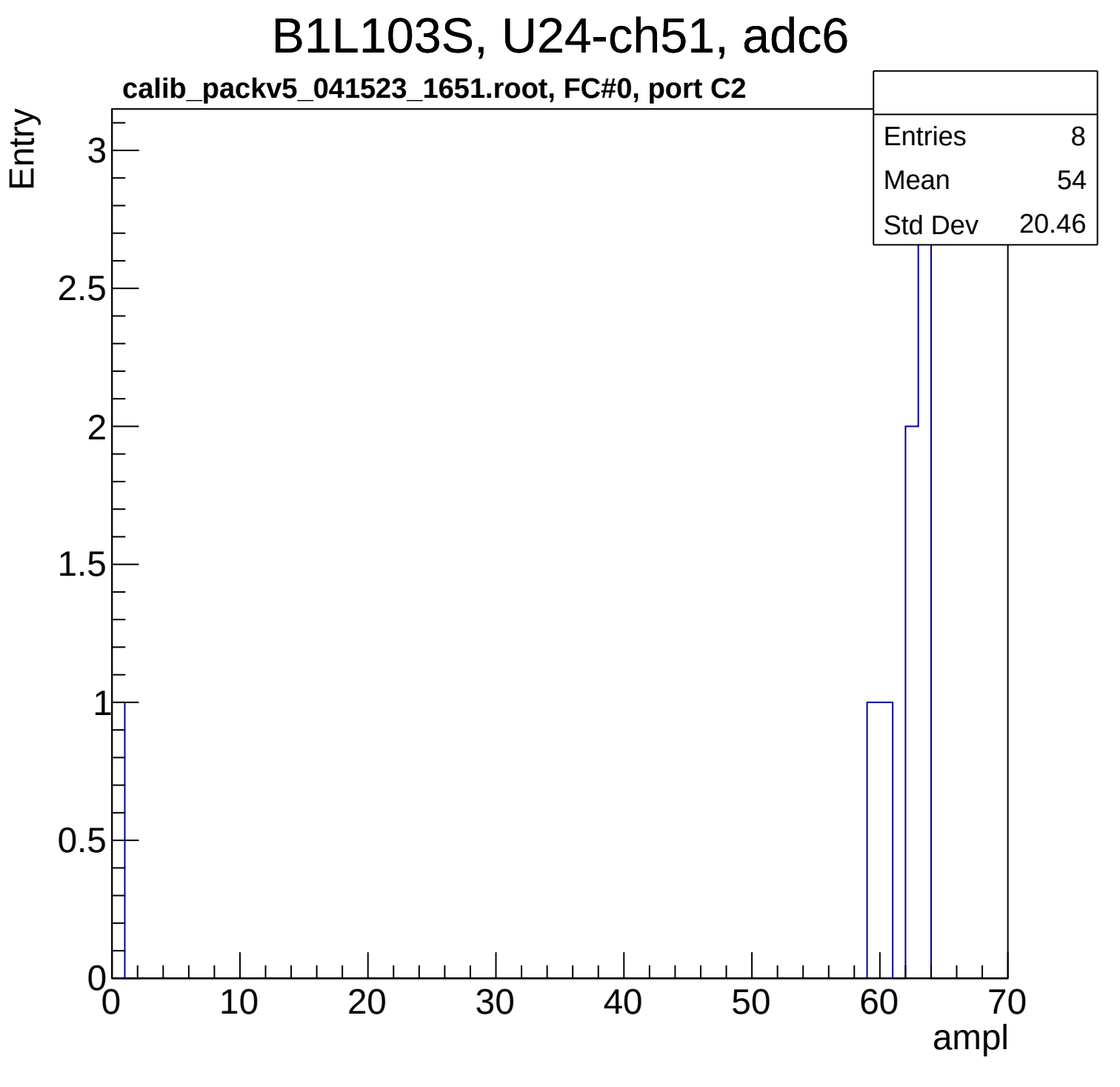
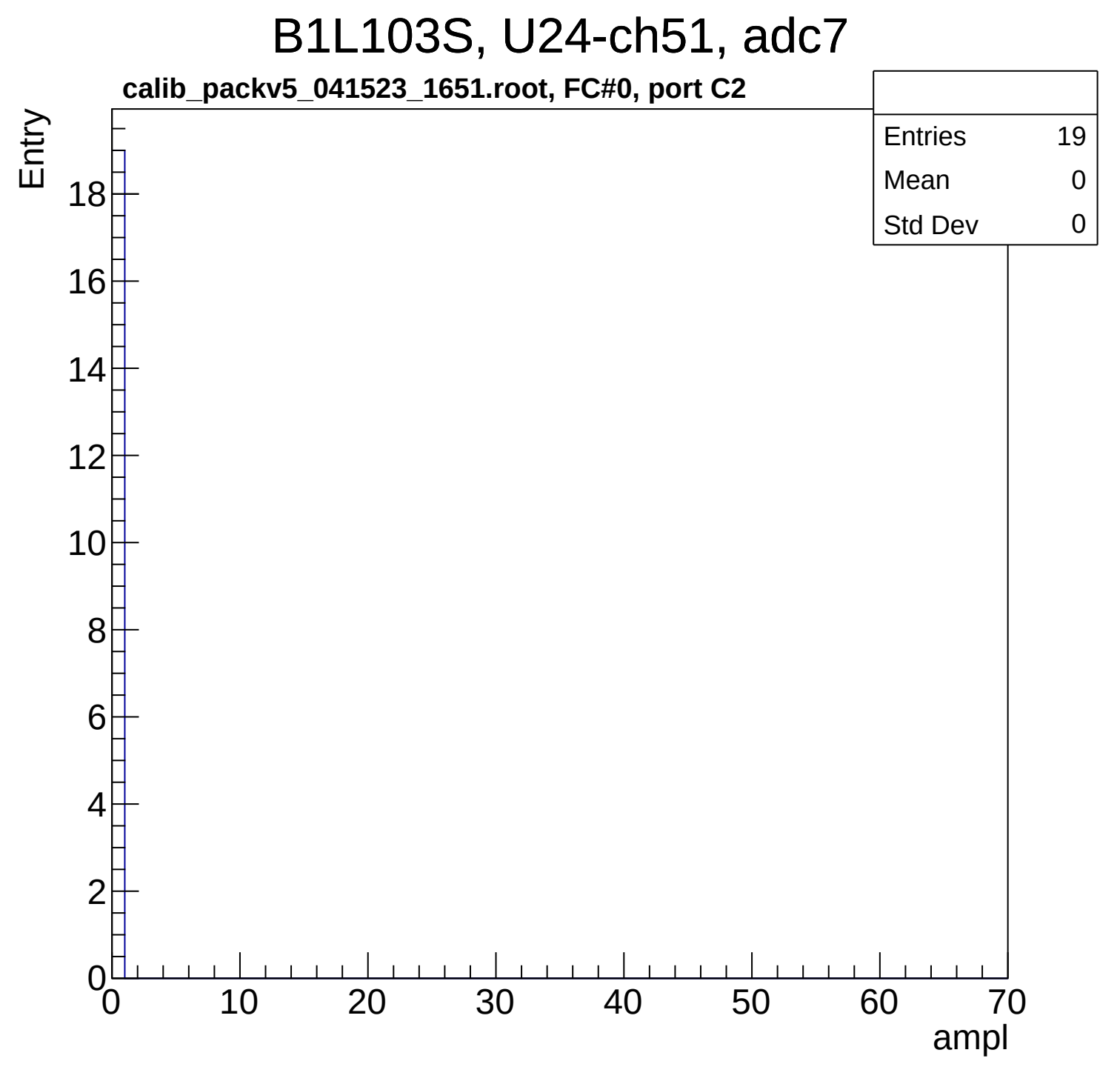
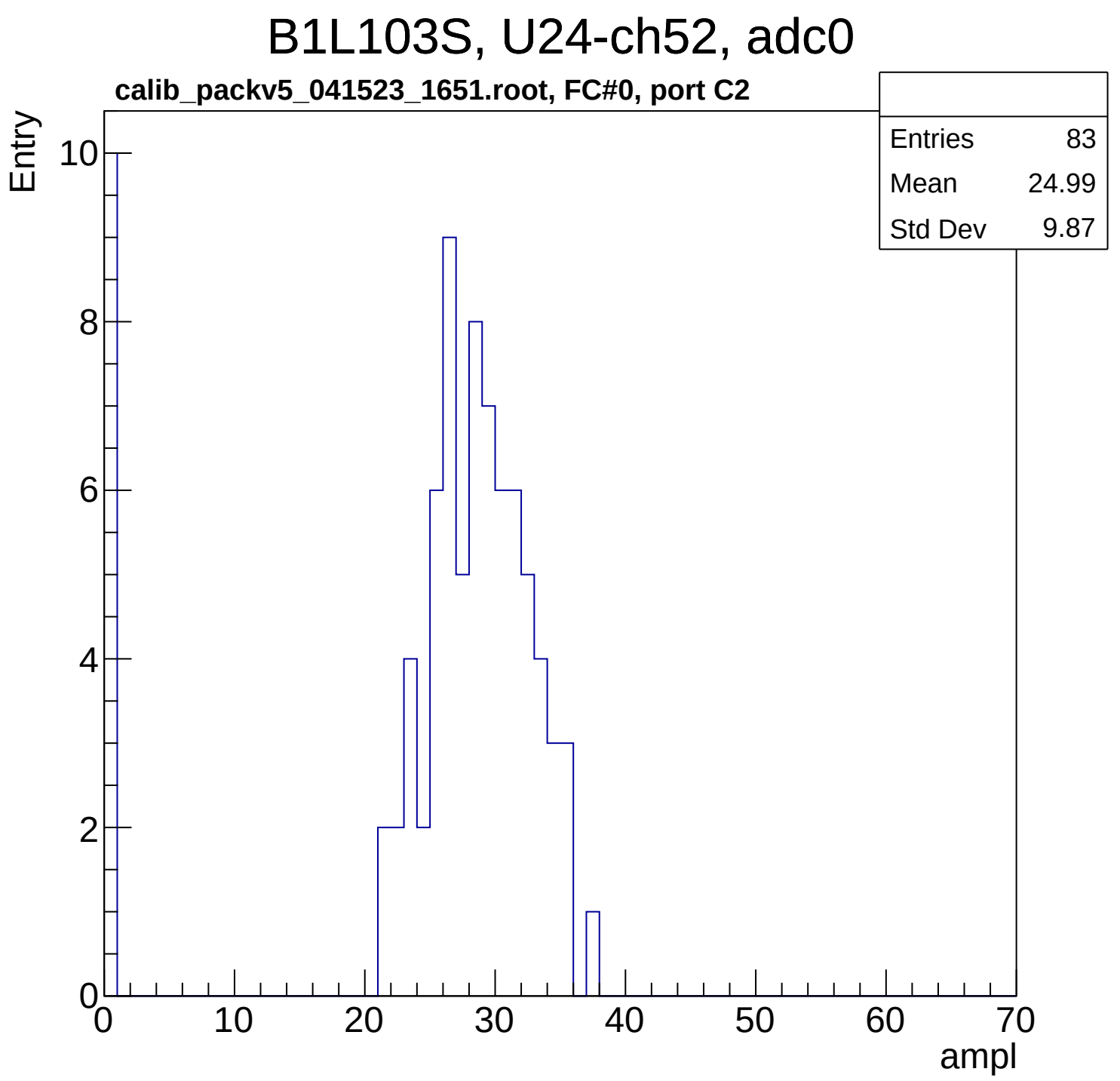
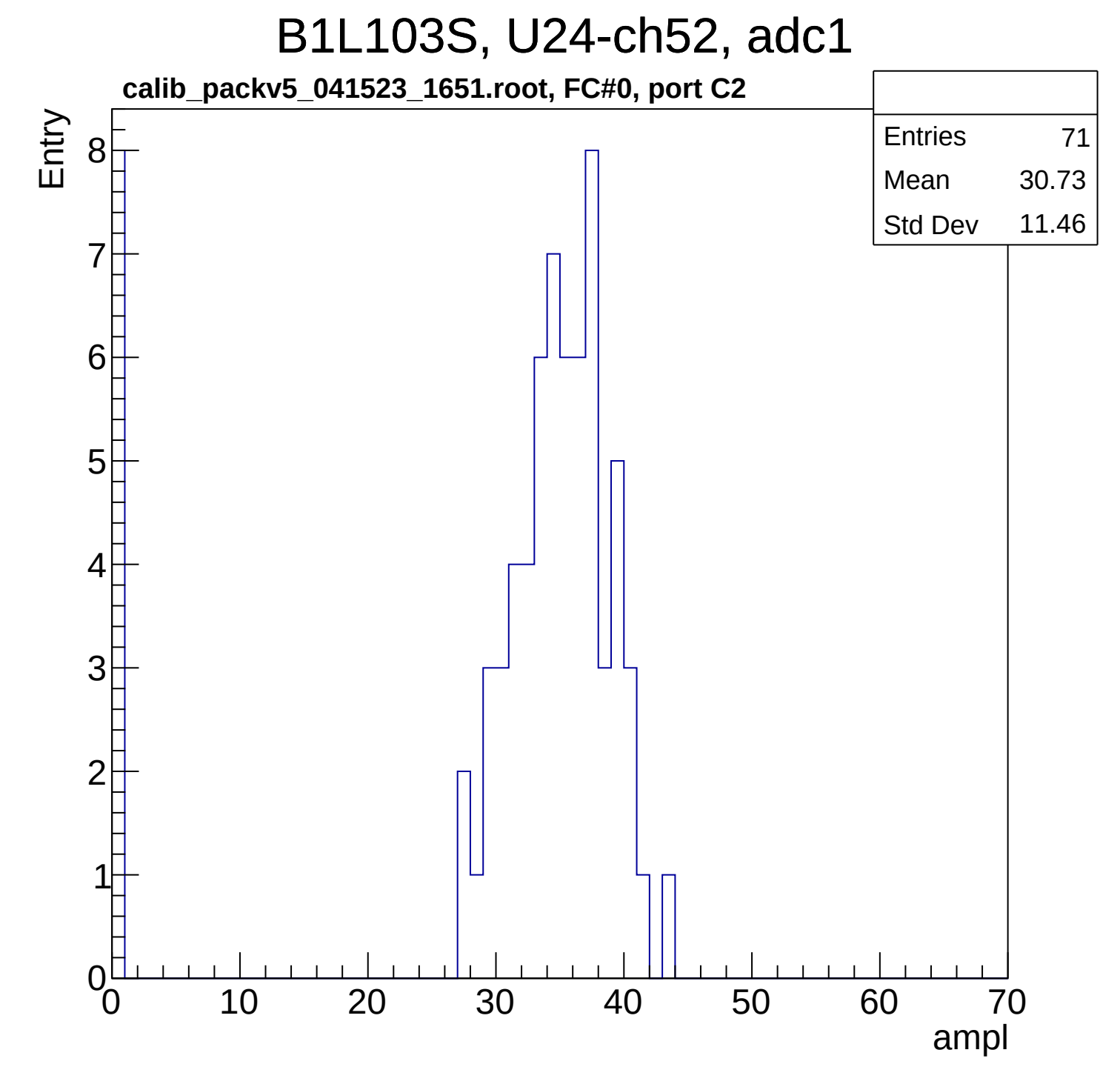
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U24-ch51, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 59.84
Std Dev 2.436
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U24-ch51, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 54
Std Dev 20.46
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U24-ch51, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch52, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 24.99
Std Dev 9.87
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch52, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 30.73
Std Dev 11.46
Entry
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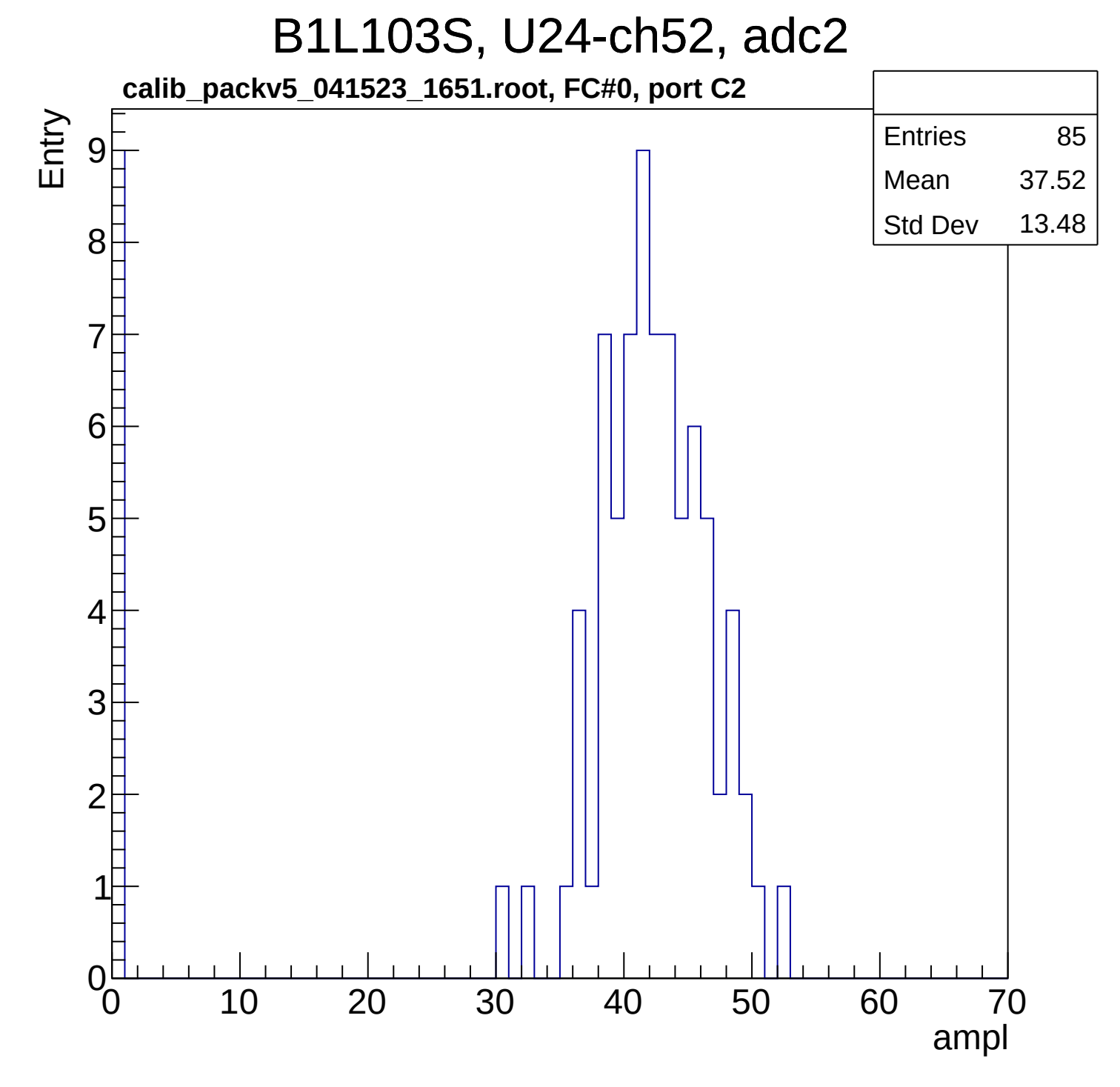
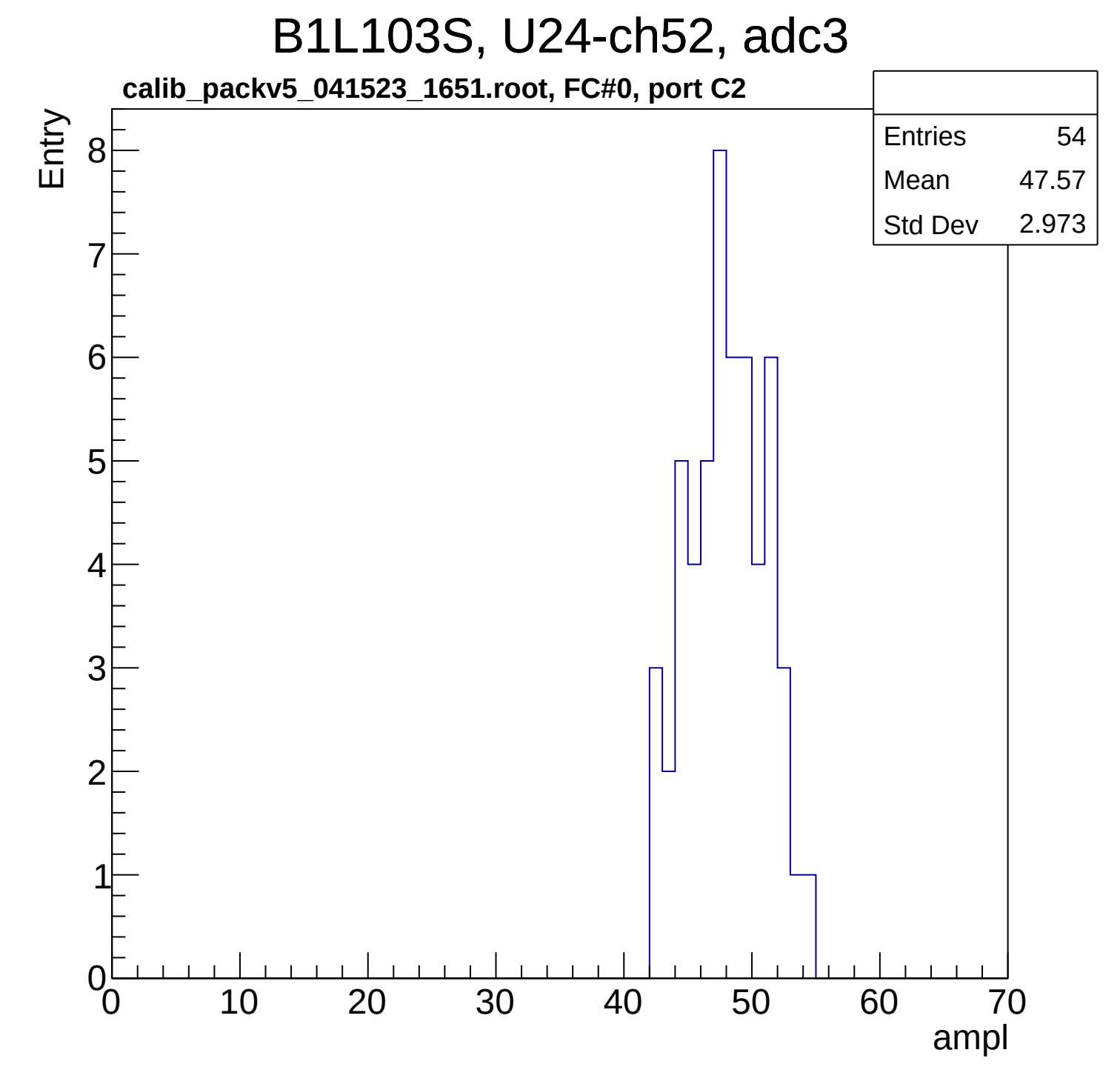
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch52, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 37.52
Std Dev 13.48
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U24-ch52, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 47.57
Std Dev 2.973
Entry
ampl
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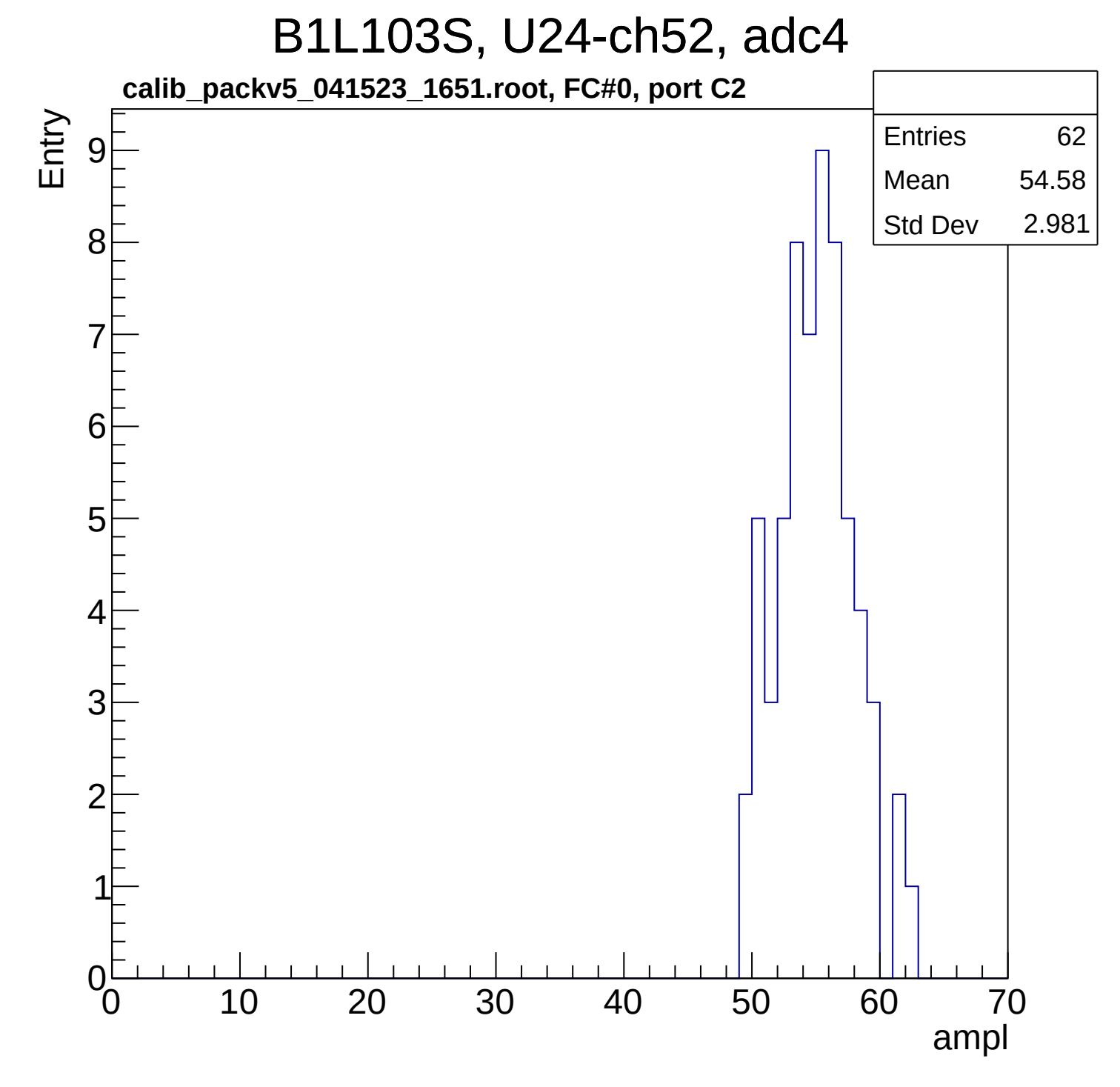
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U24-ch52, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 54.58
Std Dev 2.981
Entry
ampl
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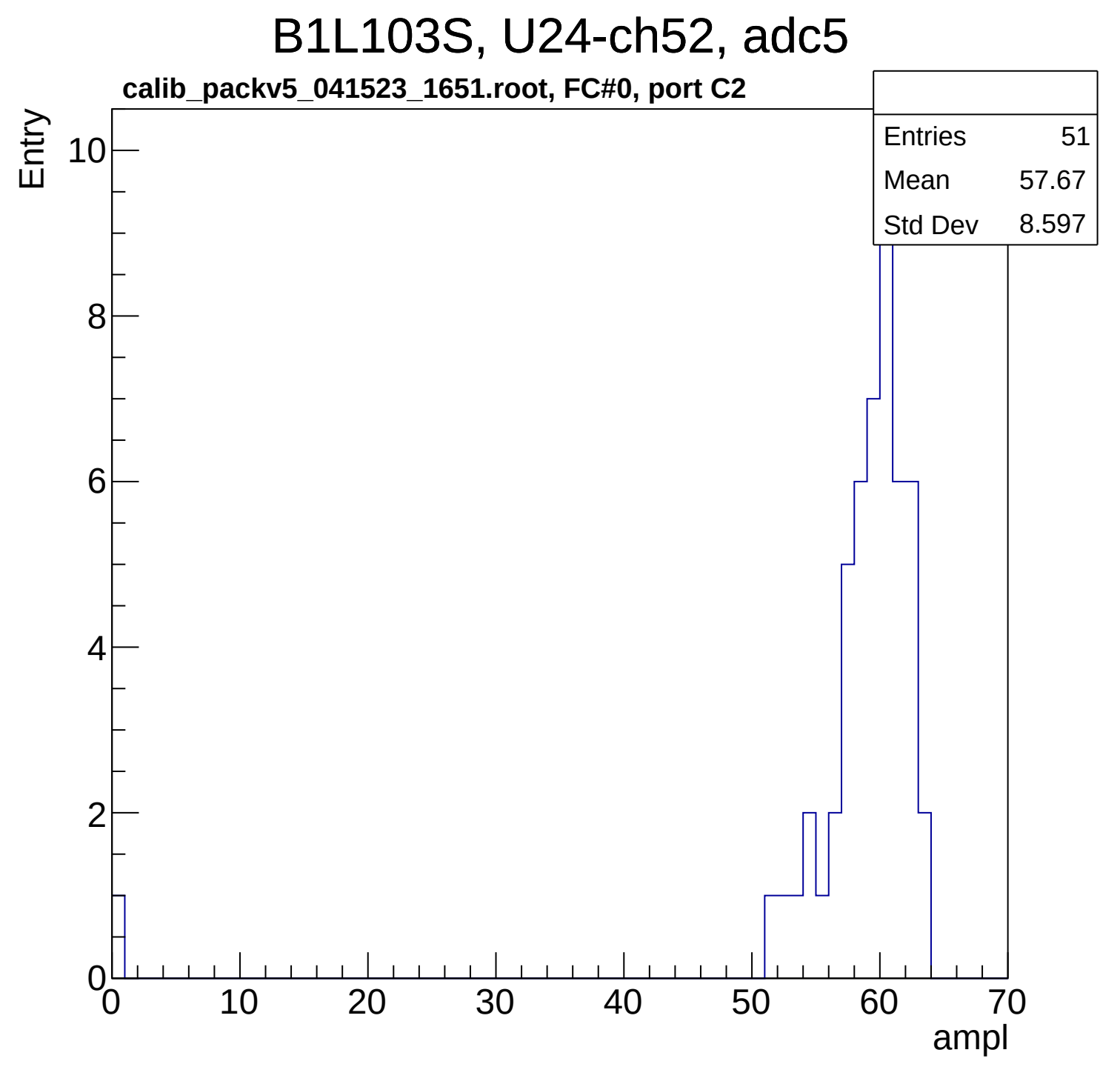
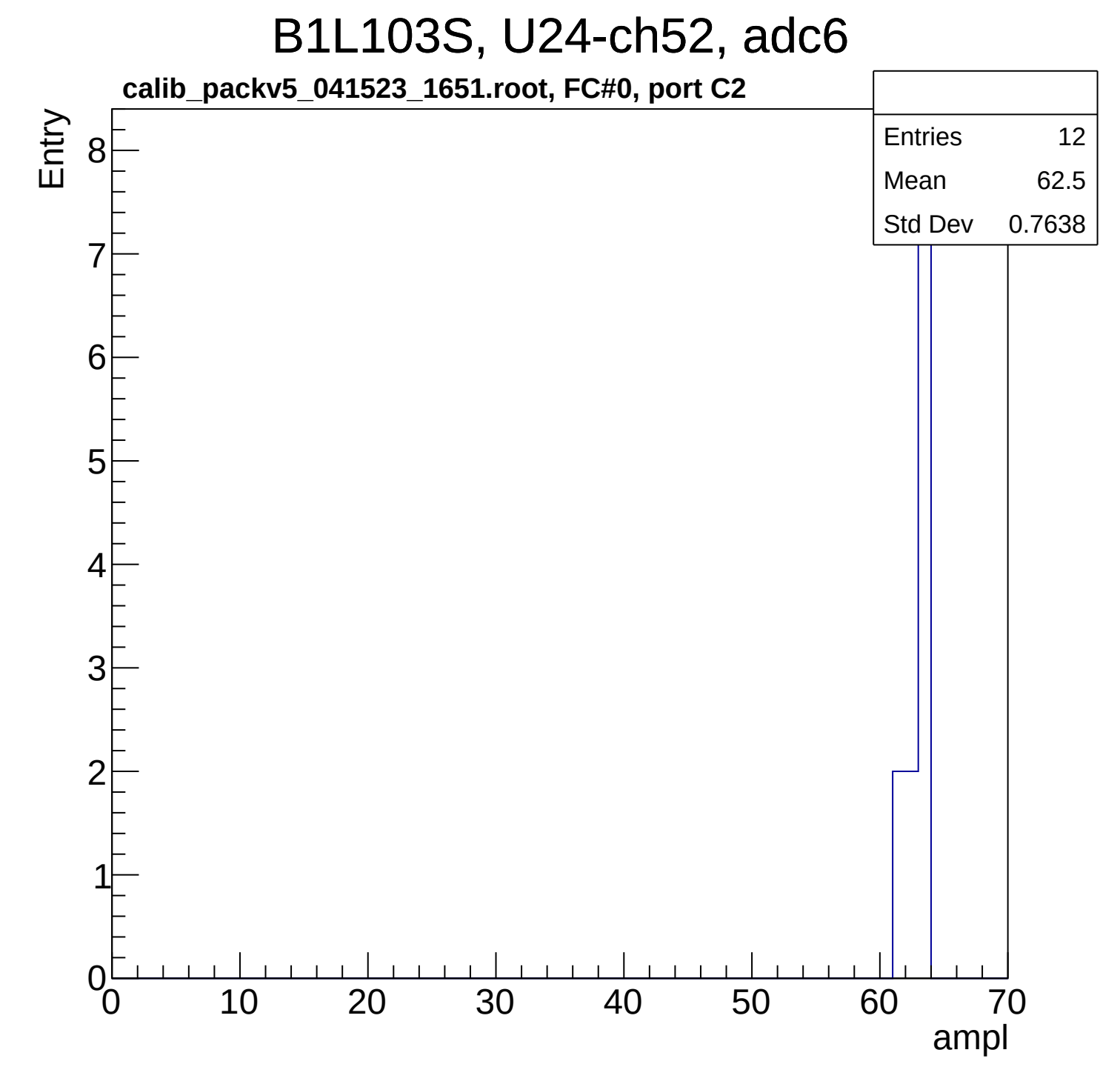
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U24-ch52, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 57.67
Std Dev 8.597
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch52, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 62.5
Std Dev 0.7638
Entry
ampl
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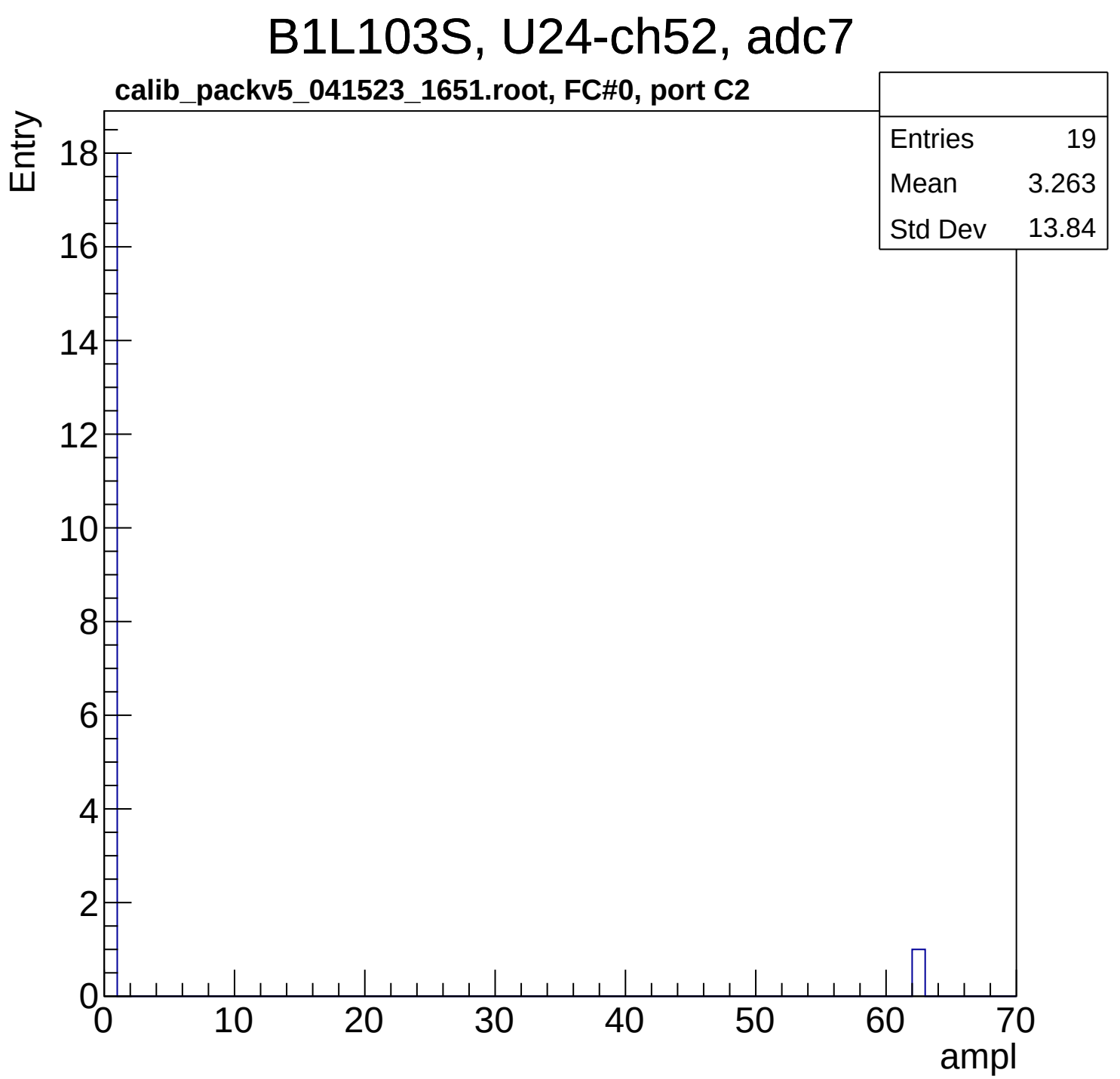
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U24-ch52, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 3.263
Std Dev 13.84
Entry
0
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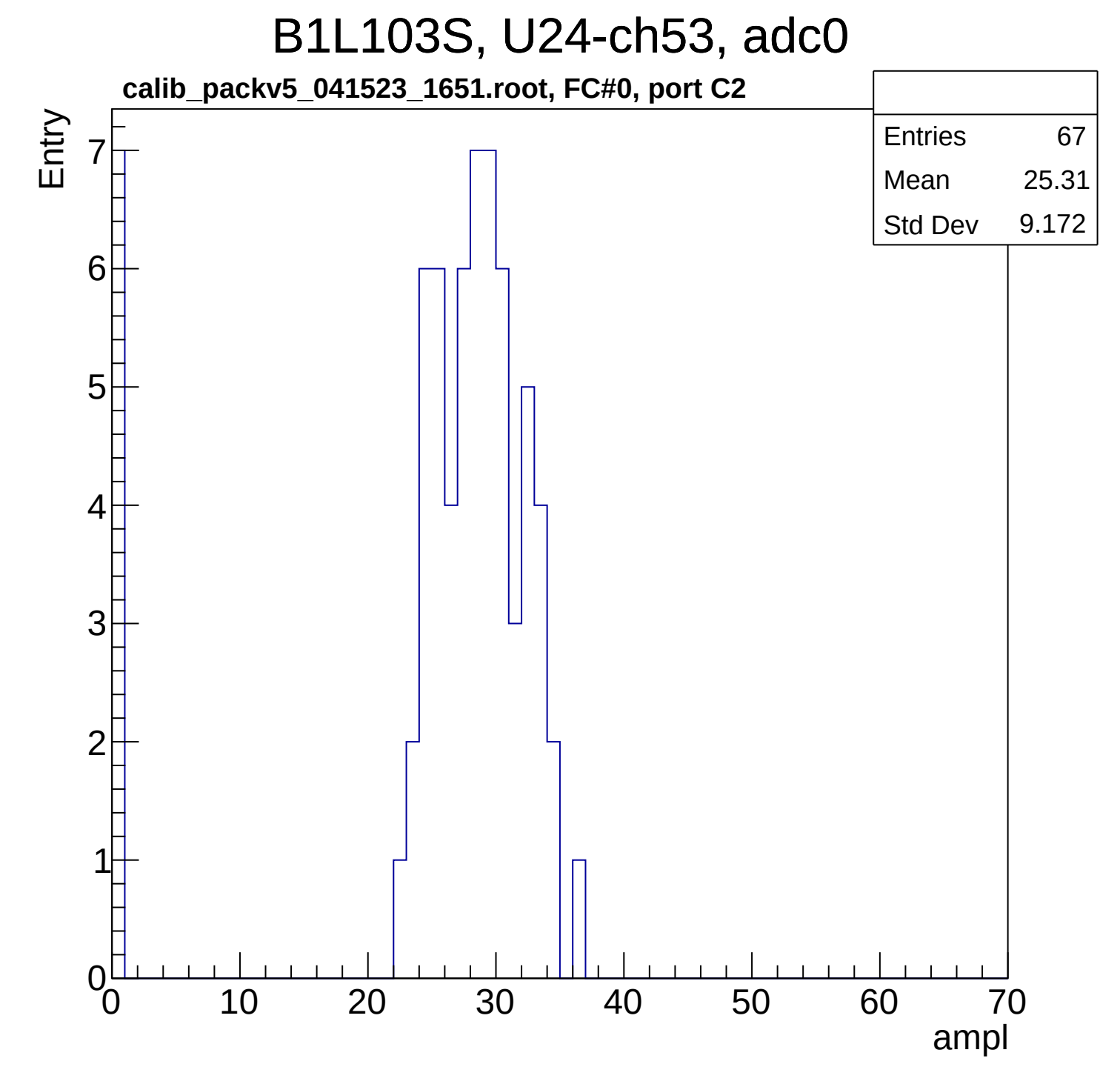
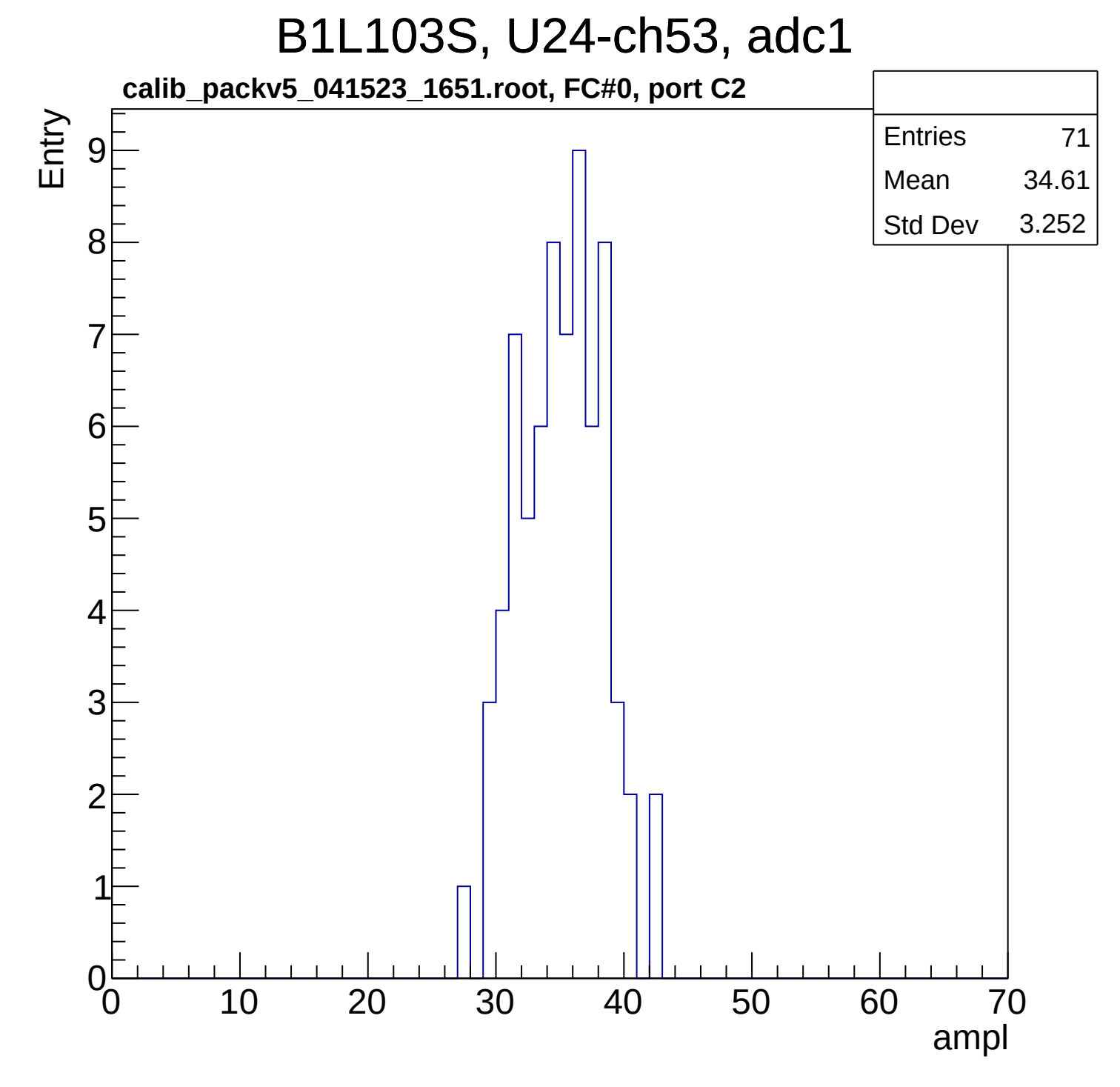
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch53, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 25.31
Std Dev 9.172
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U24-ch53, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 34.61
Std Dev 3.252
Entry
ampl
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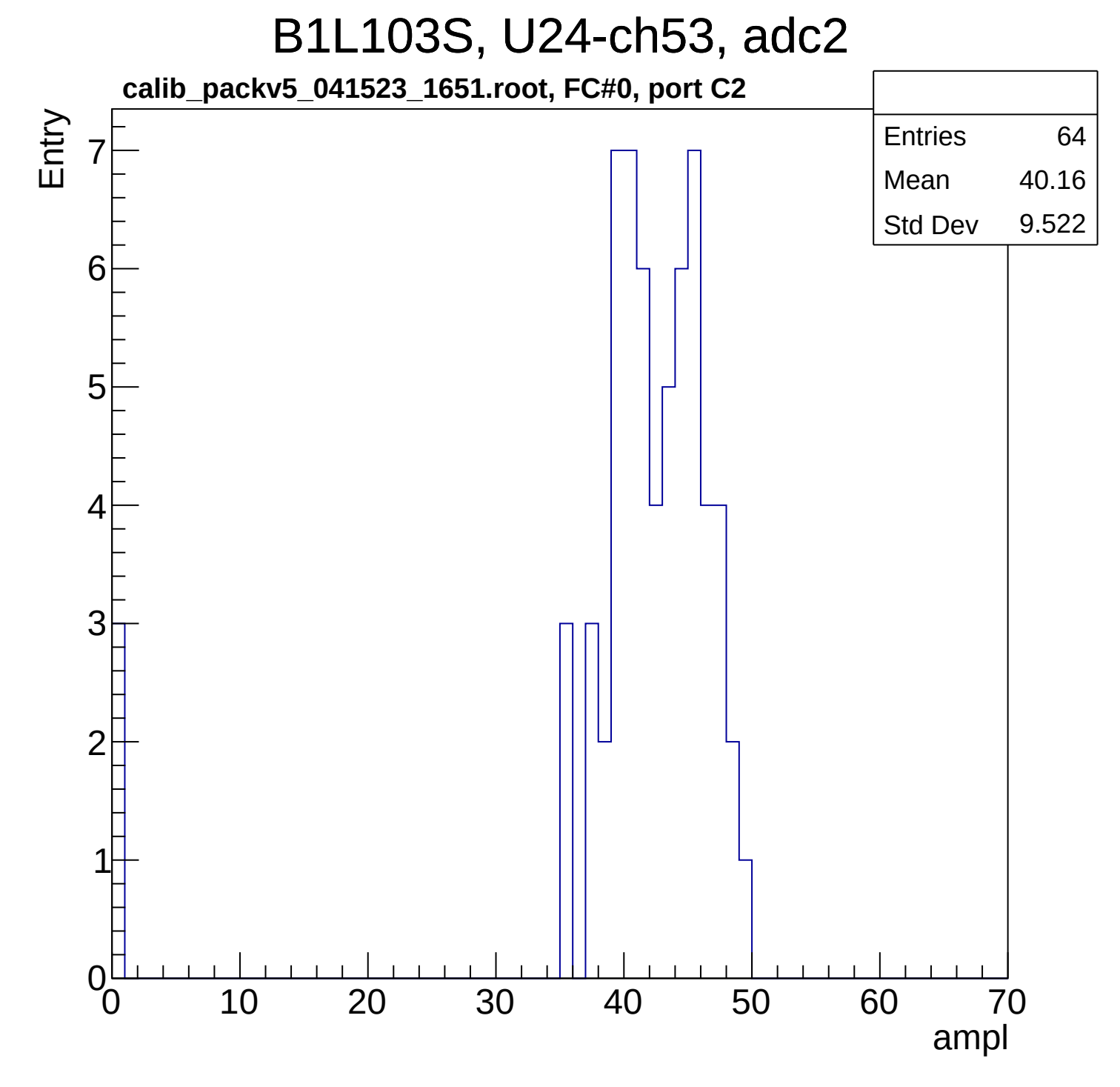
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U24-ch53, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 40.16
Std Dev 9.522
Entry
ampl
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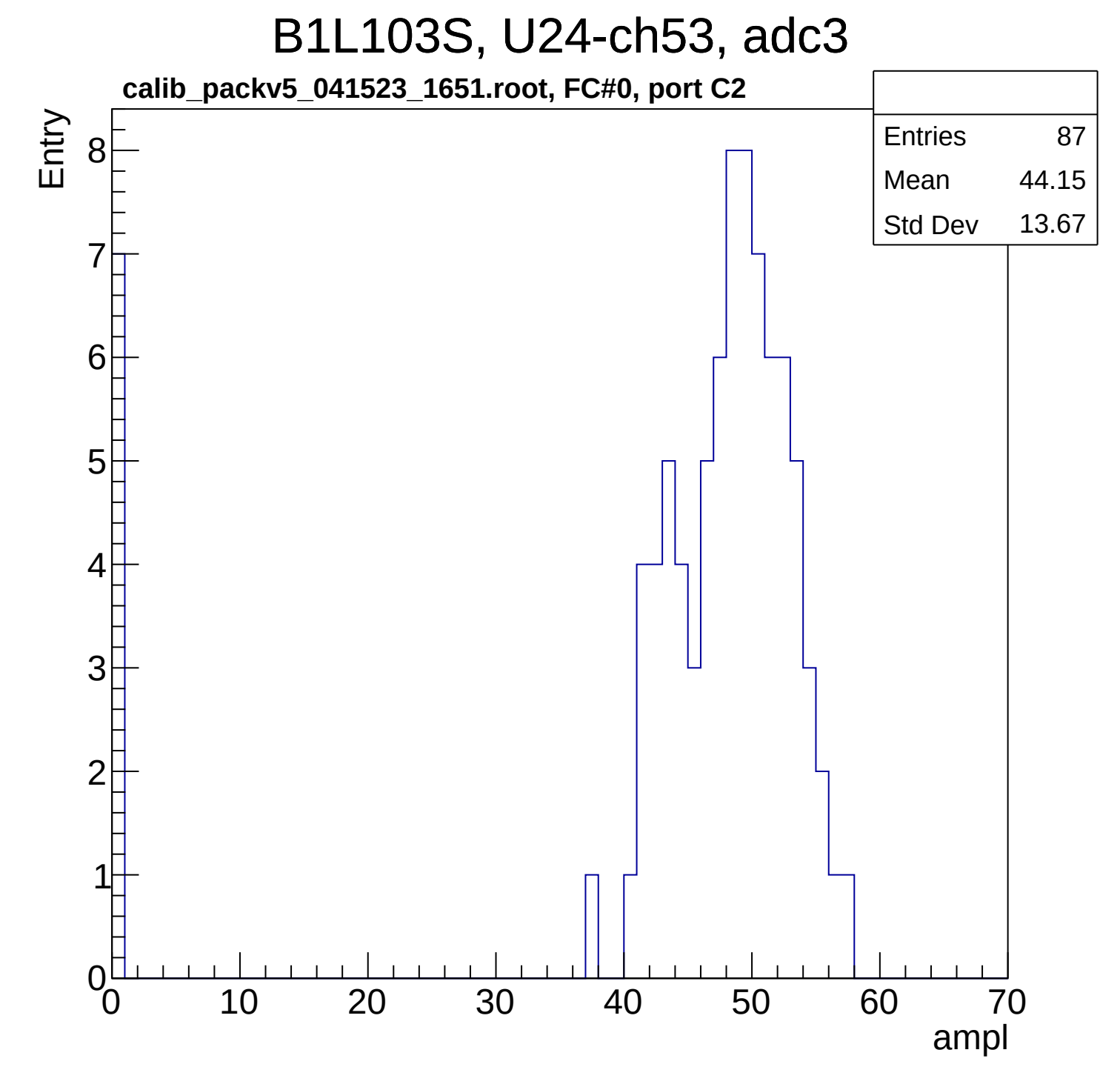
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U24-ch53, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 87
Mean 44.15
Std Dev 13.67
Entry
ampl
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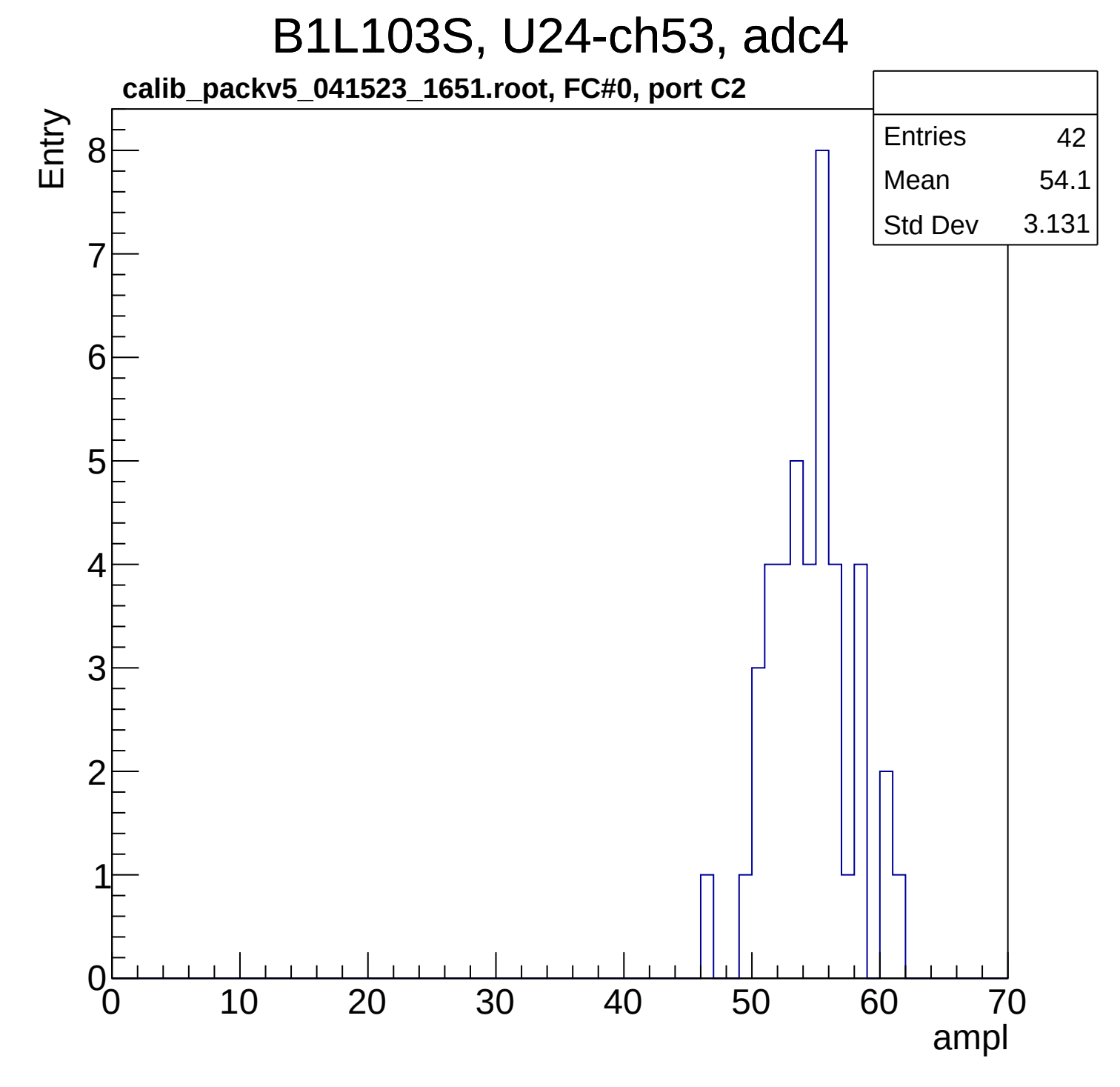
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U24-ch53, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 42
Mean 54.1
Std Dev 3.131
Entry
ampl
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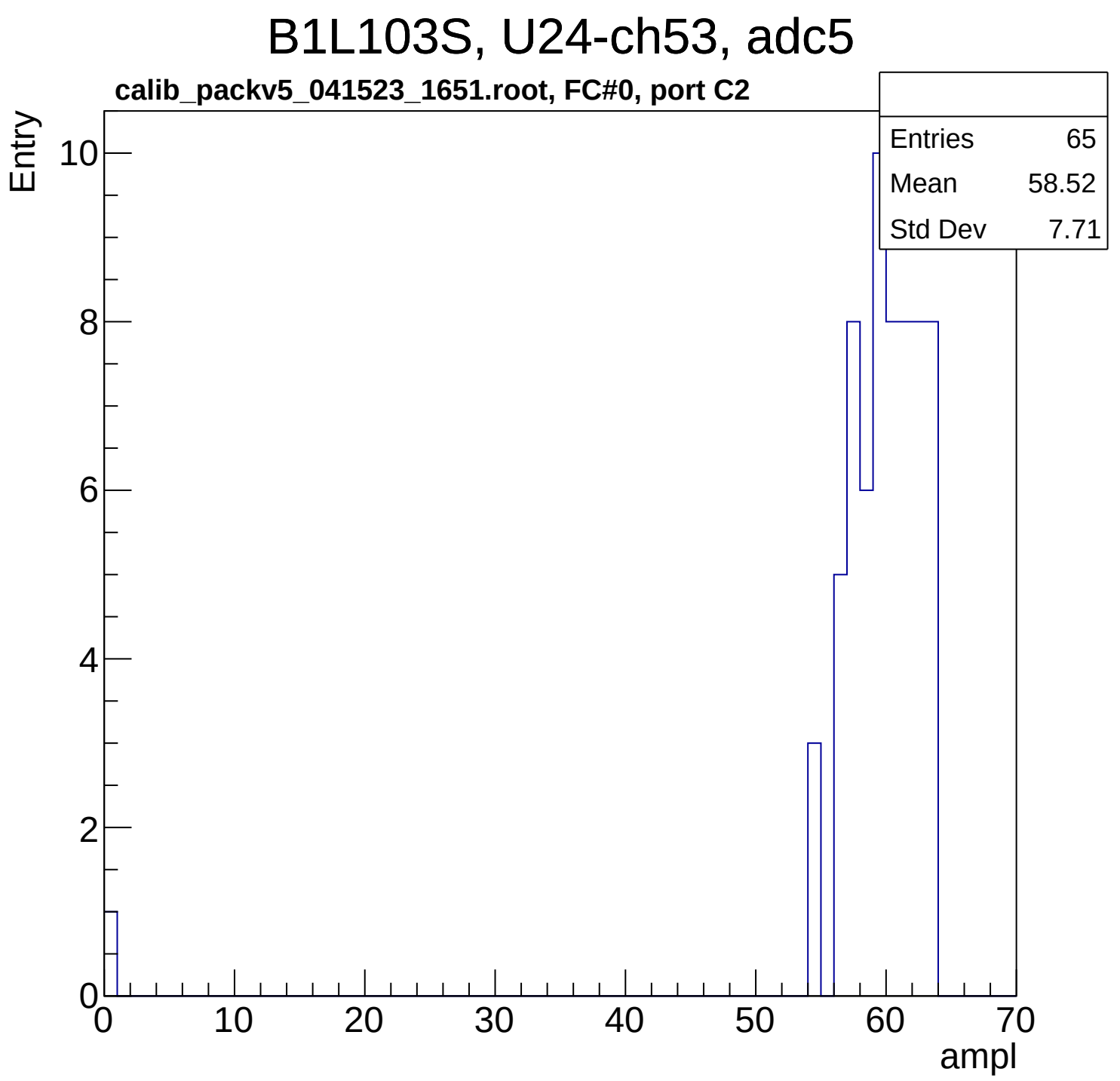
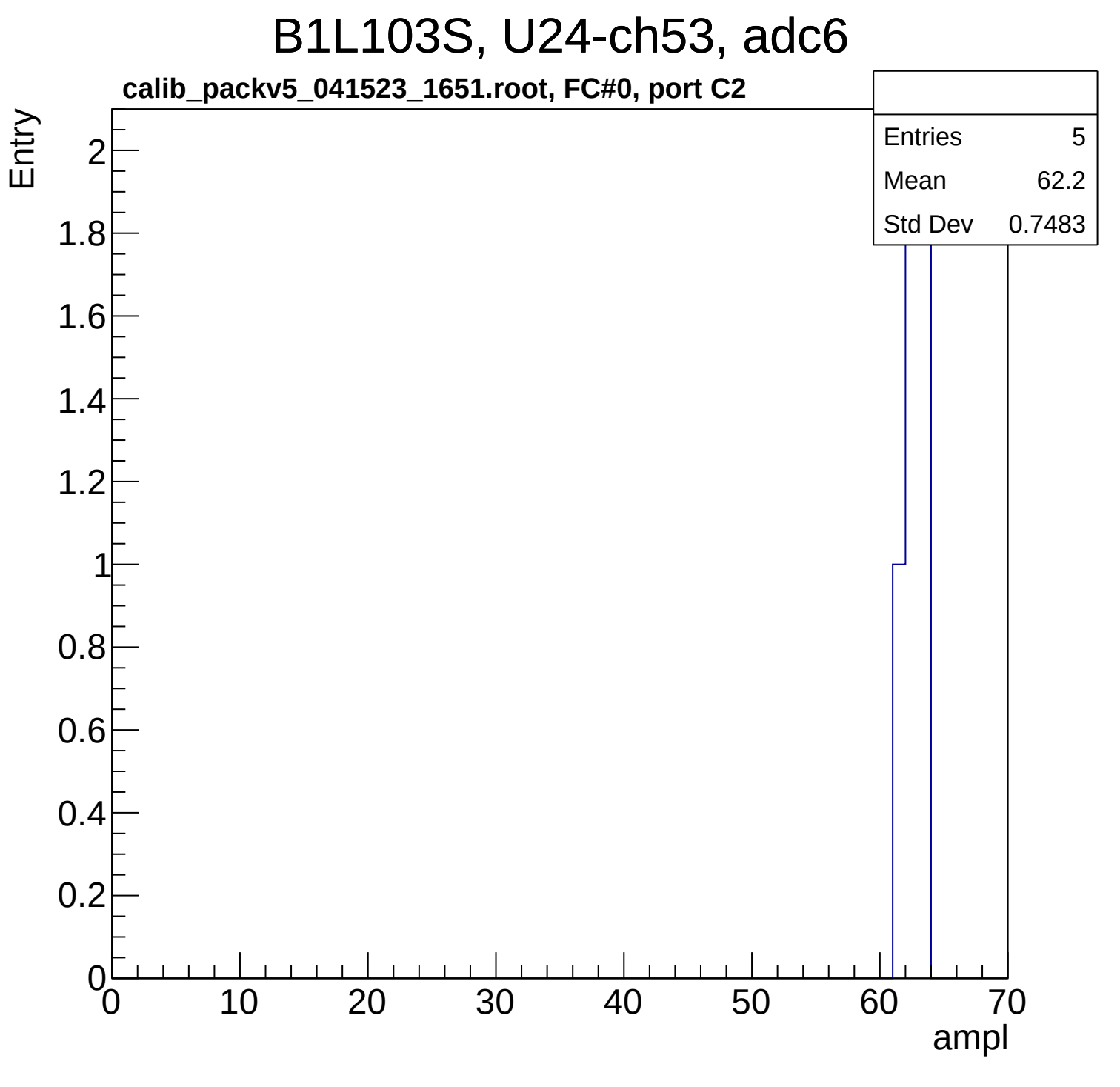
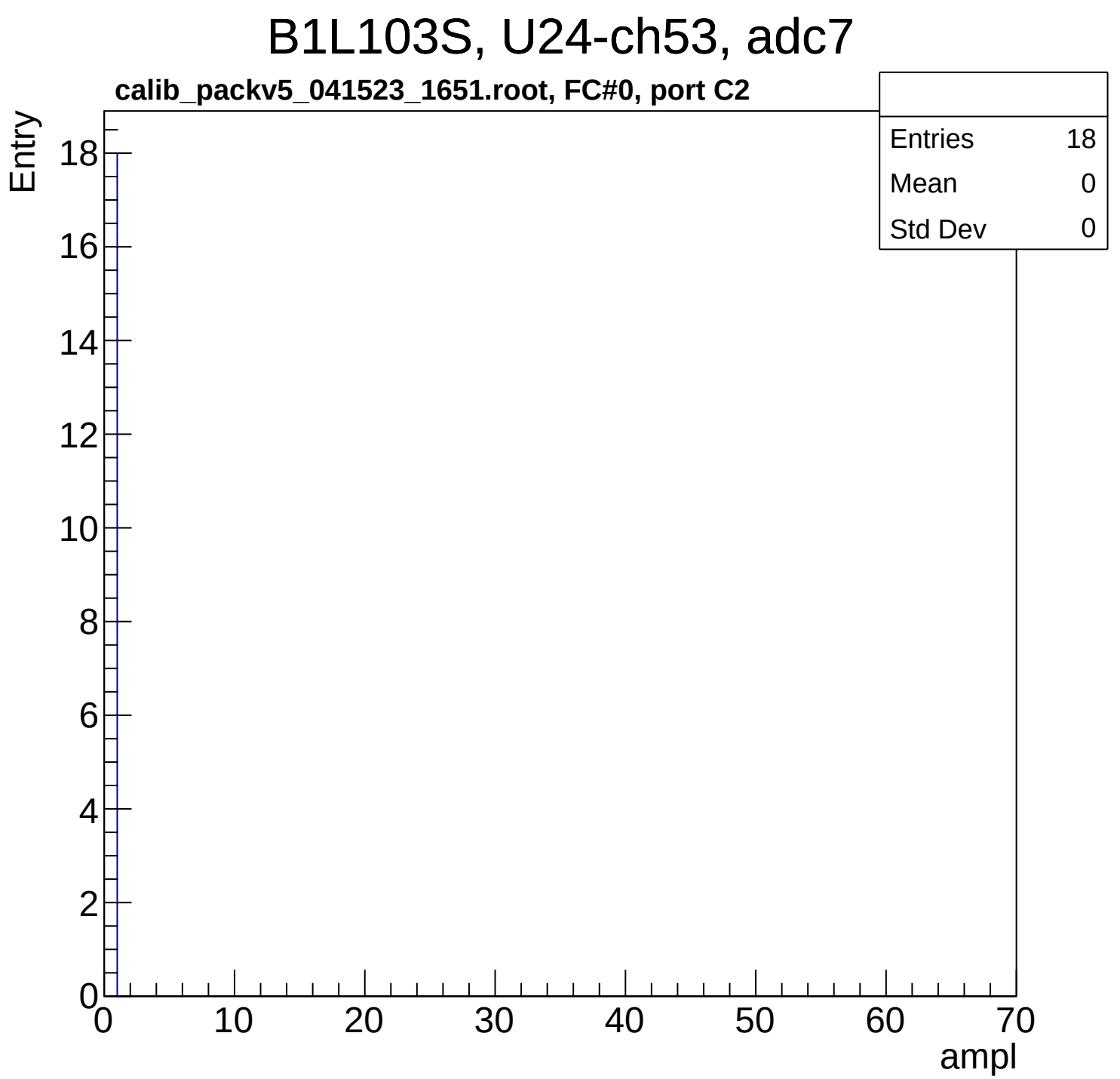
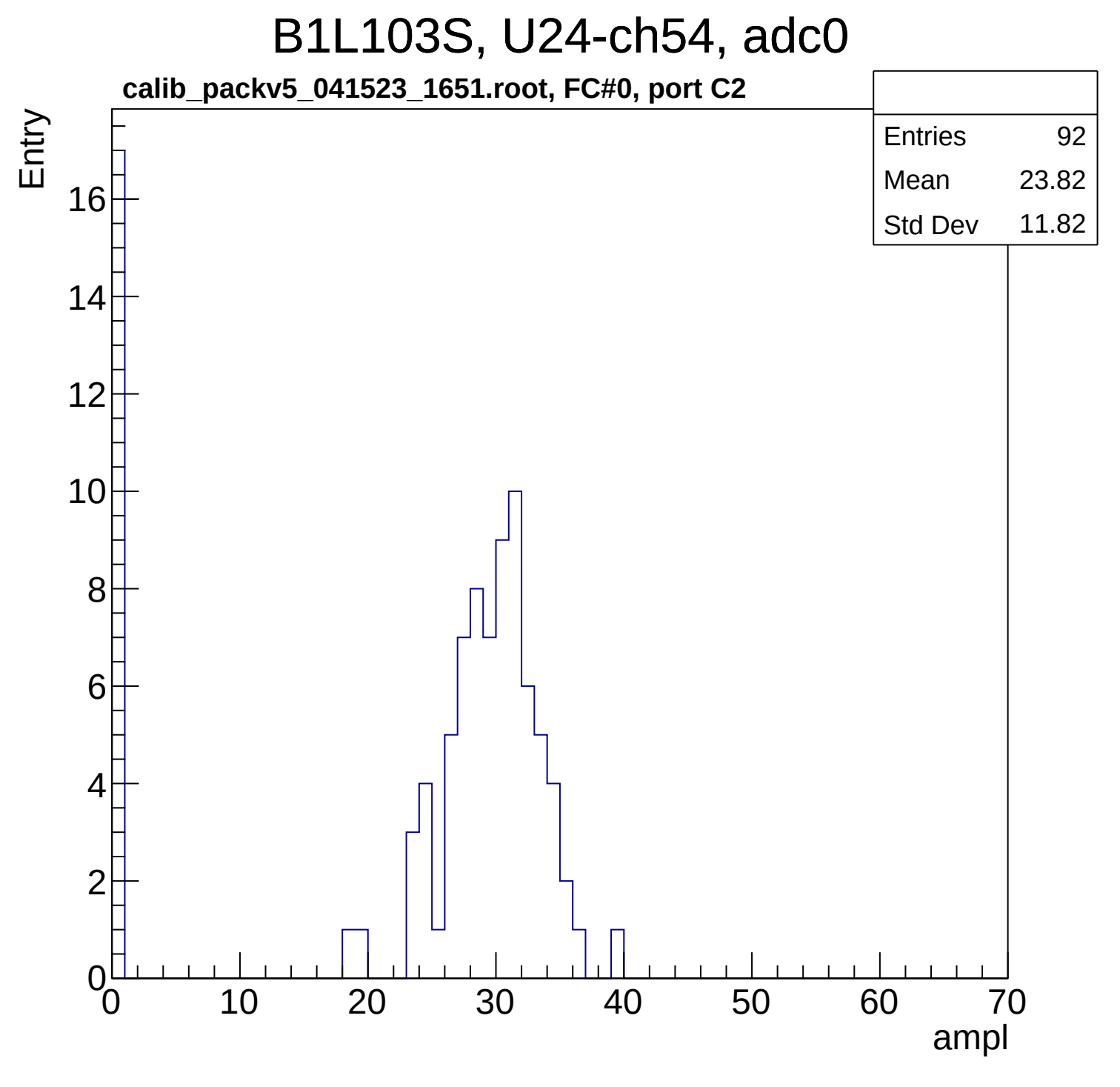
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U24-ch53, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 58.52
Std Dev 7.71
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U24-ch53, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 5
Mean 62.2
Std Dev 0.7483
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U24-ch53, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch54, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 92
Mean 23.82
Std Dev 11.82
Entry
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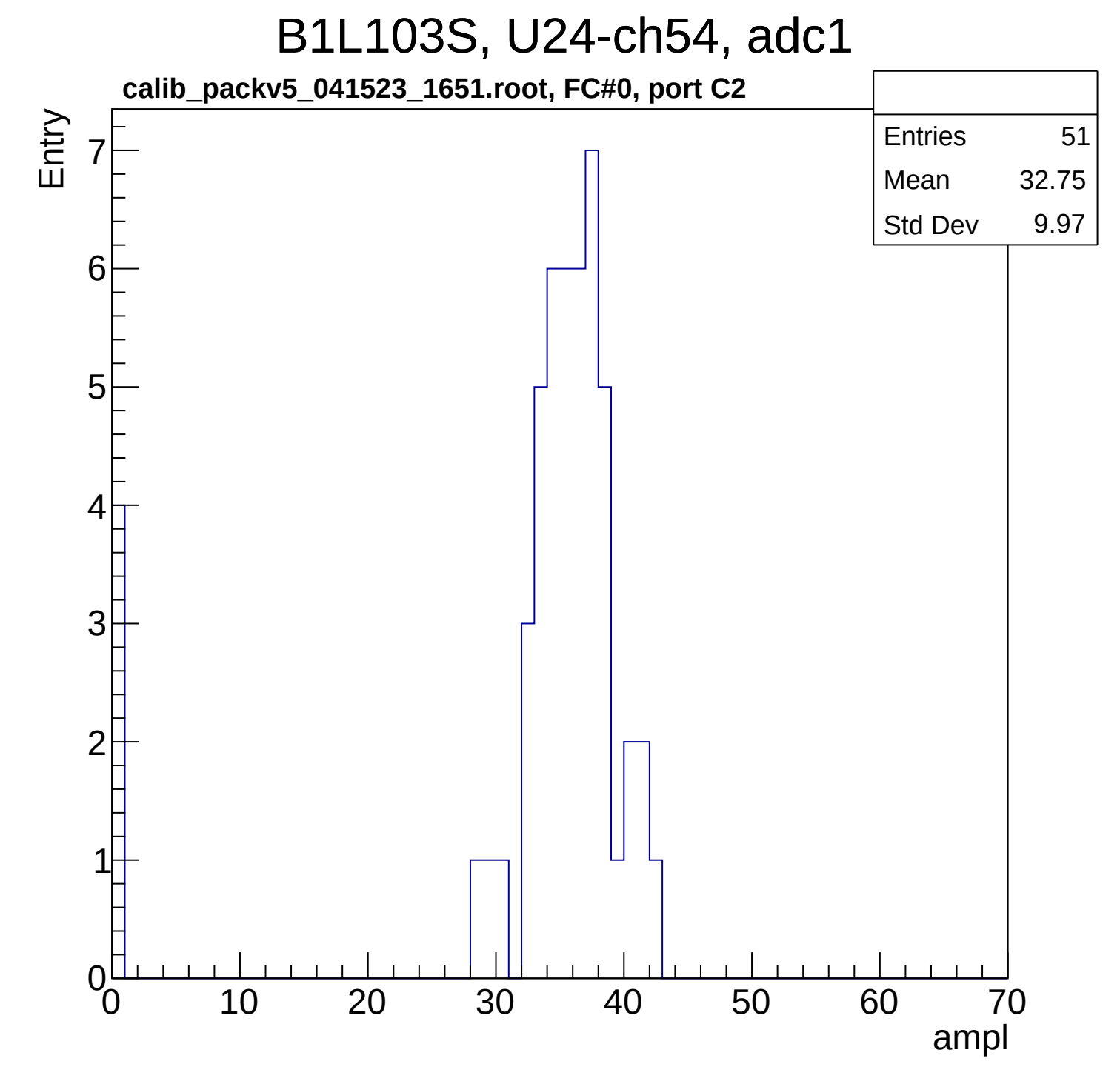
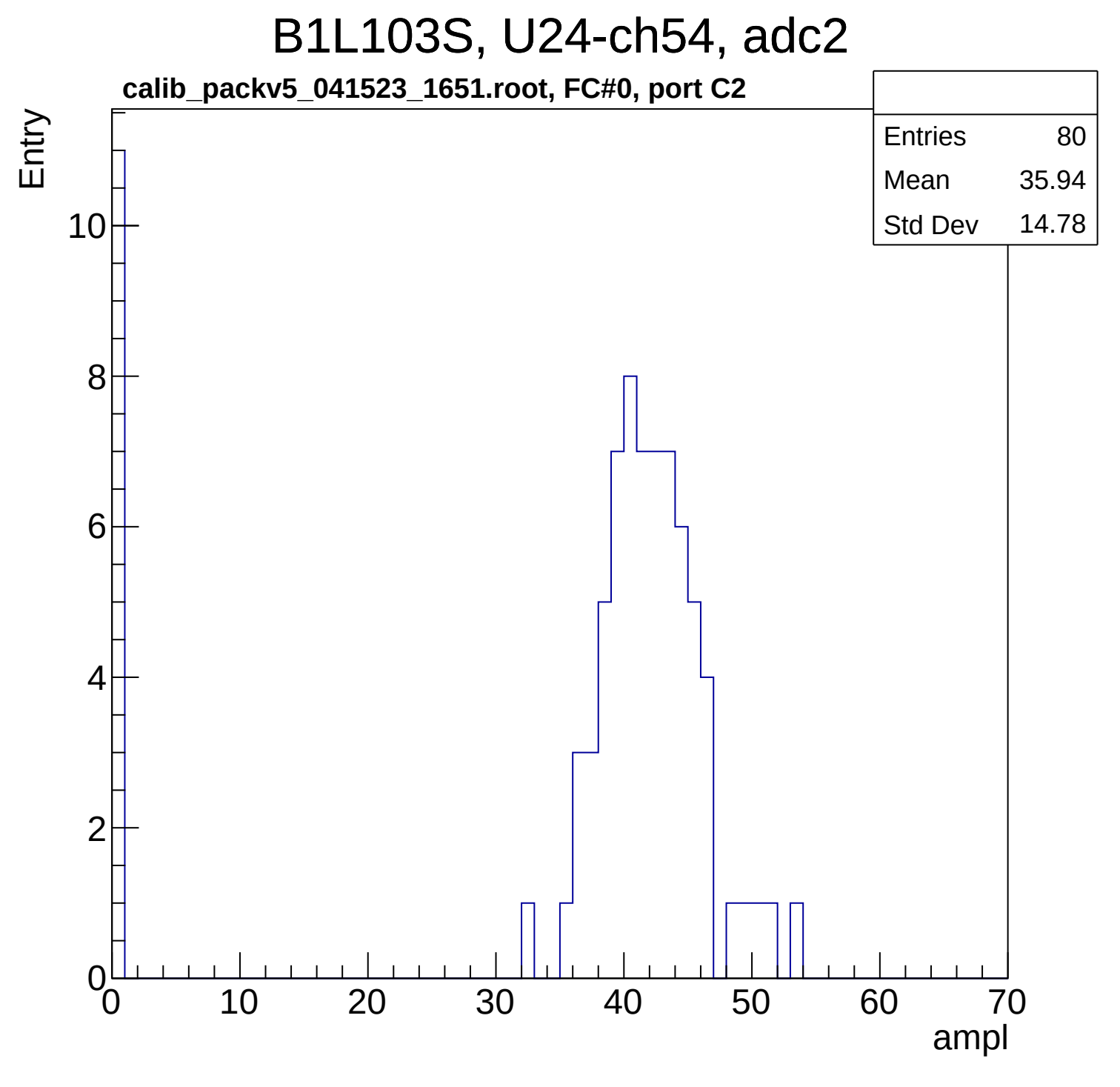
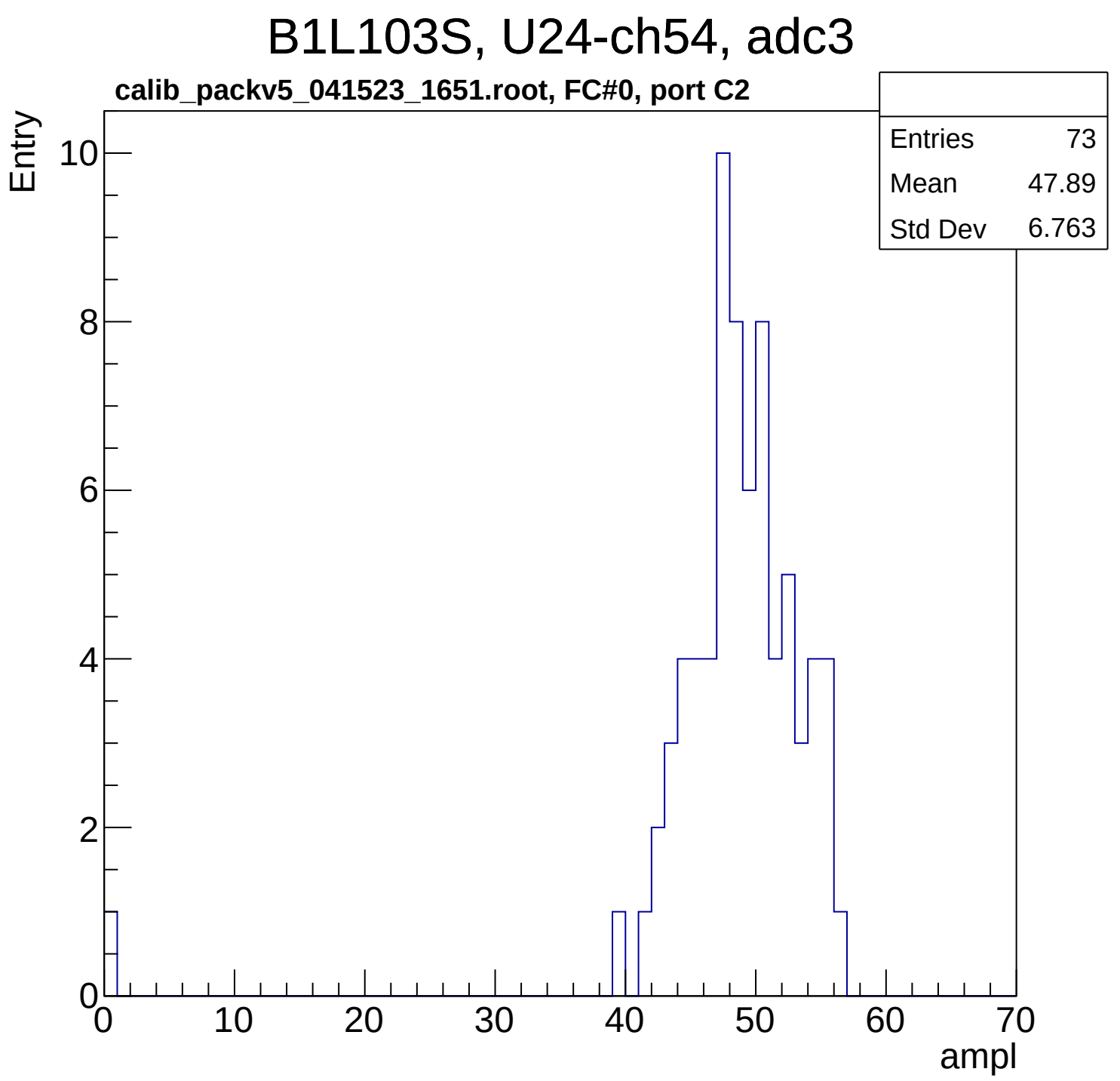
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch54, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 32.75
Std Dev 9.97
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U24-ch54, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 35.94
Std Dev 14.78
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch54, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 47.89
Std Dev 6.763
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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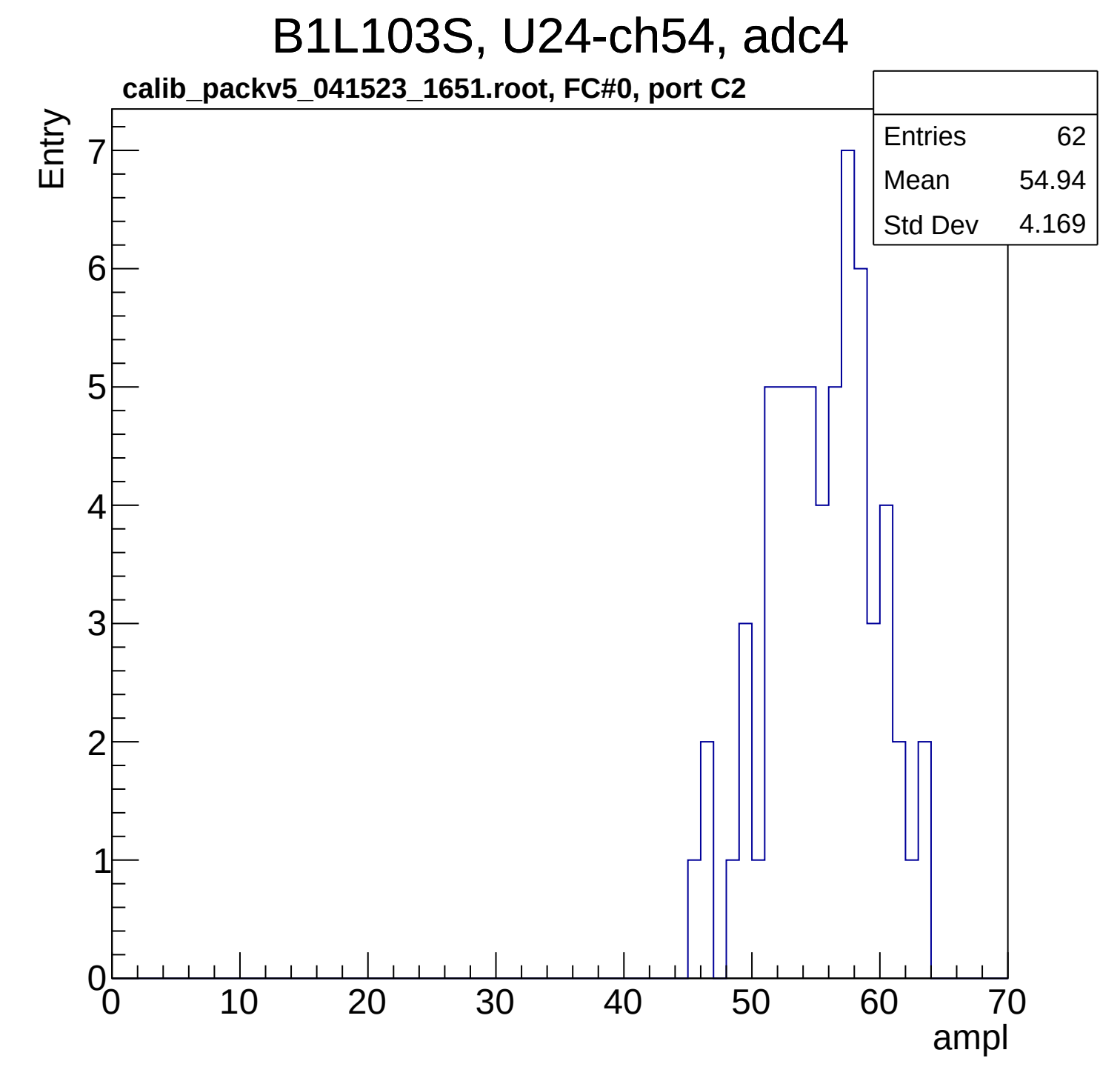
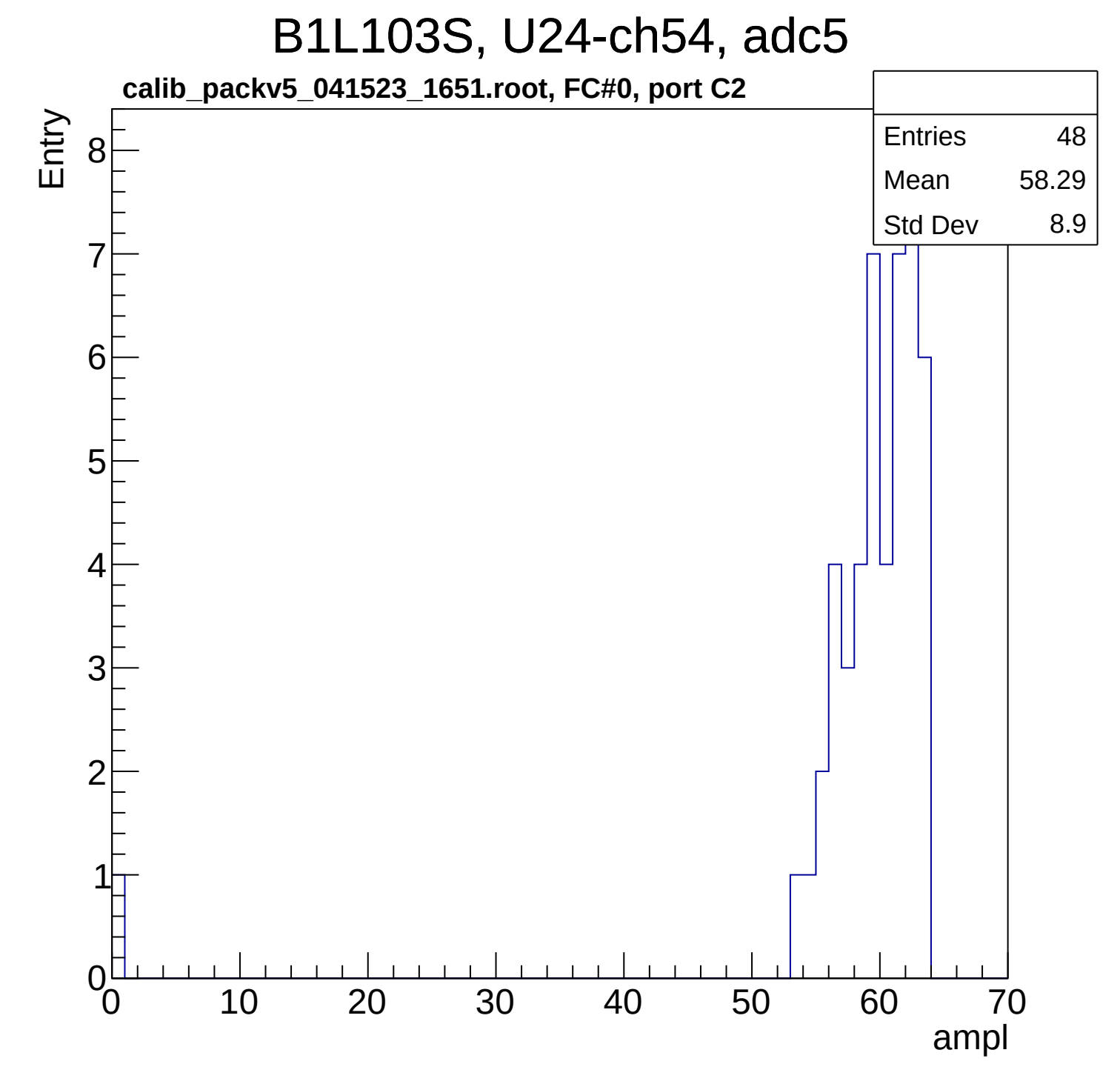

B1L103S, U24-ch54, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 54.94
Std Dev 4.169
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U24-ch54, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 58.29
Std Dev 8.9
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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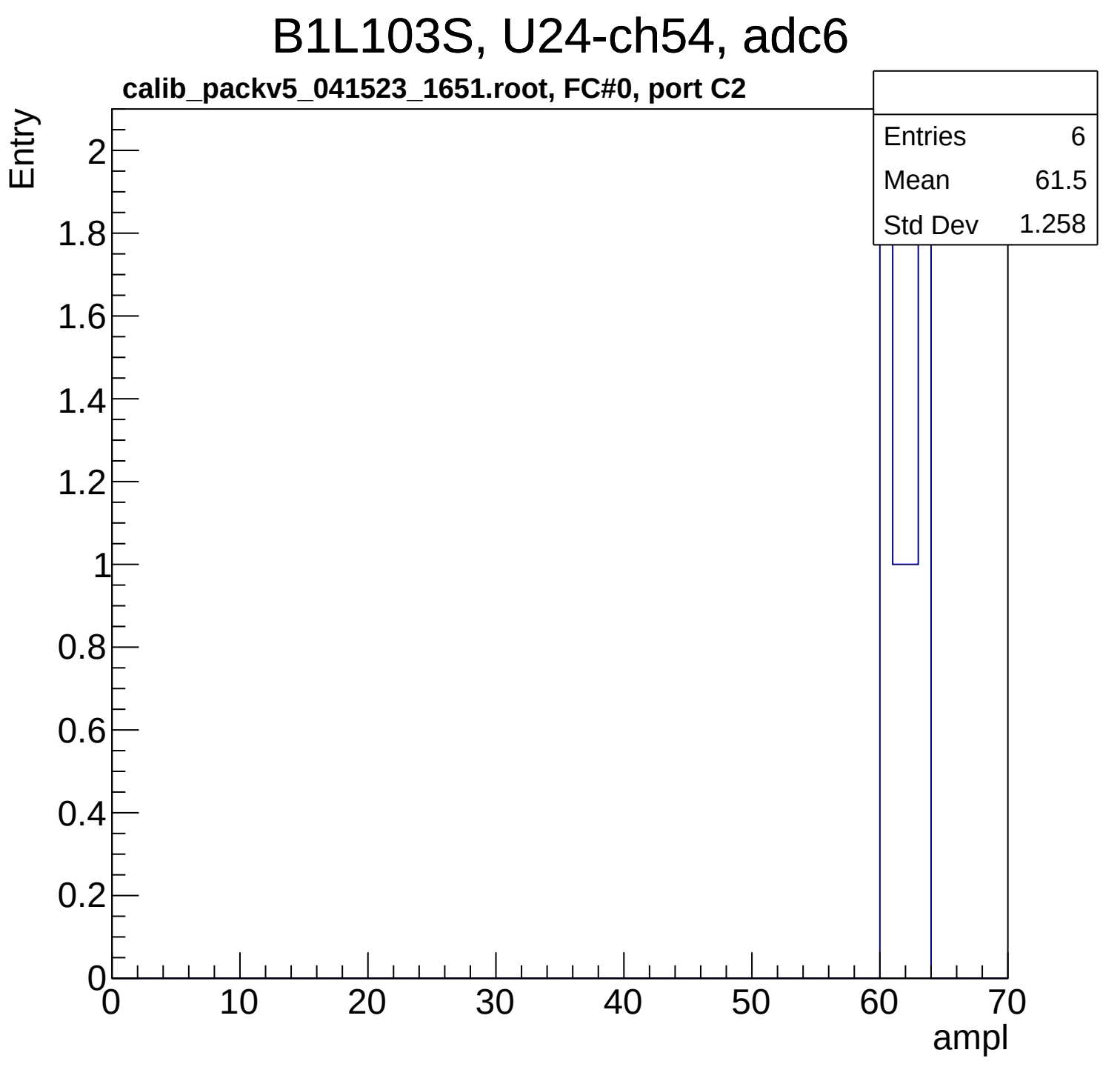
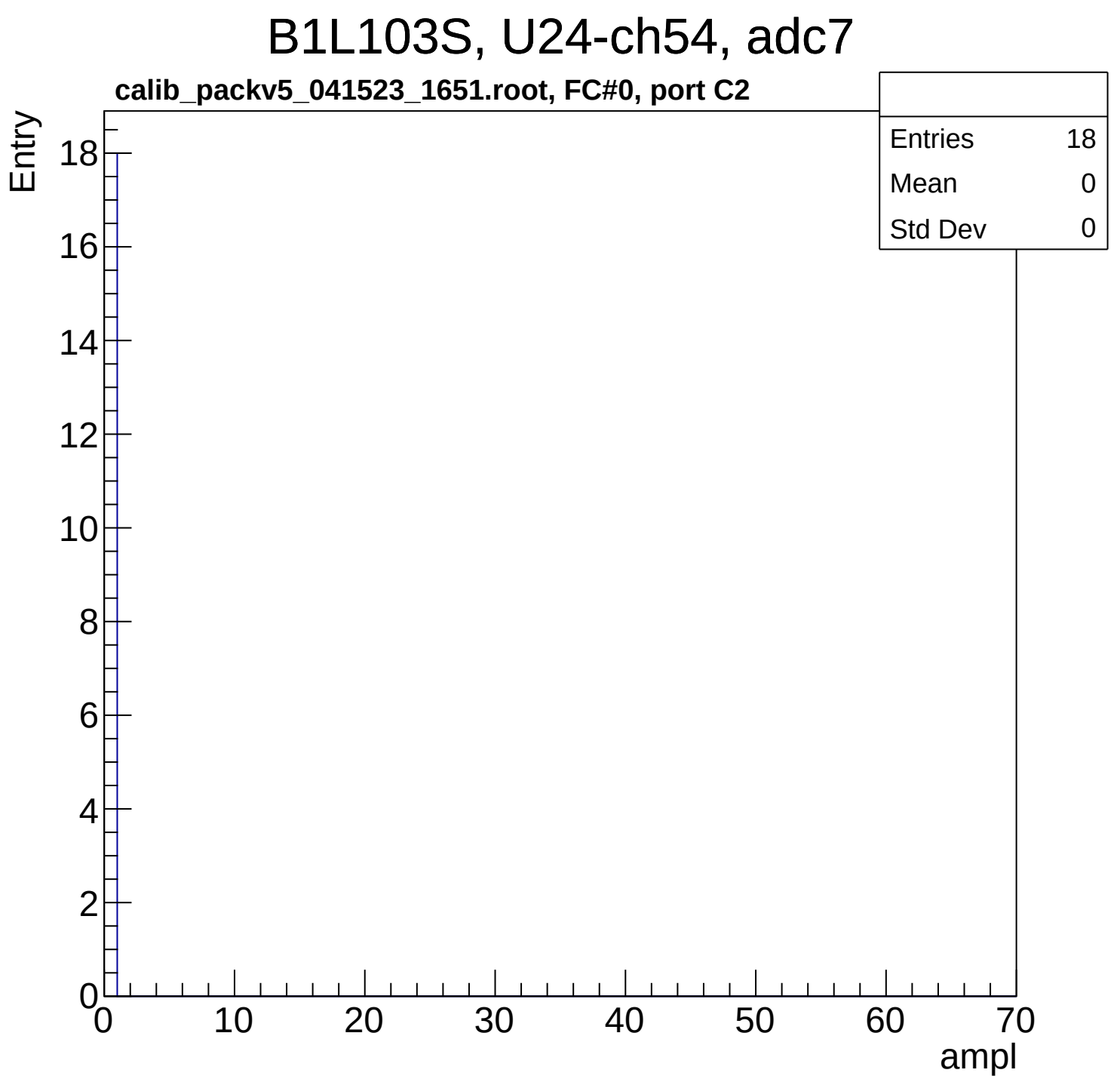
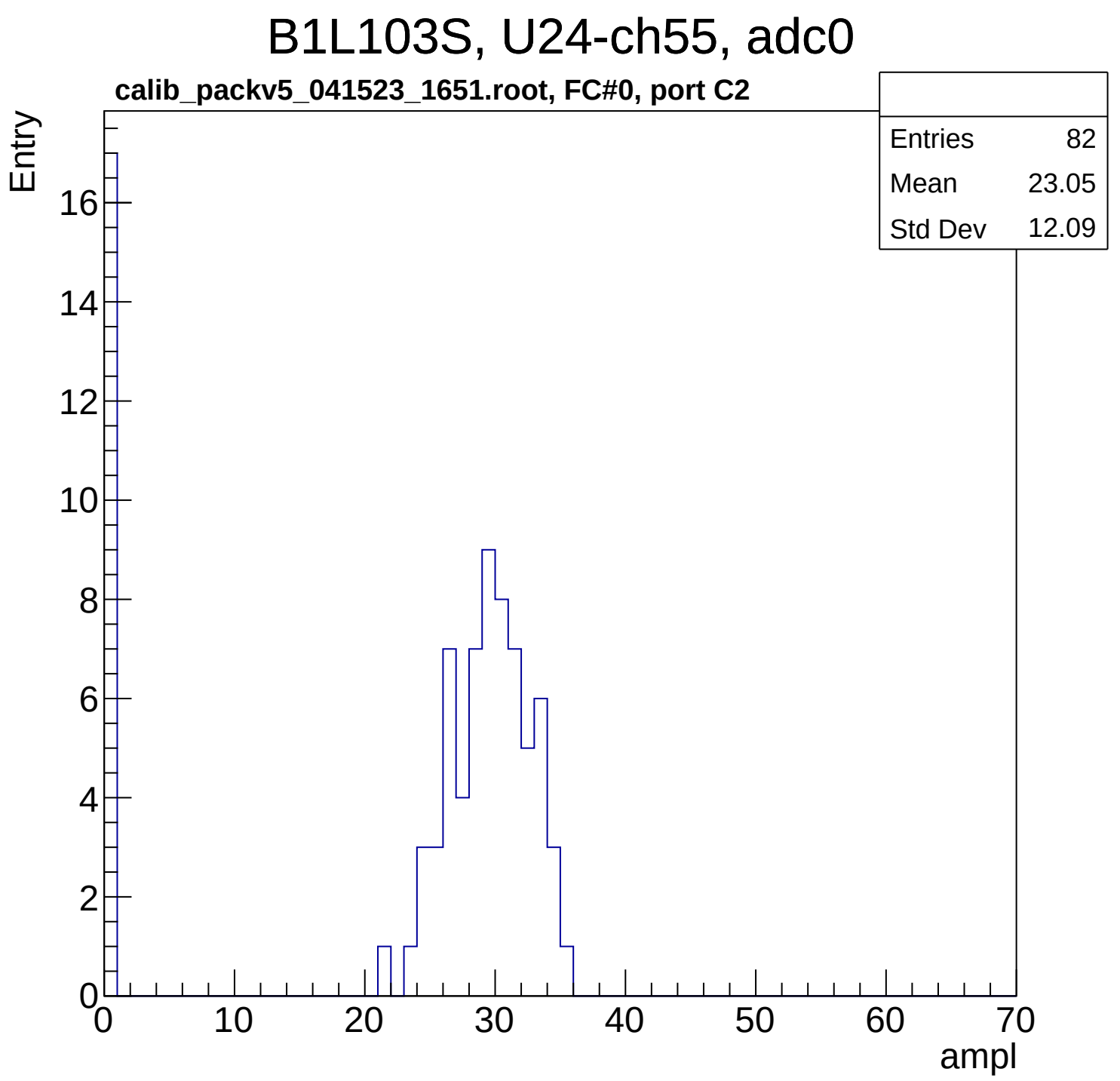
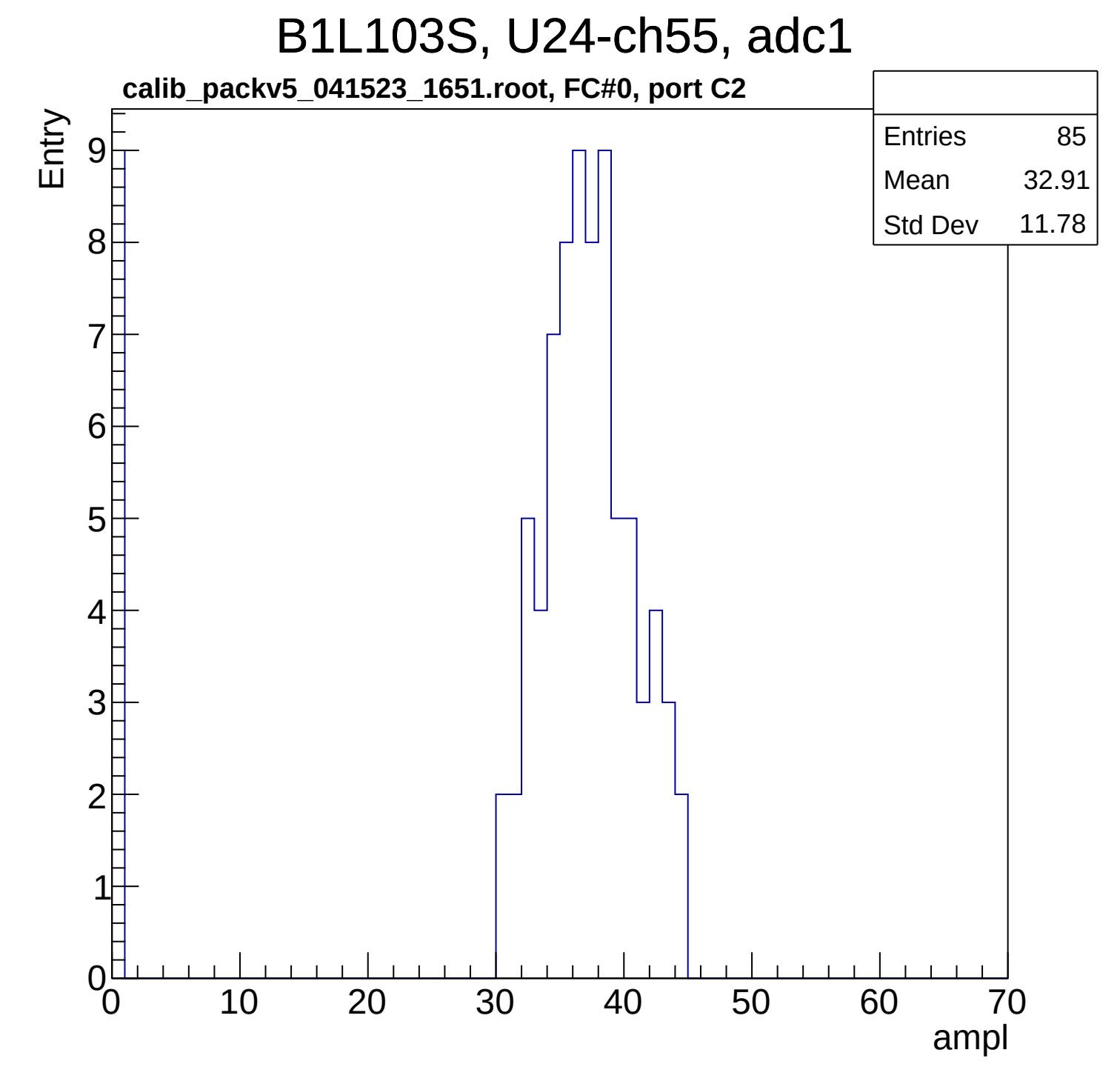
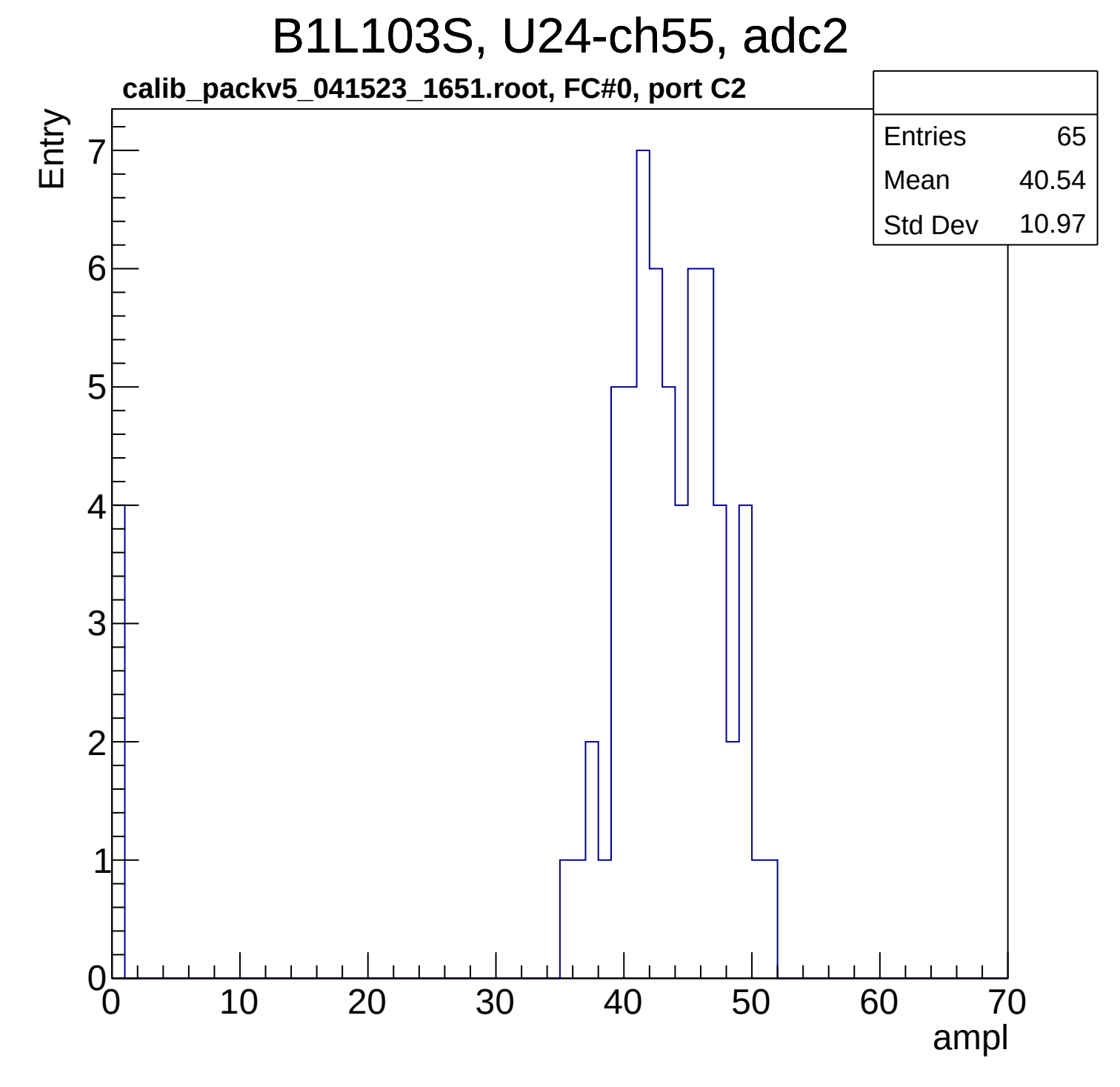
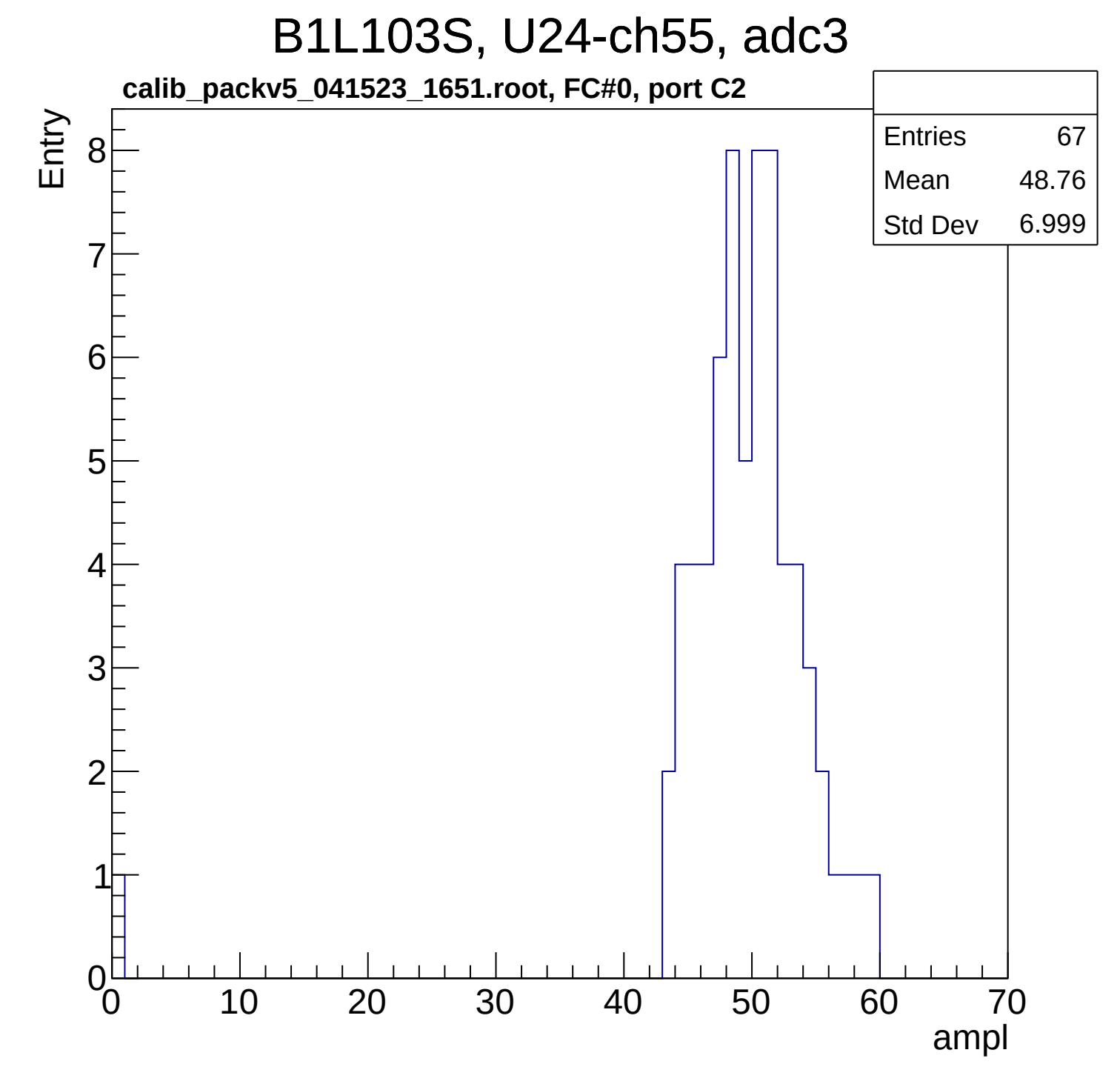

B1L103S, U24-ch54, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 61.5
Std Dev 1.258
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

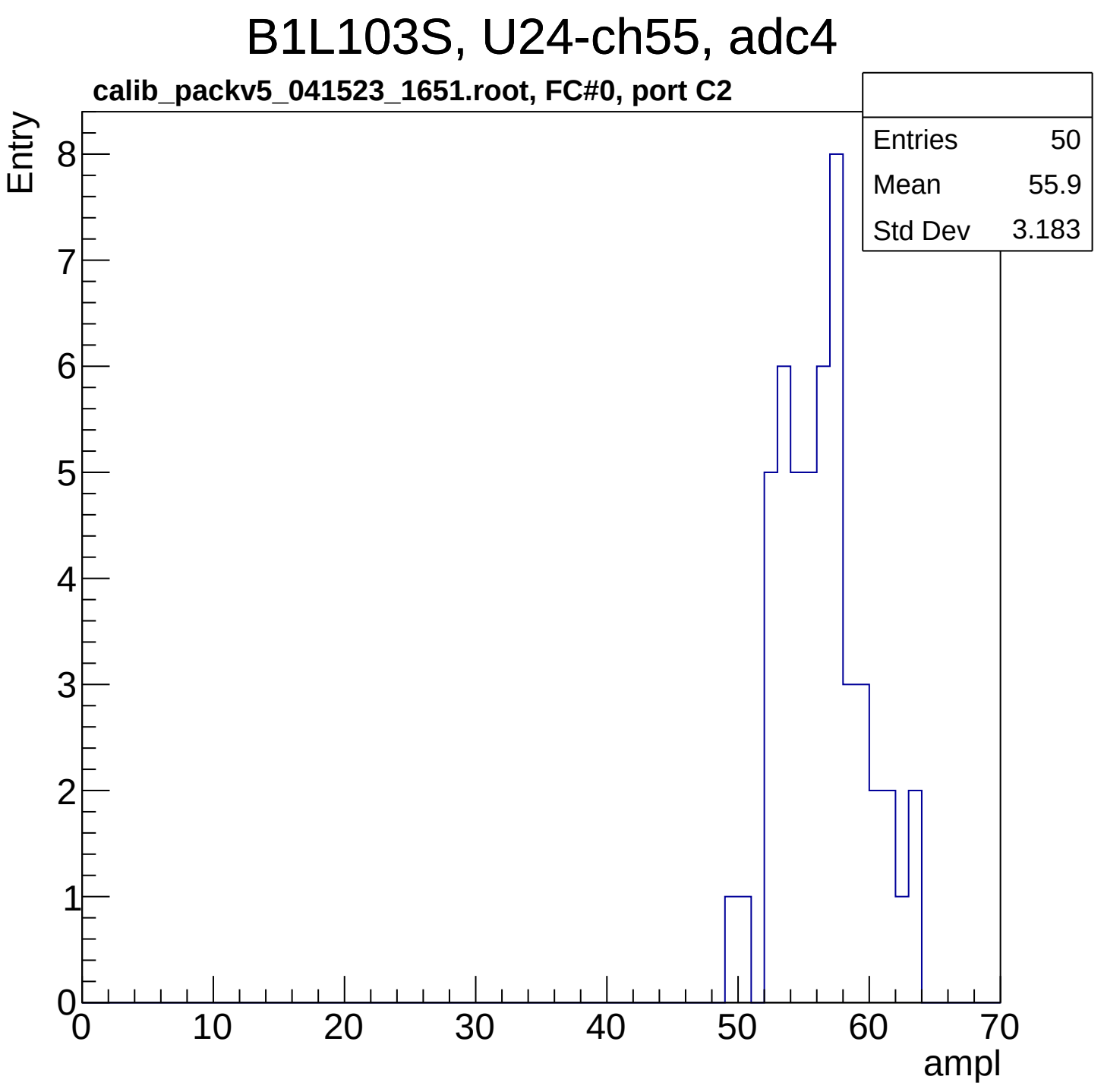

B1L103S, U24-ch54, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

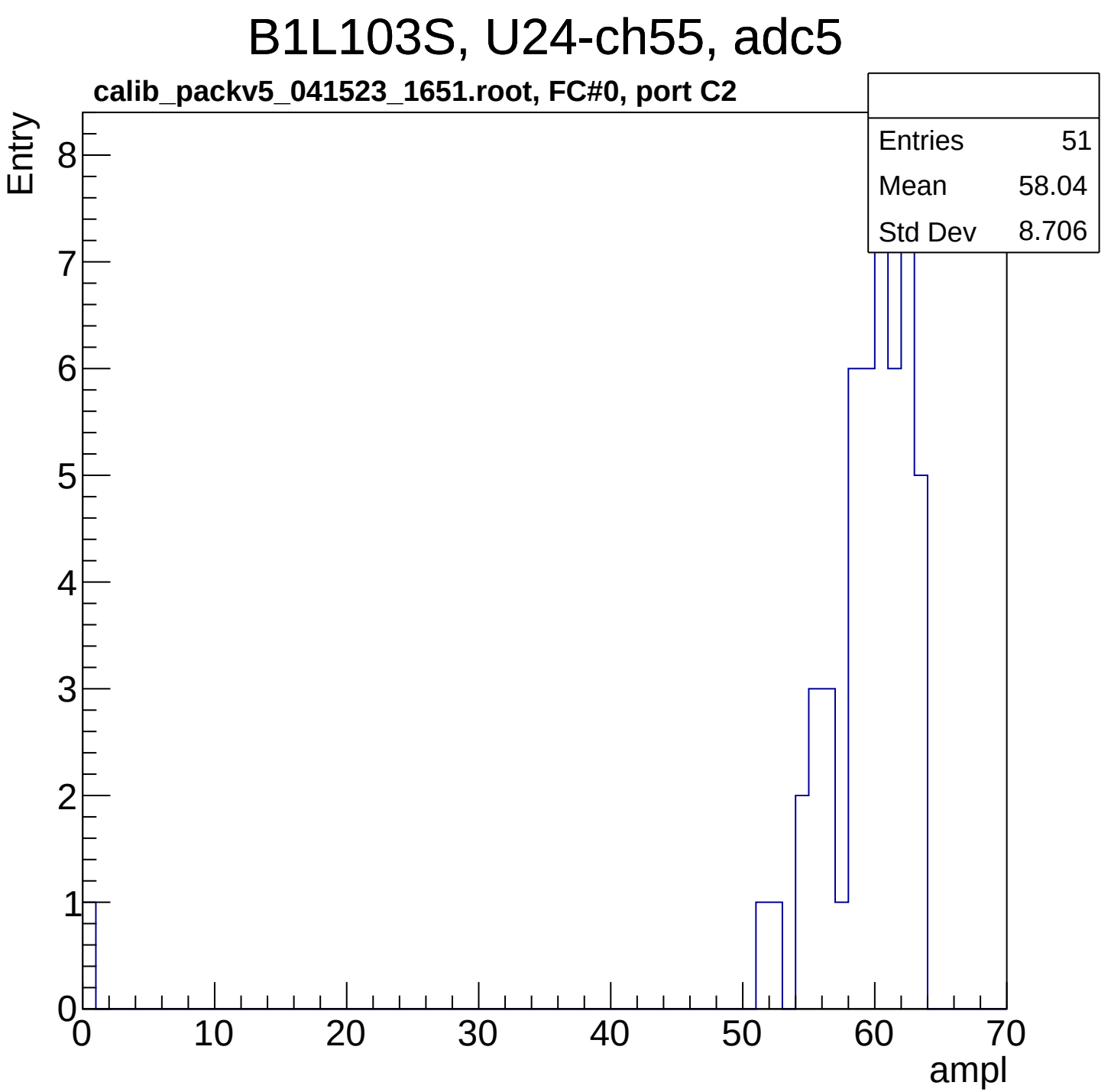

B1L103S, U24-ch55, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 23.05
Std Dev 12.09
Entry
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch55, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 32.91
Std Dev 11.78
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U24-ch55, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 40.54
Std Dev 10.97
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U24-ch55, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 48.76
Std Dev 6.999
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U24-ch55, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 55.9
Std Dev 3.183
Entry
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch55, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 58.04
Std Dev 8.706
Entry
ampl
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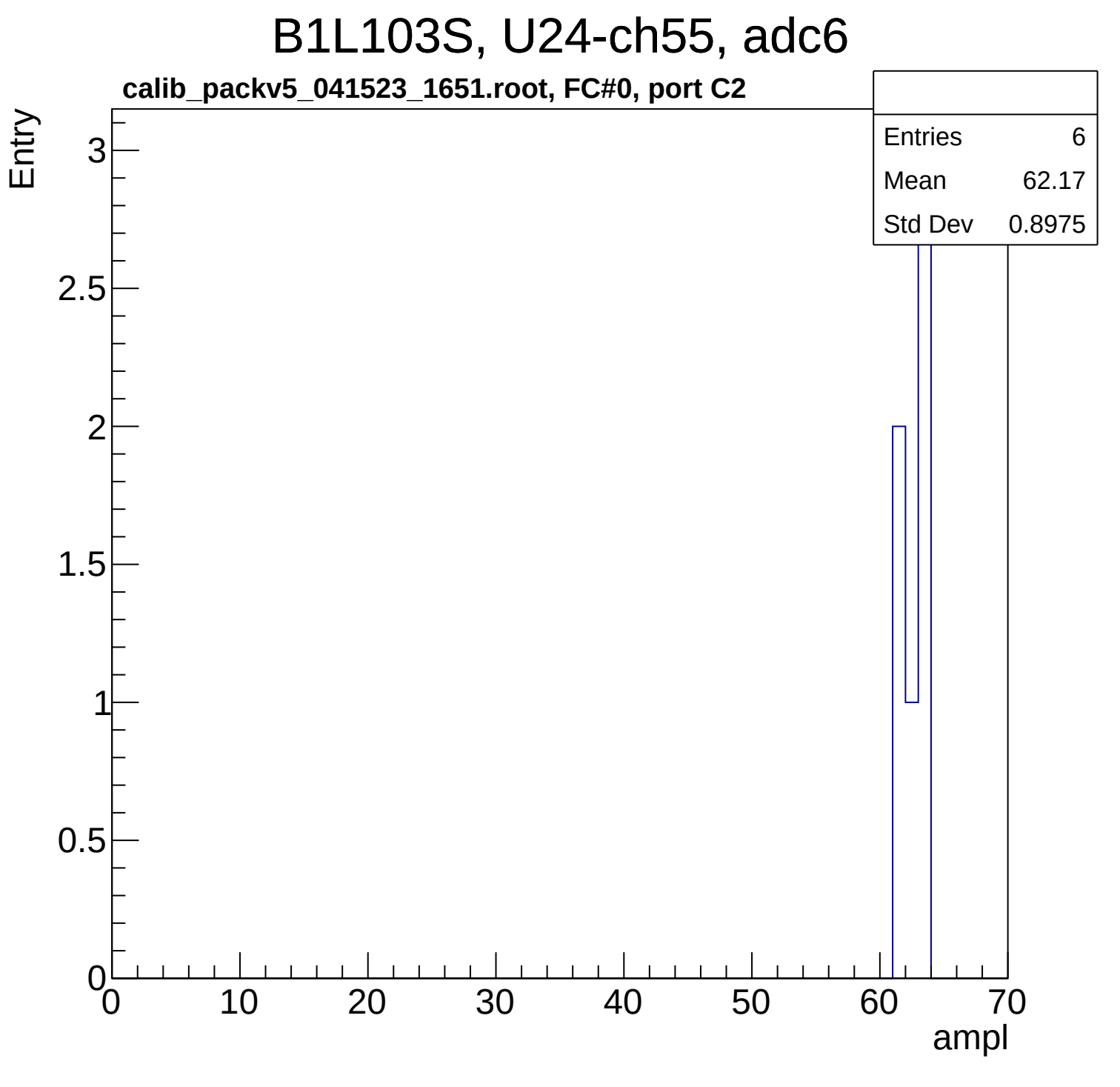
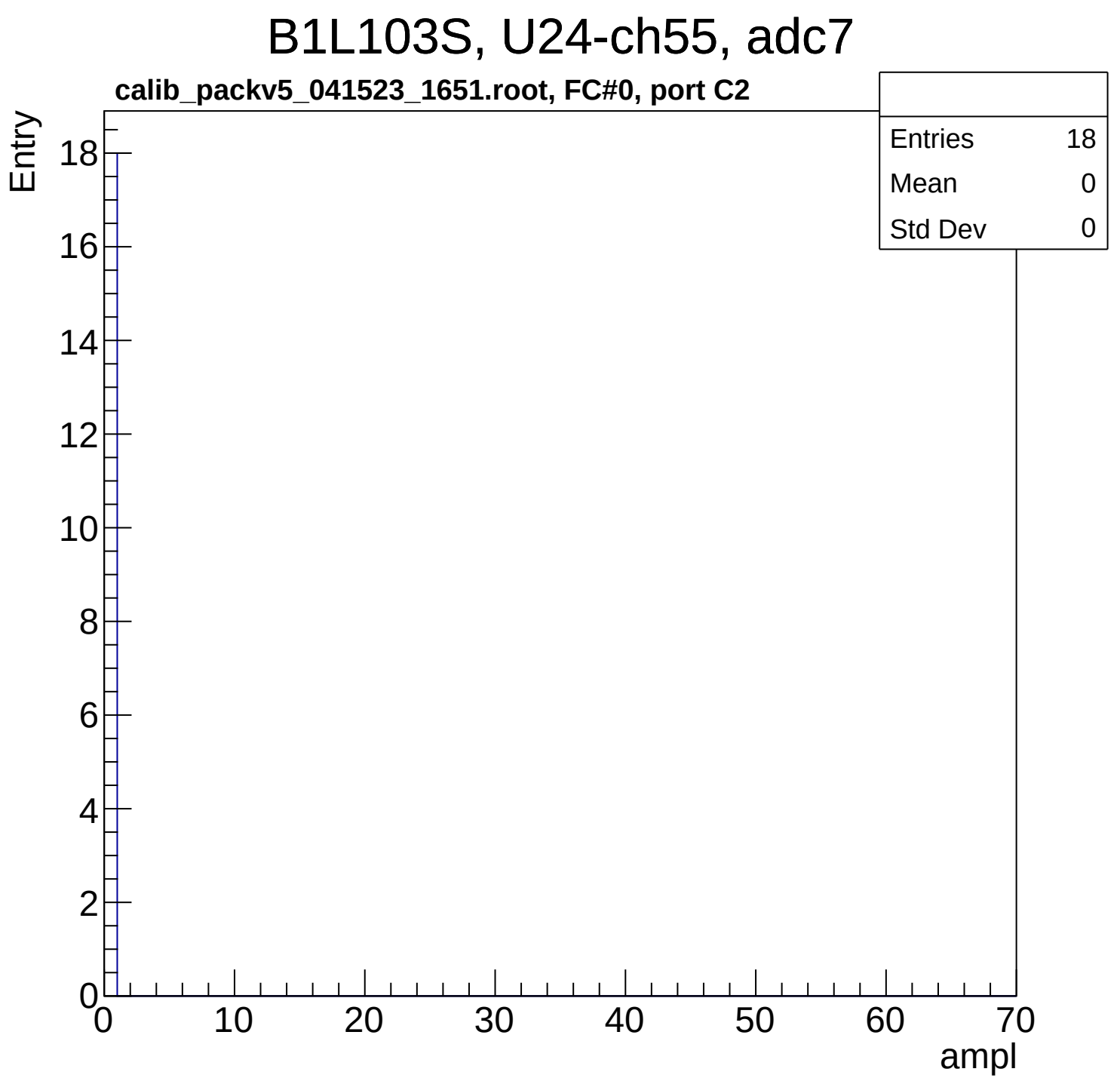
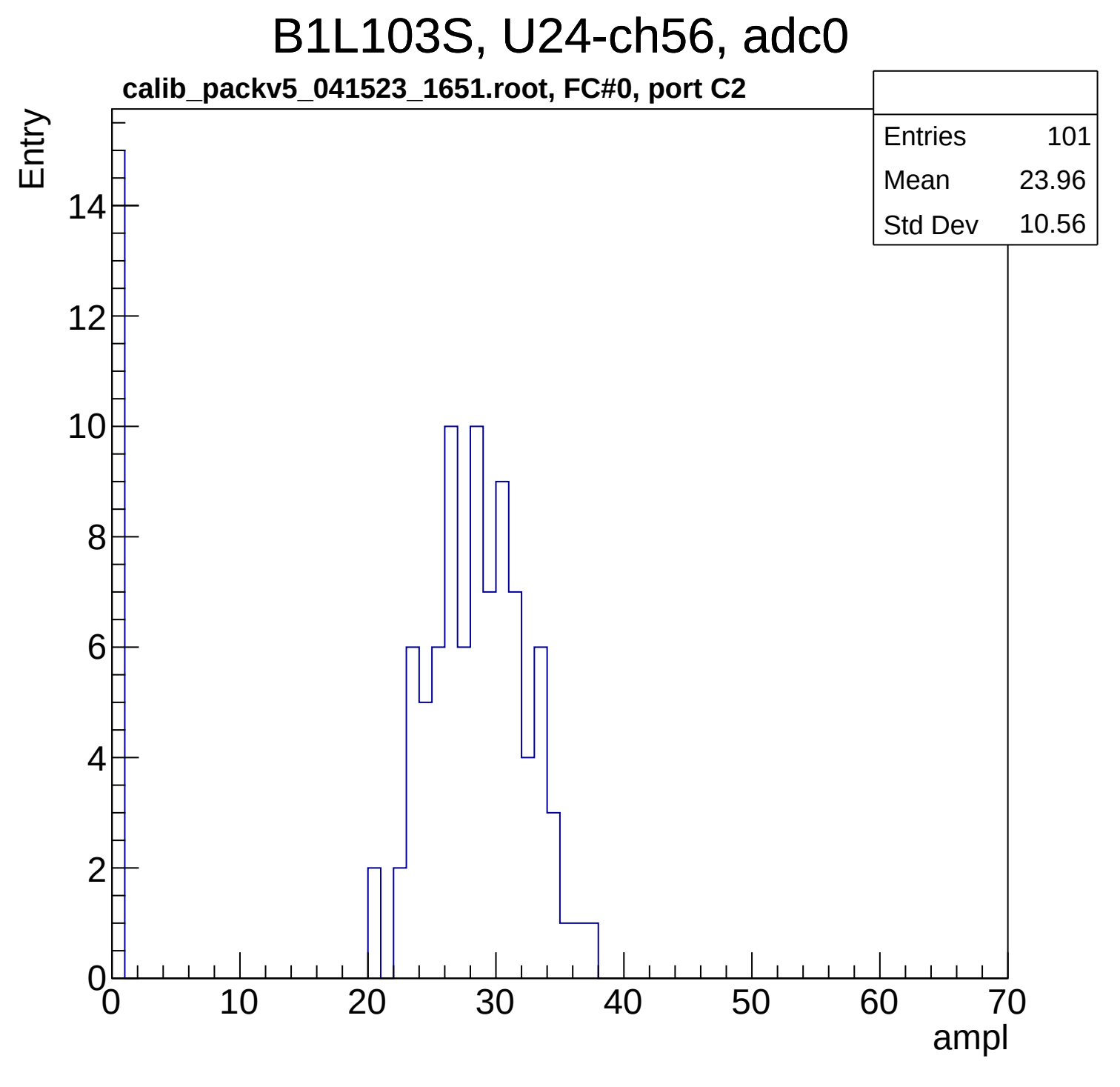
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U24-ch55, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 62.17
Std Dev 0.8975
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U24-ch55, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch56, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 101
Mean 23.96
Std Dev 10.56
Entry
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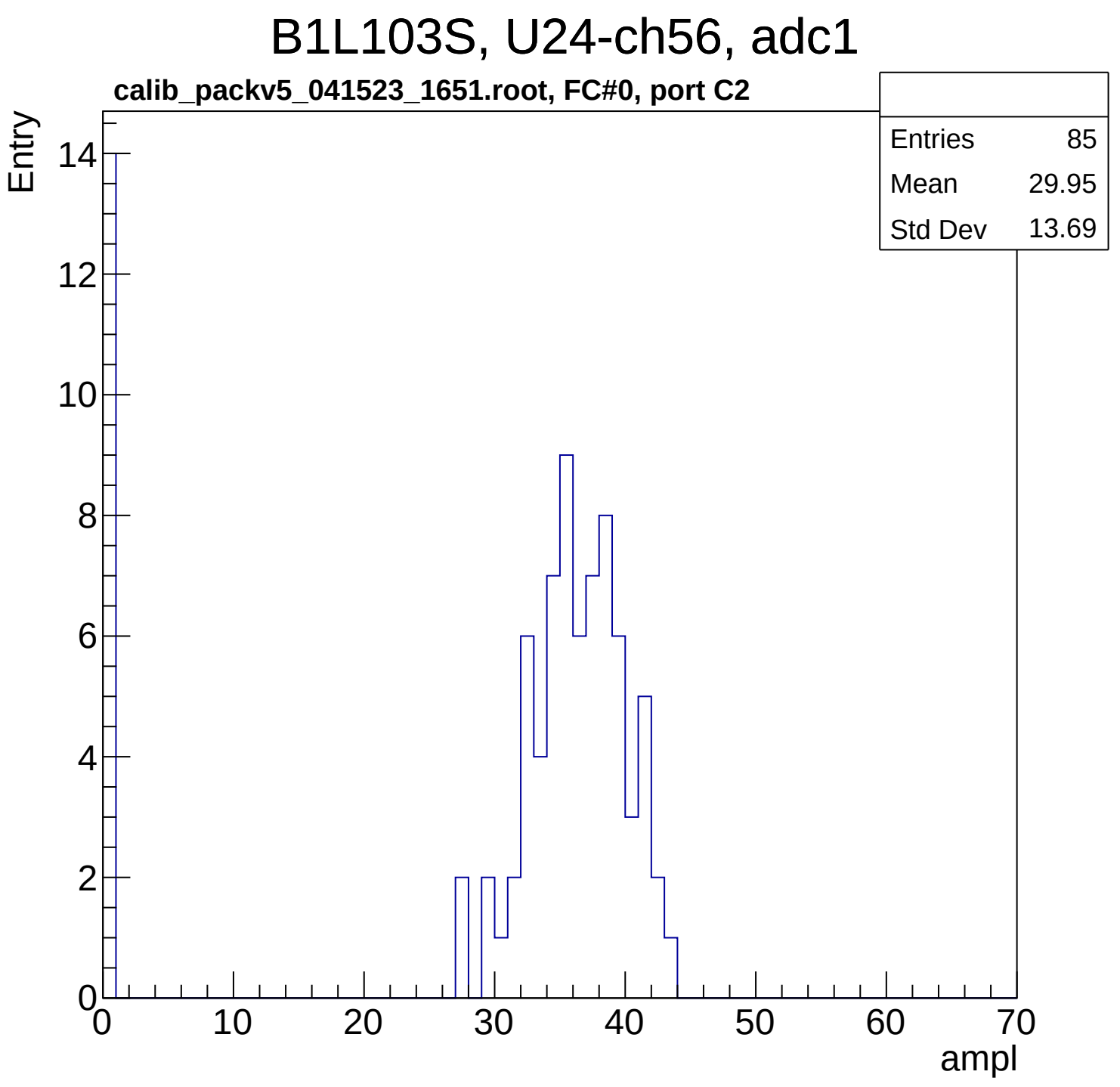
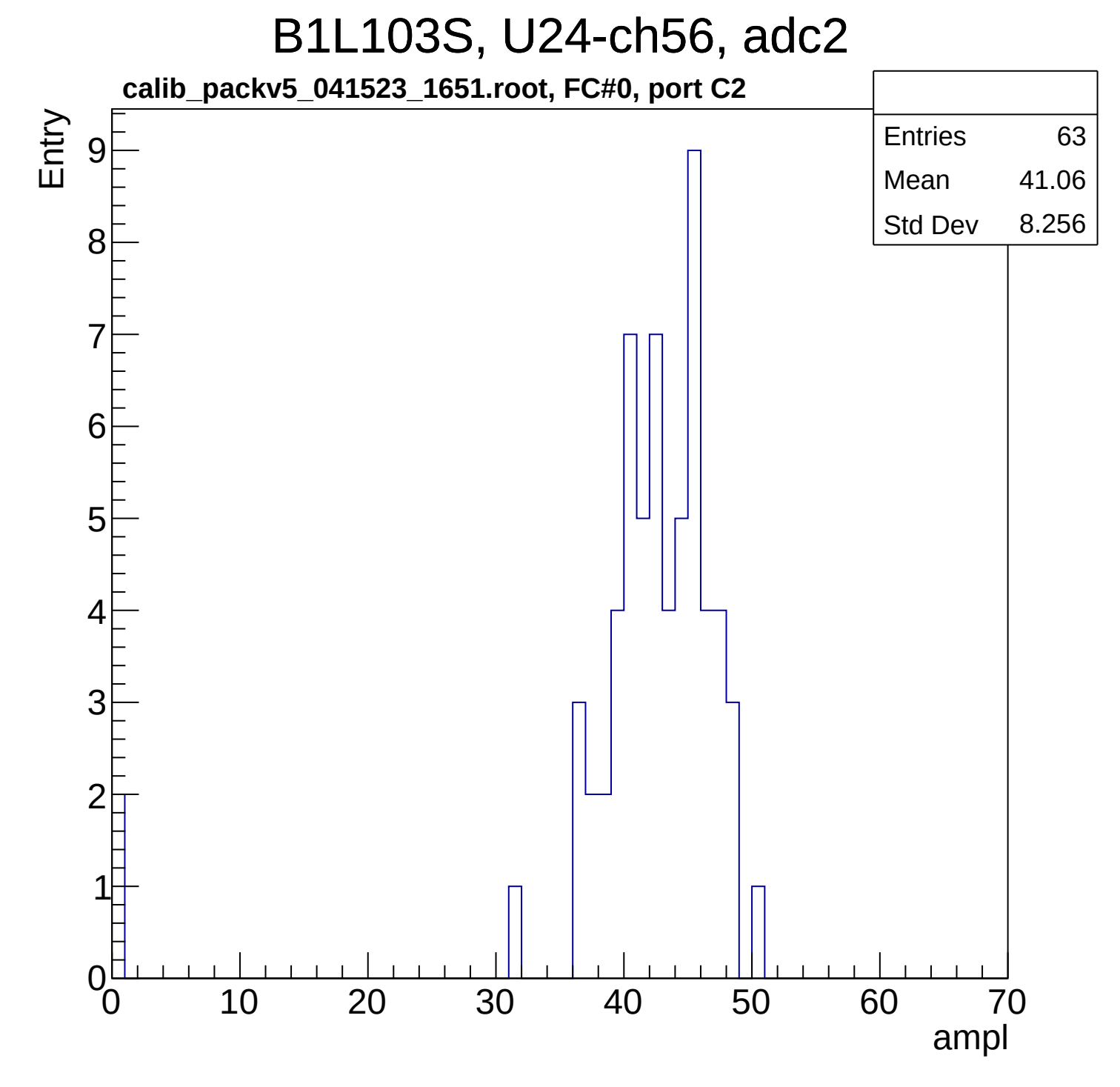
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch56, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 29.95
Std Dev 13.69
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L103S, U24-ch56, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 41.06
Std Dev 8.256
Entry
ampl
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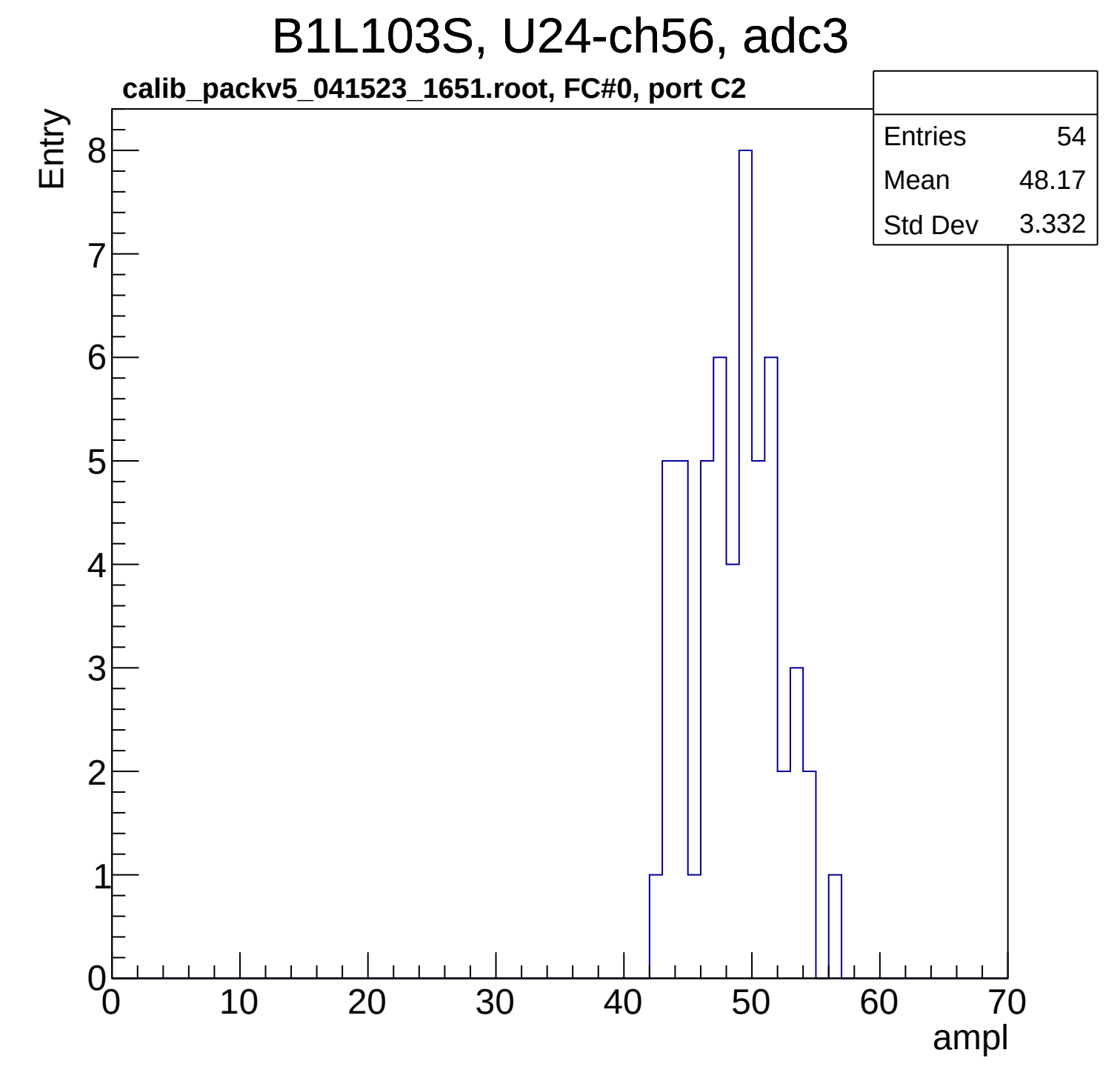
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U24-ch56, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 48.17
Std Dev 3.332
Entry
ampl
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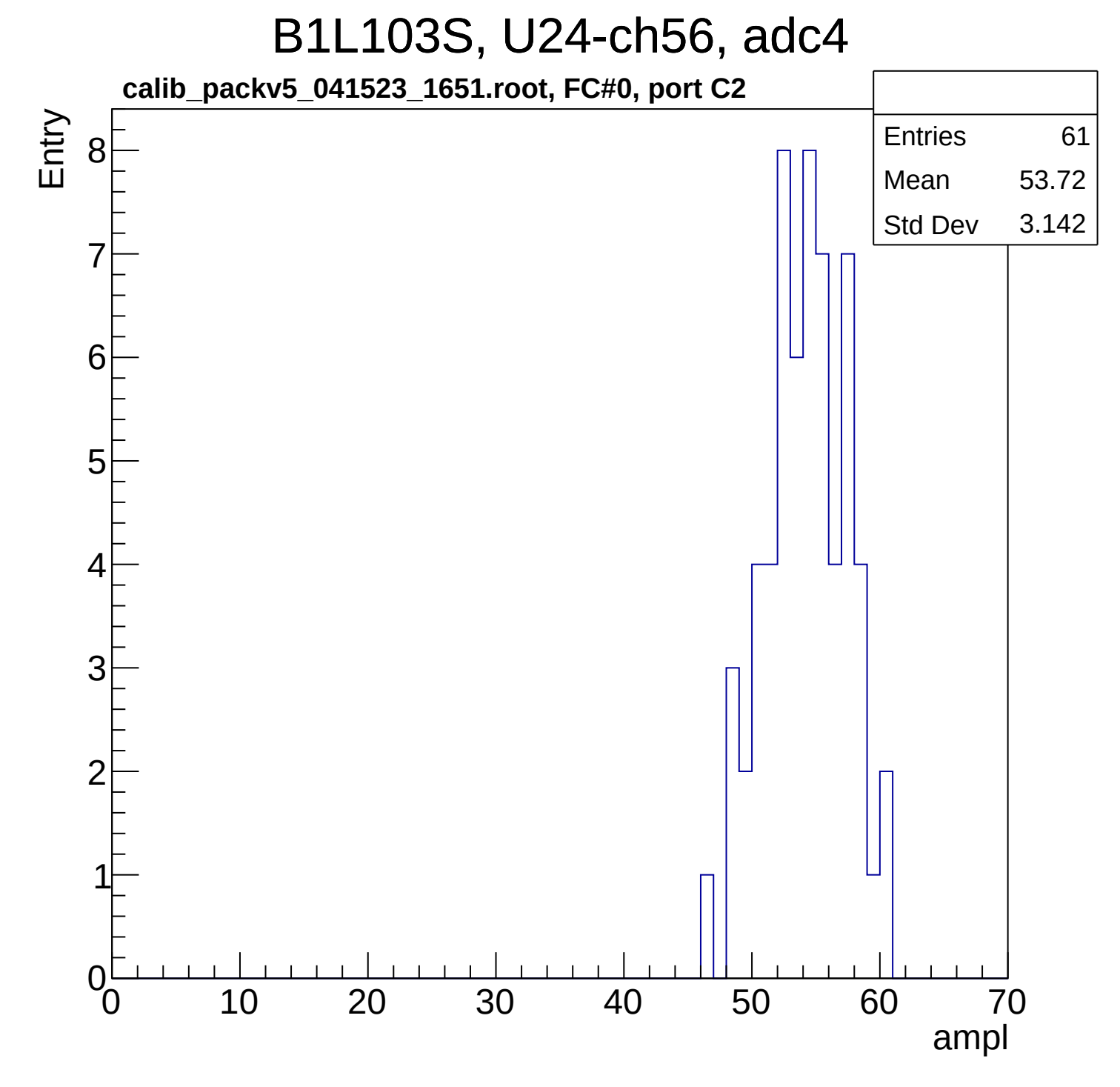
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U24-ch56, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 53.72
Std Dev 3.142
Entry
ampl
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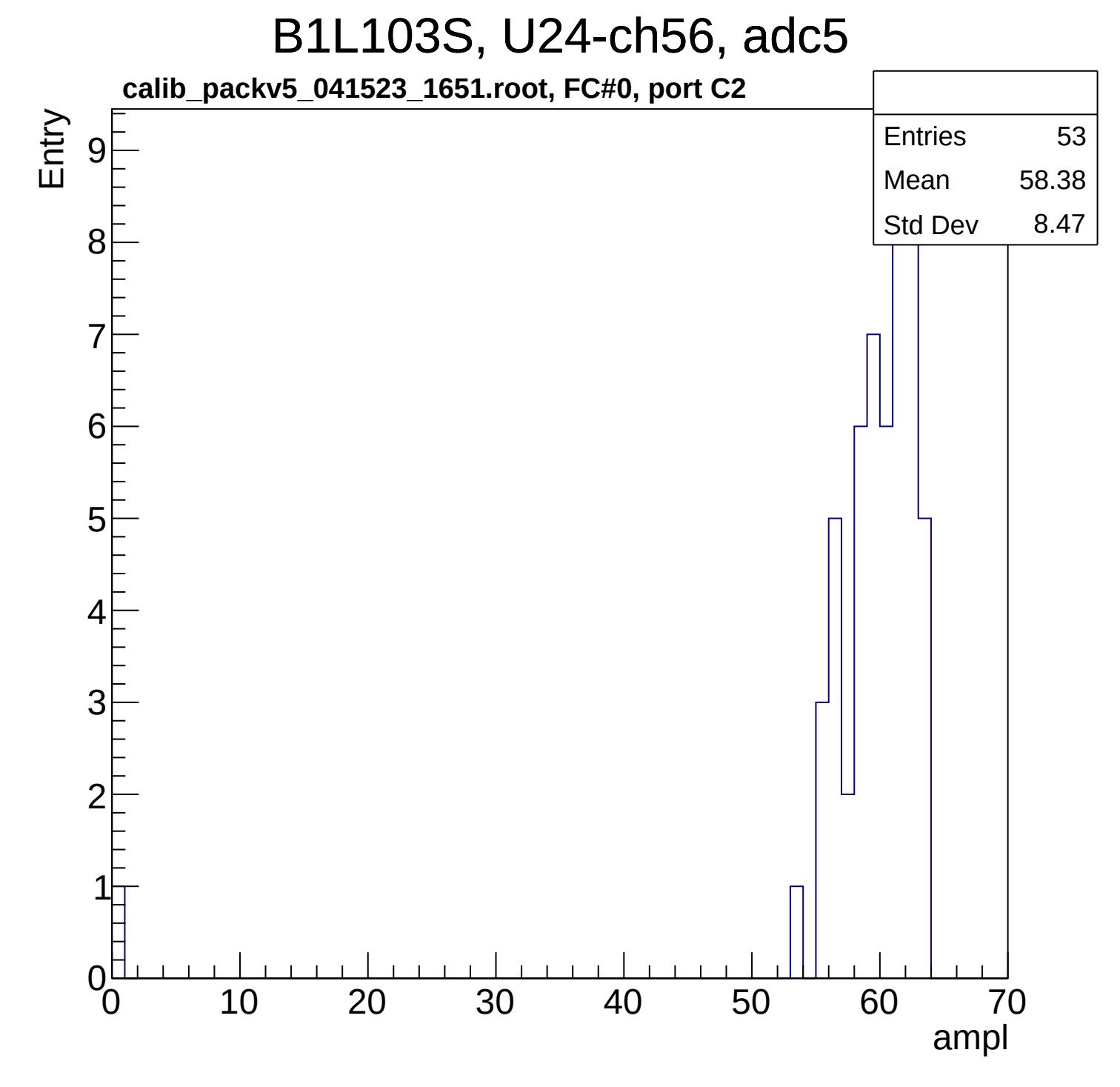
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U24-ch56, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 58.38
Std Dev 8.47
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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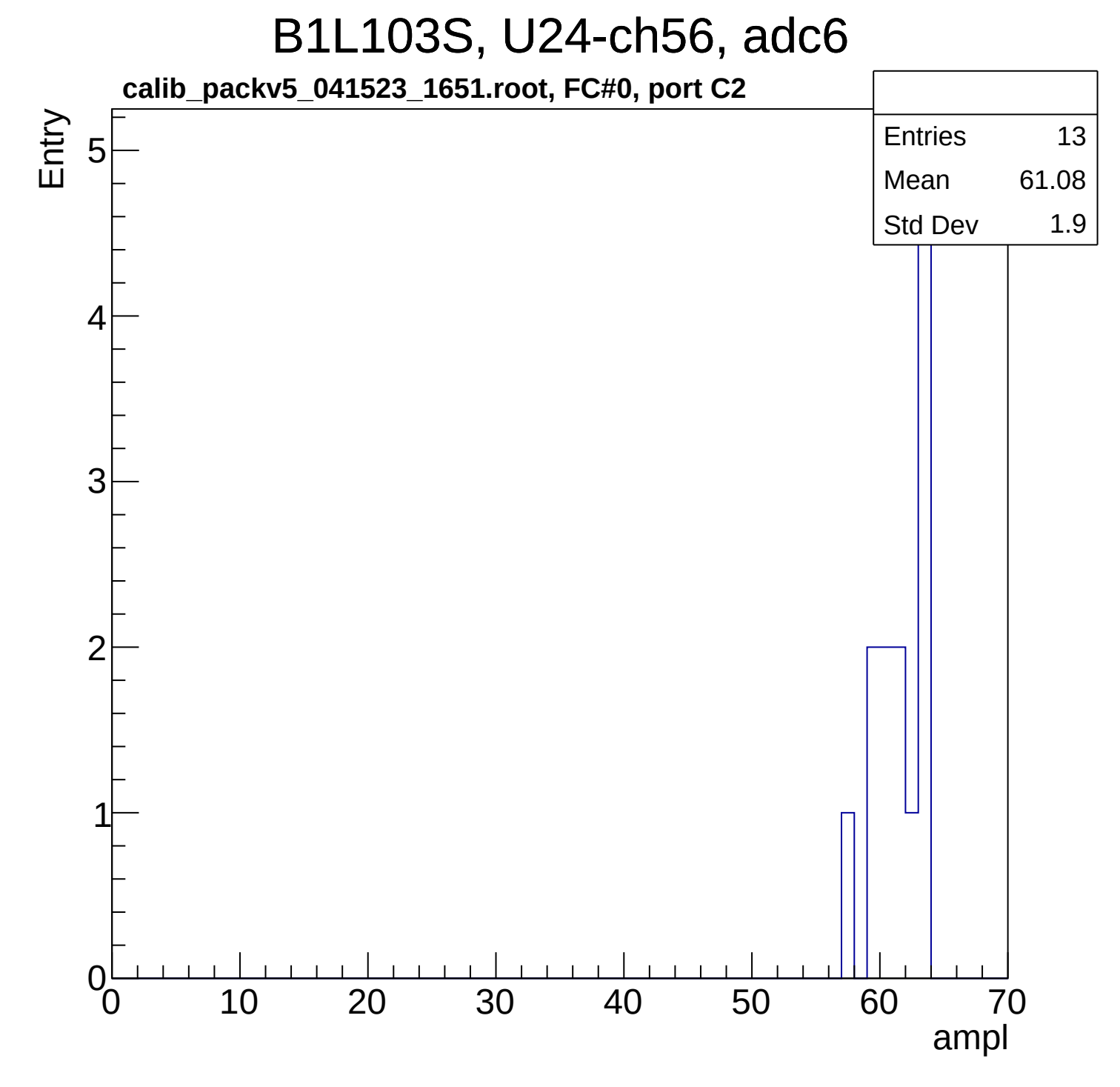
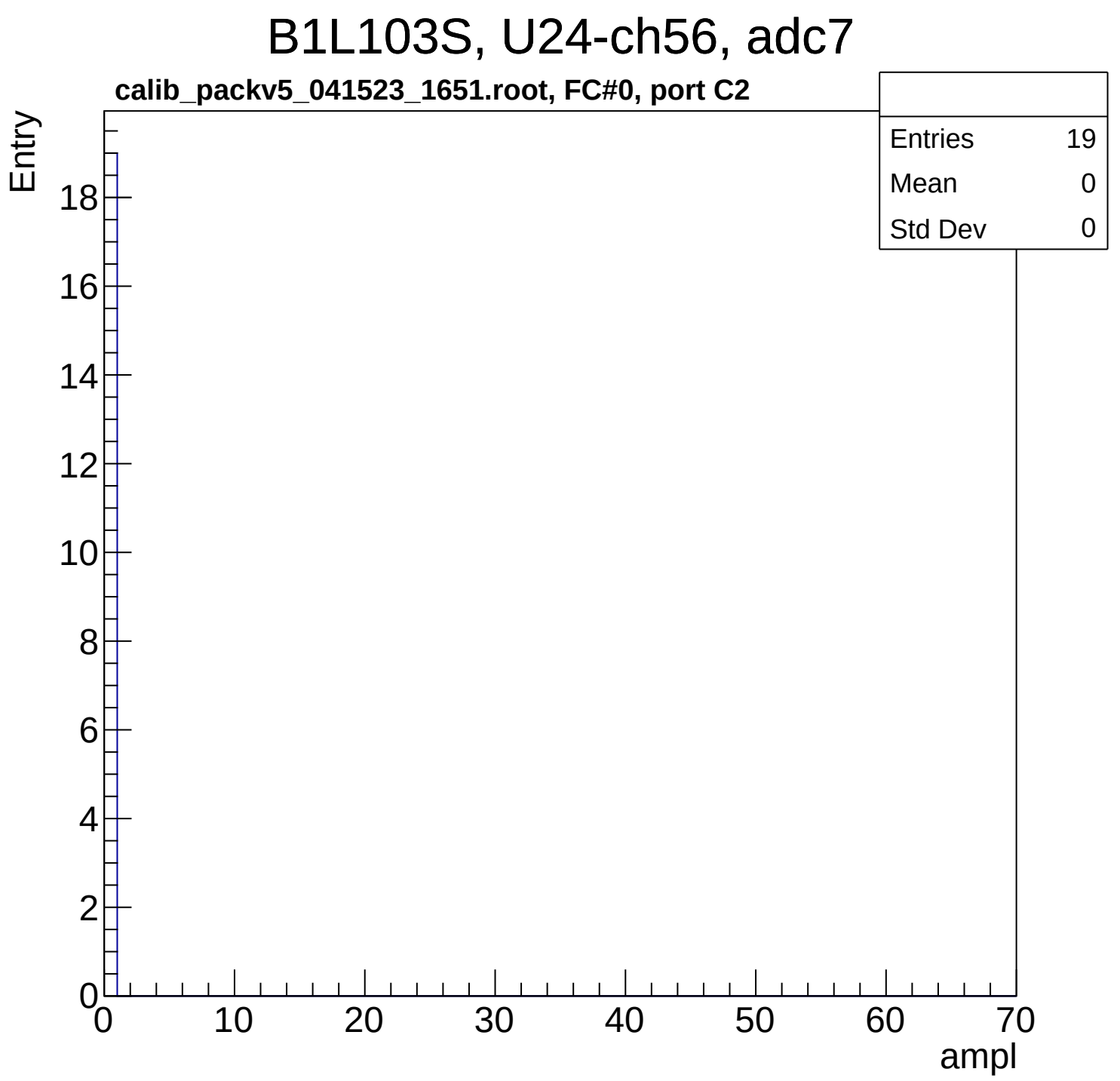
40
50
60
70


B1L103S, U24-ch56, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 13
Mean 61.08
Std Dev 1.9
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch56, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
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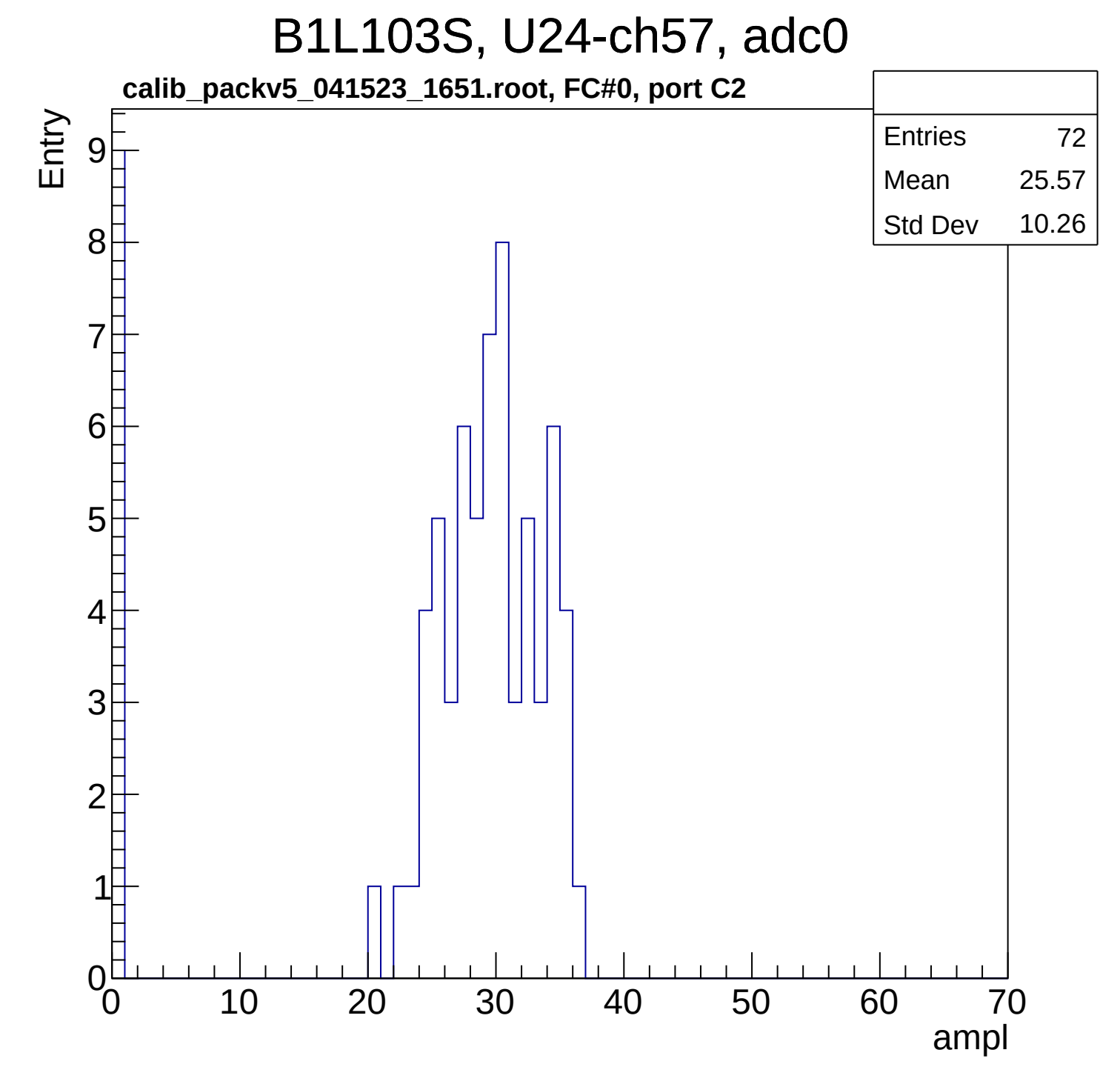
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch57, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 25.57
Std Dev 10.26
Entry
ampl
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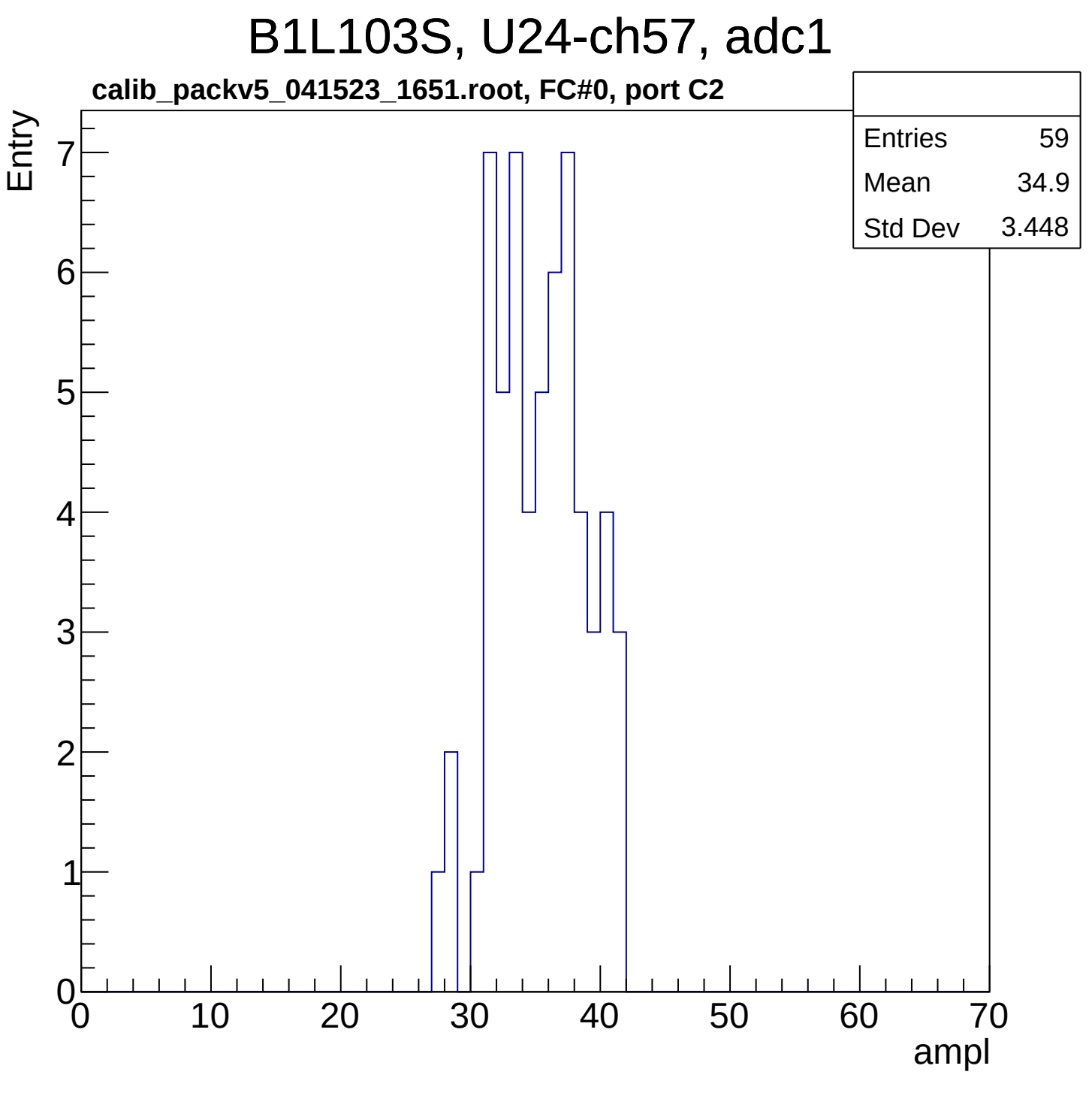
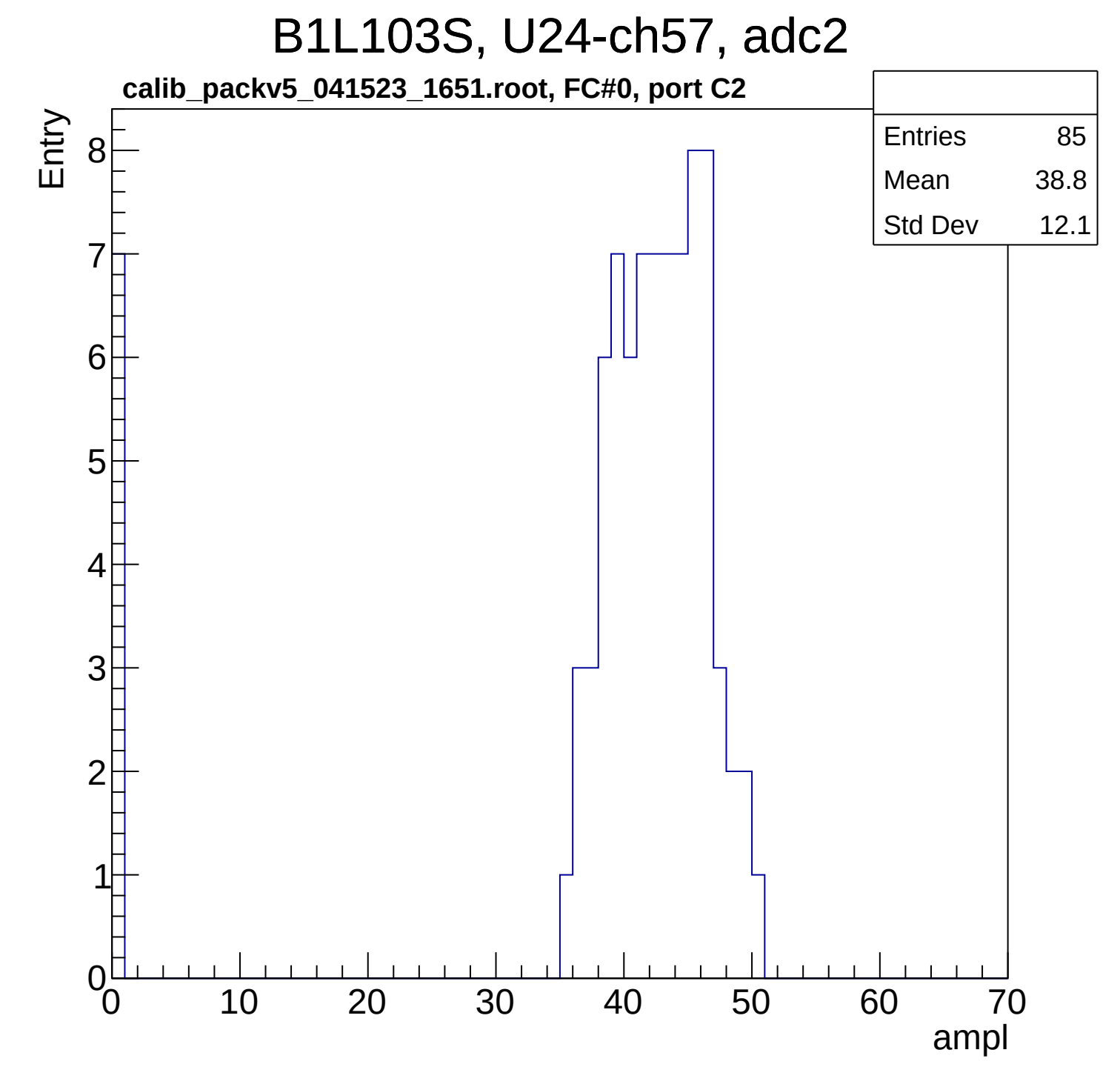
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U24-ch57, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 34.9
Std Dev 3.448
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U24-ch57, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 38.8
Std Dev 12.1
Entry
ampl
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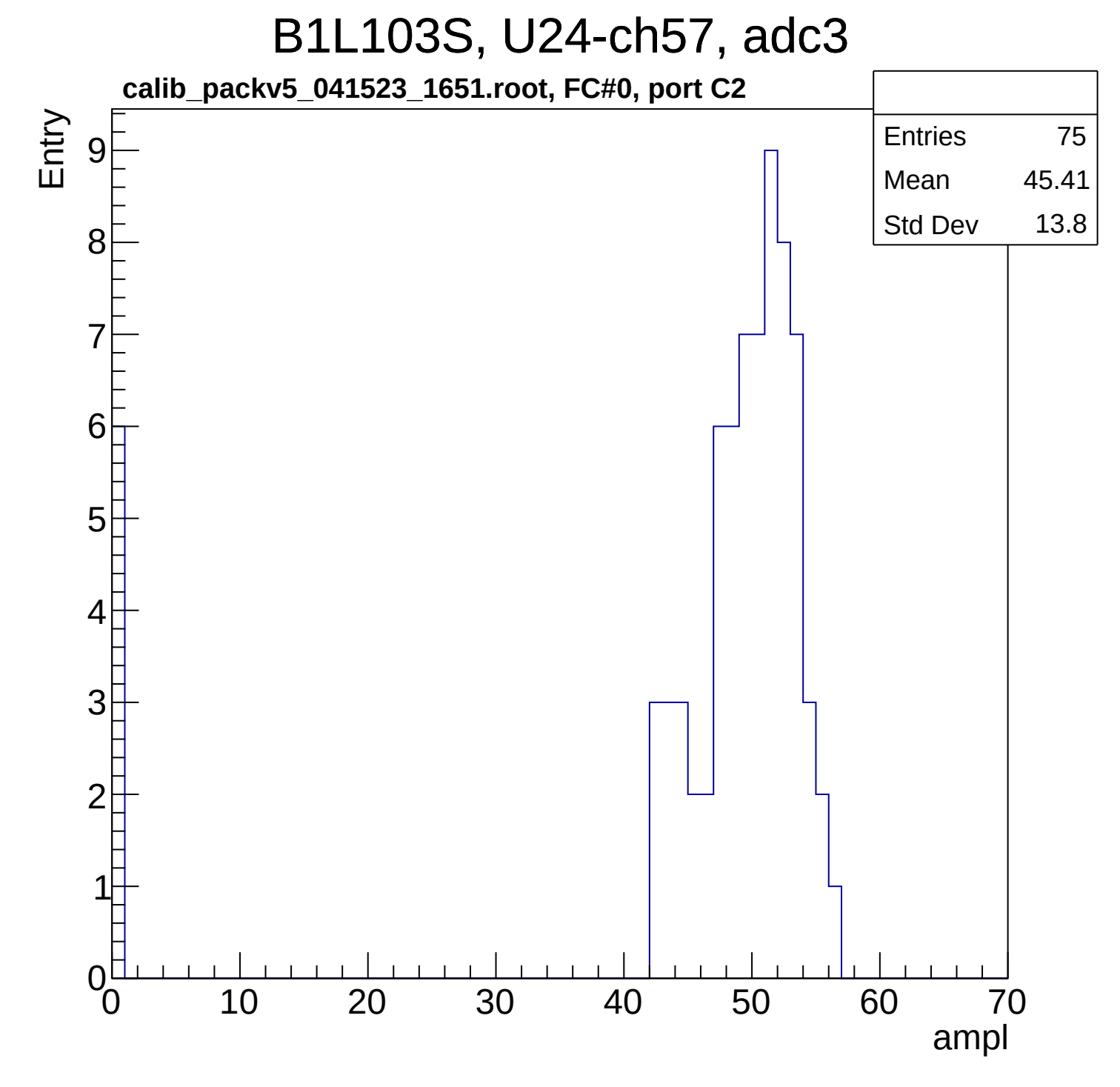
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U24-ch57, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 45.41
Std Dev 13.8
Entry
ampl
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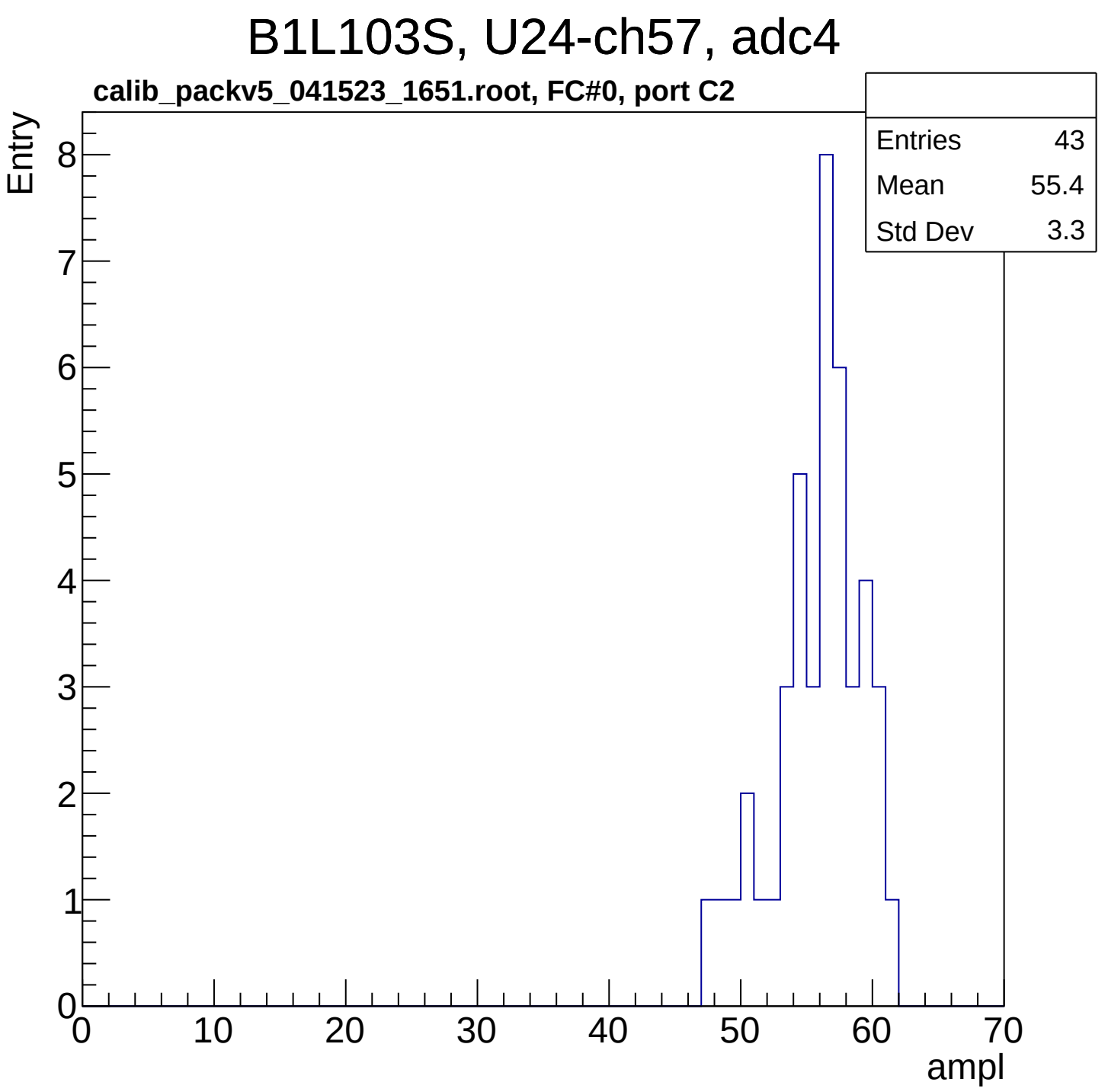
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U24-ch57, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 43
Mean 55.4
Std Dev 3.3
Entry
ampl
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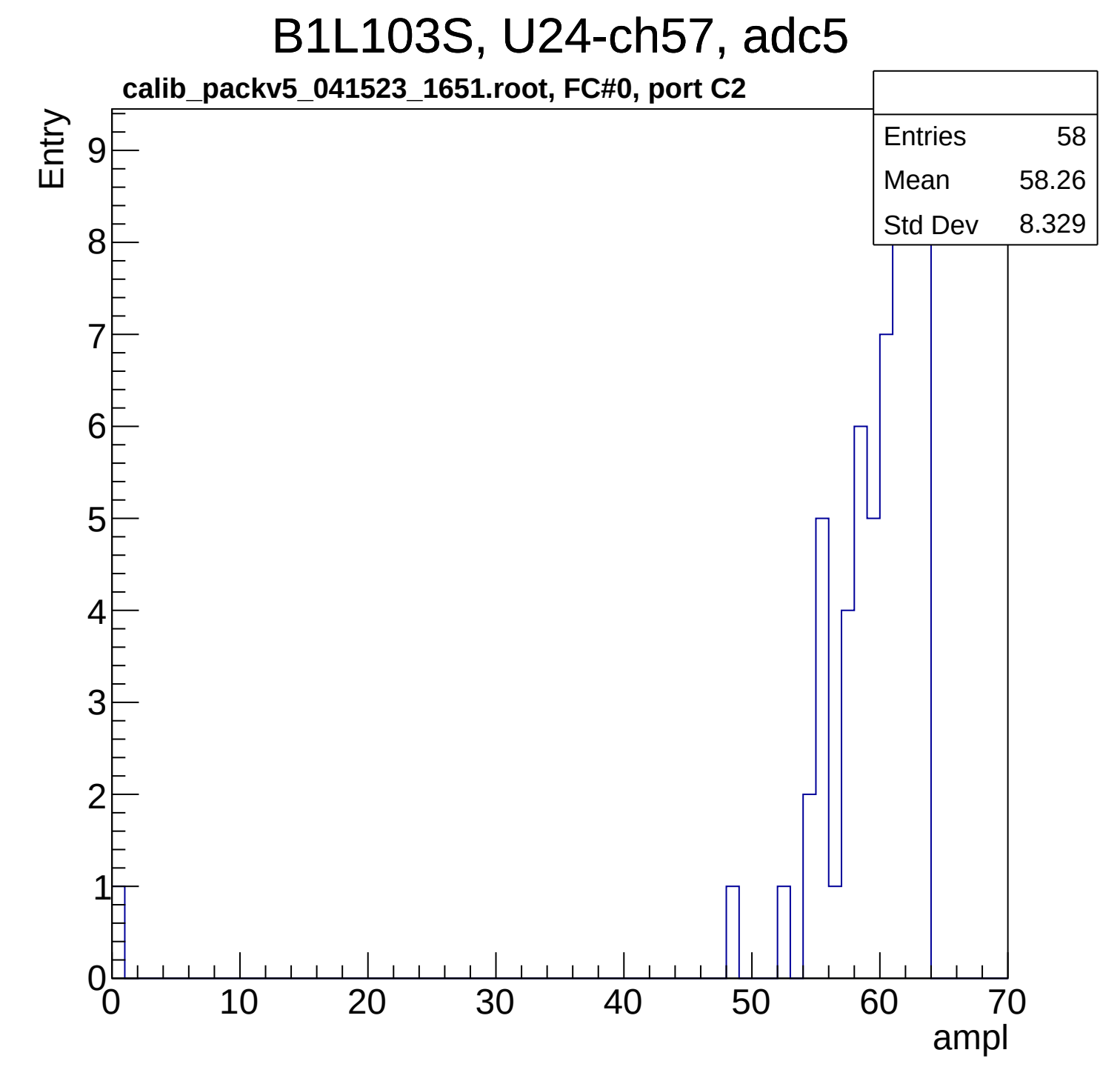
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U24-ch57, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 58.26
Std Dev 8.329
Entry
ampl
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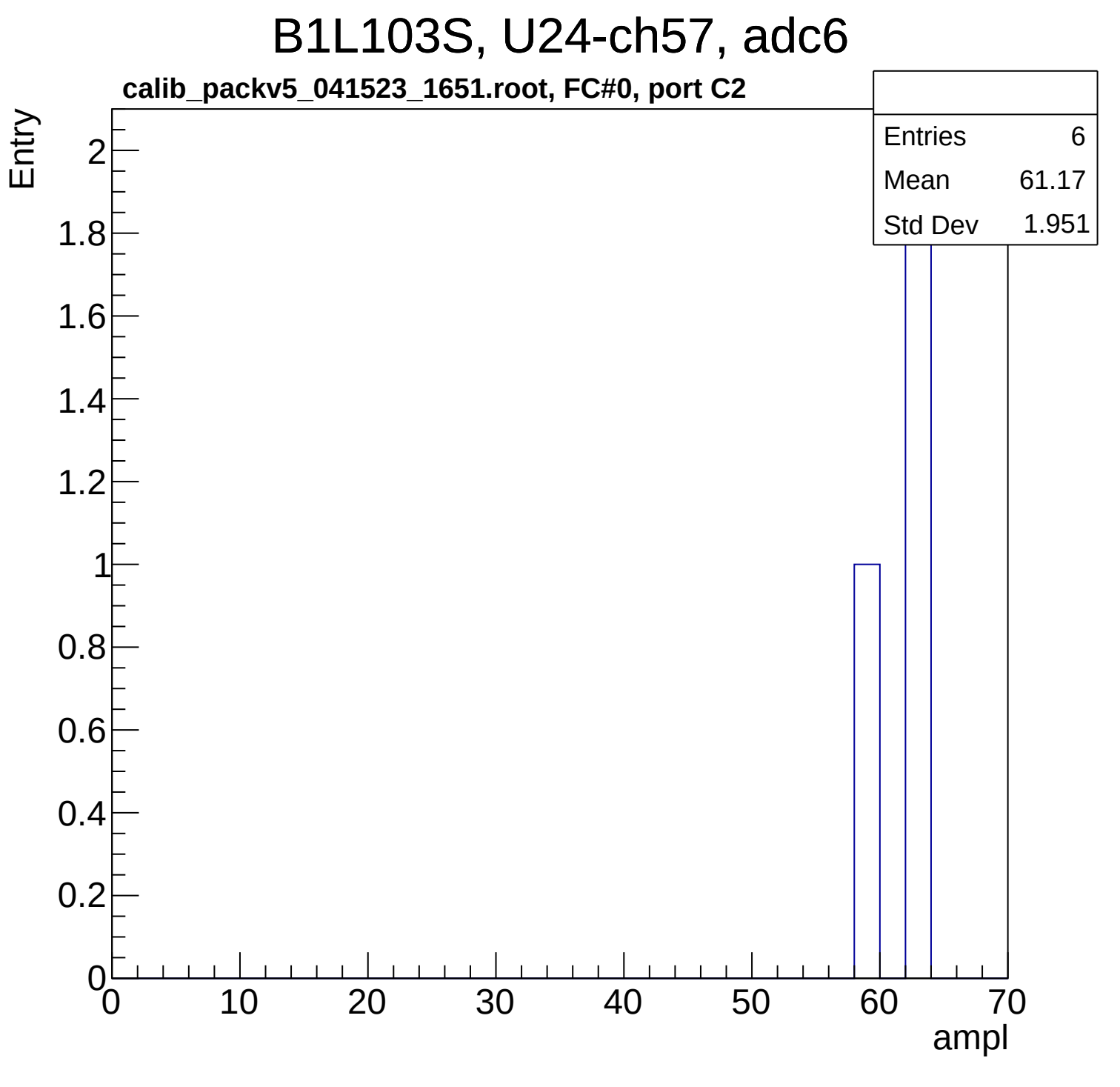
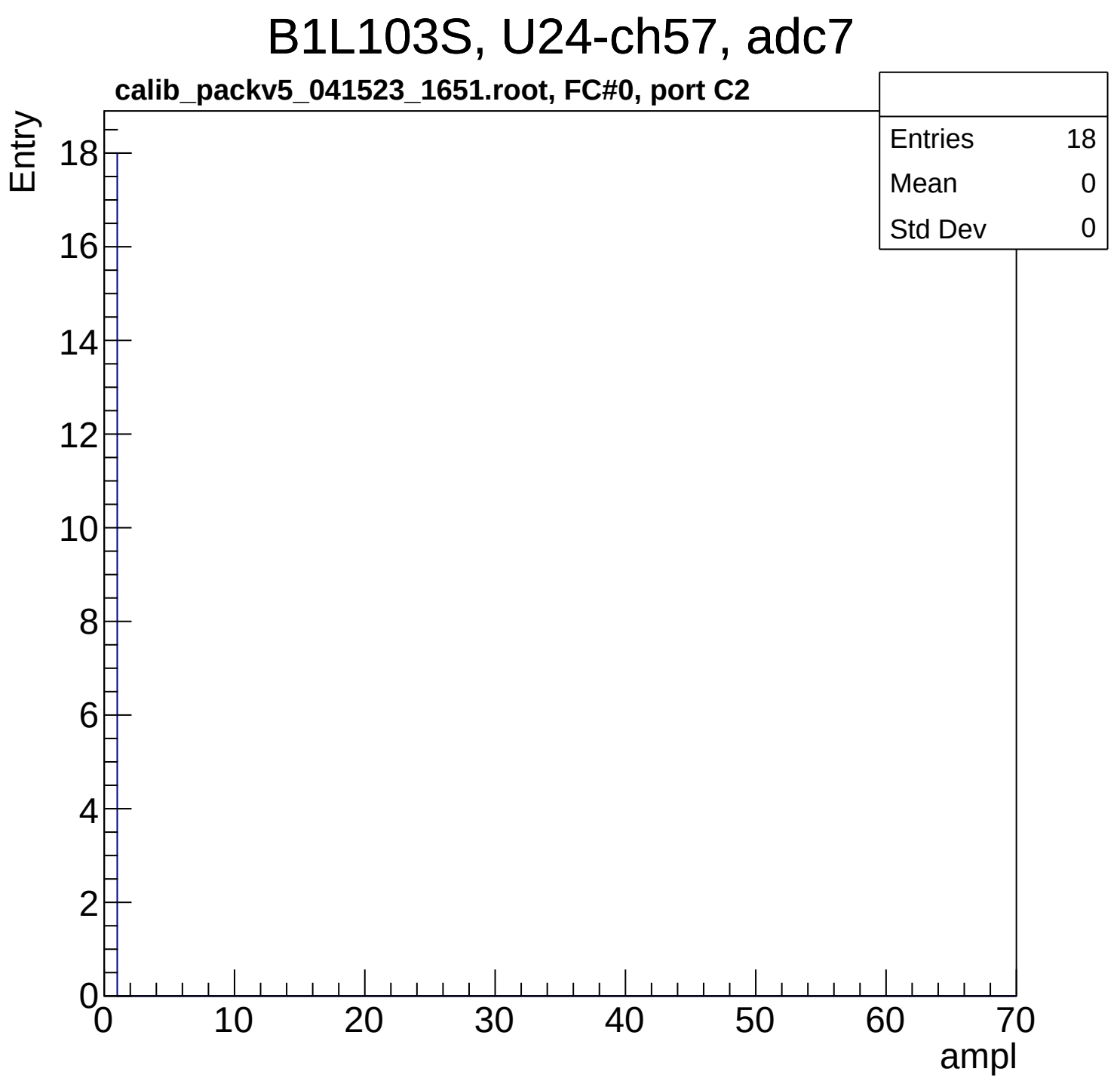
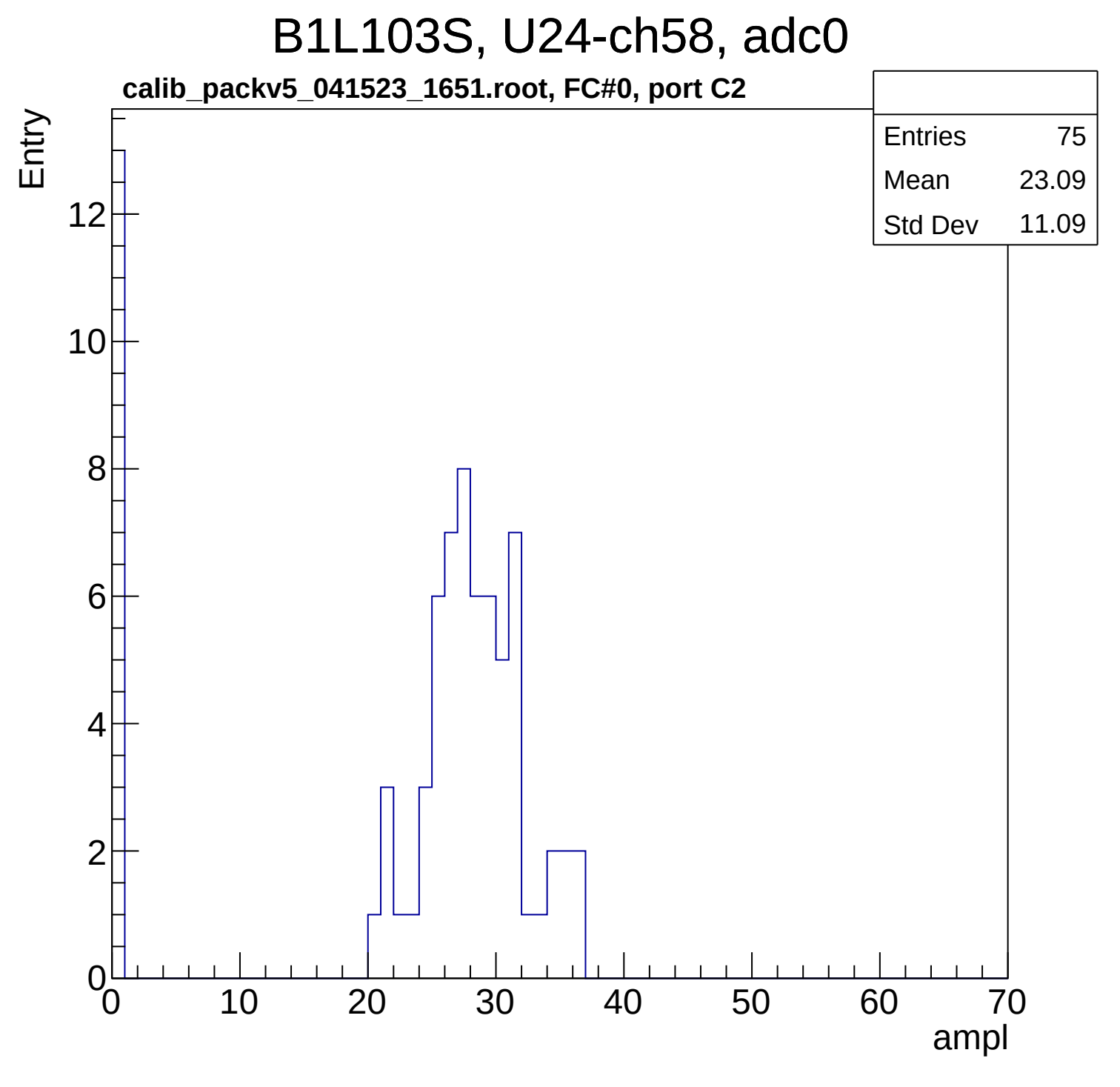
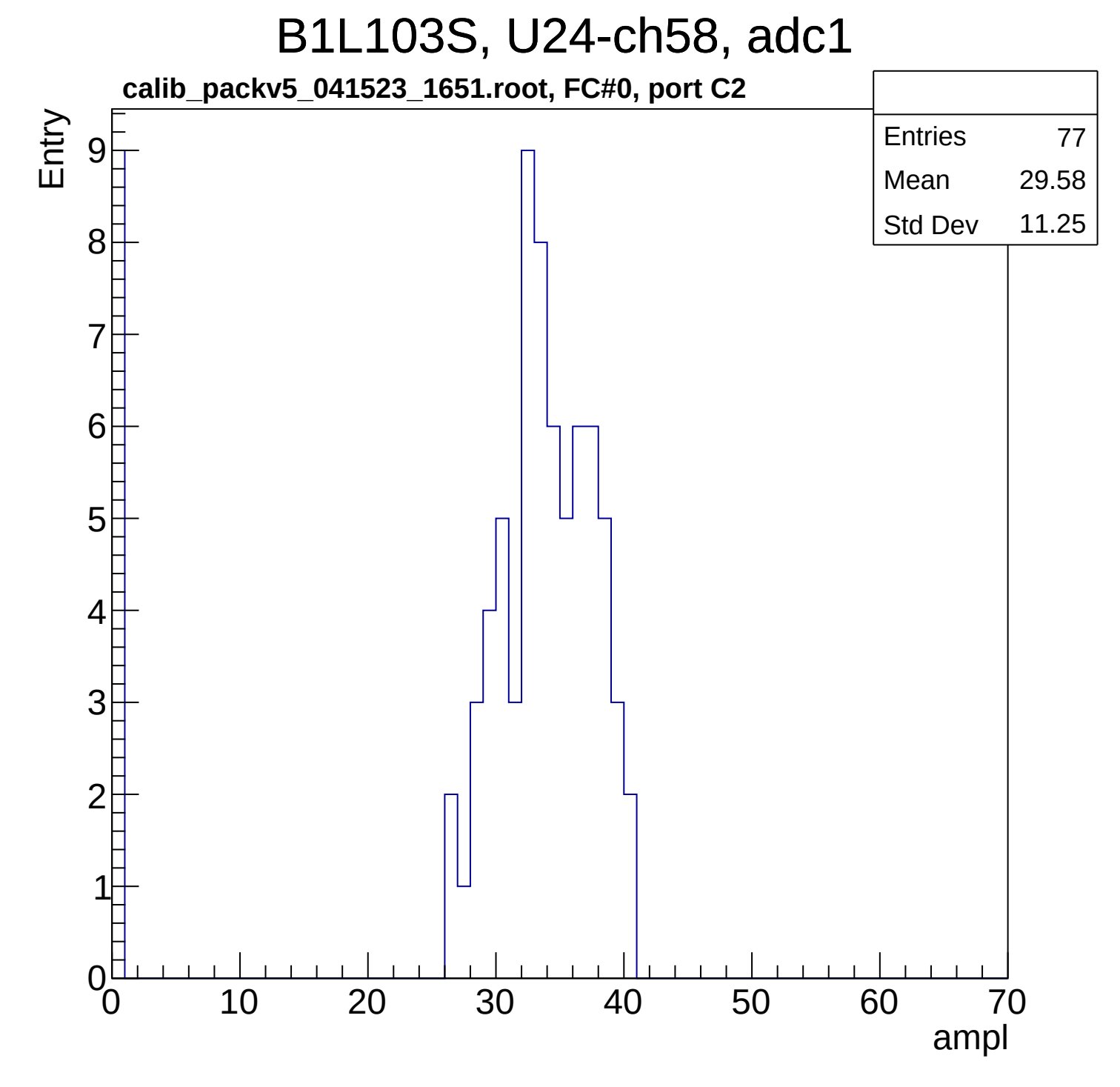
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U24-ch57, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 61.17
Std Dev 1.951
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U24-ch57, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch58, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 23.09
Std Dev 11.09
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch58, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 29.58
Std Dev 11.25
Entry
ampl
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2
3
4
5
6
7
8
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0
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60
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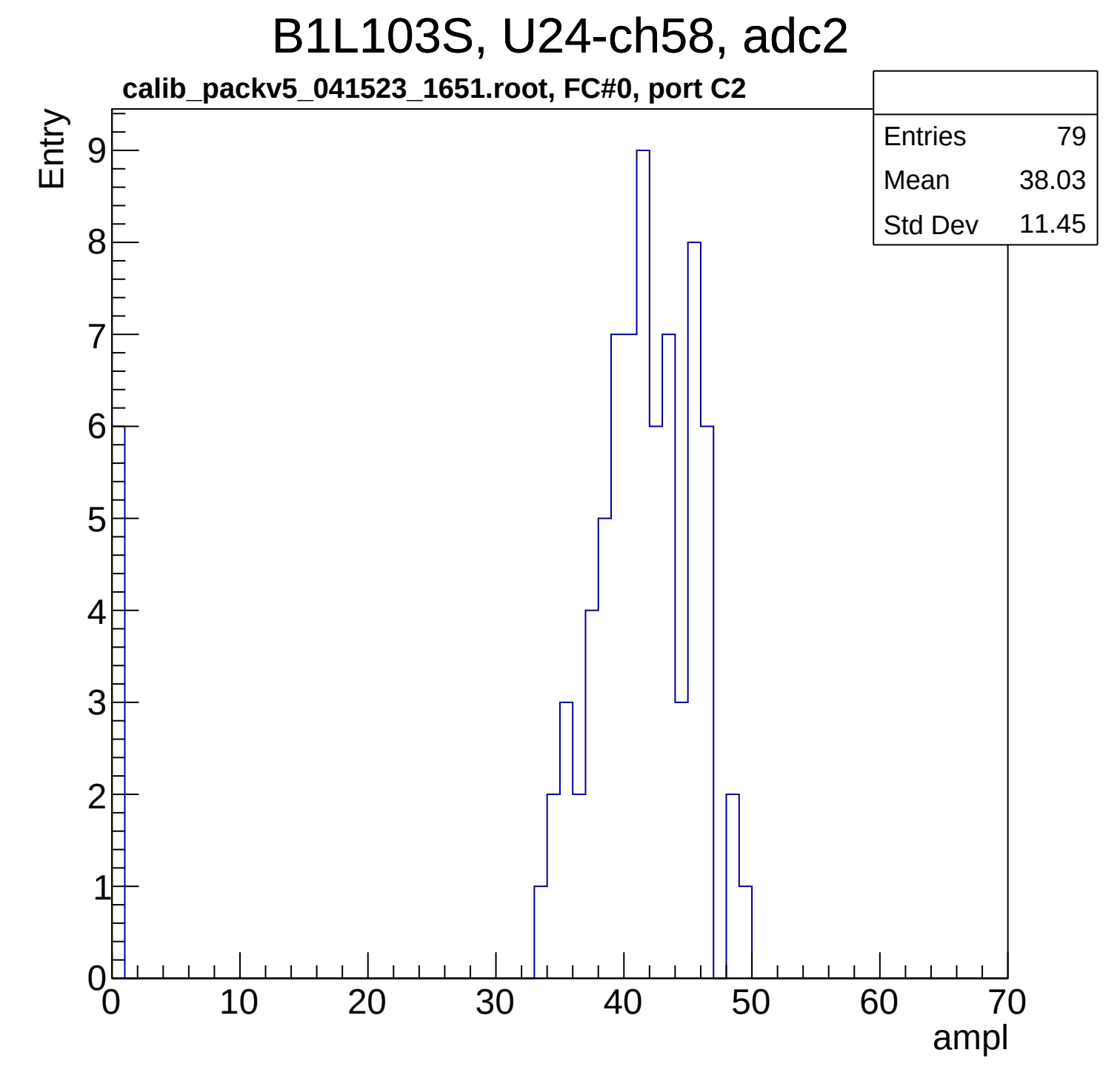
B1L103S, U24-ch58, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 38.03
Std Dev 11.45
Entry
ampl
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2
3
4
5
6
7
8
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0
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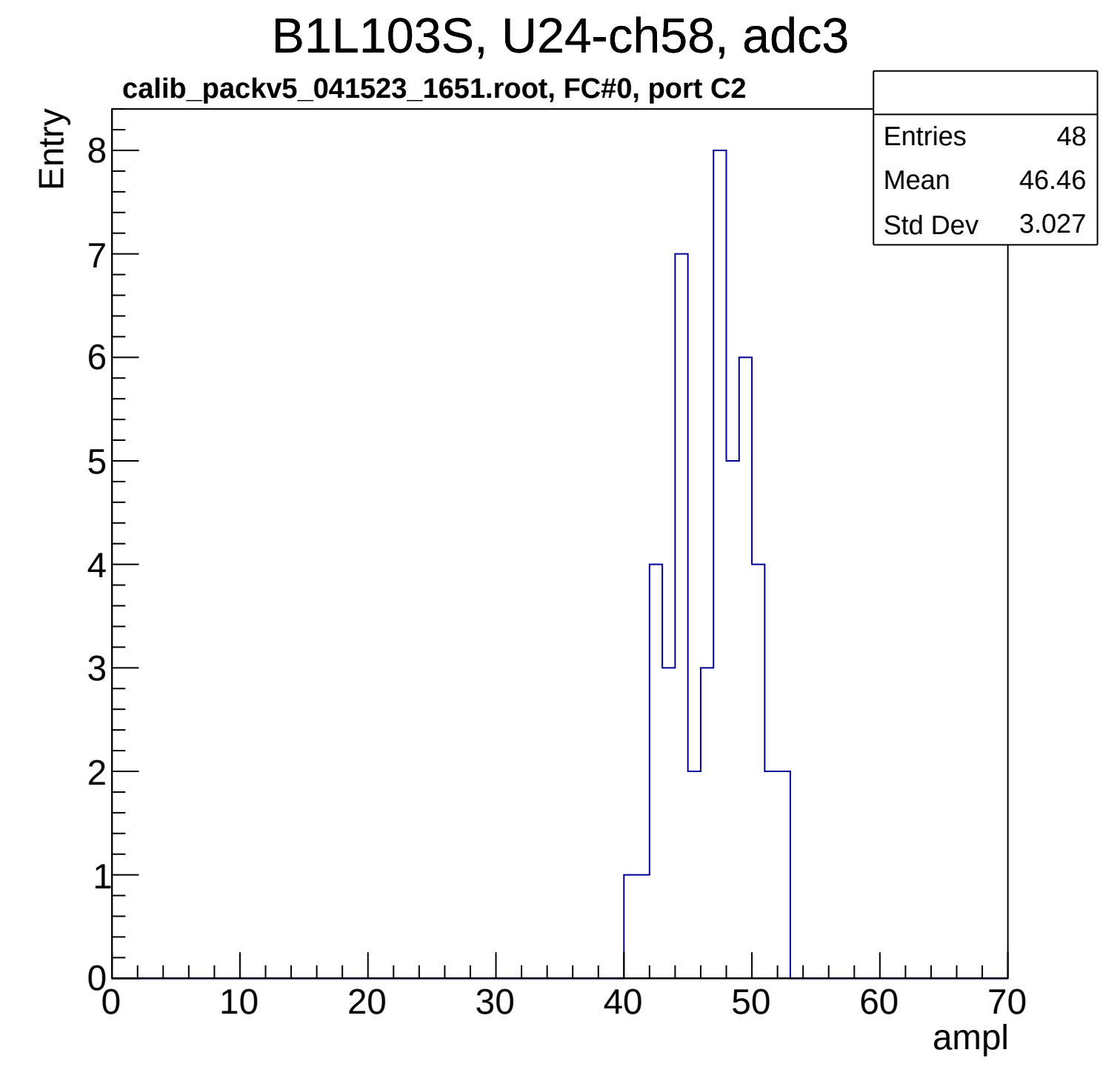
B1L103S, U24-ch58, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 46.46
Std Dev 3.027
Entry
ampl
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1
2
3
4
5
6
7
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0
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60
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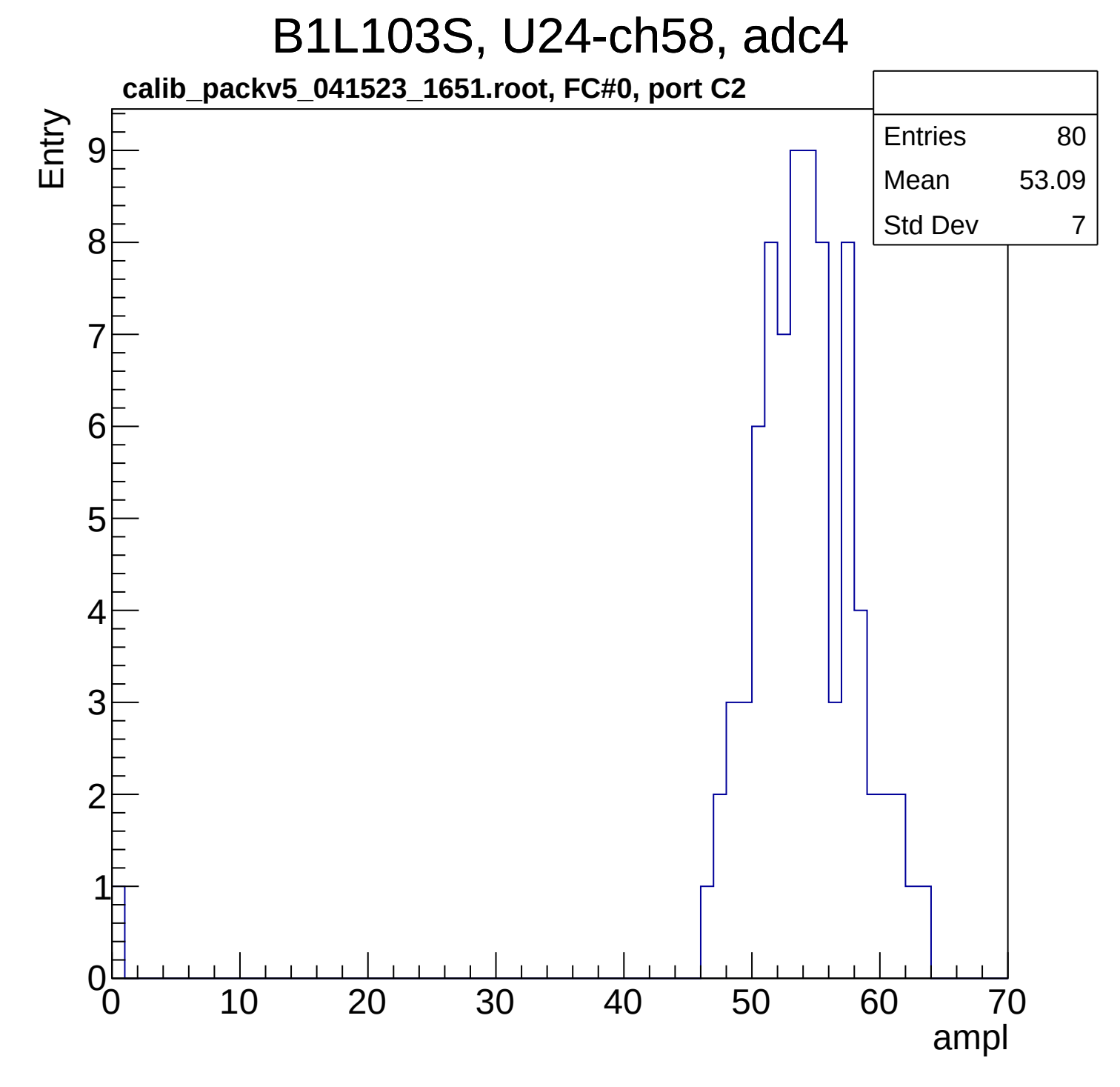
B1L103S, U24-ch58, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 53.09
Std Dev 7
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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40
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60
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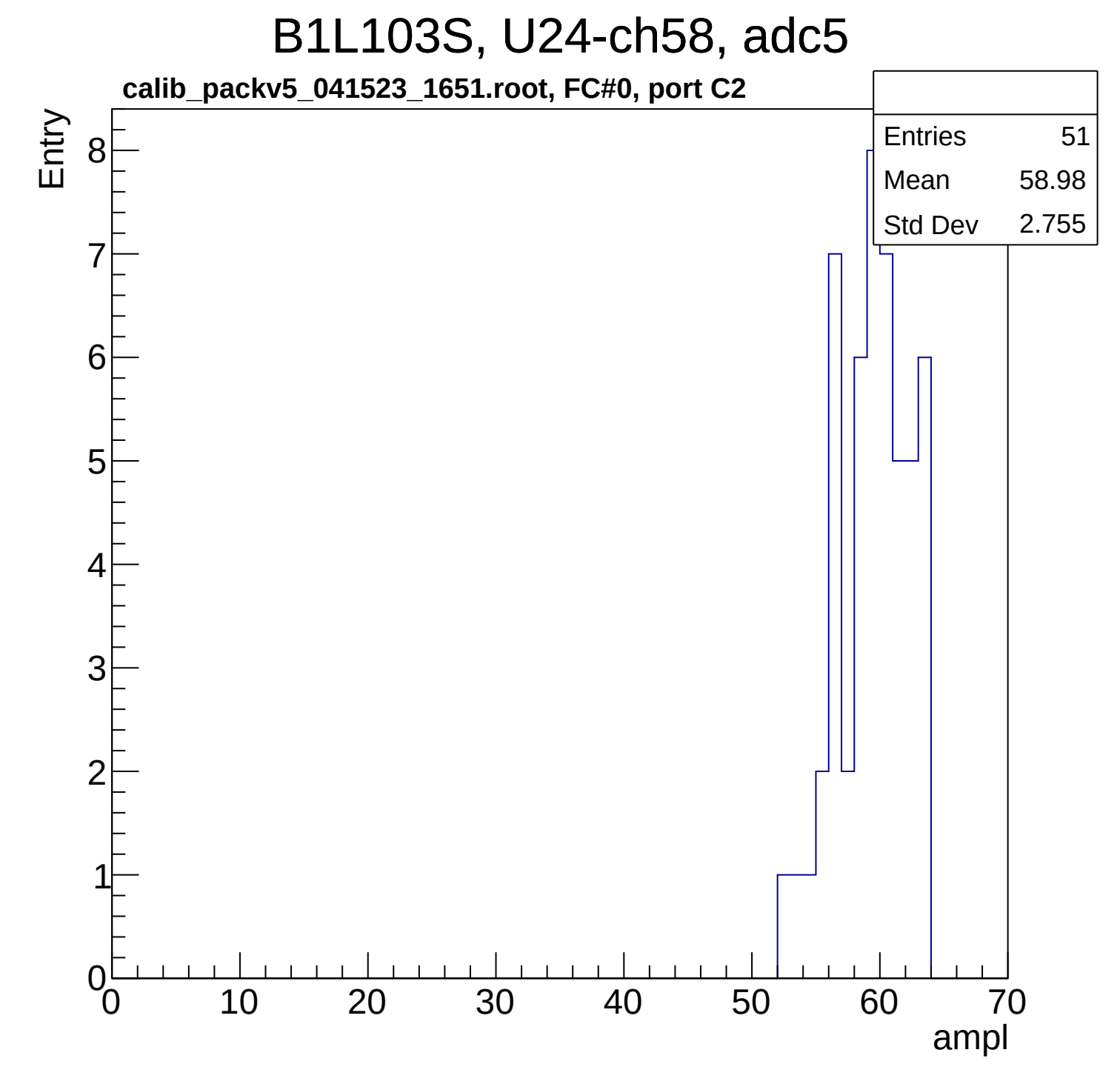
B1L103S, U24-ch58, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 58.98
Std Dev 2.755
Entry
ampl
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1
2
3
4
5
6
7
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0
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60
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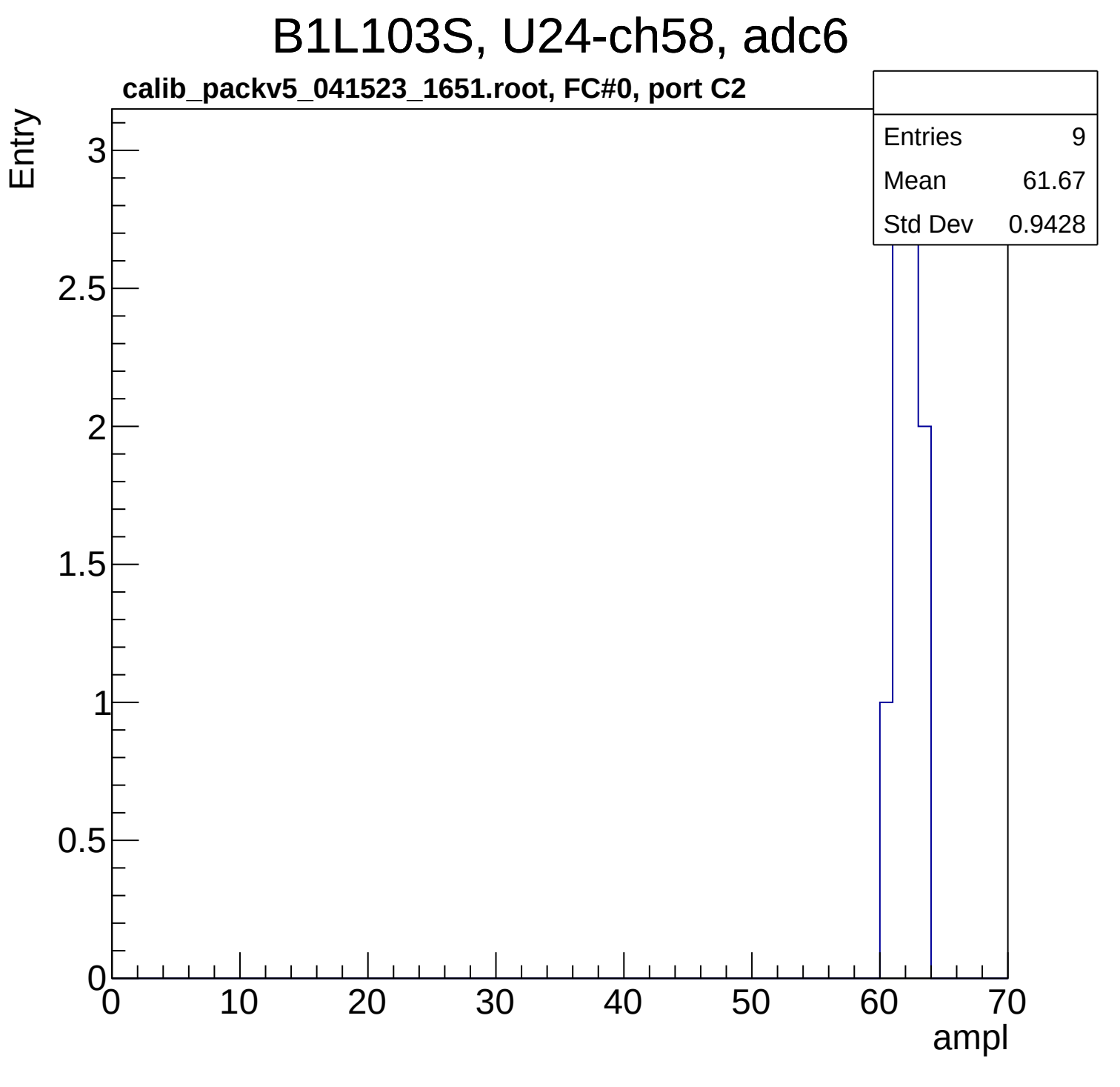
B1L103S, U24-ch58, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 9
Mean 61.67
Std Dev 0.9428
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
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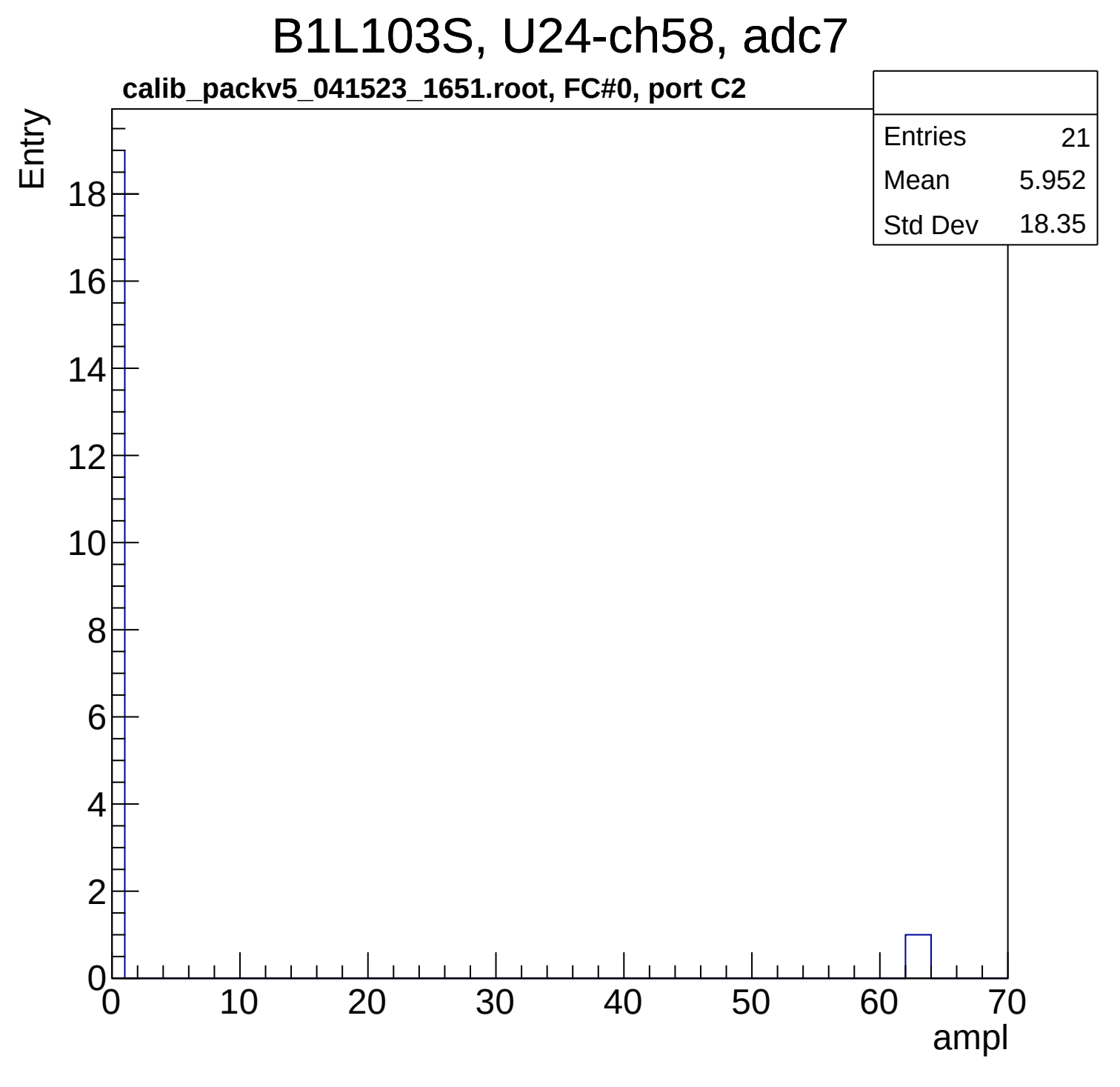
B1L103S, U24-ch58, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 5.952
Std Dev 18.35
Entry
0
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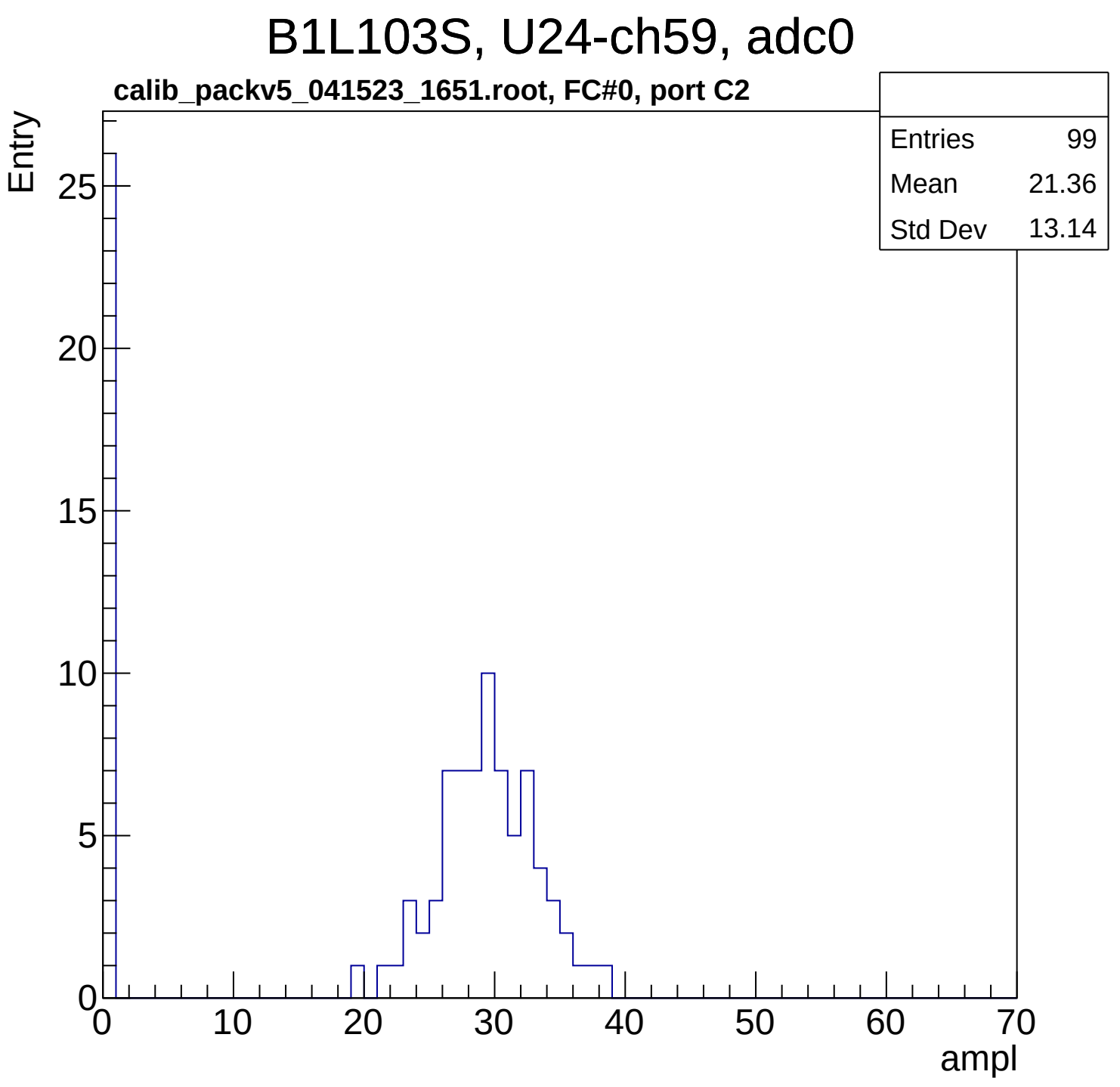
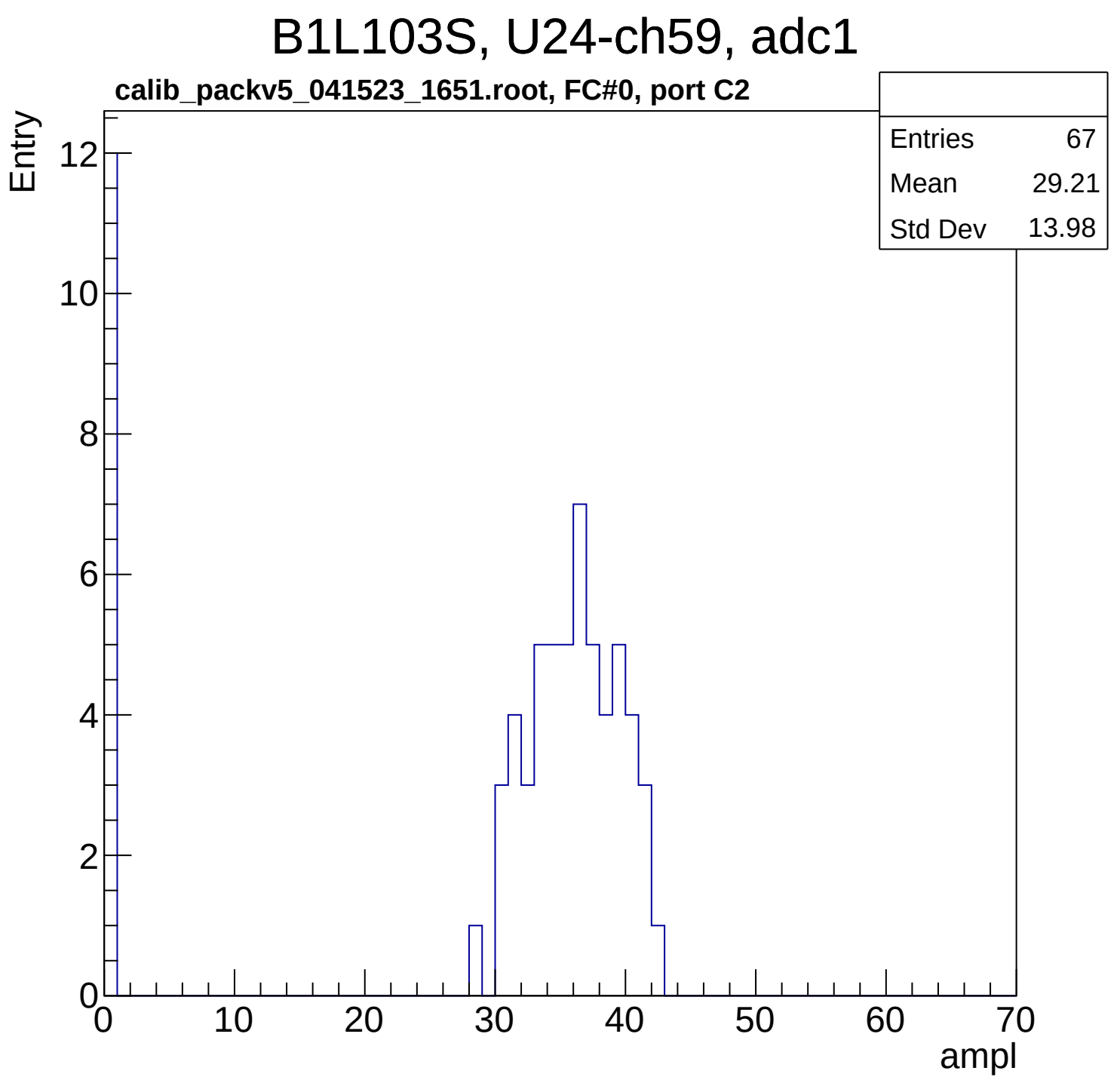
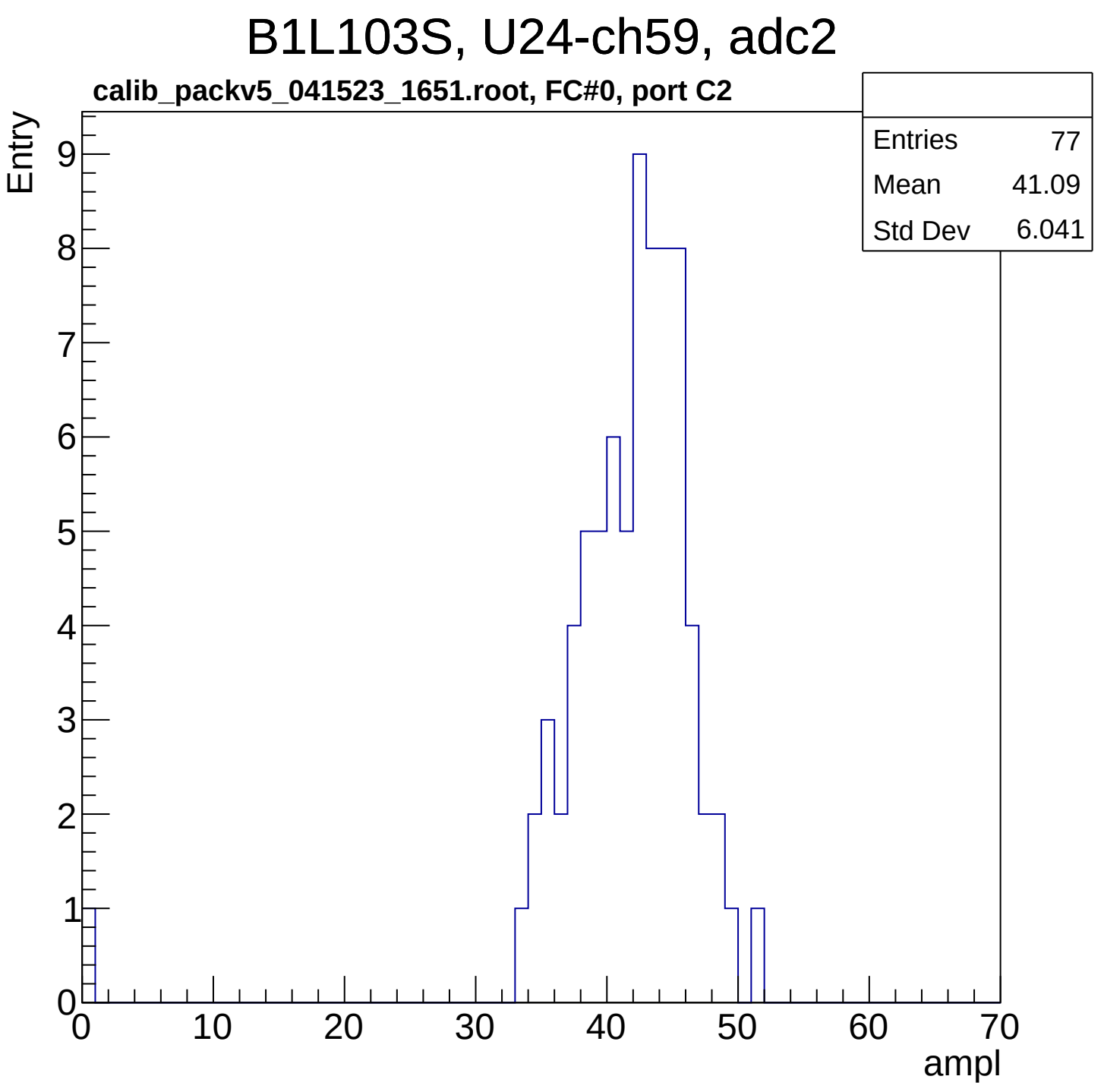
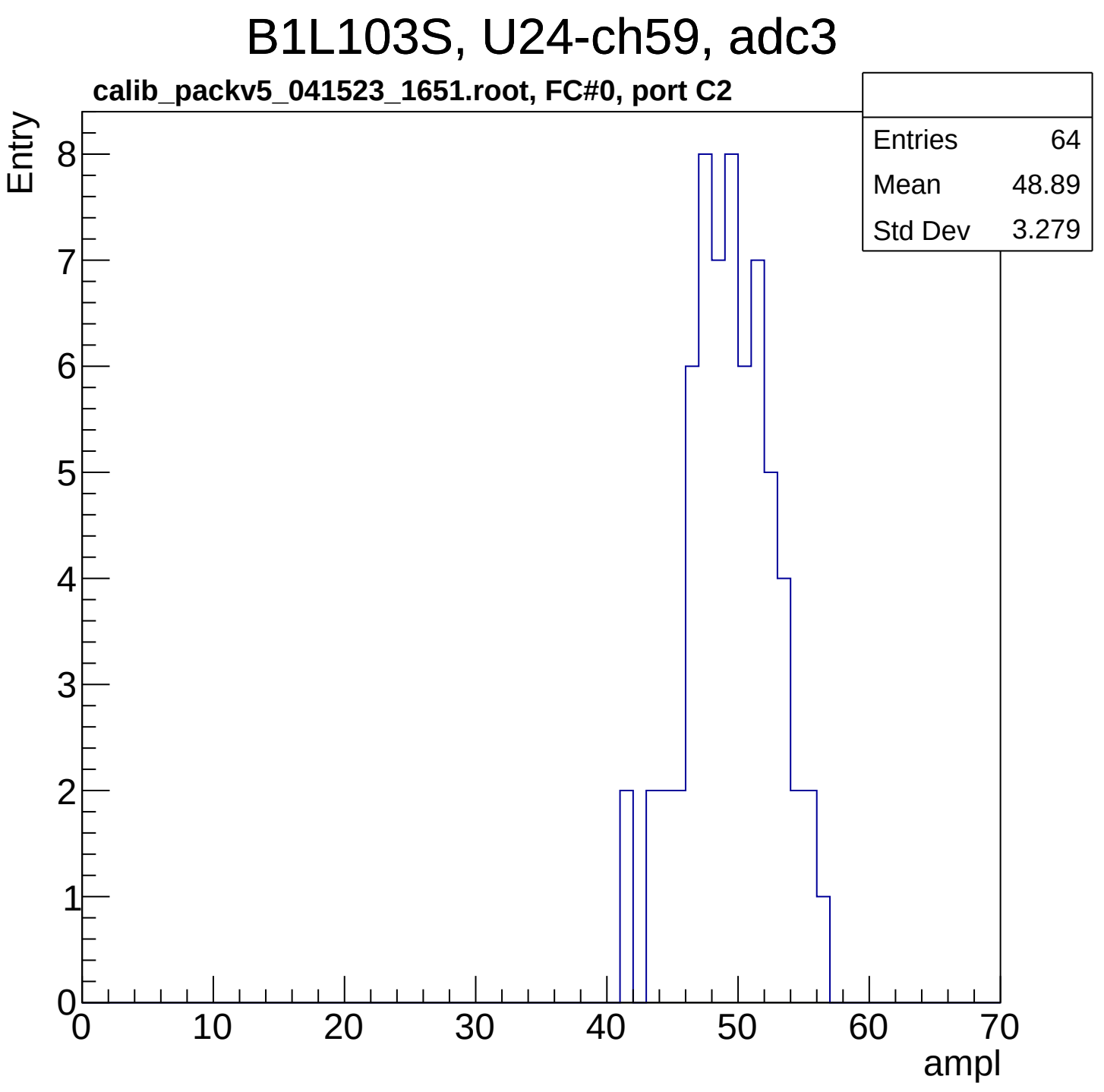
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch59, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 99
Mean 21.36
Std Dev 13.14
Entry
0
5
10
15
20
25
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch59, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 29.21
Std Dev 13.98
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch59, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 41.09
Std Dev 6.041
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U24-ch59, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 48.89
Std Dev 3.279
Entry
ampl
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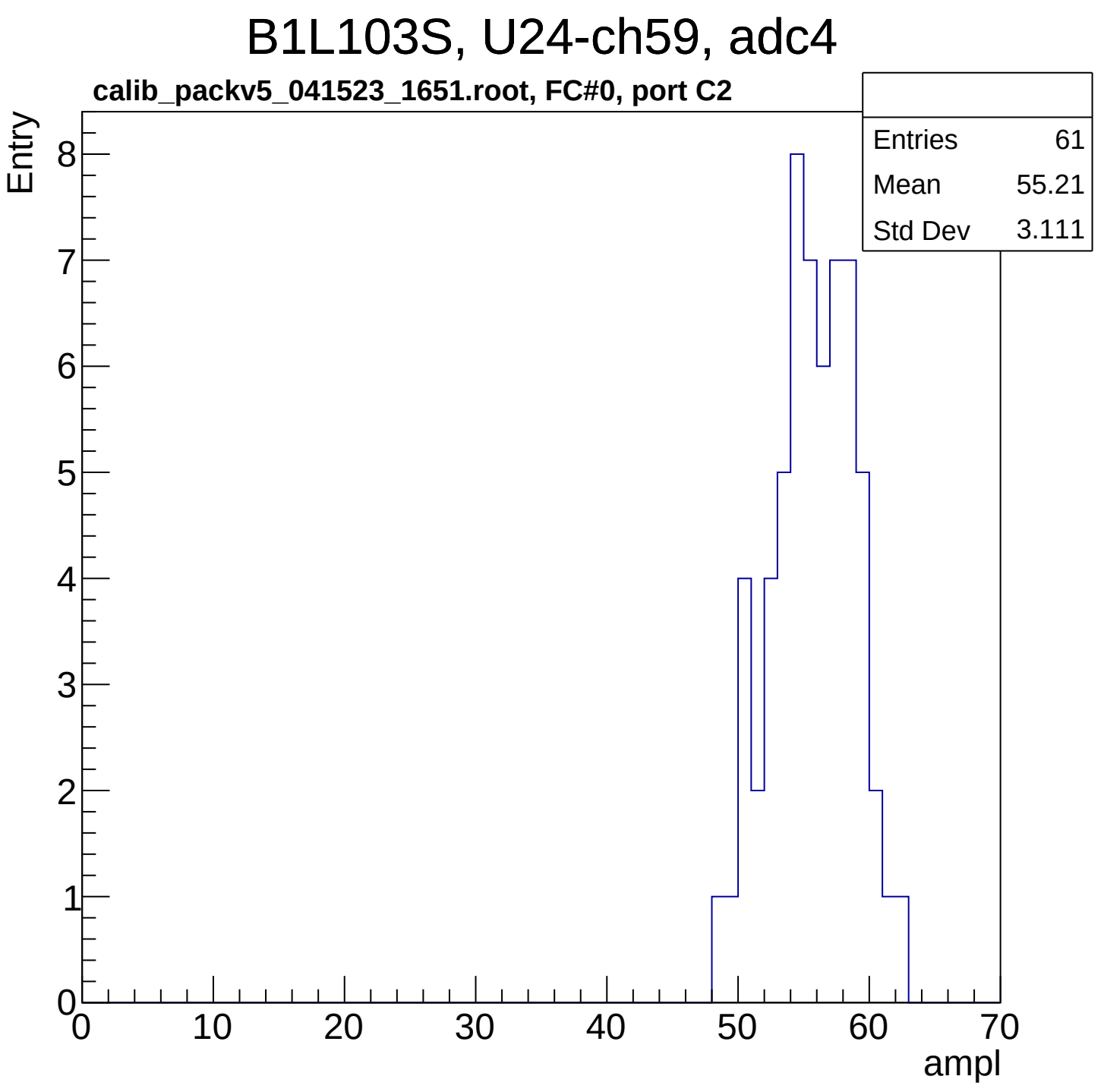
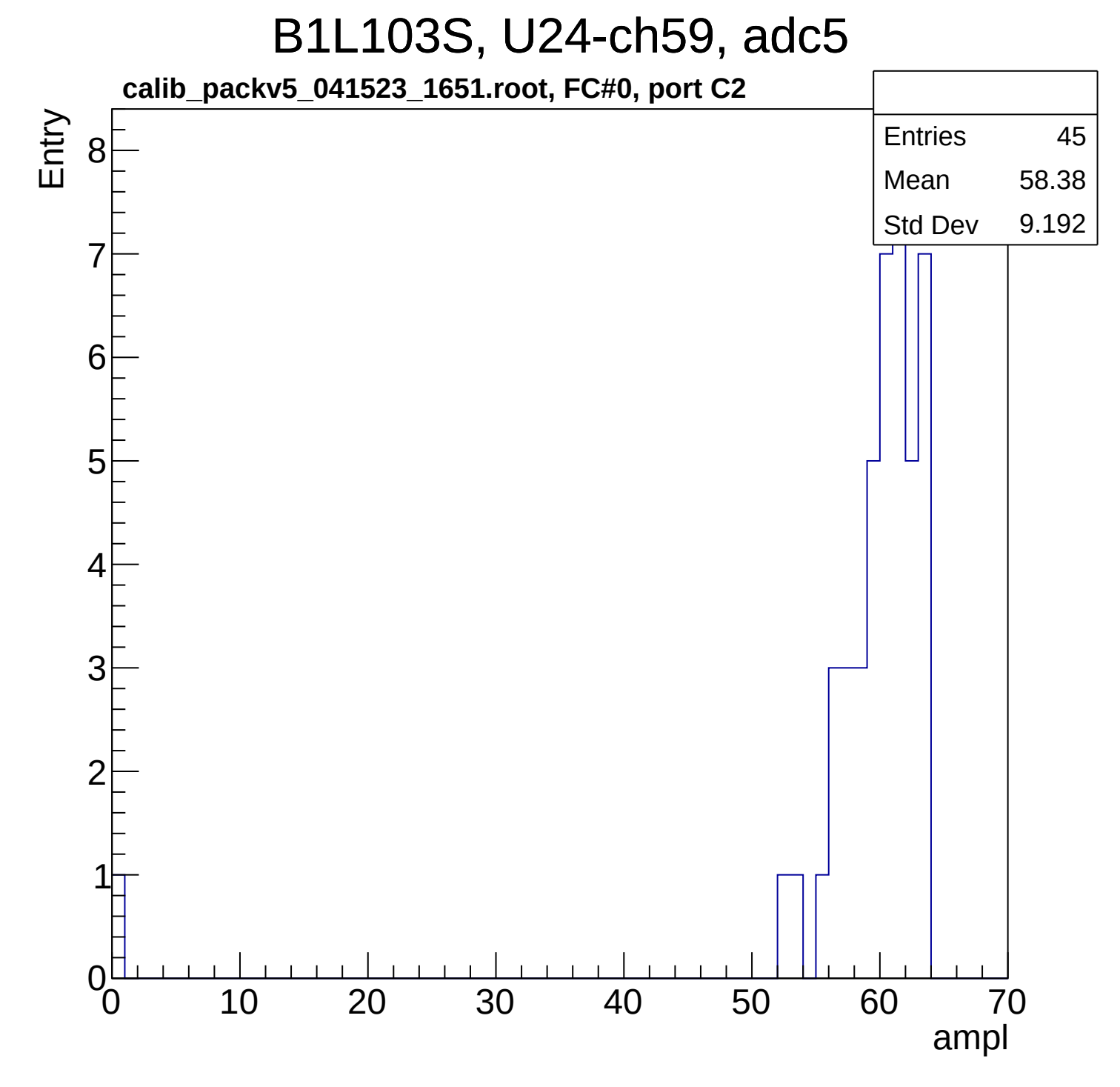
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U24-ch59, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 55.21
Std Dev 3.111
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U24-ch59, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 58.38
Std Dev 9.192
Entry
ampl
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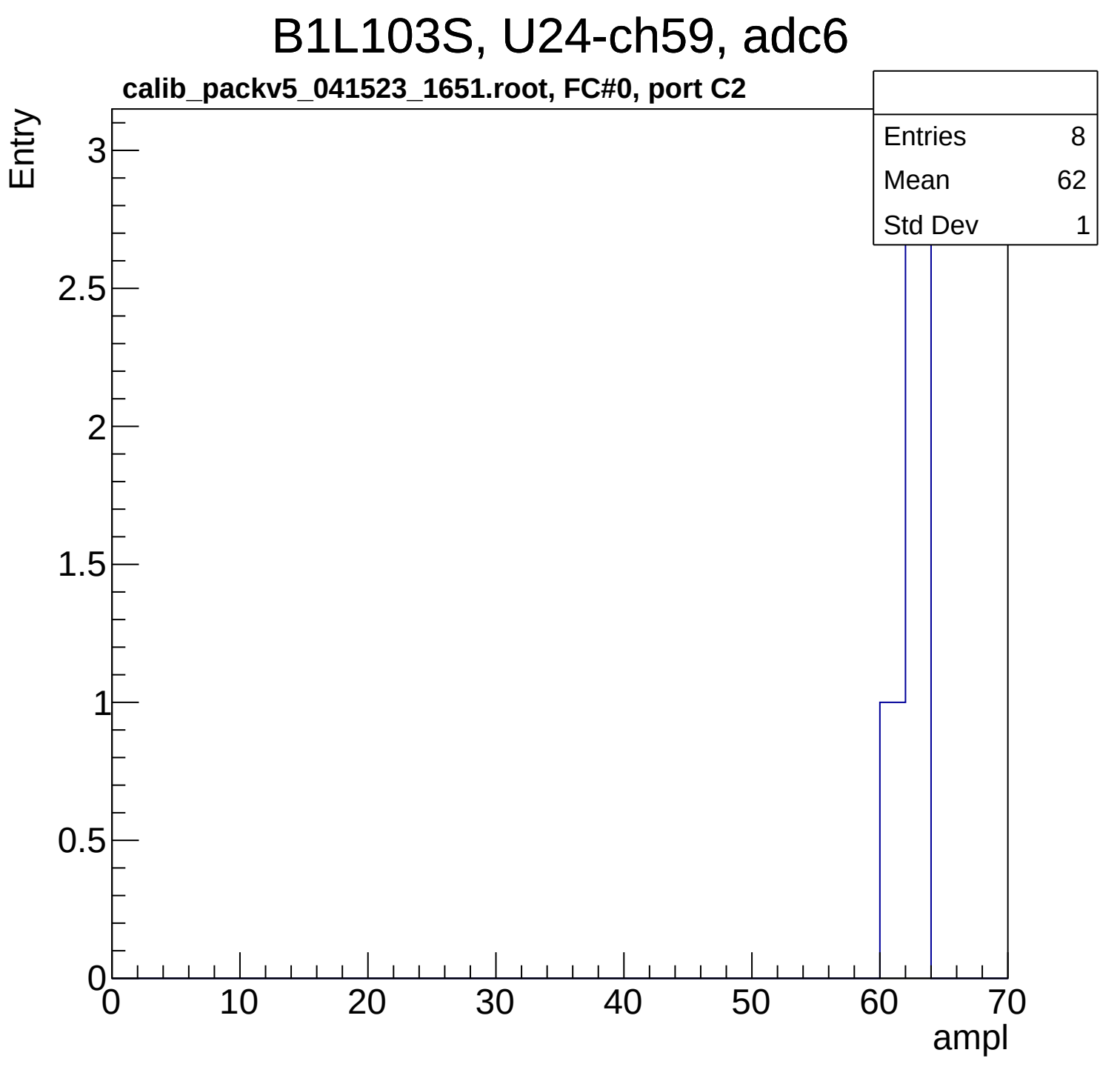
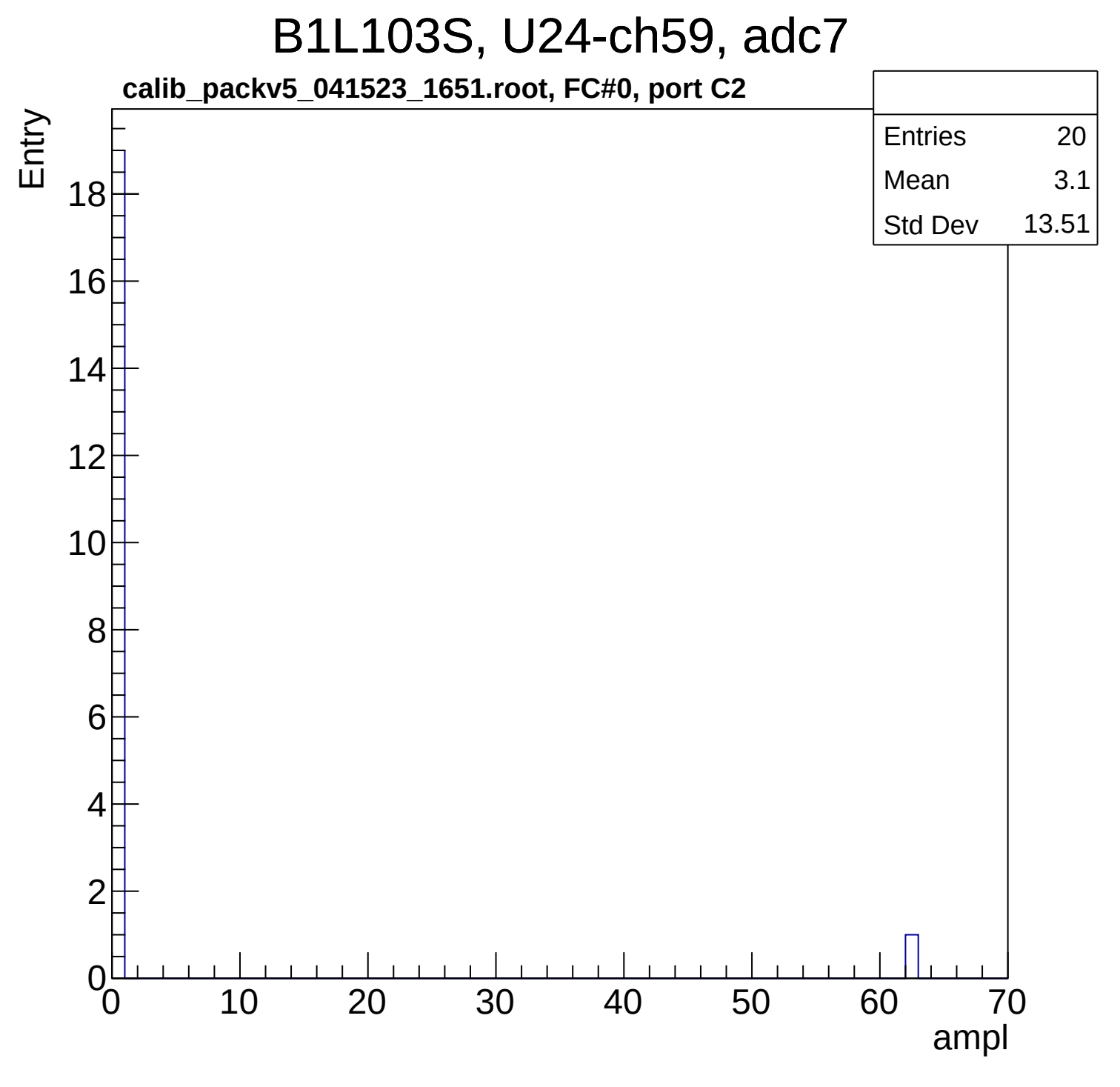
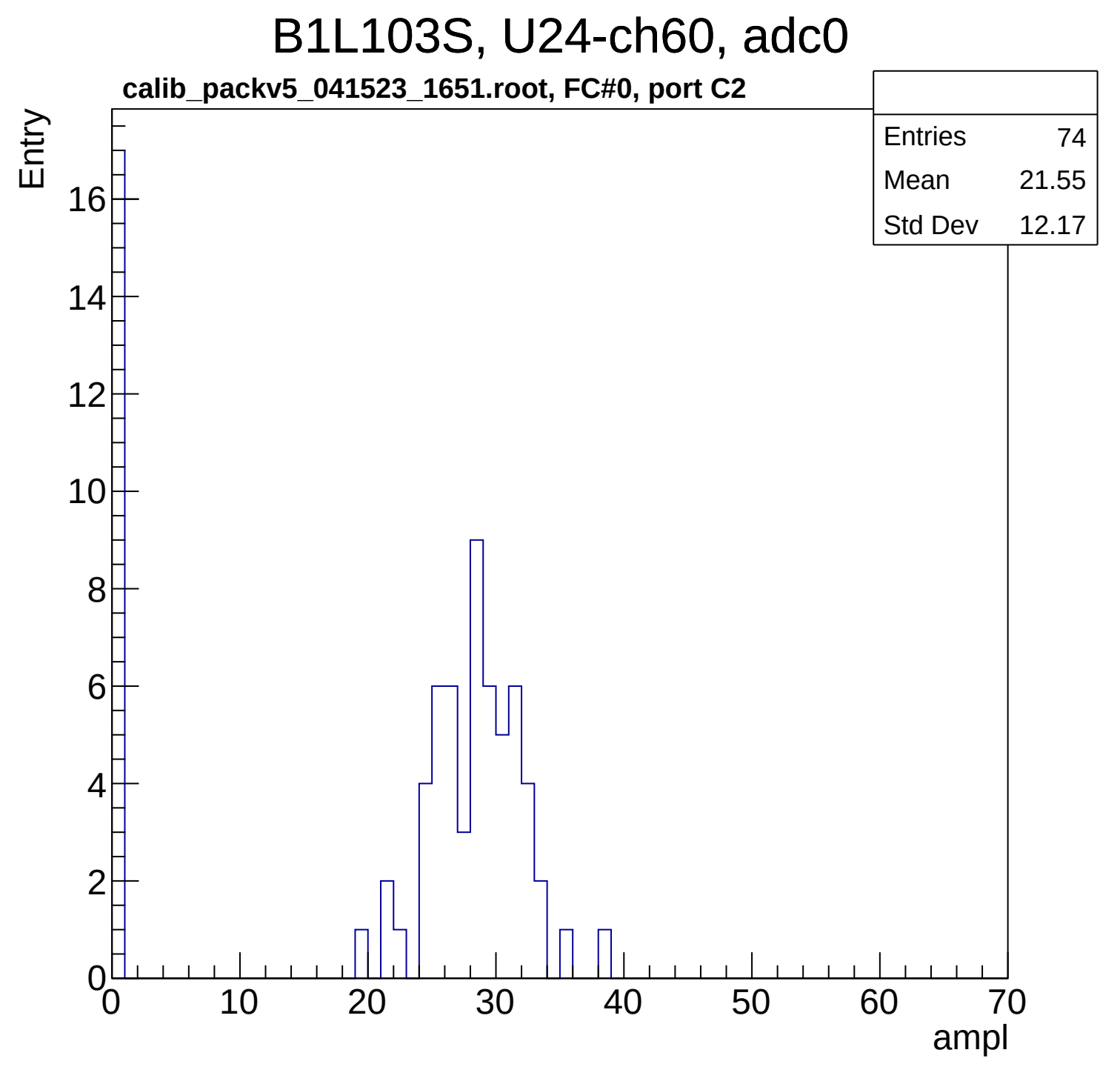
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U24-ch59, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 62
Std Dev 1
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U24-ch59, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.1
Std Dev 13.51
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch60, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 21.55
Std Dev 12.17
Entry
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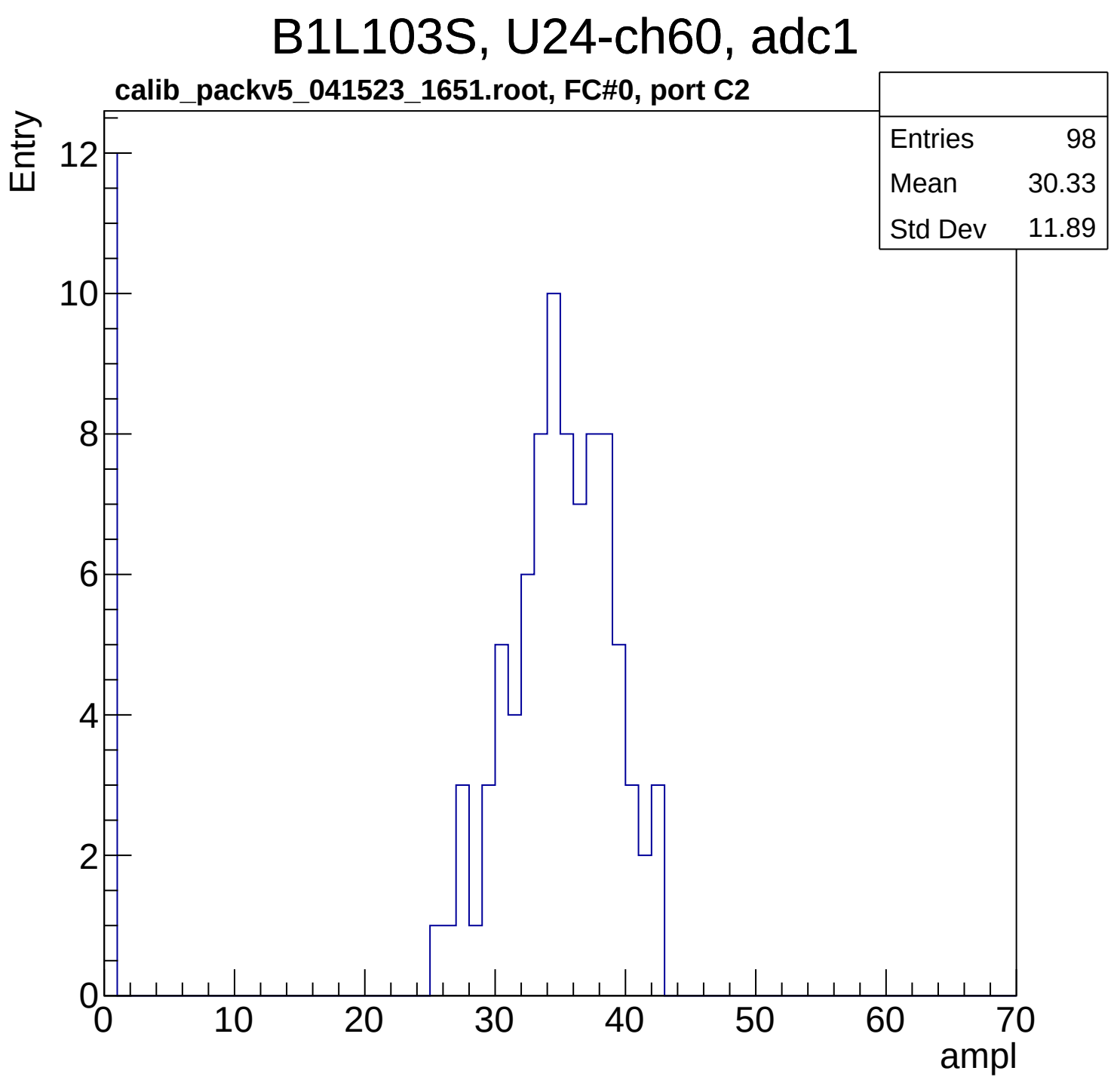
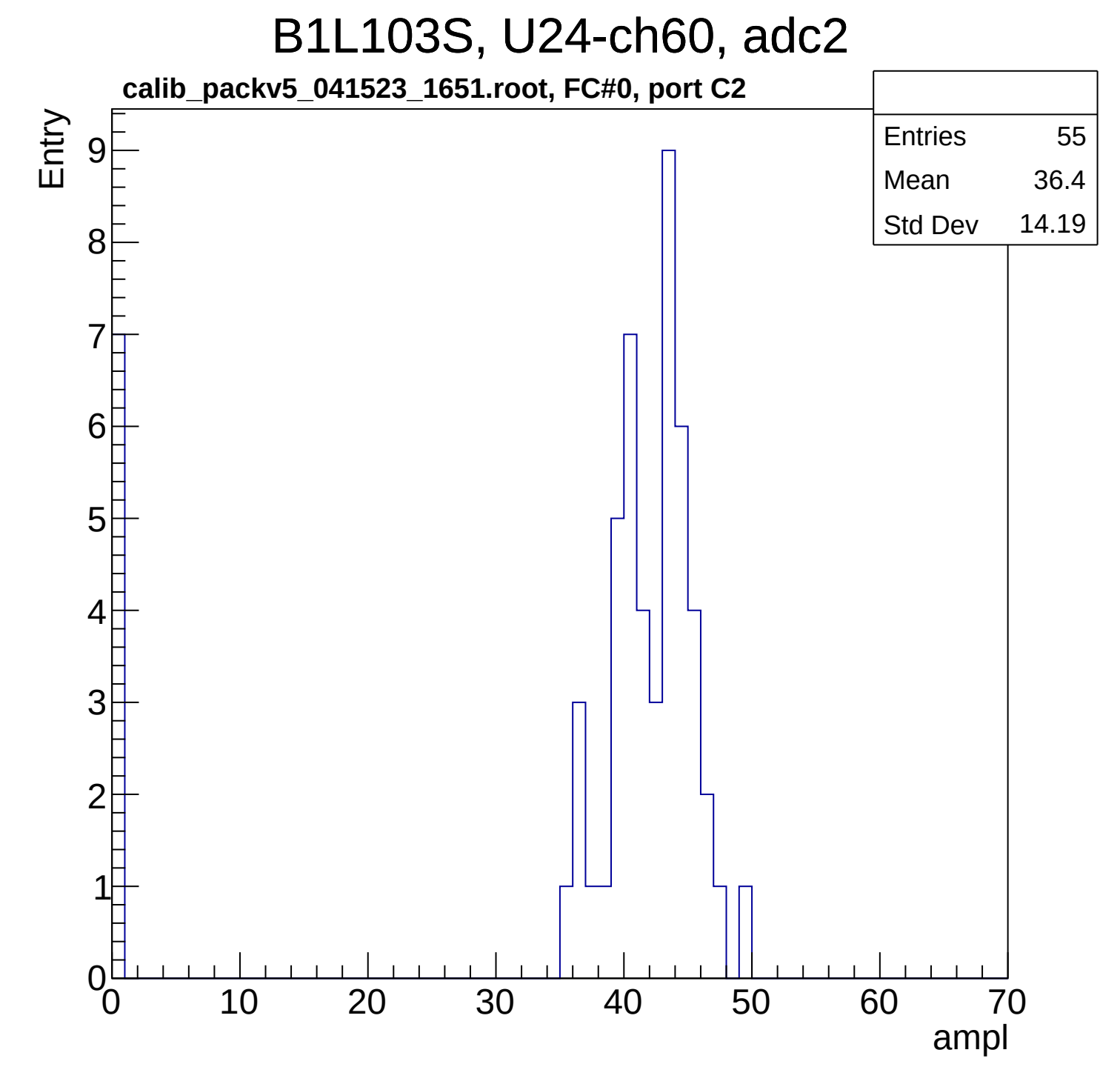
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch60, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 98
Mean 30.33
Std Dev 11.89
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch60, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 36.4
Std Dev 14.19
Entry
ampl
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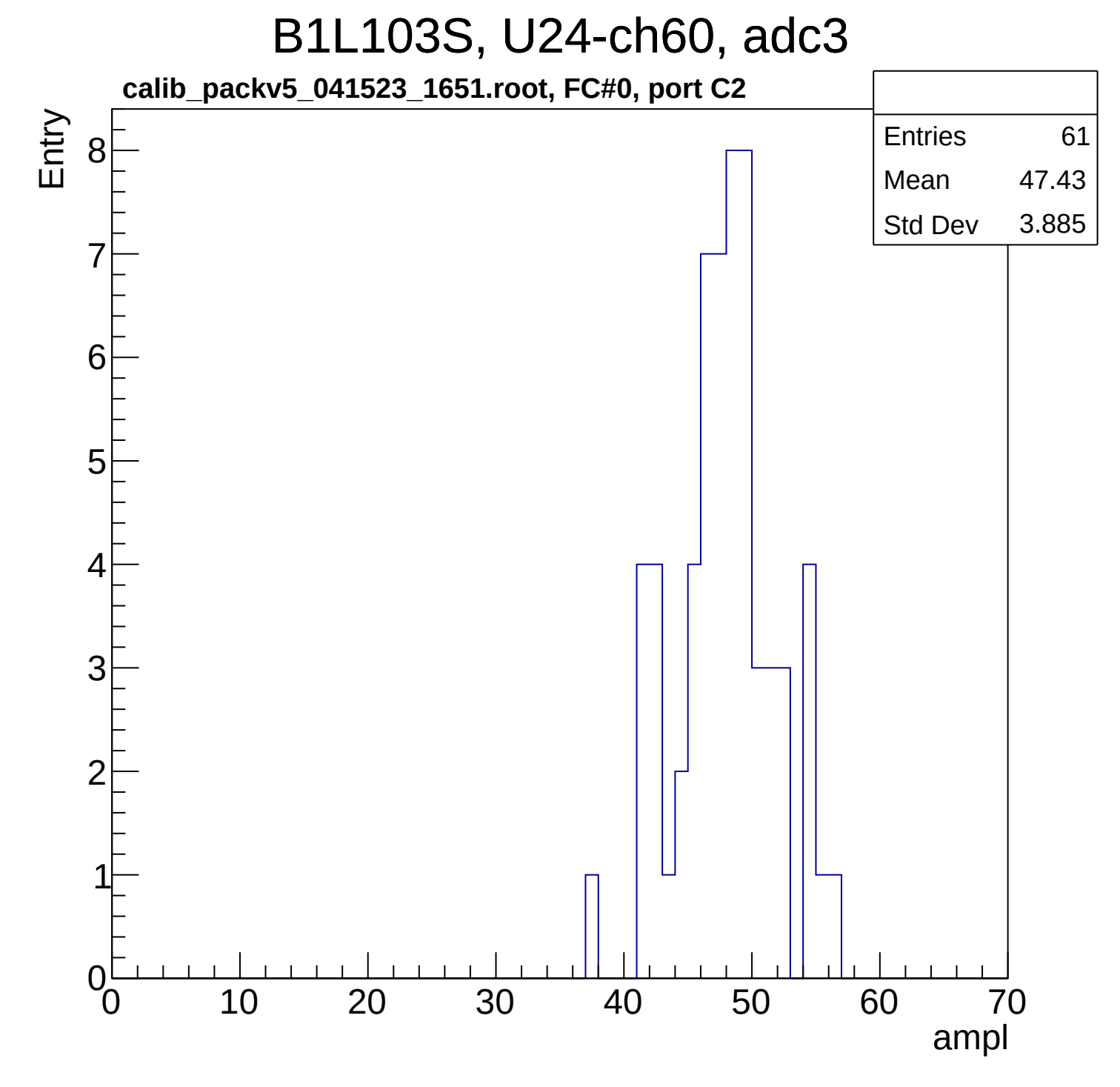
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U24-ch60, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 47.43
Std Dev 3.885
Entry
ampl
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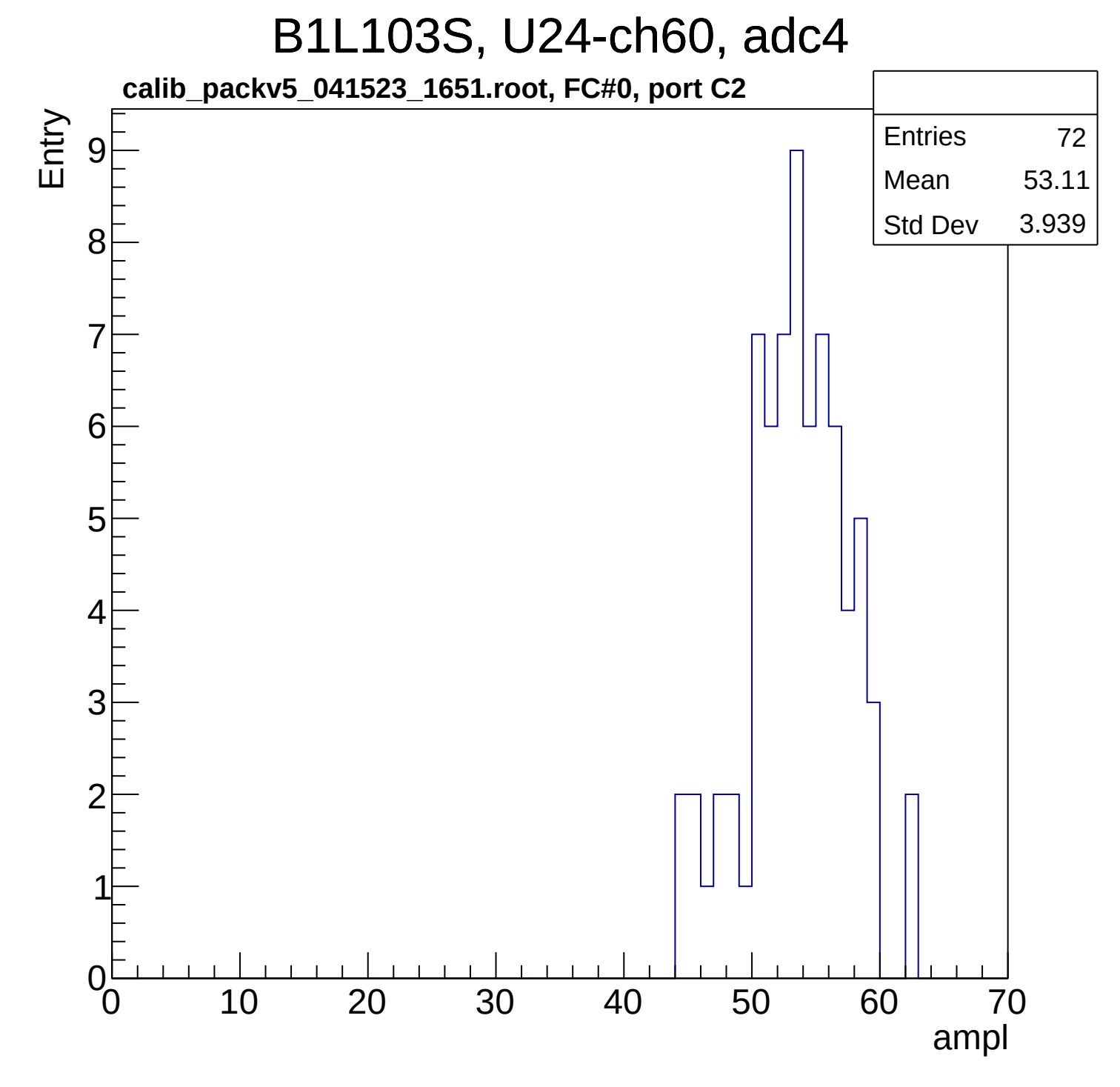
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U24-ch60, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 53.11
Std Dev 3.939
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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40
50
60
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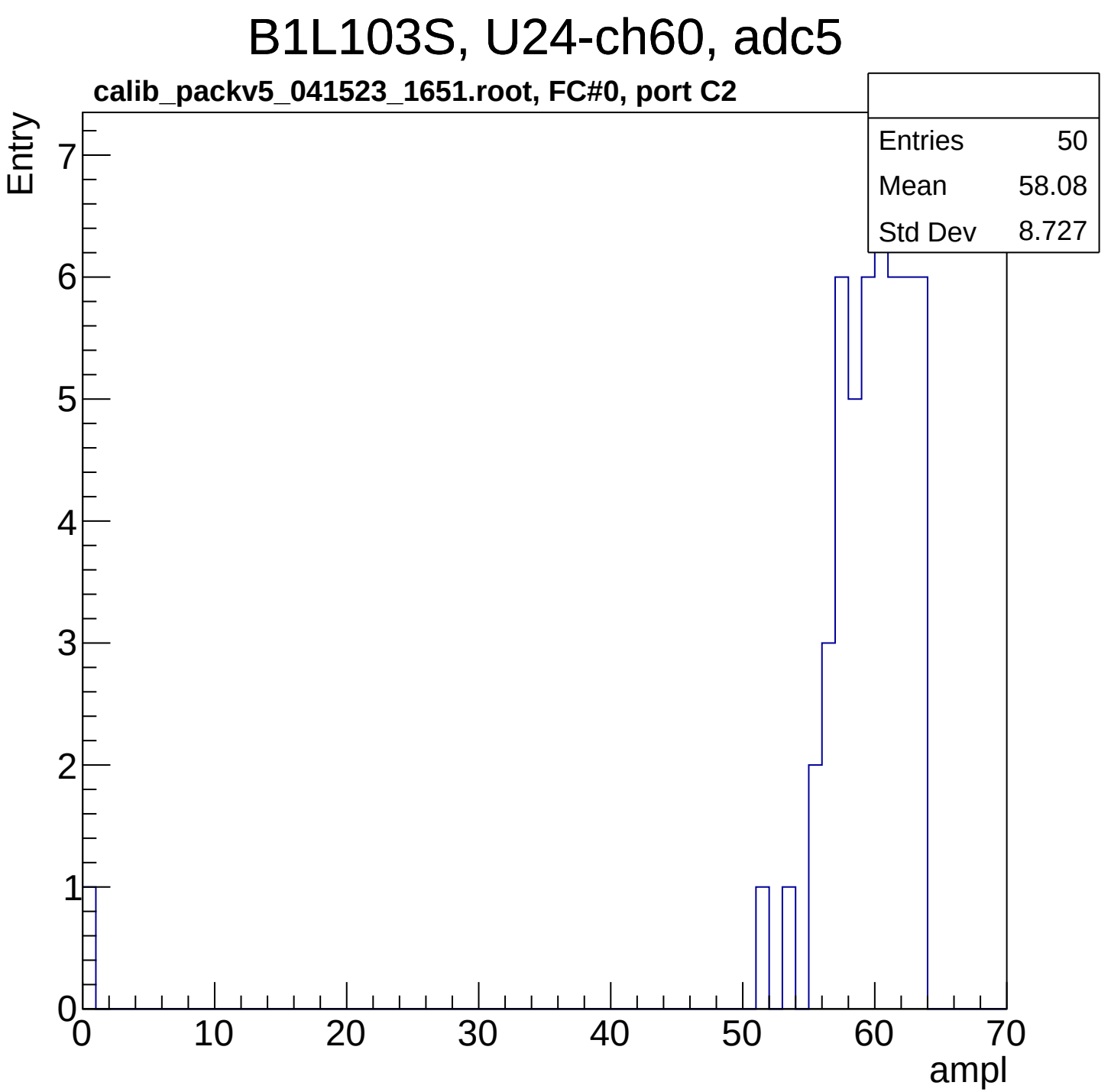
B1L103S, U24-ch60, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 58.08
Std Dev 8.727
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
30
40
50
60
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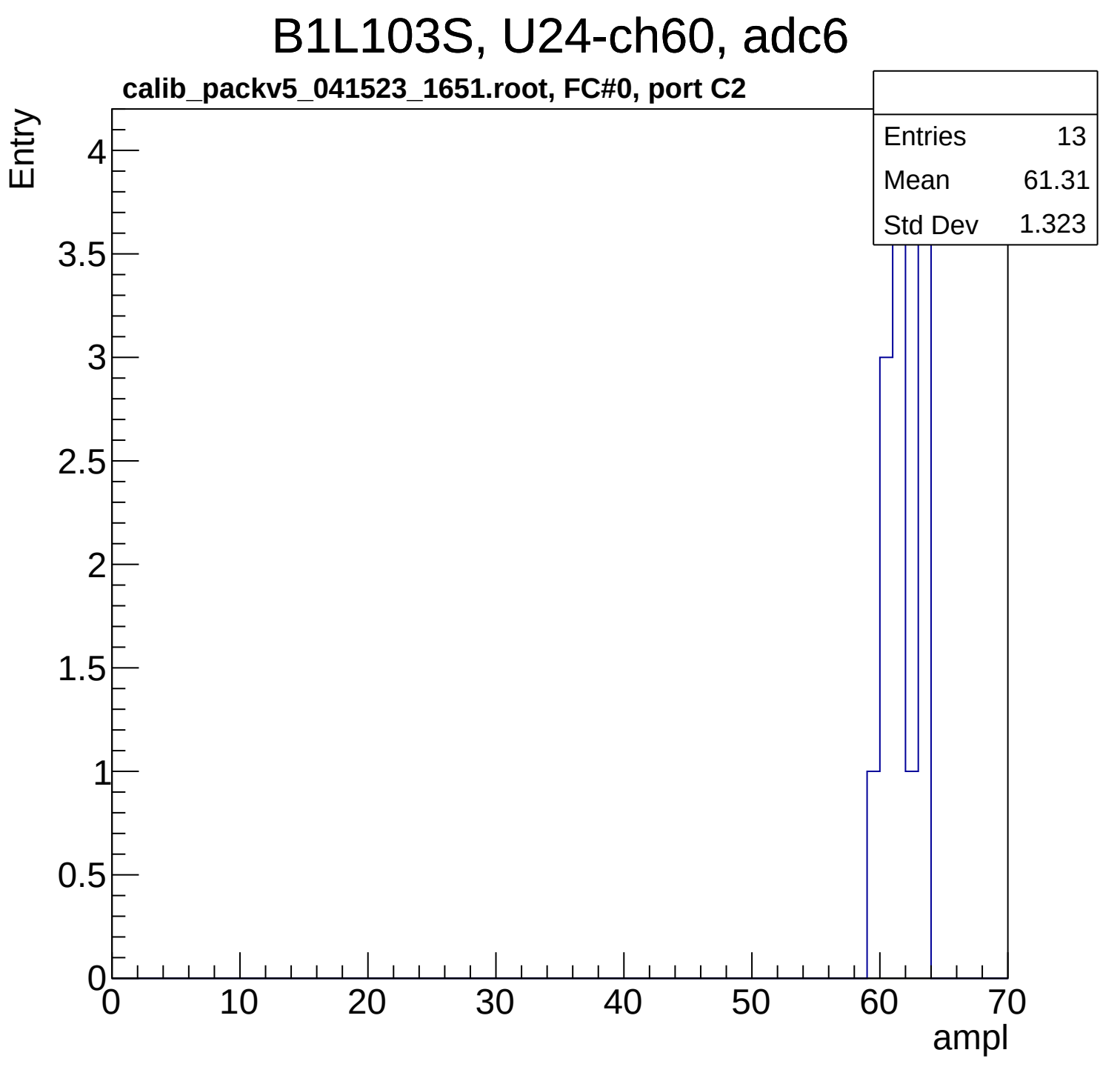
B1L103S, U24-ch60, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 13
Mean 61.31
Std Dev 1.323
Entry
ampl
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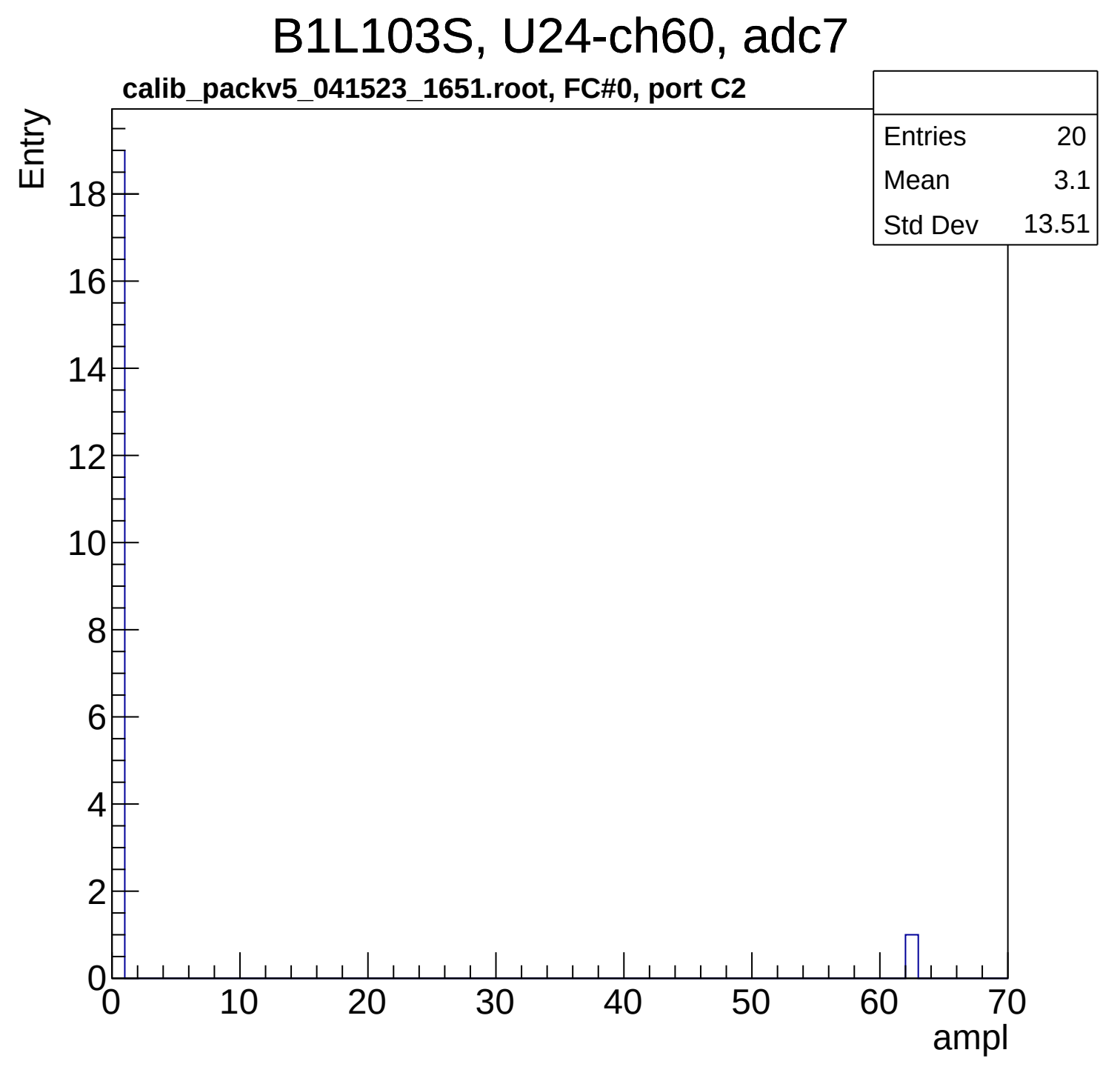
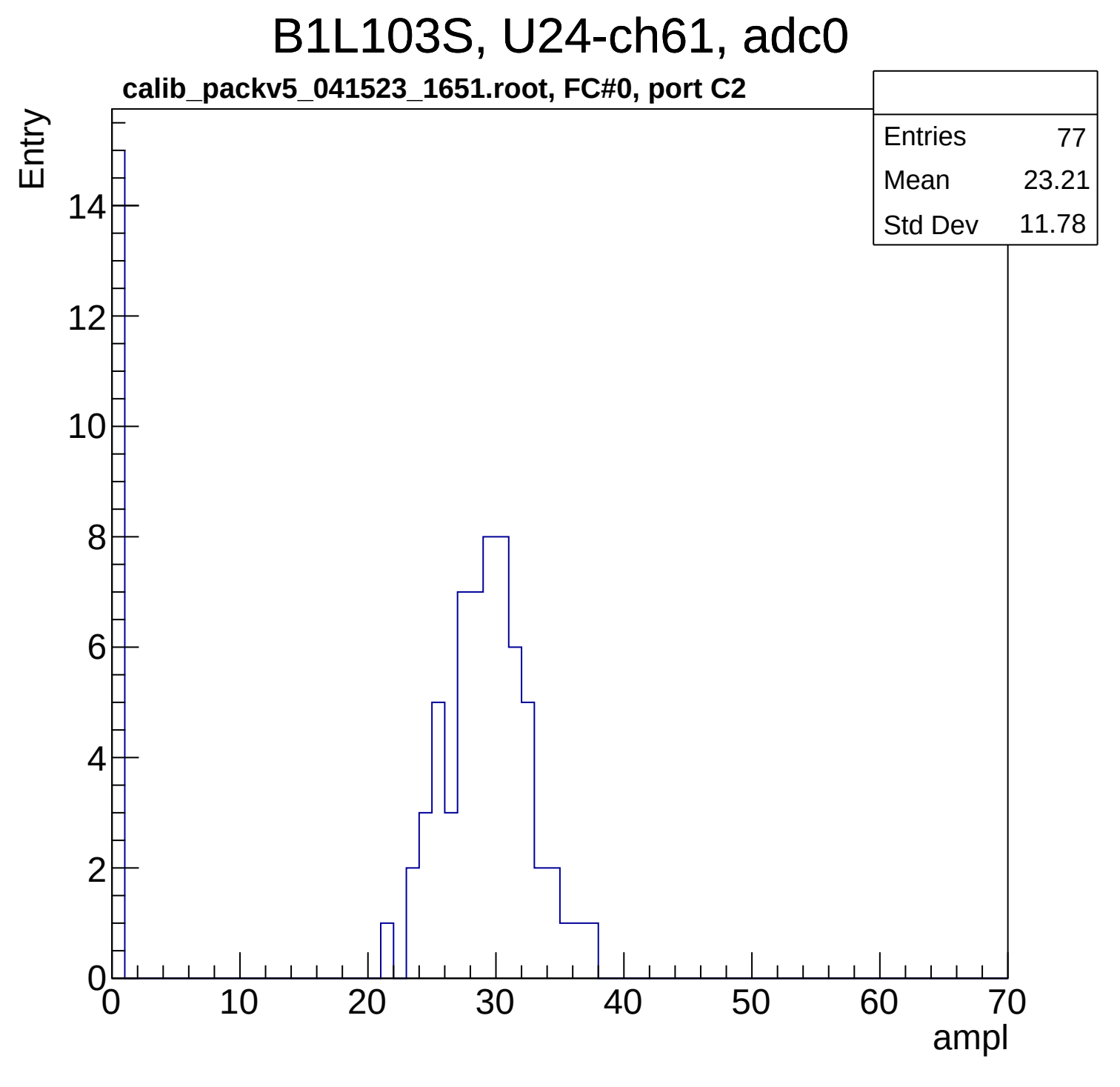
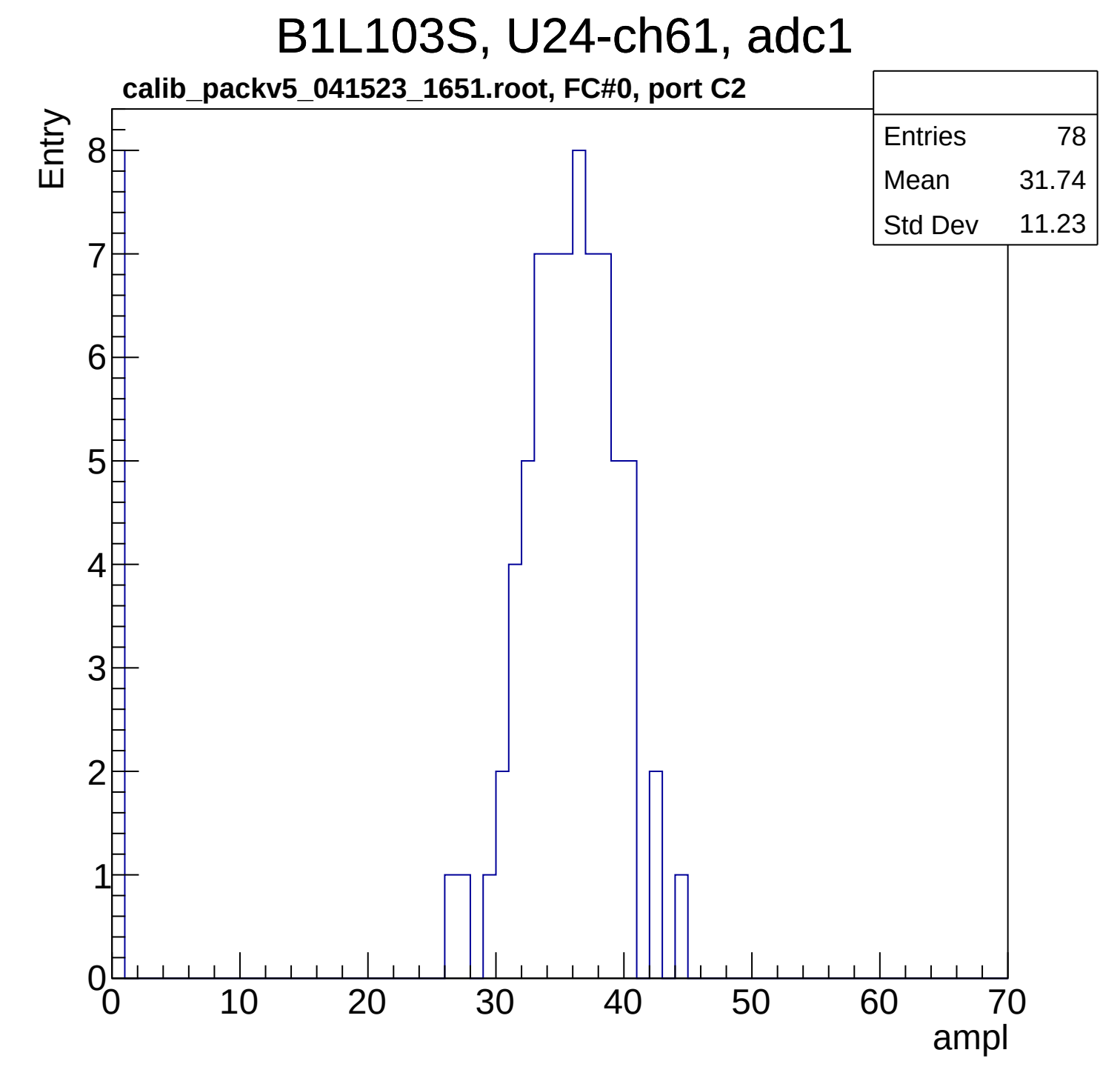
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U24-ch60, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.1
Std Dev 13.51
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch61, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 23.21
Std Dev 11.78
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch61, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 31.74
Std Dev 11.23
Entry
ampl
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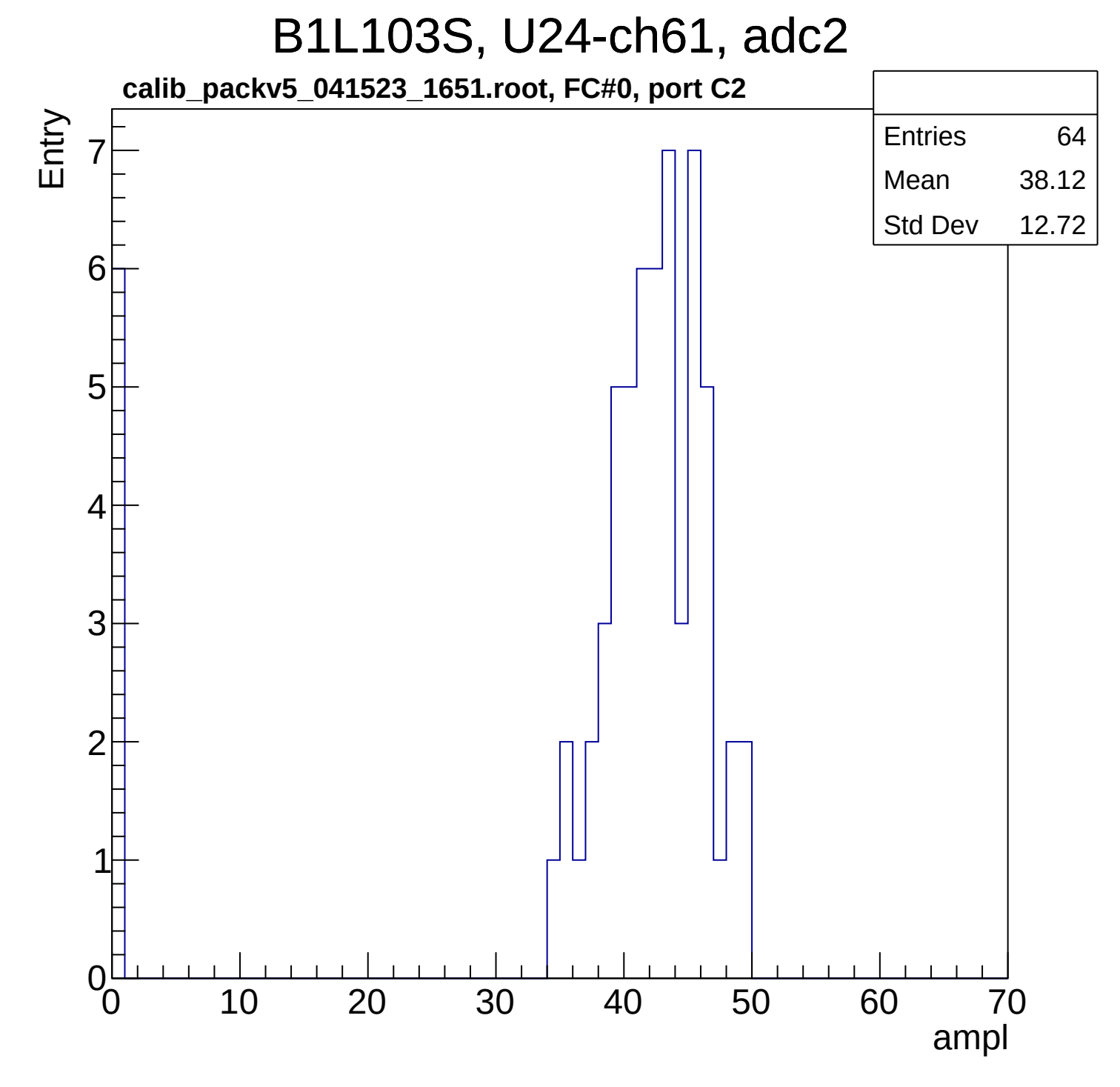
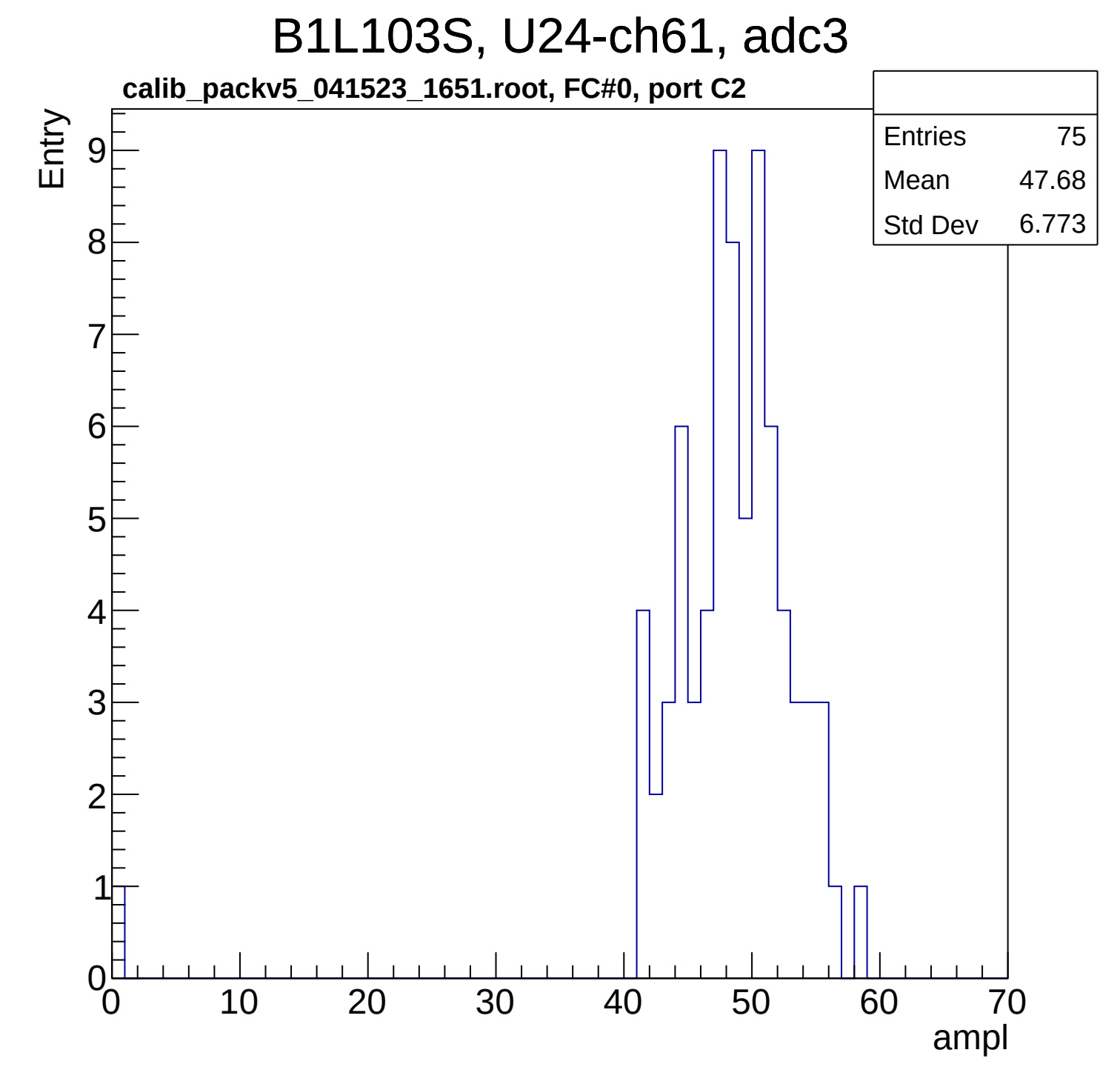
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U24-ch61, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 38.12
Std Dev 12.72
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U24-ch61, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 47.68
Std Dev 6.773
Entry
ampl
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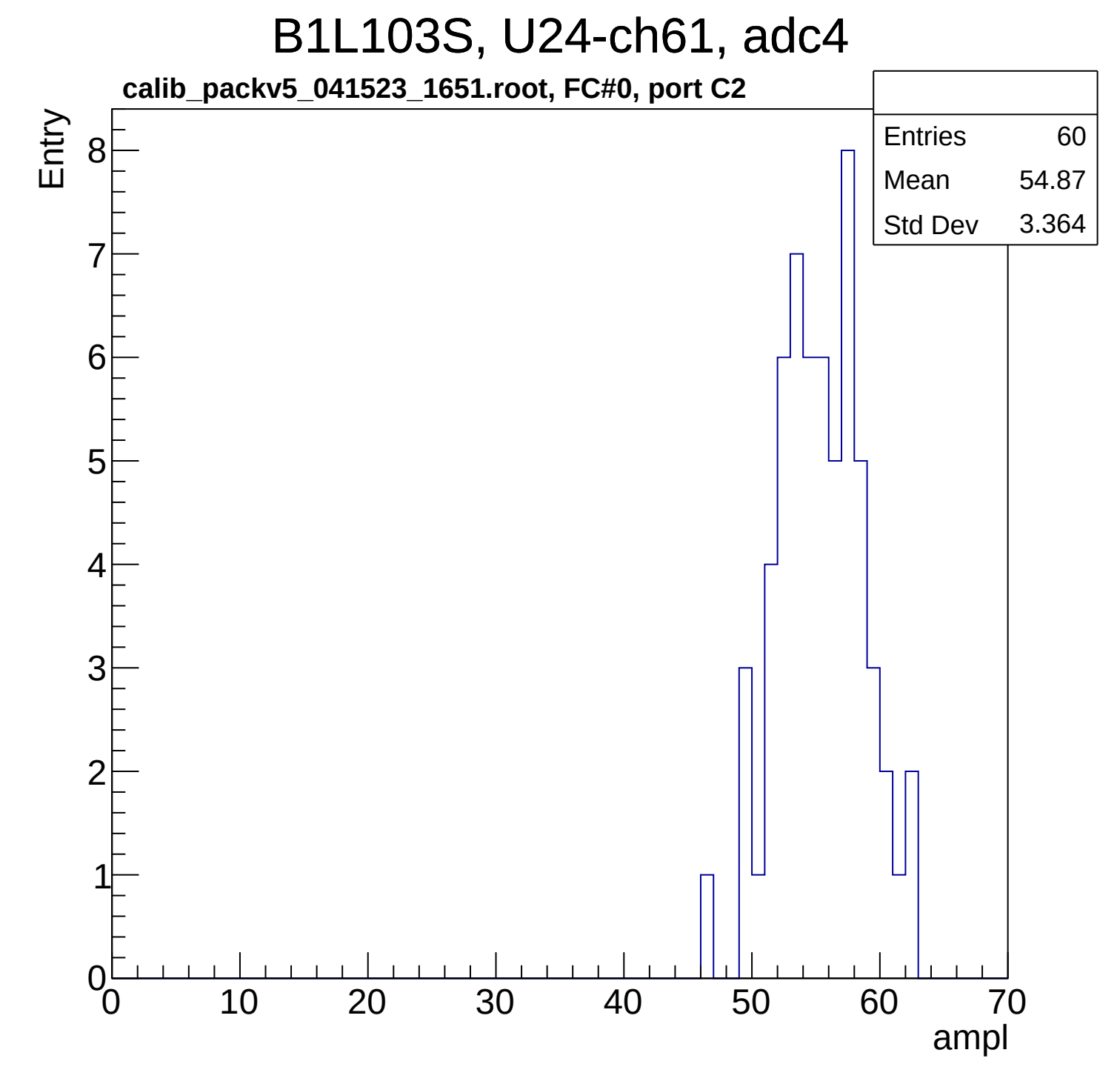
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U24-ch61, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 54.87
Std Dev 3.364
Entry
ampl
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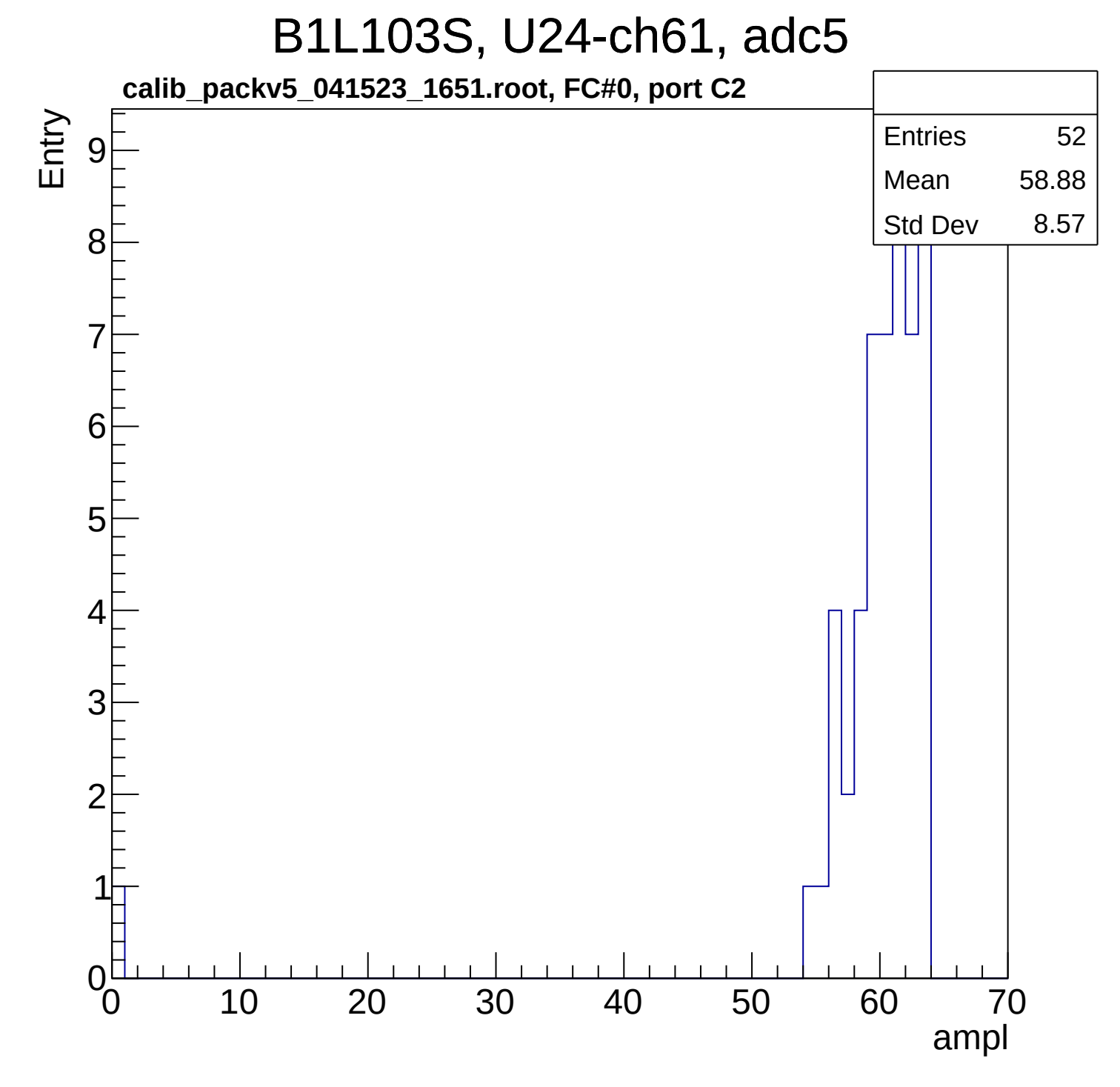
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U24-ch61, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 58.88
Std Dev 8.57
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
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20
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40
50
60
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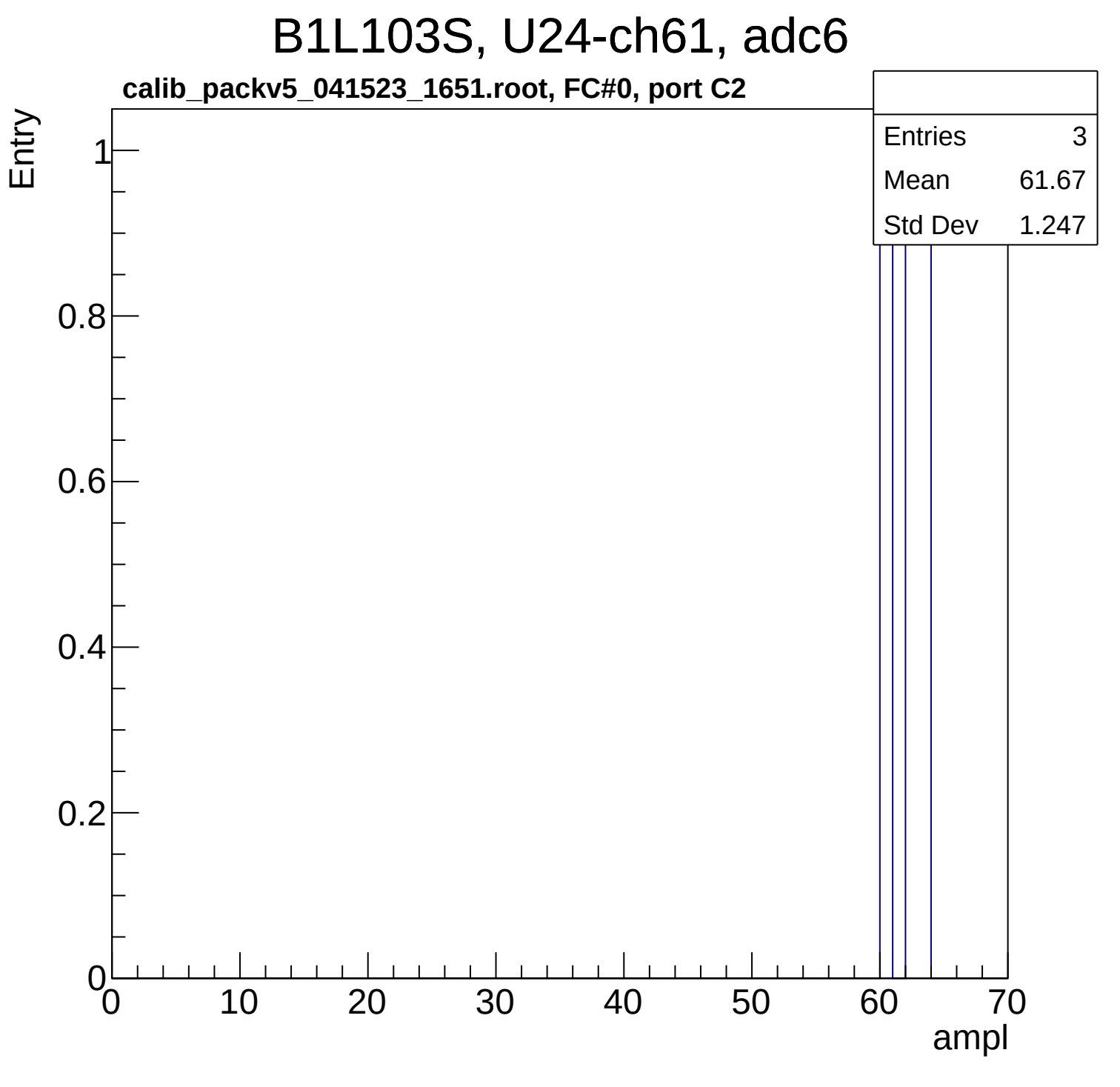
B1L103S, U24-ch61, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 3
Mean 61.67
Std Dev 1.247
Entry
ampl
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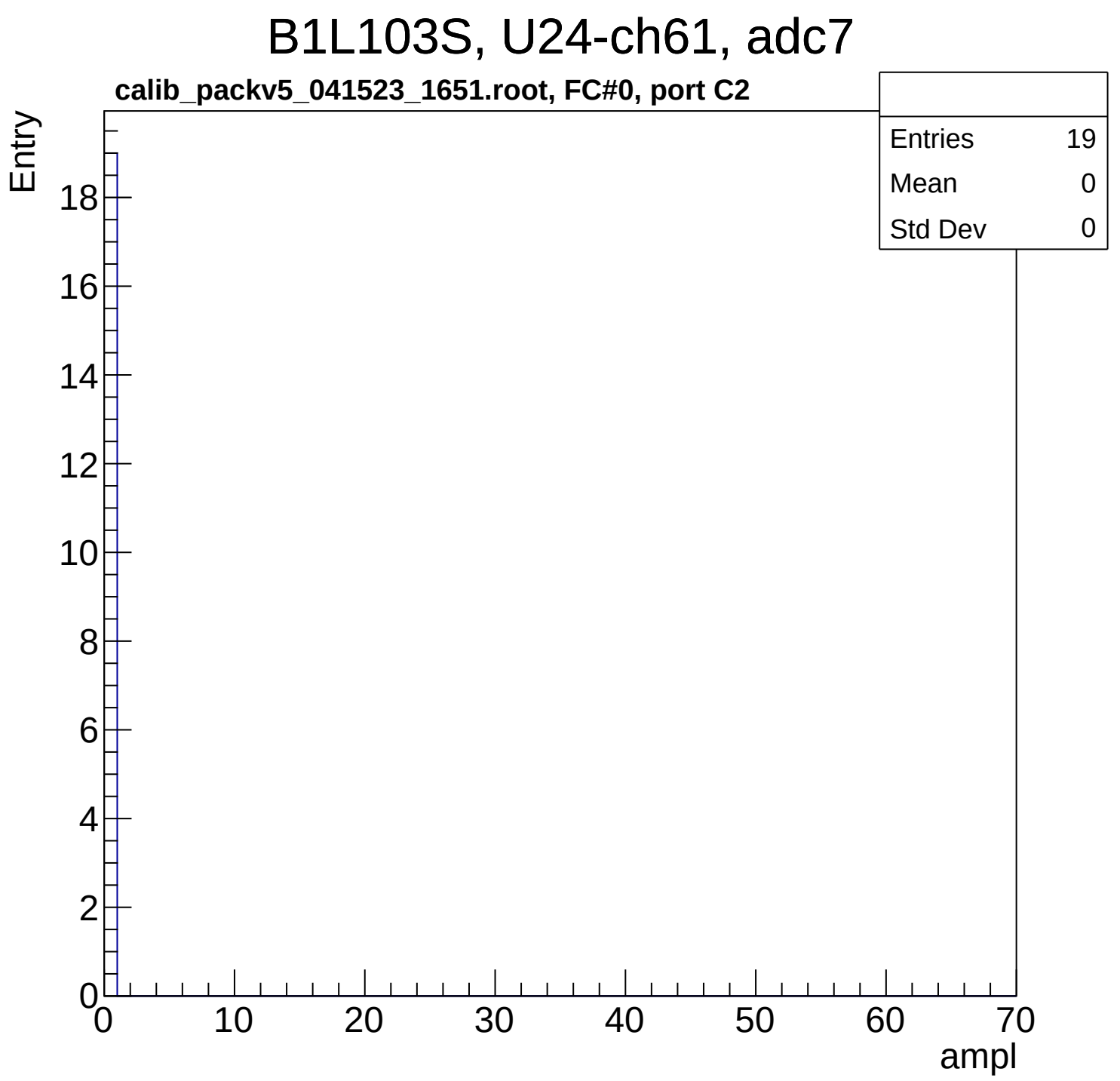
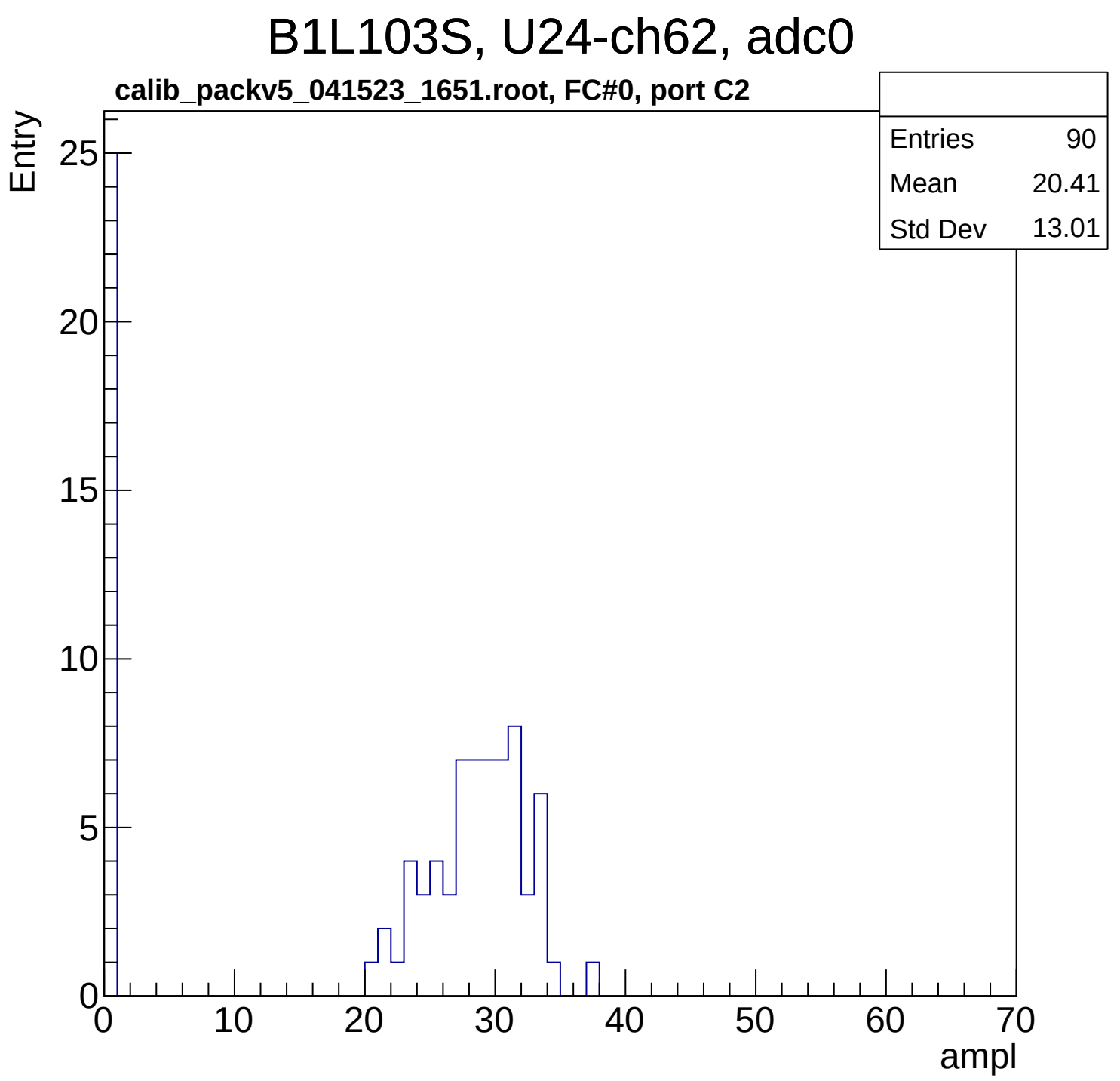
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70


B1L103S, U24-ch61, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch62, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 90
Mean 20.41
Std Dev 13.01
Entry
0
5
10
15
20
25
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10
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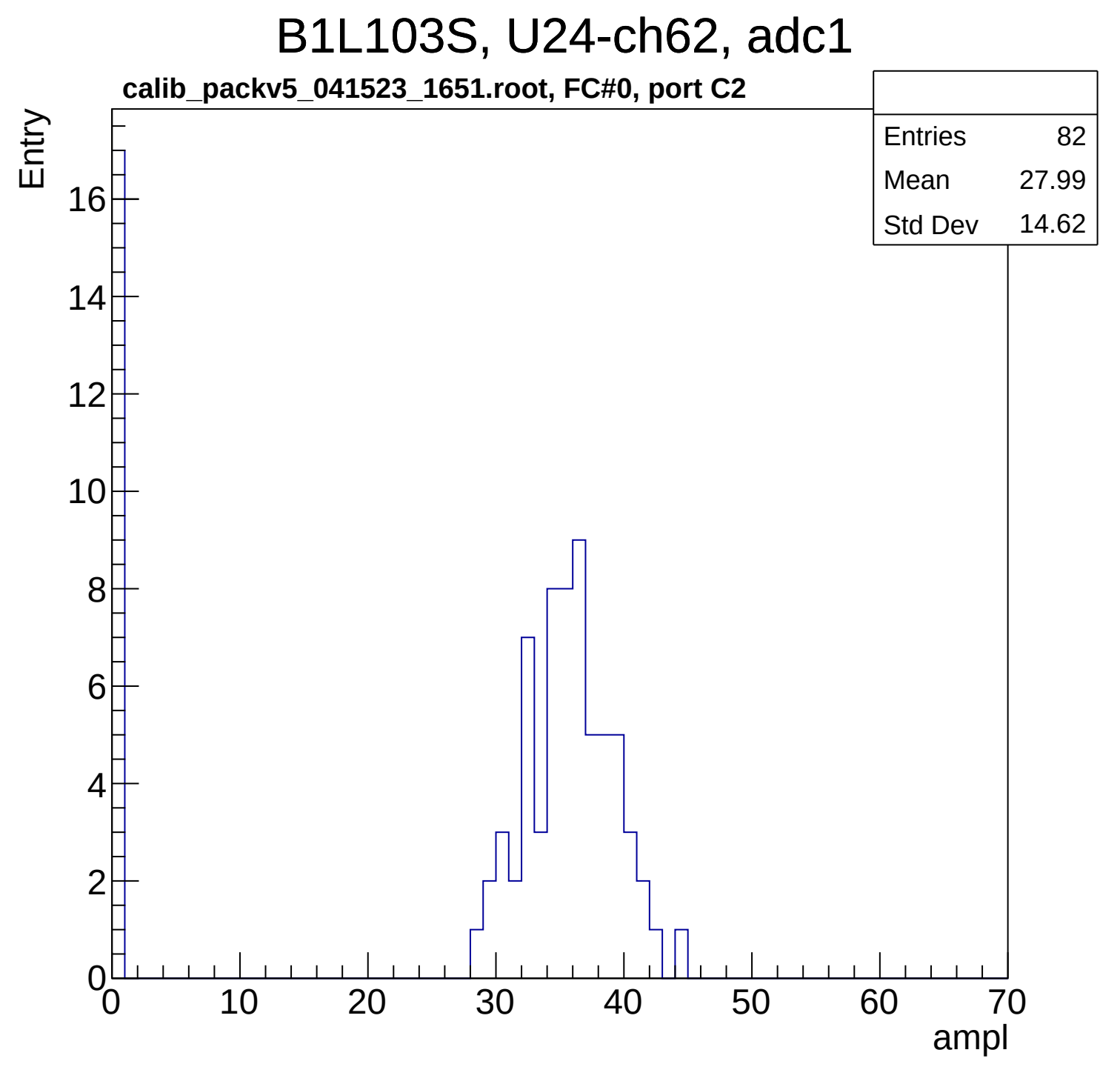
ampl


B1L103S, U24-ch62, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 27.99
Std Dev 14.62
Entry
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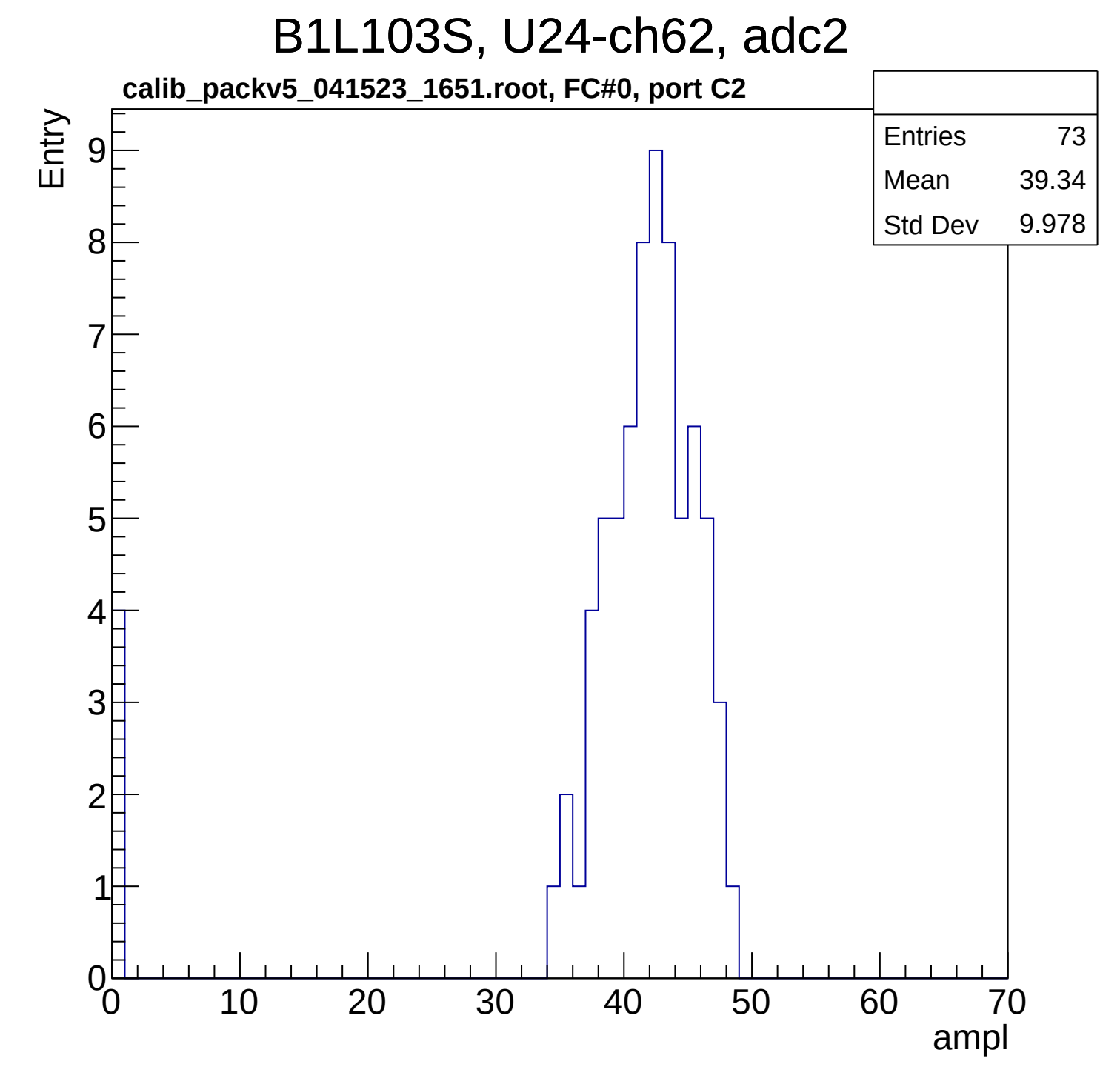
60
70
ampl


B1L103S, U24-ch62, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 39.34
Std Dev 9.978
Entry
ampl
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3
4
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6
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0
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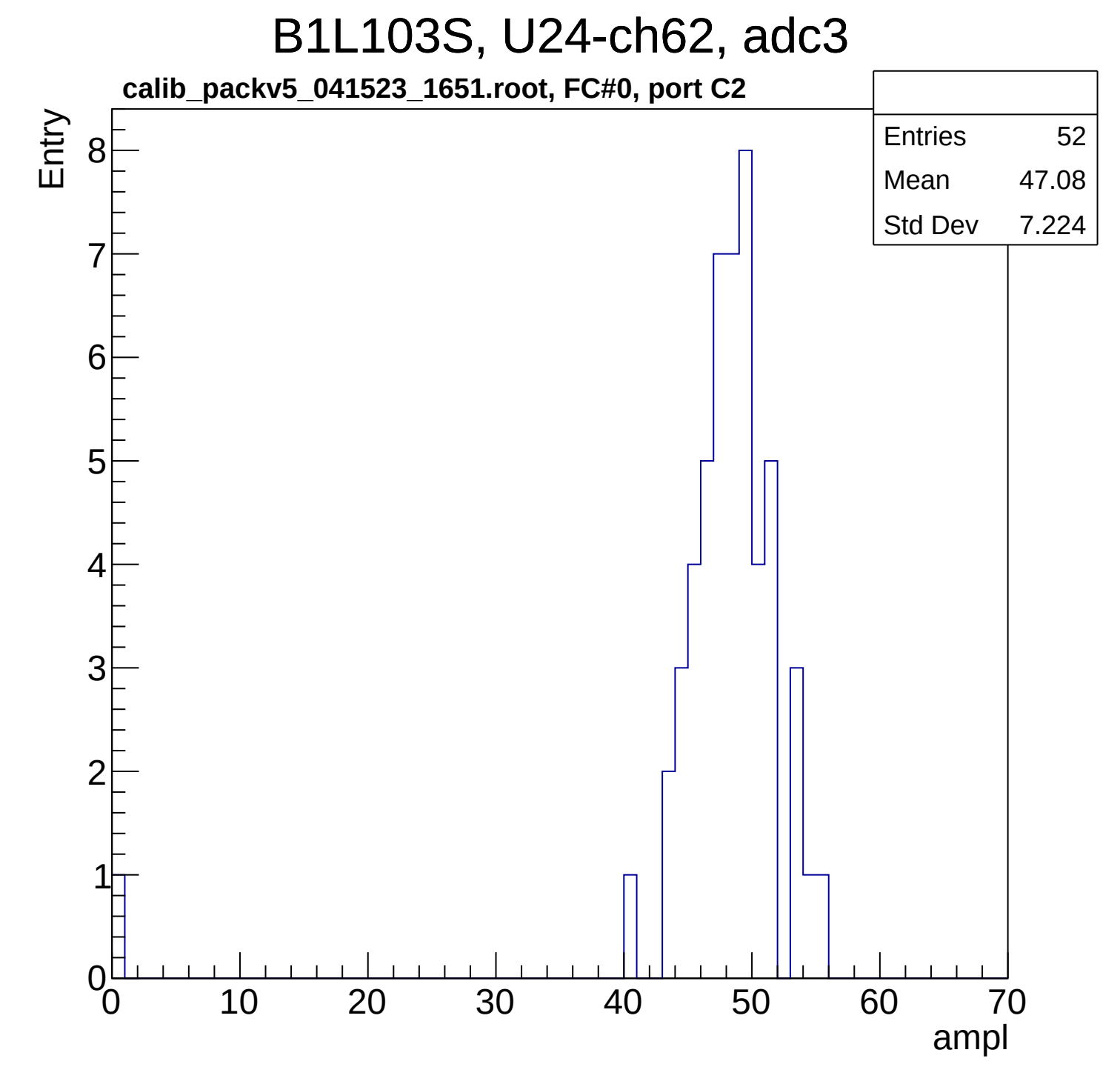
B1L103S, U24-ch62, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 47.08
Std Dev 7.224
Entry
ampl
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1
2
3
4
5
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7
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0
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40
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60
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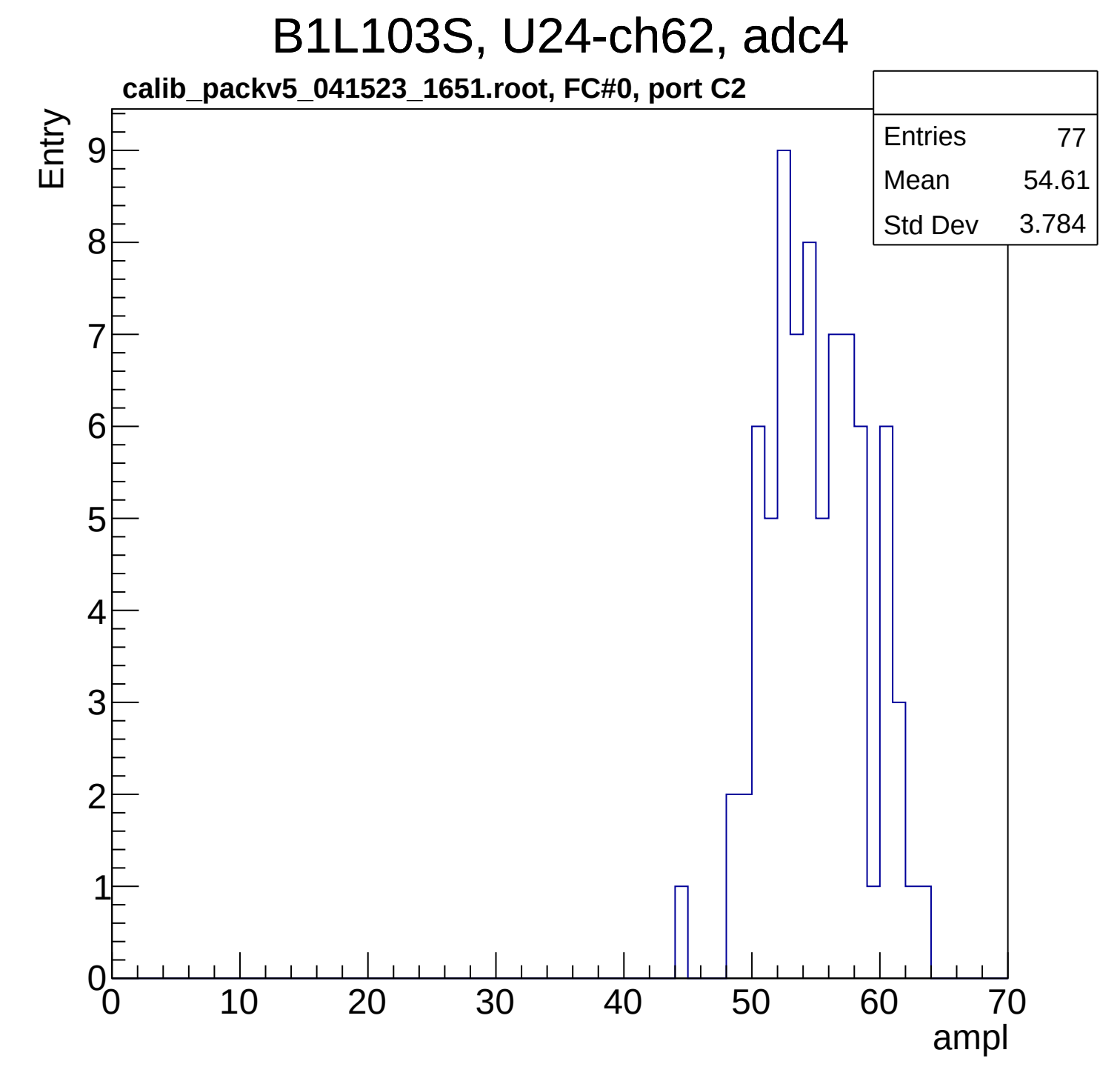
B1L103S, U24-ch62, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 54.61
Std Dev 3.784
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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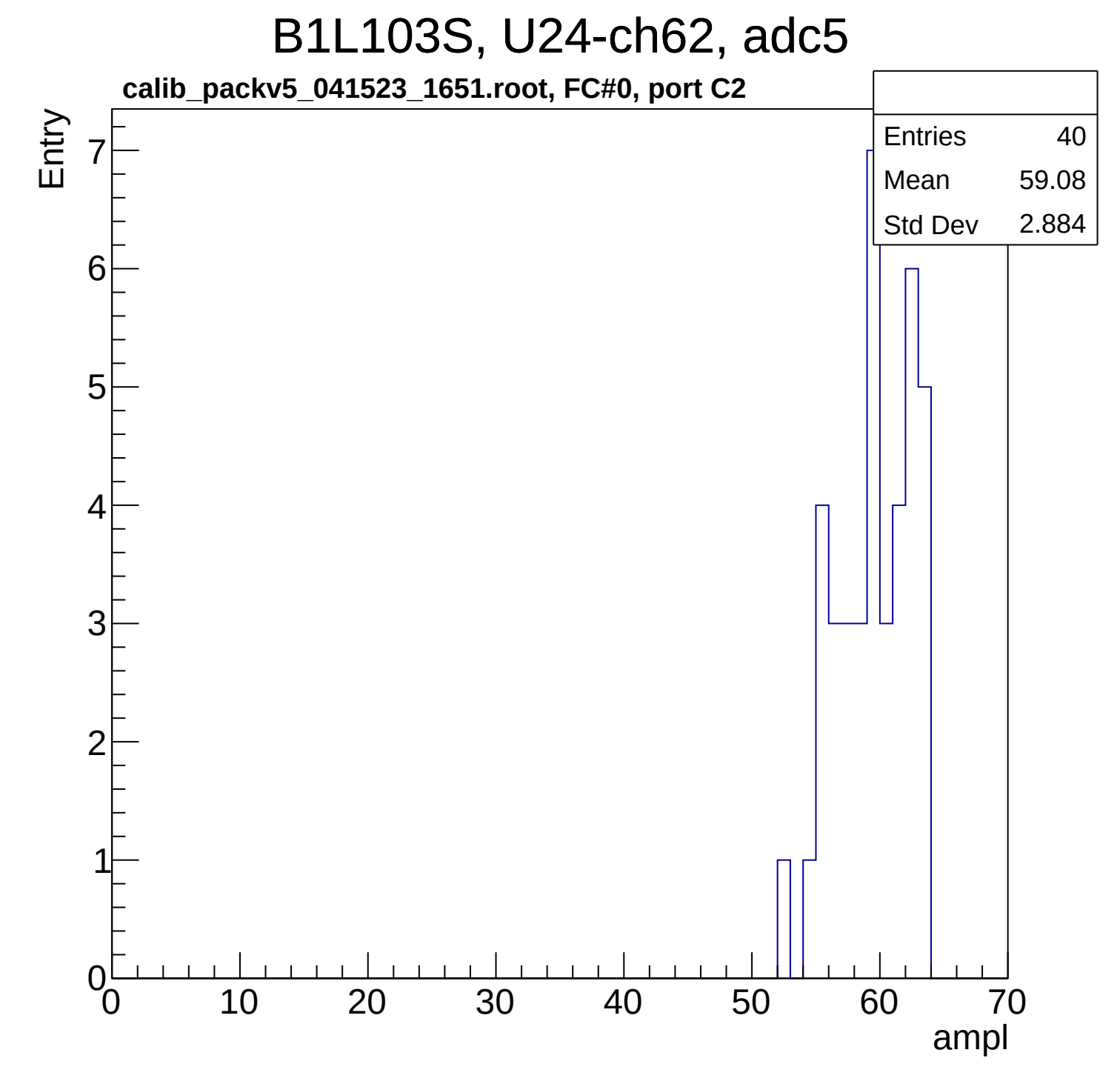
B1L103S, U24-ch62, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 40
Mean 59.08
Std Dev 2.884
Entry
ampl
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0
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40
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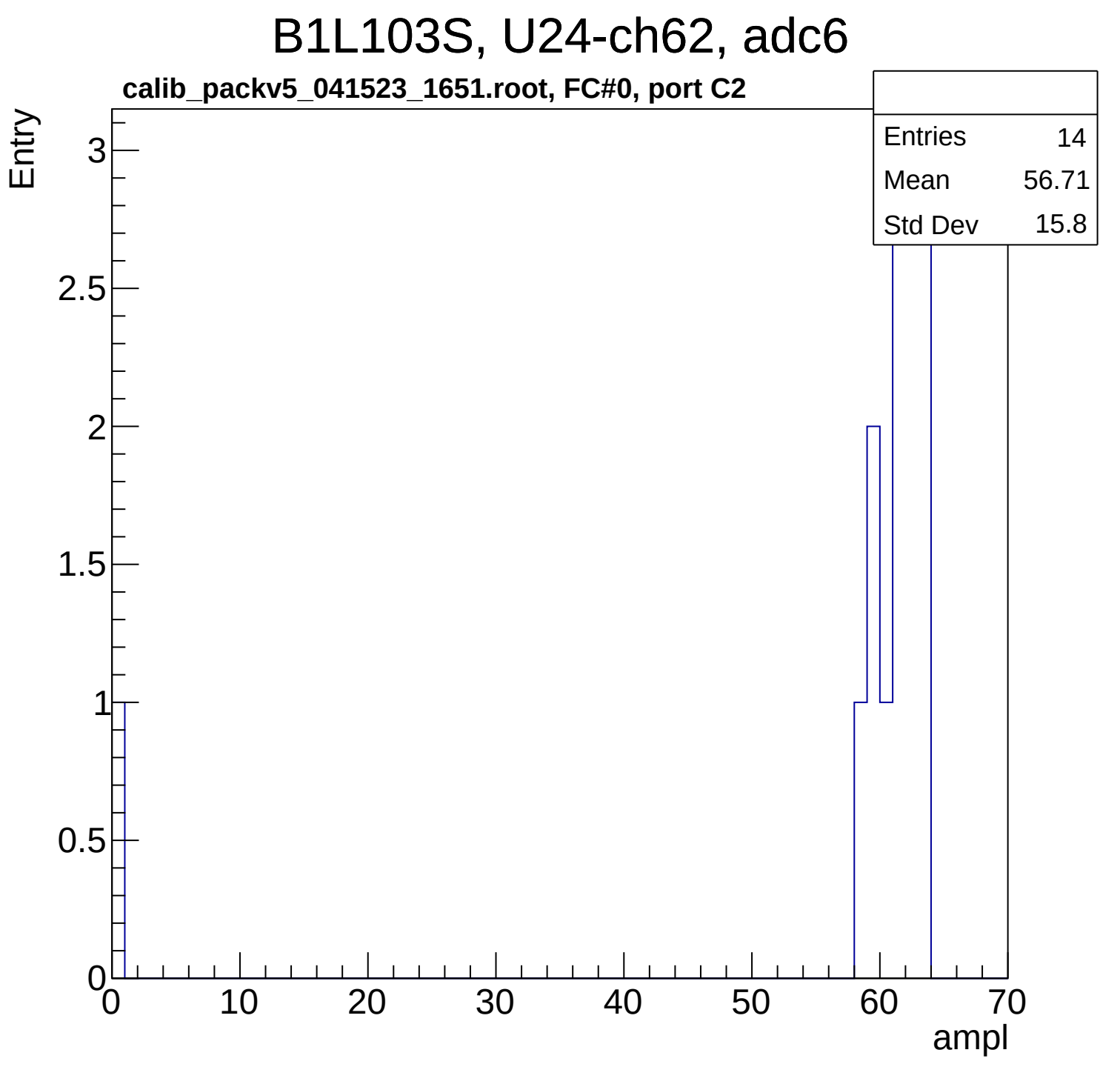
B1L103S, U24-ch62, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 14
Mean 56.71
Std Dev 15.8
Entry
ampl
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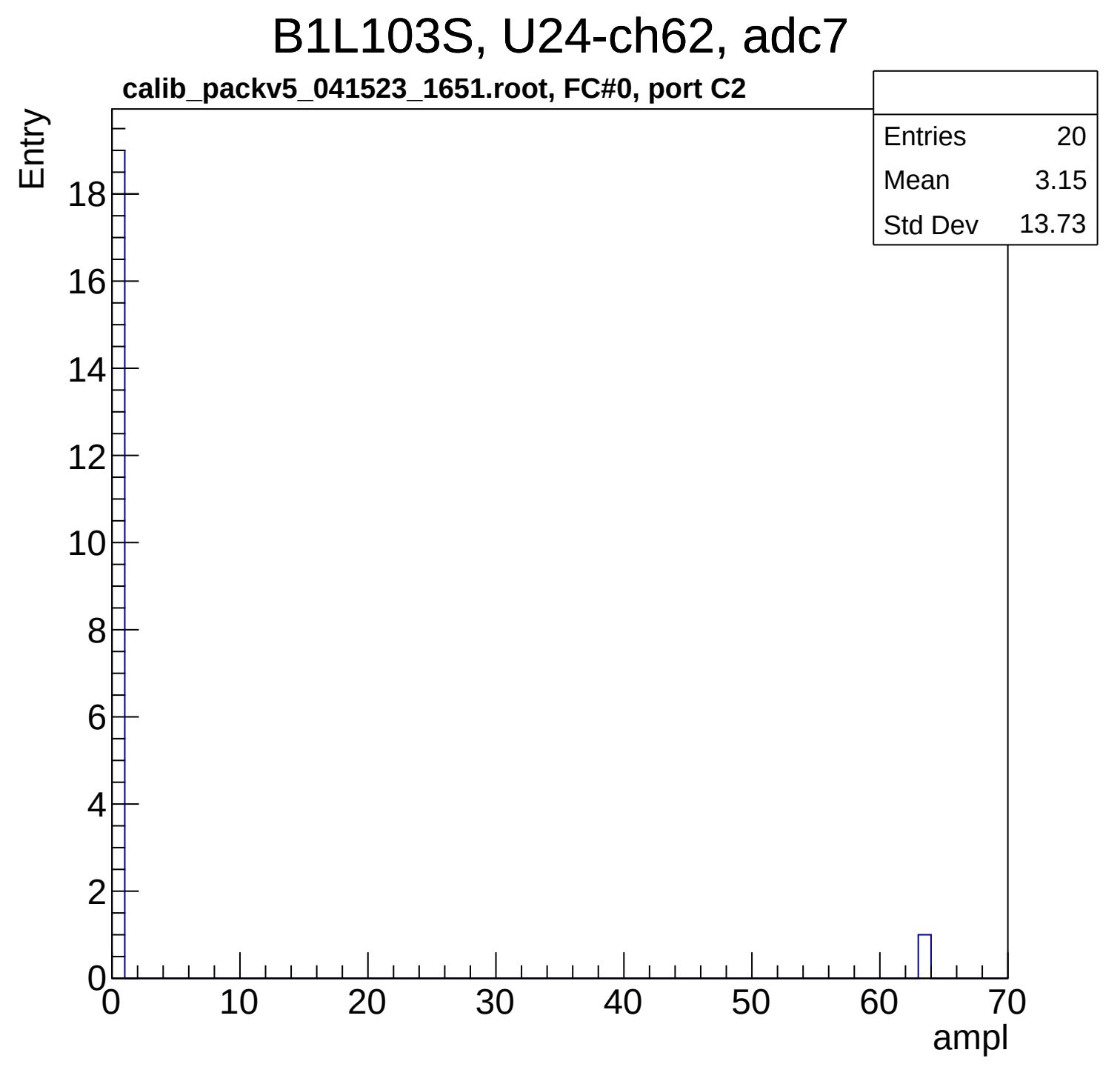
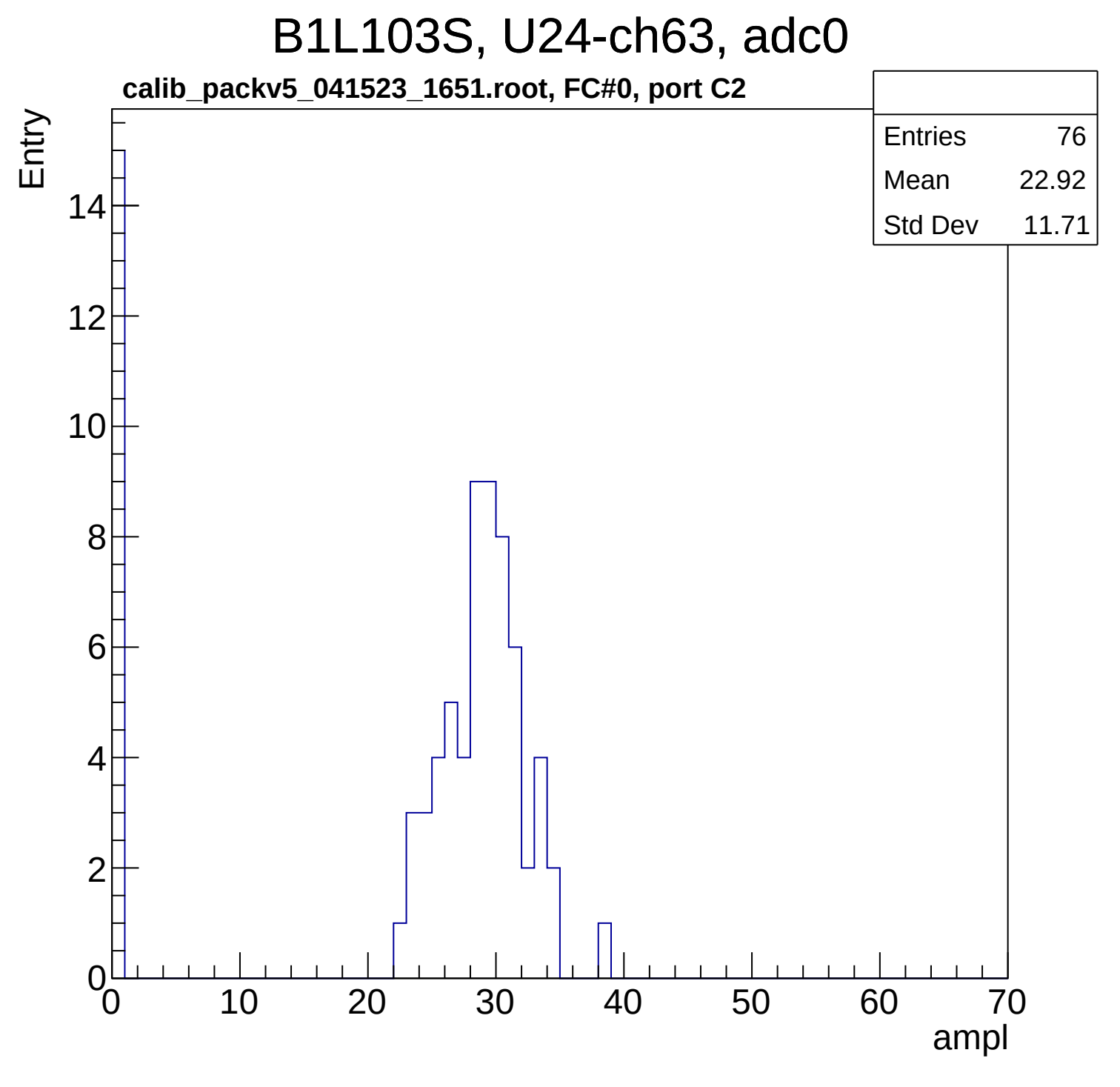
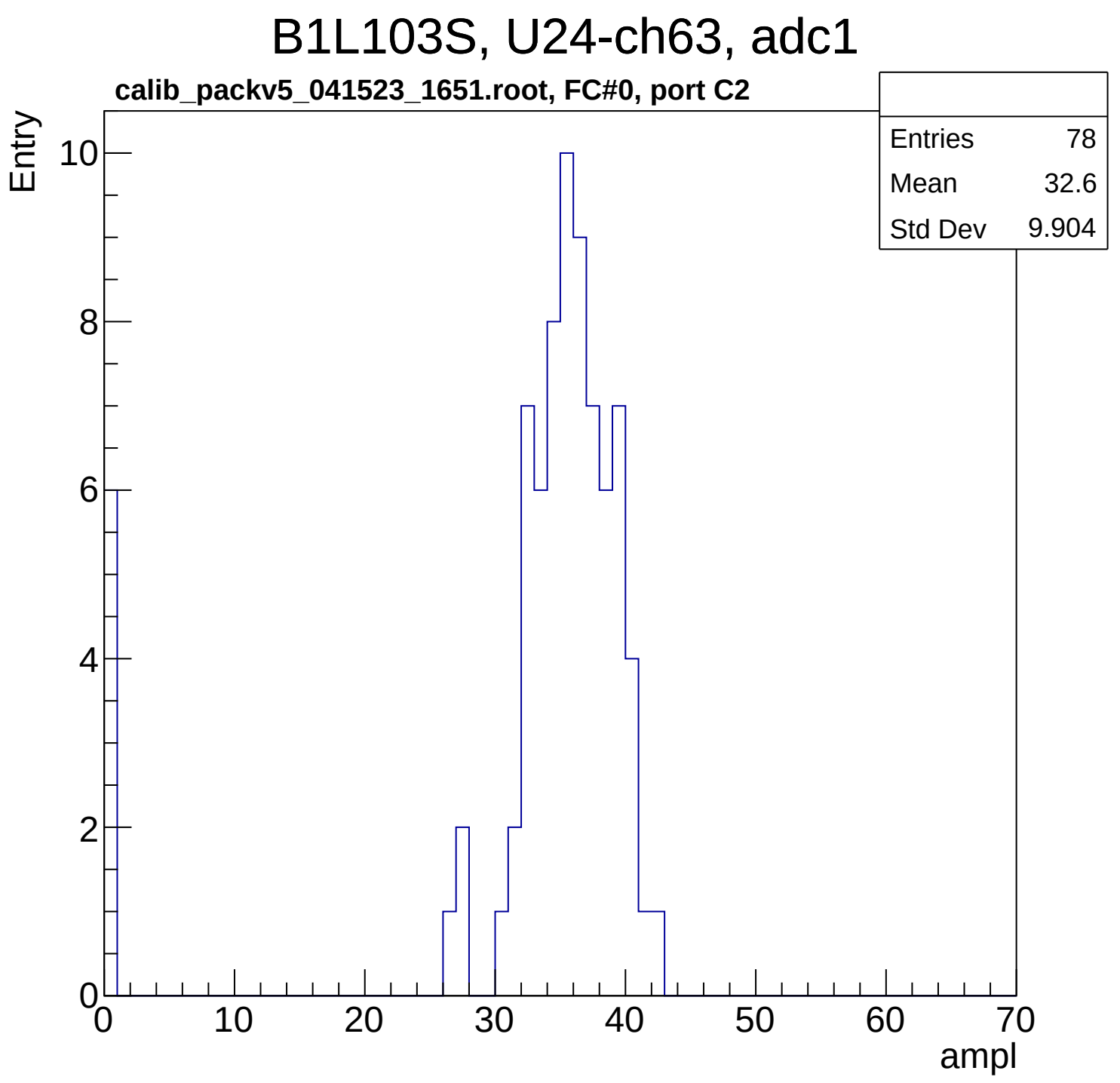
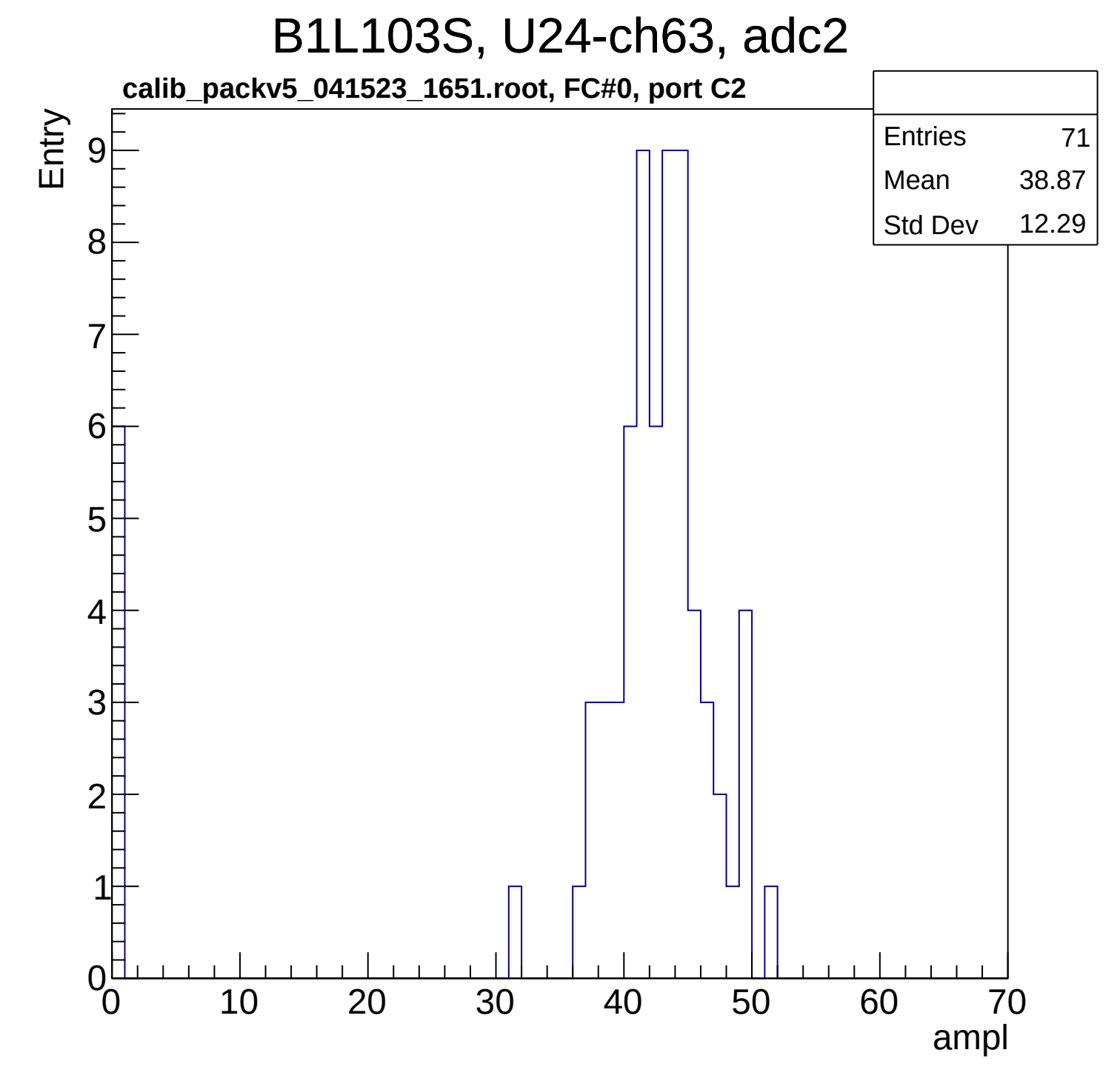
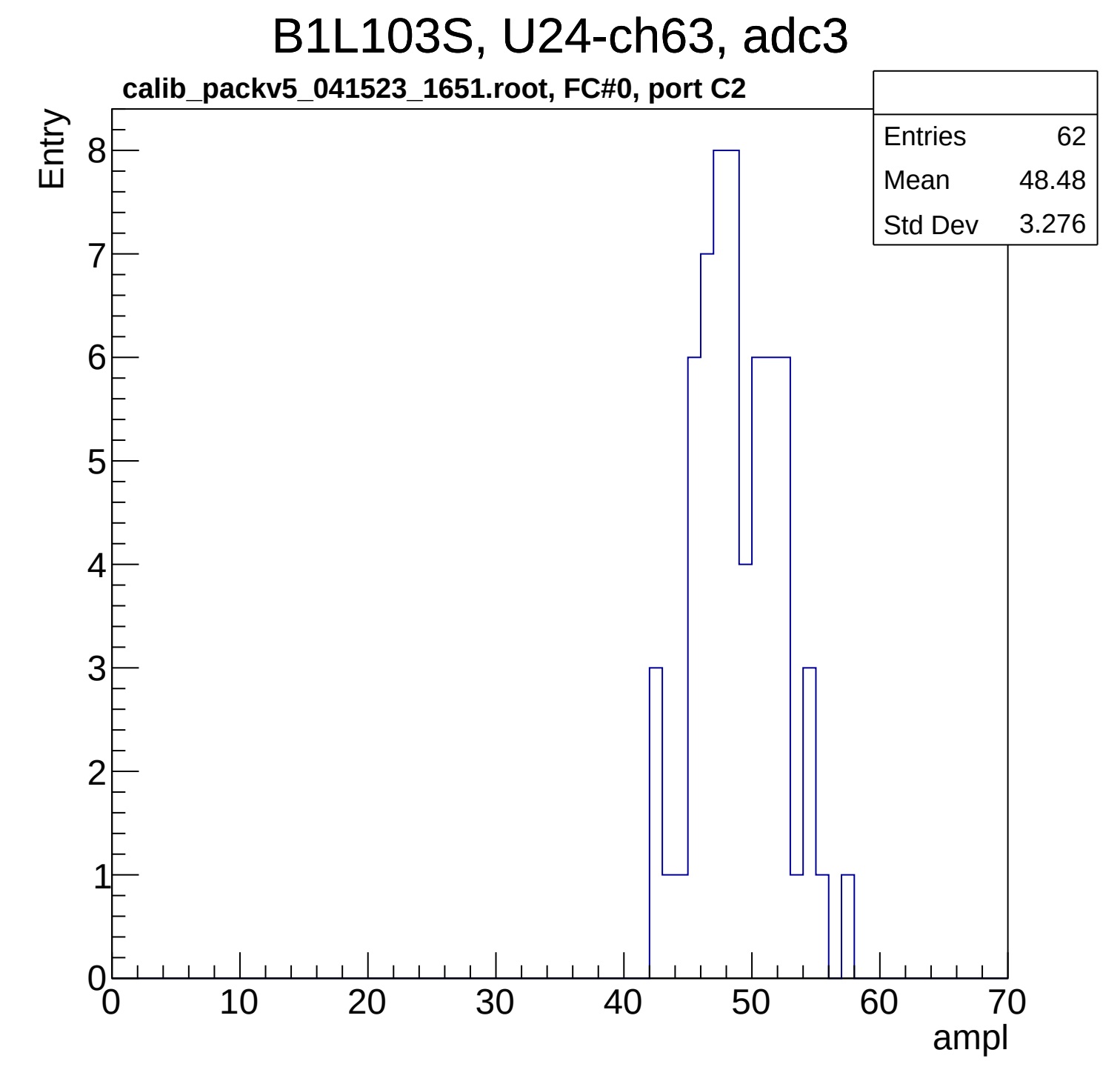
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U24-ch62, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch63, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 22.92
Std Dev 11.71
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch63, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 32.6
Std Dev 9.904
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch63, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 38.87
Std Dev 12.29
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U24-ch63, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 48.48
Std Dev 3.276
Entry
ampl
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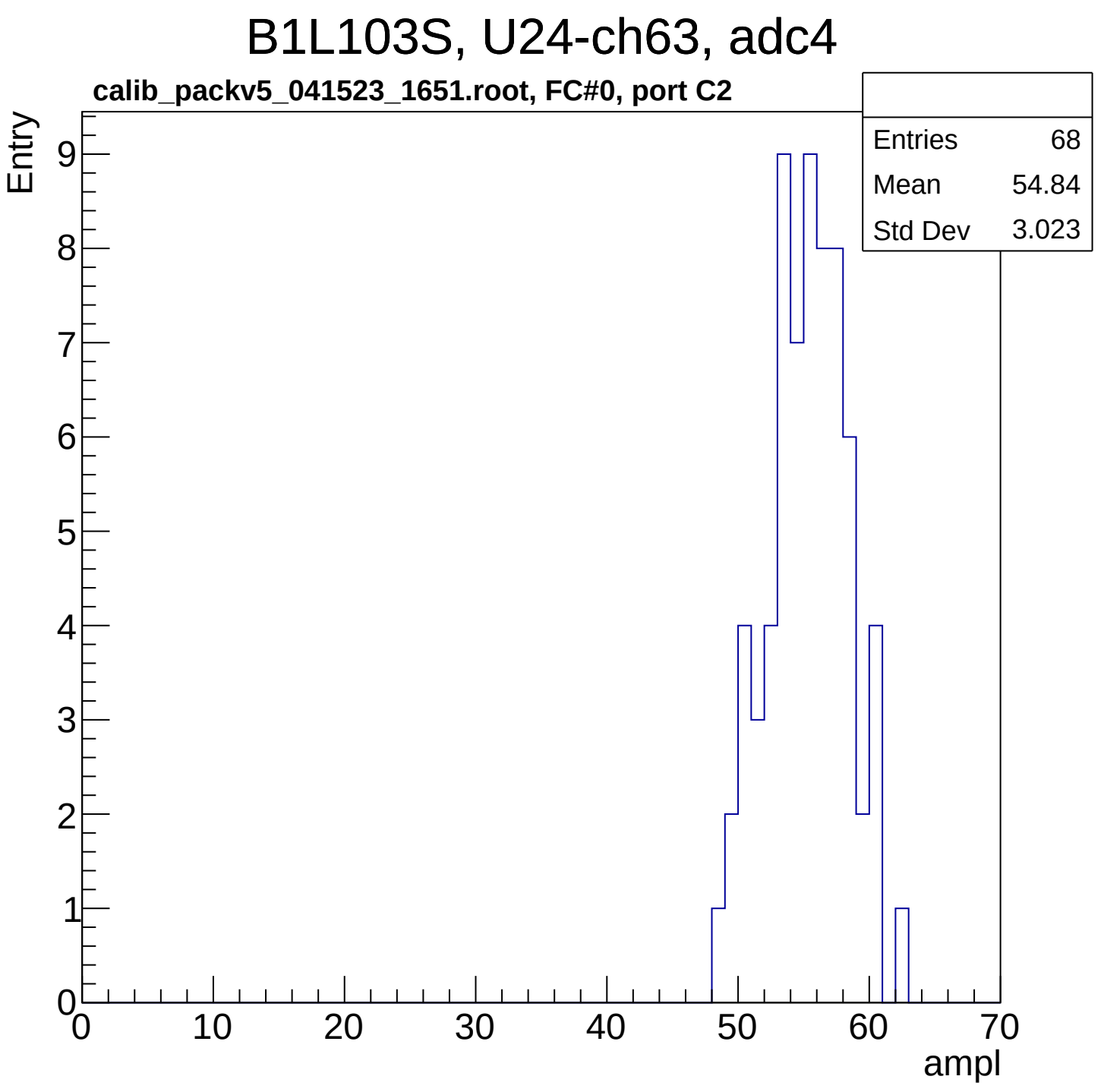
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U24-ch63, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 54.84
Std Dev 3.023
Entry
ampl
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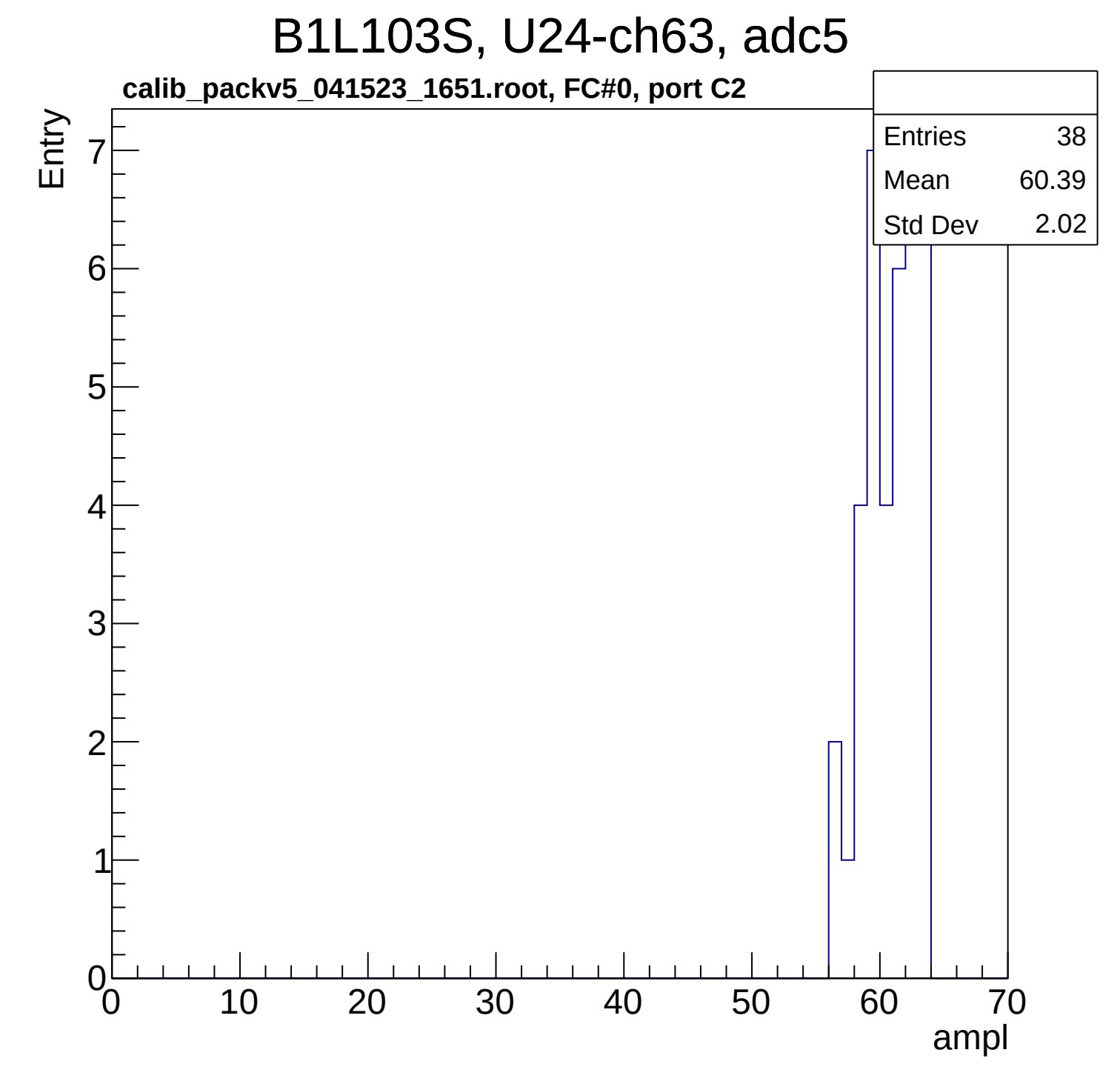
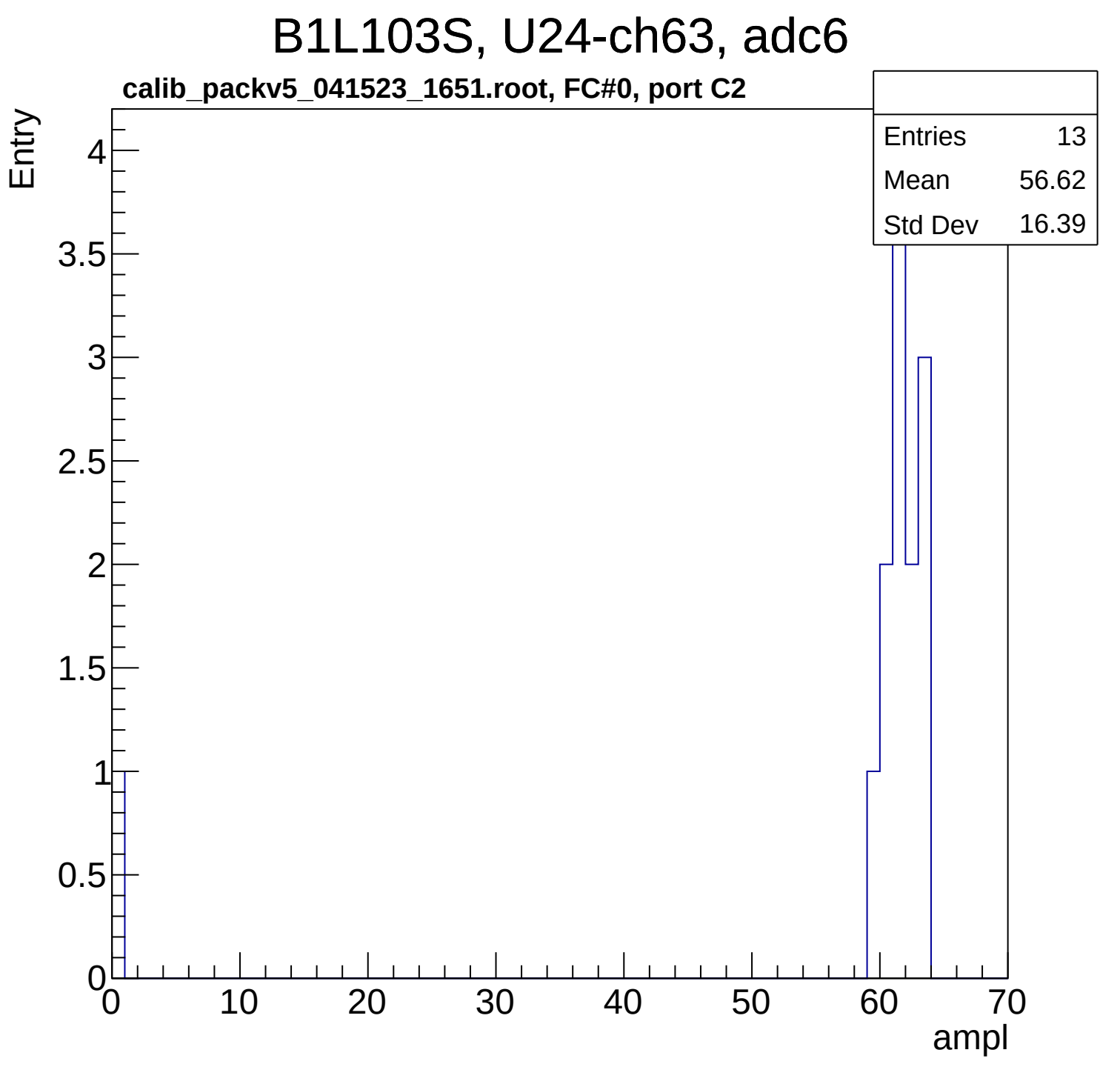
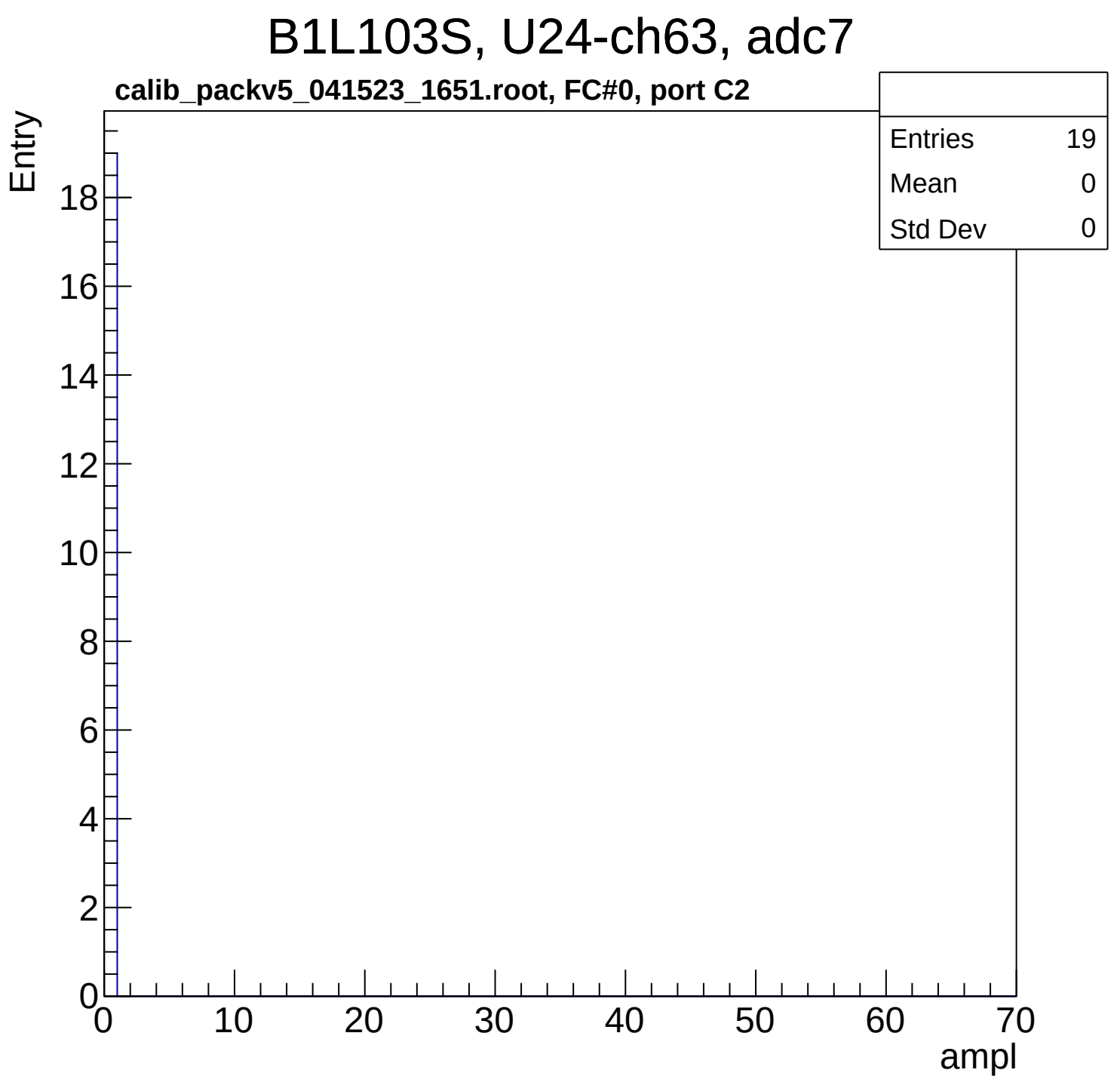
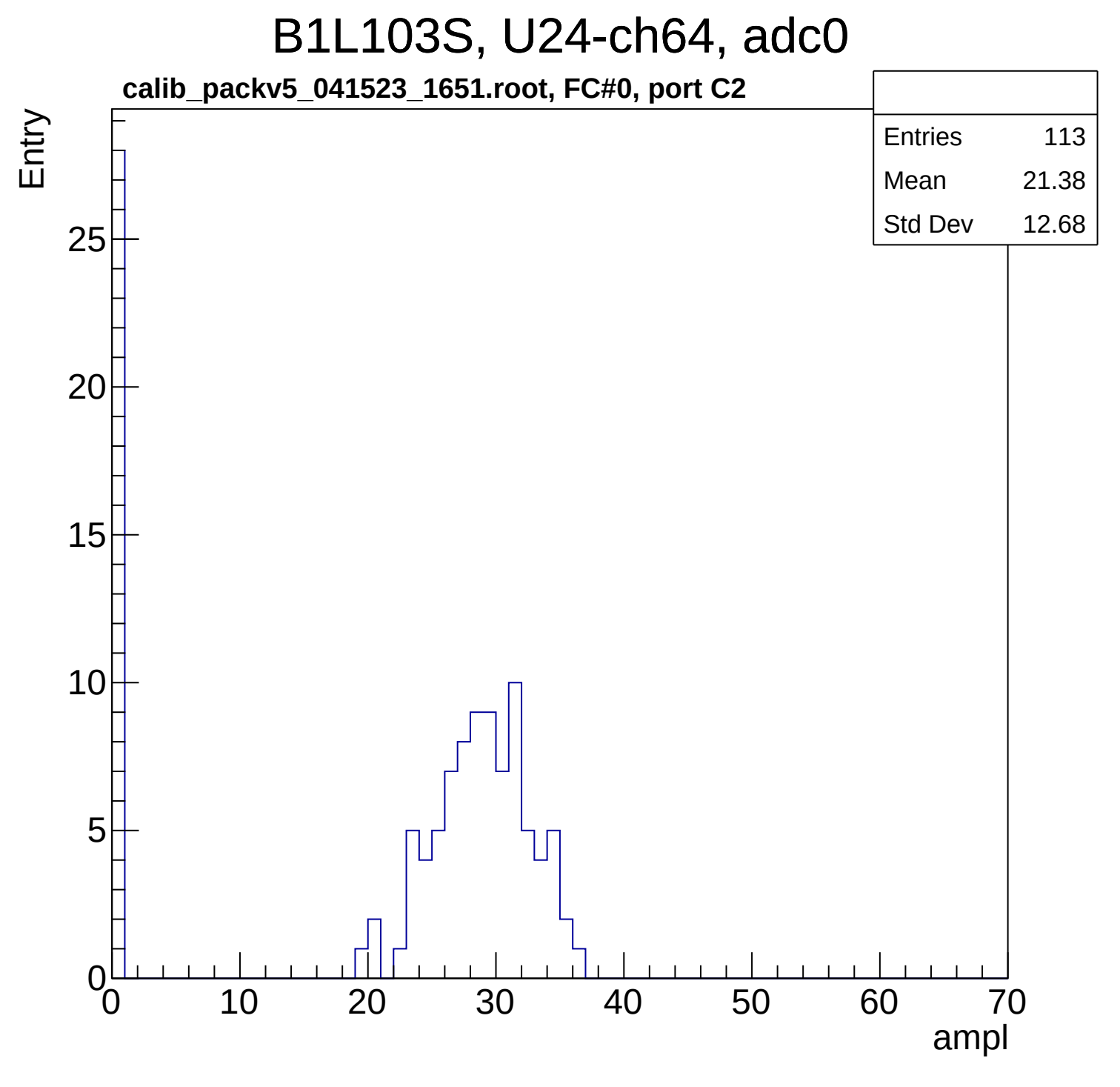
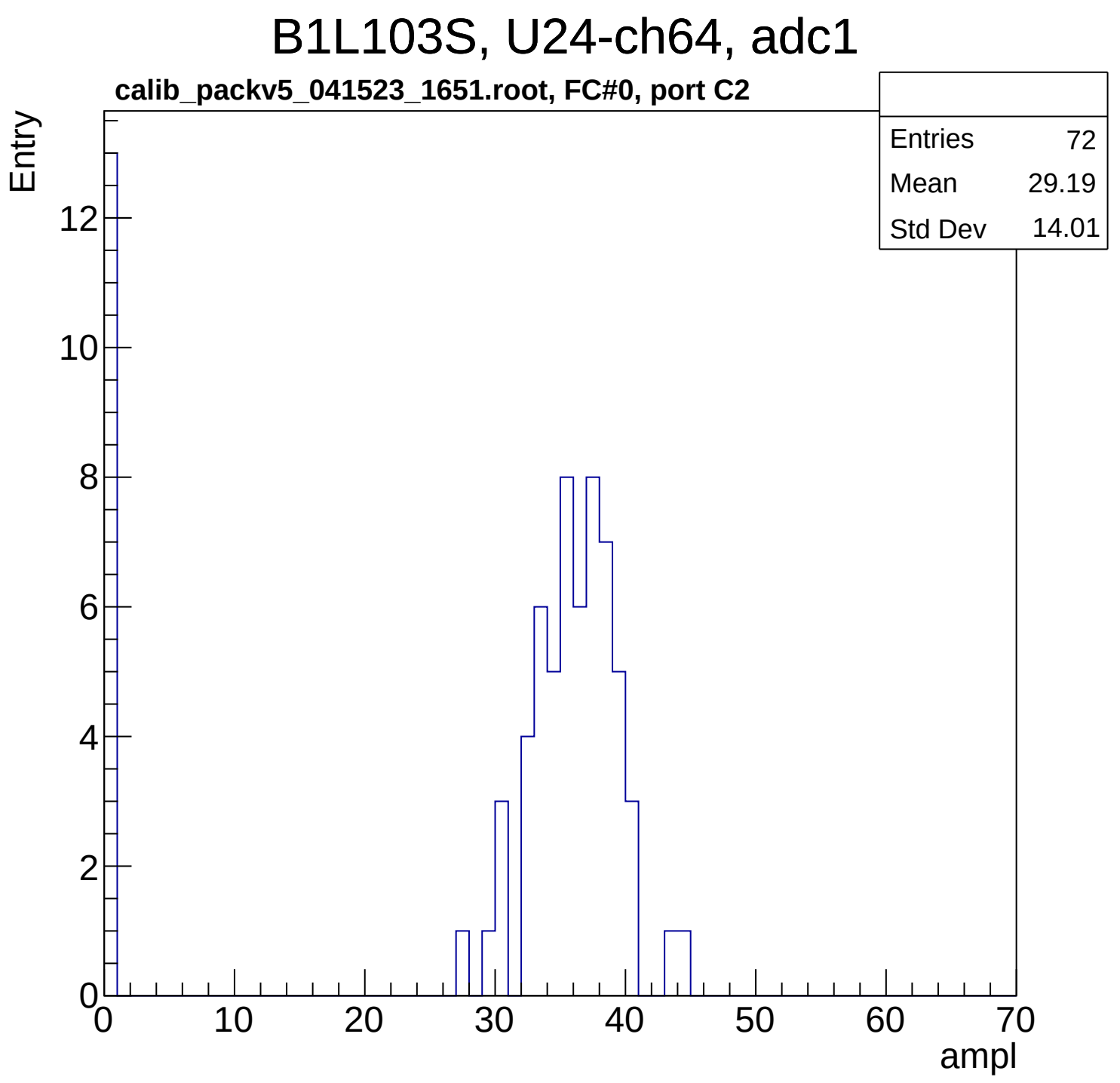
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U24-ch63, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 38
Mean 60.39
Std Dev 2.02
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U24-ch63, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 13
Mean 56.62
Std Dev 16.39
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U24-ch63, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch64, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 113
Mean 21.38
Std Dev 12.68
Entry
0
5
10
15
20
25
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch64, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 29.19
Std Dev 14.01
Entry
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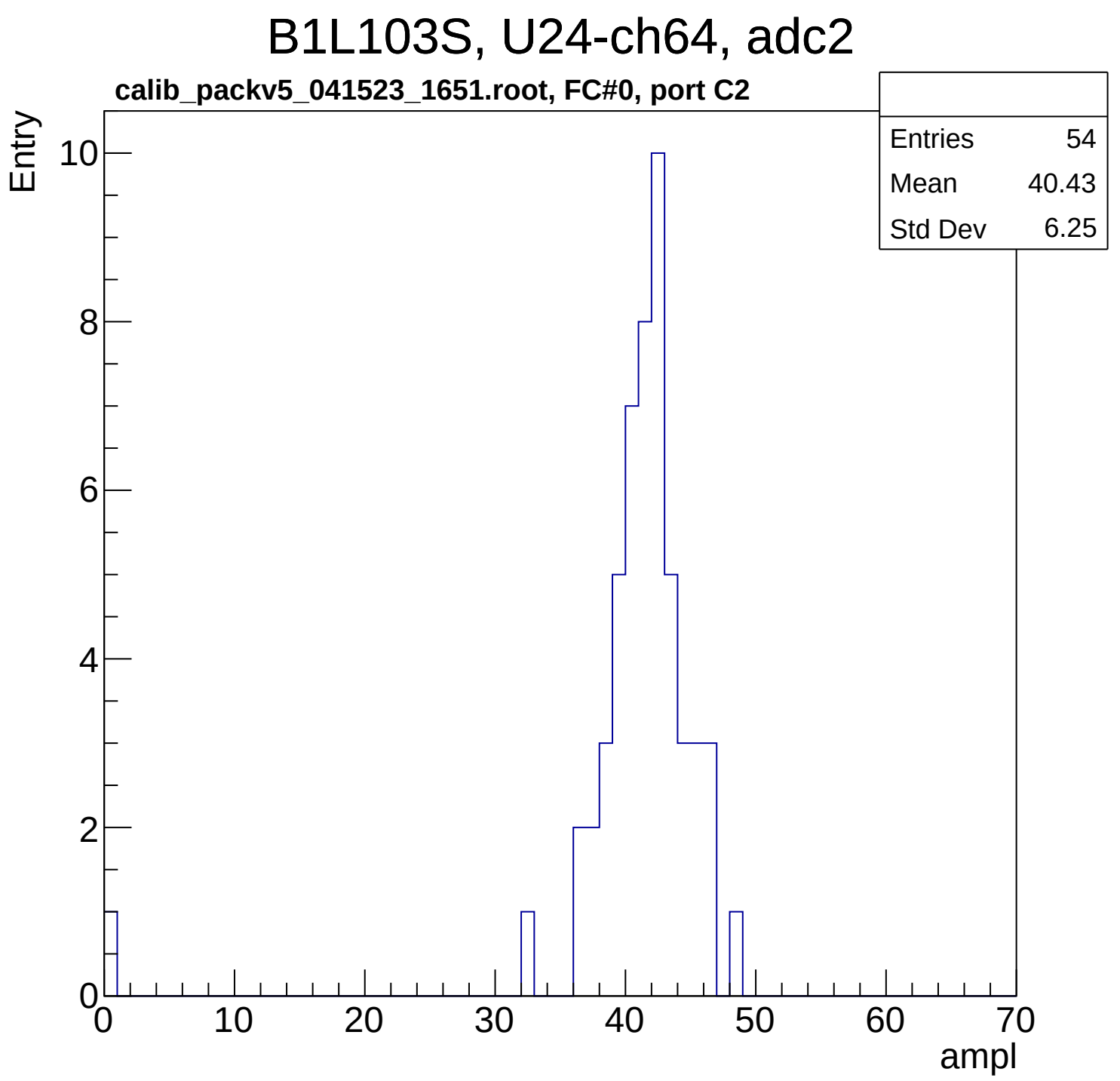
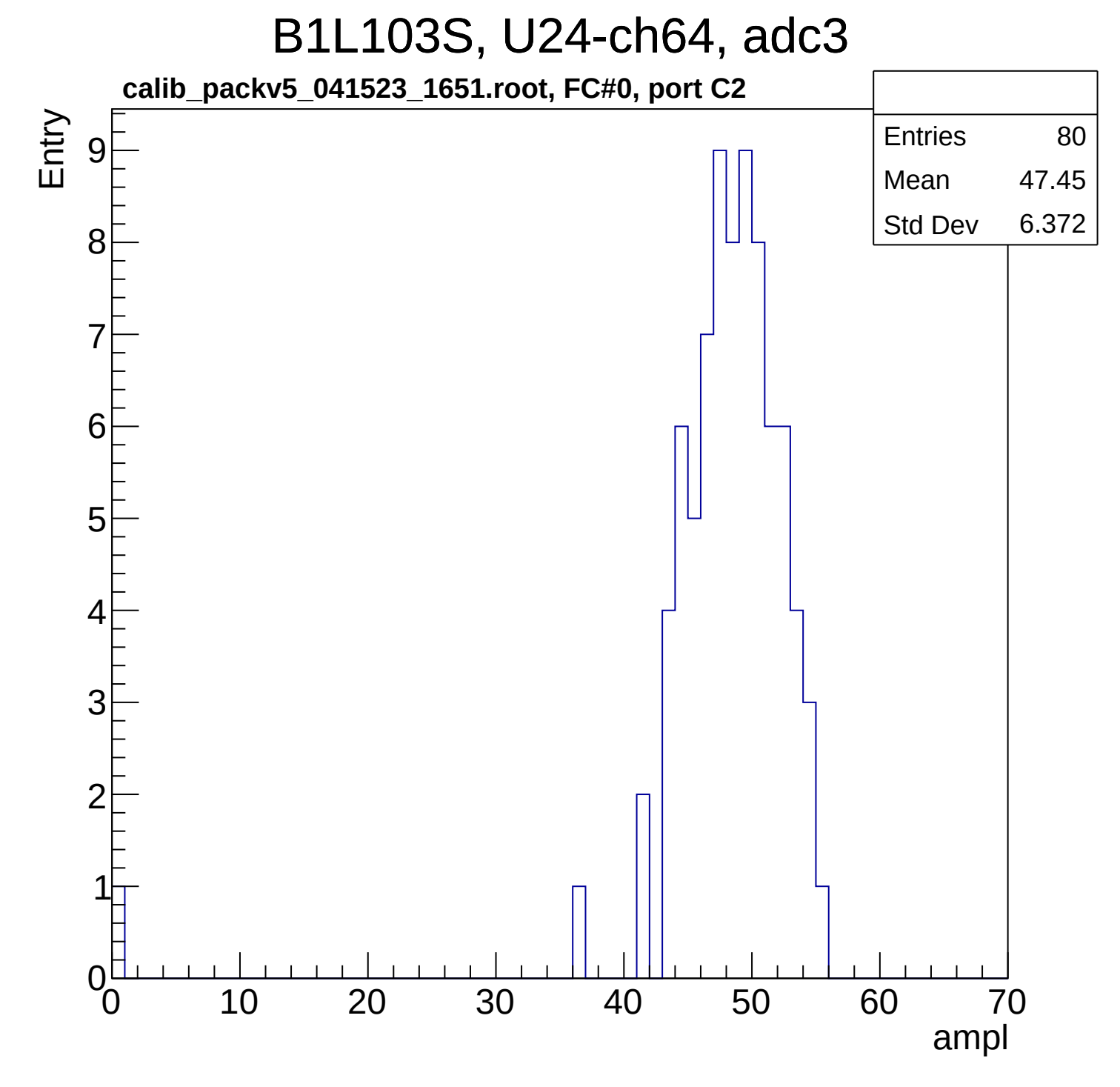
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch64, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 40.43
Std Dev 6.25
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch64, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 47.45
Std Dev 6.372
Entry
ampl
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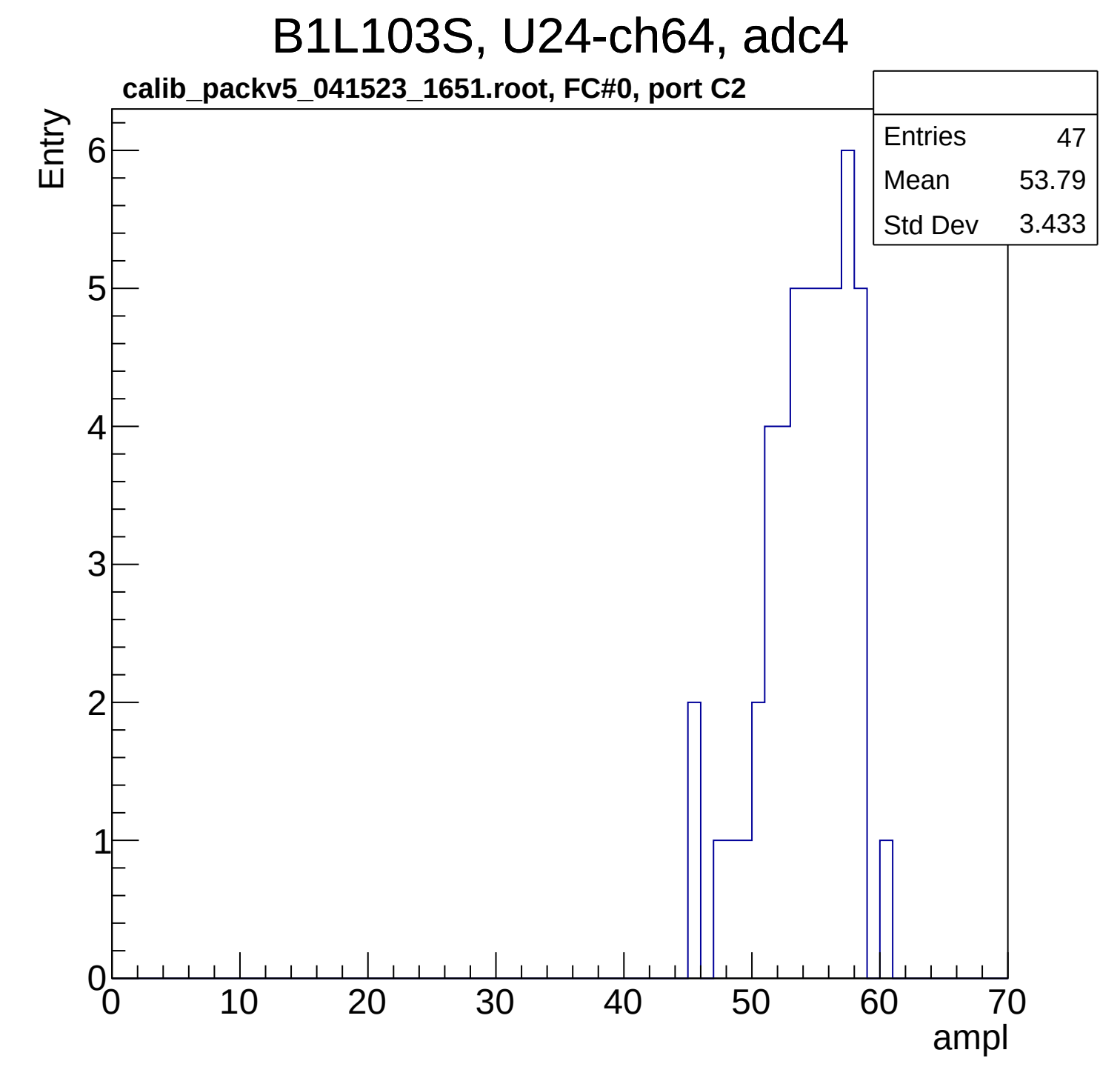
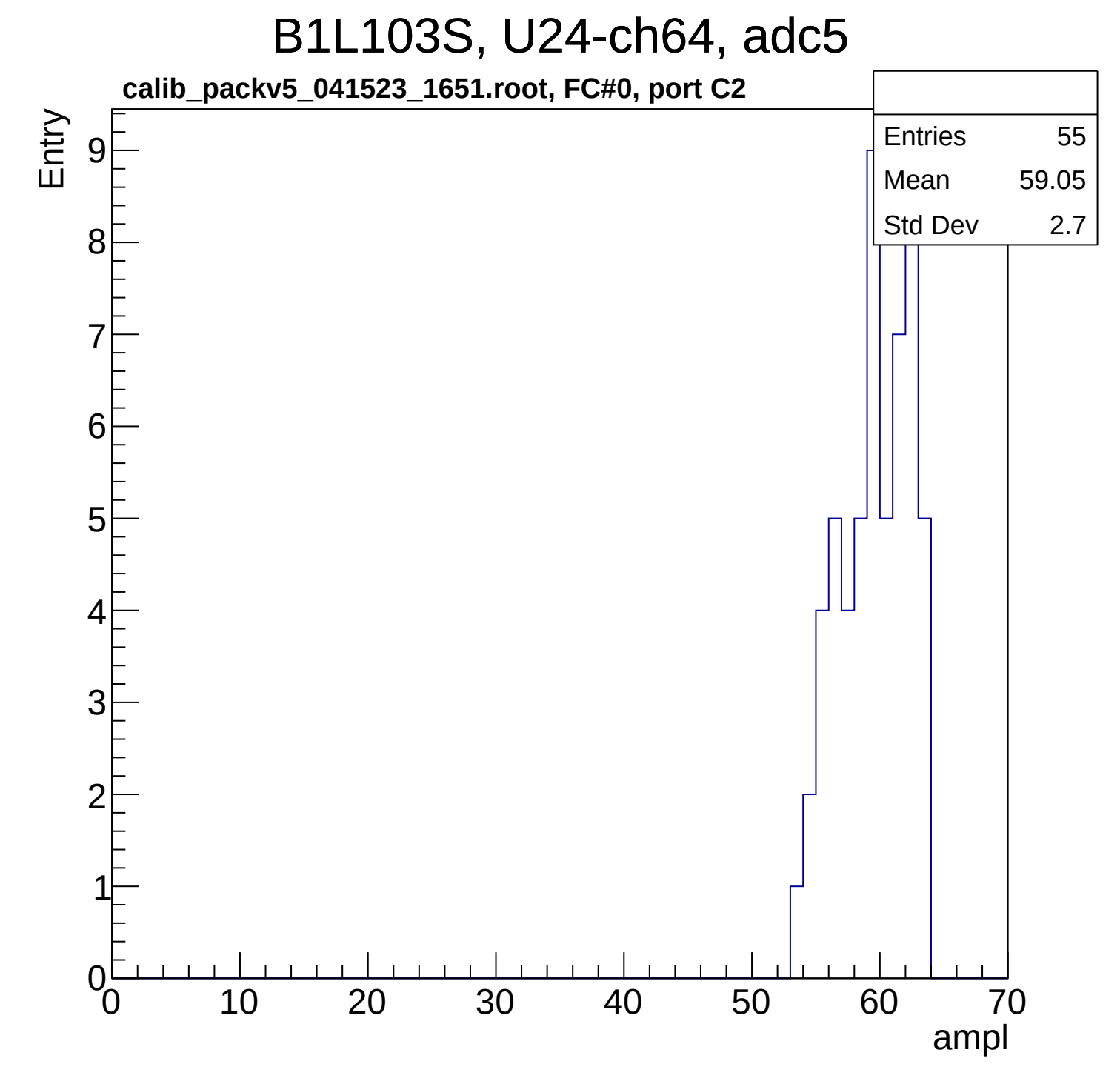
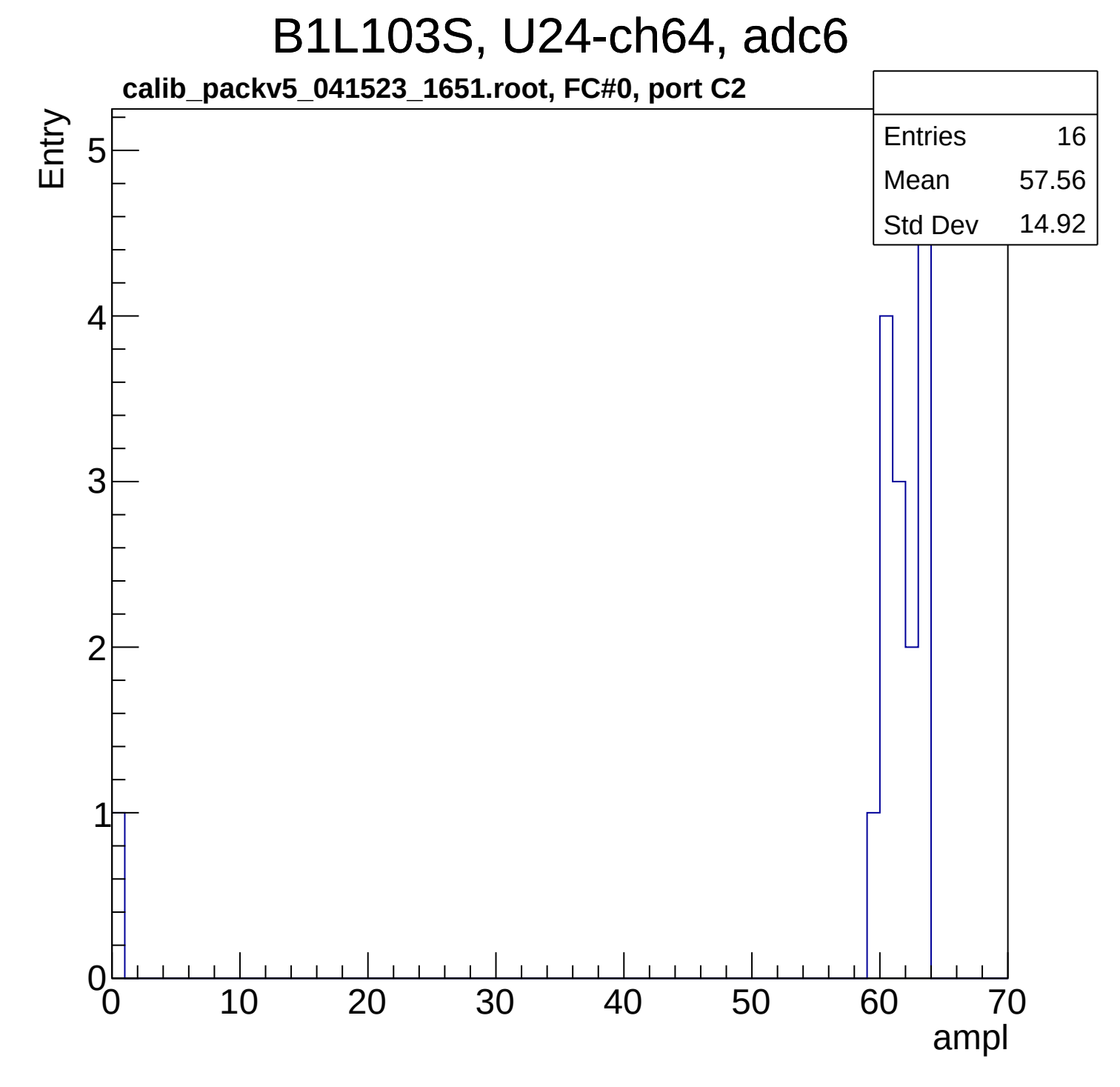
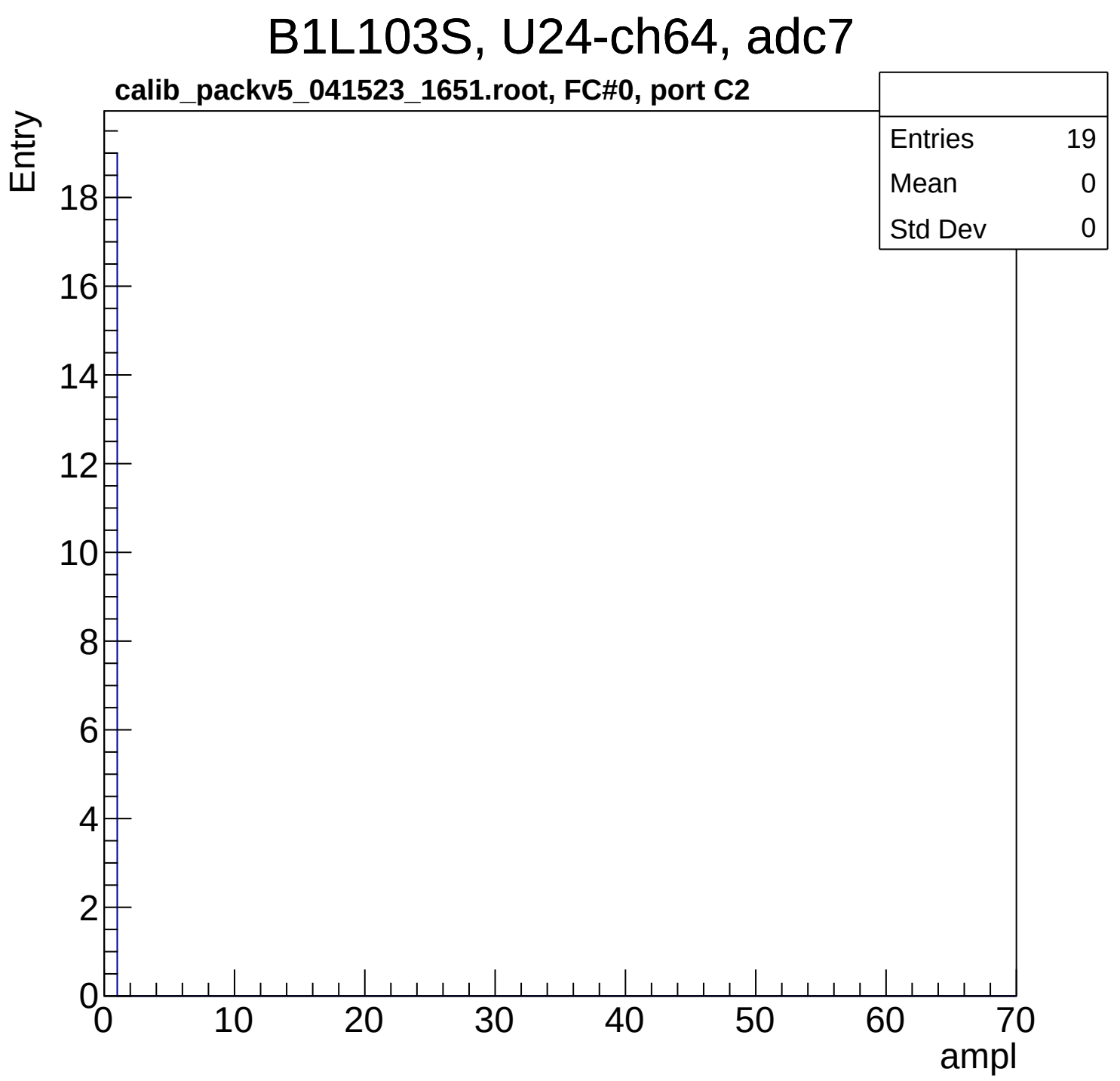
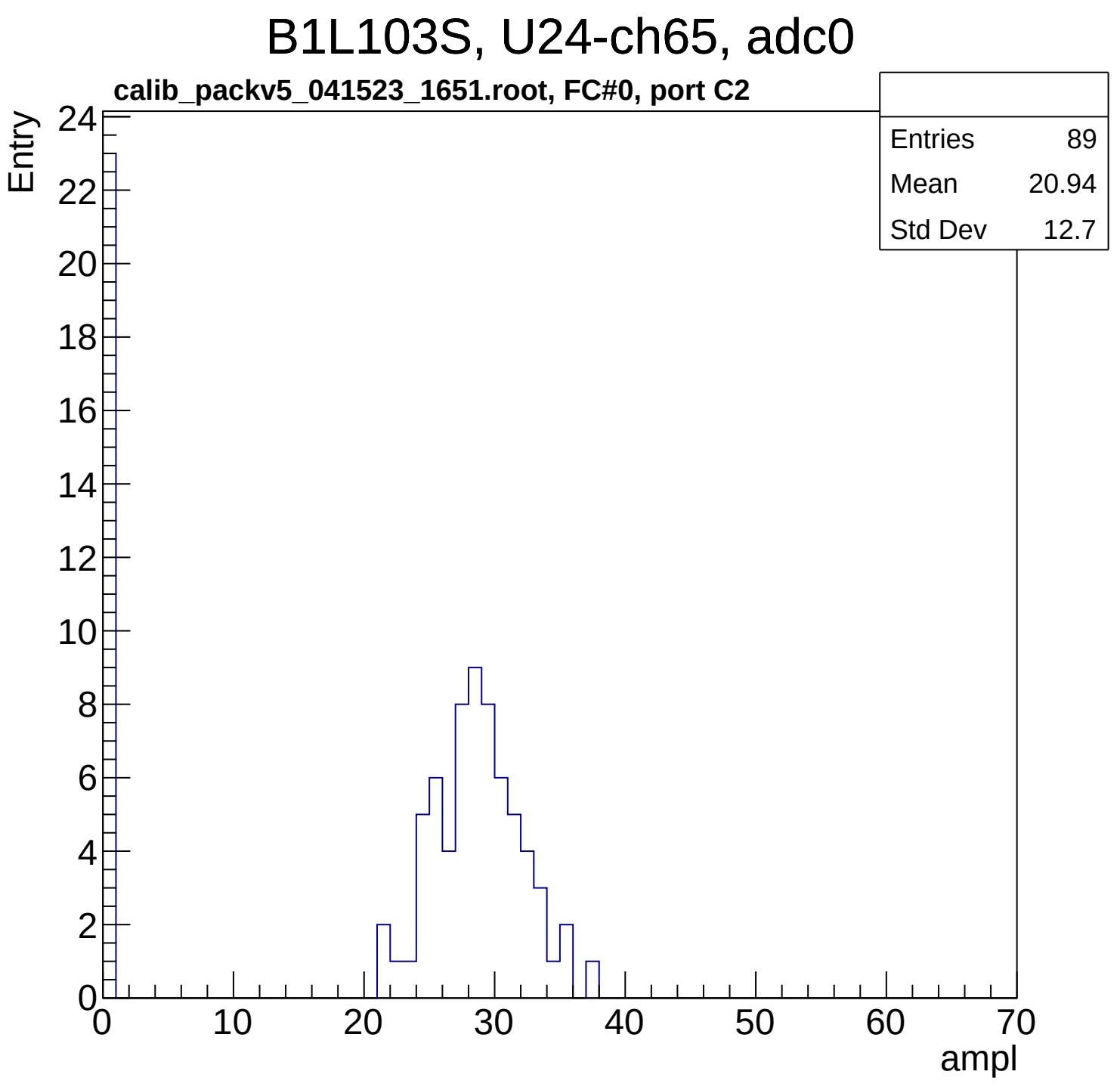
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U24-ch64, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 53.79
Std Dev 3.433
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U24-ch64, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 59.05
Std Dev 2.7
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U24-ch64, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 16
Mean 57.56
Std Dev 14.92
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch64, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch65, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 89
Mean 20.94
Std Dev 12.7
Entry
ampl
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2
4
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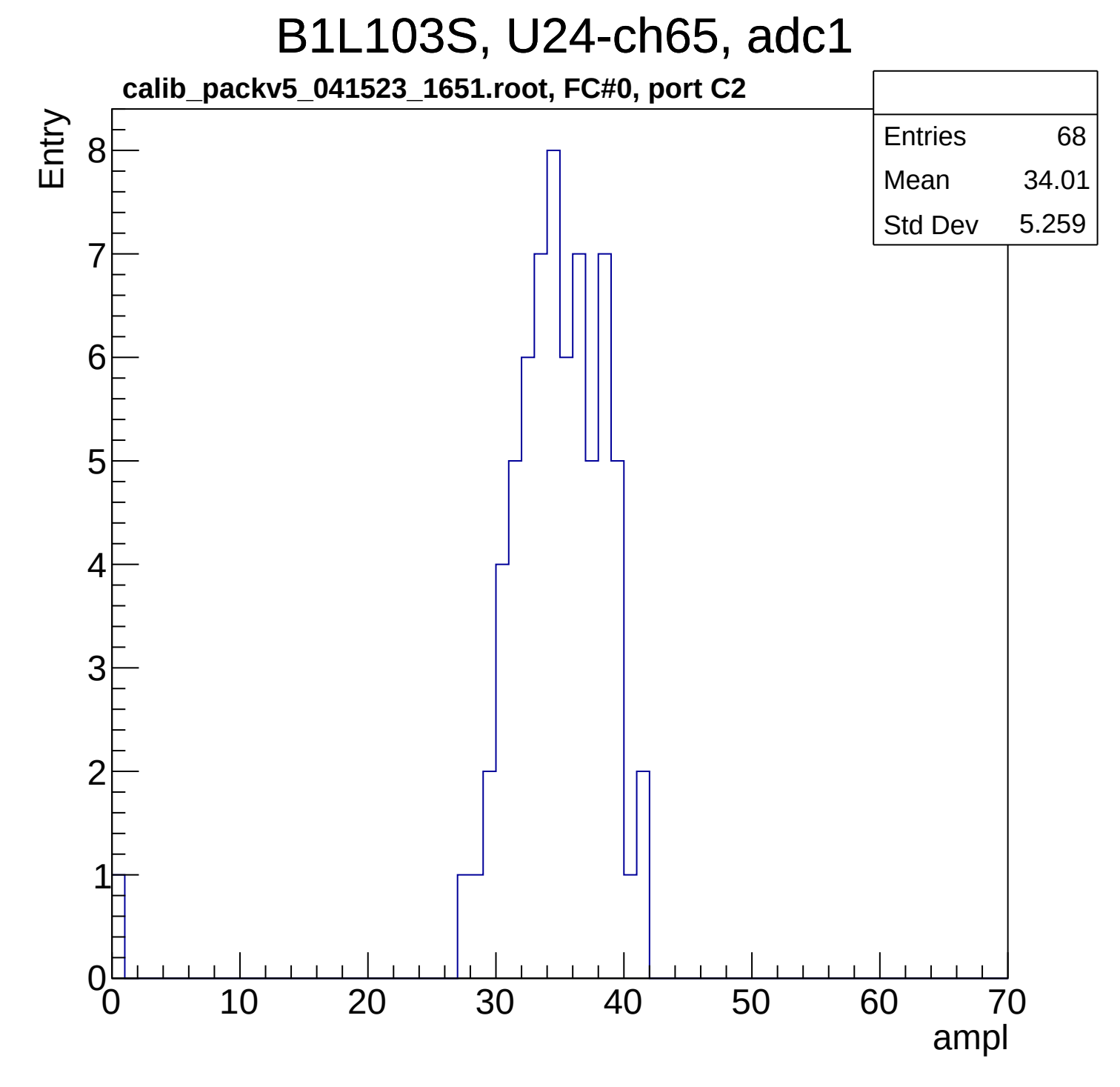
8
10
12
14
16
18
20
22
24
0
10
20
30
40
50
60
70


B1L103S, U24-ch65, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 34.01
Std Dev 5.259
Entry
ampl
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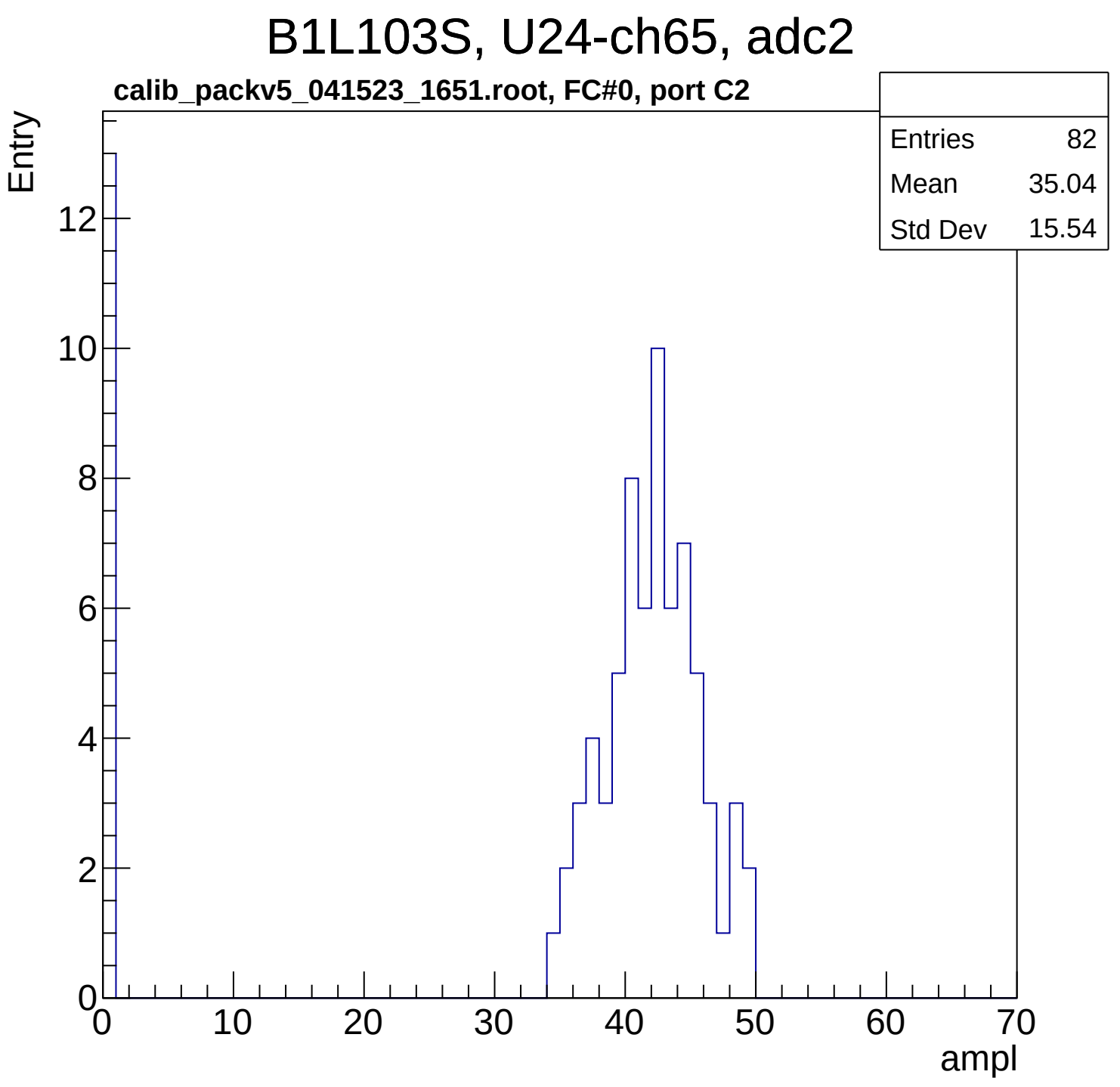
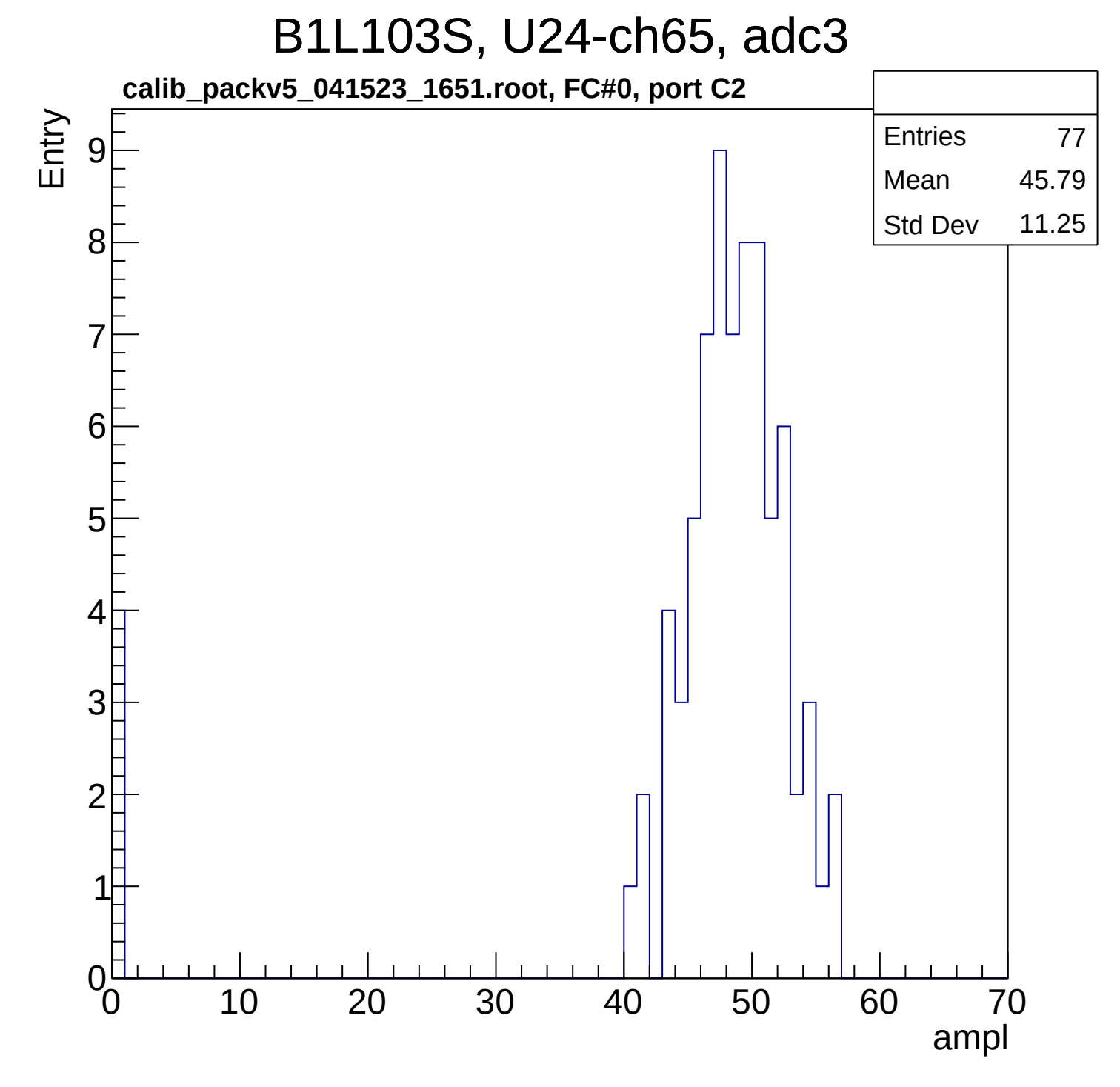
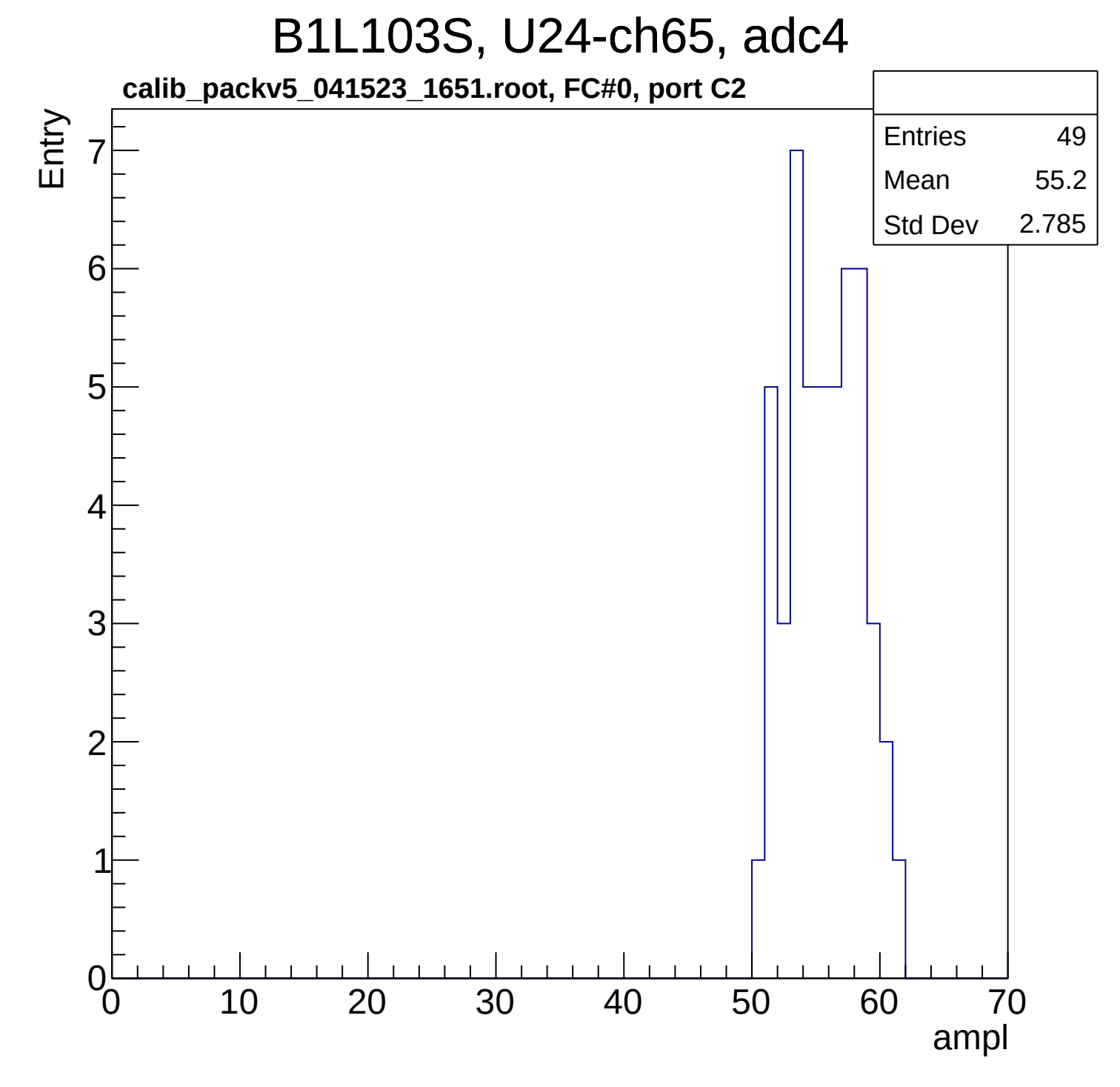
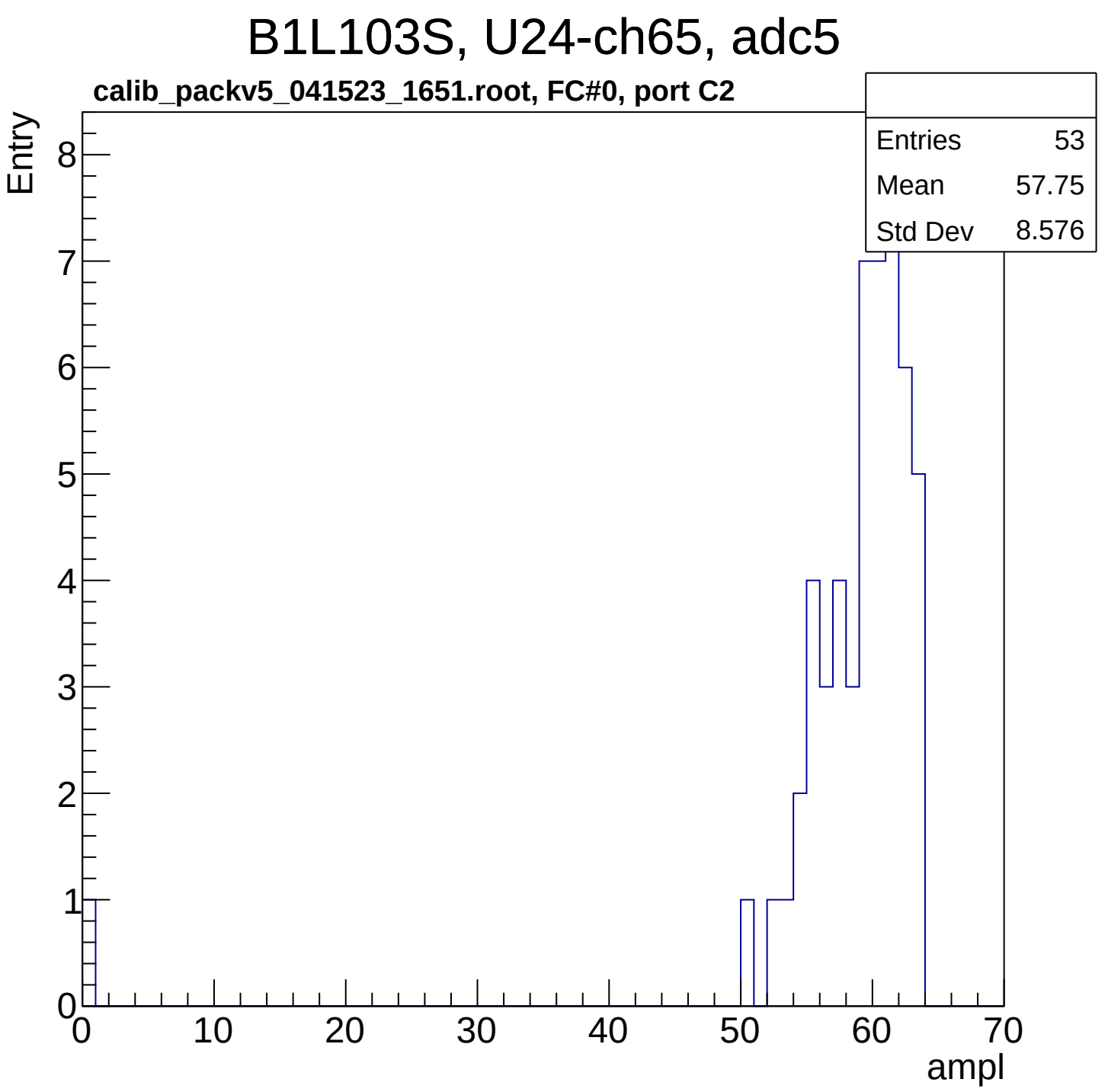
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U24-ch65, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 35.04
Std Dev 15.54
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch65, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 45.79
Std Dev 11.25
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U24-ch65, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 55.2
Std Dev 2.785
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U24-ch65, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 57.75
Std Dev 8.576
Entry
ampl
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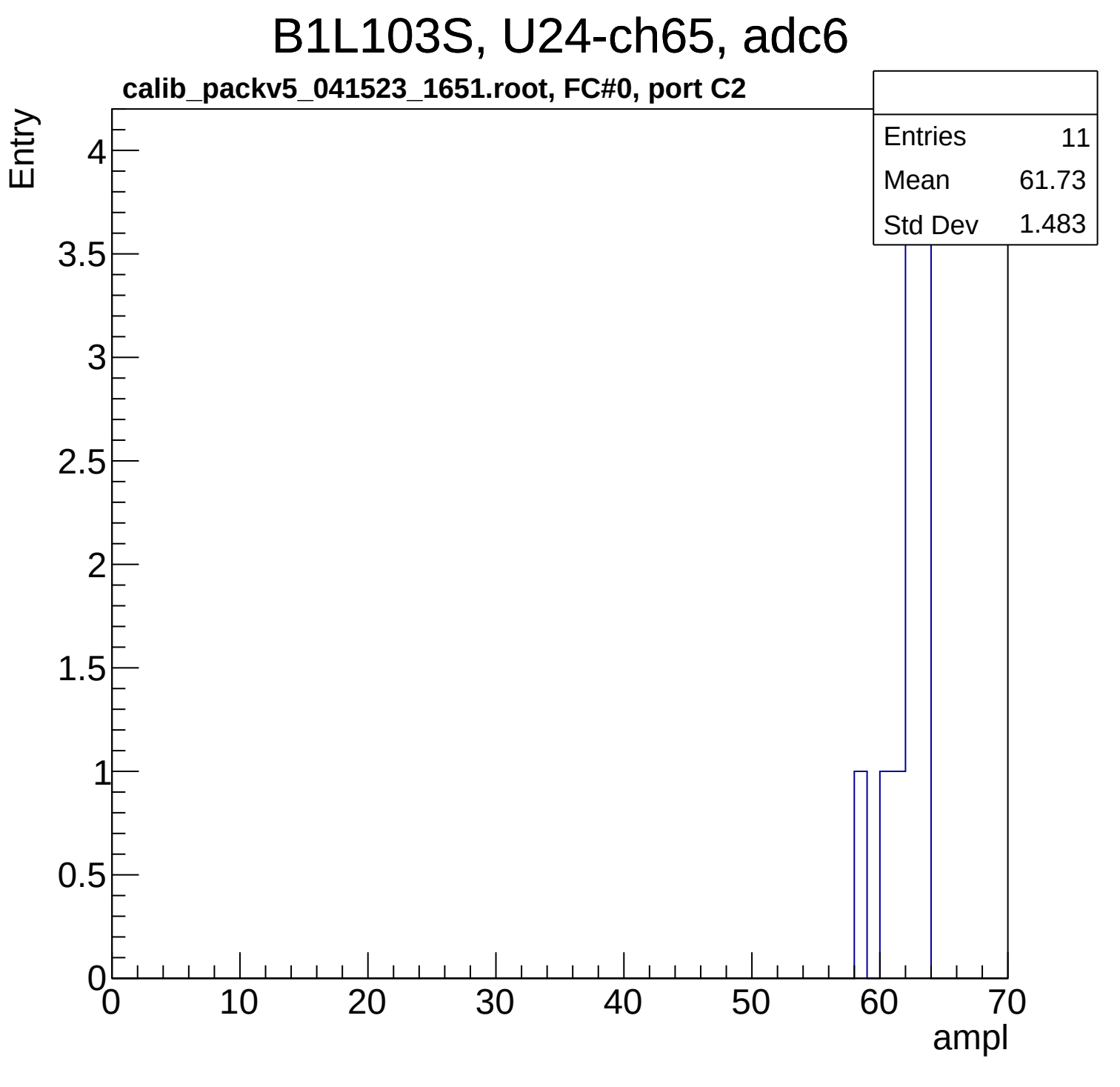
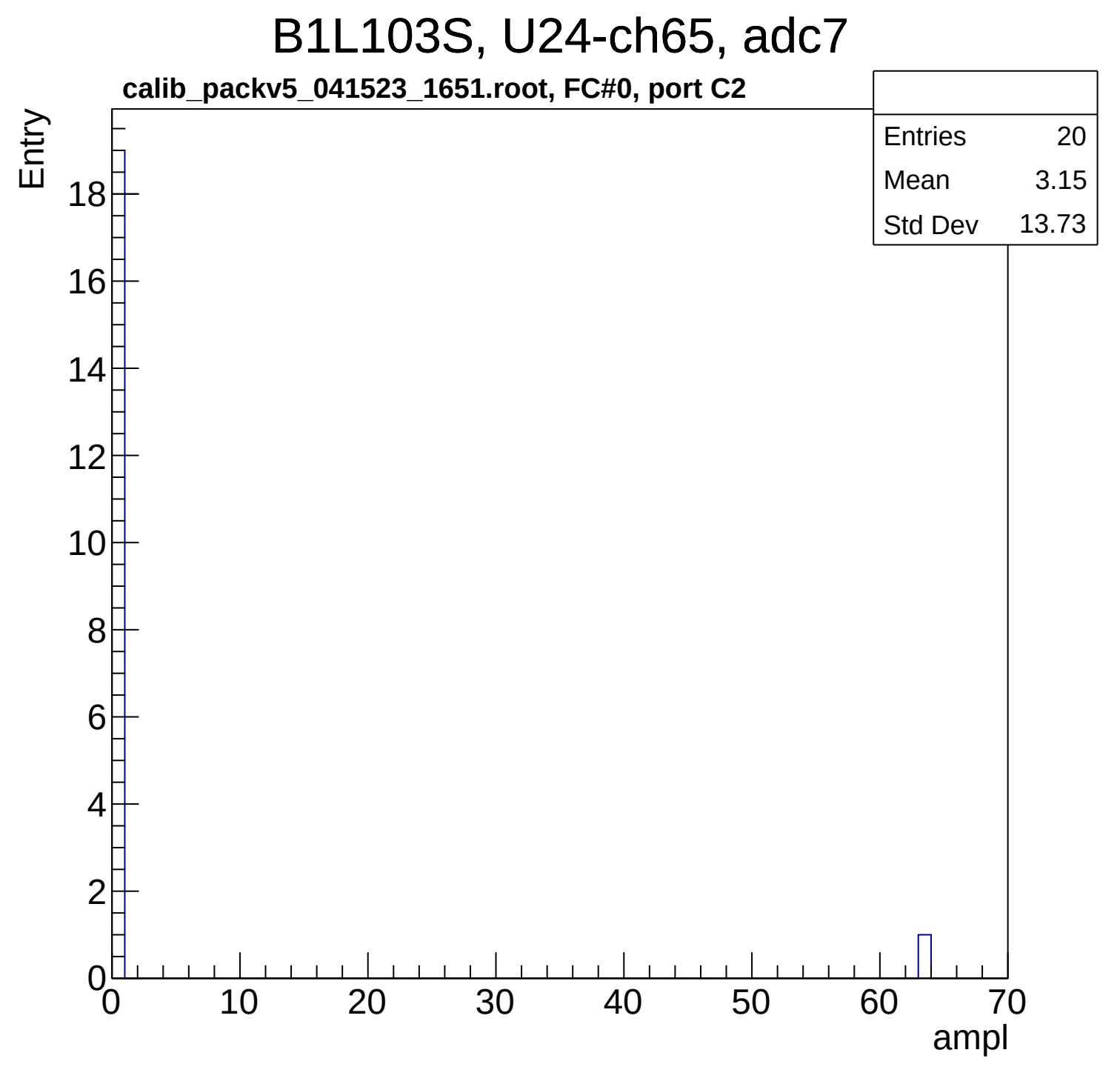
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U24-ch65, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 61.73
Std Dev 1.483
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U24-ch65, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
0
2
4
6
8
10
12
14
16
18
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10
20
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50
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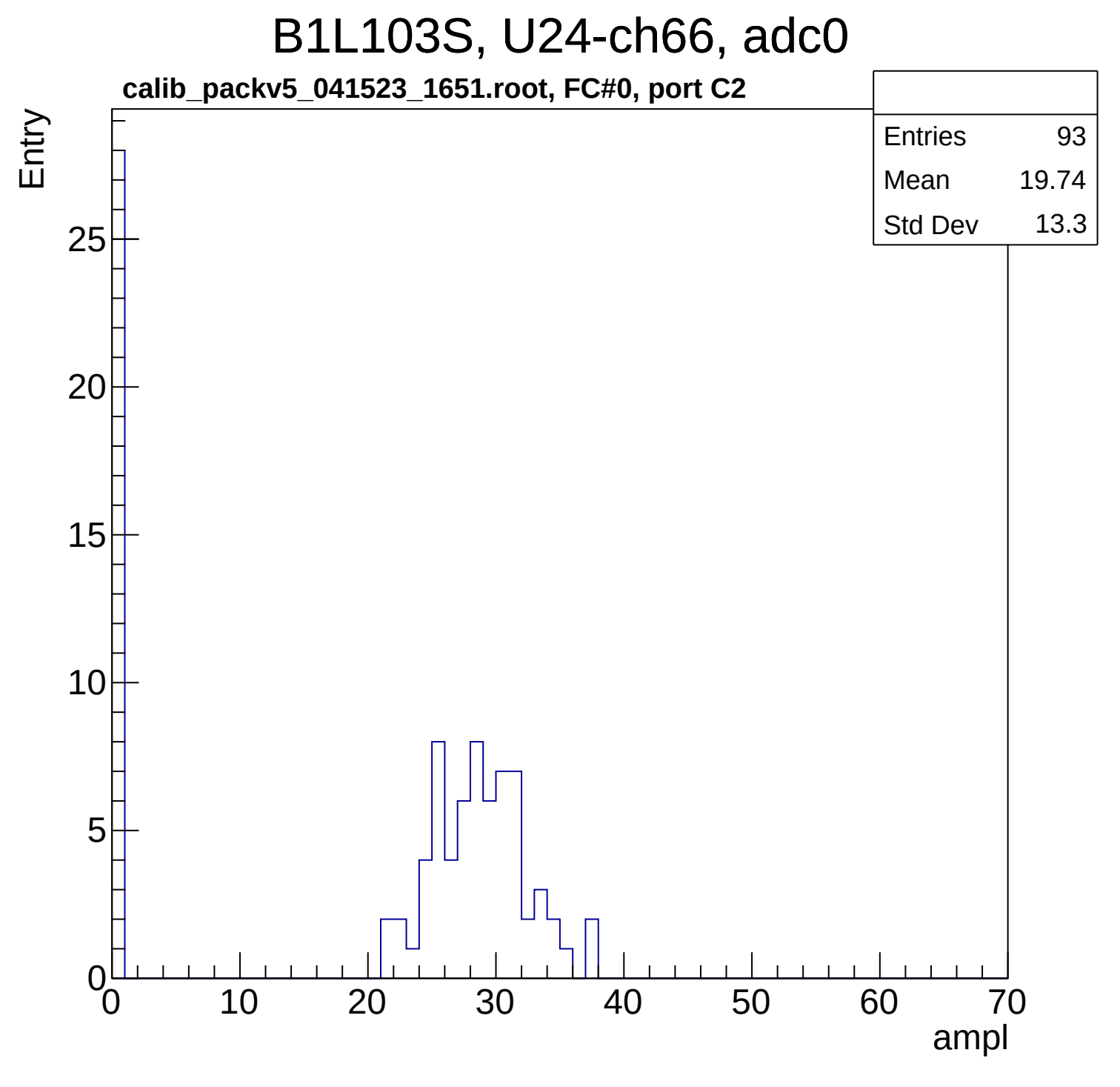
70
ampl


B1L103S, U24-ch66, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 93
Mean 19.74
Std Dev 13.3
Entry
0
5
10
15
20
25
0
10
20
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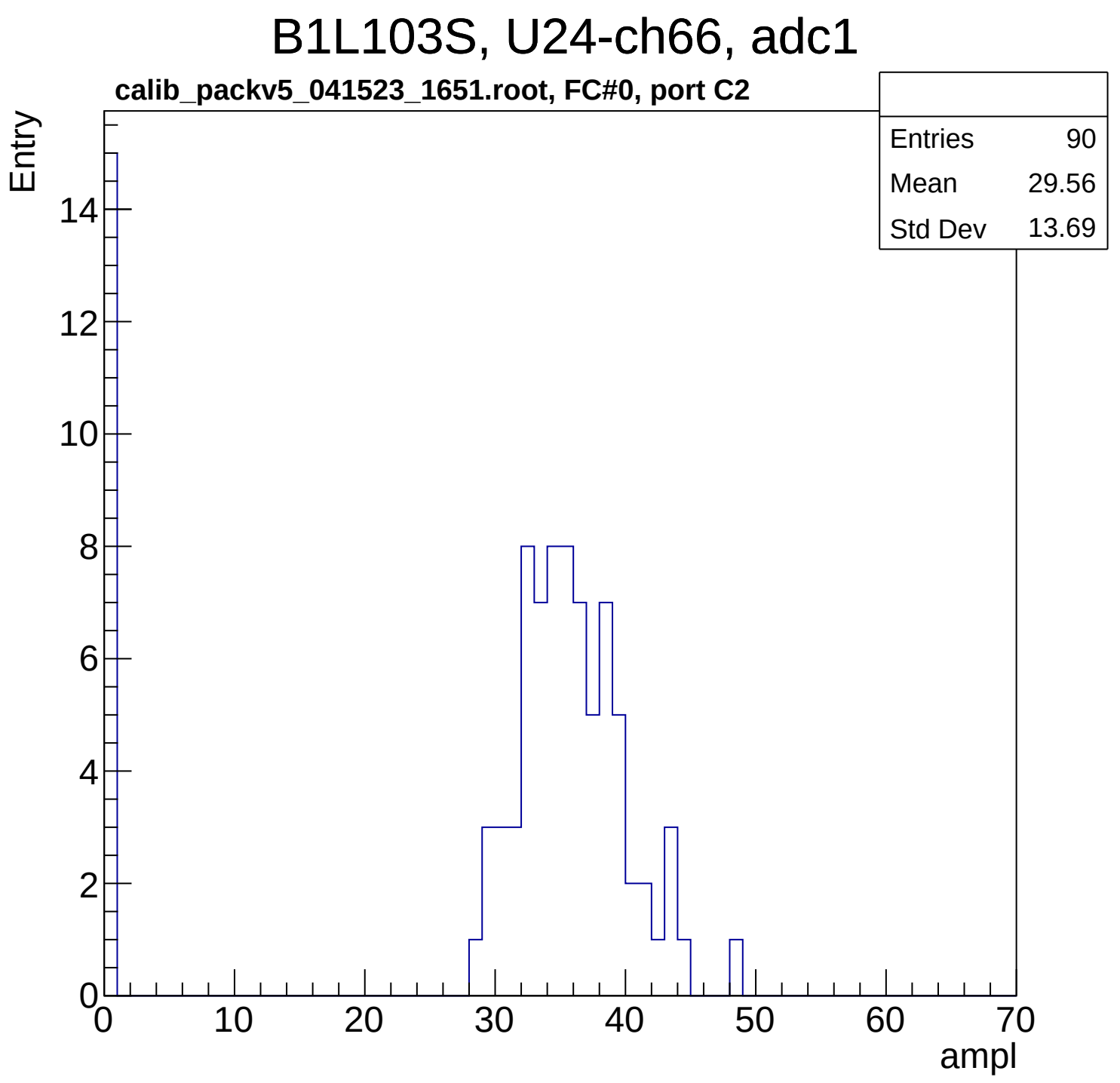
40
50
60
70
ampl


B1L103S, U24-ch66, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 90
Mean 29.56
Std Dev 13.69
Entry
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4
6
8
10
12
14
0
10
20
30
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50
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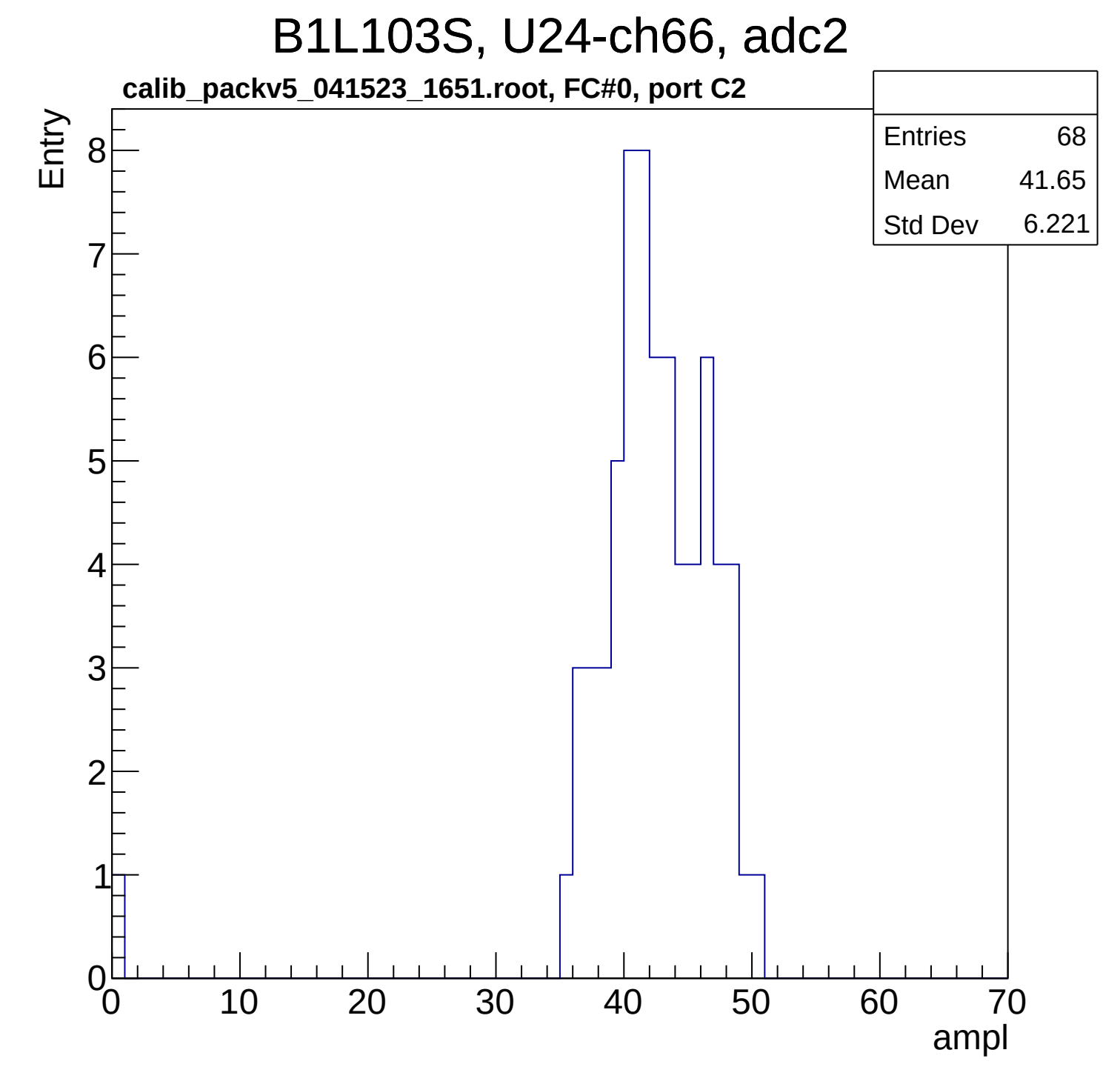
70
ampl


B1L103S, U24-ch66, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 41.65
Std Dev 6.221
Entry
ampl
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2
3
4
5
6
7
8
0
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40
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60
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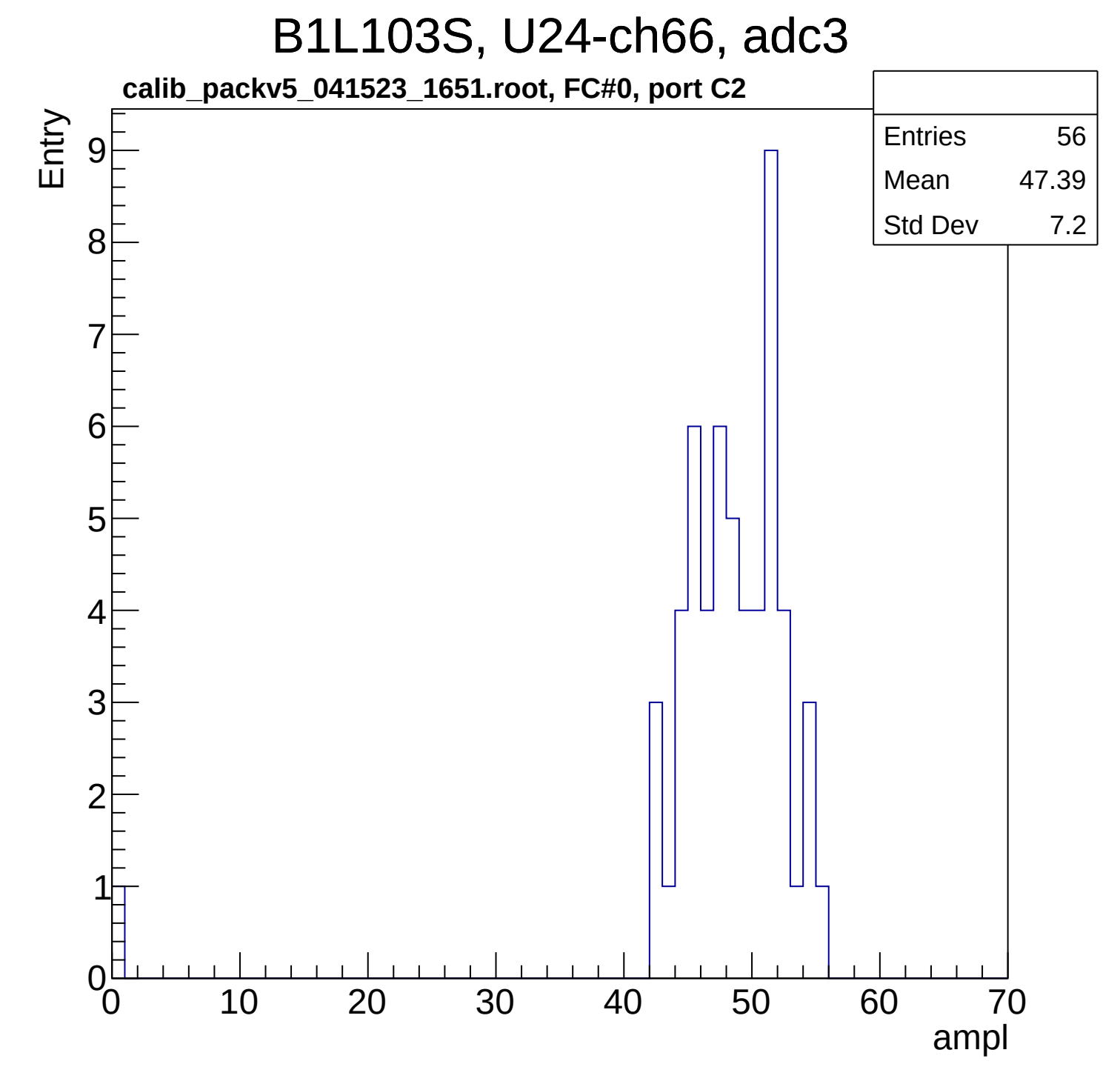
B1L103S, U24-ch66, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 47.39
Std Dev 7.2
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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60
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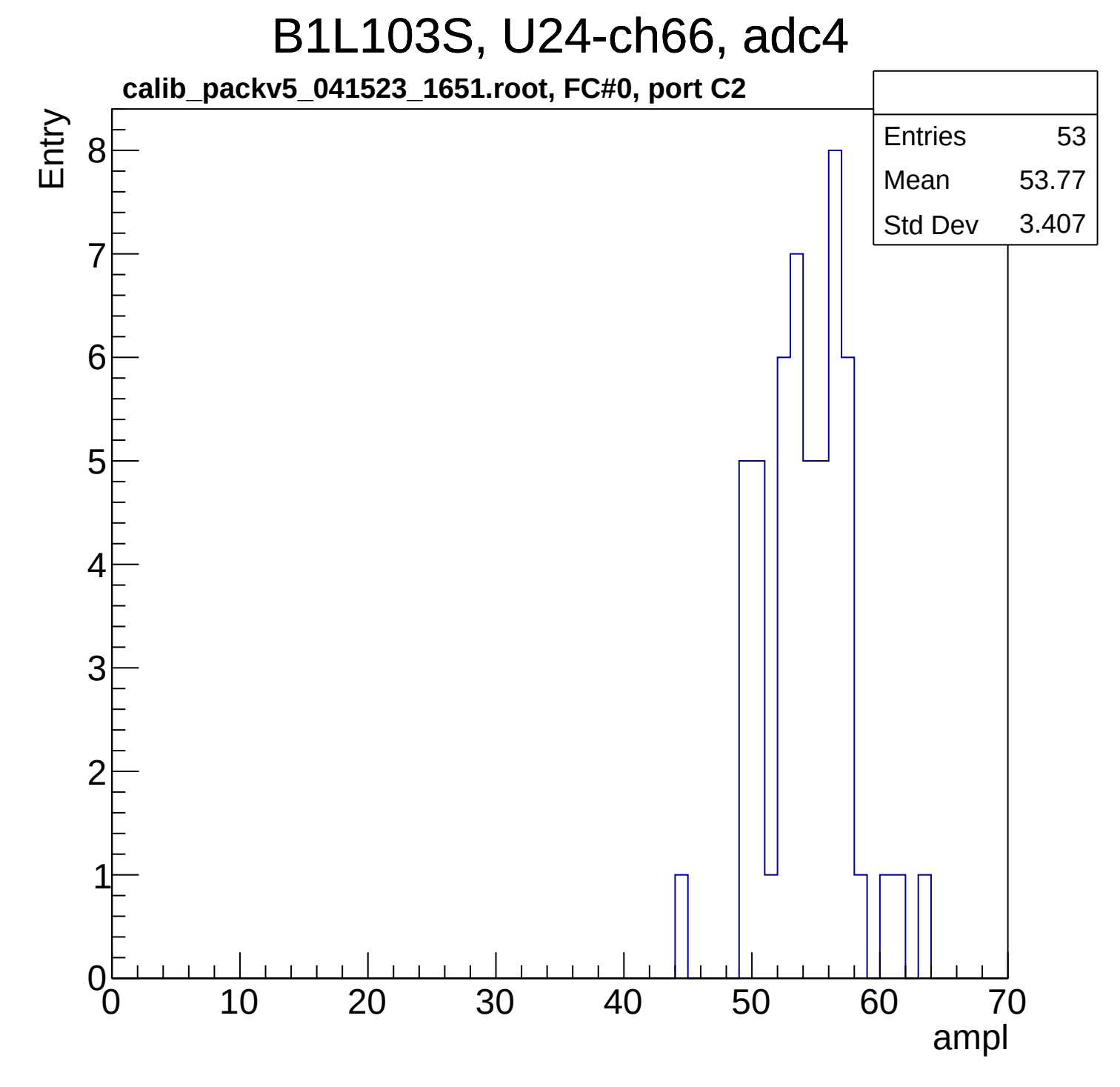
B1L103S, U24-ch66, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 53.77
Std Dev 3.407
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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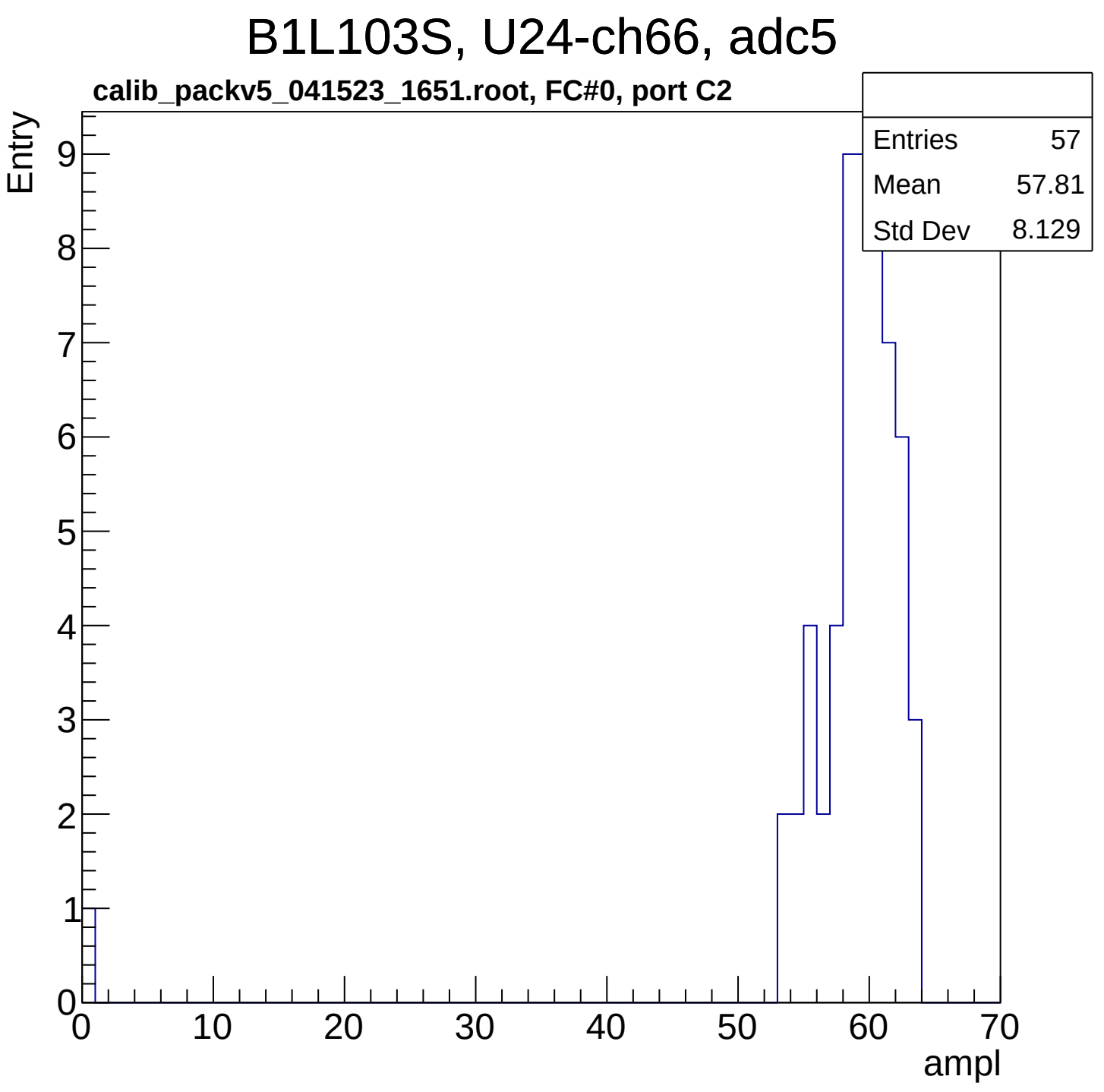
B1L103S, U24-ch66, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 57.81
Std Dev 8.129
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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60
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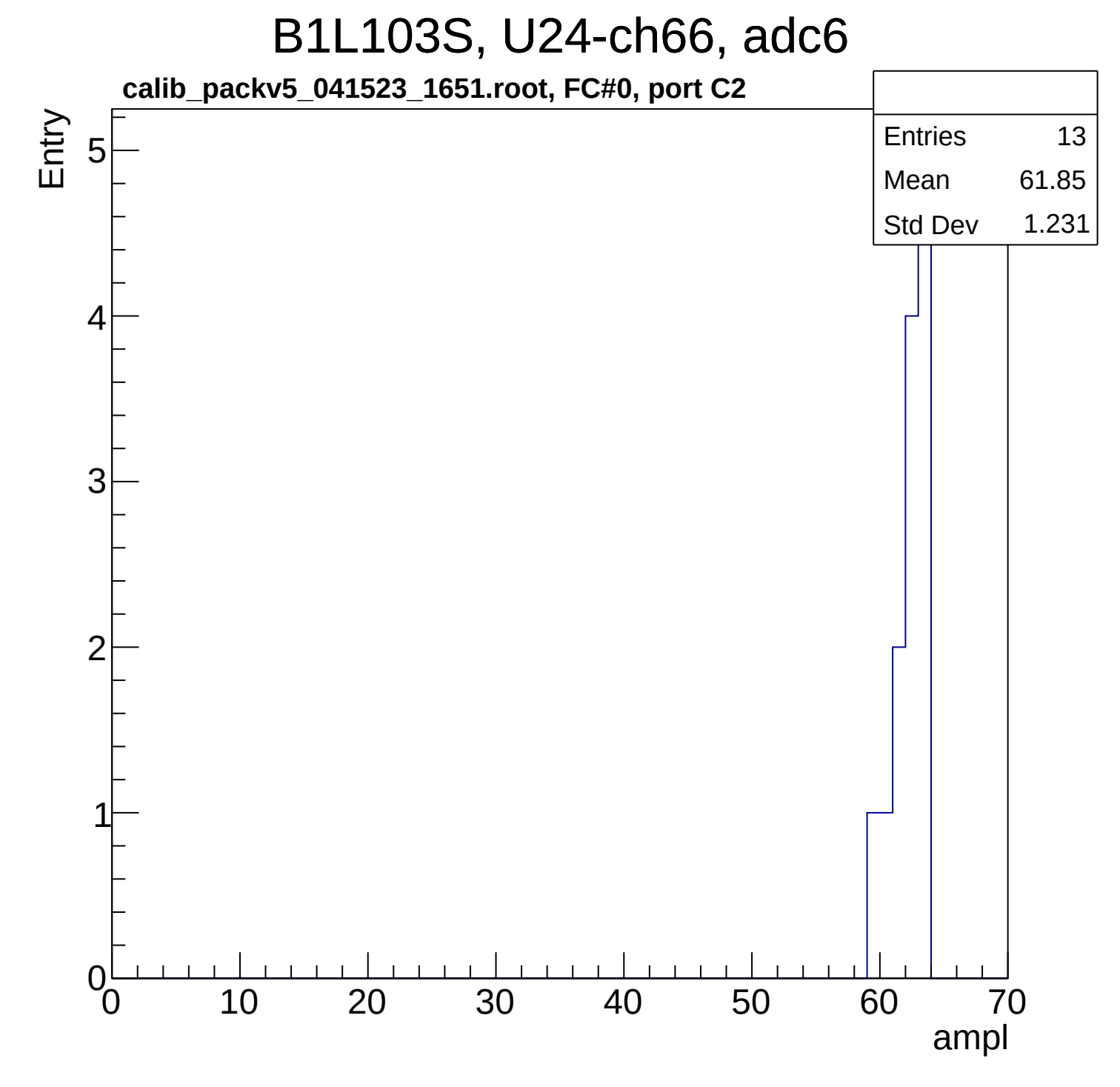
B1L103S, U24-ch66, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 13
Mean 61.85
Std Dev 1.231
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
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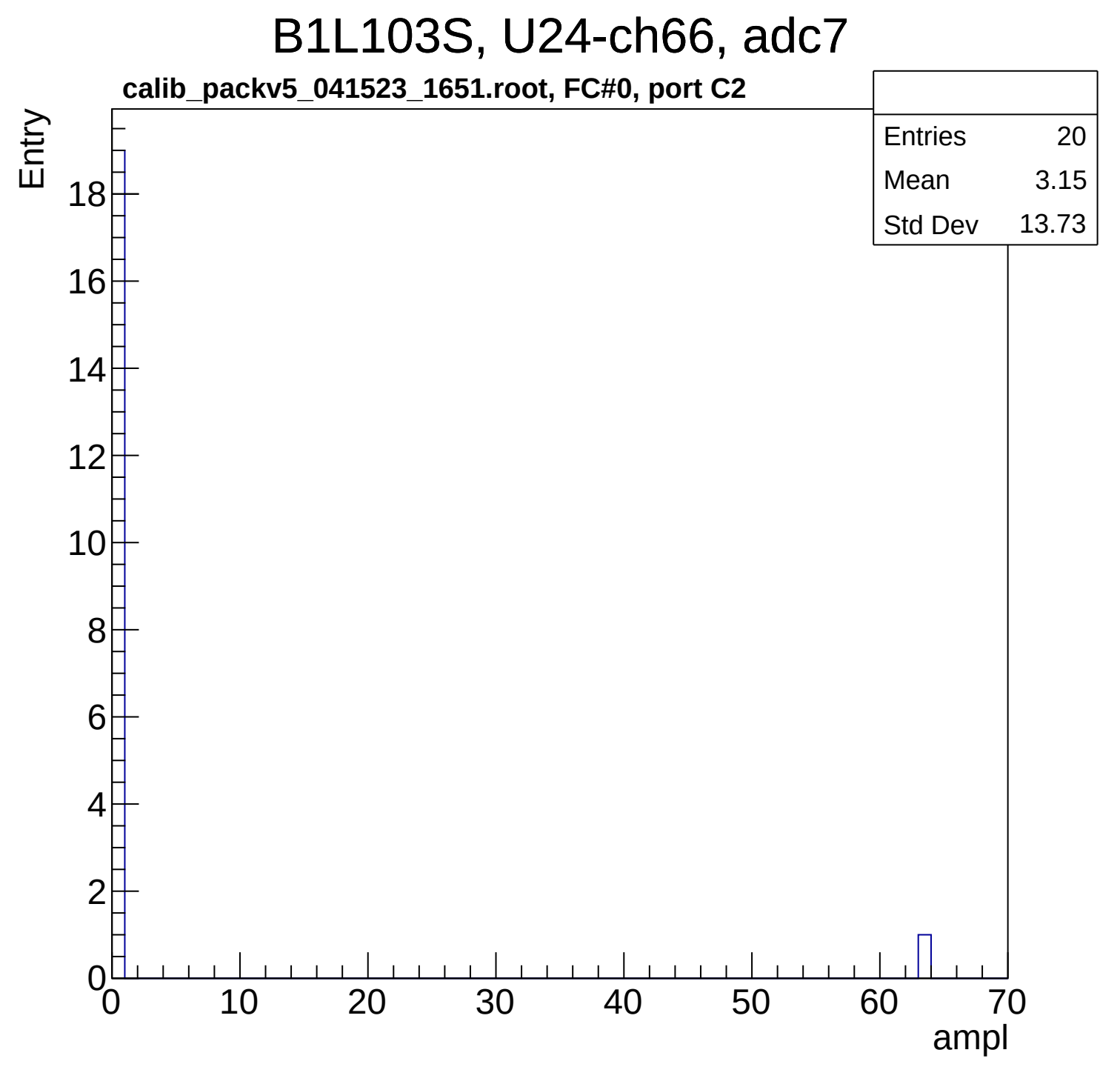
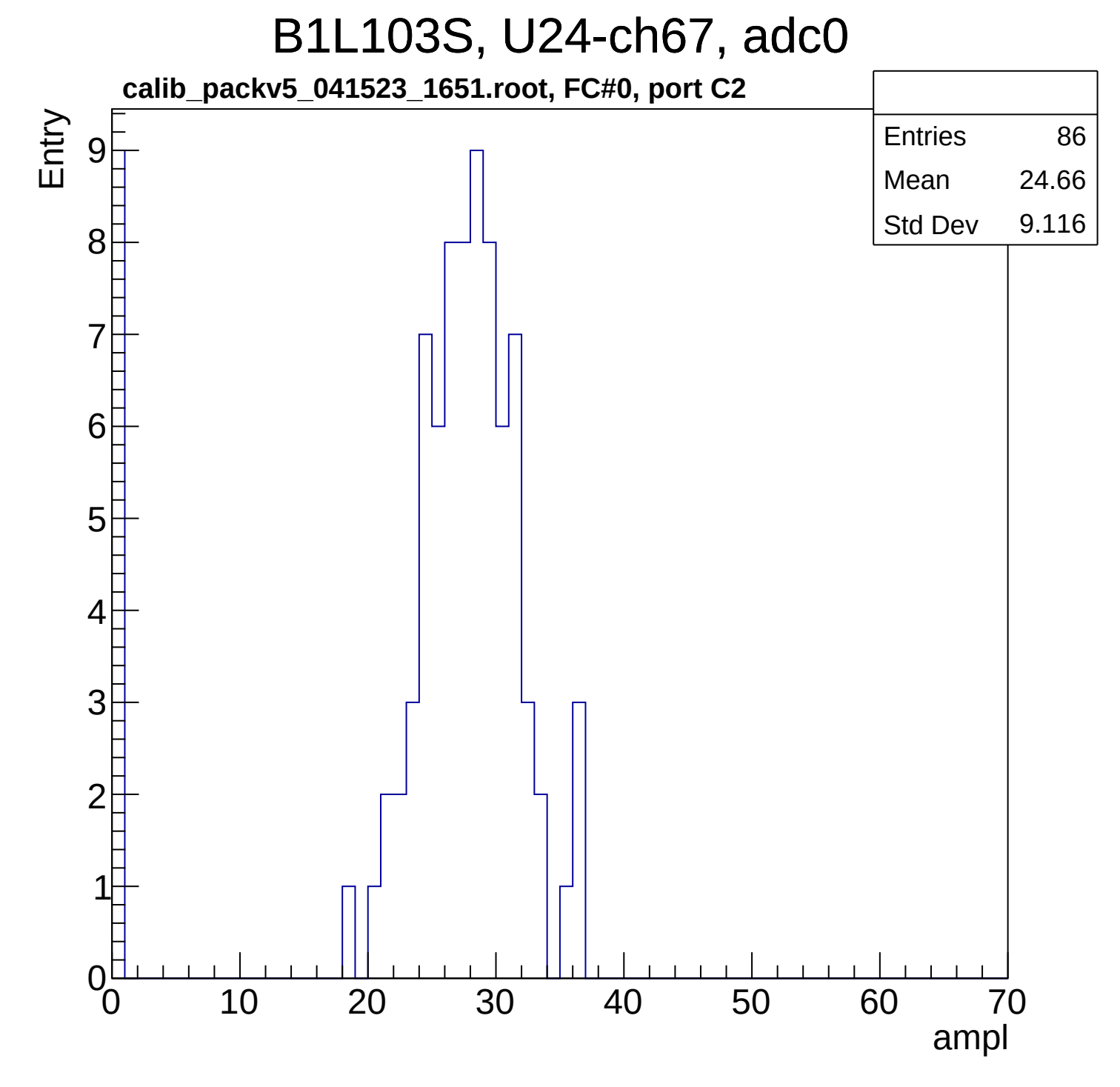

B1L103S, U24-ch66, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch67, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 24.66
Std Dev 9.116
Entry
ampl
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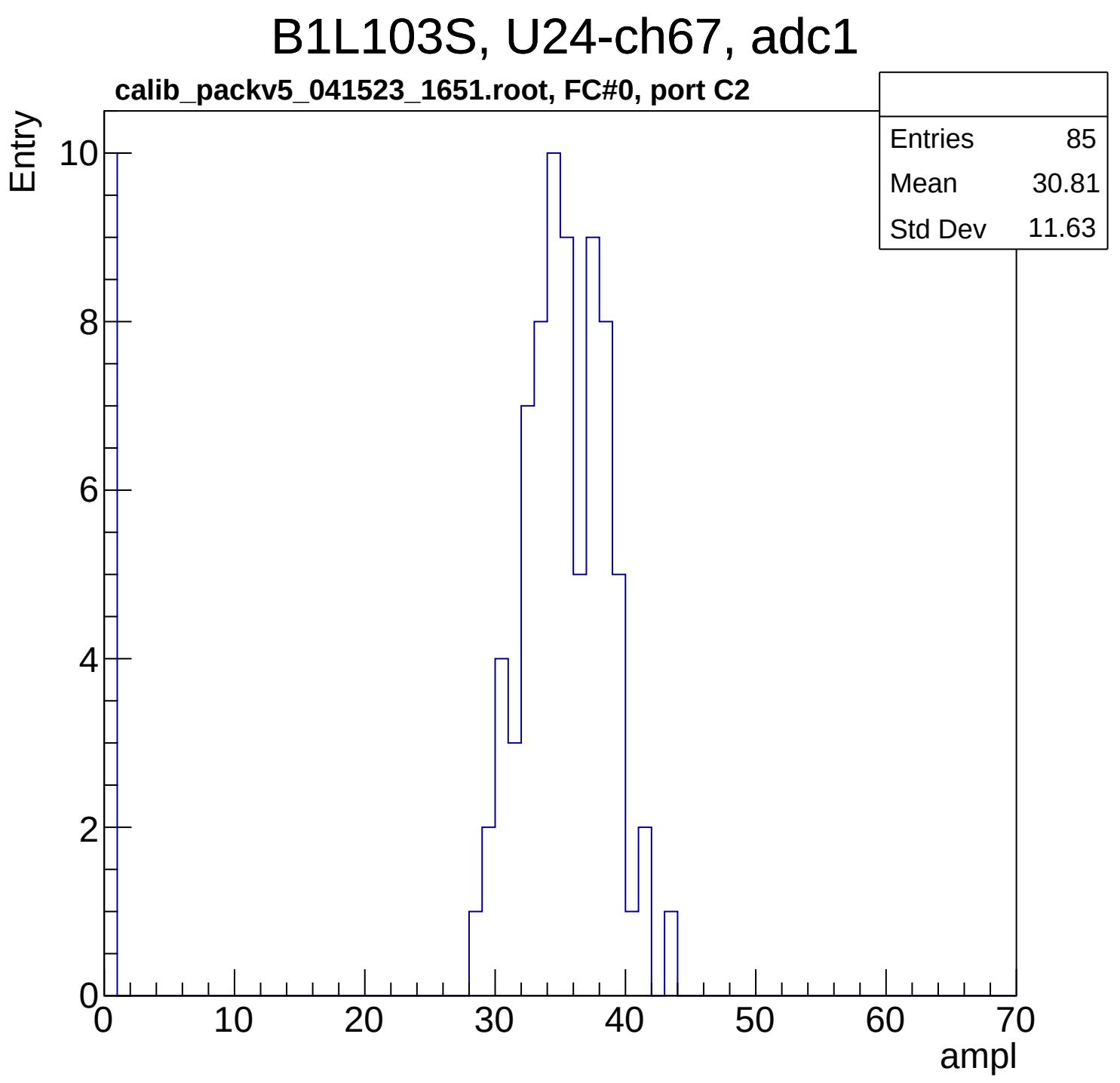
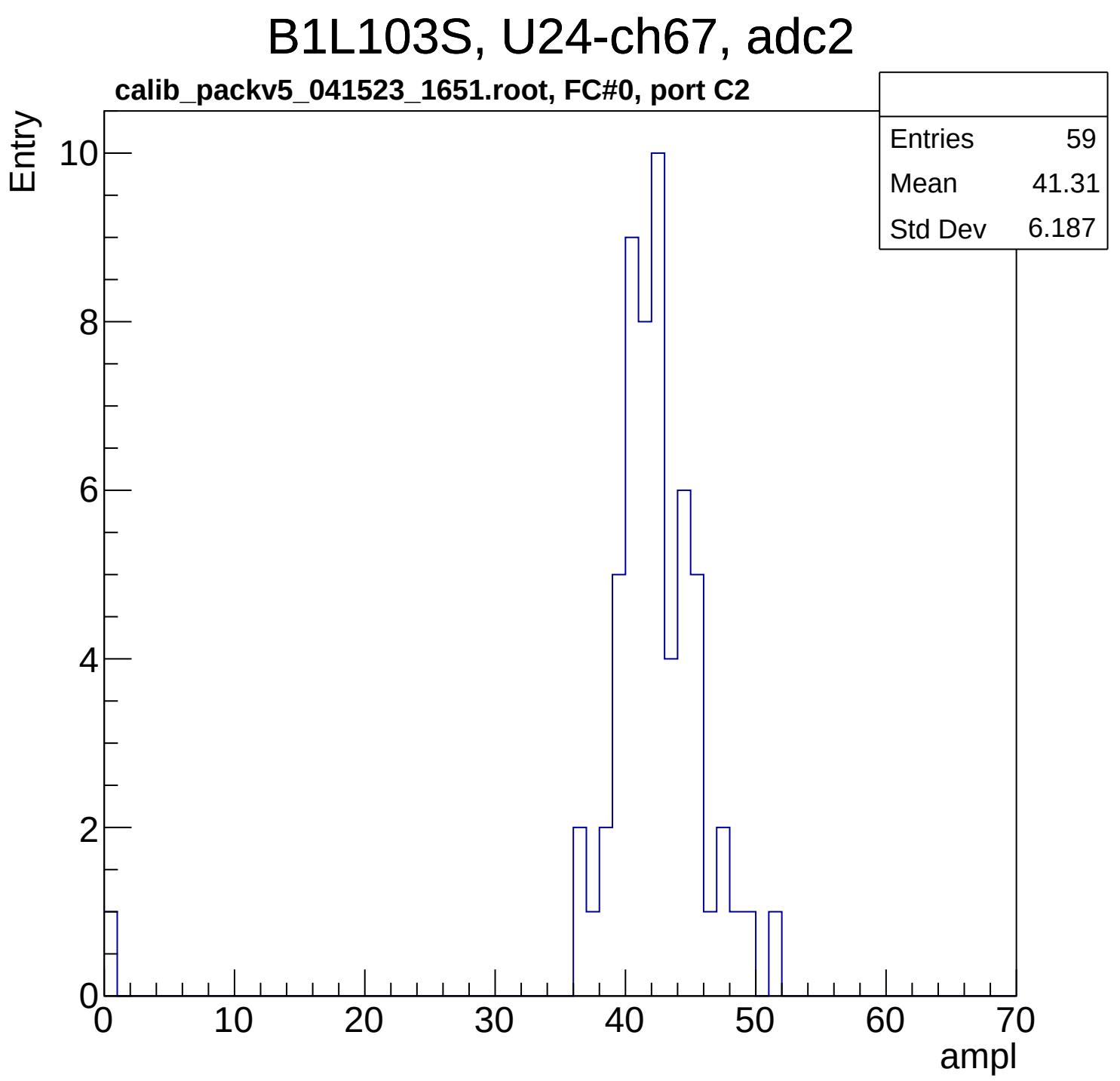
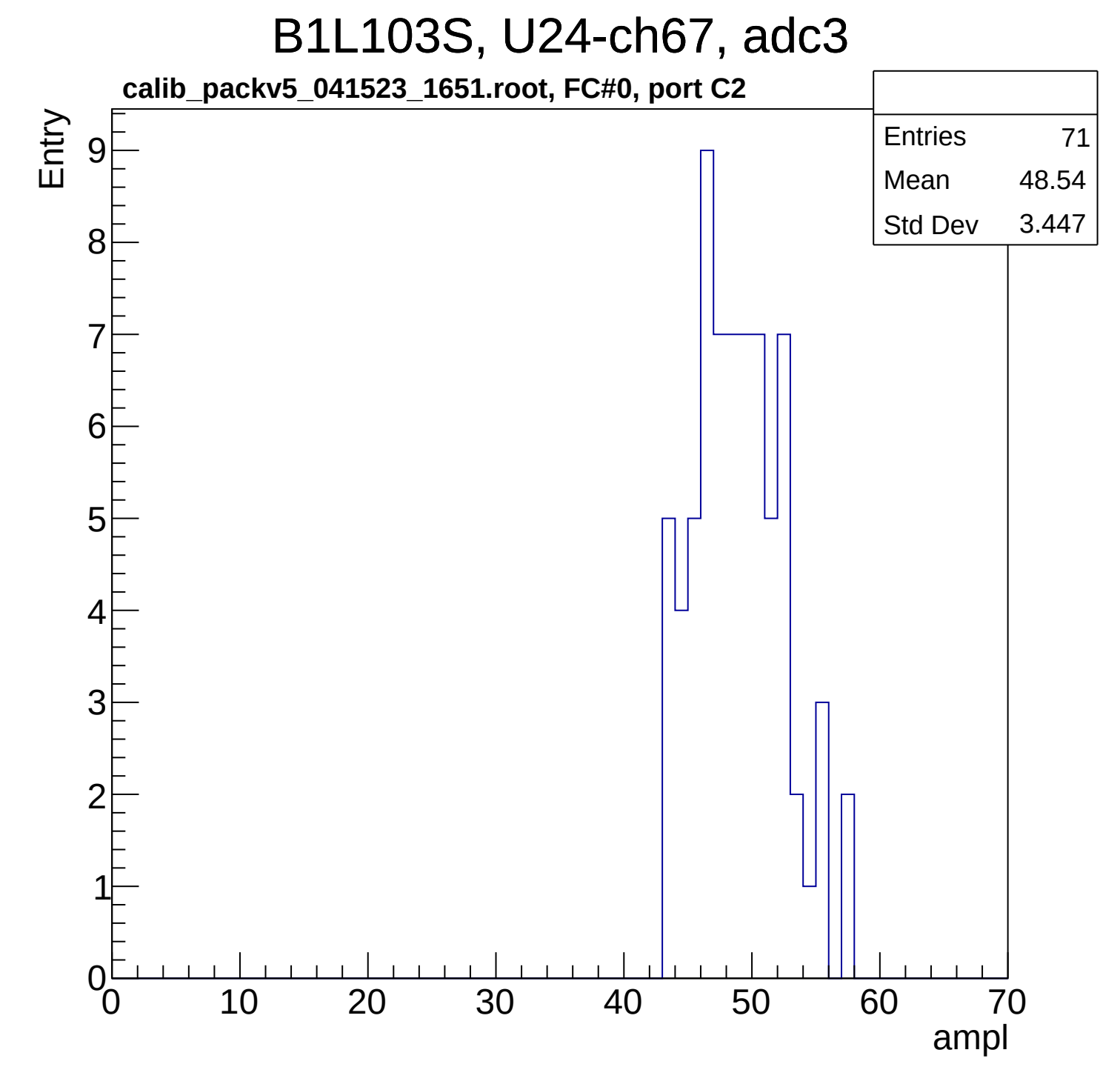
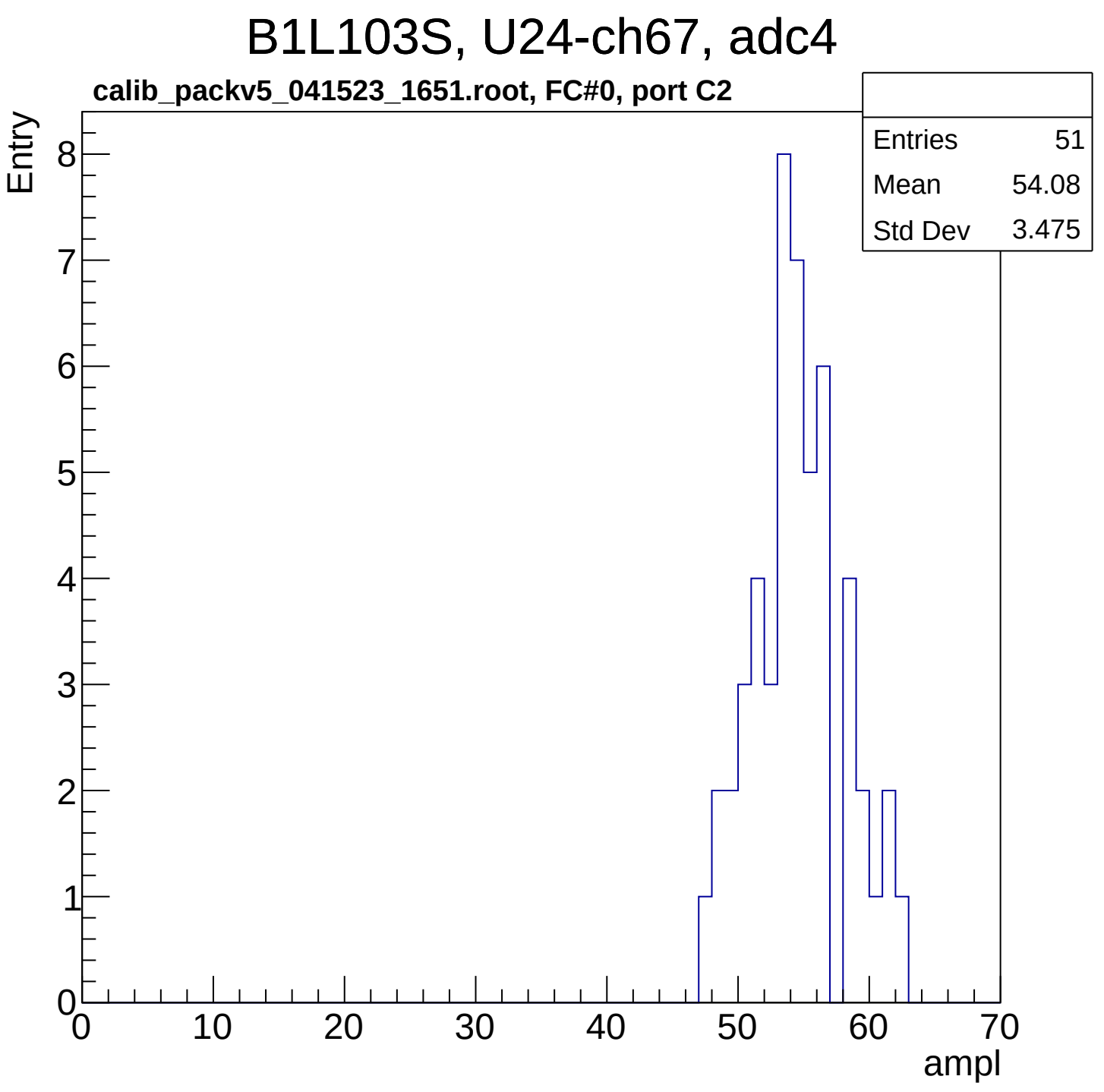
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U24-ch67, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 30.81
Std Dev 11.63
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U24-ch67, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 41.31
Std Dev 6.187
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U24-ch67, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 48.54
Std Dev 3.447
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U24-ch67, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 54.08
Std Dev 3.475
Entry
ampl
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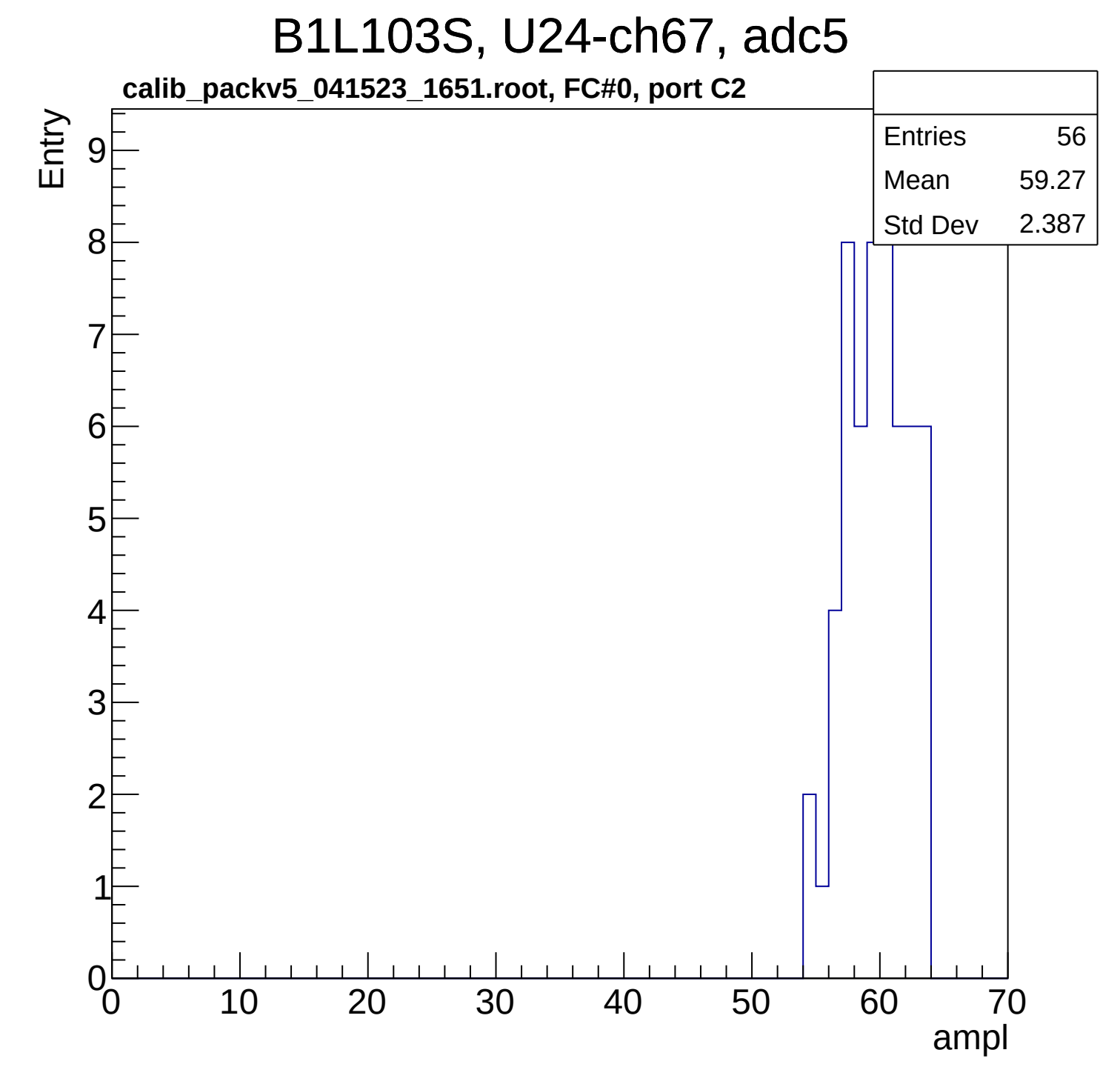
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U24-ch67, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 59.27
Std Dev 2.387
Entry
ampl
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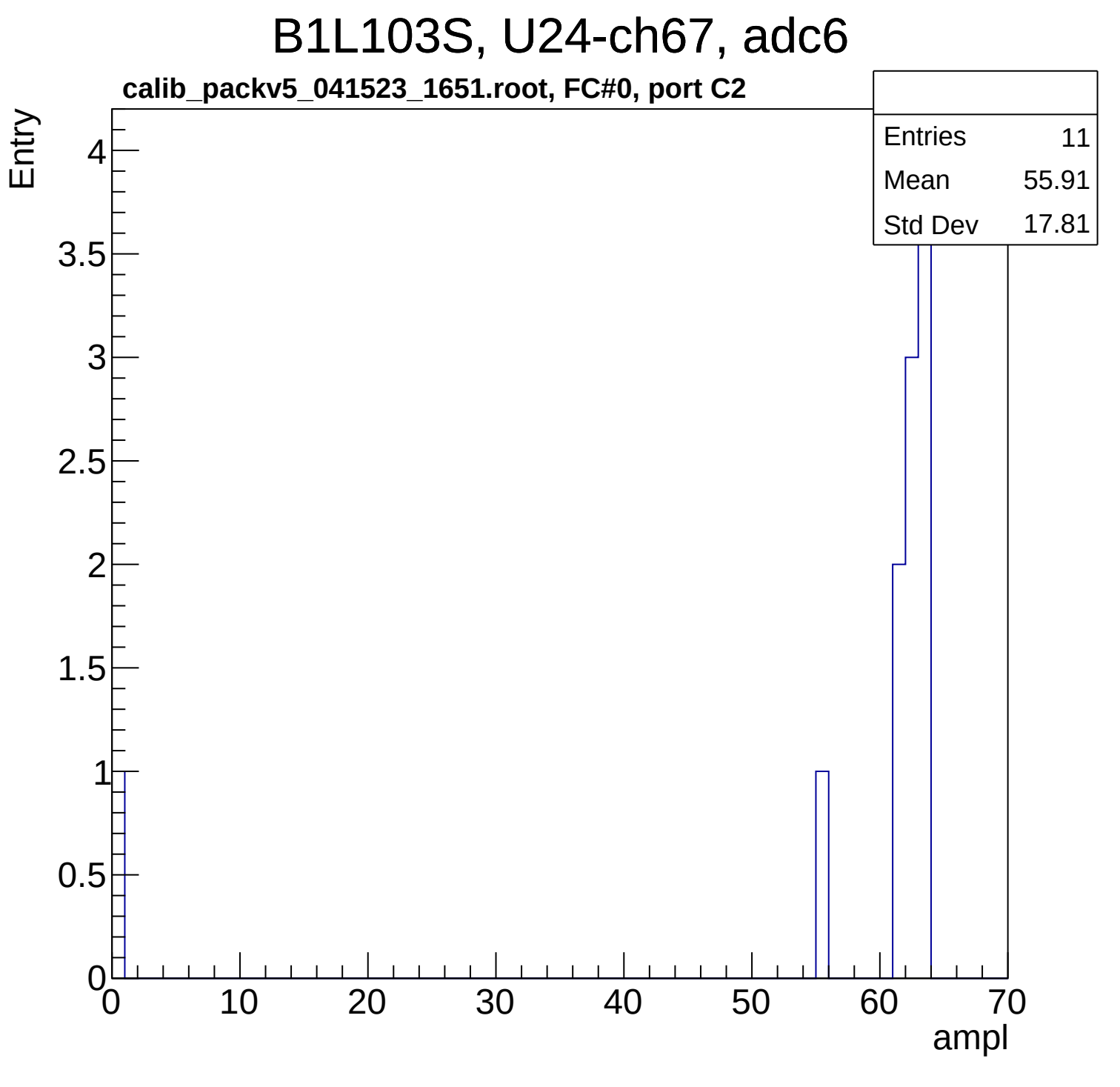
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U24-ch67, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 55.91
Std Dev 17.81
Entry
ampl
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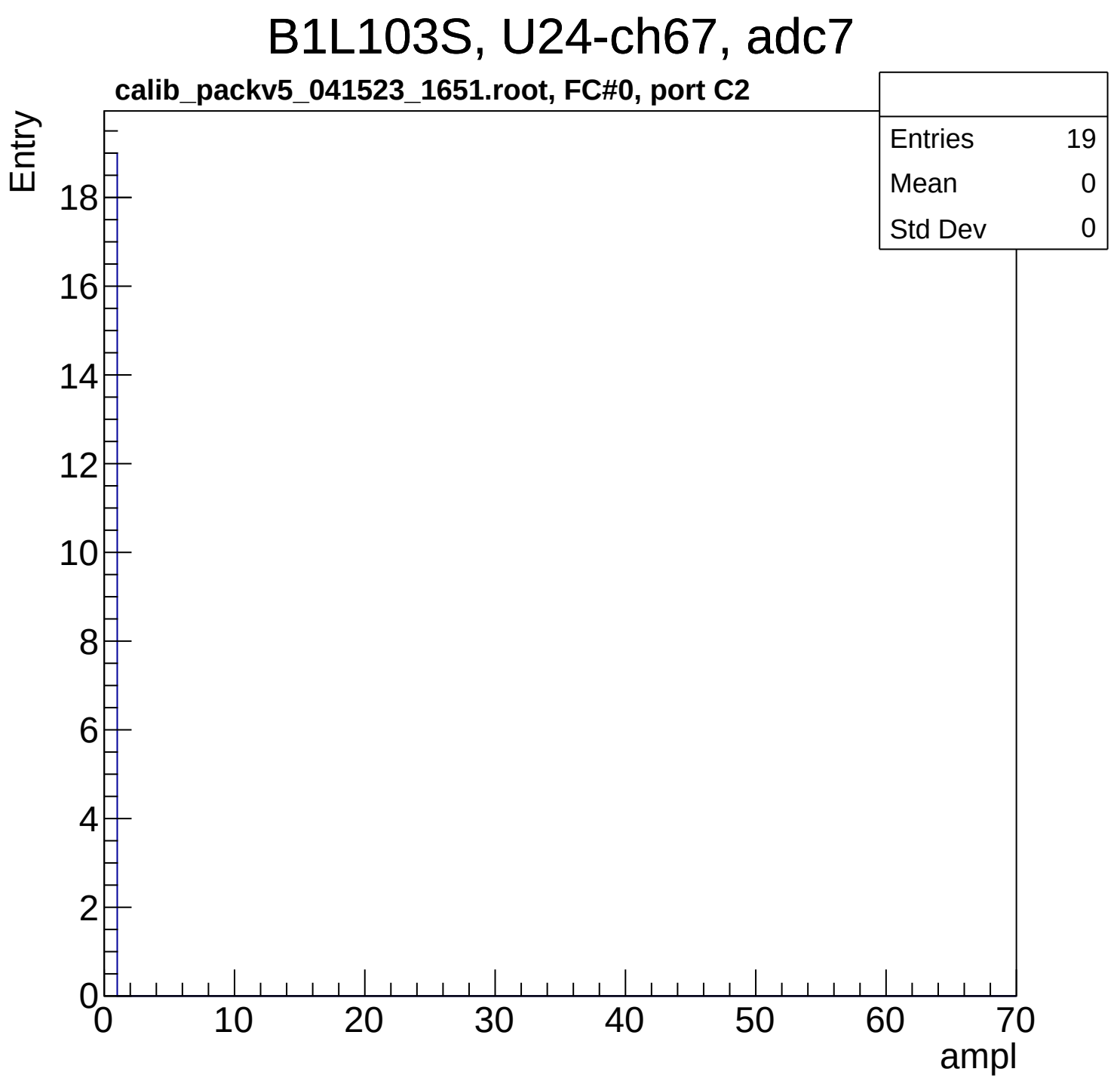
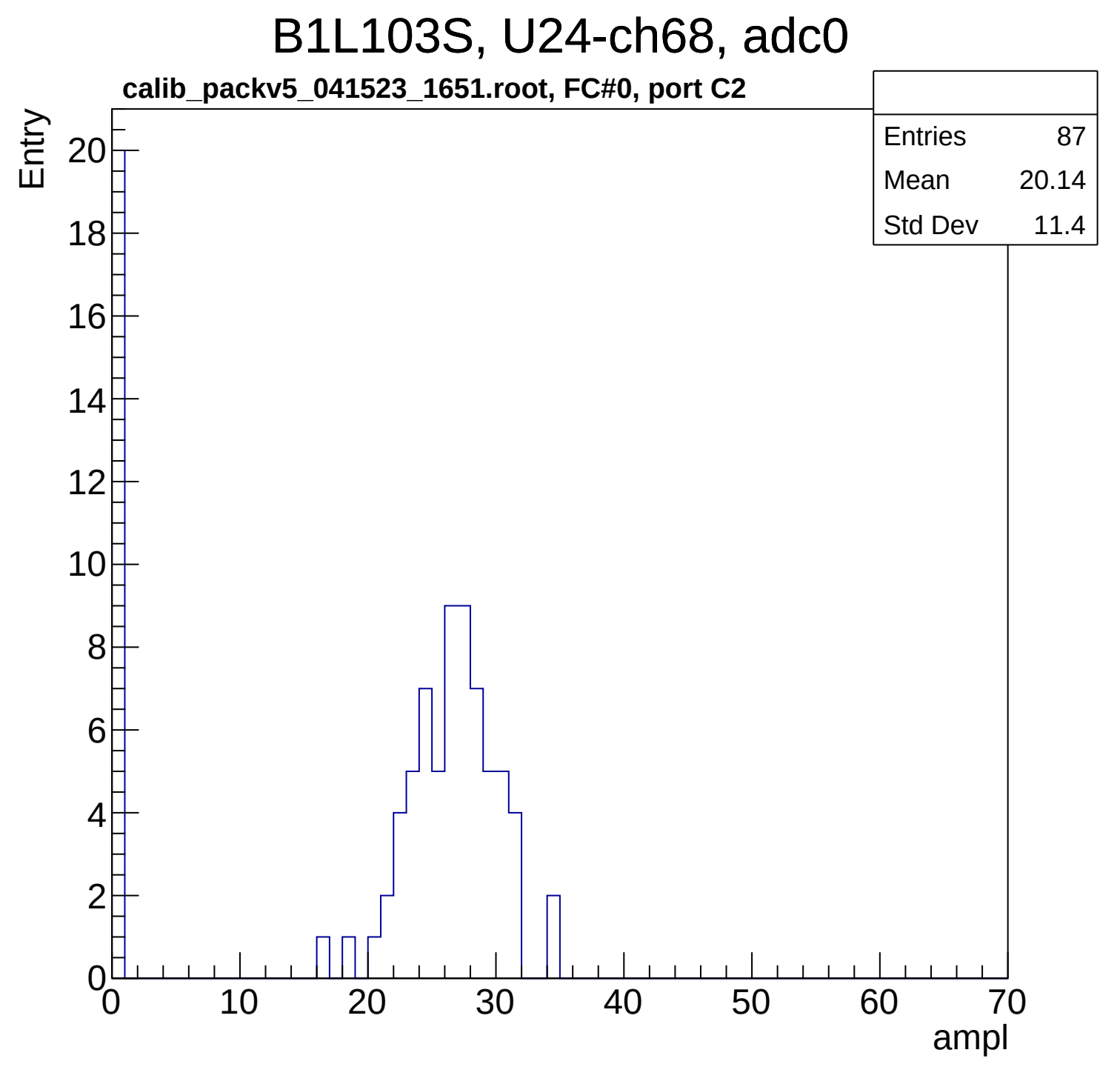
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U24-ch67, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch68, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 87
Mean 20.14
Std Dev 11.4
Entry
ampl
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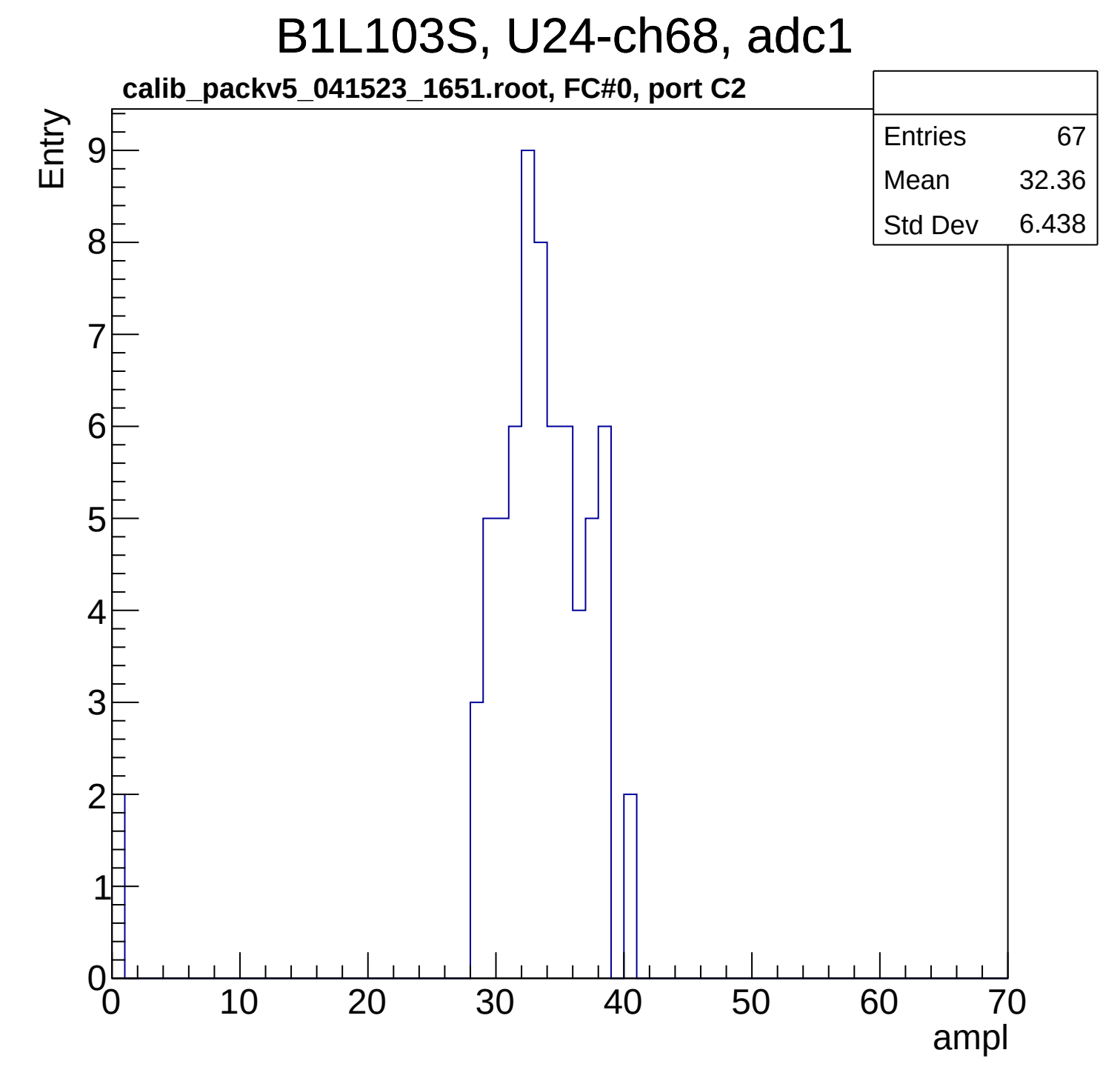
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70


B1L103S, U24-ch68, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 32.36
Std Dev 6.438
Entry
ampl
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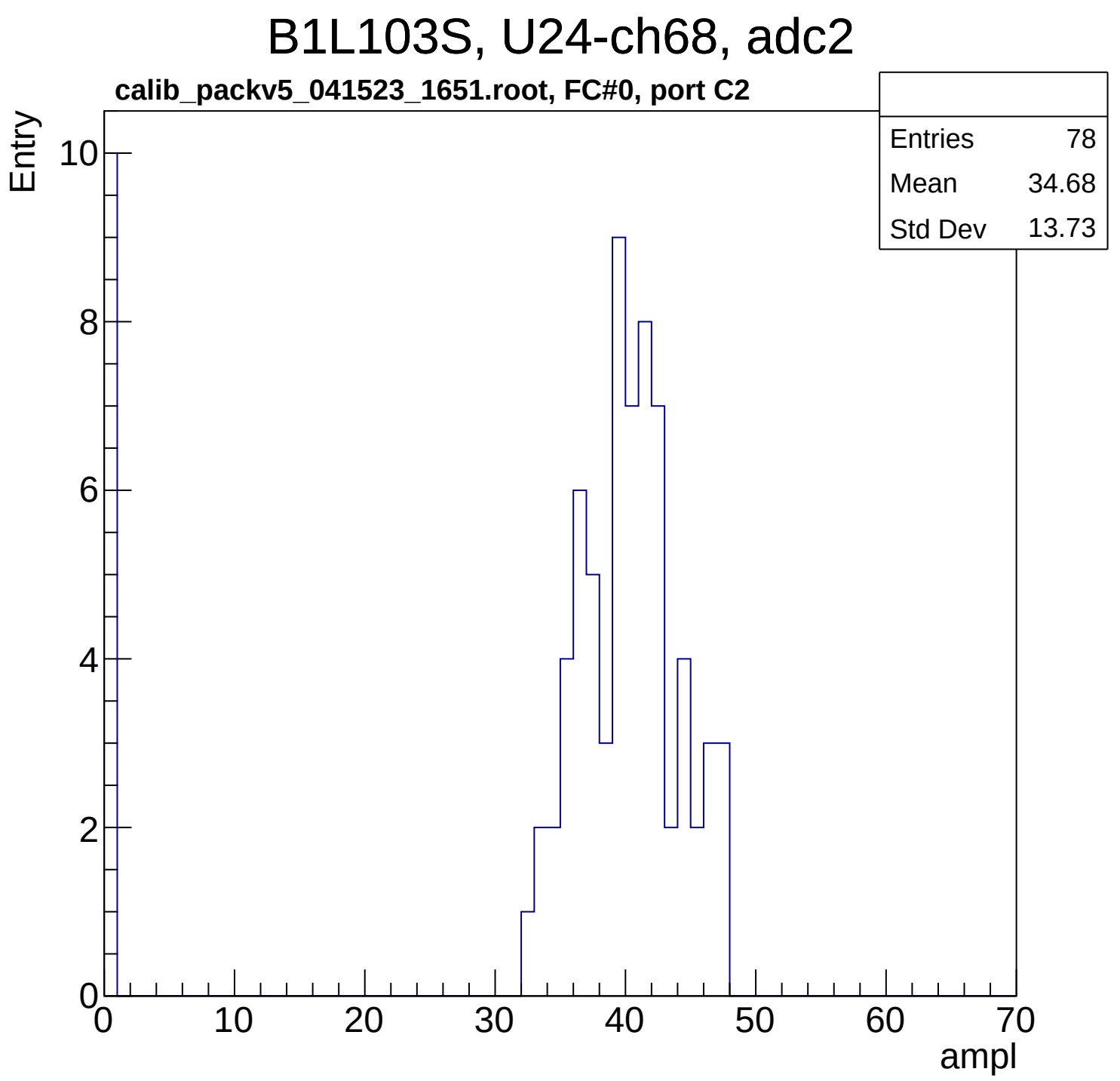
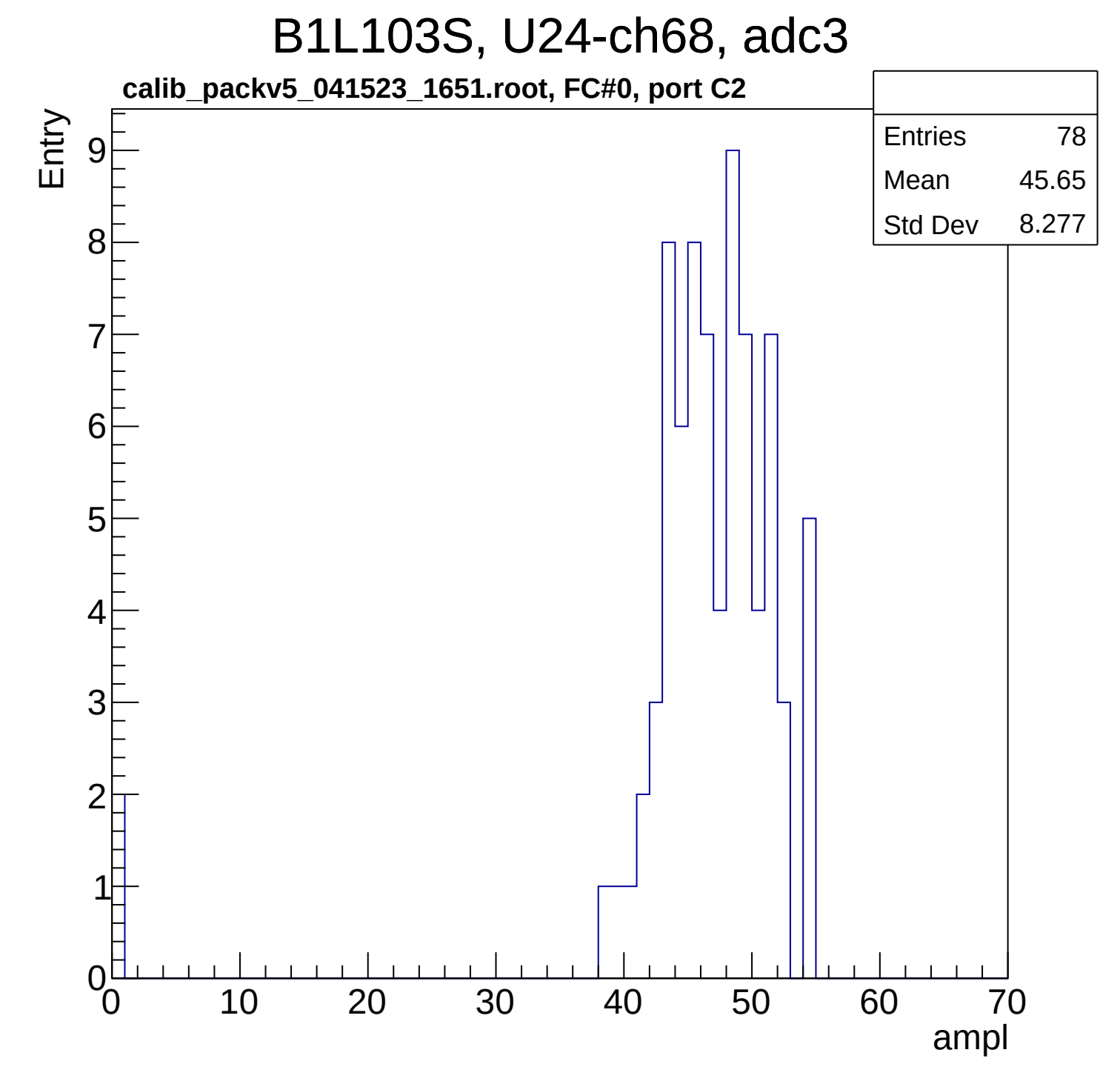
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U24-ch68, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 34.68
Std Dev 13.73
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch68, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 45.65
Std Dev 8.277
Entry
ampl
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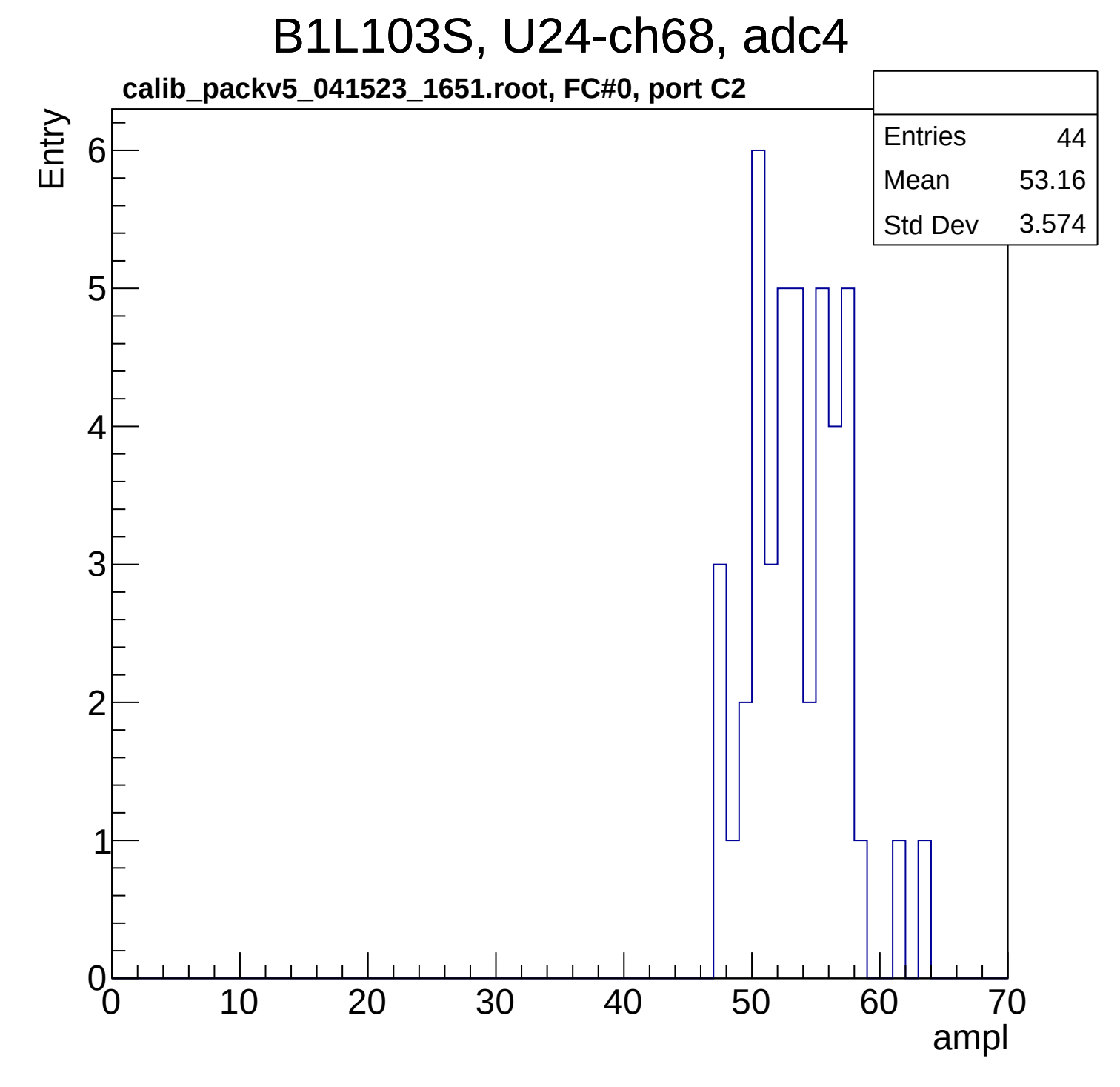
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U24-ch68, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 53.16
Std Dev 3.574
Entry
ampl
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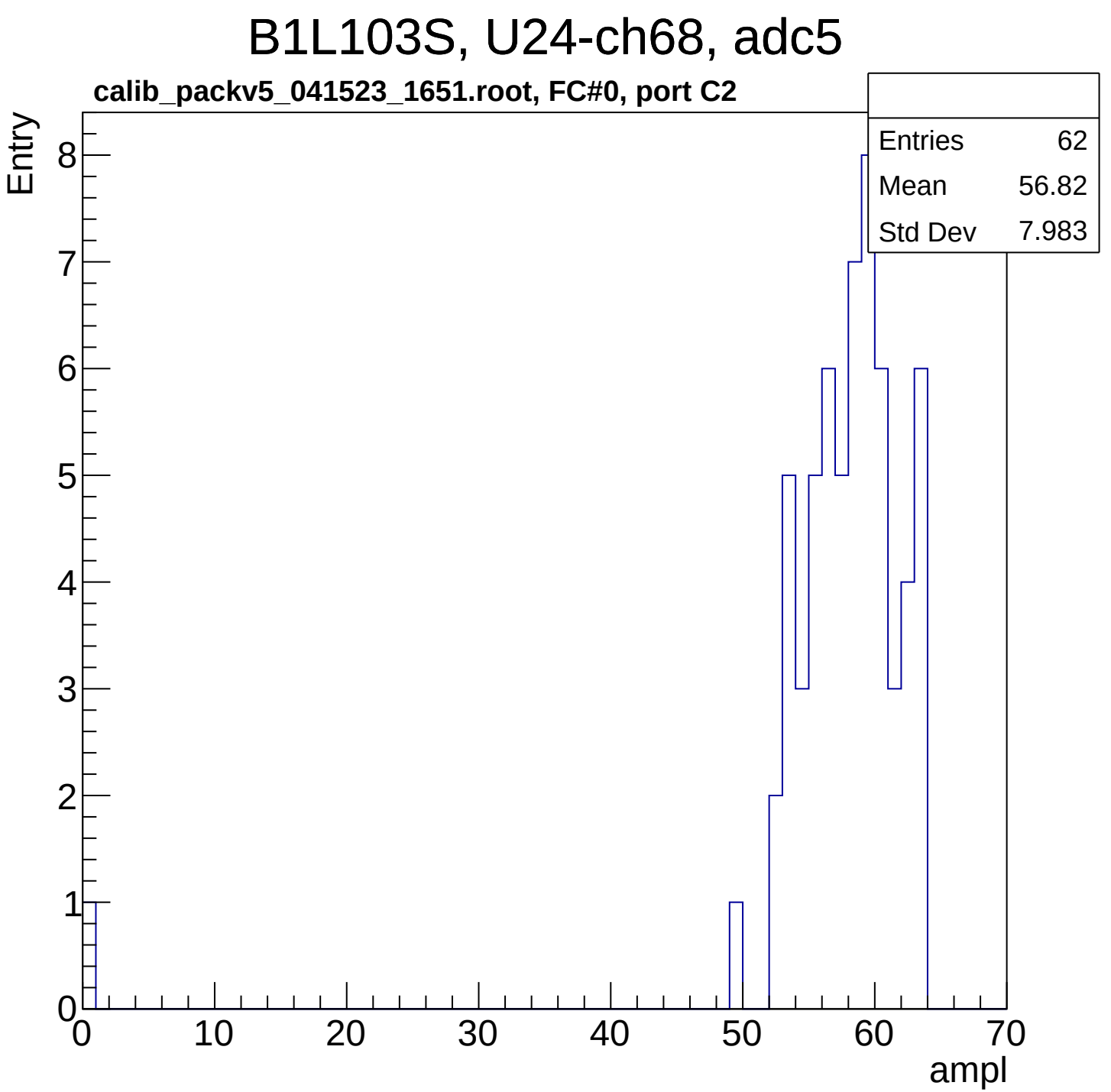
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U24-ch68, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 56.82
Std Dev 7.983
Entry
ampl
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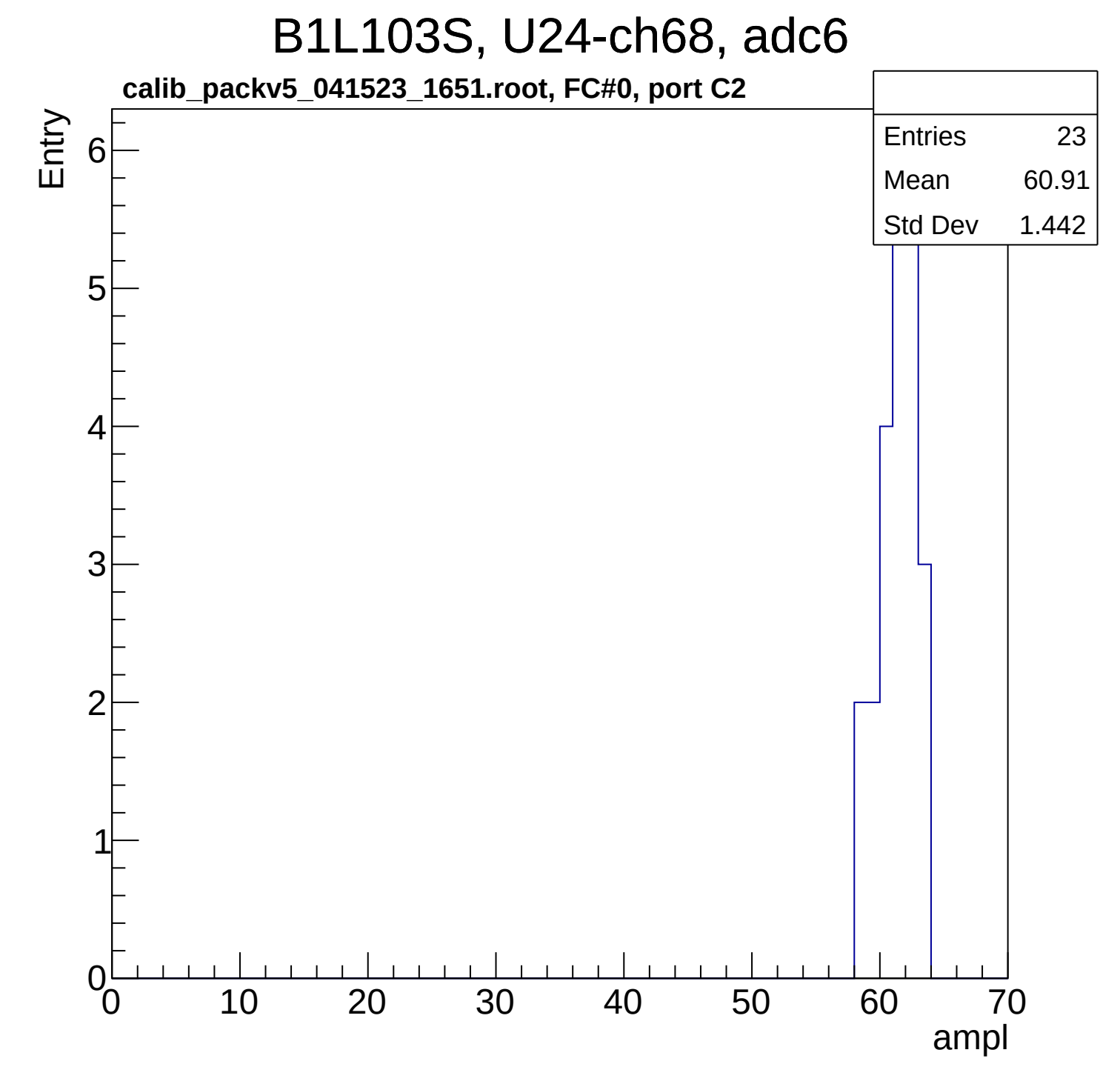
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U24-ch68, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 23
Mean 60.91
Std Dev 1.442
Entry
ampl
0
1
2
3
4
5
6
0
10
20
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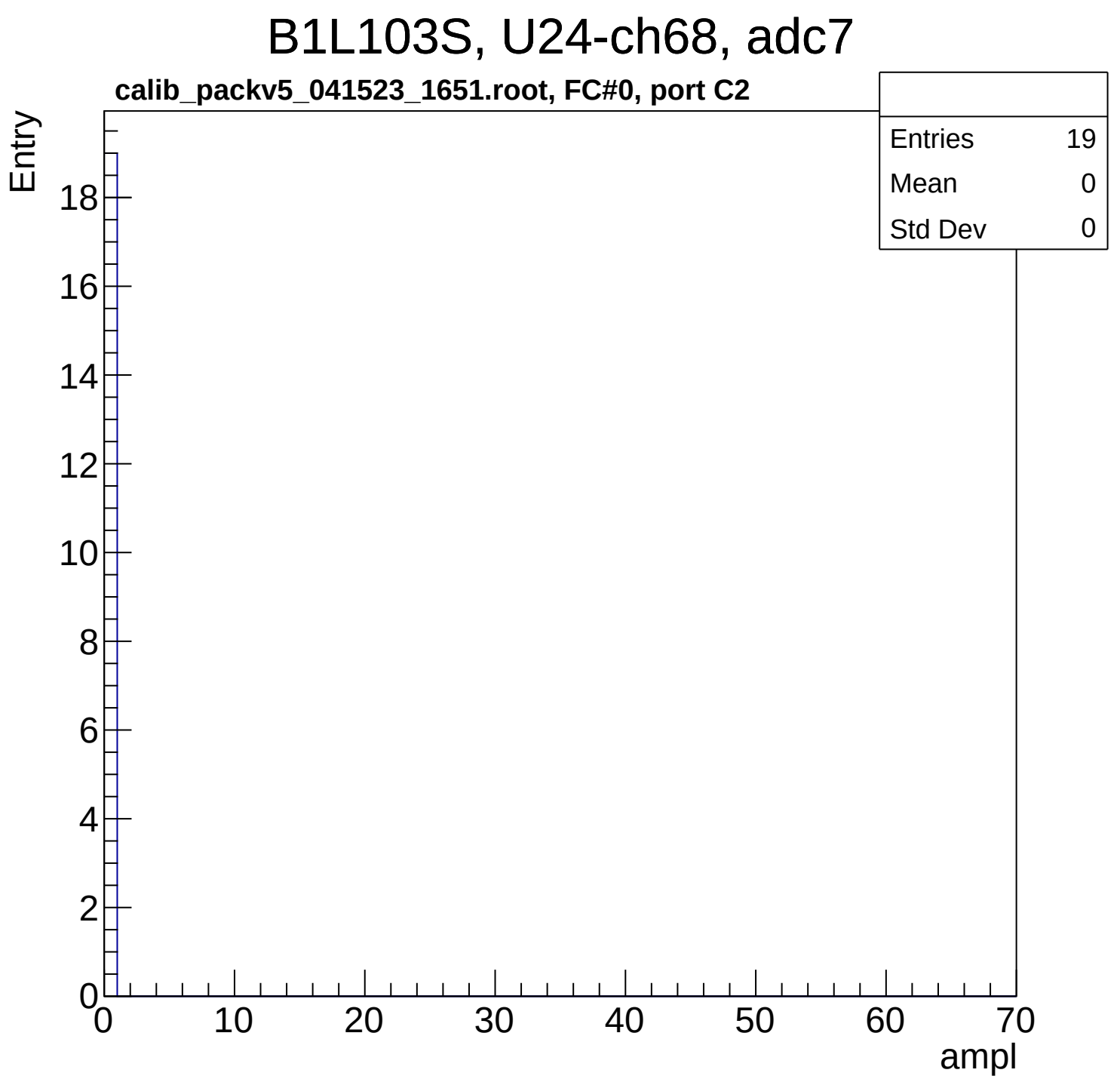
40
50
60
70


B1L103S, U24-ch68, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
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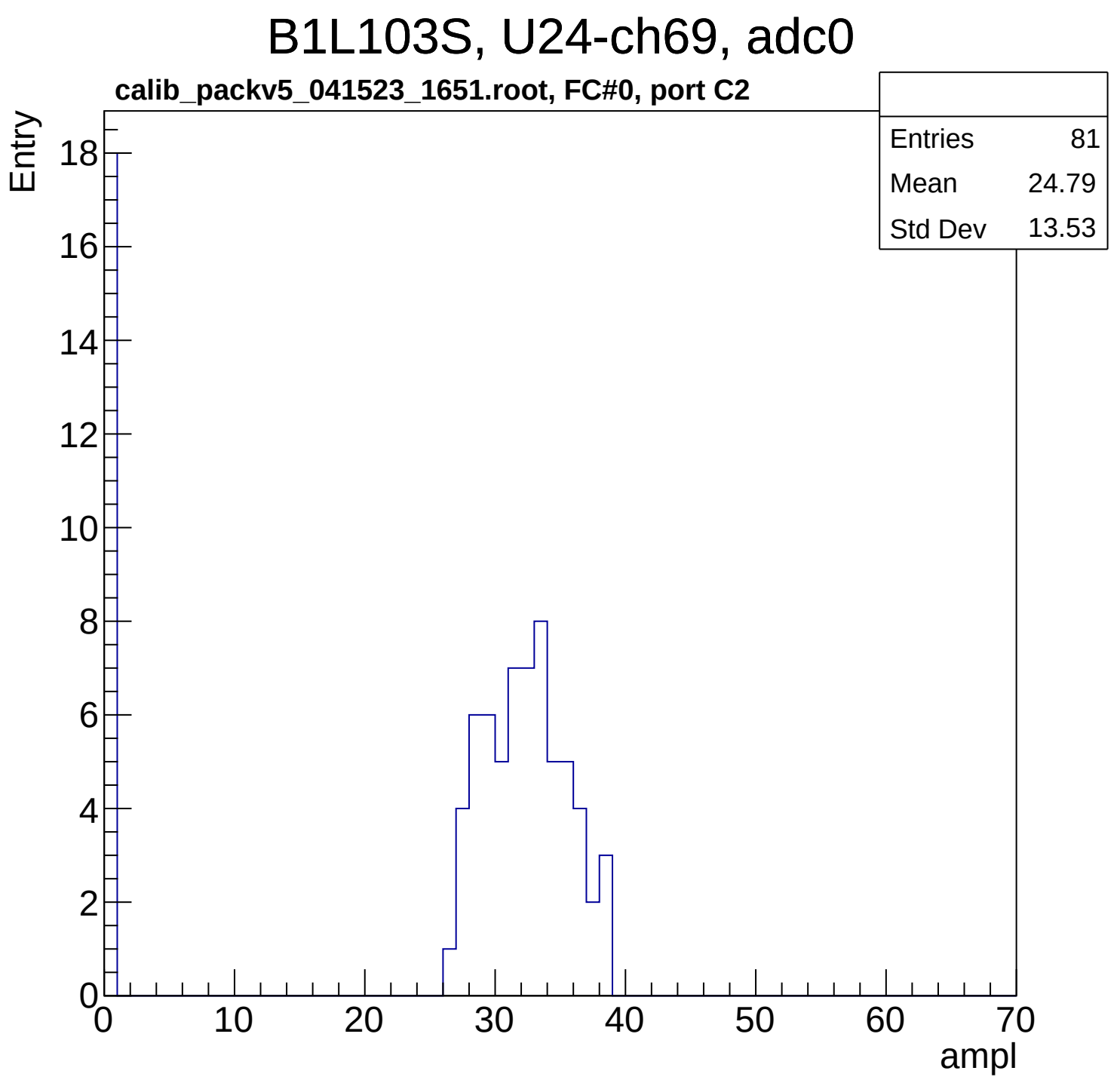
50
60
70
ampl


B1L103S, U24-ch69, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 24.79
Std Dev 13.53
Entry
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6
8
10
12
14
16
18
0
10
20
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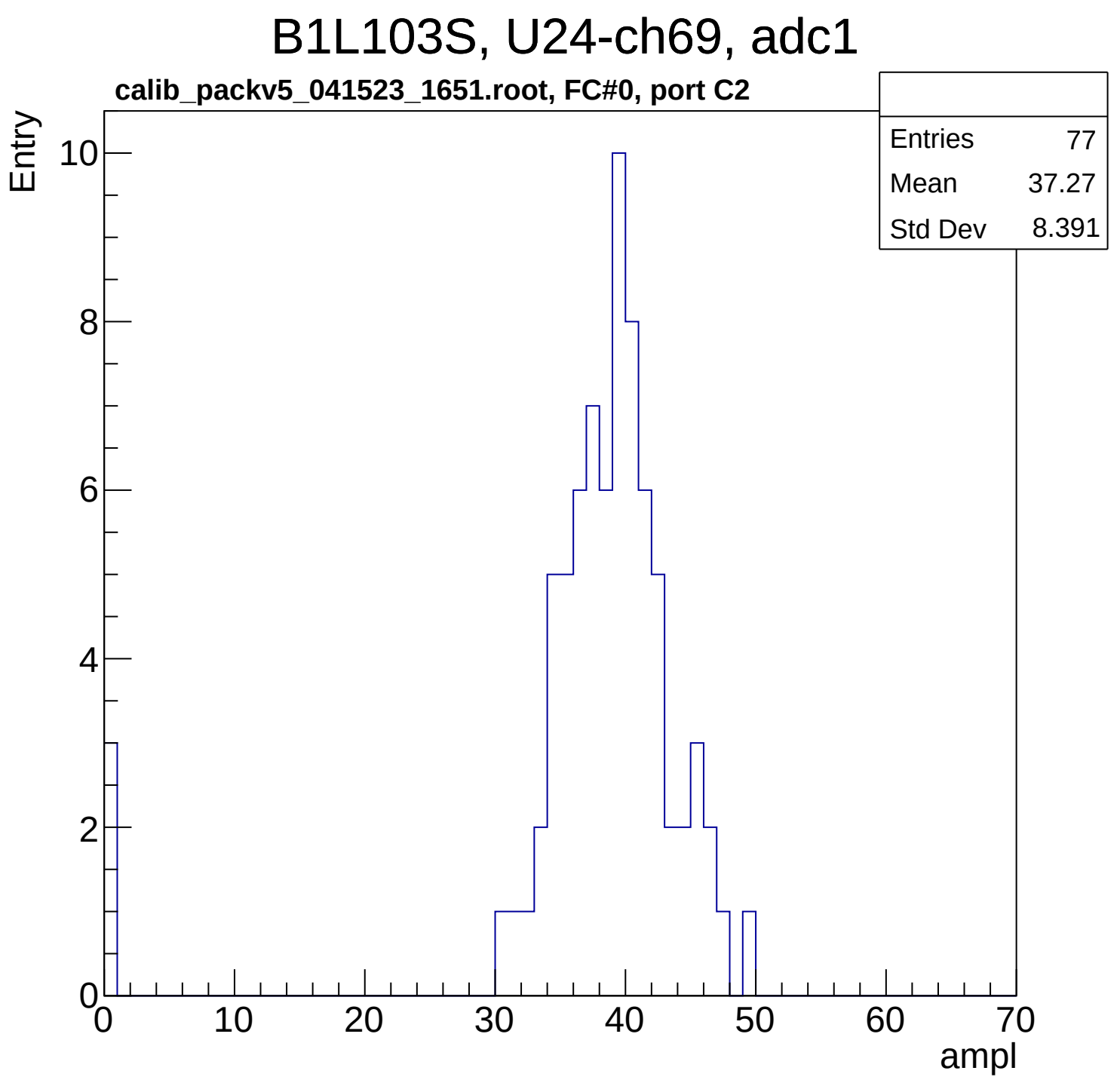
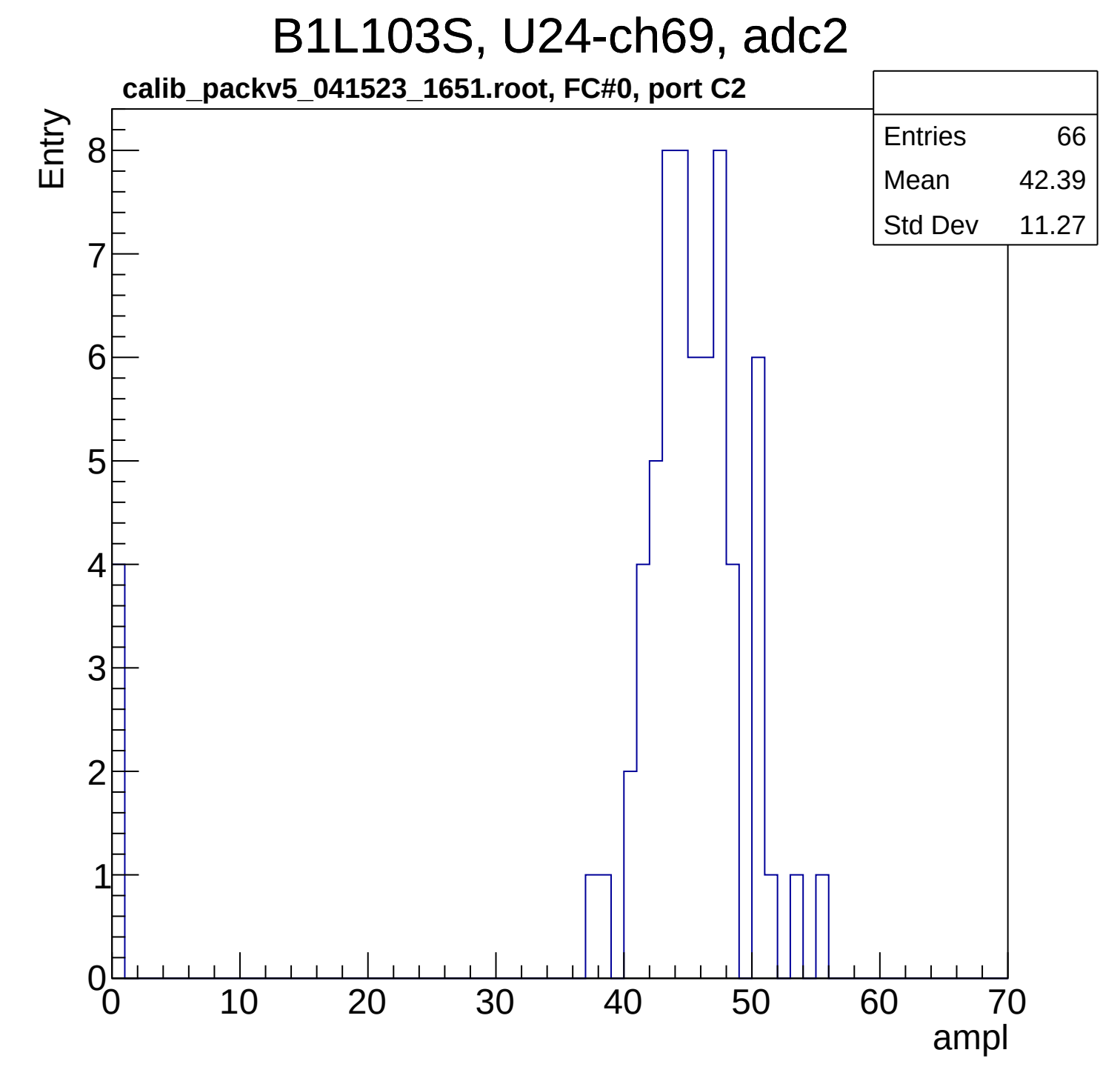
40
50
60
70
ampl


B1L103S, U24-ch69, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 37.27
Std Dev 8.391
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U24-ch69, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 42.39
Std Dev 11.27
Entry
ampl
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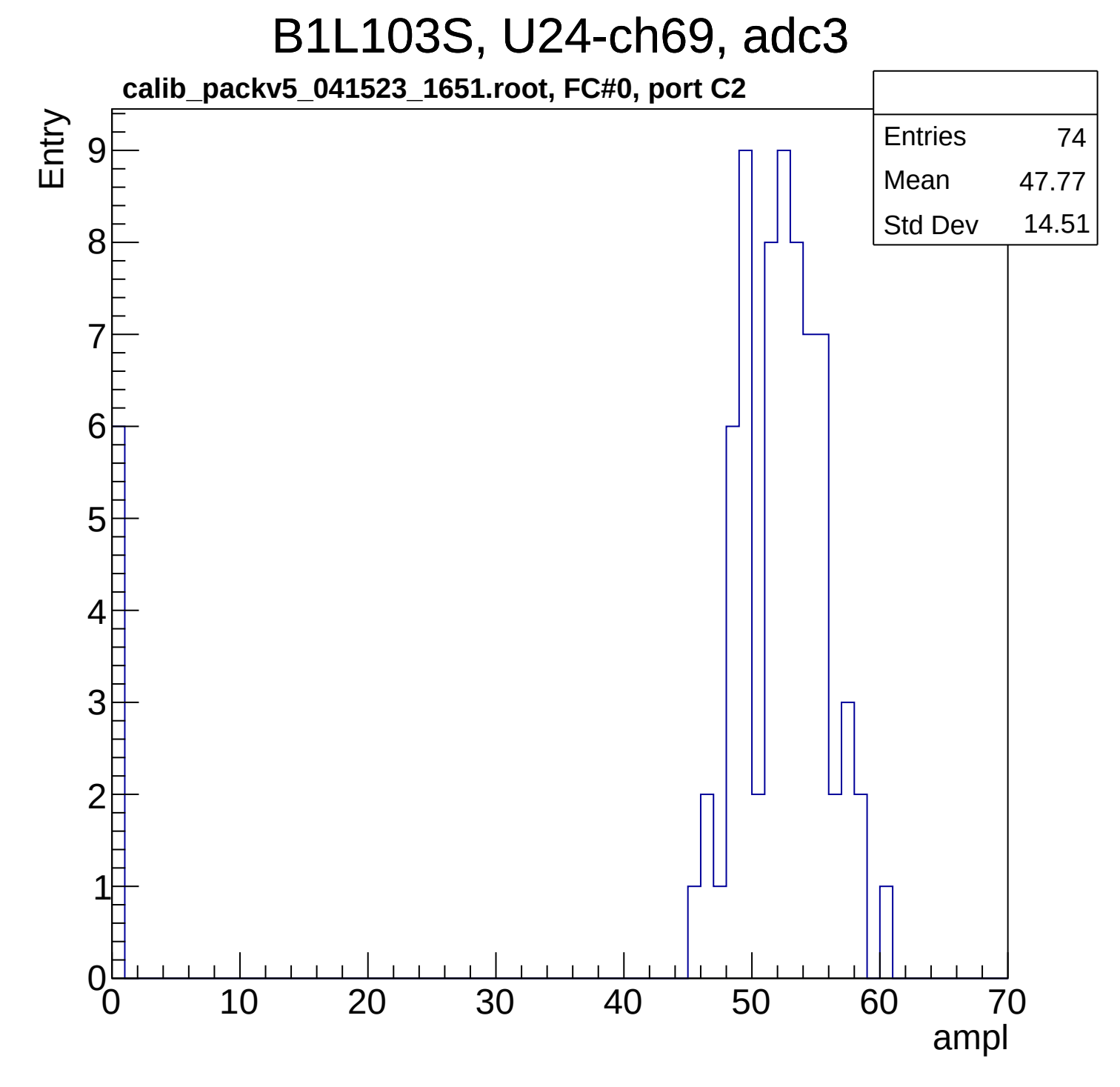
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U24-ch69, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 47.77
Std Dev 14.51
Entry
ampl
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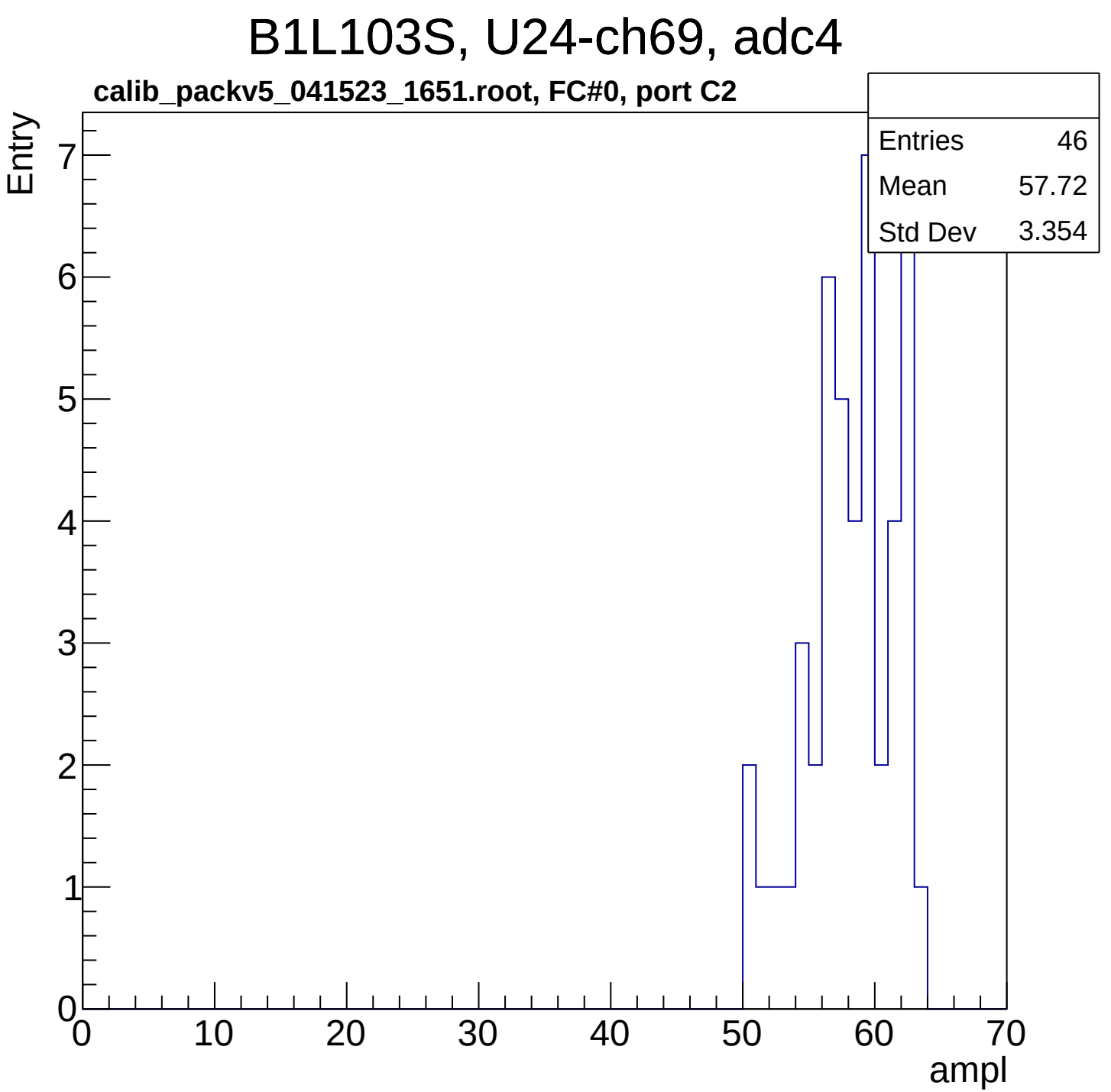
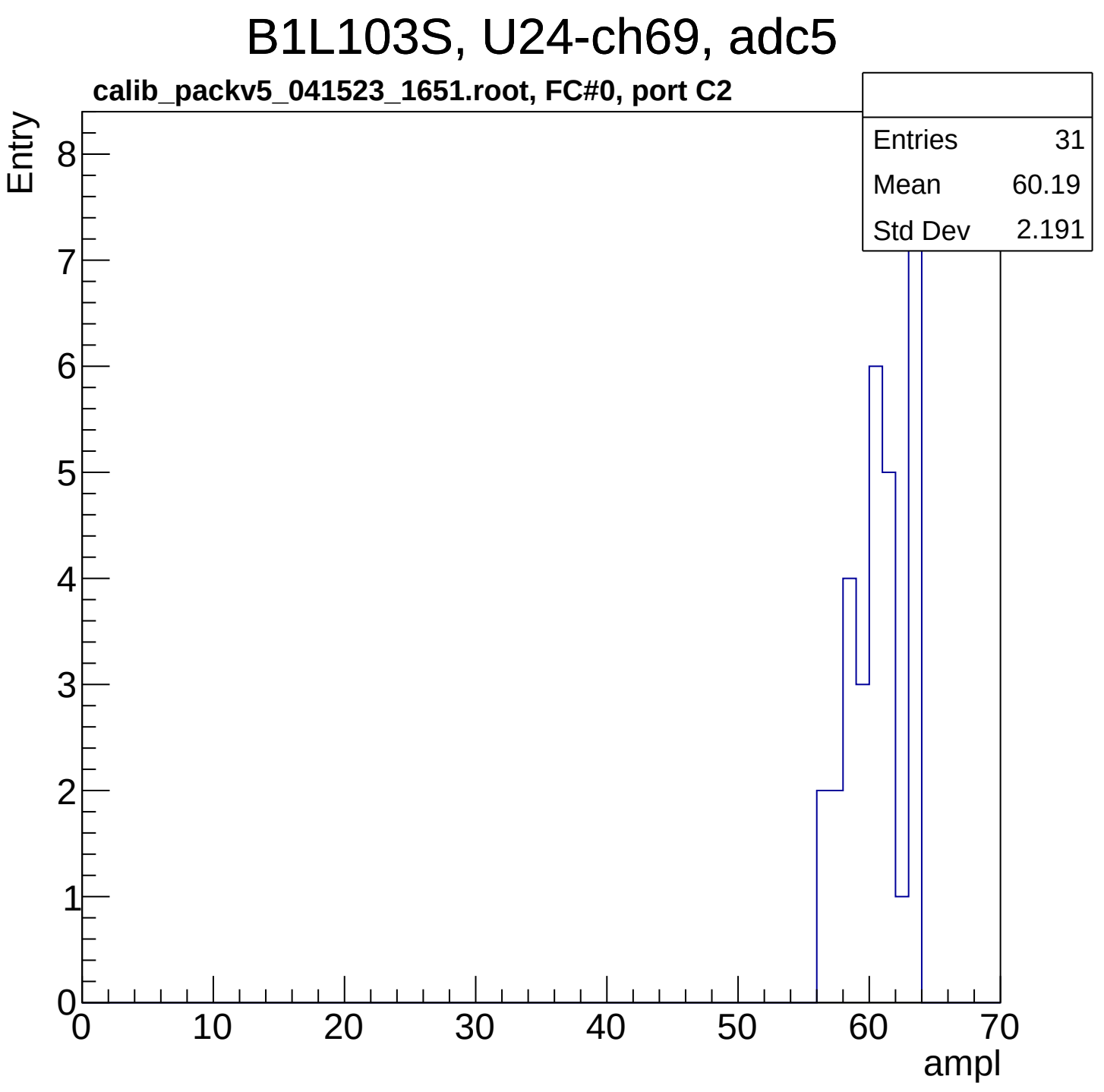
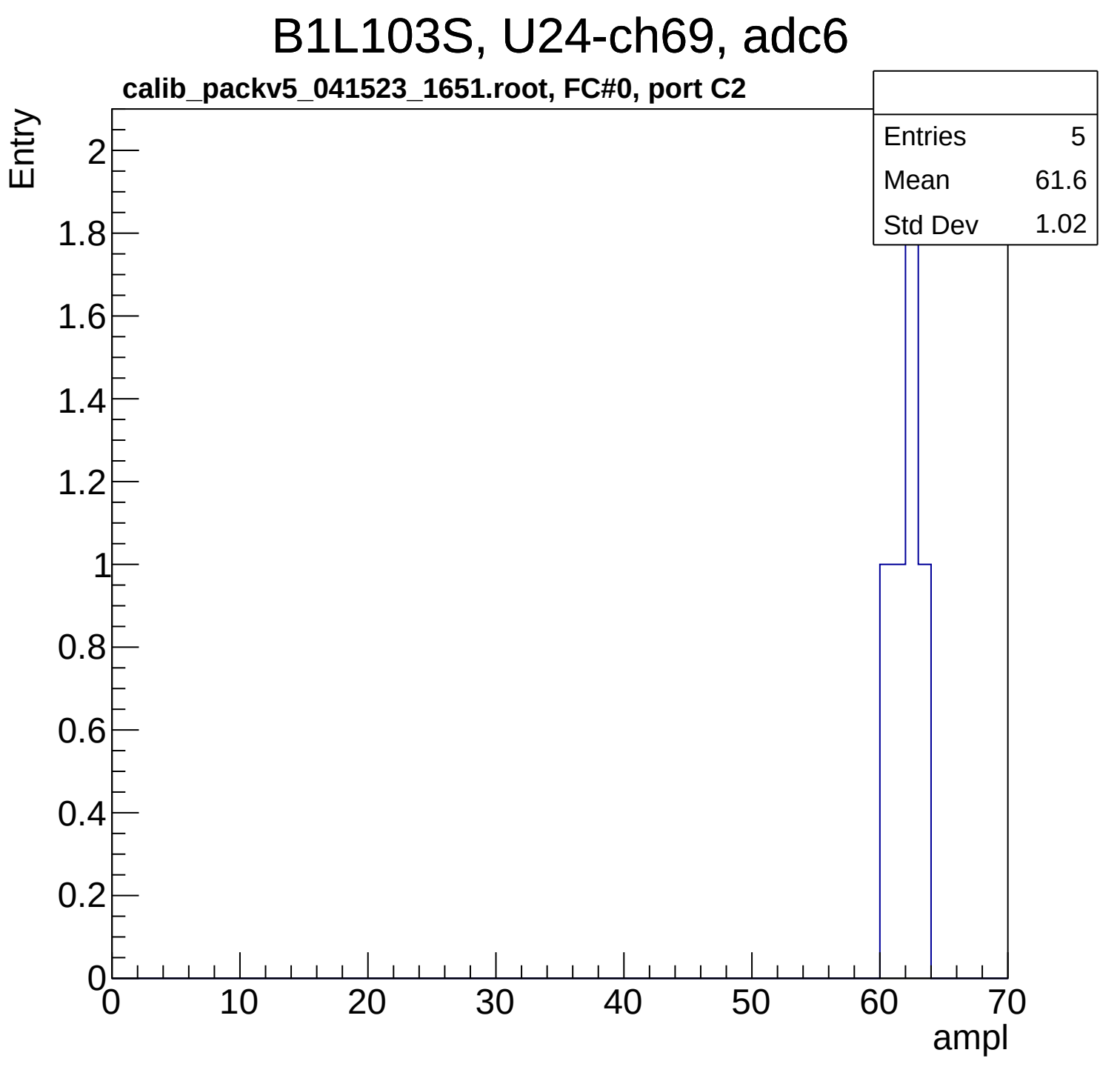
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U24-ch69, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 57.72
Std Dev 3.354
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U24-ch69, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 31
Mean 60.19
Std Dev 2.191
Entry
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch69, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 5
Mean 61.6
Std Dev 1.02
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
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30
40
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60
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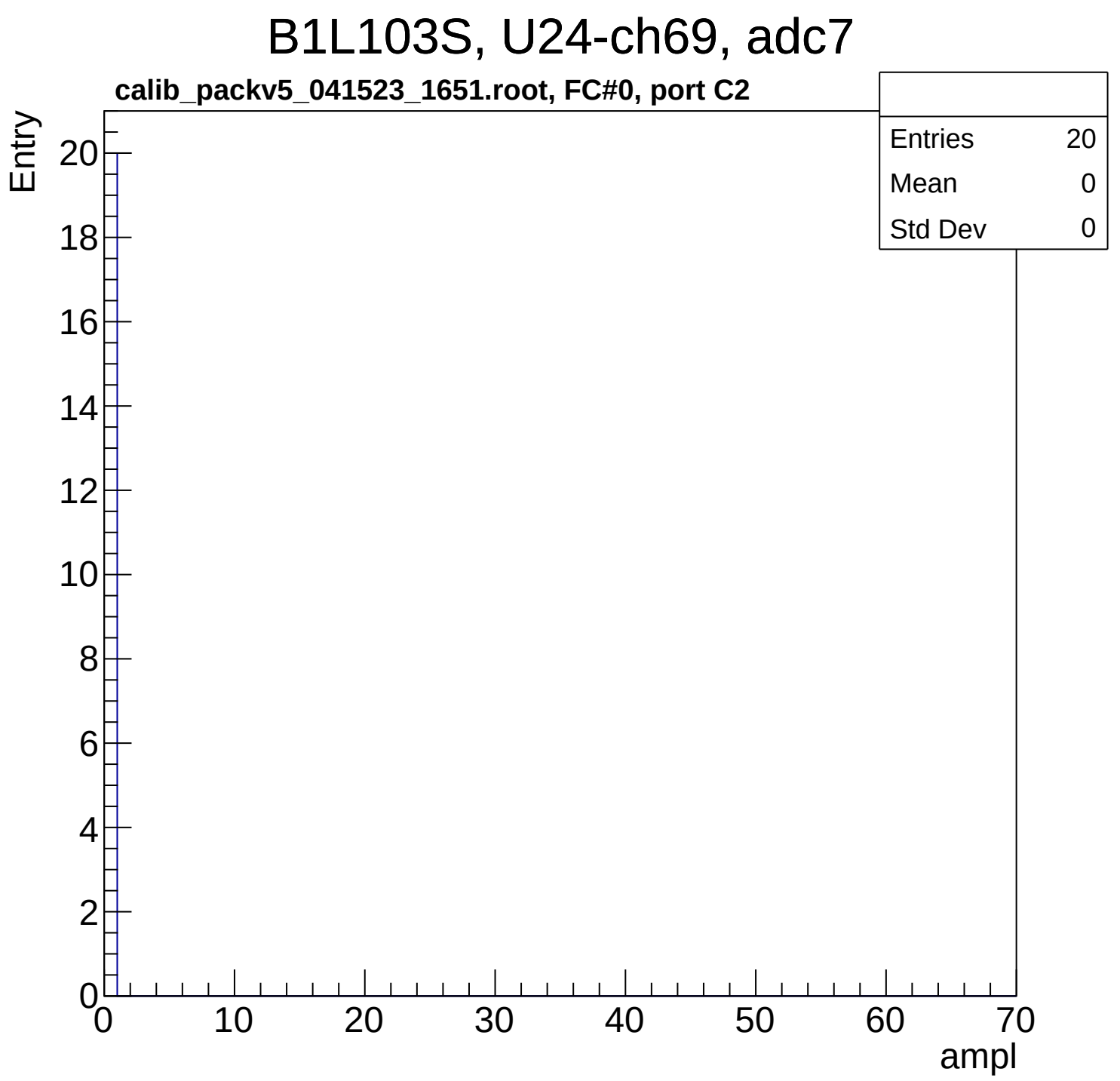
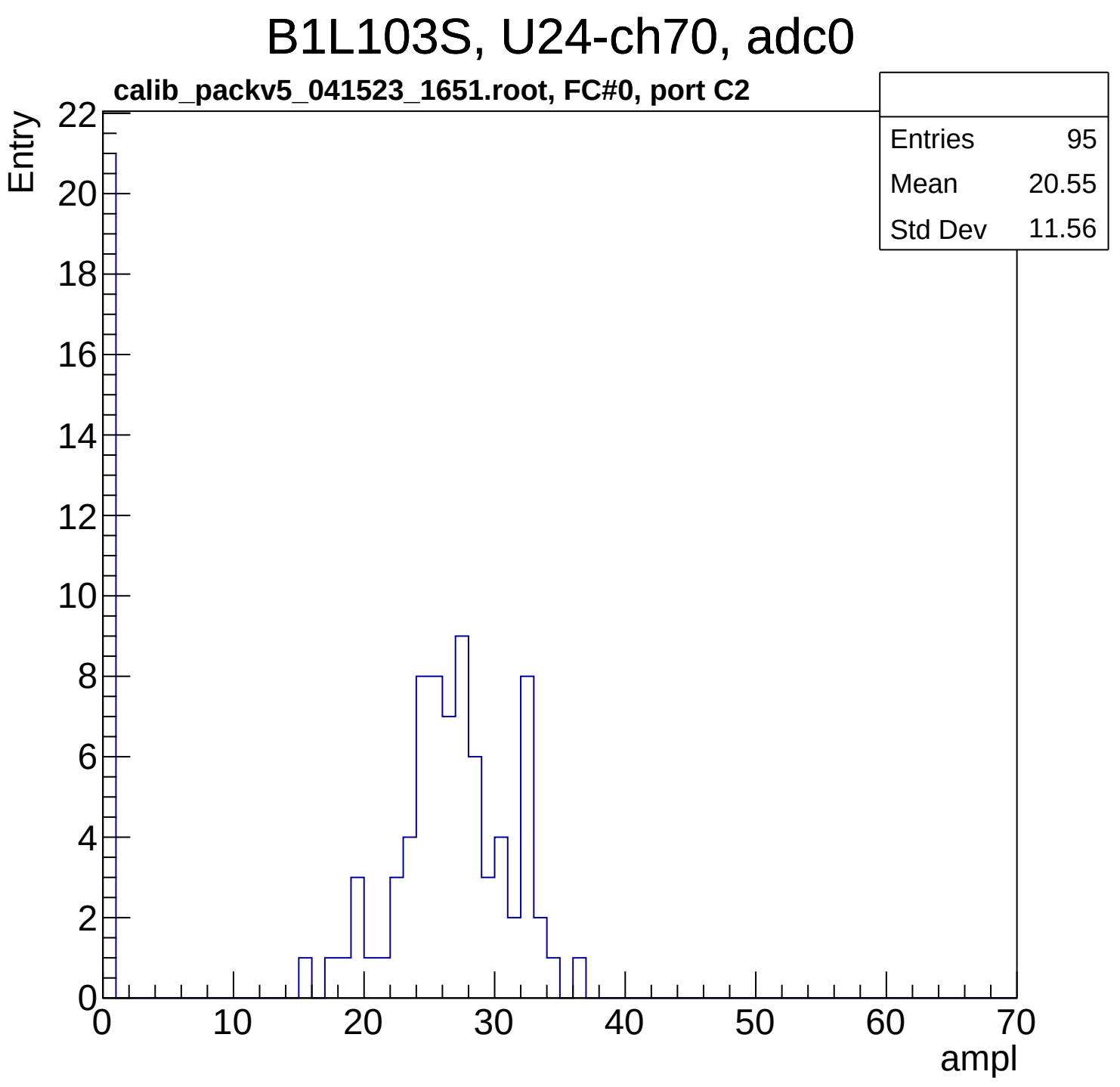

B1L103S, U24-ch69, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch70, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 95
Mean 20.55
Std Dev 11.56
Entry
ampl
0
2
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8
10
12
14
16
18
20
22
0
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30
40
50
60
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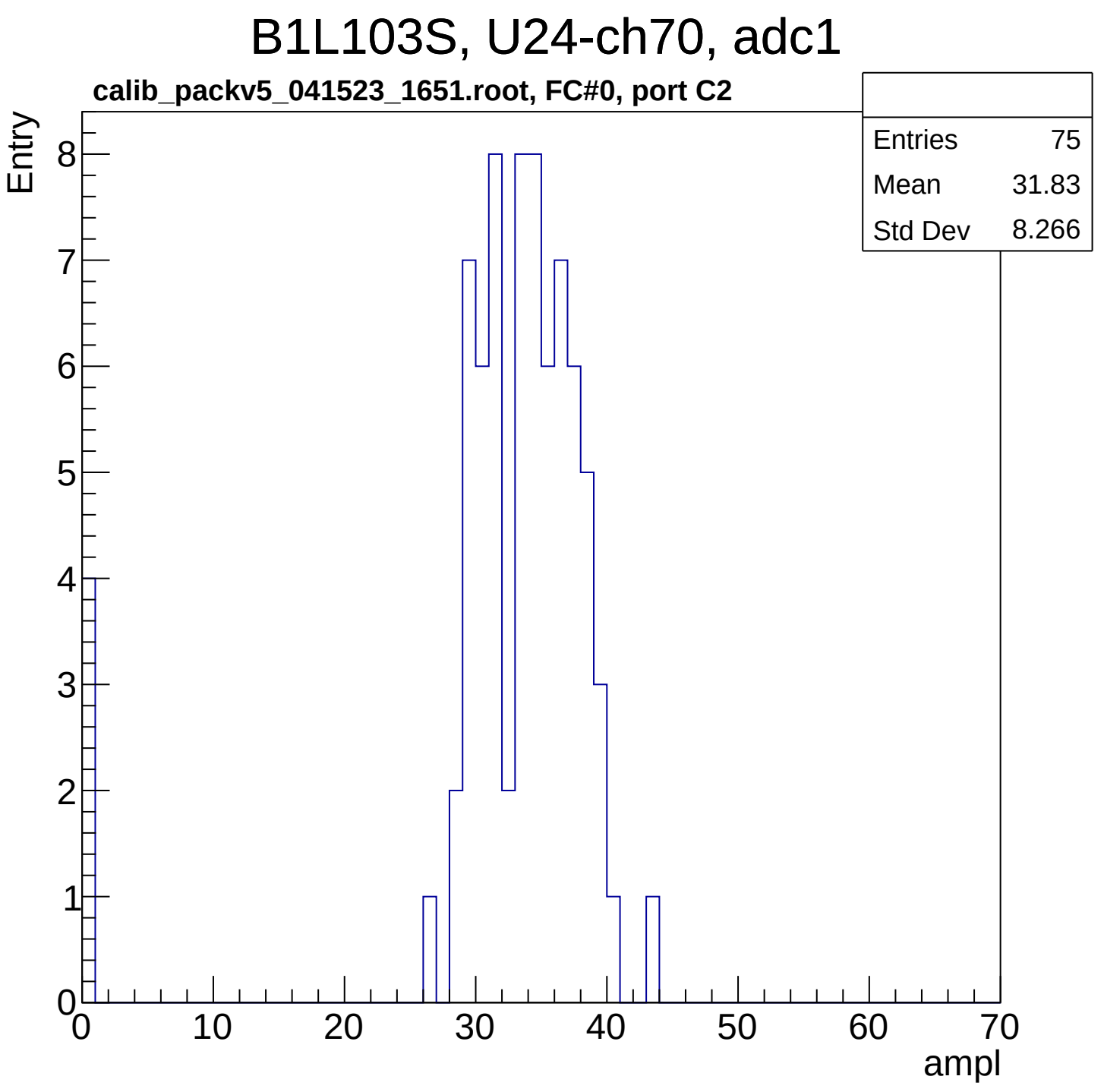
B1L103S, U24-ch70, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 31.83
Std Dev 8.266
Entry
ampl
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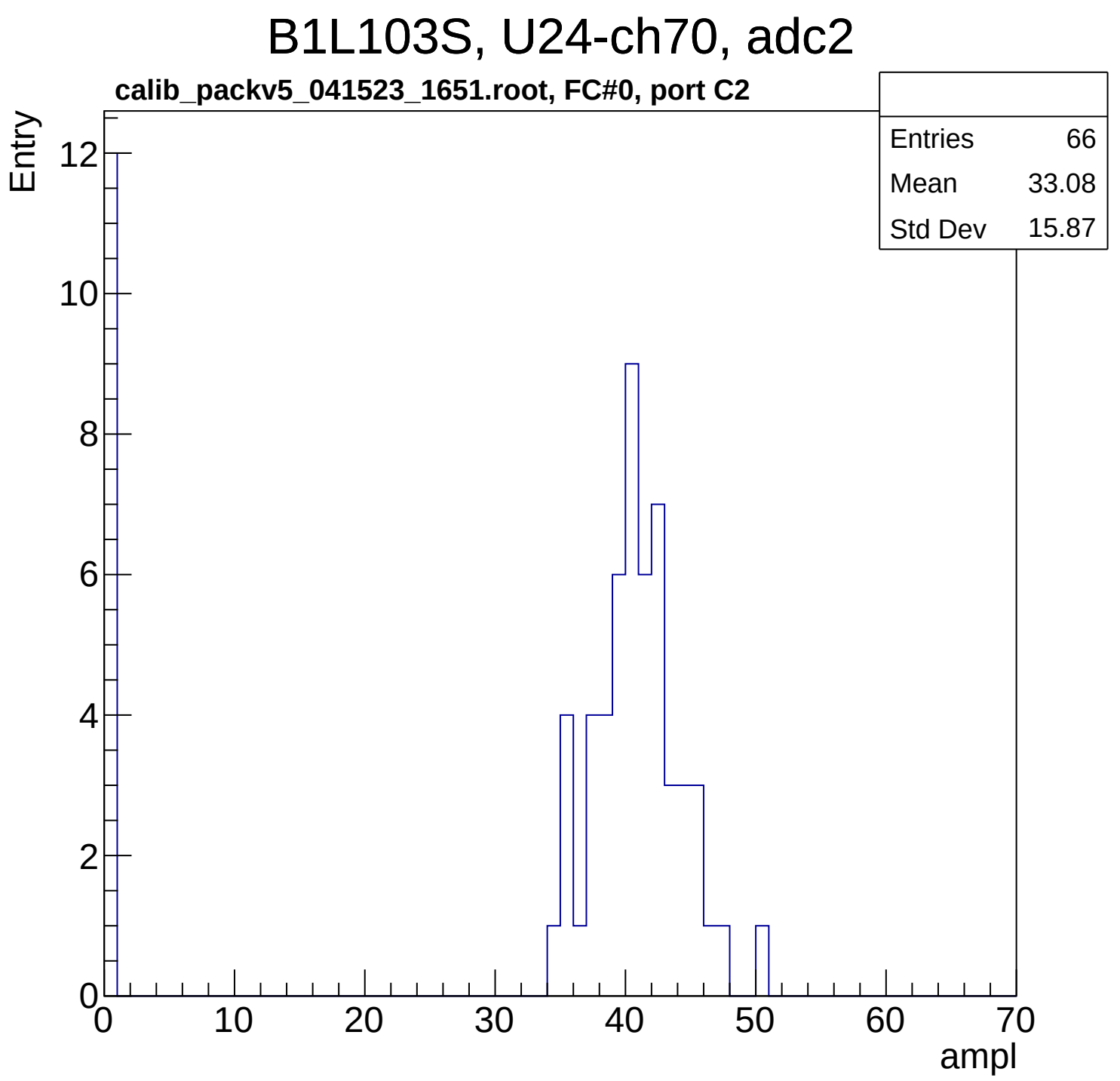
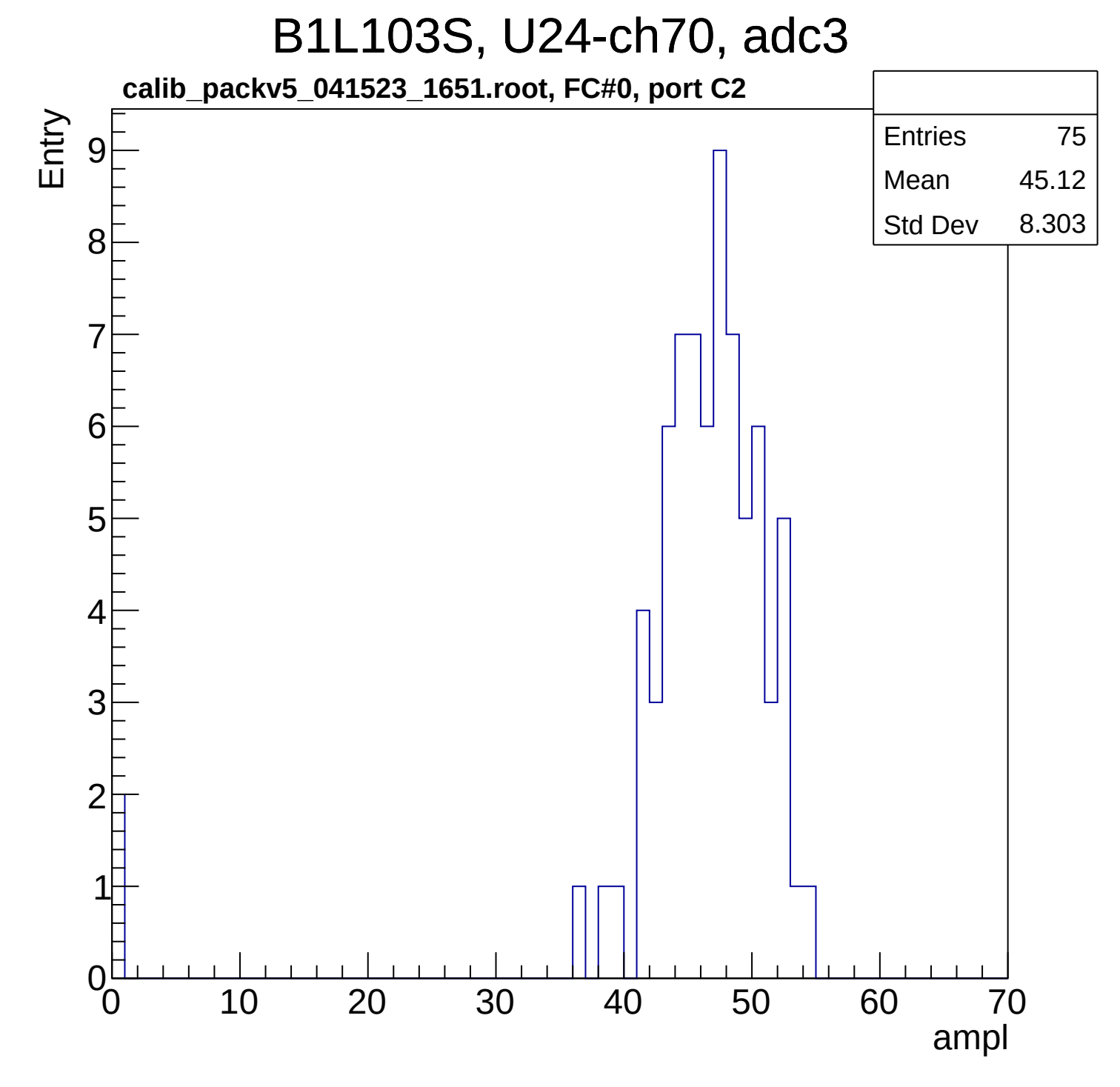
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U24-ch70, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 33.08
Std Dev 15.87
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch70, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 45.12
Std Dev 8.303
Entry
ampl
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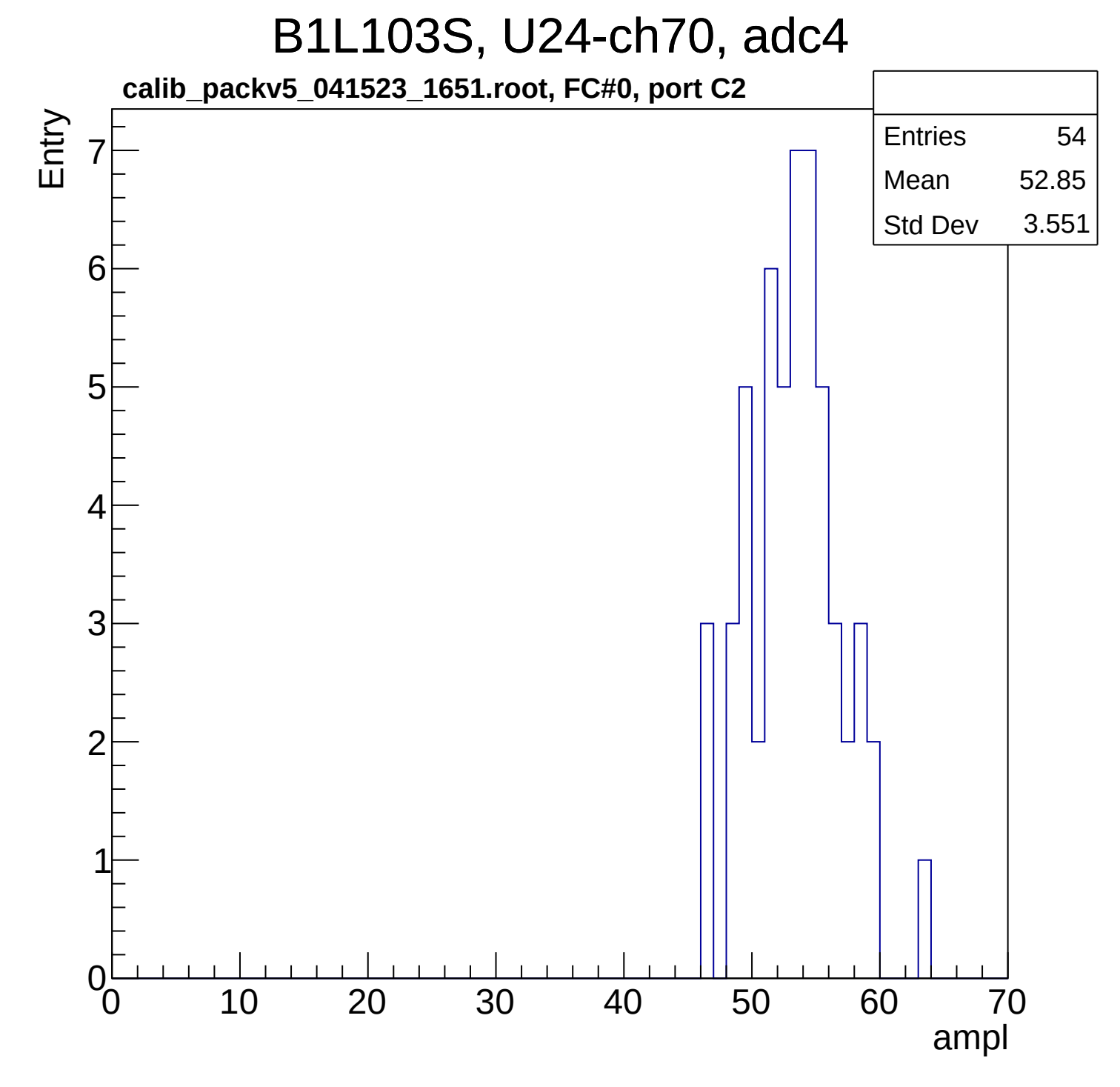
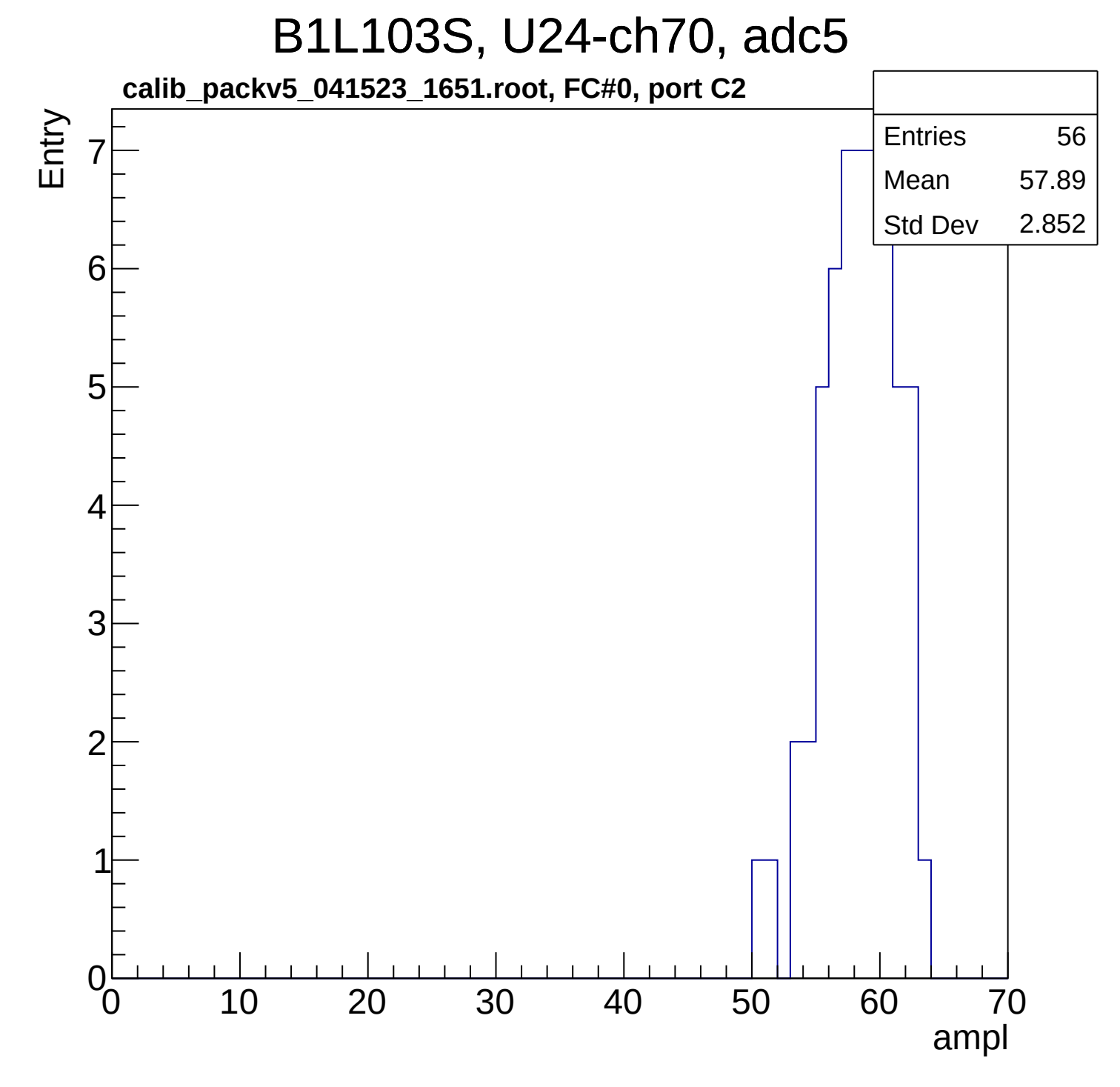
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U24-ch70, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 52.85
Std Dev 3.551
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U24-ch70, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 57.89
Std Dev 2.852
Entry
ampl
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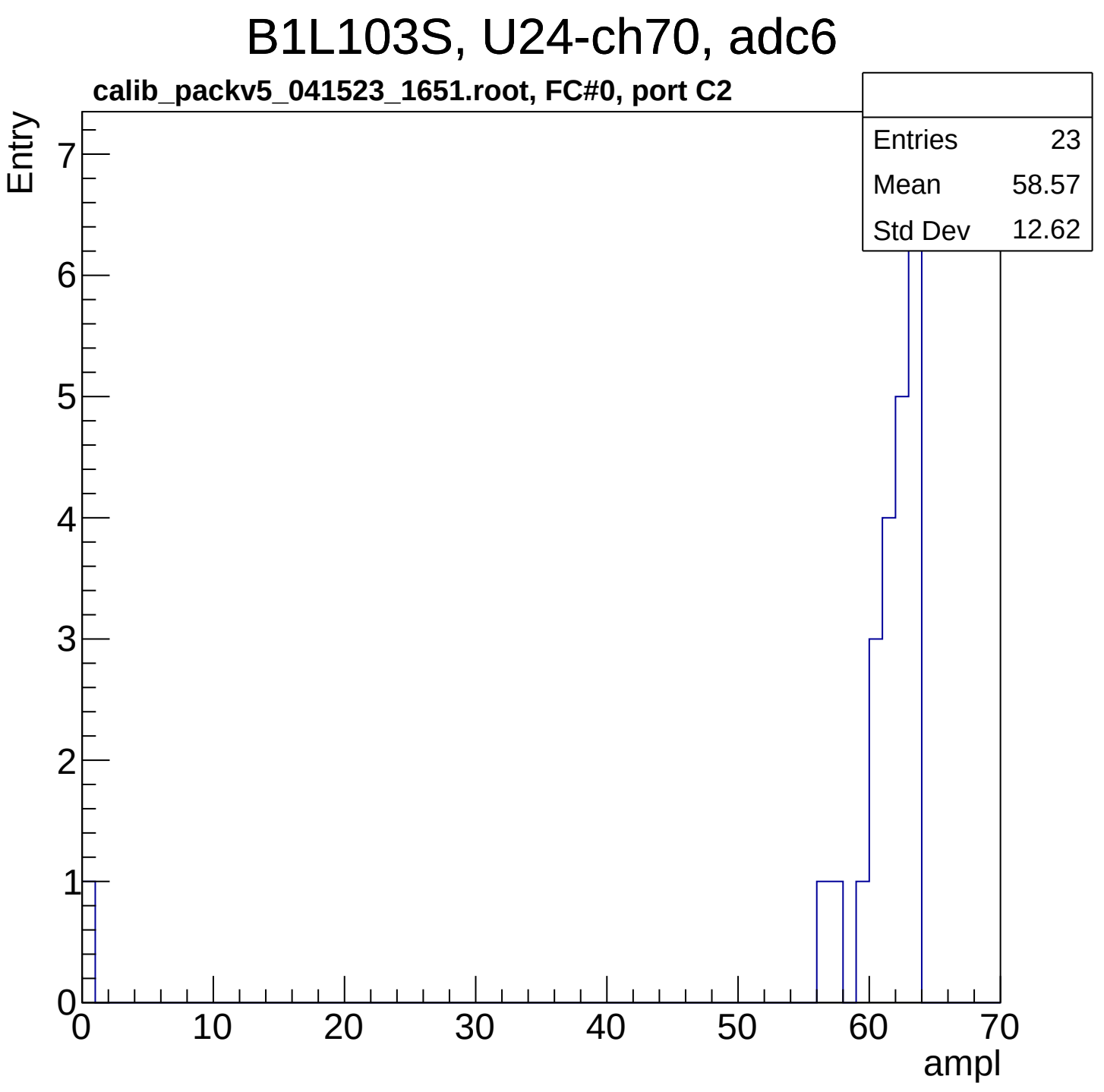
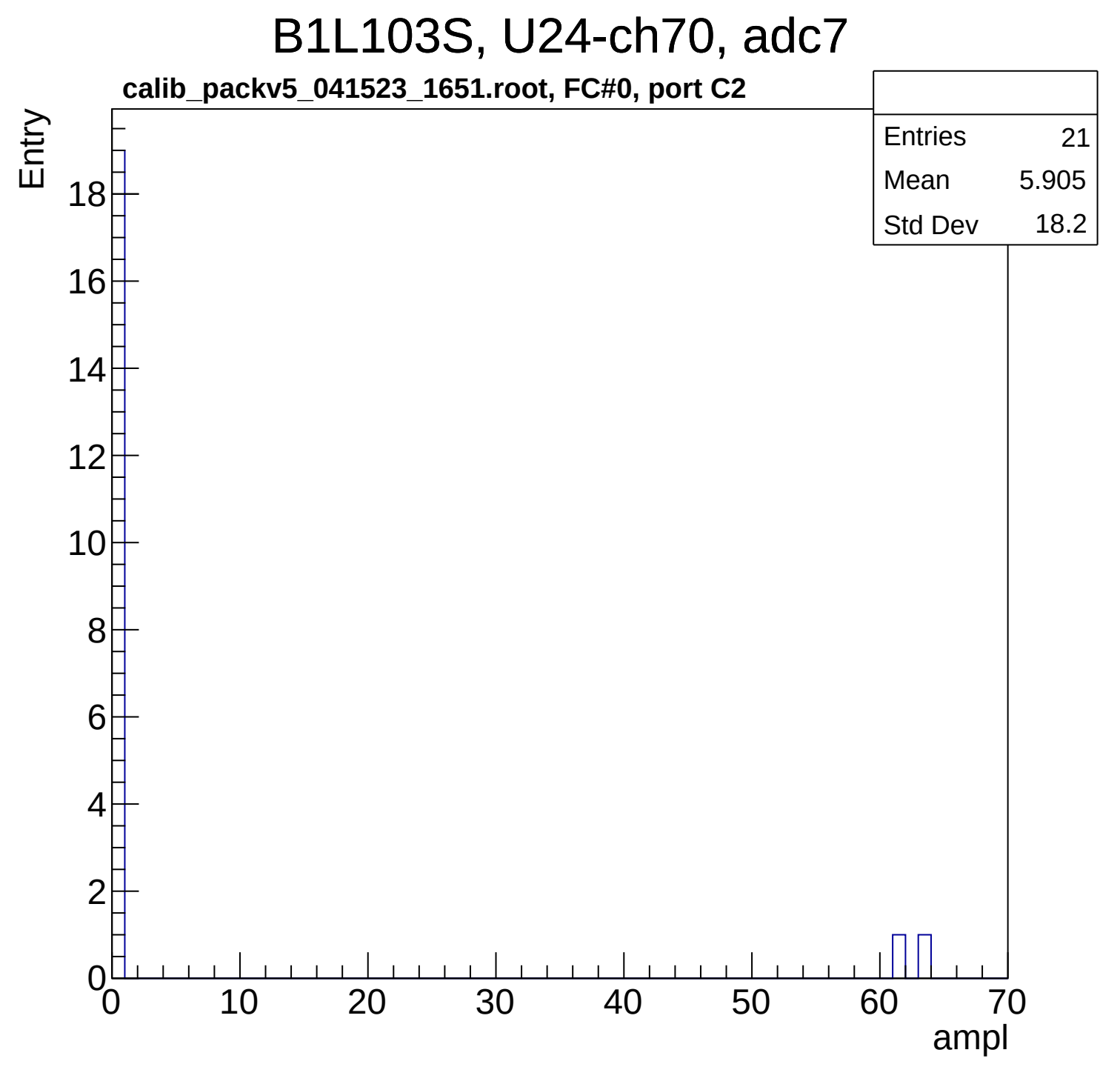
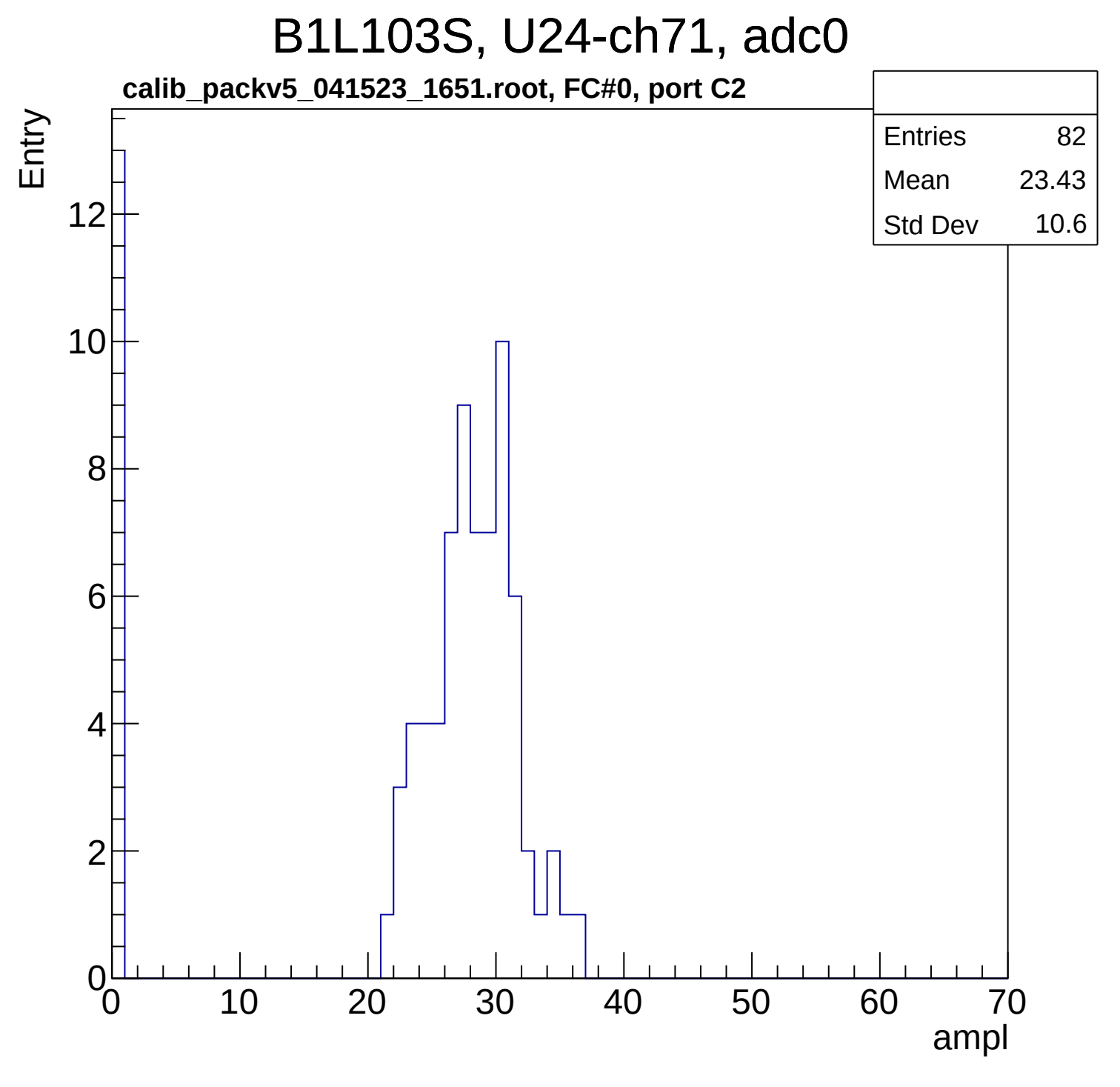
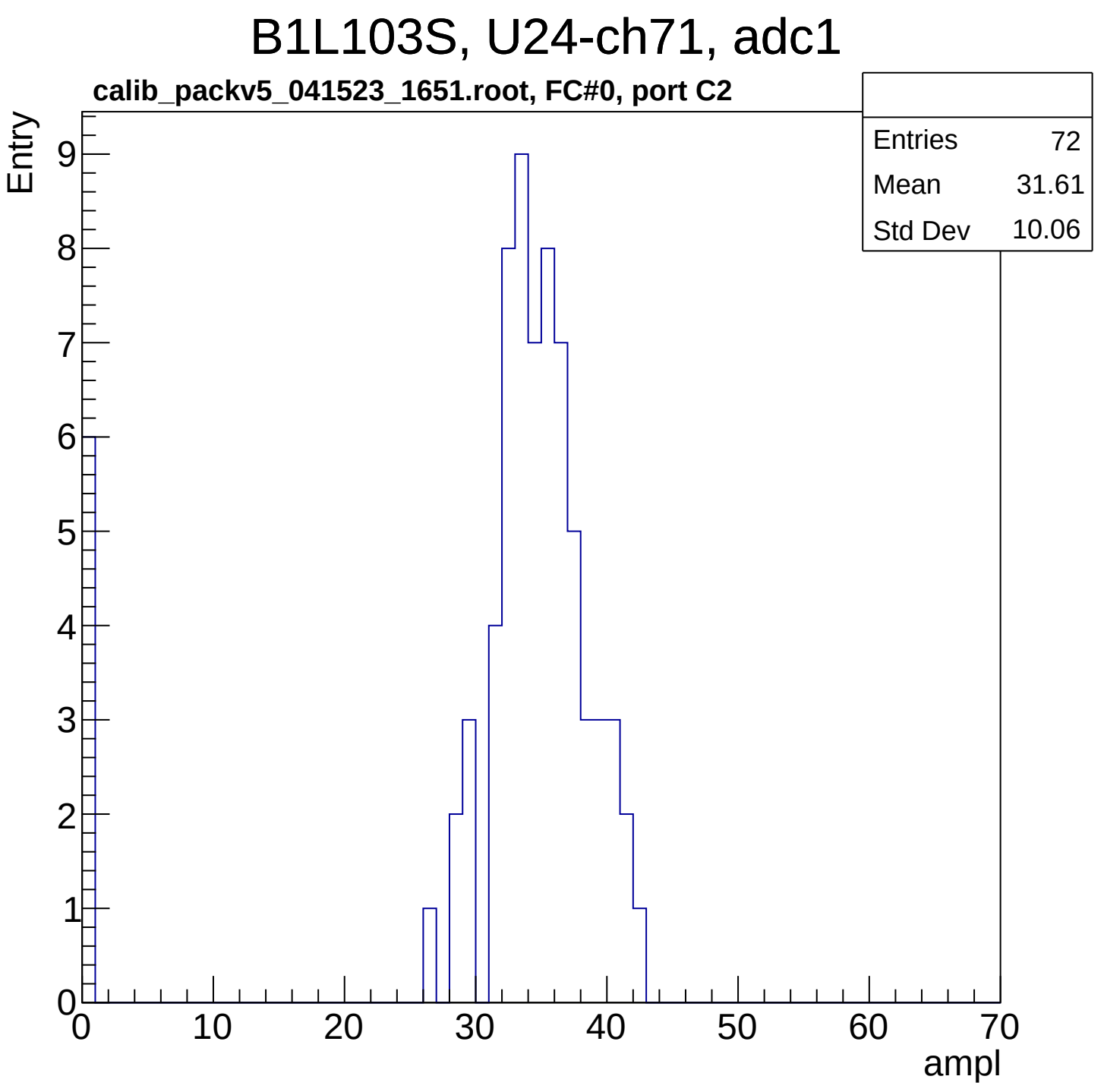
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U24-ch70, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 23
Mean 58.57
Std Dev 12.62
Entry
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch70, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 5.905
Std Dev 18.2
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch71, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 23.43
Std Dev 10.6
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch71, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 31.61
Std Dev 10.06
Entry
ampl
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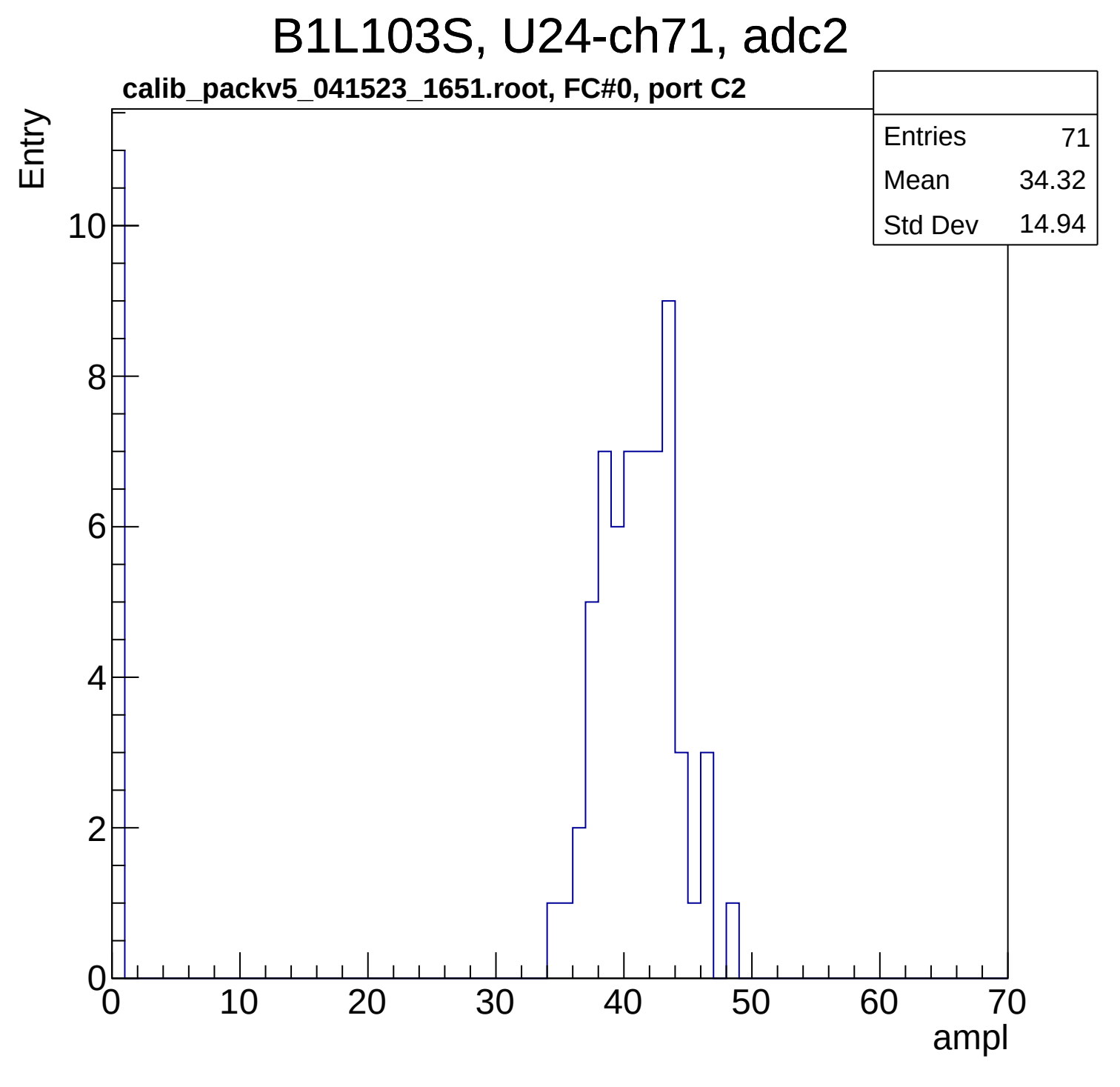
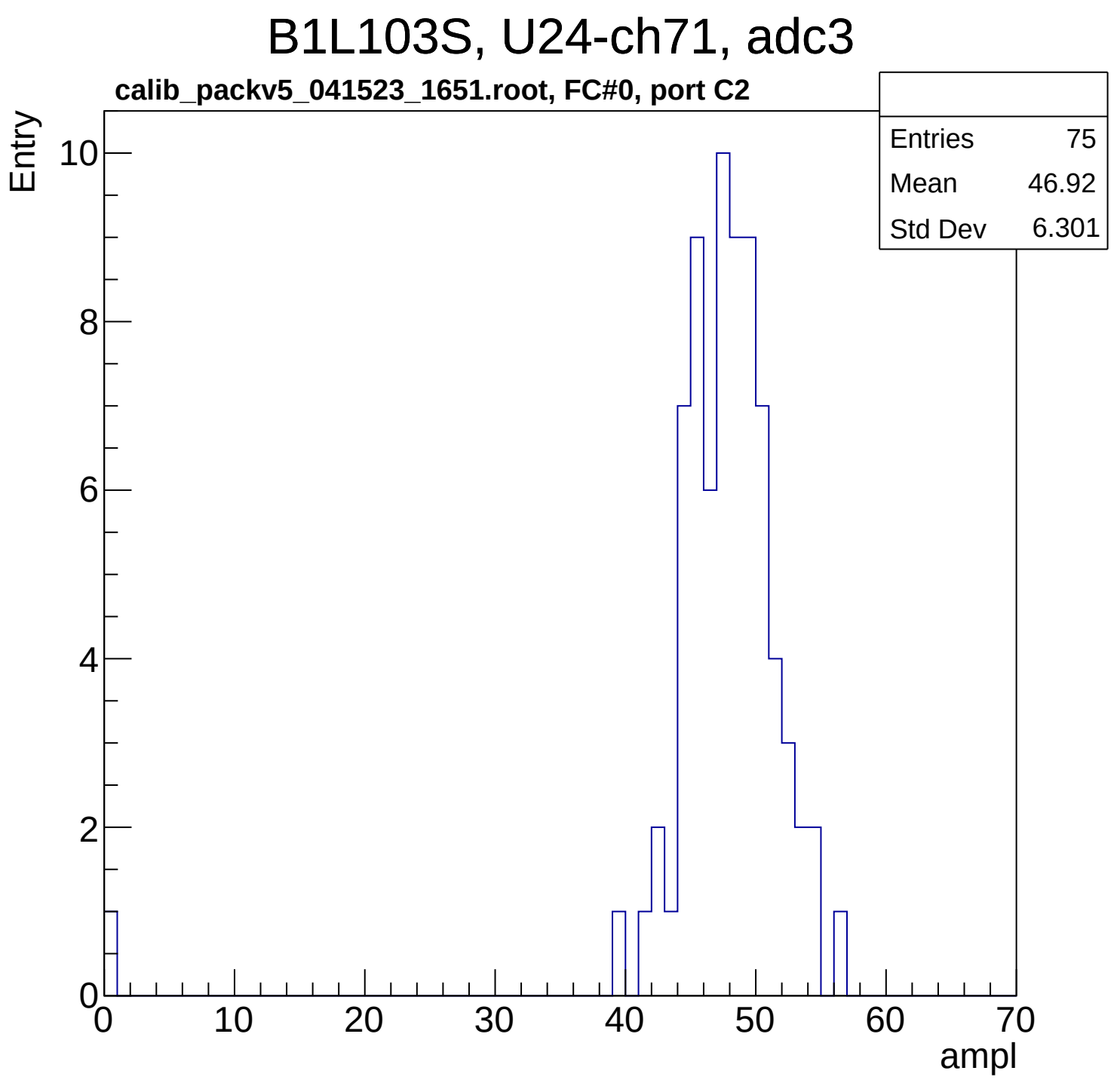
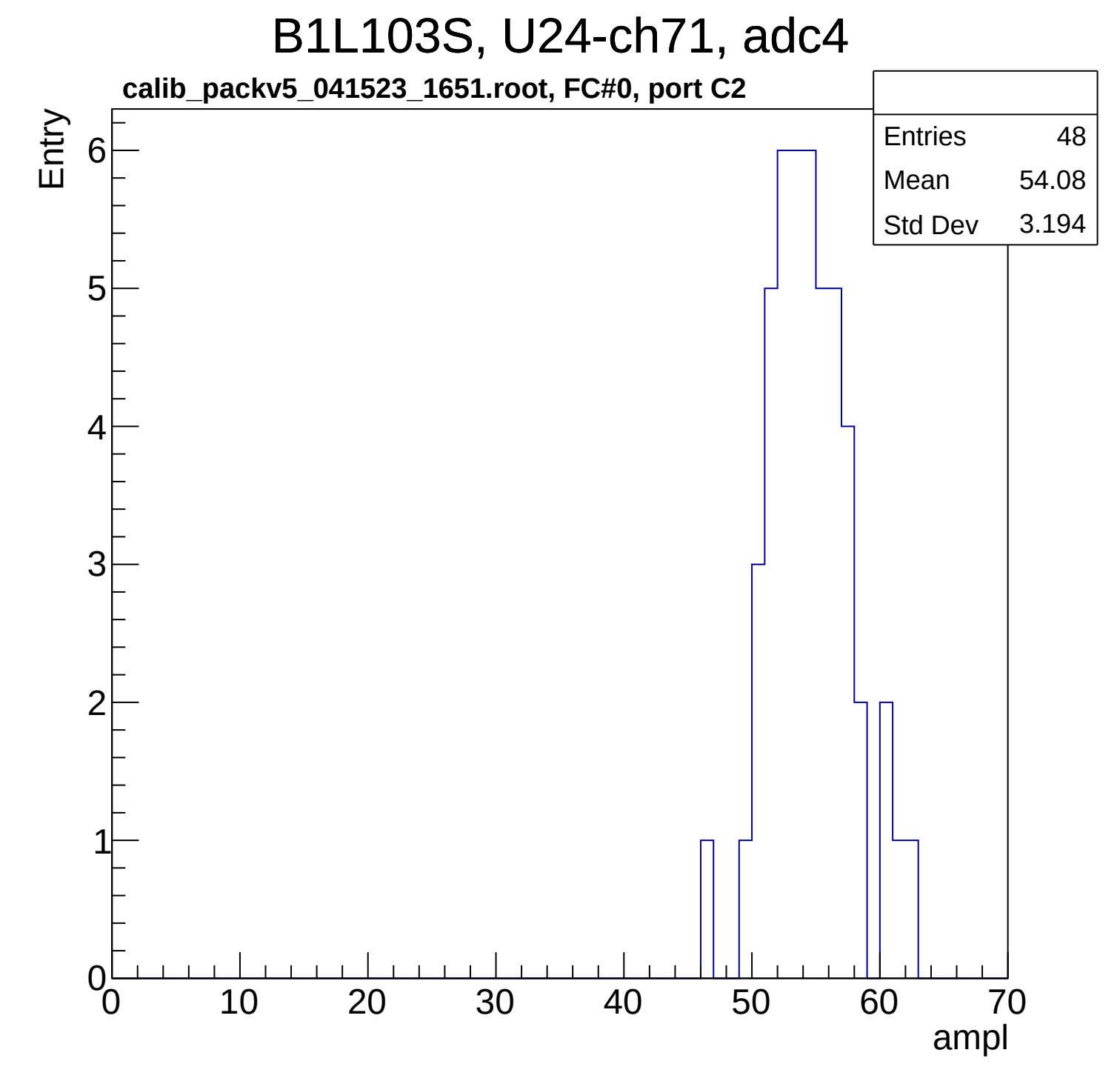
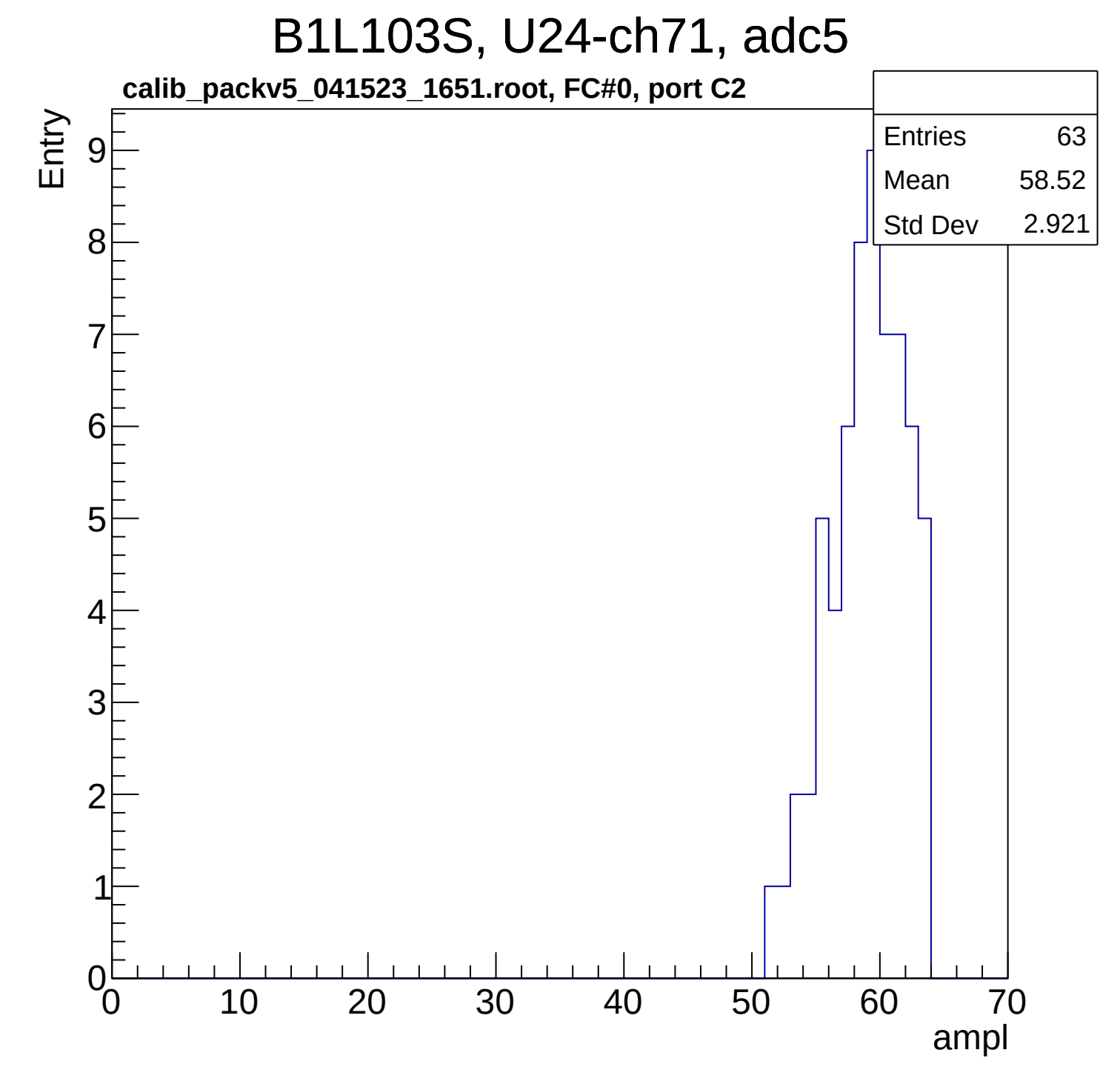
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U24-ch71, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 34.32
Std Dev 14.94
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch71, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 46.92
Std Dev 6.301
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U24-ch71, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 54.08
Std Dev 3.194
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U24-ch71, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 58.52
Std Dev 2.921
Entry
ampl
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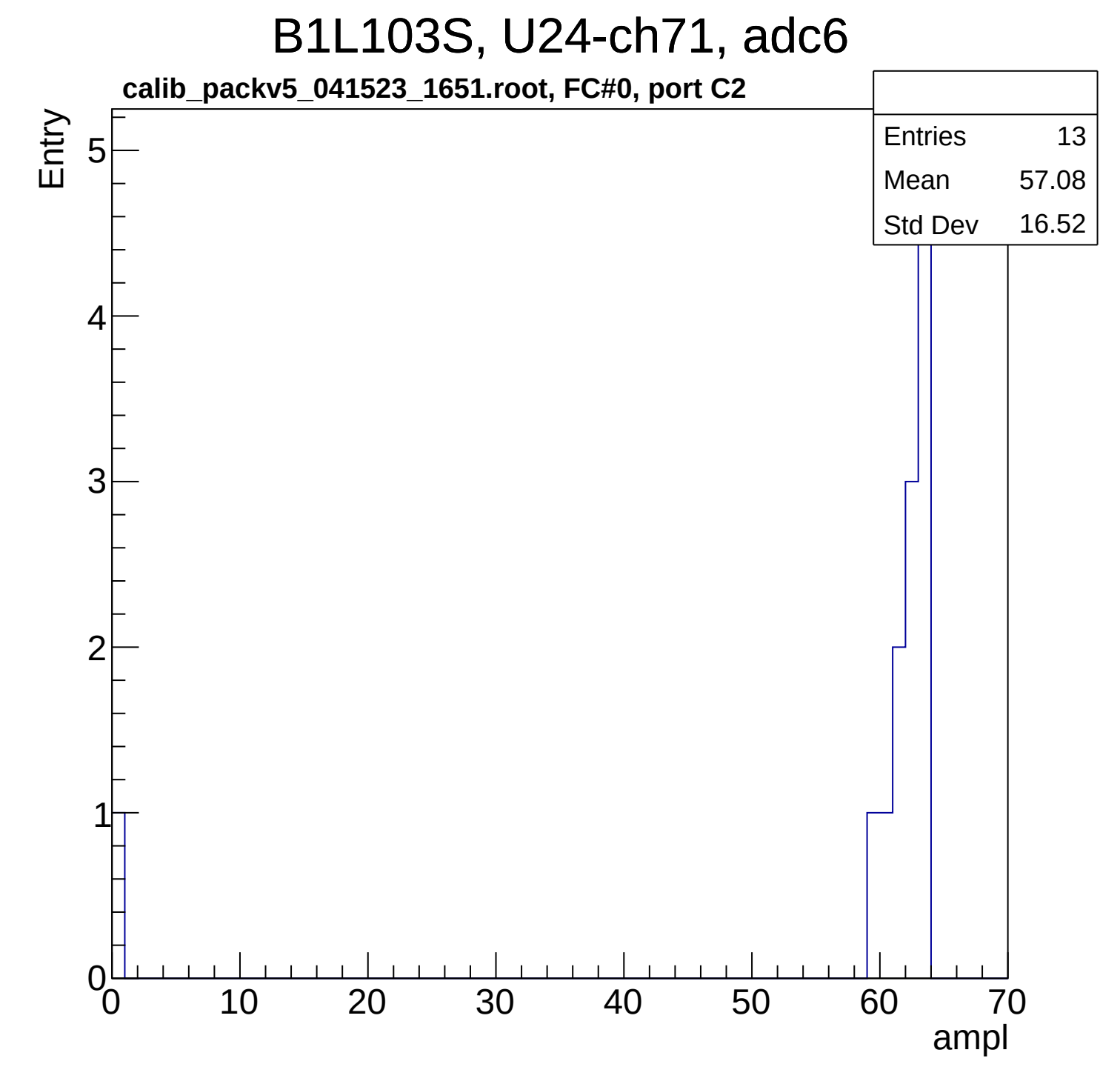
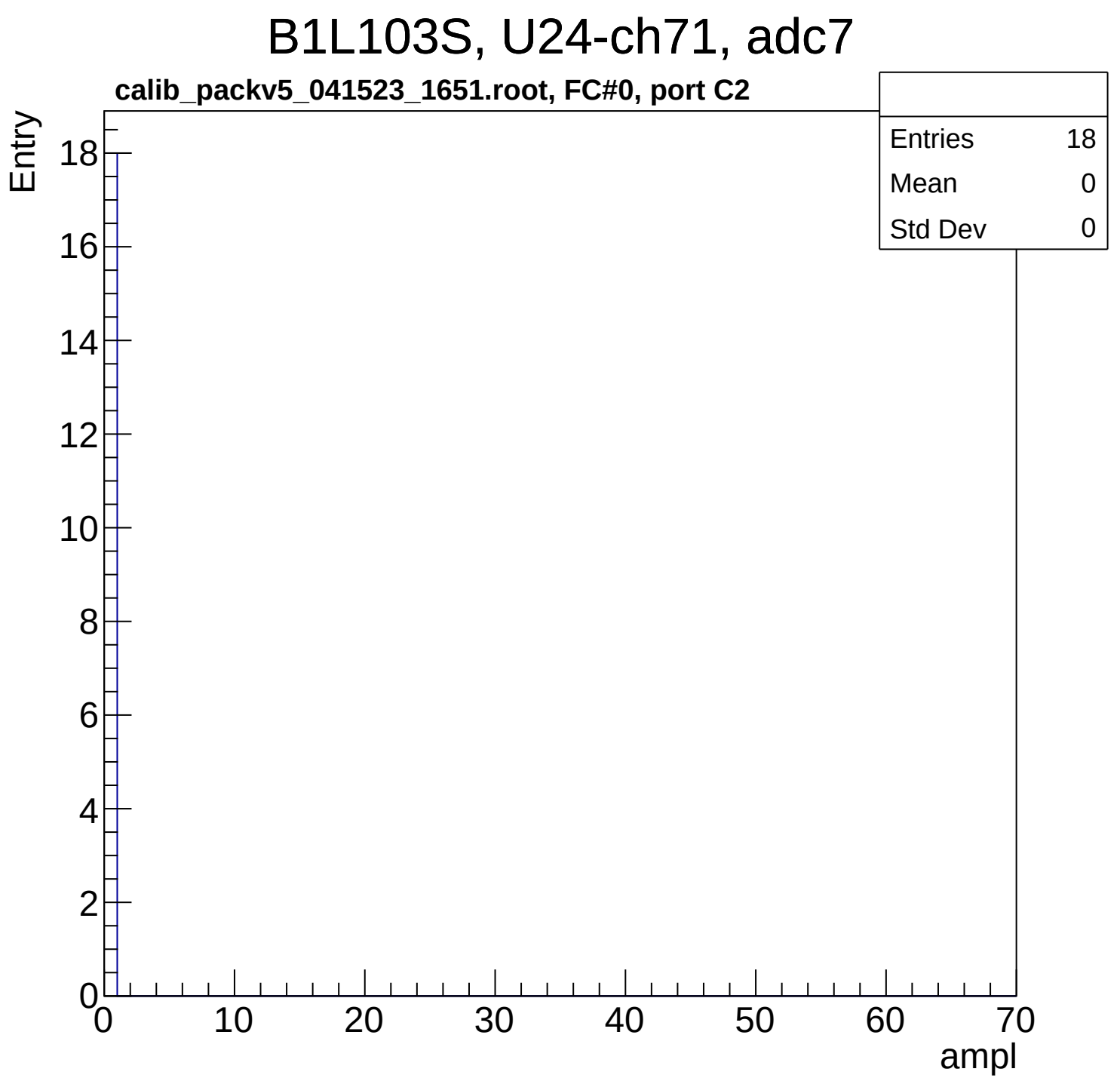
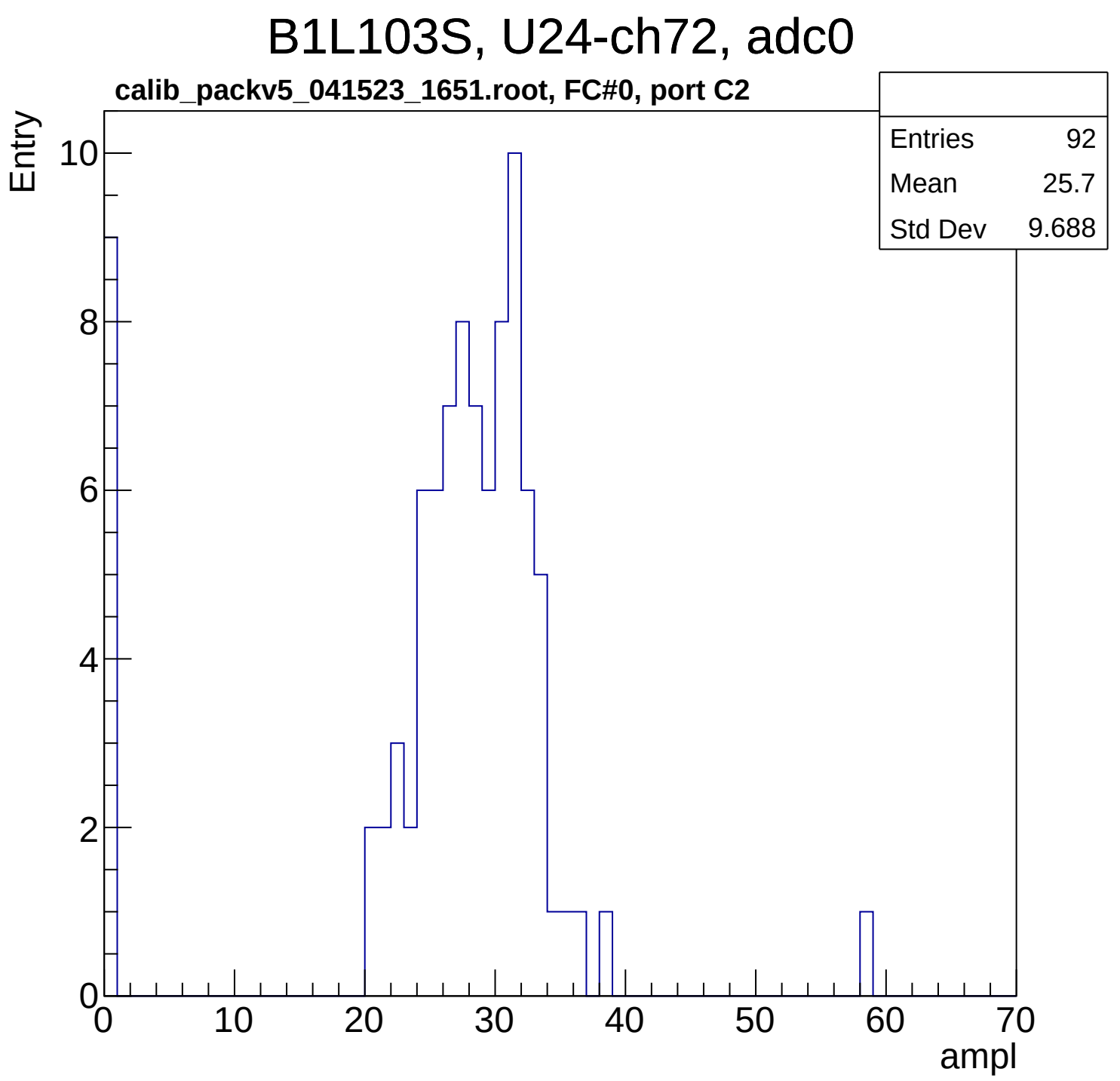
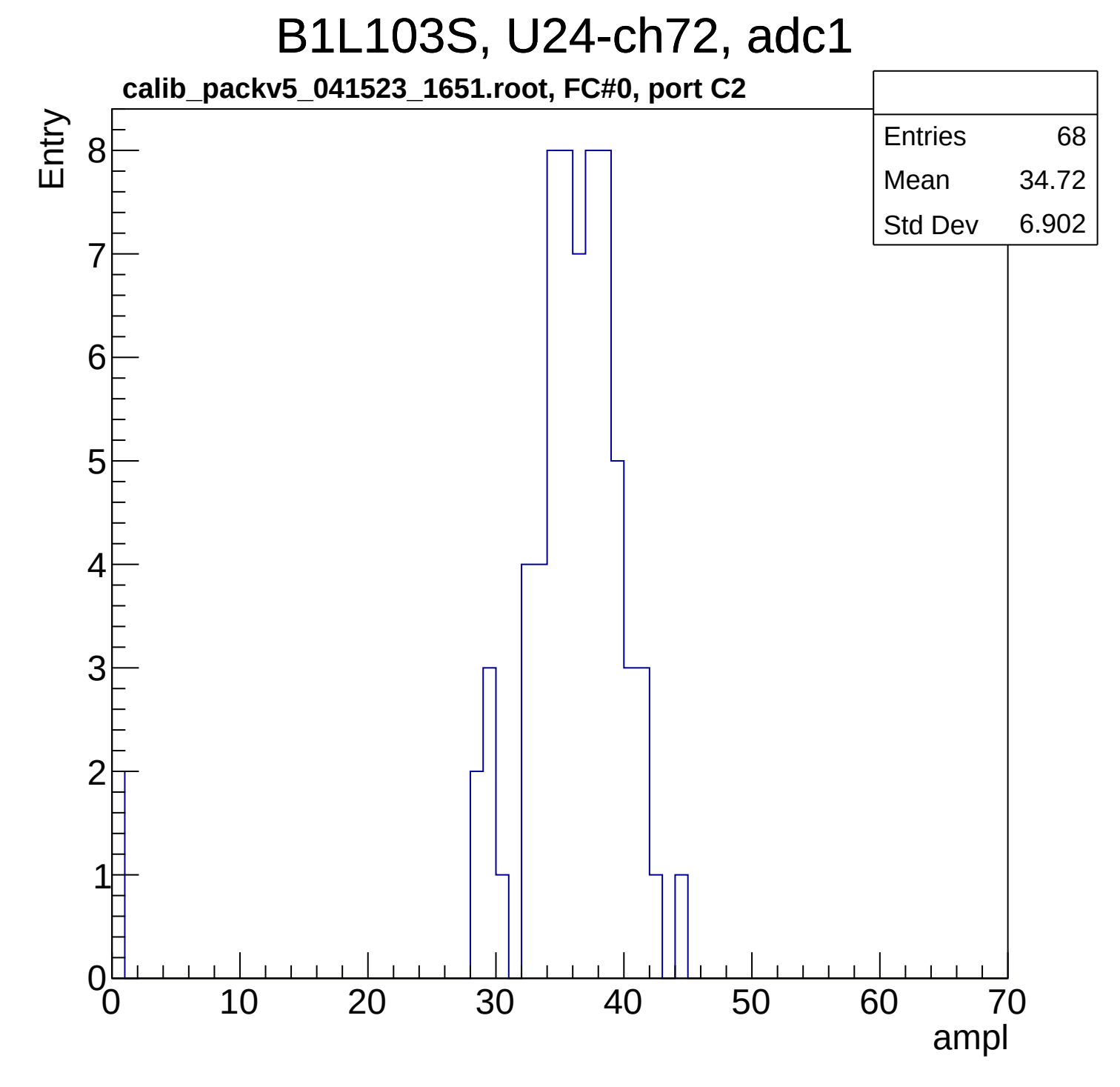
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U24-ch71, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 13
Mean 57.08
Std Dev 16.52
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch71, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch72, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 92
Mean 25.7
Std Dev 9.688
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U24-ch72, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 34.72
Std Dev 6.902
Entry
ampl
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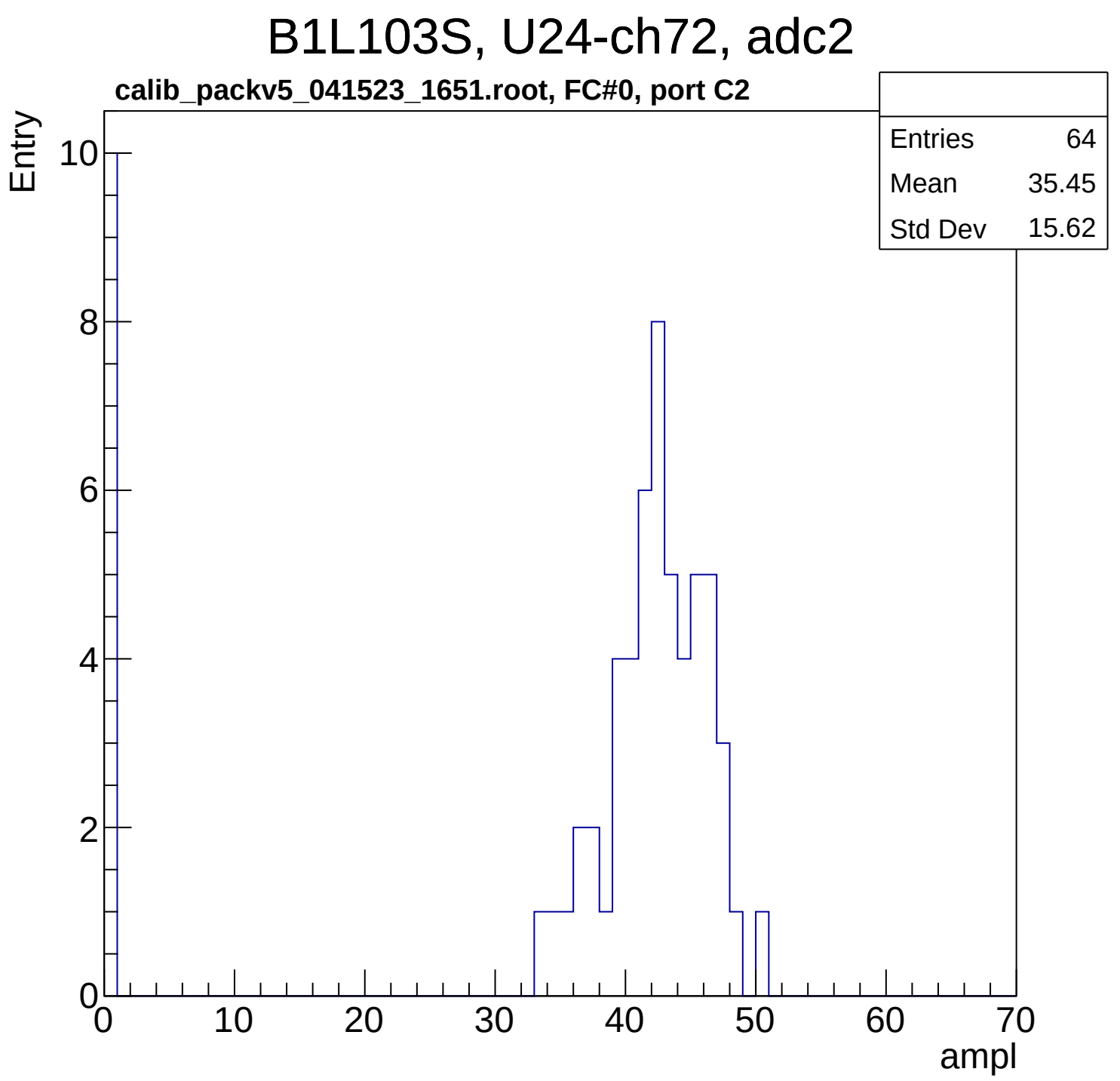
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U24-ch72, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 35.45
Std Dev 15.62
Entry
ampl
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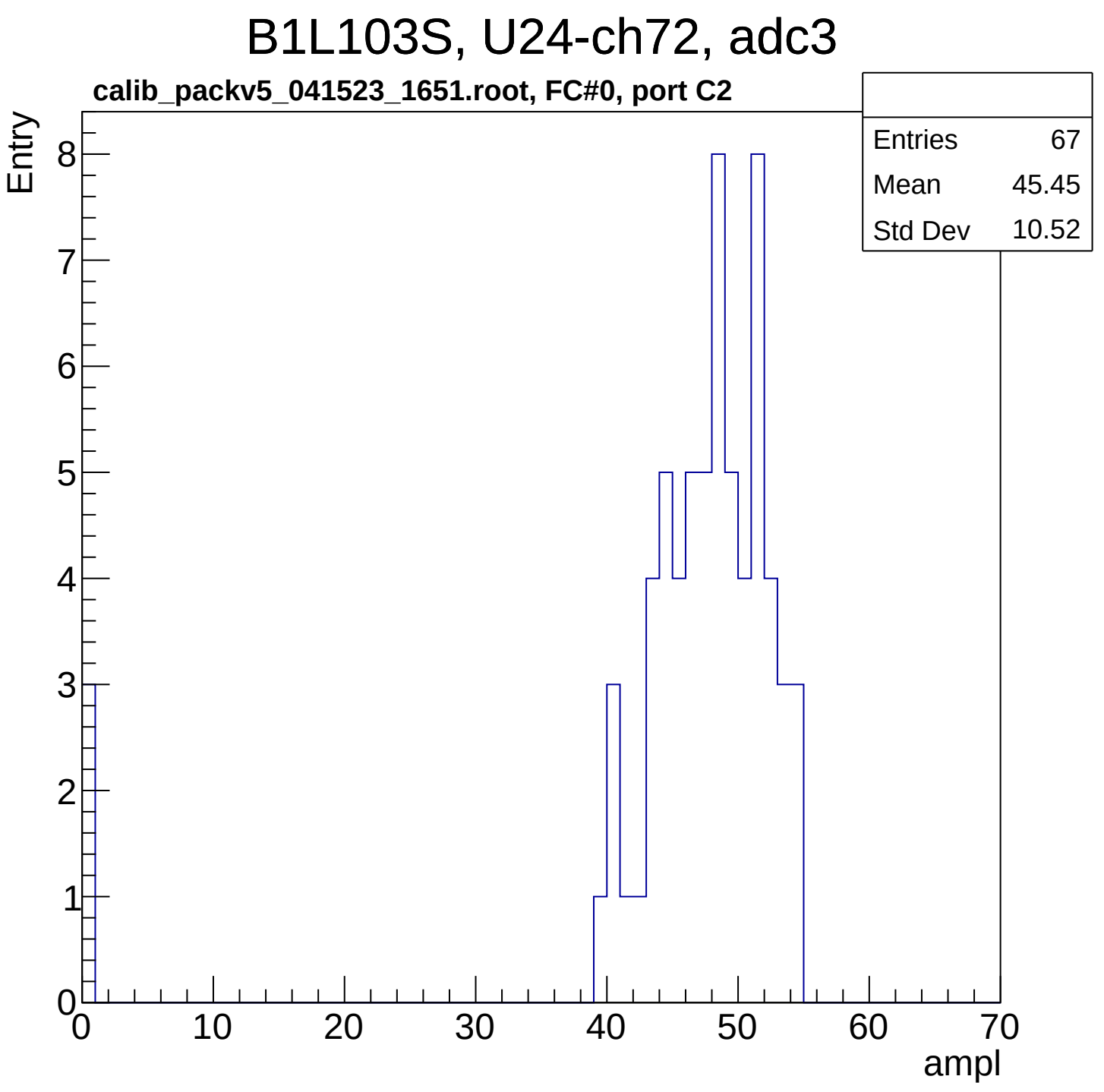
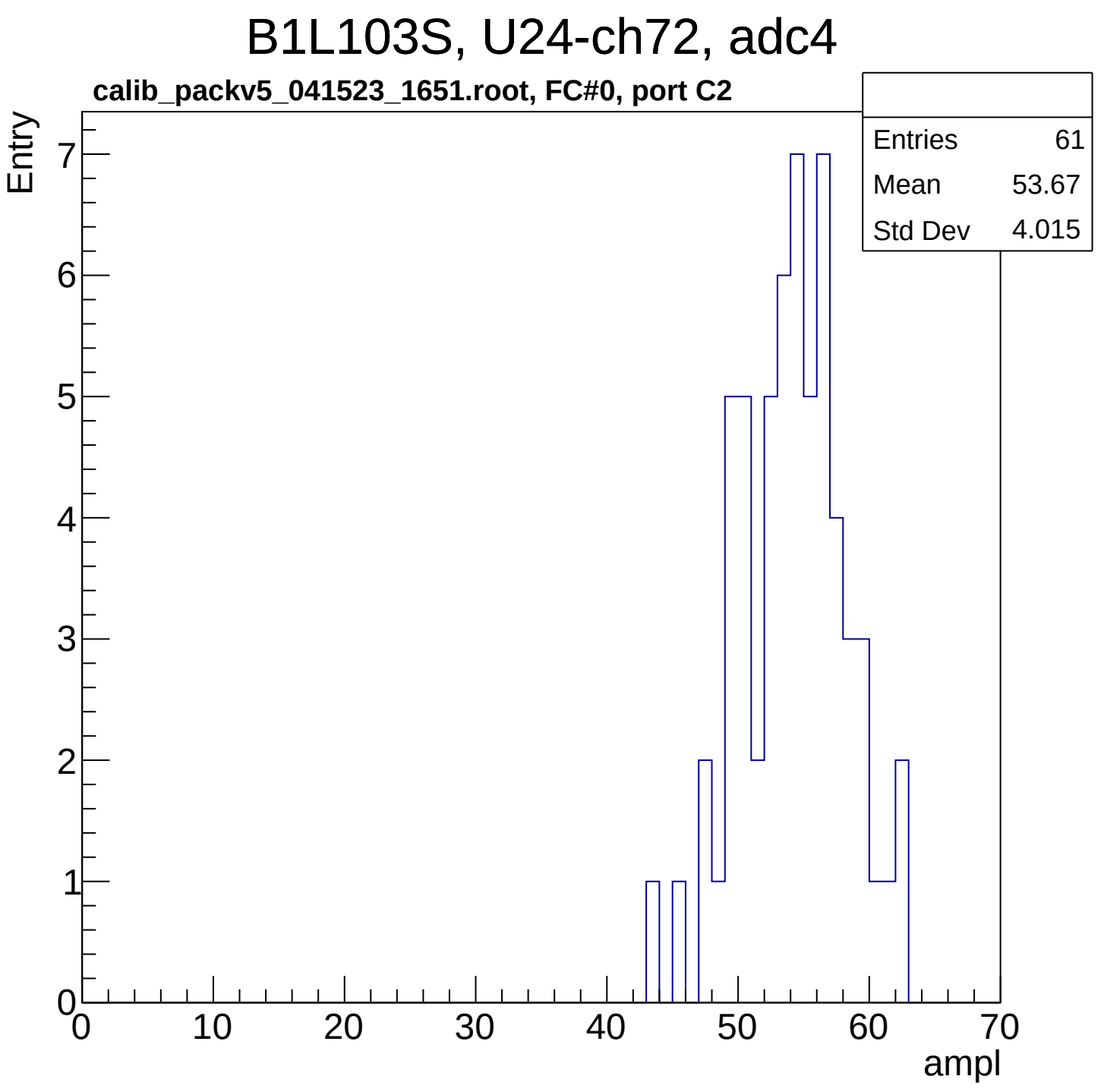
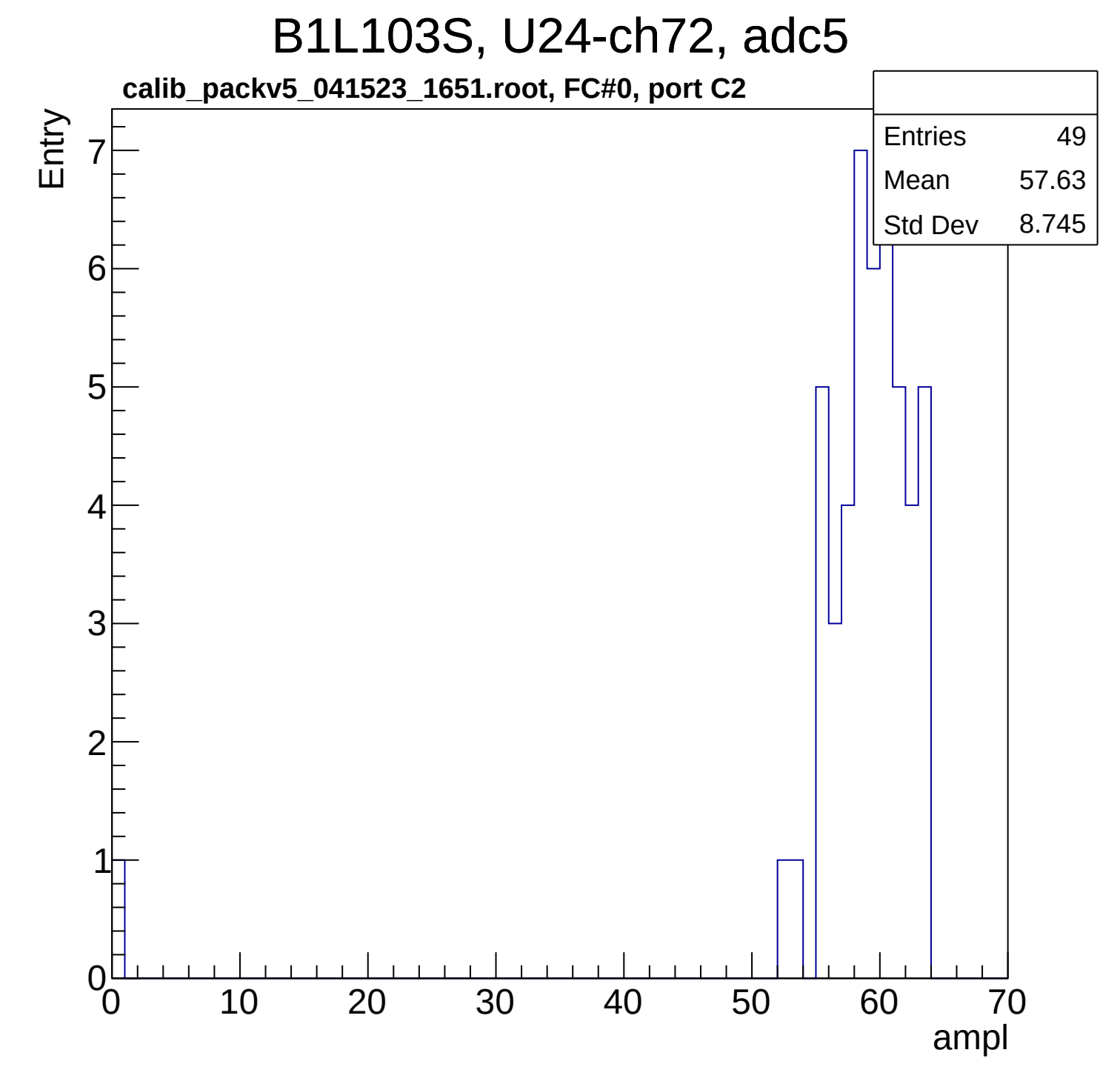
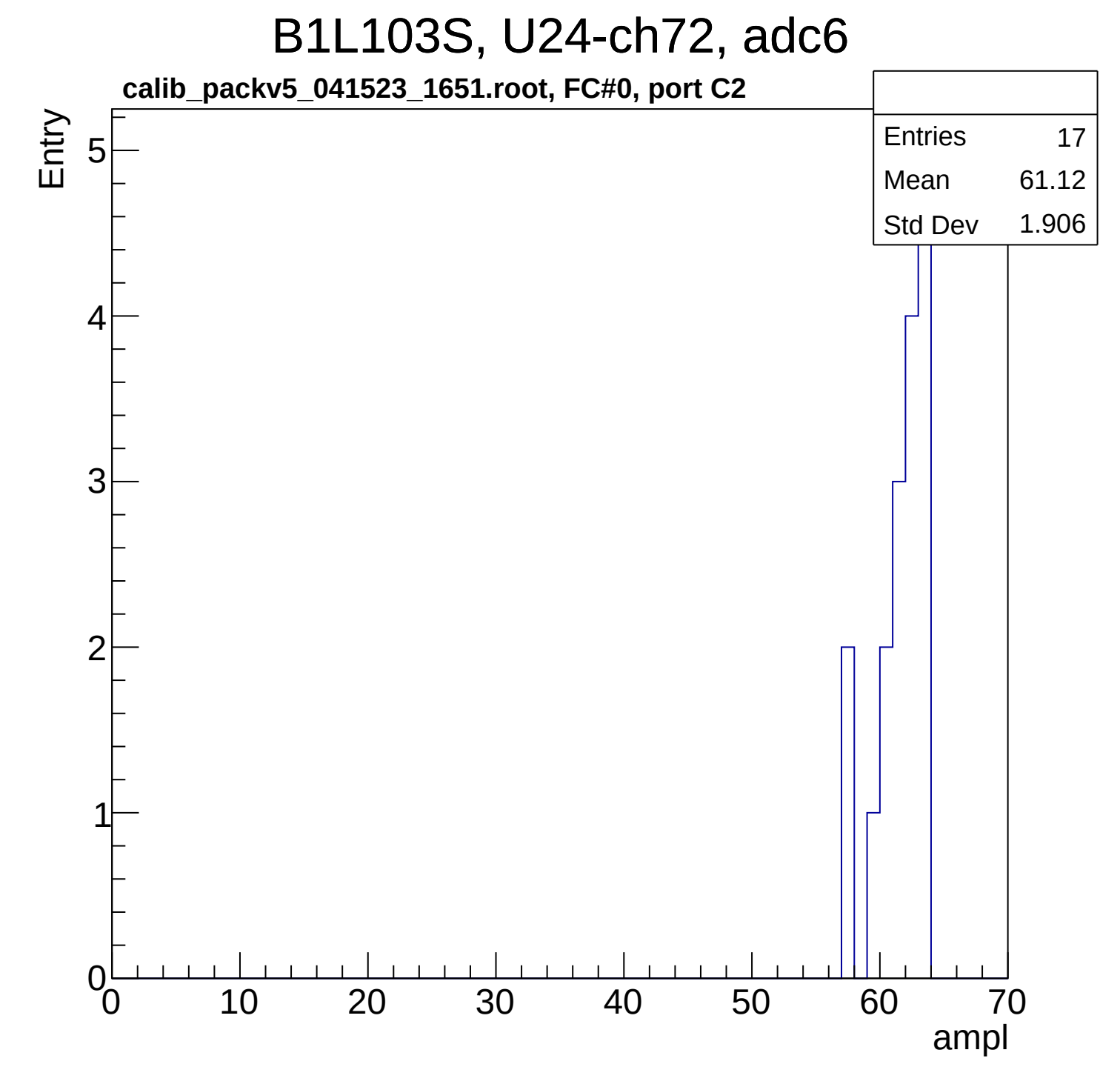
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U24-ch72, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 45.45
Std Dev 10.52
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U24-ch72, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 53.67
Std Dev 4.015
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U24-ch72, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 57.63
Std Dev 8.745
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U24-ch72, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 17
Mean 61.12
Std Dev 1.906
Entry
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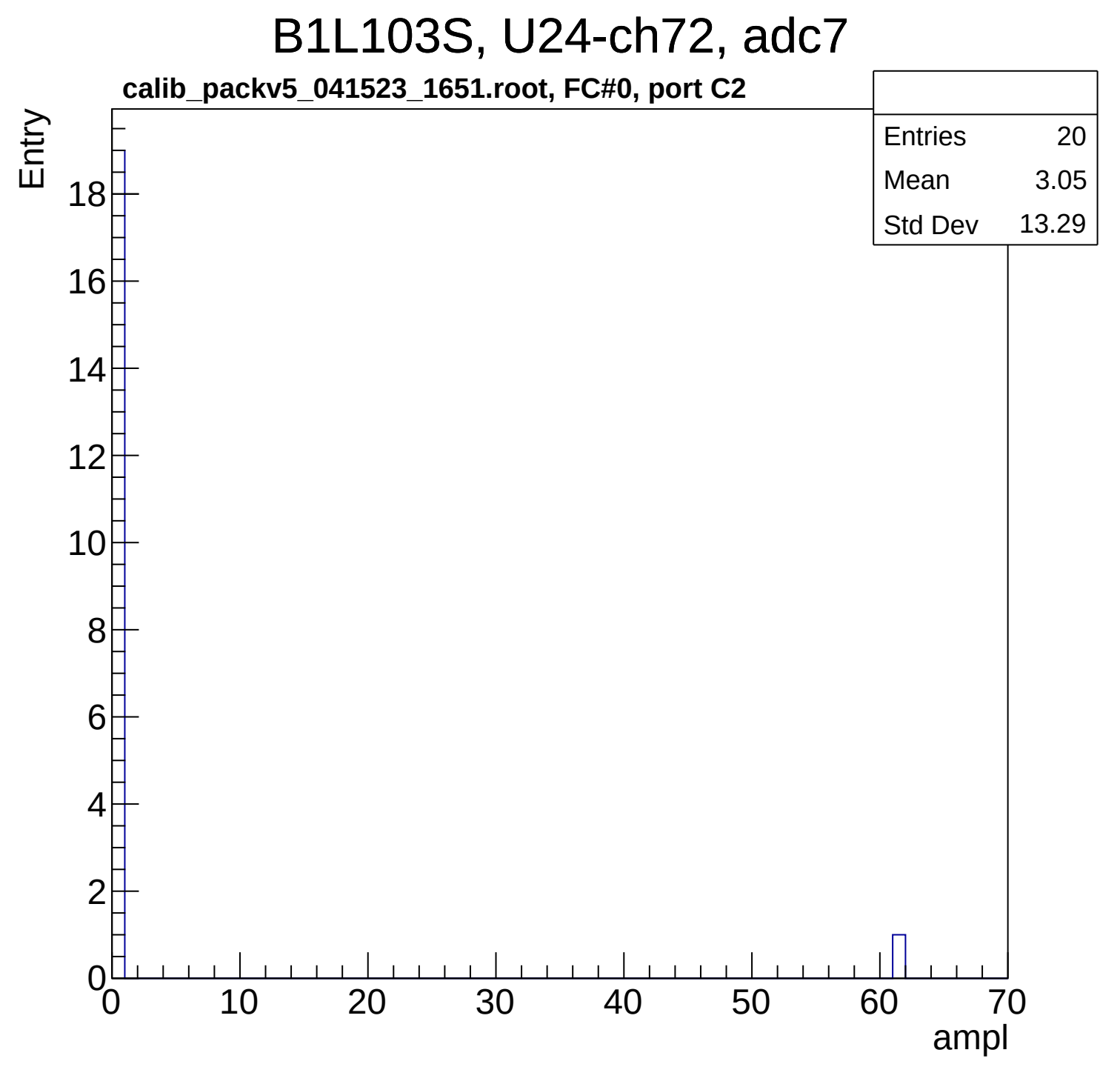
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch72, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.05
Std Dev 13.29
Entry
0
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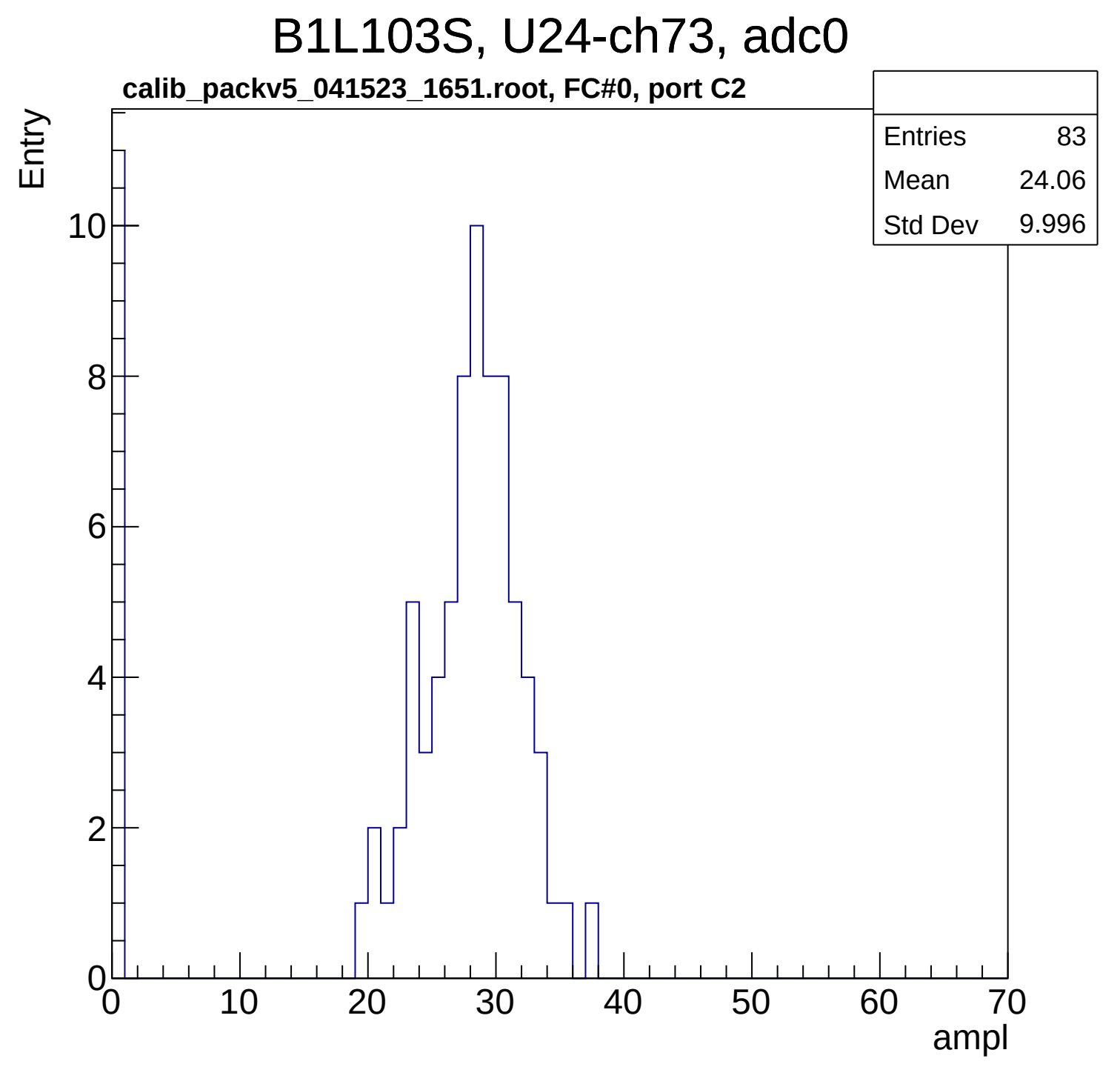
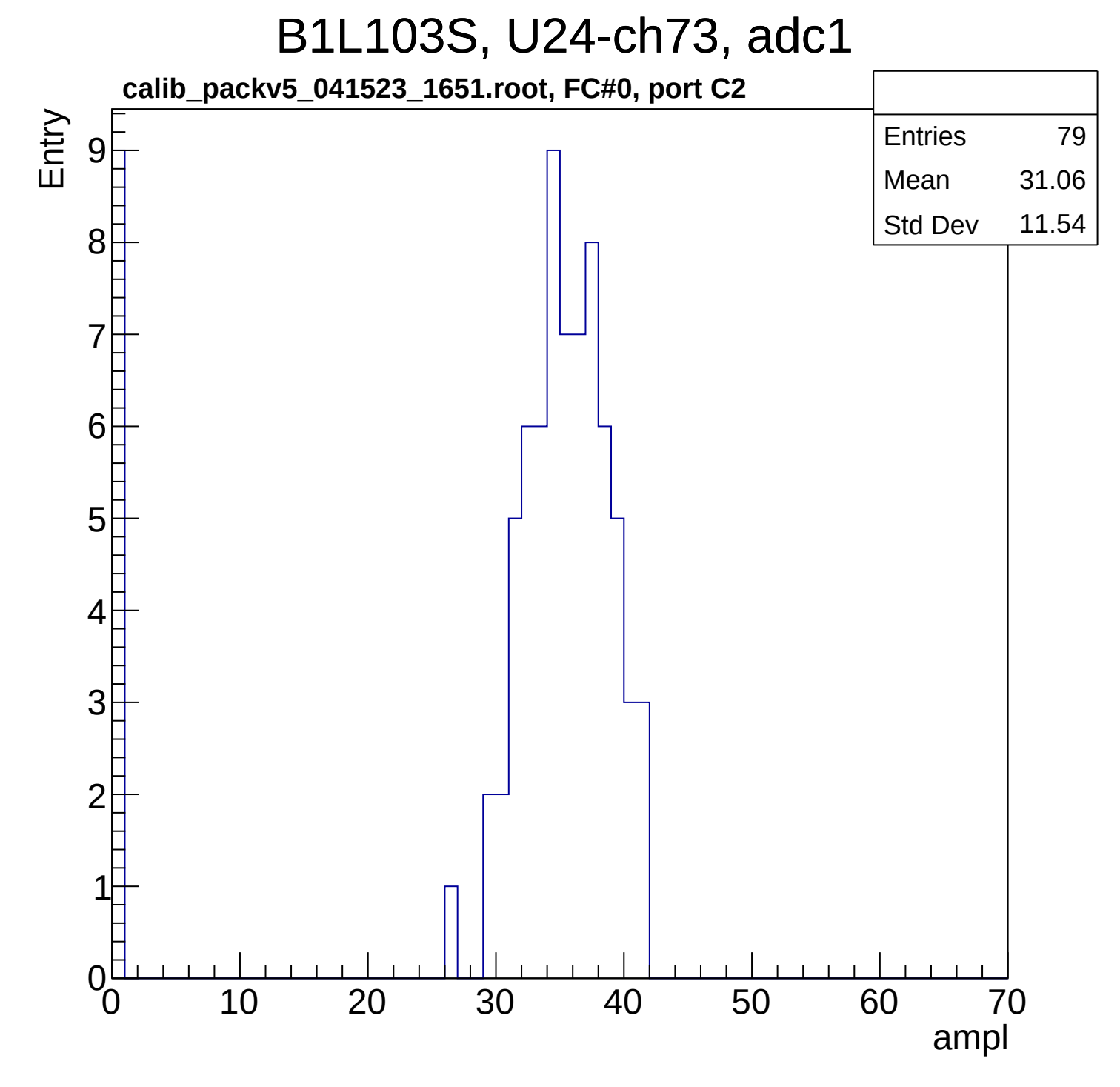
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch73, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 24.06
Std Dev 9.996
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U24-ch73, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 31.06
Std Dev 11.54
Entry
ampl
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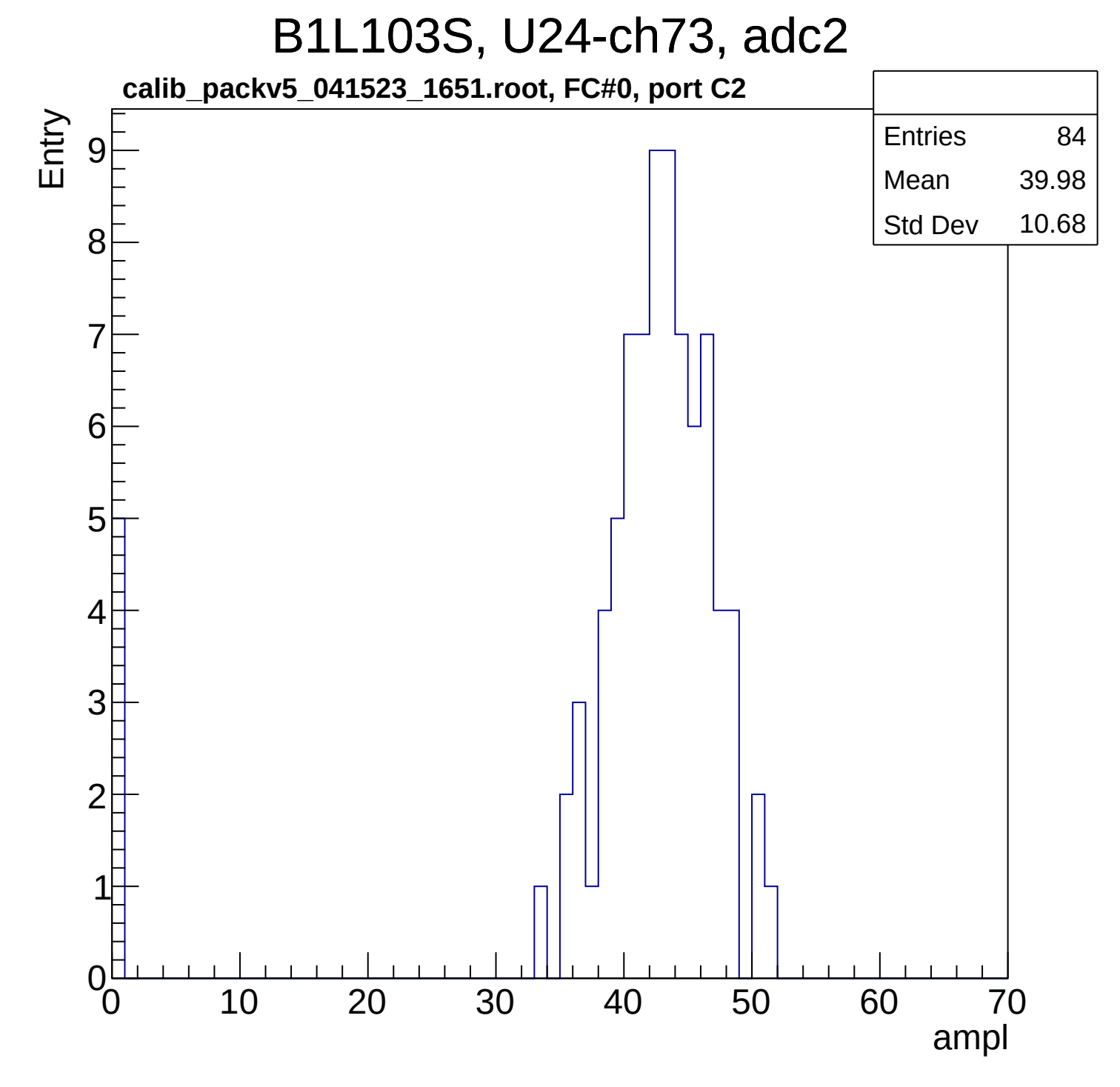
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U24-ch73, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 39.98
Std Dev 10.68
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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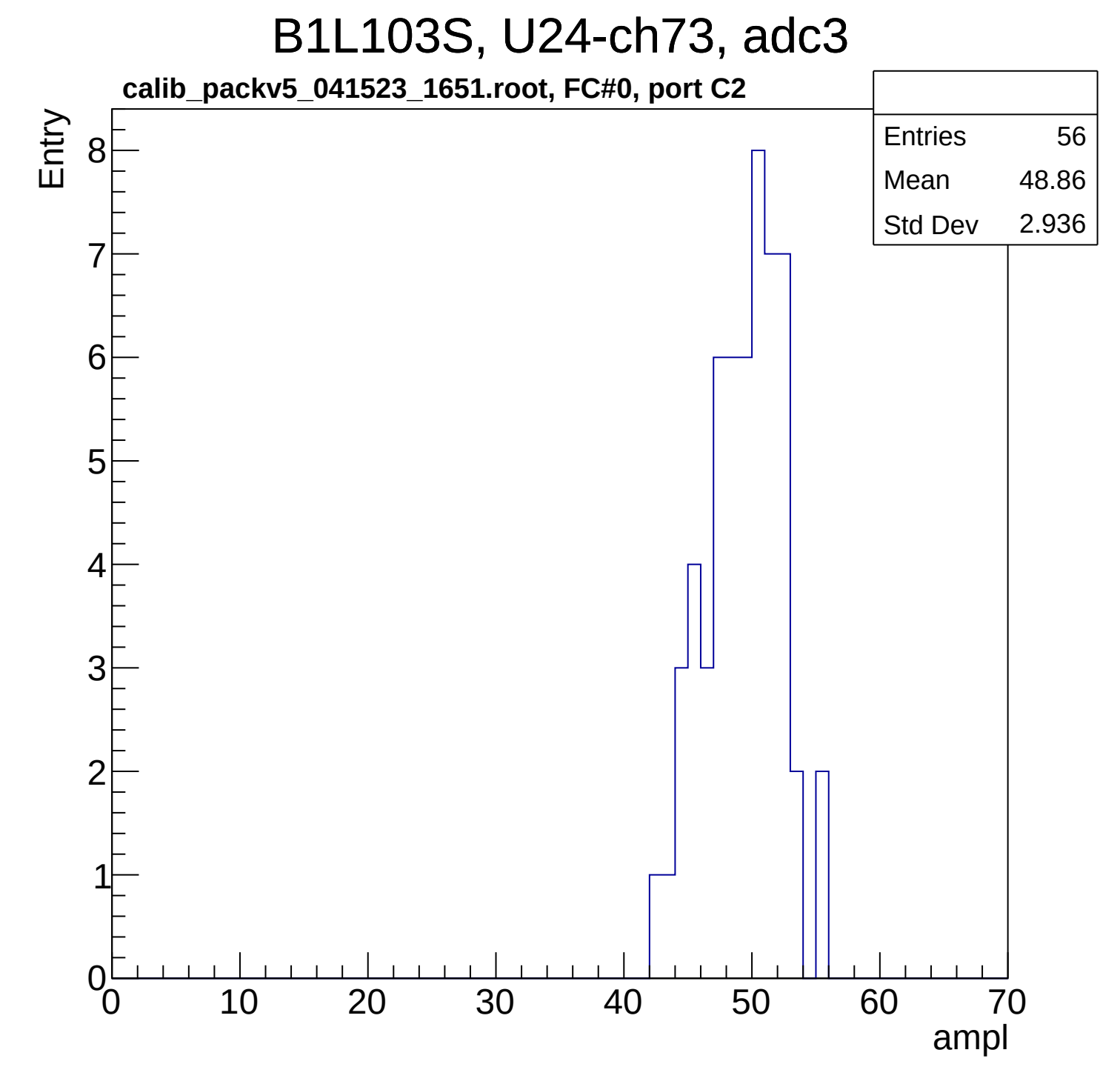
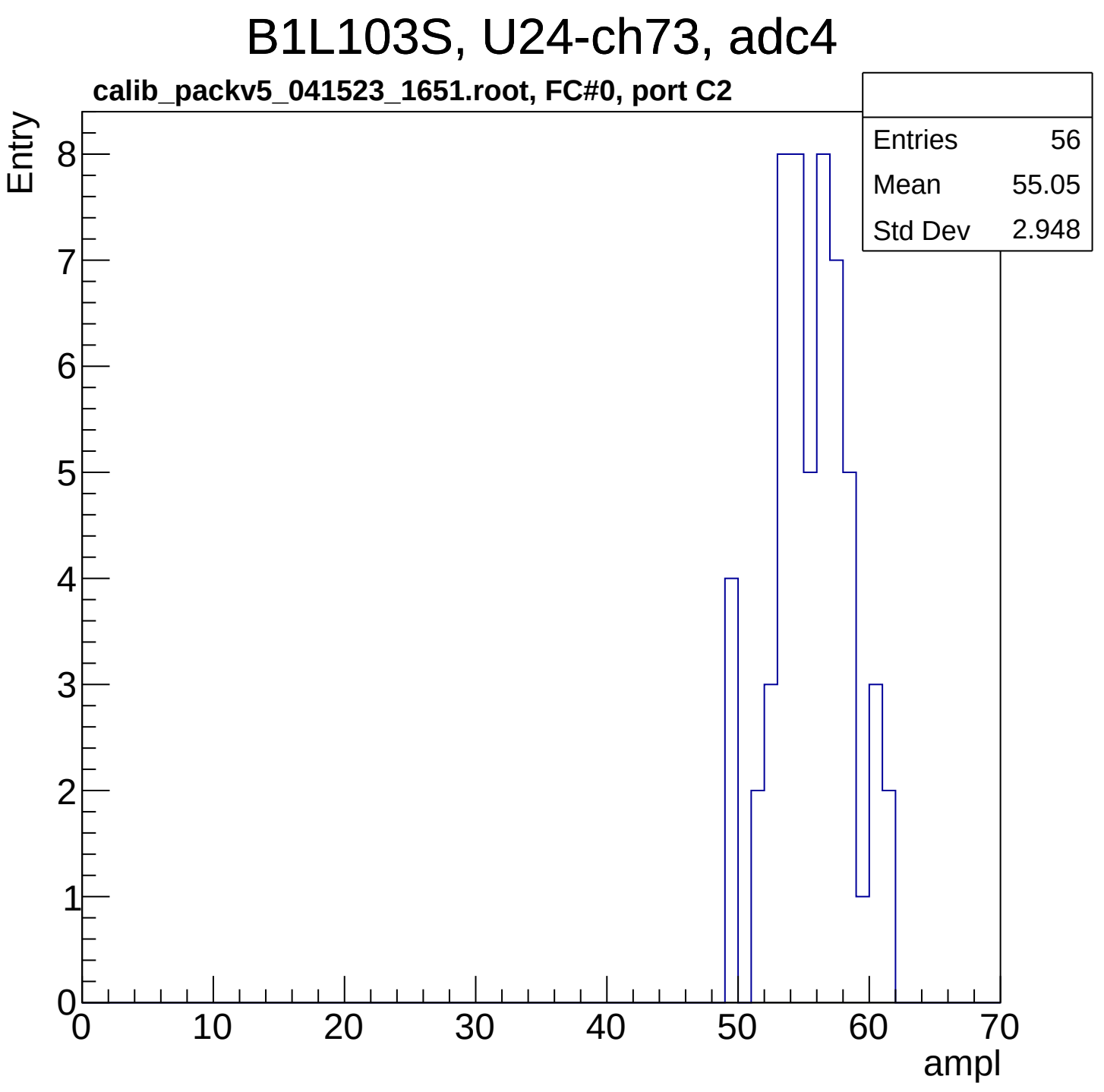
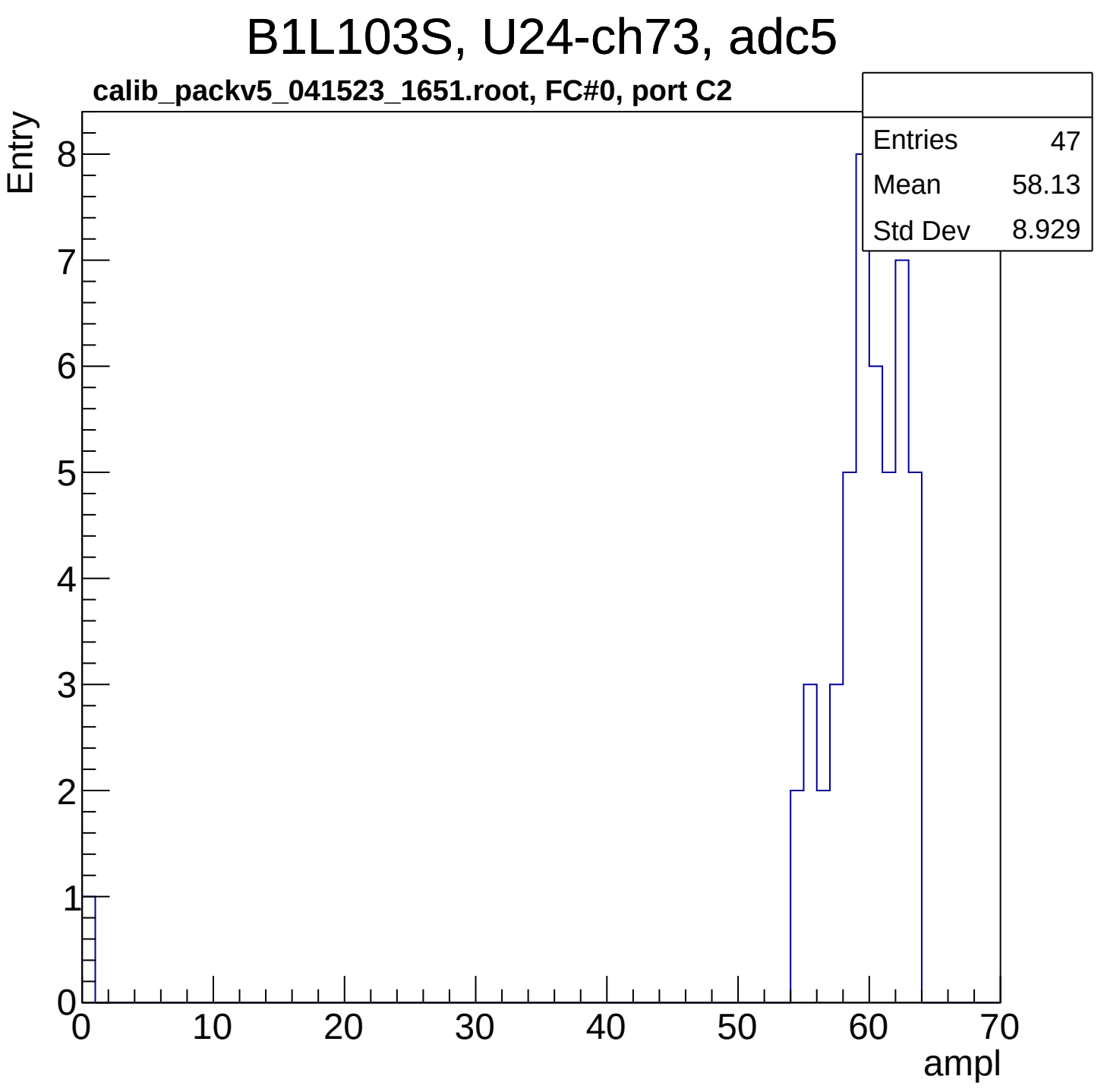

B1L103S, U24-ch73, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 48.86
Std Dev 2.936
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U24-ch73, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 55.05
Std Dev 2.948
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U24-ch73, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 58.13
Std Dev 8.929
Entry
ampl
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2
3
4
5
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7
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0
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40
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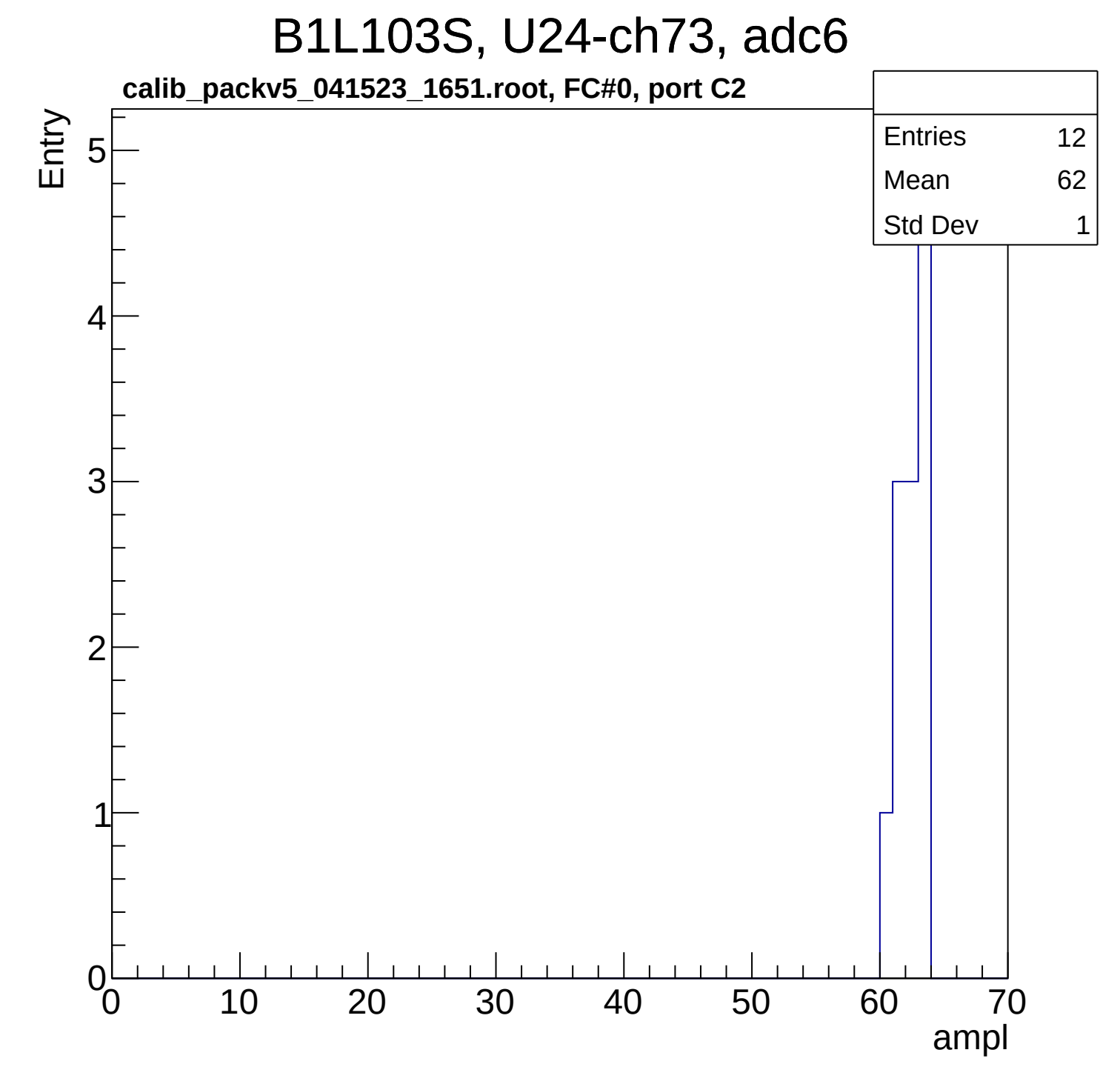
B1L103S, U24-ch73, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 62
Std Dev 1
Entry
0
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2
3
4
5
0
10
20
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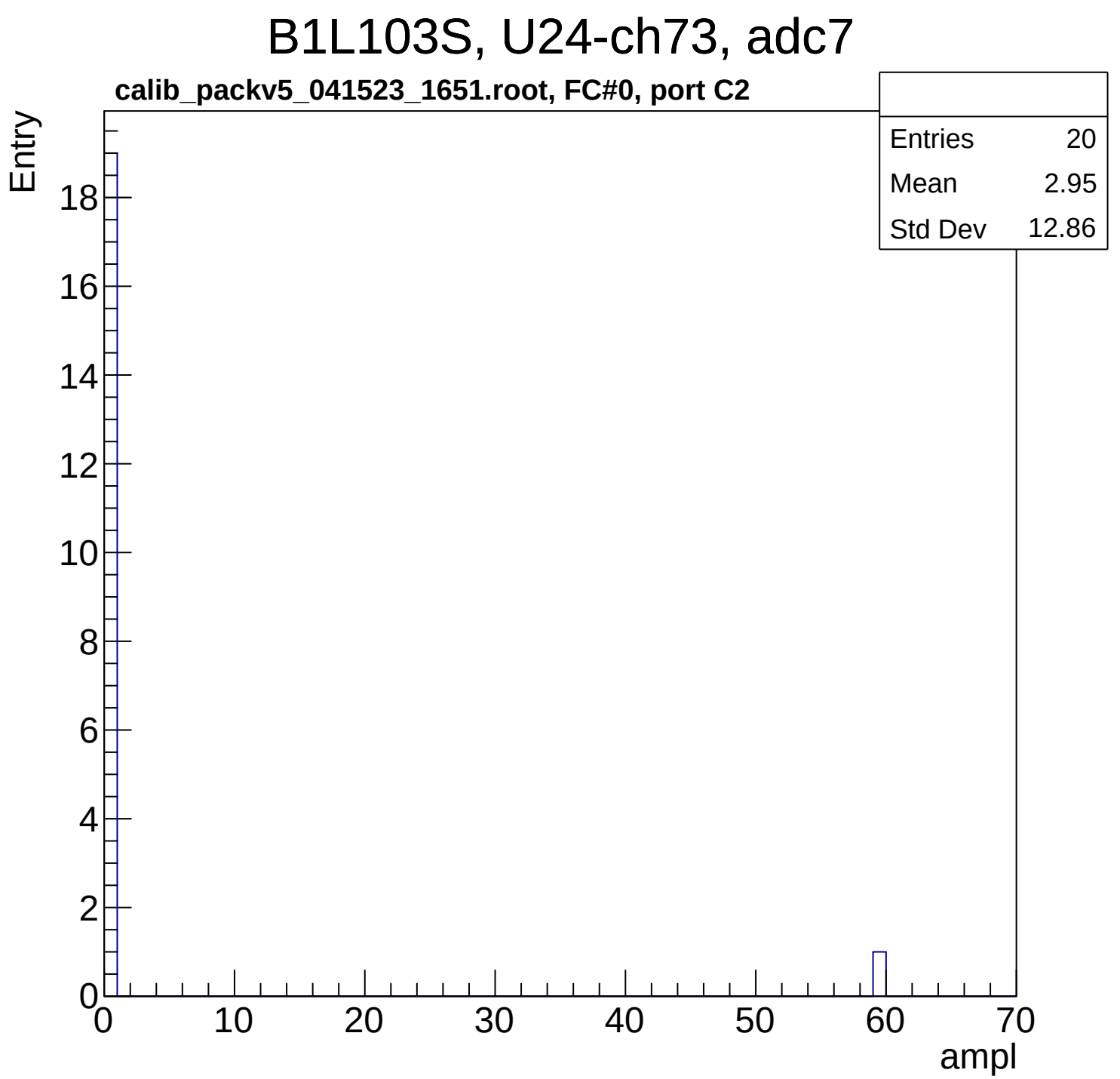
40
50
60
70
ampl


B1L103S, U24-ch73, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 2.95
Std Dev 12.86
Entry
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8
10
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14
16
18
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10
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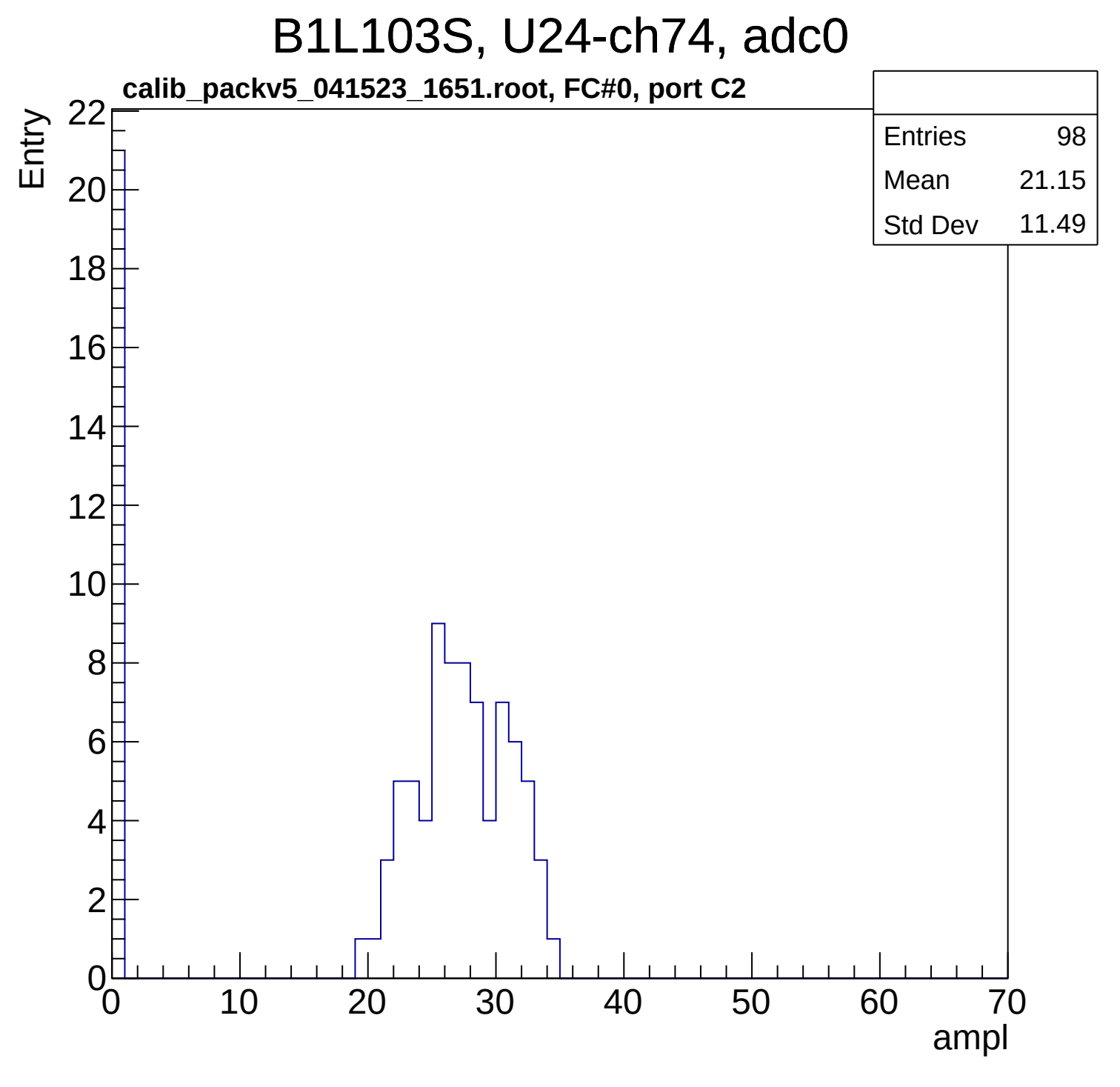
50
60
70
ampl


B1L103S, U24-ch74, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 98
Mean 21.15
Std Dev 11.49
Entry
ampl
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8
10
12
14
16
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0
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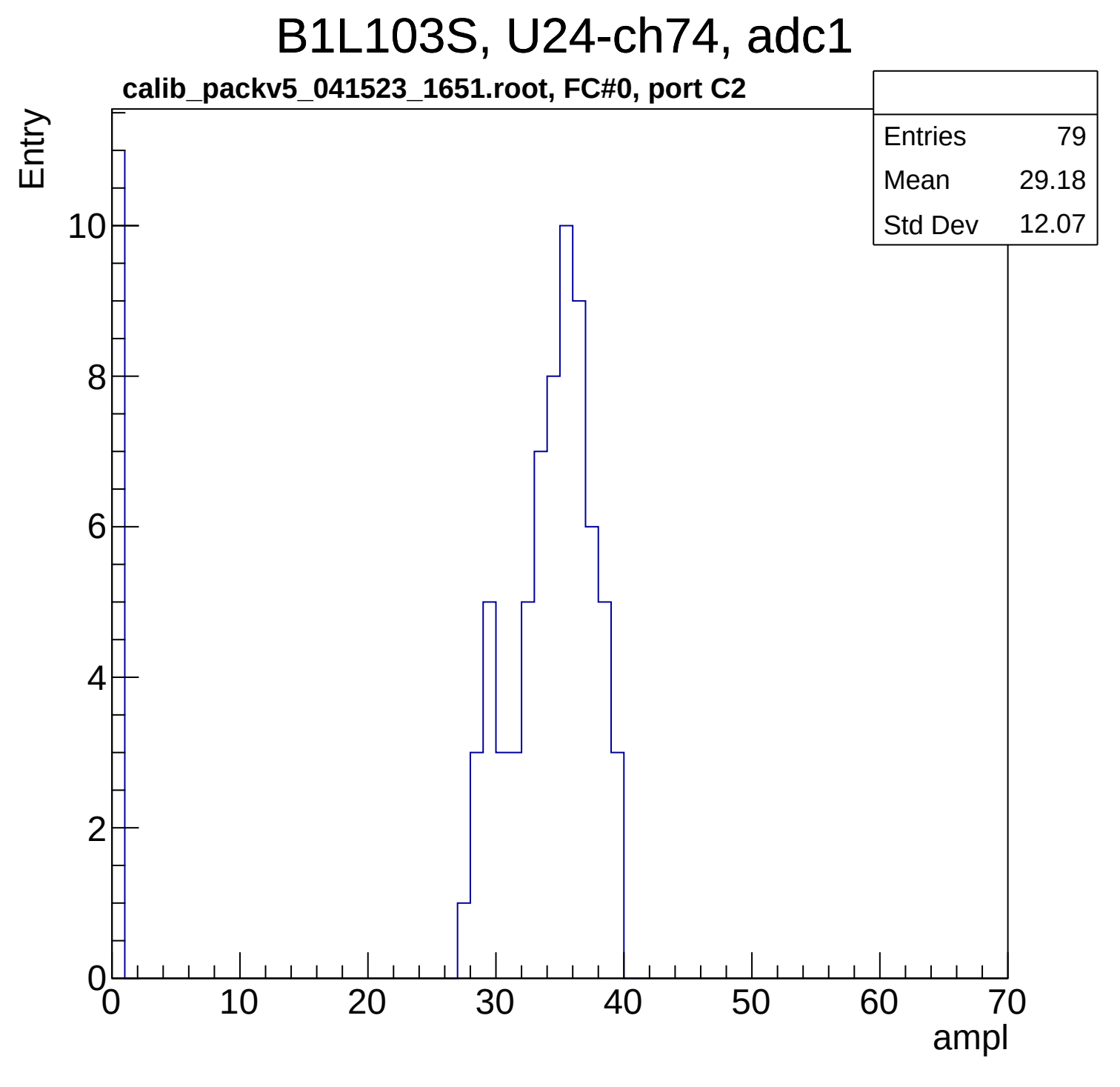
B1L103S, U24-ch74, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 29.18
Std Dev 12.07
Entry
0
2
4
6
8
10
0
10
20
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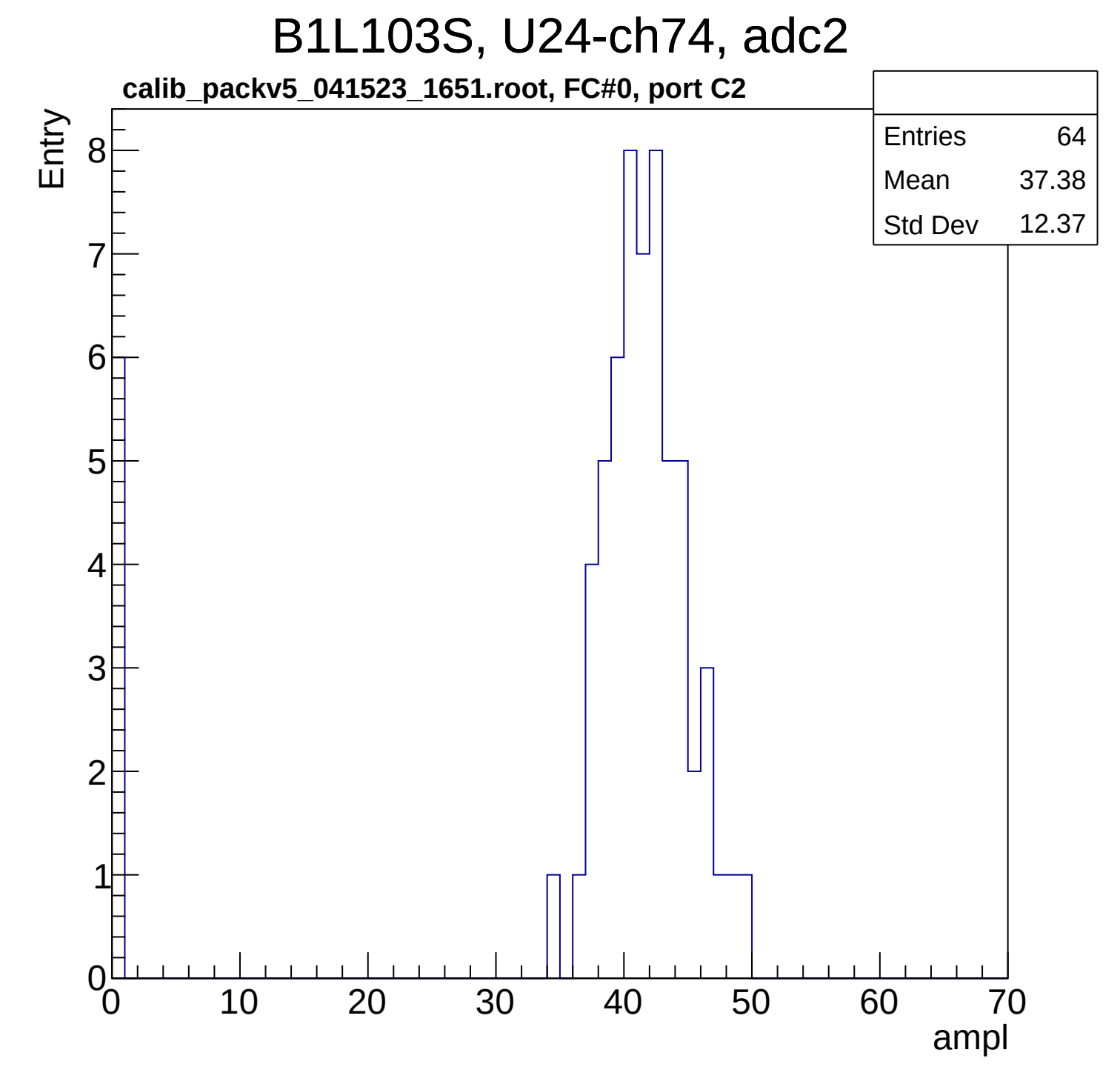
50
60
70
ampl


B1L103S, U24-ch74, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 37.38
Std Dev 12.37
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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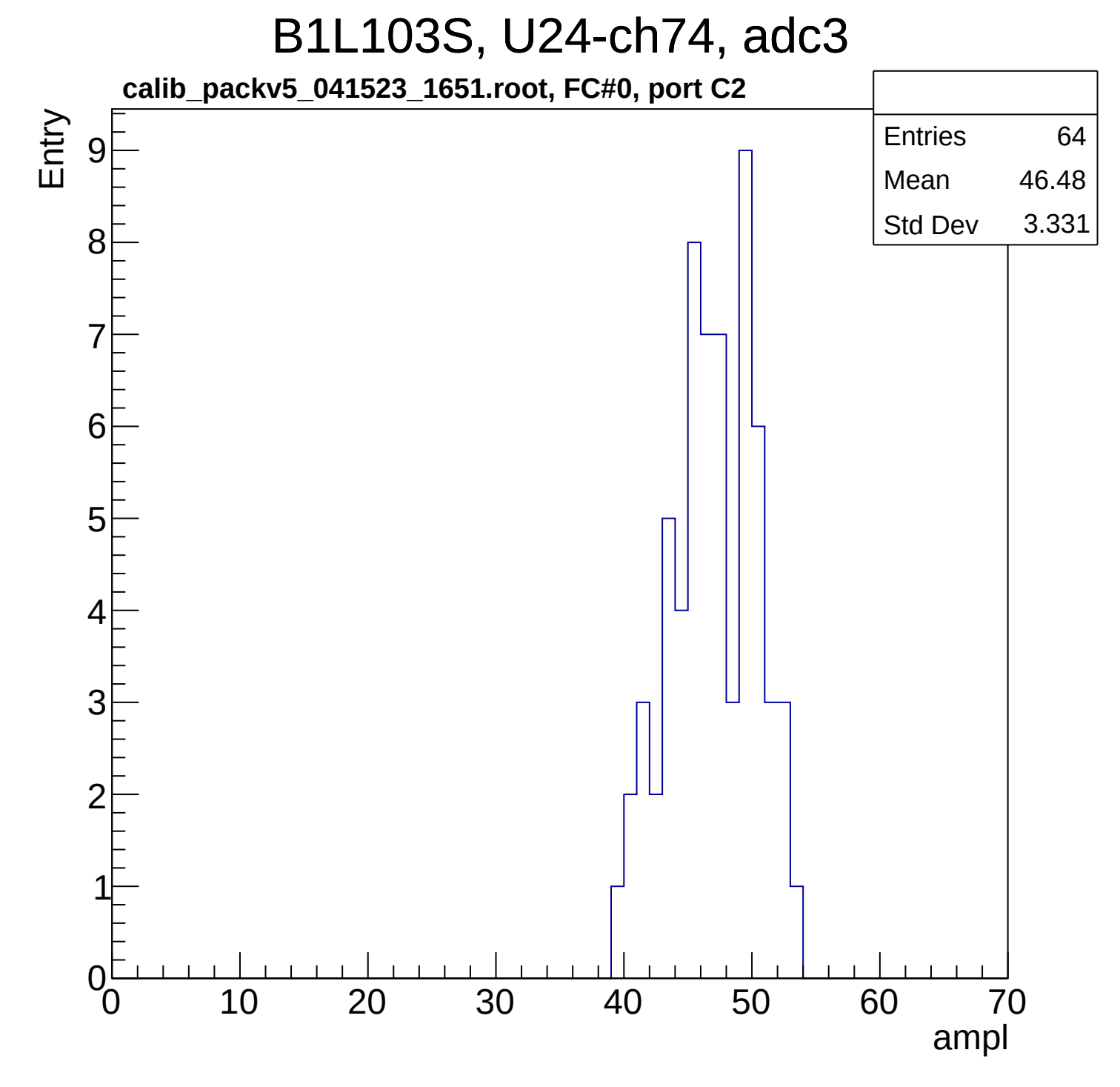
B1L103S, U24-ch74, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 46.48
Std Dev 3.331
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
30
40
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60
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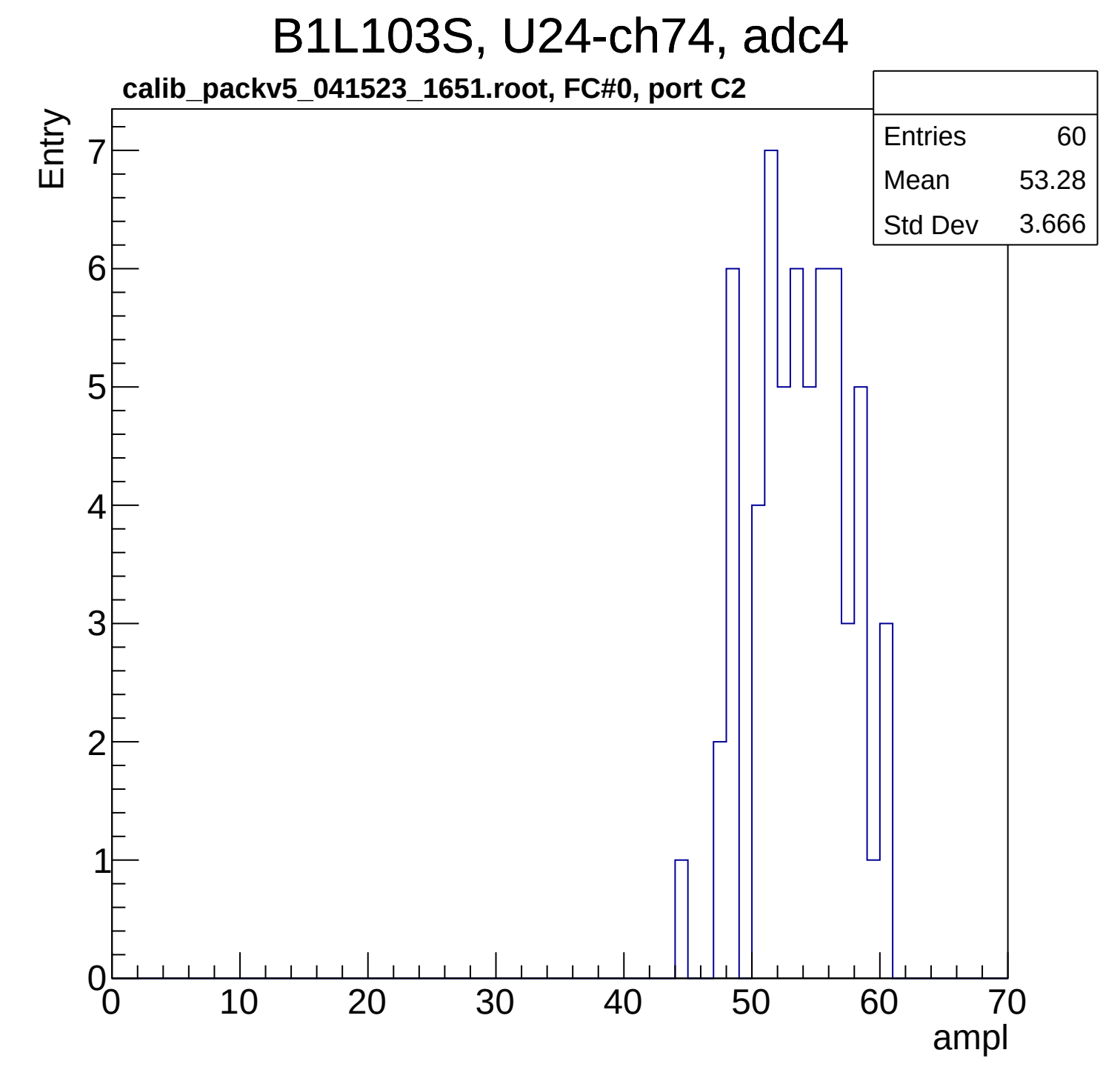
B1L103S, U24-ch74, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 53.28
Std Dev 3.666
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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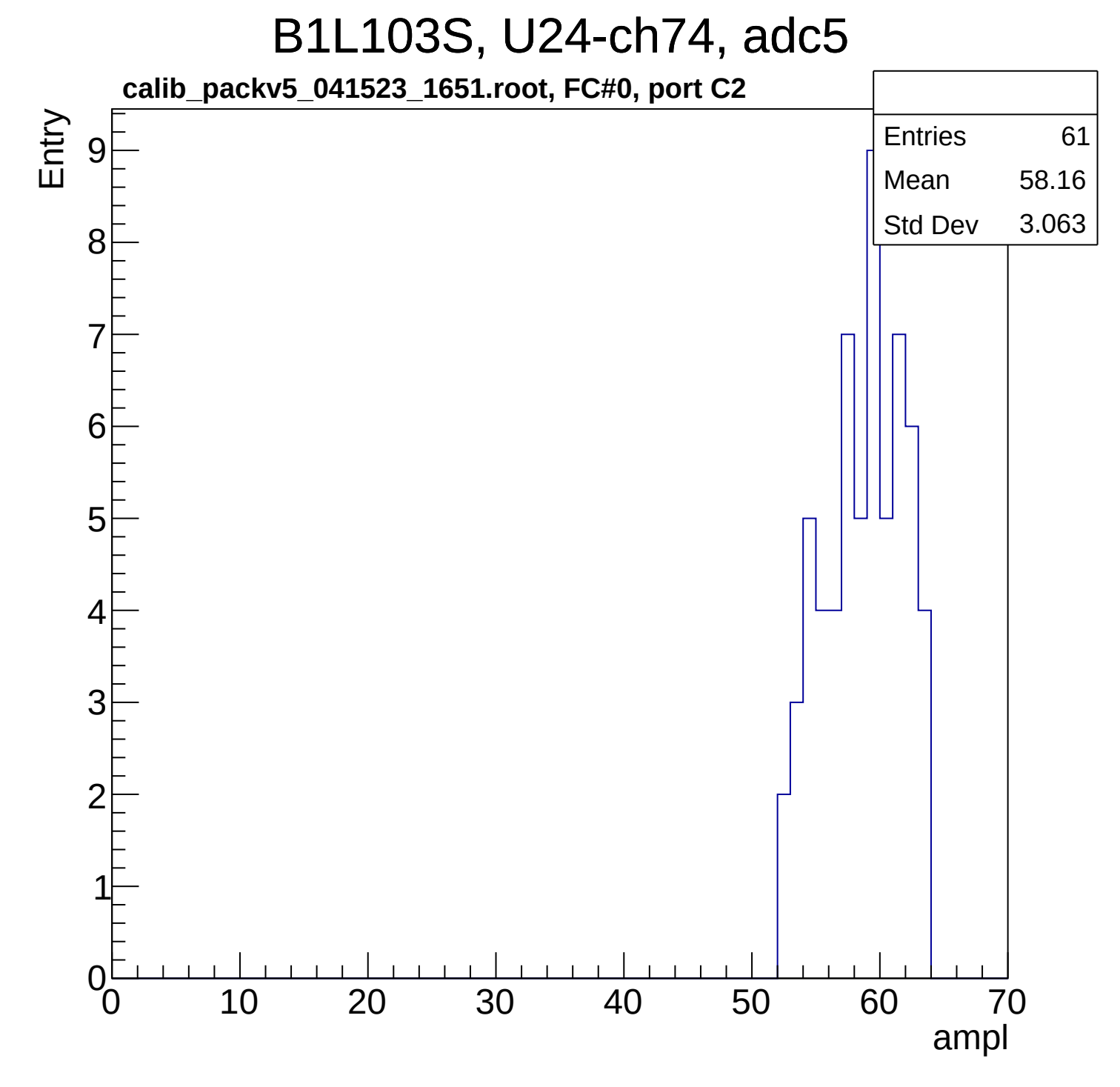
B1L103S, U24-ch74, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 58.16
Std Dev 3.063
Entry
ampl
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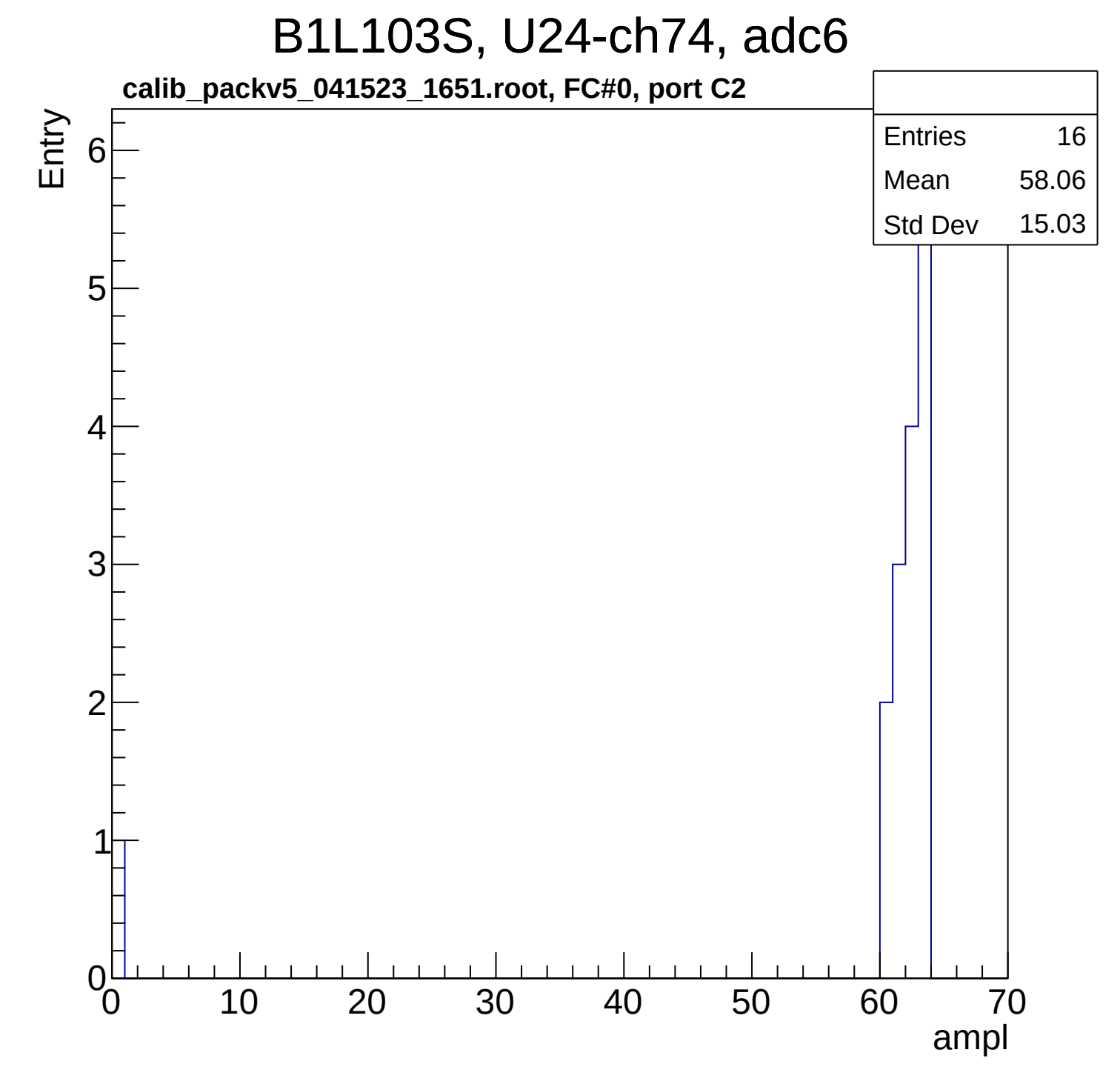
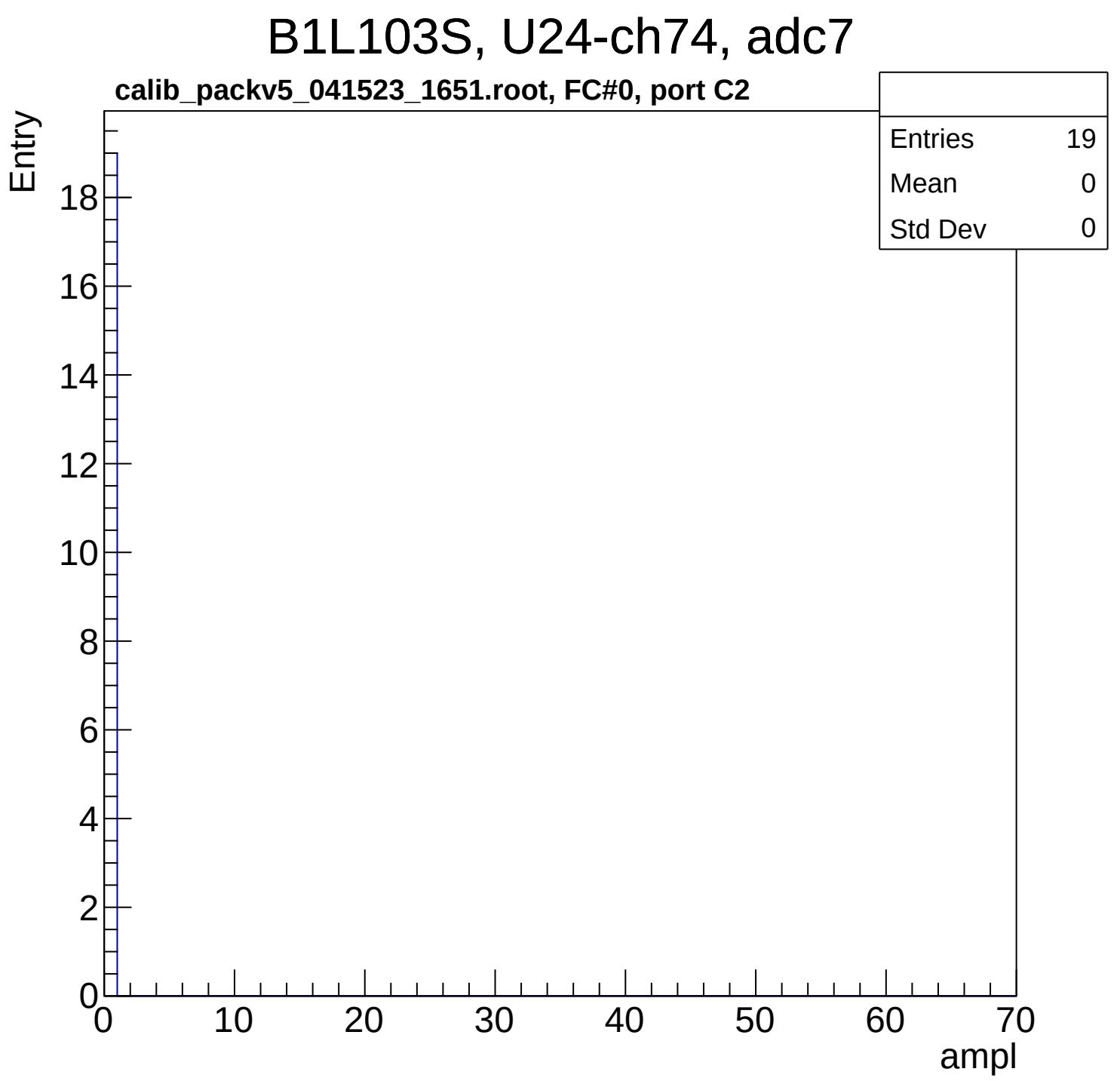
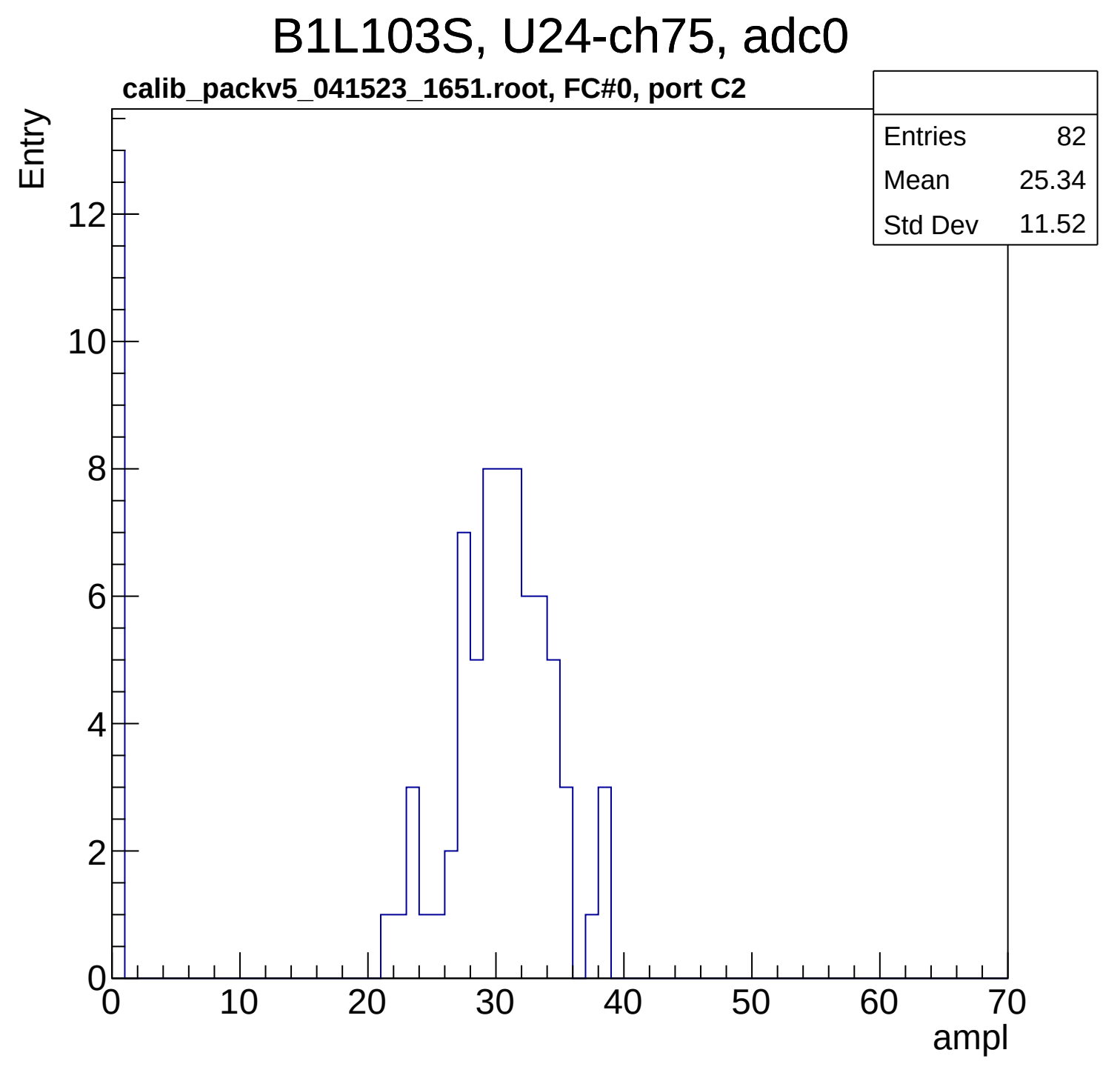
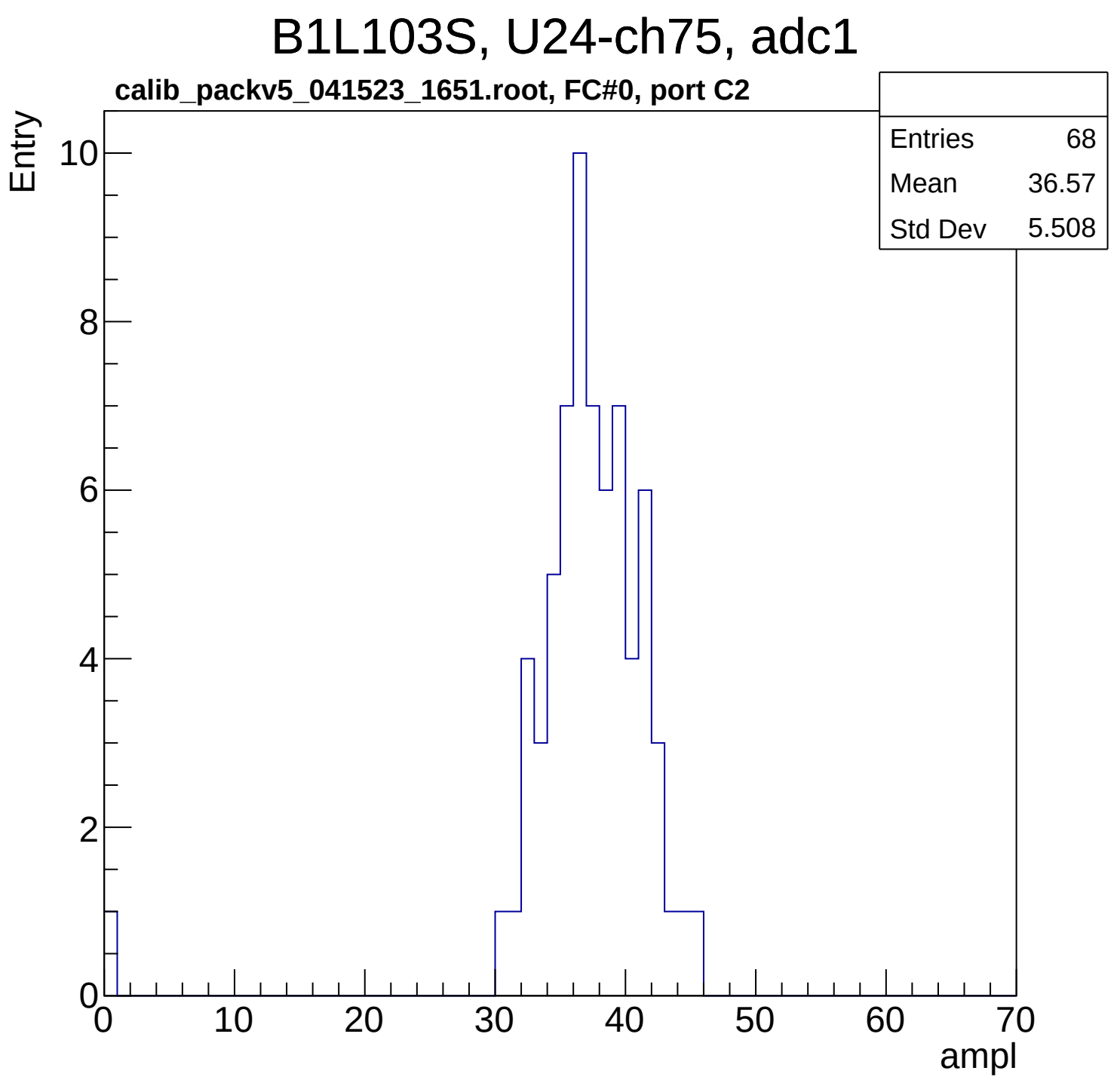
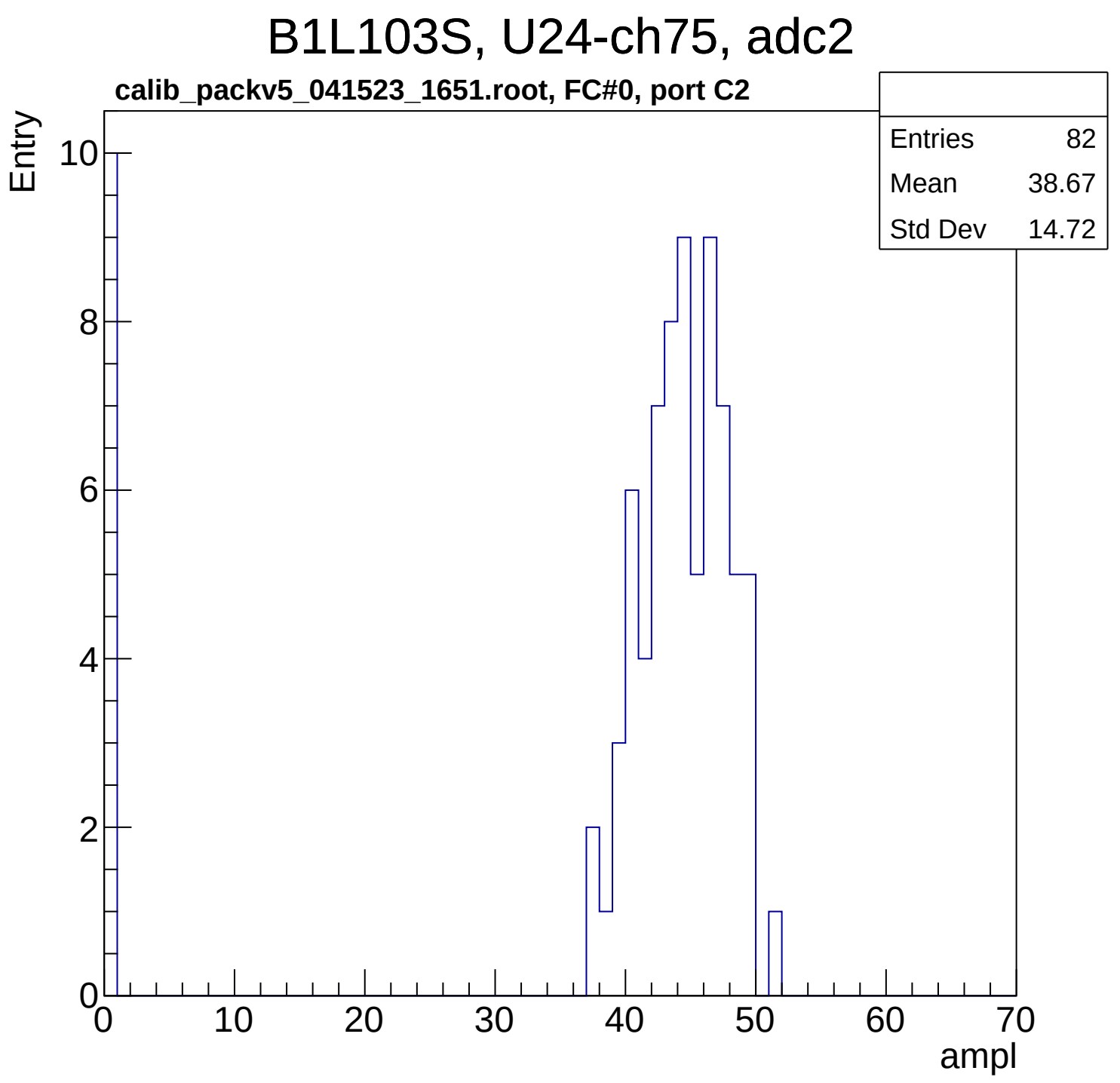
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

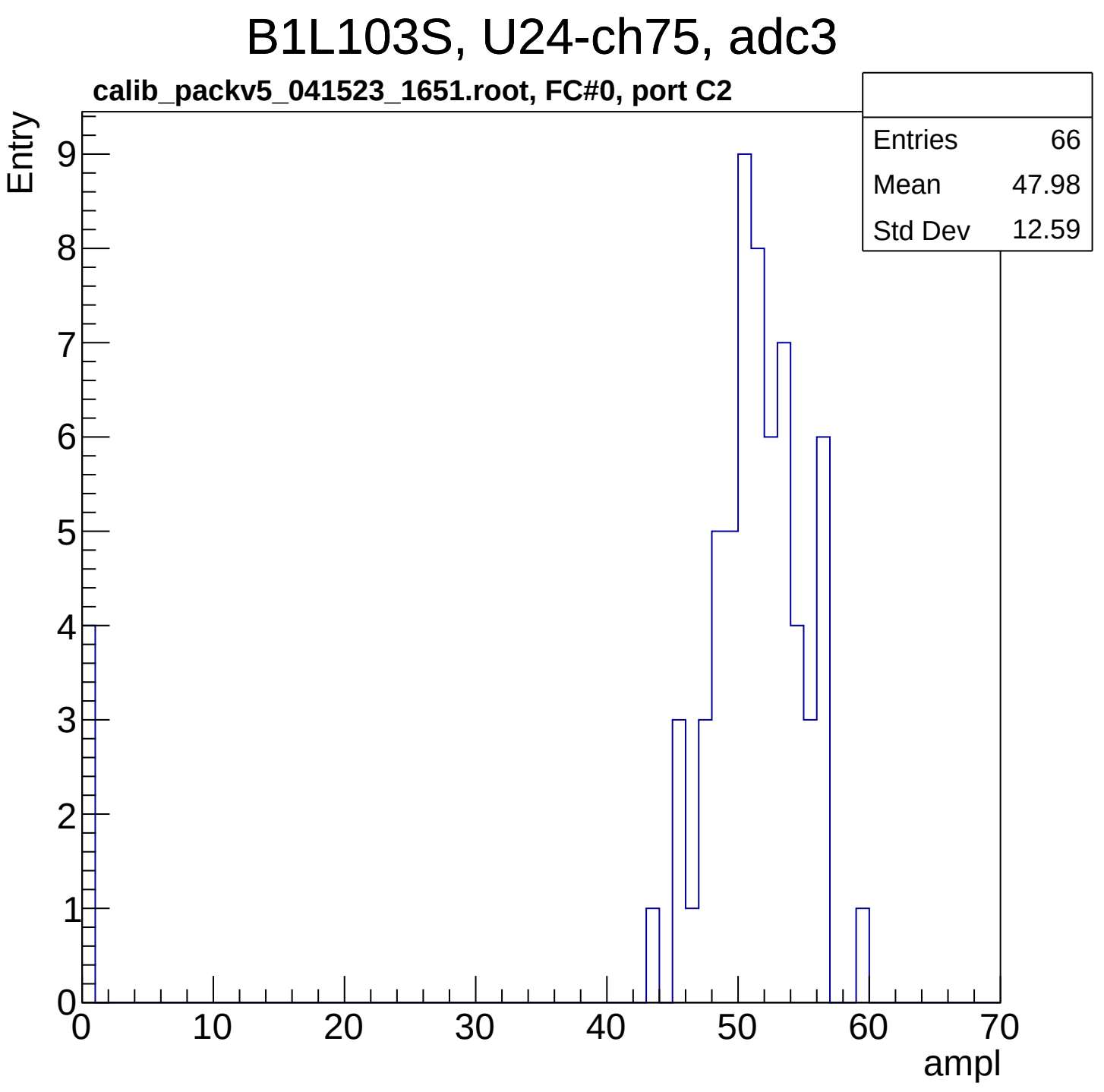

B1L103S, U24-ch74, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 16
Mean 58.06
Std Dev 15.03
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch74, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch75, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 25.34
Std Dev 11.52
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch75, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 36.57
Std Dev 5.508
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch75, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 38.67
Std Dev 14.72
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U24-ch75, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 47.98
Std Dev 12.59
Entry
ampl
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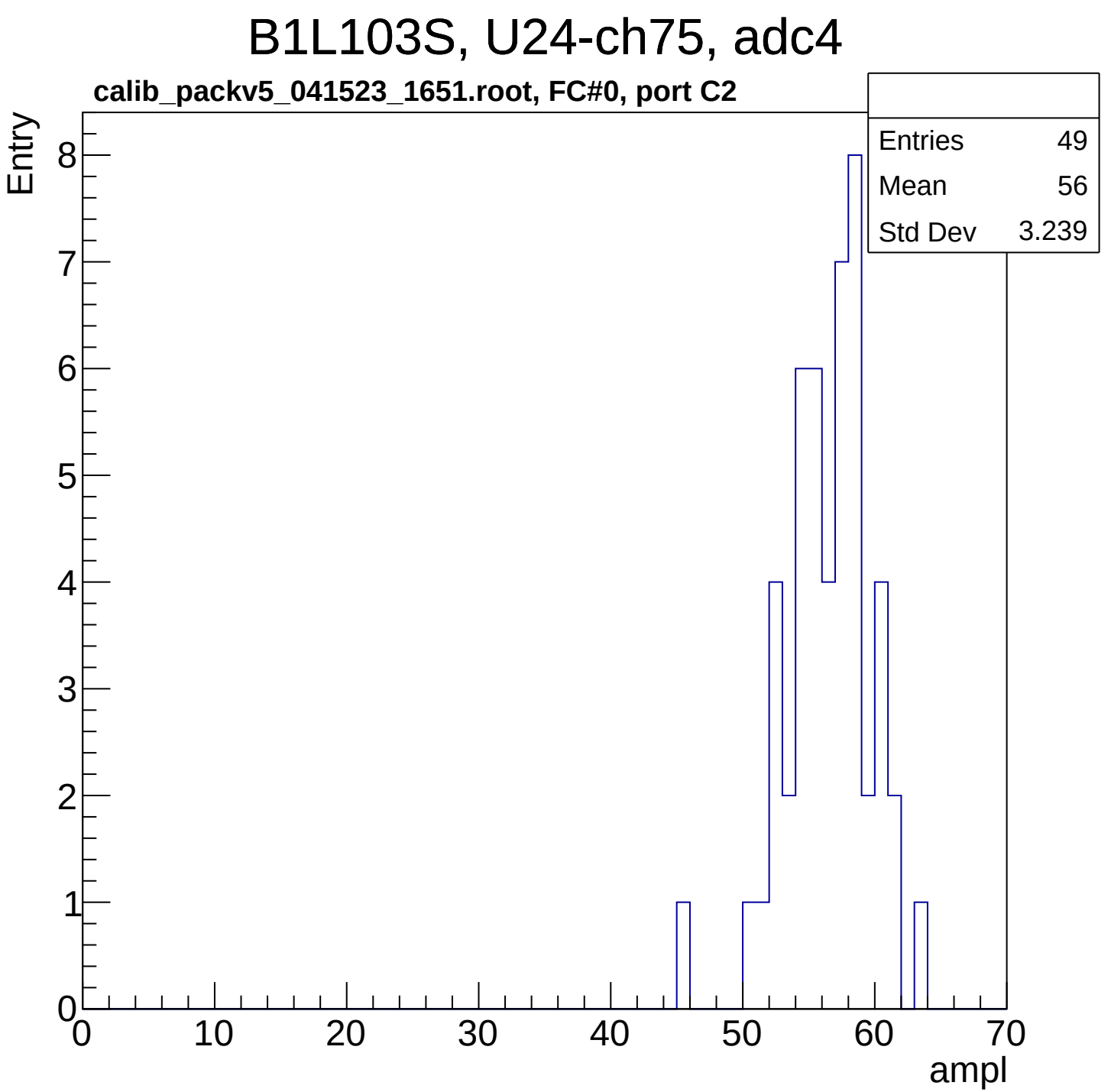
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U24-ch75, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 56
Std Dev 3.239
Entry
ampl
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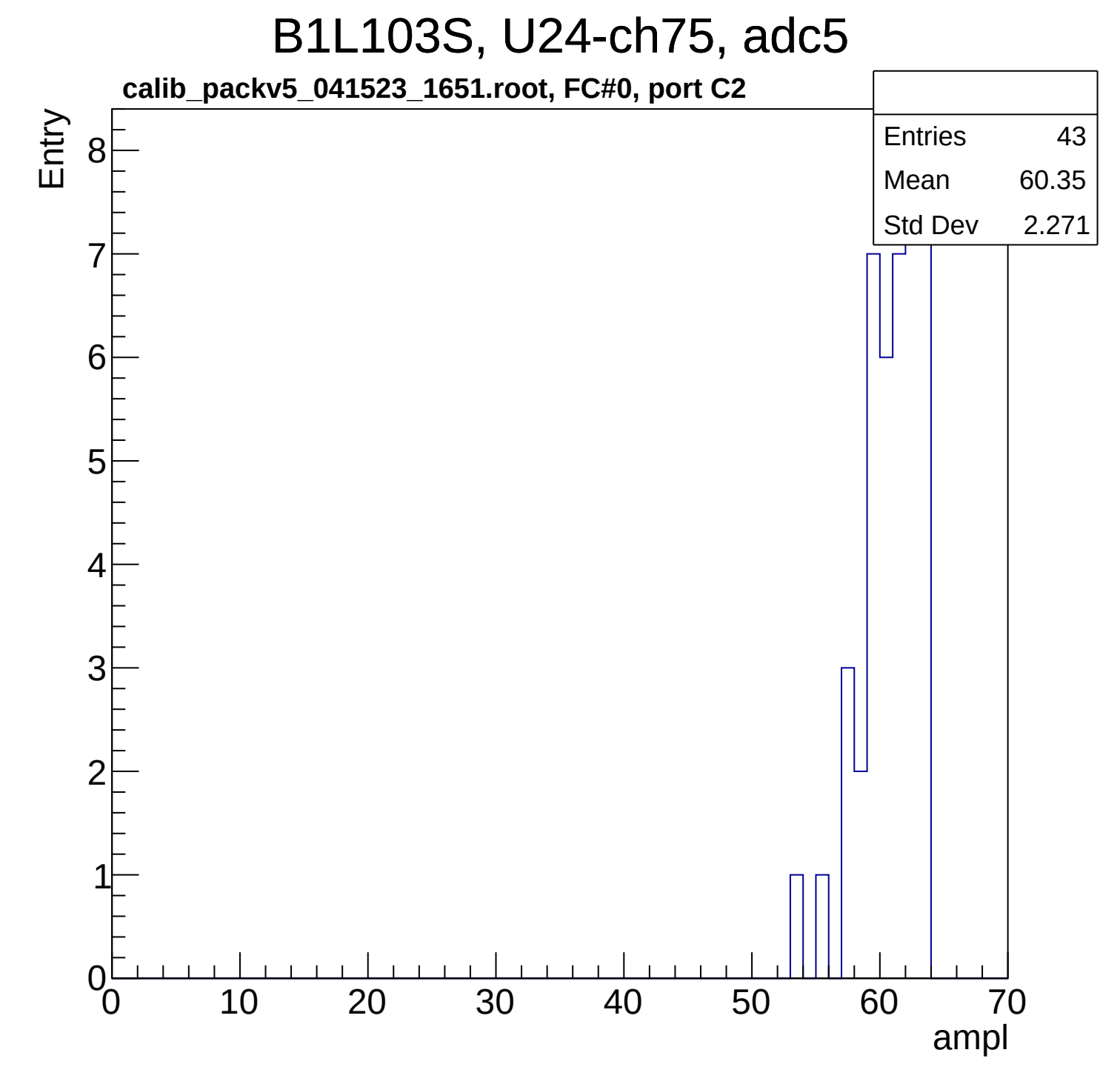
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U24-ch75, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 43
Mean 60.35
Std Dev 2.271
Entry
ampl
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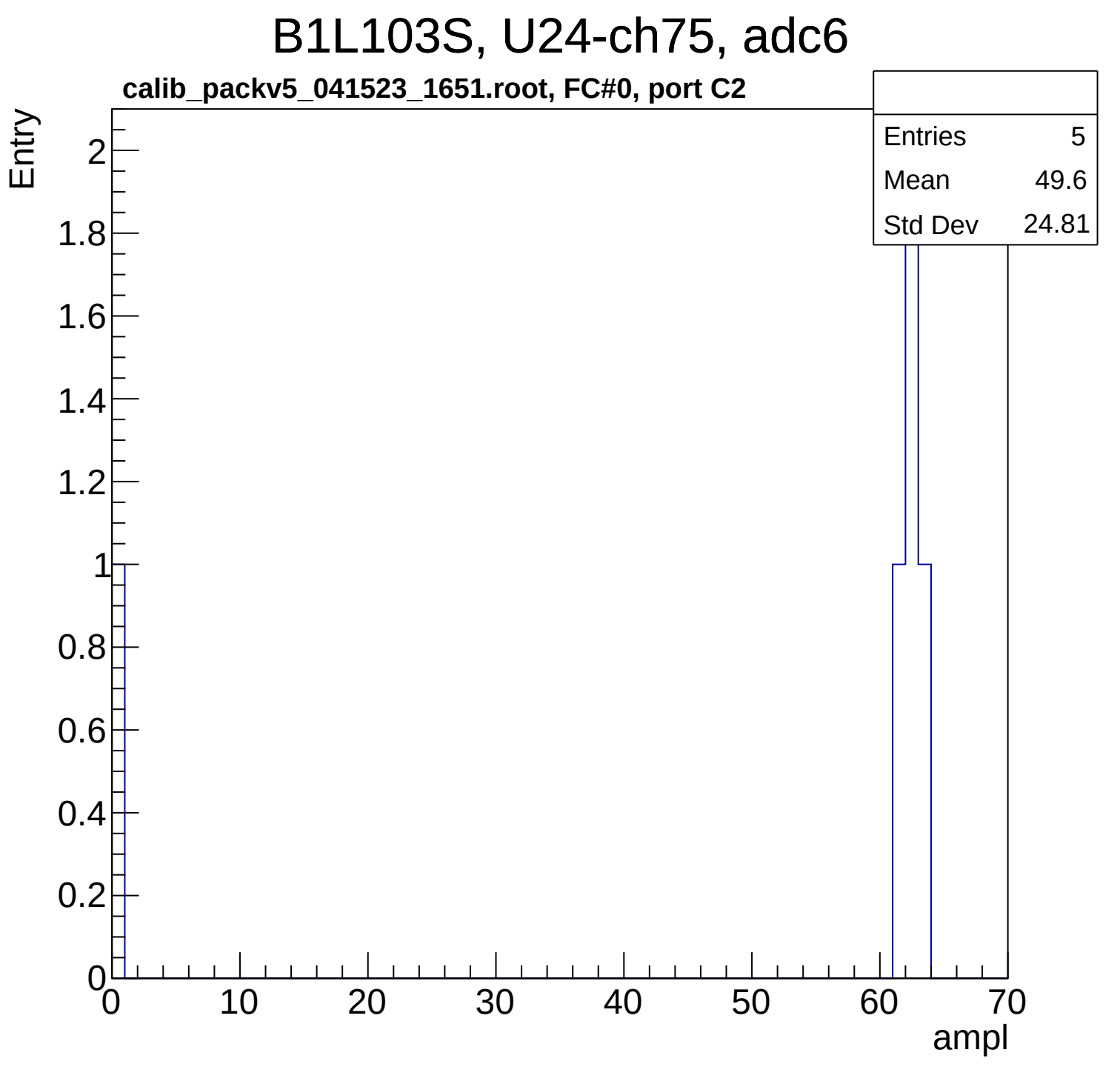
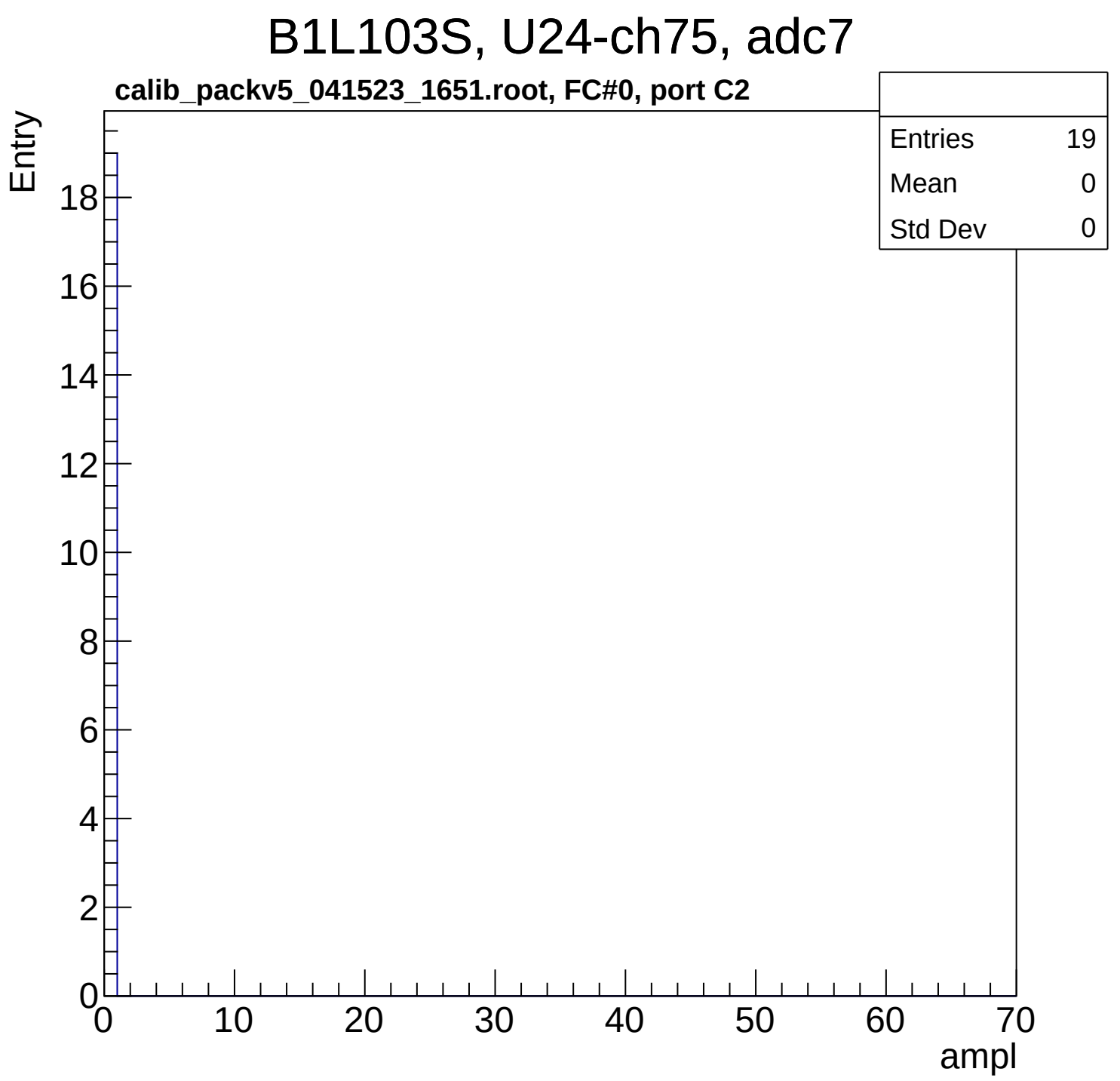
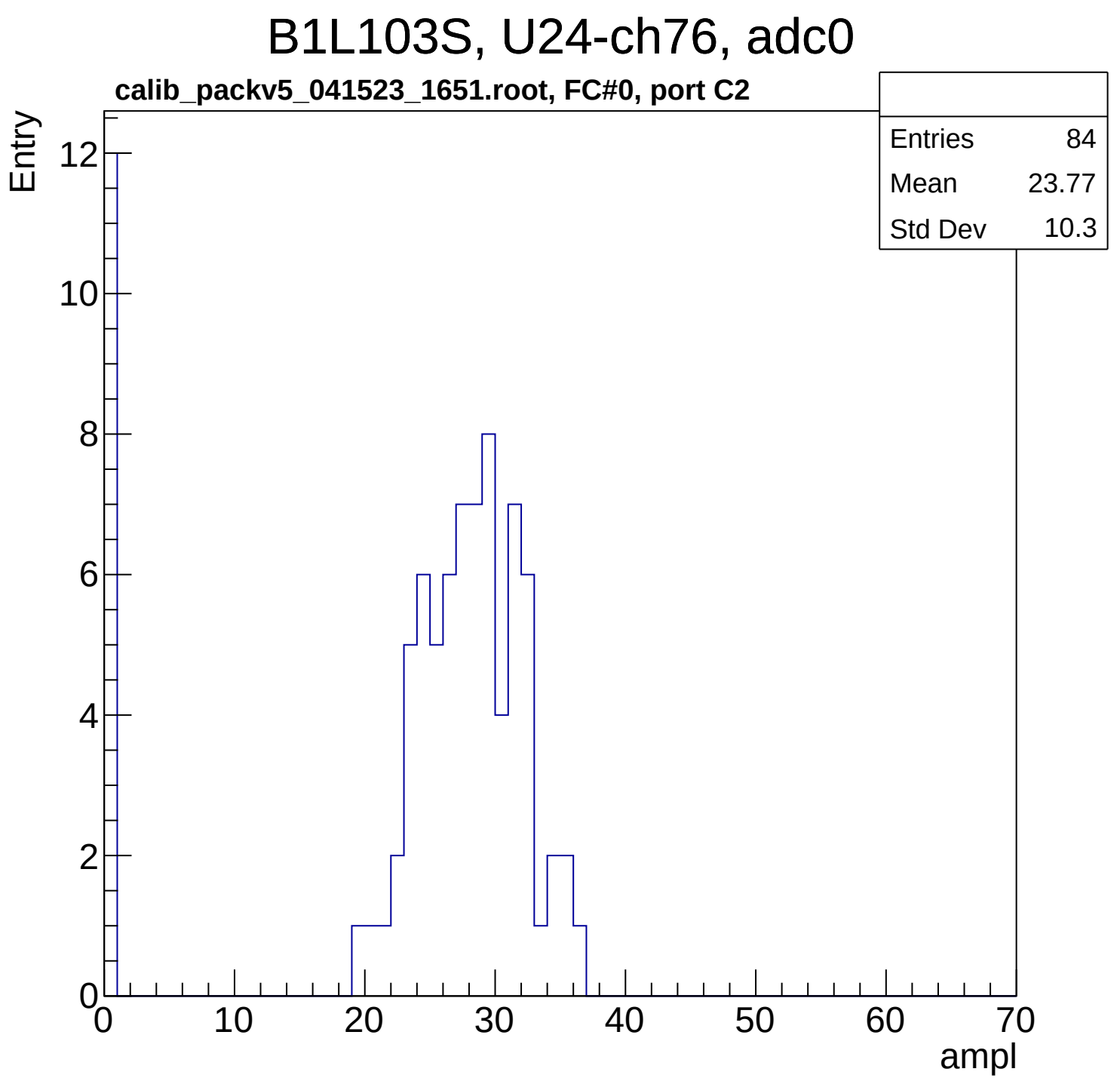
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U24-ch75, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 5
Mean 49.6
Std Dev 24.81
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U24-ch75, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch76, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 23.77
Std Dev 10.3
Entry
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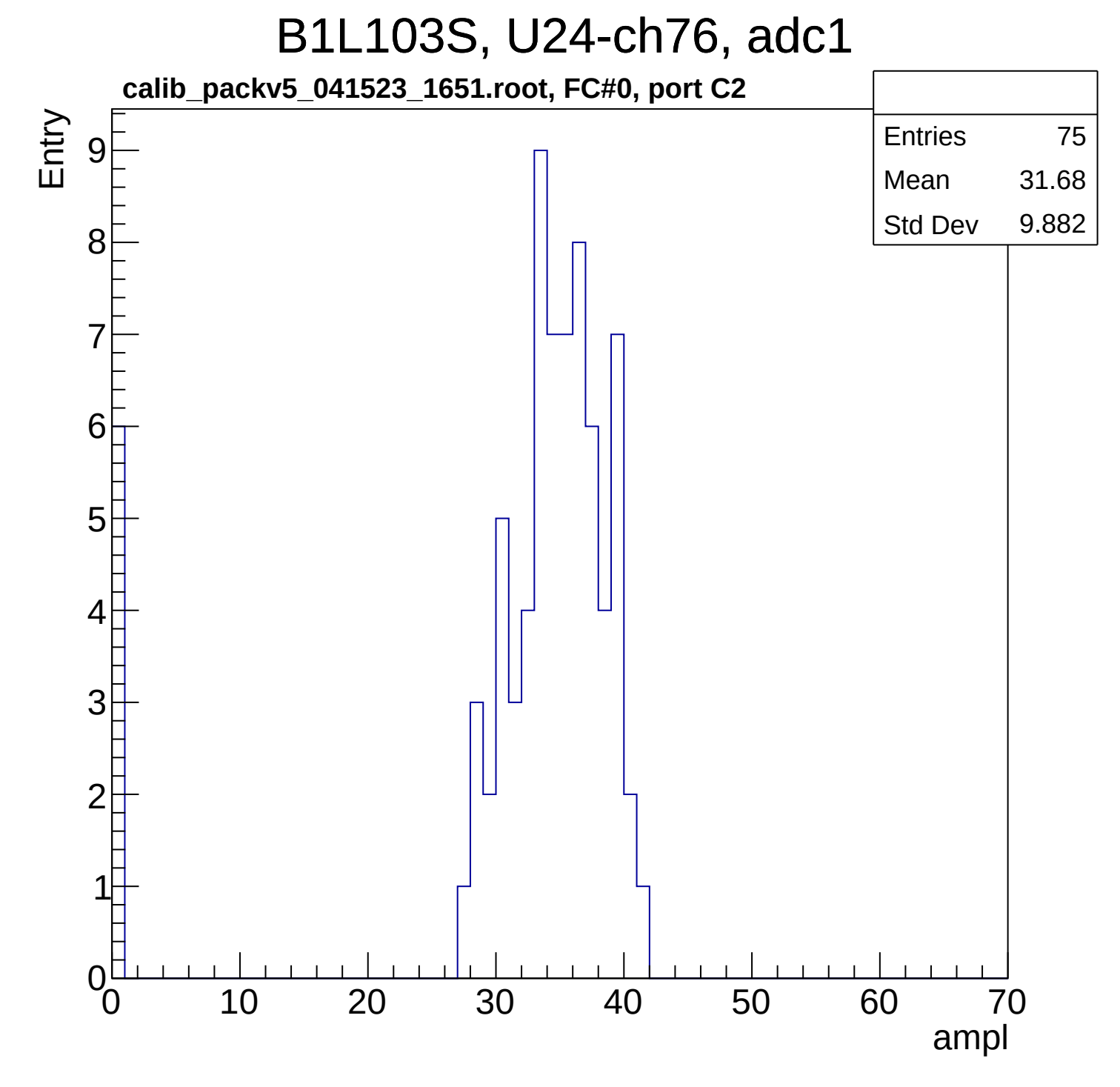
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch76, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 31.68
Std Dev 9.882
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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60
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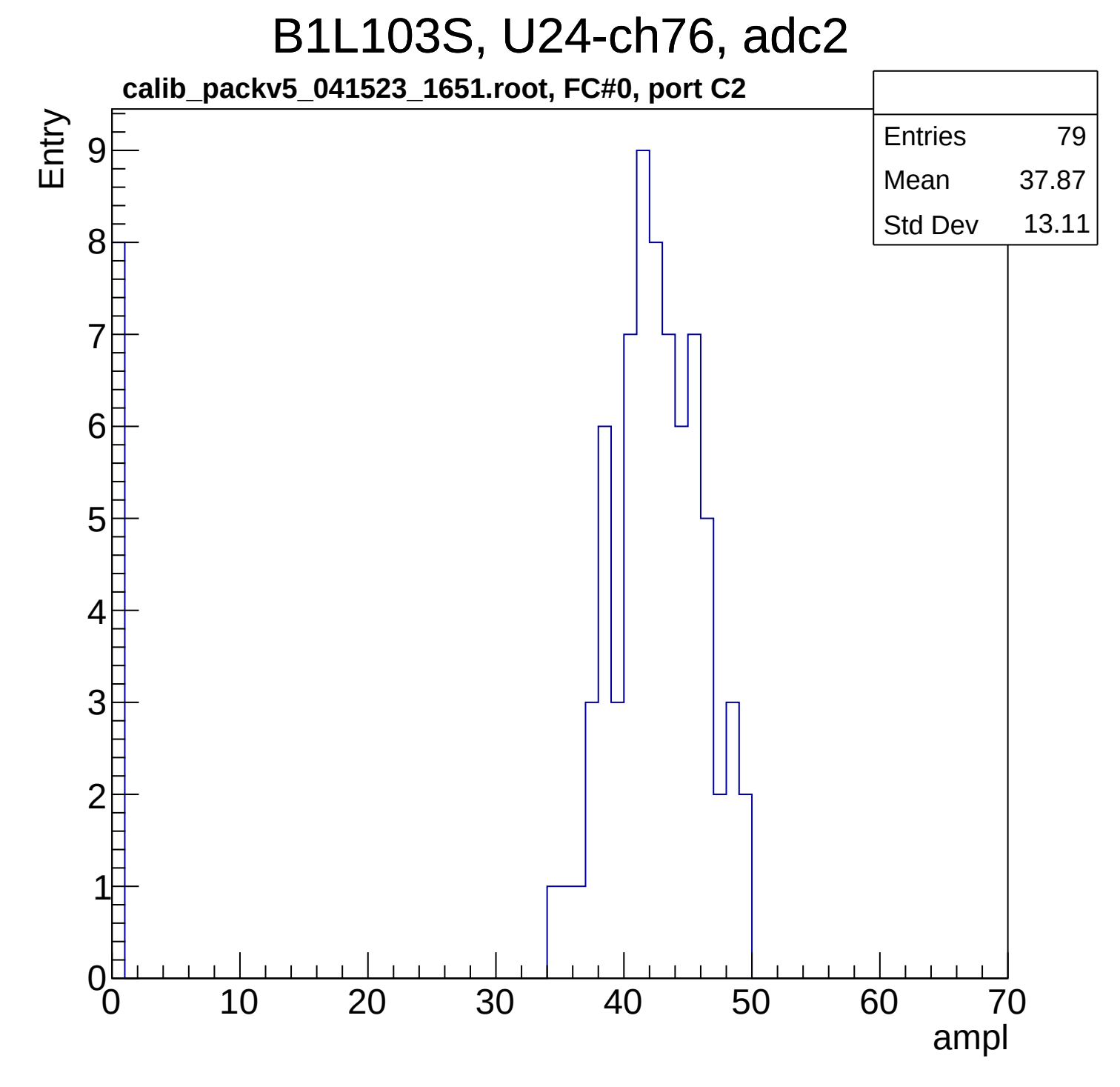
B1L103S, U24-ch76, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 37.87
Std Dev 13.11
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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60
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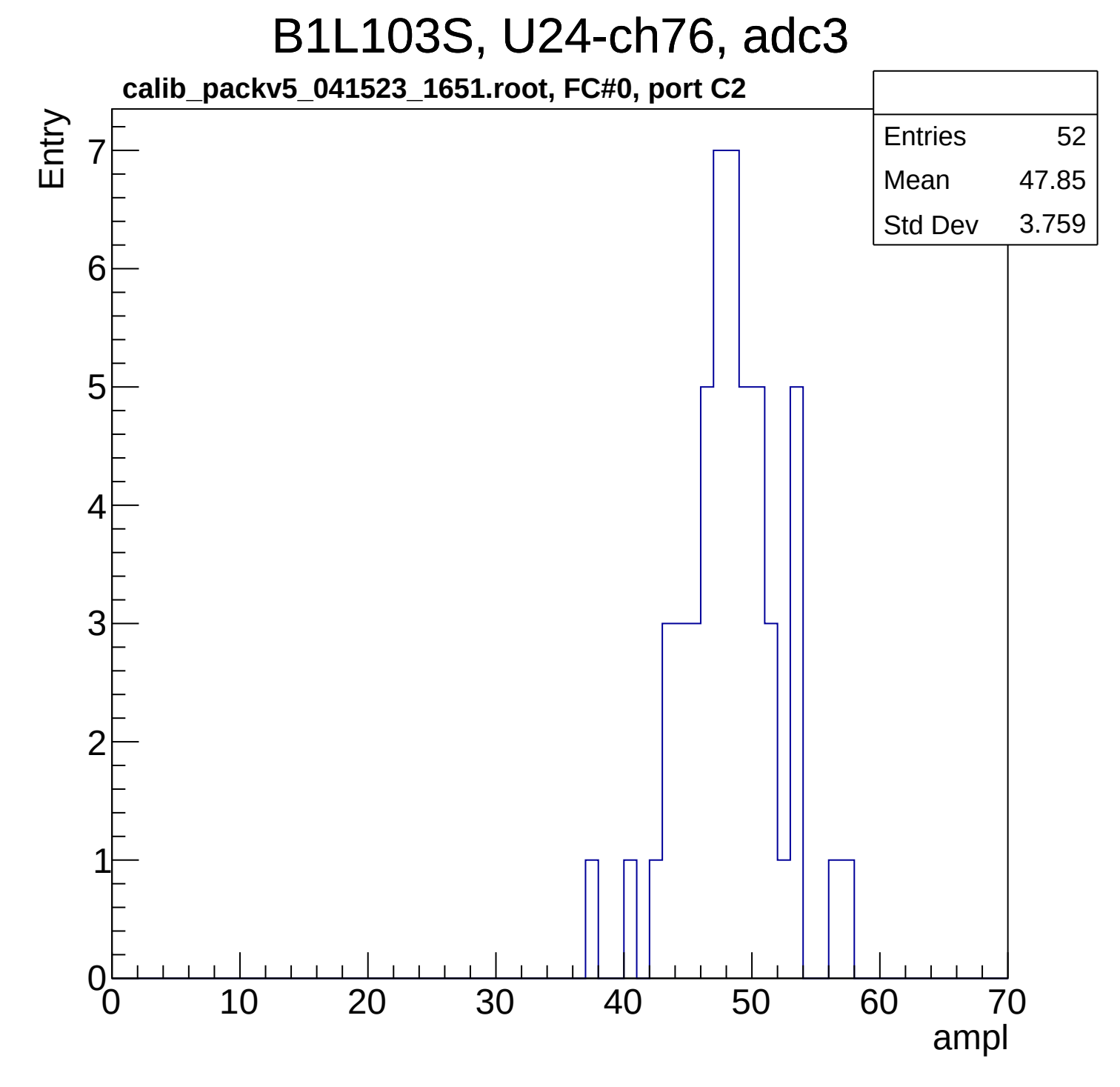
B1L103S, U24-ch76, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 47.85
Std Dev 3.759
Entry
ampl
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1
2
3
4
5
6
7
0
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40
50
60
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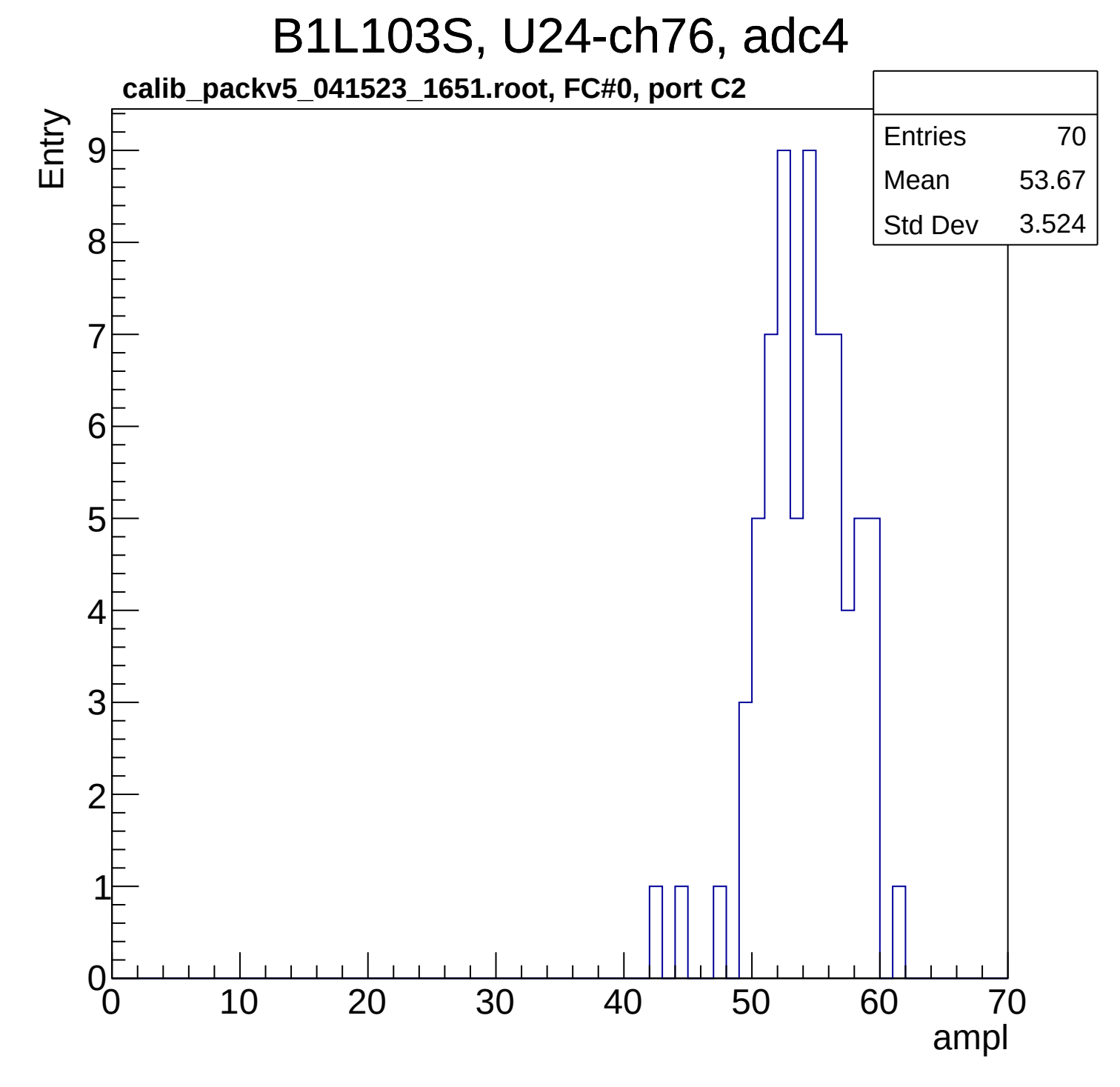
B1L103S, U24-ch76, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 53.67
Std Dev 3.524
Entry
ampl
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3
4
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6
7
8
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0
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60
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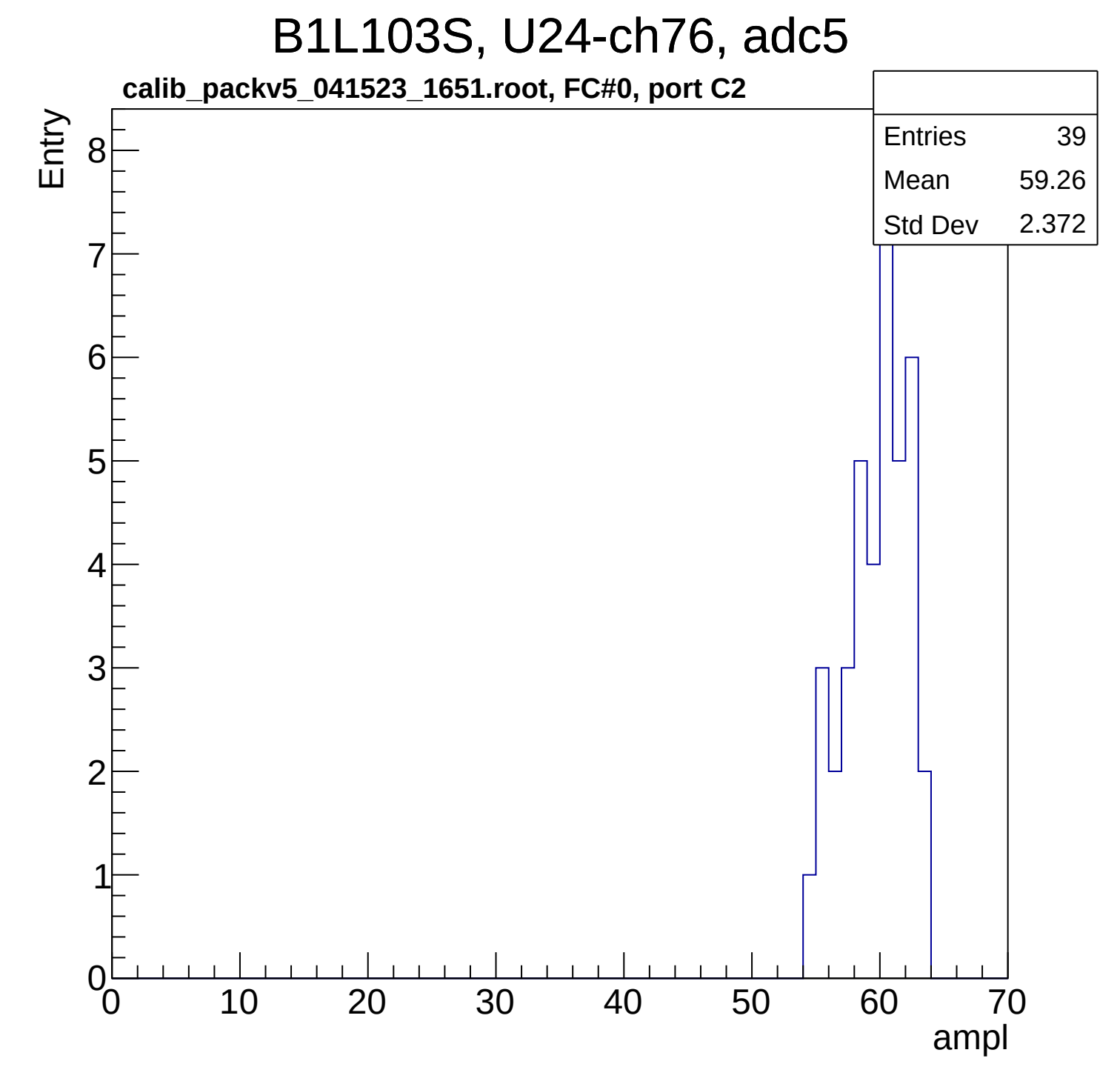
B1L103S, U24-ch76, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 39
Mean 59.26
Std Dev 2.372
Entry
ampl
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2
3
4
5
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0
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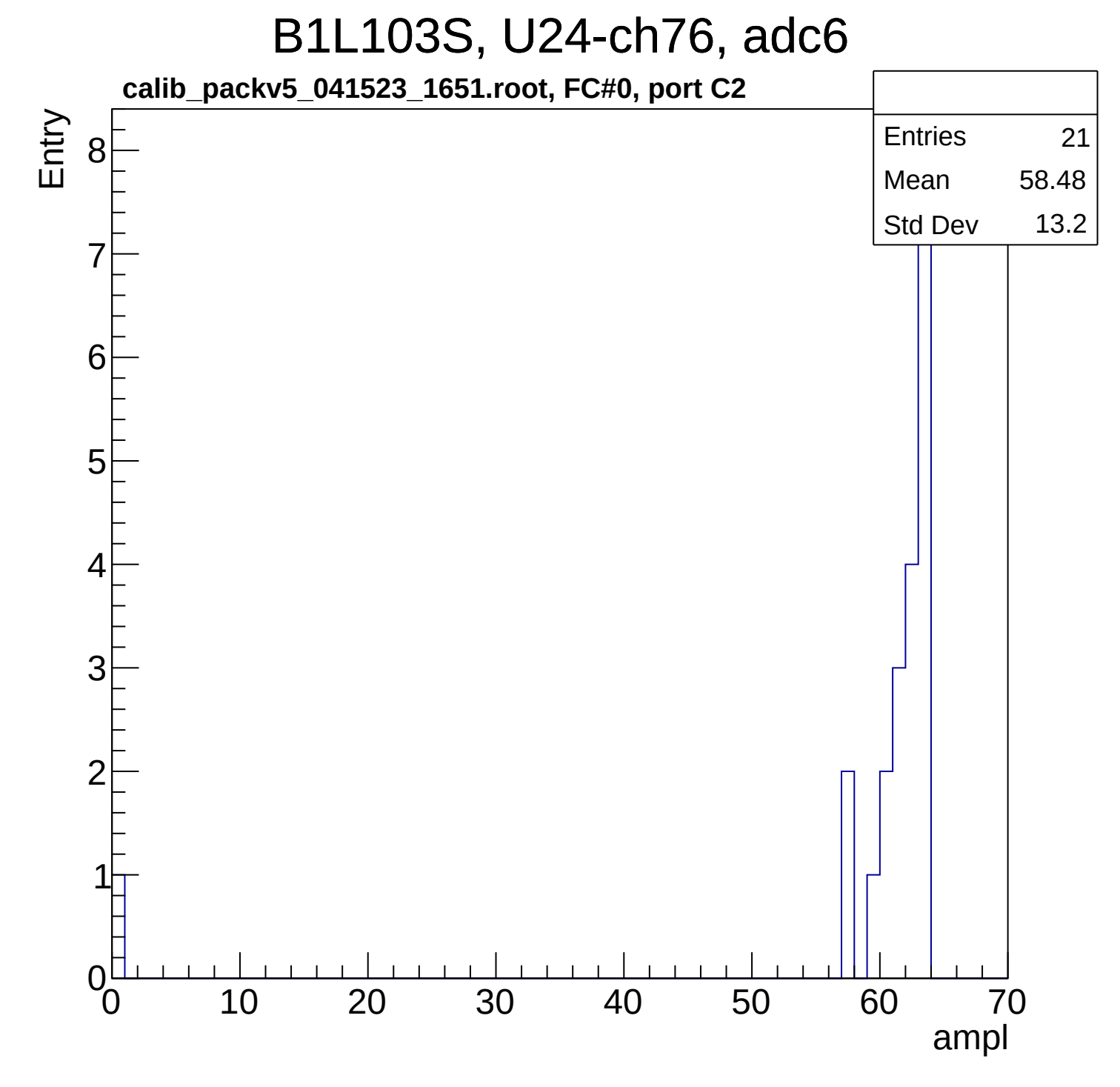
B1L103S, U24-ch76, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 58.48
Std Dev 13.2
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
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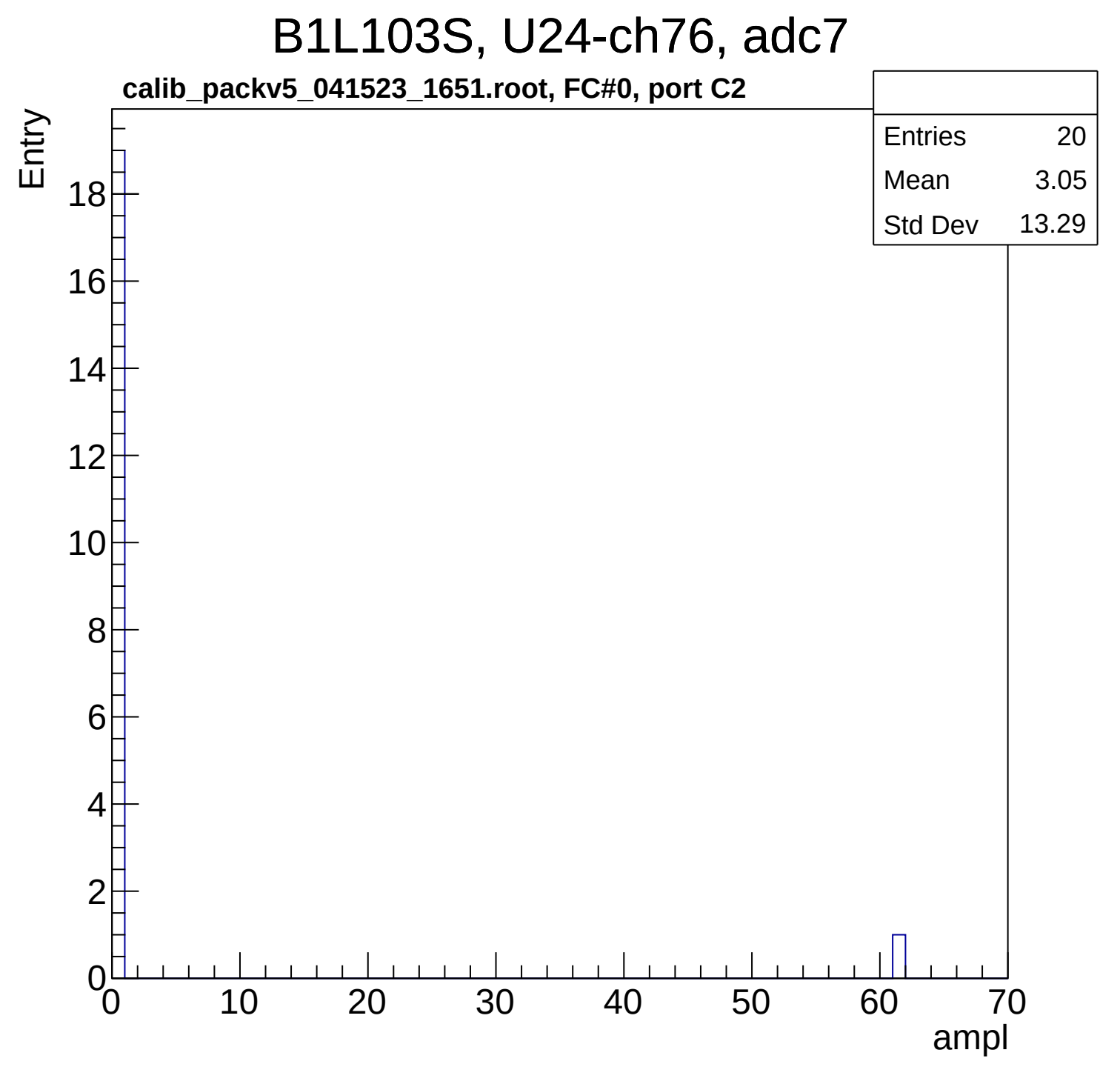
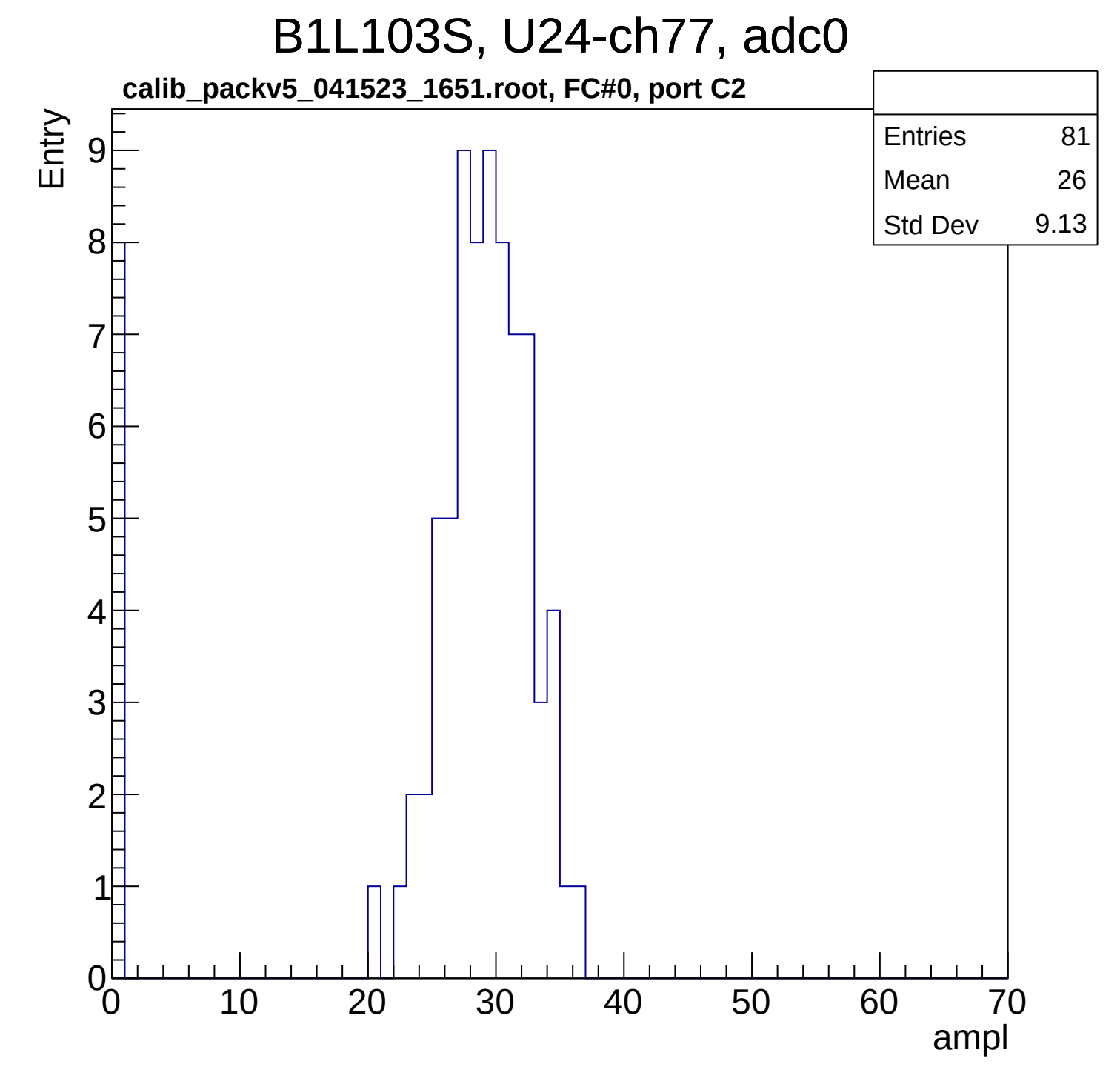
40
50
60
70


B1L103S, U24-ch76, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.05
Std Dev 13.29
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch77, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 26
Std Dev 9.13
Entry
ampl
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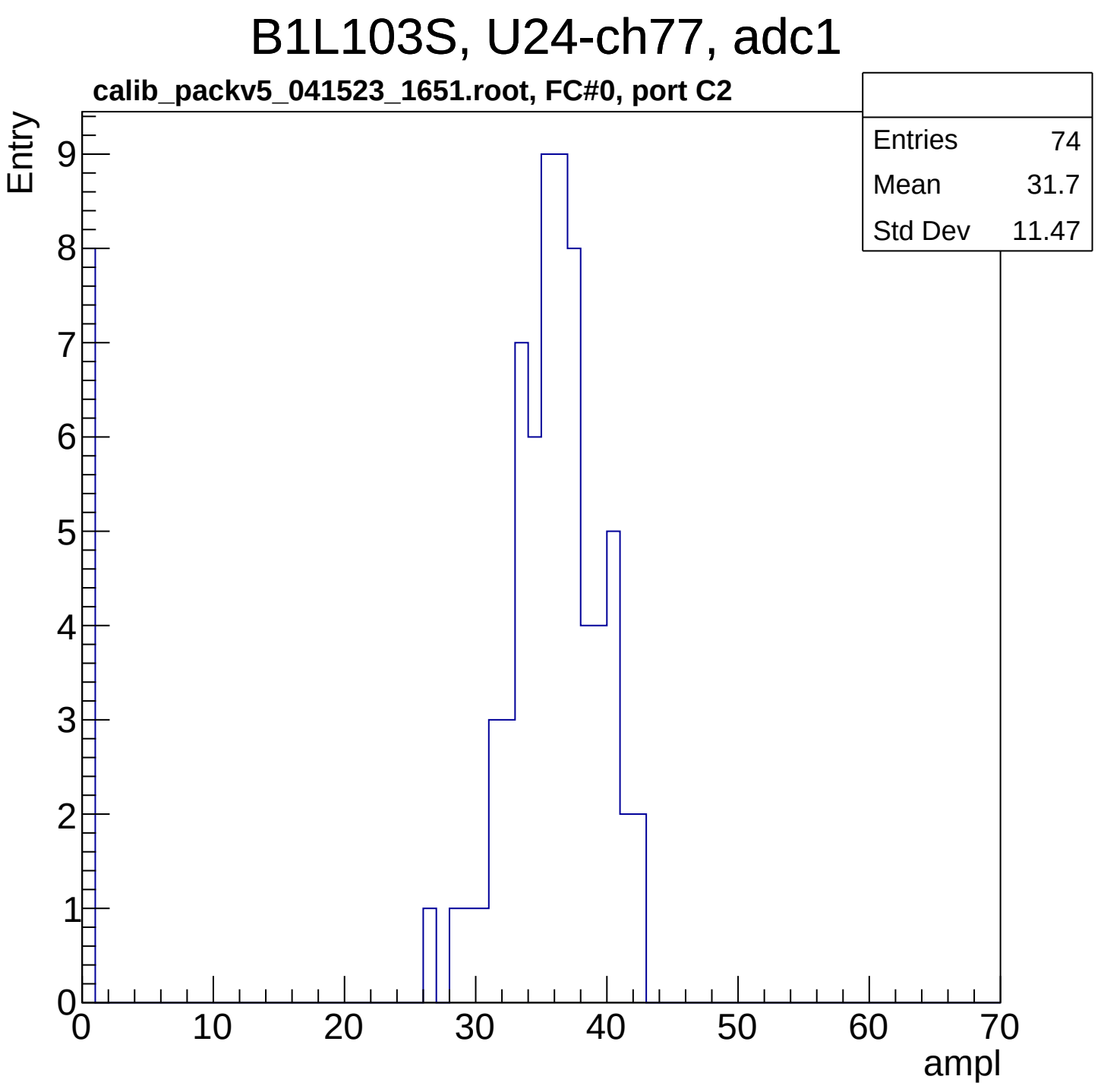
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U24-ch77, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 31.7
Std Dev 11.47
Entry
ampl
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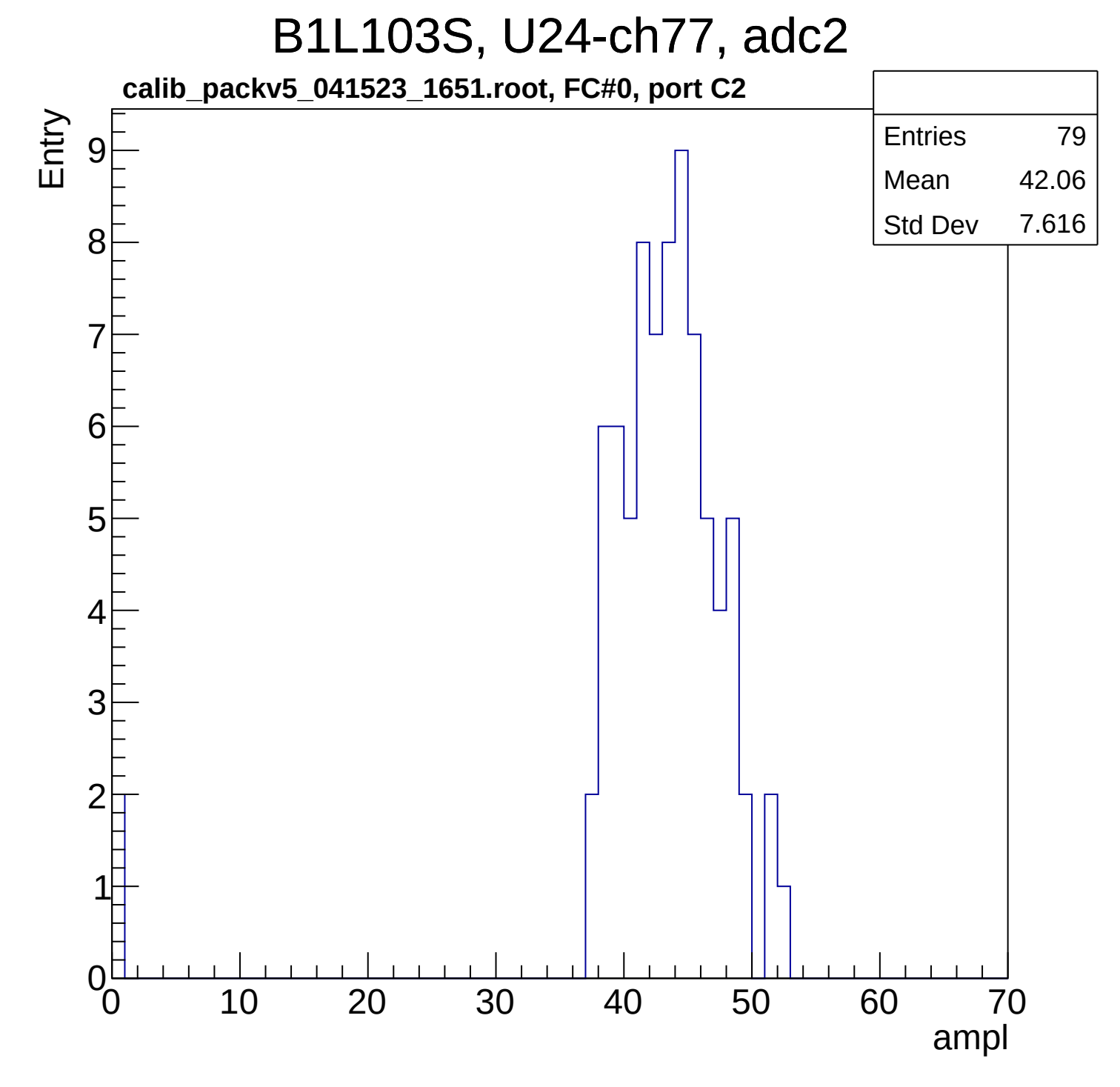
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U24-ch77, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 42.06
Std Dev 7.616
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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60
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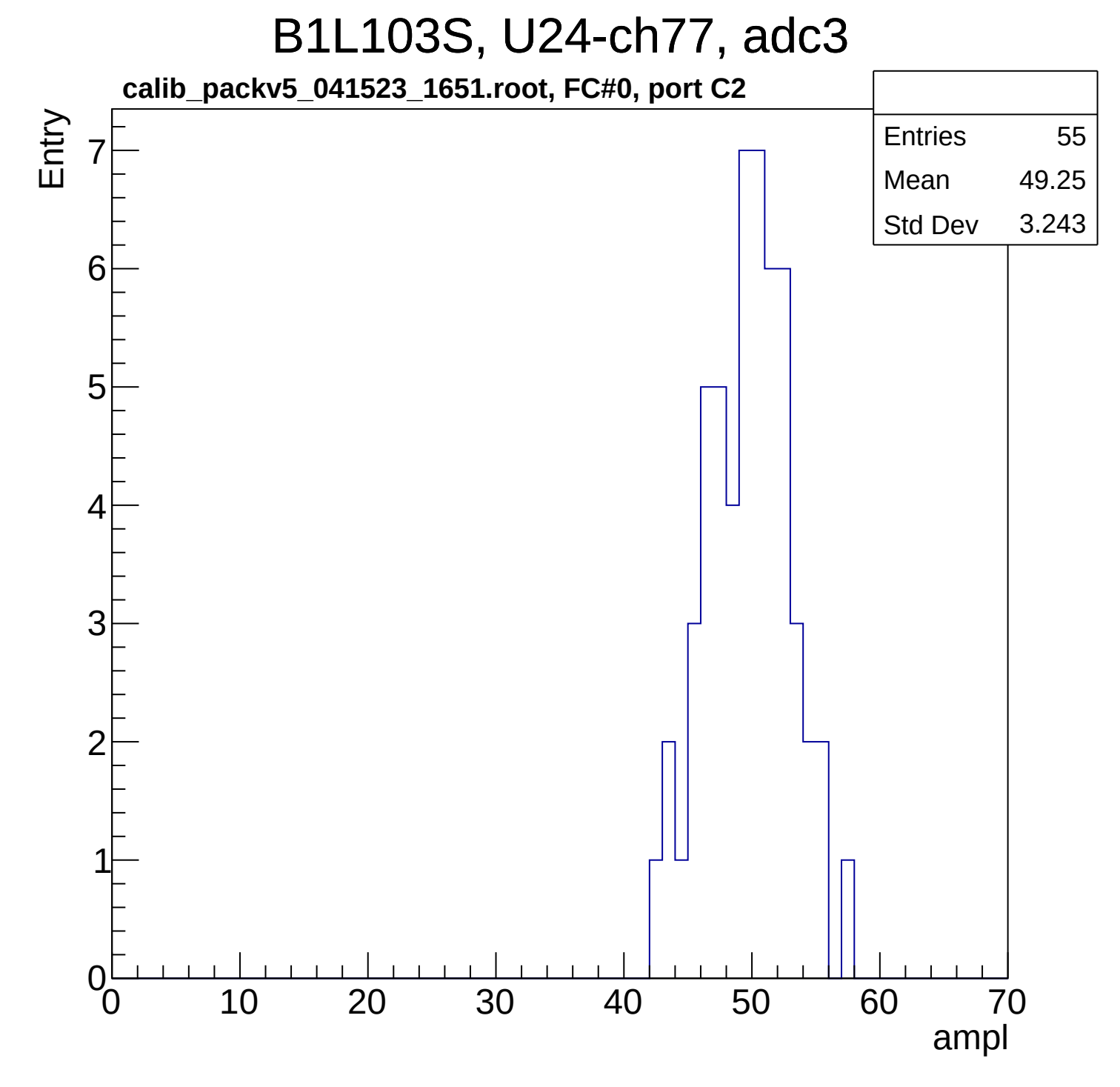
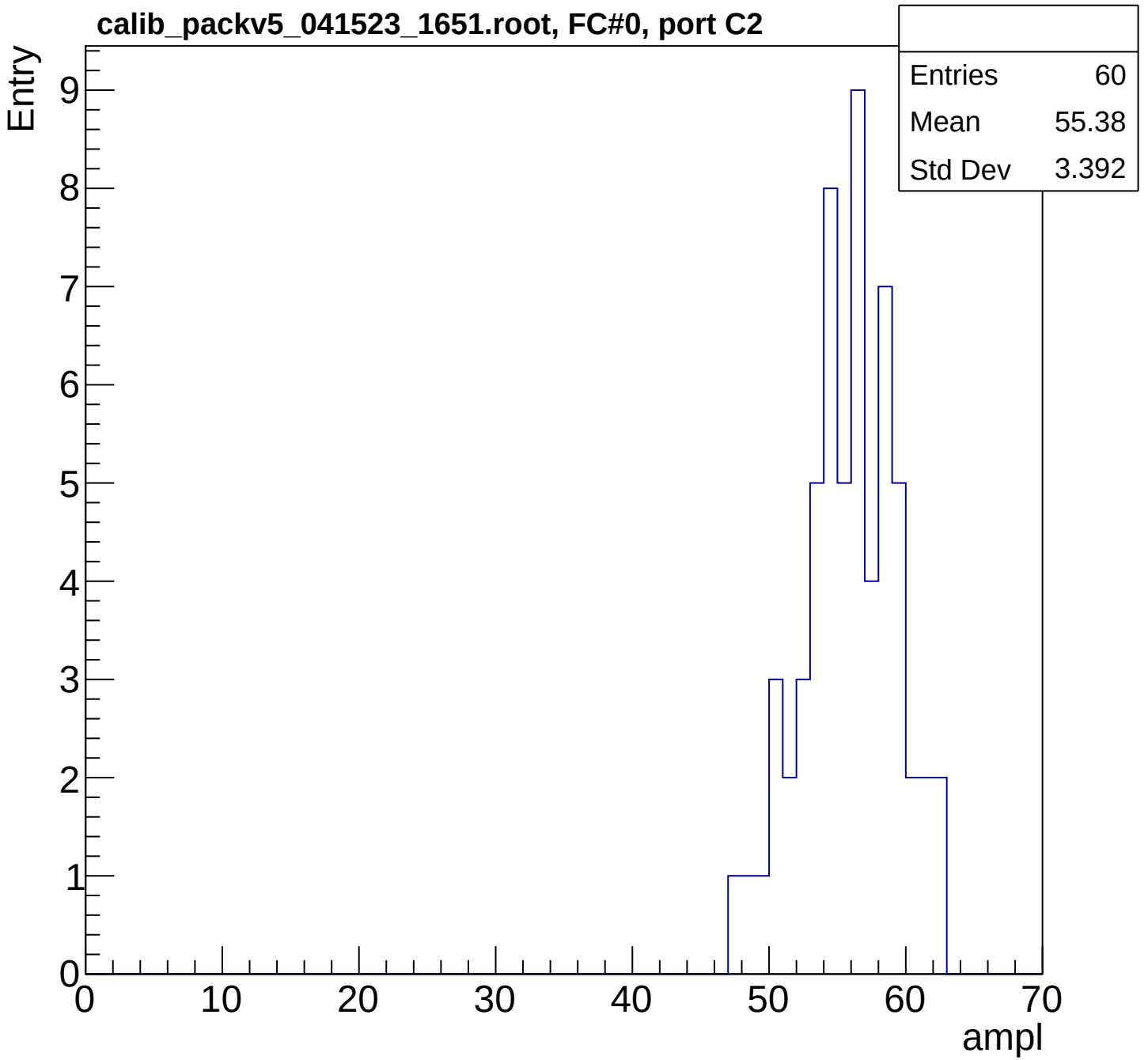

B1L103S, U24-ch77, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 49.25
Std Dev 3.243
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U24-ch77, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 55.38
Std Dev 3.392
Entry
ampl
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2
3
4
5
6
7
8
9
0
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40
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60
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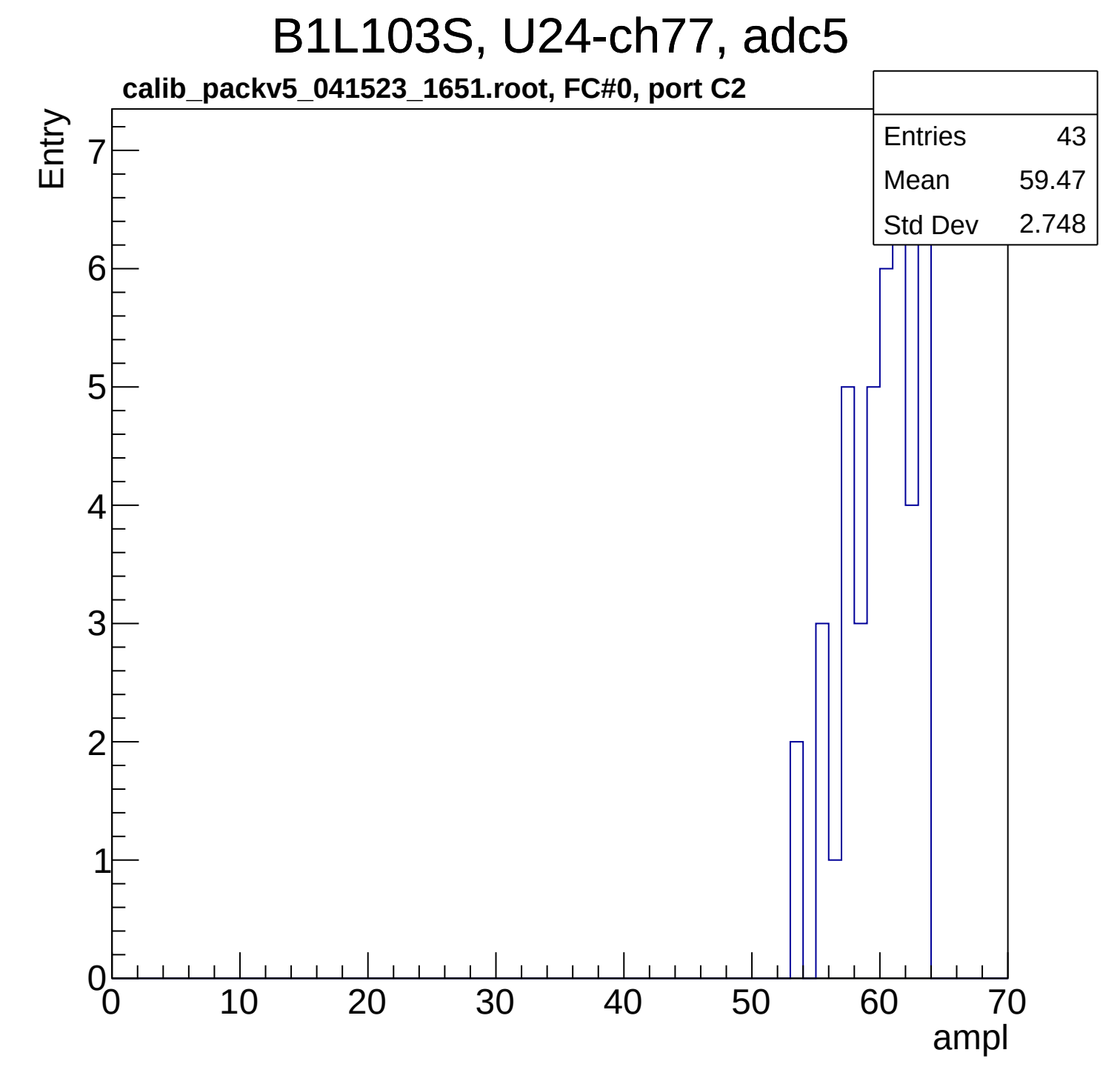
B1L103S, U24-ch77, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 43
Mean 59.47
Std Dev 2.748
Entry
ampl
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4
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6
7
0
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60
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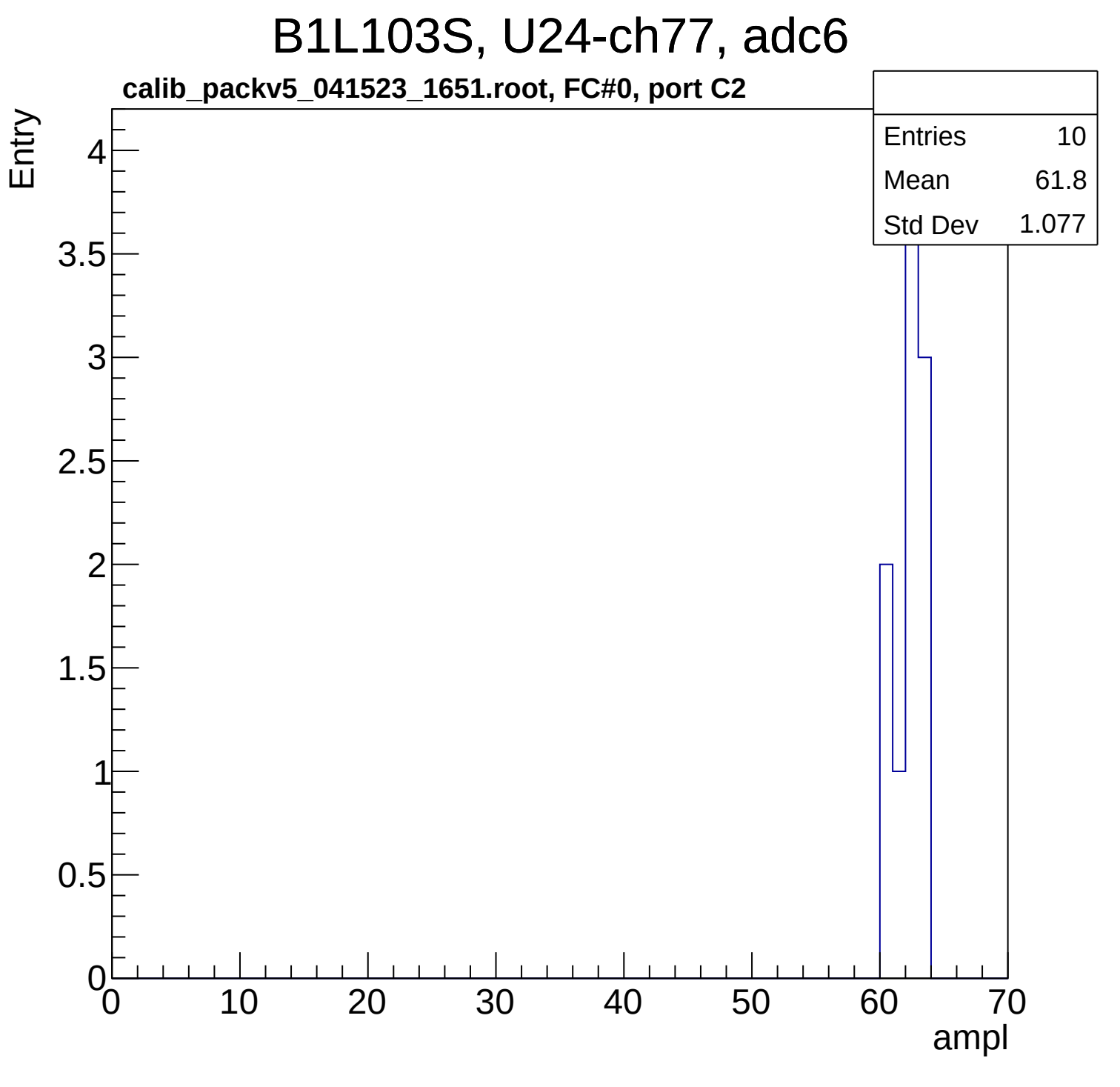
B1L103S, U24-ch77, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 61.8
Std Dev 1.077
Entry
ampl
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0.5
1
1.5
2
2.5
3
3.5
4
0
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40
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60
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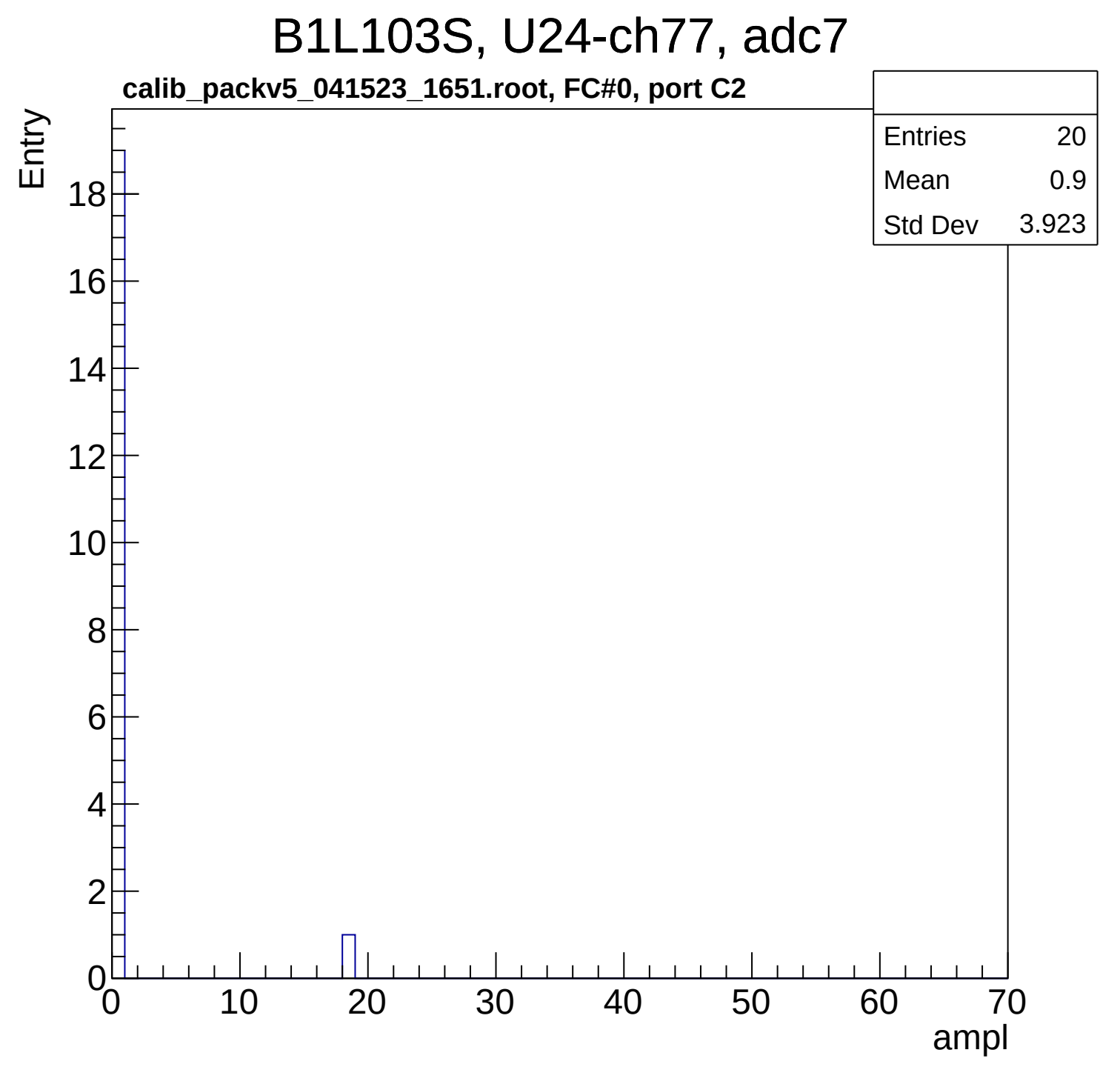
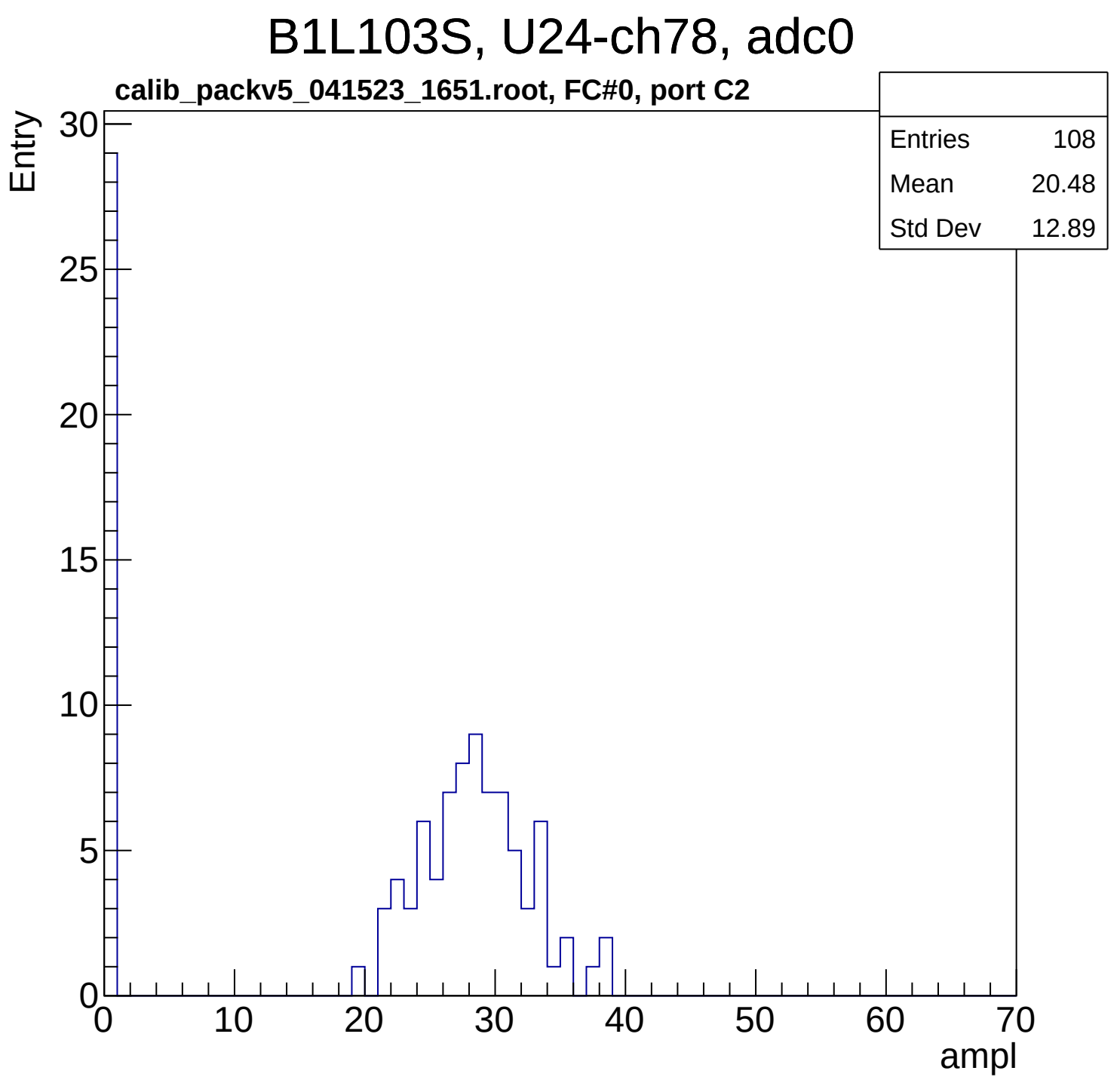

B1L103S, U24-ch77, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 0.9
Std Dev 3.923
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch78, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 108
Mean 20.48
Std Dev 12.89
Entry
ampl
0
5
10
15
20
25
30
0
10
20
30
40
50
60
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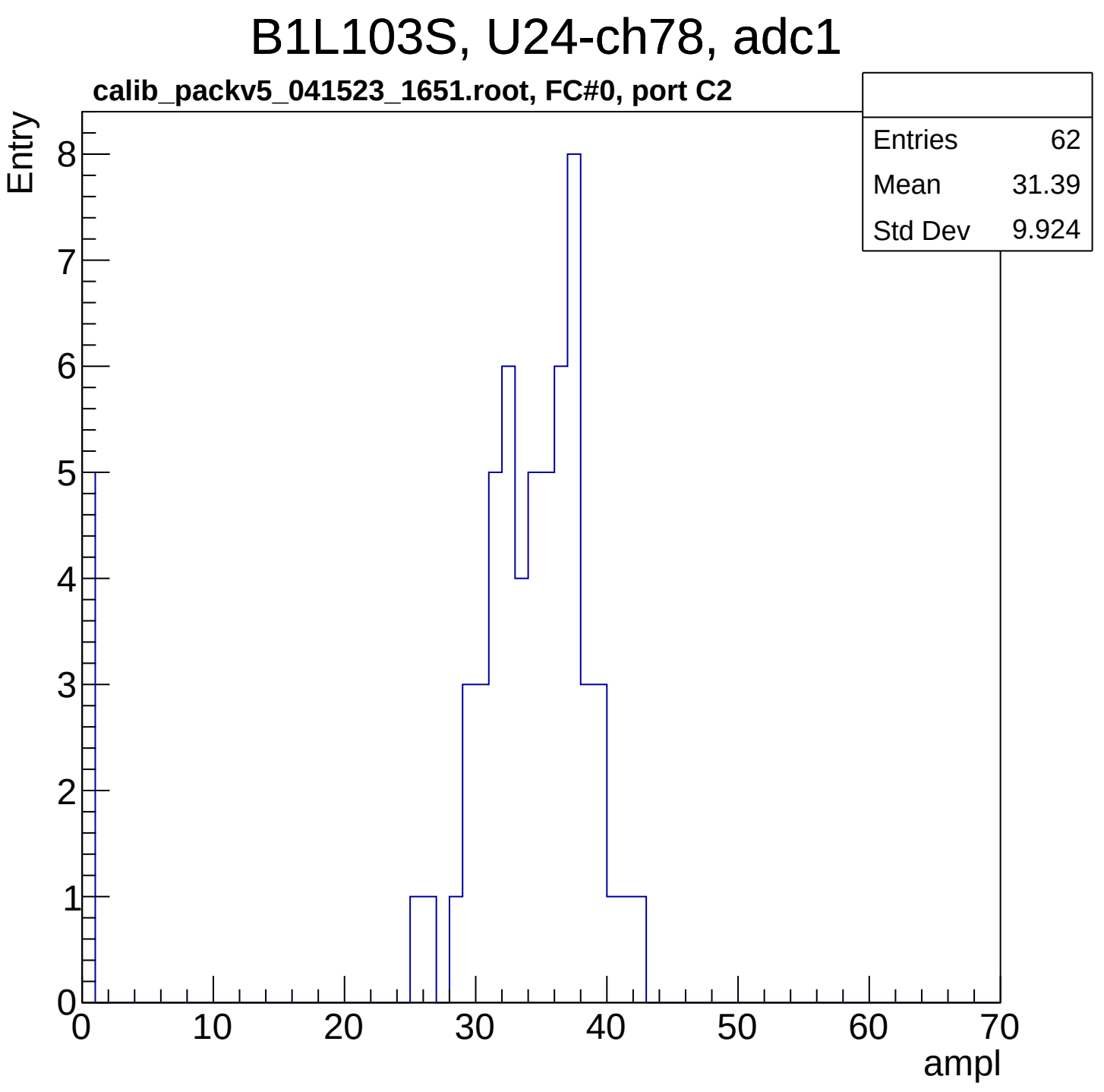
B1L103S, U24-ch78, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 31.39
Std Dev 9.924
Entry
ampl
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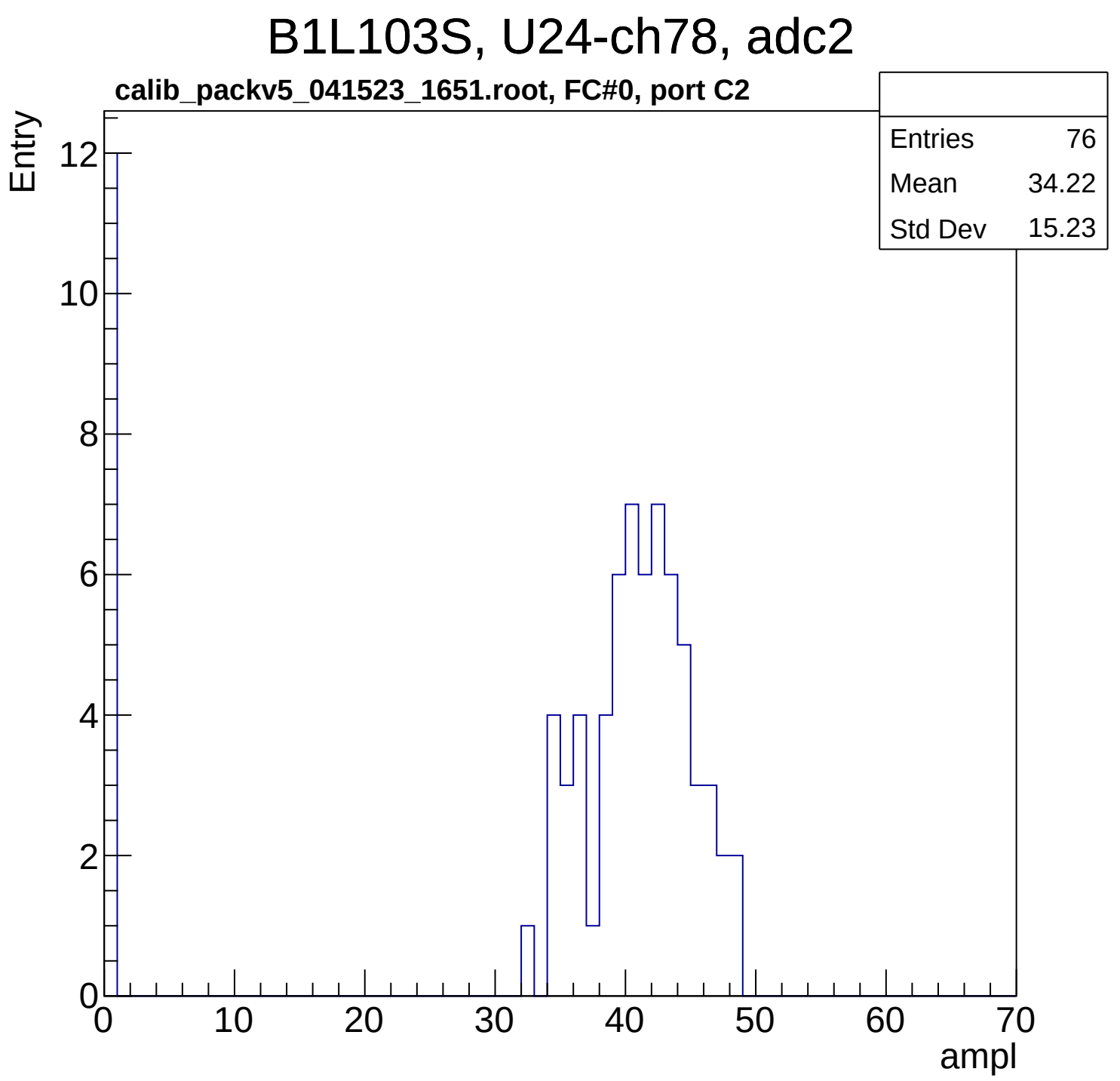
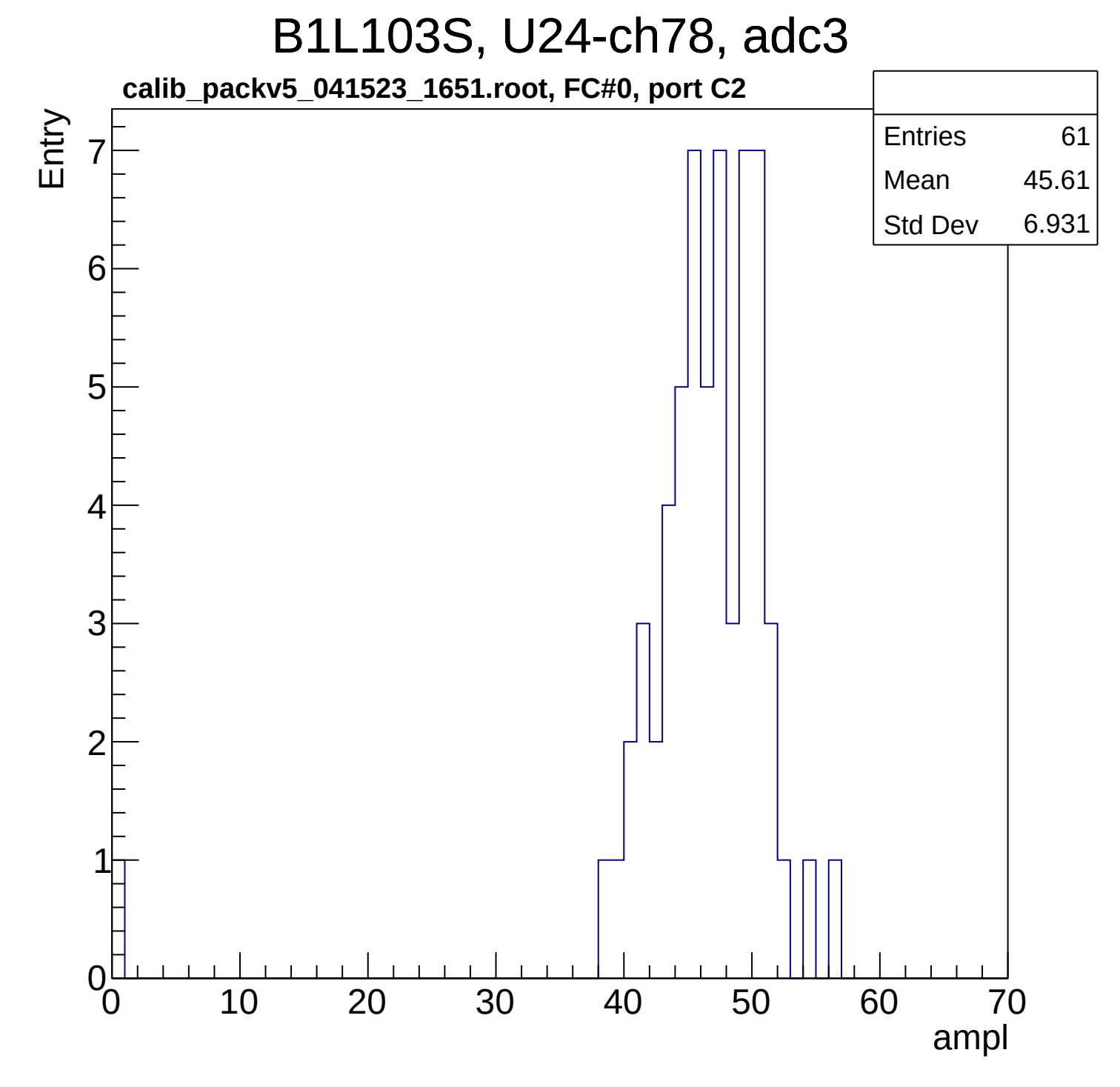
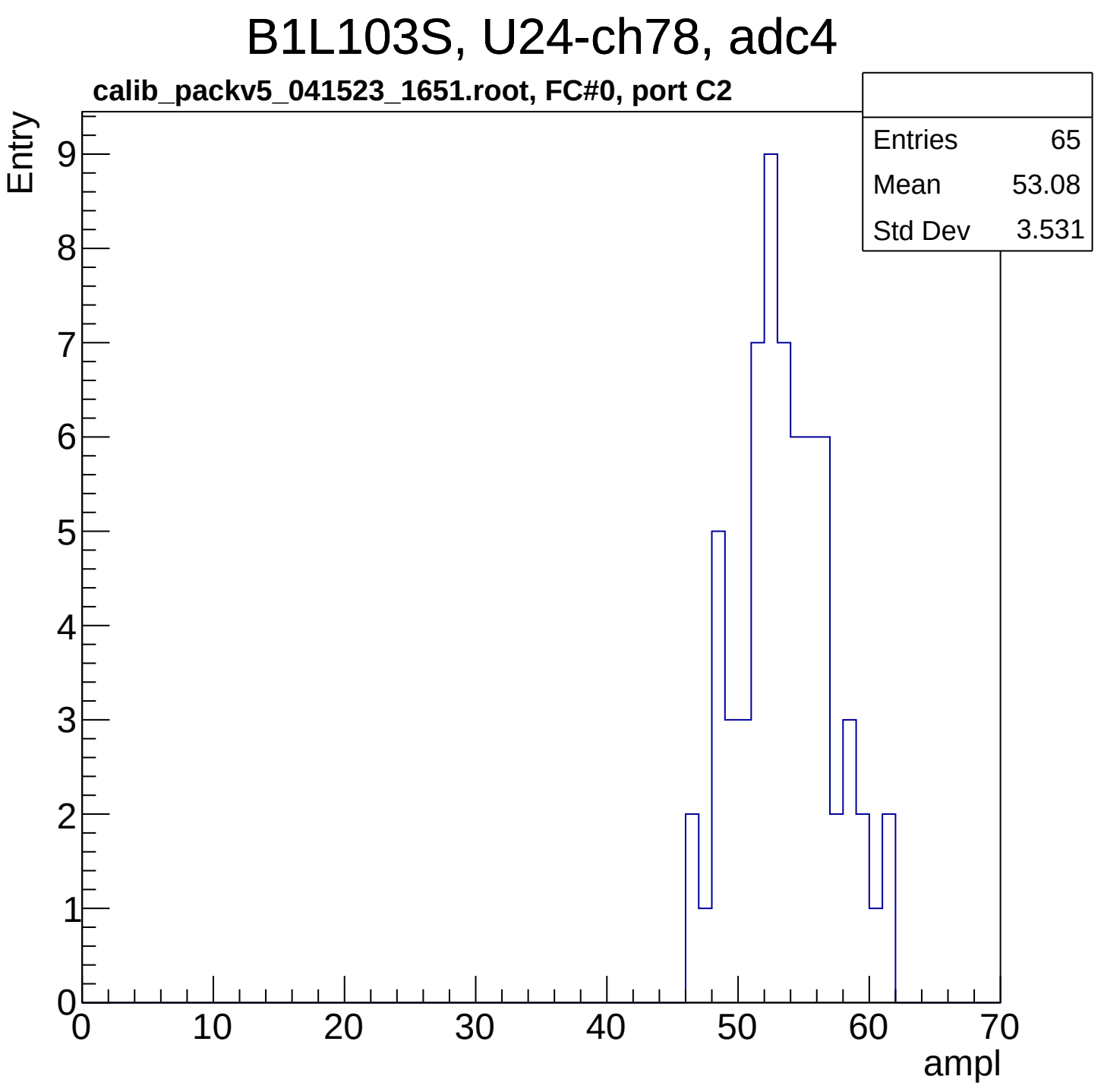
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U24-ch78, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 34.22
Std Dev 15.23
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch78, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 45.61
Std Dev 6.931
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U24-ch78, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 53.08
Std Dev 3.531
Entry
ampl
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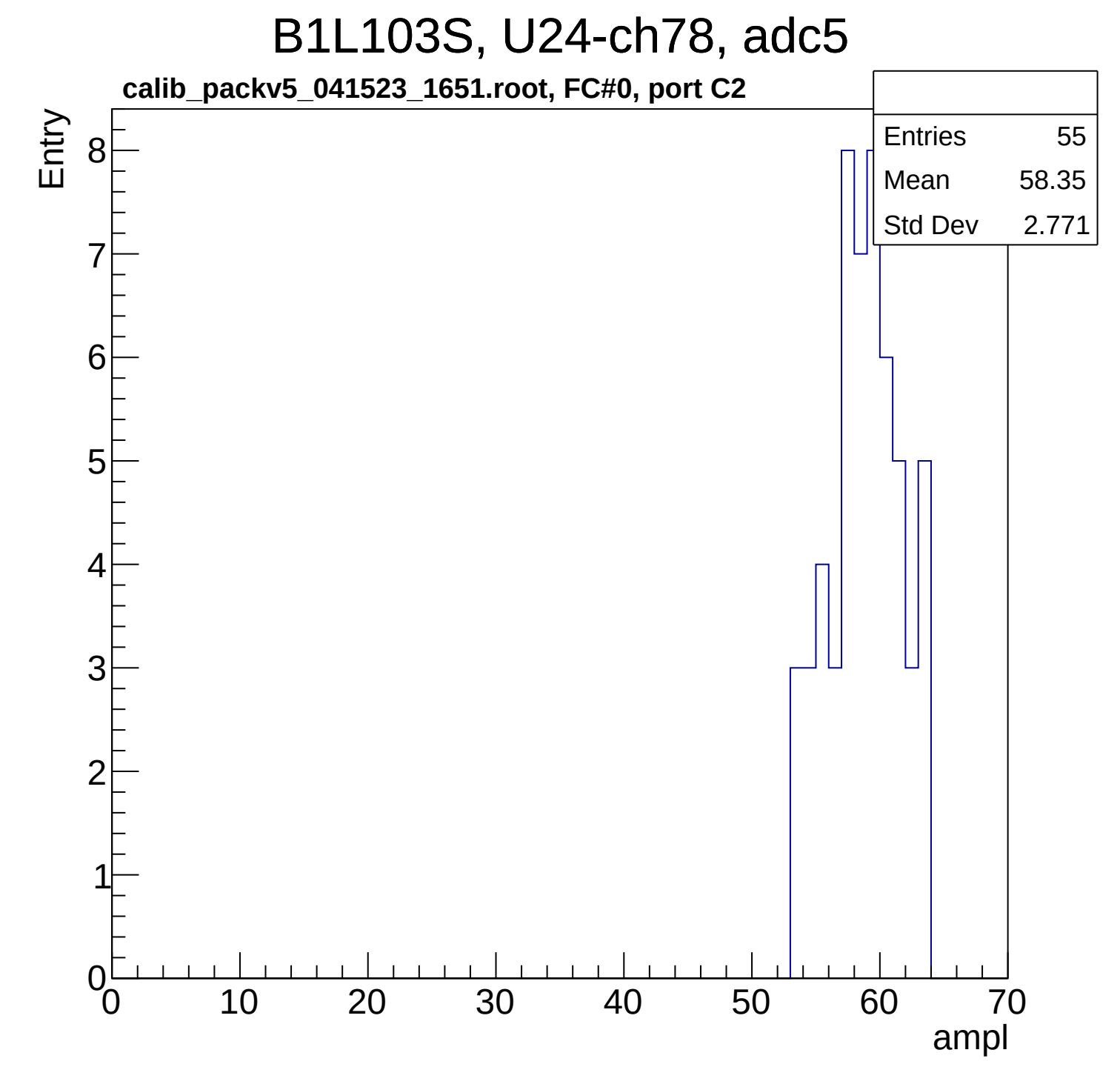
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U24-ch78, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 58.35
Std Dev 2.771
Entry
ampl
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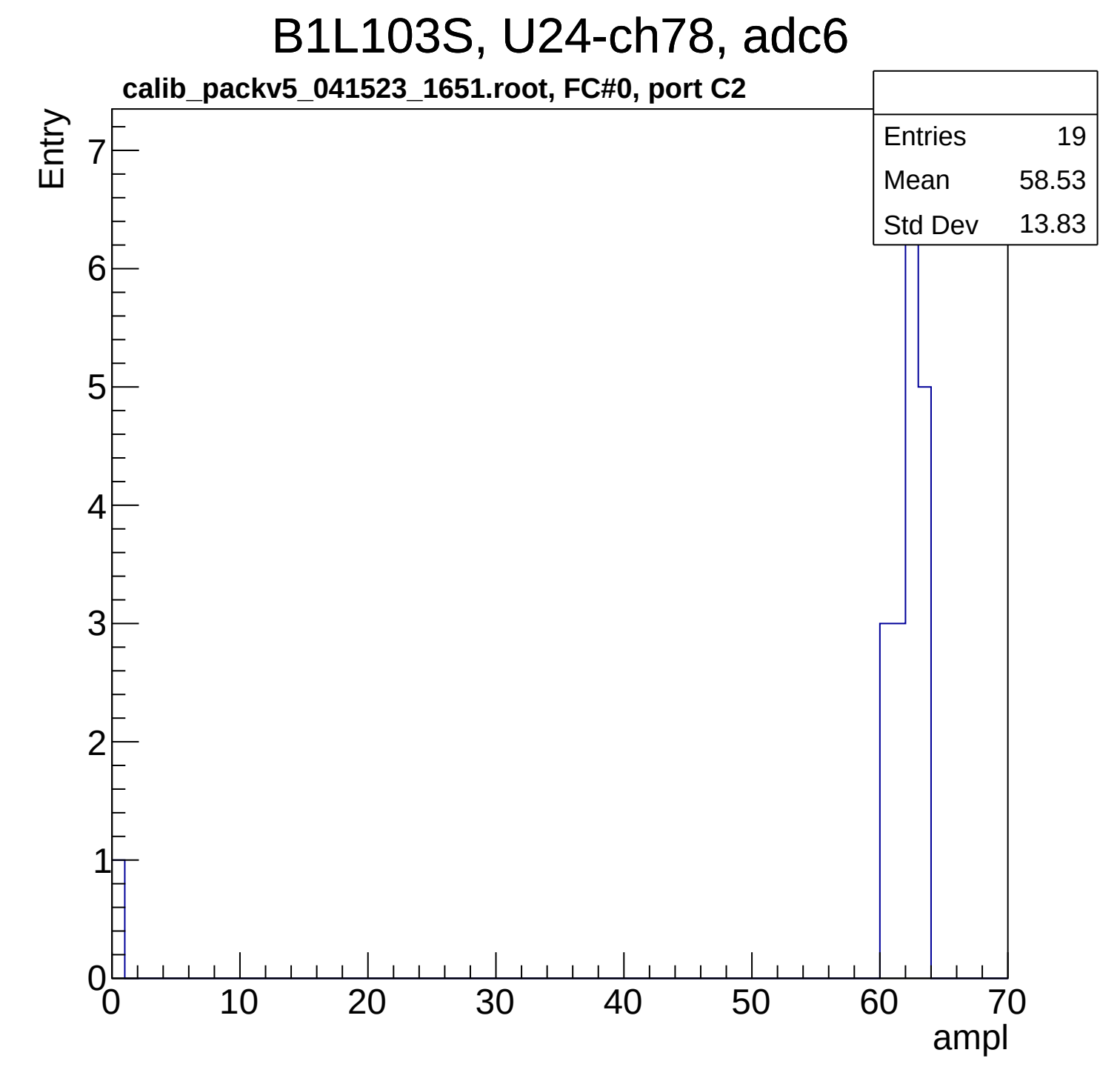
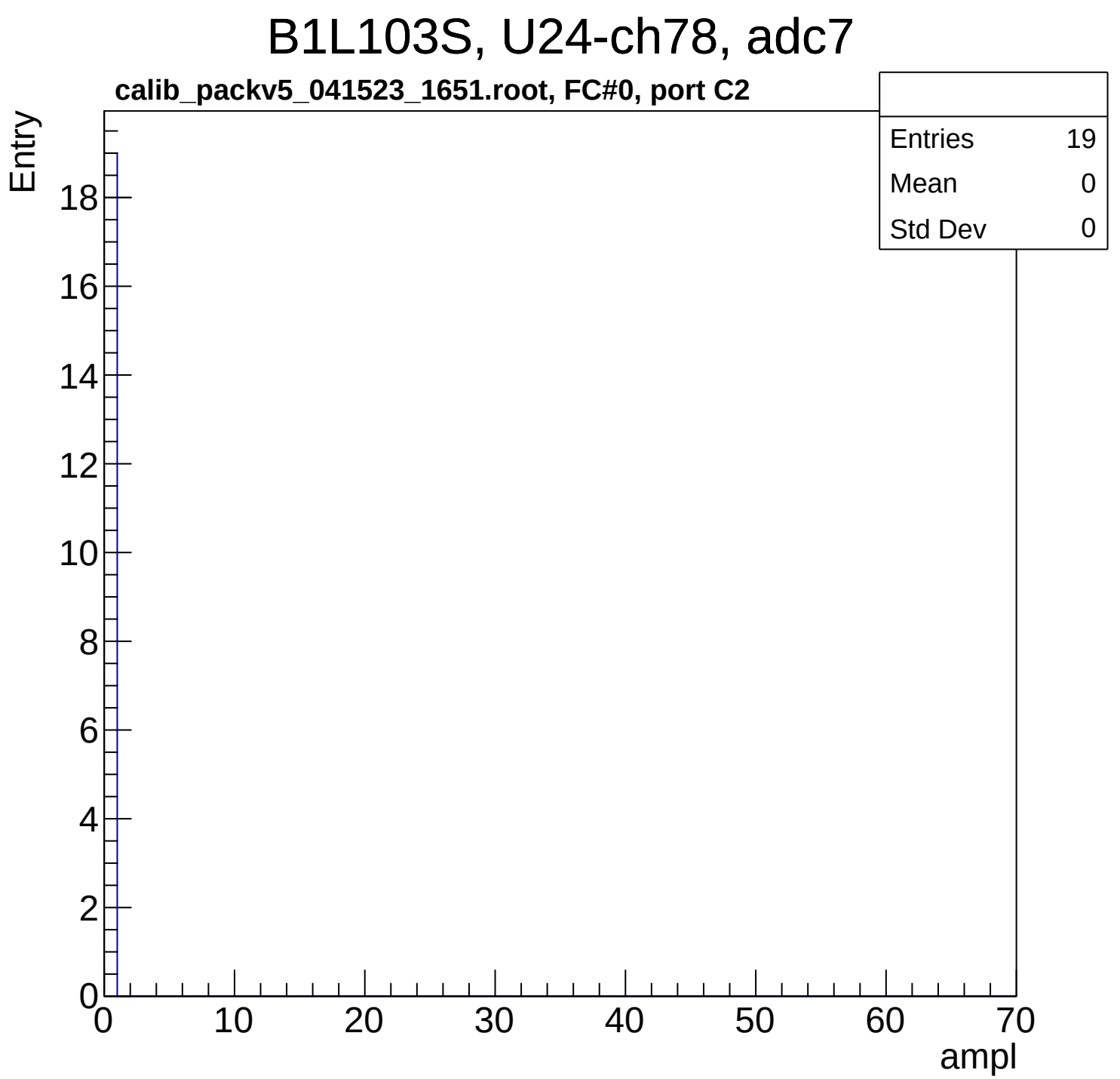
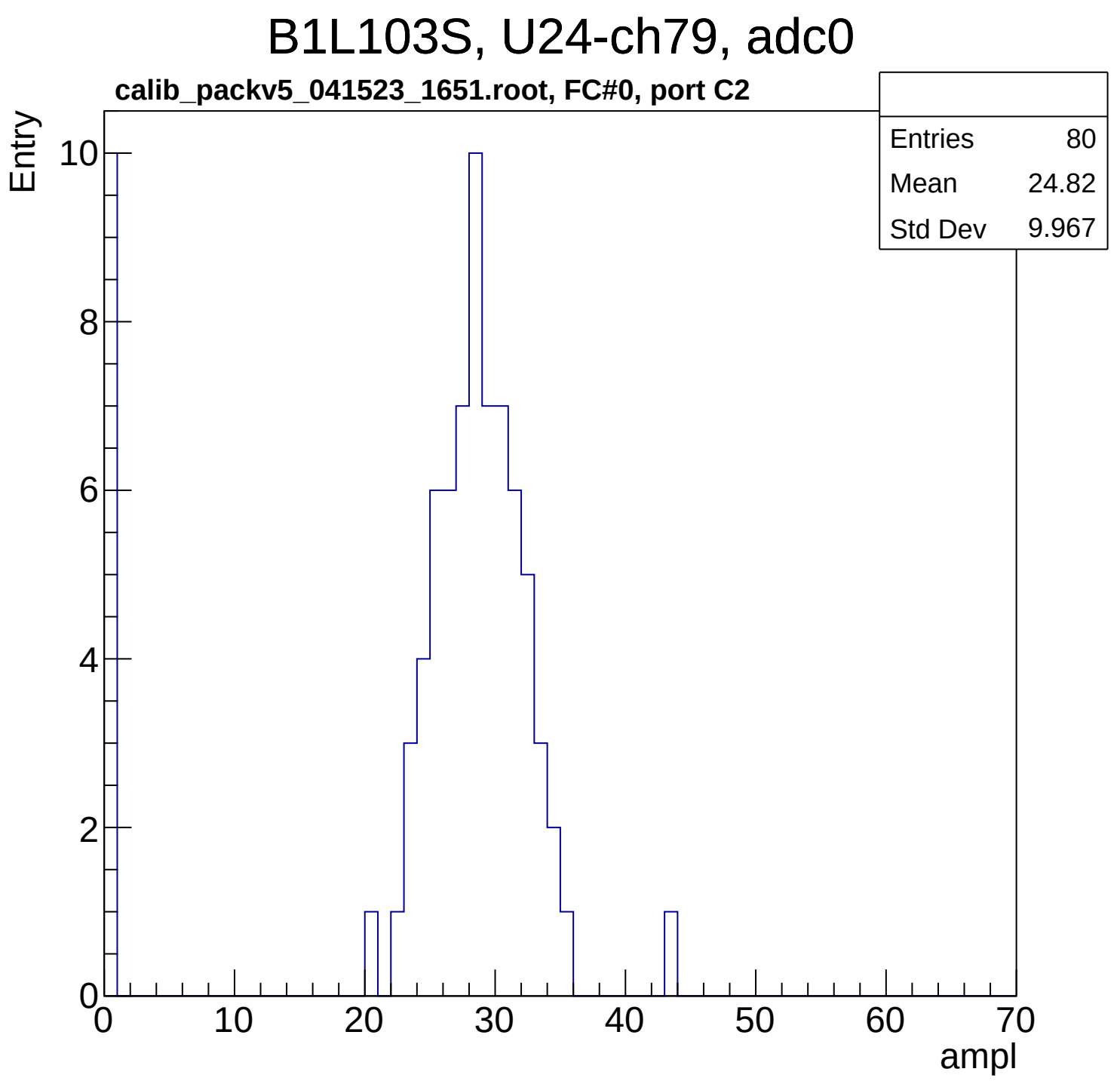
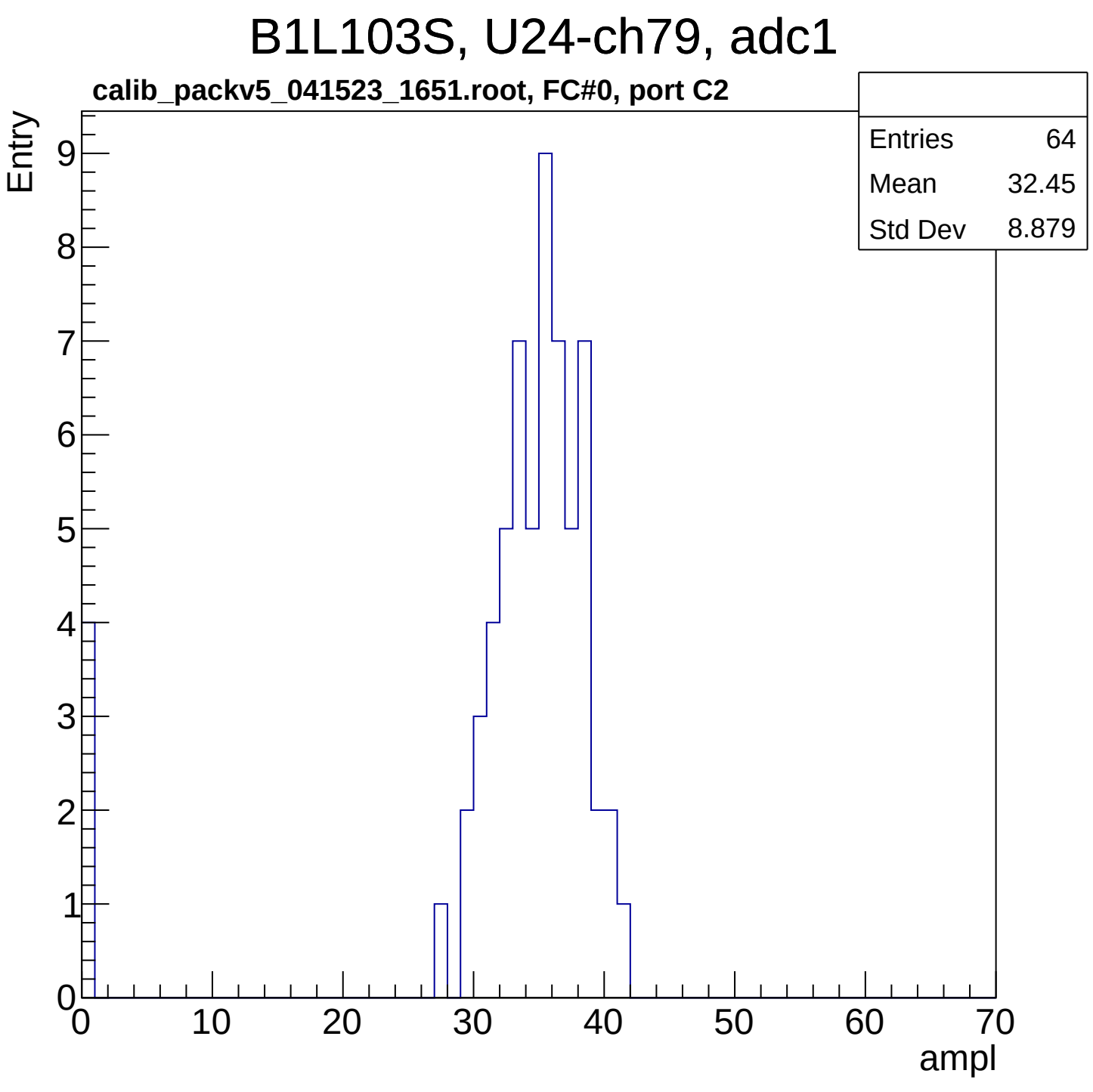
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U24-ch78, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 58.53
Std Dev 13.83
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U24-ch78, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch79, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 24.82
Std Dev 9.967
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch79, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 32.45
Std Dev 8.879
Entry
ampl
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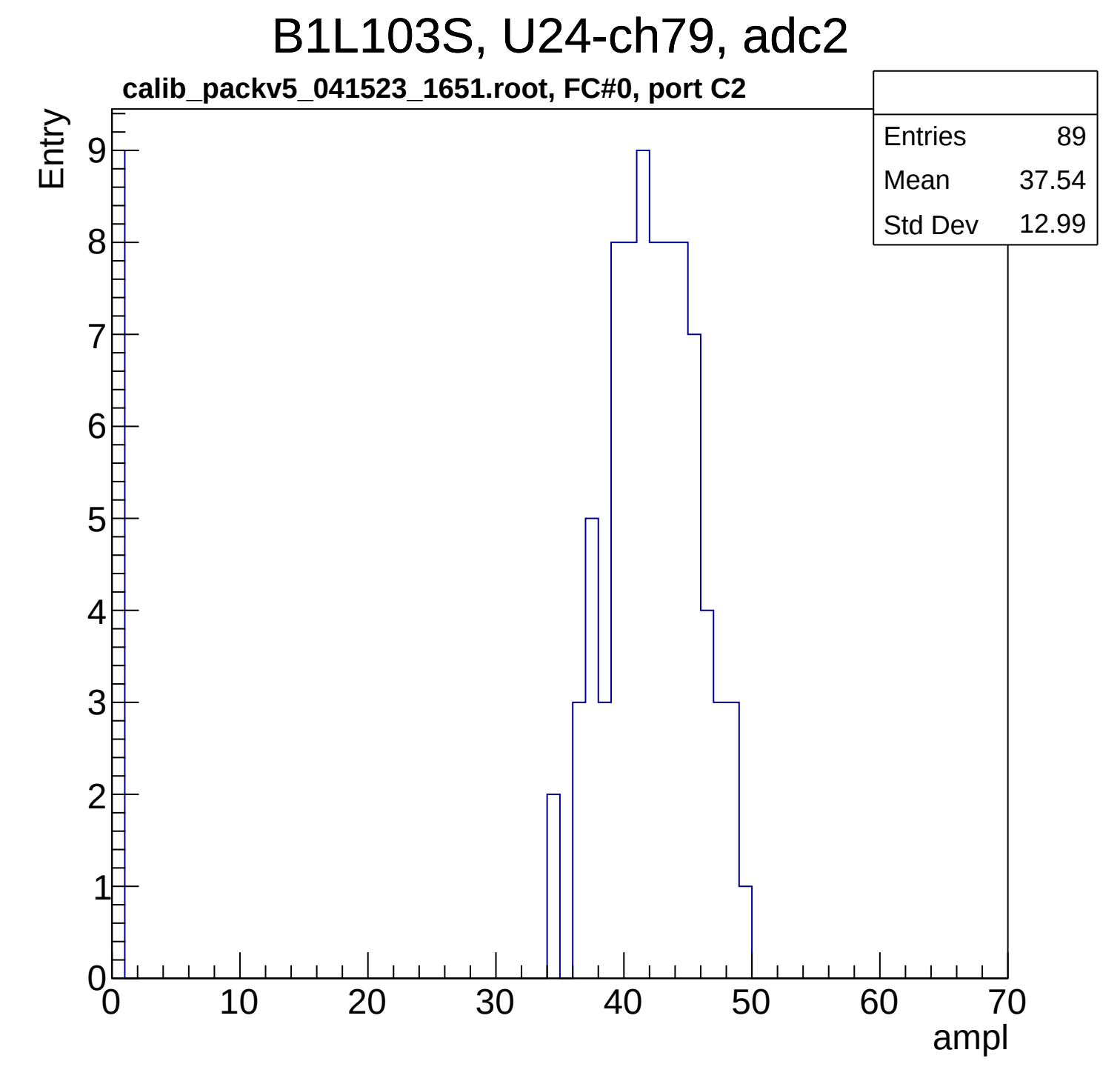
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U24-ch79, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 89
Mean 37.54
Std Dev 12.99
Entry
ampl
0
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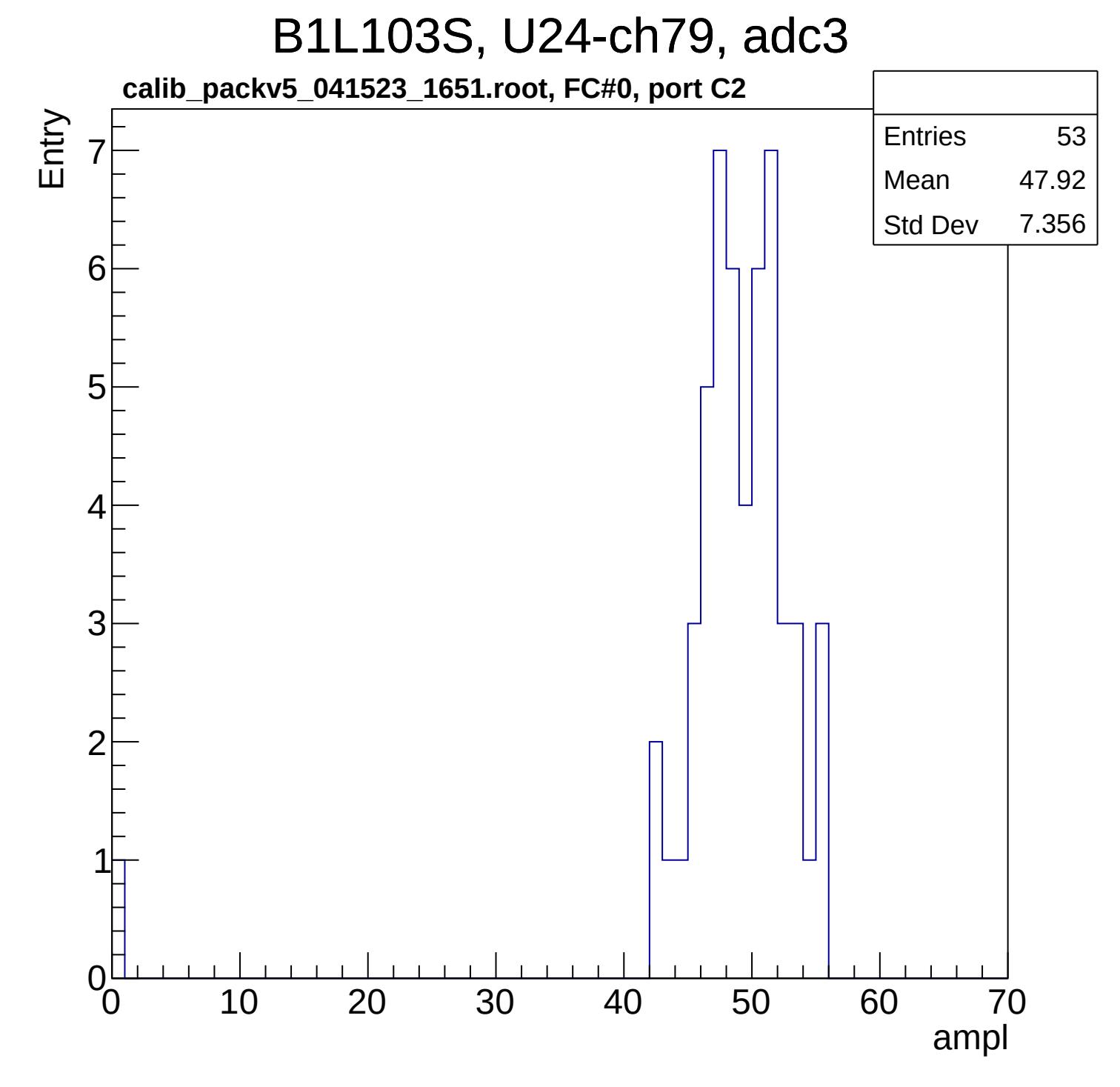
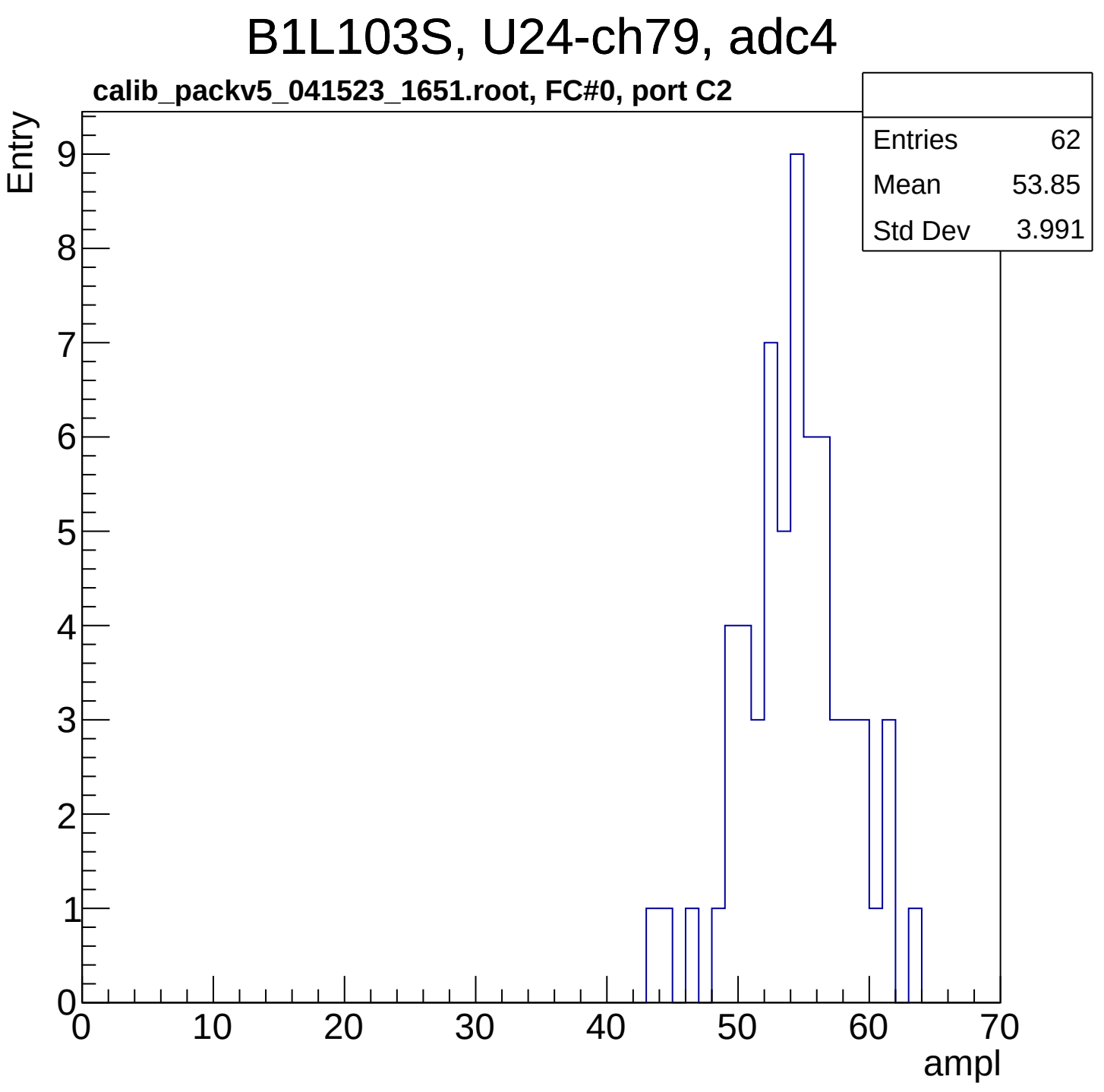
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U24-ch79, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 47.92
Std Dev 7.356
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U24-ch79, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 53.85
Std Dev 3.991
Entry
ampl
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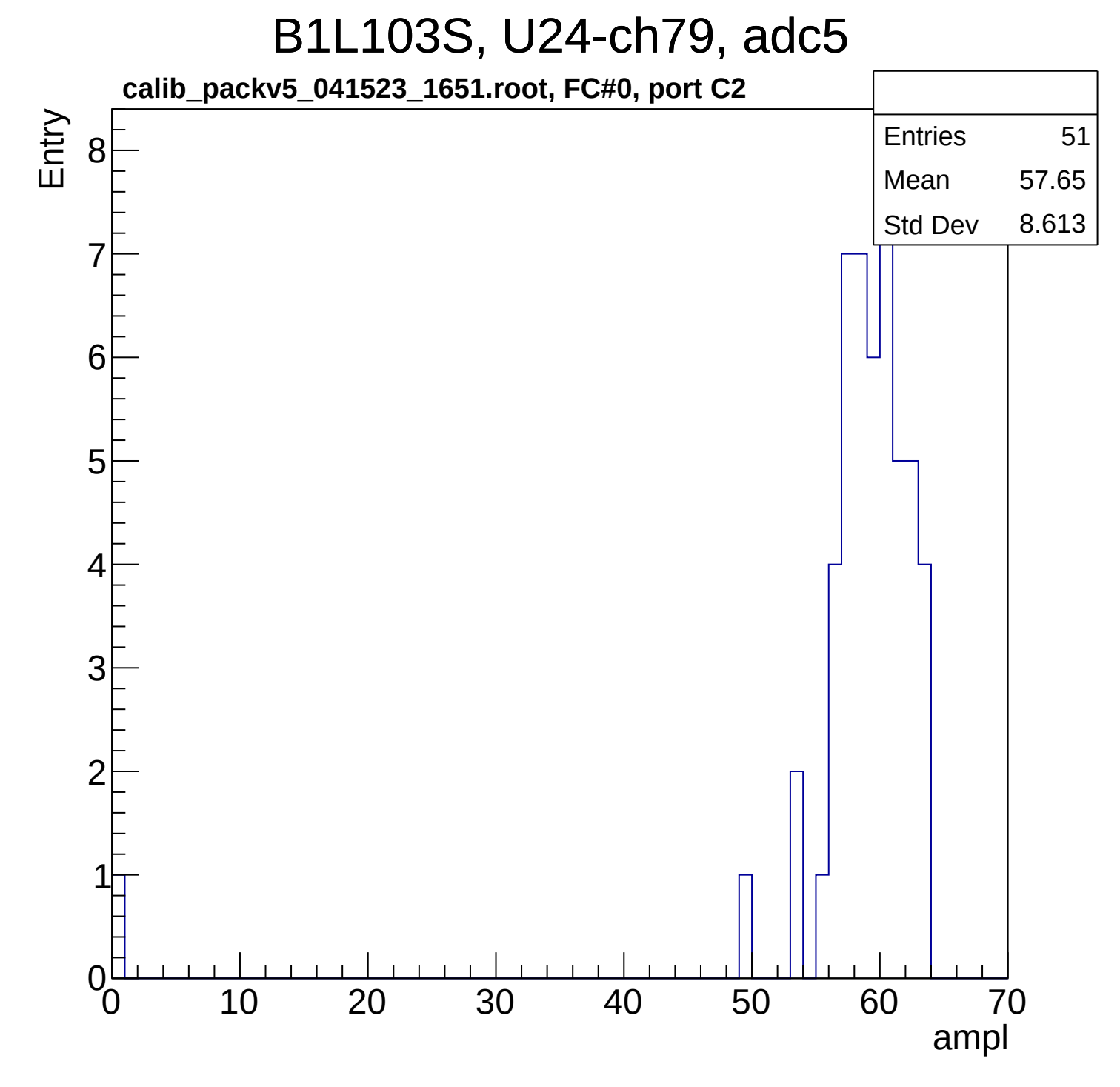
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U24-ch79, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 57.65
Std Dev 8.613
Entry
ampl
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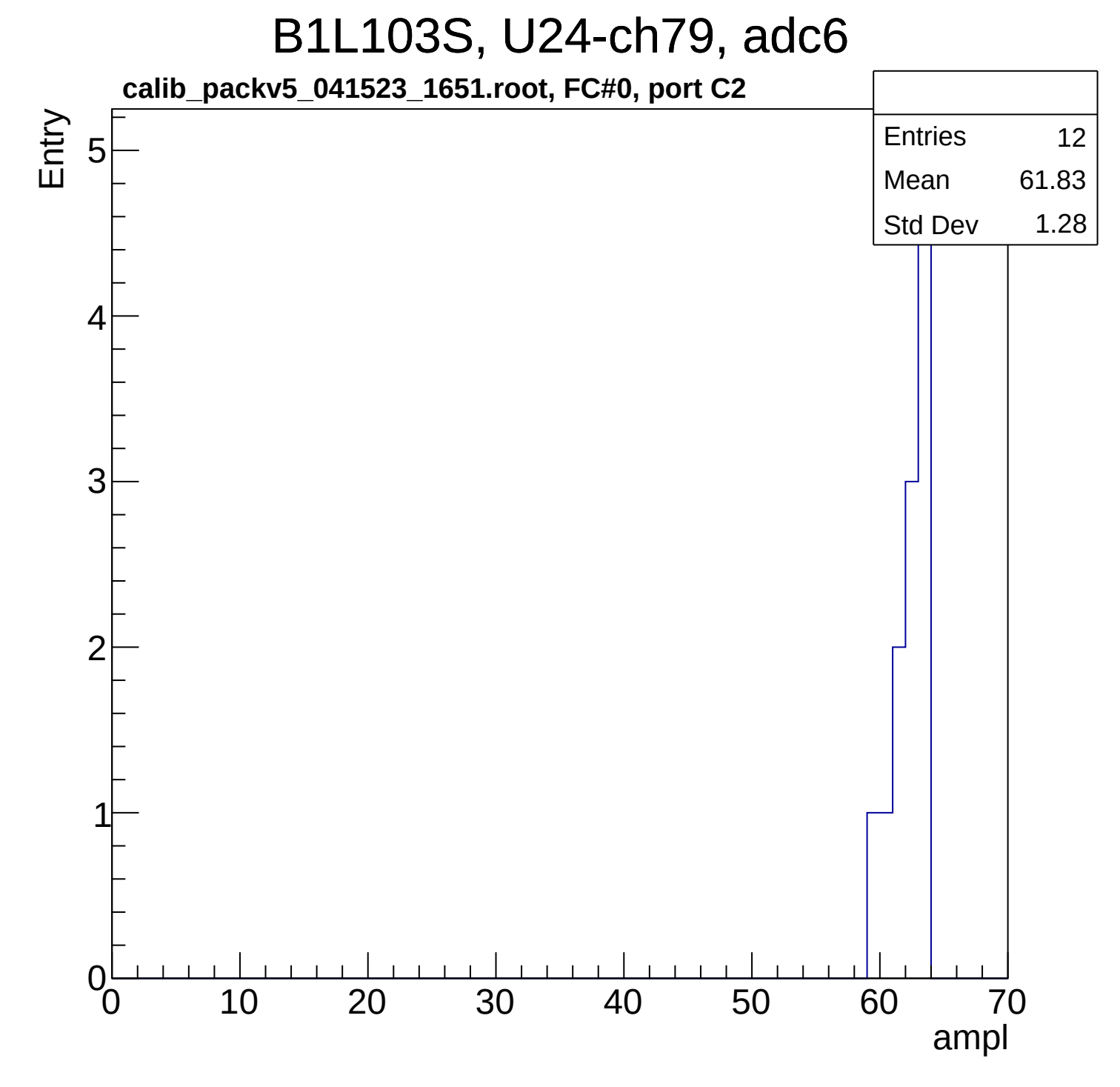
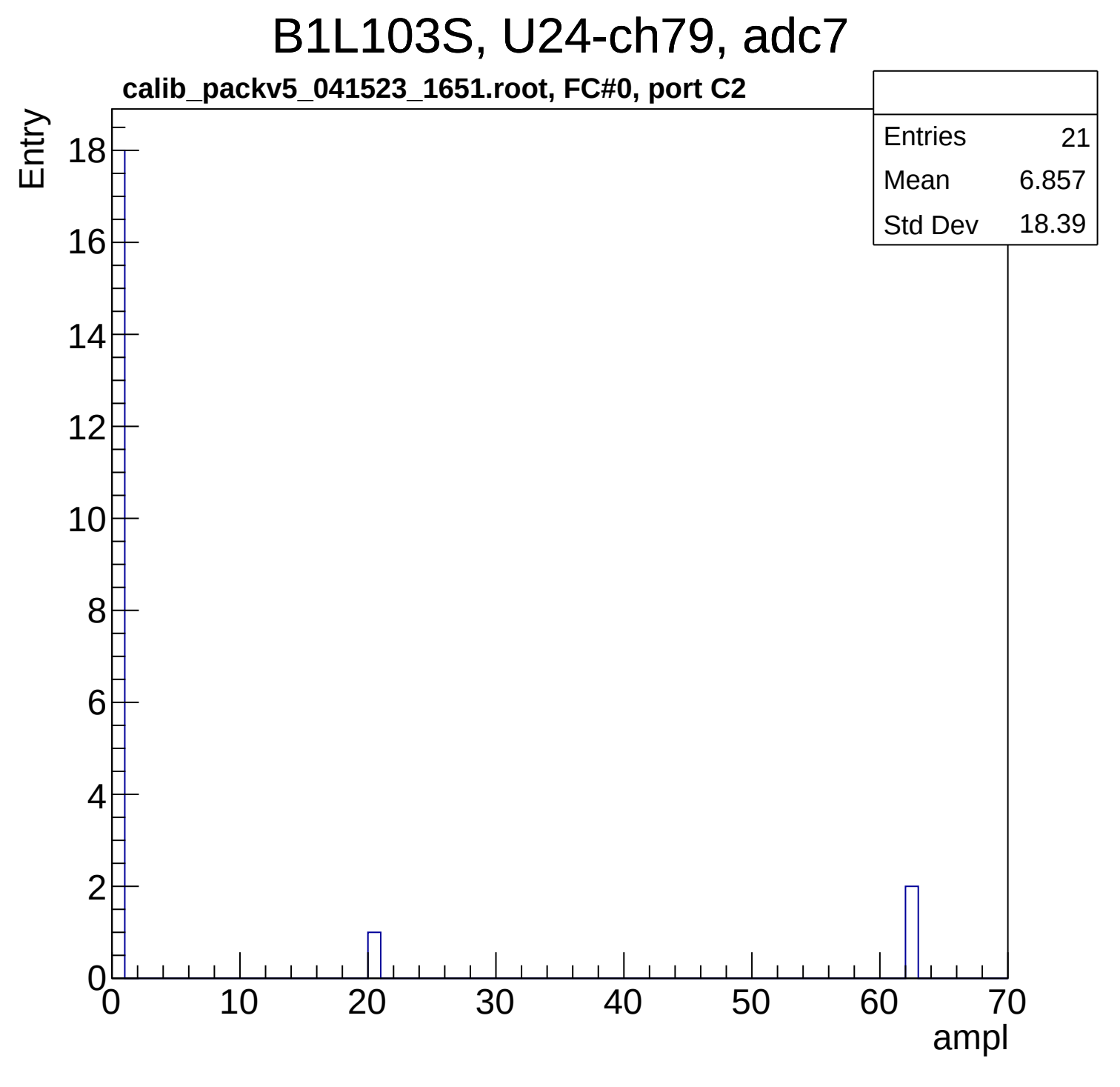
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U24-ch79, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 61.83
Std Dev 1.28
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch79, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 6.857
Std Dev 18.39
Entry
0
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4
6
8
10
12
14
16
18
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10
20
30
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50
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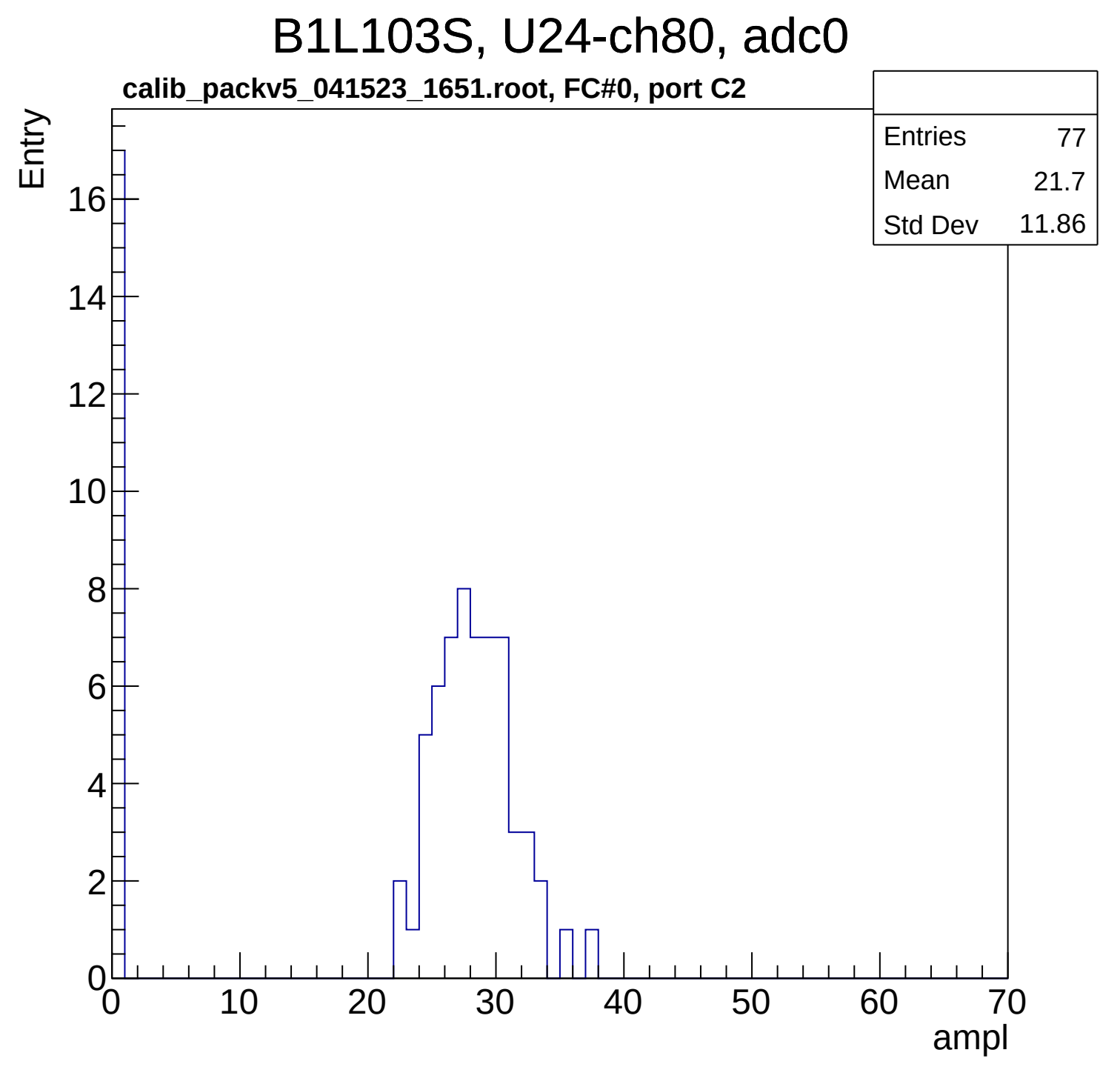
70
ampl


B1L103S, U24-ch80, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 21.7
Std Dev 11.86
Entry
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6
8
10
12
14
16
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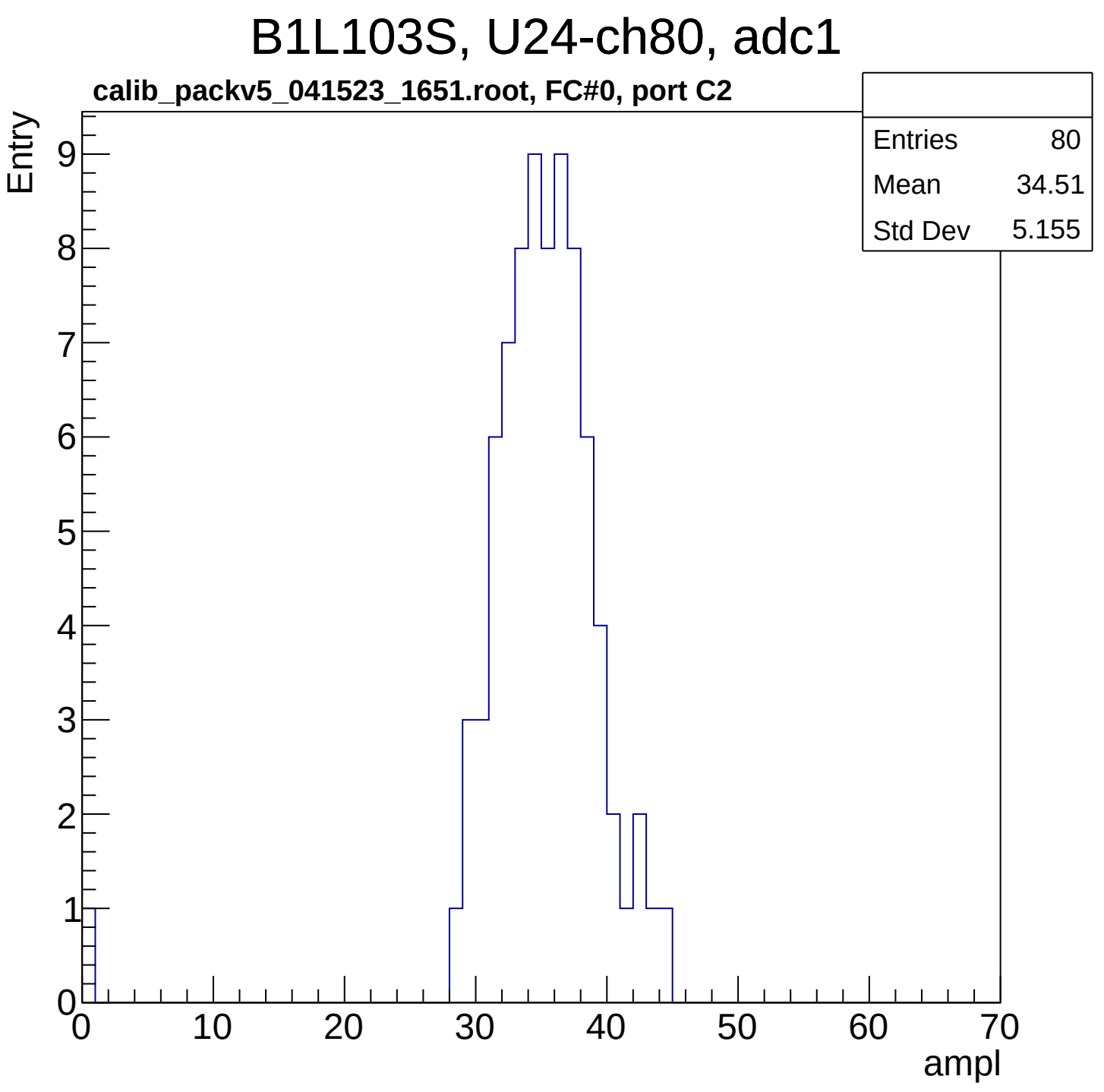
20
30
40
50
60
70
ampl


B1L103S, U24-ch80, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 34.51
Std Dev 5.155
Entry
ampl
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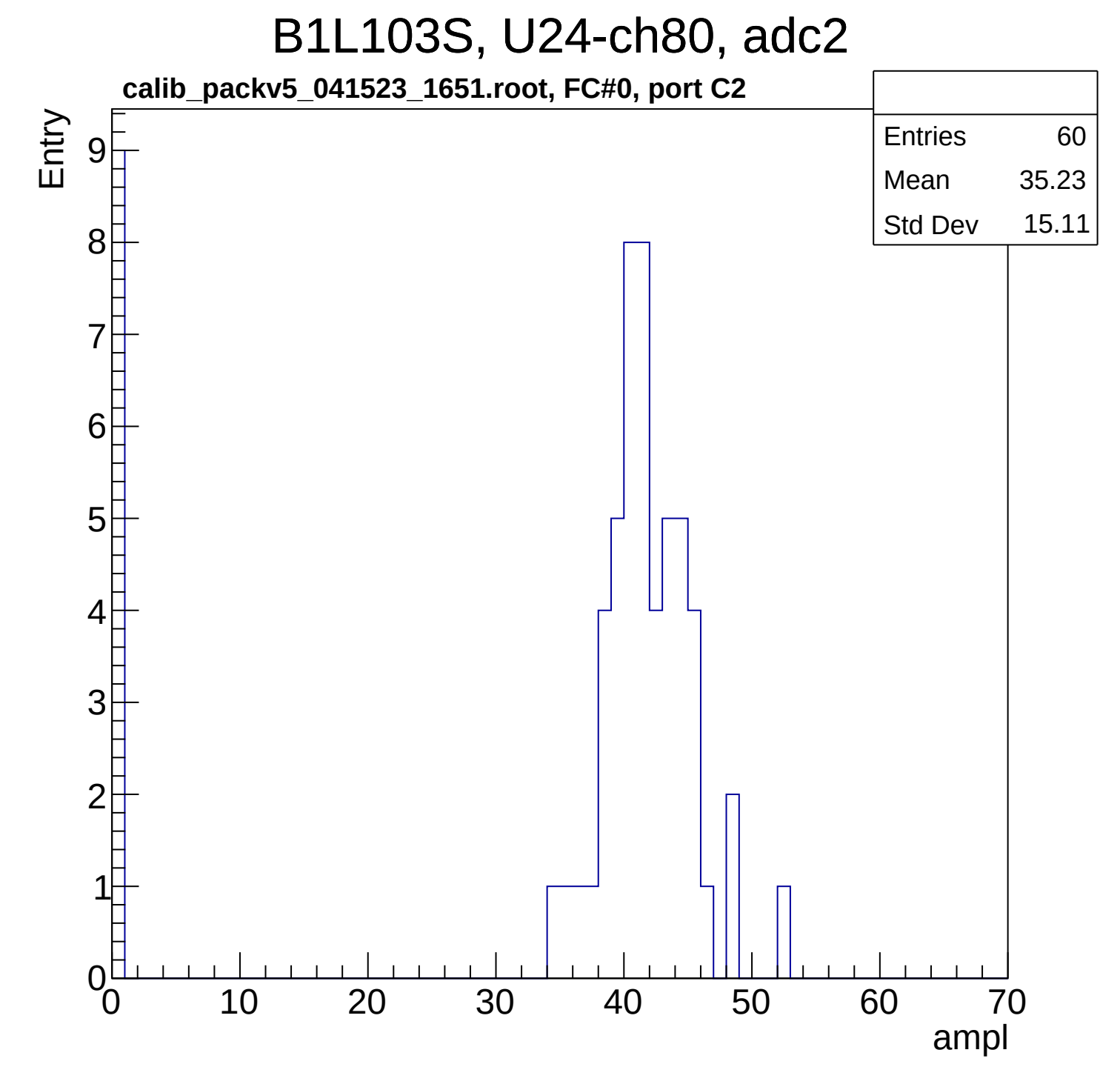
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U24-ch80, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 35.23
Std Dev 15.11
Entry
ampl
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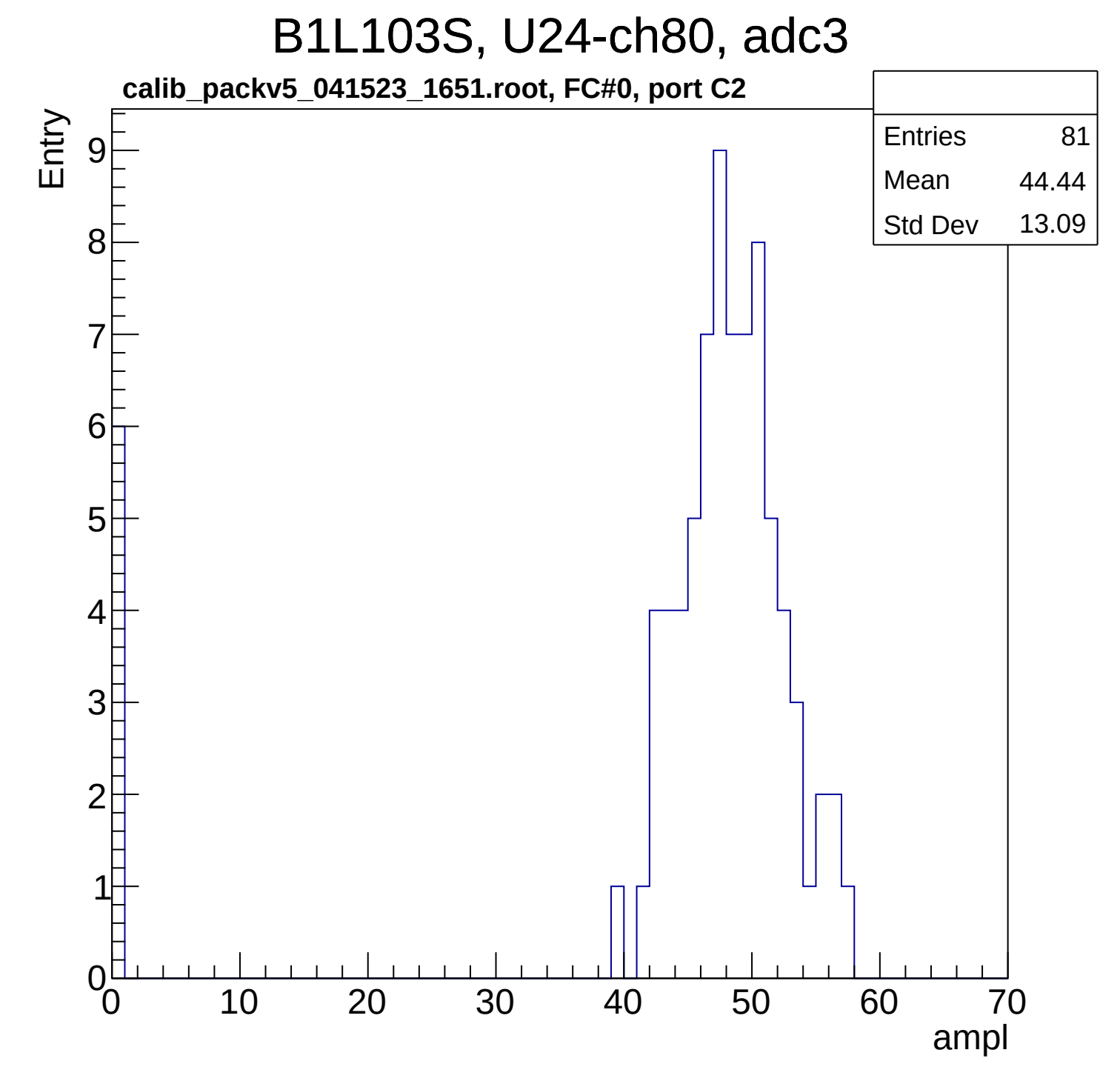
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U24-ch80, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 44.44
Std Dev 13.09
Entry
ampl
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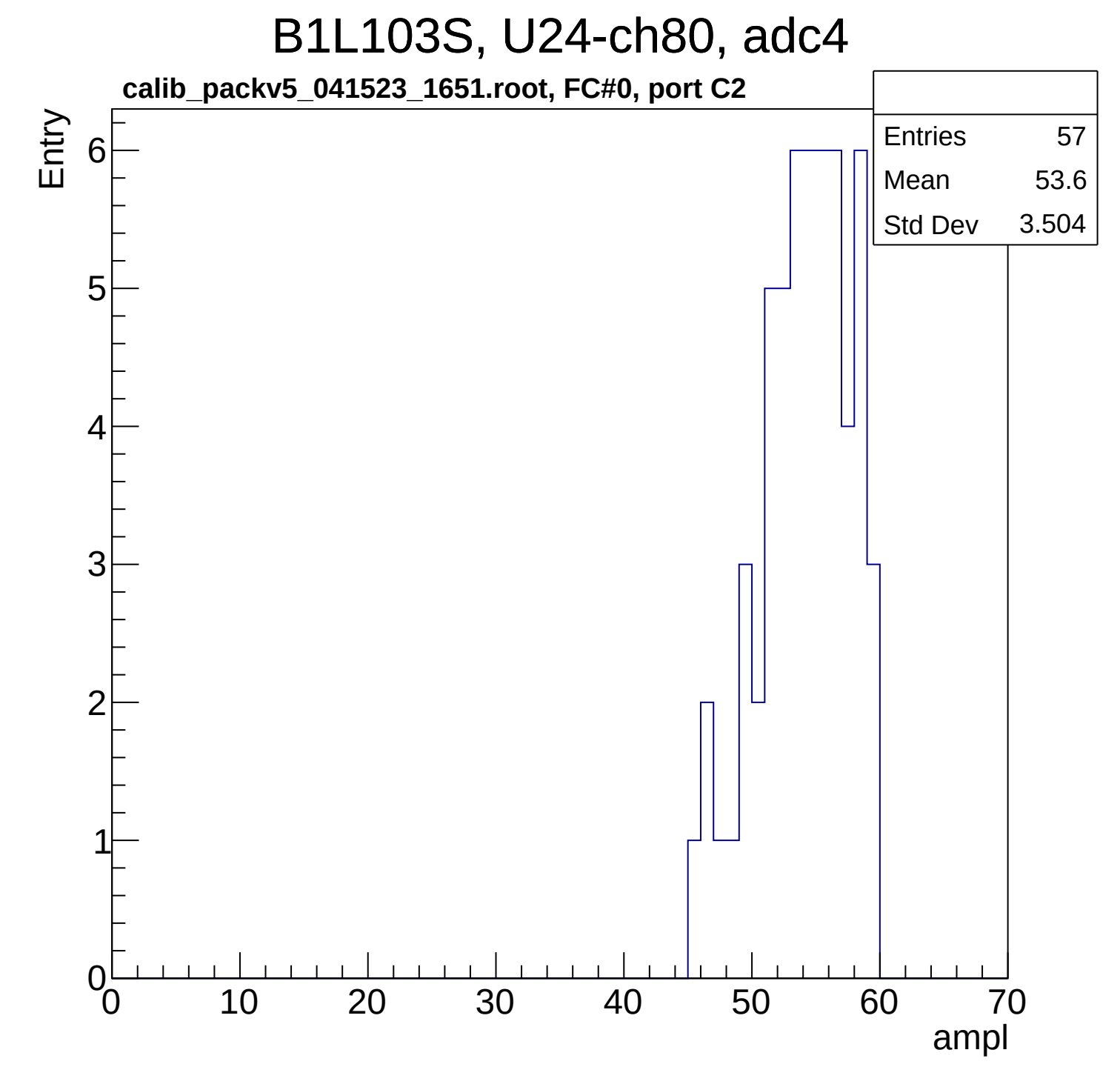
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U24-ch80, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 53.6
Std Dev 3.504
Entry
ampl
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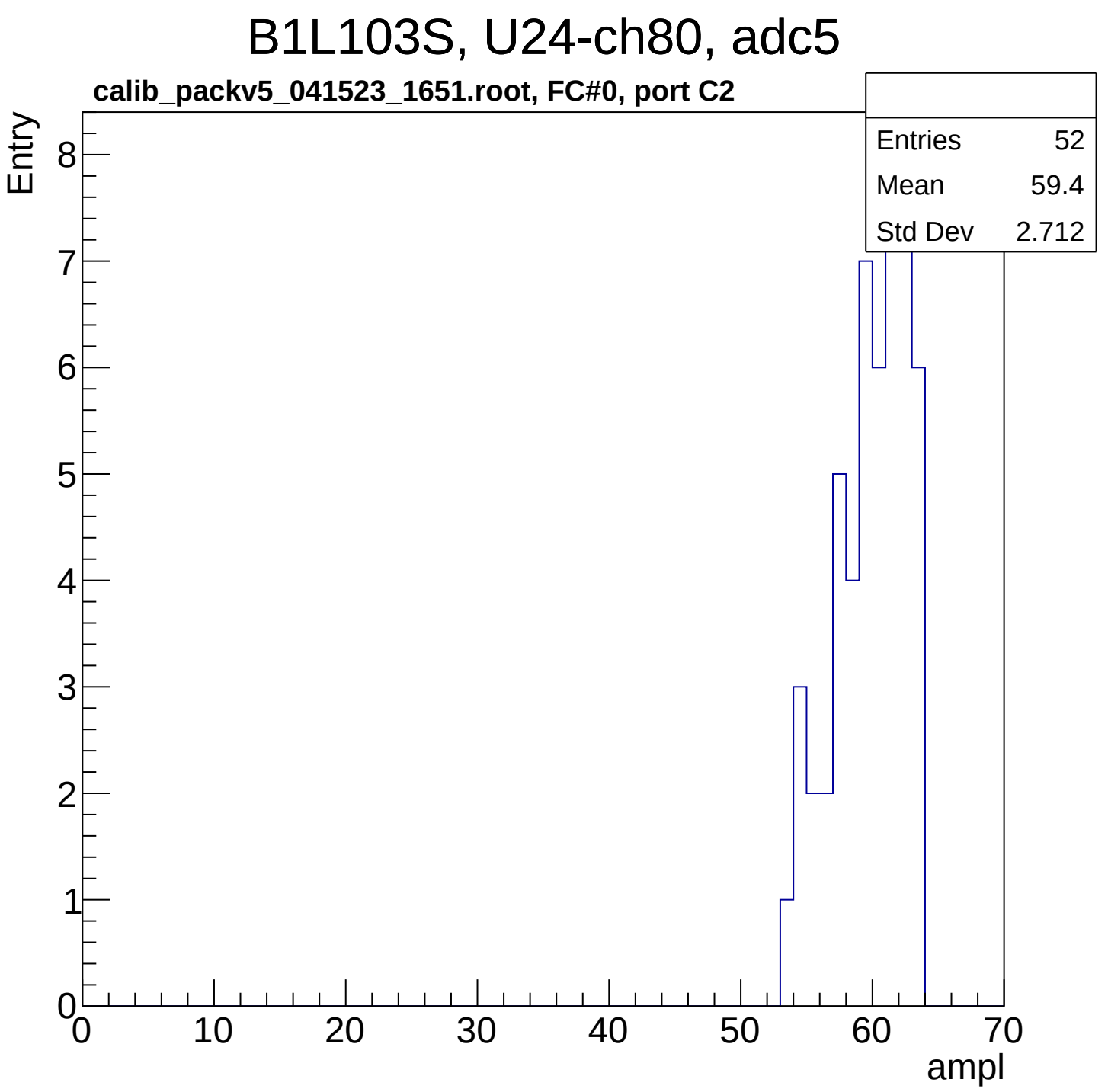
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U24-ch80, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 59.4
Std Dev 2.712
Entry
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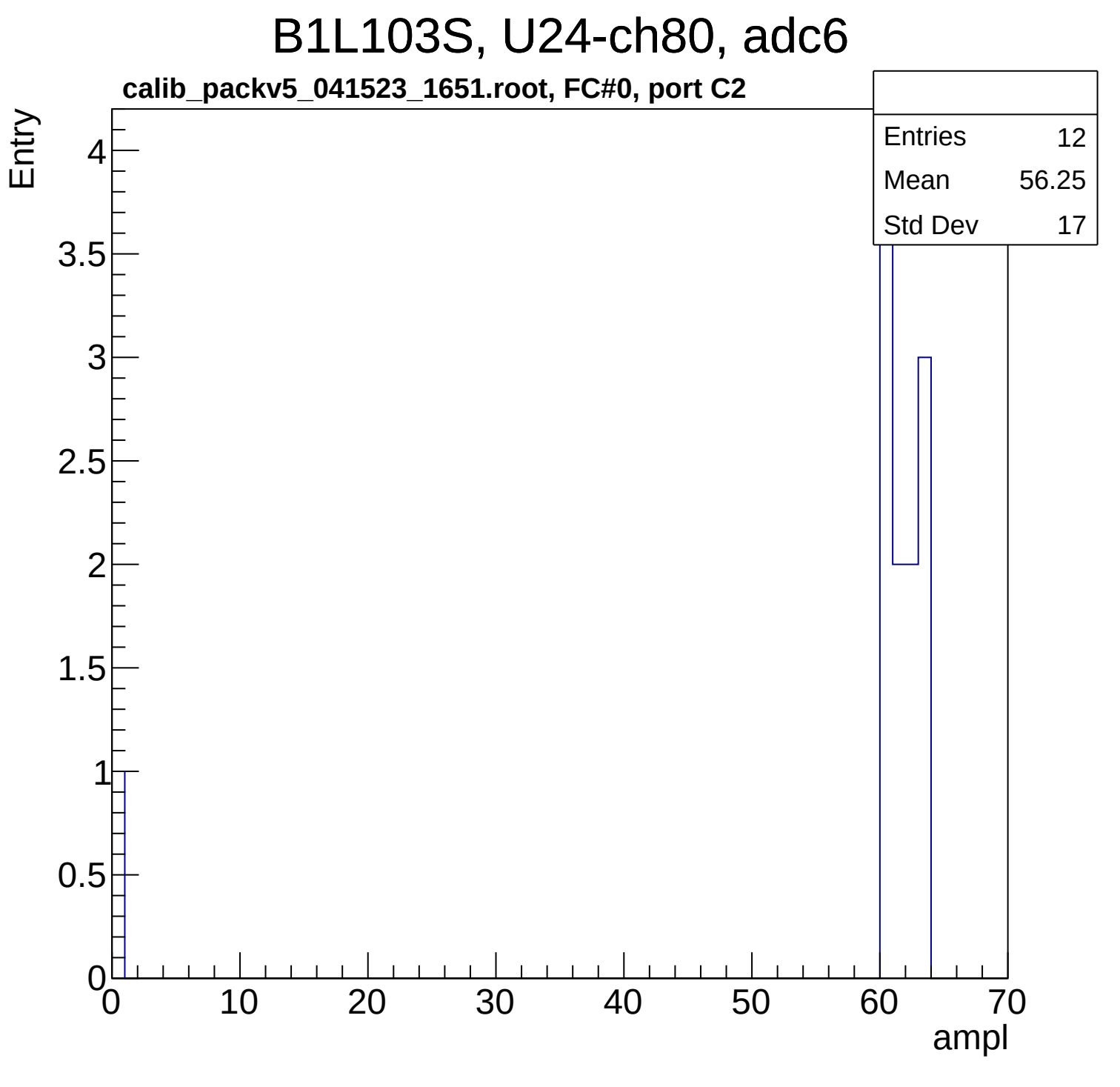
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch80, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 56.25
Std Dev 17
Entry
ampl
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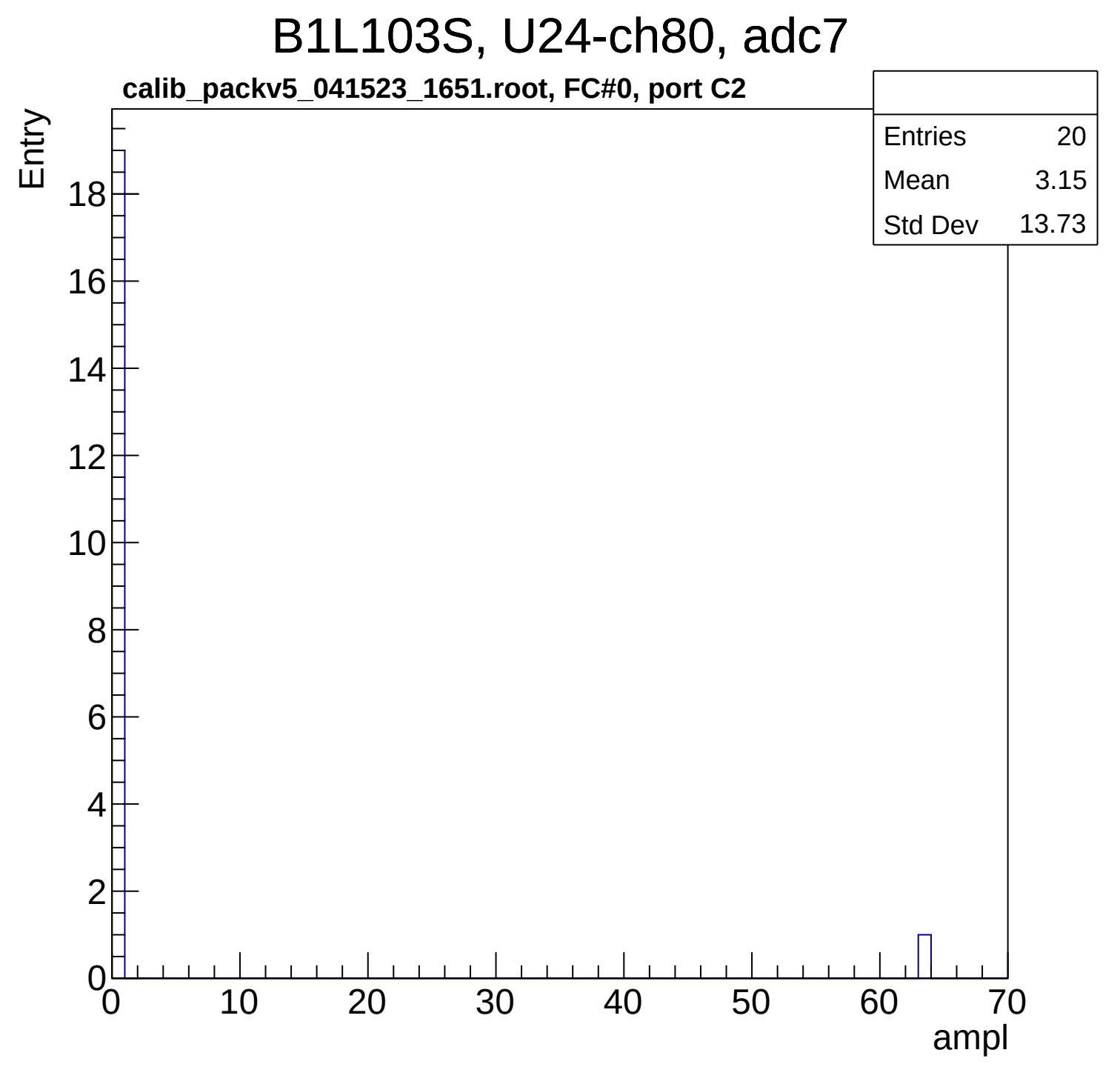
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U24-ch80, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
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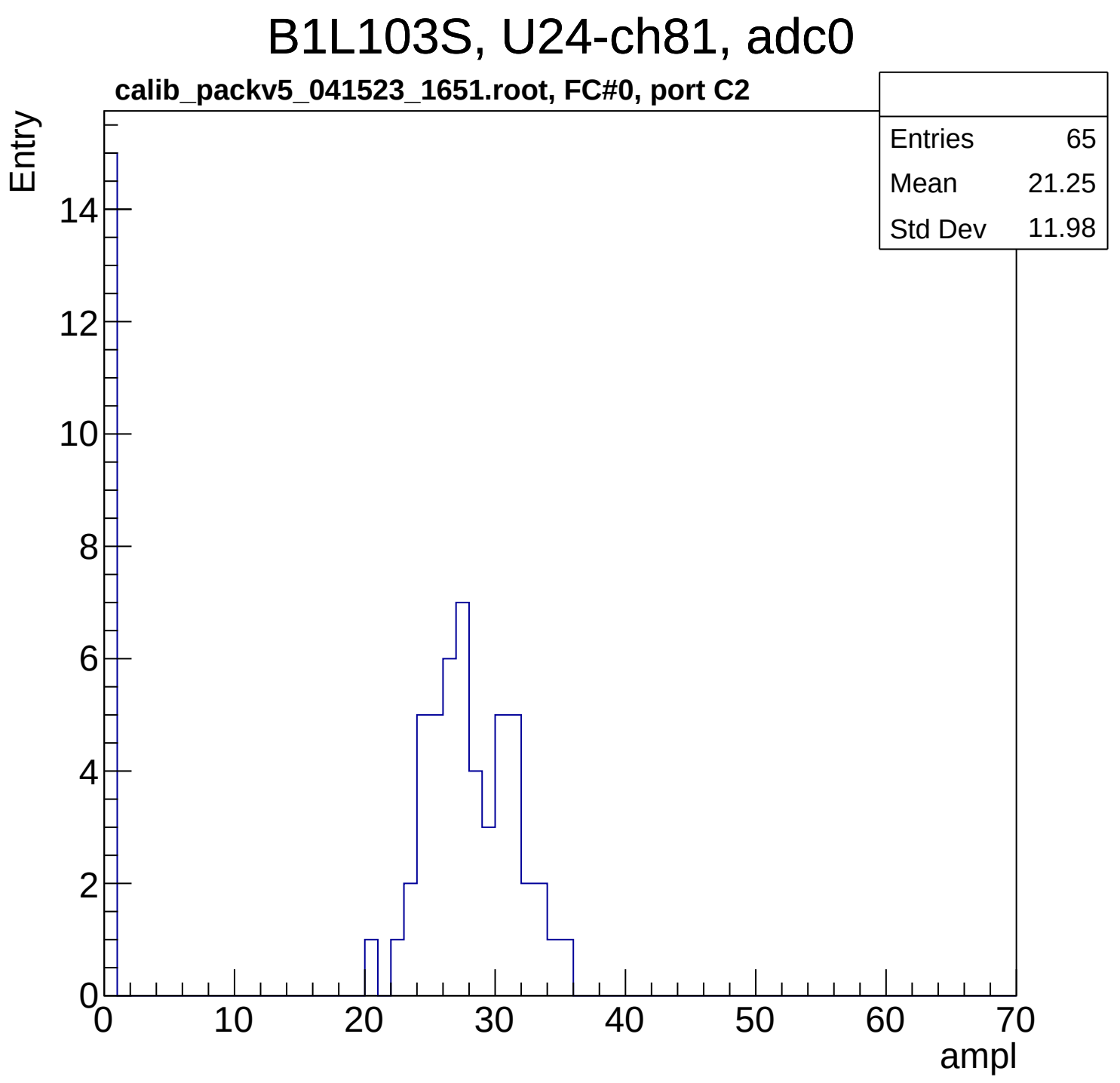
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch81, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 21.25
Std Dev 11.98
Entry
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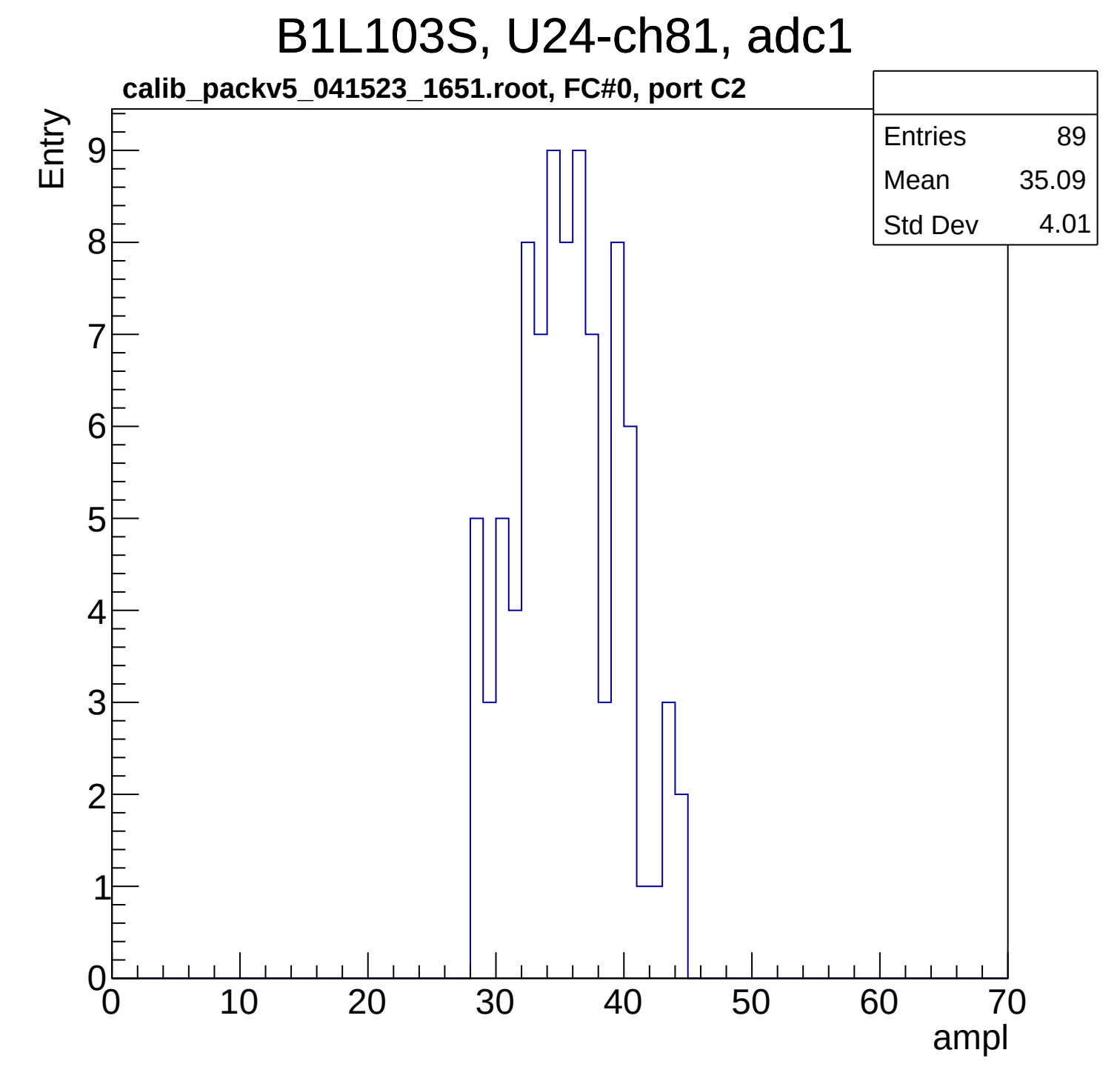
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch81, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 89
Mean 35.09
Std Dev 4.01
Entry
ampl
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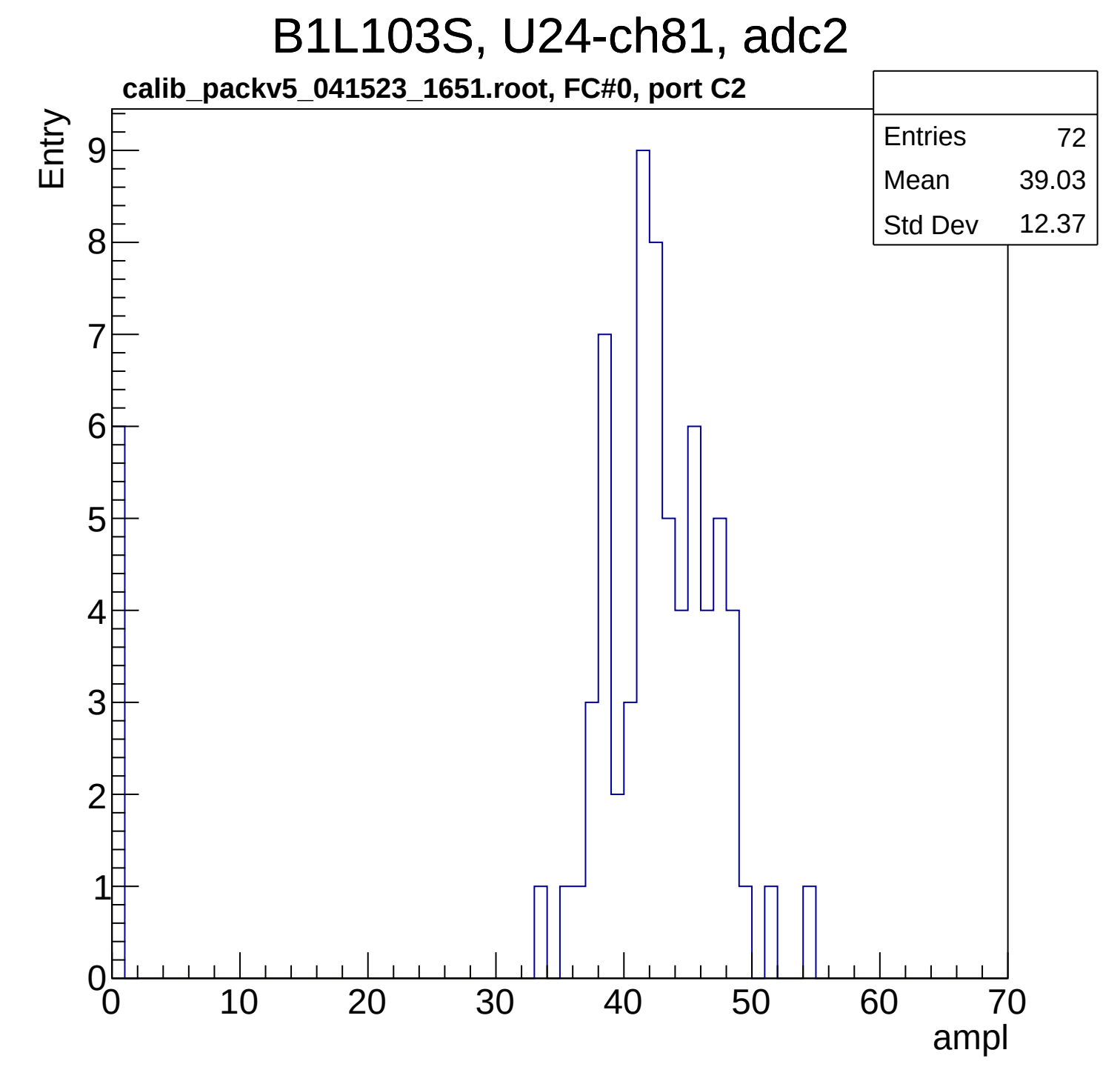
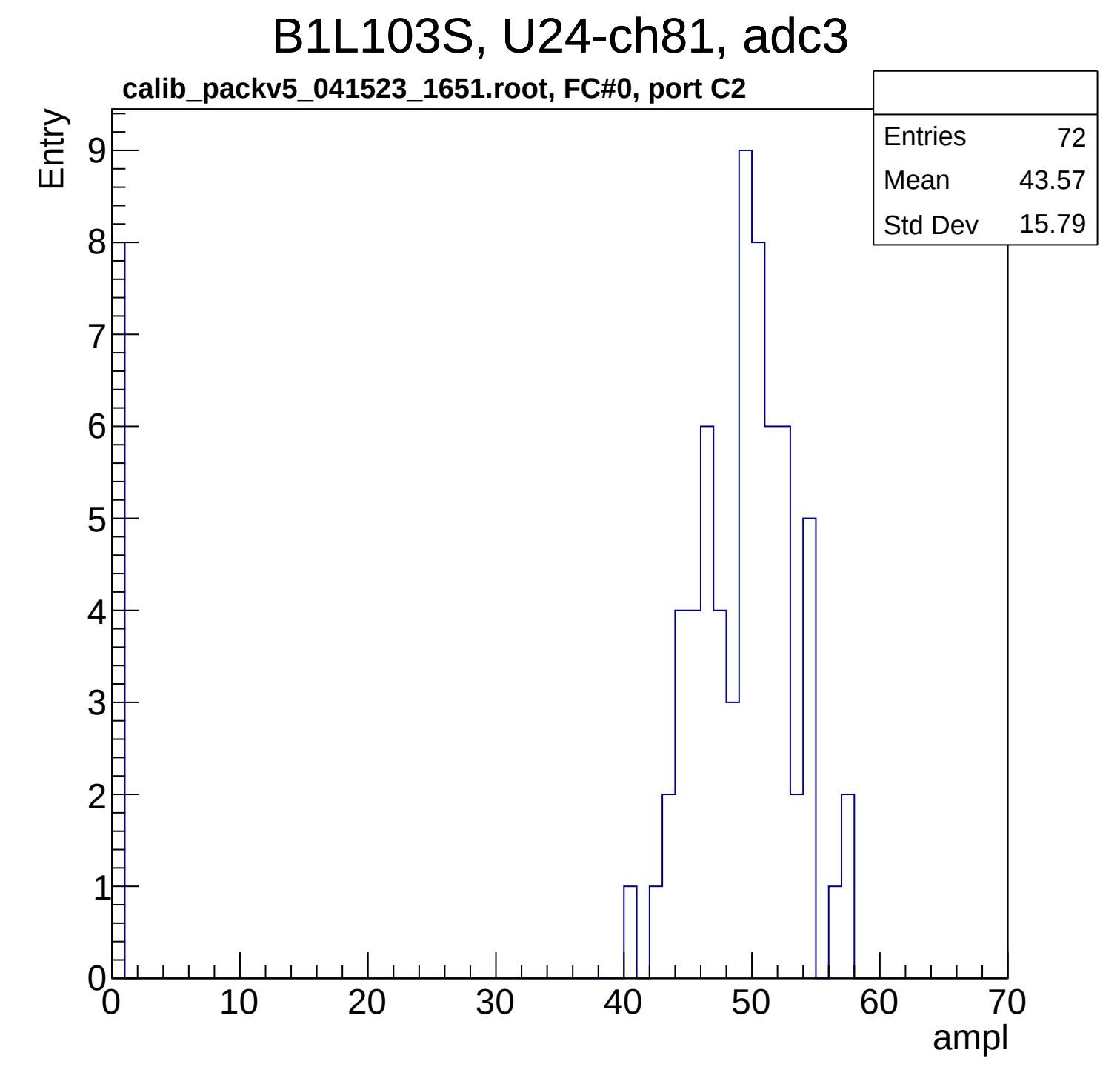
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U24-ch81, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 39.03
Std Dev 12.37
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U24-ch81, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 43.57
Std Dev 15.79
Entry
ampl
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2
3
4
5
6
7
8
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0
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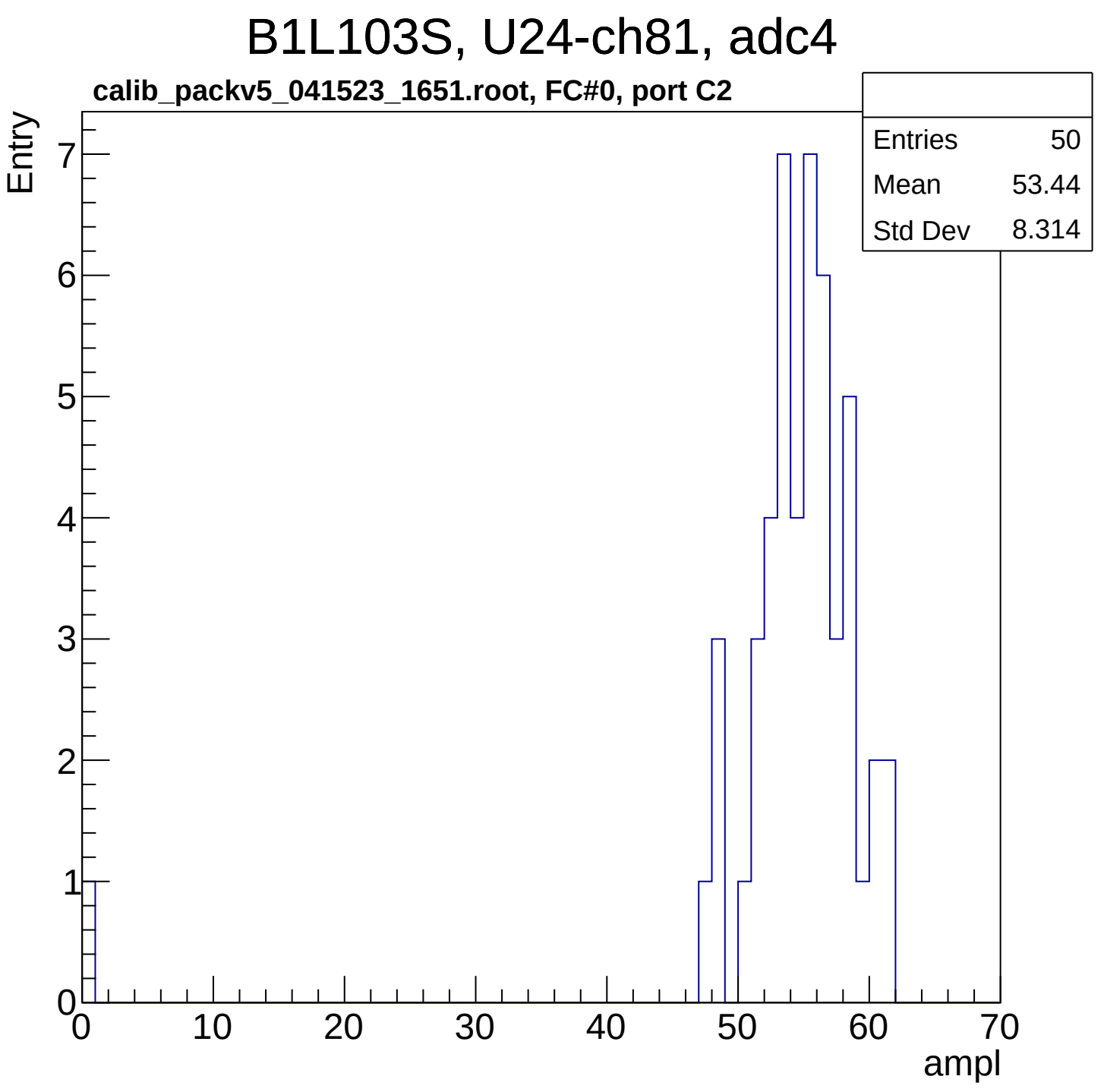
B1L103S, U24-ch81, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 53.44
Std Dev 8.314
Entry
ampl
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4
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0
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40
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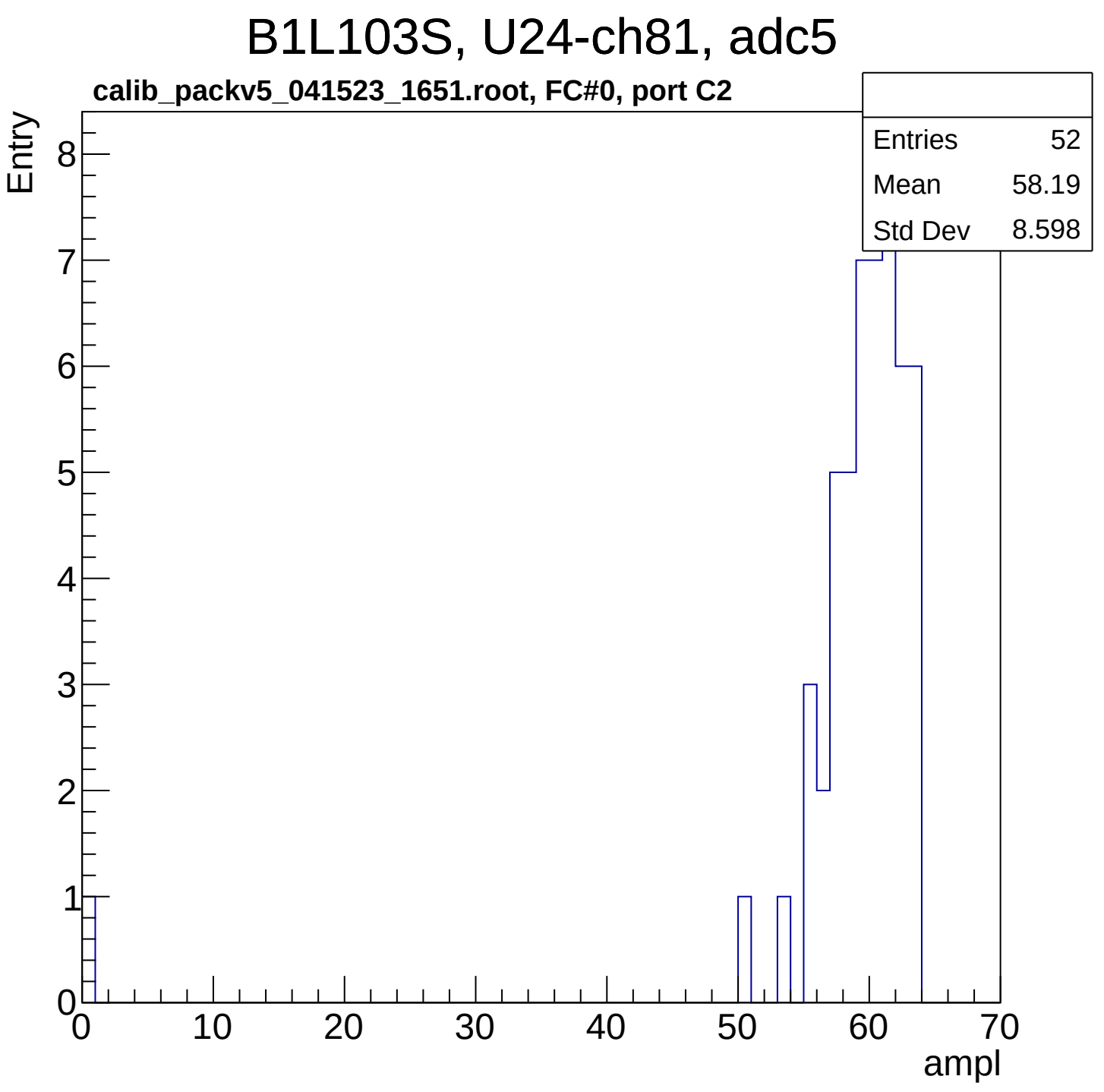
B1L103S, U24-ch81, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 58.19
Std Dev 8.598
Entry
ampl
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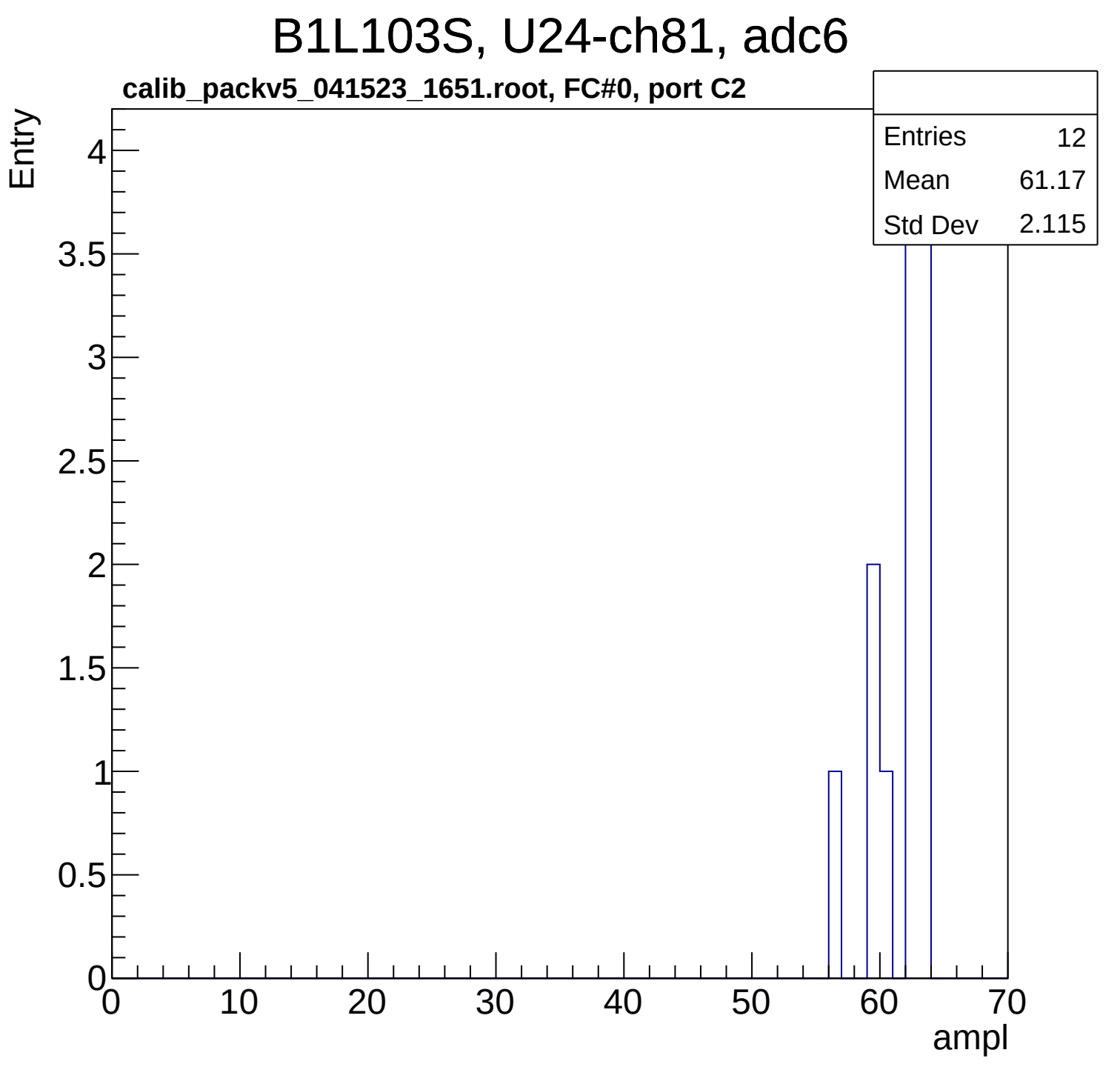
B1L103S, U24-ch81, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 61.17
Std Dev 2.115
Entry
ampl
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1.5
2
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3.5
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0
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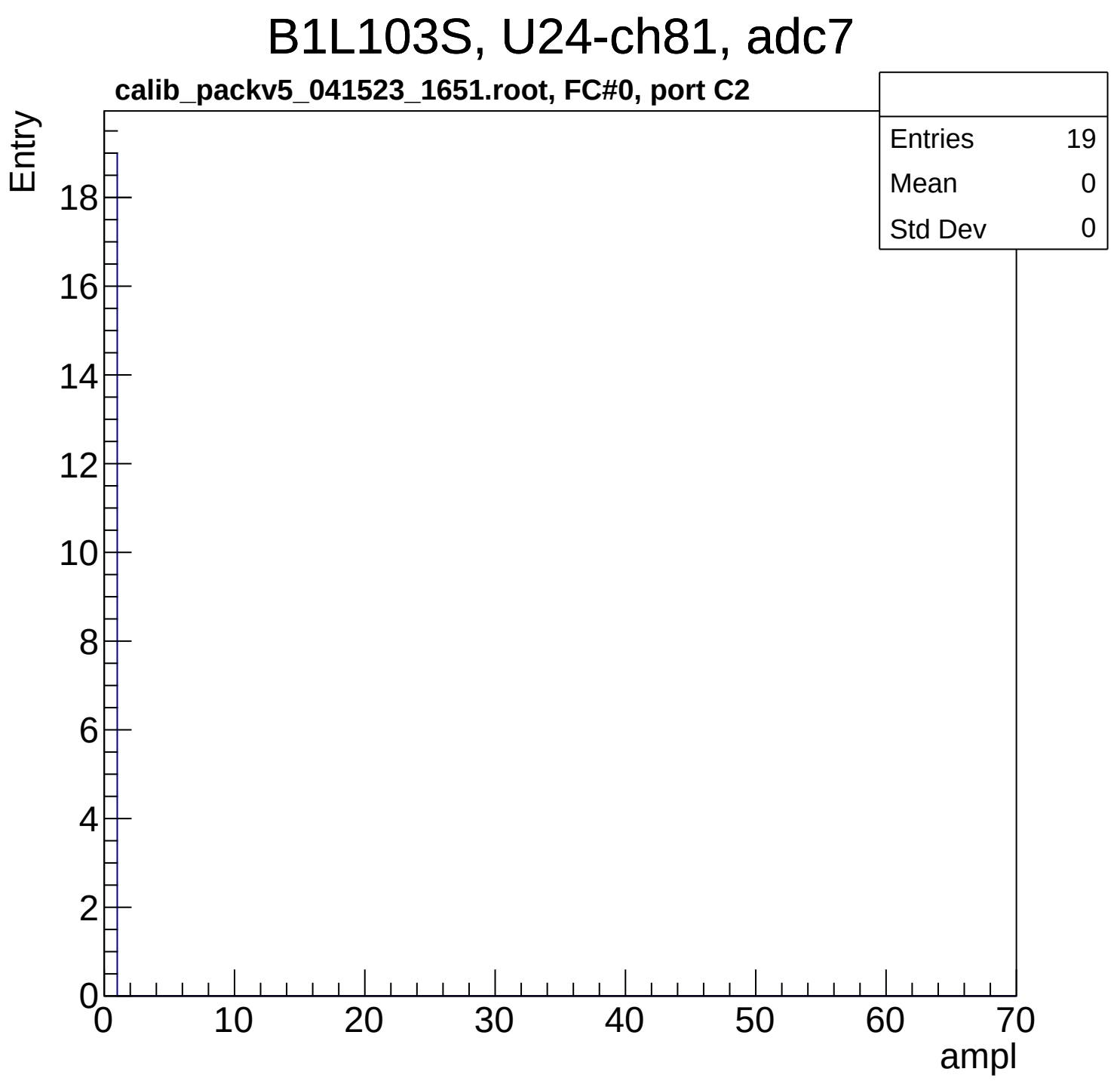
B1L103S, U24-ch81, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
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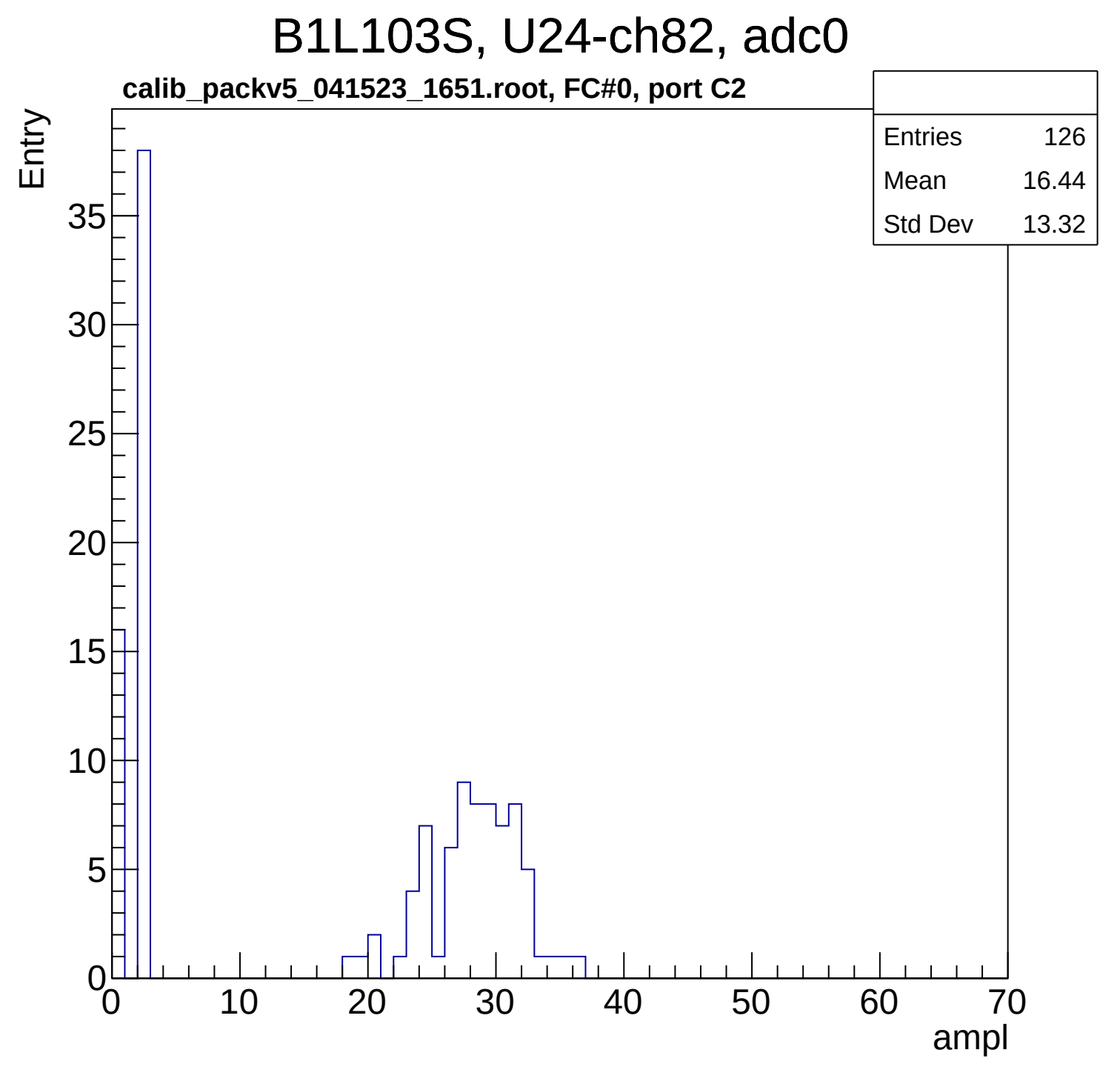
50
60
70
ampl


B1L103S, U24-ch82, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 126
Mean 16.44
Std Dev 13.32
Entry
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5
10
15
20
25
30
35
0
10
20
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40
50
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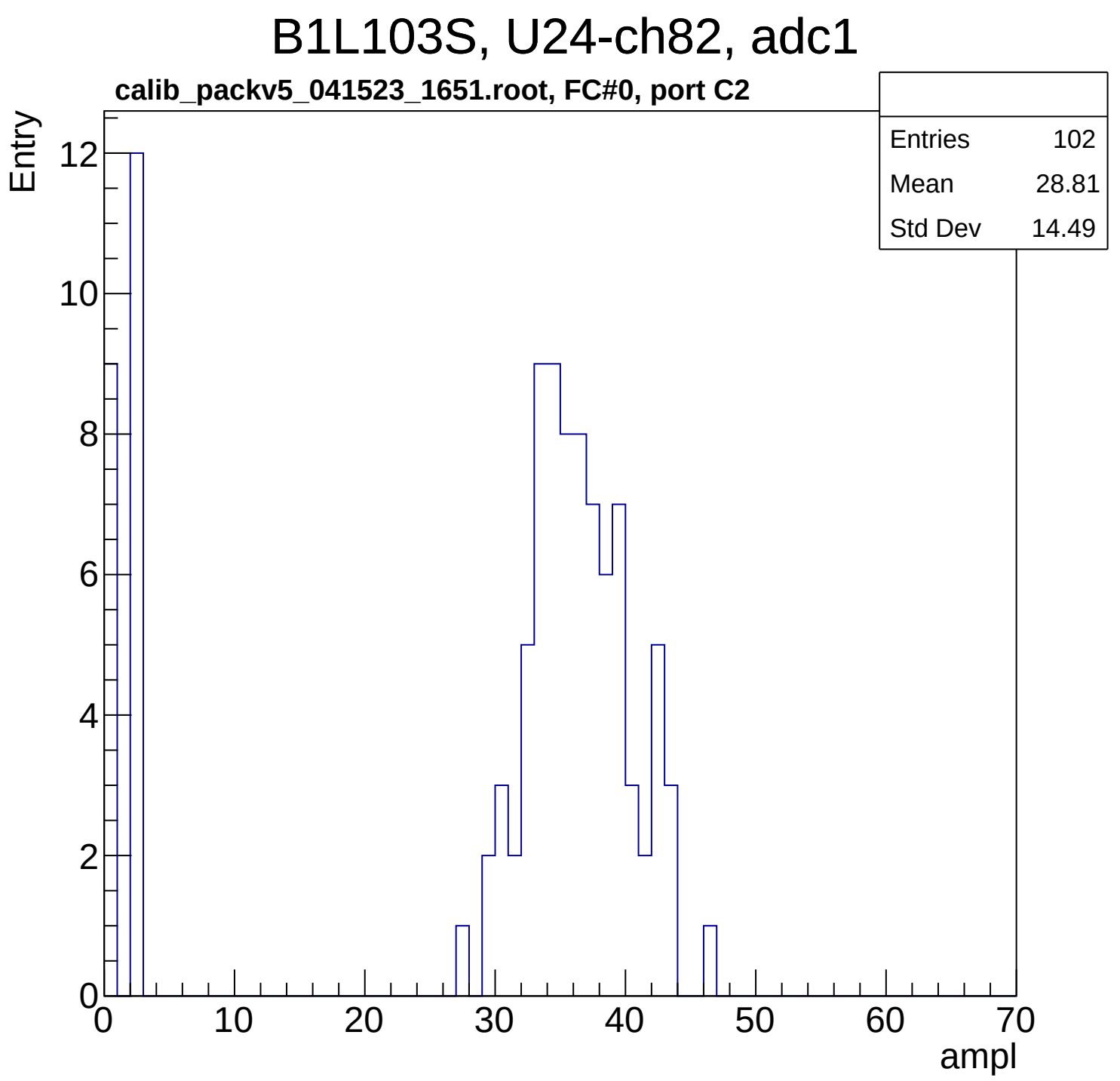
70
ampl


B1L103S, U24-ch82, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 102
Mean 28.81
Std Dev 14.49
Entry
ampl
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2
4
6
8
10
12
0
10
20
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40
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60
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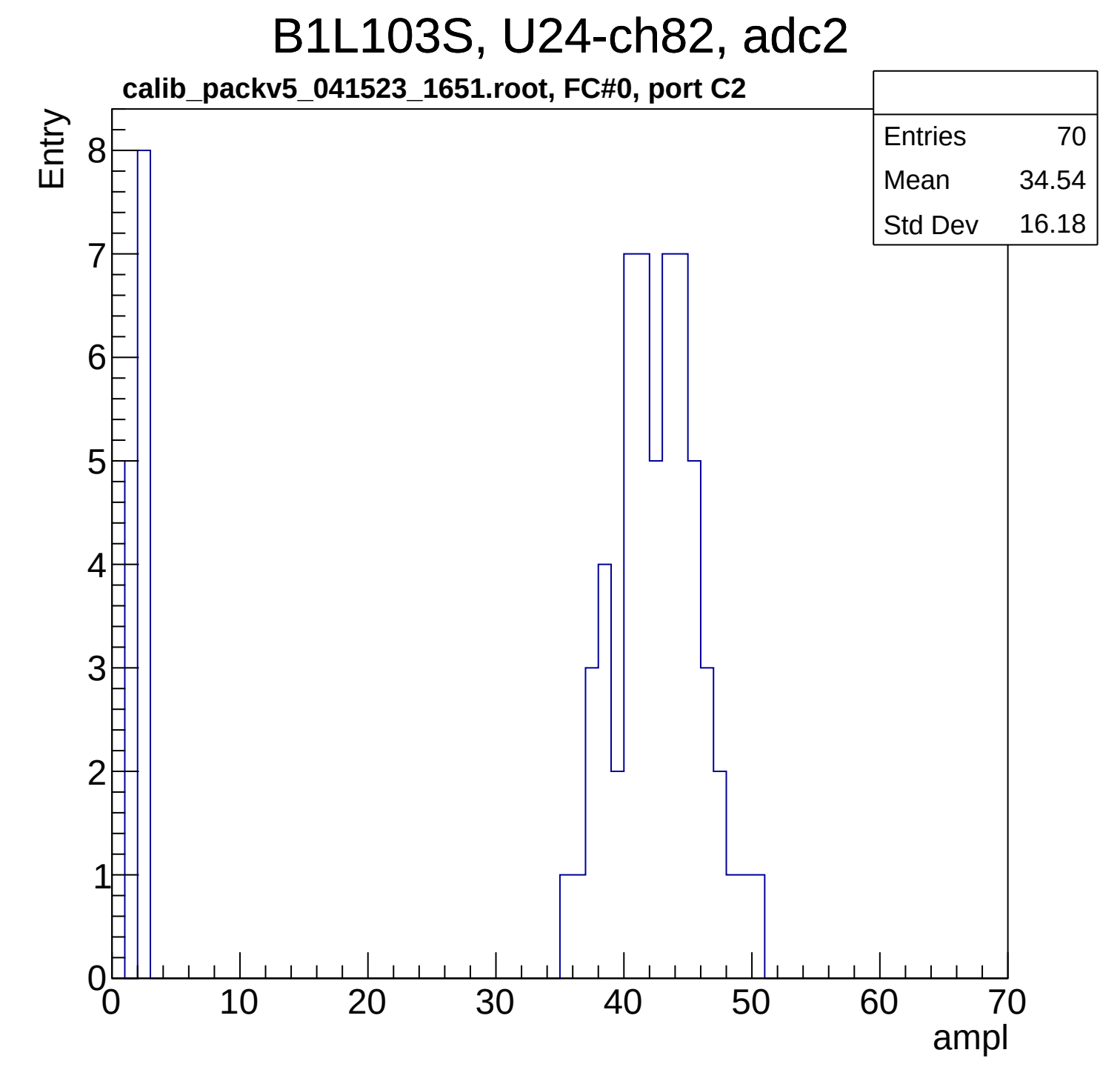
B1L103S, U24-ch82, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 34.54
Std Dev 16.18
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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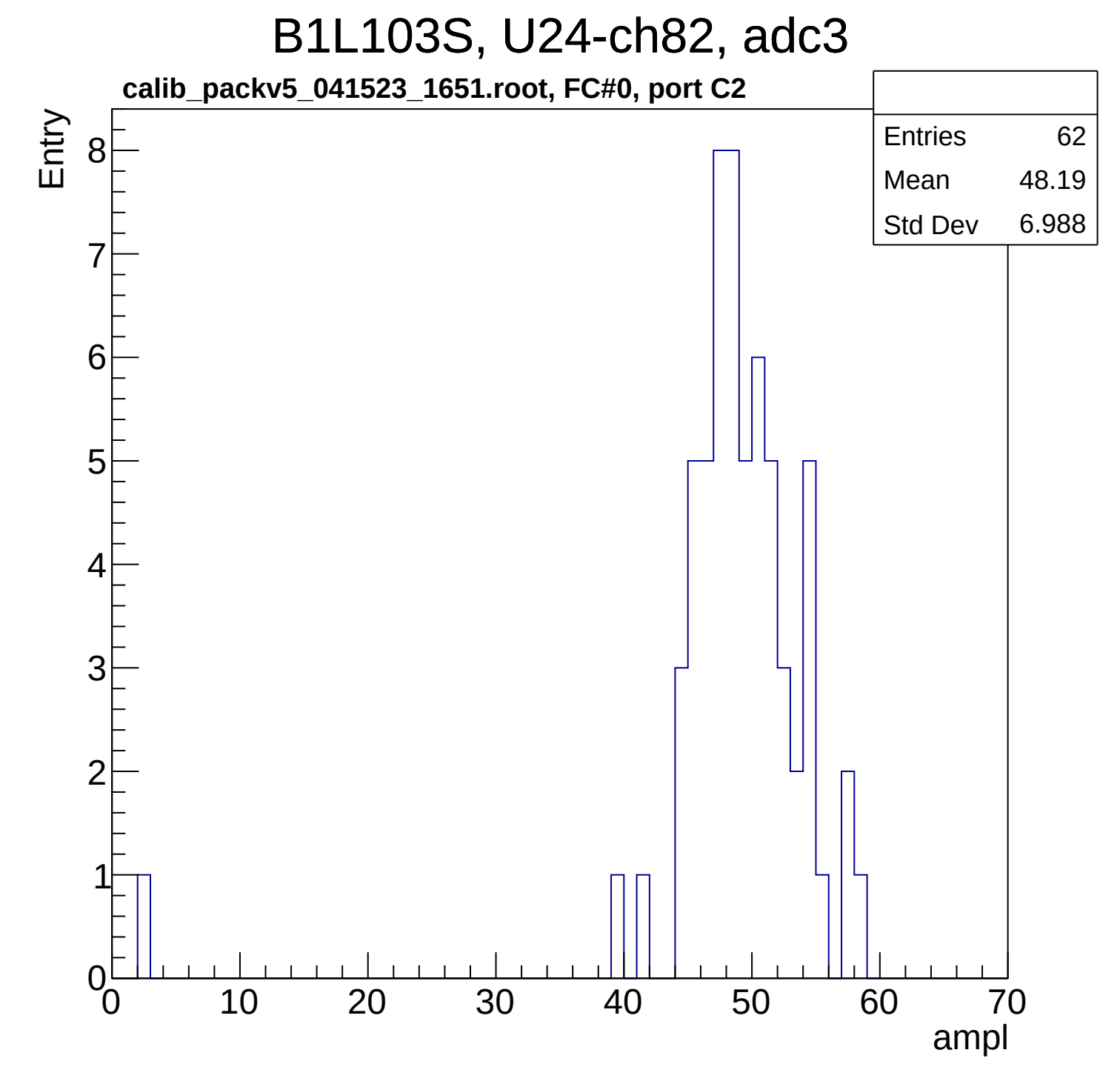
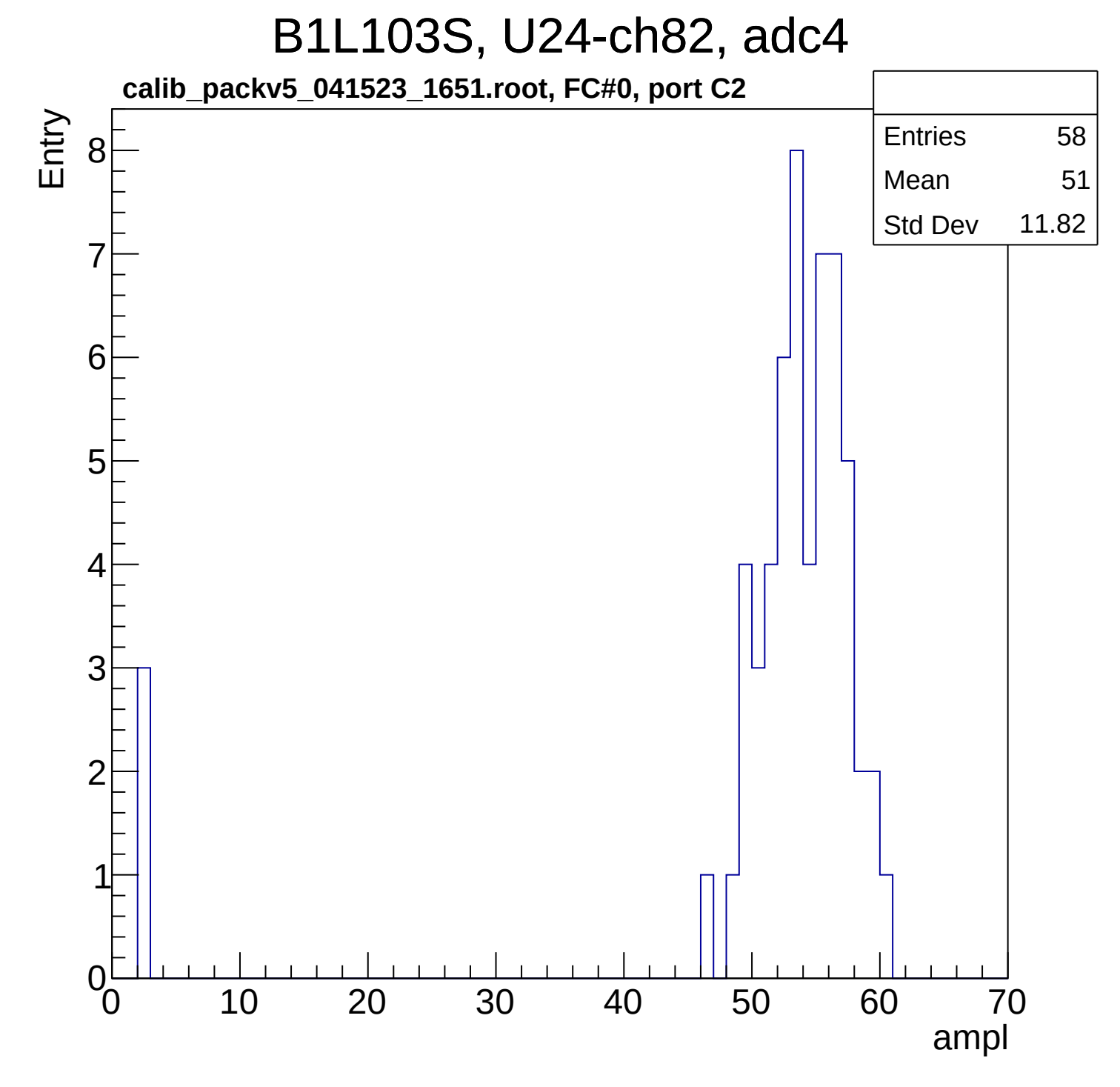

B1L103S, U24-ch82, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 48.19
Std Dev 6.988
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U24-ch82, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 51
Std Dev 11.82
Entry
ampl
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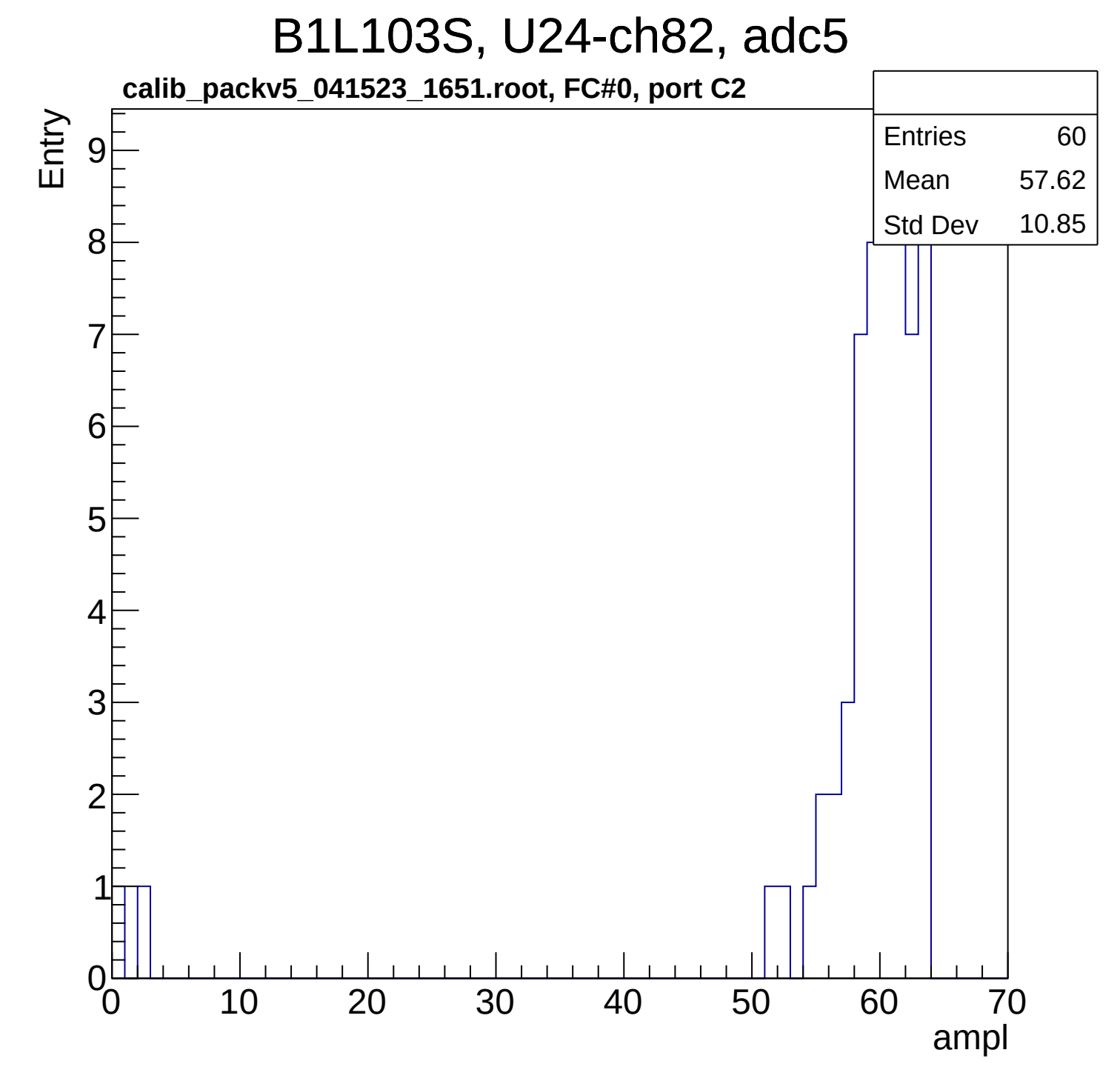
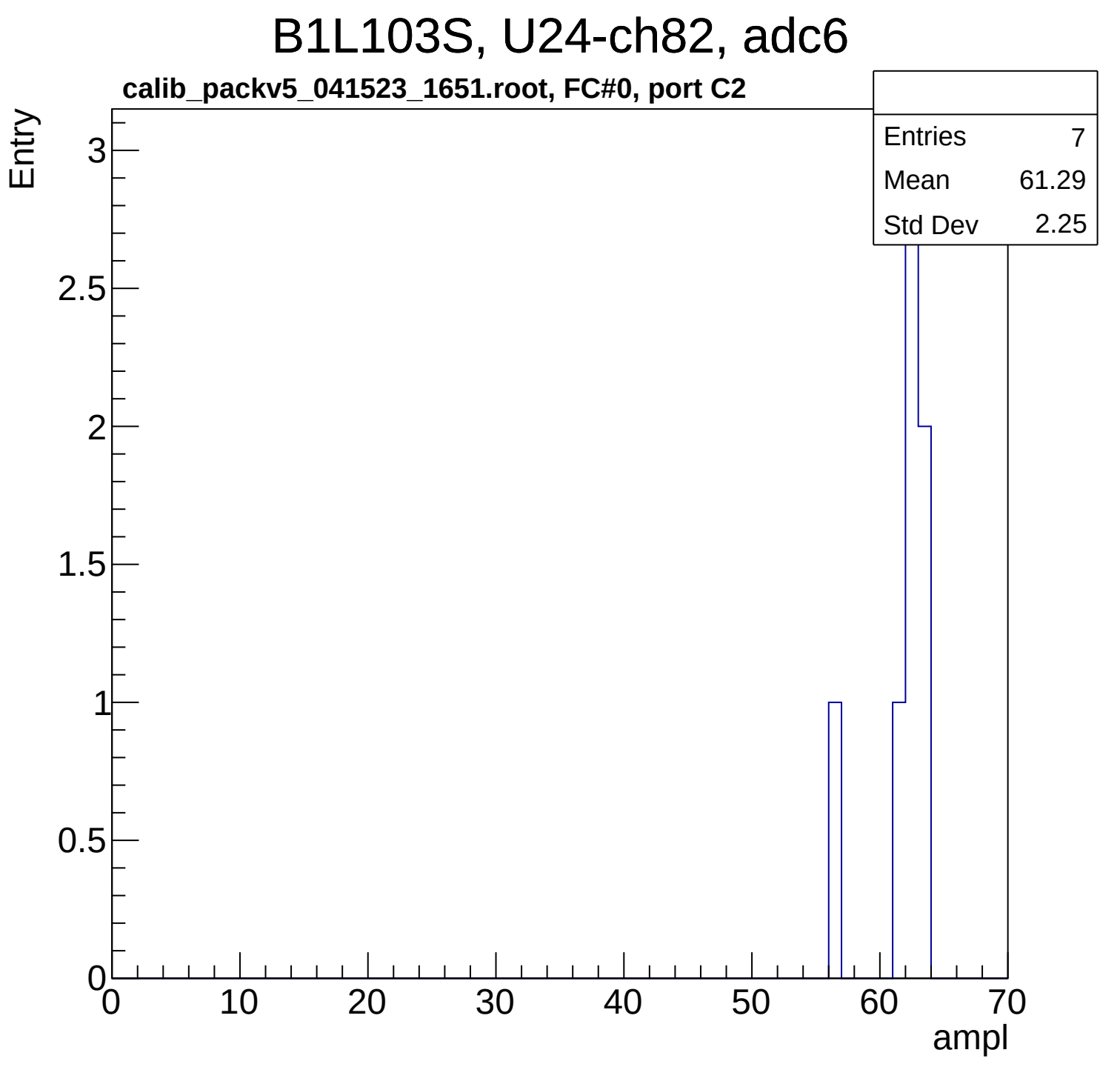
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U24-ch82, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 57.62
Std Dev 10.85
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U24-ch82, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 61.29
Std Dev 2.25
Entry
ampl
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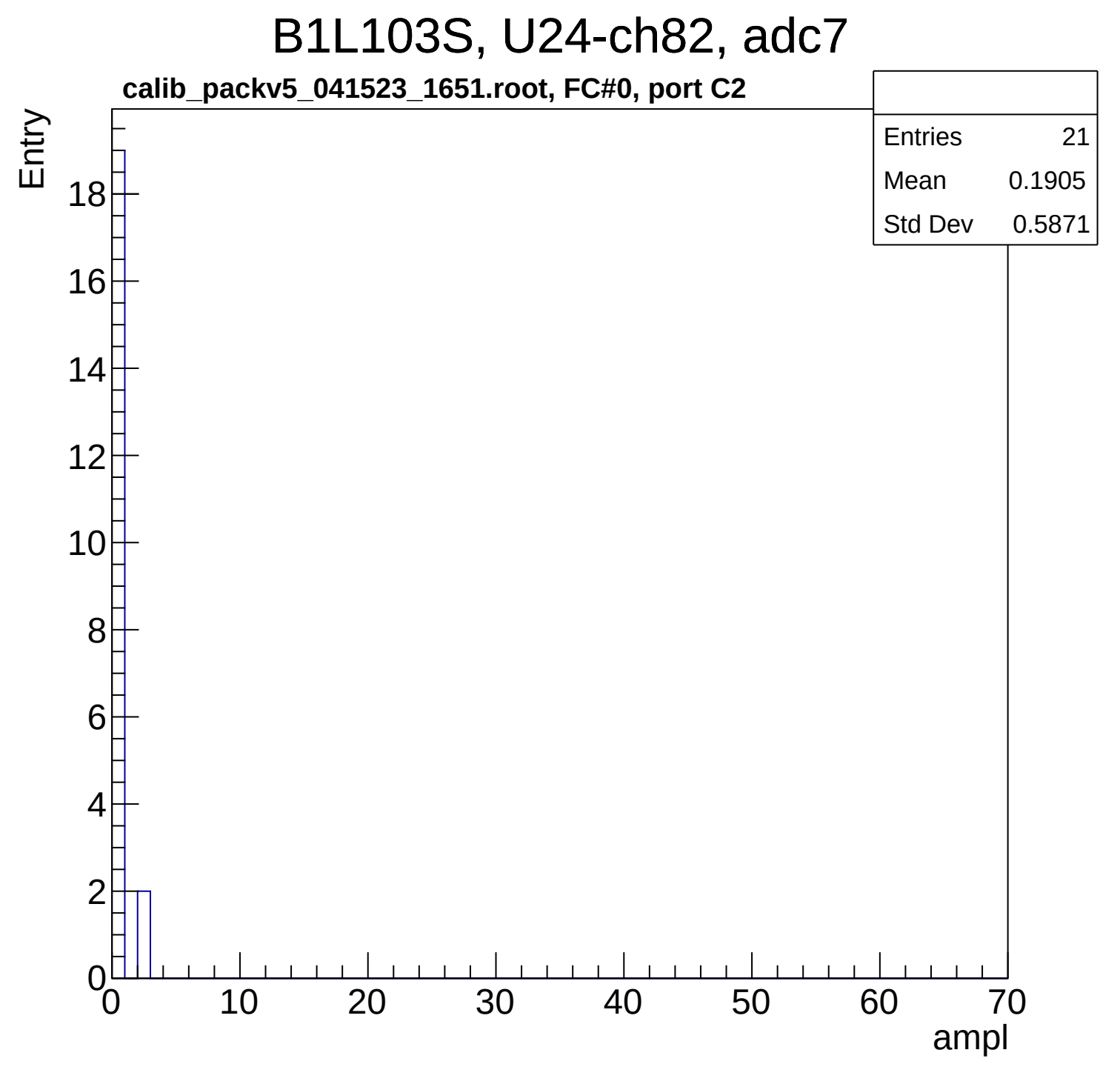
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U24-ch82, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 0.1905
Std Dev 0.5871
Entry
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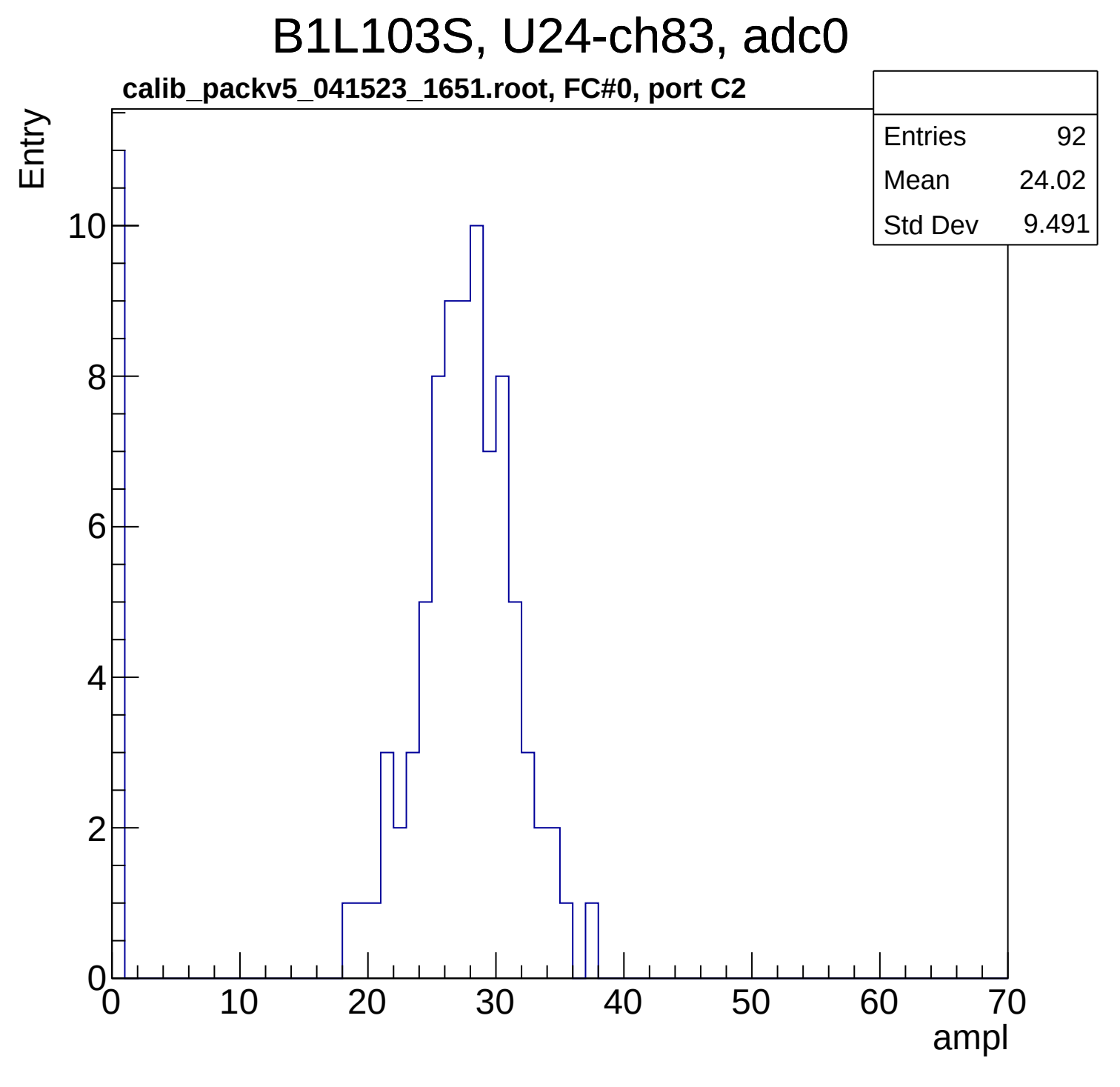
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch83, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 92
Mean 24.02
Std Dev 9.491
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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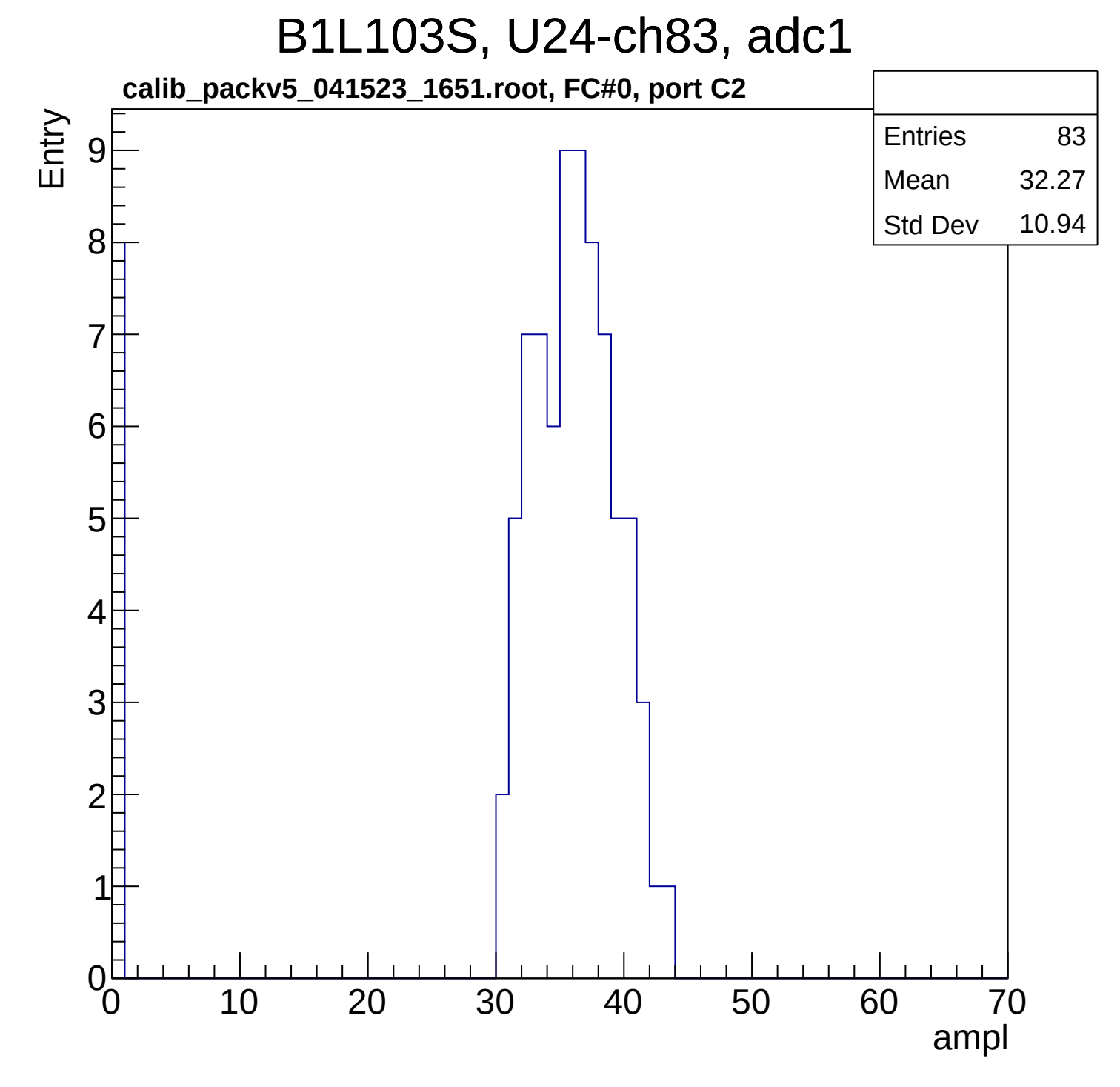
B1L103S, U24-ch83, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 32.27
Std Dev 10.94
Entry
ampl
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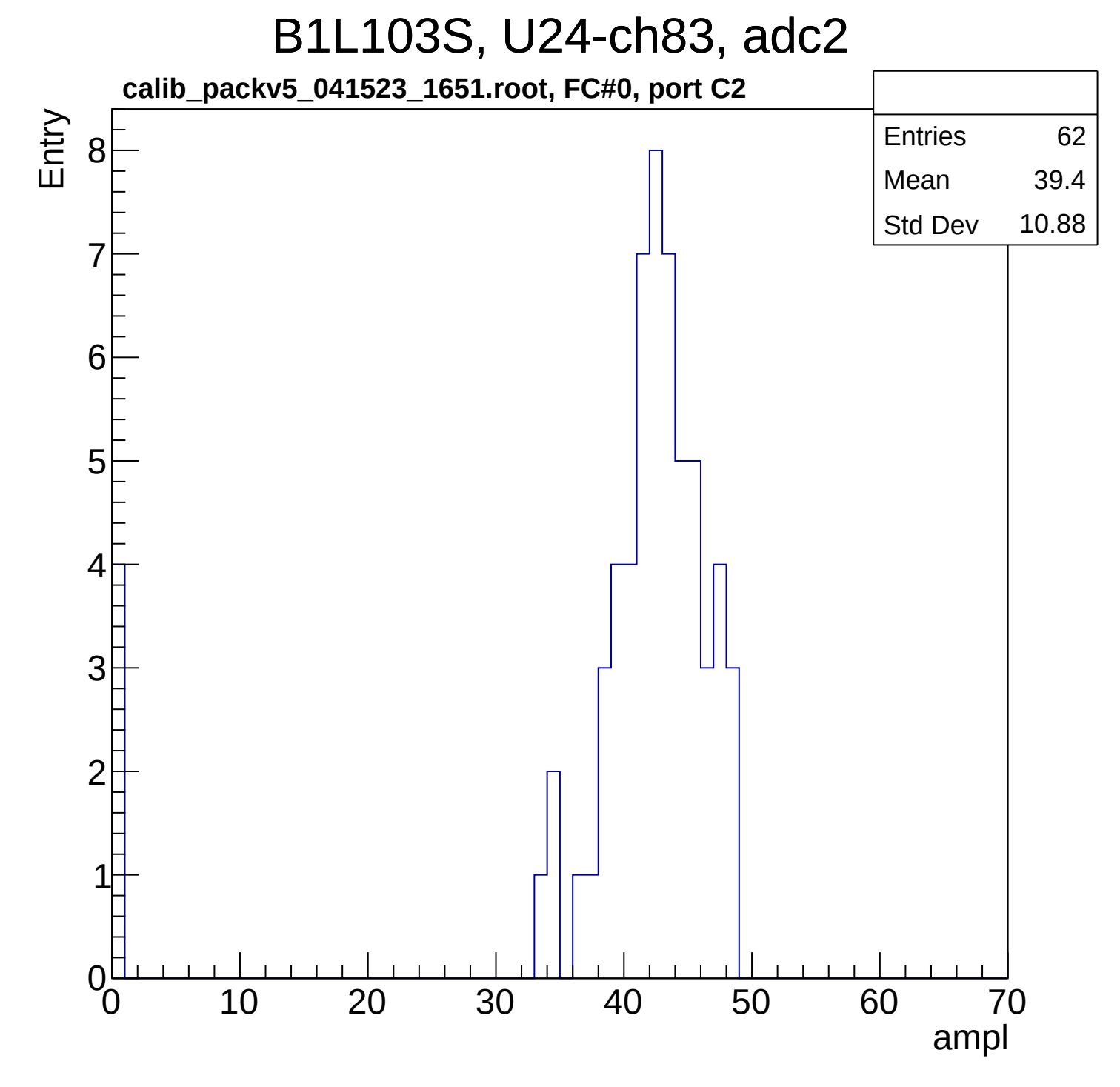
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U24-ch83, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 39.4
Std Dev 10.88
Entry
ampl
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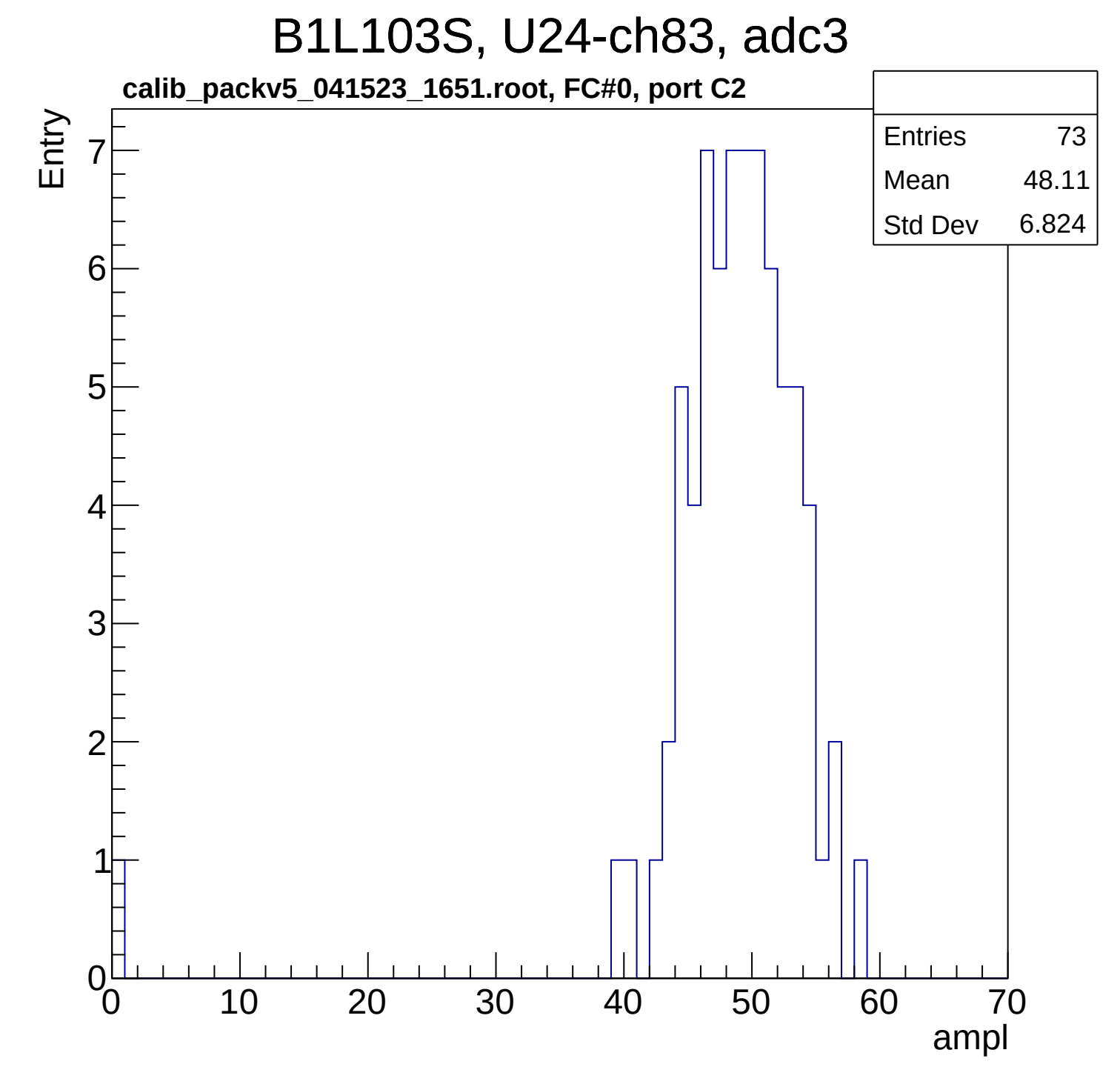
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U24-ch83, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 48.11
Std Dev 6.824
Entry
ampl
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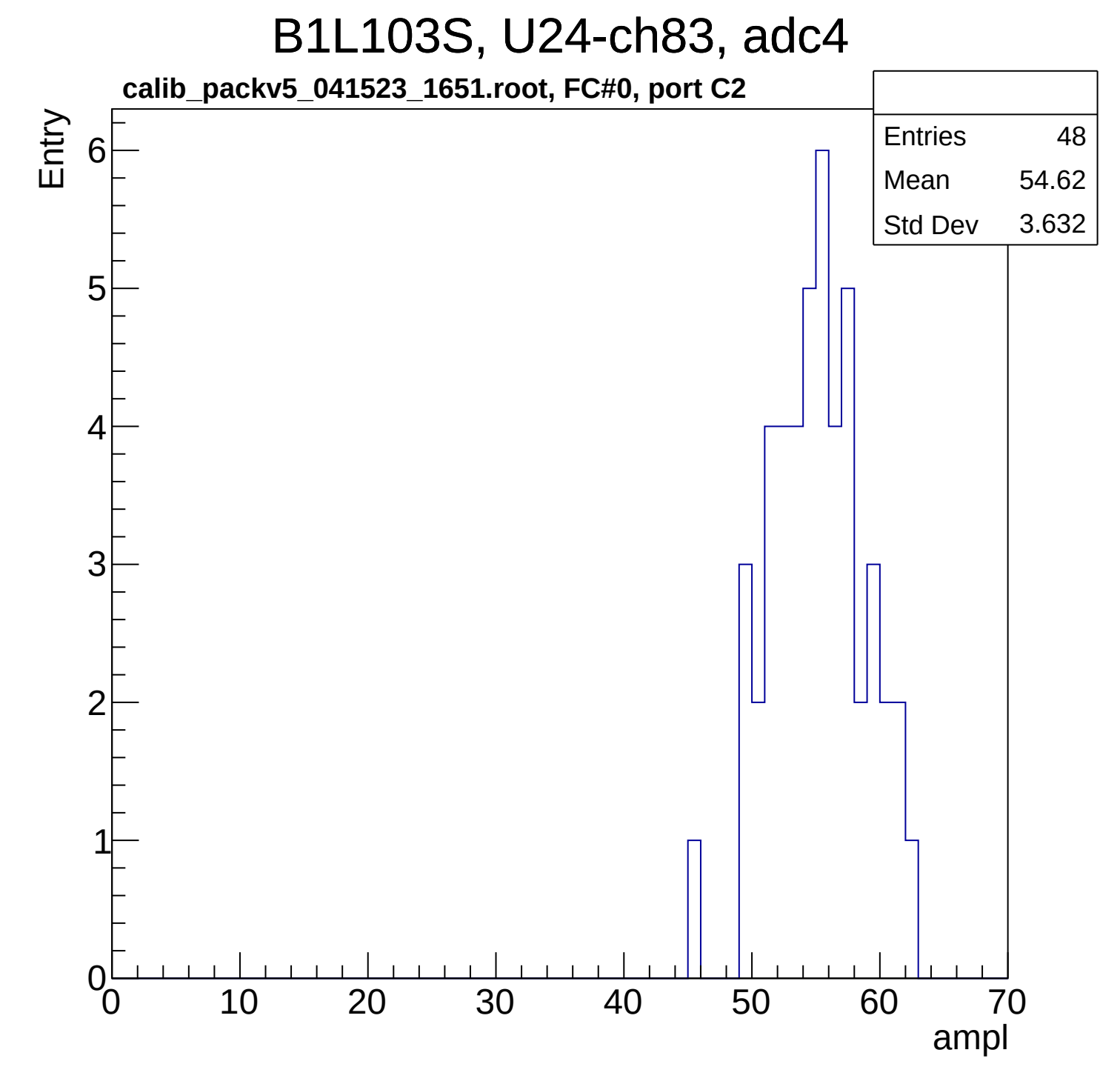
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U24-ch83, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 54.62
Std Dev 3.632
Entry
ampl
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2
3
4
5
6
0
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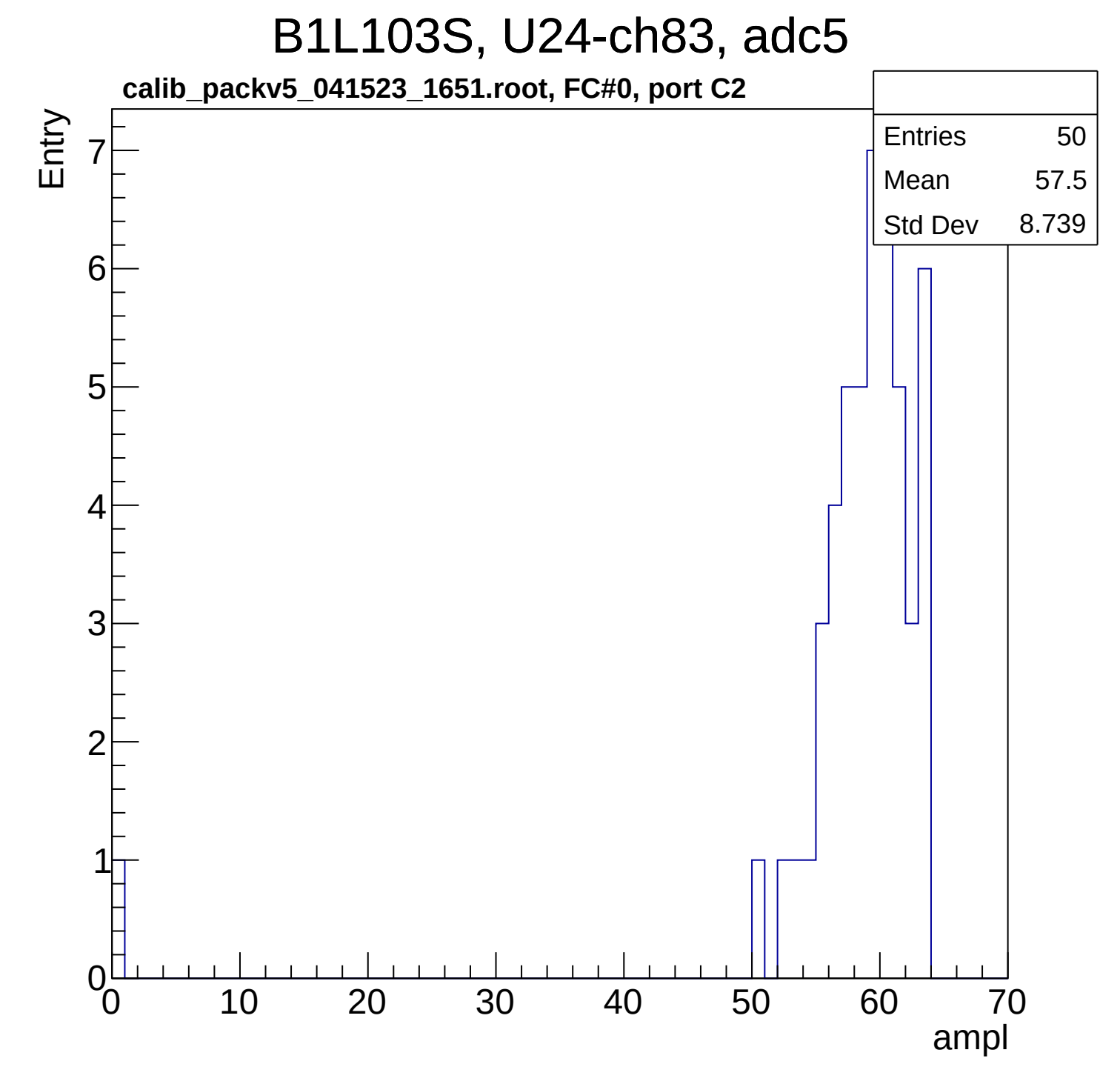
20
30
40
50
60
70


B1L103S, U24-ch83, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 57.5
Std Dev 8.739
Entry
ampl
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2
3
4
5
6
7
0
10
20
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40
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60
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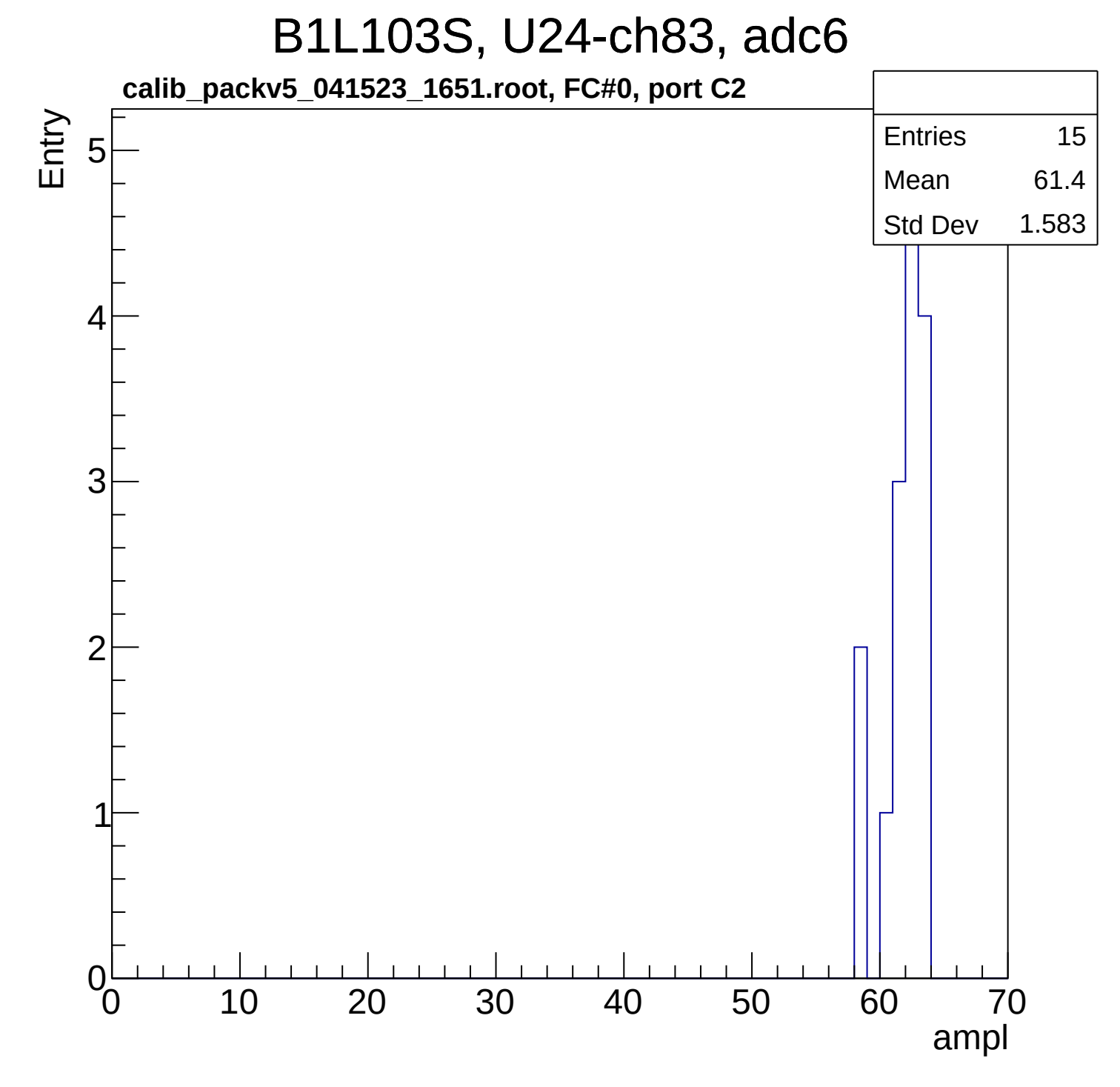
B1L103S, U24-ch83, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 15
Mean 61.4
Std Dev 1.583
Entry
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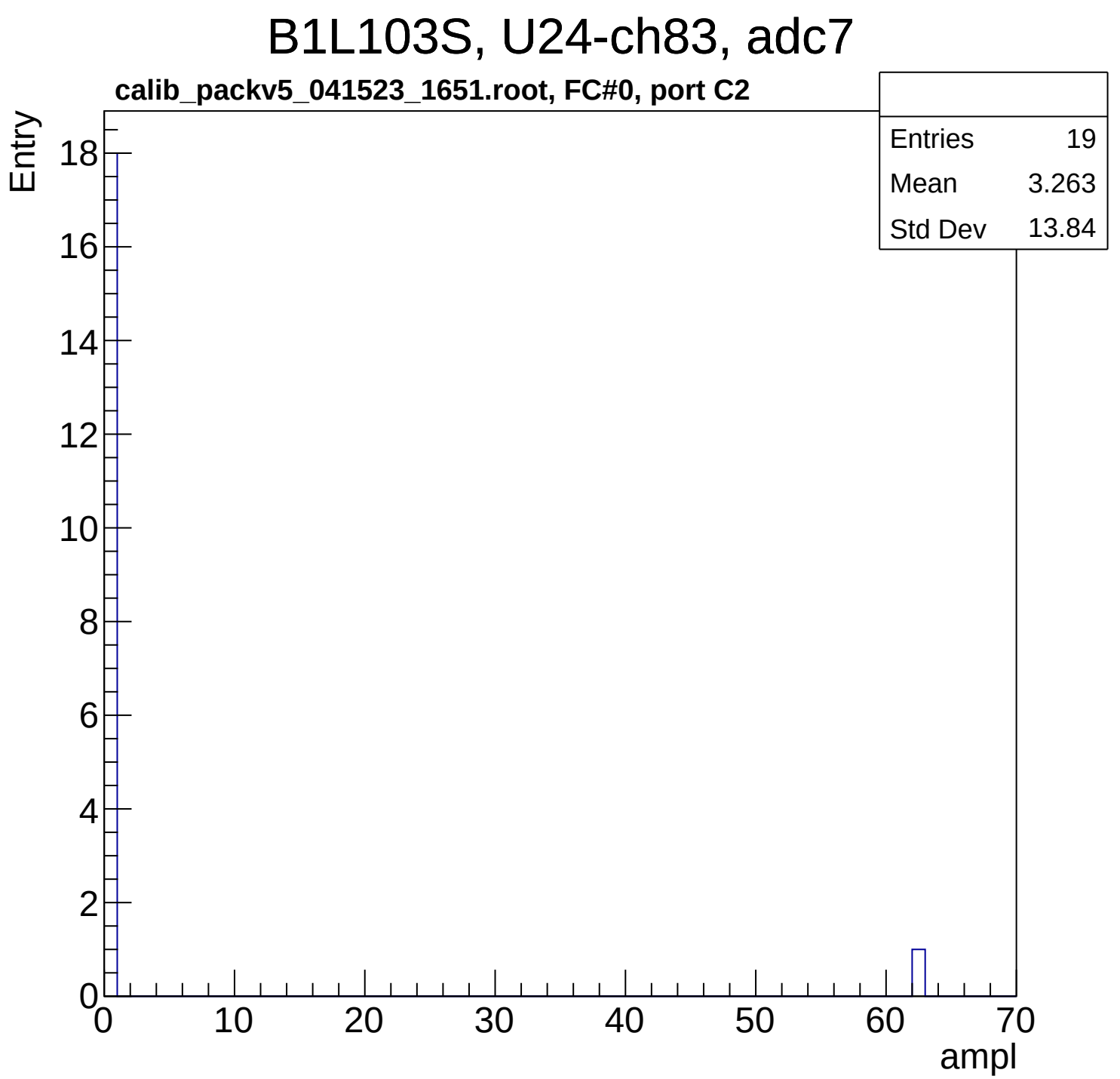
50
60
70
ampl


B1L103S, U24-ch83, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 3.263
Std Dev 13.84
Entry
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6
8
10
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14
16
18
0
10
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30
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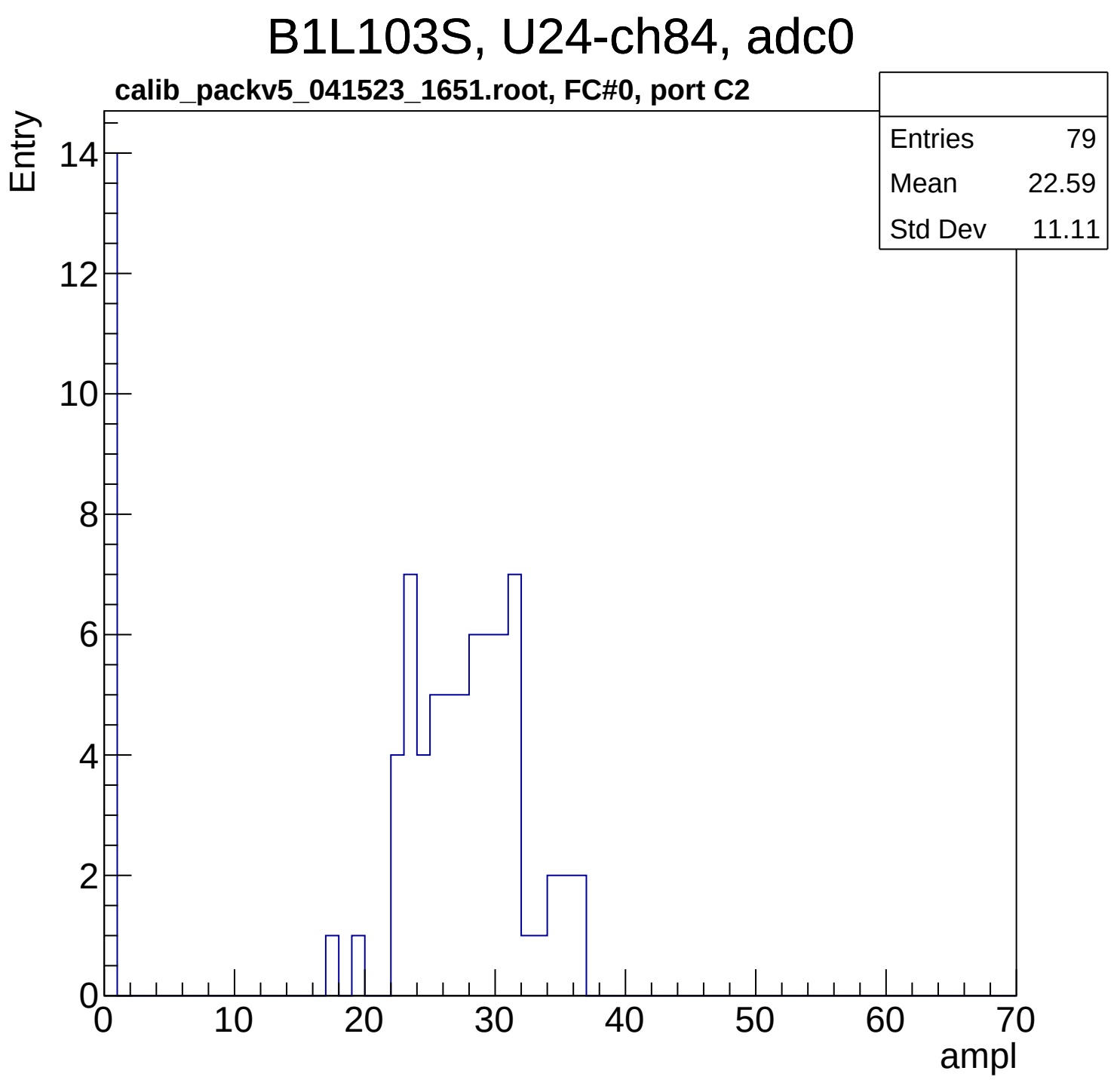
50
60
70
ampl


B1L103S, U24-ch84, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 22.59
Std Dev 11.11
Entry
ampl
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4
6
8
10
12
14
0
10
20
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40
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60
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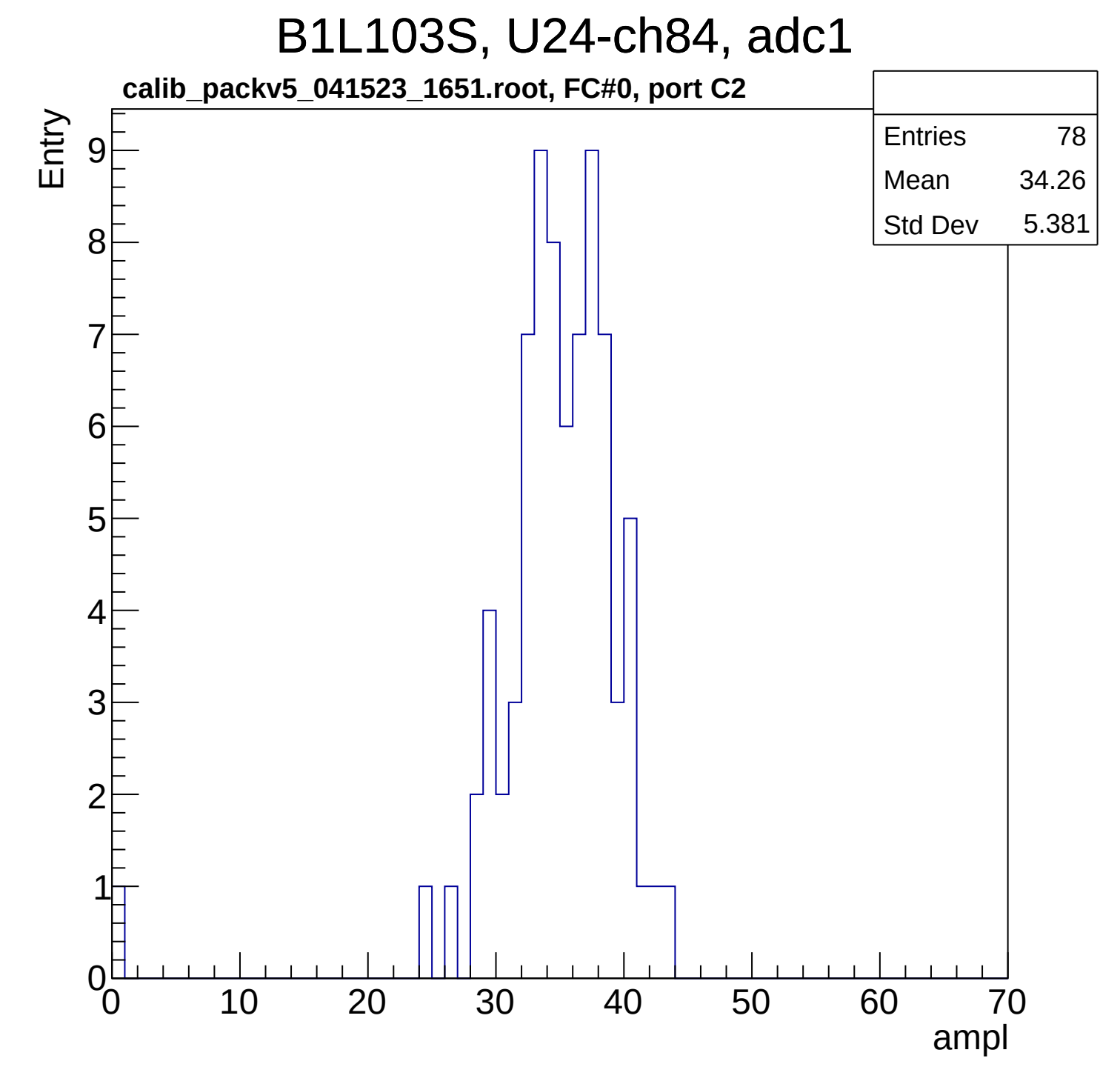
B1L103S, U24-ch84, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 34.26
Std Dev 5.381
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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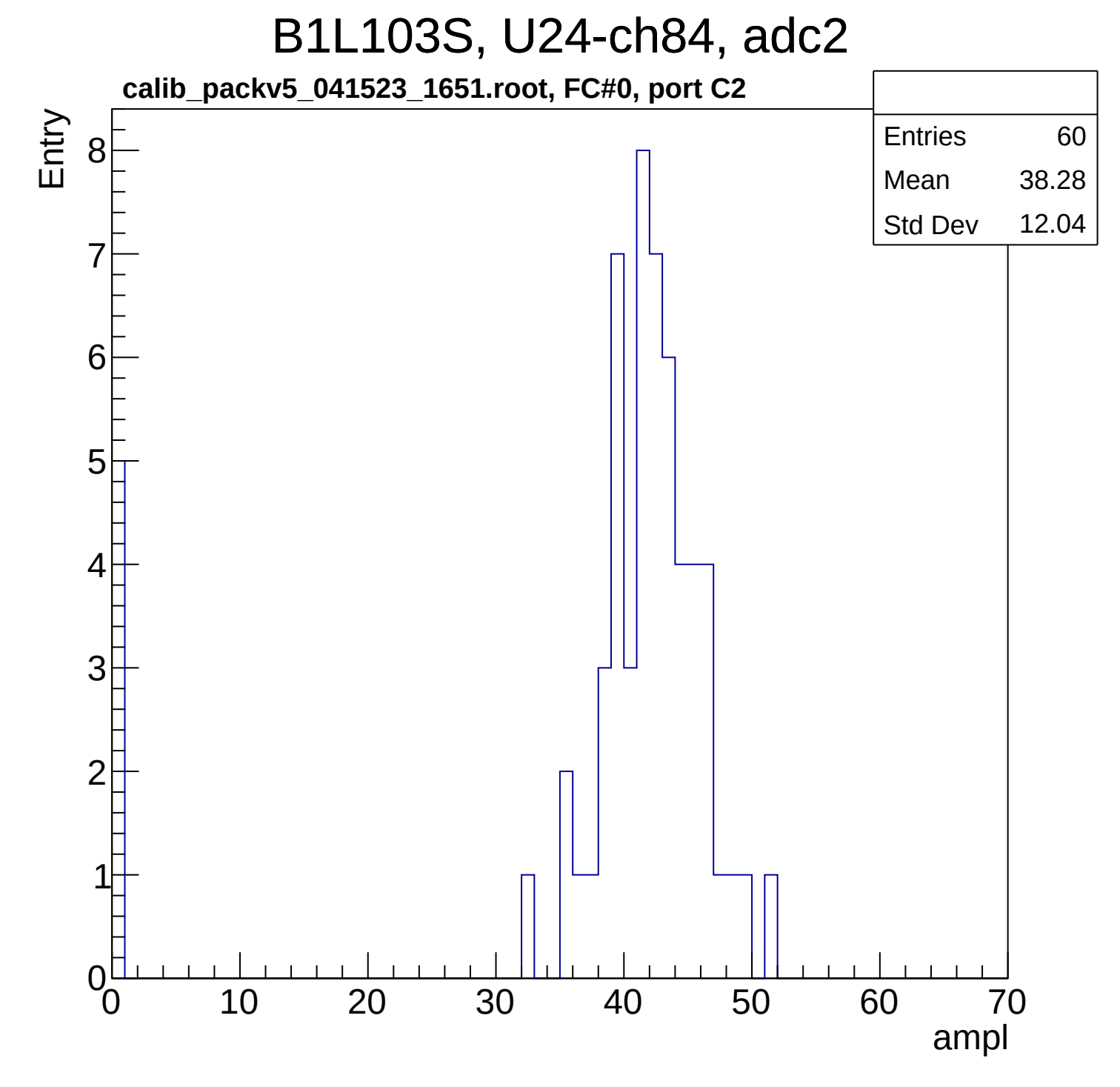
40
50
60
70


B1L103S, U24-ch84, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 38.28
Std Dev 12.04
Entry
ampl
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2
3
4
5
6
7
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0
10
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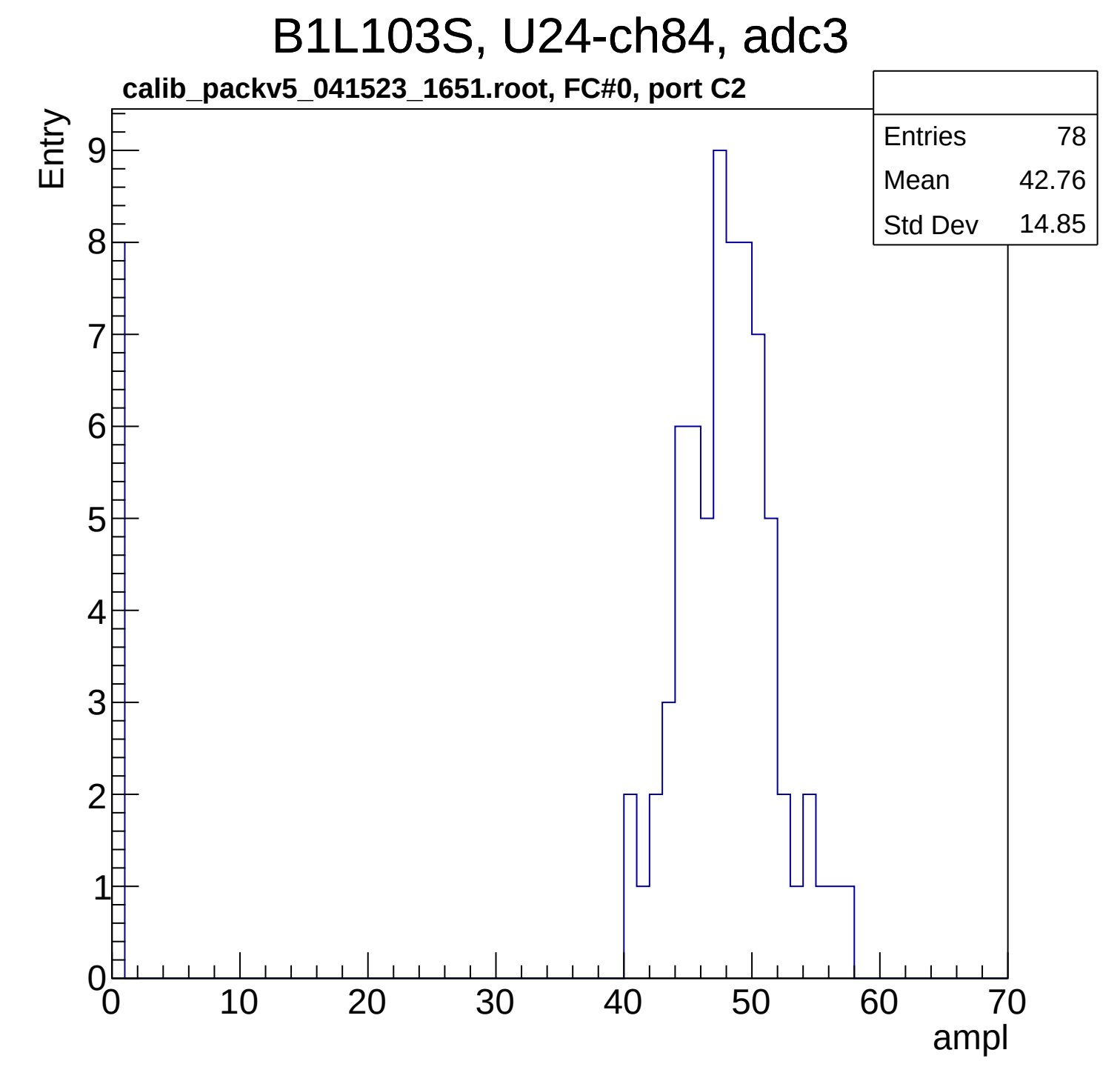
60
70


B1L103S, U24-ch84, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 42.76
Std Dev 14.85
Entry
ampl
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2
3
4
5
6
7
8
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0
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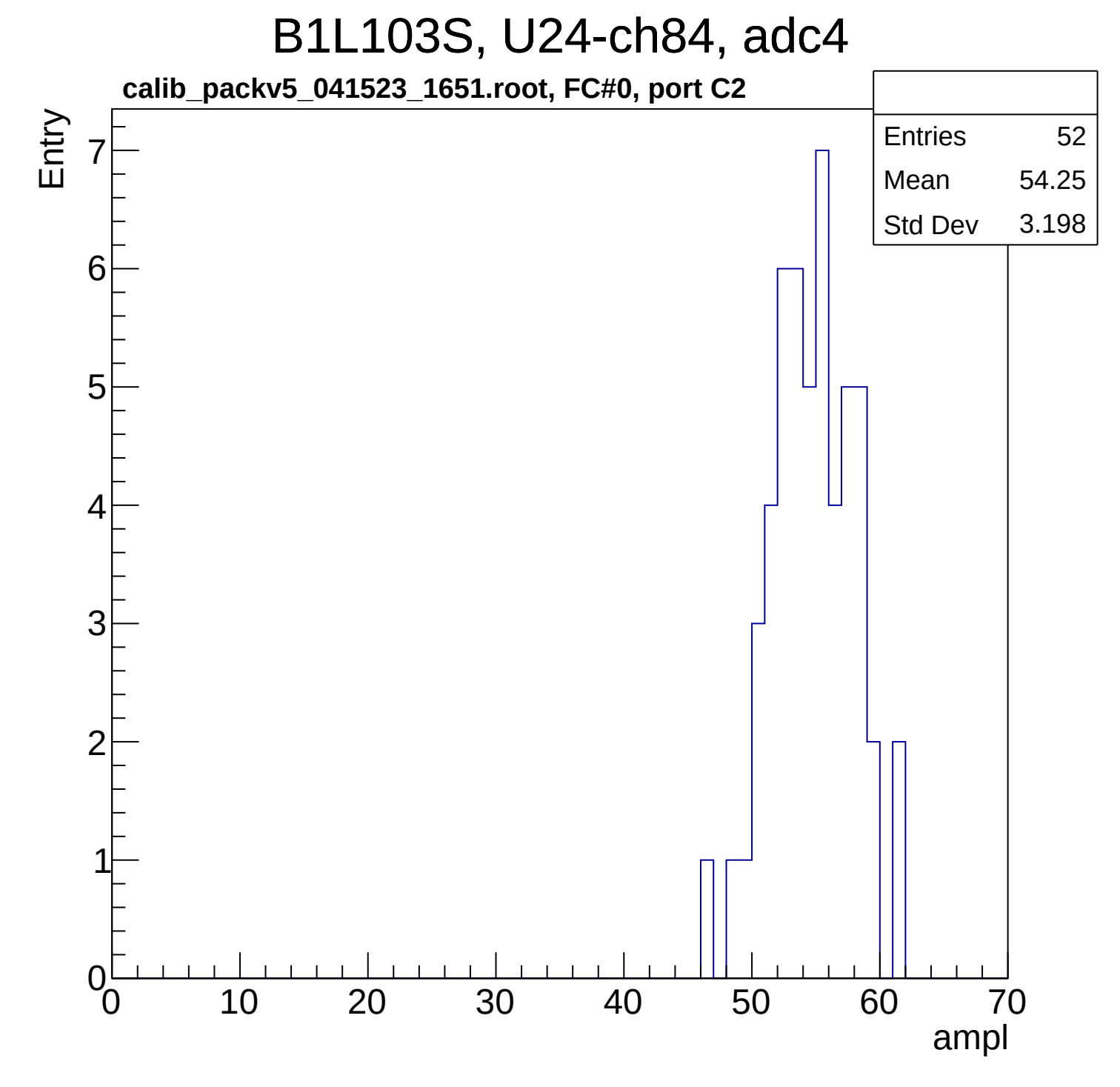
60
70


B1L103S, U24-ch84, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 54.25
Std Dev 3.198
Entry
ampl
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1
2
3
4
5
6
7
0
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20
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40
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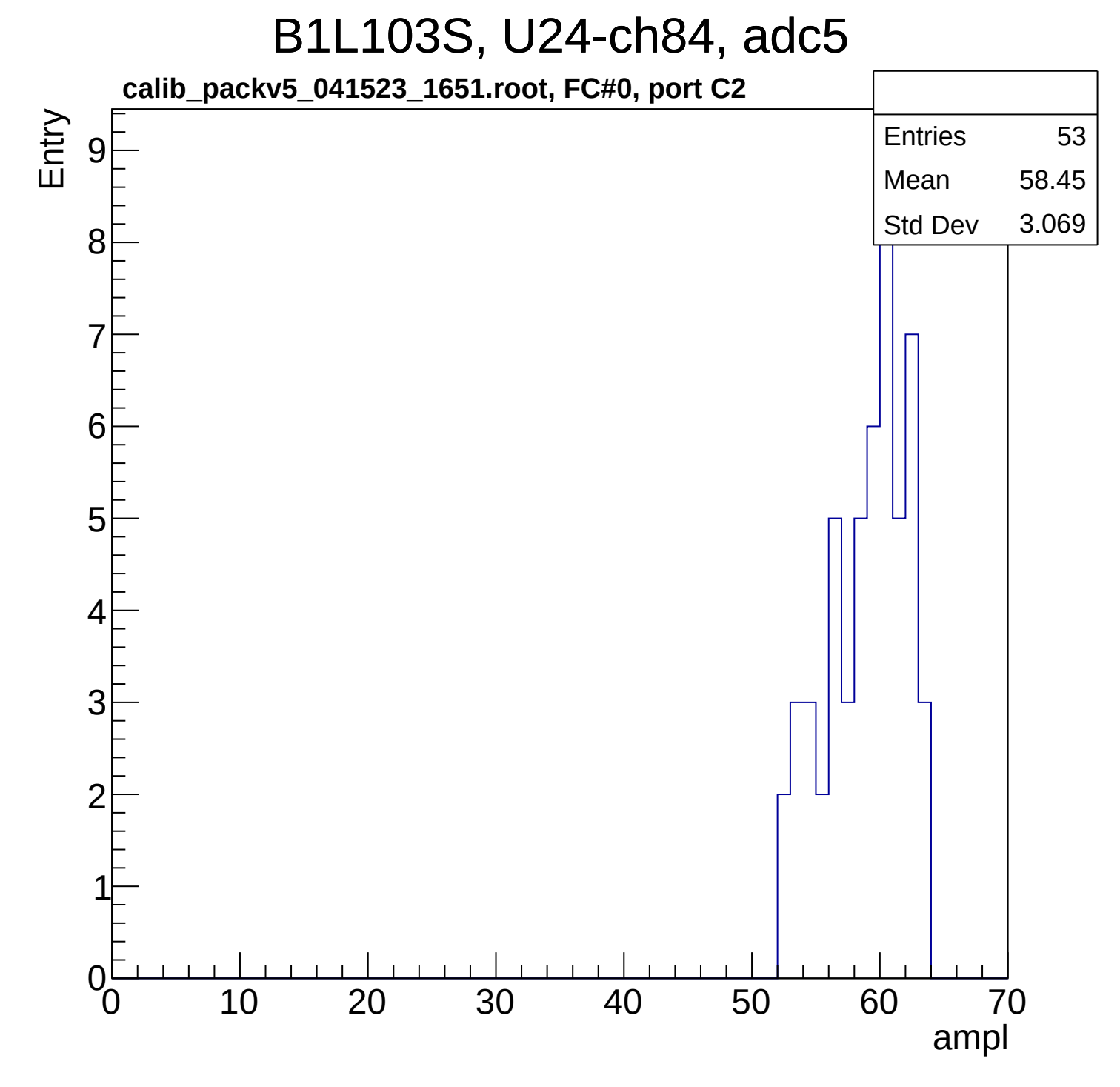
60
70


B1L103S, U24-ch84, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 58.45
Std Dev 3.069
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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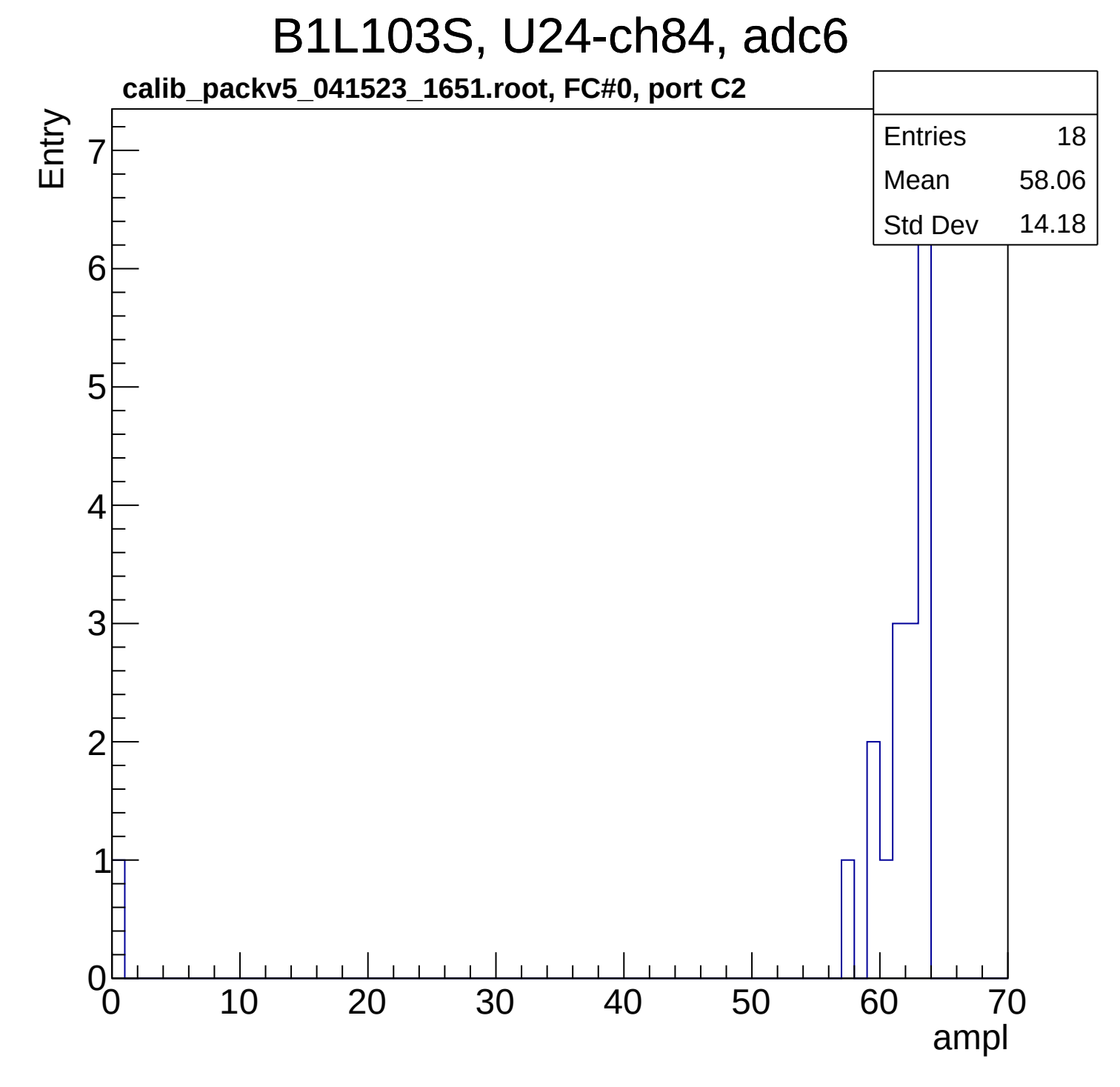
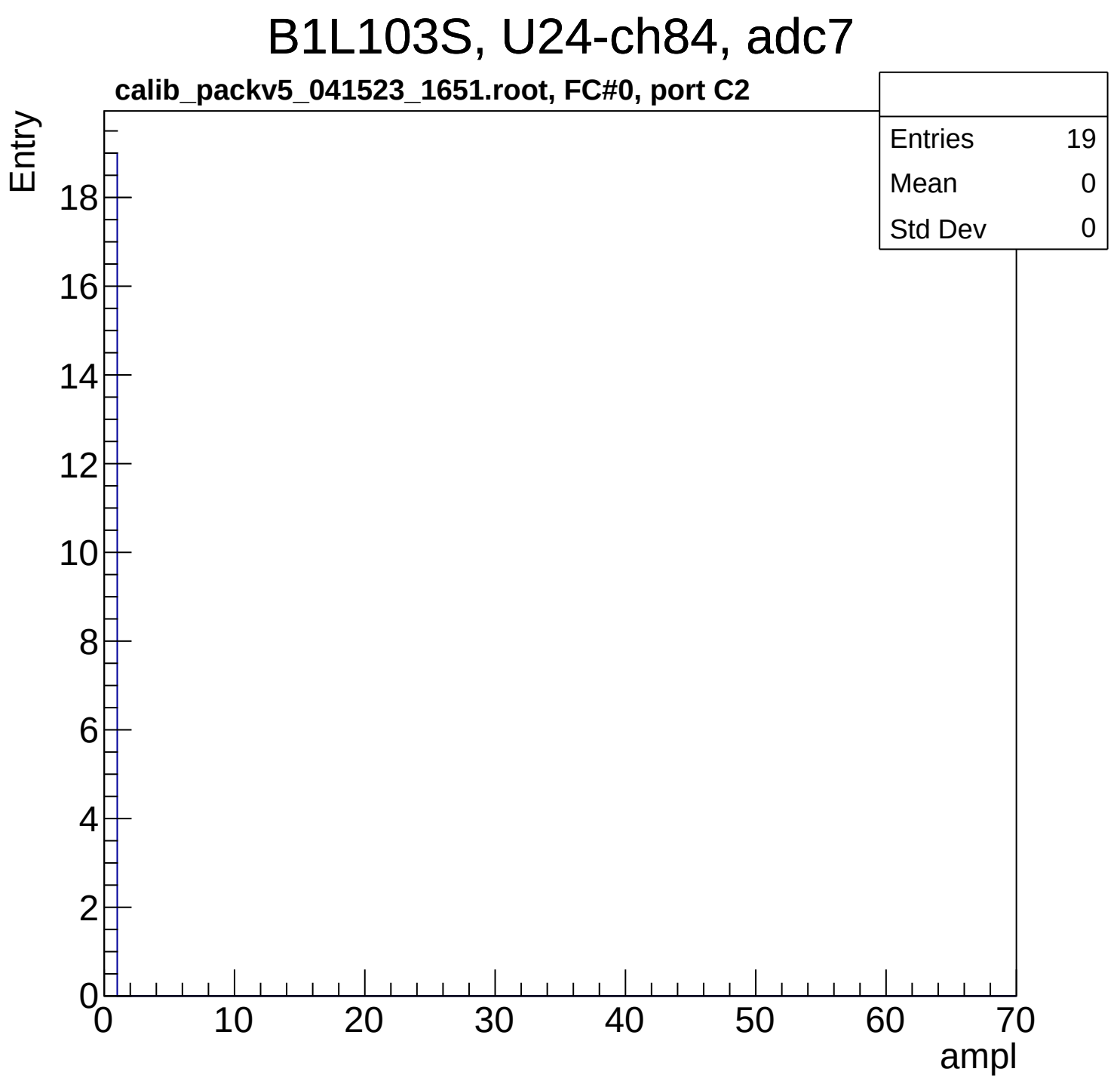
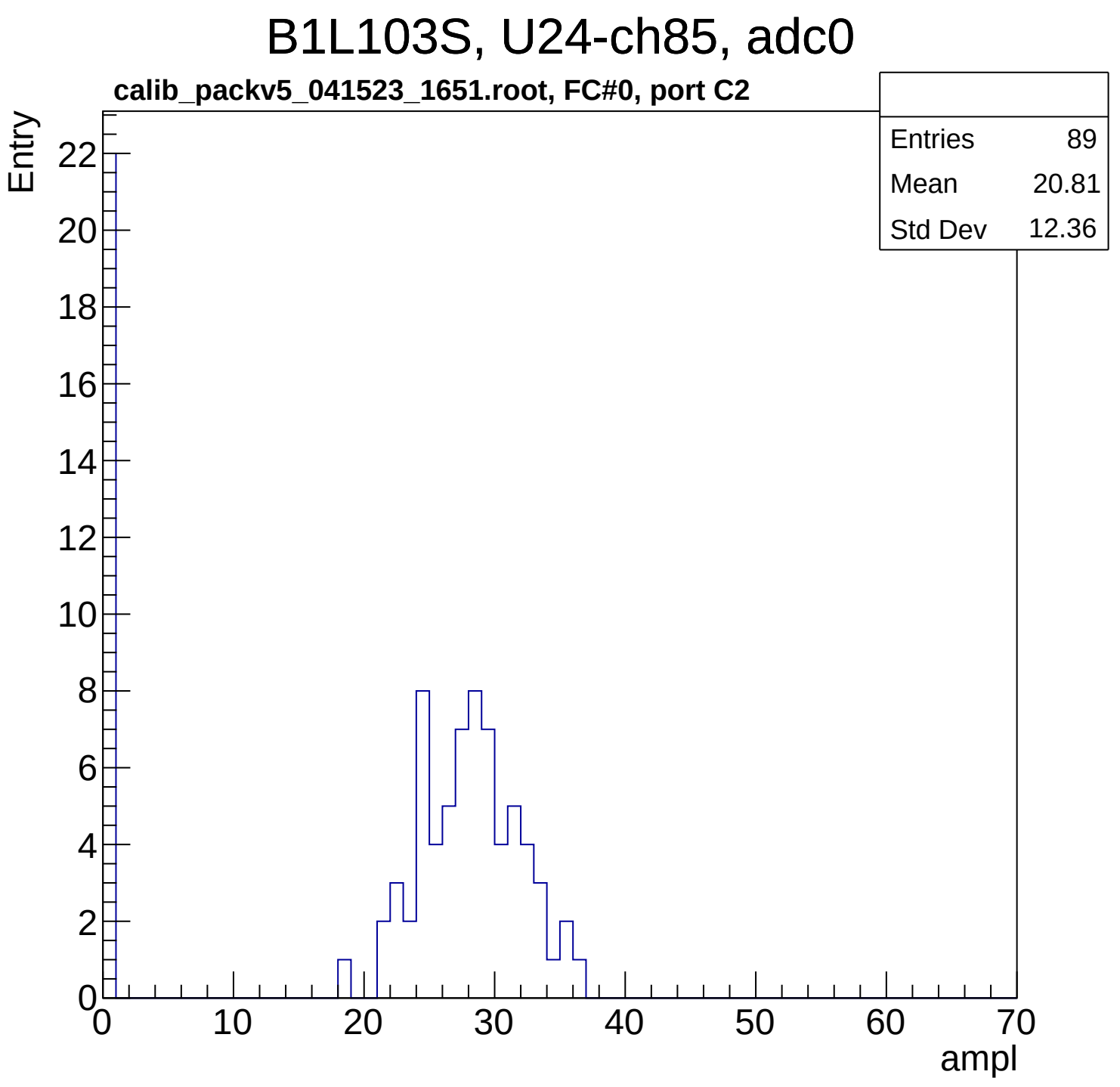
50
60
70


B1L103S, U24-ch84, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 58.06
Std Dev 14.18
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U24-ch84, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch85, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 89
Mean 20.81
Std Dev 12.36
Entry
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10
12
14
16
18
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22
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10
20
30
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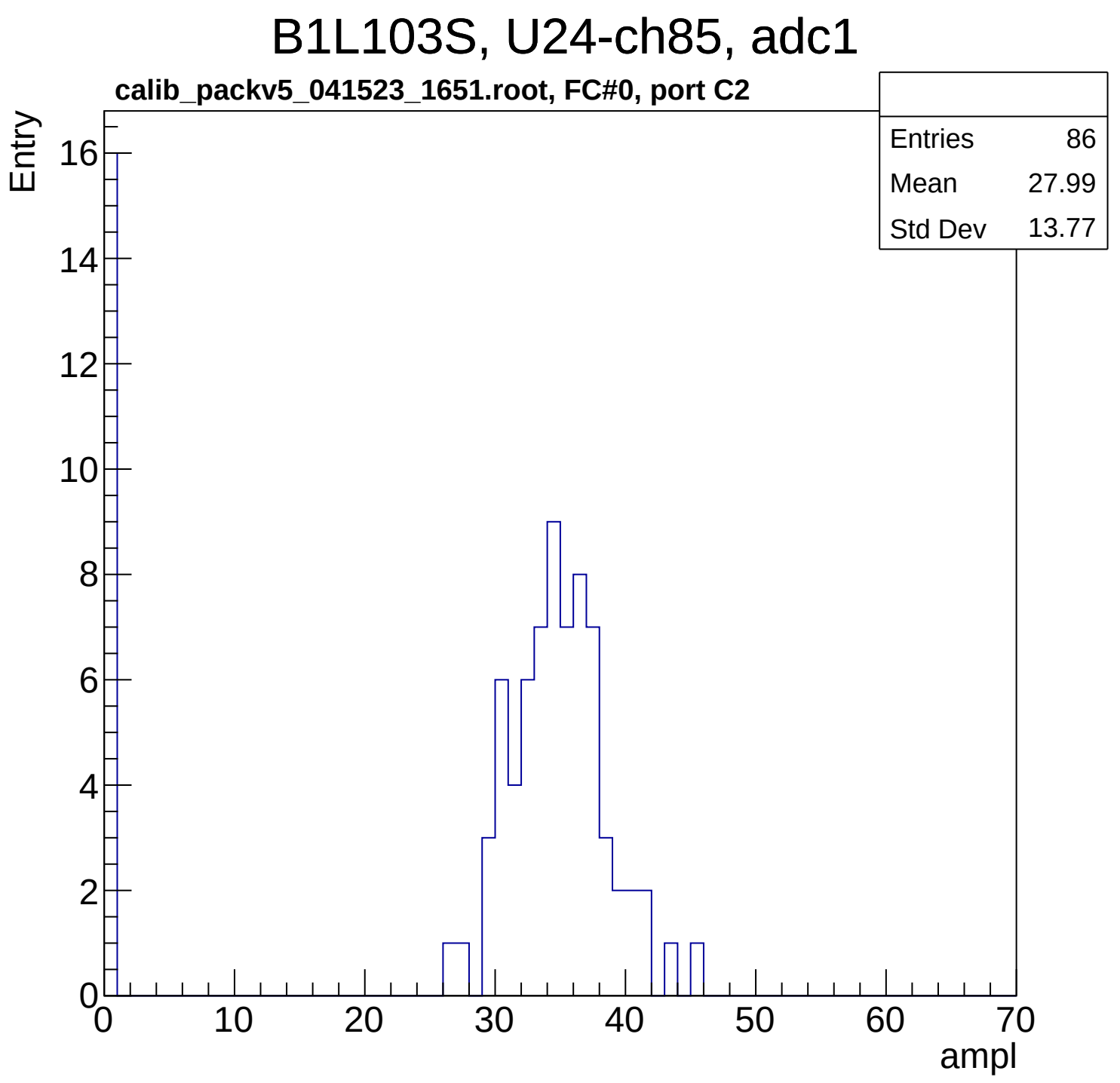
50
60
70
ampl


B1L103S, U24-ch85, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 27.99
Std Dev 13.77
Entry
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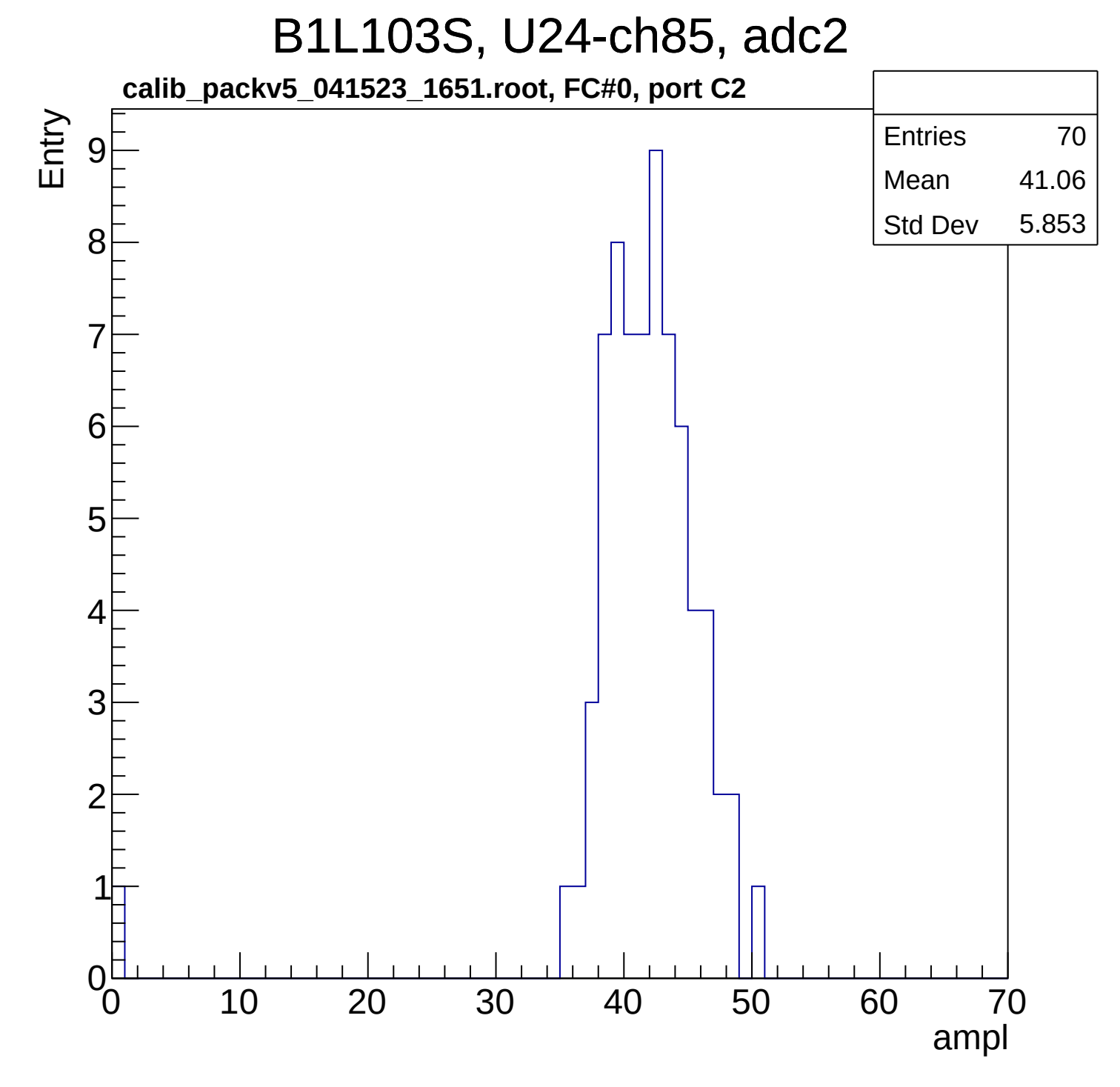
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch85, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 41.06
Std Dev 5.853
Entry
ampl
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2
3
4
5
6
7
8
9
0
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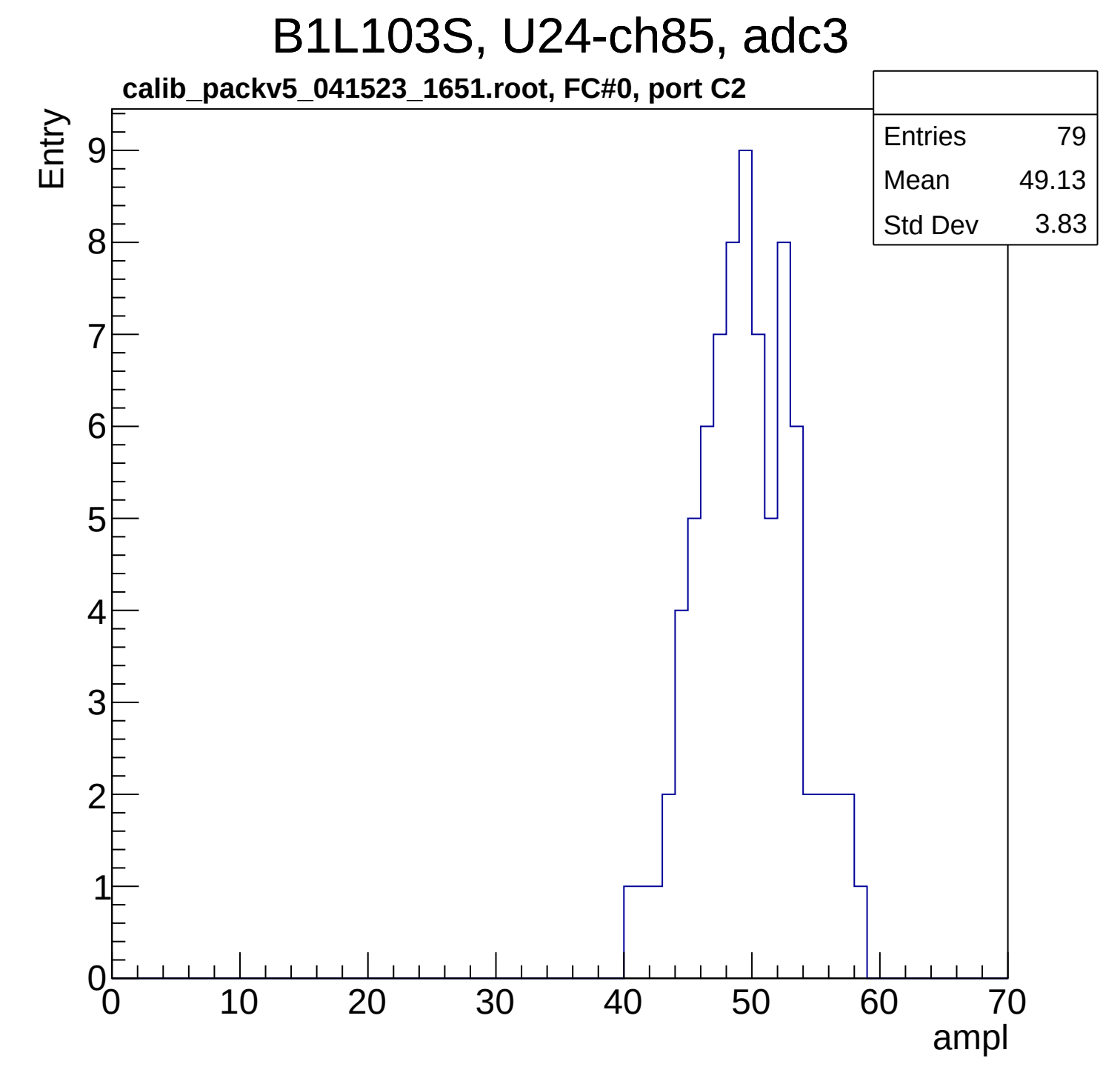
B1L103S, U24-ch85, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 49.13
Std Dev 3.83
Entry
ampl
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3
4
5
6
7
8
9
0
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40
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60
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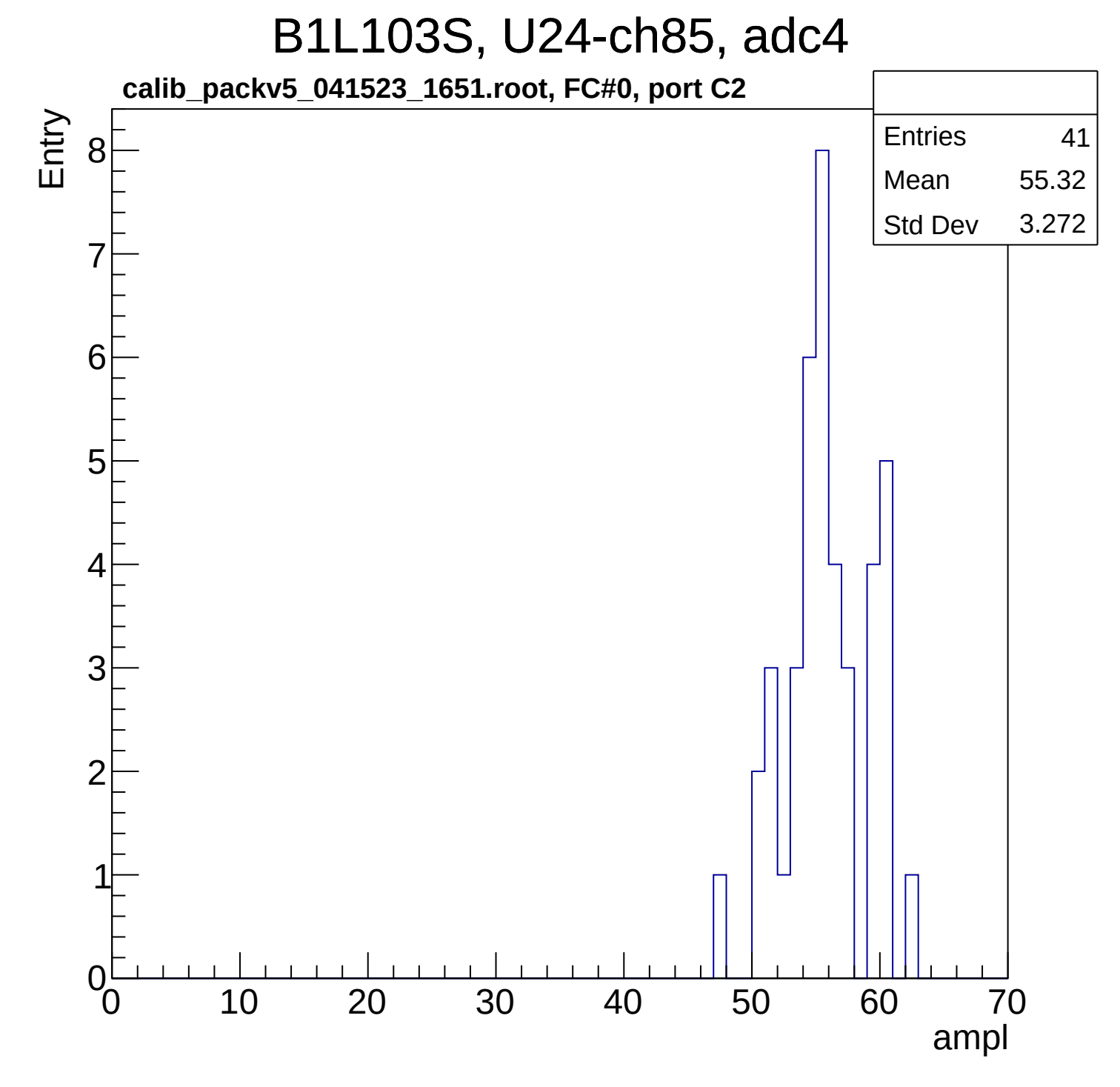
B1L103S, U24-ch85, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 41
Mean 55.32
Std Dev 3.272
Entry
ampl
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2
3
4
5
6
7
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0
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40
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60
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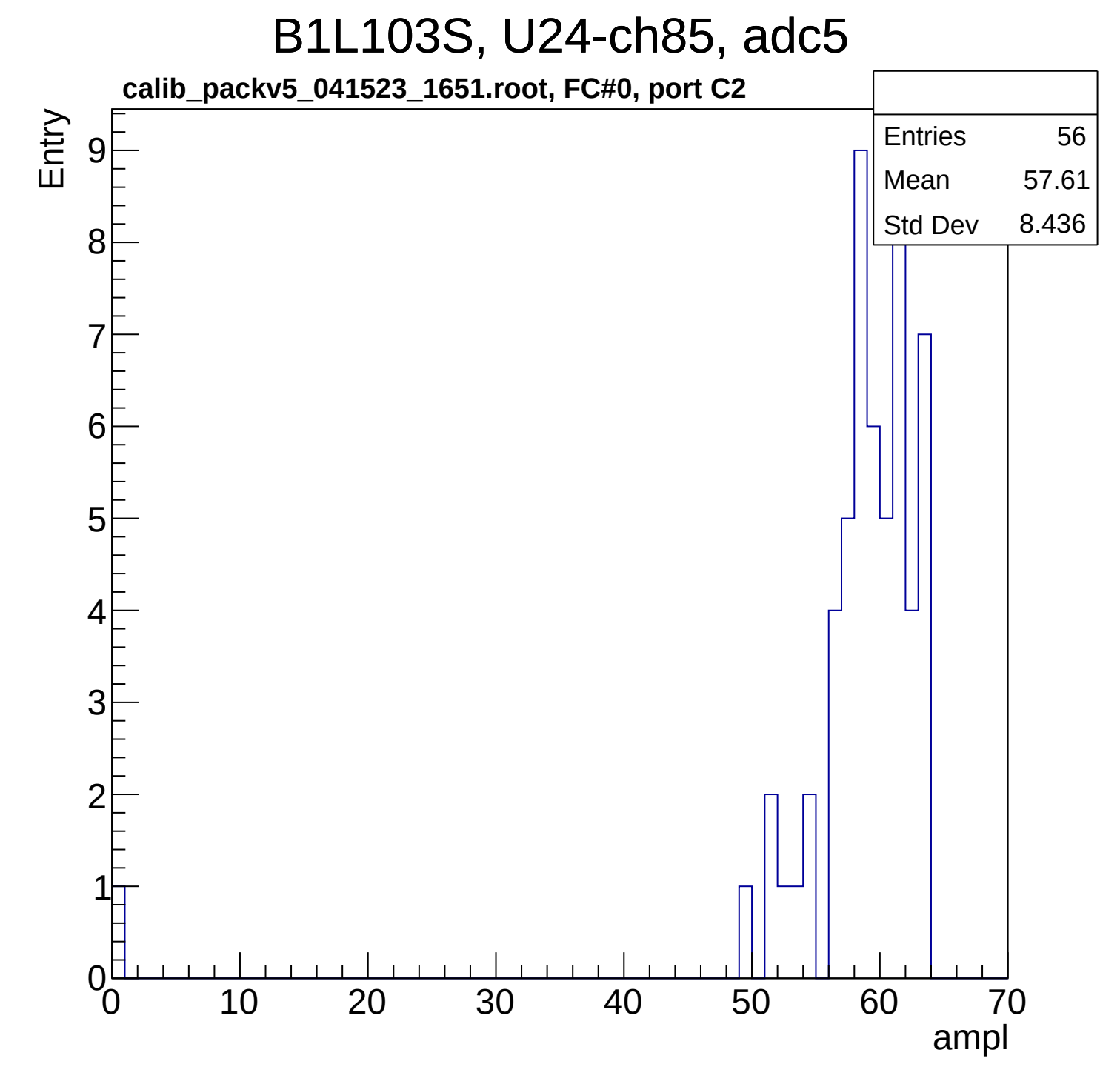
B1L103S, U24-ch85, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 57.61
Std Dev 8.436
Entry
ampl
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2
3
4
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8
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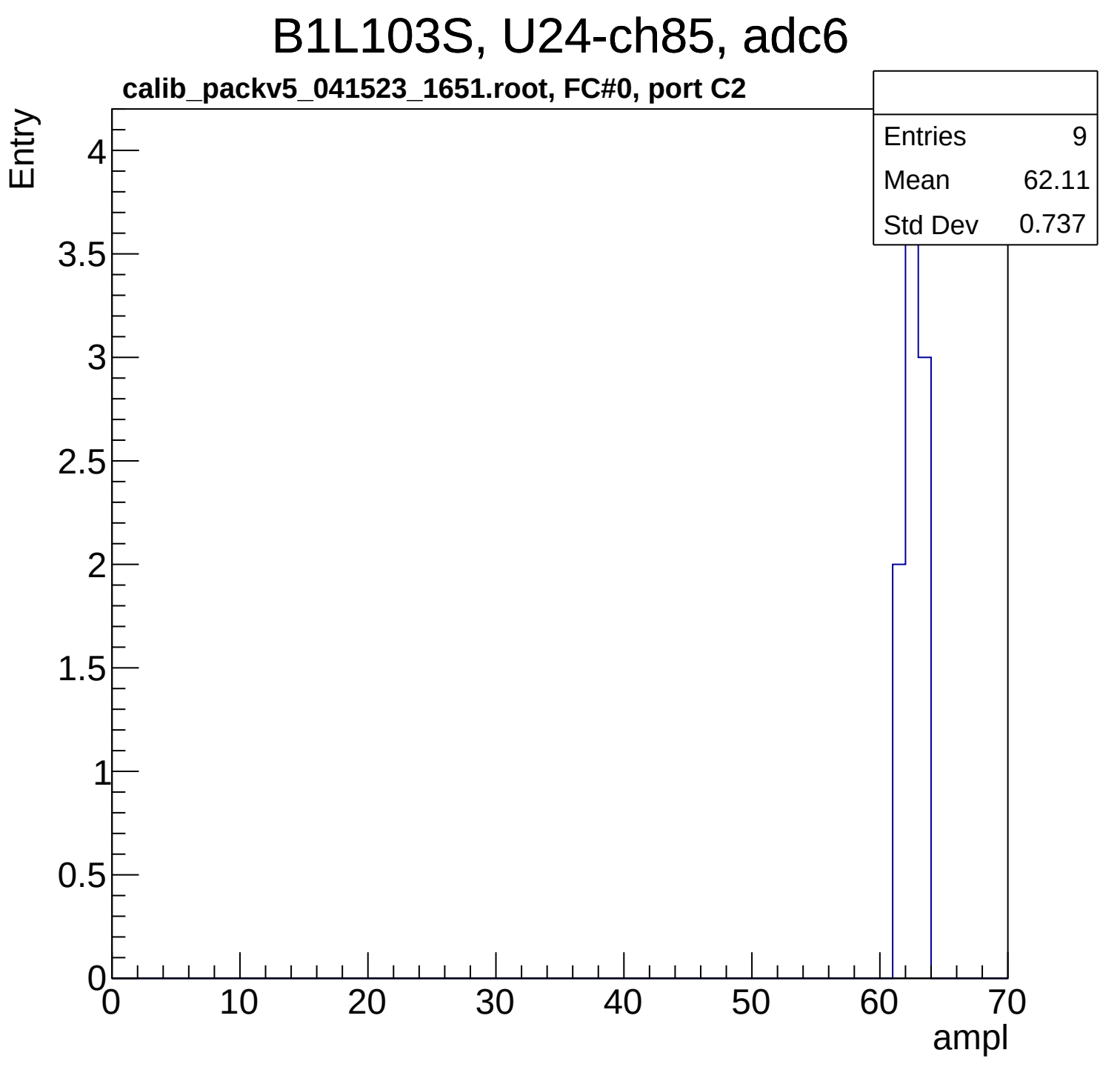
B1L103S, U24-ch85, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 9
Mean 62.11
Std Dev 0.737
Entry
ampl
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0.5
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1.5
2
2.5
3
3.5
4
0
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40
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60
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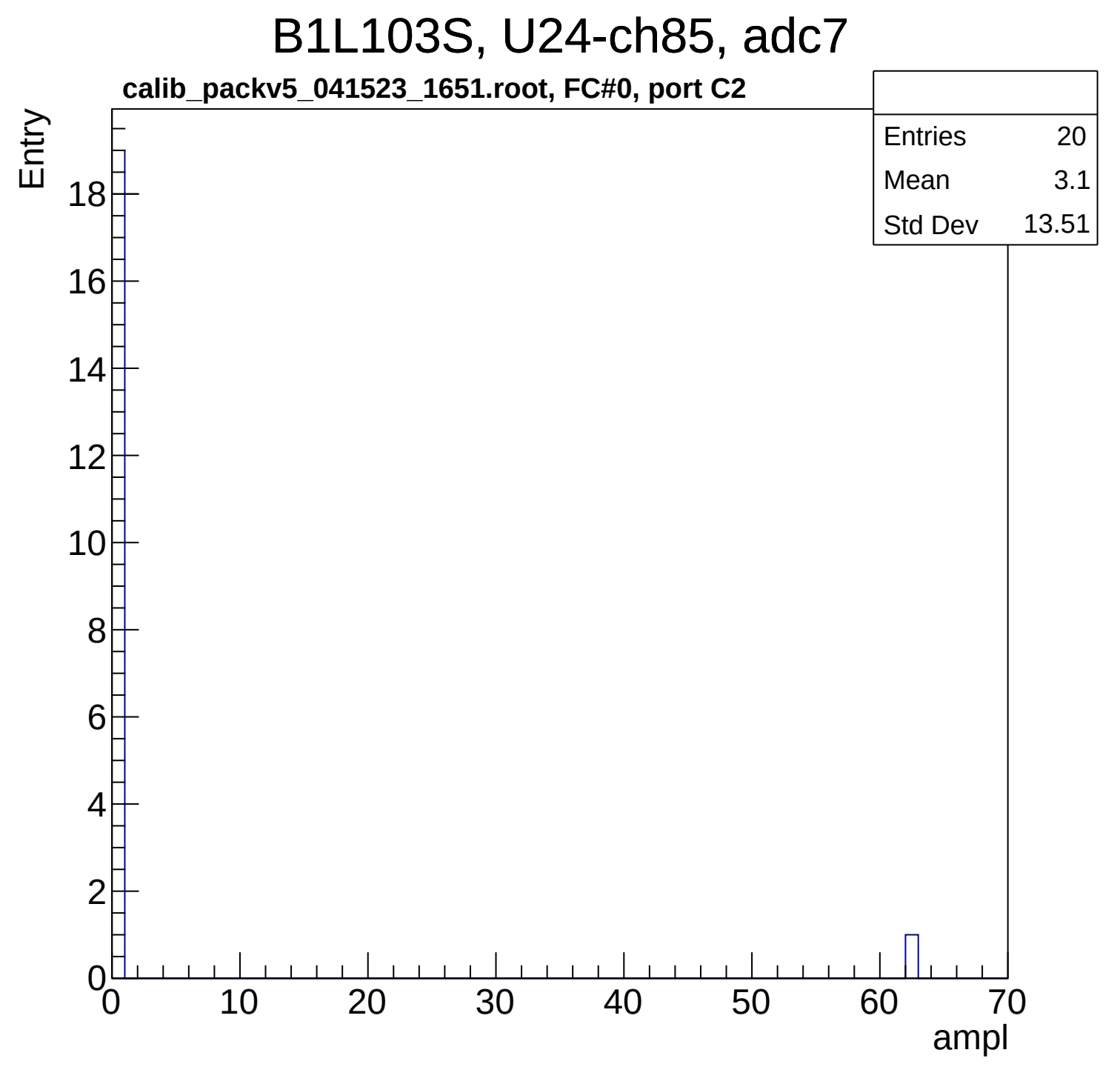
B1L103S, U24-ch85, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.1
Std Dev 13.51
Entry
0
2
4
6
8
10
12
14
16
18
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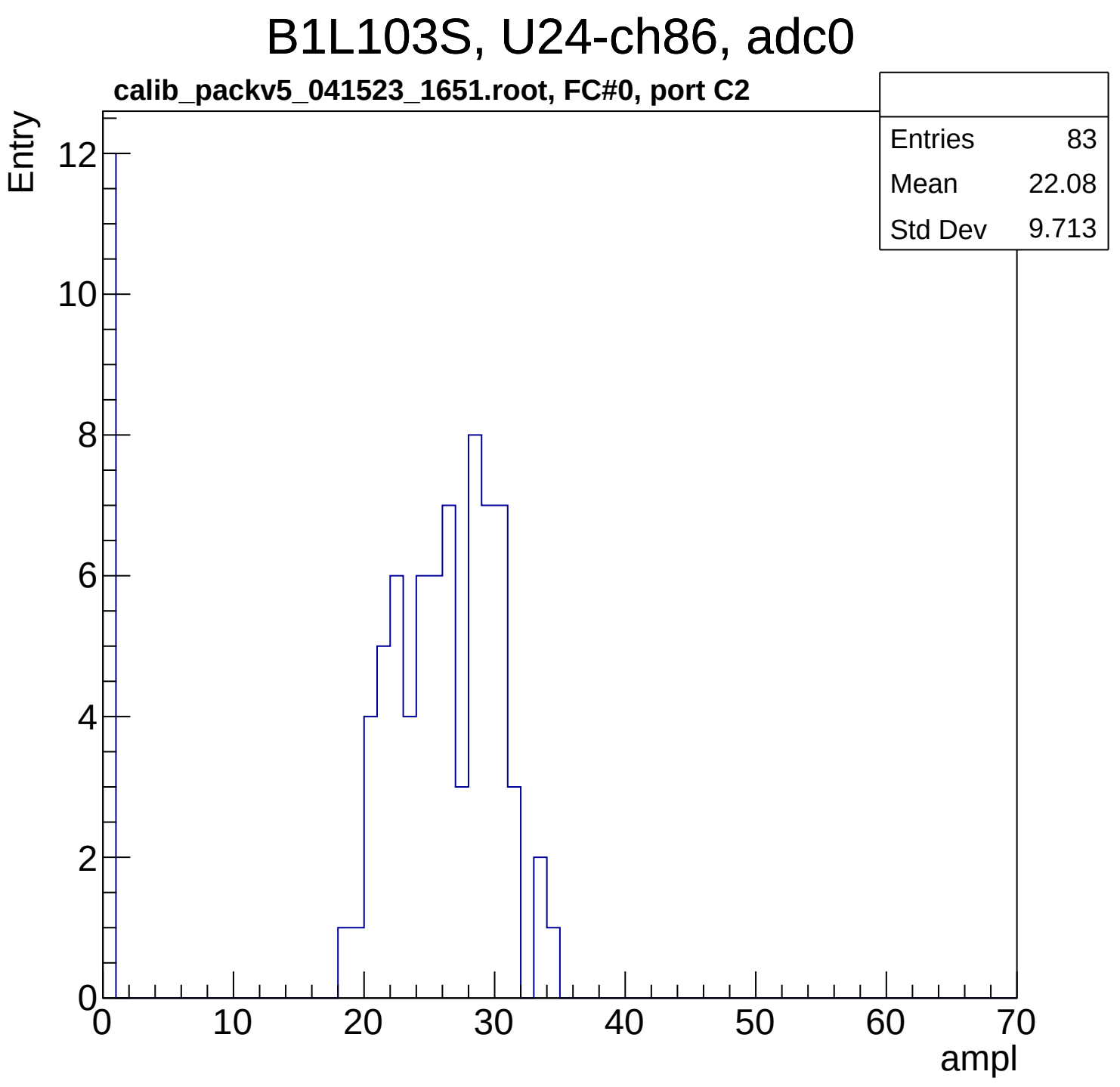
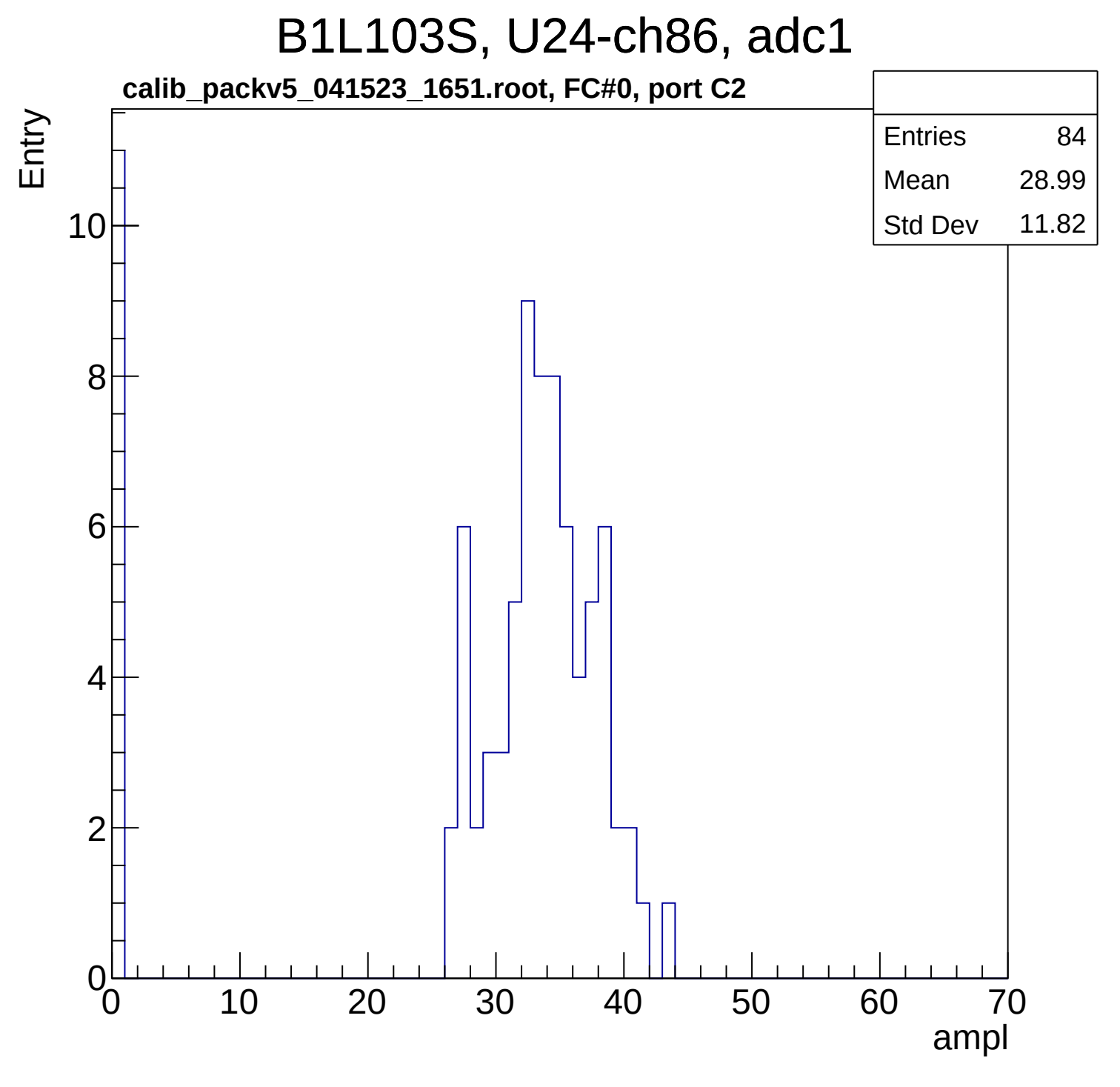
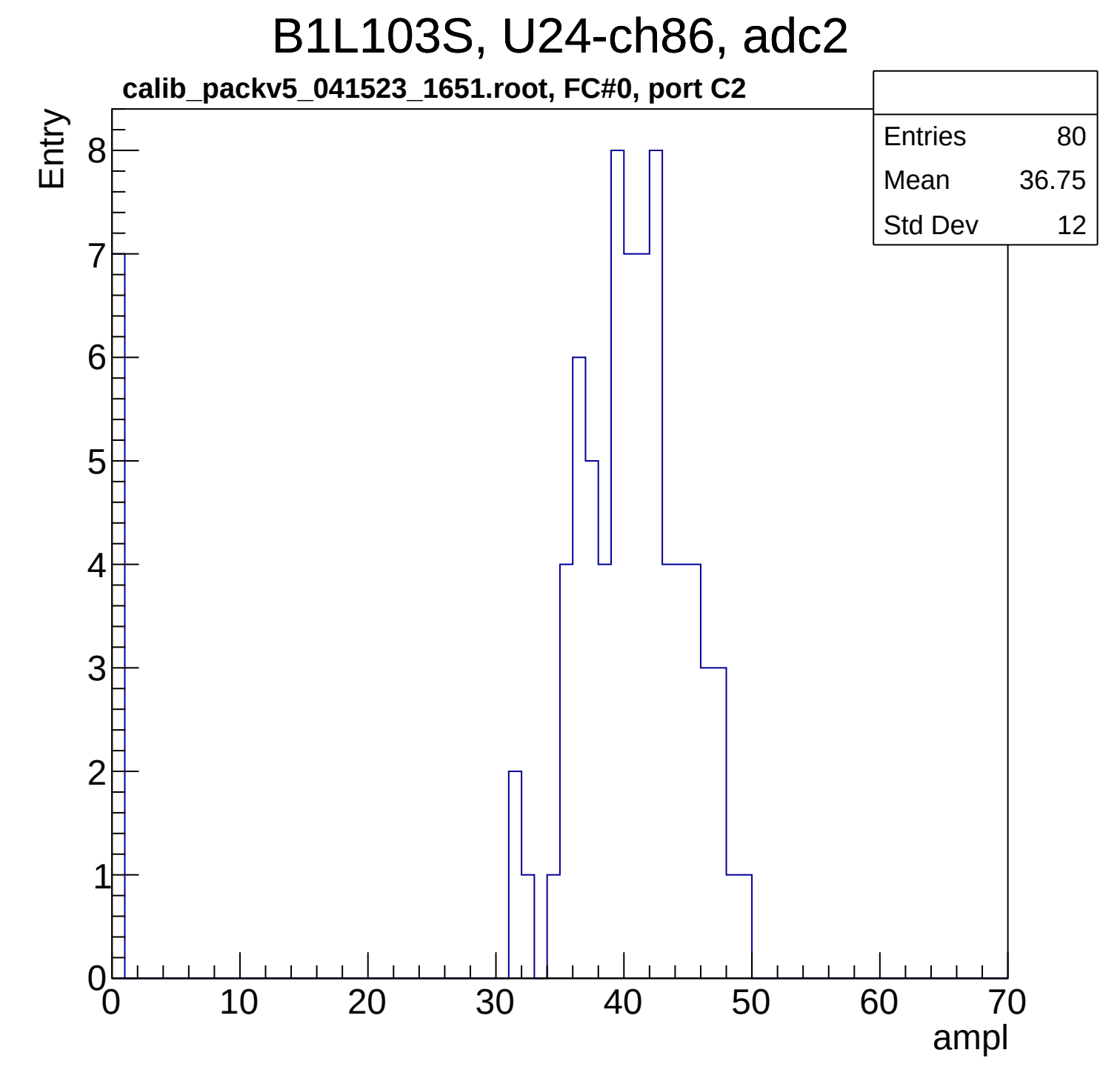
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch86, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 22.08
Std Dev 9.713
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch86, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 28.99
Std Dev 11.82
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch86, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 36.75
Std Dev 12
Entry
ampl
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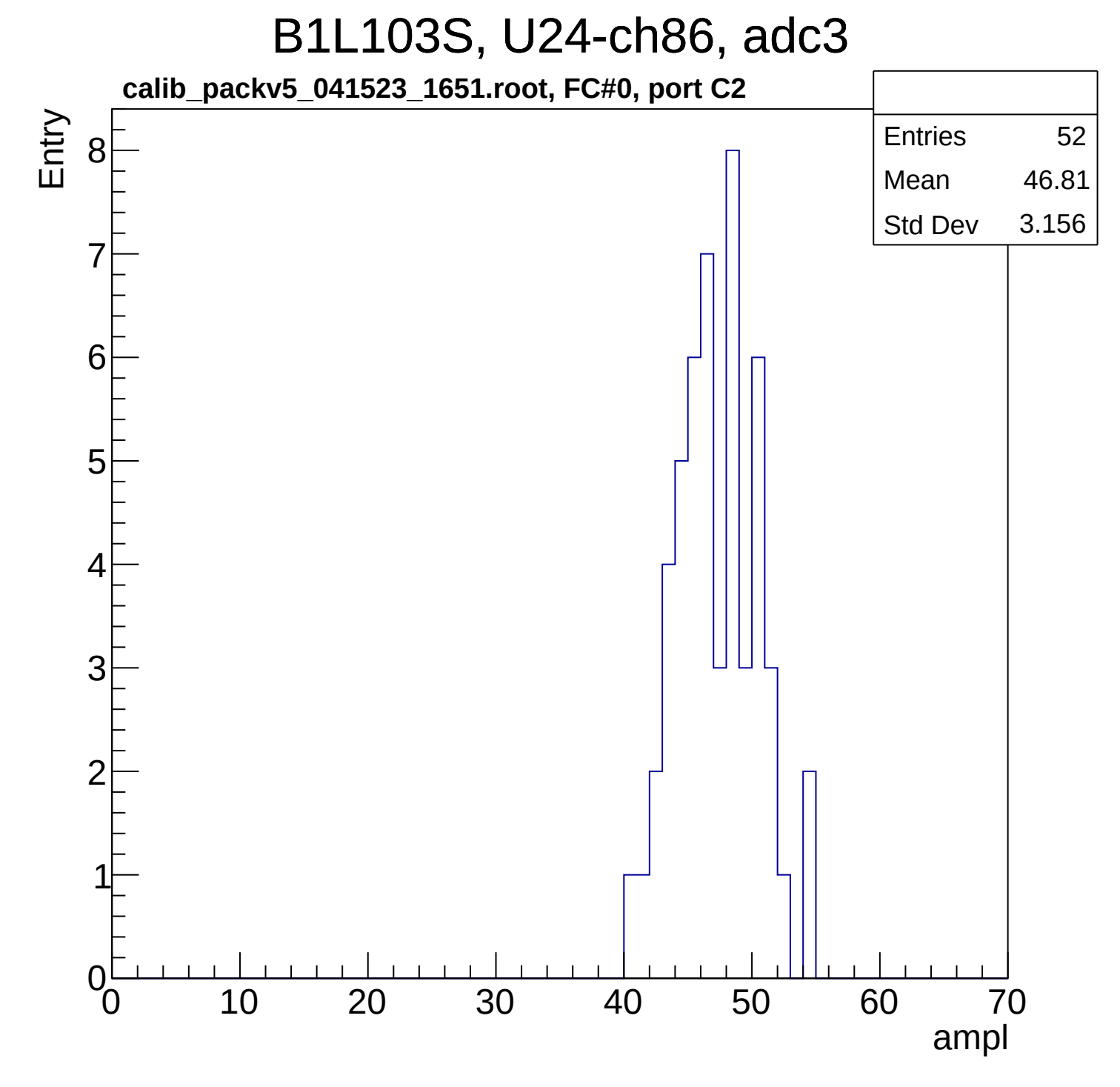
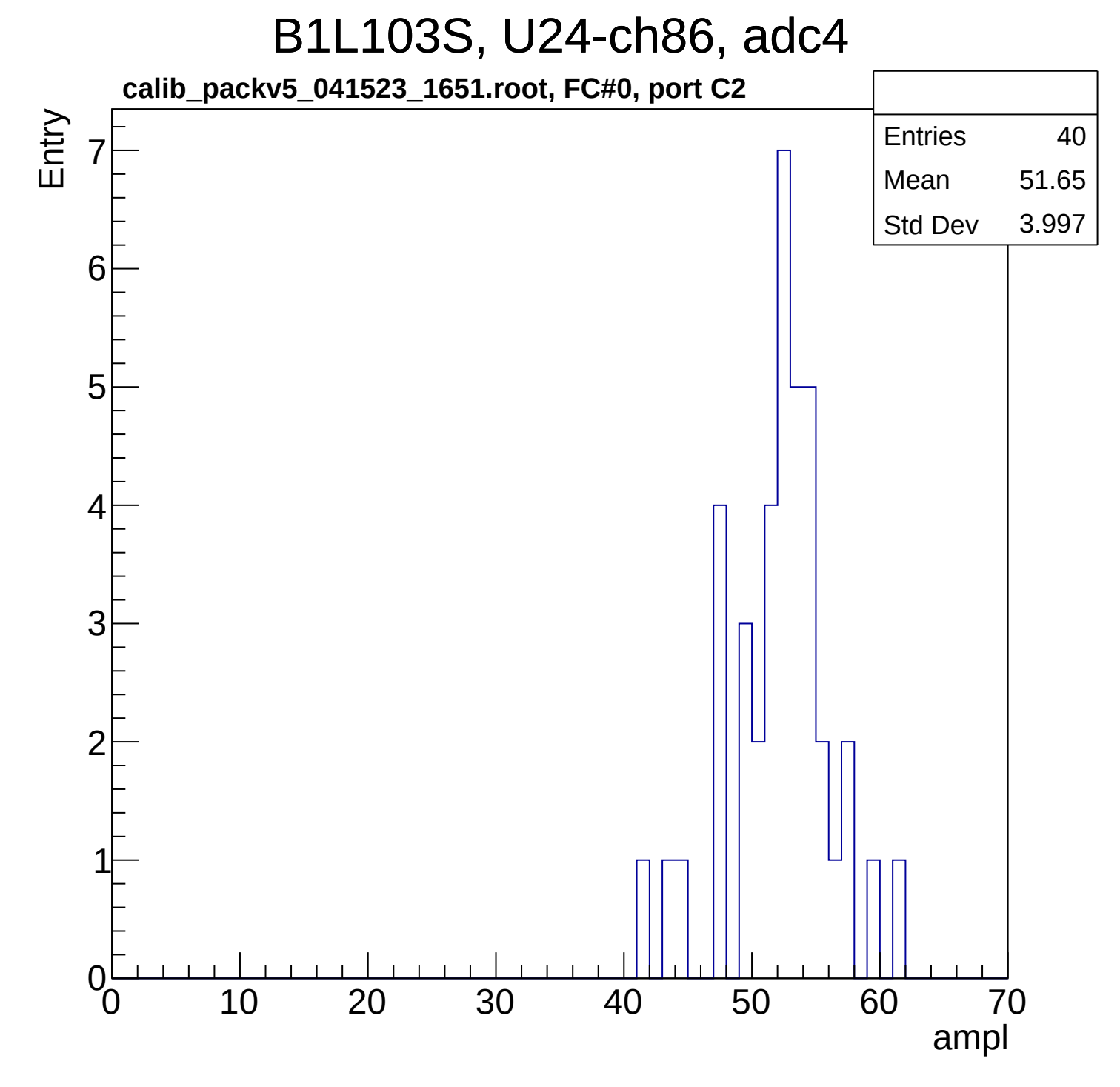
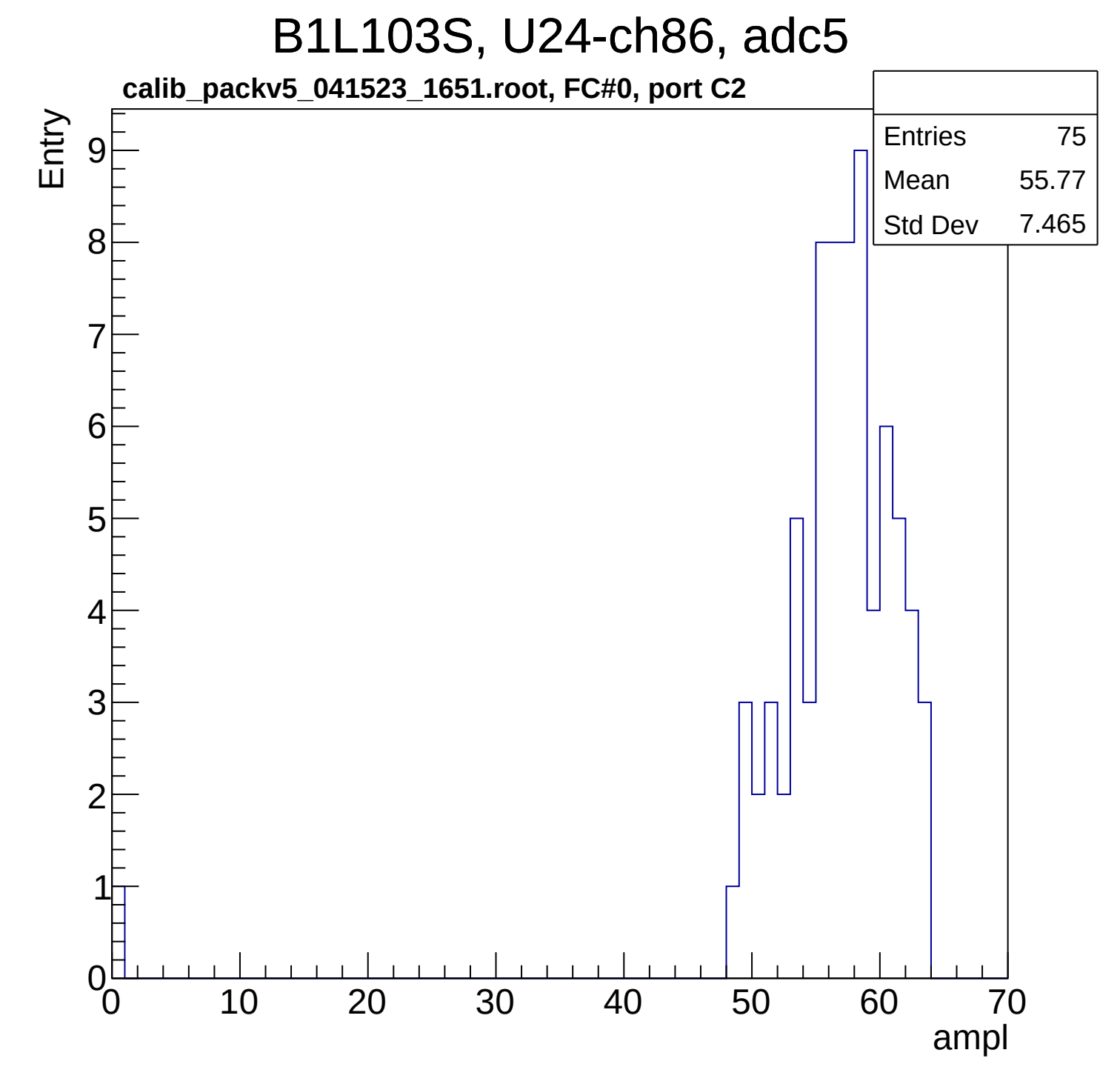
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U24-ch86, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 46.81
Std Dev 3.156
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U24-ch86, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 40
Mean 51.65
Std Dev 3.997
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U24-ch86, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 55.77
Std Dev 7.465
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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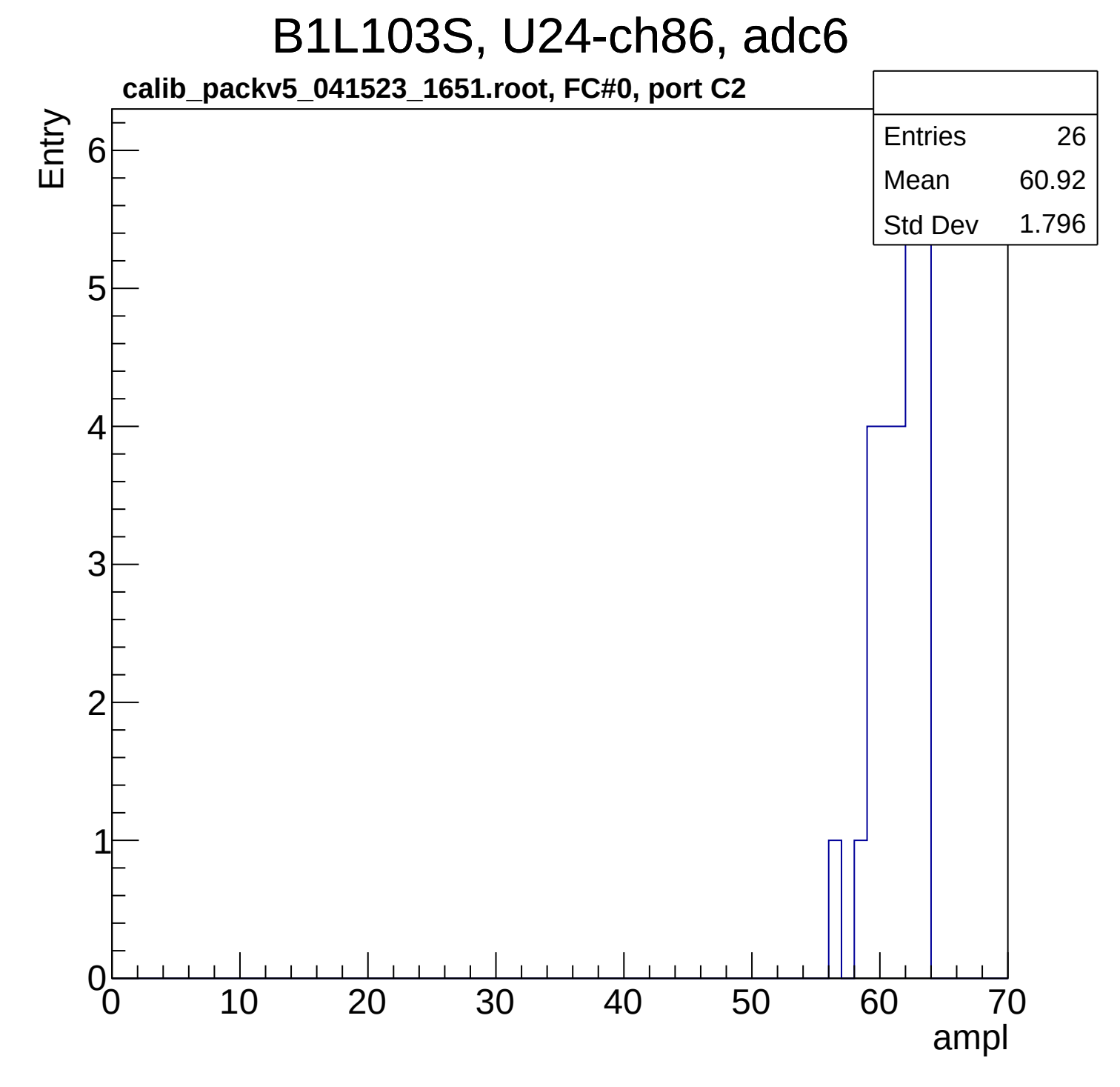
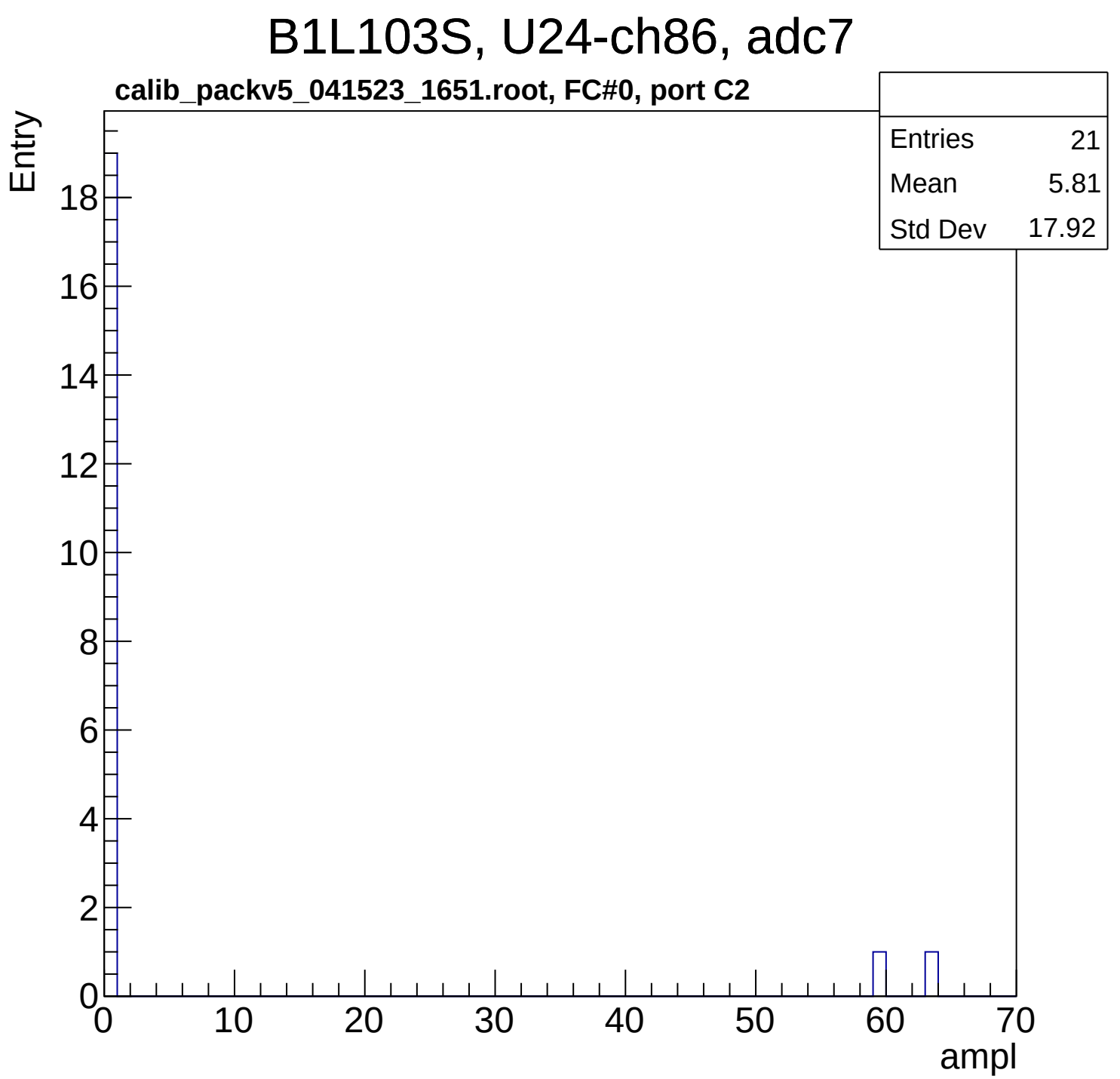
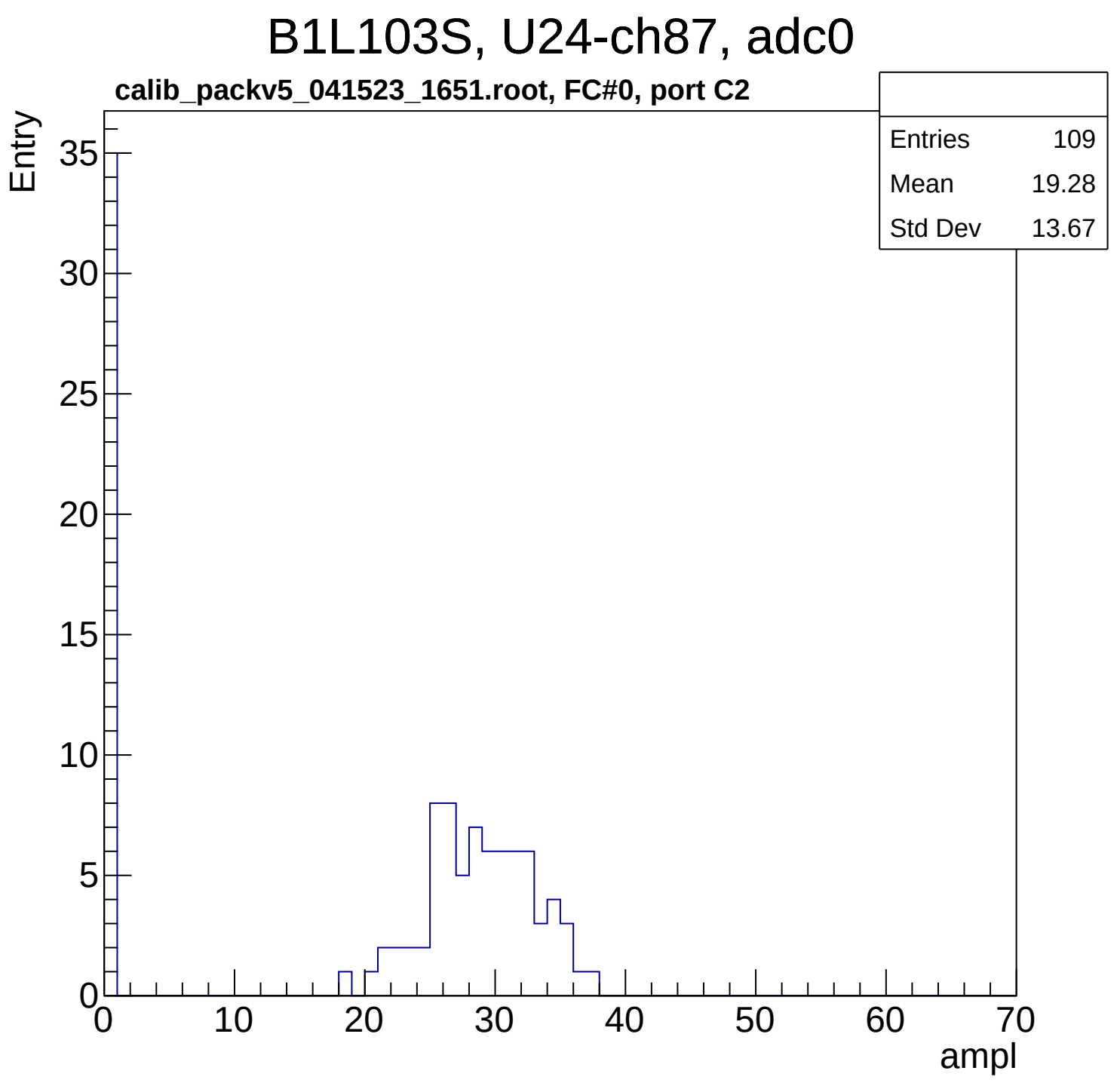
40
50
60
70


B1L103S, U24-ch86, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 26
Mean 60.92
Std Dev 1.796
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U24-ch86, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 5.81
Std Dev 17.92
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch87, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 109
Mean 19.28
Std Dev 13.67
Entry
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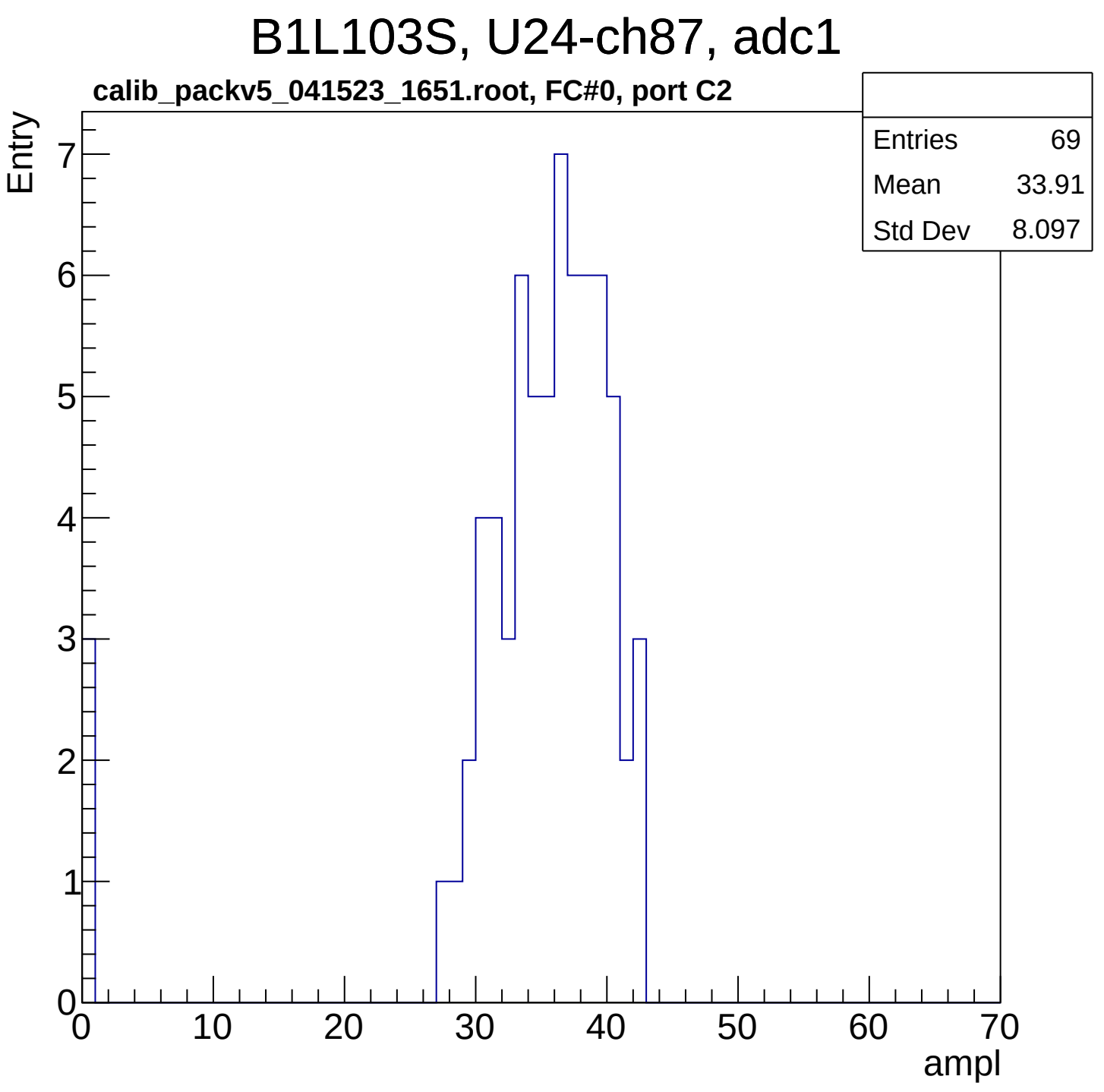
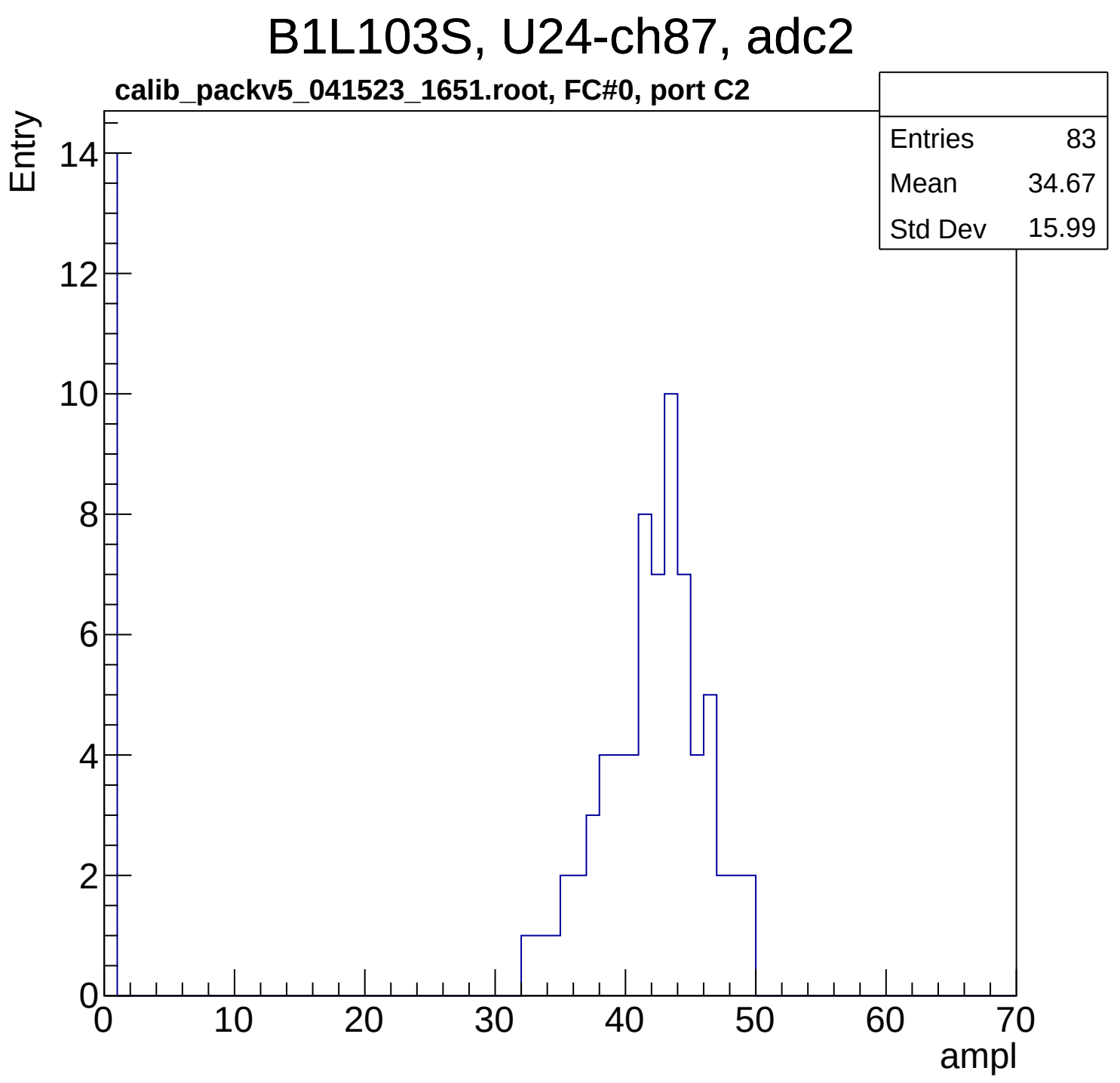
5
10
15
20
25
30
35
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch87, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 33.91
Std Dev 8.097
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U24-ch87, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 34.67
Std Dev 15.99
Entry
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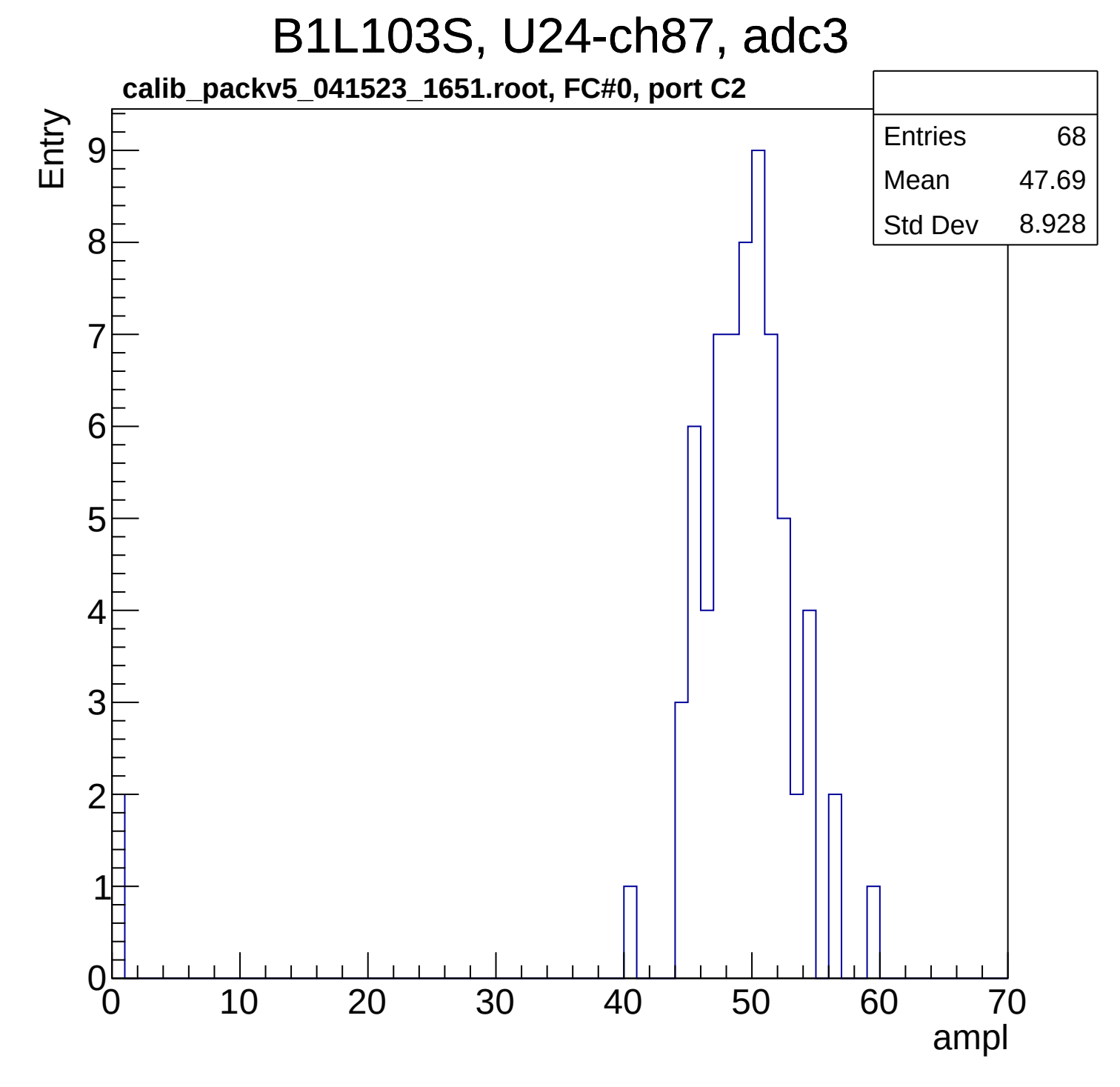
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch87, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 47.69
Std Dev 8.928
Entry
ampl
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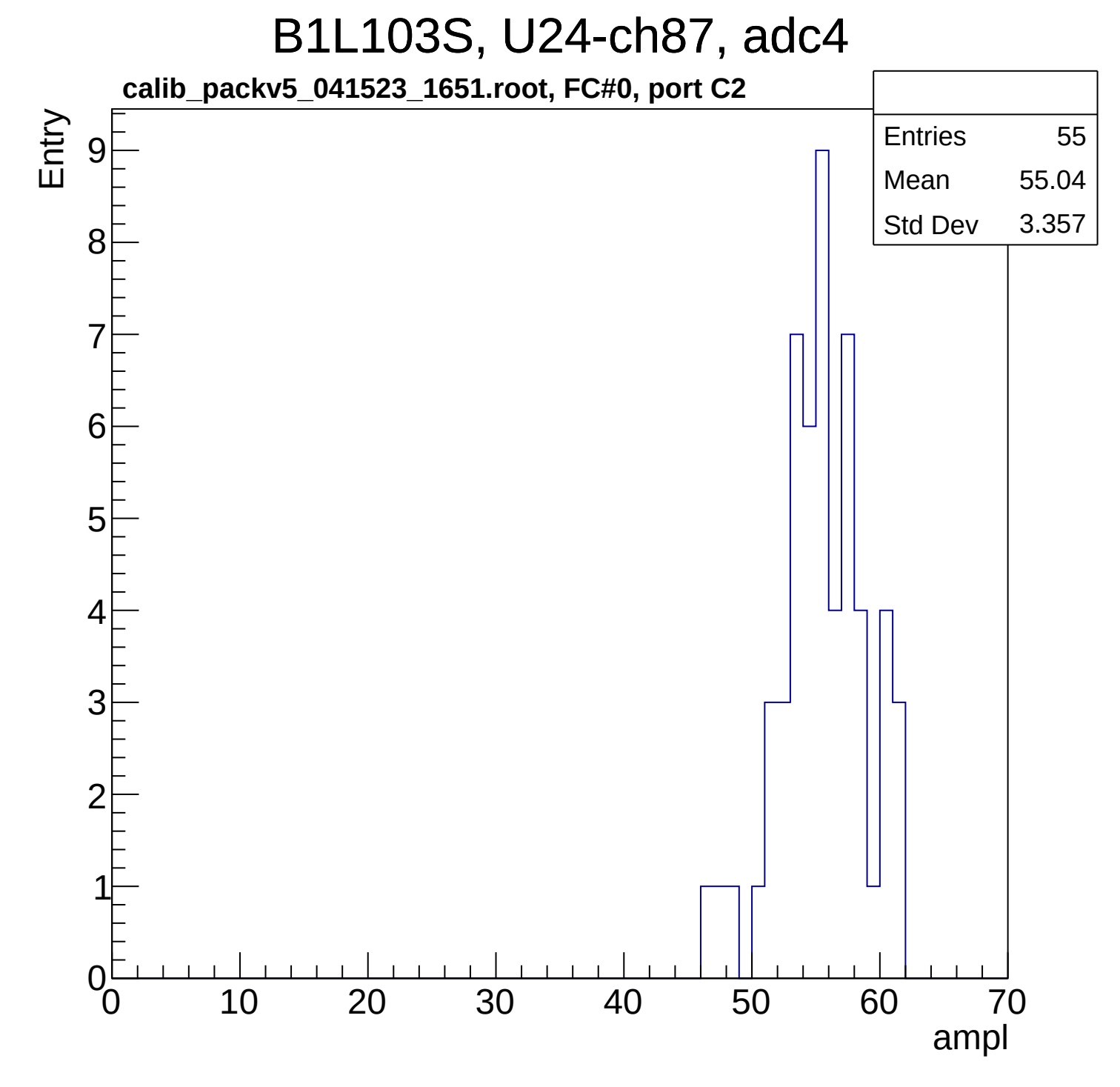
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U24-ch87, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 55.04
Std Dev 3.357
Entry
ampl
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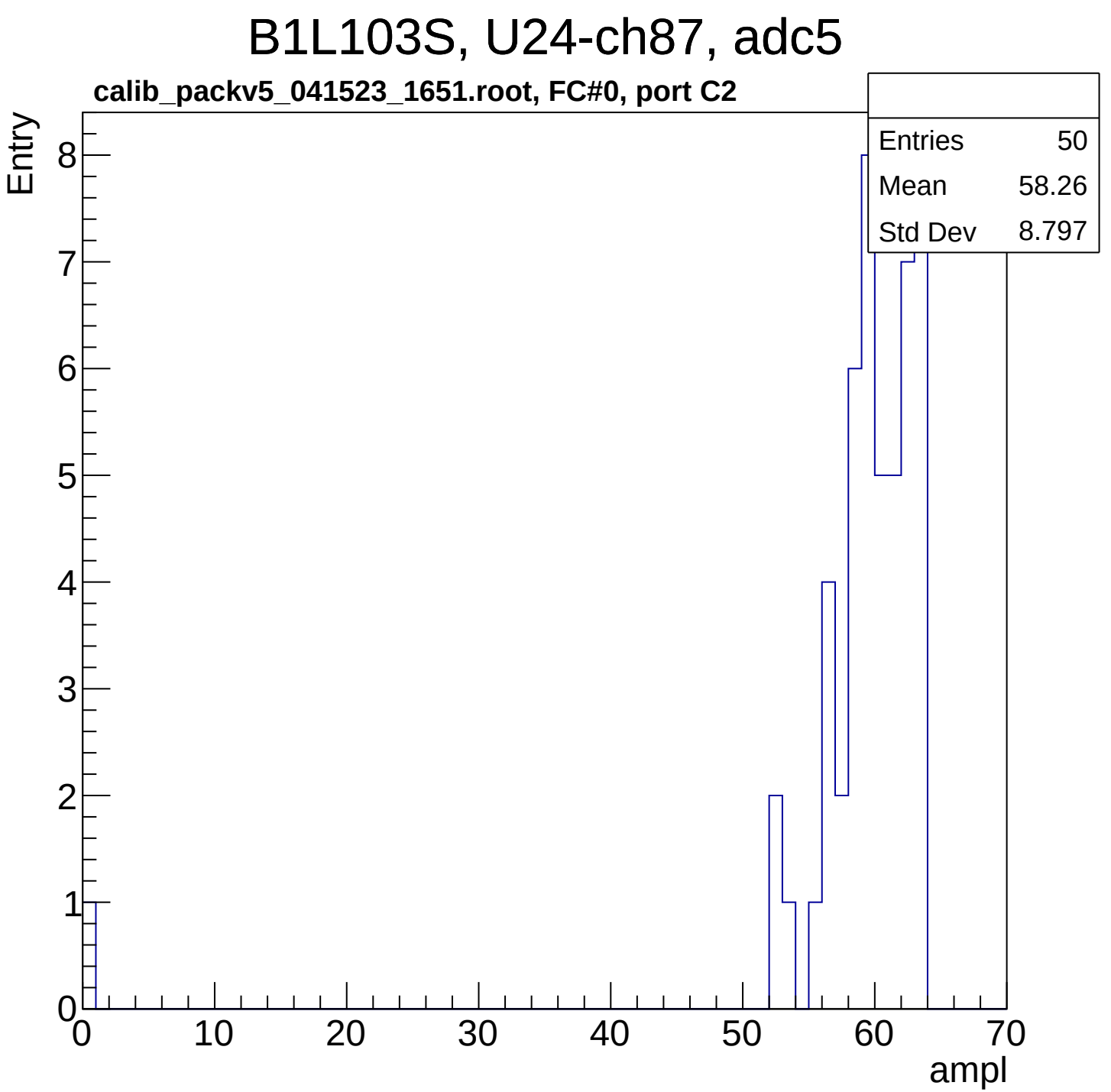
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U24-ch87, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 58.26
Std Dev 8.797
Entry
ampl
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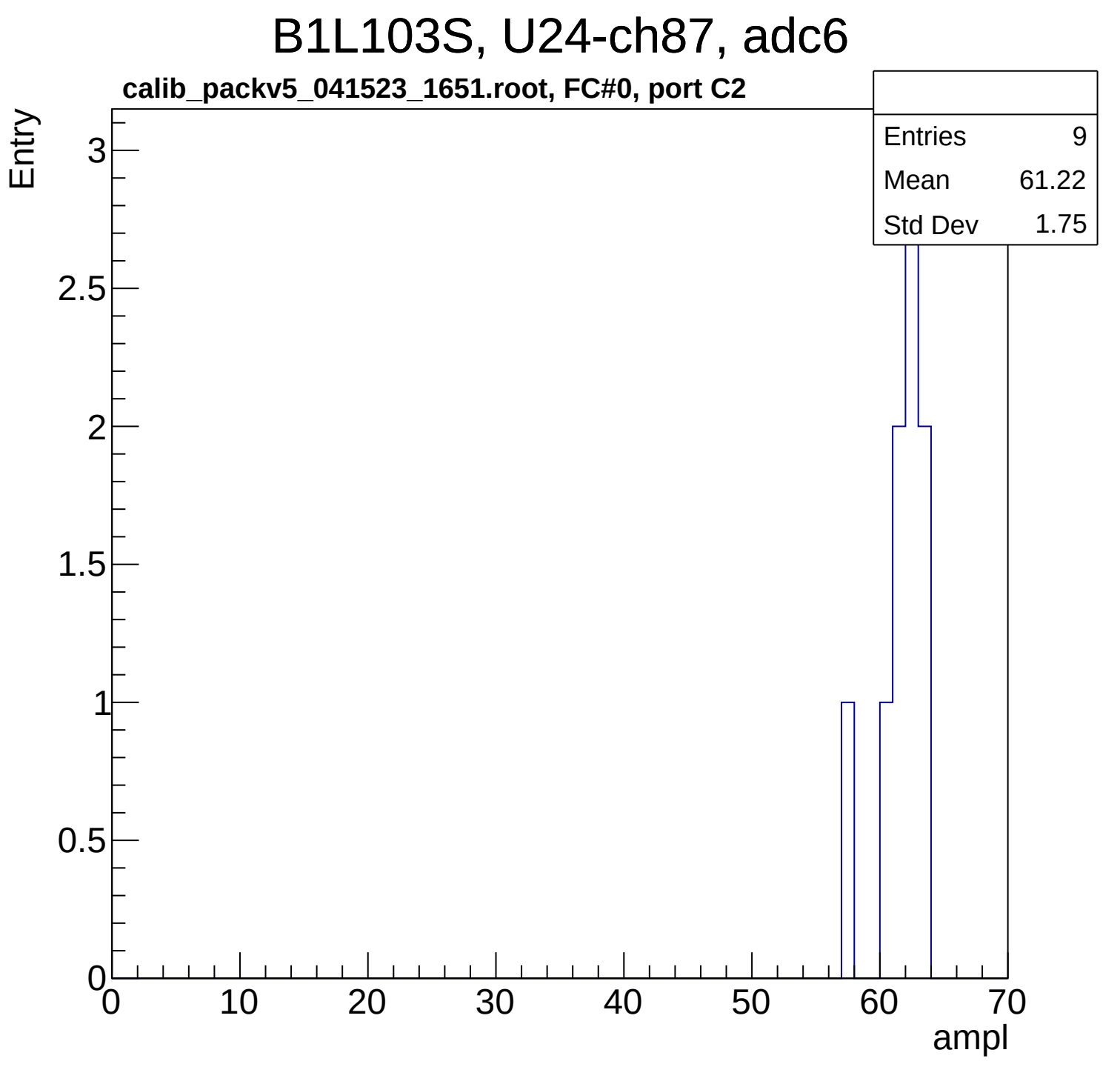
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U24-ch87, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 9
Mean 61.22
Std Dev 1.75
Entry
ampl
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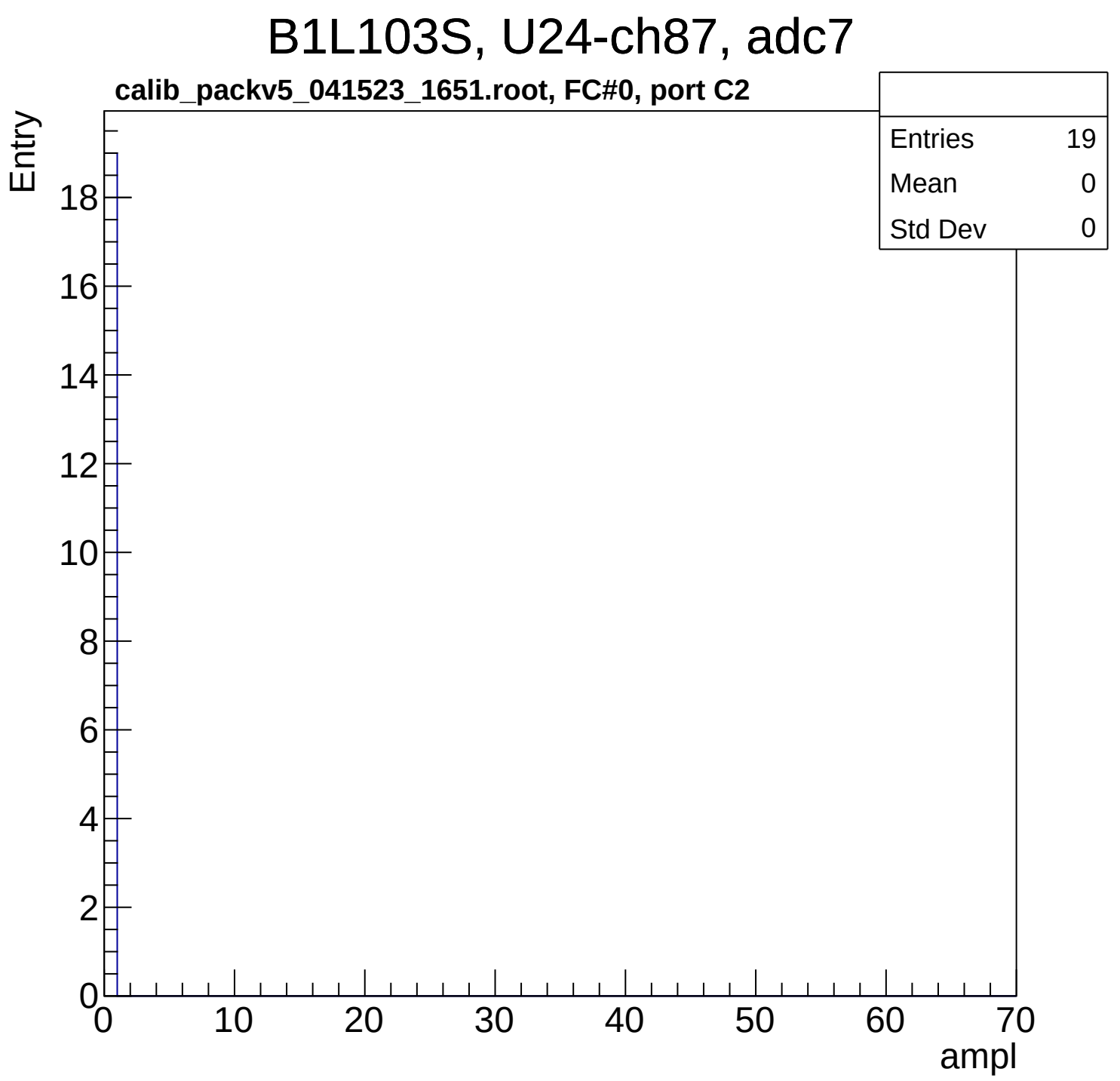
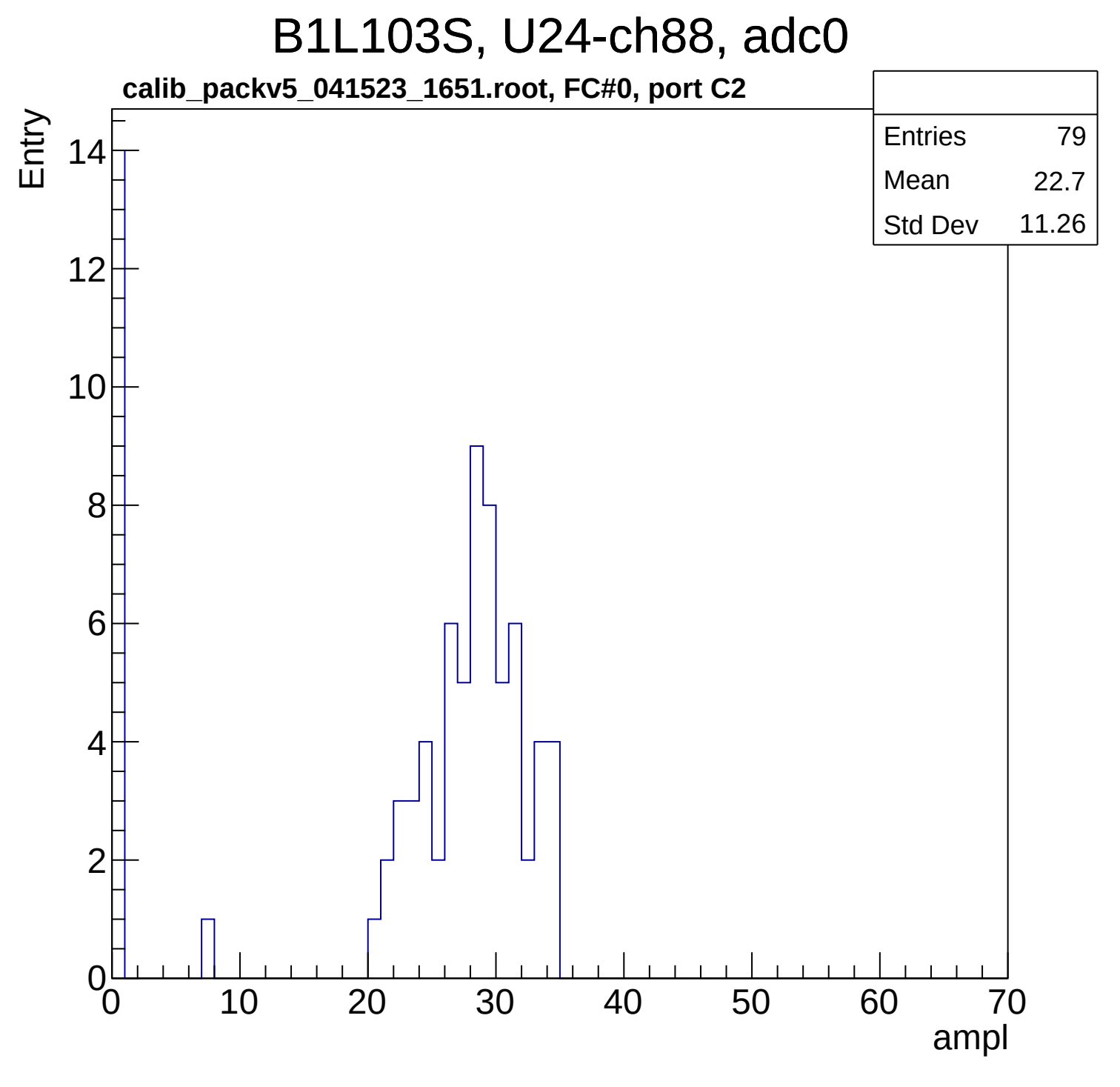
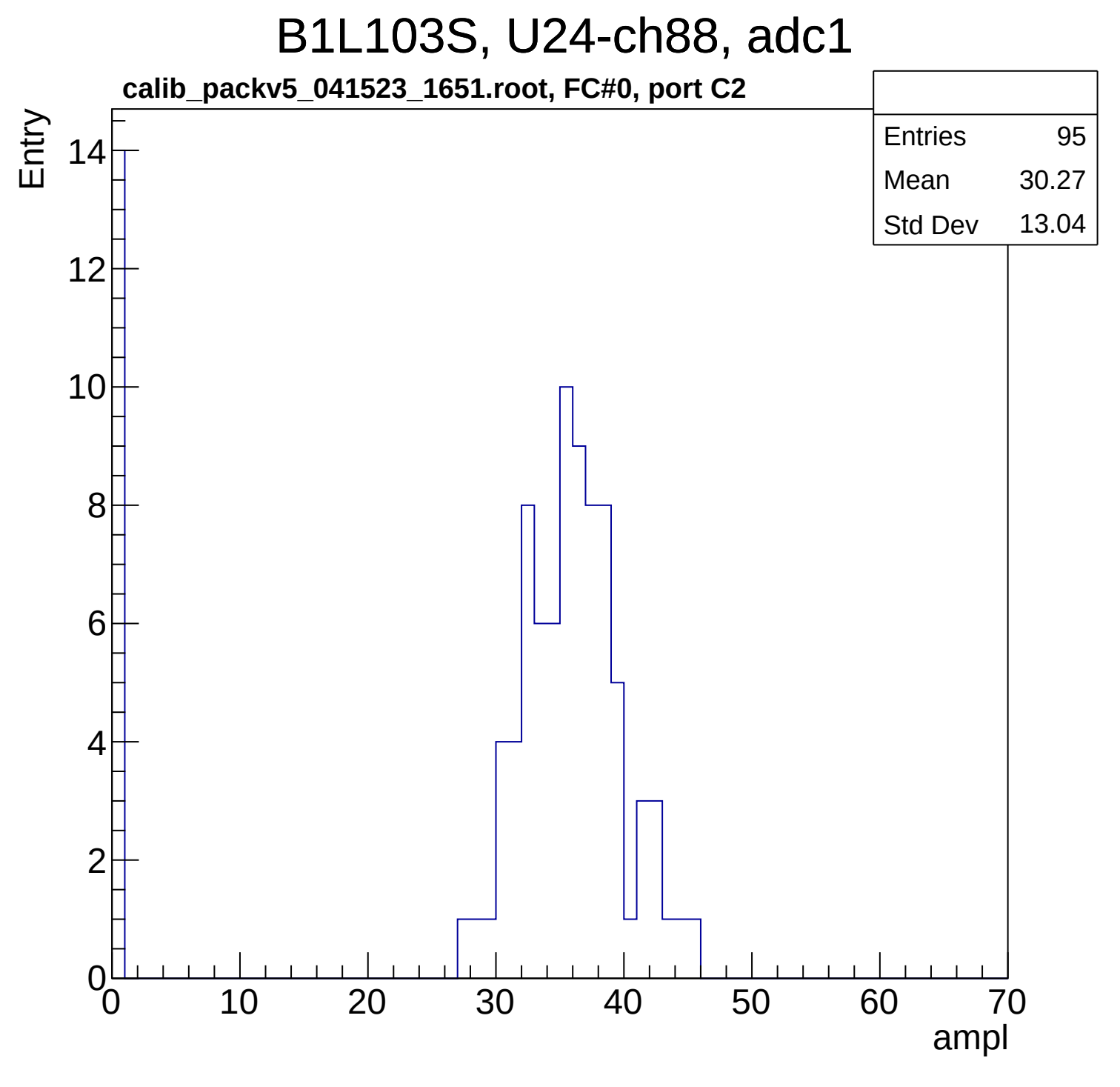
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U24-ch87, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch88, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 22.7
Std Dev 11.26
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L103S, U24-ch88, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 95
Mean 30.27
Std Dev 13.04
Entry
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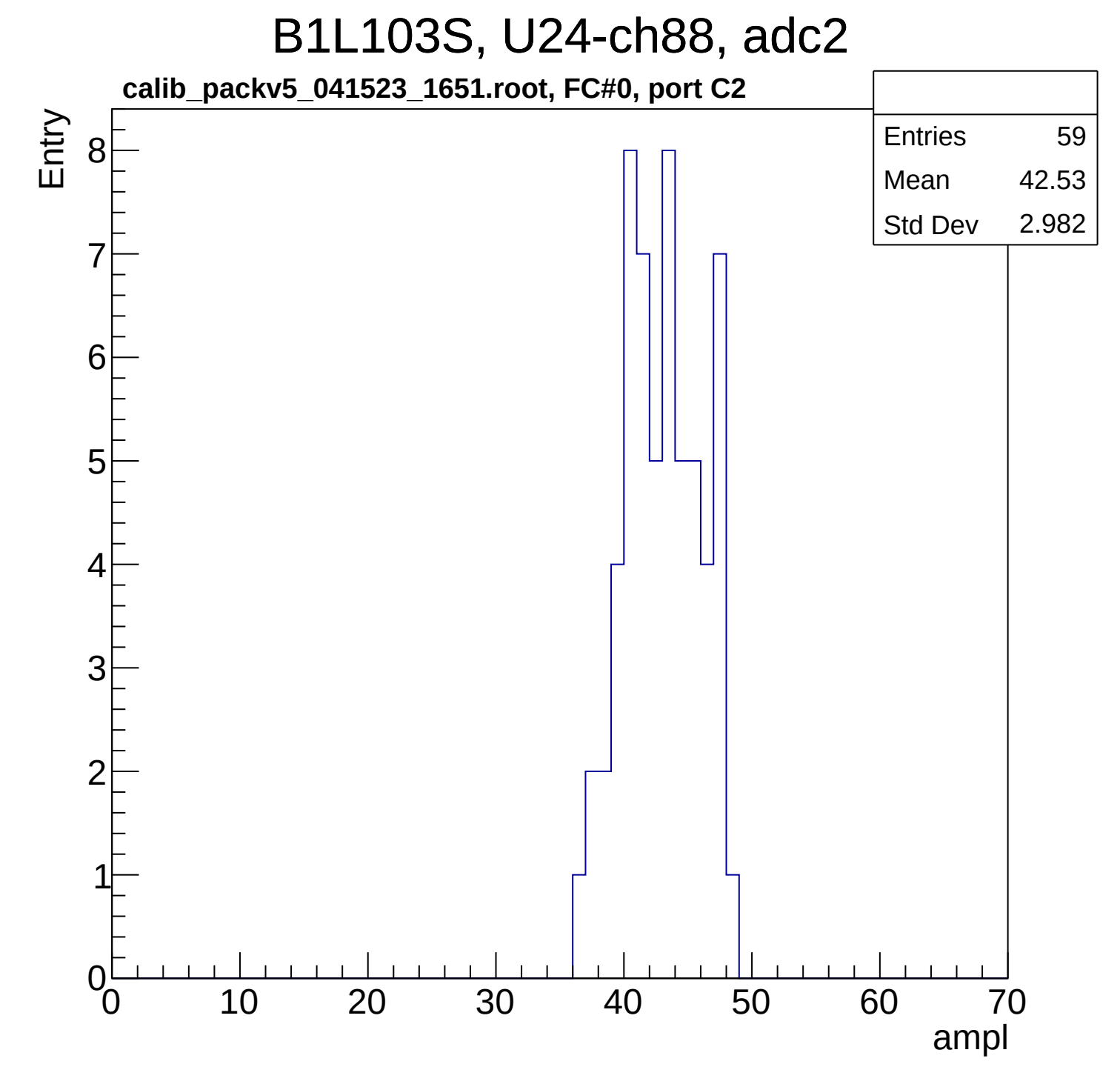
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch88, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 42.53
Std Dev 2.982
Entry
ampl
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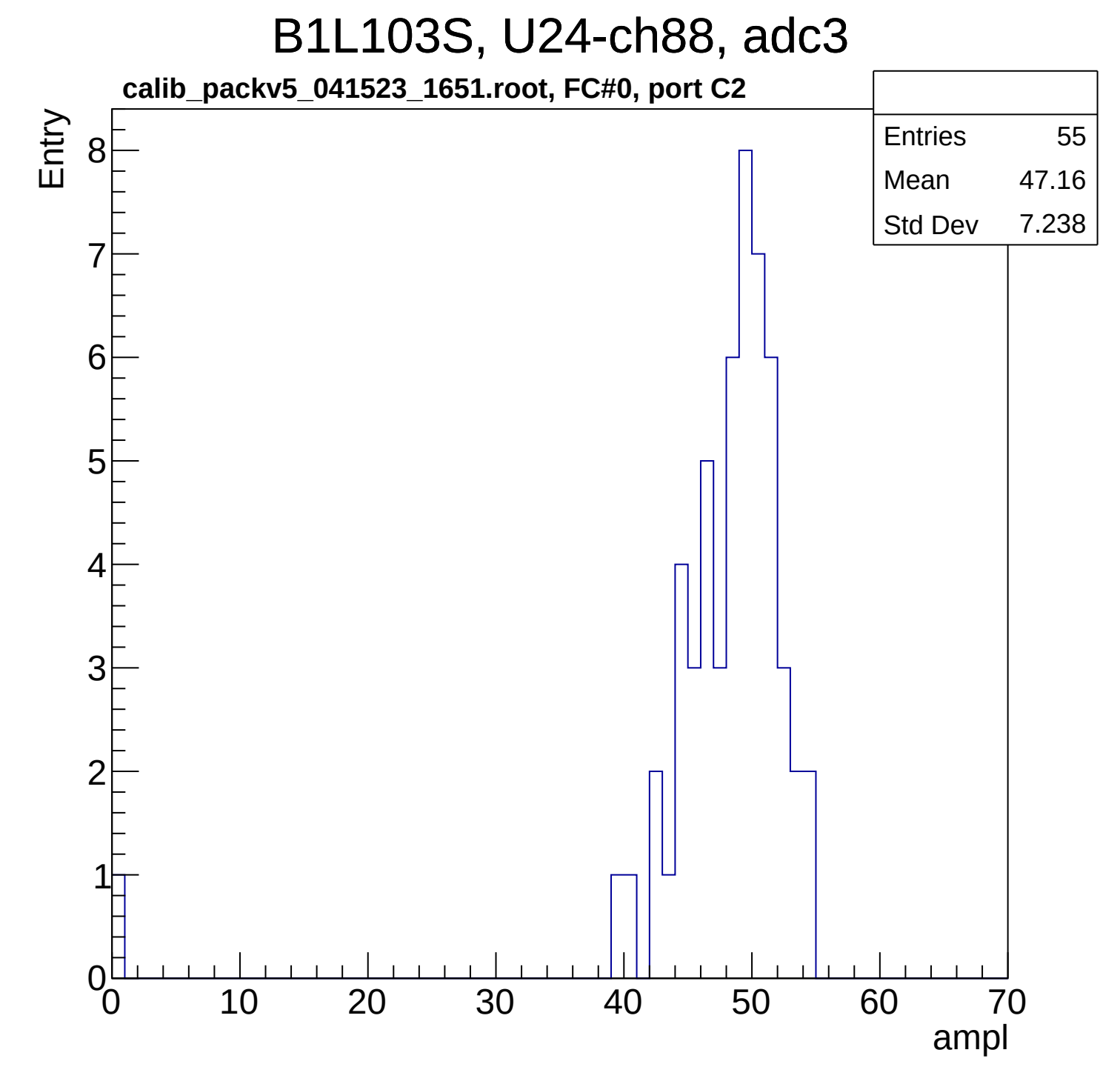
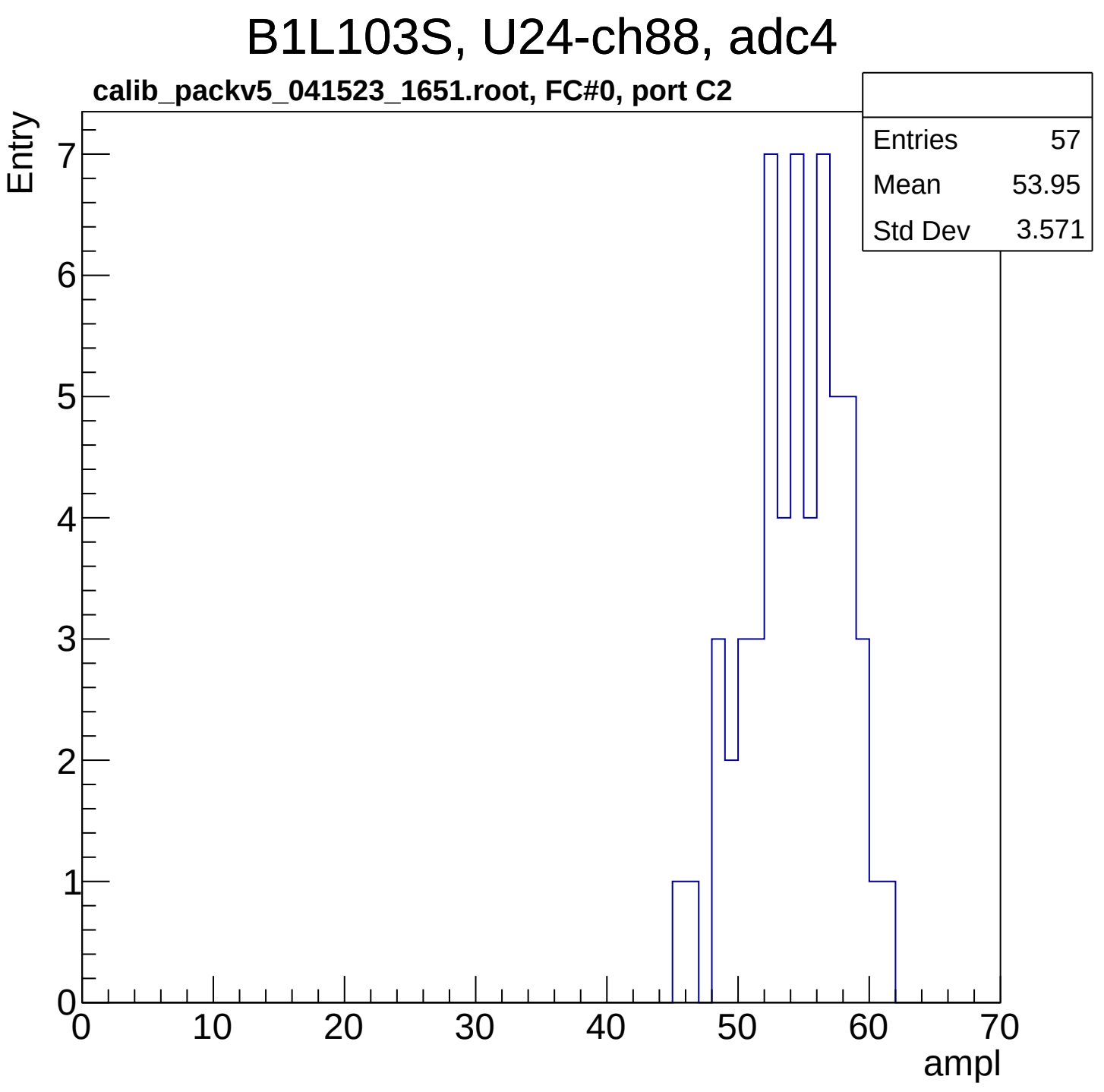
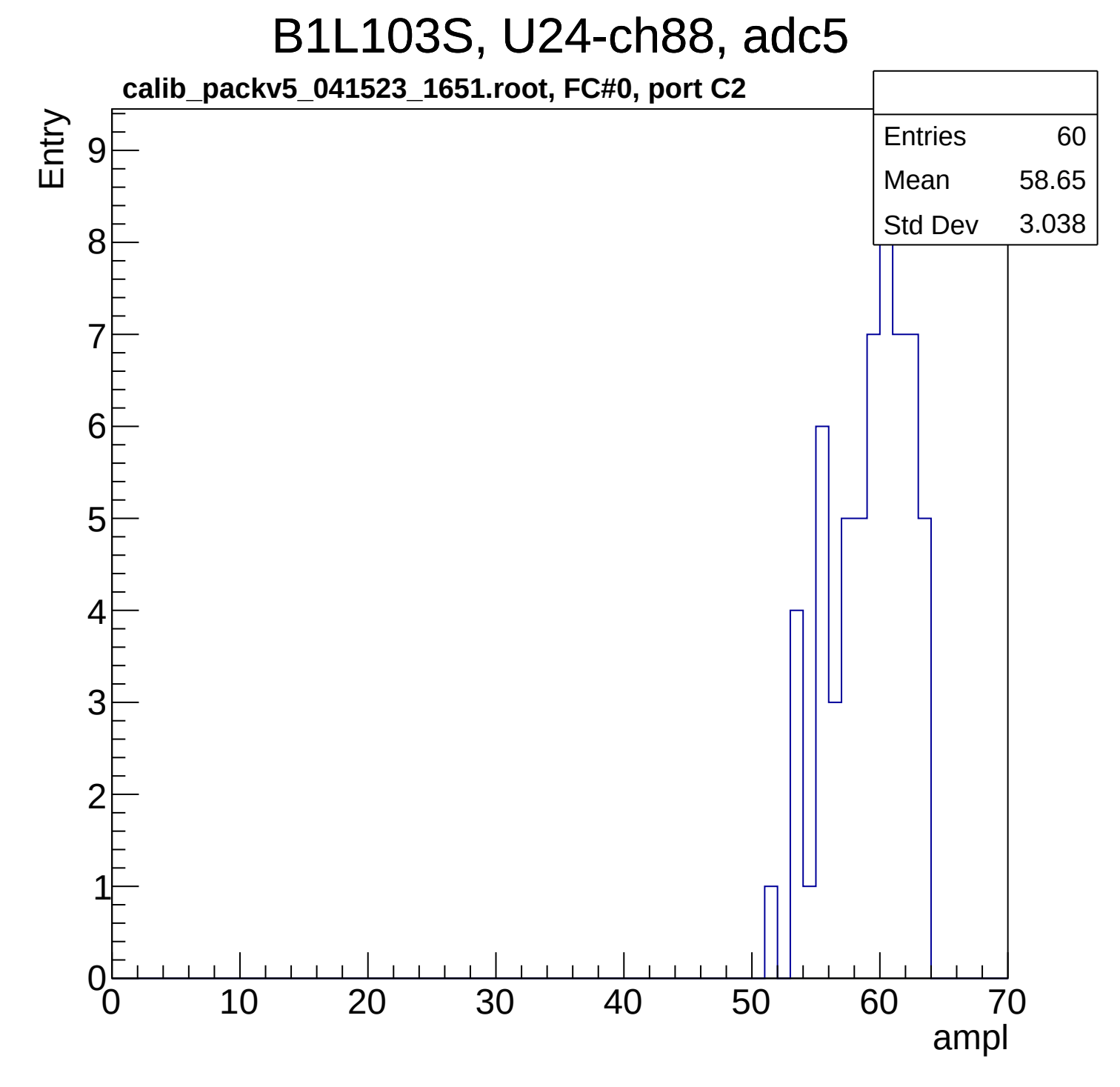
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U24-ch88, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 47.16
Std Dev 7.238
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U24-ch88, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 53.95
Std Dev 3.571
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U24-ch88, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 58.65
Std Dev 3.038
Entry
ampl
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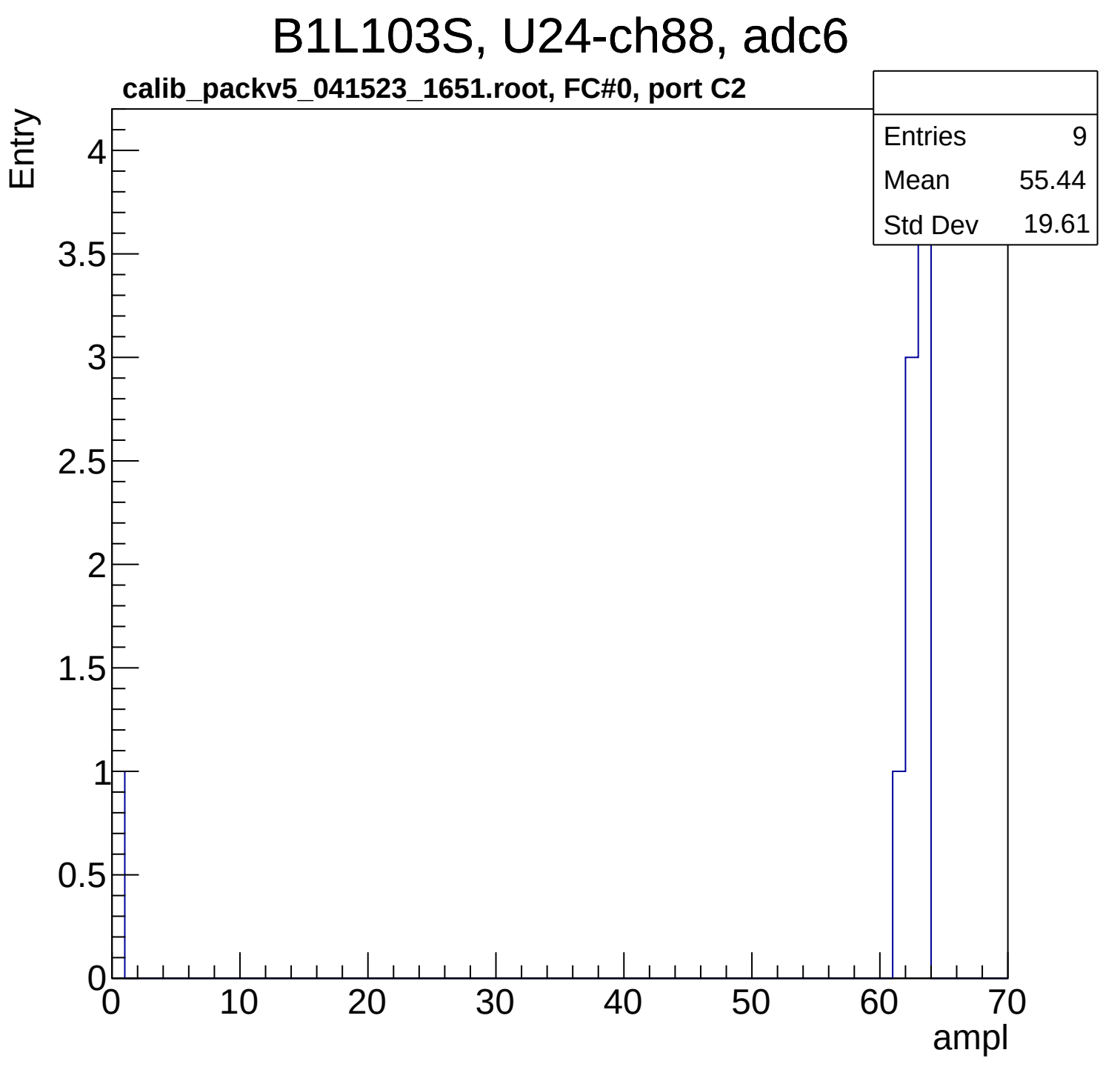
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U24-ch88, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 9
Mean 55.44
Std Dev 19.61
Entry
ampl
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0.5
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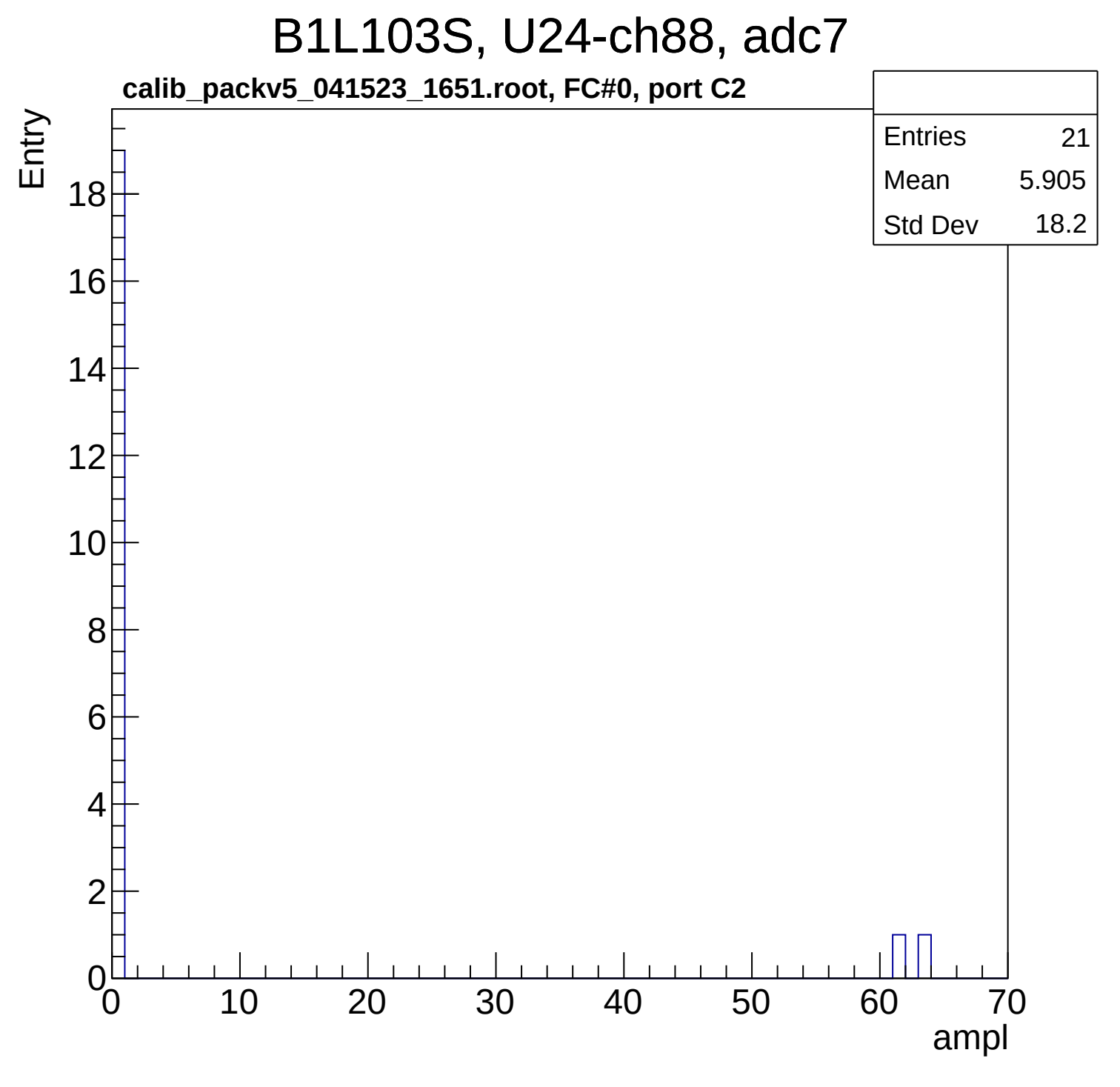
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U24-ch88, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 5.905
Std Dev 18.2
Entry
0
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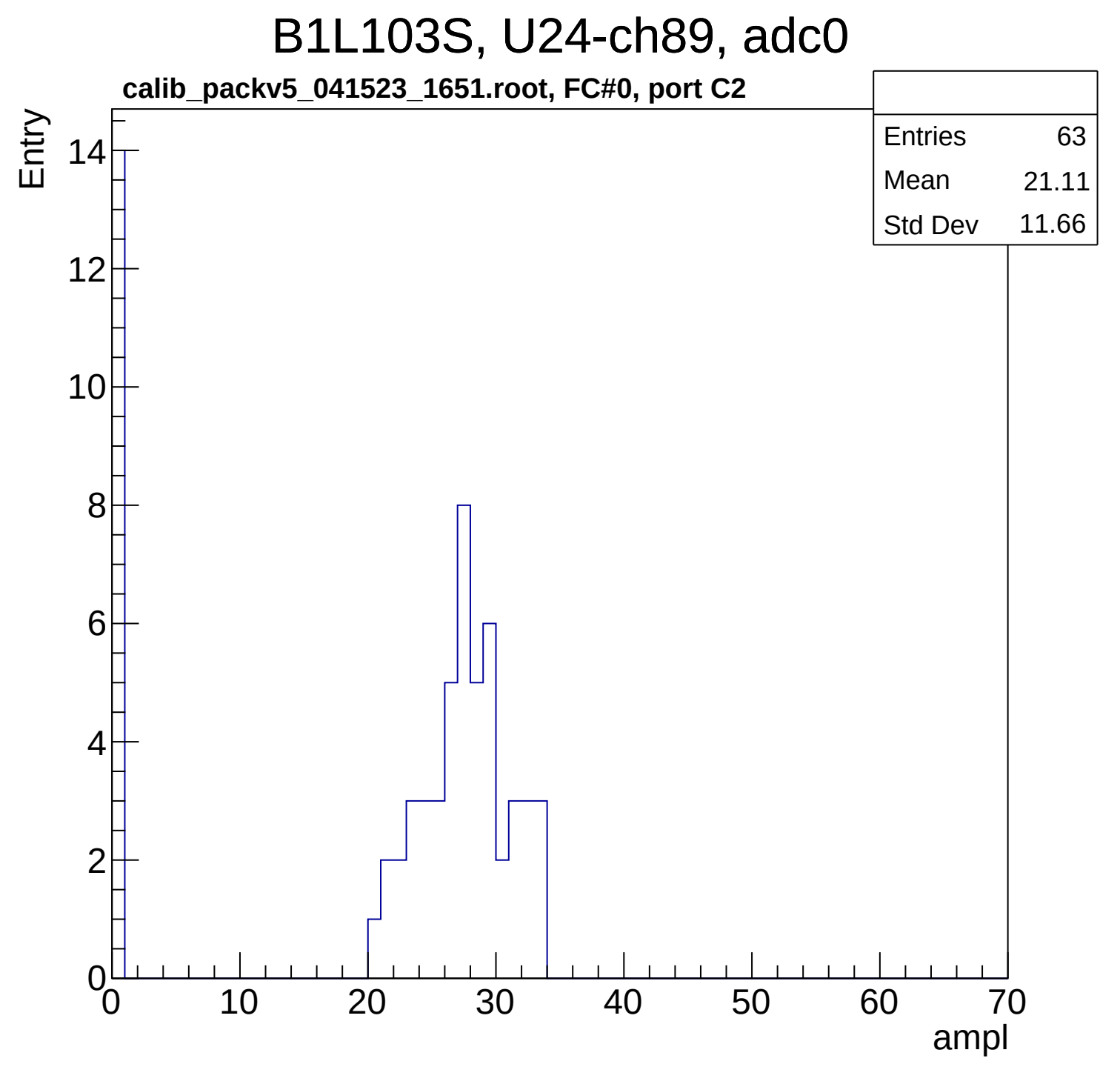
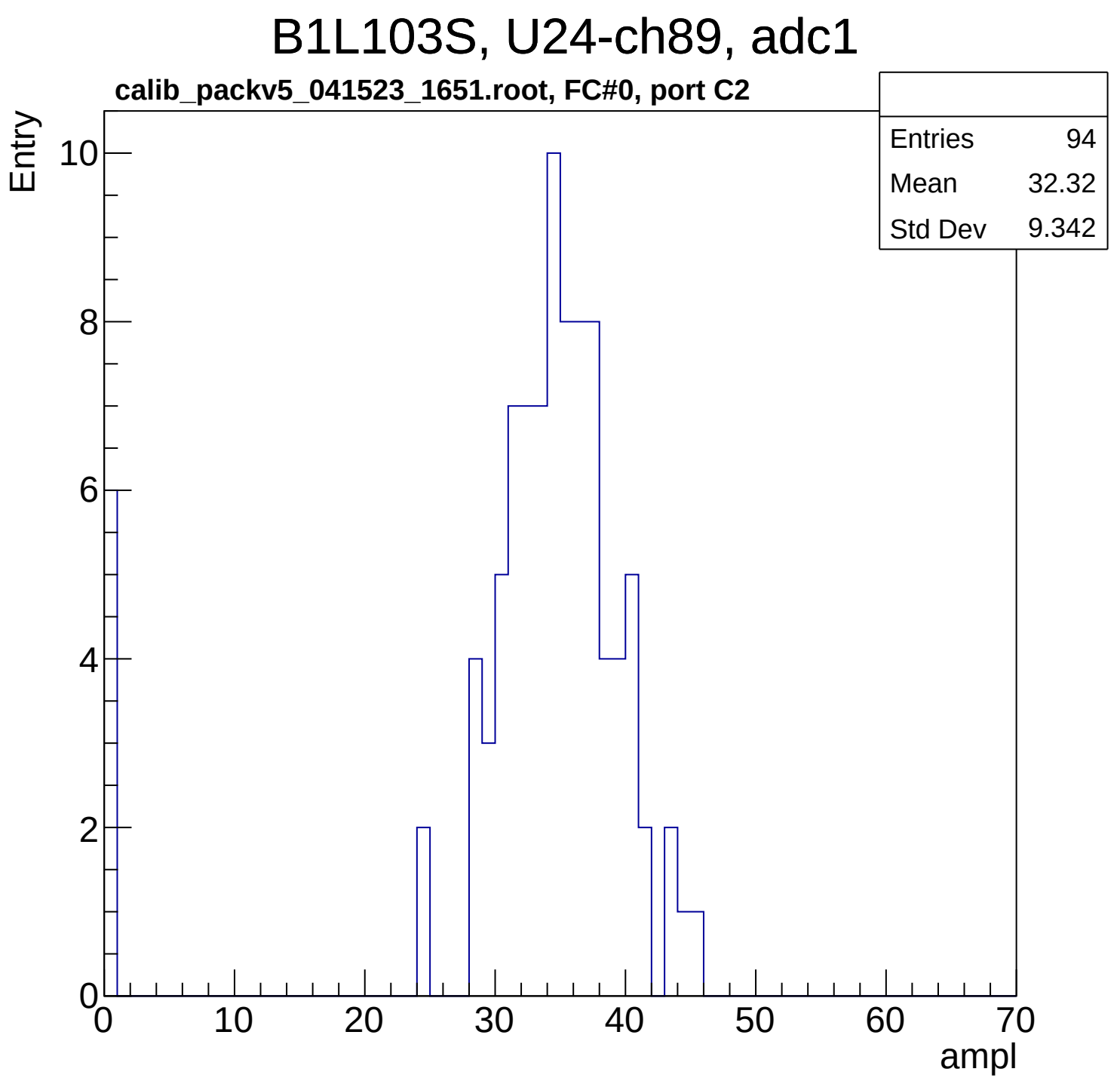
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch89, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 21.11
Std Dev 11.66
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch89, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 94
Mean 32.32
Std Dev 9.342
Entry
ampl
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2
4
6
8
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0
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60
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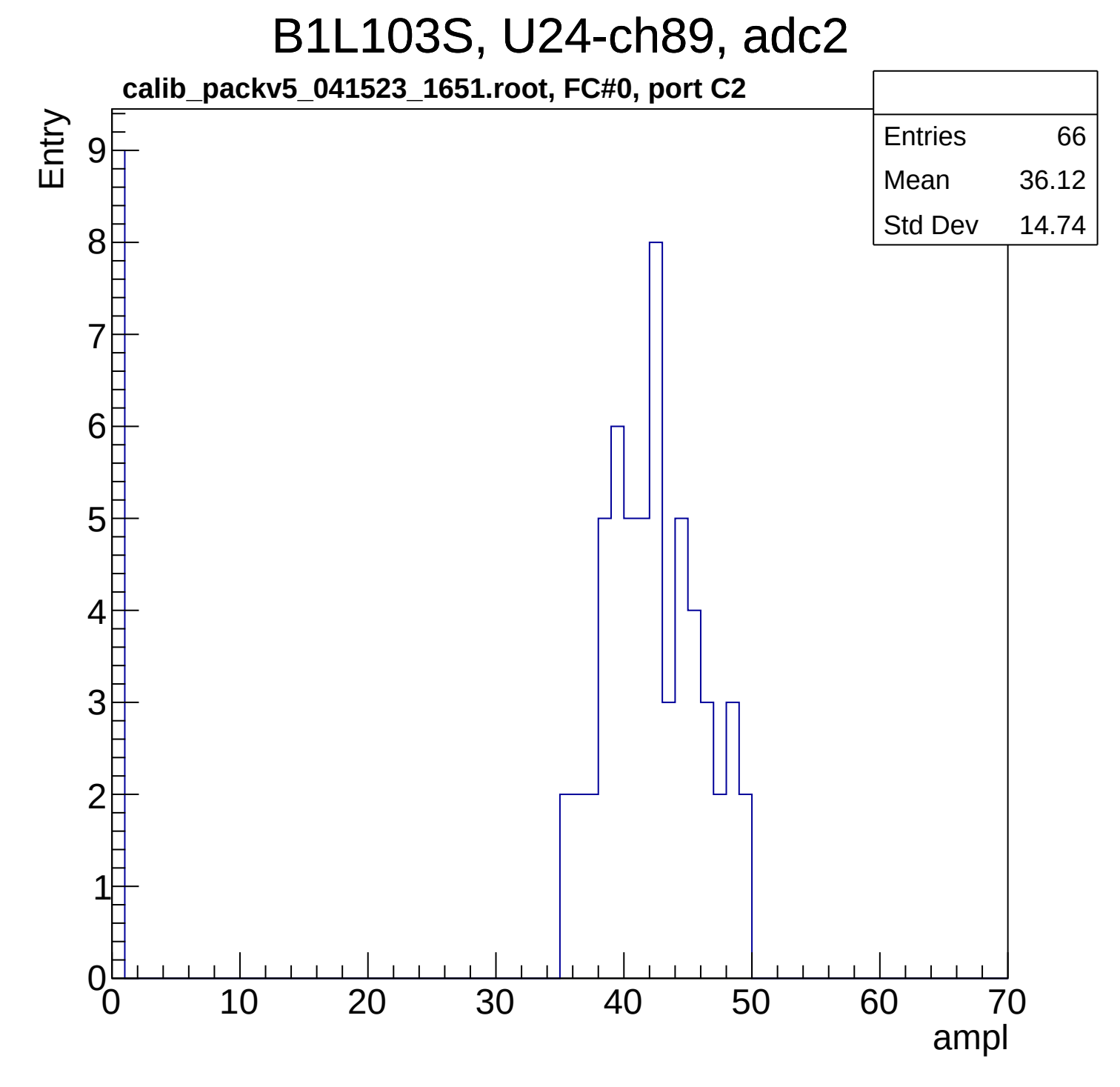
B1L103S, U24-ch89, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 36.12
Std Dev 14.74
Entry
ampl
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2
3
4
5
6
7
8
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0
10
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60
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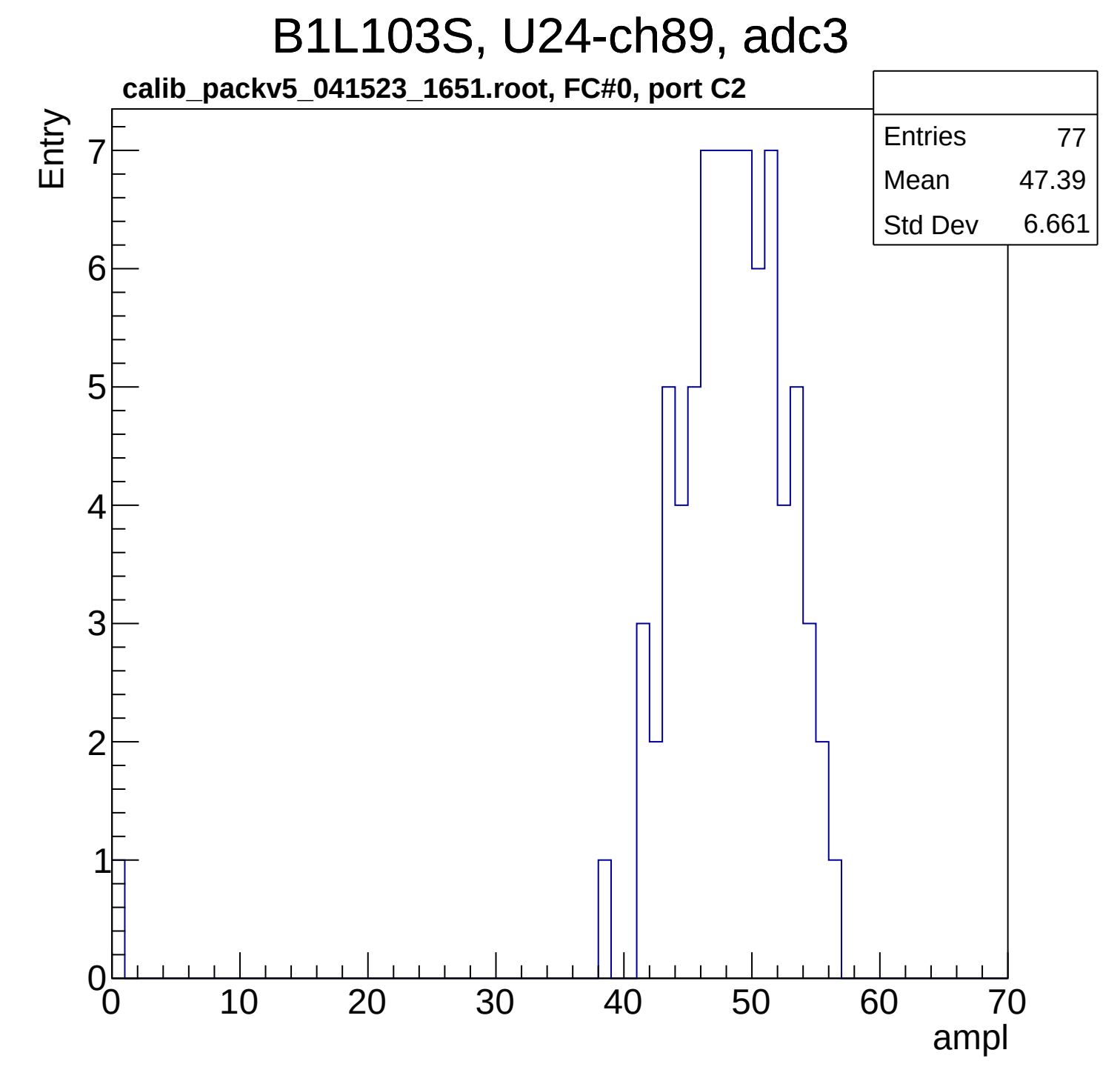
B1L103S, U24-ch89, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 47.39
Std Dev 6.661
Entry
ampl
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1
2
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4
5
6
7
0
10
20
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40
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60
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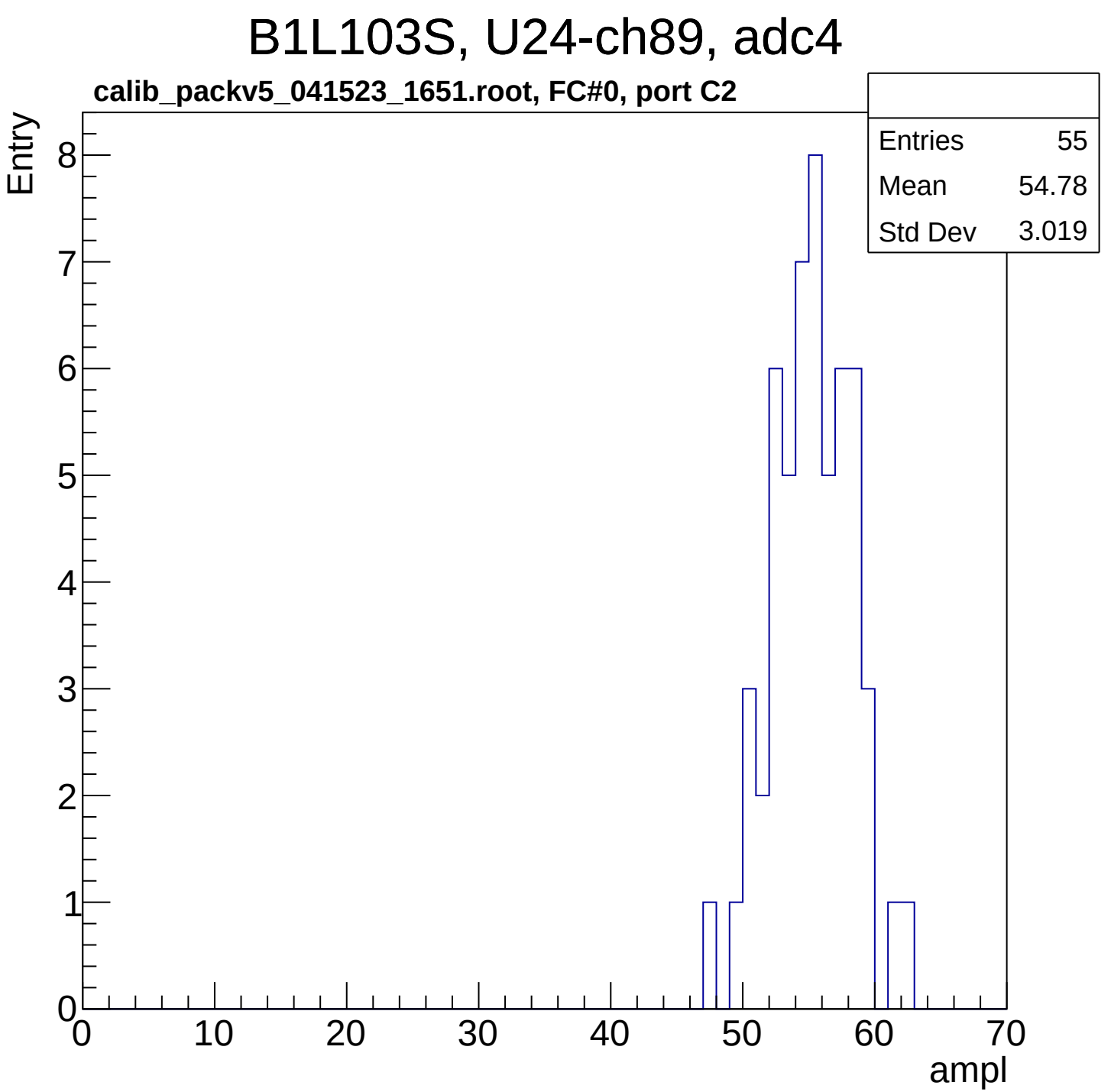
B1L103S, U24-ch89, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 54.78
Std Dev 3.019
Entry
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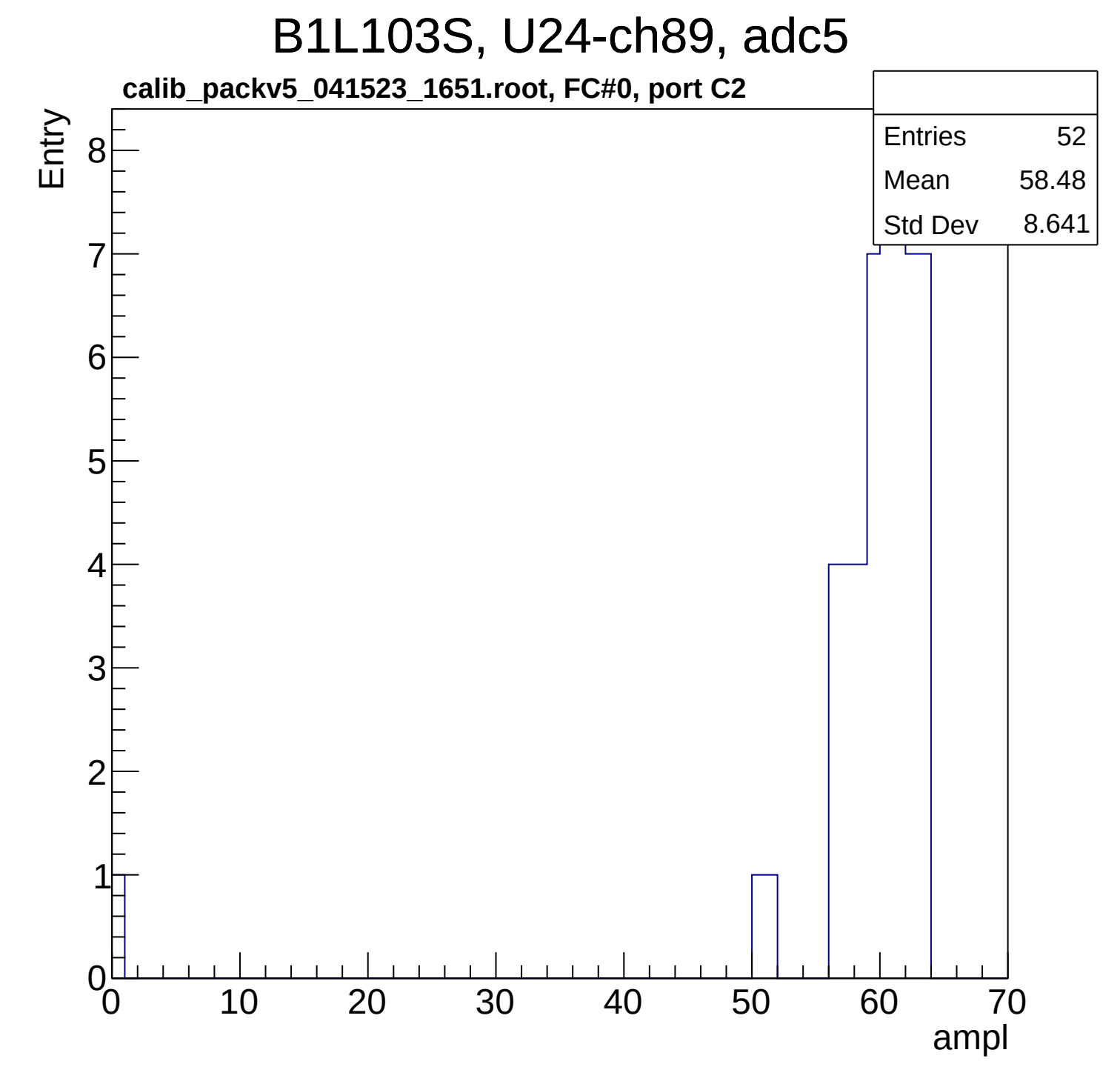
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch89, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 58.48
Std Dev 8.641
Entry
ampl
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1
2
3
4
5
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7
8
0
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40
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60
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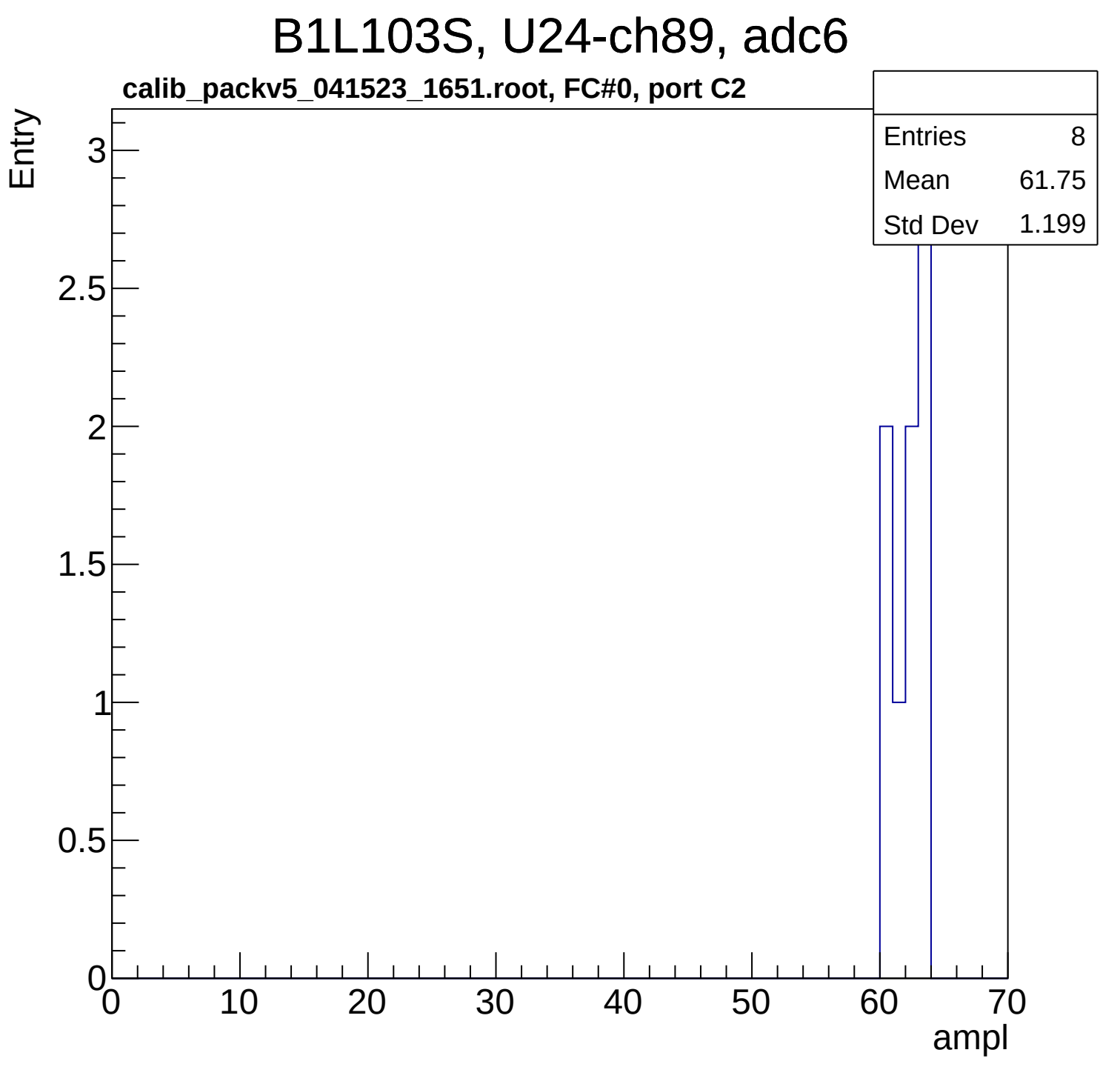
B1L103S, U24-ch89, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 61.75
Std Dev 1.199
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
10
20
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40
50
60
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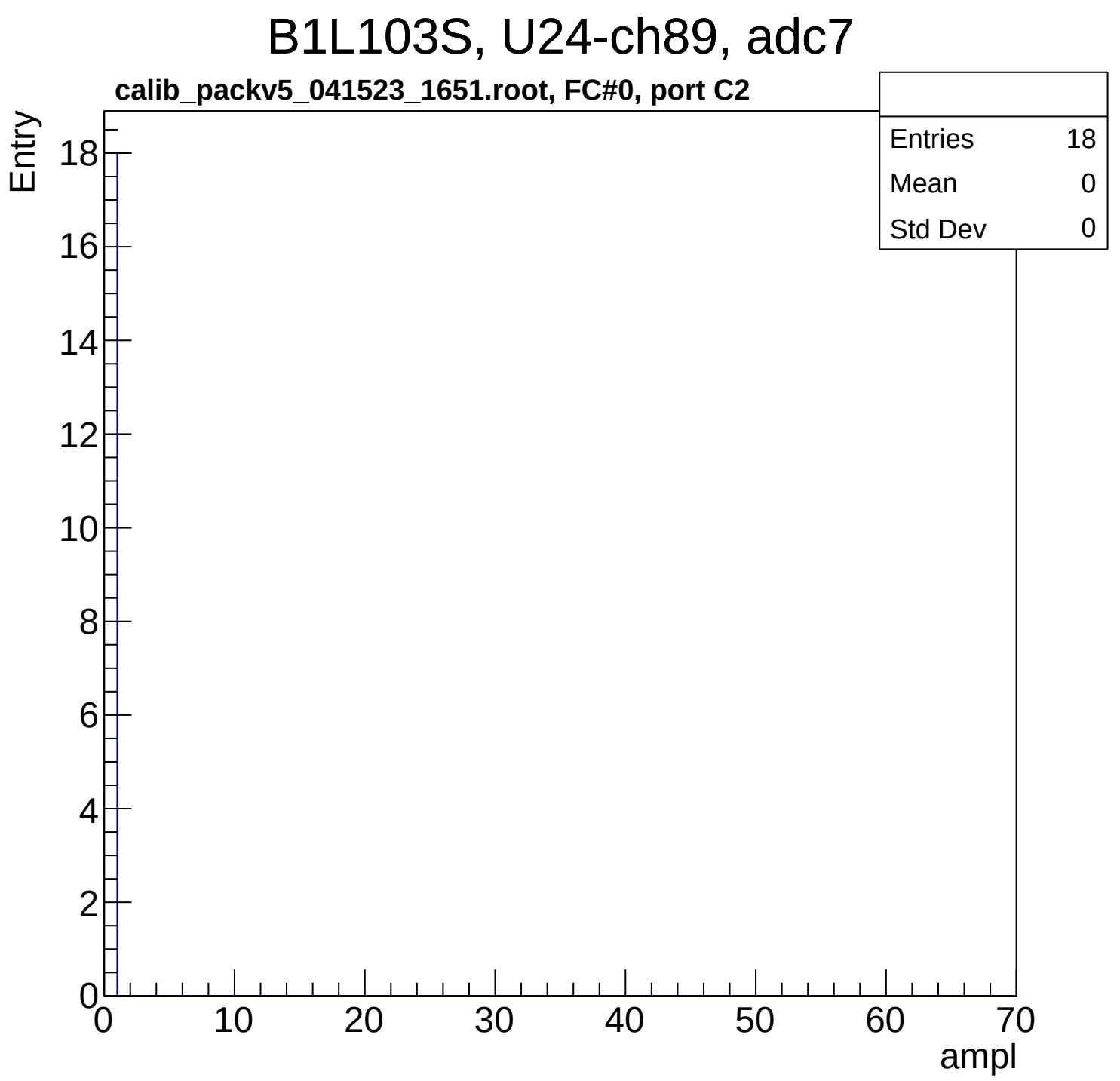
B1L103S, U24-ch89, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
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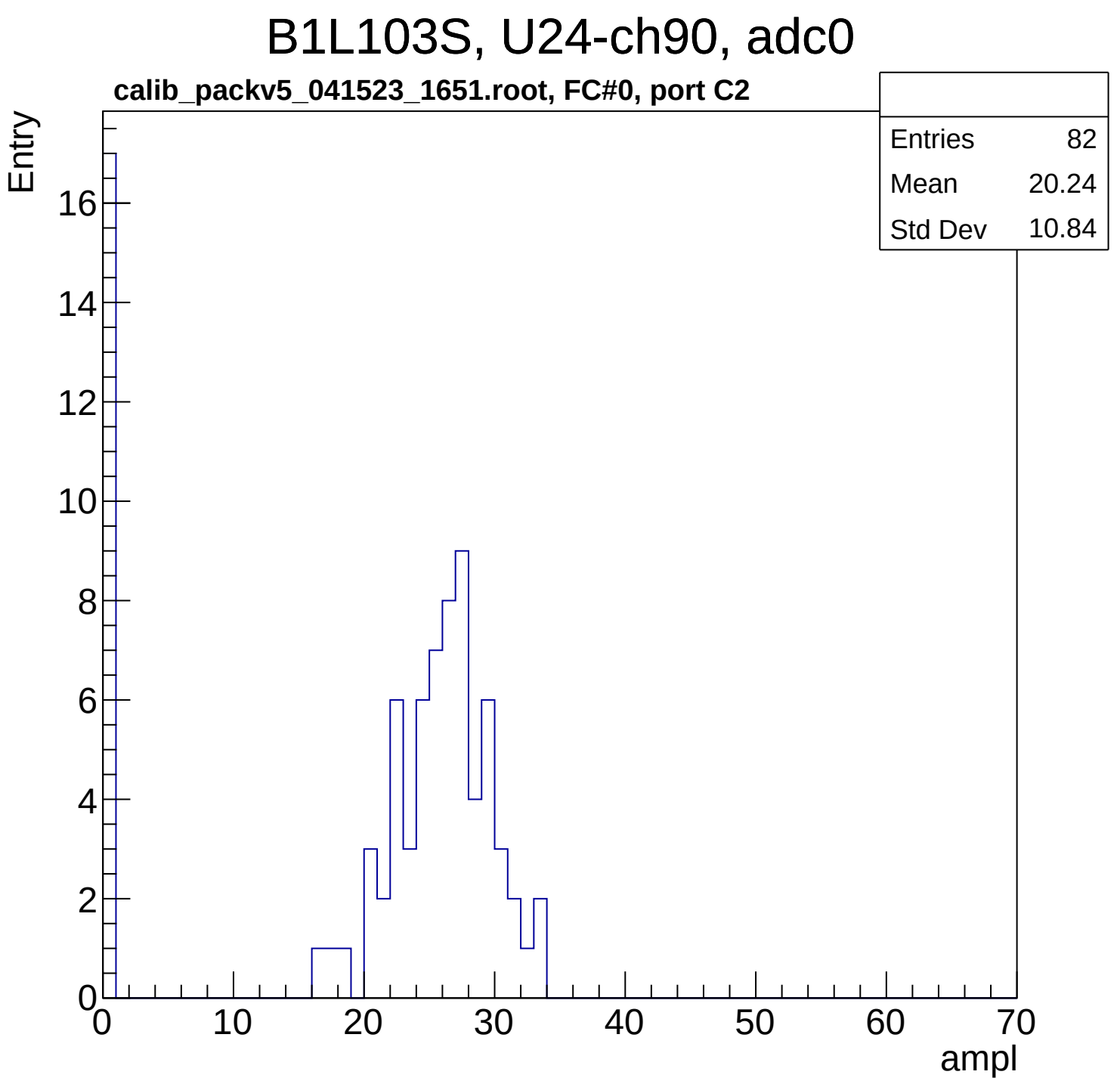
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch90, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 20.24
Std Dev 10.84
Entry
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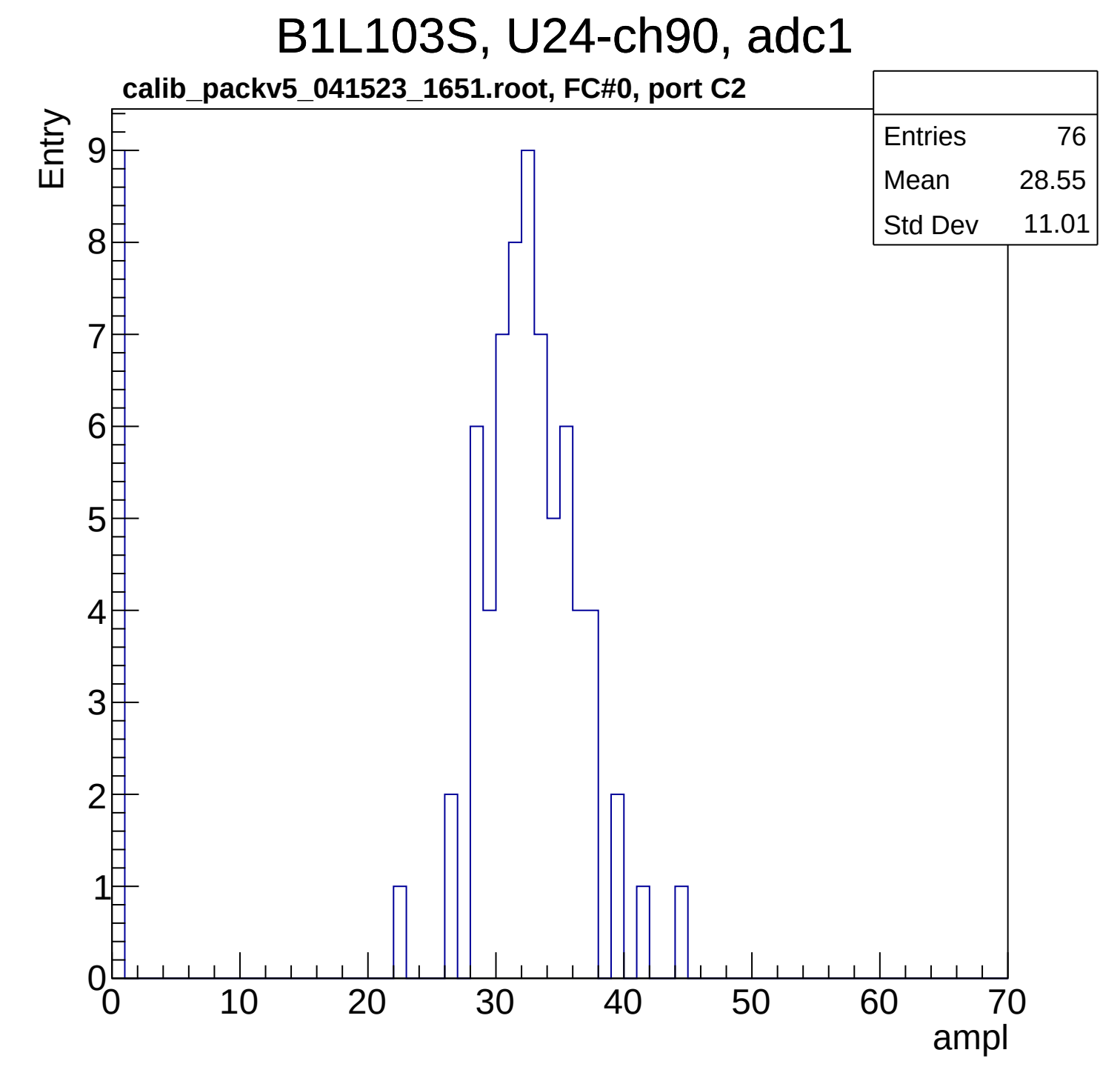
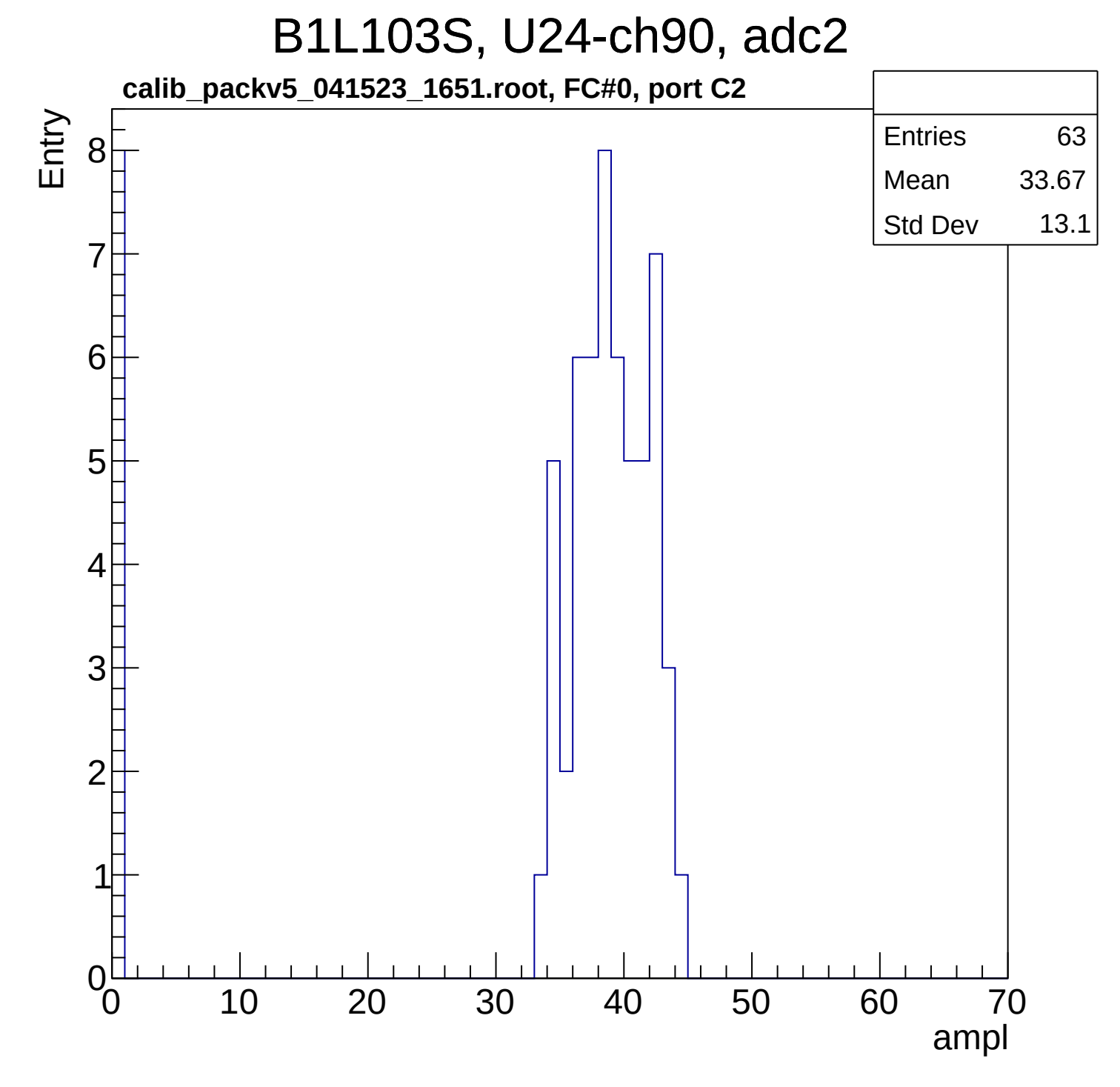
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch90, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 28.55
Std Dev 11.01
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U24-ch90, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 33.67
Std Dev 13.1
Entry
ampl
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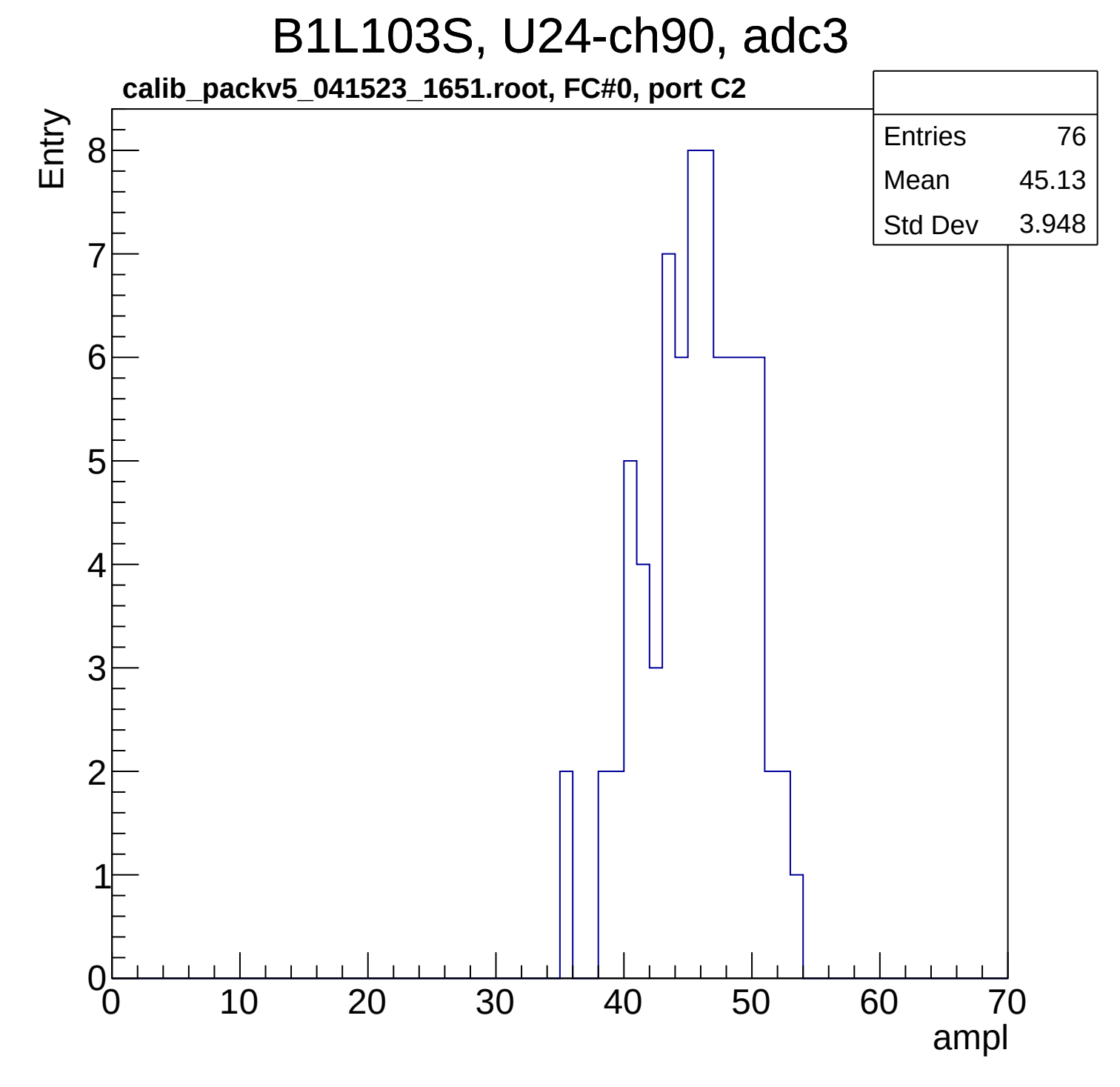
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U24-ch90, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 45.13
Std Dev 3.948
Entry
ampl
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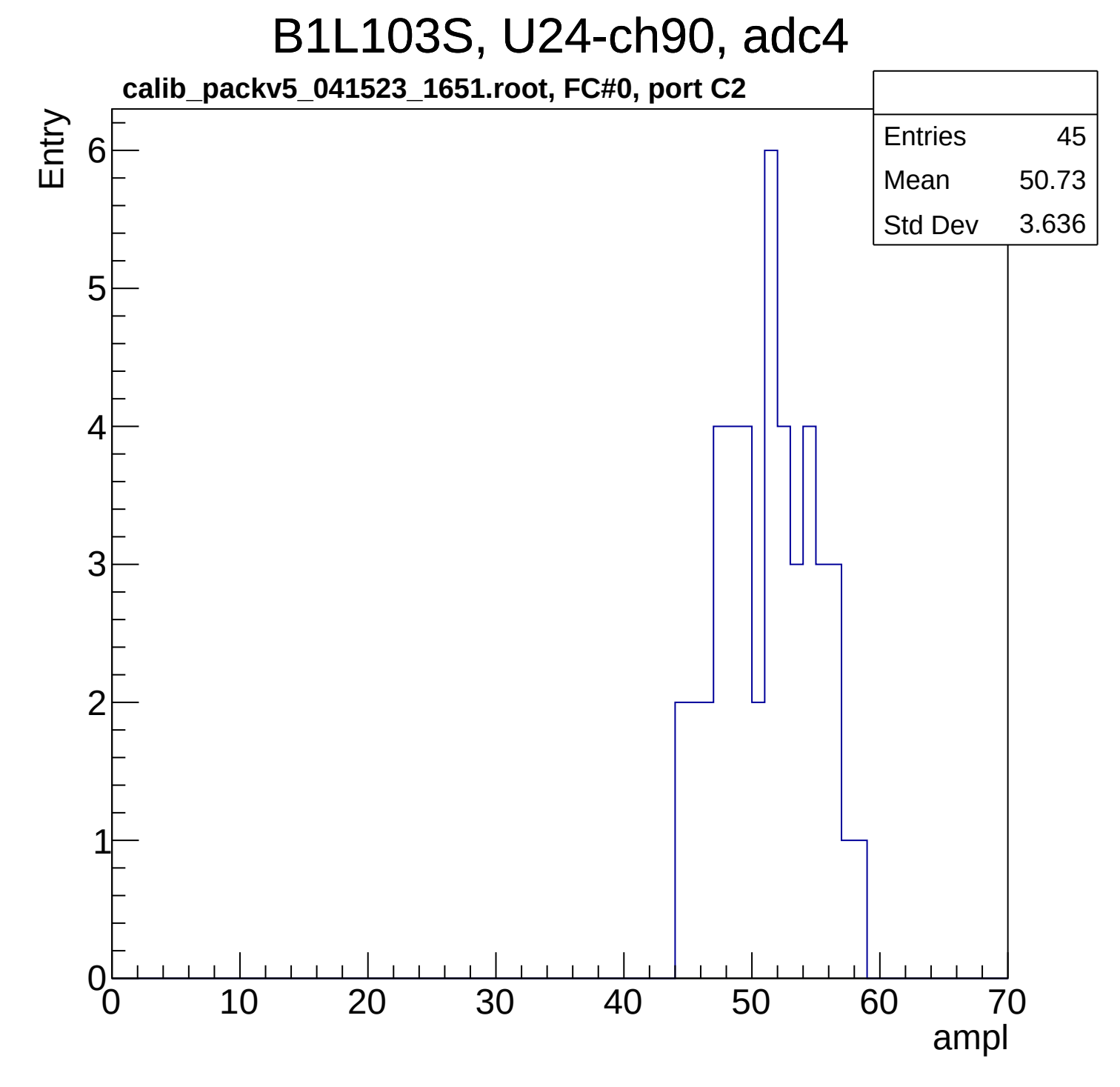
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U24-ch90, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 50.73
Std Dev 3.636
Entry
ampl
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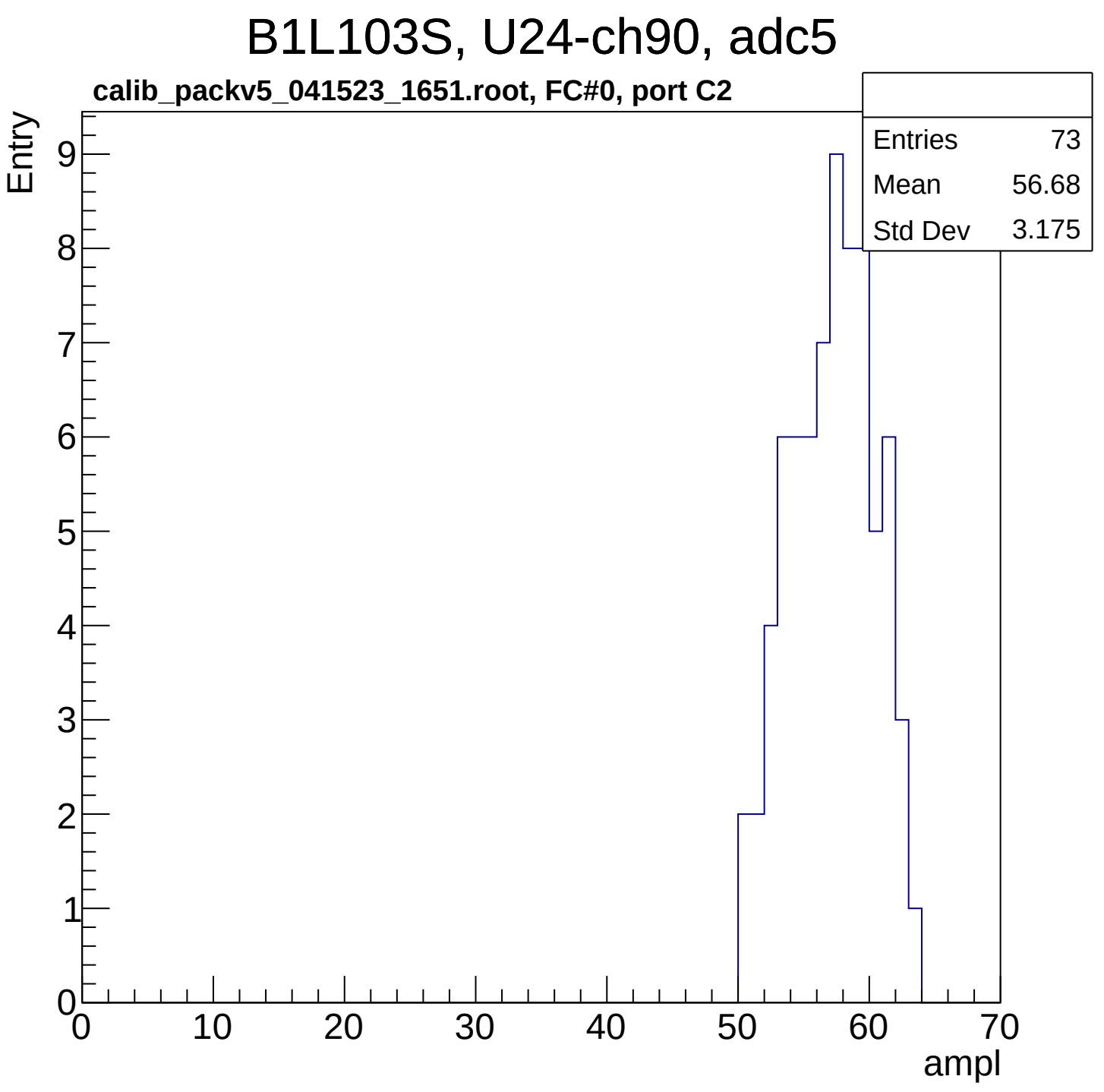
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U24-ch90, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 56.68
Std Dev 3.175
Entry
ampl
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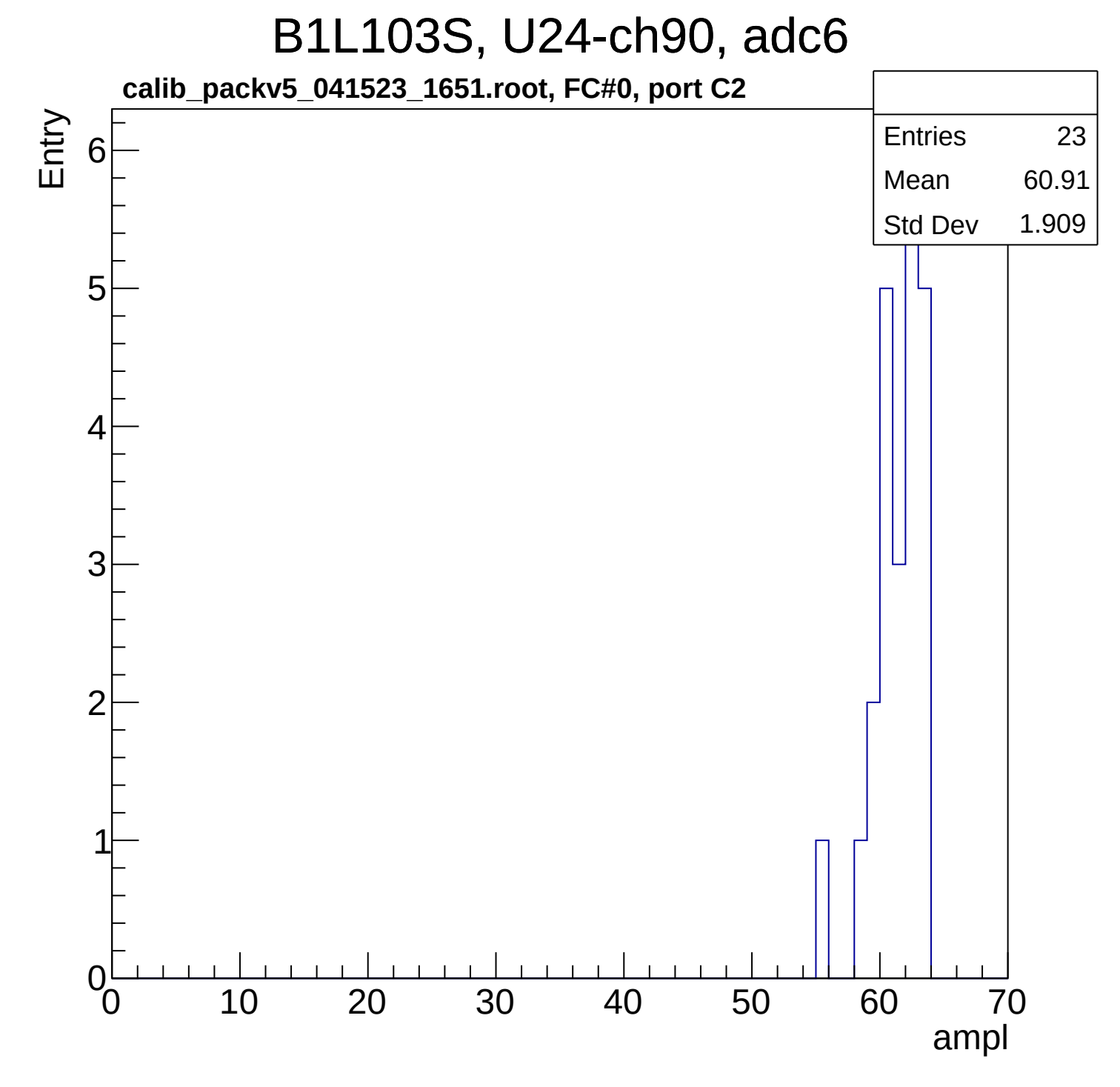
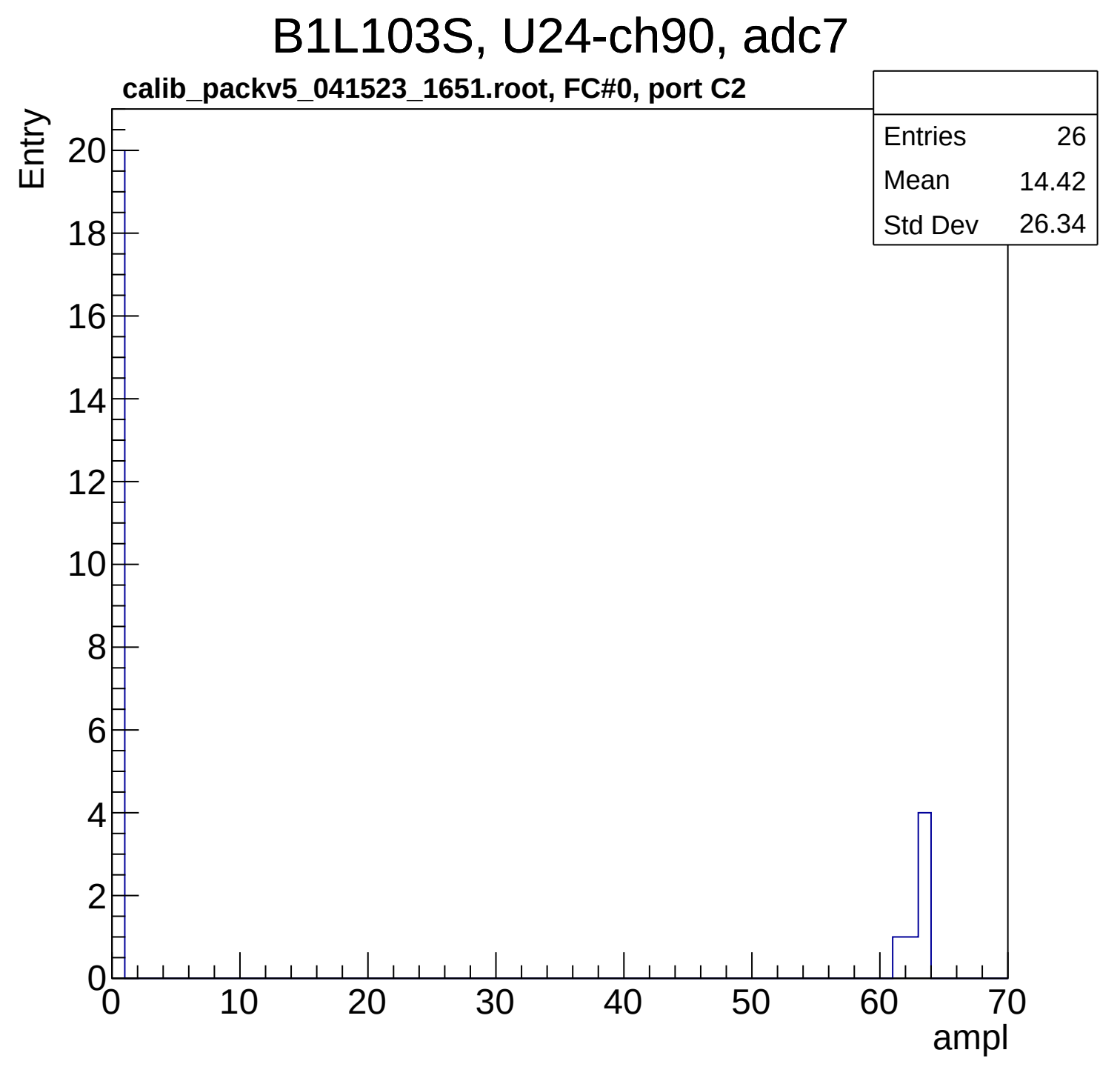
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U24-ch90, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 23
Mean 60.91
Std Dev 1.909
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U24-ch90, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 26
Mean 14.42
Std Dev 26.34
Entry
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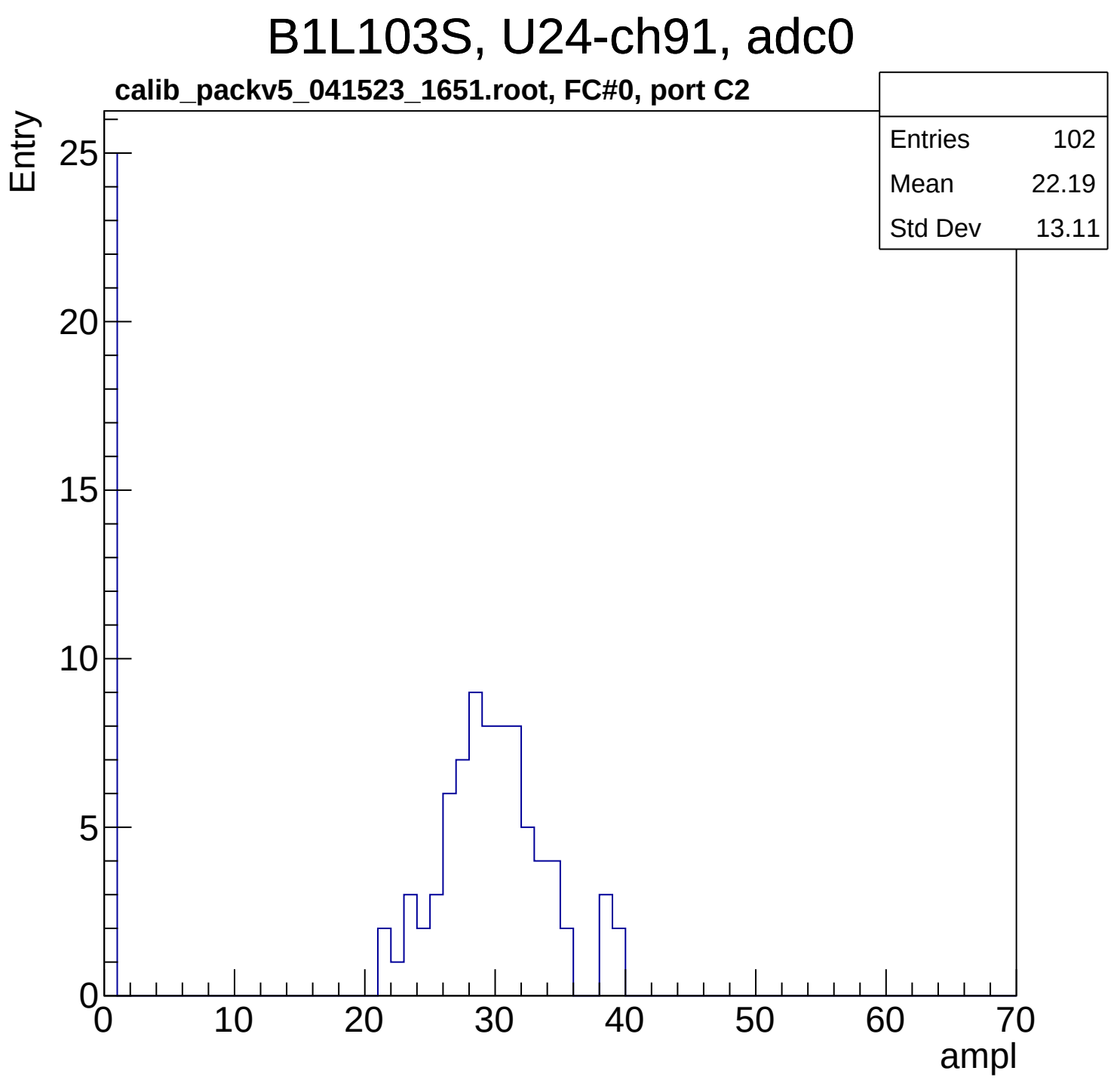
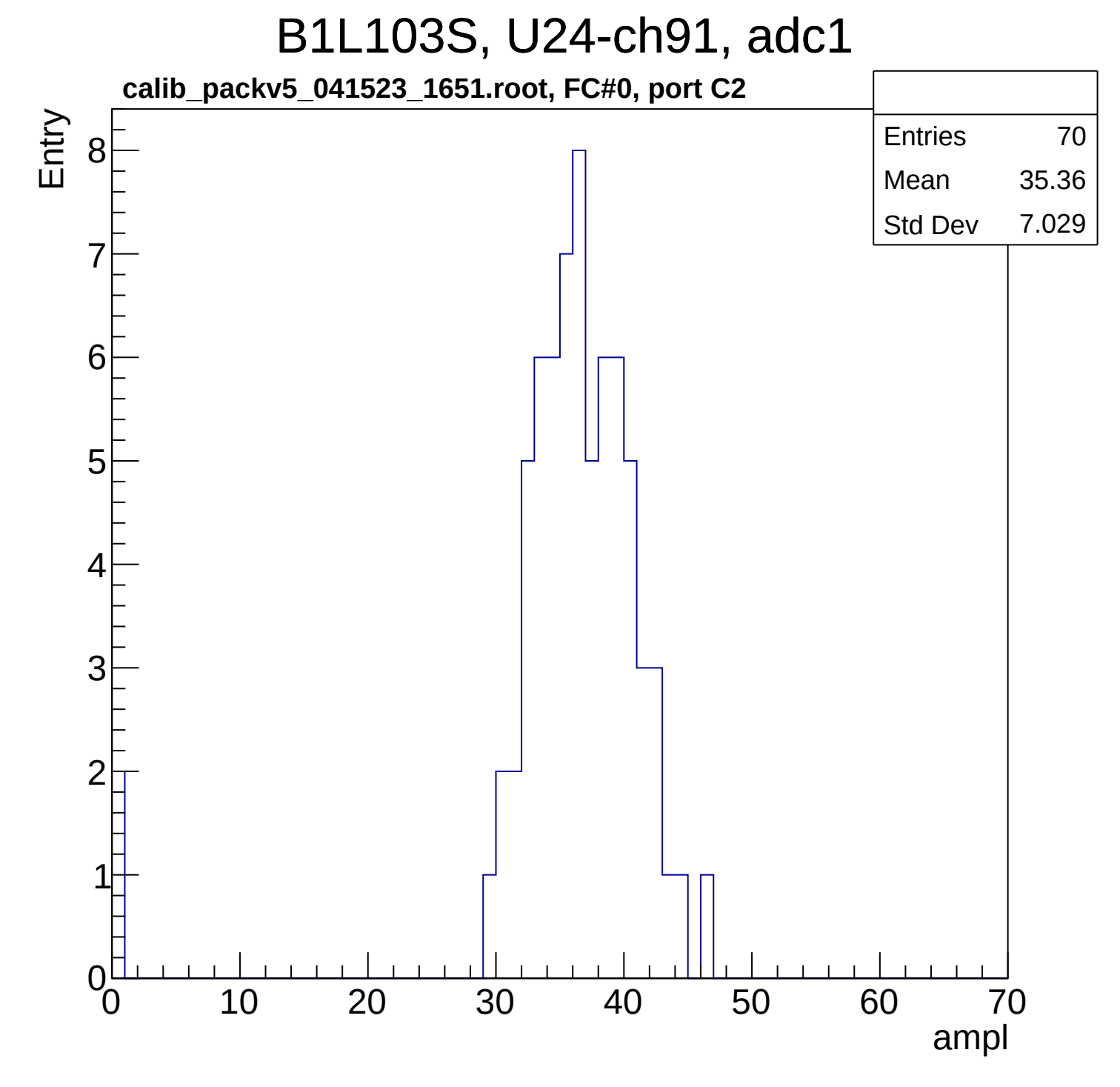
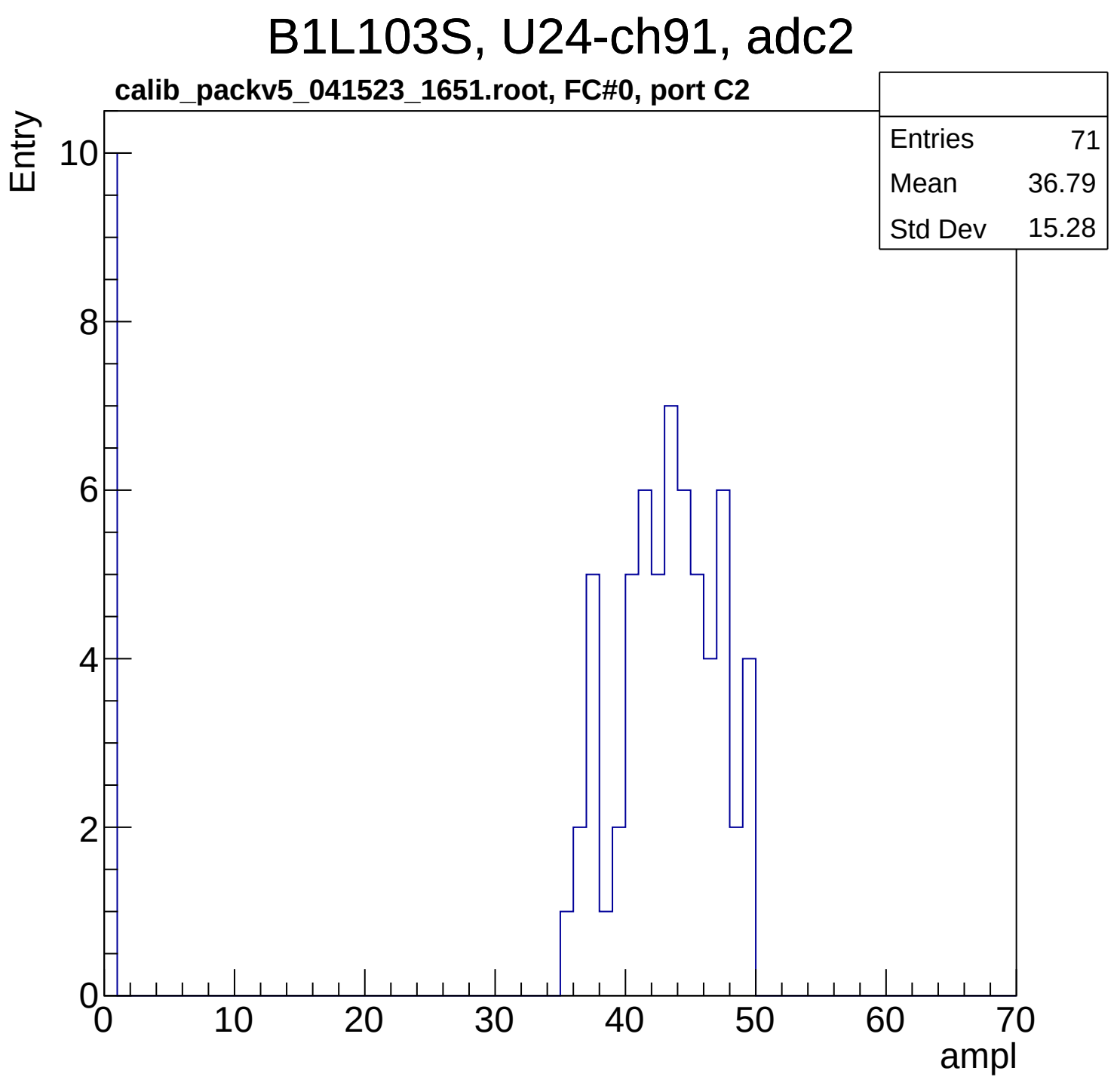
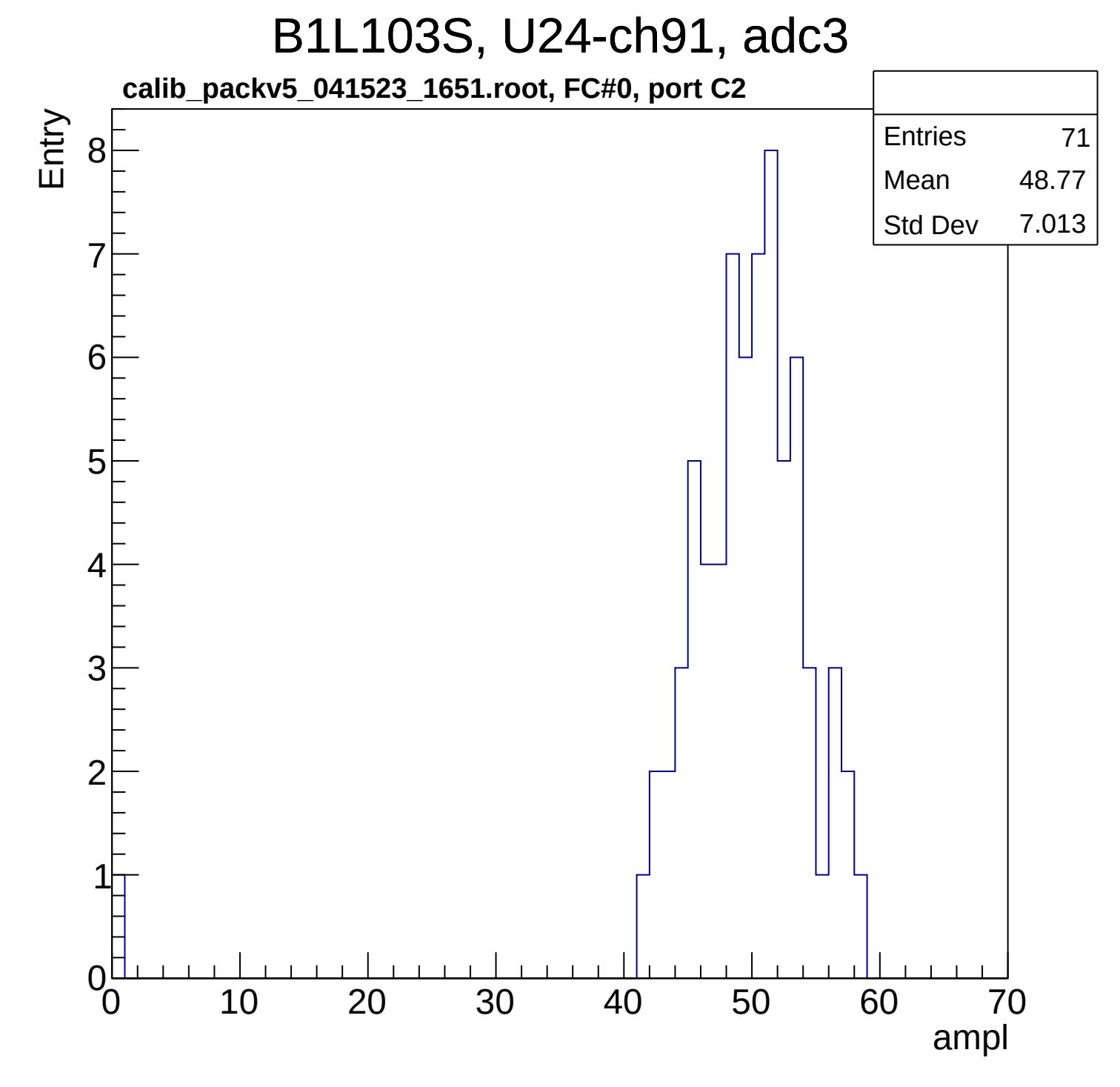
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch91, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 102
Mean 22.19
Std Dev 13.11
Entry
0
5
10
15
20
25
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch91, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 35.36
Std Dev 7.029
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U24-ch91, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 36.79
Std Dev 15.28
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch91, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 48.77
Std Dev 7.013
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
30
40
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60
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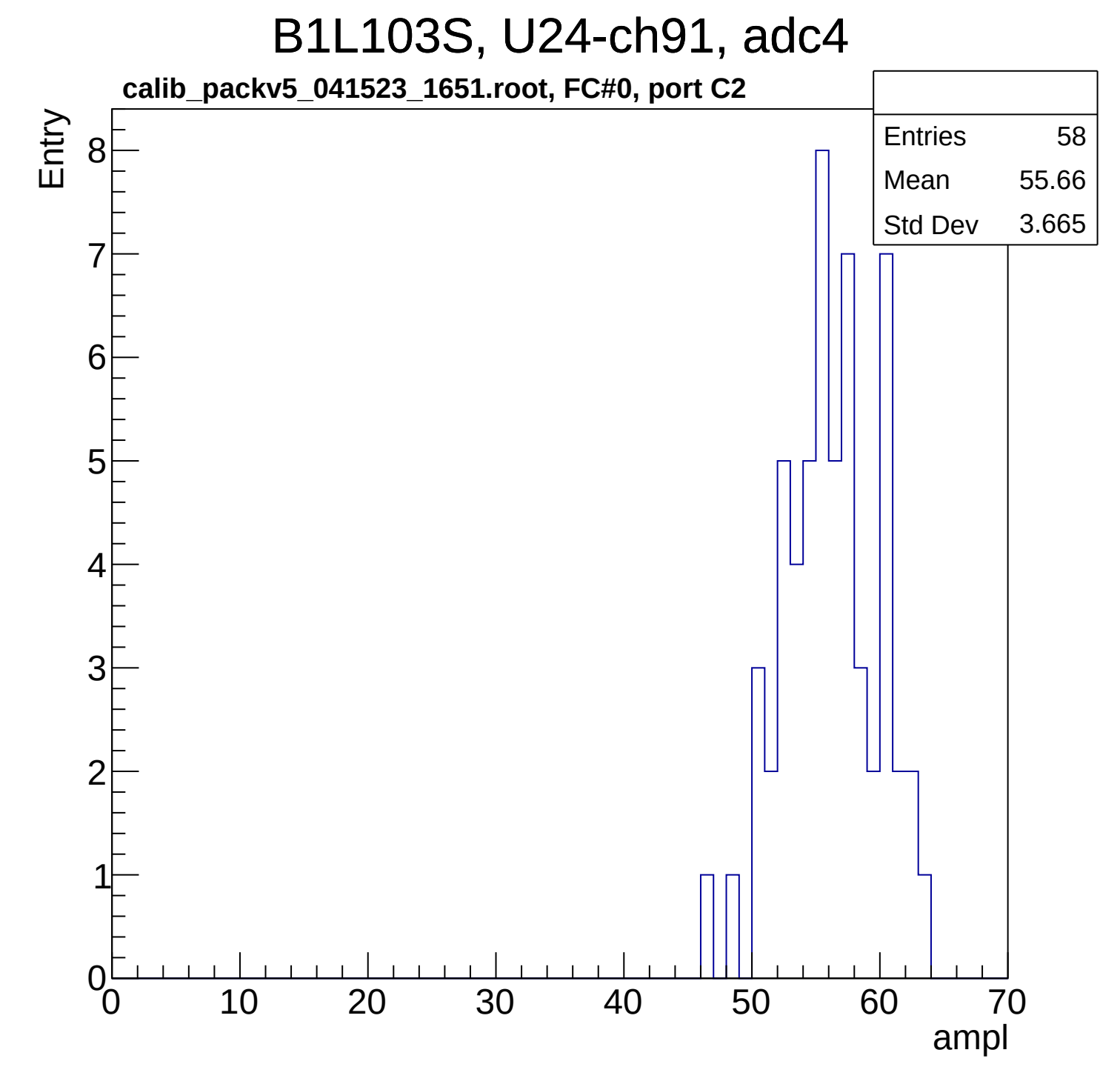
B1L103S, U24-ch91, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 55.66
Std Dev 3.665
Entry
ampl
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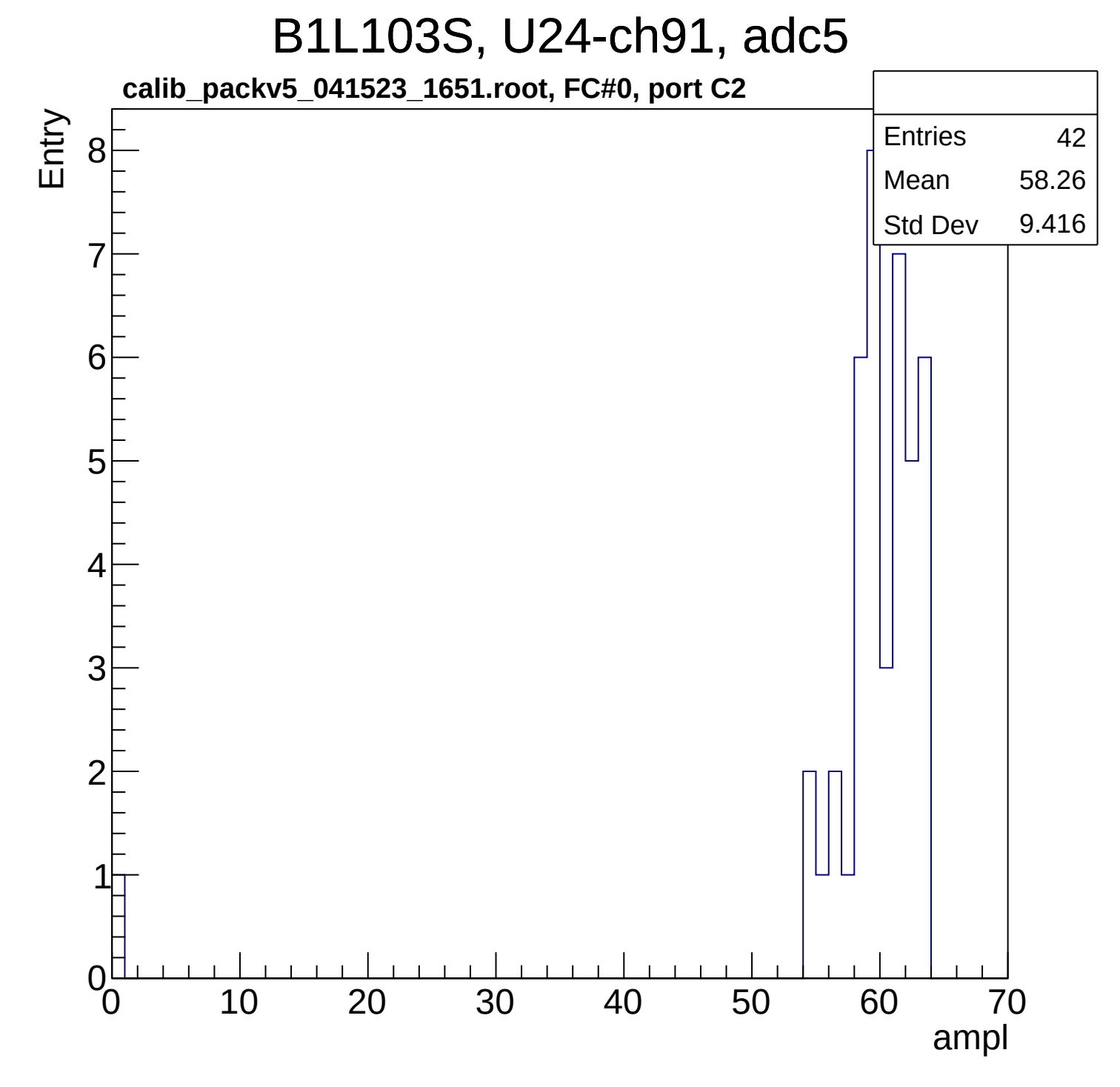
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U24-ch91, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 42
Mean 58.26
Std Dev 9.416
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
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40
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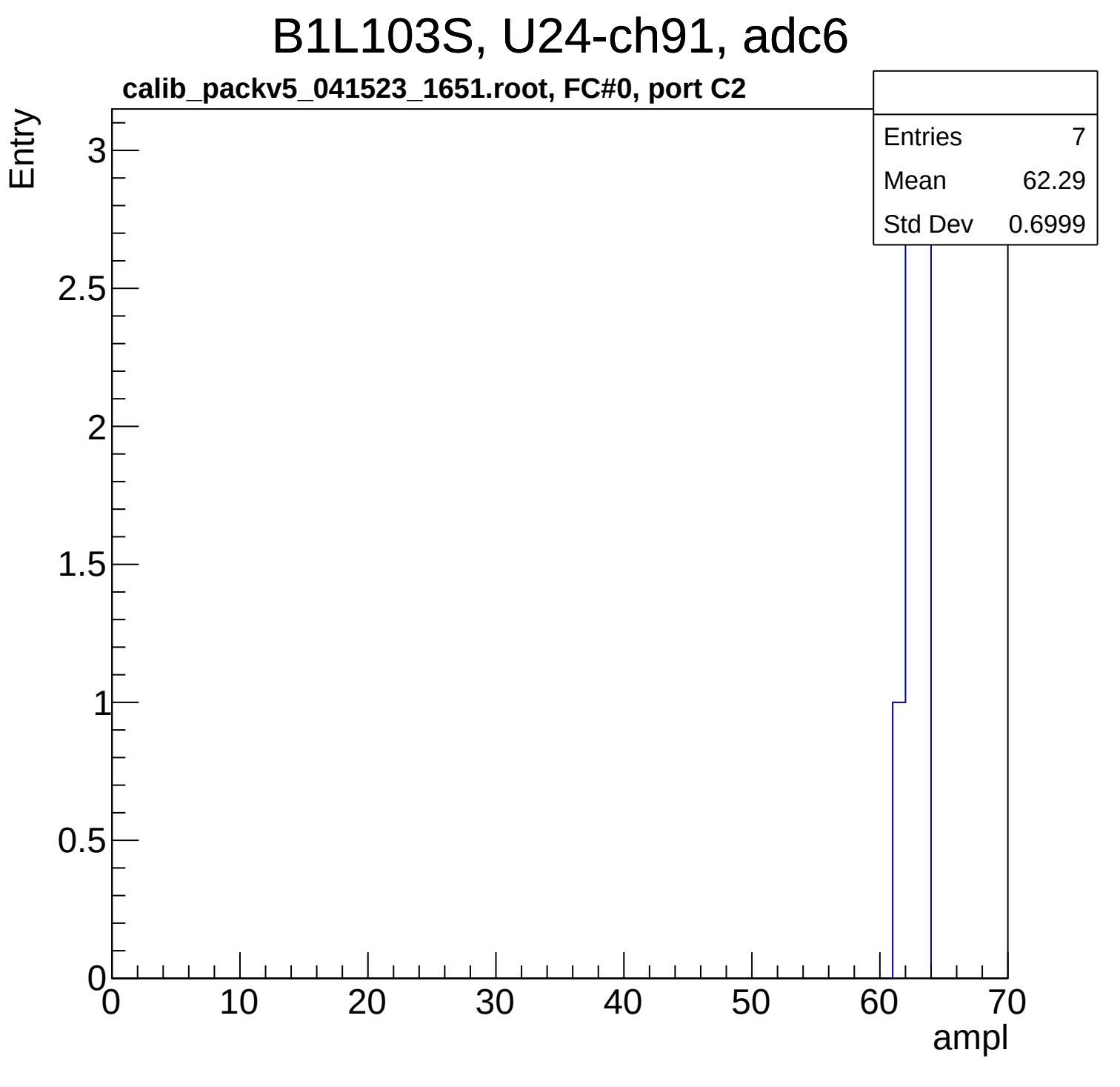
60
70


B1L103S, U24-ch91, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 62.29
Std Dev 0.6999
Entry
ampl
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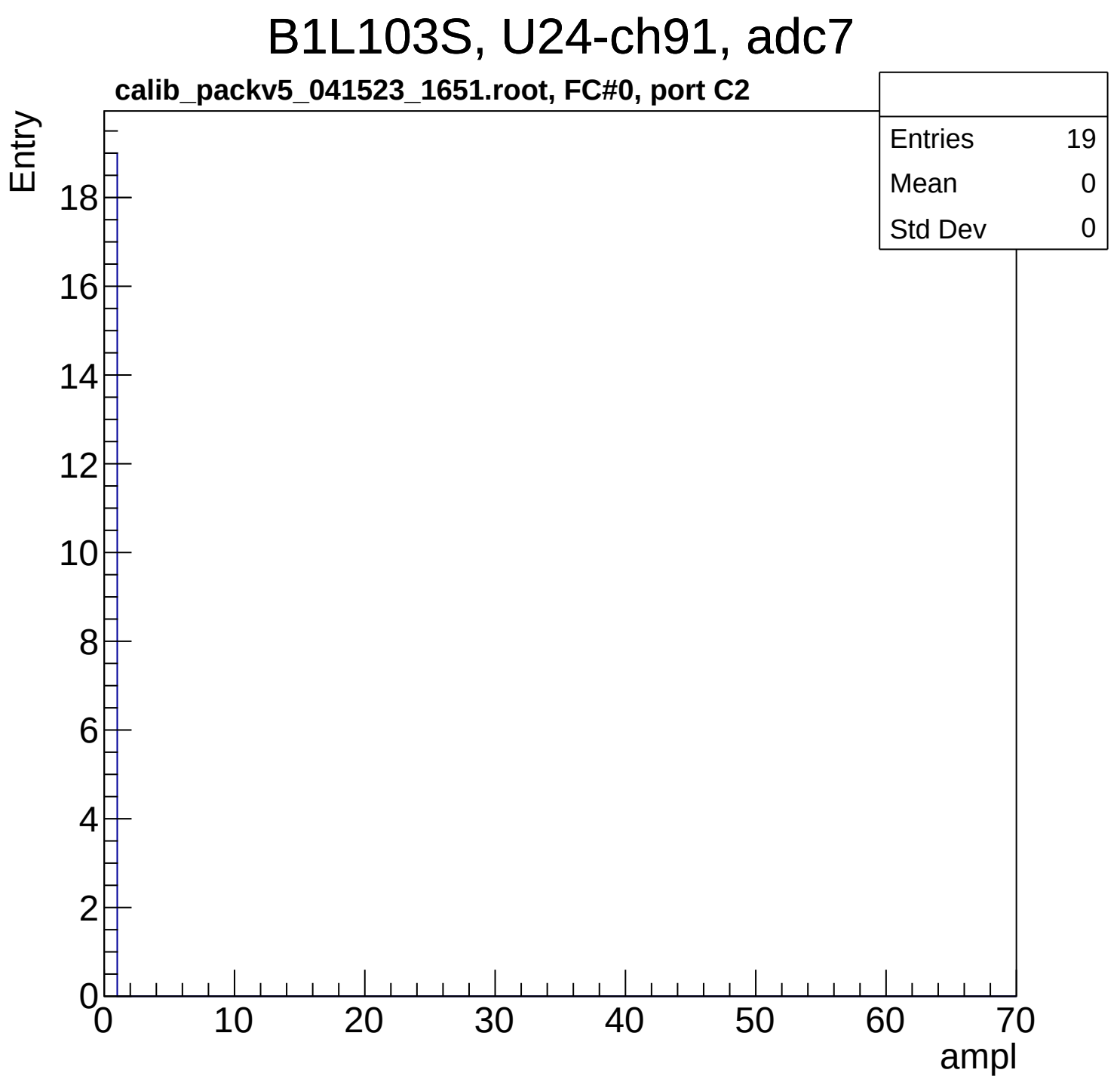
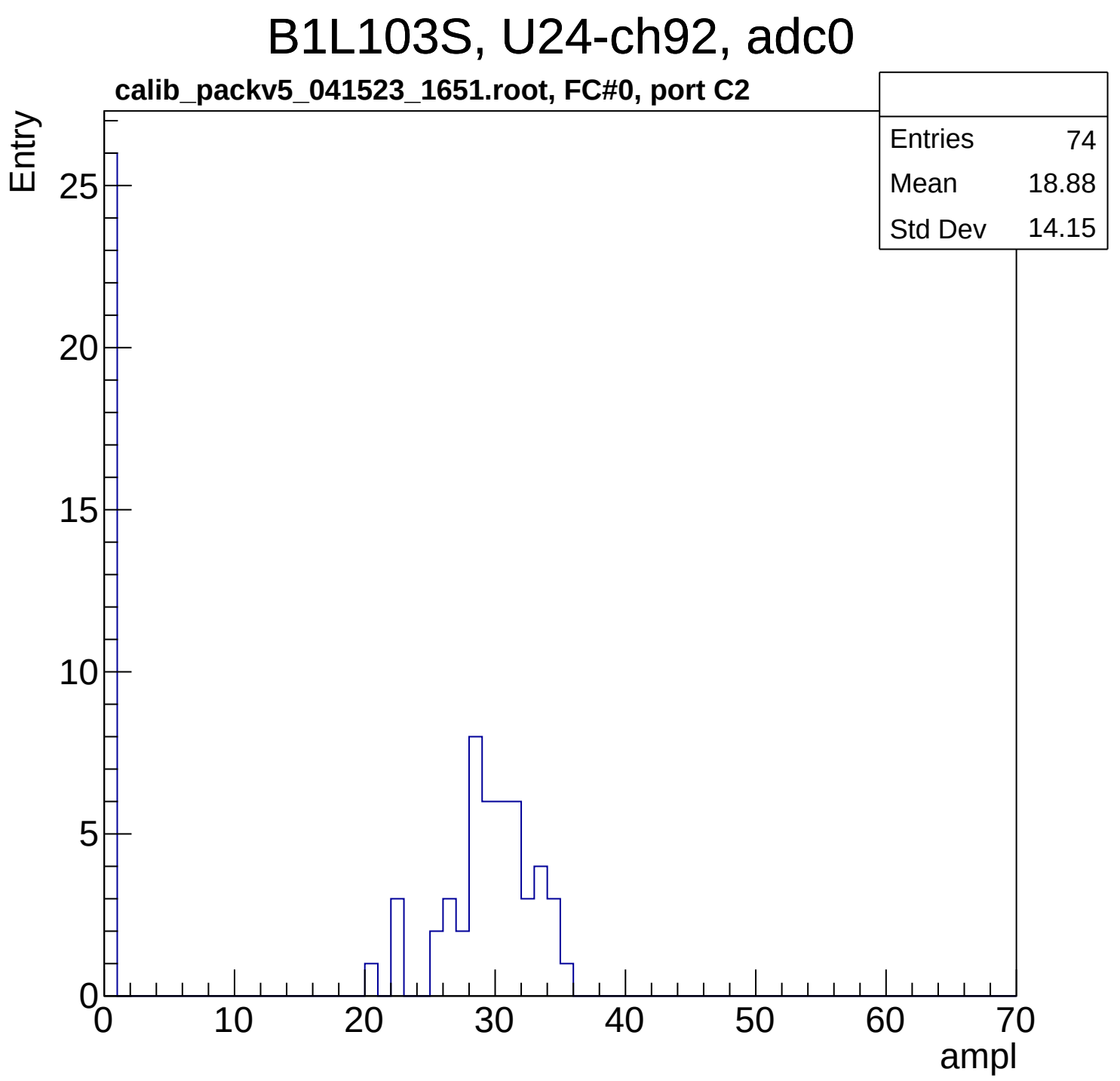
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U24-ch91, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch92, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 18.88
Std Dev 14.15
Entry
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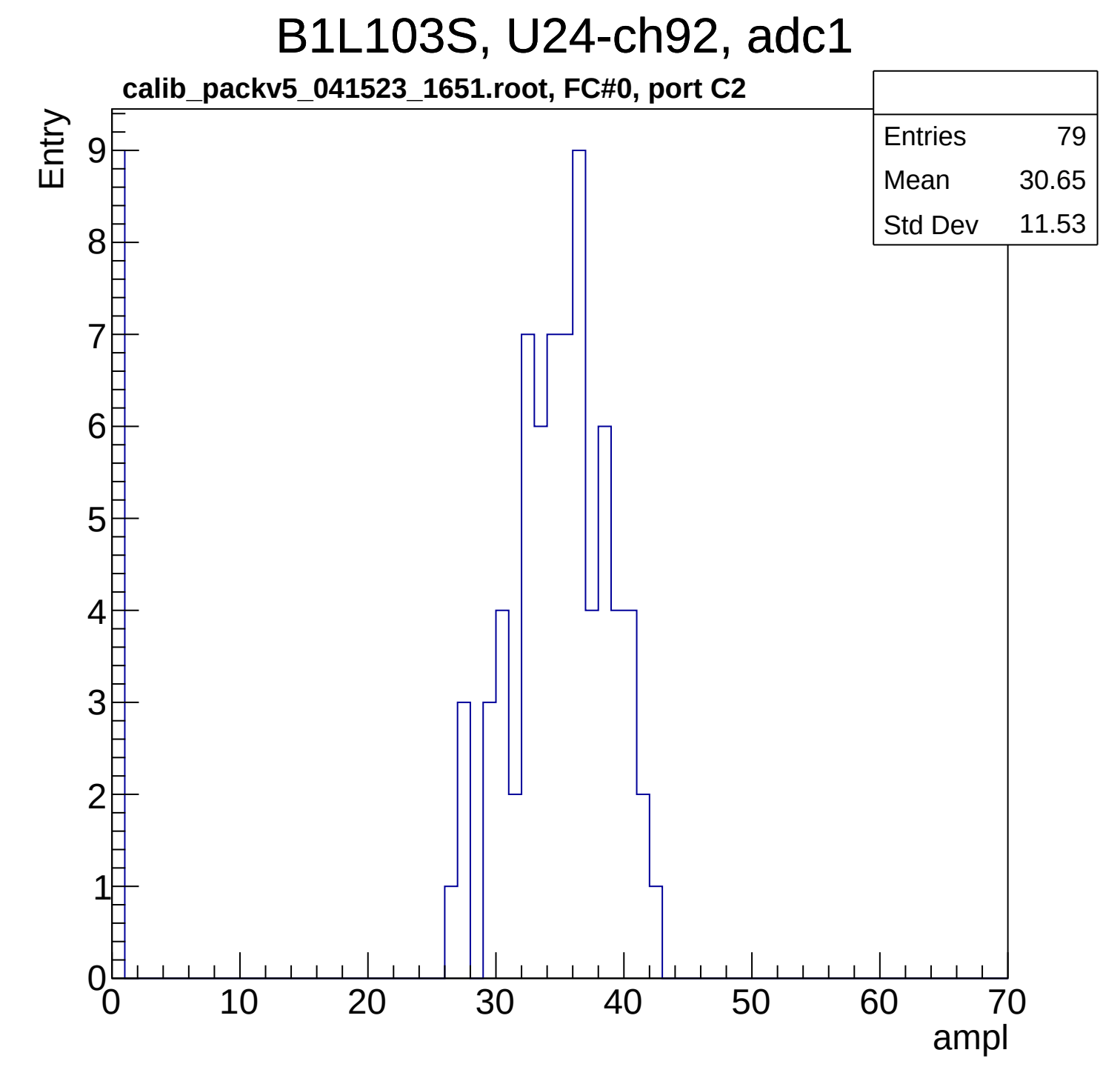
5
10
15
20
25
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch92, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 30.65
Std Dev 11.53
Entry
ampl
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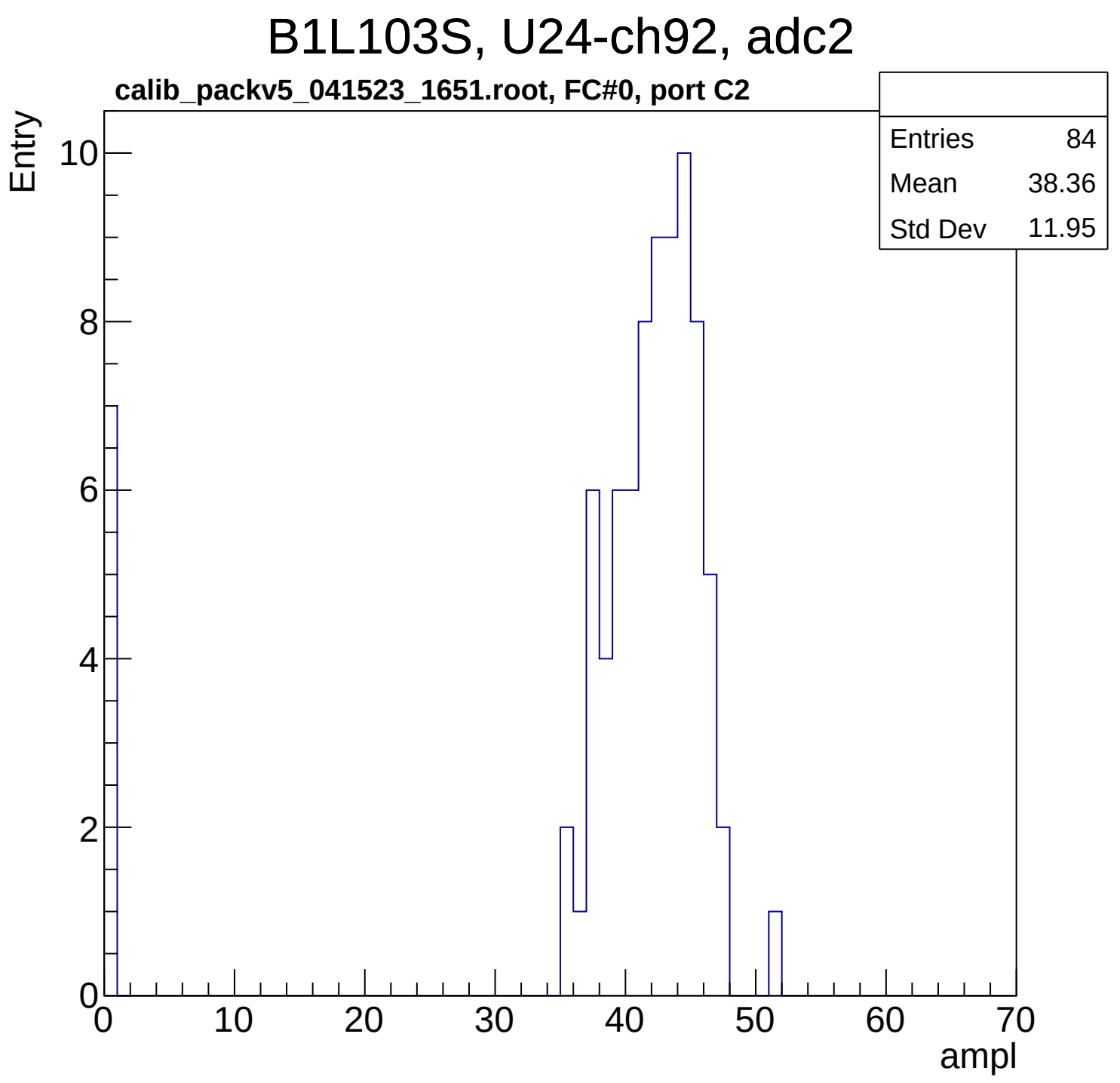
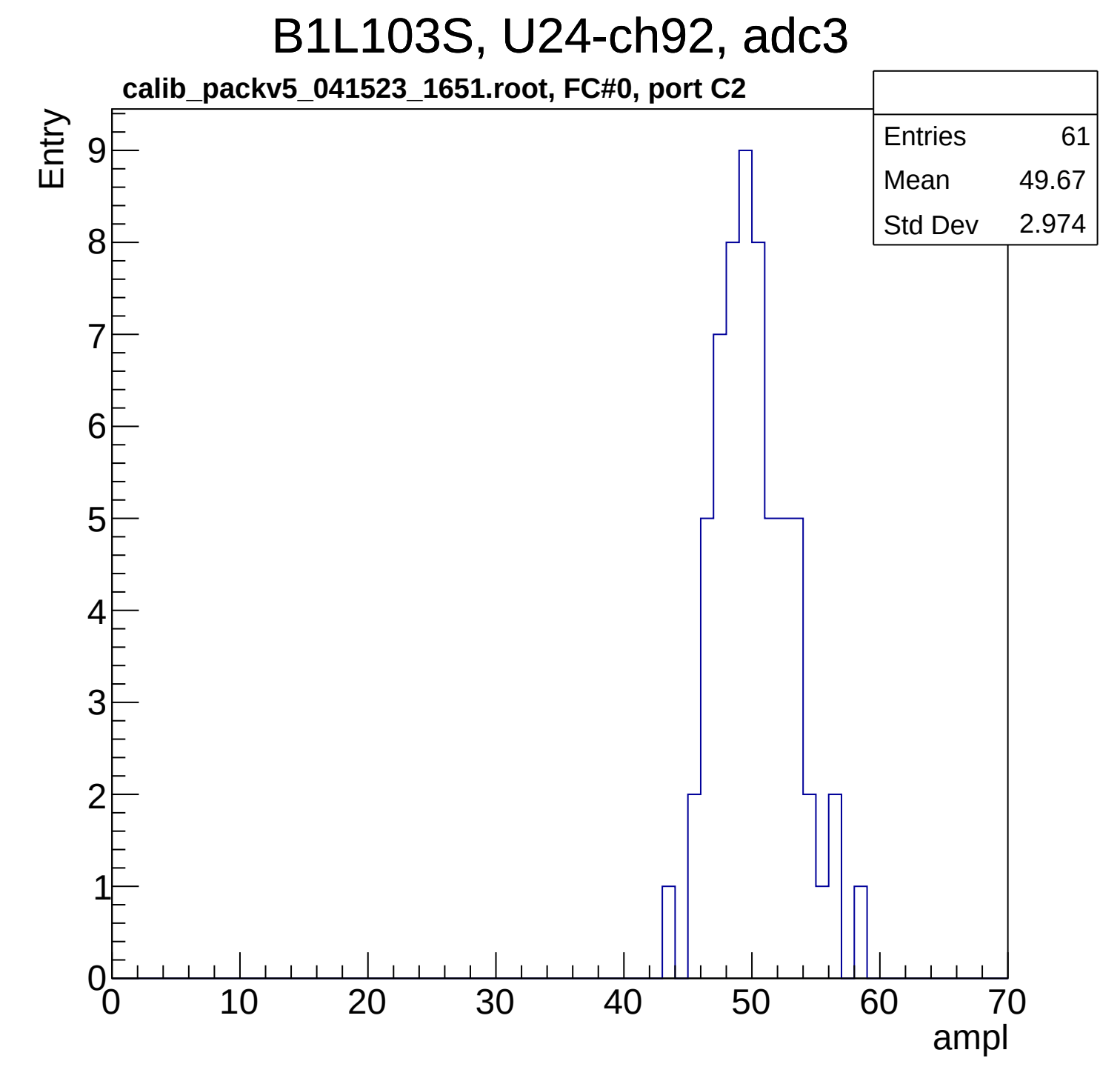
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U24-ch92, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 38.36
Std Dev 11.95
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U24-ch92, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 49.67
Std Dev 2.974
Entry
ampl
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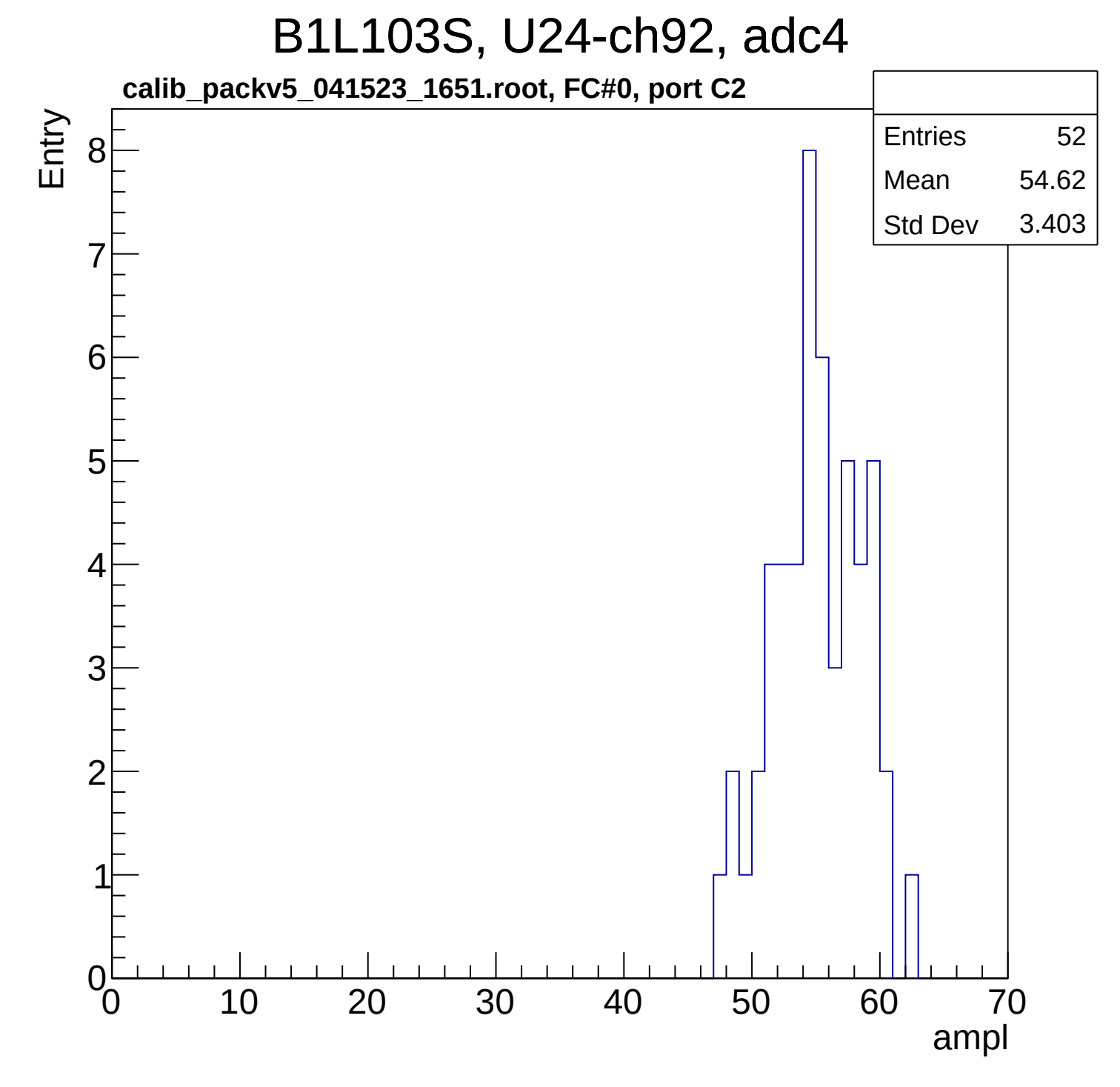
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U24-ch92, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 54.62
Std Dev 3.403
Entry
ampl
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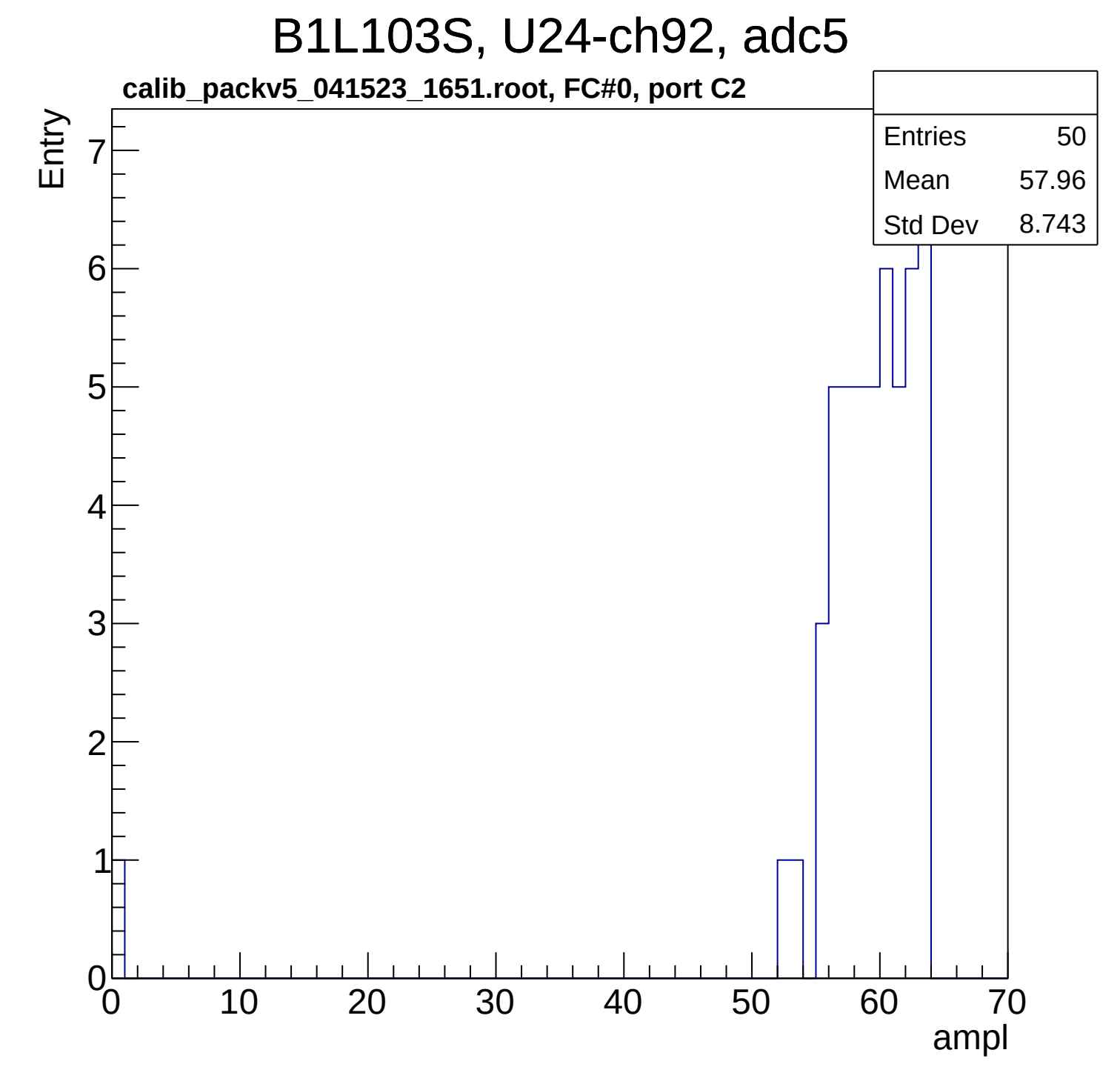
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U24-ch92, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 57.96
Std Dev 8.743
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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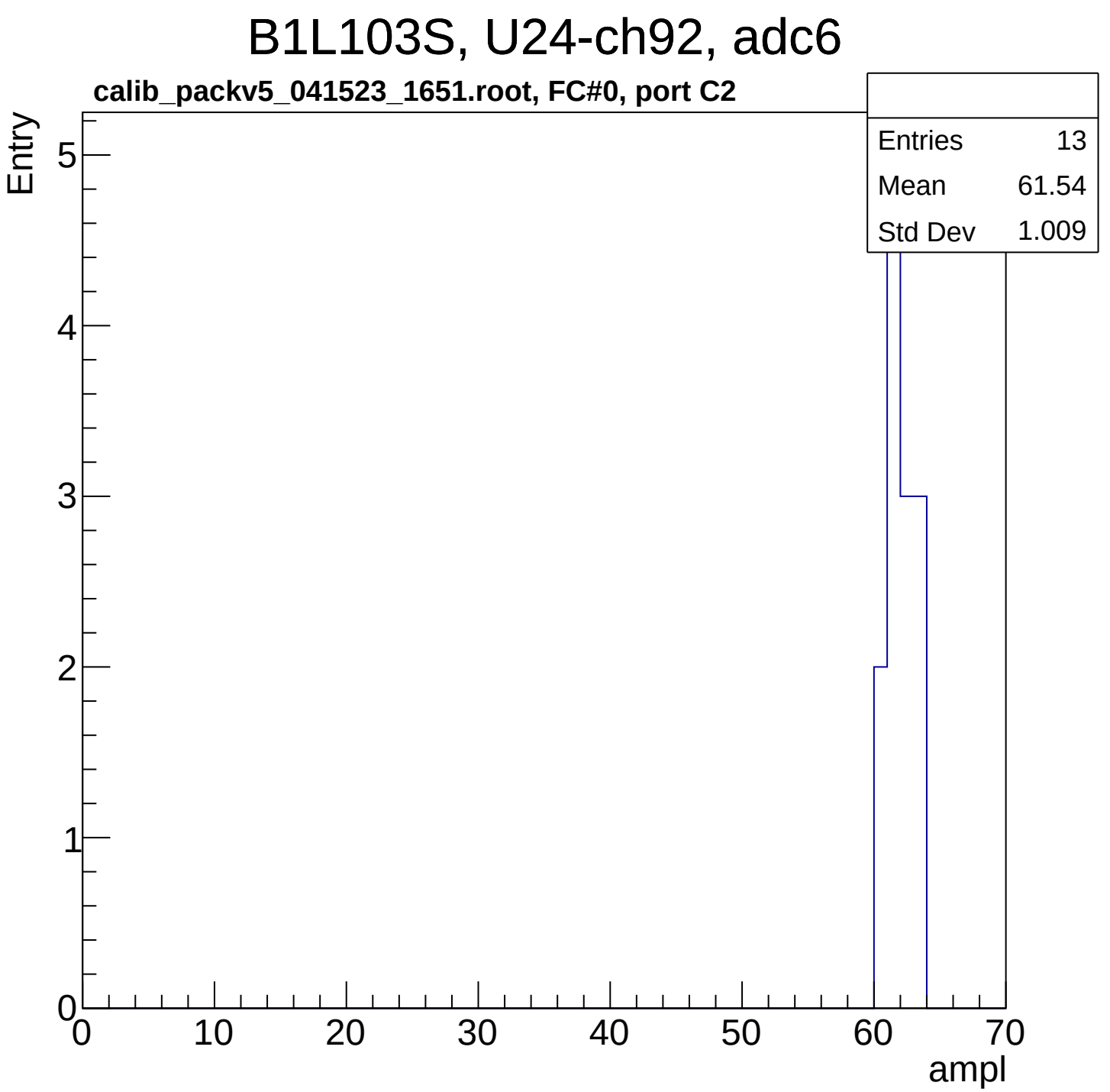
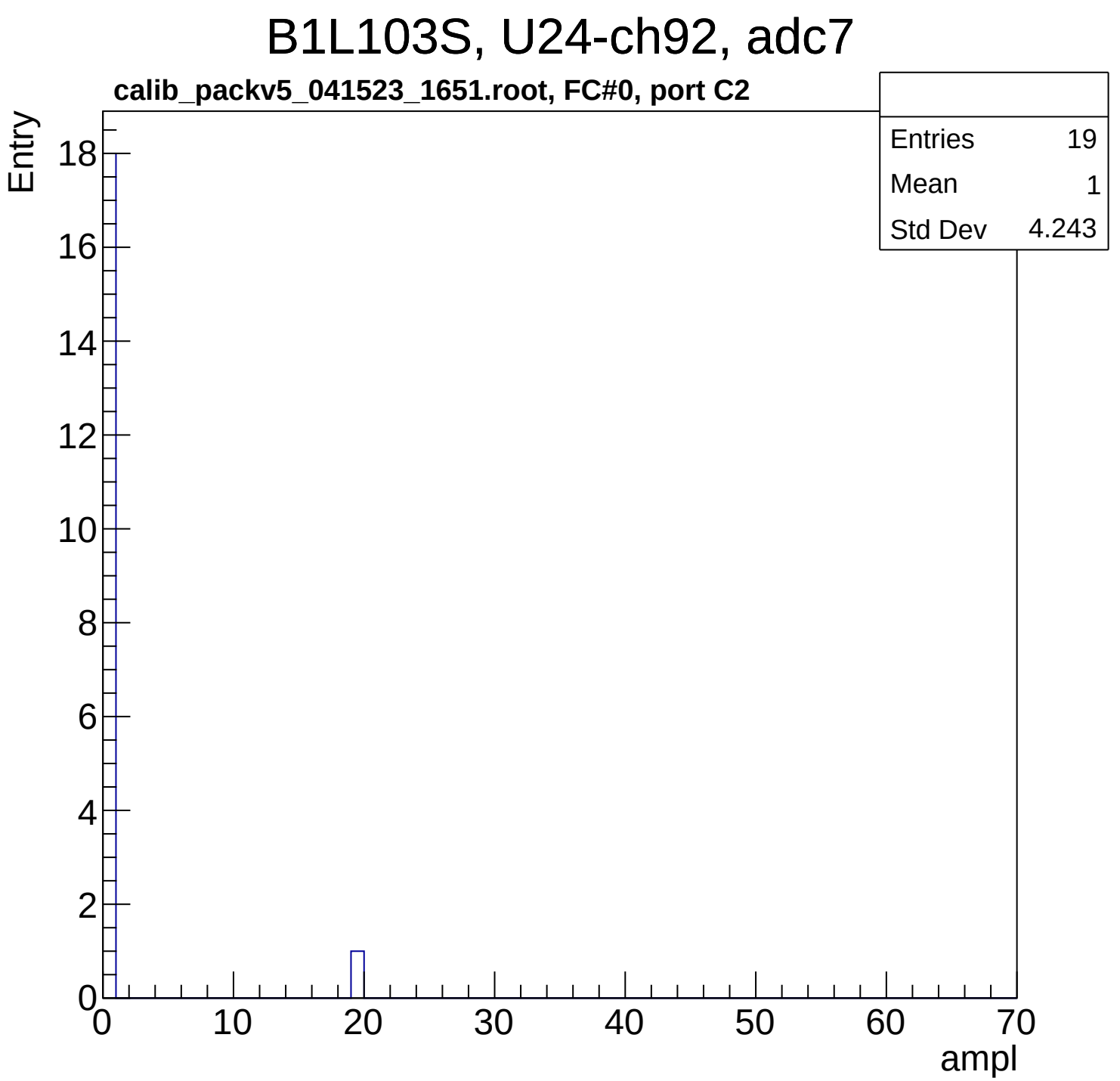

B1L103S, U24-ch92, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 13
Mean 61.54
Std Dev 1.009
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch92, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1
Std Dev 4.243
Entry
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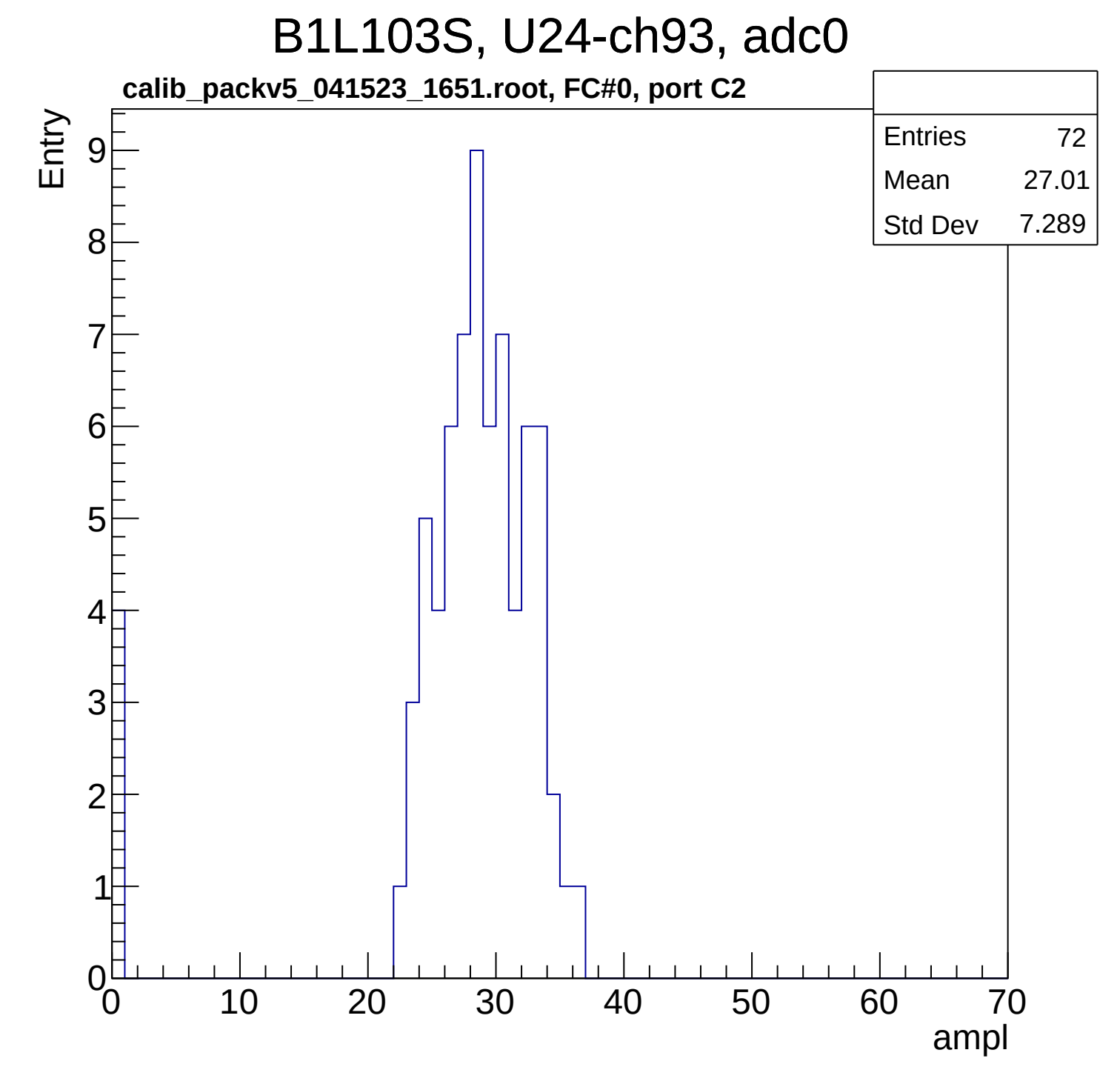
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch93, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 27.01
Std Dev 7.289
Entry
ampl
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4
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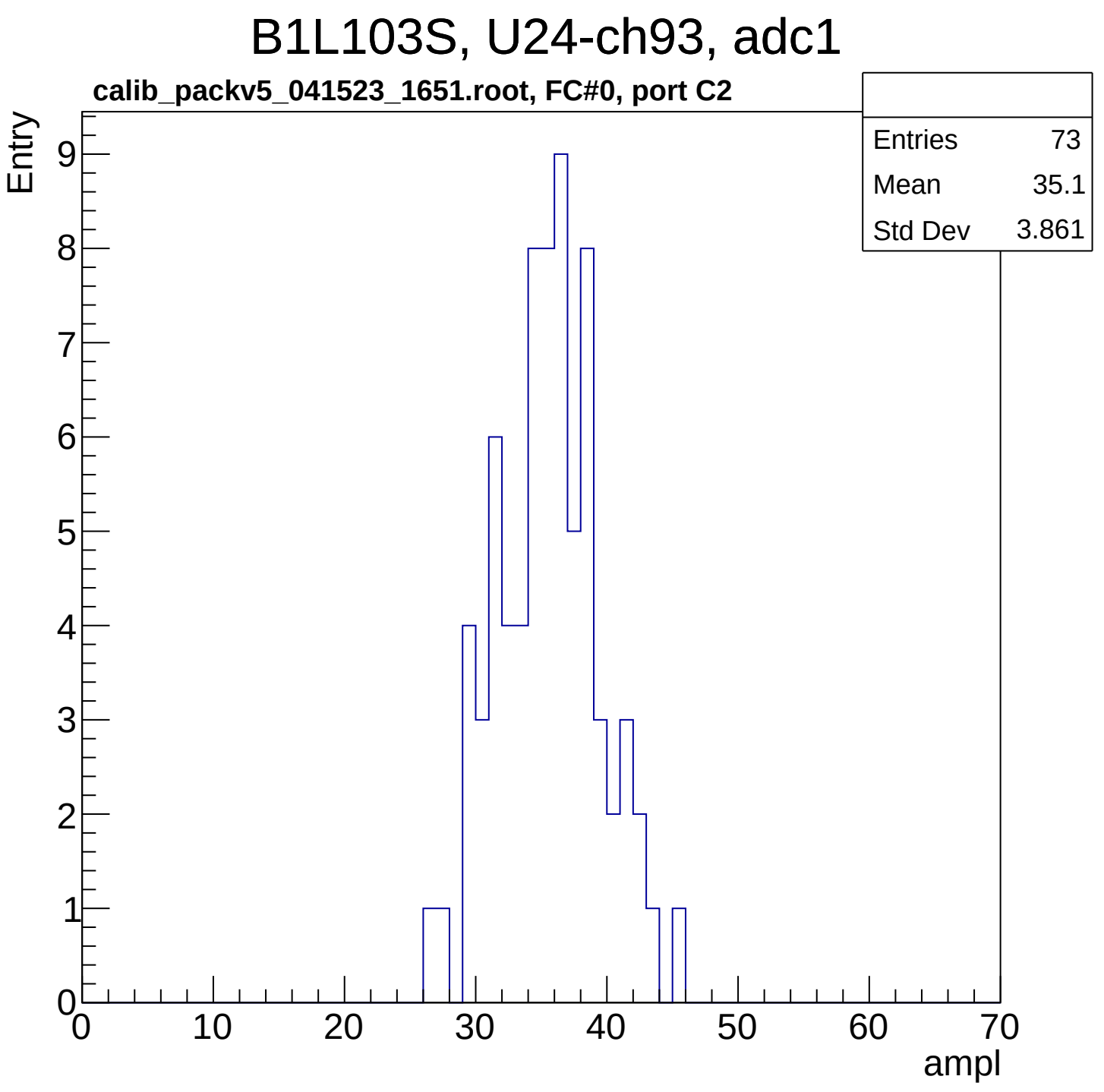
B1L103S, U24-ch93, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 35.1
Std Dev 3.861
Entry
ampl
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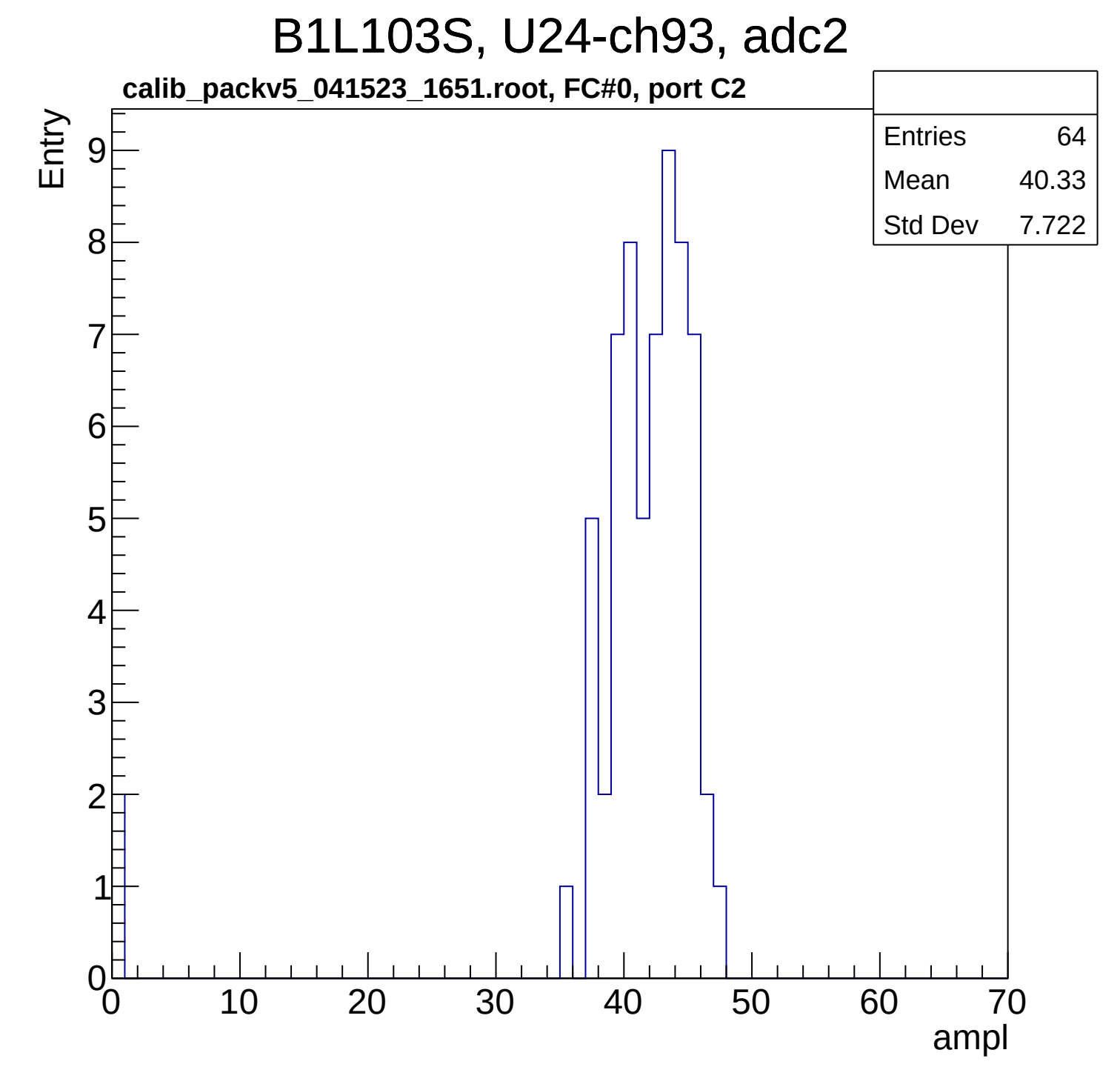
B1L103S, U24-ch93, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 40.33
Std Dev 7.722
Entry
ampl
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3
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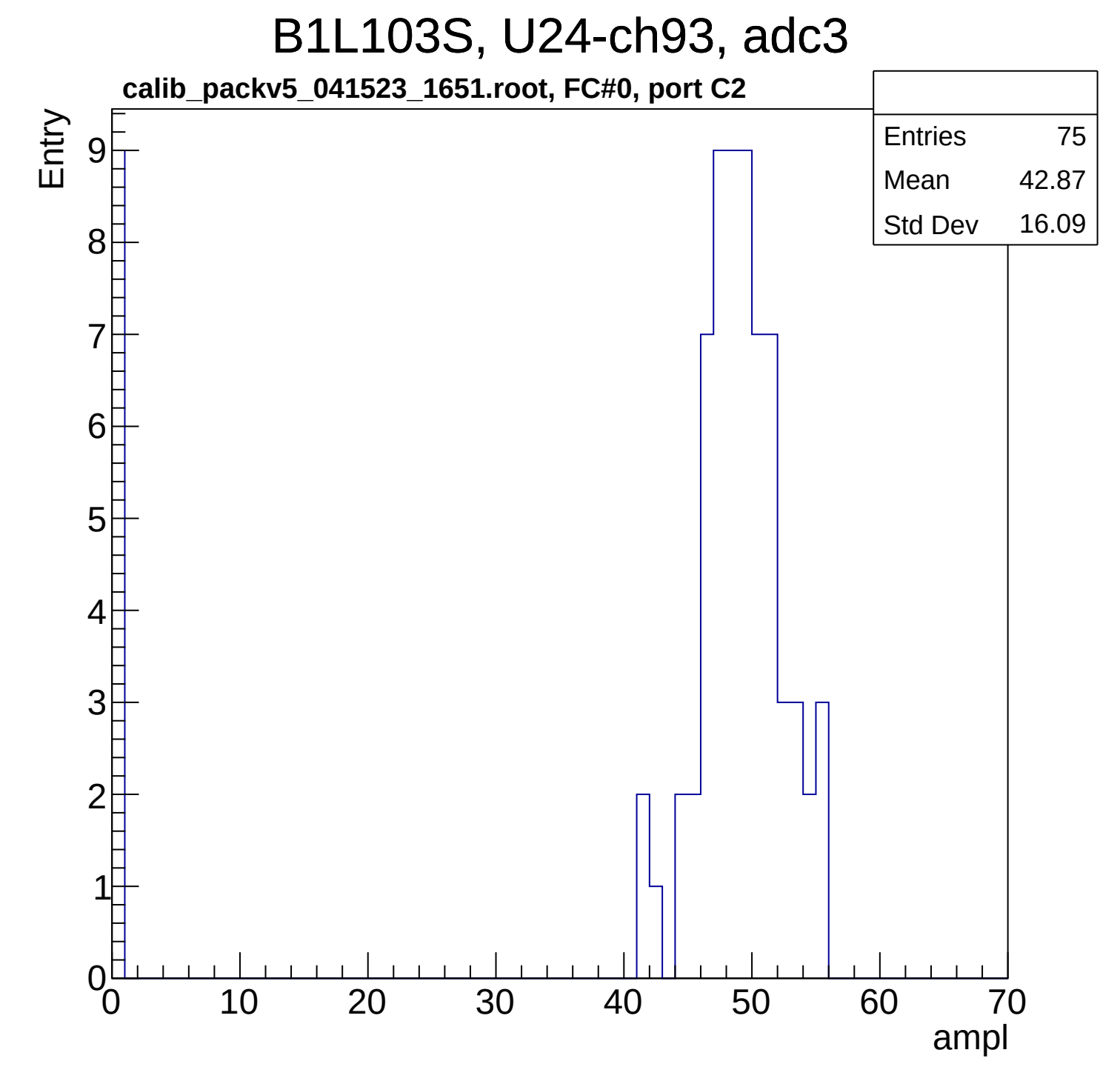
B1L103S, U24-ch93, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 42.87
Std Dev 16.09
Entry
ampl
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2
3
4
5
6
7
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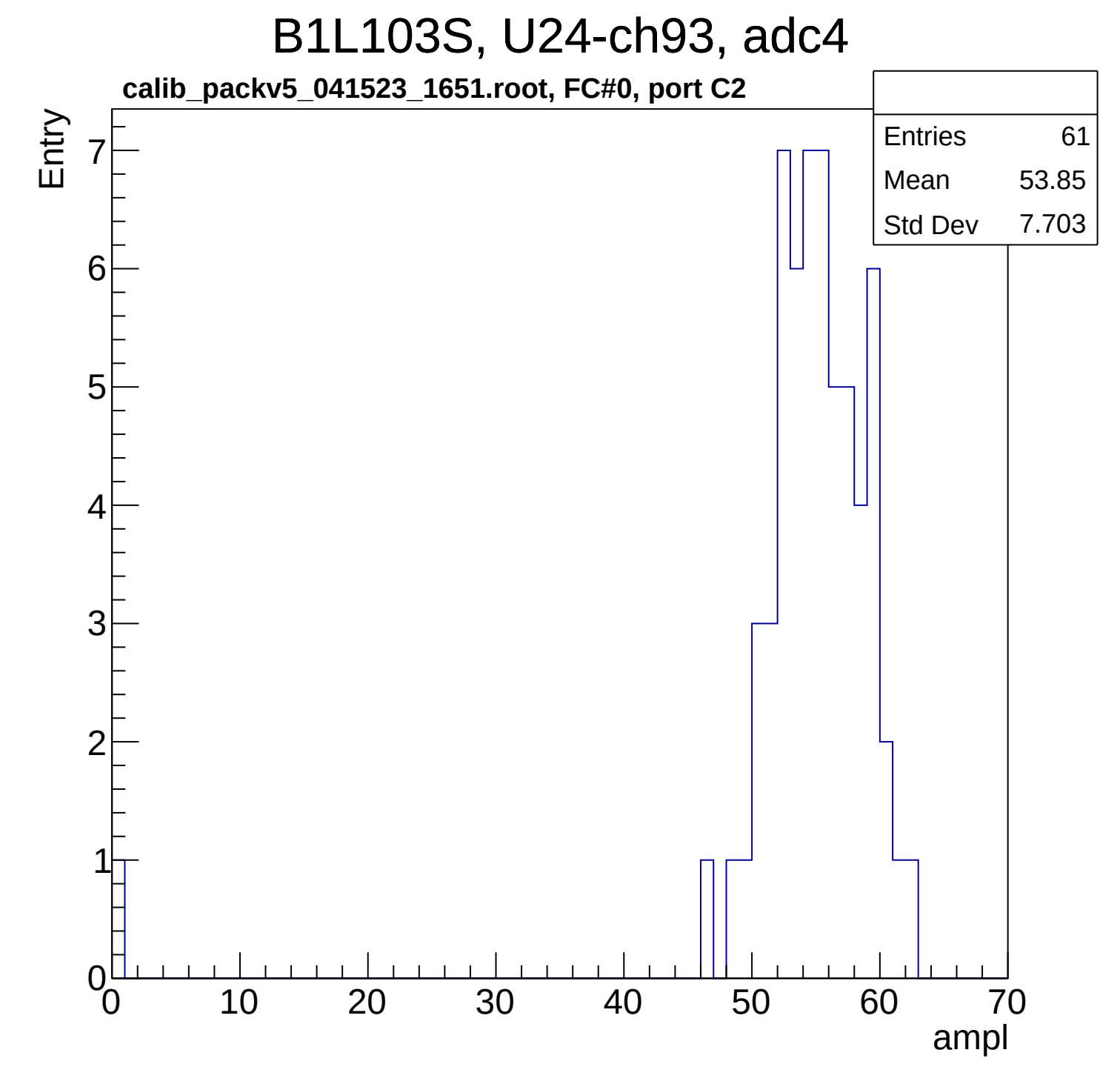
B1L103S, U24-ch93, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 53.85
Std Dev 7.703
Entry
ampl
0
1
2
3
4
5
6
7
0
10
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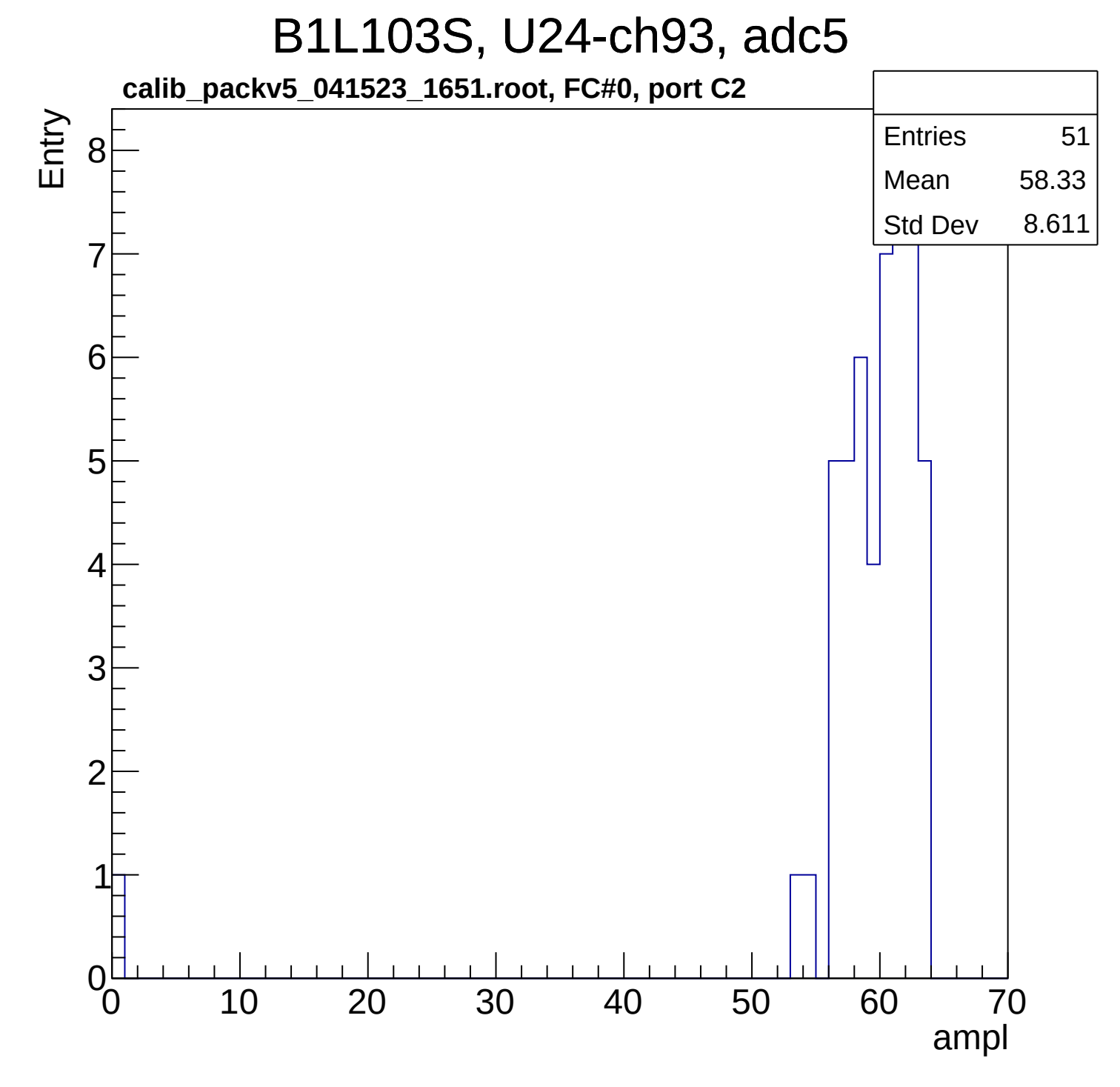
B1L103S, U24-ch93, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 58.33
Std Dev 8.611
Entry
ampl
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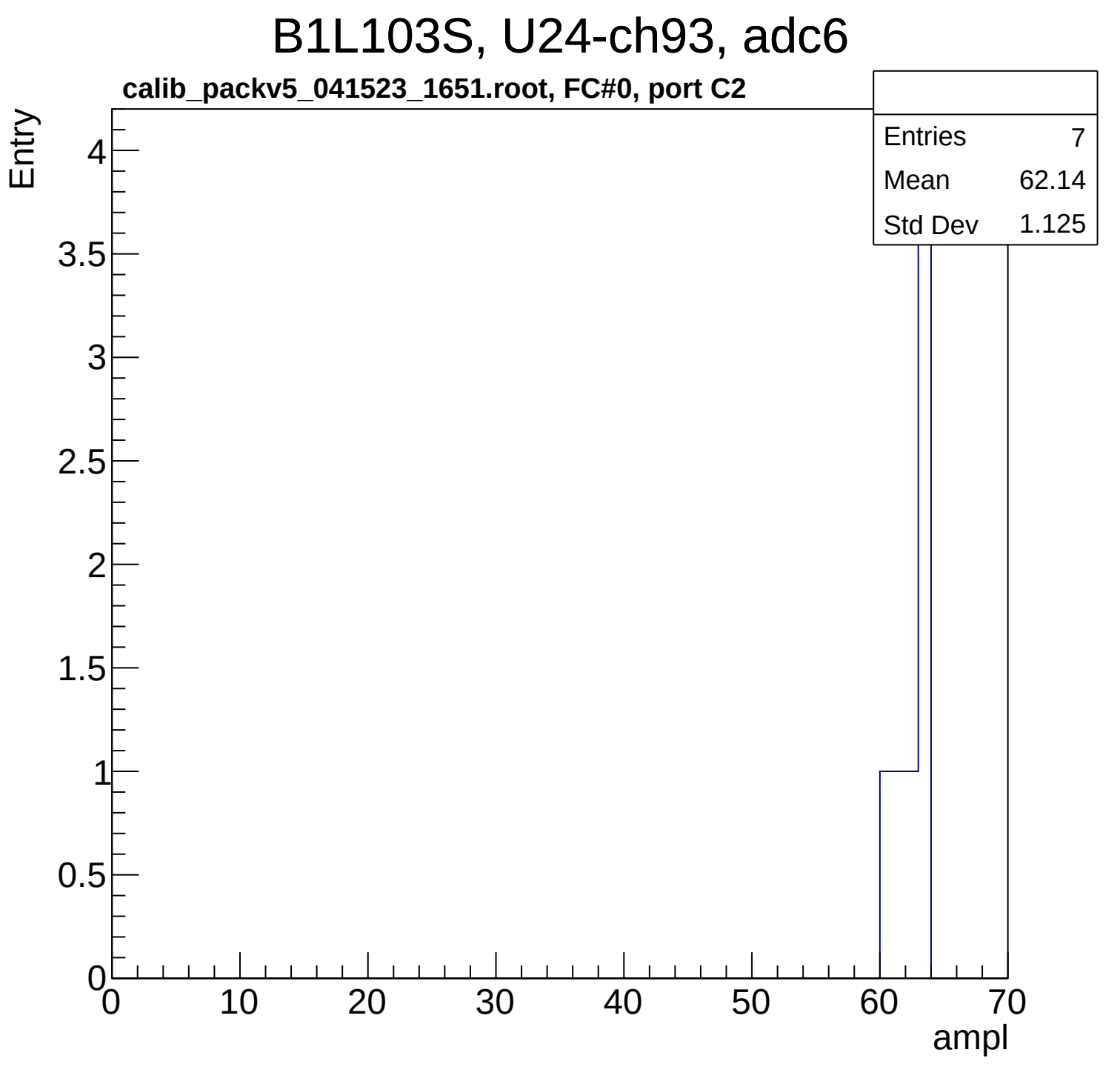
B1L103S, U24-ch93, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 62.14
Std Dev 1.125
Entry
ampl
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1.5
2
2.5
3
3.5
4
0
10
20
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40
50
60
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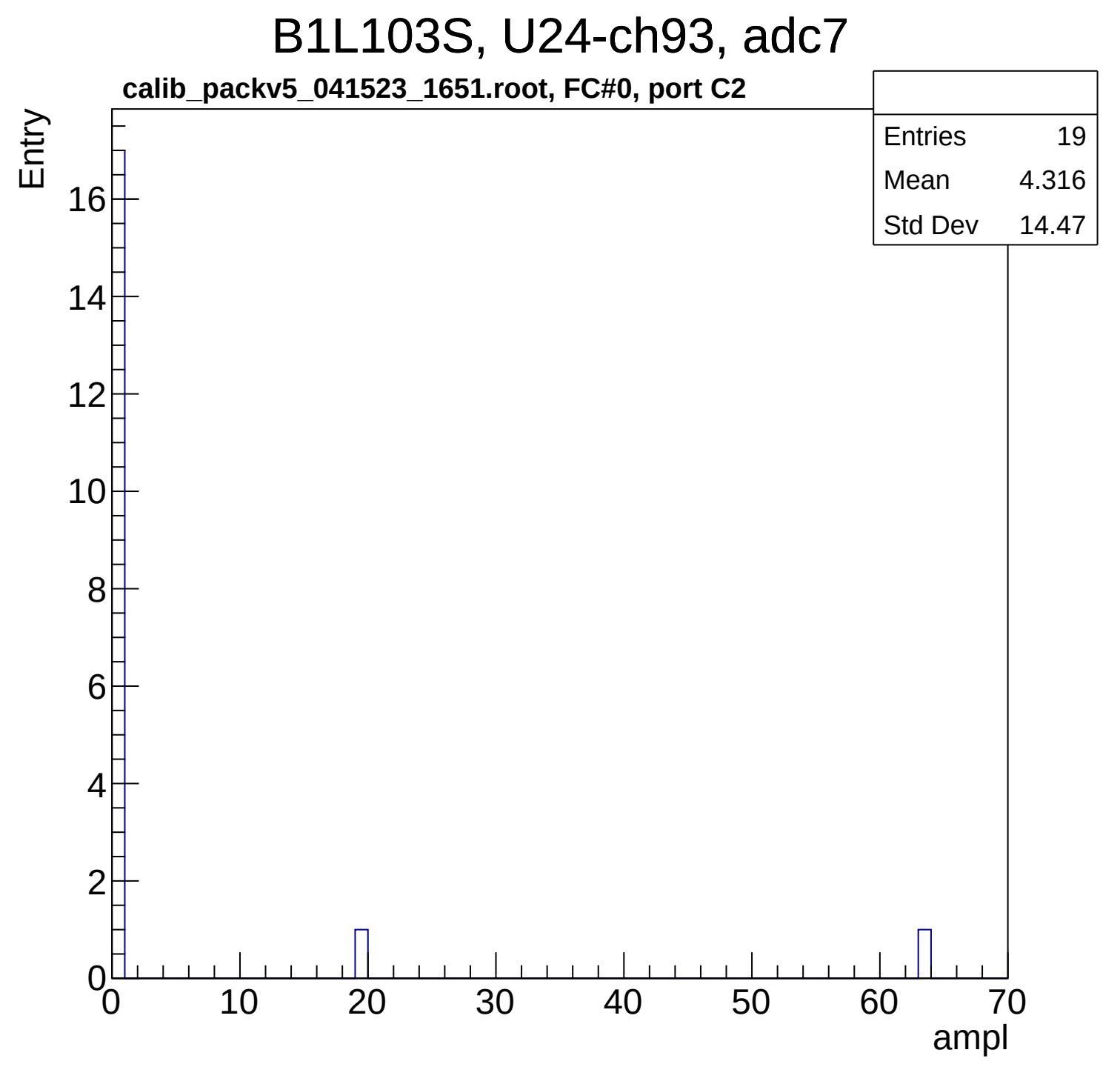
B1L103S, U24-ch93, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 4.316
Std Dev 14.47
Entry
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6
8
10
12
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16
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10
20
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50
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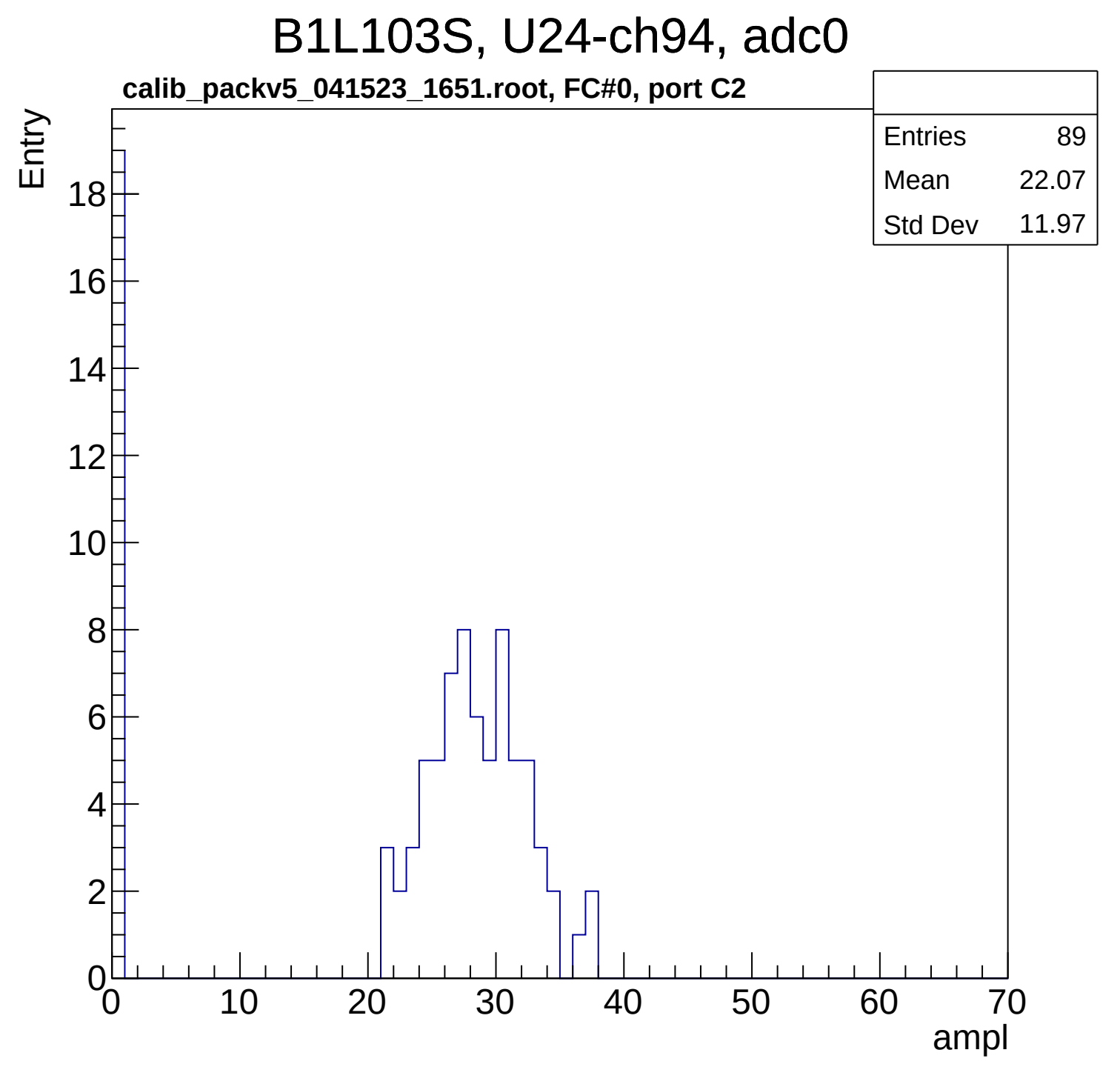
70
ampl


B1L103S, U24-ch94, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 89
Mean 22.07
Std Dev 11.97
Entry
ampl
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4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
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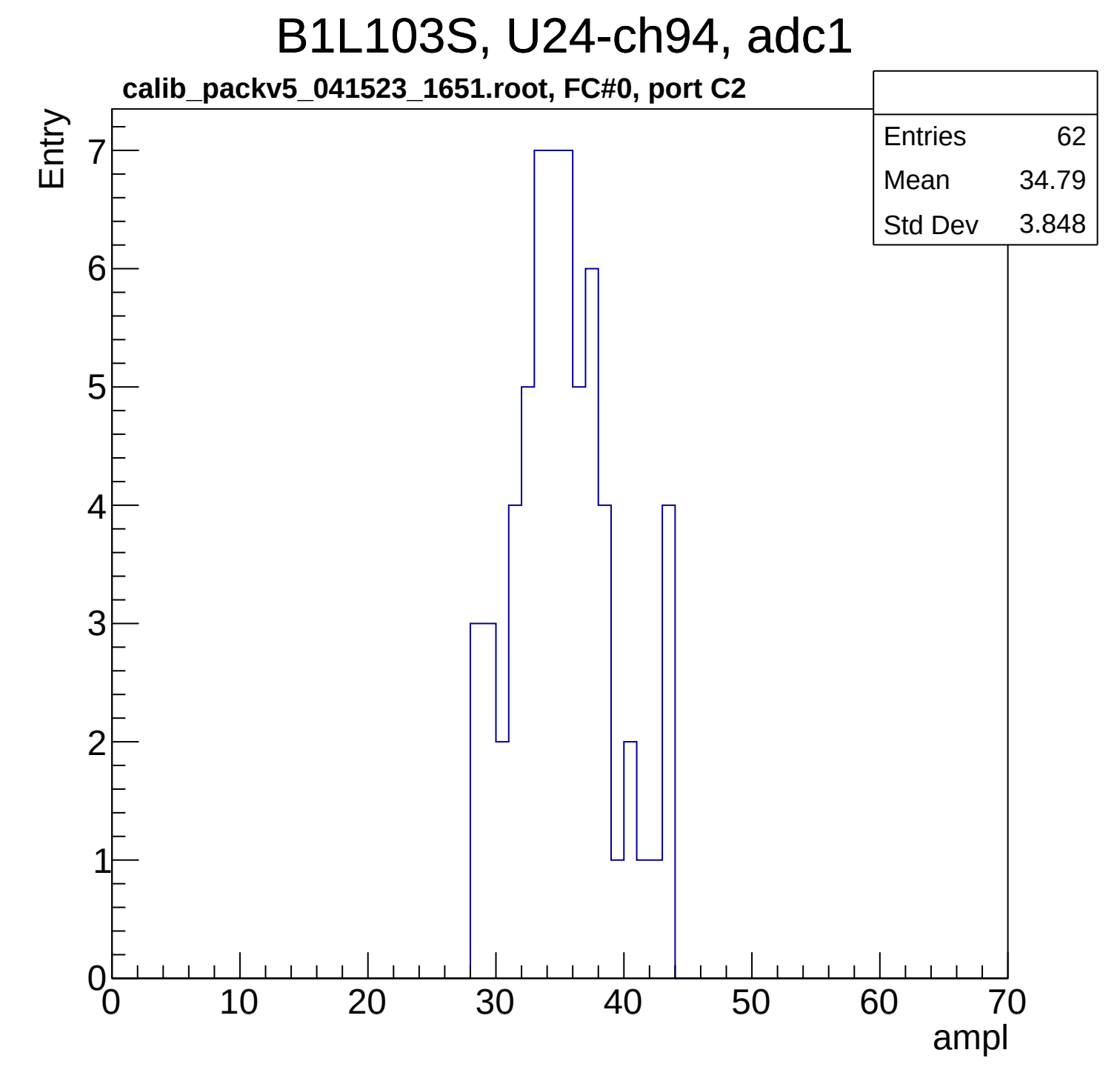
B1L103S, U24-ch94, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 34.79
Std Dev 3.848
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
30
40
50
60
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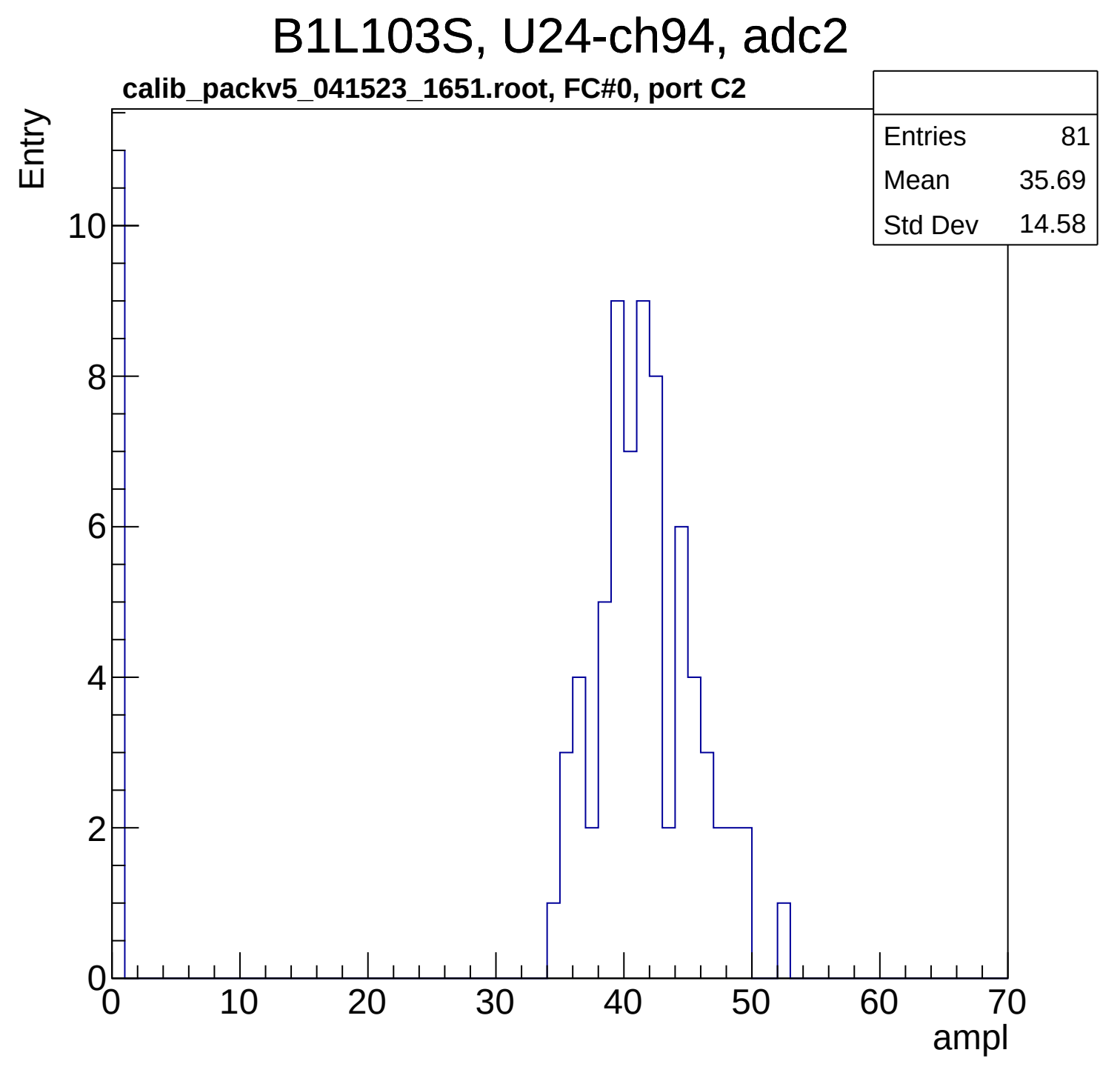
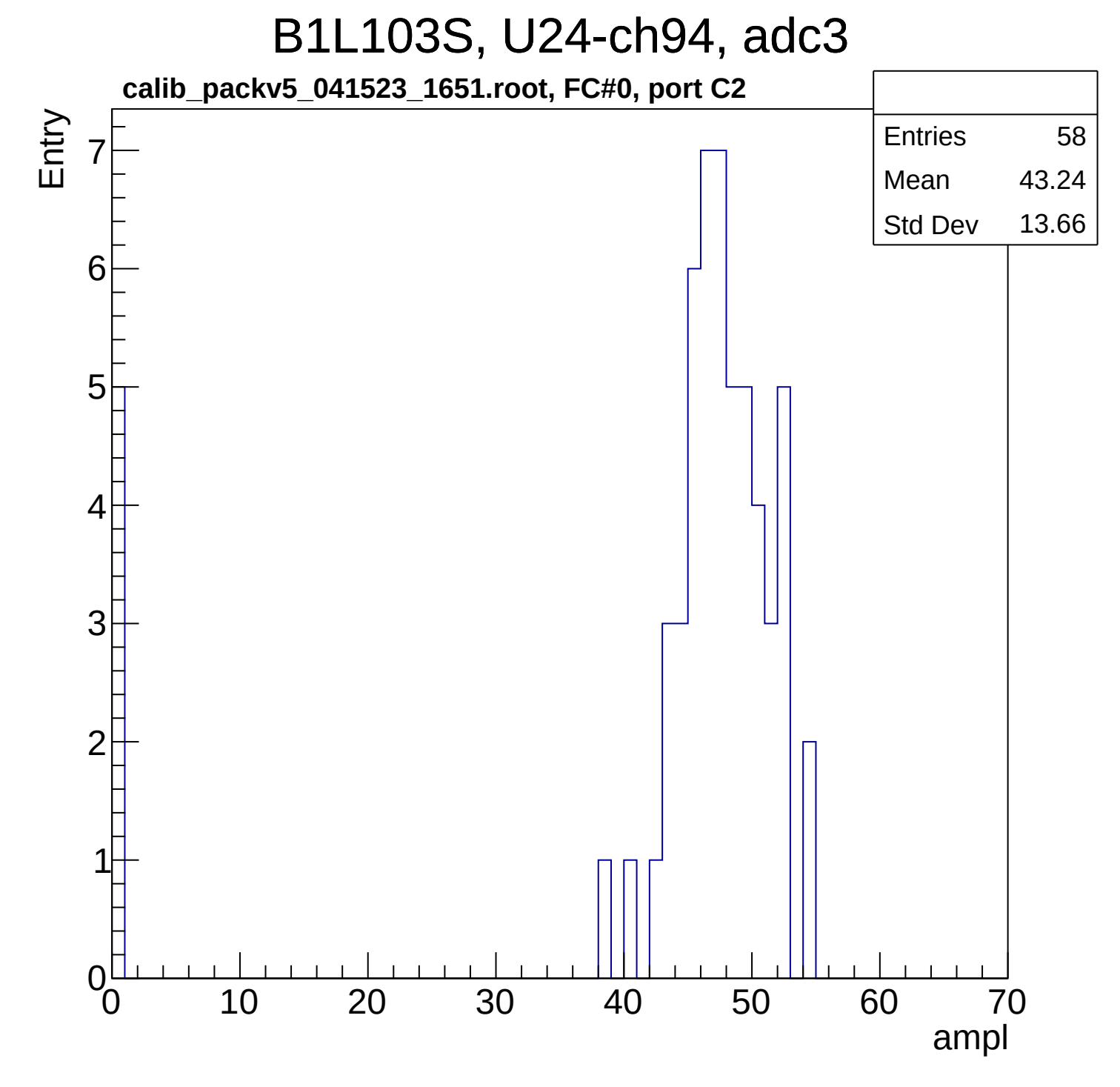

B1L103S, U24-ch94, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 35.69
Std Dev 14.58
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch94, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 43.24
Std Dev 13.66
Entry
ampl
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2
3
4
5
6
7
0
10
20
30
40
50
60
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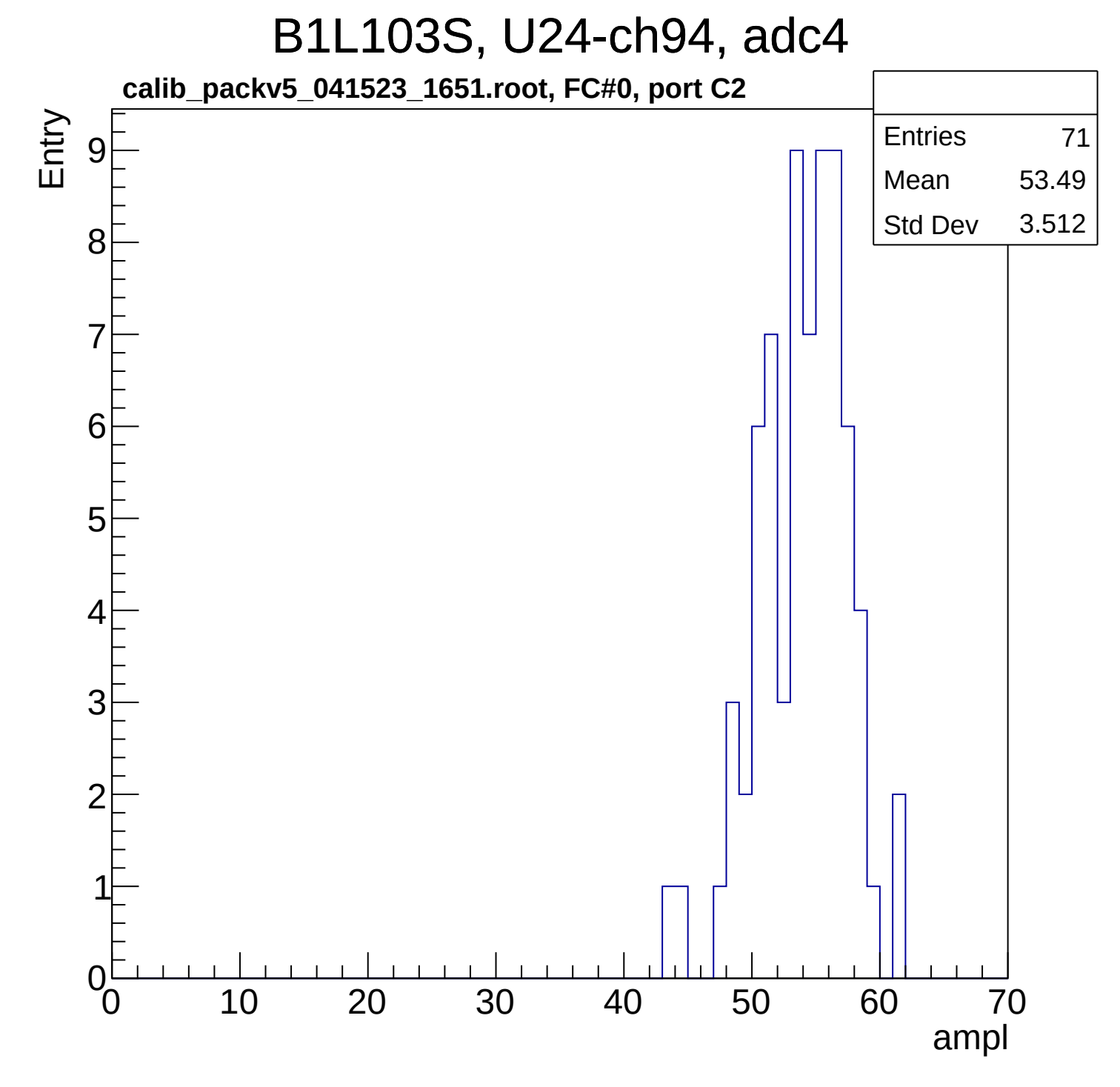
B1L103S, U24-ch94, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 53.49
Std Dev 3.512
Entry
ampl
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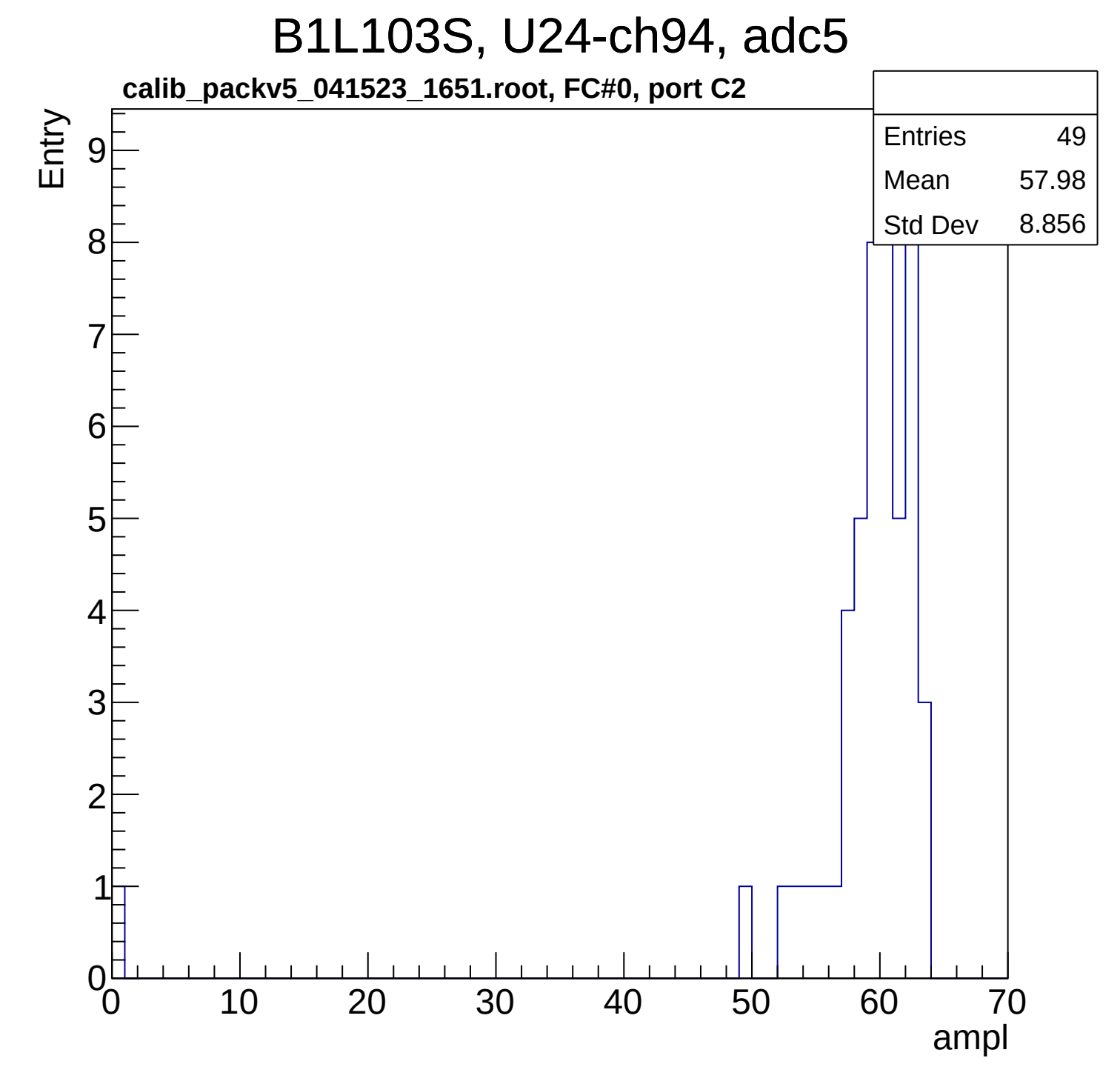
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U24-ch94, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 57.98
Std Dev 8.856
Entry
ampl
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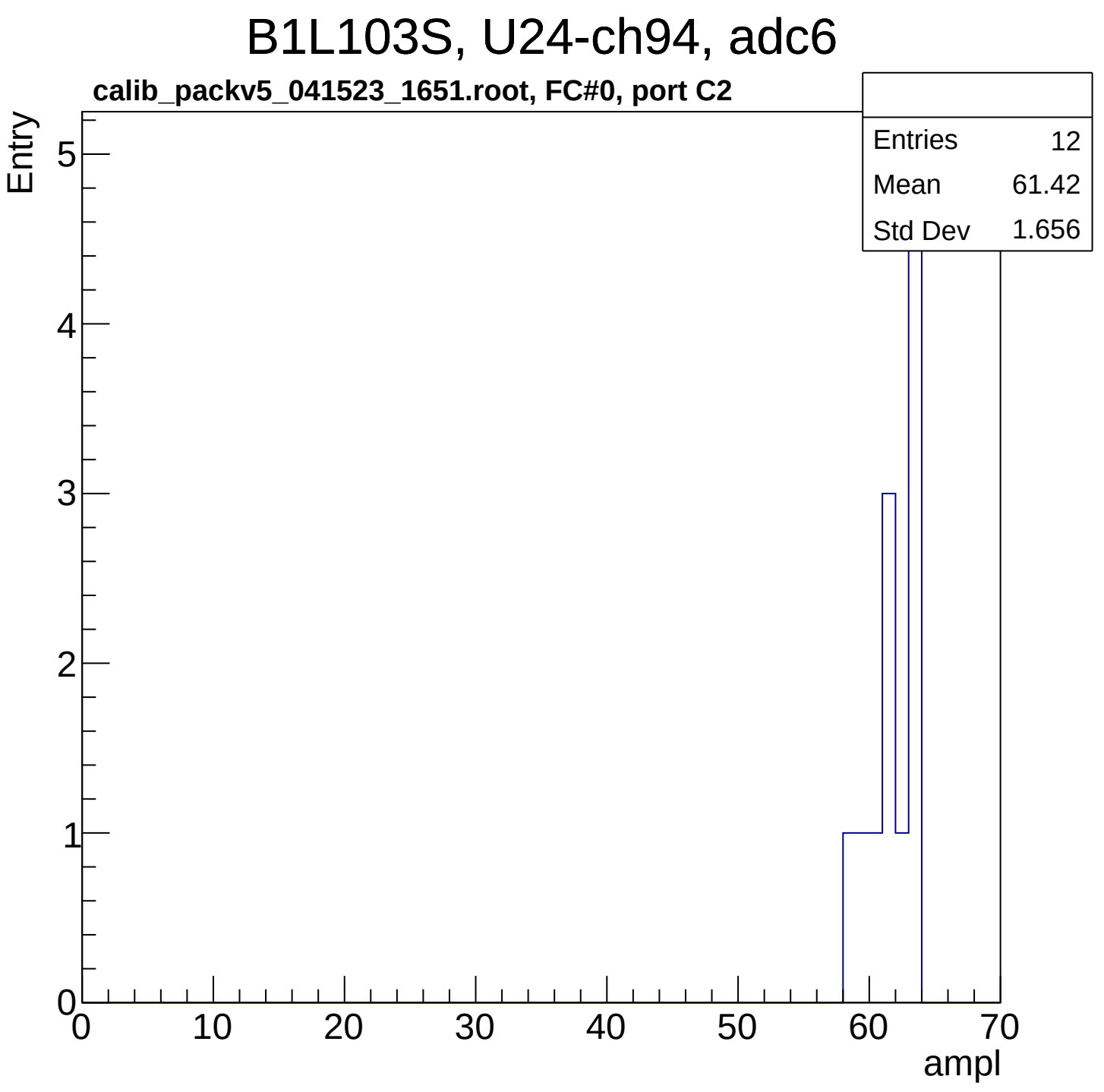
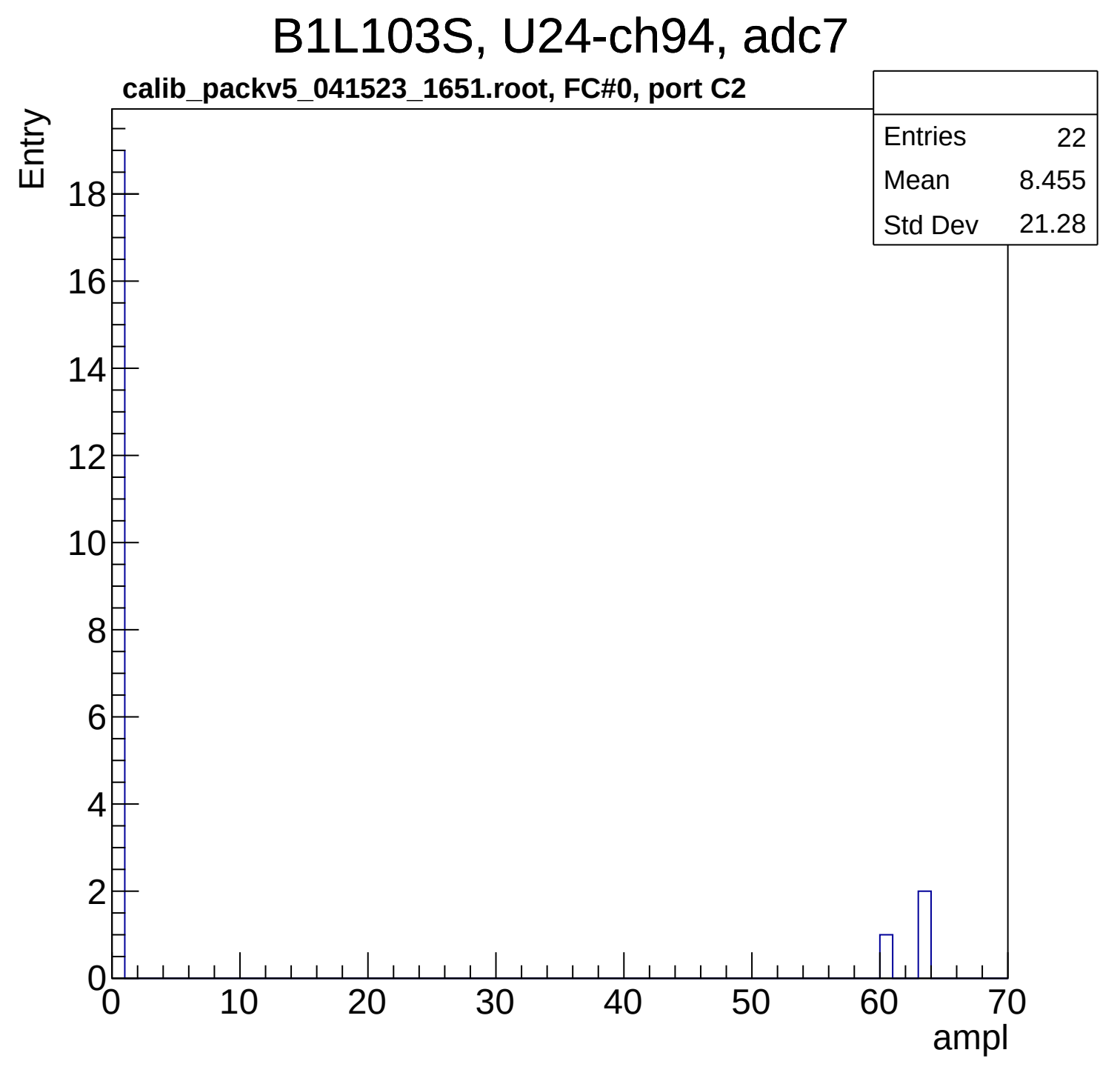
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U24-ch94, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 61.42
Std Dev 1.656
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch94, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 8.455
Std Dev 21.28
Entry
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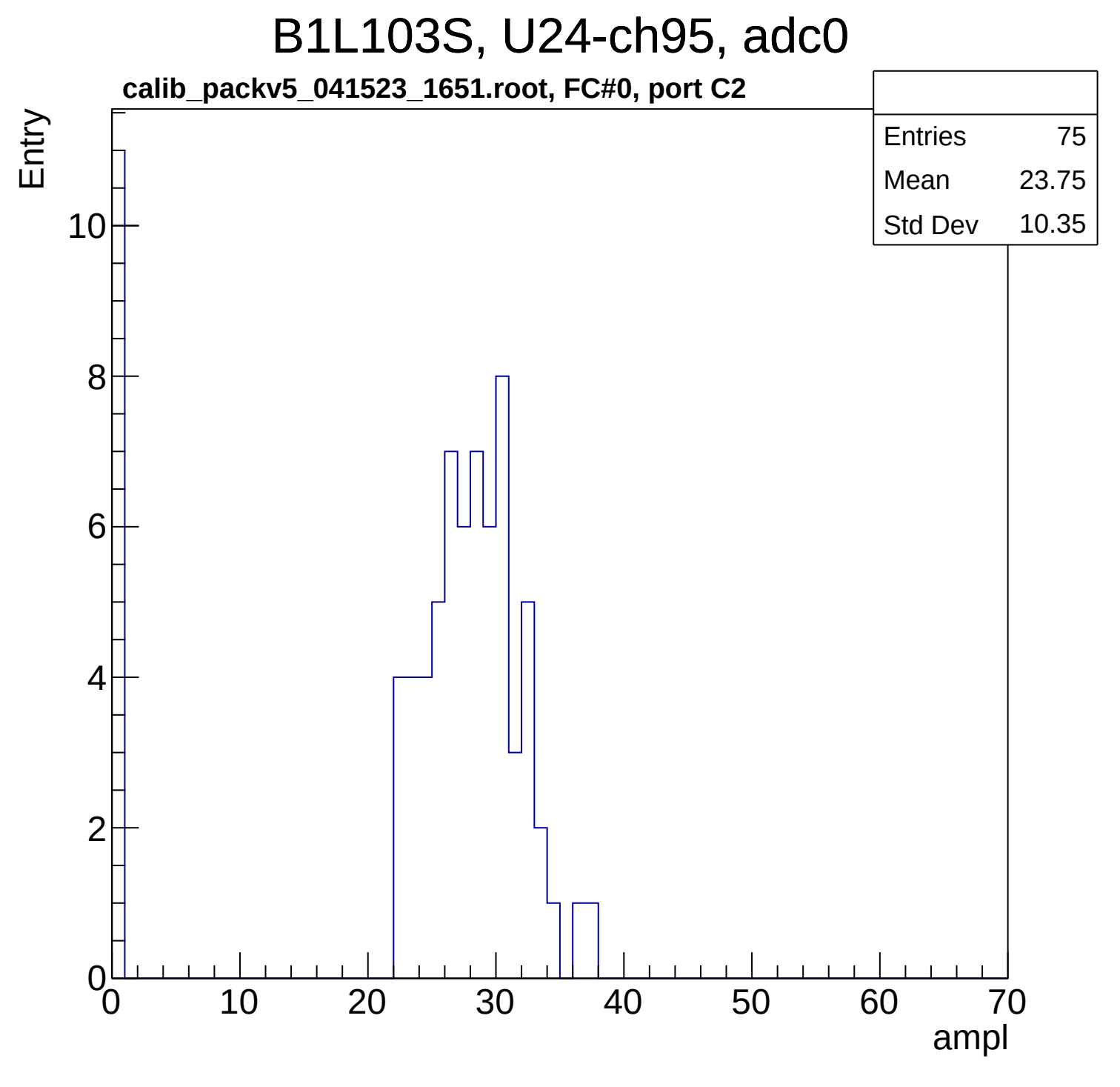
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch95, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 23.75
Std Dev 10.35
Entry
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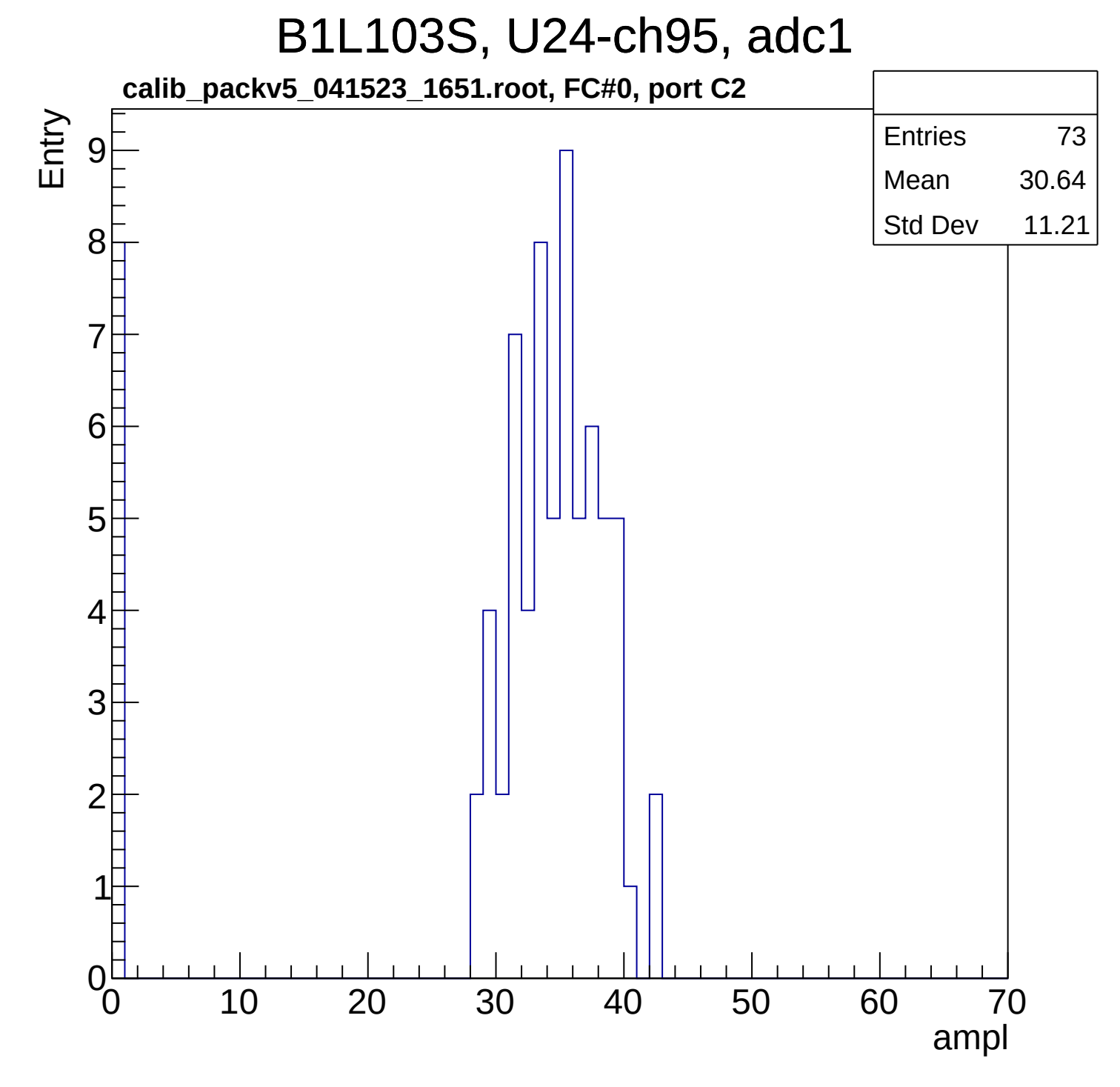
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch95, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 30.64
Std Dev 11.21
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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60
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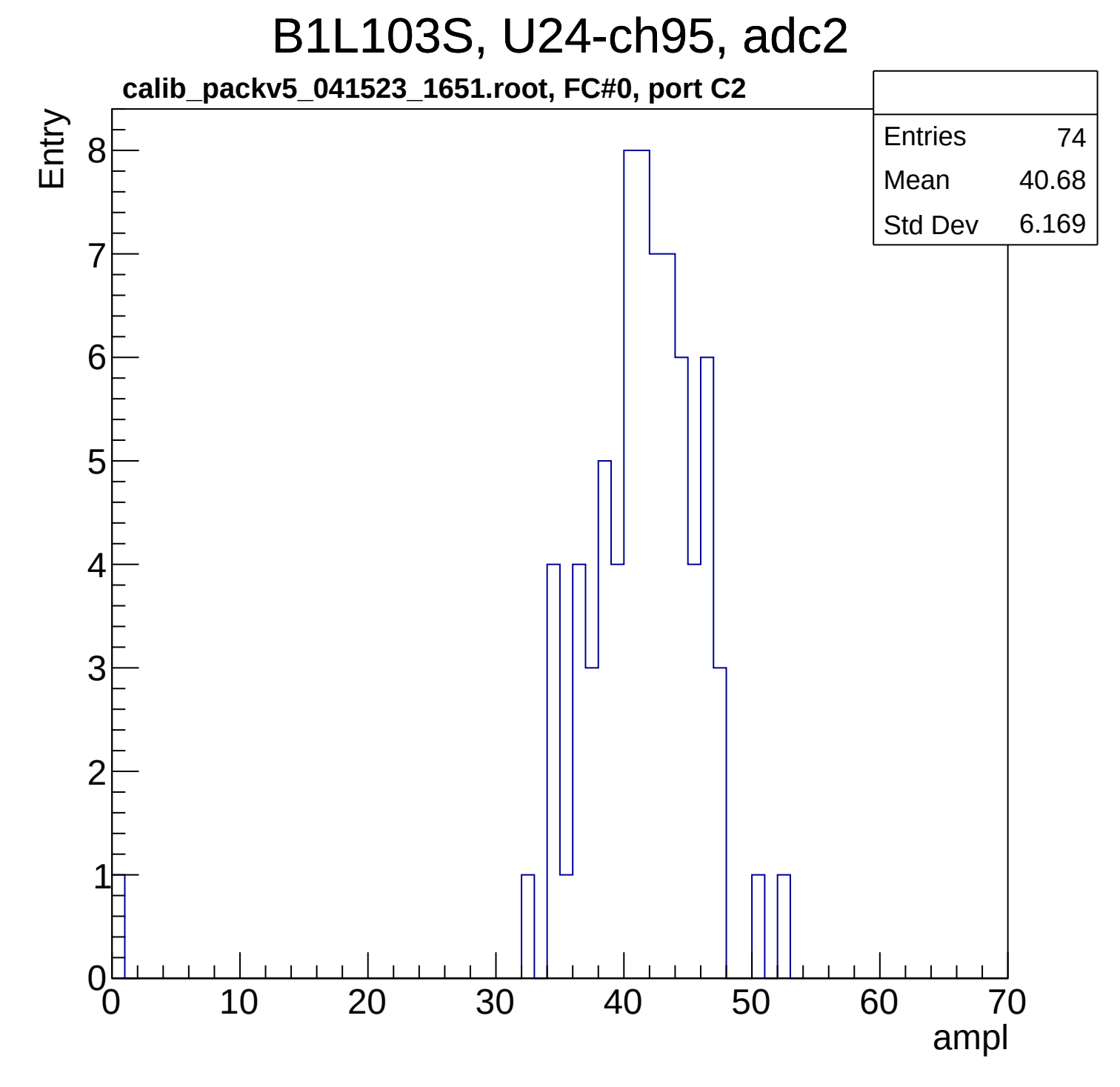
B1L103S, U24-ch95, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 40.68
Std Dev 6.169
Entry
ampl
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2
3
4
5
6
7
8
0
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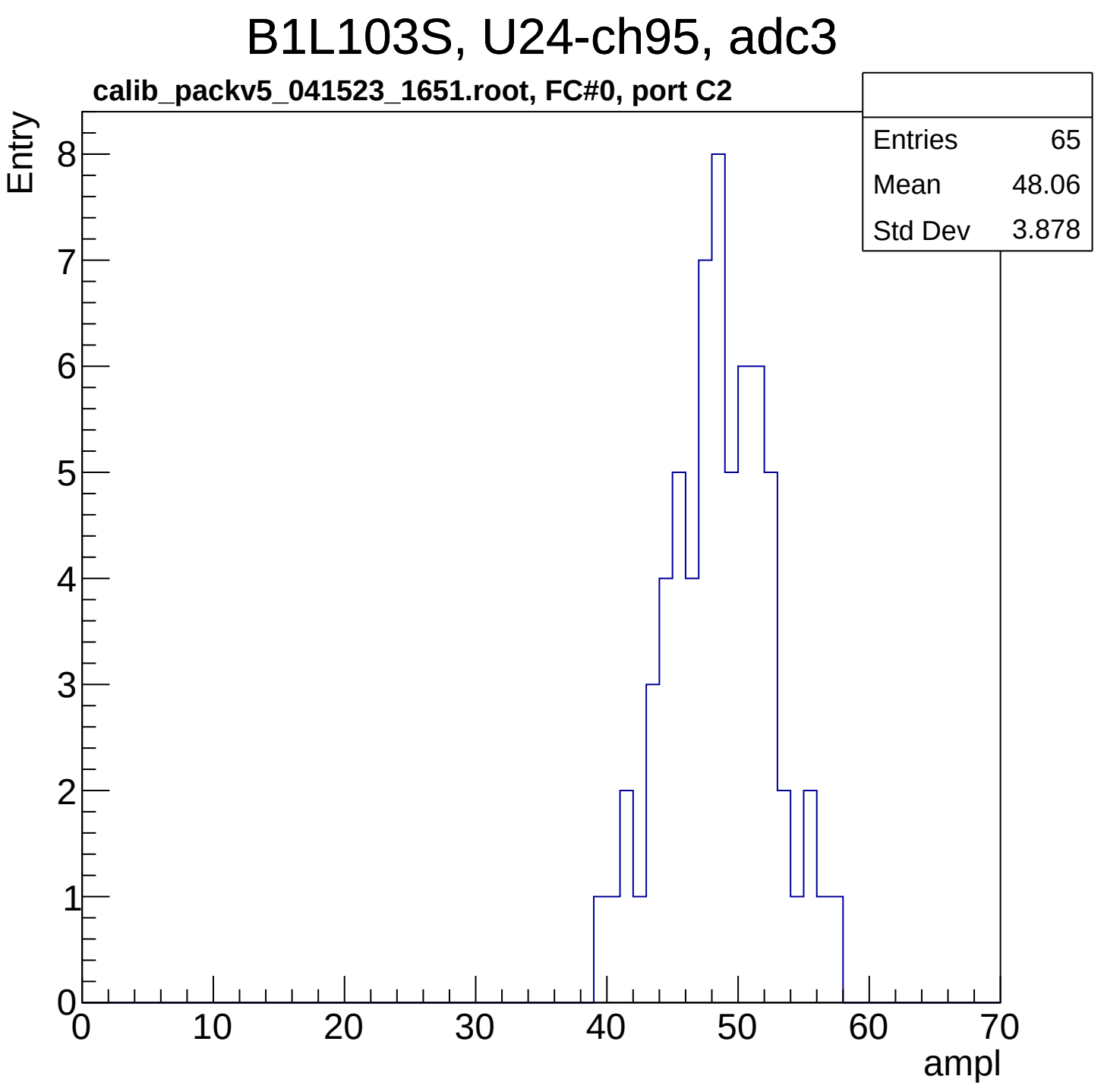
B1L103S, U24-ch95, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 48.06
Std Dev 3.878
Entry
ampl
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2
3
4
5
6
7
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0
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60
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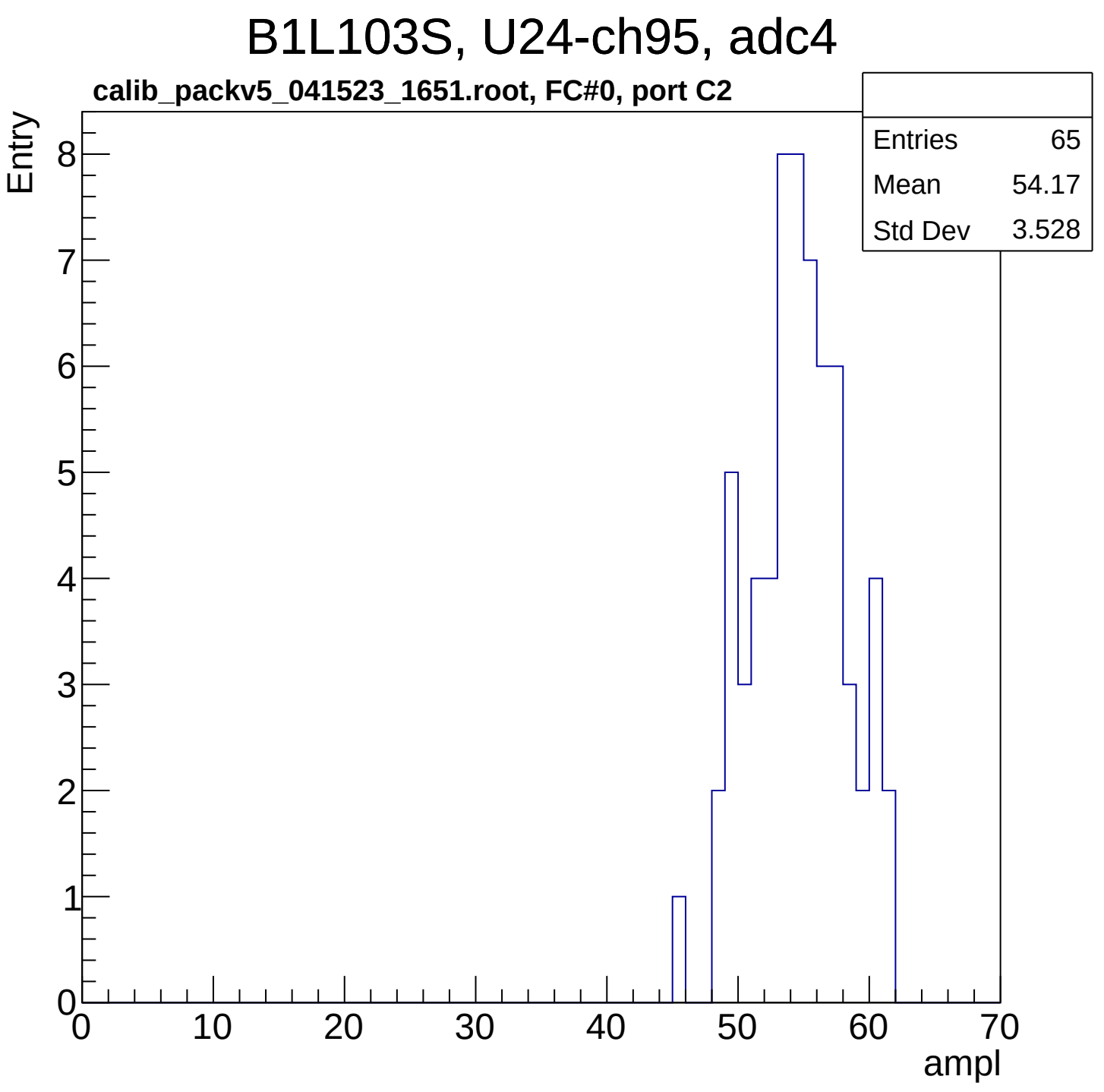
B1L103S, U24-ch95, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 54.17
Std Dev 3.528
Entry
ampl
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2
3
4
5
6
7
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0
10
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40
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60
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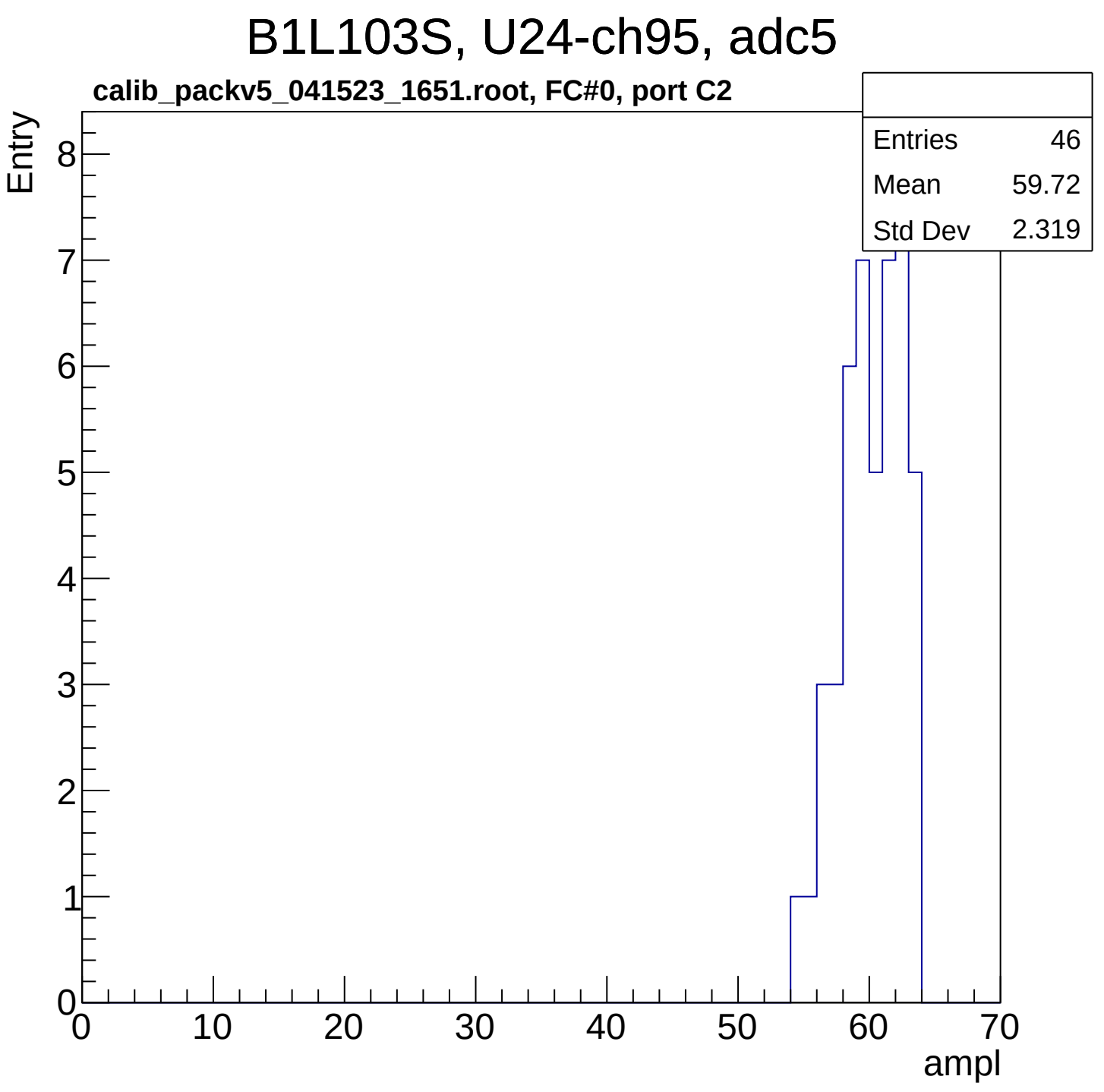
B1L103S, U24-ch95, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 59.72
Std Dev 2.319
Entry
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2
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4
5
6
7
8
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10
20
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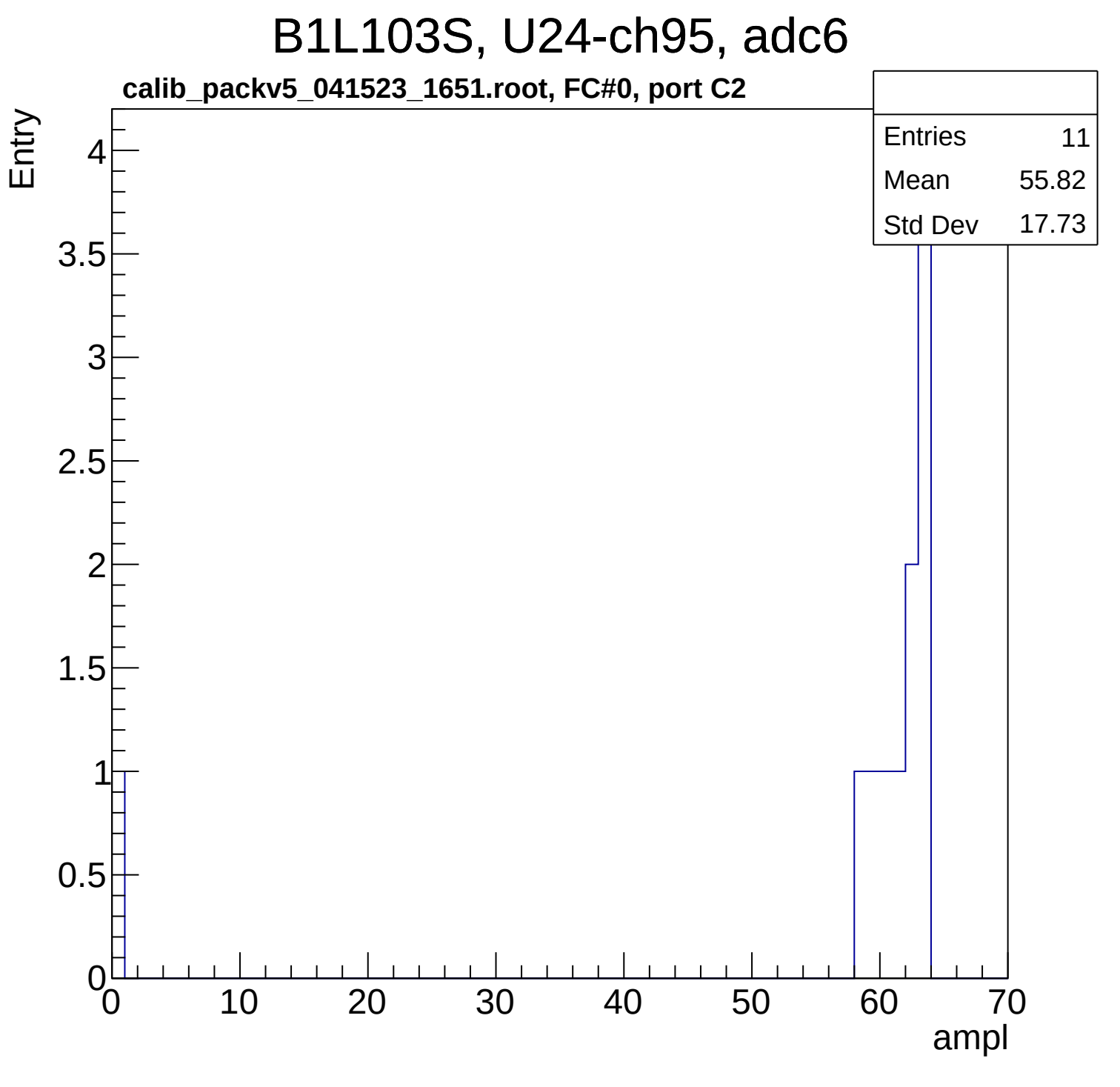
50
60
70
ampl


B1L103S, U24-ch95, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 55.82
Std Dev 17.73
Entry
ampl
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0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
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40
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60
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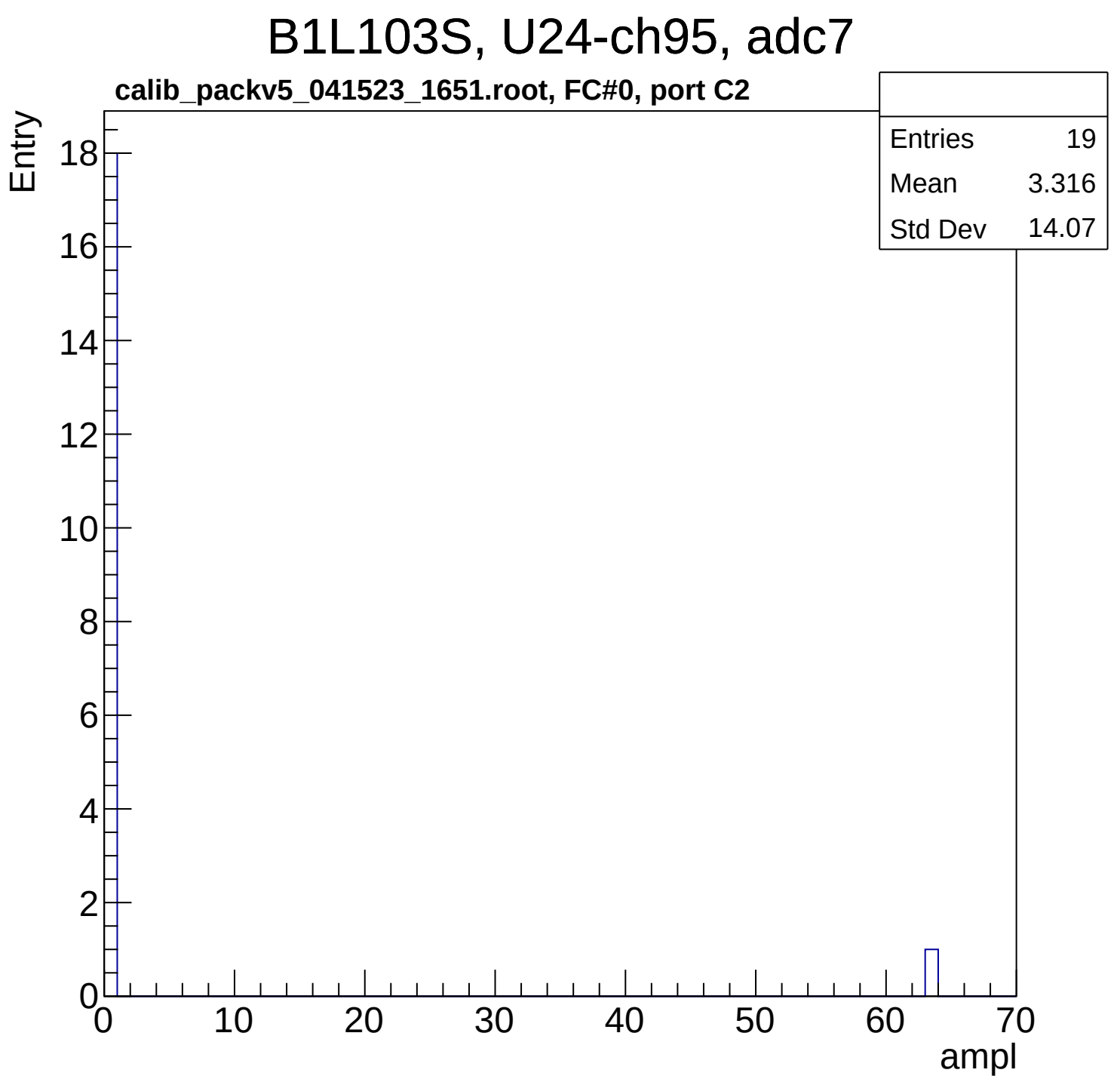
B1L103S, U24-ch95, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 3.316
Std Dev 14.07
Entry
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6
8
10
12
14
16
18
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10
20
30
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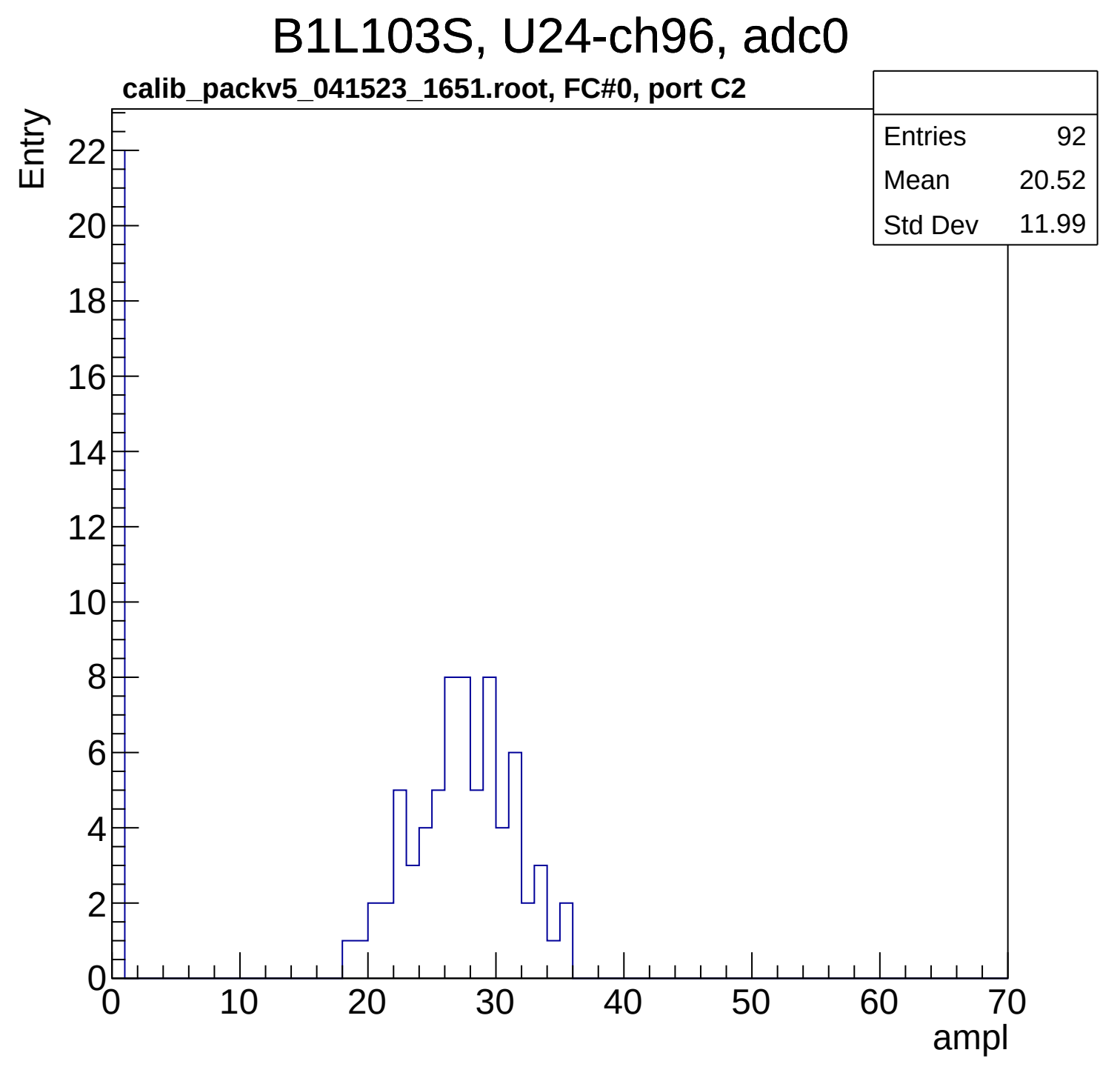
50
60
70
ampl


B1L103S, U24-ch96, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 92
Mean 20.52
Std Dev 11.99
Entry
ampl
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10
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16
18
20
22
0
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40
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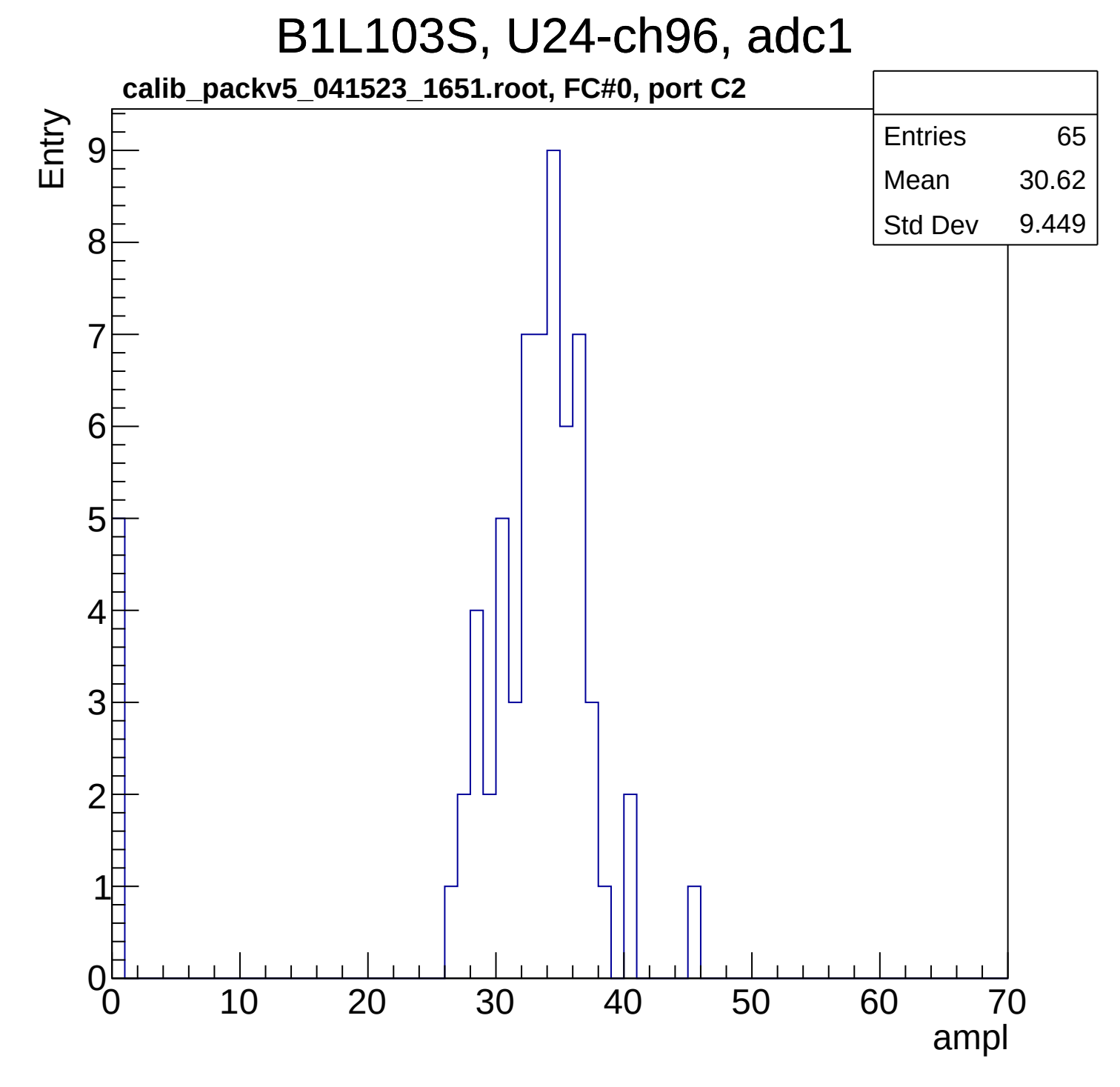
60
70


B1L103S, U24-ch96, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 30.62
Std Dev 9.449
Entry
ampl
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4
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7
8
9
0
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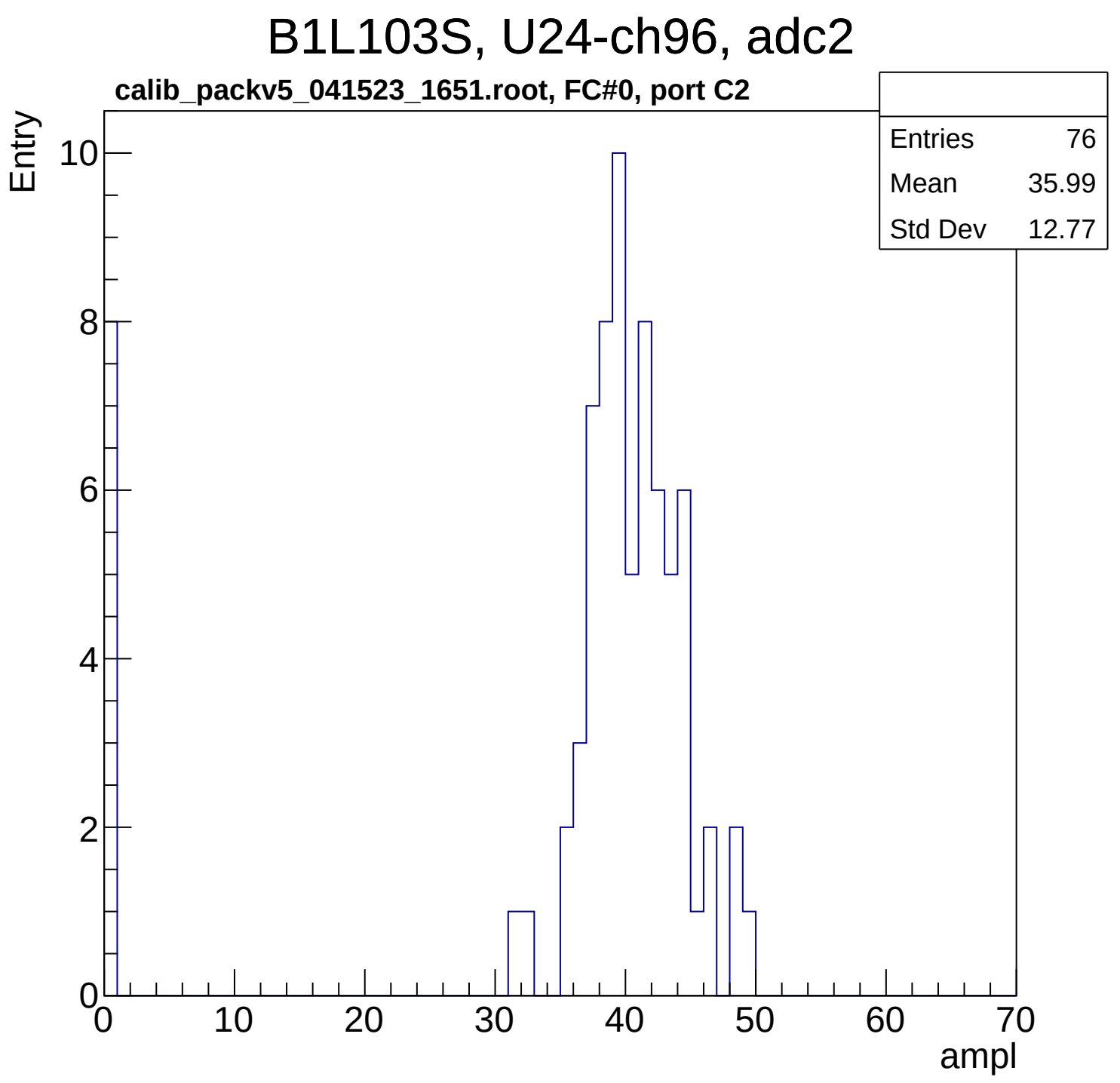
B1L103S, U24-ch96, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 35.99
Std Dev 12.77
Entry
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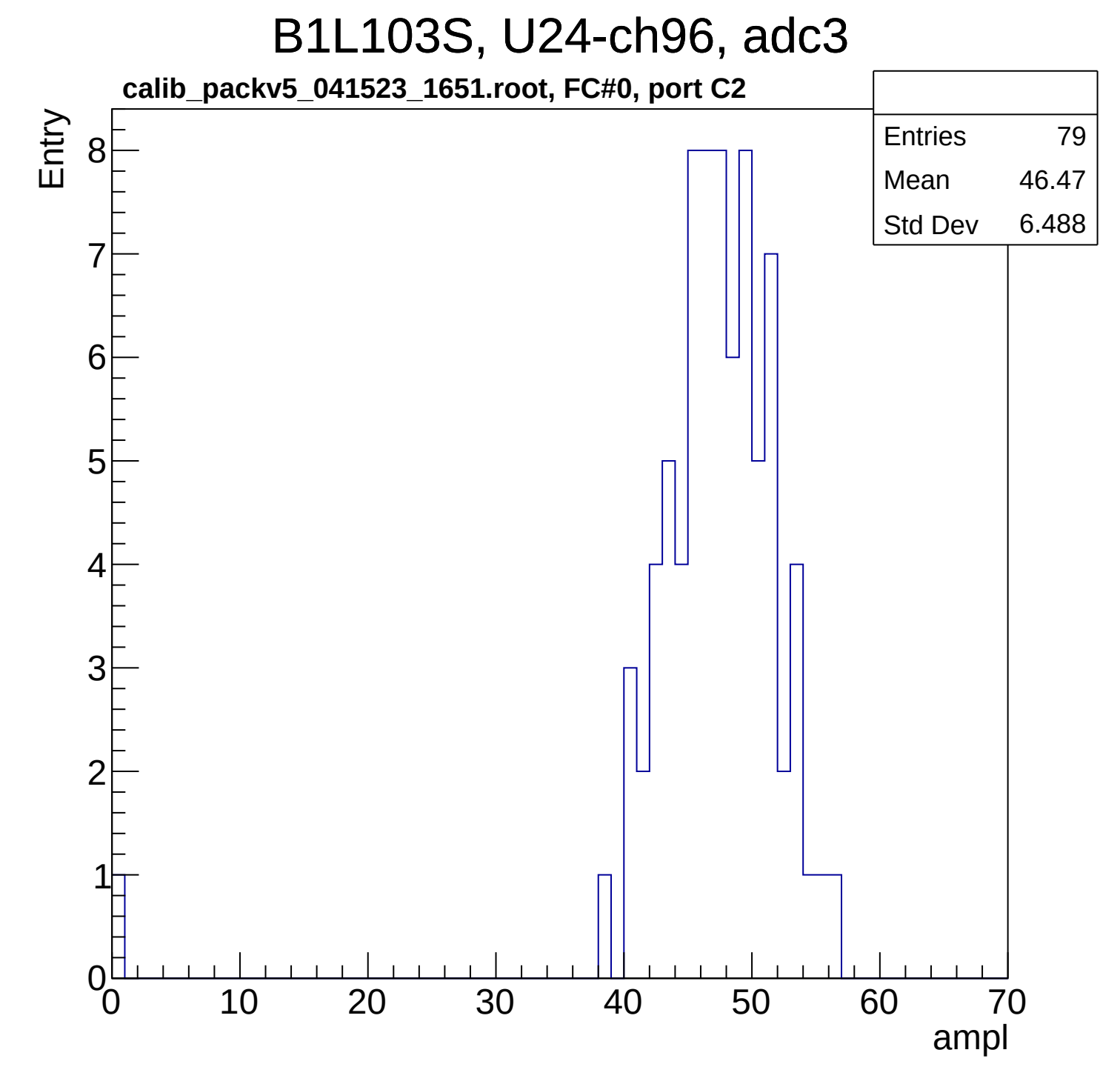
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch96, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 46.47
Std Dev 6.488
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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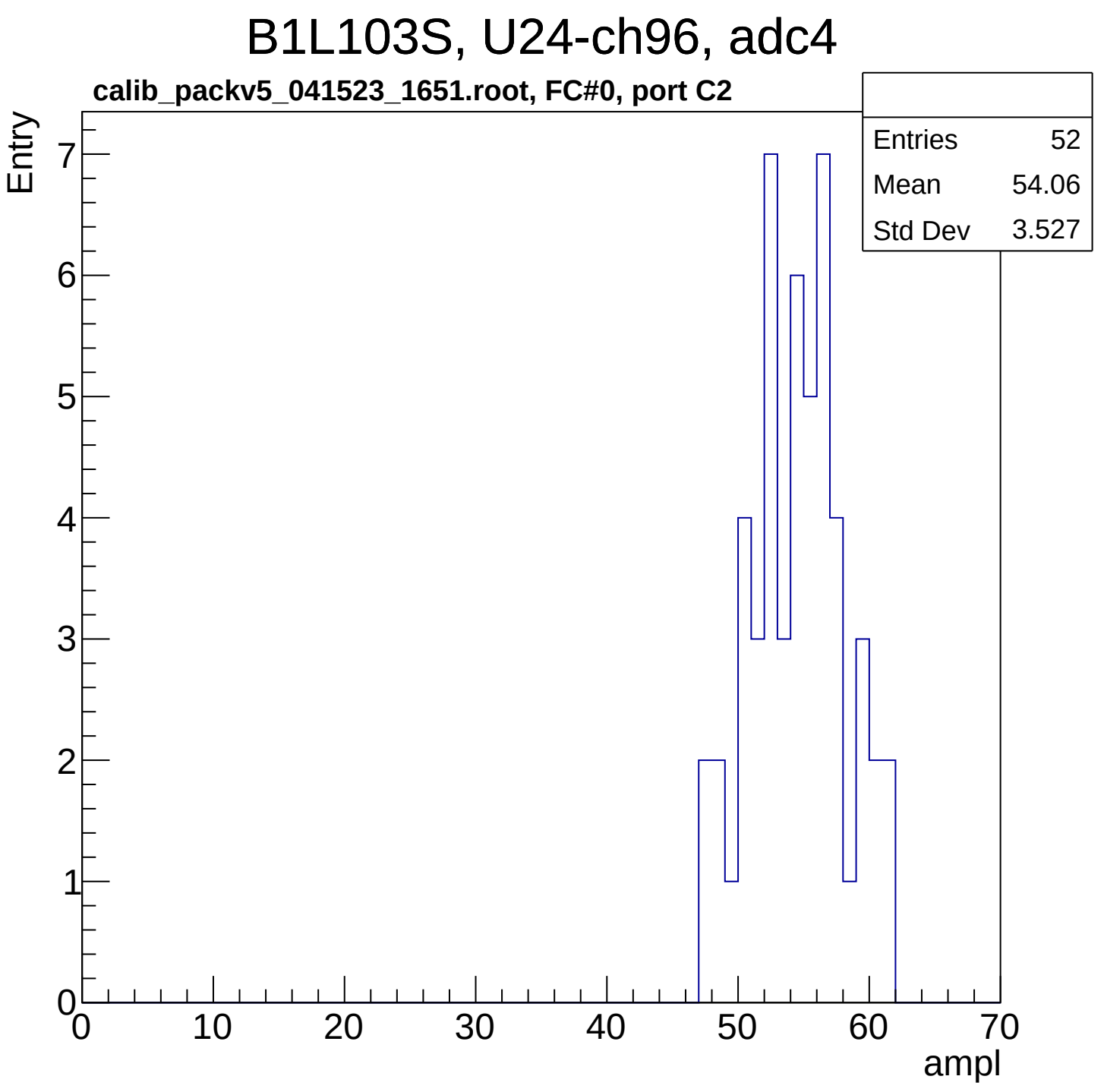
40
50
60
70


B1L103S, U24-ch96, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 54.06
Std Dev 3.527
Entry
ampl
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2
3
4
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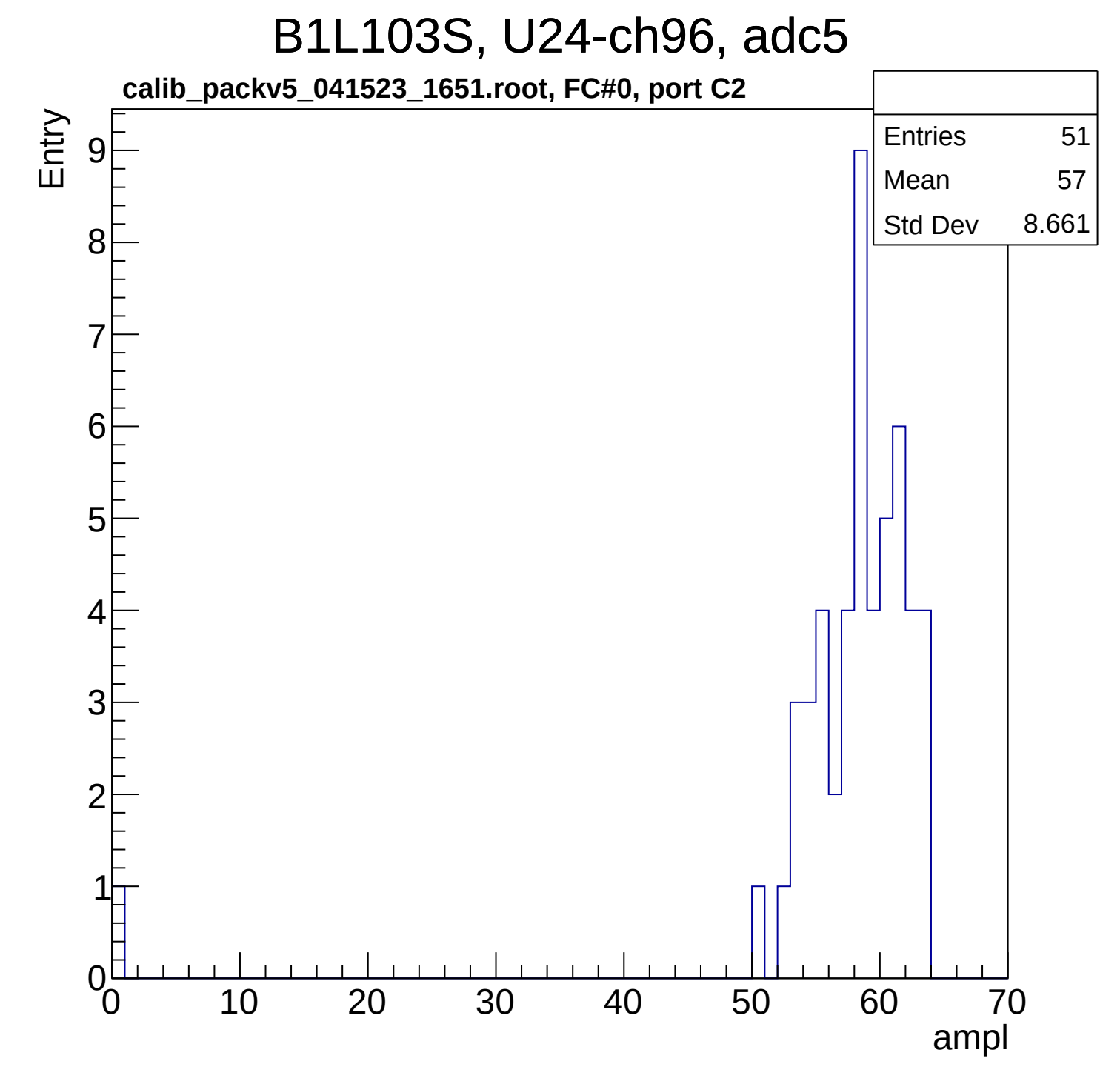
B1L103S, U24-ch96, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 57
Std Dev 8.661
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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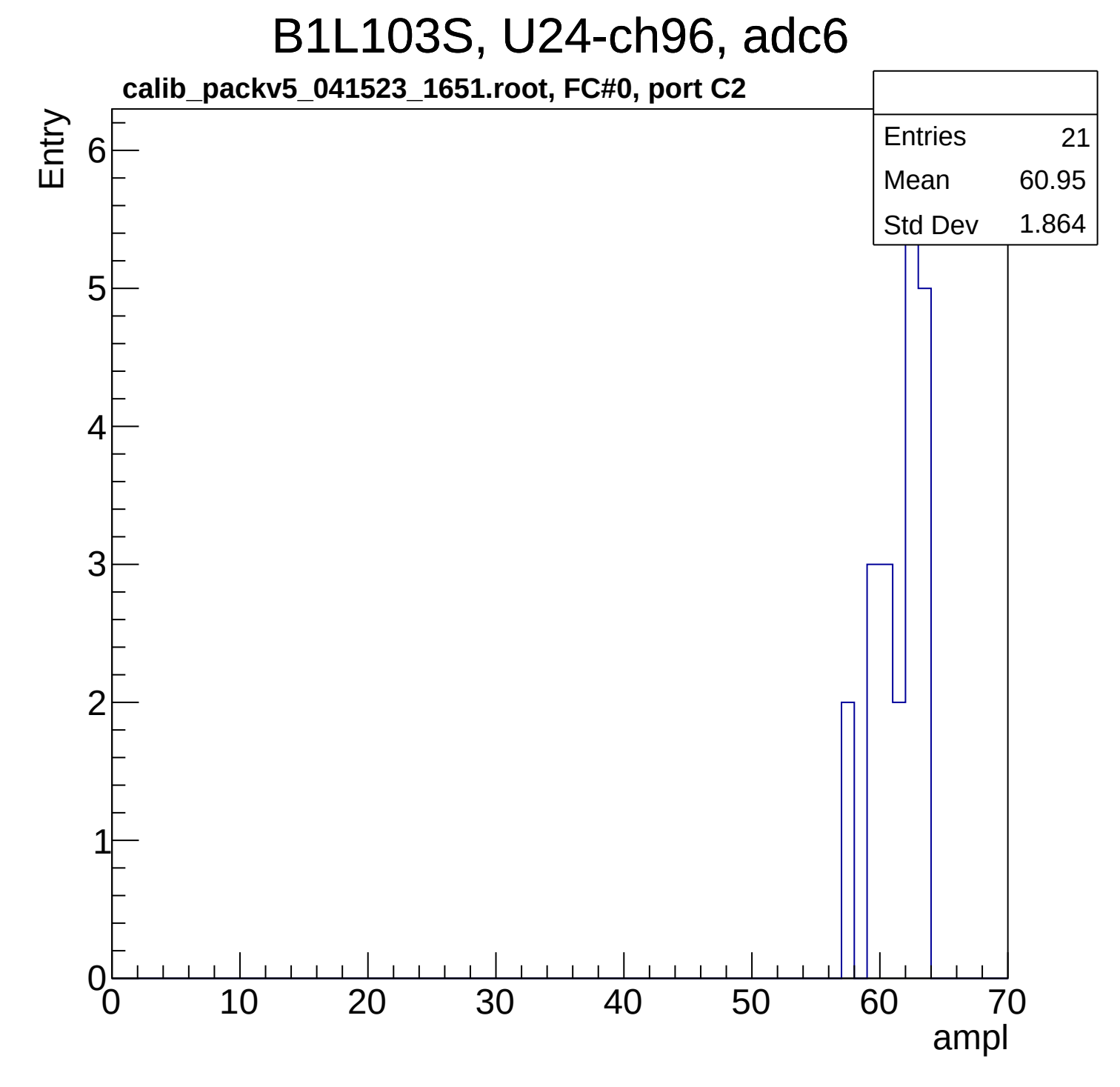
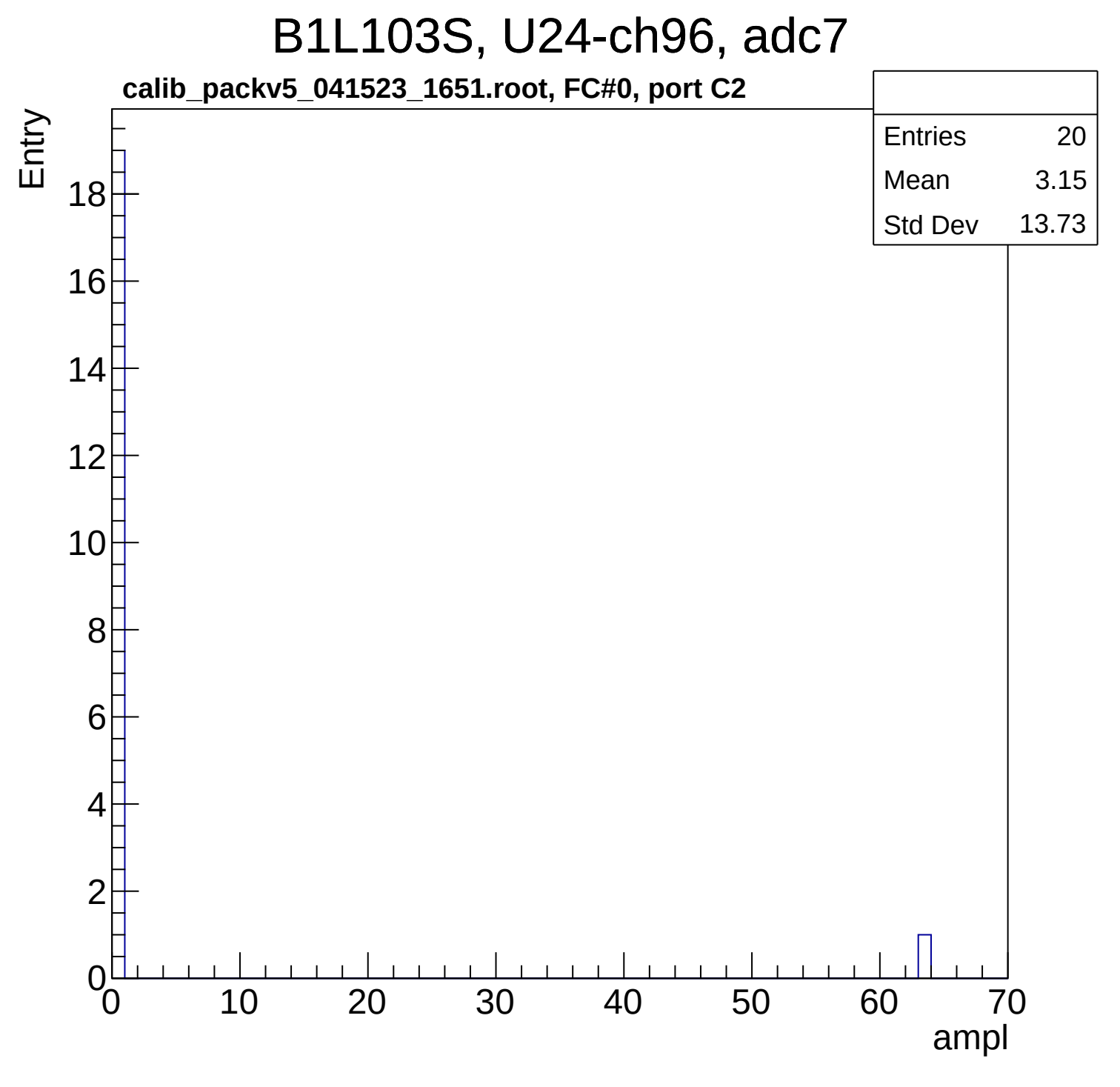

B1L103S, U24-ch96, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 60.95
Std Dev 1.864
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U24-ch96, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
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6
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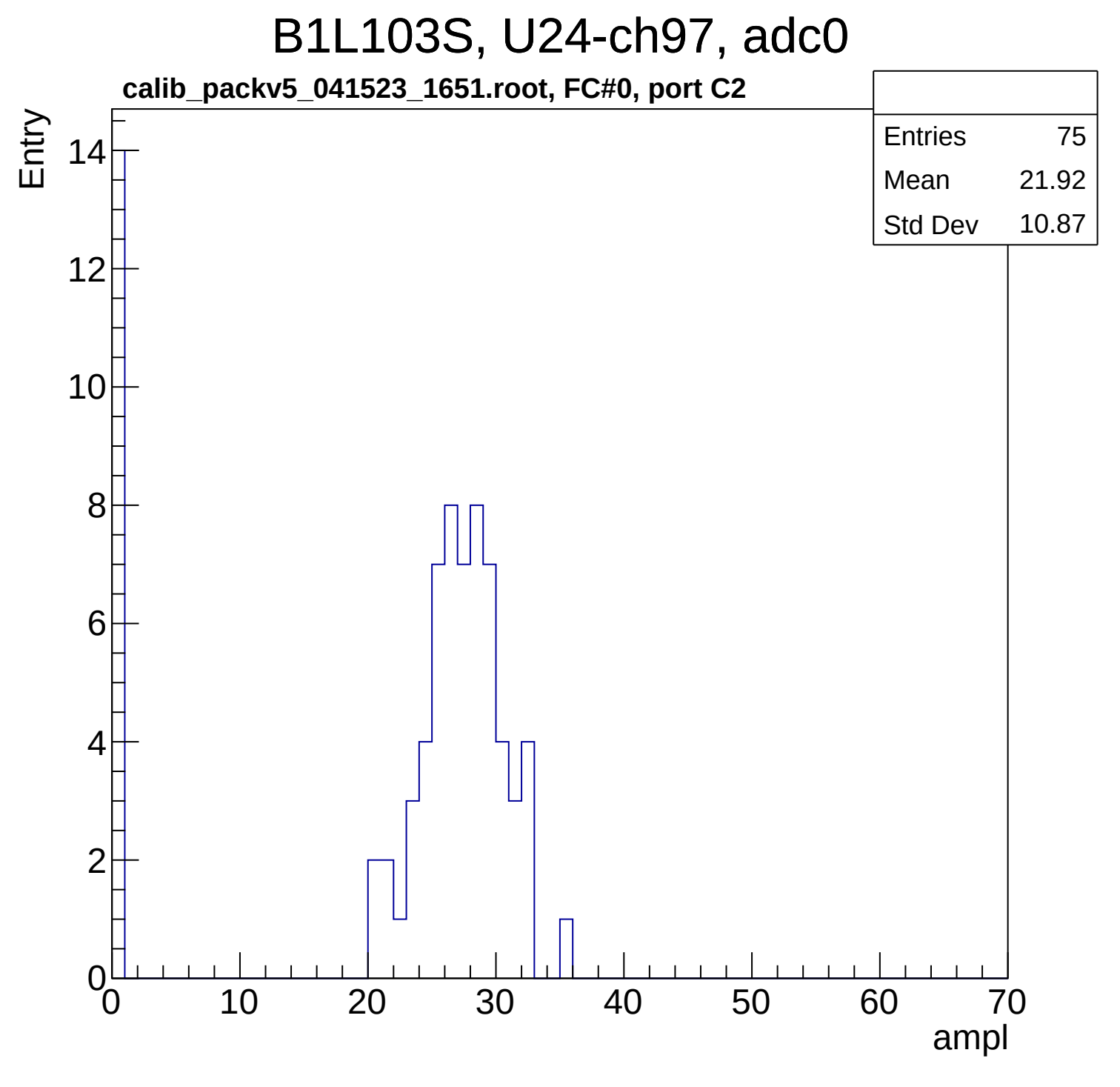
ampl


B1L103S, U24-ch97, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 21.92
Std Dev 10.87
Entry
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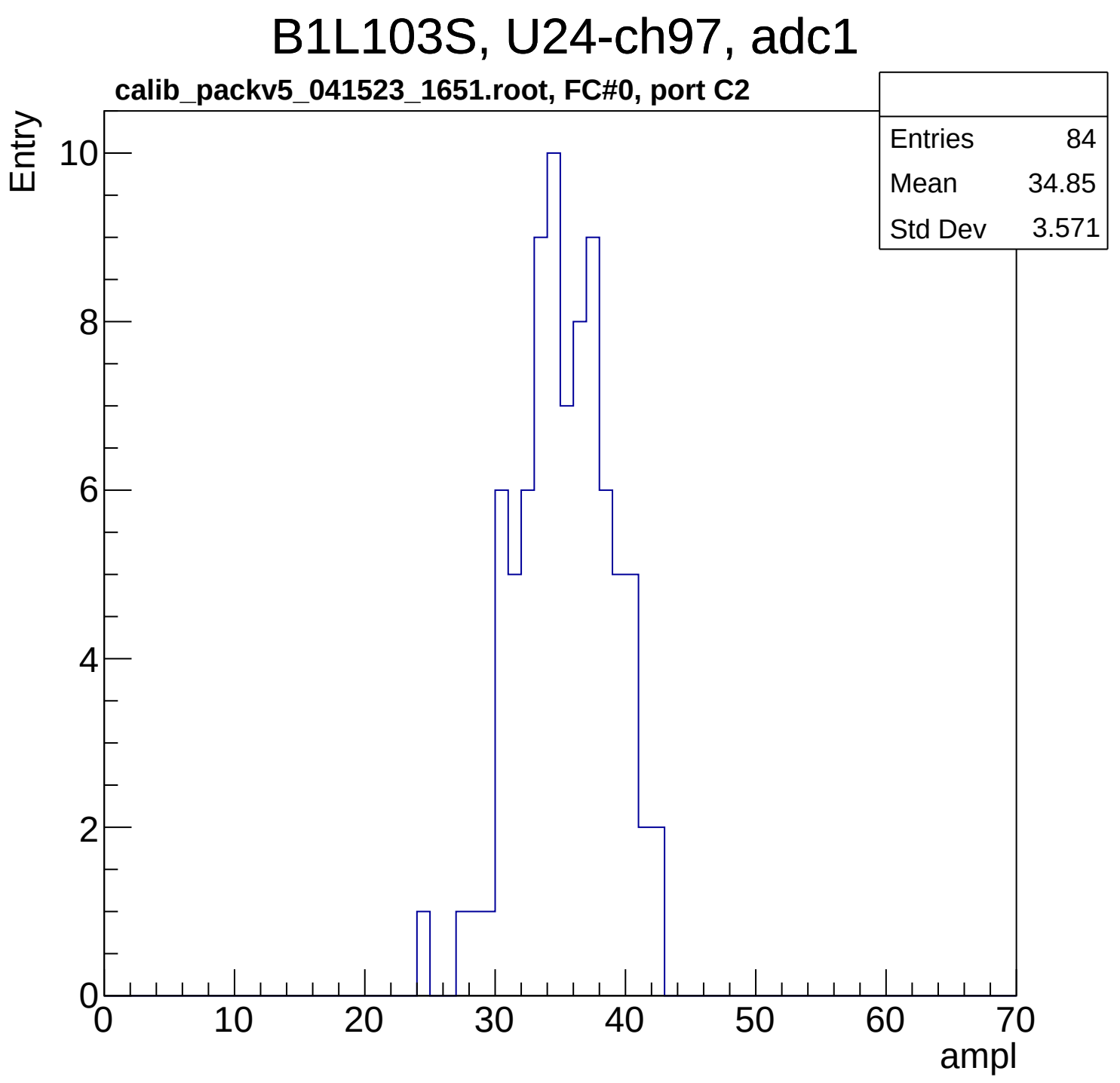
ampl


B1L103S, U24-ch97, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 34.85
Std Dev 3.571
Entry
ampl
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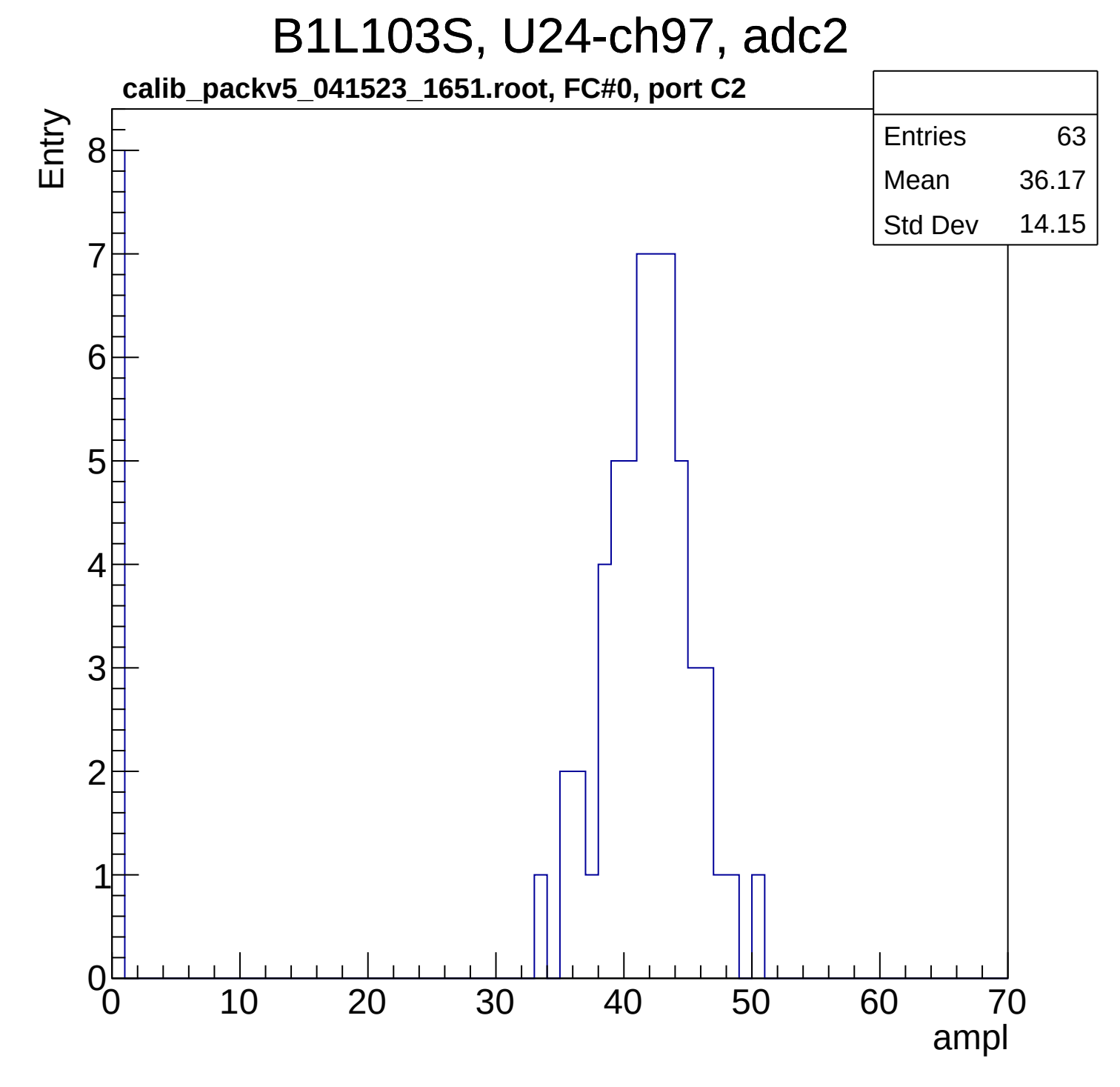
B1L103S, U24-ch97, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 36.17
Std Dev 14.15
Entry
ampl
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0
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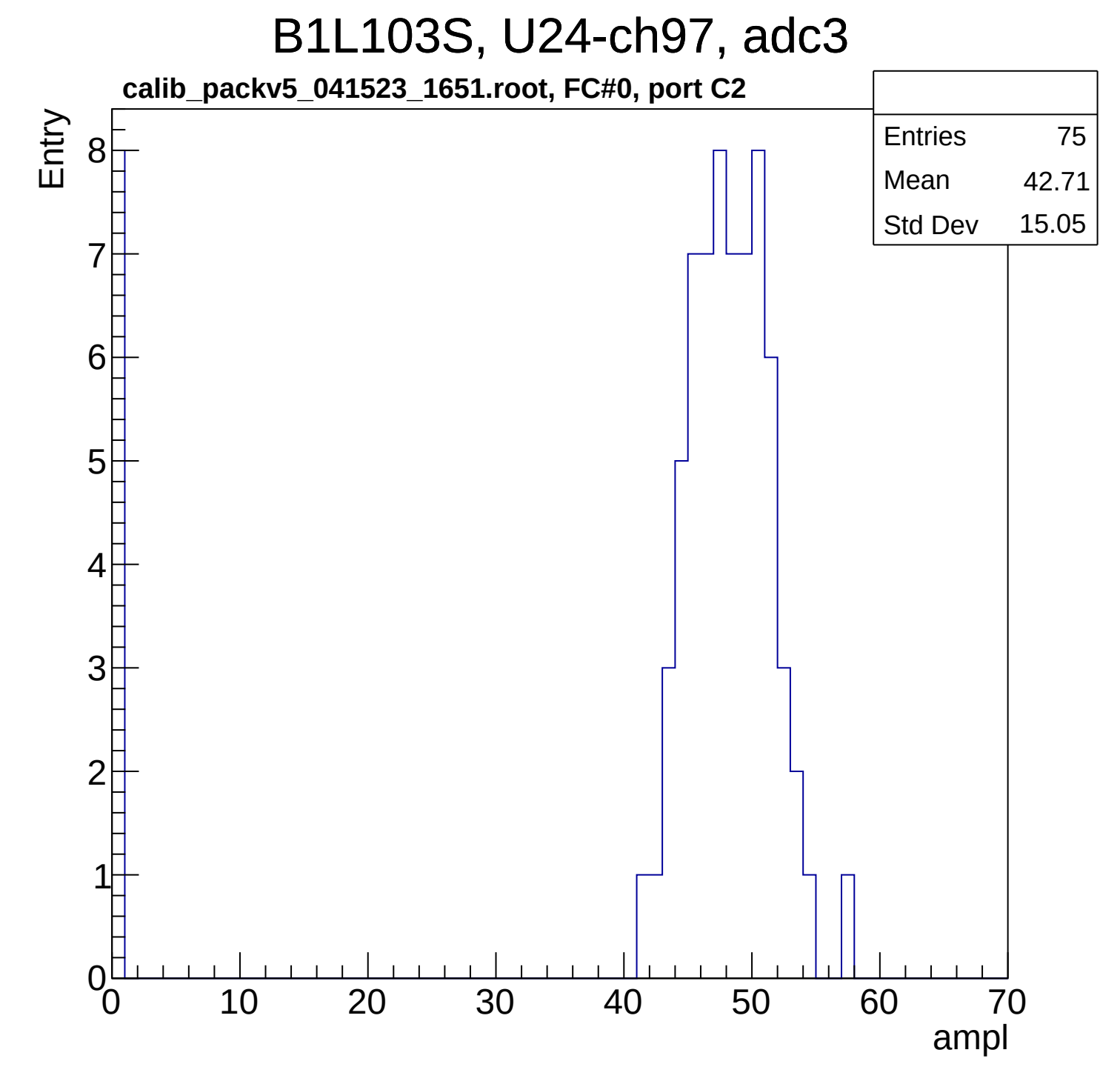
B1L103S, U24-ch97, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 42.71
Std Dev 15.05
Entry
ampl
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4
5
6
7
8
0
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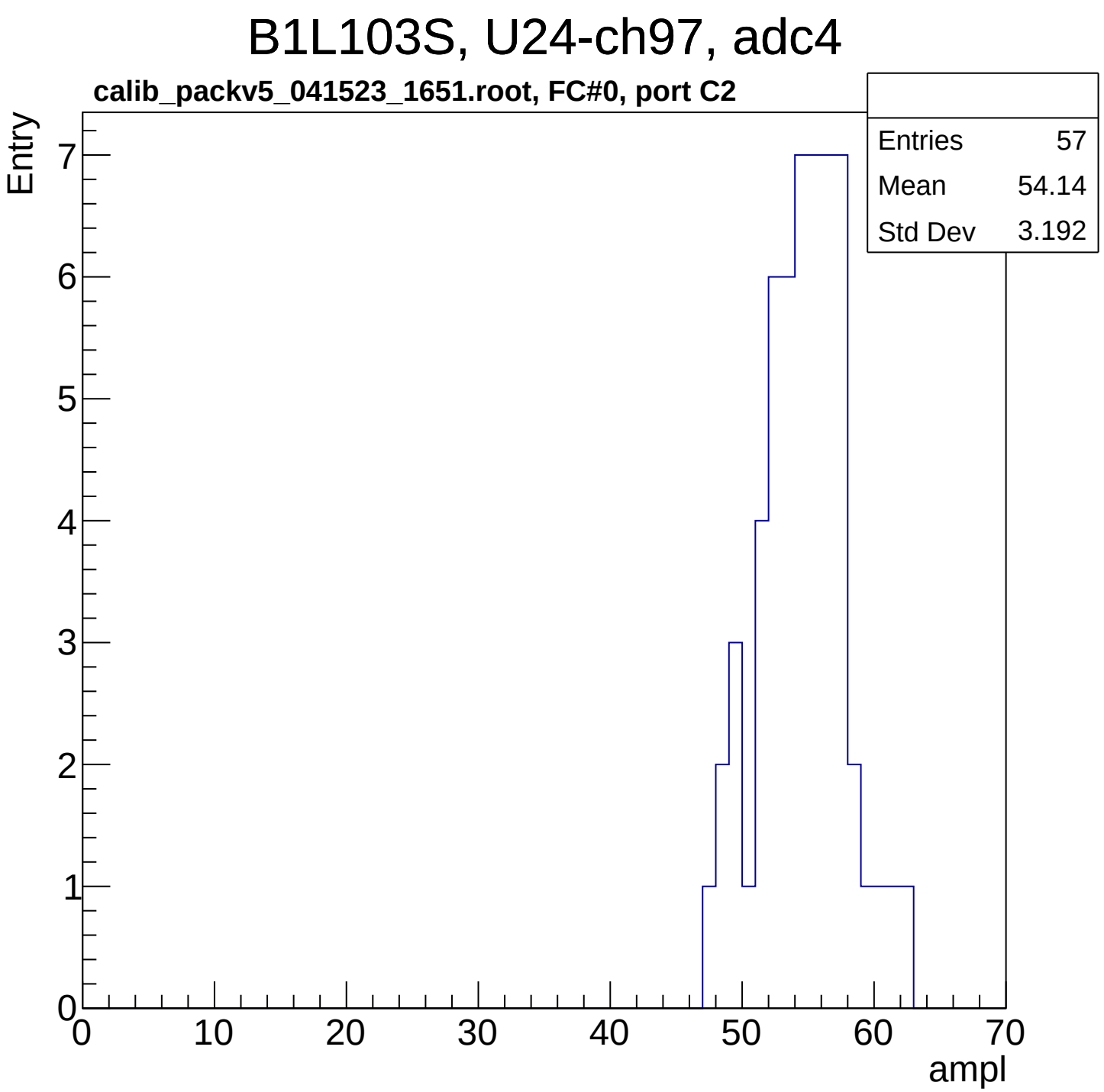
B1L103S, U24-ch97, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 54.14
Std Dev 3.192
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
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40
50
60
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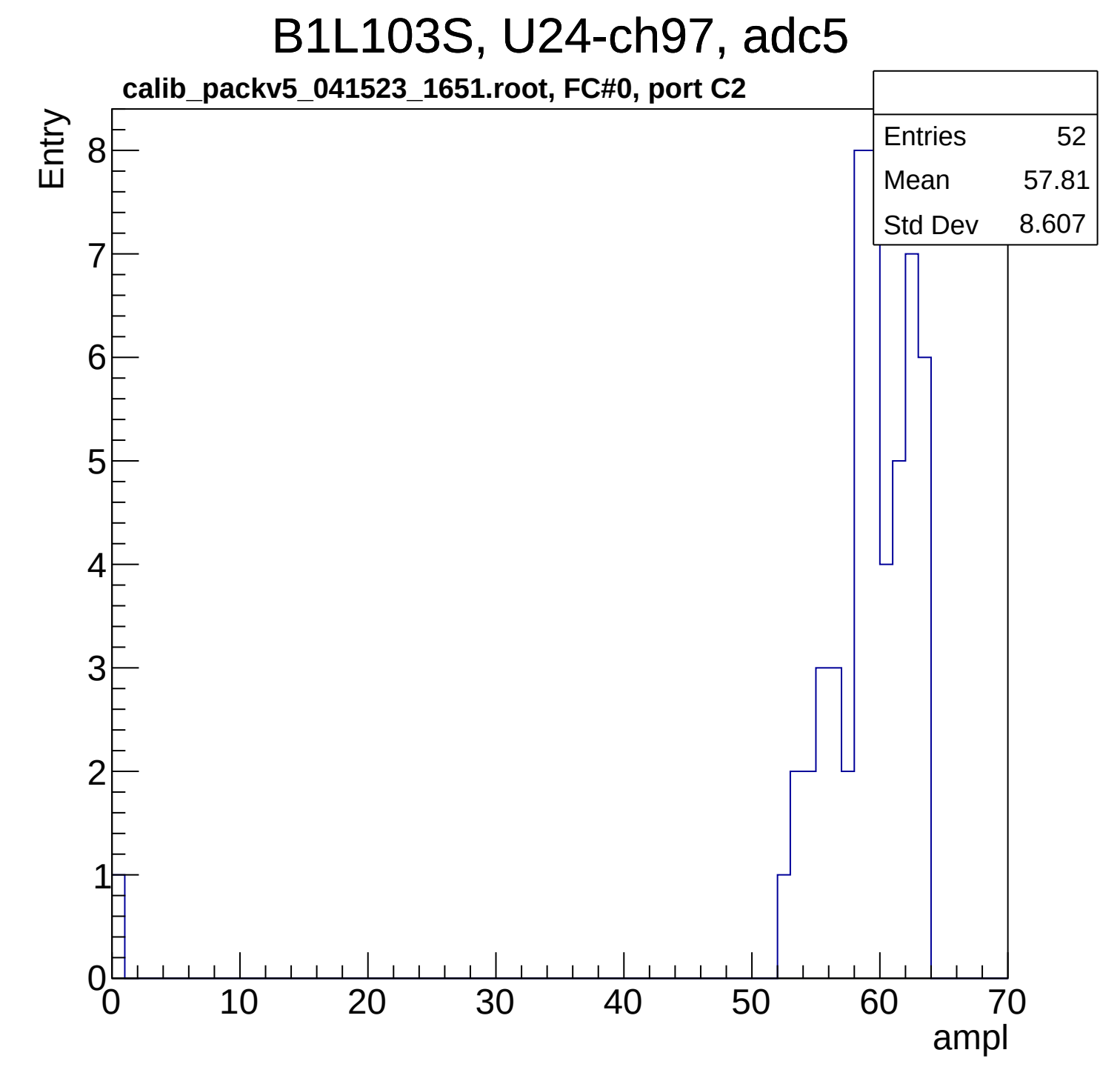
B1L103S, U24-ch97, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 57.81
Std Dev 8.607
Entry
ampl
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7
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0
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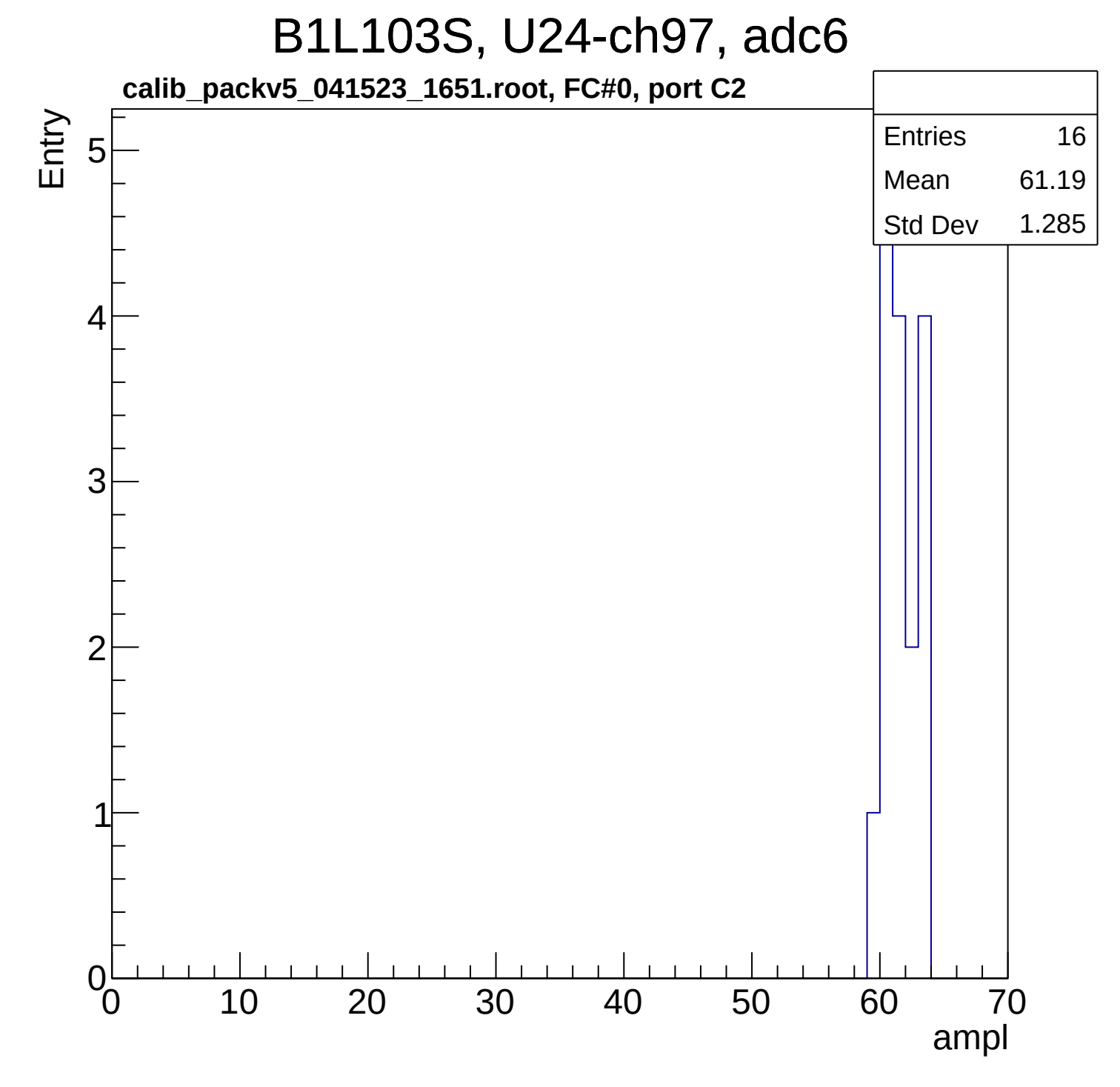
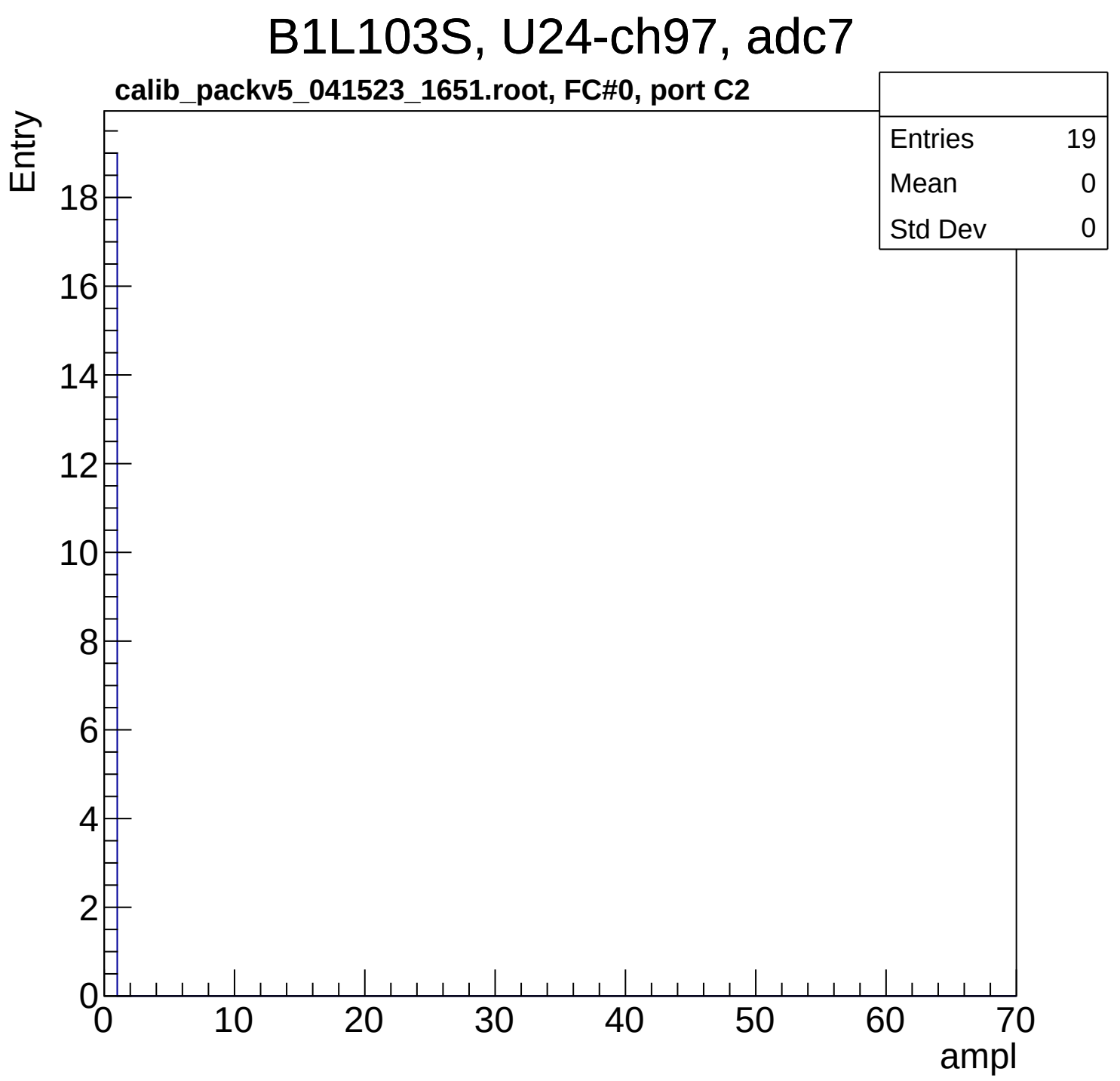
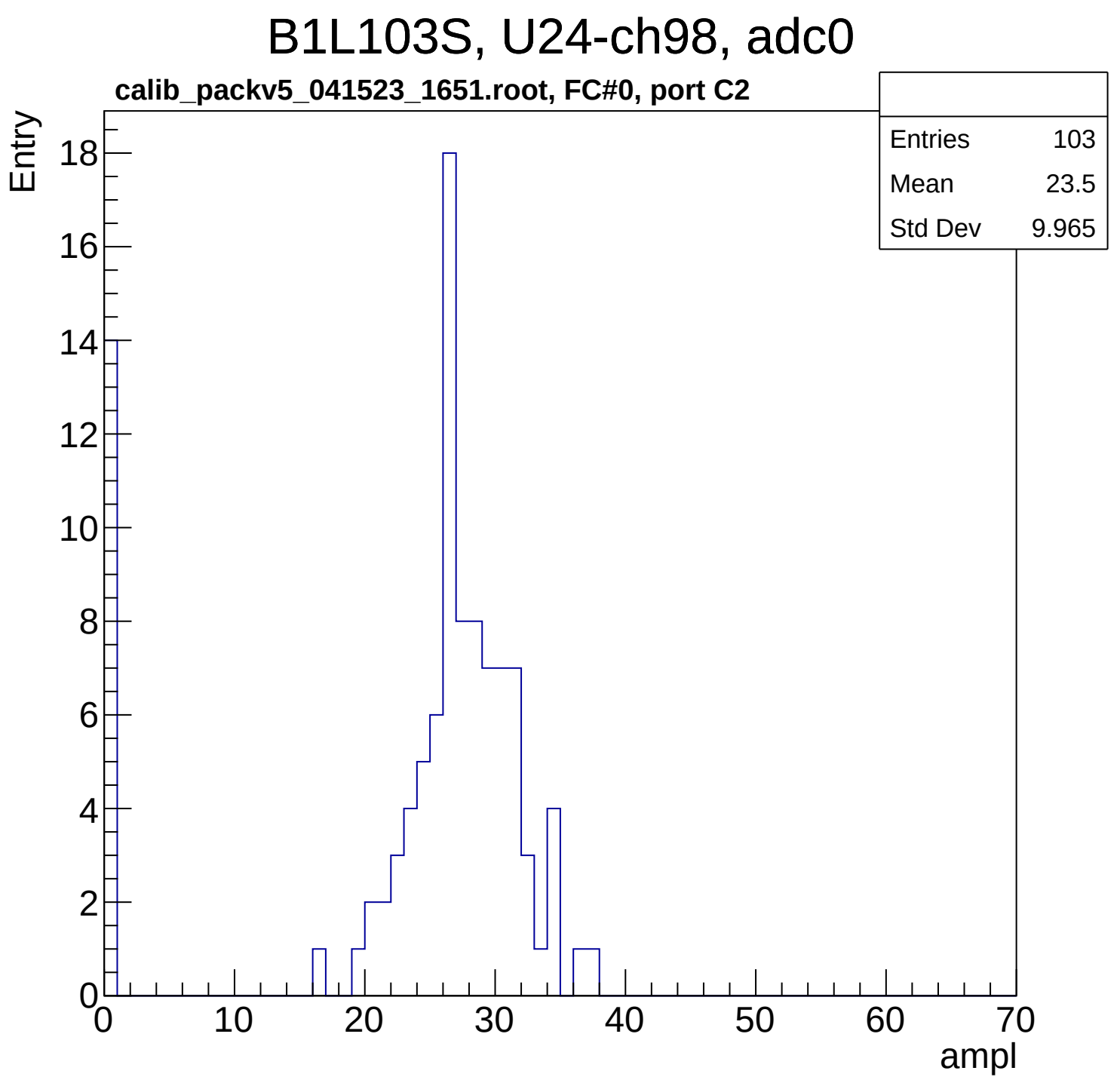

B1L103S, U24-ch97, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 16
Mean 61.19
Std Dev 1.285
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch97, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch98, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 103
Mean 23.5
Std Dev 9.965
Entry
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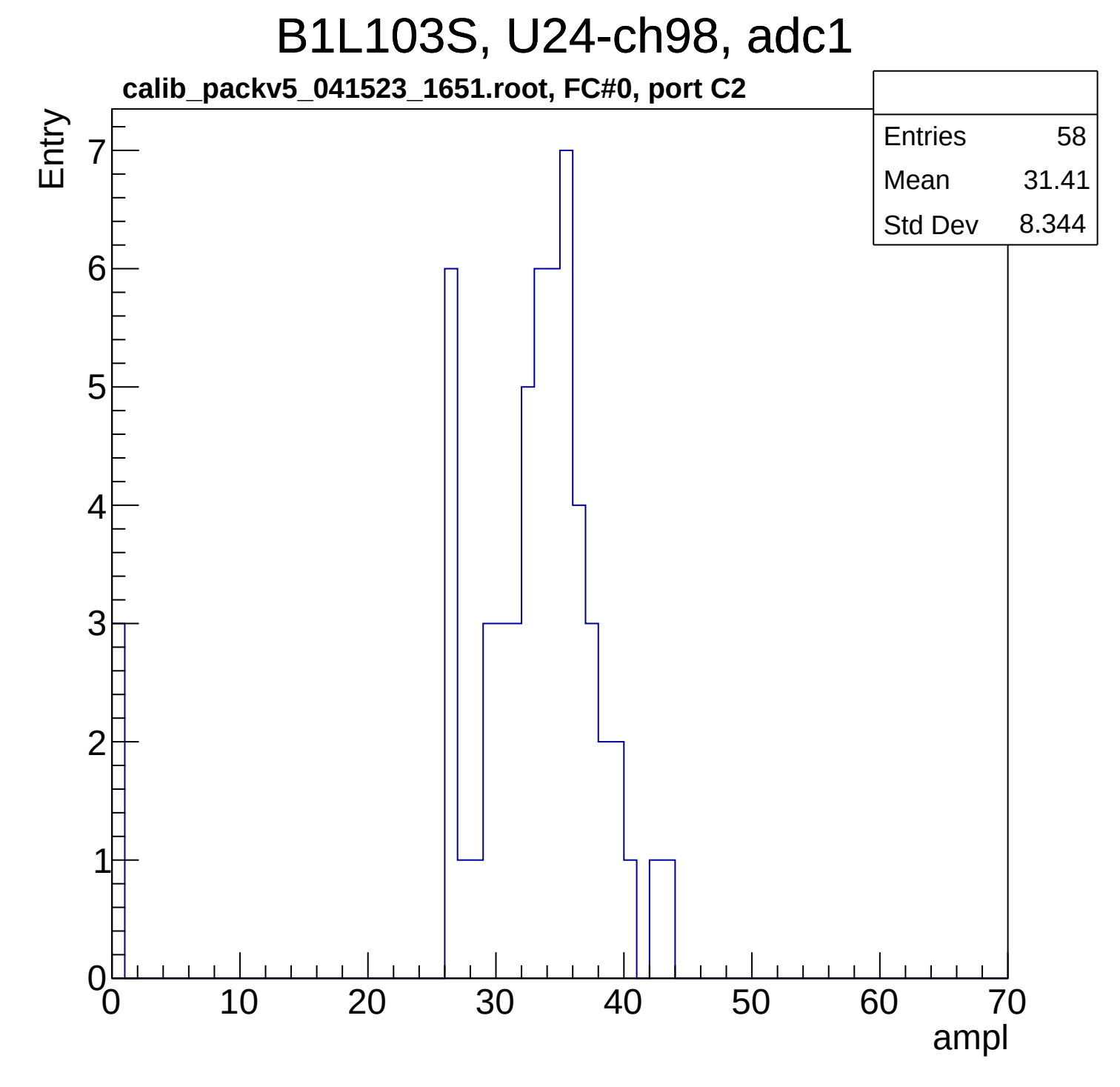
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch98, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 31.41
Std Dev 8.344
Entry
ampl
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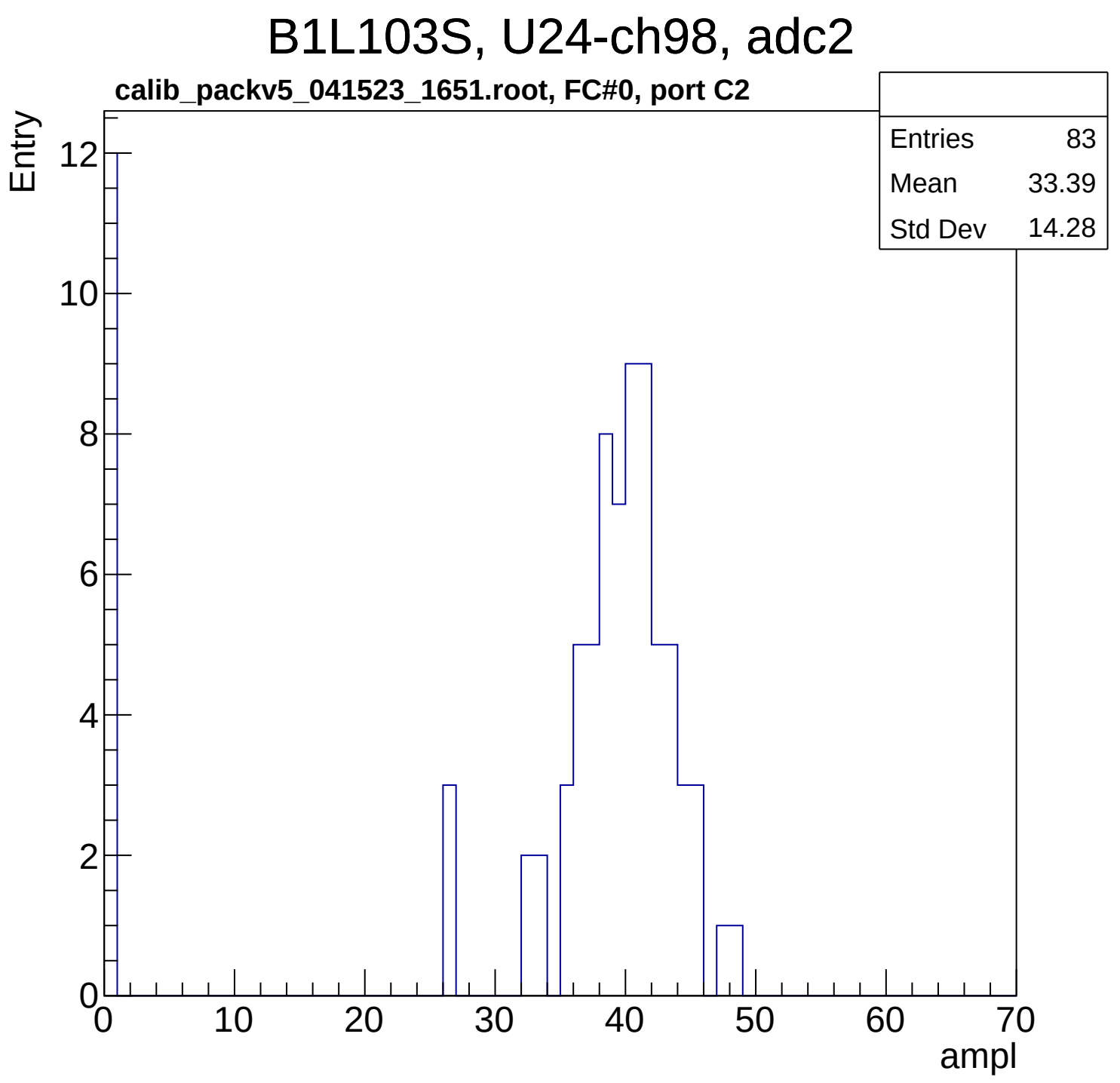
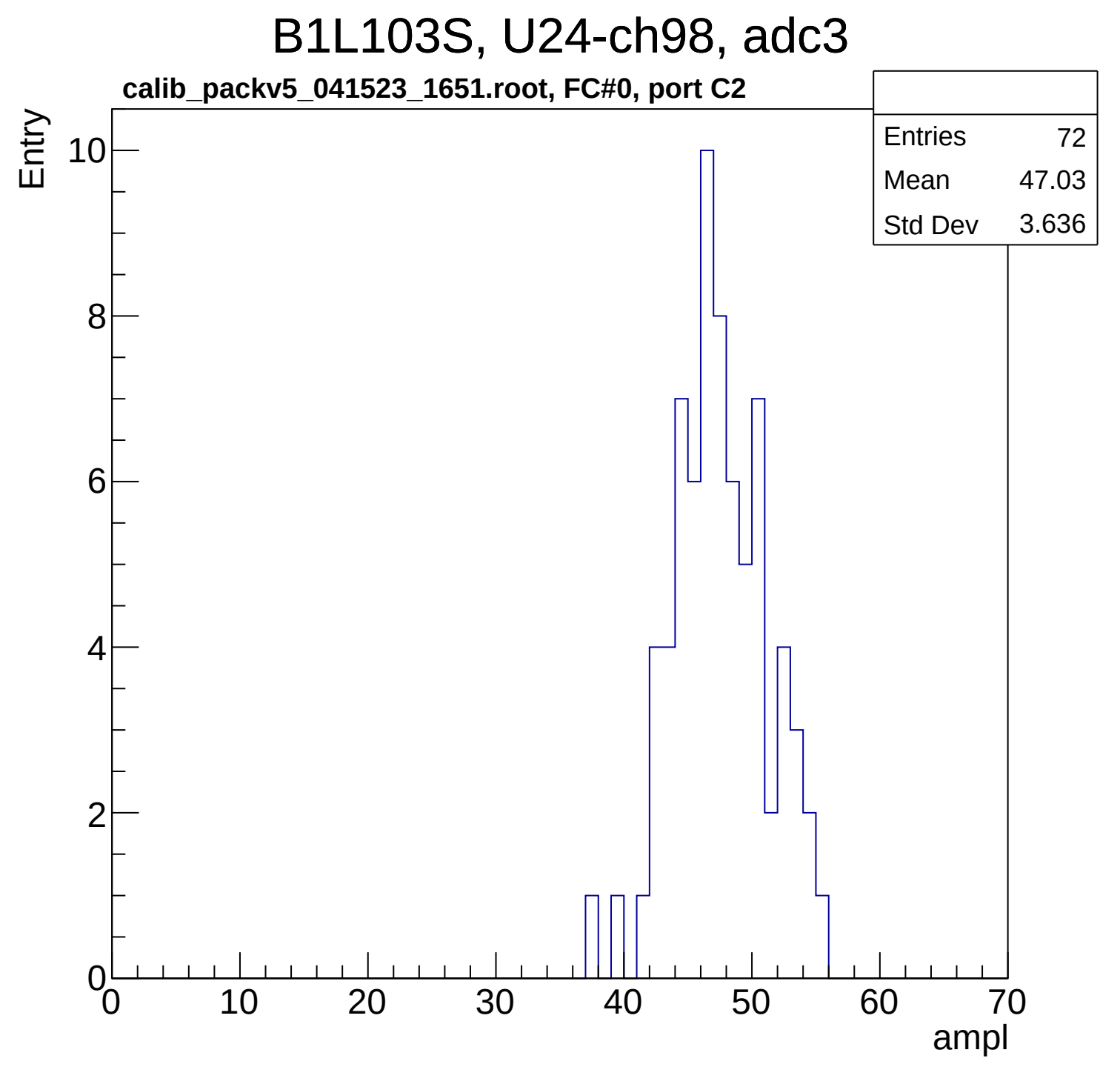
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U24-ch98, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 33.39
Std Dev 14.28
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch98, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 47.03
Std Dev 3.636
Entry
ampl
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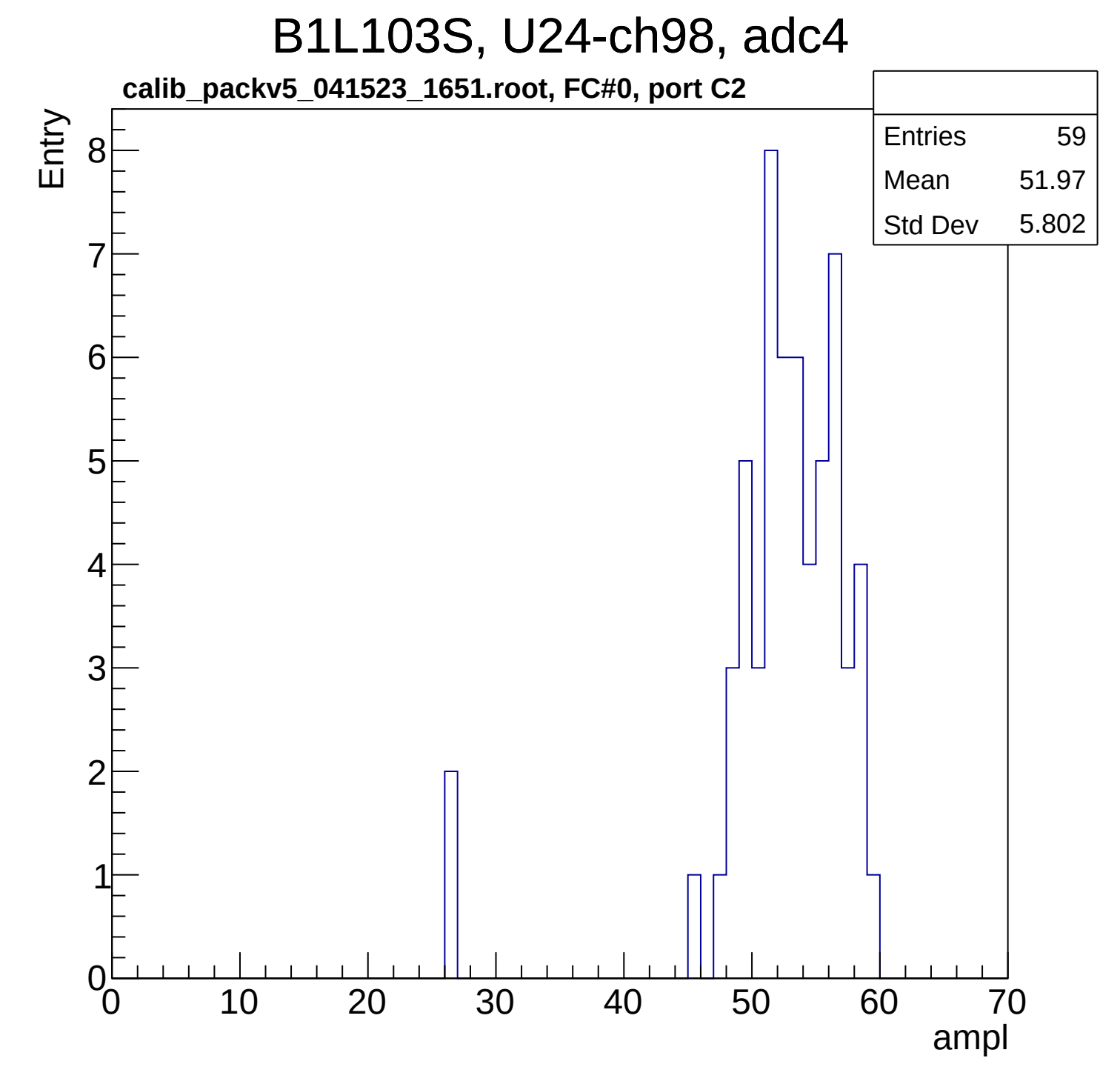
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U24-ch98, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 51.97
Std Dev 5.802
Entry
ampl
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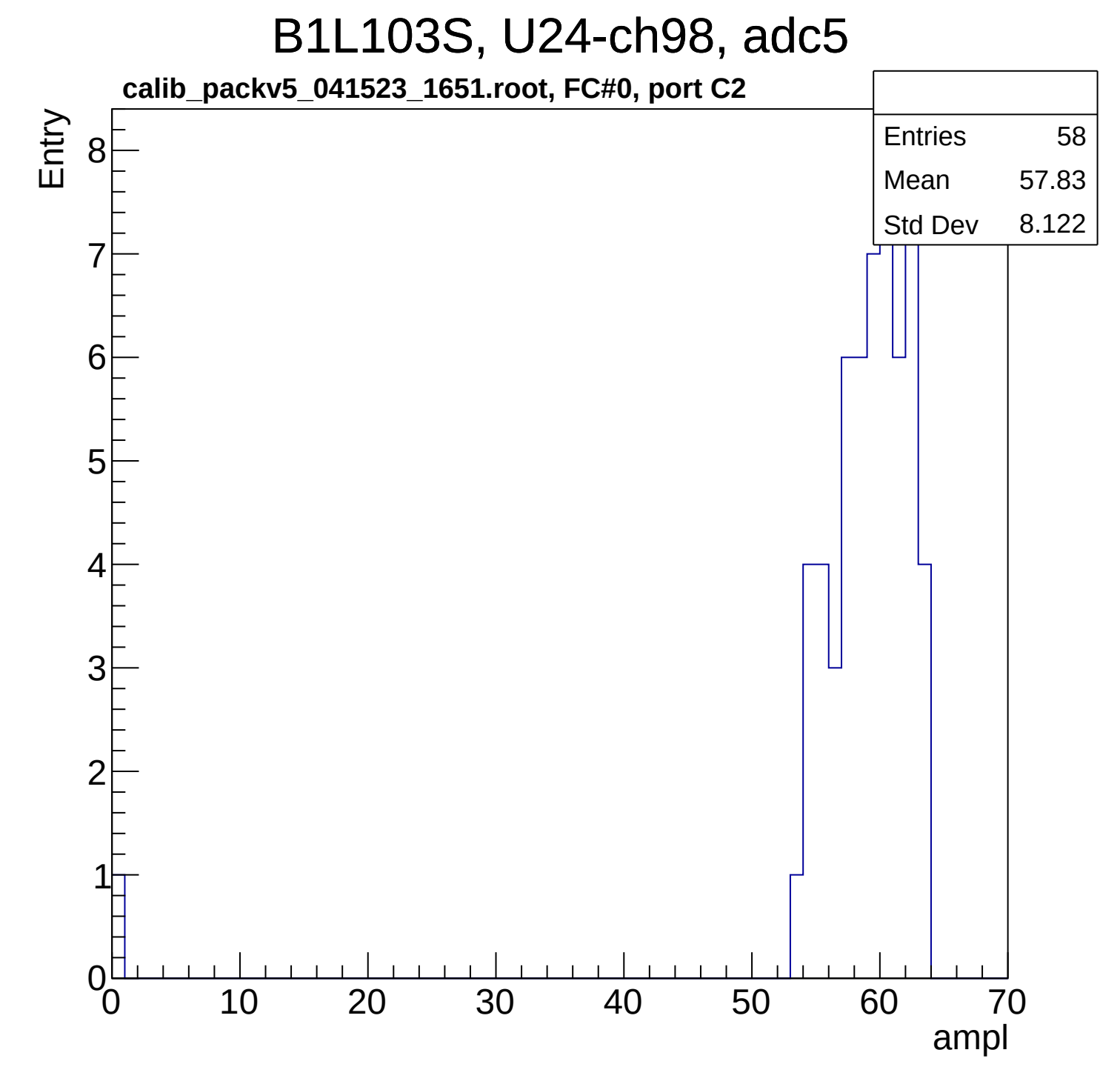
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U24-ch98, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 57.83
Std Dev 8.122
Entry
ampl
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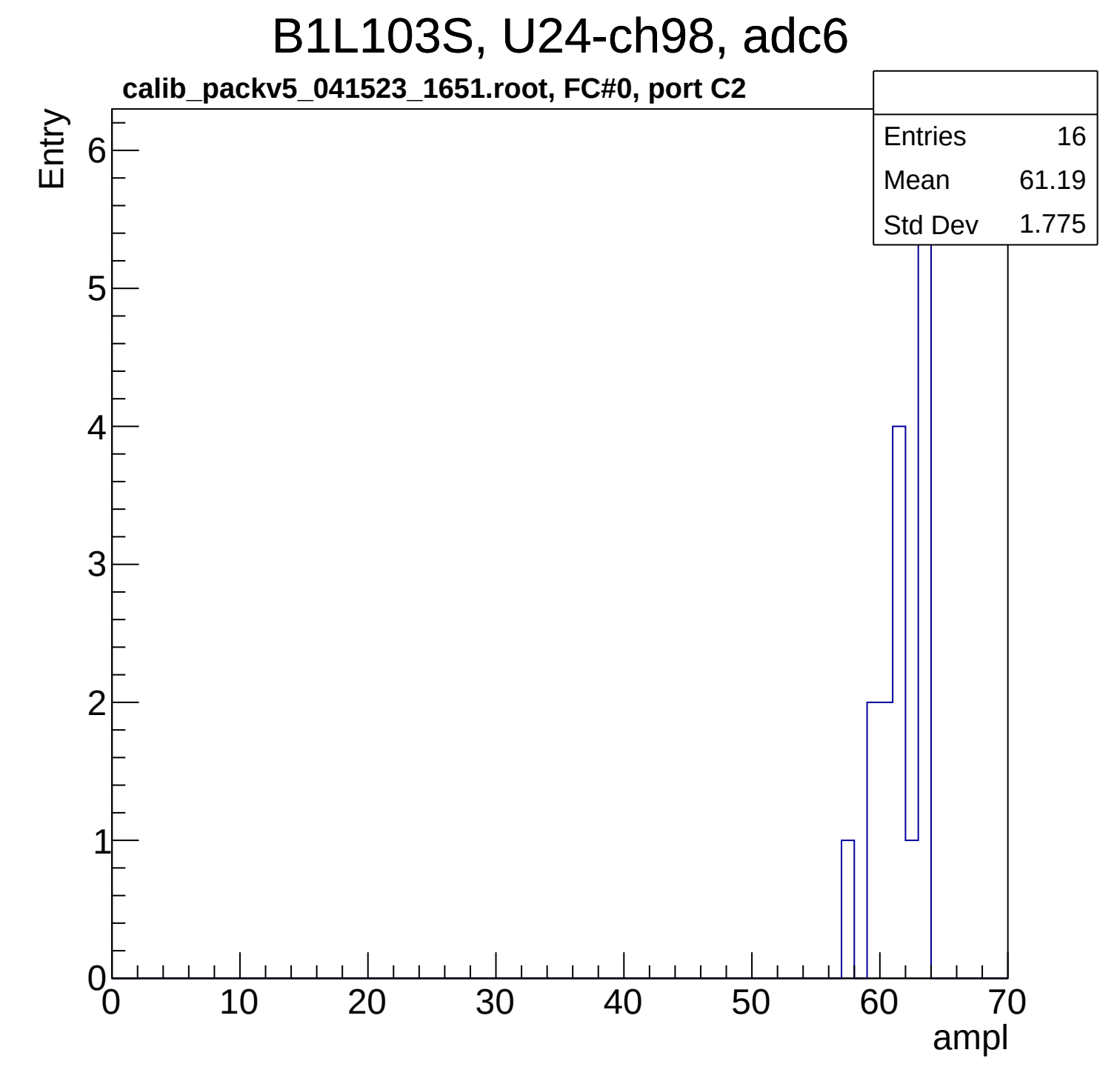
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U24-ch98, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 16
Mean 61.19
Std Dev 1.775
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
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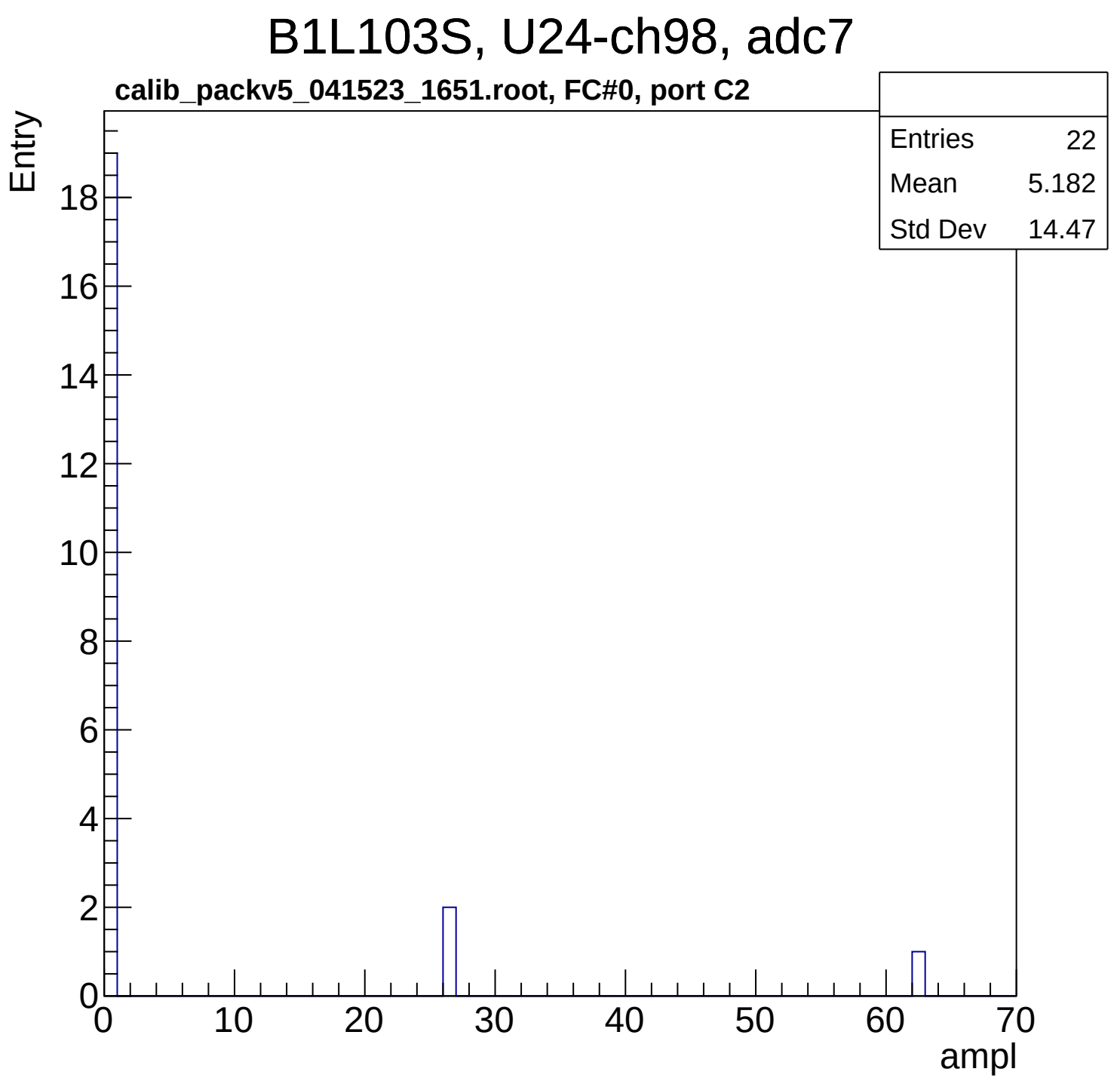
B1L103S, U24-ch98, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 5.182
Std Dev 14.47
Entry
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6
8
10
12
14
16
18
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10
20
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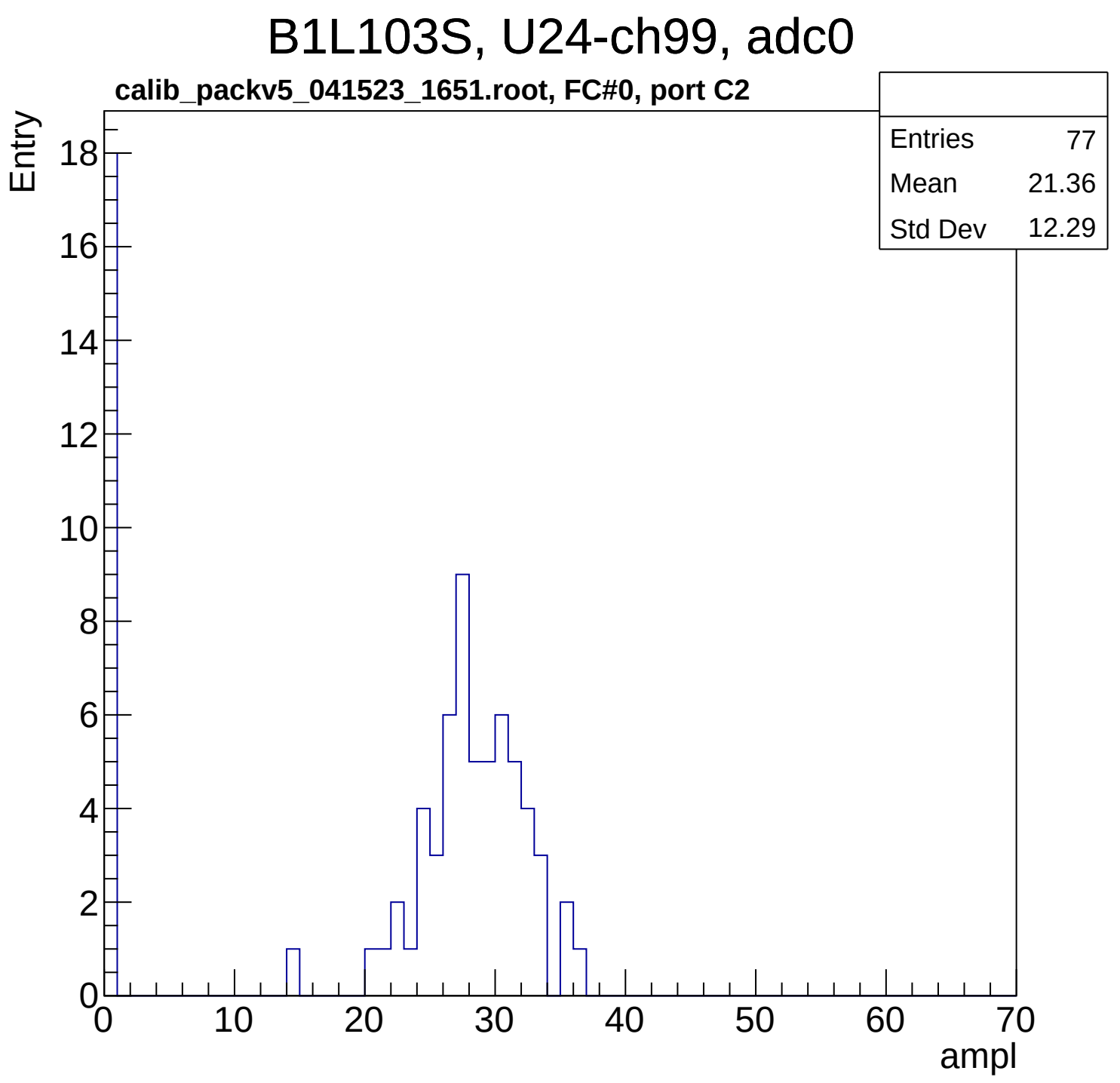
50
60
70
ampl


B1L103S, U24-ch99, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 21.36
Std Dev 12.29
Entry
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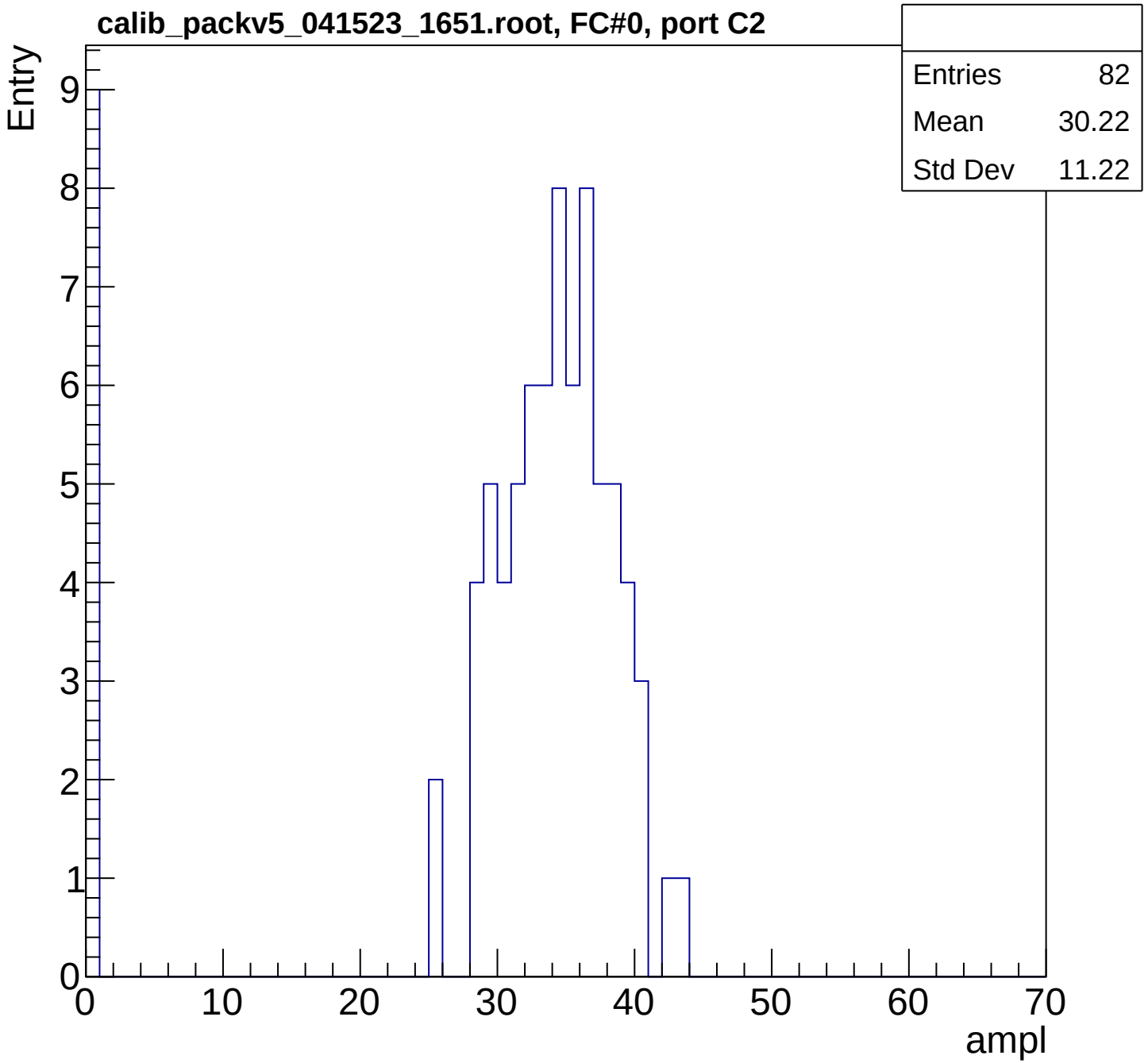
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch99, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 30.22
Std Dev 11.22
Entry
ampl
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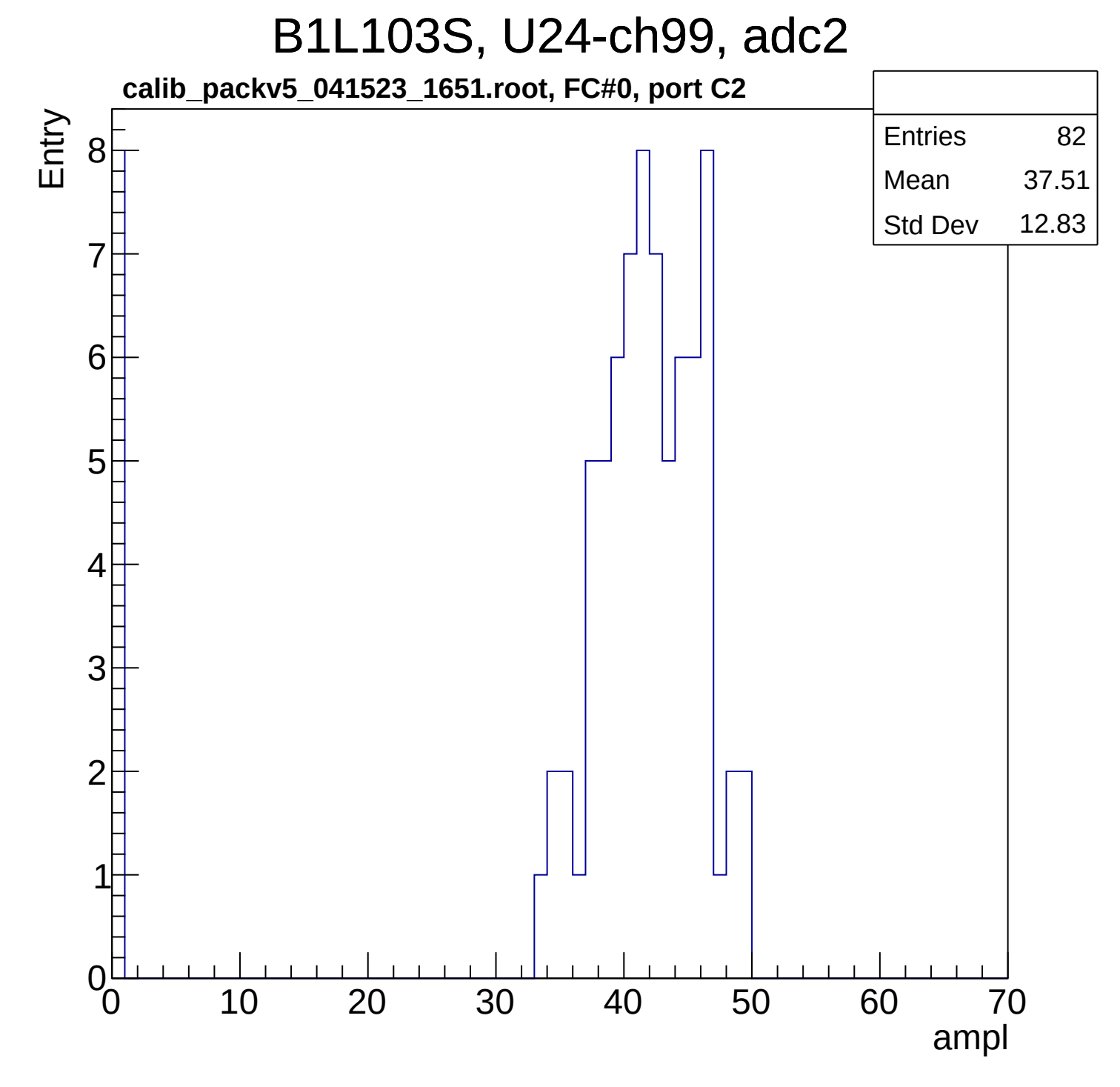
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U24-ch99, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 37.51
Std Dev 12.83
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
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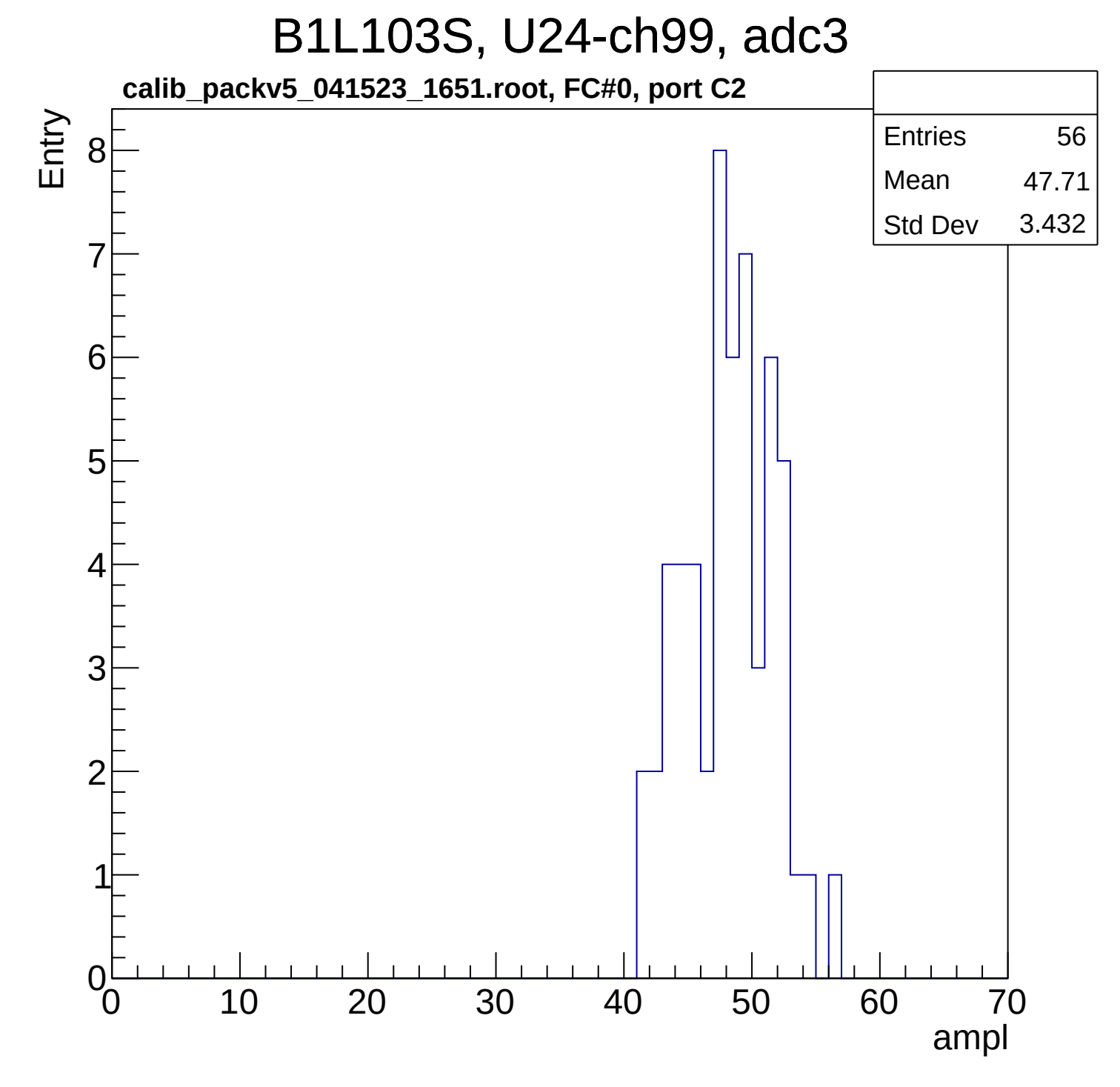
70


B1L103S, U24-ch99, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 47.71
Std Dev 3.432
Entry
ampl
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2
3
4
5
6
7
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0
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40
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60
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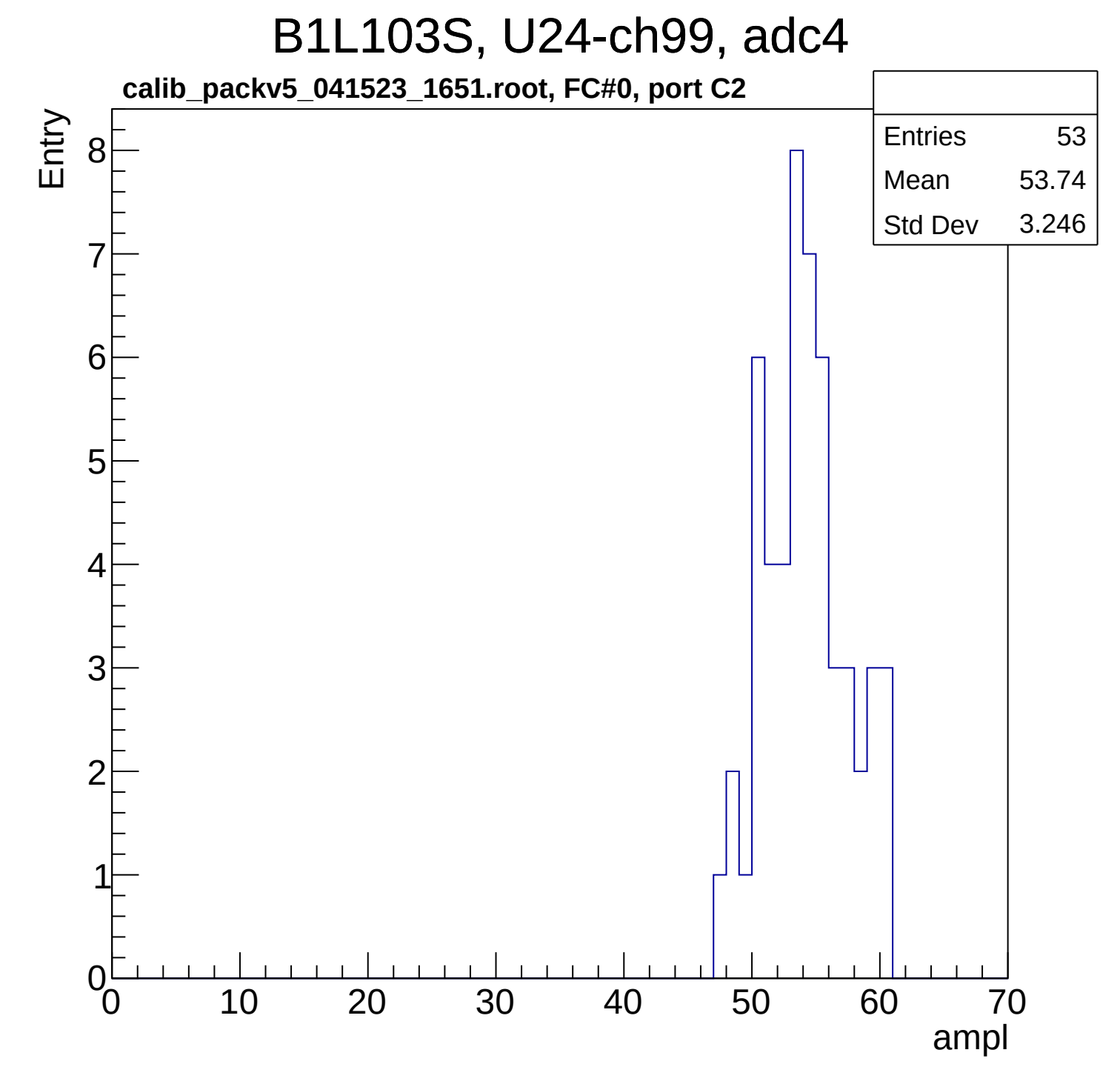
B1L103S, U24-ch99, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 53.74
Std Dev 3.246
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
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40
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60
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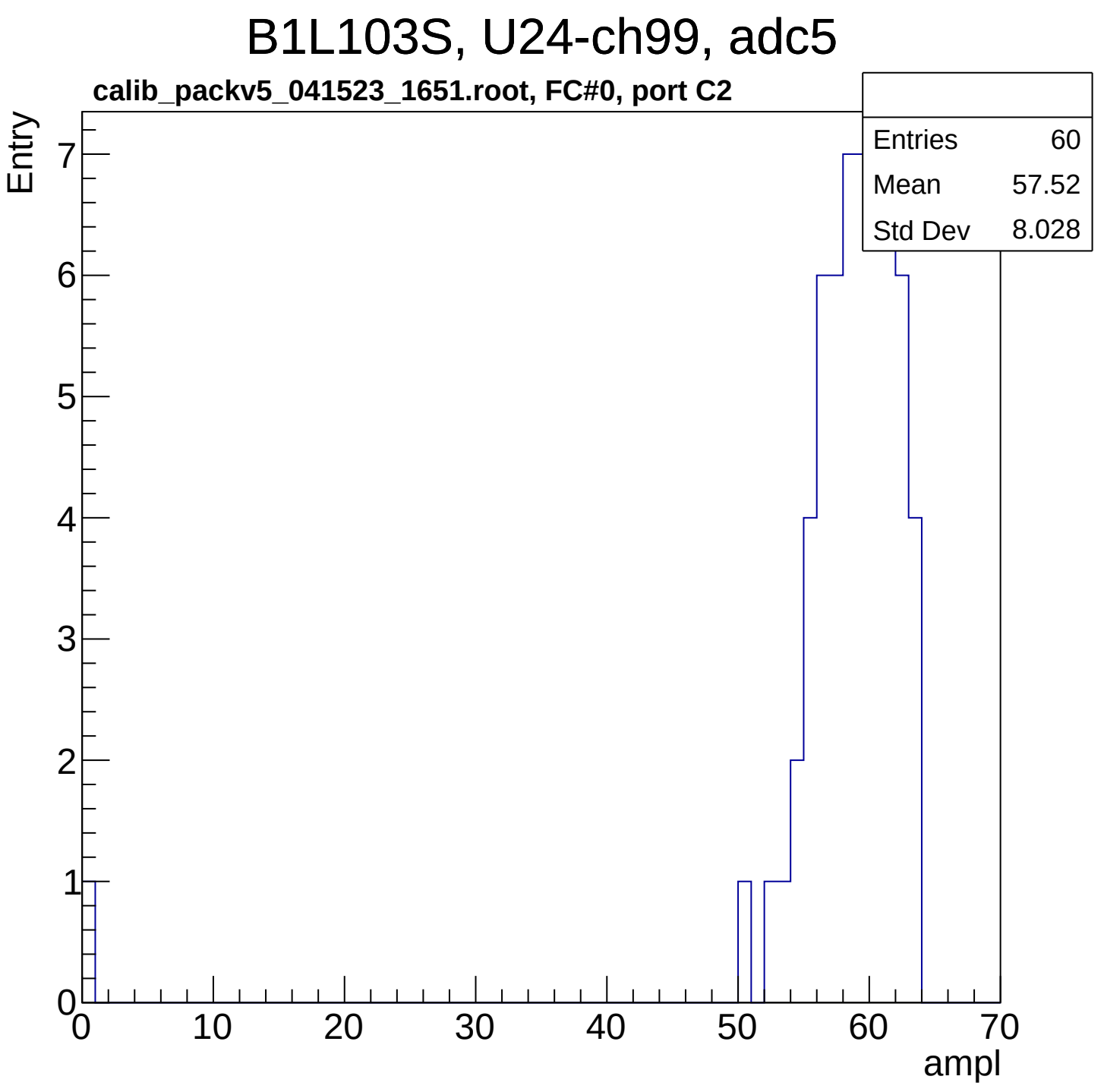
B1L103S, U24-ch99, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 57.52
Std Dev 8.028
Entry
ampl
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1
2
3
4
5
6
7
0
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20
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40
50
60
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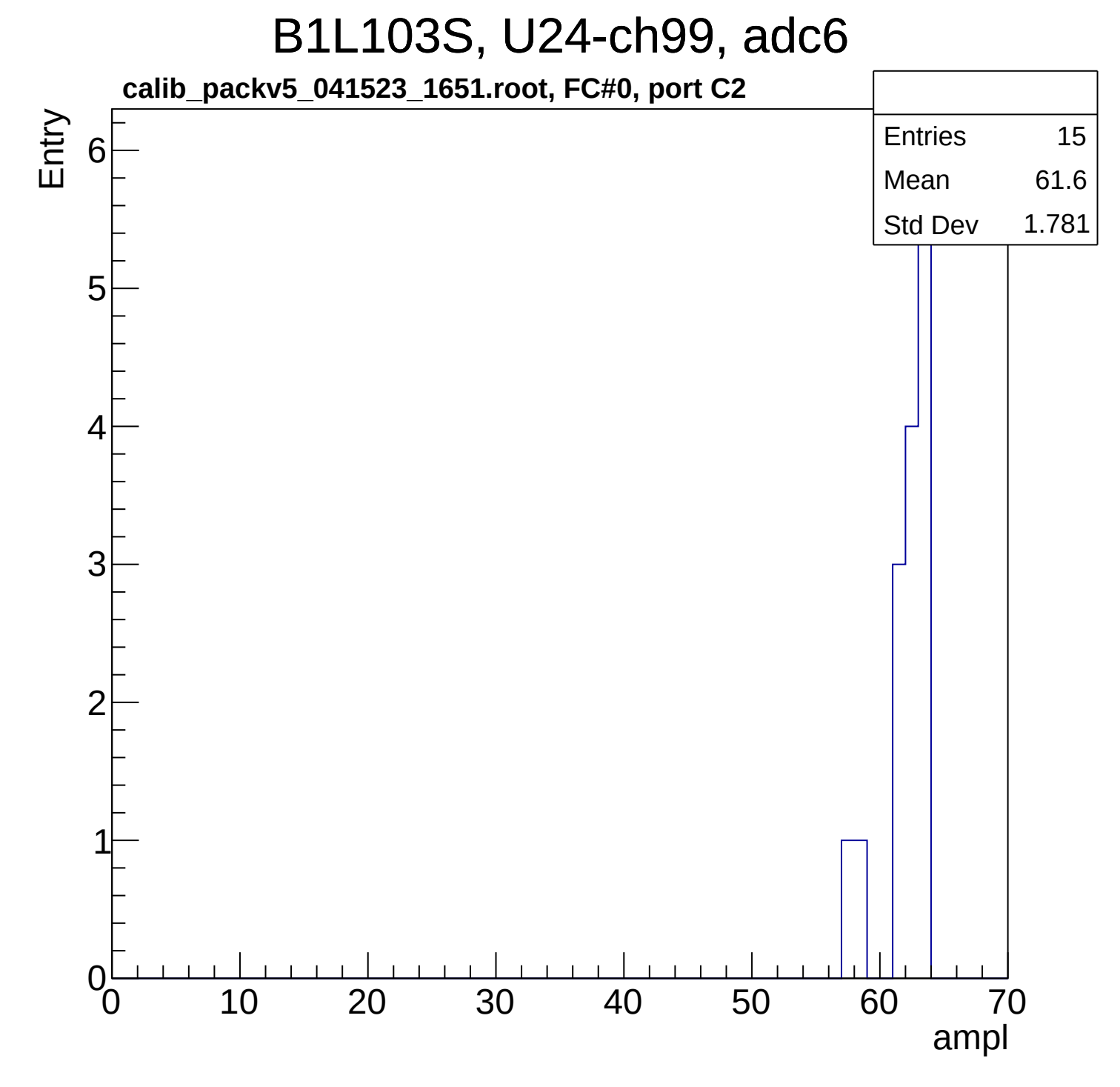
B1L103S, U24-ch99, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 15
Mean 61.6
Std Dev 1.781
Entry
ampl
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3
4
5
6
0
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20
30
40
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60
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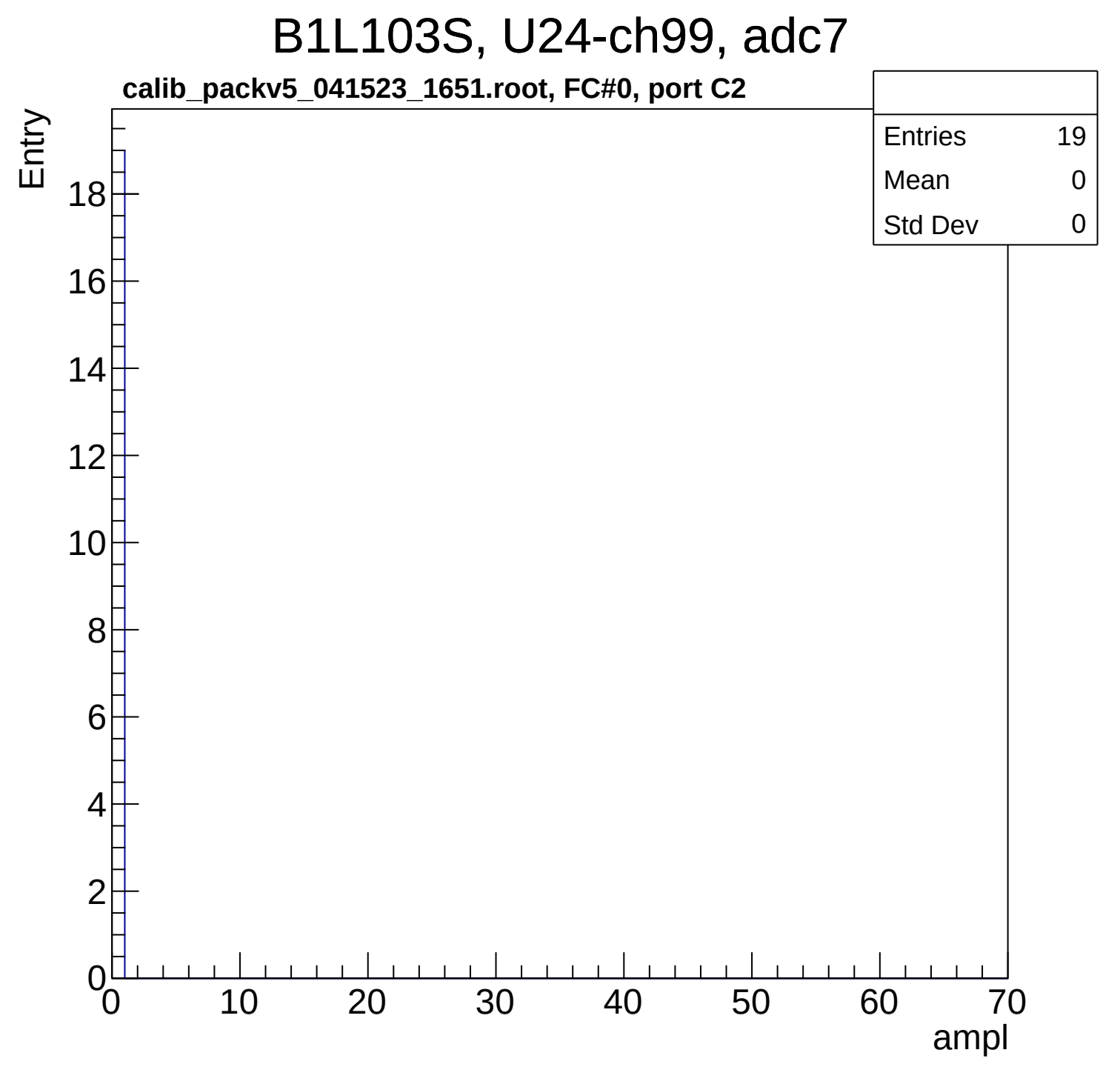
B1L103S, U24-ch99, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
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6
8
10
12
14
16
18
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10
20
30
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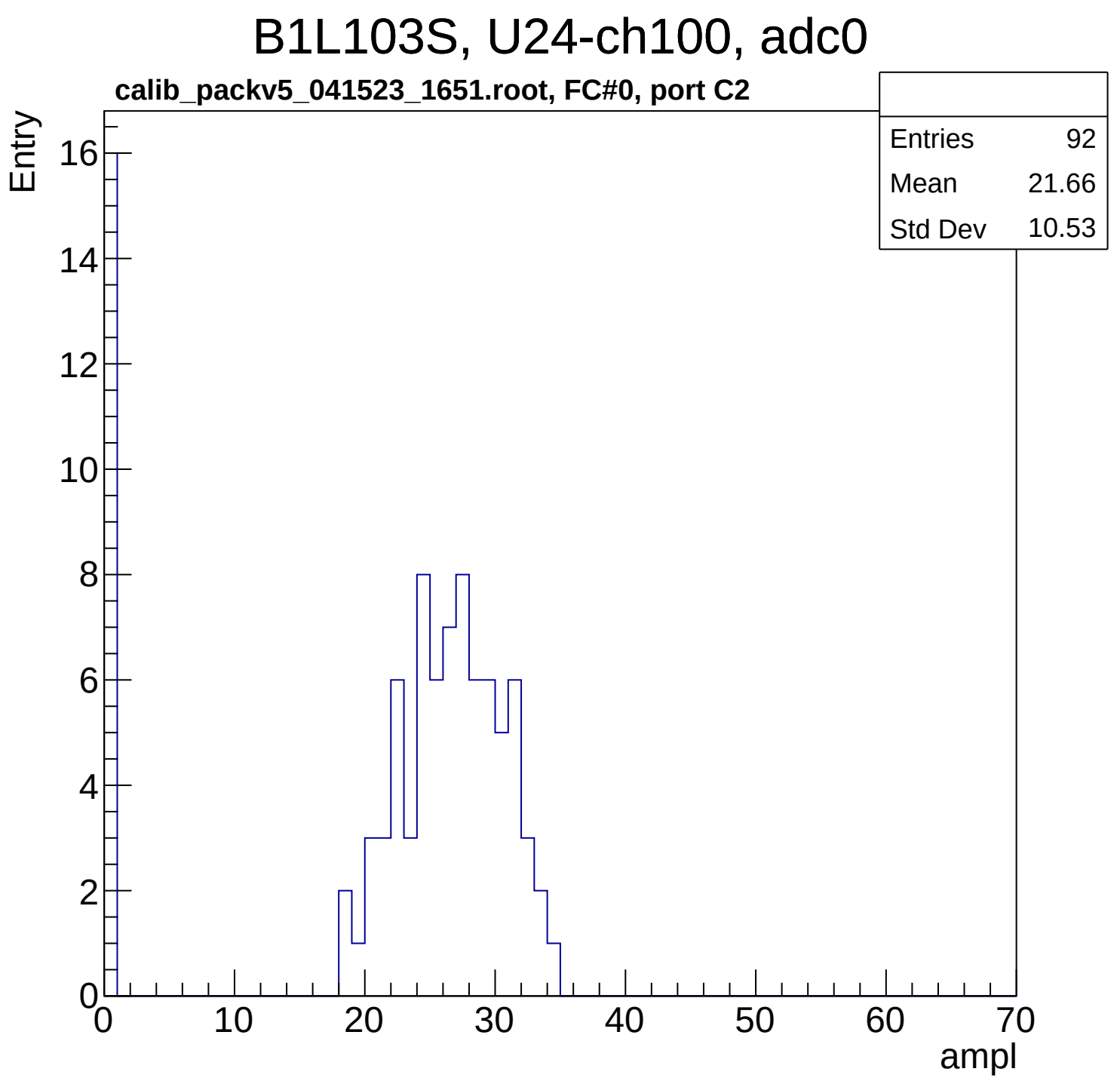
70
ampl


B1L103S, U24-ch100, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 92
Mean 21.66
Std Dev 10.53
Entry
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4
6
8
10
12
14
16
0
10
20
30
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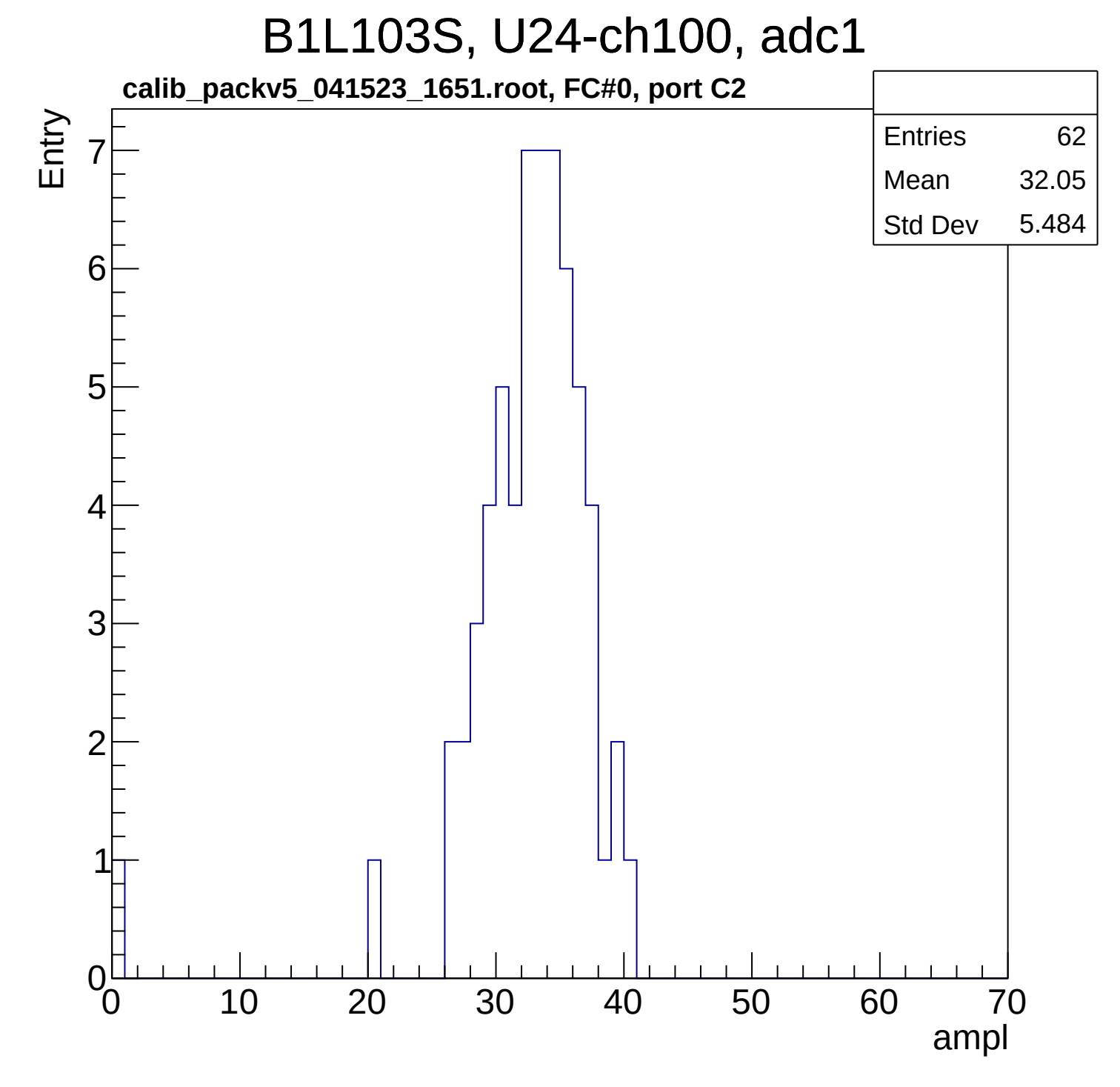
50
60
70
ampl


B1L103S, U24-ch100, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 32.05
Std Dev 5.484
Entry
ampl
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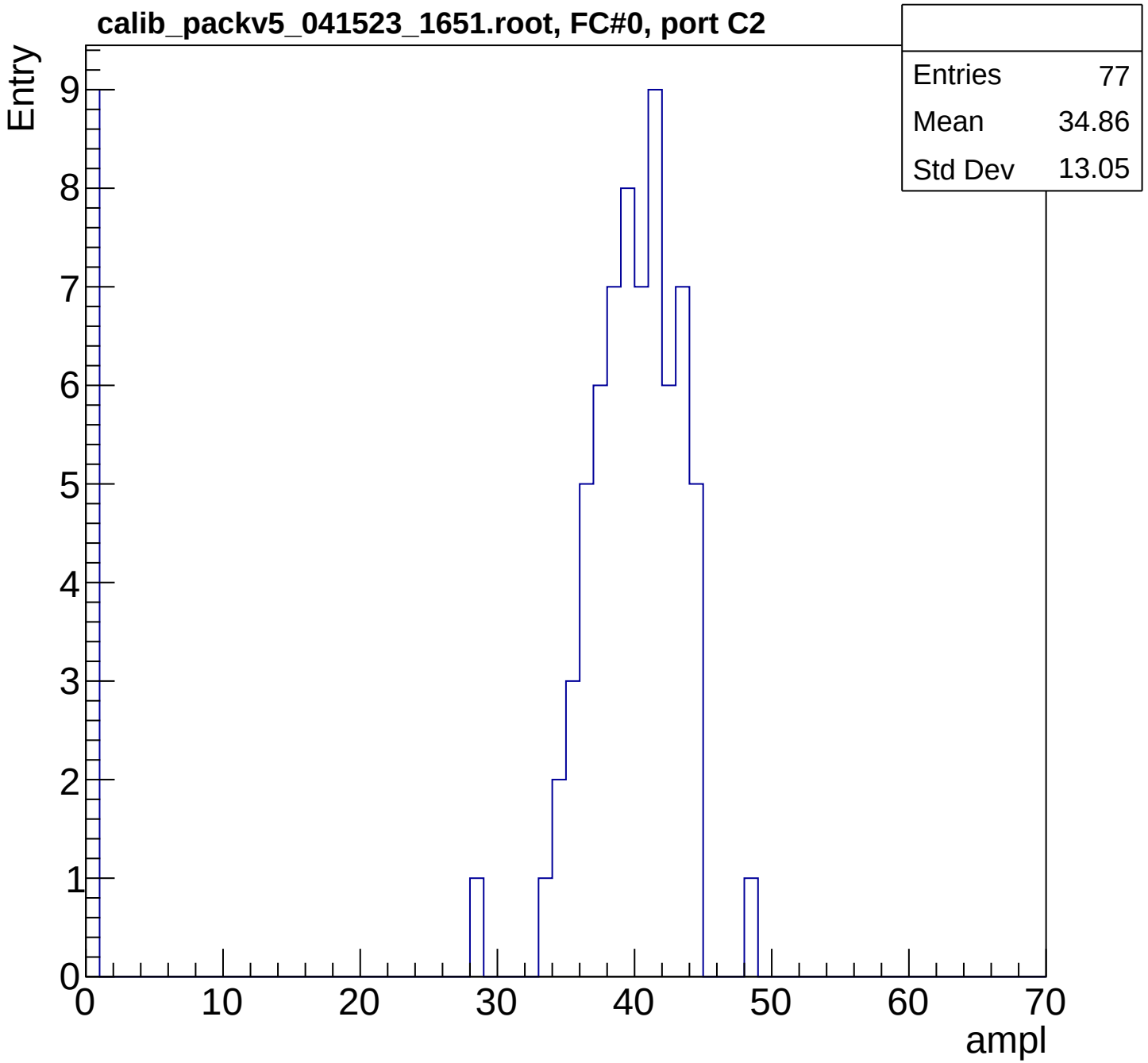
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U24-ch100, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 34.86
Std Dev 13.05
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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60
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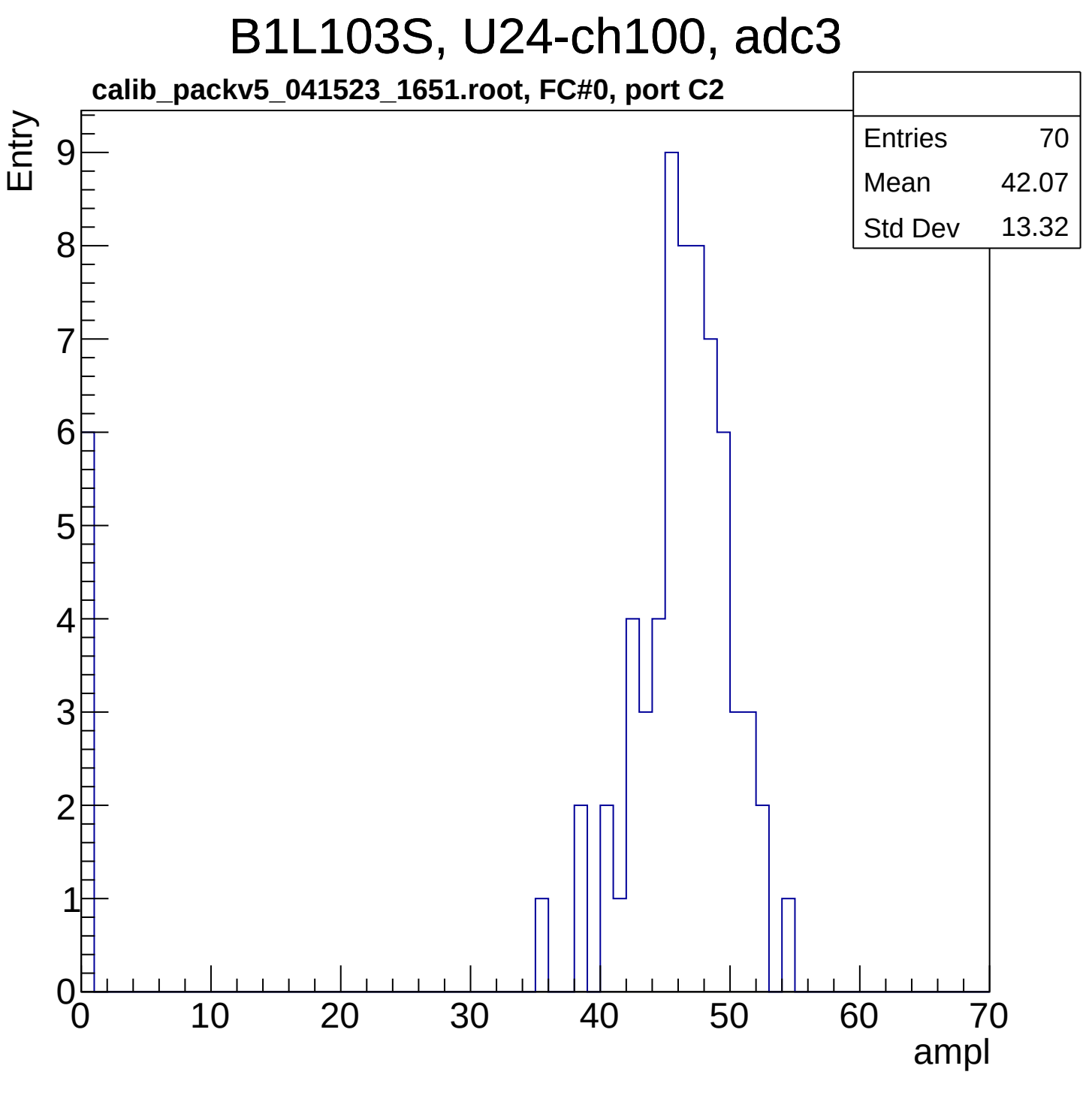
B1L103S, U24-ch100, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 42.07
Std Dev 13.32
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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60
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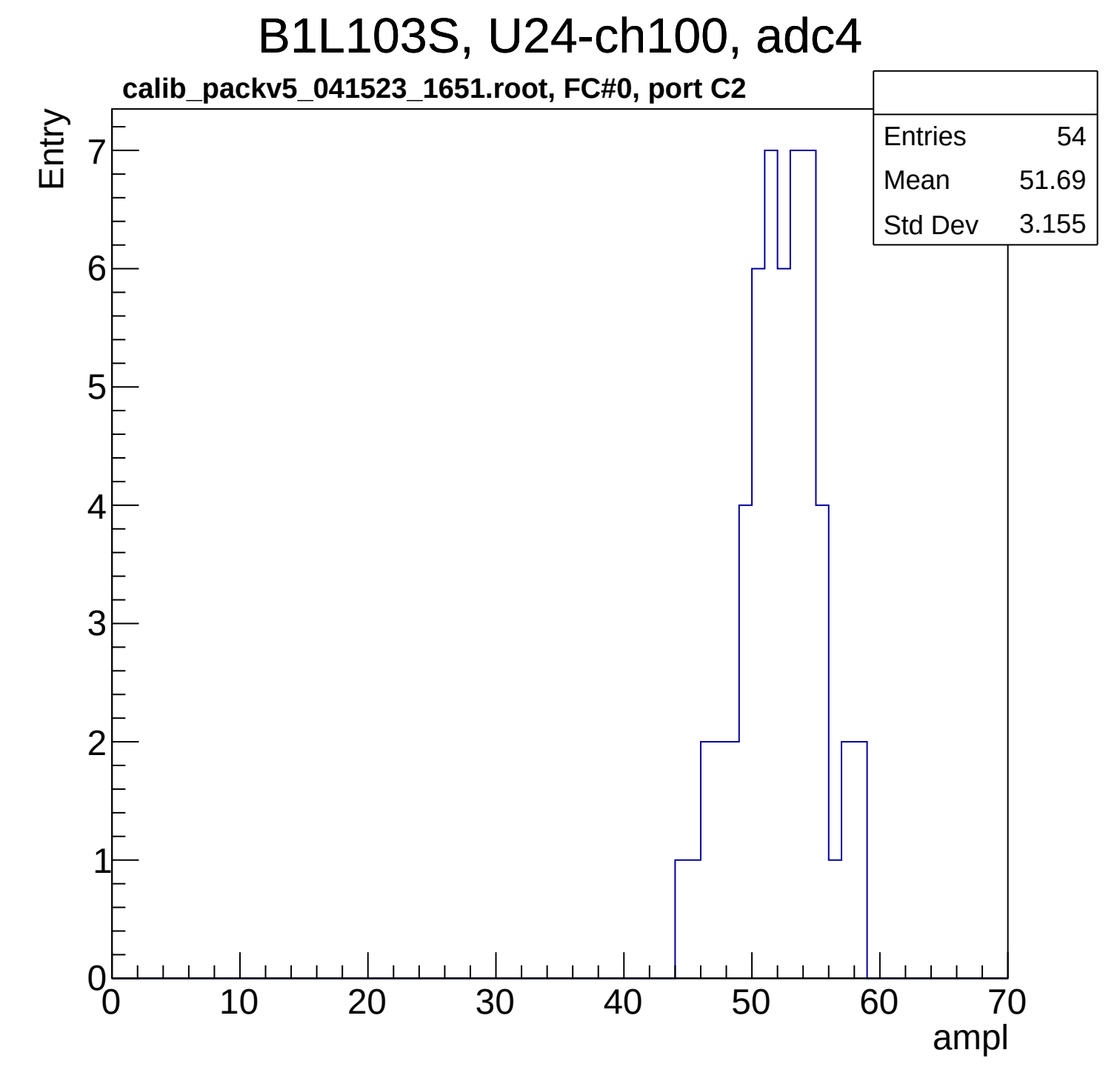
B1L103S, U24-ch100, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 51.69
Std Dev 3.155
Entry
ampl
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3
4
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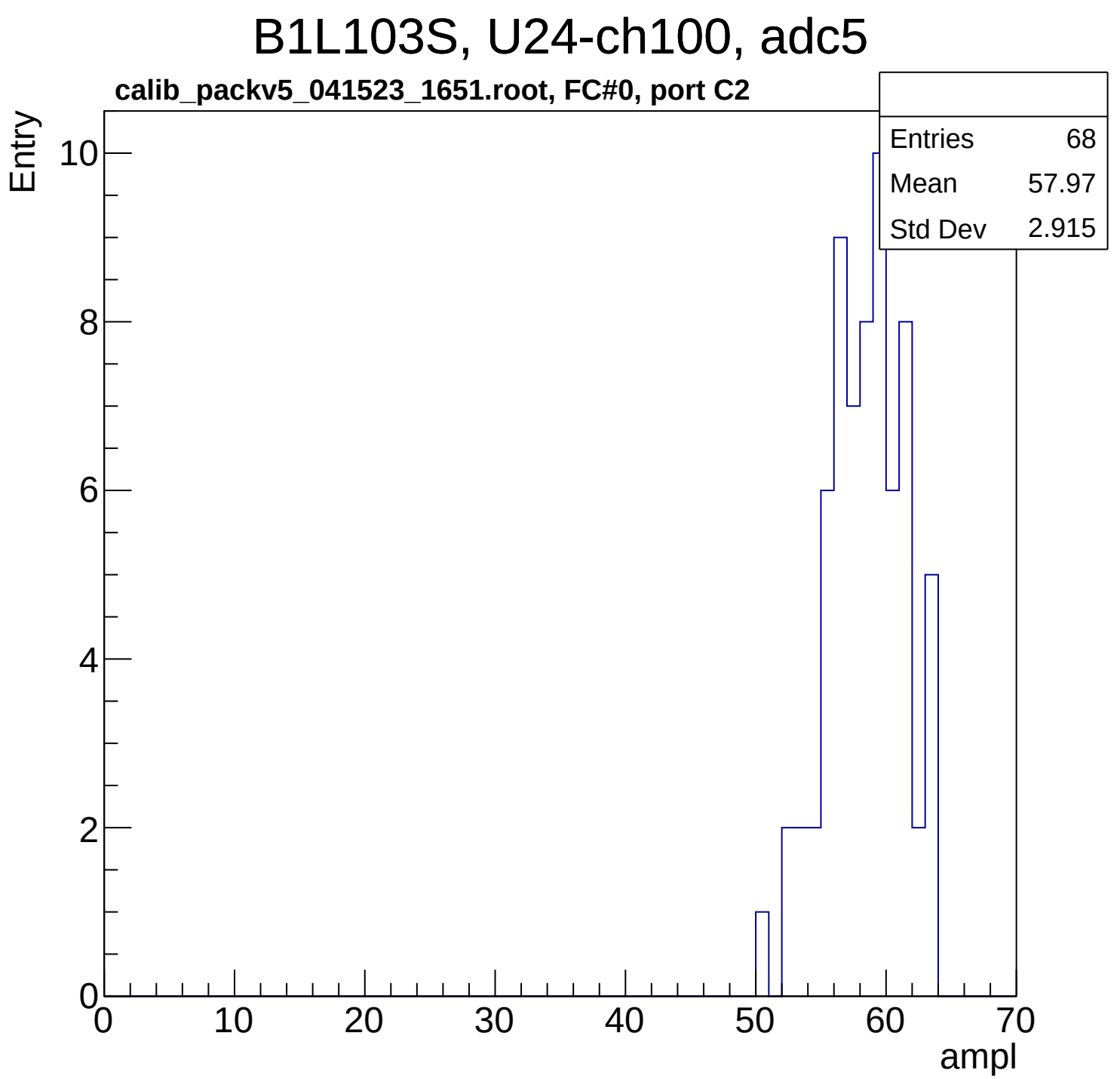
6
7
0
10
20
30
40
50
60
70


B1L103S, U24-ch100, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 57.97
Std Dev 2.915
Entry
ampl
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4
6
8
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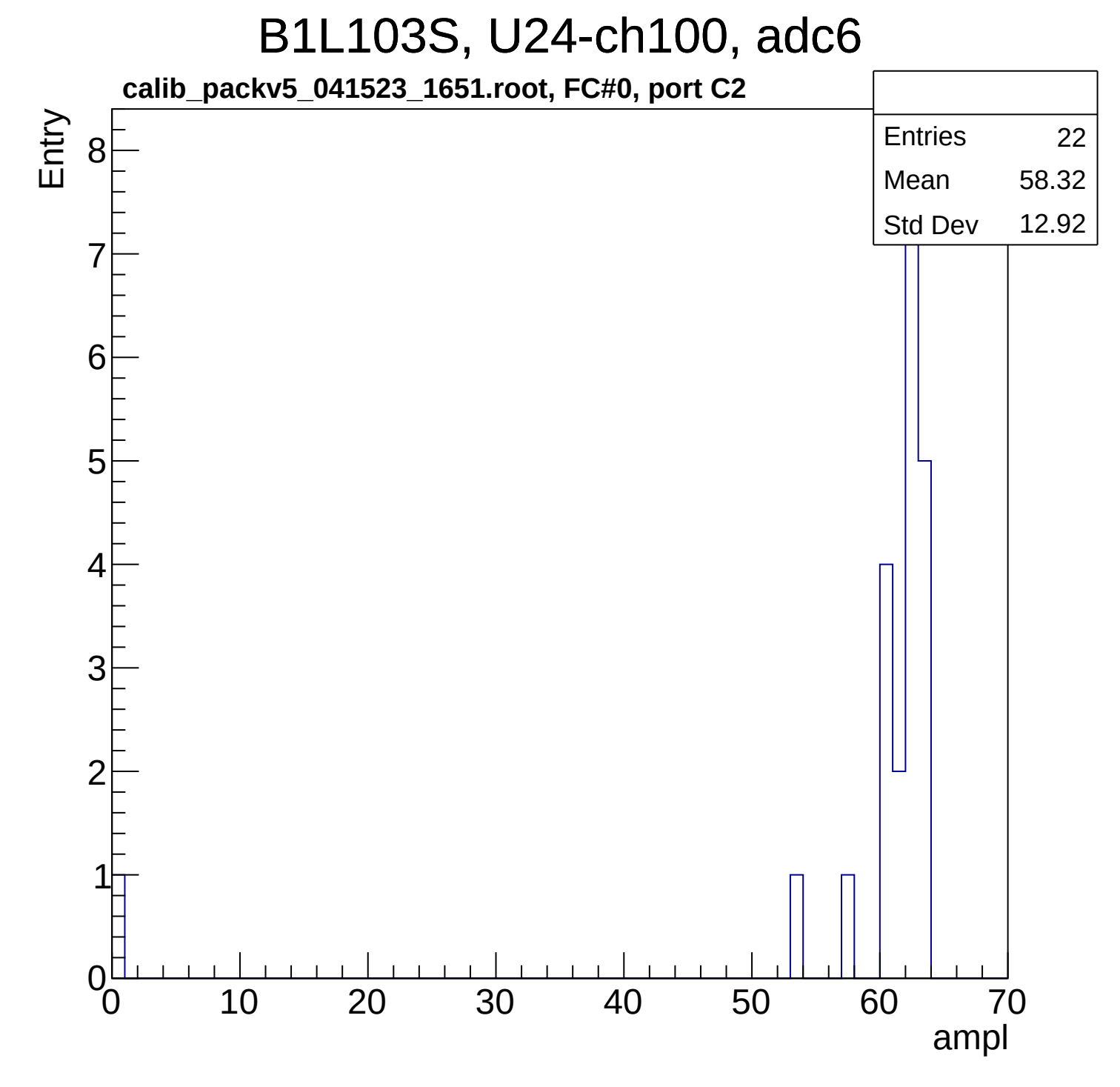
0
10
20
30
40
50
60
70


B1L103S, U24-ch100, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 58.32
Std Dev 12.92
Entry
ampl
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7
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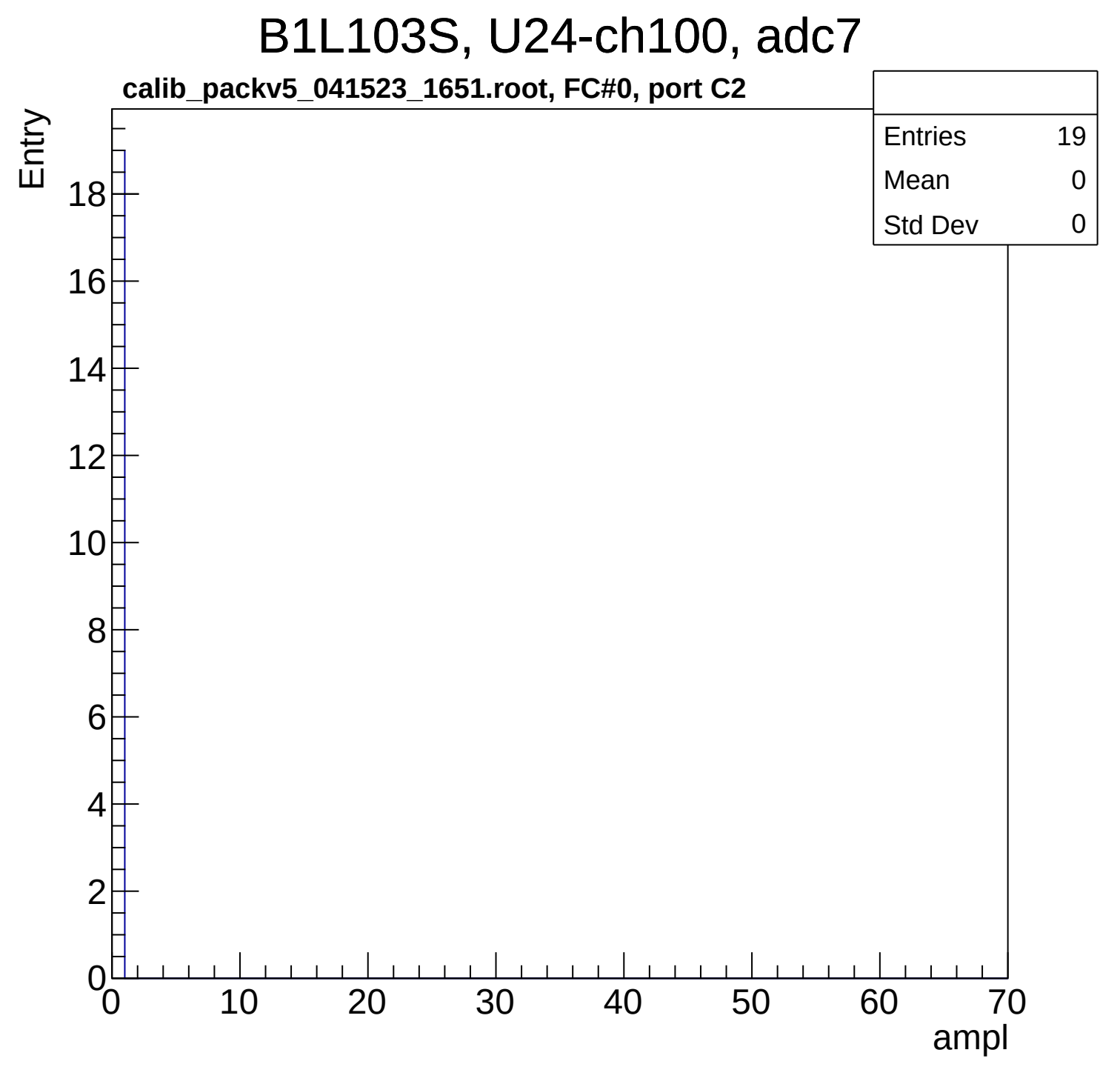
B1L103S, U24-ch100, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
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14
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18
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10
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50
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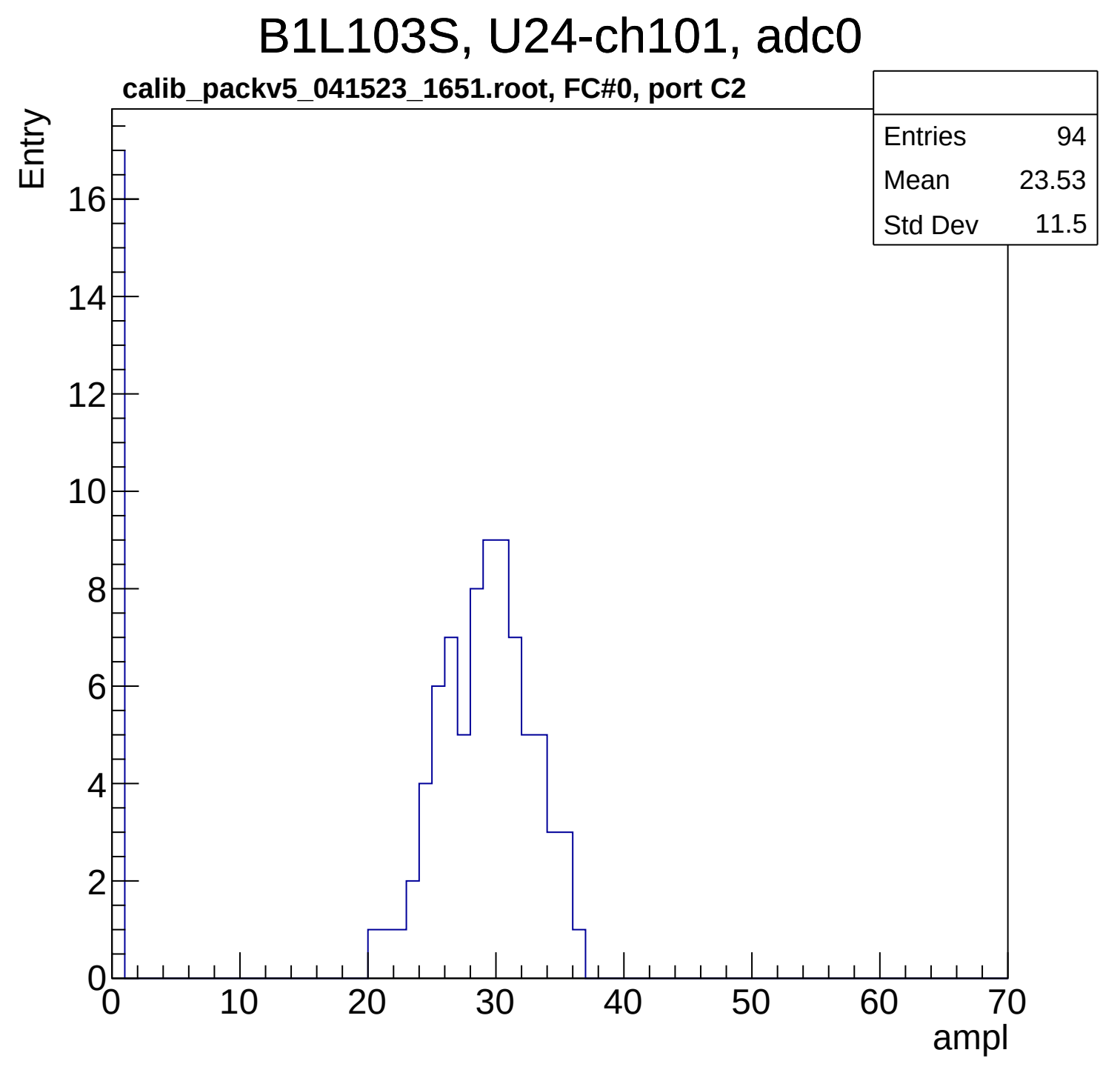
70
ampl


B1L103S, U24-ch101, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 94
Mean 23.53
Std Dev 11.5
Entry
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8
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16
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50
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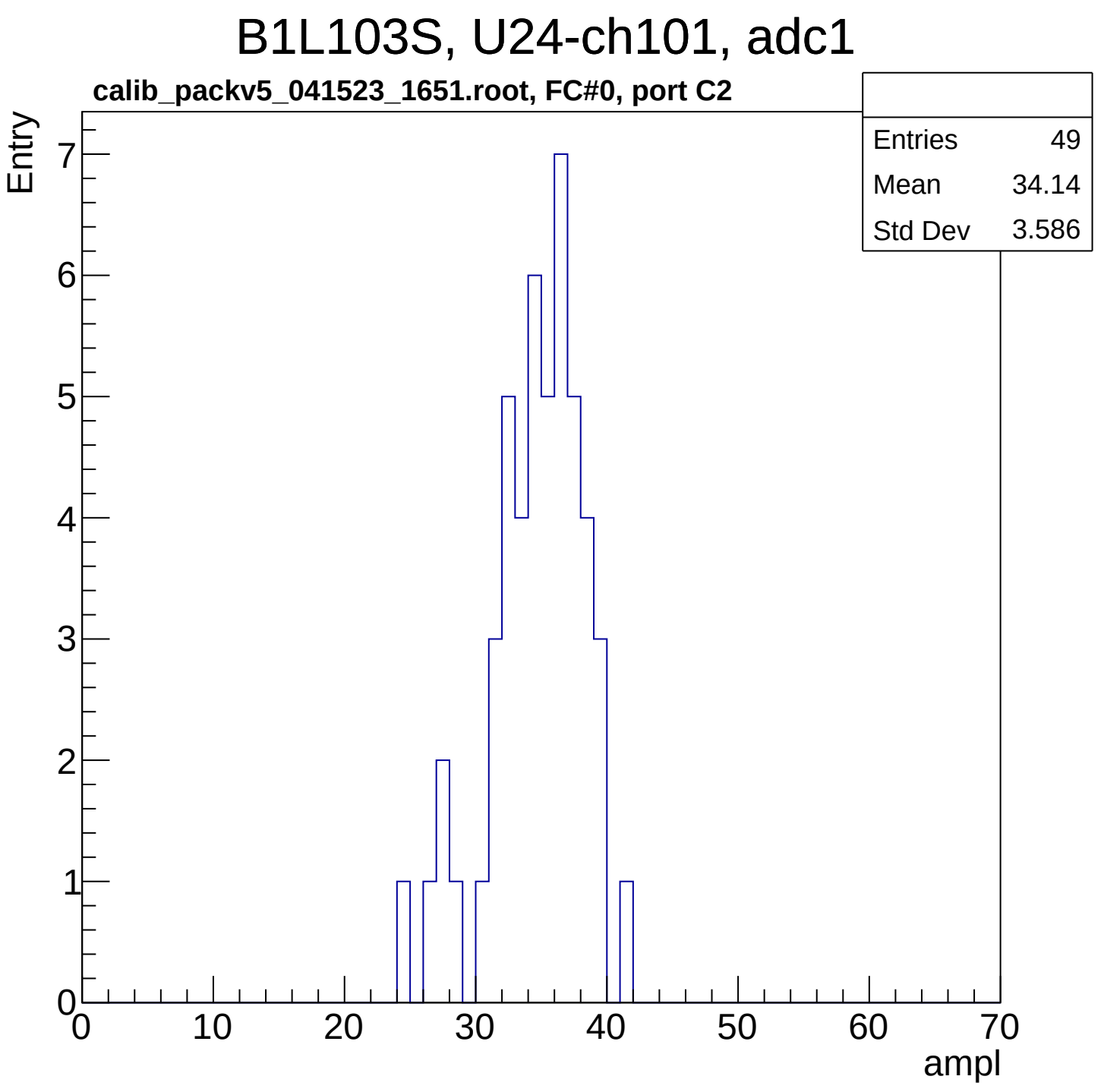
ampl


B1L103S, U24-ch101, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 34.14
Std Dev 3.586
Entry
ampl
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4
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6
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0
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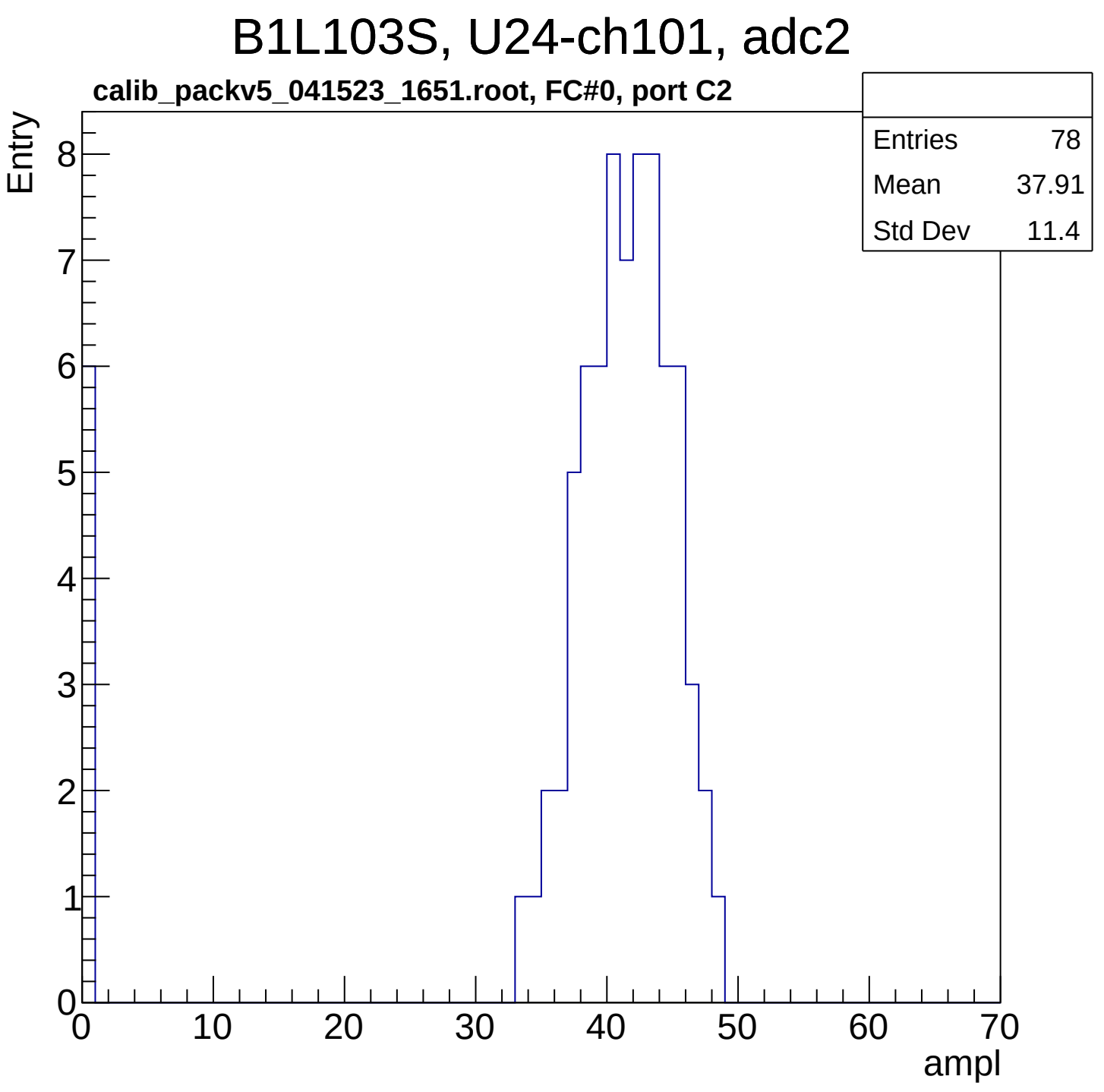
B1L103S, U24-ch101, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 37.91
Std Dev 11.4
Entry
ampl
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3
4
5
6
7
8
0
10
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40
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60
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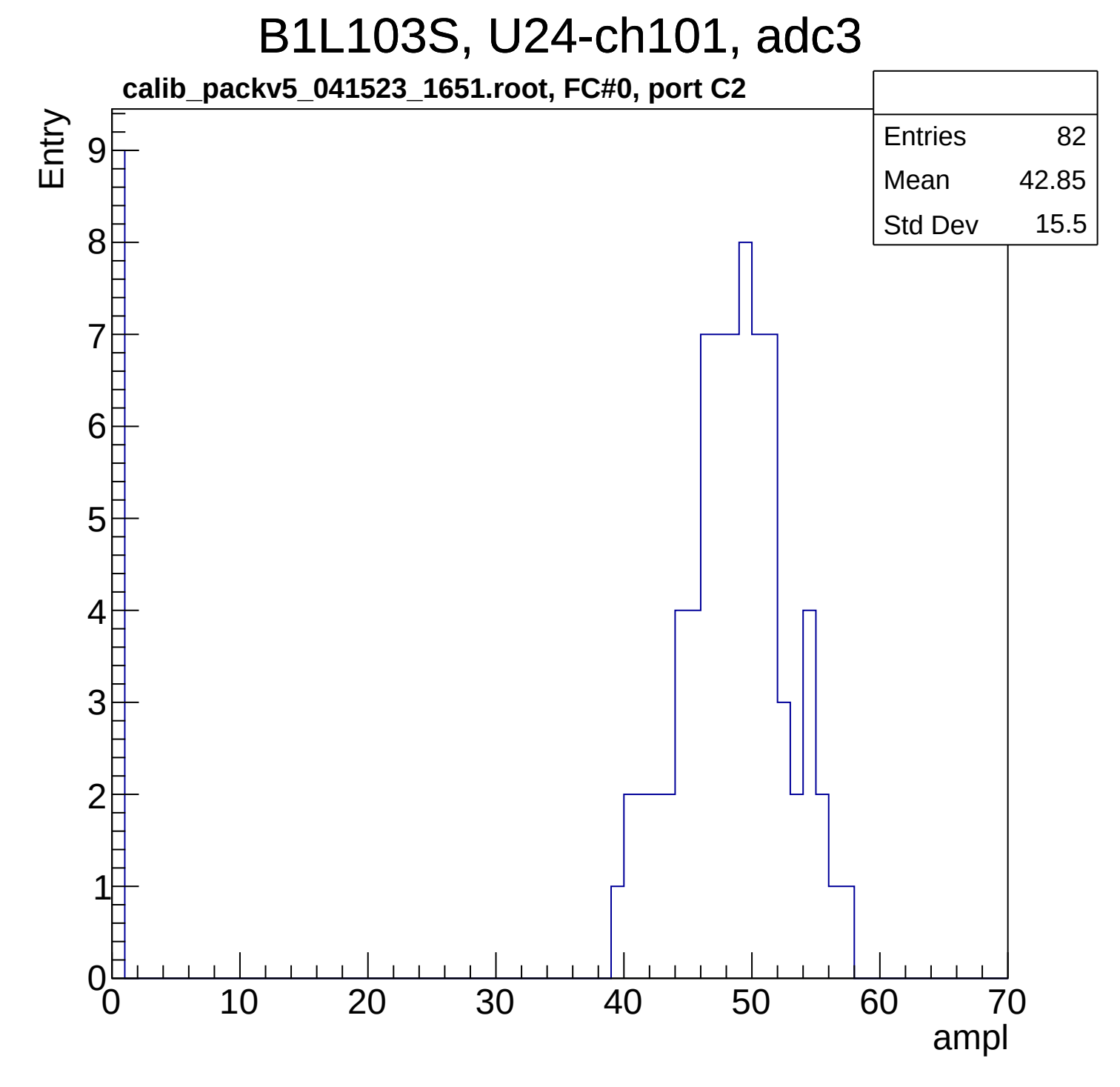
B1L103S, U24-ch101, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 42.85
Std Dev 15.5
Entry
ampl
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3
4
5
6
7
8
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0
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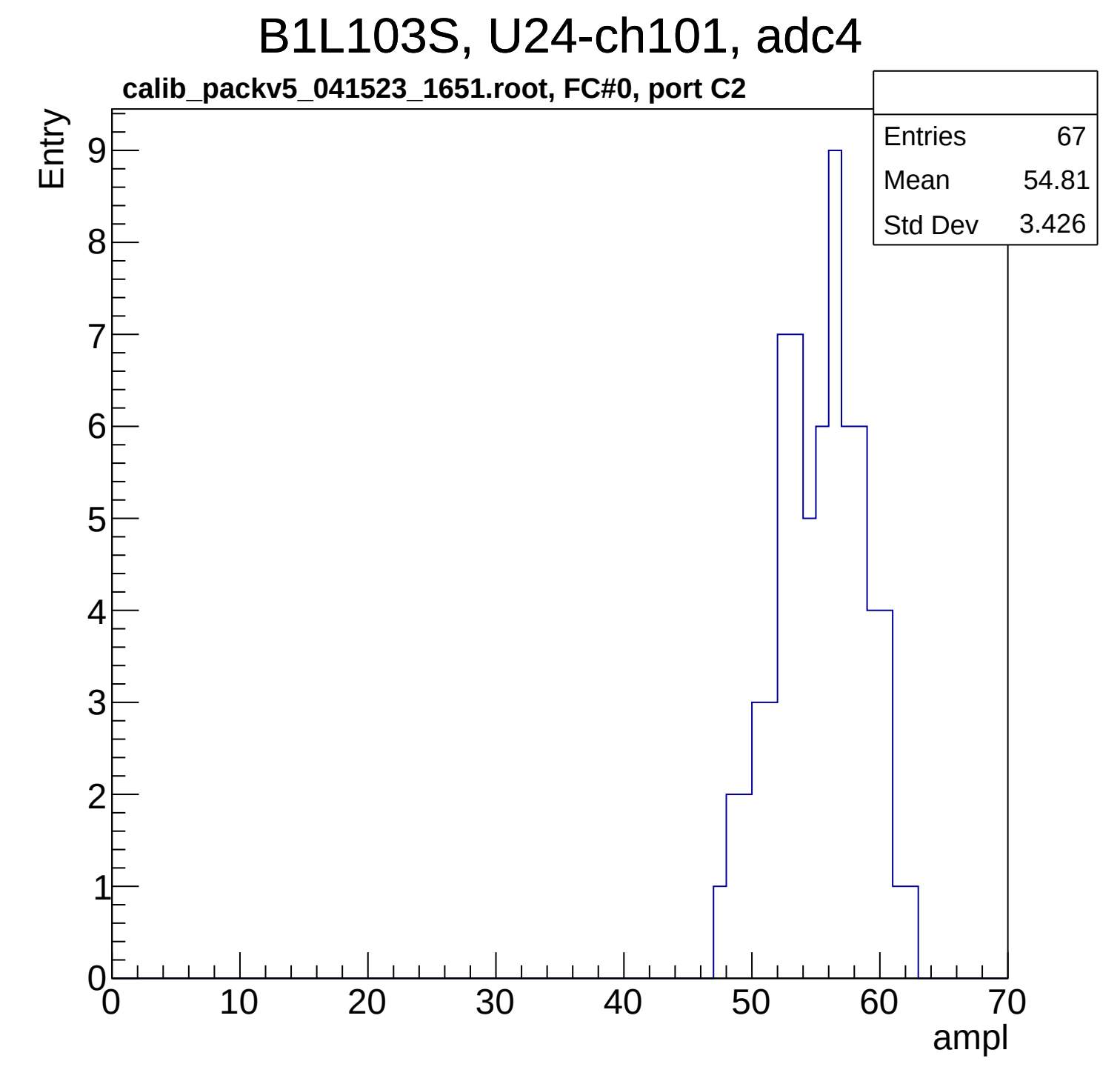
B1L103S, U24-ch101, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 54.81
Std Dev 3.426
Entry
ampl
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5
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8
9
0
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40
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60
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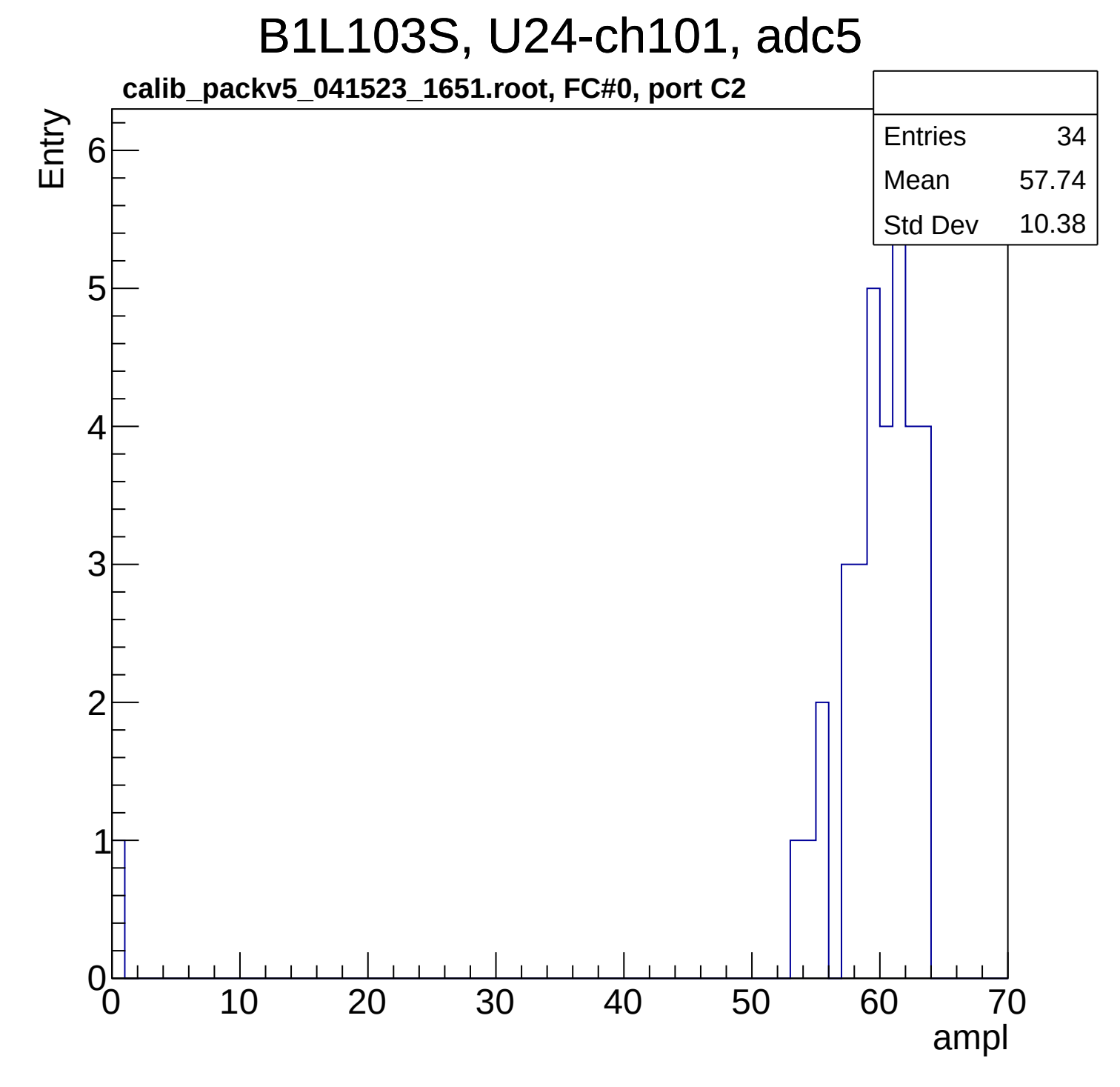
B1L103S, U24-ch101, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 34
Mean 57.74
Std Dev 10.38
Entry
ampl
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2
3
4
5
6
0
10
20
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40
50
60
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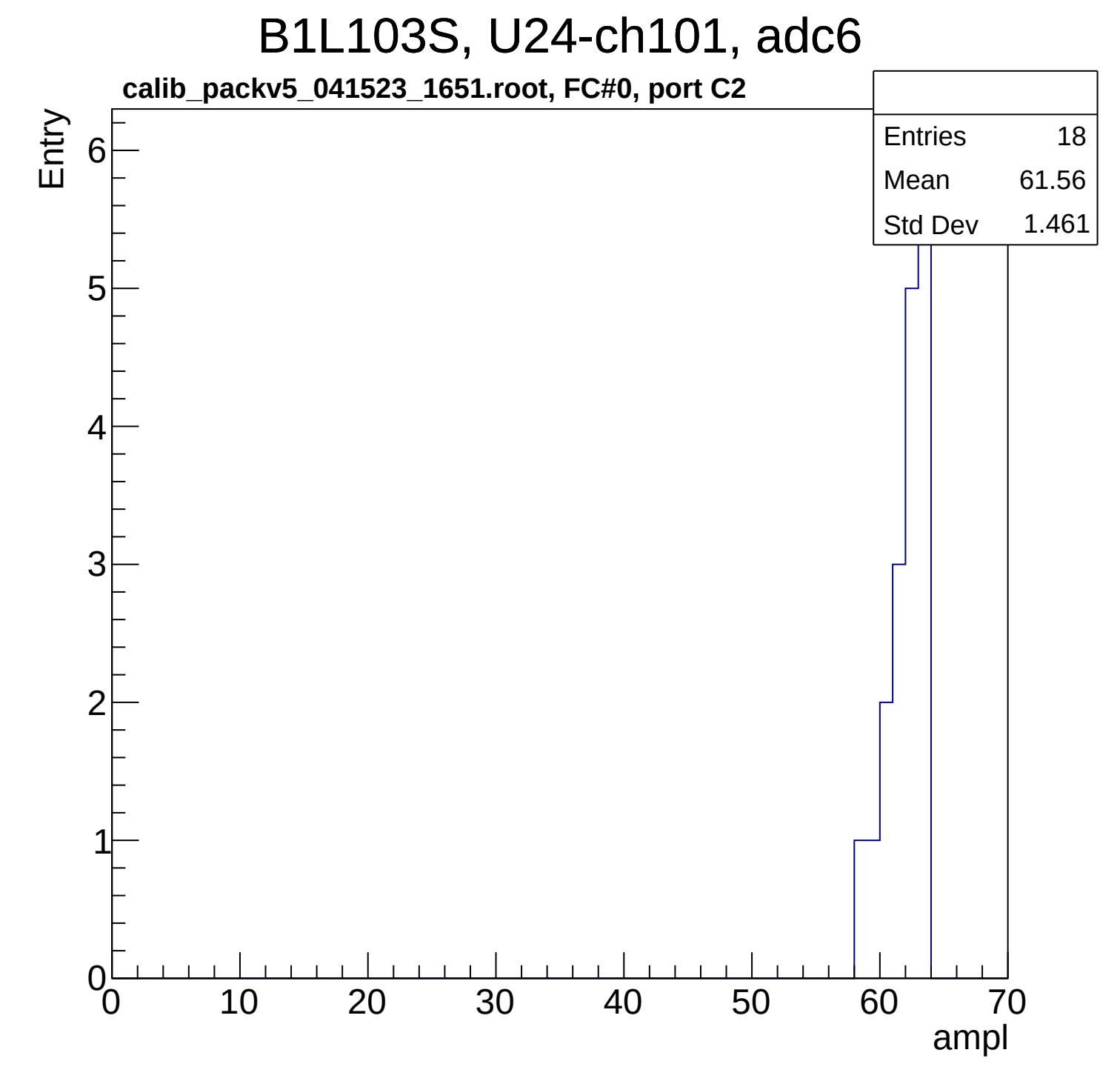
B1L103S, U24-ch101, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 61.56
Std Dev 1.461
Entry
ampl
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1
2
3
4
5
6
0
10
20
30
40
50
60
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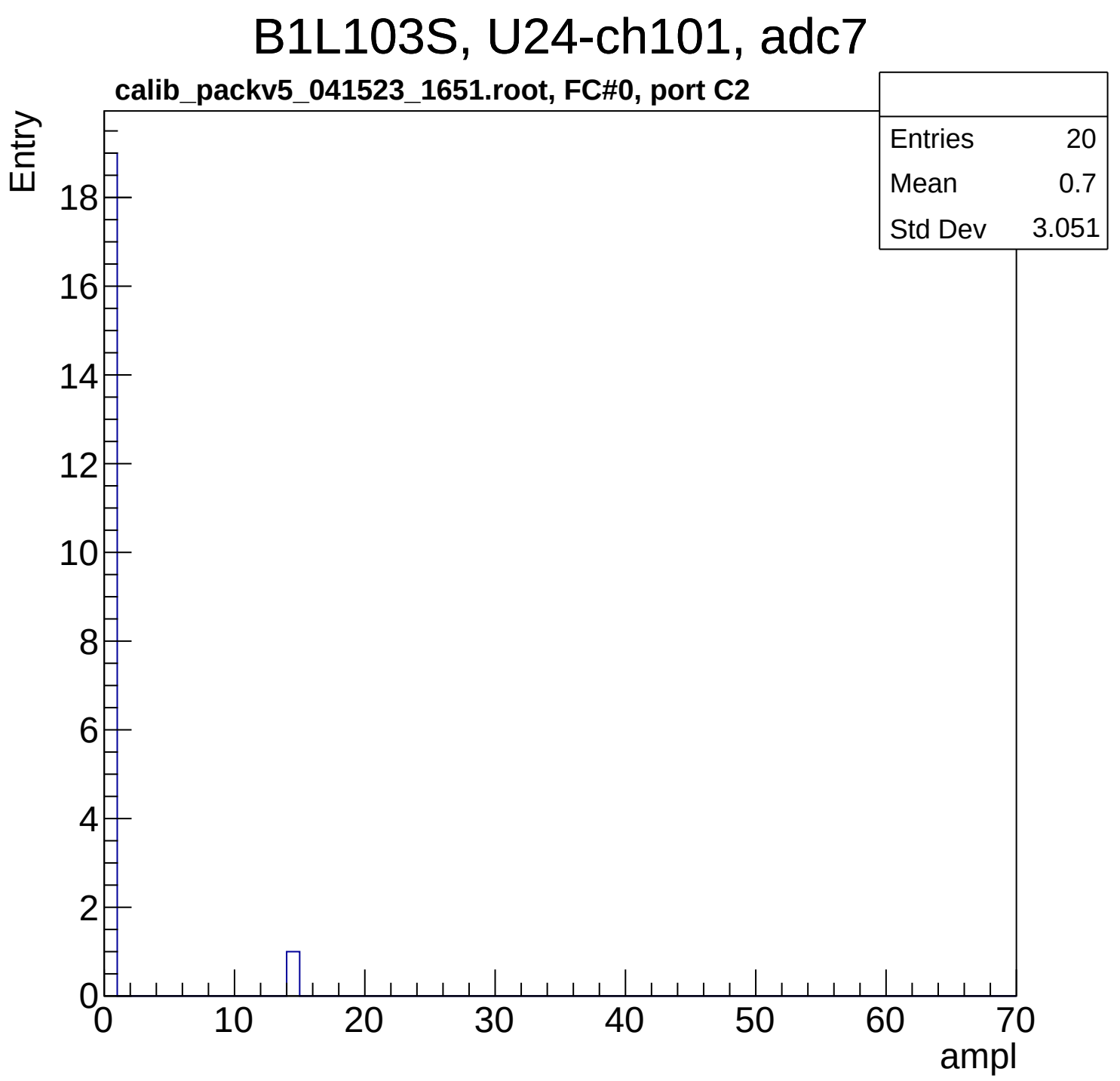
B1L103S, U24-ch101, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 0.7
Std Dev 3.051
Entry
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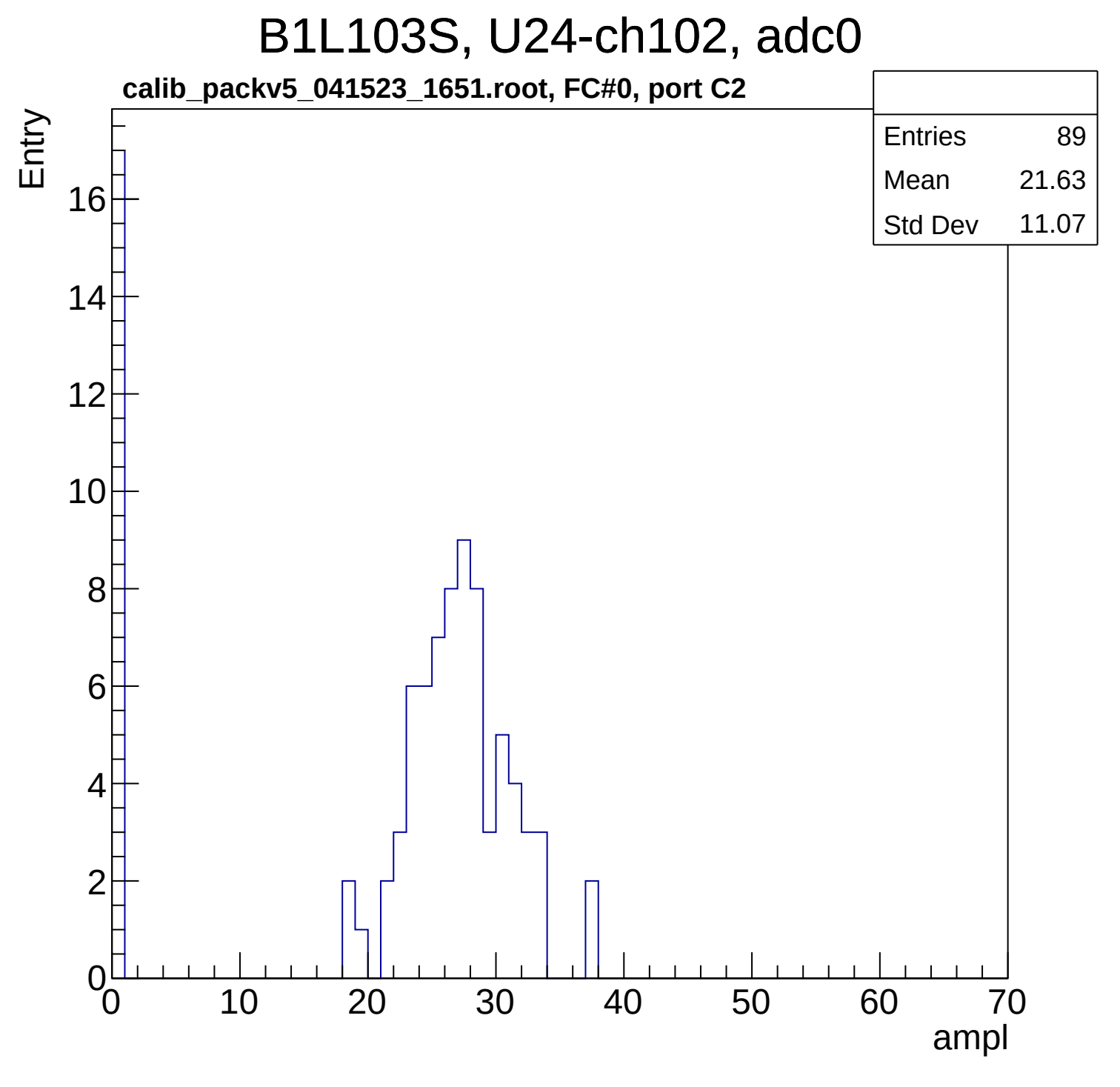
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch102, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 89
Mean 21.63
Std Dev 11.07
Entry
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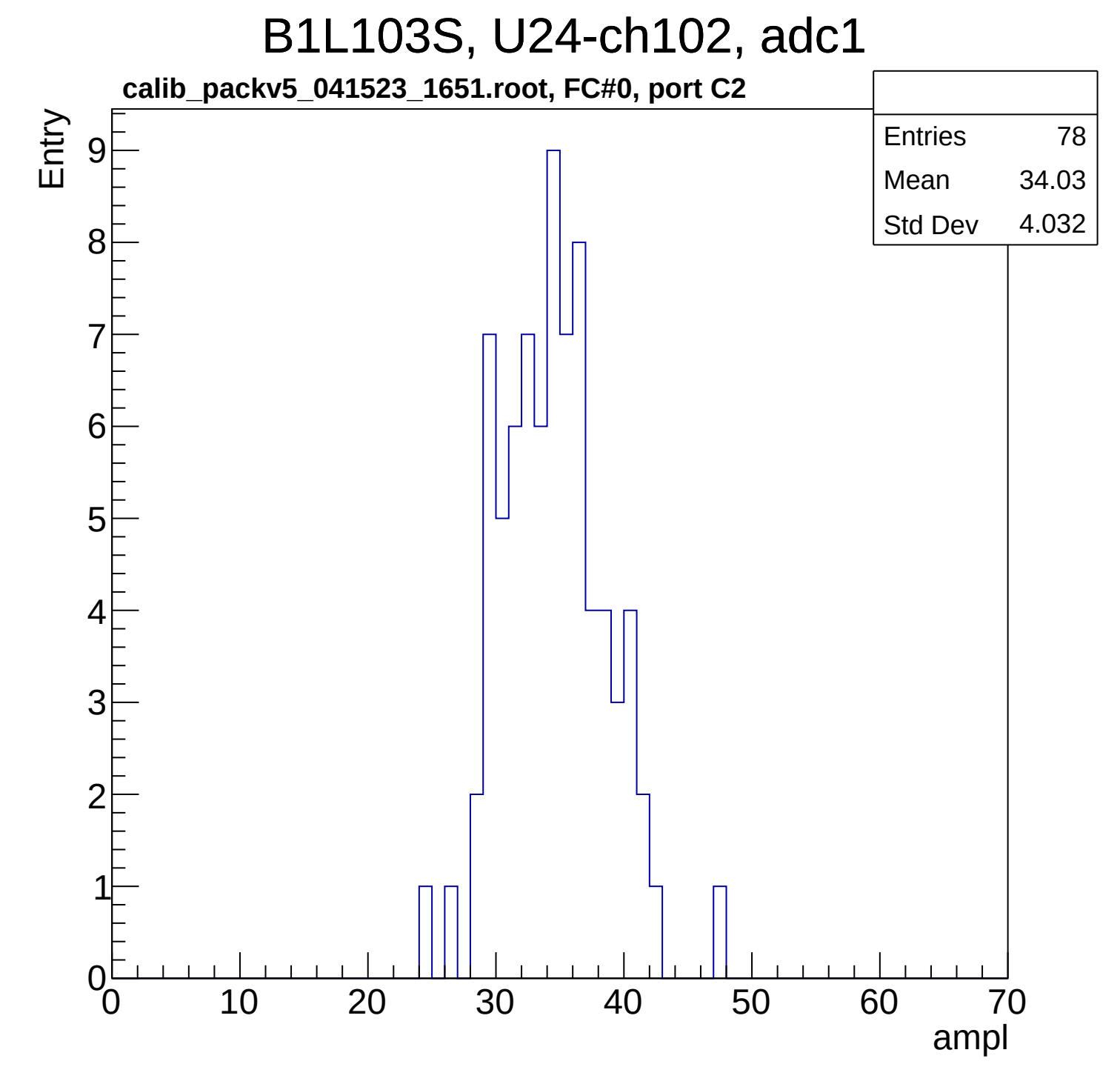
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch102, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 34.03
Std Dev 4.032
Entry
ampl
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2
3
4
5
6
7
8
9
0
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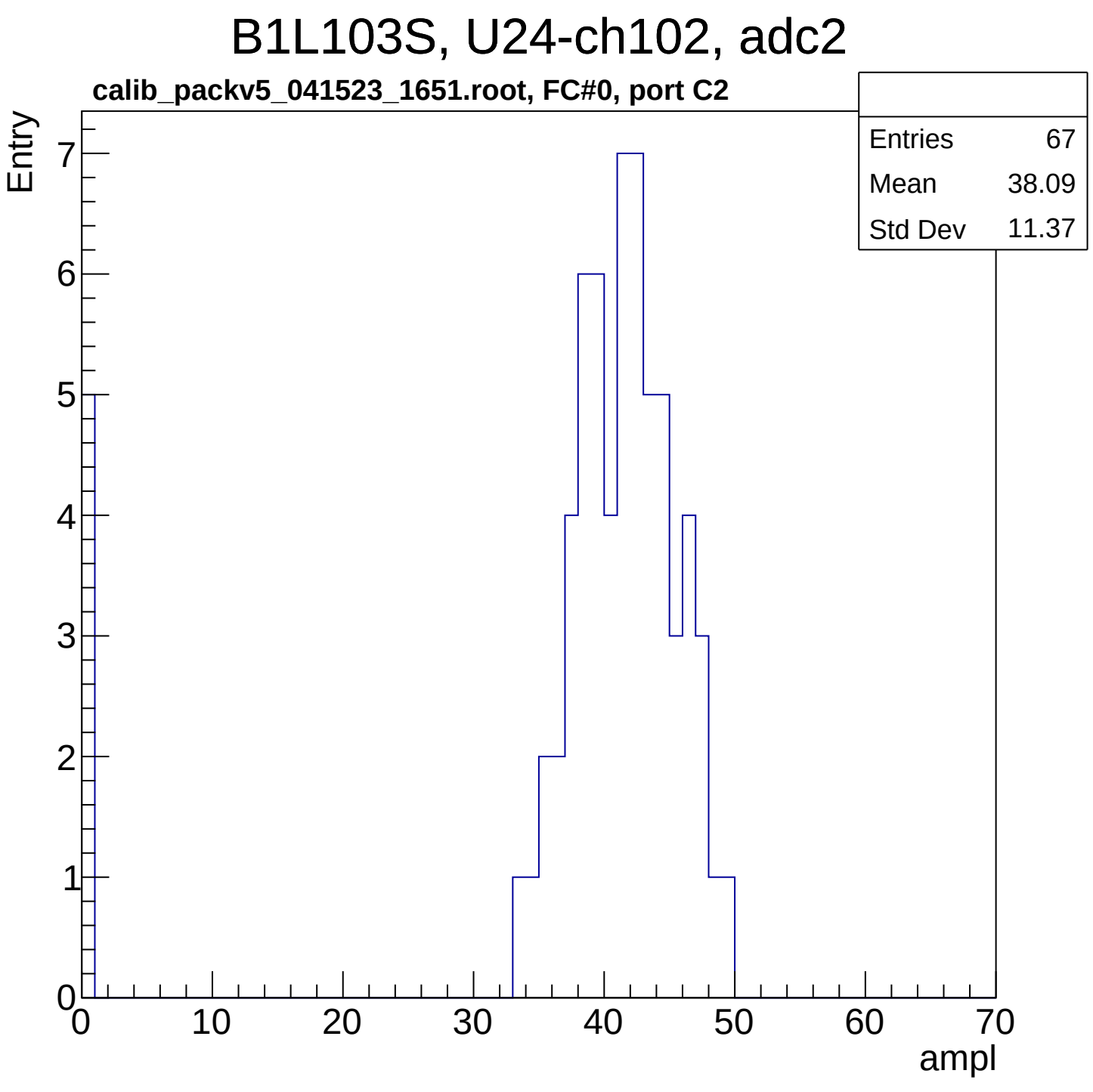
B1L103S, U24-ch102, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 38.09
Std Dev 11.37
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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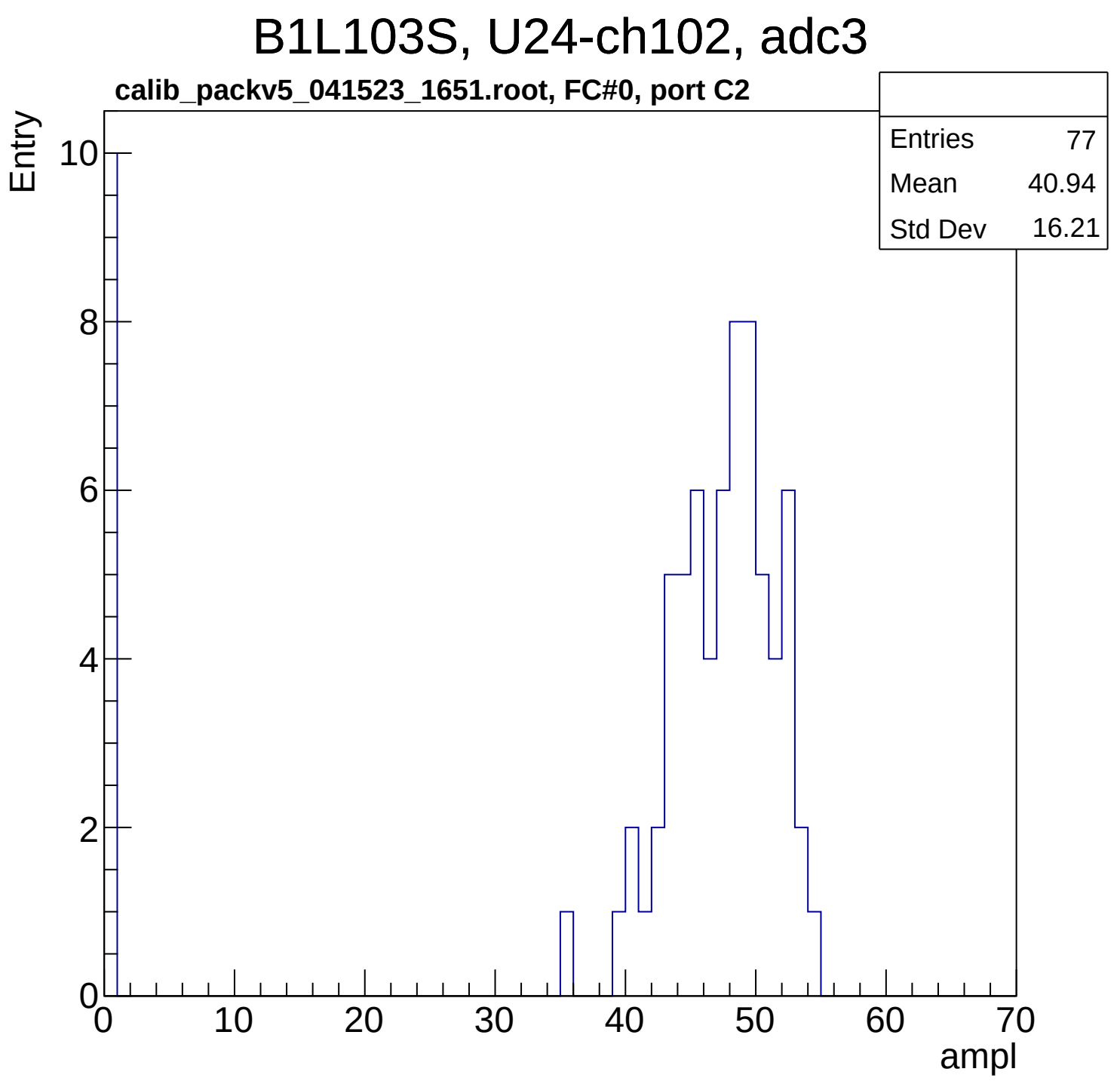
B1L103S, U24-ch102, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 40.94
Std Dev 16.21
Entry
ampl
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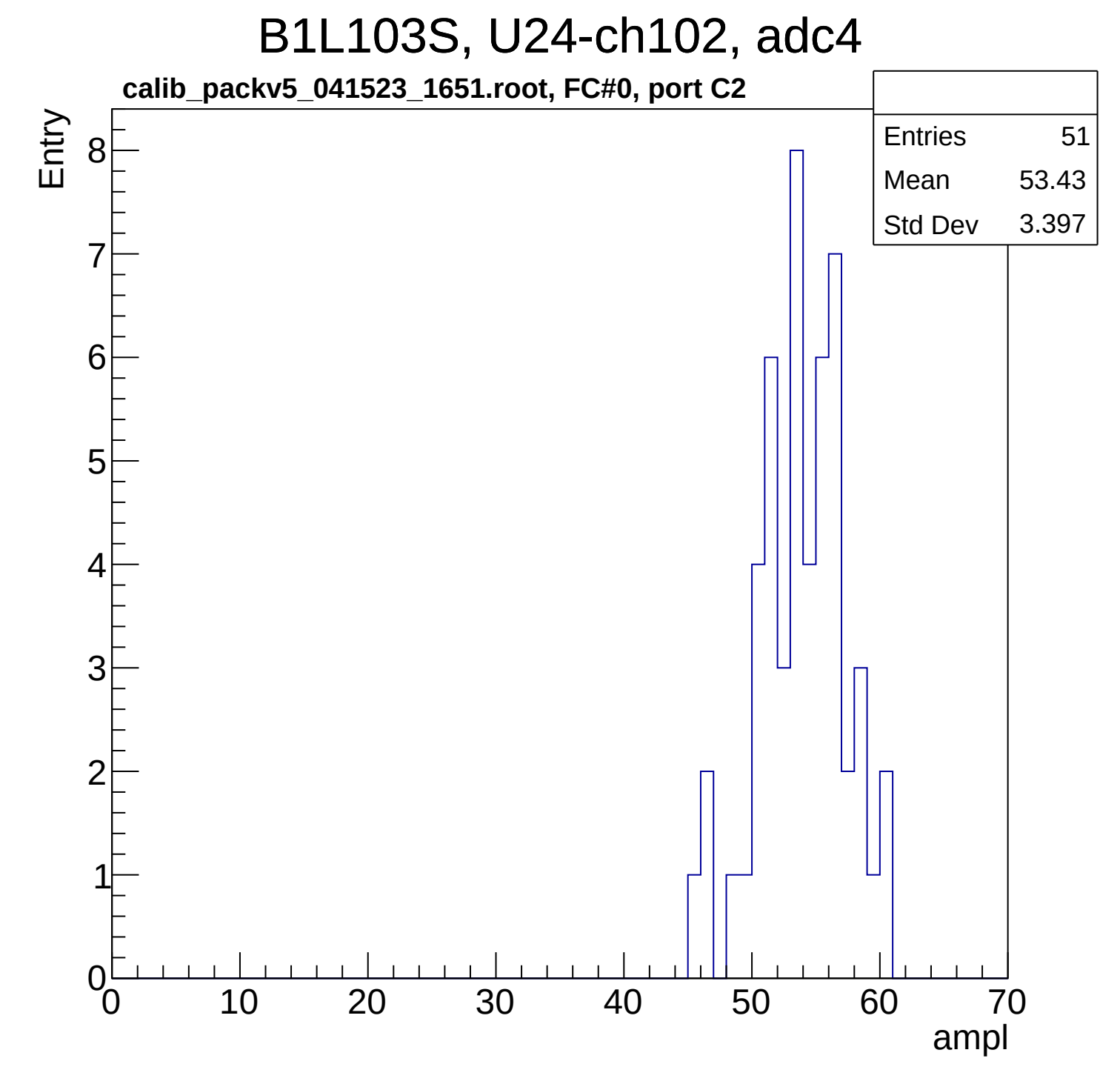
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U24-ch102, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 53.43
Std Dev 3.397
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
30
40
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60
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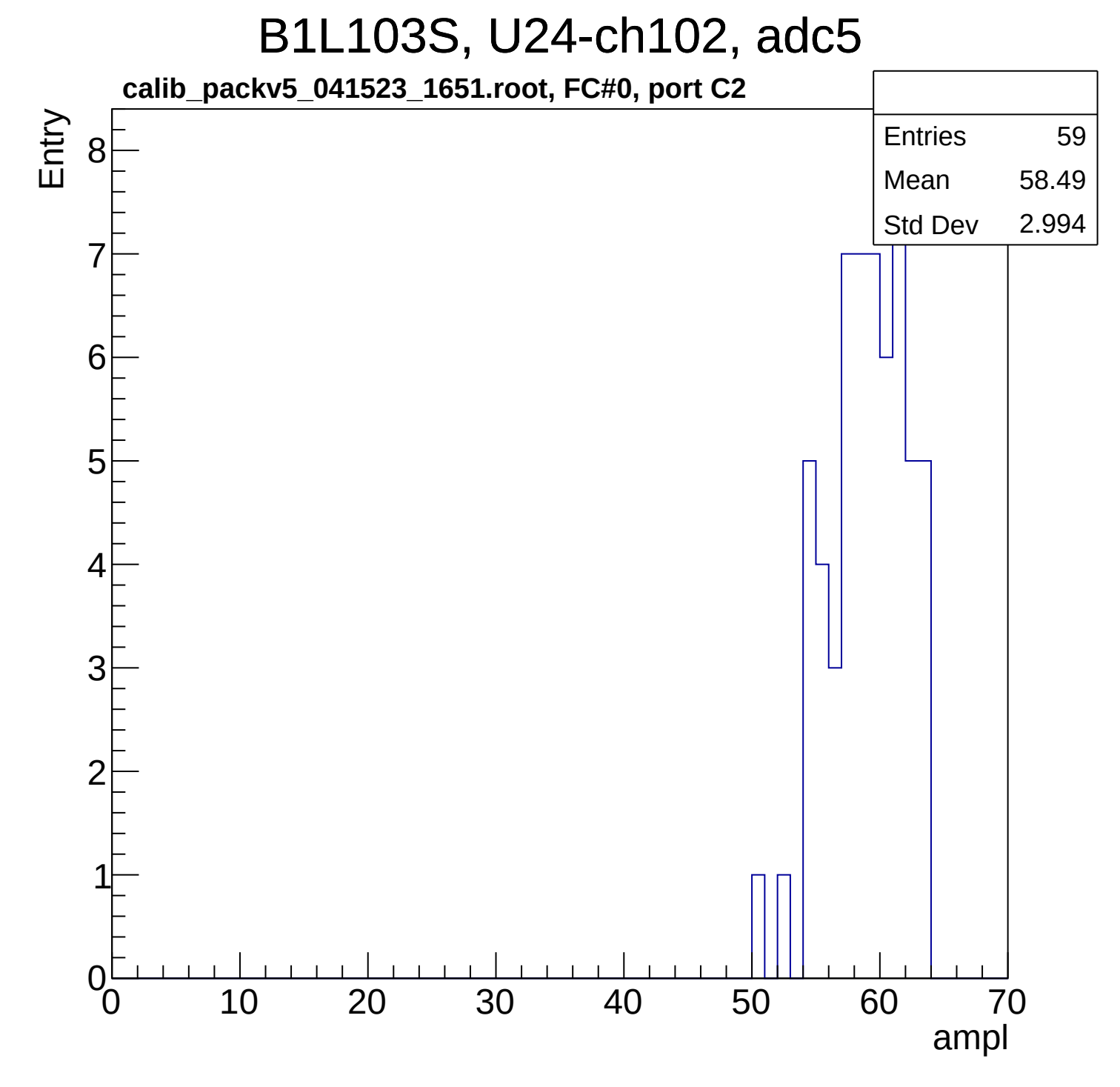
B1L103S, U24-ch102, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 58.49
Std Dev 2.994
Entry
ampl
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2
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5
6
7
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0
10
20
30
40
50
60
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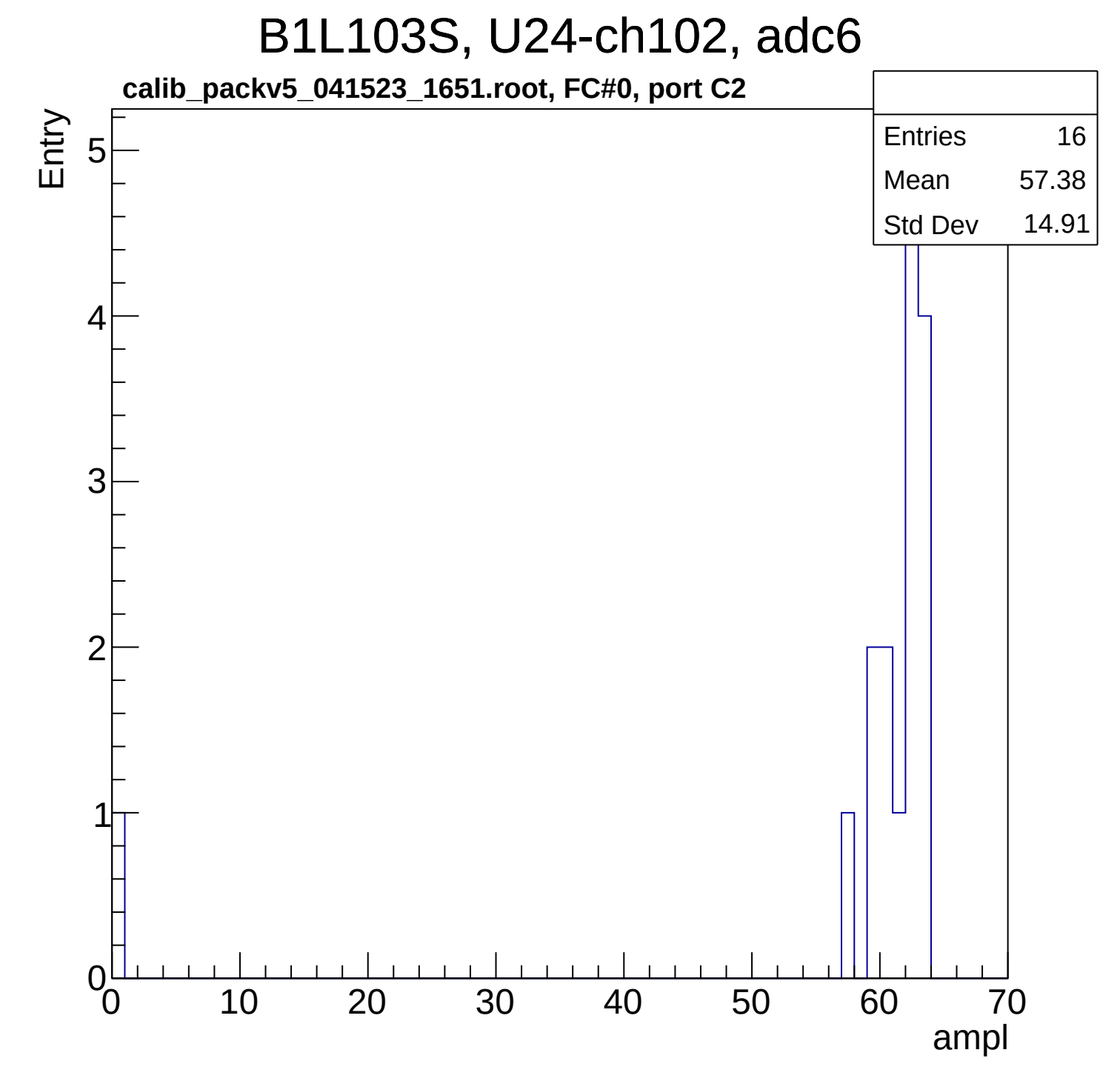
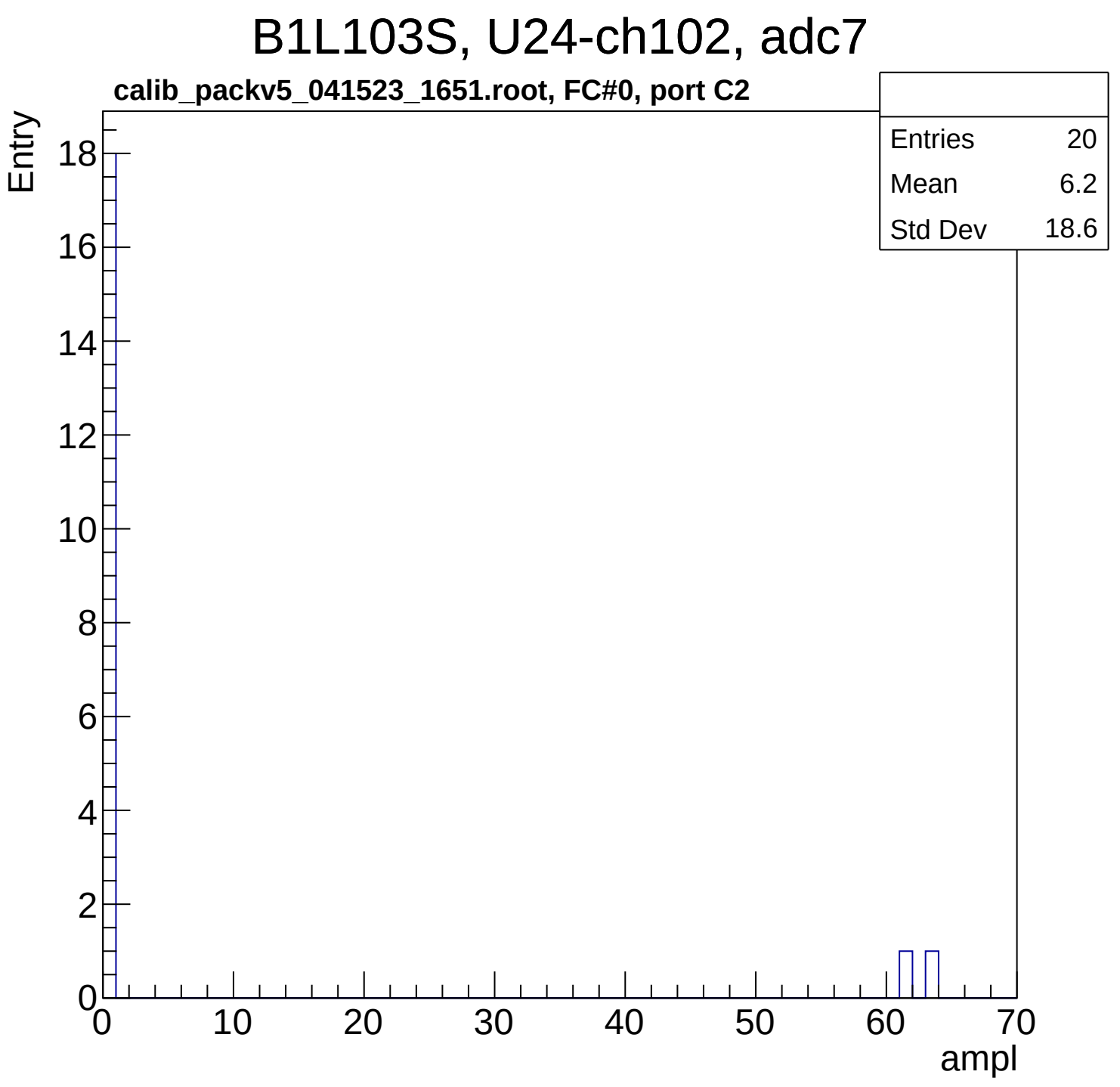

B1L103S, U24-ch102, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 16
Mean 57.38
Std Dev 14.91
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U24-ch102, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 6.2
Std Dev 18.6
Entry
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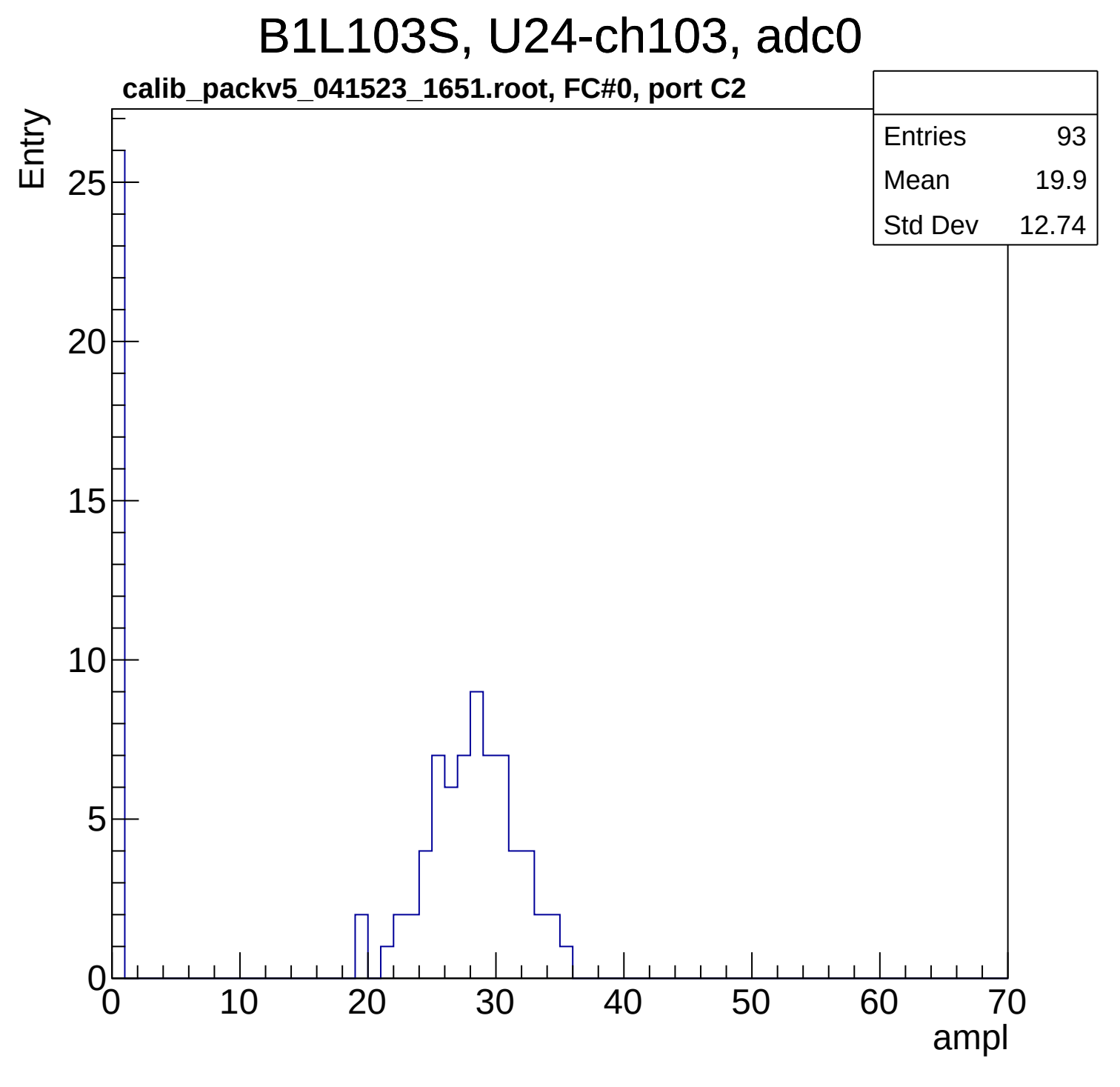
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch103, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 93
Mean 19.9
Std Dev 12.74
Entry
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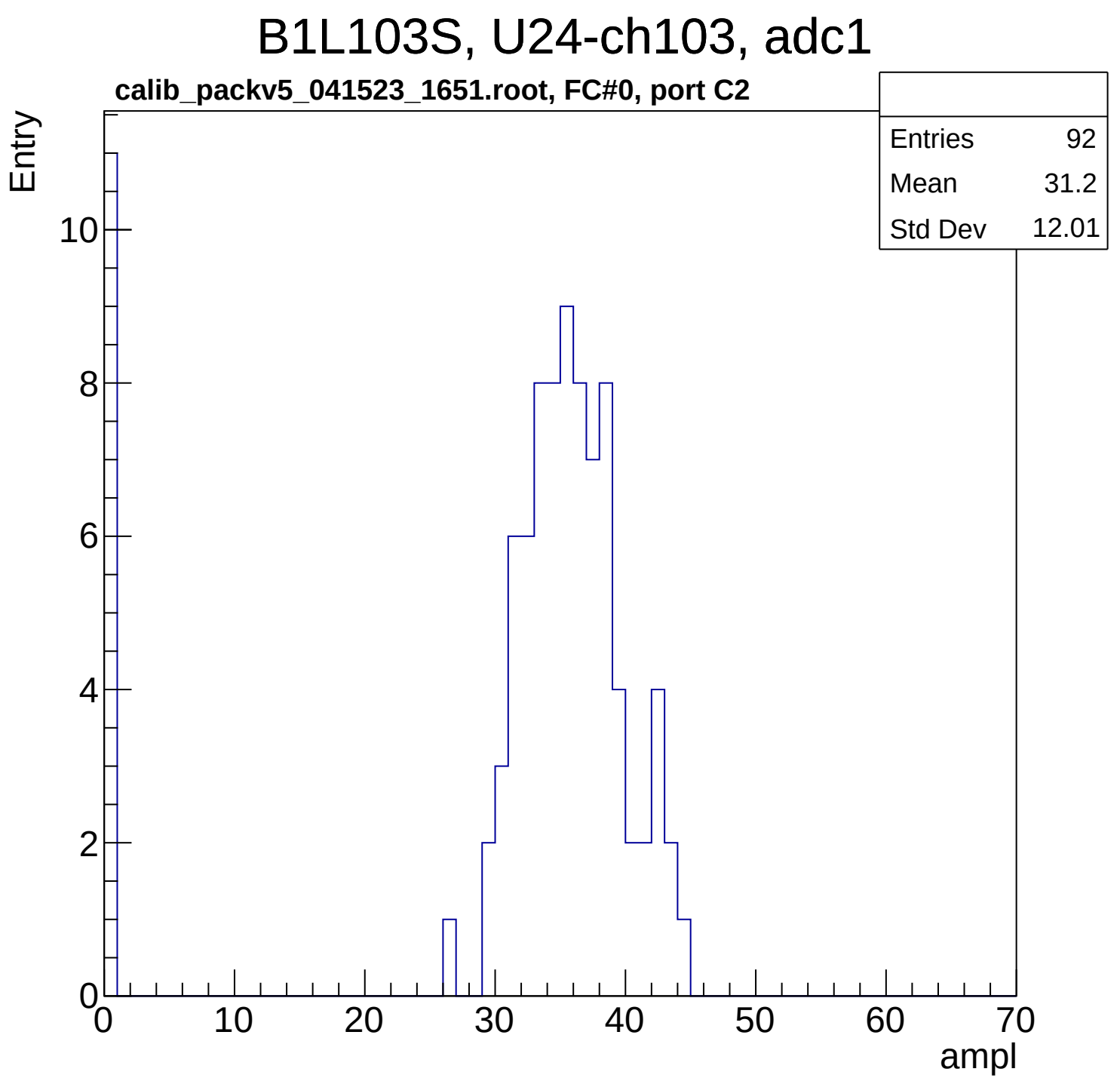
10
15
20
25
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch103, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 92
Mean 31.2
Std Dev 12.01
Entry
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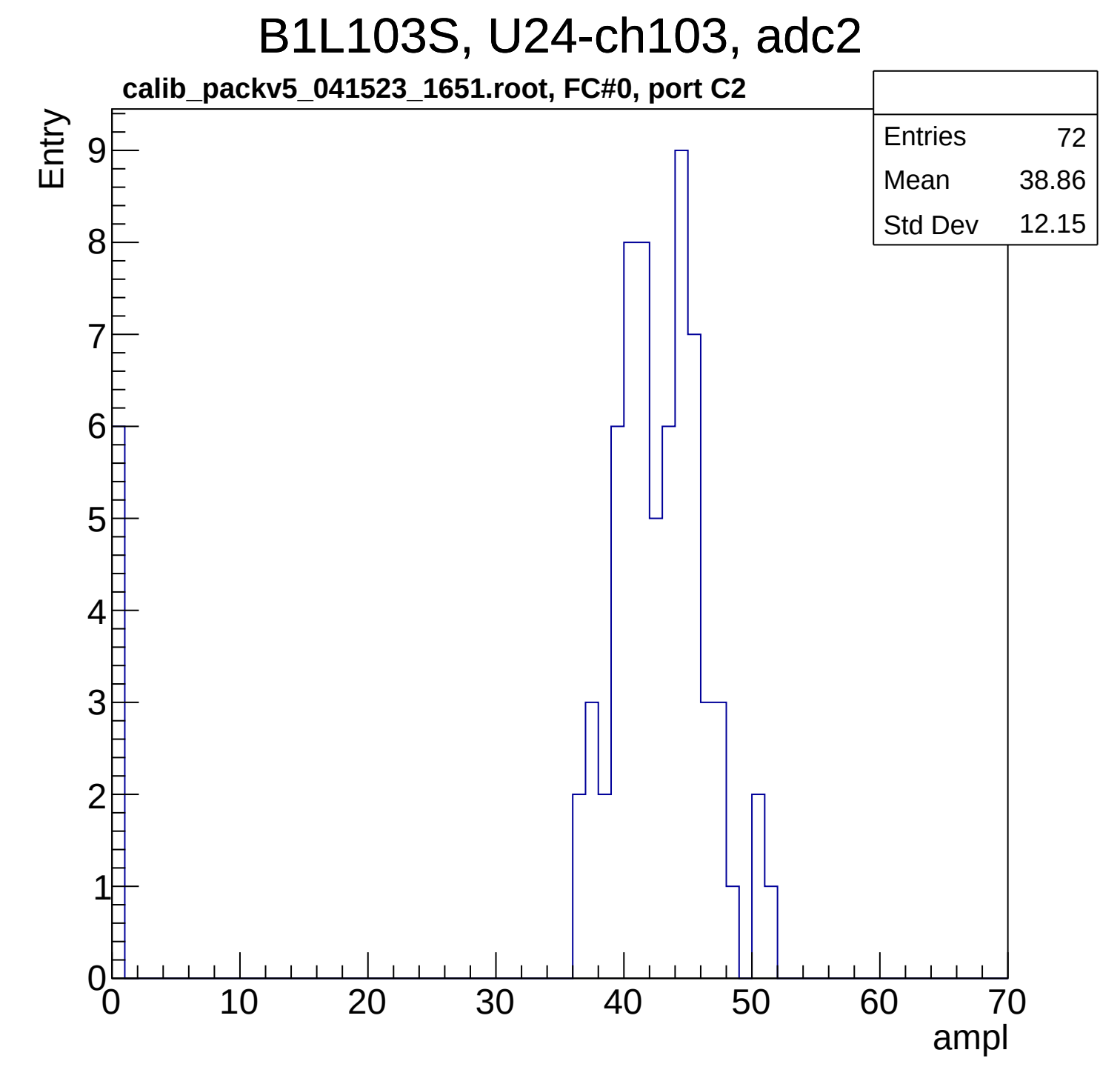
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch103, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 38.86
Std Dev 12.15
Entry
ampl
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3
4
5
6
7
8
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0
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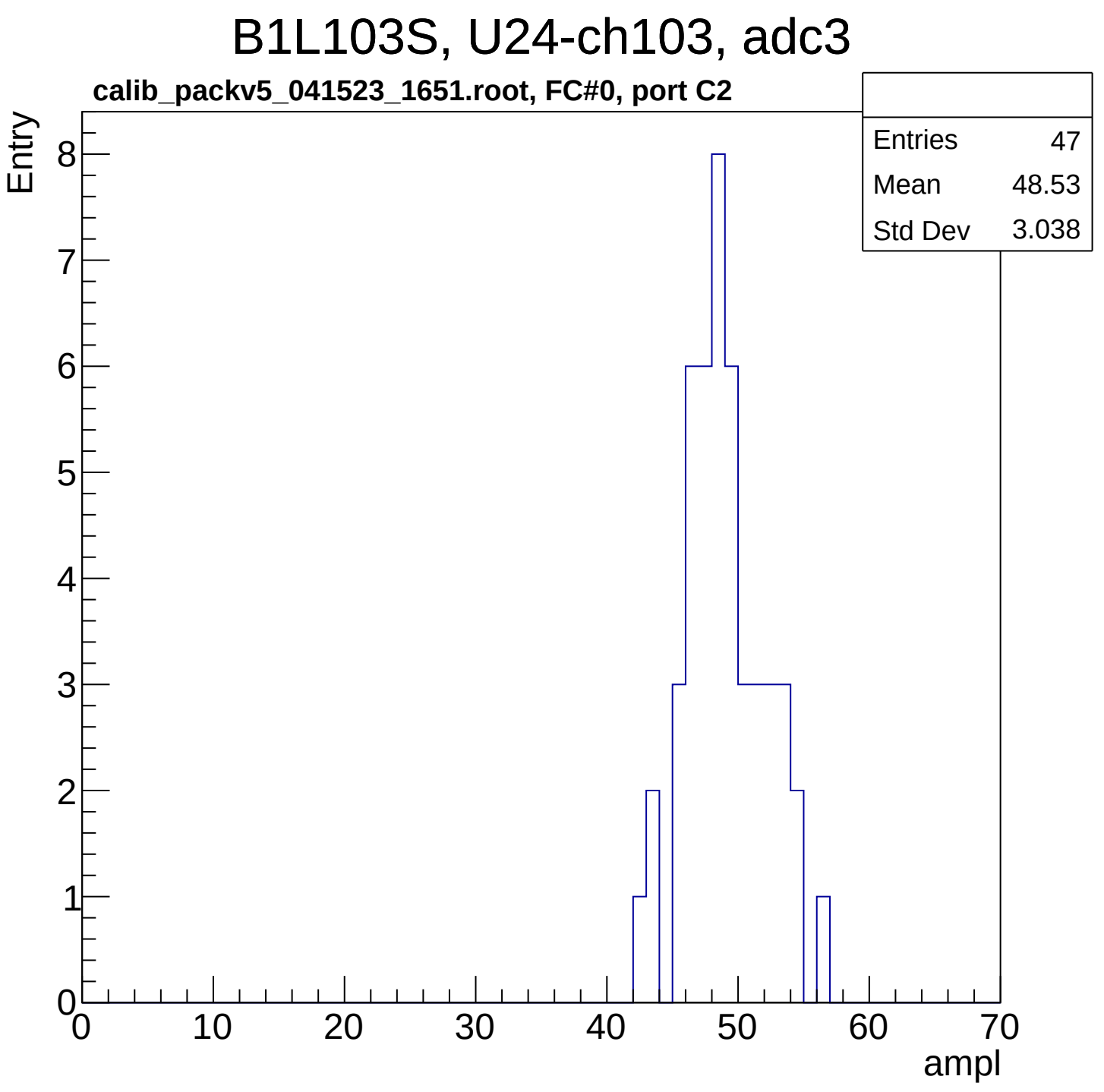
B1L103S, U24-ch103, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 48.53
Std Dev 3.038
Entry
ampl
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2
3
4
5
6
7
8
0
10
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50
60
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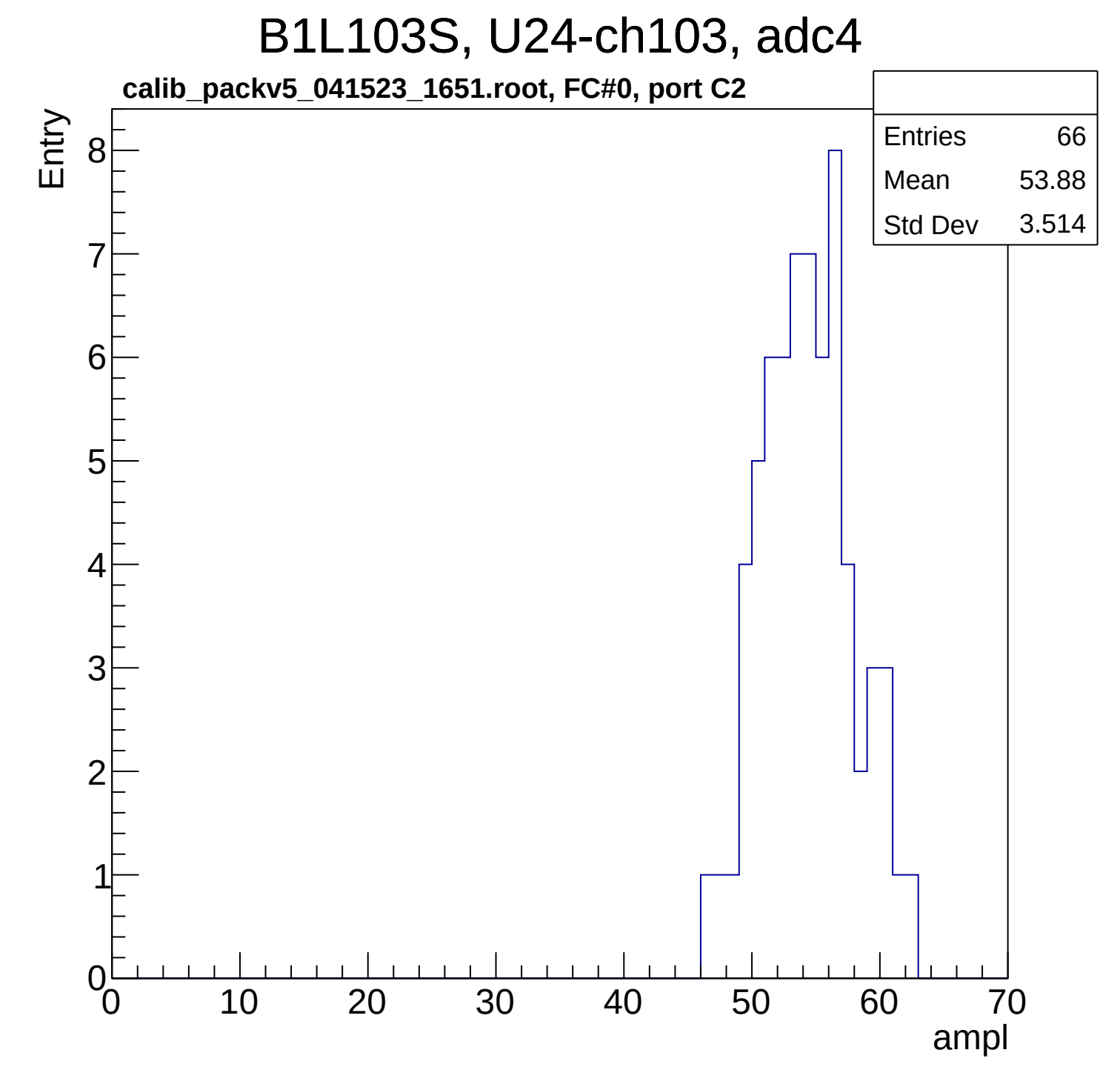
B1L103S, U24-ch103, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 53.88
Std Dev 3.514
Entry
ampl
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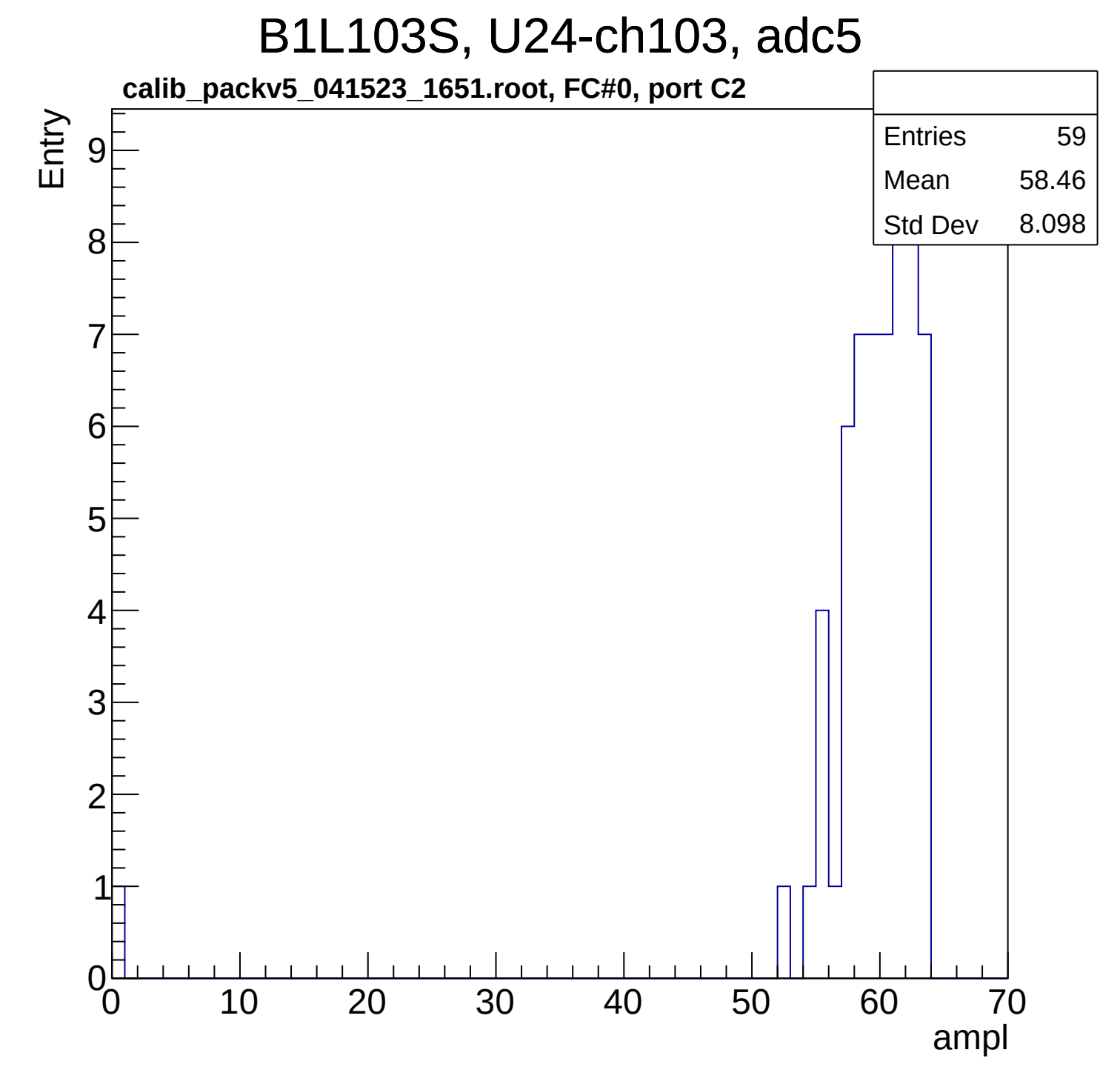
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U24-ch103, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 58.46
Std Dev 8.098
Entry
ampl
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2
3
4
5
6
7
8
9
0
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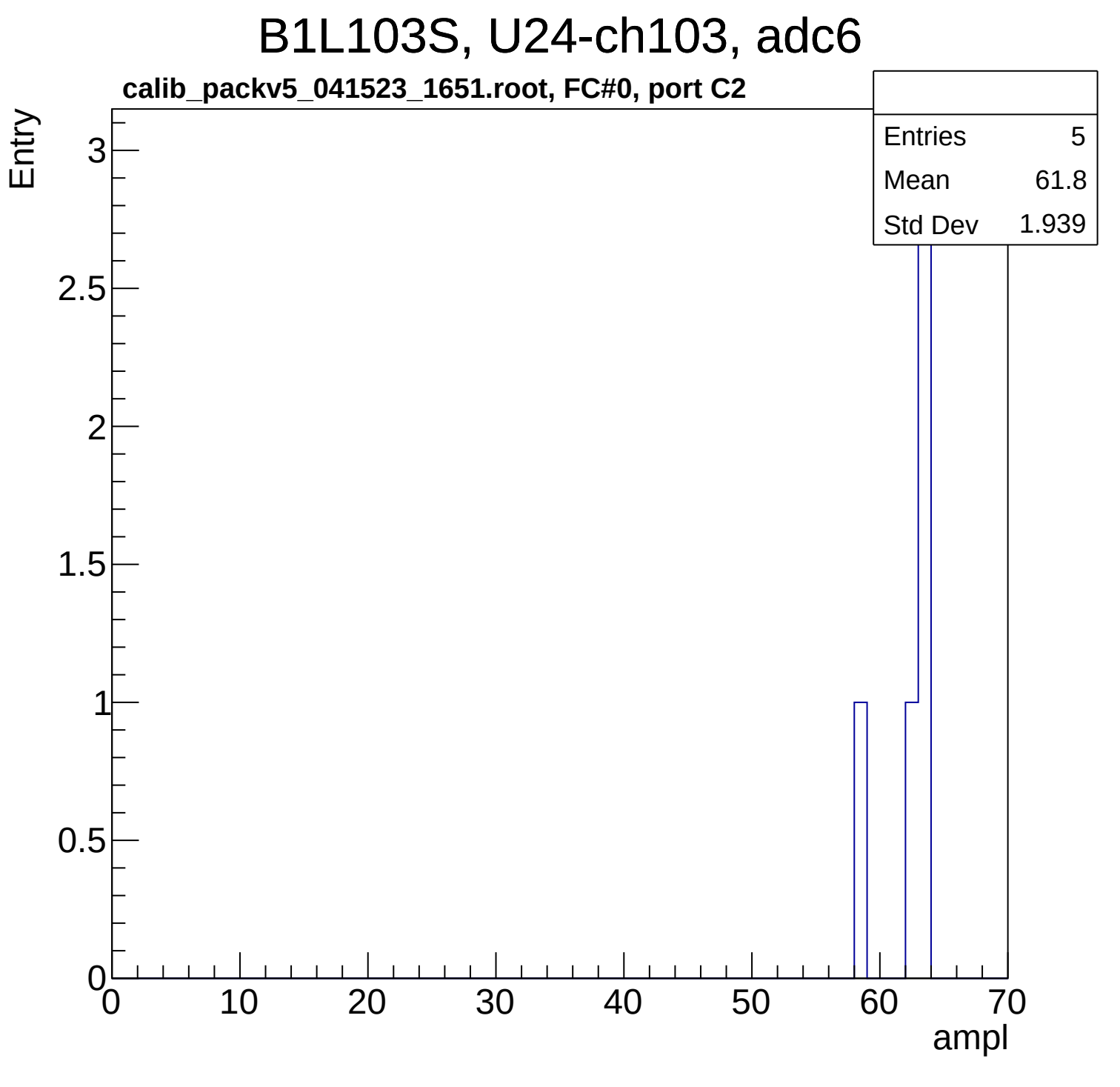
B1L103S, U24-ch103, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 5
Mean 61.8
Std Dev 1.939
Entry
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1
1.5
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2.5
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0
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20
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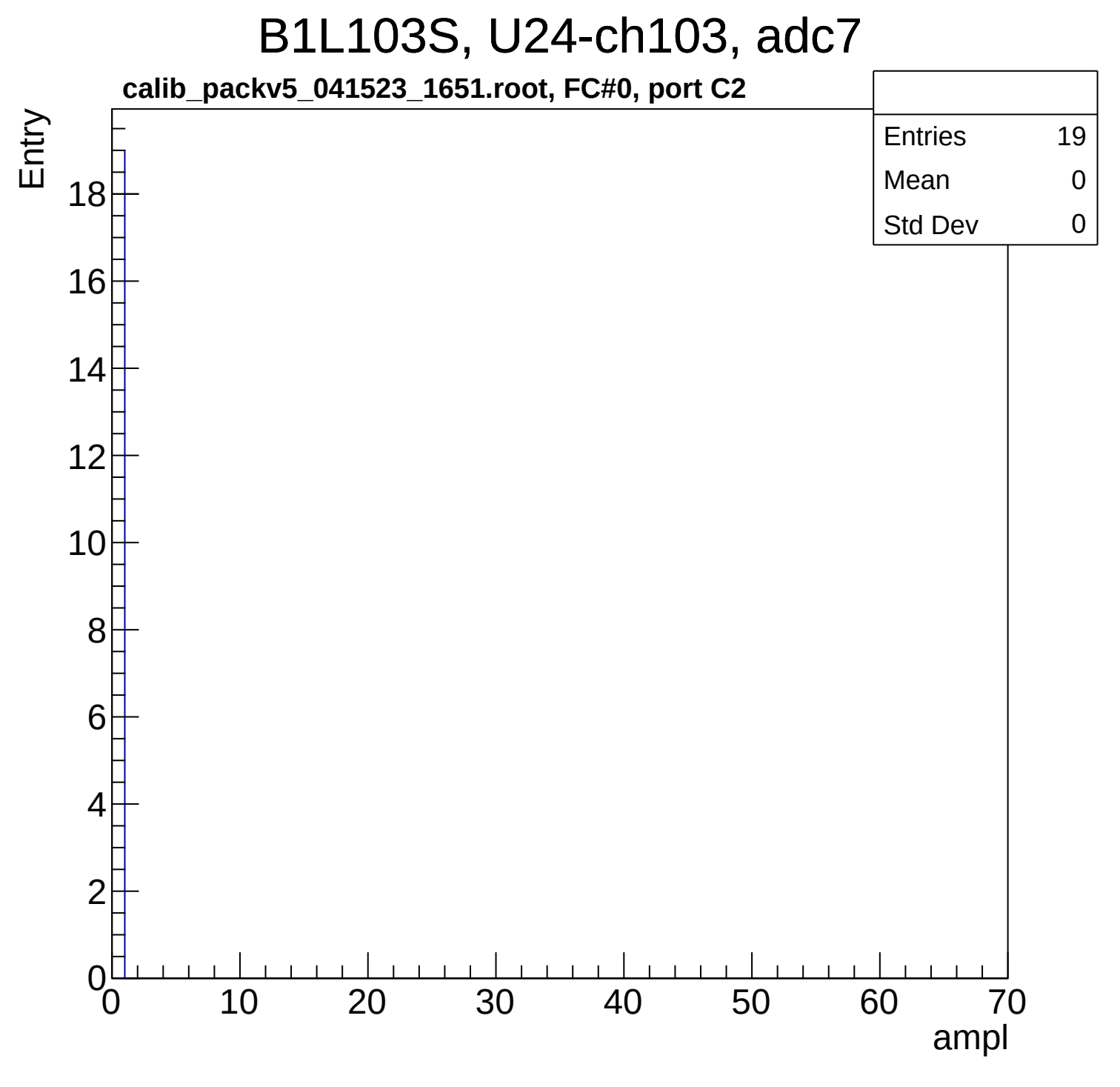
B1L103S, U24-ch103, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
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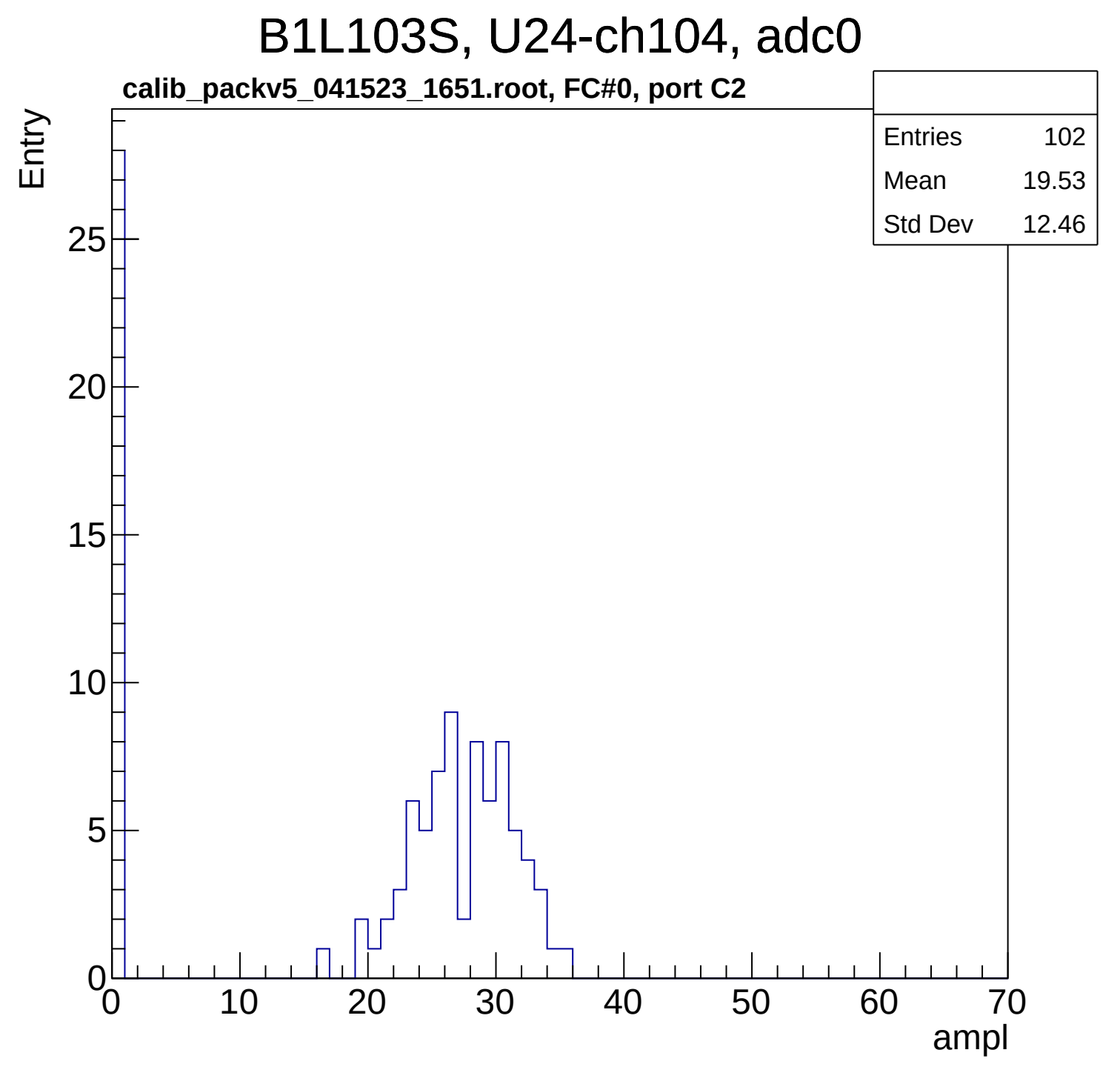
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch104, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 102
Mean 19.53
Std Dev 12.46
Entry
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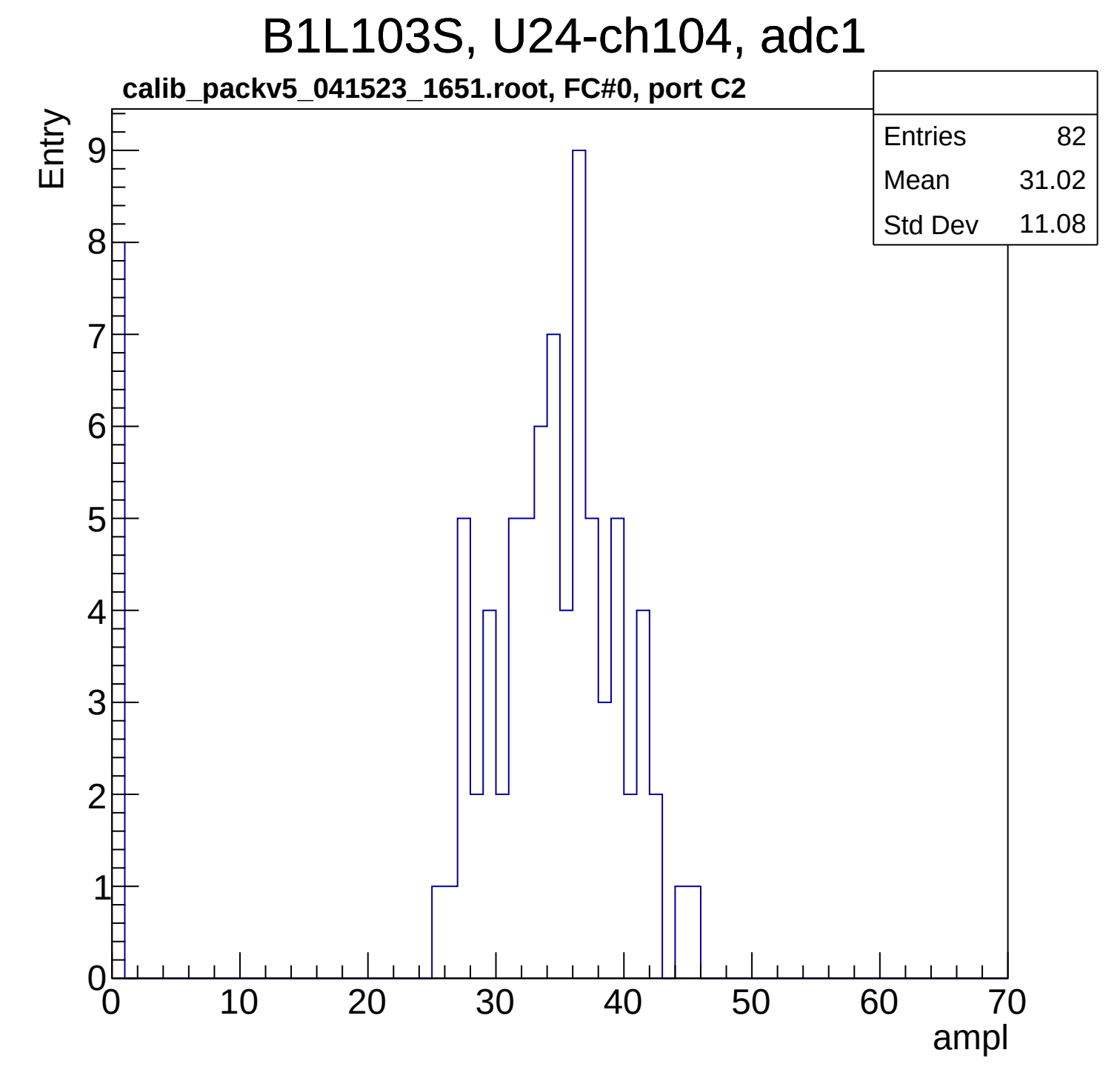
10
15
20
25
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch104, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 31.02
Std Dev 11.08
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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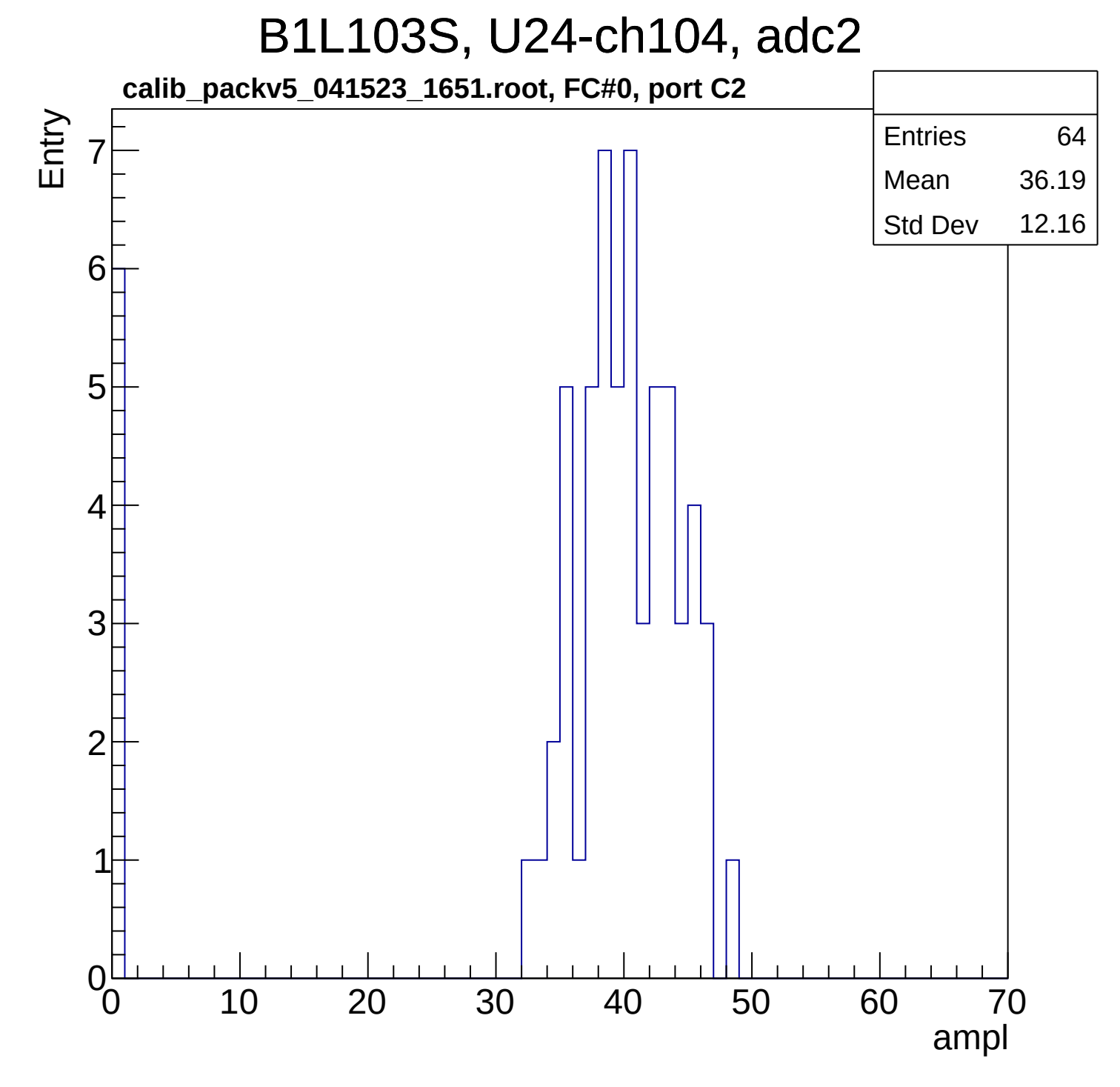
40
50
60
70


B1L103S, U24-ch104, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 36.19
Std Dev 12.16
Entry
ampl
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1
2
3
4
5
6
7
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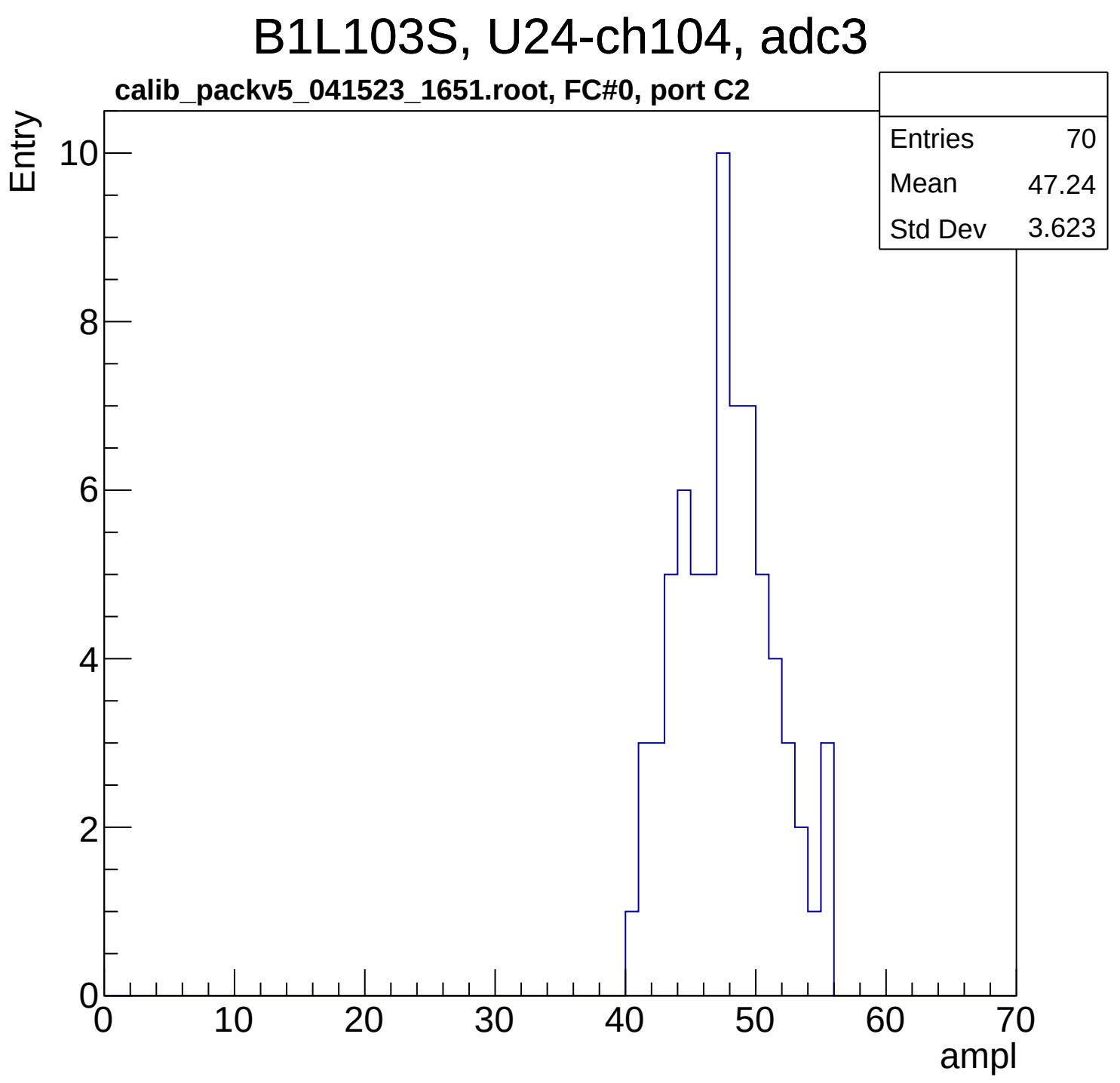
10
20
30
40
50
60
70


B1L103S, U24-ch104, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 47.24
Std Dev 3.623
Entry
ampl
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20
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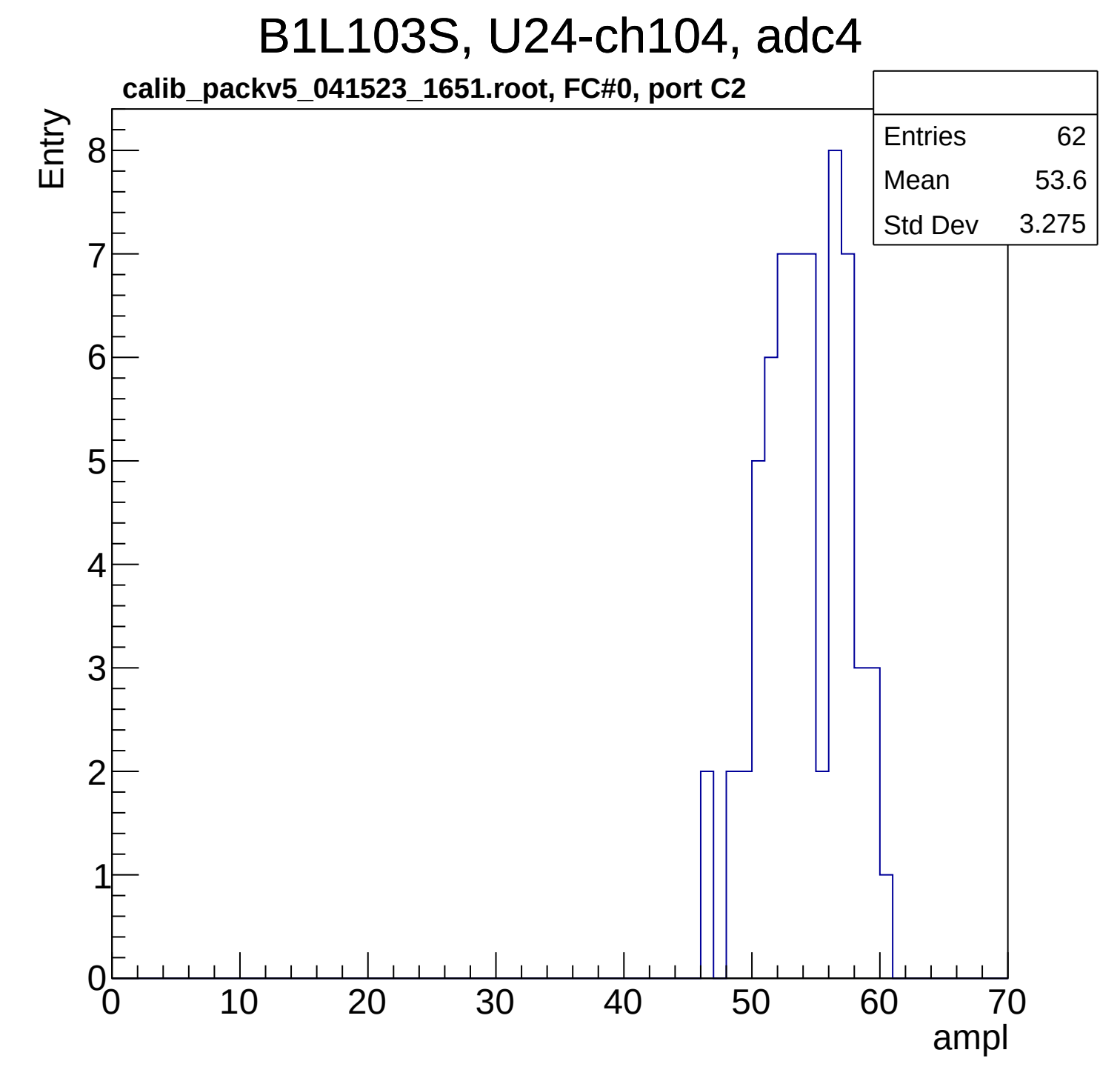
50
60
70


B1L103S, U24-ch104, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 53.6
Std Dev 3.275
Entry
ampl
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40
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60
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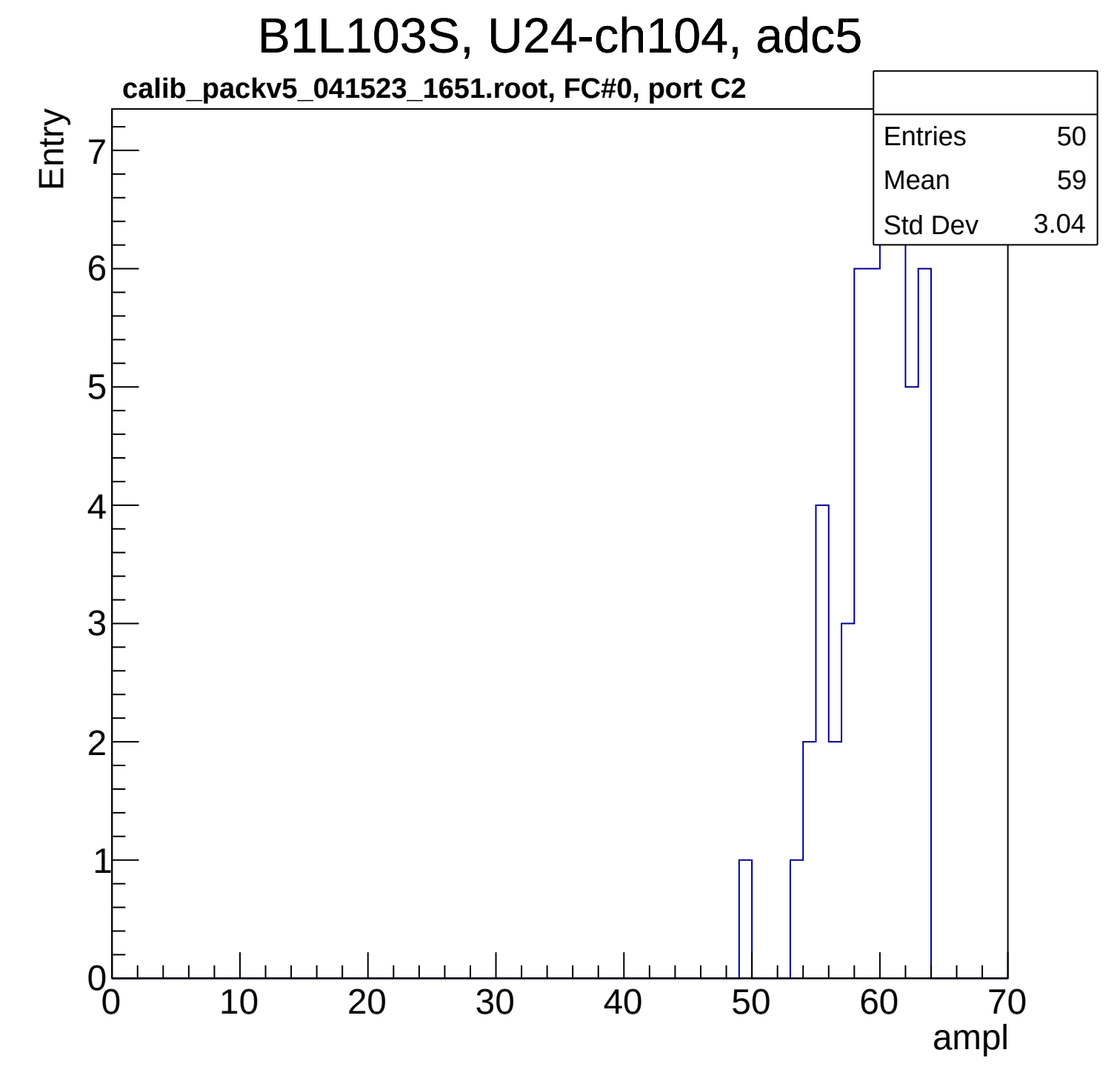
B1L103S, U24-ch104, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 59
Std Dev 3.04
Entry
ampl
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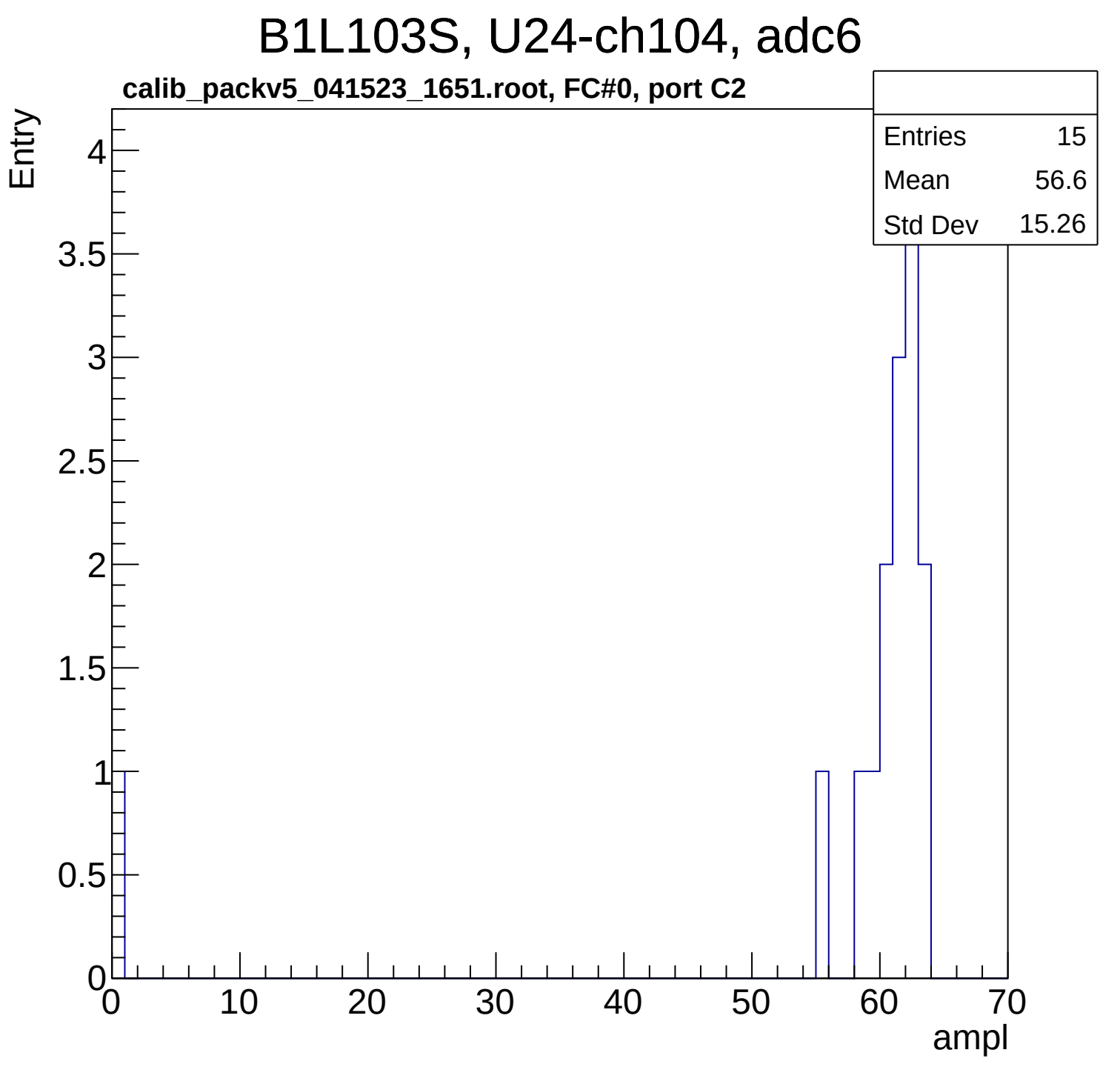
B1L103S, U24-ch104, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 15
Mean 56.6
Std Dev 15.26
Entry
ampl
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1.5
2
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3.5
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0
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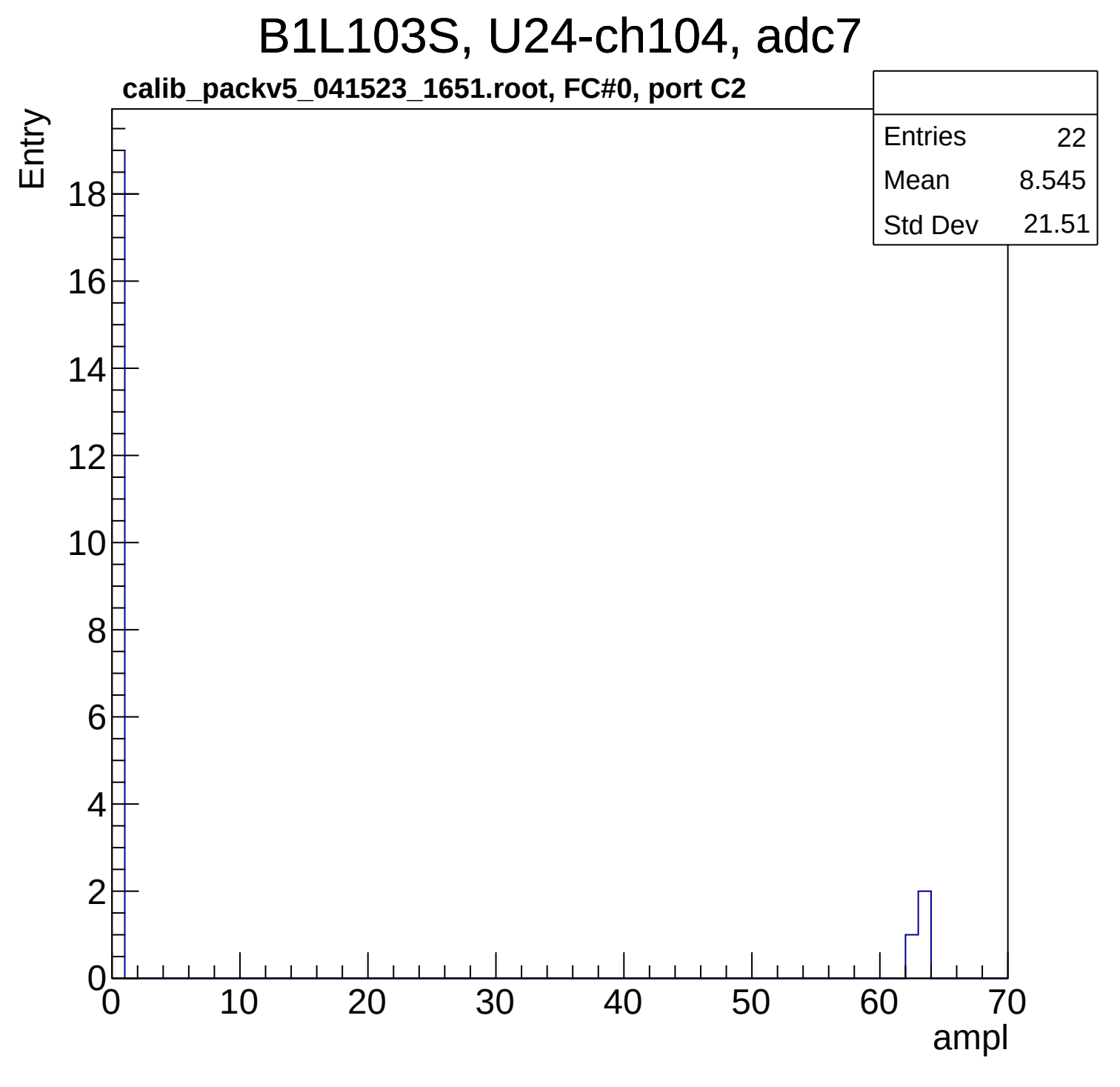
B1L103S, U24-ch104, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 8.545
Std Dev 21.51
Entry
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6
8
10
12
14
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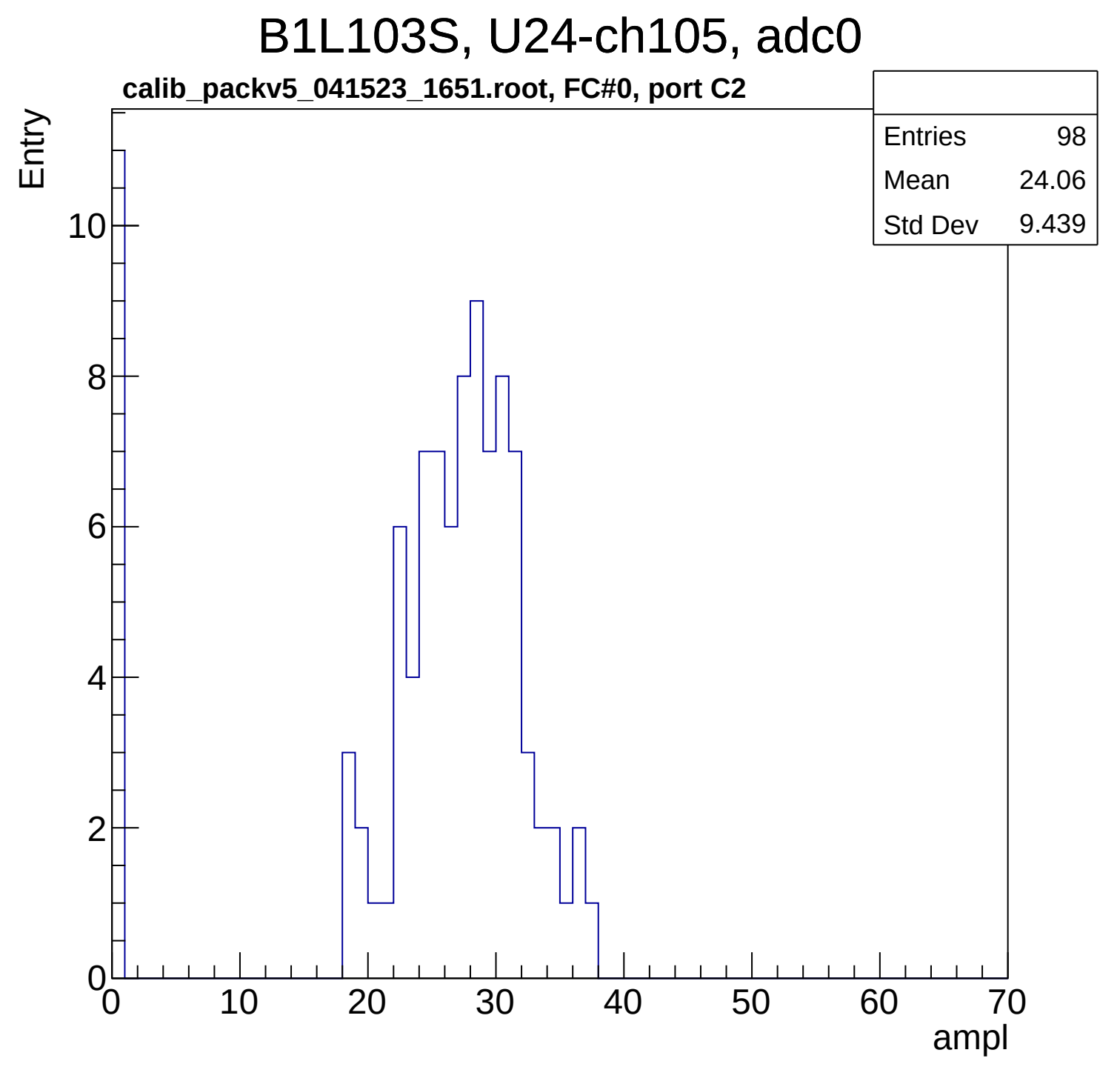
70
ampl


B1L103S, U24-ch105, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 98
Mean 24.06
Std Dev 9.439
Entry
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4
6
8
10
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10
20
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50
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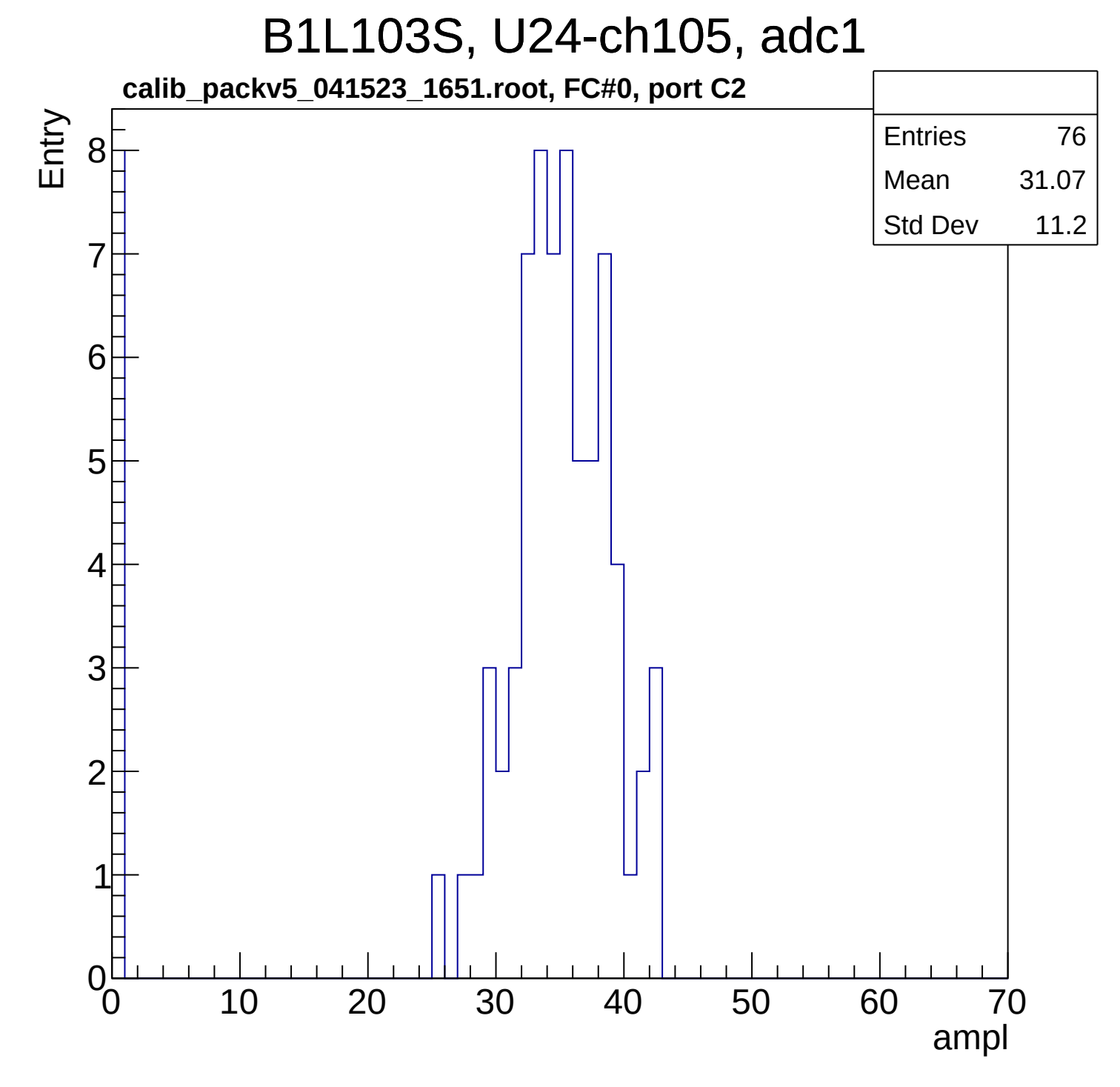
70
ampl


B1L103S, U24-ch105, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 31.07
Std Dev 11.2
Entry
ampl
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1
2
3
4
5
6
7
8
0
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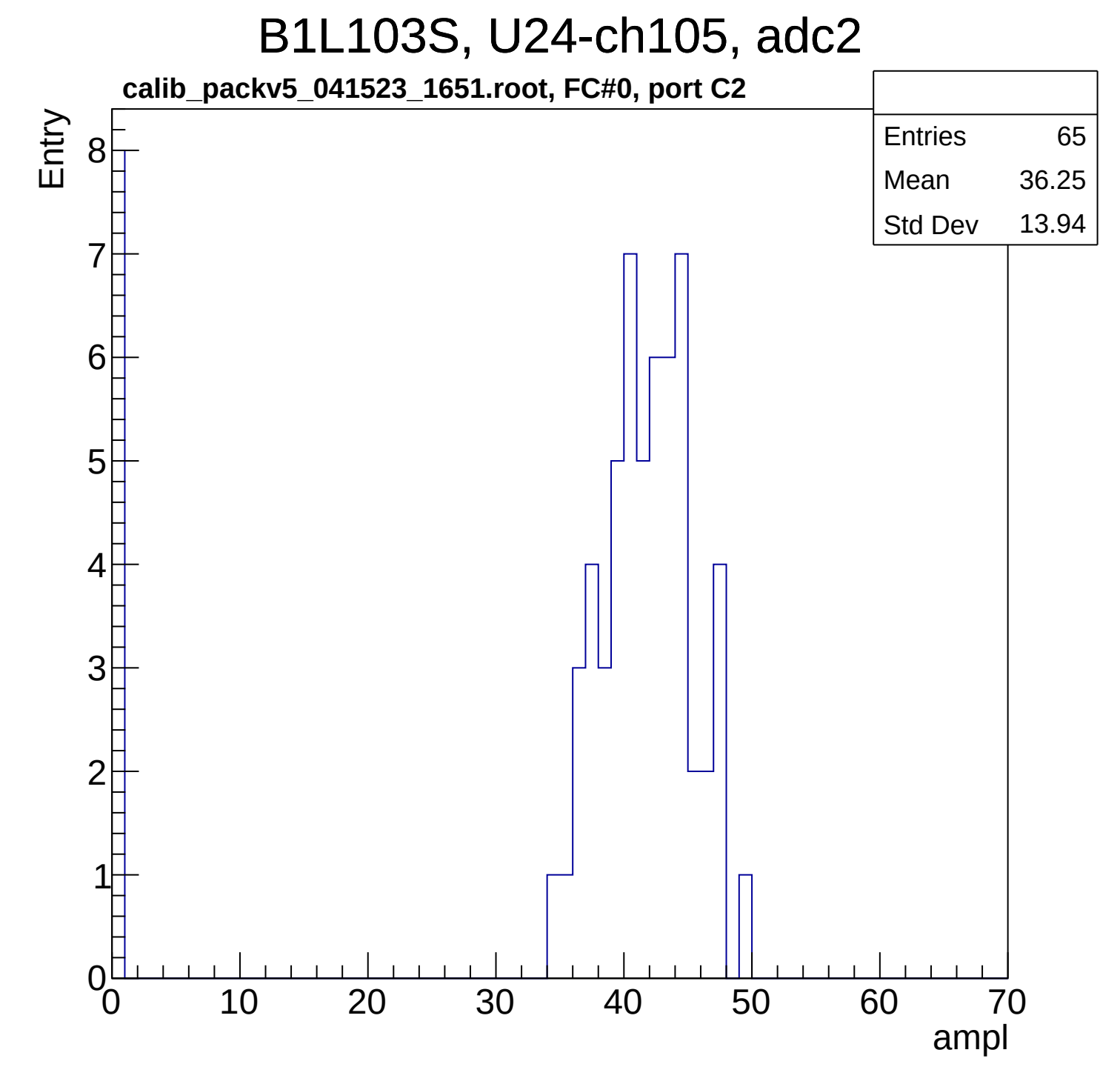
B1L103S, U24-ch105, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 36.25
Std Dev 13.94
Entry
ampl
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2
3
4
5
6
7
8
0
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40
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60
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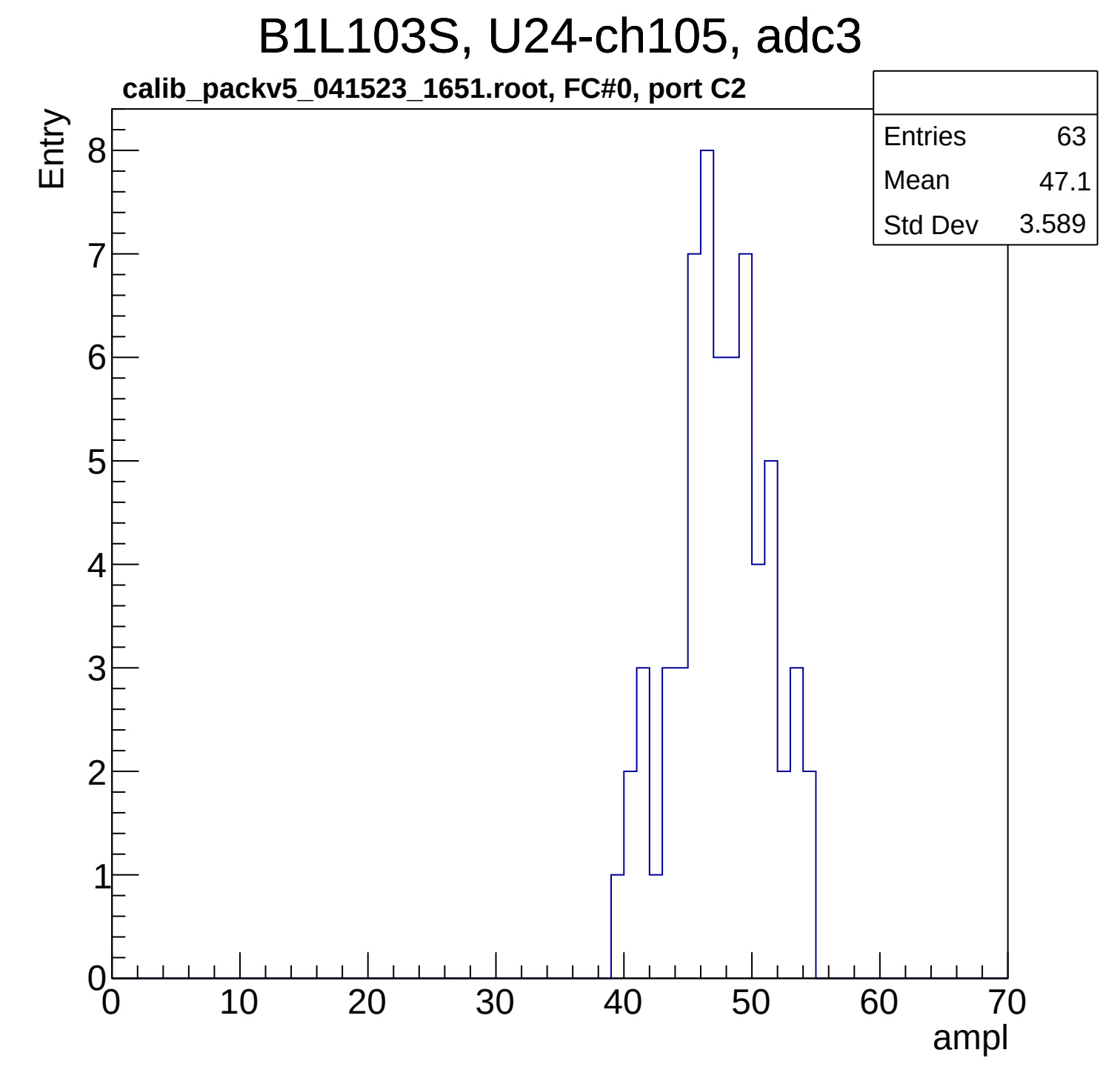
B1L103S, U24-ch105, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 47.1
Std Dev 3.589
Entry
ampl
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2
3
4
5
6
7
8
0
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20
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40
50
60
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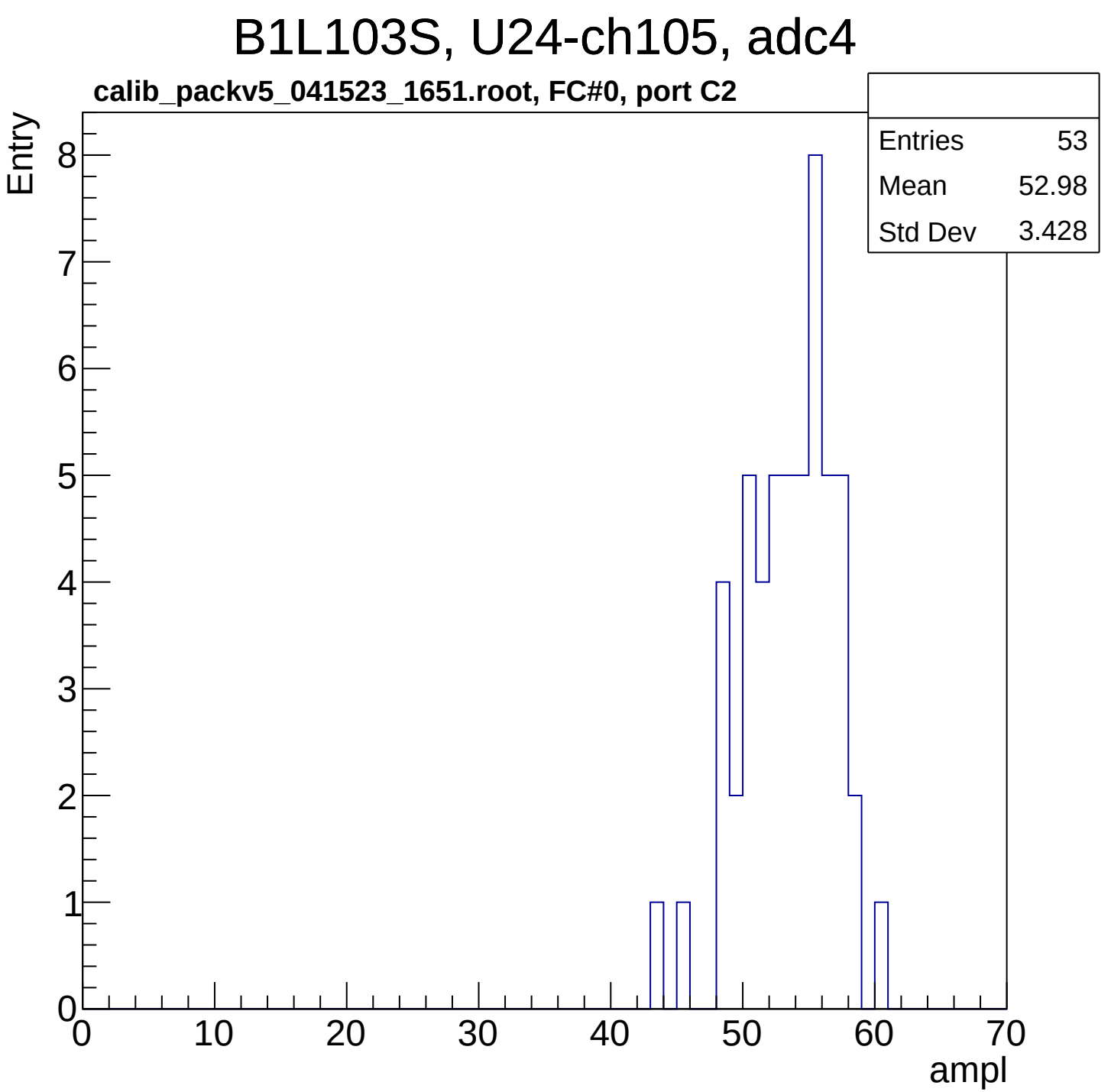
B1L103S, U24-ch105, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 52.98
Std Dev 3.428
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
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60
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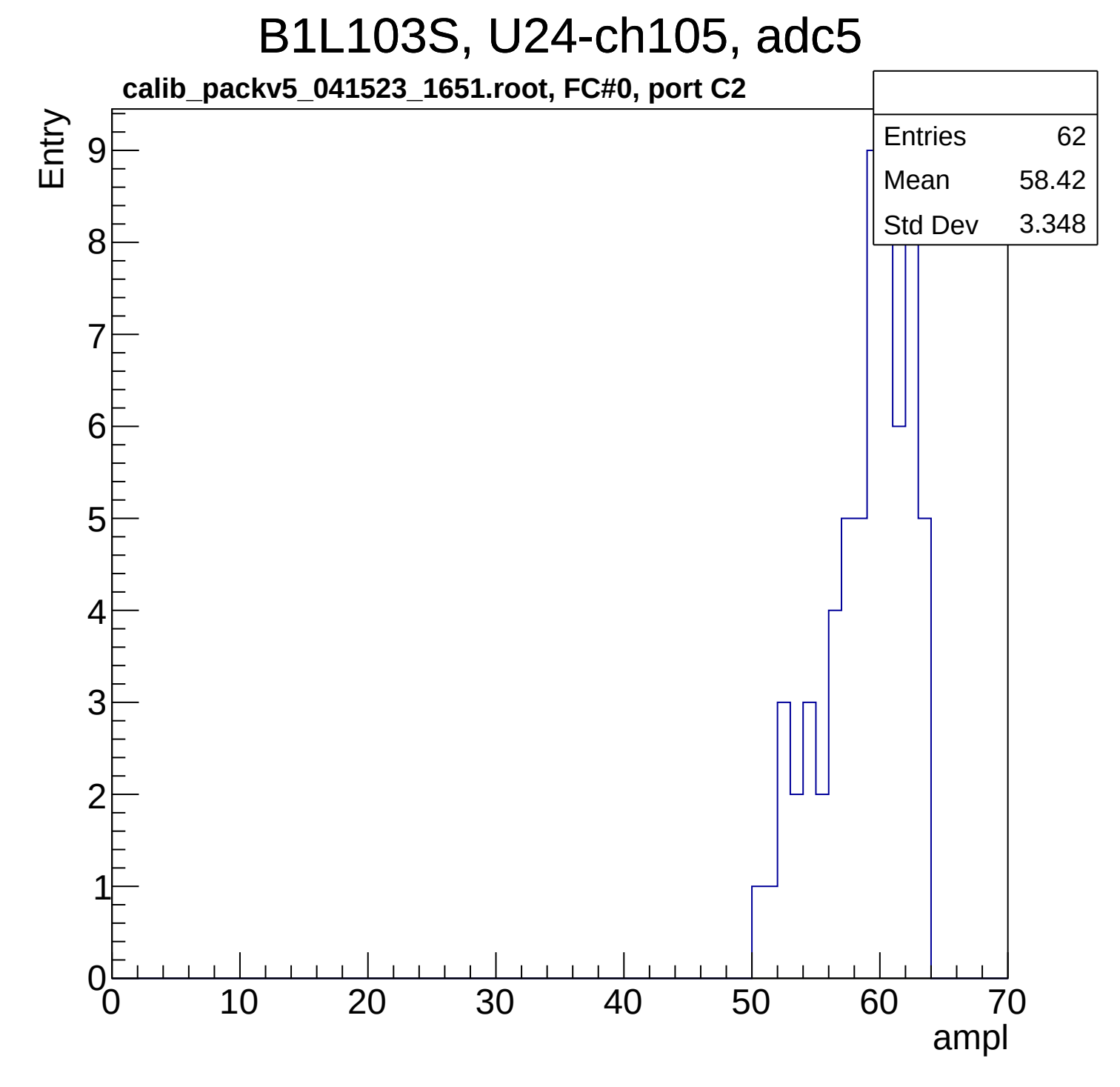
B1L103S, U24-ch105, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 58.42
Std Dev 3.348
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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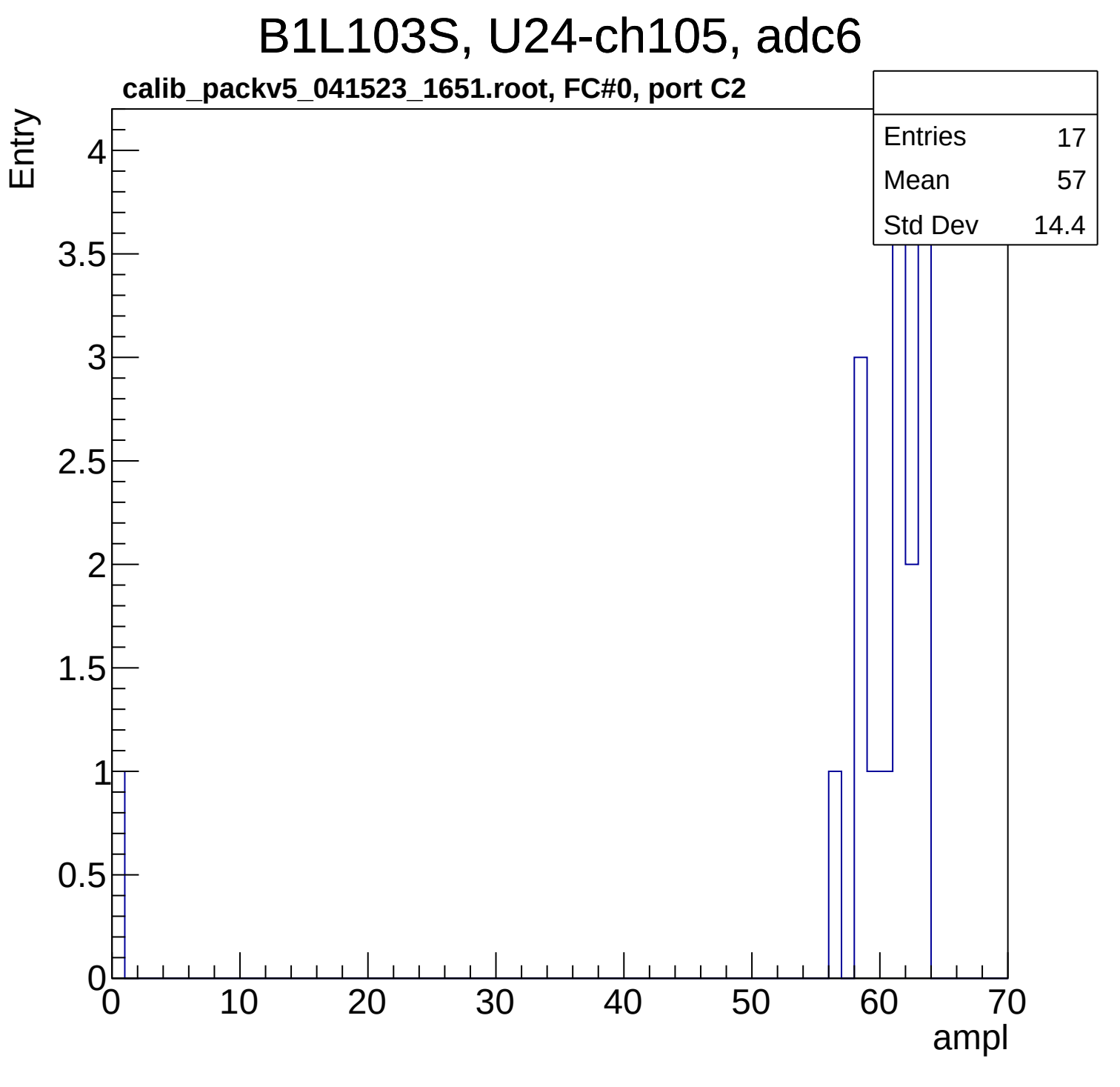
B1L103S, U24-ch105, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 17
Mean 57
Std Dev 14.4
Entry
ampl
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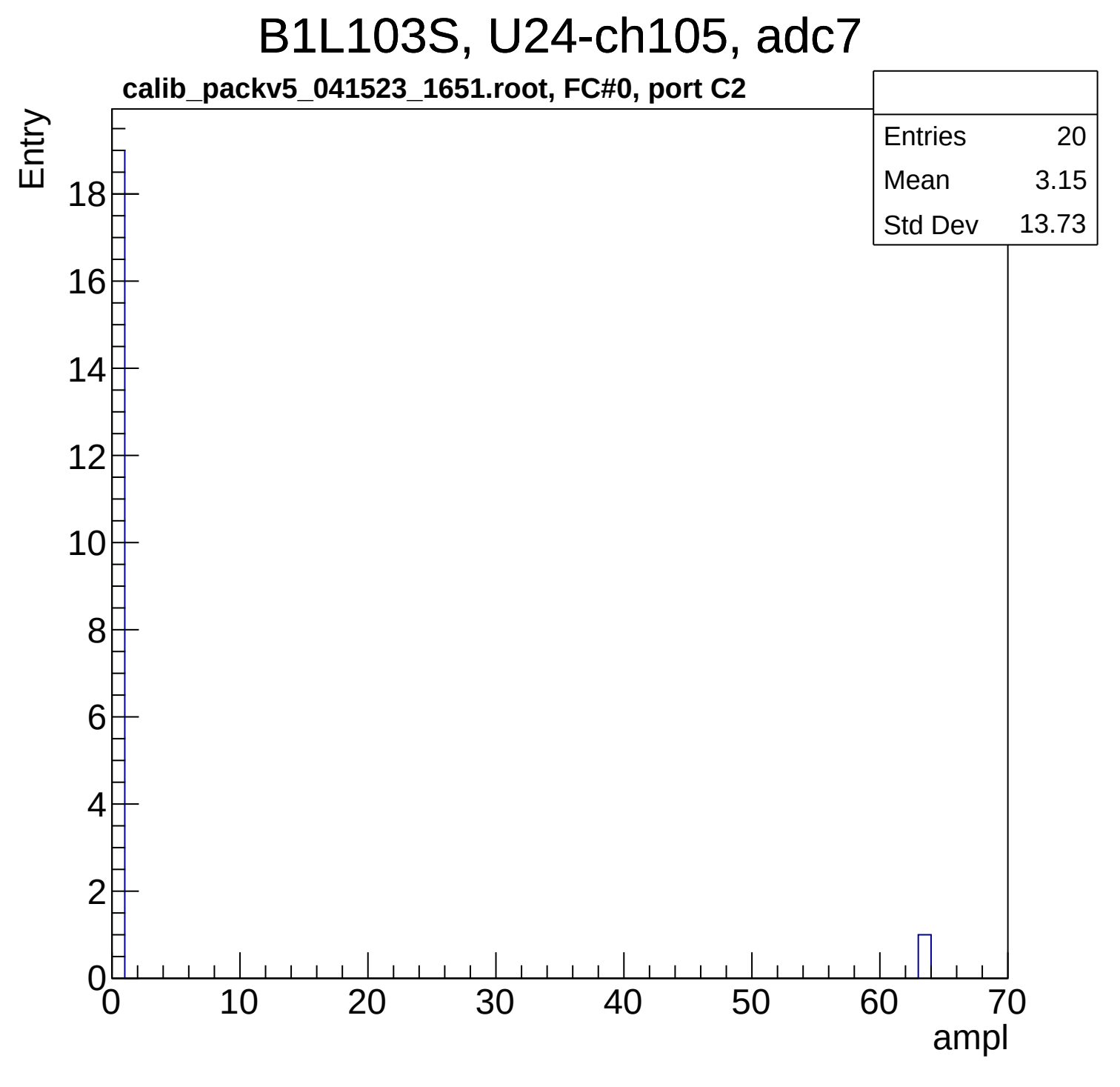
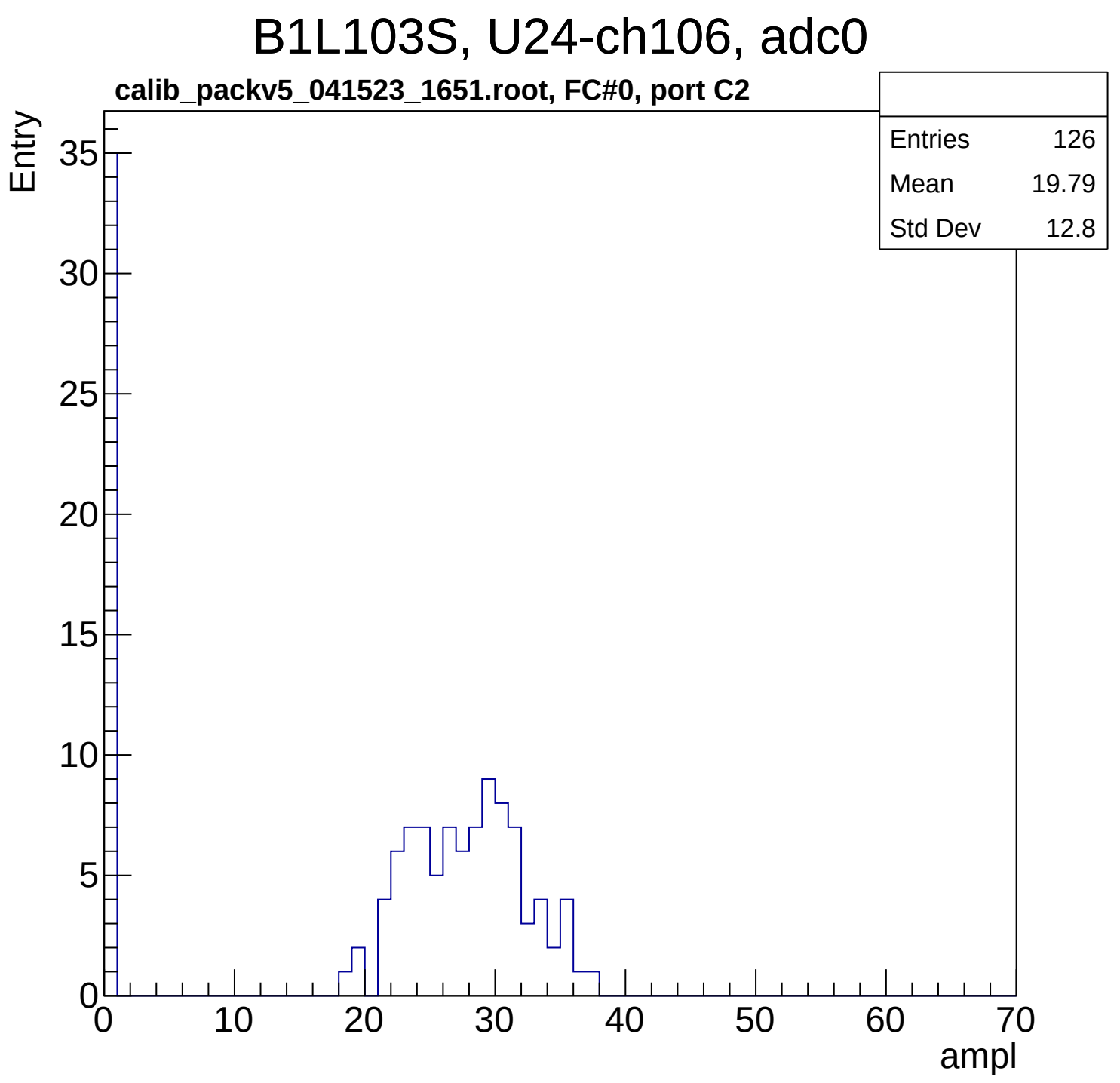
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U24-ch105, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch106, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 126
Mean 19.79
Std Dev 12.8
Entry
ampl
0
5
10
15
20
25
30
35
0
10
20
30
40
50
60
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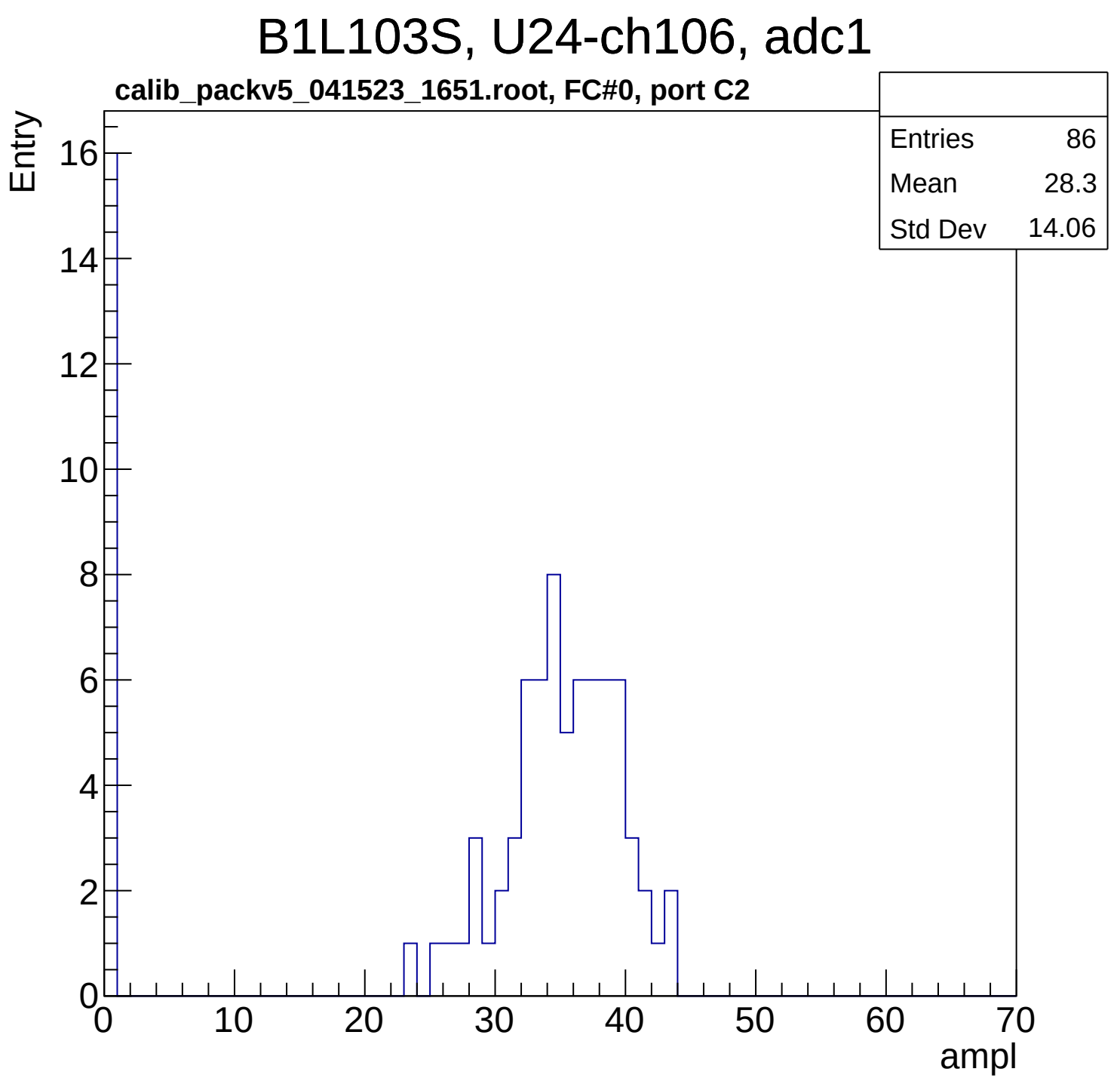
B1L103S, U24-ch106, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 28.3
Std Dev 14.06
Entry
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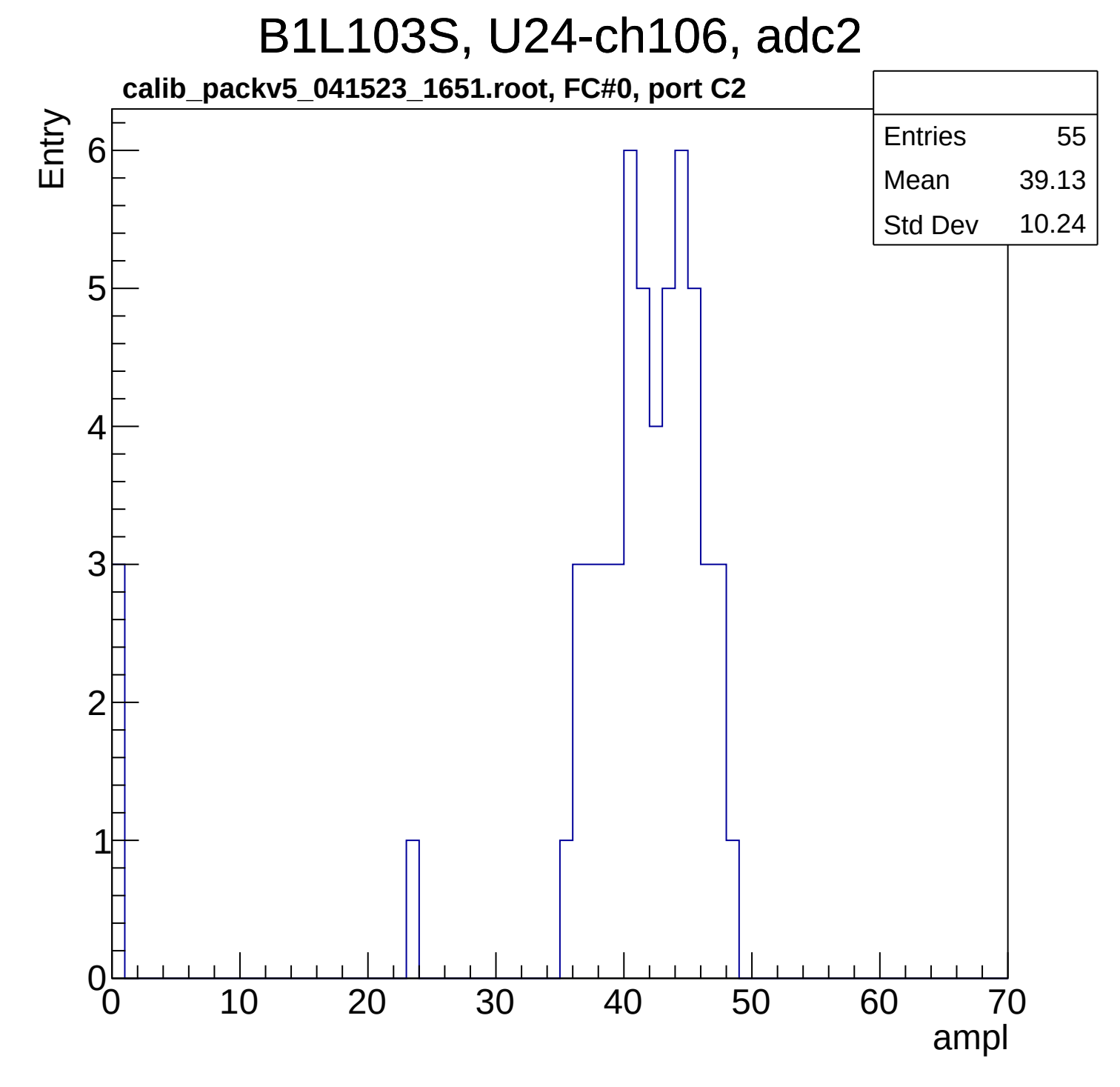
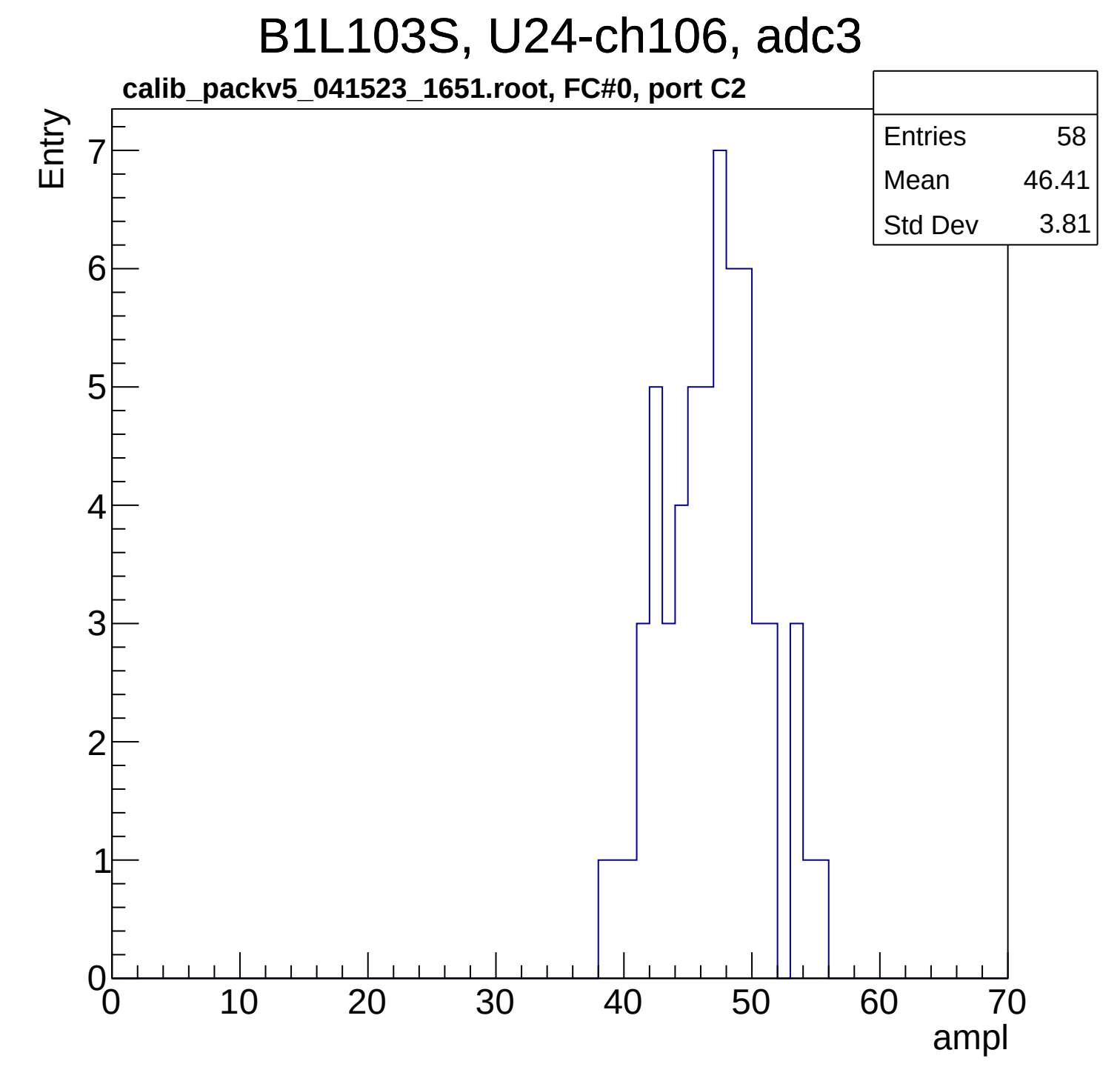
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch106, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 39.13
Std Dev 10.24
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch106, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 46.41
Std Dev 3.81
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
30
40
50
60
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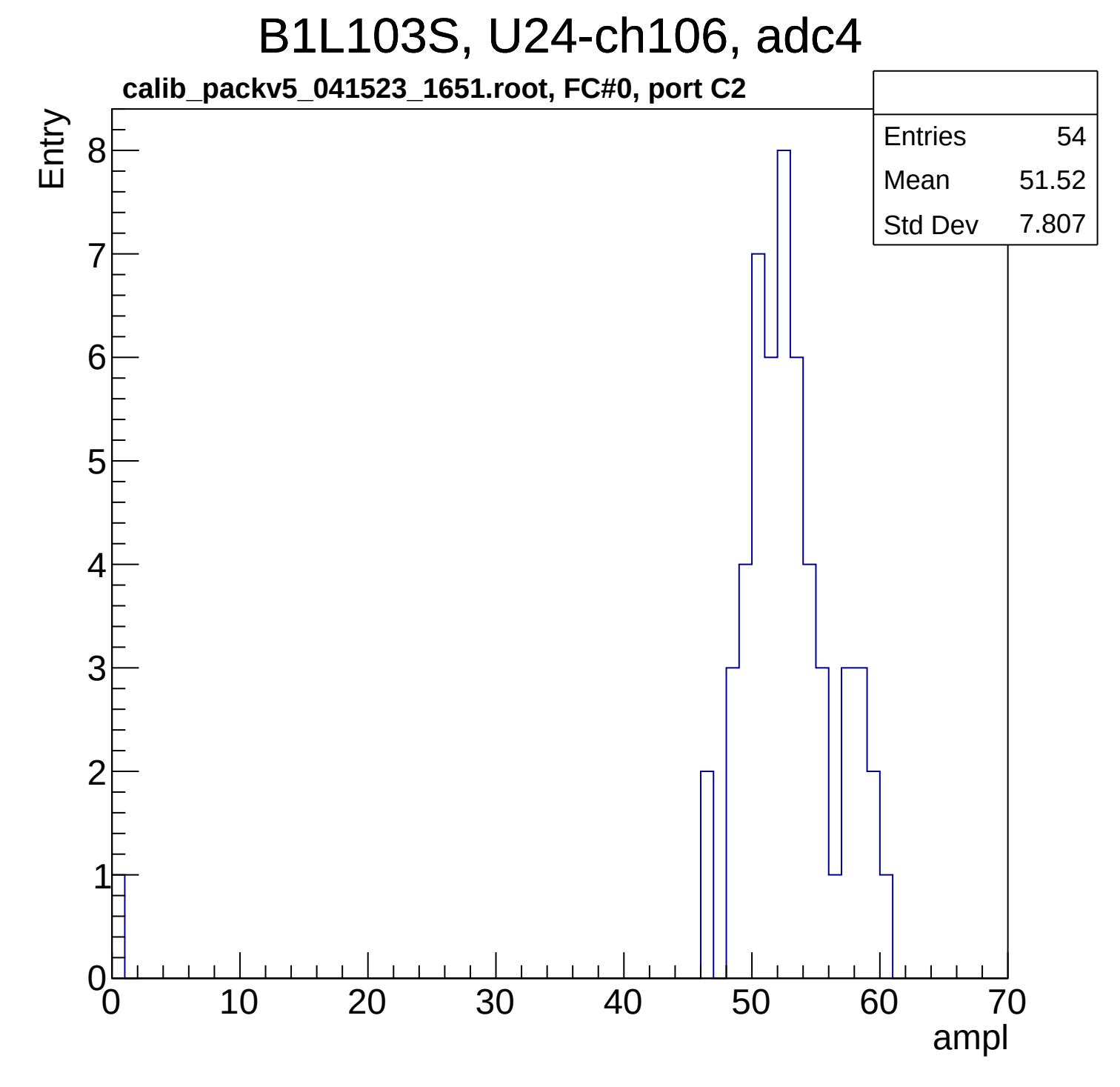
B1L103S, U24-ch106, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 51.52
Std Dev 7.807
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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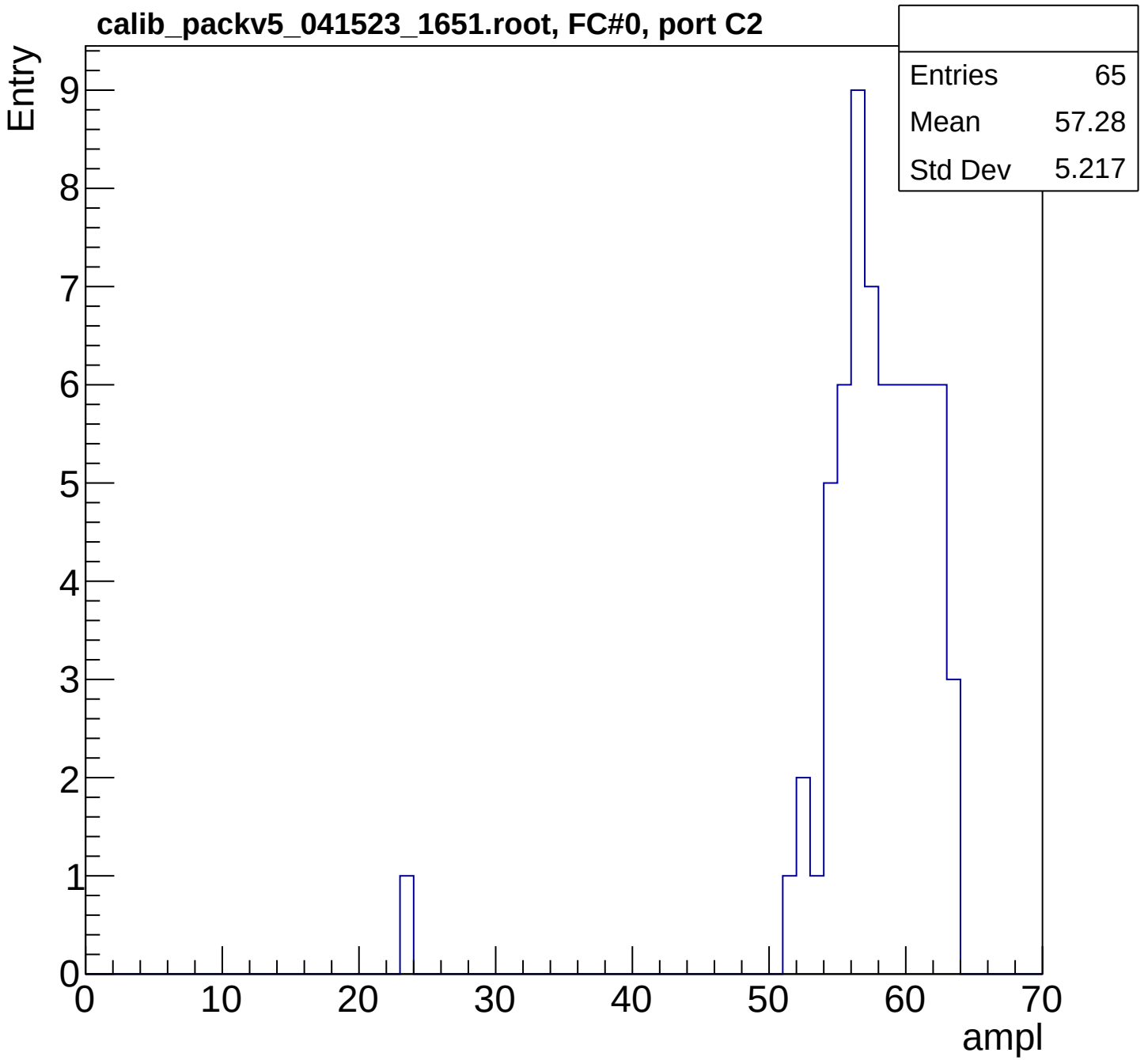
B1L103S, U24-ch106, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 57.28
Std Dev 5.217
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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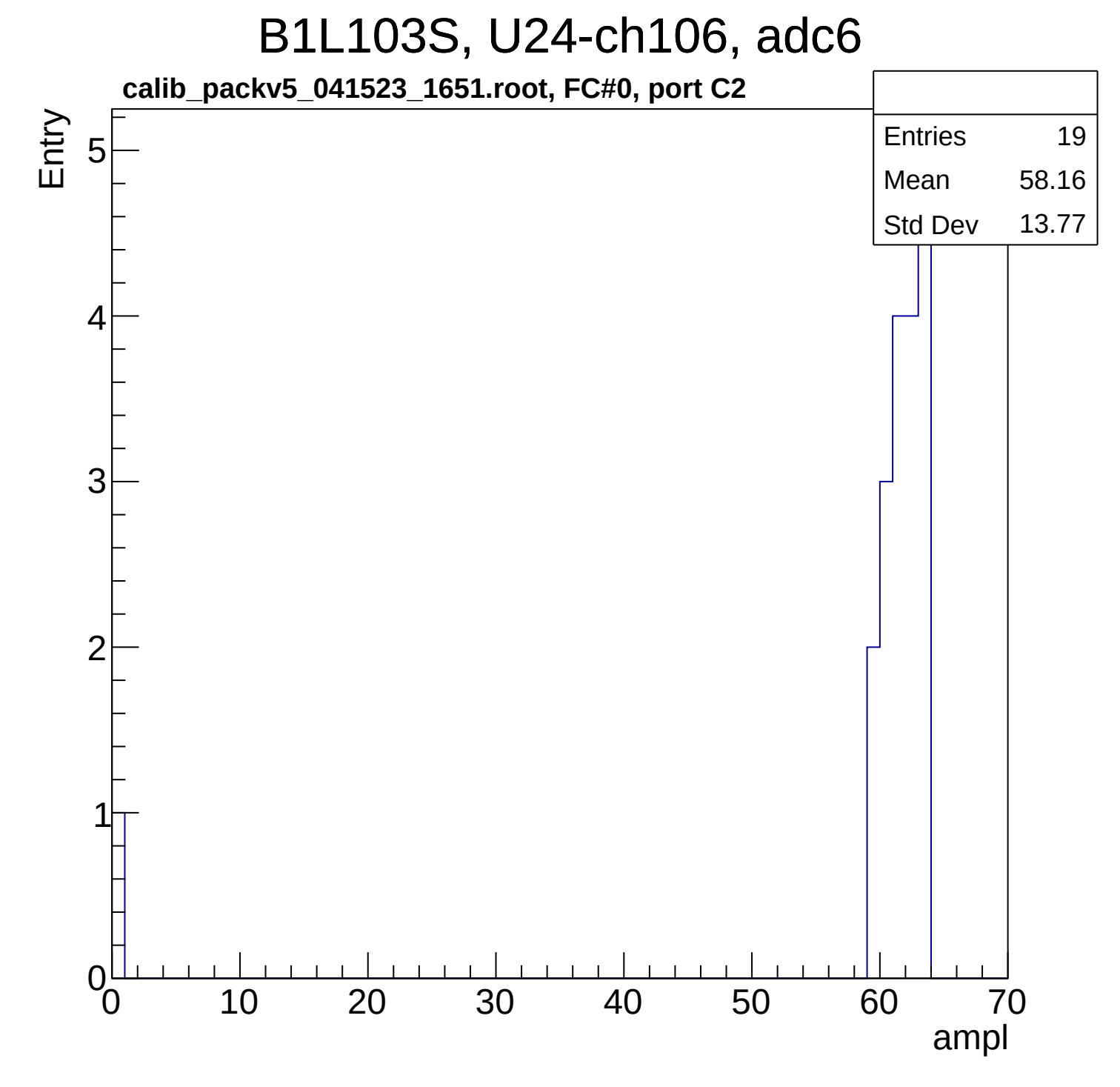
B1L103S, U24-ch106, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 58.16
Std Dev 13.77
Entry
ampl
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2
3
4
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0
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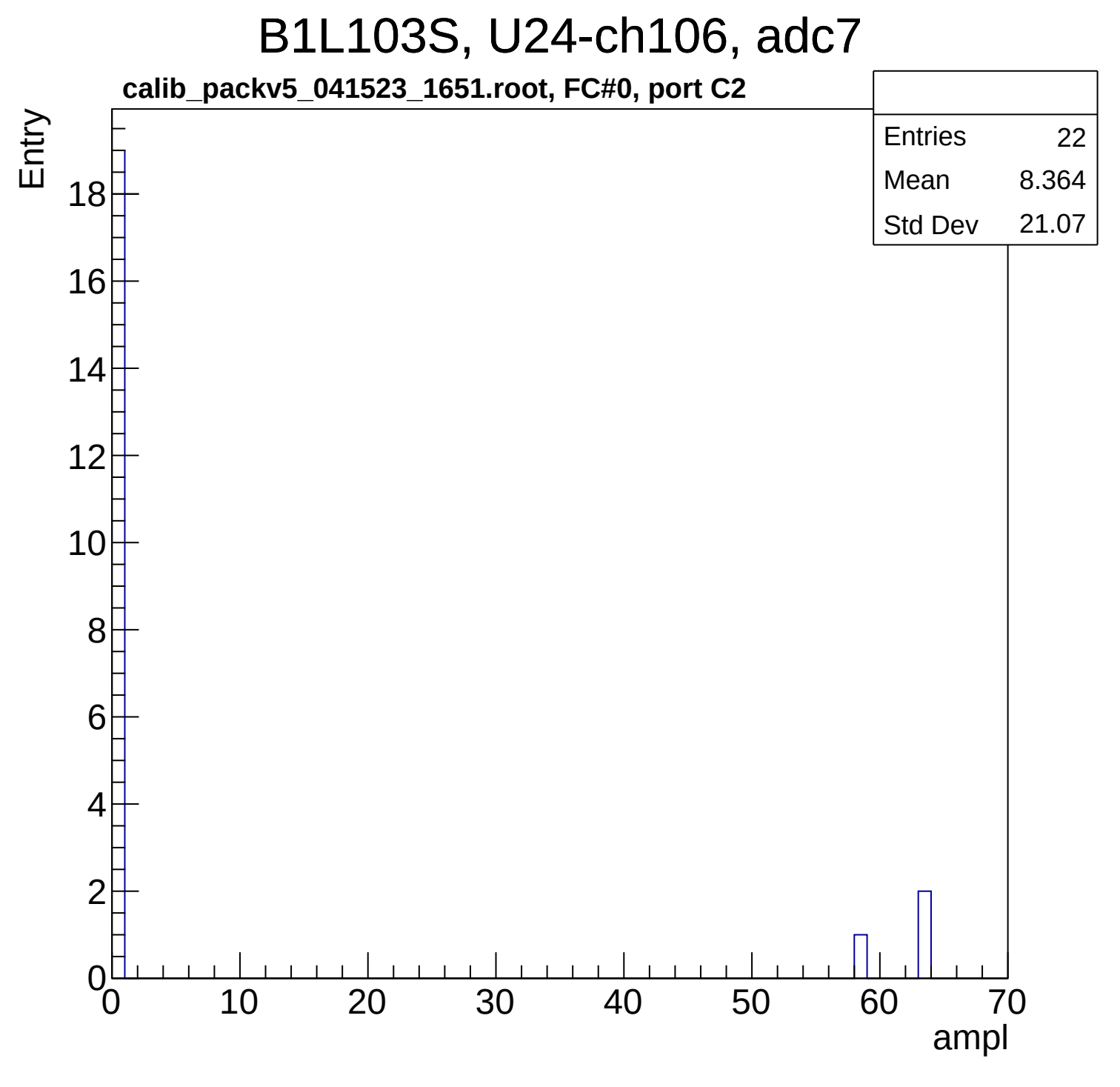
20
30
40
50
60
70


B1L103S, U24-ch106, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 8.364
Std Dev 21.07
Entry
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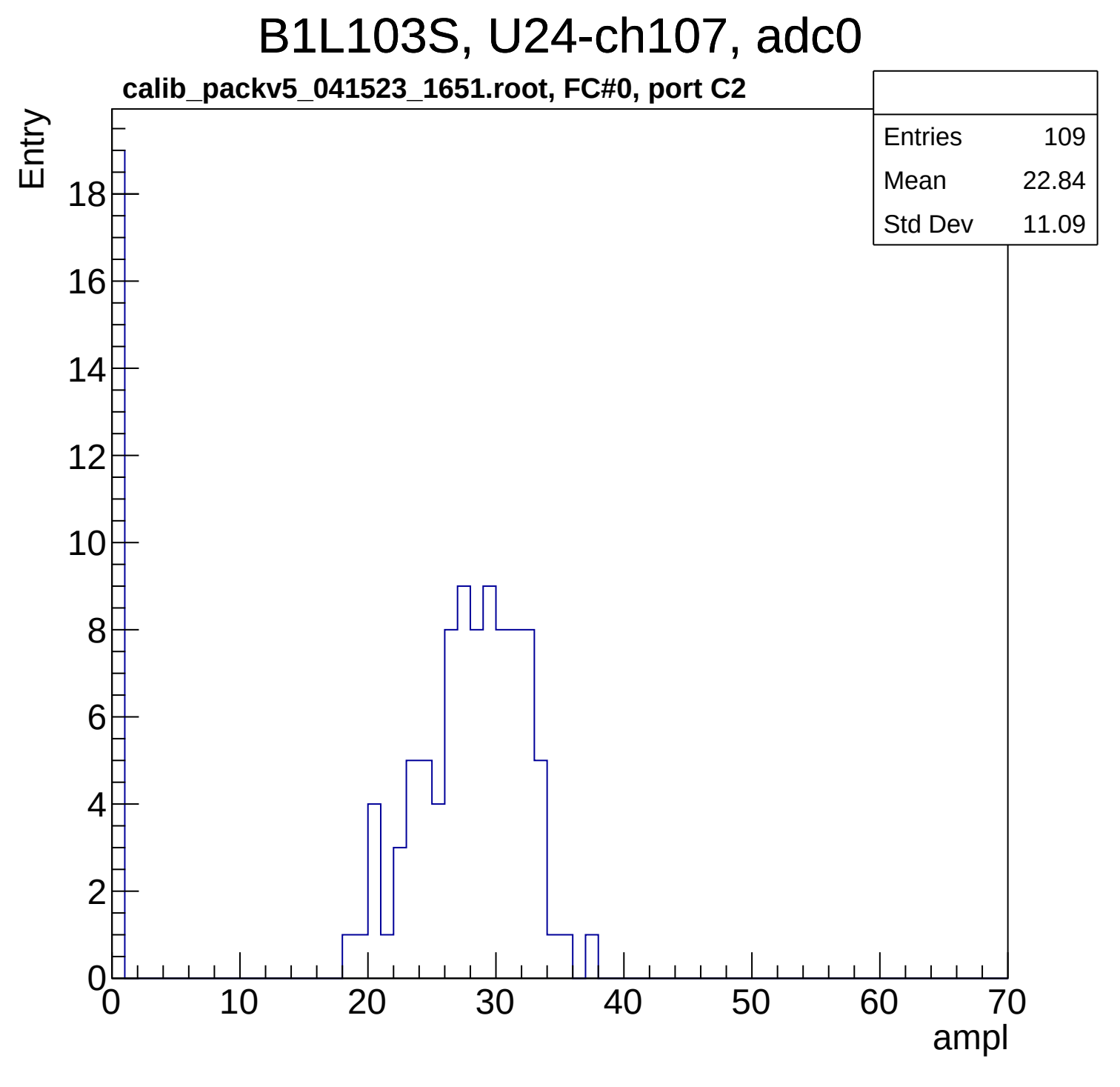
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch107, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 109
Mean 22.84
Std Dev 11.09
Entry
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6
8
10
12
14
16
18
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20
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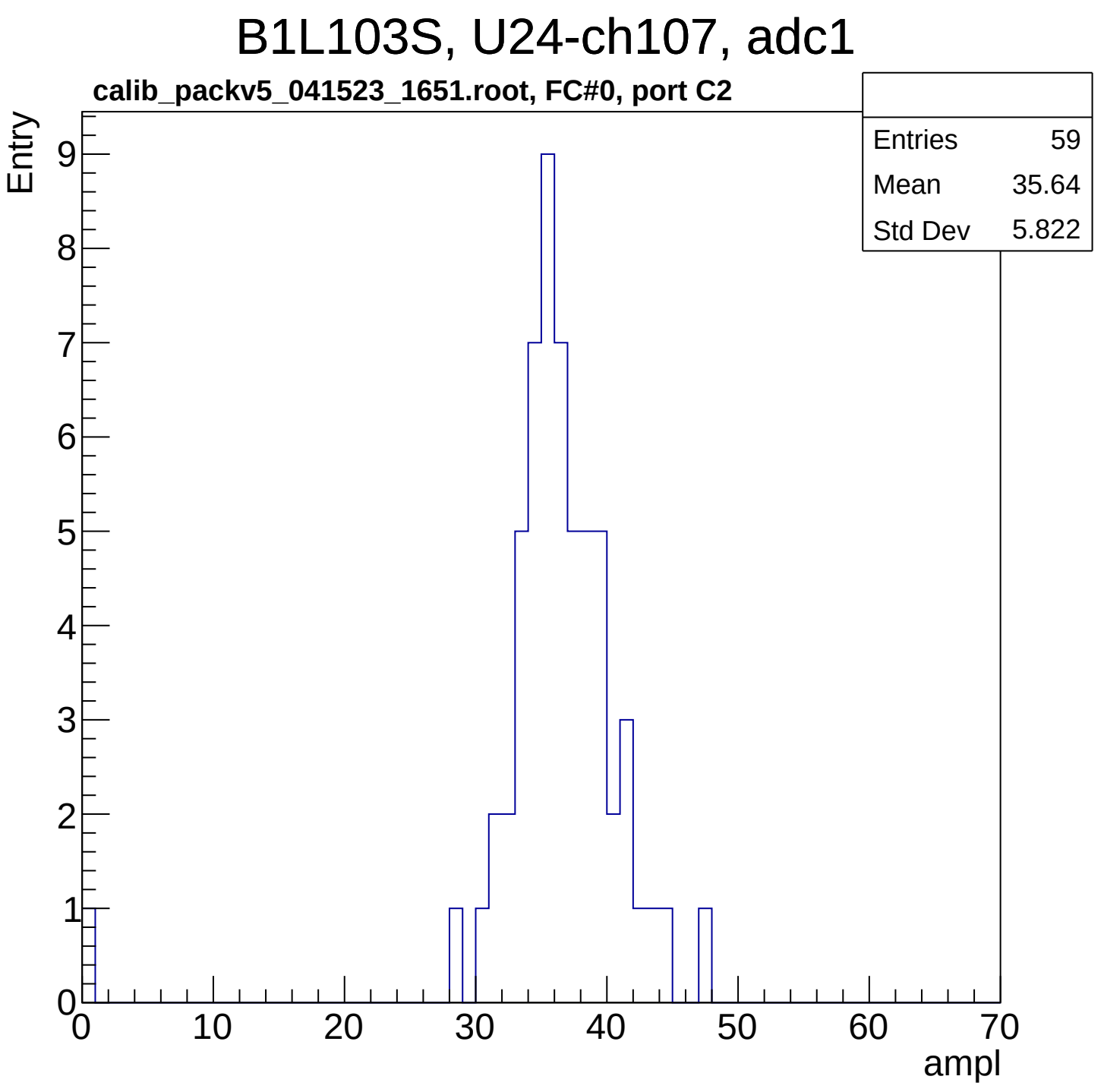
40
50
60
70
ampl


B1L103S, U24-ch107, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 35.64
Std Dev 5.822
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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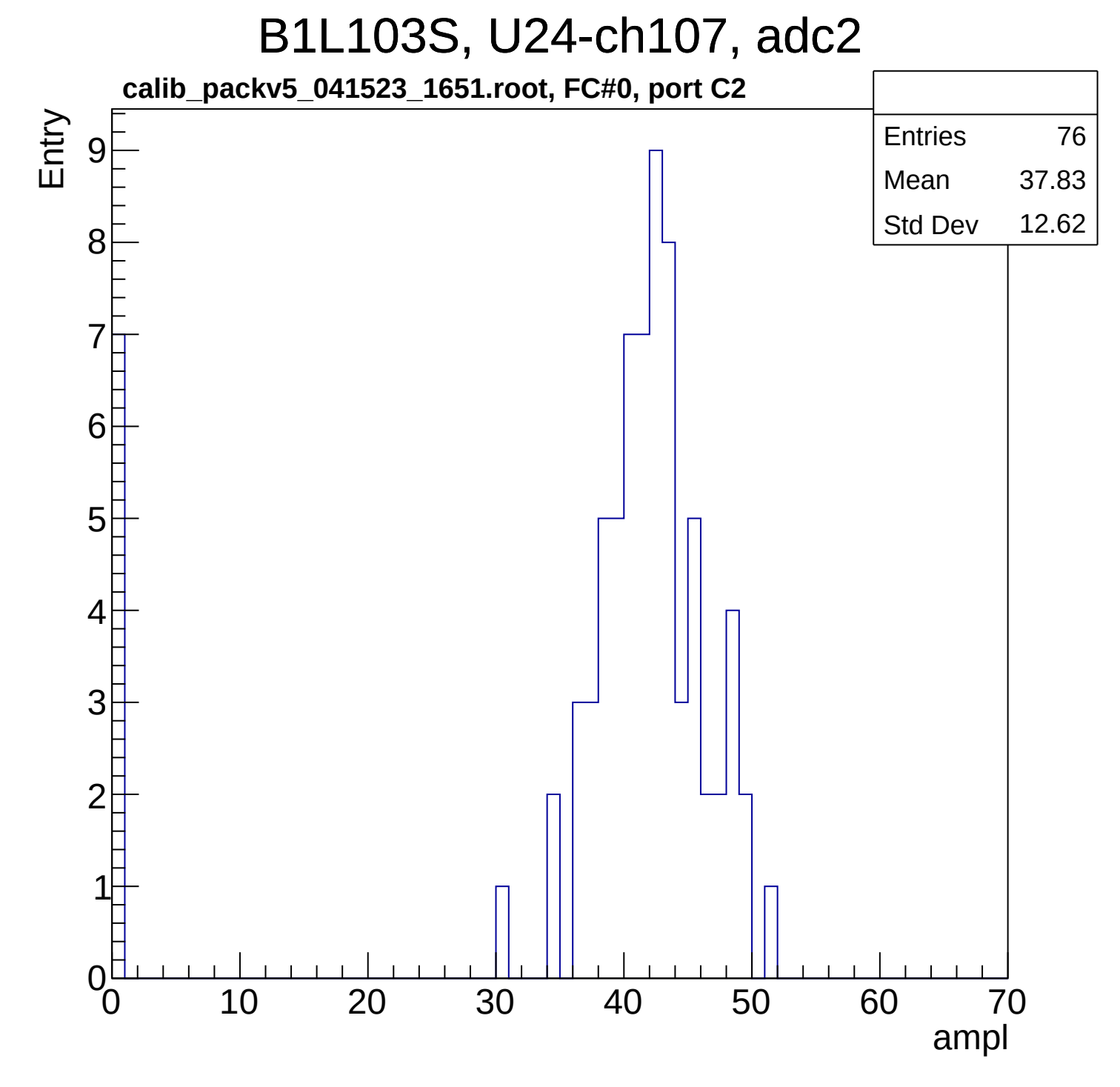
30
40
50
60
70


B1L103S, U24-ch107, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 37.83
Std Dev 12.62
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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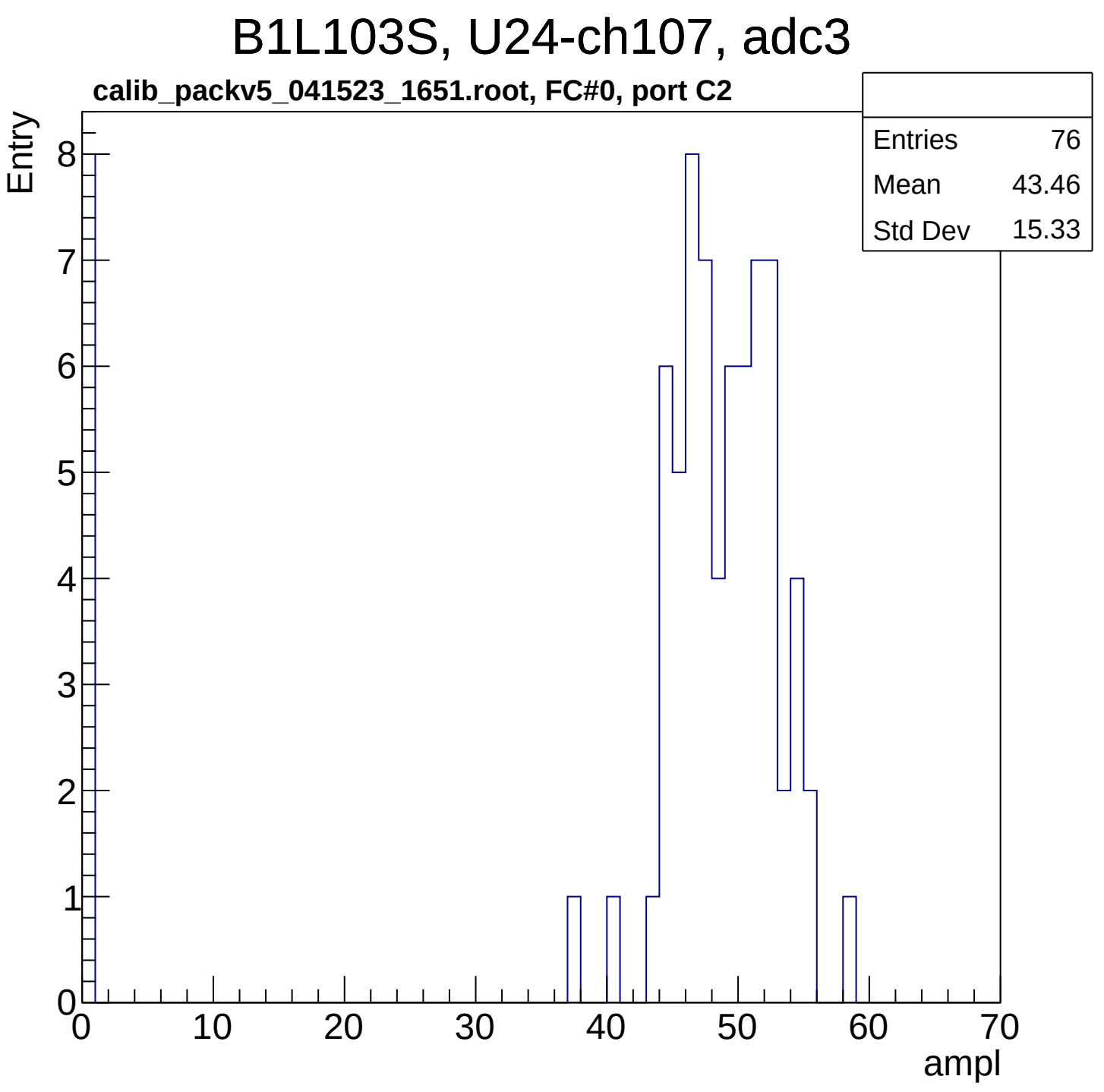
B1L103S, U24-ch107, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 43.46
Std Dev 15.33
Entry
ampl
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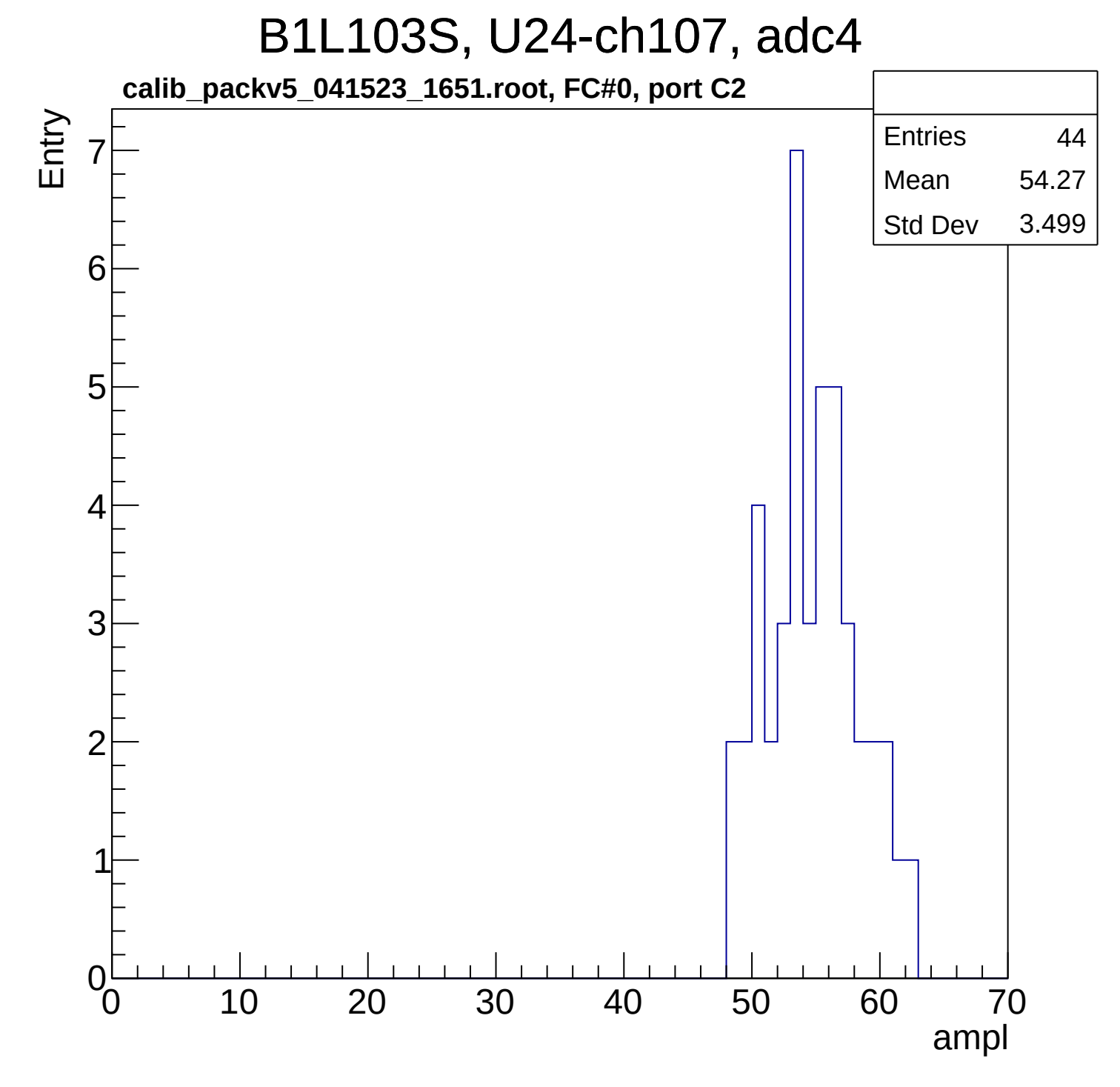
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U24-ch107, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 54.27
Std Dev 3.499
Entry
ampl
0
1
2
3
4
5
6
7
0
10
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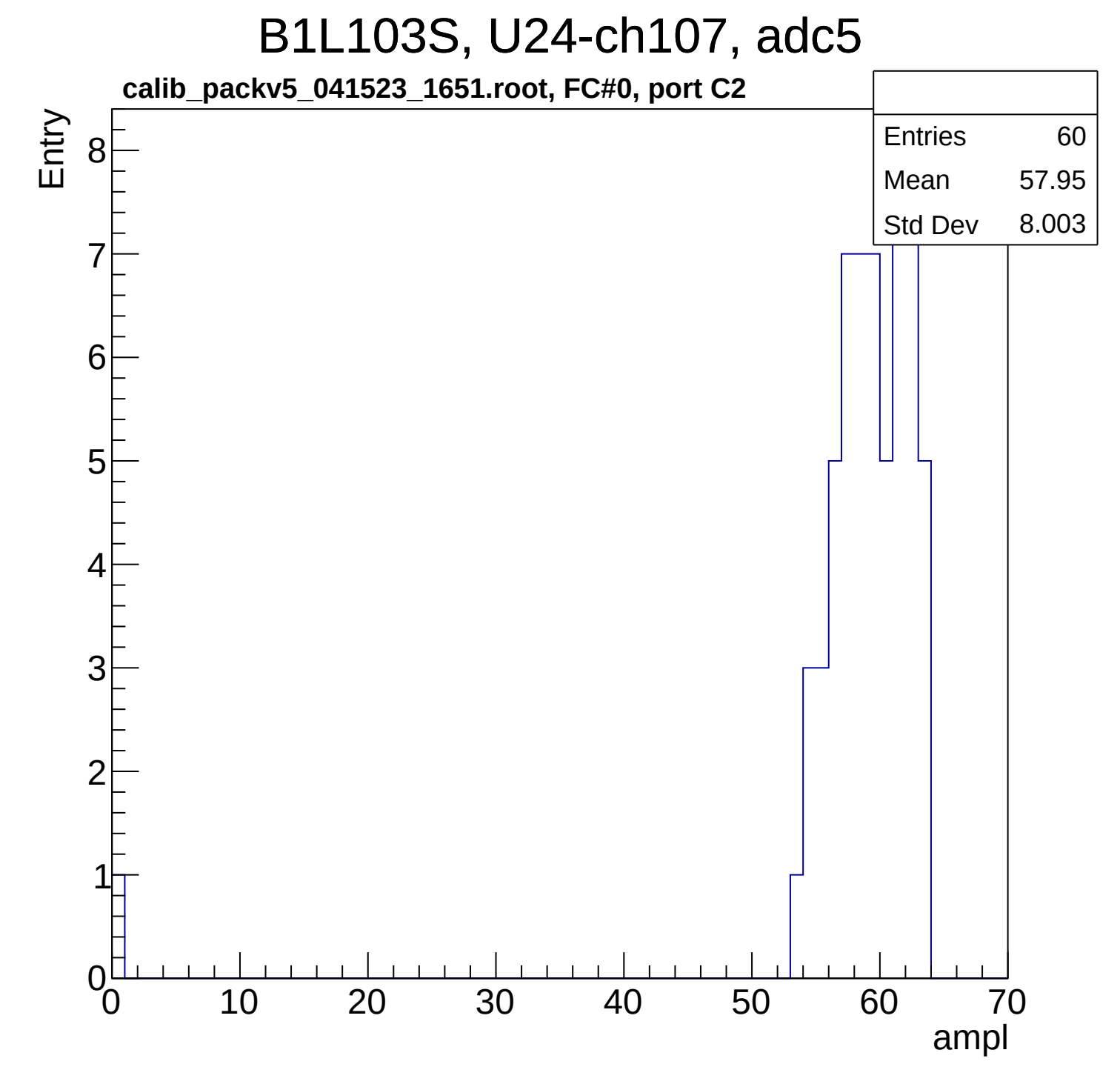
40
50
60
70


B1L103S, U24-ch107, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 57.95
Std Dev 8.003
Entry
ampl
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1
2
3
4
5
6
7
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0
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40
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60
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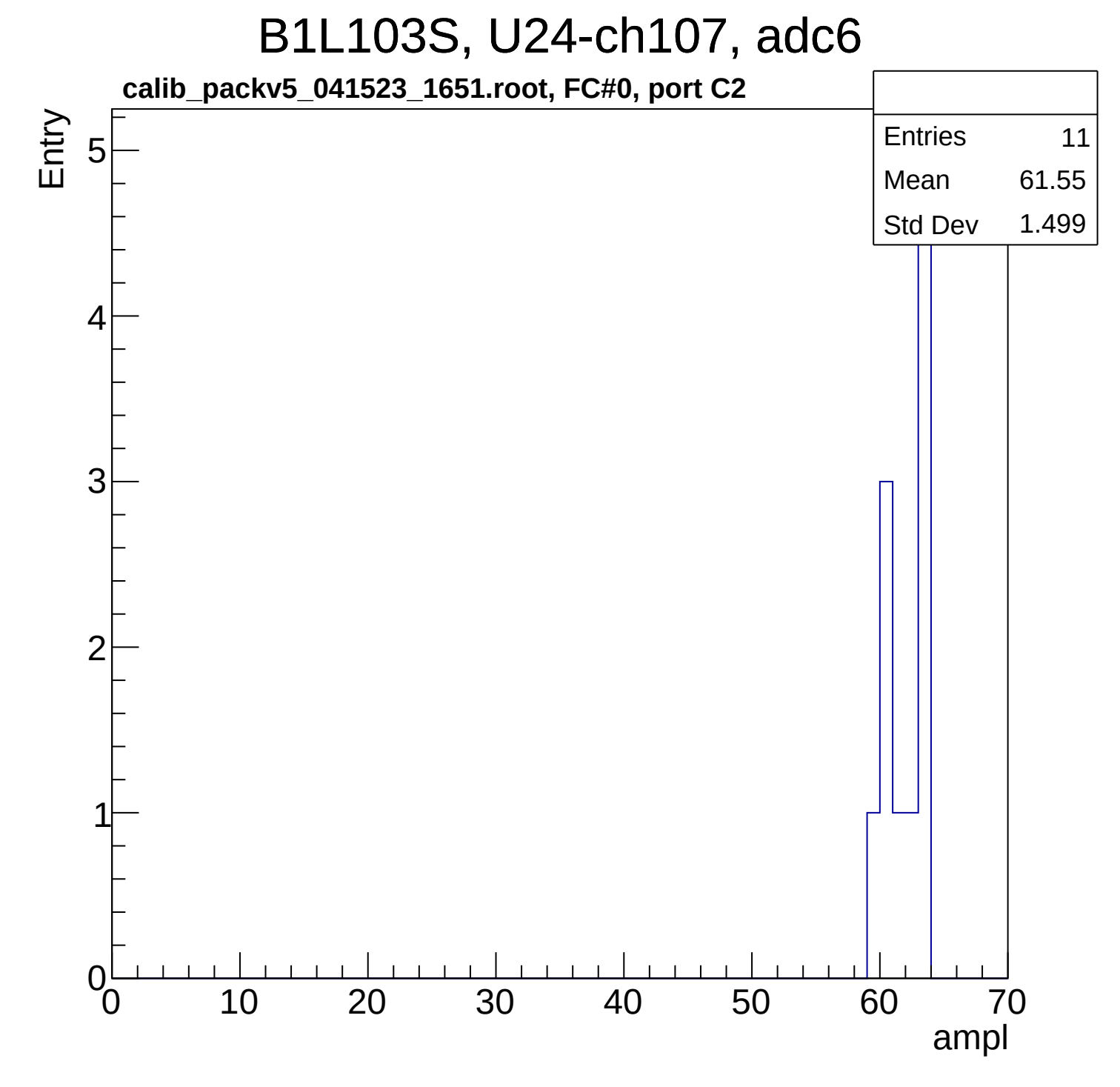
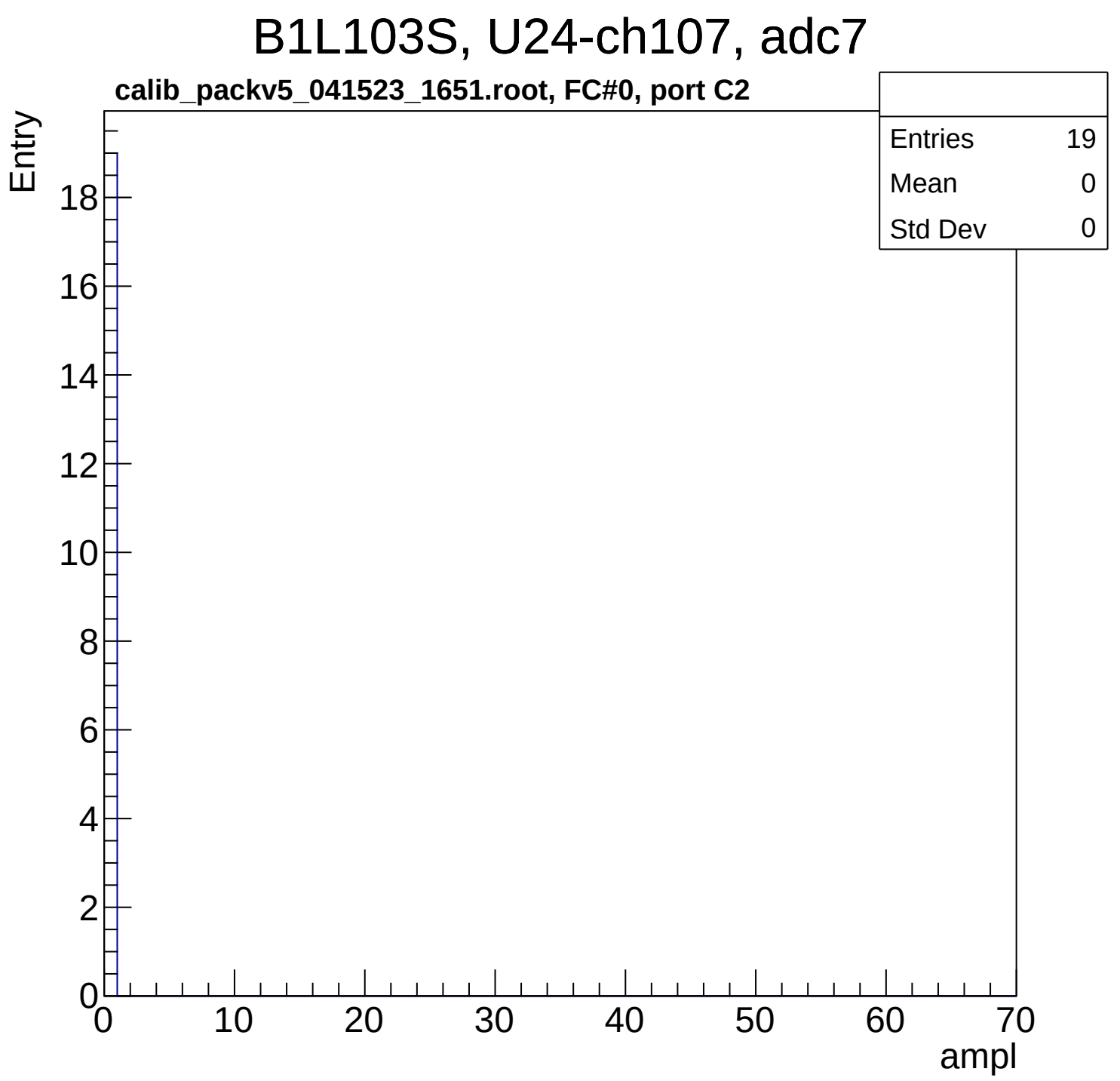
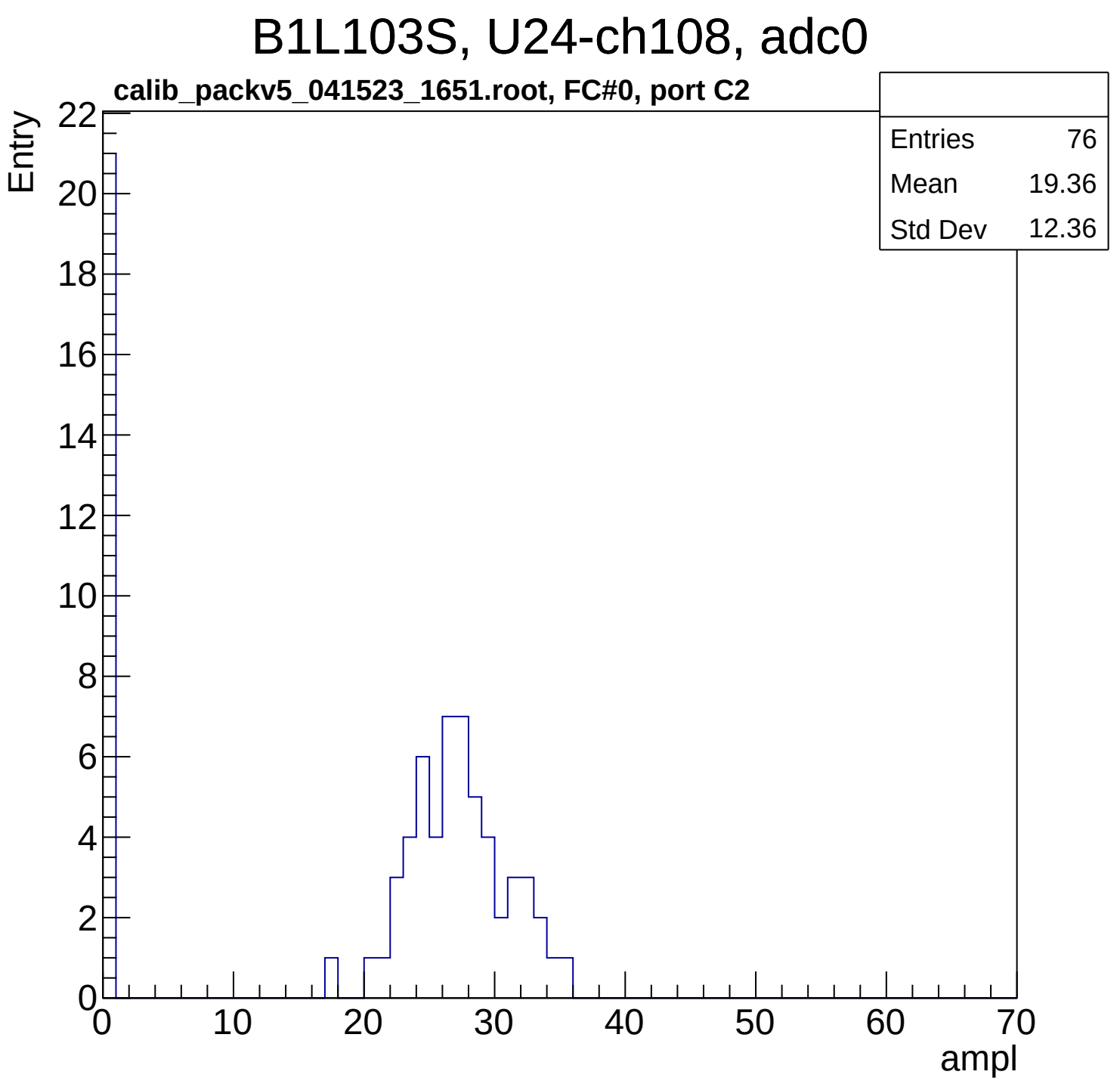
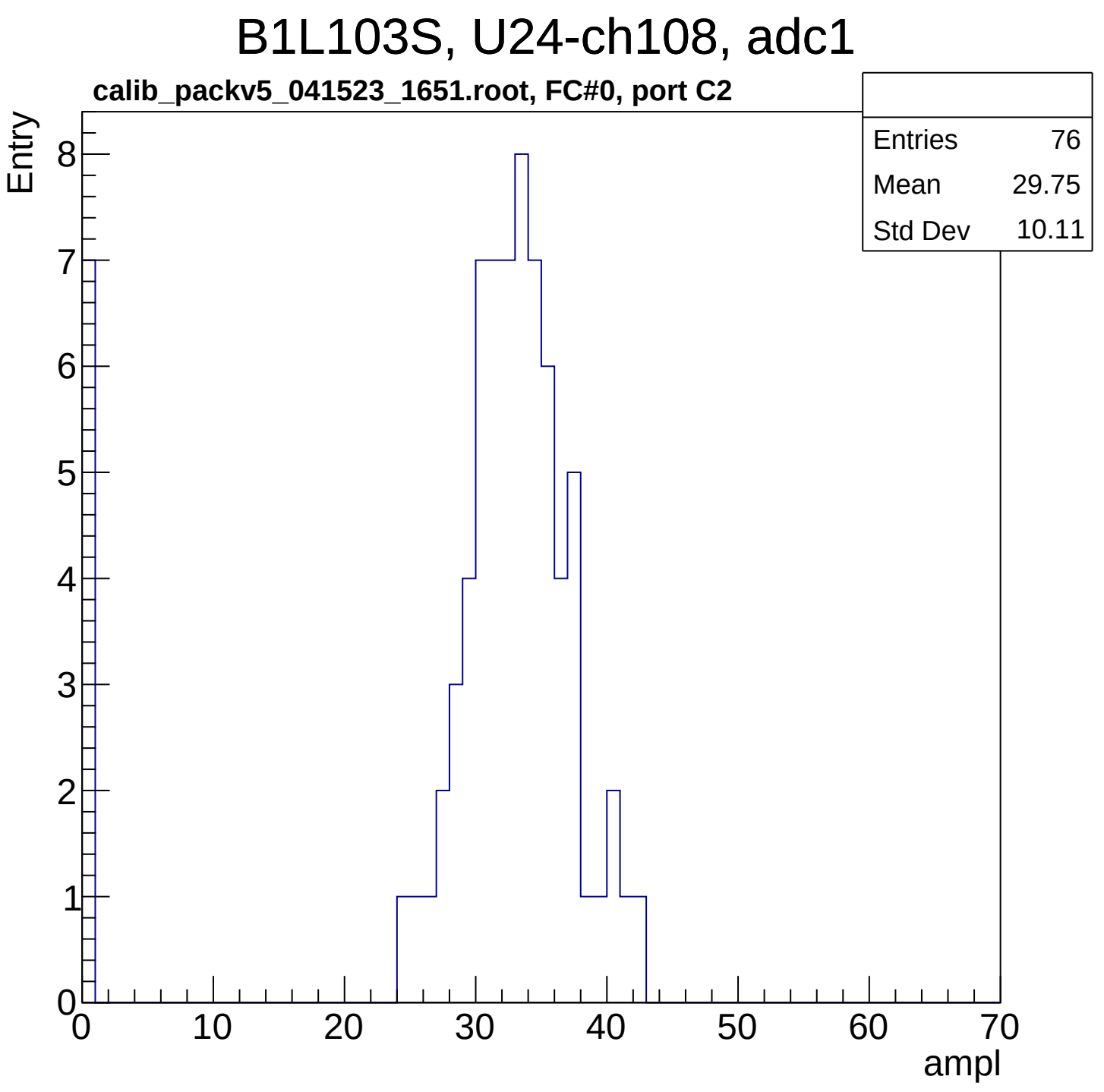

B1L103S, U24-ch107, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 61.55
Std Dev 1.499
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U24-ch107, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch108, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 19.36
Std Dev 12.36
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
22
0
10
20
30
40
50
60
70


B1L103S, U24-ch108, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 29.75
Std Dev 10.11
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
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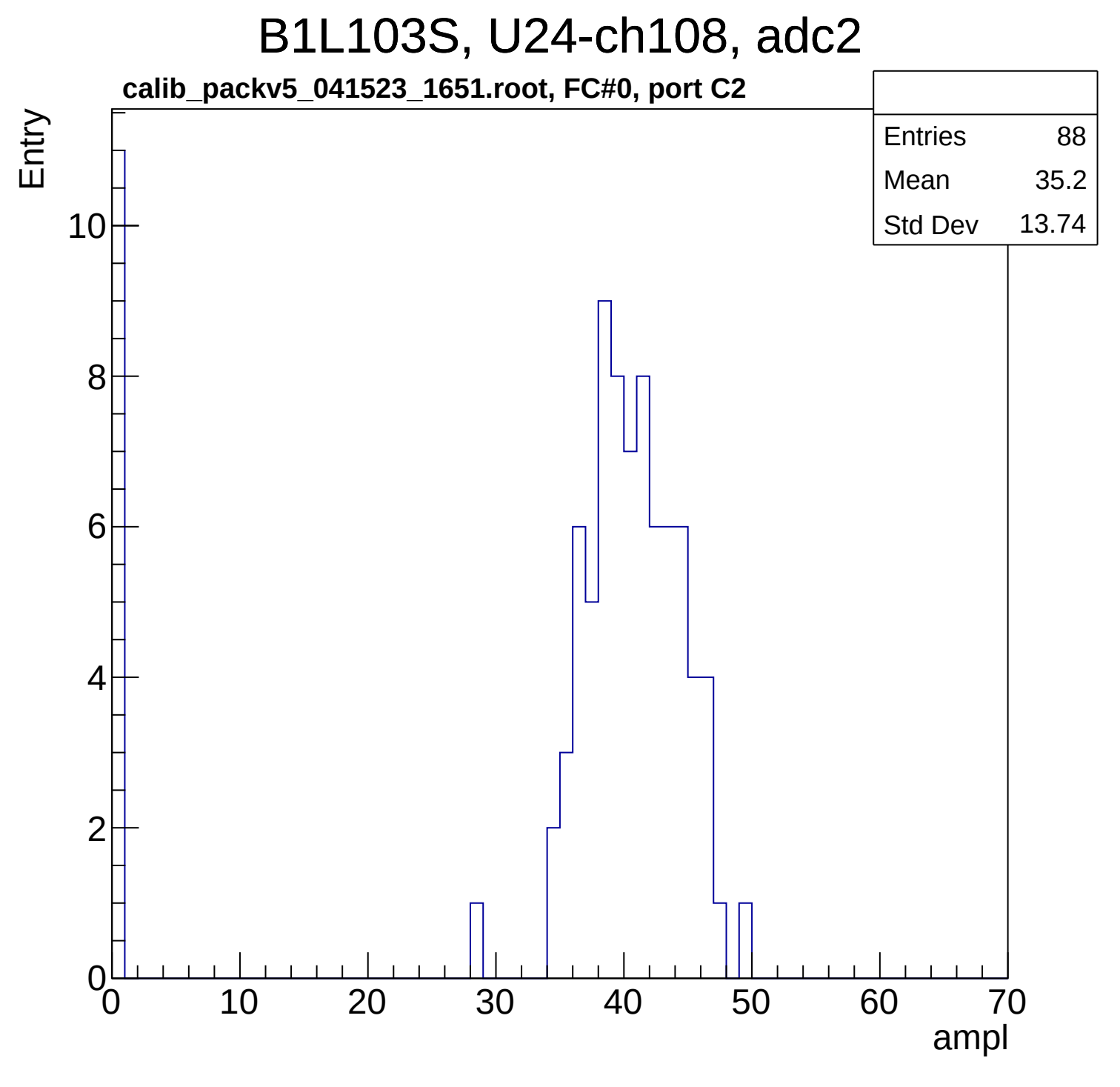
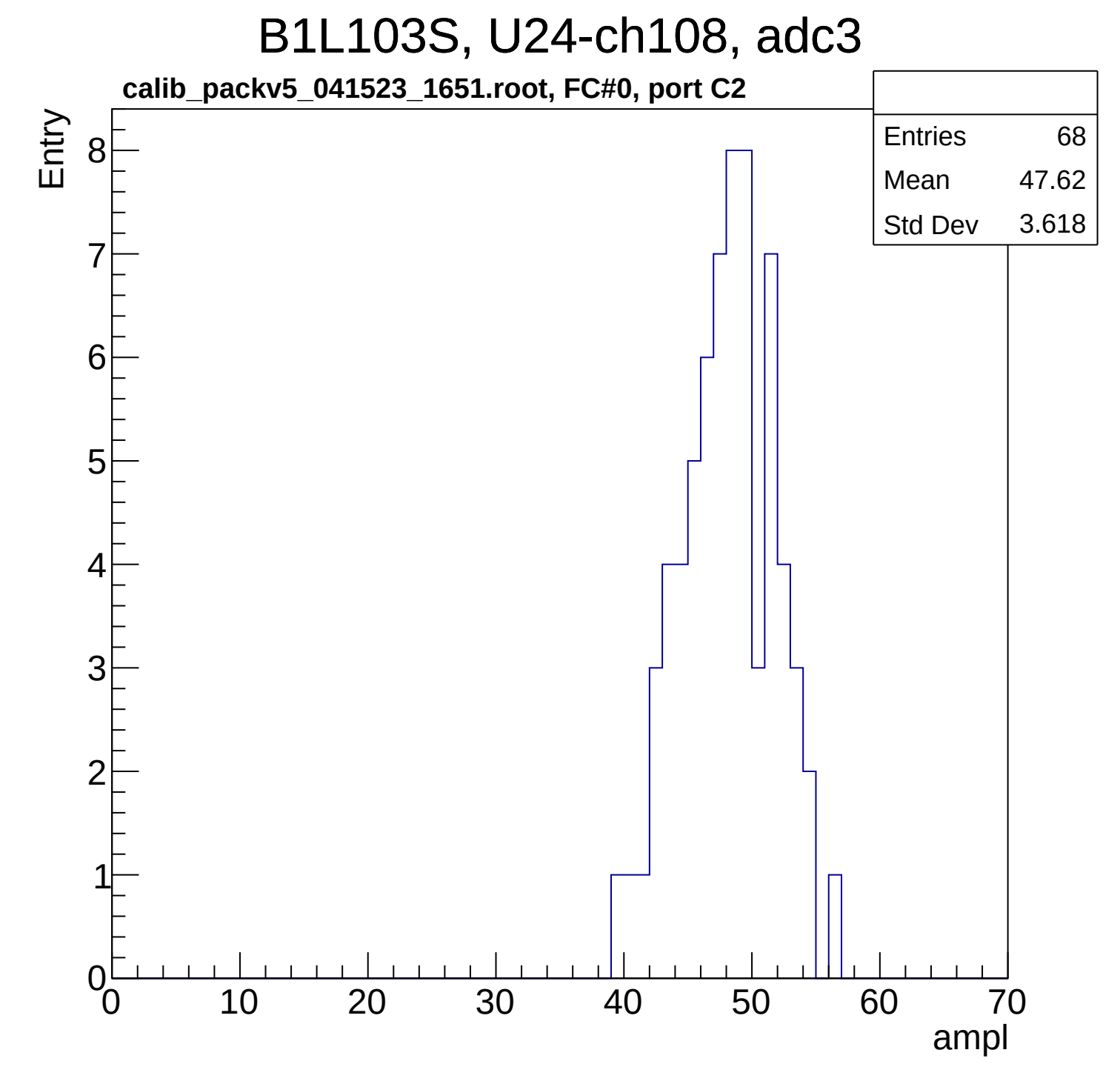
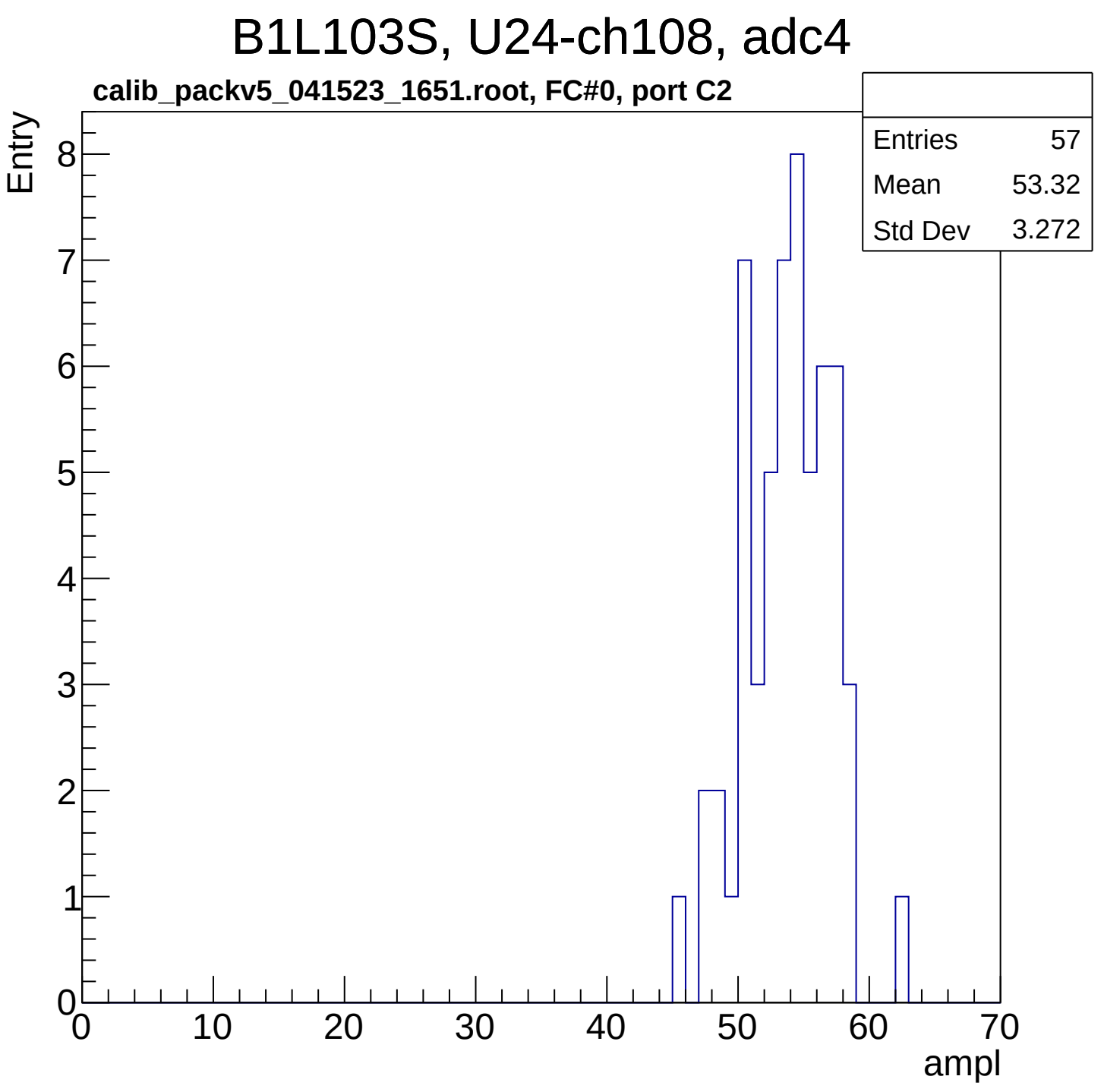
30
40
50
60
70


B1L103S, U24-ch108, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 88
Mean 35.2
Std Dev 13.74
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch108, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 47.62
Std Dev 3.618
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U24-ch108, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 53.32
Std Dev 3.272
Entry
ampl
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2
3
4
5
6
7
8
0
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20
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40
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60
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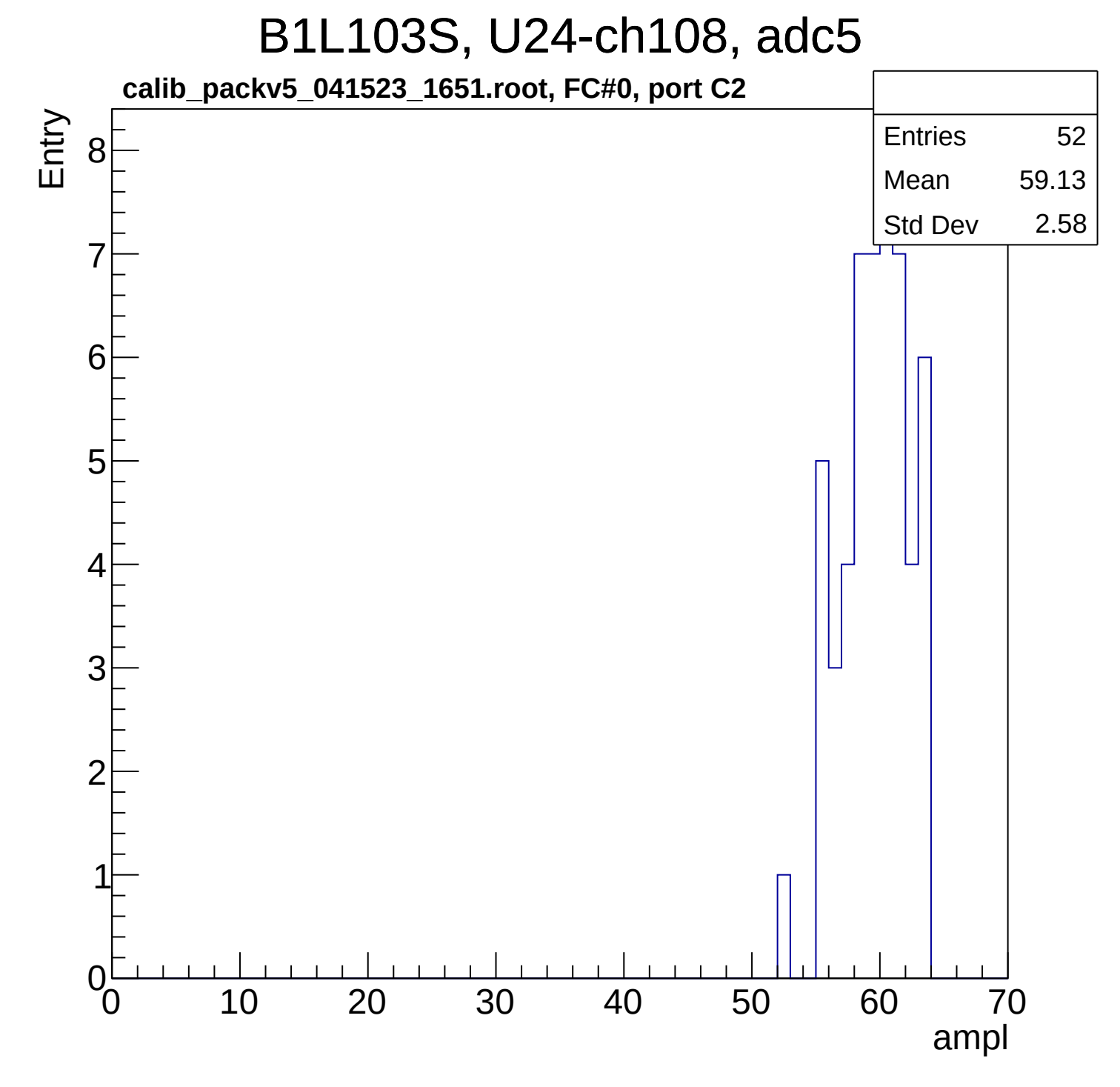
B1L103S, U24-ch108, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 59.13
Std Dev 2.58
Entry
ampl
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2
3
4
5
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7
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0
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40
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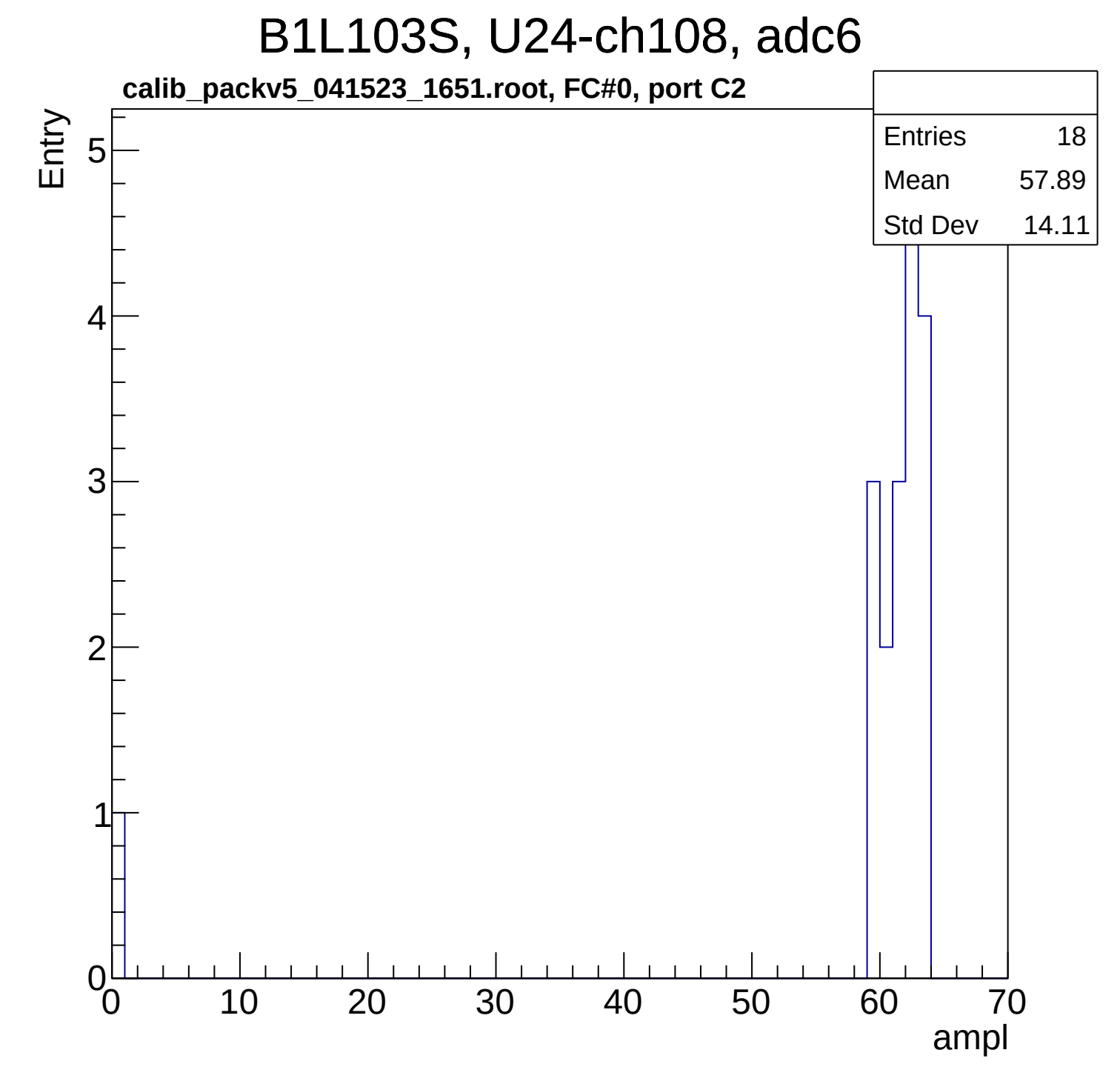
60
70


B1L103S, U24-ch108, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 57.89
Std Dev 14.11
Entry
ampl
0
1
2
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4
5
0
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40
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60
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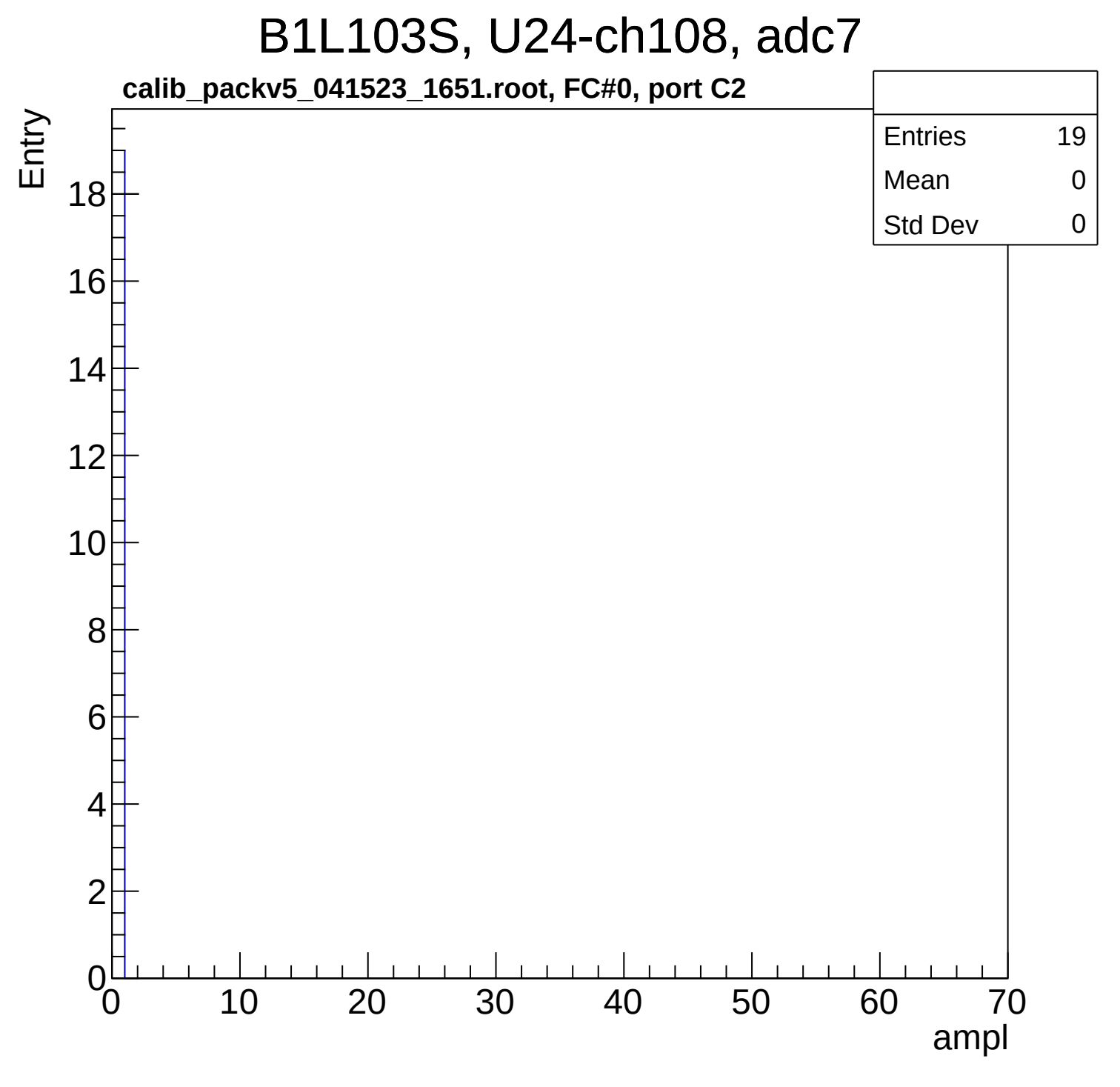
B1L103S, U24-ch108, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
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2
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6
8
10
12
14
16
18
0
10
20
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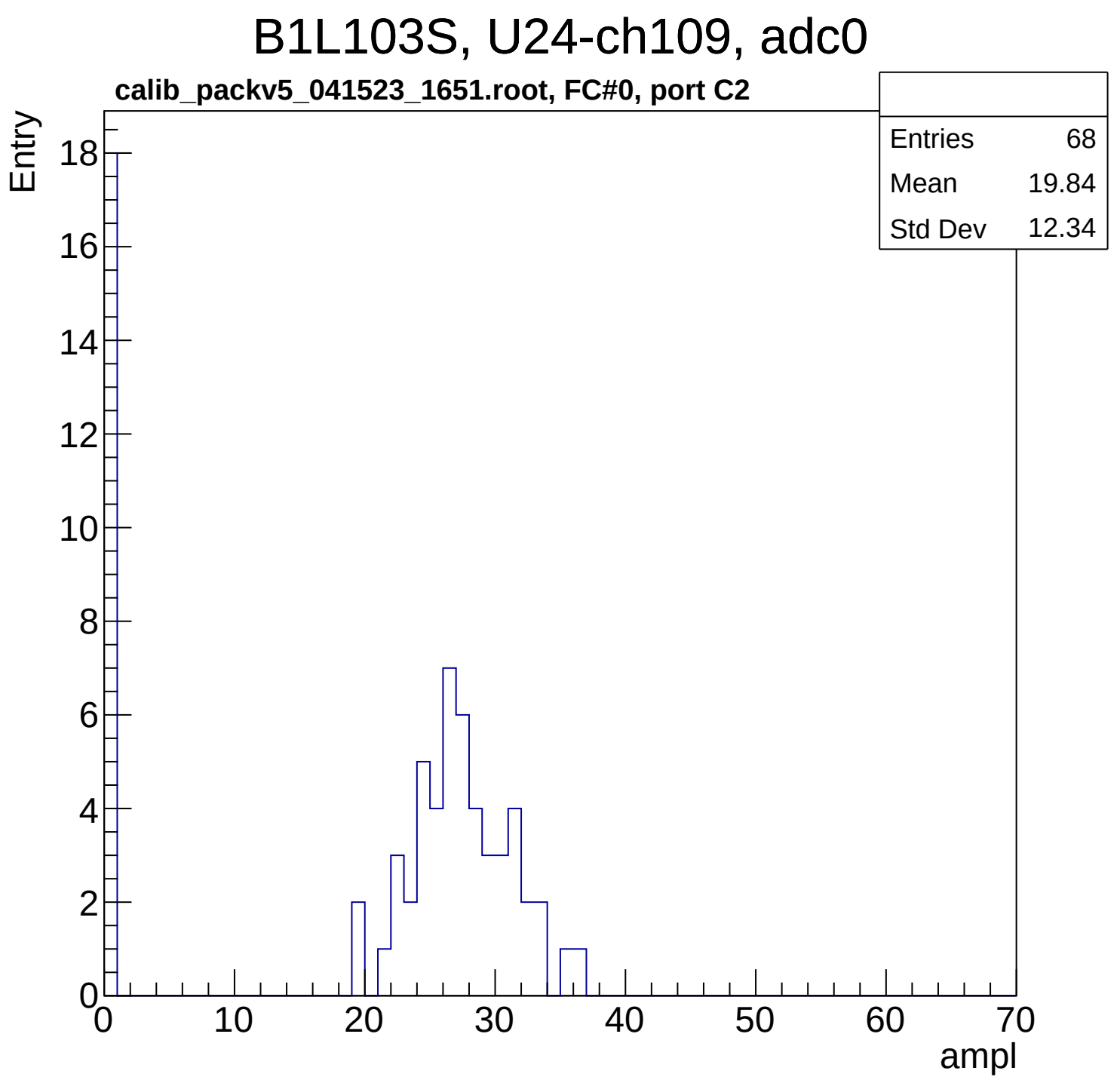
50
60
70
ampl


B1L103S, U24-ch109, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 19.84
Std Dev 12.34
Entry
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6
8
10
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14
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18
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50
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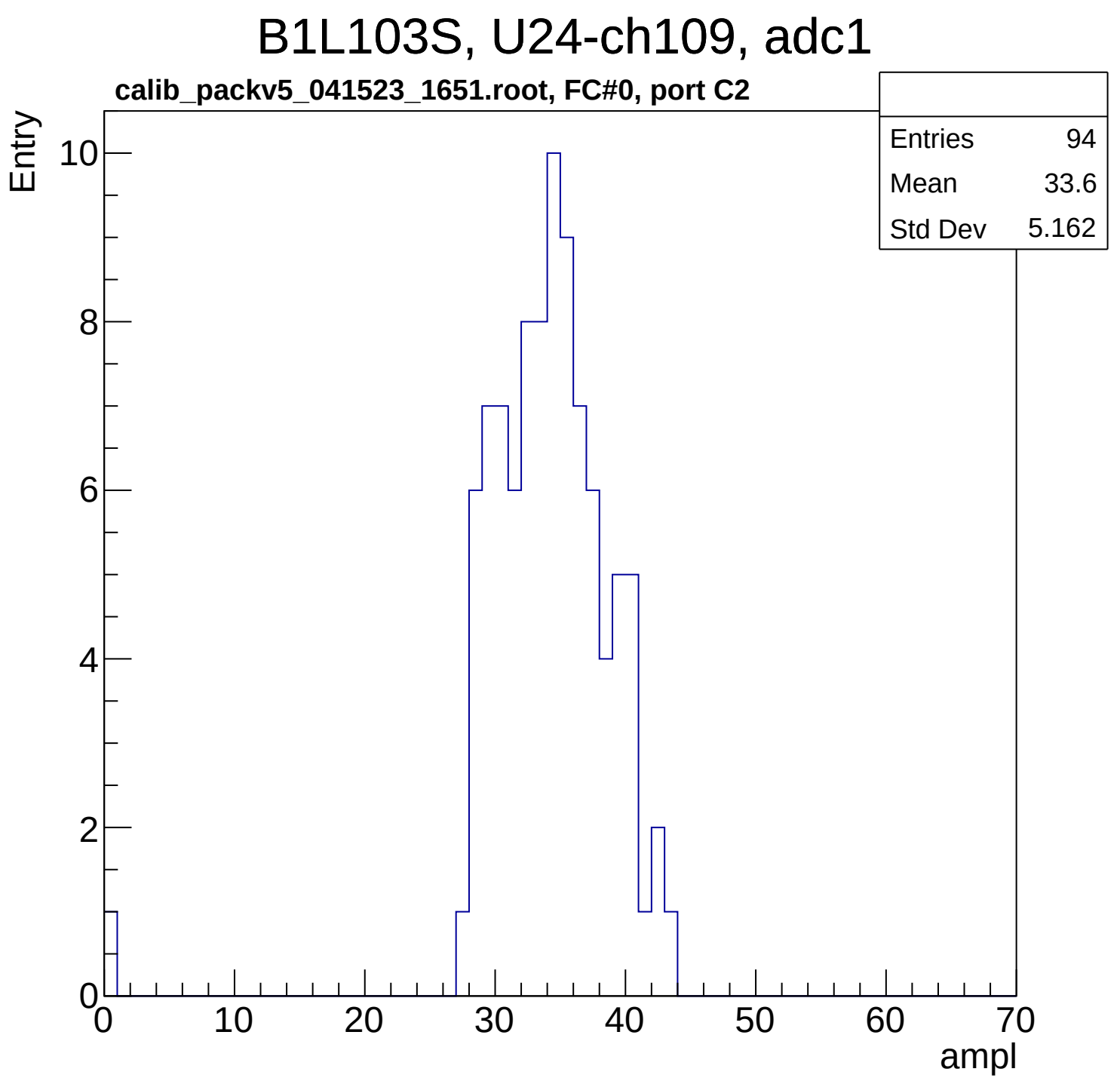
70
ampl


B1L103S, U24-ch109, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 94
Mean 33.6
Std Dev 5.162
Entry
ampl
0
2
4
6
8
10
0
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30
40
50
60
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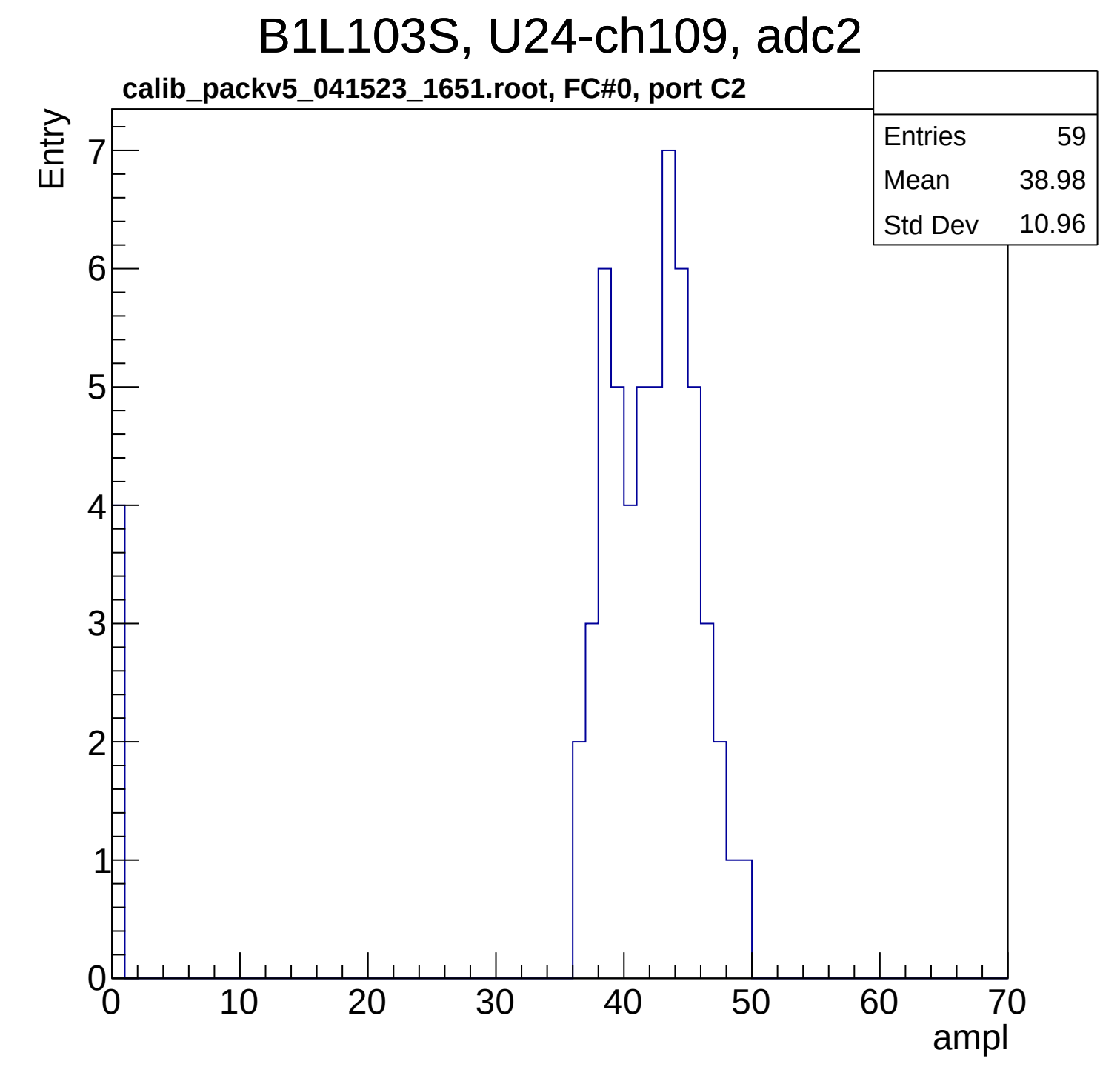
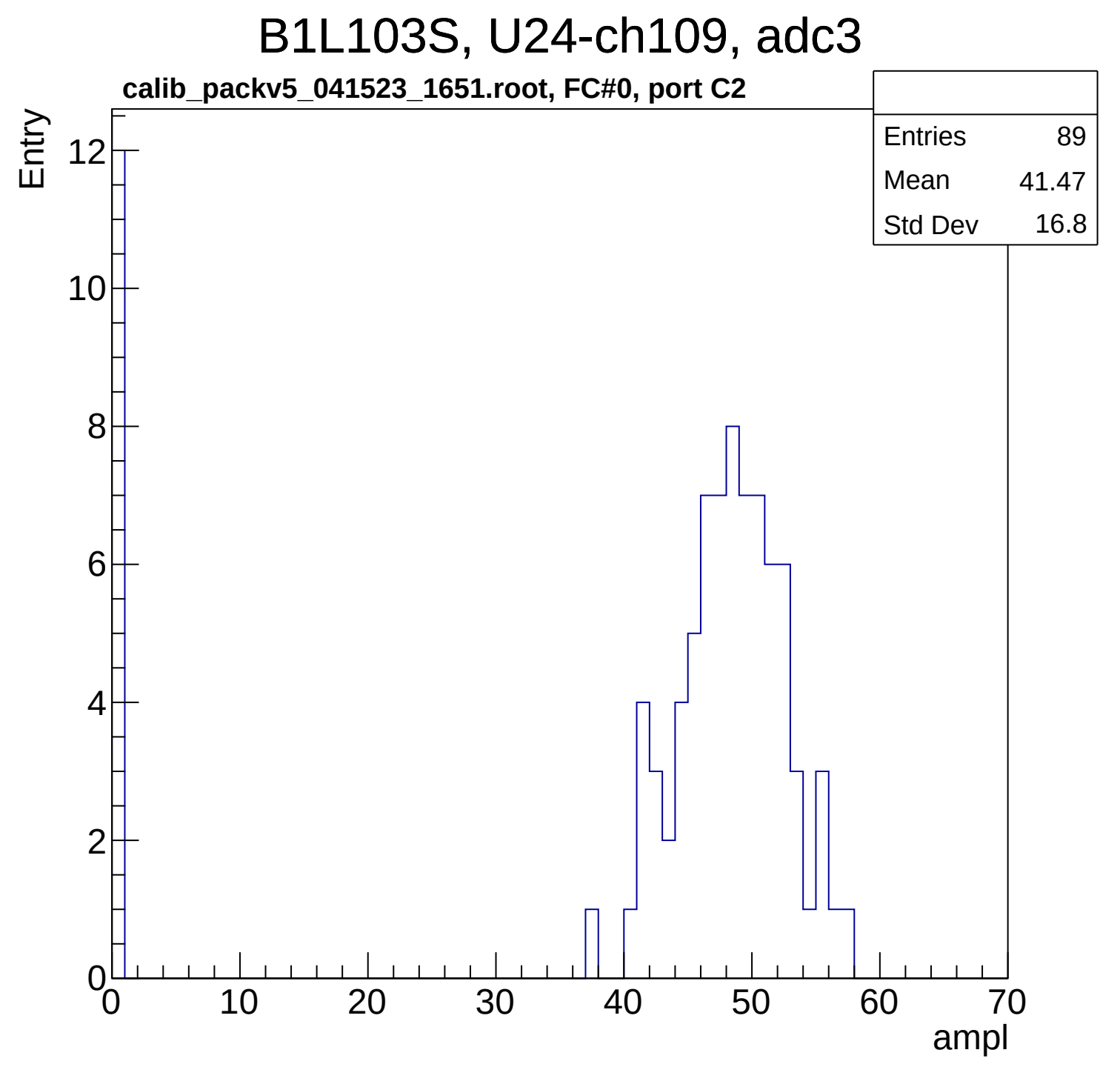

B1L103S, U24-ch109, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 38.98
Std Dev 10.96
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U24-ch109, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 89
Mean 41.47
Std Dev 16.8
Entry
0
2
4
6
8
10
12
0
10
20
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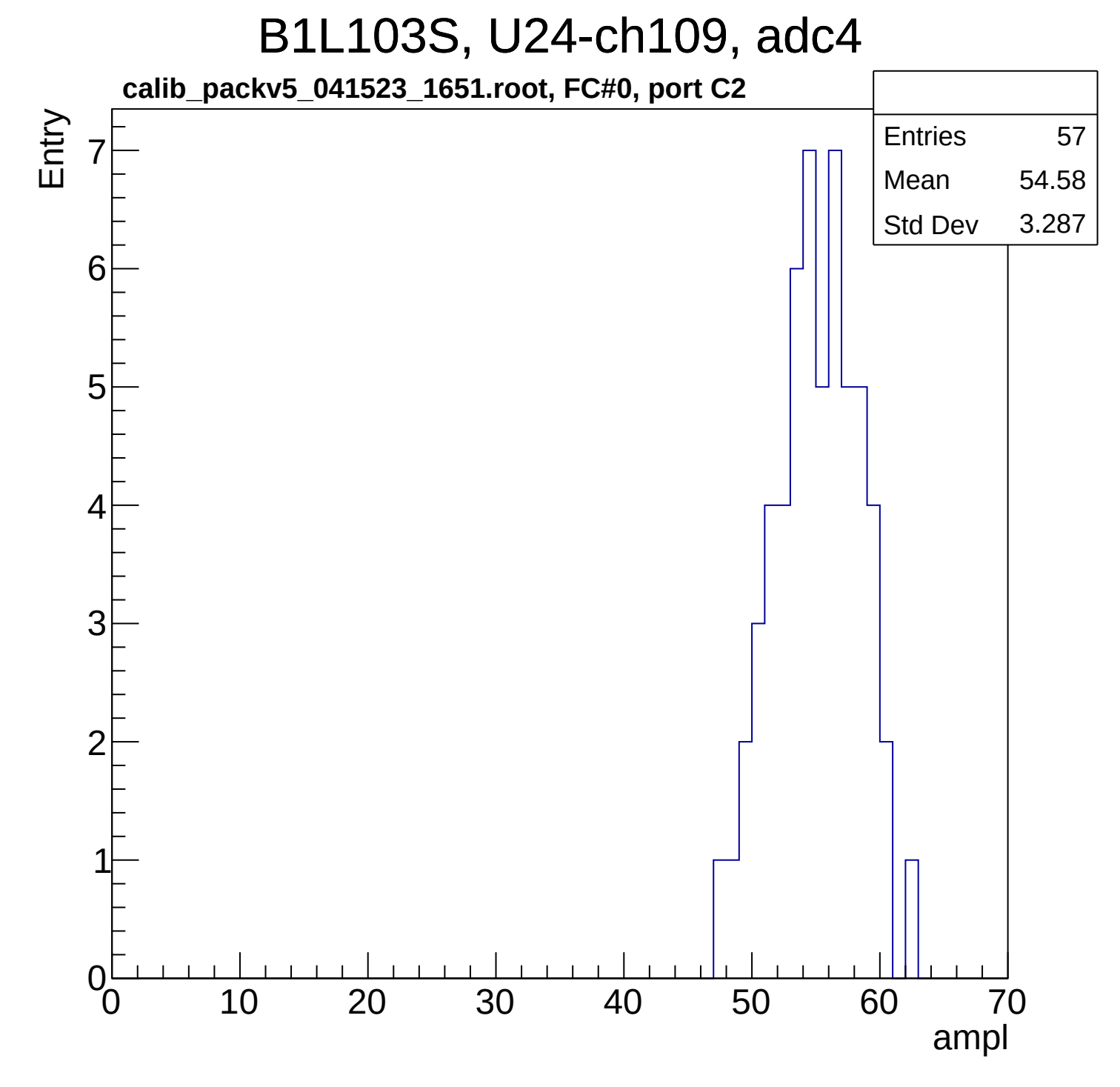
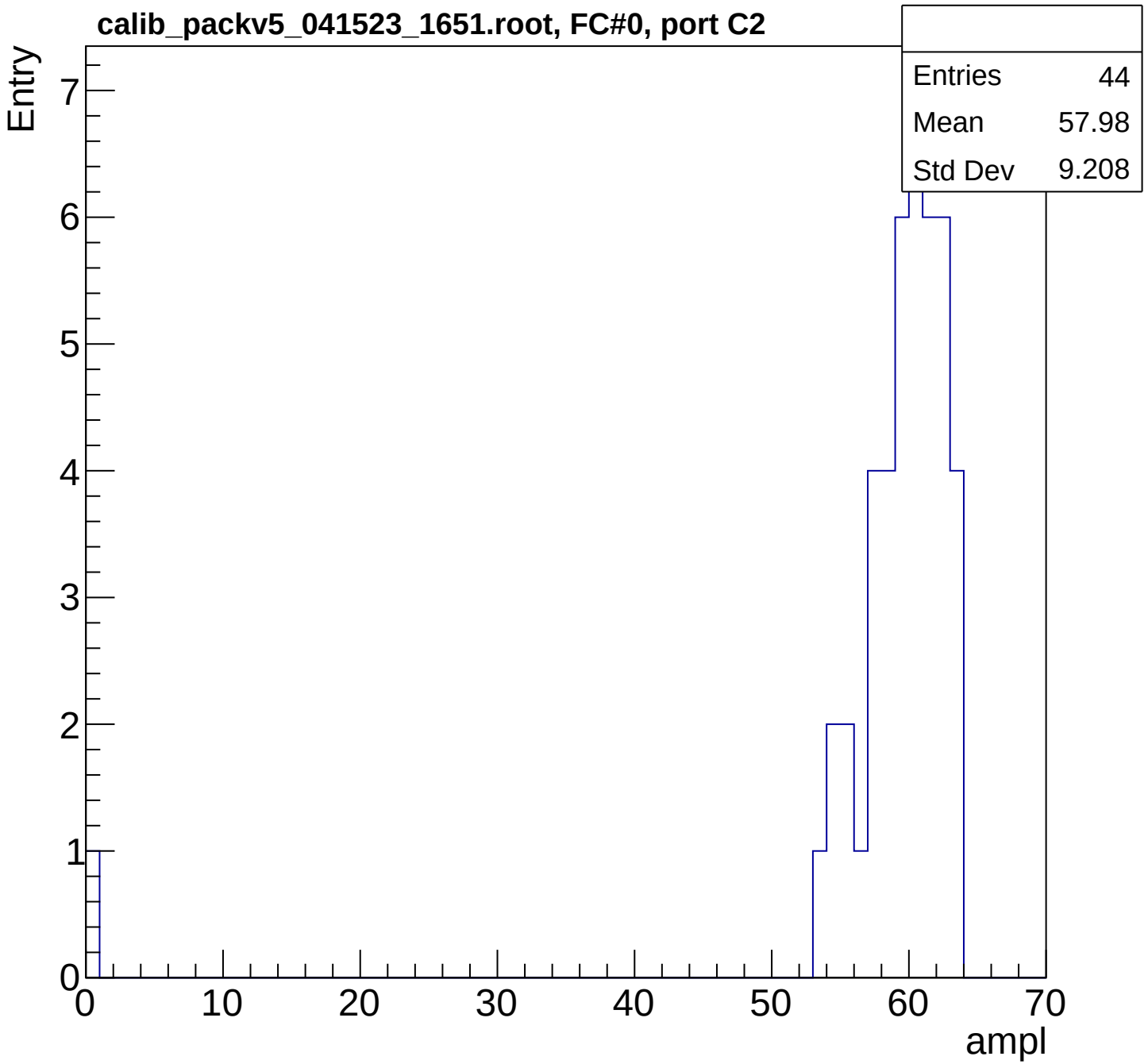
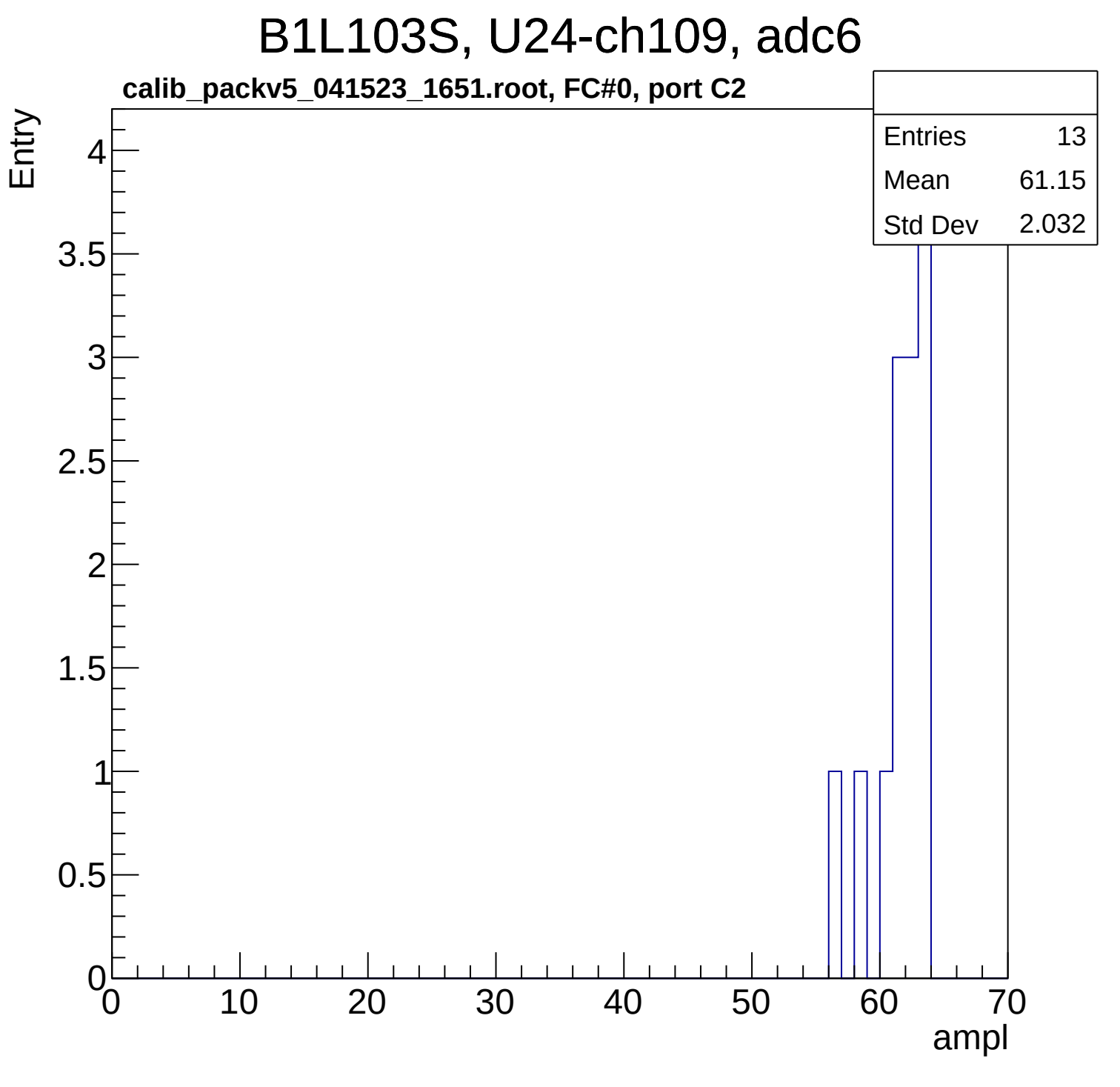
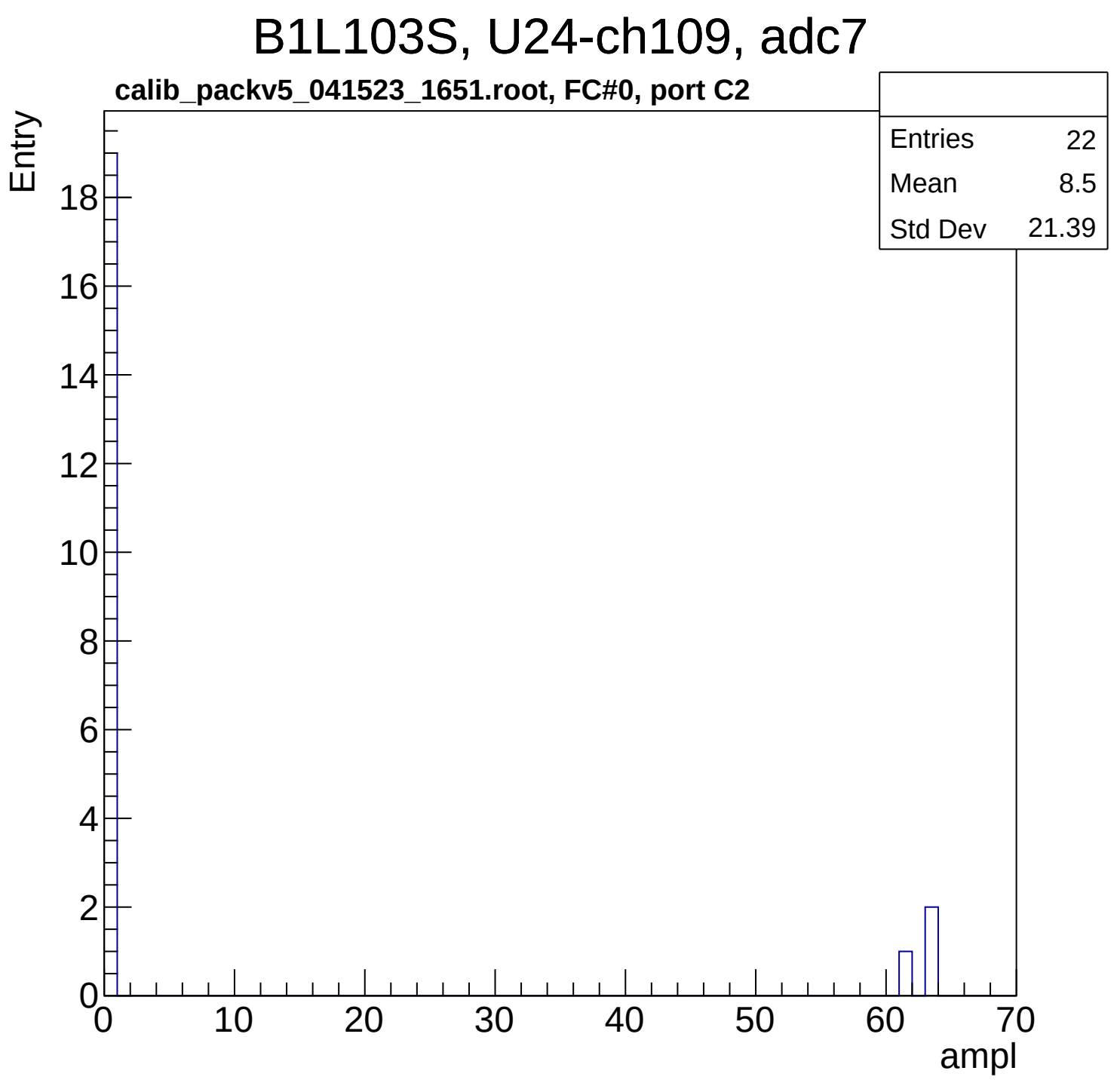
40
50
60
70
ampl


B1L103S, U24-ch109, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 54.58
Std Dev 3.287
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U24-ch109, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 57.98
Std Dev 9.208
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U24-ch109, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 13
Mean 61.15
Std Dev 2.032
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U24-ch109, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 8.5
Std Dev 21.39
Entry
0
2
4
6
8
10
12
14
16
18
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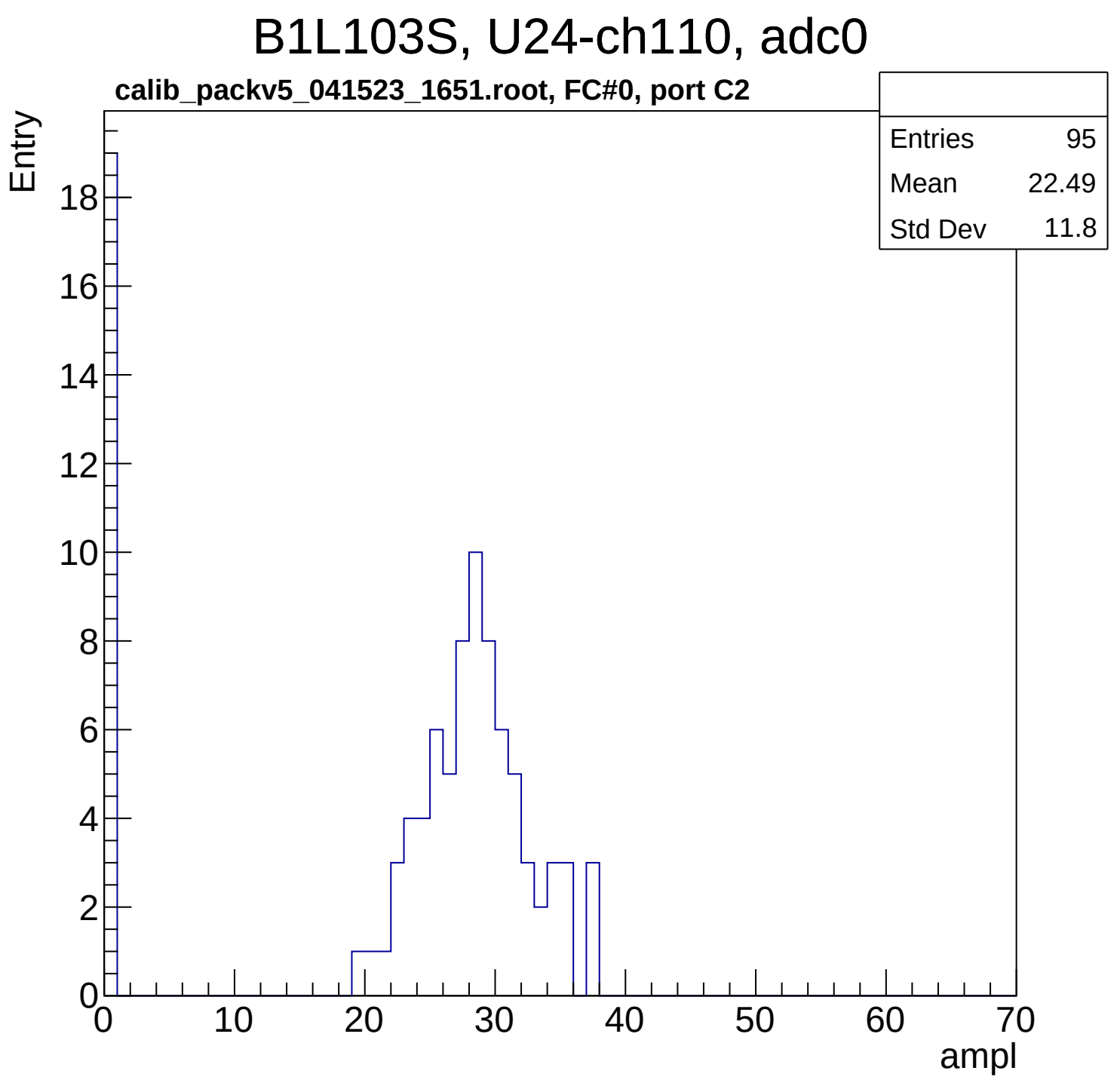
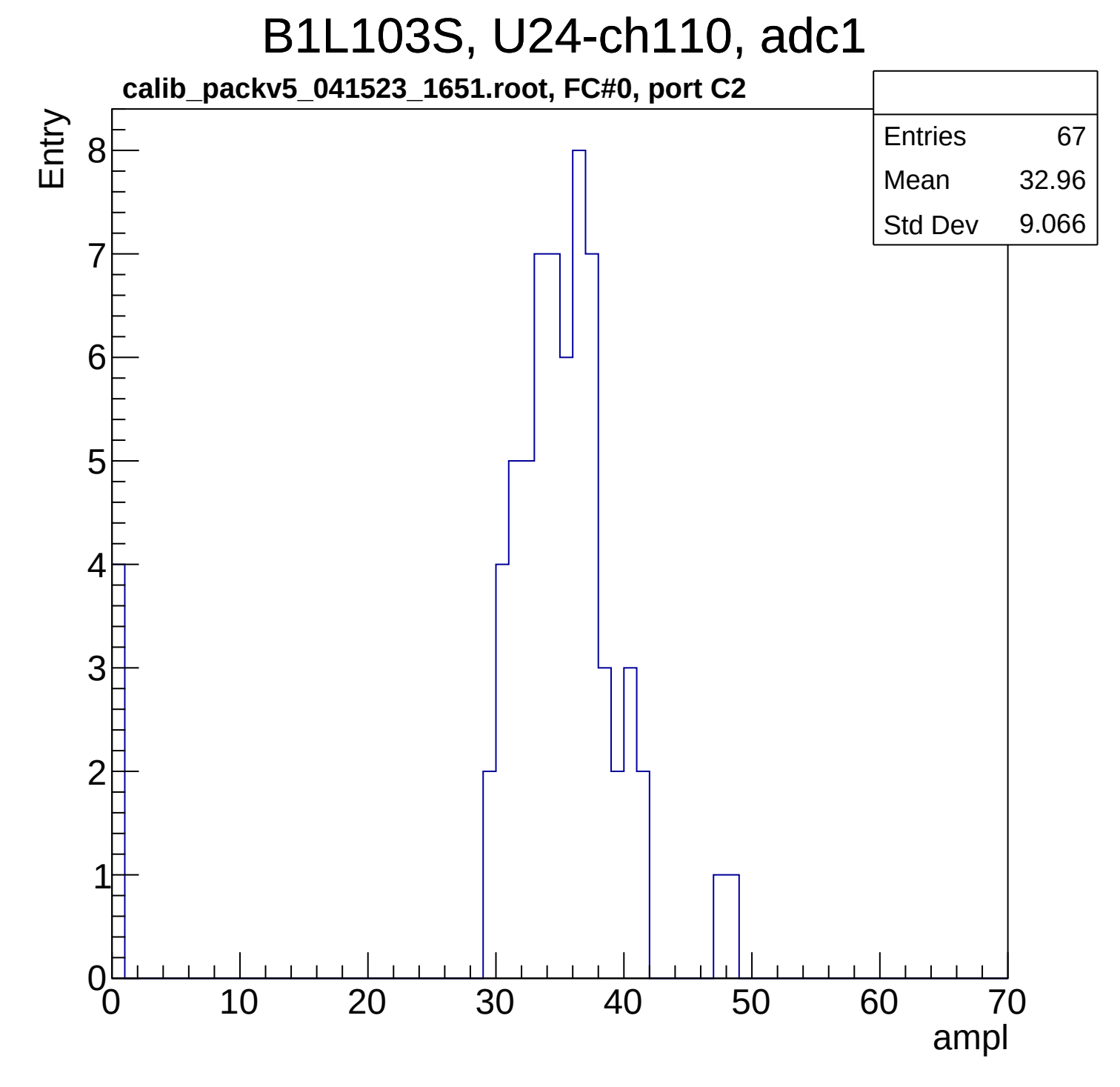
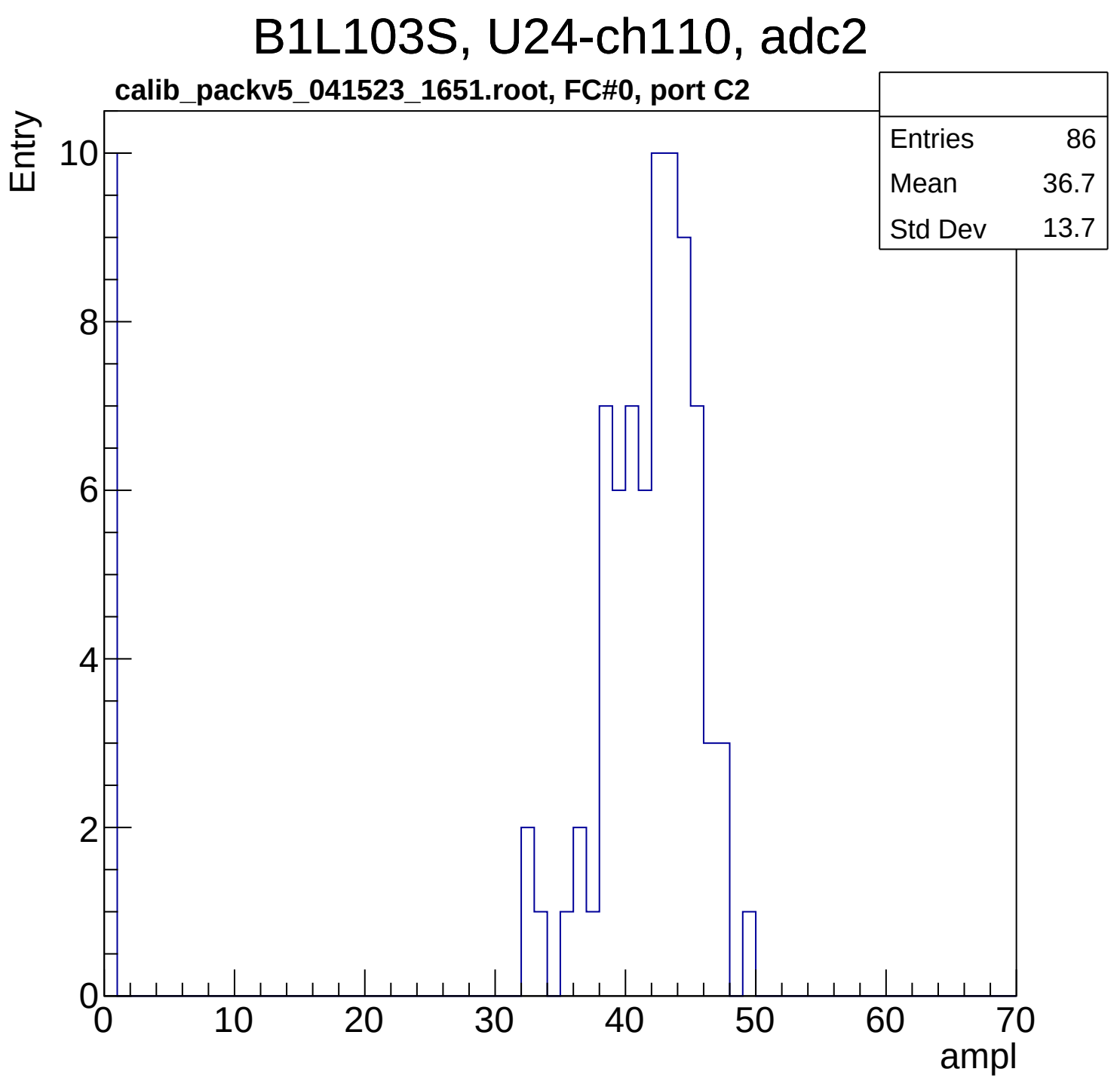
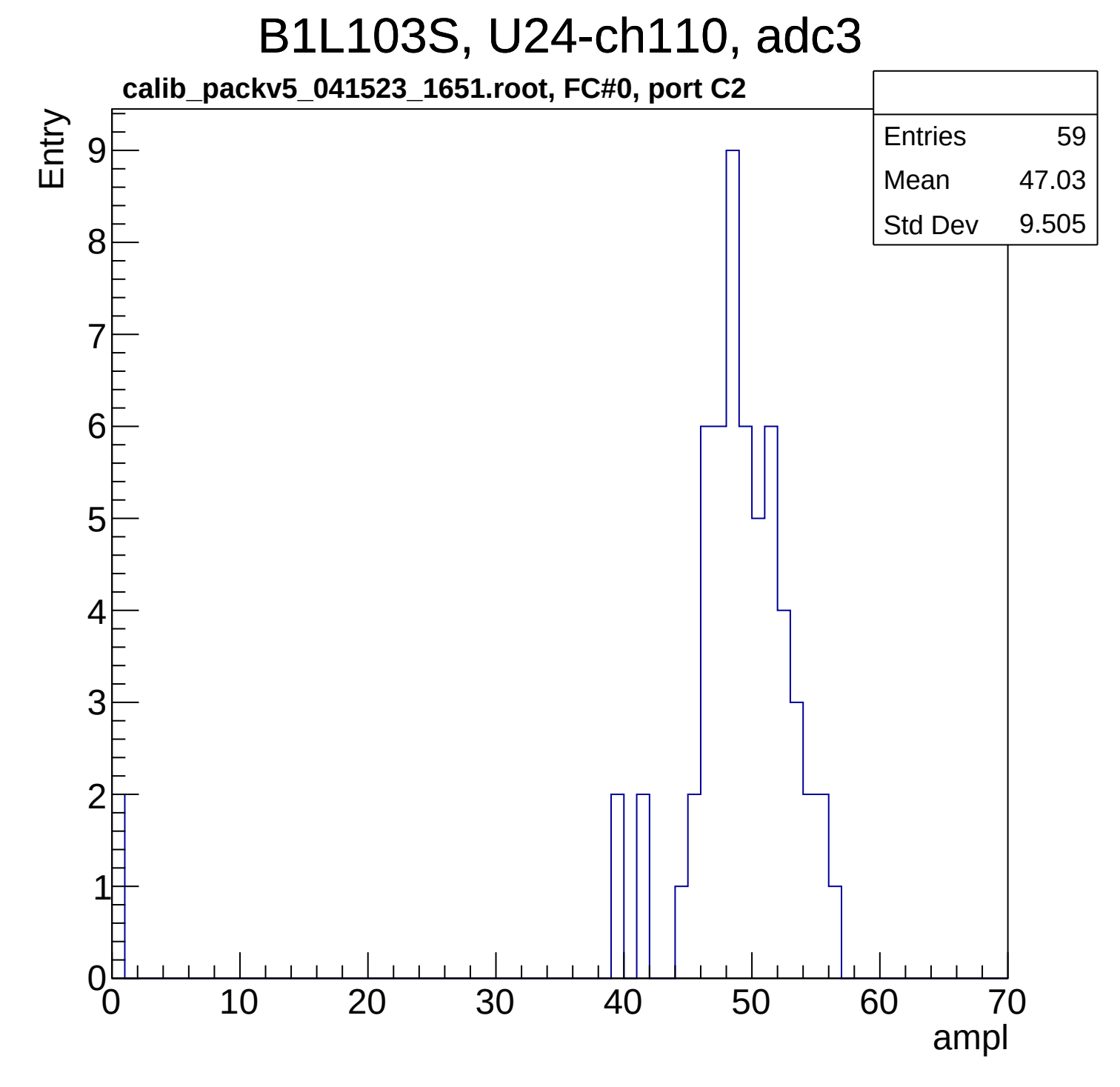
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch110, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 95
Mean 22.49
Std Dev 11.8
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch110, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 32.96
Std Dev 9.066
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U24-ch110, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 36.7
Std Dev 13.7
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch110, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 47.03
Std Dev 9.505
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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40
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60
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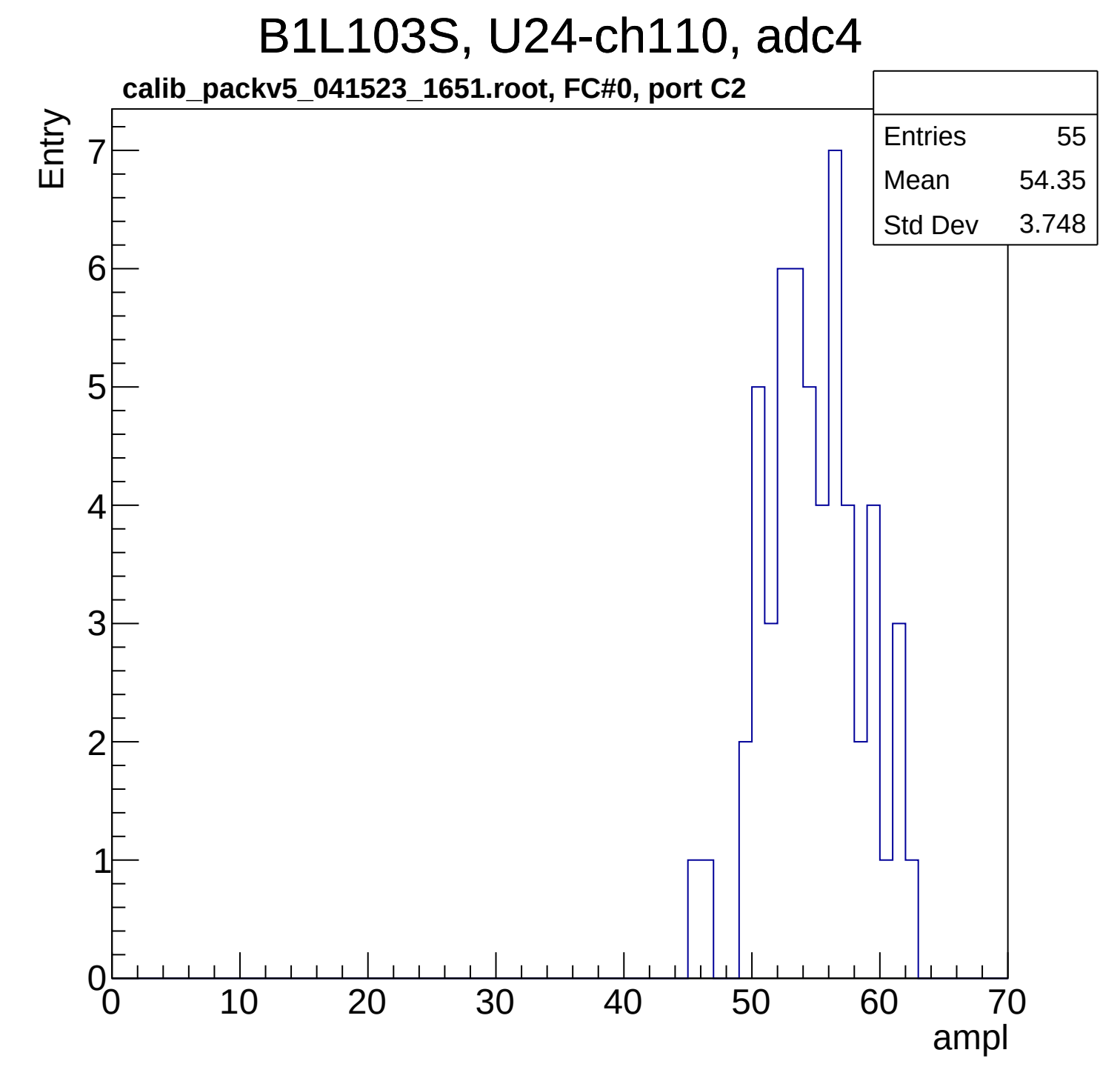
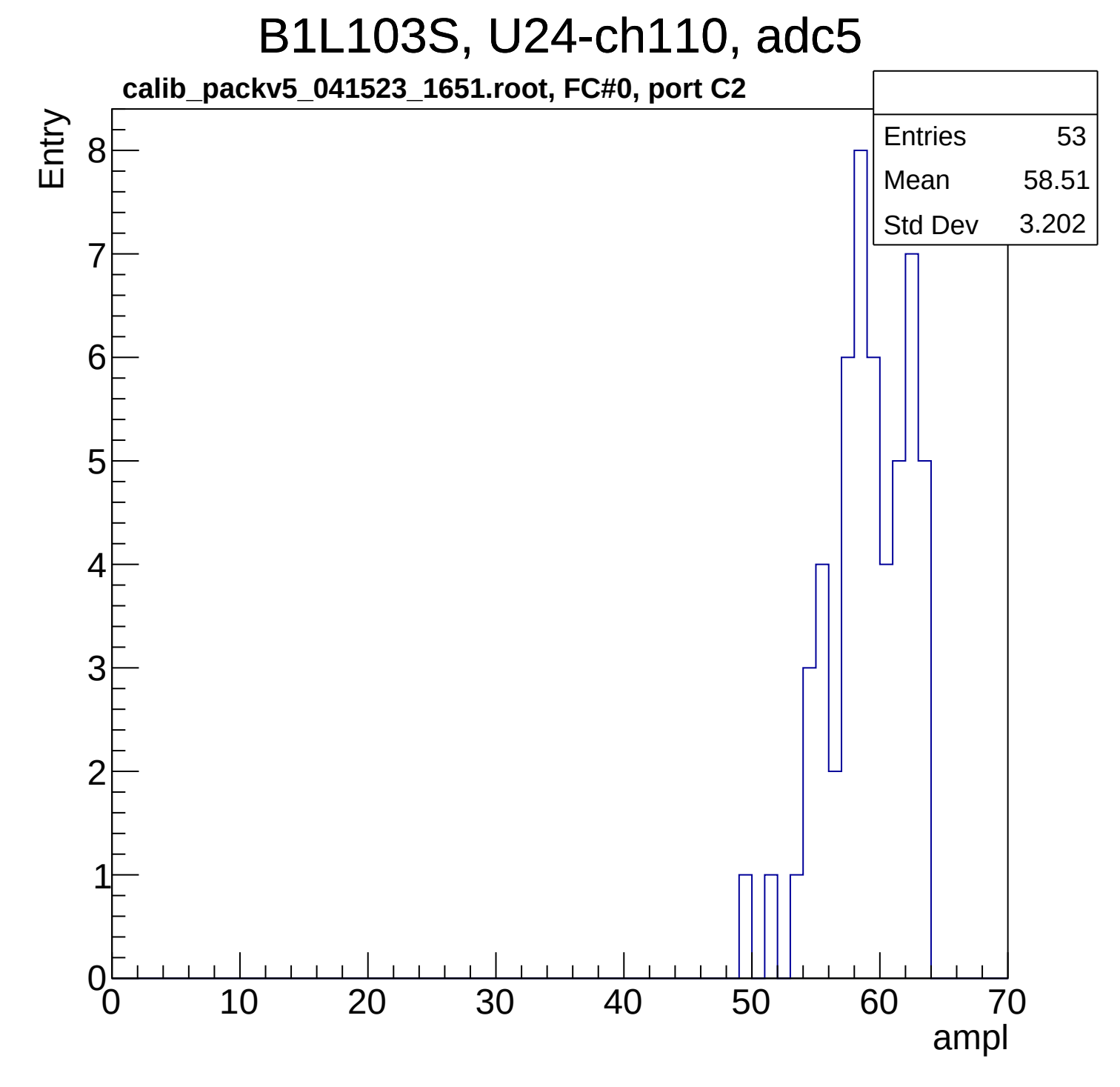

B1L103S, U24-ch110, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 54.35
Std Dev 3.748
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U24-ch110, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 58.51
Std Dev 3.202
Entry
ampl
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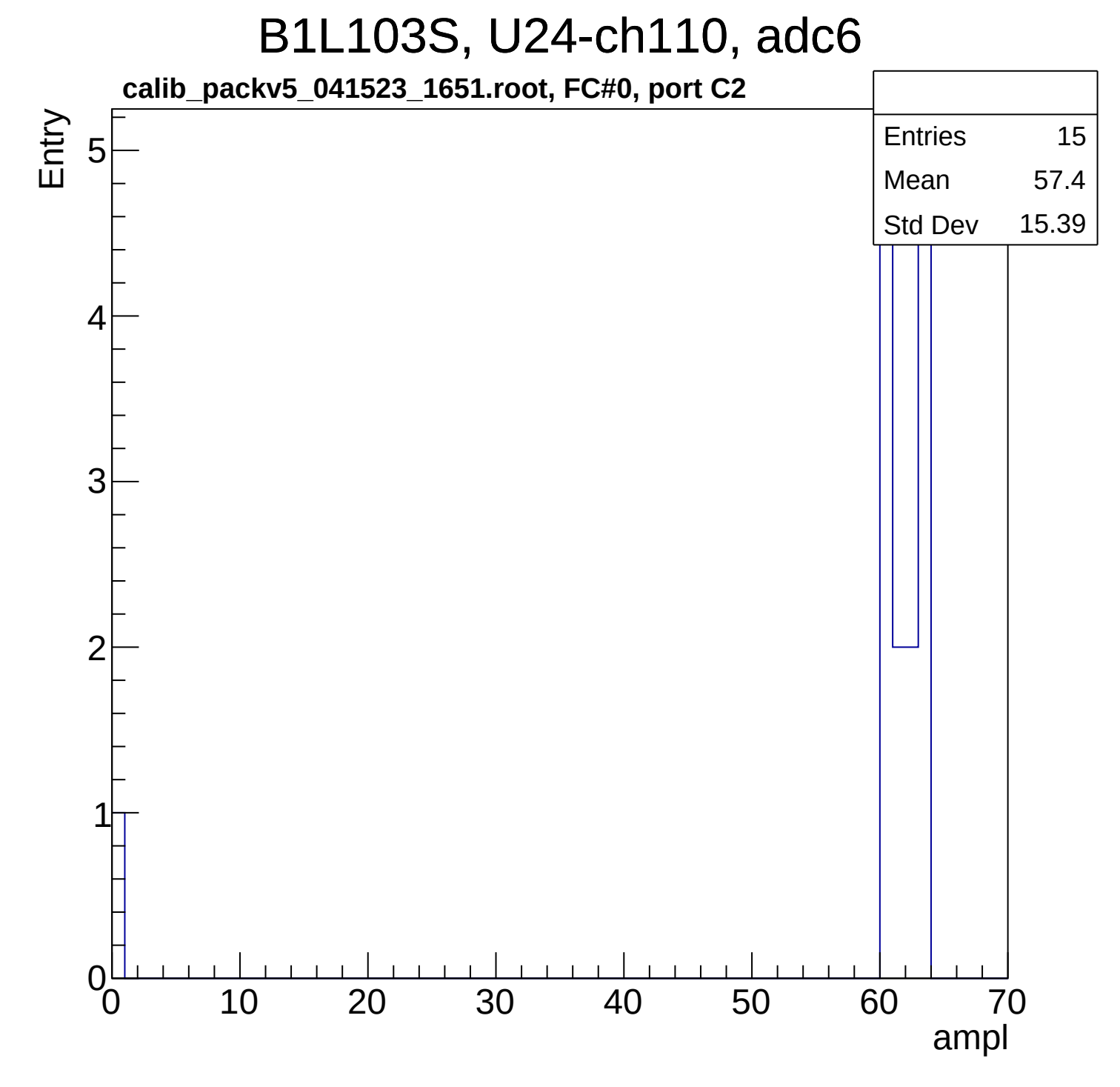
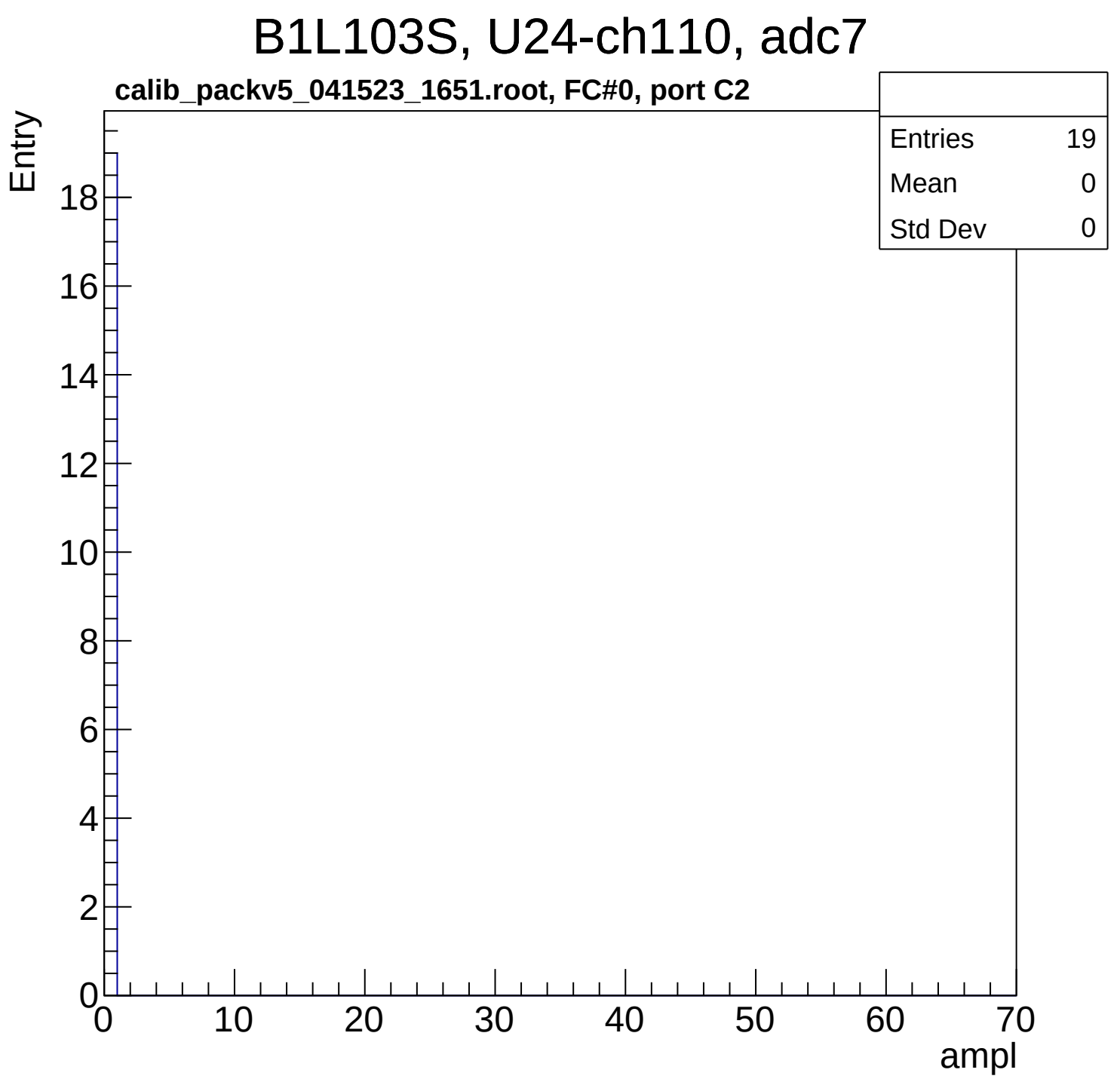
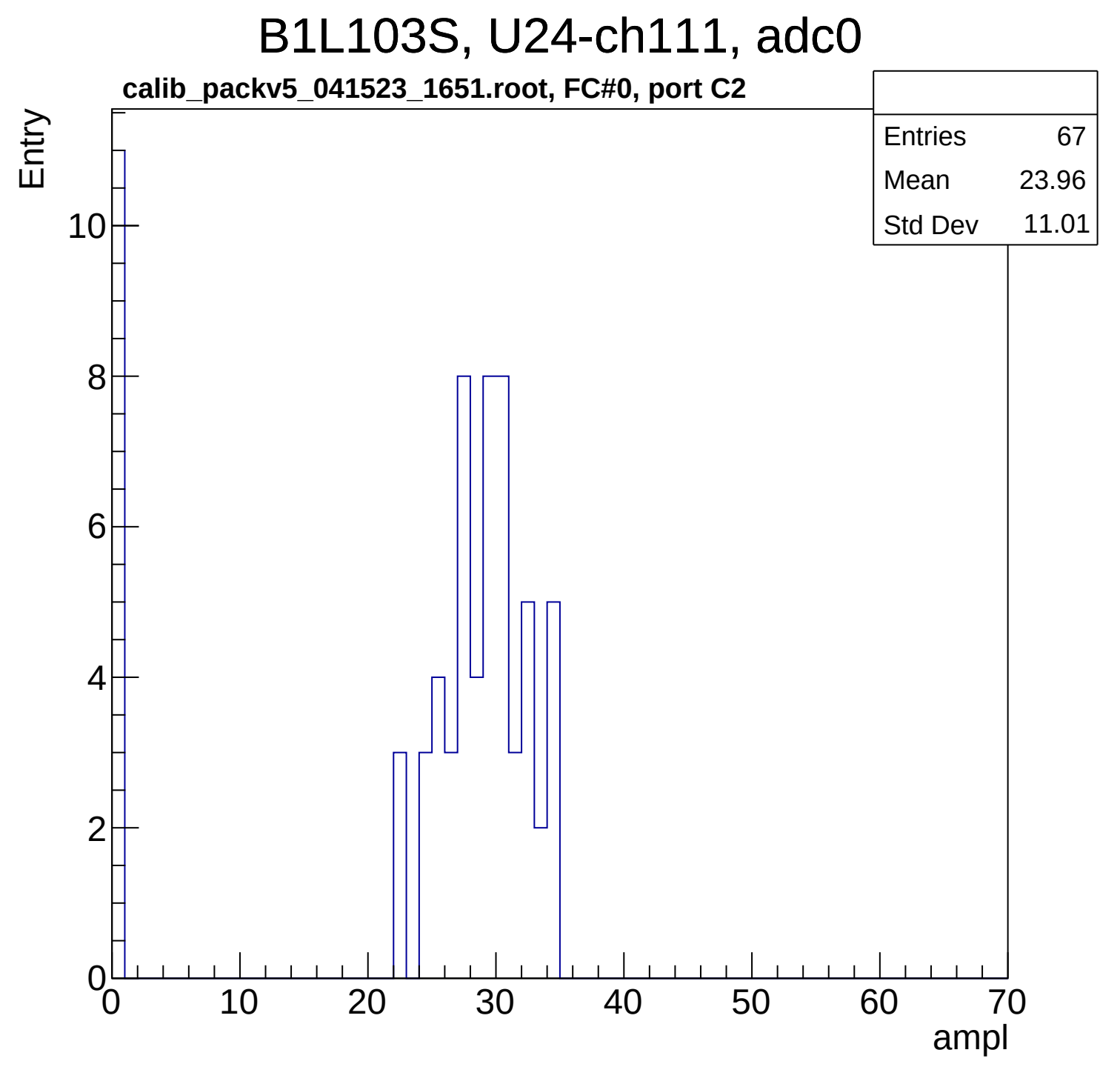
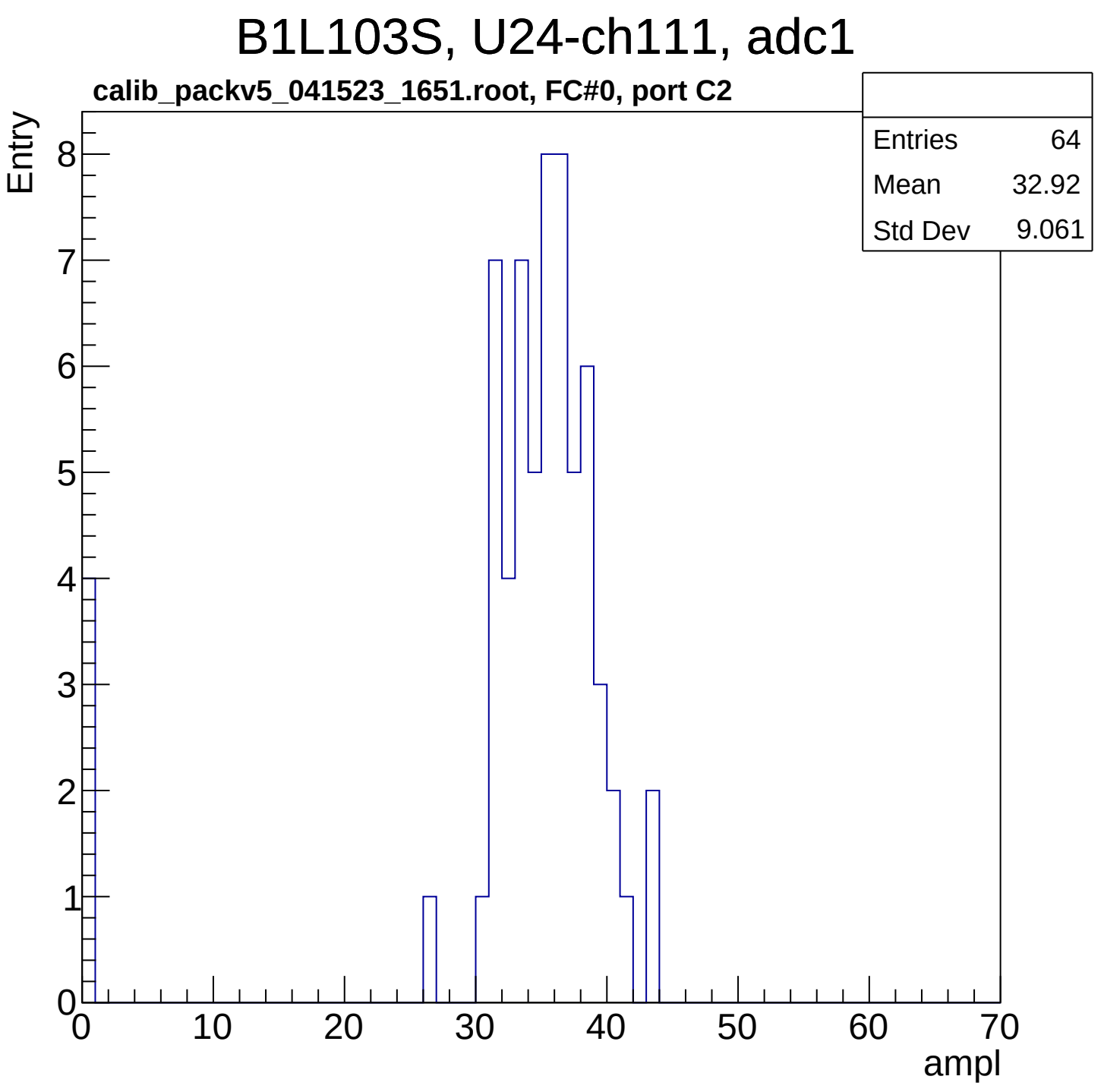
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U24-ch110, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 15
Mean 57.4
Std Dev 15.39
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U24-ch110, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch111, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 23.96
Std Dev 11.01
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch111, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 32.92
Std Dev 9.061
Entry
ampl
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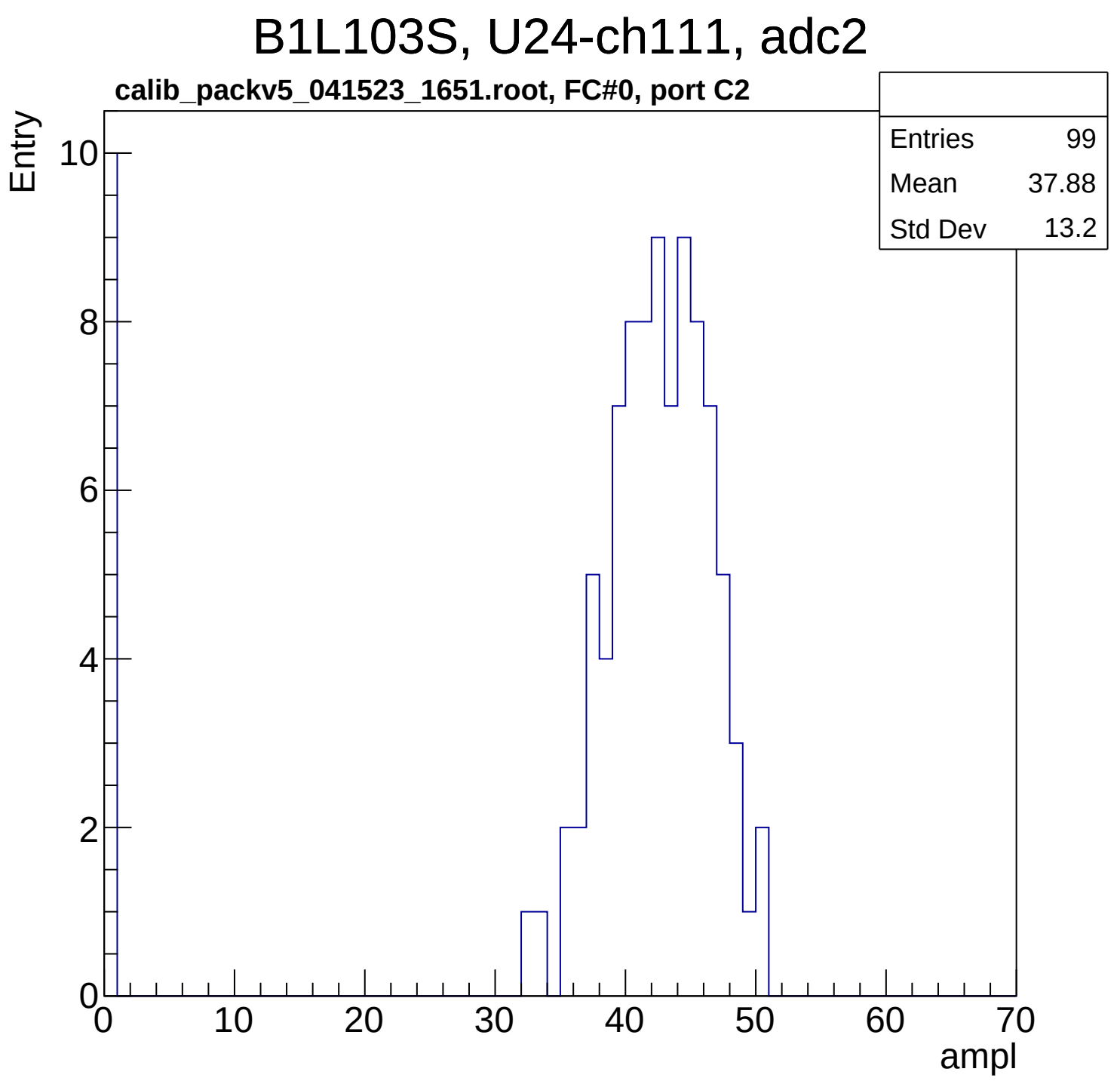
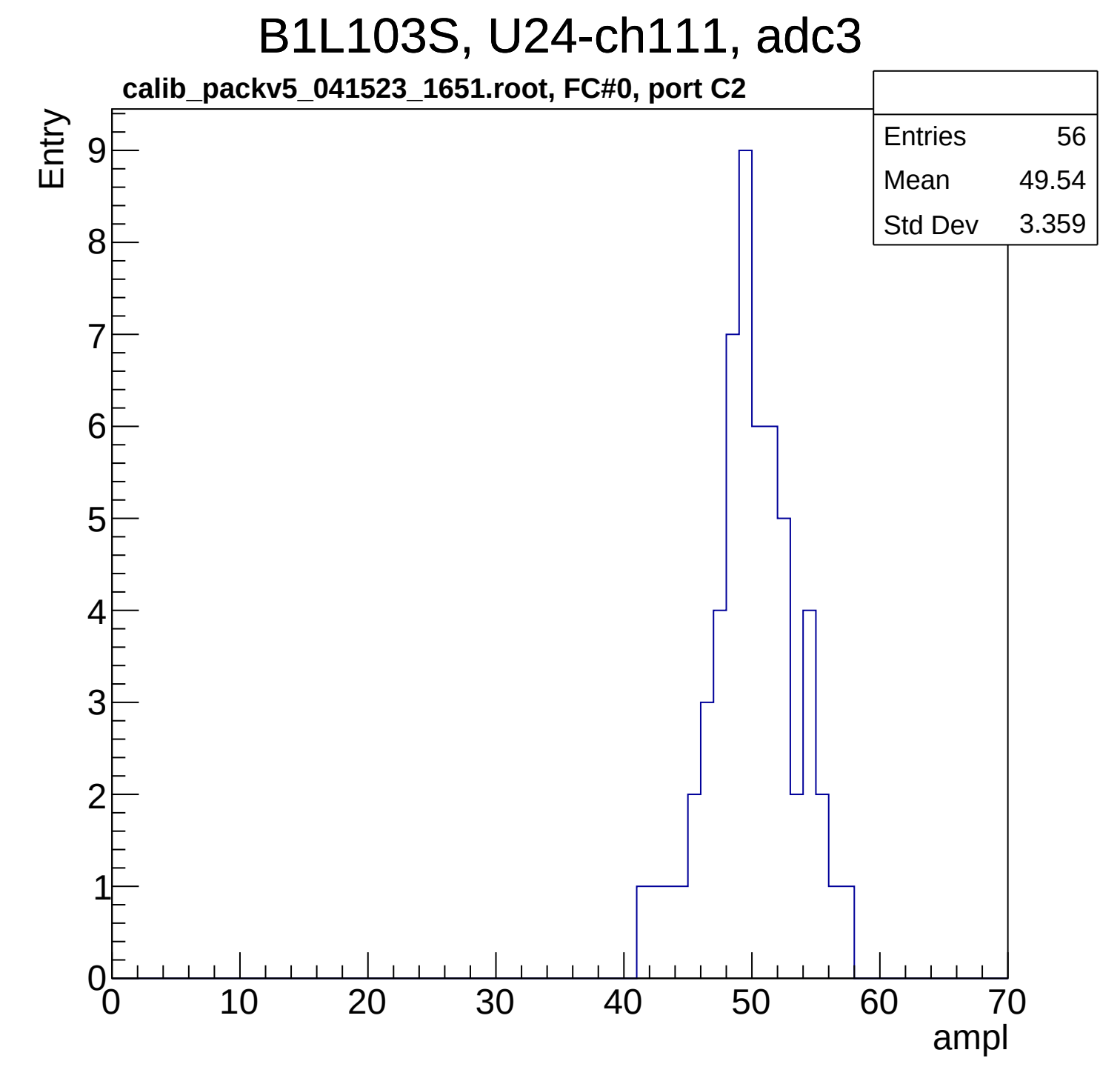
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U24-ch111, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 99
Mean 37.88
Std Dev 13.2
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U24-ch111, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 49.54
Std Dev 3.359
Entry
ampl
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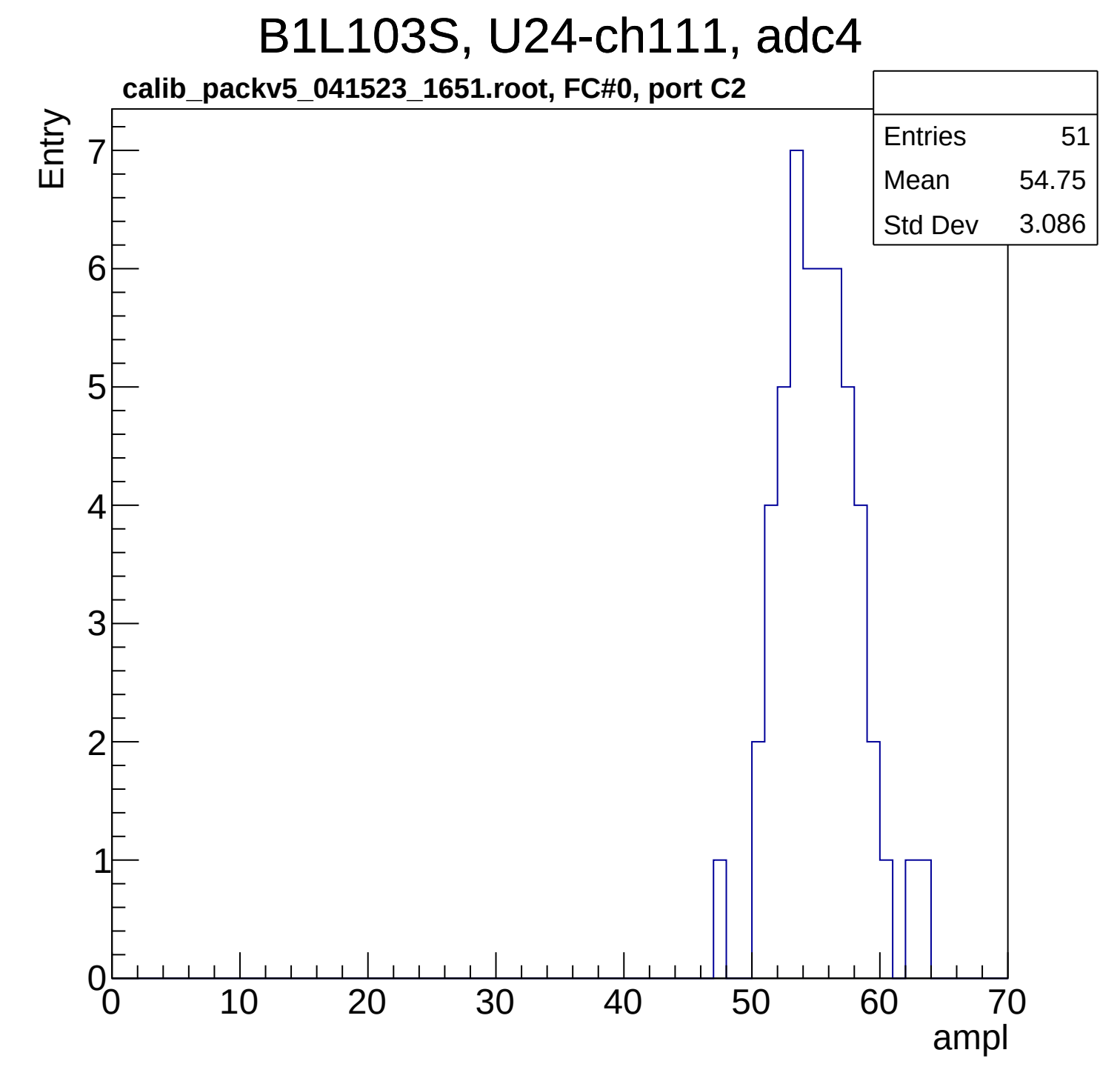
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U24-ch111, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 54.75
Std Dev 3.086
Entry
ampl
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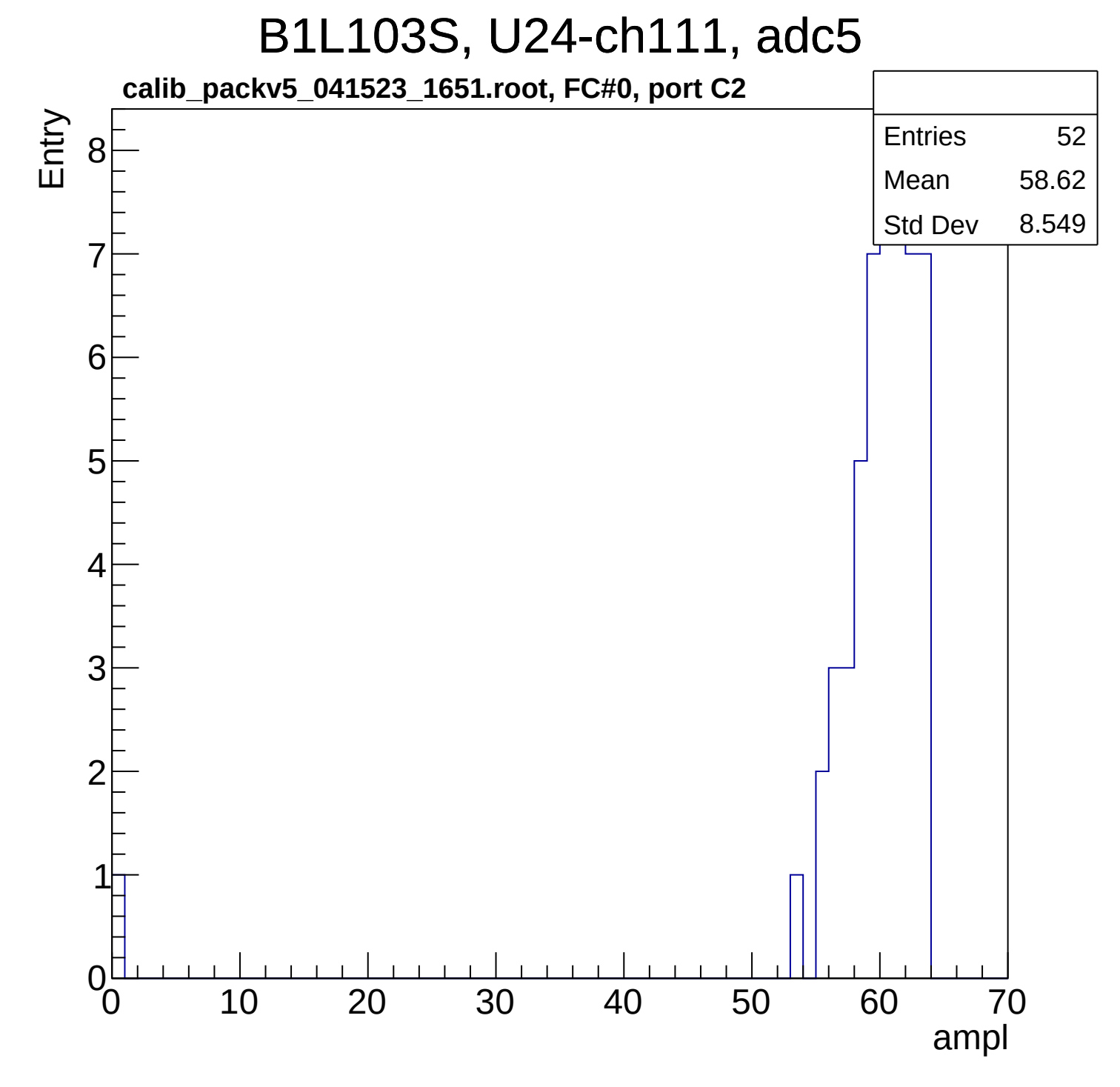
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U24-ch111, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 58.62
Std Dev 8.549
Entry
ampl
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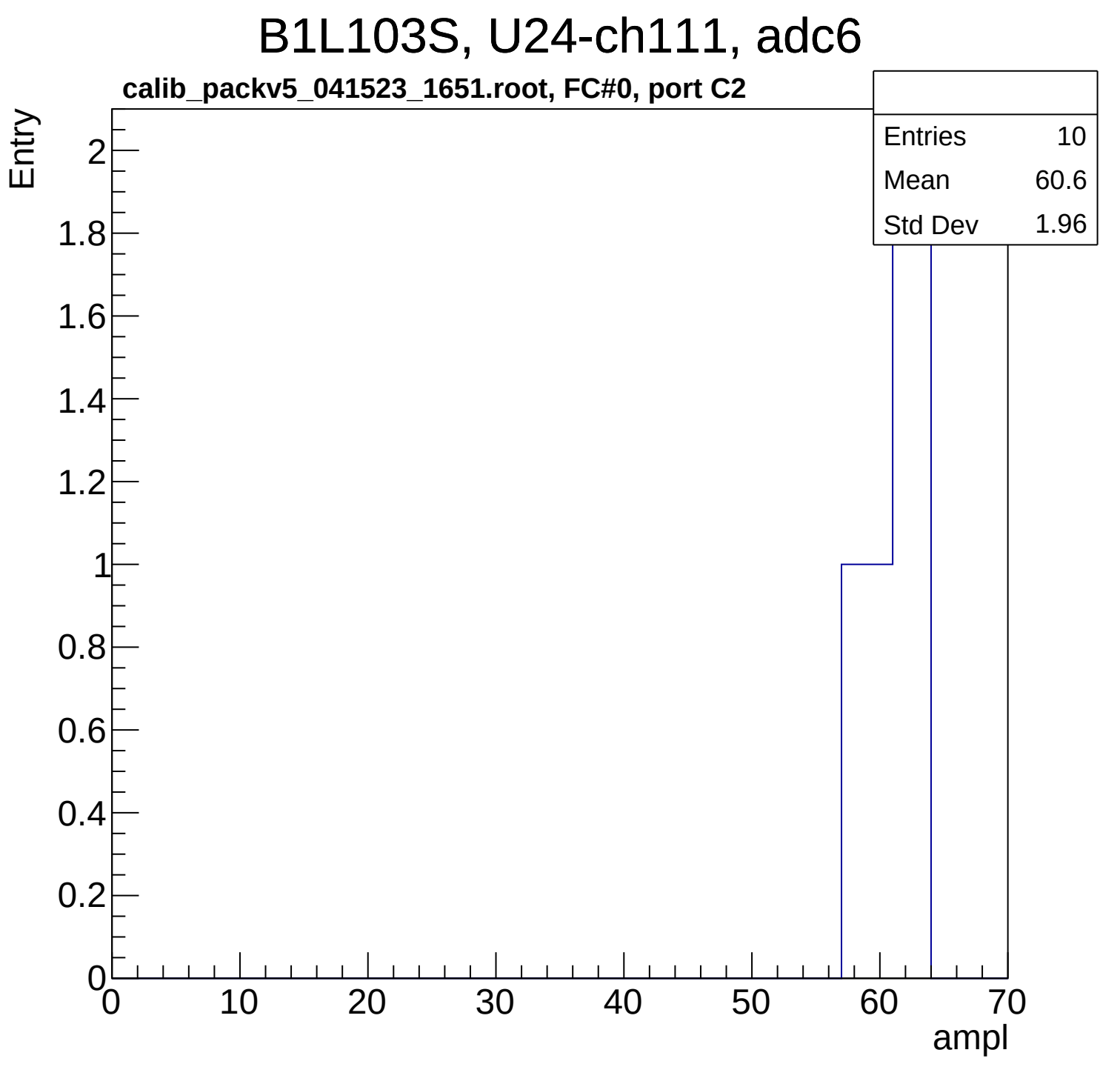
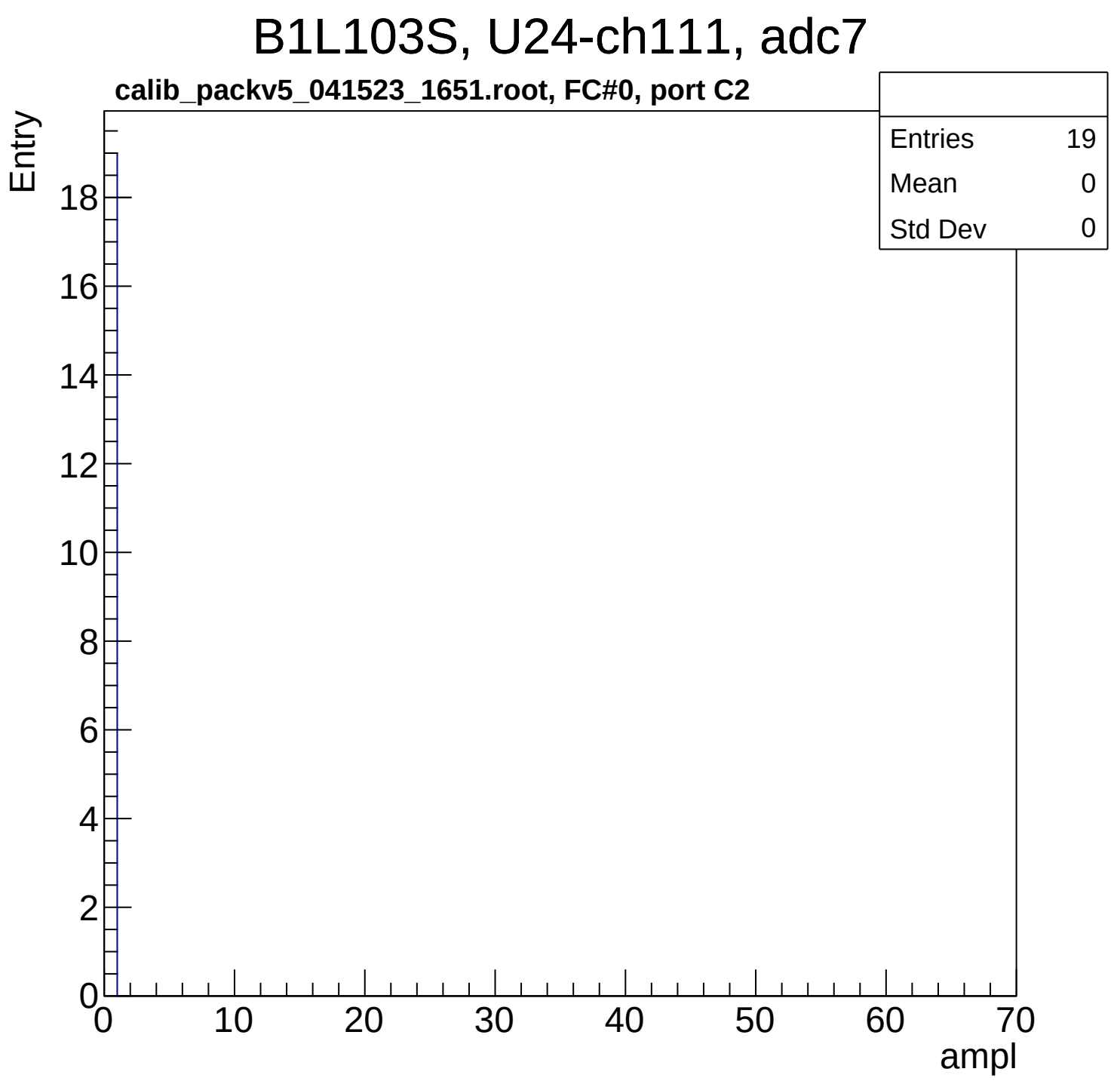
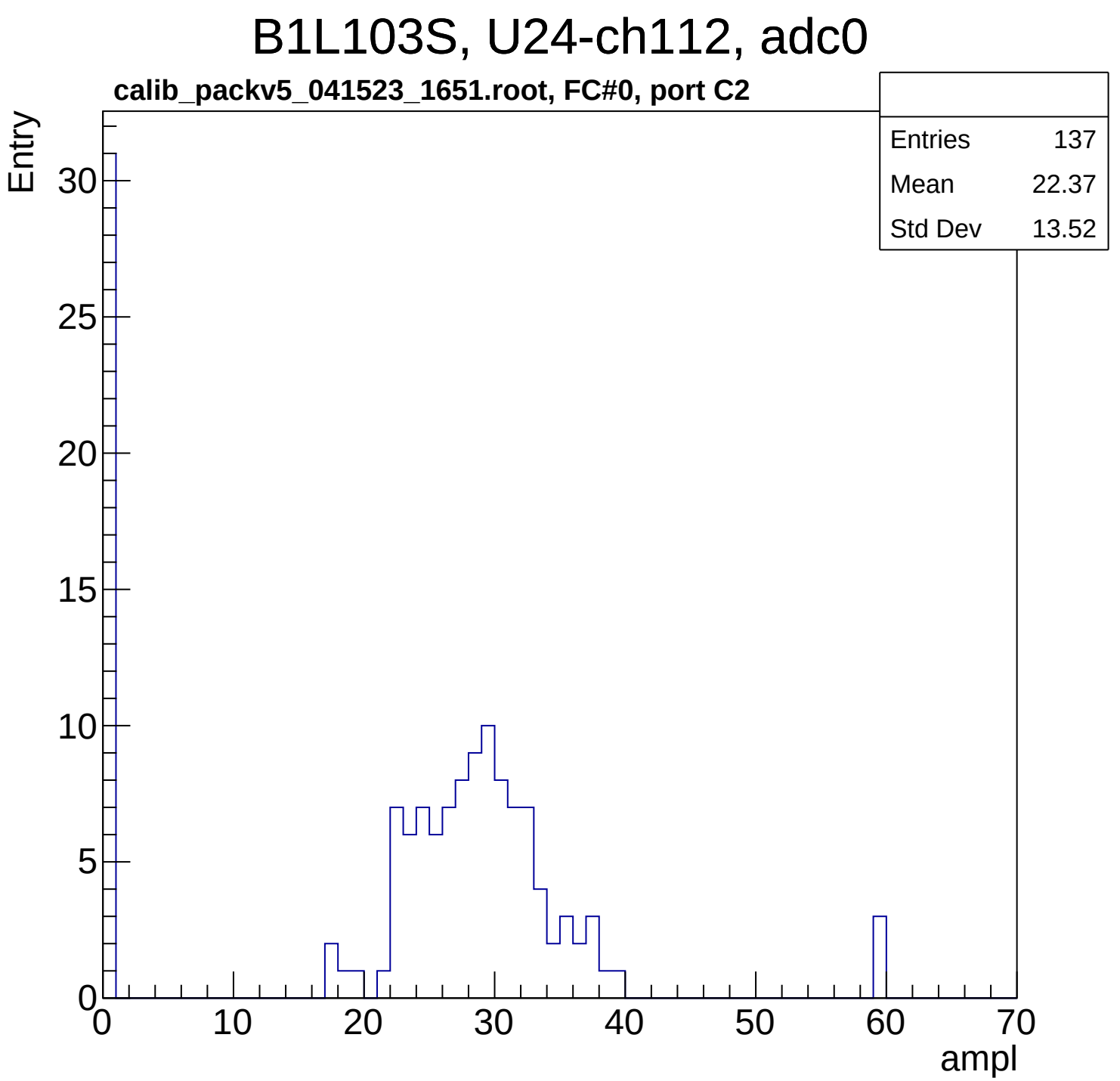
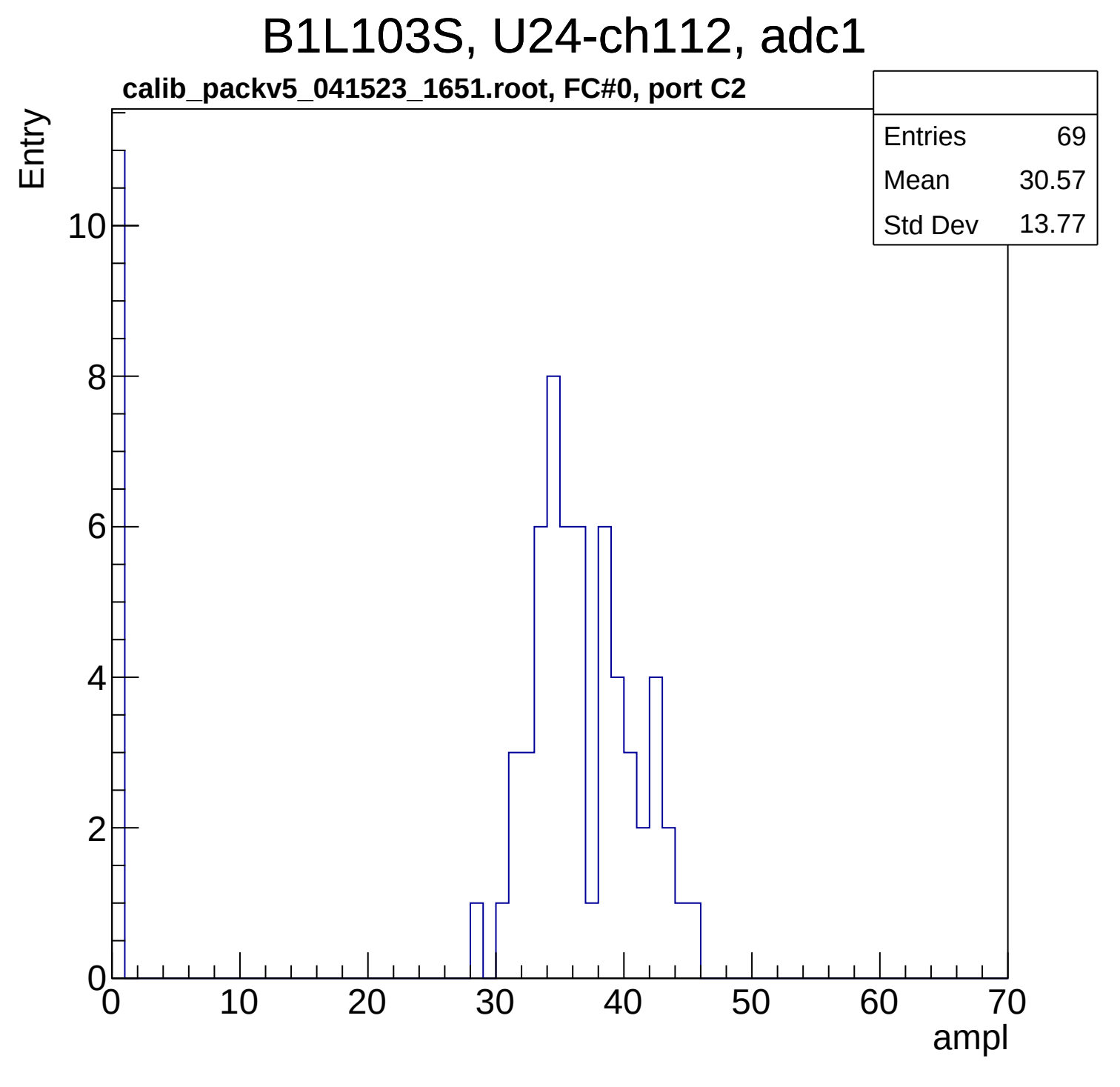
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U24-ch111, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 60.6
Std Dev 1.96
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U24-ch111, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch112, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 137
Mean 22.37
Std Dev 13.52
Entry
0
5
10
15
20
25
30
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch112, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 30.57
Std Dev 13.77
Entry
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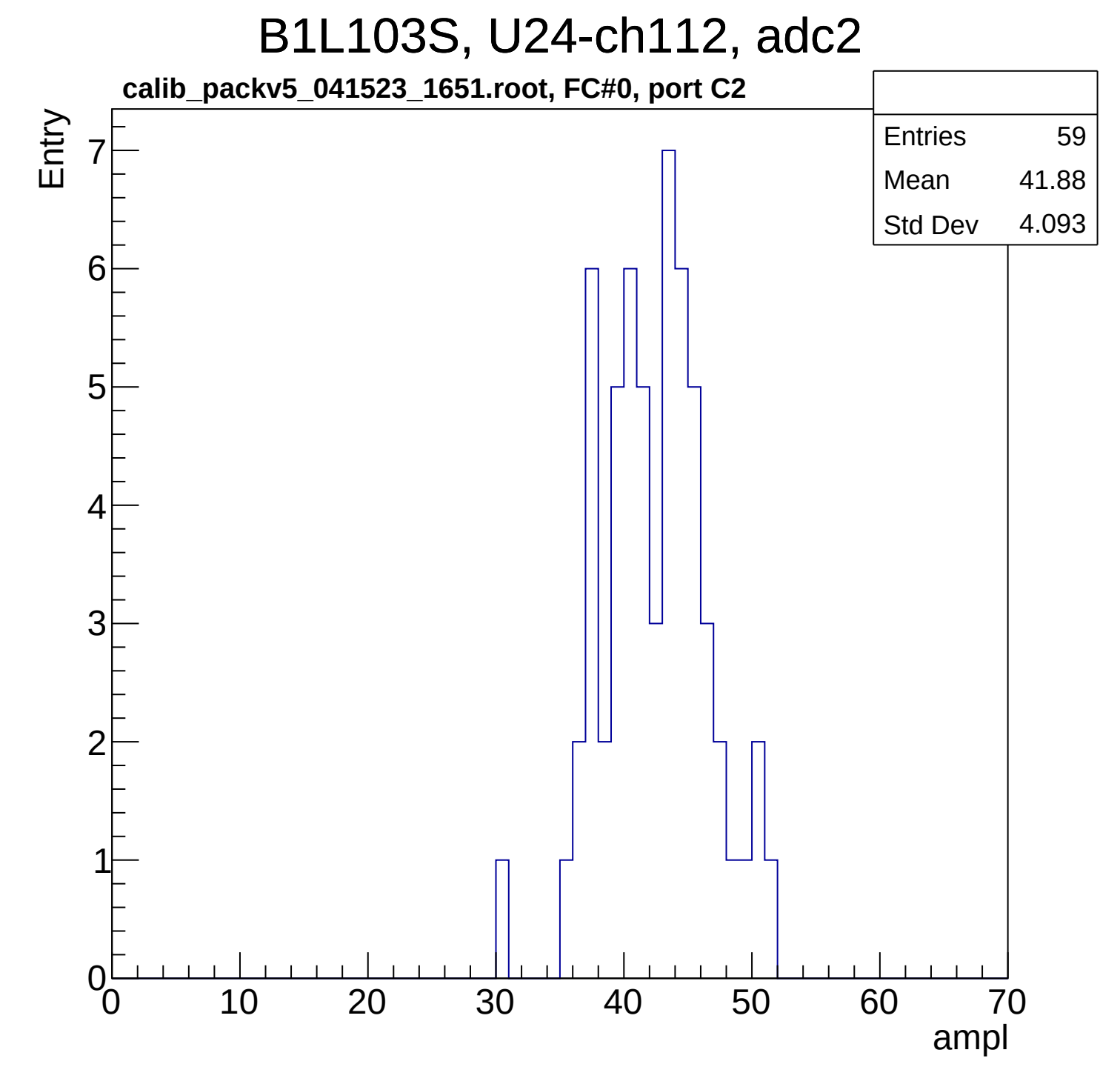
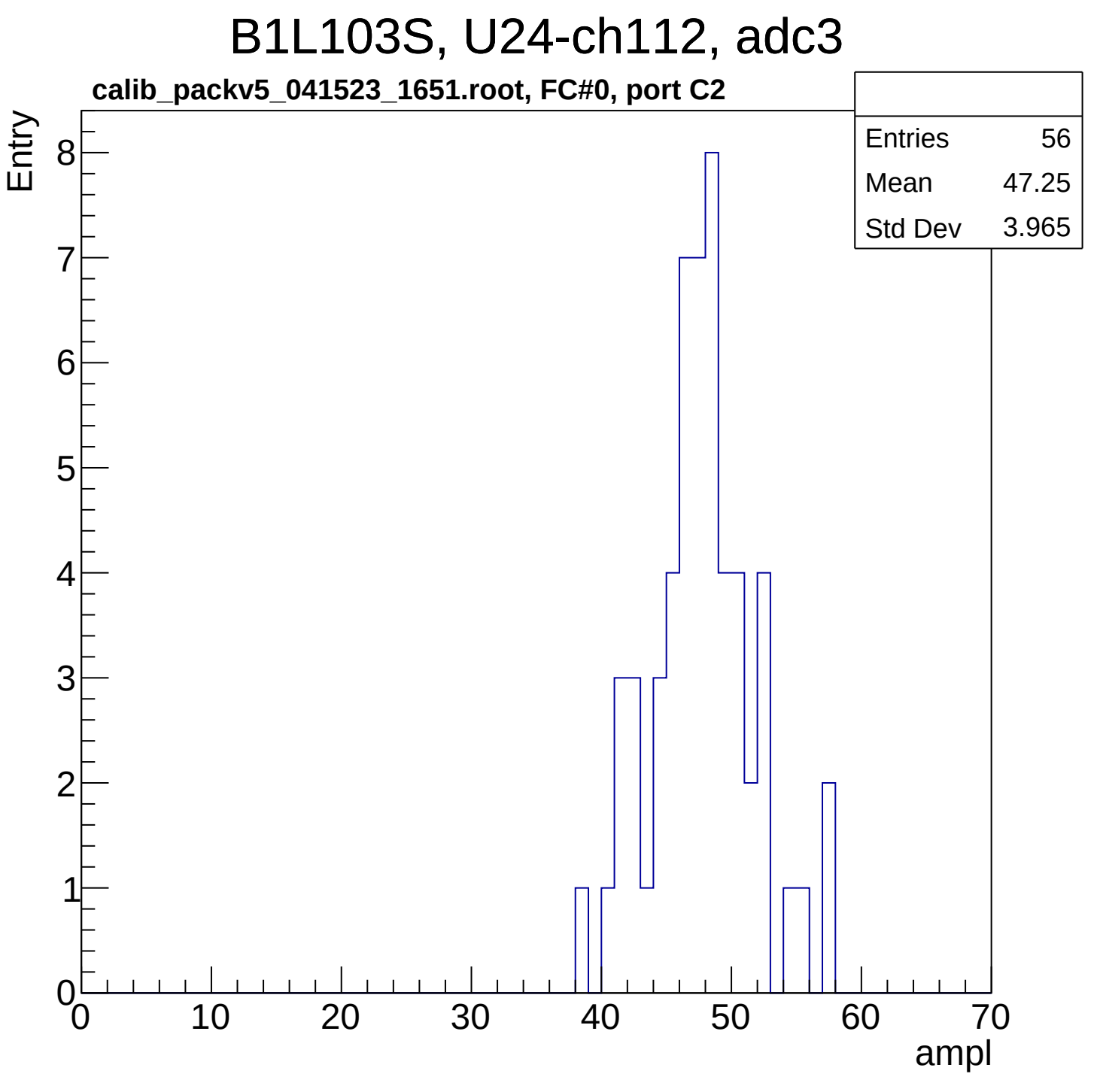
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch112, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 41.88
Std Dev 4.093
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U24-ch112, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 47.25
Std Dev 3.965
Entry
ampl
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2
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0
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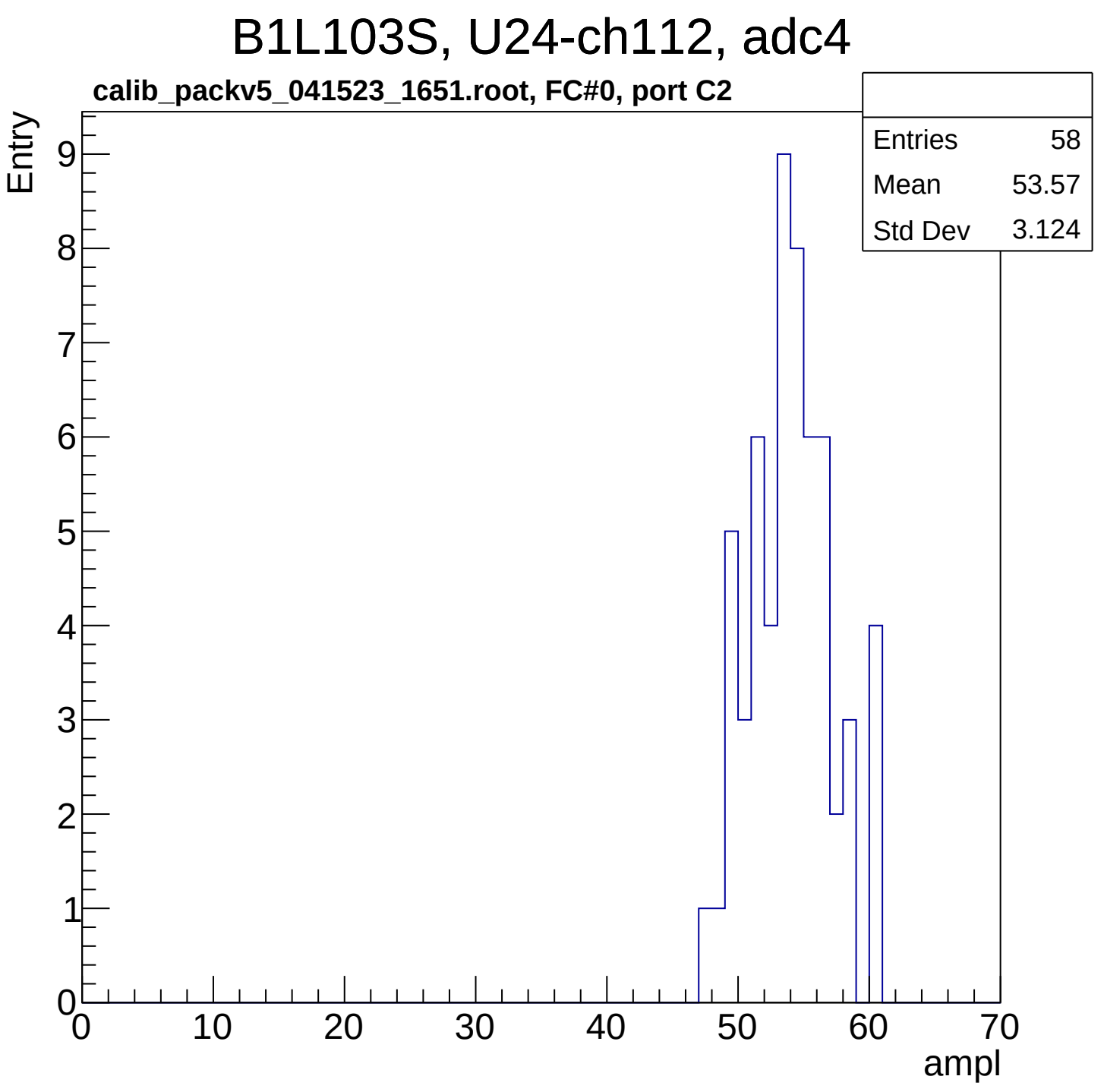
B1L103S, U24-ch112, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 53.57
Std Dev 3.124
Entry
ampl
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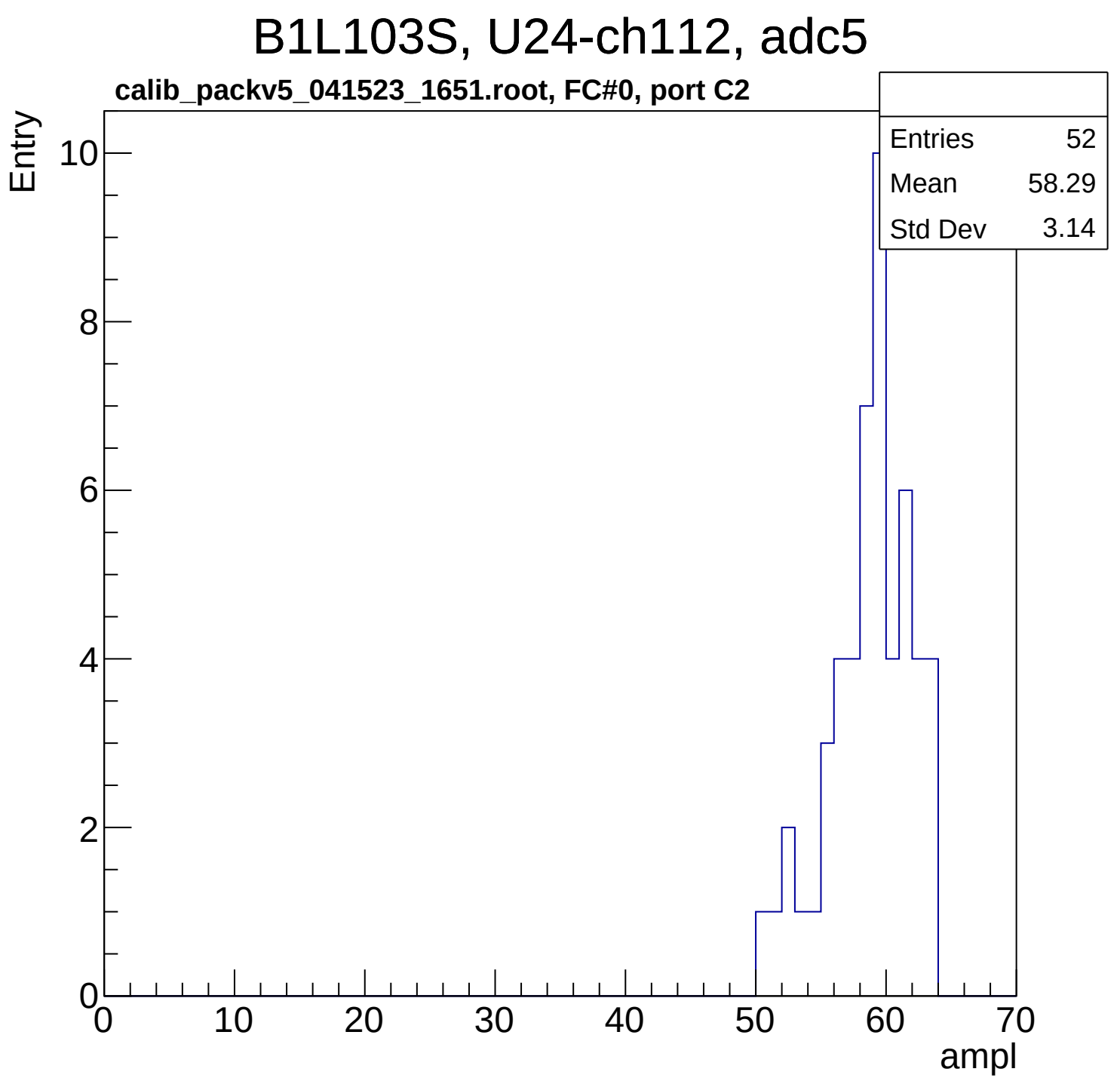
B1L103S, U24-ch112, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 58.29
Std Dev 3.14
Entry
ampl
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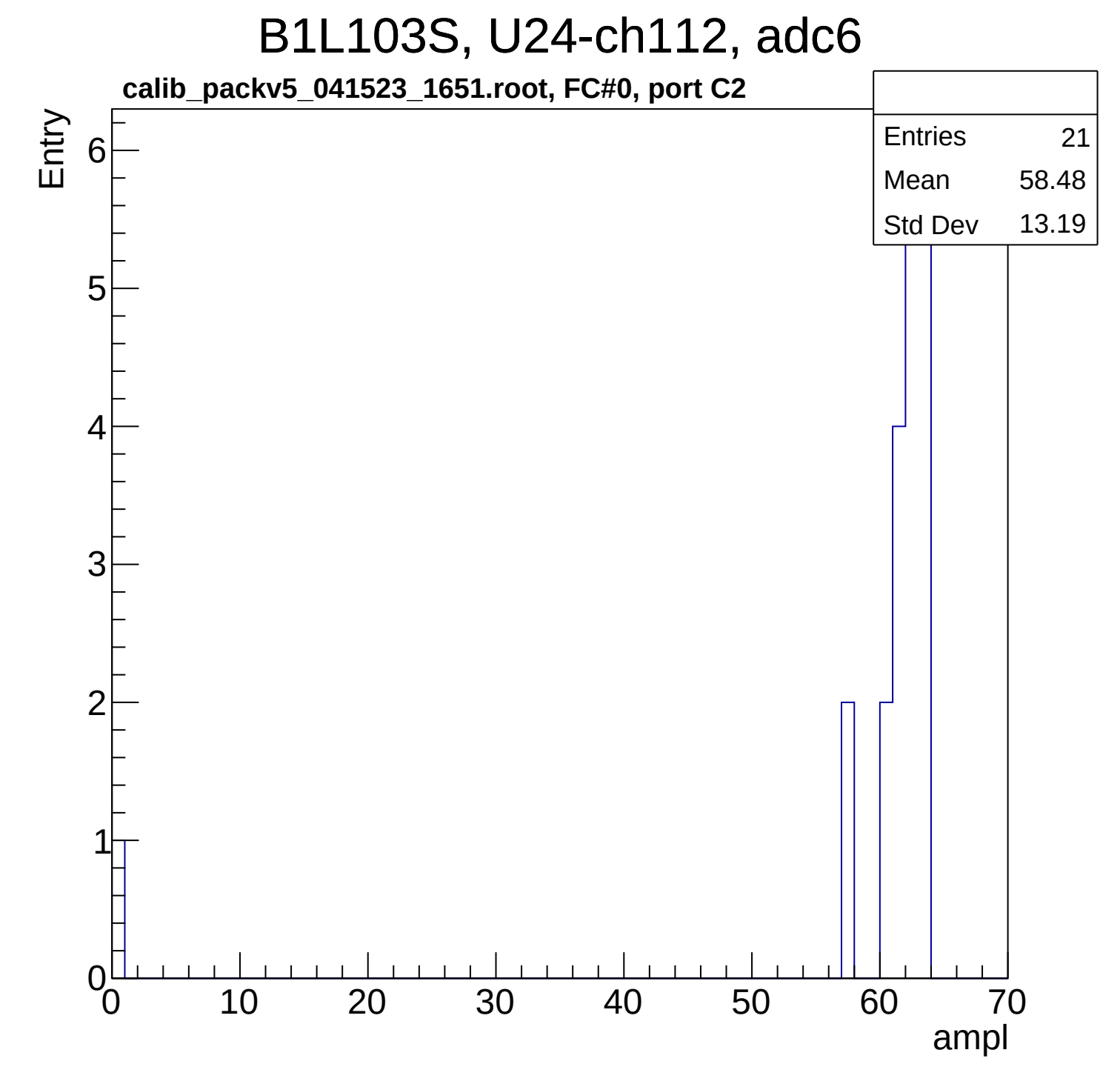
B1L103S, U24-ch112, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 58.48
Std Dev 13.19
Entry
0
1
2
3
4
5
6
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10
20
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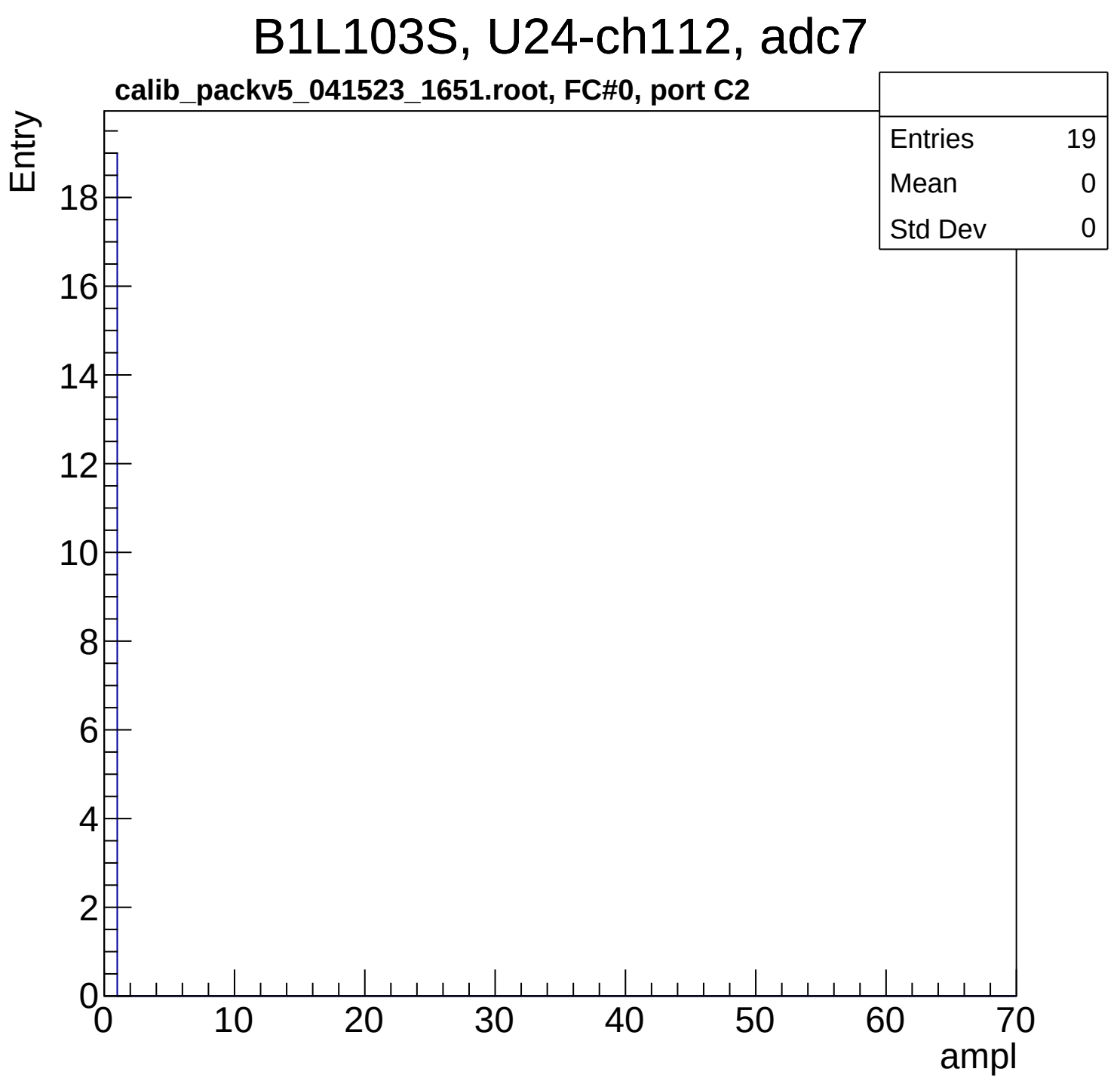
40
50
60
70
ampl


B1L103S, U24-ch112, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
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6
8
10
12
14
16
18
0
10
20
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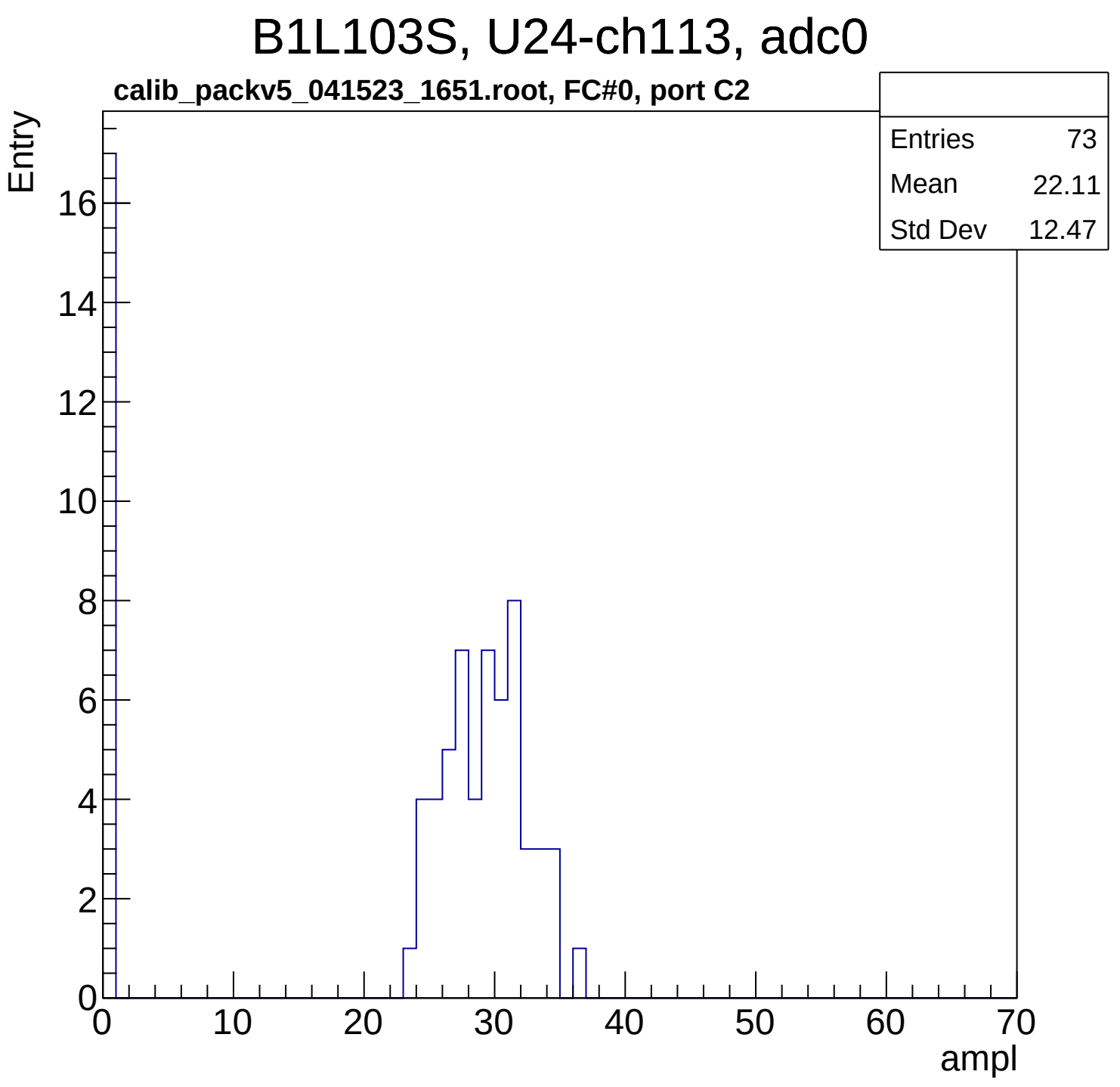
50
60
70
ampl


B1L103S, U24-ch113, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 22.11
Std Dev 12.47
Entry
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4
6
8
10
12
14
16
0
10
20
30
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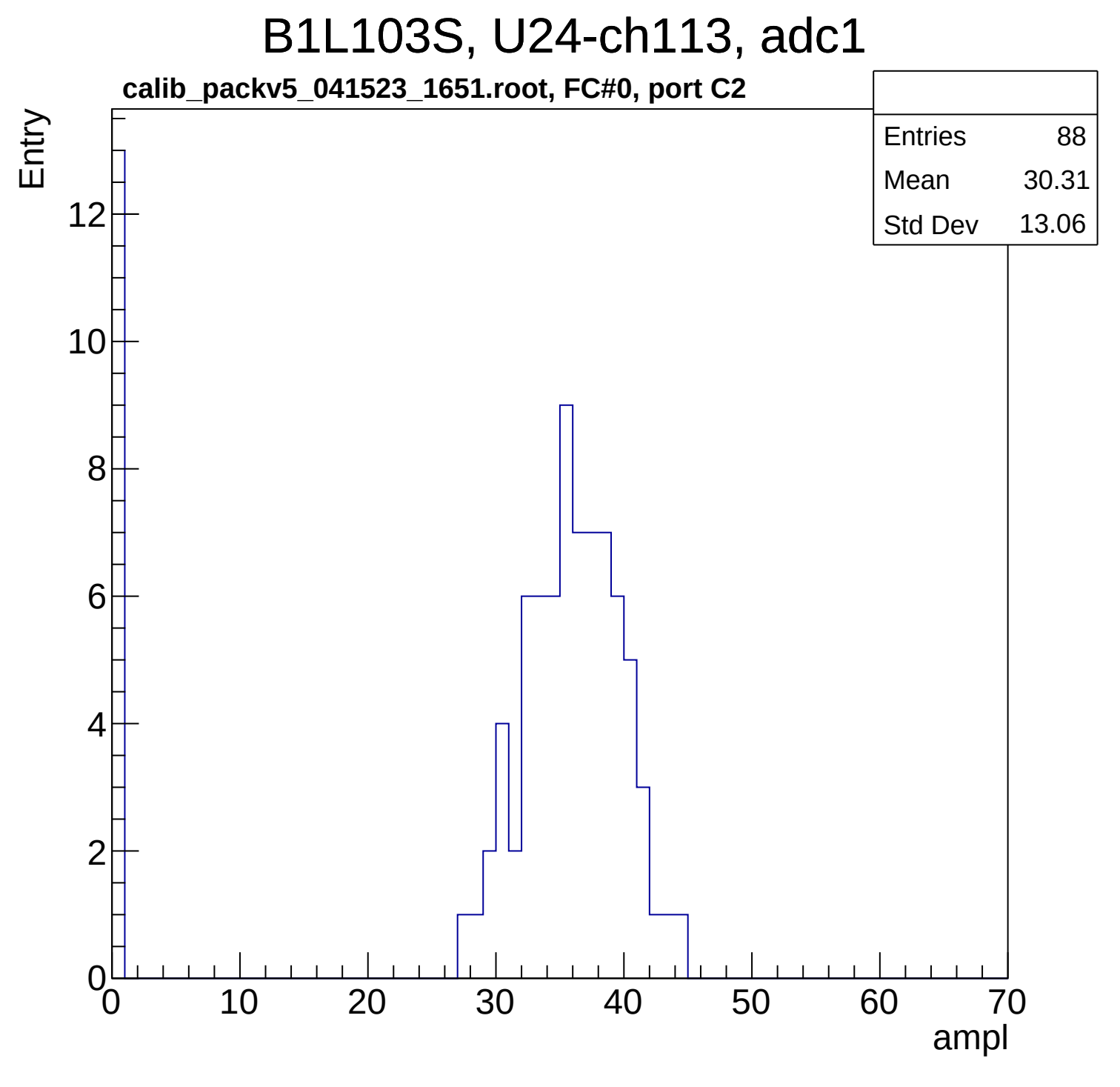
50
60
70
ampl


B1L103S, U24-ch113, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 88
Mean 30.31
Std Dev 13.06
Entry
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12
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10
20
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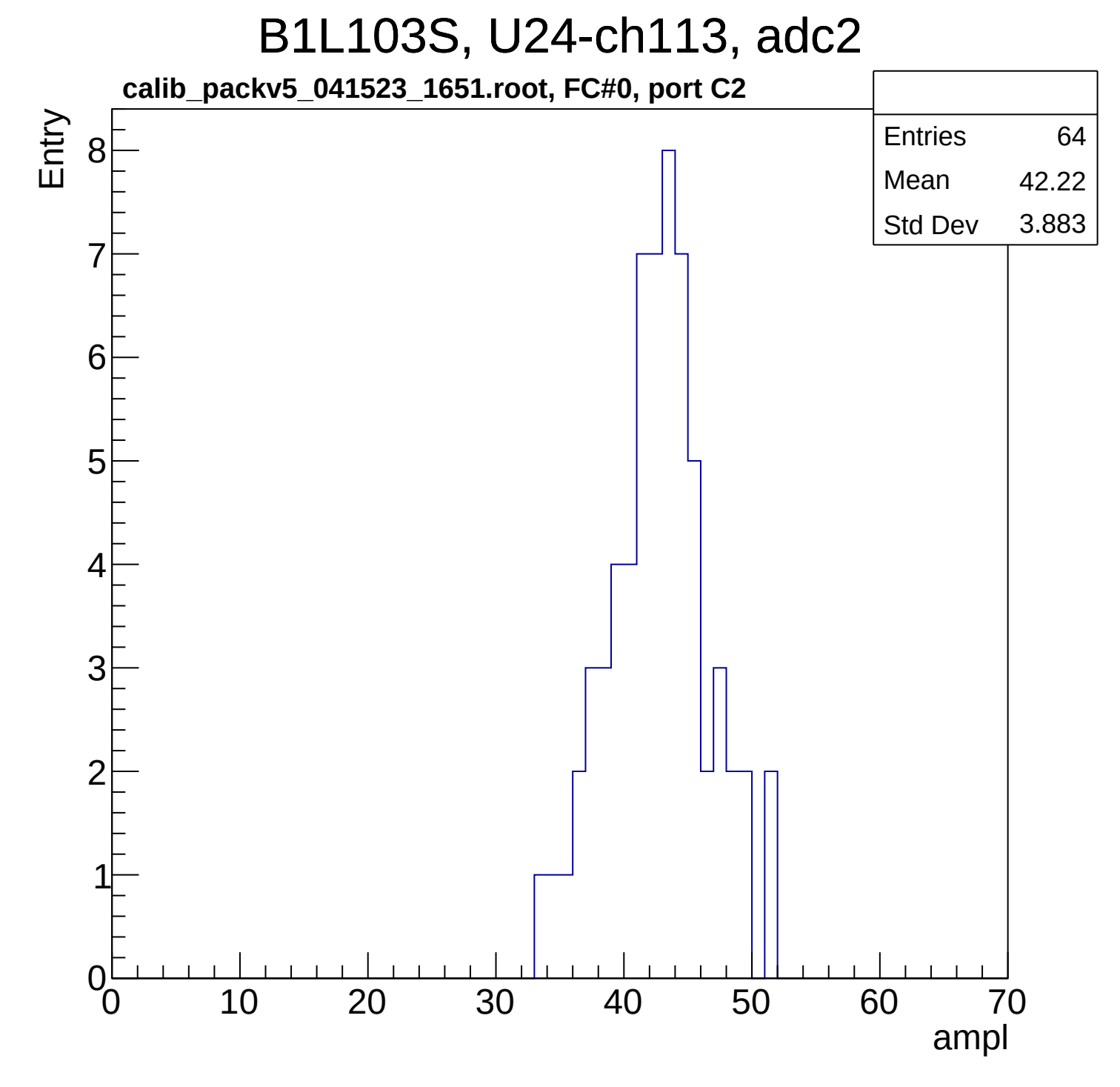
40
50
60
70
ampl


B1L103S, U24-ch113, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 42.22
Std Dev 3.883
Entry
ampl
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4
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7
8
0
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20
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40
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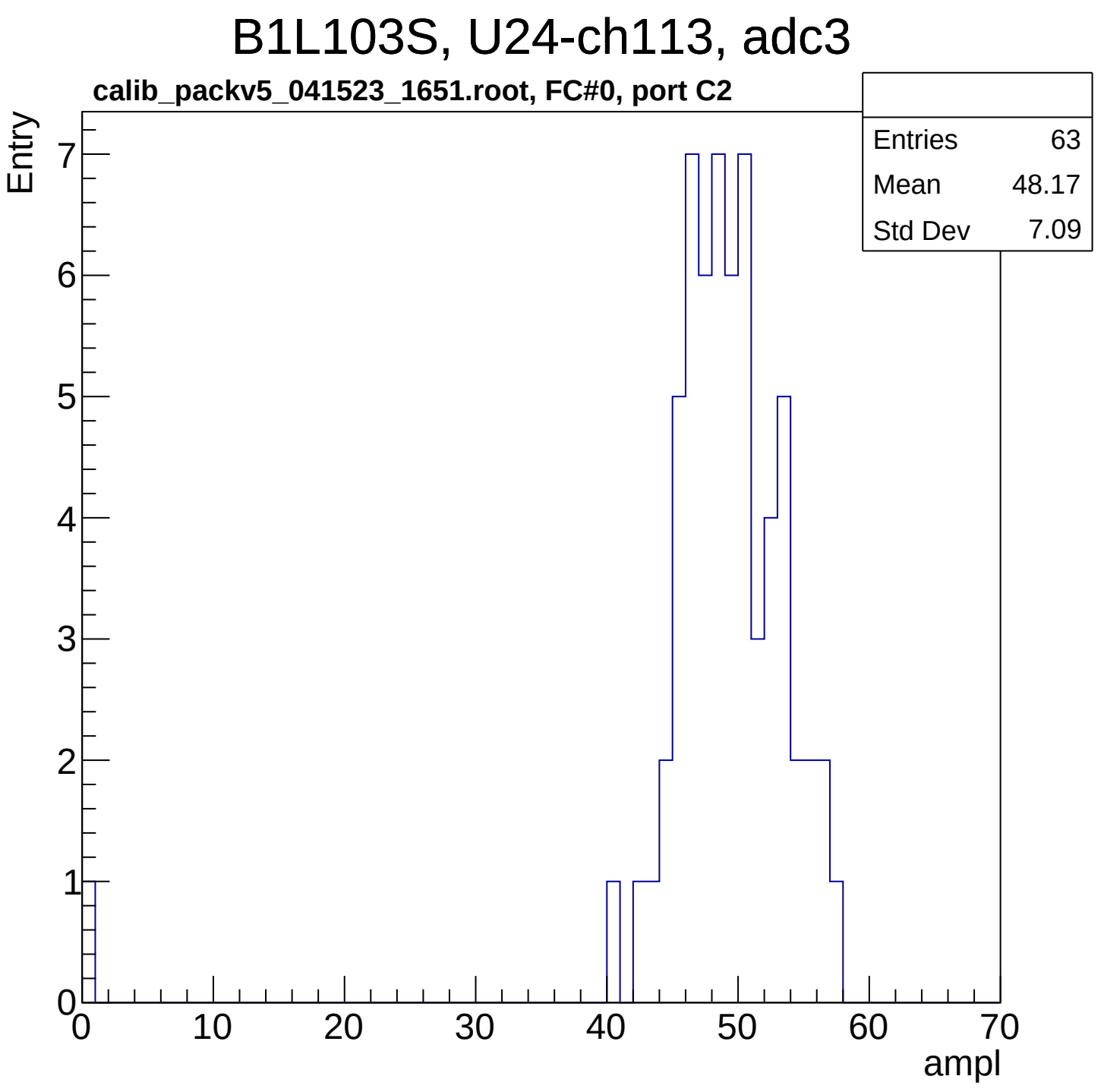
B1L103S, U24-ch113, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 48.17
Std Dev 7.09
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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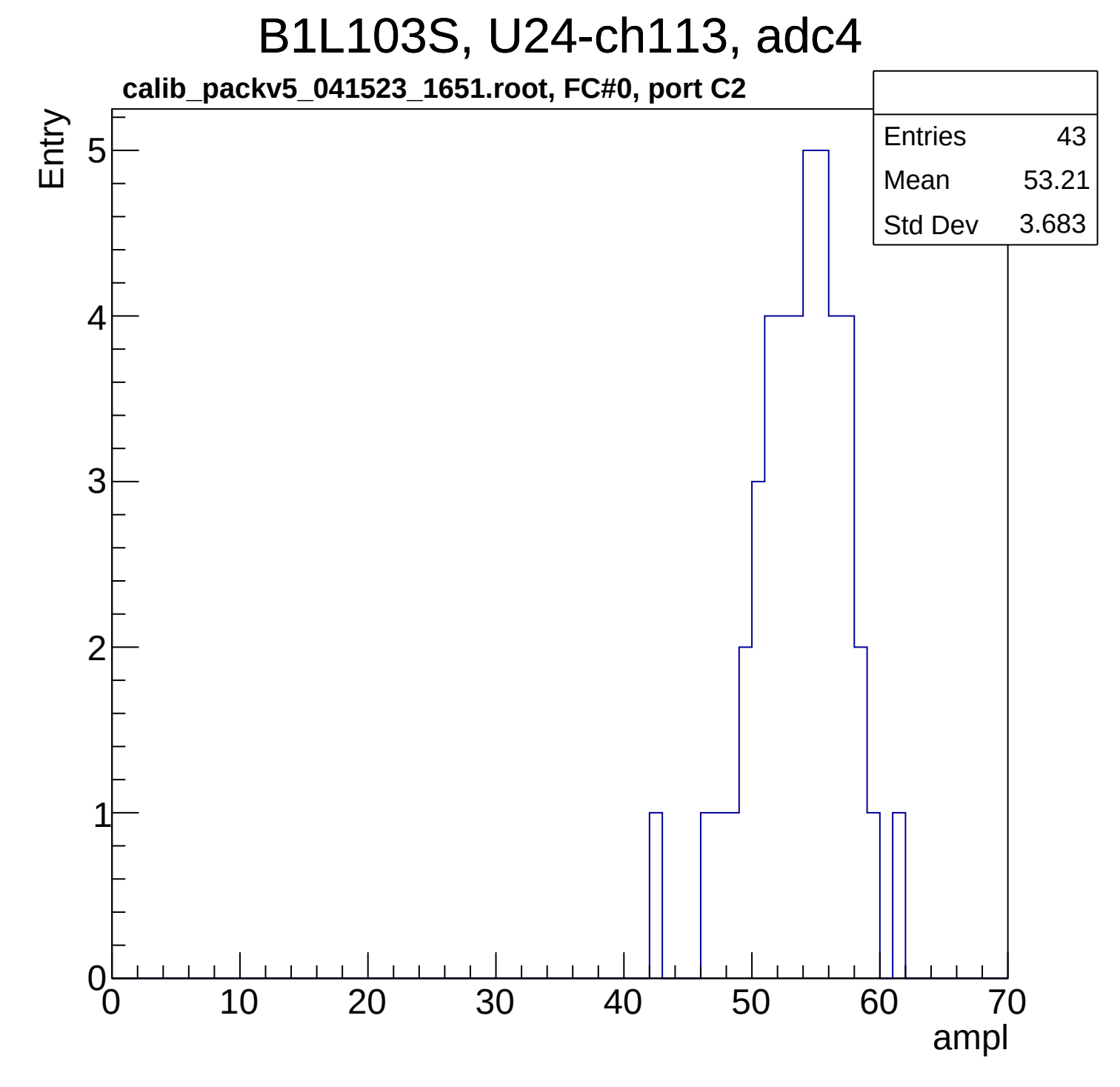
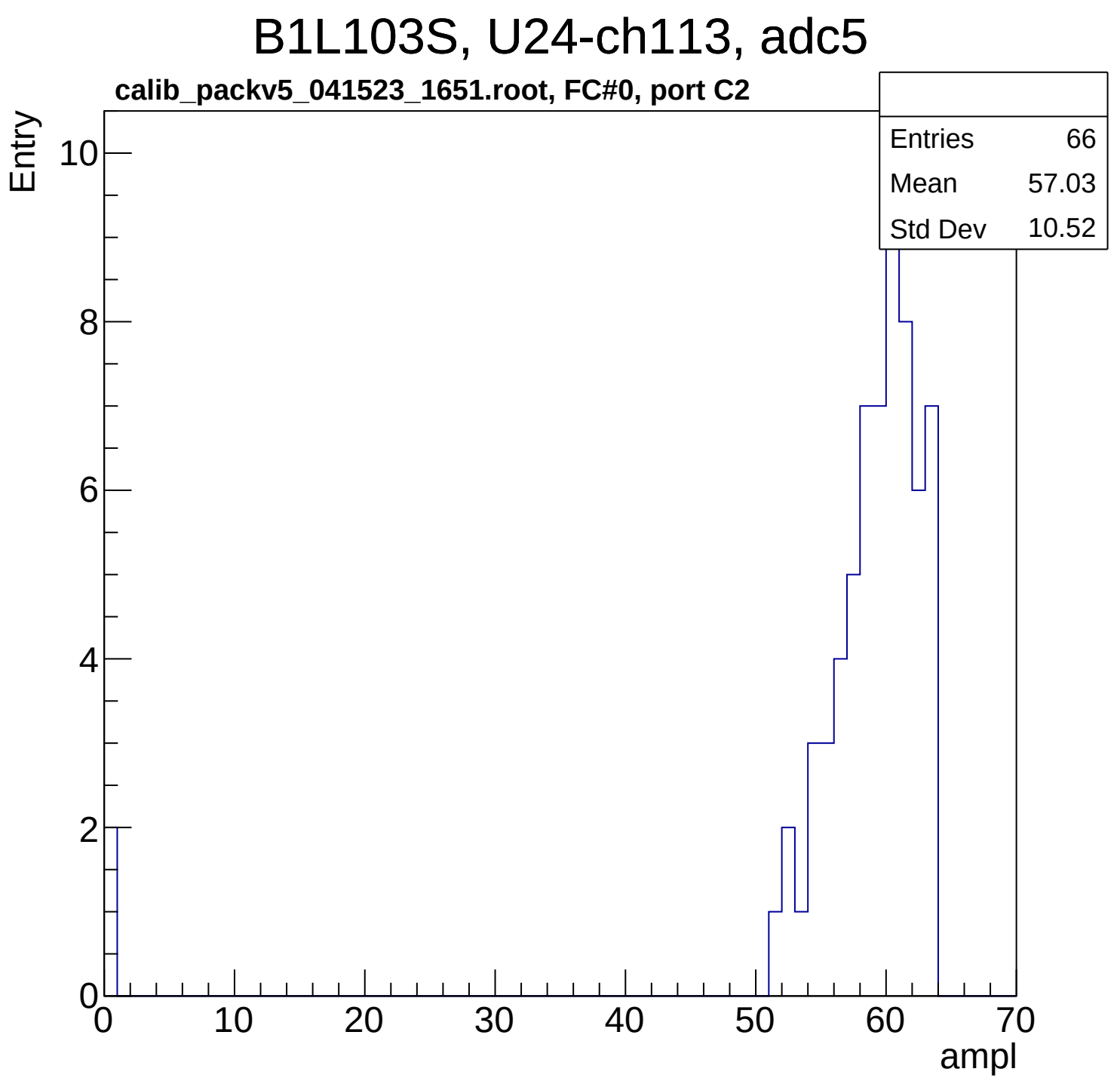
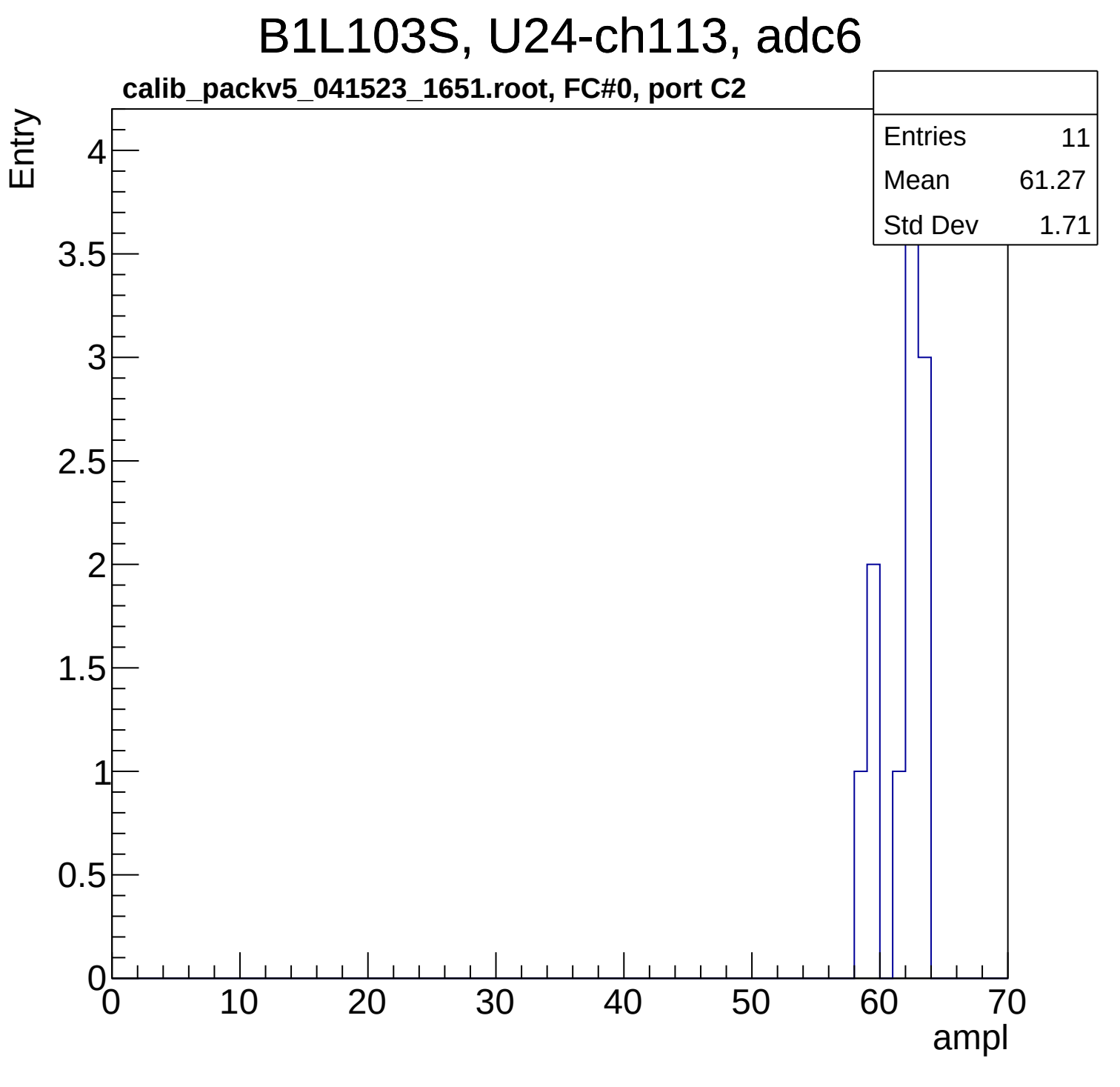

B1L103S, U24-ch113, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 43
Mean 53.21
Std Dev 3.683
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U24-ch113, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 57.03
Std Dev 10.52
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch113, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 61.27
Std Dev 1.71
Entry
ampl
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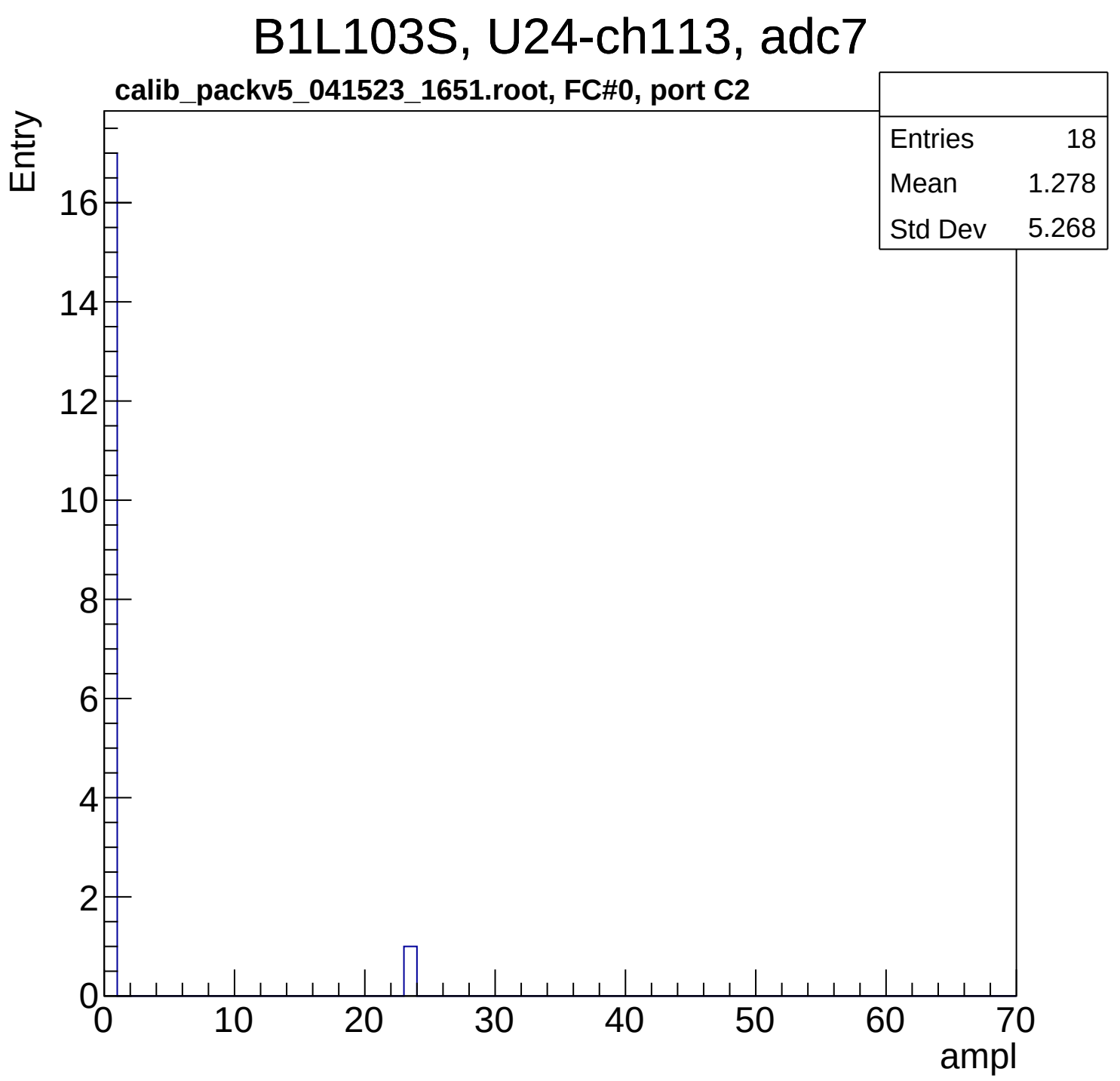
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U24-ch113, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 1.278
Std Dev 5.268
Entry
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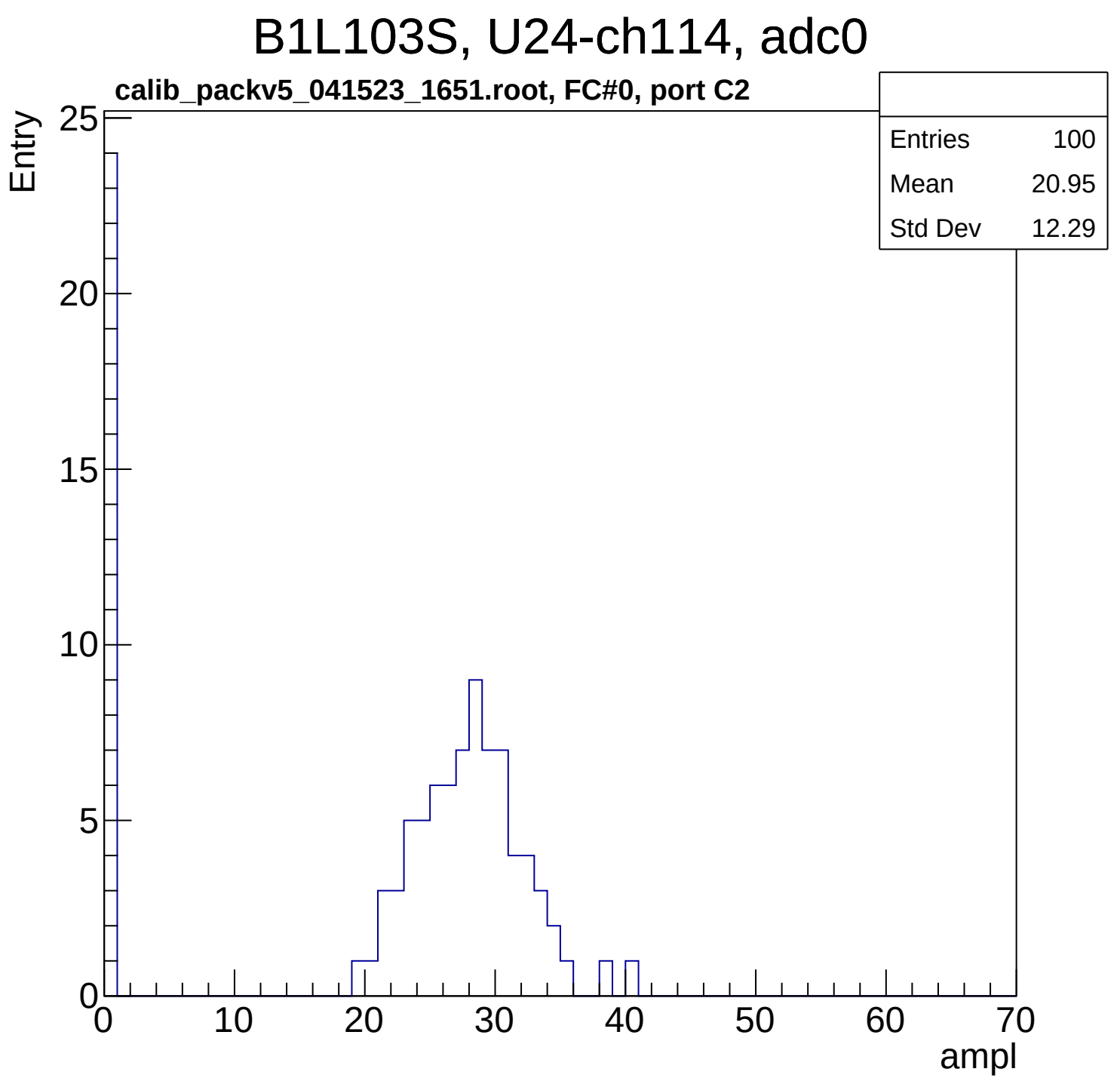
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch114, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 100
Mean 20.95
Std Dev 12.29
Entry
ampl
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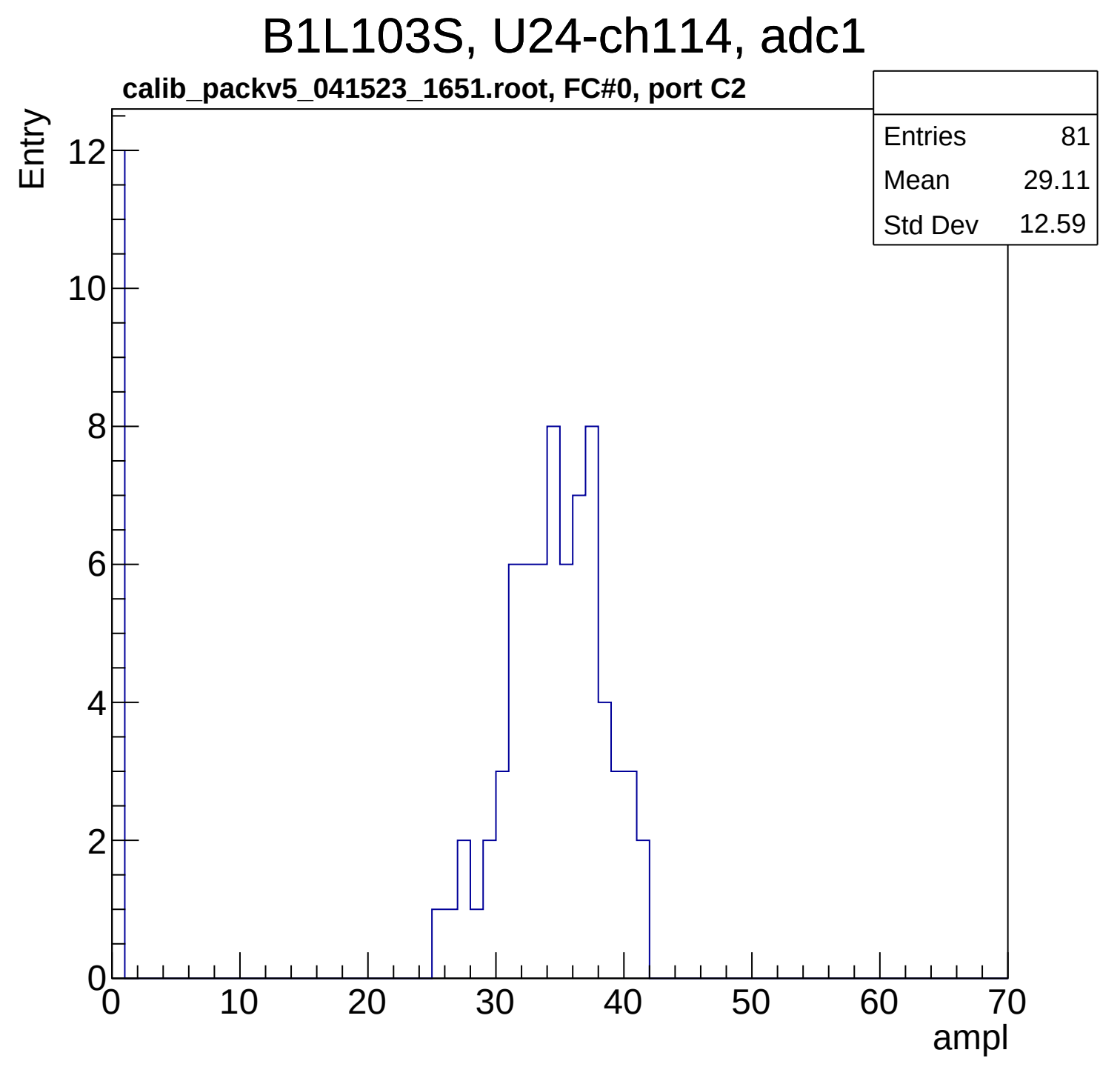
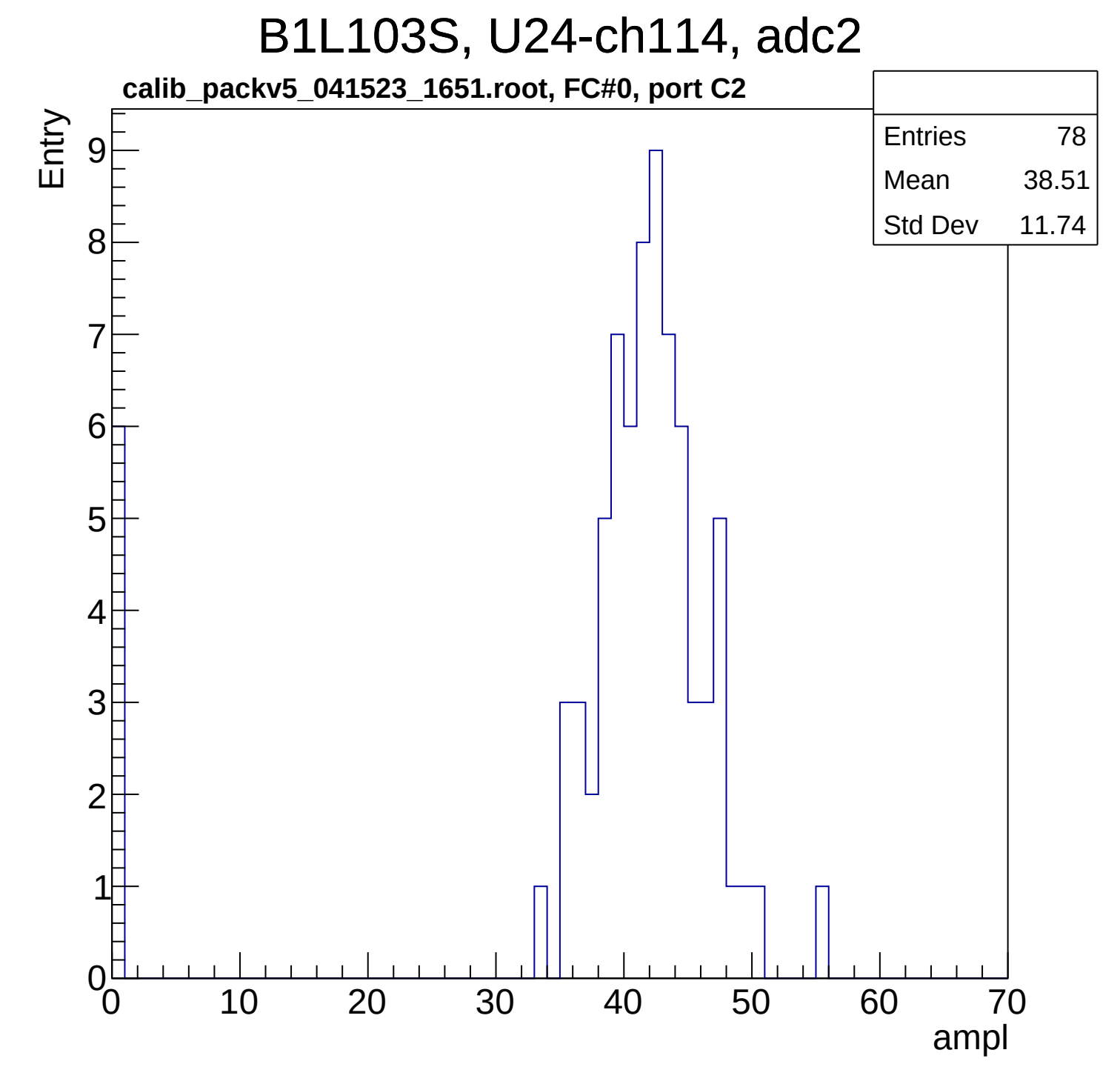
5
10
15
20
25
0
10
20
30
40
50
60
70


B1L103S, U24-ch114, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 29.11
Std Dev 12.59
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch114, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 38.51
Std Dev 11.74
Entry
ampl
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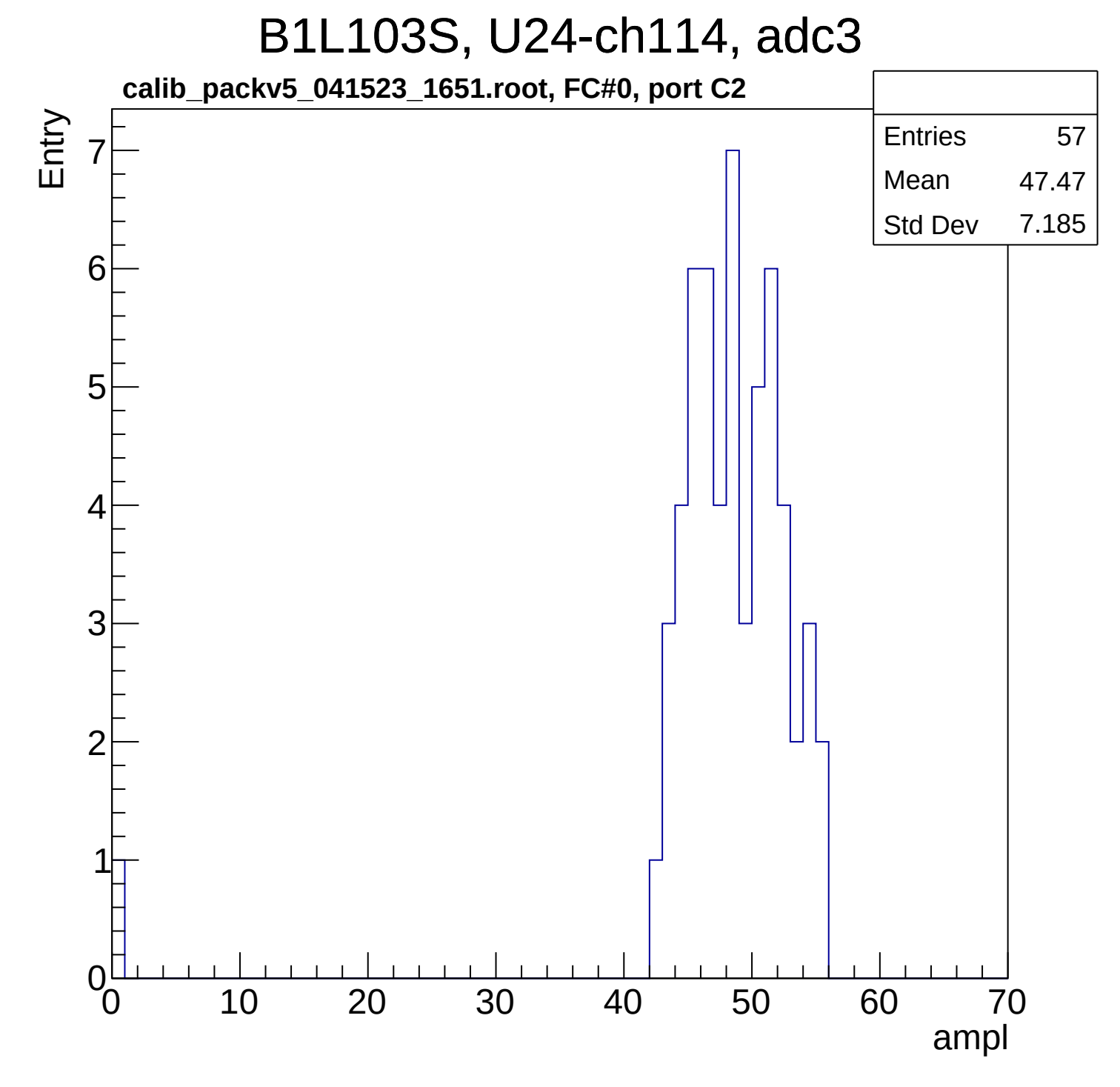
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U24-ch114, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 47.47
Std Dev 7.185
Entry
ampl
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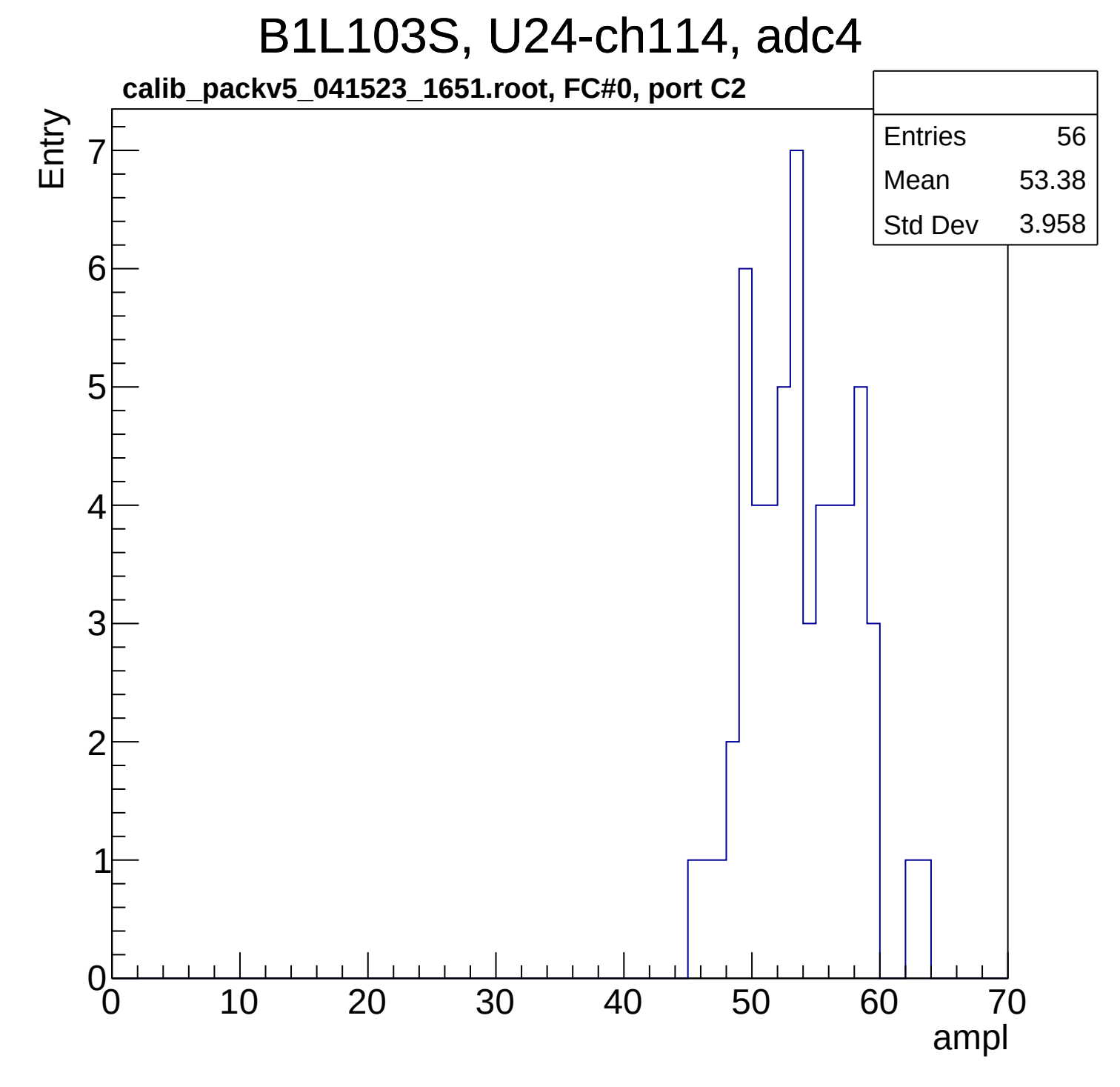
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U24-ch114, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 53.38
Std Dev 3.958
Entry
ampl
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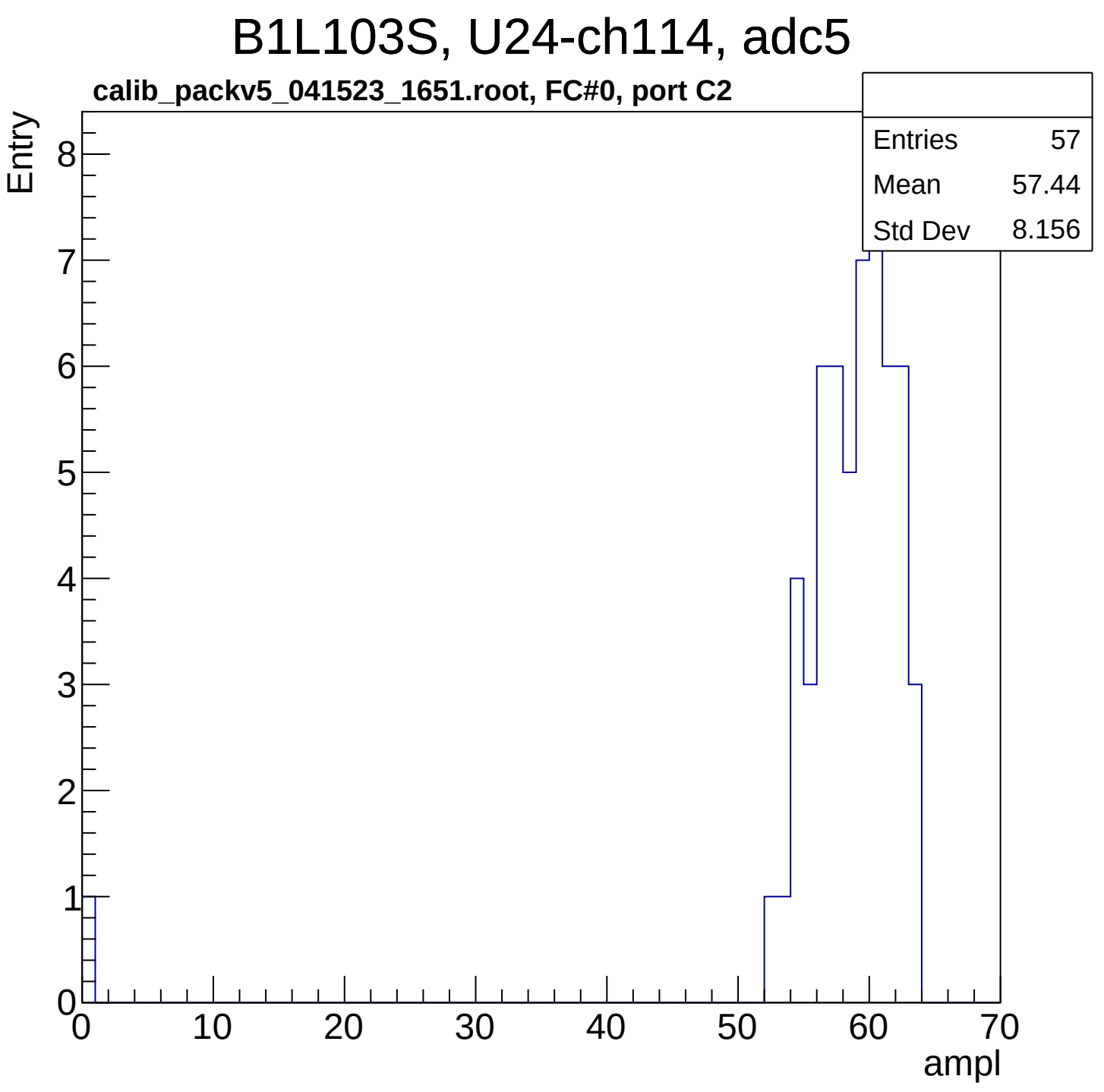
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U24-ch114, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 57.44
Std Dev 8.156
Entry
ampl
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2
3
4
5
6
7
8
0
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20
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60
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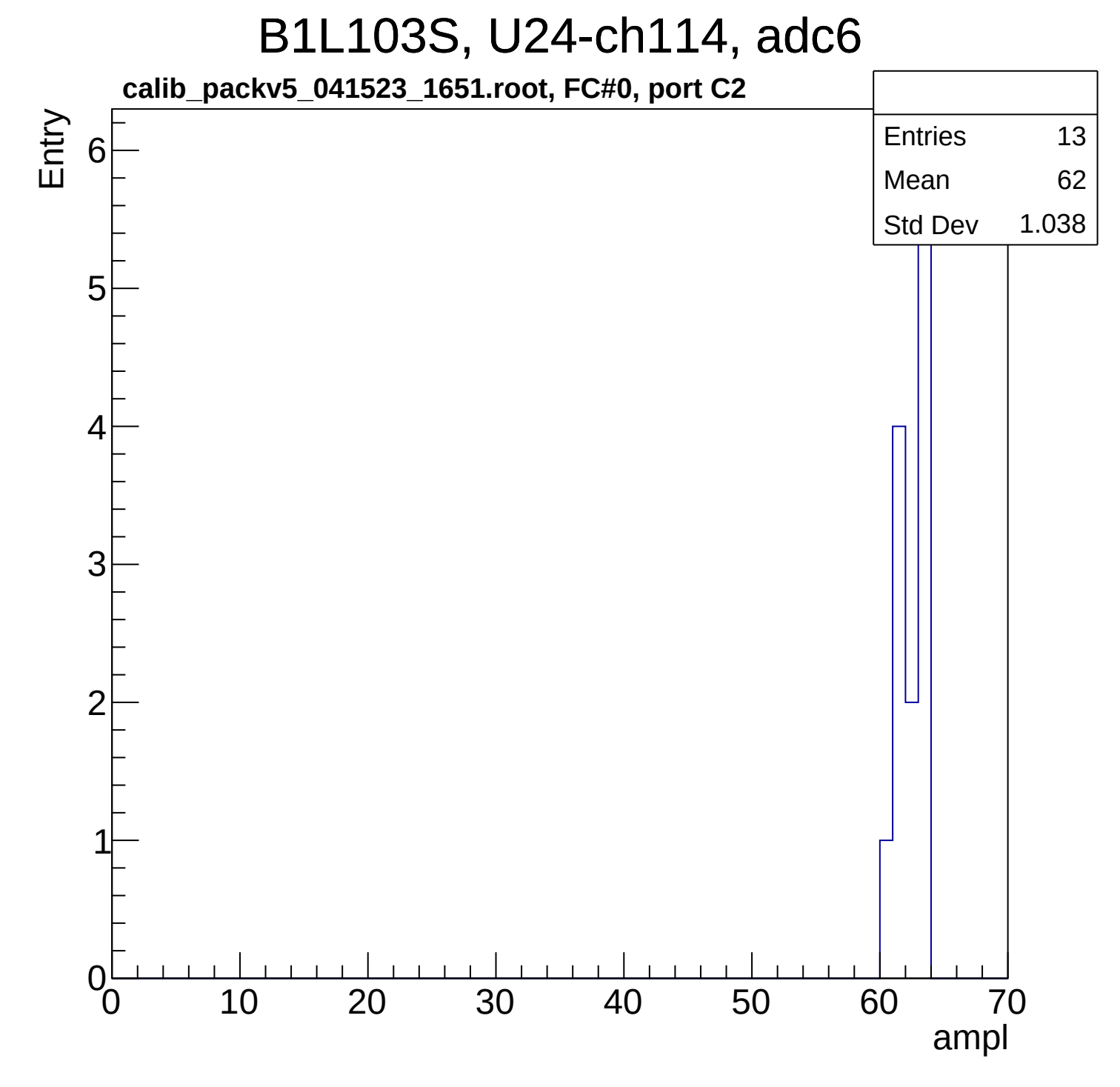
B1L103S, U24-ch114, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 13
Mean 62
Std Dev 1.038
Entry
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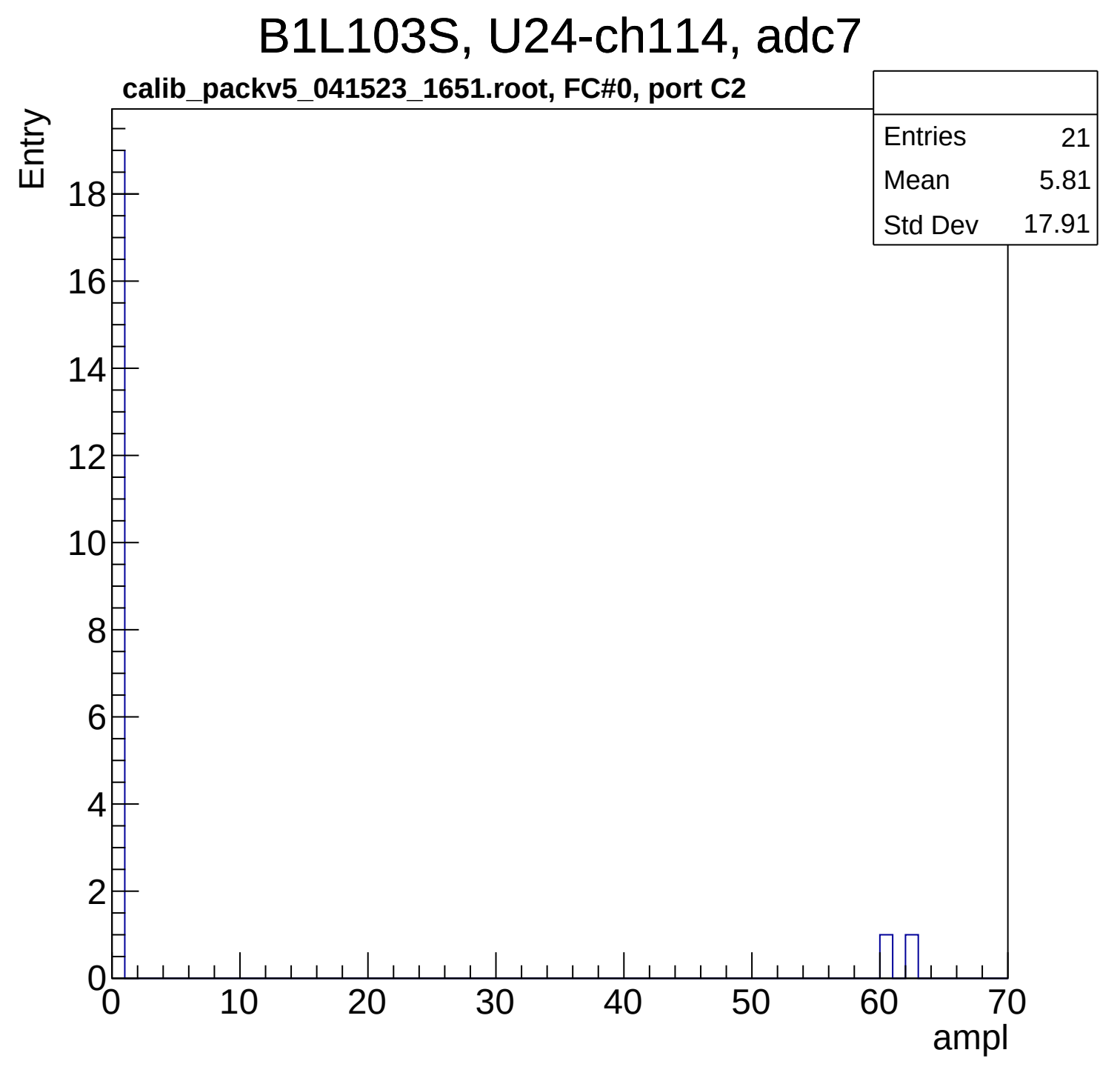
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch114, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 5.81
Std Dev 17.91
Entry
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6
8
10
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14
16
18
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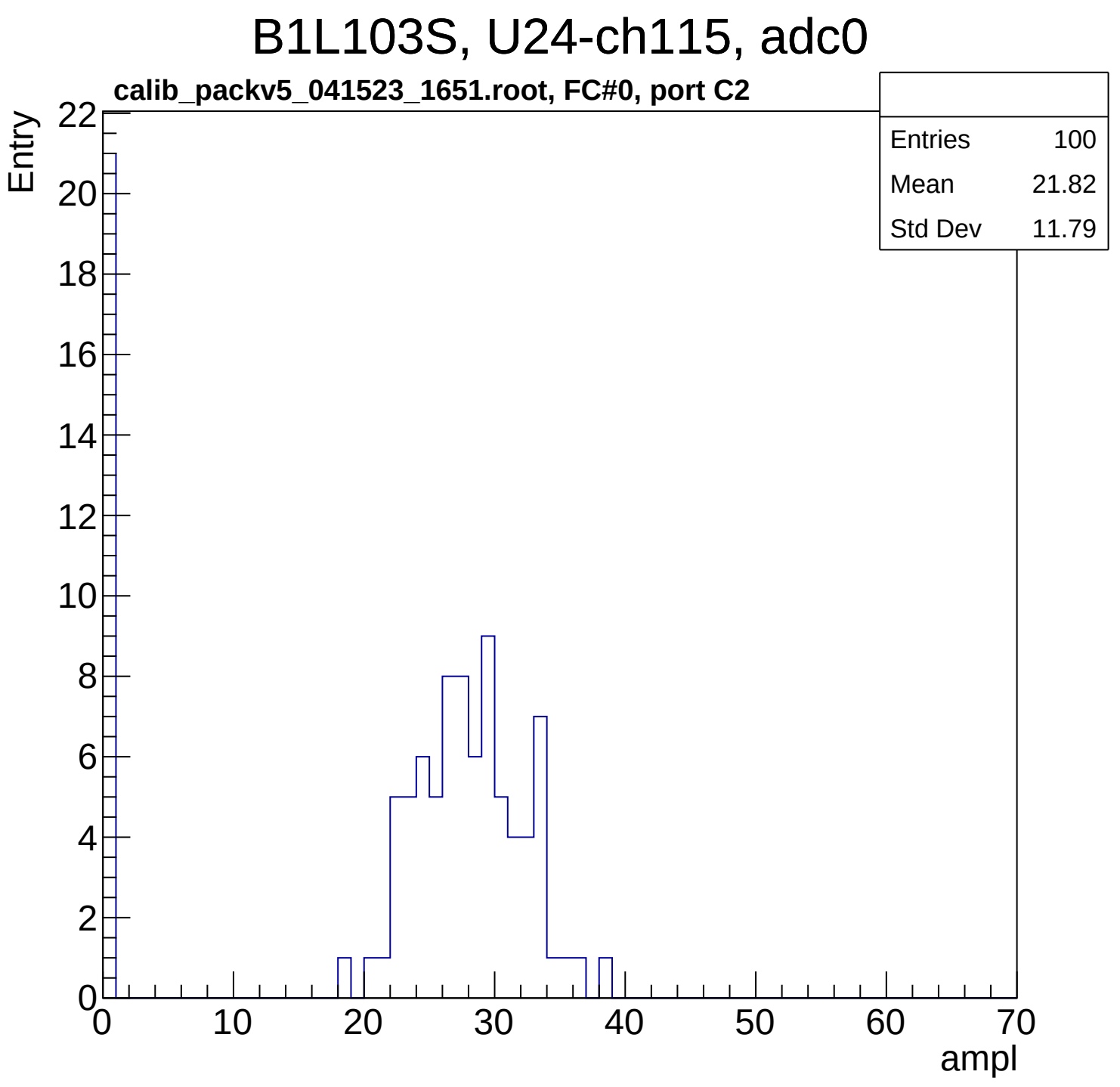
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch115, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 100
Mean 21.82
Std Dev 11.79
Entry
ampl
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8
10
12
14
16
18
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22
0
10
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40
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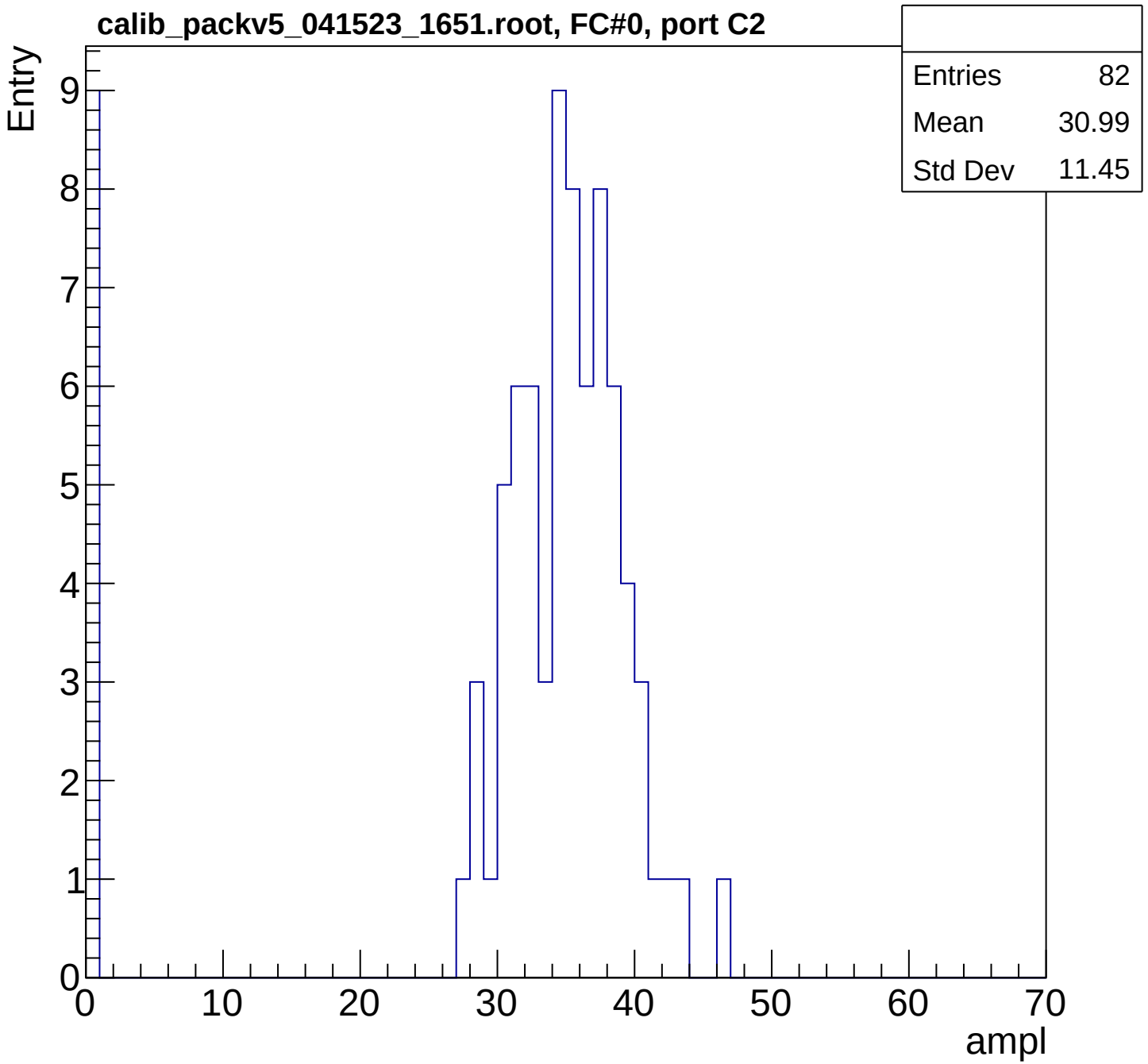
60
70


B1L103S, U24-ch115, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 30.99
Std Dev 11.45
Entry
ampl
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2
3
4
5
6
7
8
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0
10
20
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60
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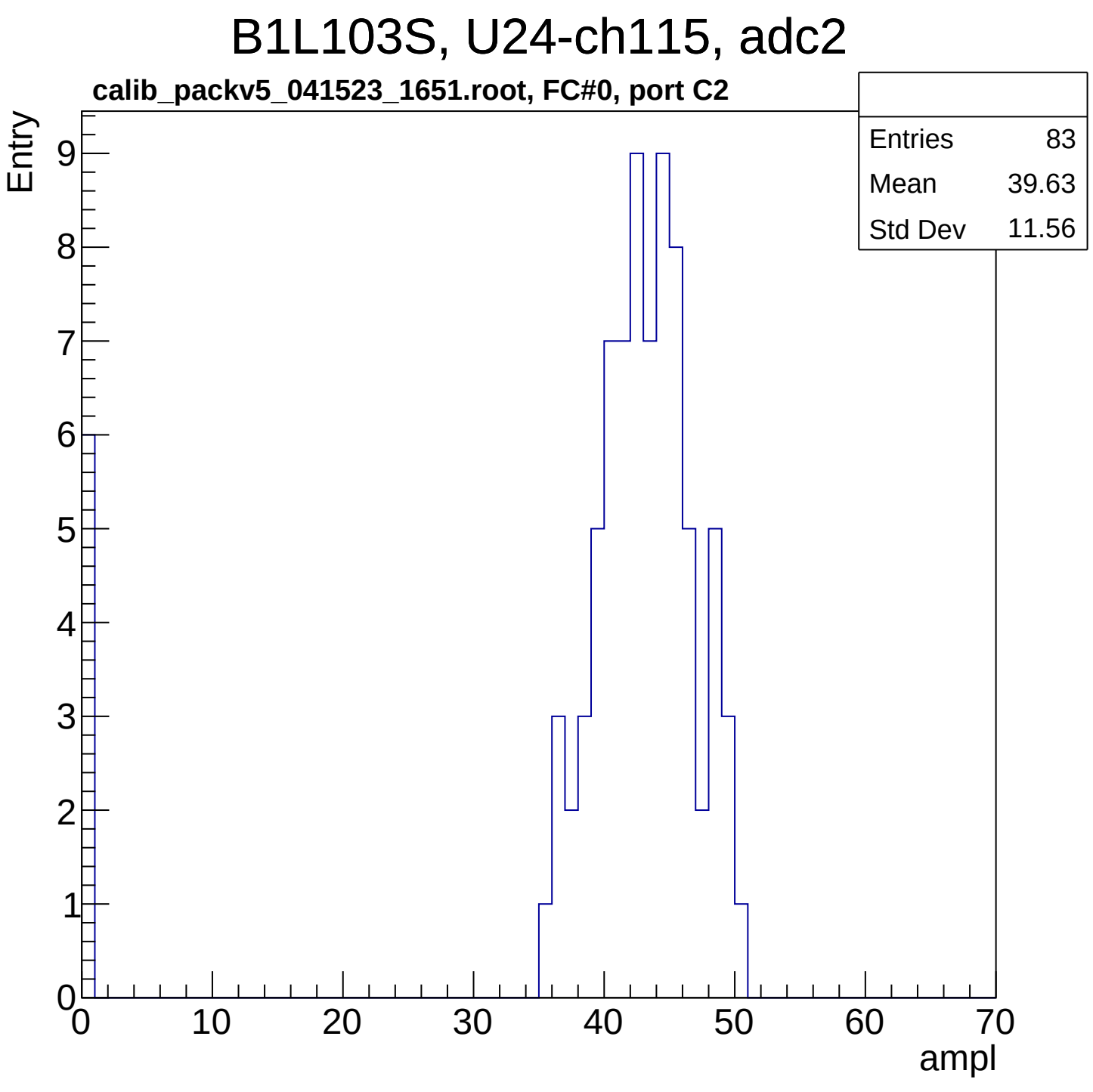
B1L103S, U24-ch115, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 39.63
Std Dev 11.56
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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40
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60
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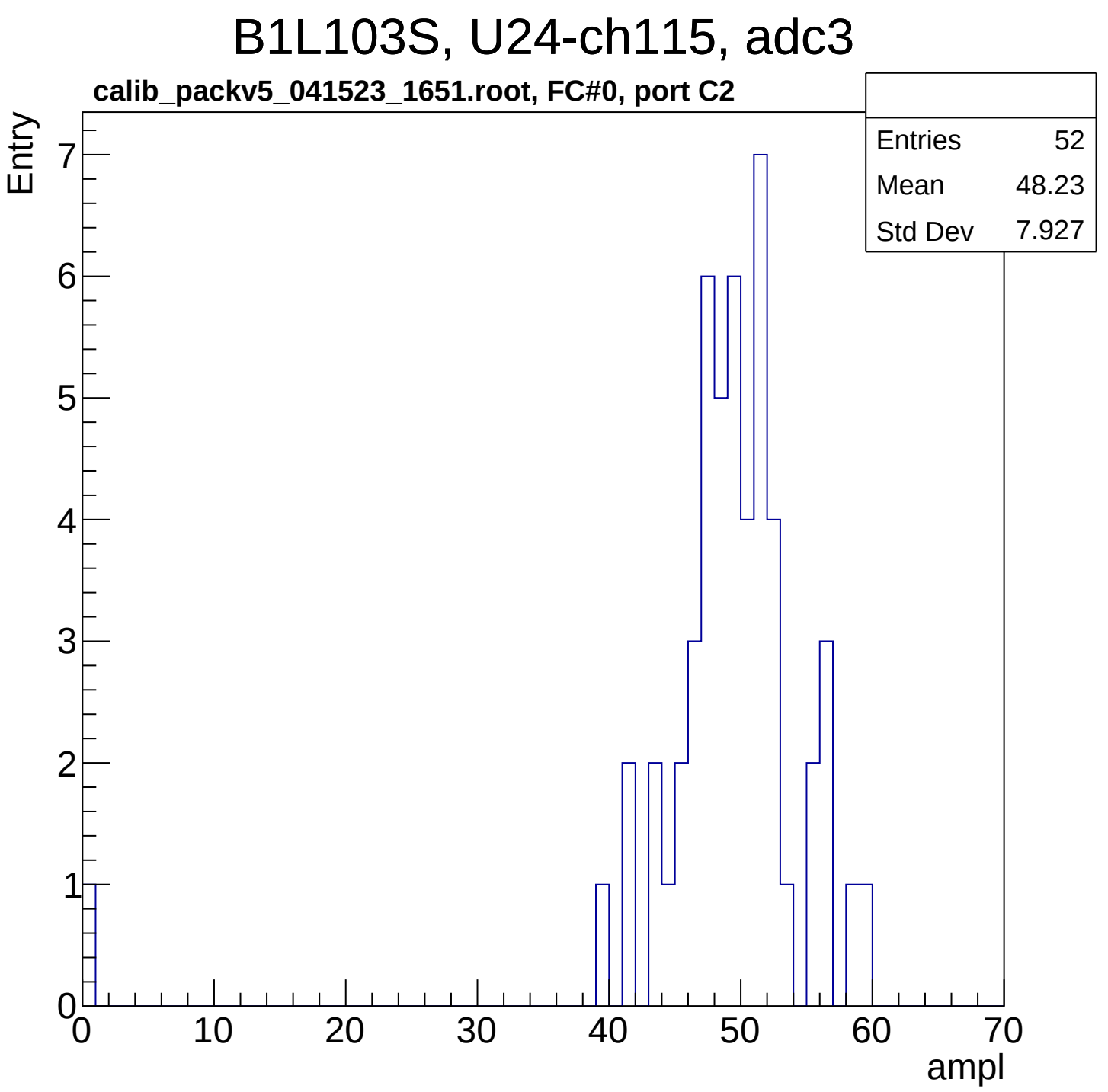
B1L103S, U24-ch115, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 48.23
Std Dev 7.927
Entry
ampl
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3
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6
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0
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60
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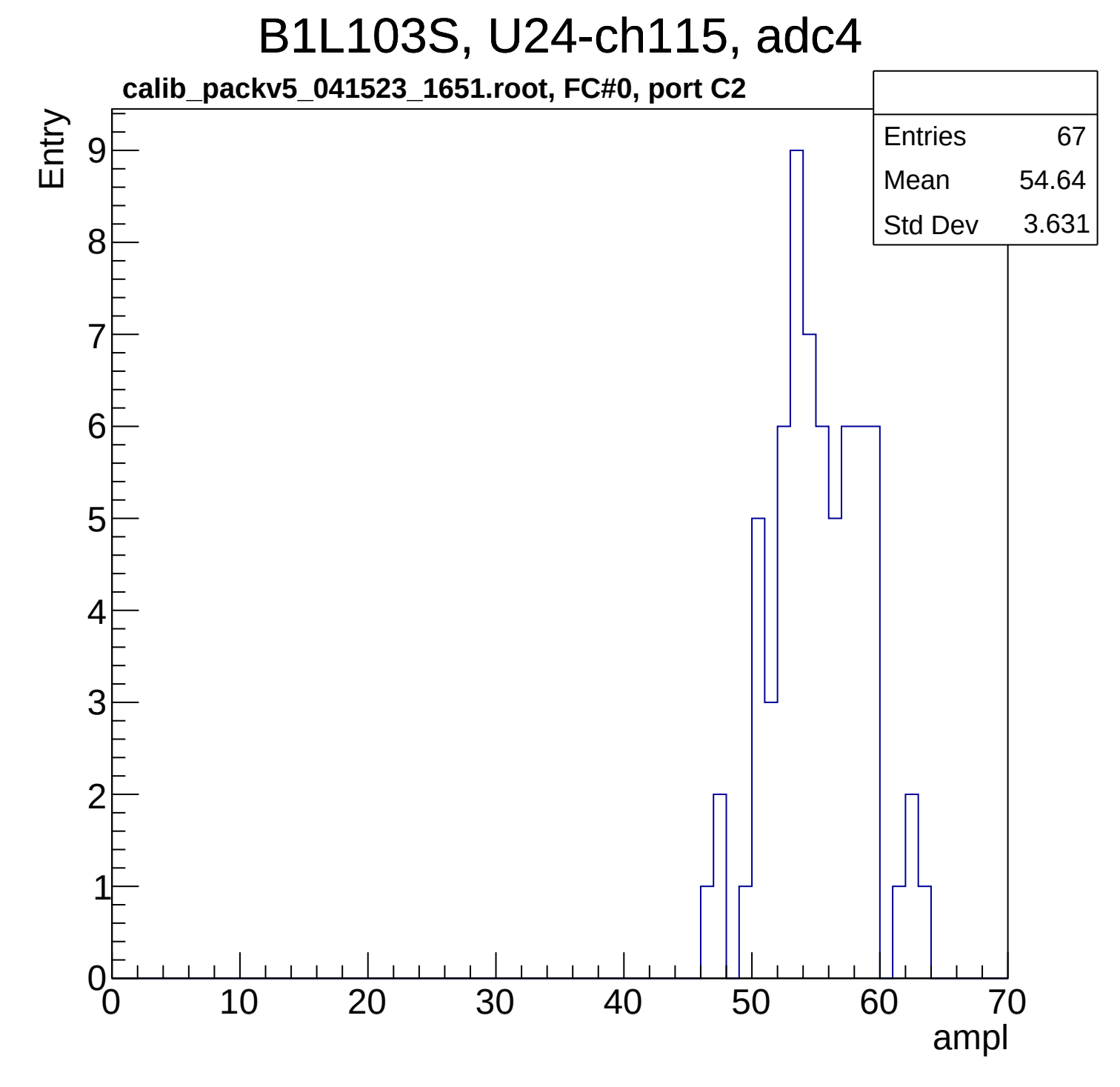
B1L103S, U24-ch115, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 54.64
Std Dev 3.631
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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60
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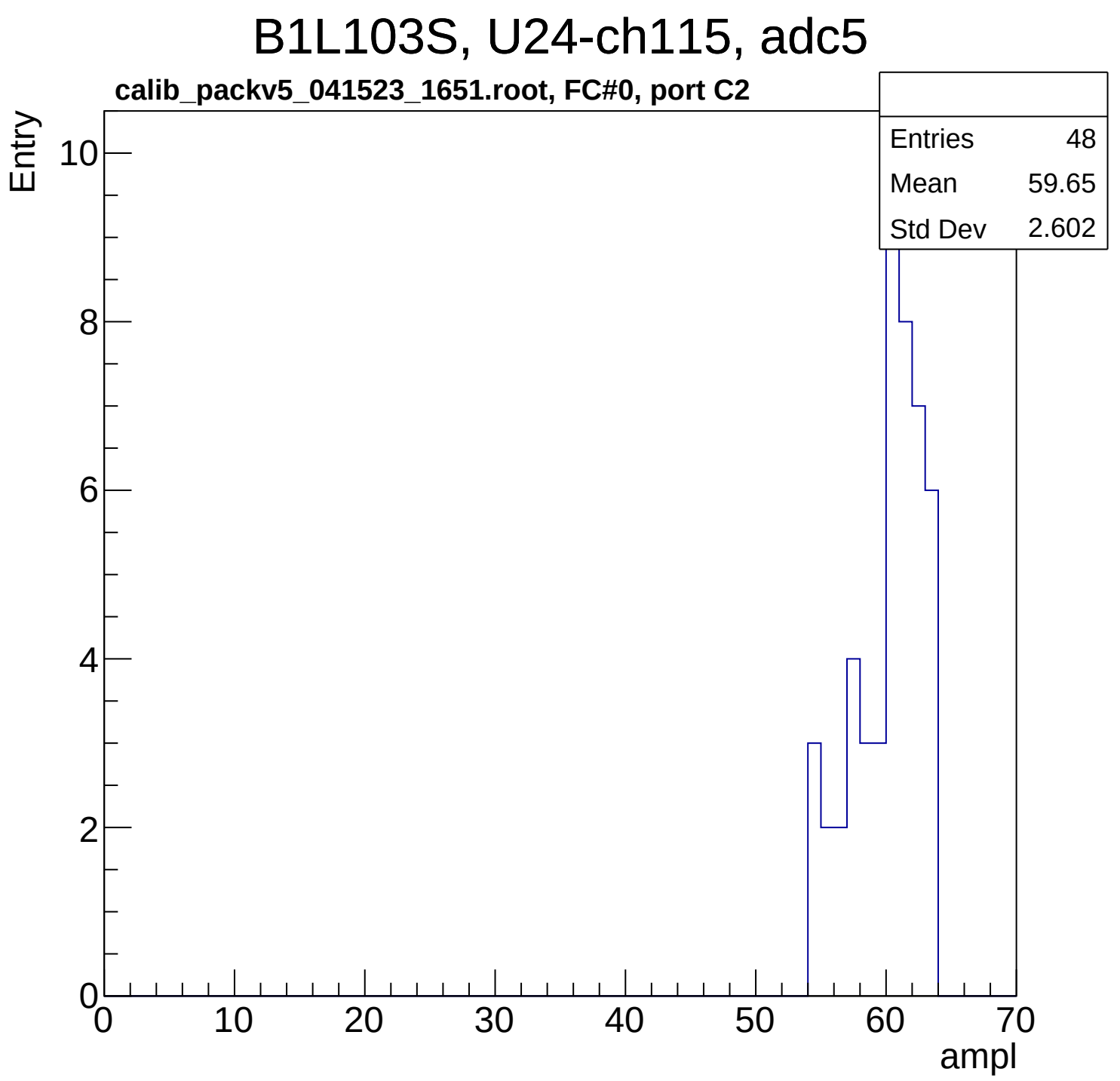
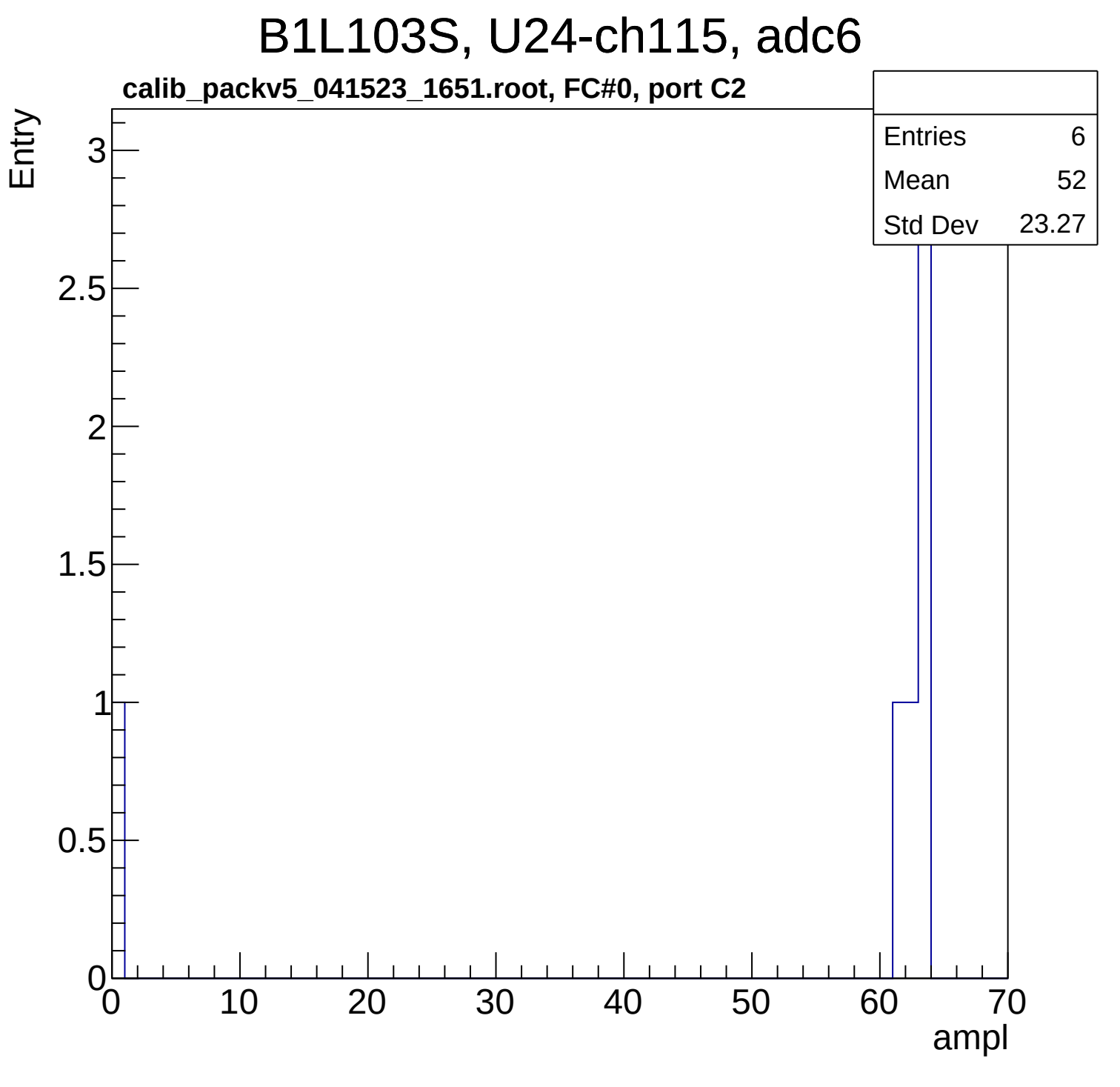

B1L103S, U24-ch115, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 59.65
Std Dev 2.602
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U24-ch115, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 52
Std Dev 23.27
Entry
ampl
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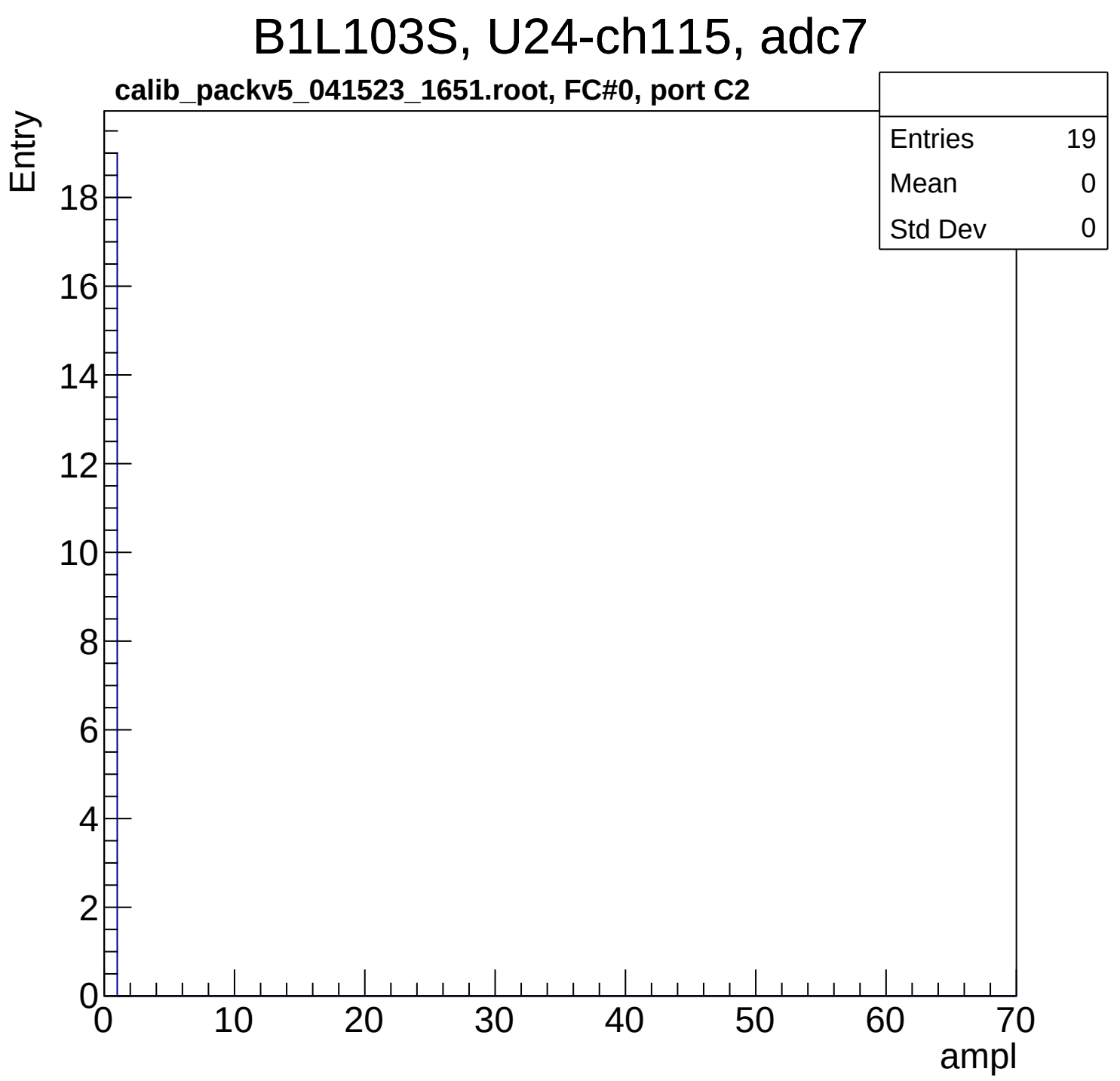
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U24-ch115, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
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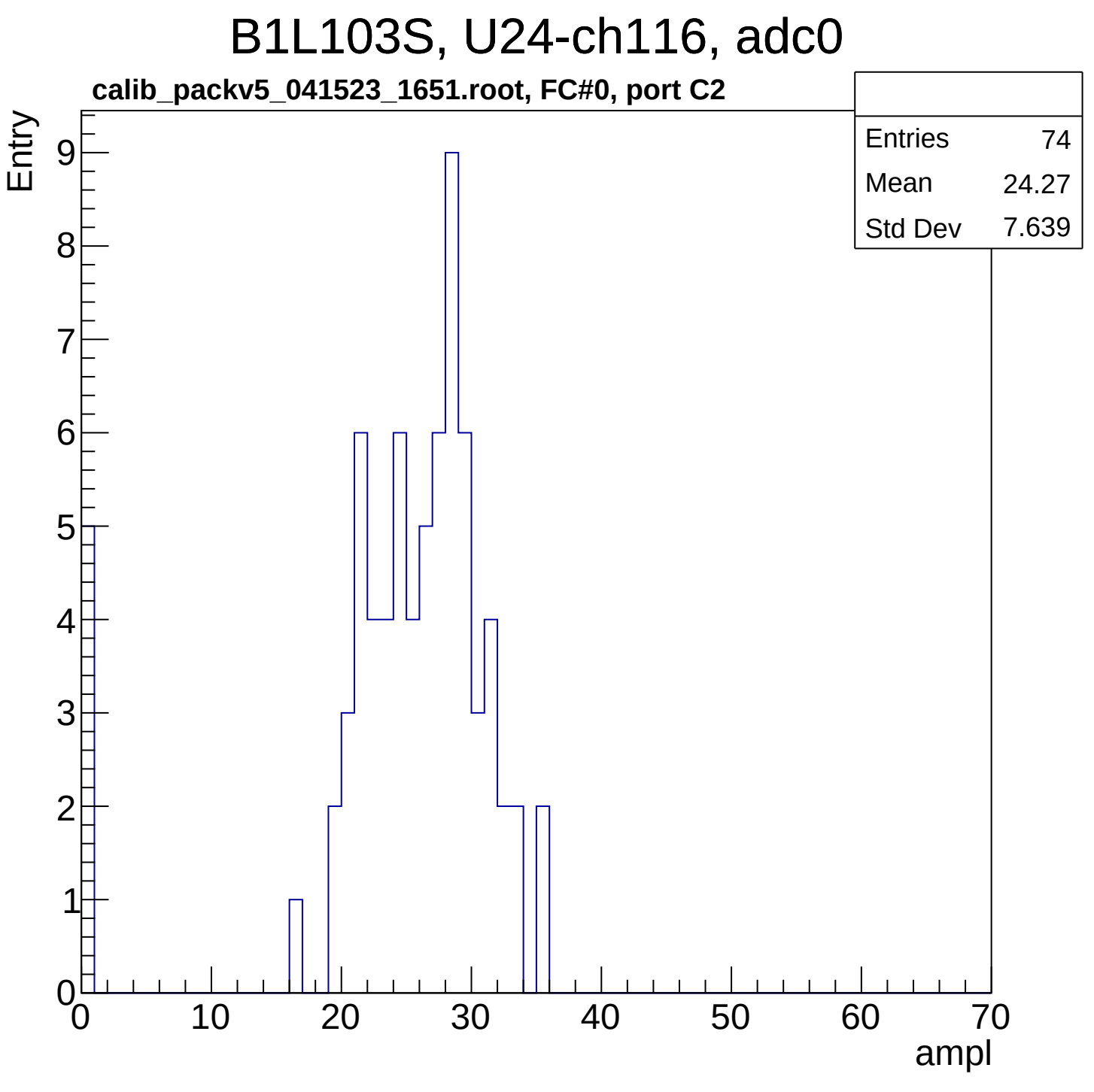
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch116, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 24.27
Std Dev 7.639
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
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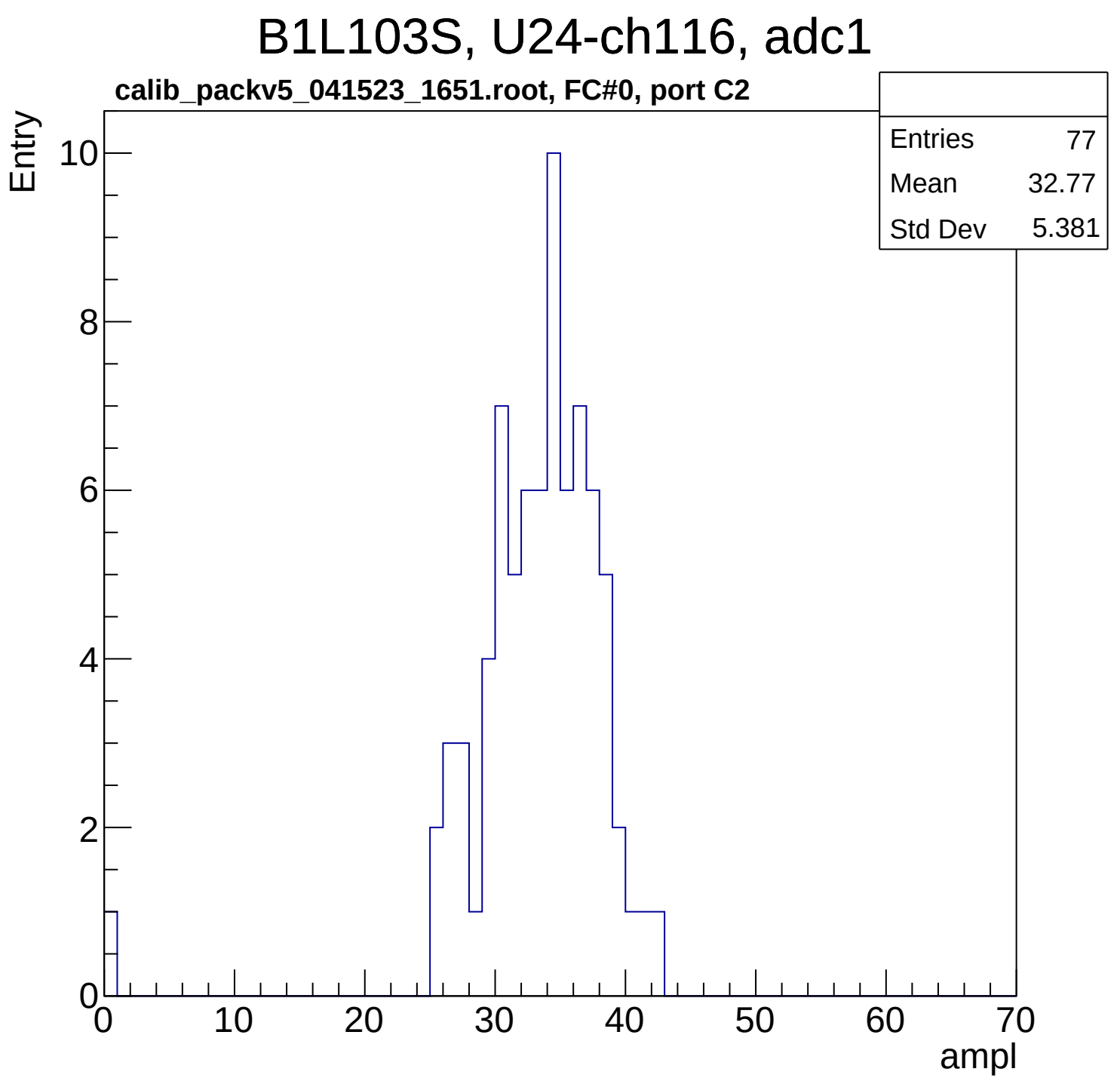
60
70


B1L103S, U24-ch116, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 32.77
Std Dev 5.381
Entry
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4
6
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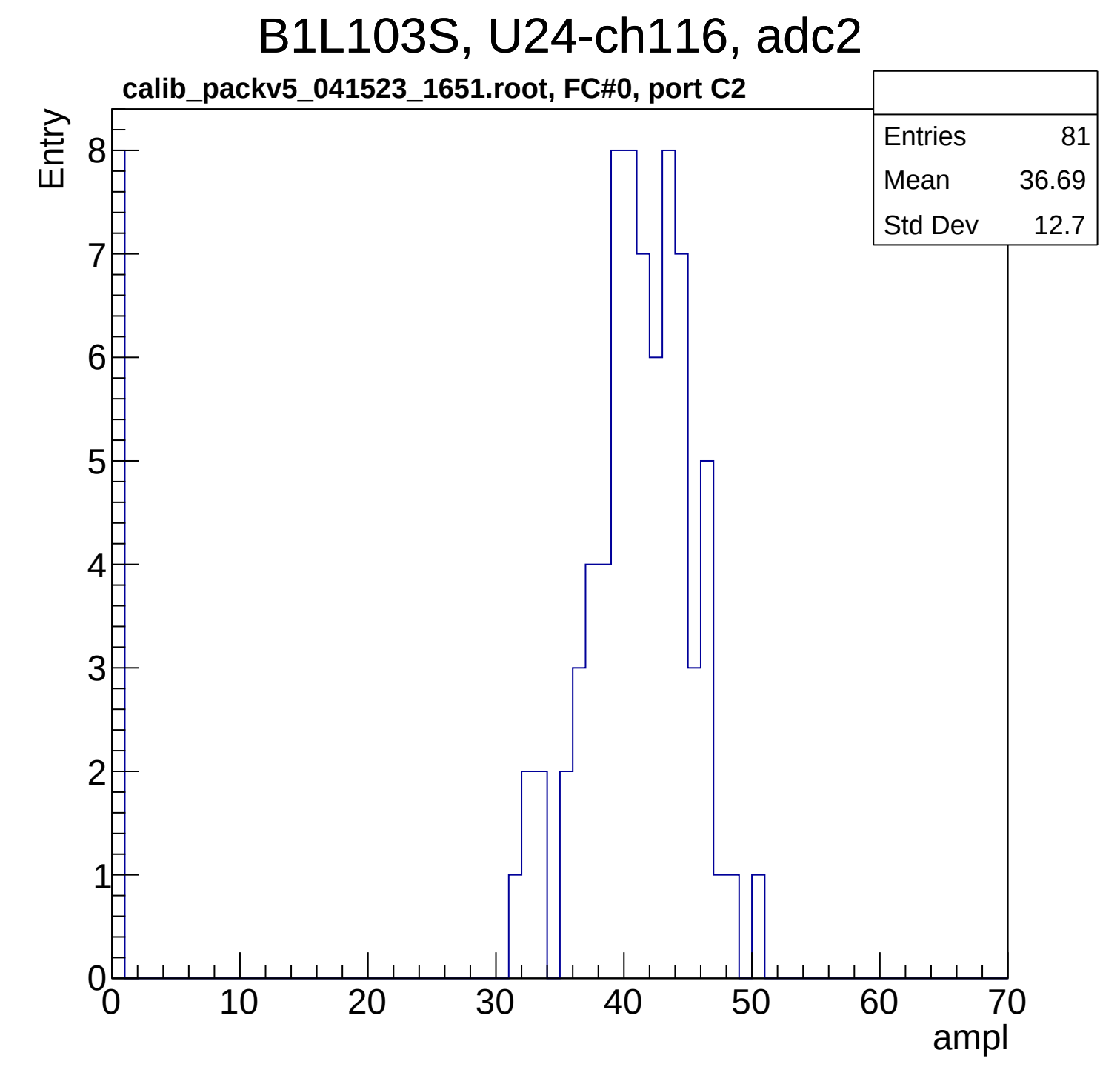
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch116, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 36.69
Std Dev 12.7
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
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60
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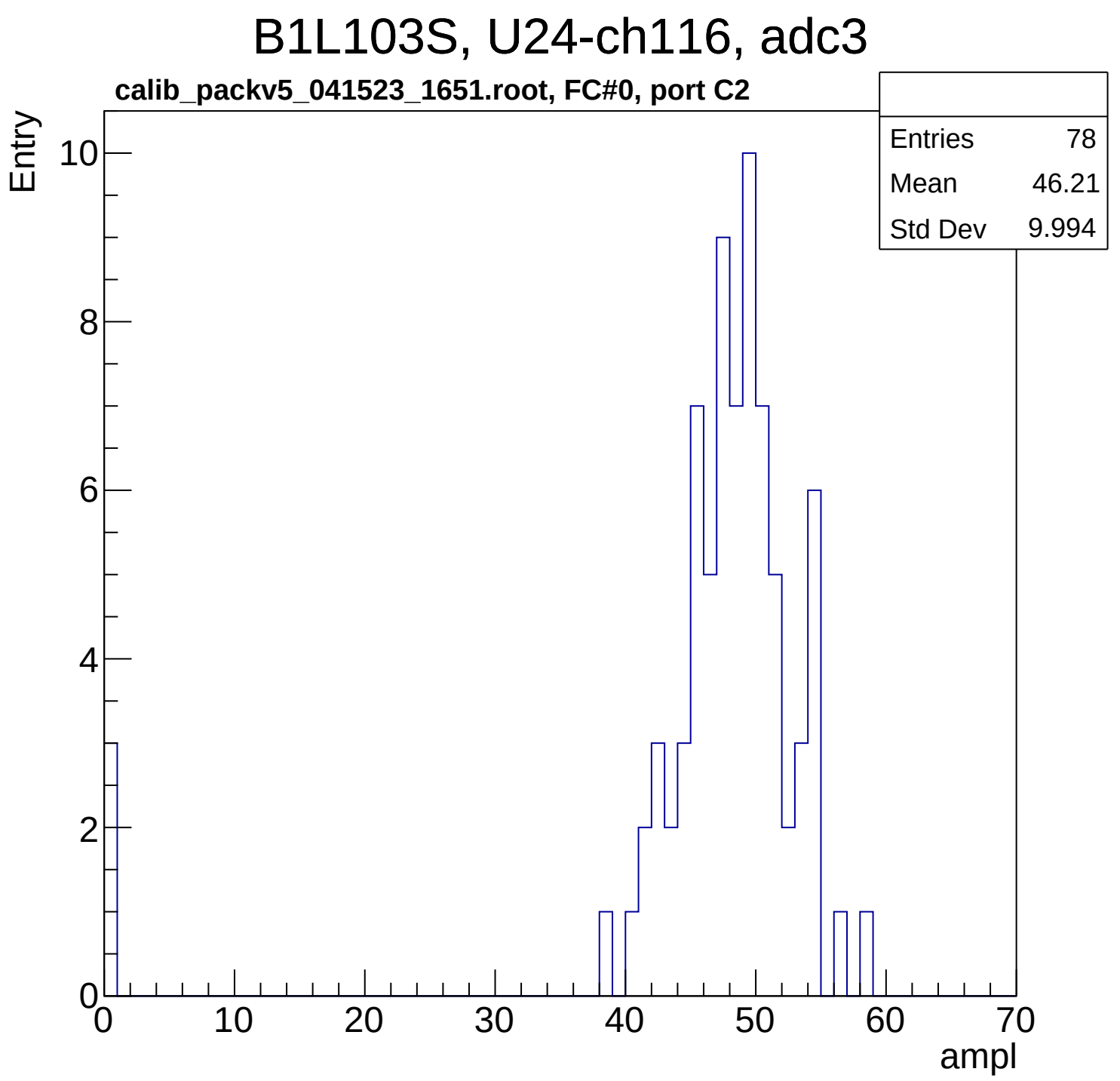
B1L103S, U24-ch116, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 46.21
Std Dev 9.994
Entry
ampl
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40
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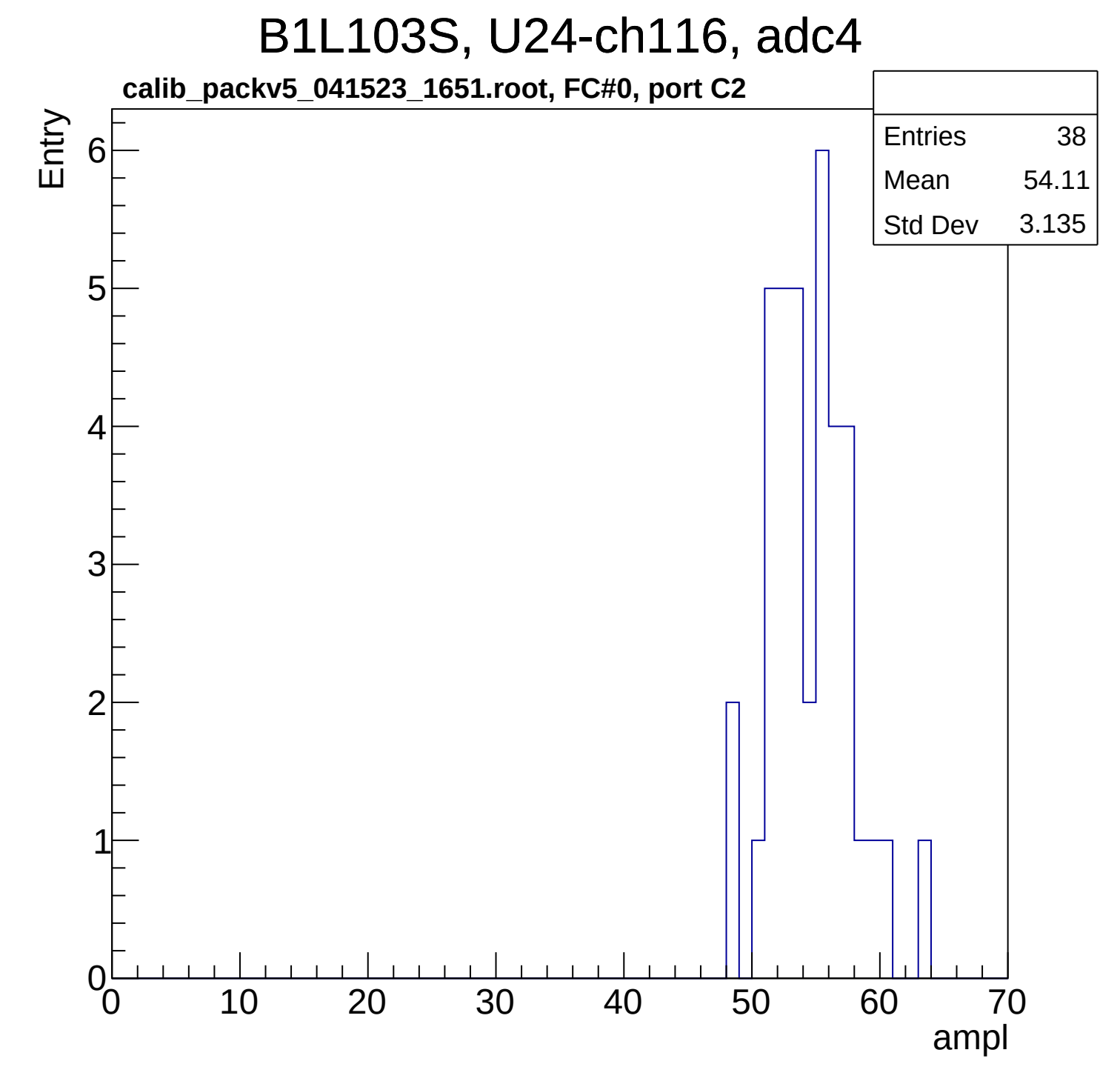
B1L103S, U24-ch116, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 38
Mean 54.11
Std Dev 3.135
Entry
ampl
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2
3
4
5
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0
10
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40
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60
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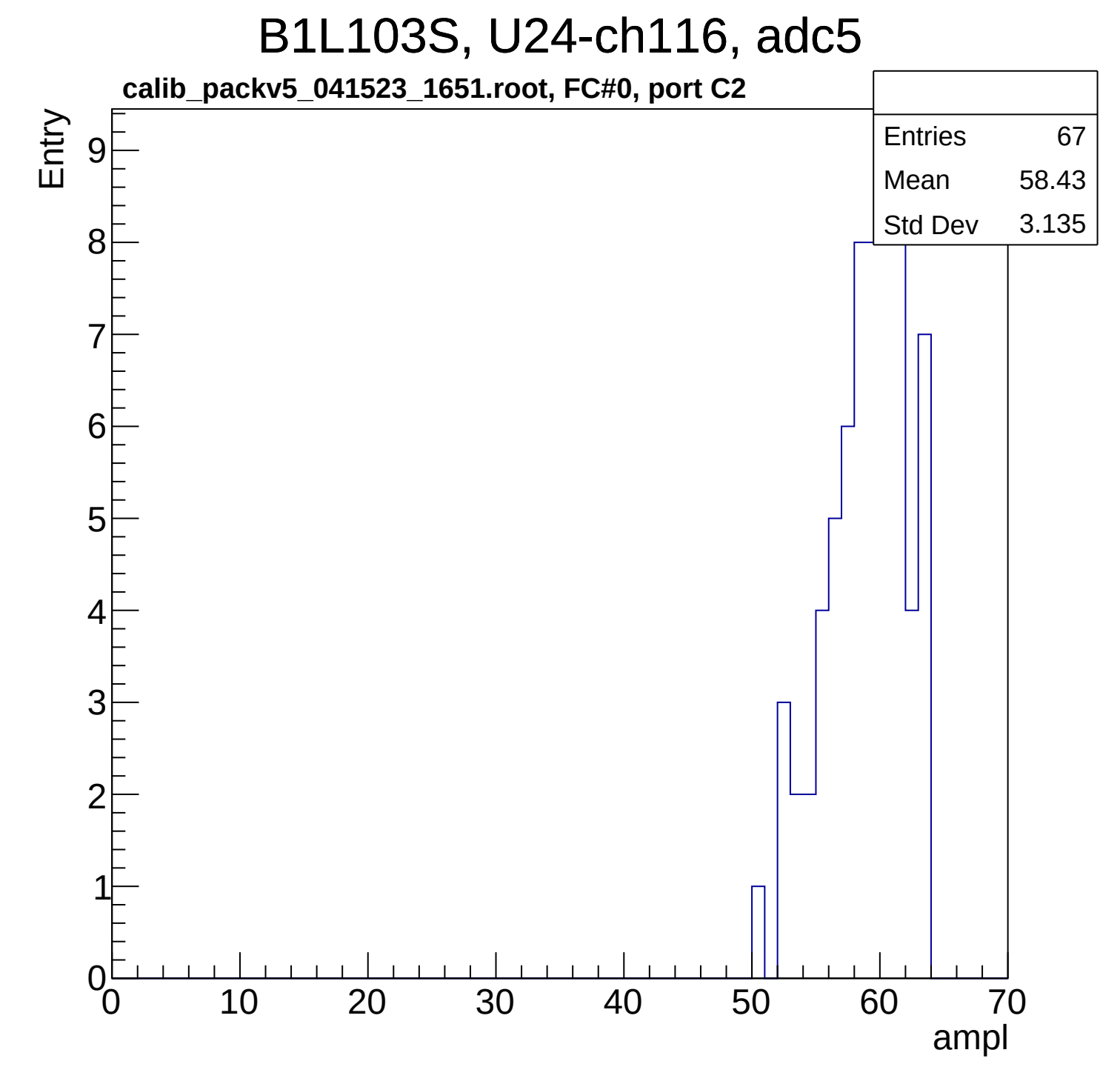
B1L103S, U24-ch116, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 58.43
Std Dev 3.135
Entry
ampl
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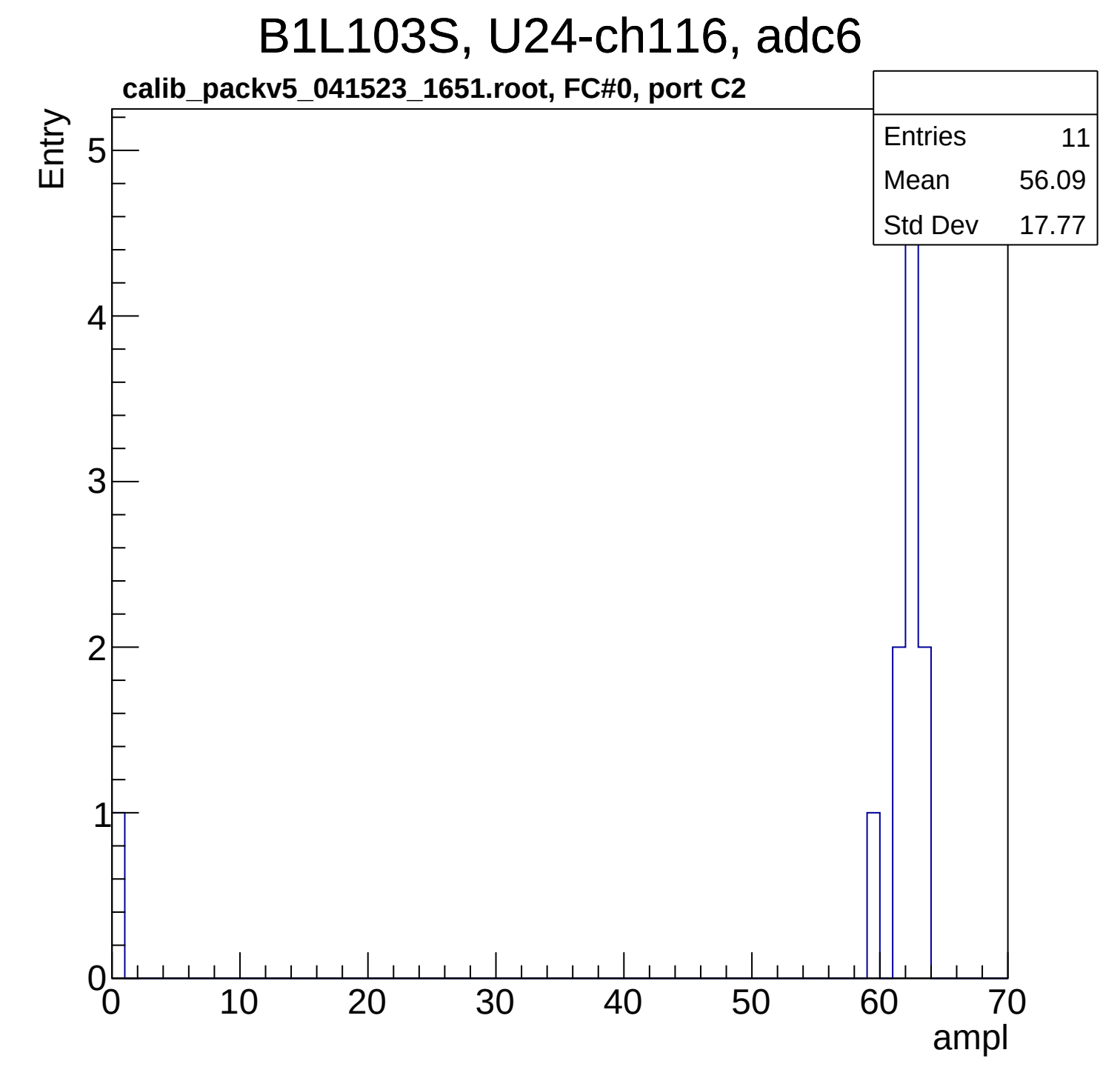
B1L103S, U24-ch116, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 56.09
Std Dev 17.77
Entry
ampl
0
1
2
3
4
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0
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40
50
60
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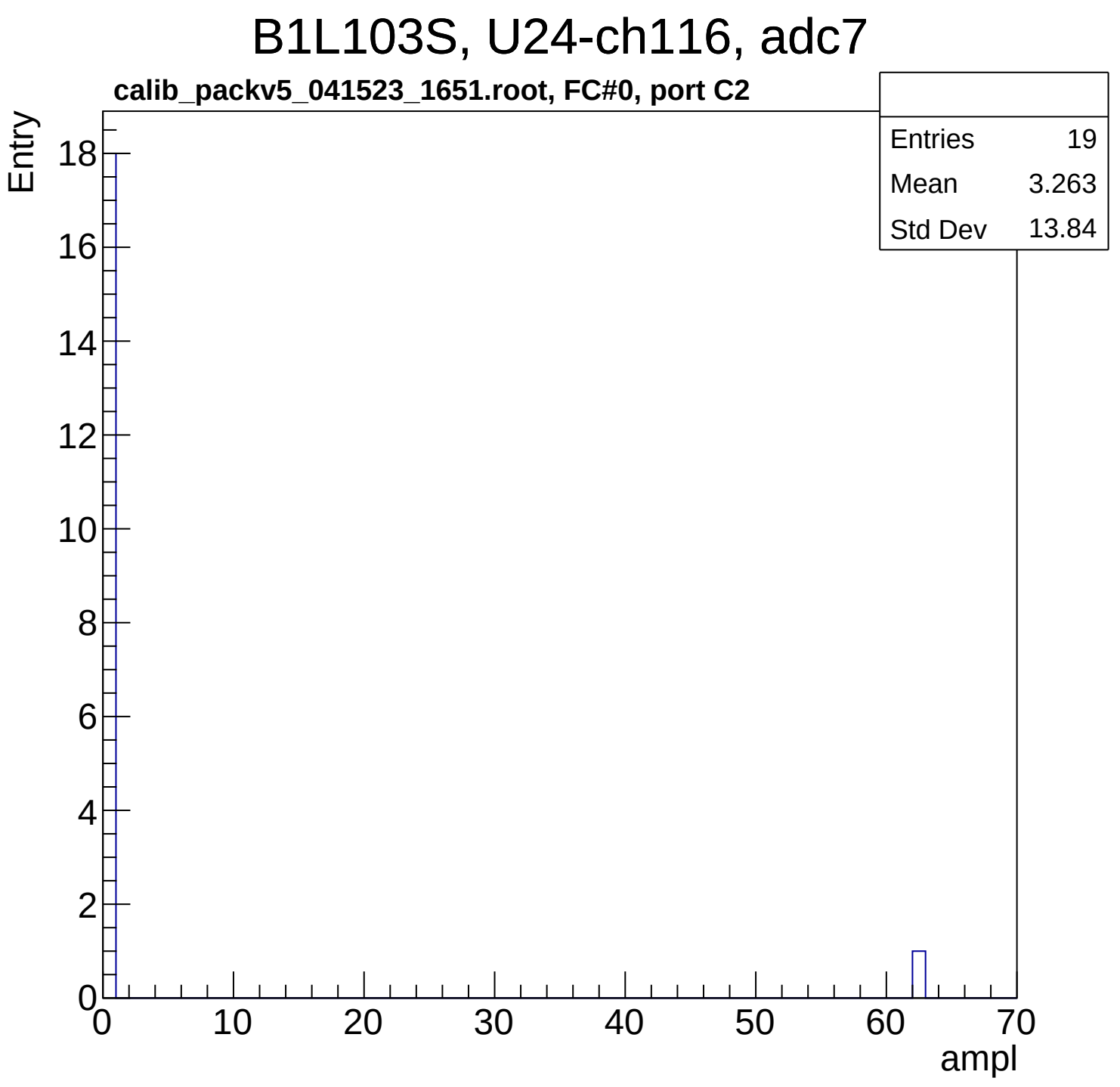
B1L103S, U24-ch116, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 3.263
Std Dev 13.84
Entry
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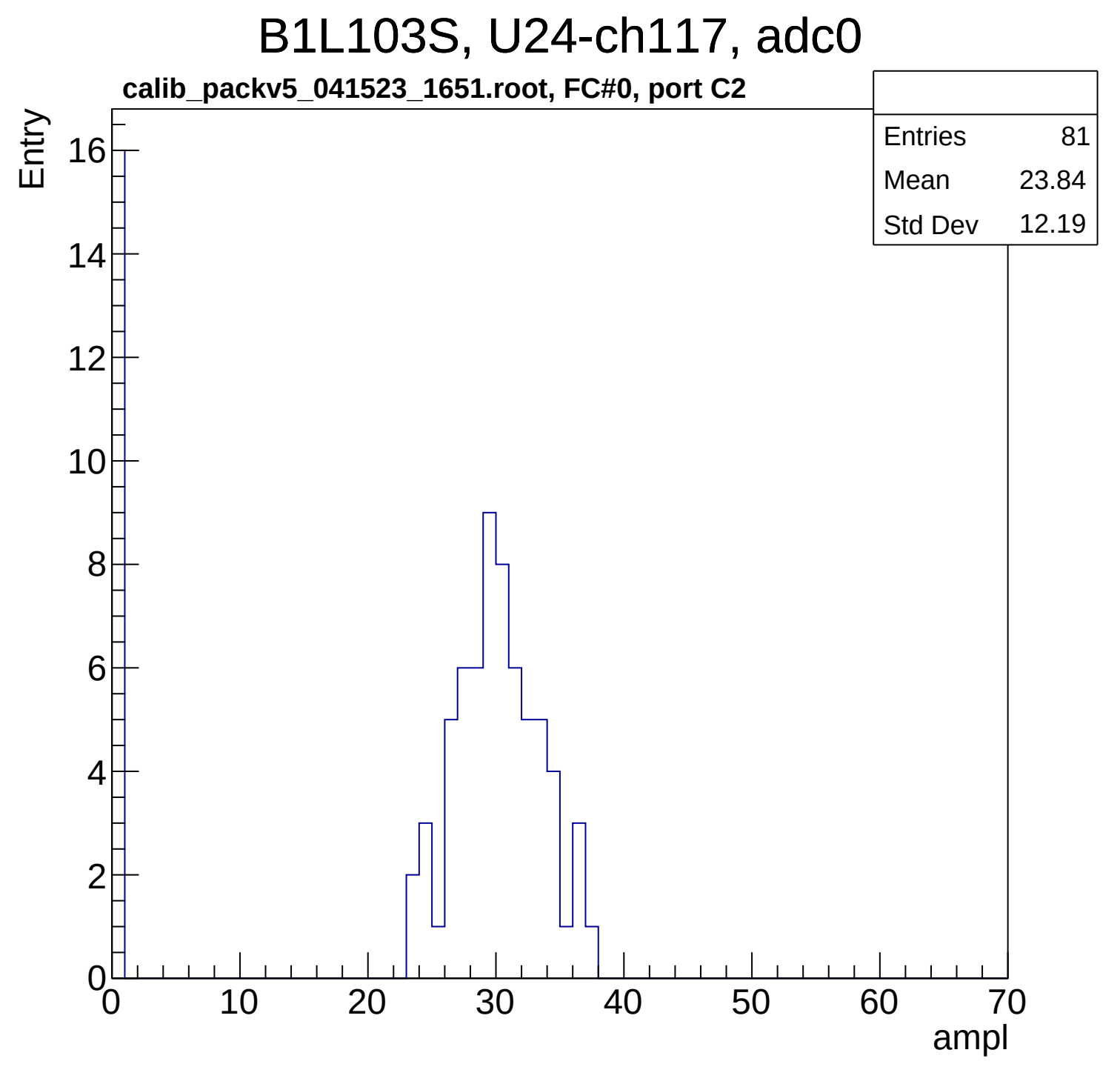
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch117, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 23.84
Std Dev 12.19
Entry
0
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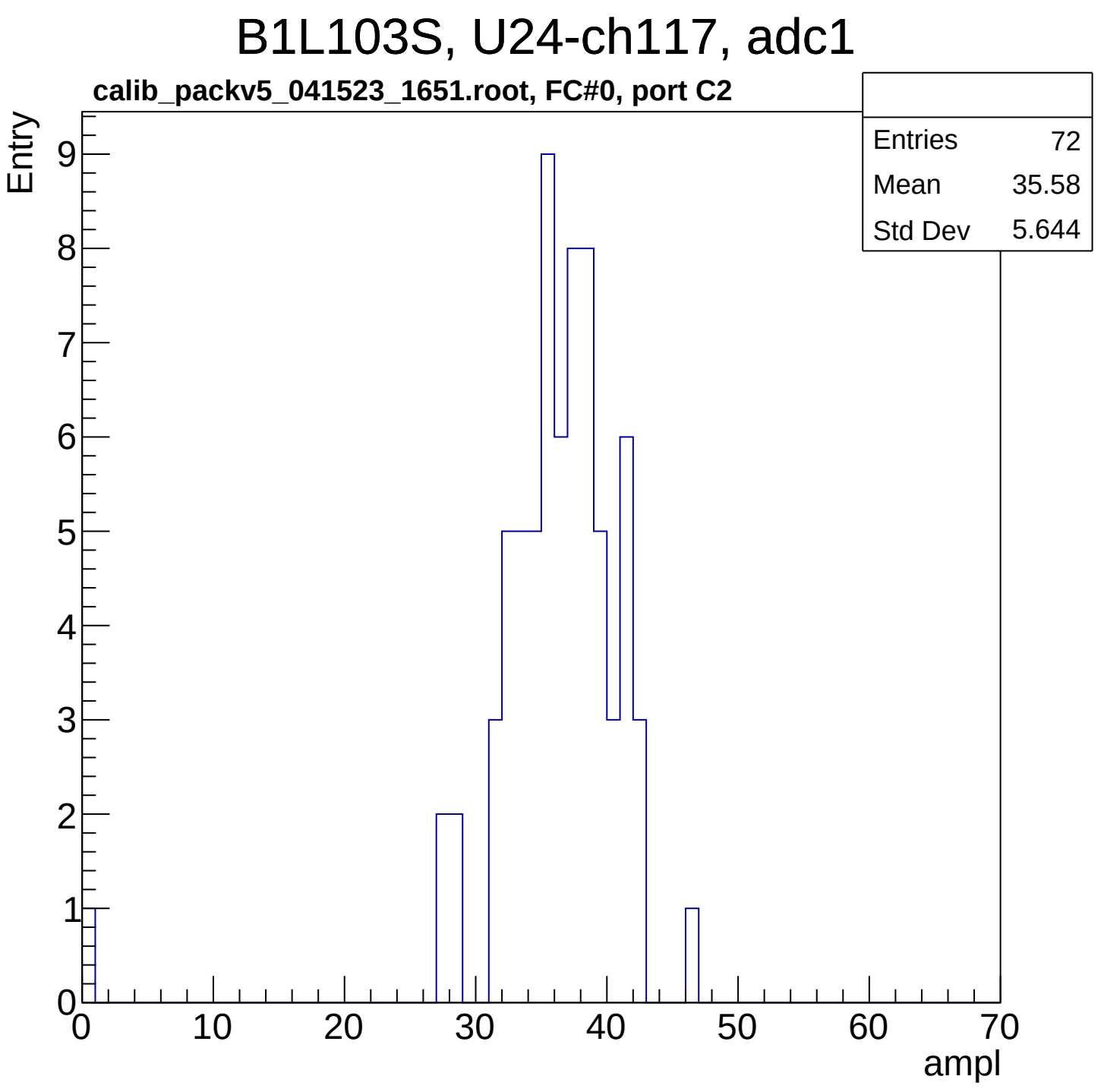
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch117, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 35.58
Std Dev 5.644
Entry
ampl
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3
4
5
6
7
8
9
0
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20
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40
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60
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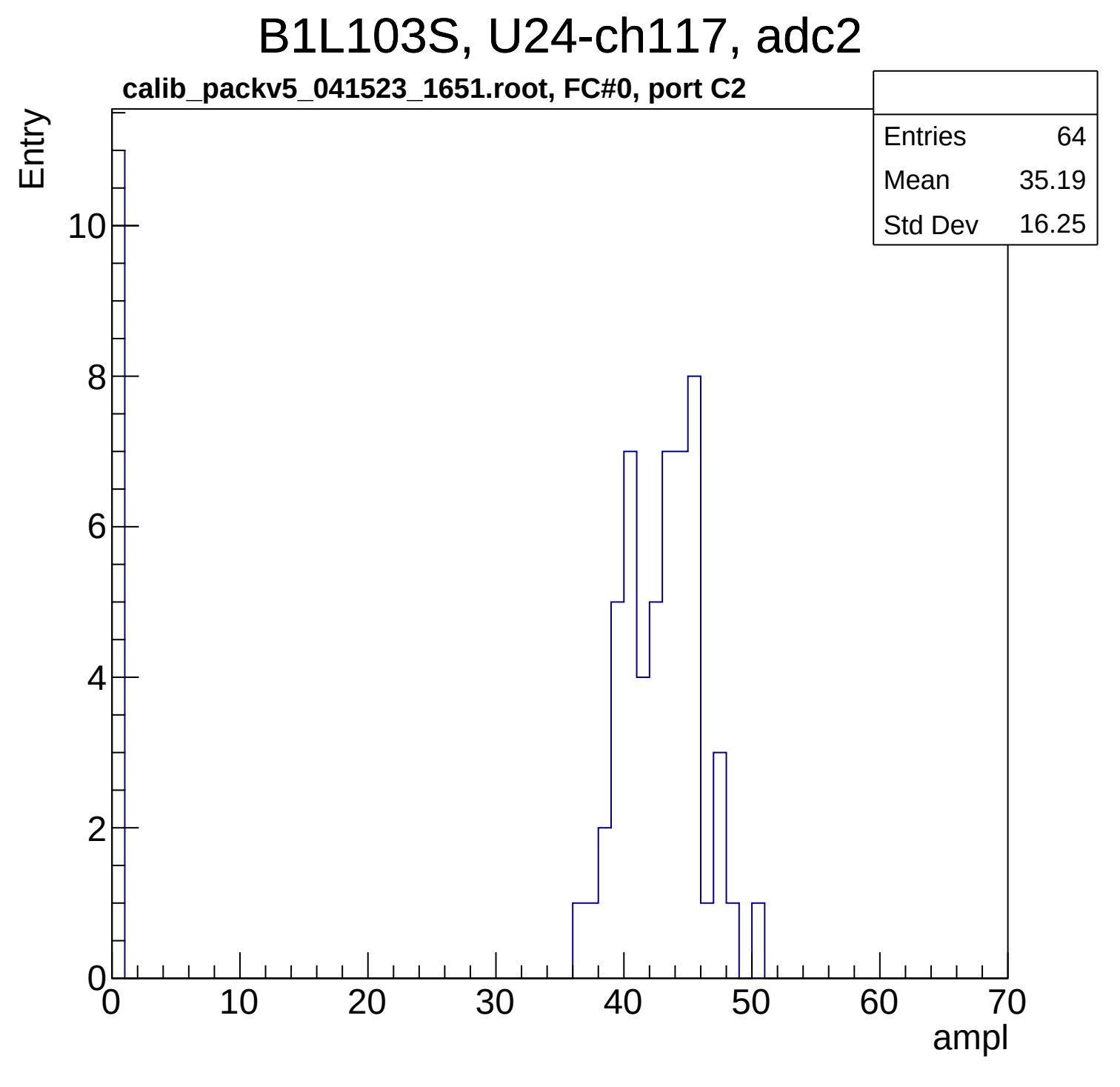
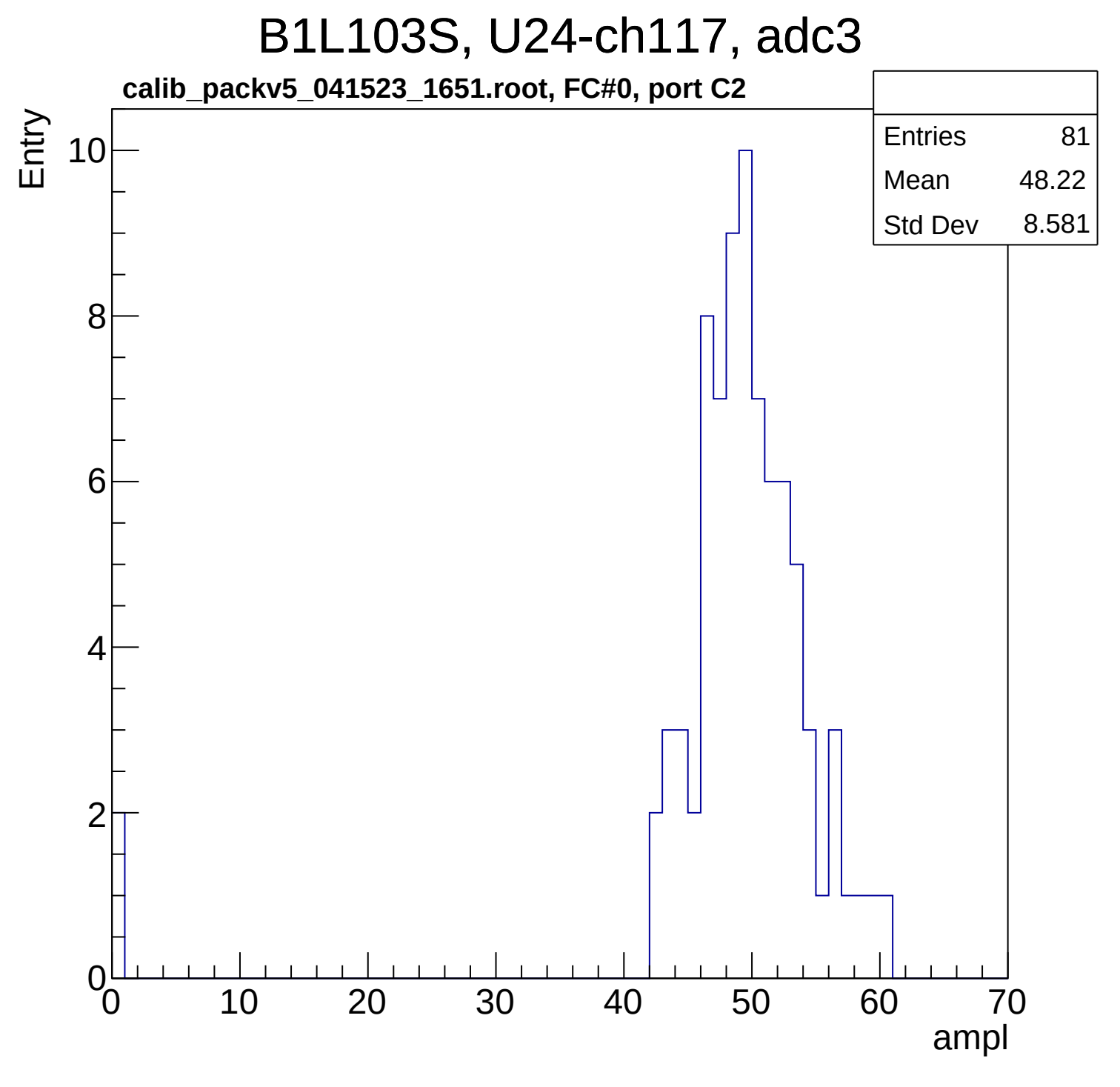
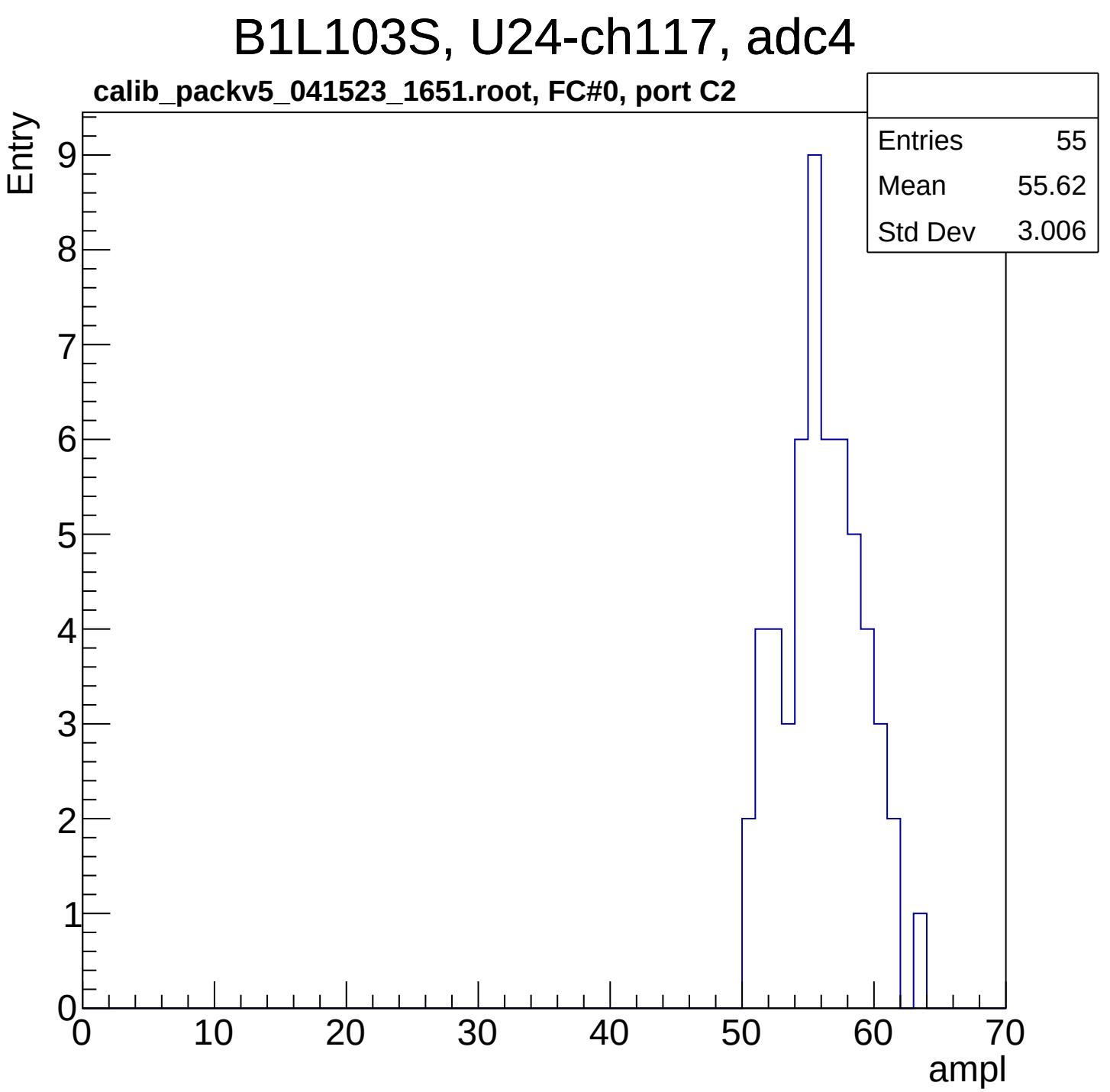

B1L103S, U24-ch117, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 35.19
Std Dev 16.25
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch117, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 48.22
Std Dev 8.581
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U24-ch117, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 55.62
Std Dev 3.006
Entry
ampl
0
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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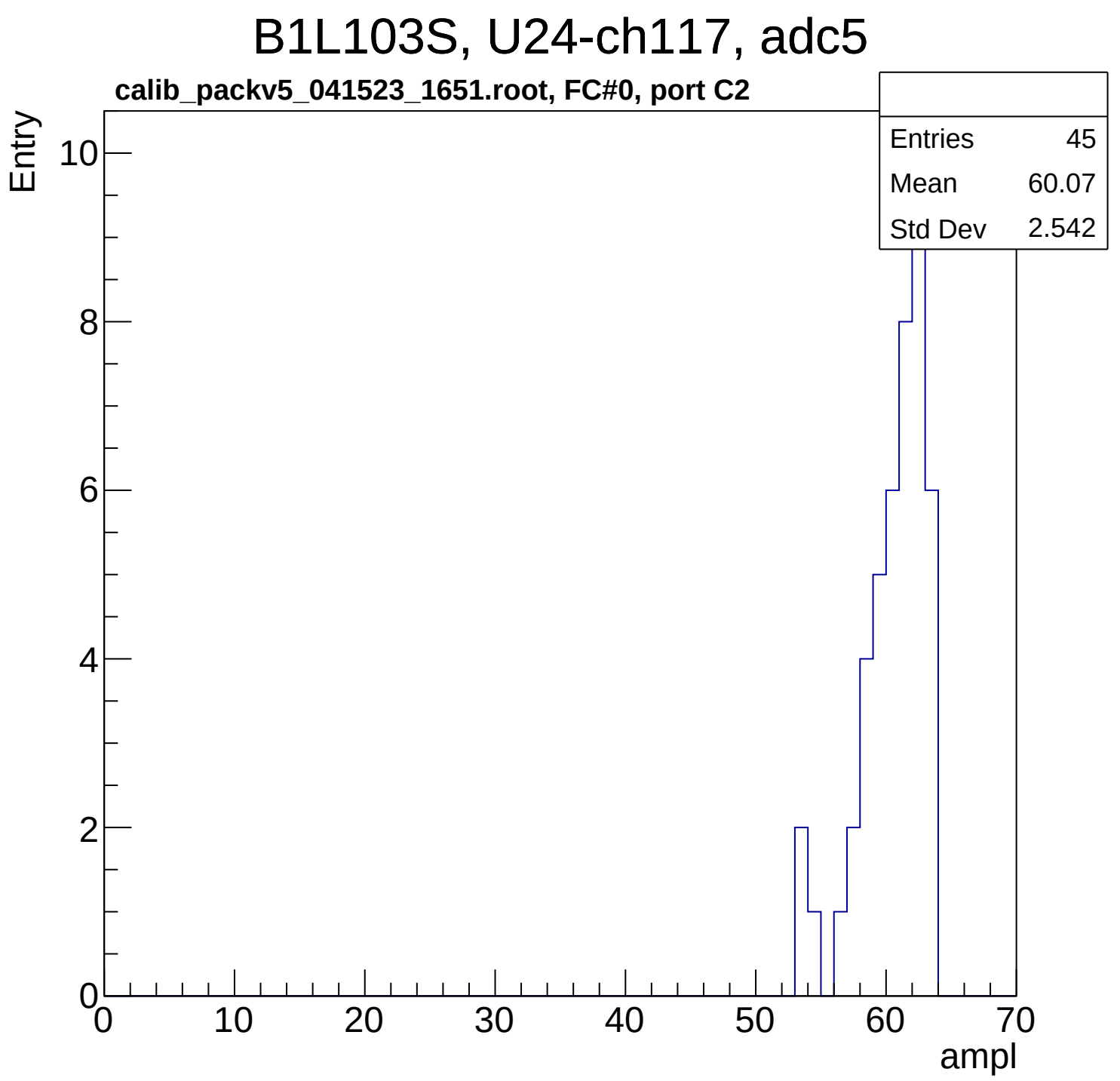
B1L103S, U24-ch117, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 60.07
Std Dev 2.542
Entry
ampl
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2
4
6
8
10
0
10
20
30
40
50
60
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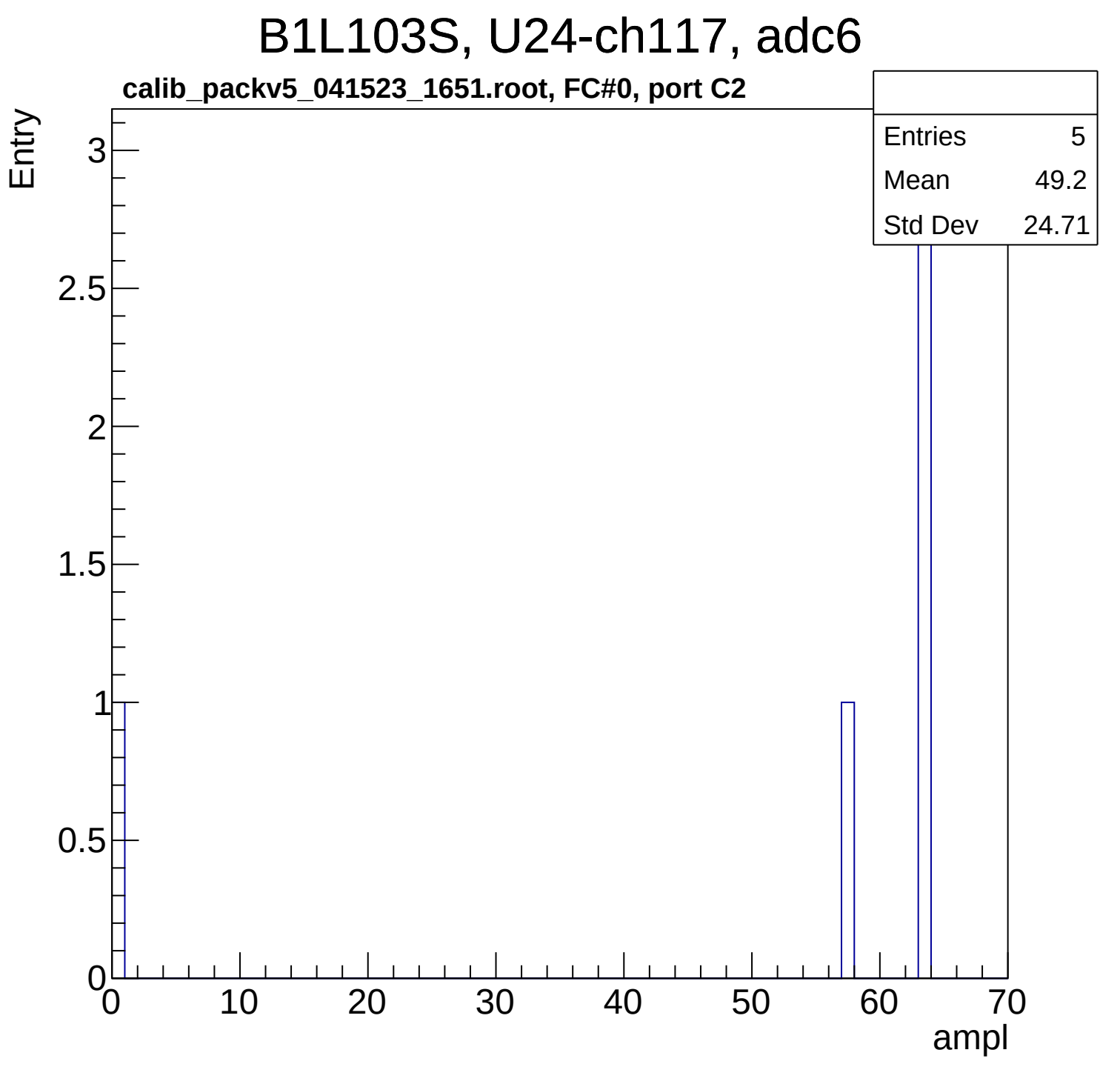
B1L103S, U24-ch117, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 5
Mean 49.2
Std Dev 24.71
Entry
ampl
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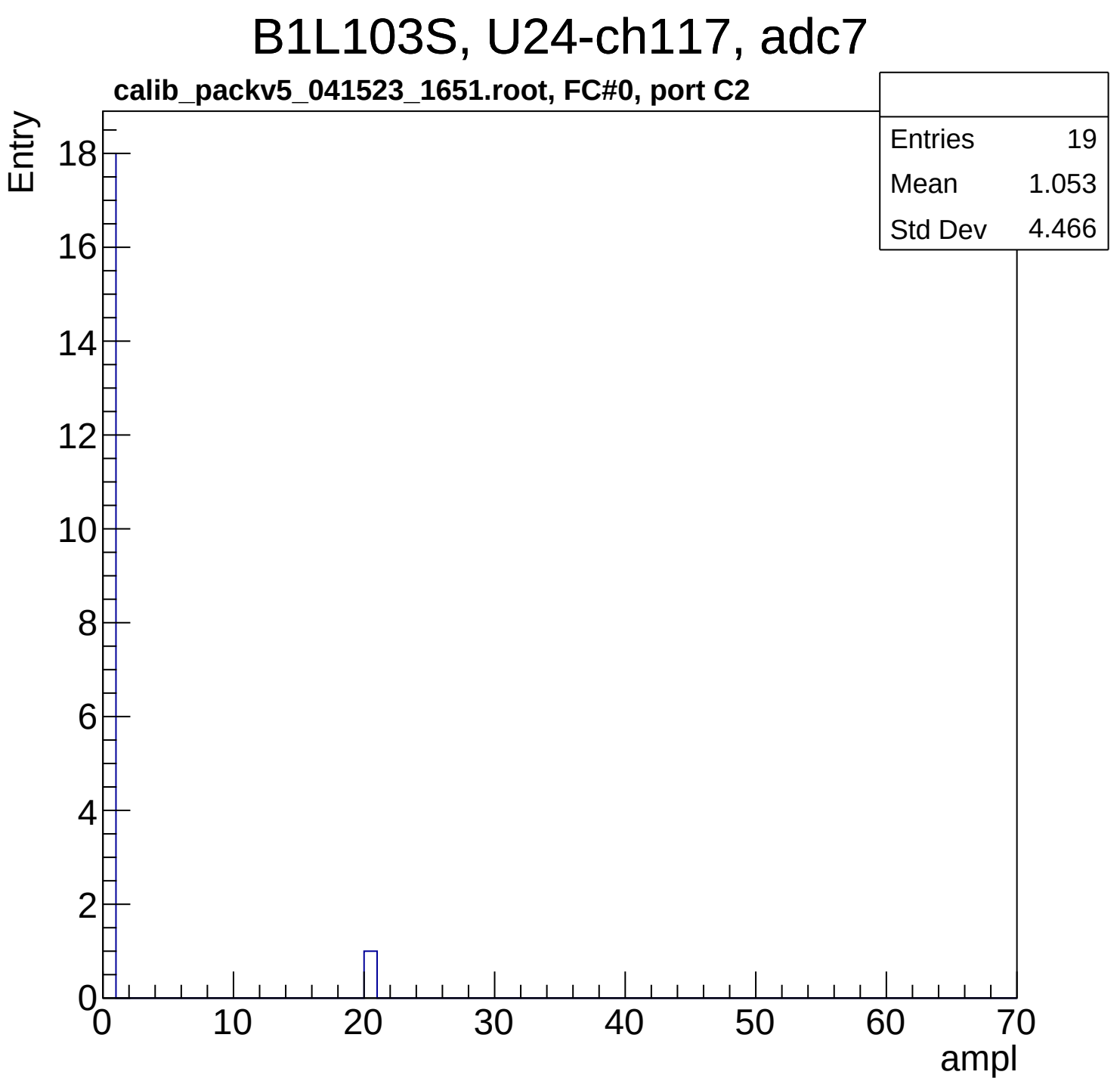
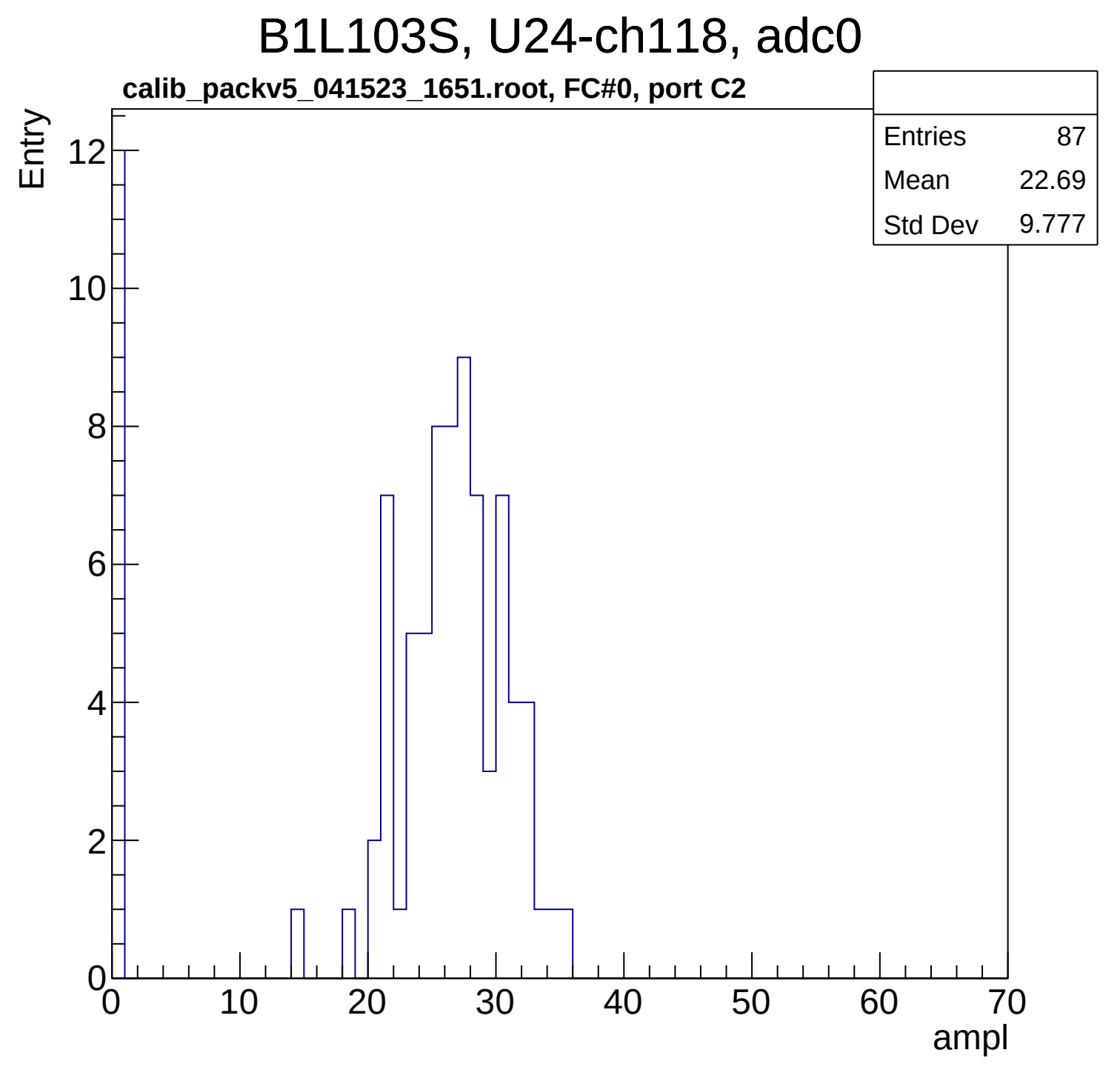
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U24-ch117, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.053
Std Dev 4.466
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70


B1L103S, U24-ch118, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 87
Mean 22.69
Std Dev 9.777
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
50
60
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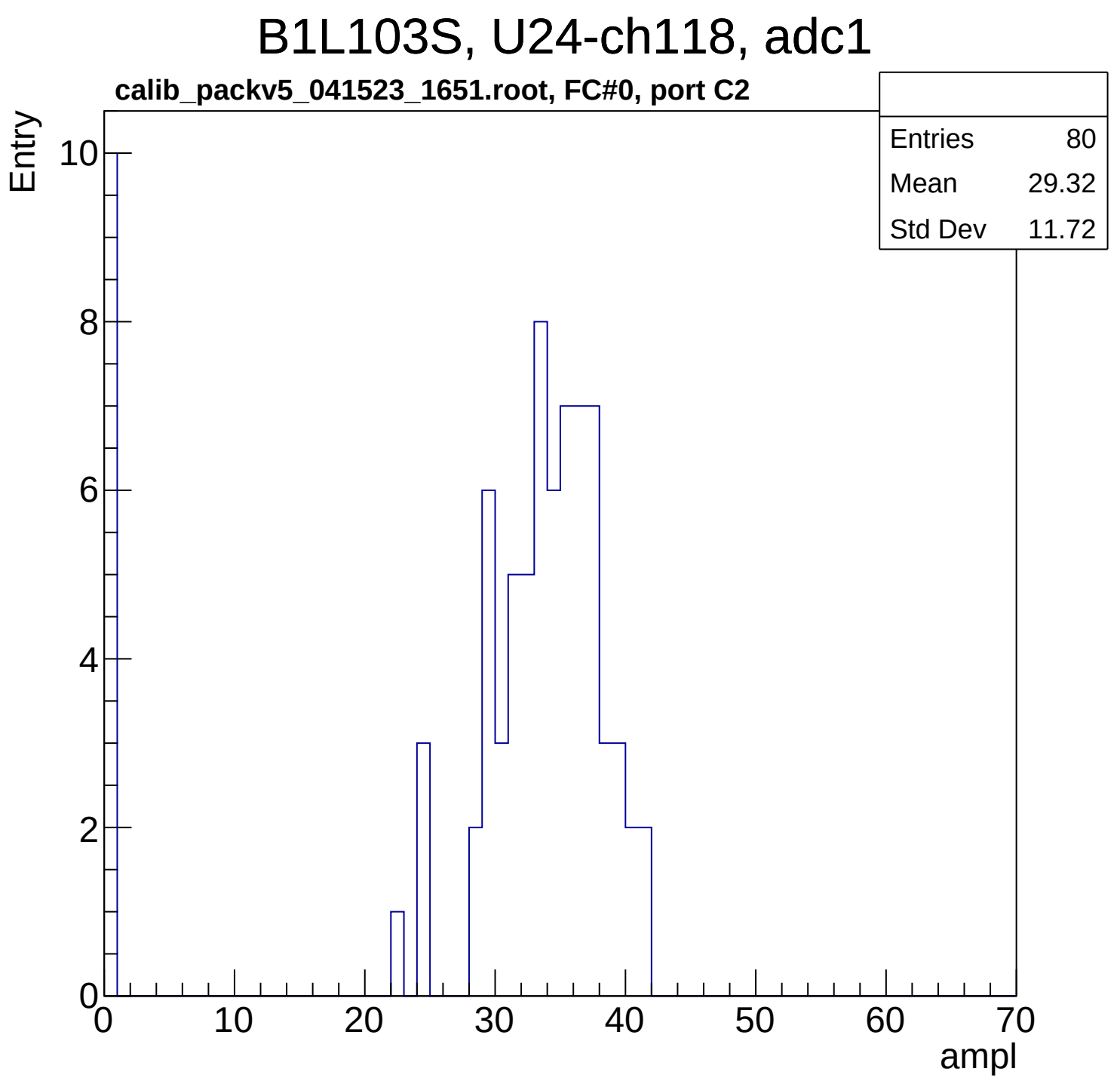
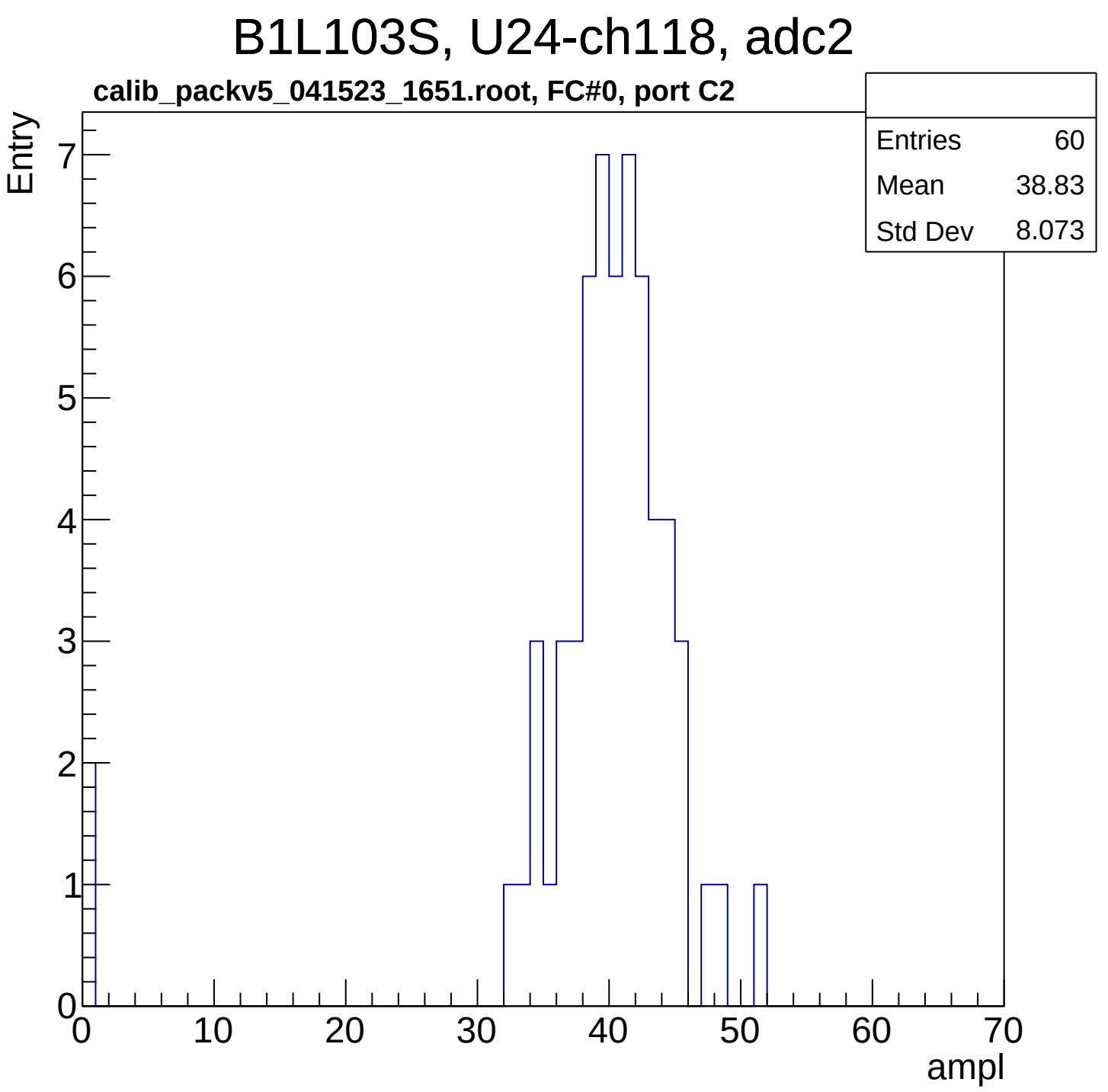

B1L103S, U24-ch118, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 29.32
Std Dev 11.72
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch118, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 38.83
Std Dev 8.073
Entry
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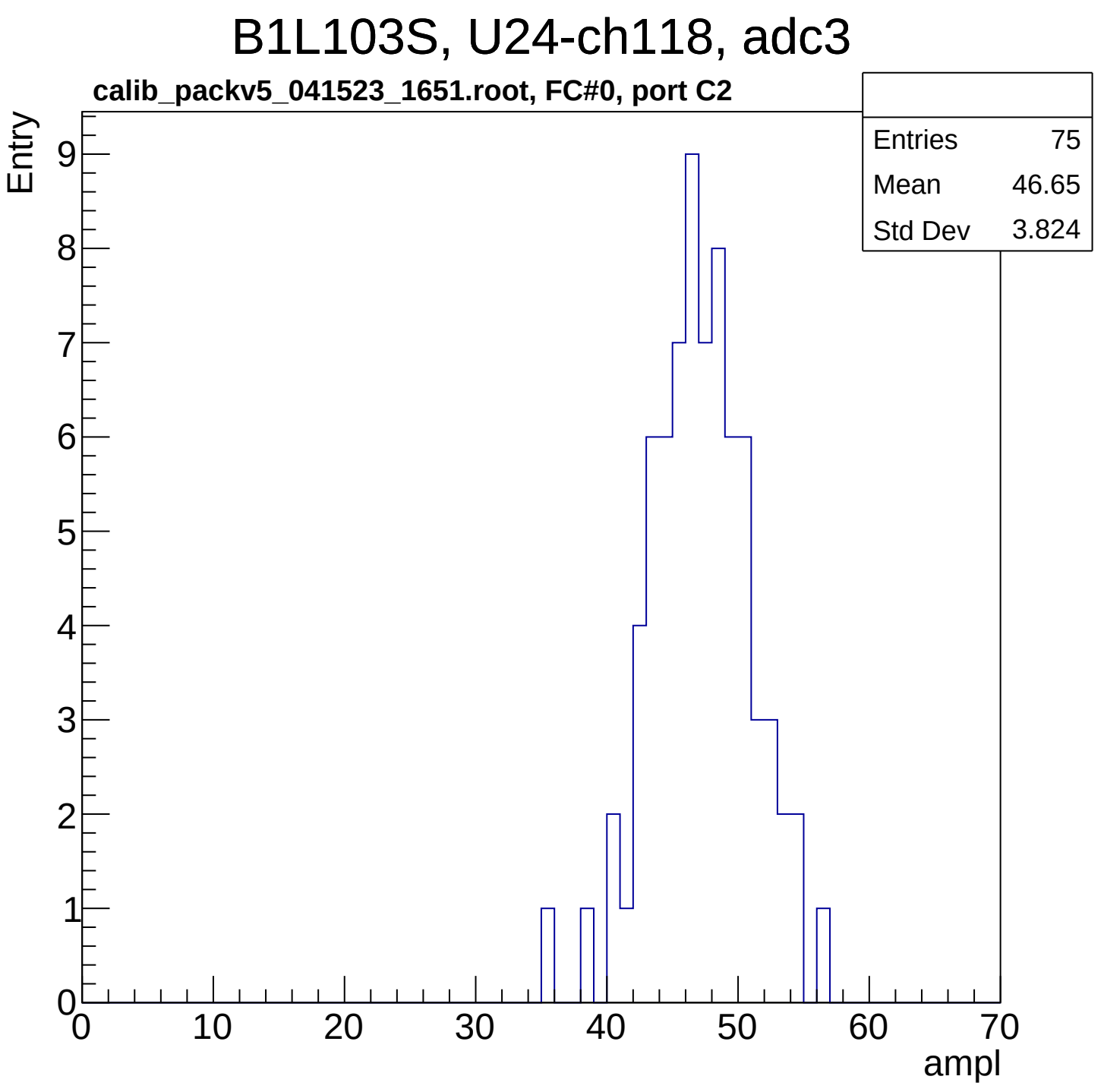
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch118, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 46.65
Std Dev 3.824
Entry
ampl
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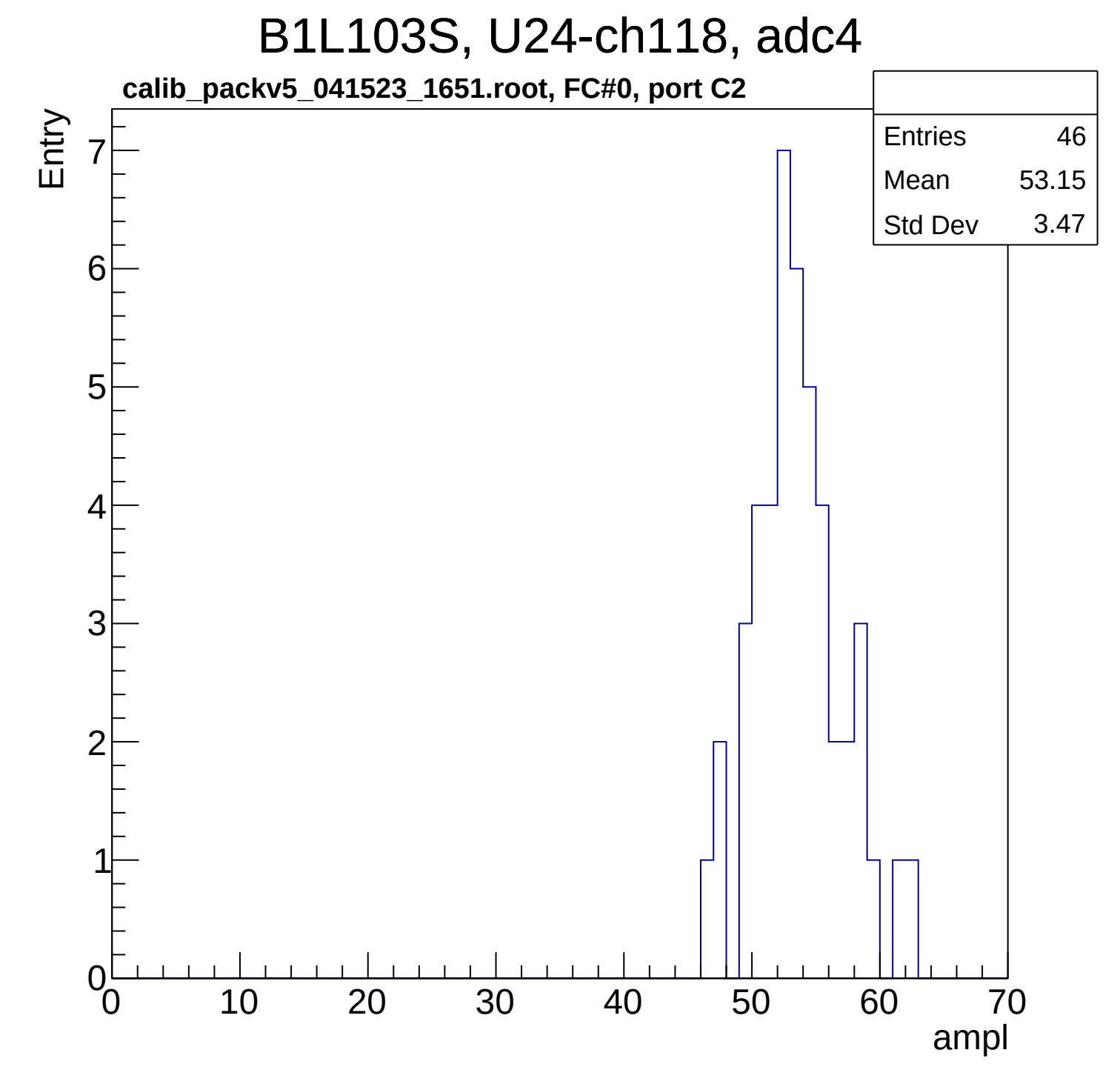
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U24-ch118, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 53.15
Std Dev 3.47
Entry
ampl
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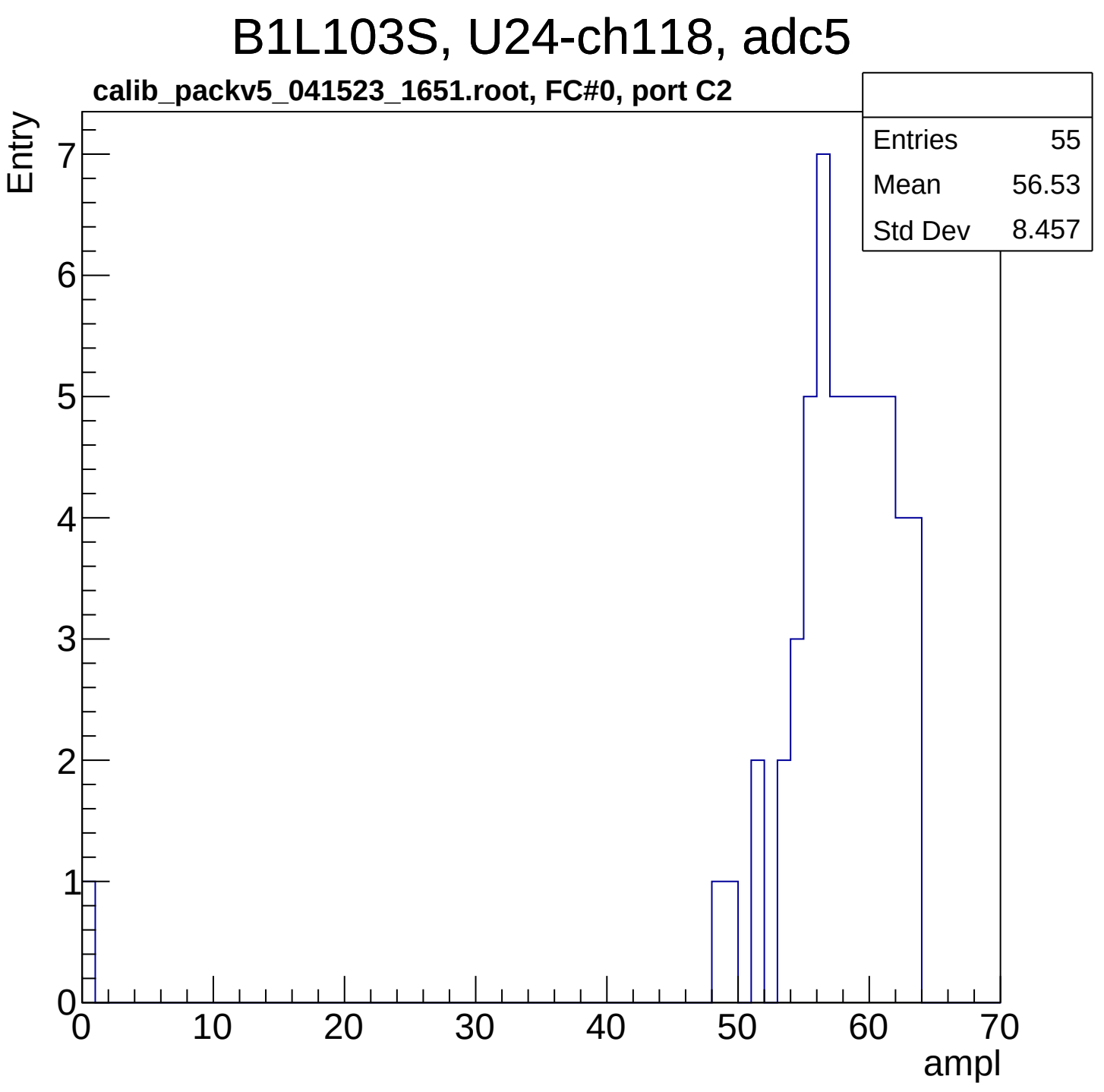
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U24-ch118, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 56.53
Std Dev 8.457
Entry
ampl
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1
2
3
4
5
6
7
0
10
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40
50
60
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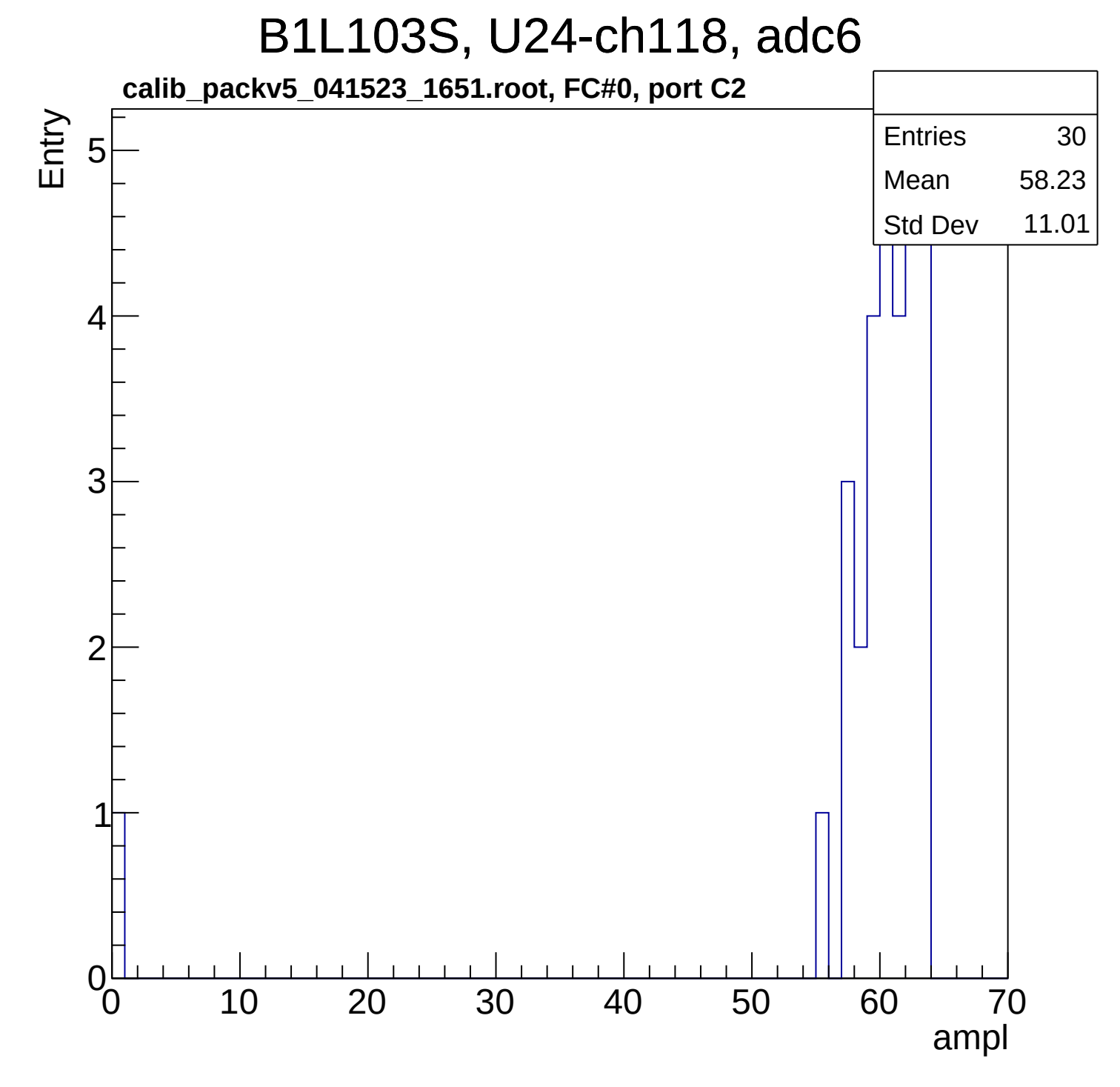
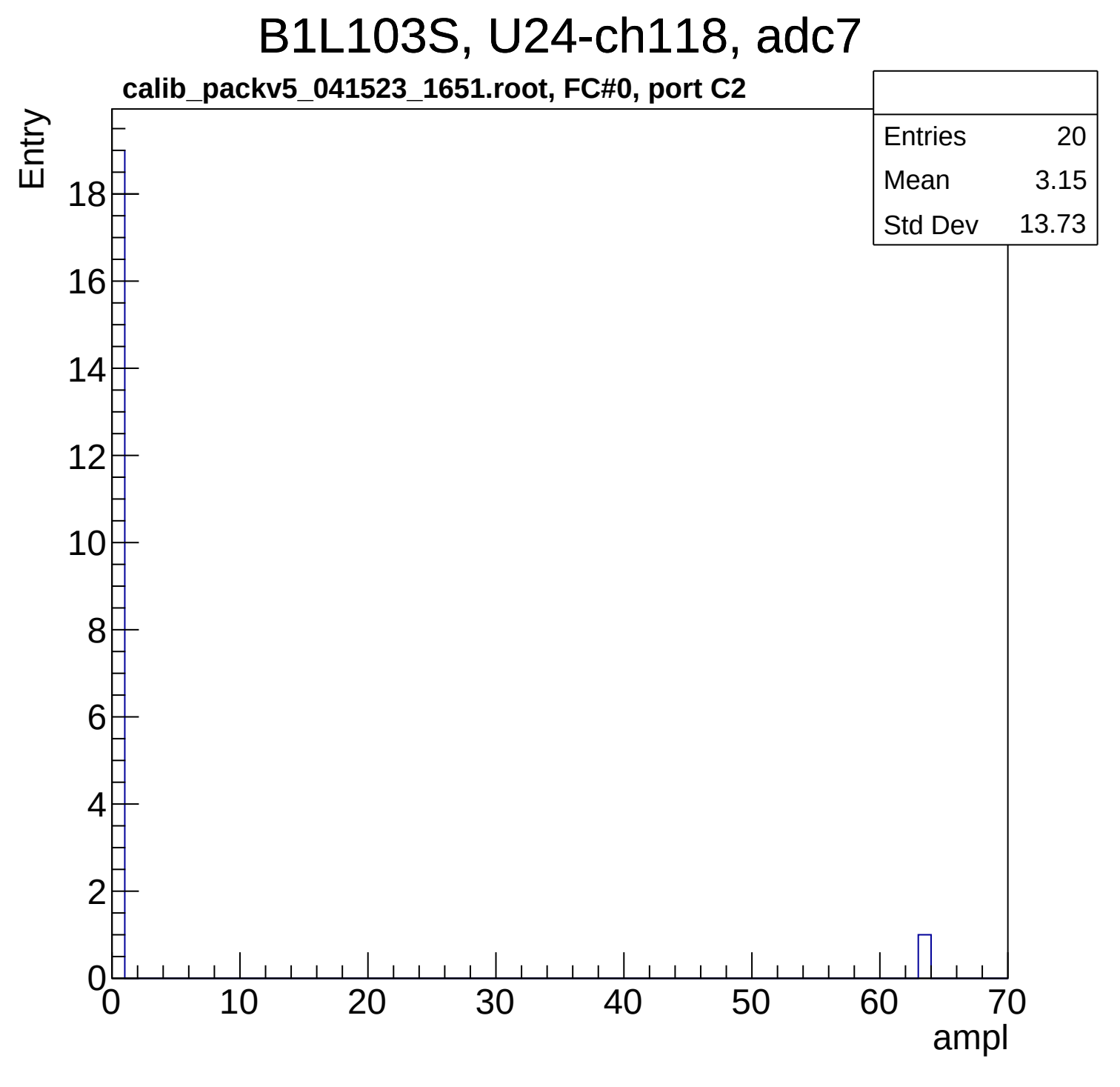

B1L103S, U24-ch118, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 30
Mean 58.23
Std Dev 11.01
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U24-ch118, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
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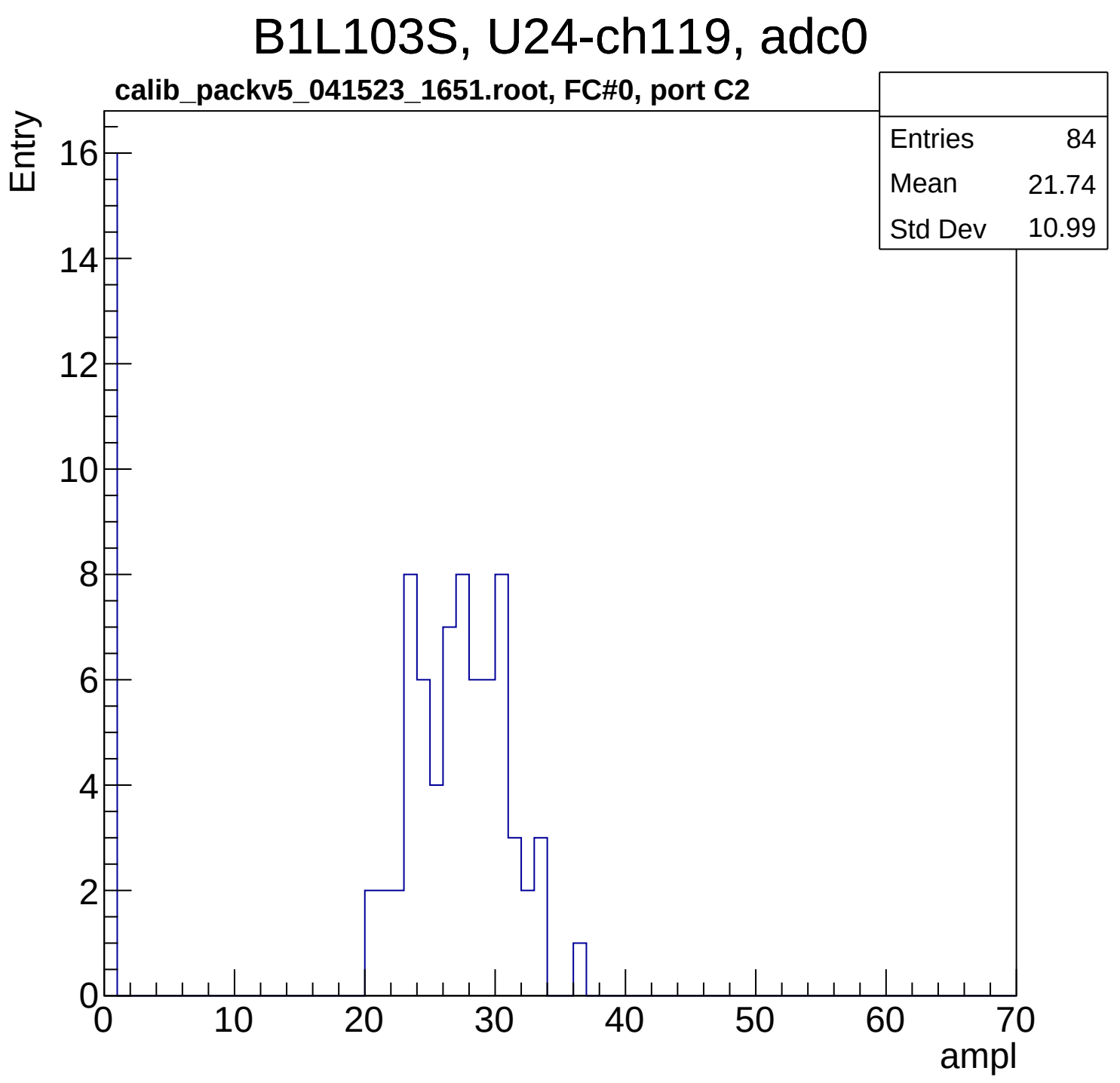
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch119, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 21.74
Std Dev 10.99
Entry
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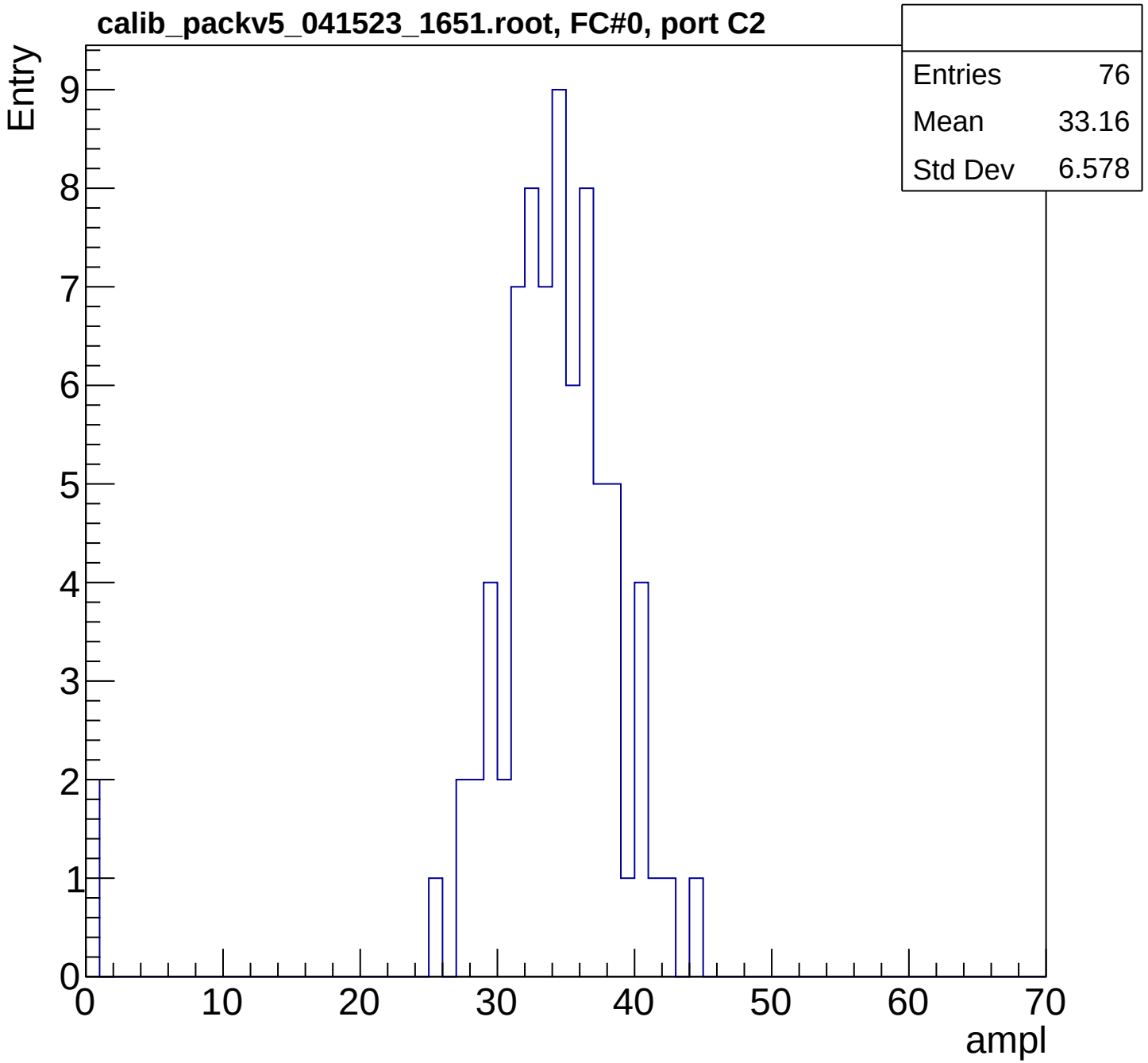
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch119, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 33.16
Std Dev 6.578
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
50
60
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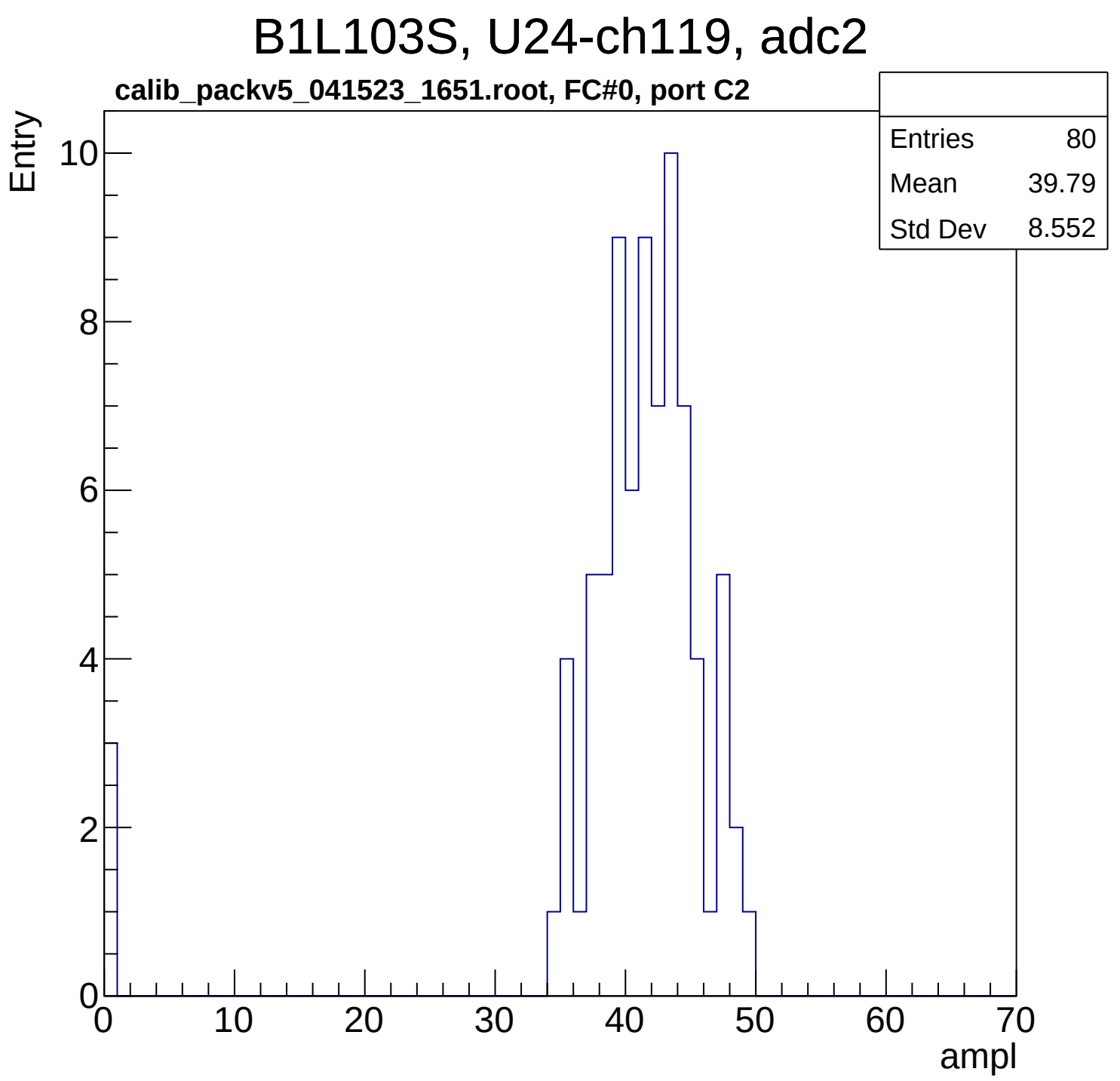
B1L103S, U24-ch119, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 39.79
Std Dev 8.552
Entry
ampl
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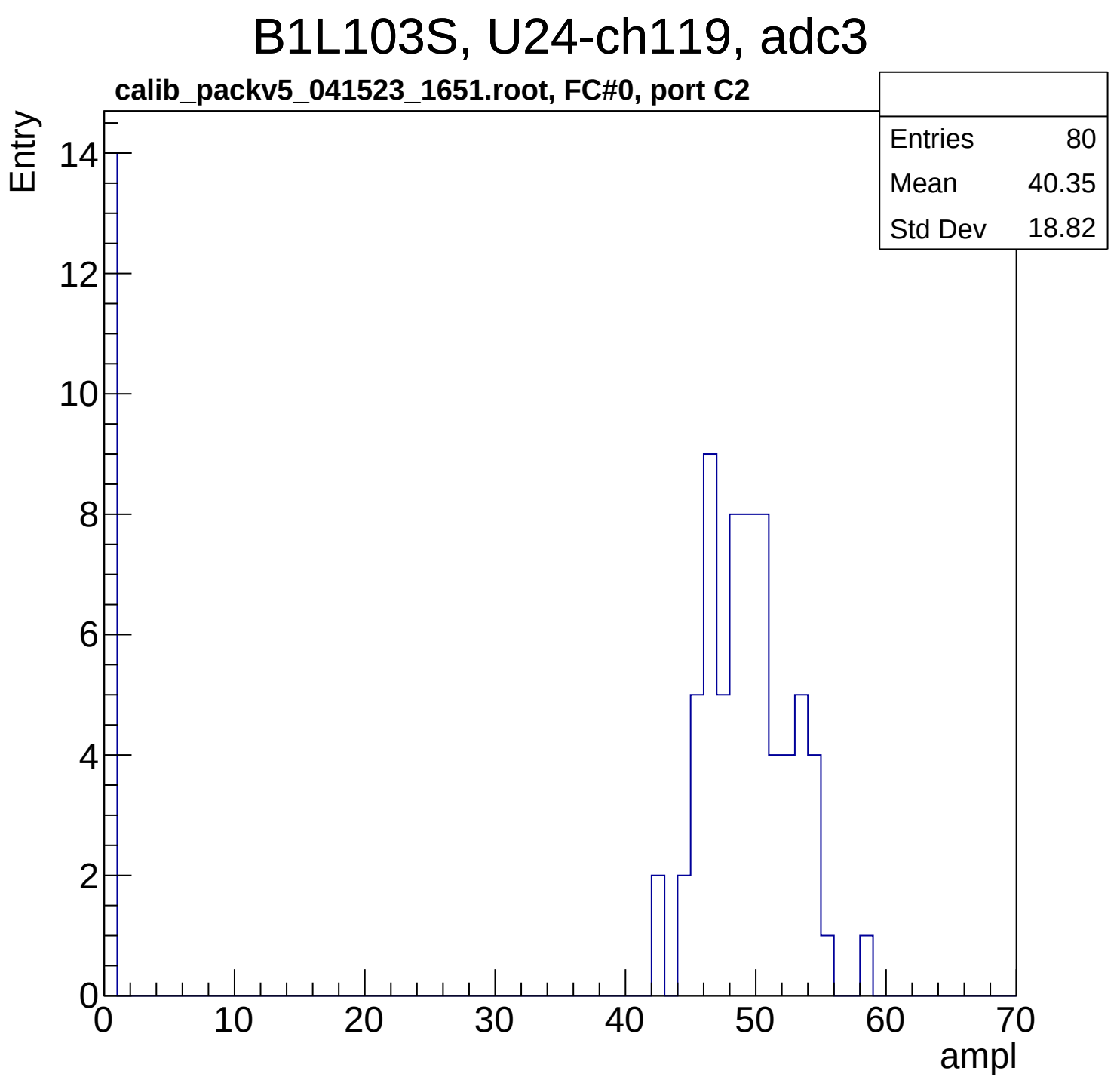
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U24-ch119, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 40.35
Std Dev 18.82
Entry
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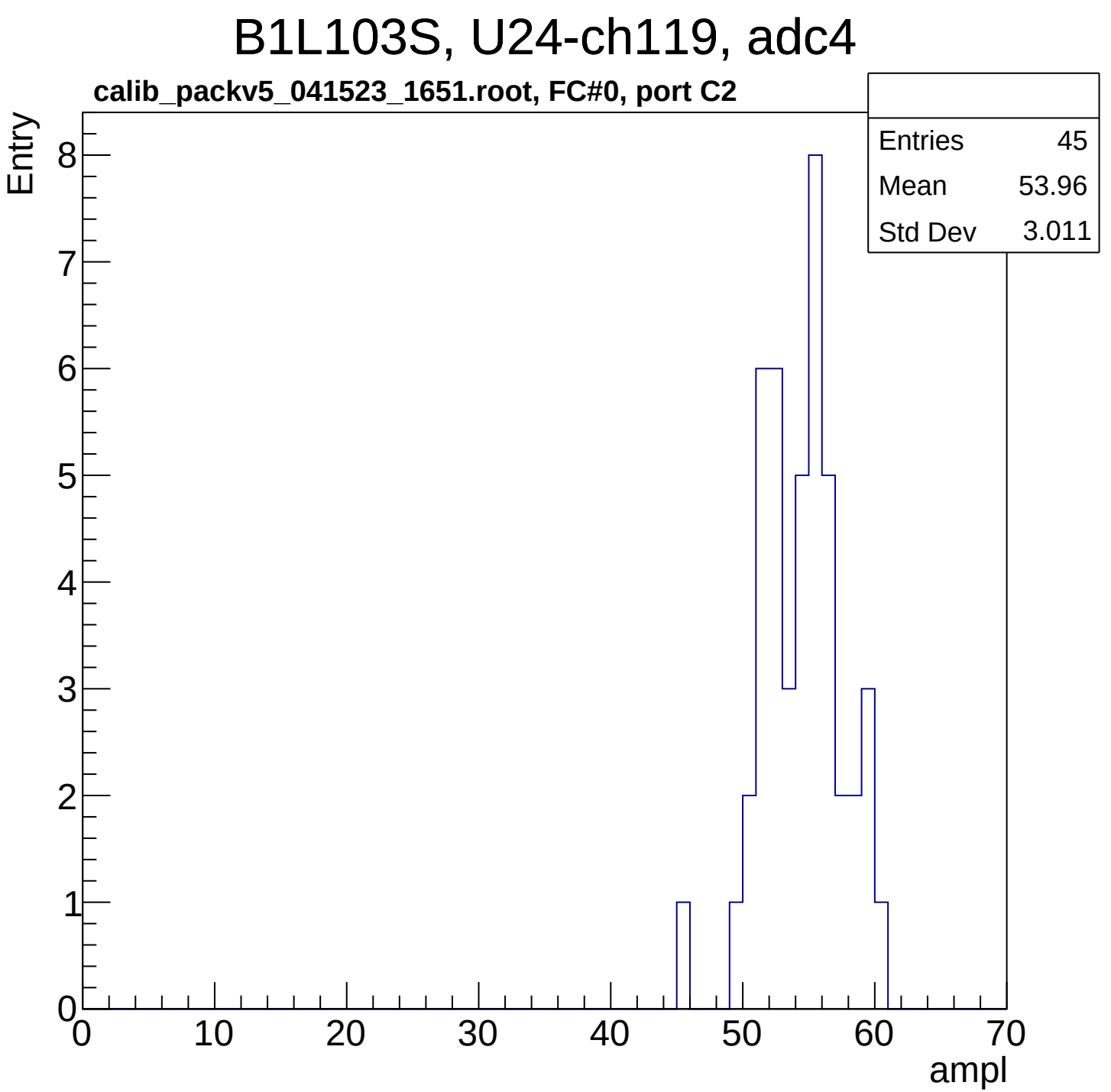
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch119, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 53.96
Std Dev 3.011
Entry
ampl
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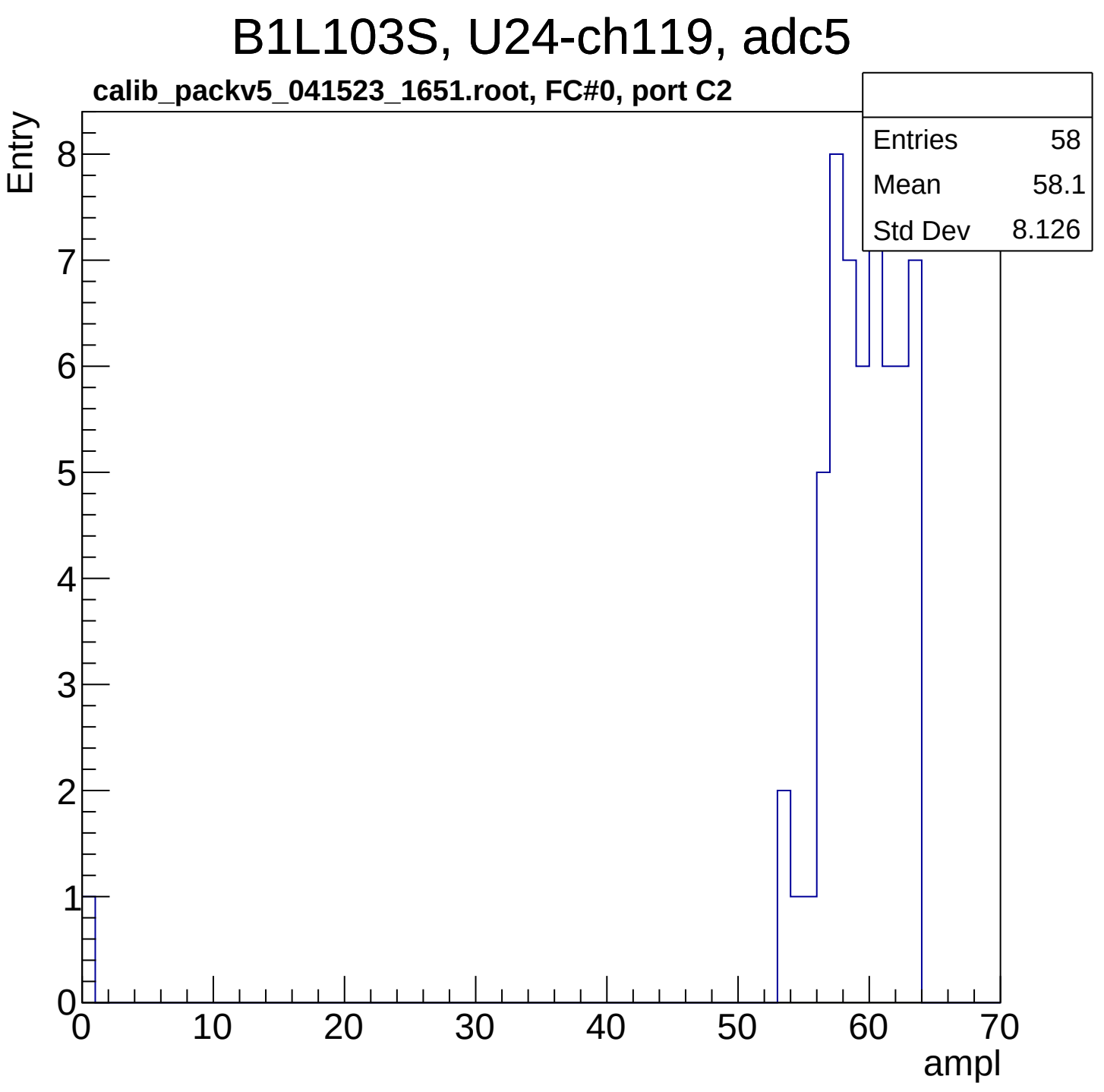
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U24-ch119, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 58.1
Std Dev 8.126
Entry
ampl
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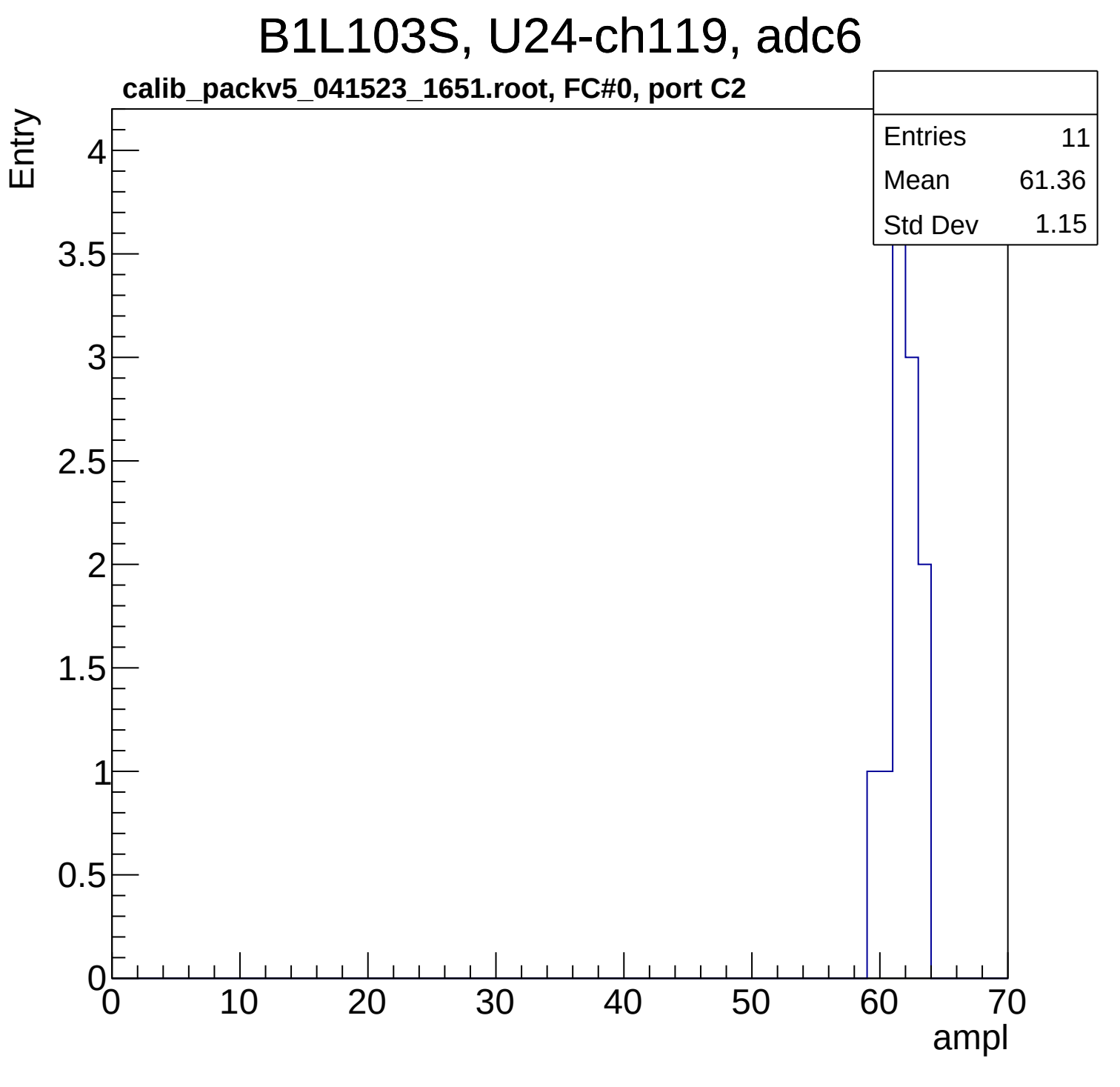
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U24-ch119, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 61.36
Std Dev 1.15
Entry
ampl
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0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
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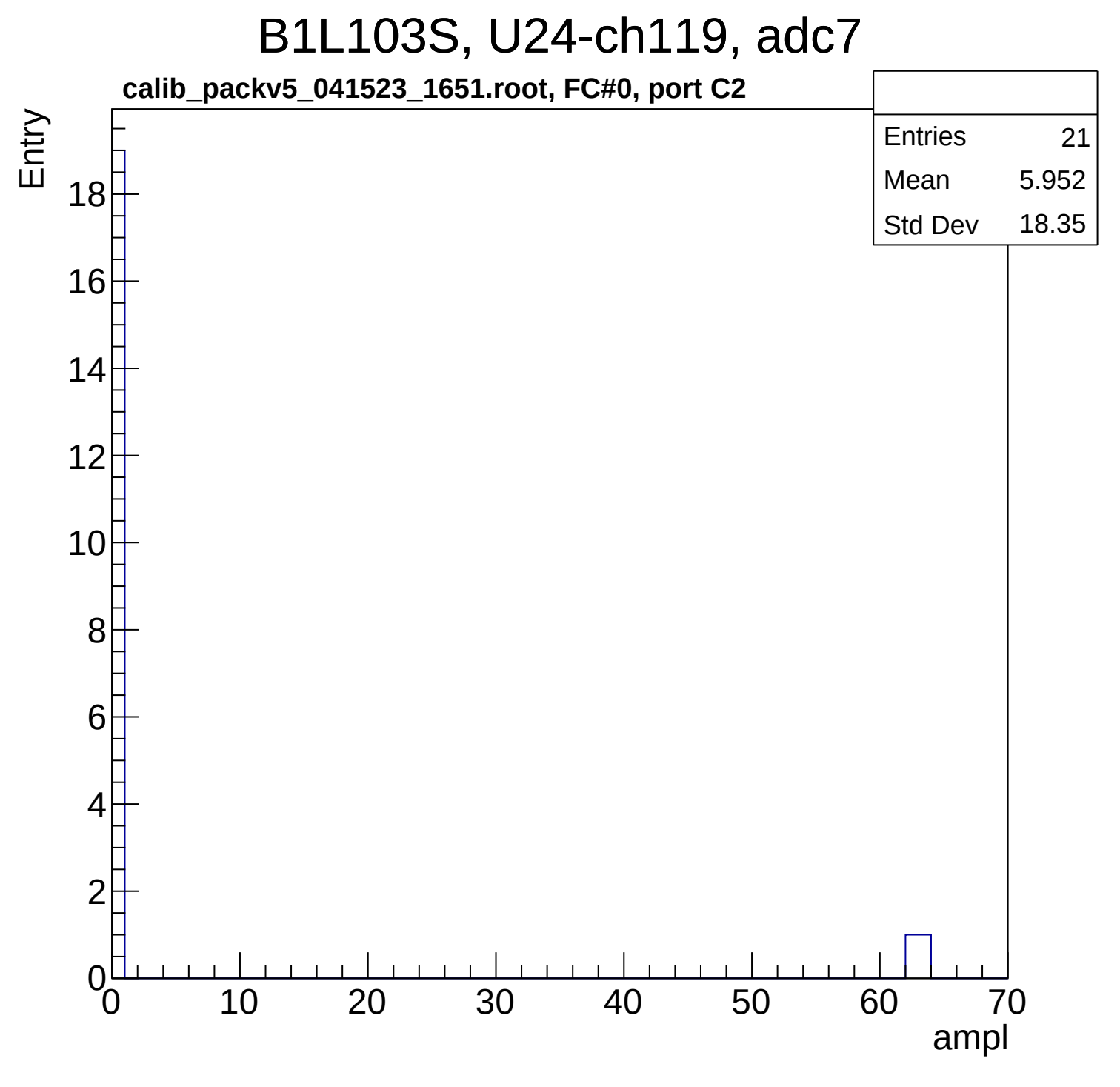
60
70


B1L103S, U24-ch119, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 5.952
Std Dev 18.35
Entry
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6
8
10
12
14
16
18
0
10
20
30
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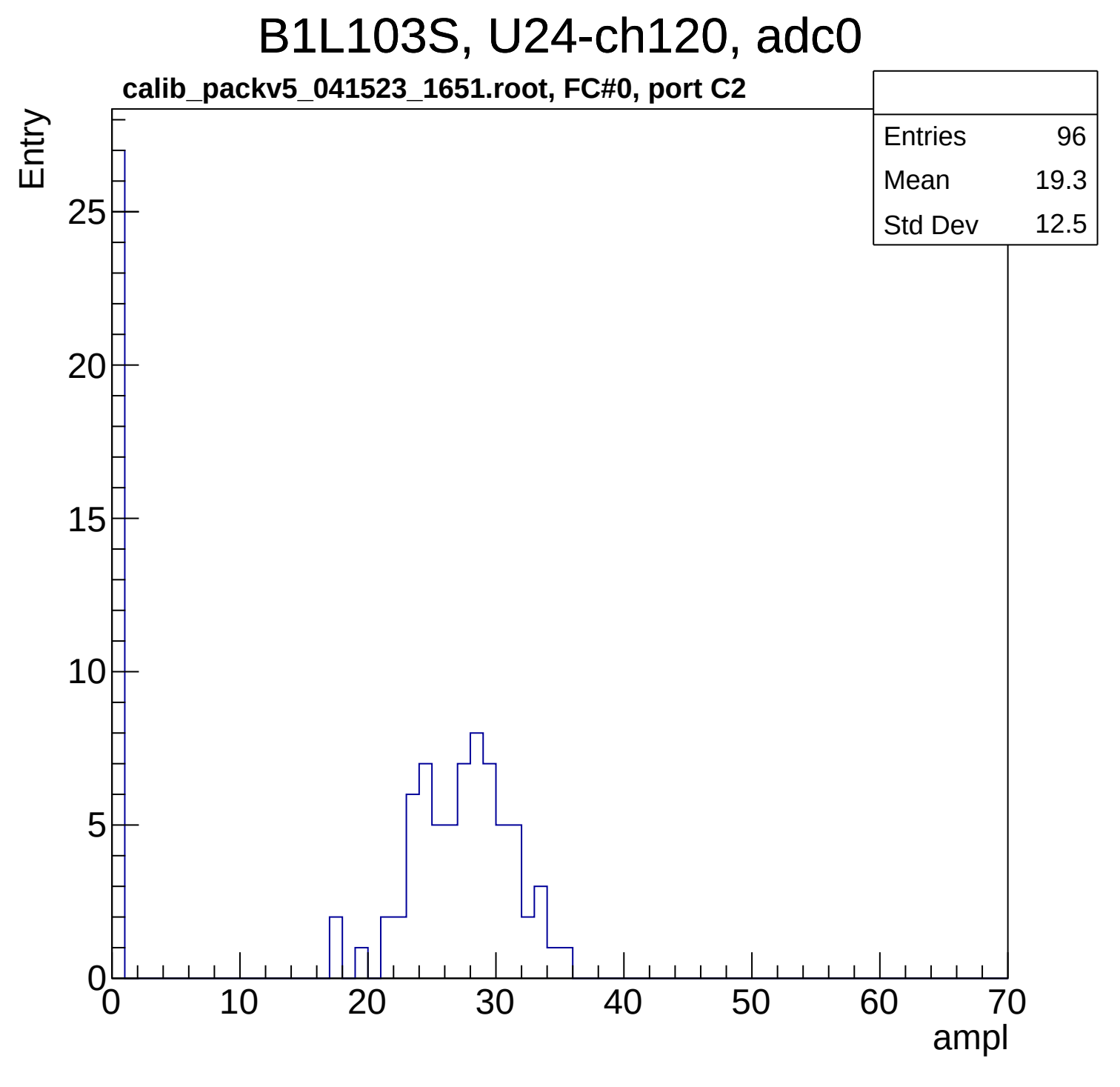
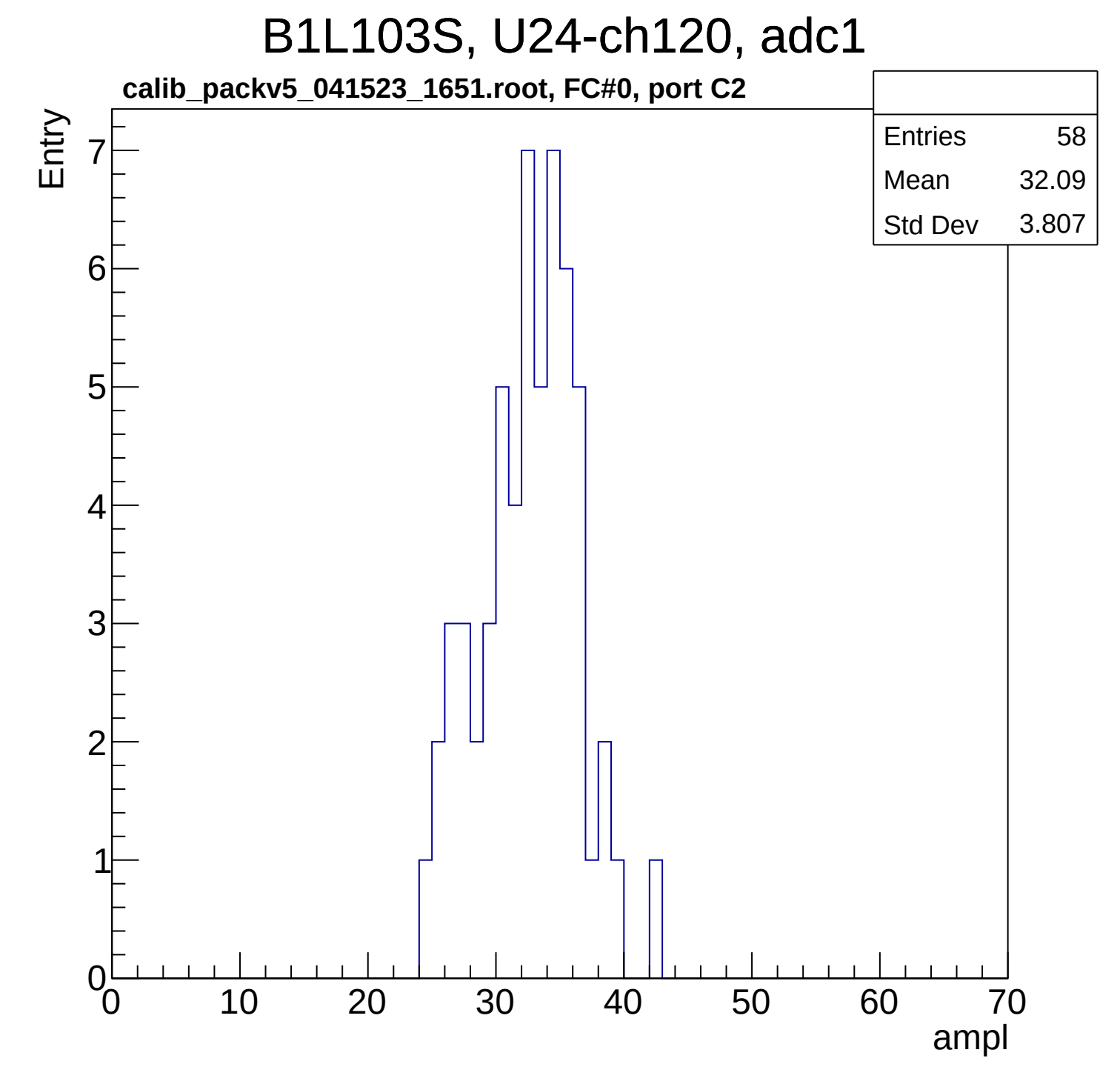
50
60
70
ampl


B1L103S, U24-ch120, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 96
Mean 19.3
Std Dev 12.5
Entry
0
5
10
15
20
25
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch120, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 32.09
Std Dev 3.807
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
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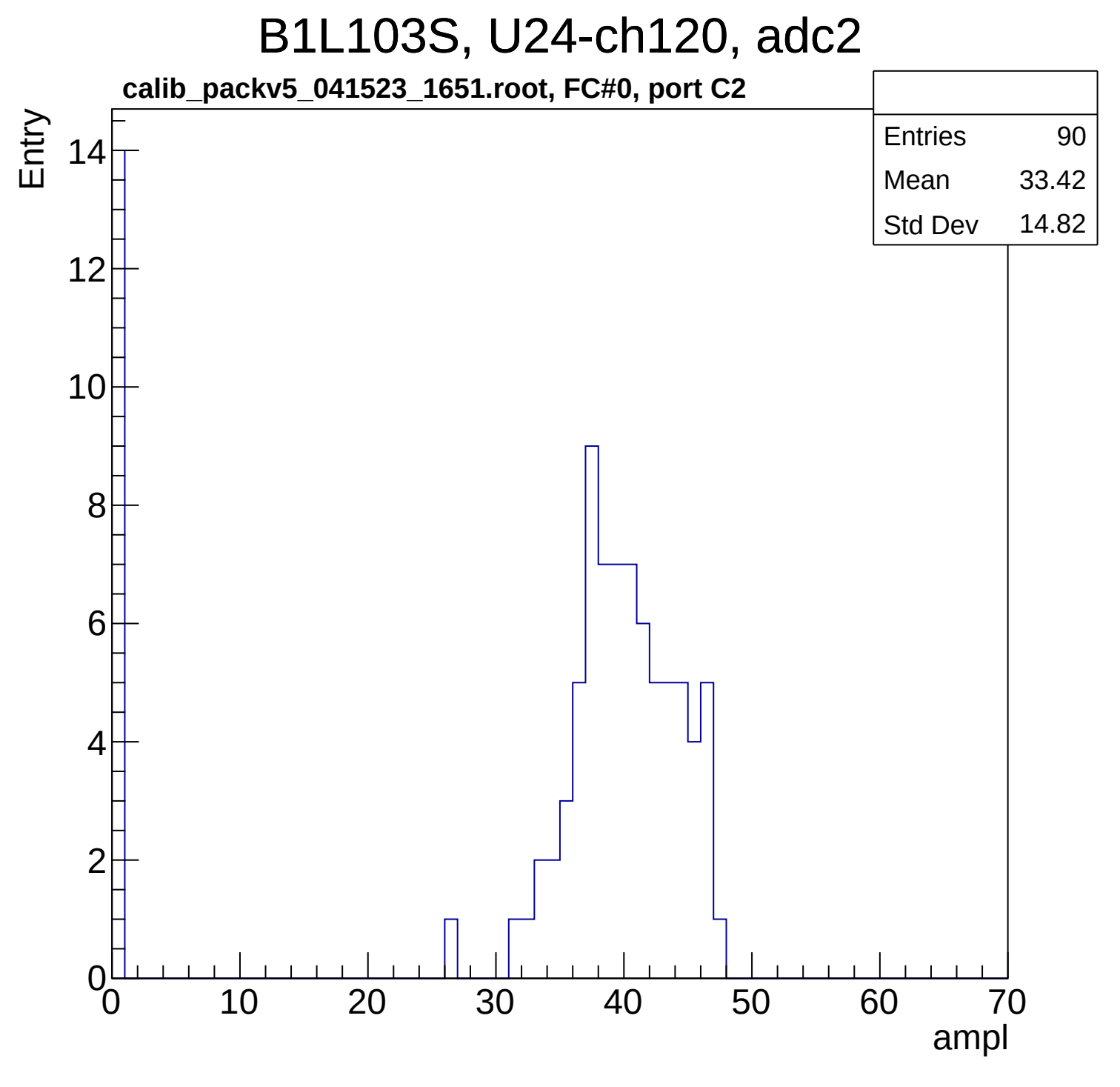
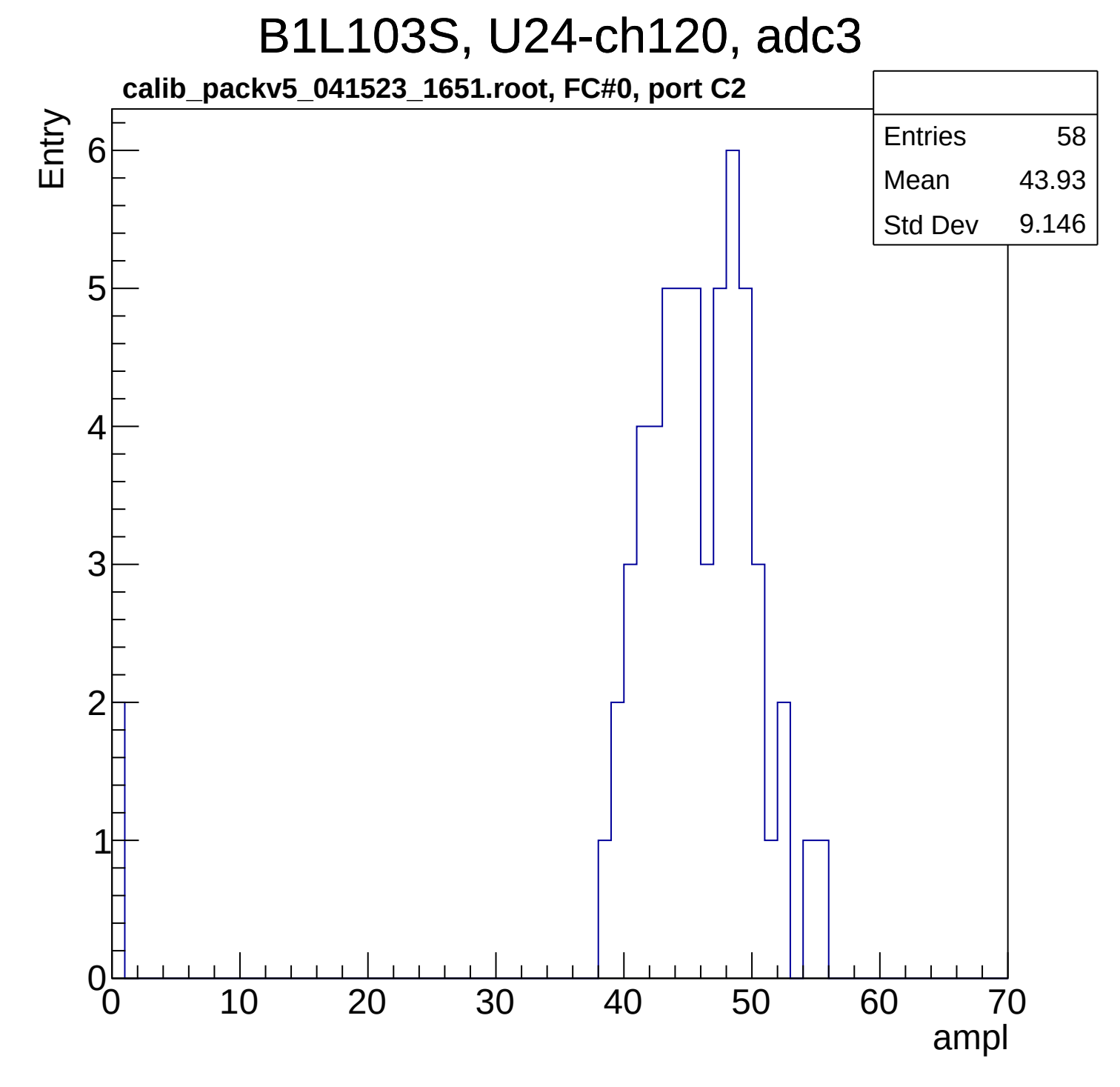
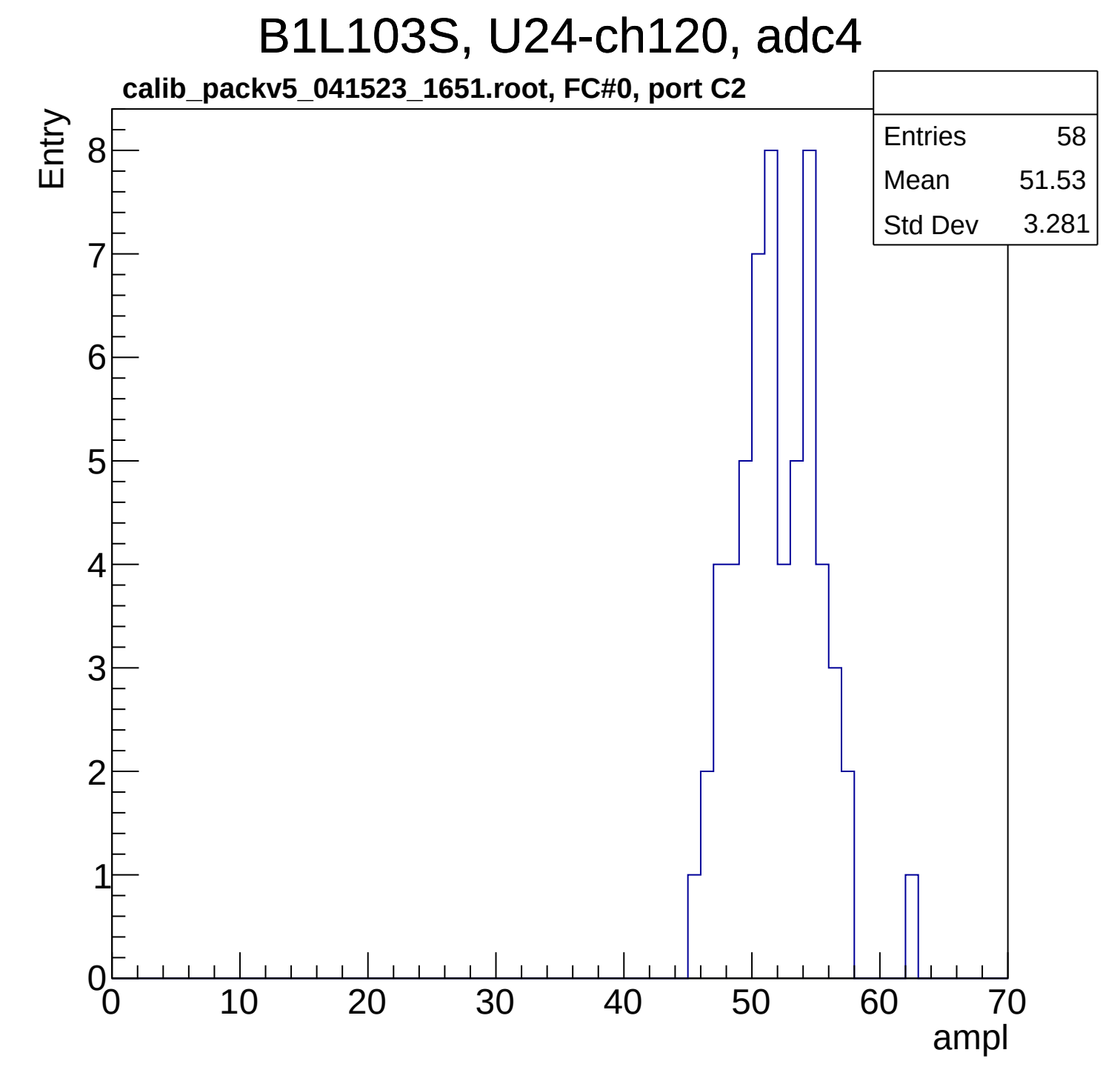
60
70


B1L103S, U24-ch120, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 90
Mean 33.42
Std Dev 14.82
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch120, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 43.93
Std Dev 9.146
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U24-ch120, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 51.53
Std Dev 3.281
Entry
ampl
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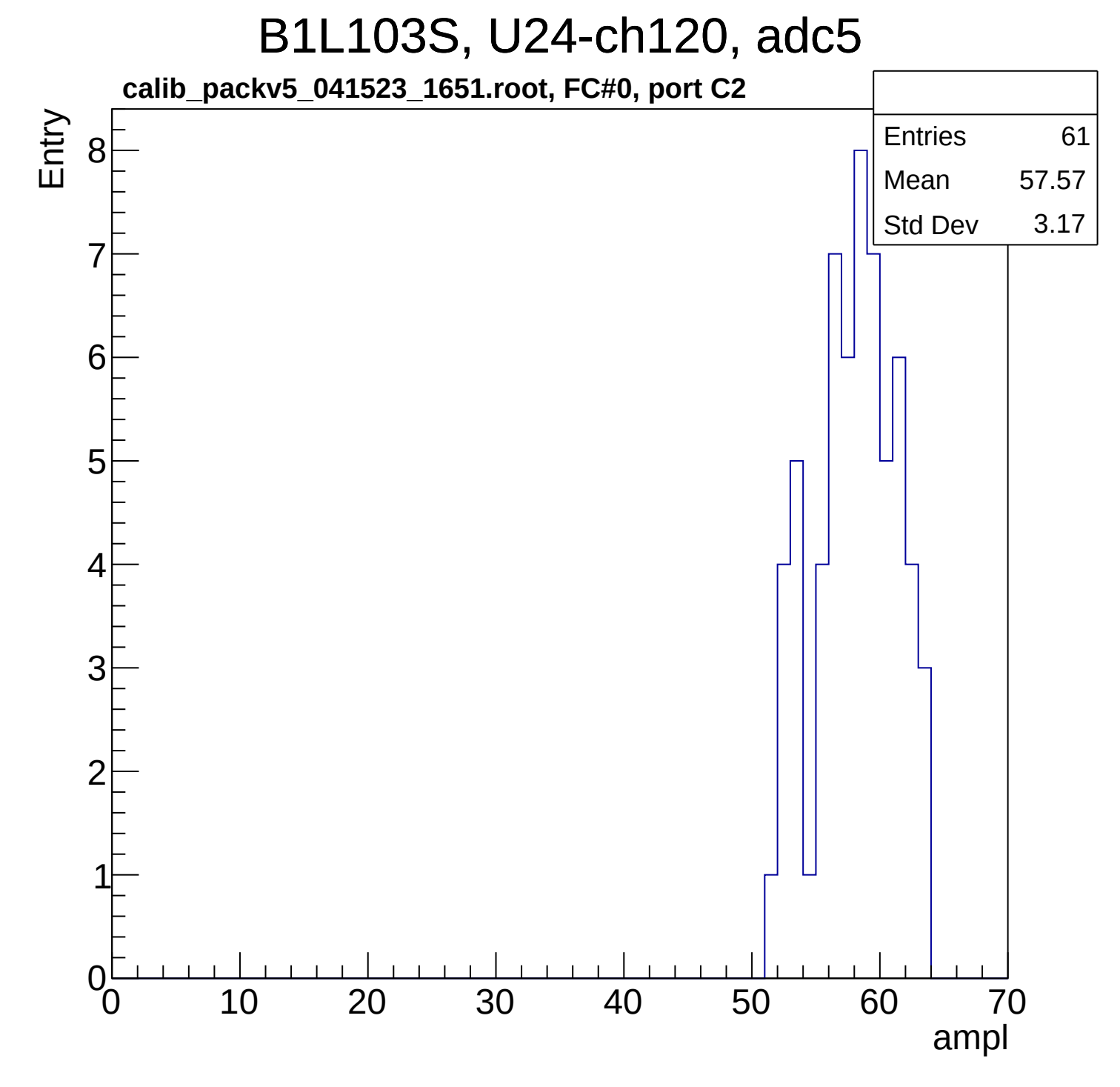
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U24-ch120, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 57.57
Std Dev 3.17
Entry
ampl
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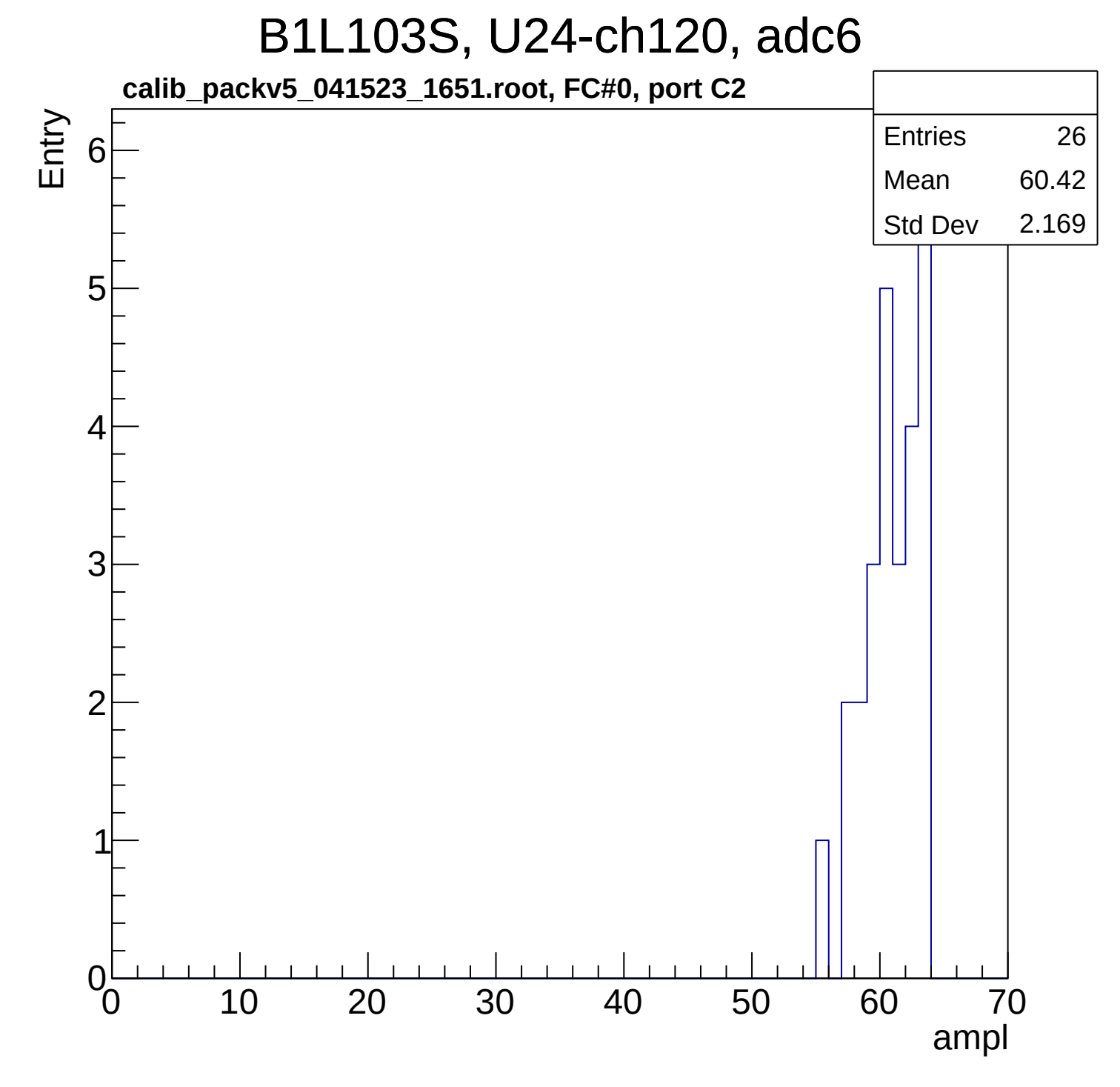
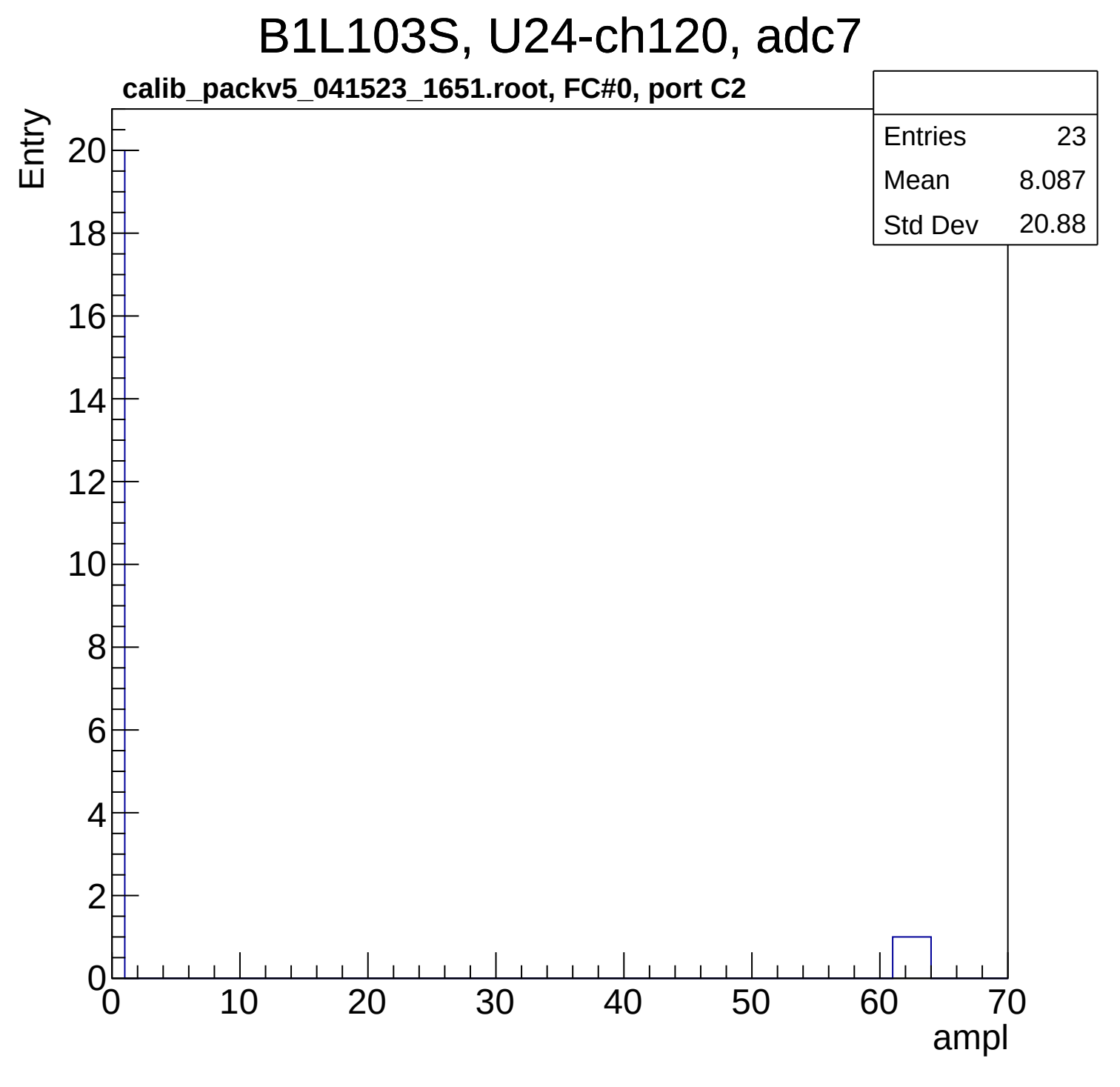
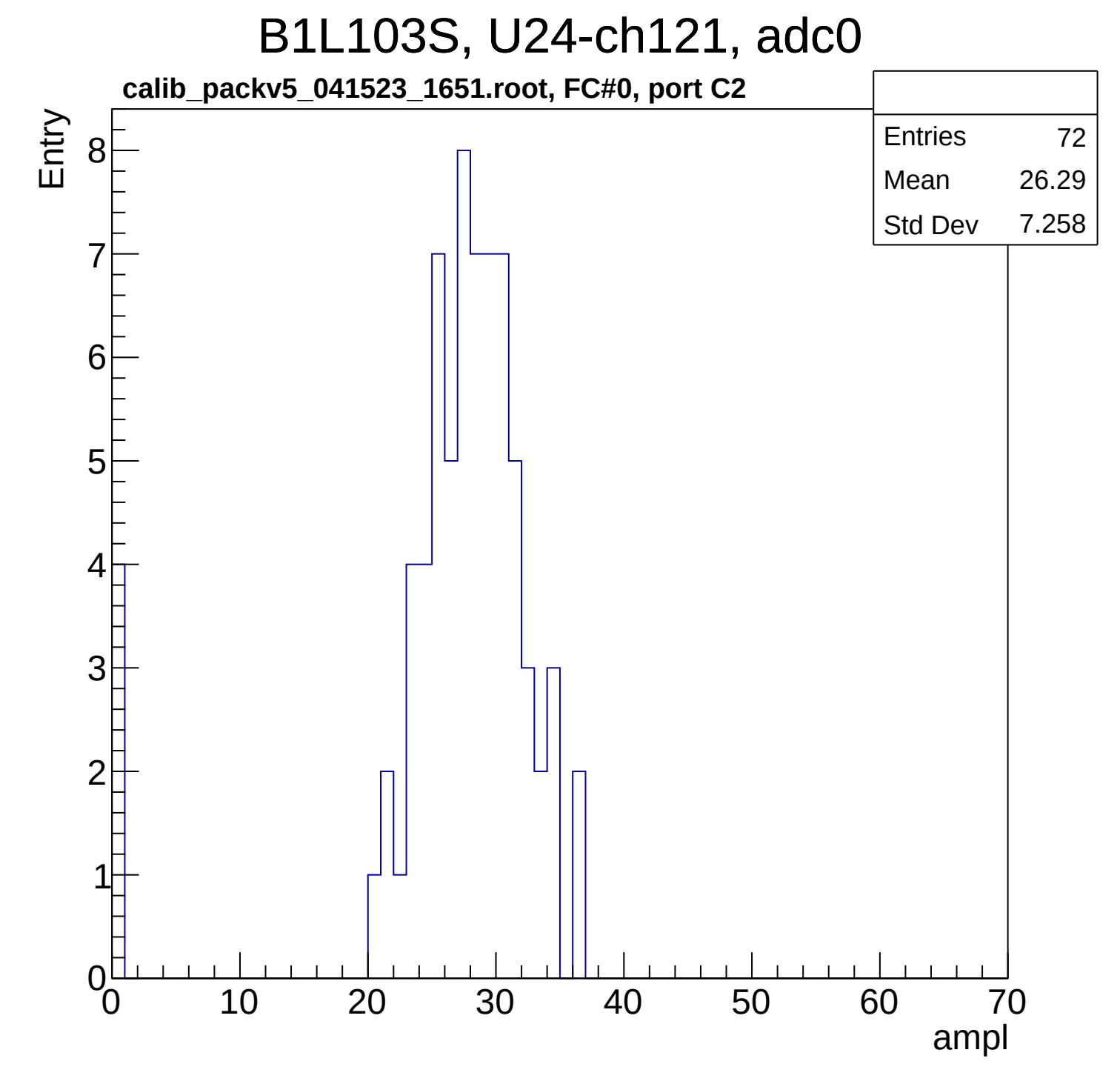
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U24-ch120, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 26
Mean 60.42
Std Dev 2.169
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U24-ch120, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 23
Mean 8.087
Std Dev 20.88
Entry
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch121, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 26.29
Std Dev 7.258
Entry
ampl
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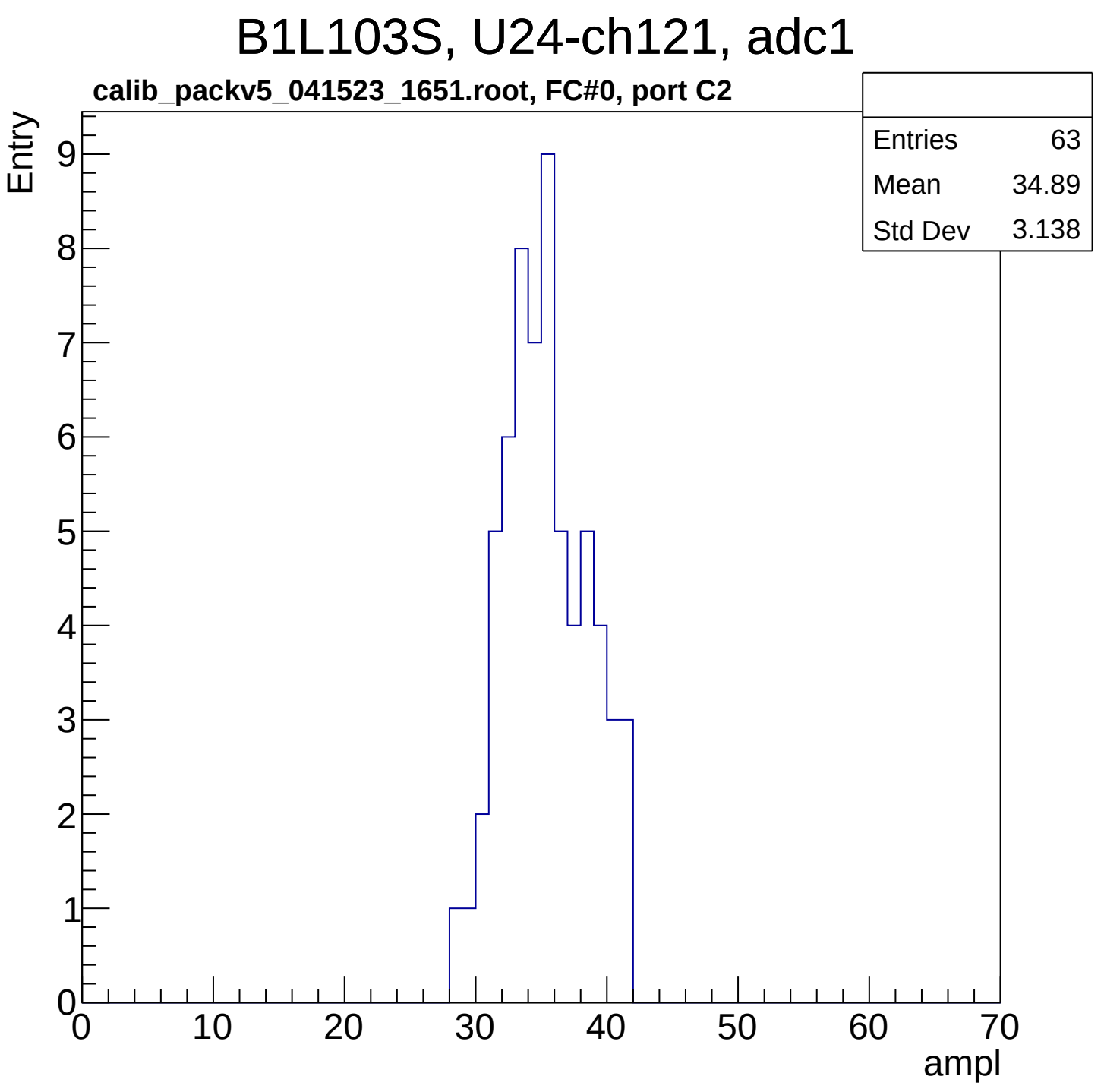
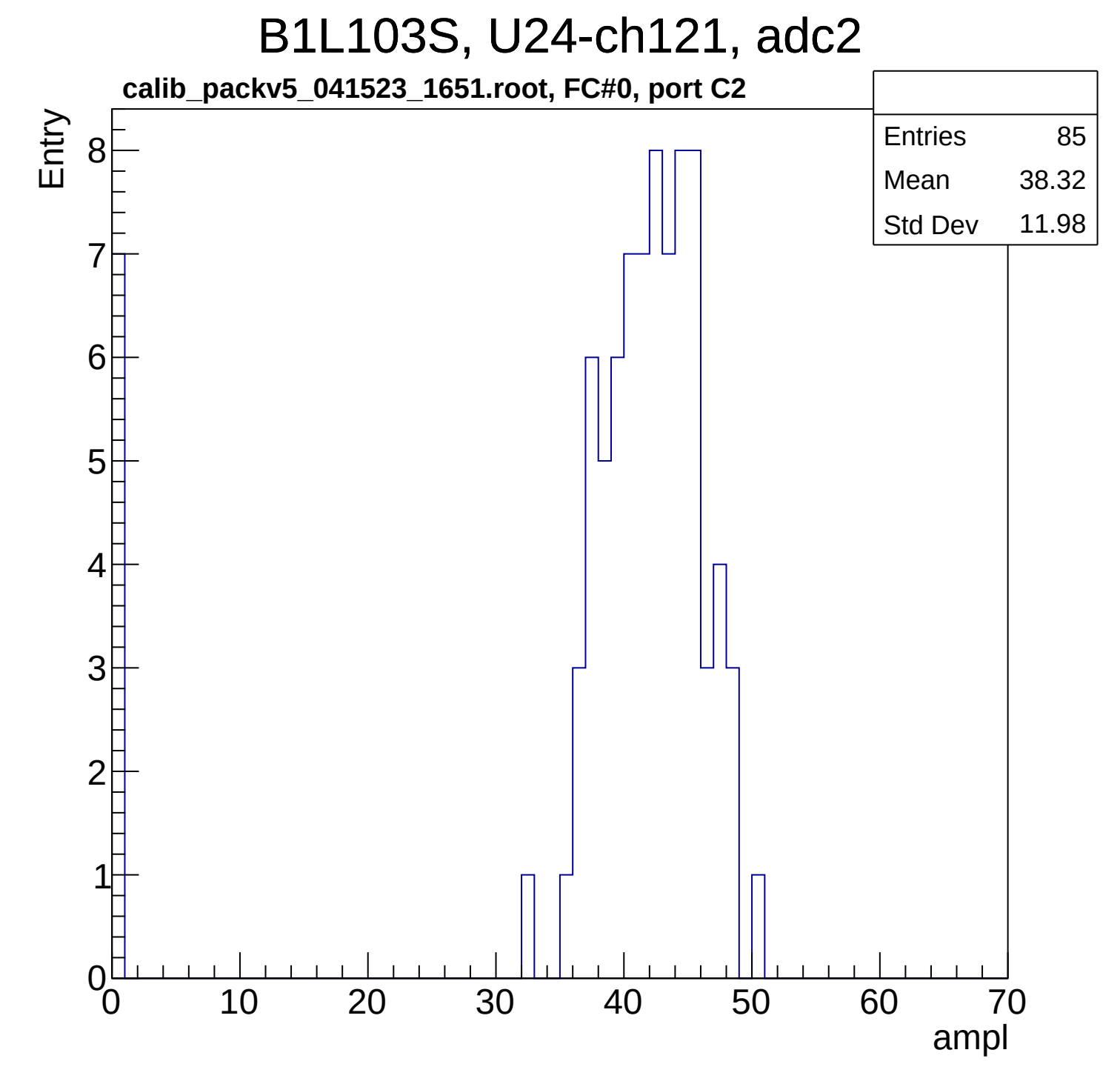
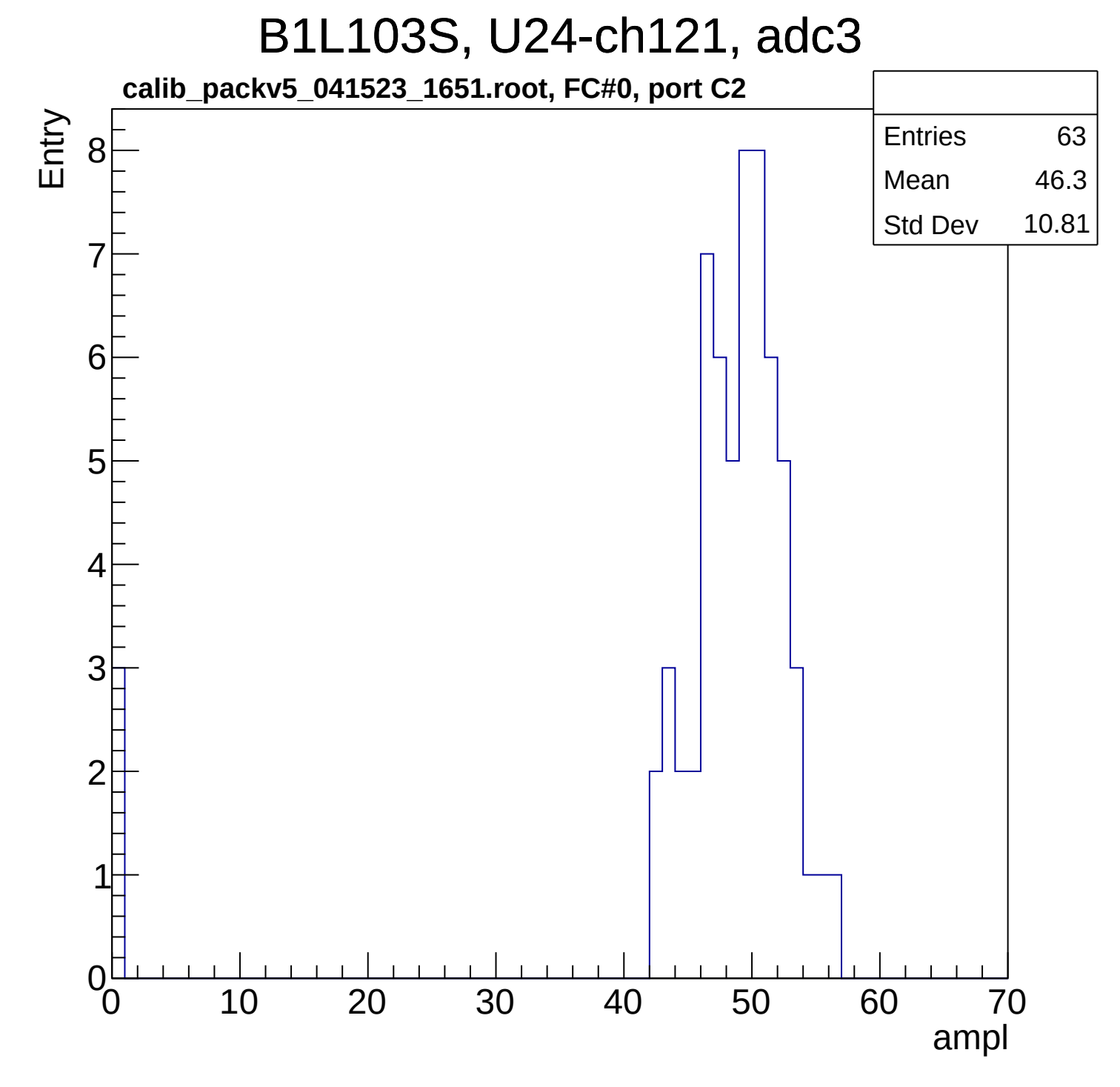
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U24-ch121, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 34.89
Std Dev 3.138
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U24-ch121, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 38.32
Std Dev 11.98
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U24-ch121, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 46.3
Std Dev 10.81
Entry
ampl
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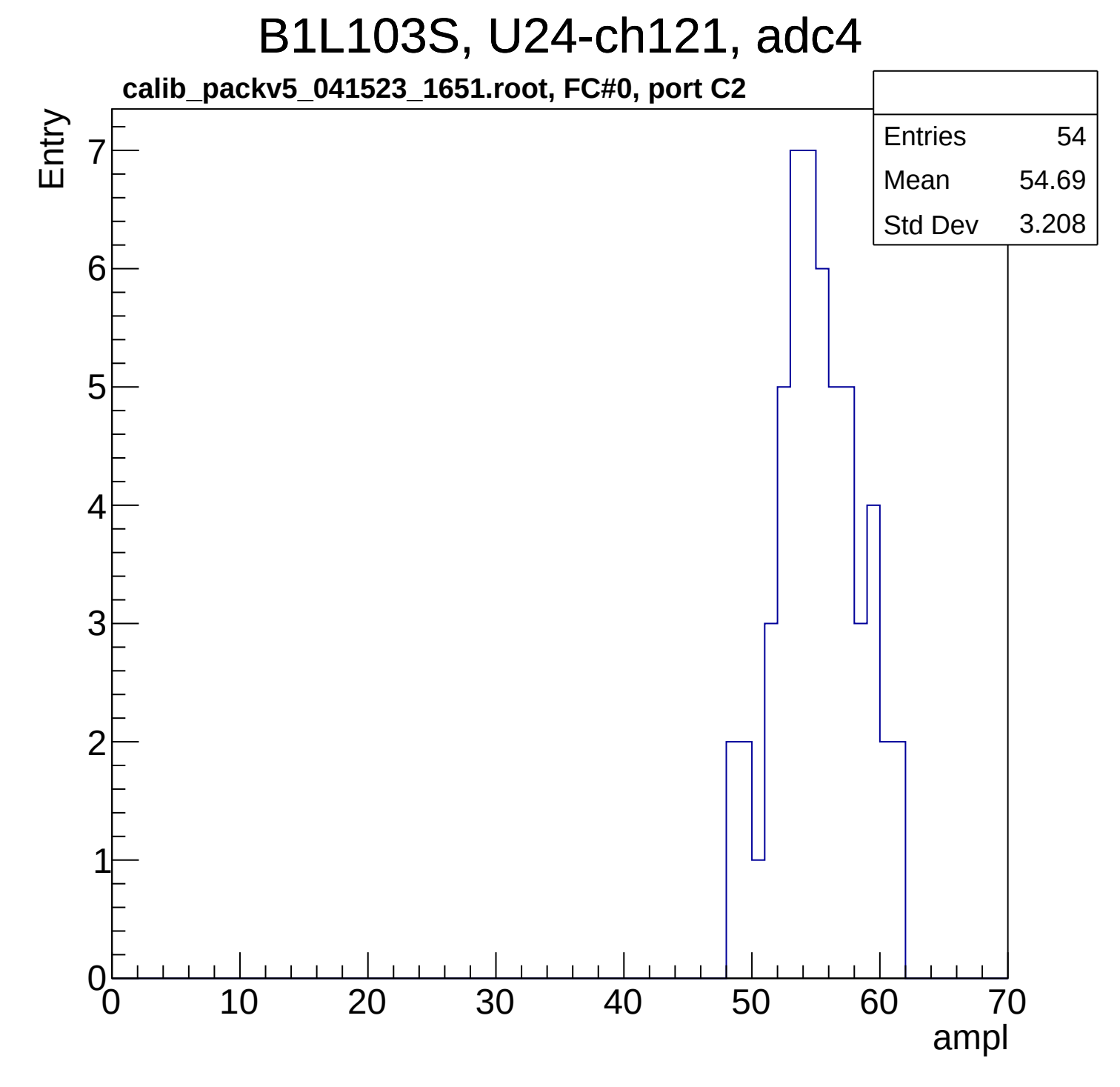
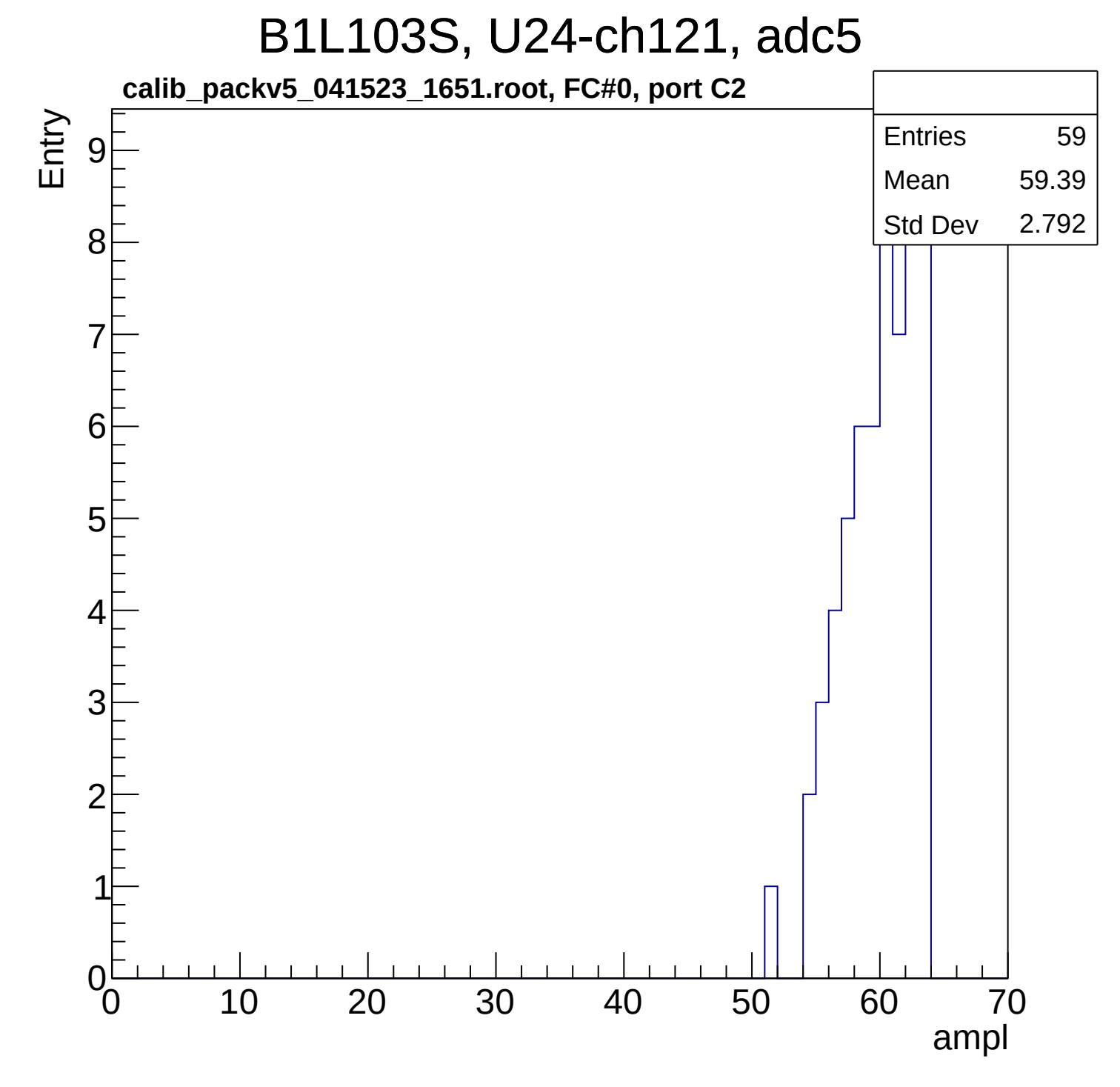
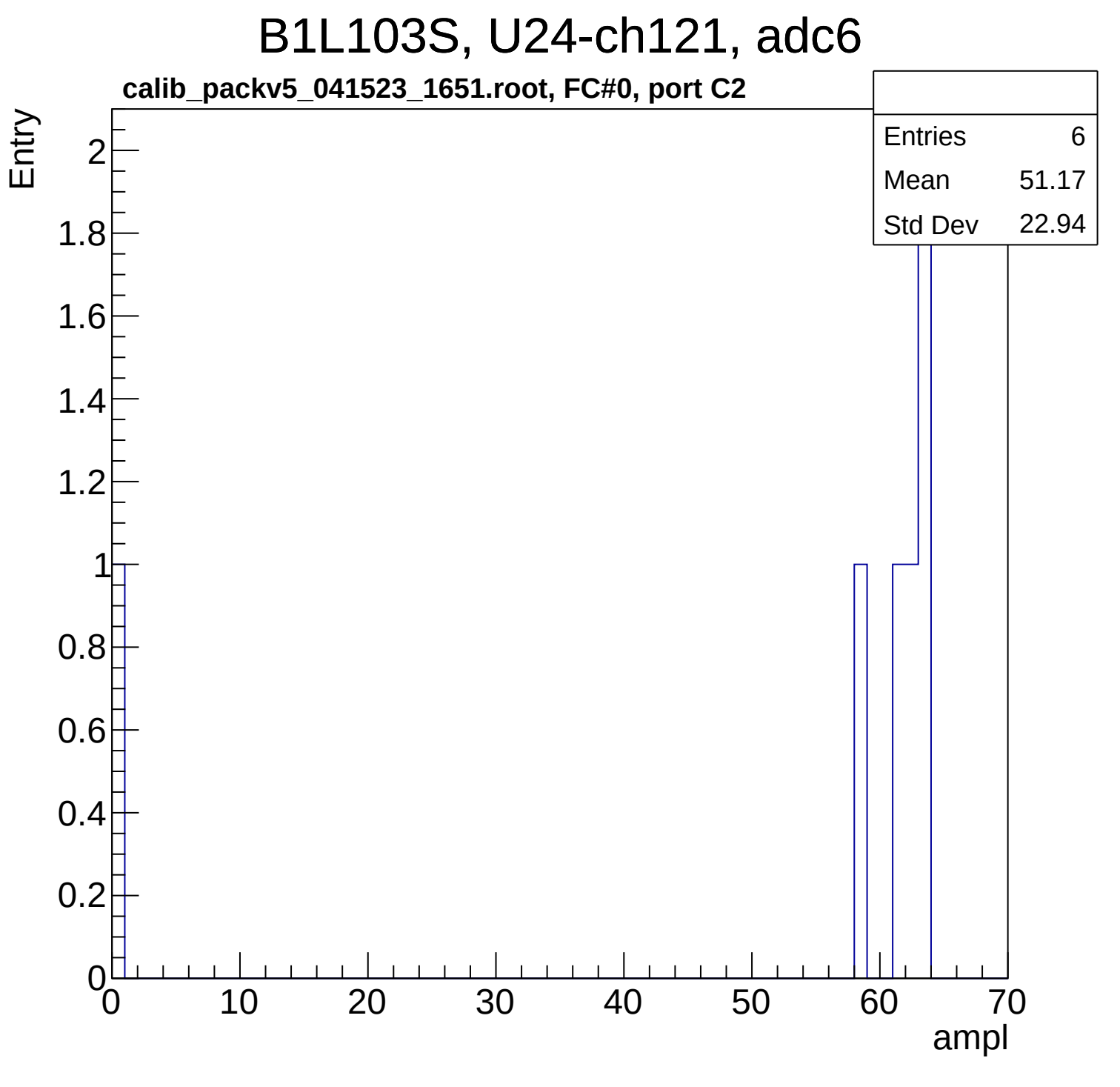
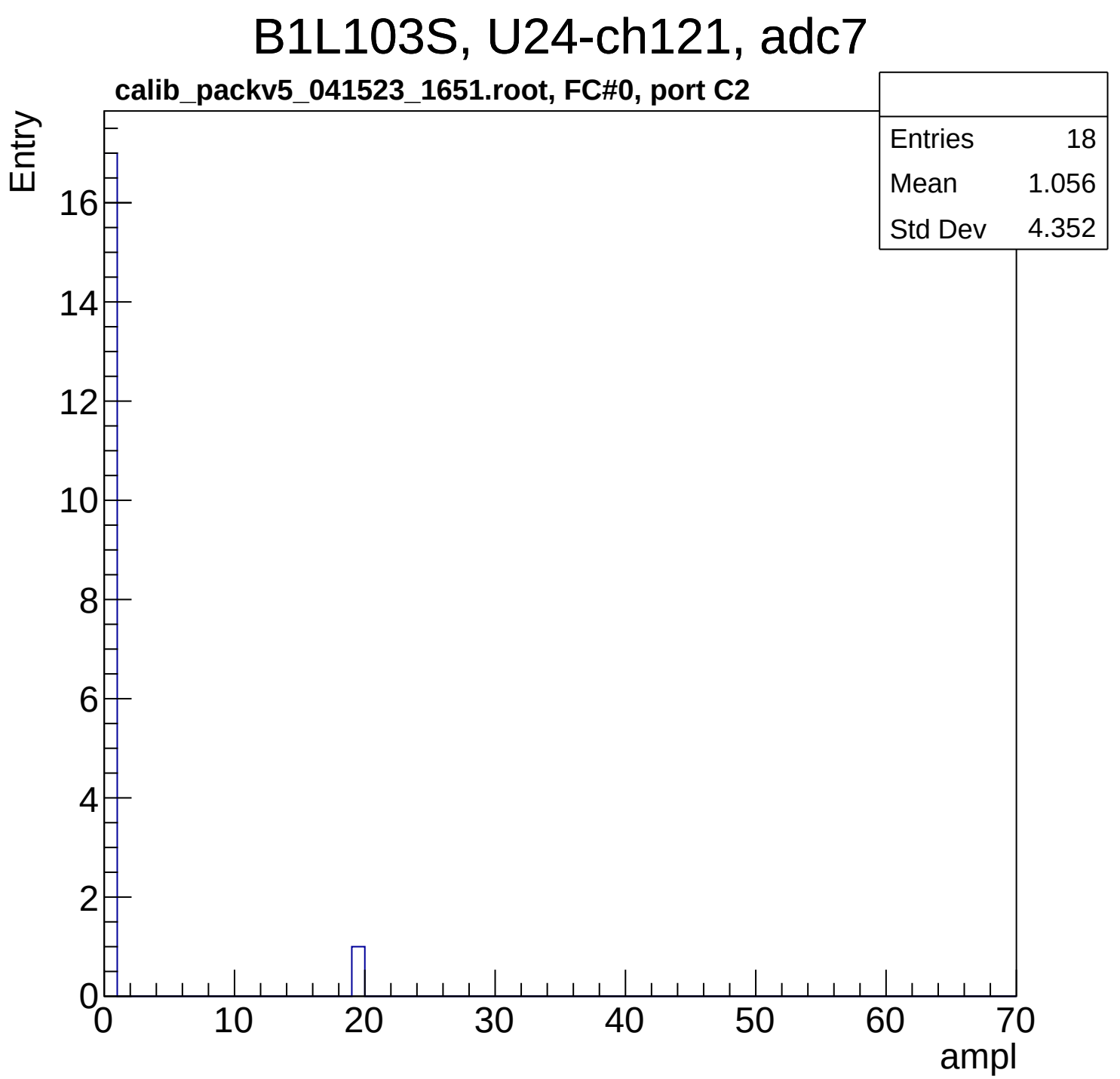
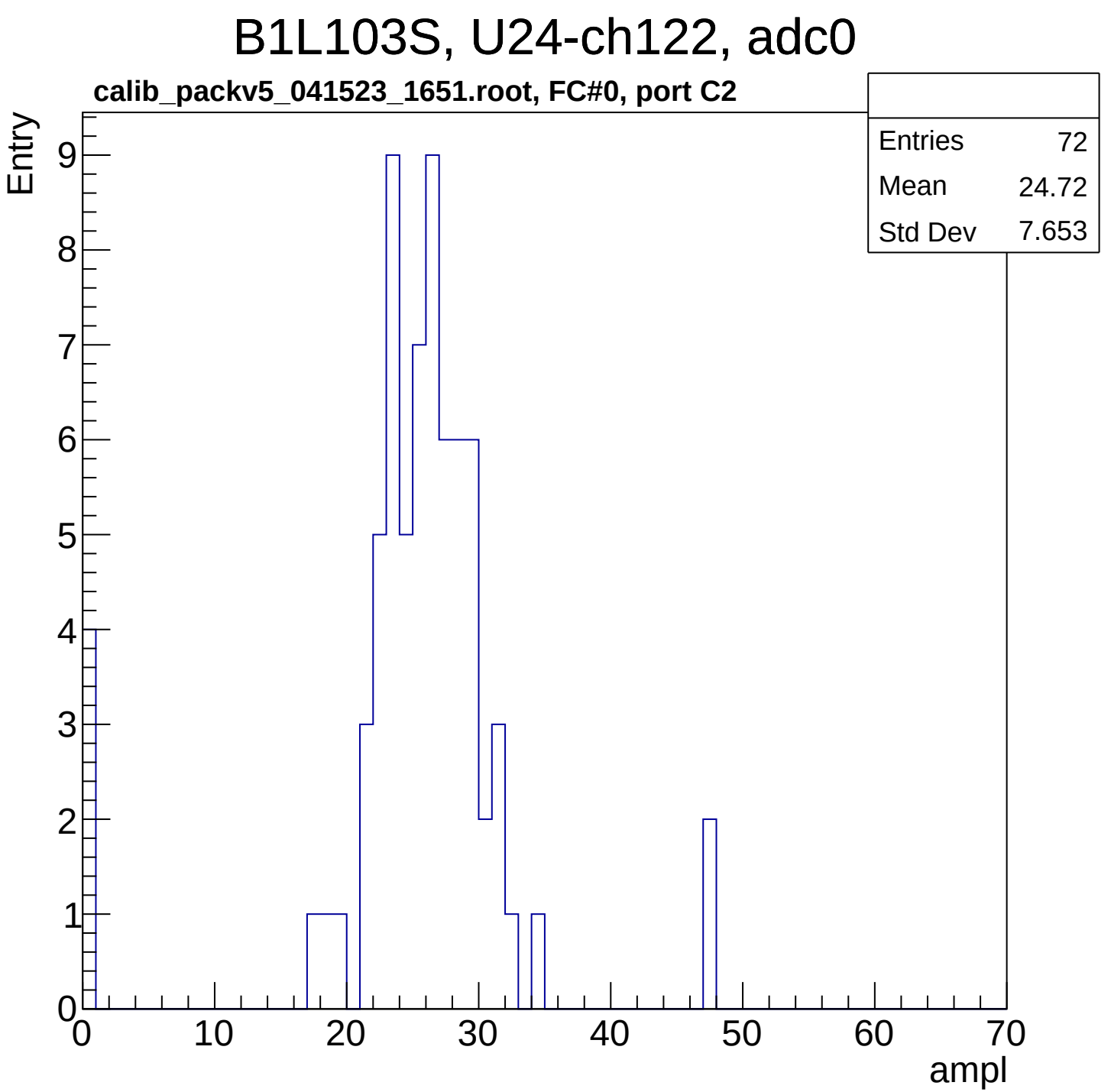
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

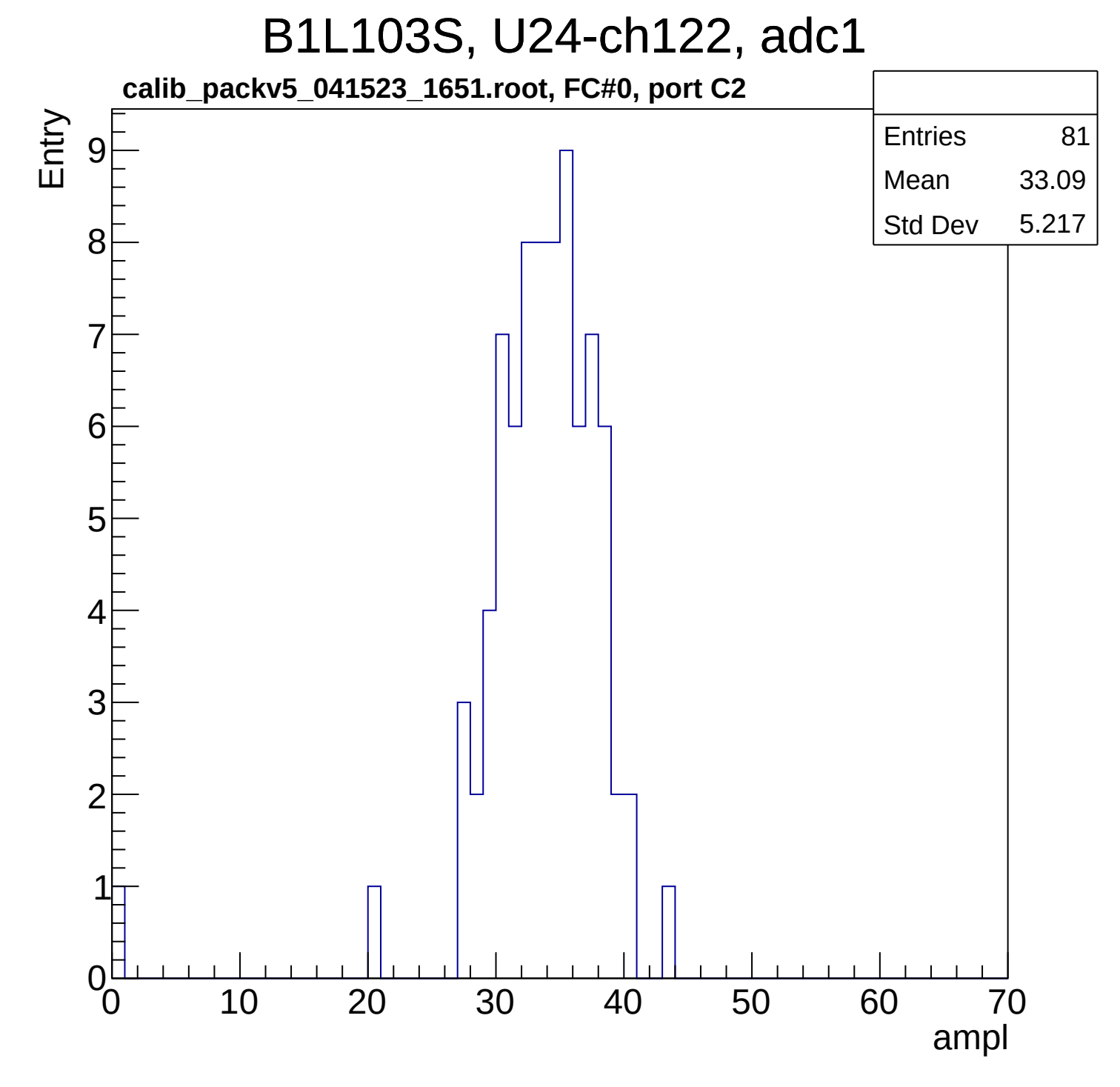

B1L103S, U24-ch121, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 54.69
Std Dev 3.208
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U24-ch121, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 59.39
Std Dev 2.792
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U24-ch121, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 51.17
Std Dev 22.94
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U24-ch121, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 1.056
Std Dev 4.352
Entry
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch122, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 24.72
Std Dev 7.653
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U24-ch122, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 33.09
Std Dev 5.217
Entry
ampl
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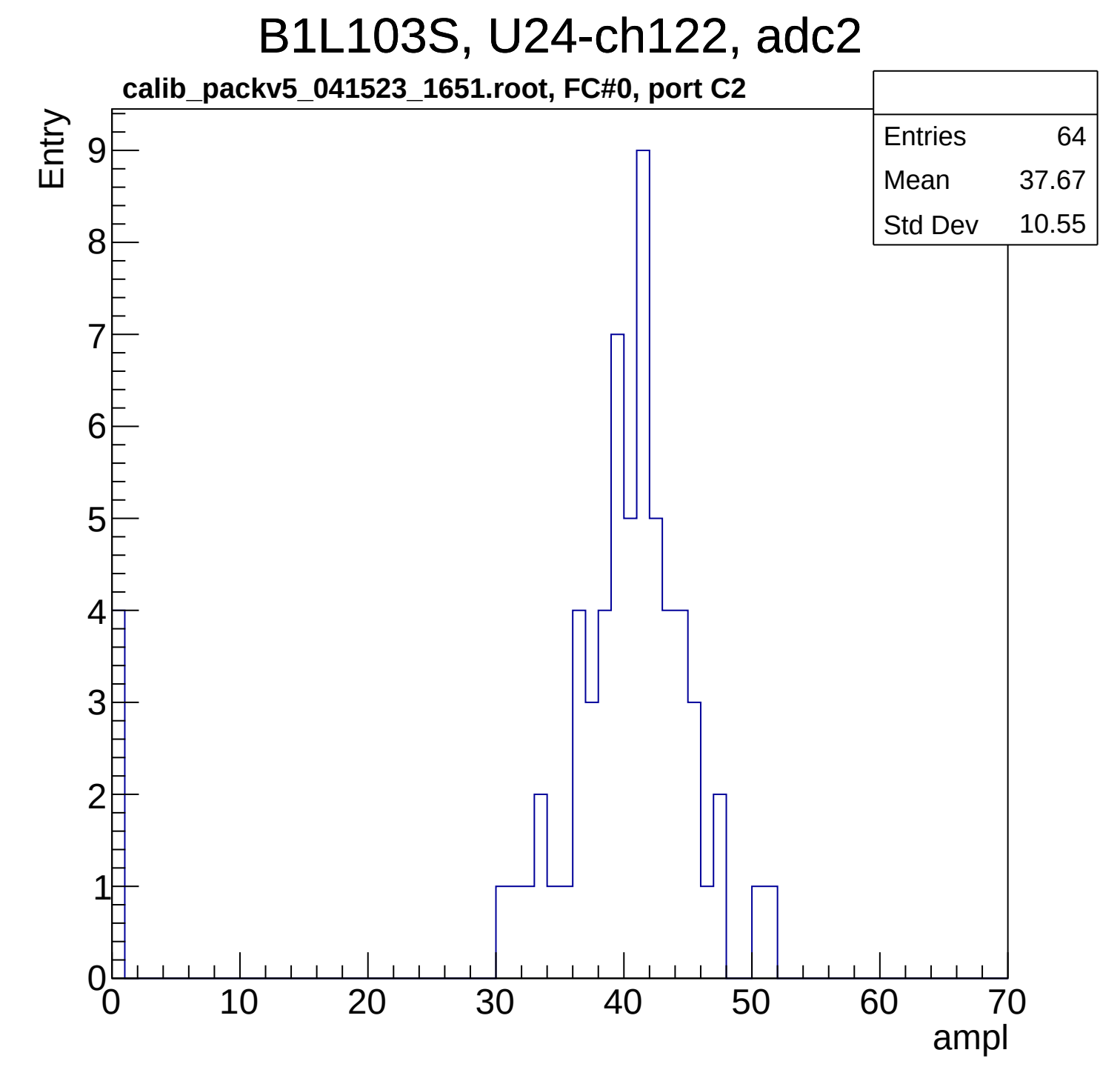
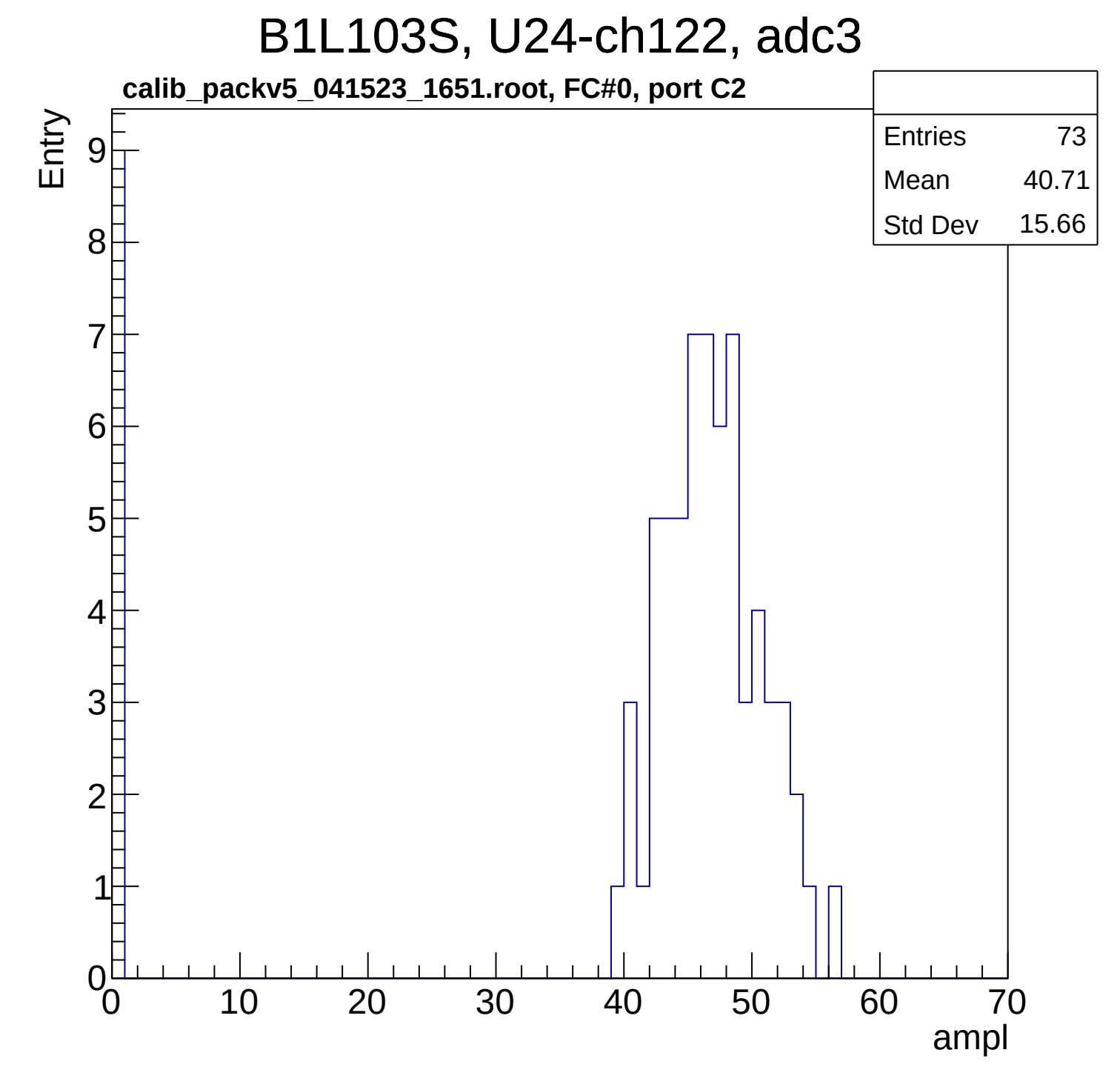
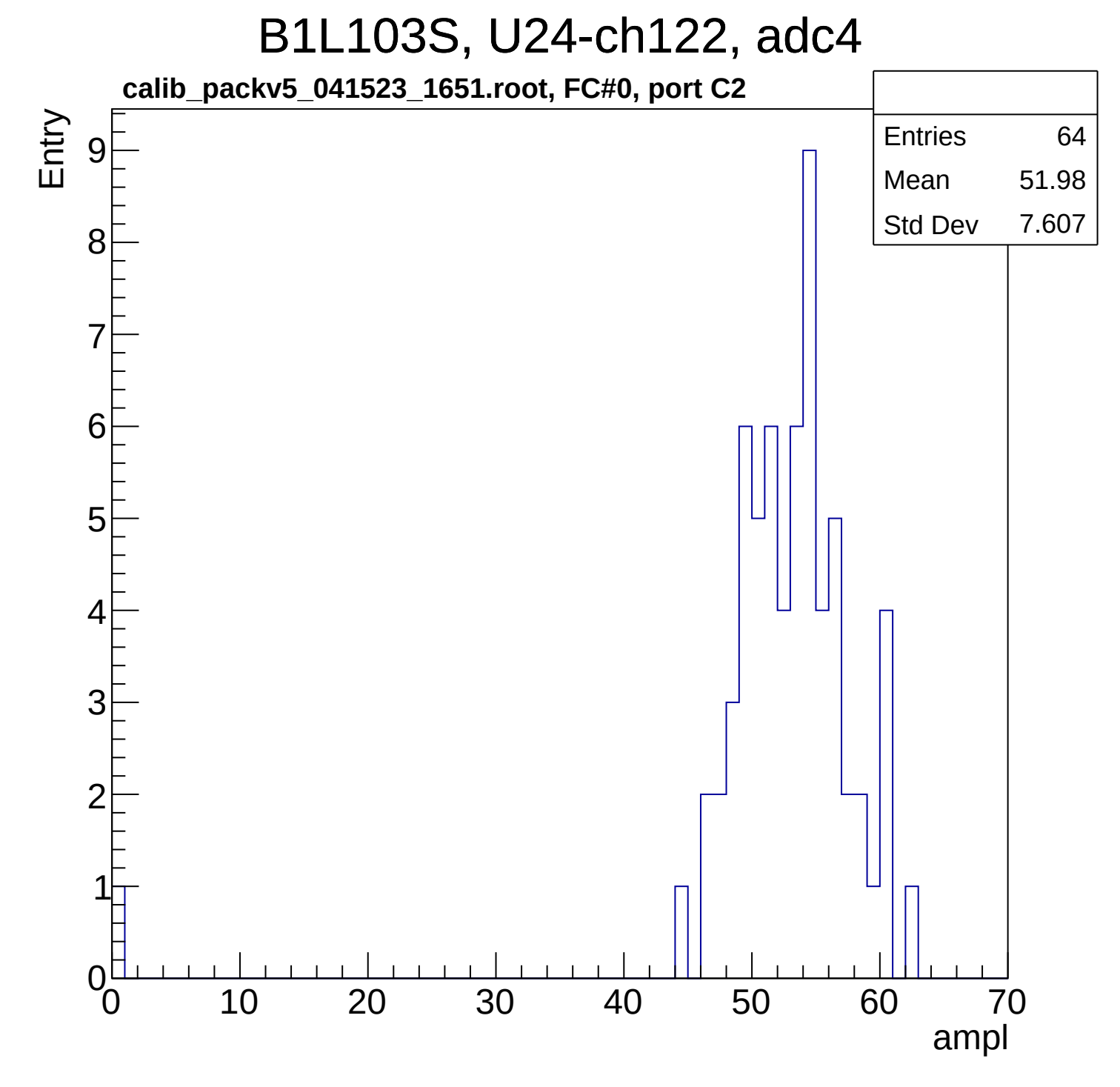
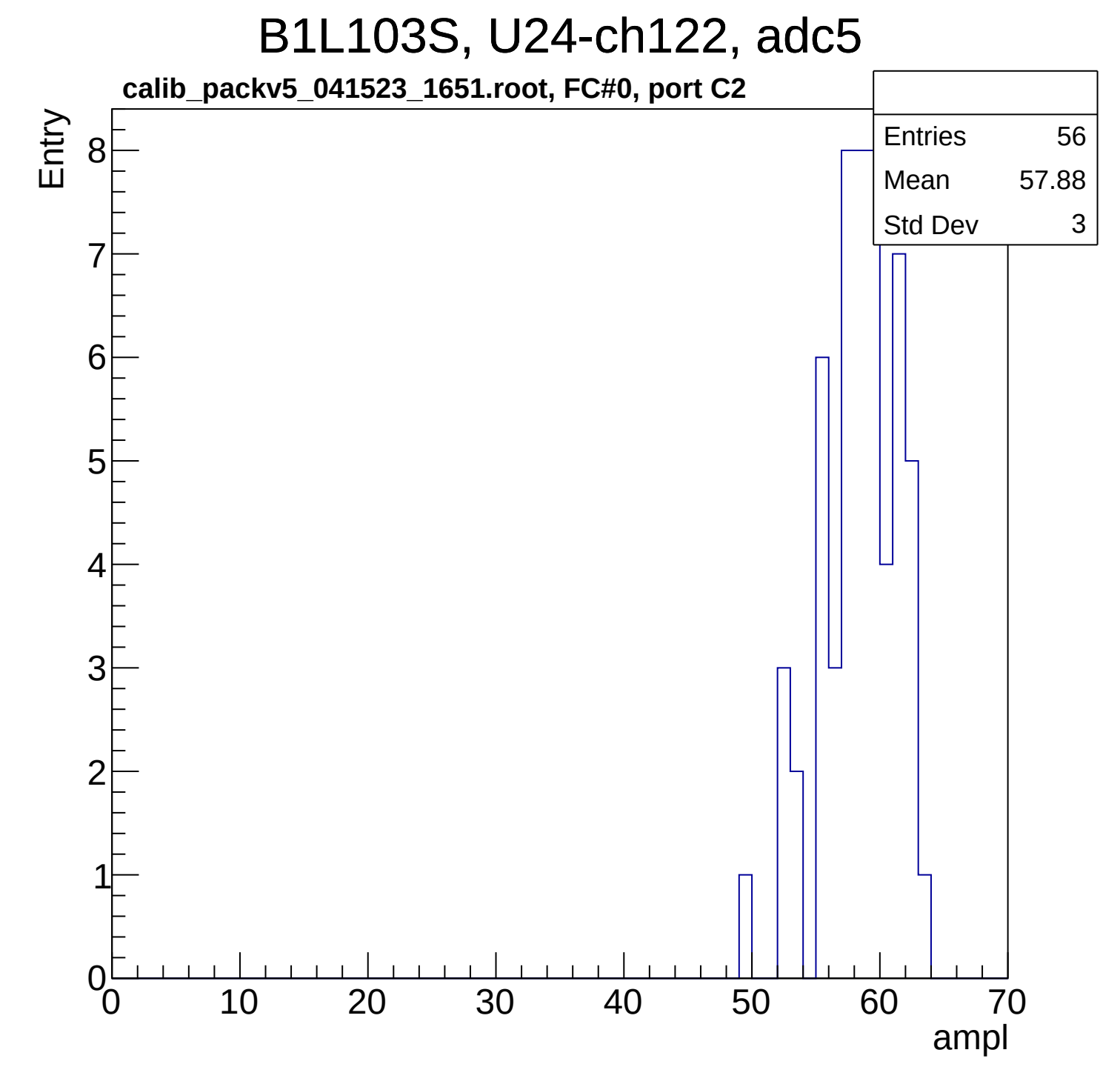
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U24-ch122, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 37.67
Std Dev 10.55
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U24-ch122, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 40.71
Std Dev 15.66
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U24-ch122, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 51.98
Std Dev 7.607
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U24-ch122, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 57.88
Std Dev 3
Entry
ampl
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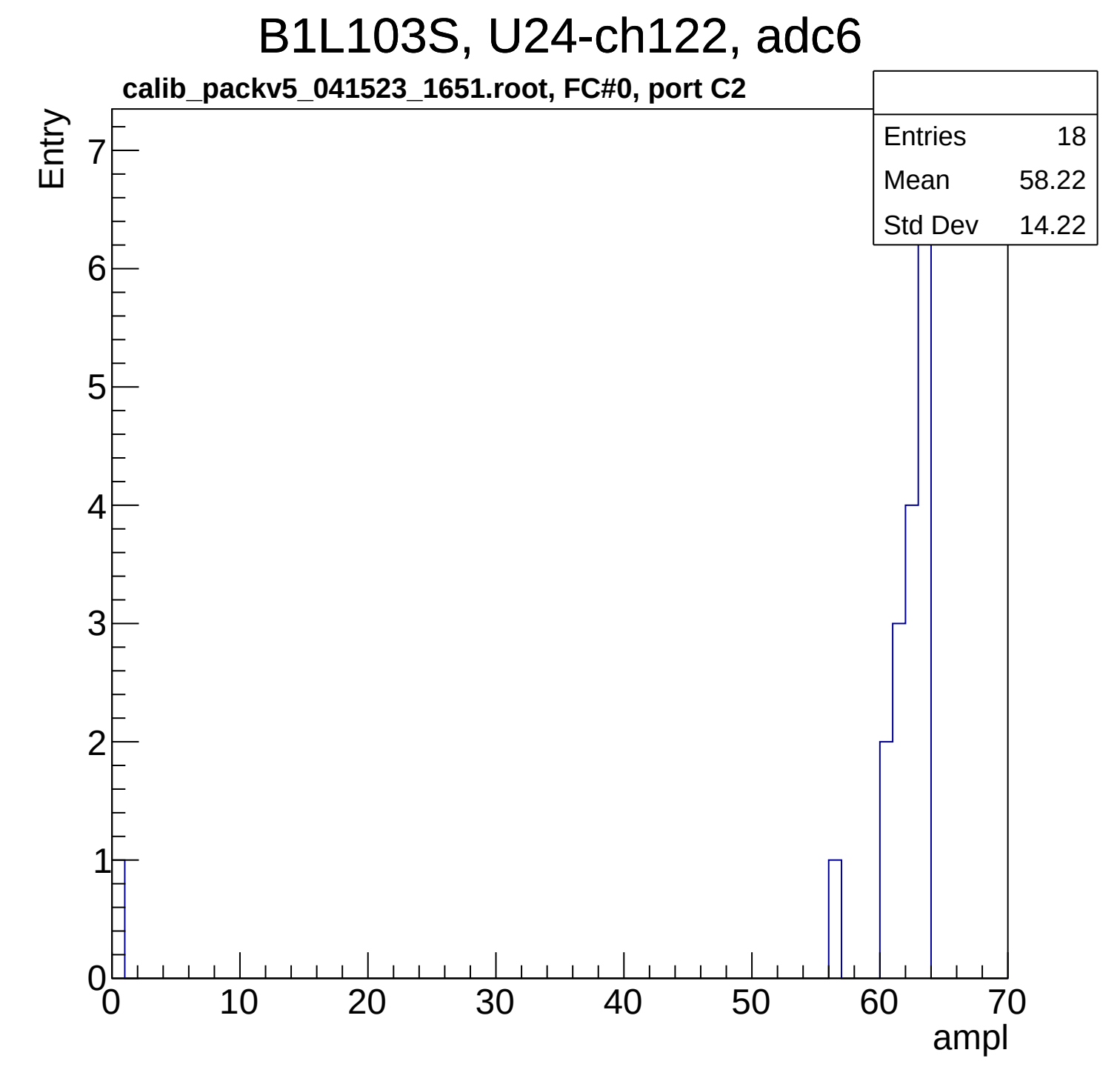
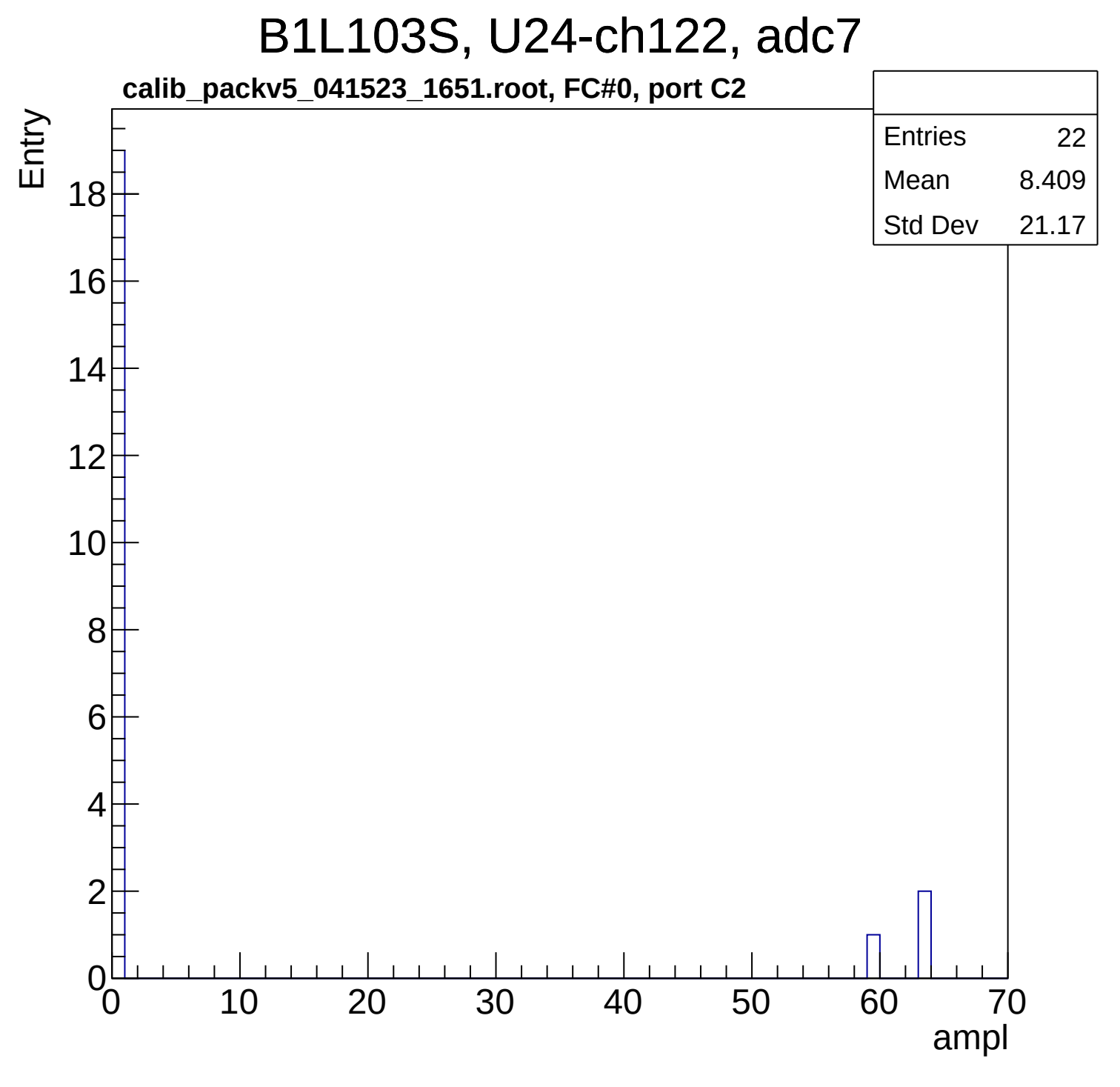
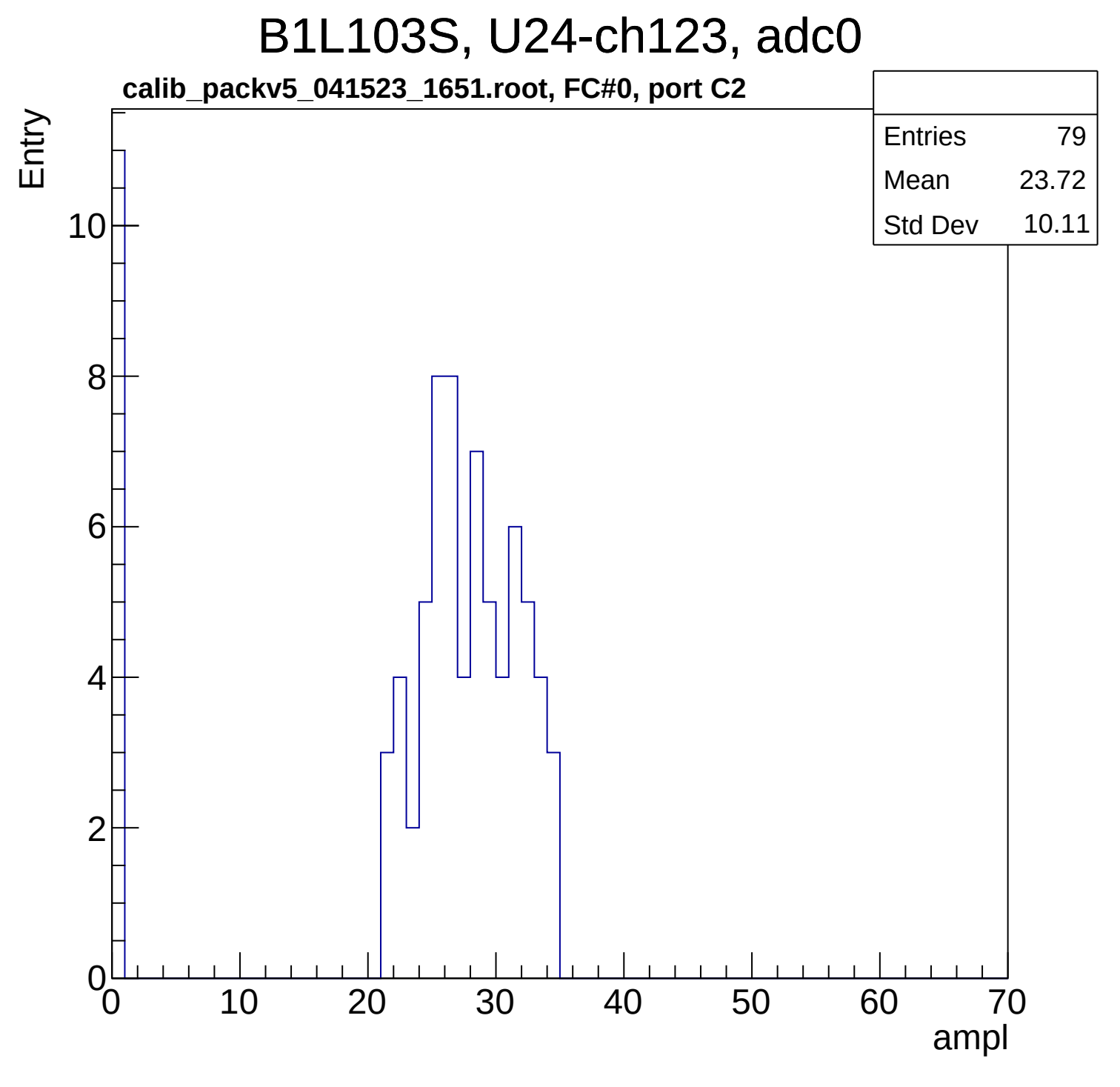
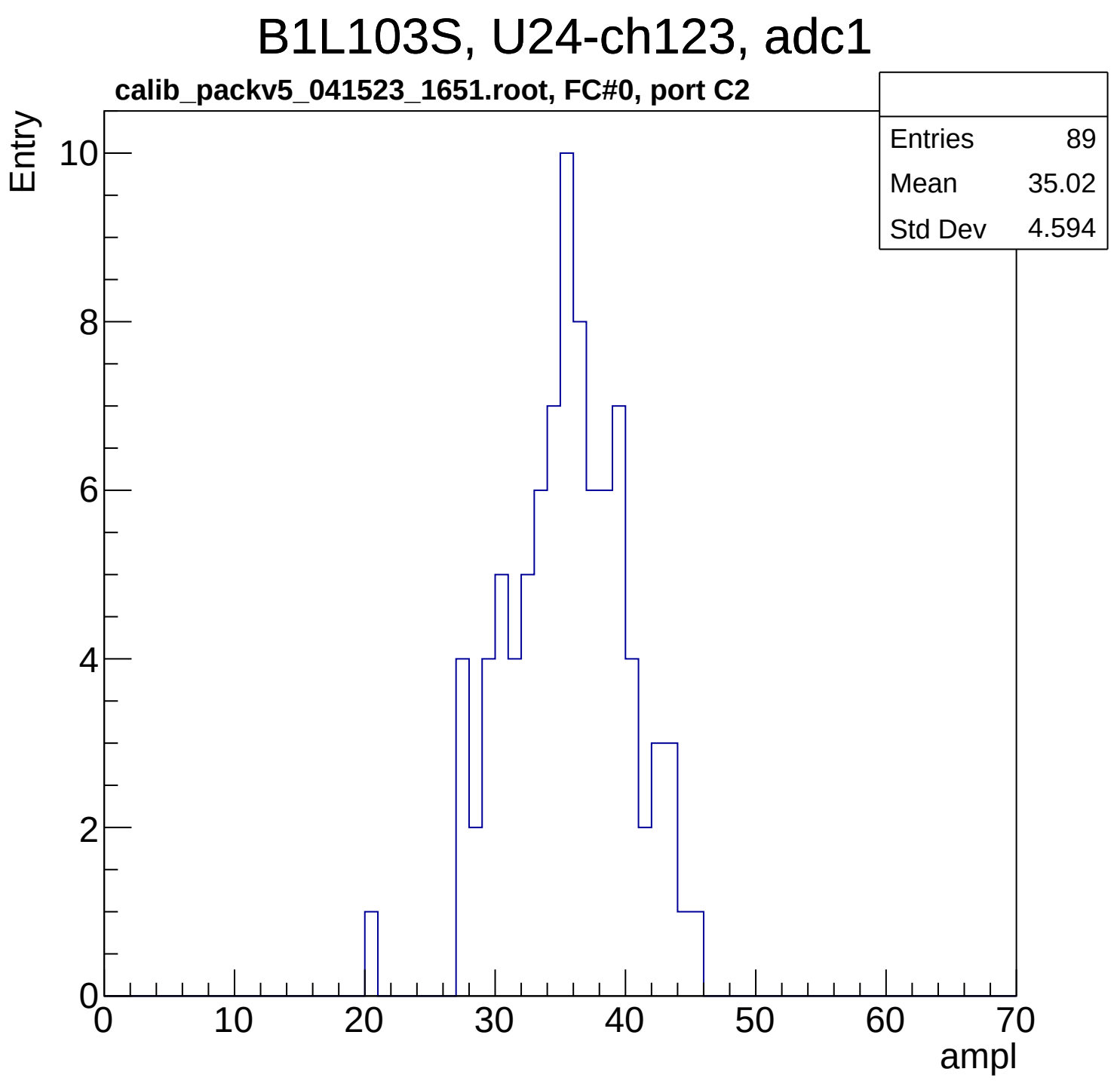
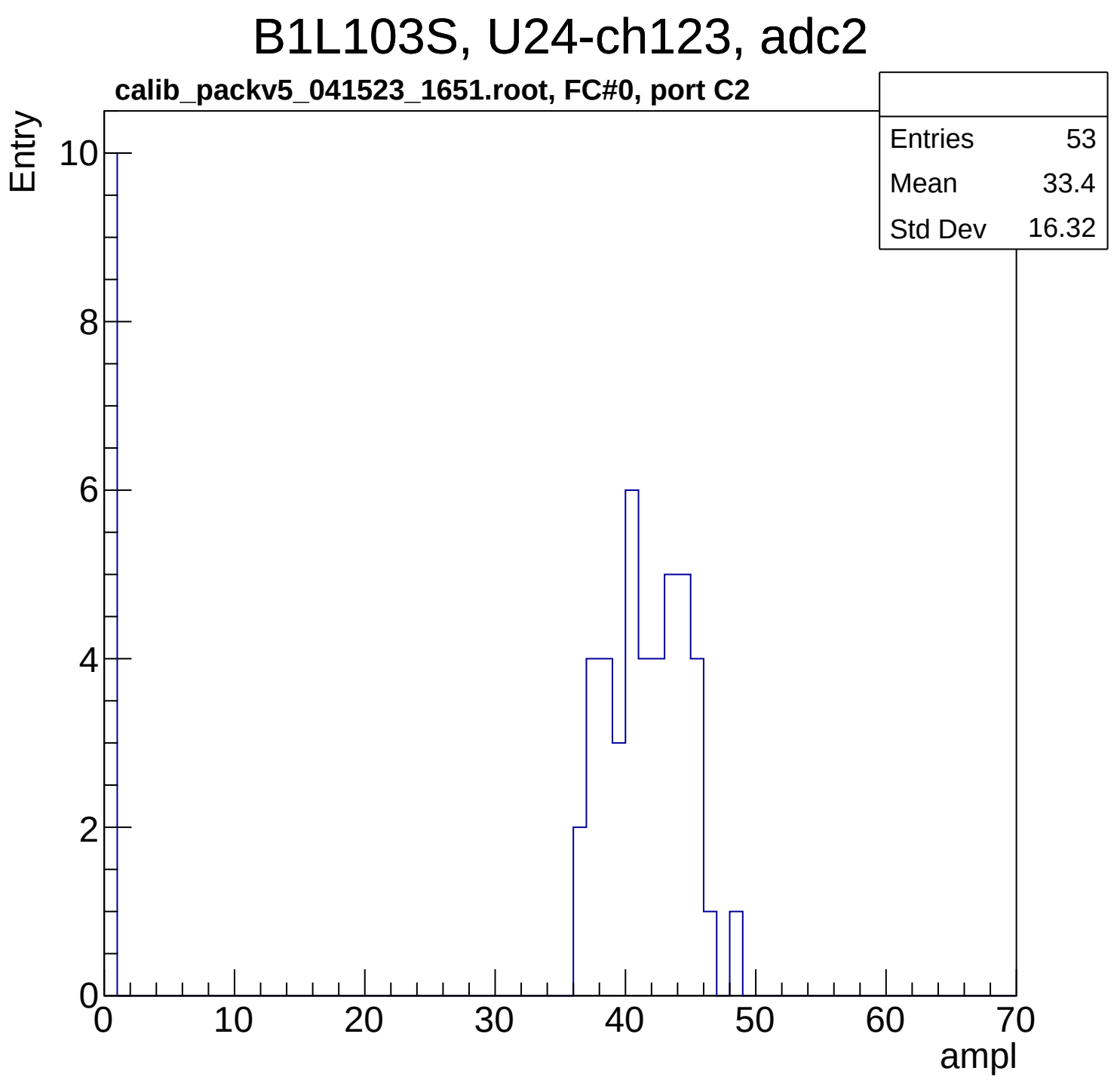
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

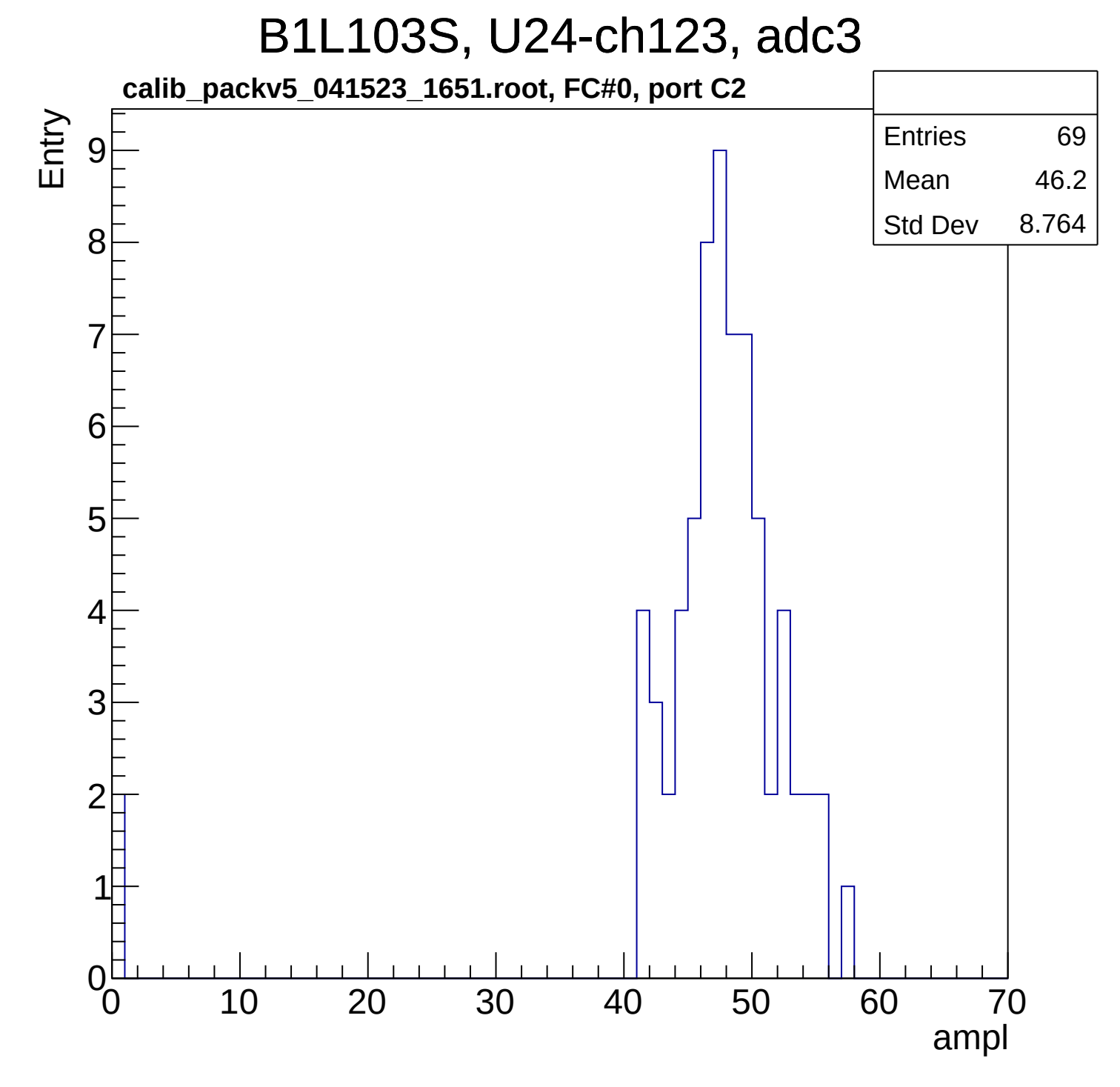

B1L103S, U24-ch122, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 58.22
Std Dev 14.22
Entry
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch122, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 8.409
Std Dev 21.17
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch123, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 23.72
Std Dev 10.11
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch123, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 89
Mean 35.02
Std Dev 4.594
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U24-ch123, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 33.4
Std Dev 16.32
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U24-ch123, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 46.2
Std Dev 8.764
Entry
ampl
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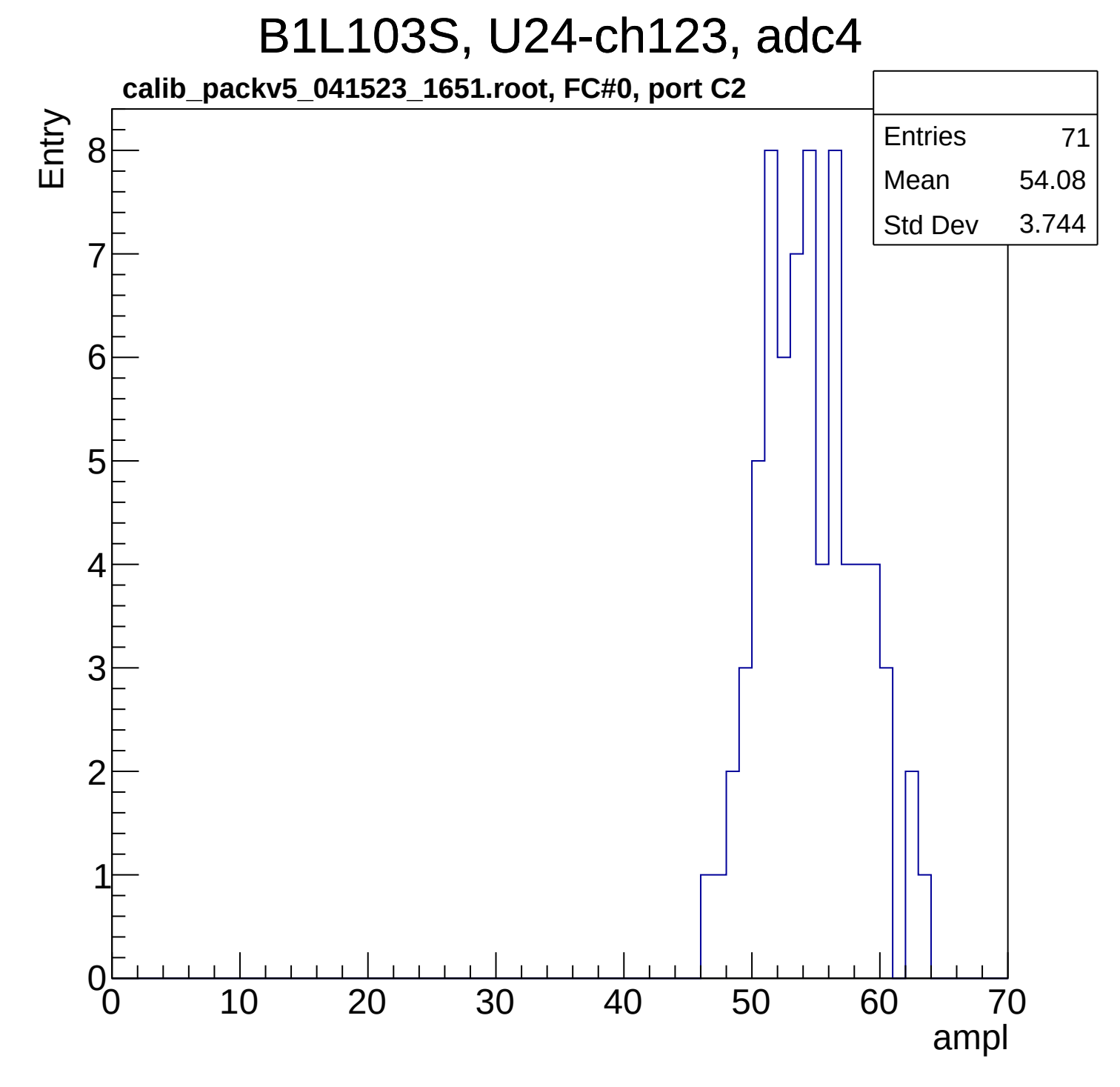
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U24-ch123, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 54.08
Std Dev 3.744
Entry
ampl
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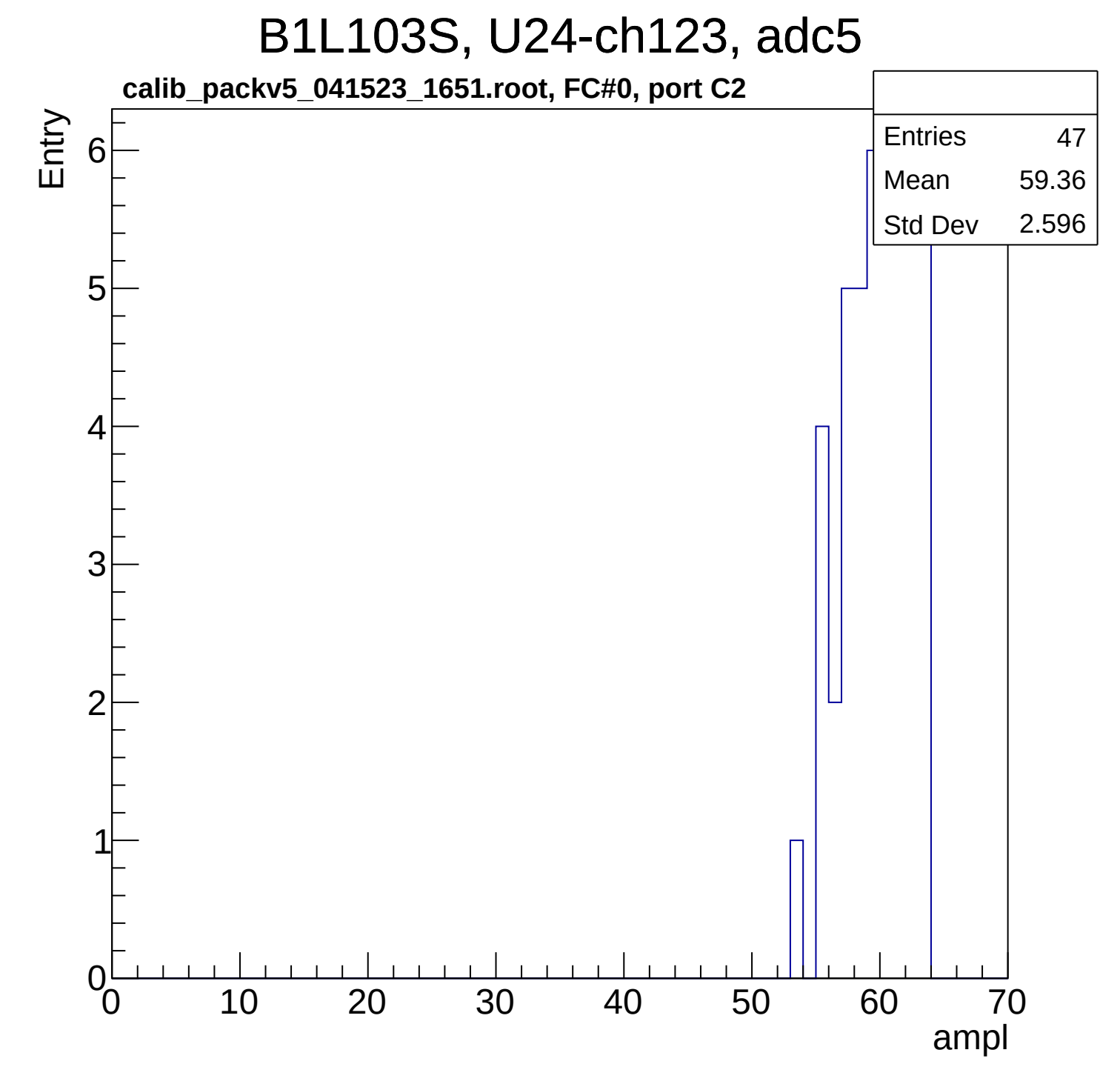
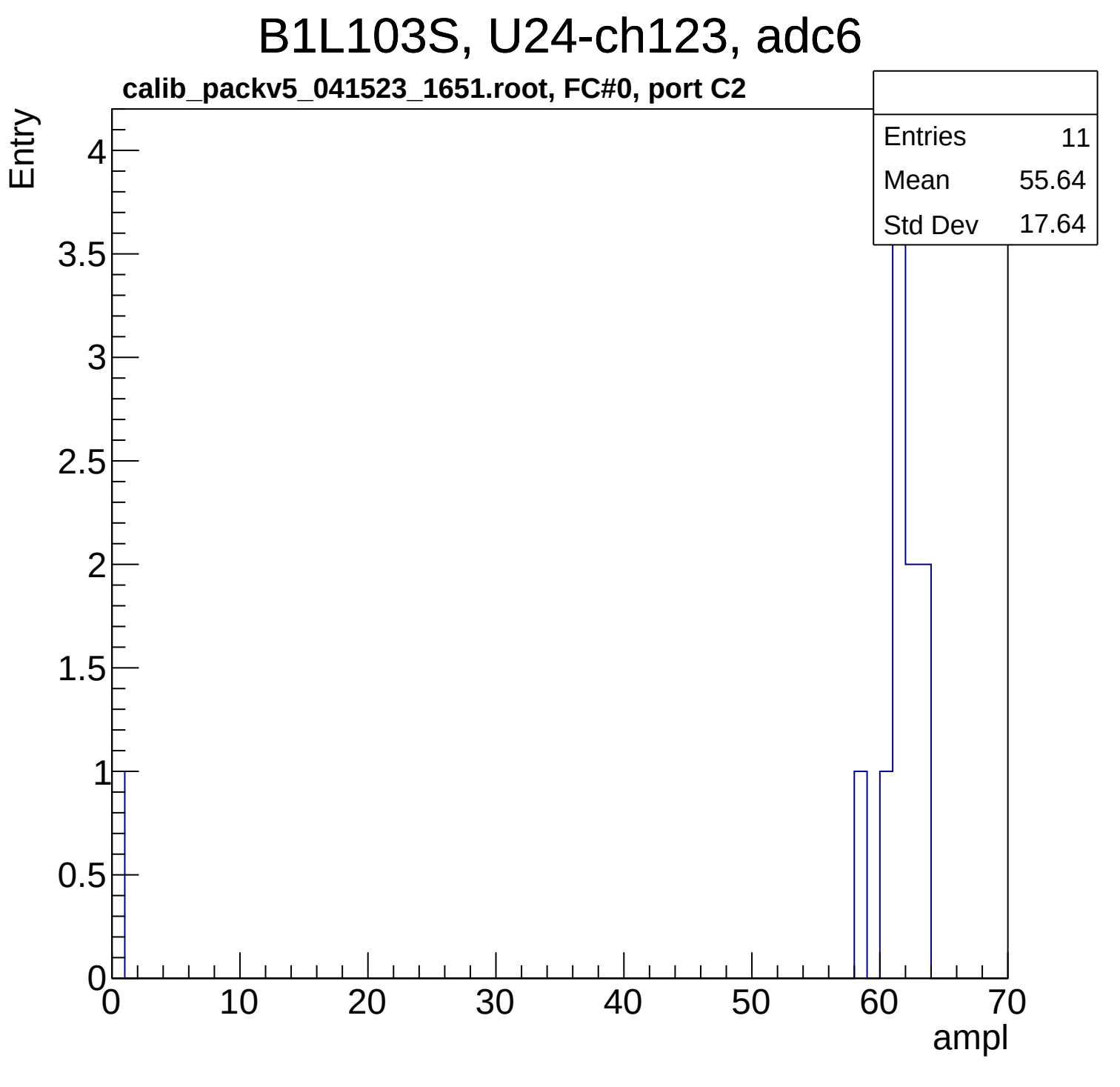
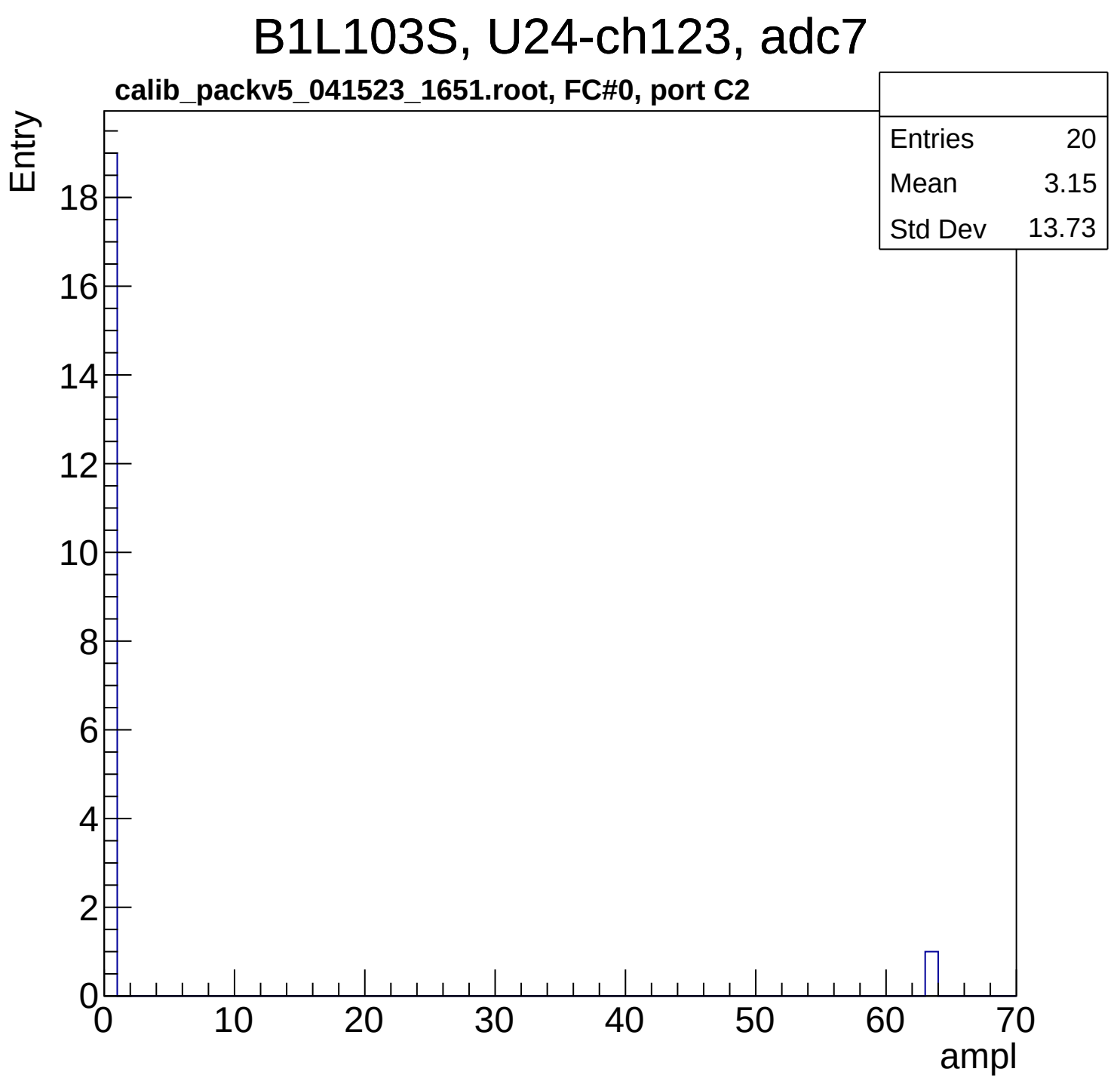
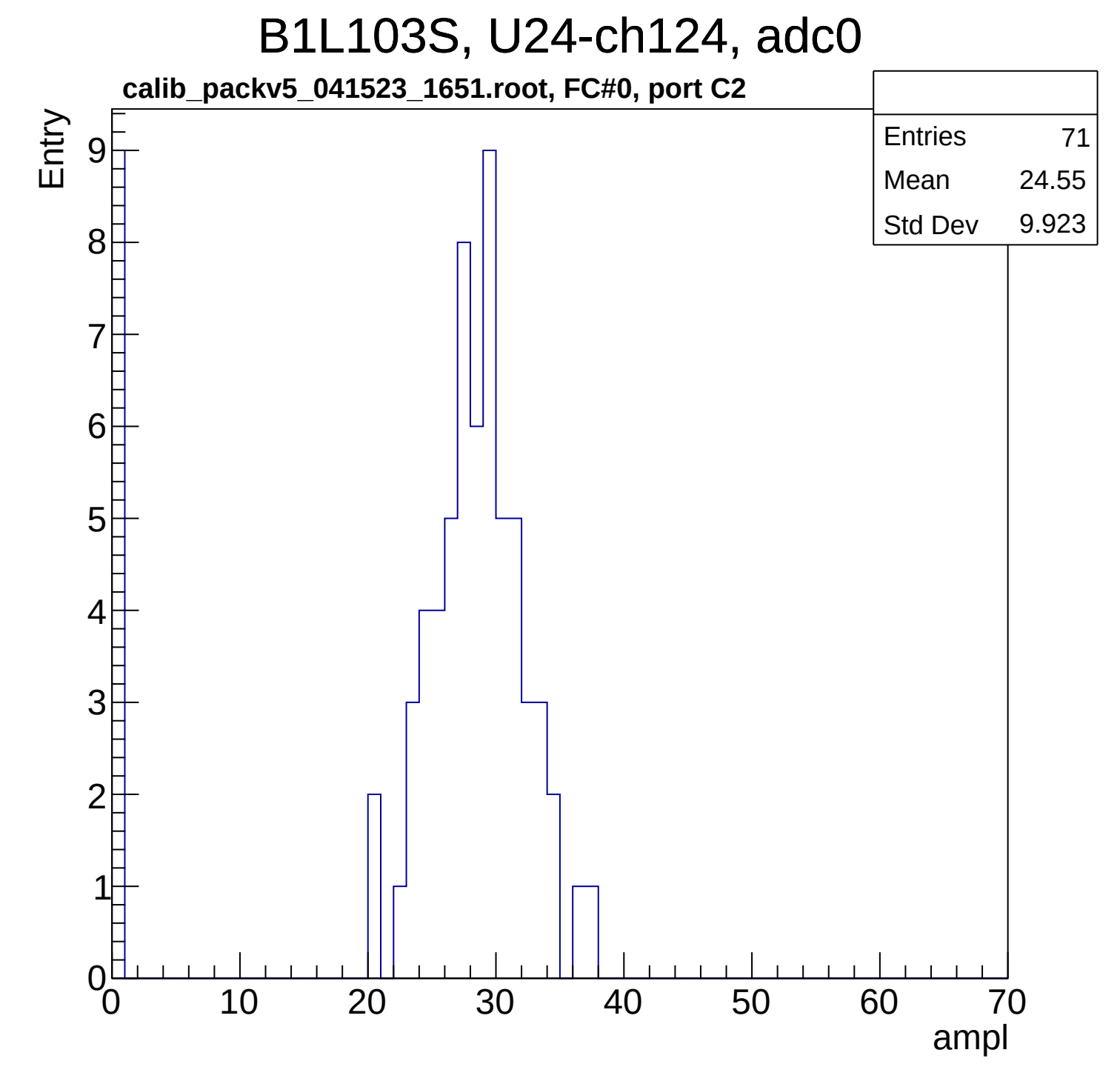
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U24-ch123, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 59.36
Std Dev 2.596
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U24-ch123, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 55.64
Std Dev 17.64
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U24-ch123, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch124, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 24.55
Std Dev 9.923
Entry
ampl
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2
3
4
5
6
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8
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0
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60
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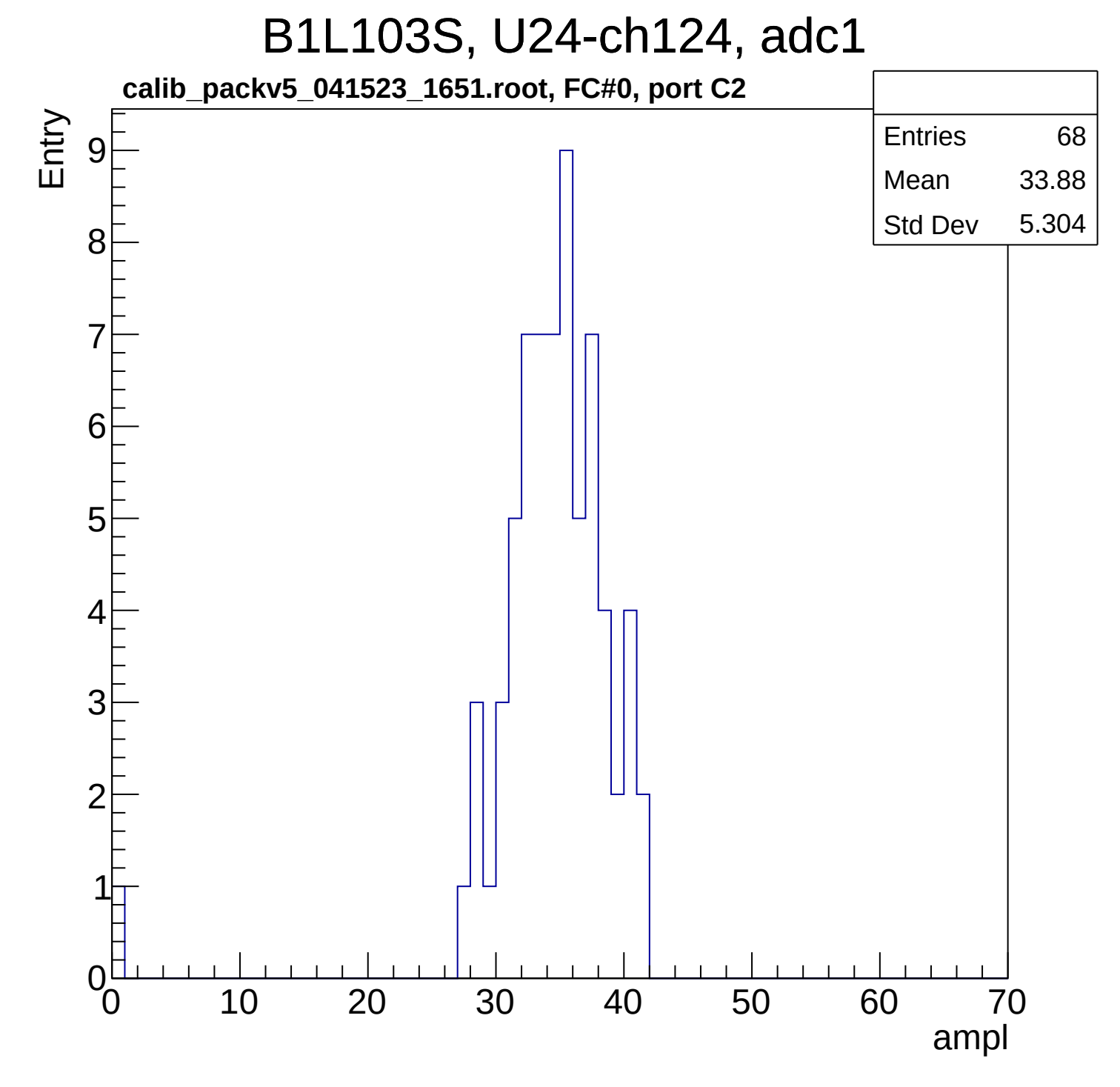
B1L103S, U24-ch124, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 33.88
Std Dev 5.304
Entry
ampl
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4
5
6
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8
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0
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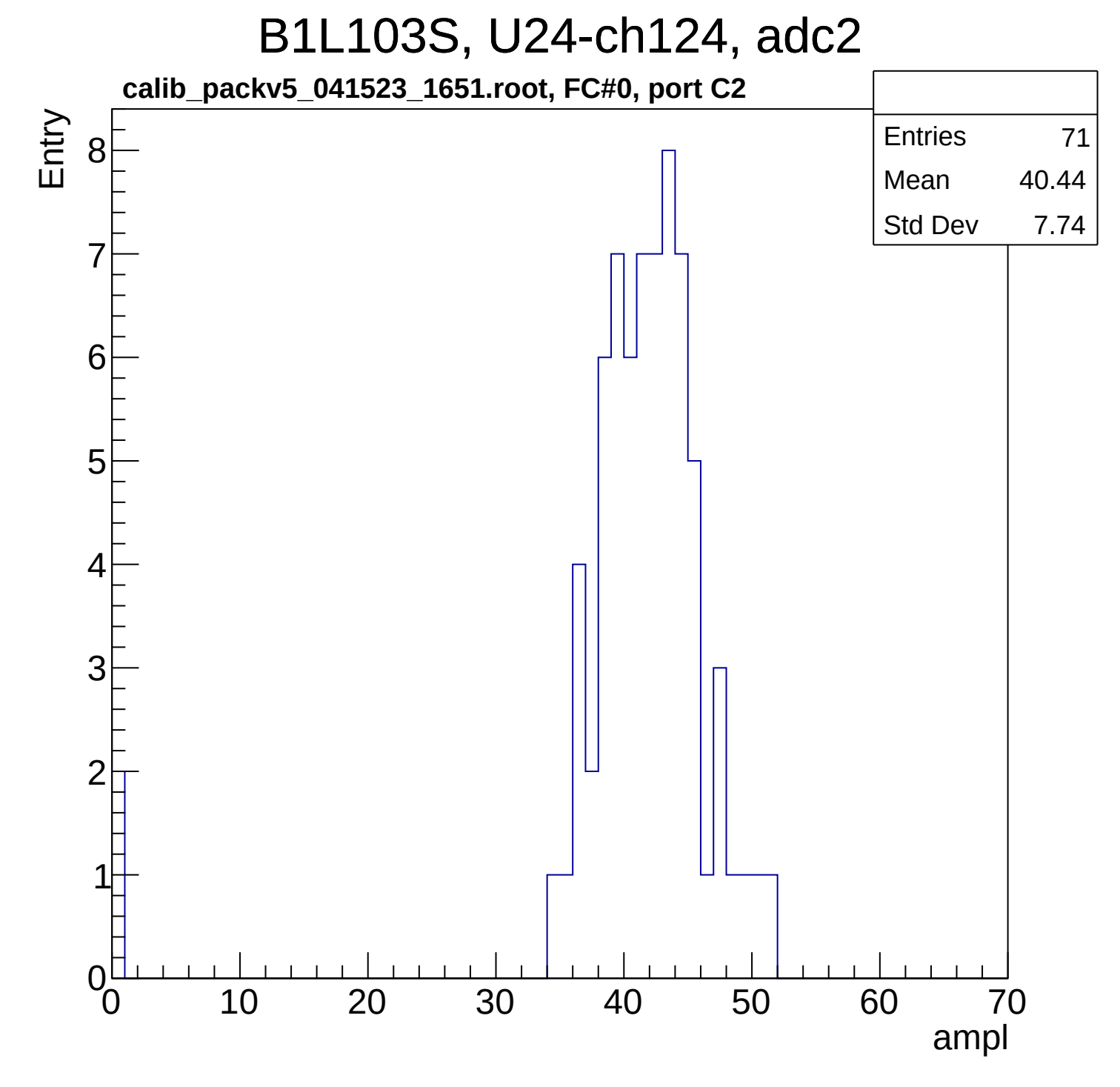
B1L103S, U24-ch124, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 40.44
Std Dev 7.74
Entry
ampl
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7
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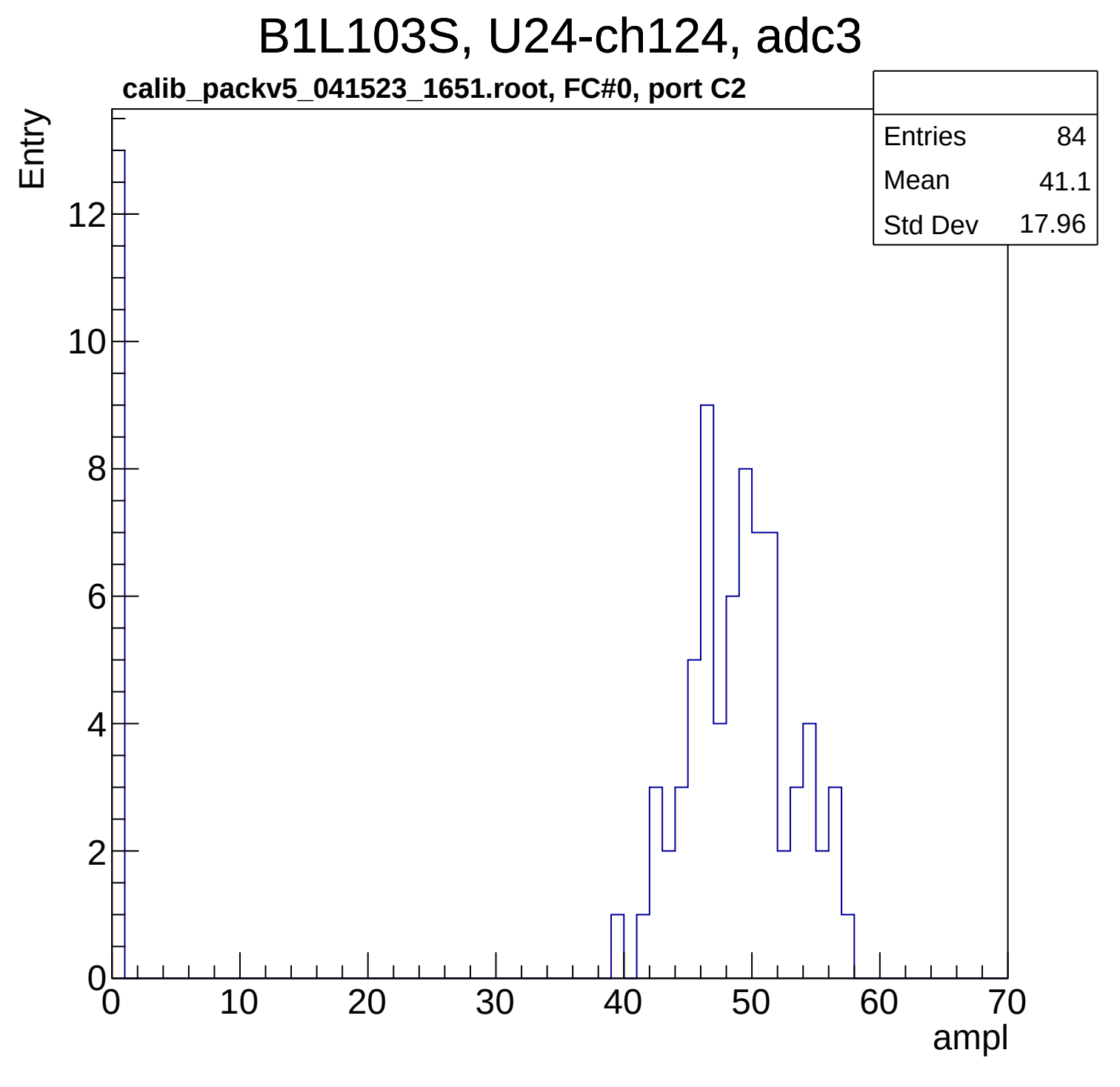
B1L103S, U24-ch124, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 41.1
Std Dev 17.96
Entry
ampl
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2
4
6
8
10
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0
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40
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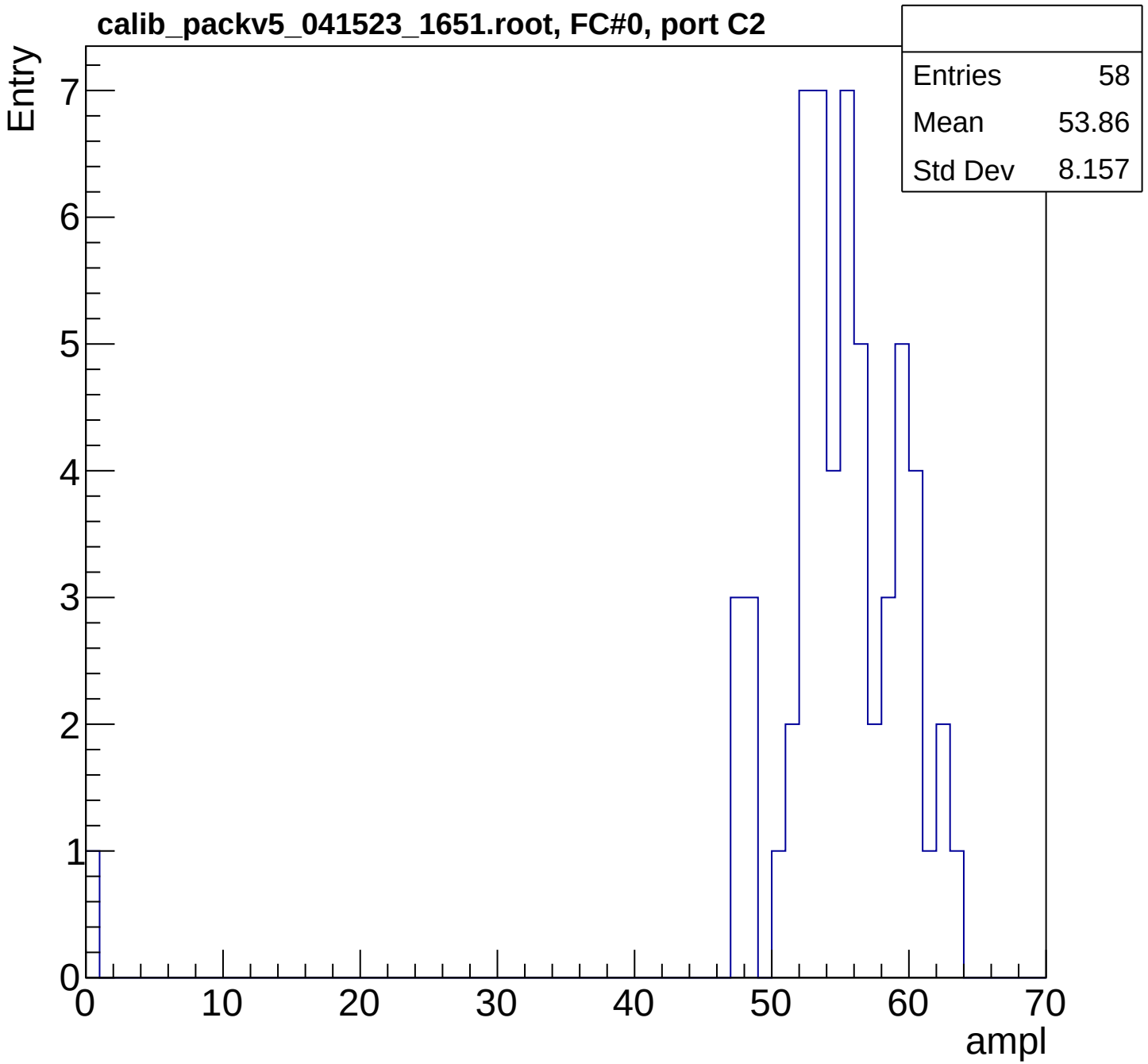
B1L103S, U24-ch124, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 53.86
Std Dev 8.157
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
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40
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60
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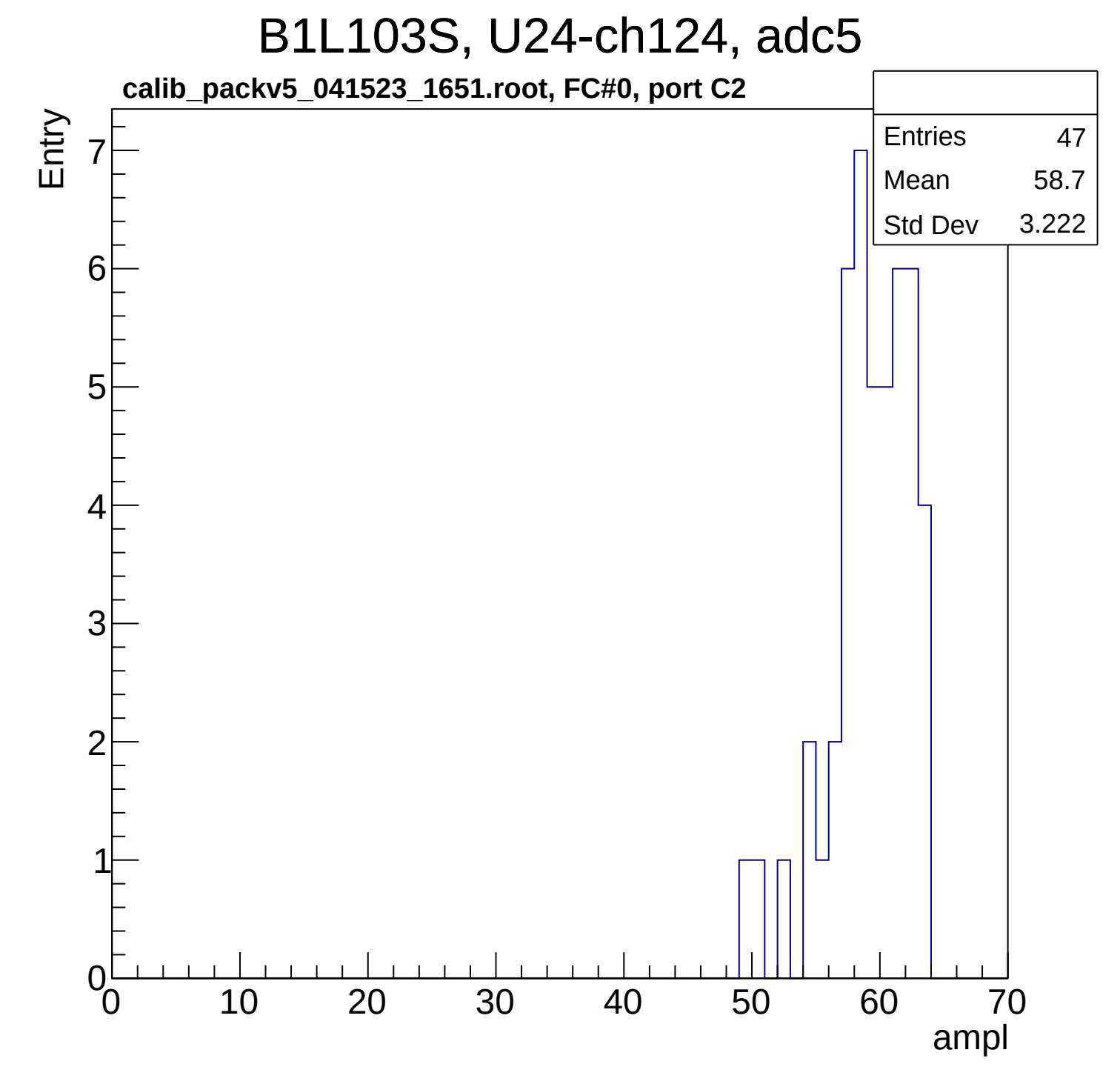
B1L103S, U24-ch124, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 58.7
Std Dev 3.222
Entry
ampl
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3
4
5
6
7
0
10
20
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40
50
60
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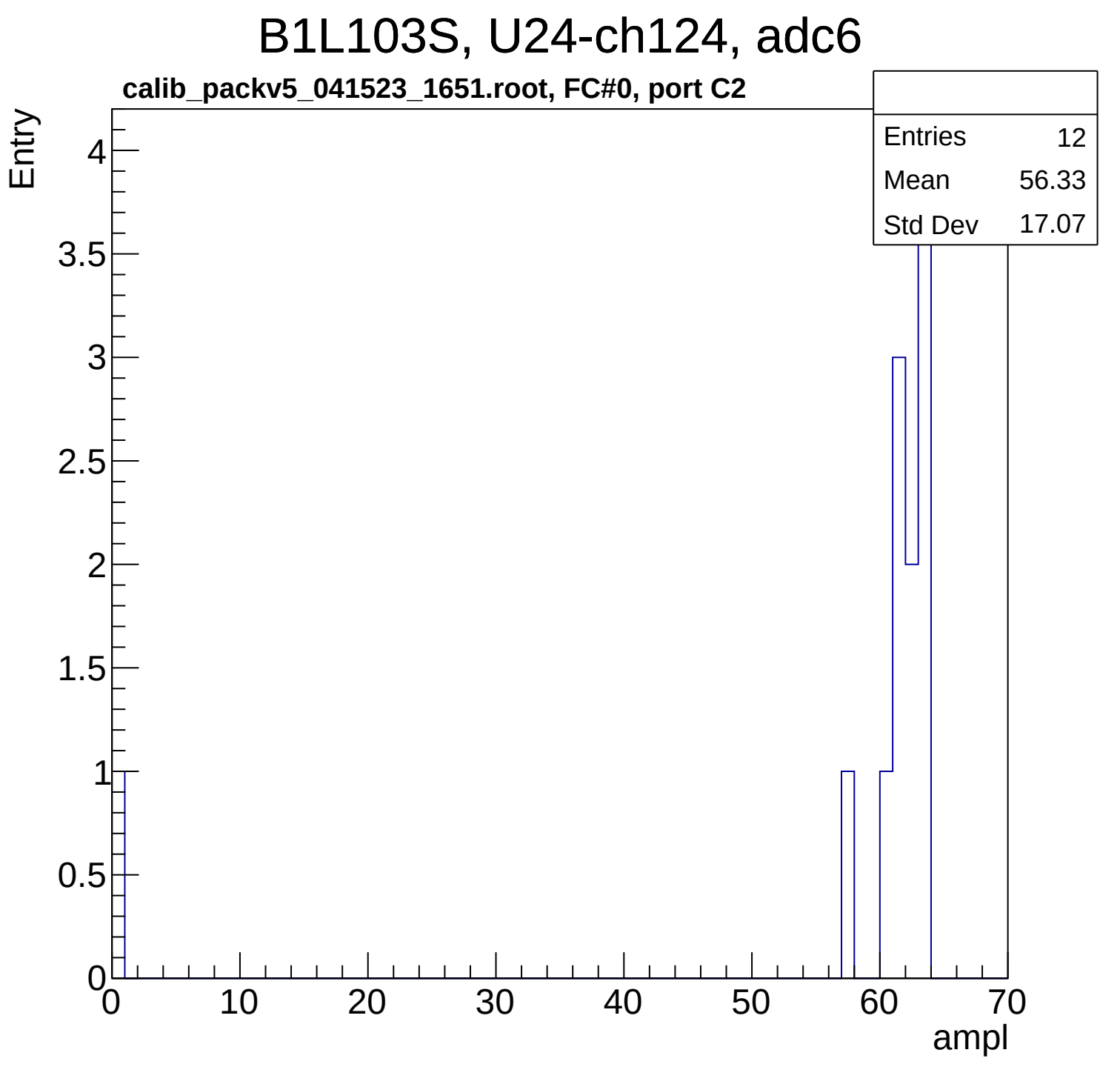
B1L103S, U24-ch124, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 56.33
Std Dev 17.07
Entry
ampl
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0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
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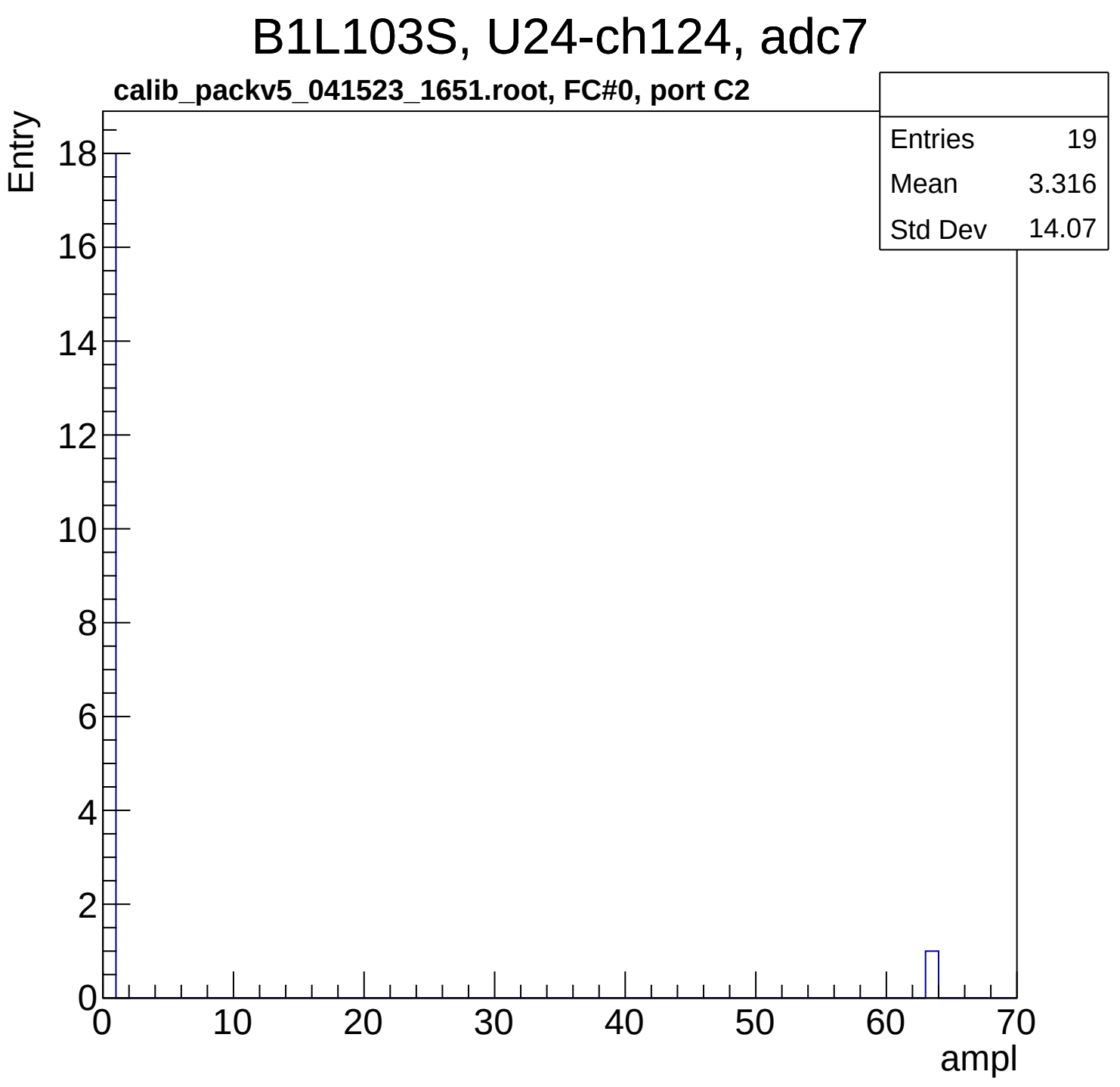
B1L103S, U24-ch124, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 3.316
Std Dev 14.07
Entry
0
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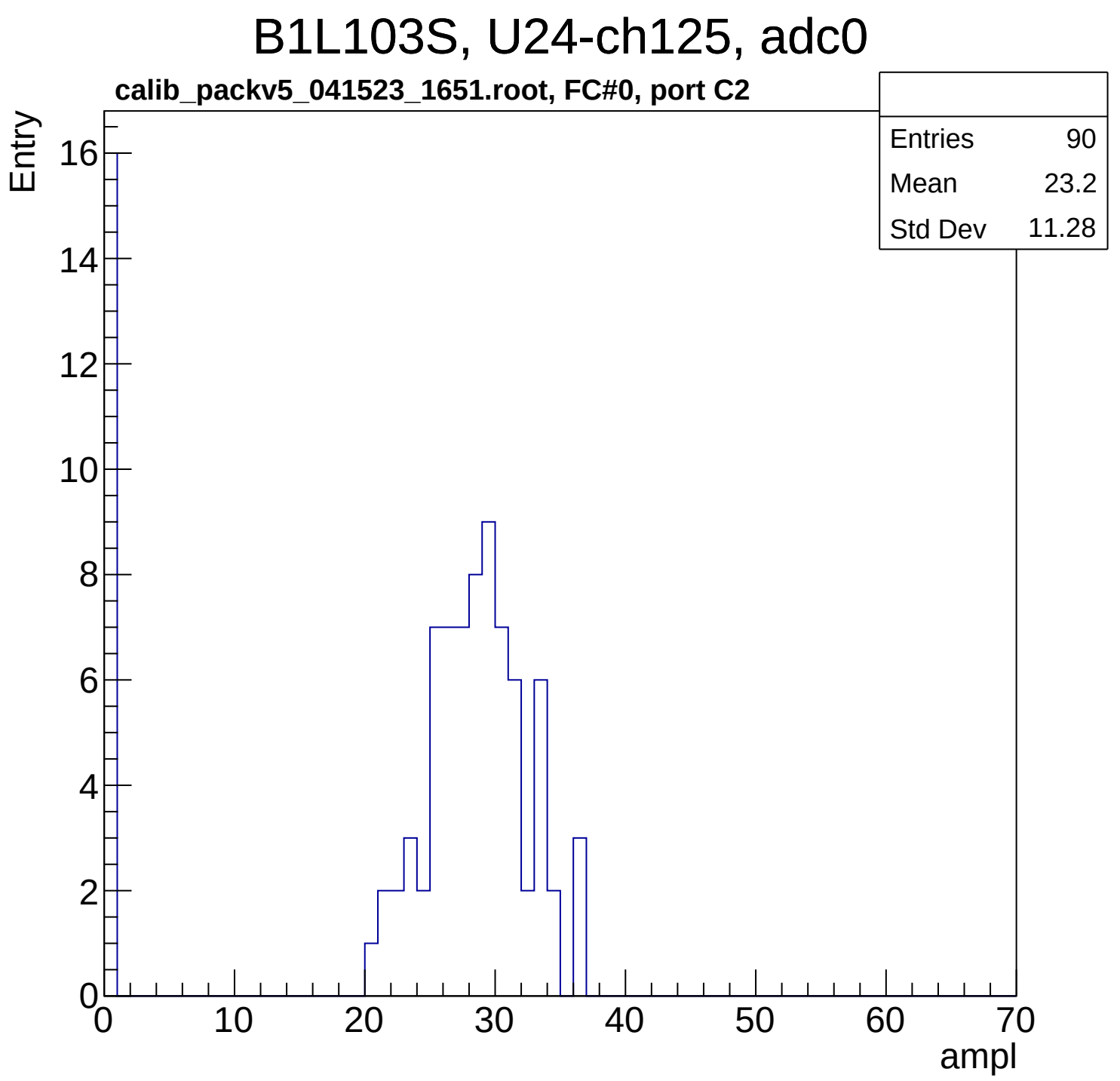
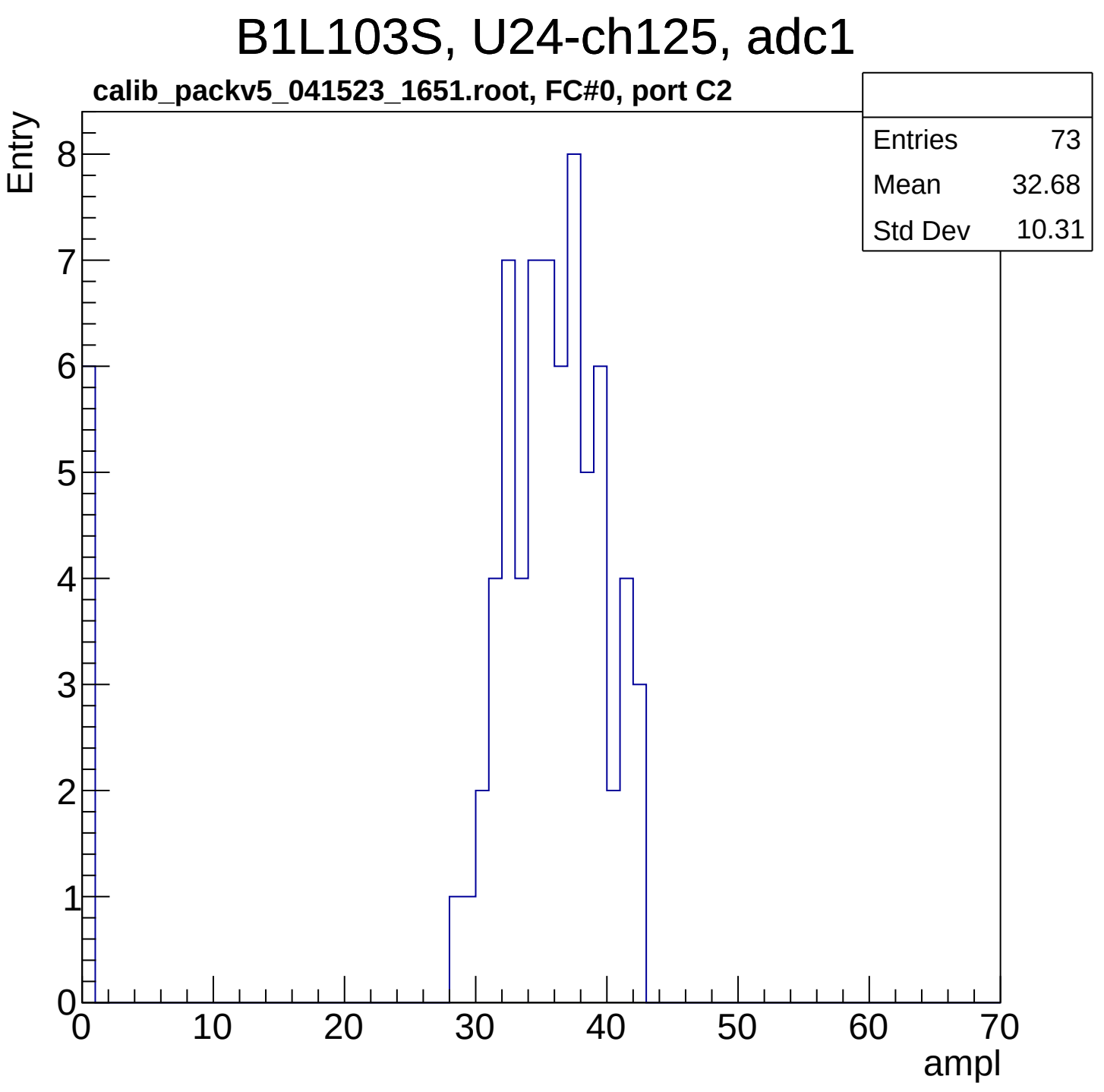
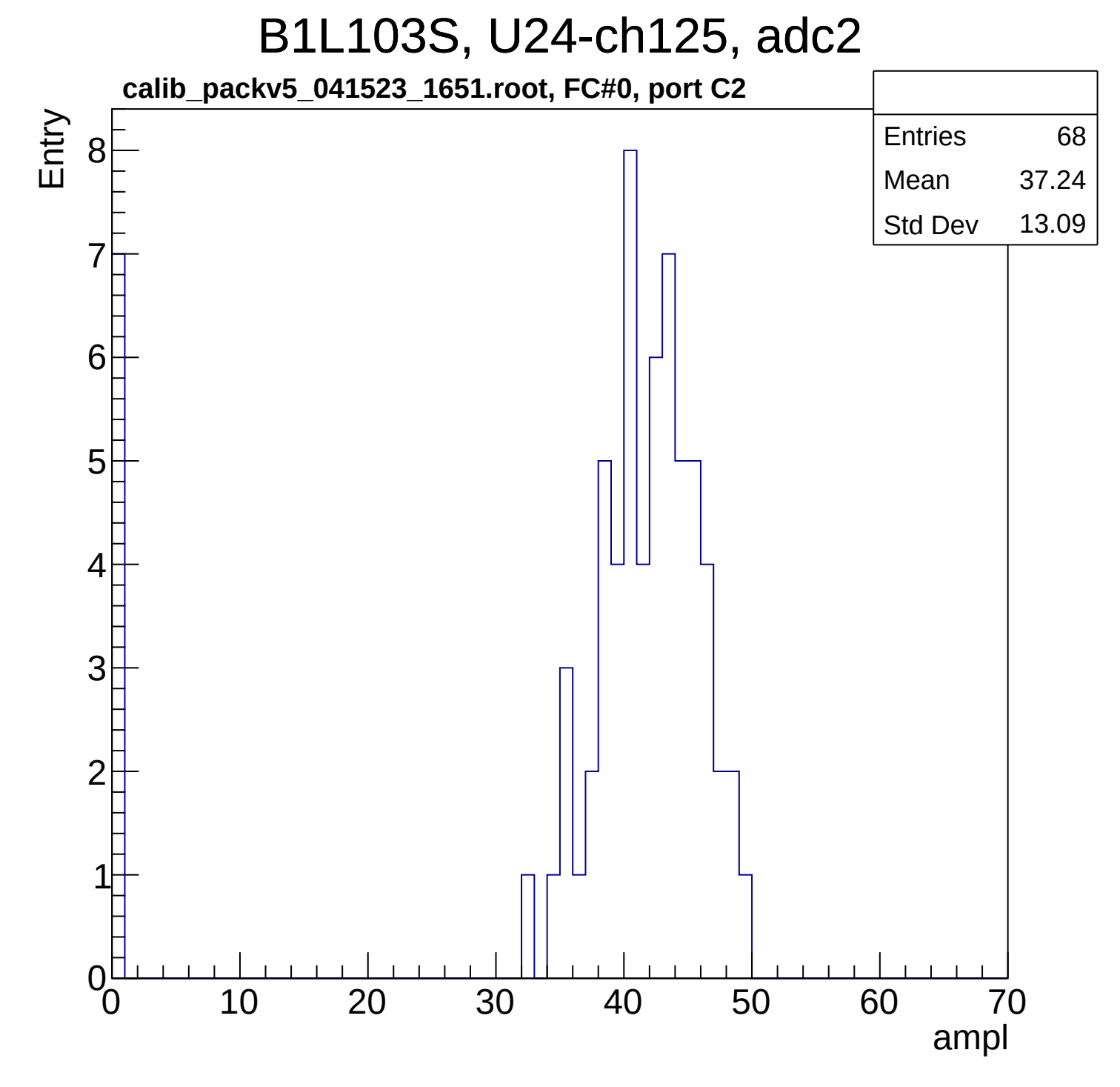
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch125, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 90
Mean 23.2
Std Dev 11.28
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70


B1L103S, U24-ch125, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 32.68
Std Dev 10.31
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U24-ch125, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 37.24
Std Dev 13.09
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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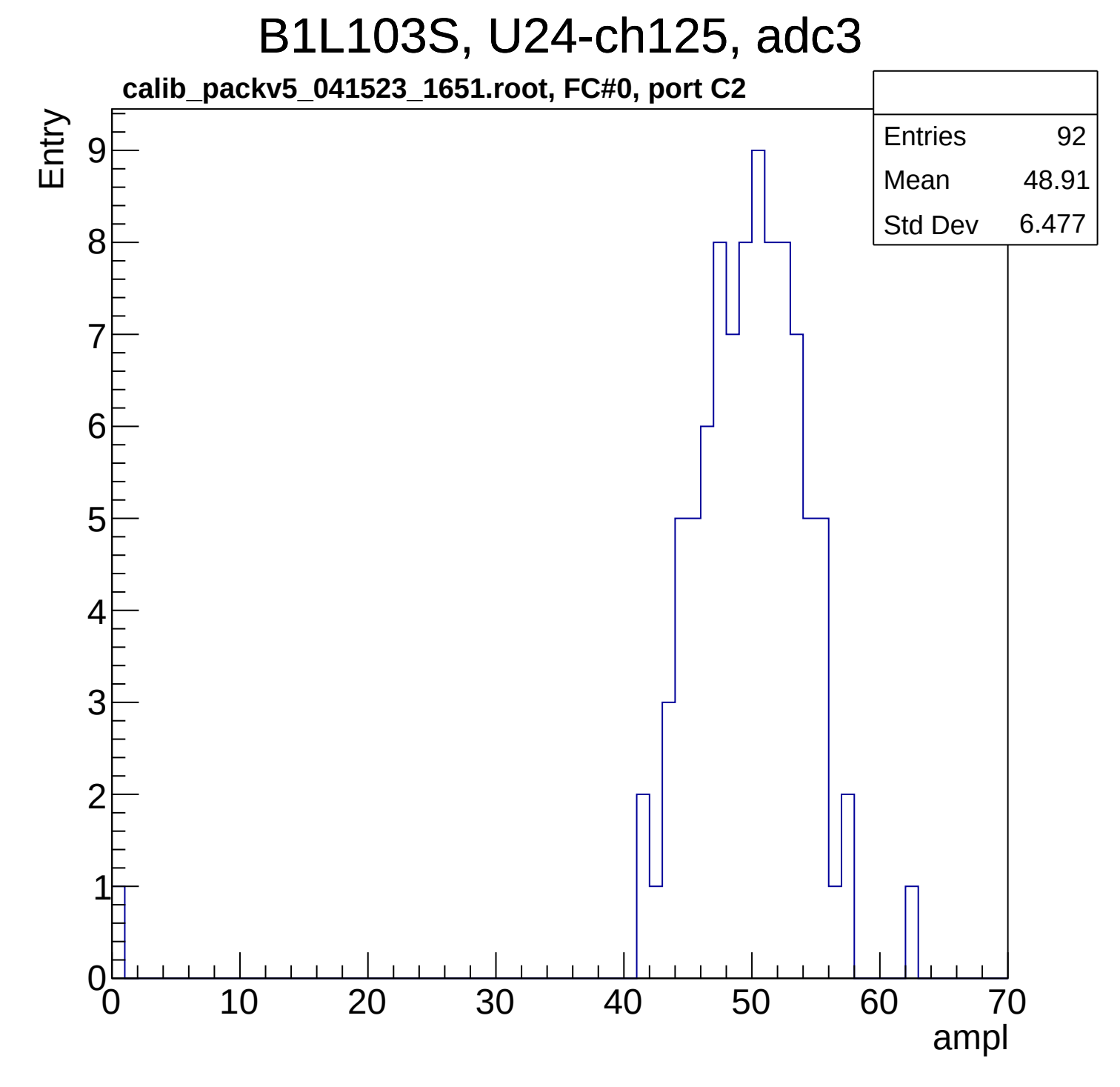
B1L103S, U24-ch125, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 92
Mean 48.91
Std Dev 6.477
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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60
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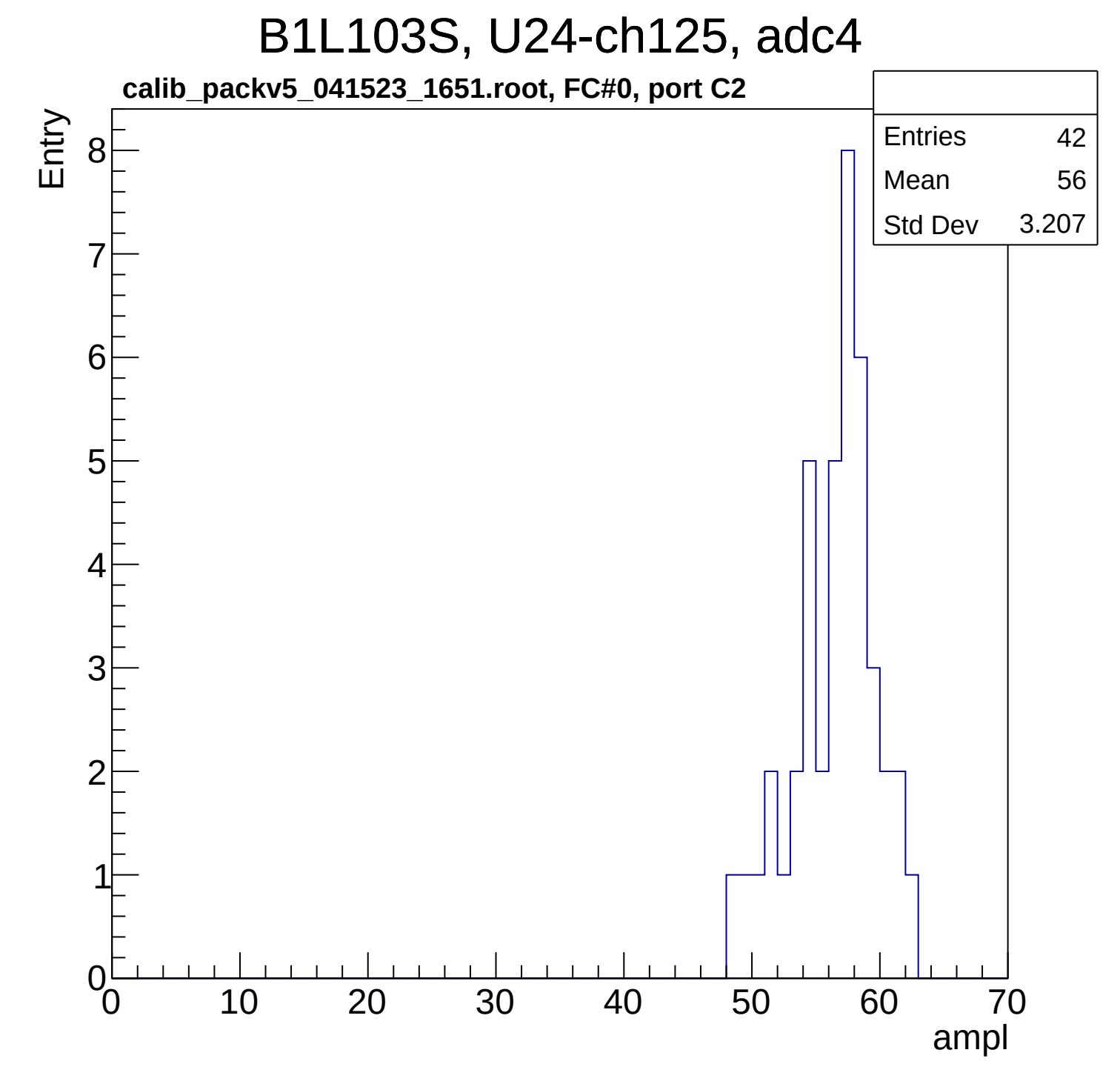
B1L103S, U24-ch125, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 42
Mean 56
Std Dev 3.207
Entry
ampl
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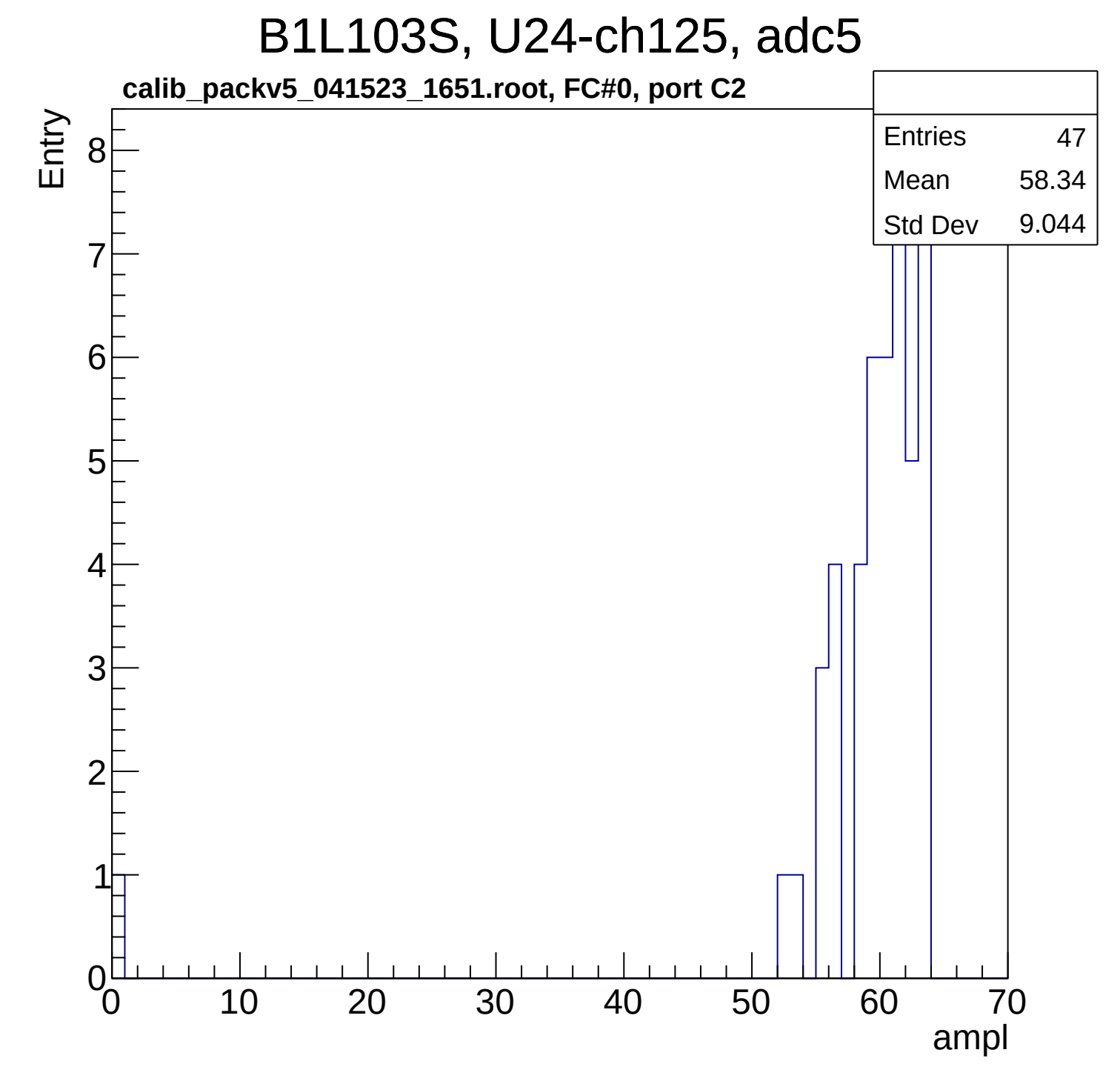
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U24-ch125, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 58.34
Std Dev 9.044
Entry
ampl
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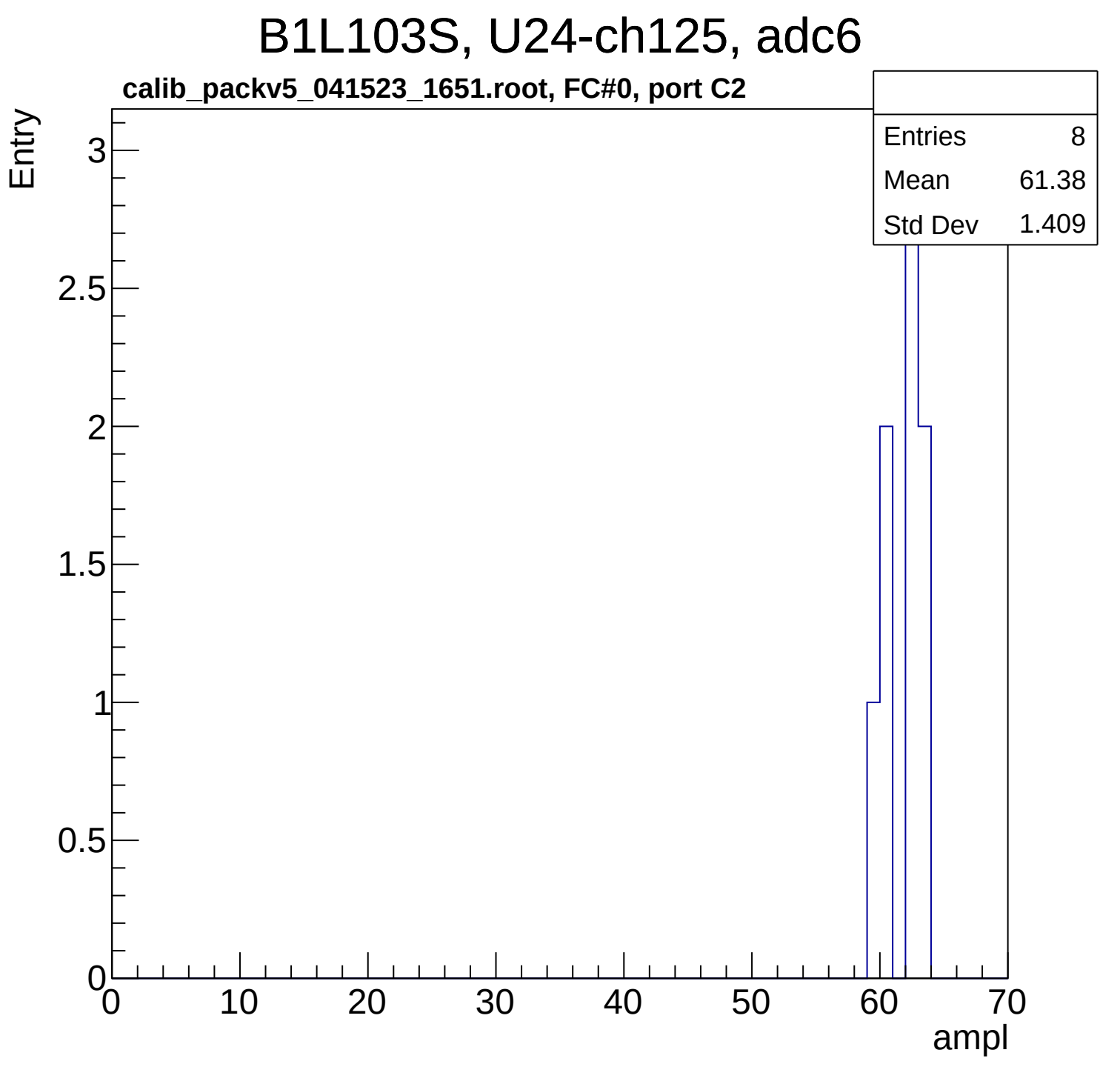
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U24-ch125, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 61.38
Std Dev 1.409
Entry
ampl
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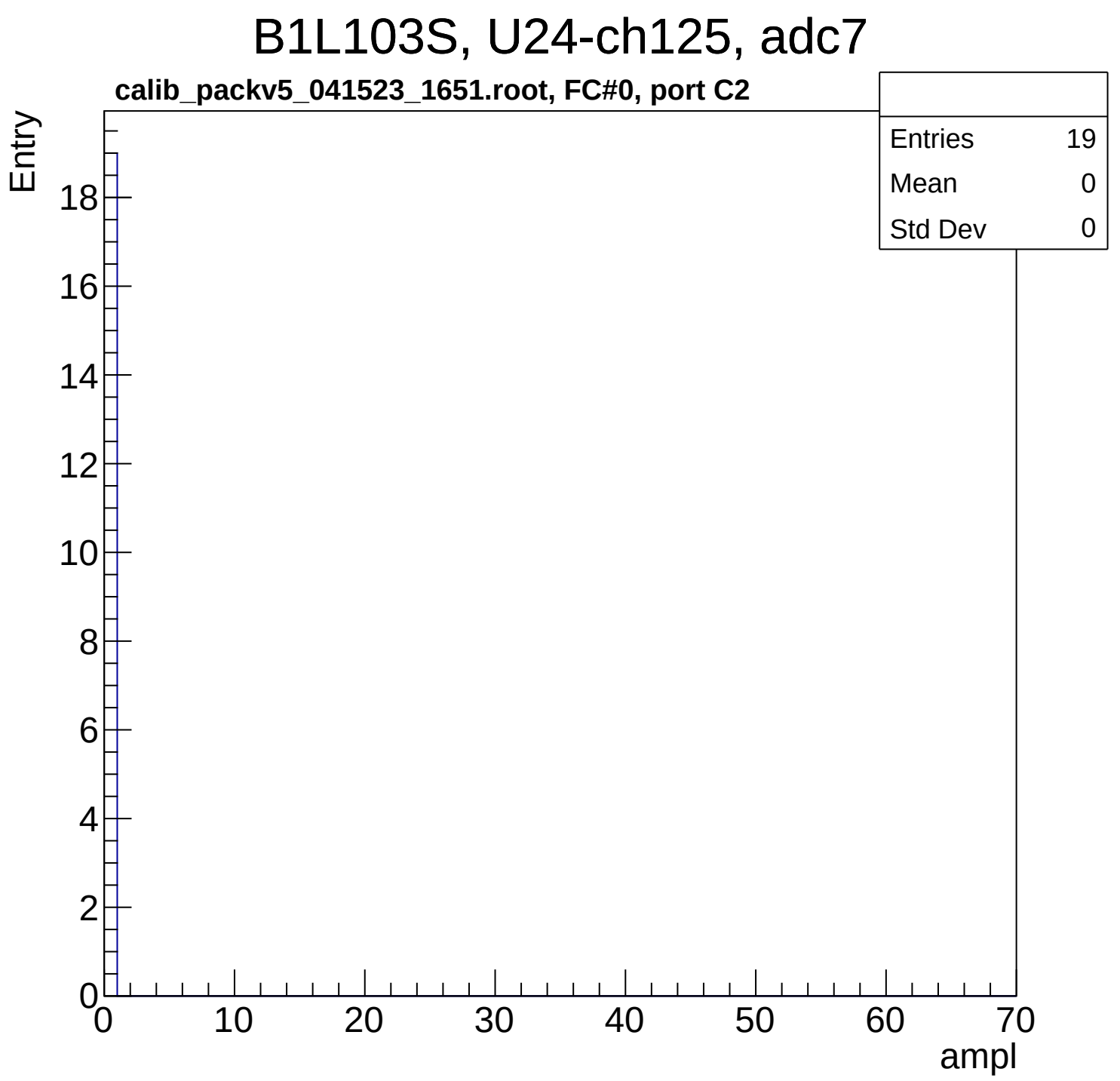
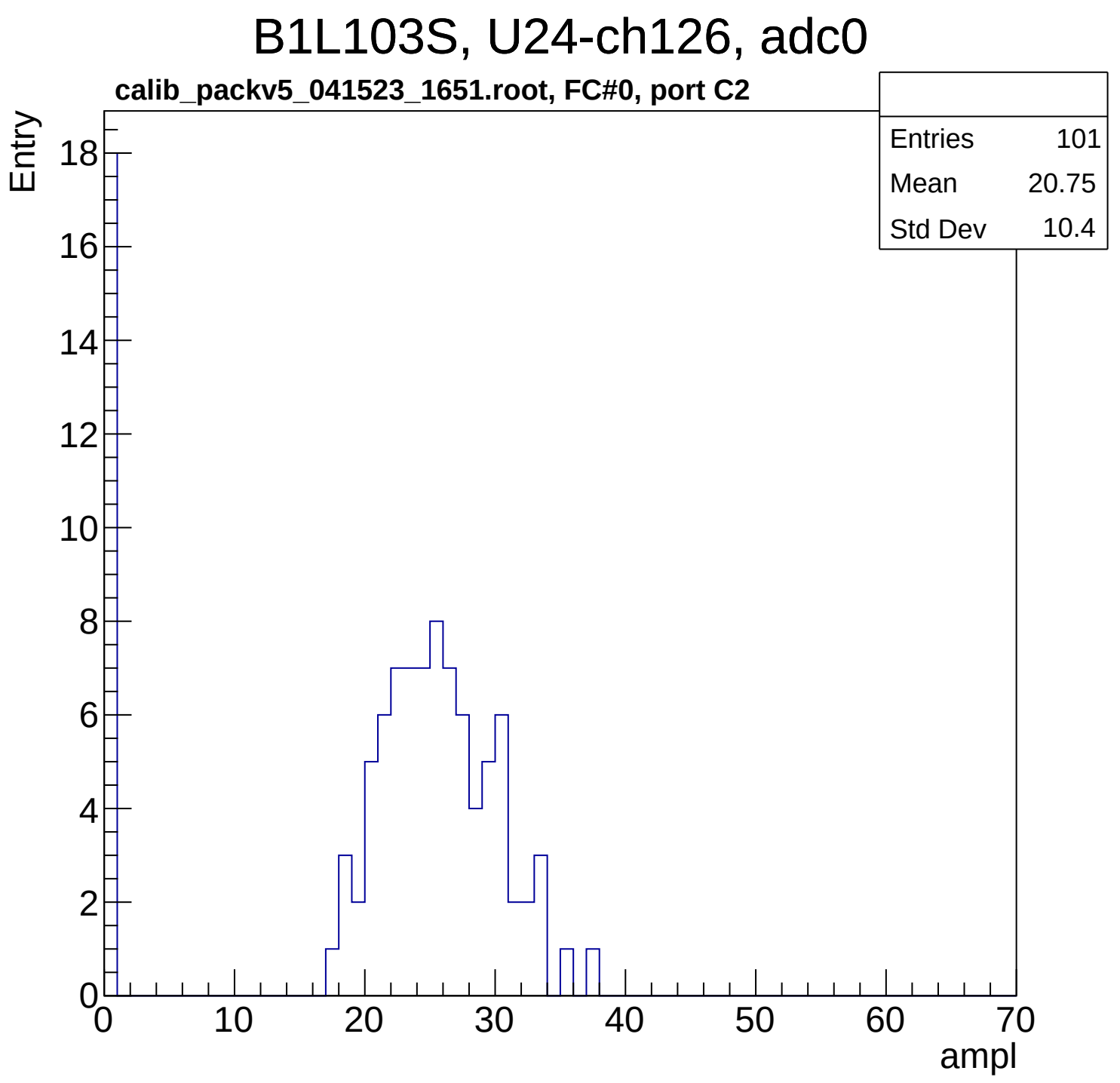
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U24-ch125, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch126, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 101
Mean 20.75
Std Dev 10.4
Entry
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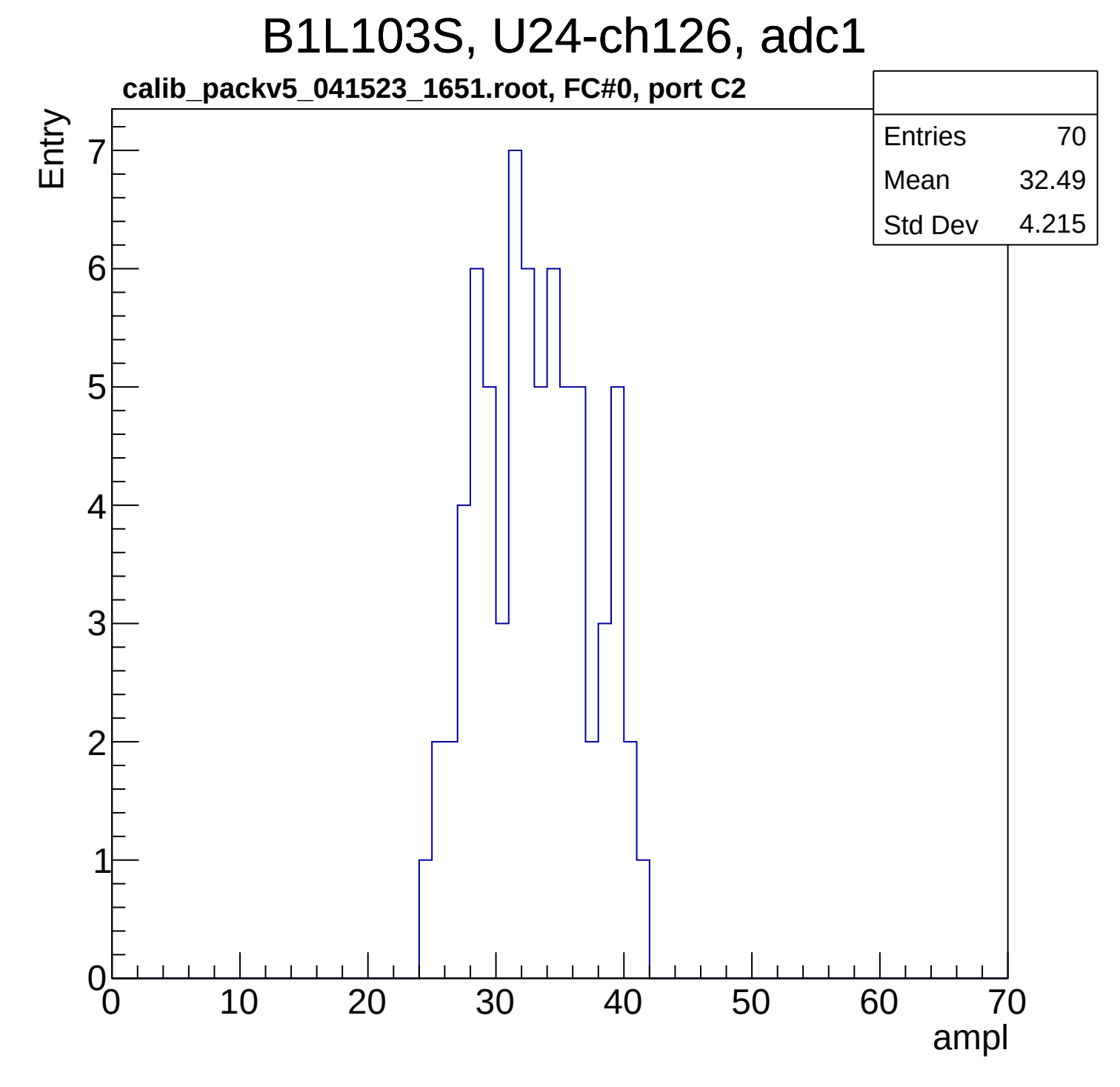
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch126, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 32.49
Std Dev 4.215
Entry
ampl
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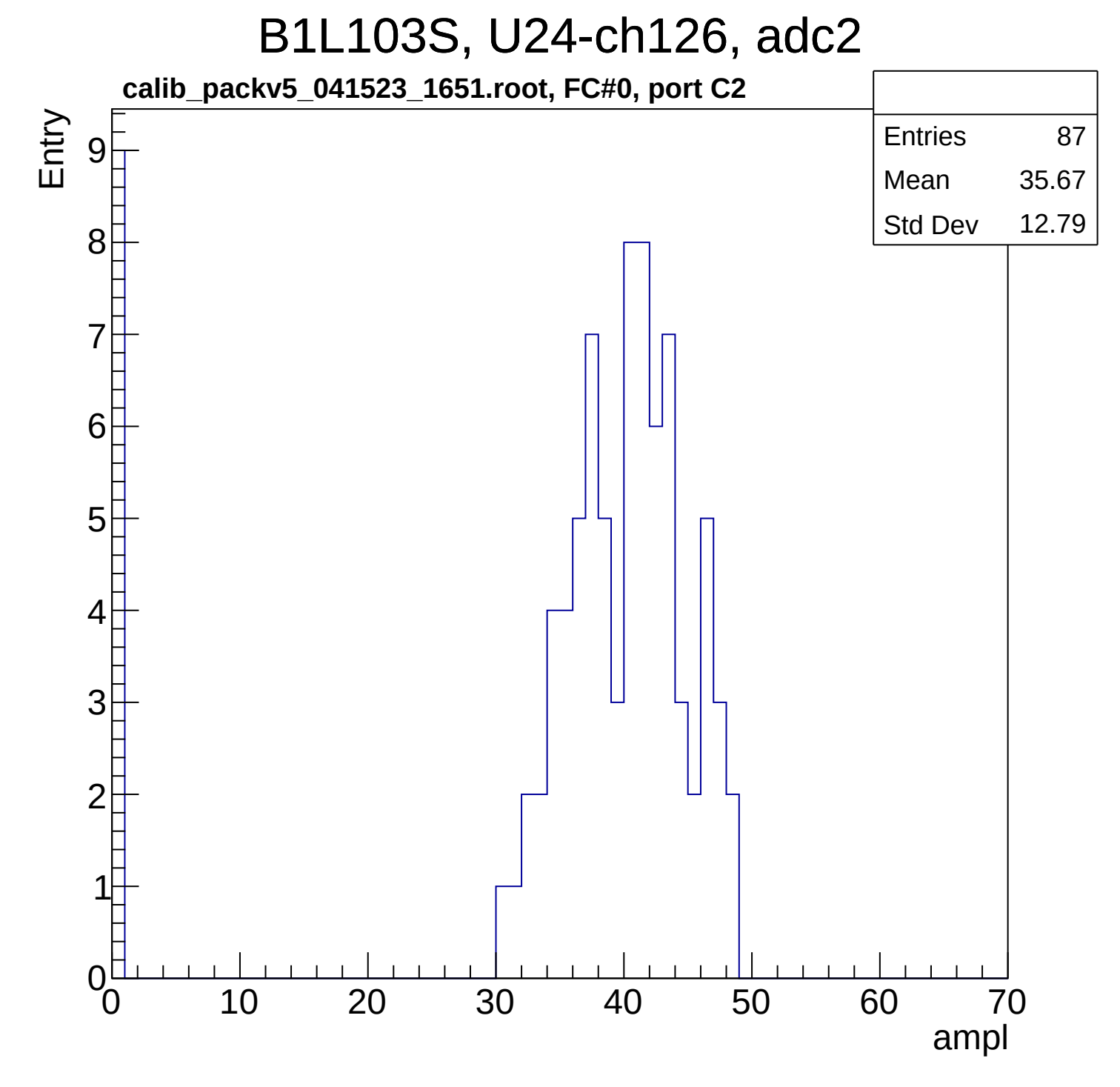
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U24-ch126, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 87
Mean 35.67
Std Dev 12.79
Entry
ampl
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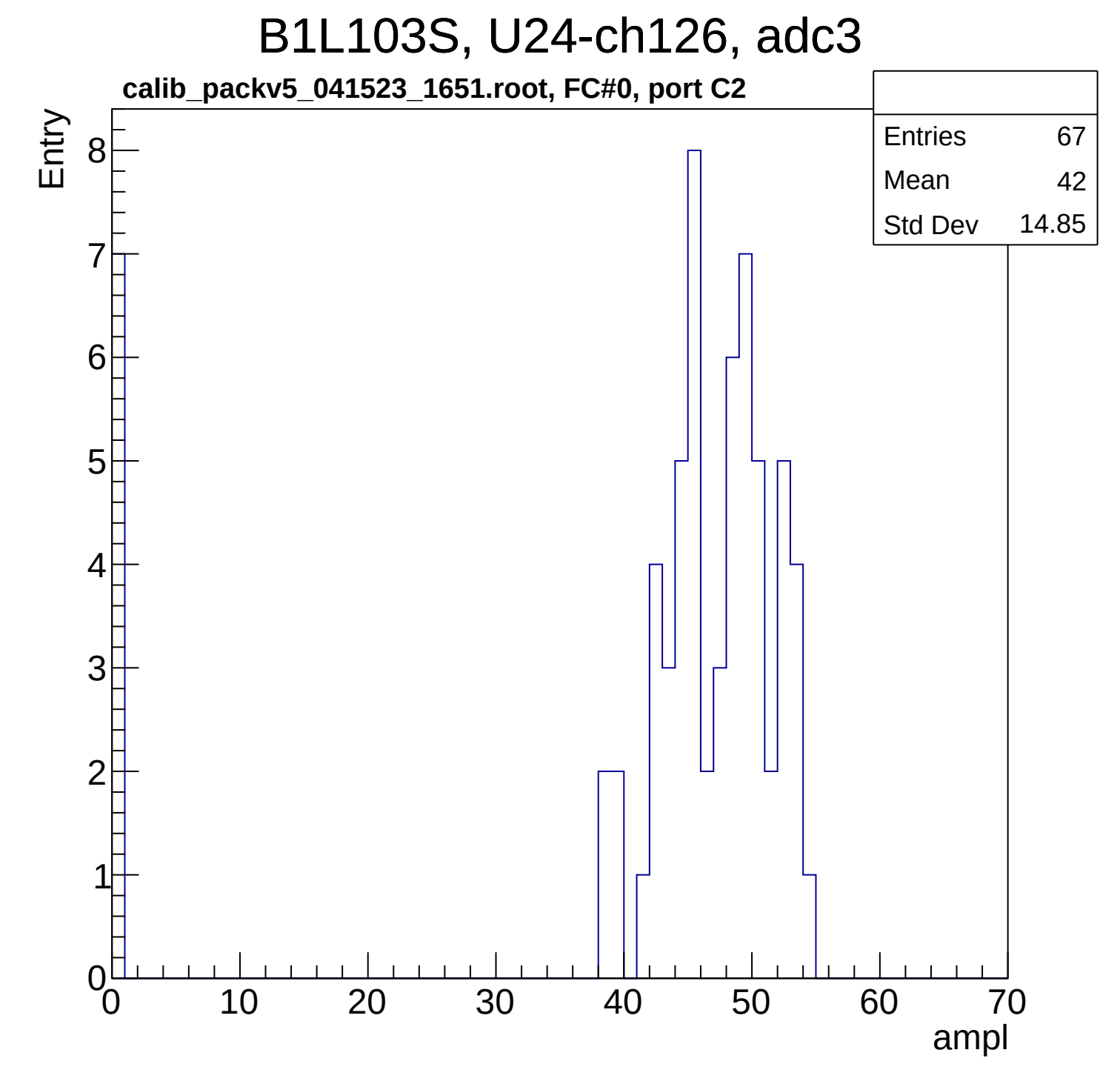
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U24-ch126, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 42
Std Dev 14.85
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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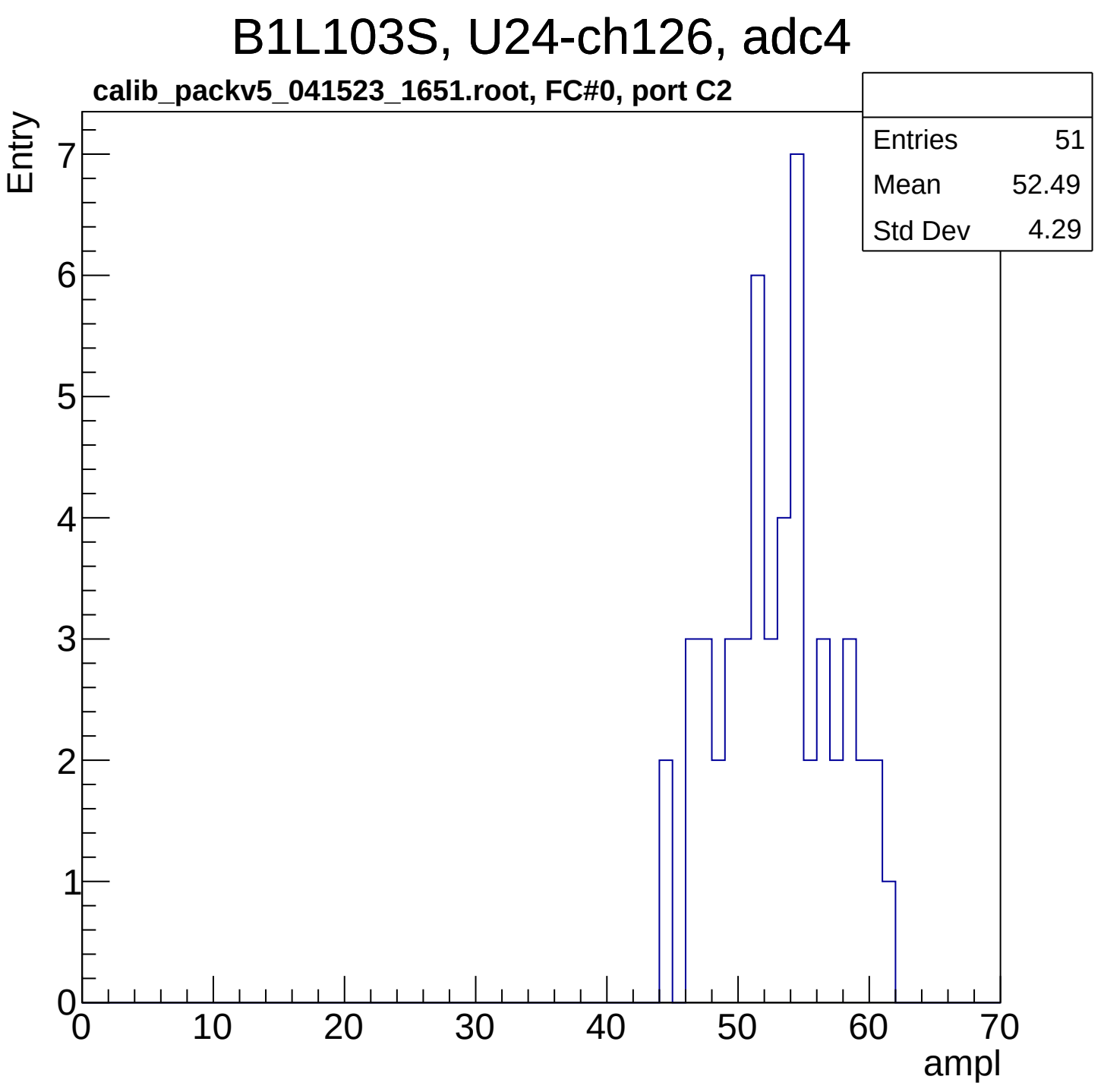
40
50
60
70


B1L103S, U24-ch126, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 52.49
Std Dev 4.29
Entry
ampl
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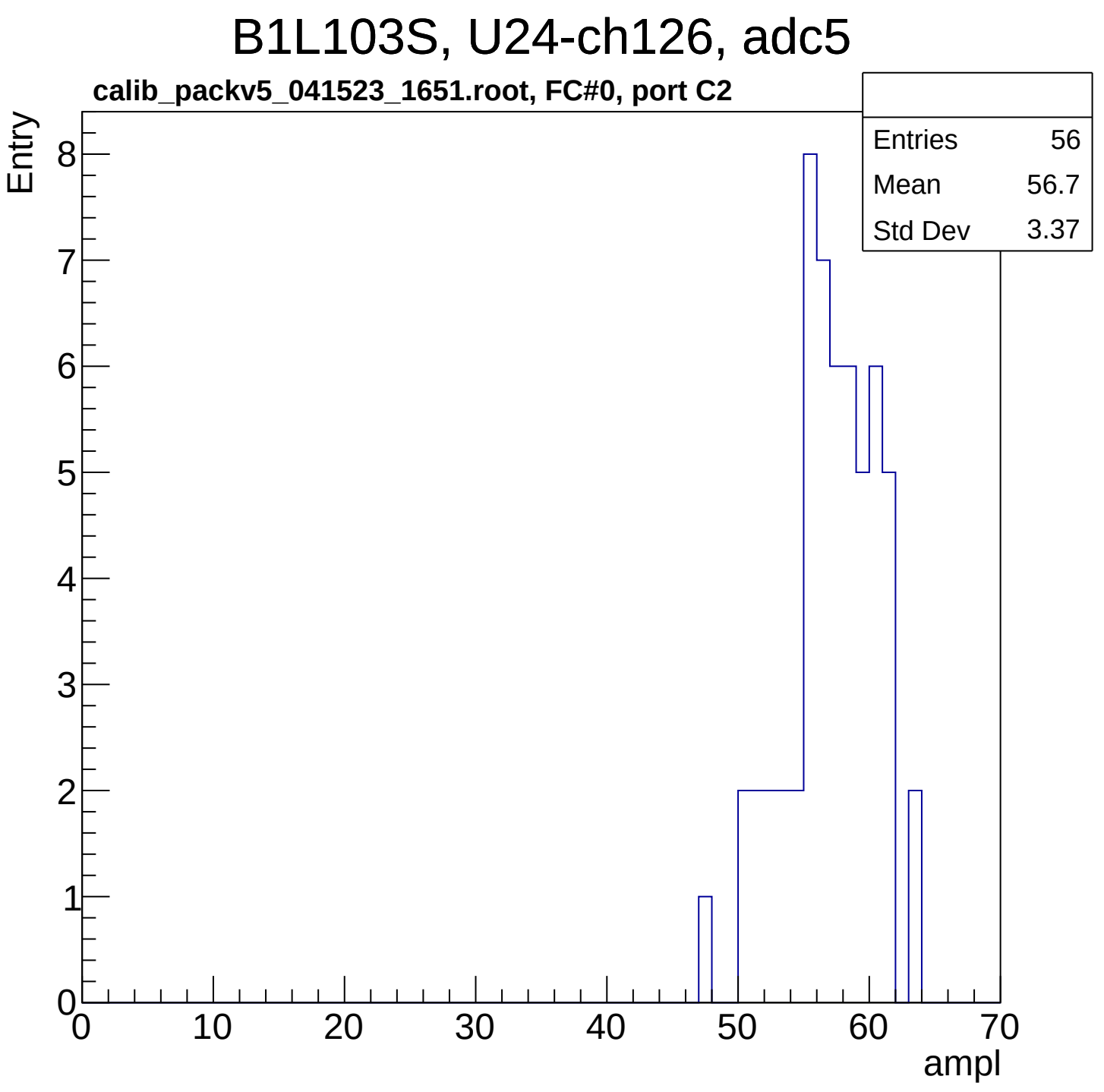
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U24-ch126, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 56.7
Std Dev 3.37
Entry
ampl
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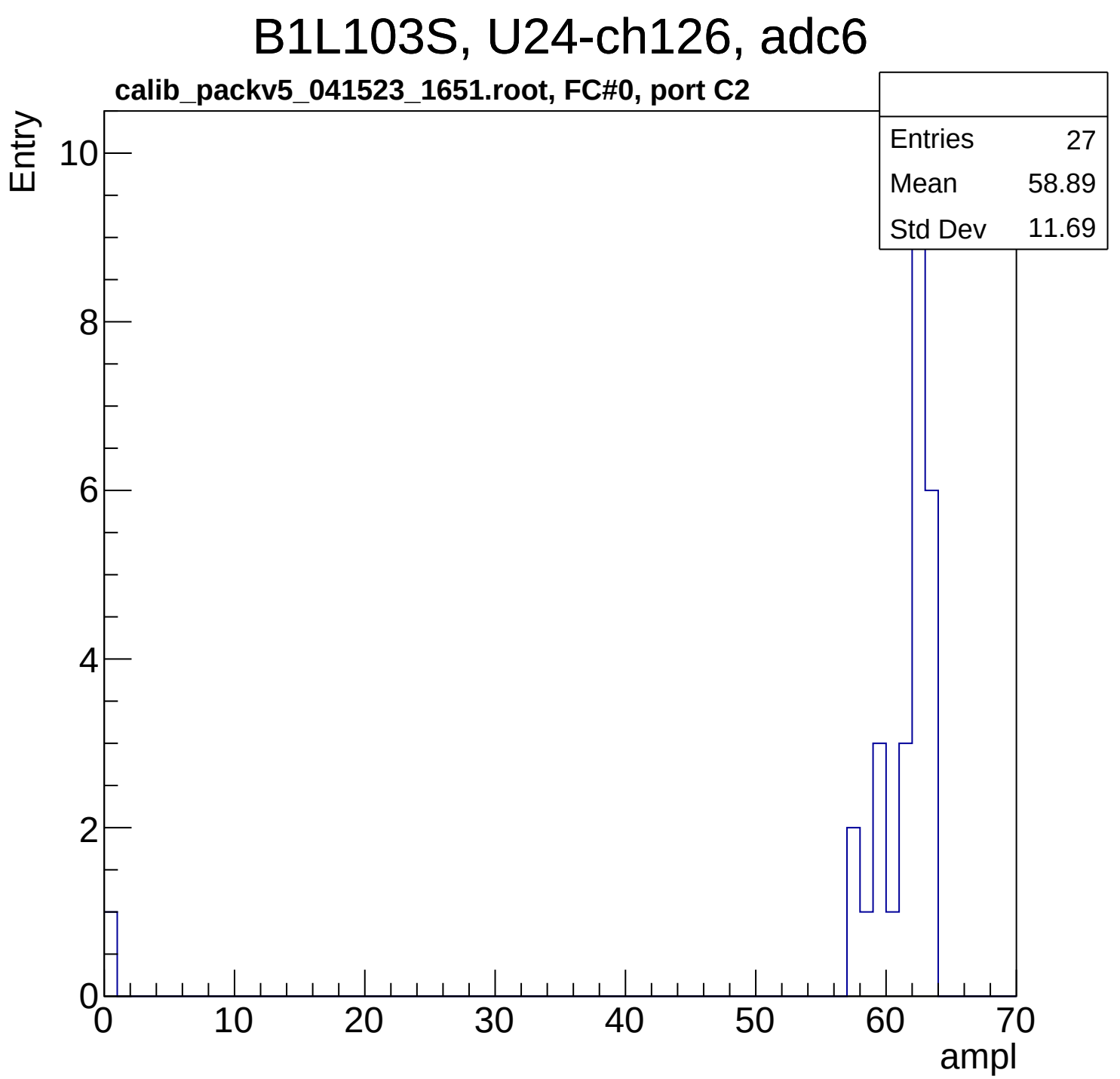
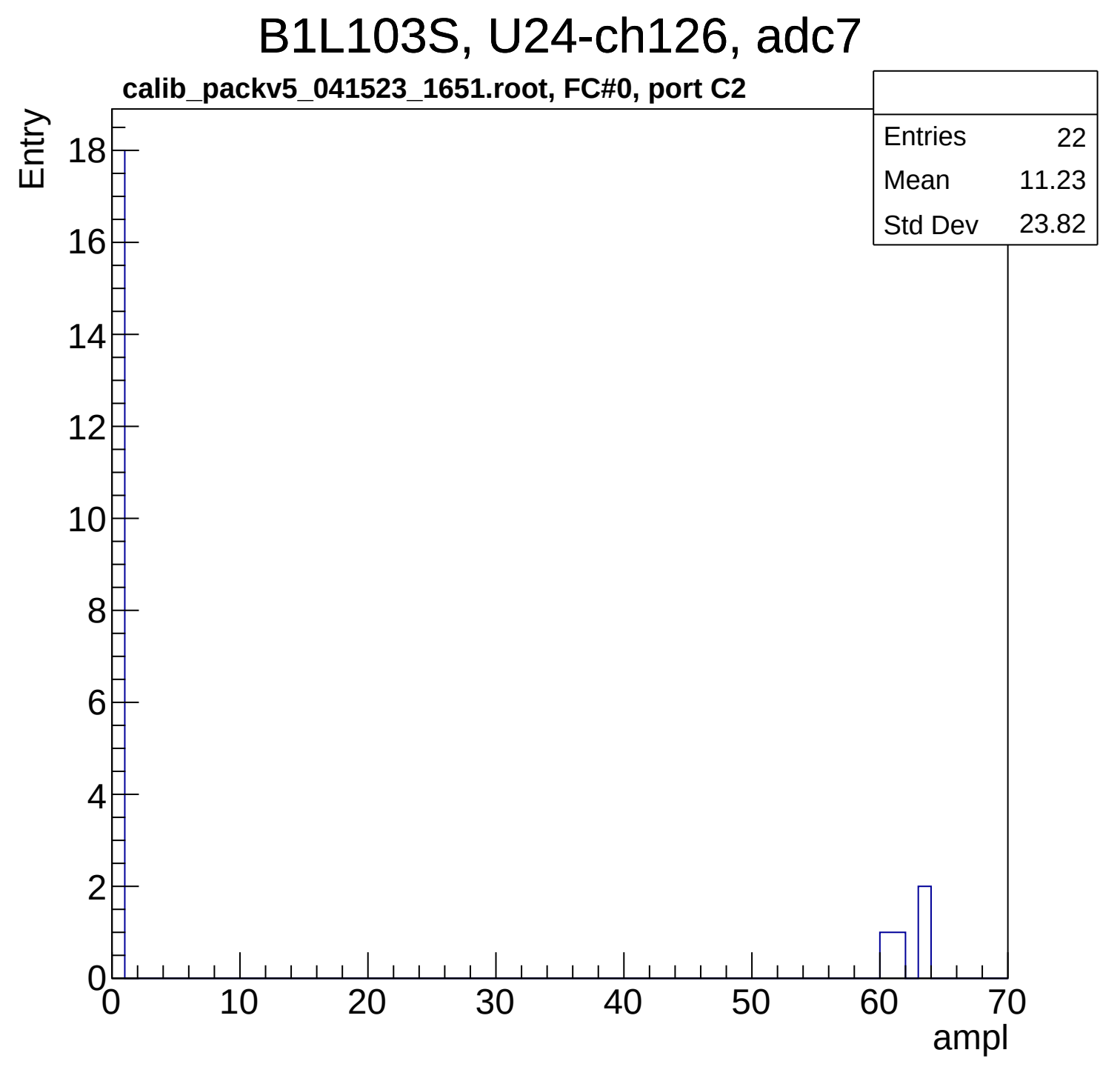
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U24-ch126, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 27
Mean 58.89
Std Dev 11.69
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U24-ch126, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 11.23
Std Dev 23.82
Entry
0
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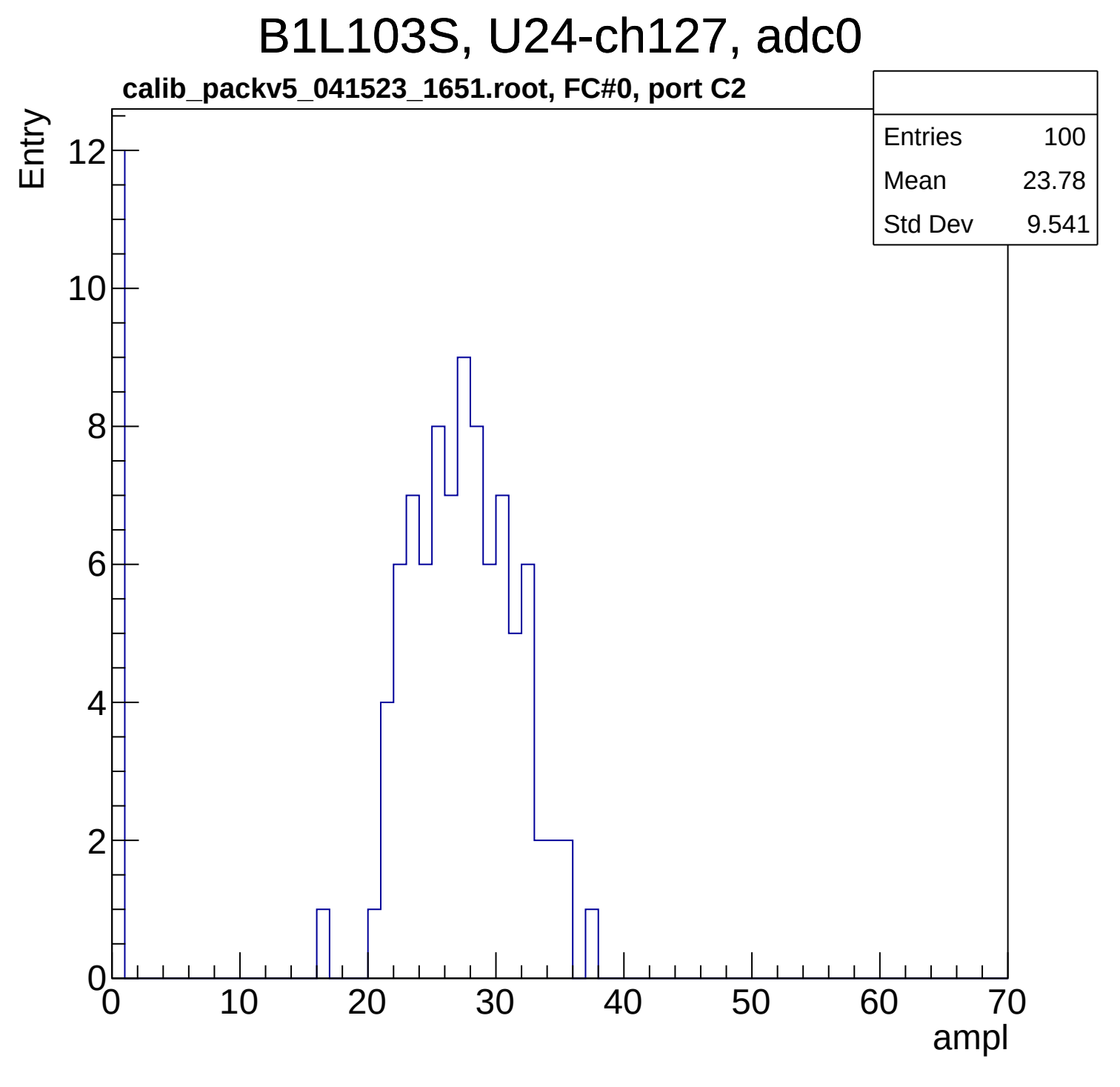
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch127, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 100
Mean 23.78
Std Dev 9.541
Entry
ampl
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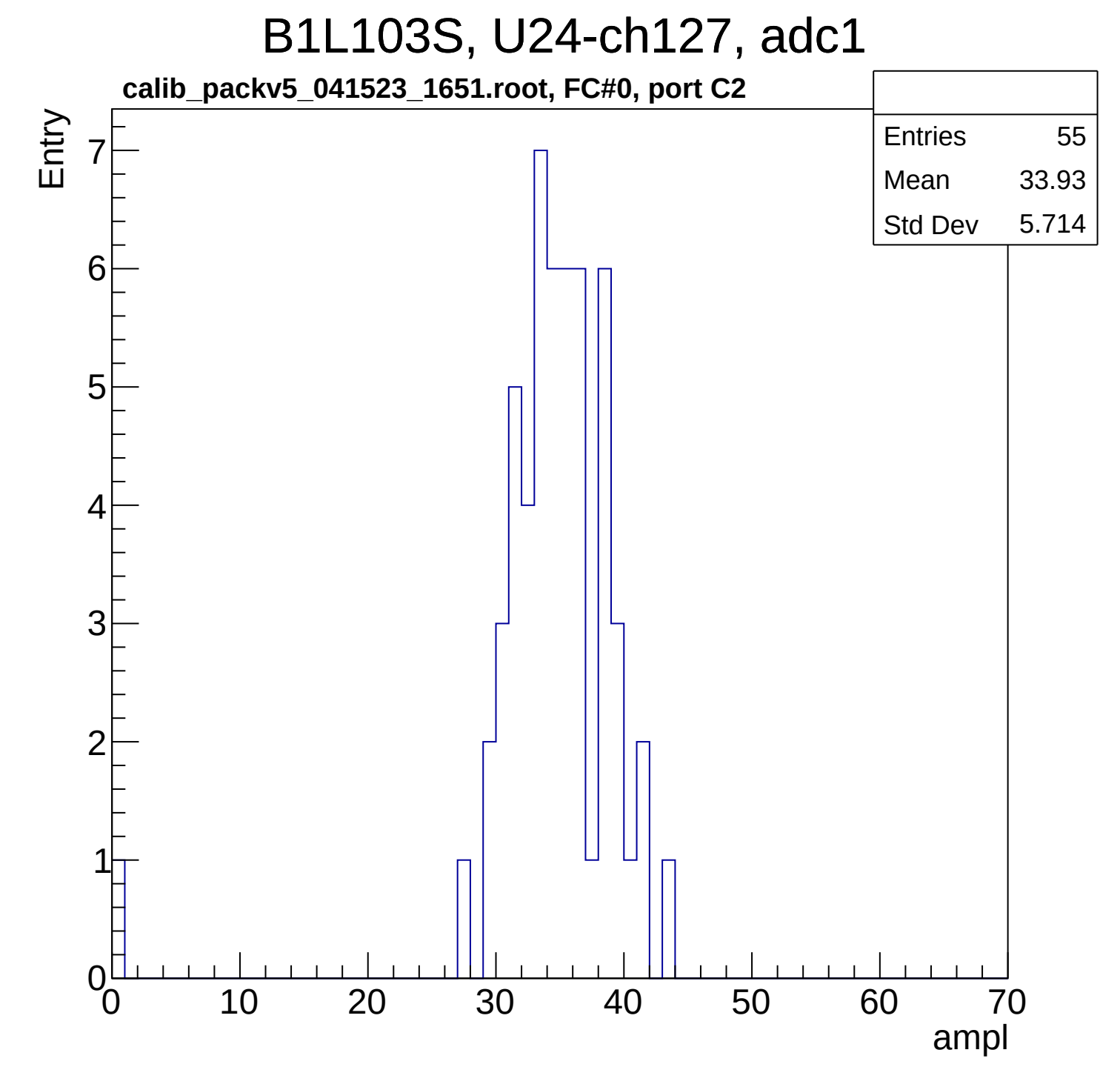
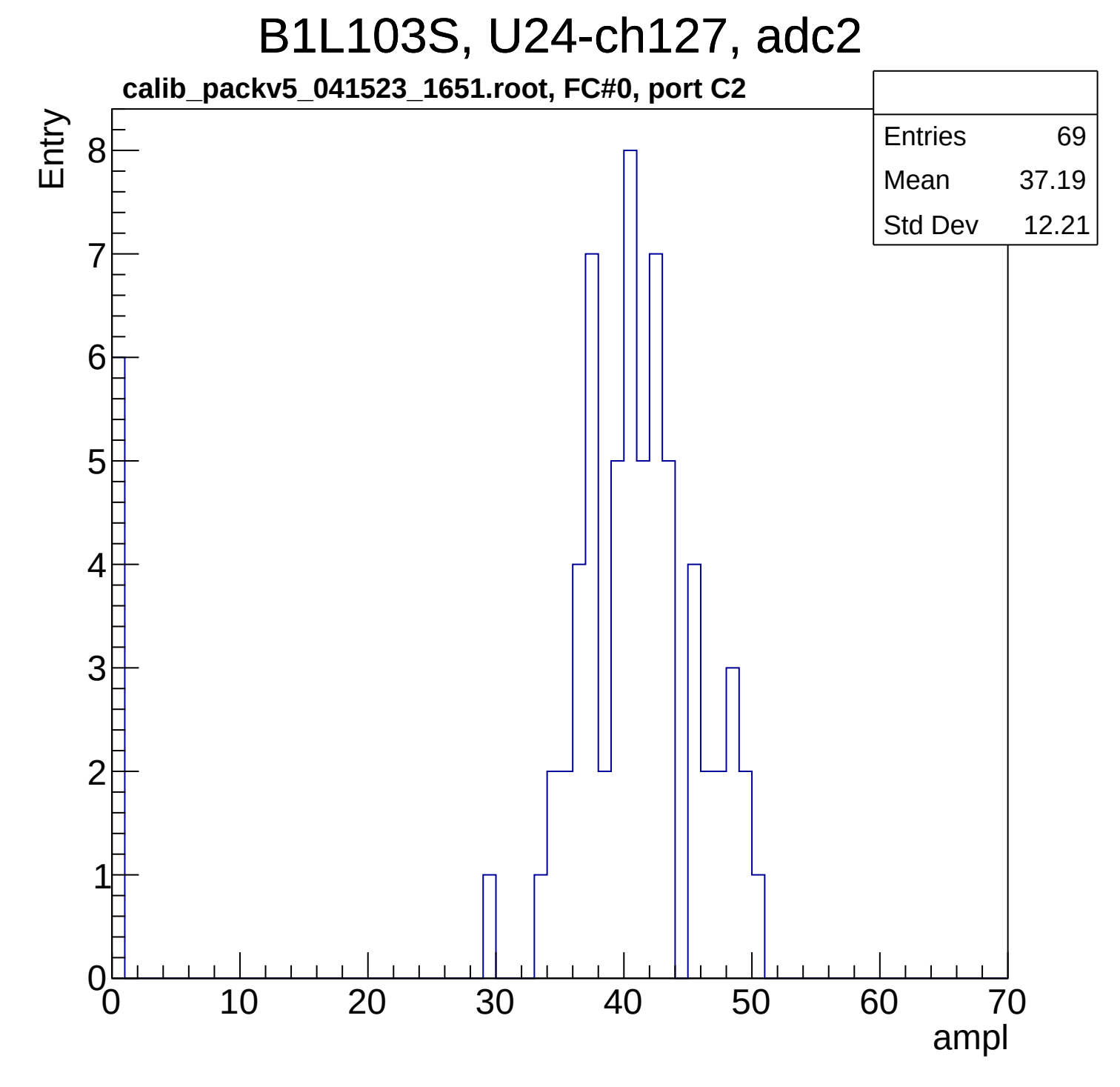
2
4
6
8
10
12
0
10
20
30
40
50
60
70


B1L103S, U24-ch127, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 33.93
Std Dev 5.714
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U24-ch127, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 37.19
Std Dev 12.21
Entry
ampl
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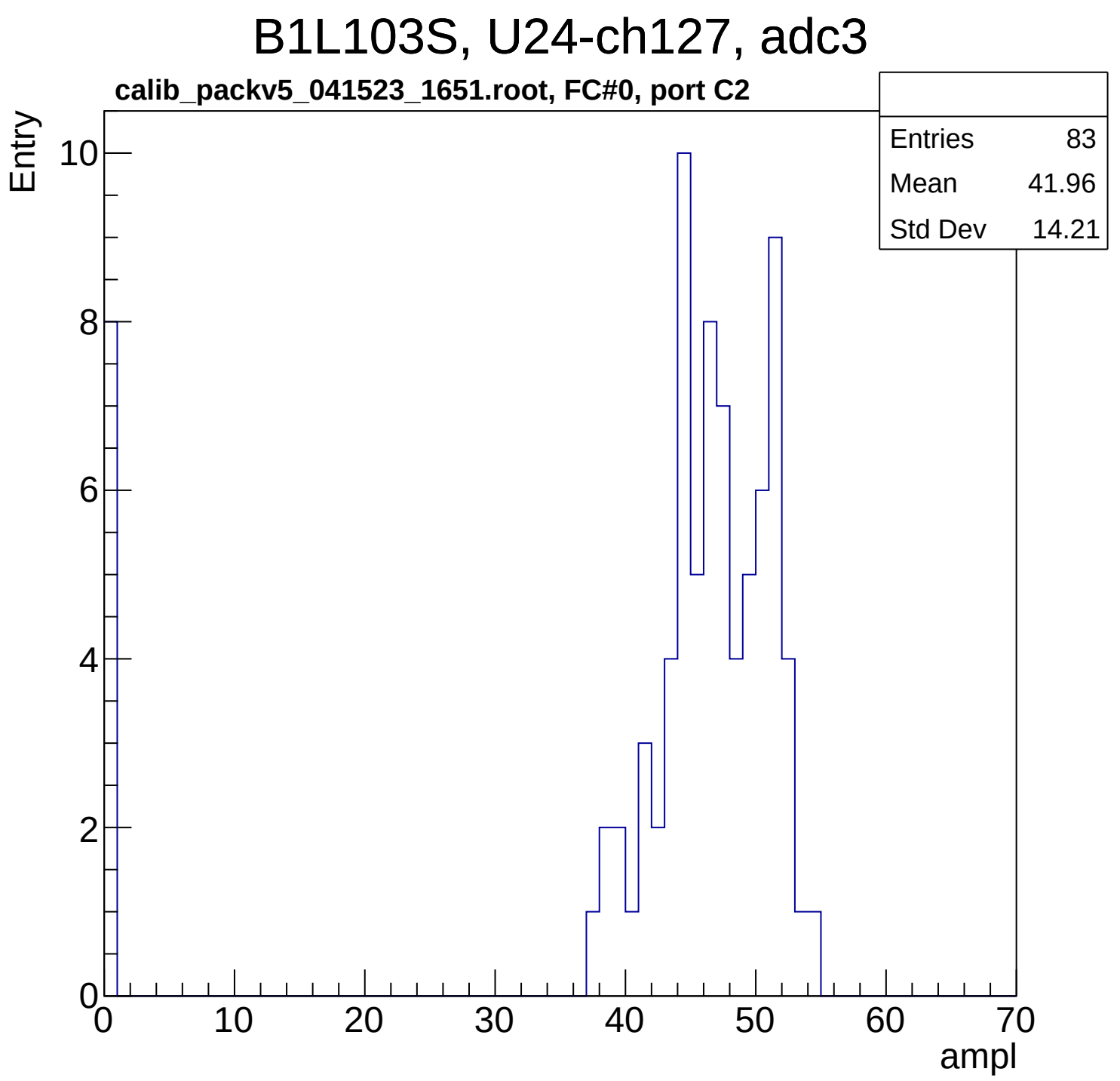
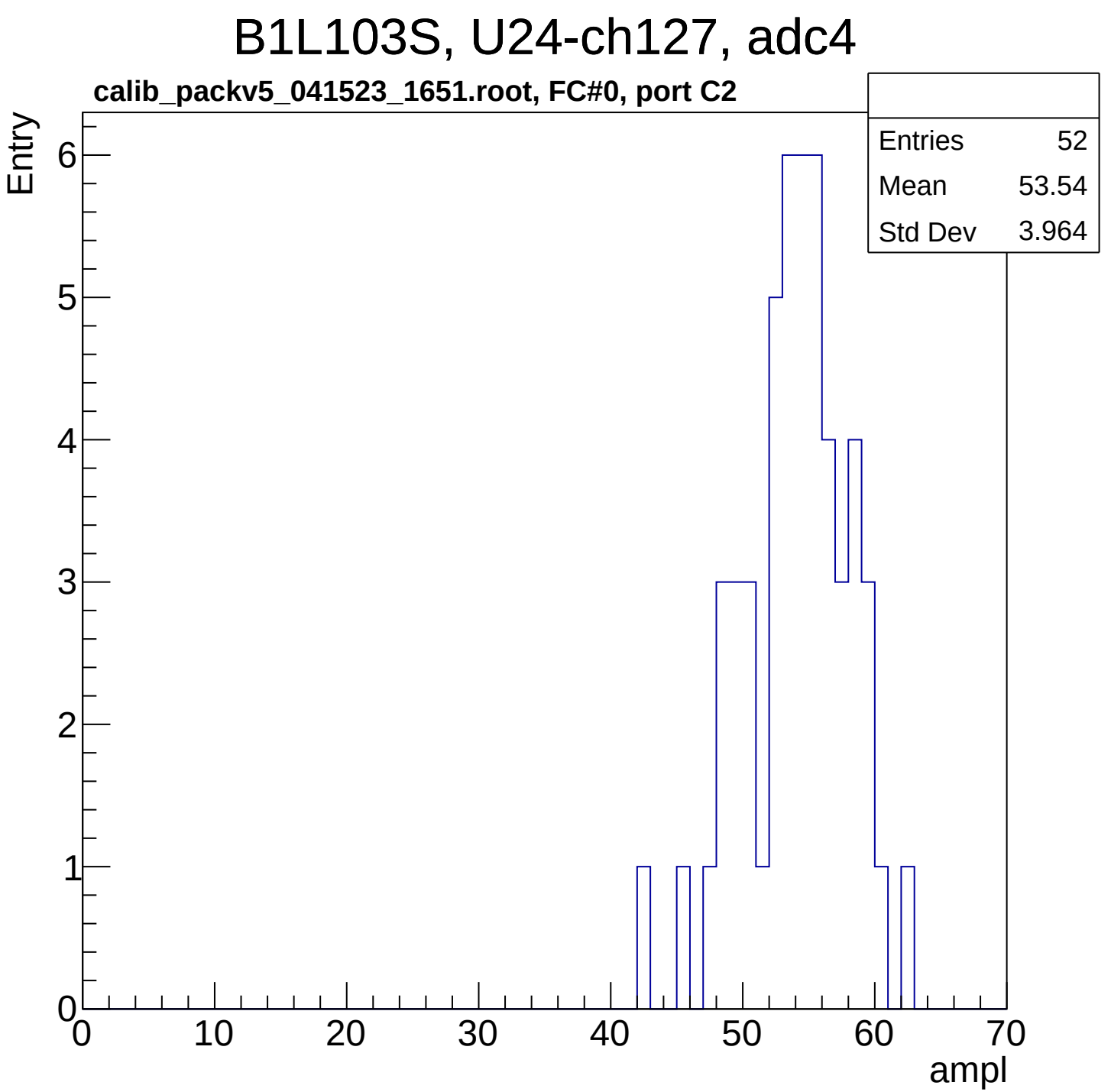
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U24-ch127, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 41.96
Std Dev 14.21
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U24-ch127, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 53.54
Std Dev 3.964
Entry
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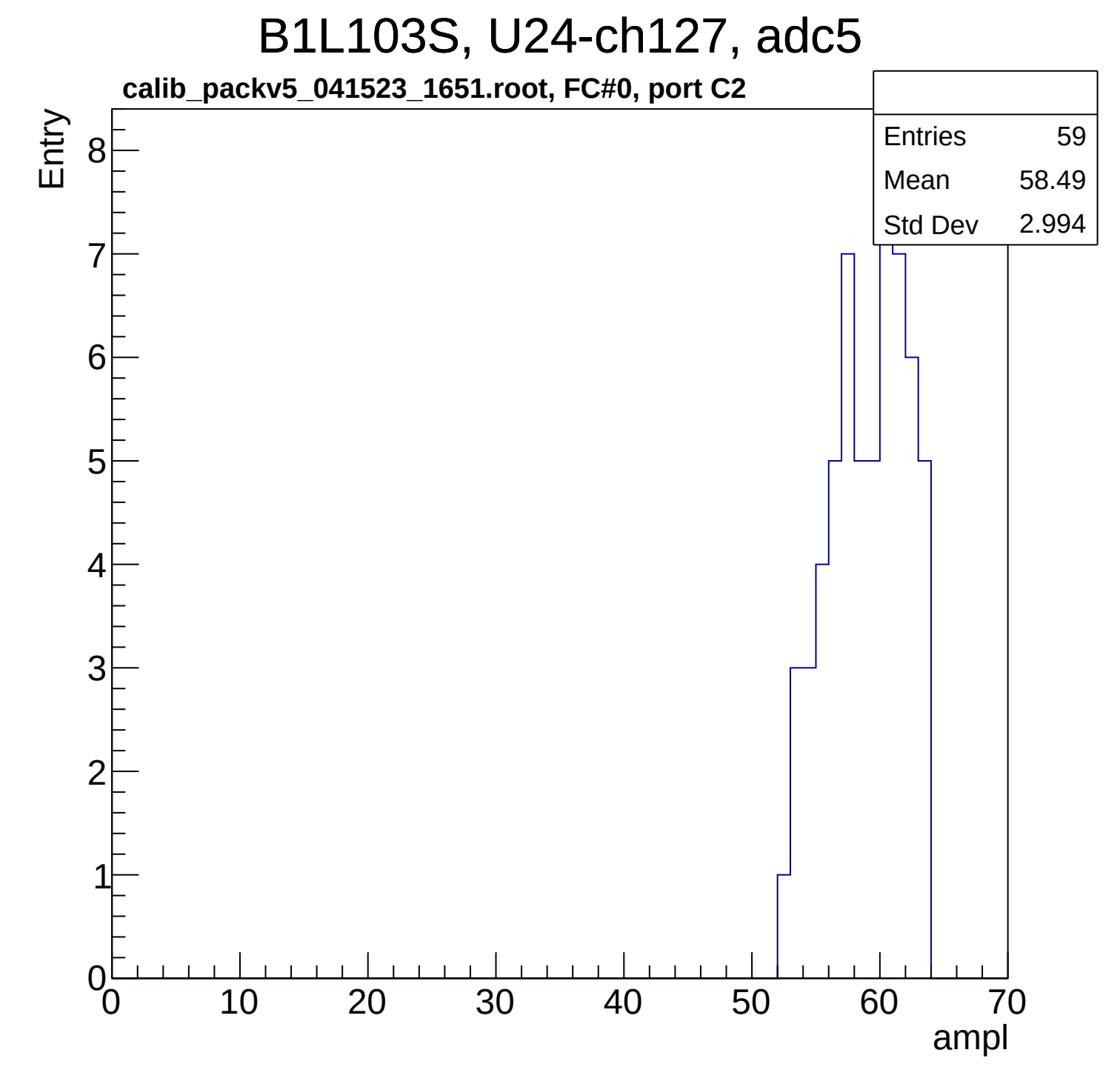
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U24-ch127, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 58.49
Std Dev 2.994
Entry
ampl
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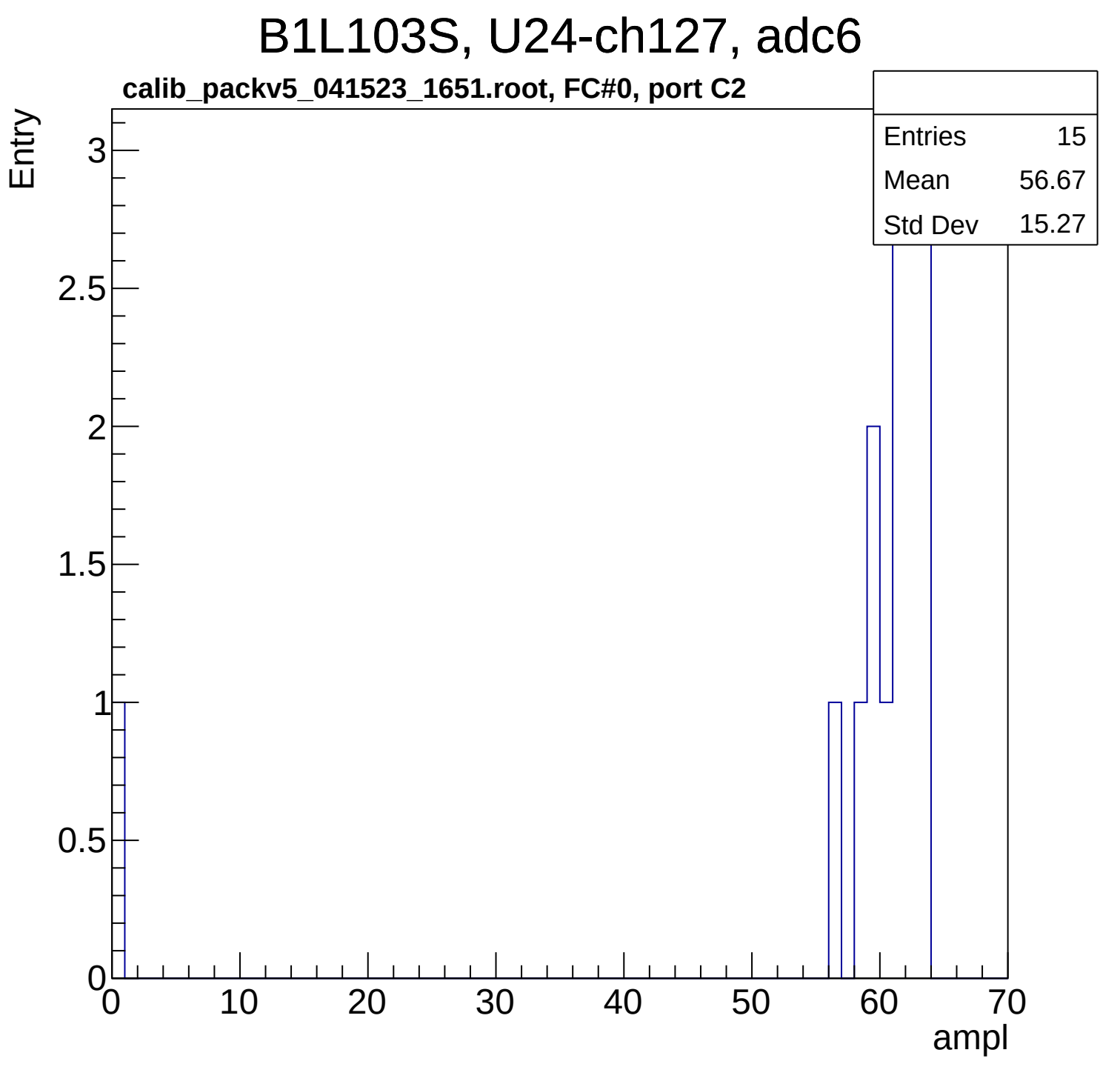
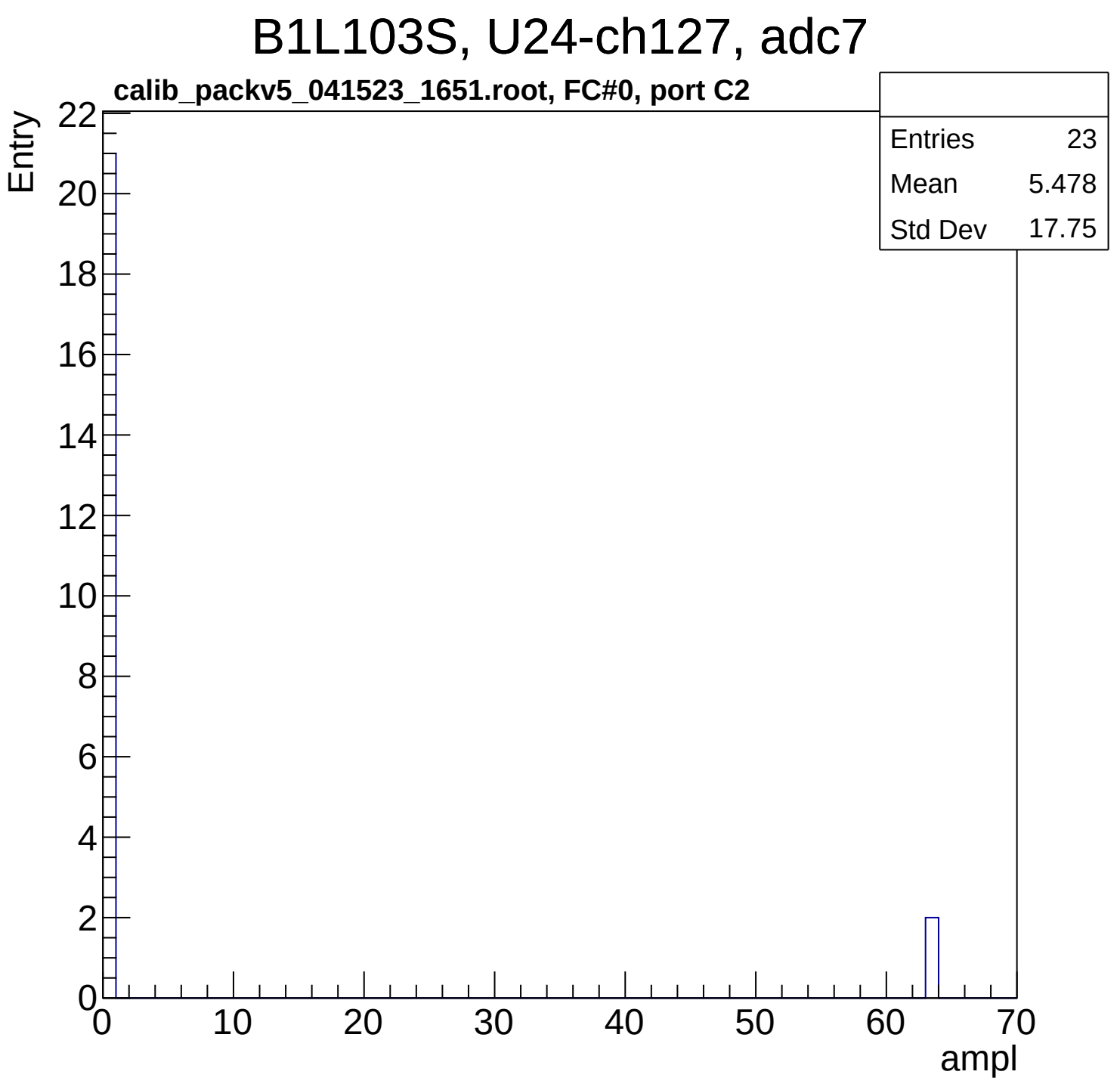
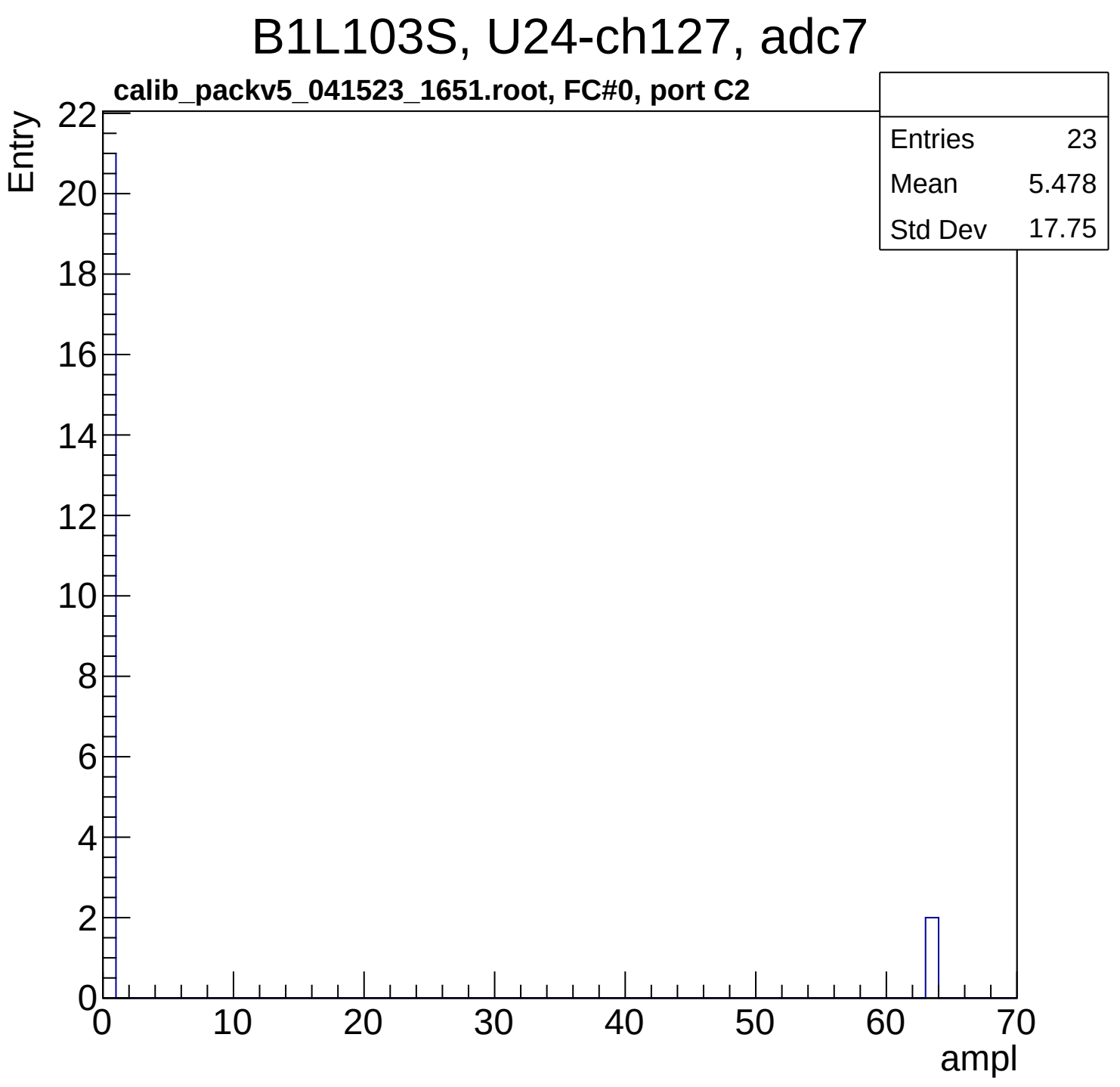
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U24-ch127, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 15
Mean 56.67
Std Dev 15.27
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U24-ch127, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 23
Mean 5.478
Std Dev 17.75
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
22
0
10
20
30
40
50
60
70


B1L103S, U24-ch127, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 23
Mean 5.478
Std Dev 17.75
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
22
0
10
20
30
40
50
60
70