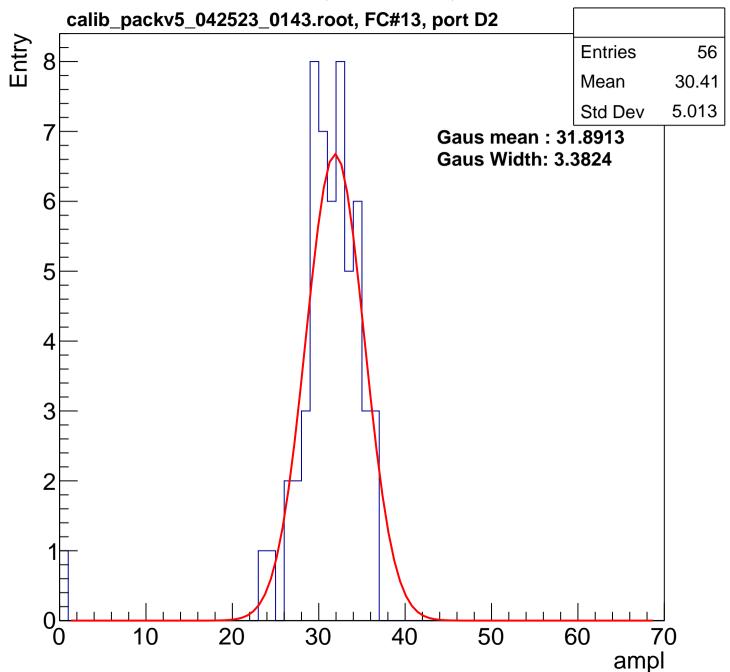
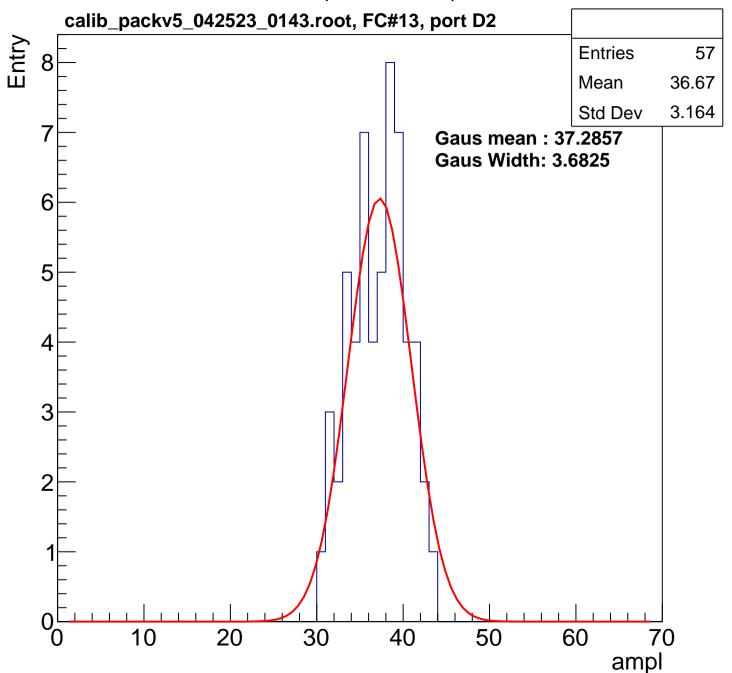
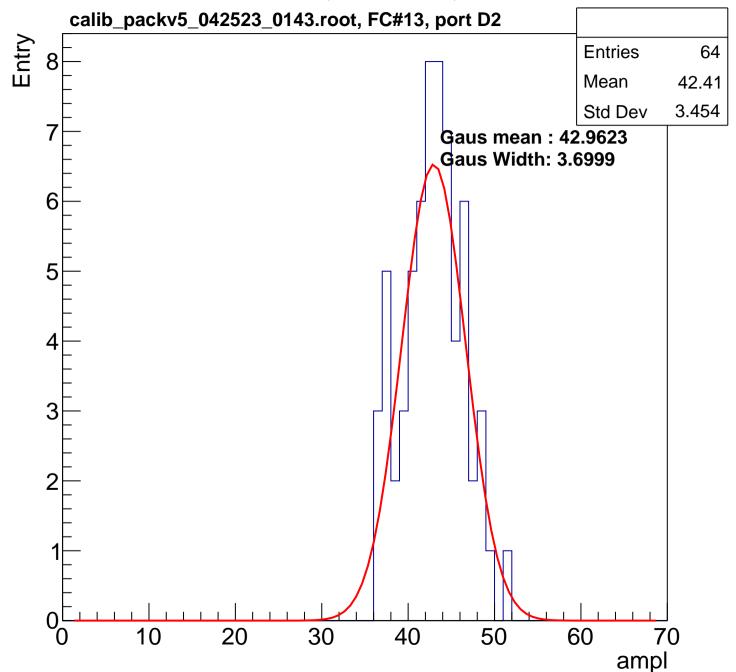
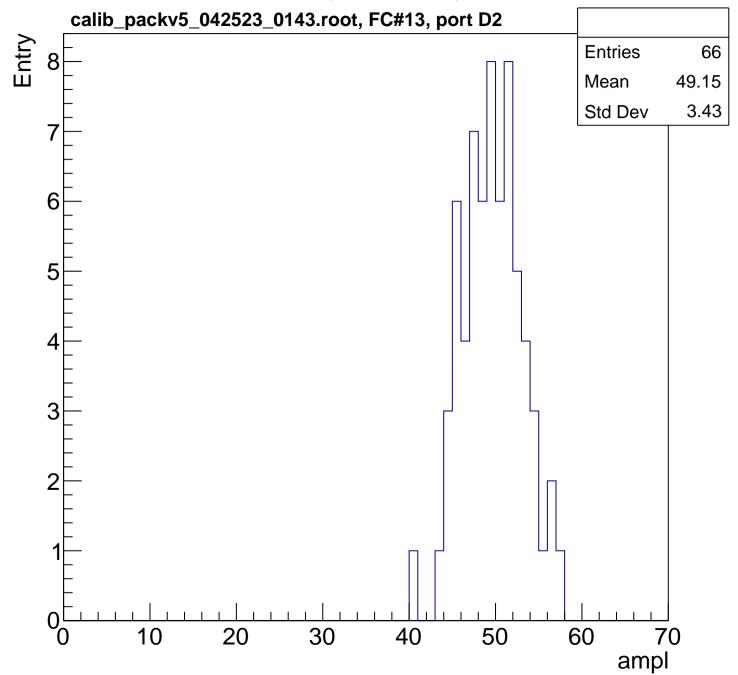


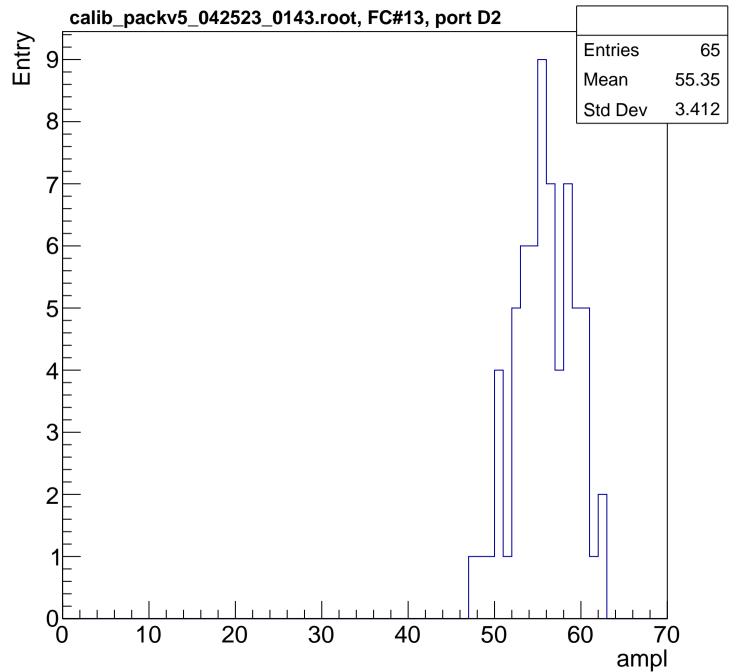
B1L003S, U4-ch3, adc7 calib_packv5_042523_0143.root, FC#13, port D2 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

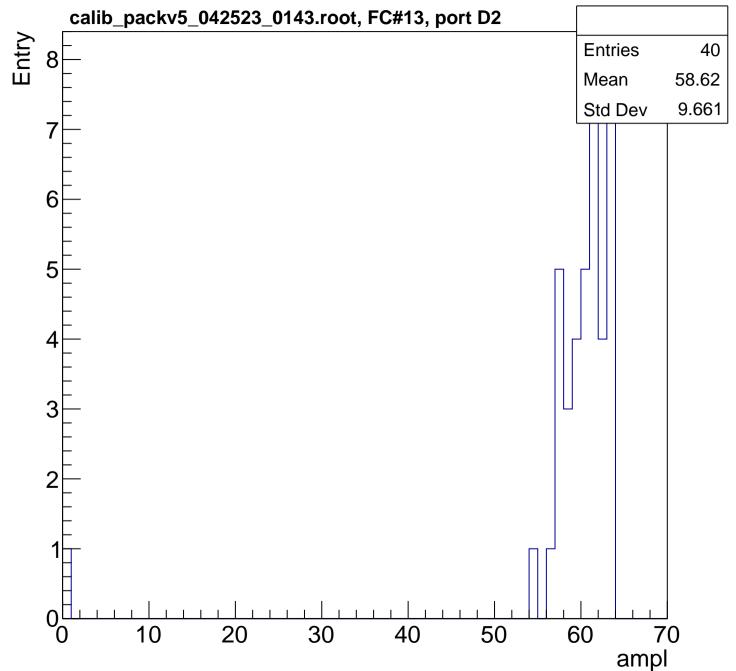


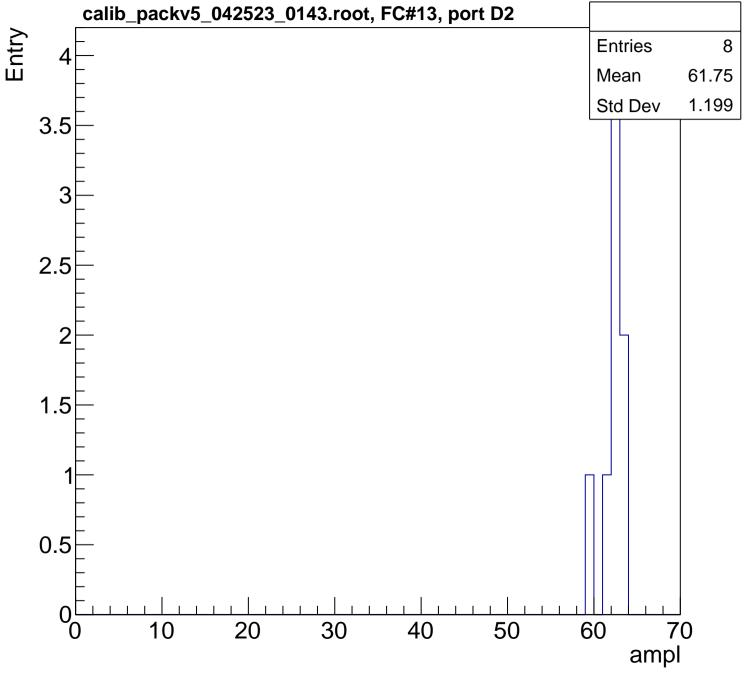




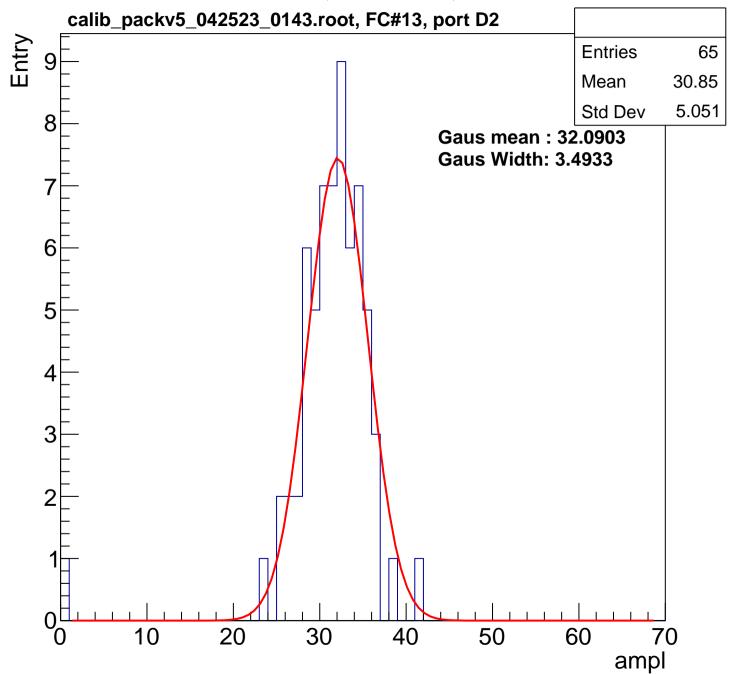


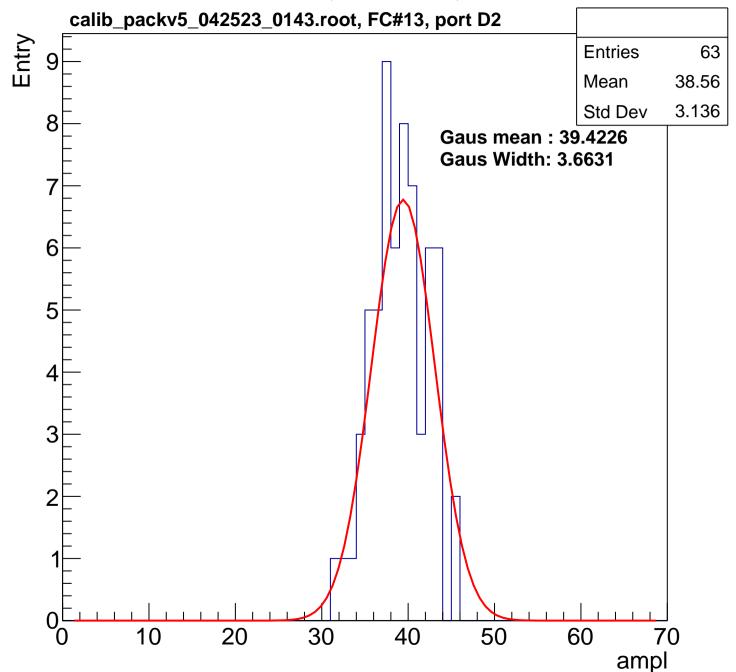


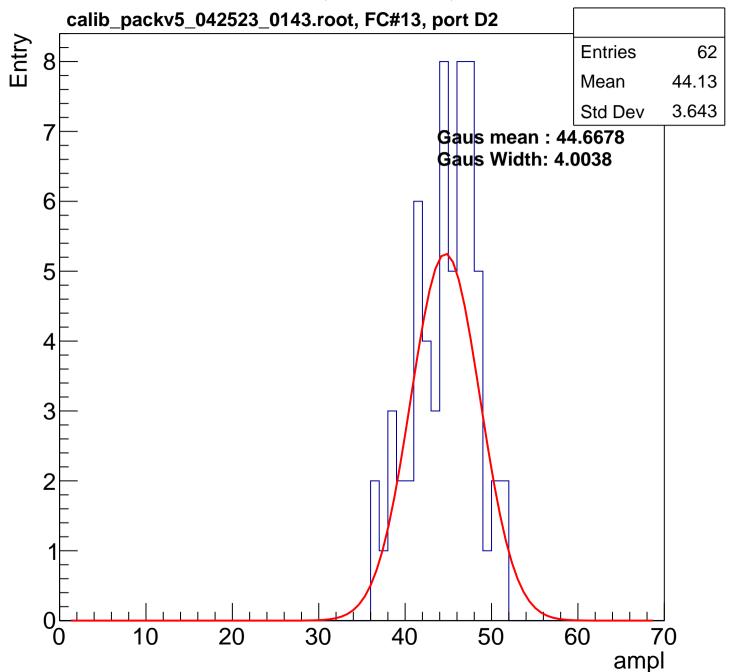


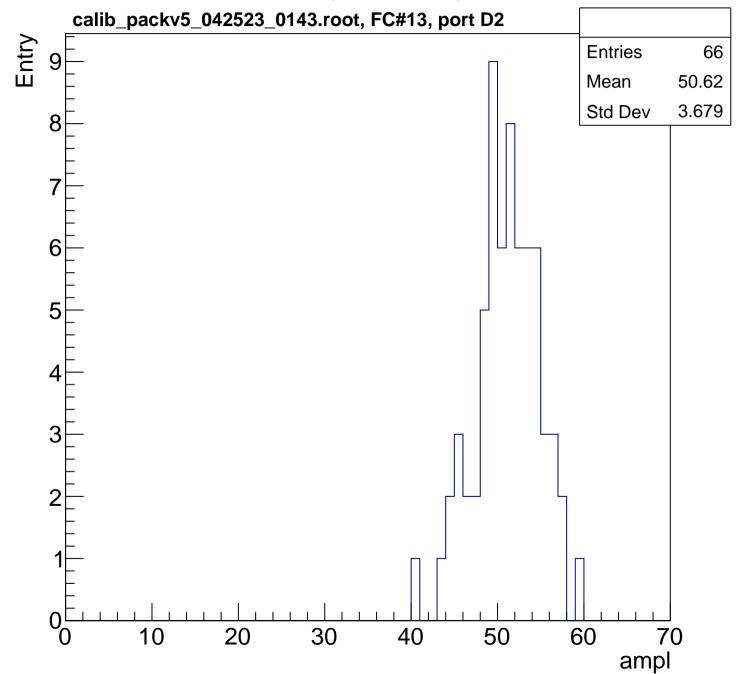


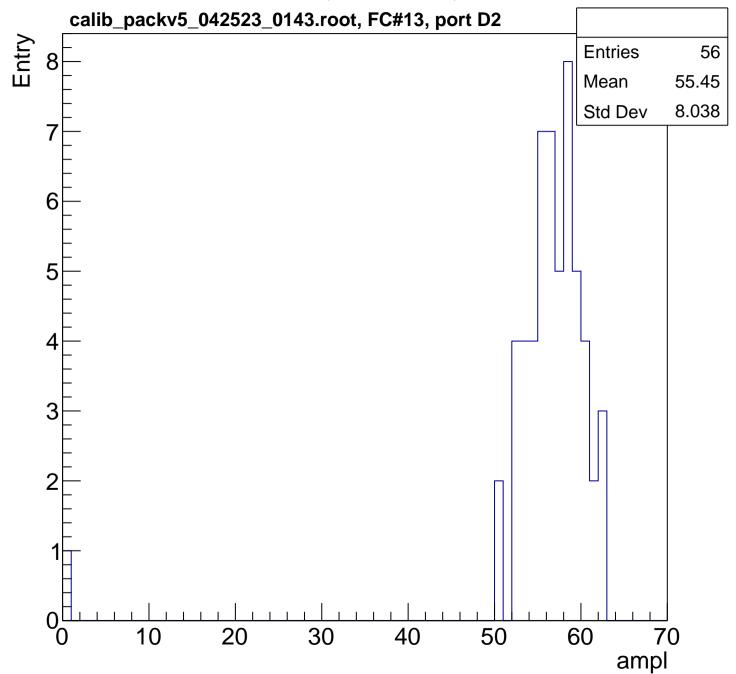
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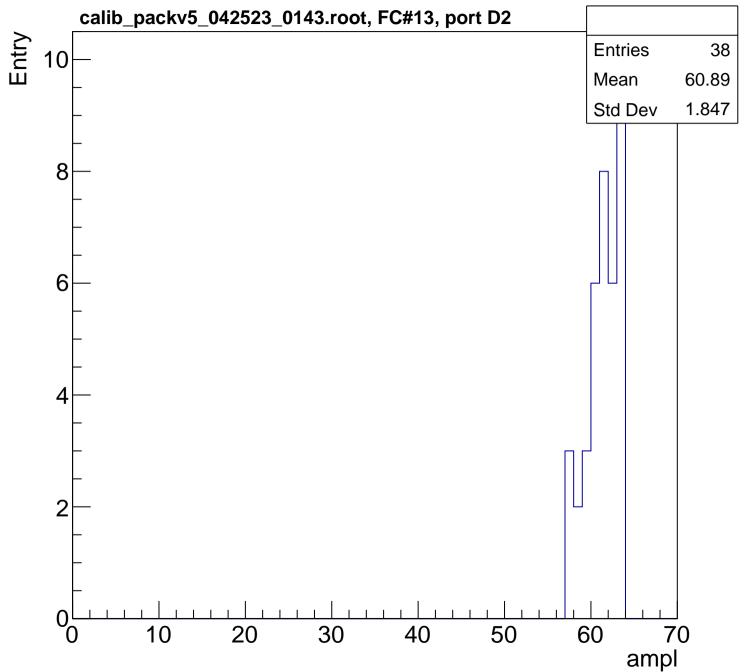


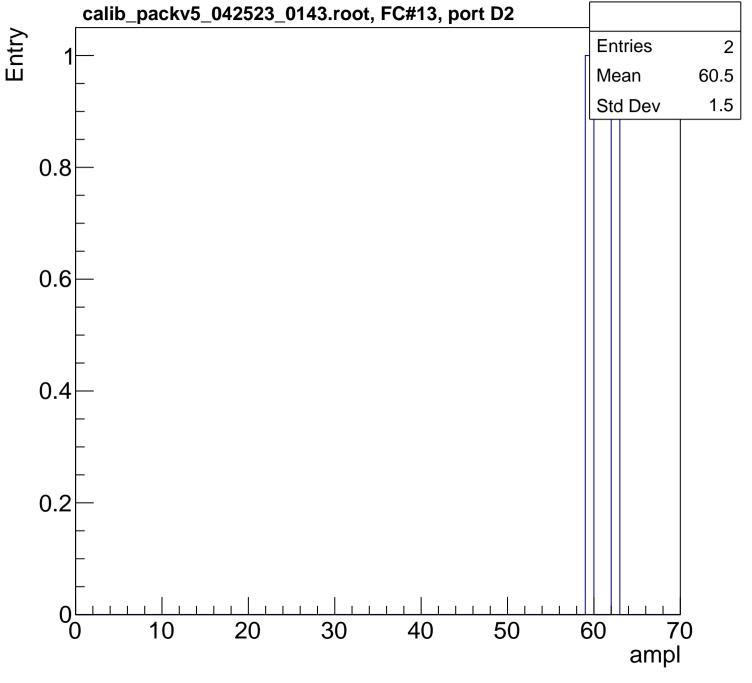


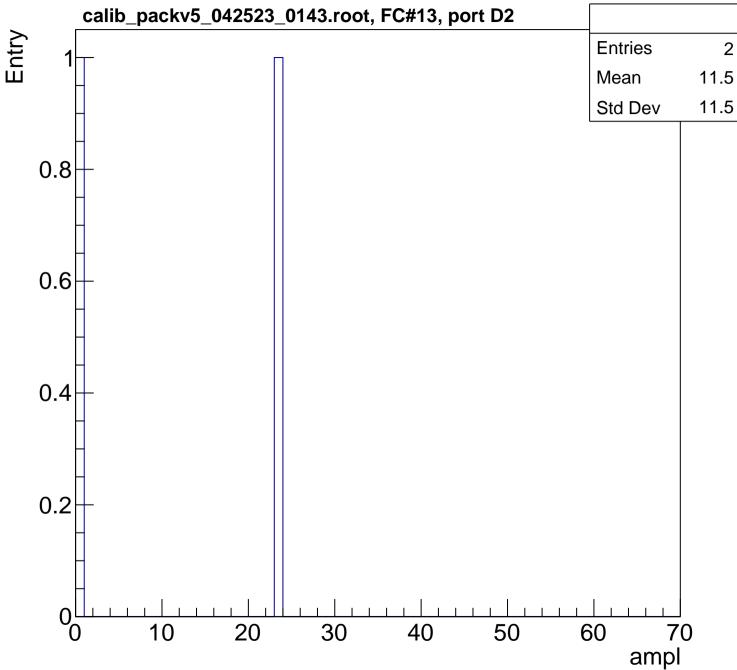


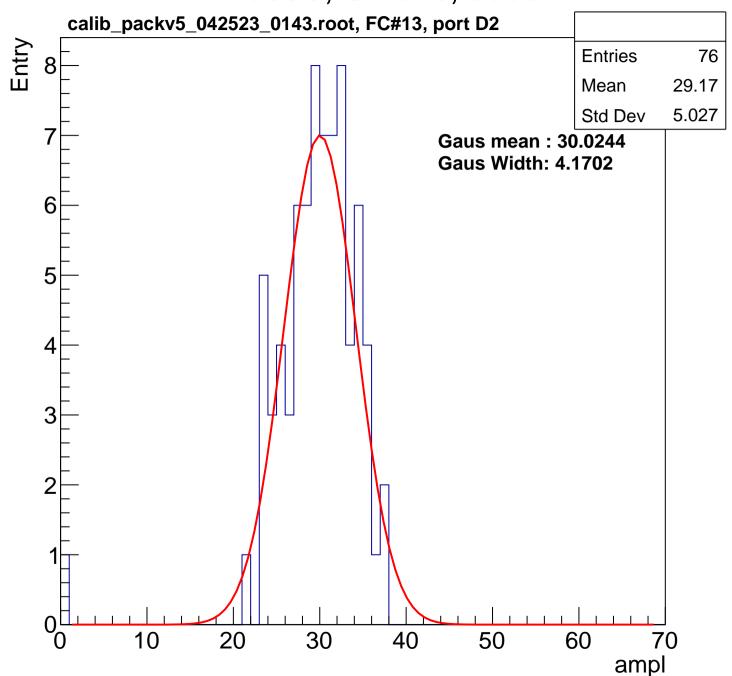


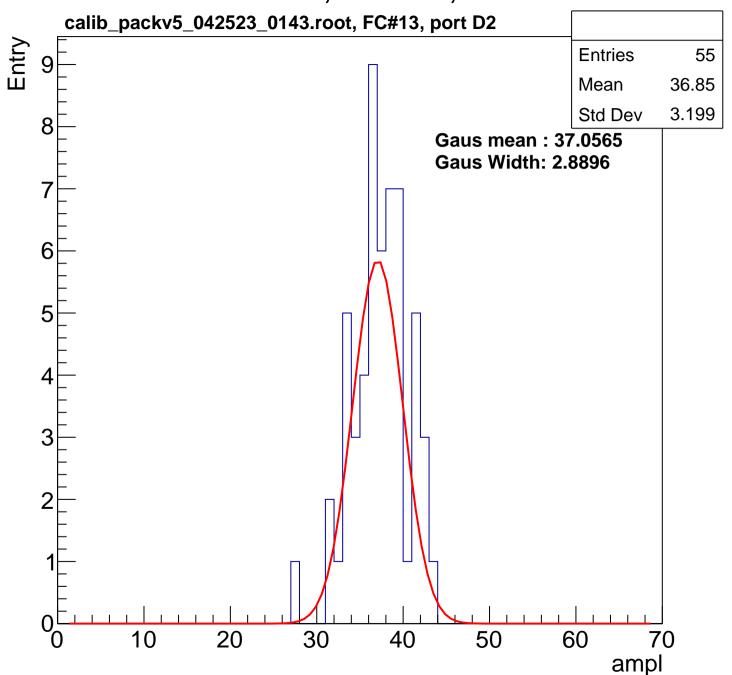


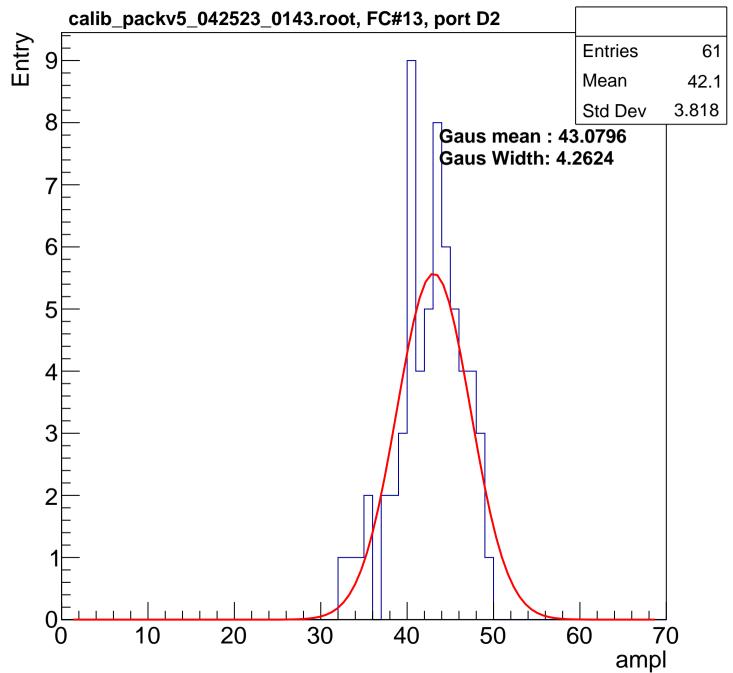


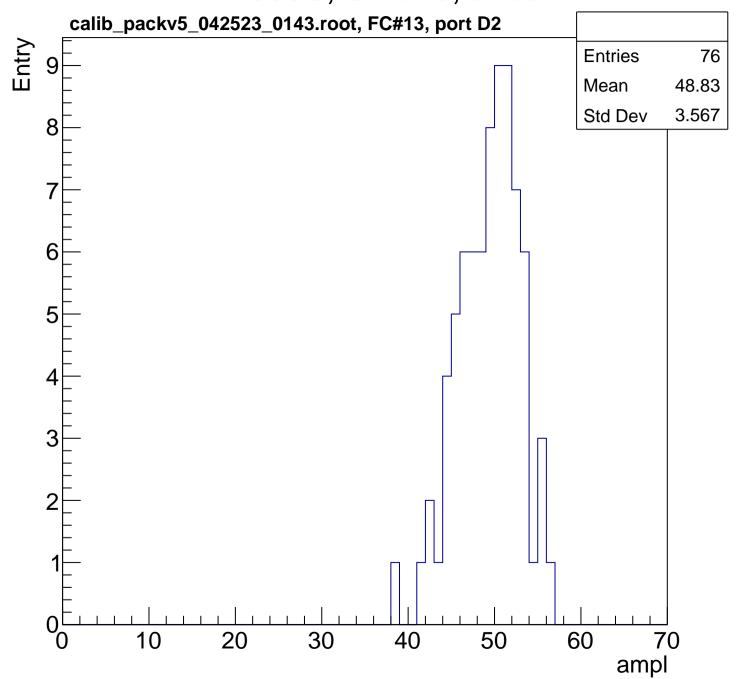


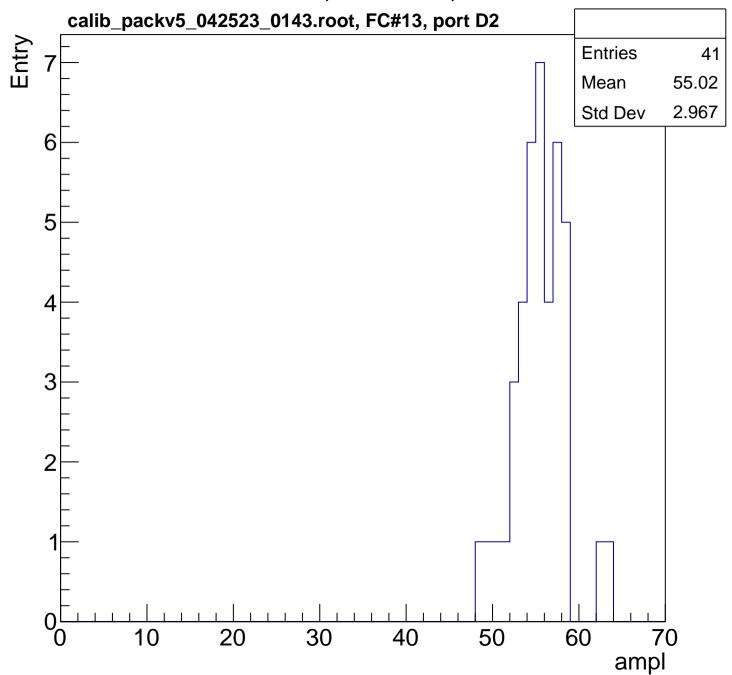


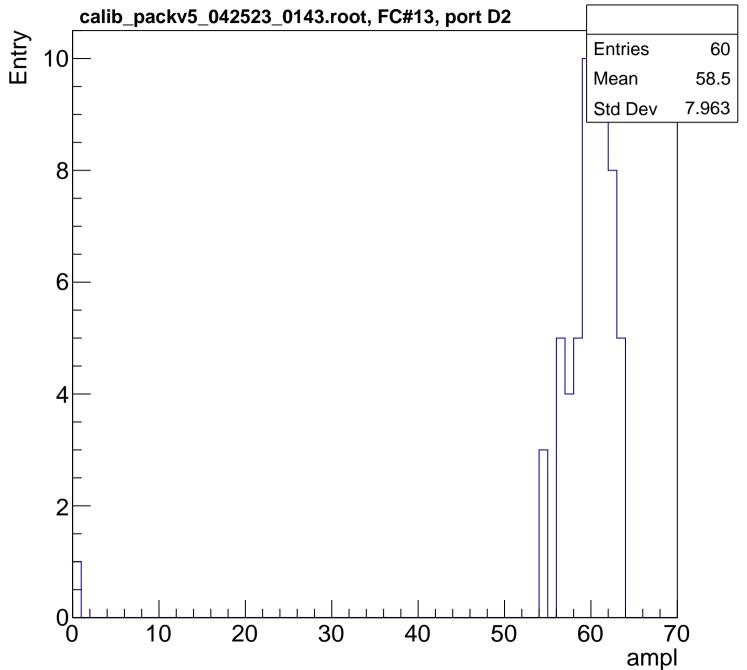


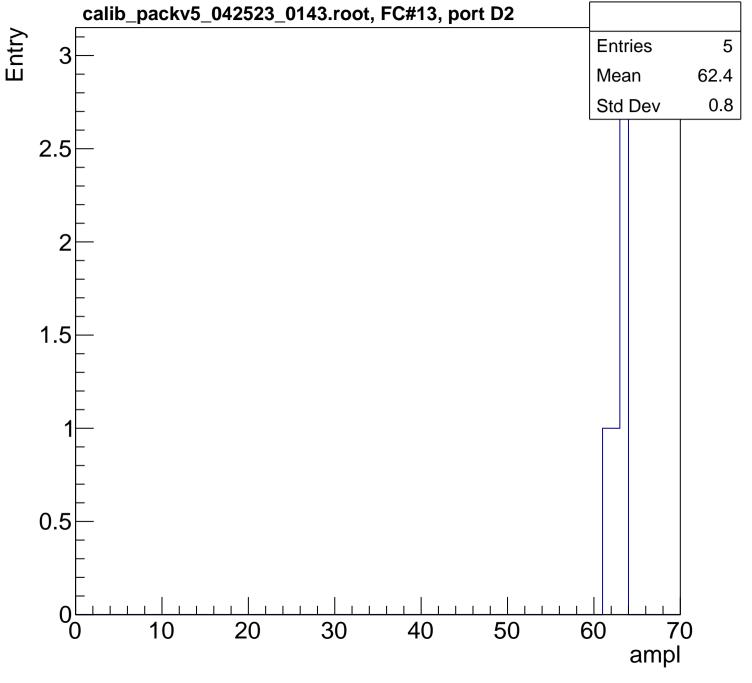




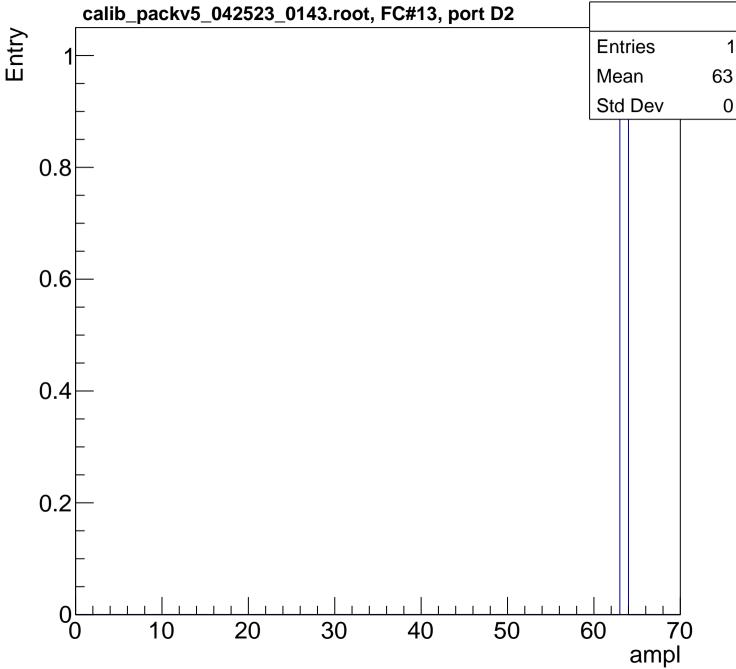


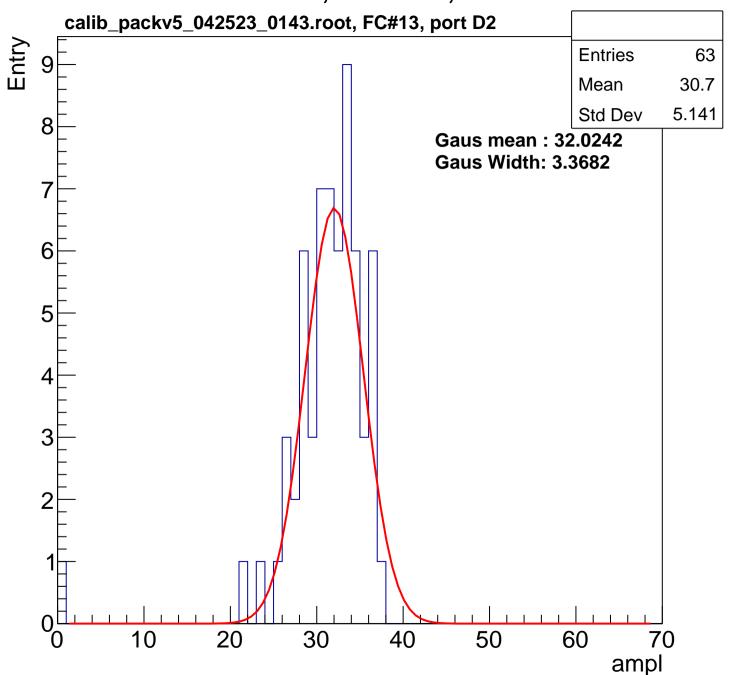


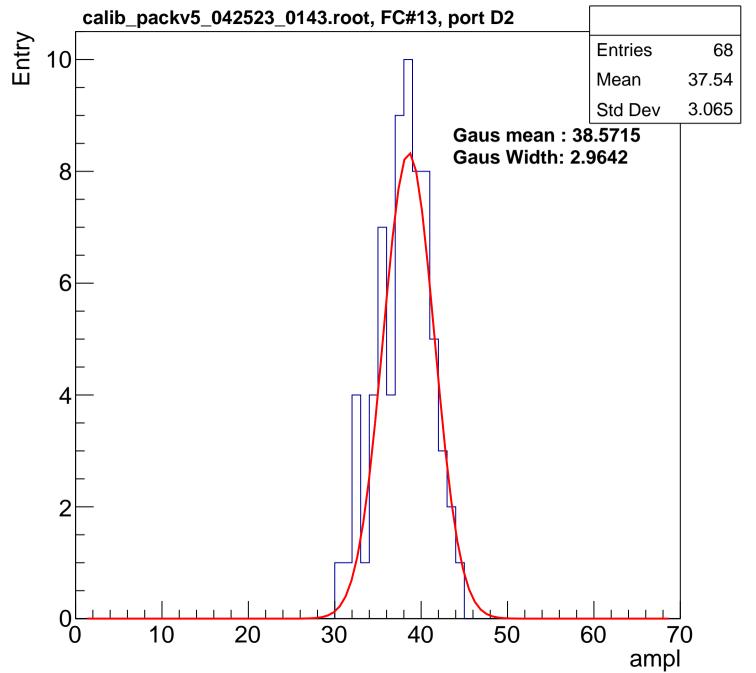


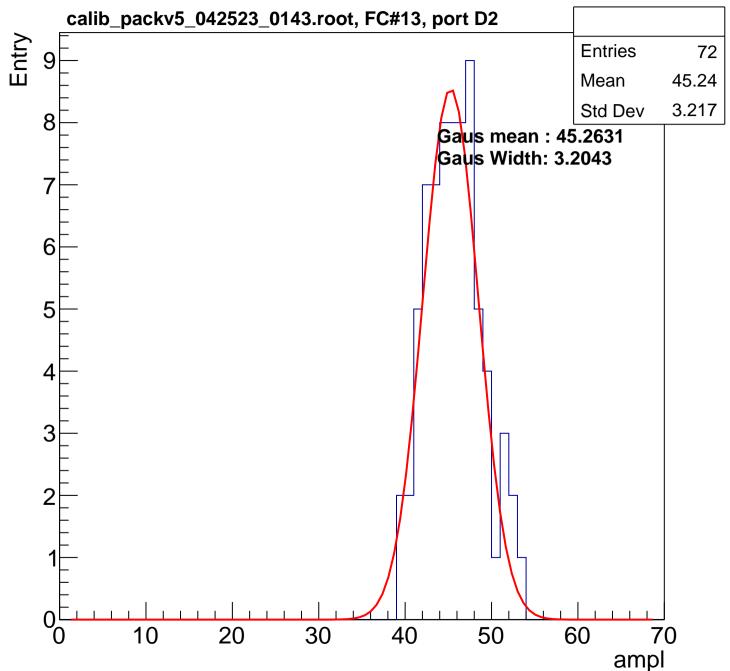


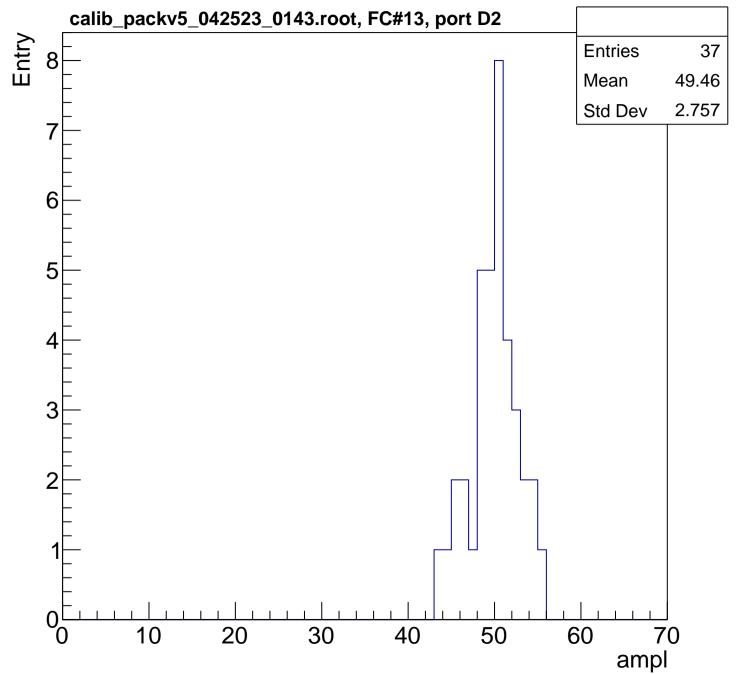
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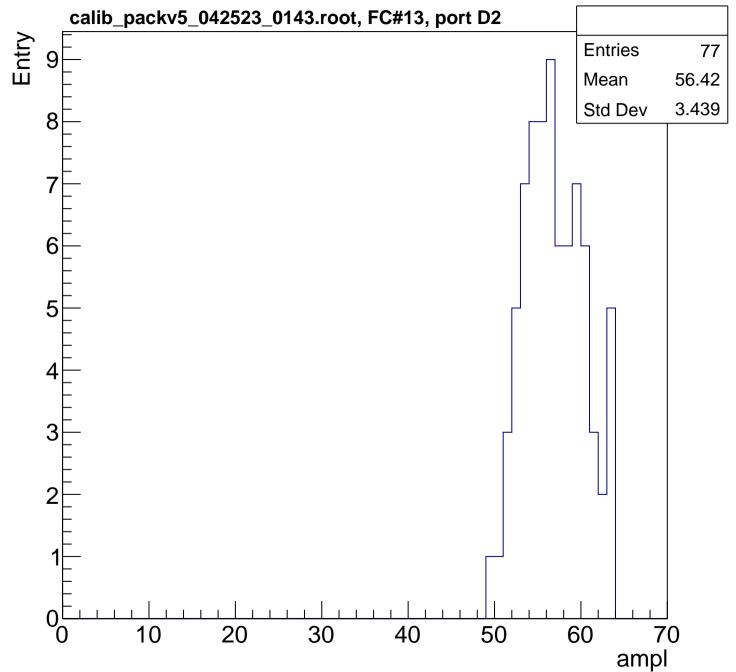


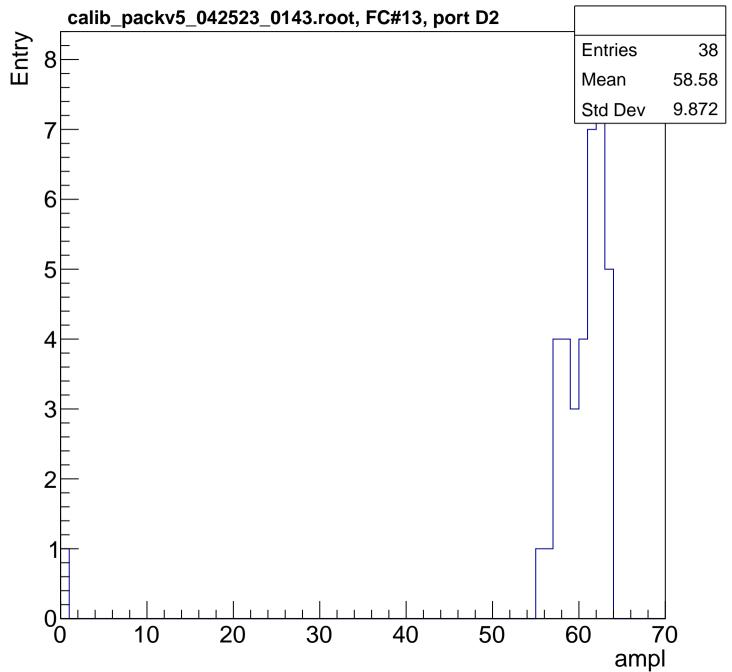


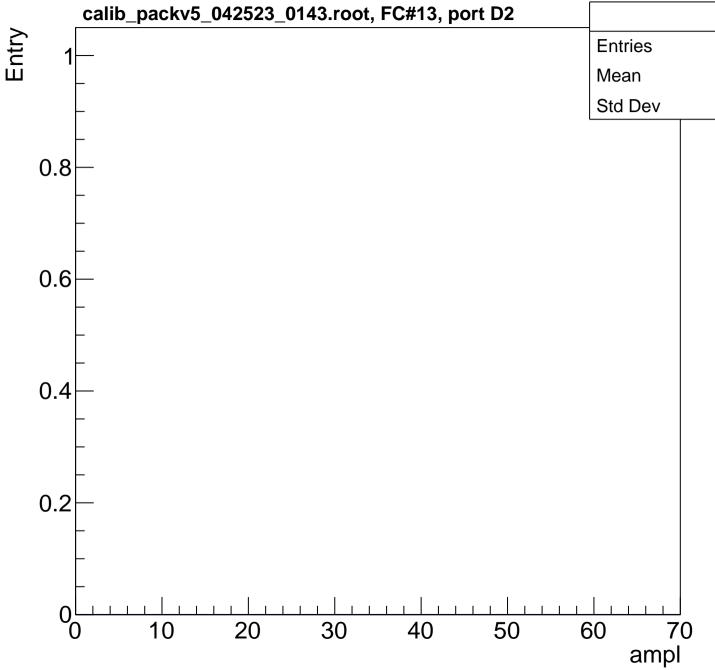




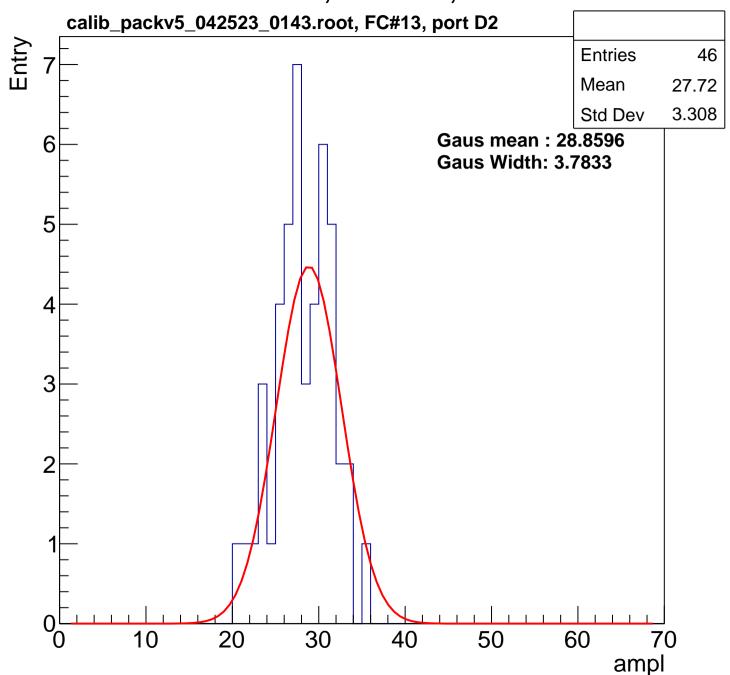


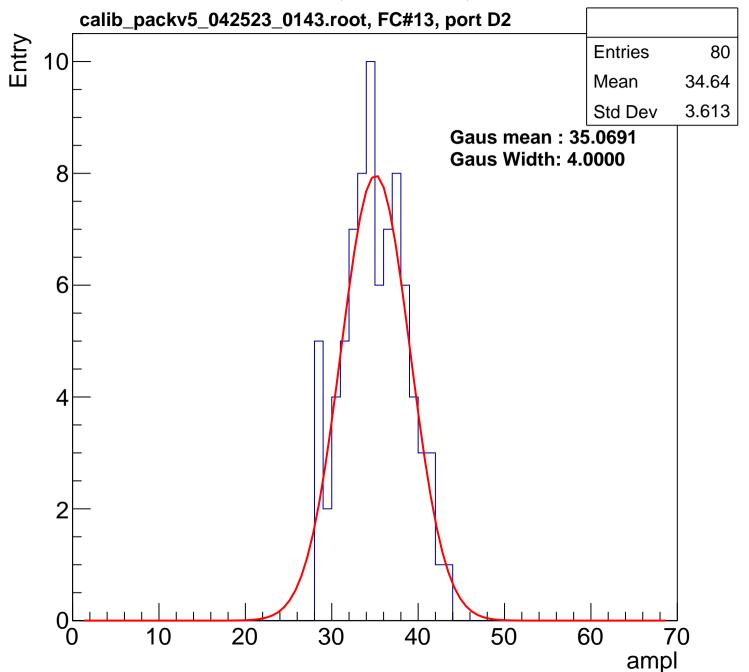


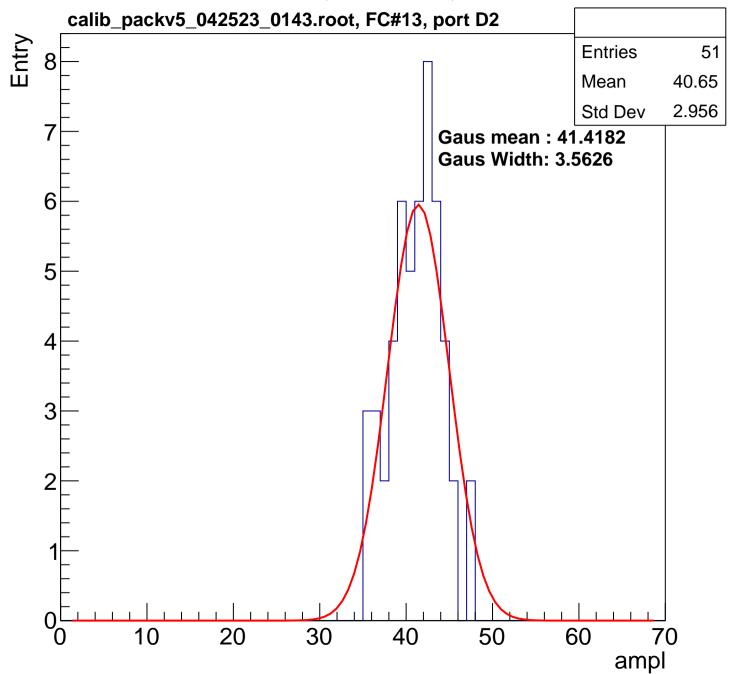


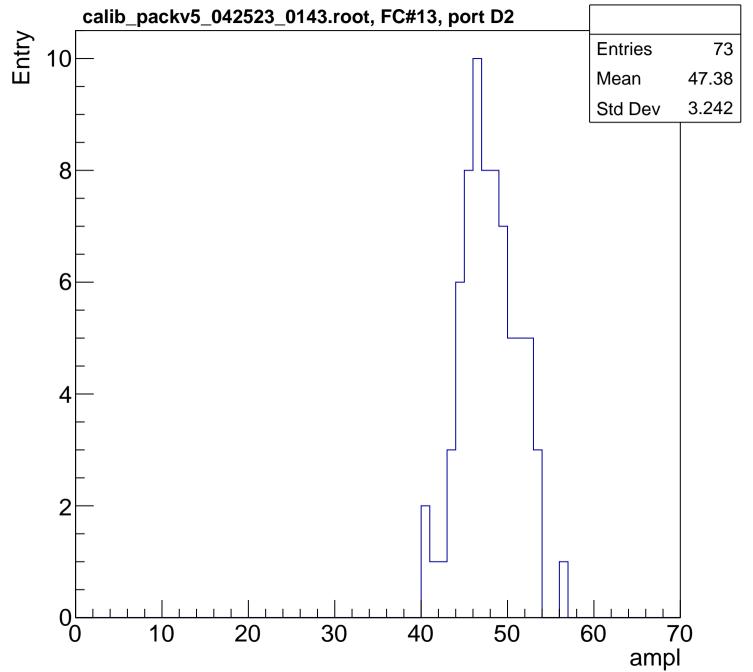


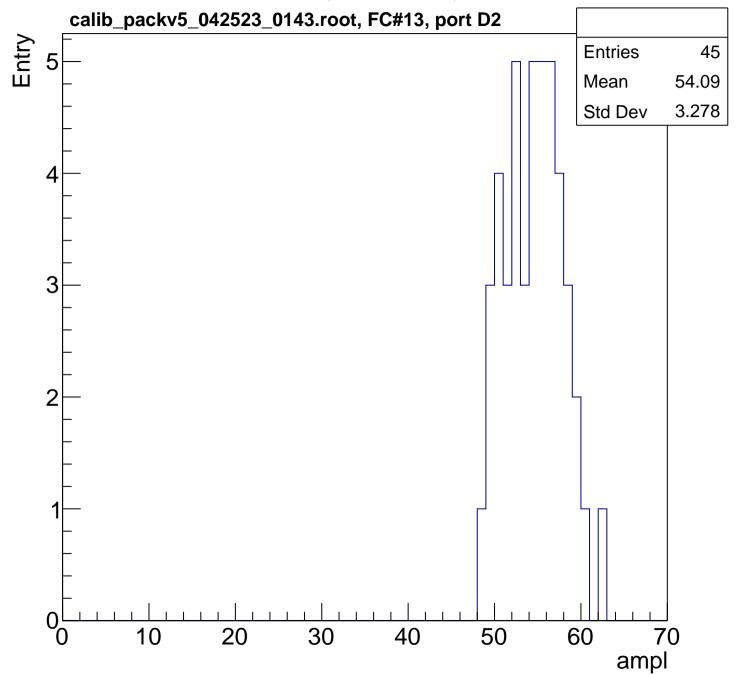
B1L003S, U4-ch7, adc7 calib_packv5_042523_0143.root, FC#13, port D2 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

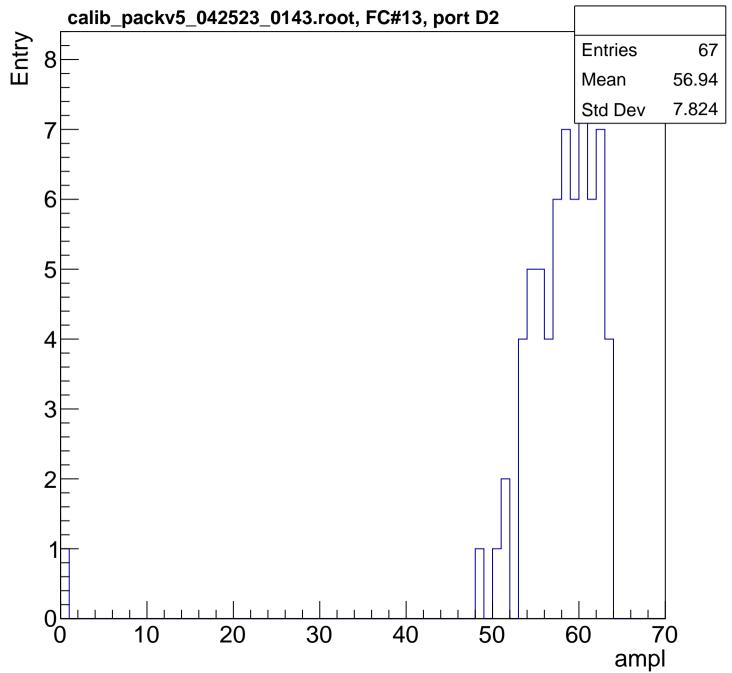


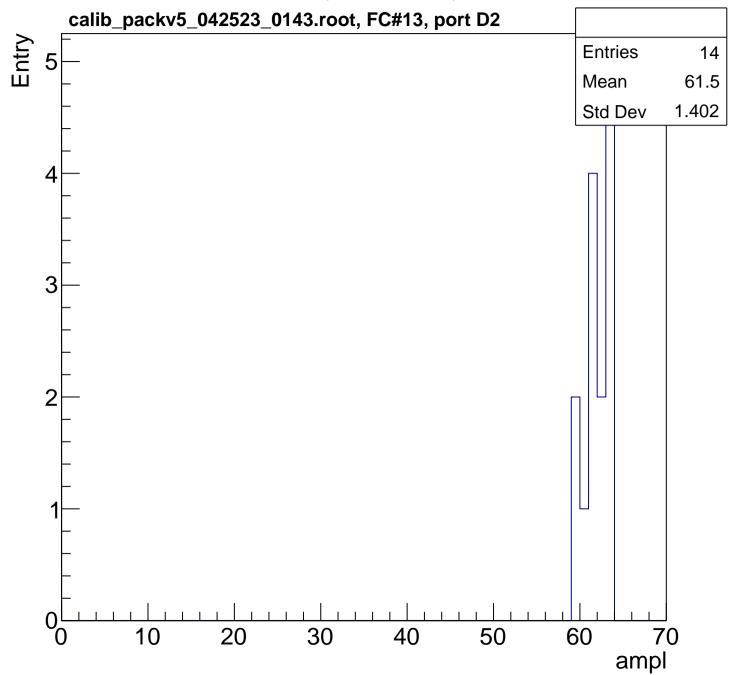


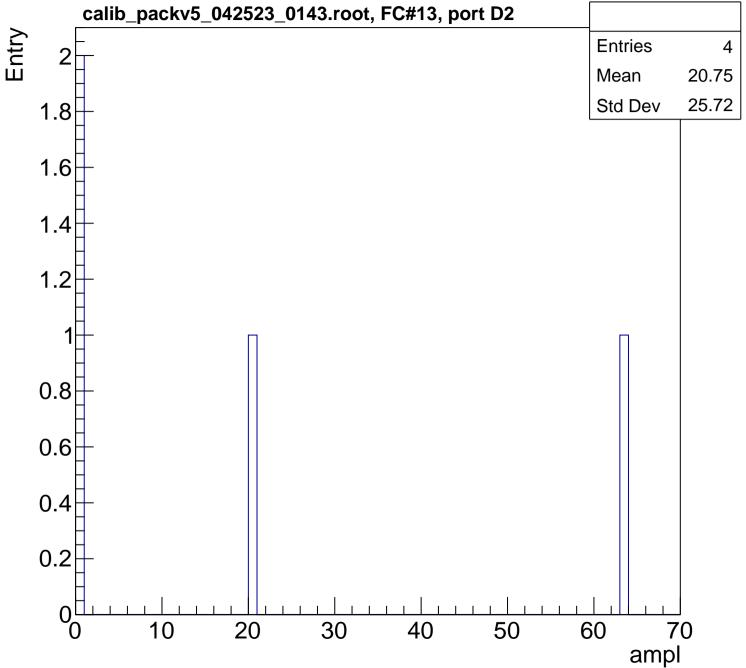


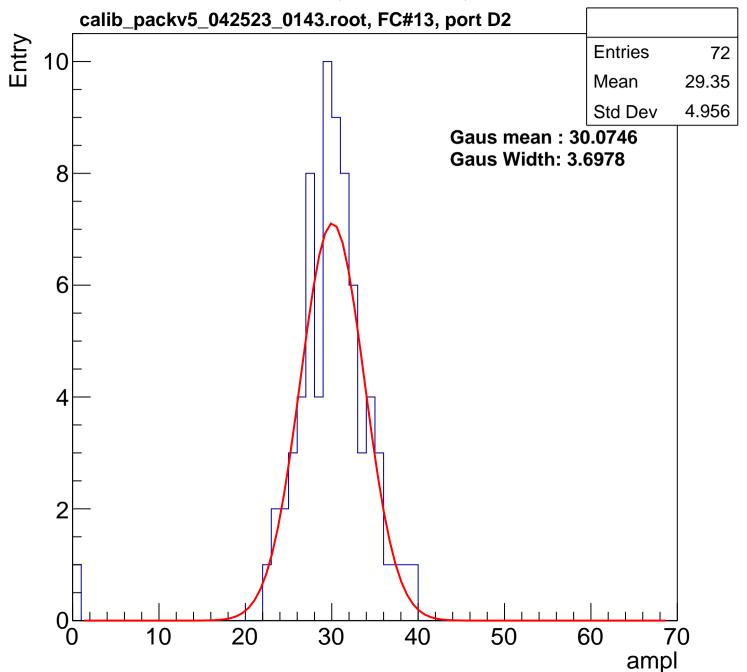


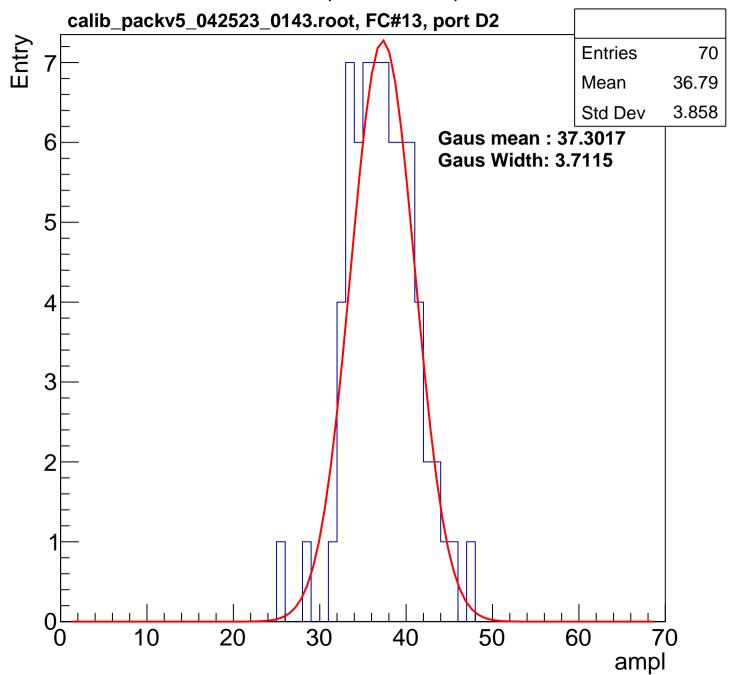


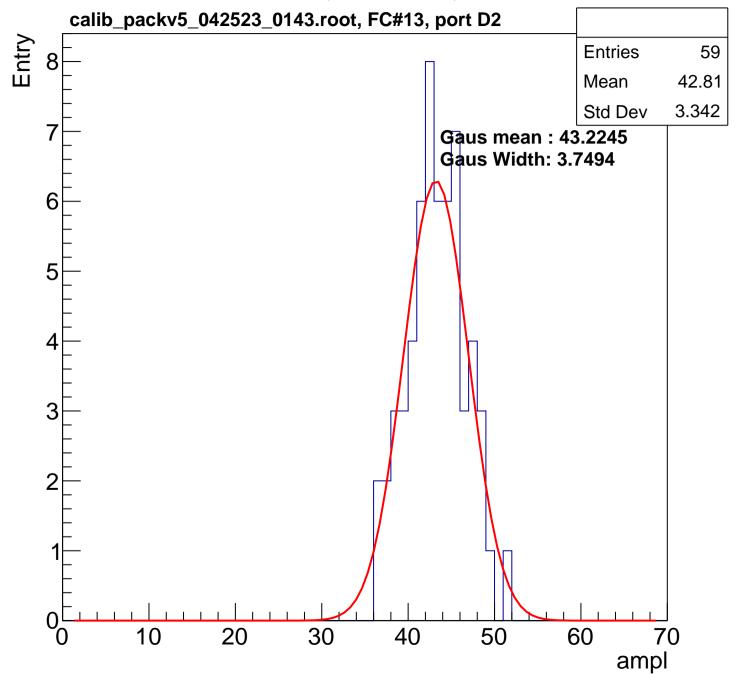


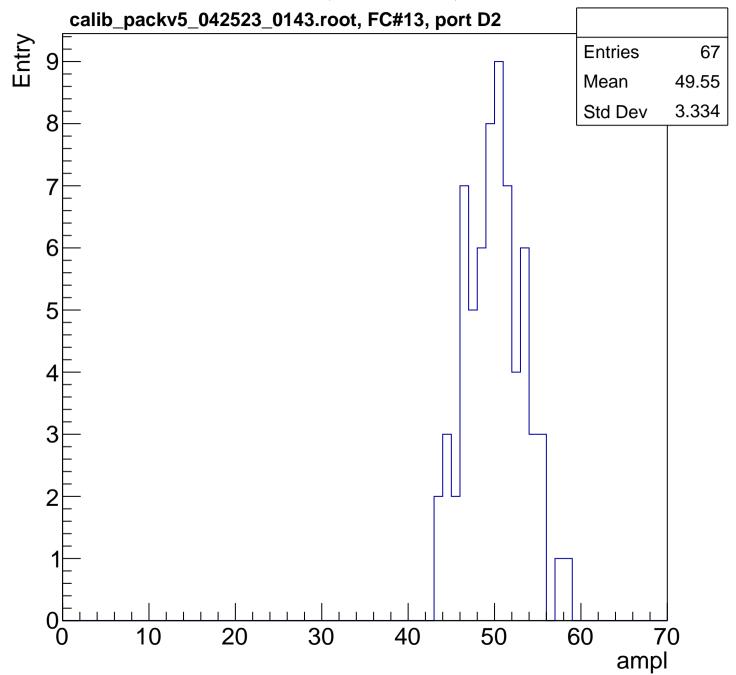


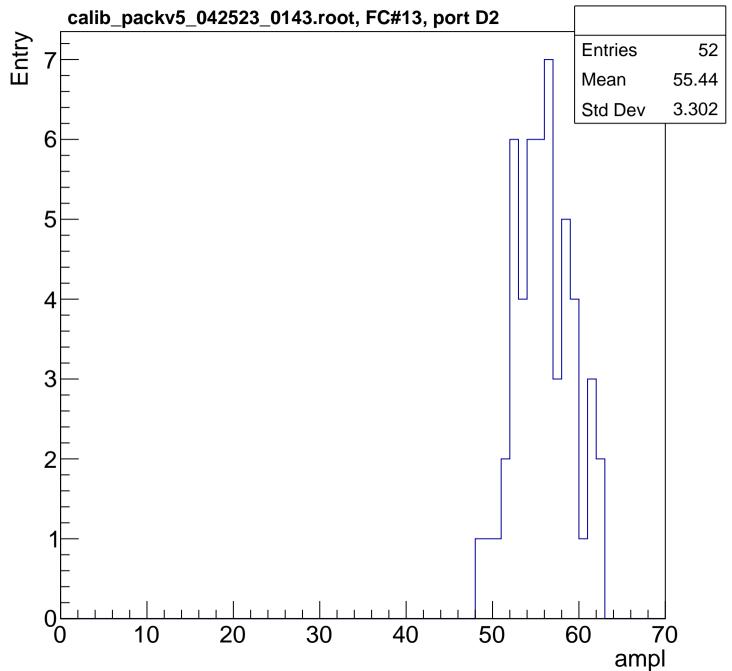


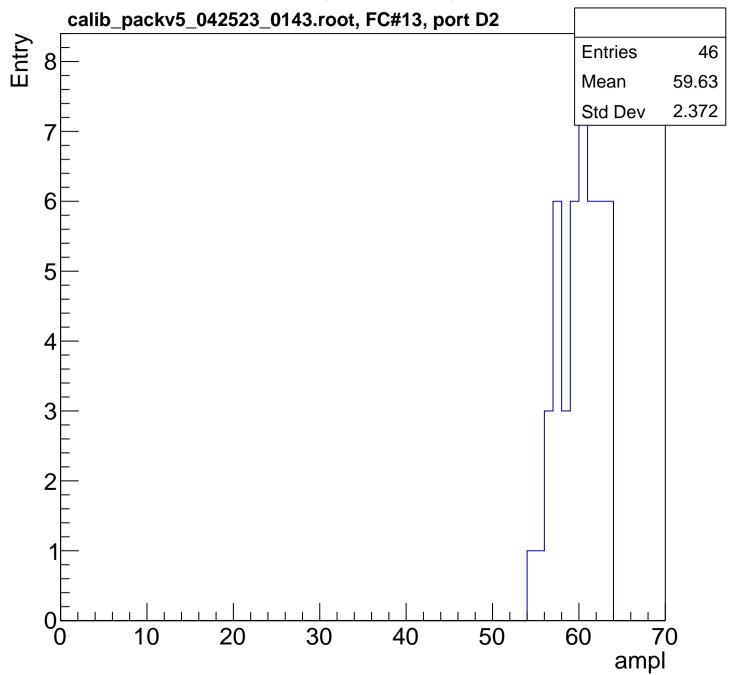


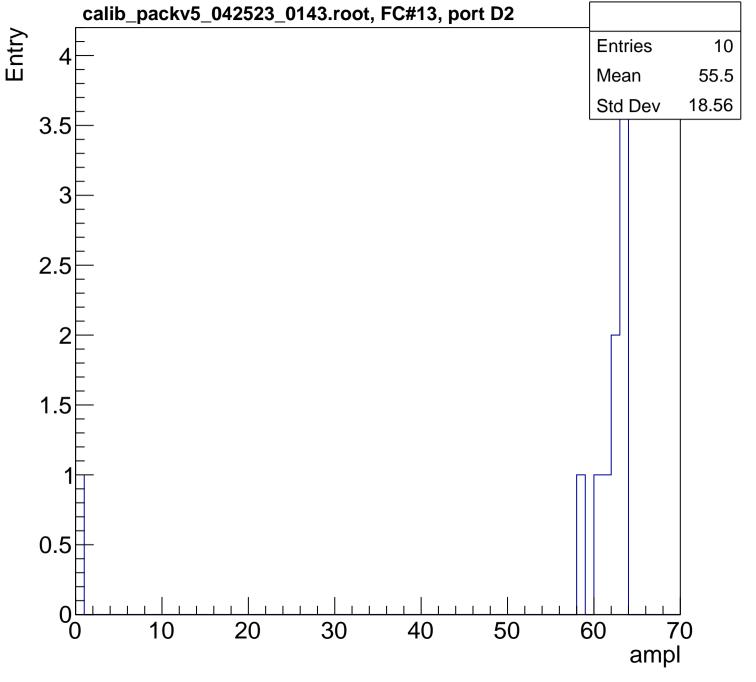


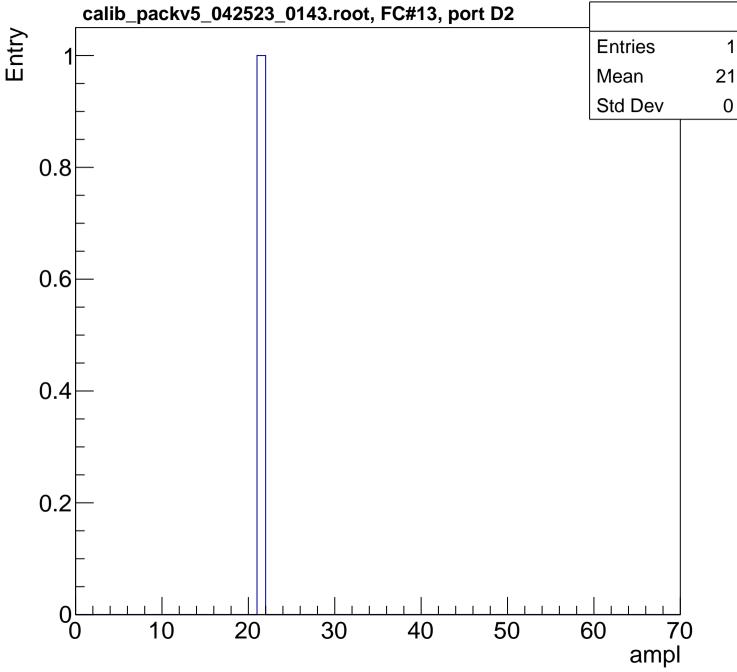


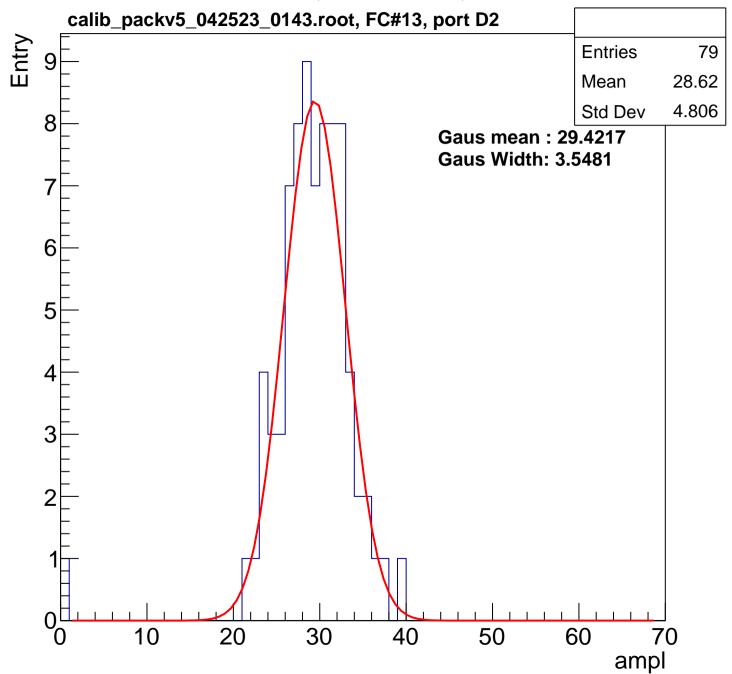


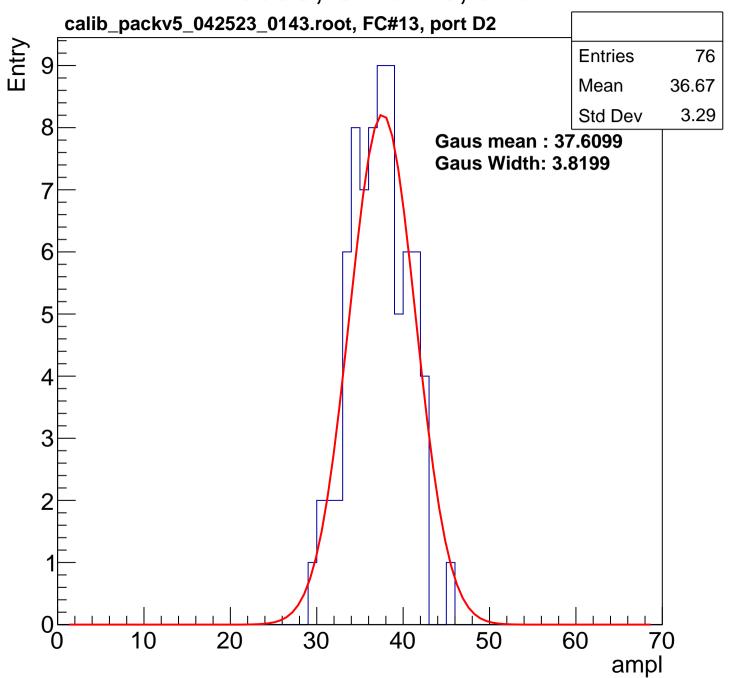


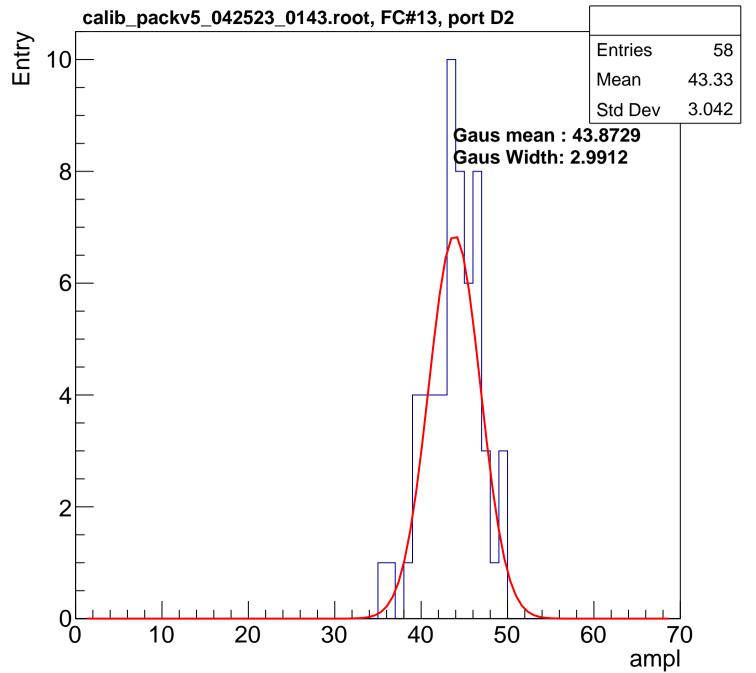


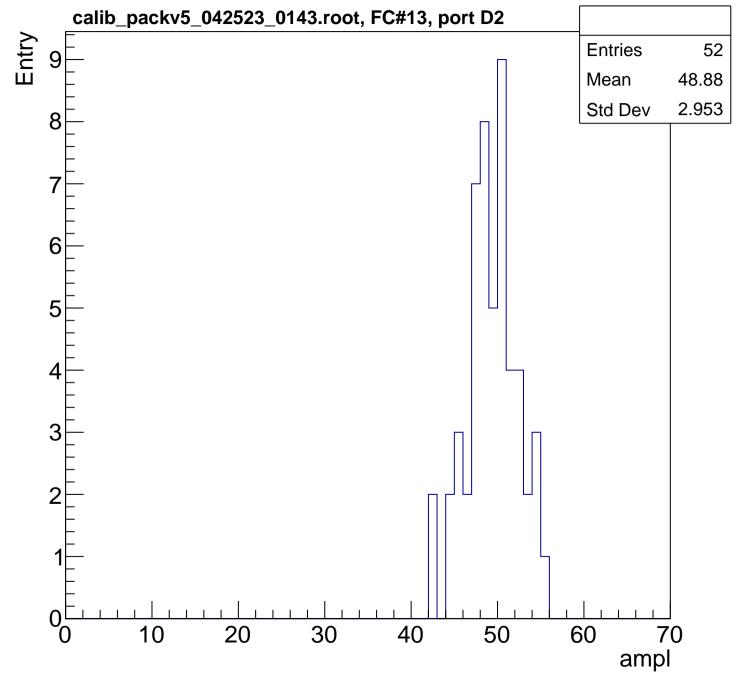


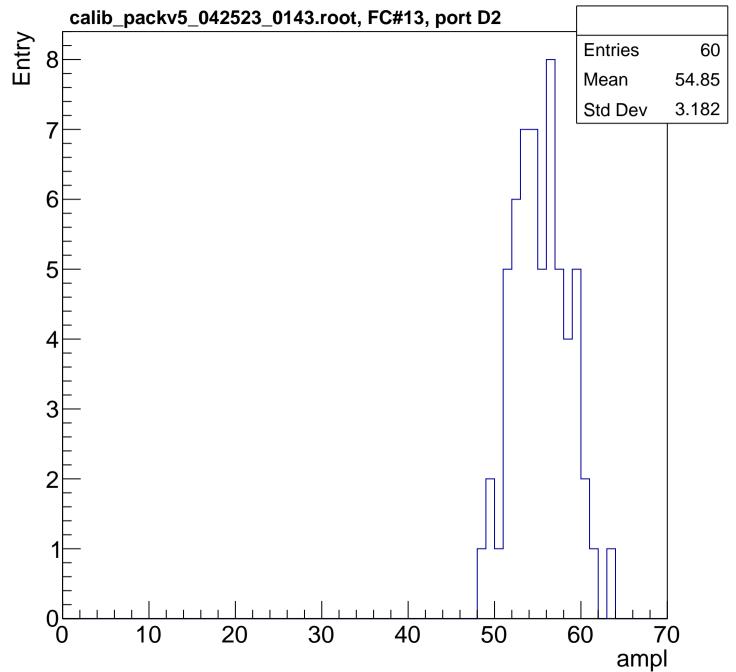


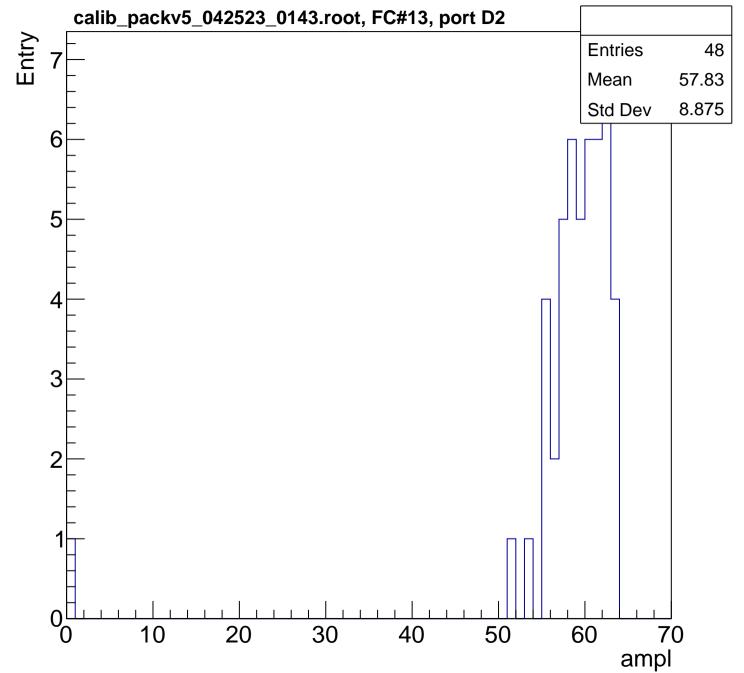


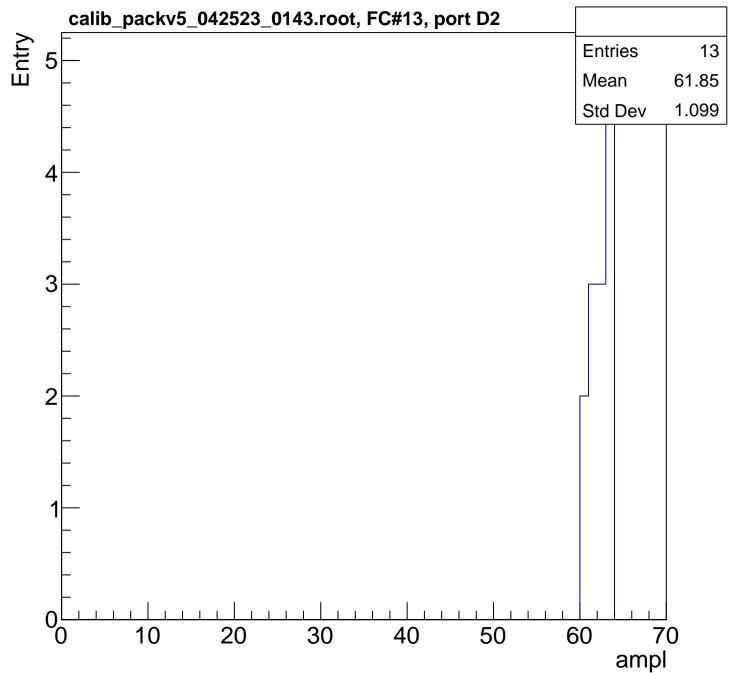


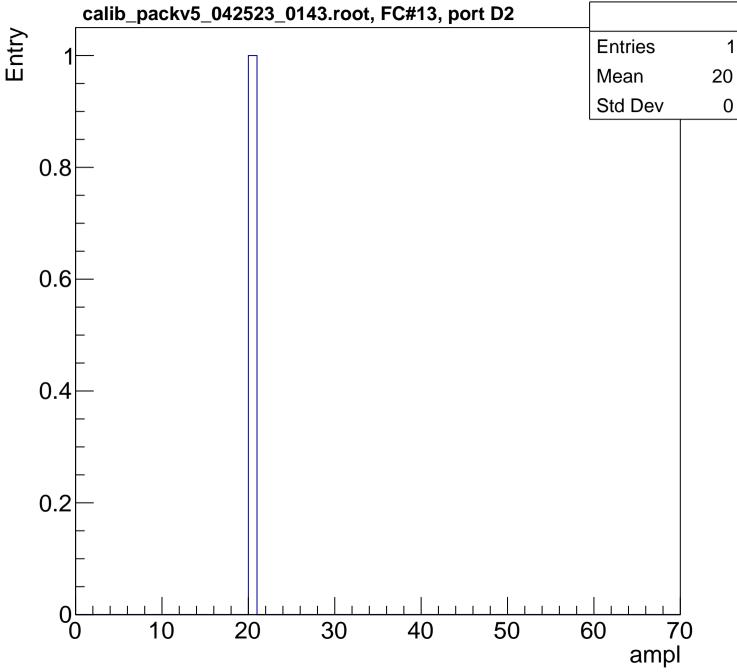


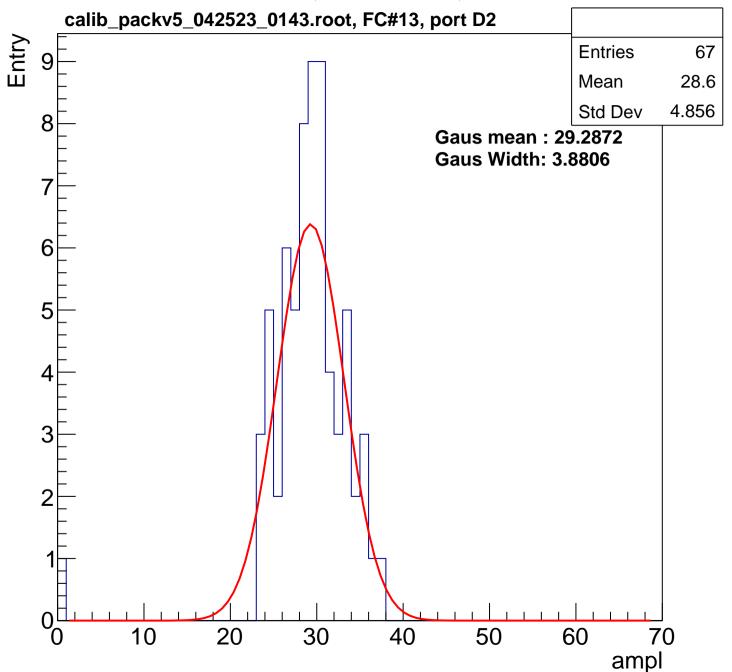


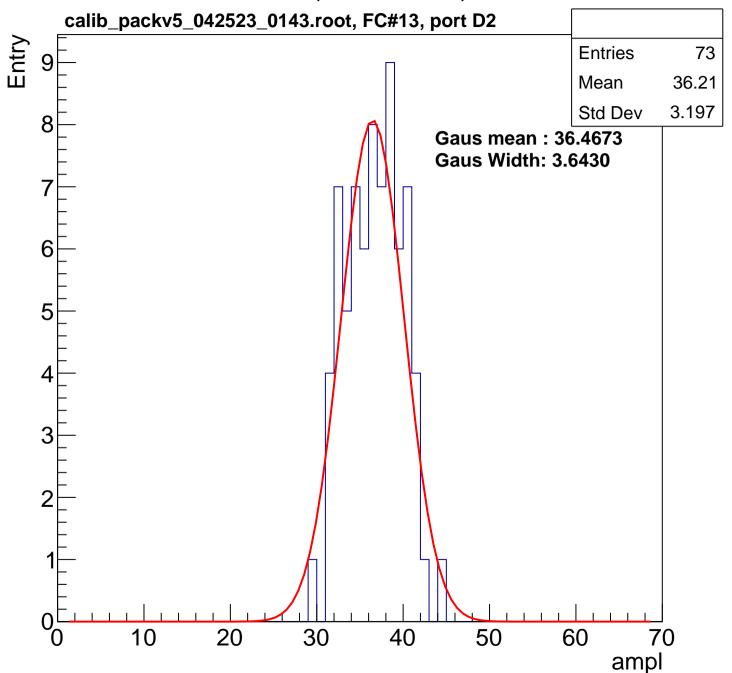


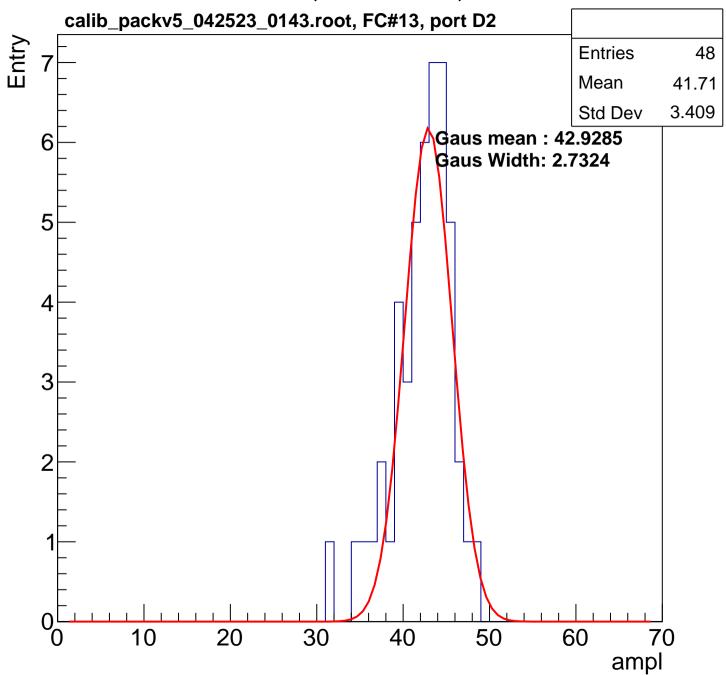


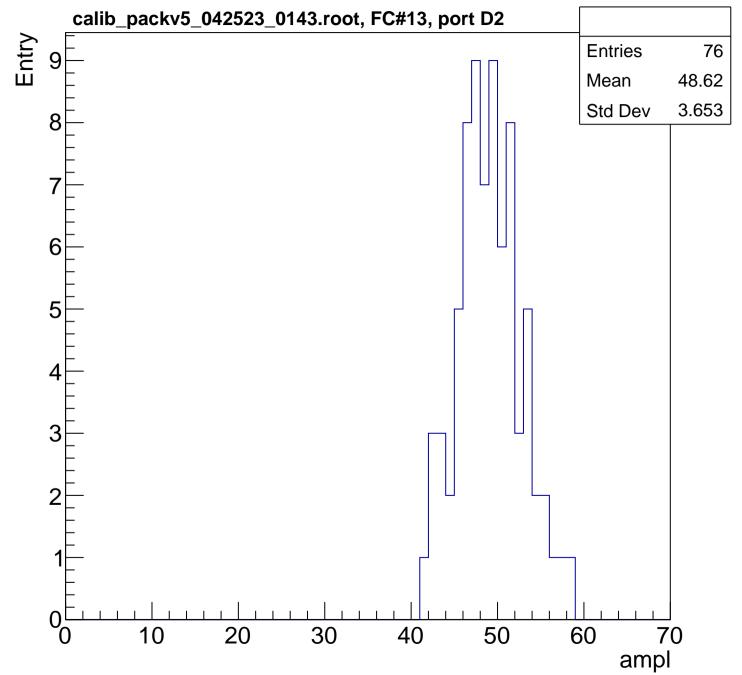


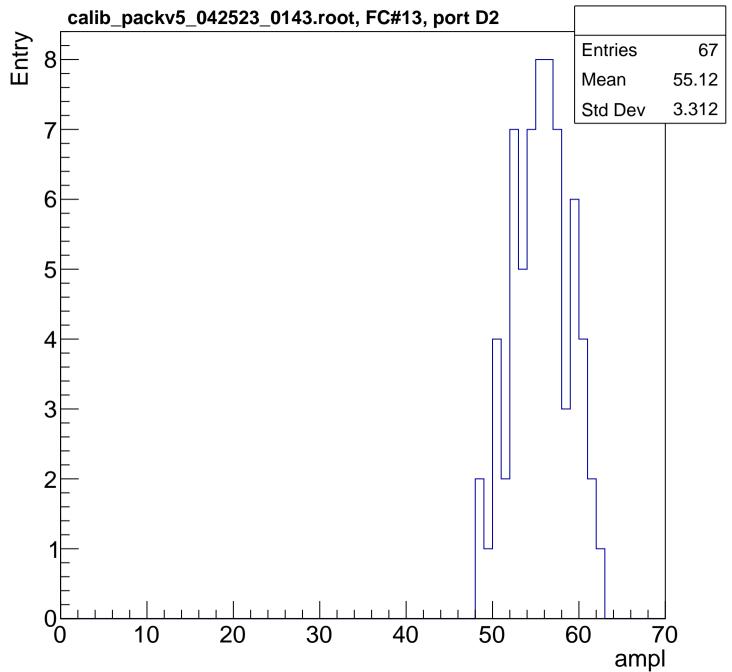


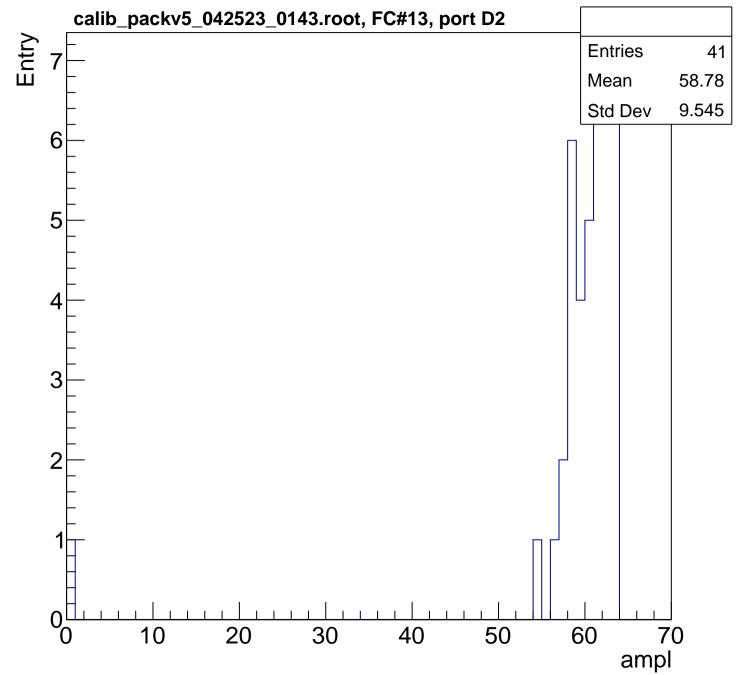


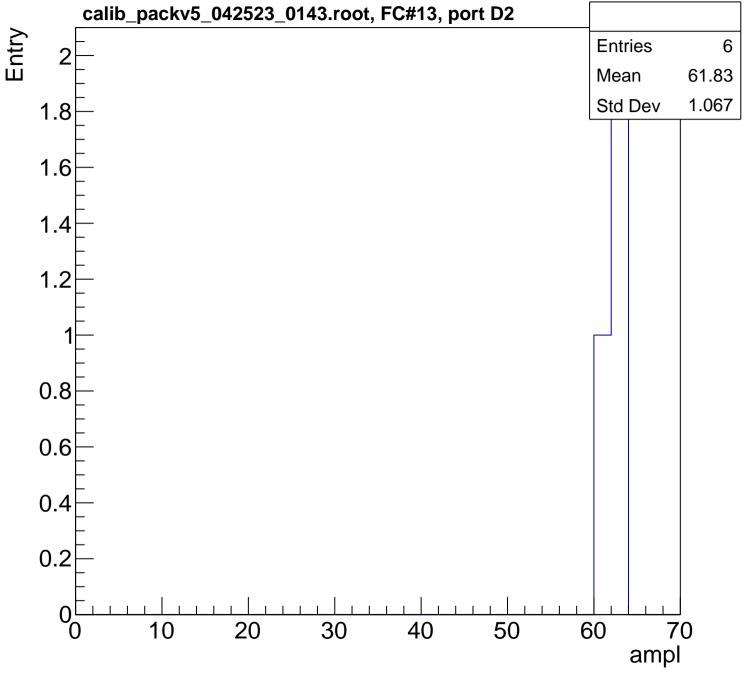


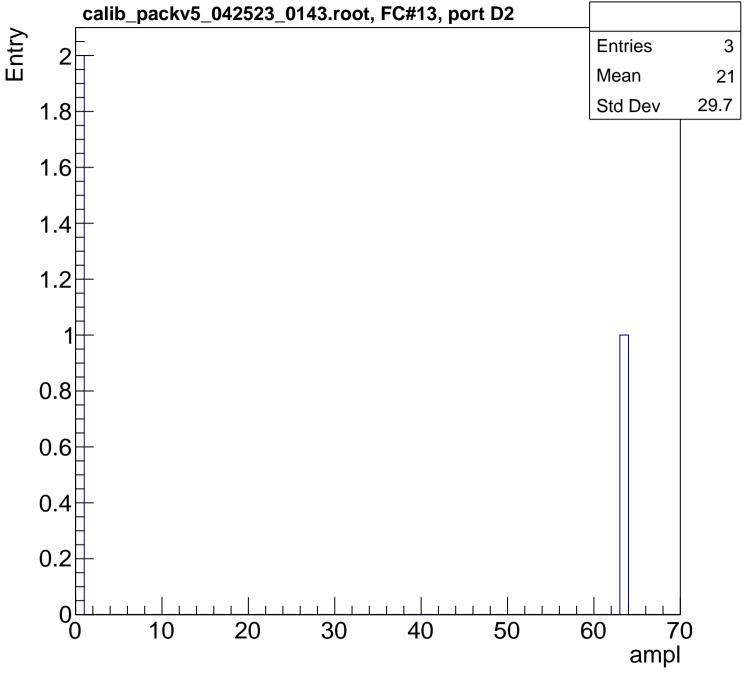


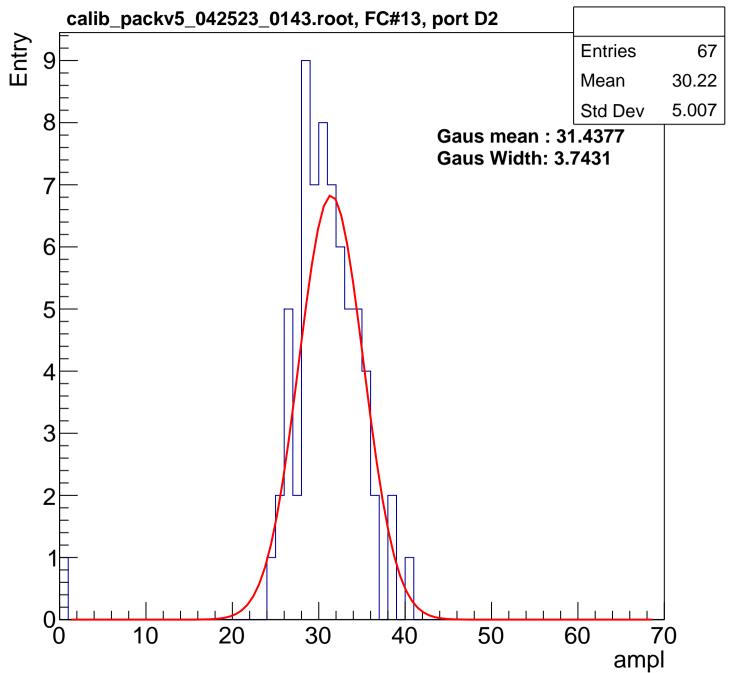


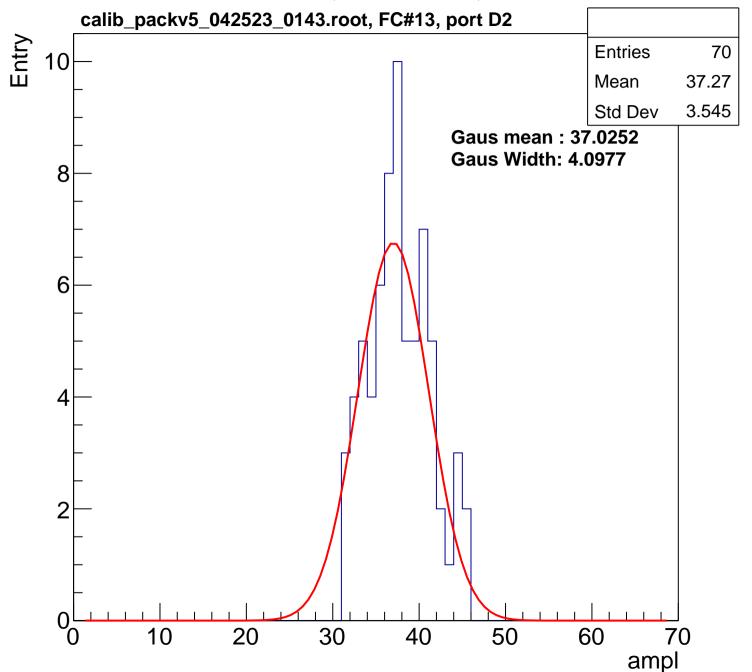


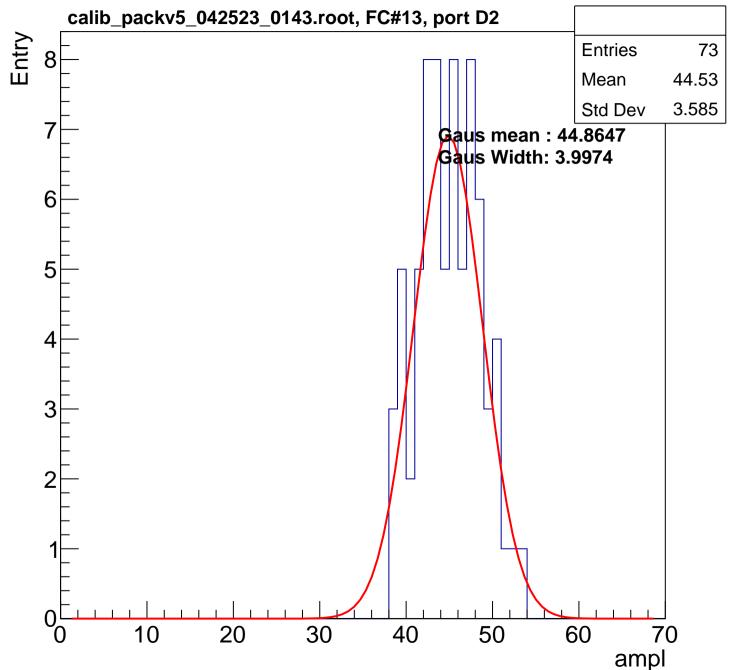


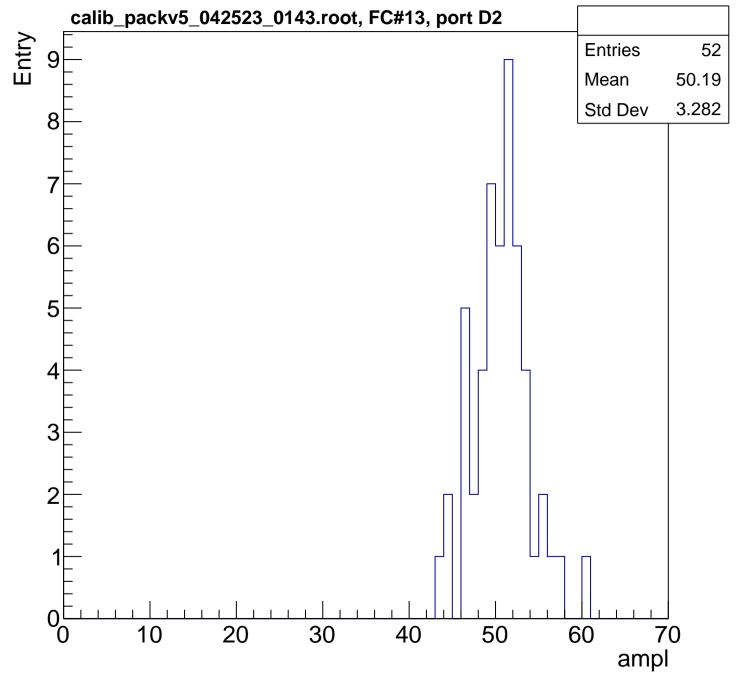


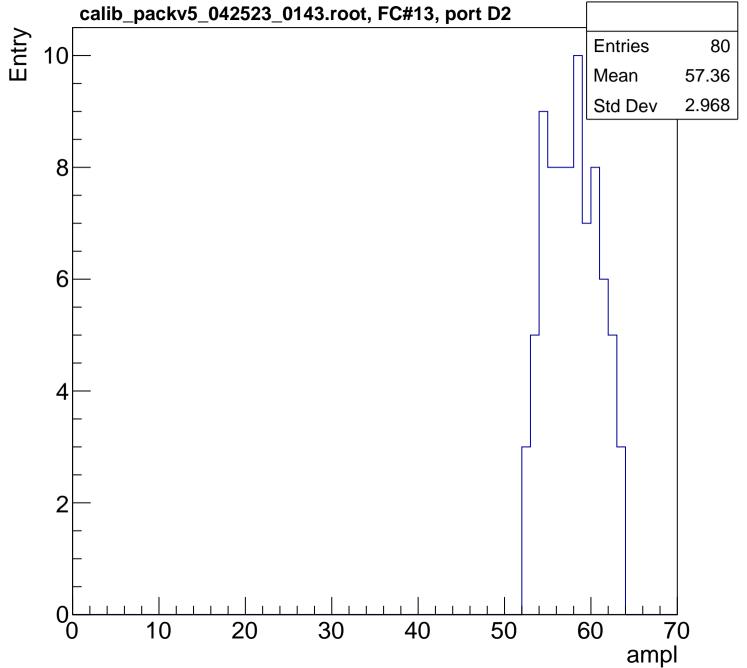


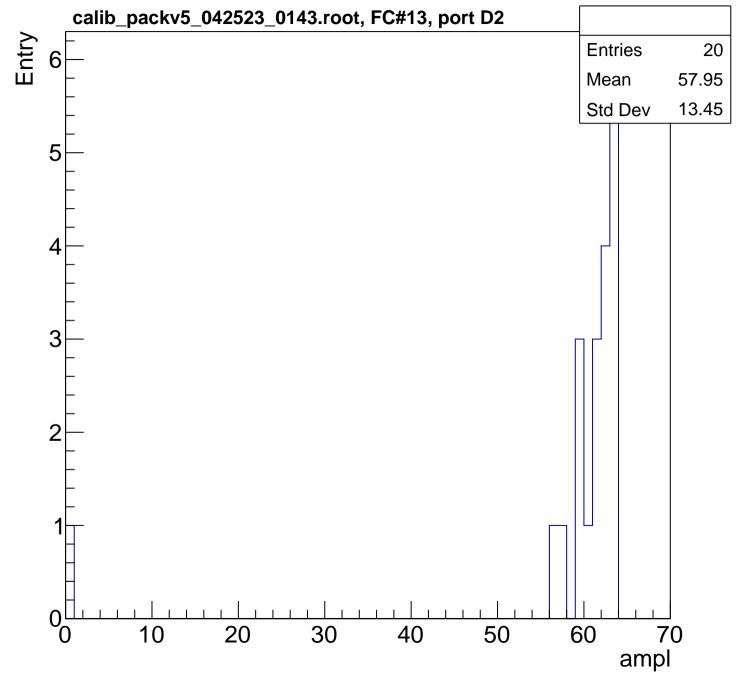


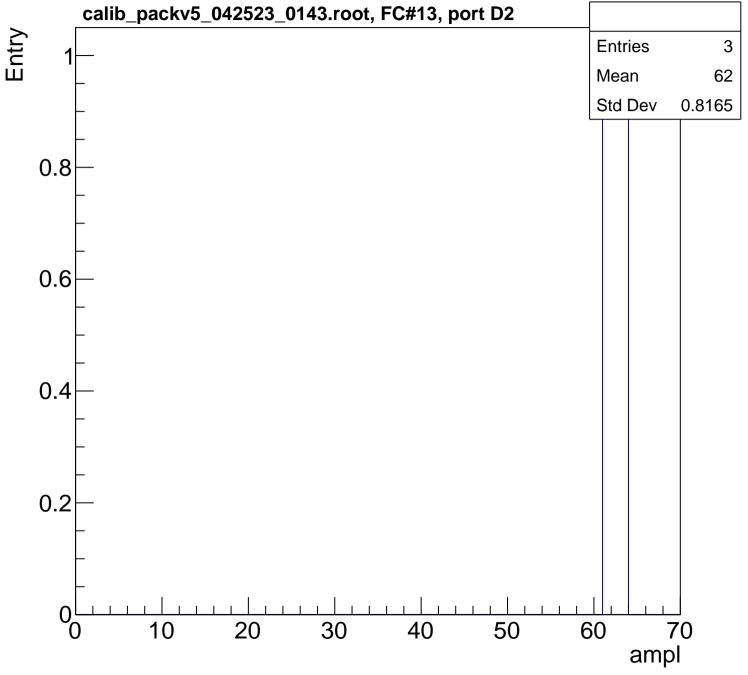


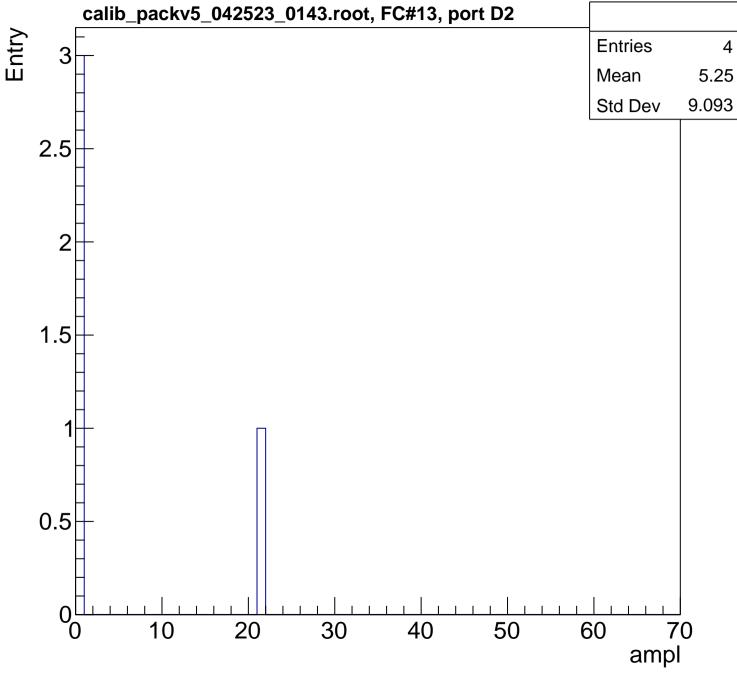


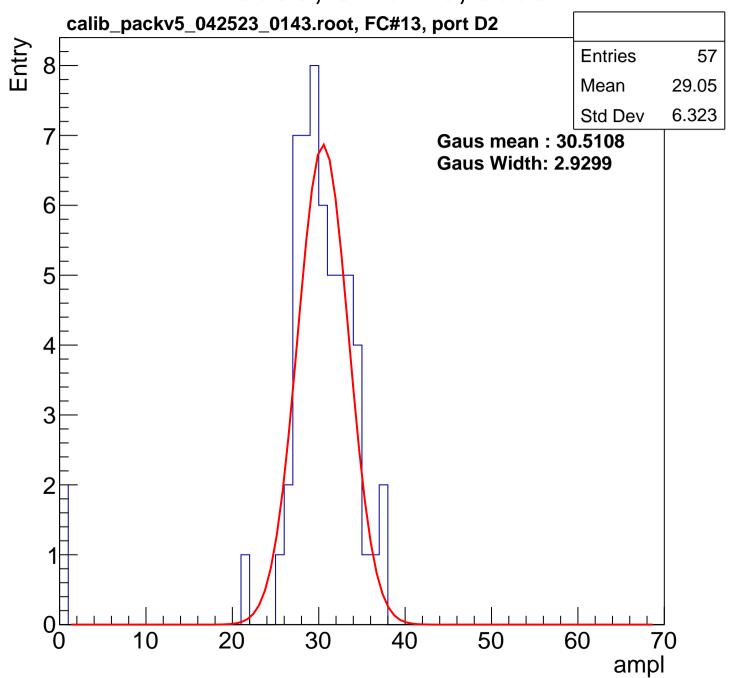


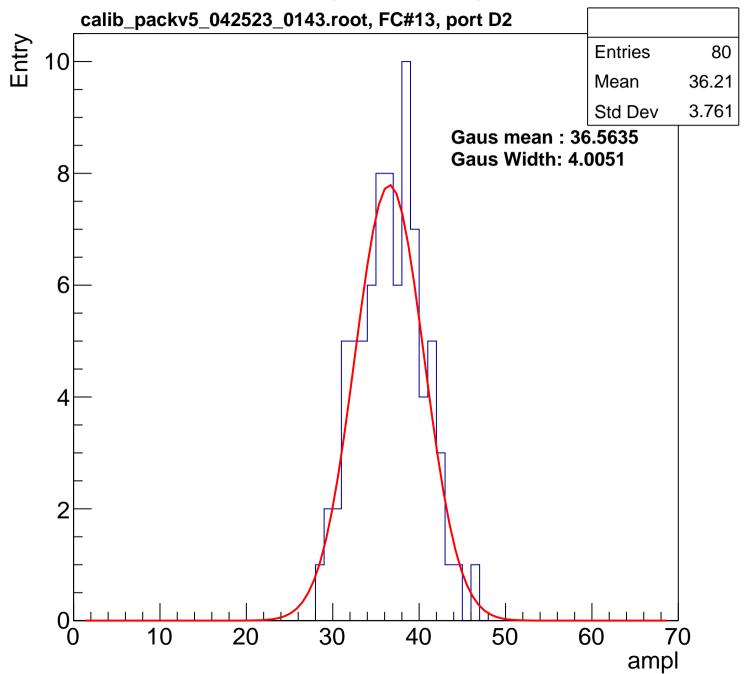


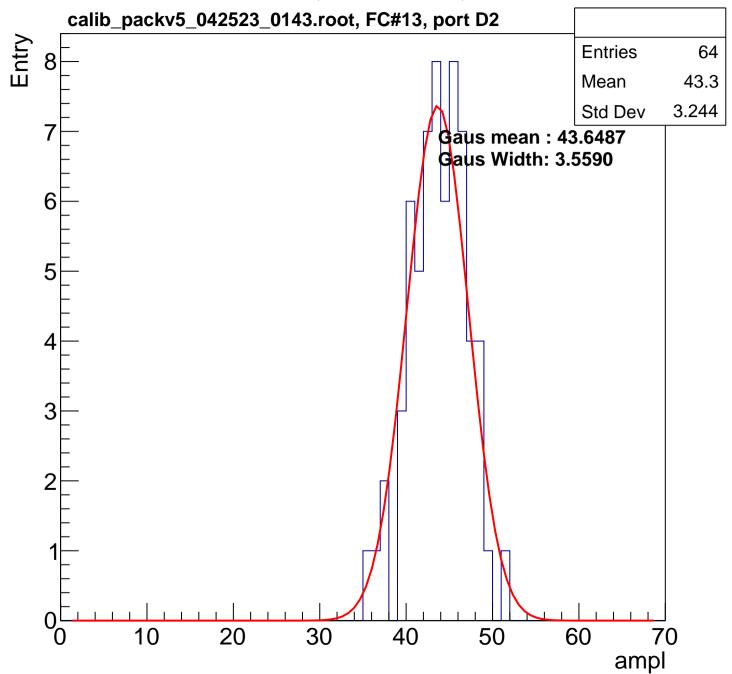


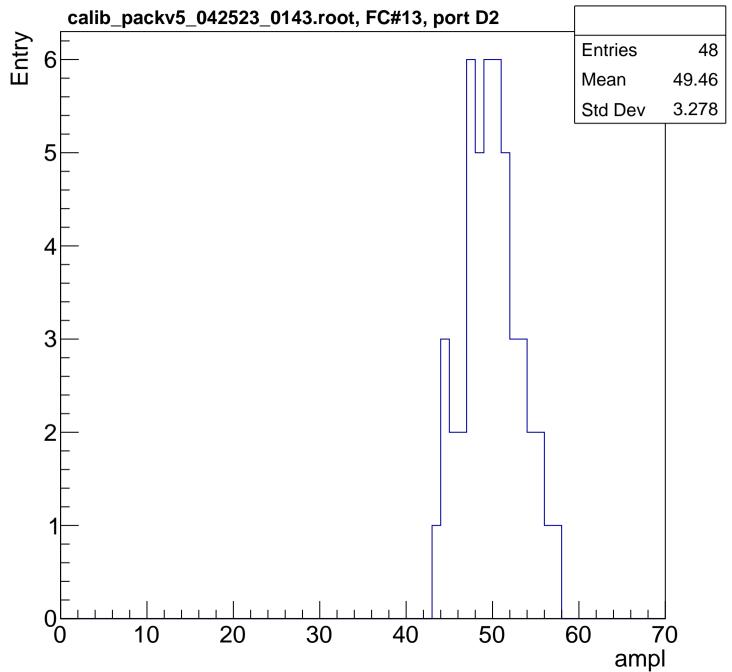


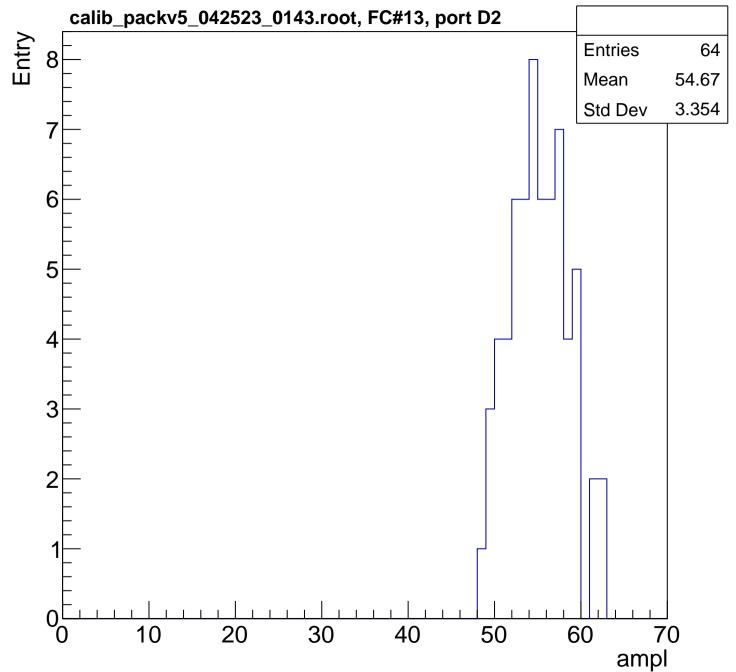


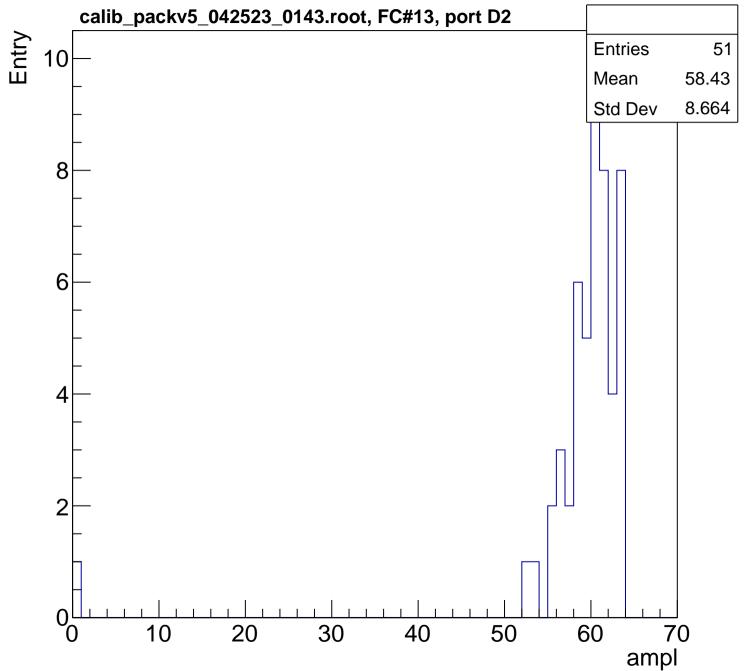


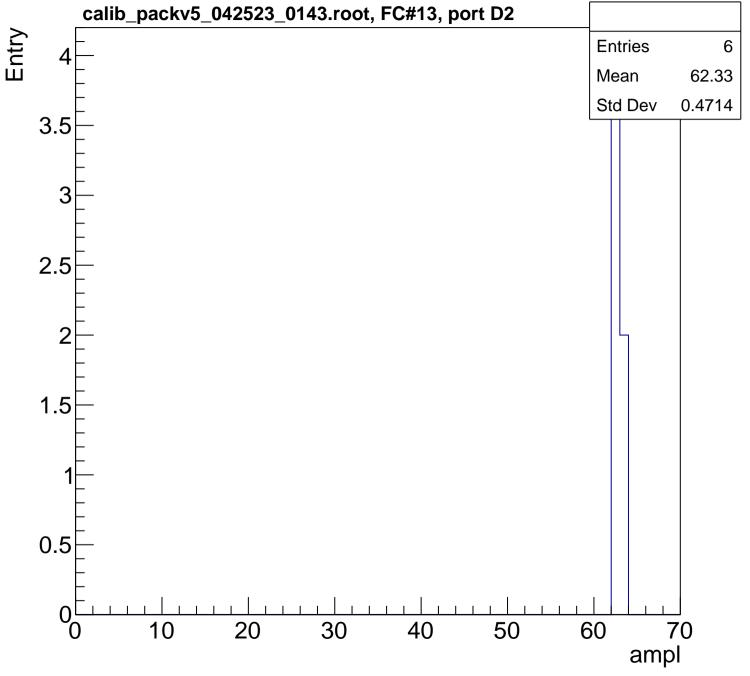


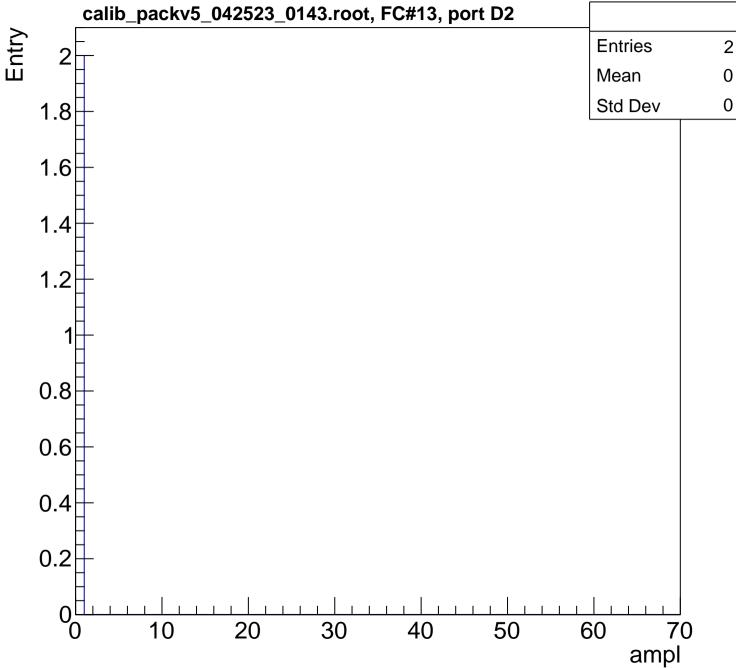


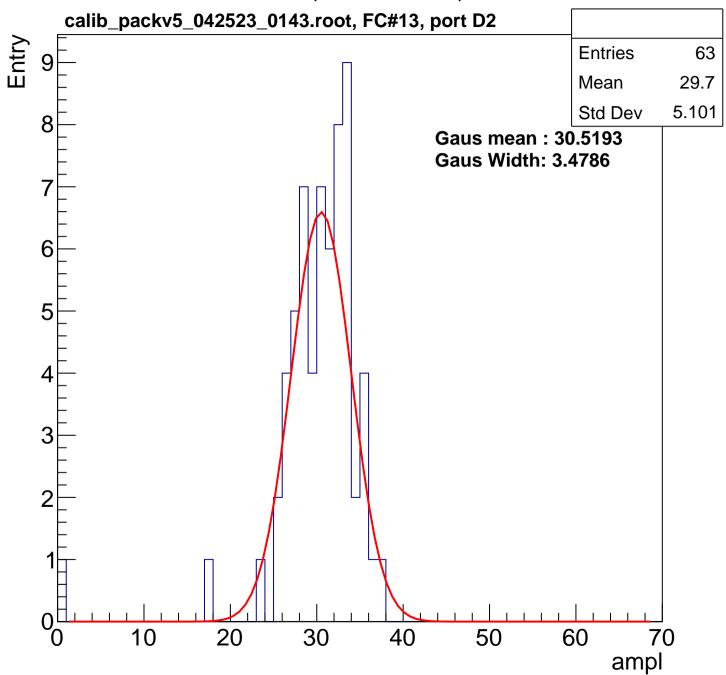


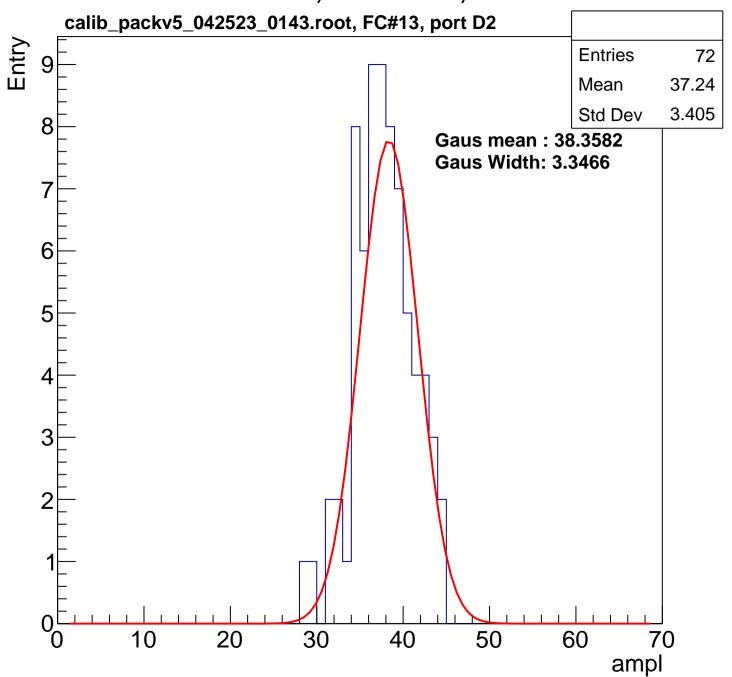


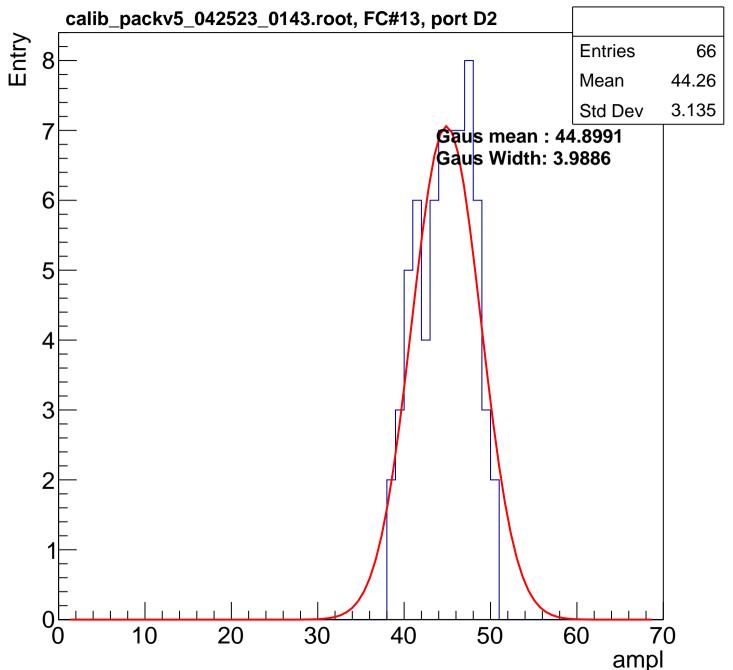


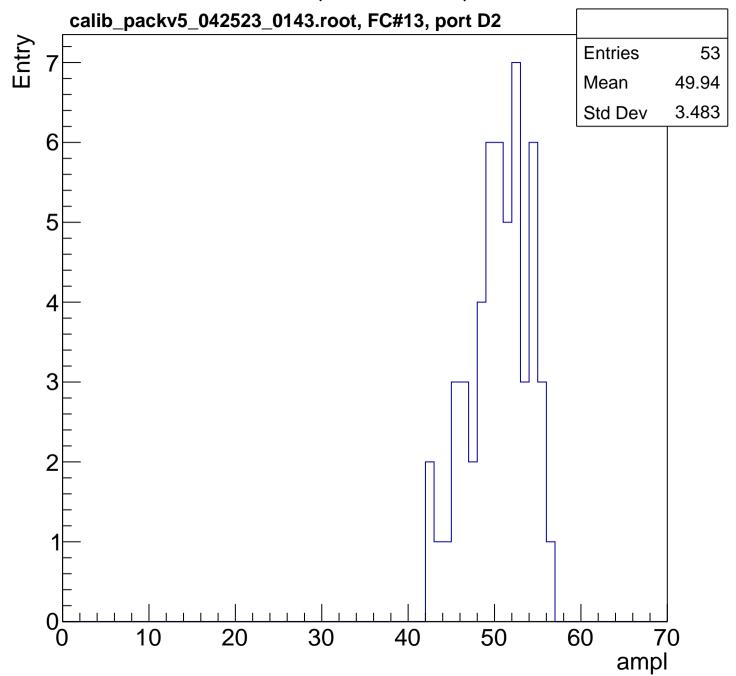


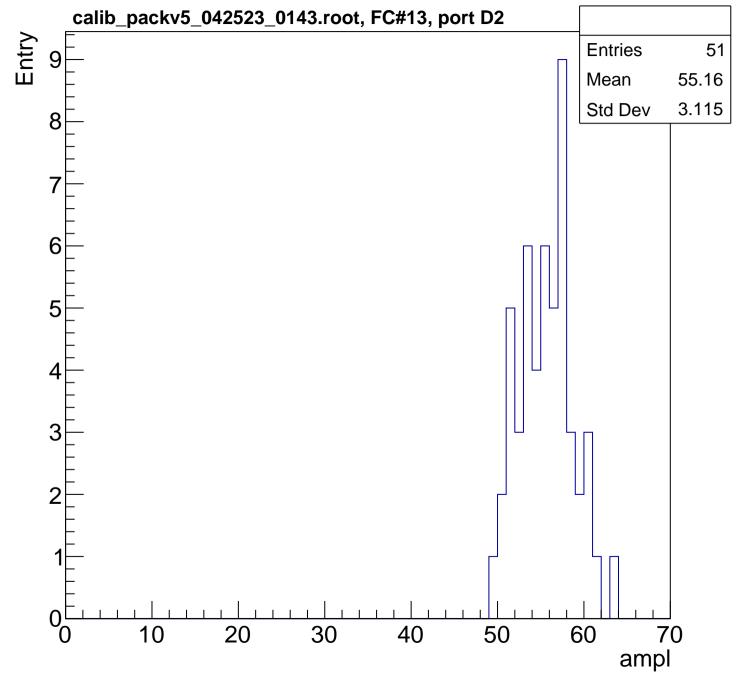


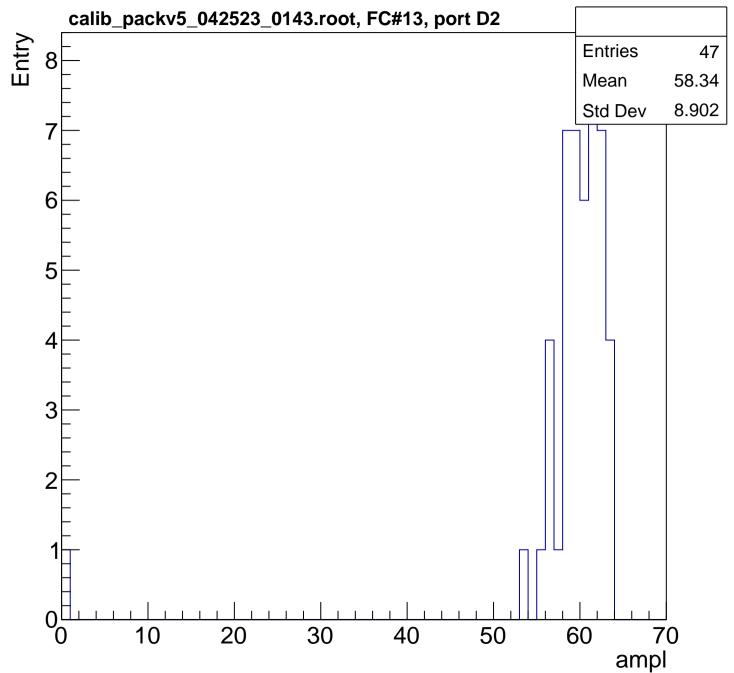


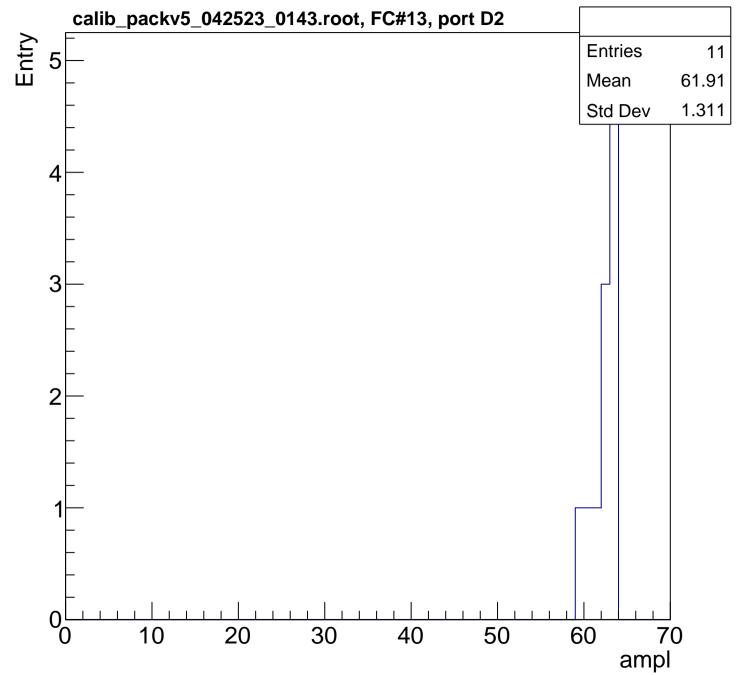




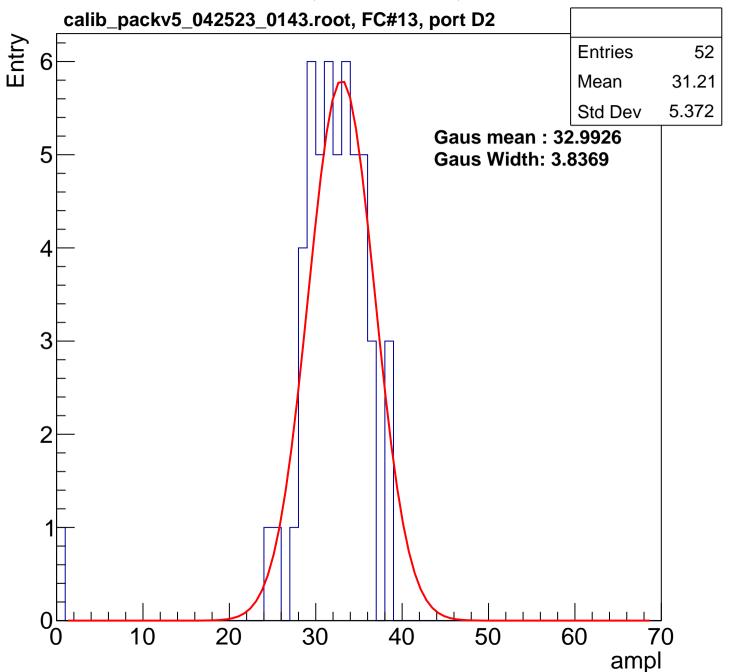


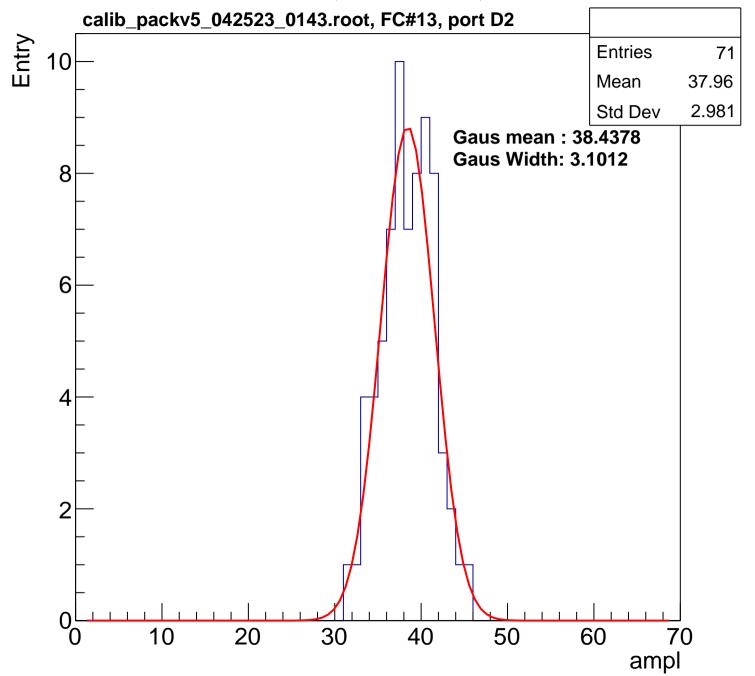


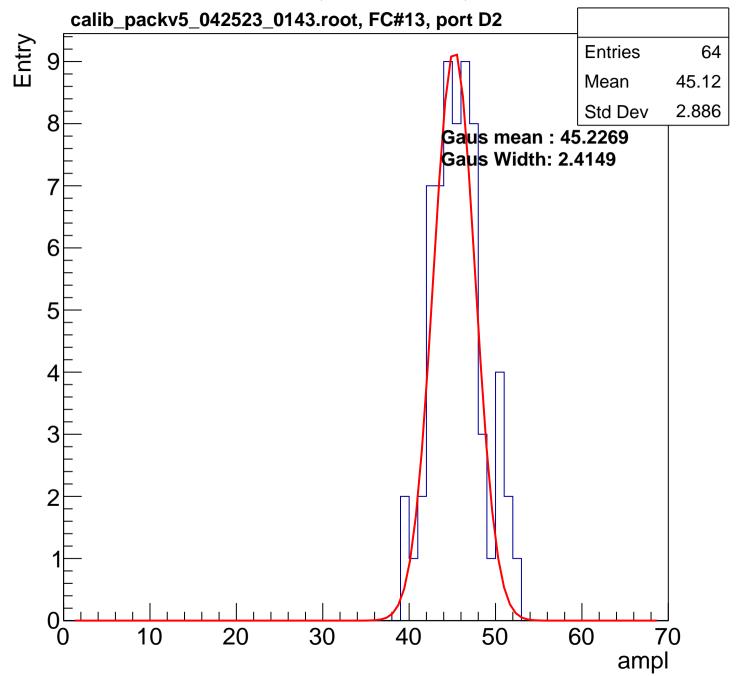


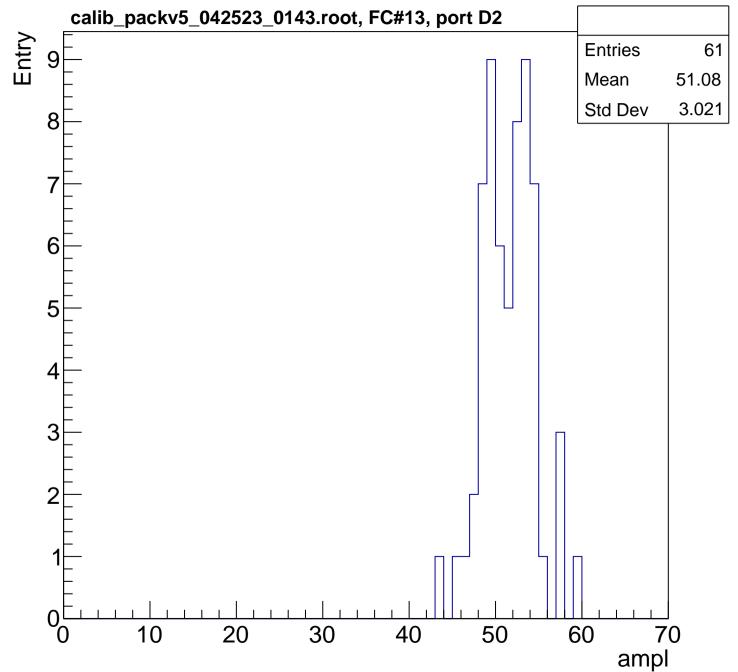


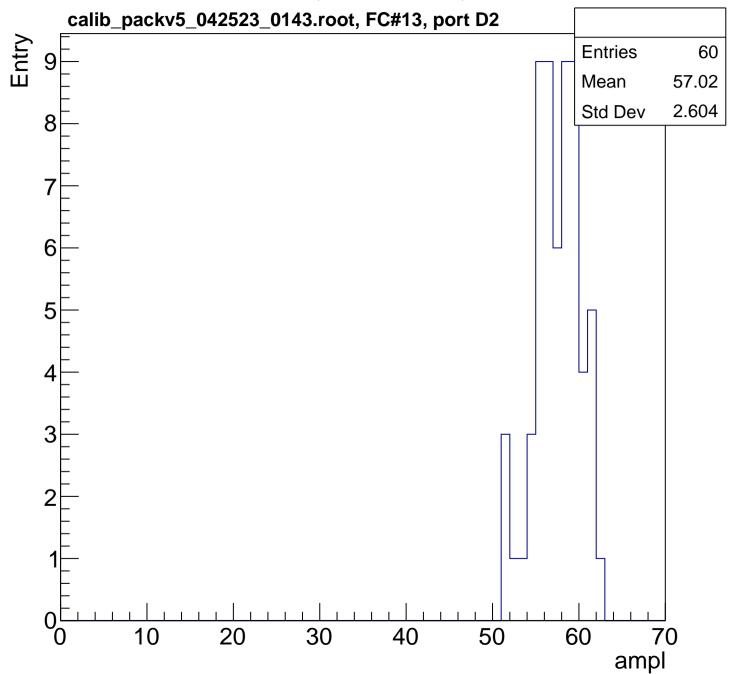
B1L003S, U4-ch14, adc7 calib_packv5_042523_0143.root, FC#13, port D2 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

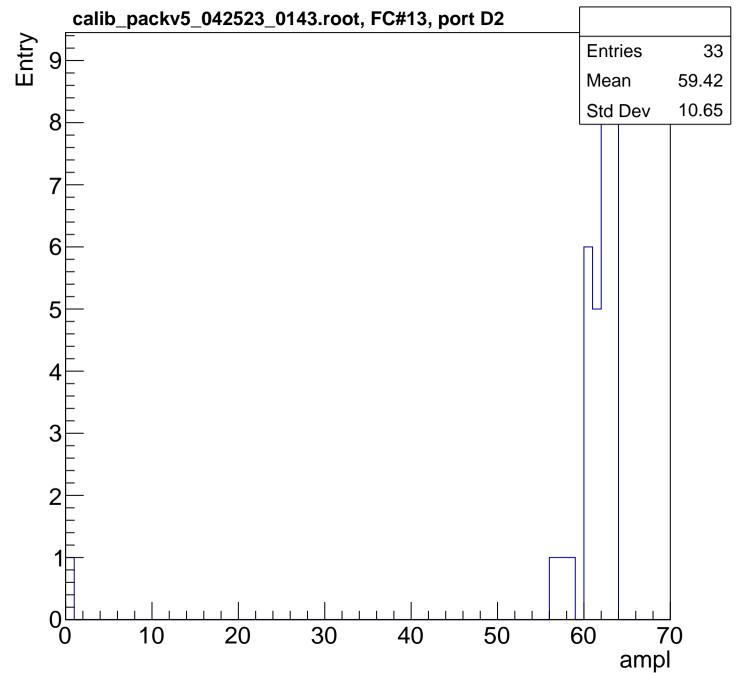


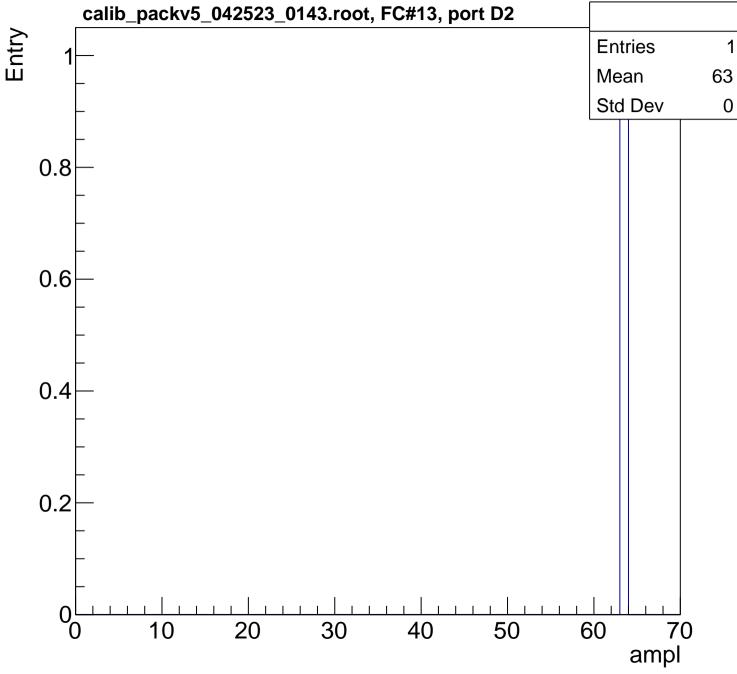


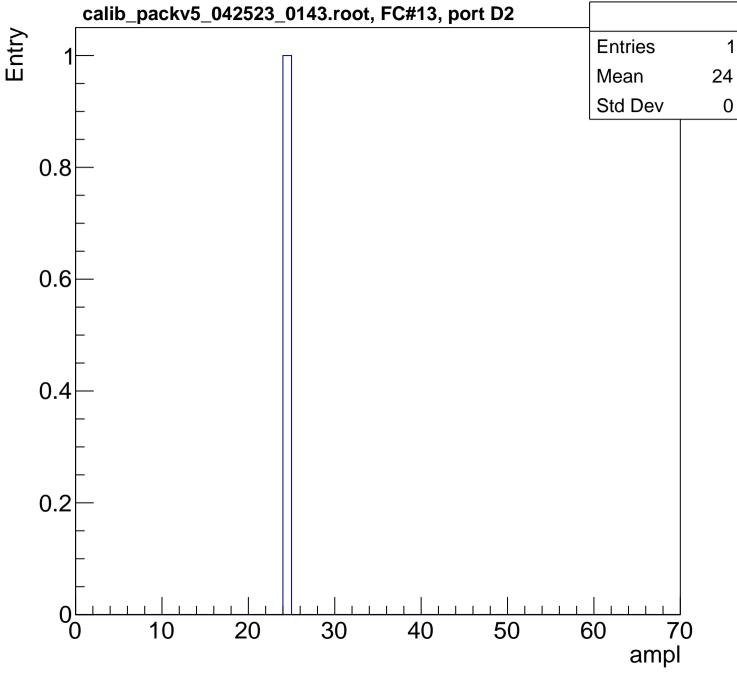


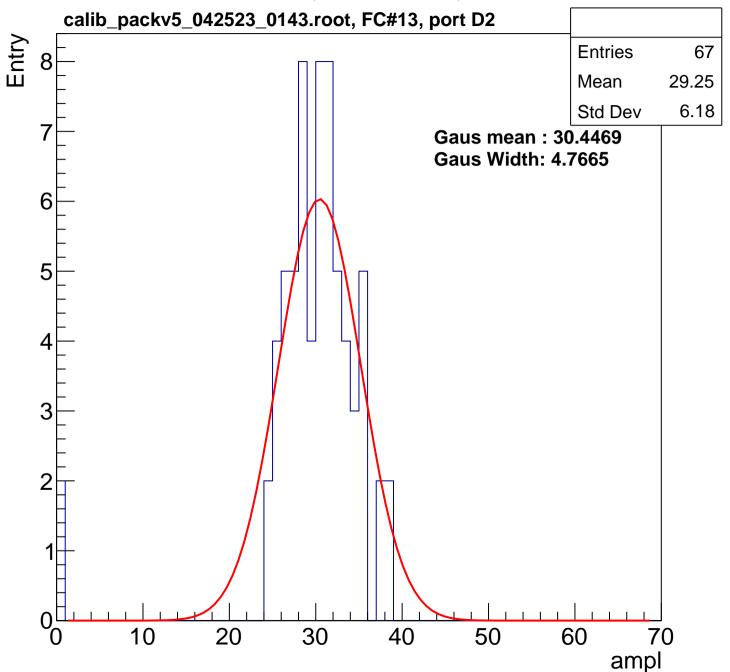


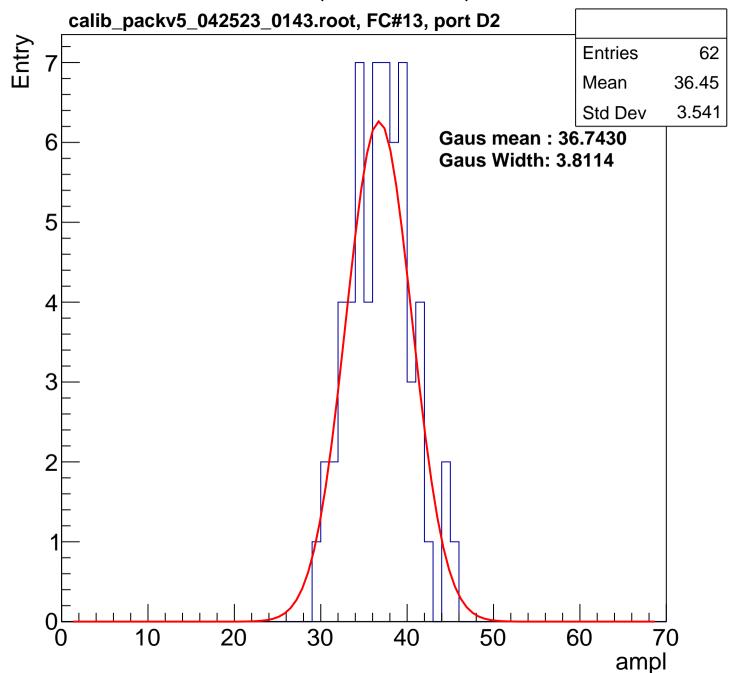


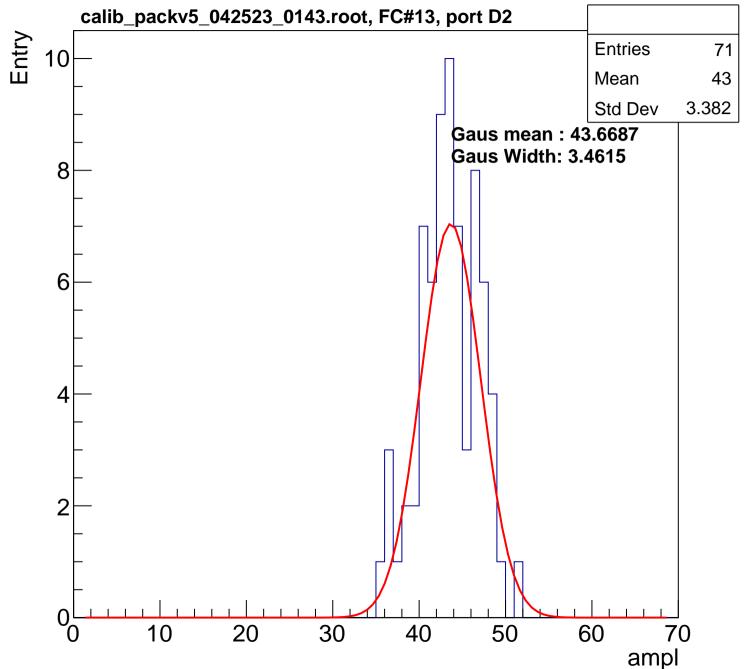


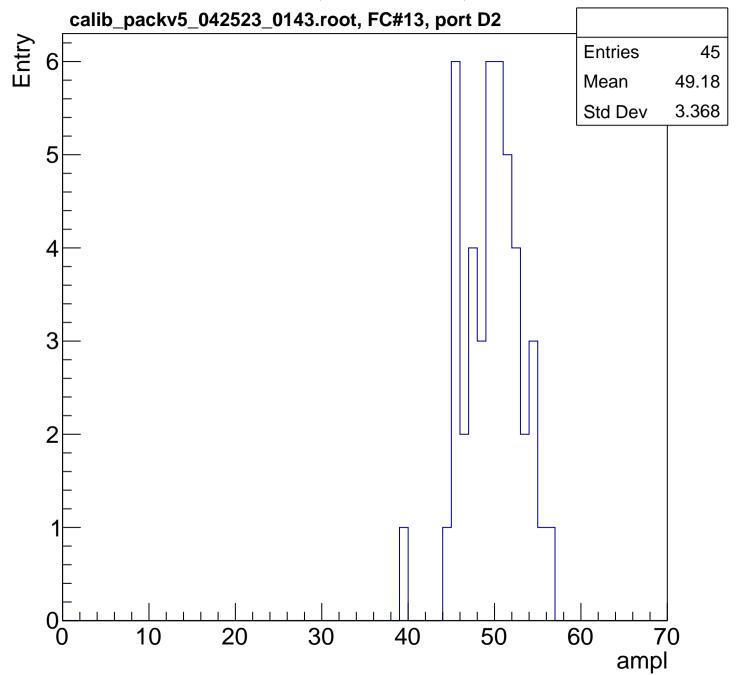


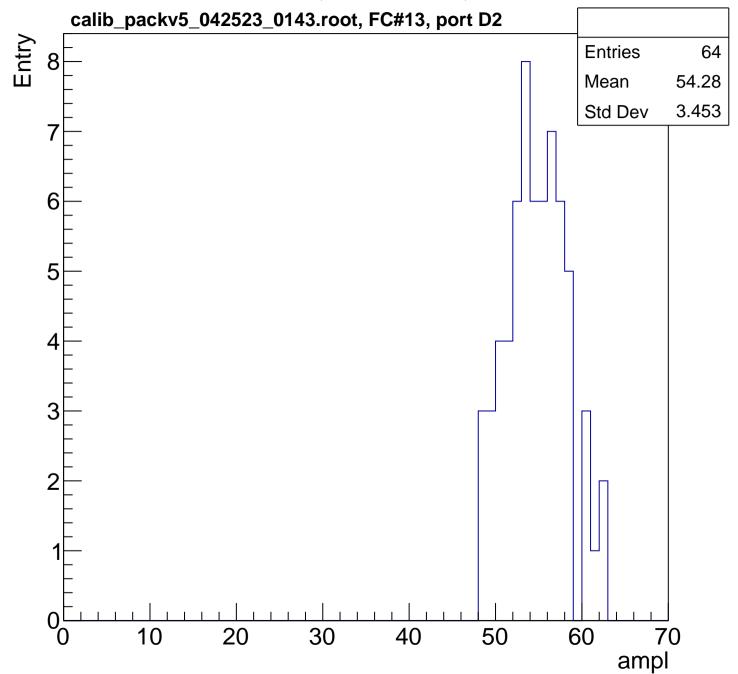


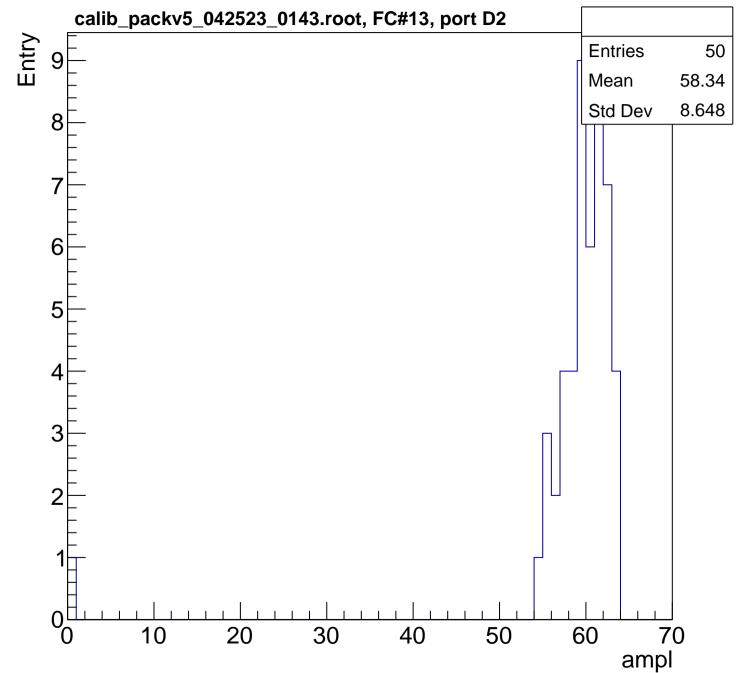


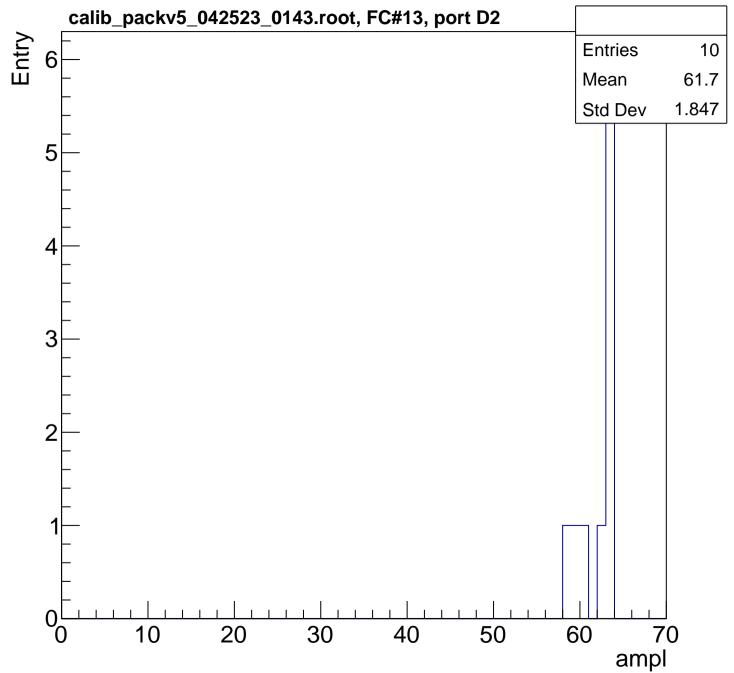




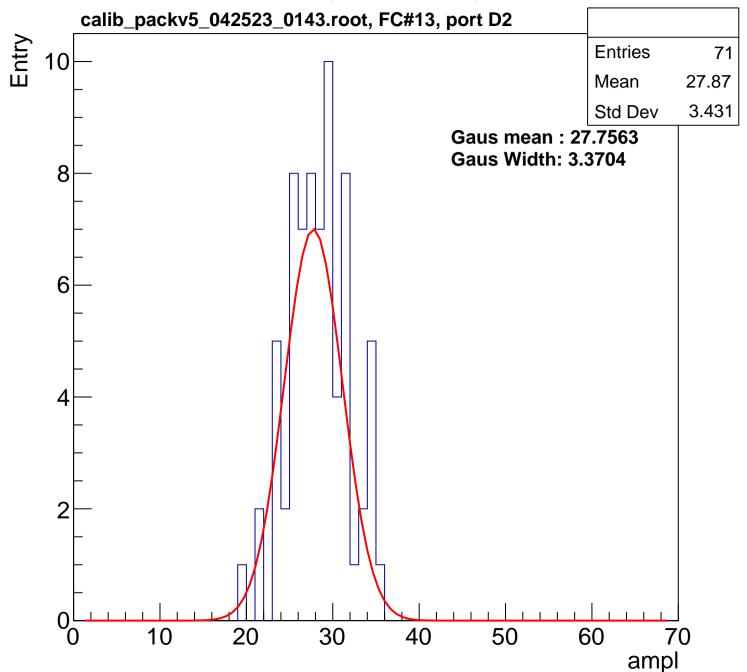


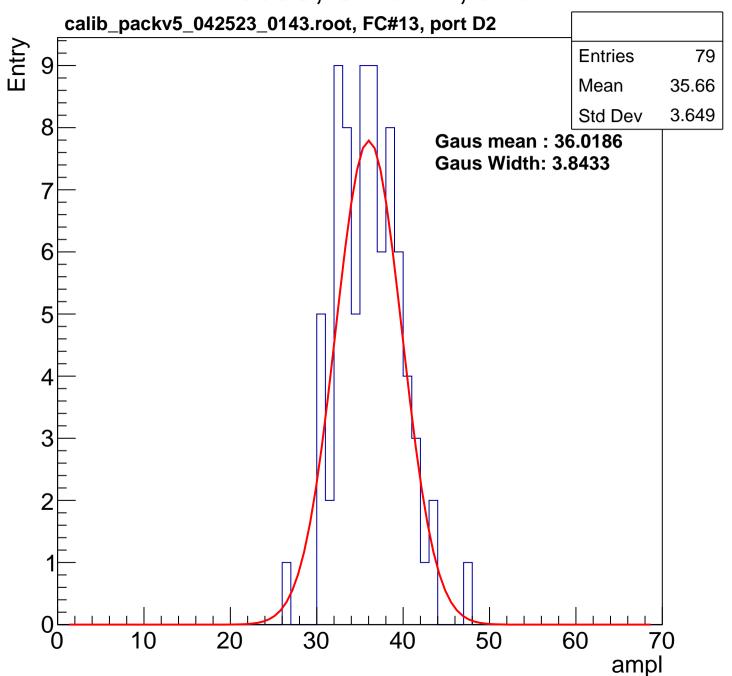


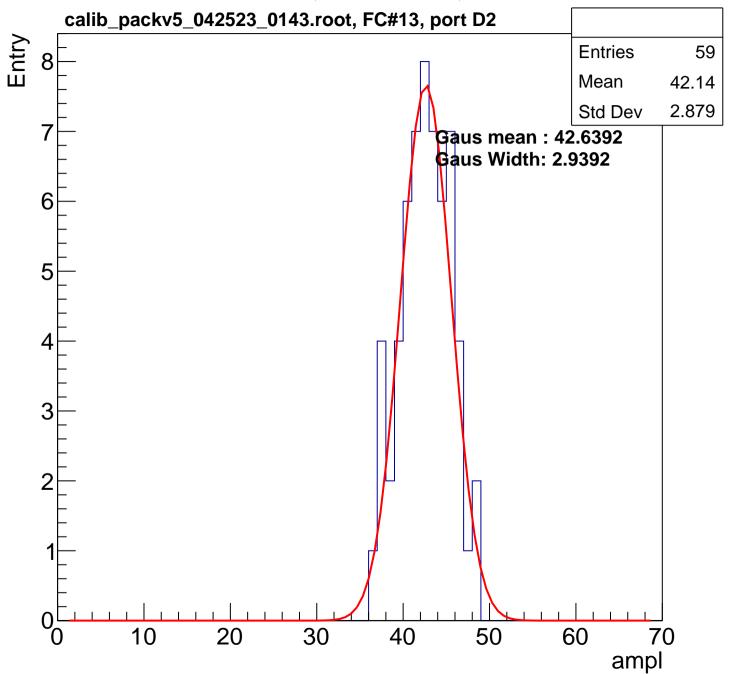


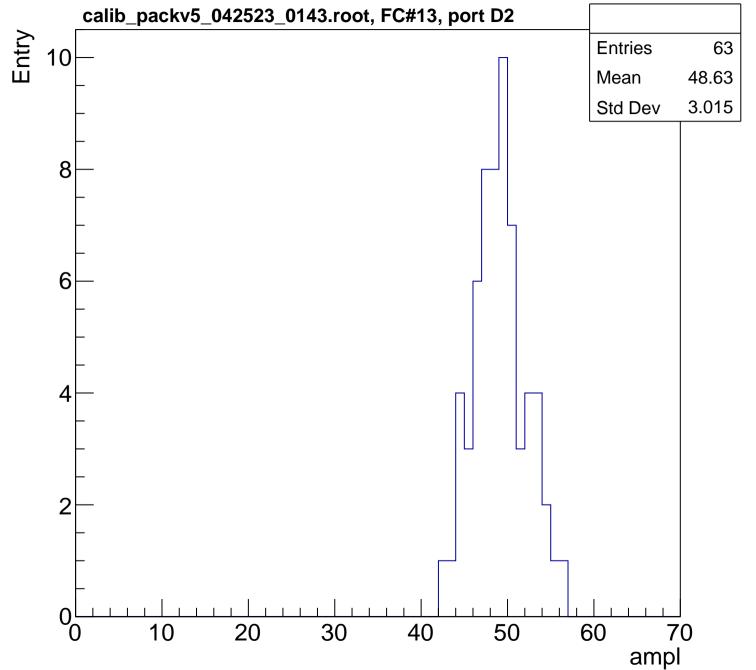


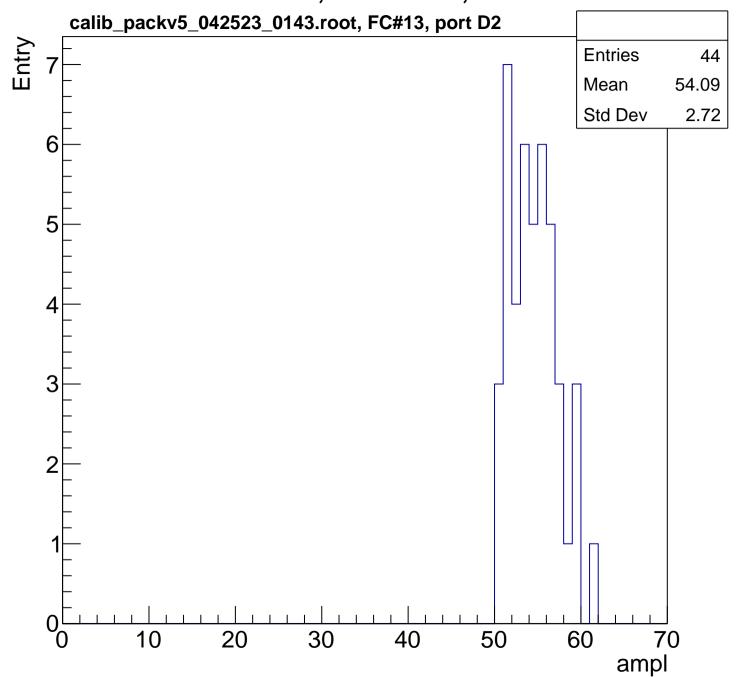
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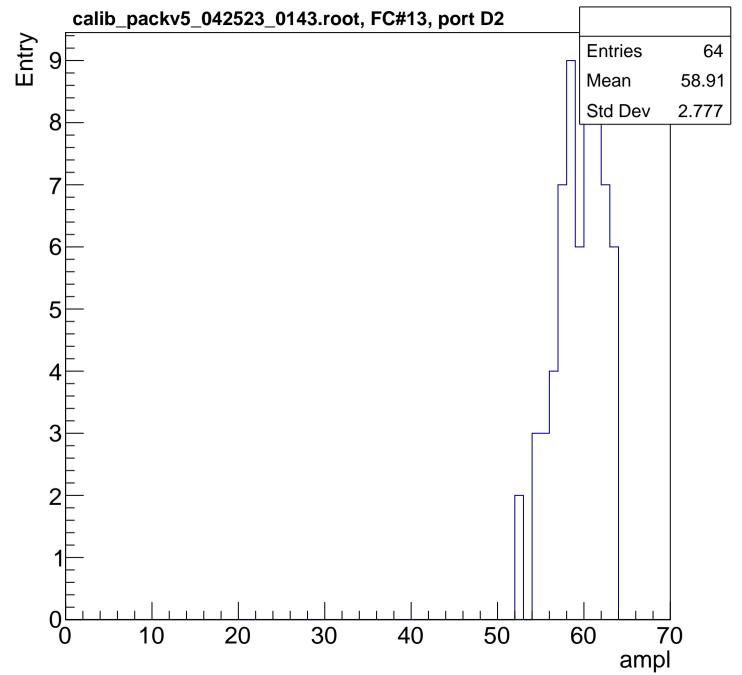


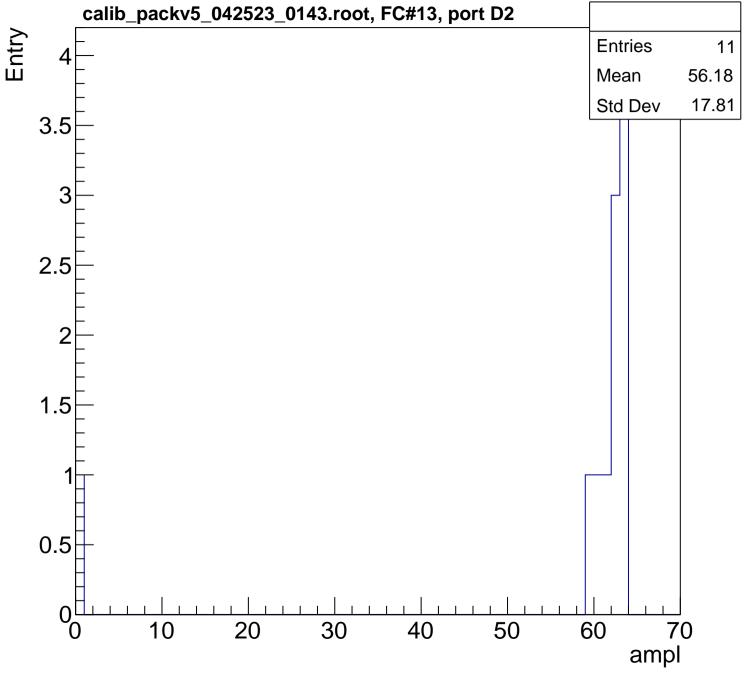




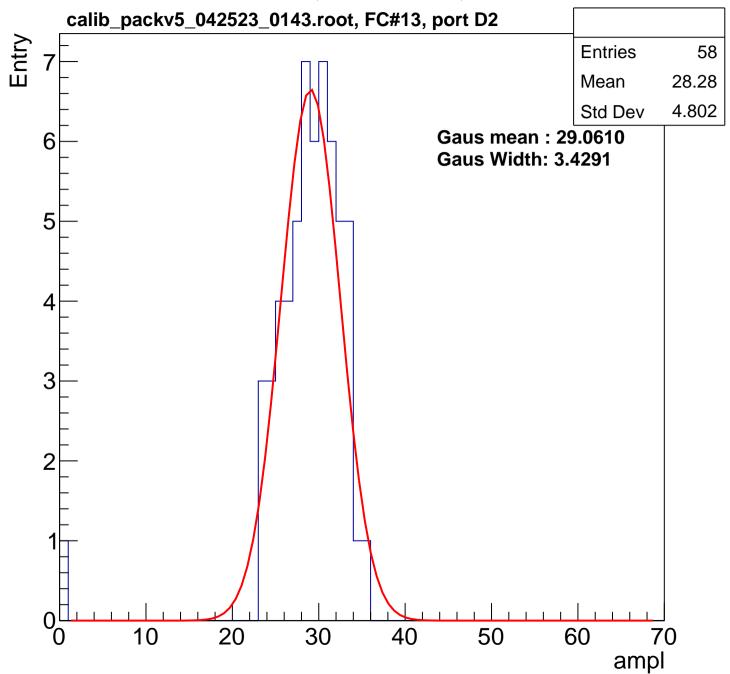


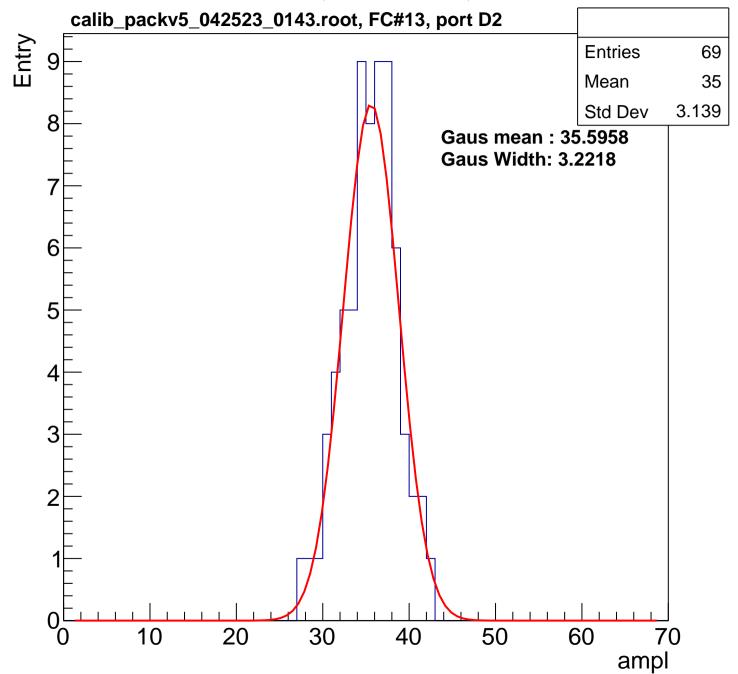


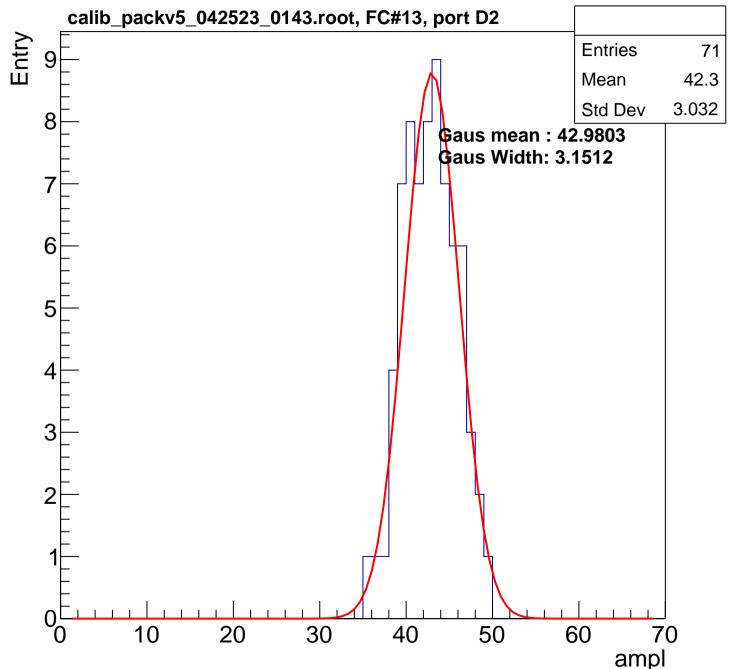


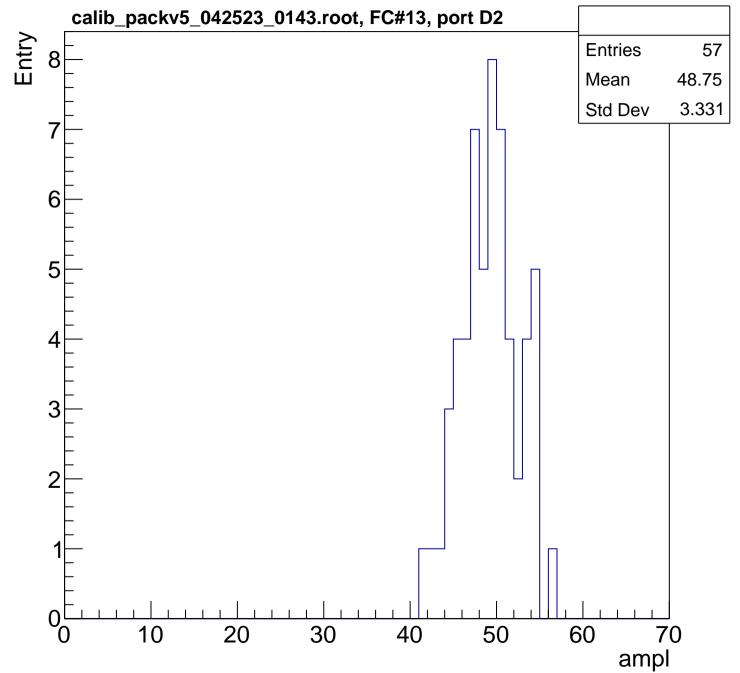


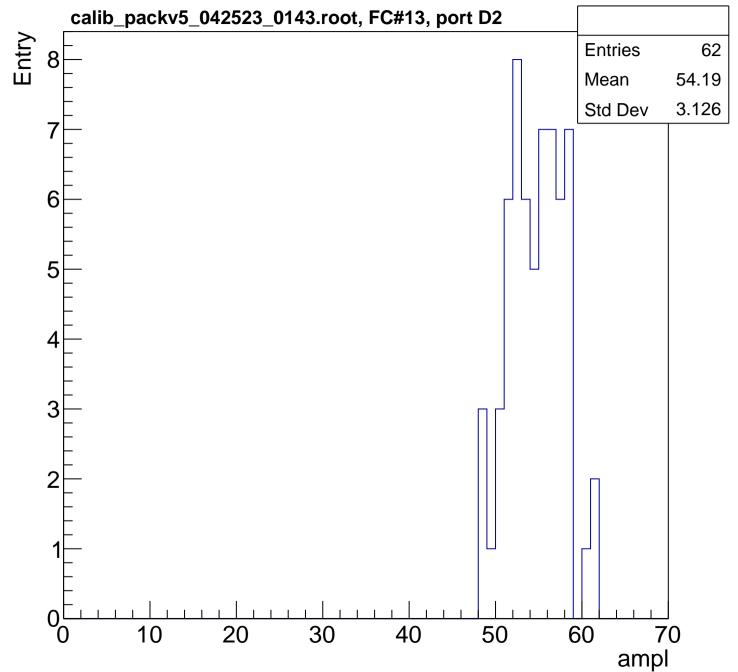


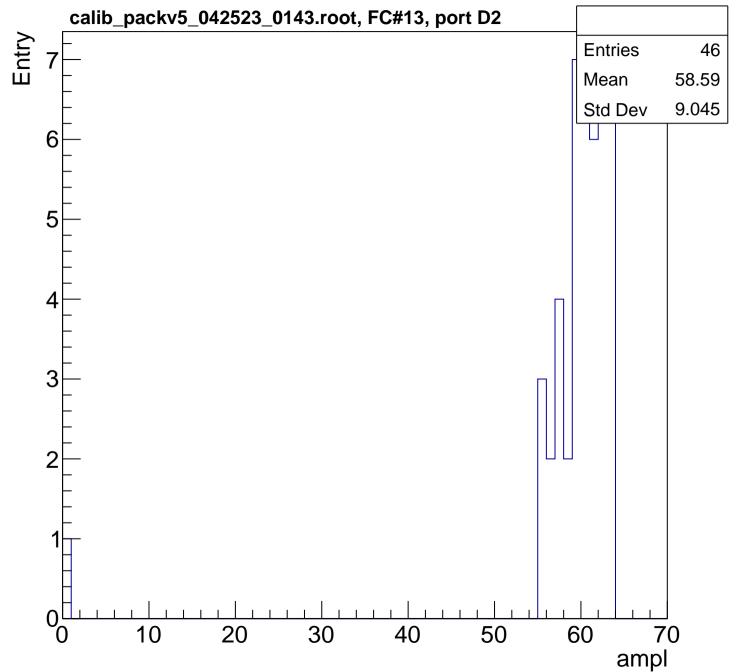


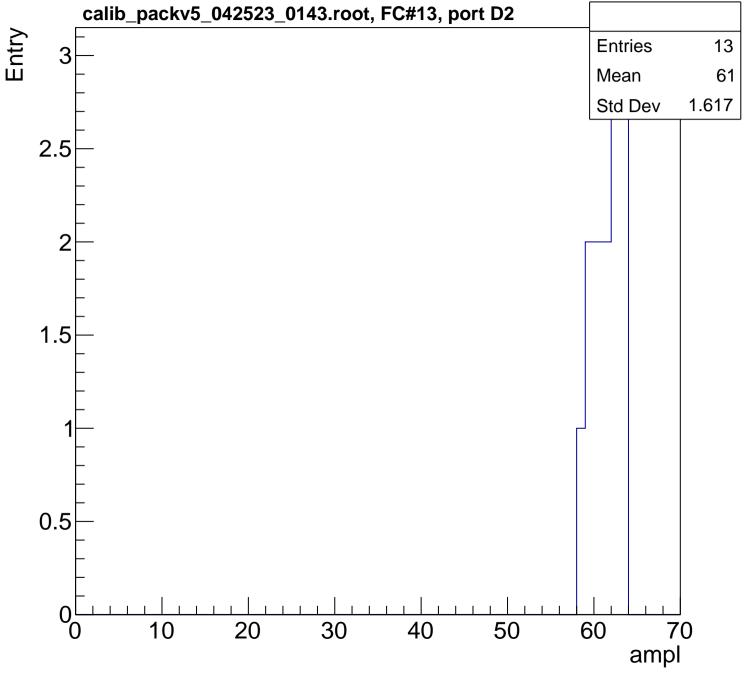


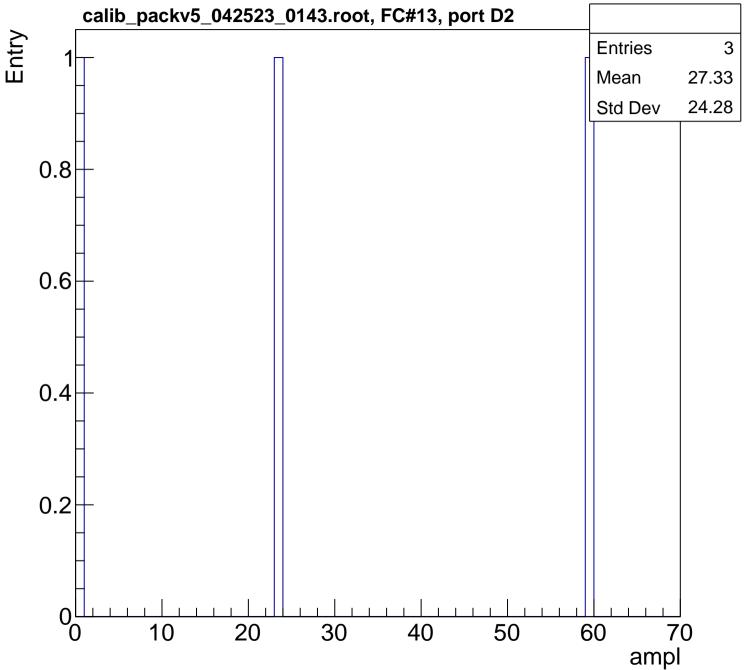


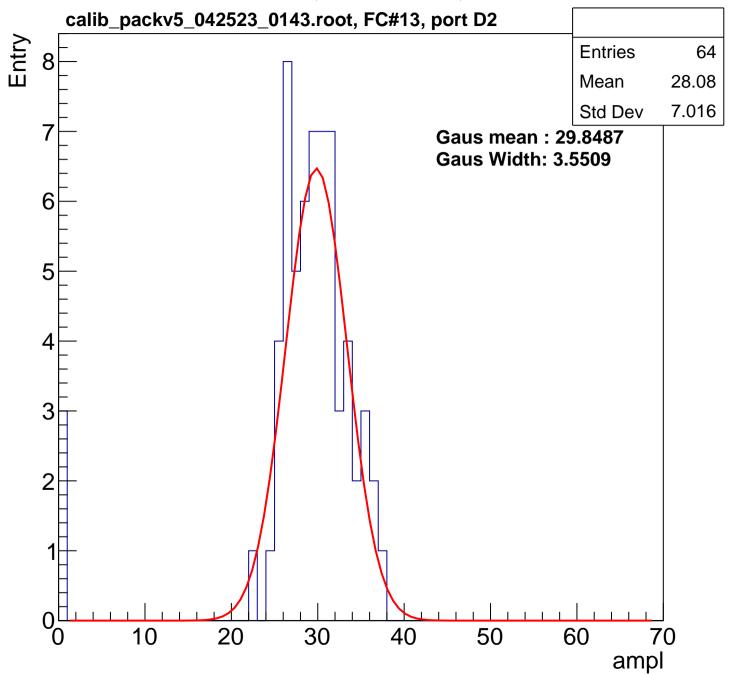


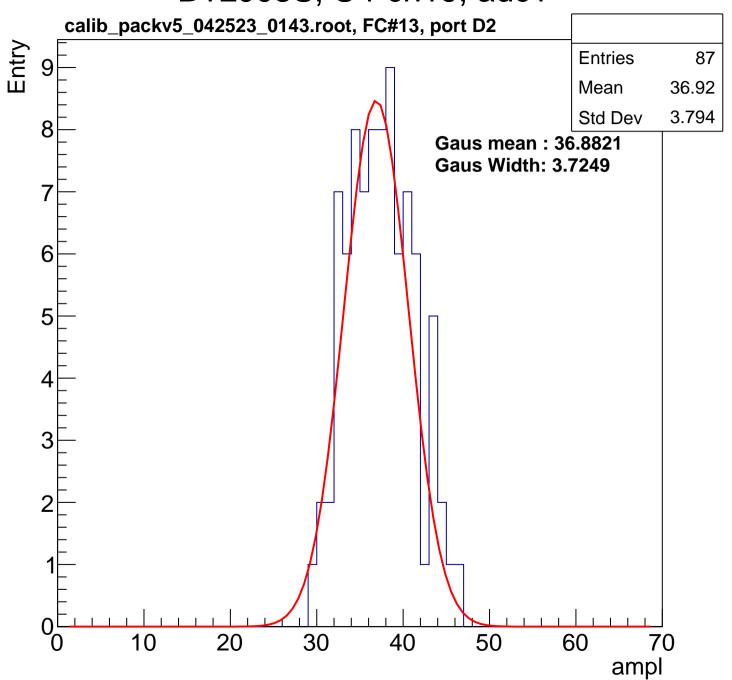


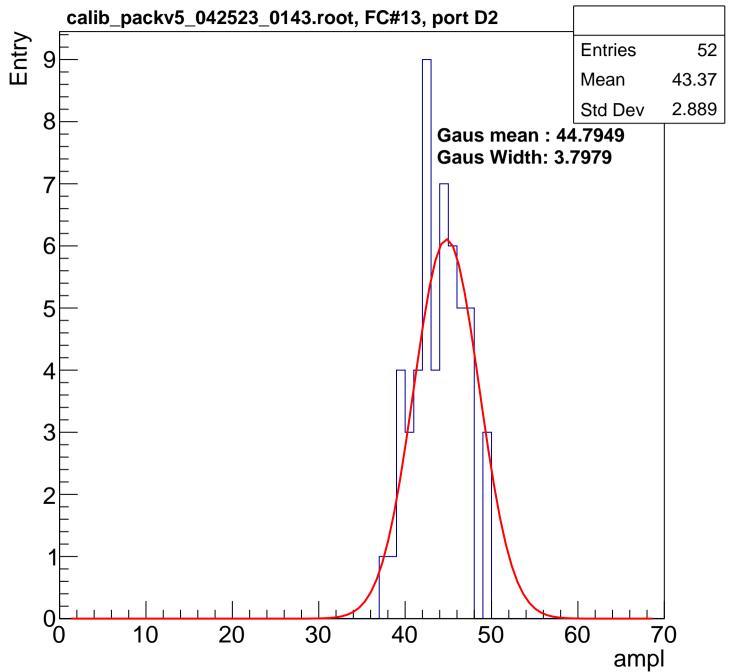


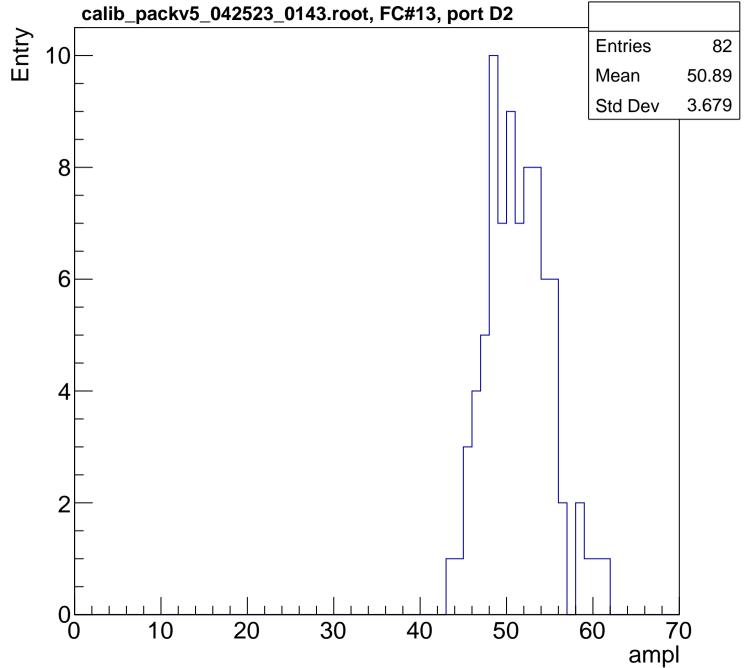


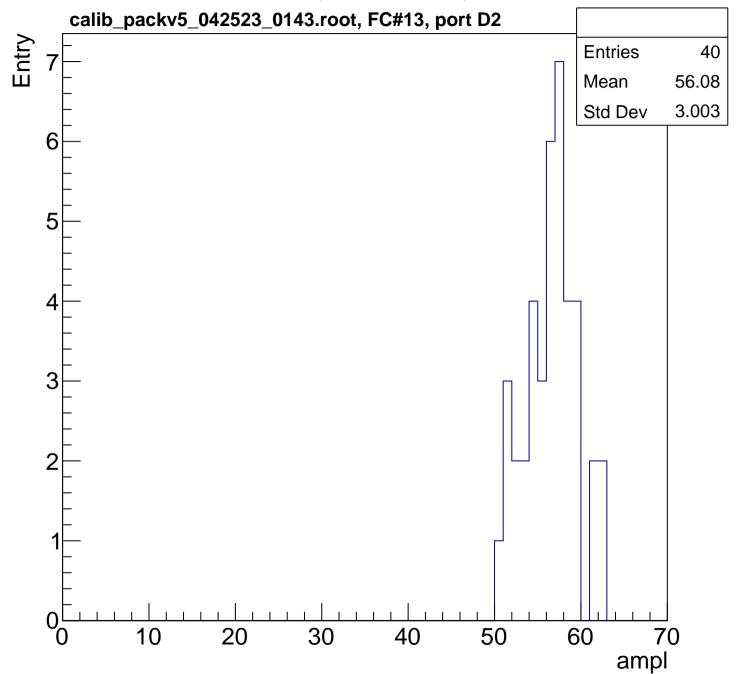


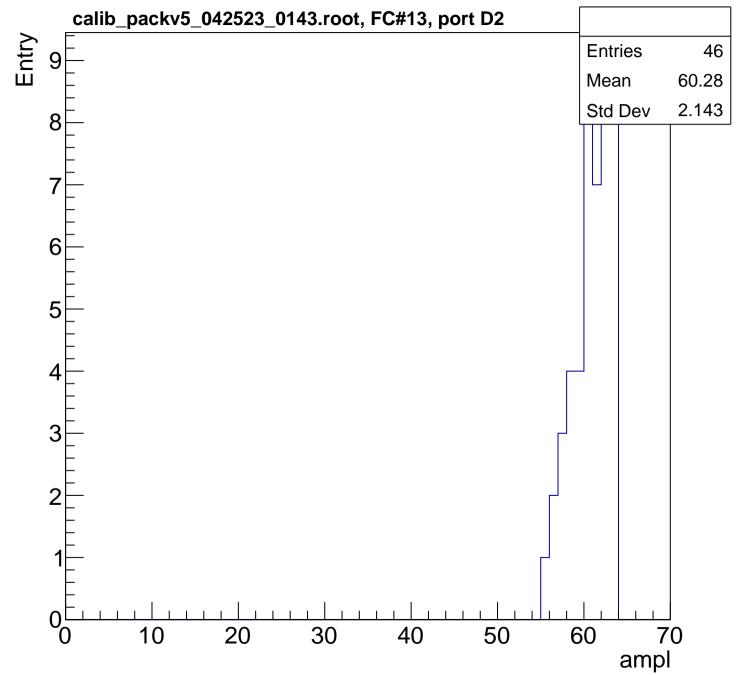


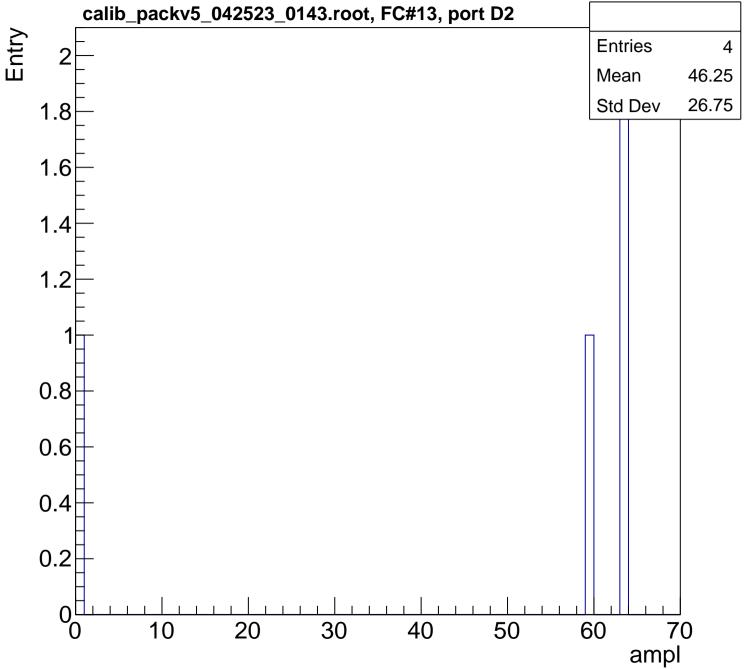


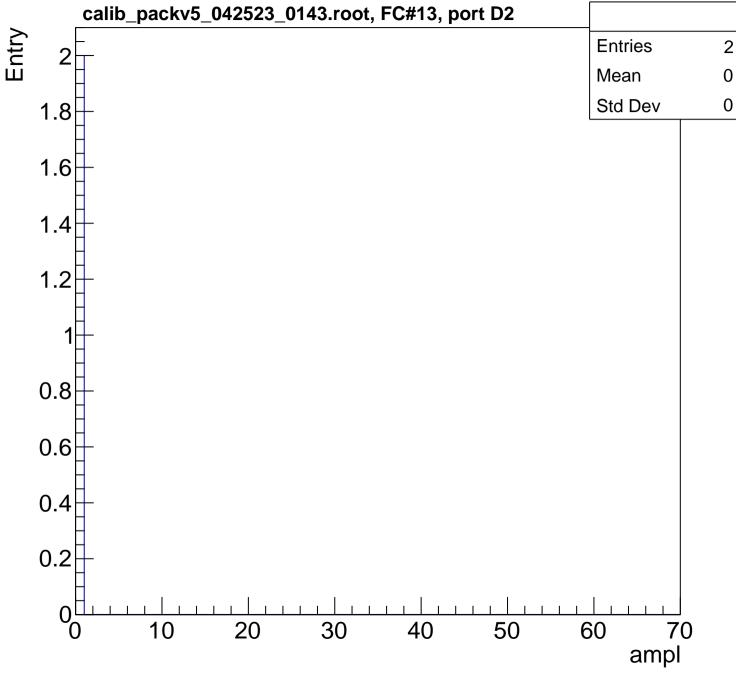


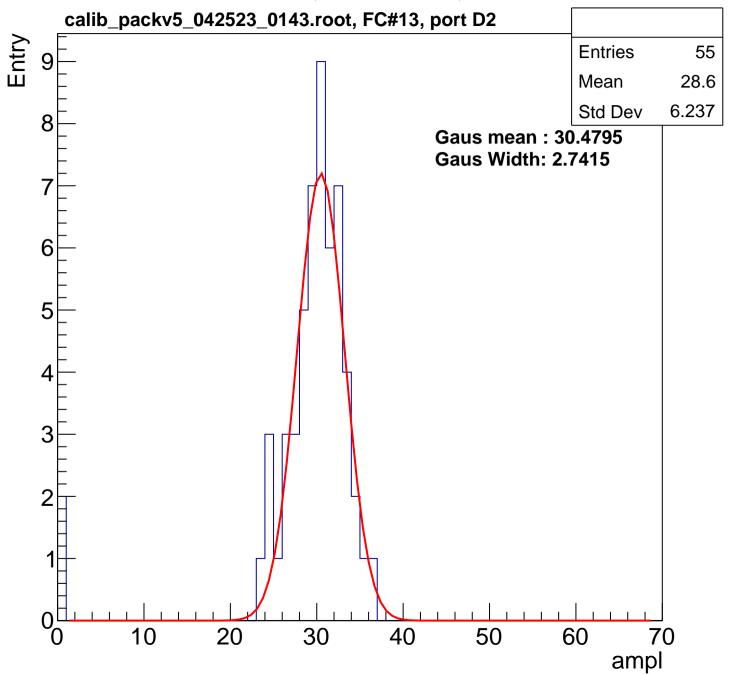


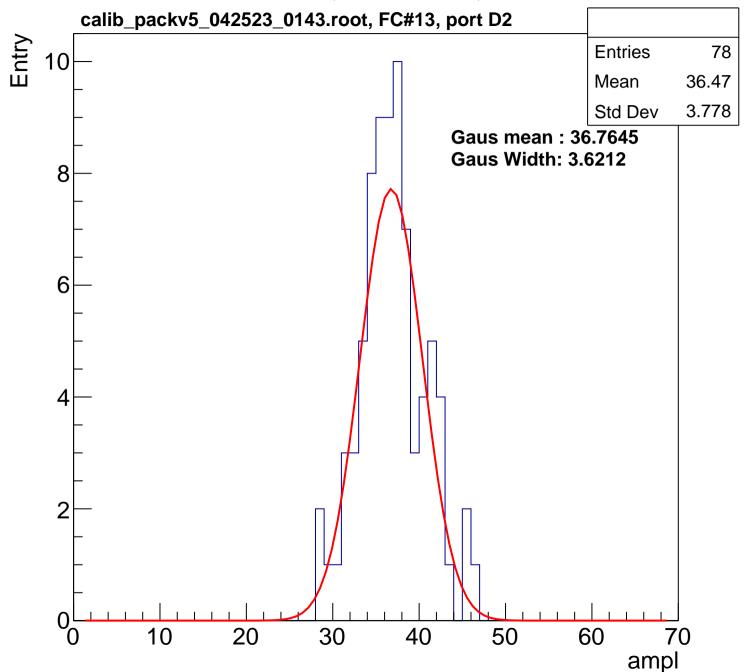


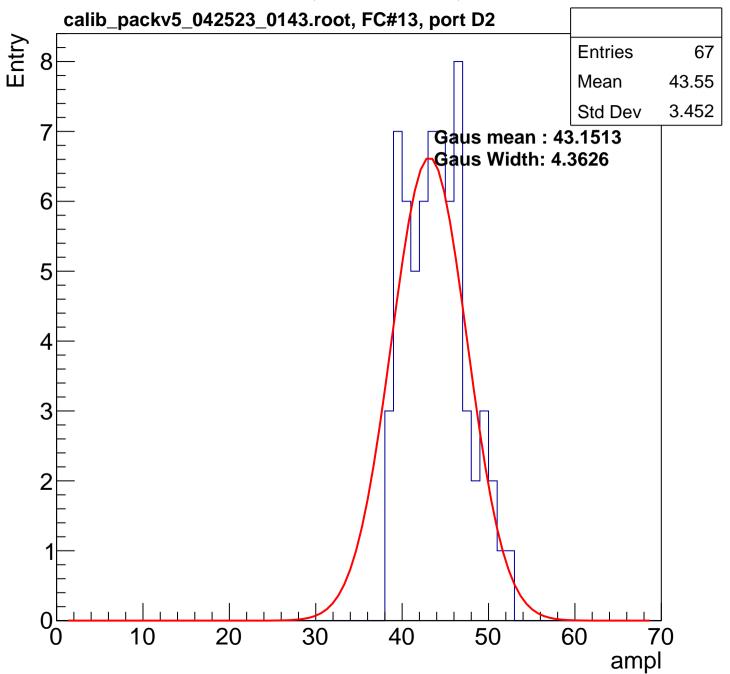


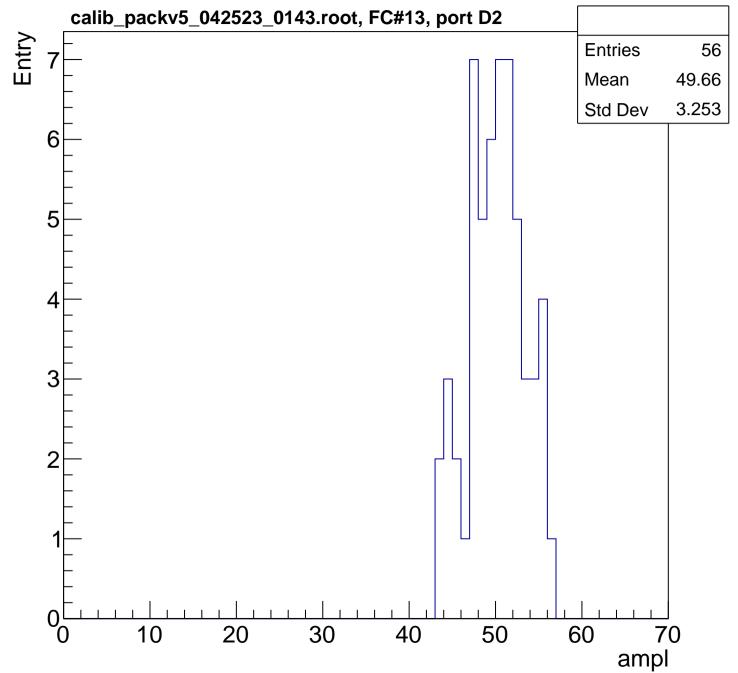


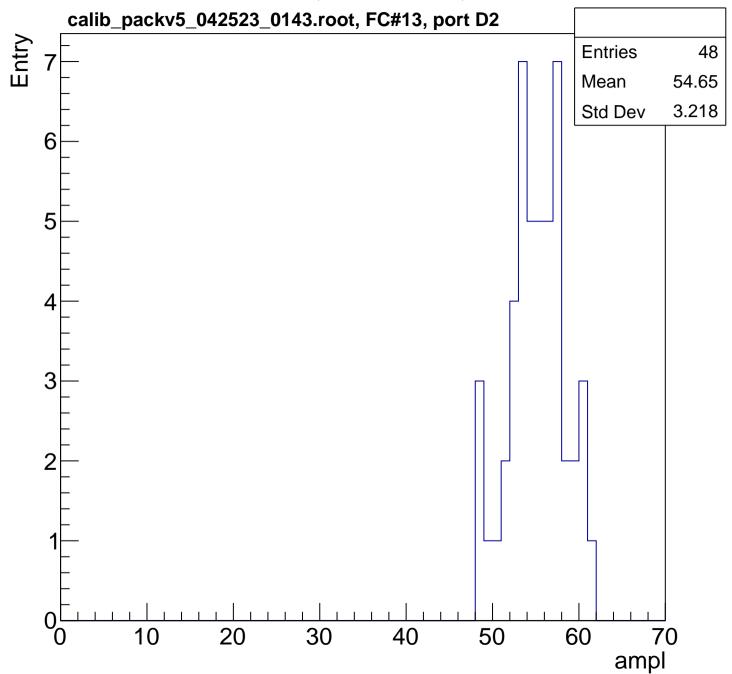


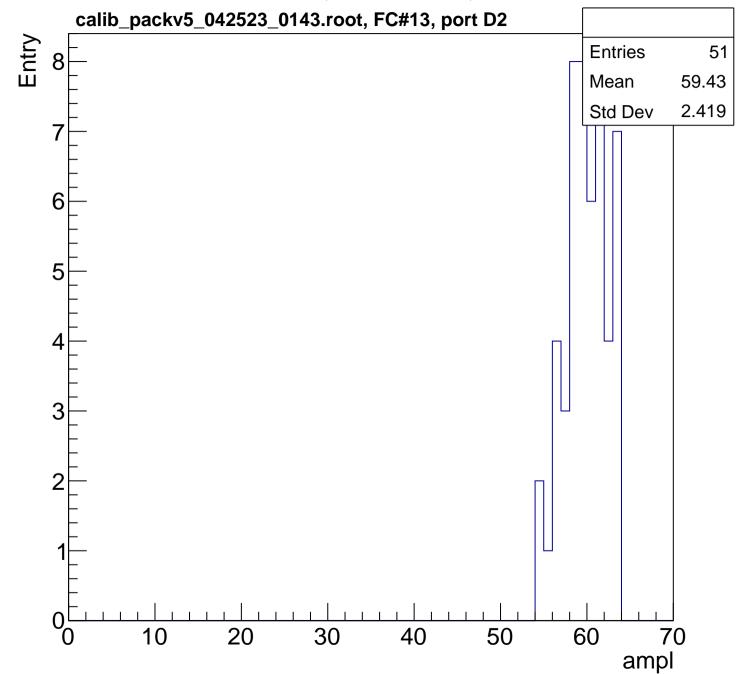


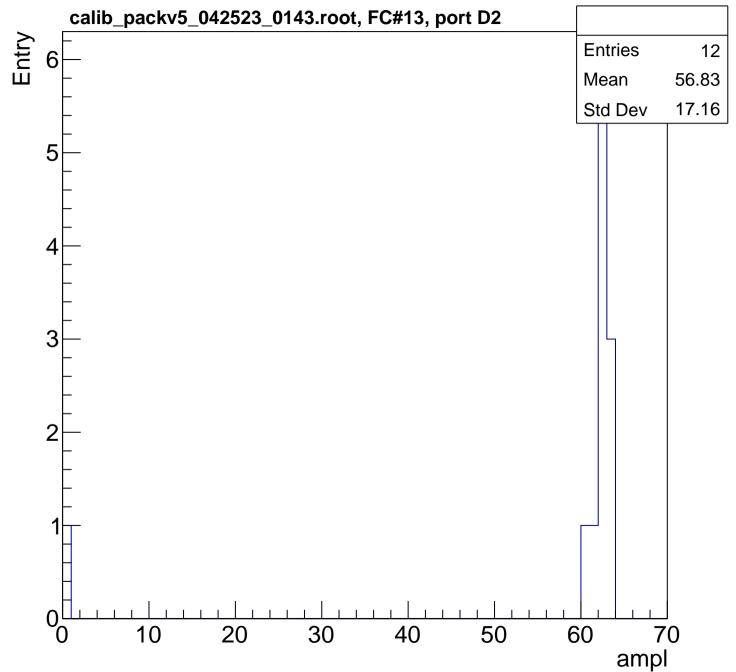


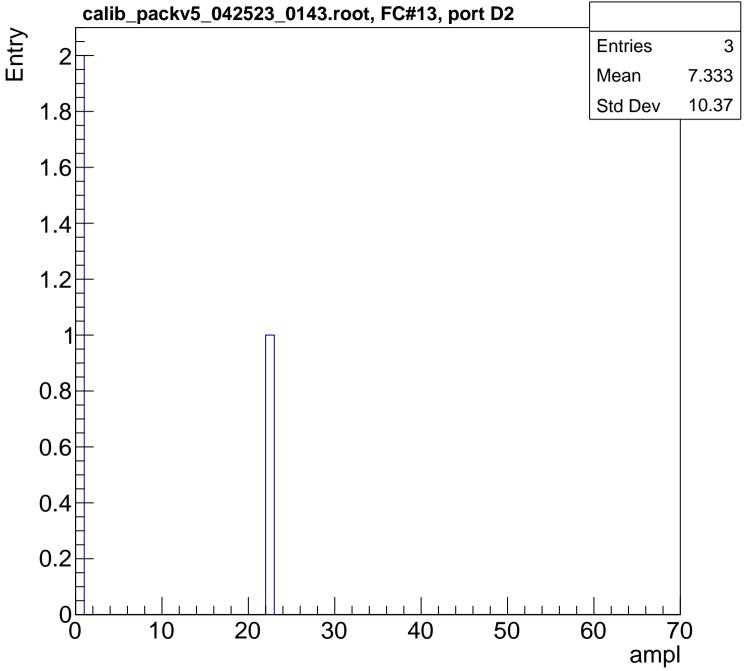


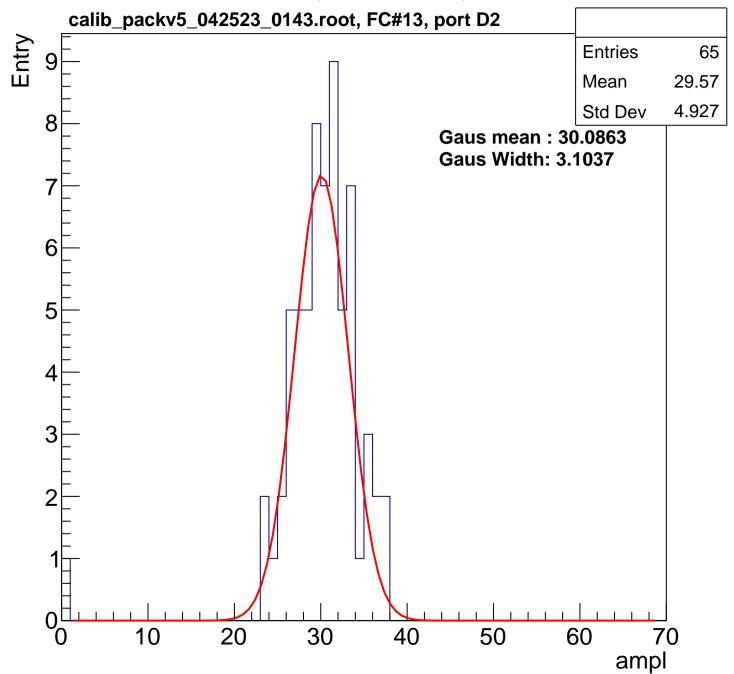


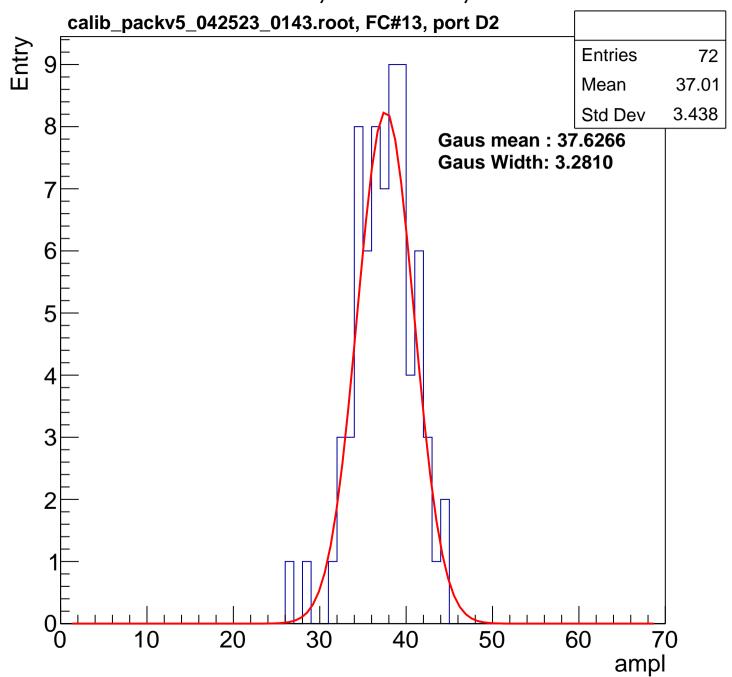


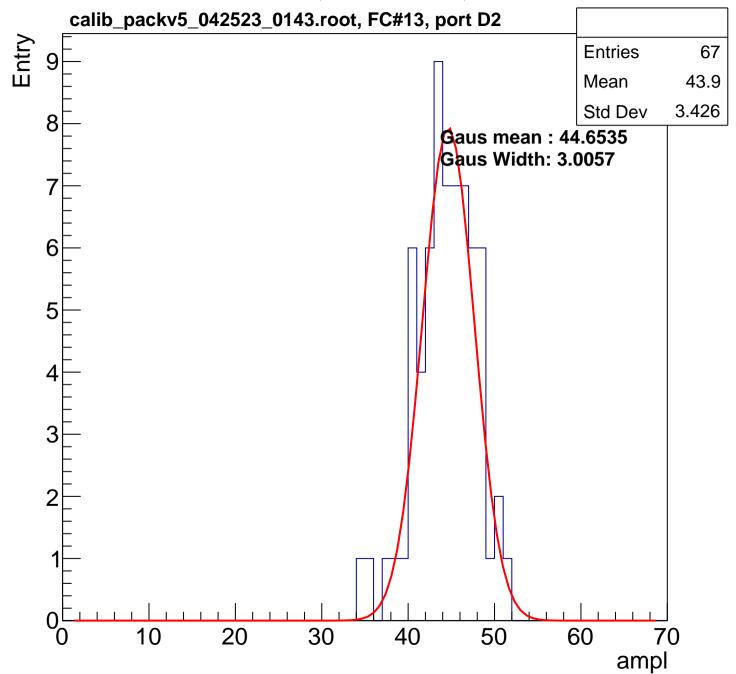


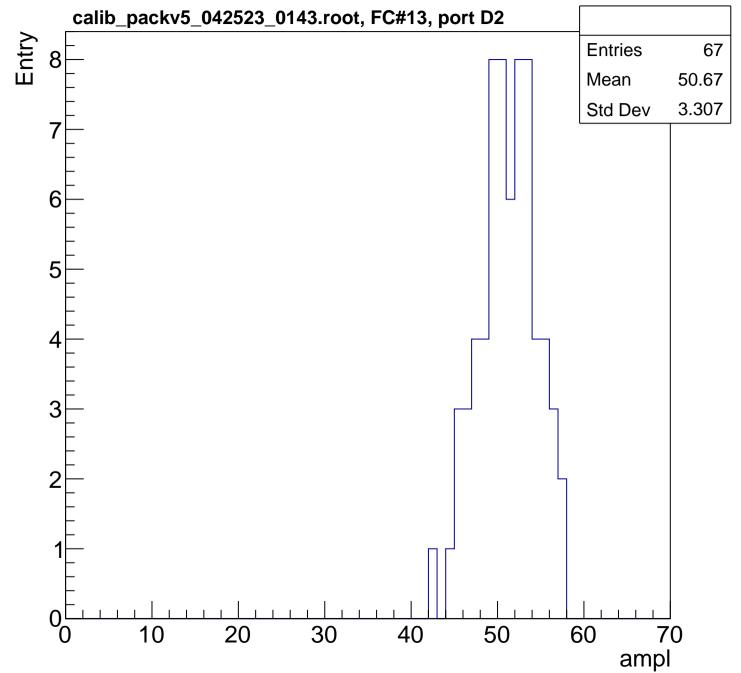


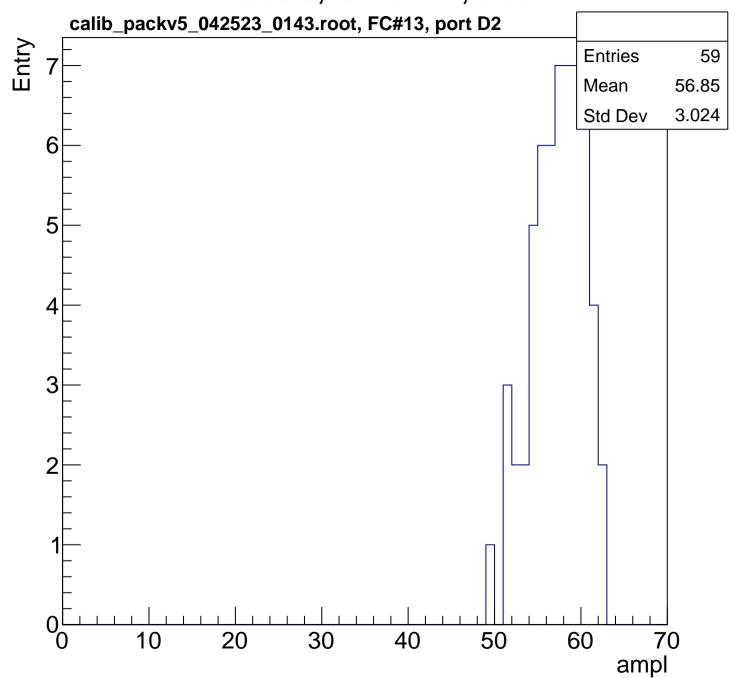


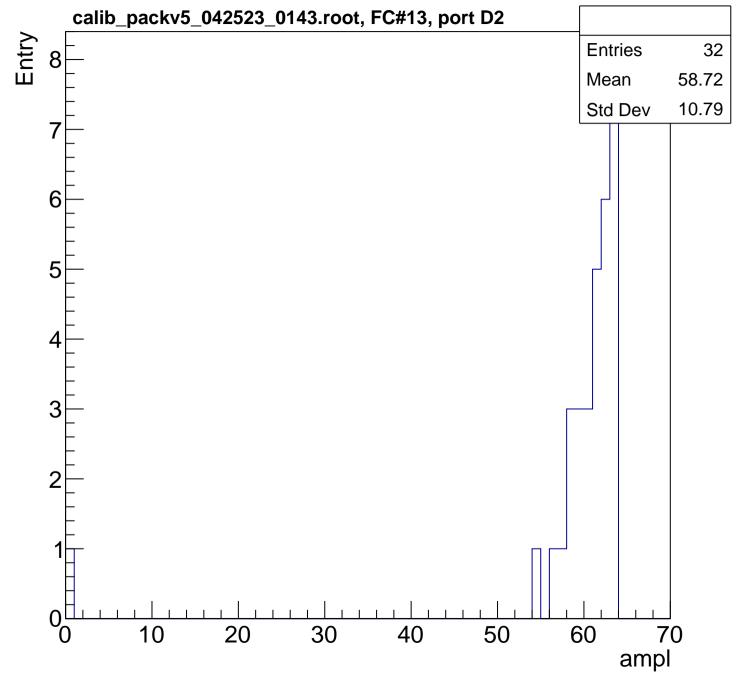


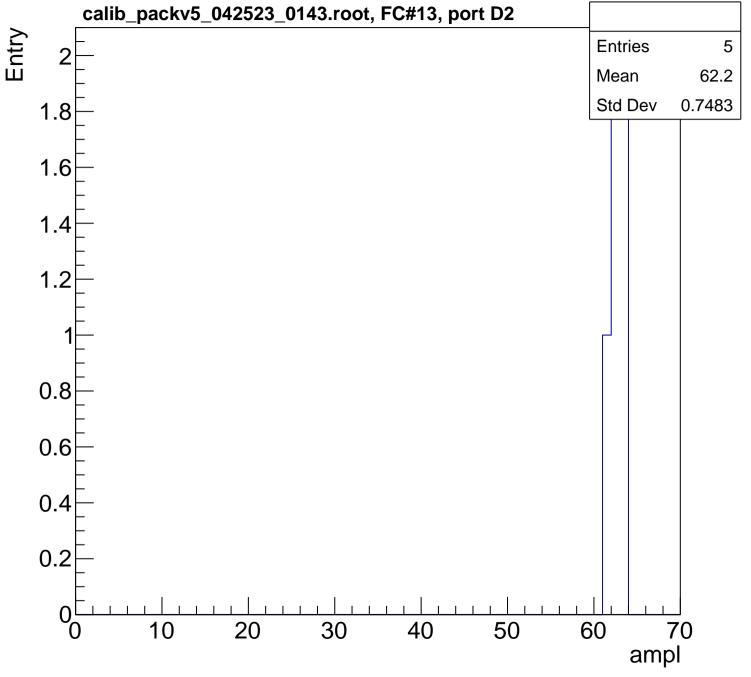




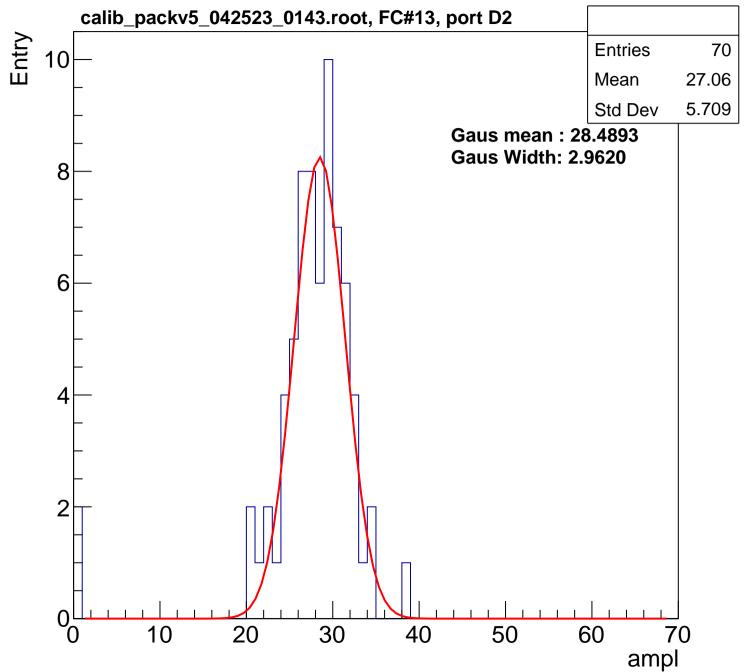


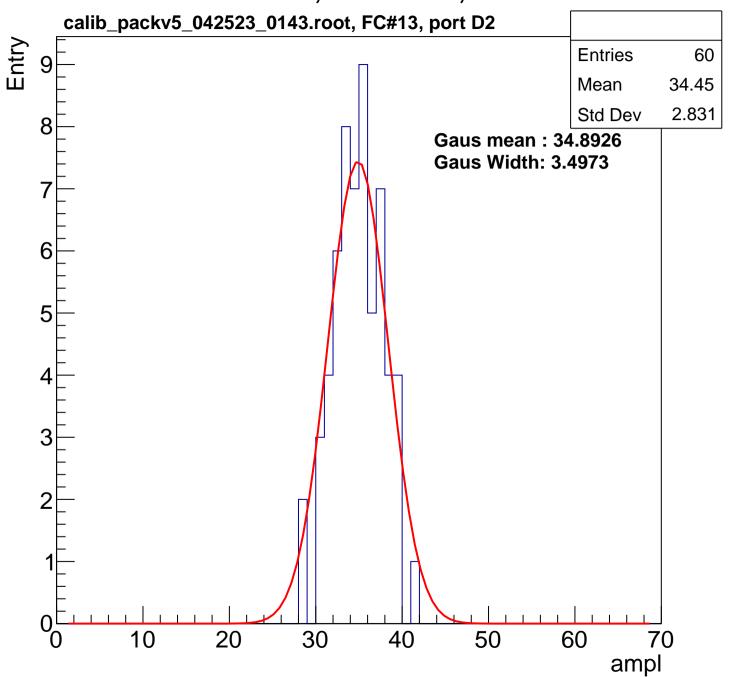


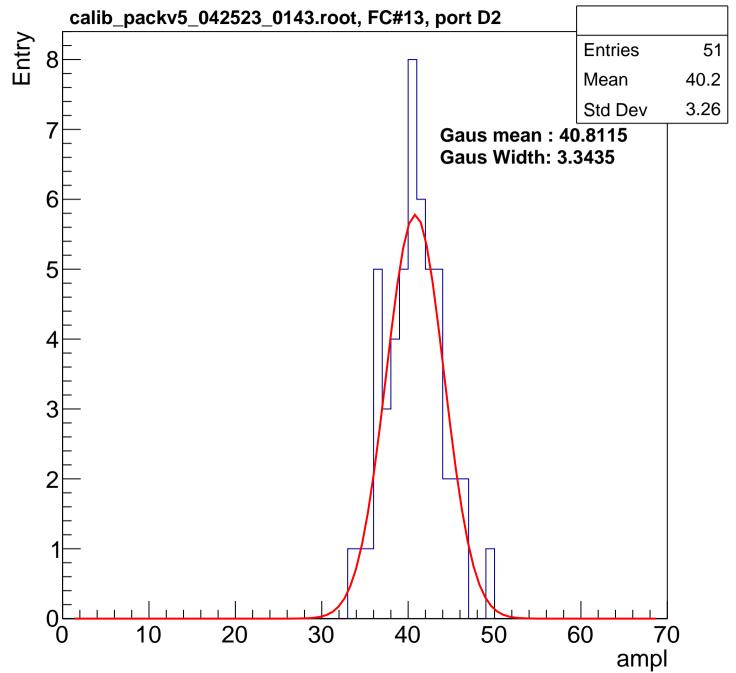


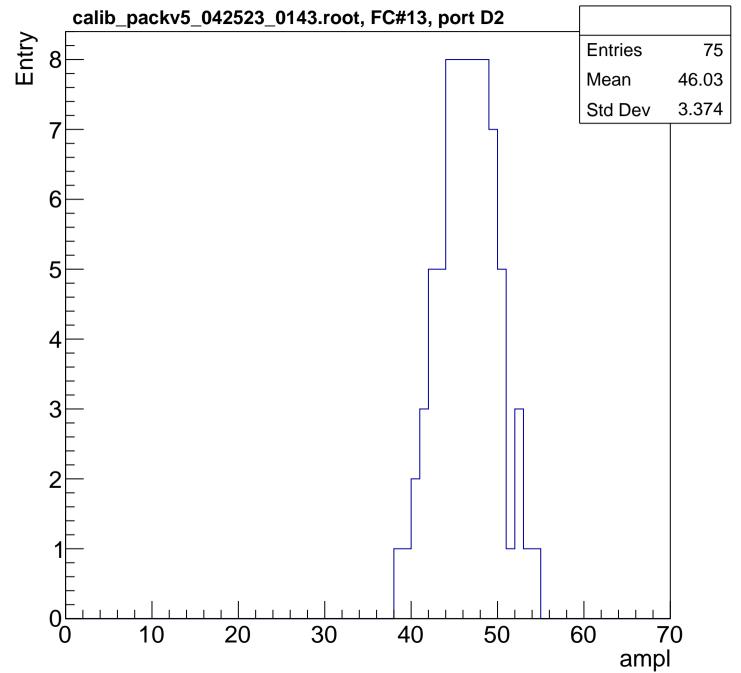


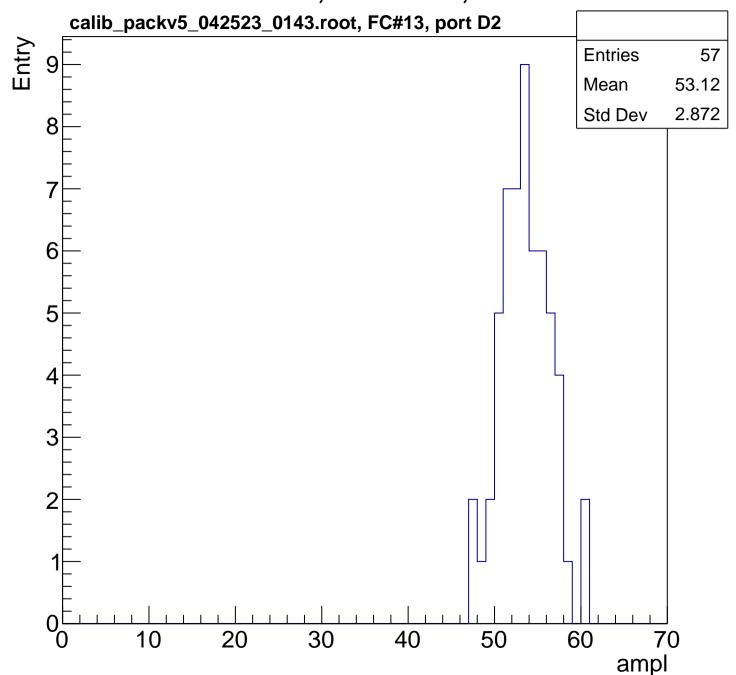


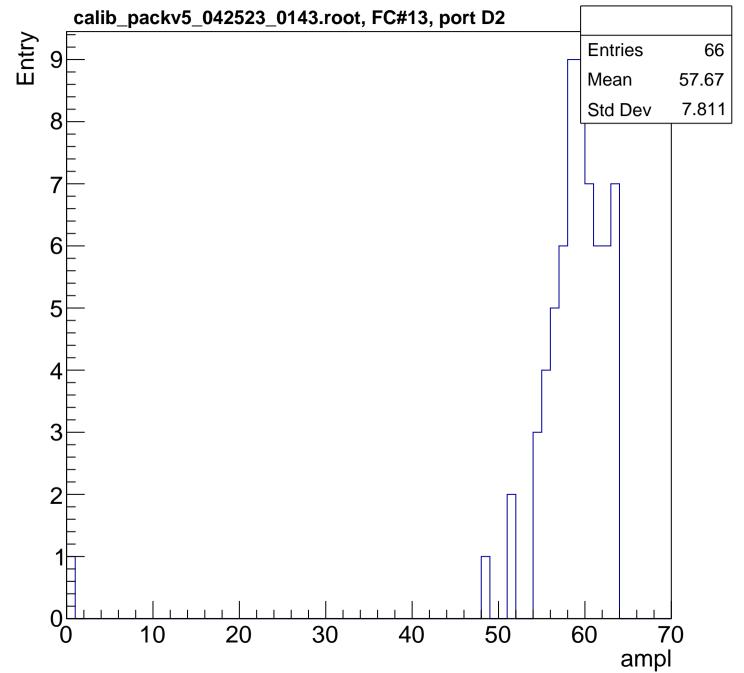


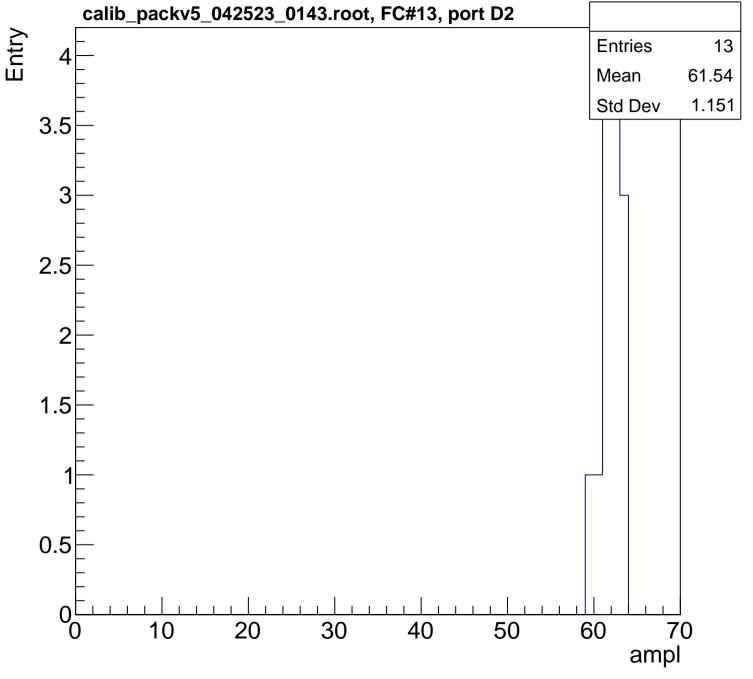


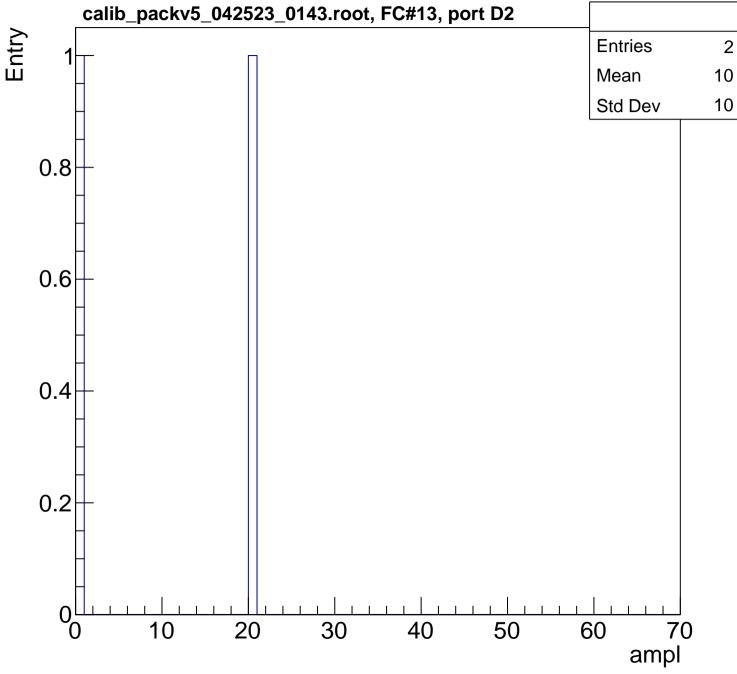


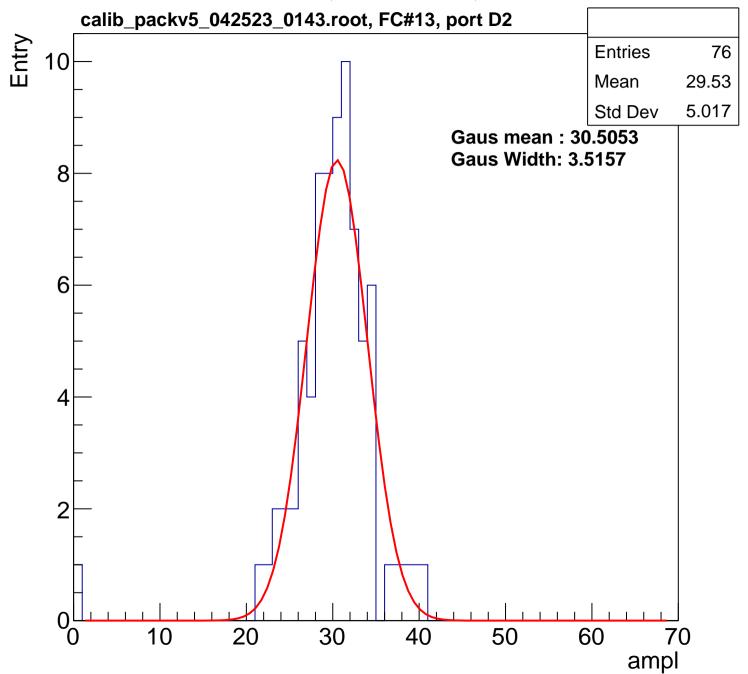


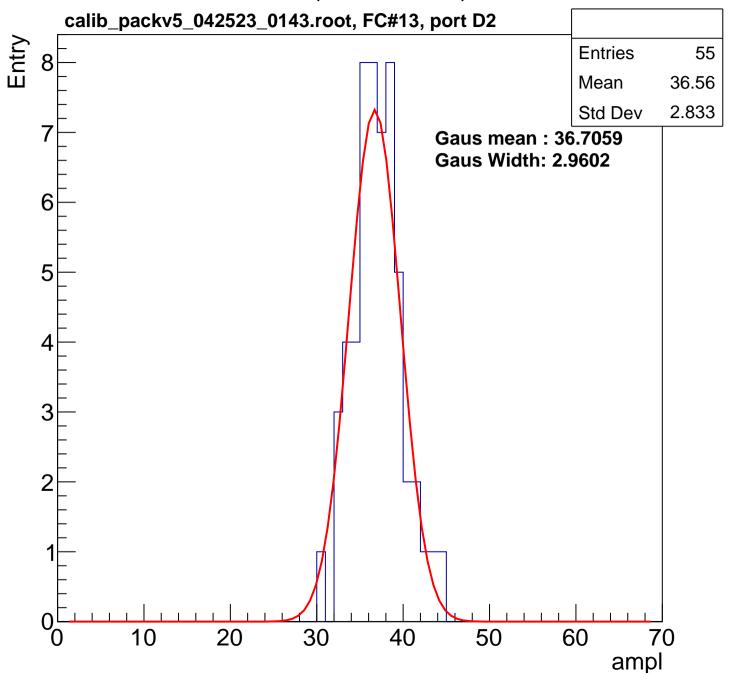


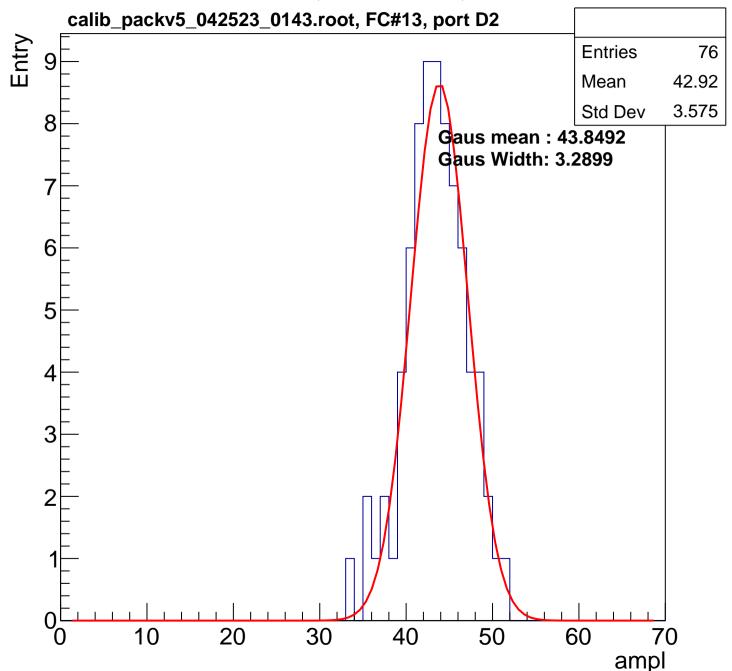


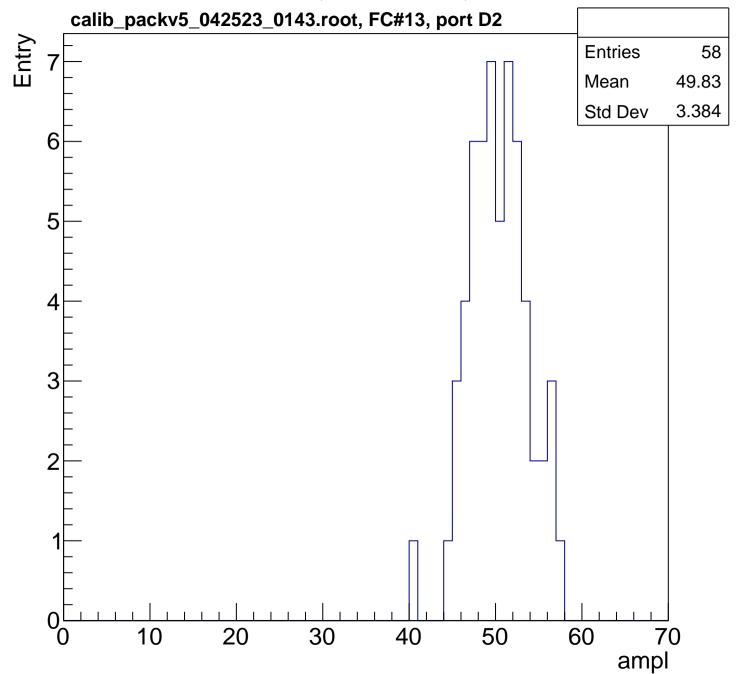


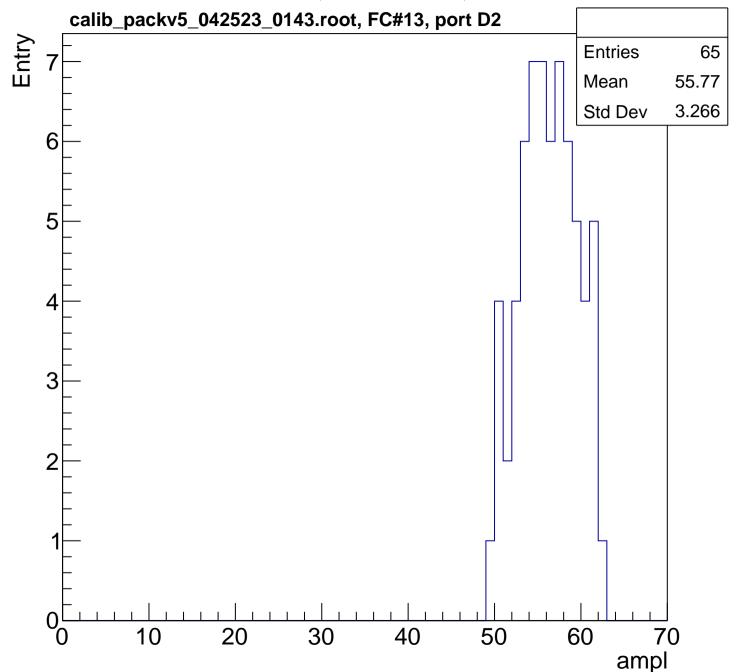


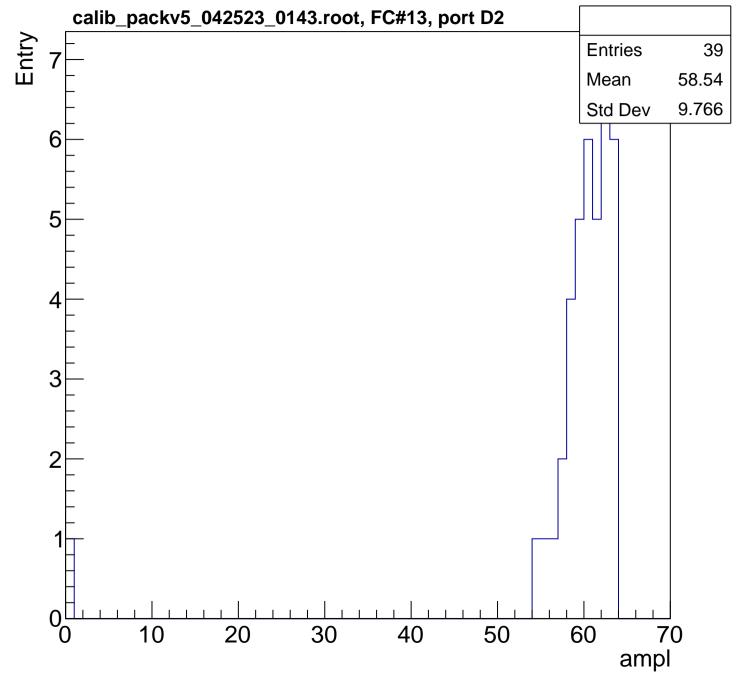


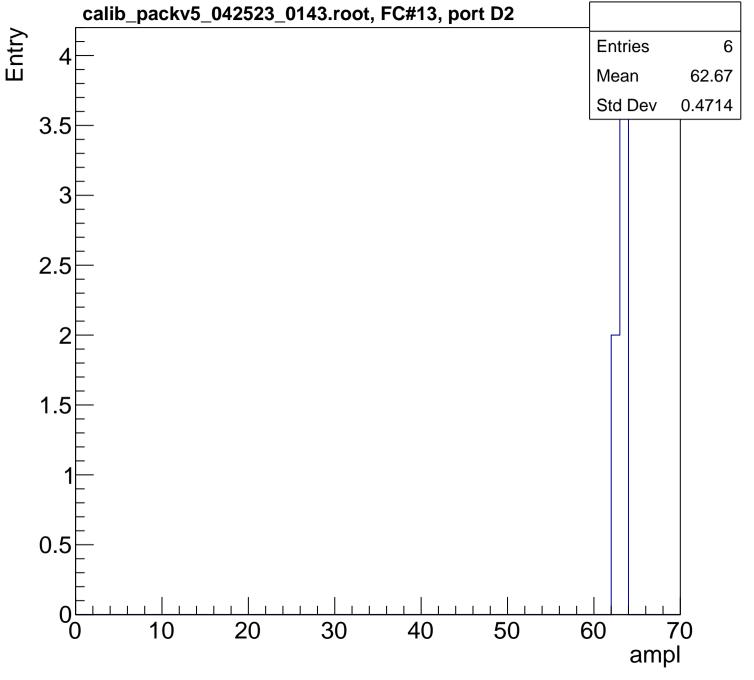


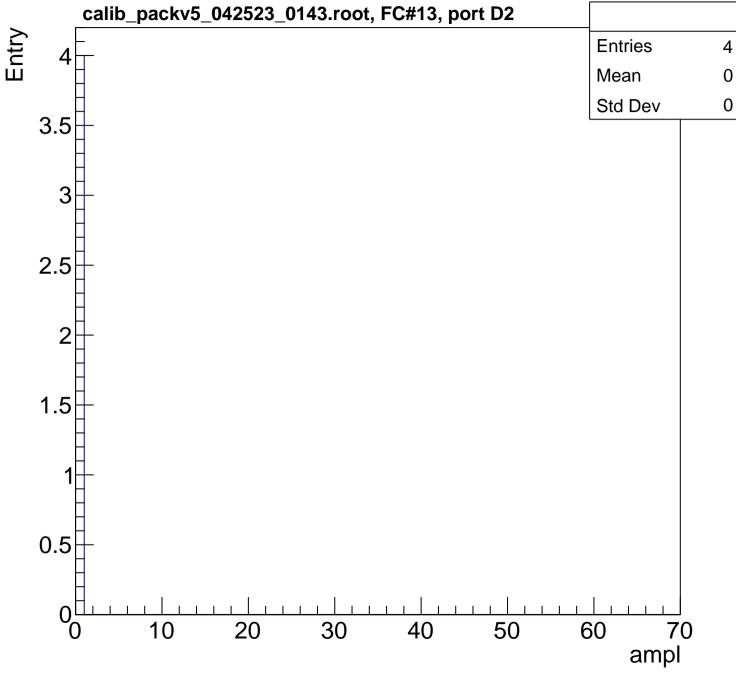


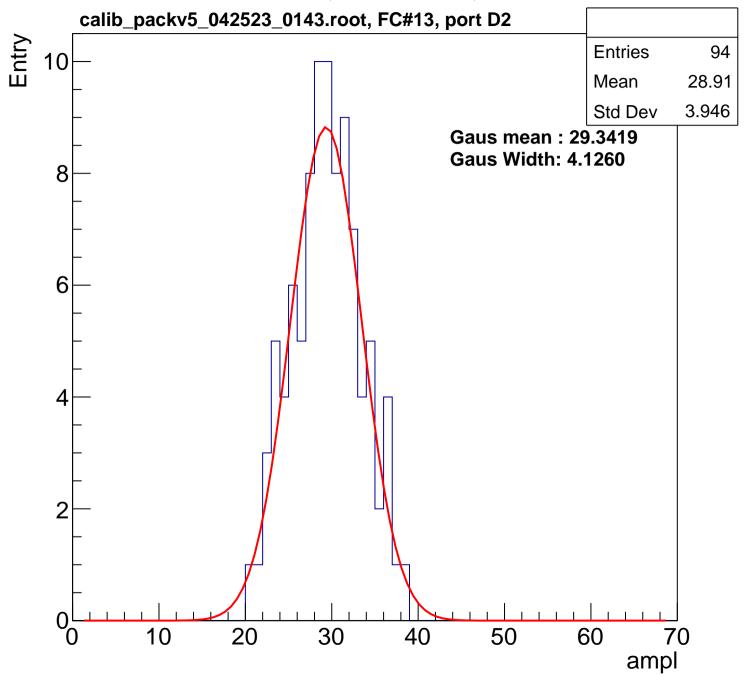


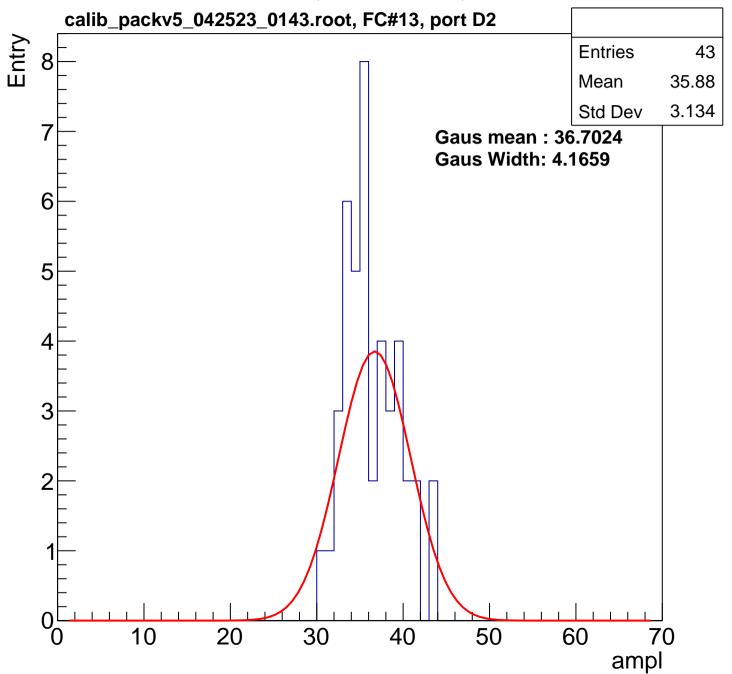


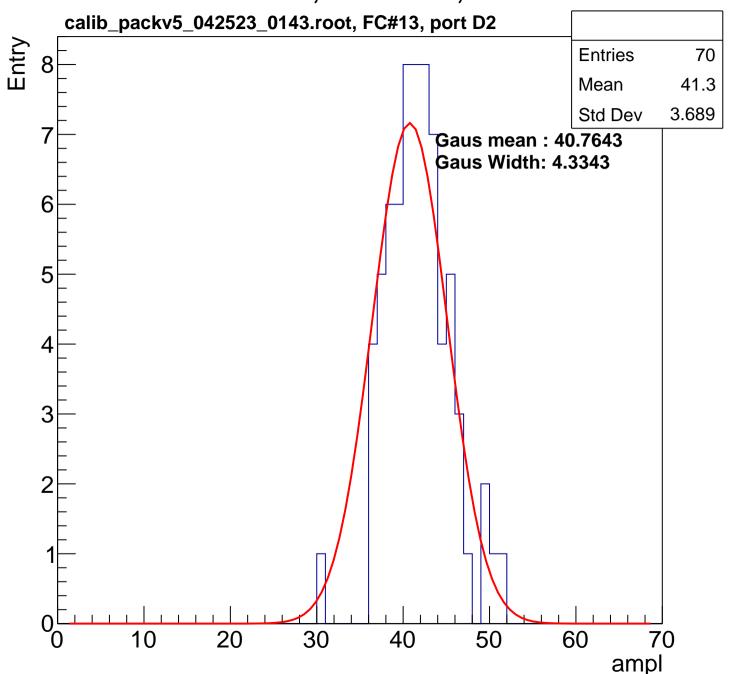


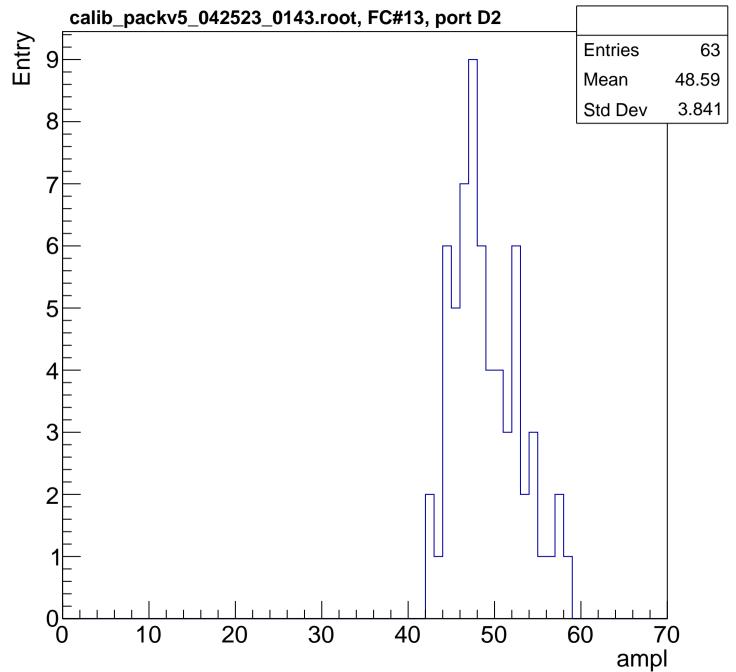


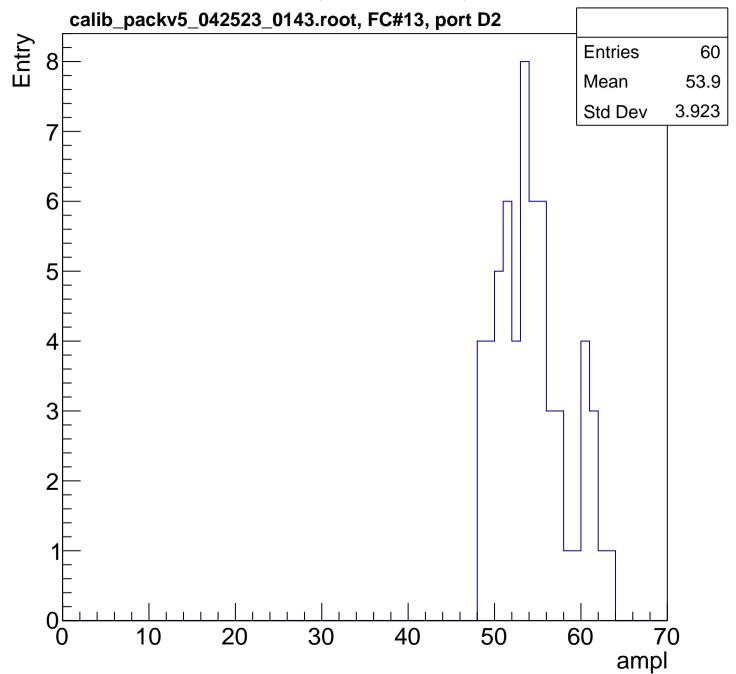


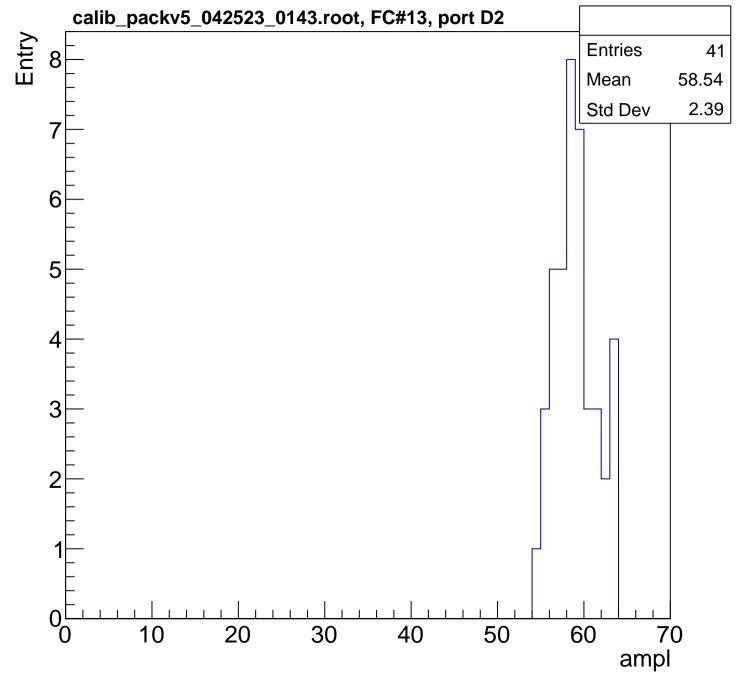


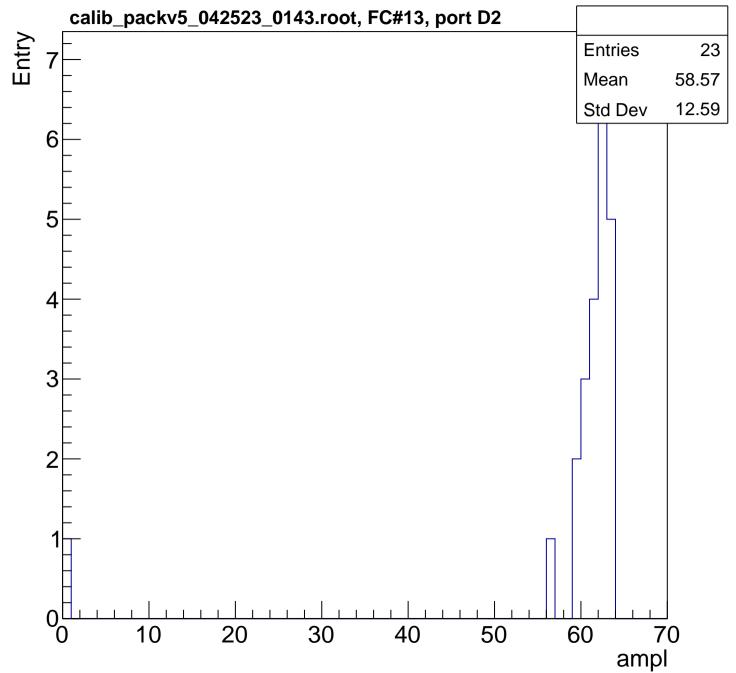






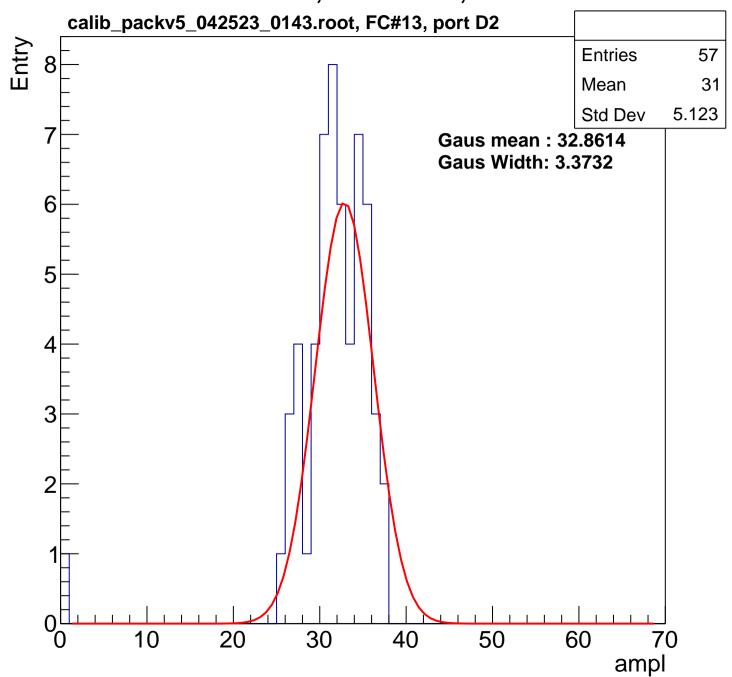


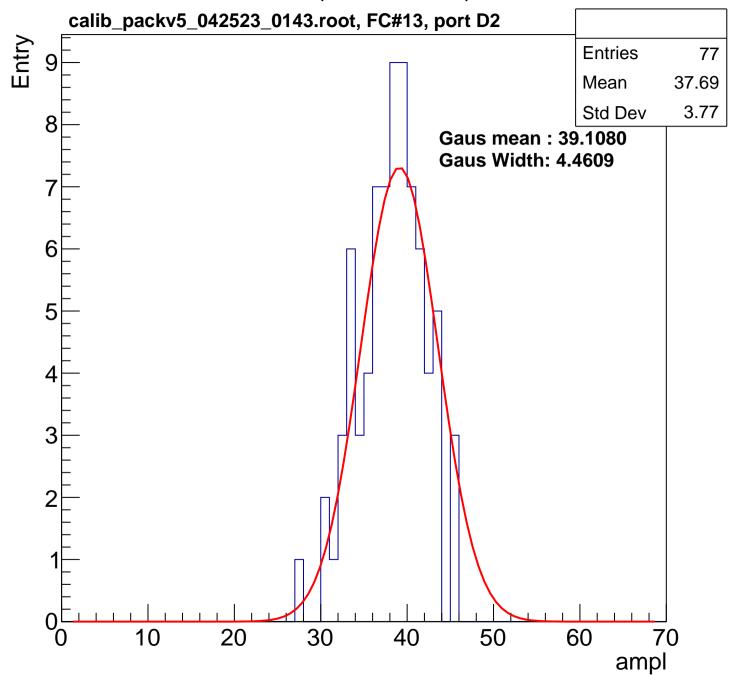


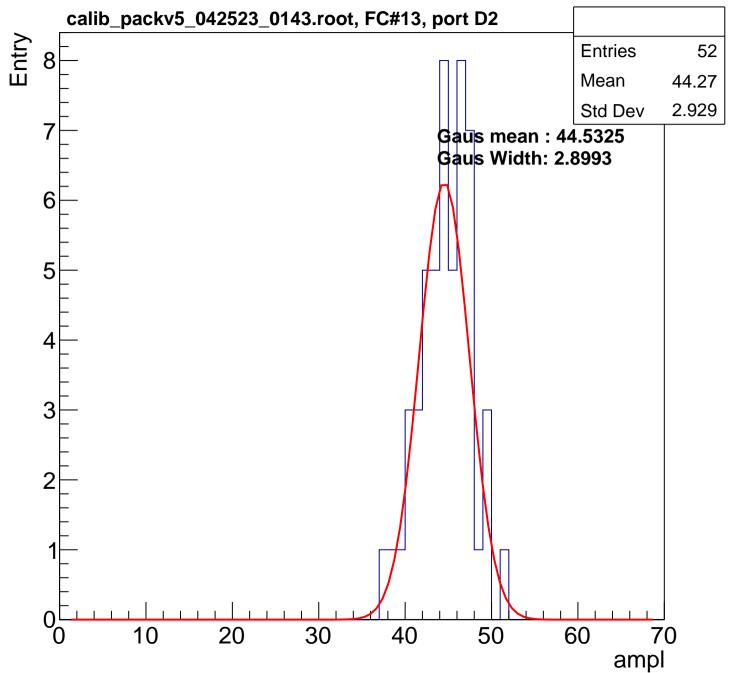


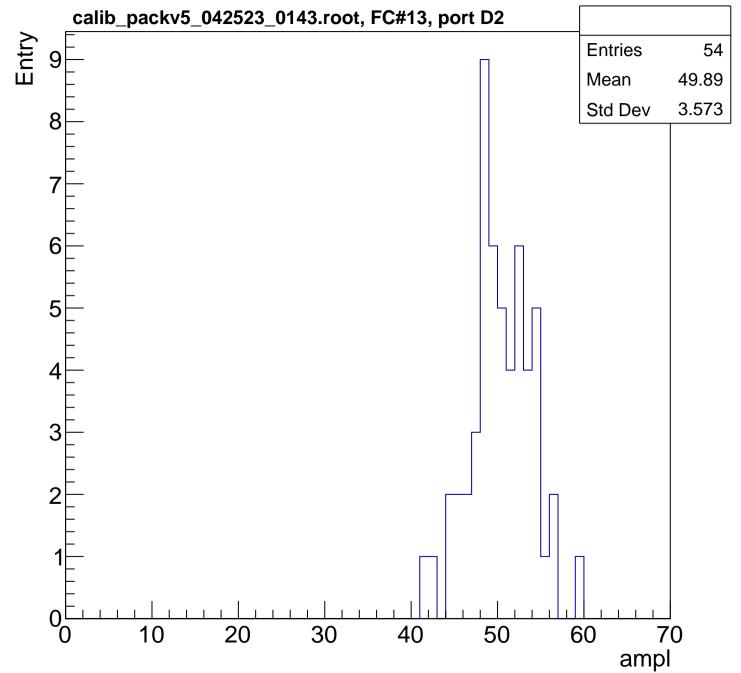
B1L003S, U4-ch24, adc7 calib_packv5_042523_0143.root, FC#13, port D2 Entry **Entries** Mean 19 Std Dev 0 8.0 0.6 0.4 0.2 10 20 30 40 50 60 70

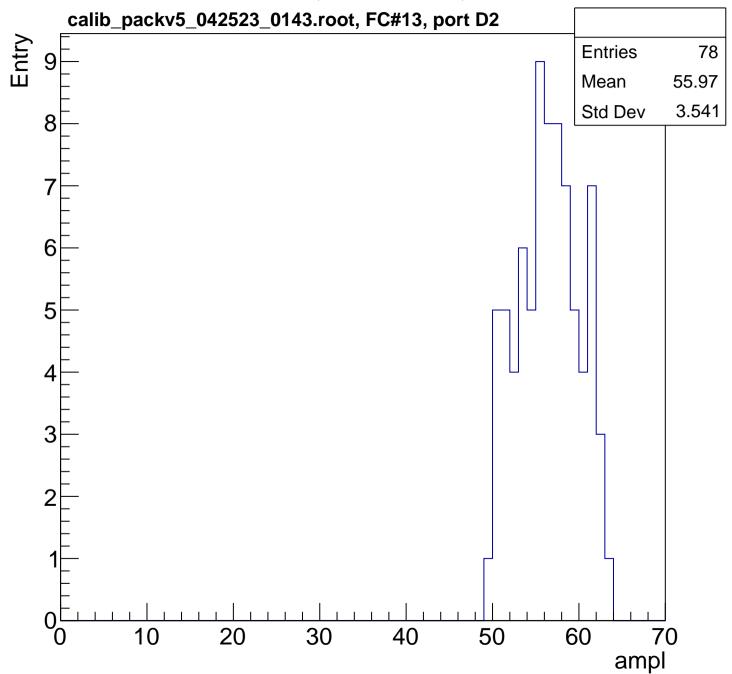
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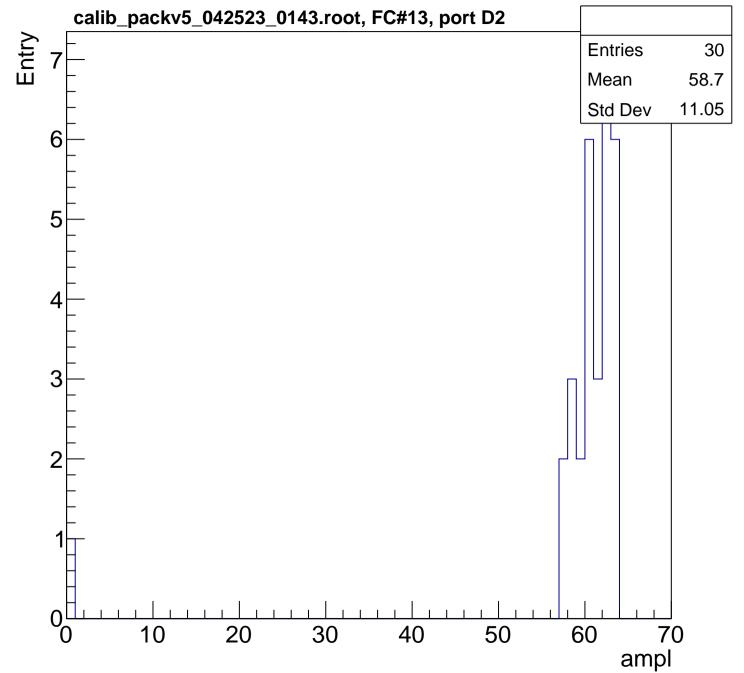


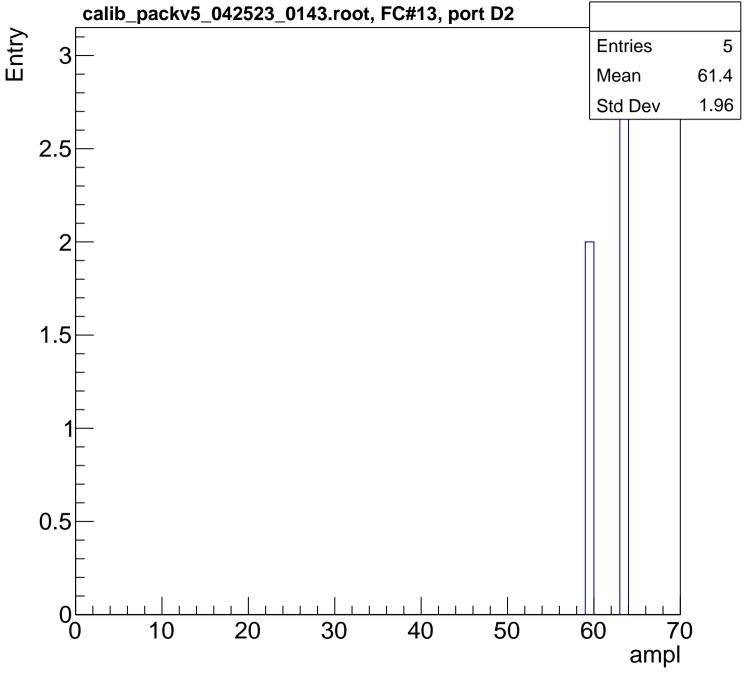


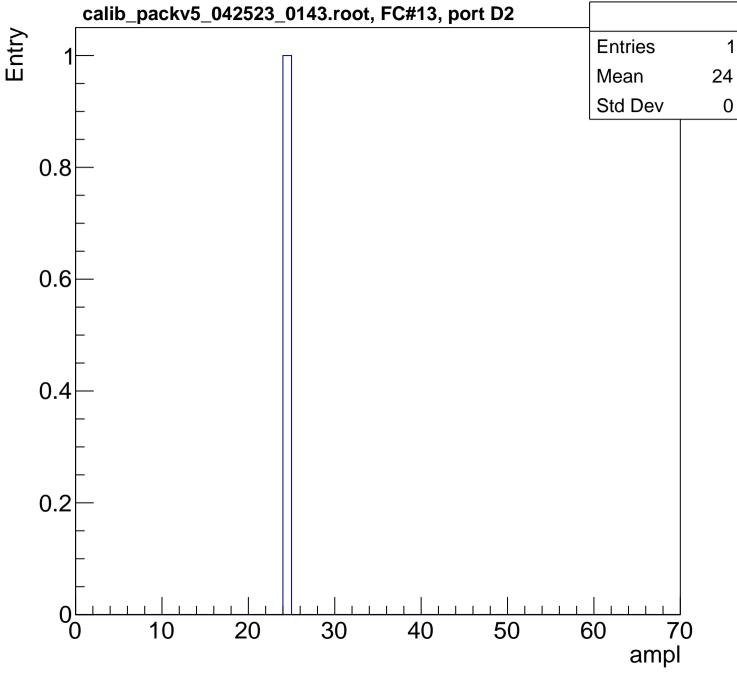


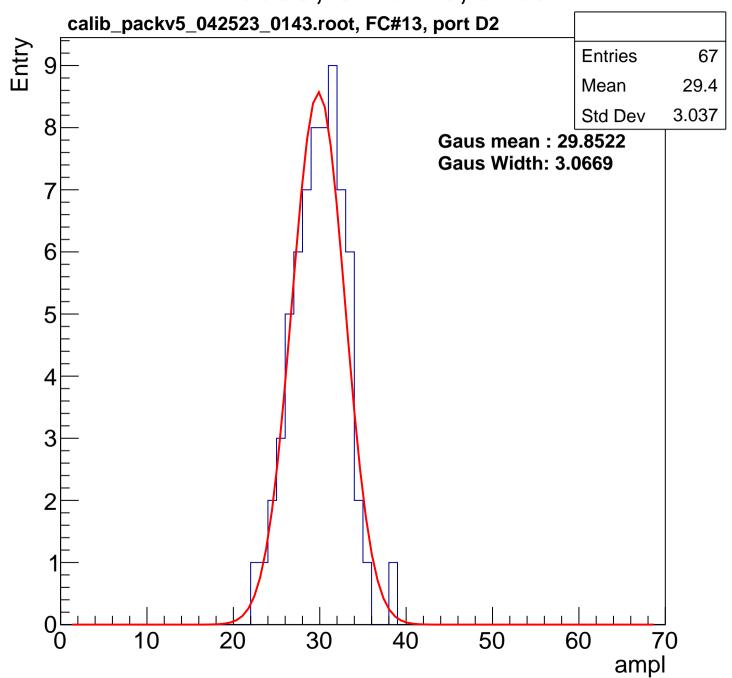


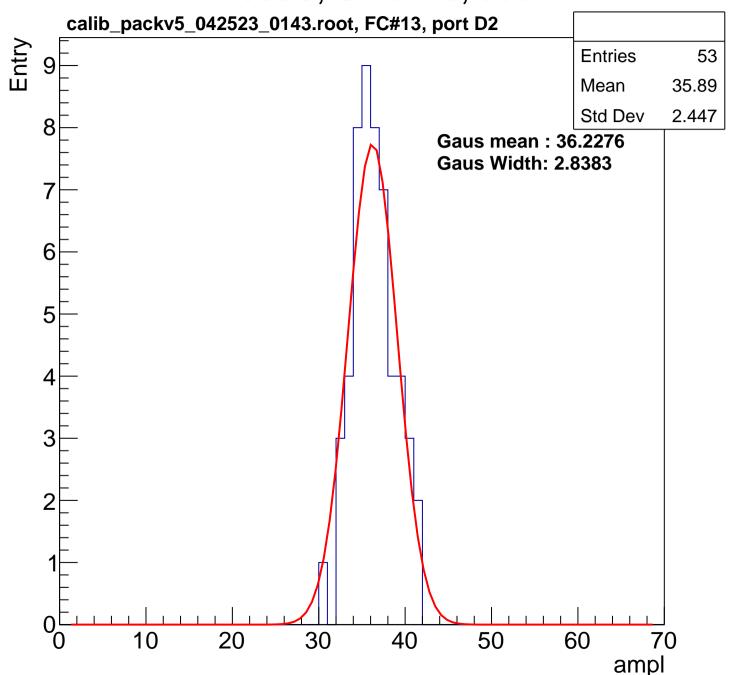


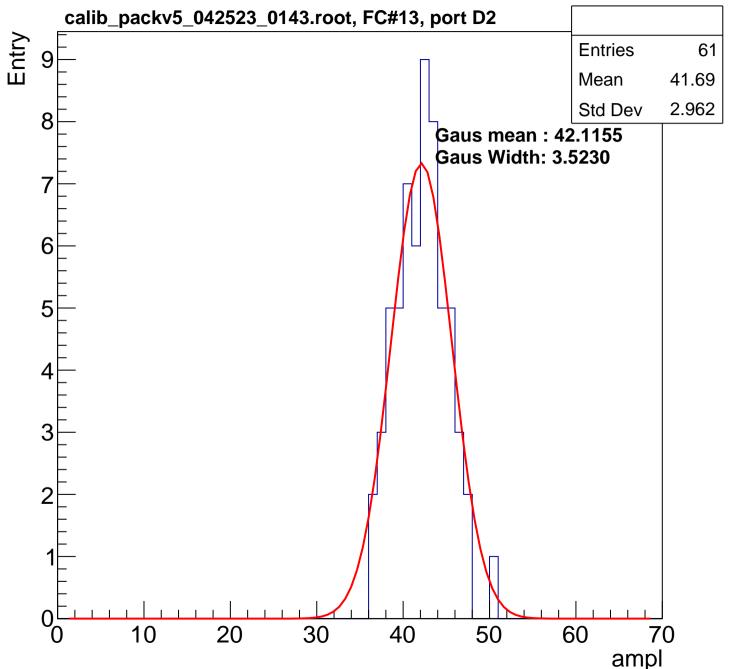


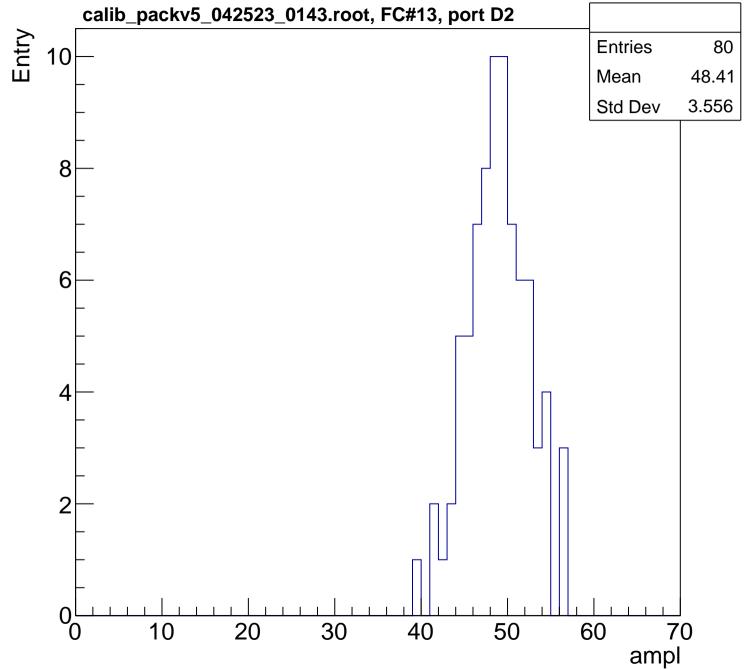


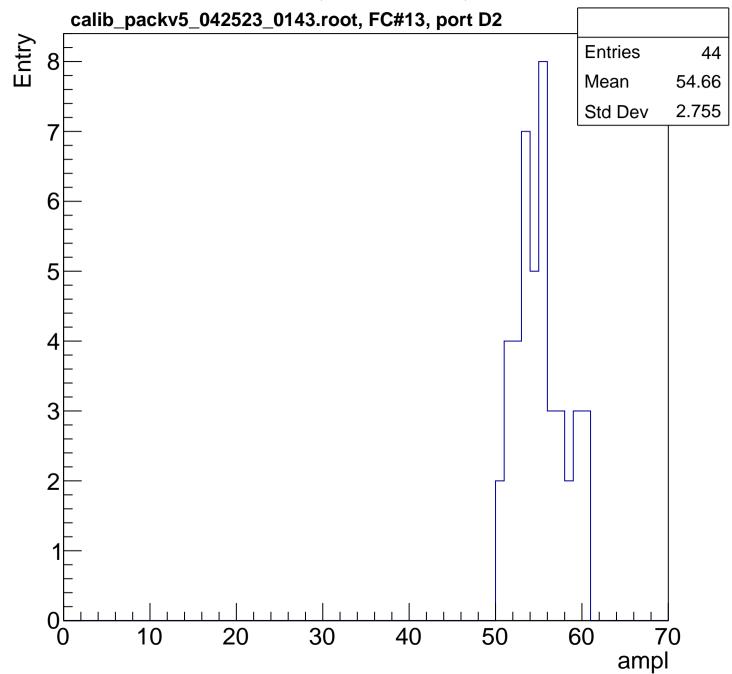


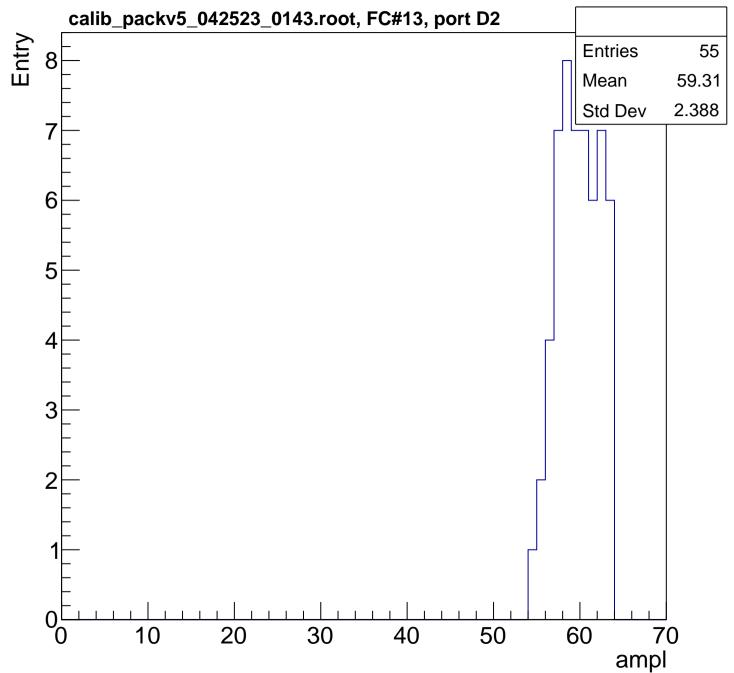


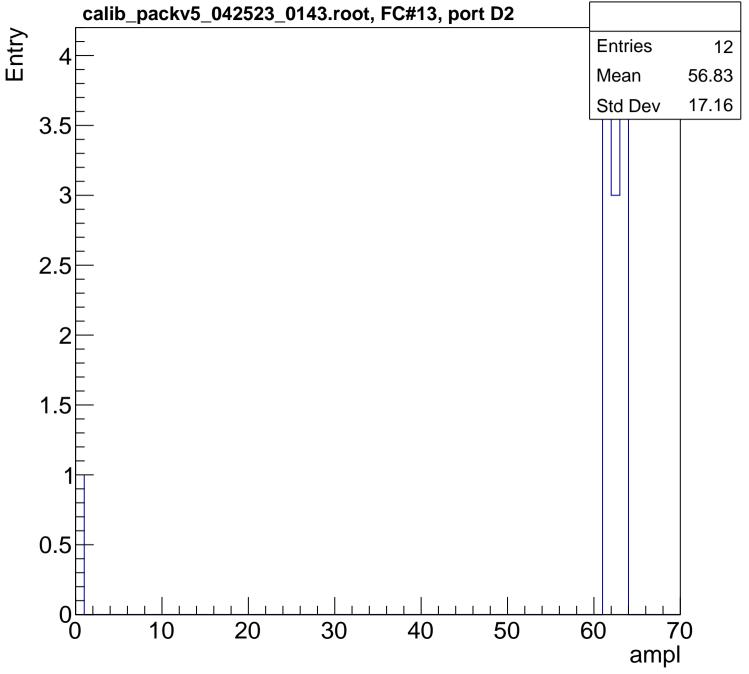




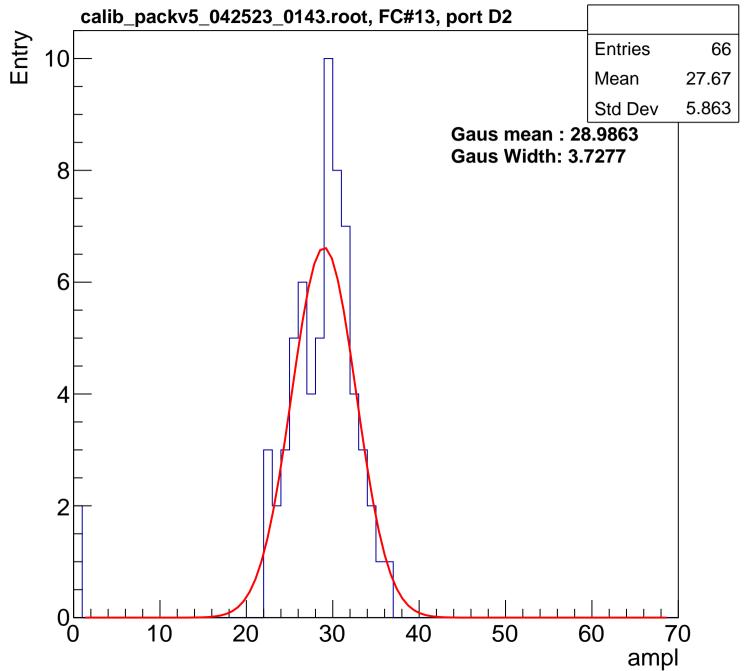


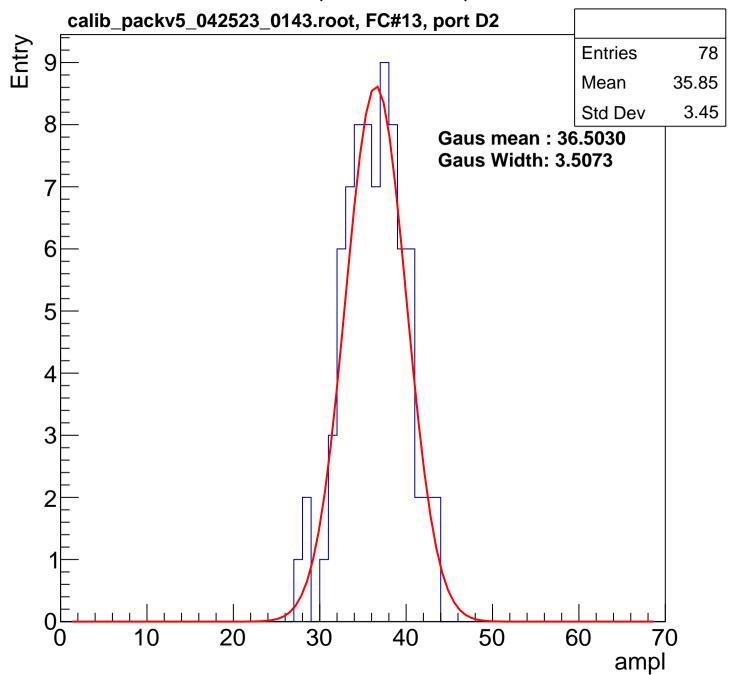


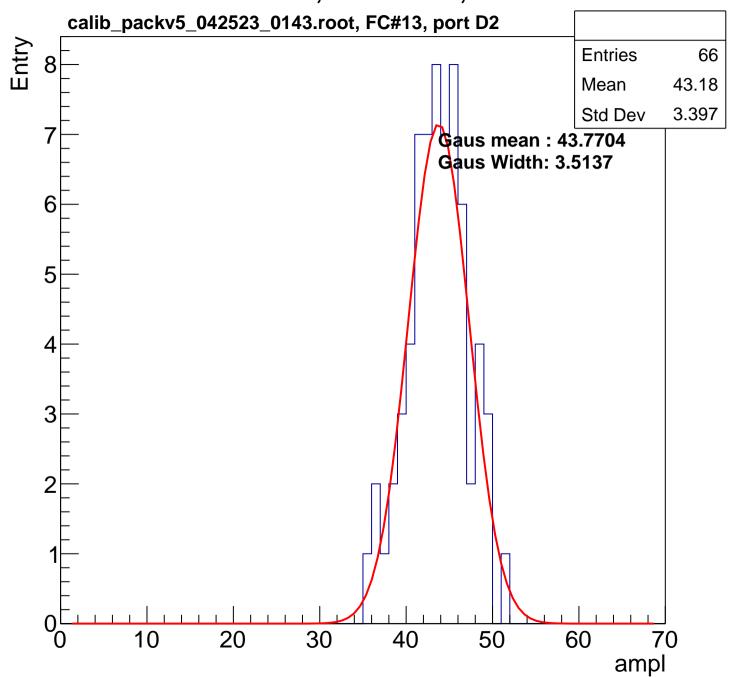


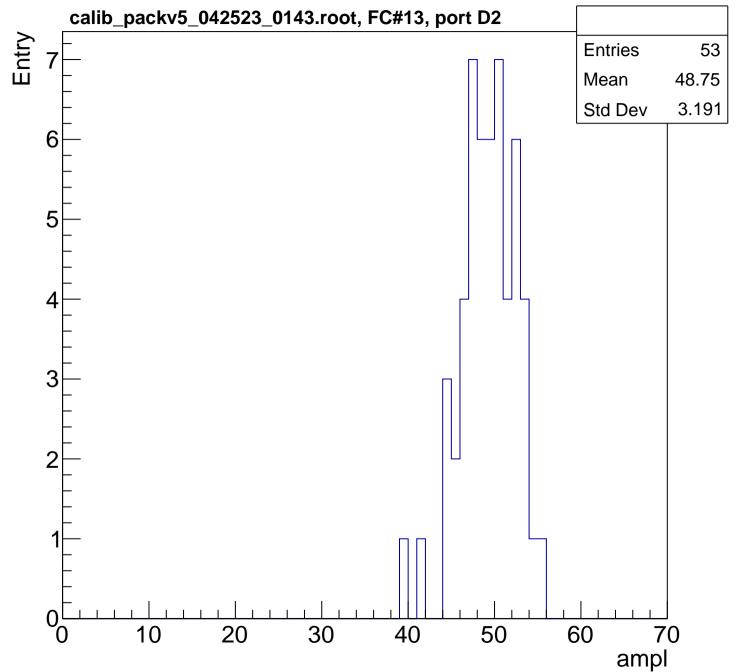


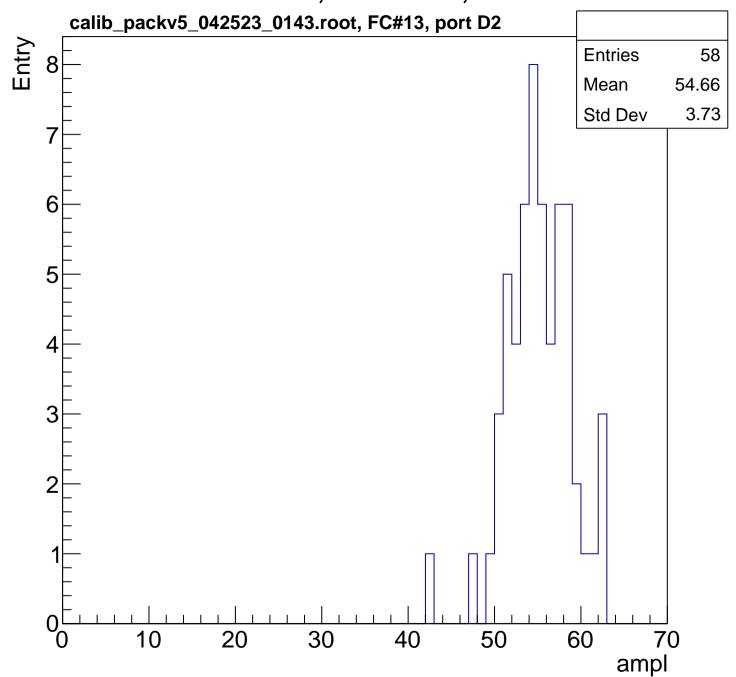


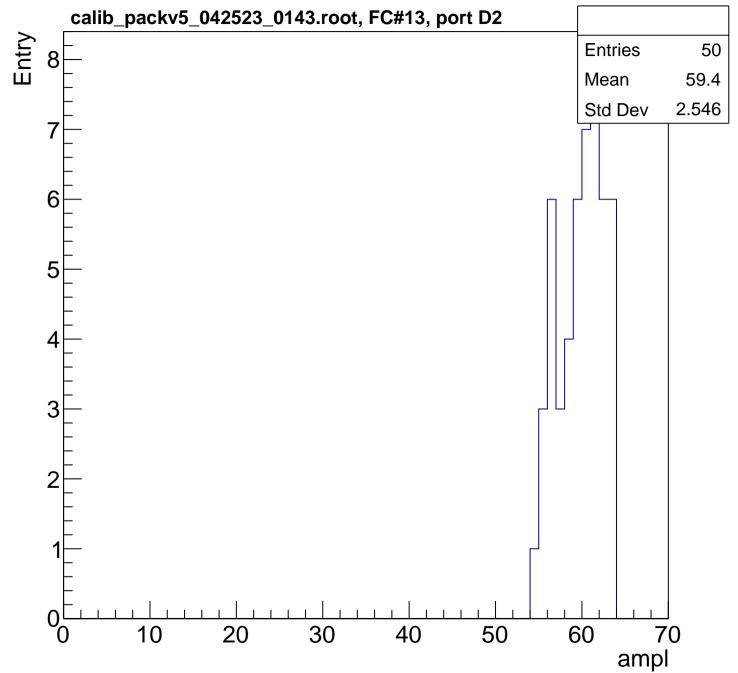


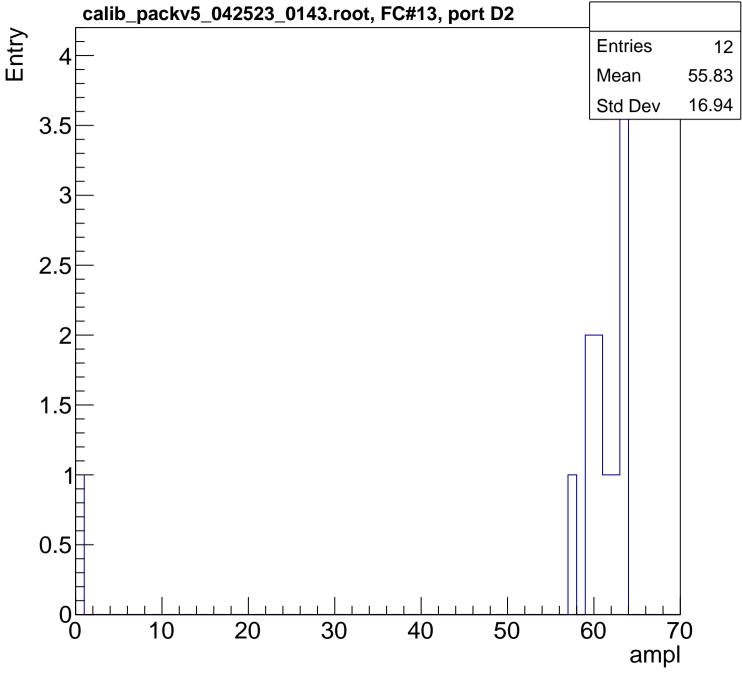




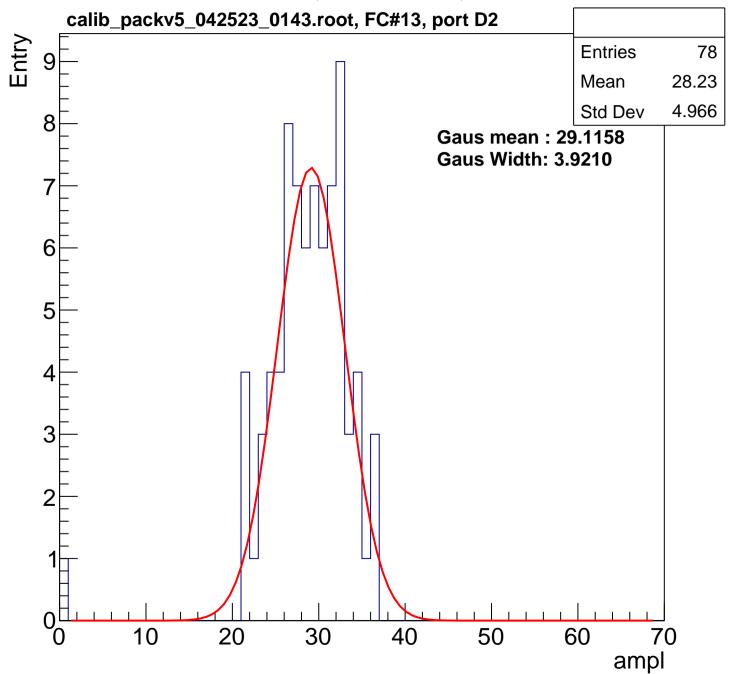


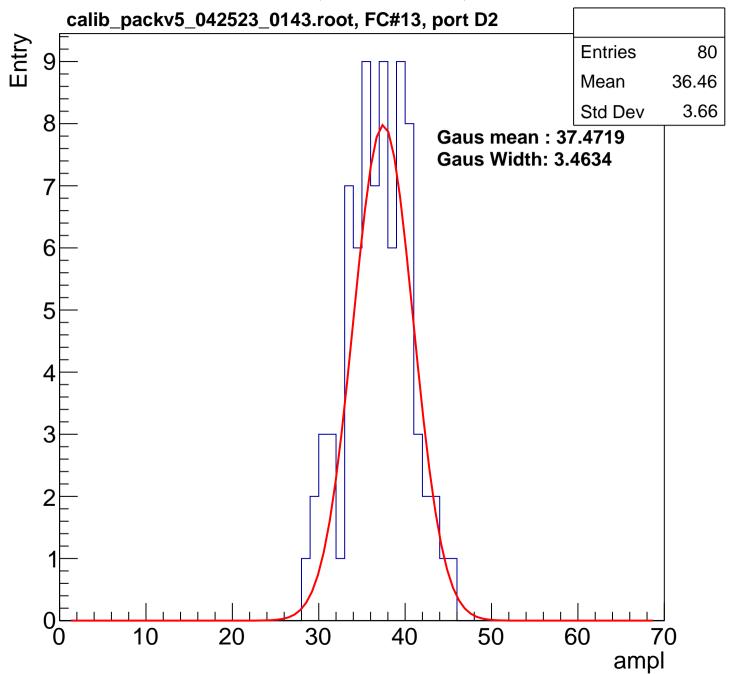


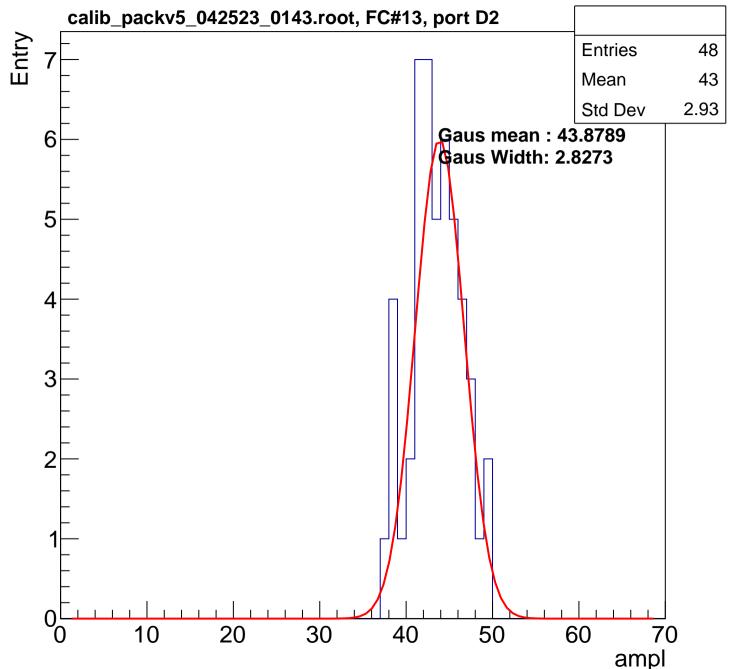


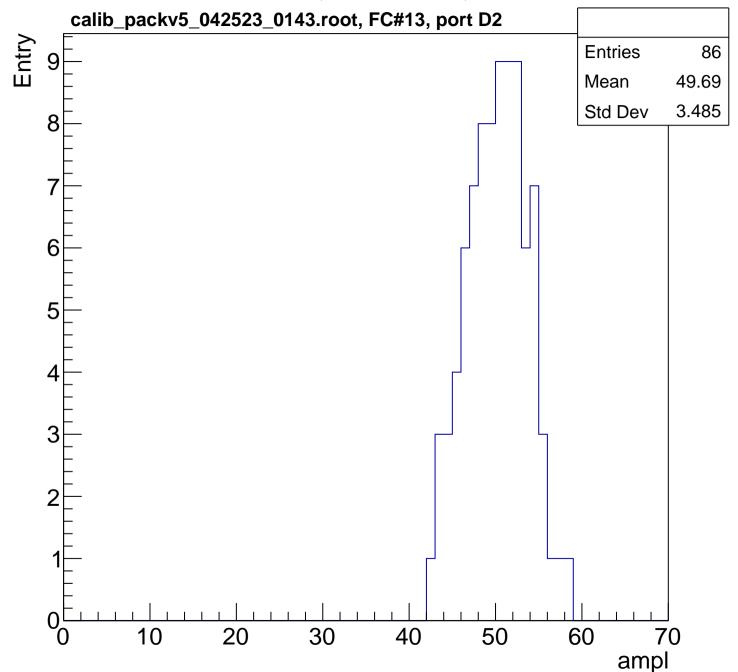


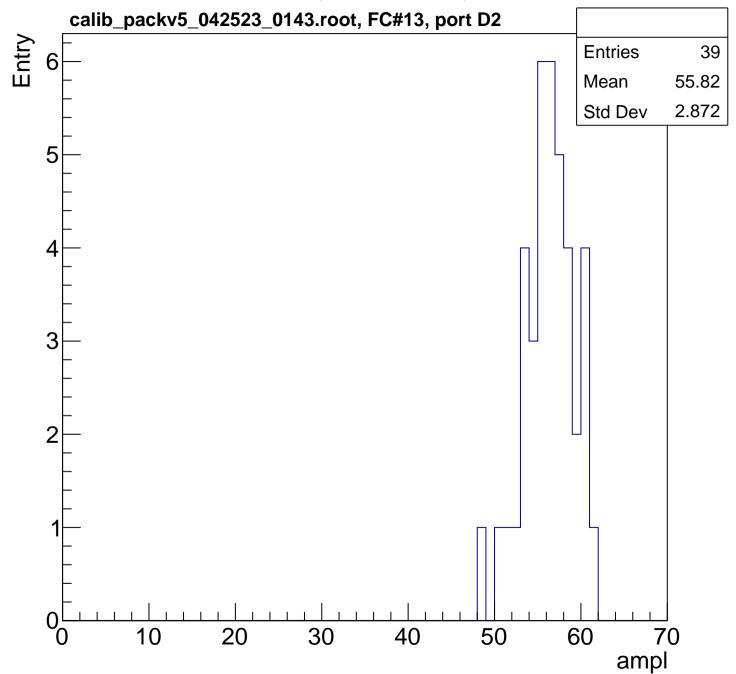
B1L003S, U4-ch27, adc7 calib_packv5_042523_0143.root, FC#13, port D2 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

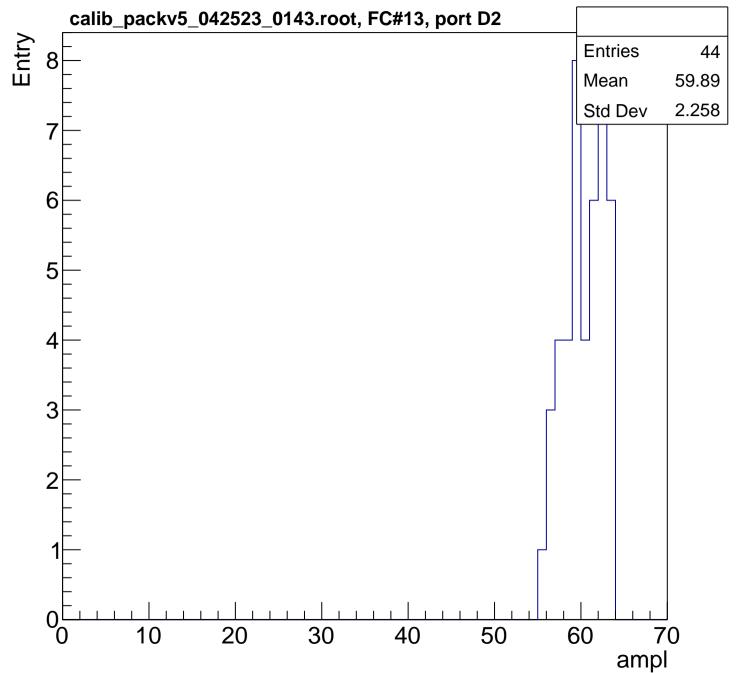


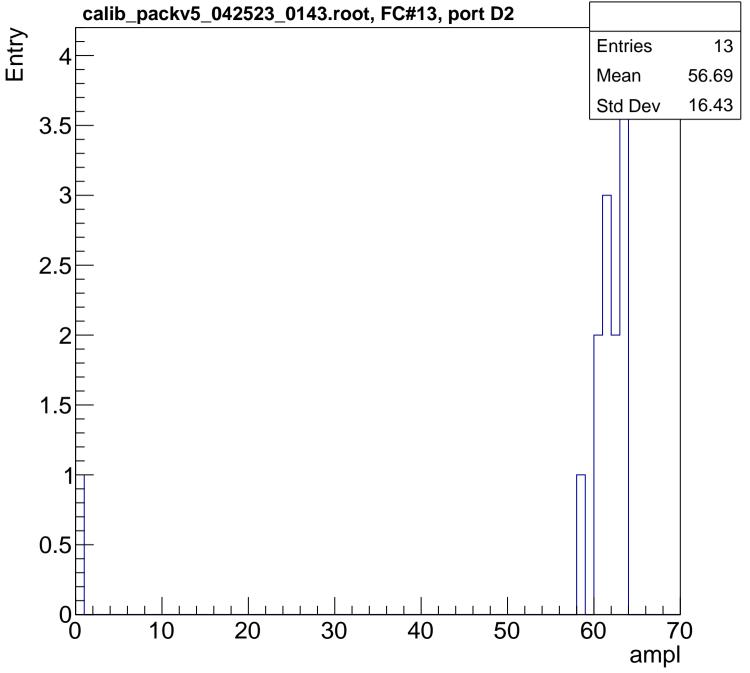






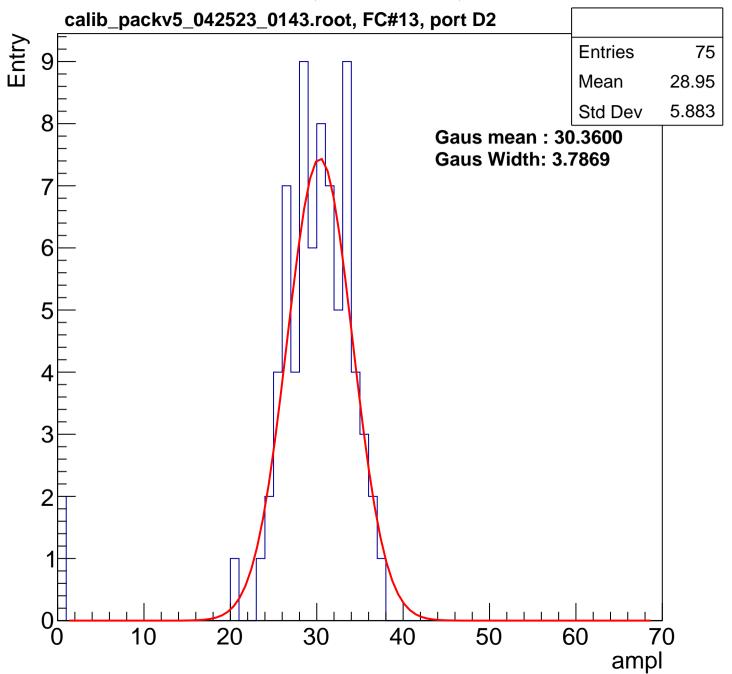


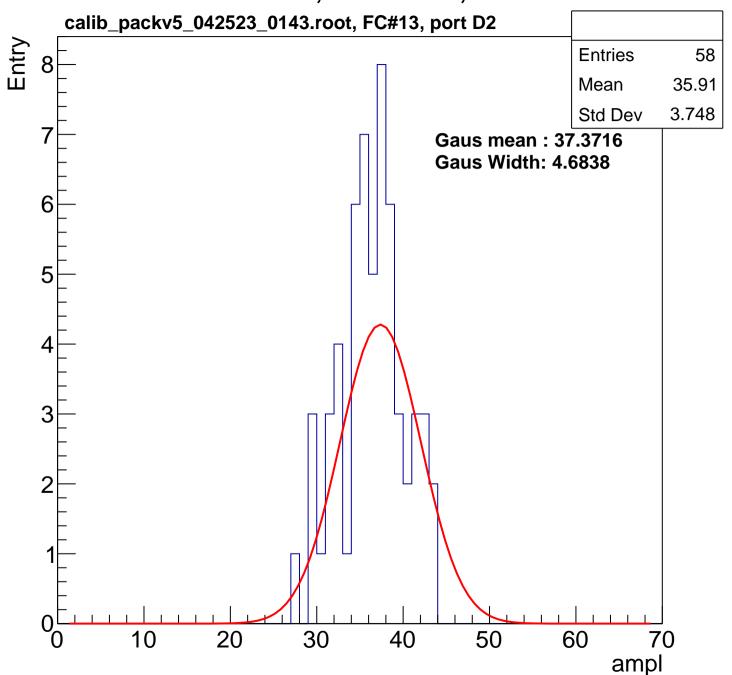


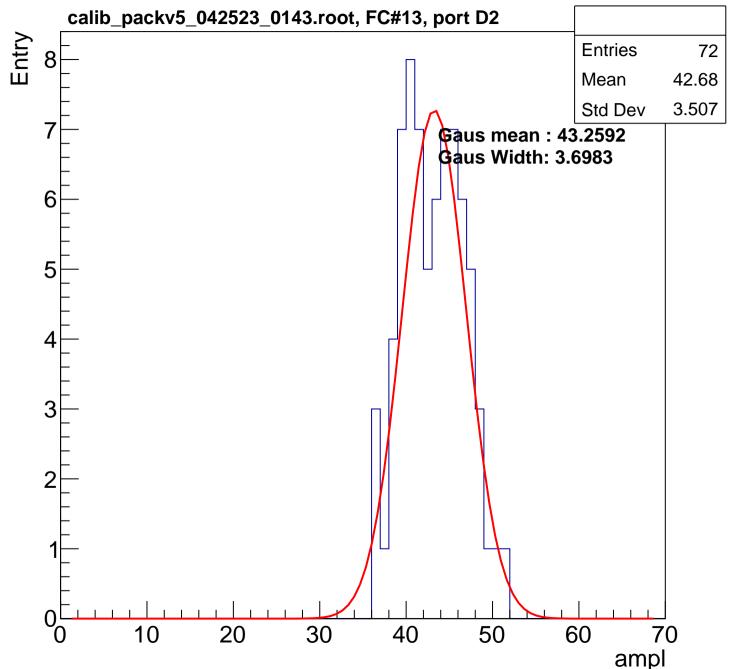


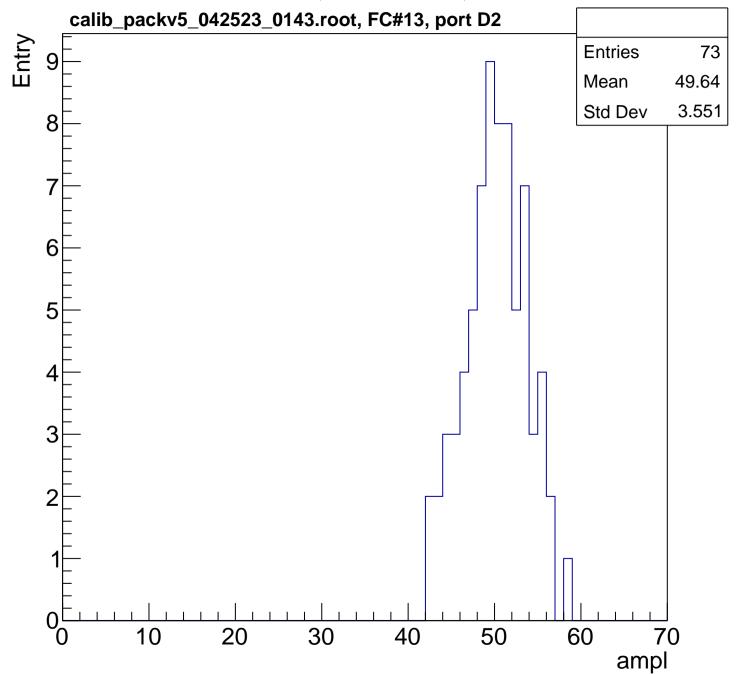
B1L003S, U4-ch28, adc7 calib_packv5_042523_0143.root, FC#13, port D2 Entry **Entries** Mean 19 Std Dev 0 8.0 0.6 0.4 0.2 10 20 30 40 50 60 70

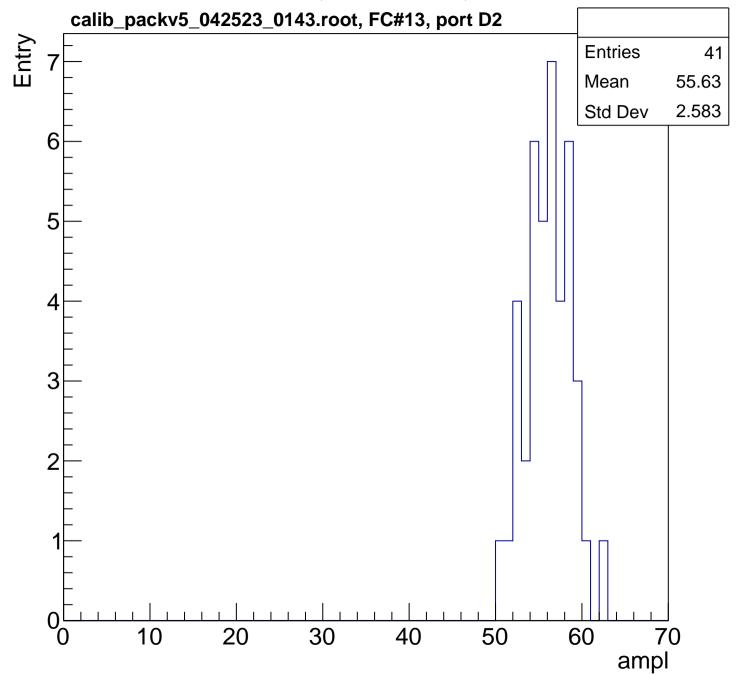
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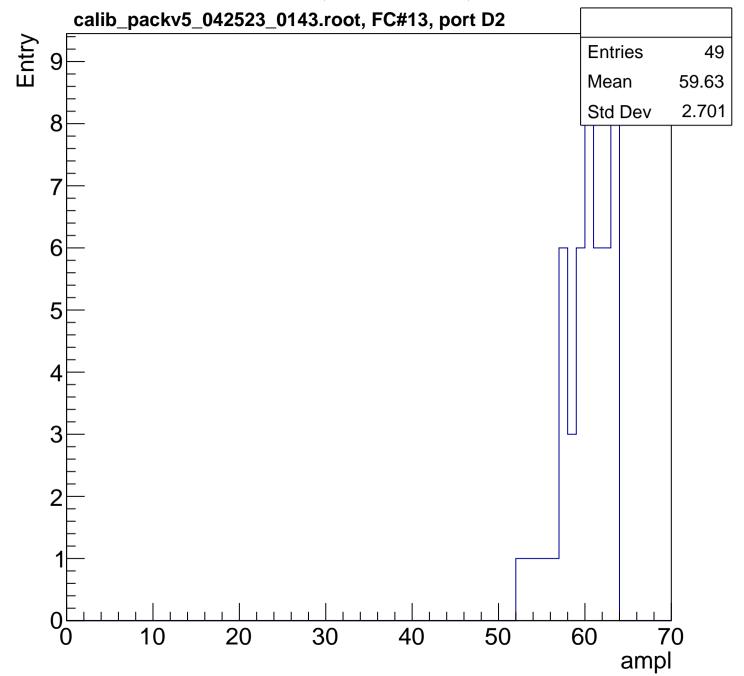


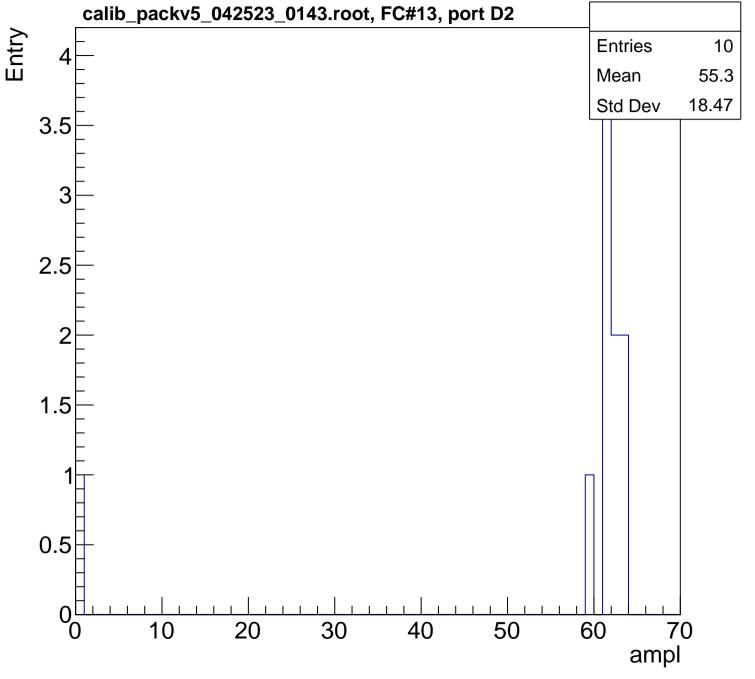


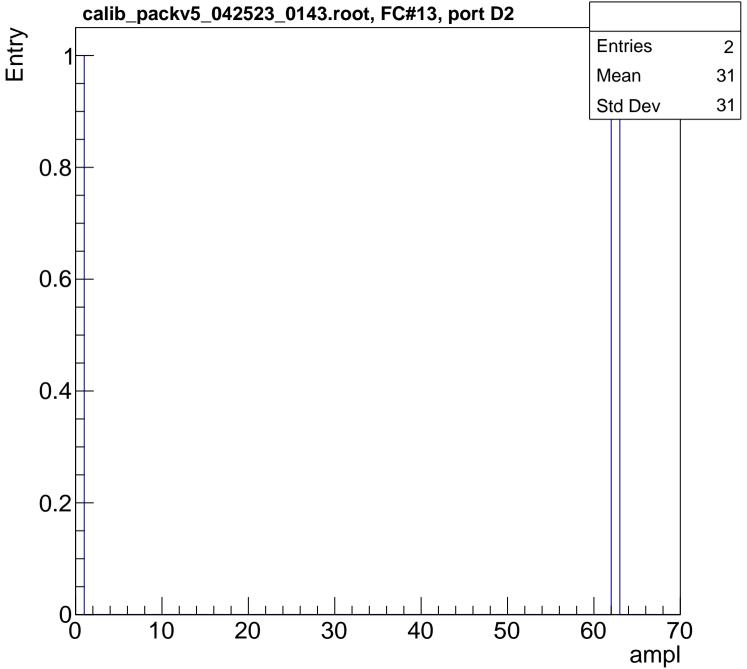


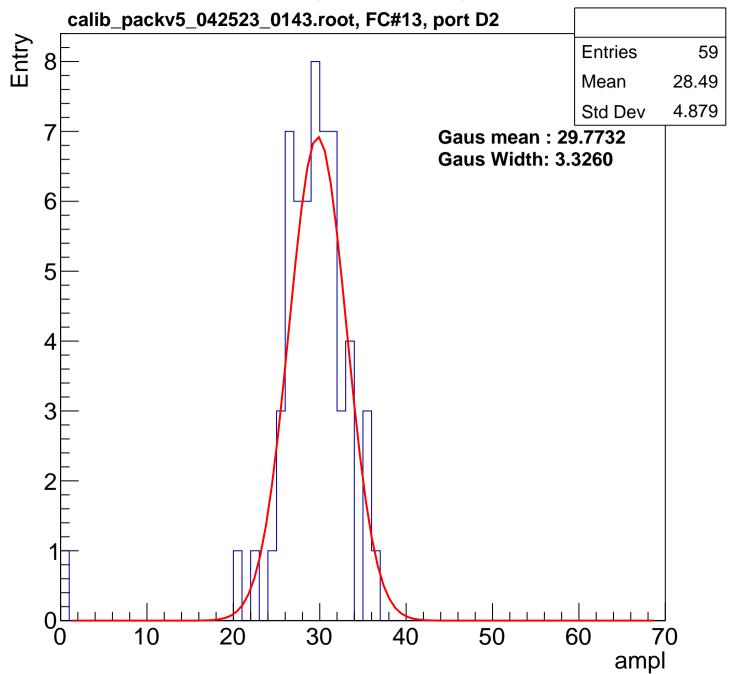


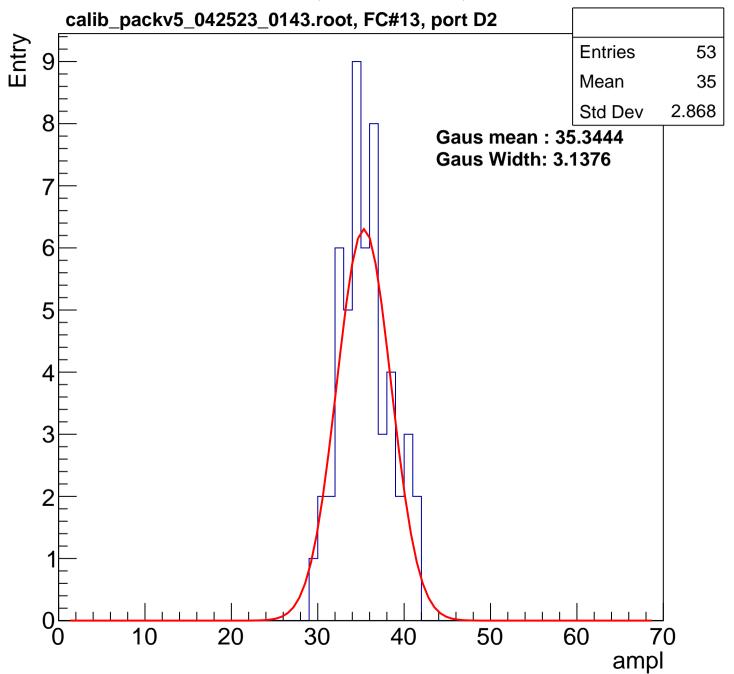


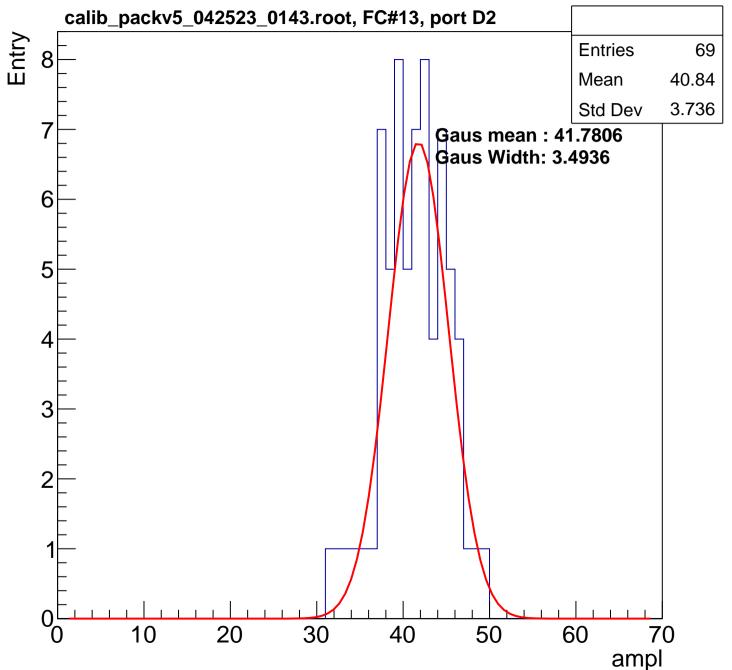


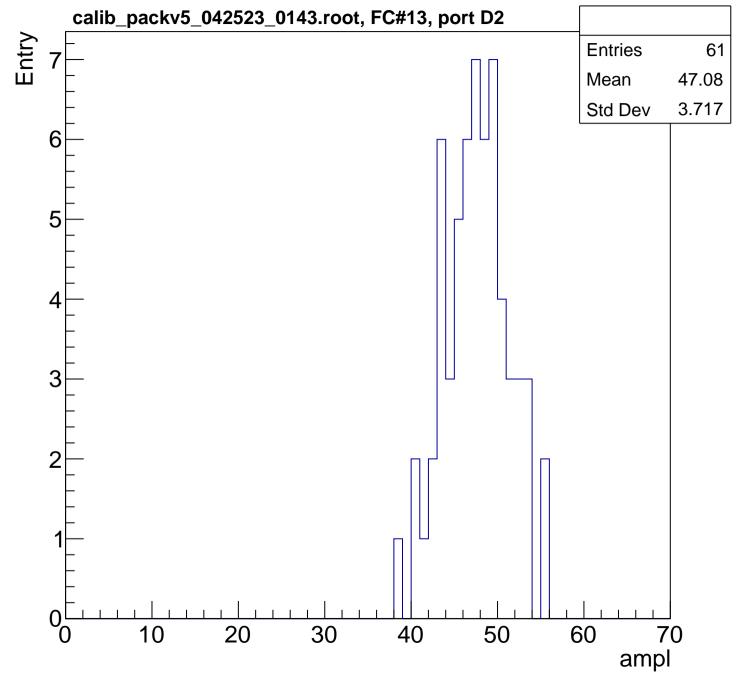


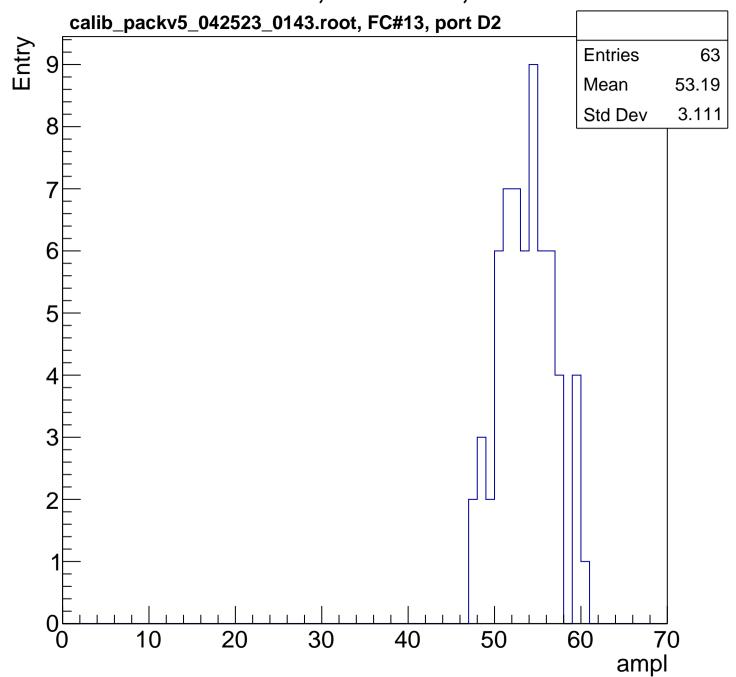


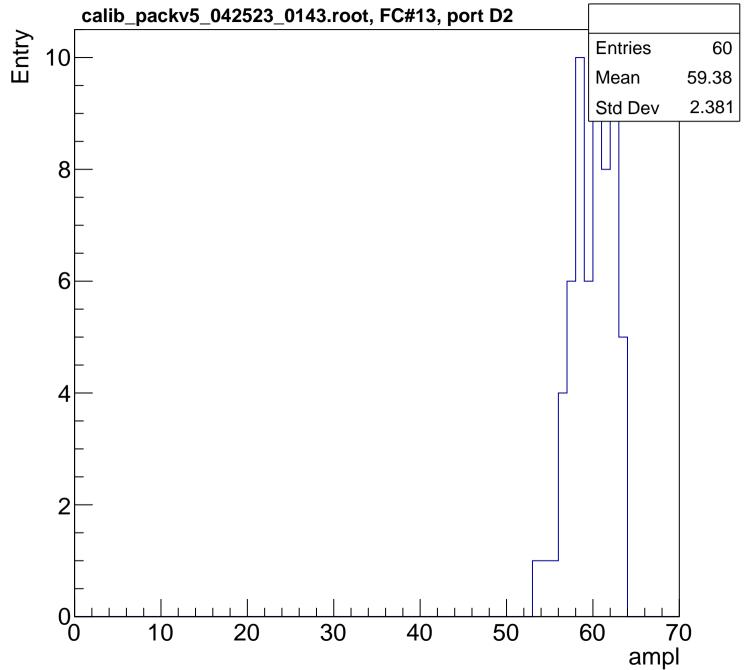


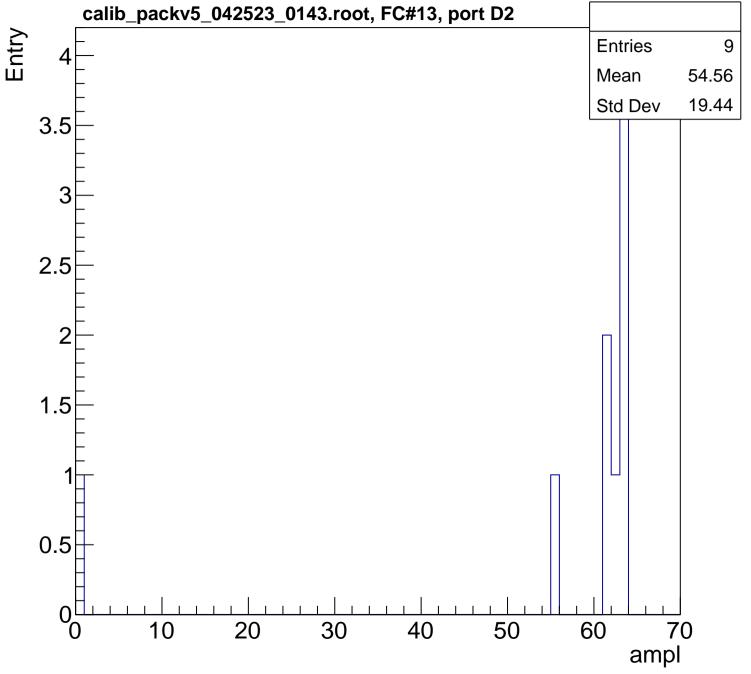


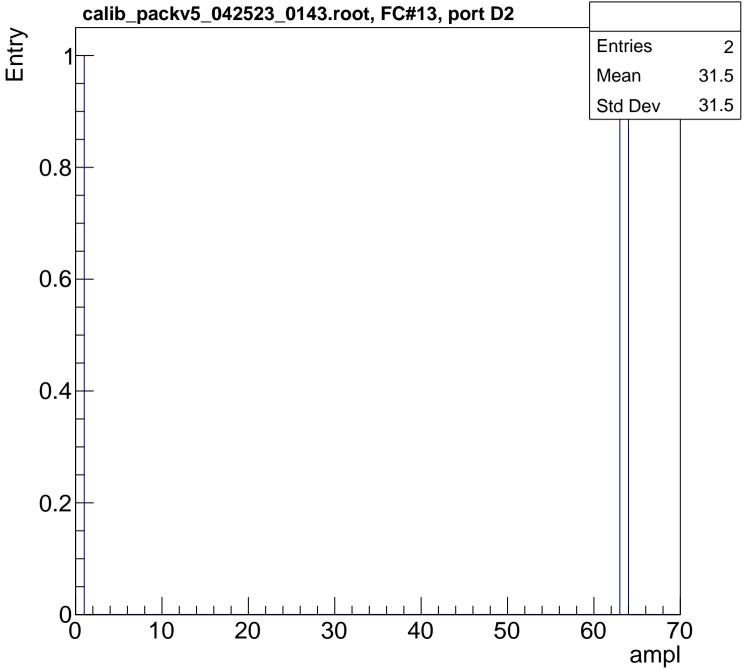


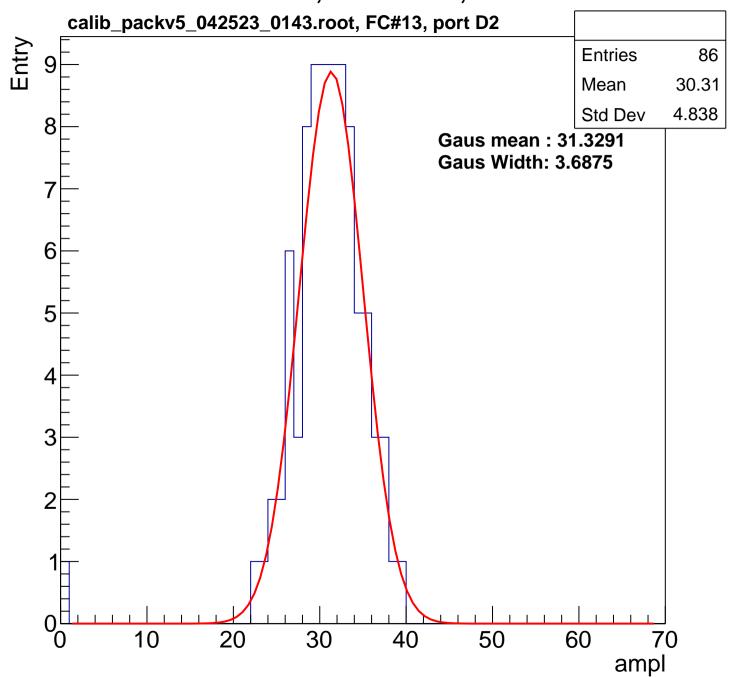


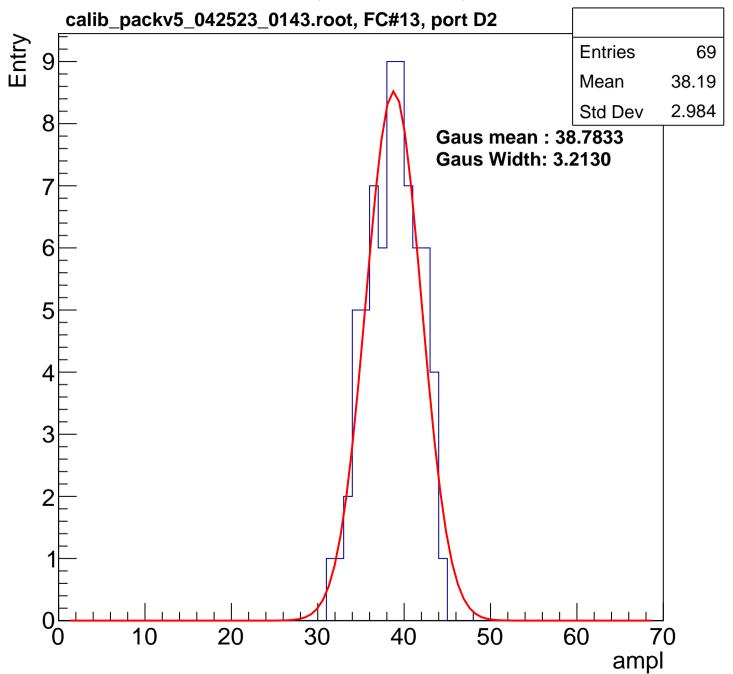


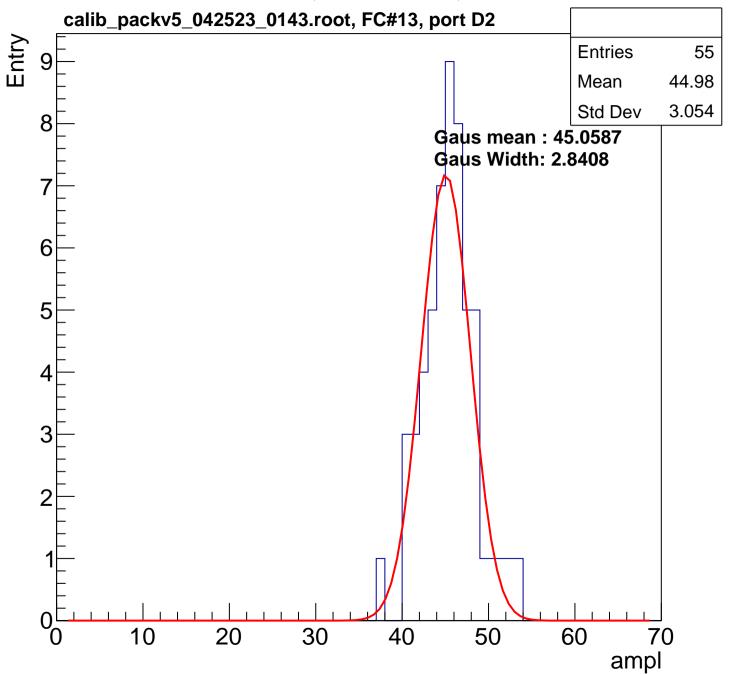


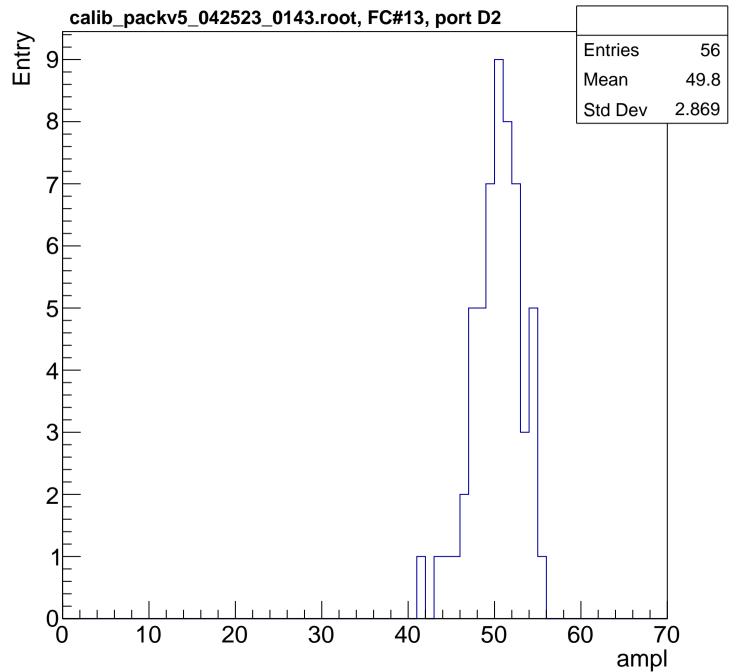


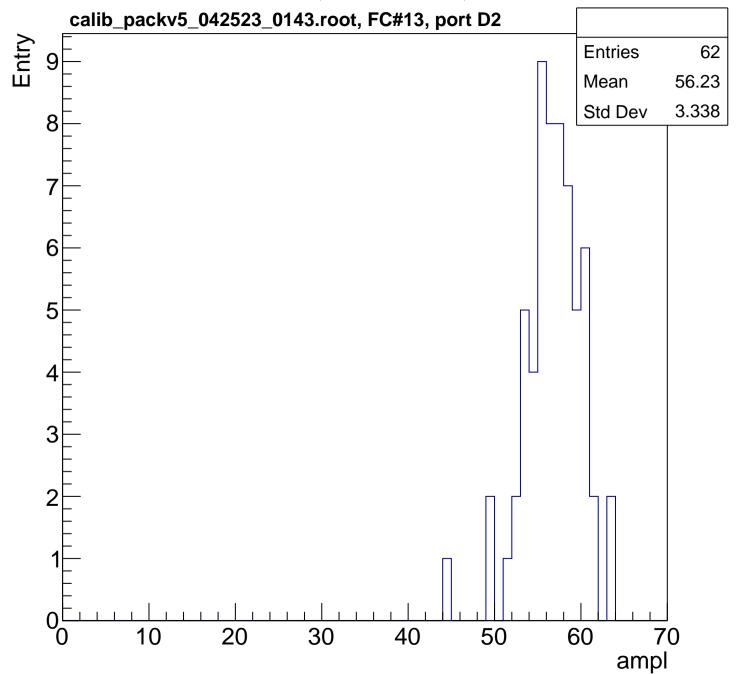


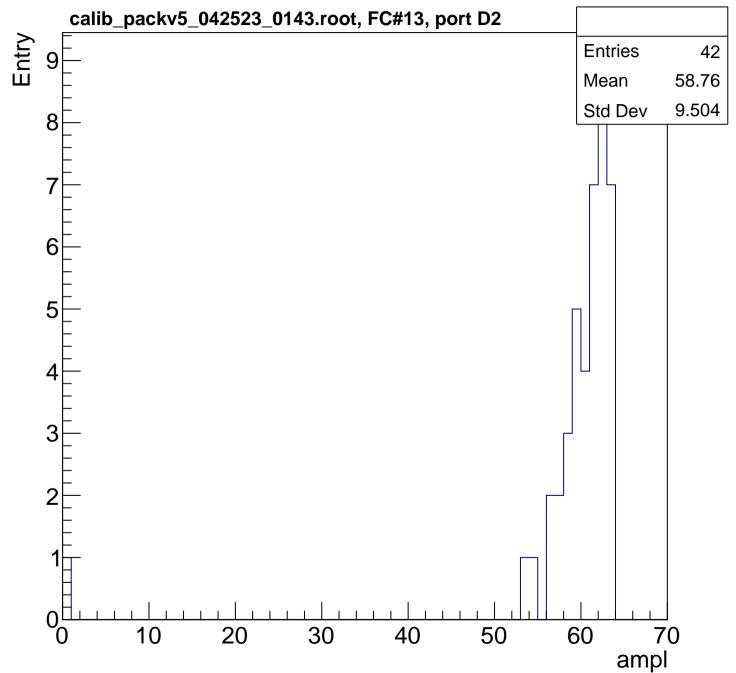


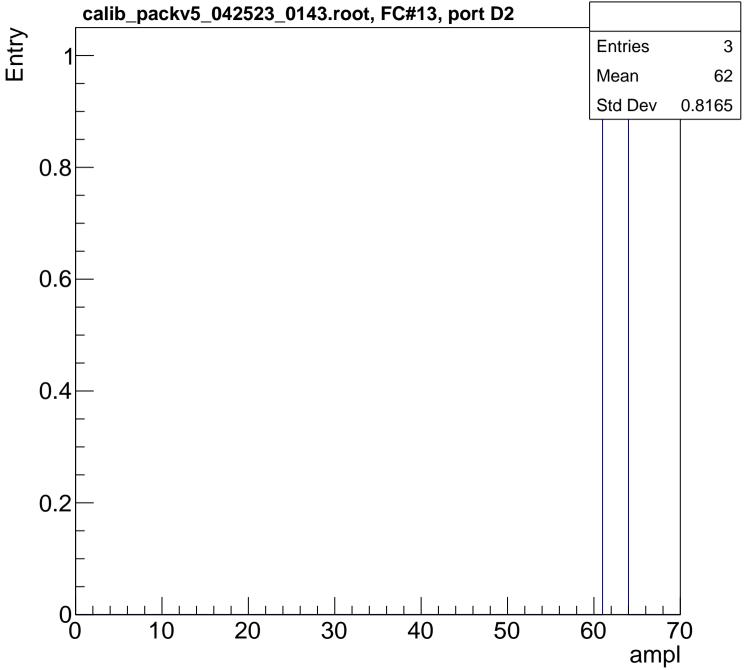




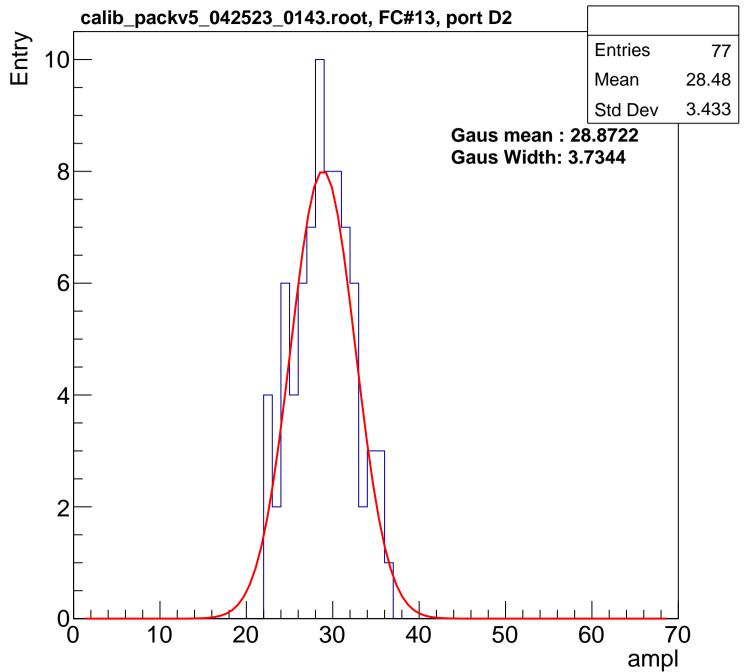


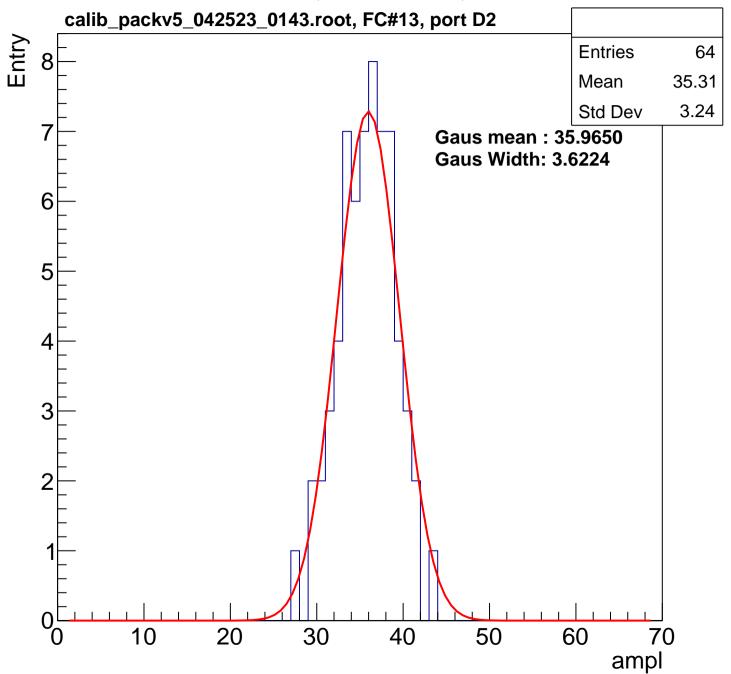


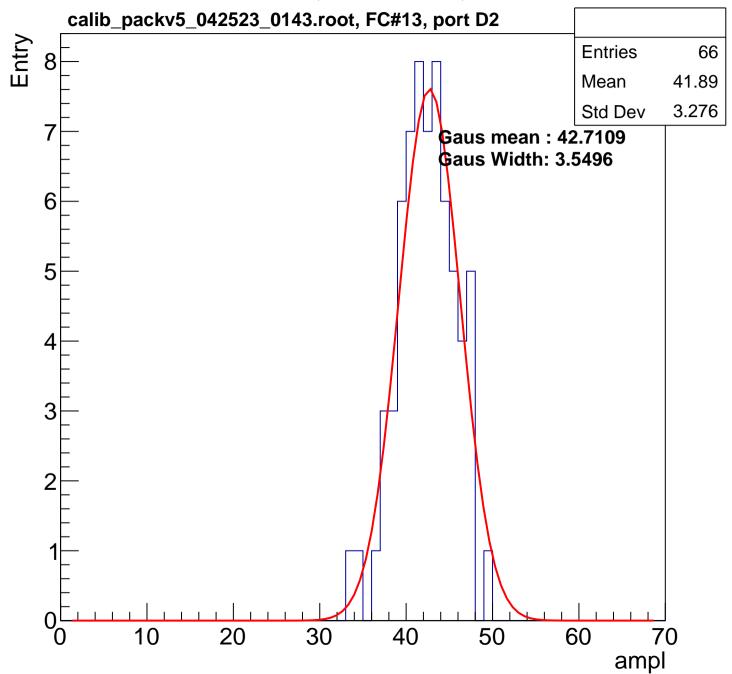


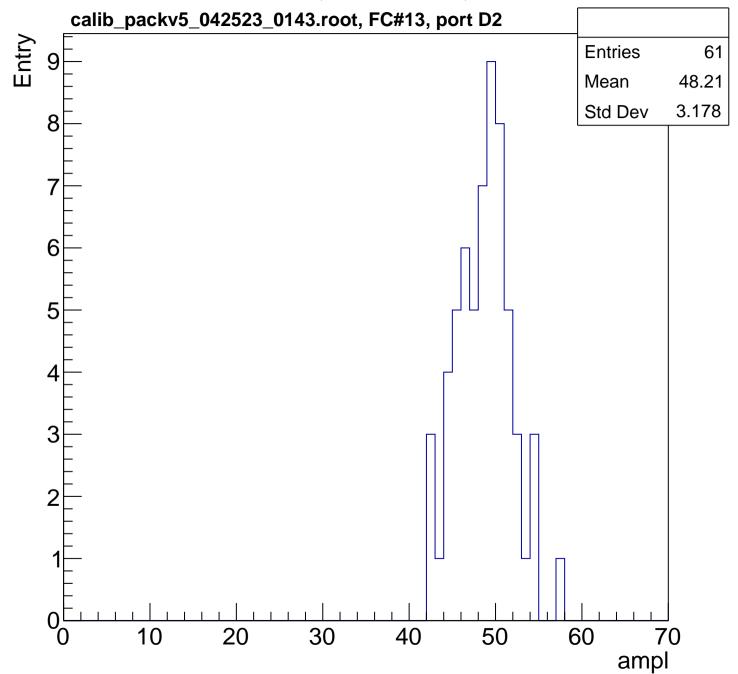


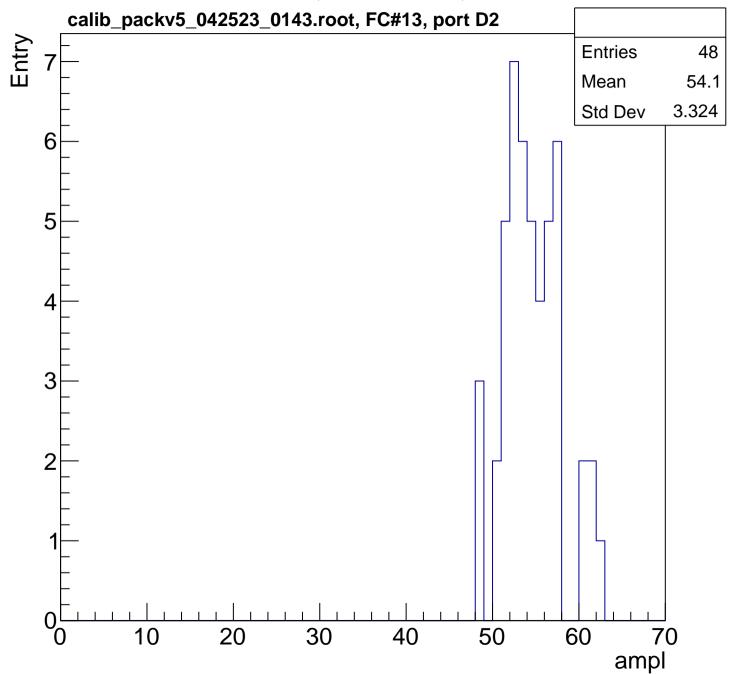
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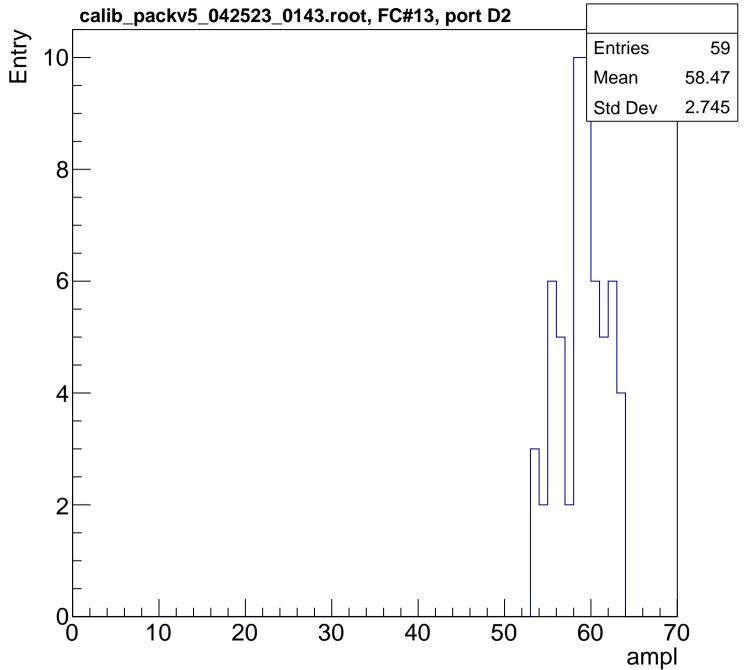


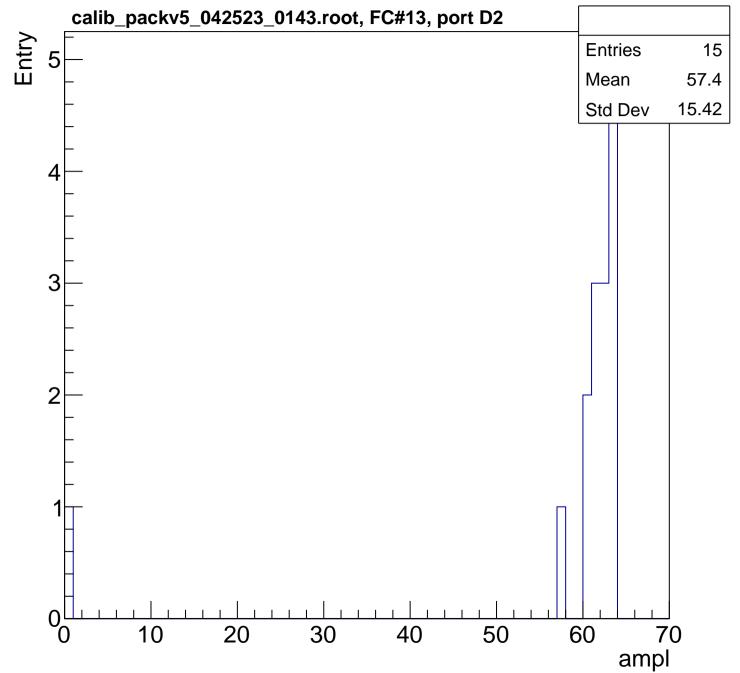


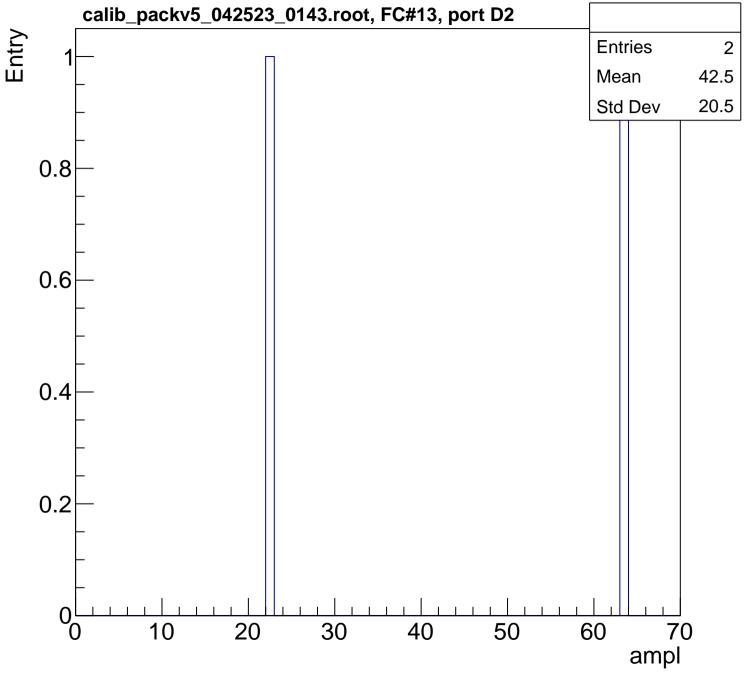


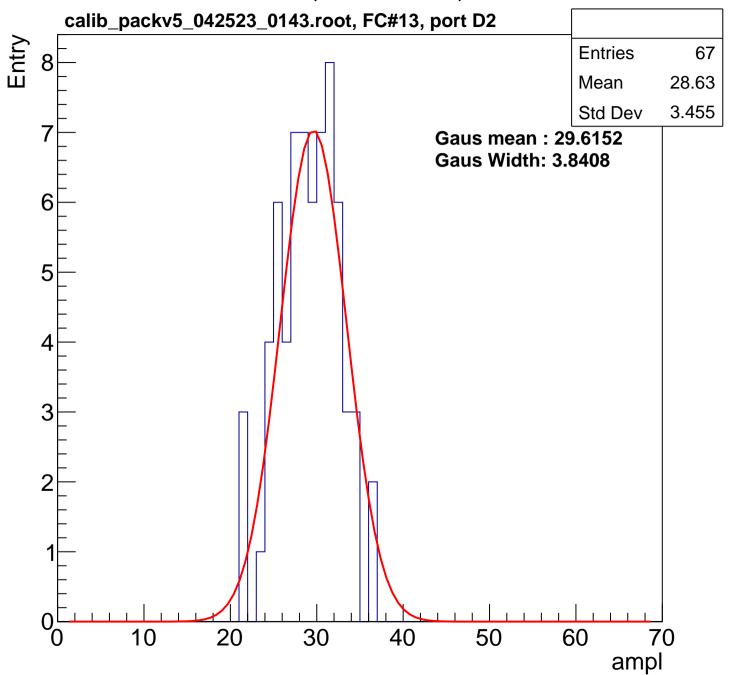


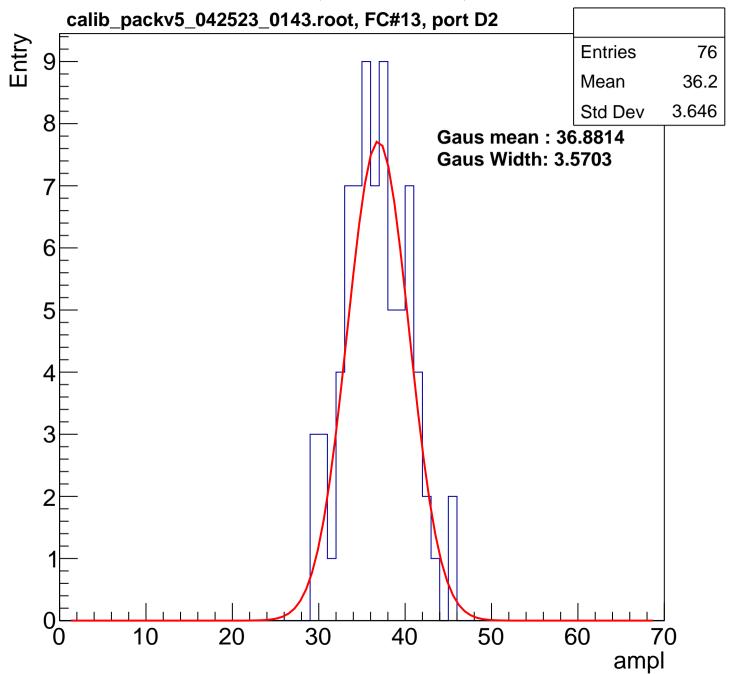


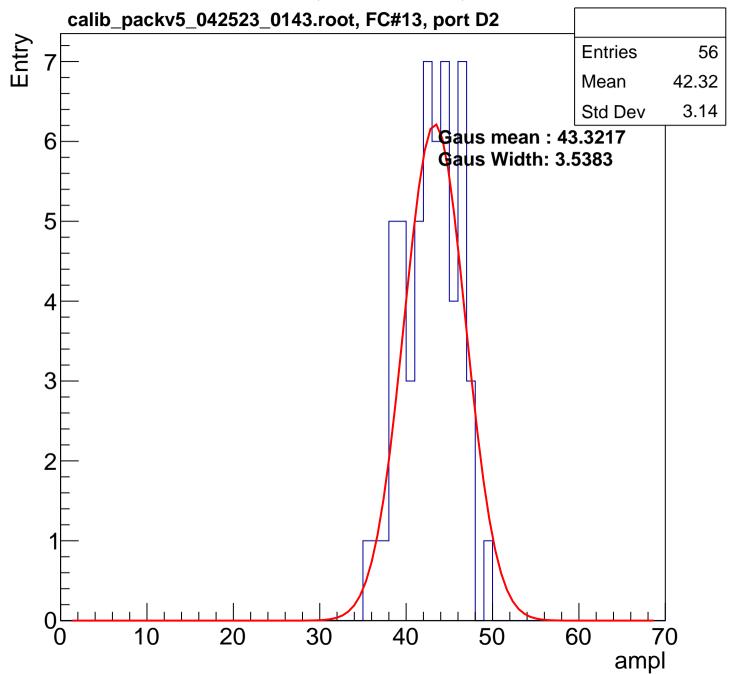


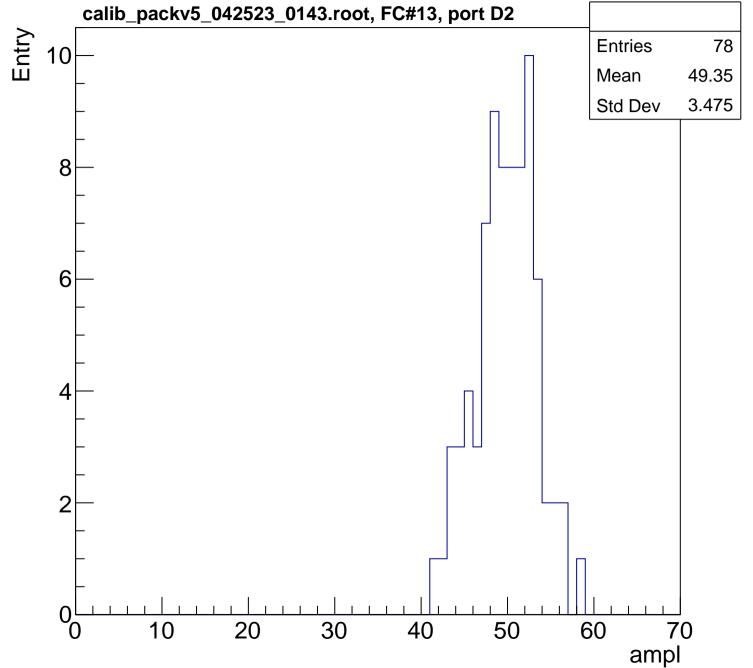


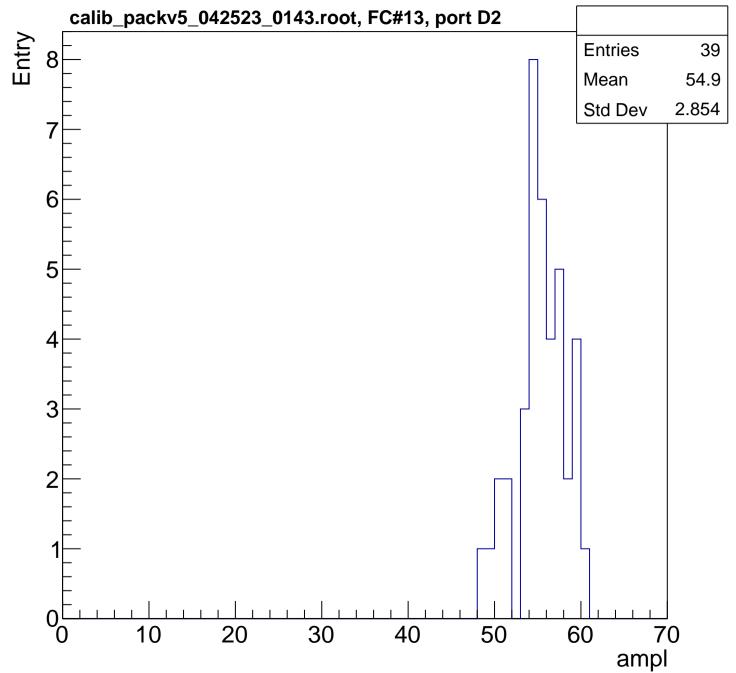


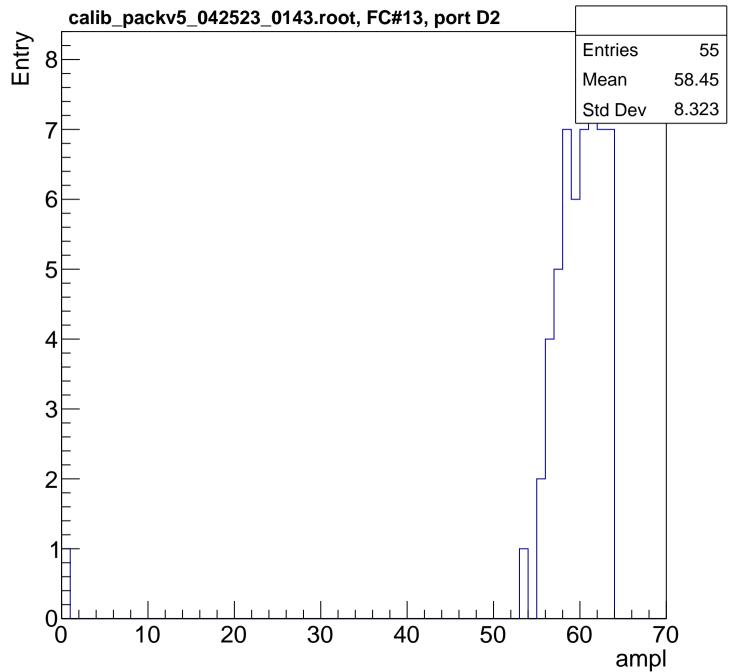


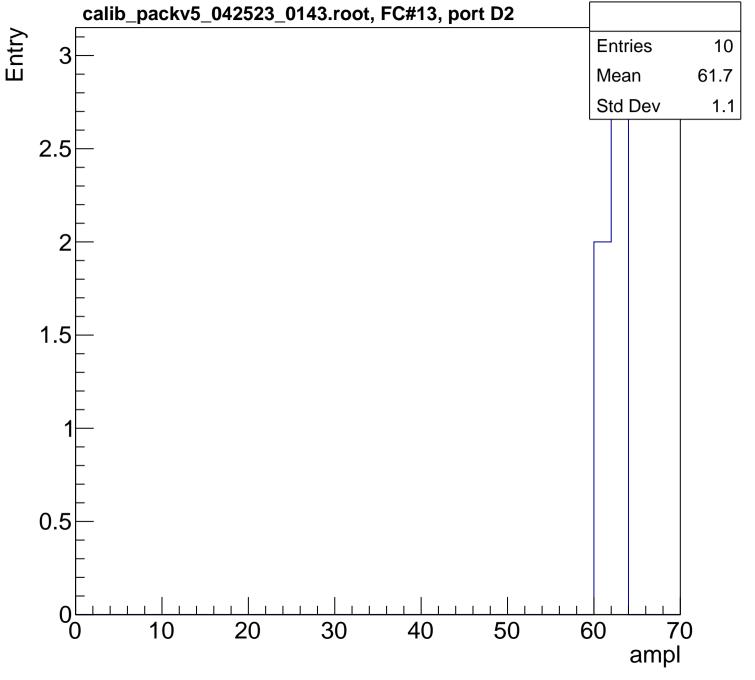




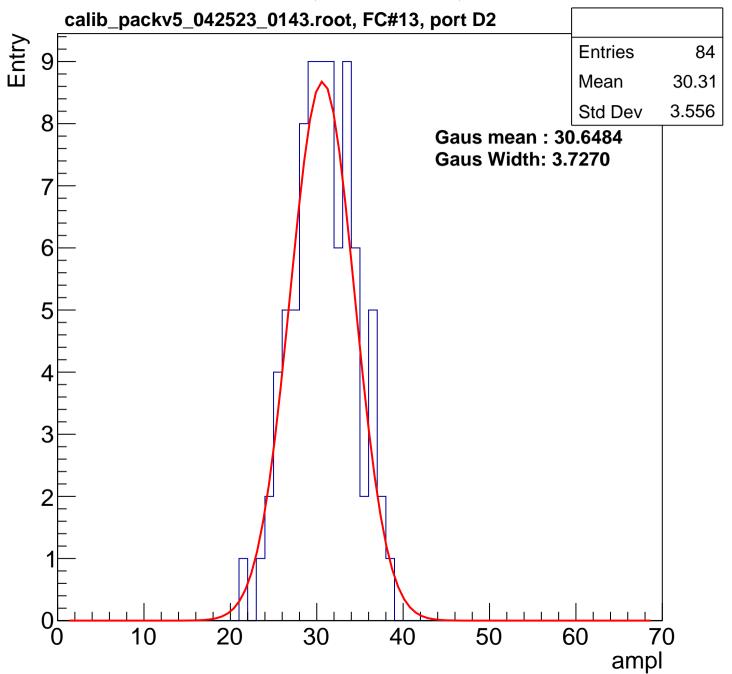


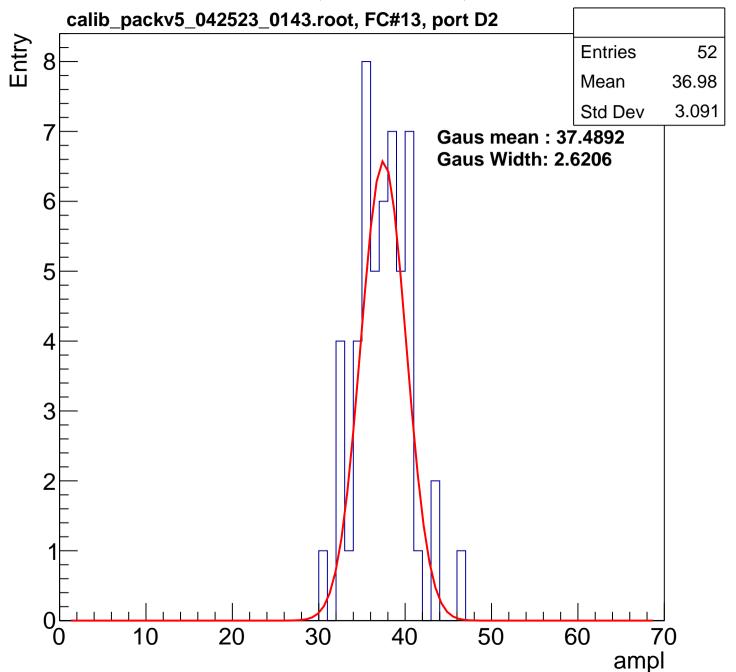


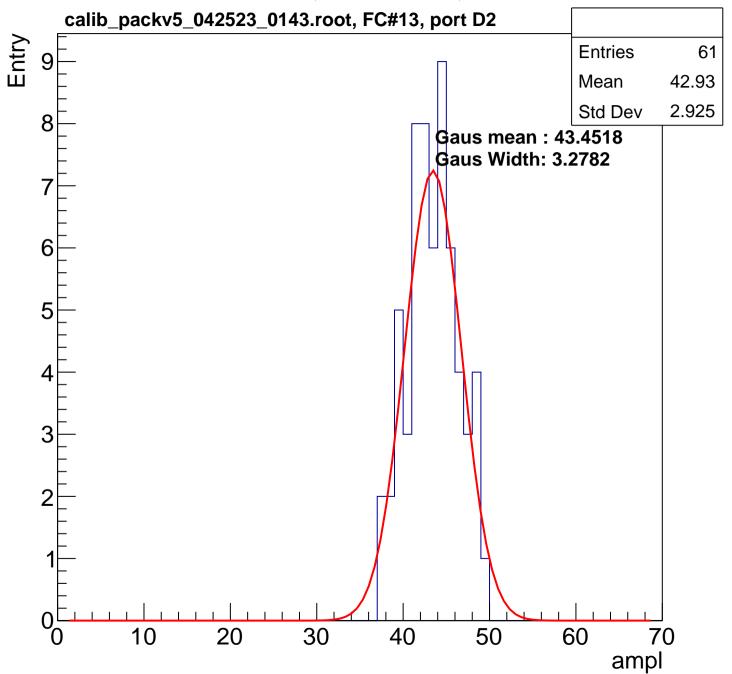


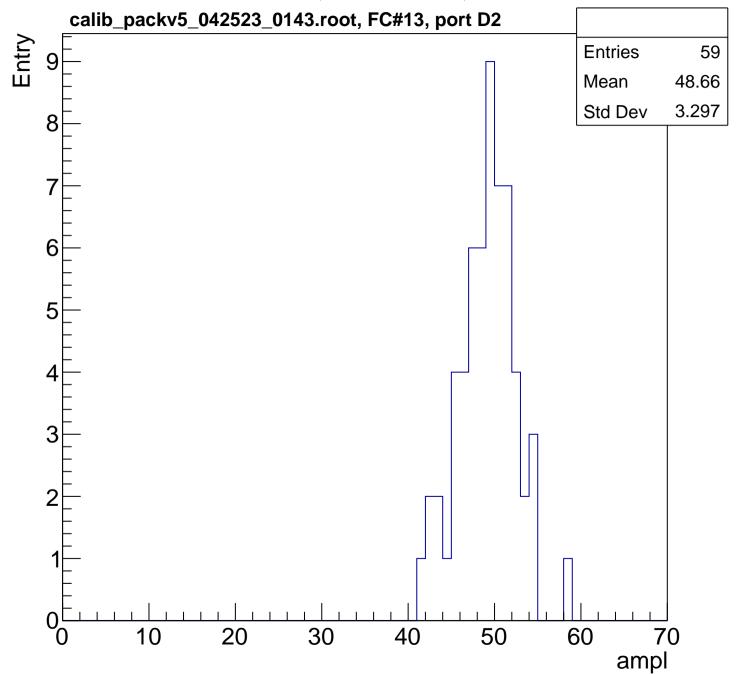


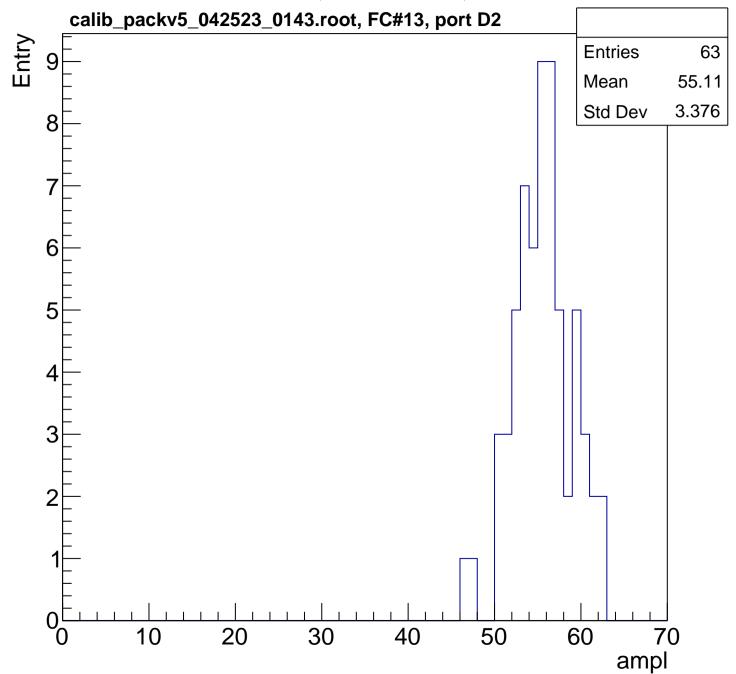
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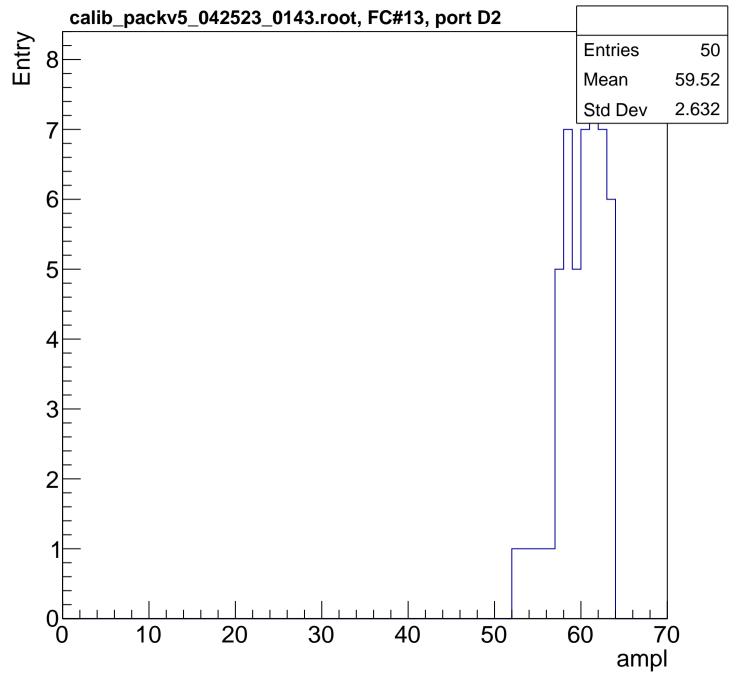


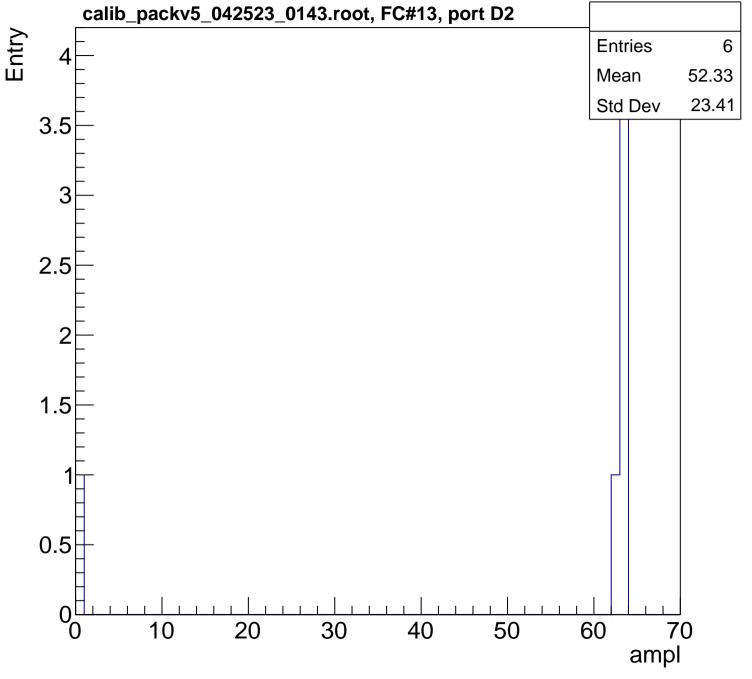




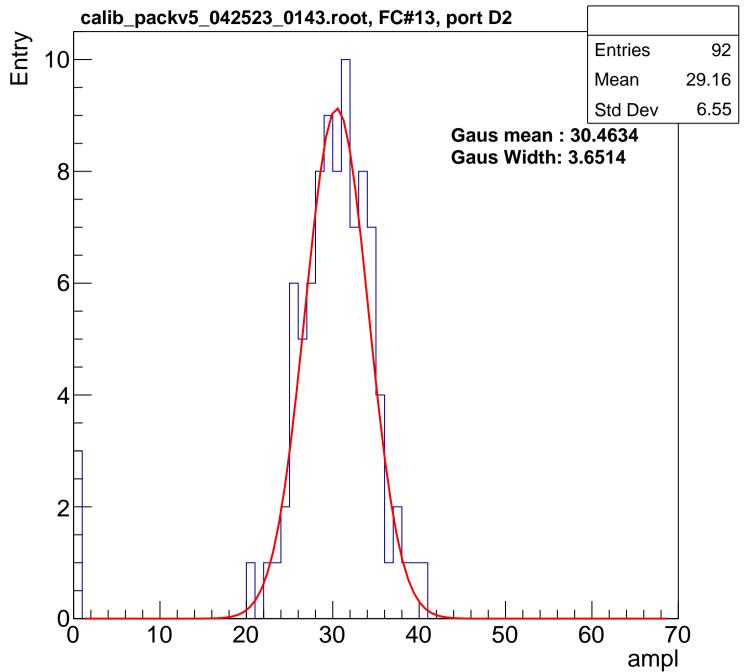


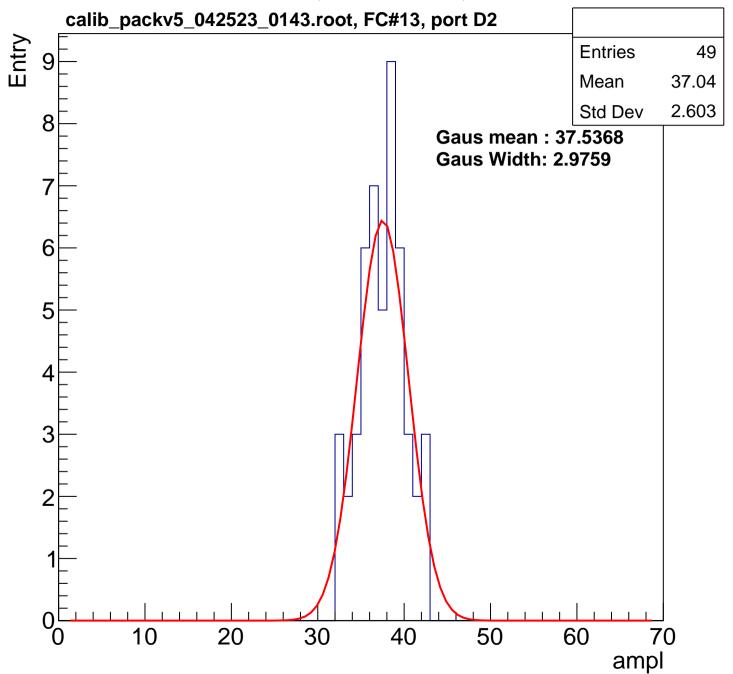


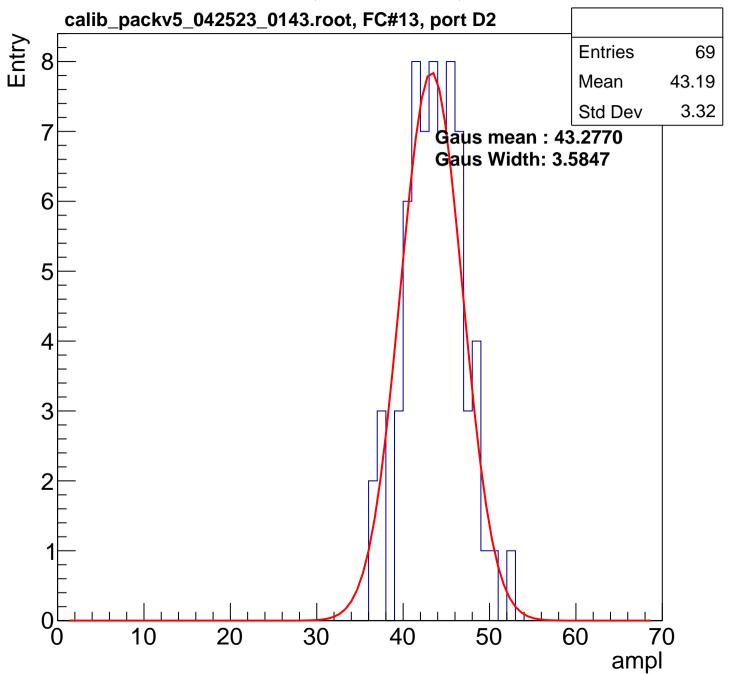


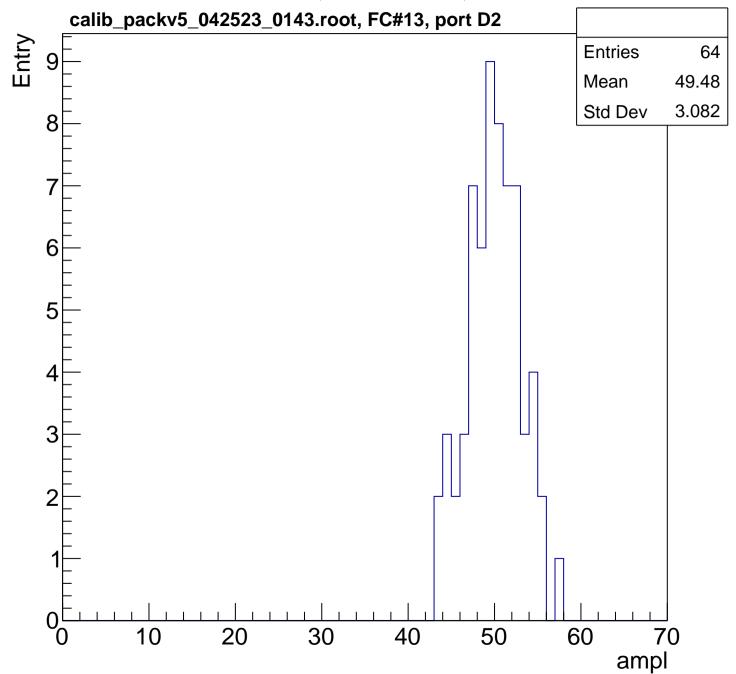


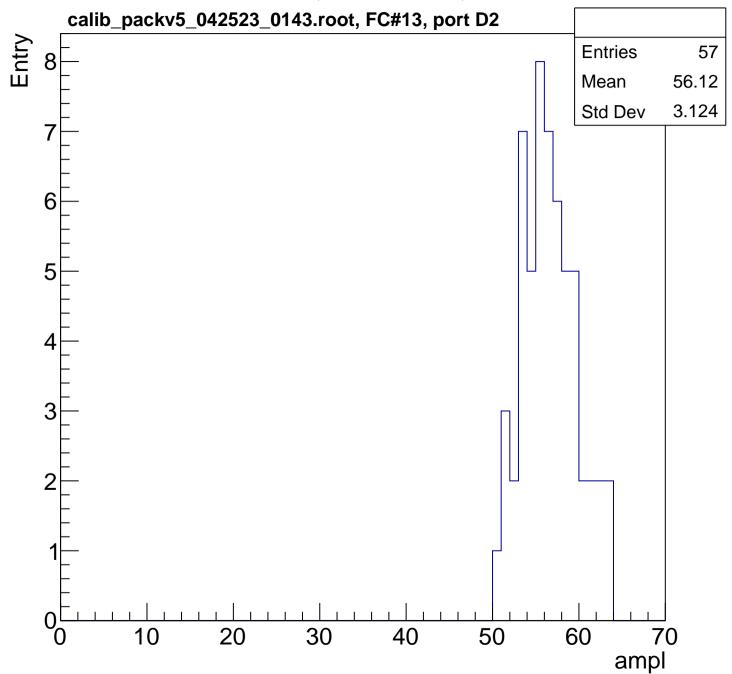
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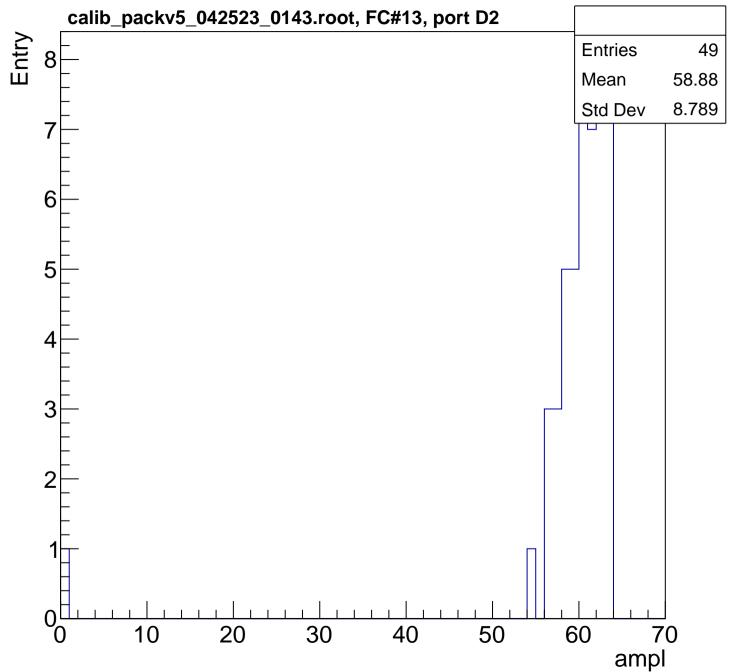


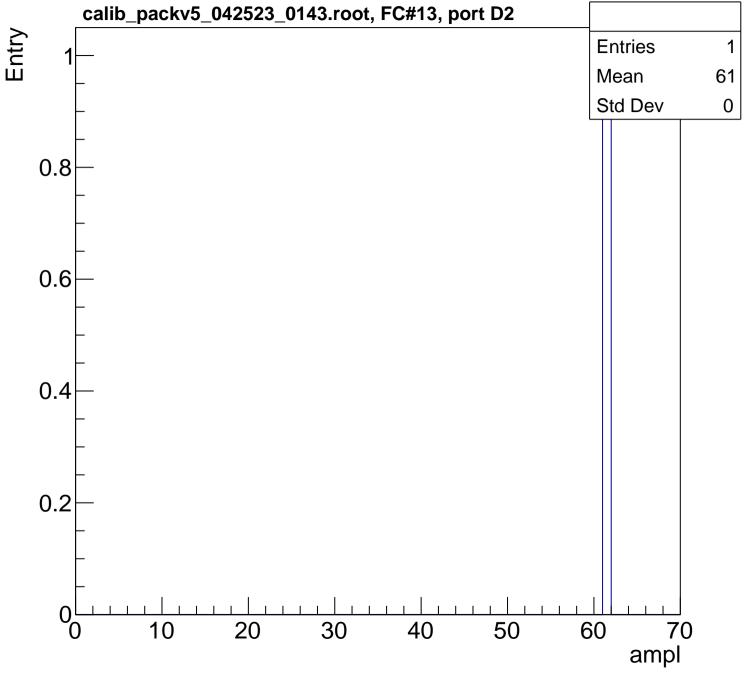




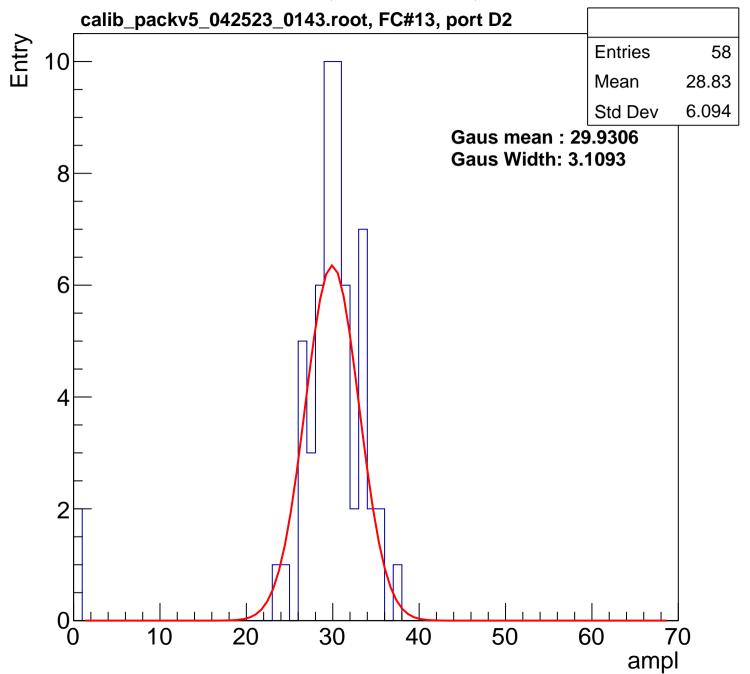


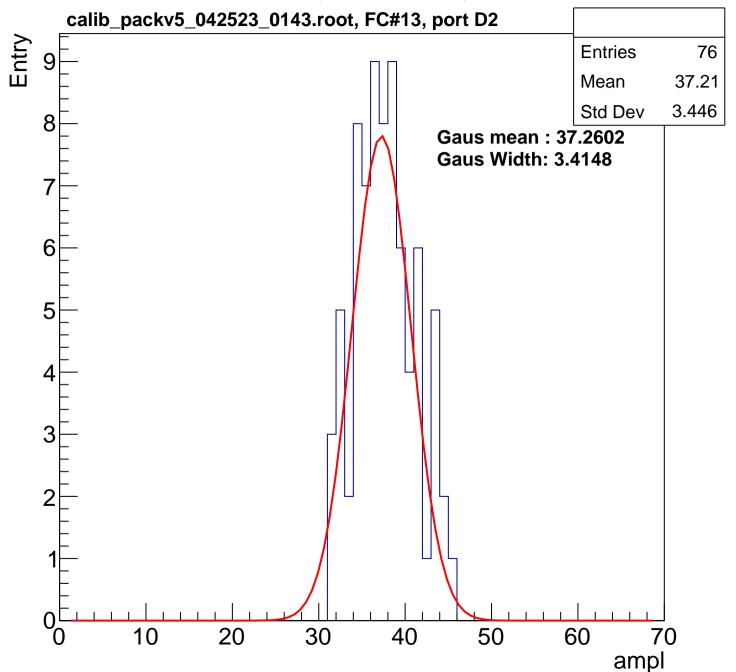


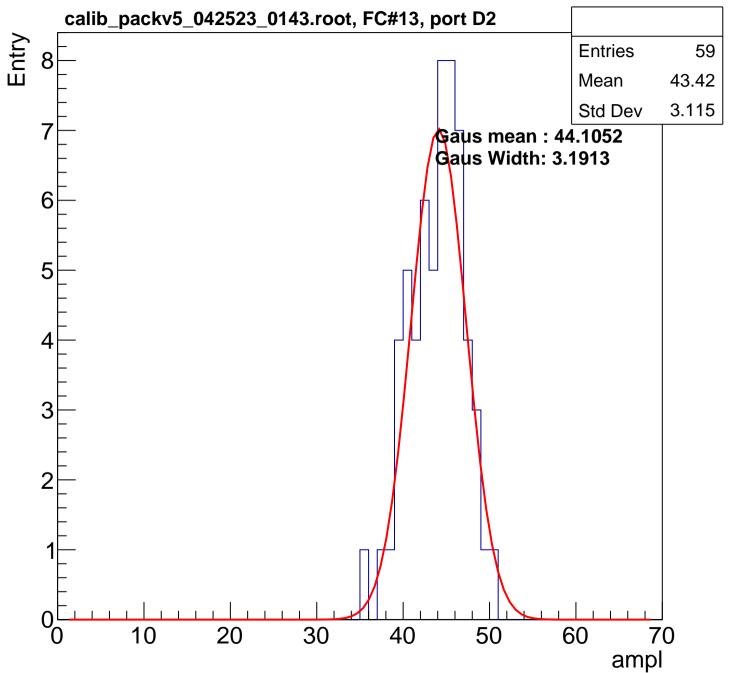


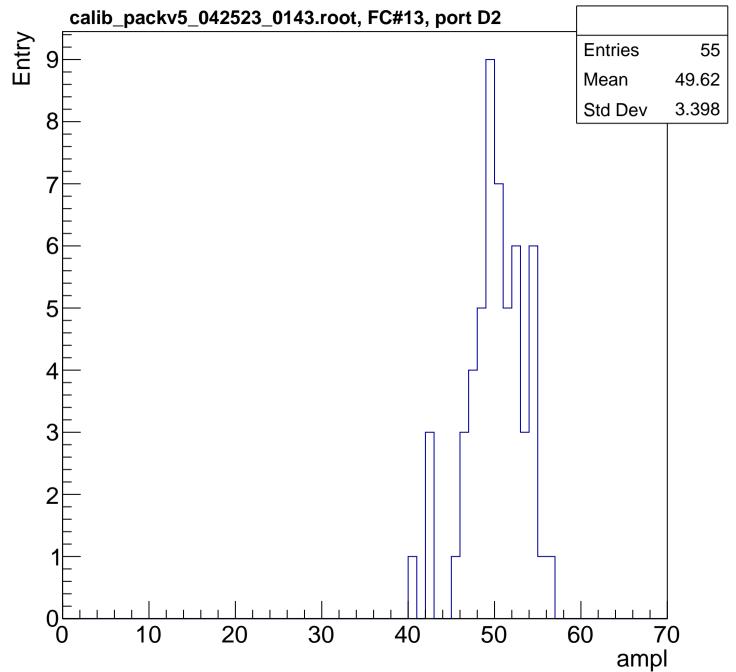


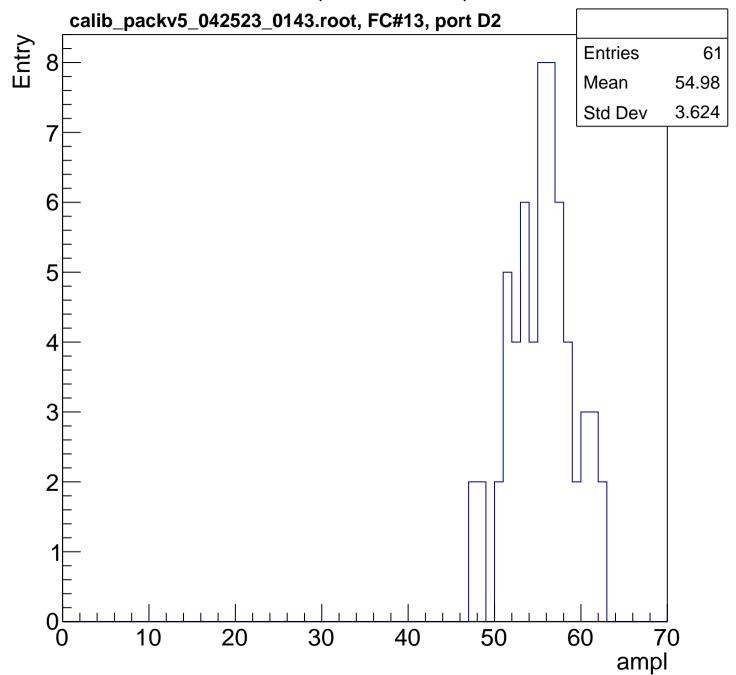


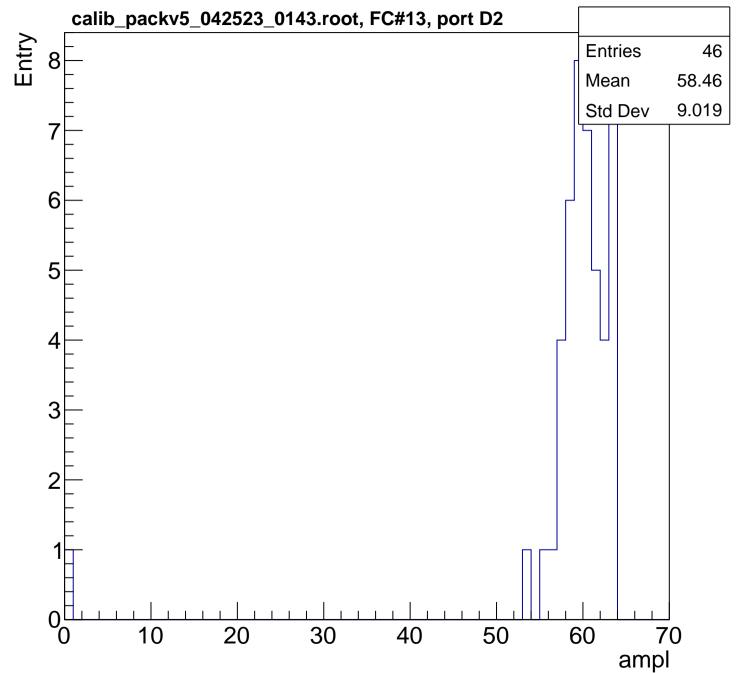


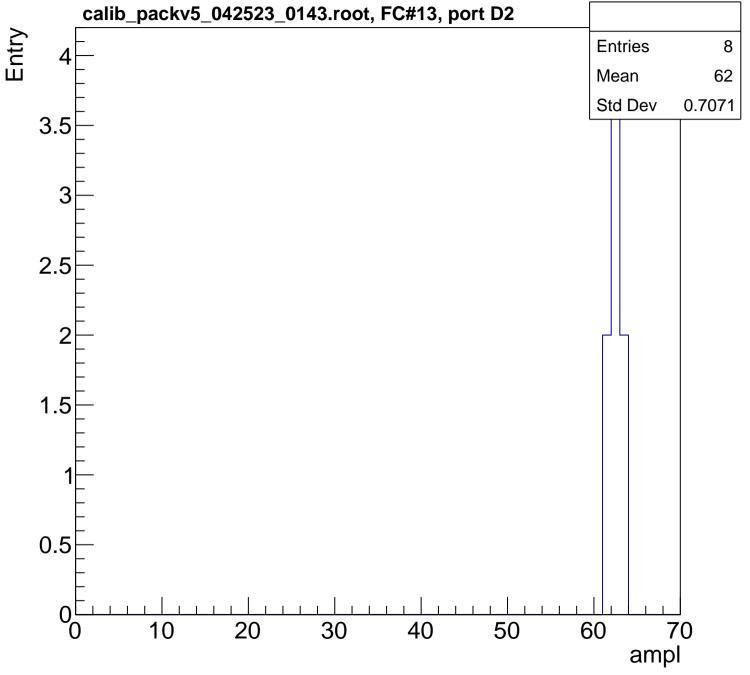


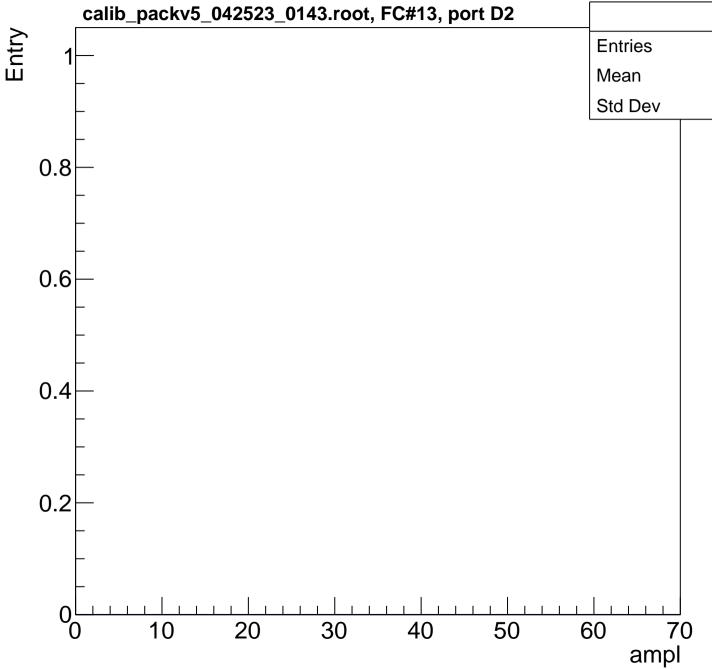


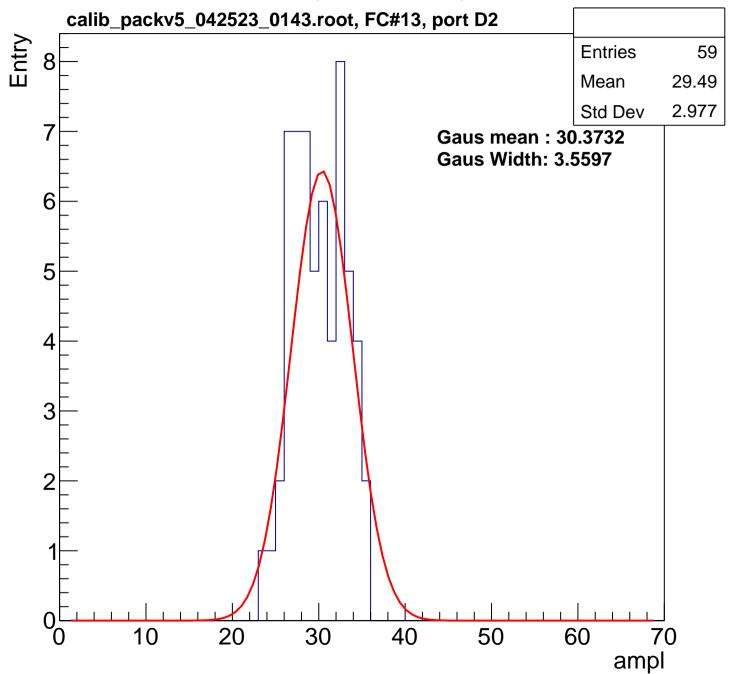


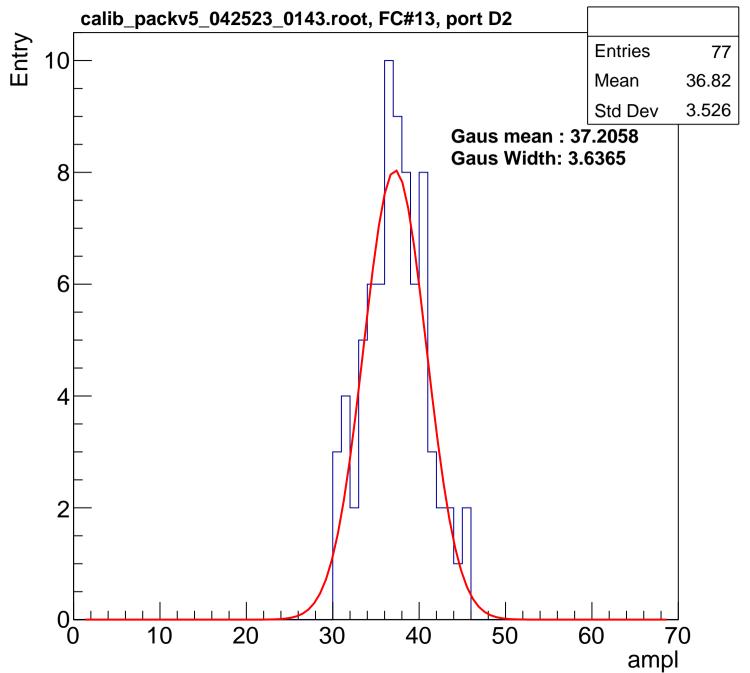


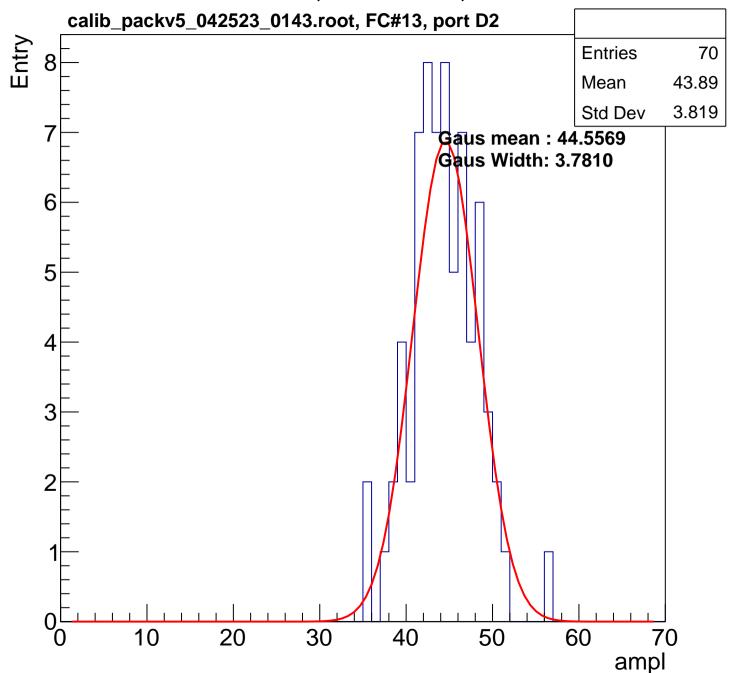


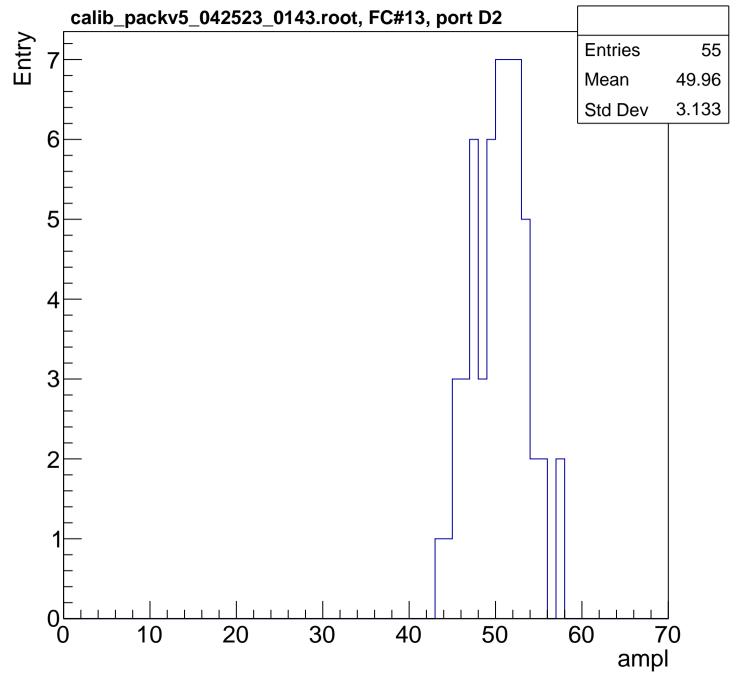


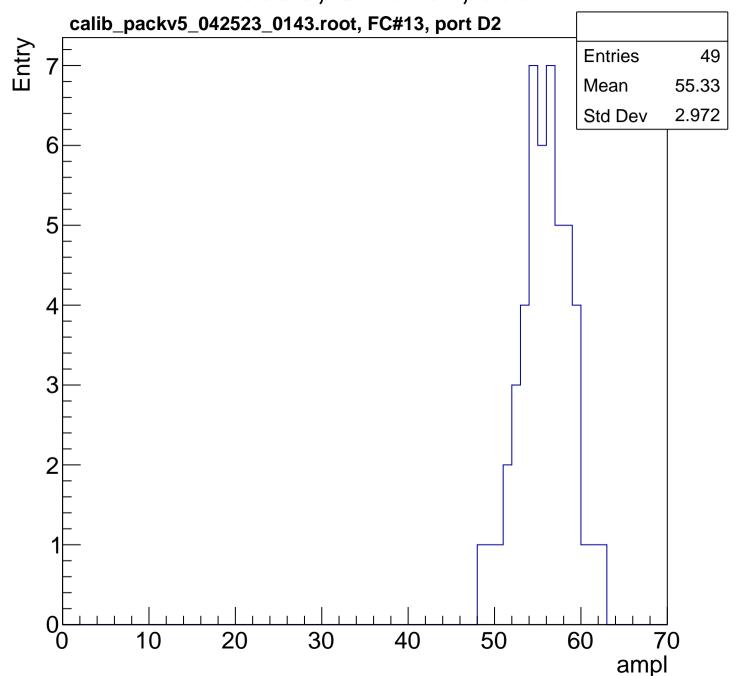


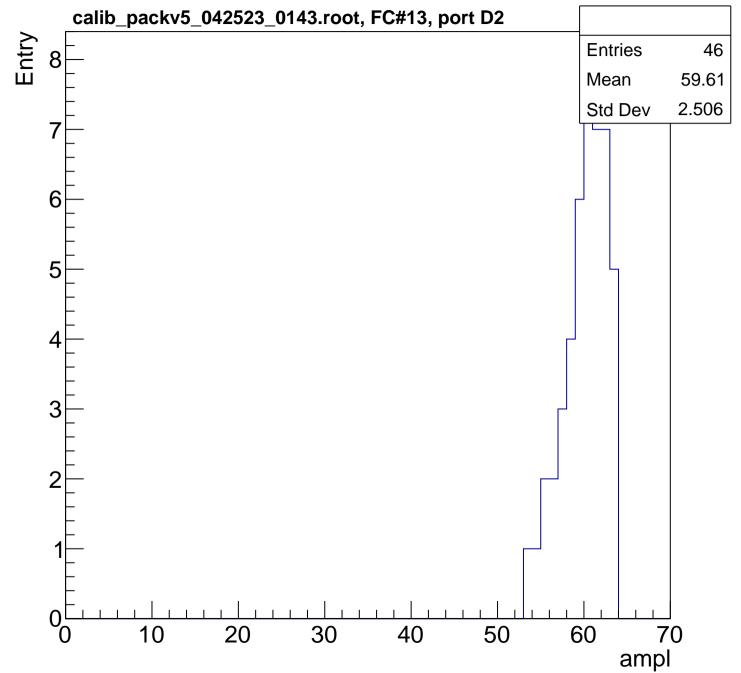


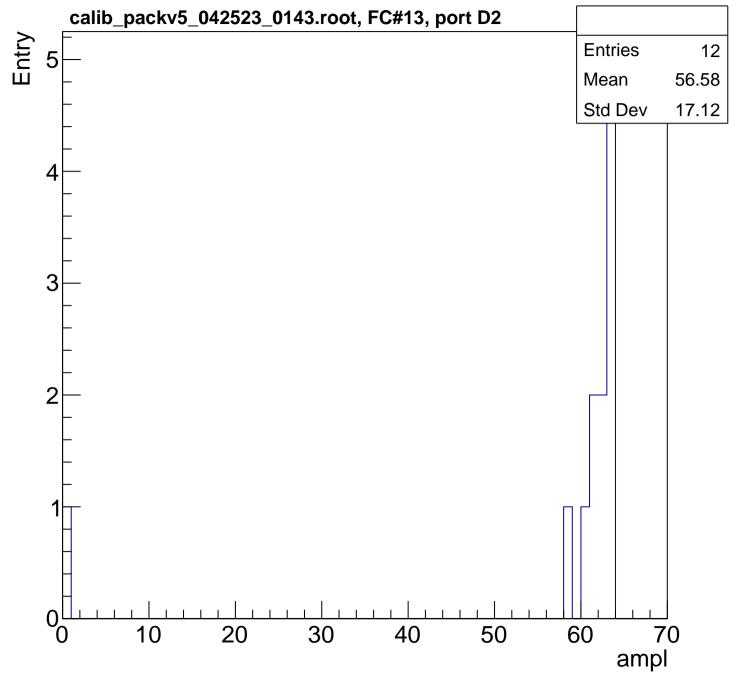




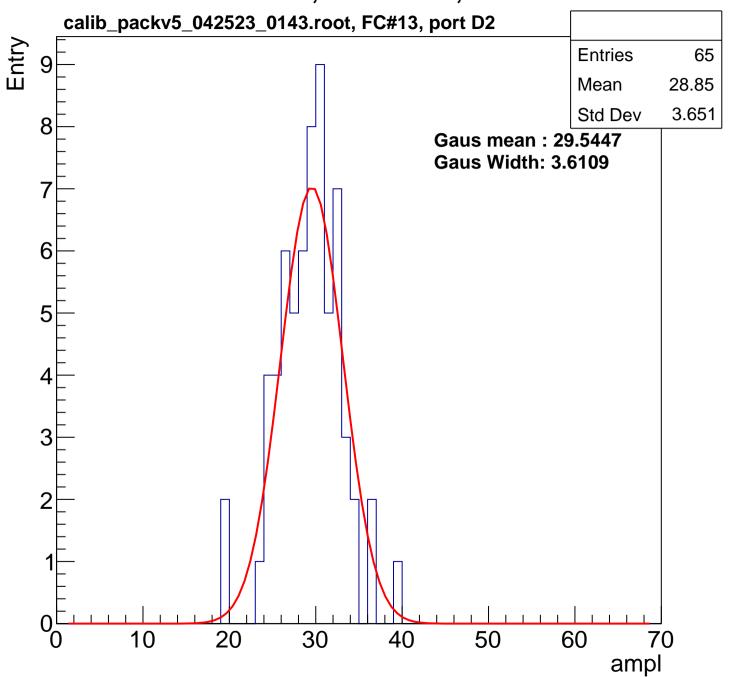


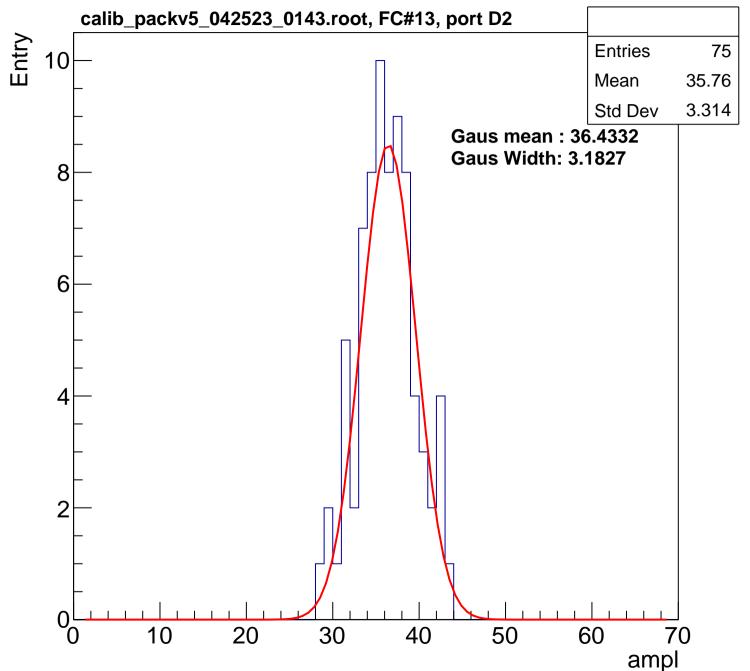


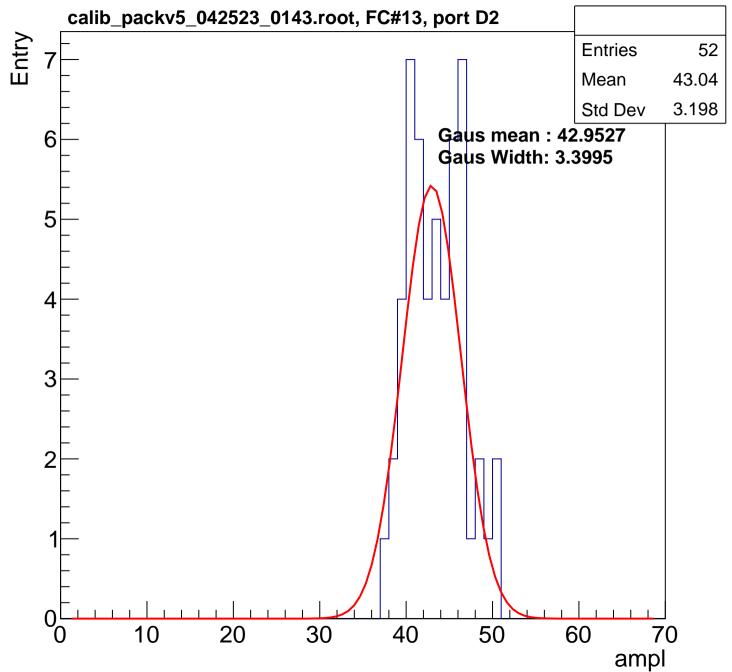


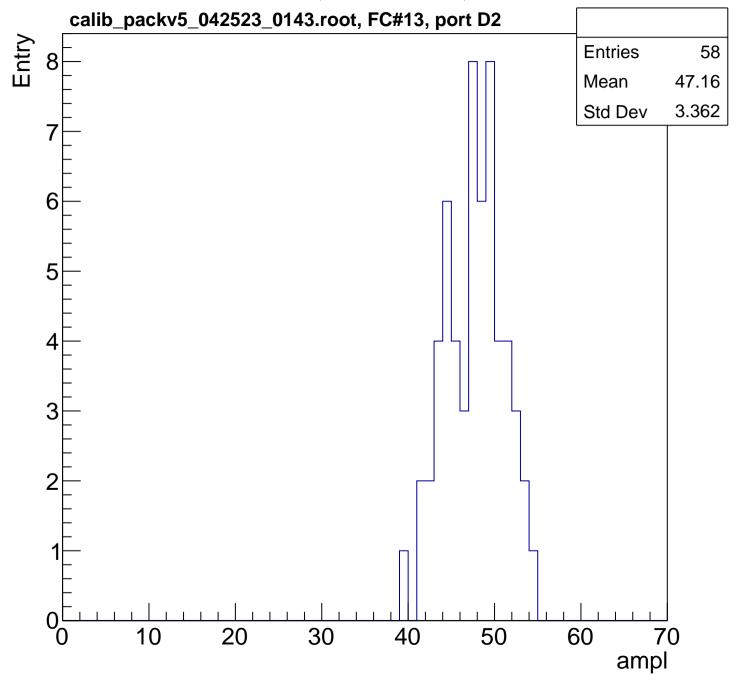


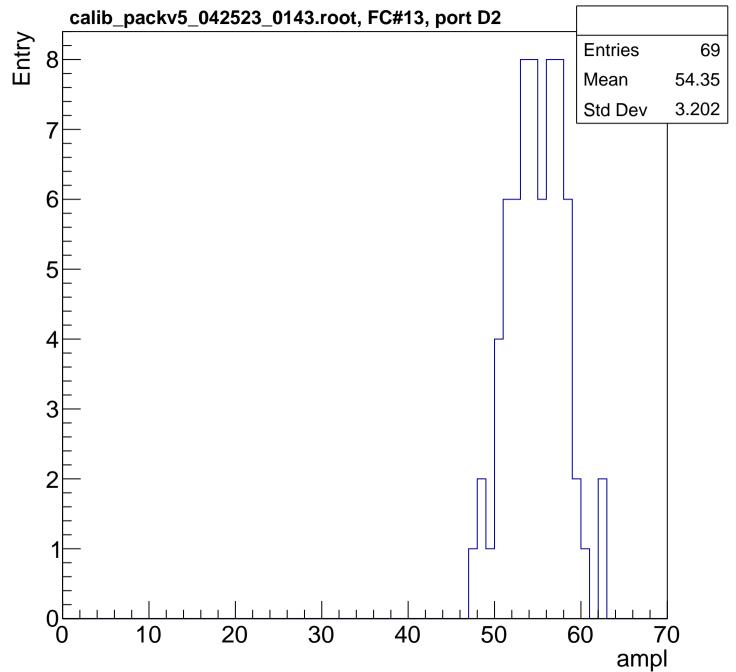


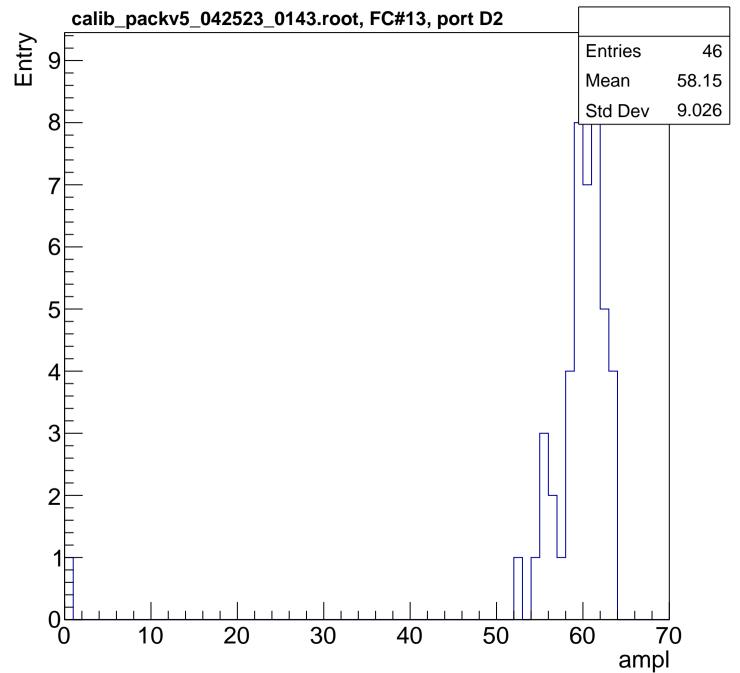


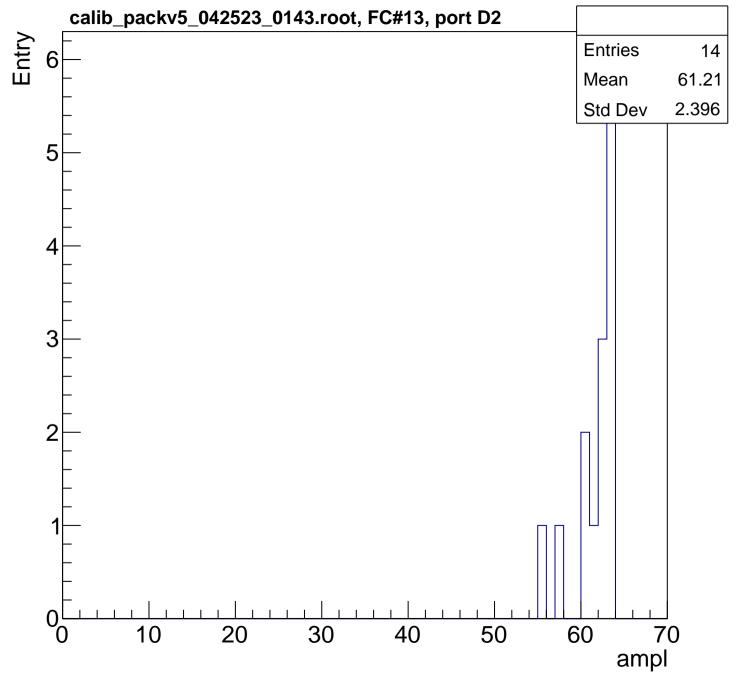




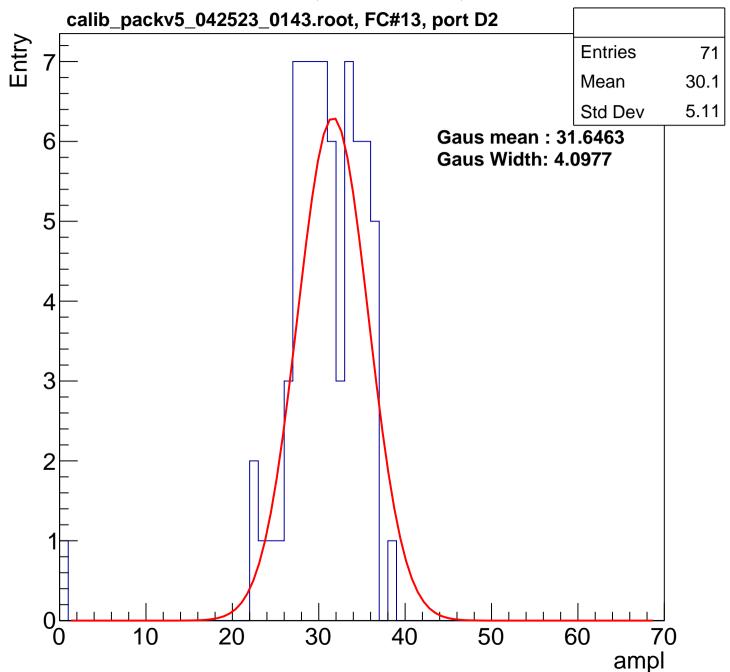


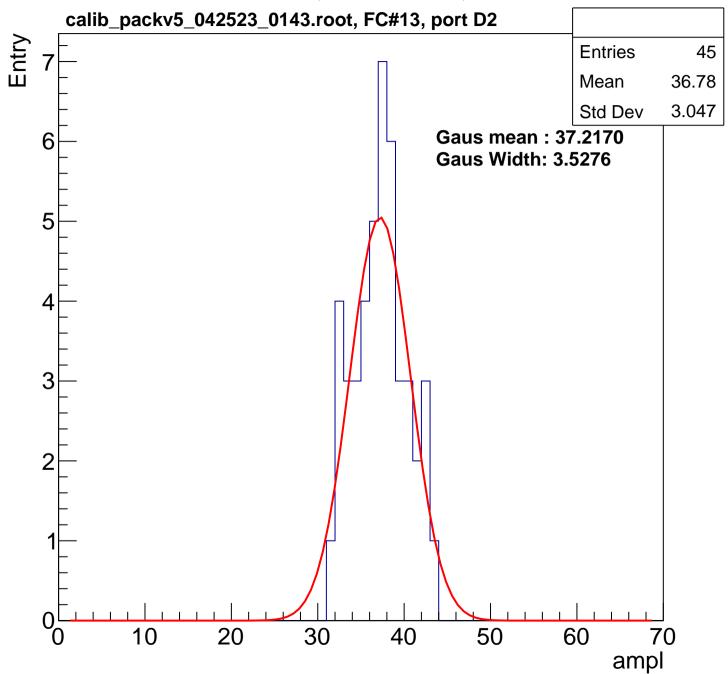


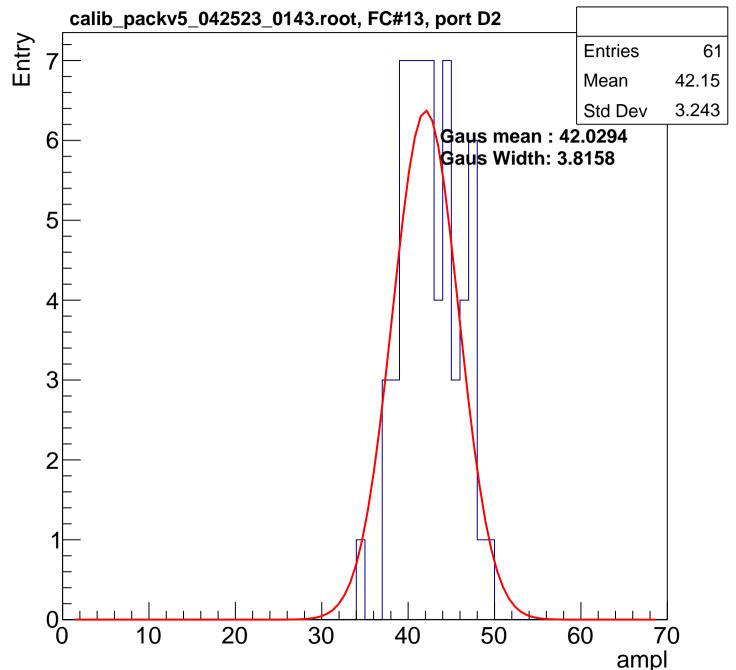


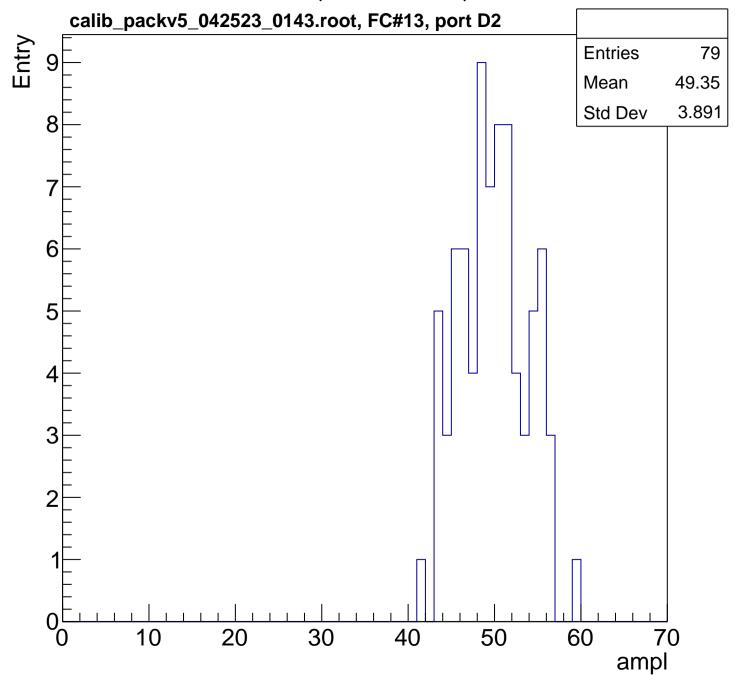


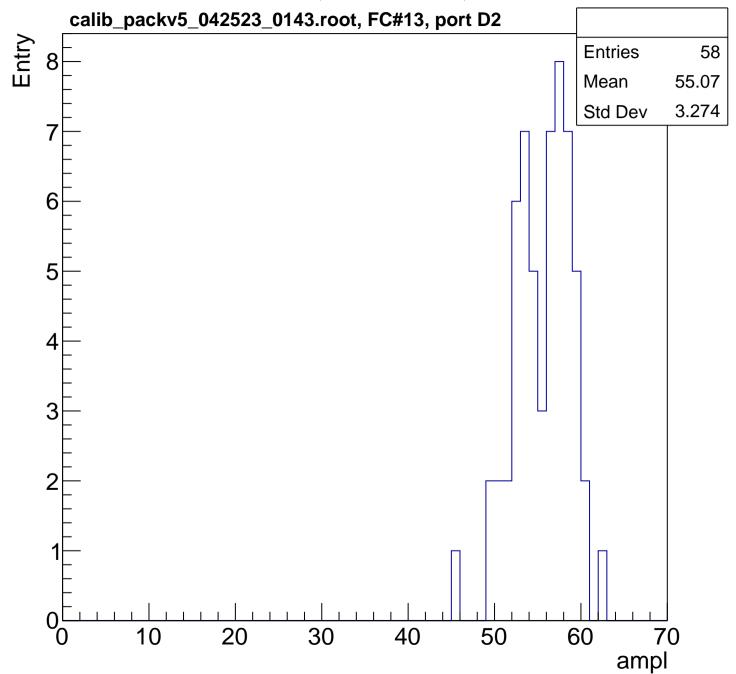
B1L003S, U4-ch38, adc7 calib_packv5_042523_0143.root, FC#13, port D2 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

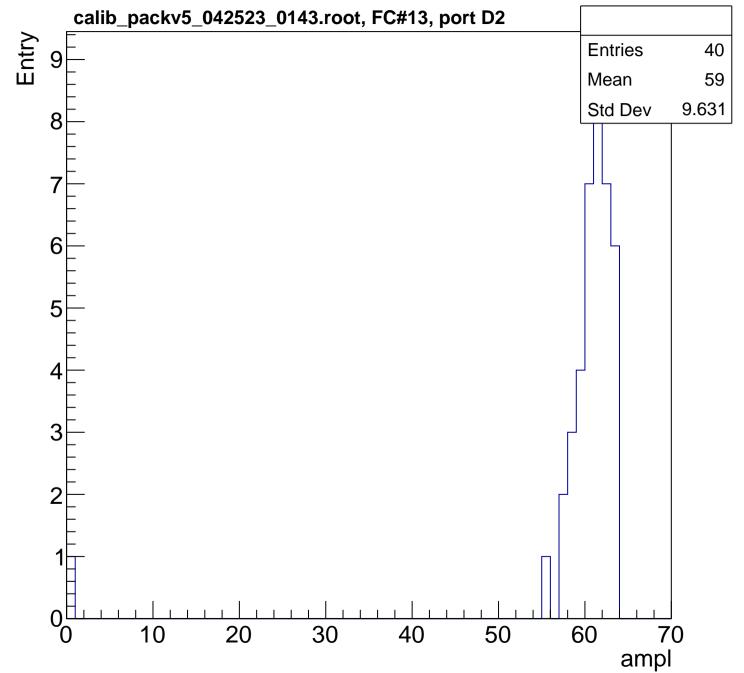


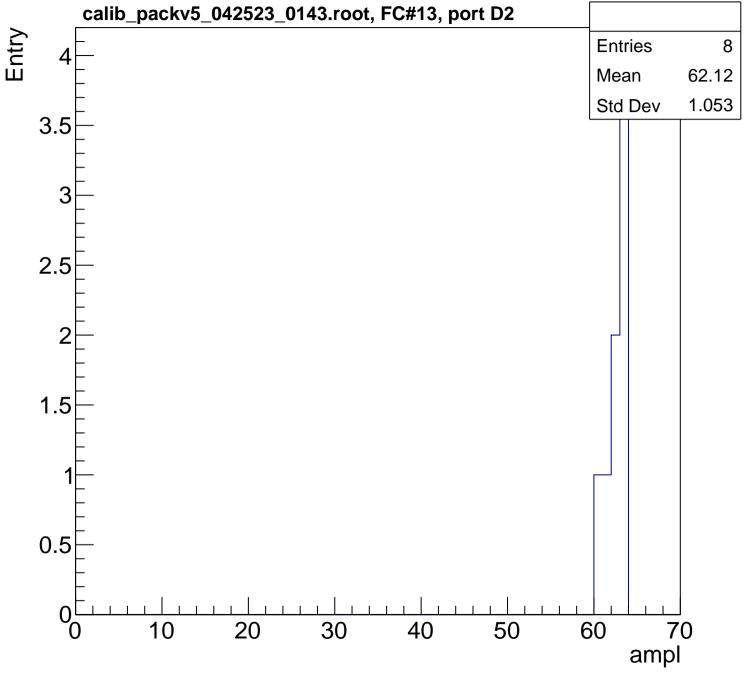




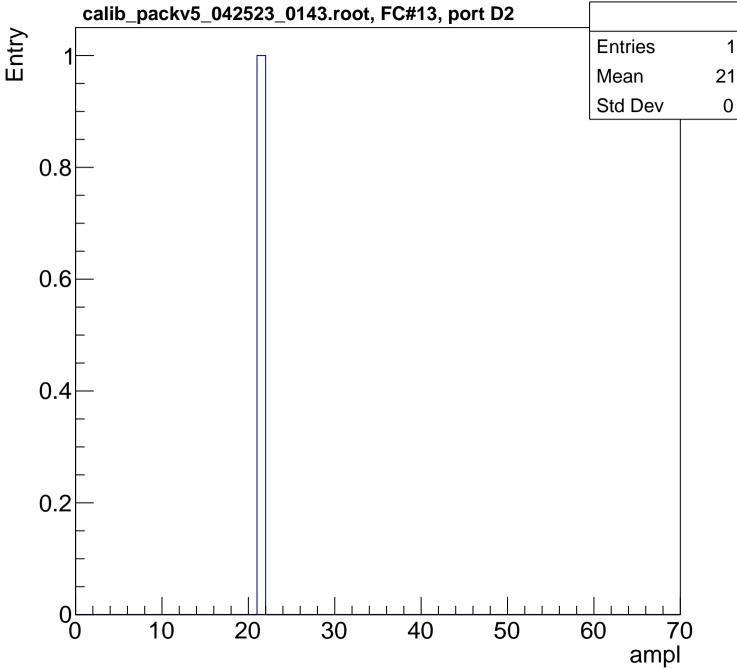


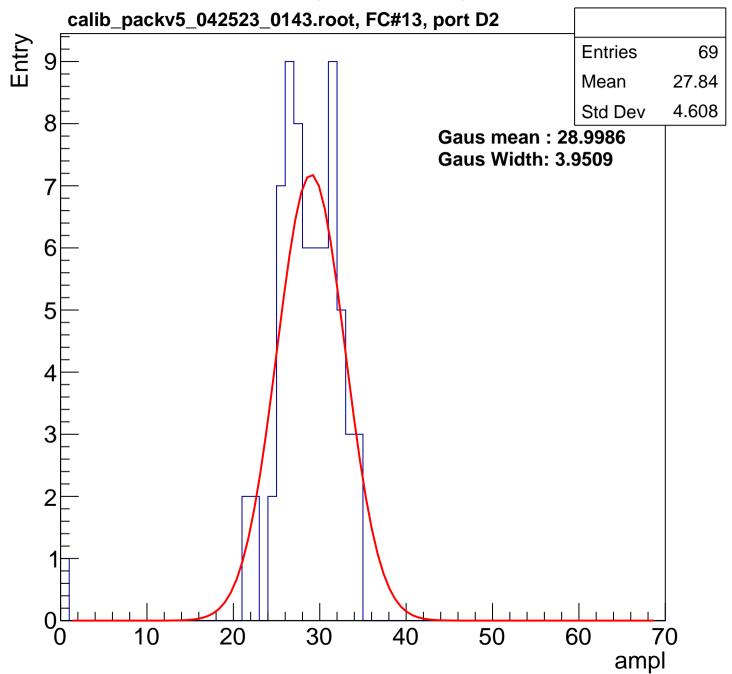


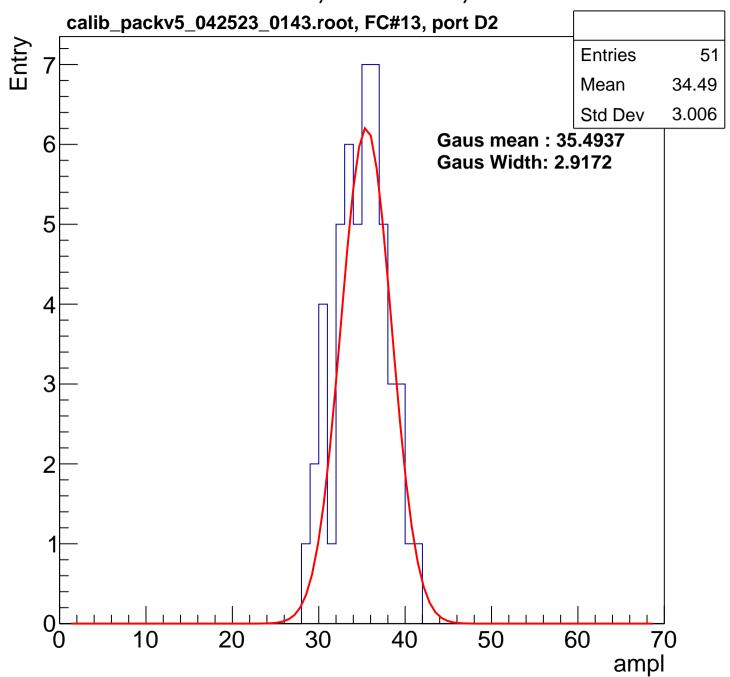


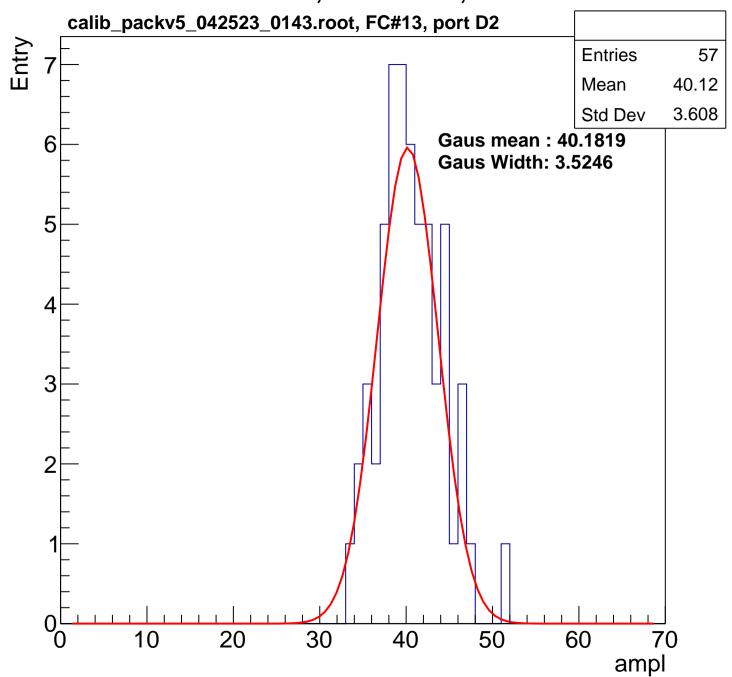


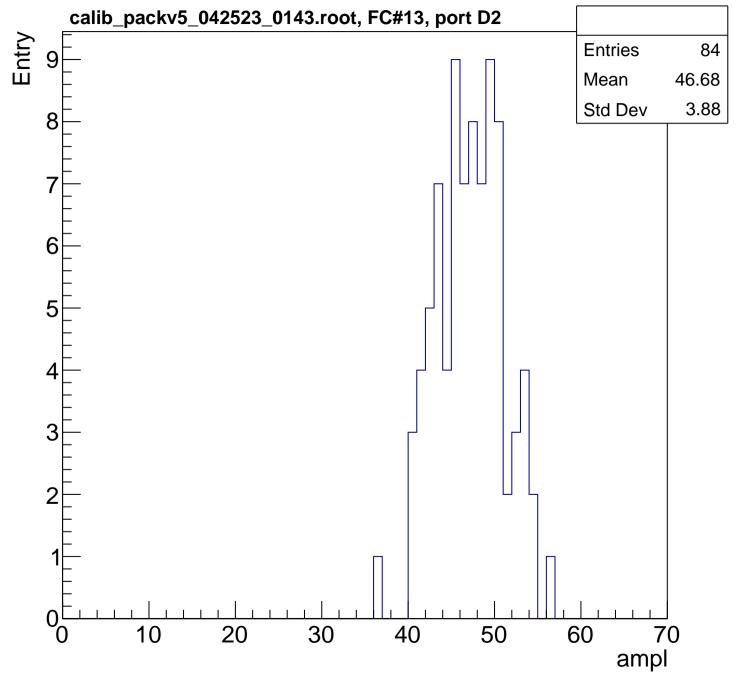
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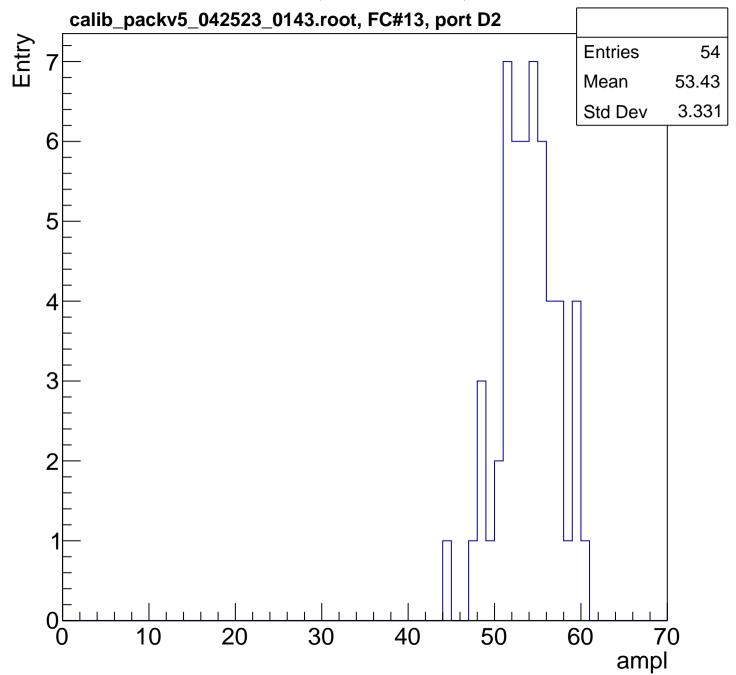


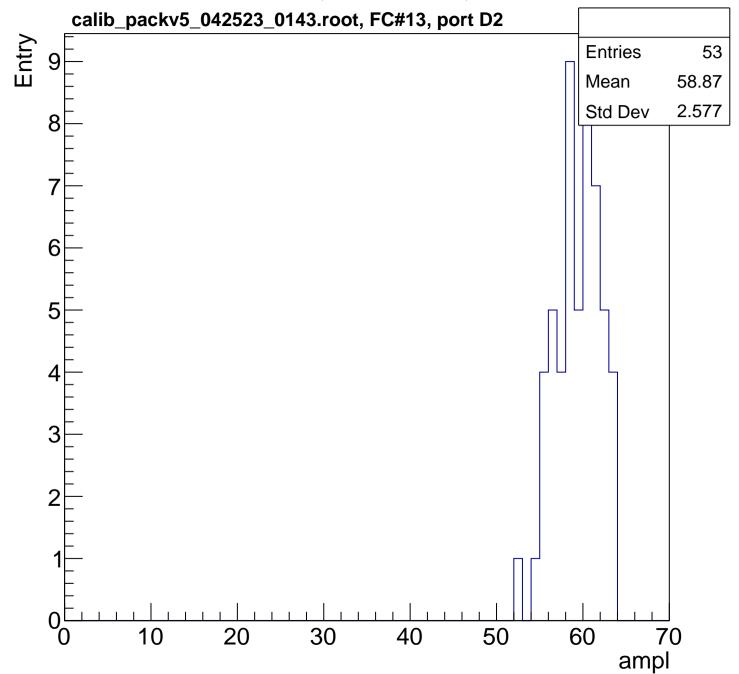


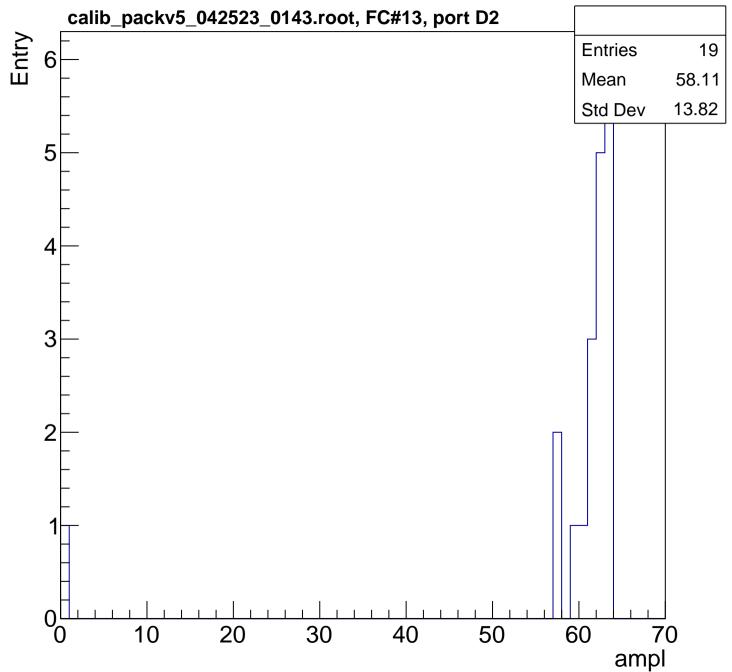




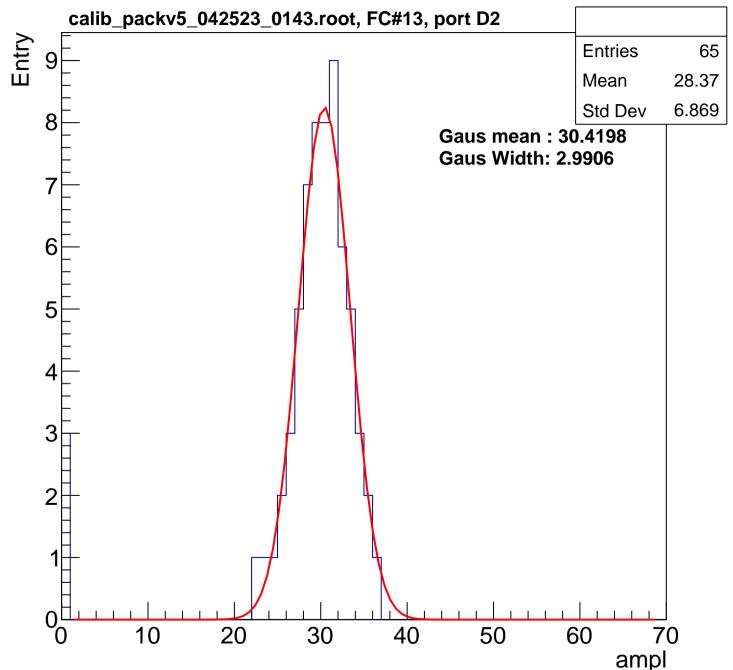


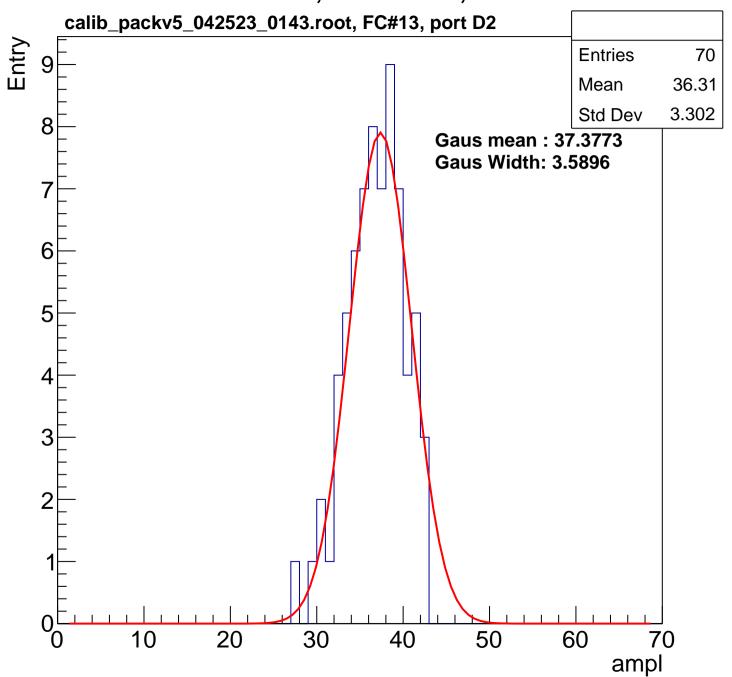


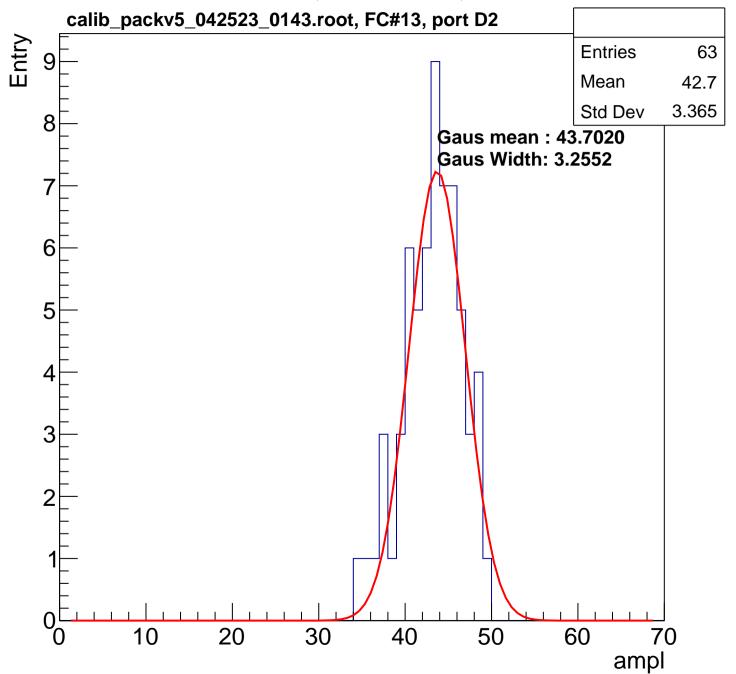


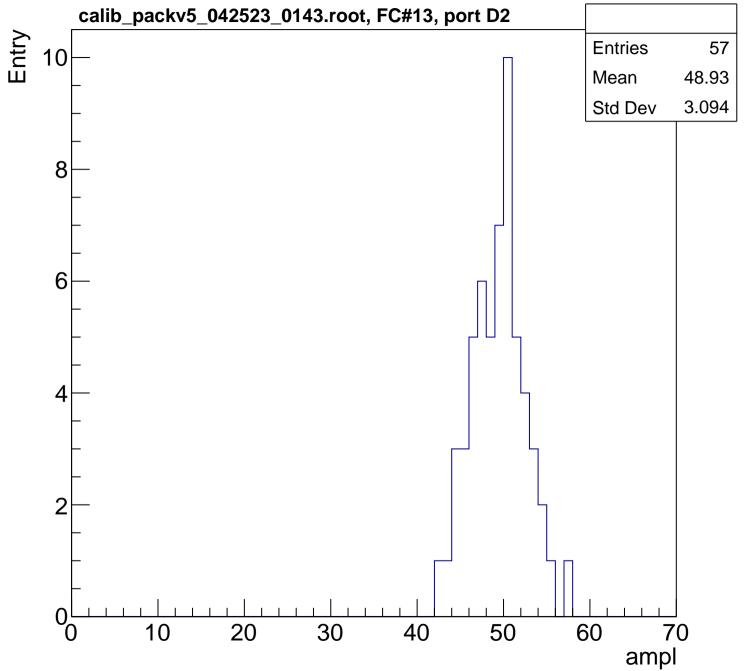


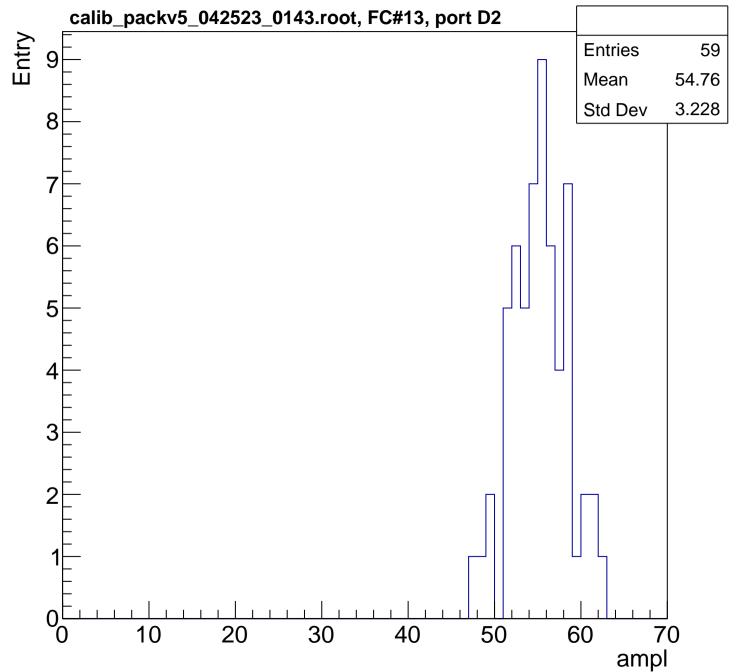


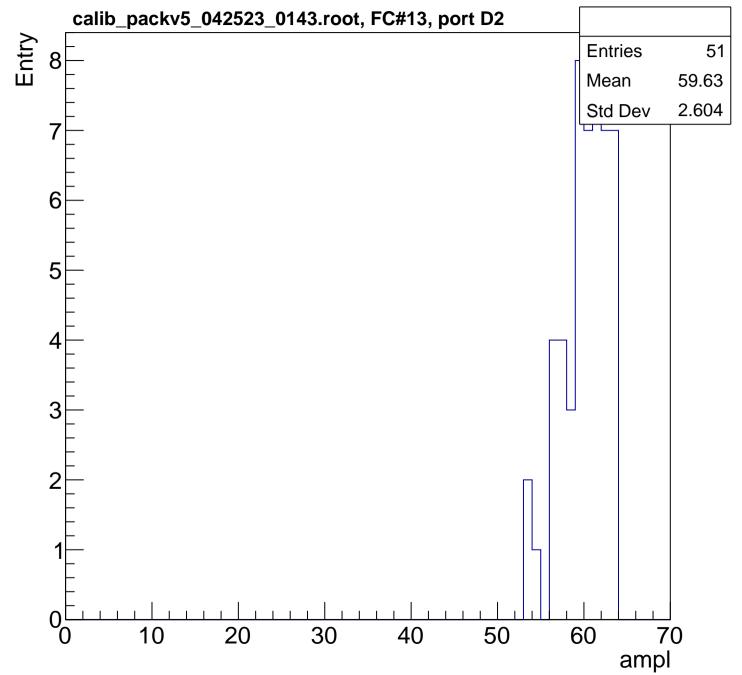


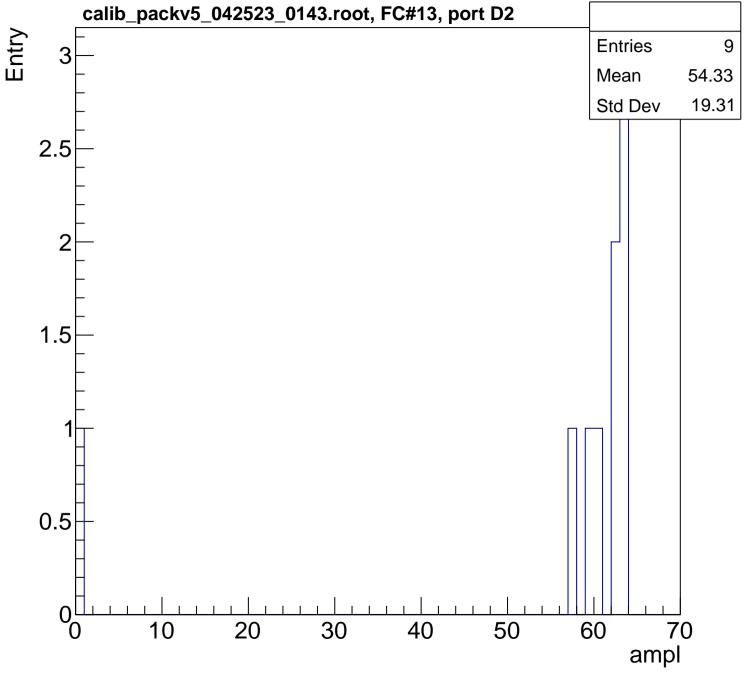




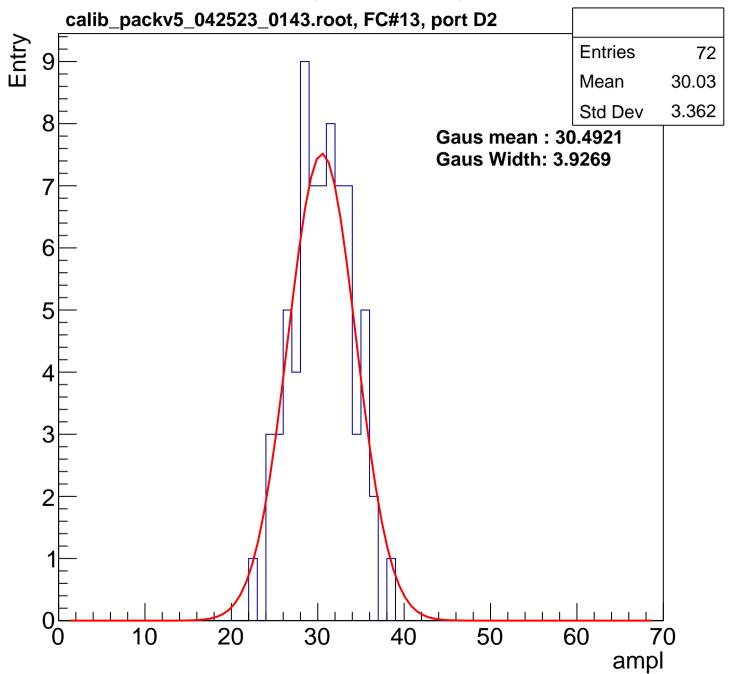


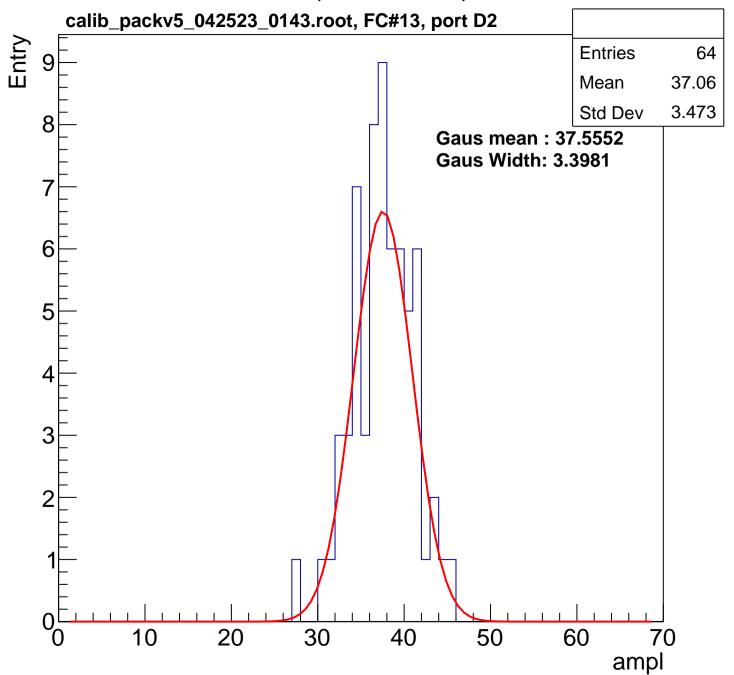


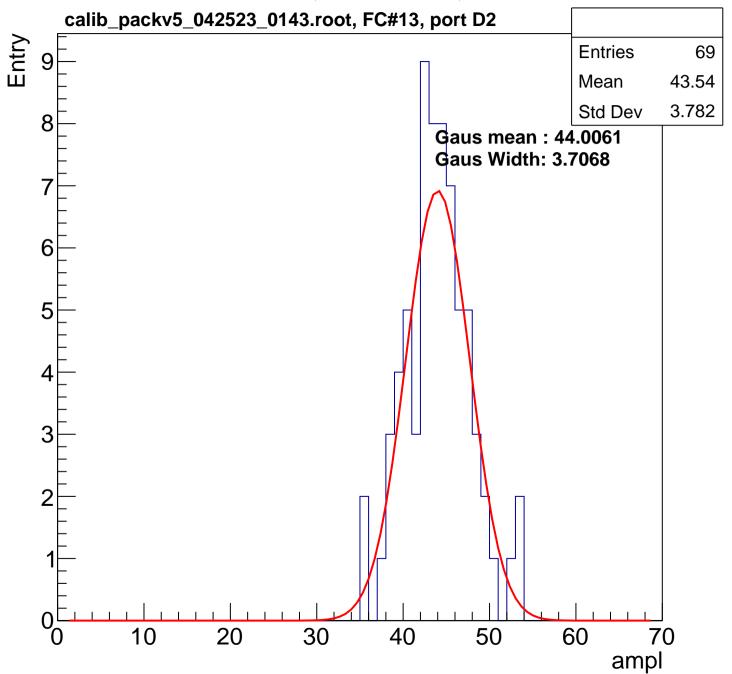


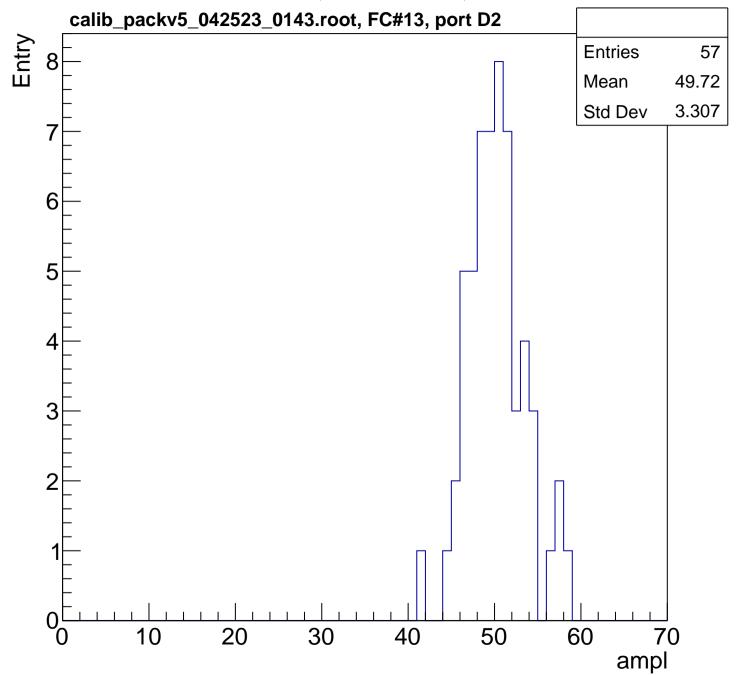


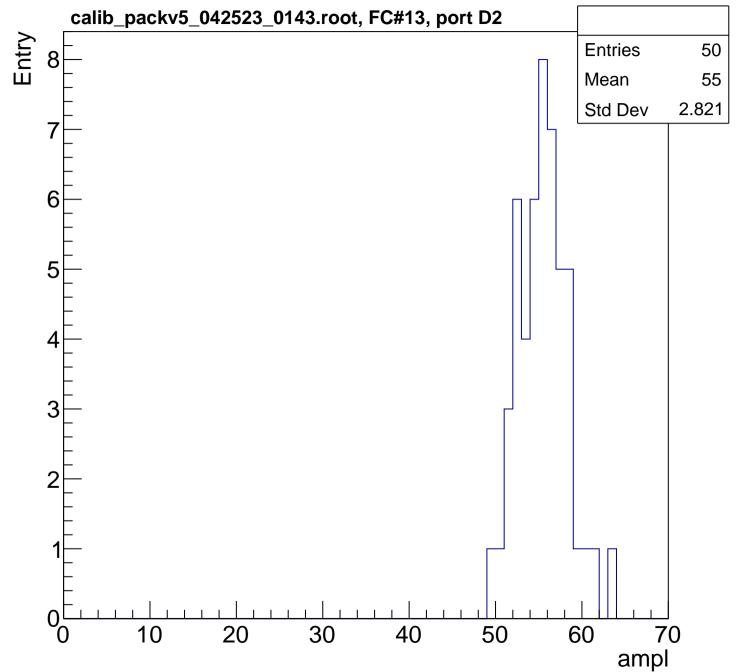


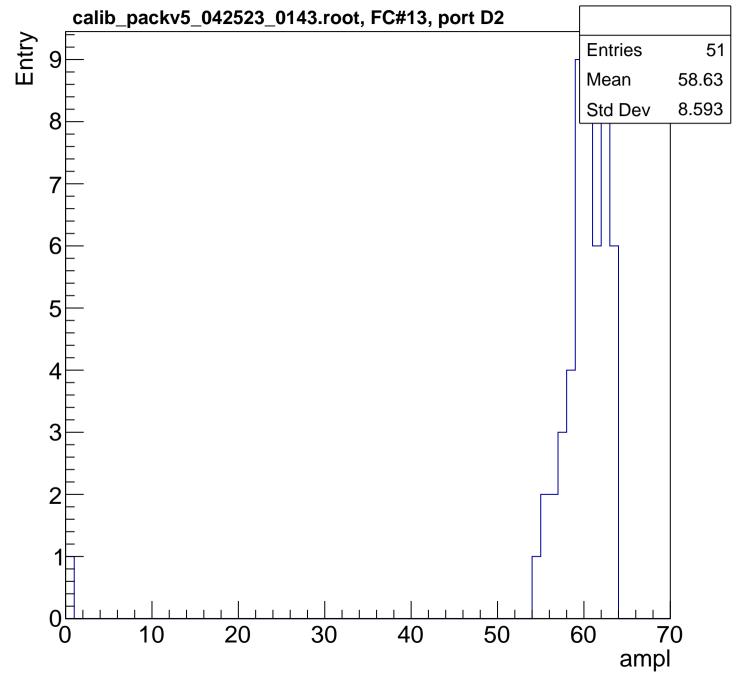


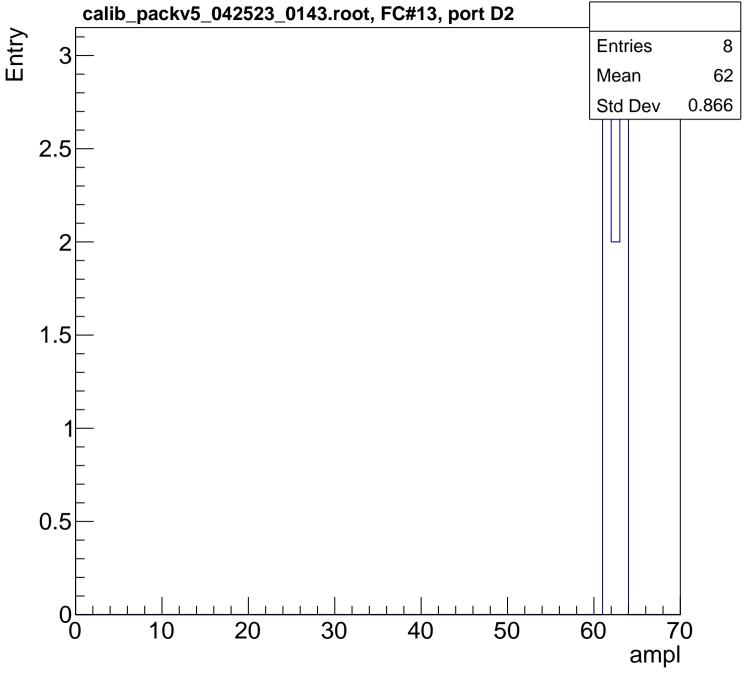




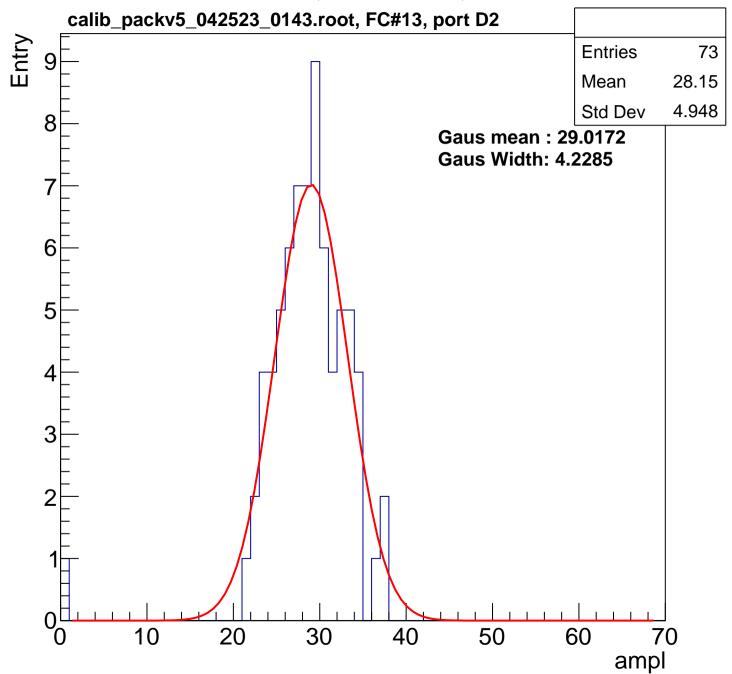


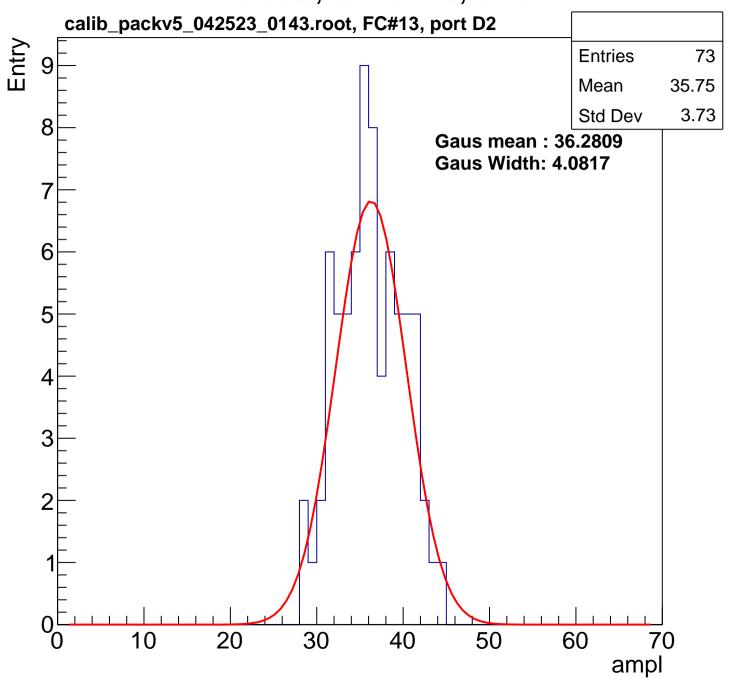


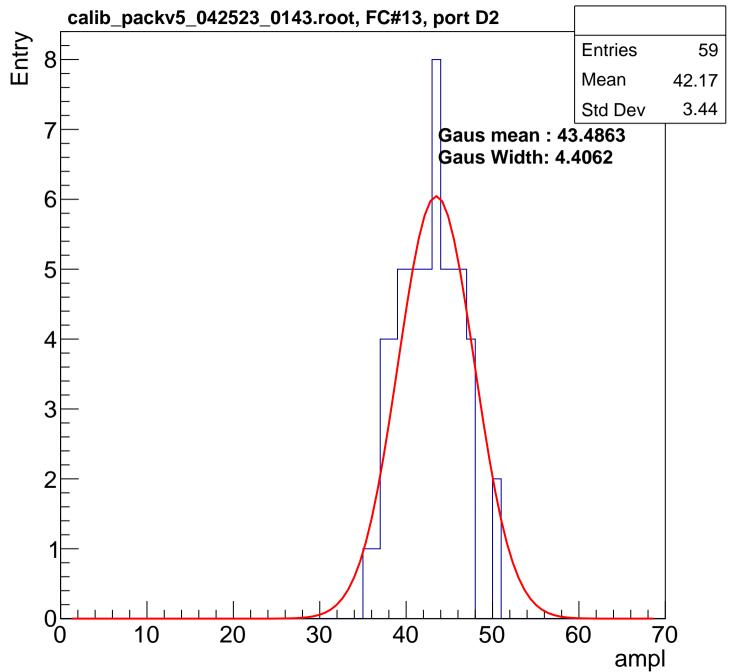


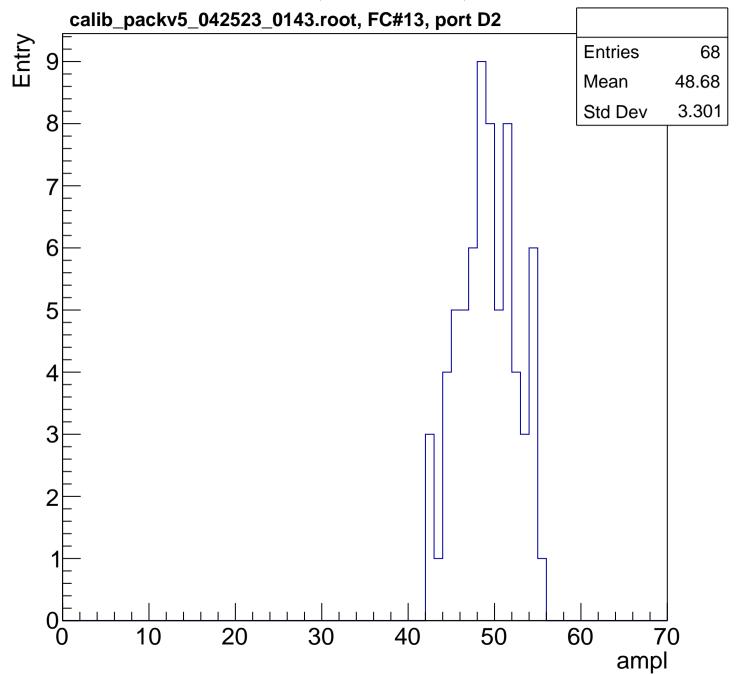


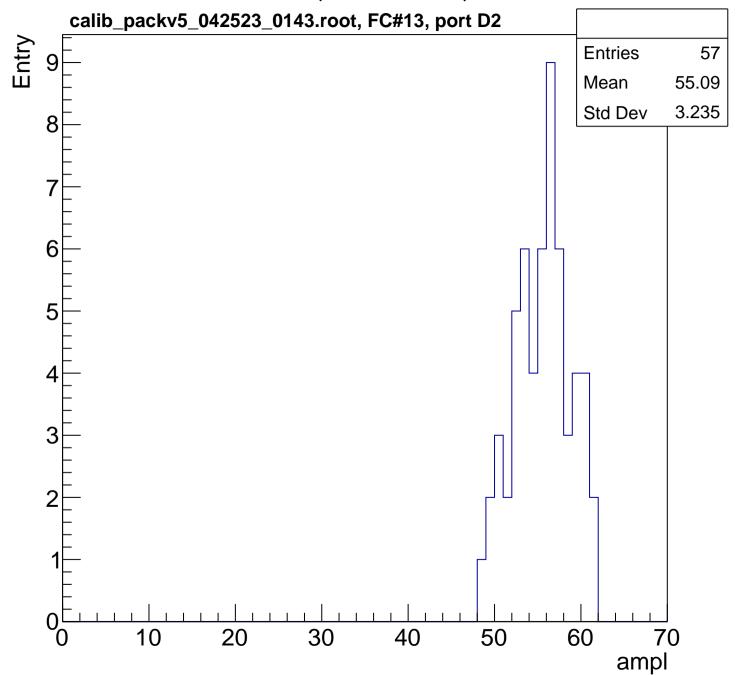
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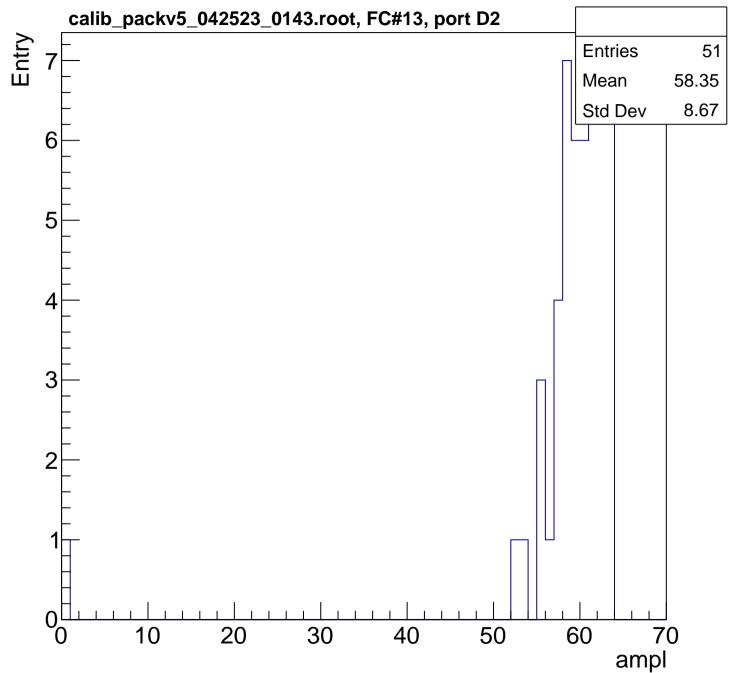


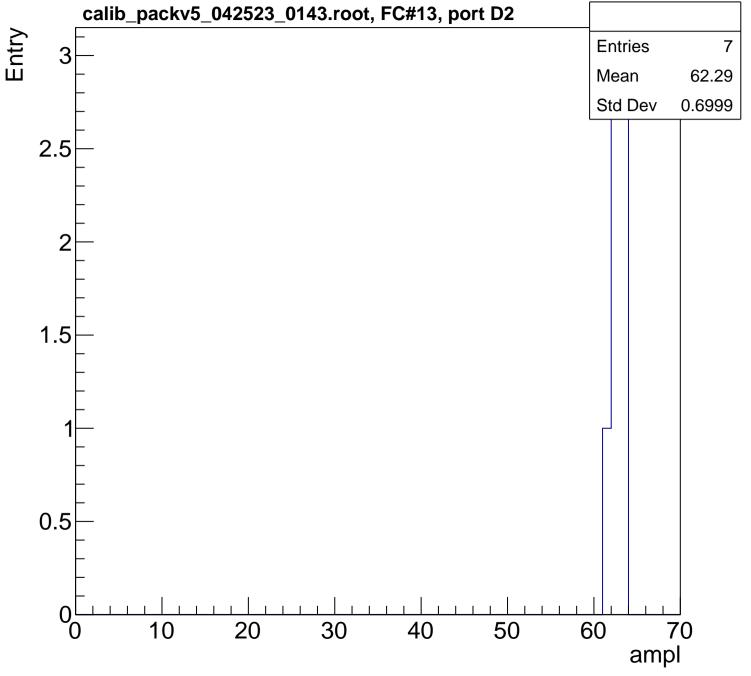




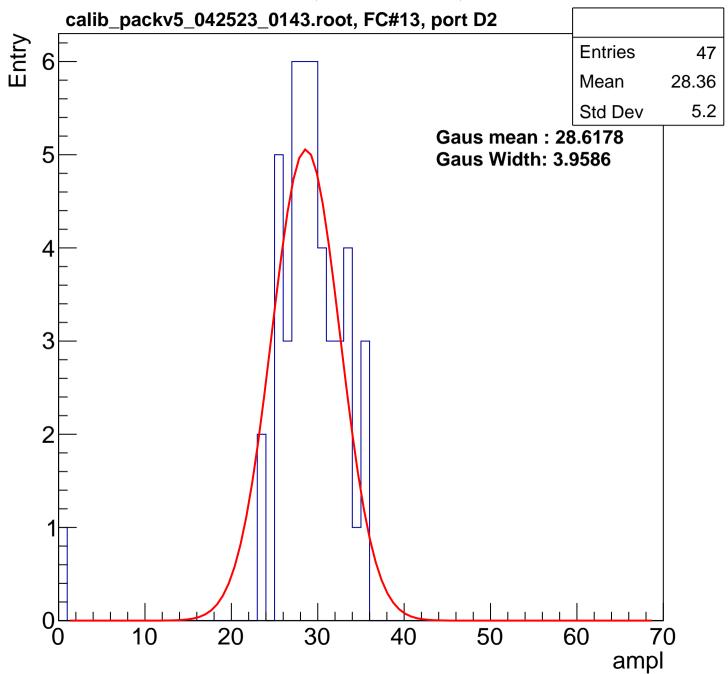


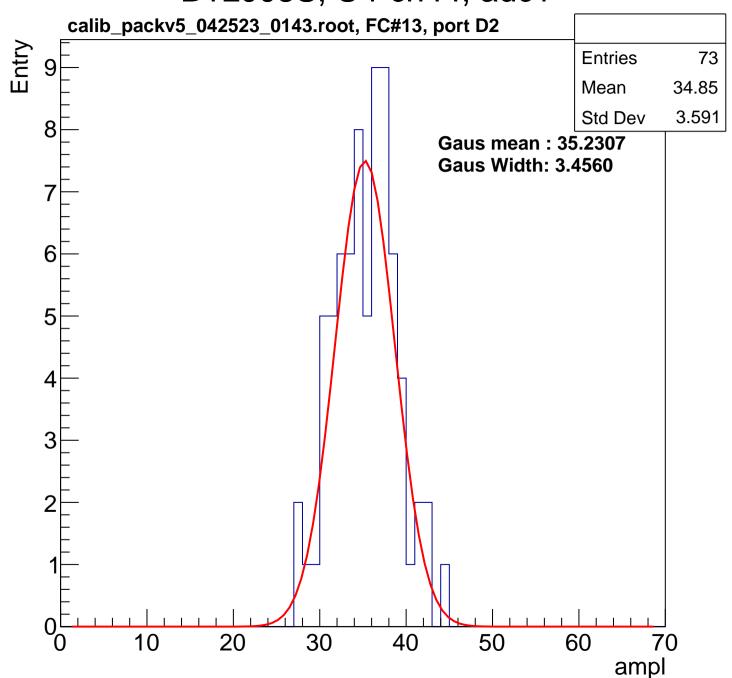


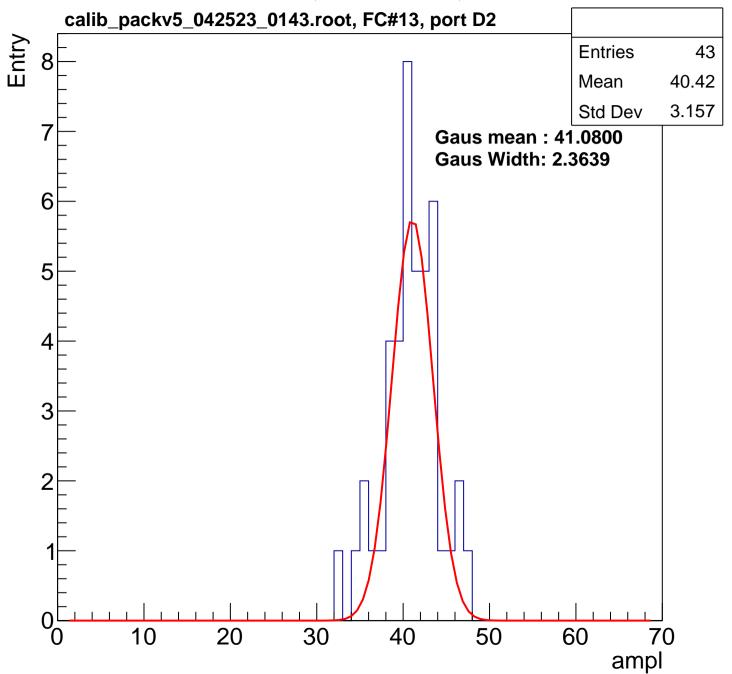


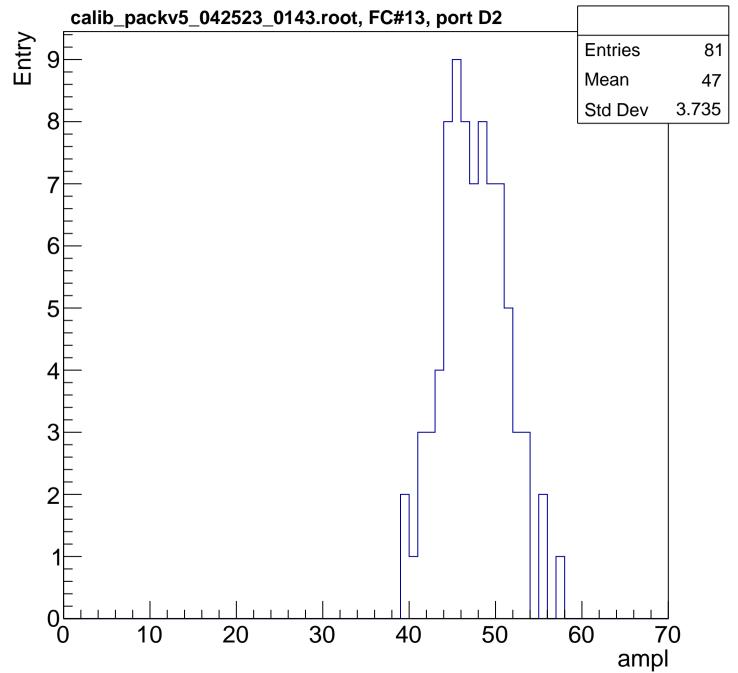


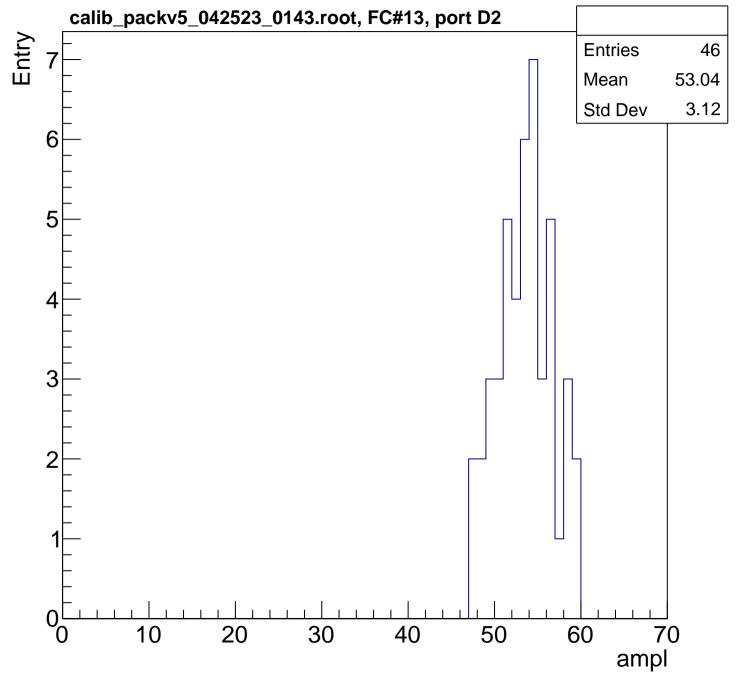


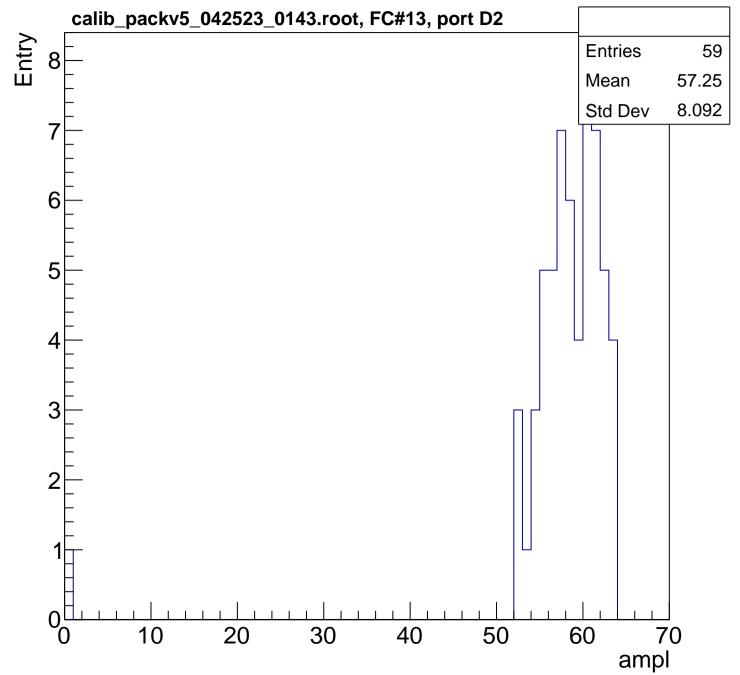


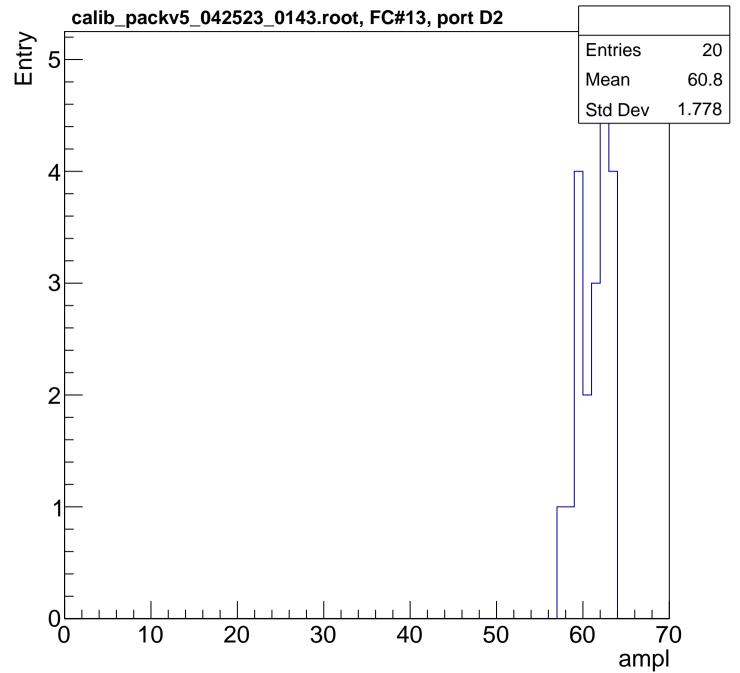


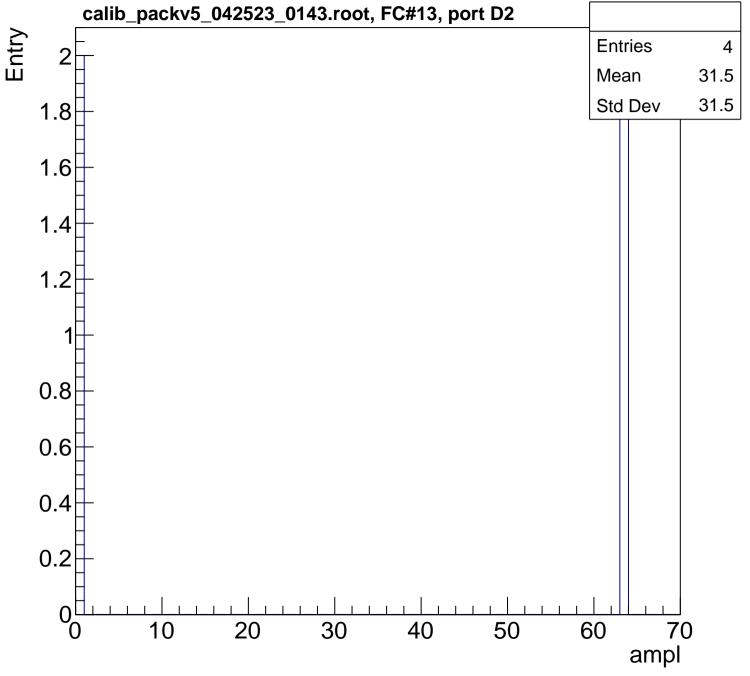


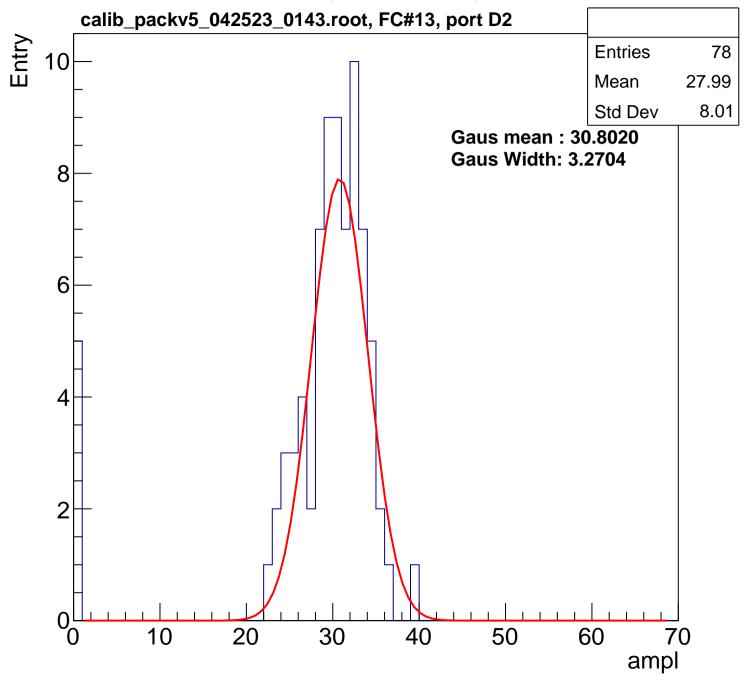


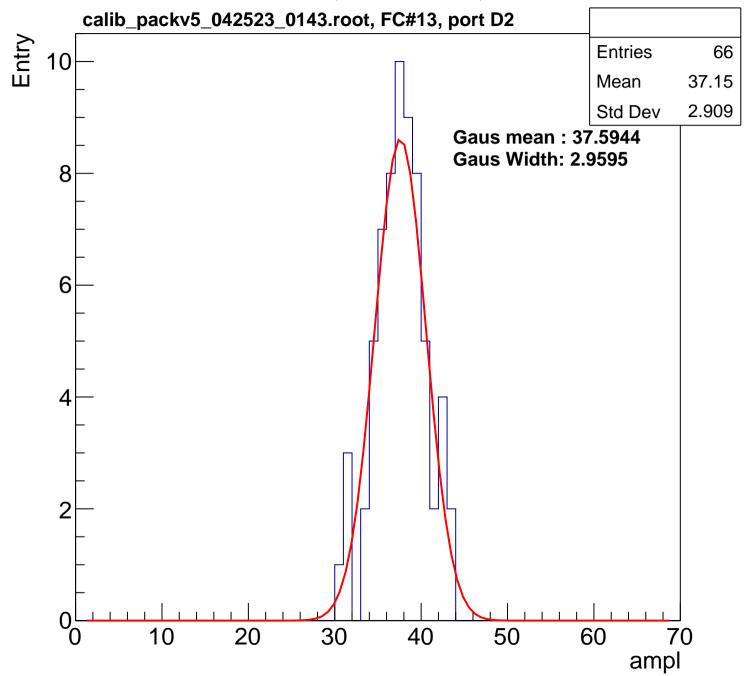


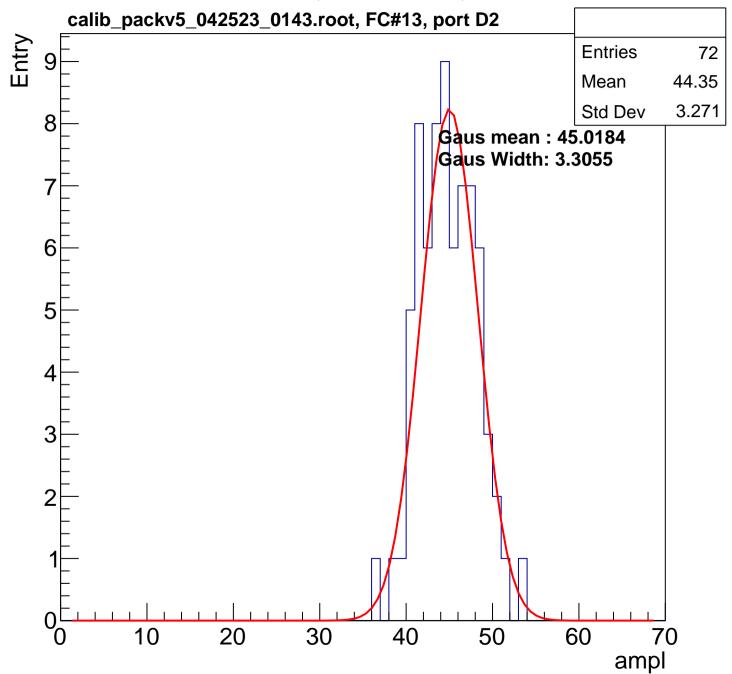


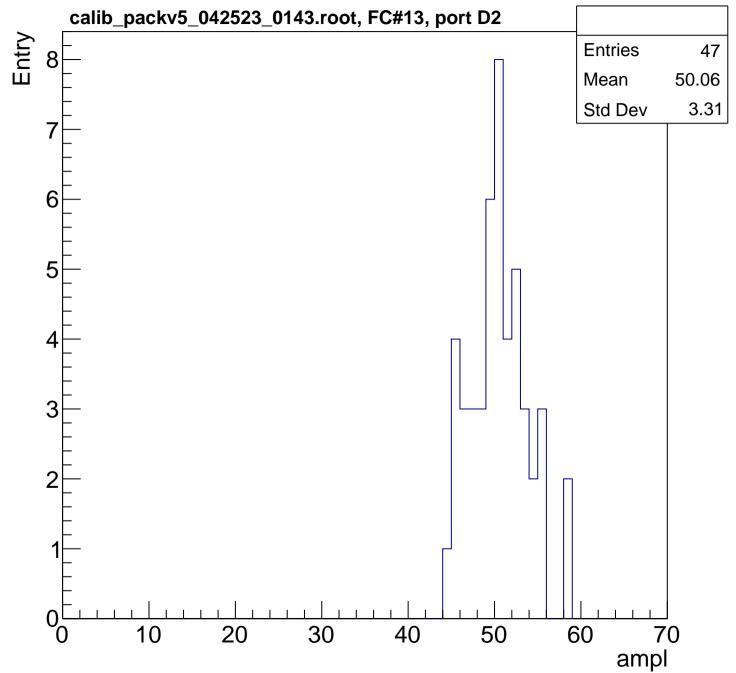


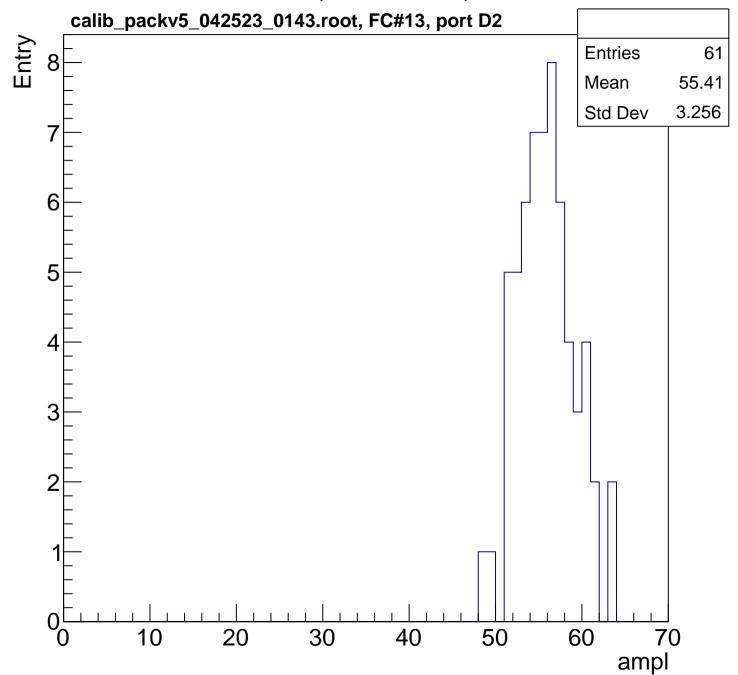


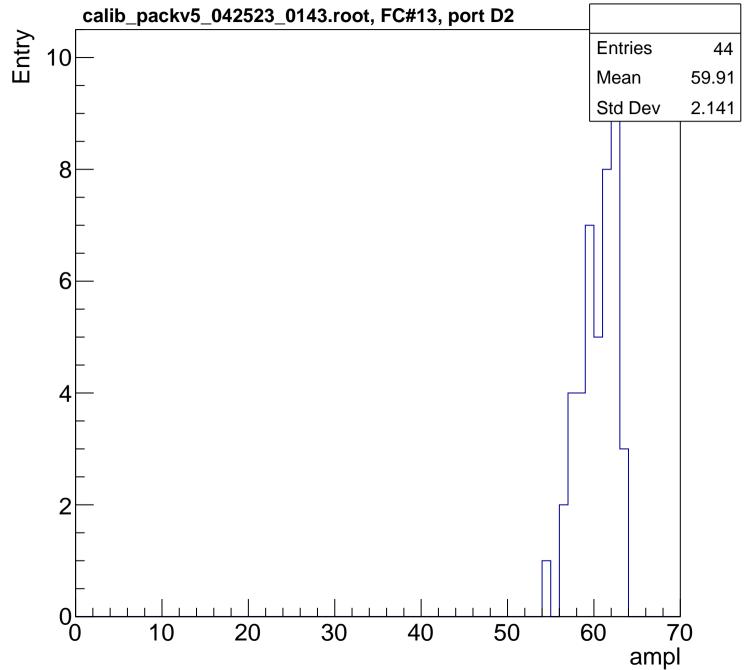


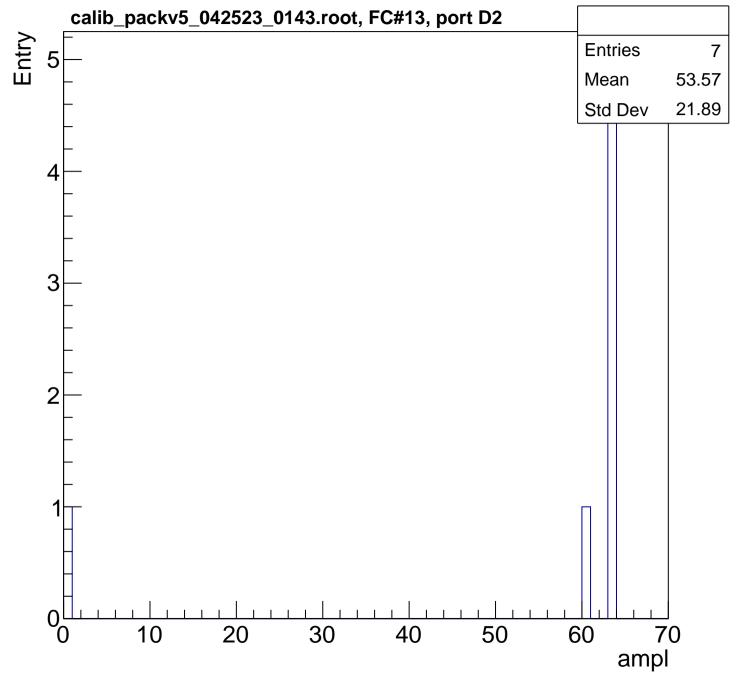


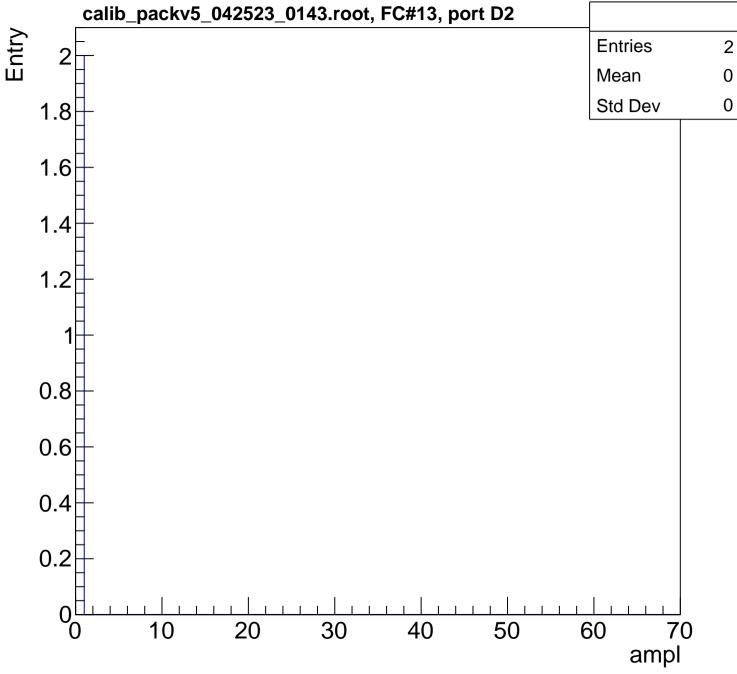


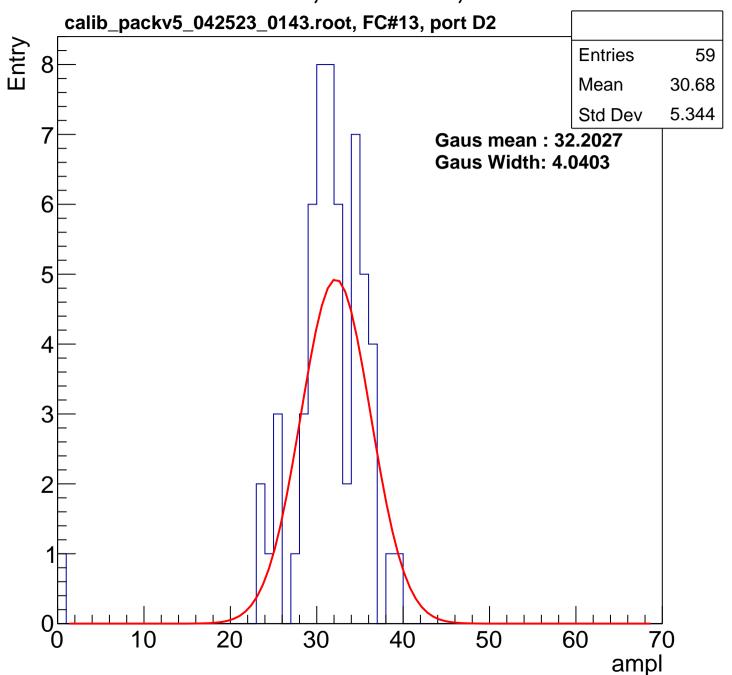


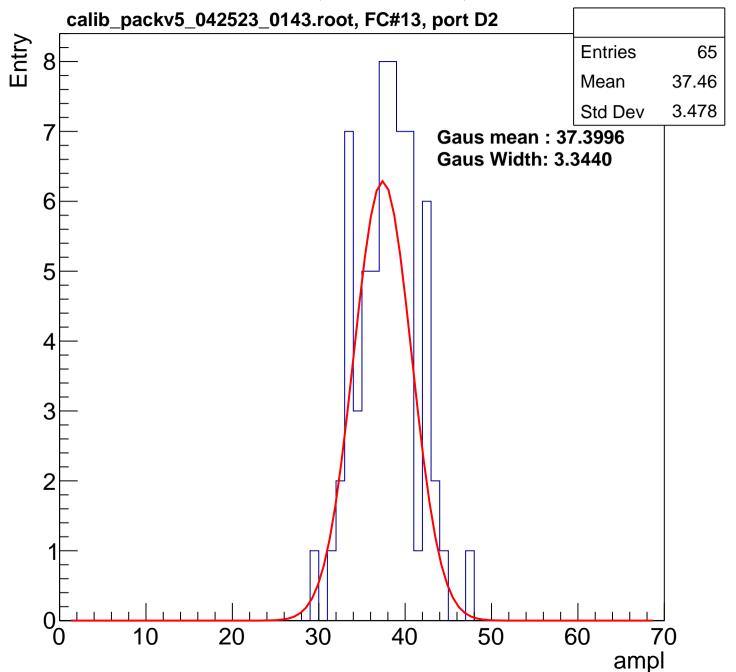


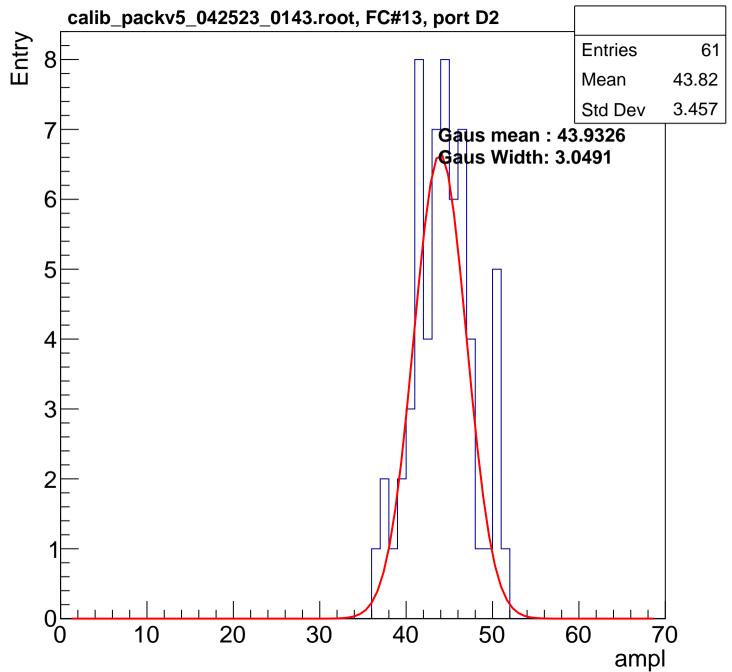


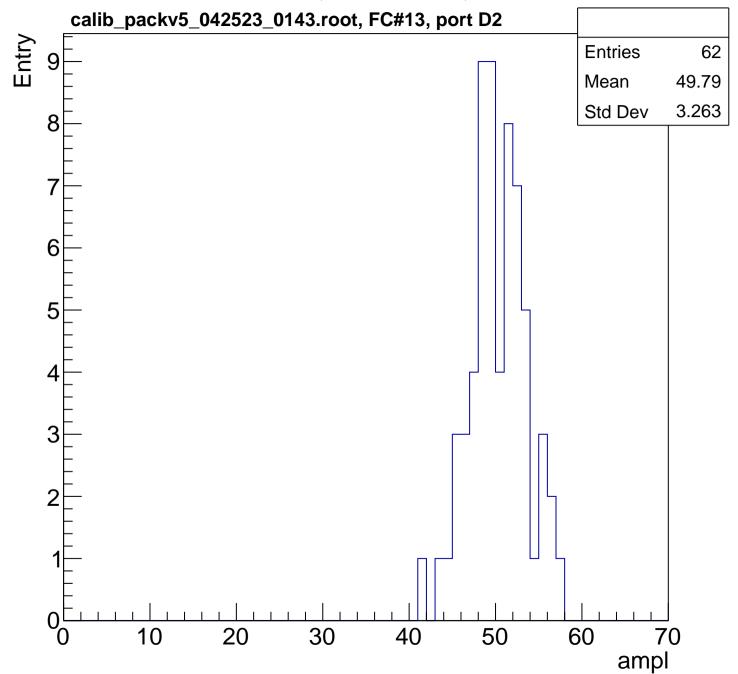


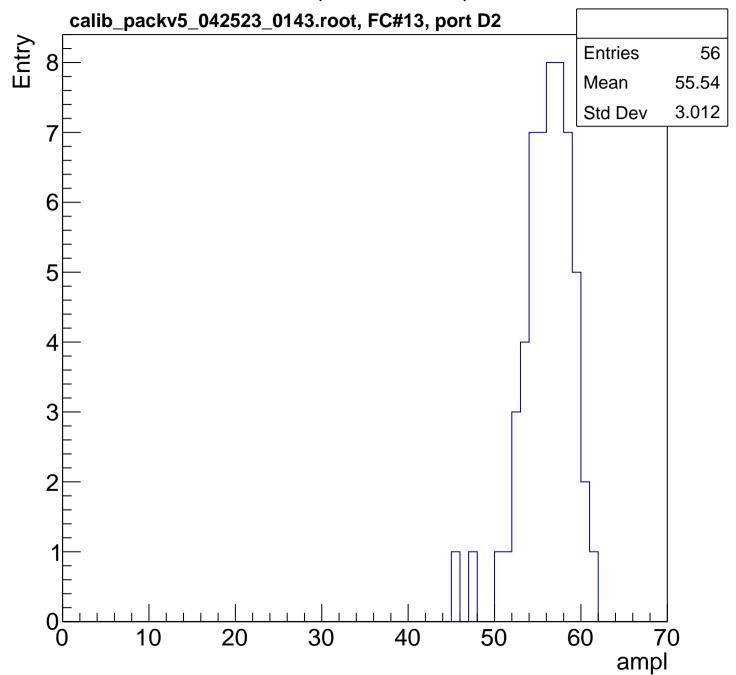


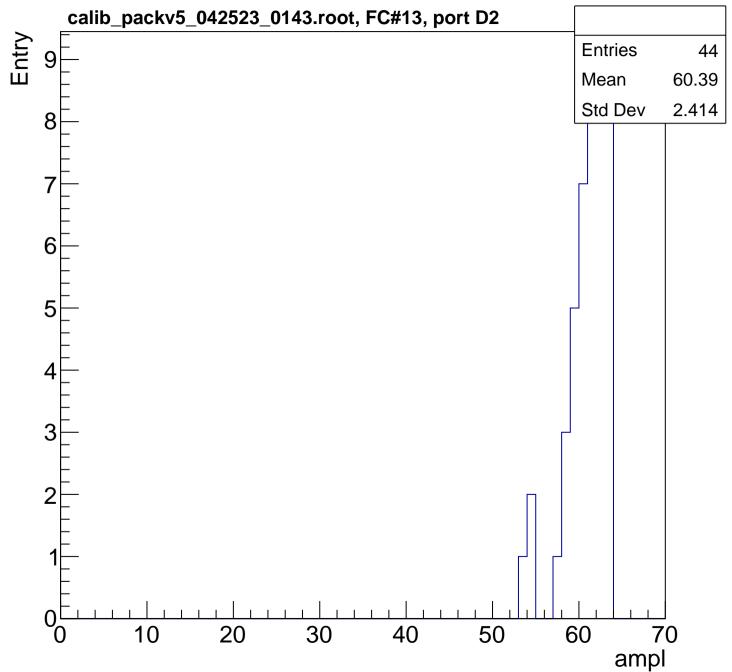


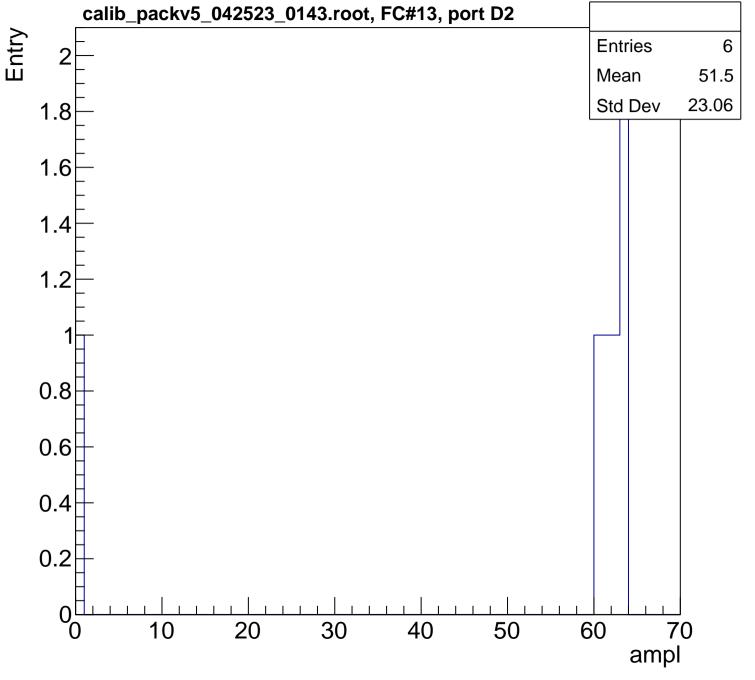




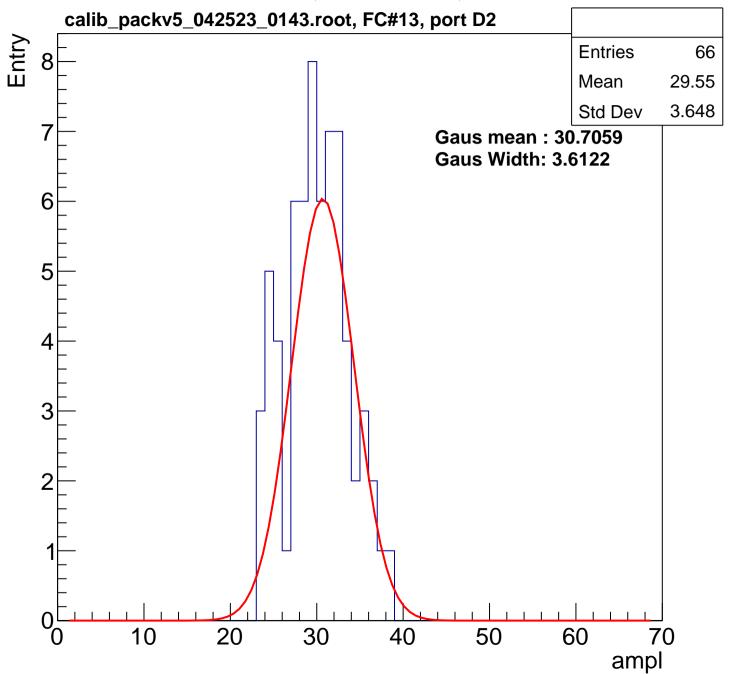


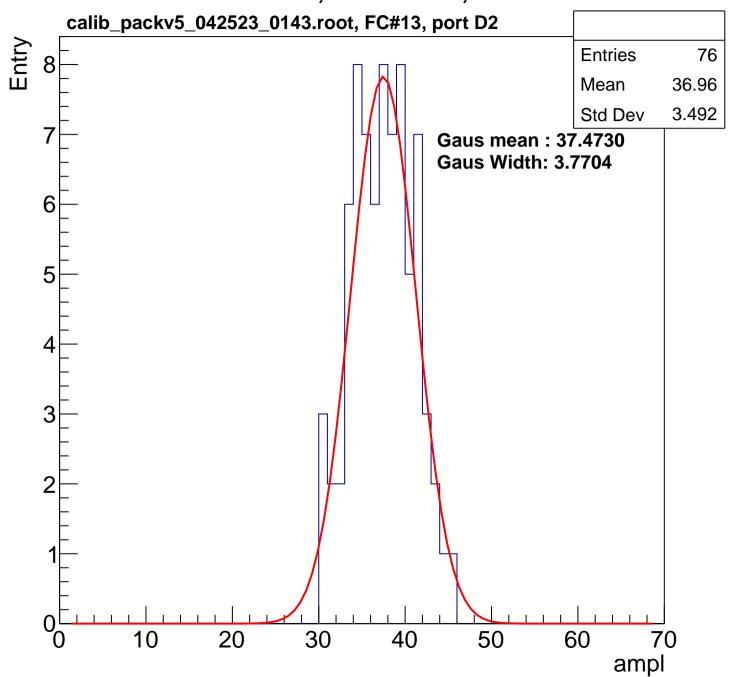


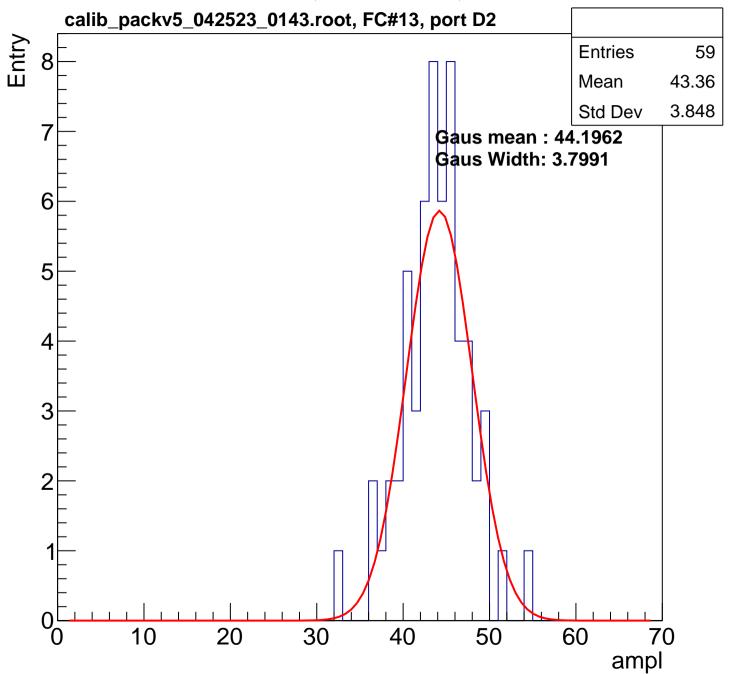


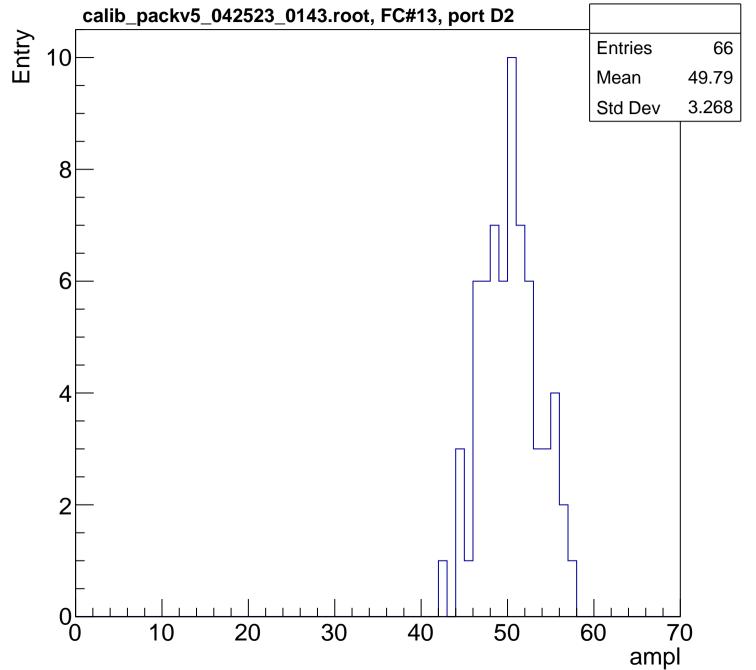


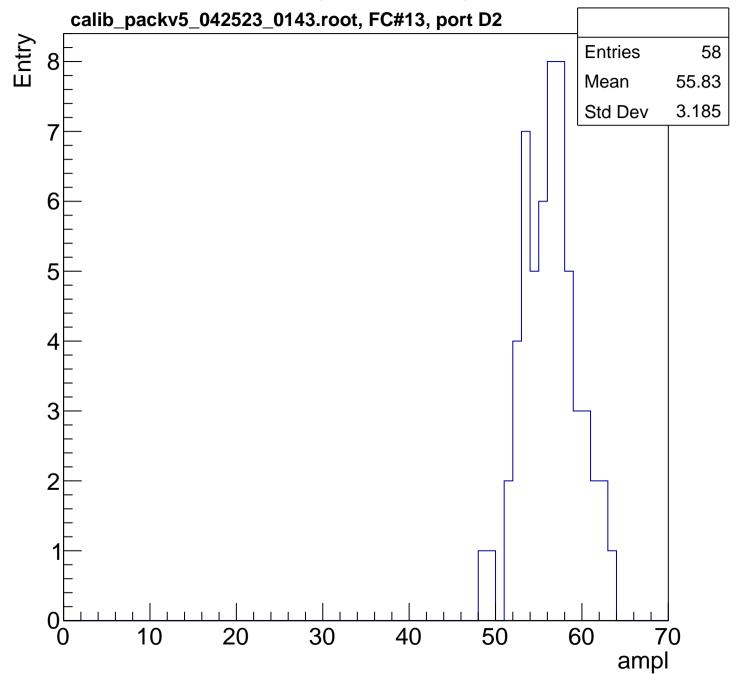
B1L003S, U4-ch46, adc7 calib_packv5_042523_0143.root, FC#13, port D2 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

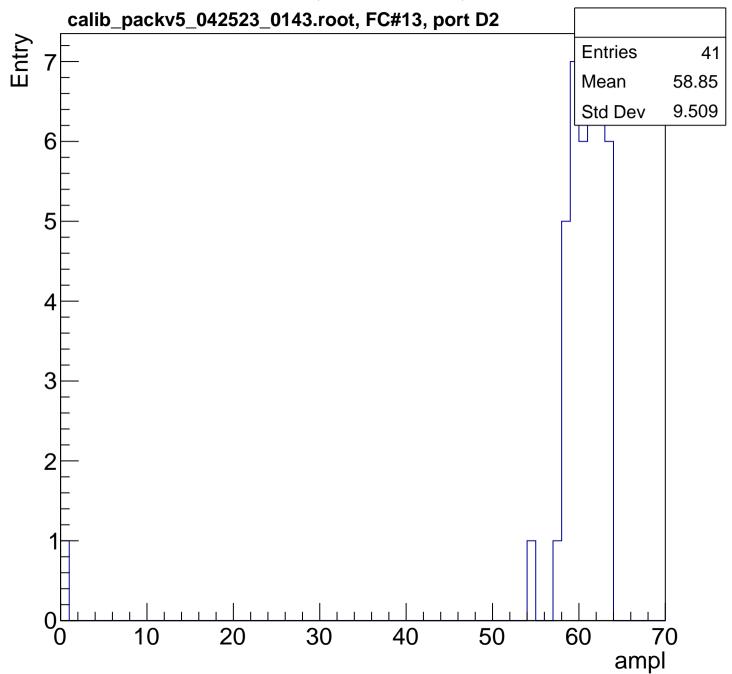


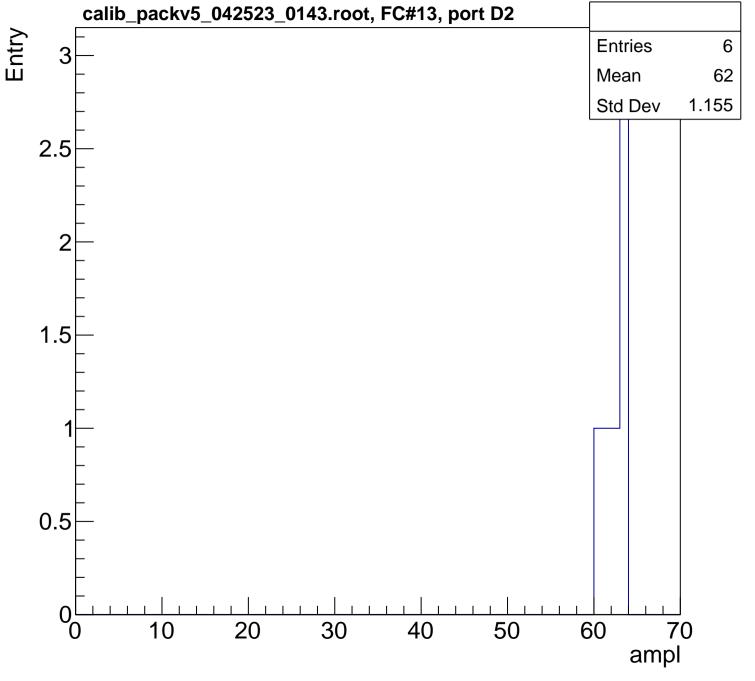


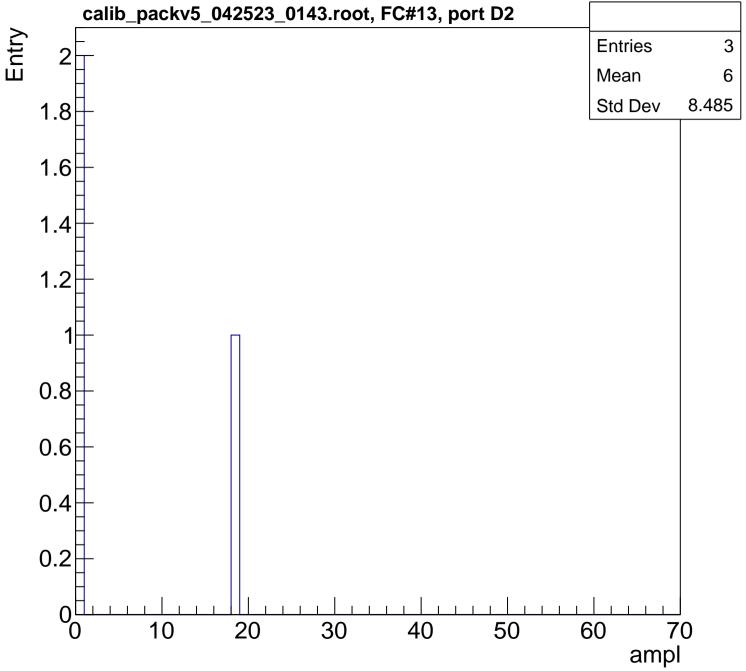


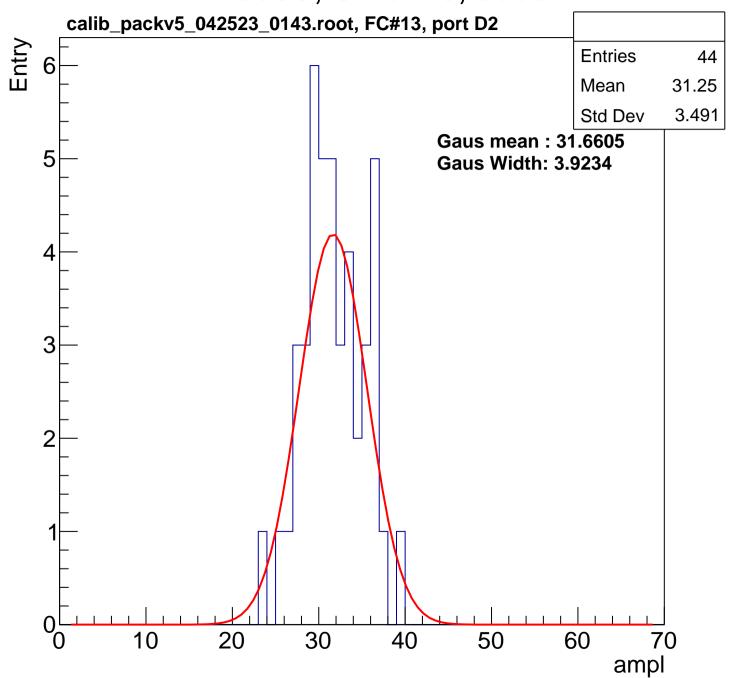


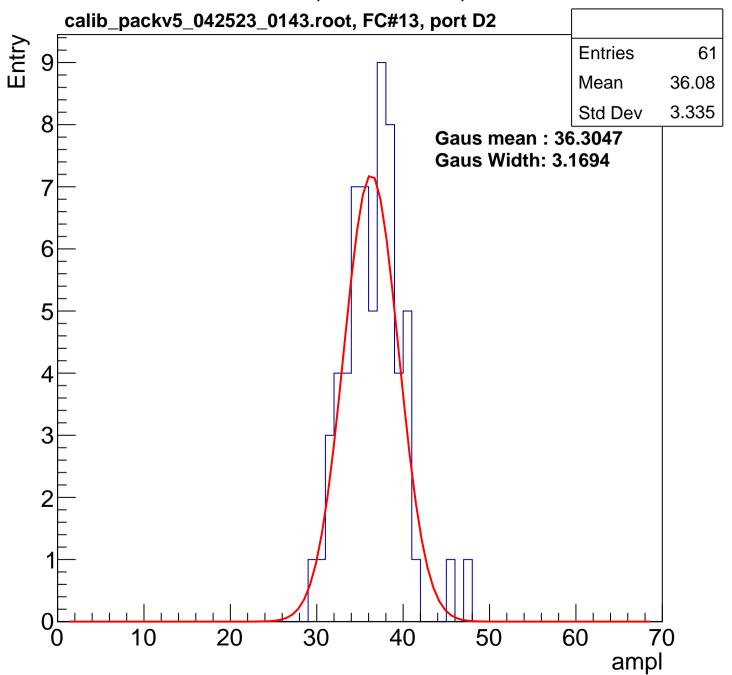


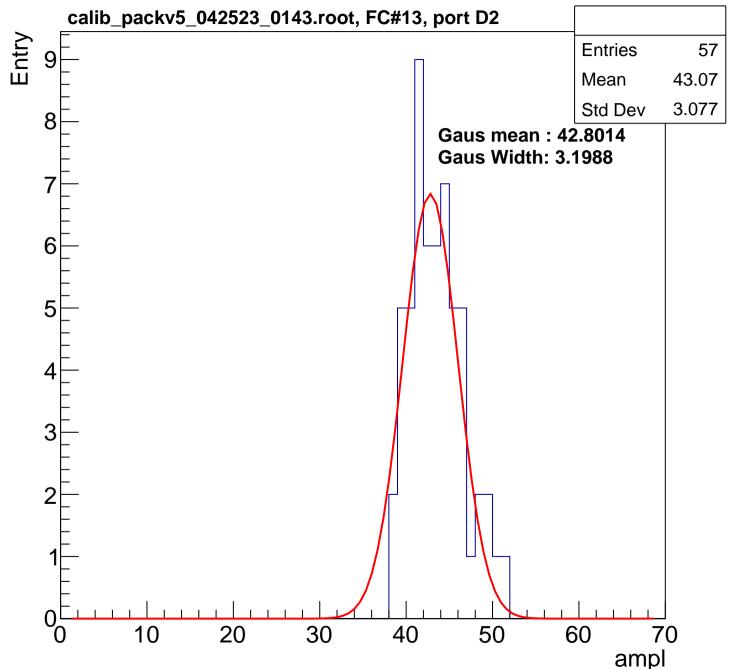


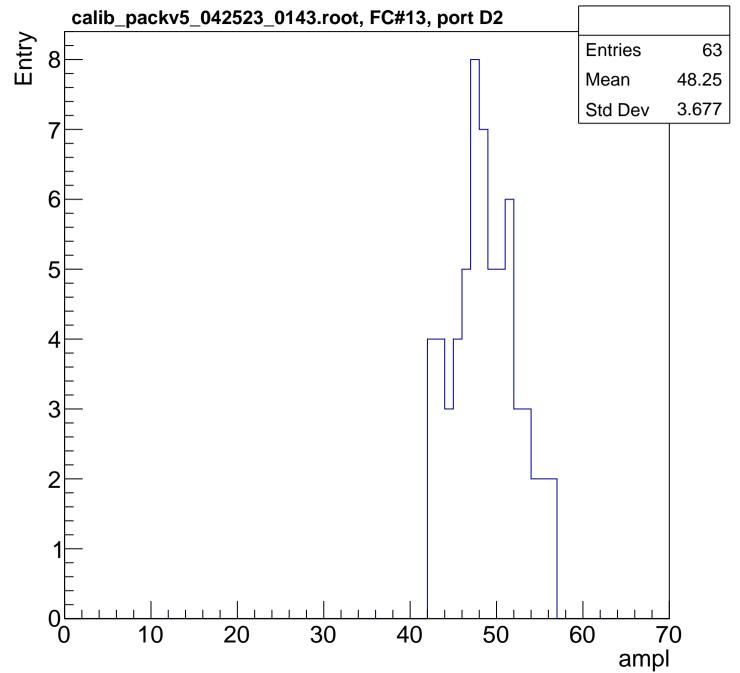


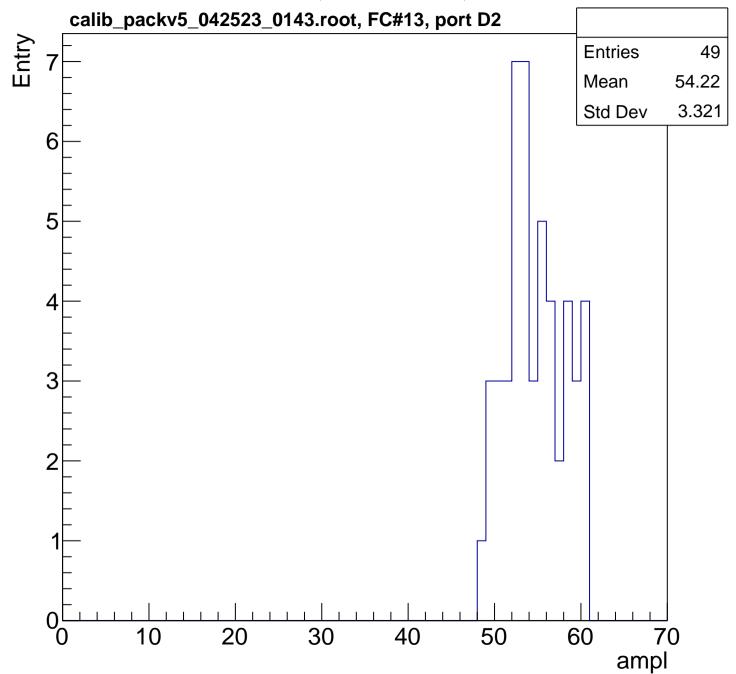


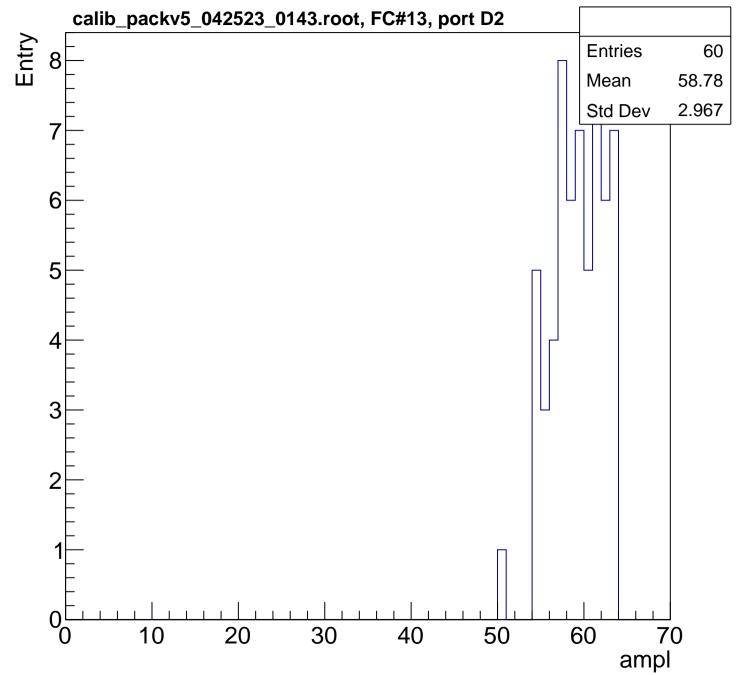


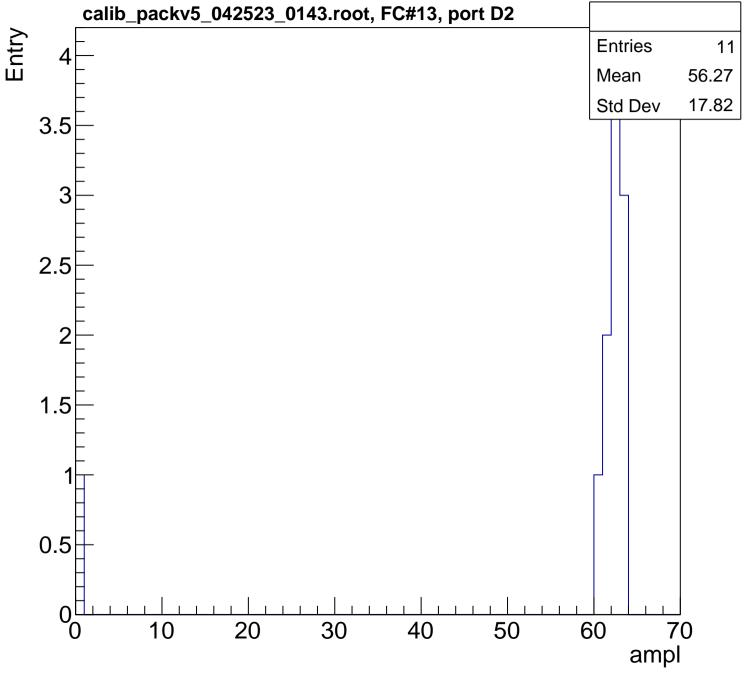


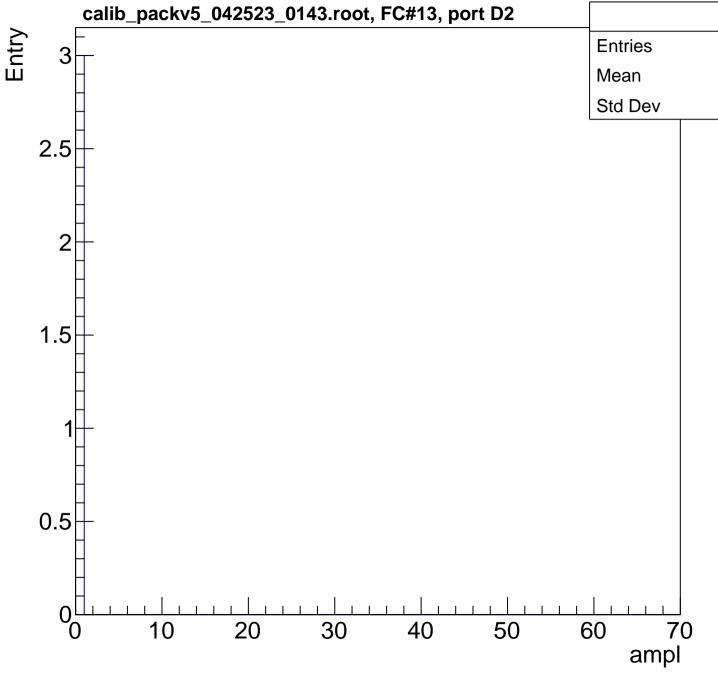


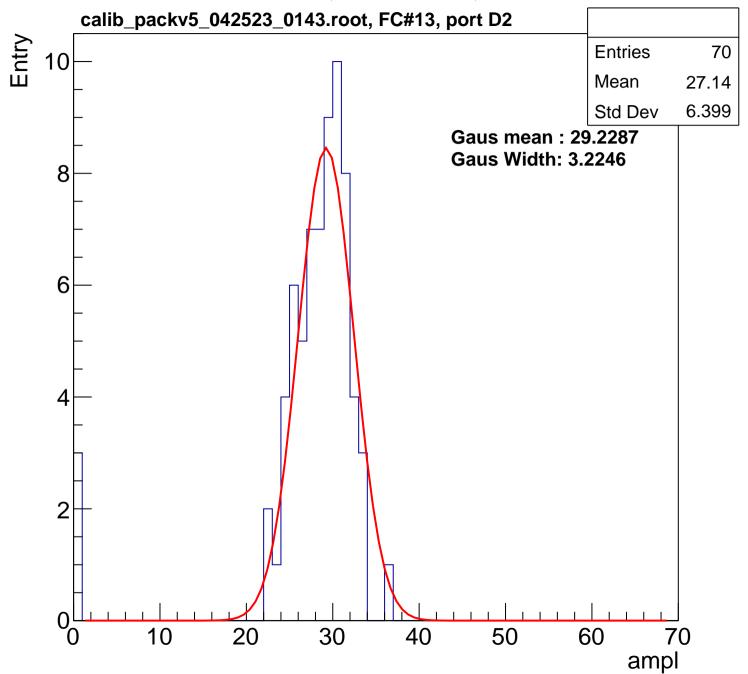


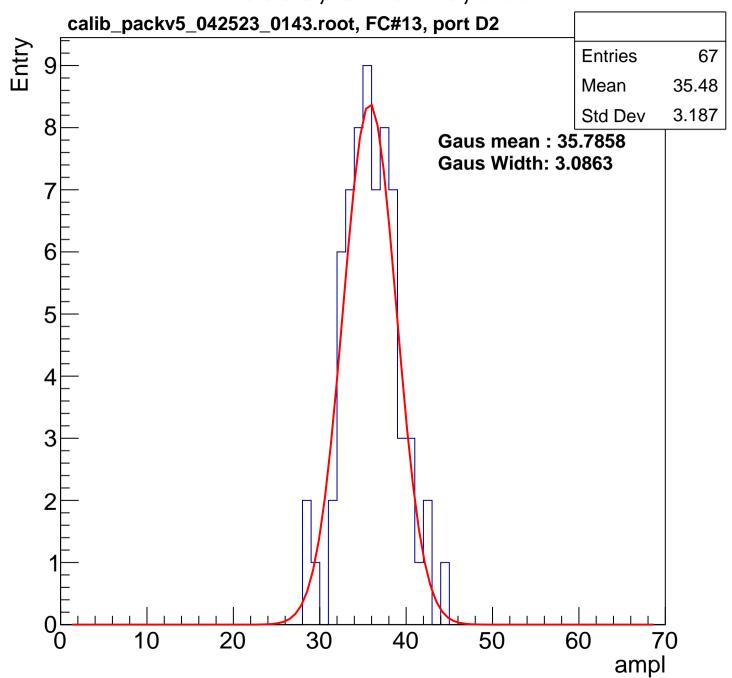


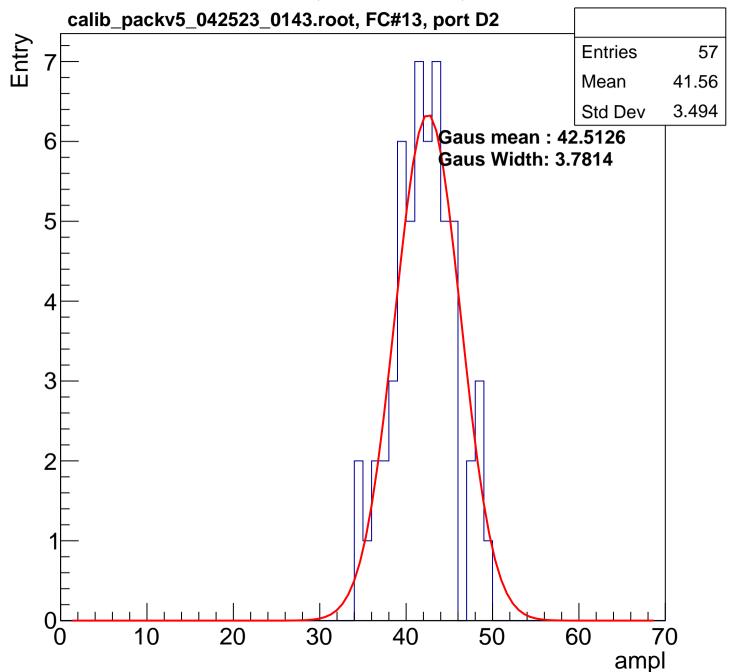


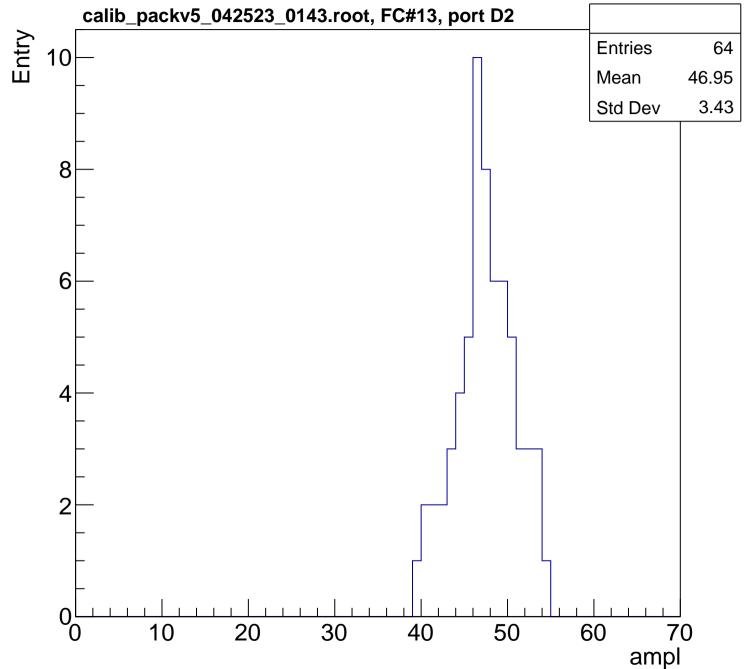


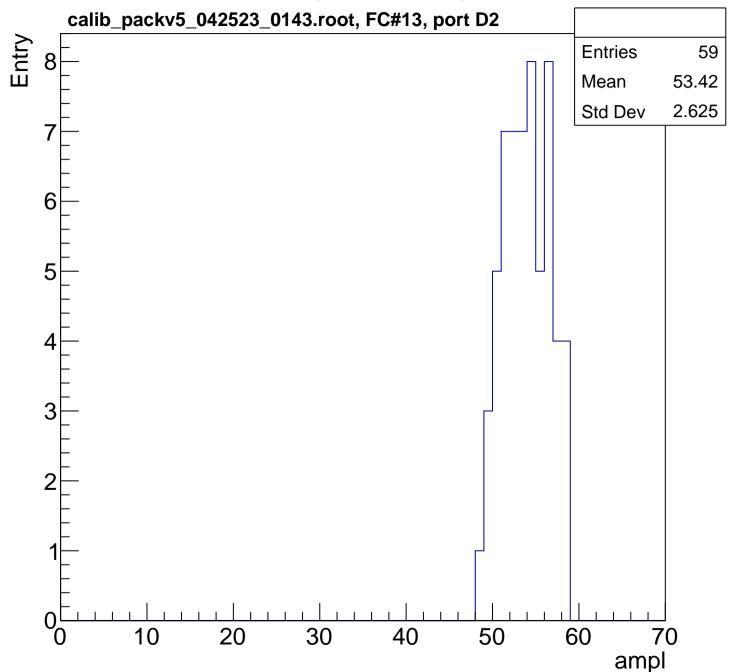


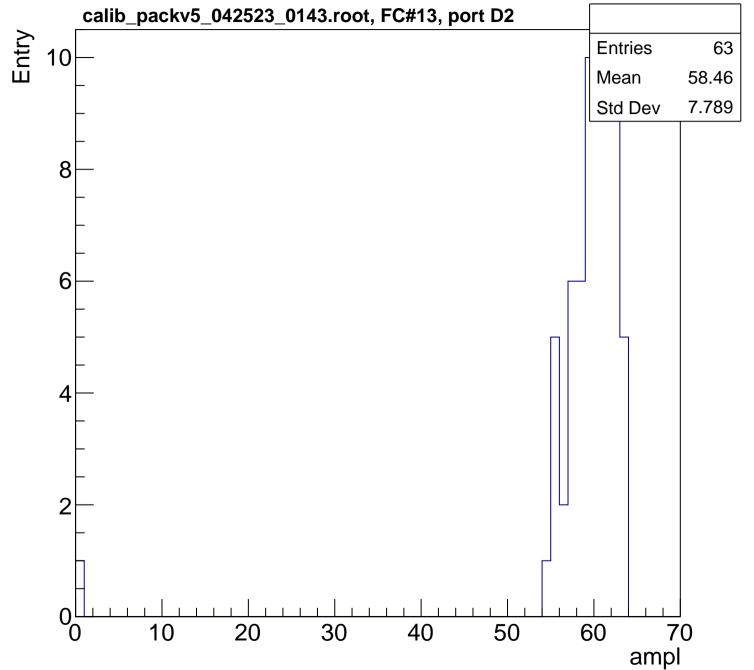


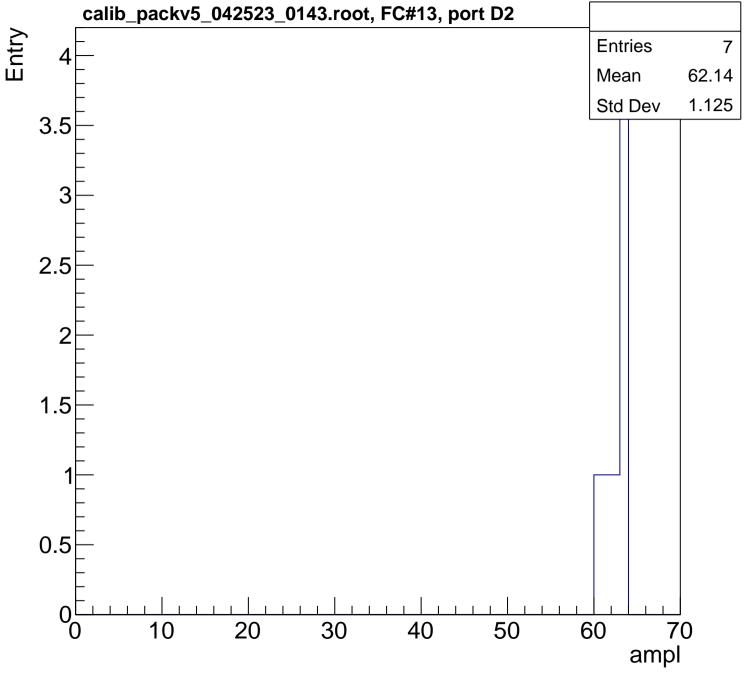




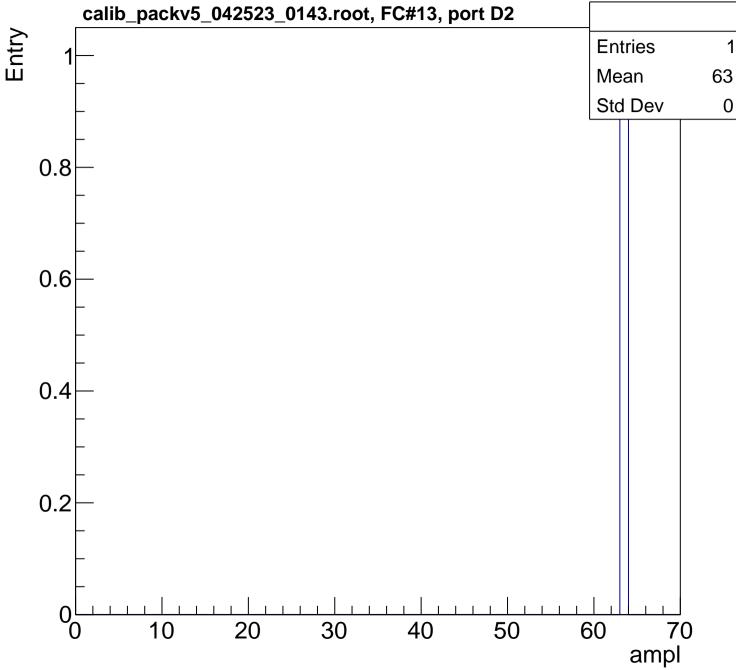


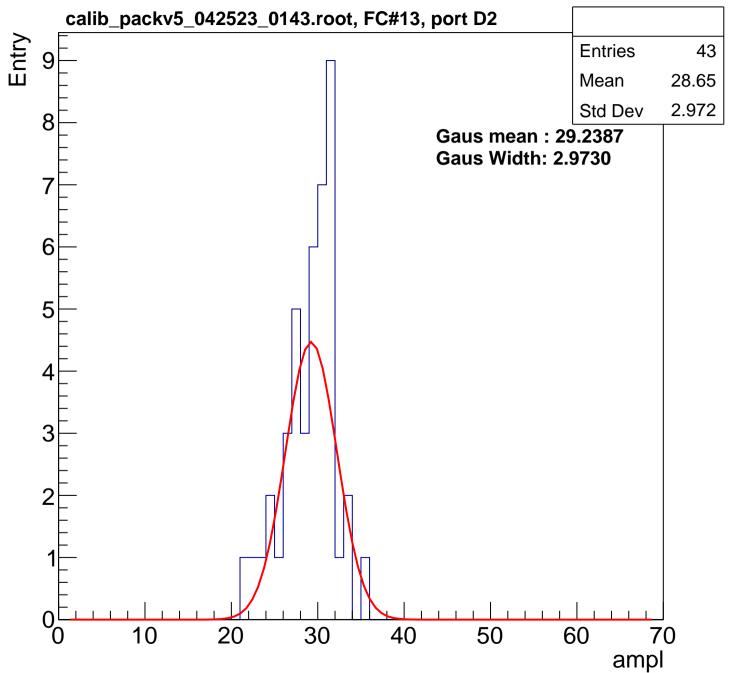


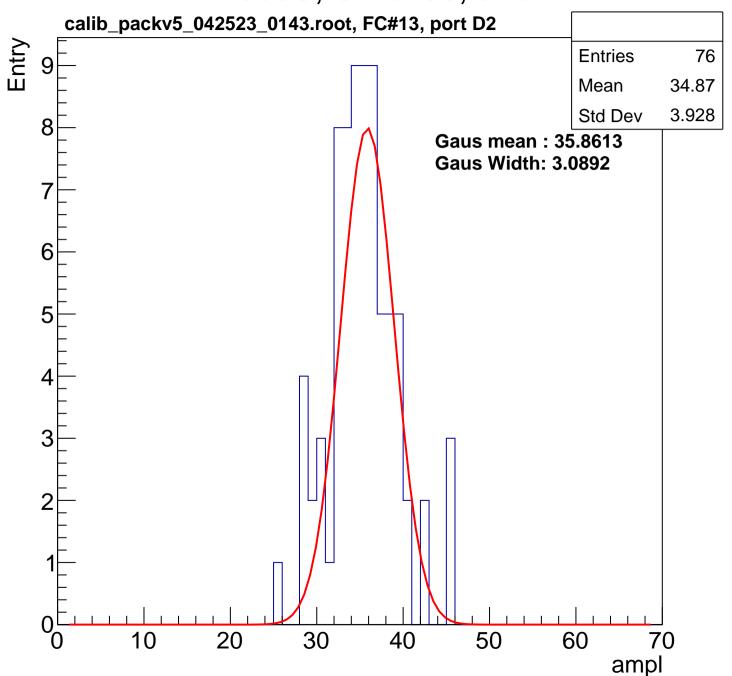


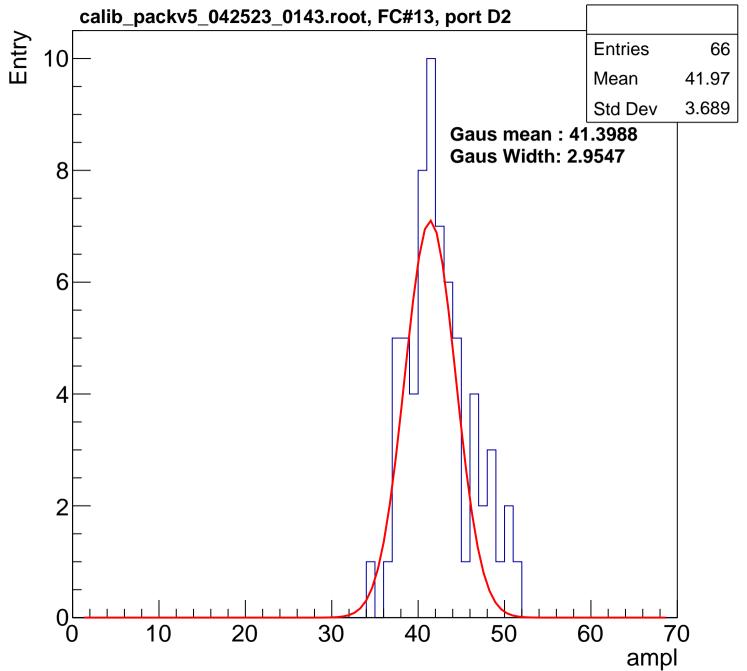


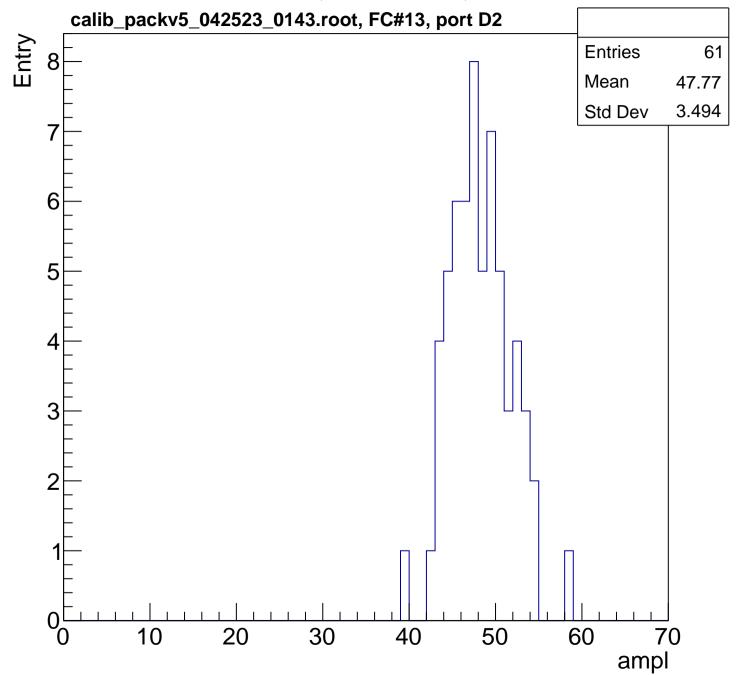
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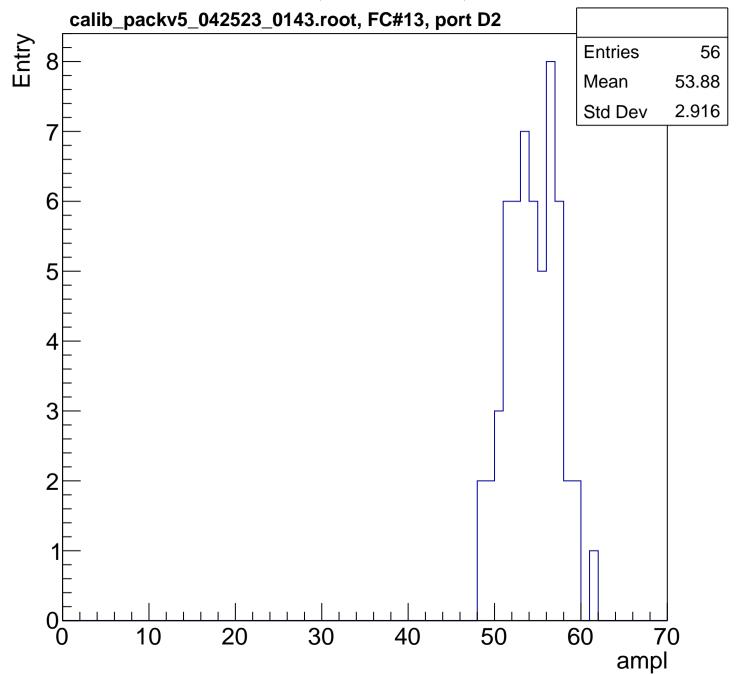


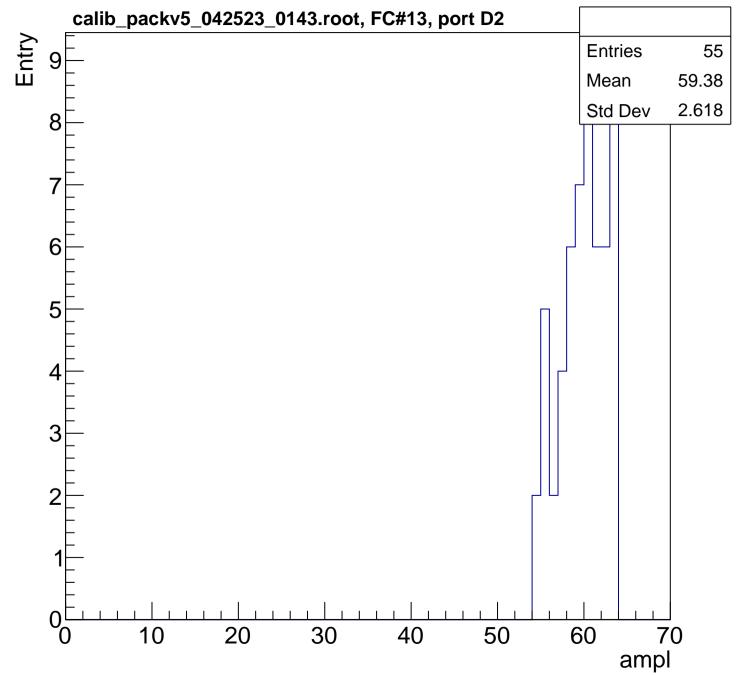


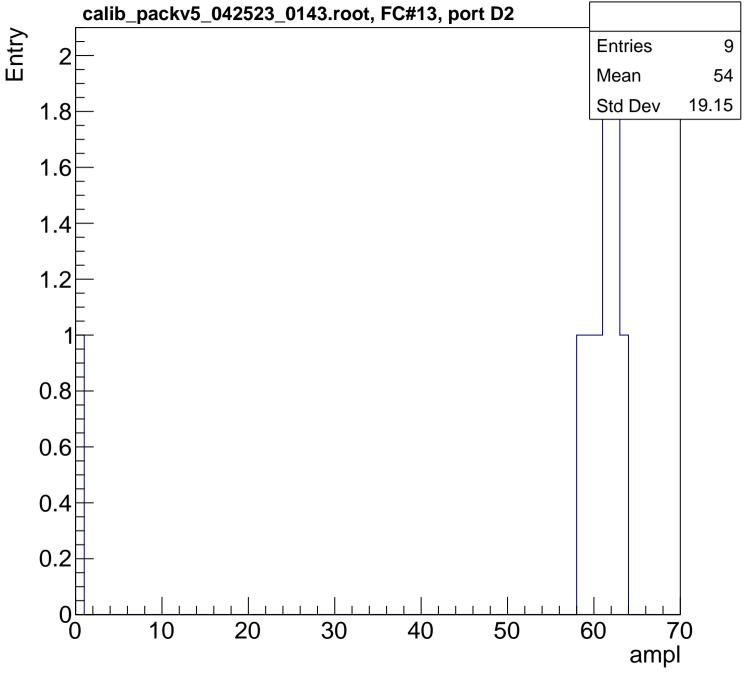


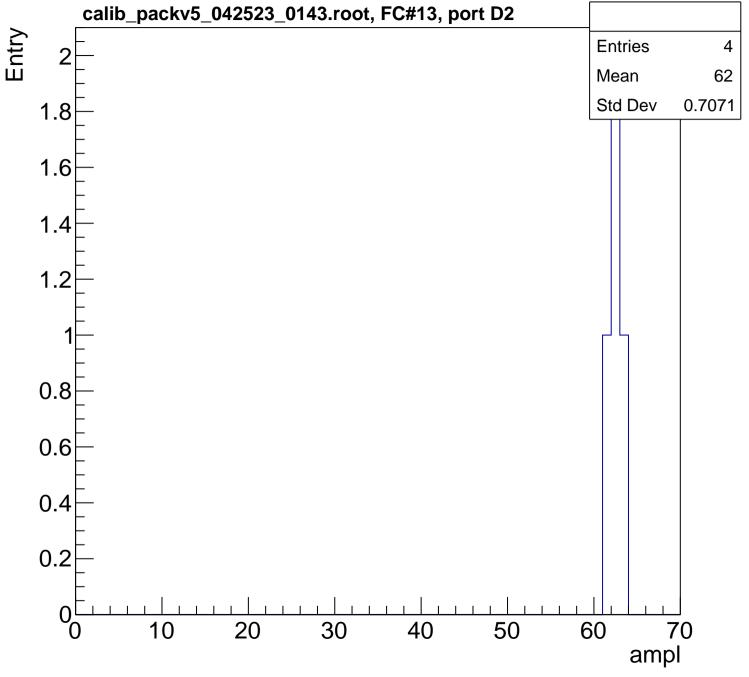


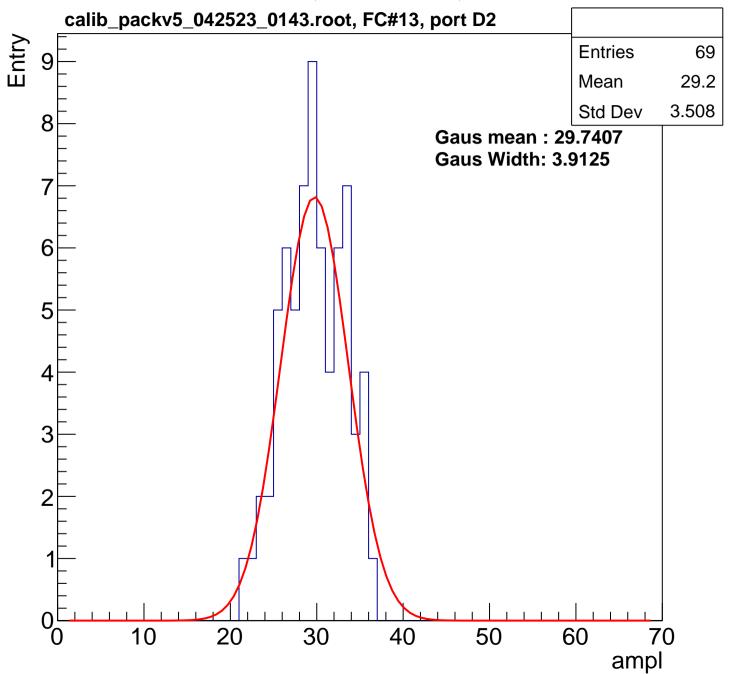


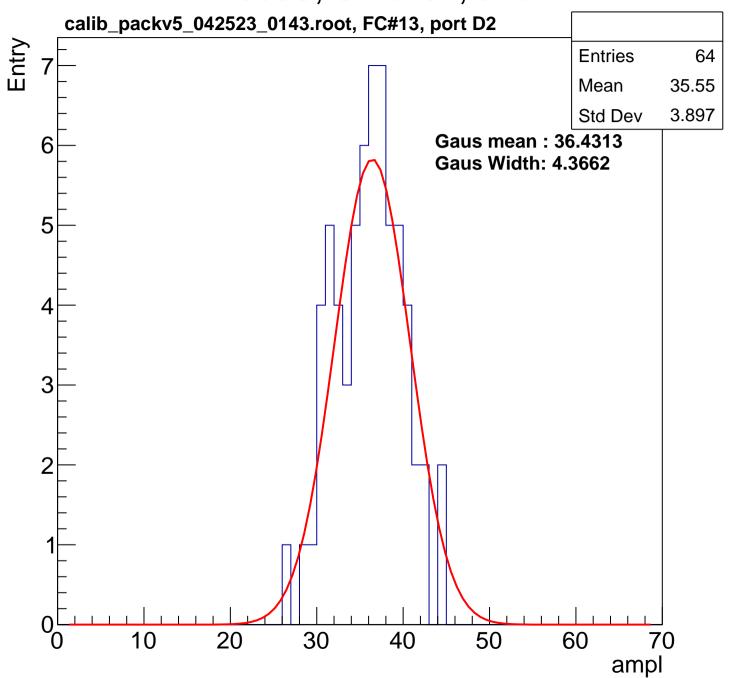


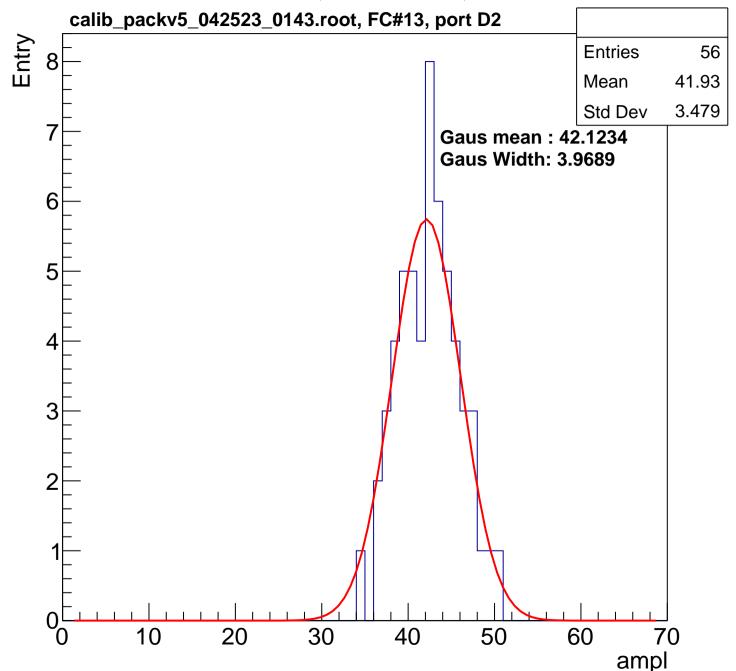


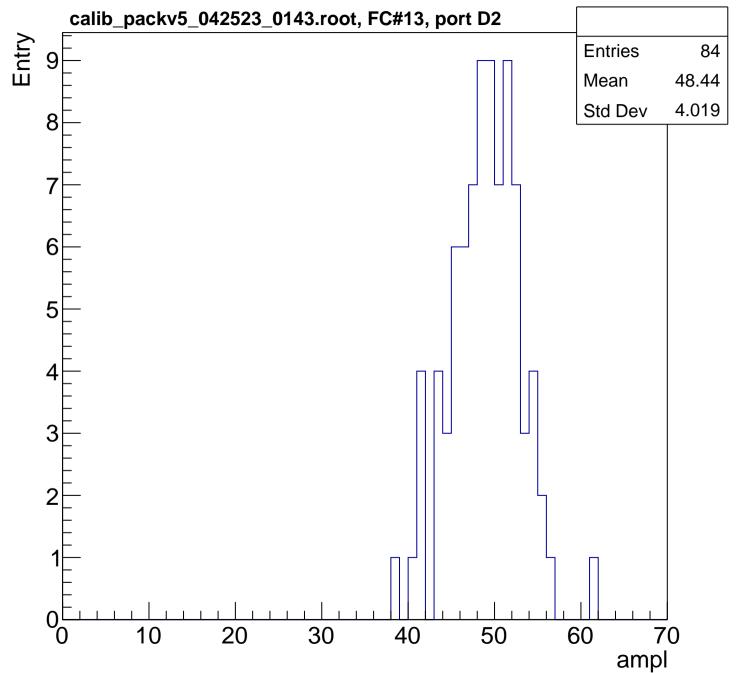


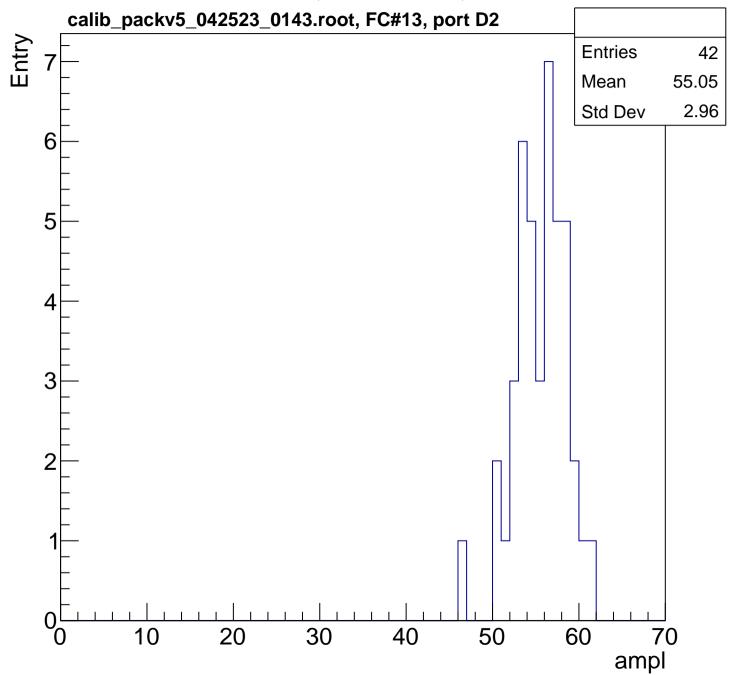


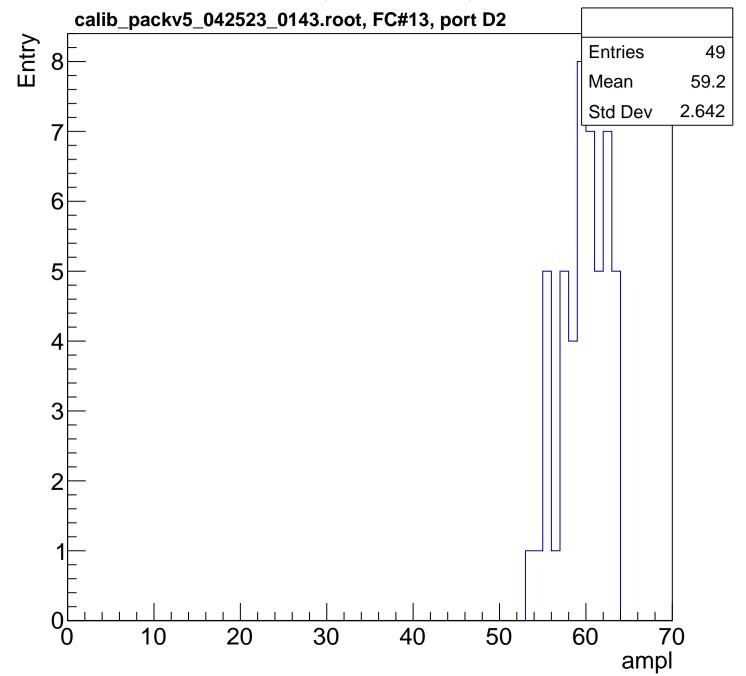


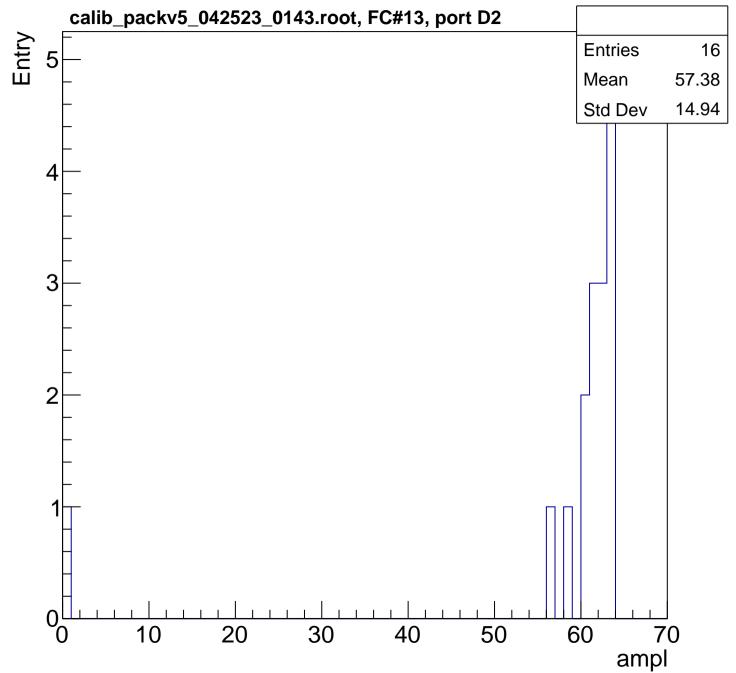






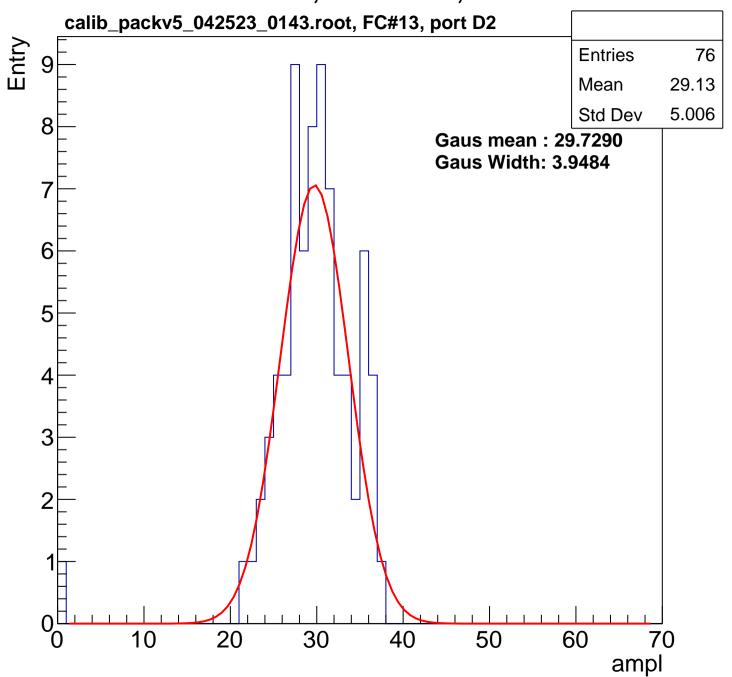


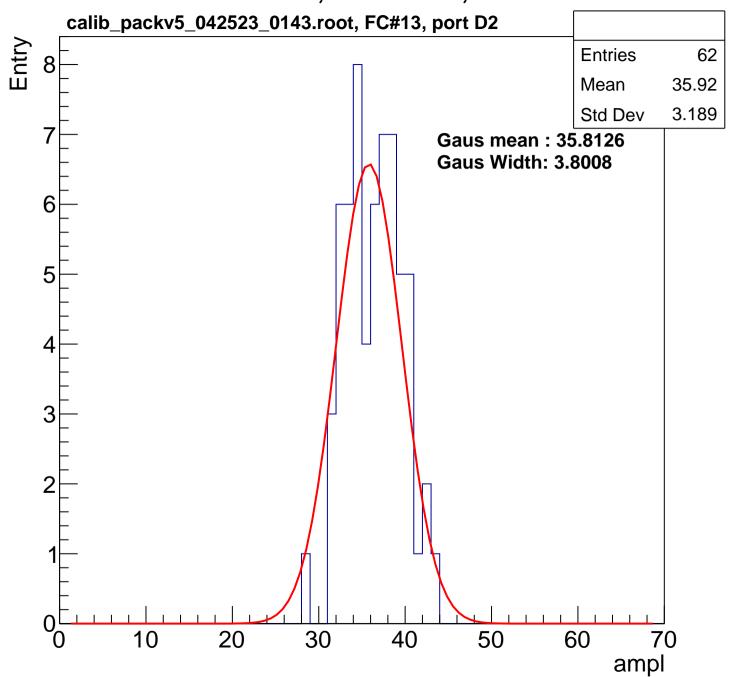


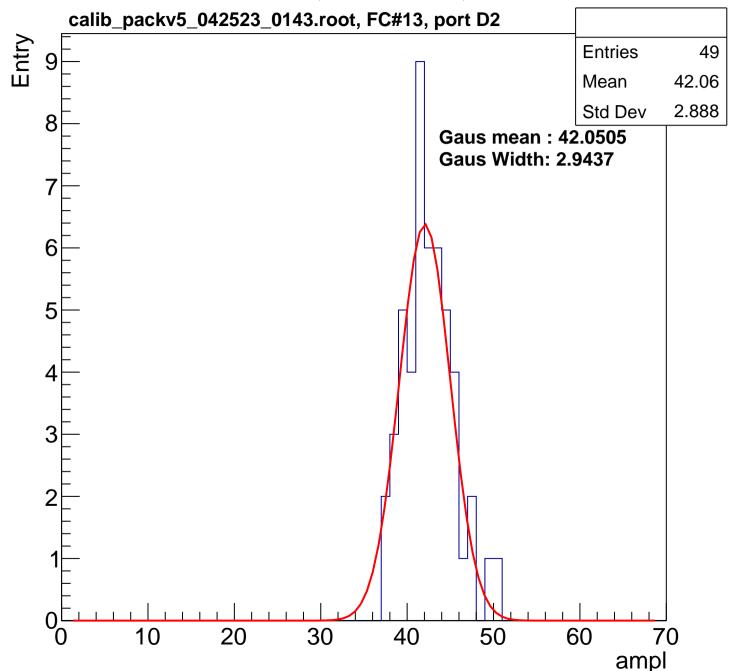


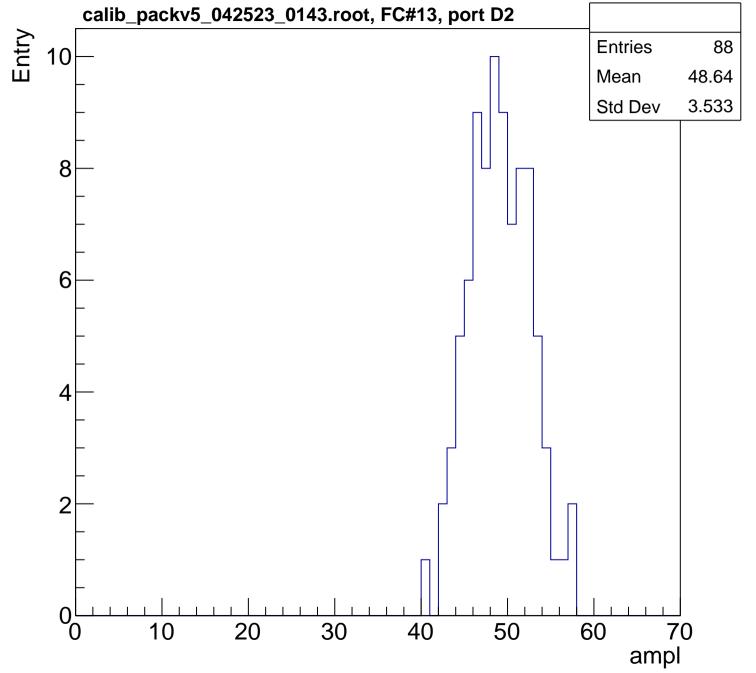
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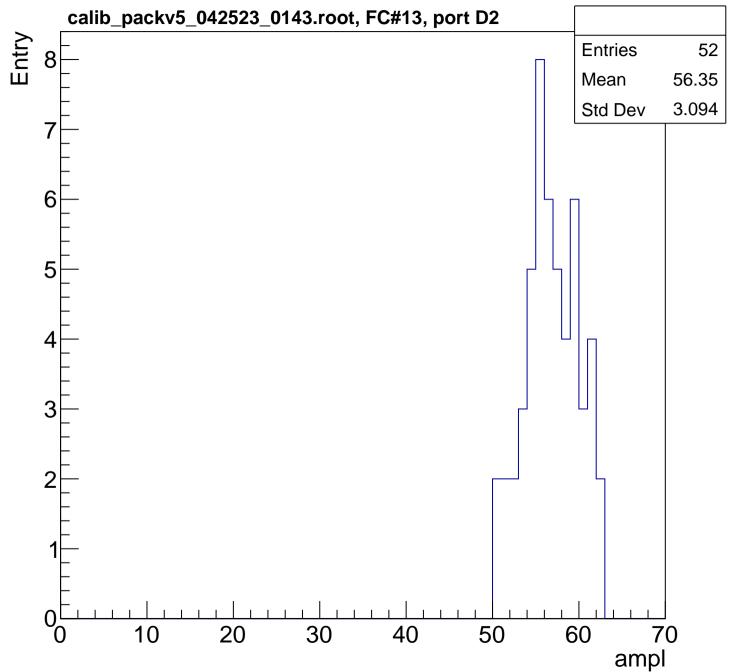
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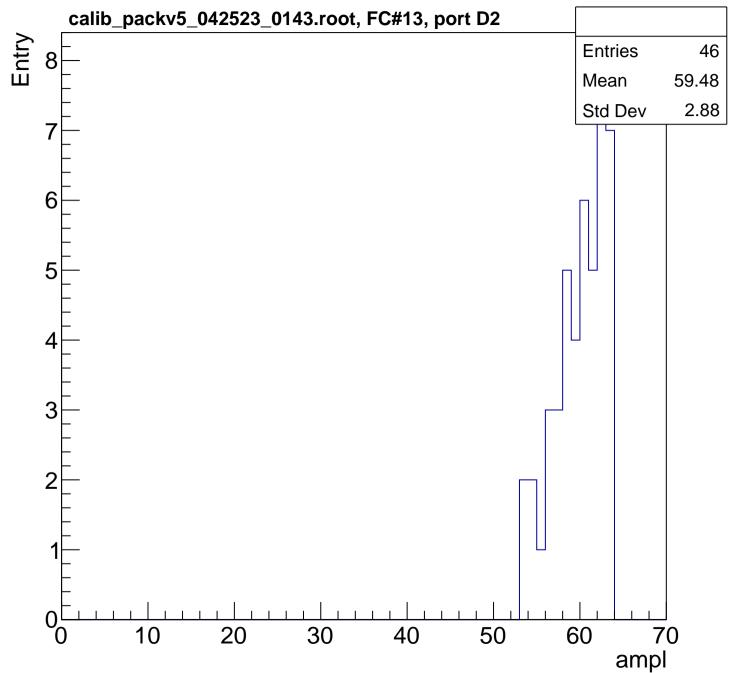


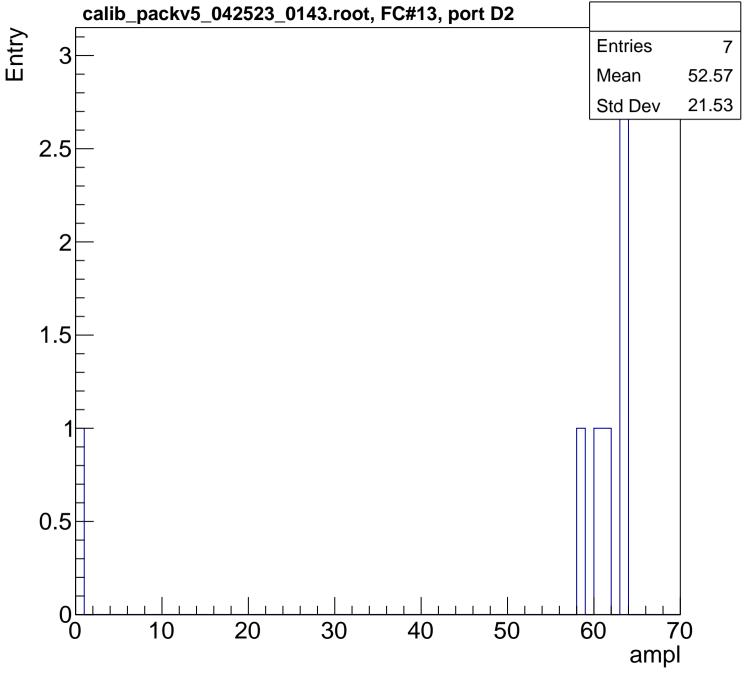


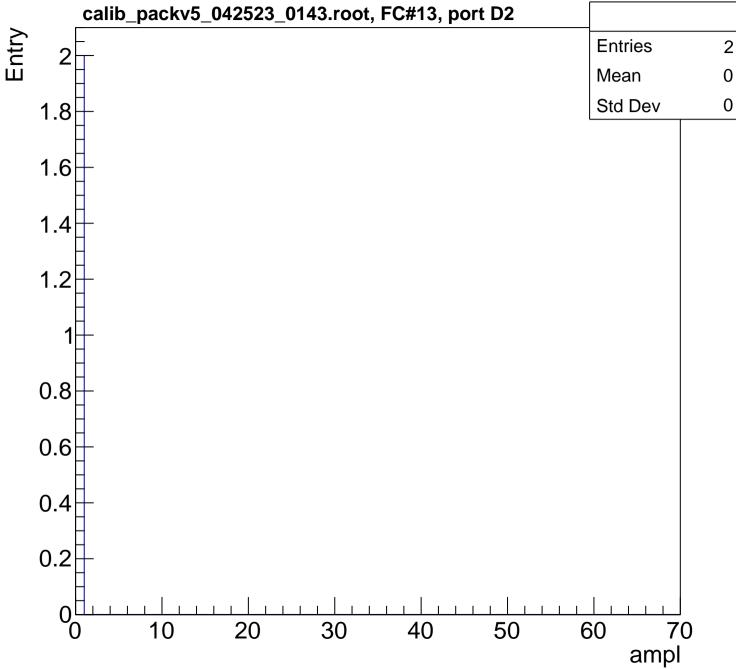


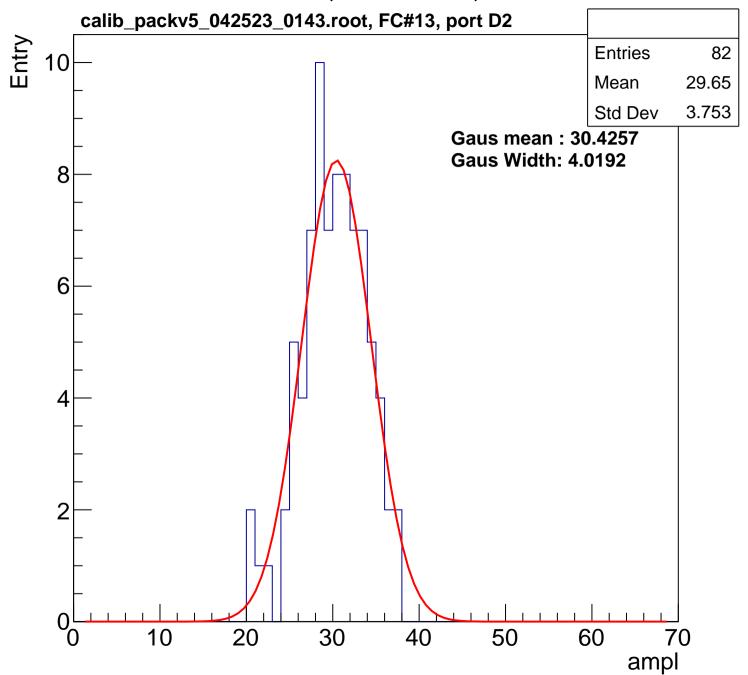


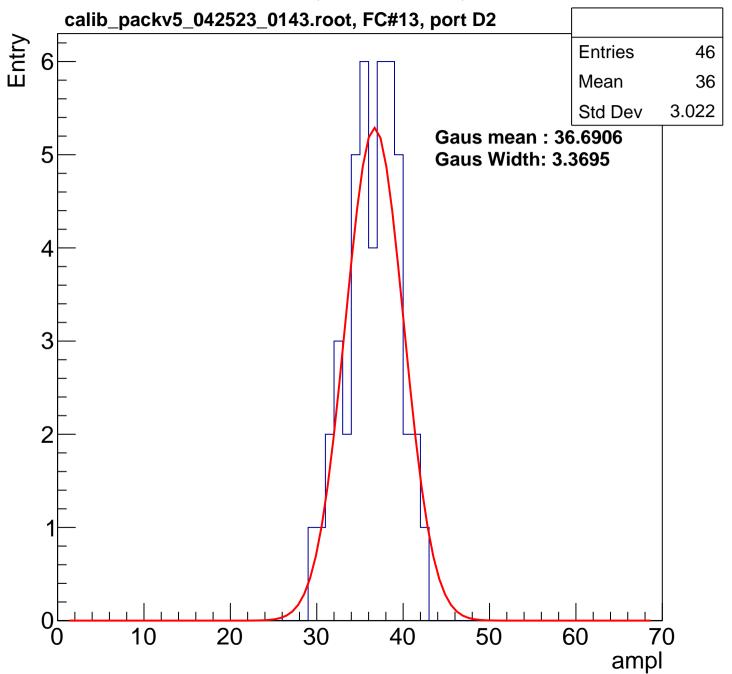


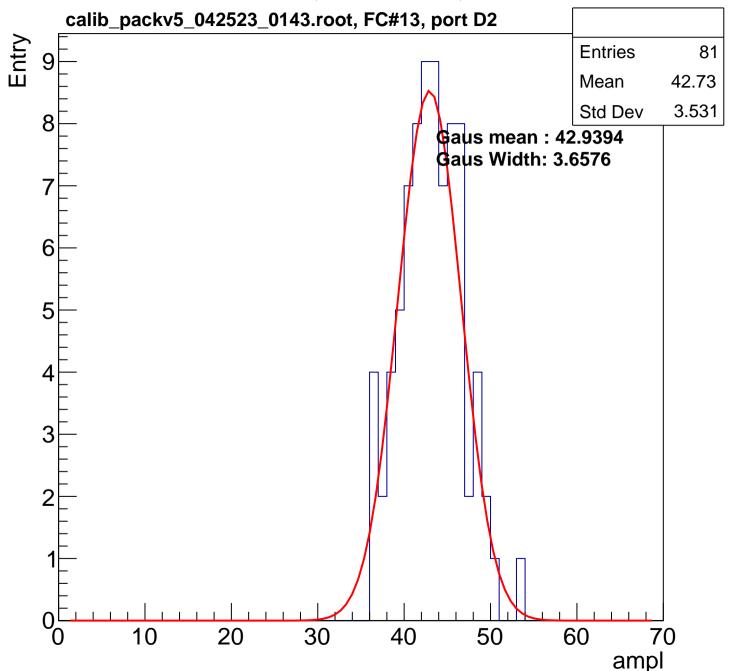


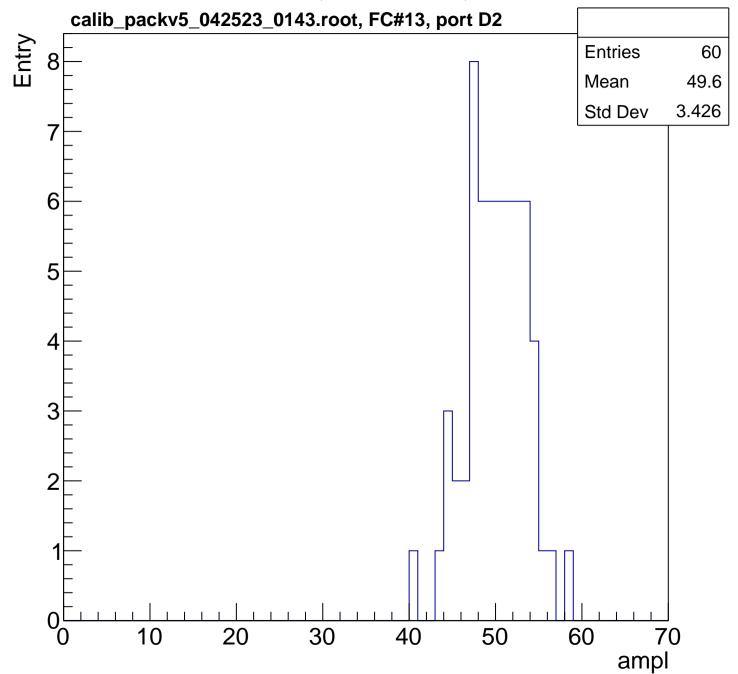


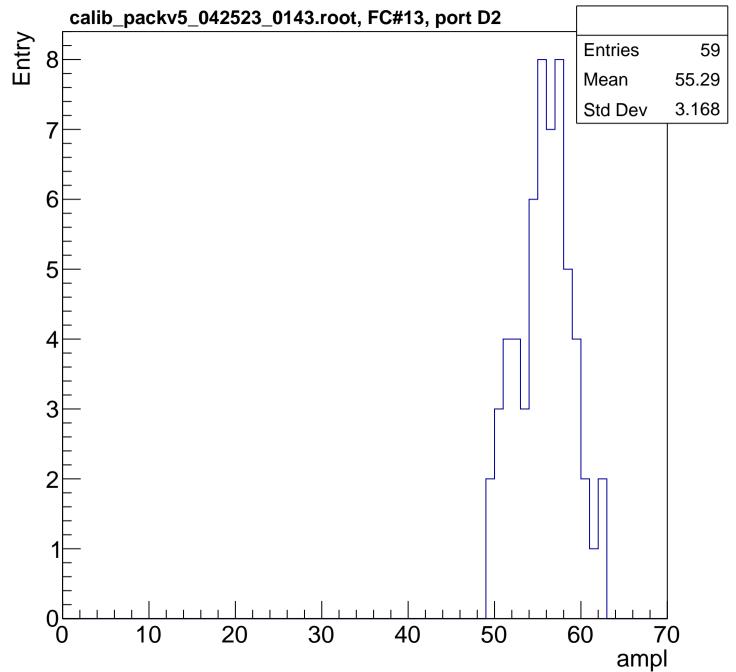


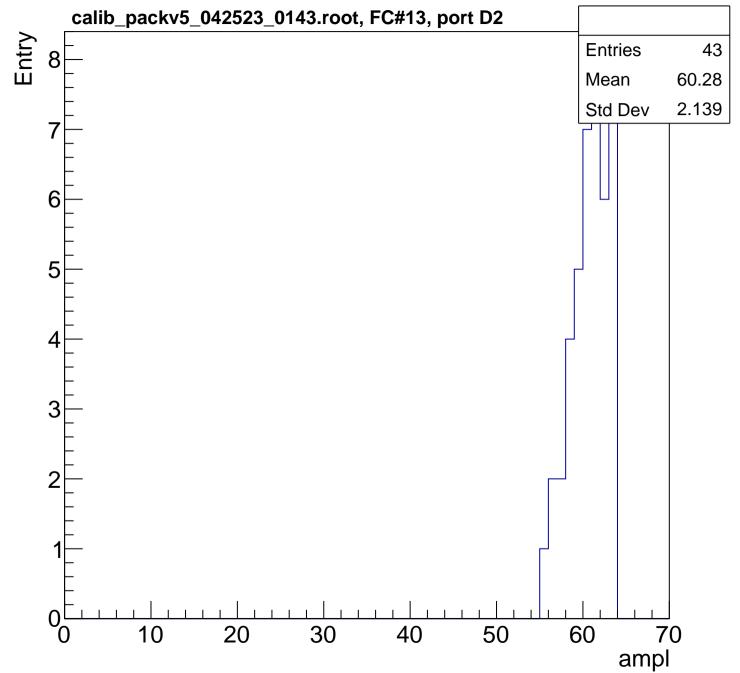


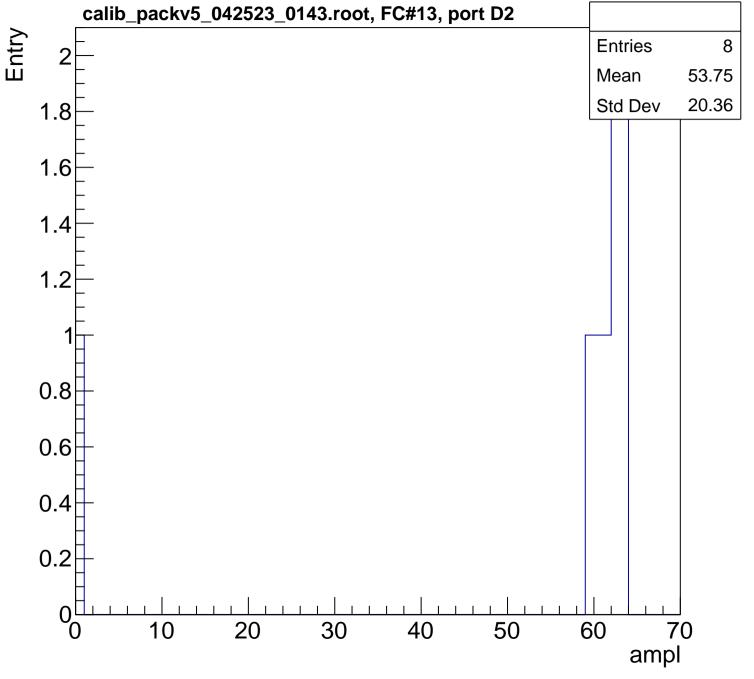


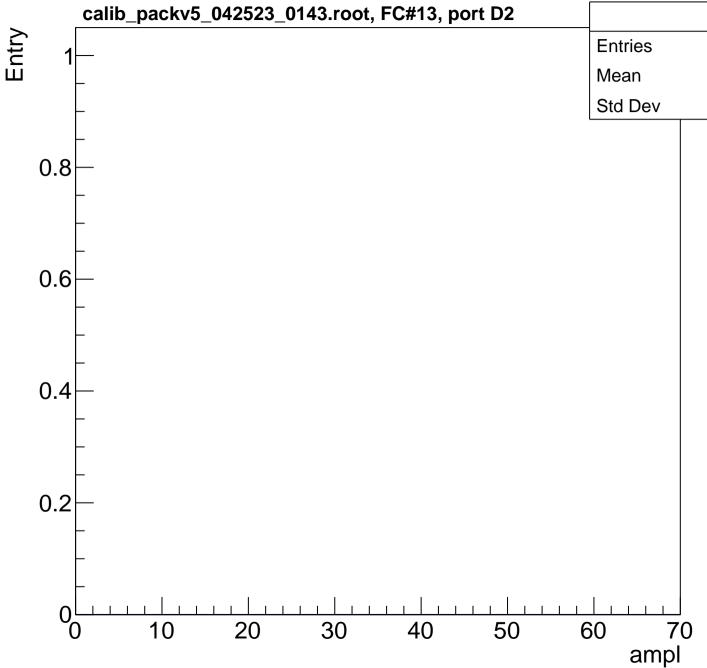


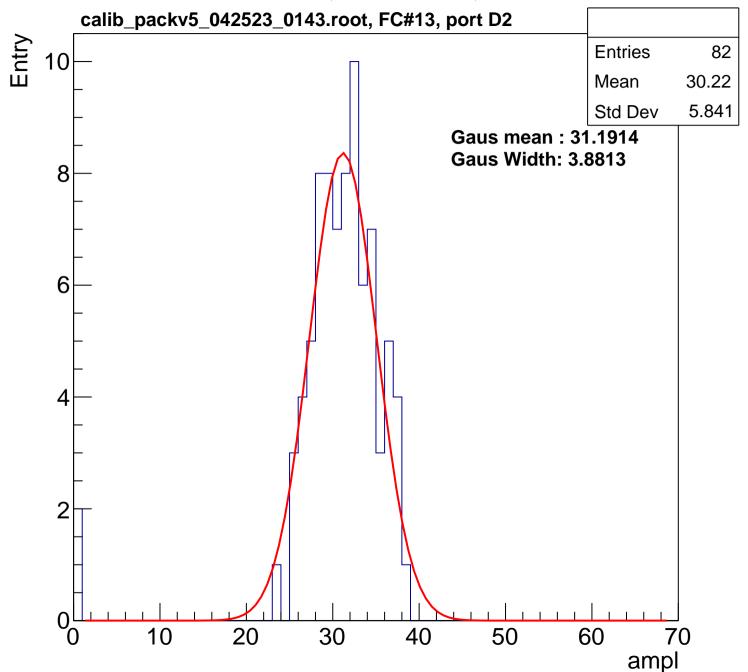


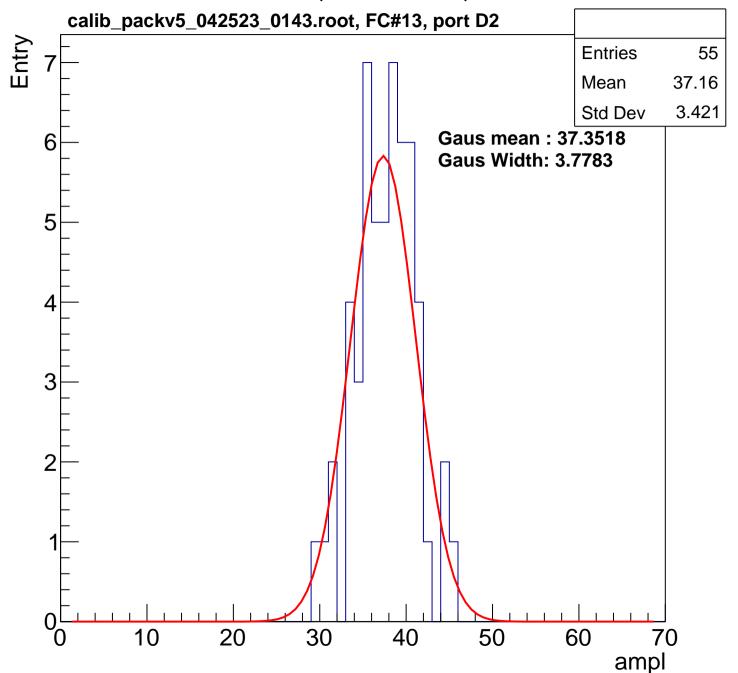


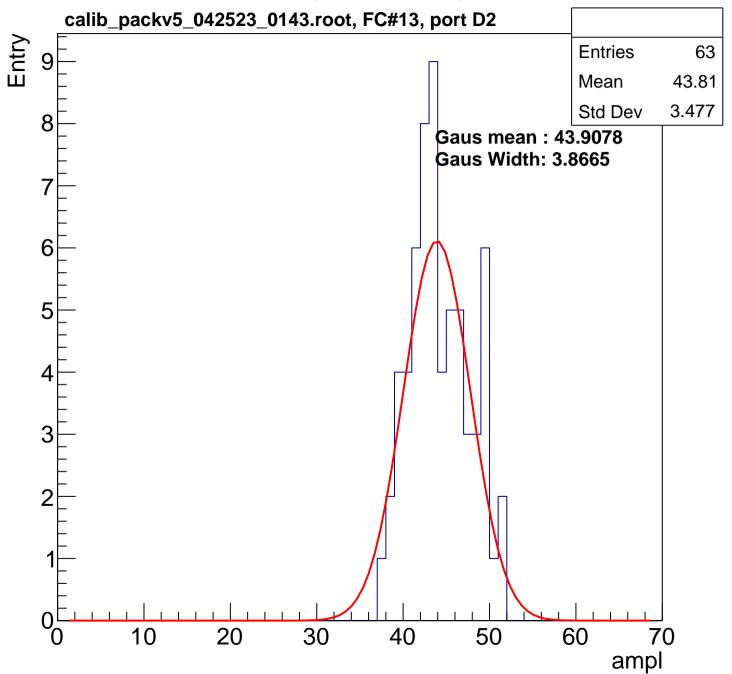


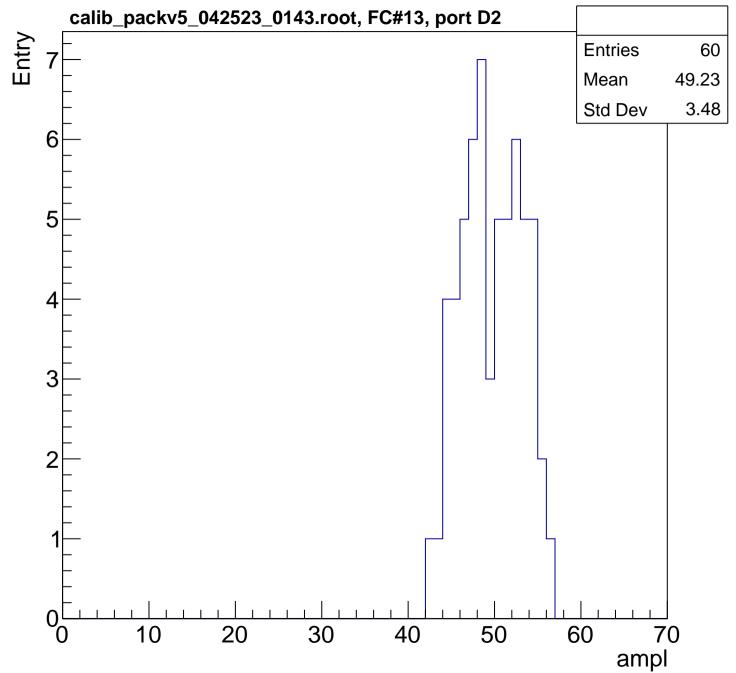


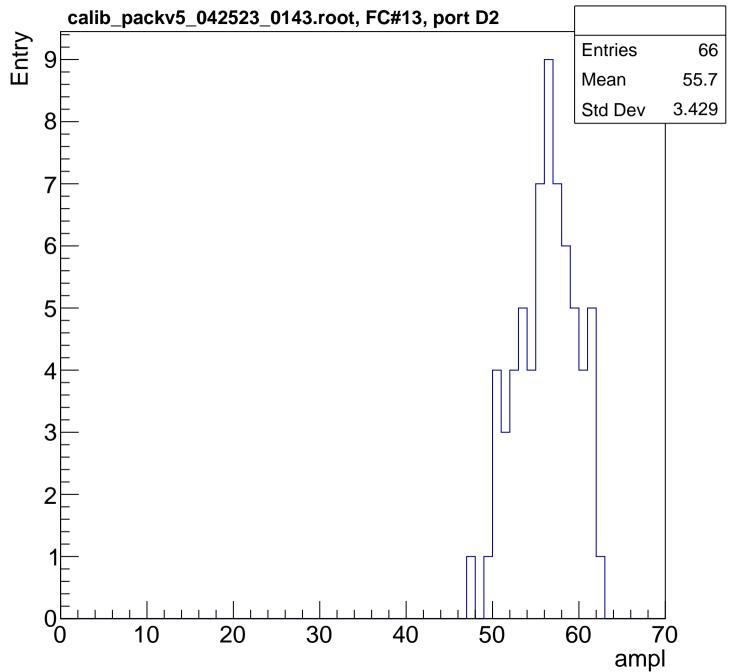


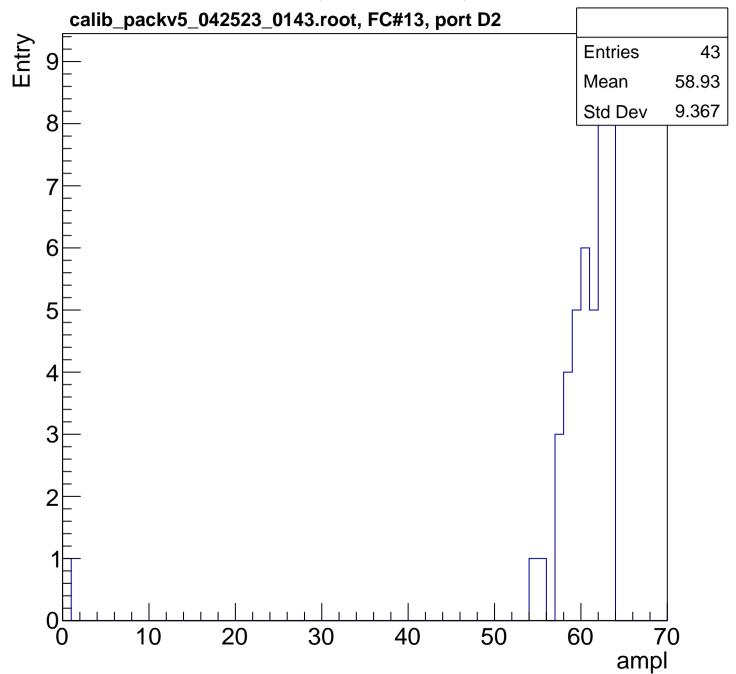


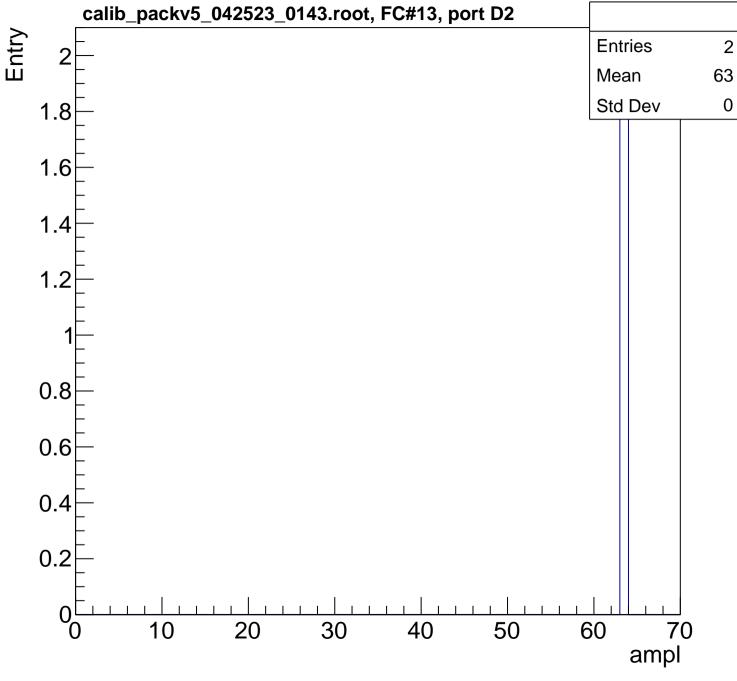


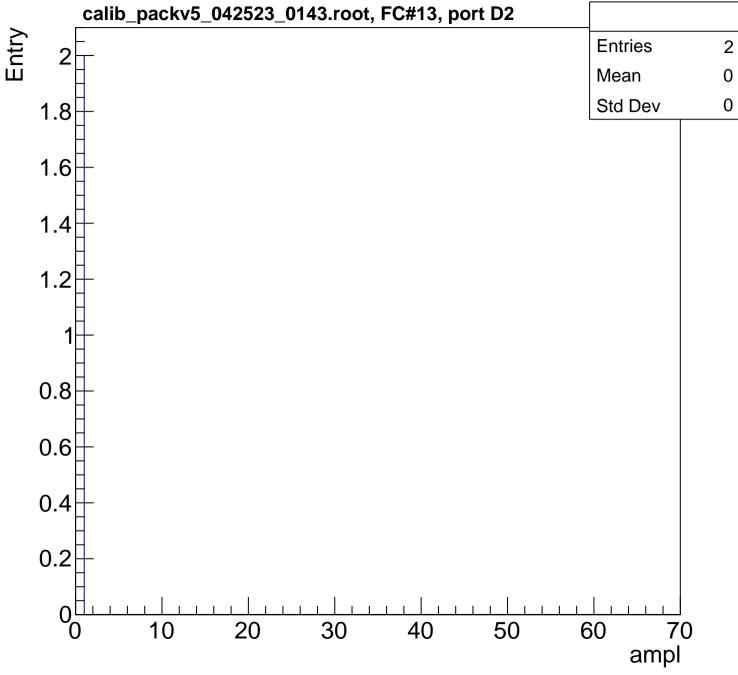


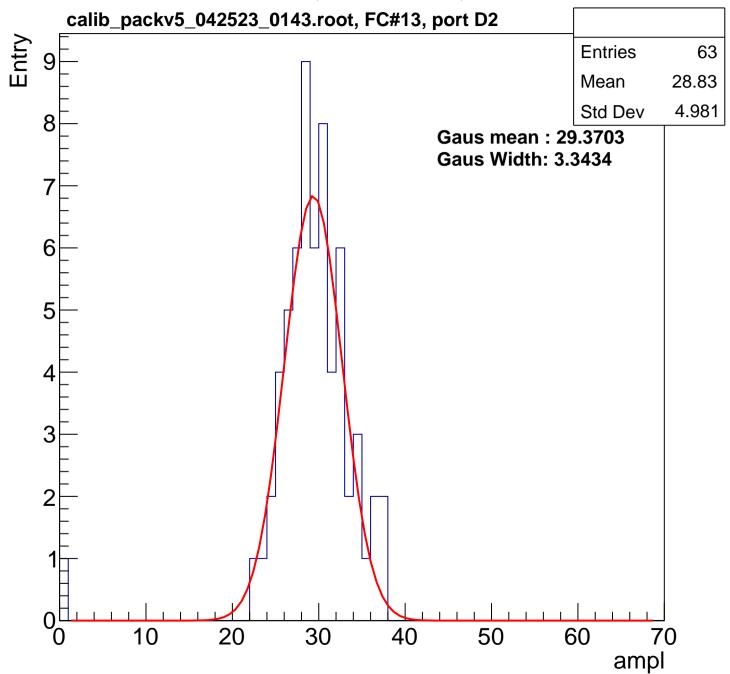


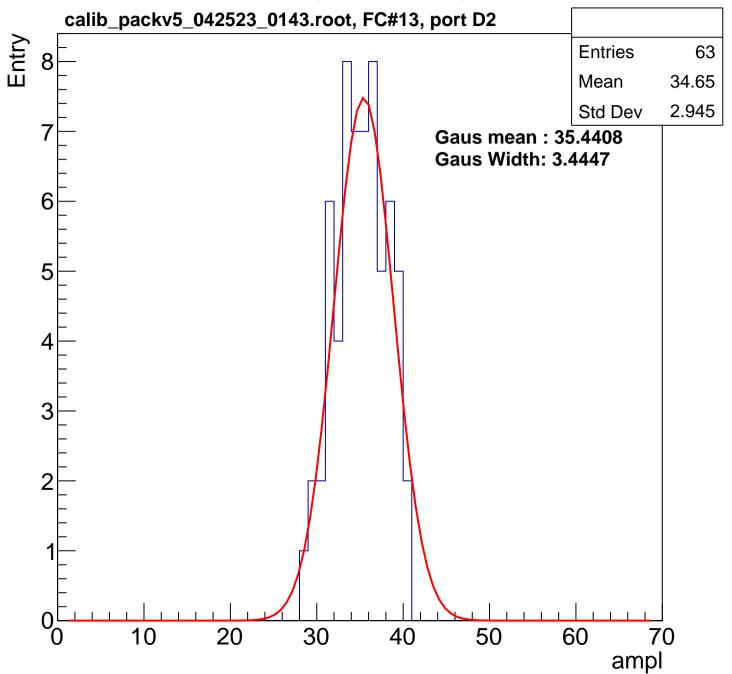


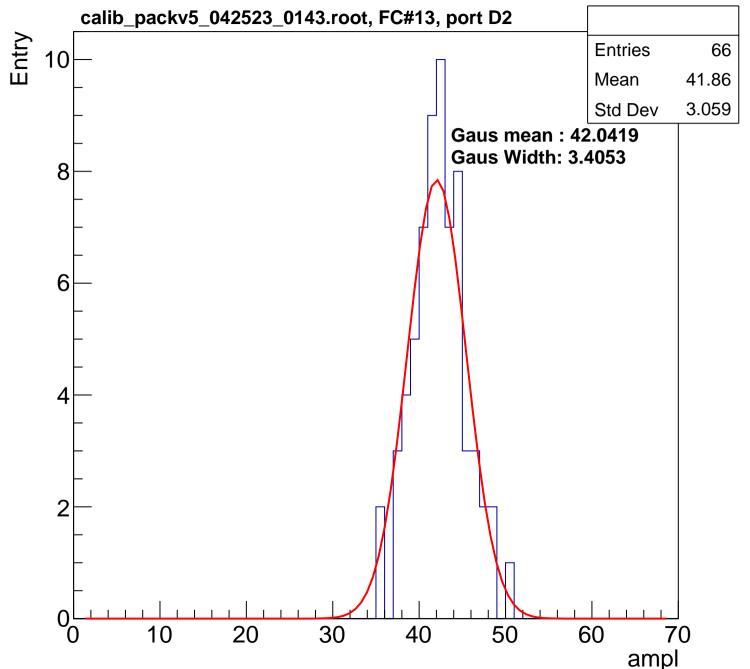


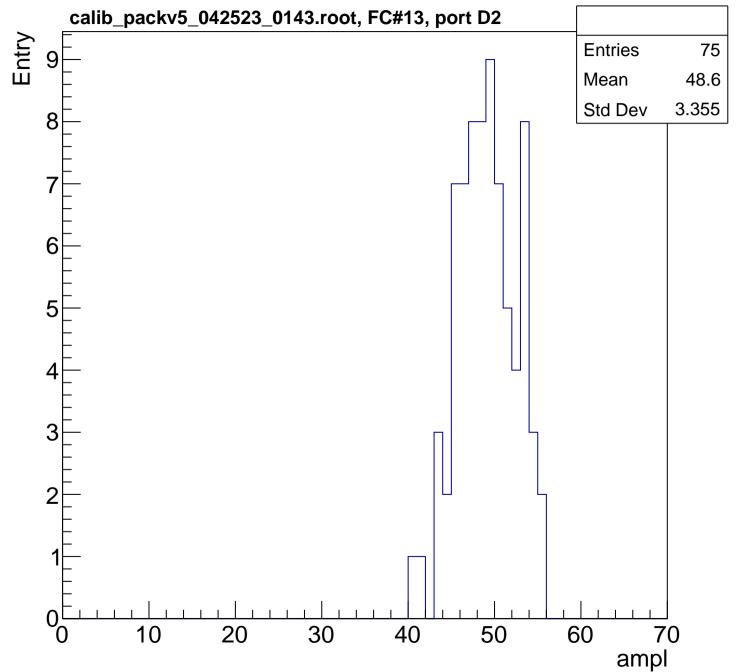


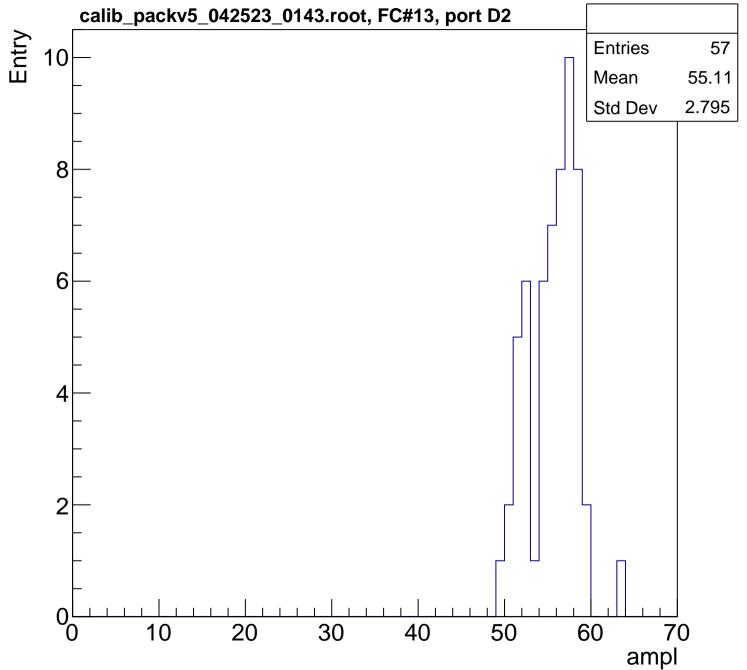


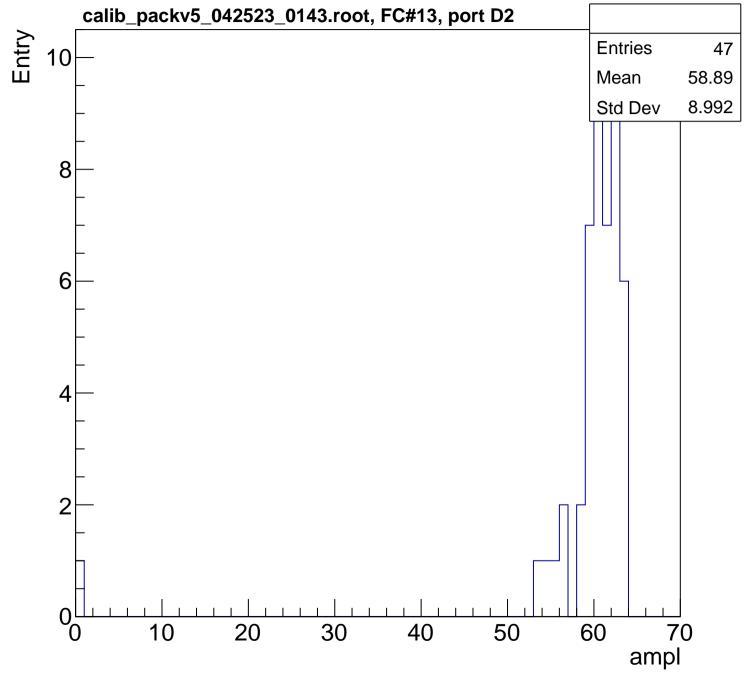


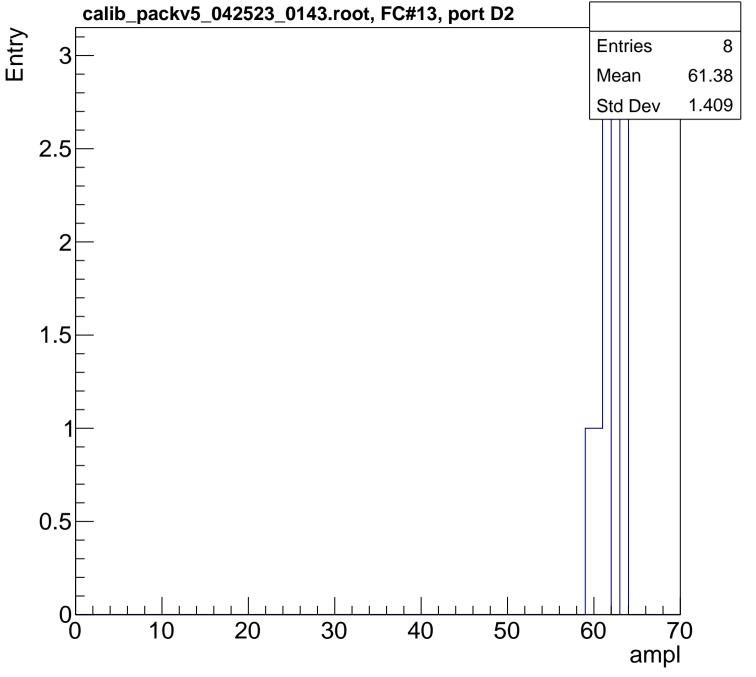




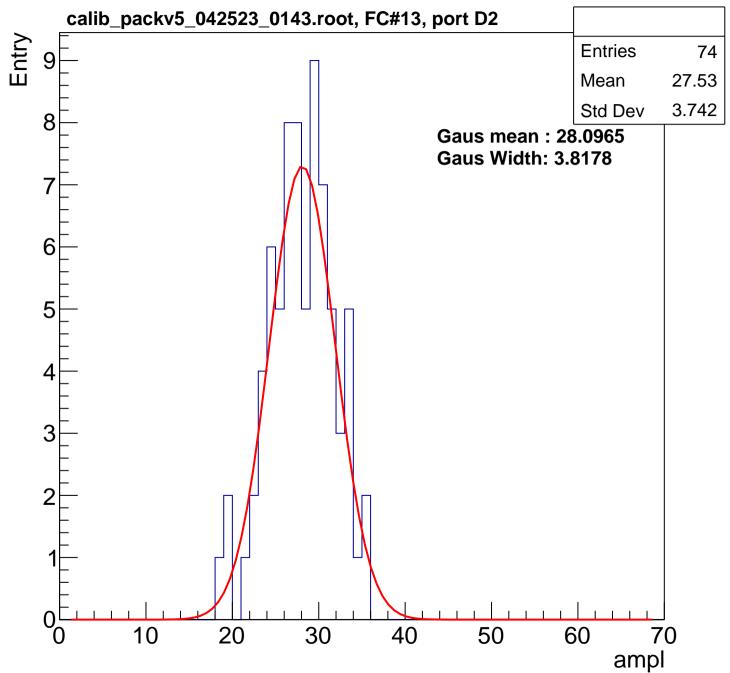


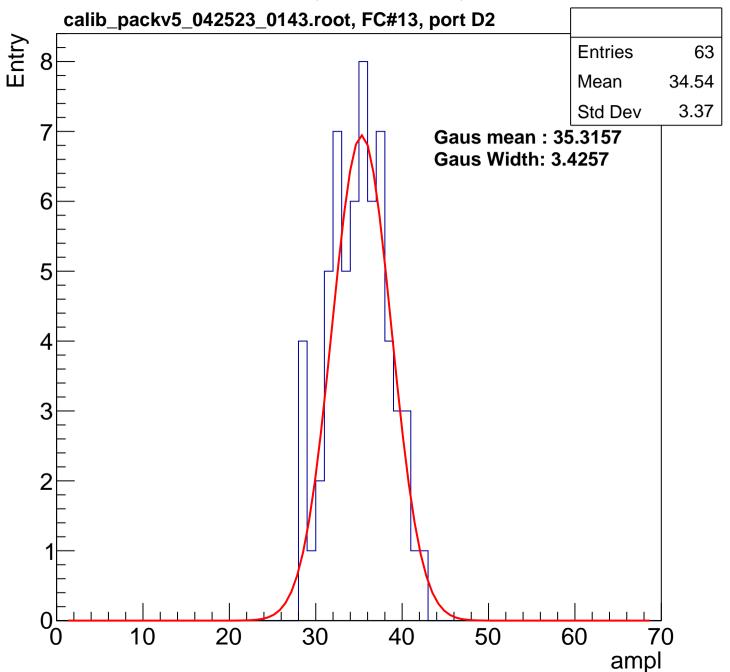


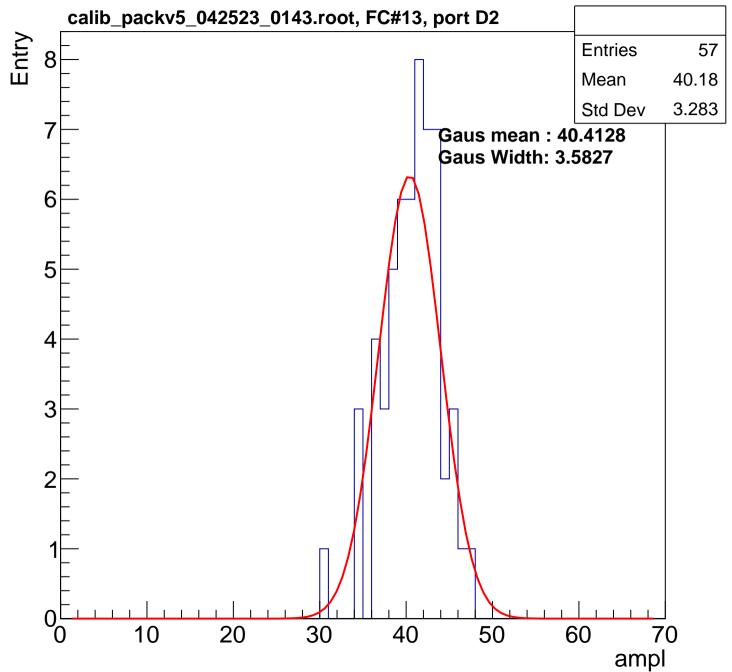


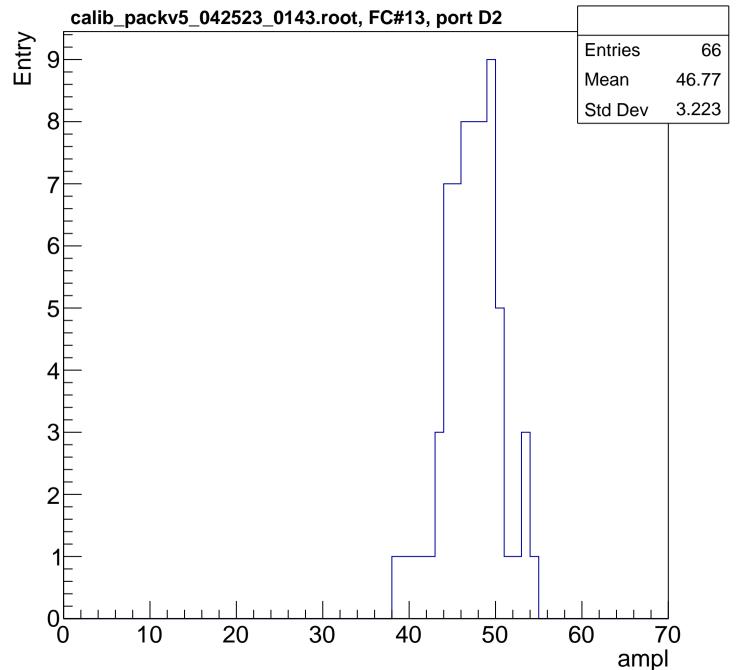


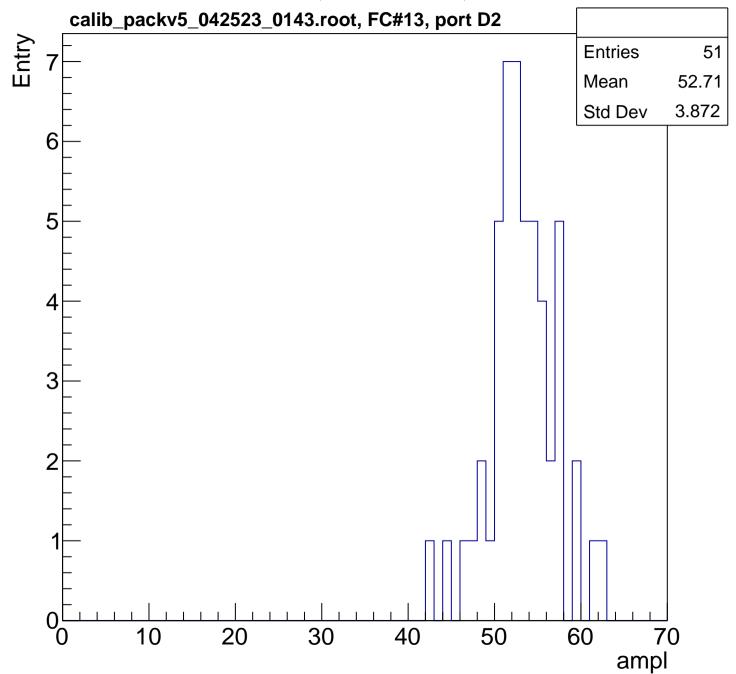
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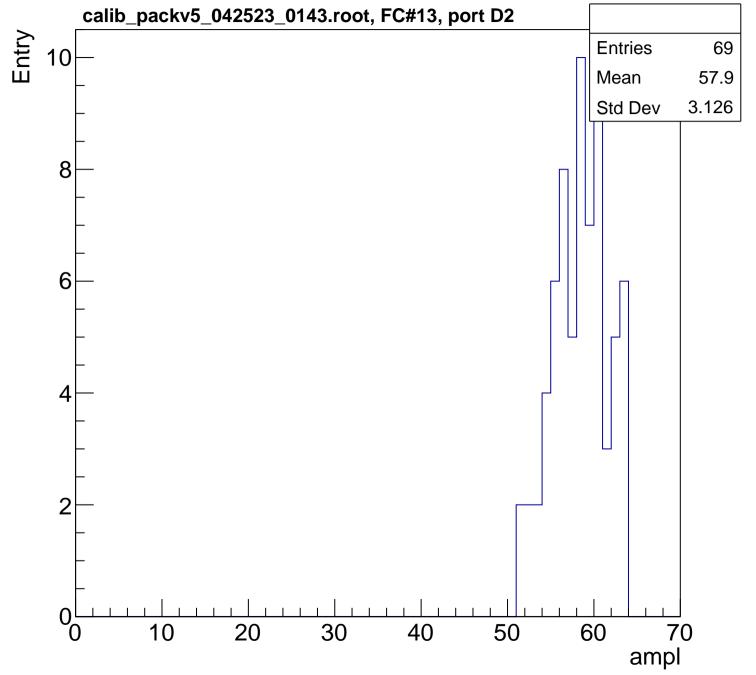


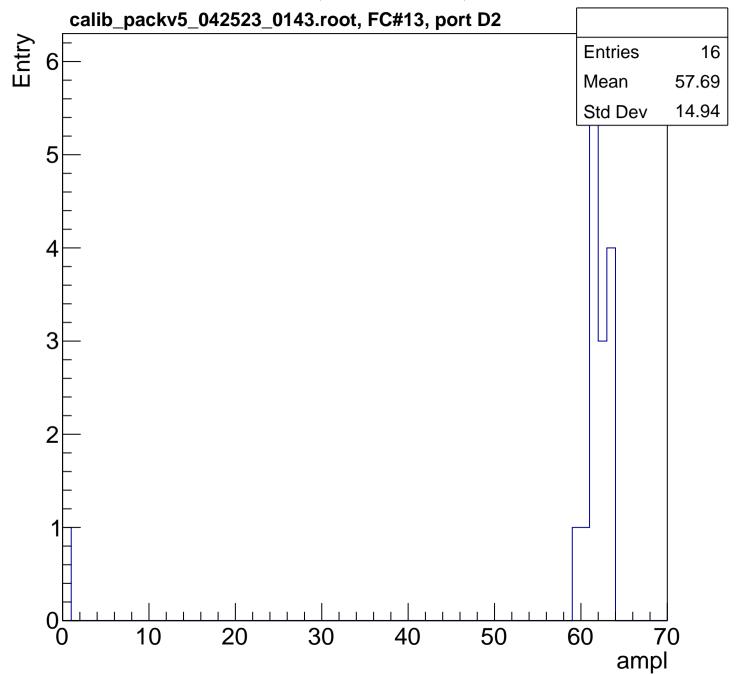




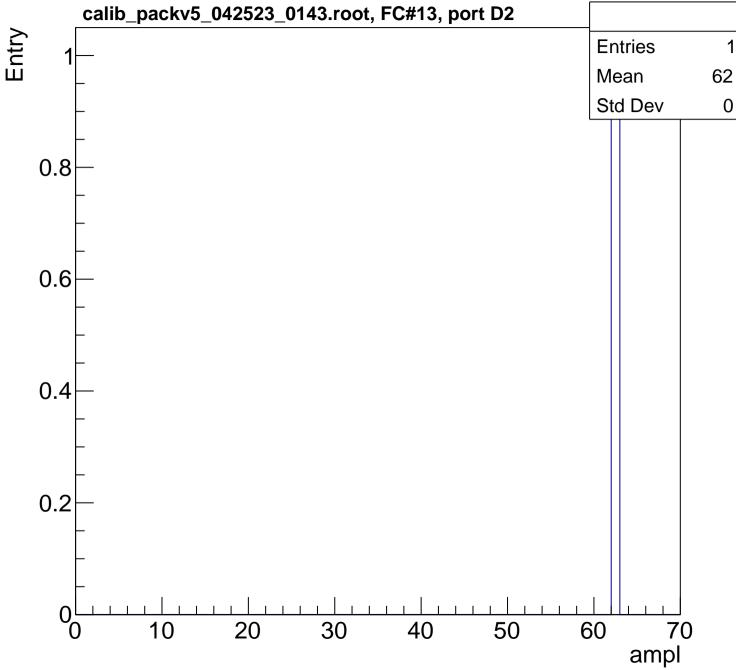


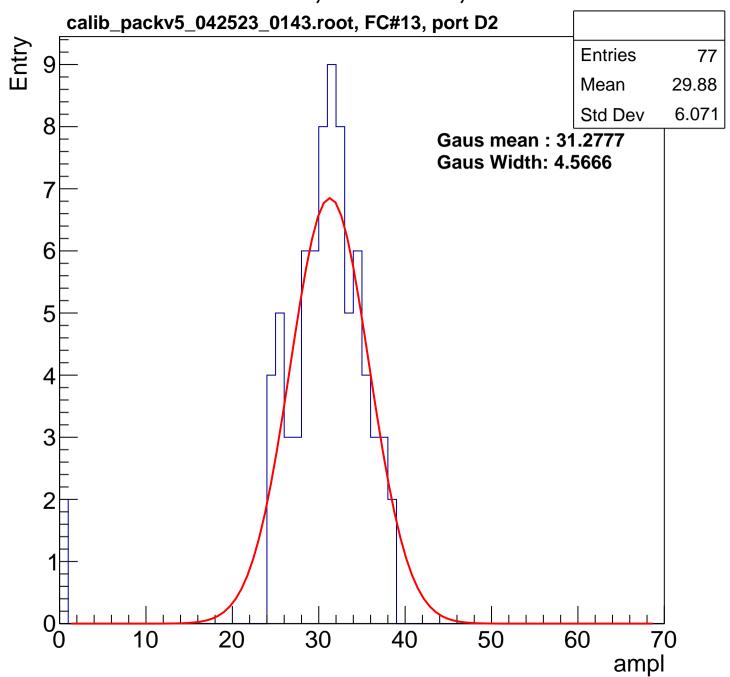


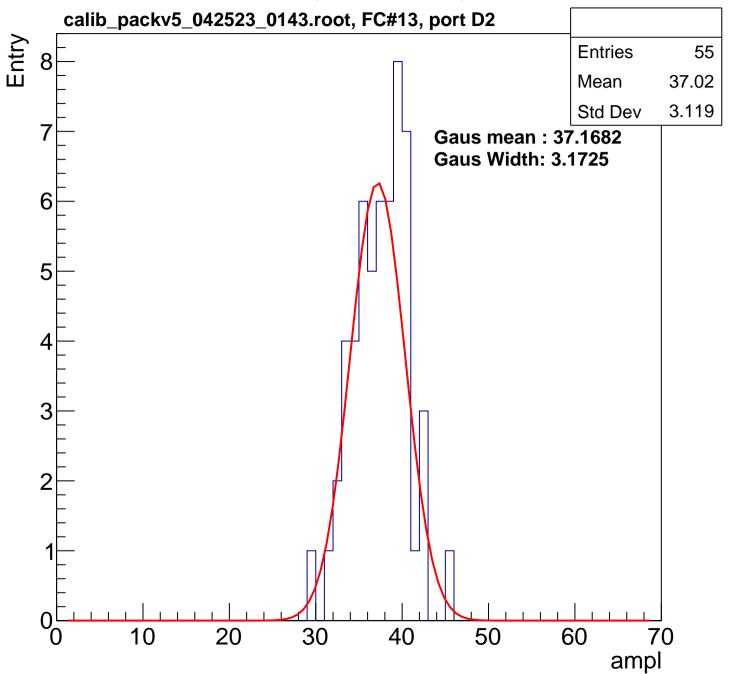


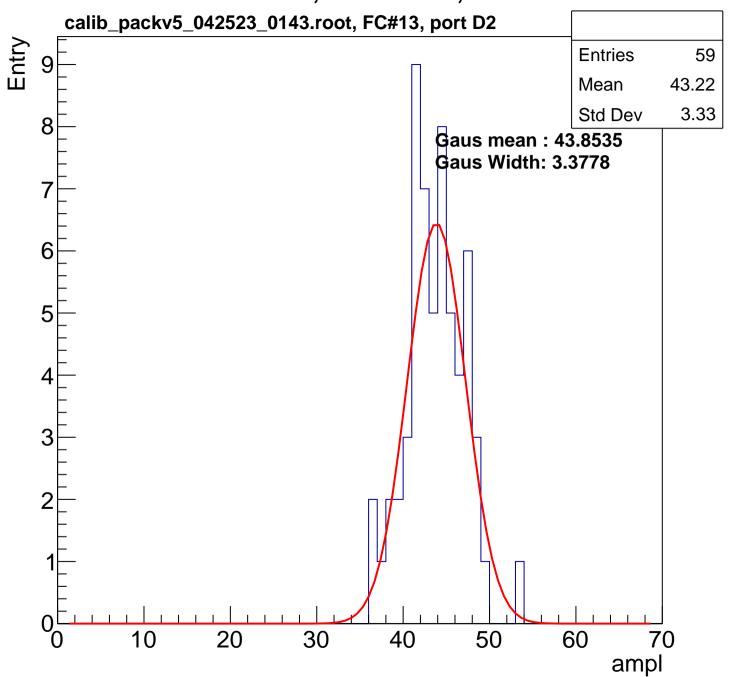


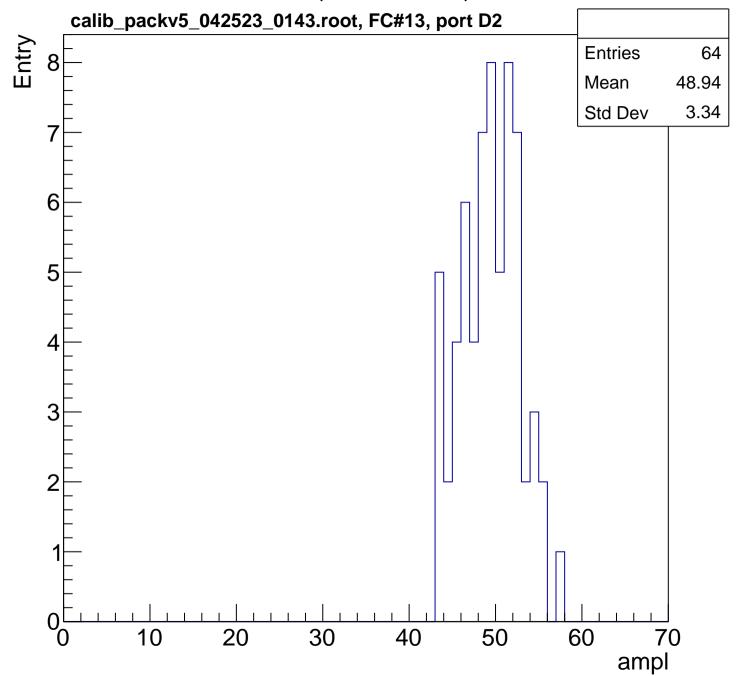
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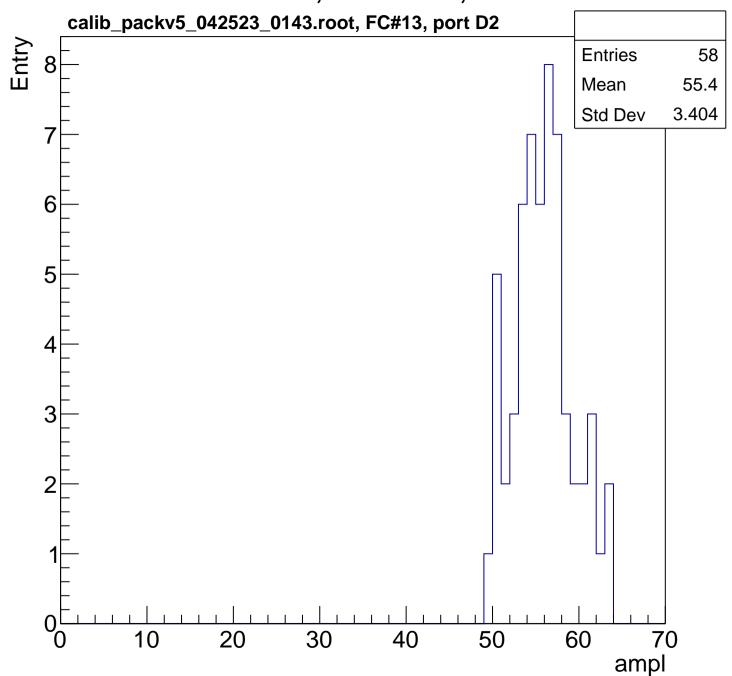


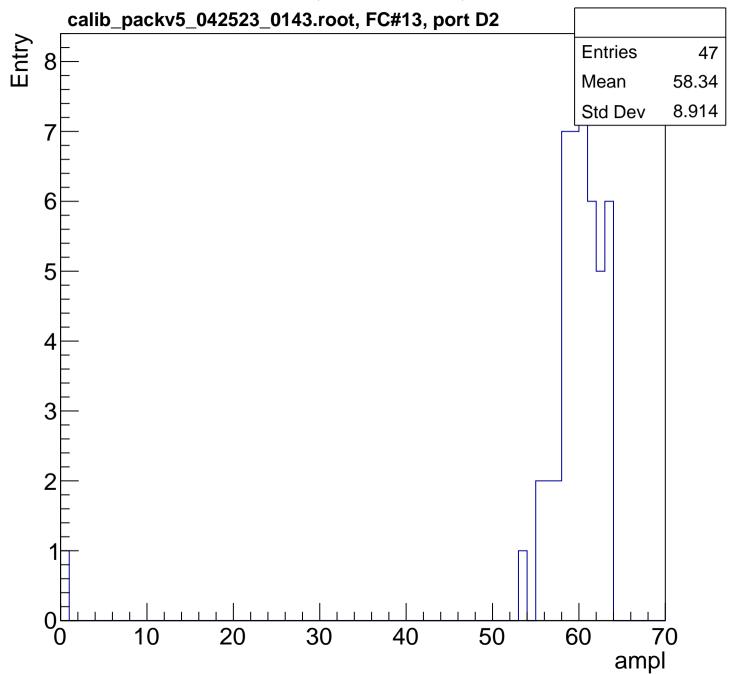


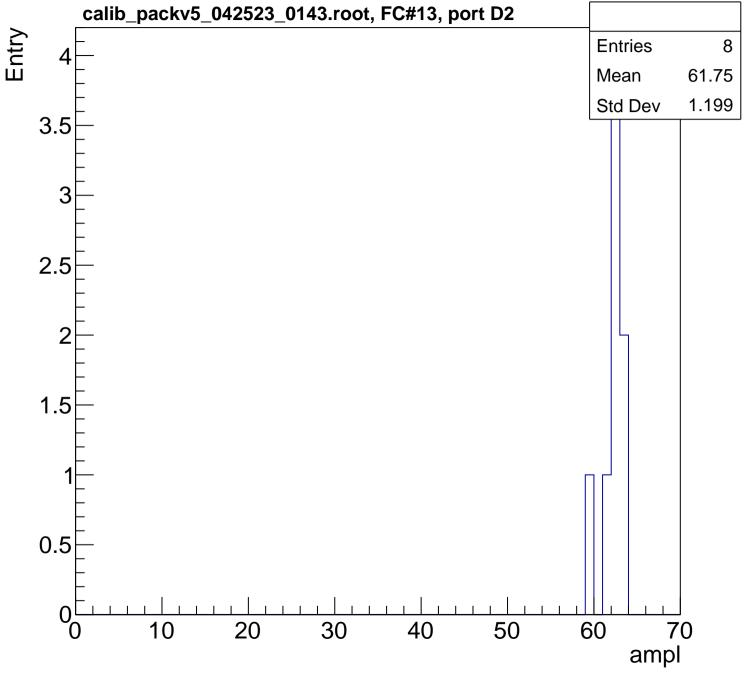




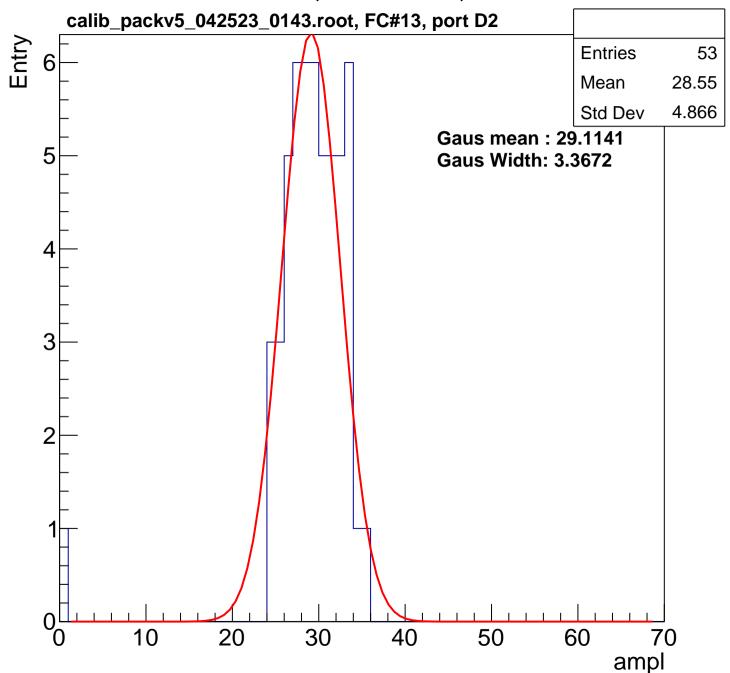


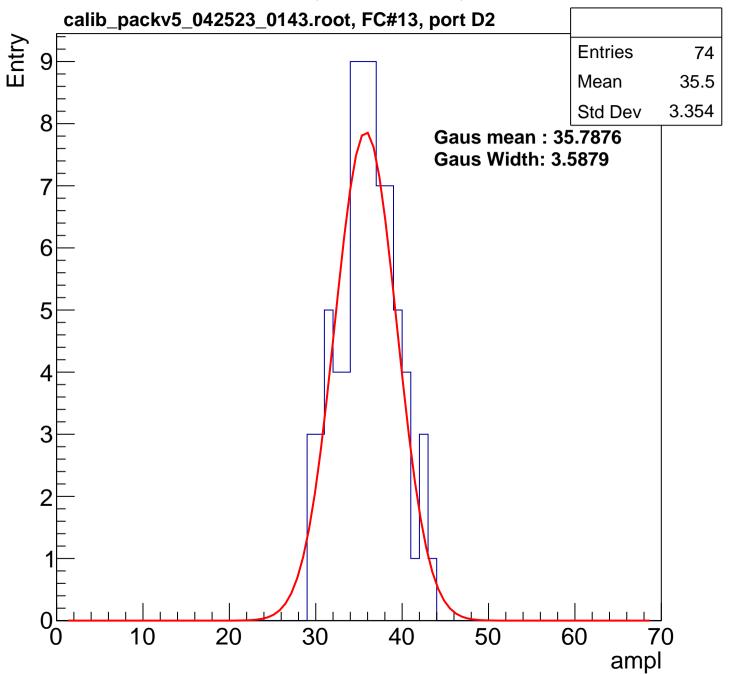


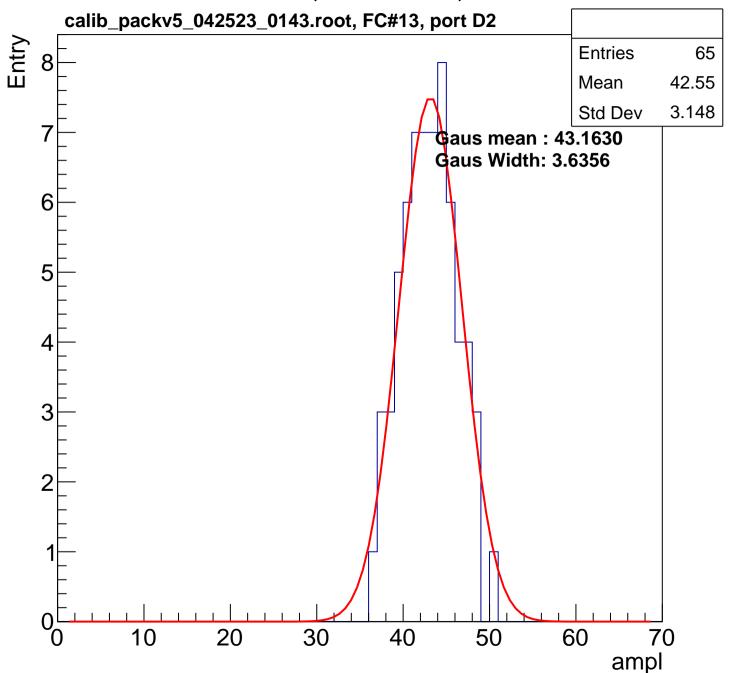


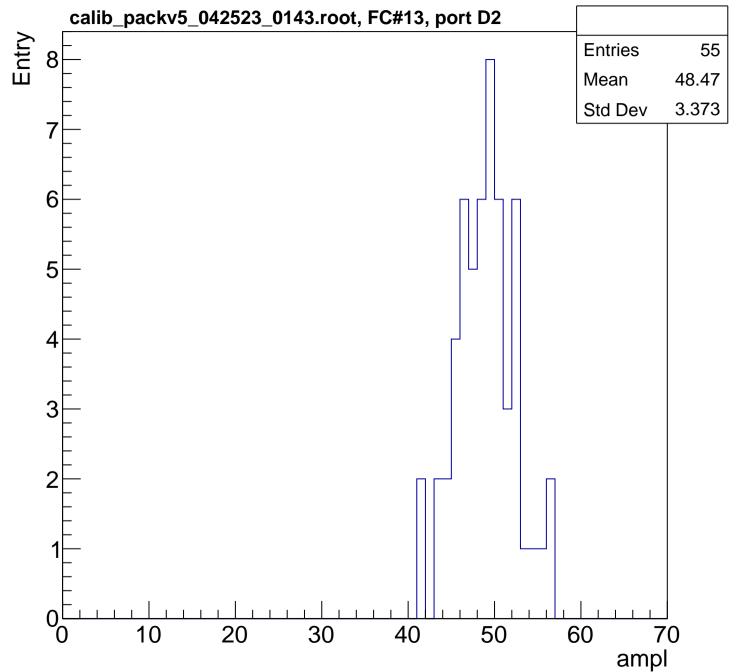


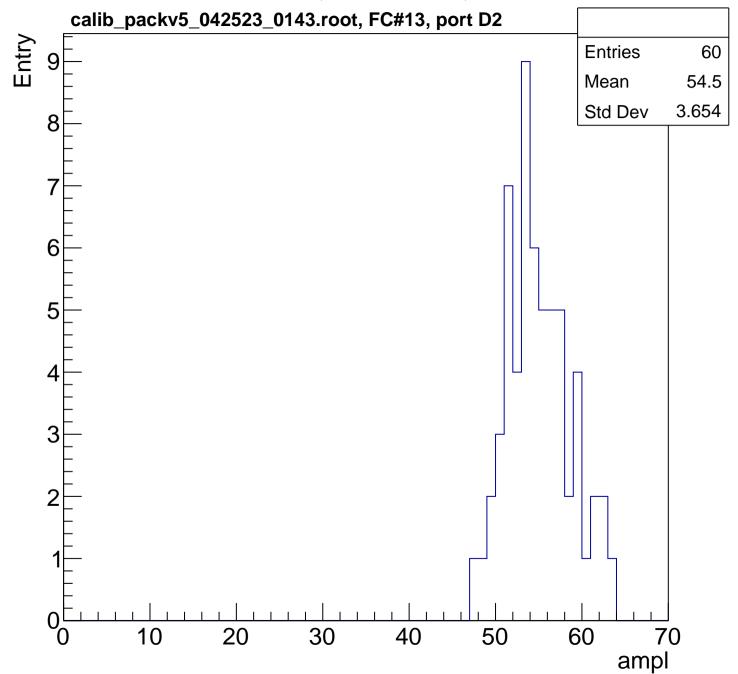
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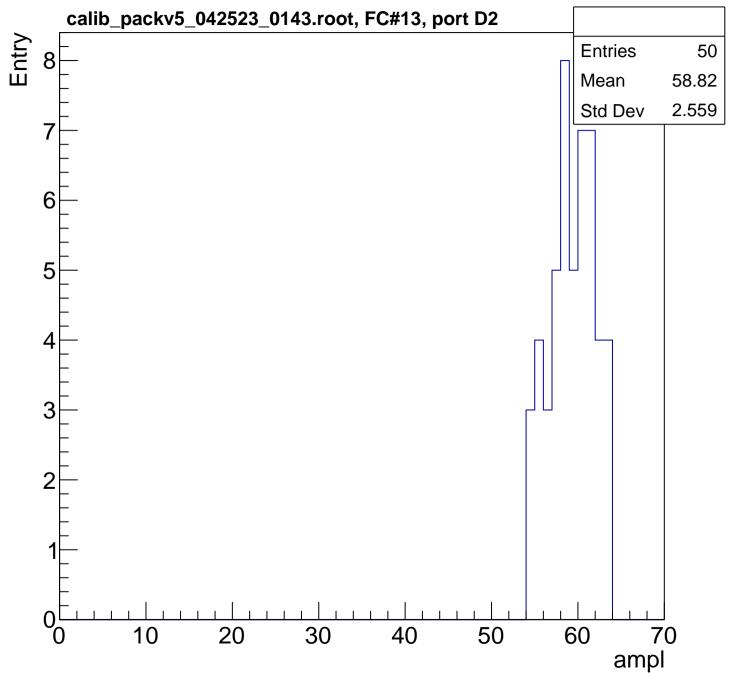


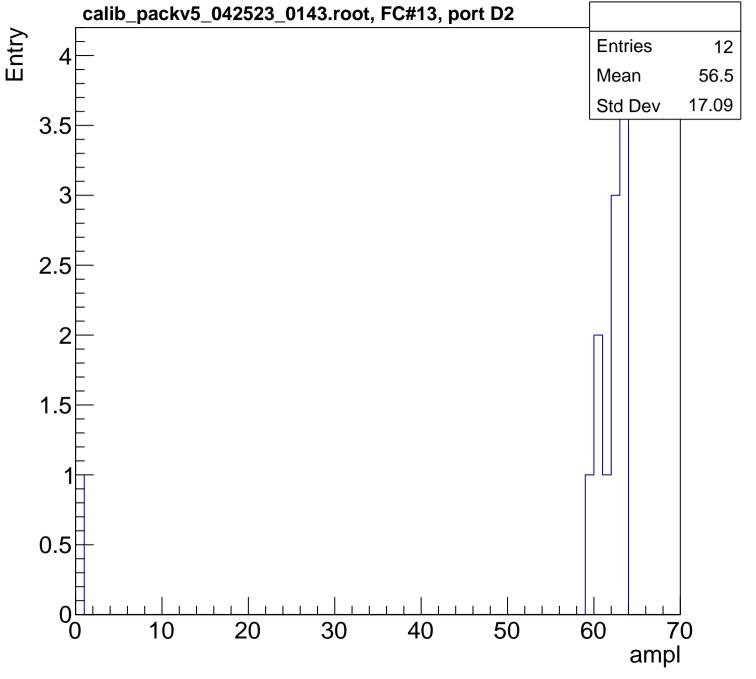


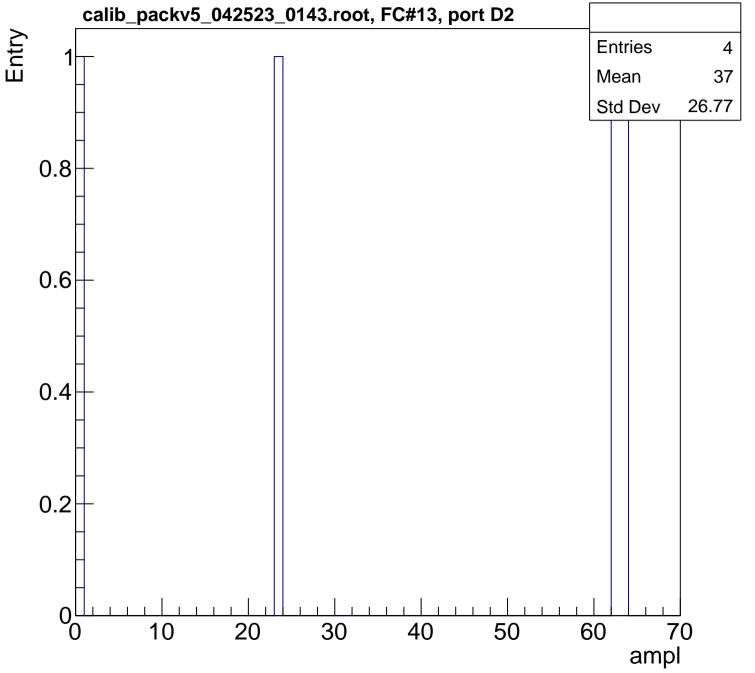


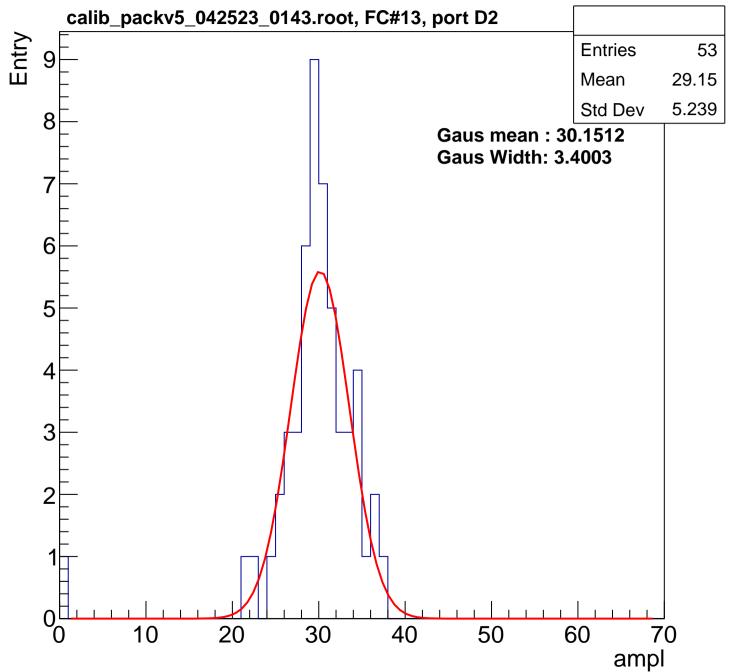


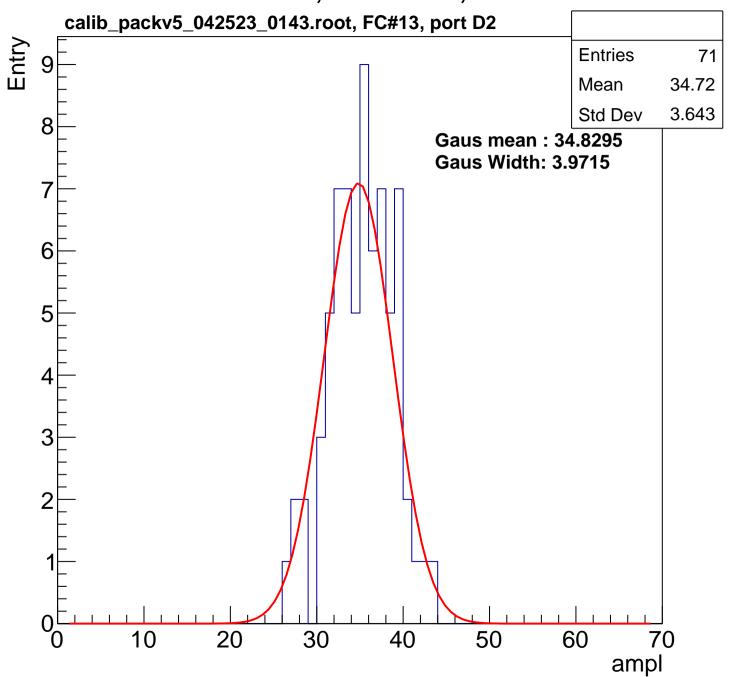


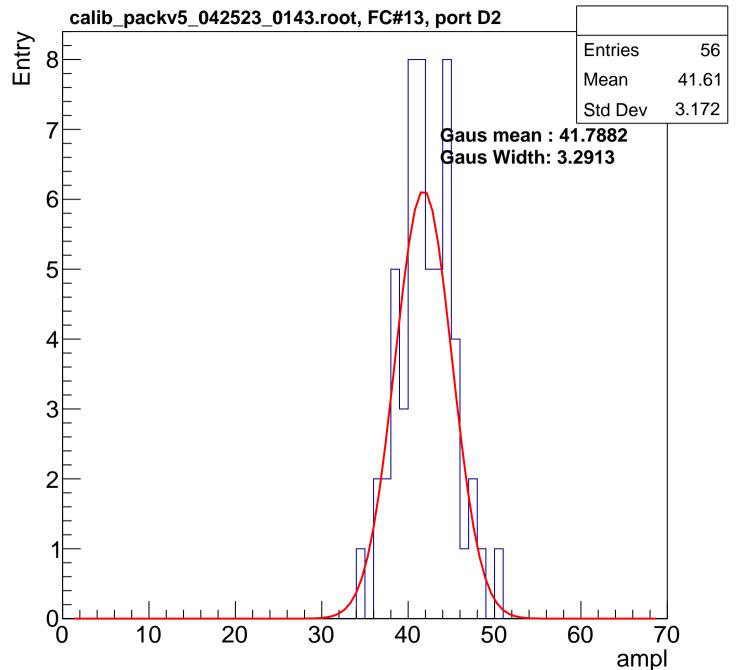


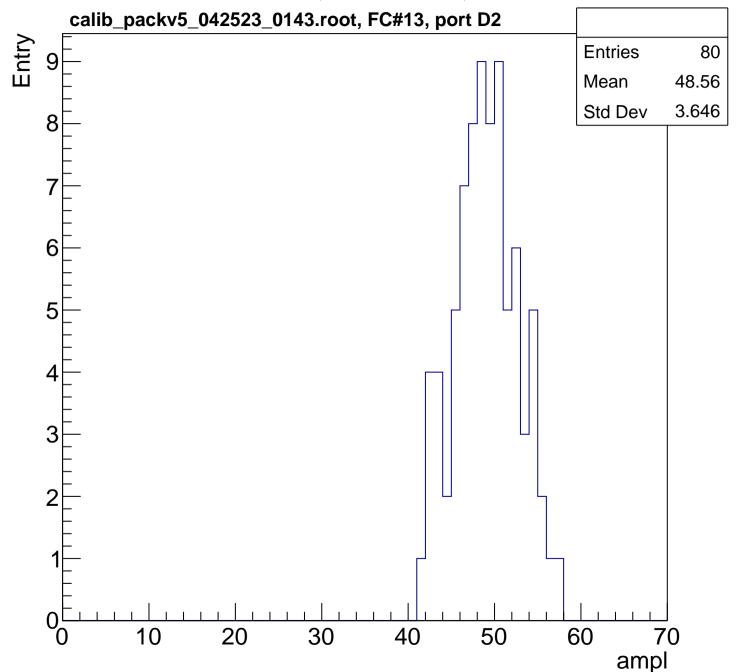


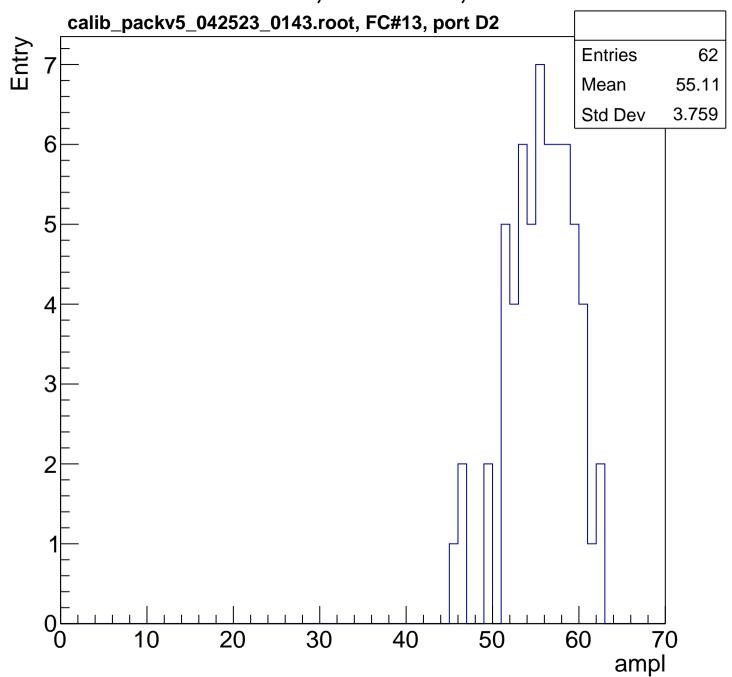


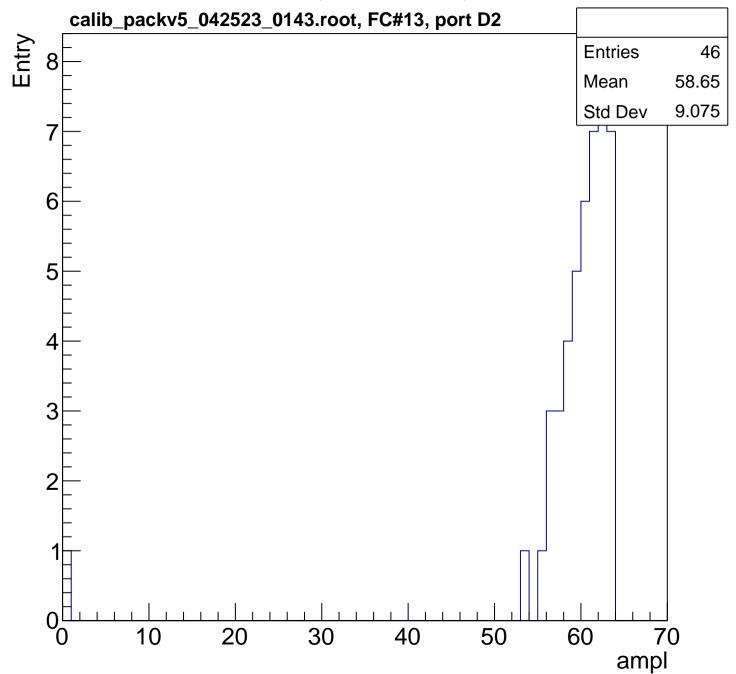


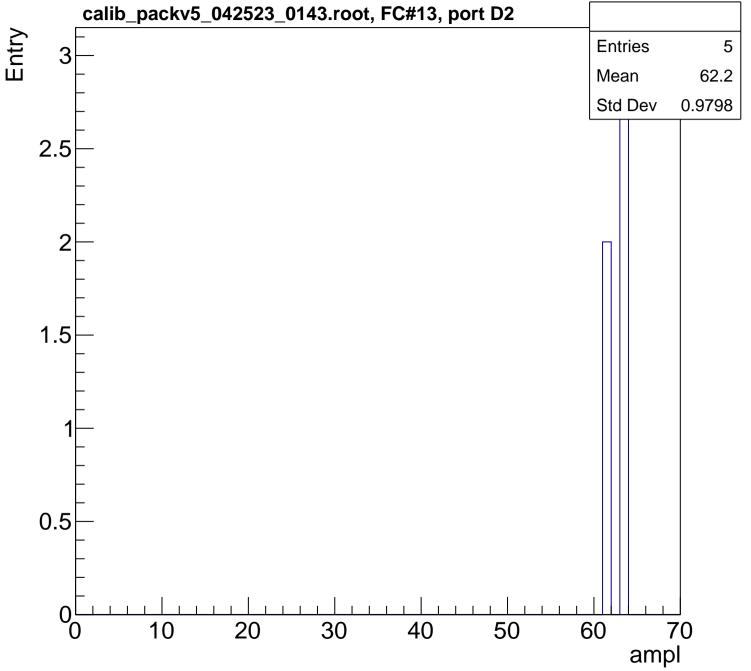




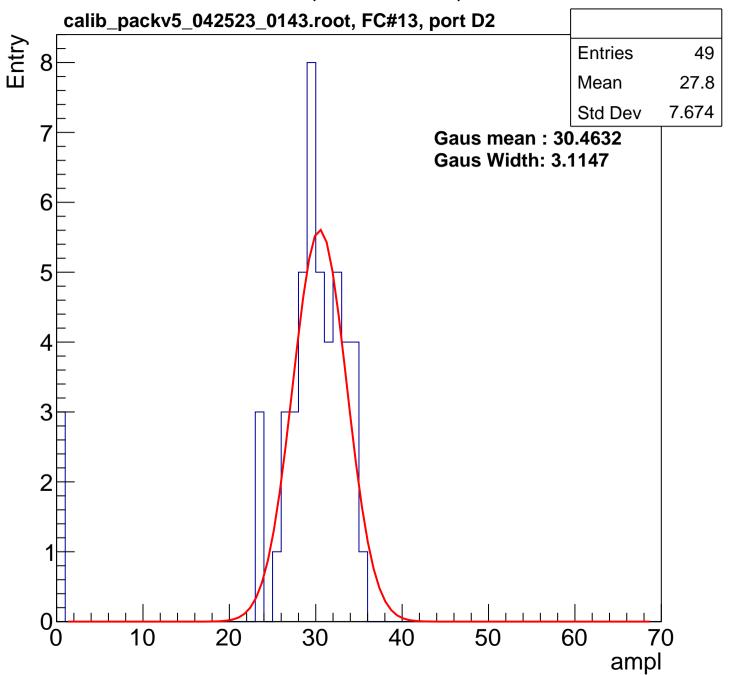


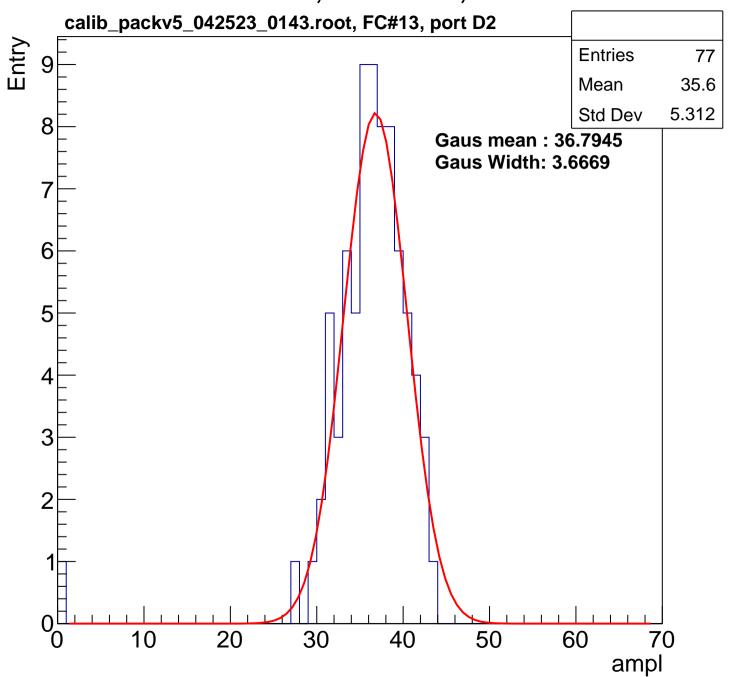


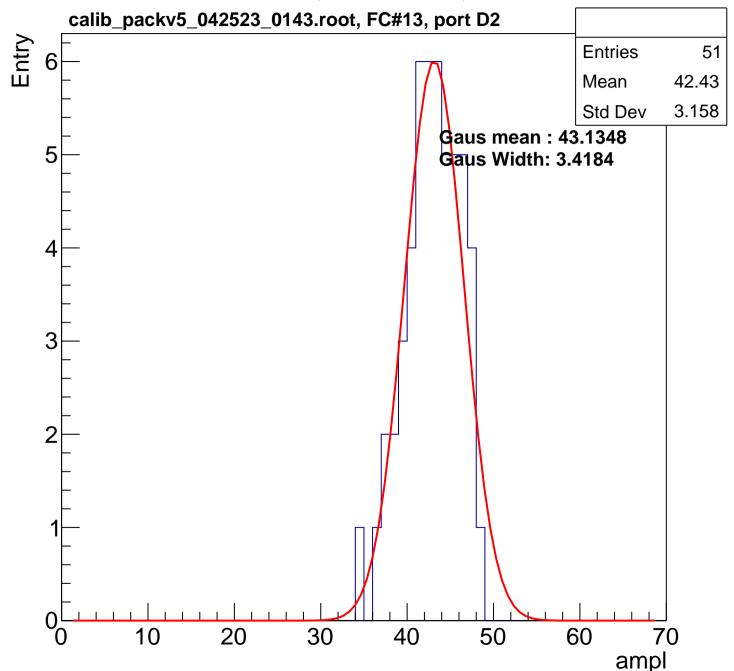


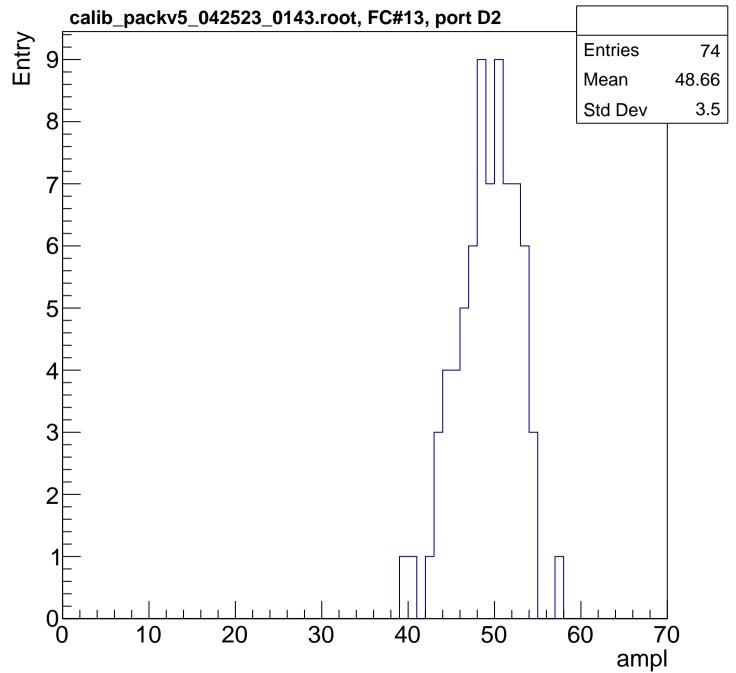


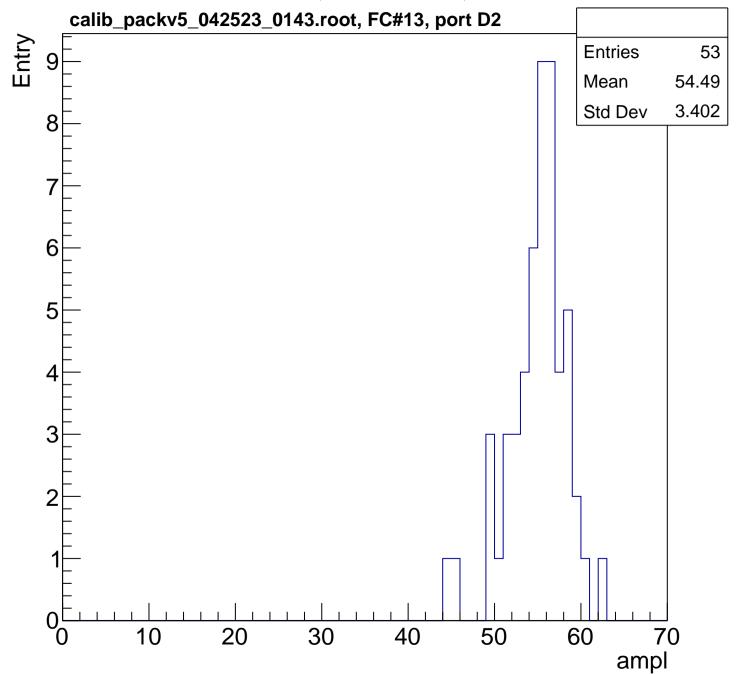


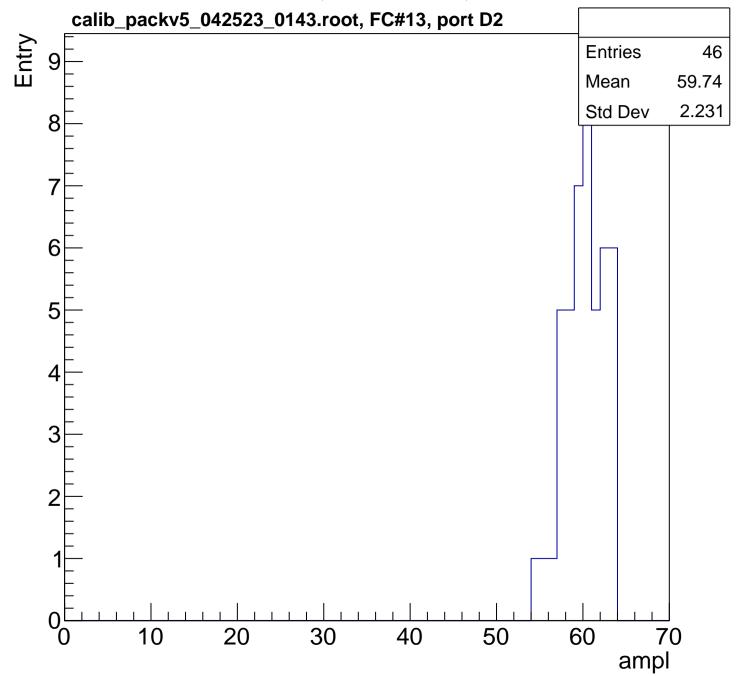


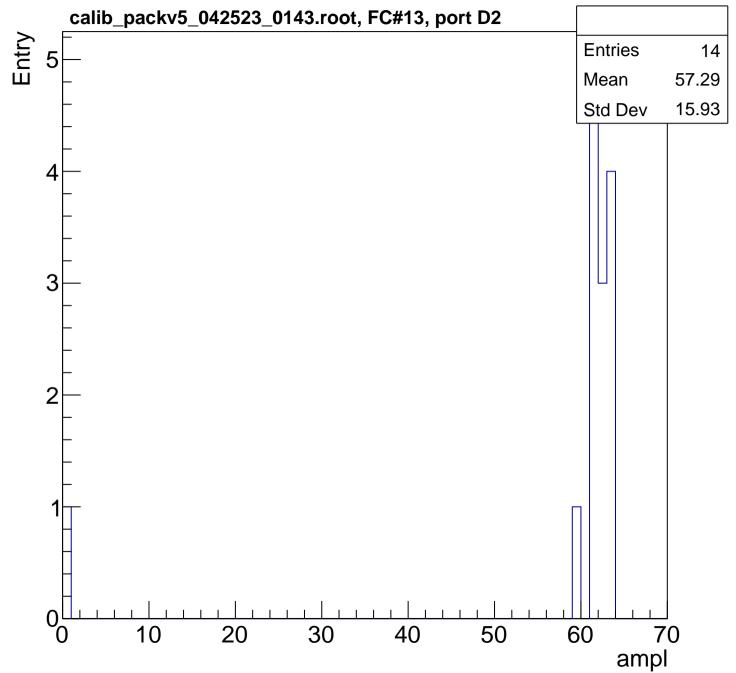




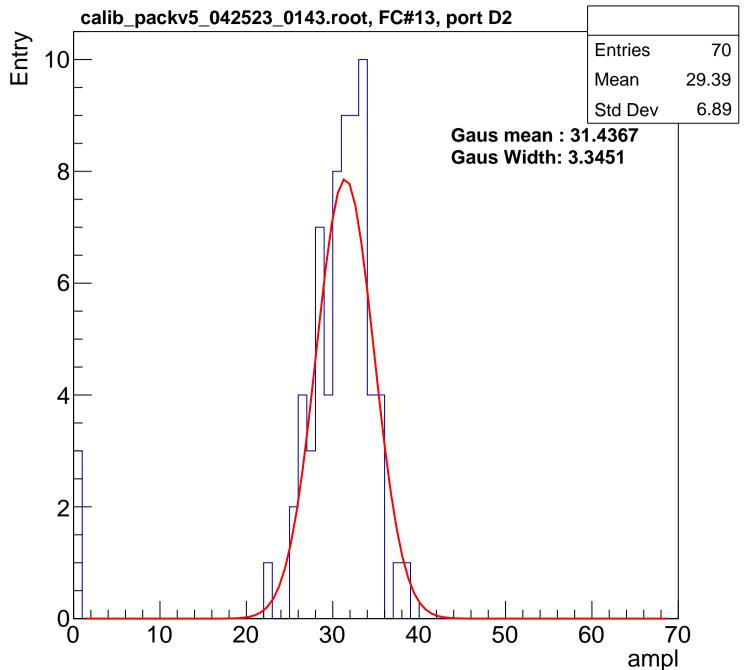


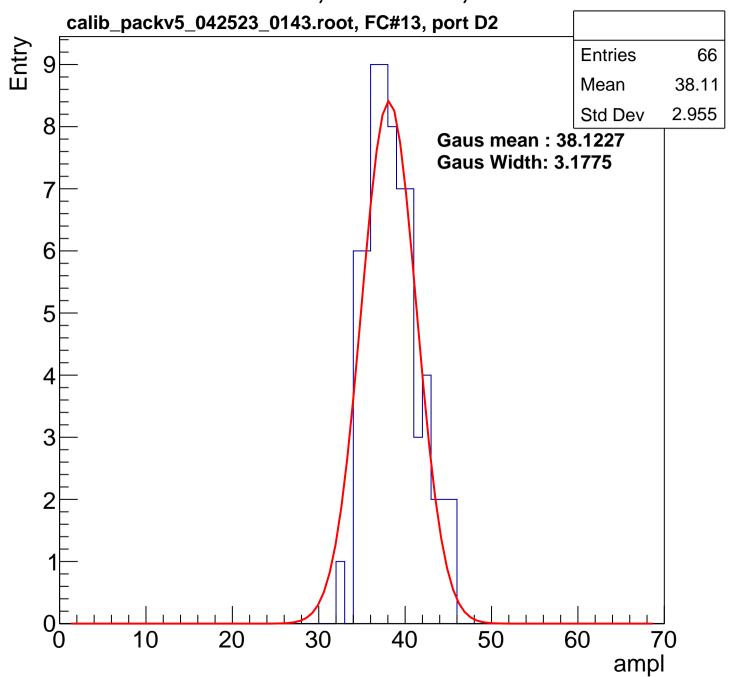


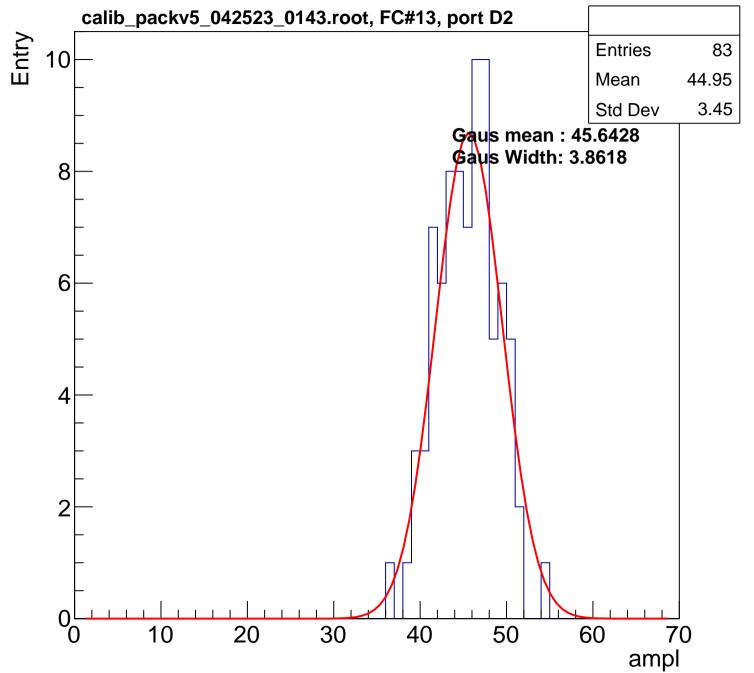


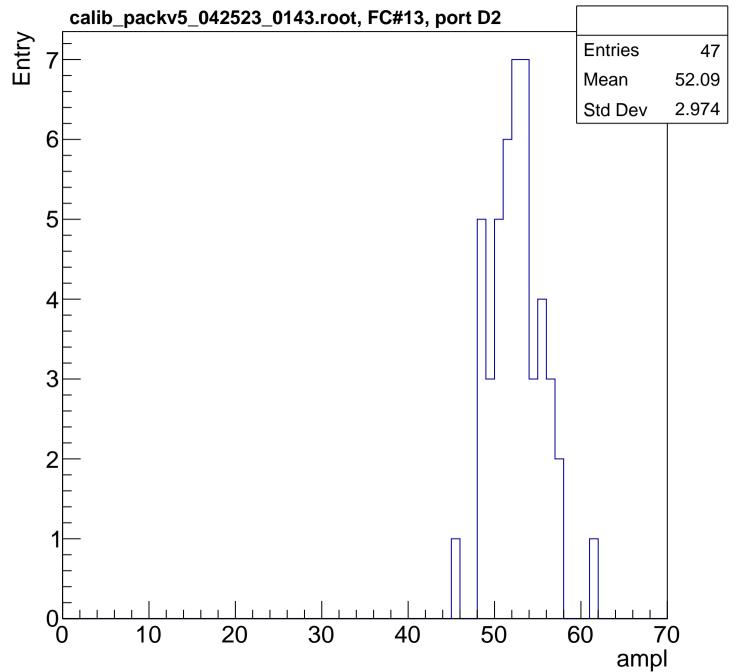


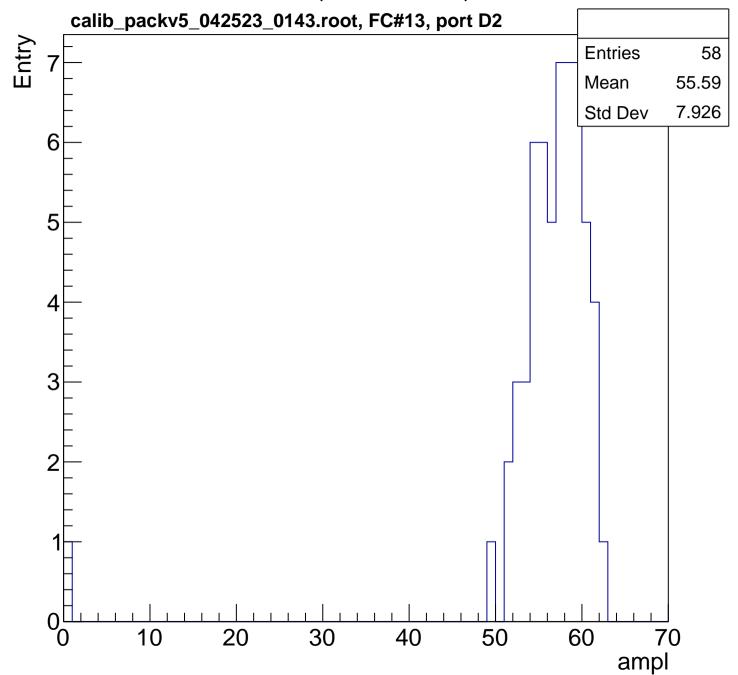


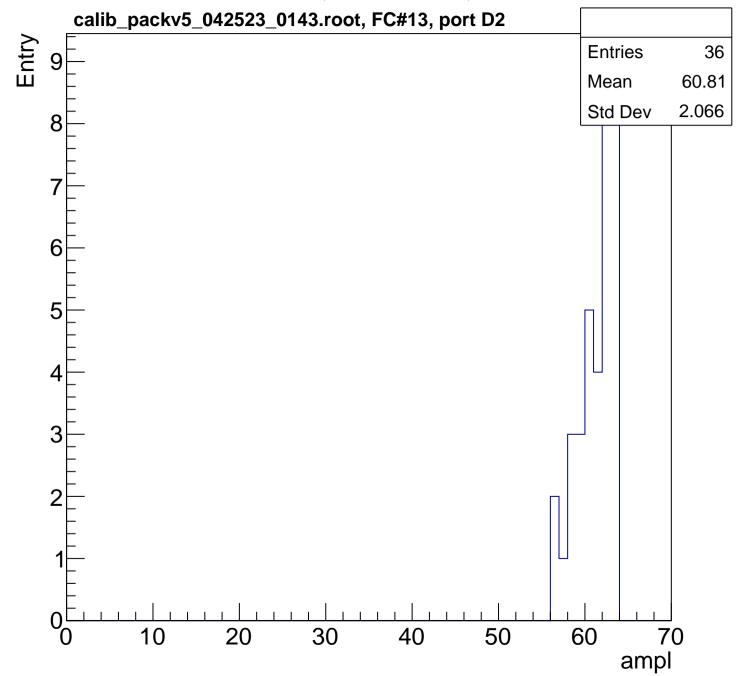


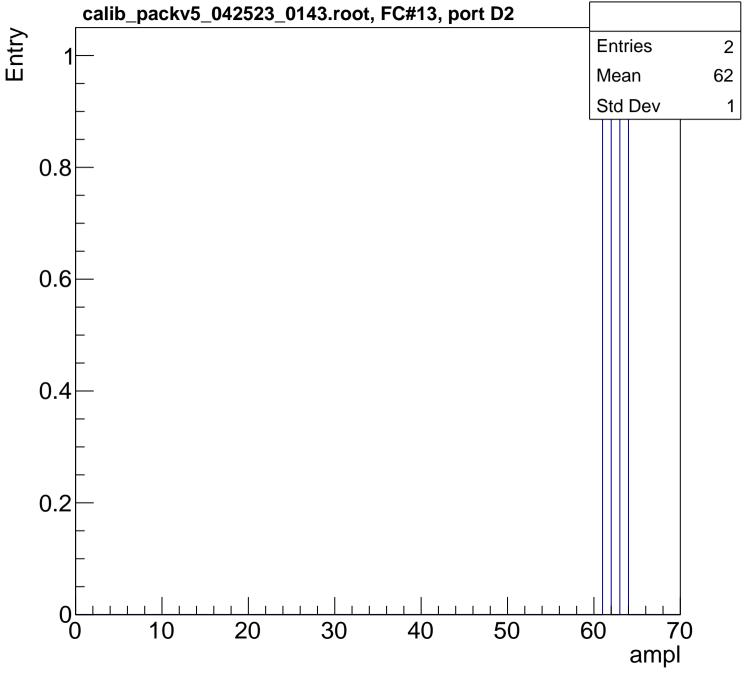




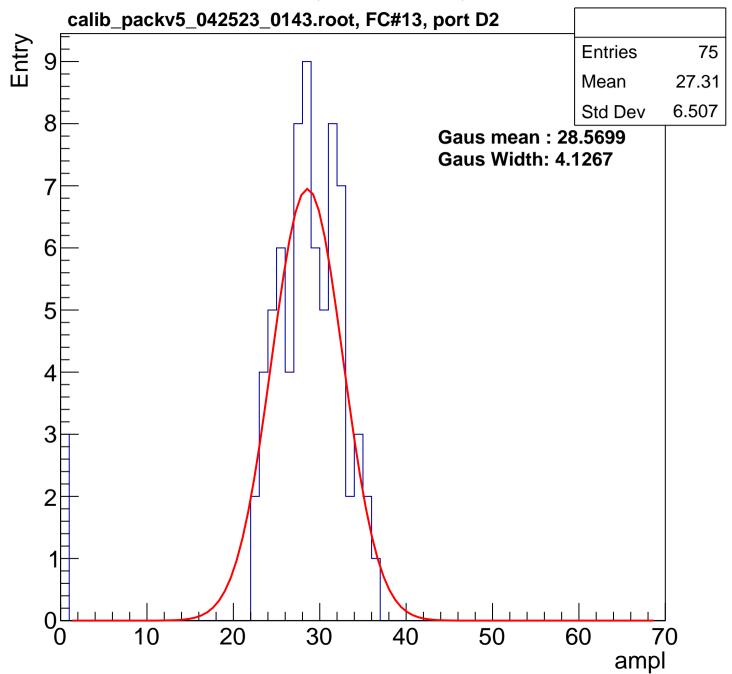


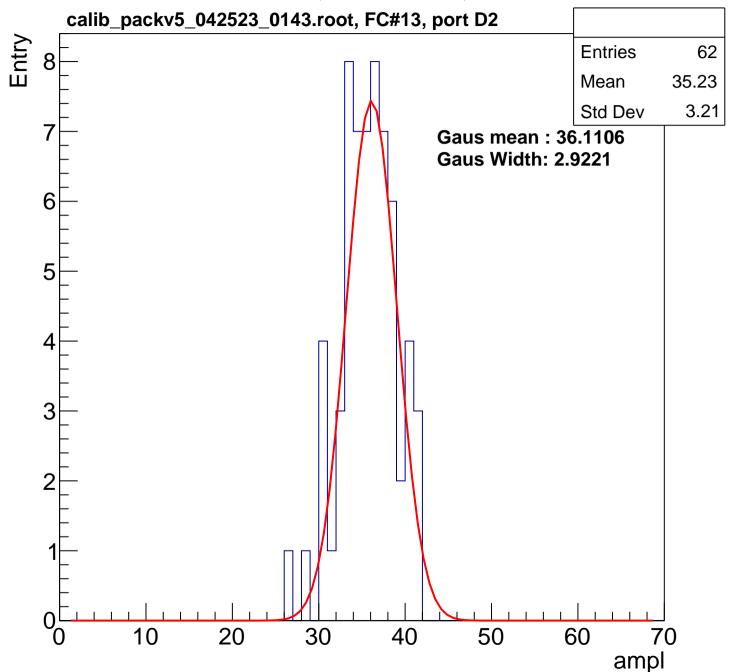


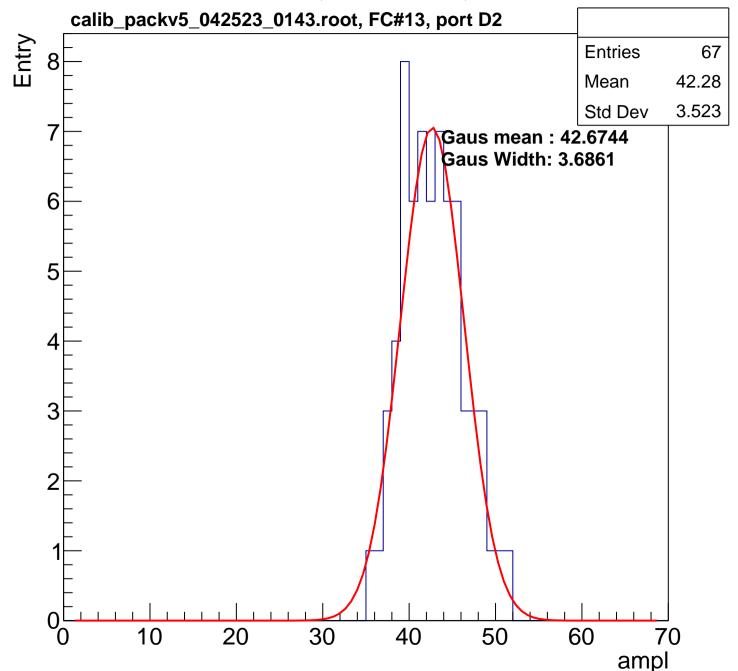


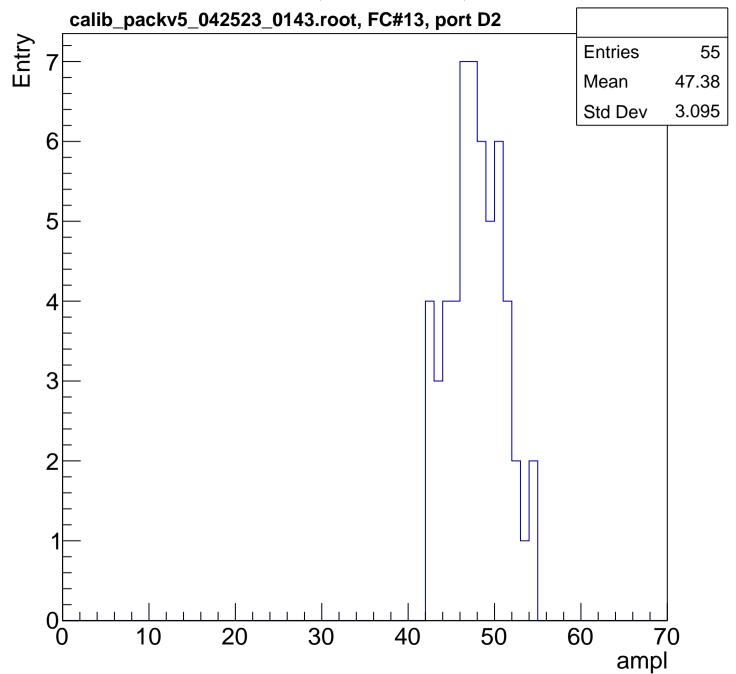


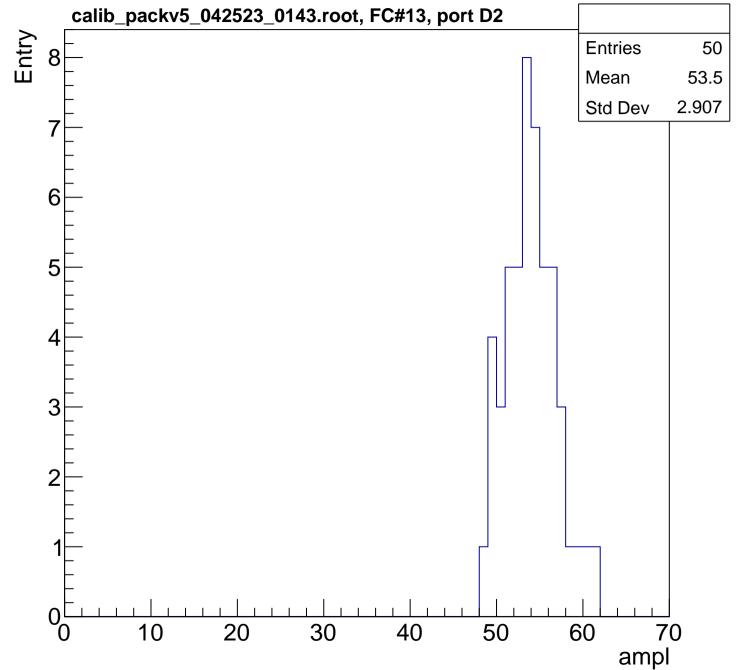


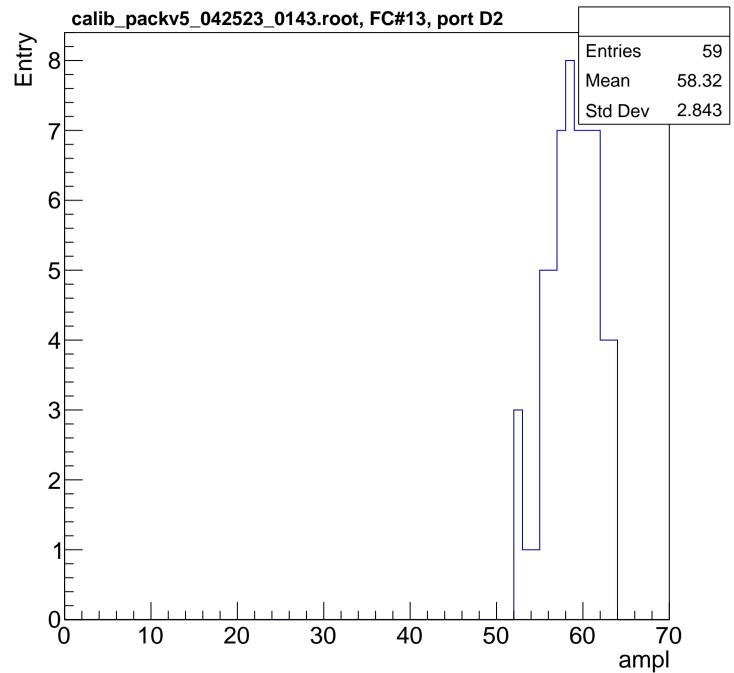


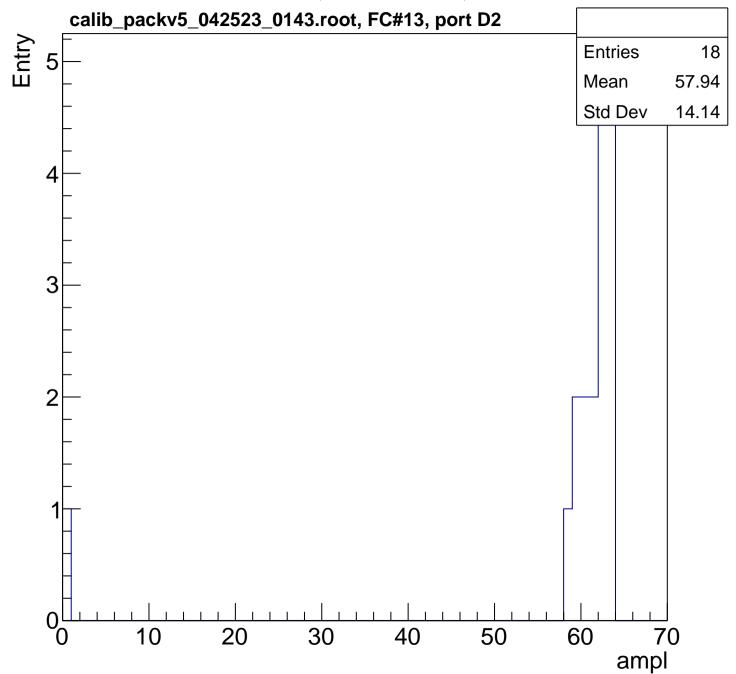


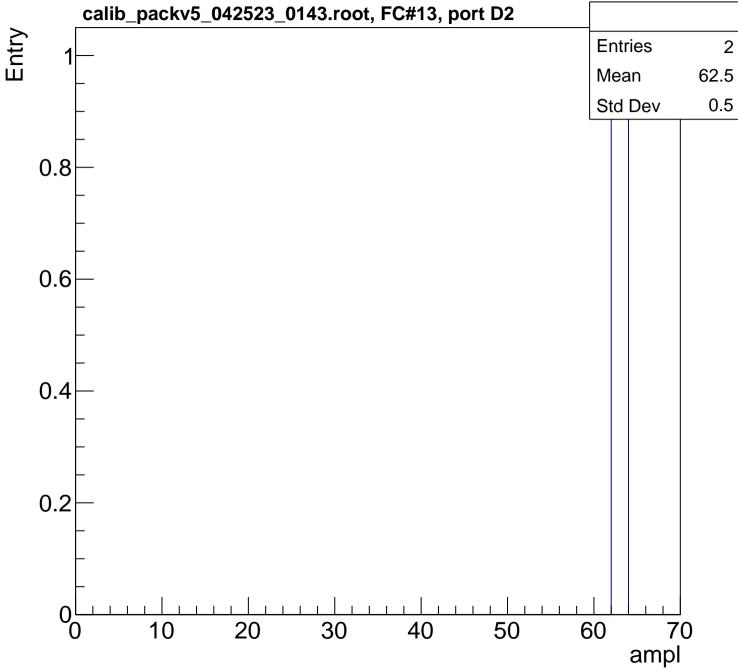


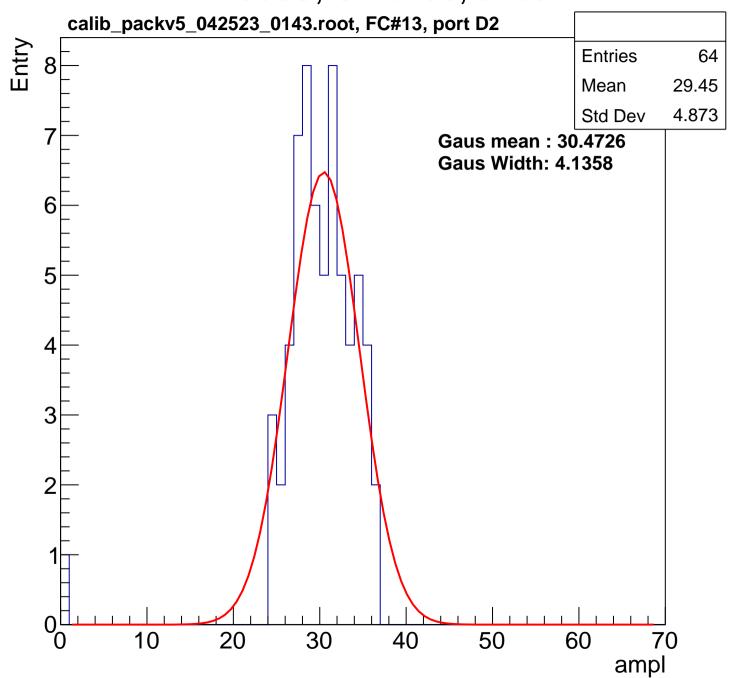


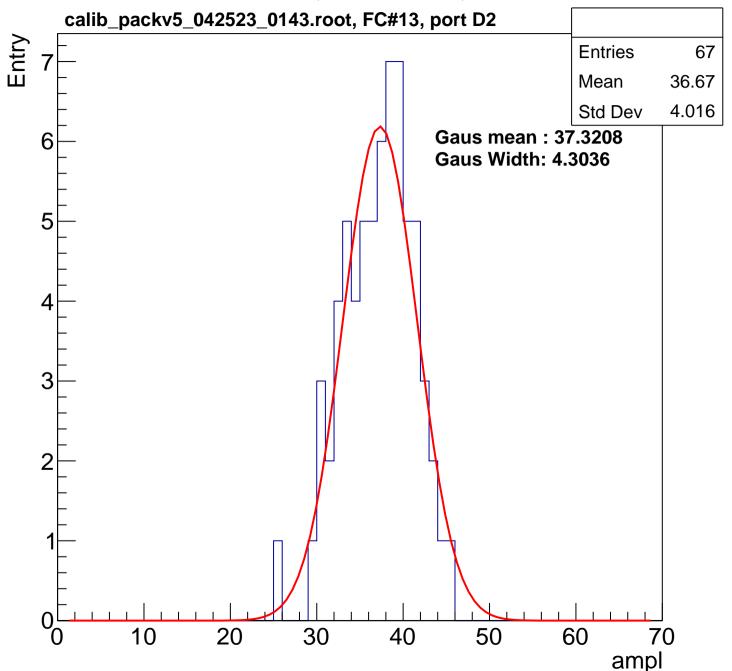


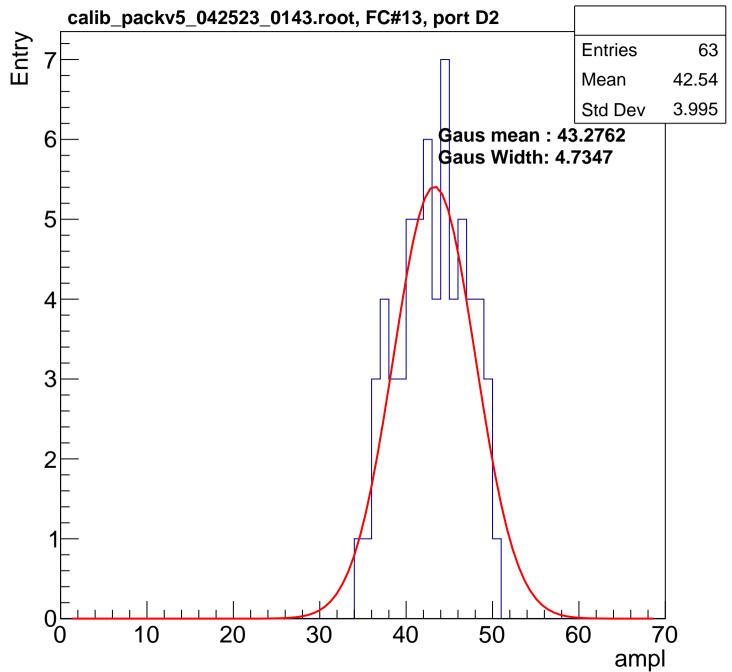


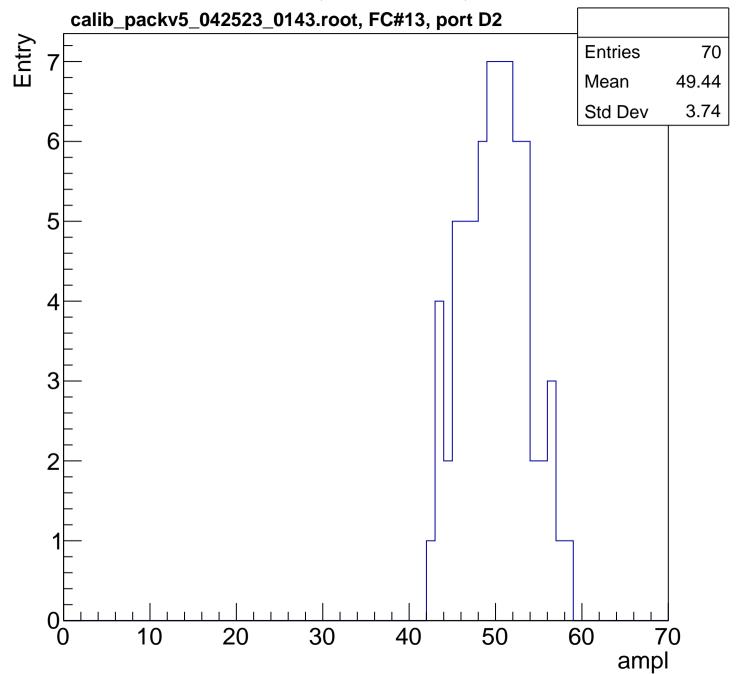


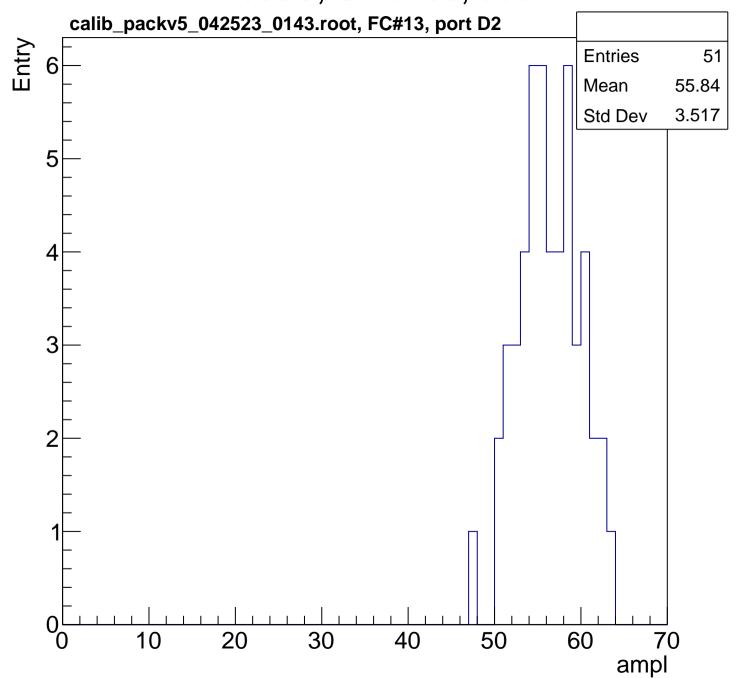


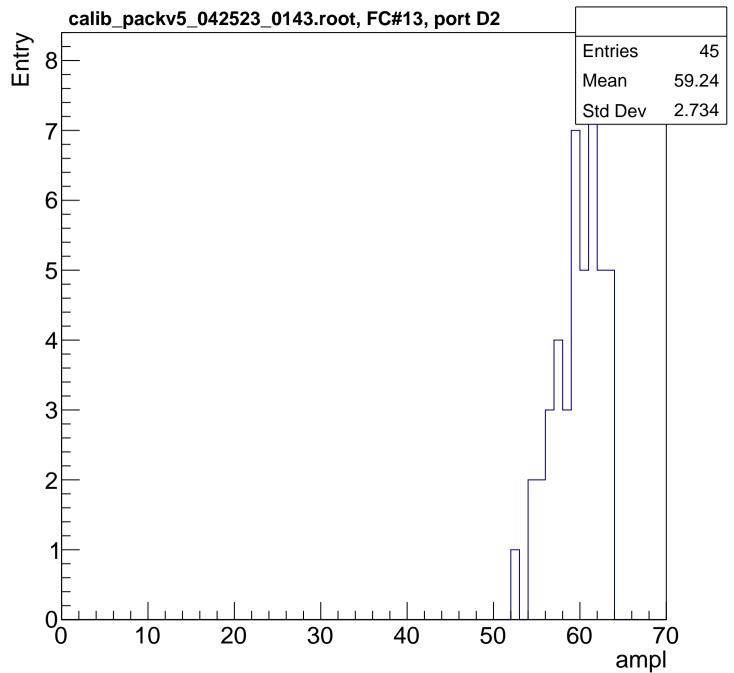


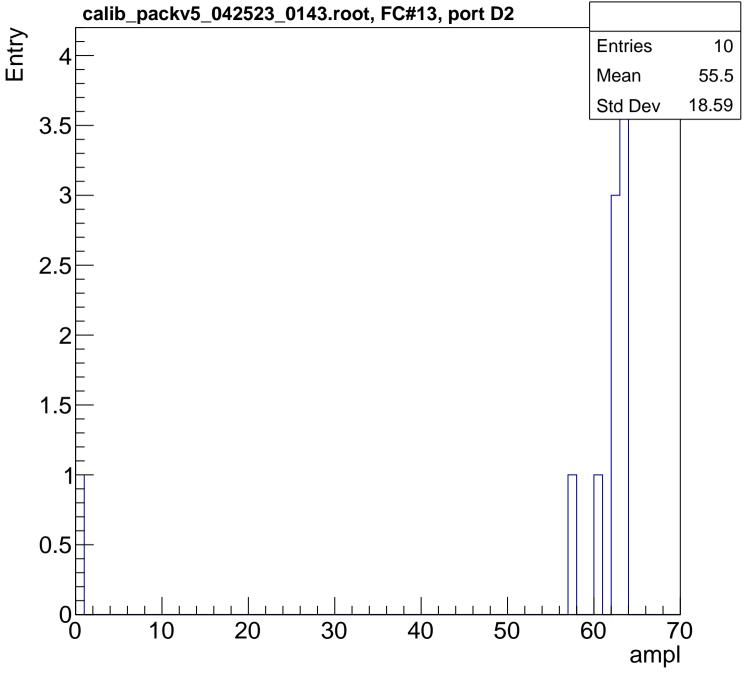


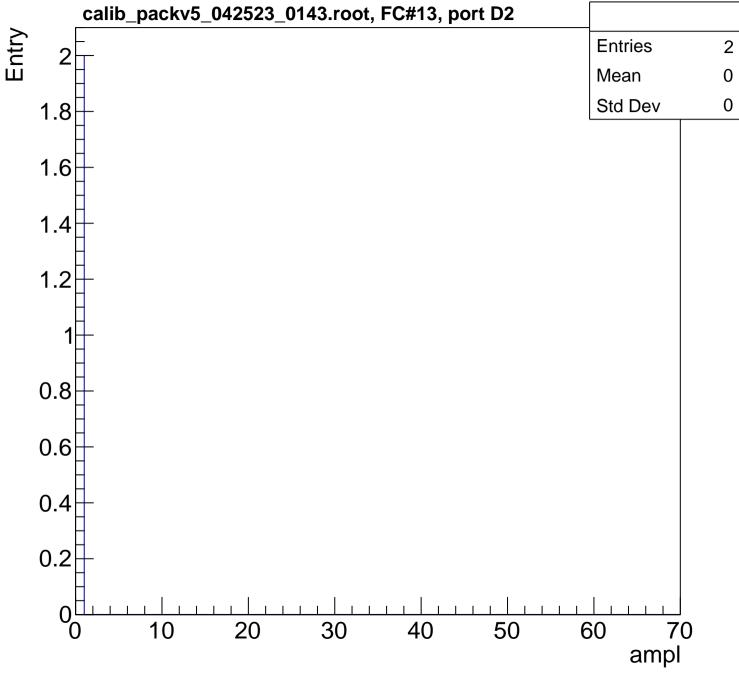


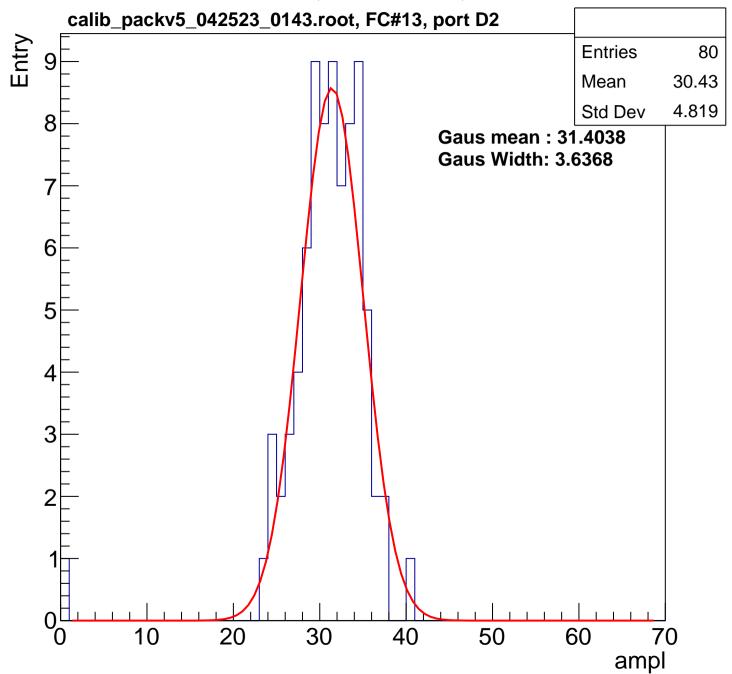


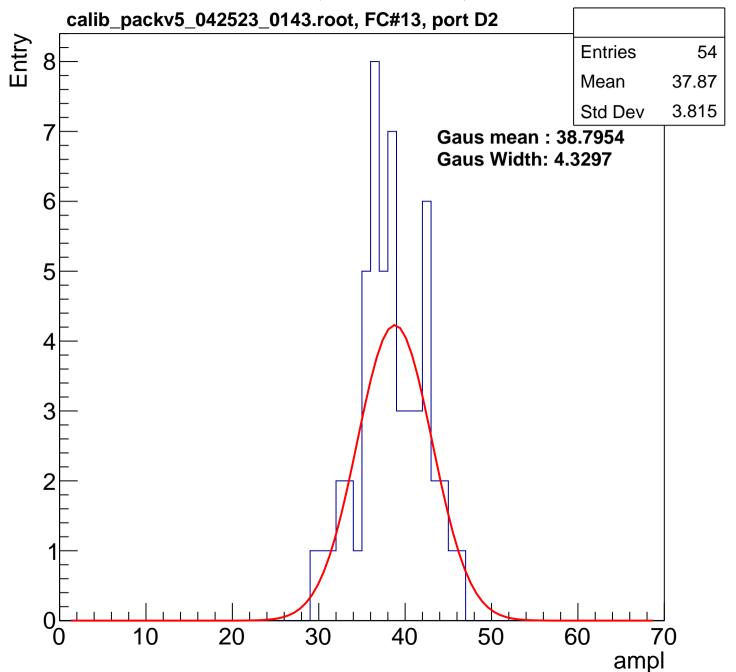


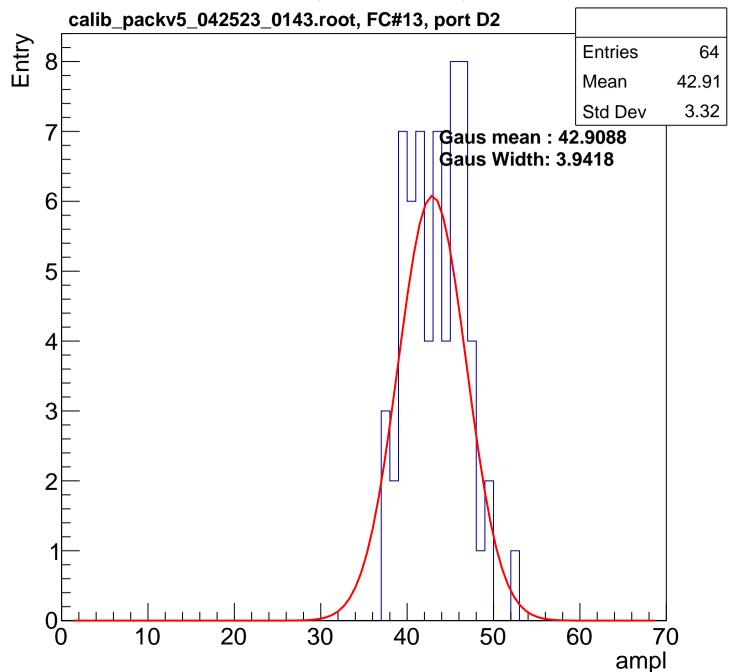


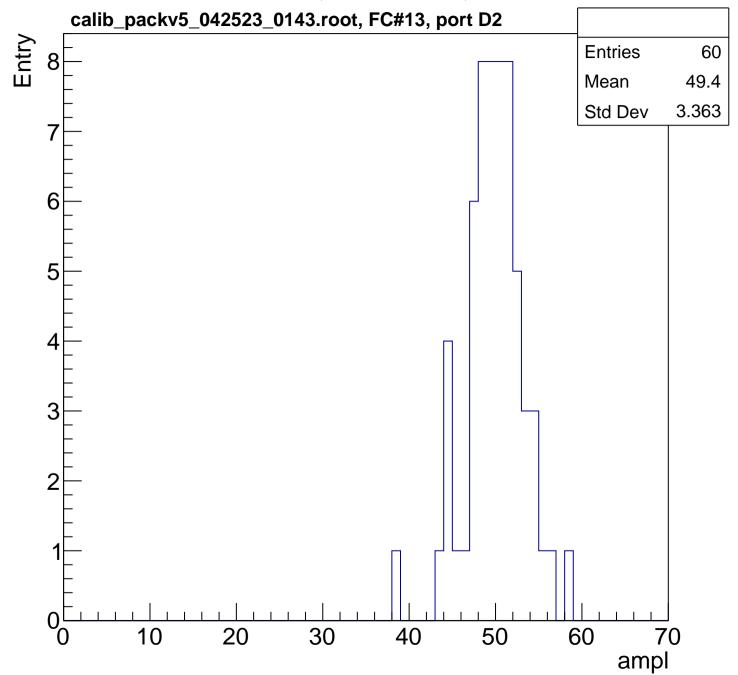


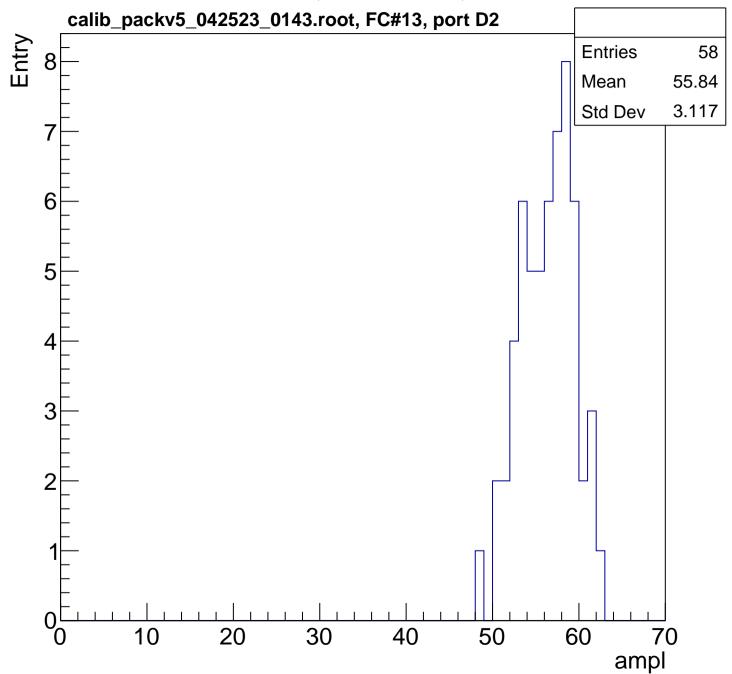


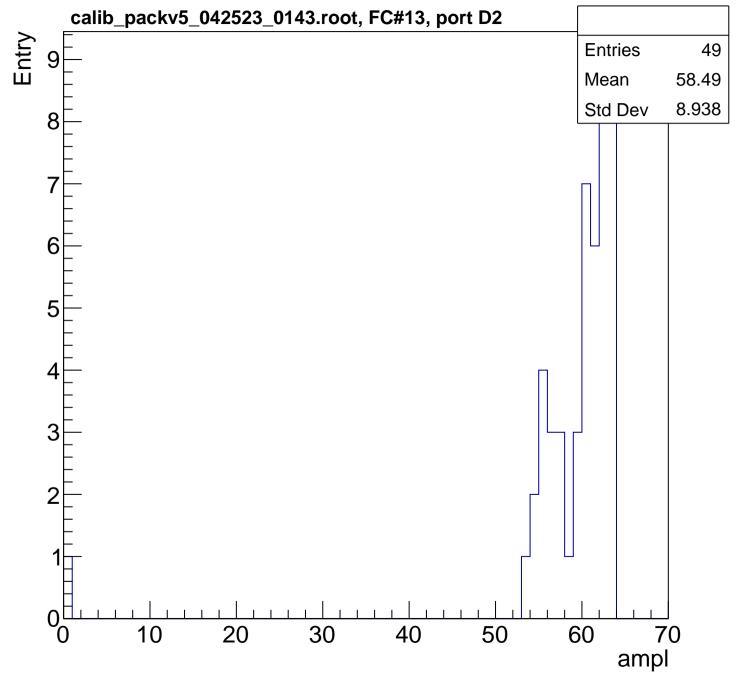


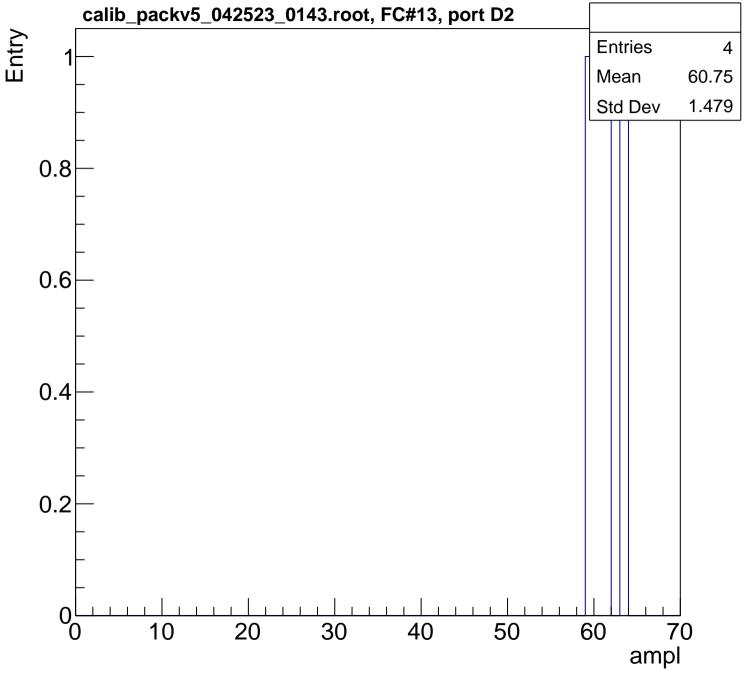


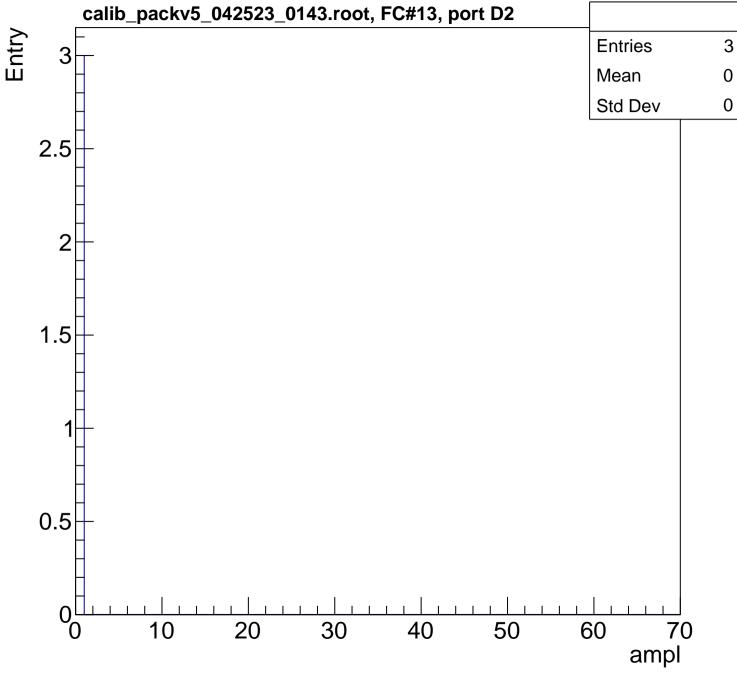


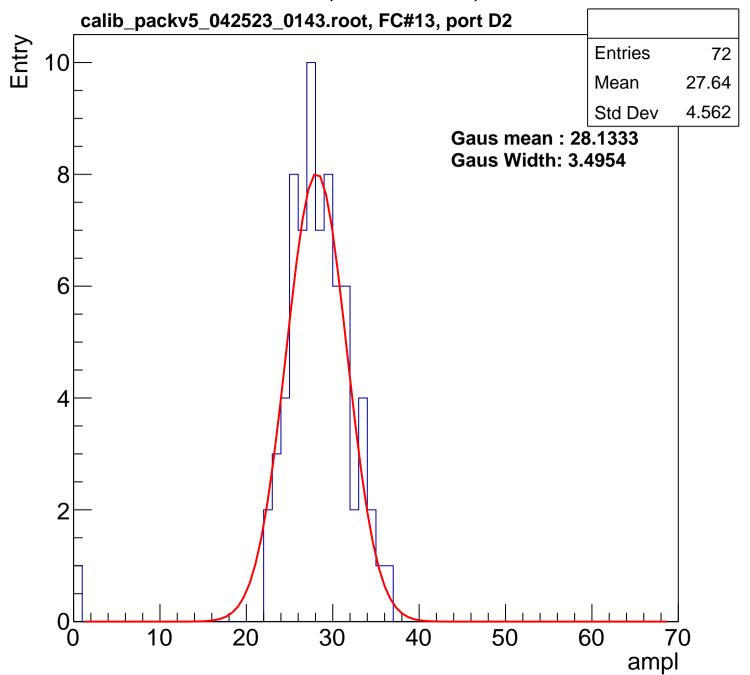


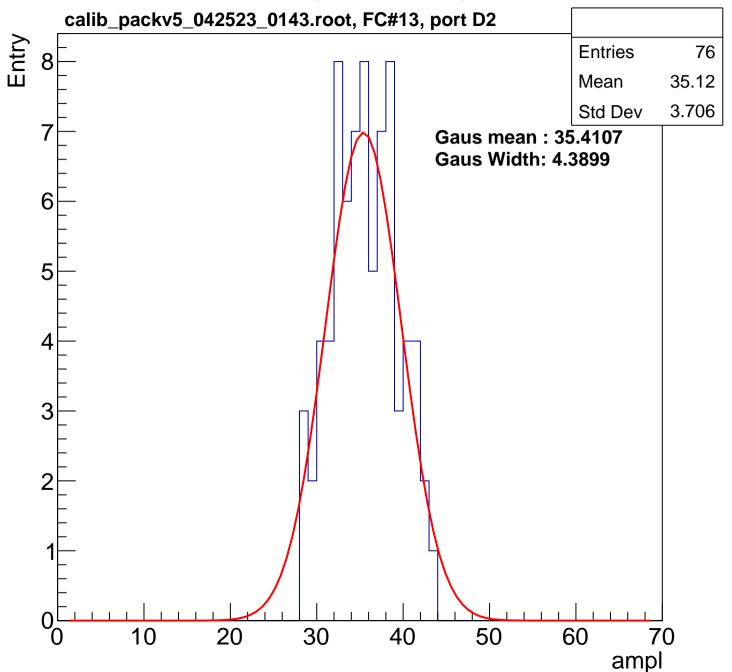


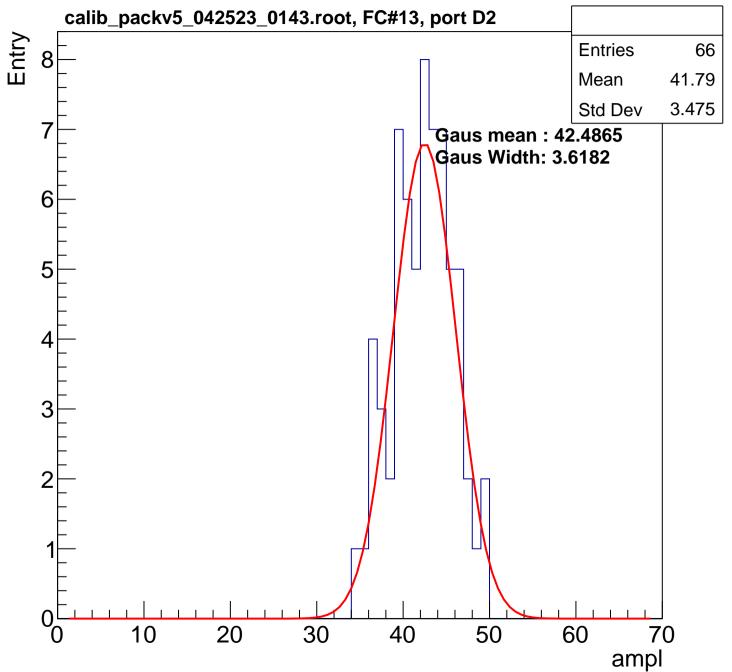


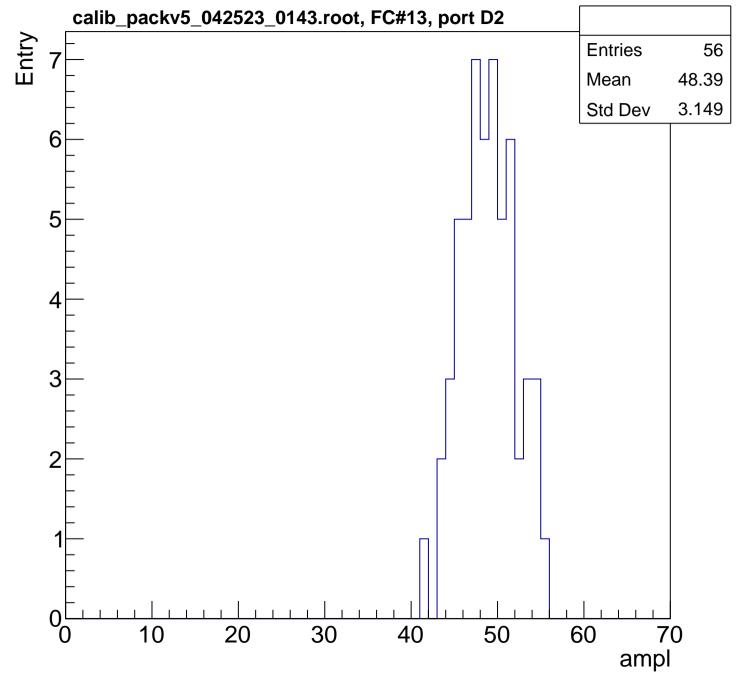


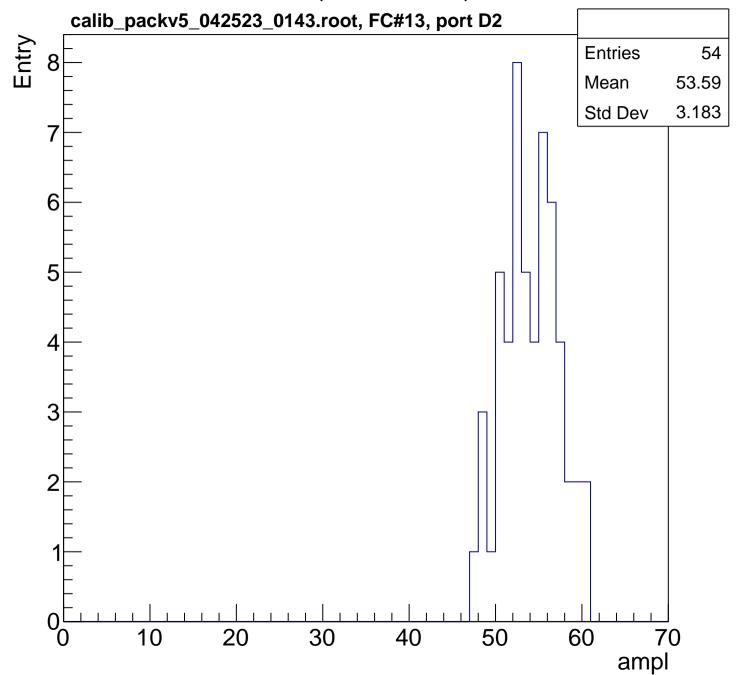


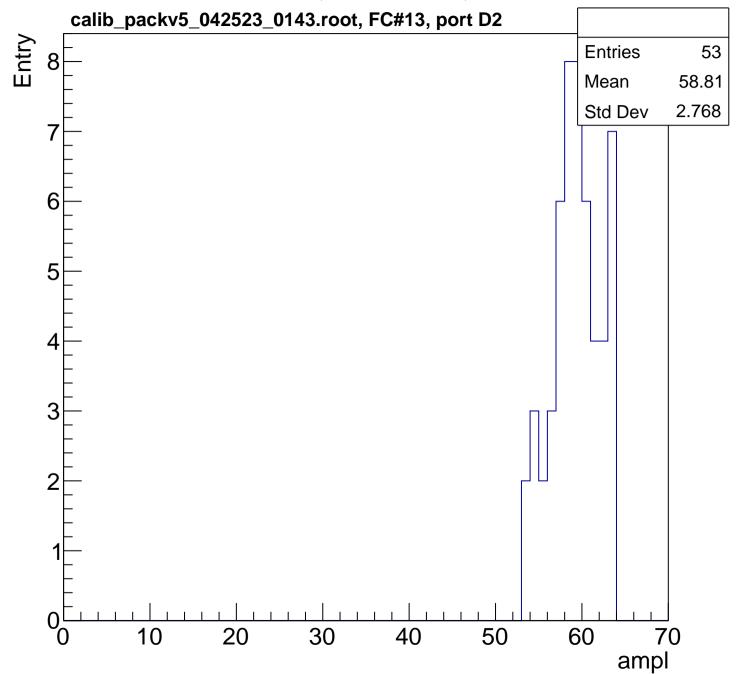


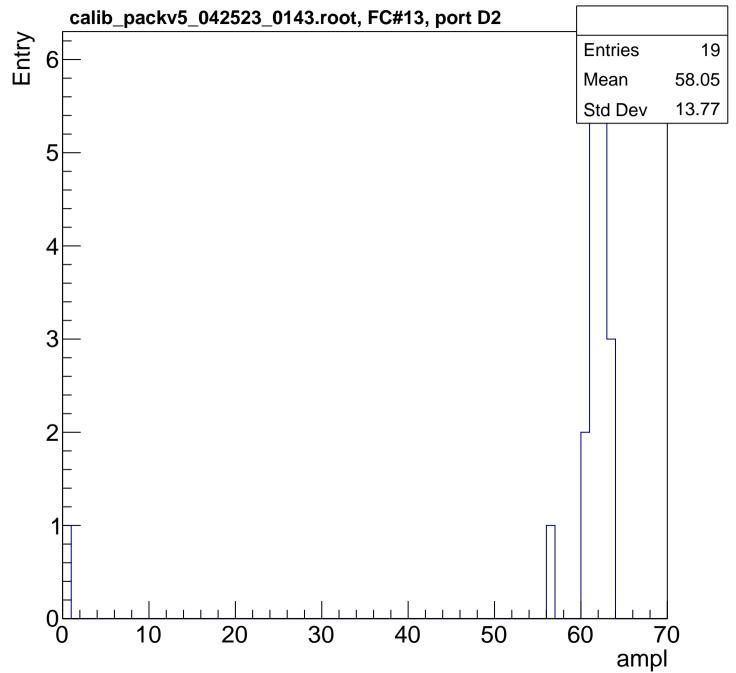


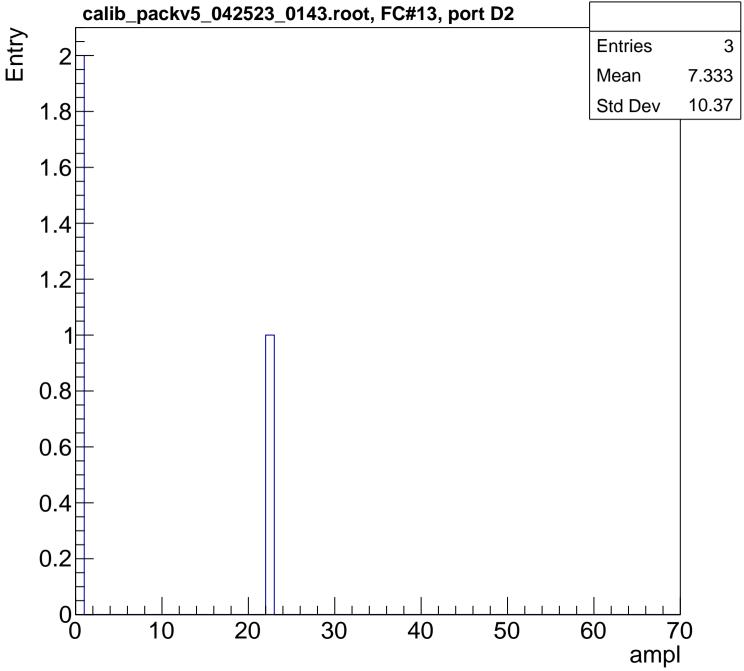


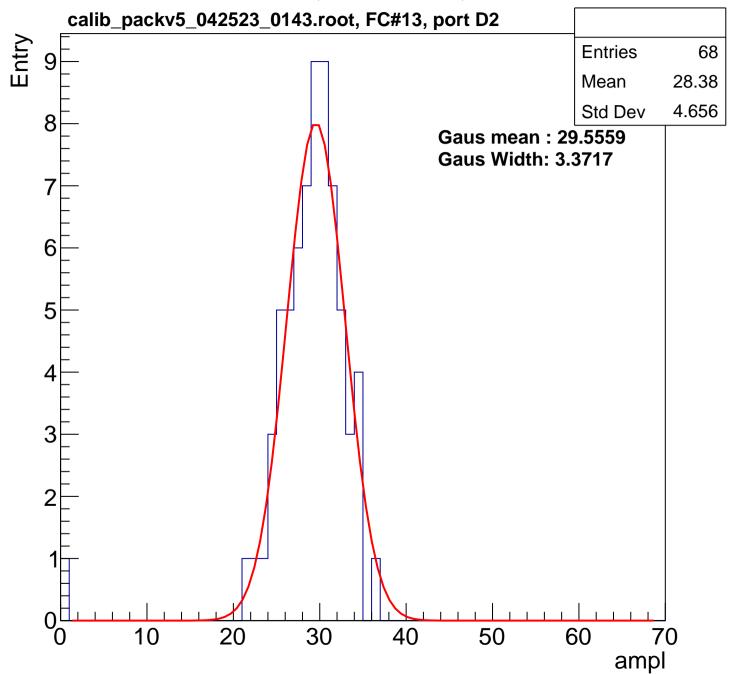


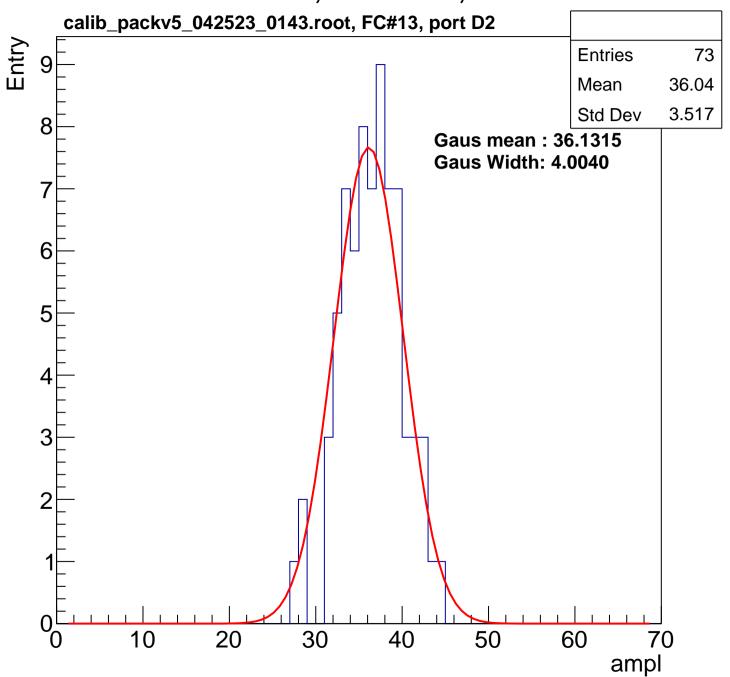


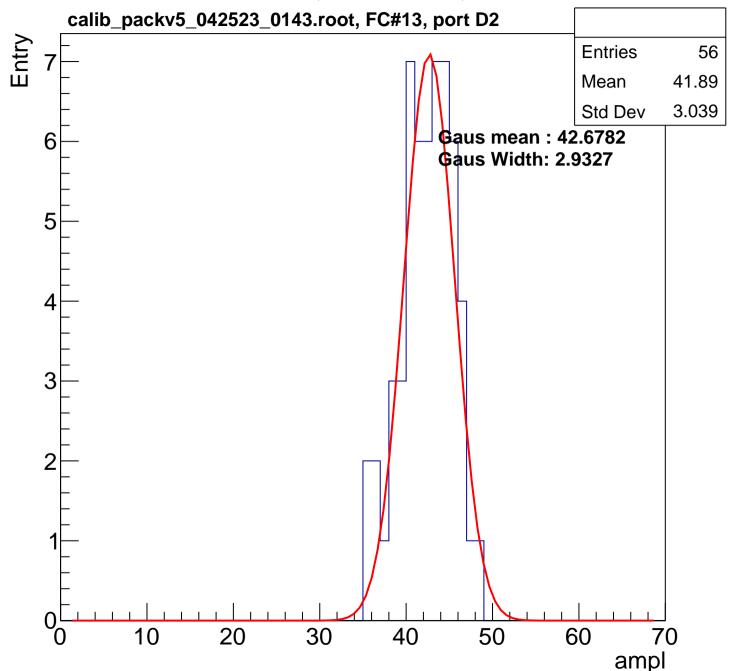


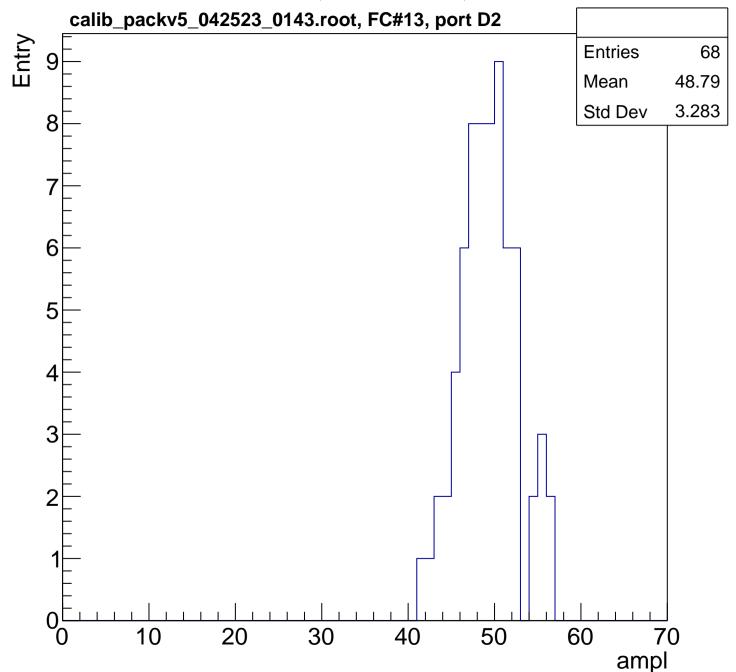


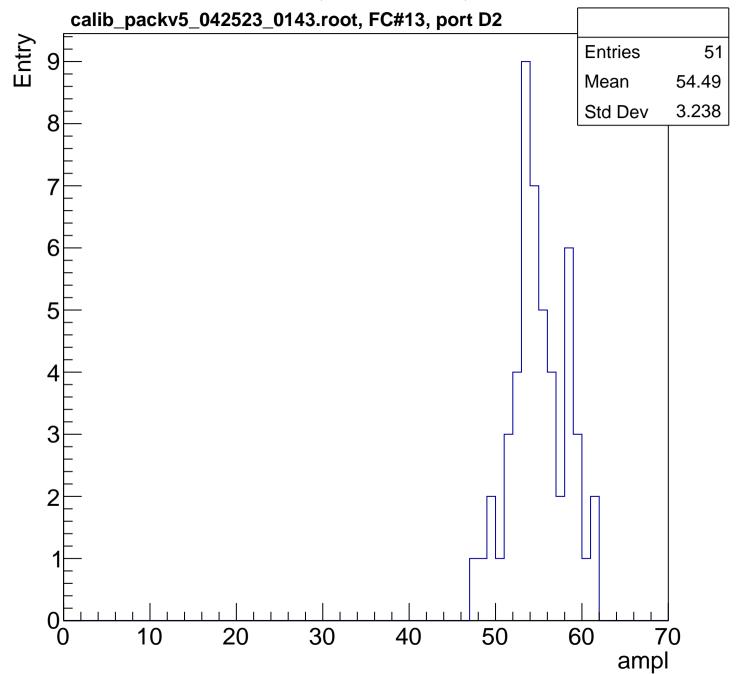


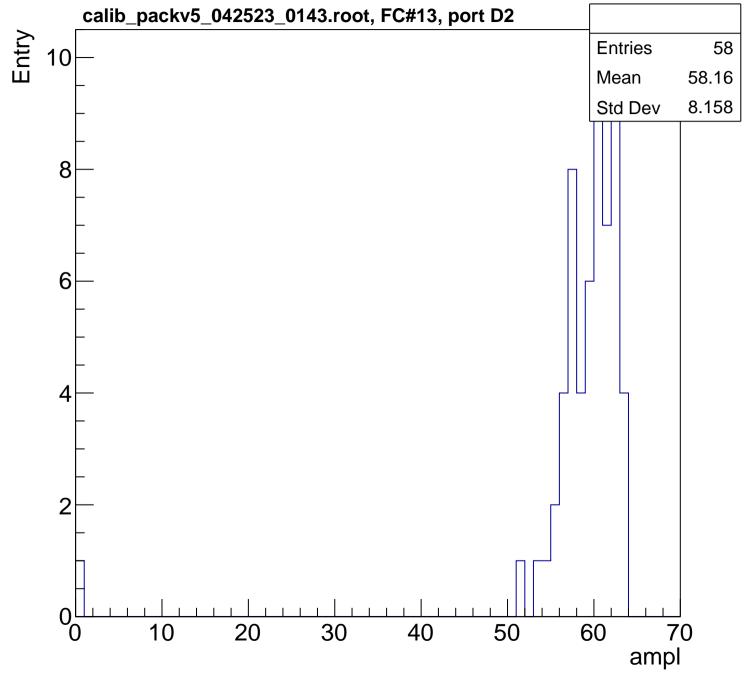


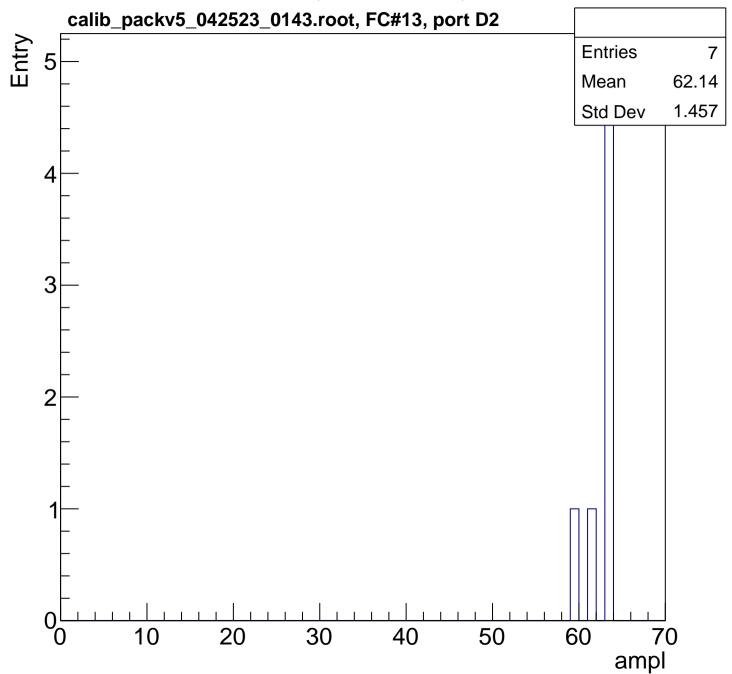


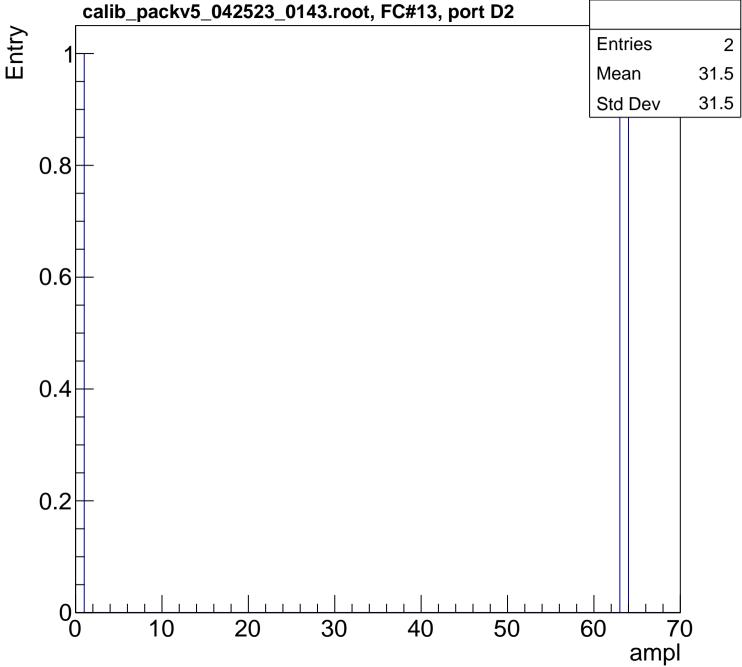


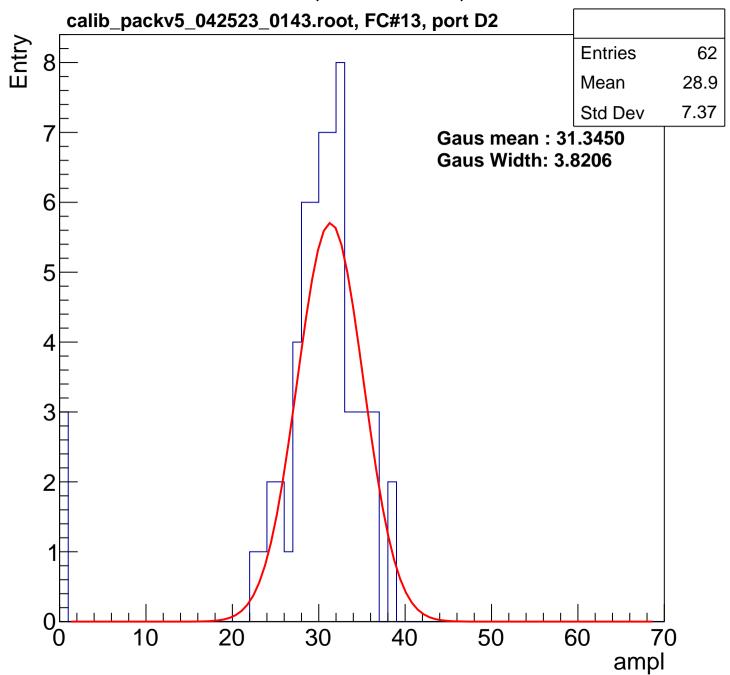


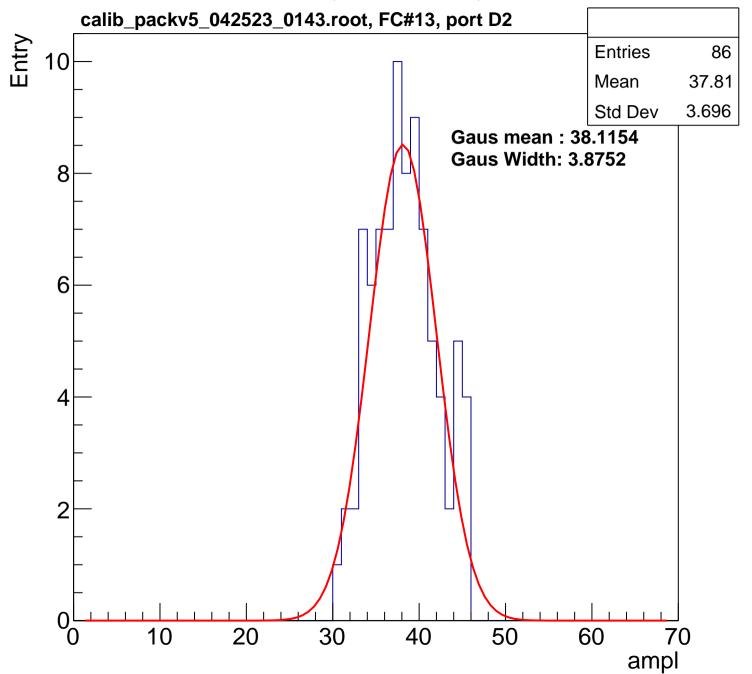


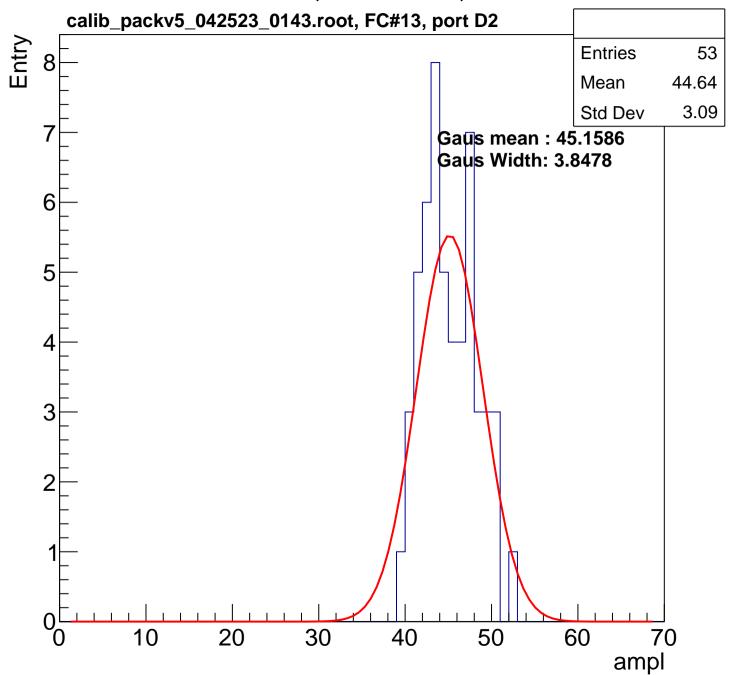


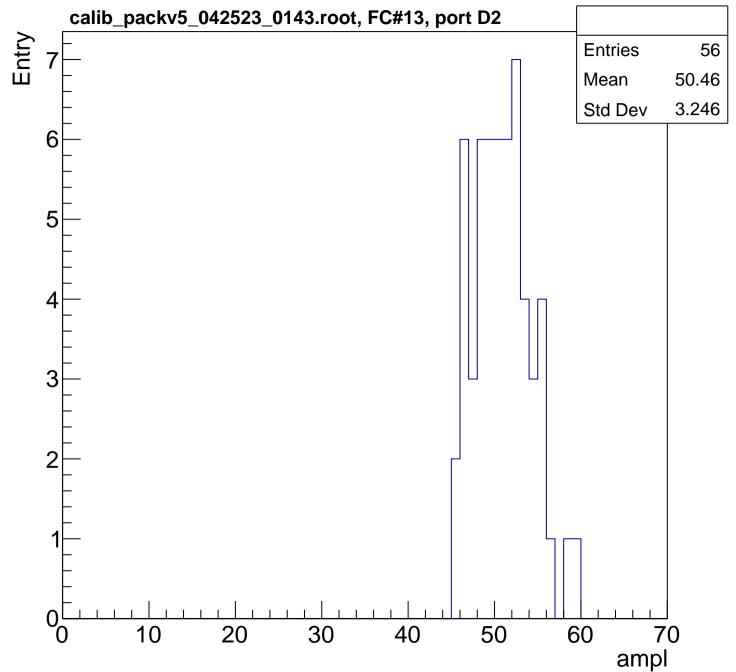


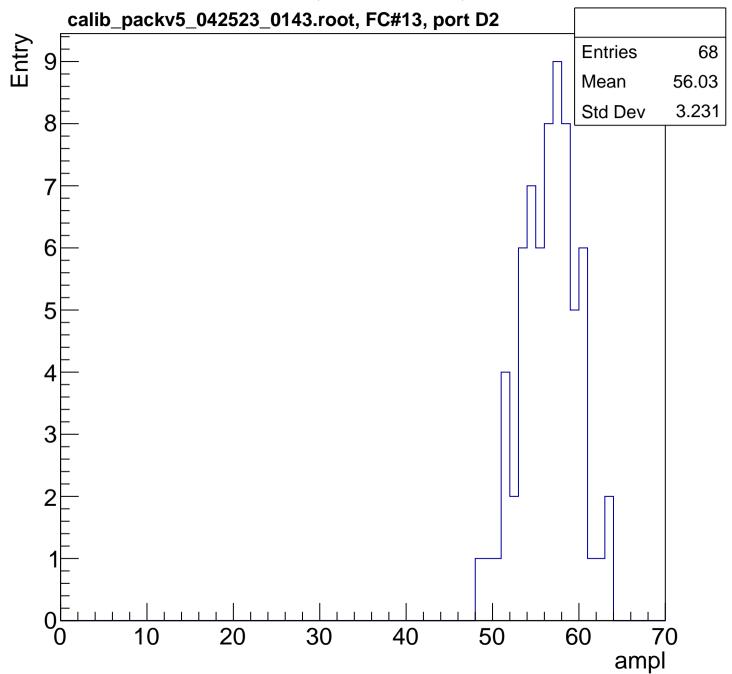


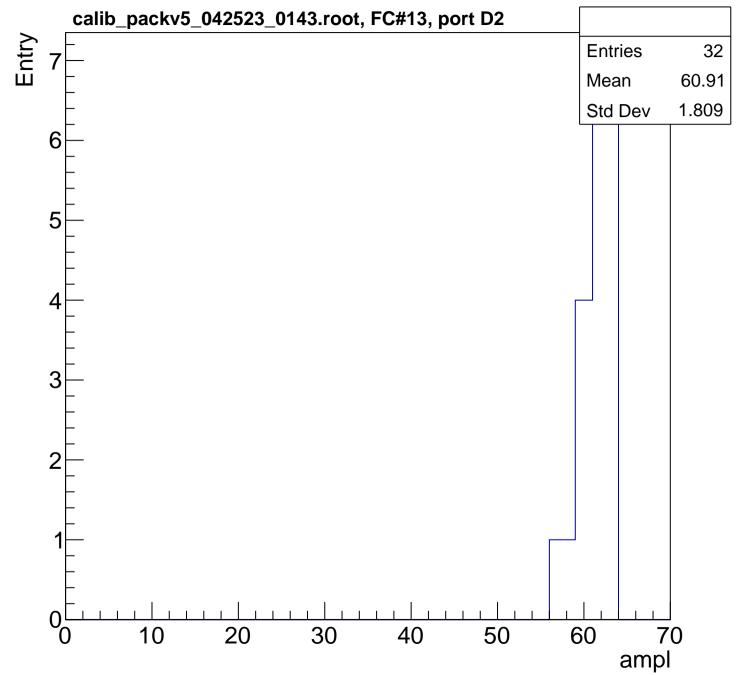


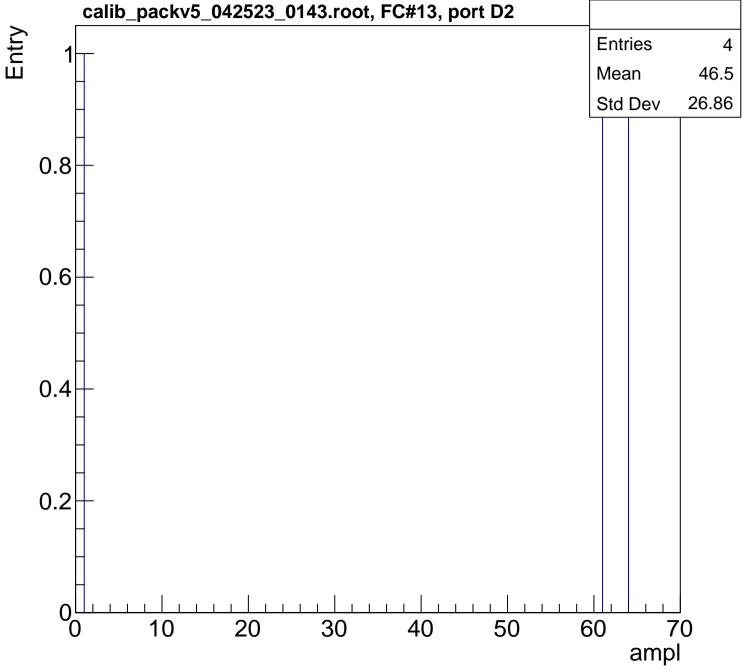


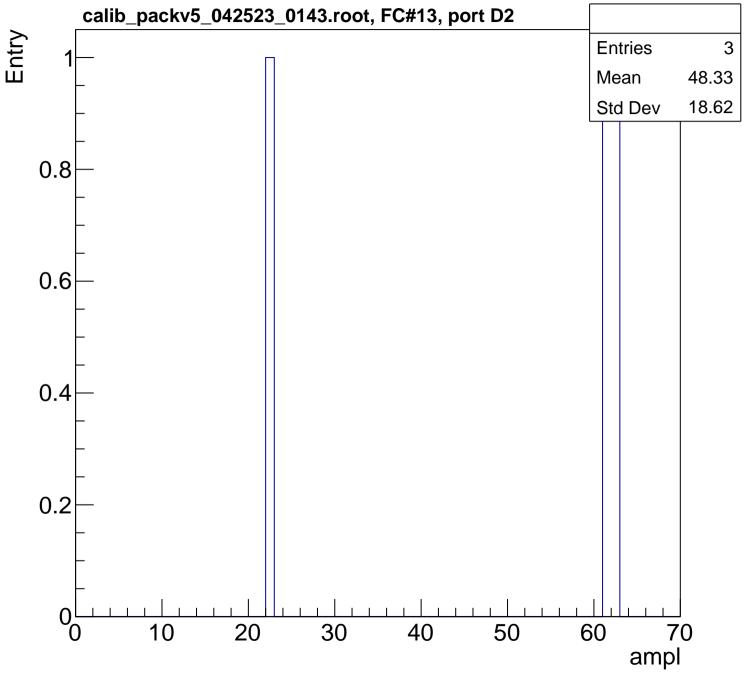


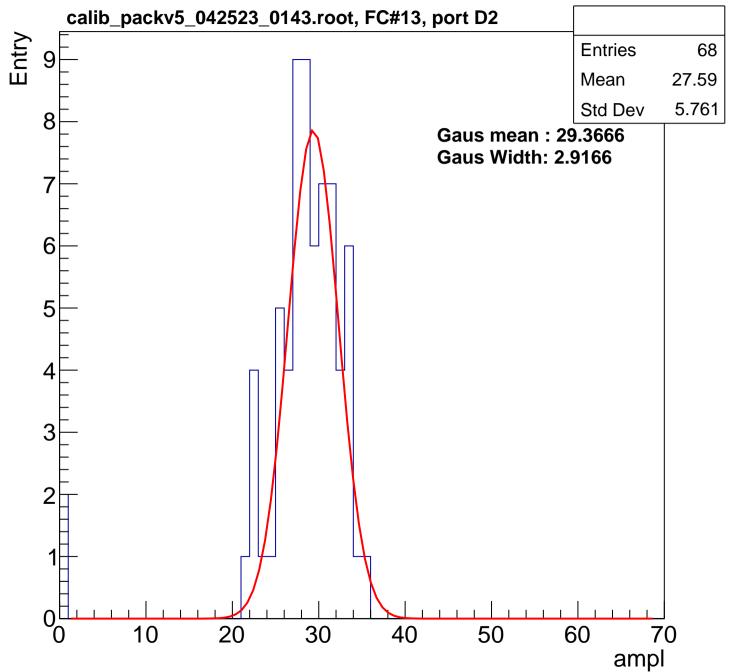


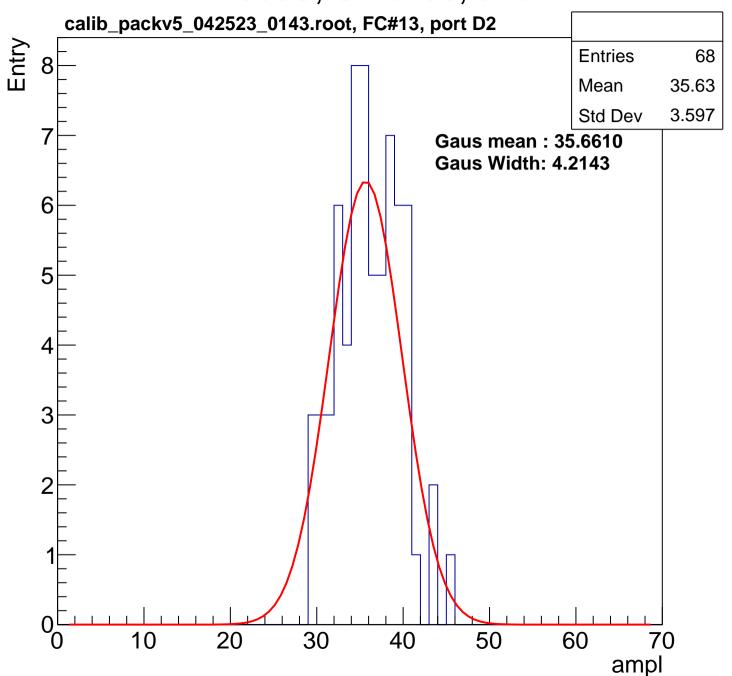


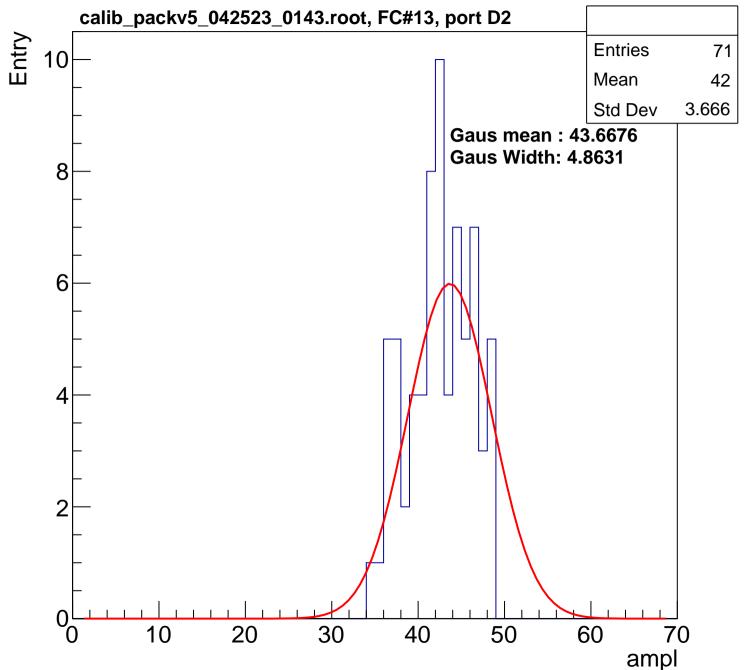


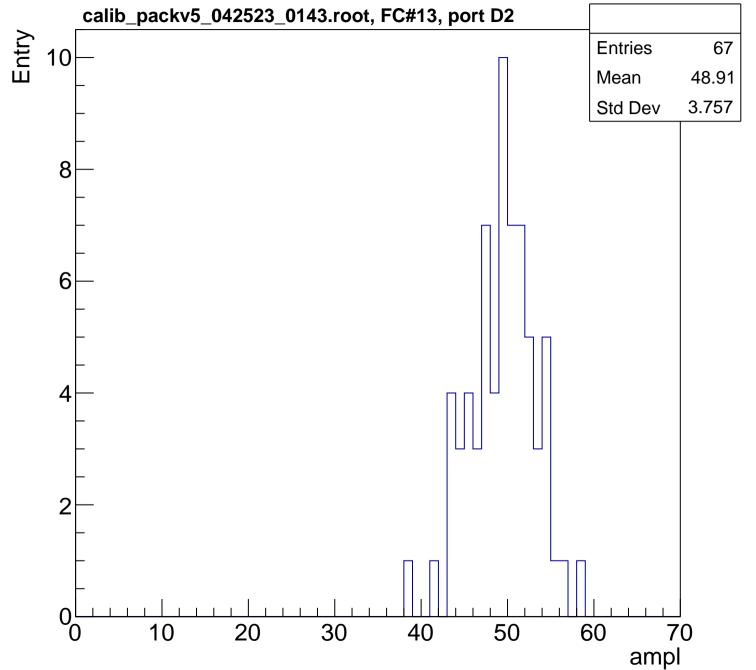


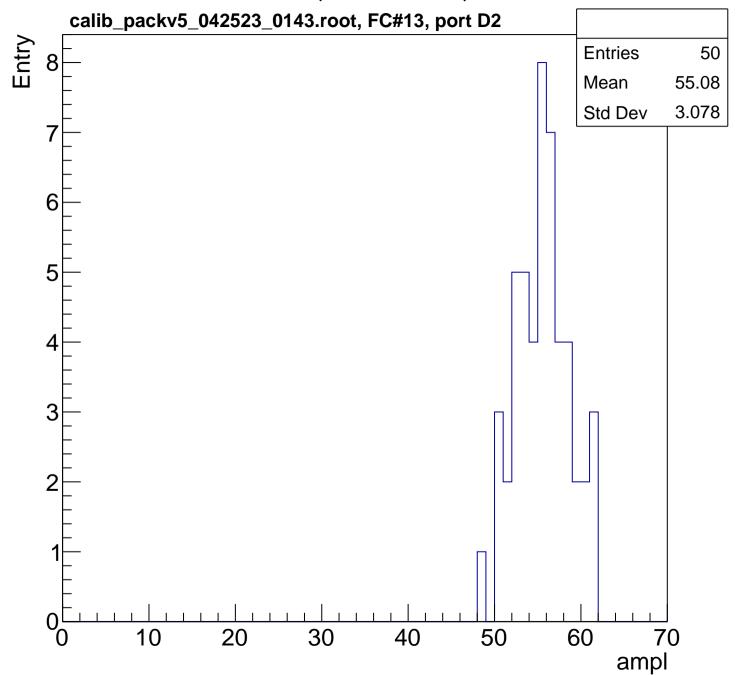


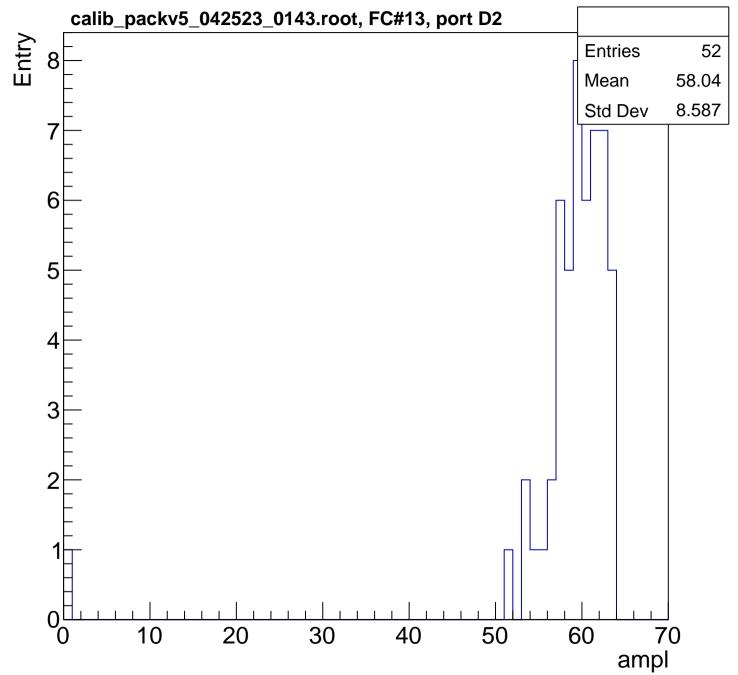


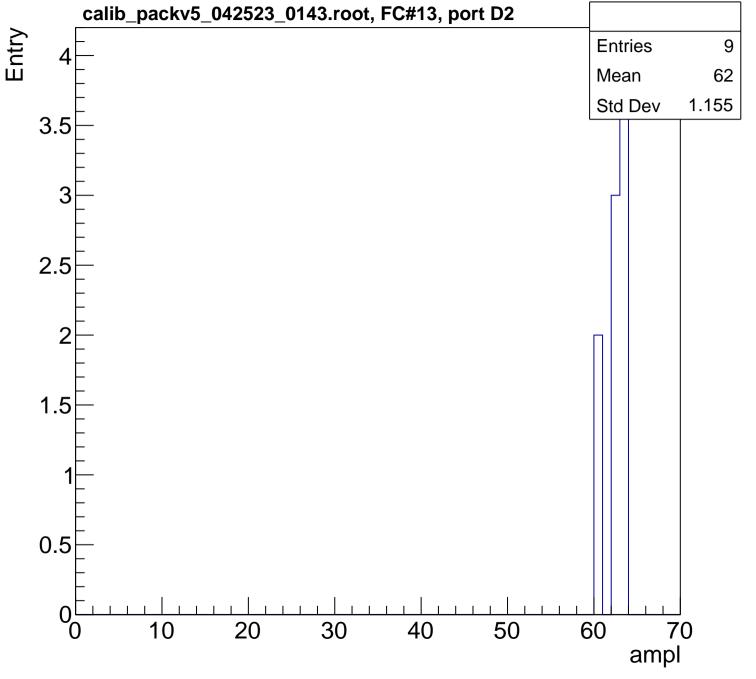


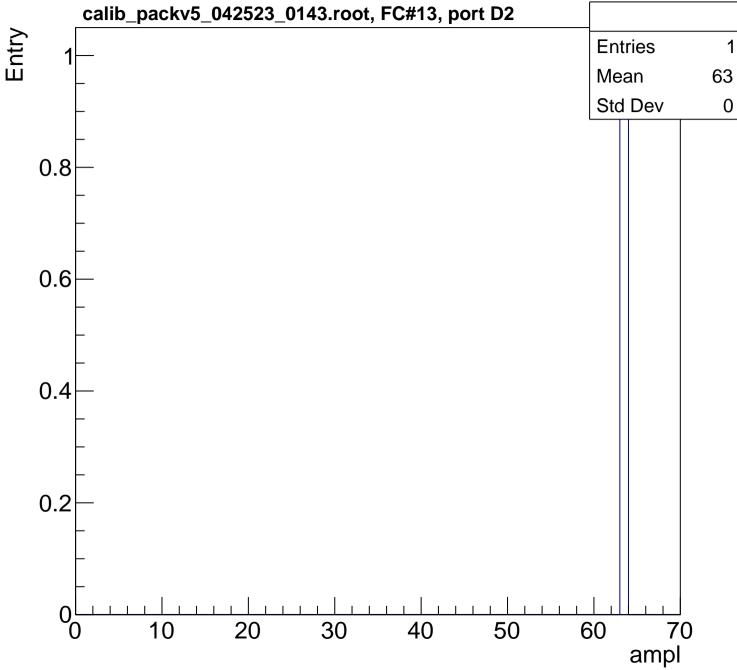


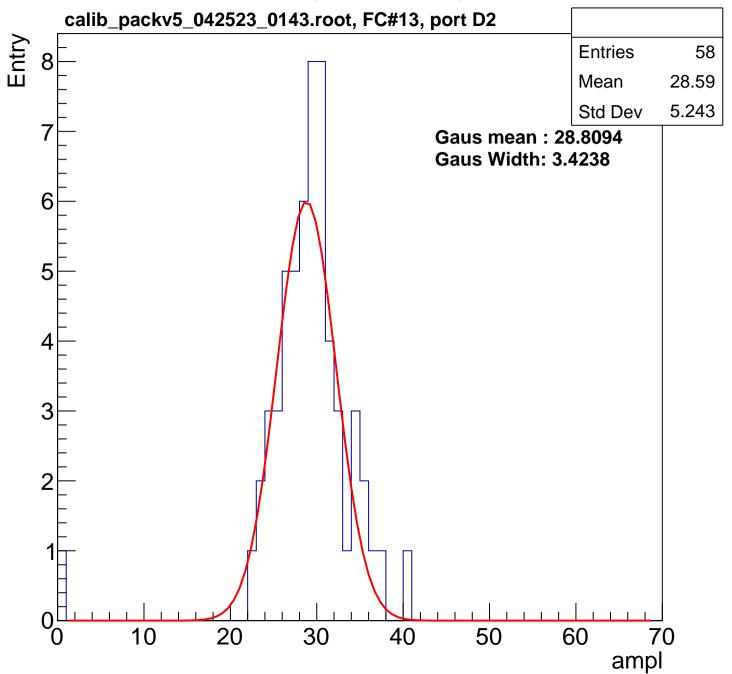


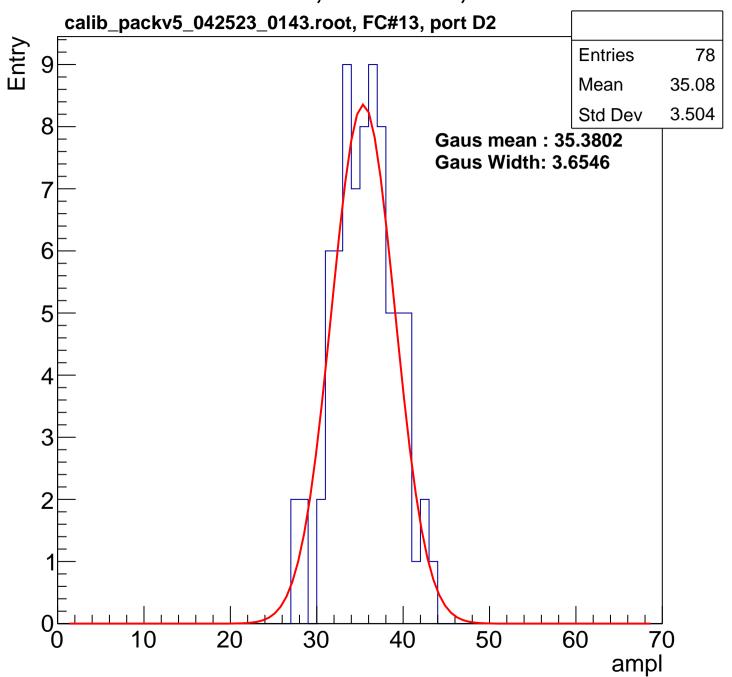


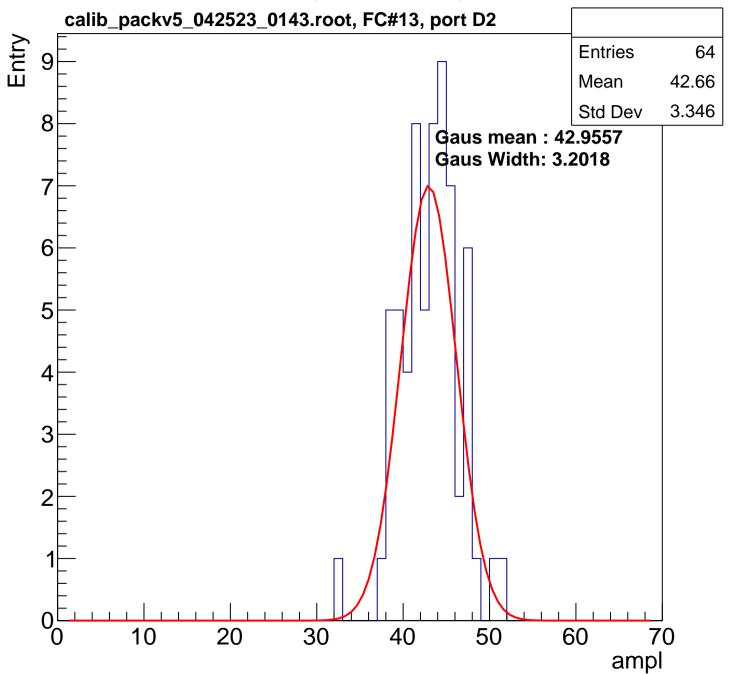


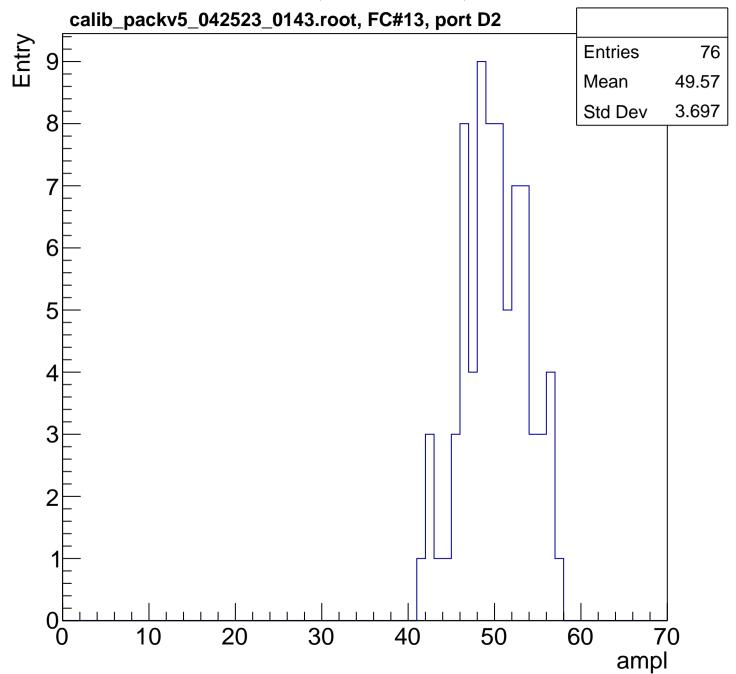


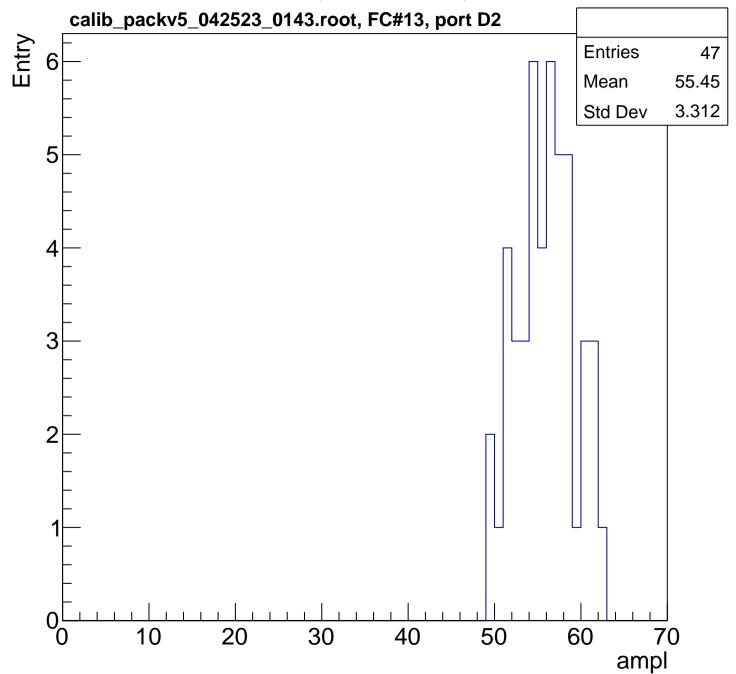


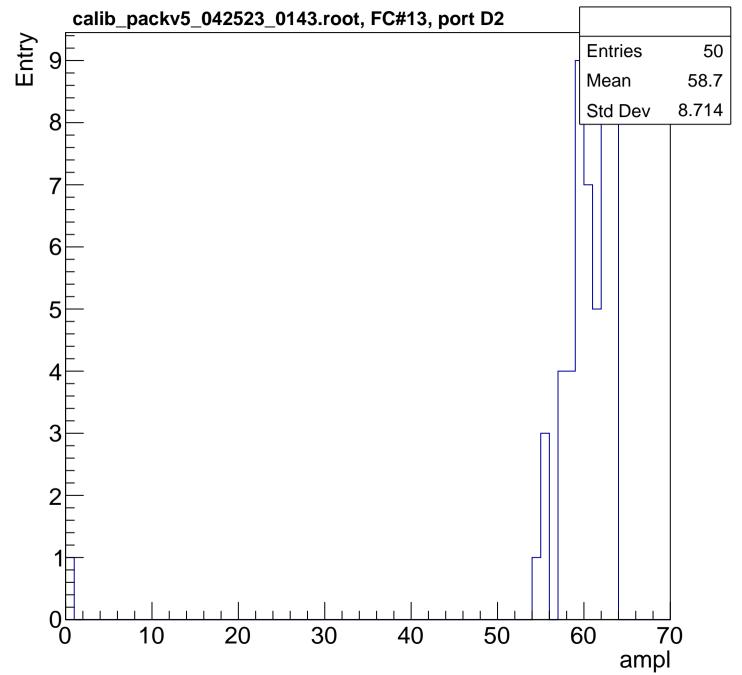


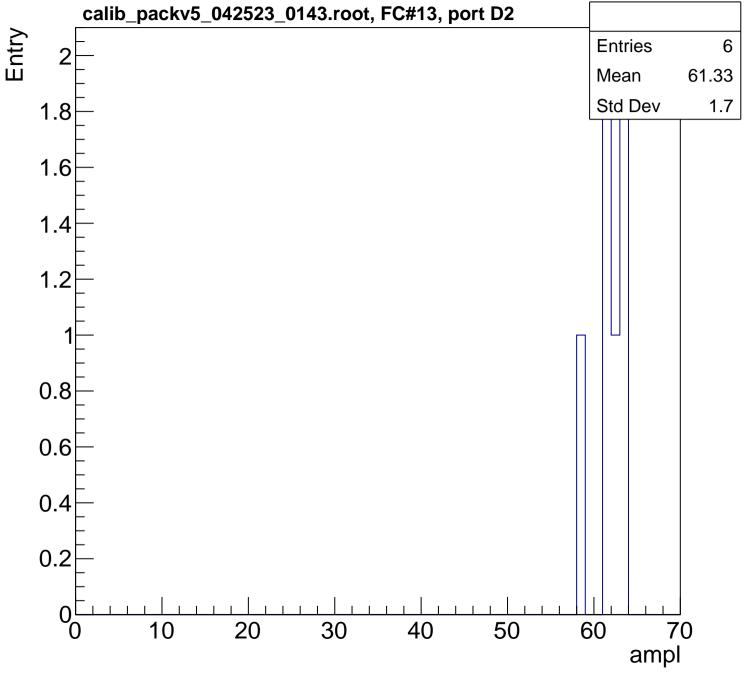


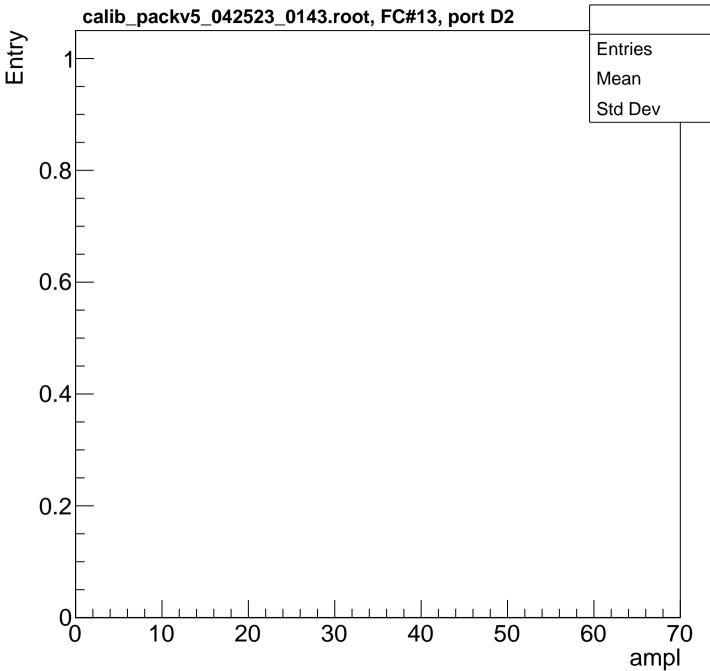


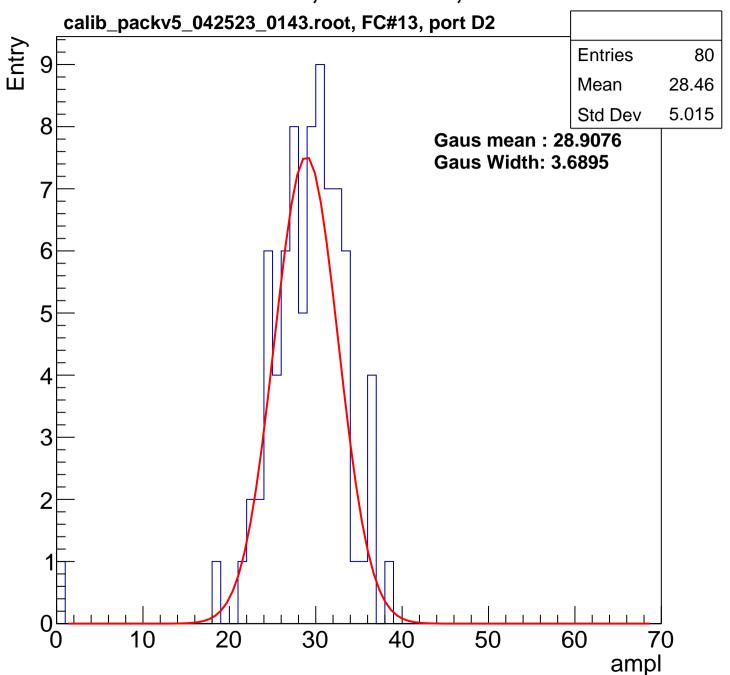


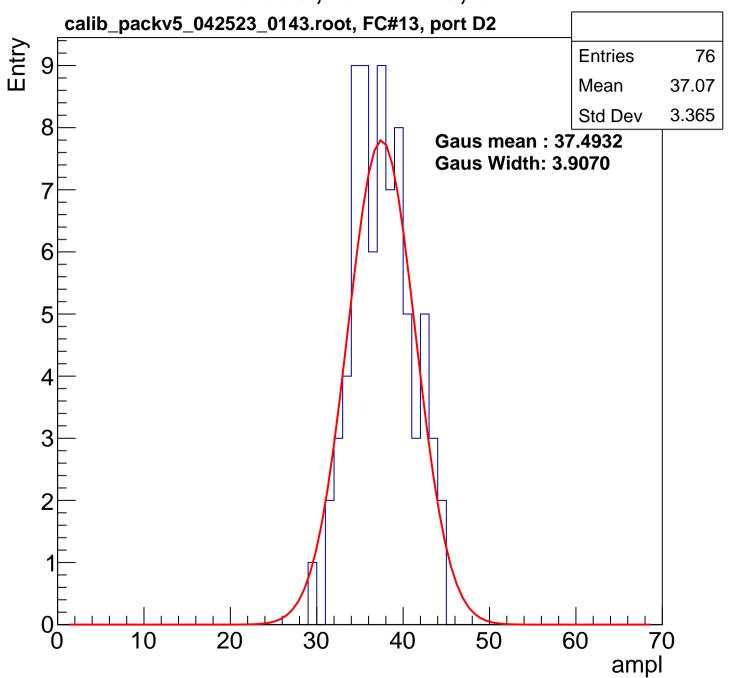


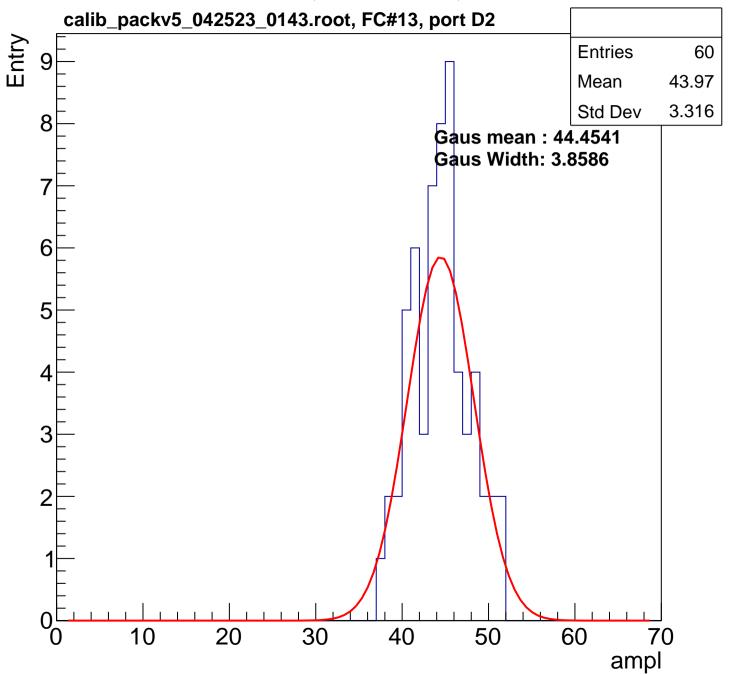


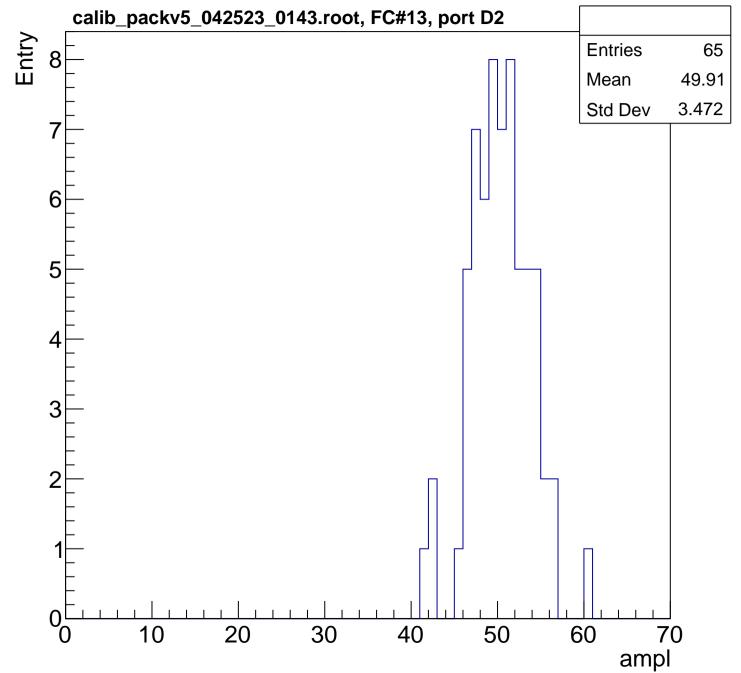


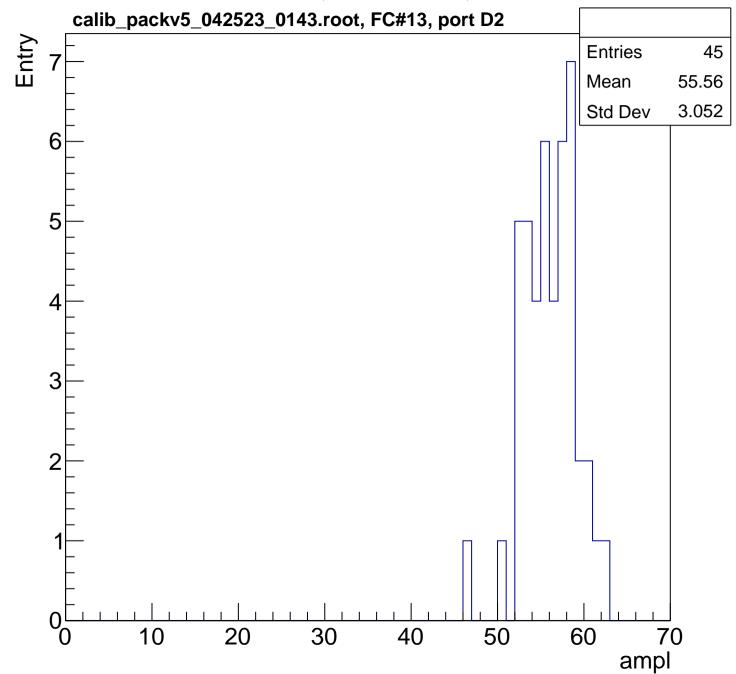


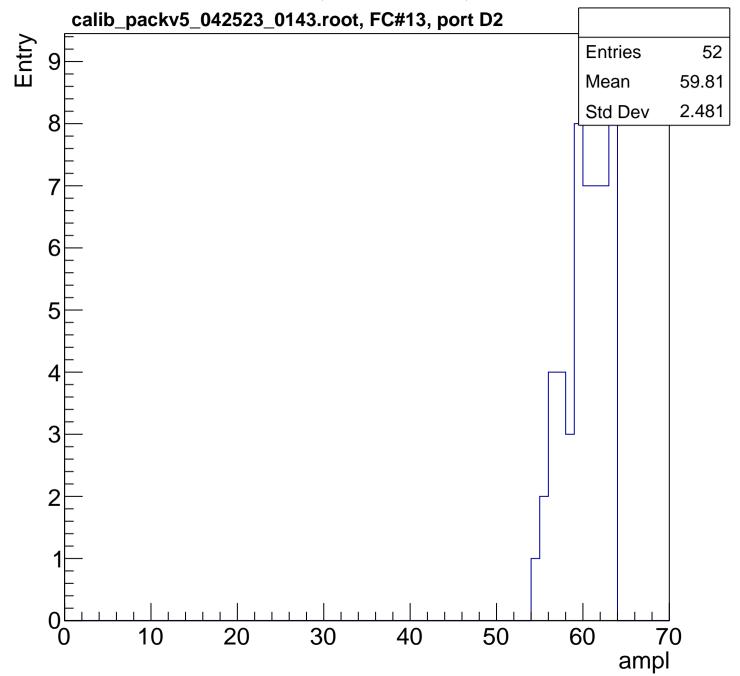


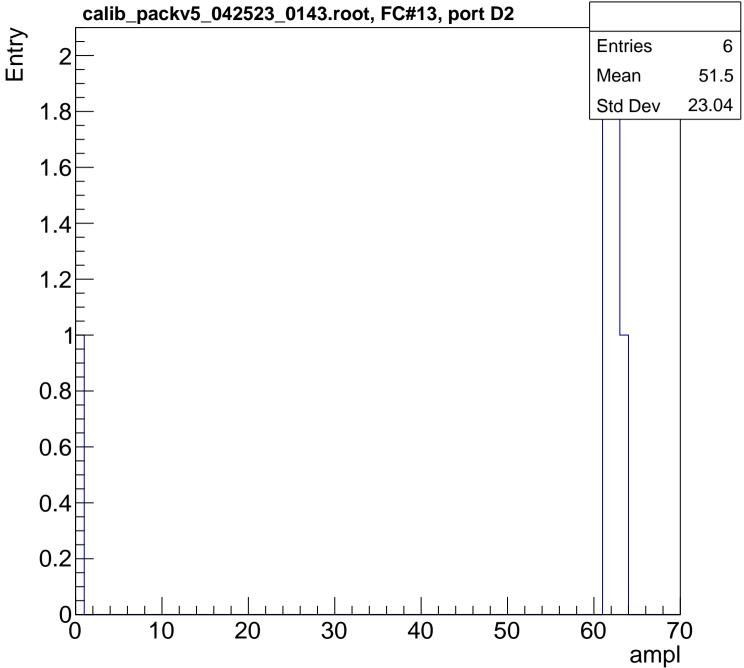




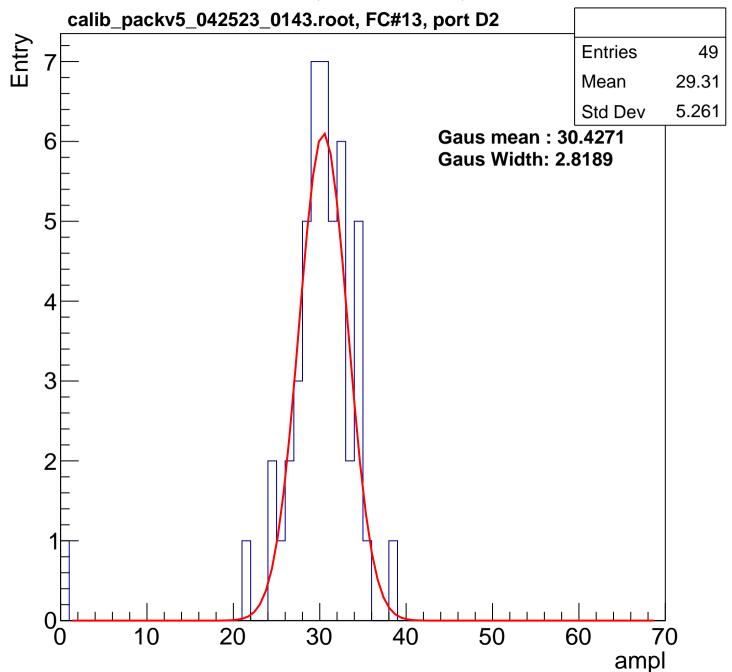


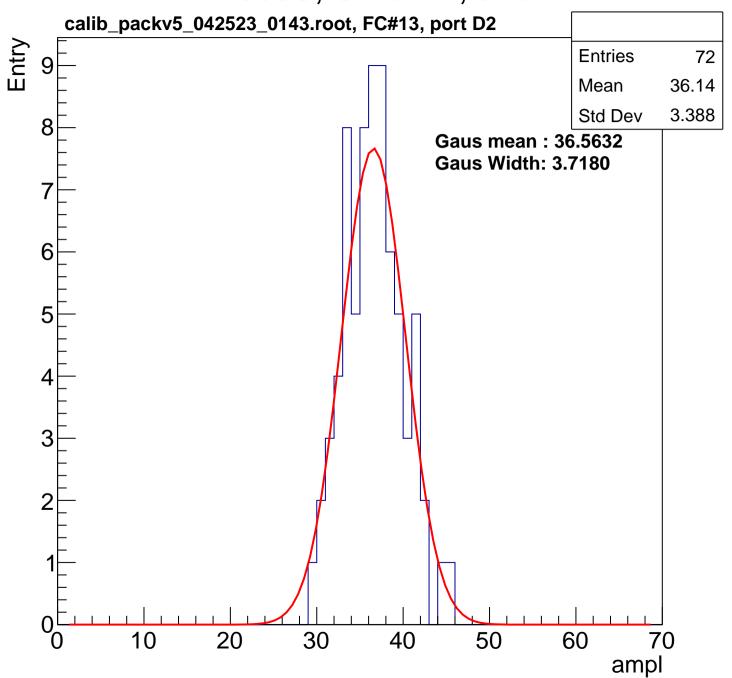


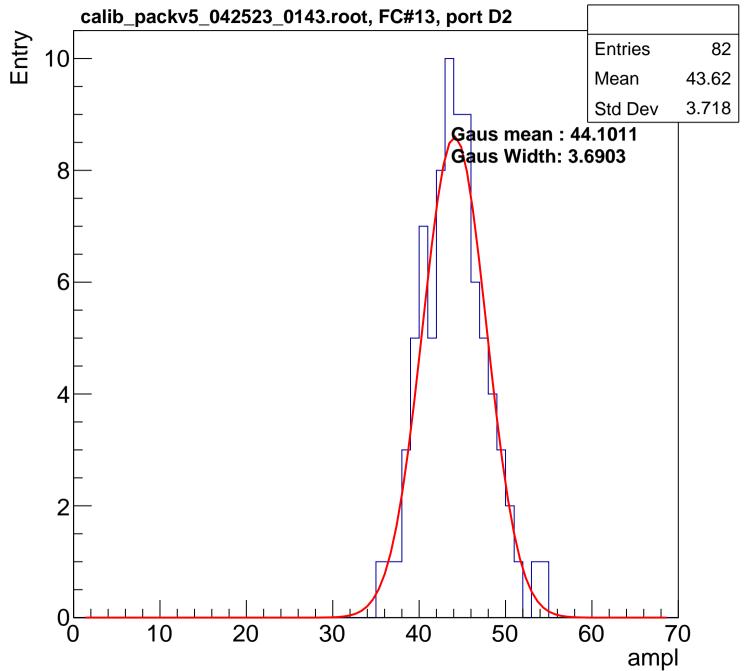


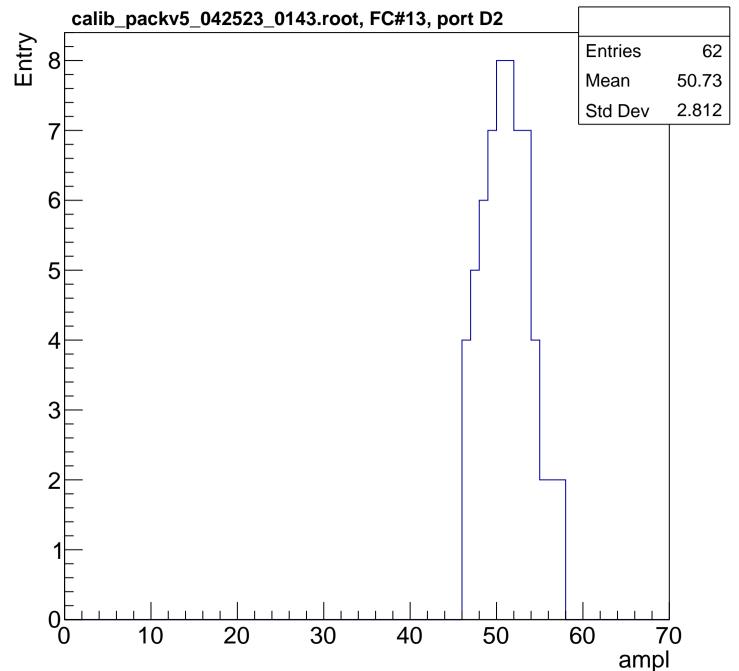


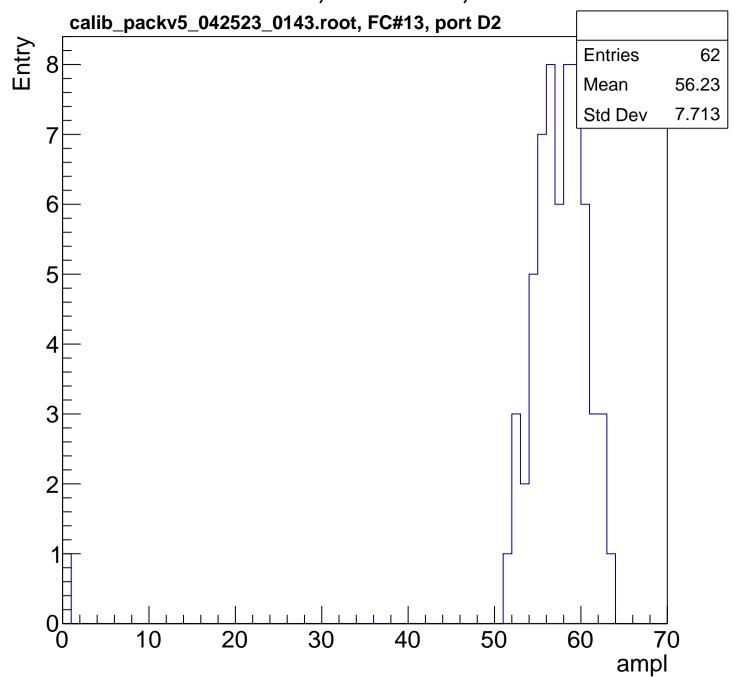
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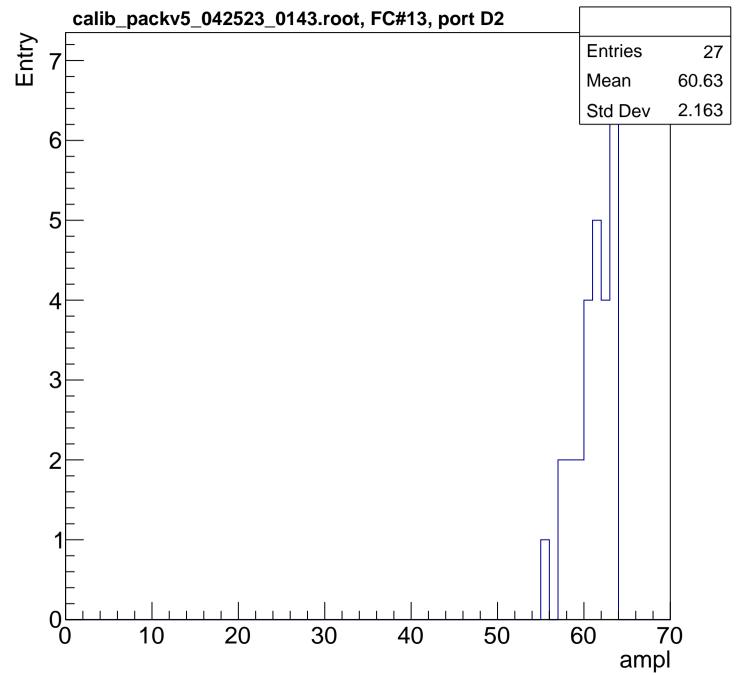


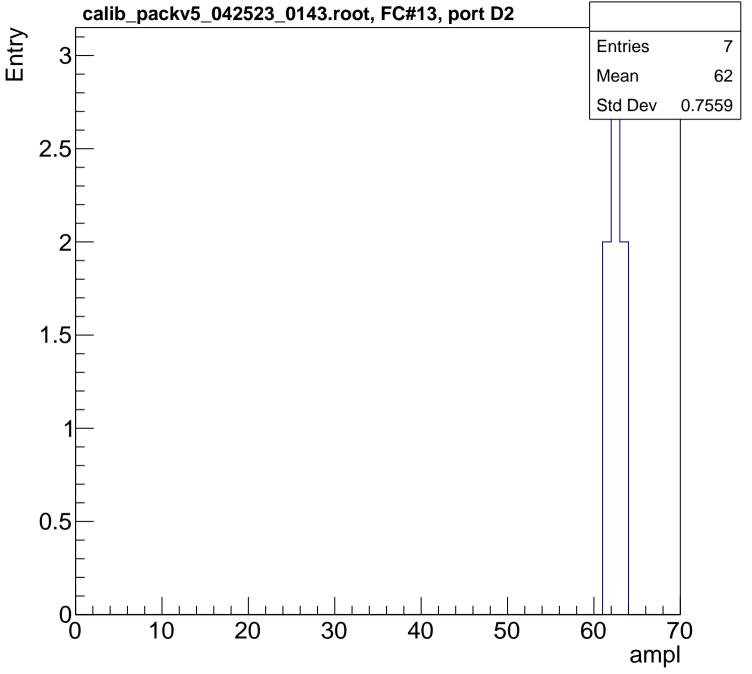




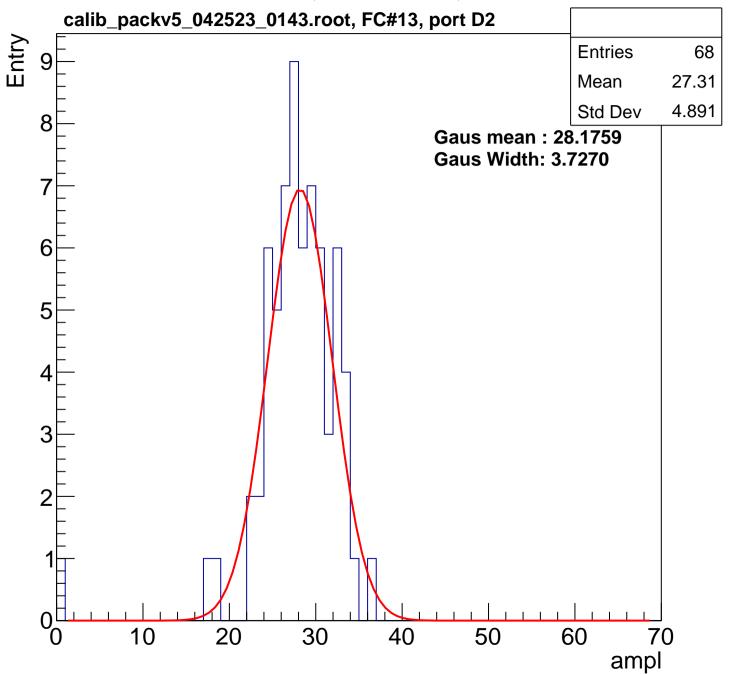


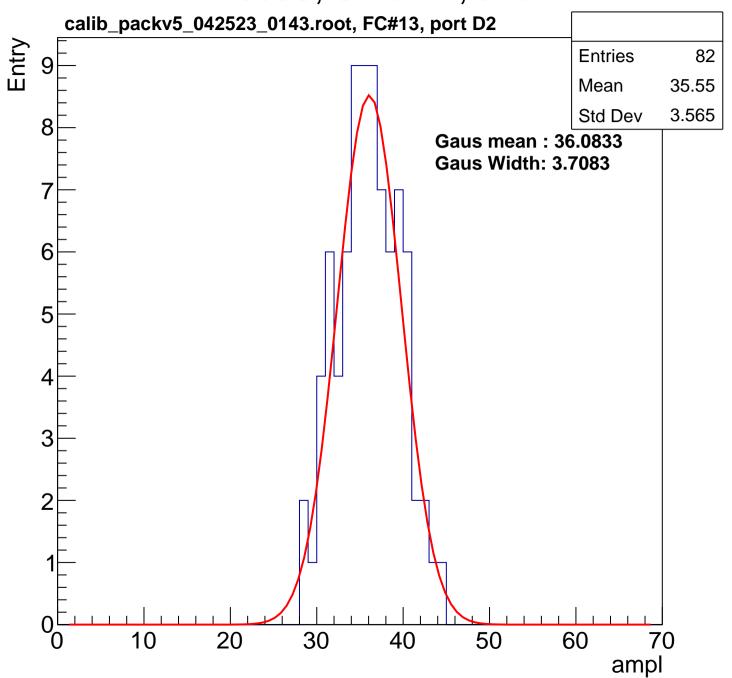


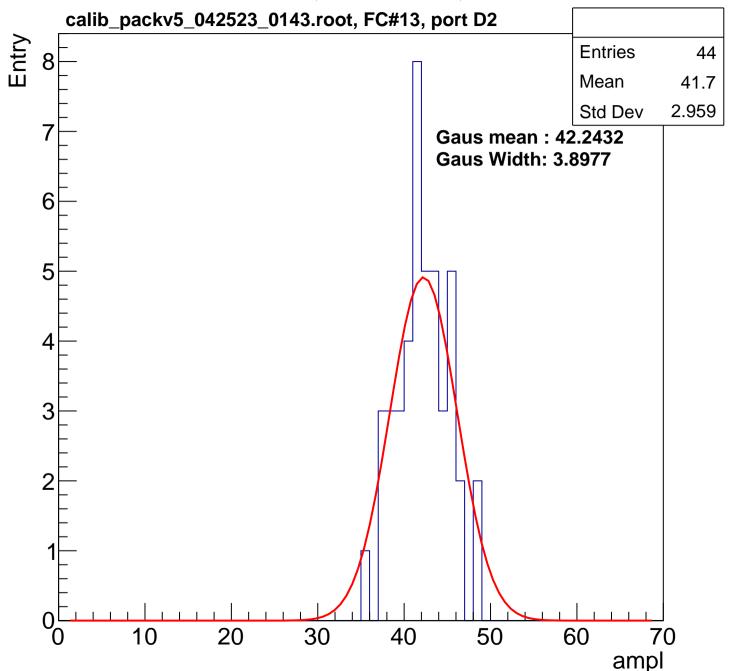


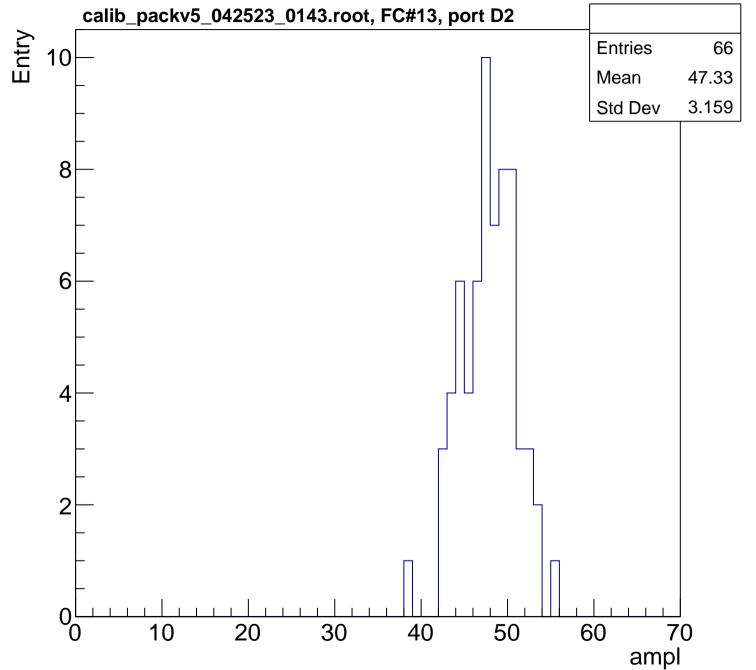


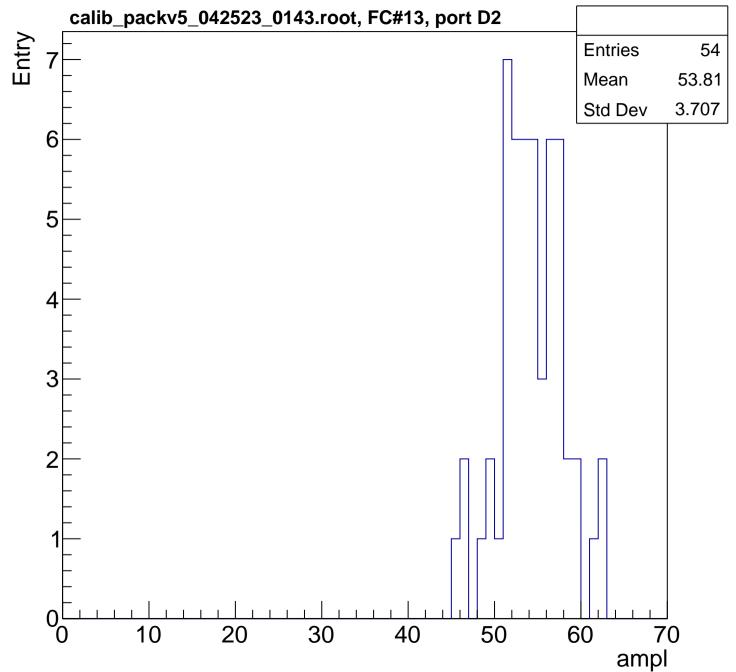
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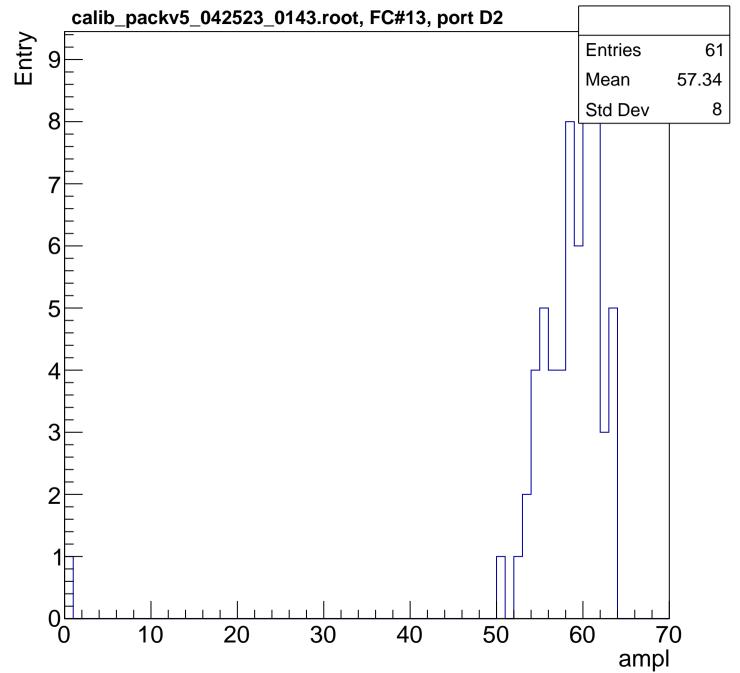


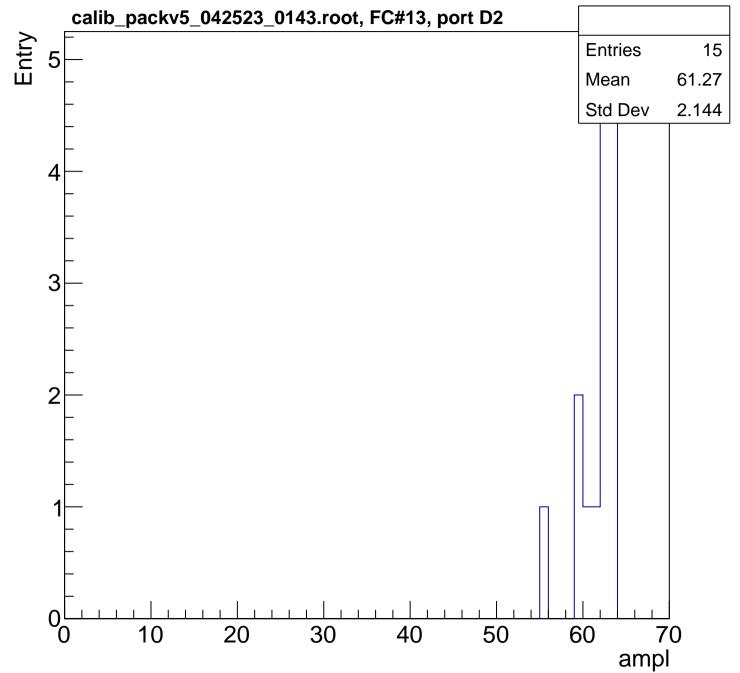




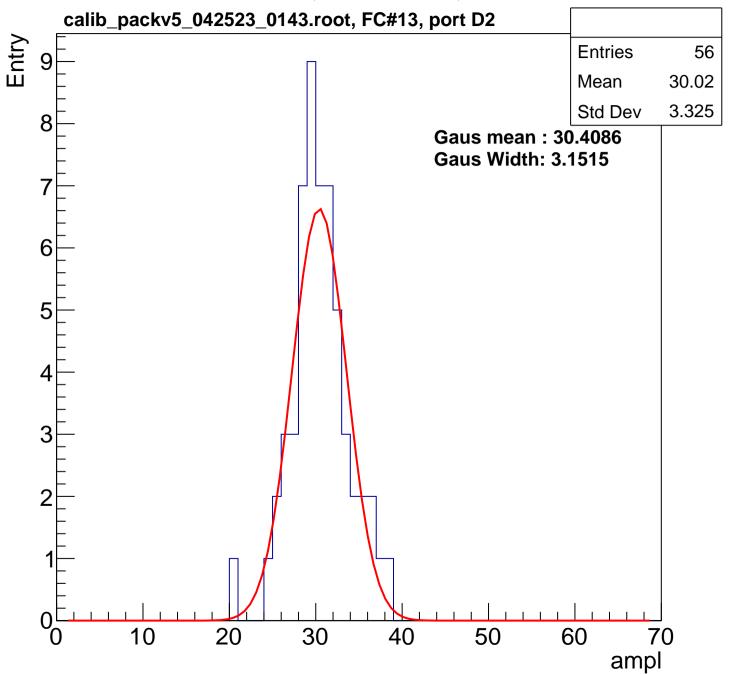


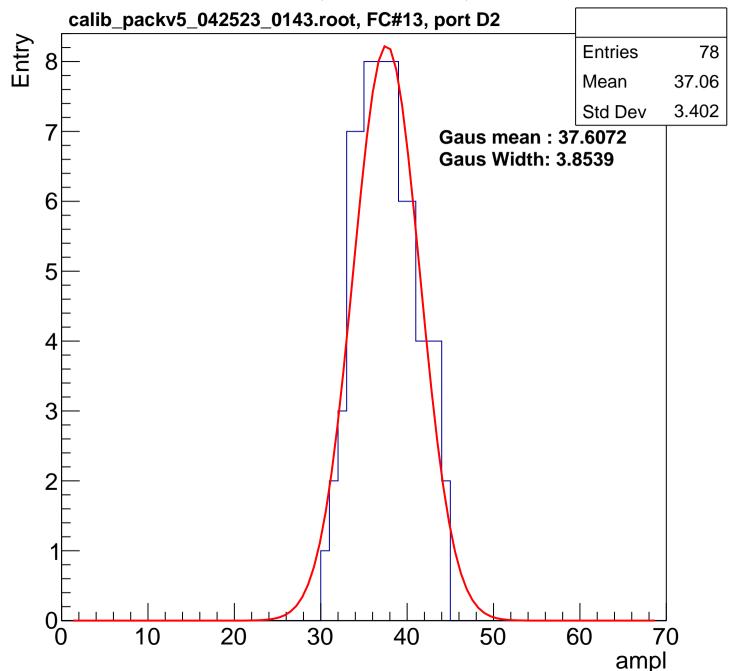


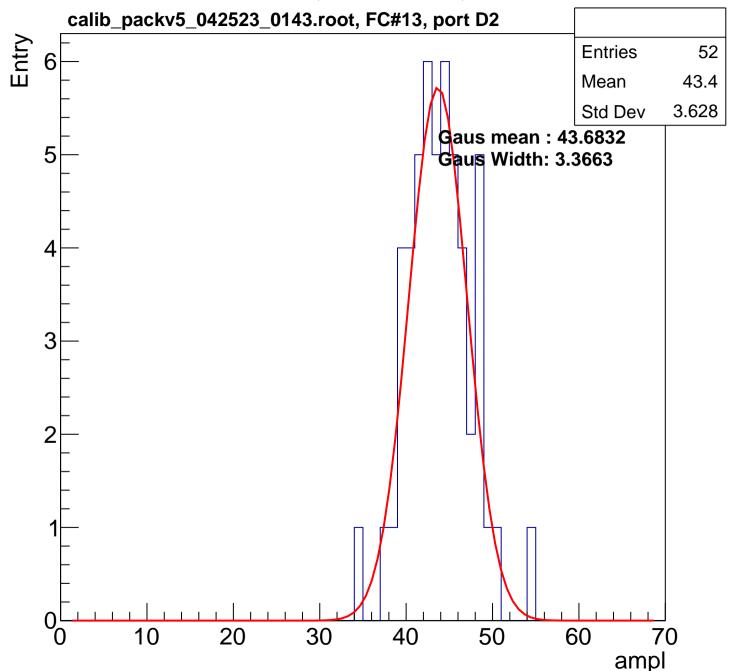


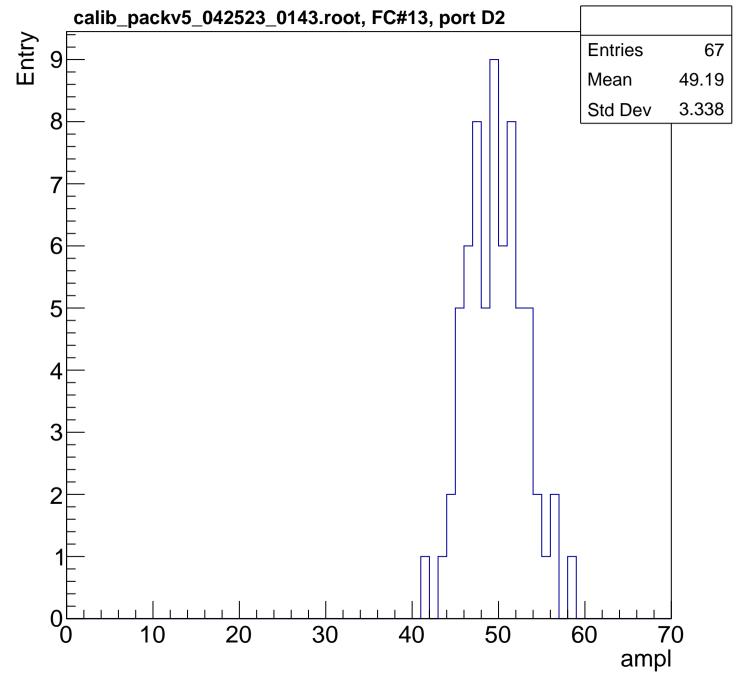


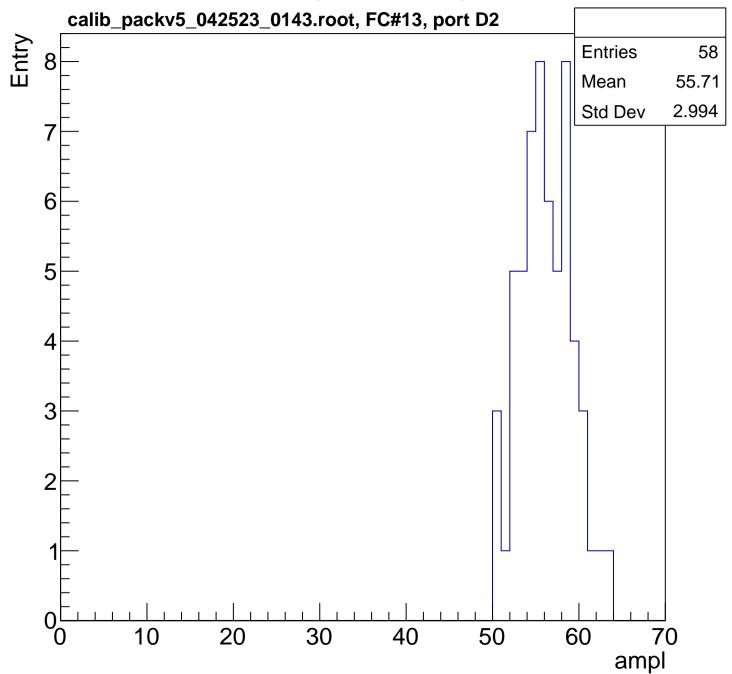
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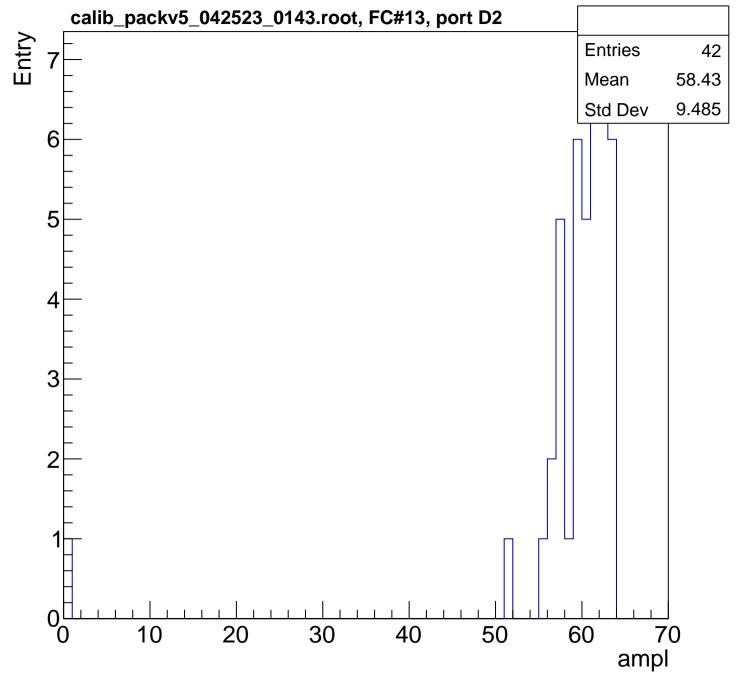


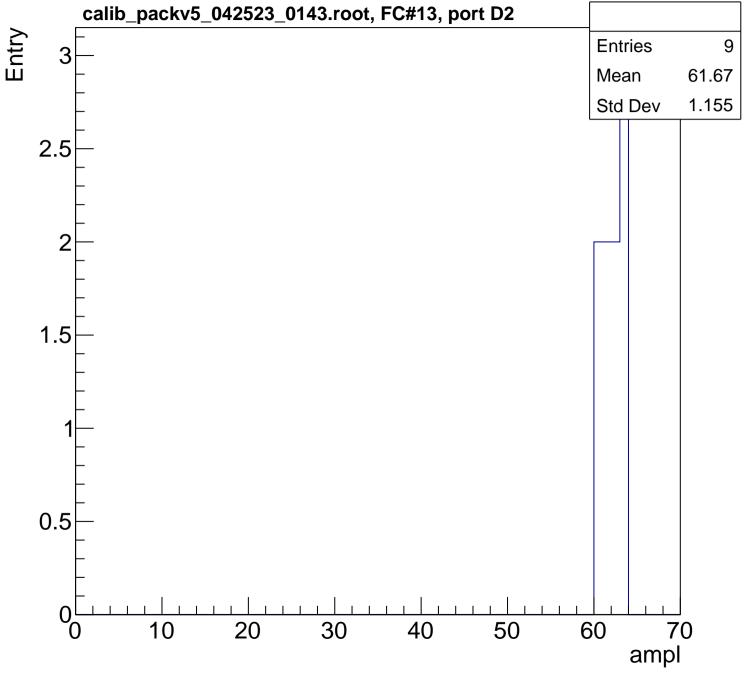


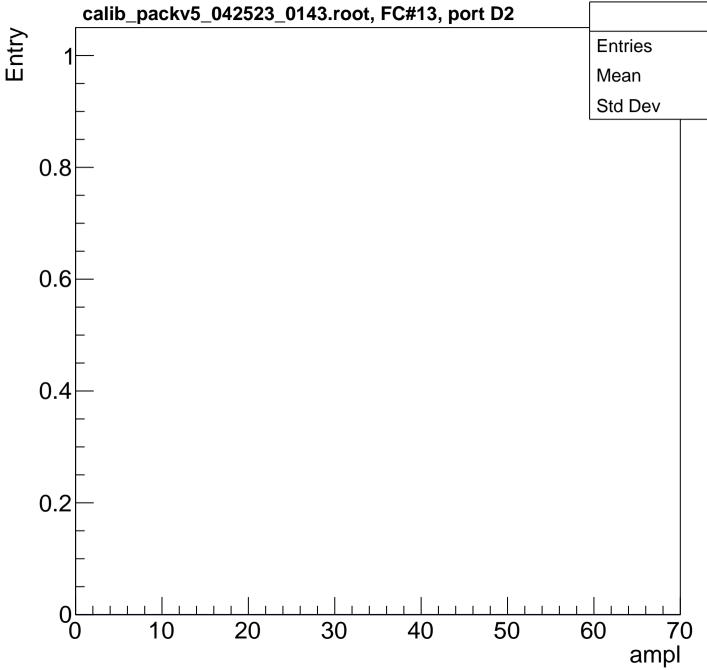


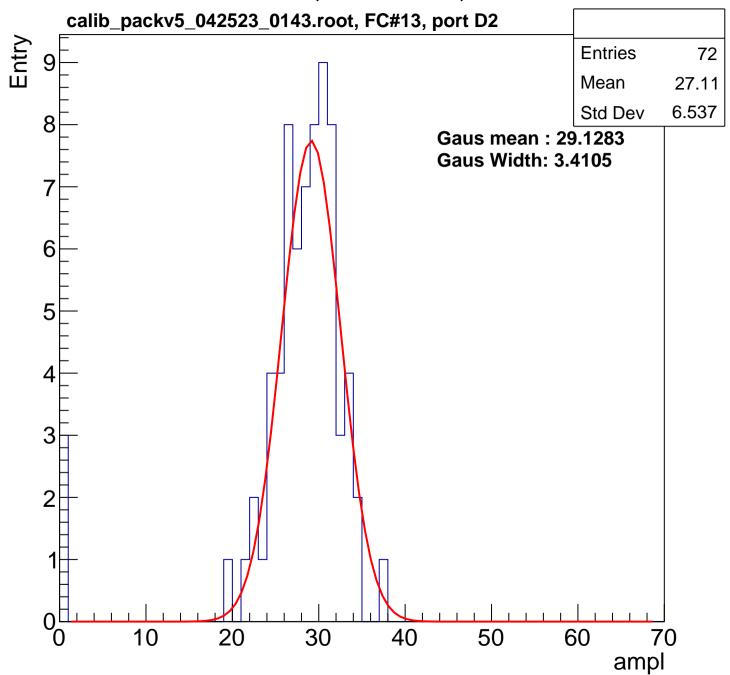


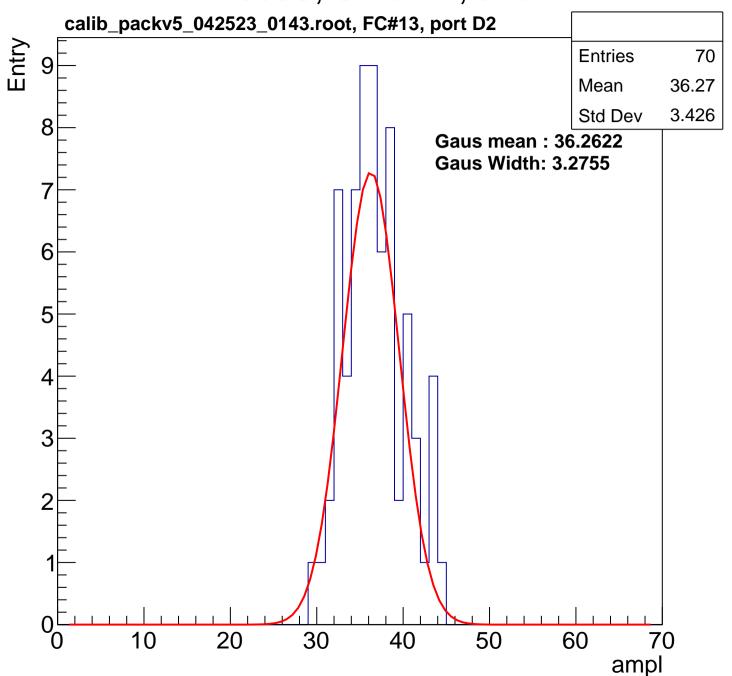


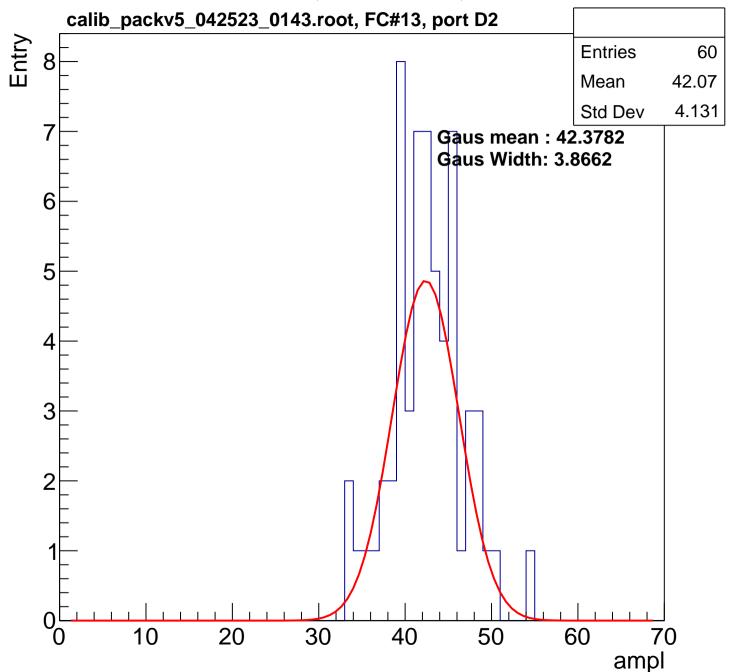


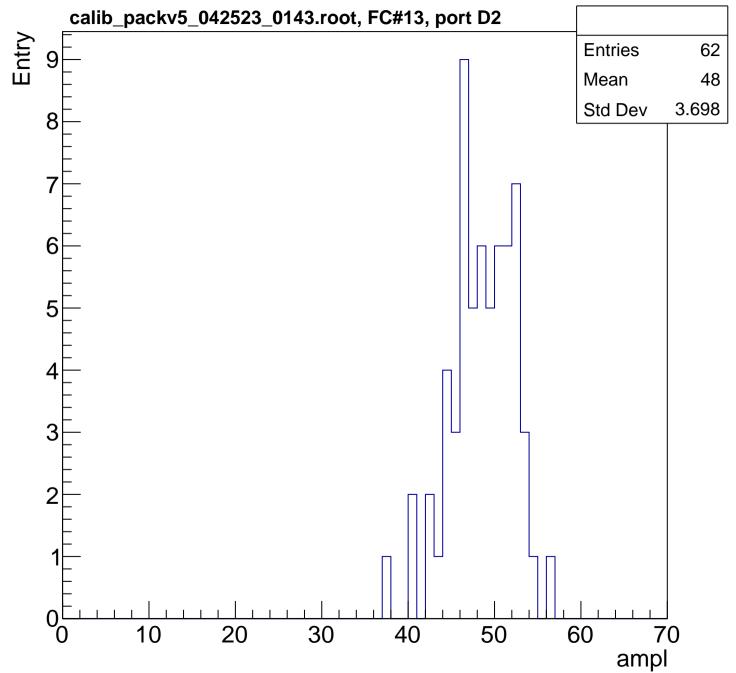


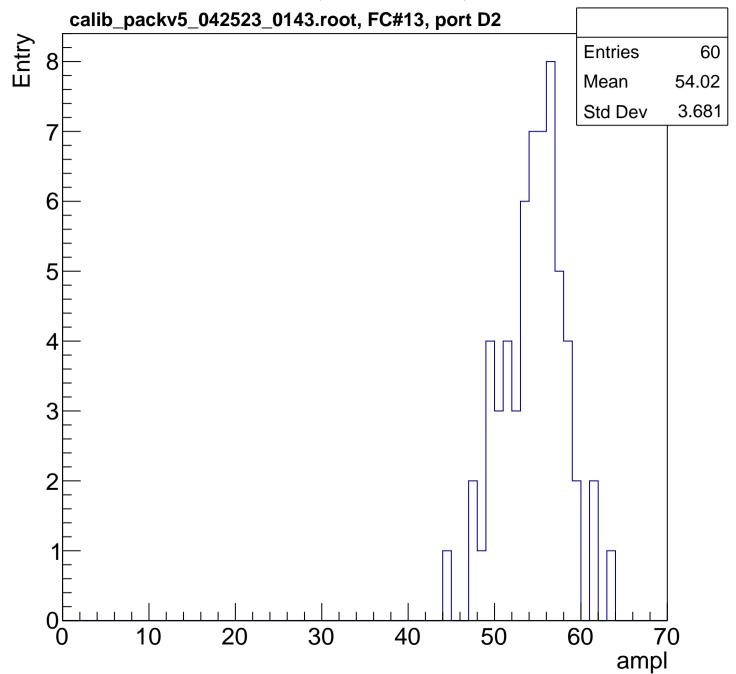


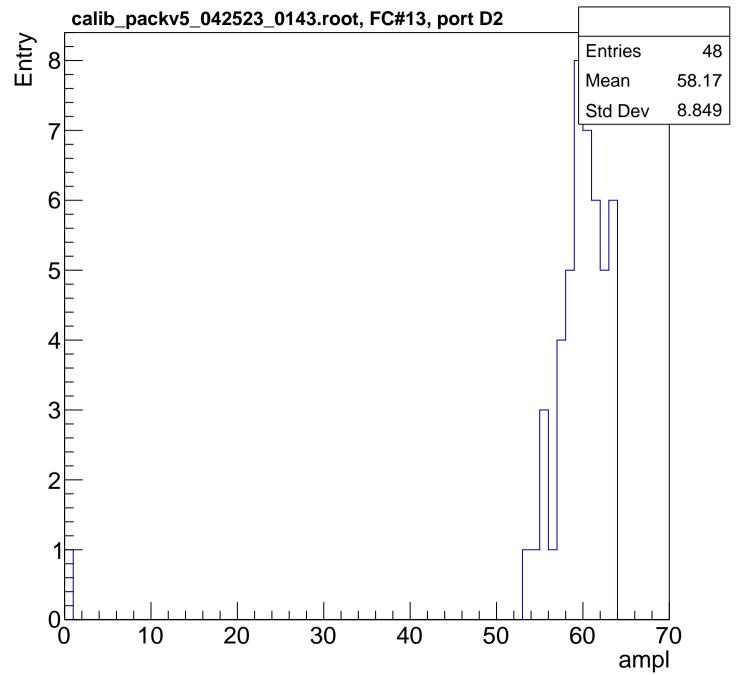


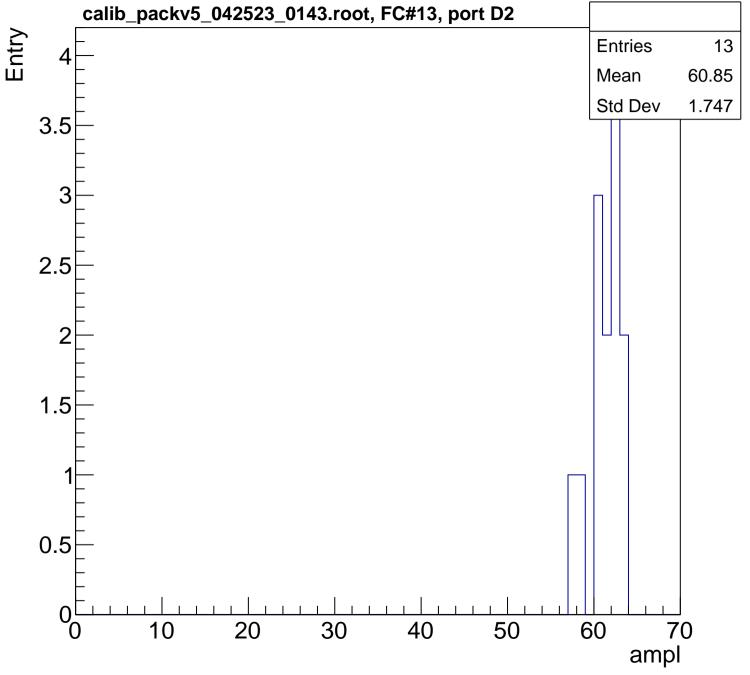


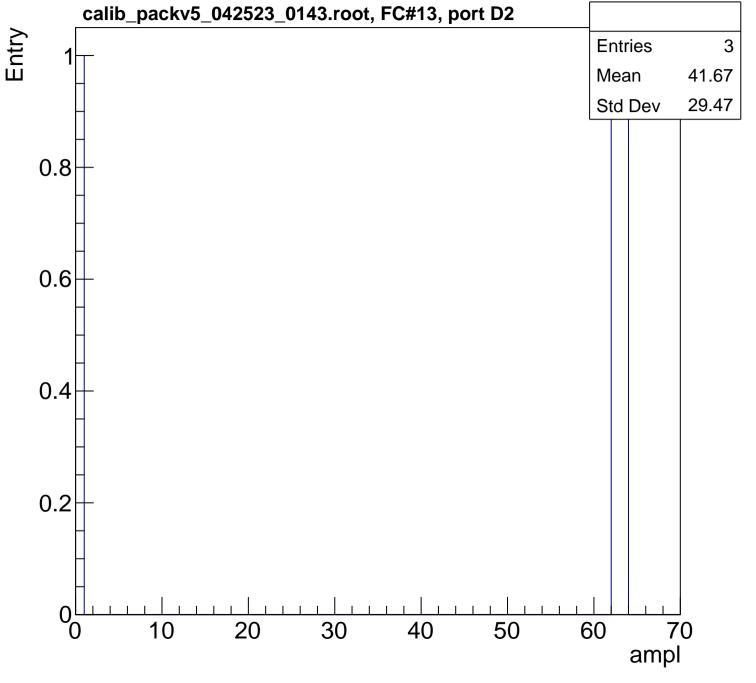


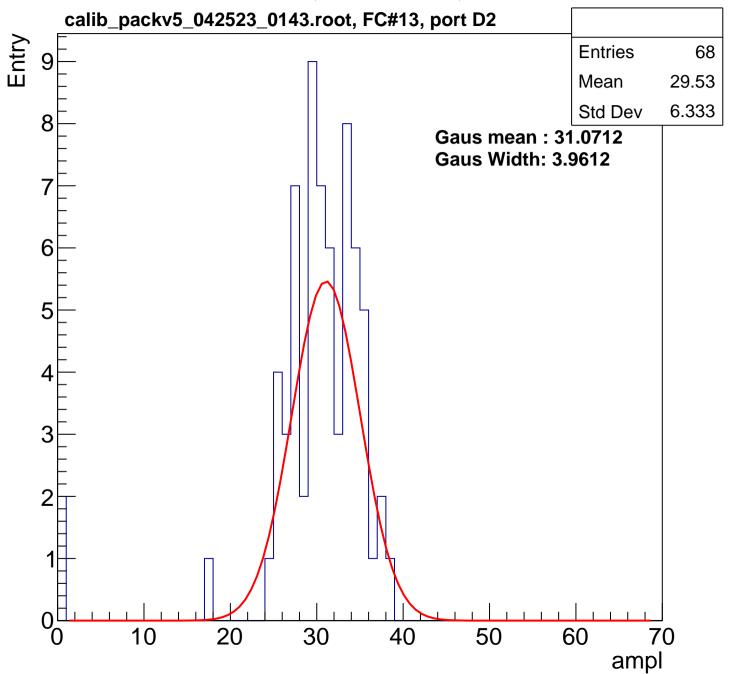


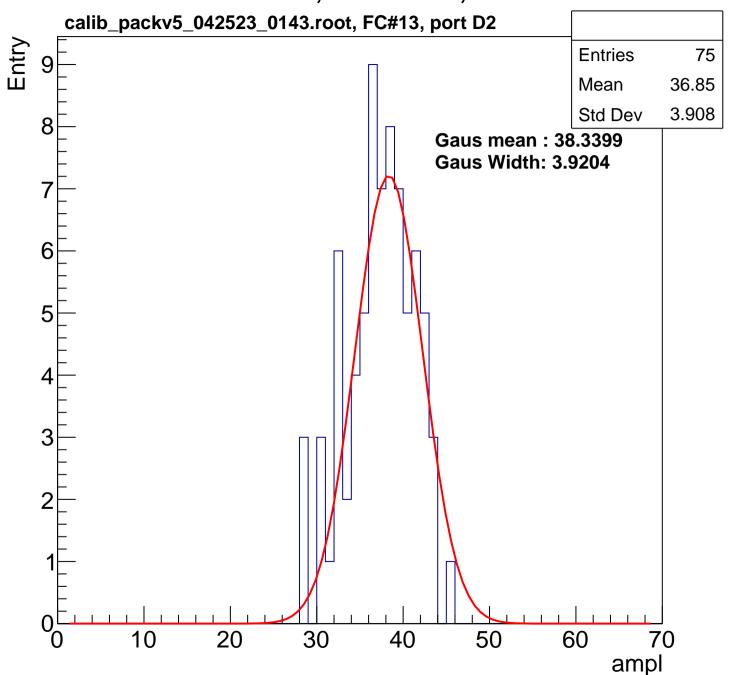


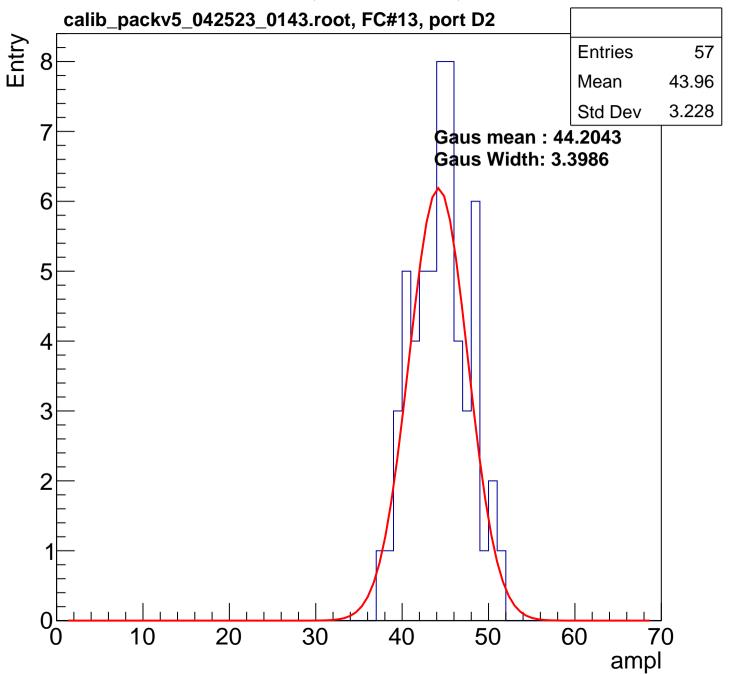


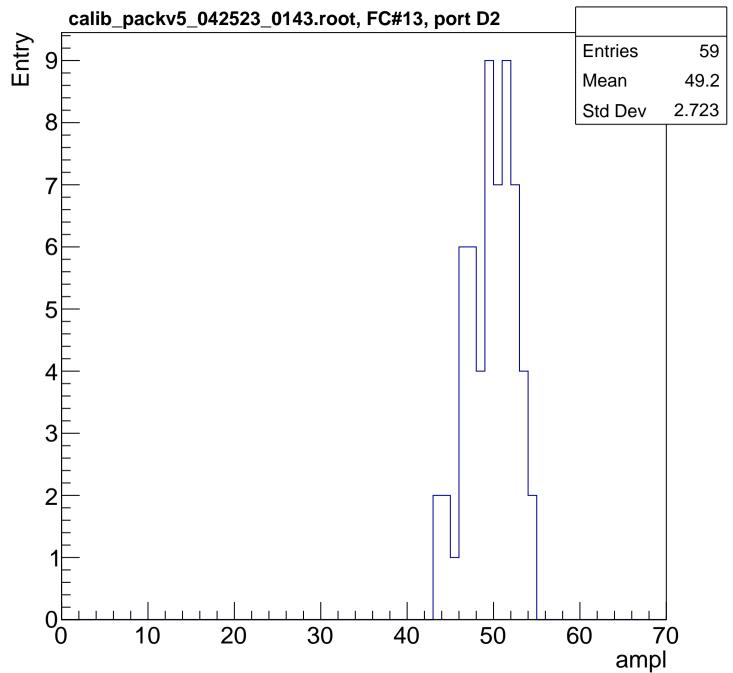


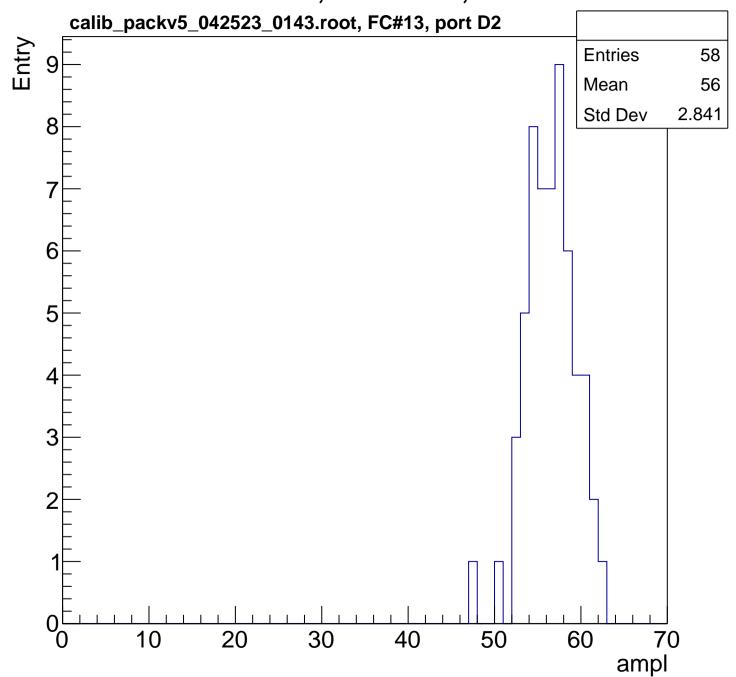


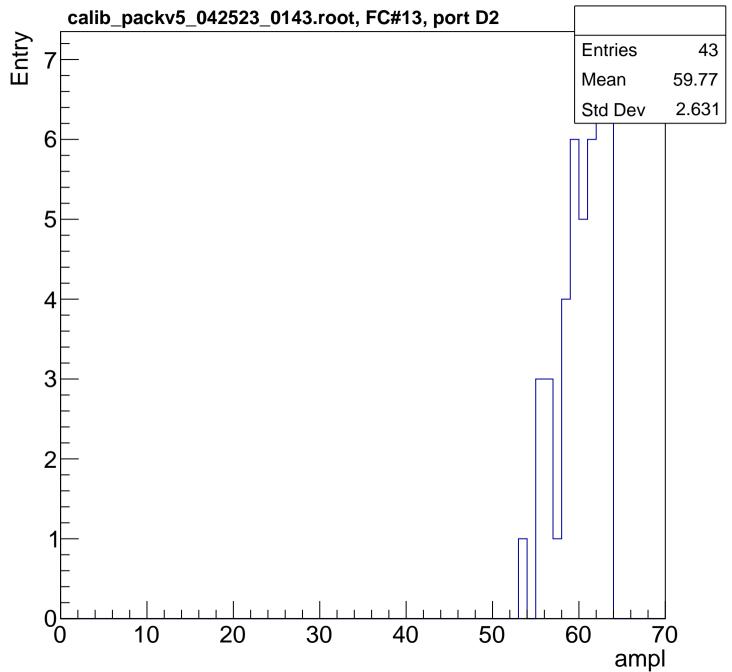


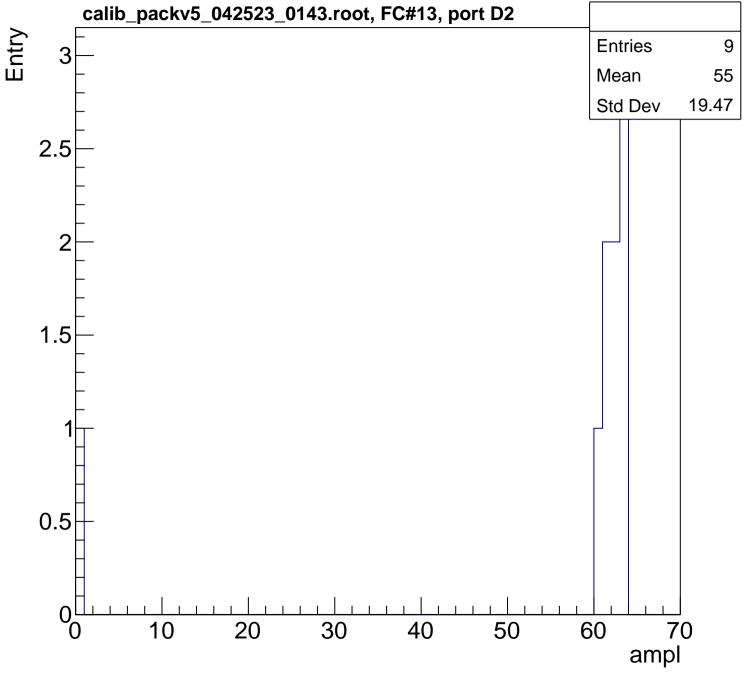




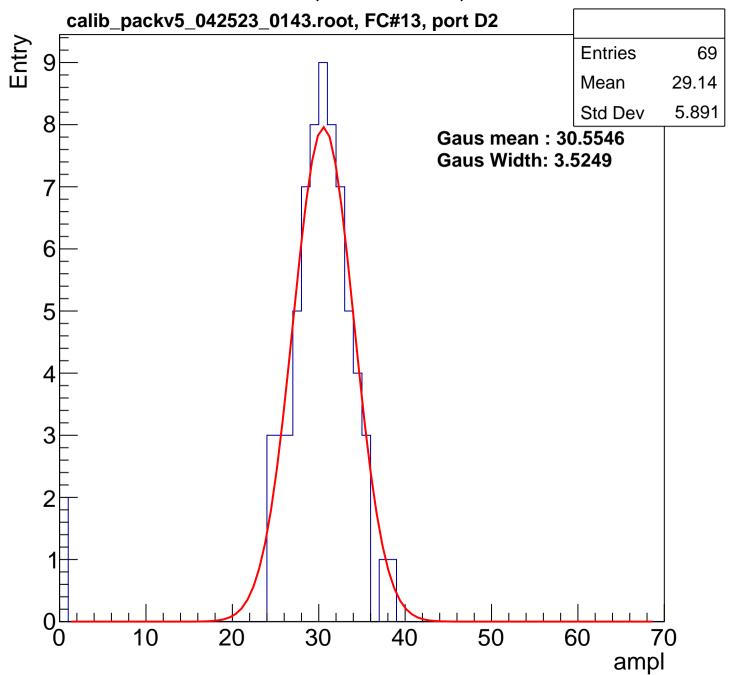


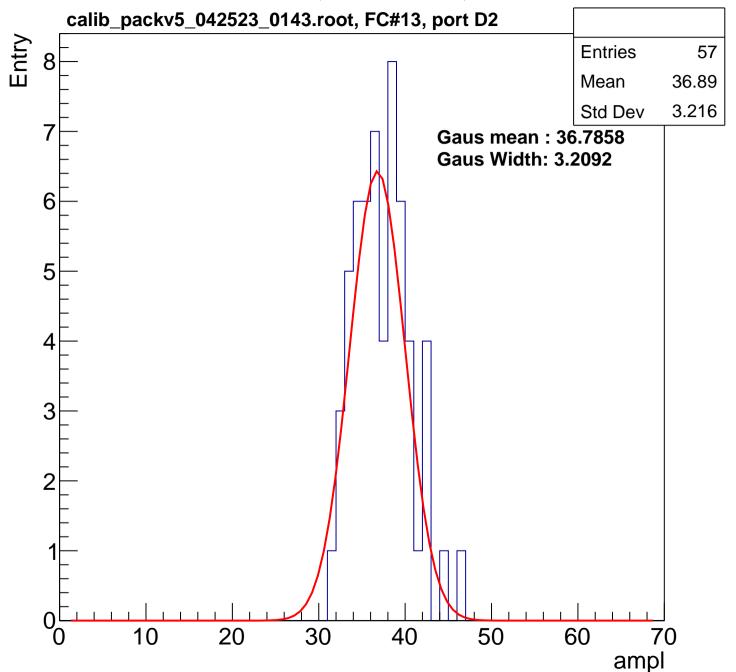


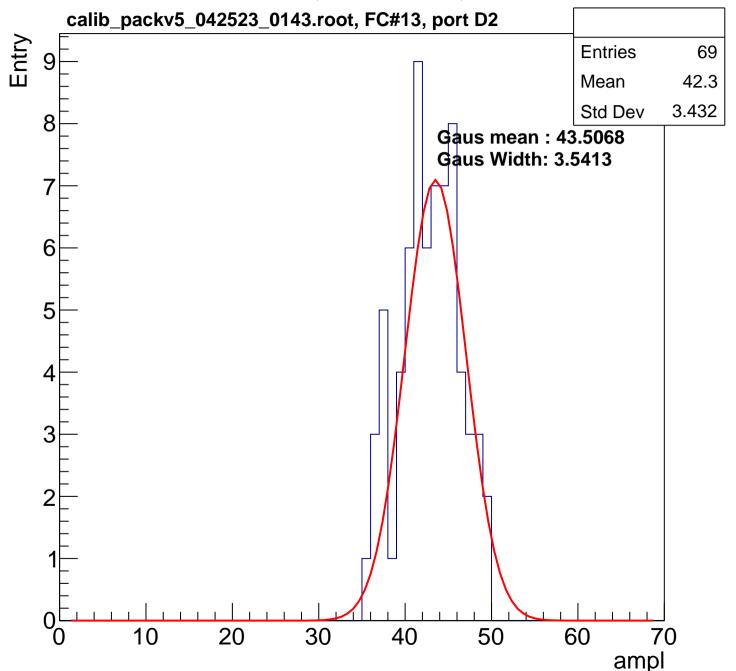


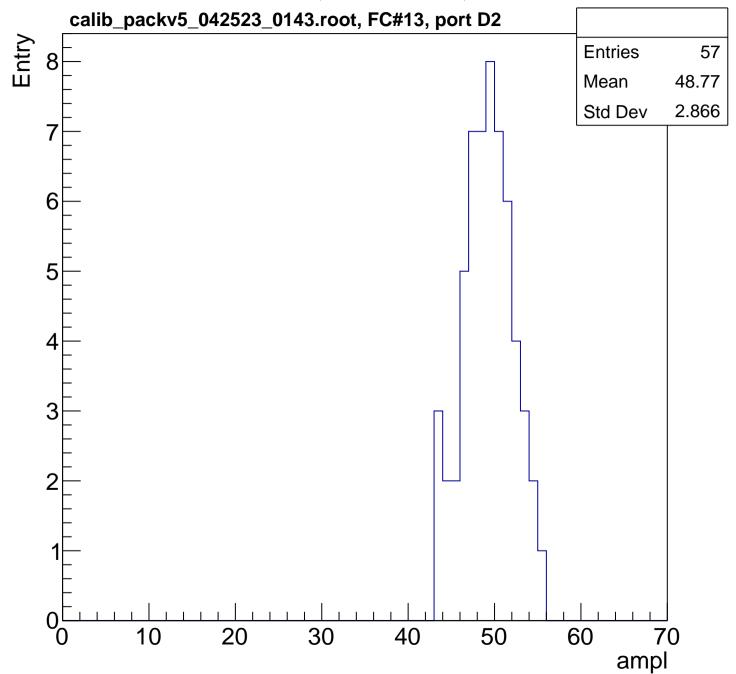


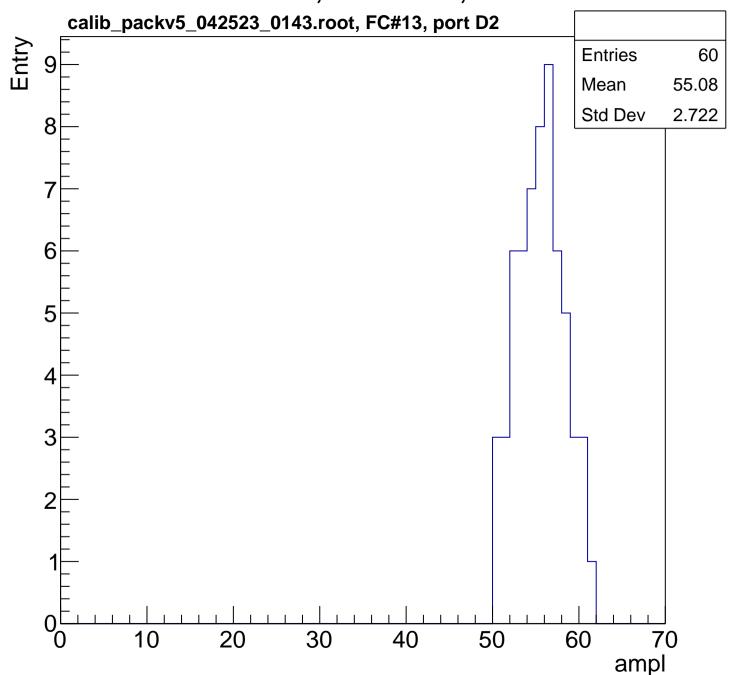


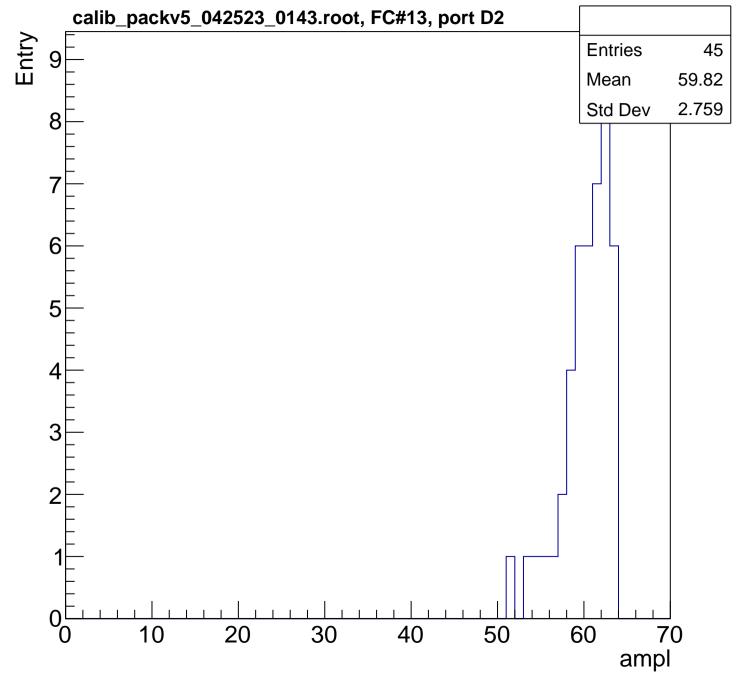


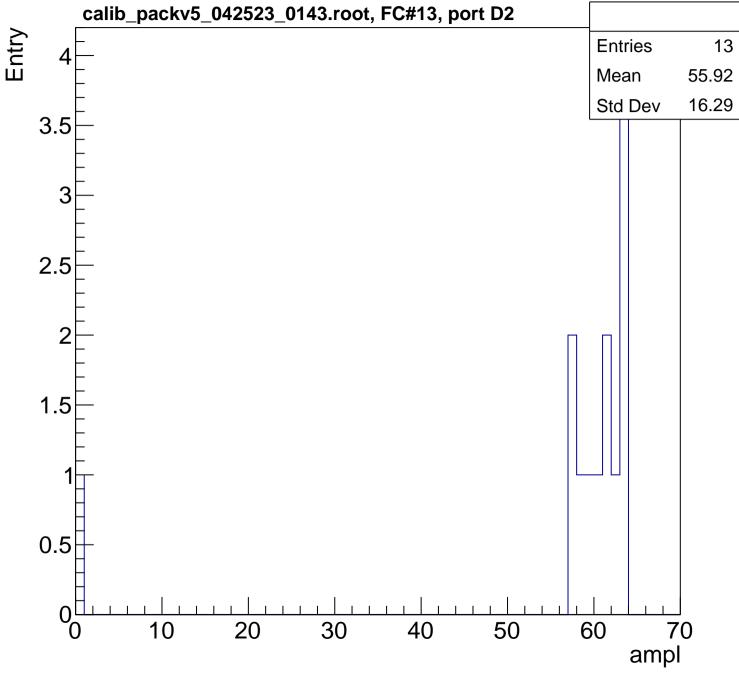


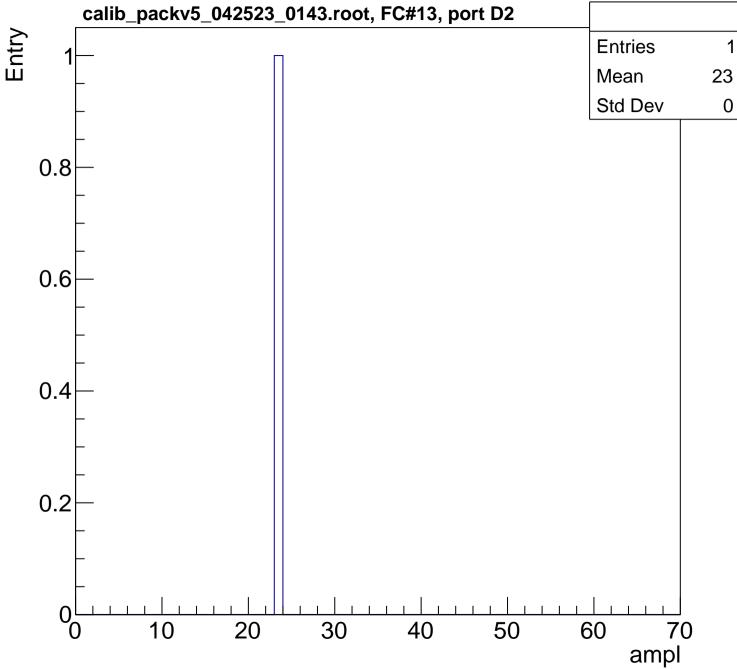


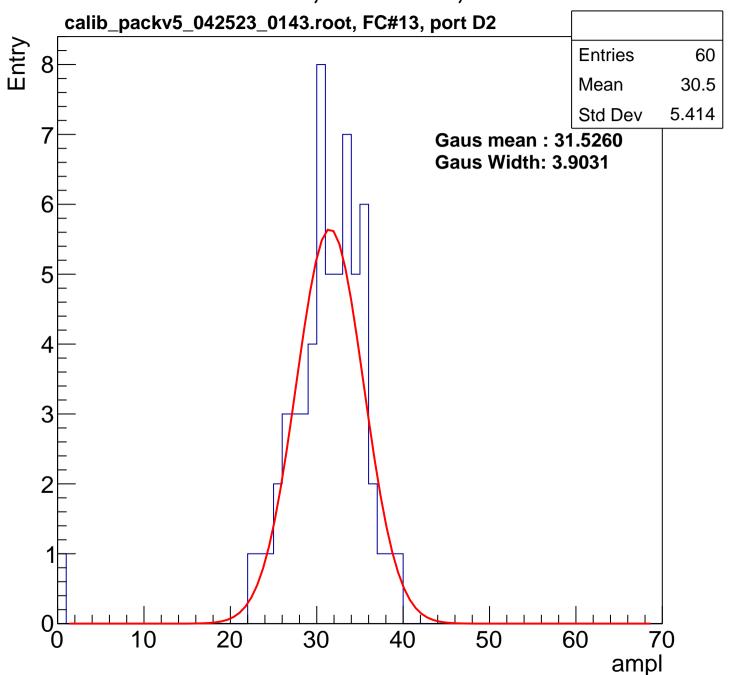


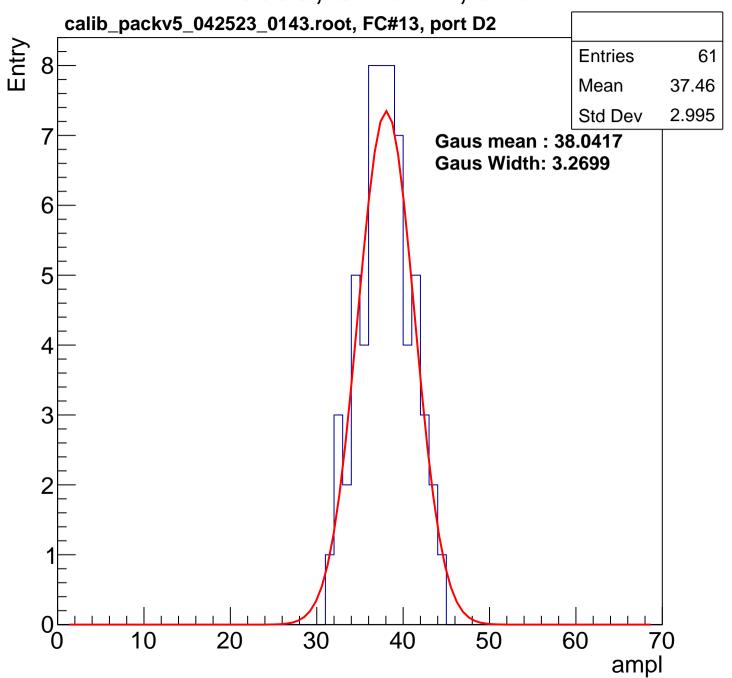


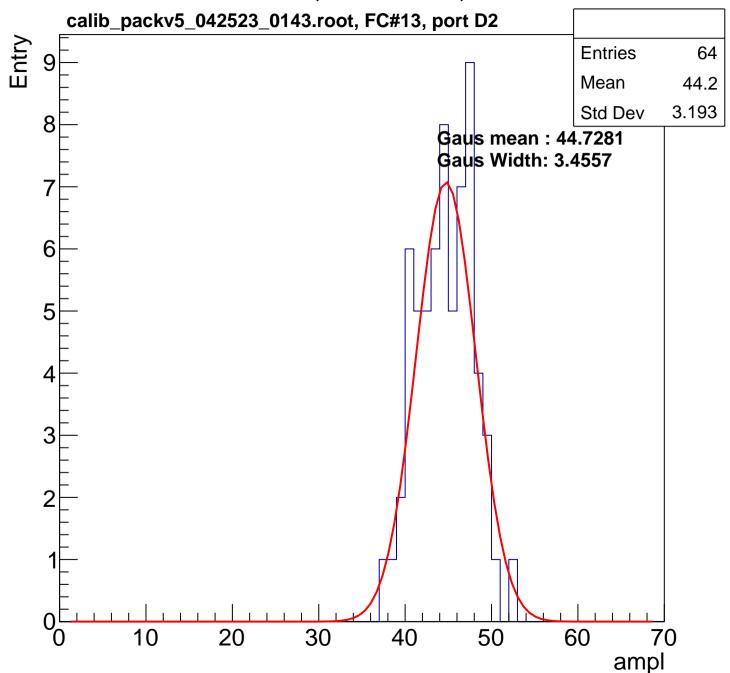


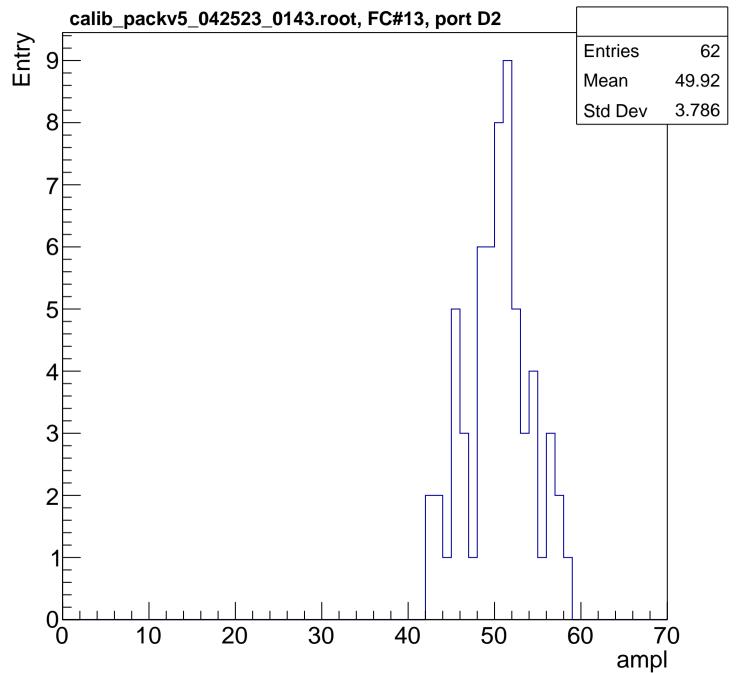


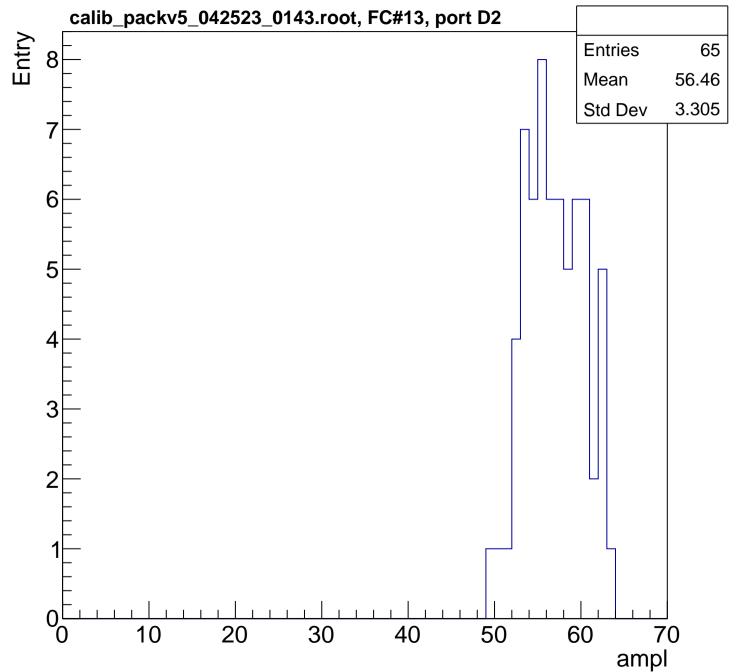


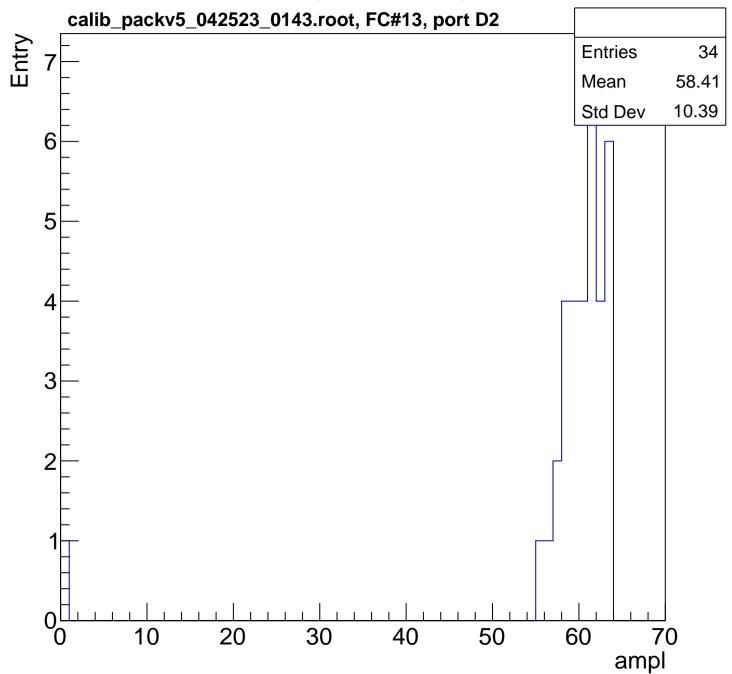


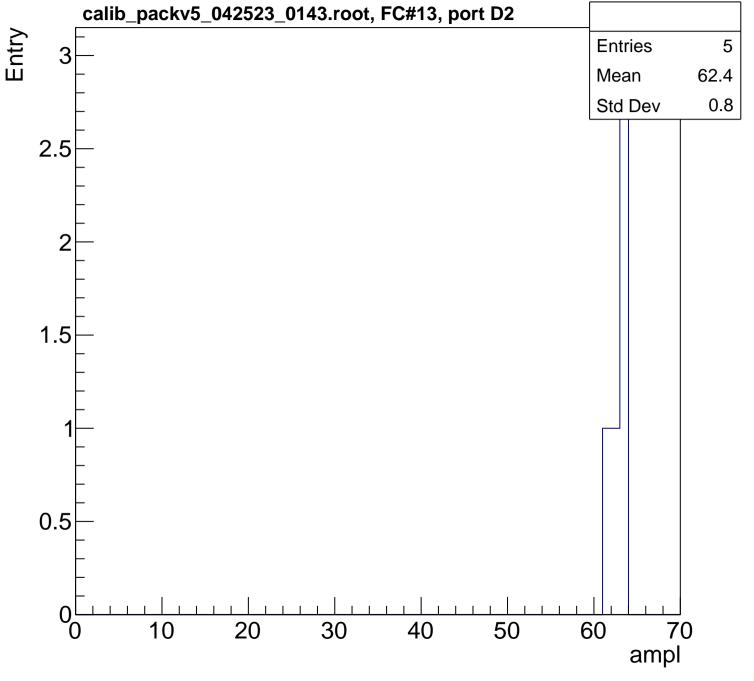




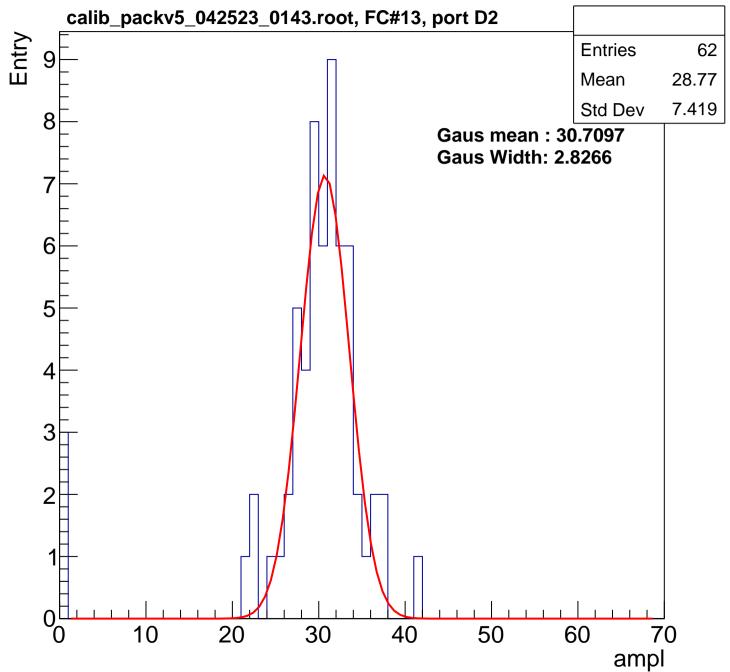


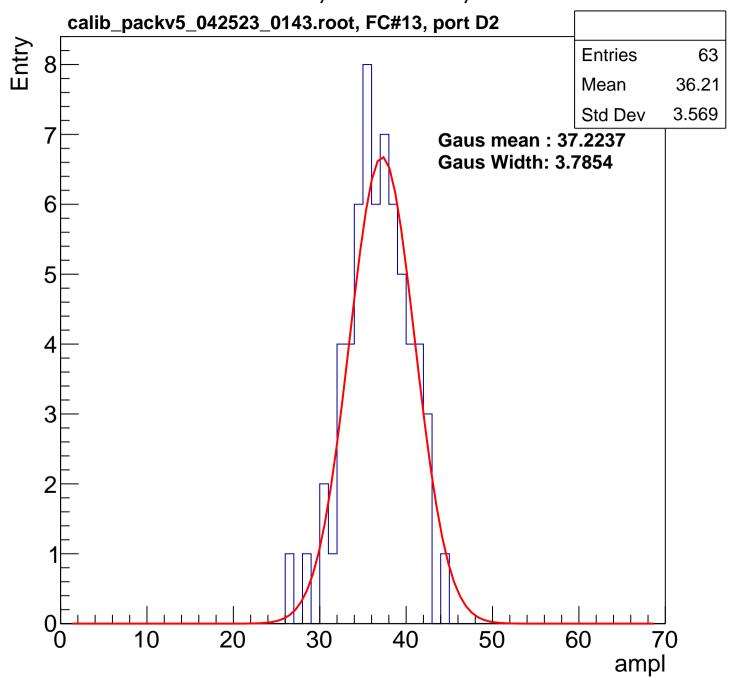


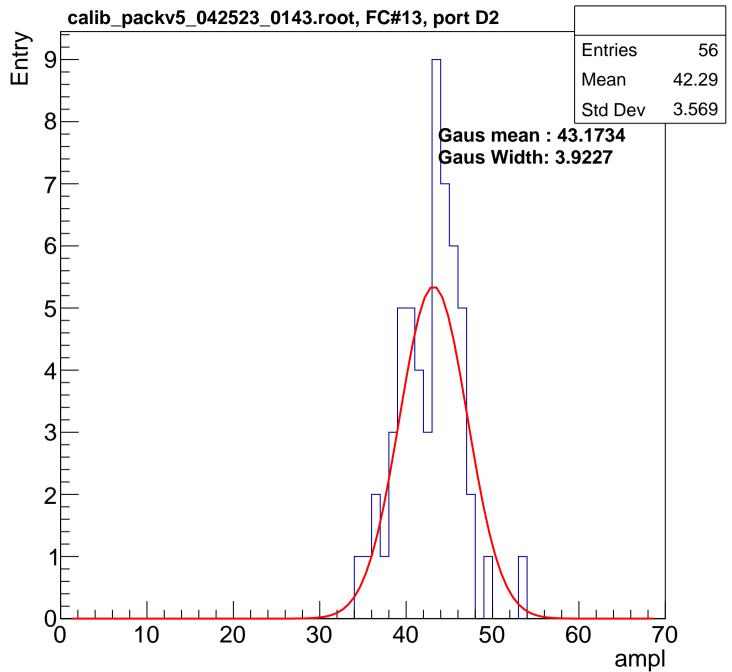


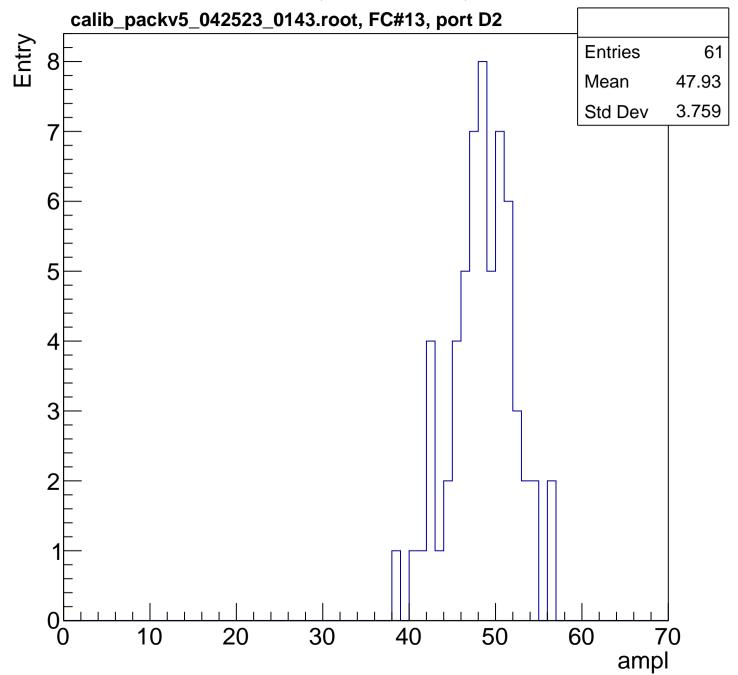


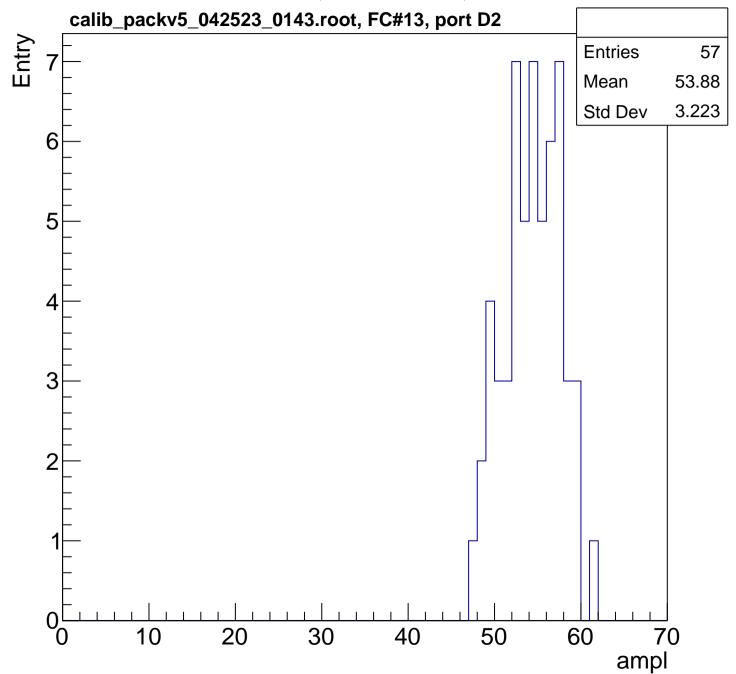
B1L003S, U4-ch77, adc7 calib_packv5_042523_0143.root, FC#13, port D2 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

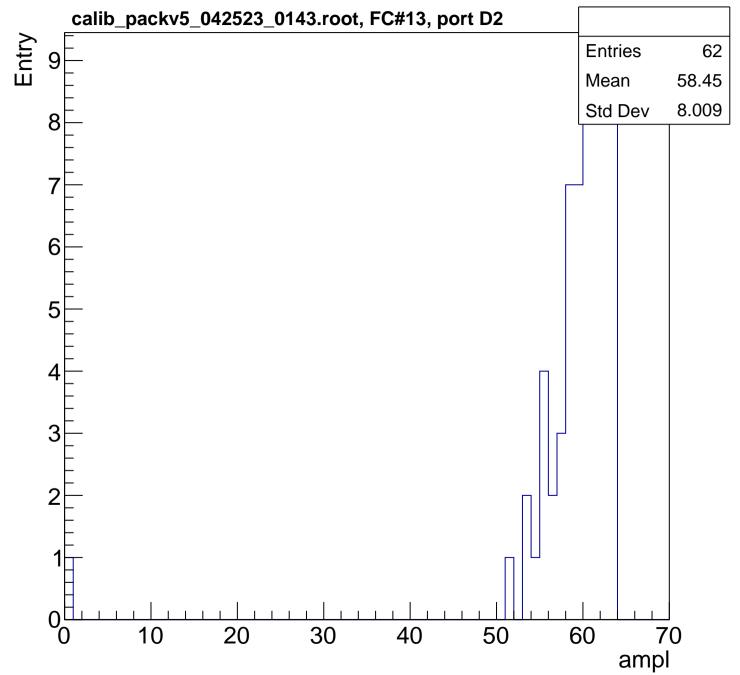


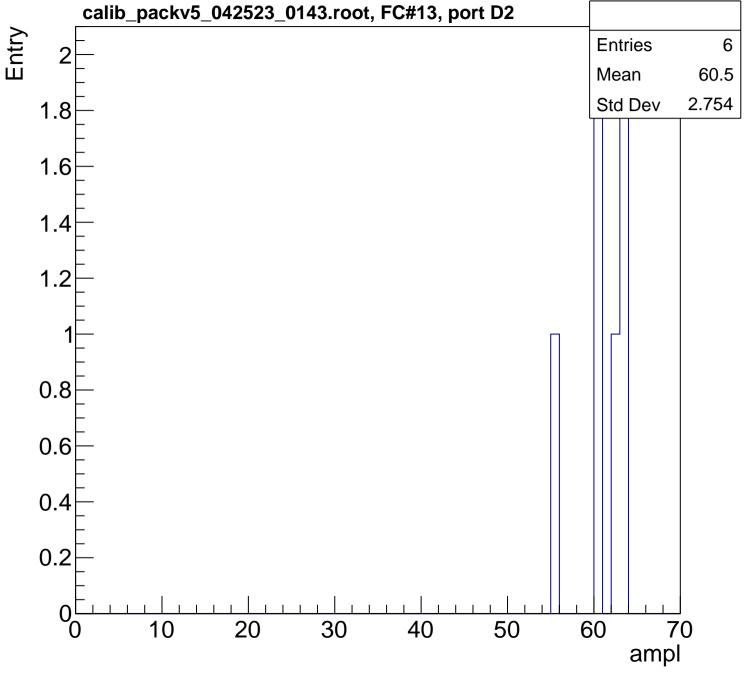


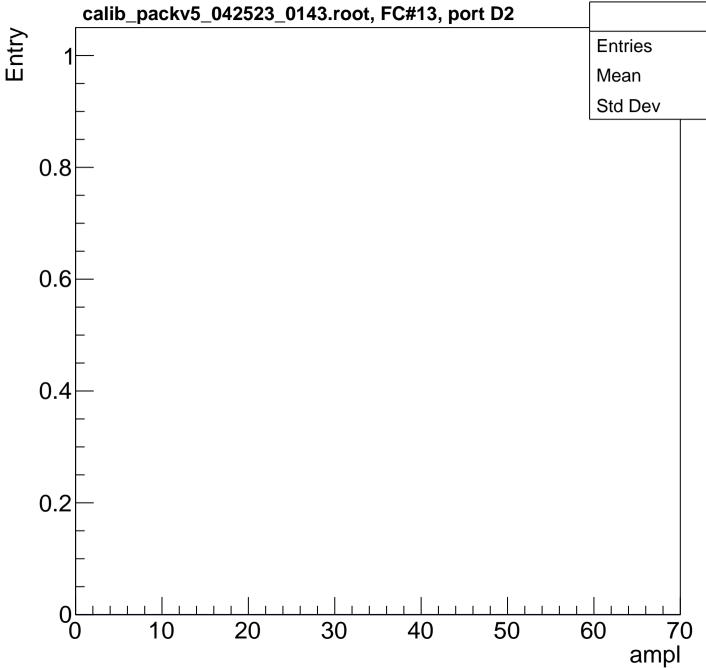


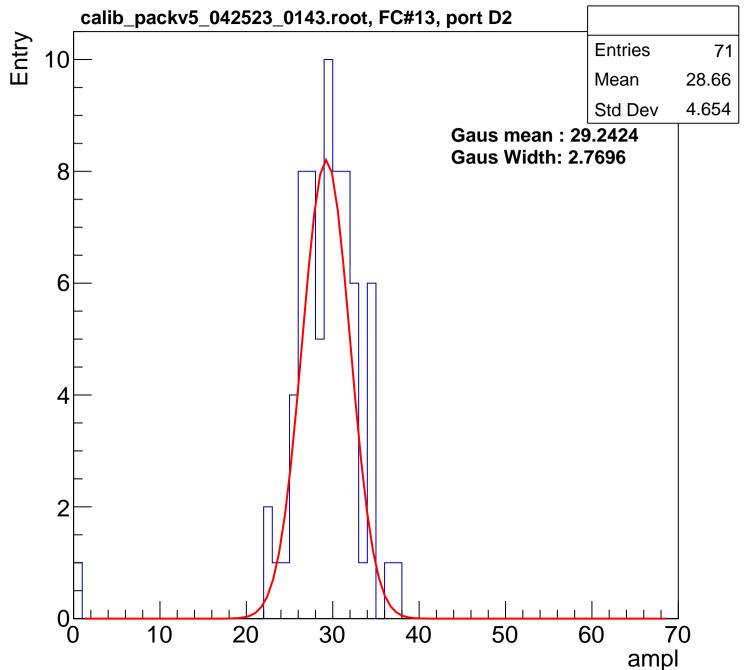


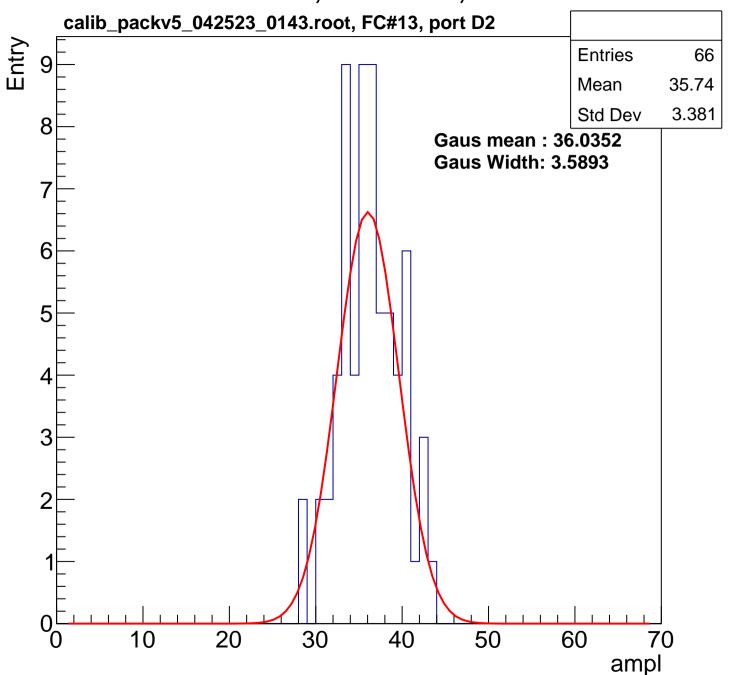


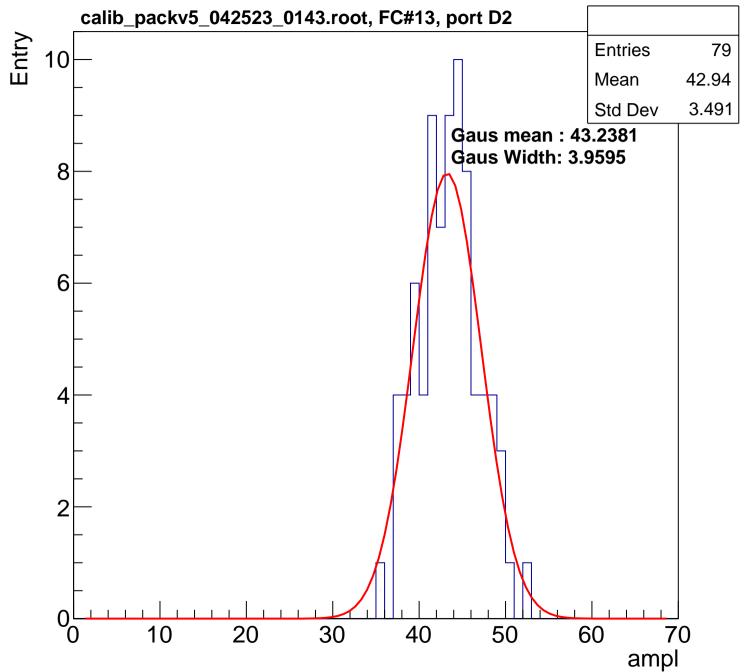


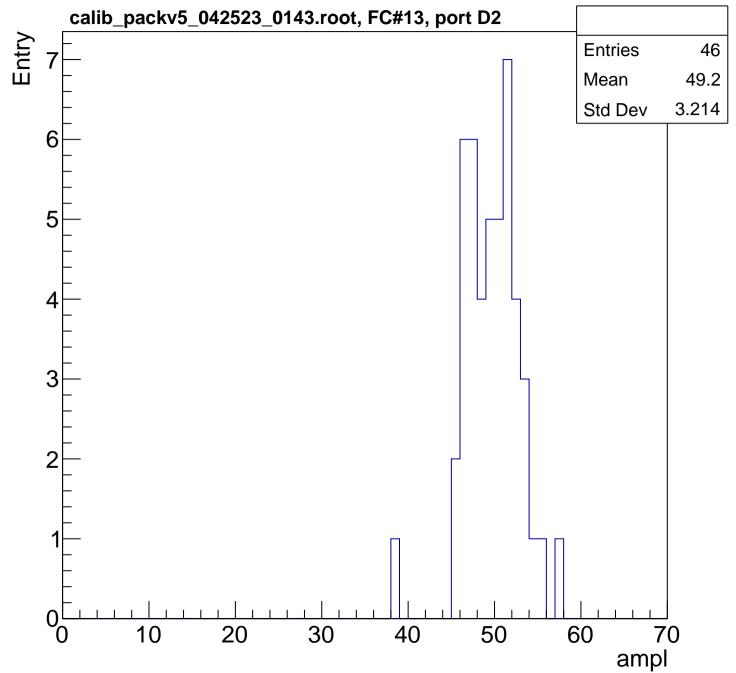


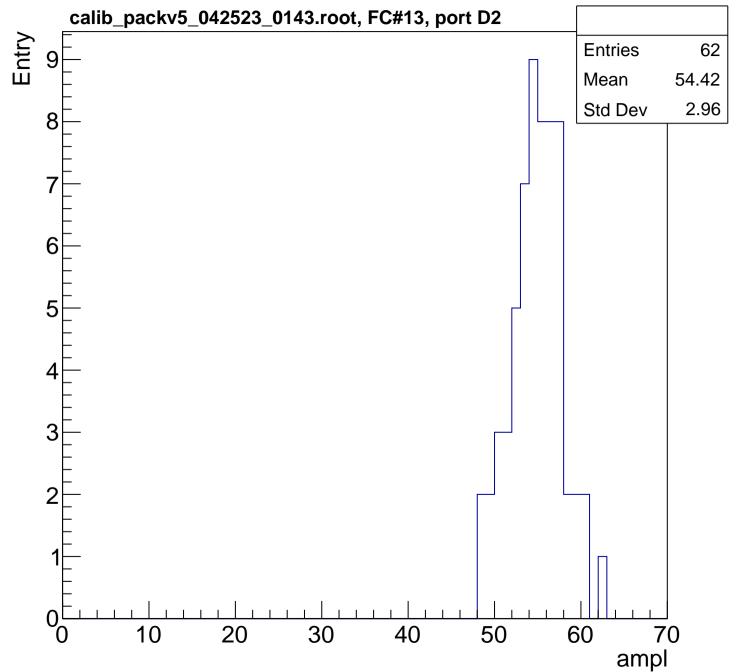


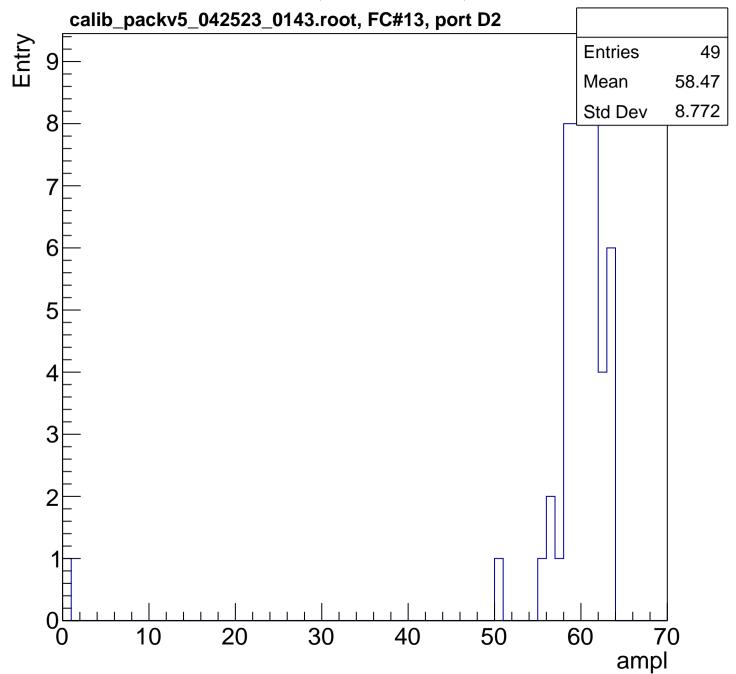


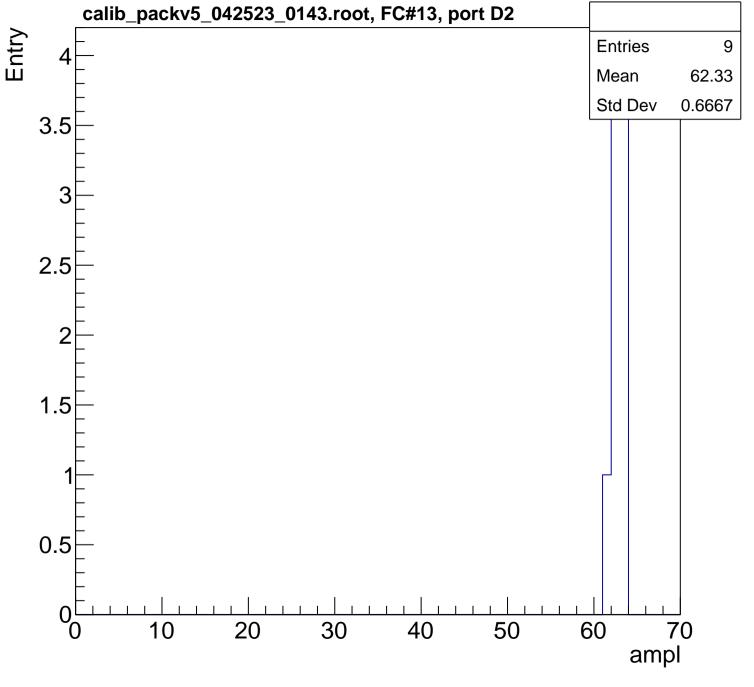




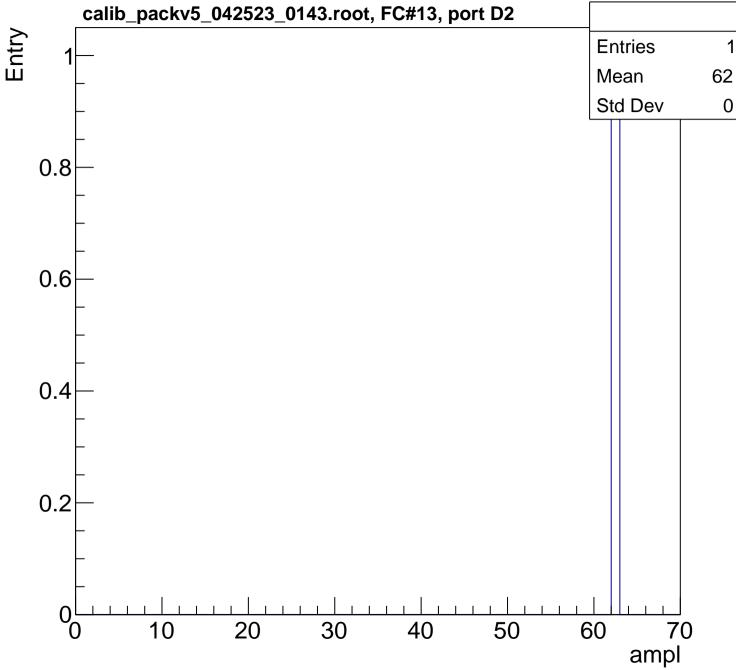


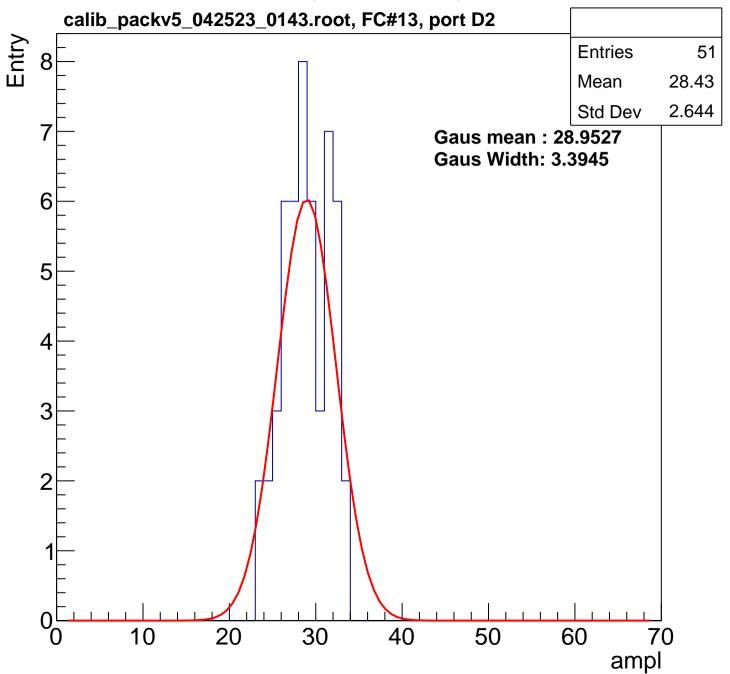


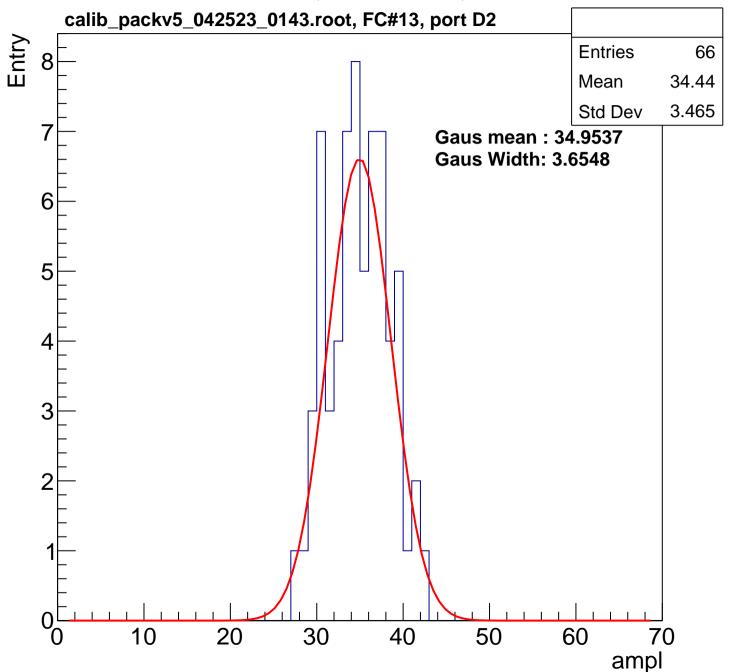


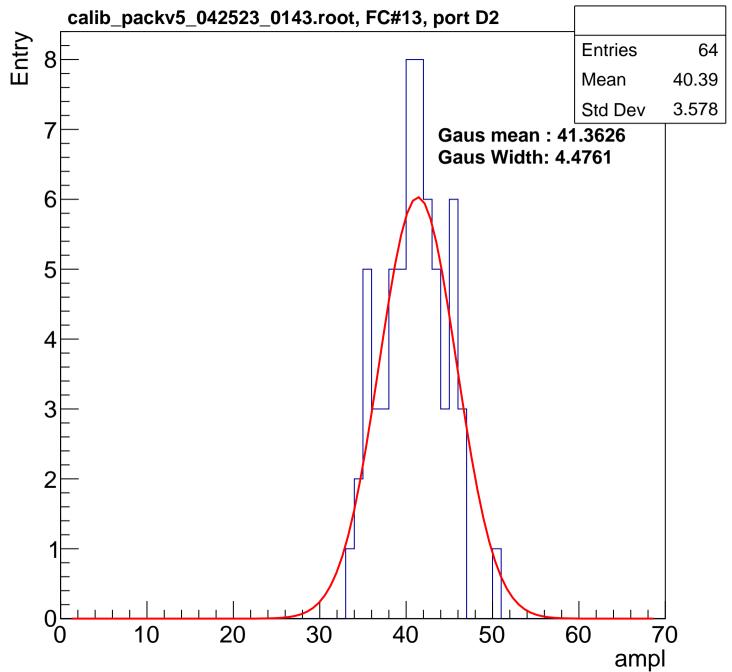


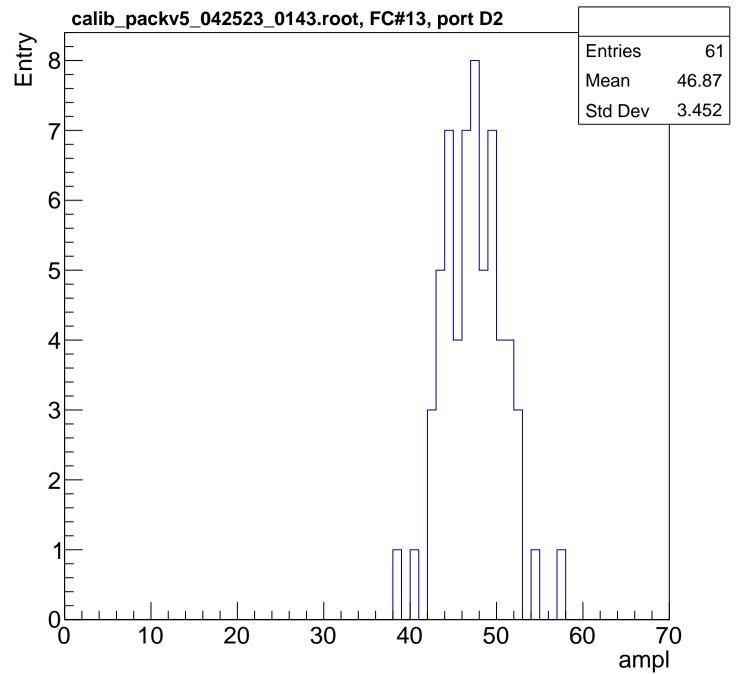
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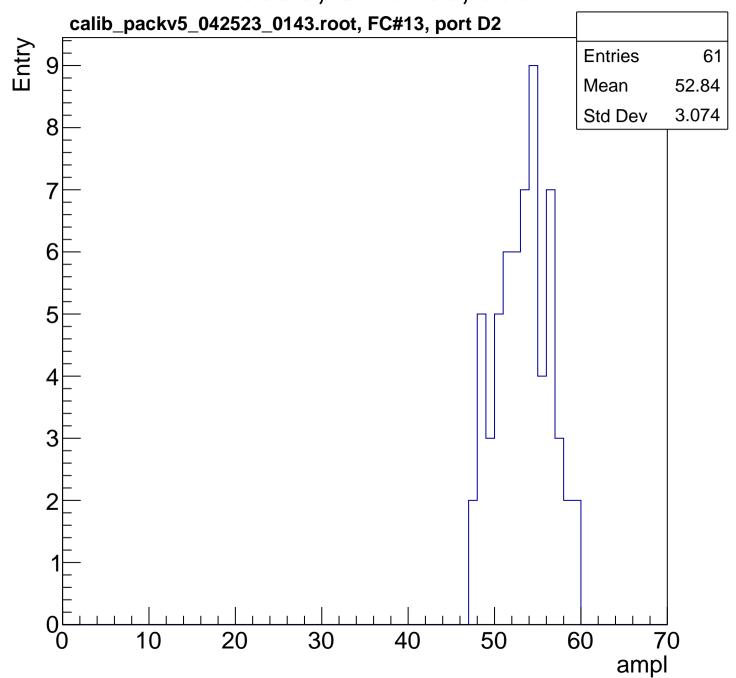


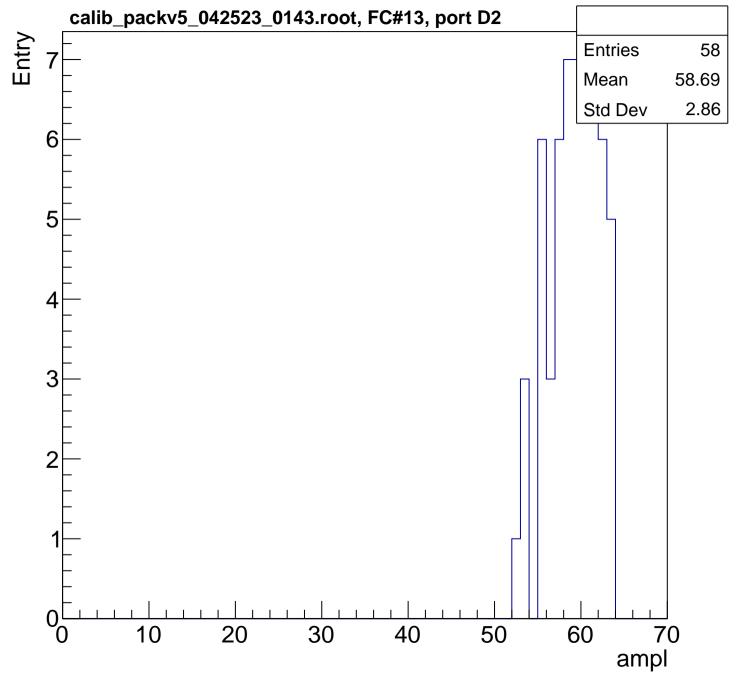


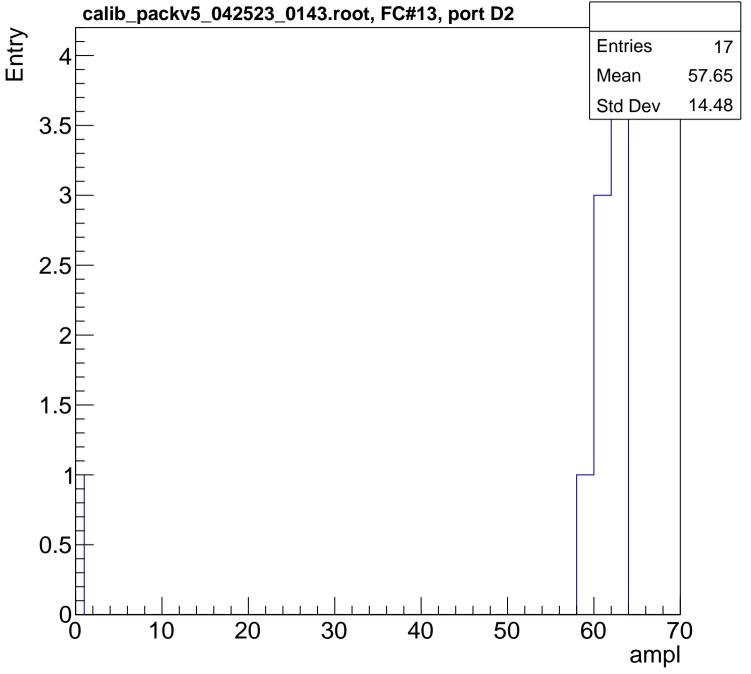


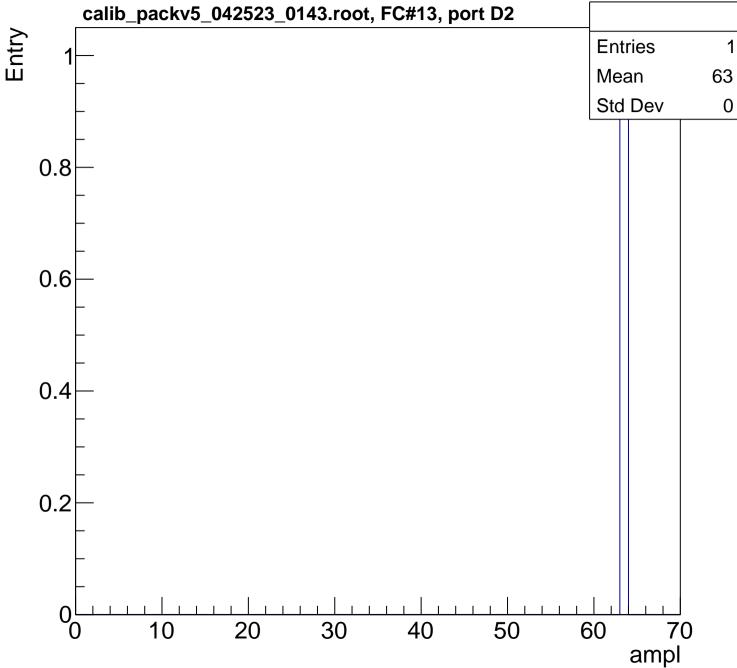


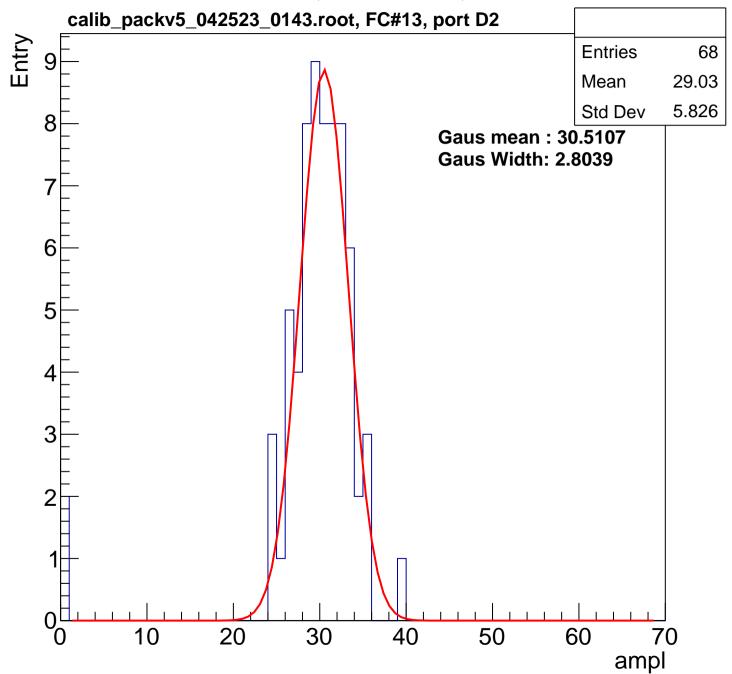


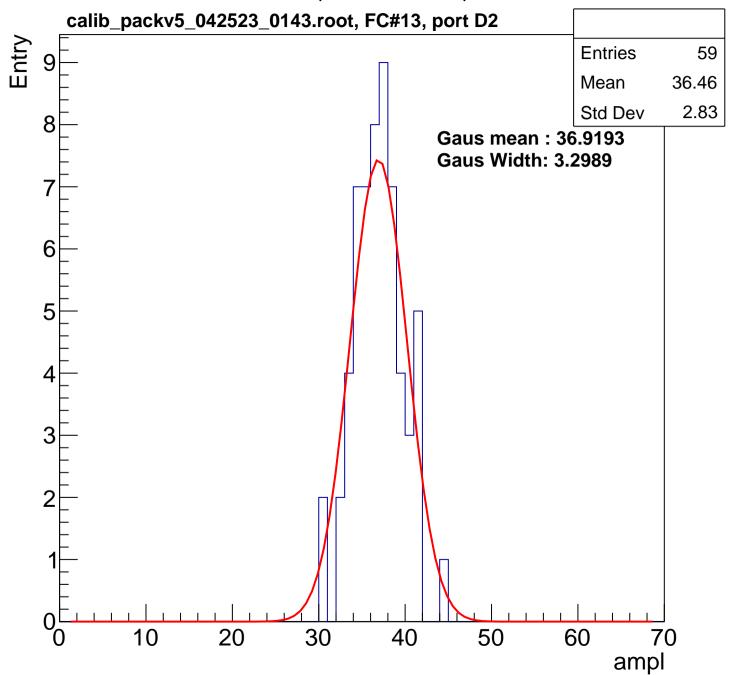


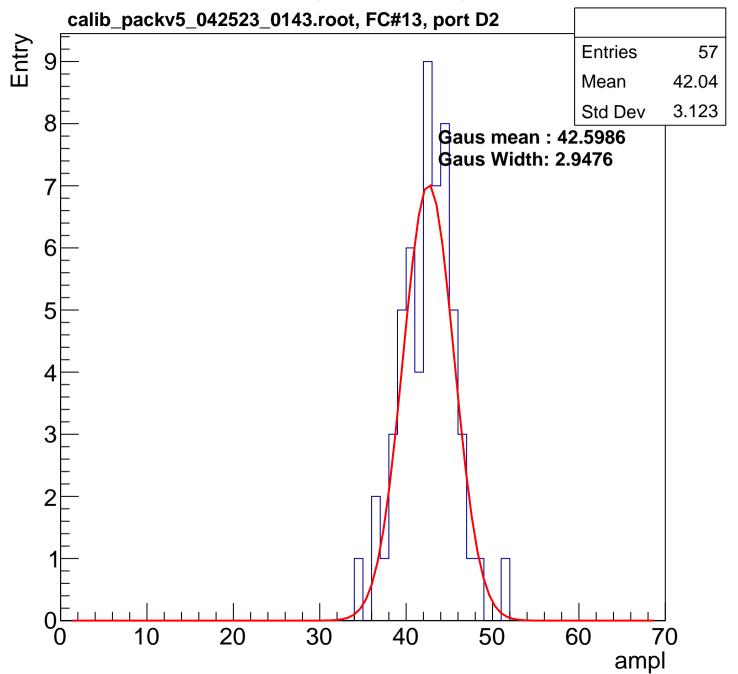


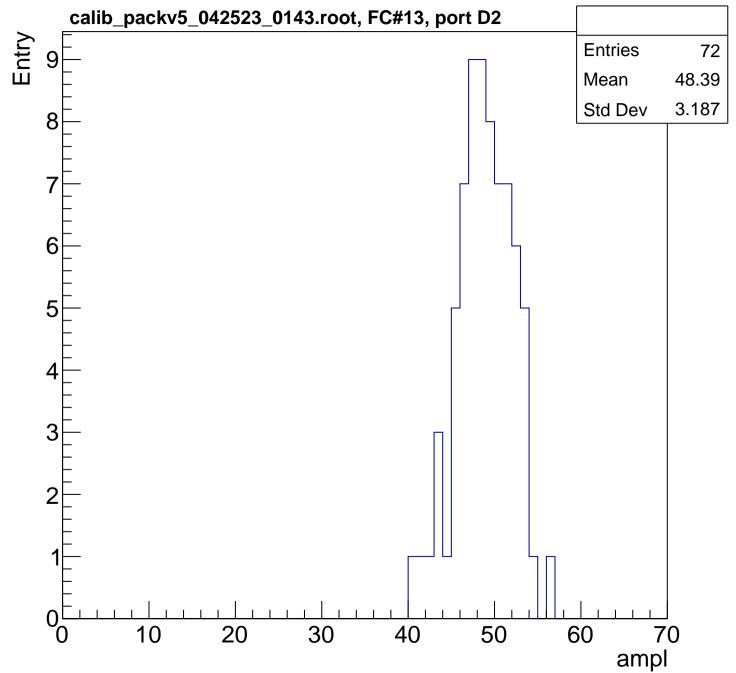


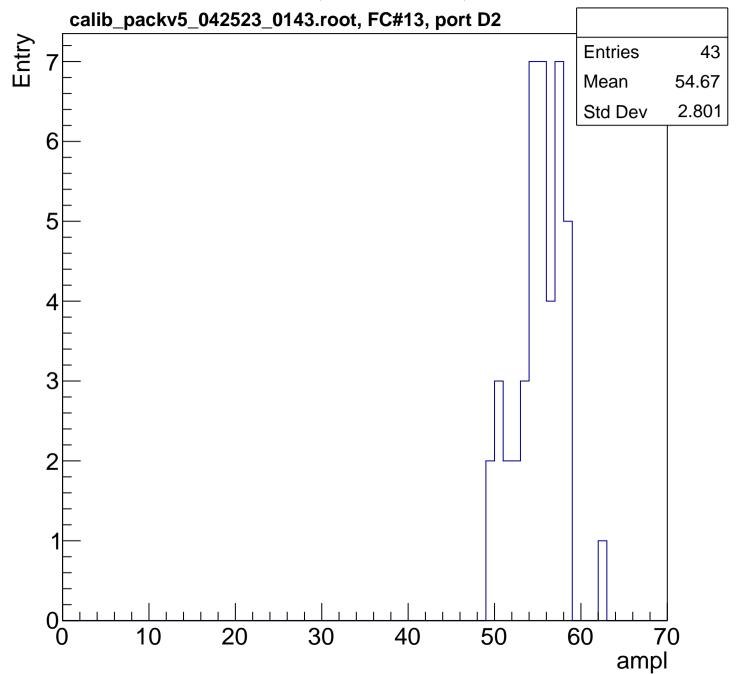


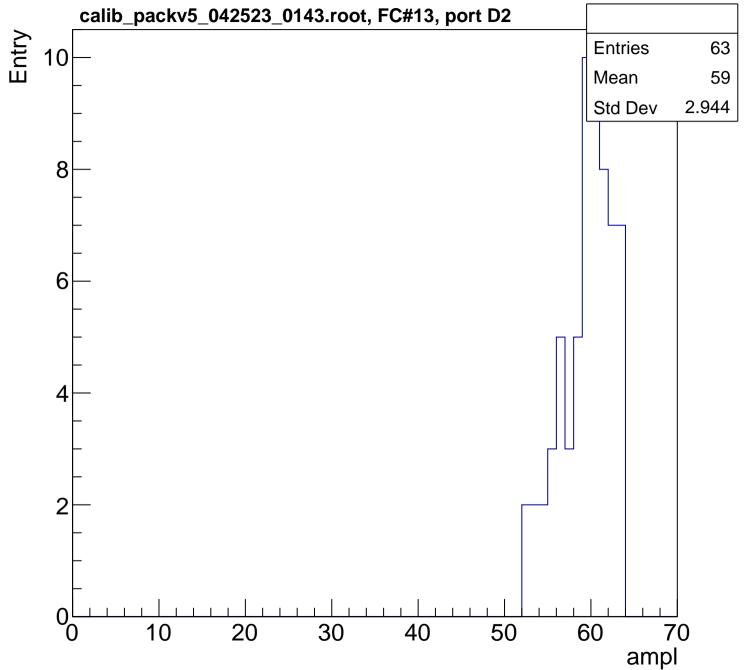


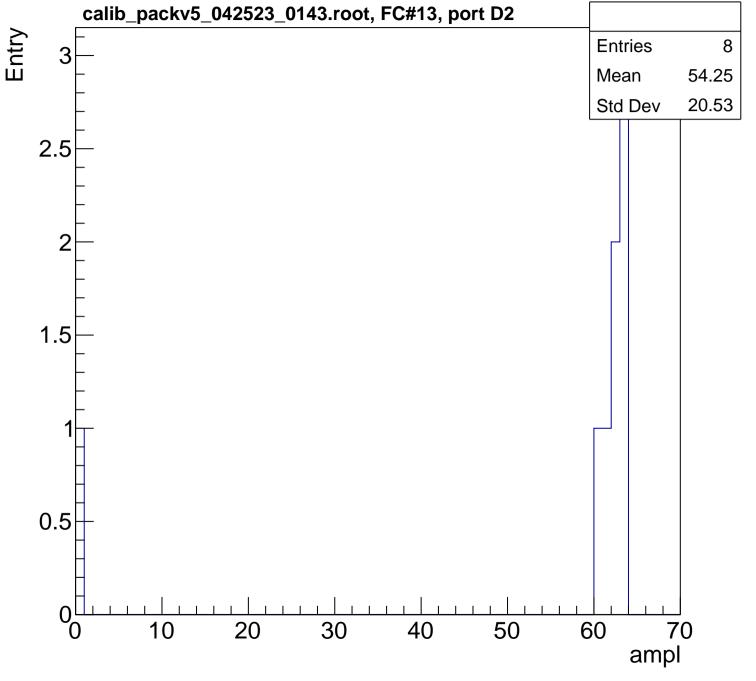


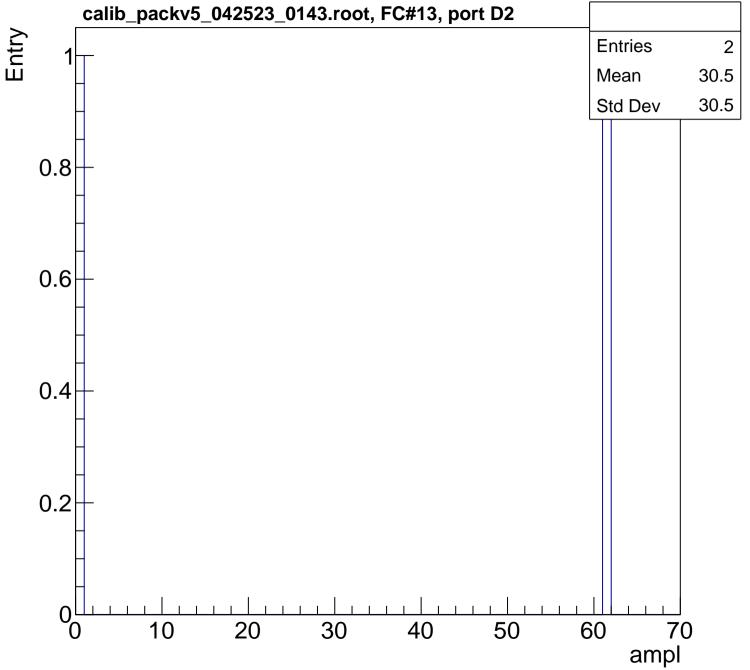


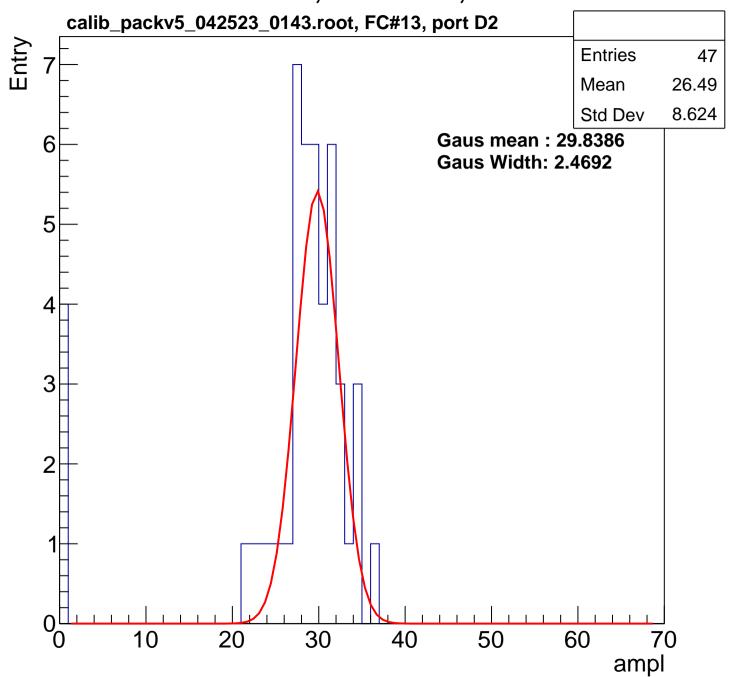


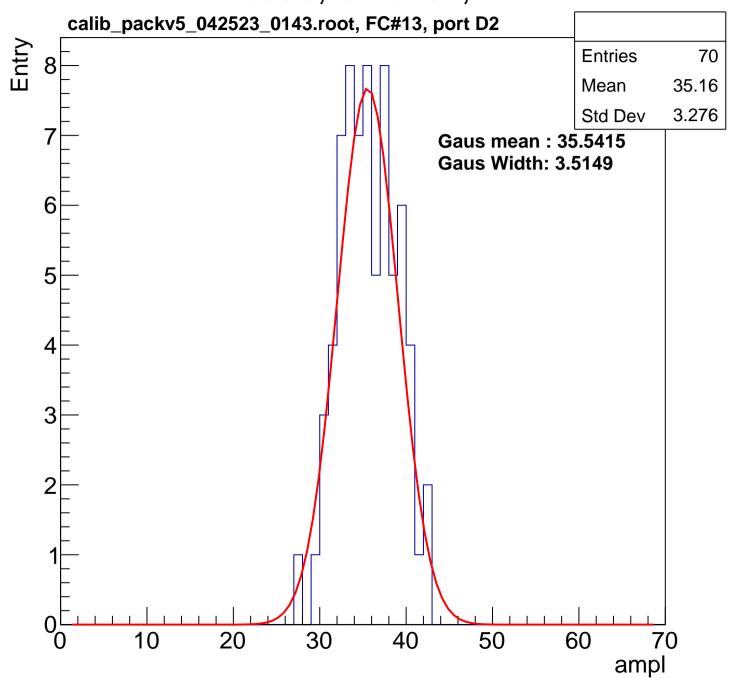


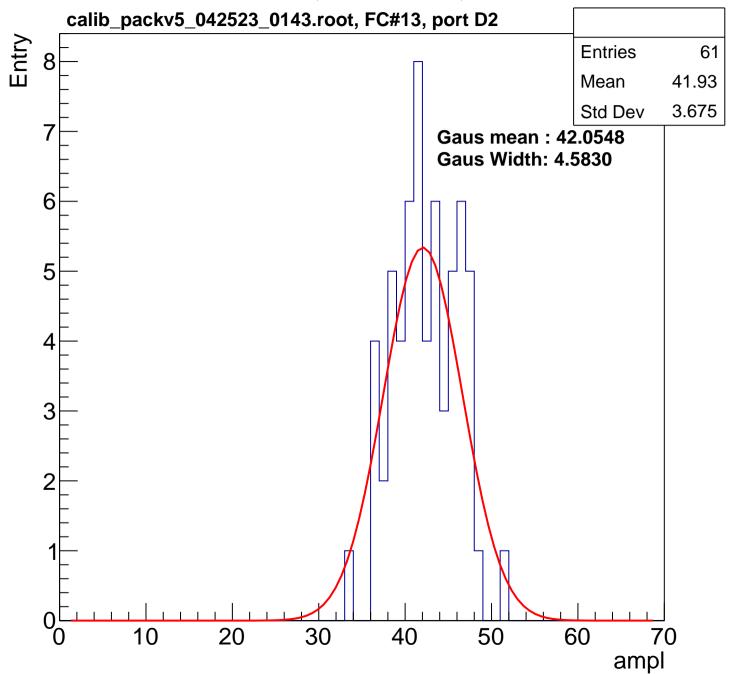


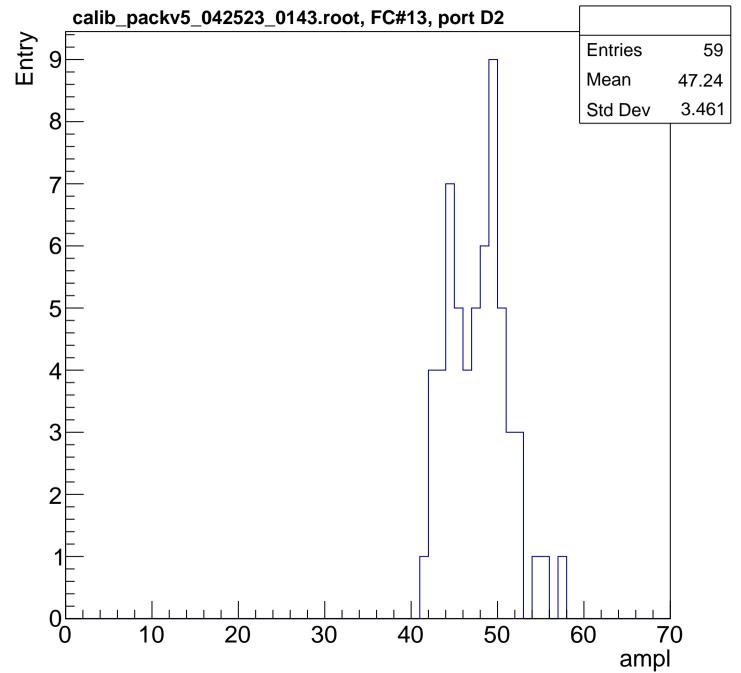


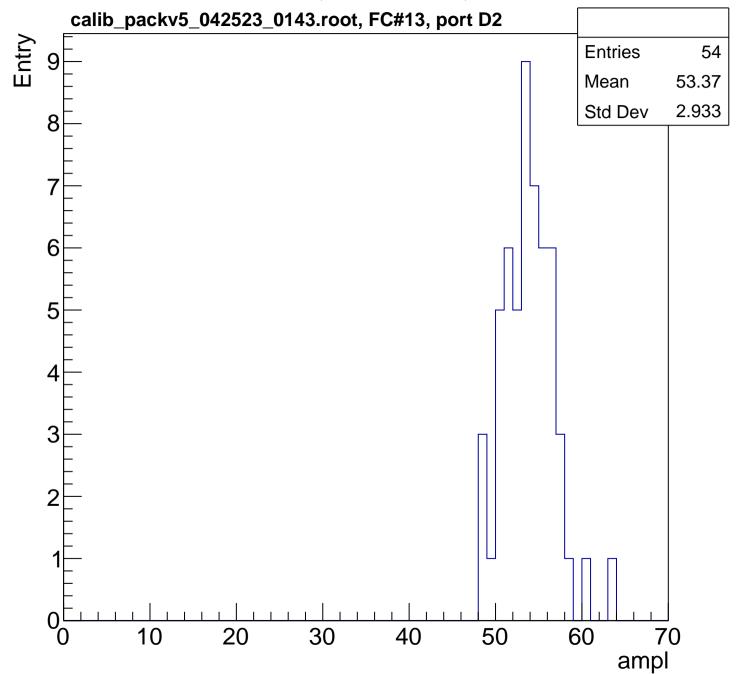


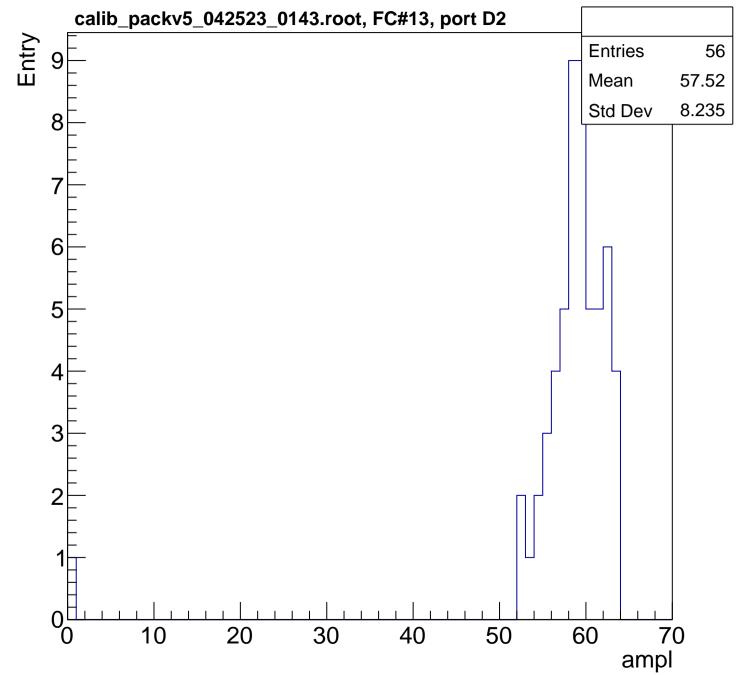


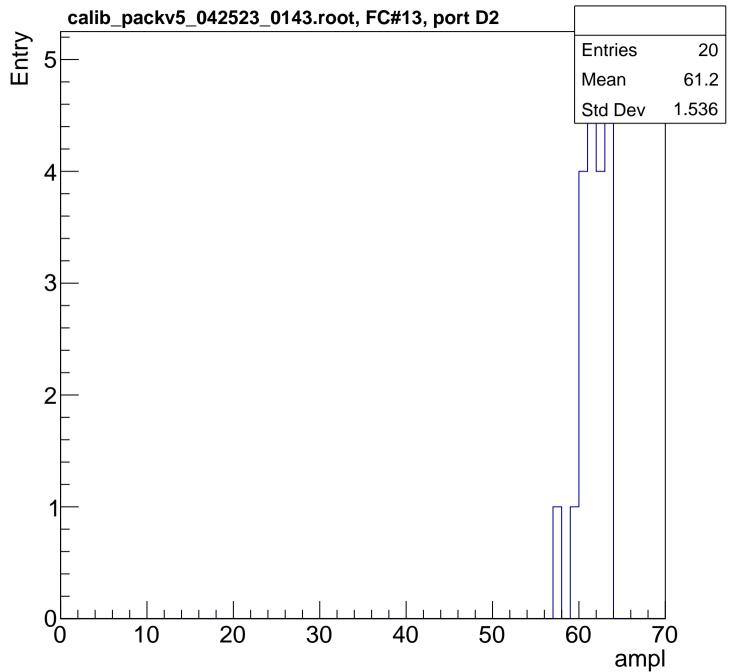


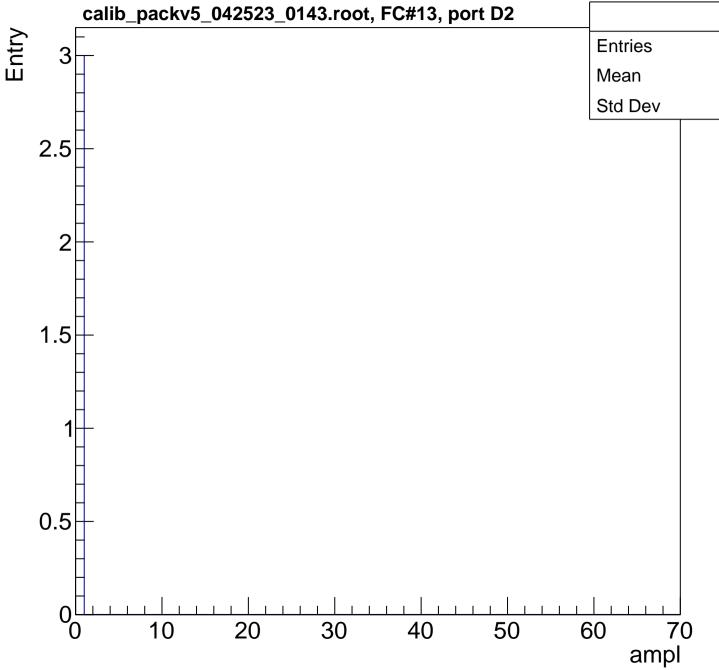


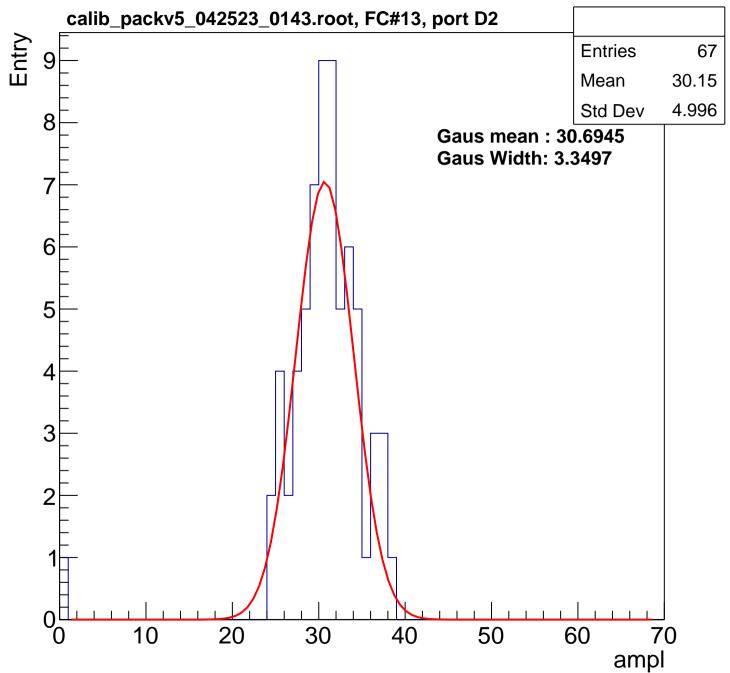


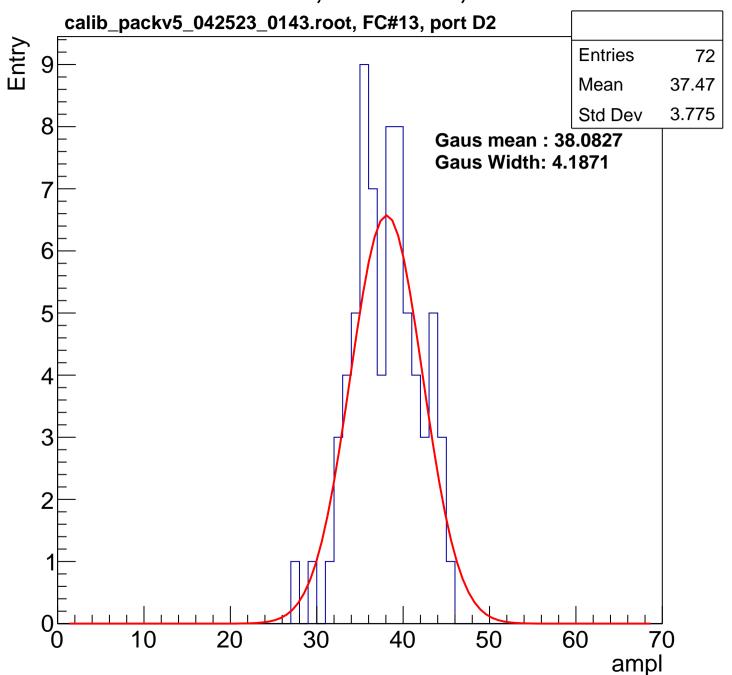


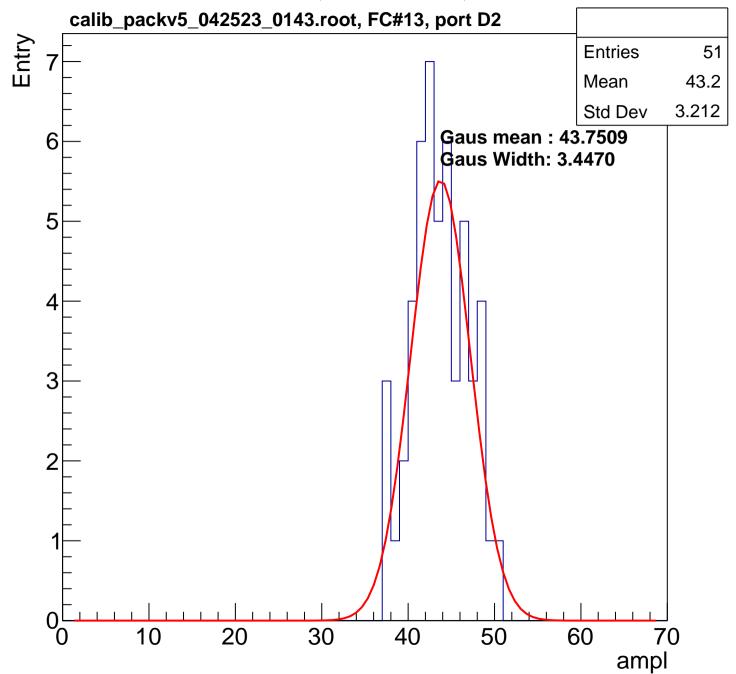


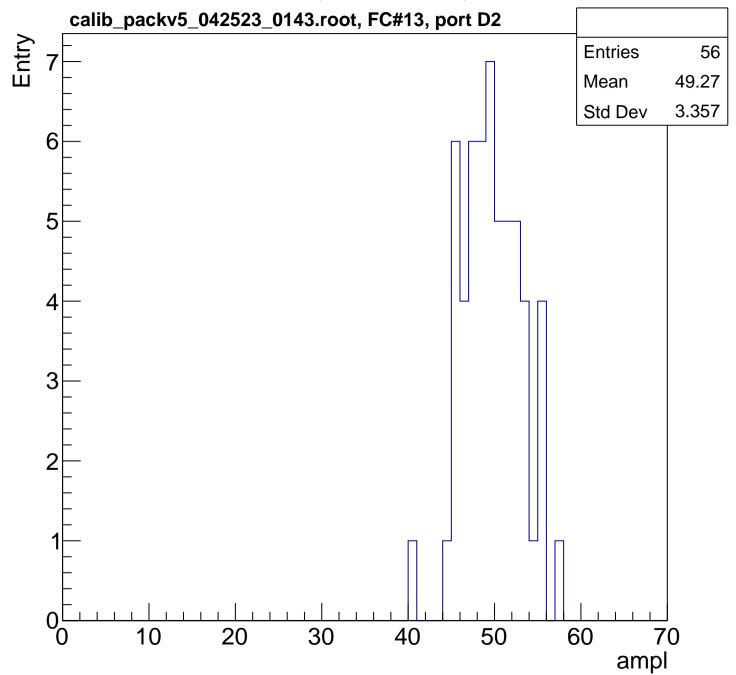


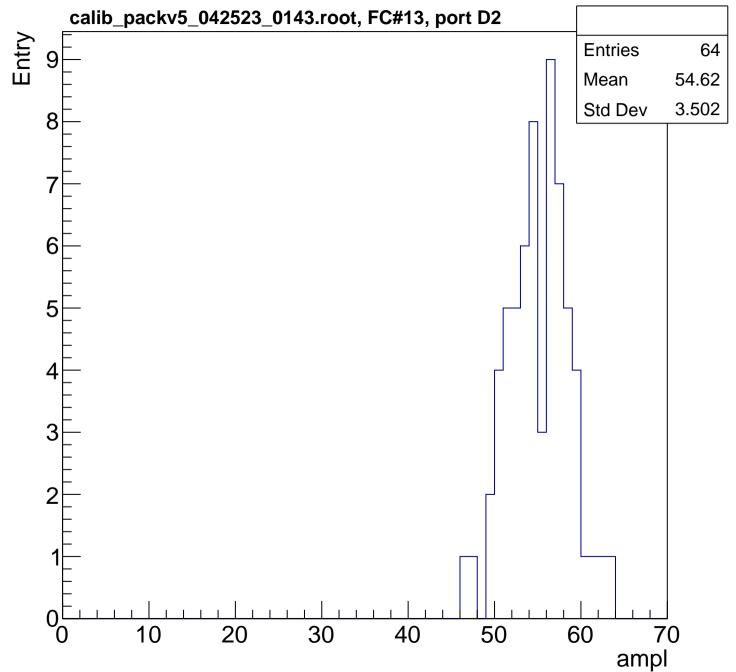


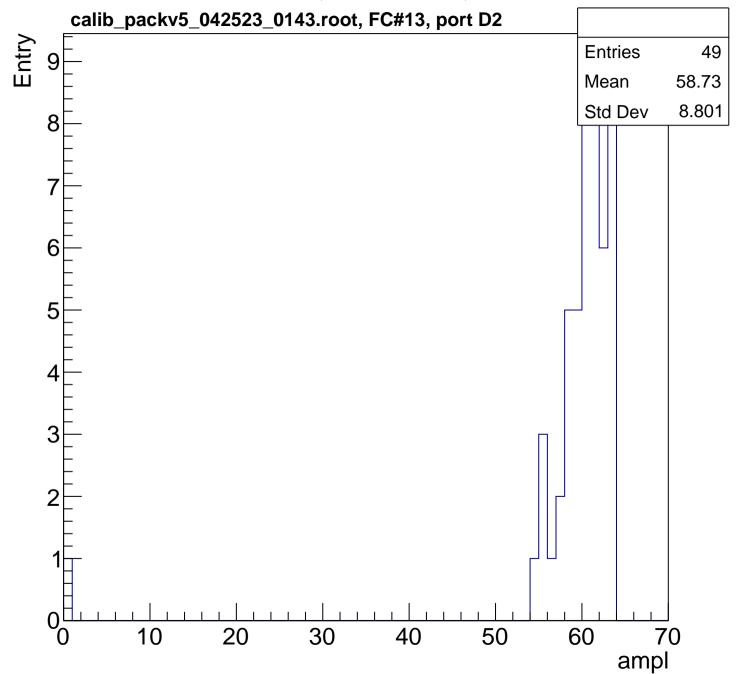


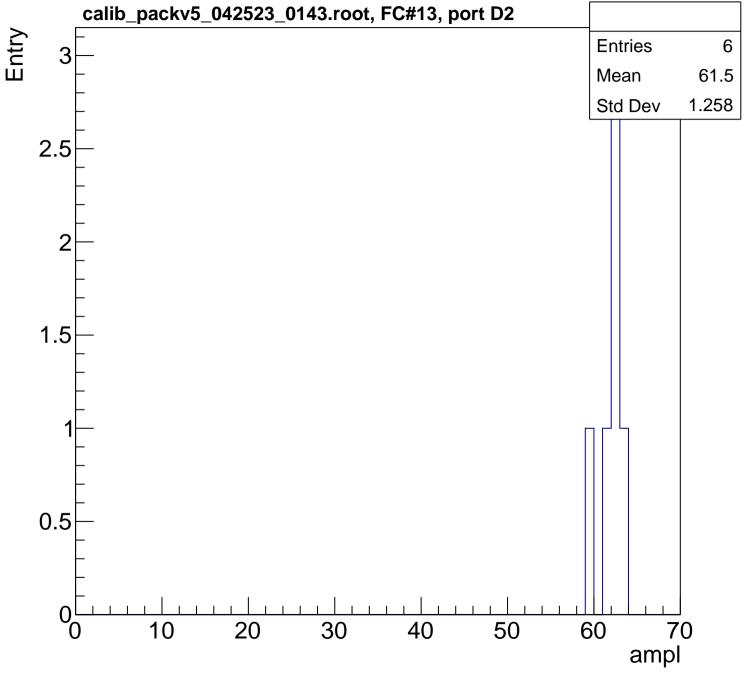


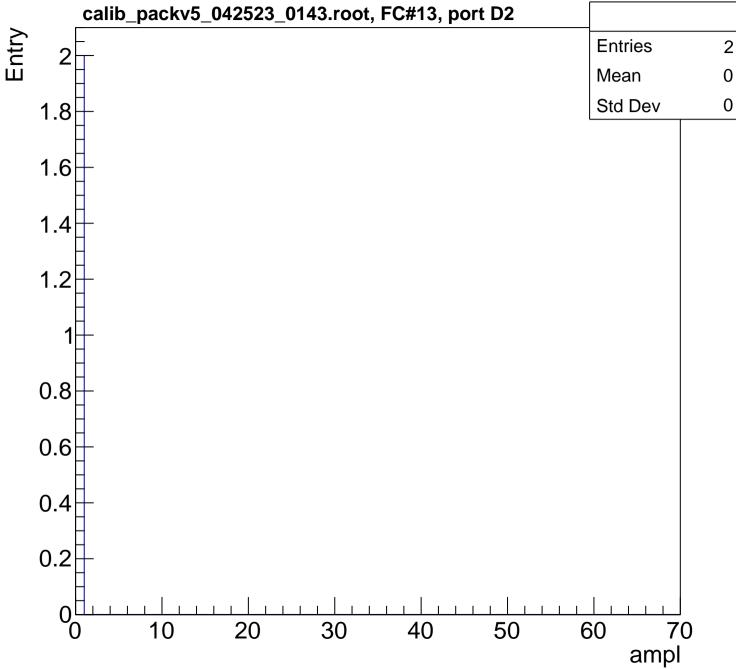


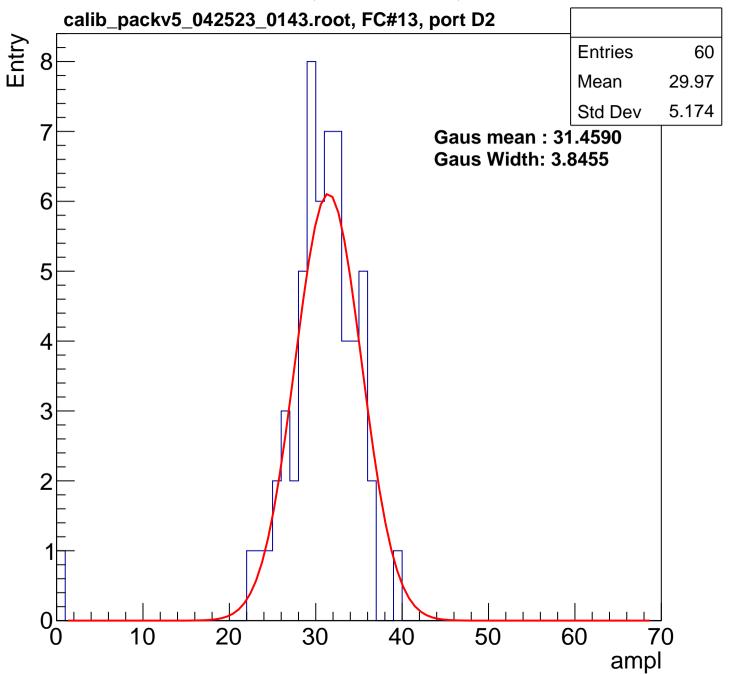


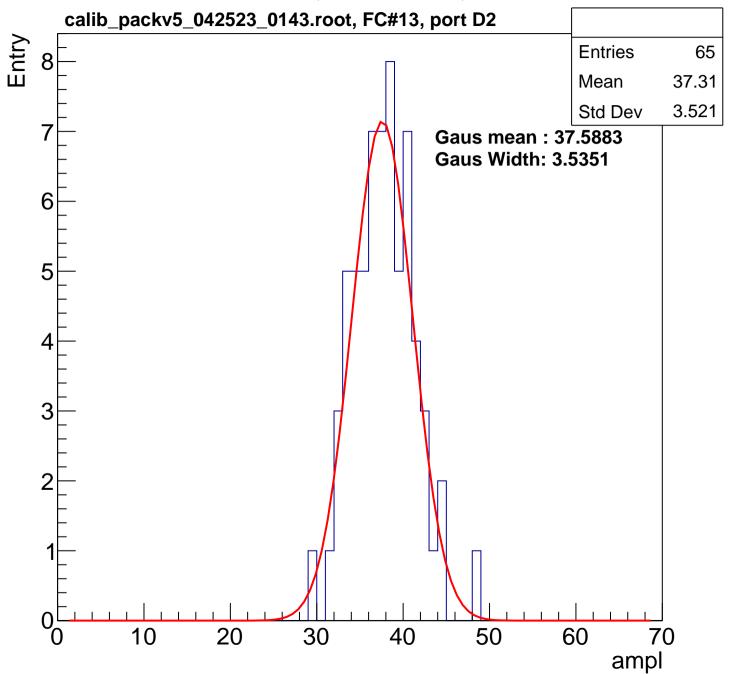


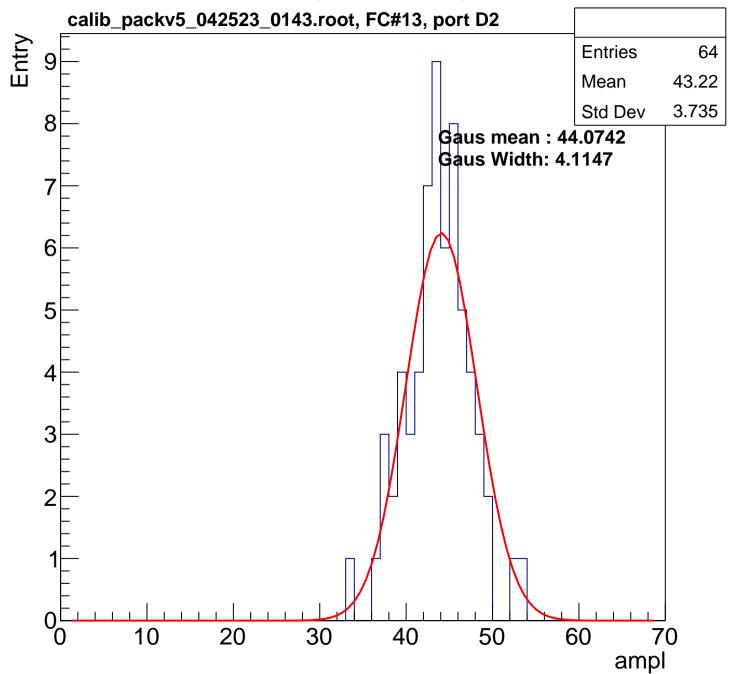


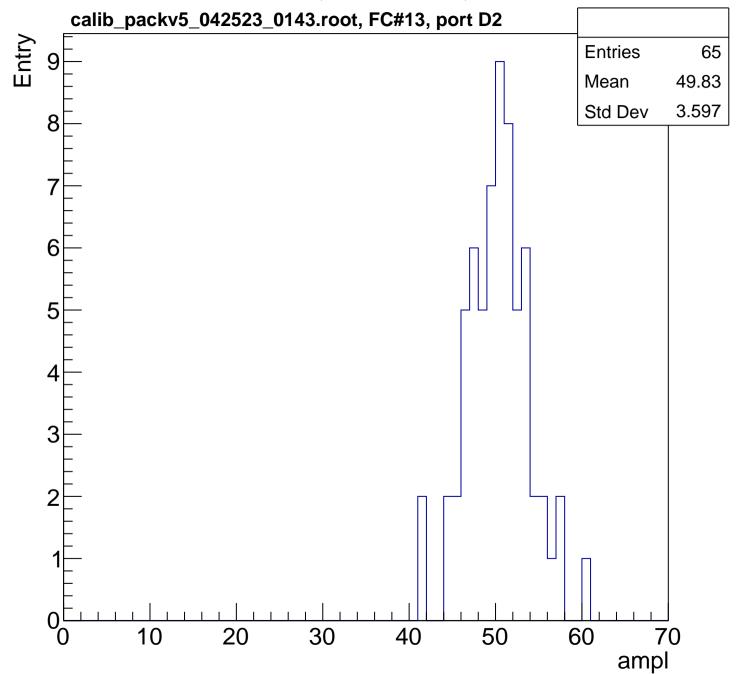


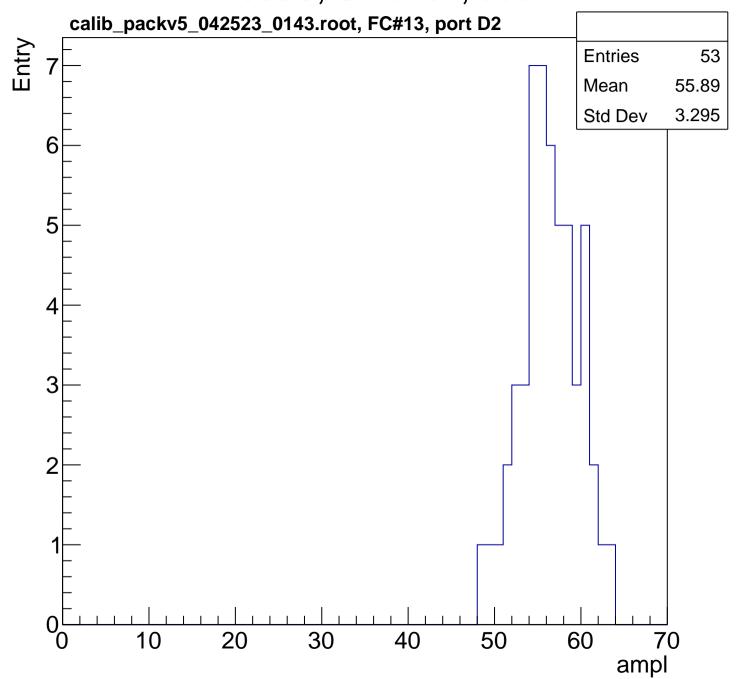


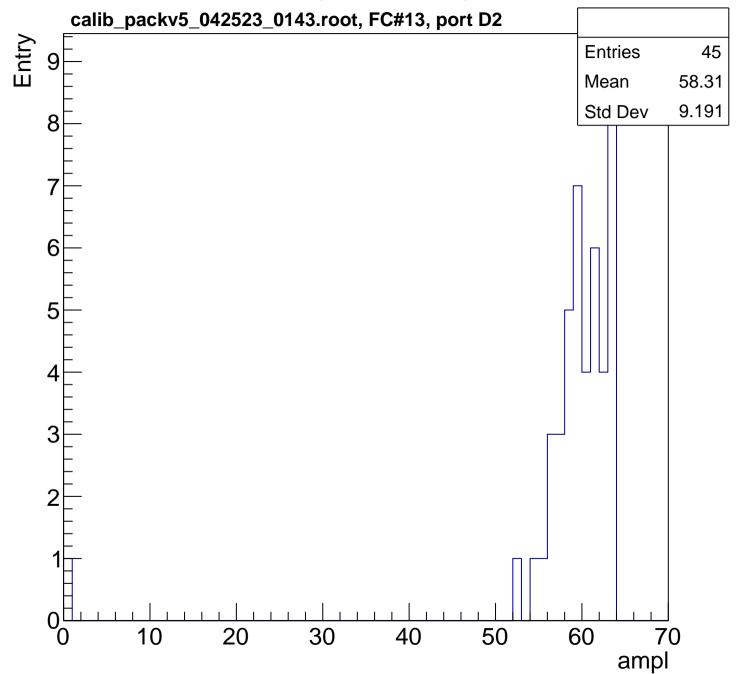


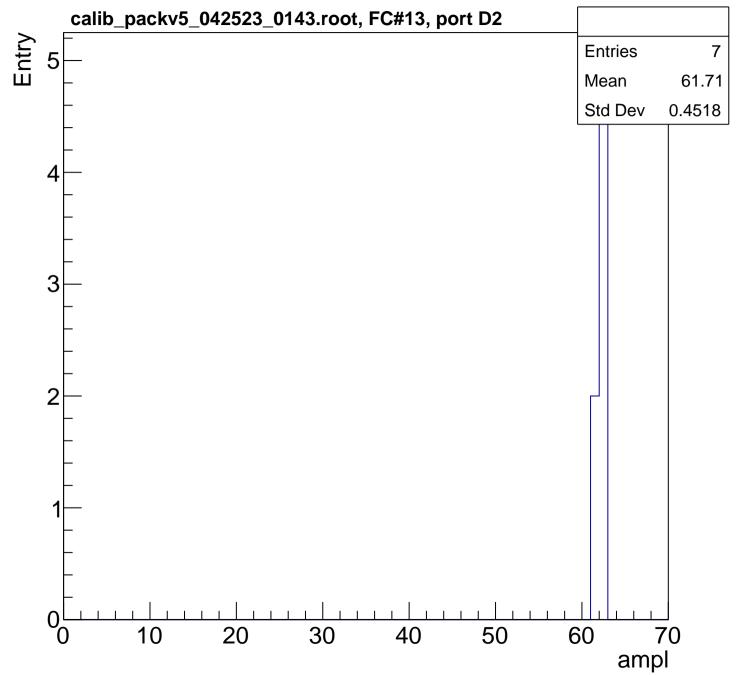


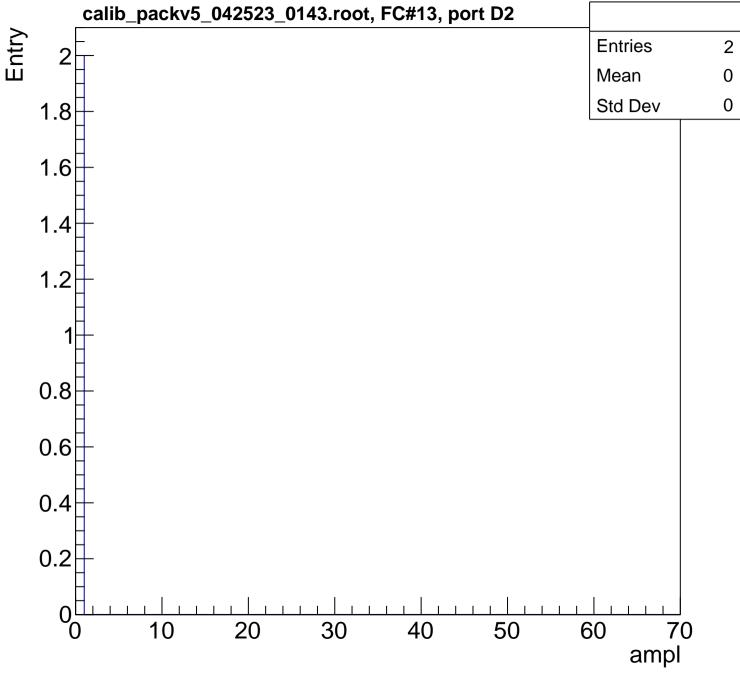


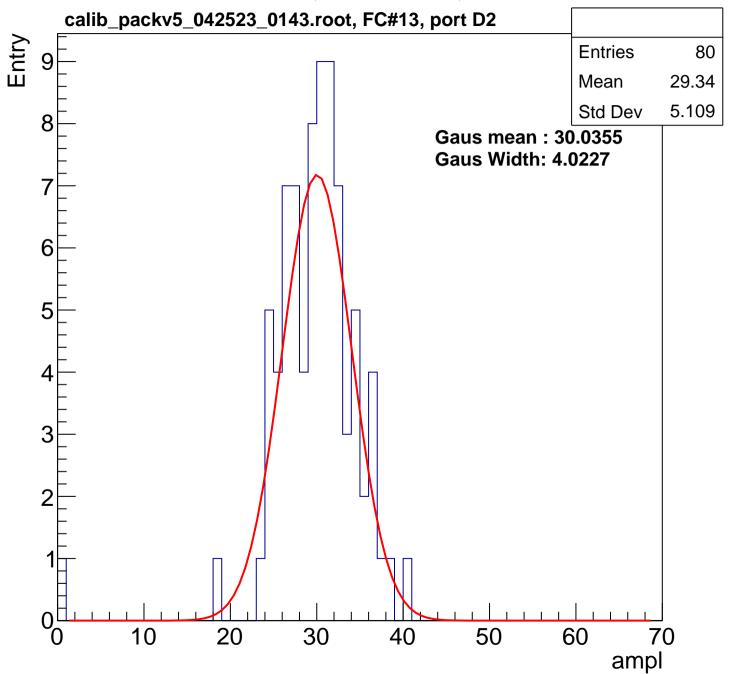


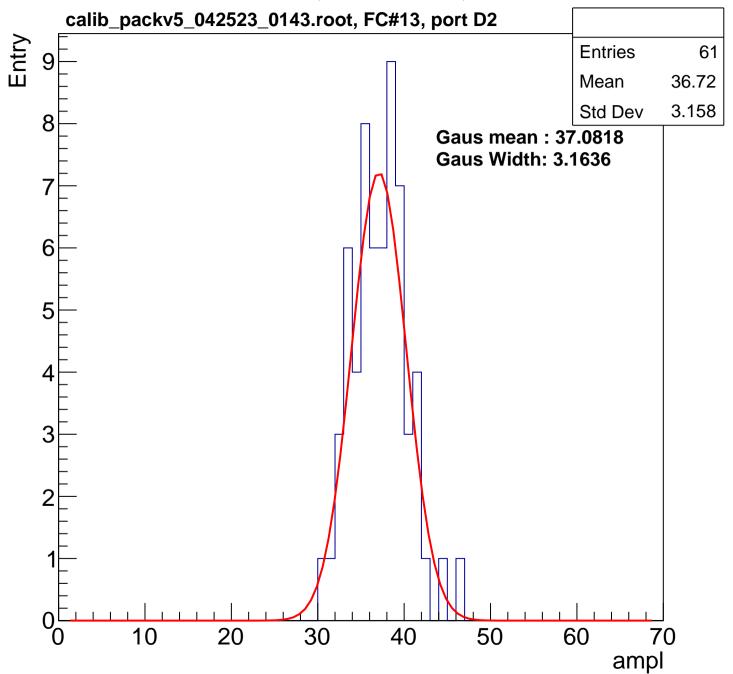


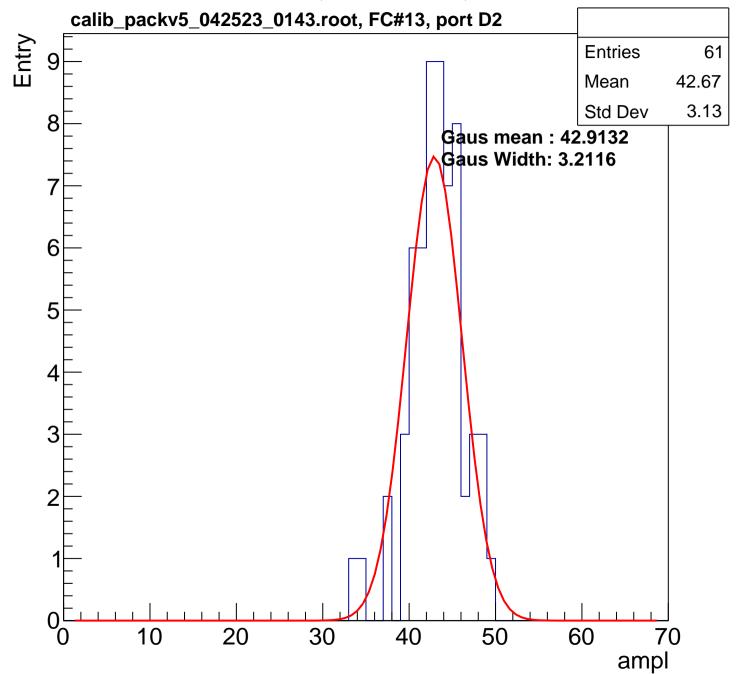


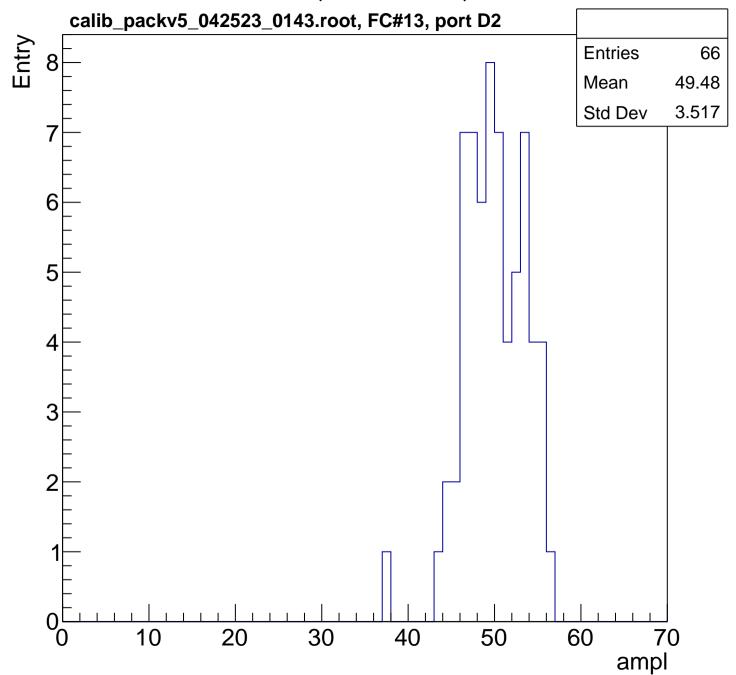


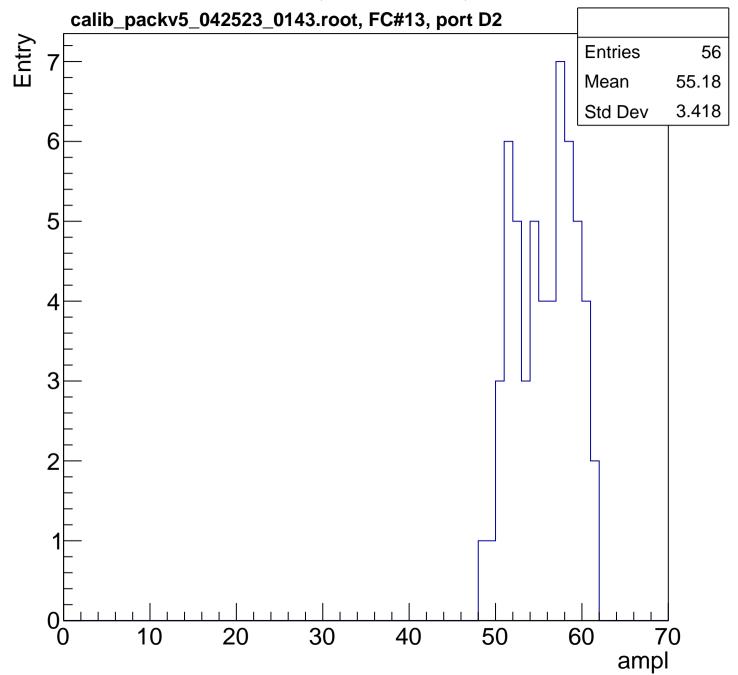


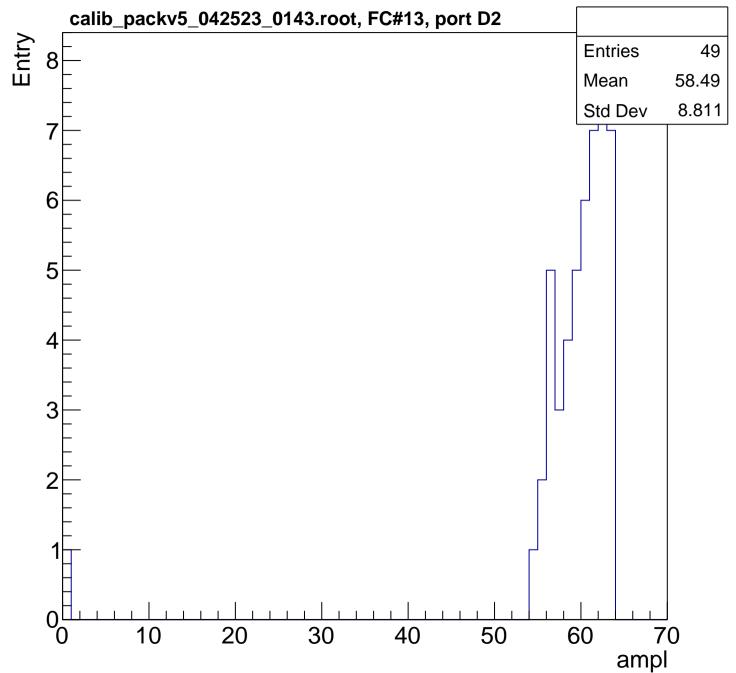


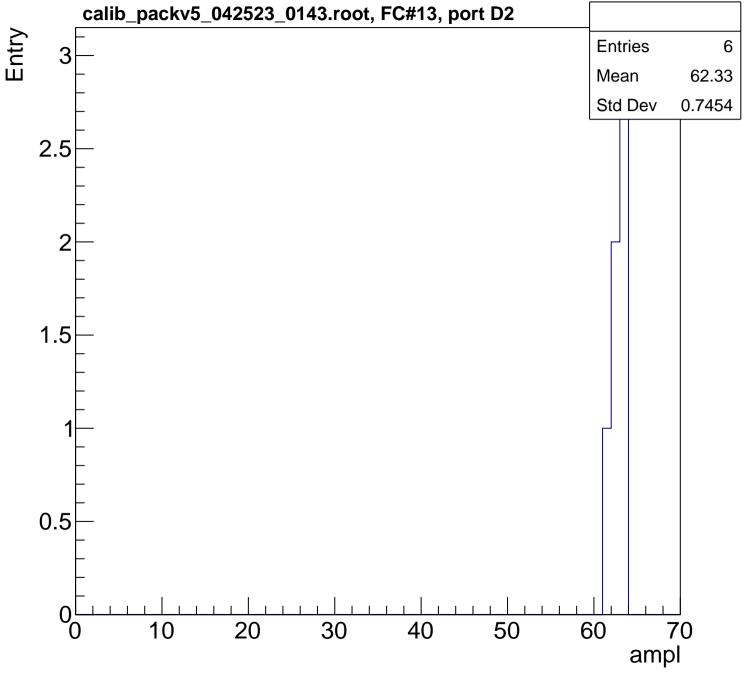




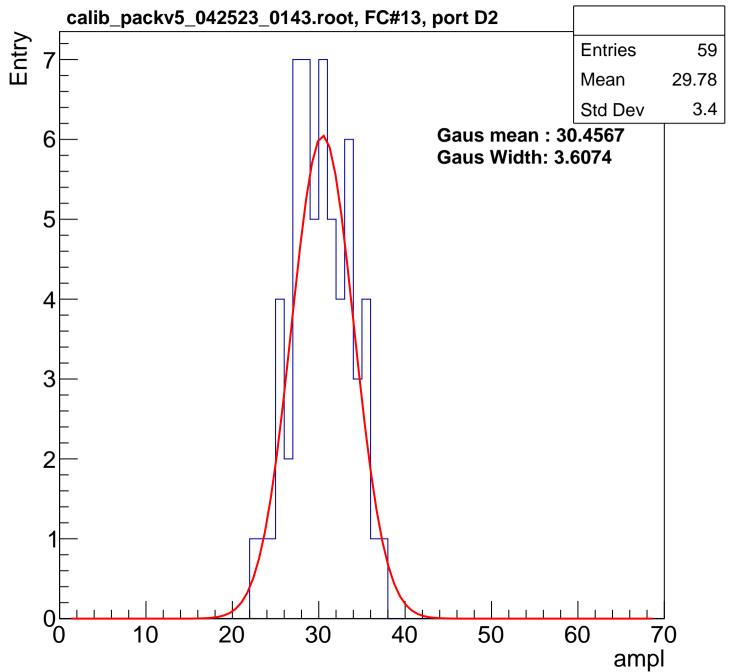


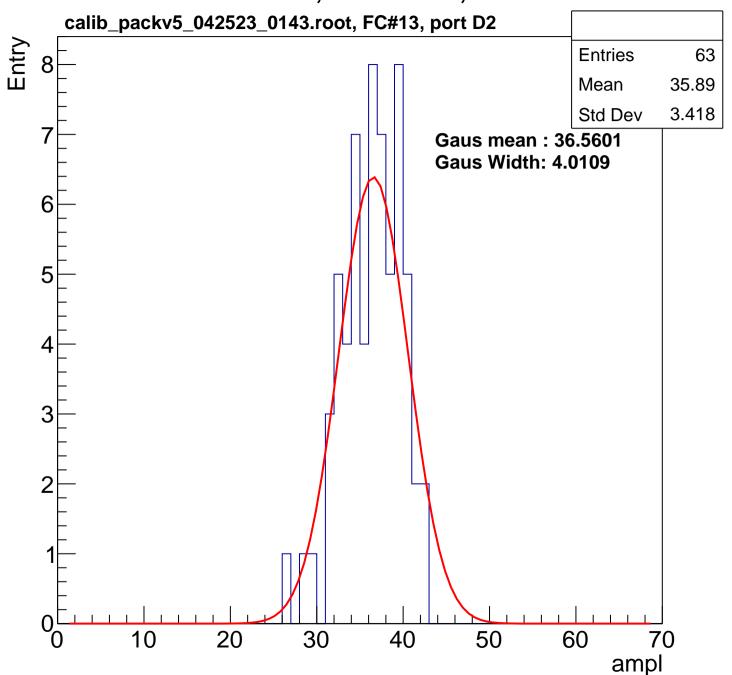


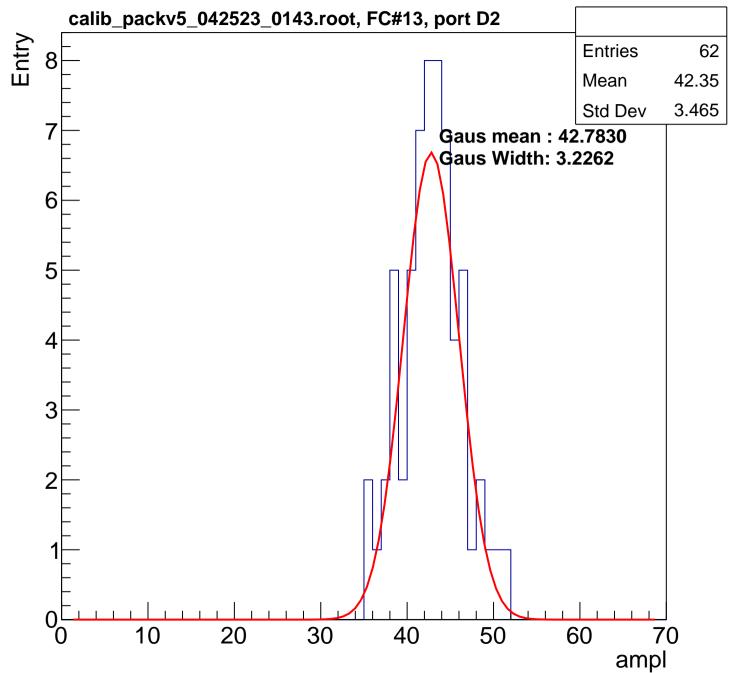


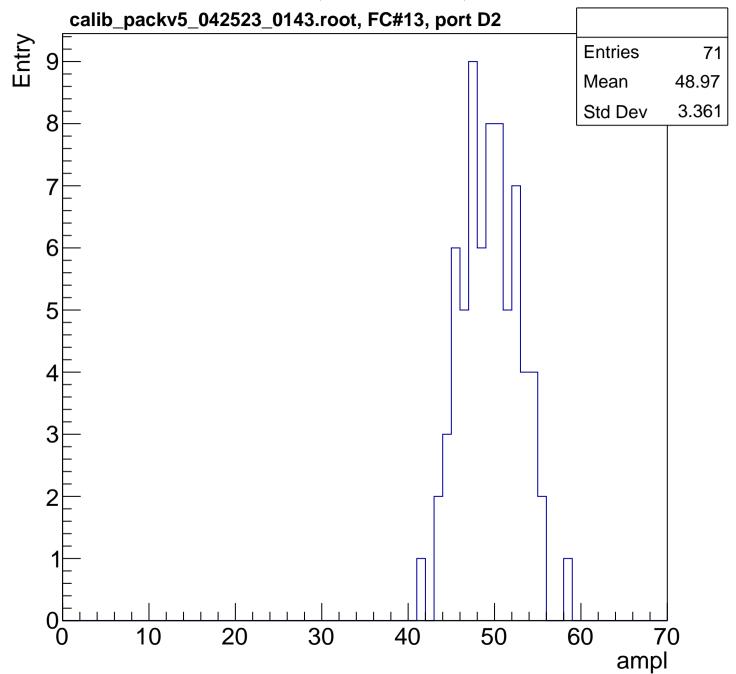


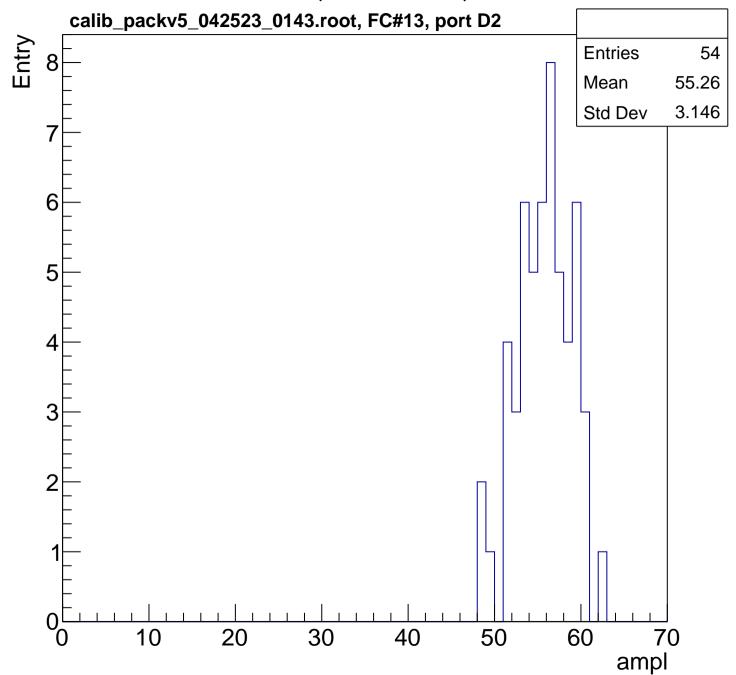
B1L003S, U4-ch85, adc7 calib_packv5_042523_0143.root, FC#13, port D2 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

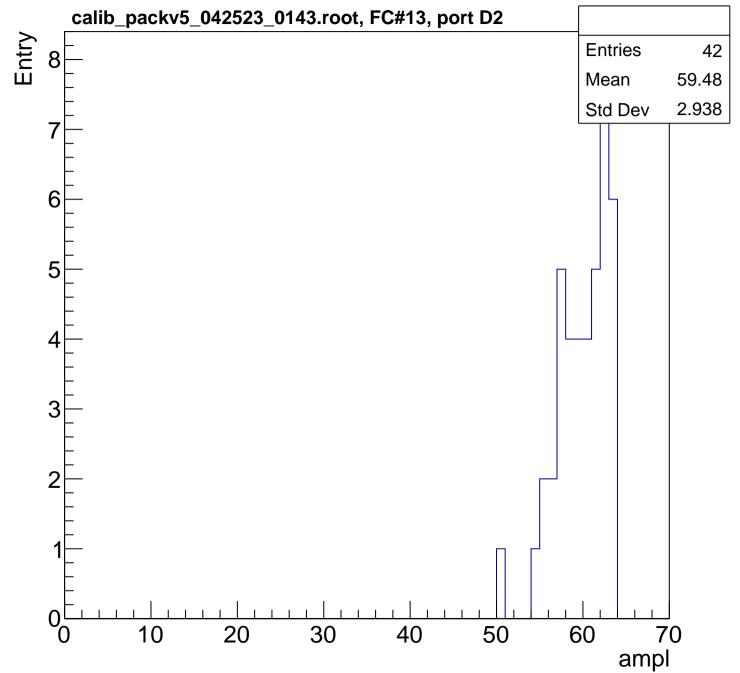


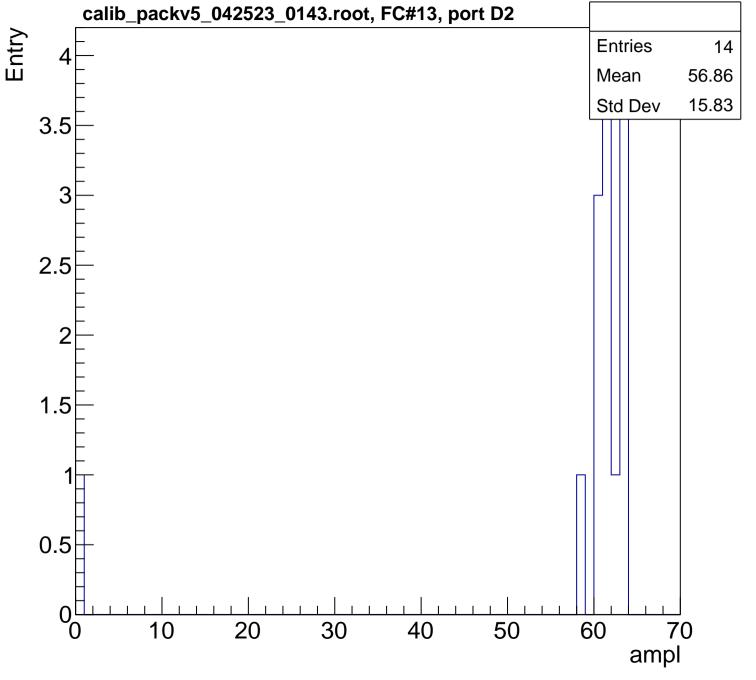


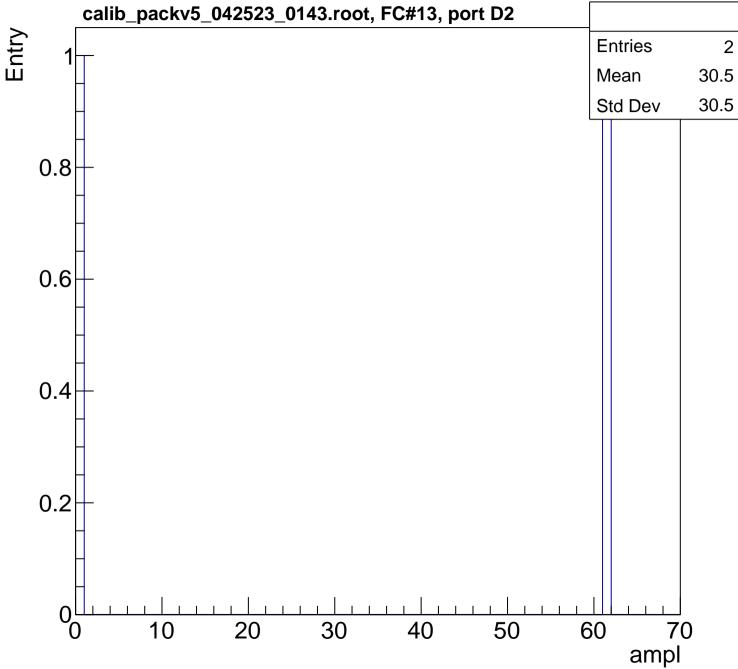


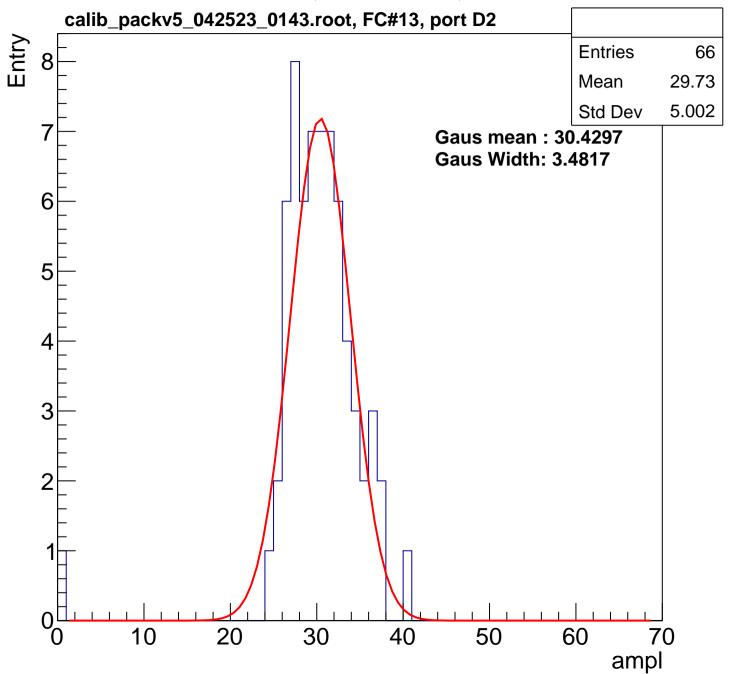


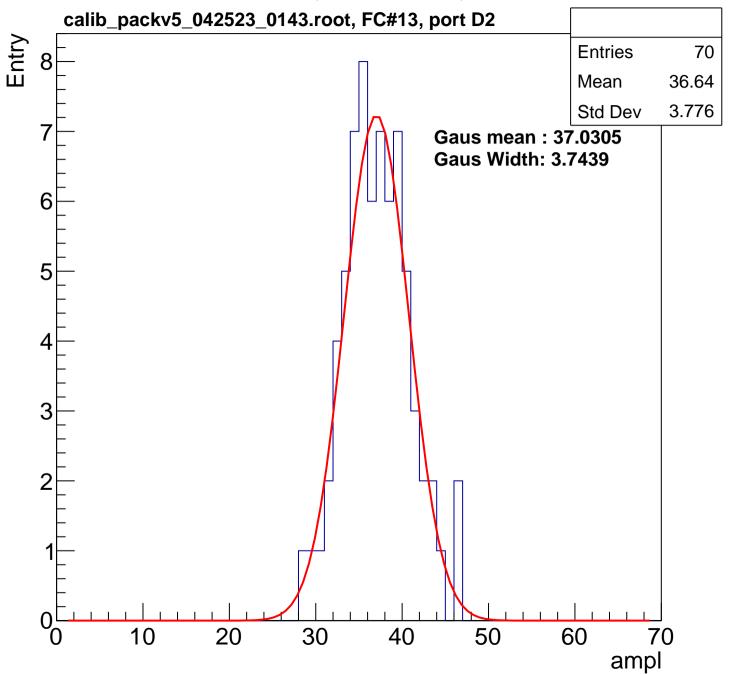


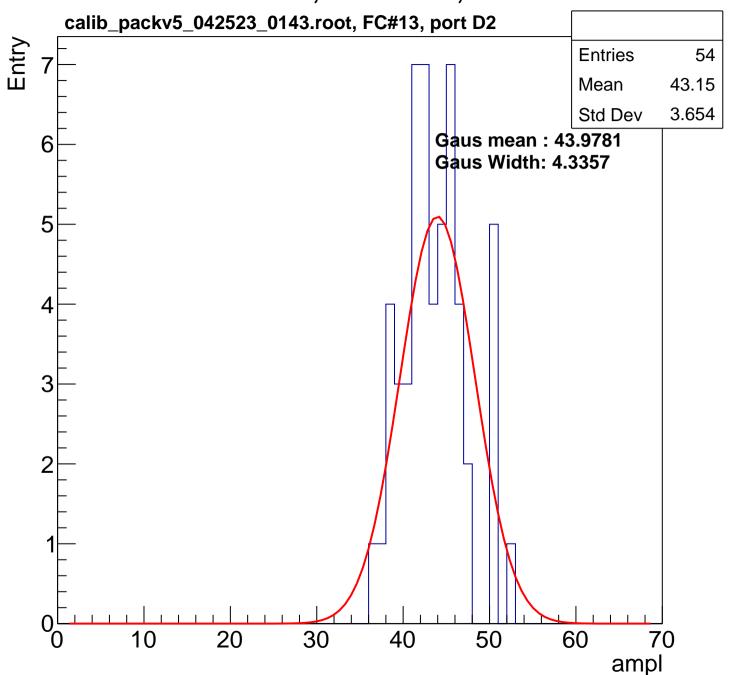


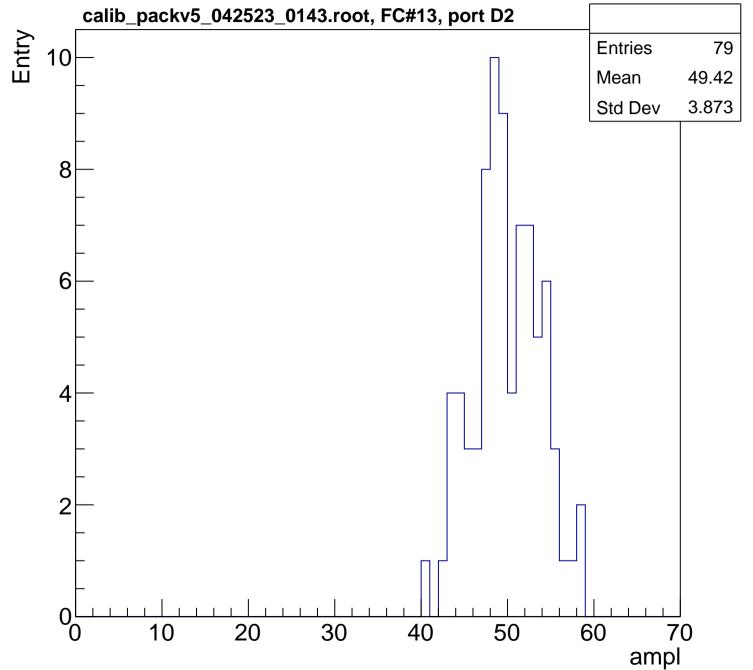


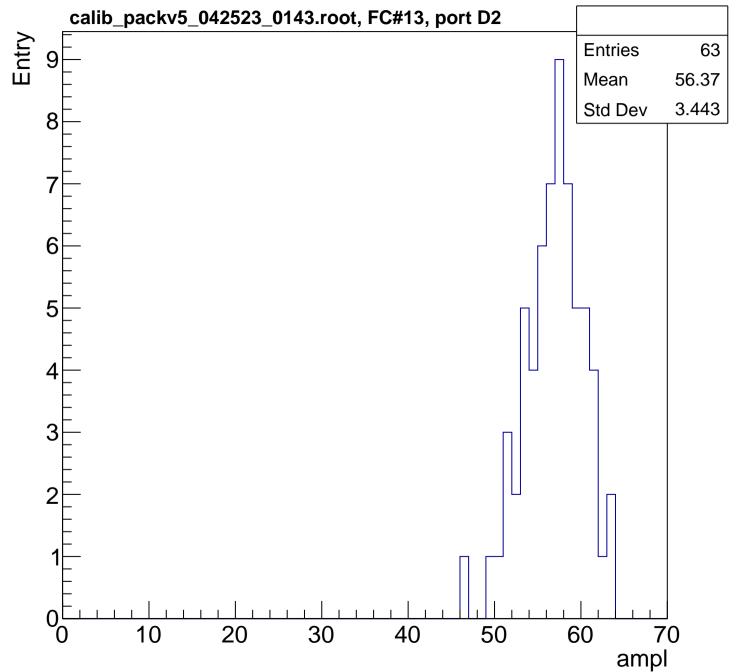


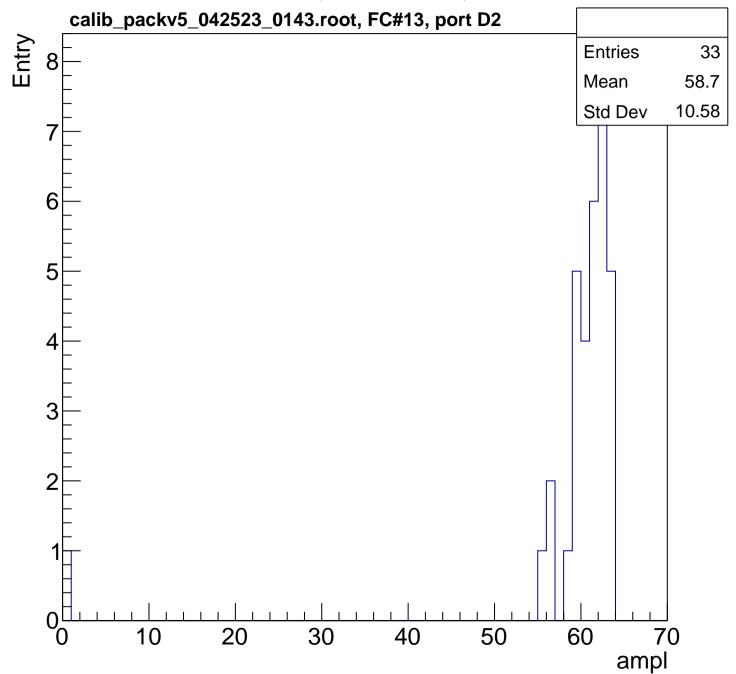


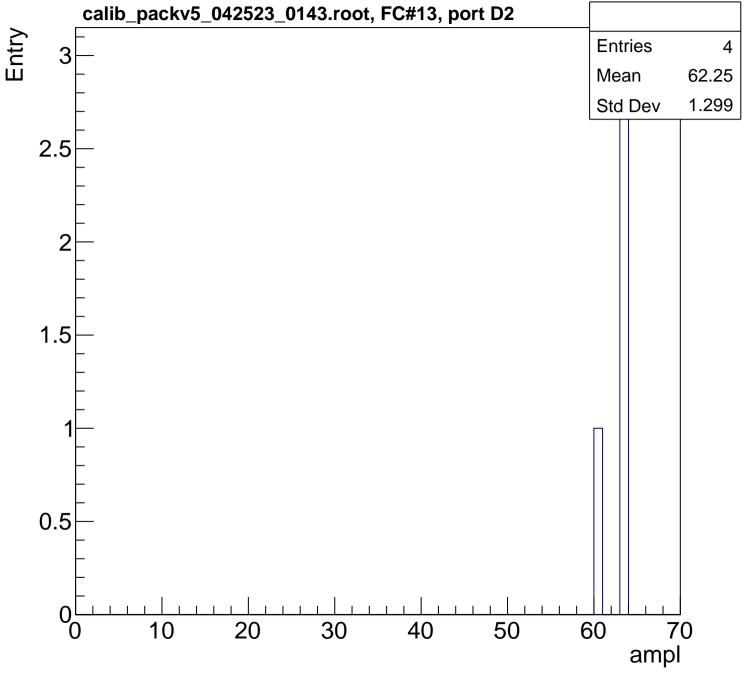


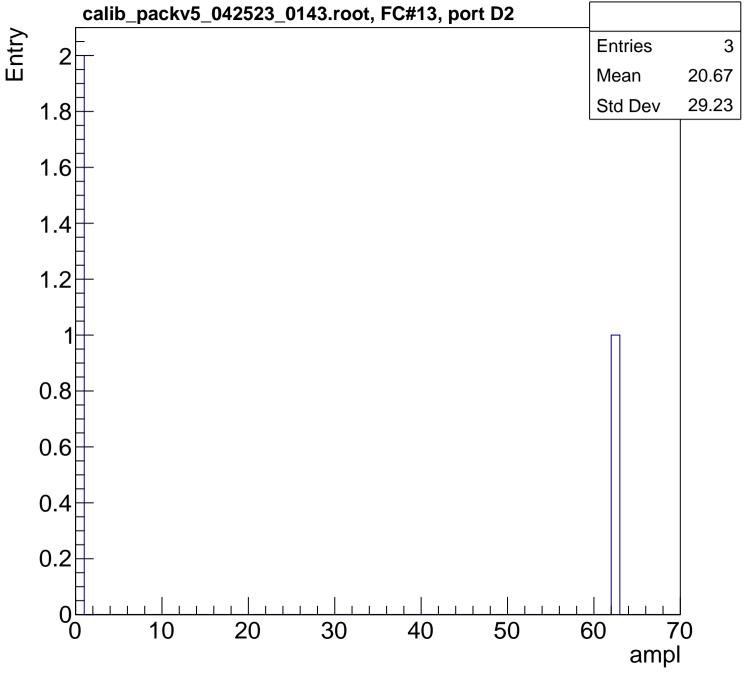


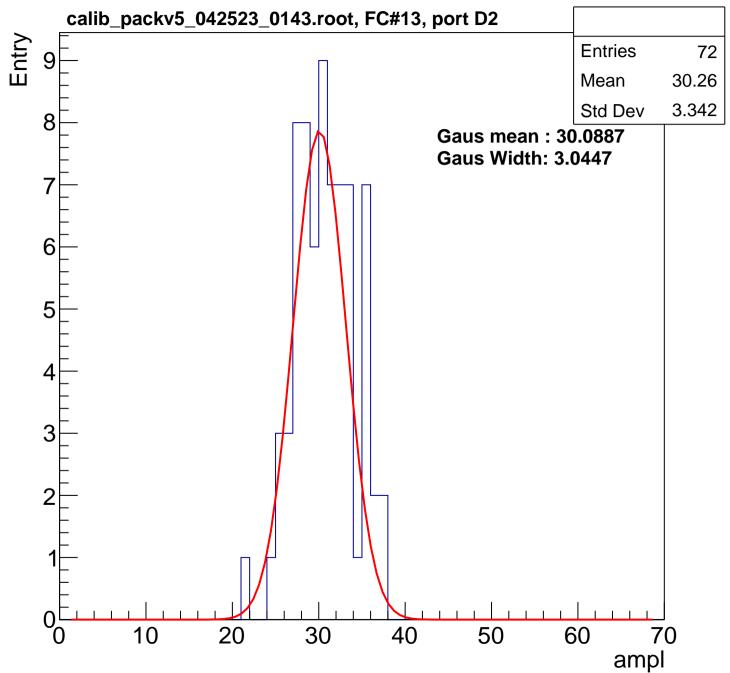


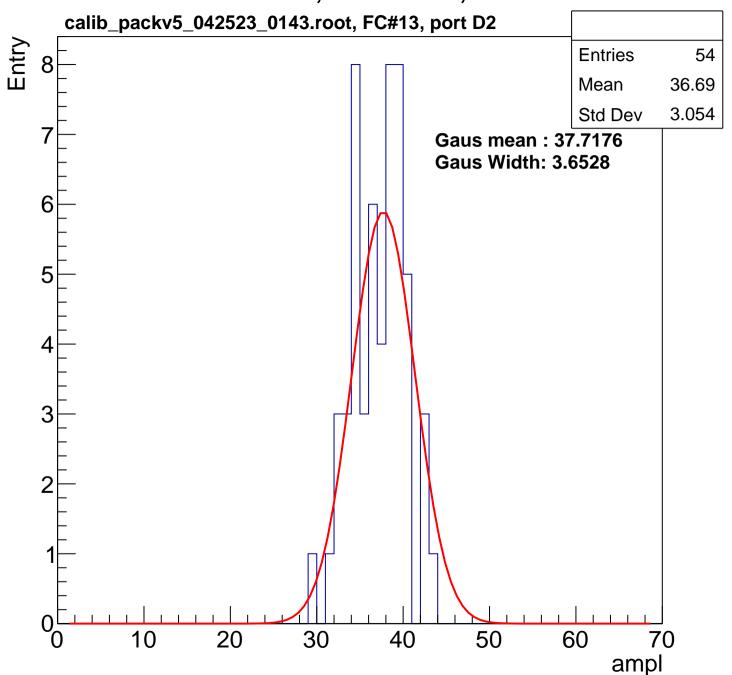


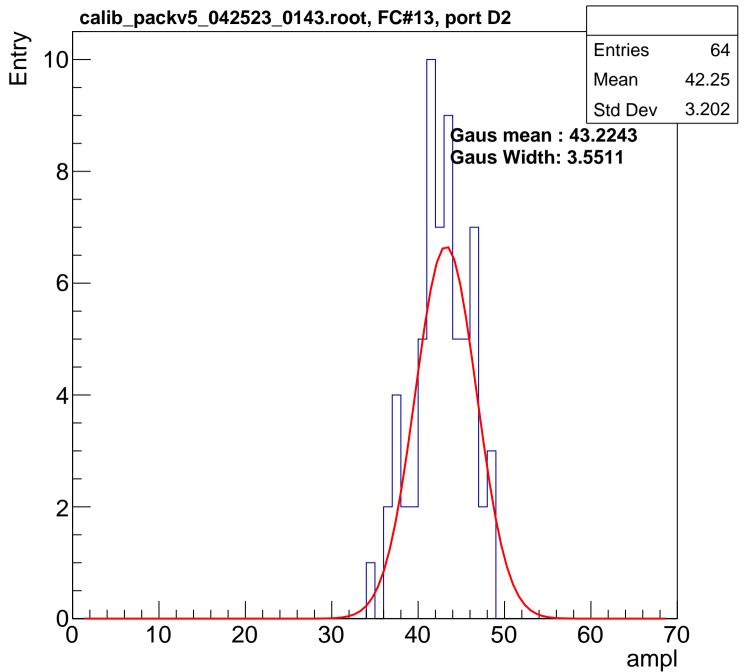


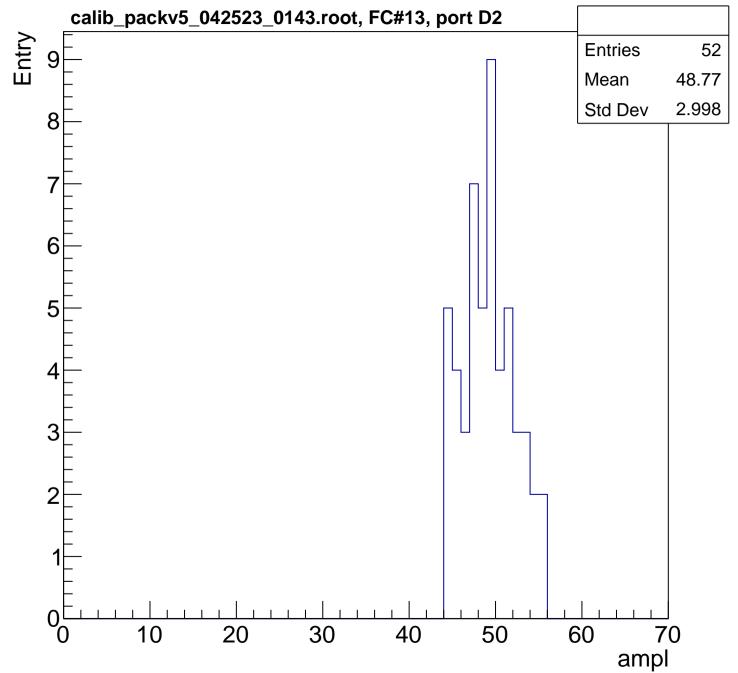


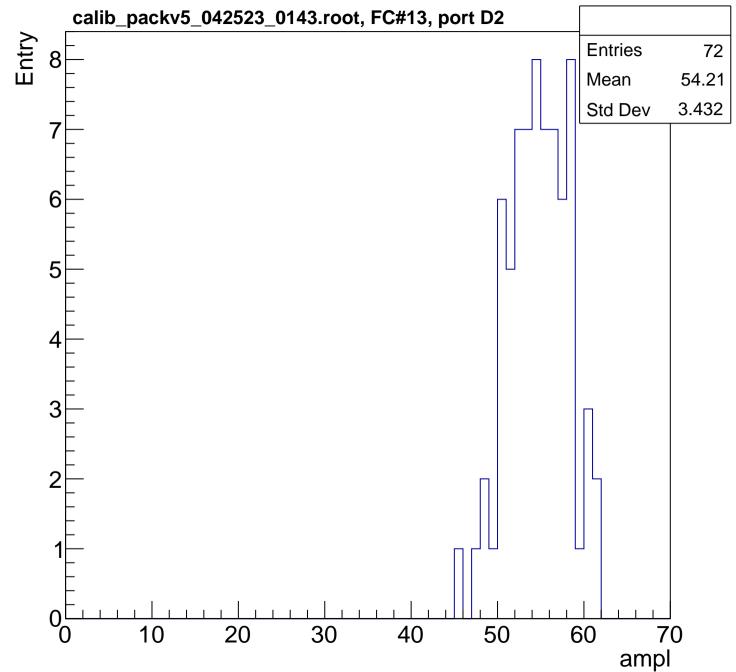


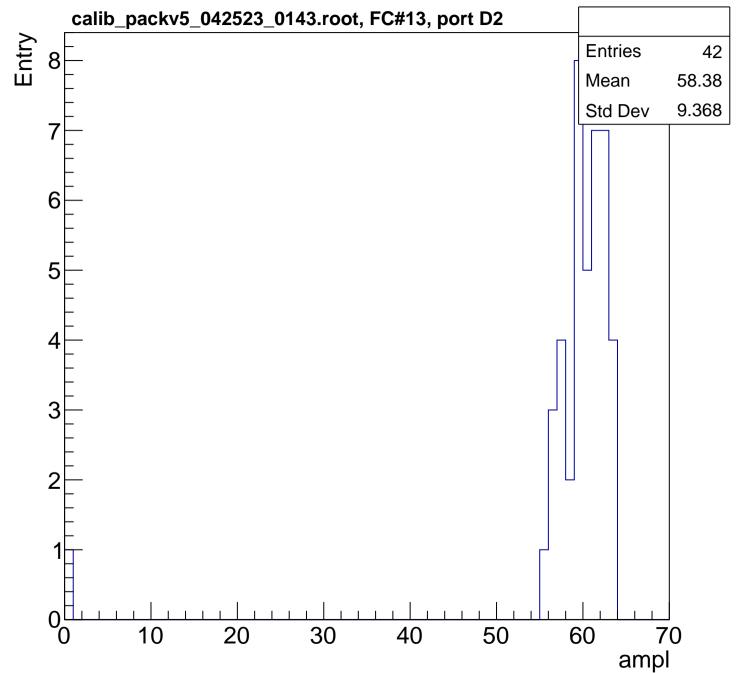


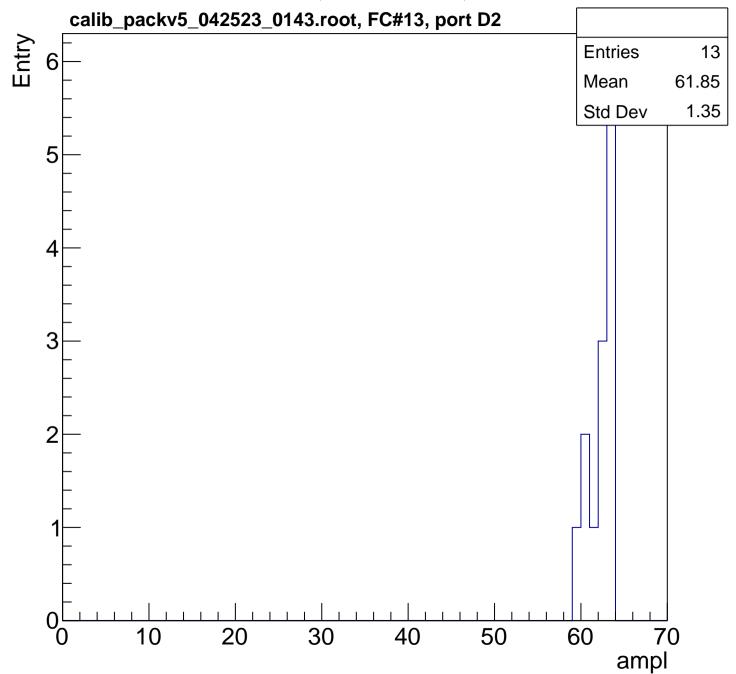


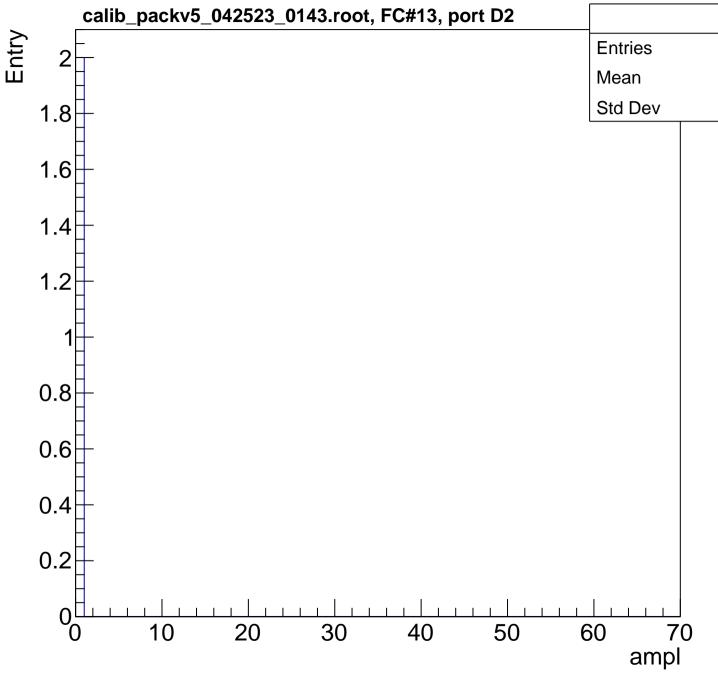


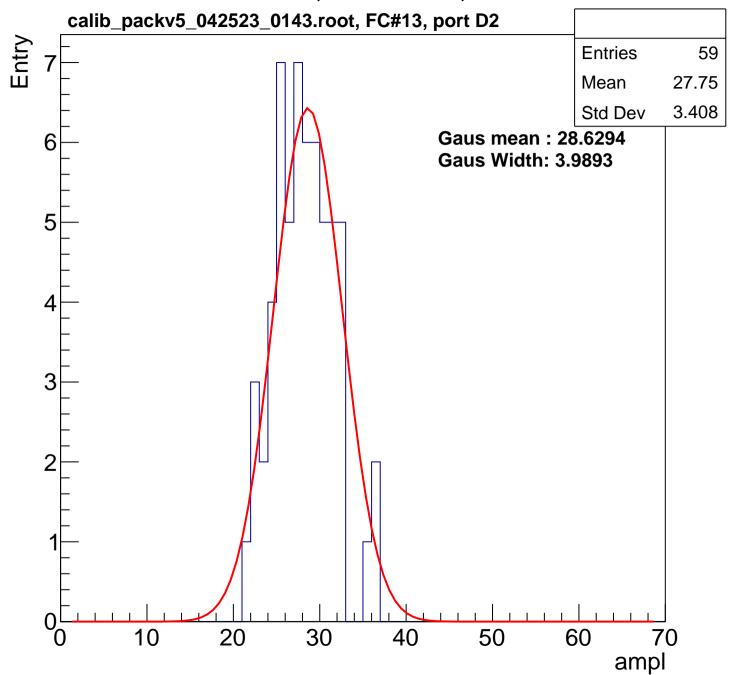


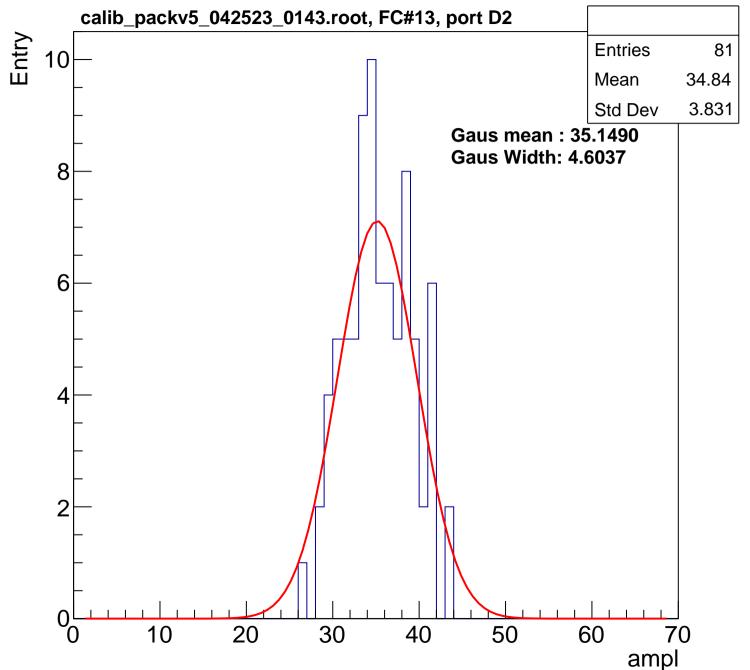


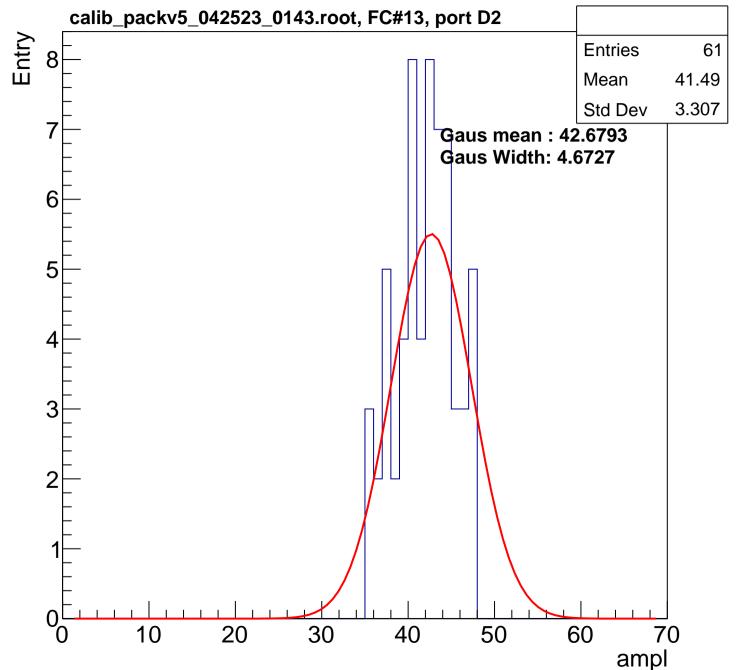


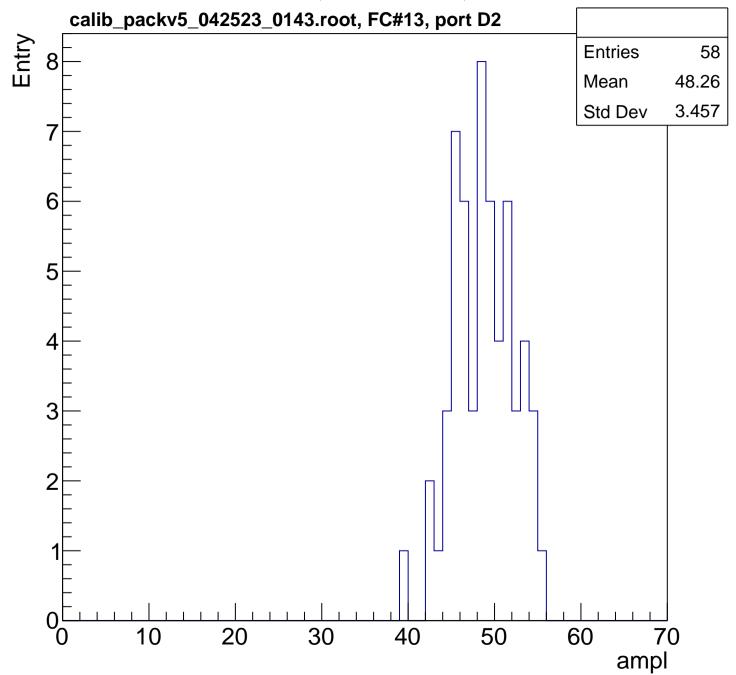


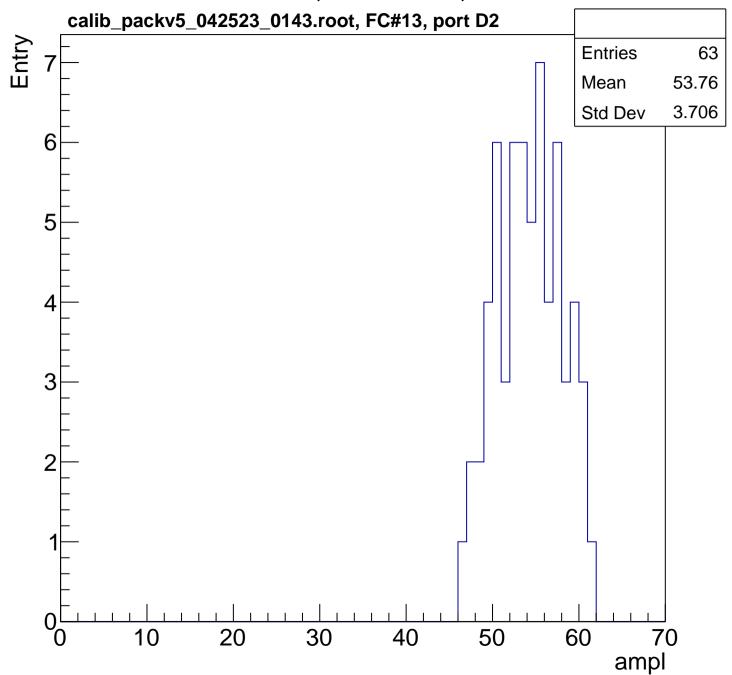


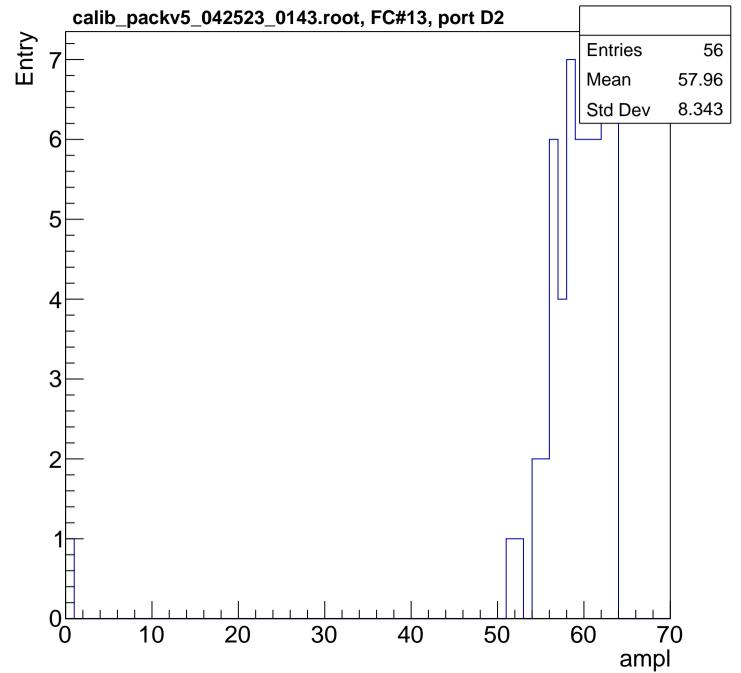


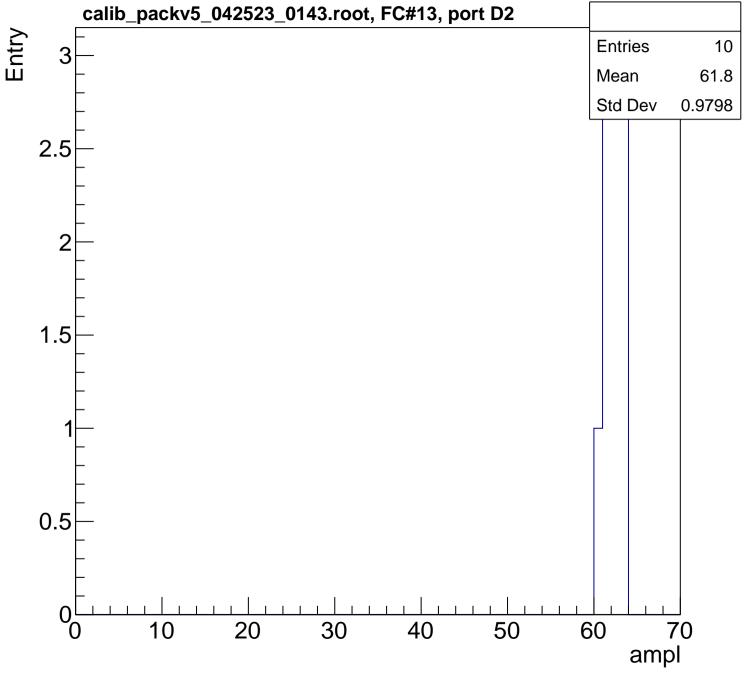




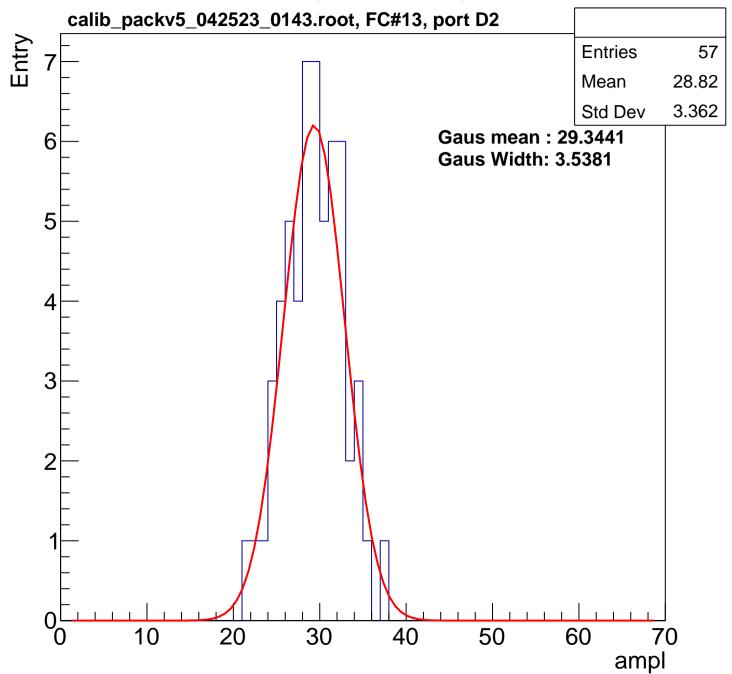


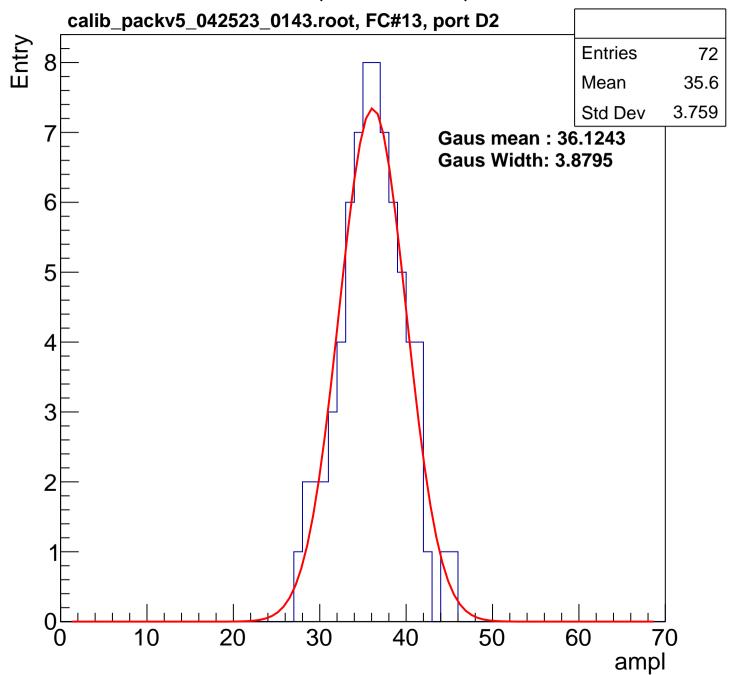


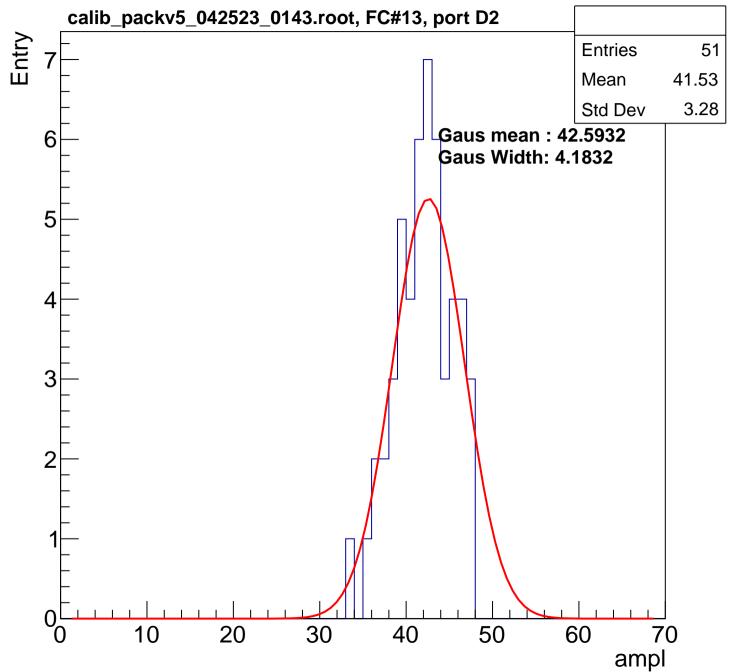


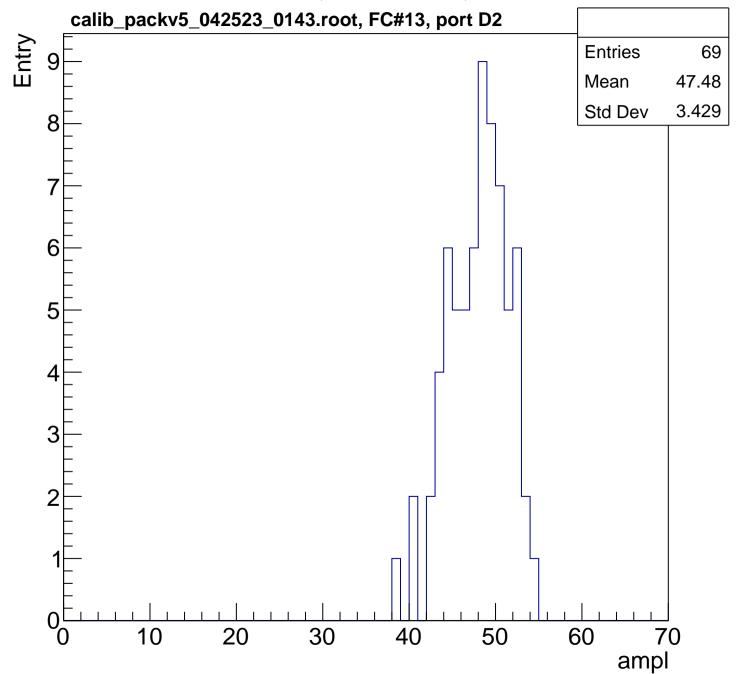


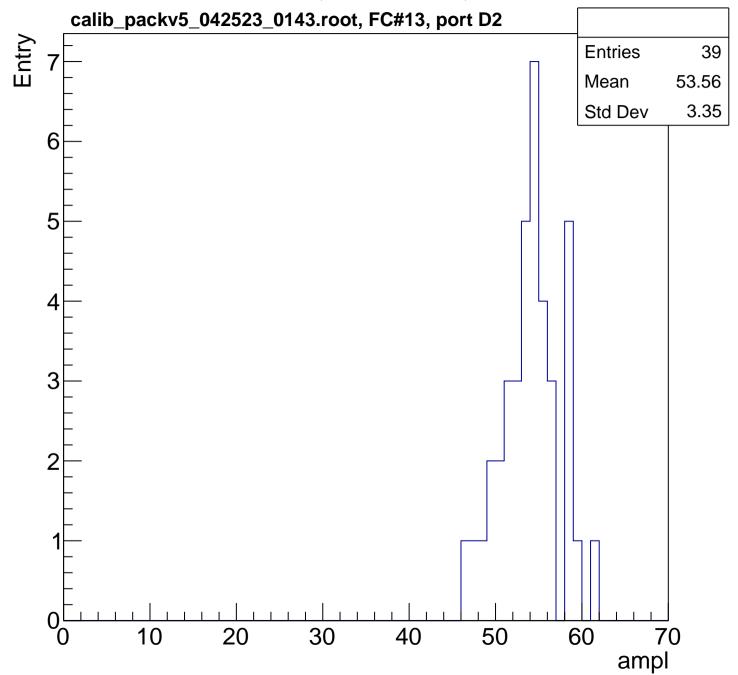
B1L003S, U4-ch89, adc7 calib_packv5_042523_0143.root, FC#13, port D2 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

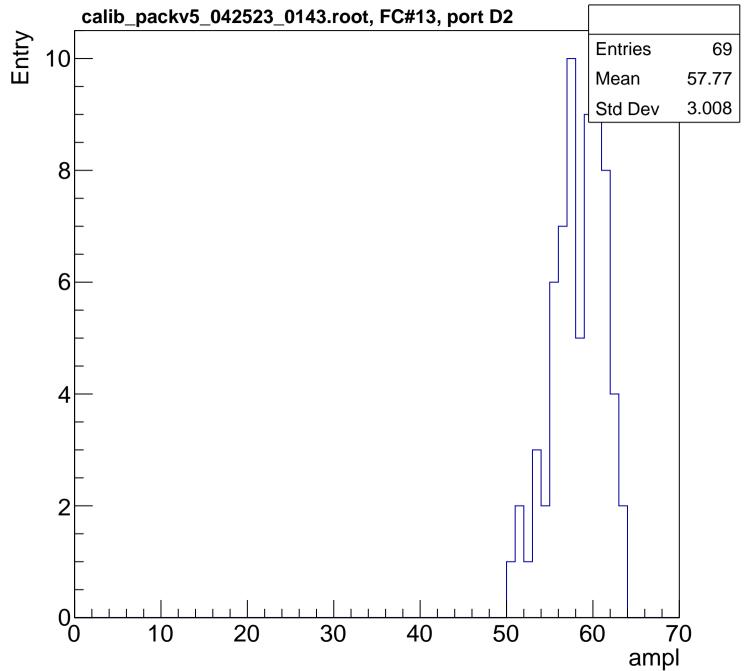


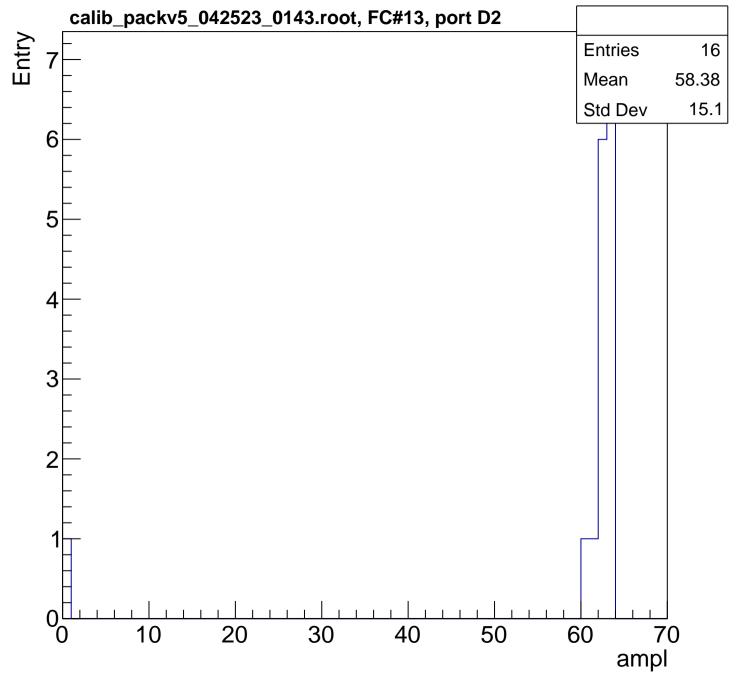


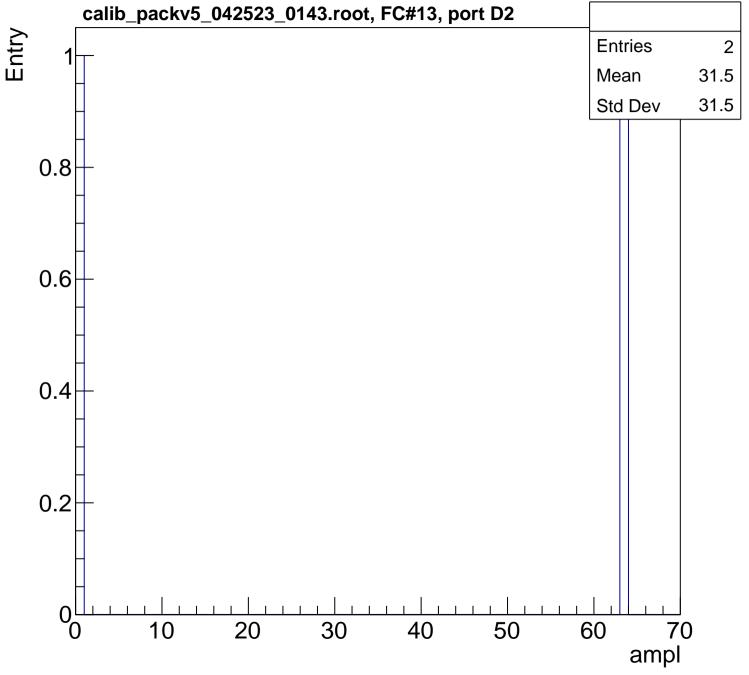


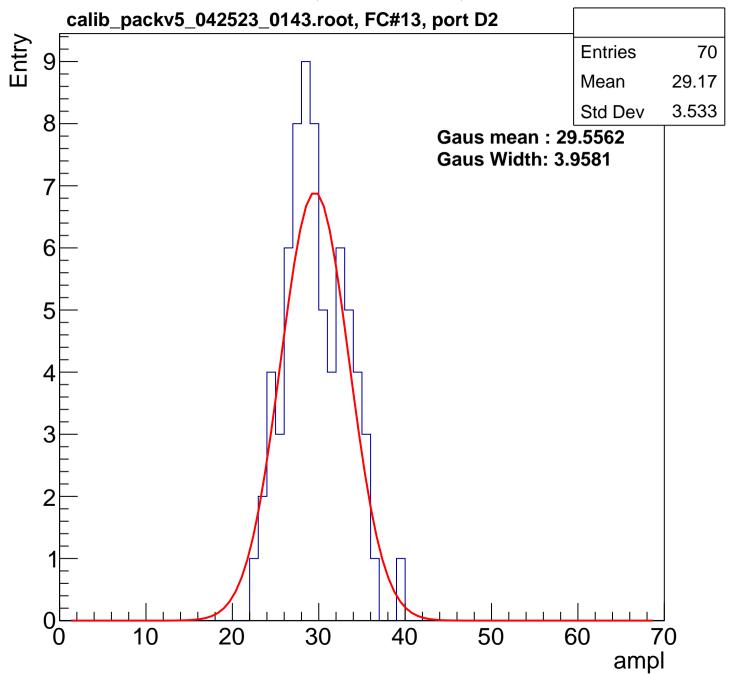


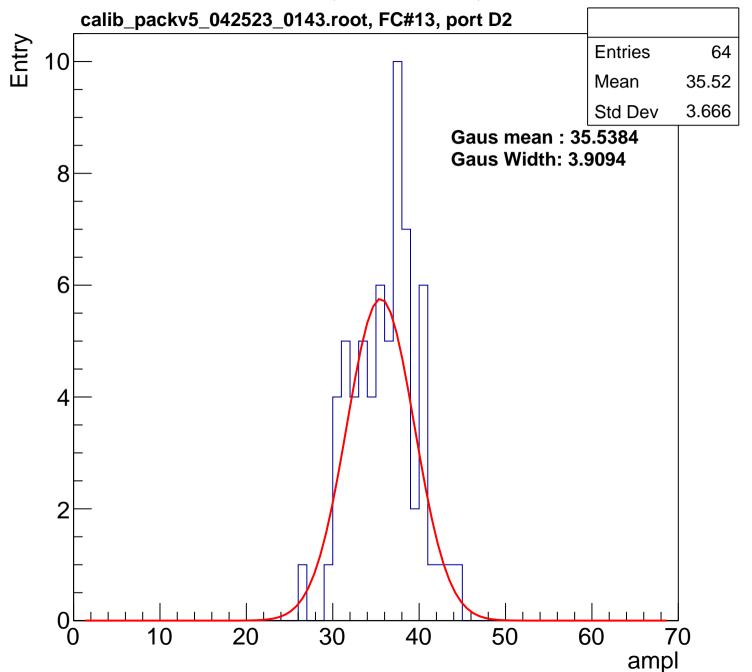


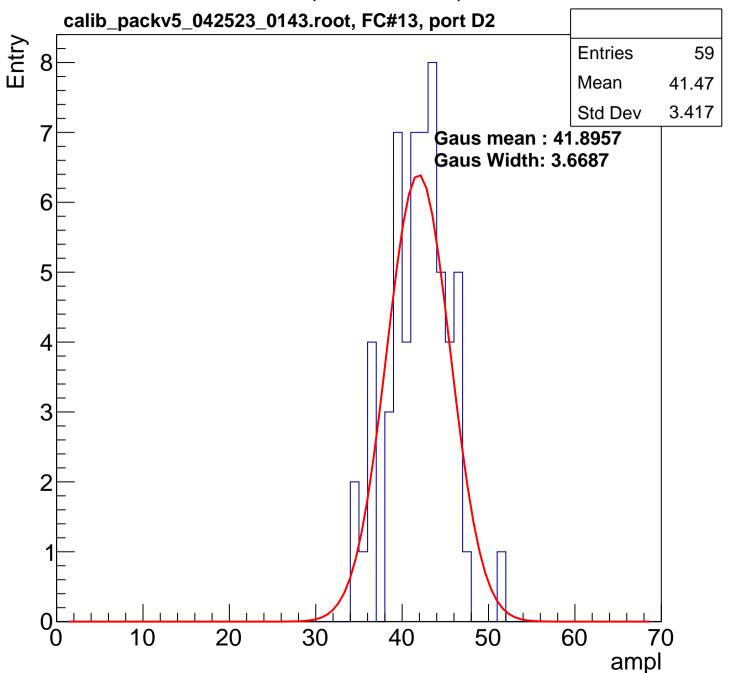


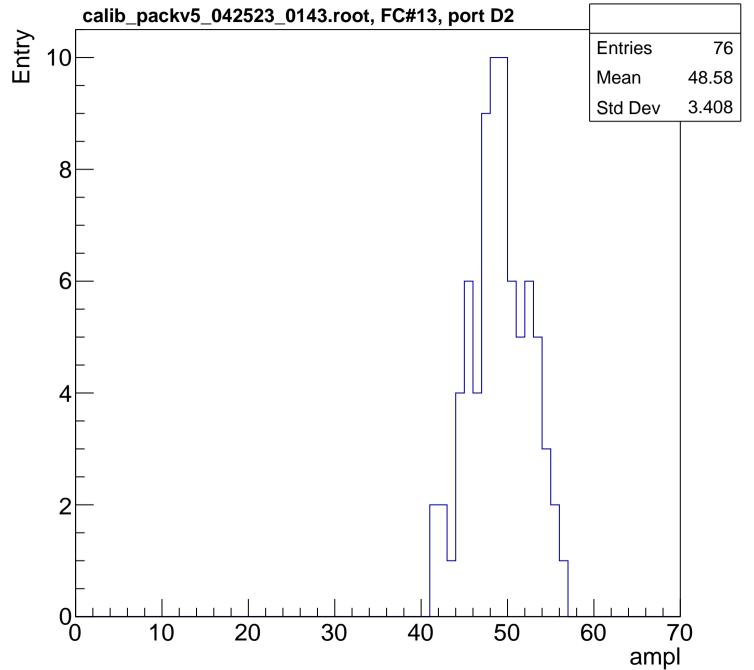


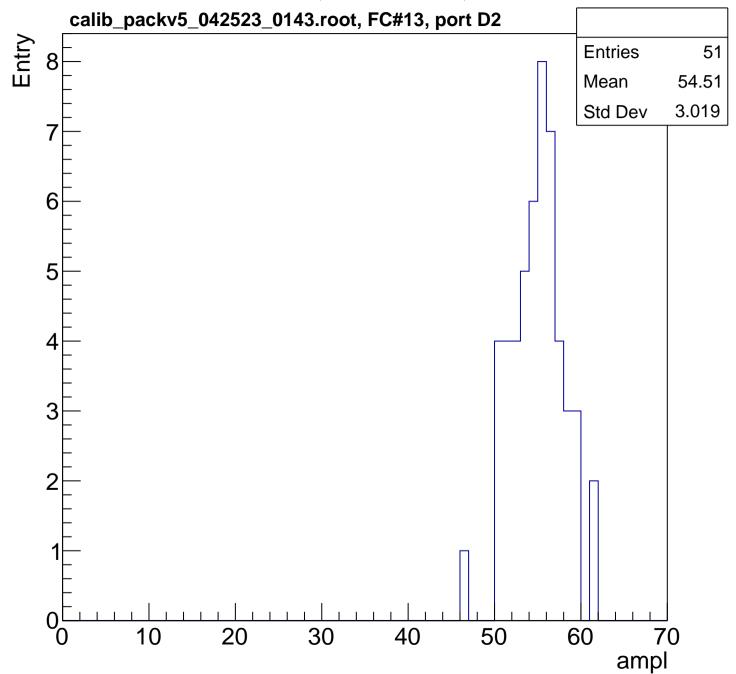


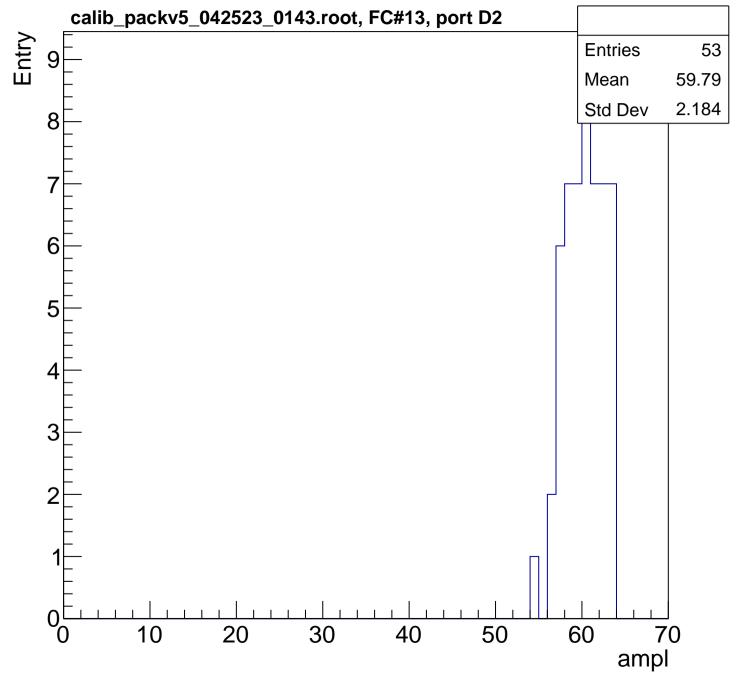


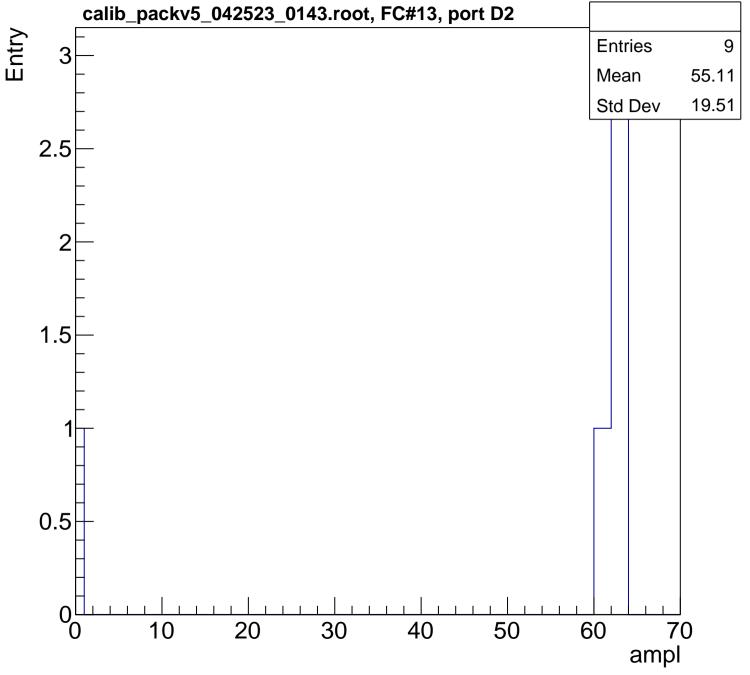




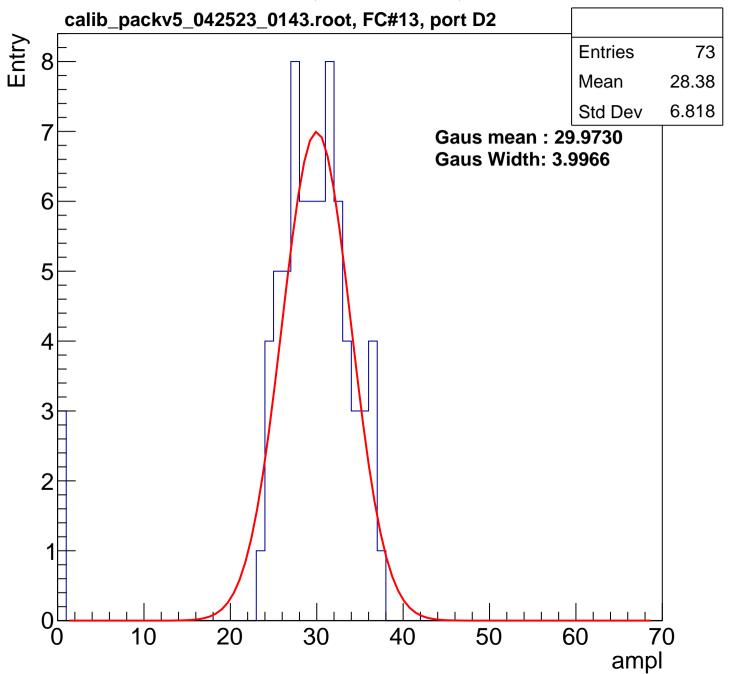


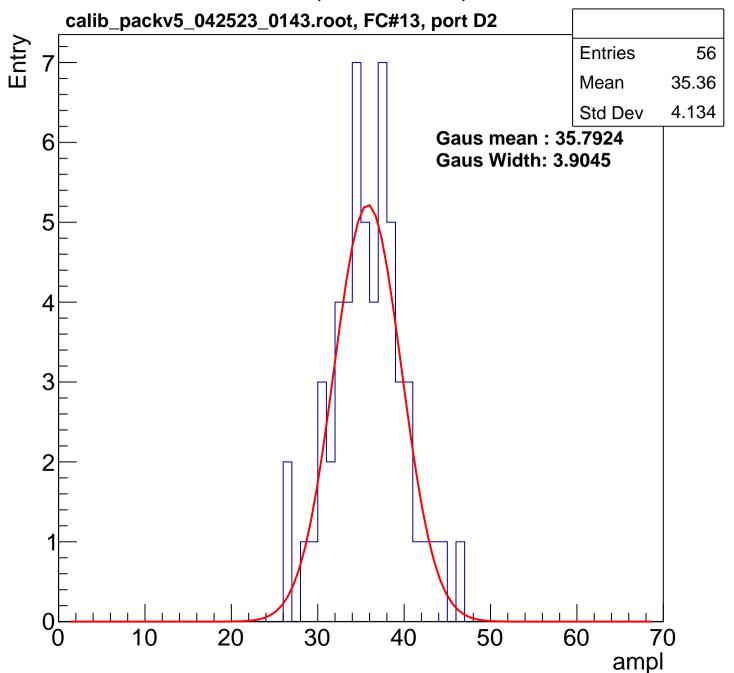


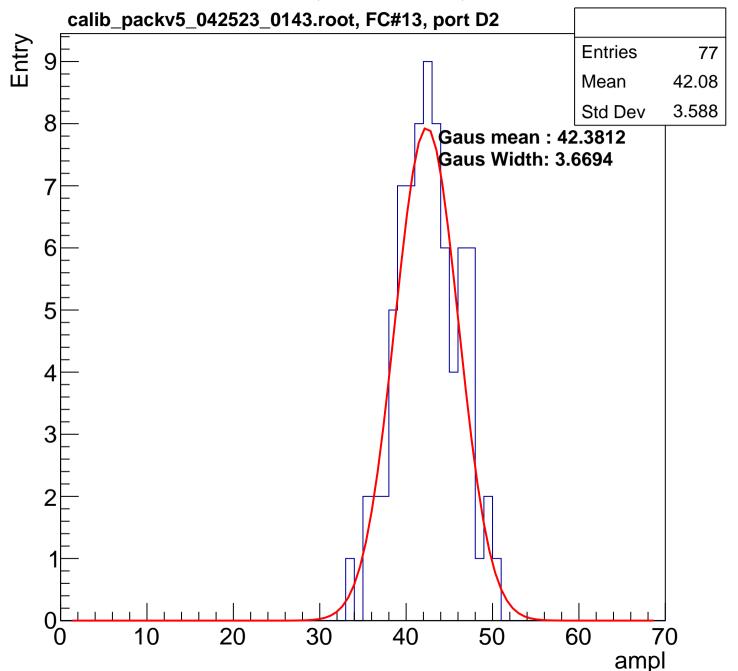


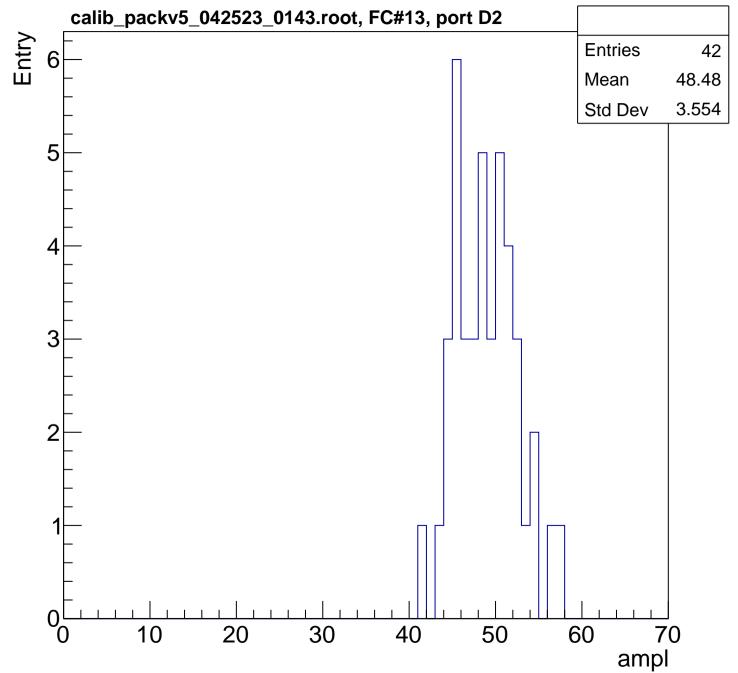


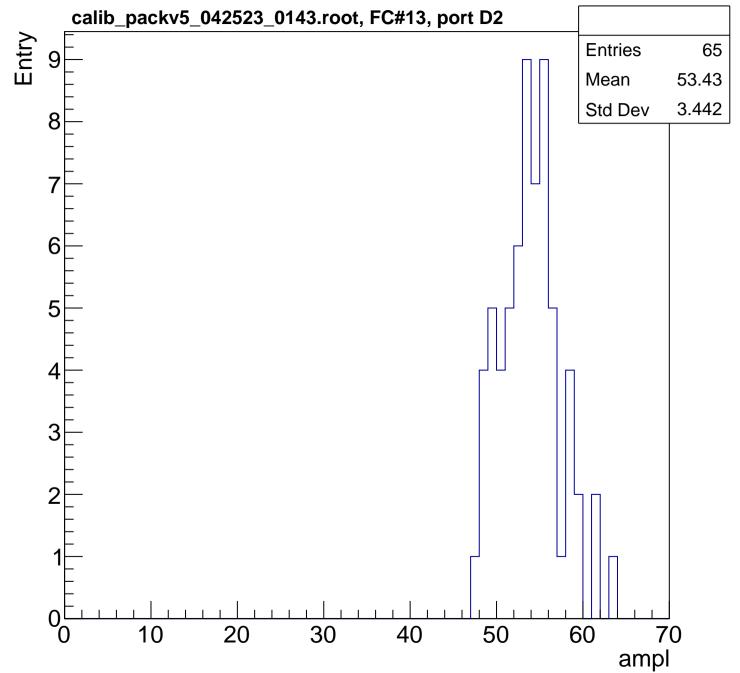
B1L003S, U4-ch91, adc7 calib_packv5_042523_0143.root, FC#13, port D2 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

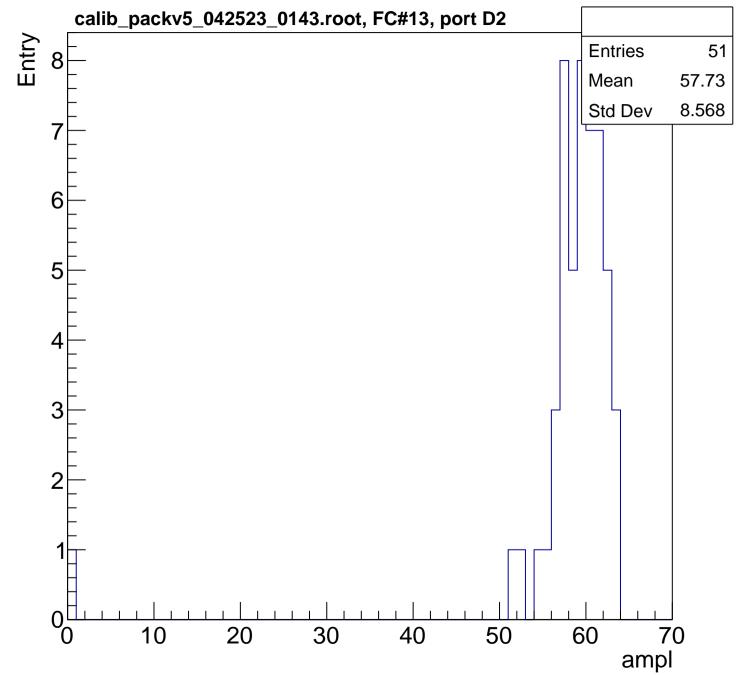


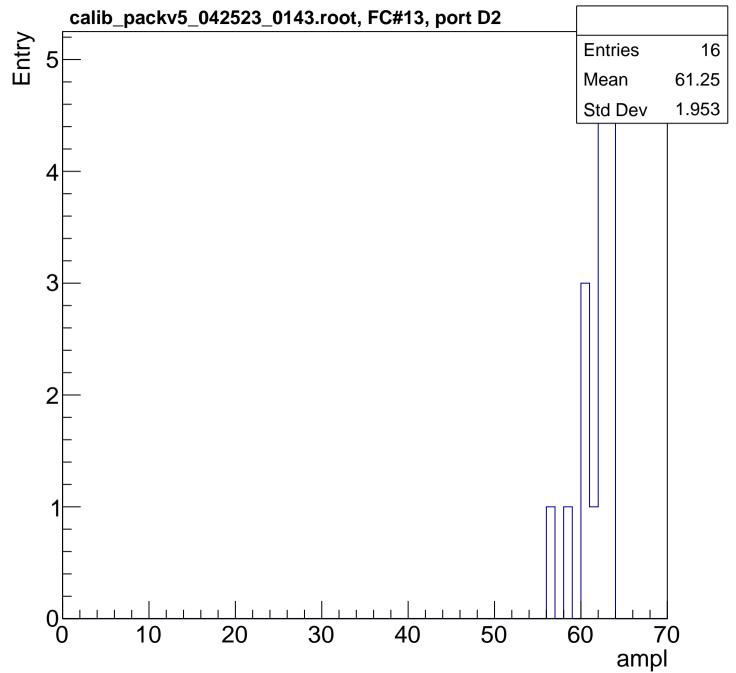


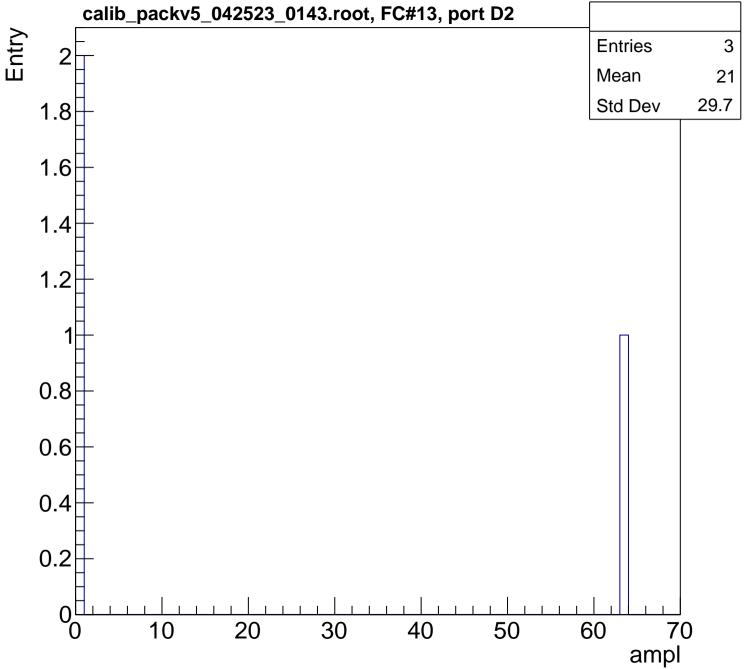


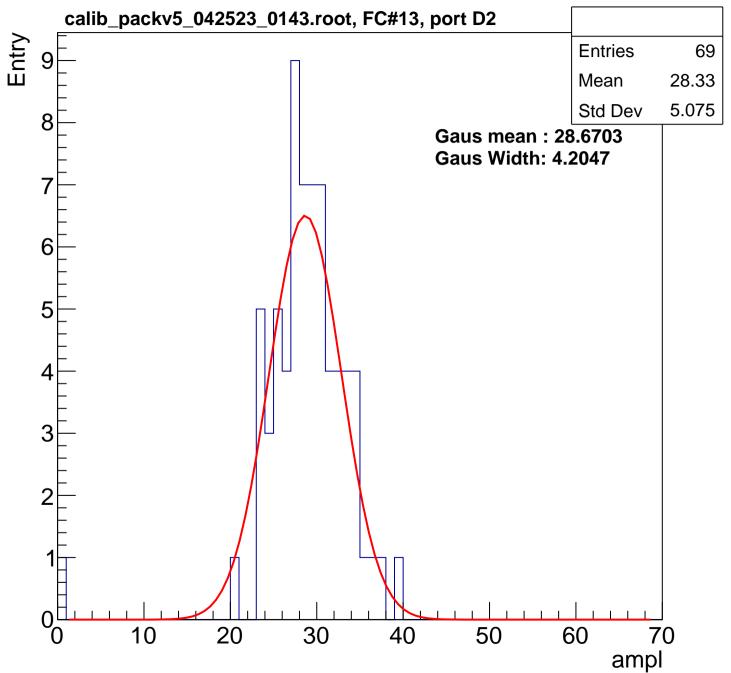


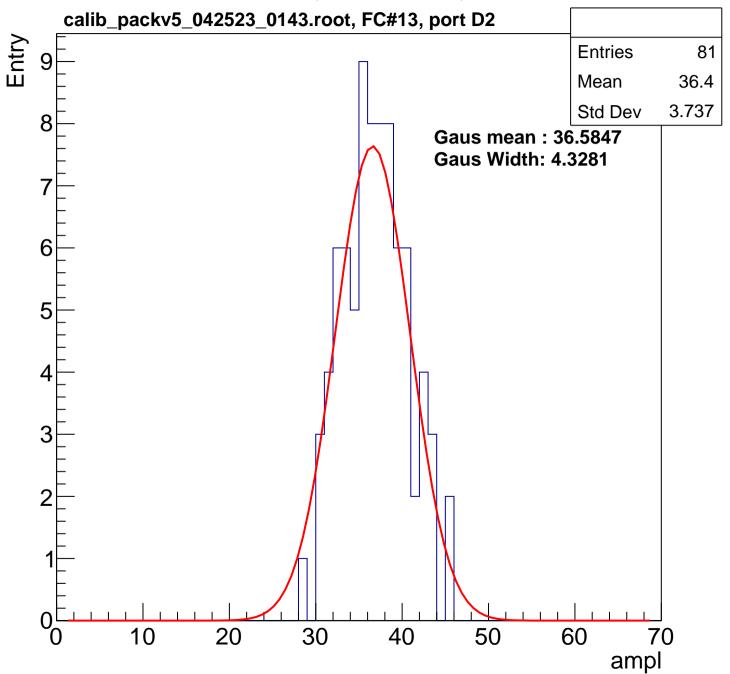


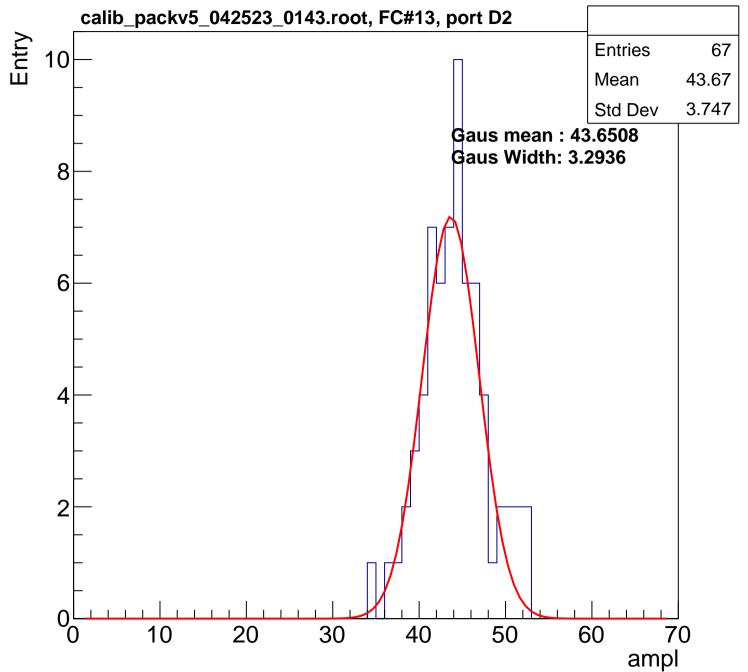


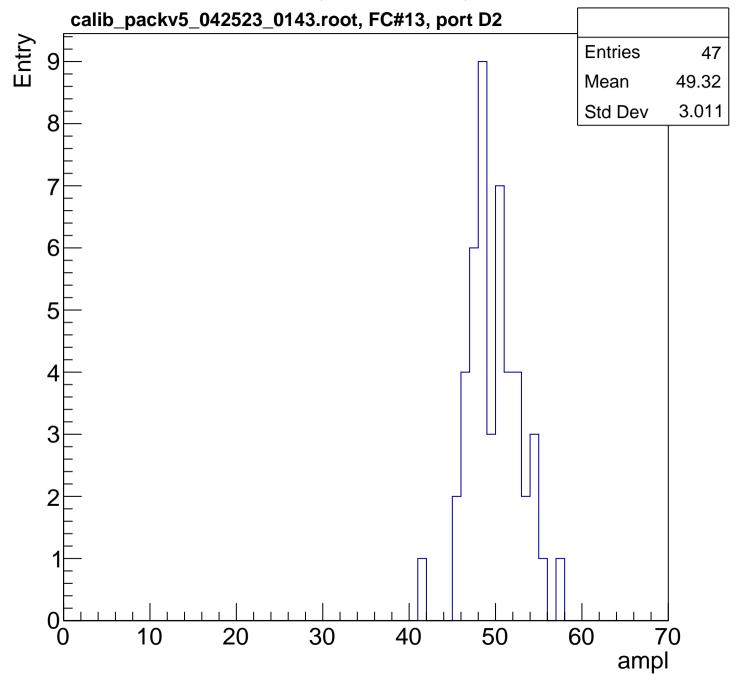


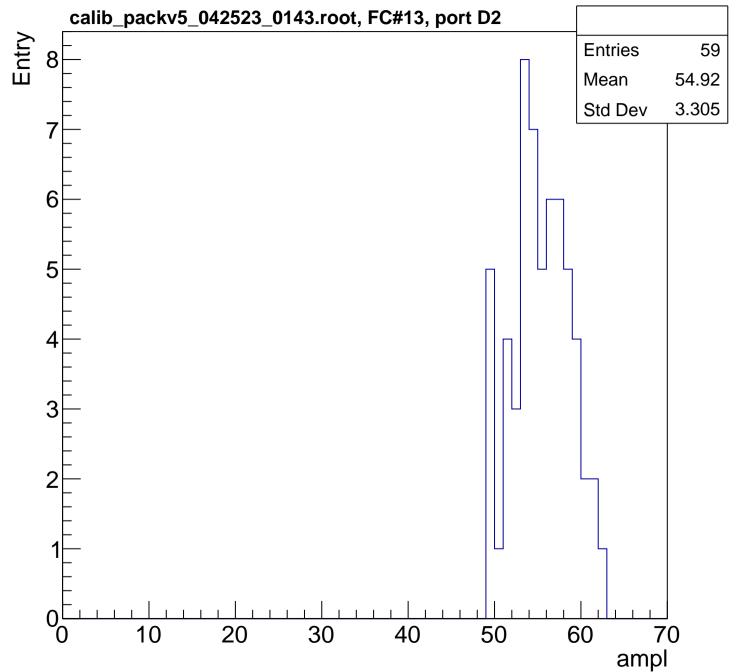


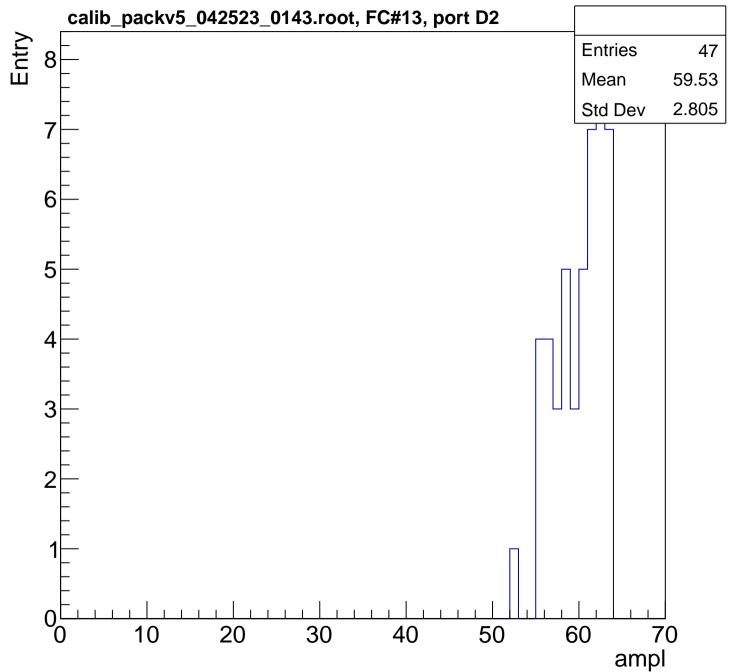


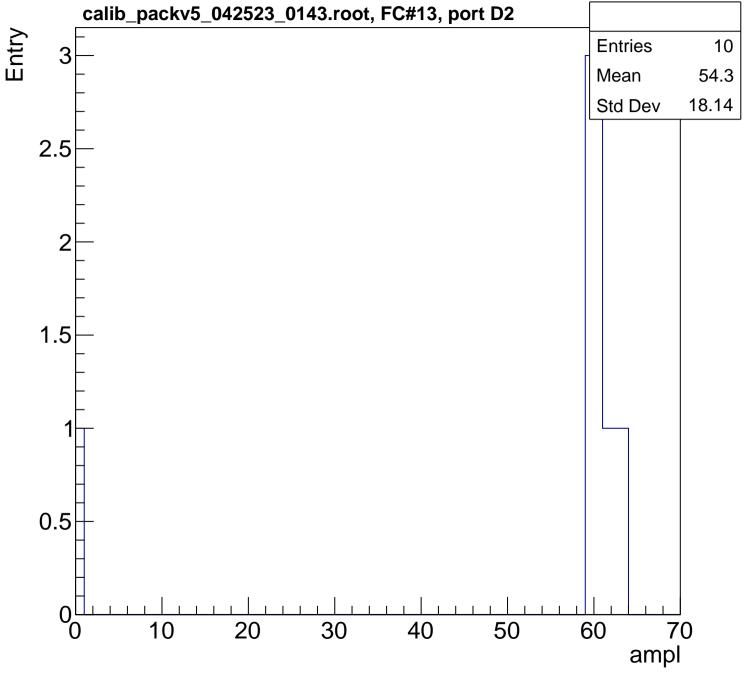


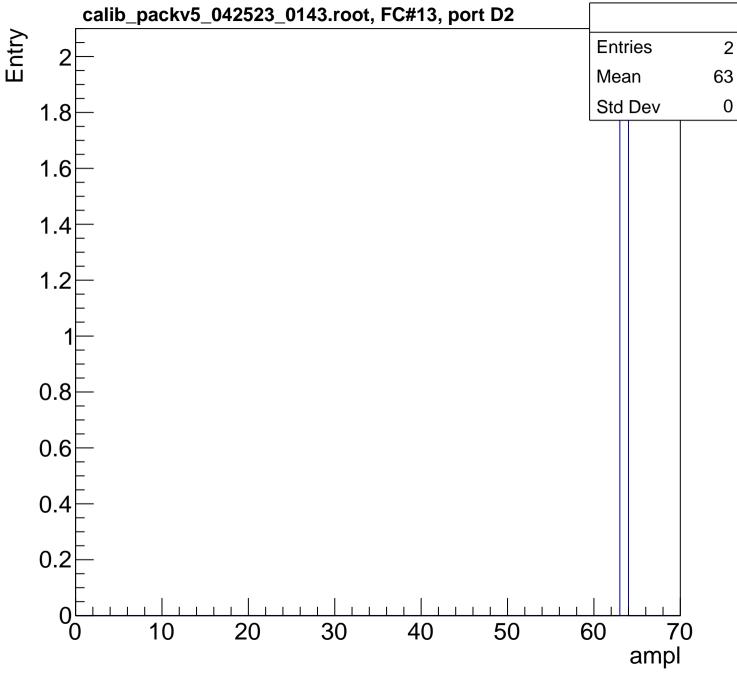


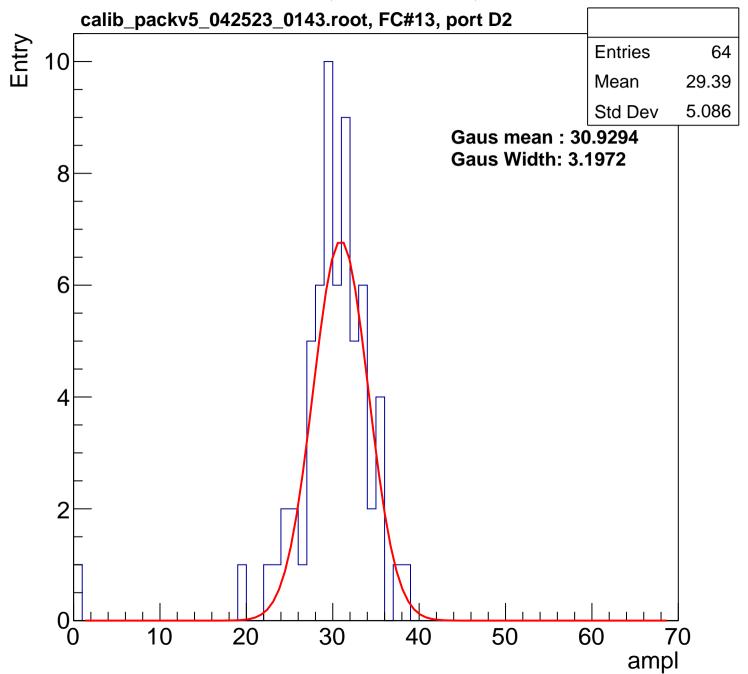


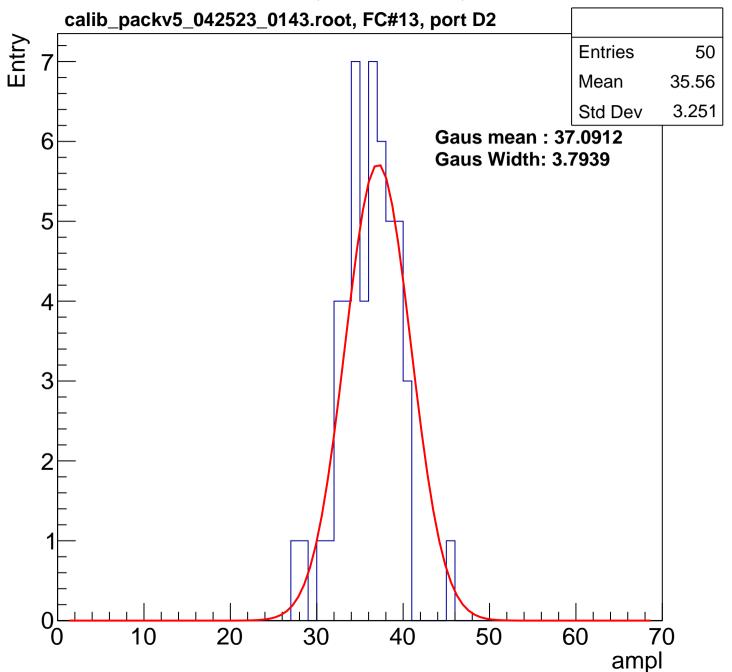


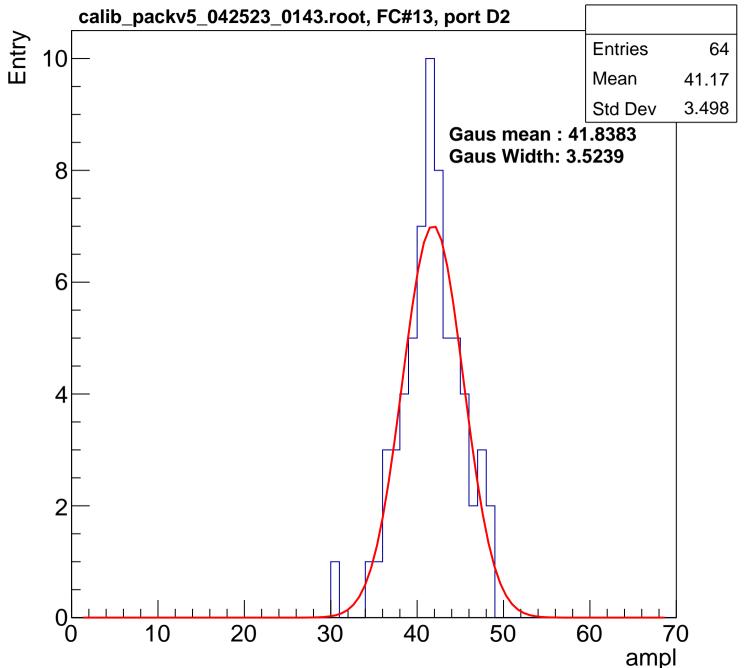


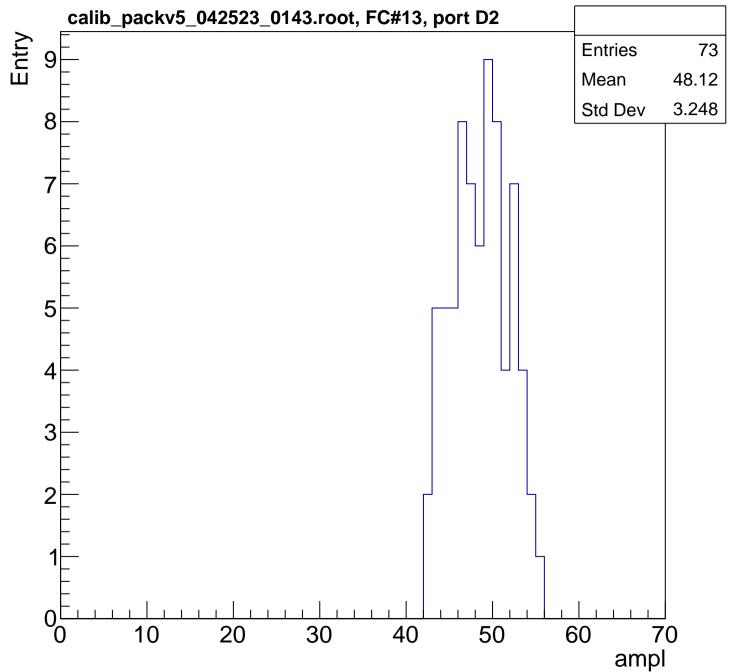


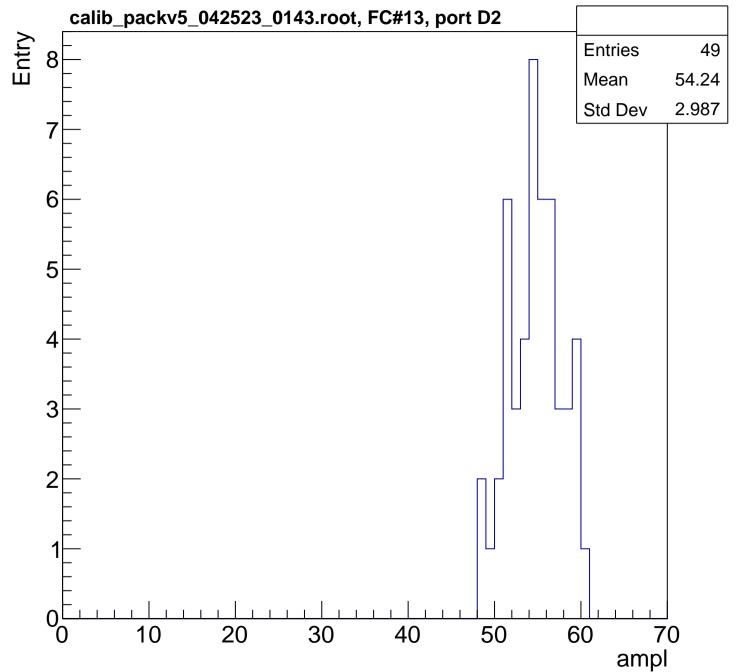


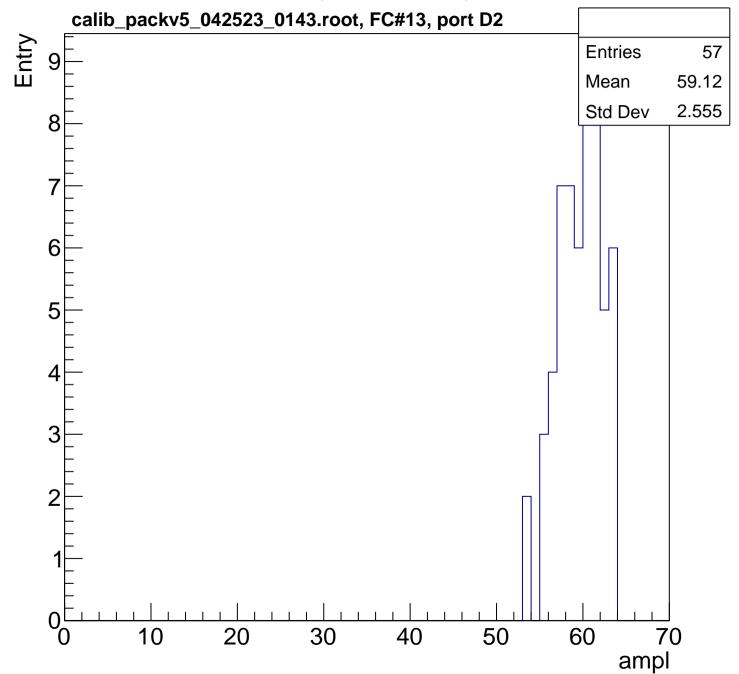


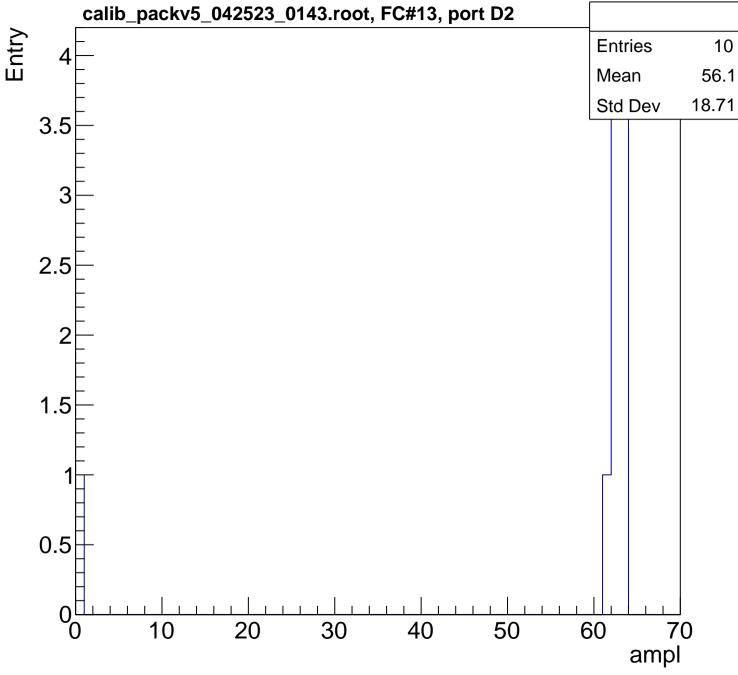


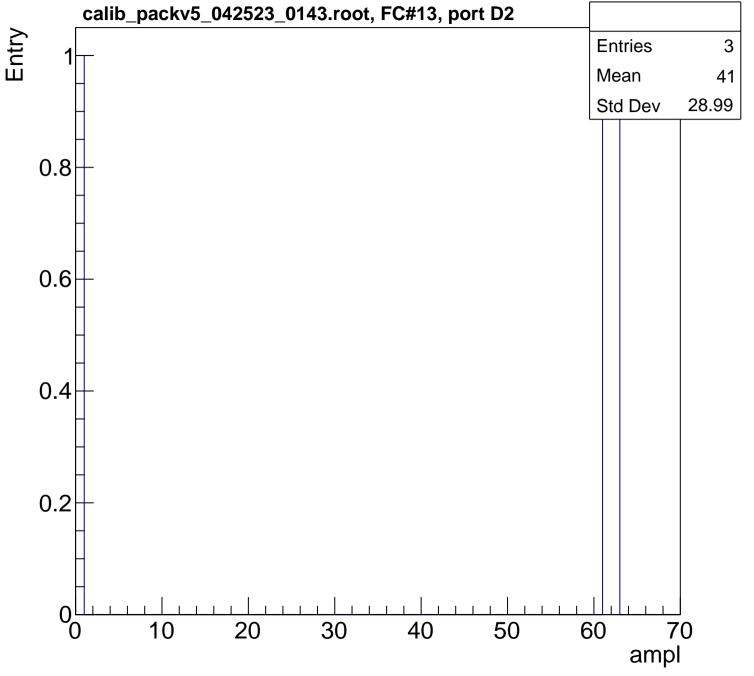


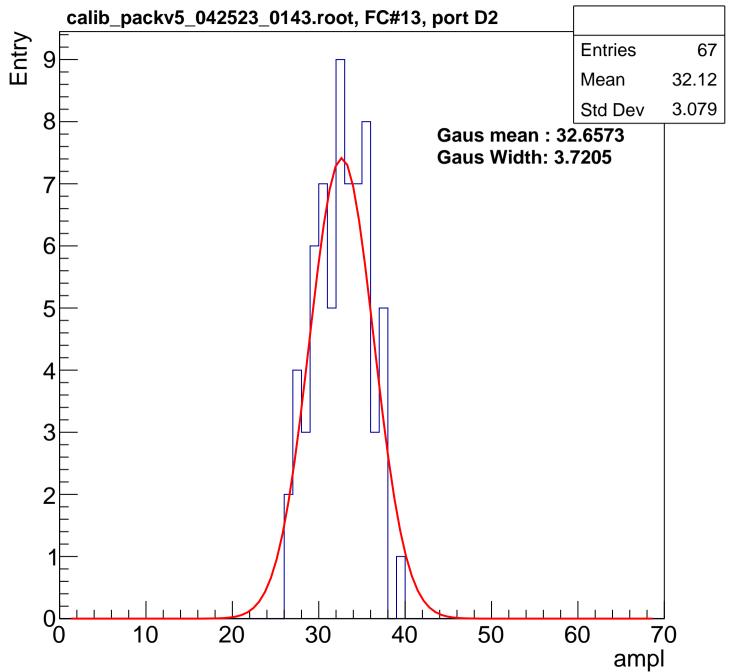


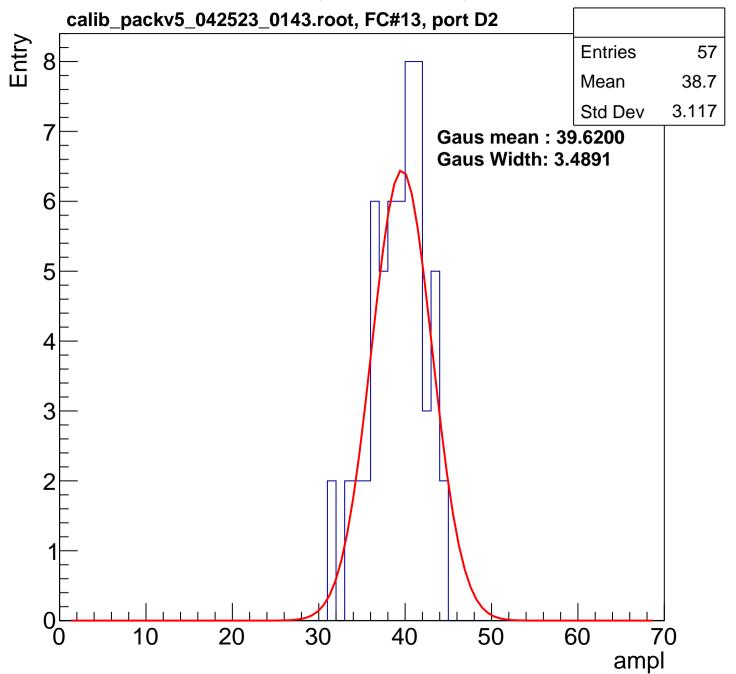


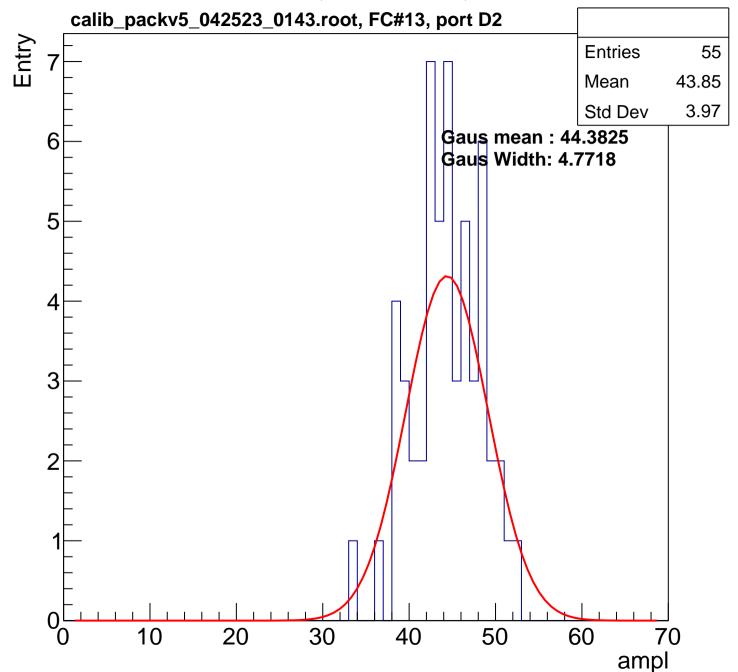


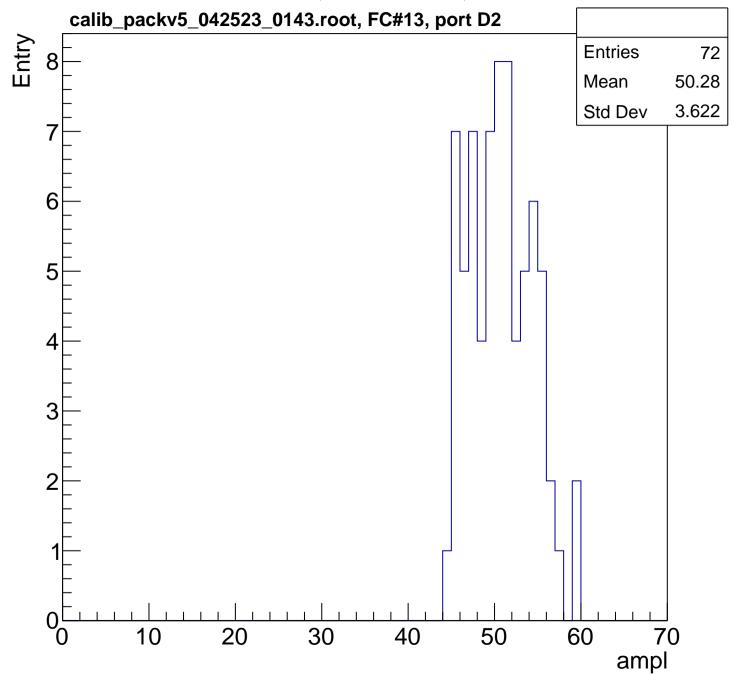


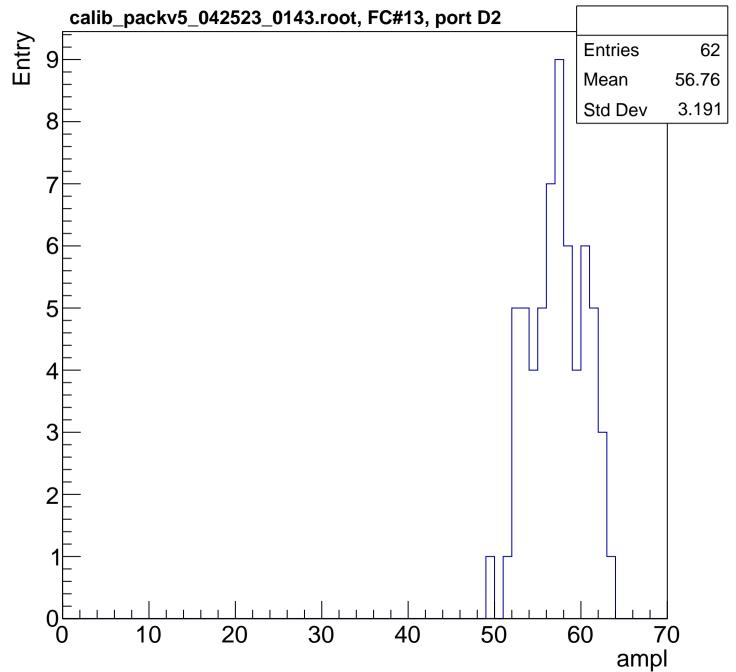


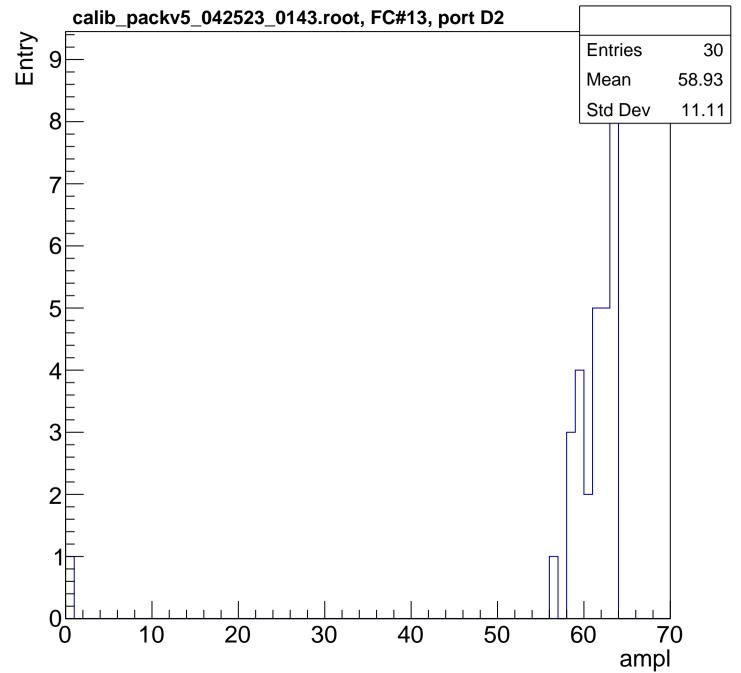


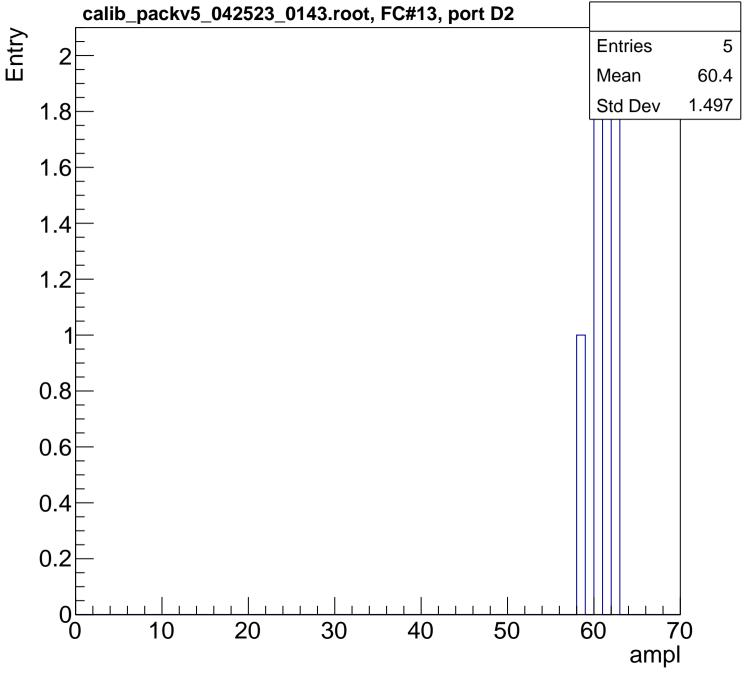




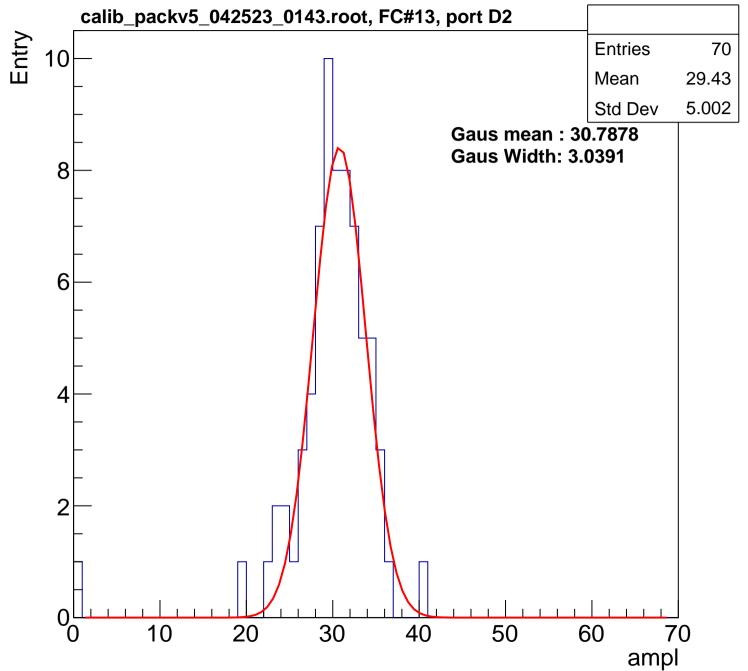


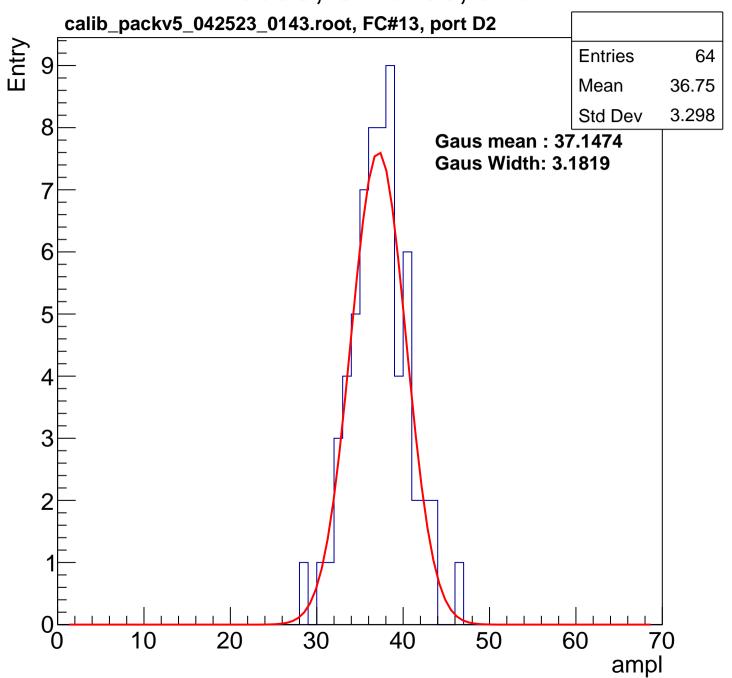


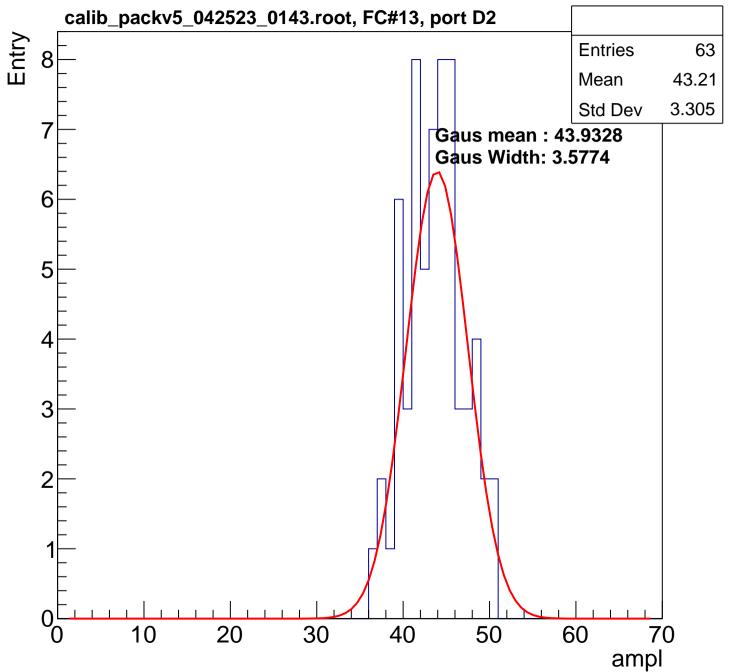


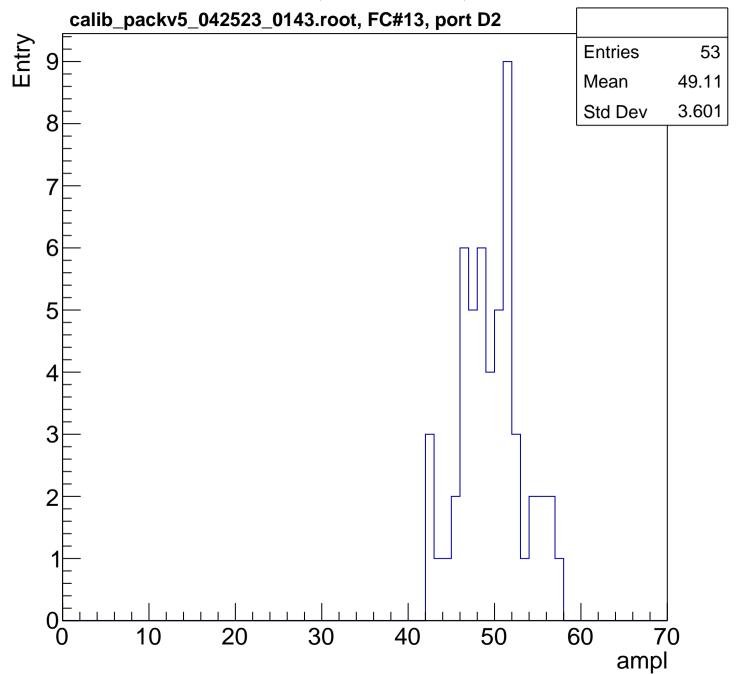


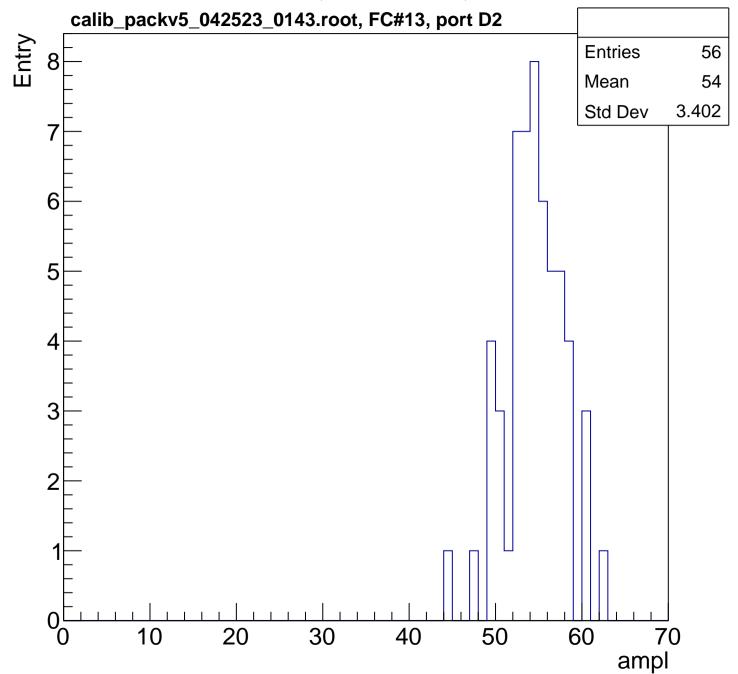
B1L003S, U4-ch95, adc7 calib_packv5_042523_0143.root, FC#13, port D2 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

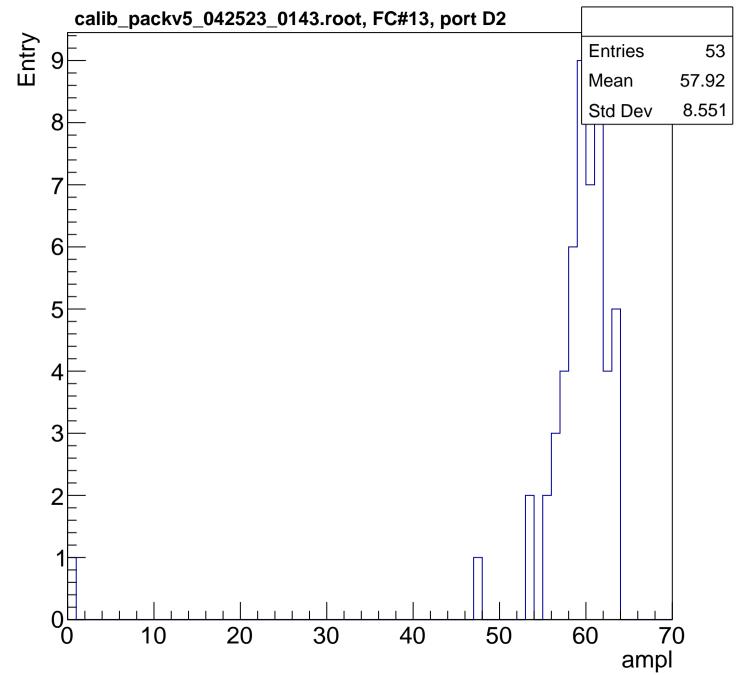


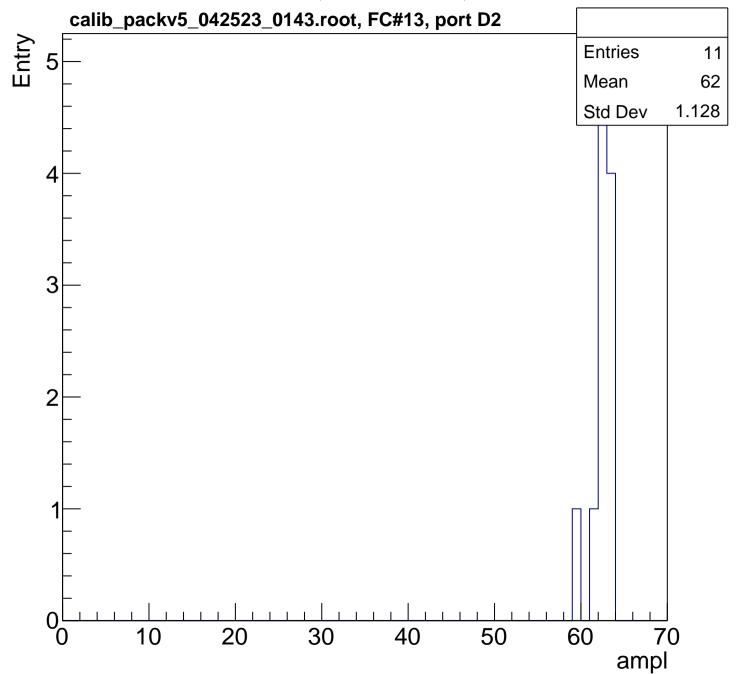


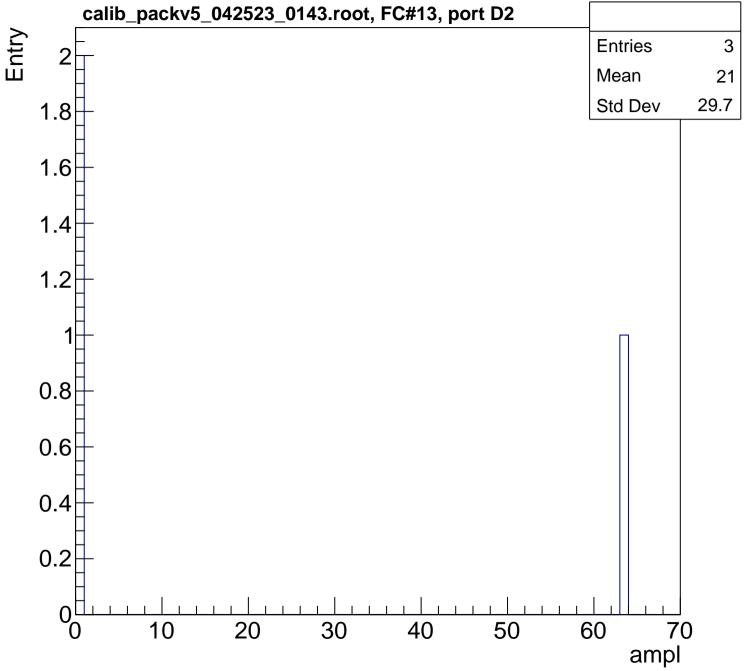


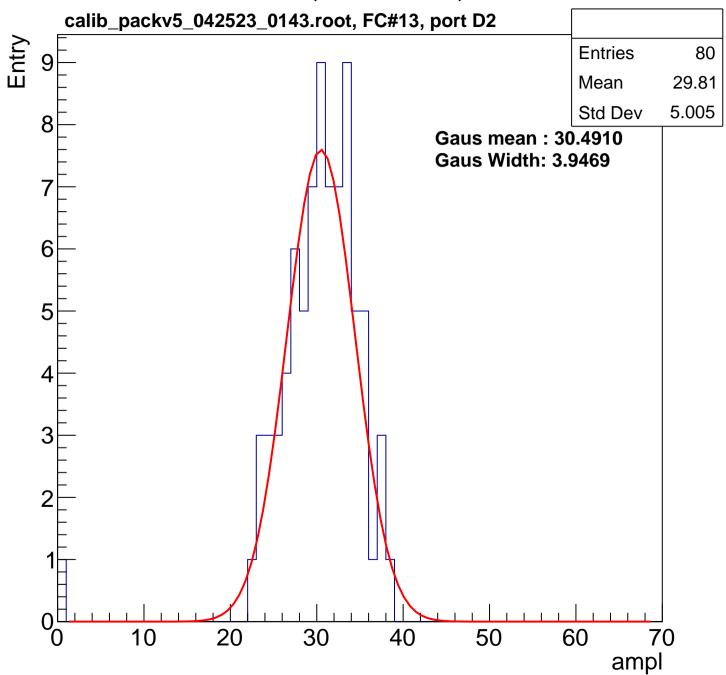


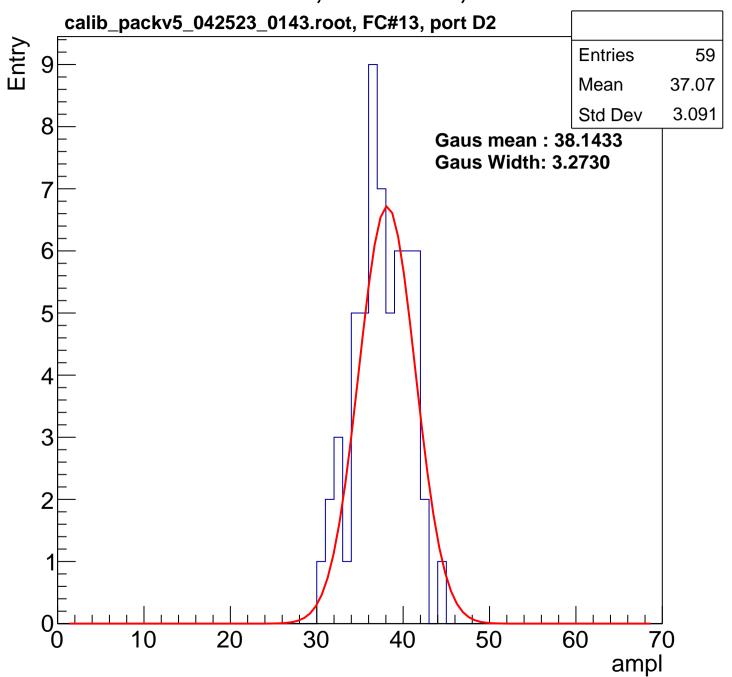


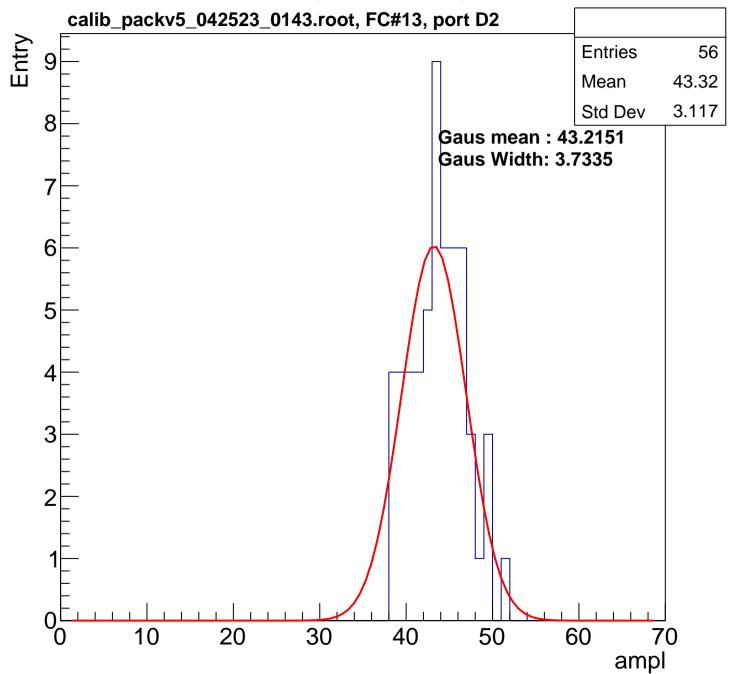


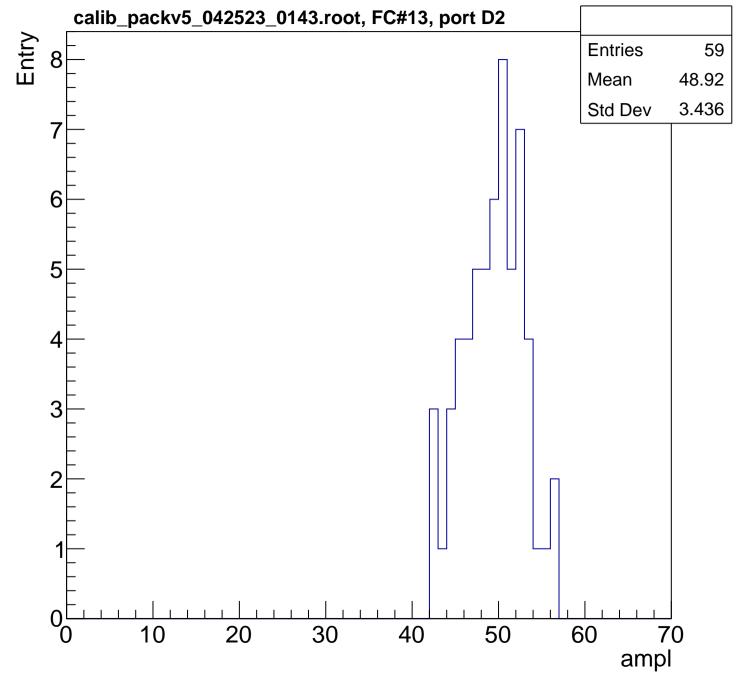


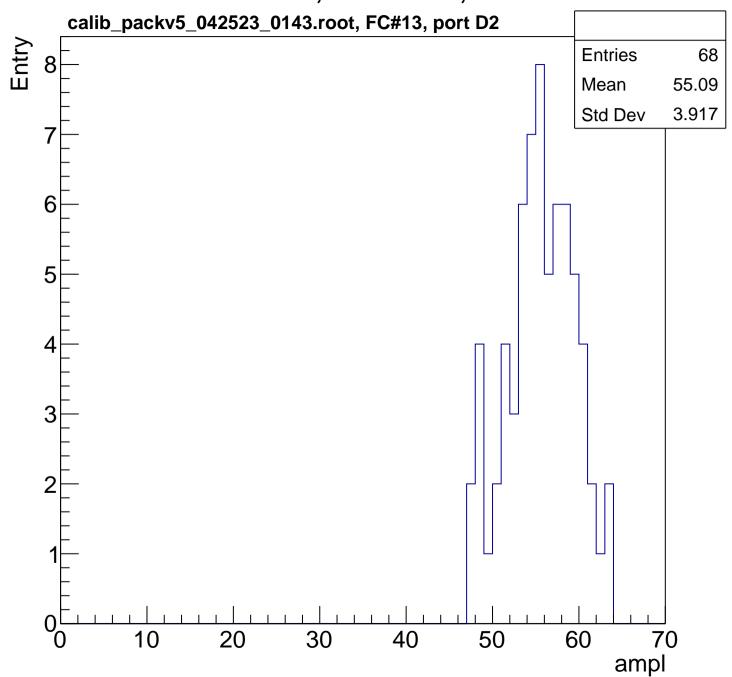


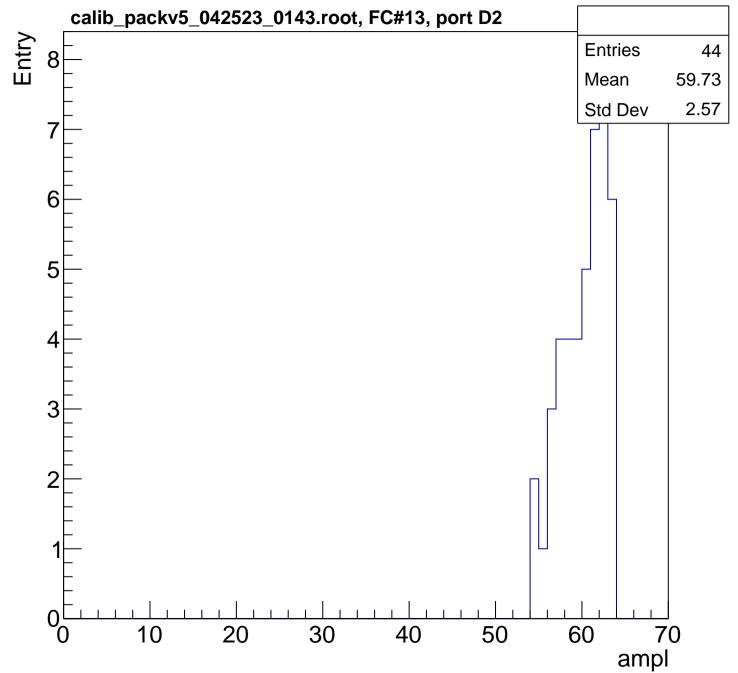


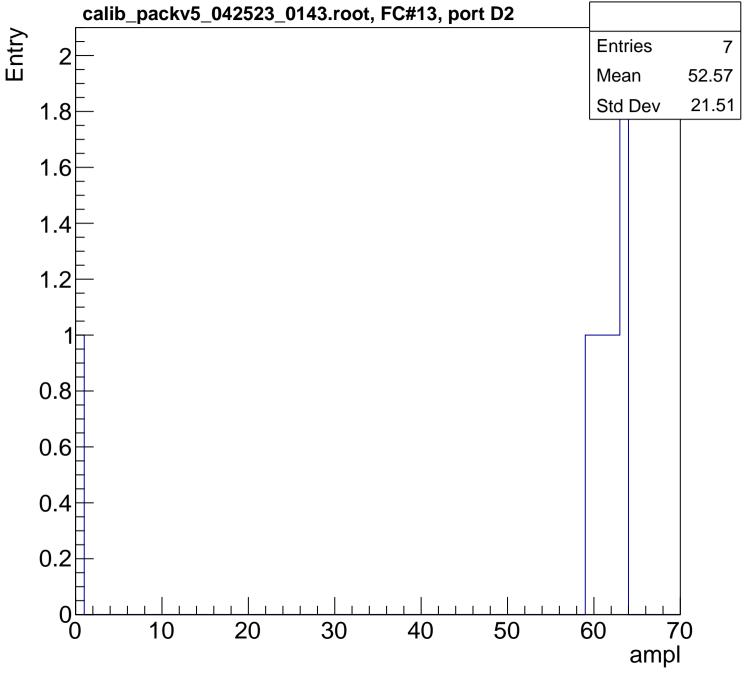




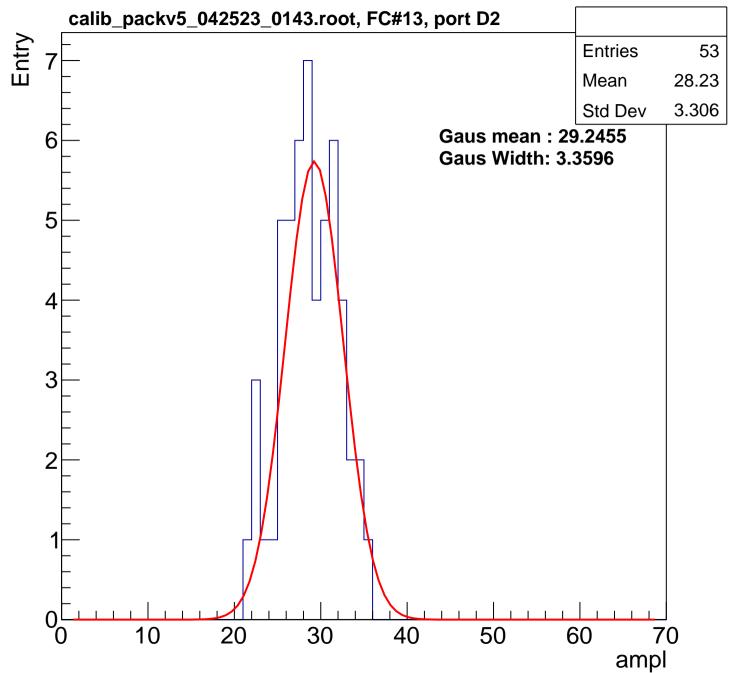


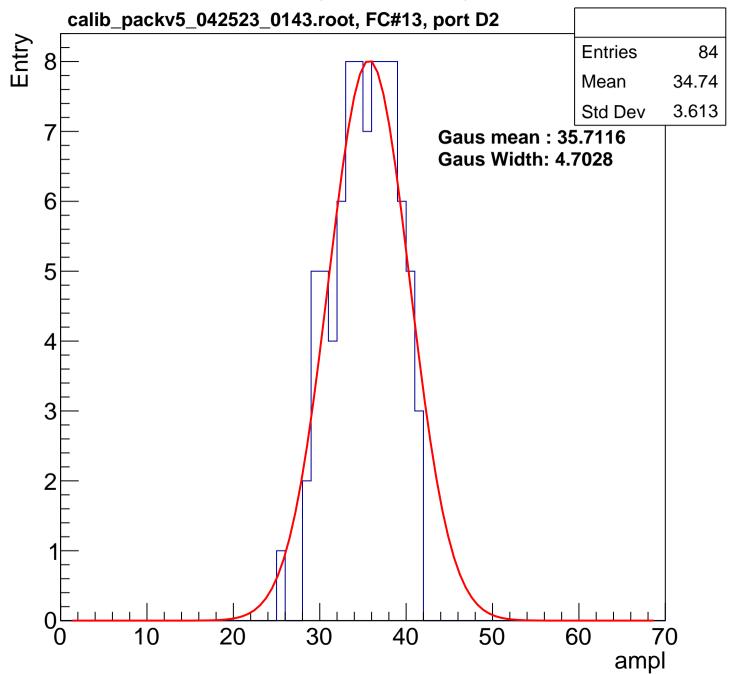


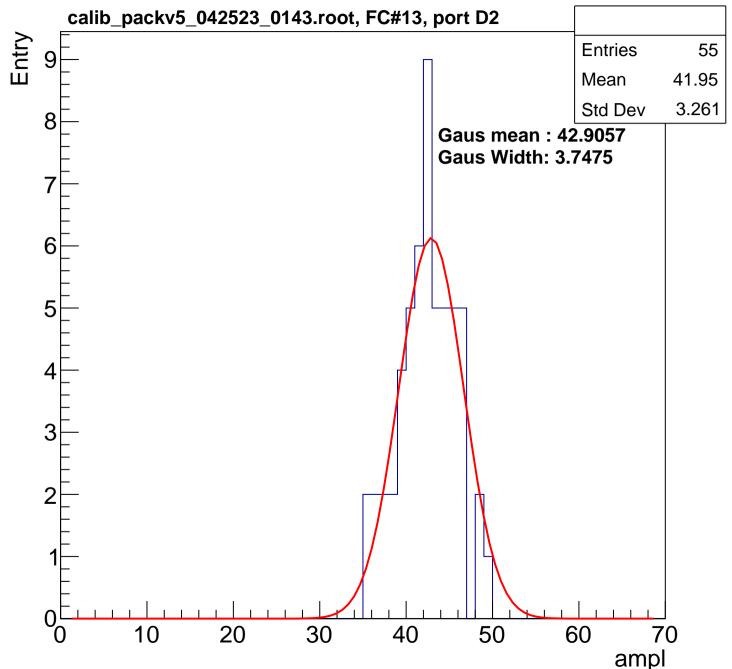


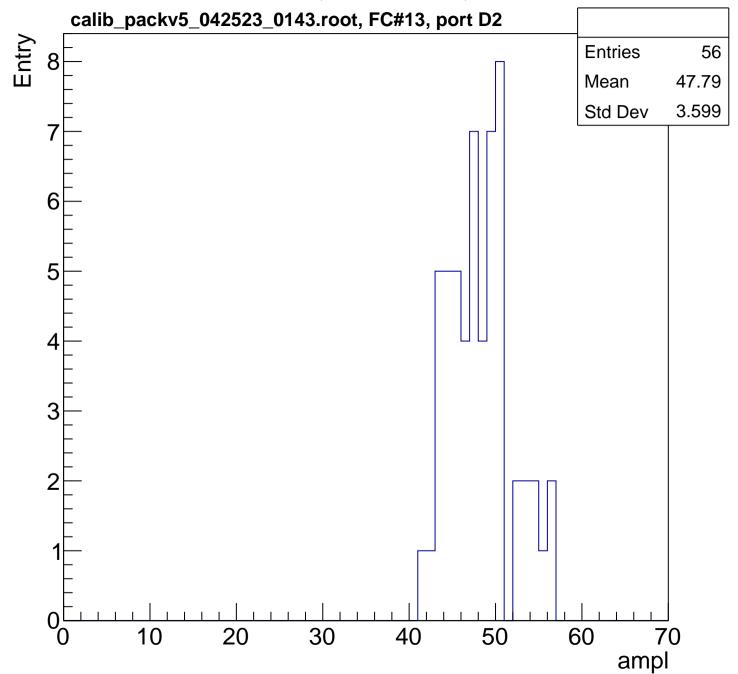


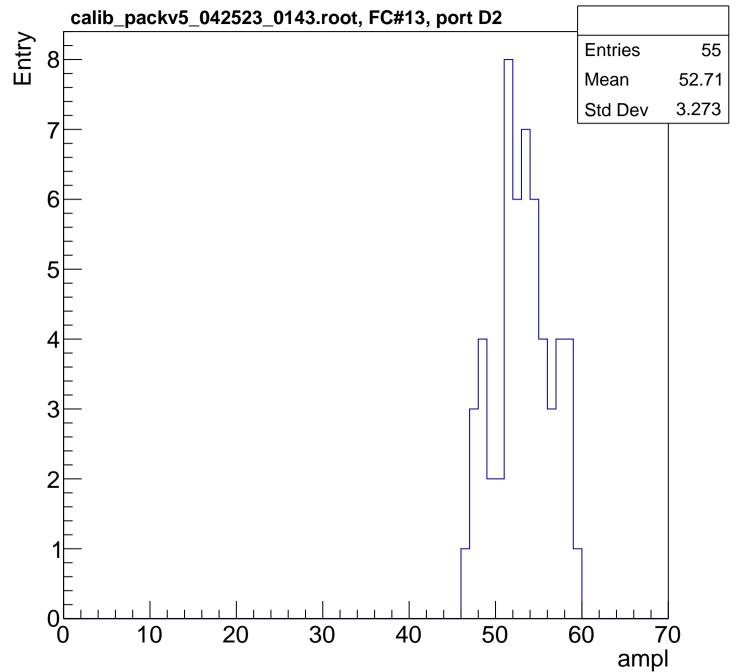


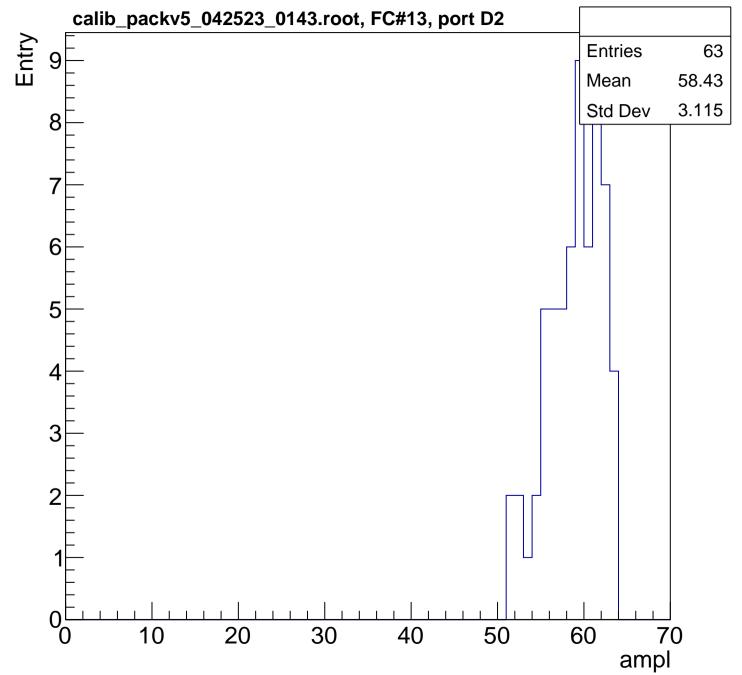


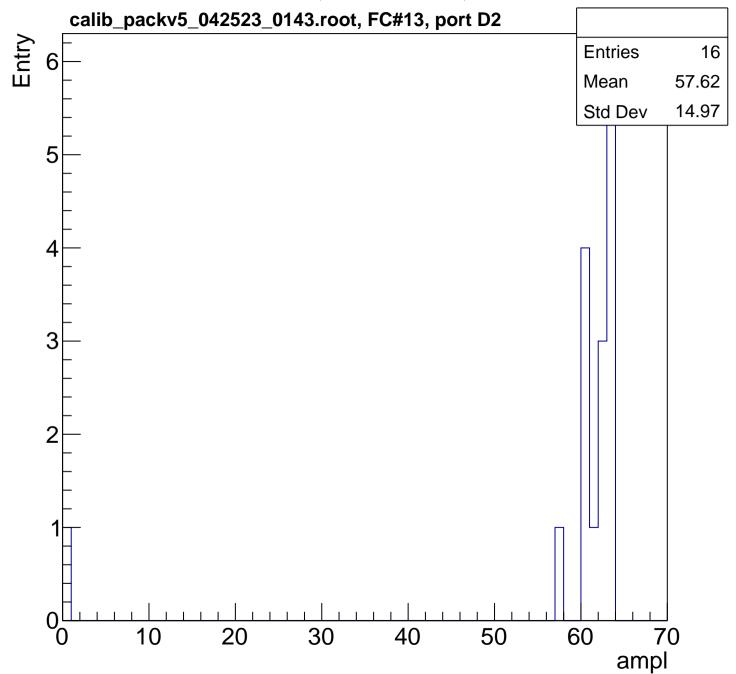


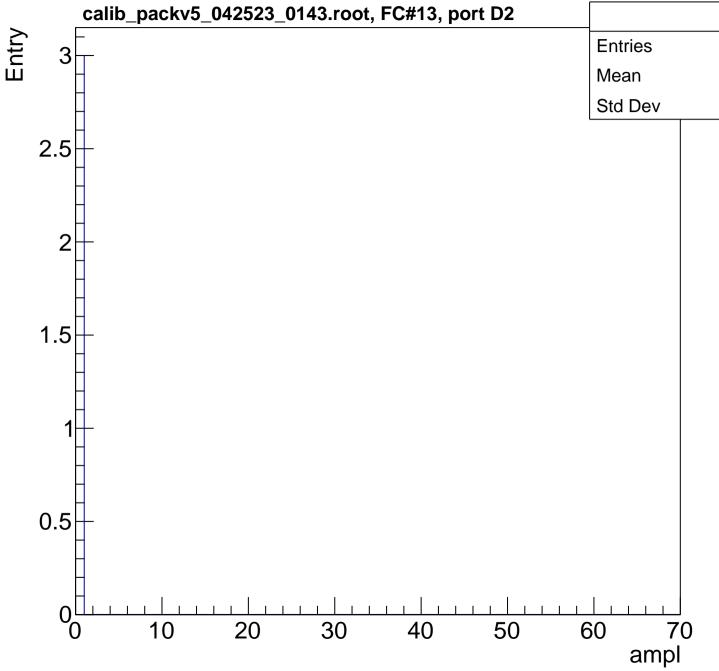


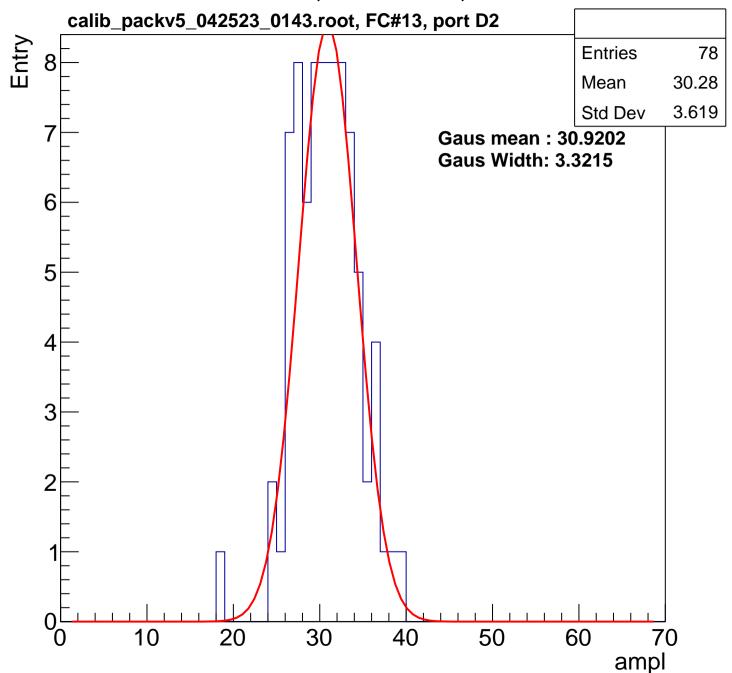


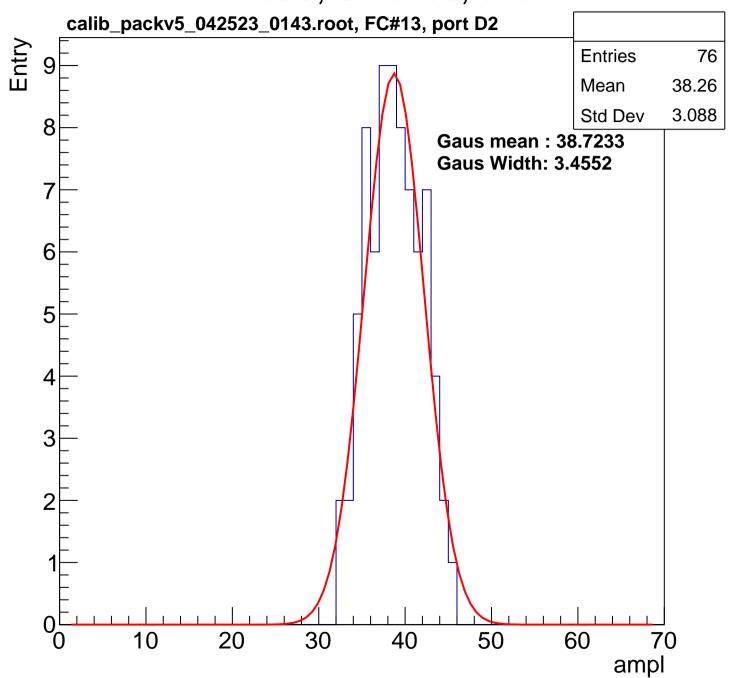


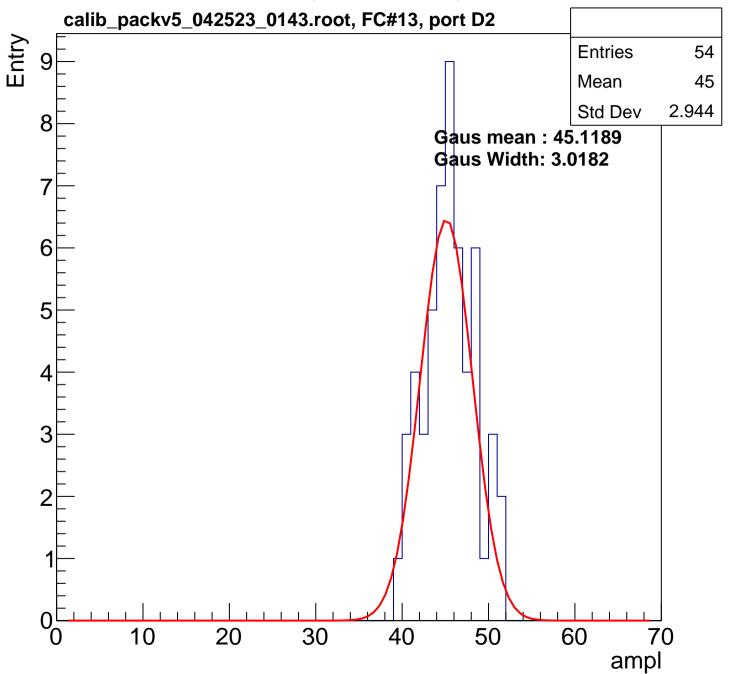


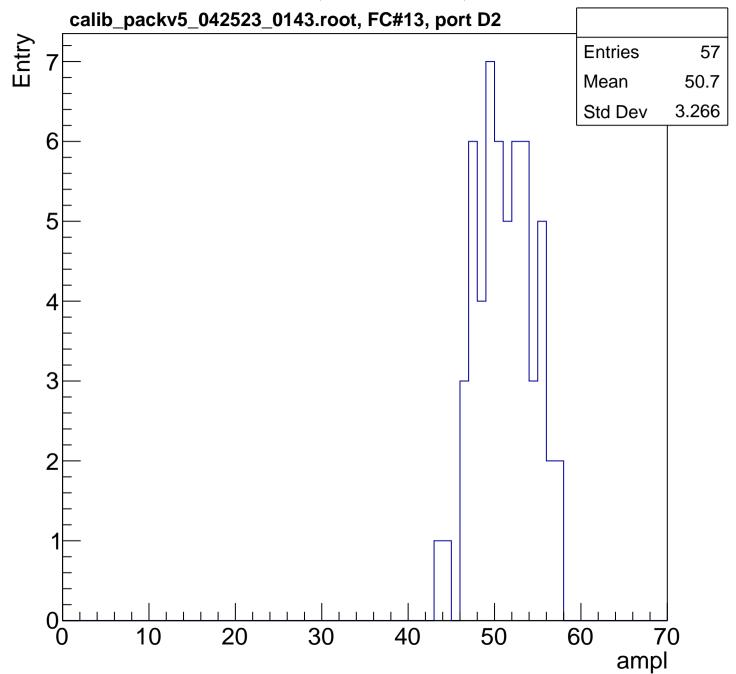


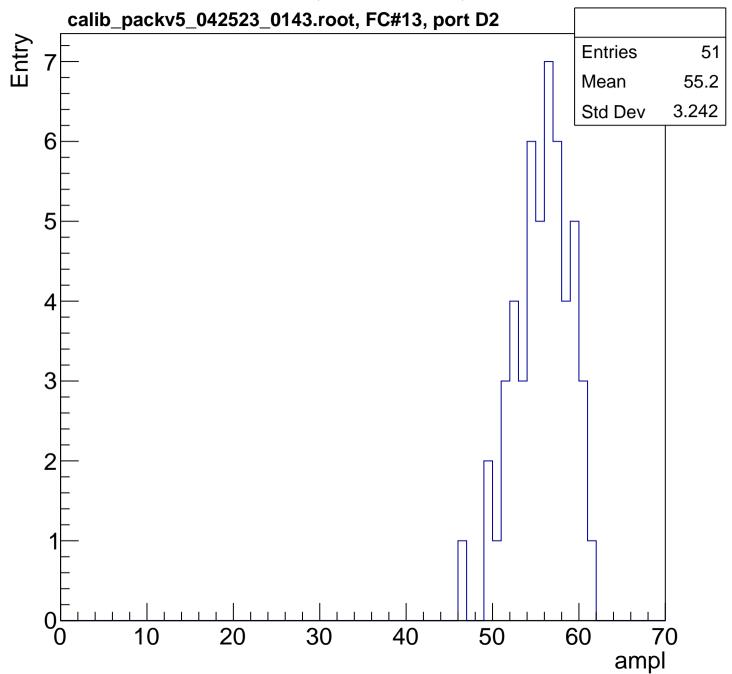


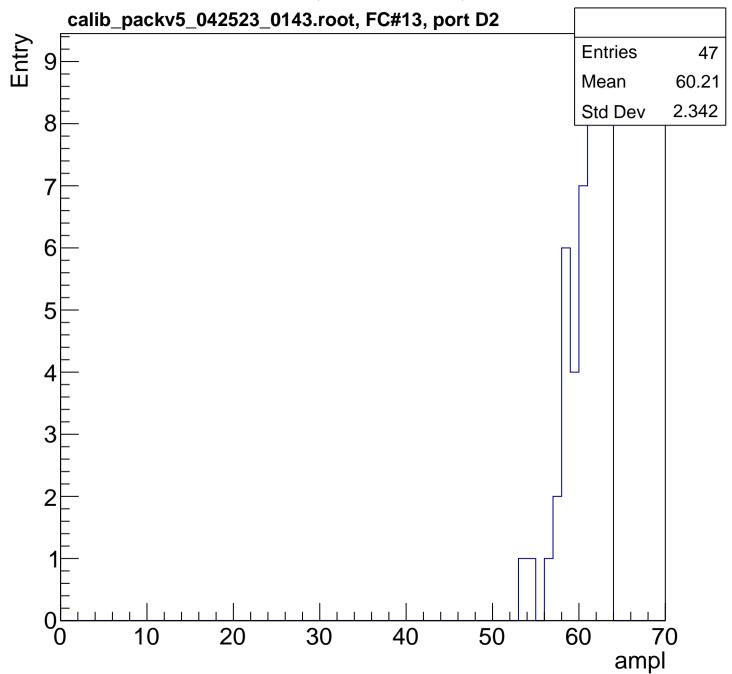


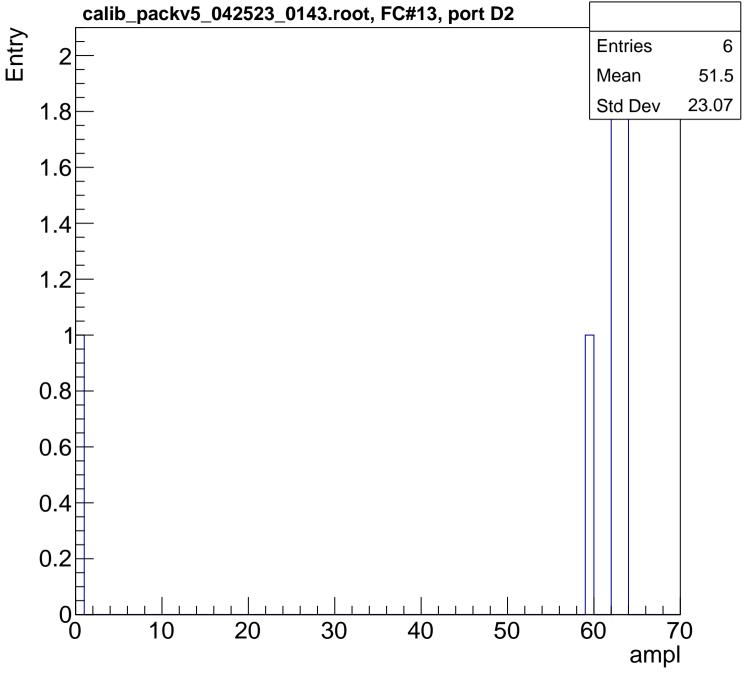


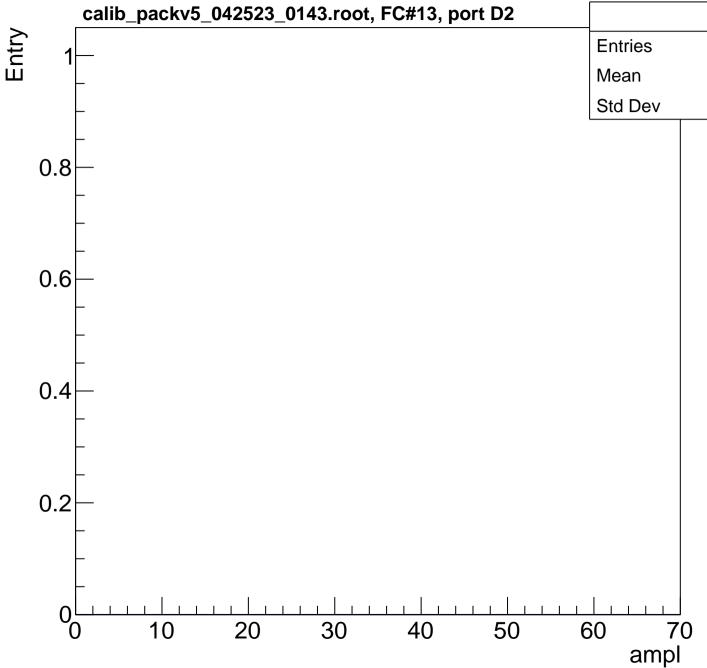


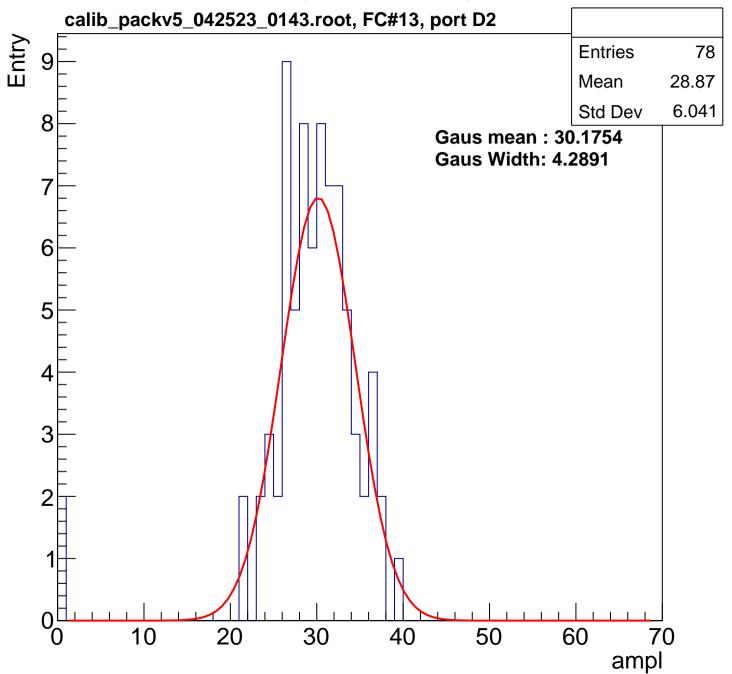


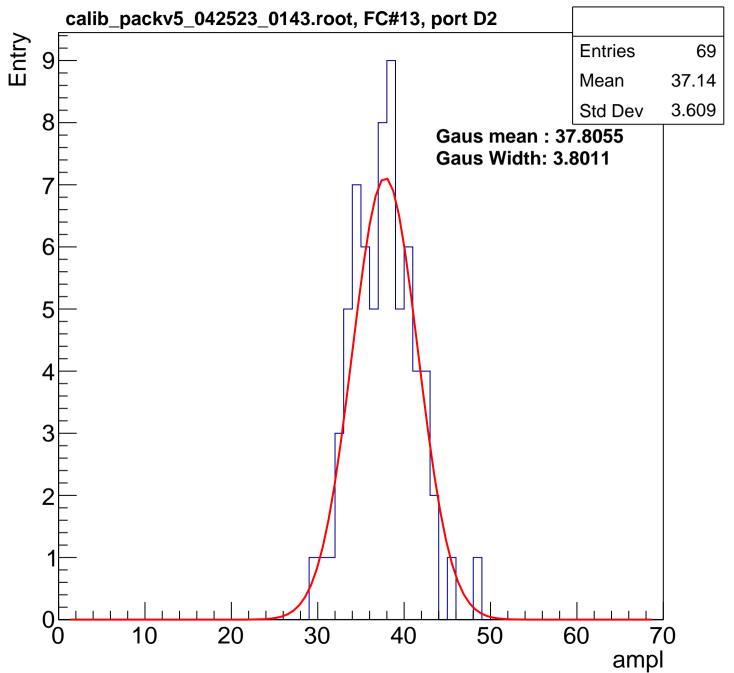


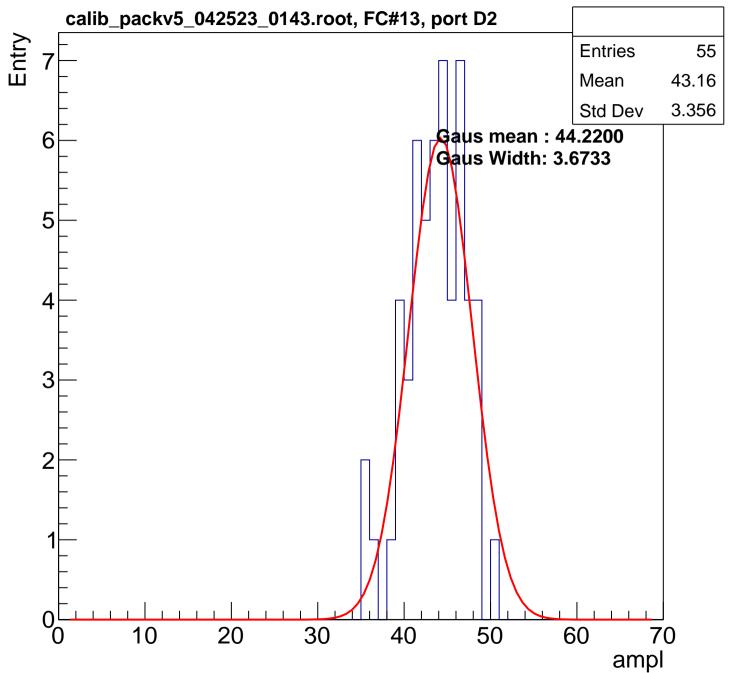


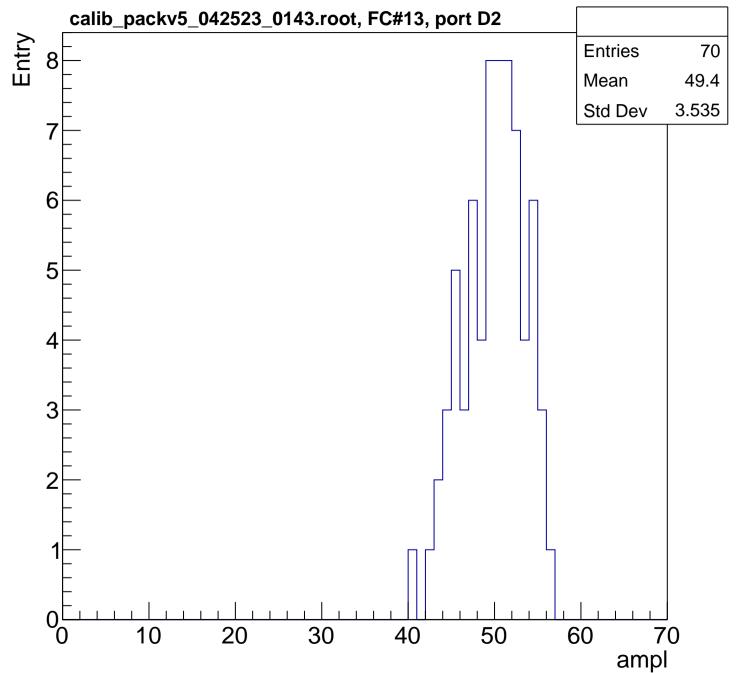


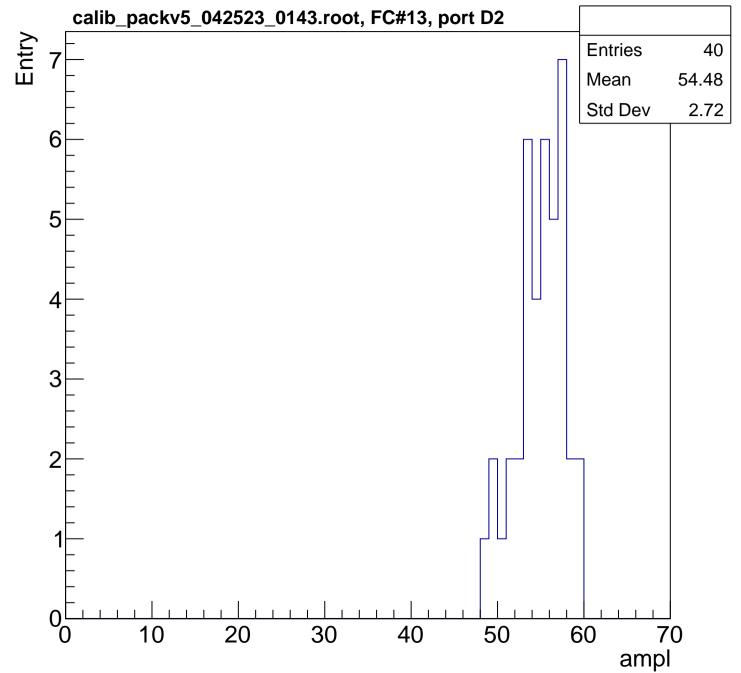


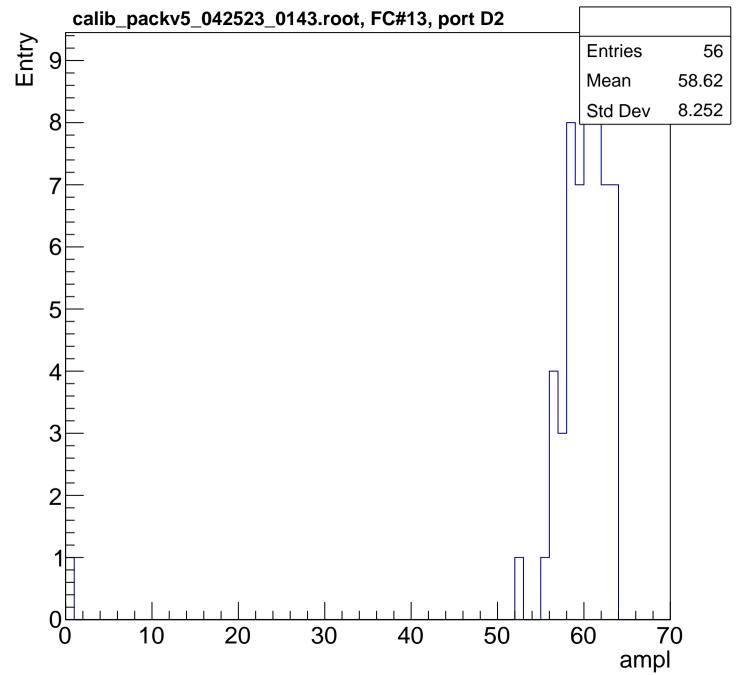


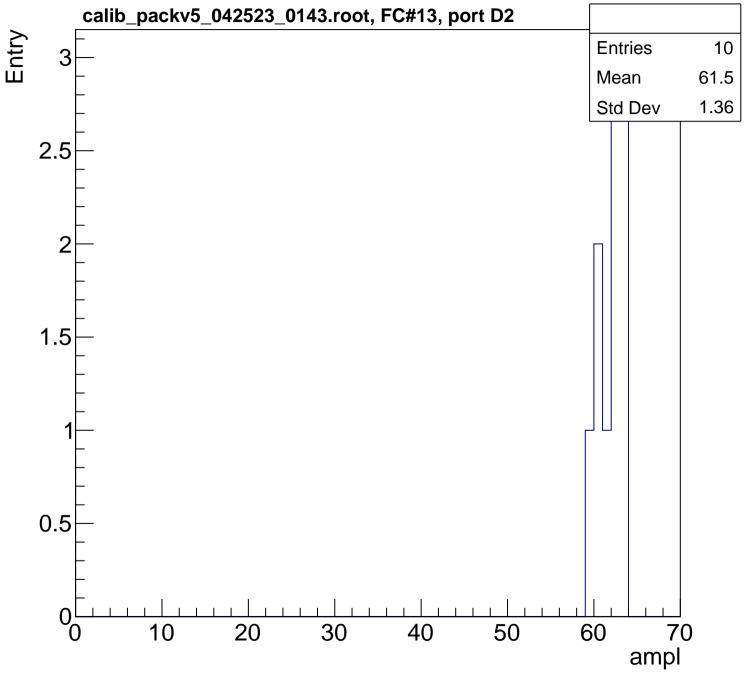


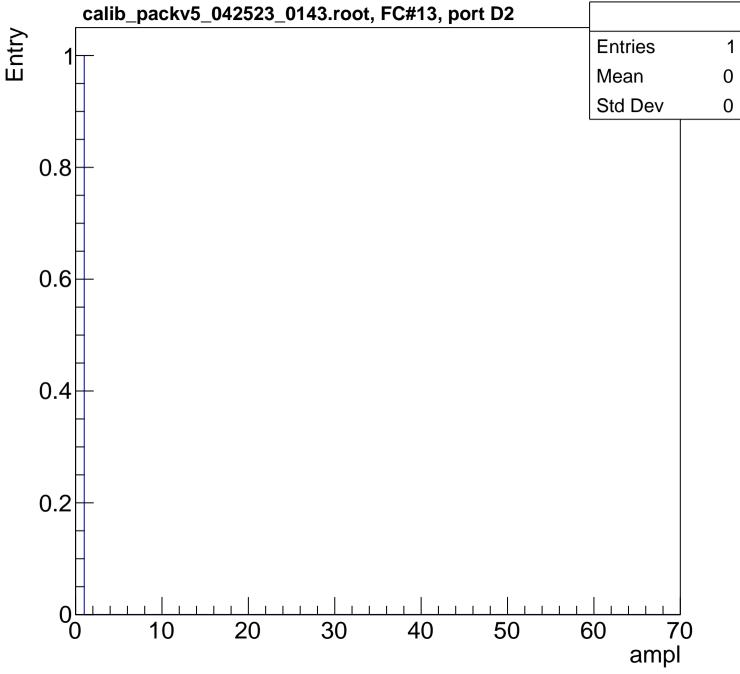


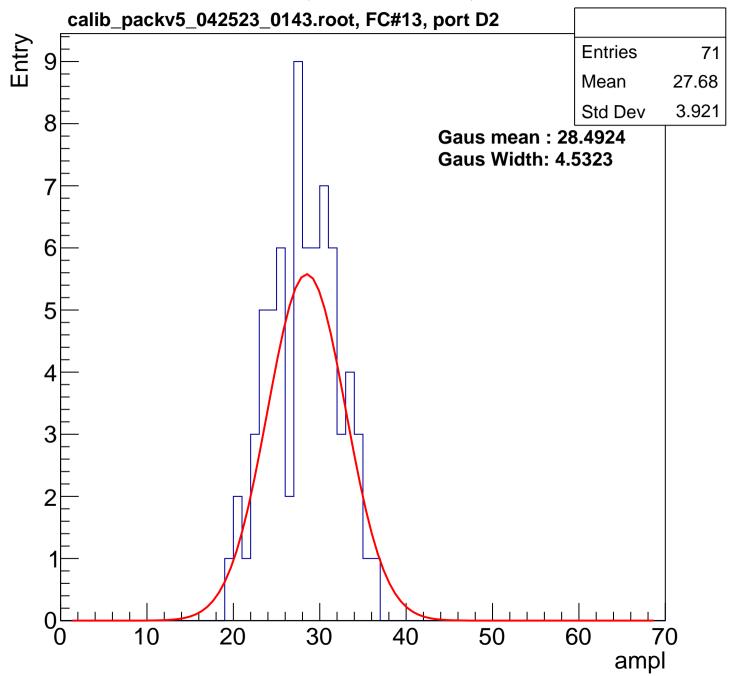


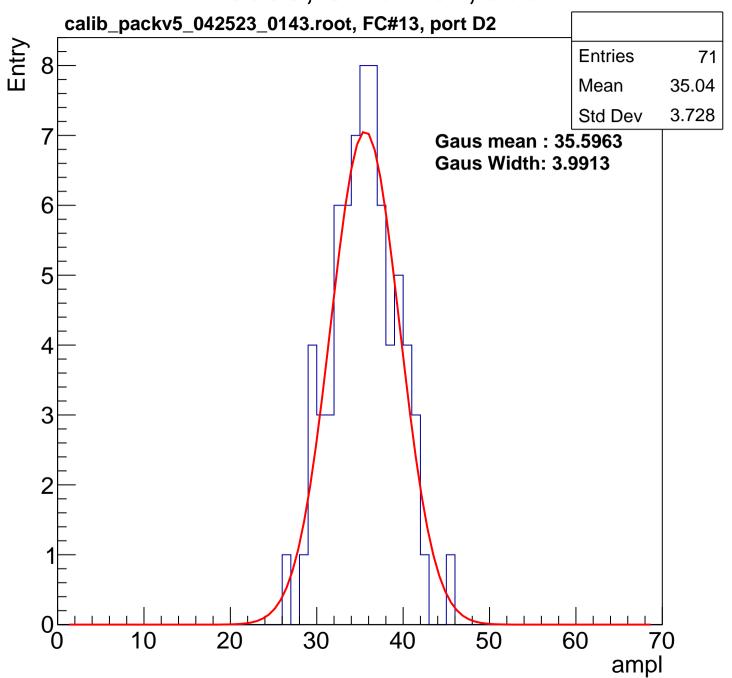


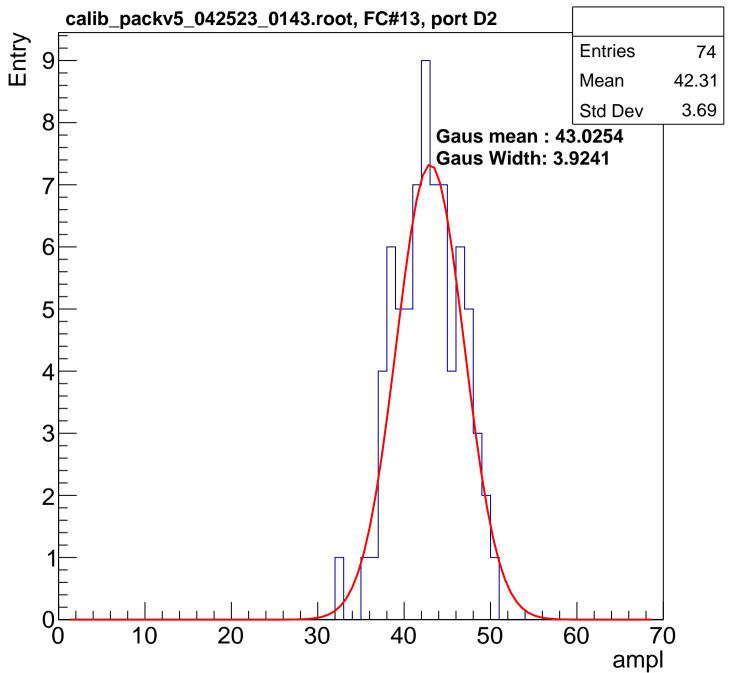


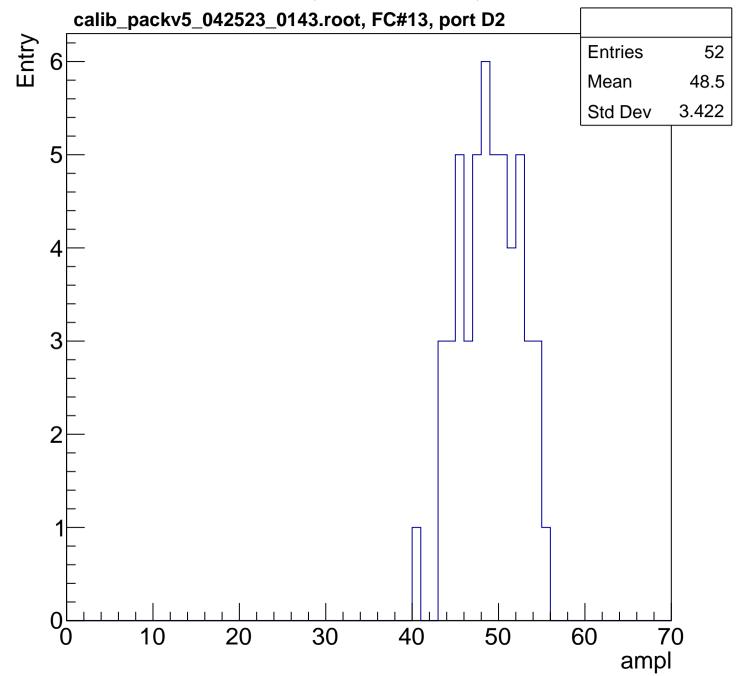


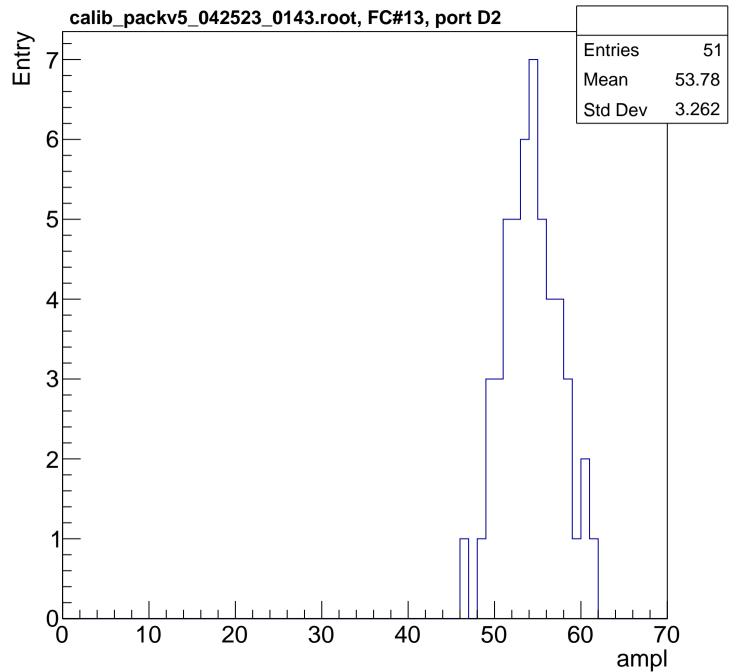


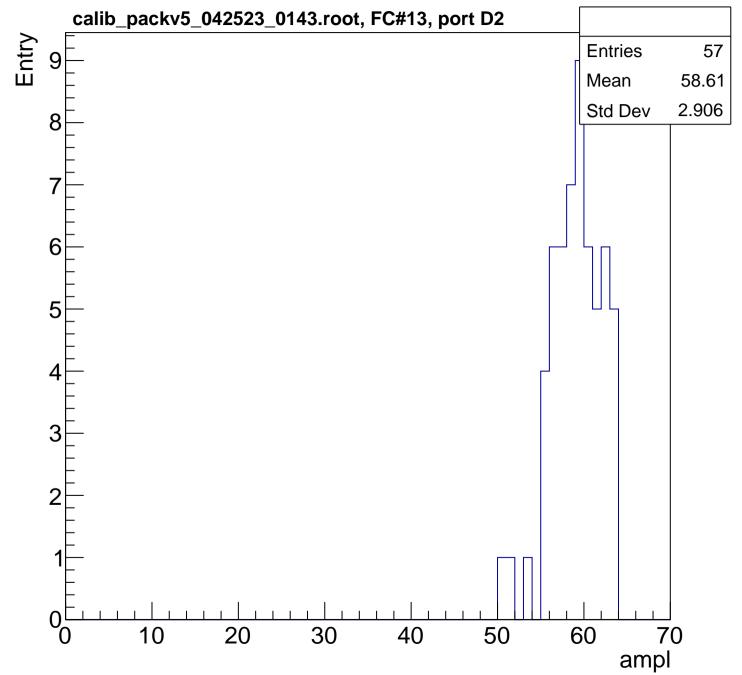


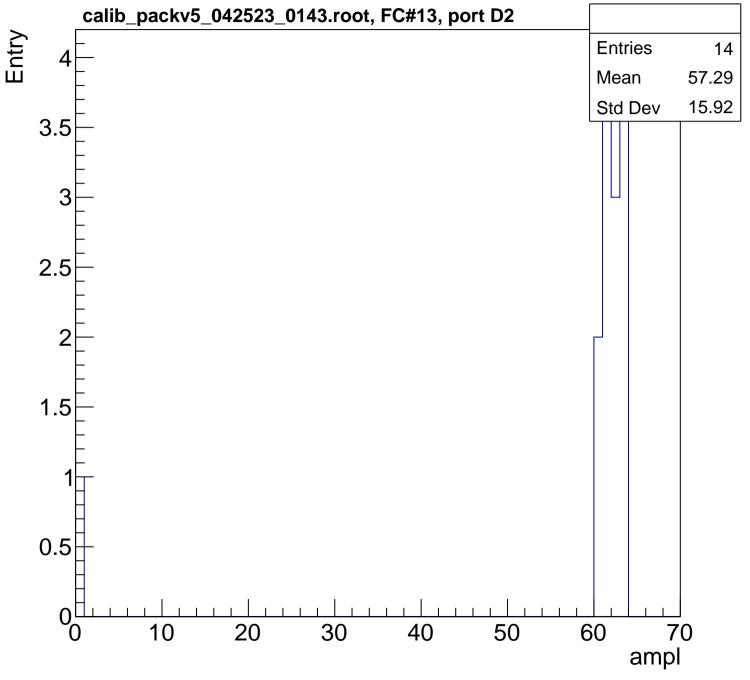


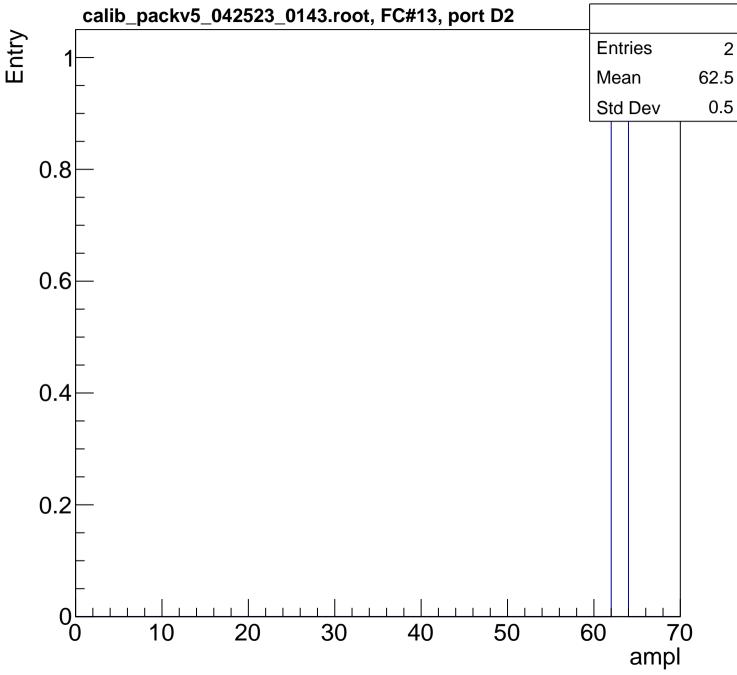


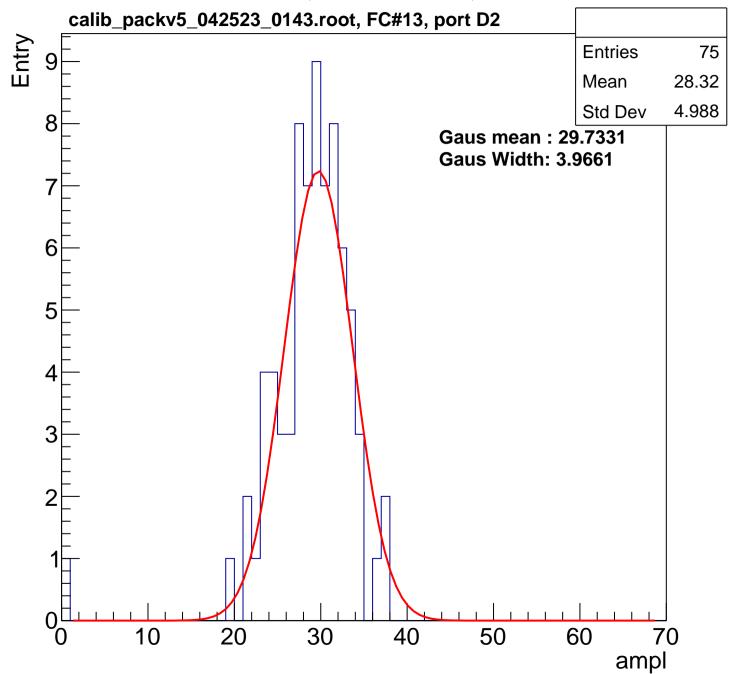


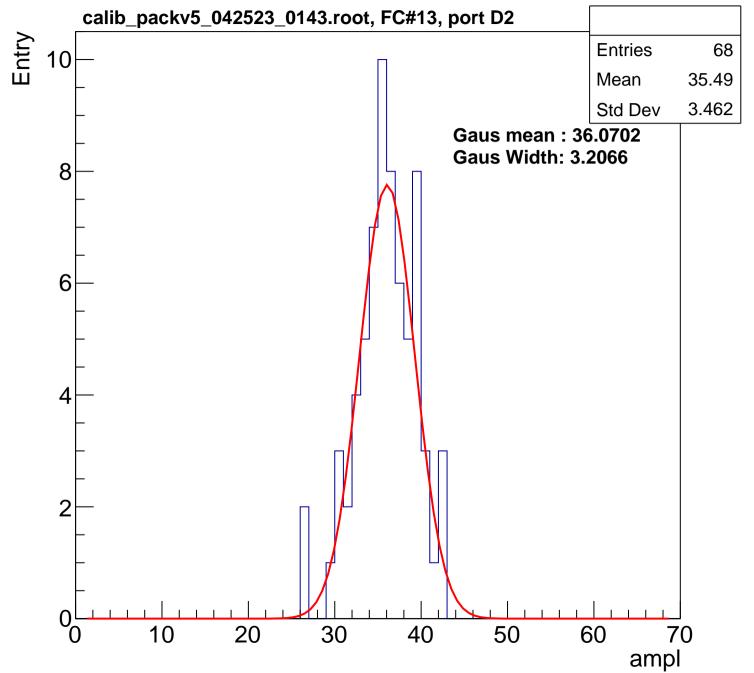


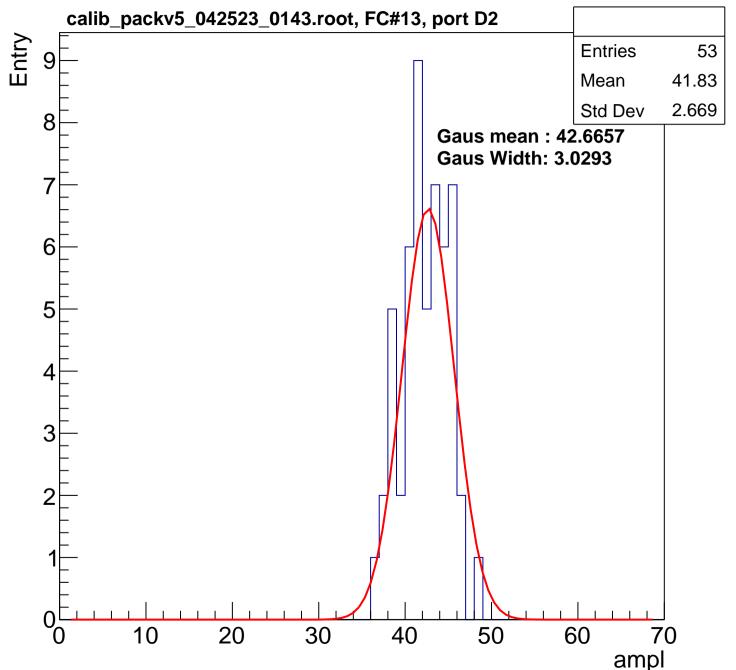


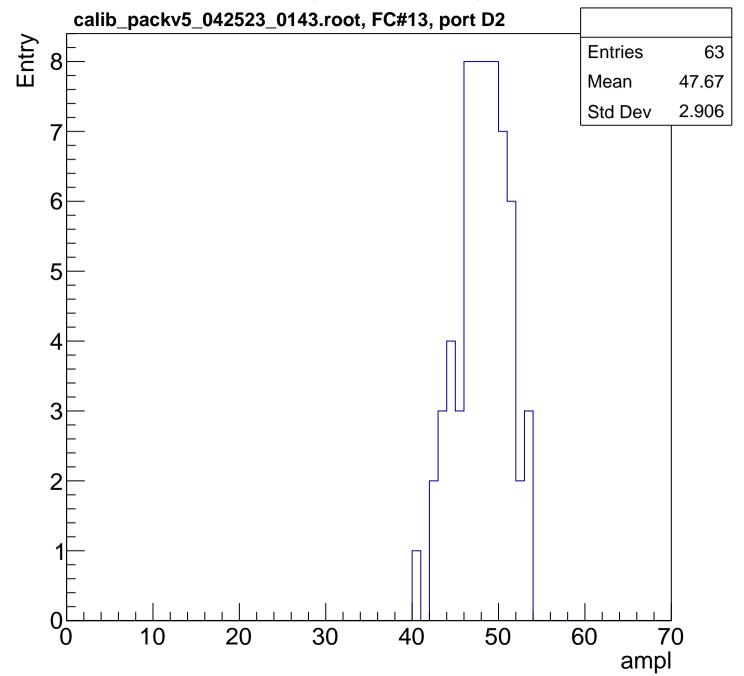


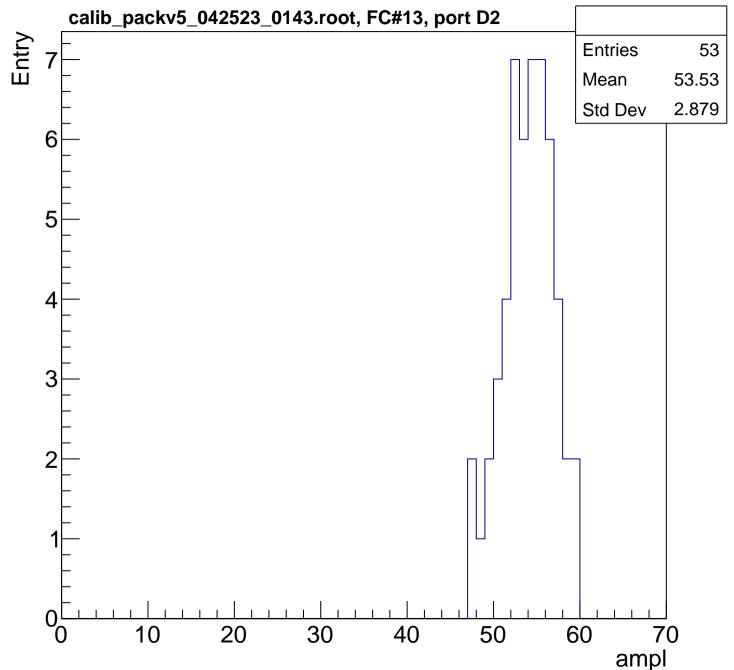


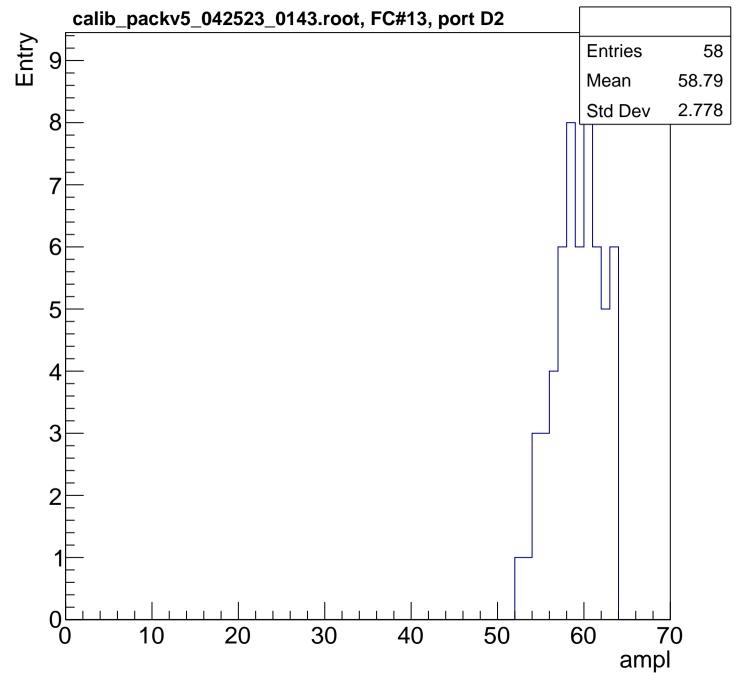


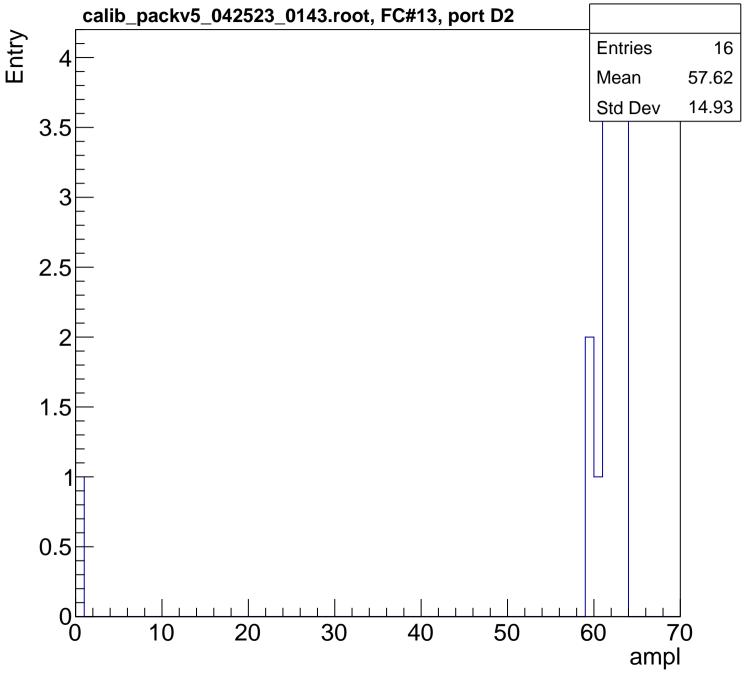


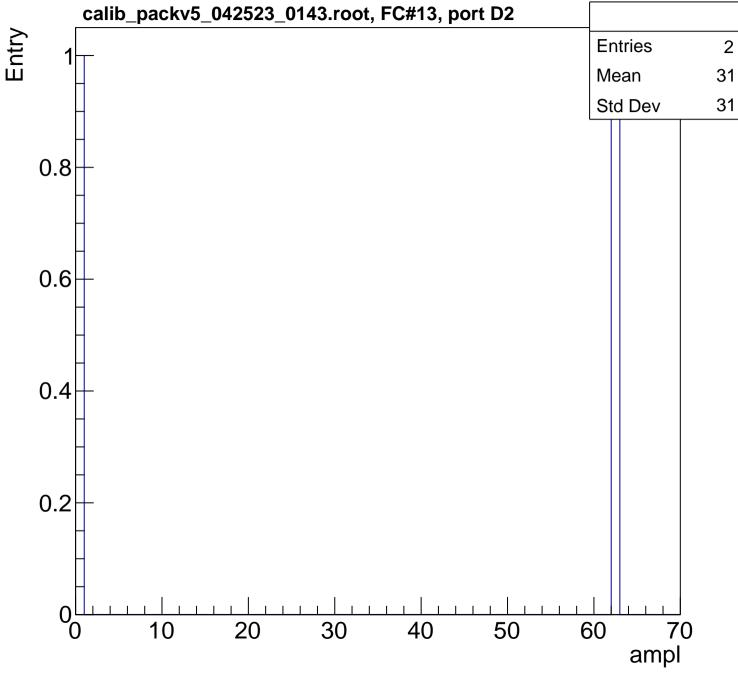


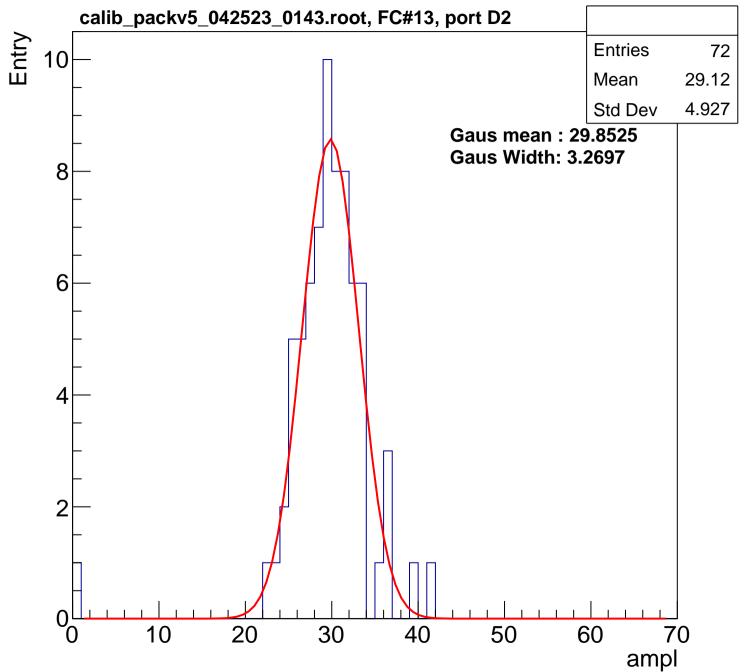


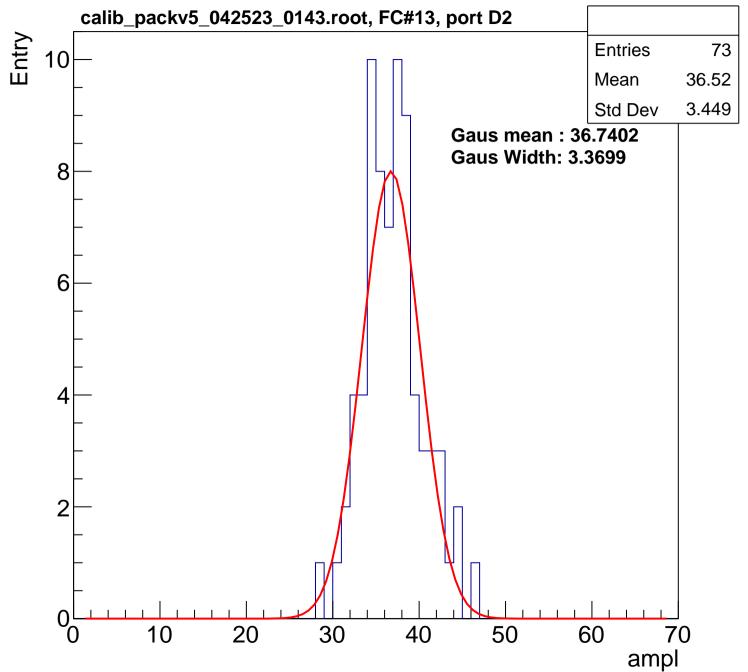


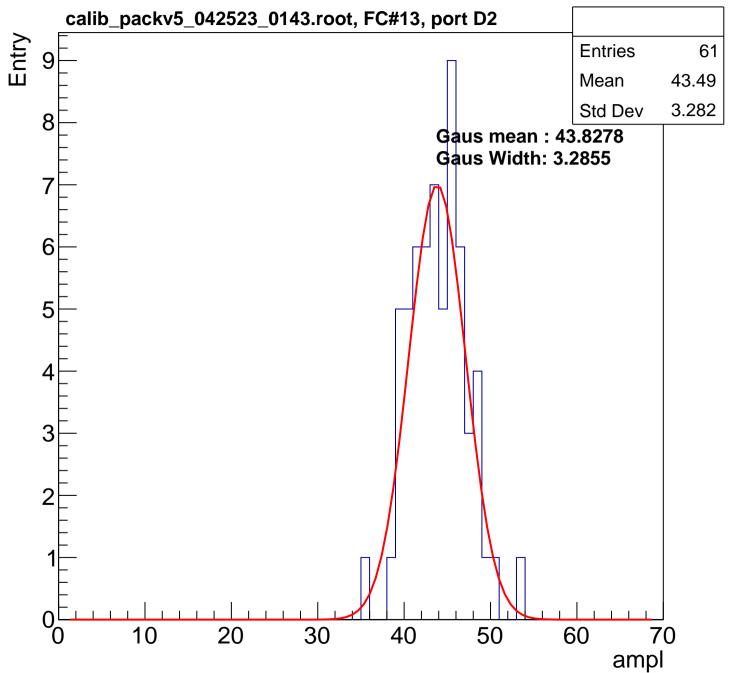


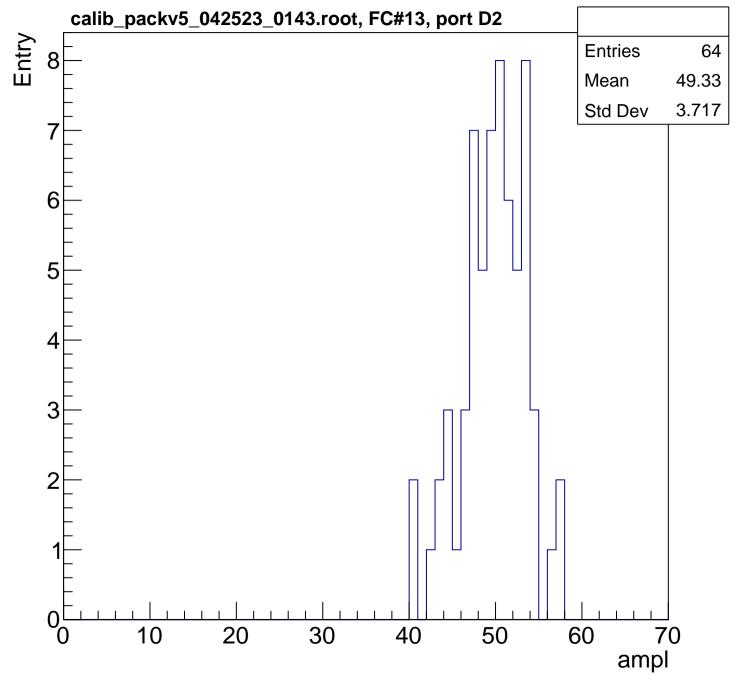


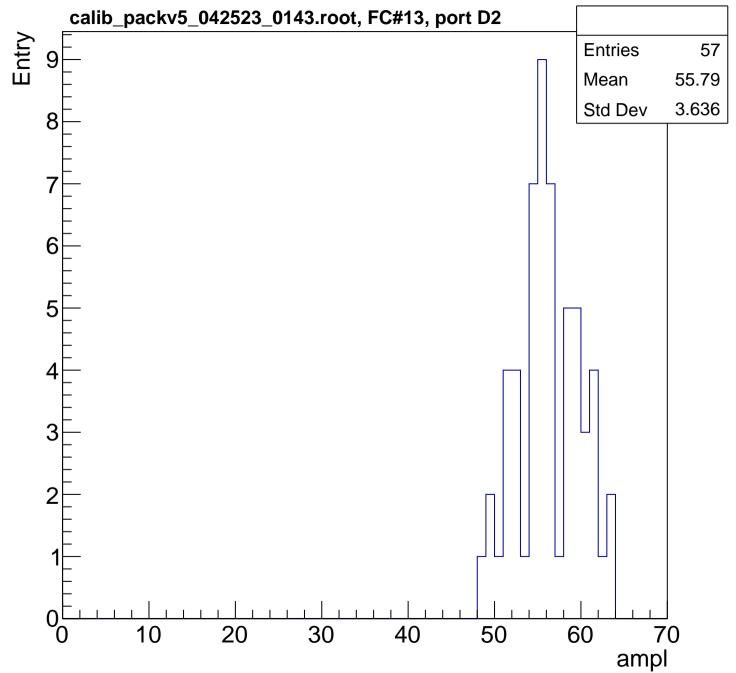


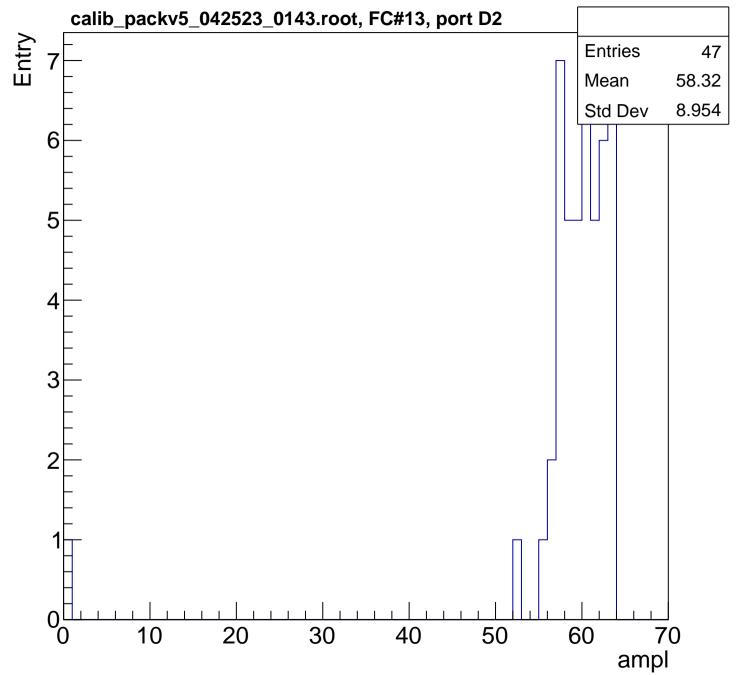


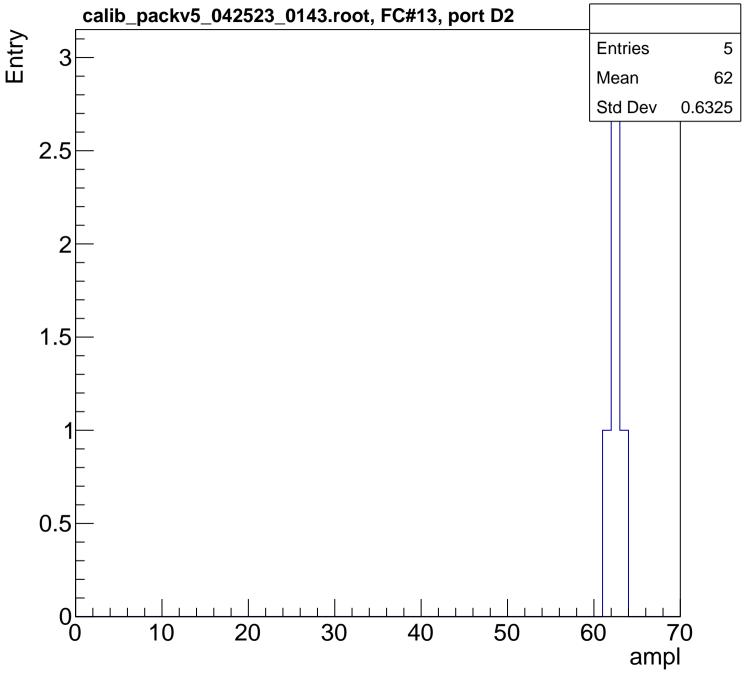




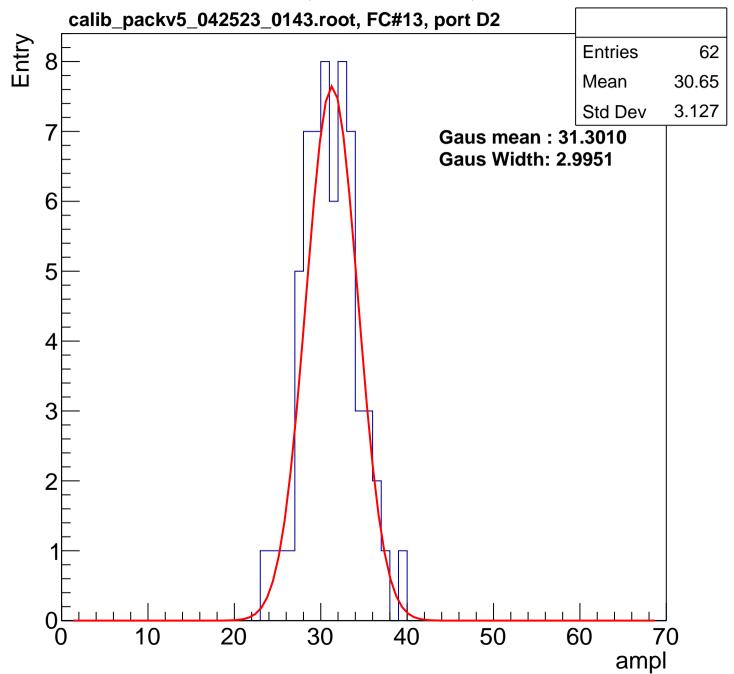


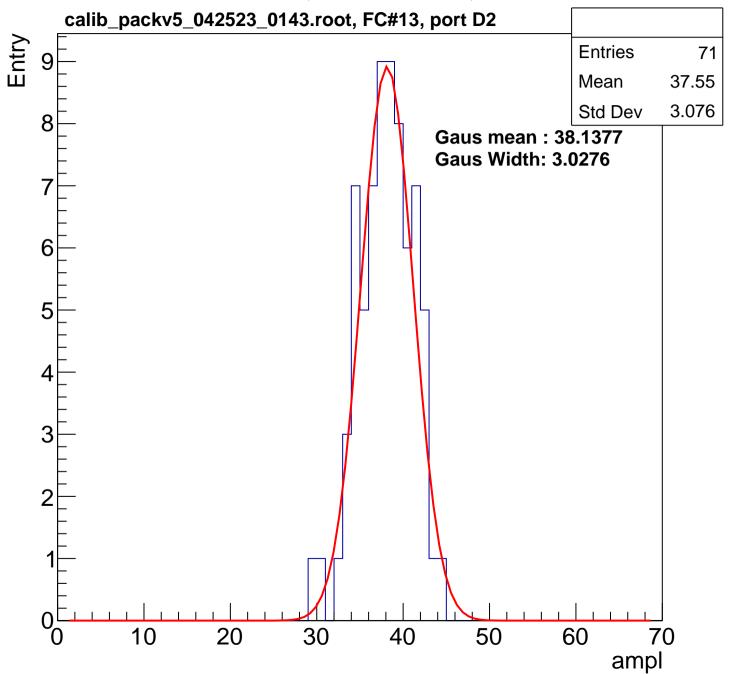


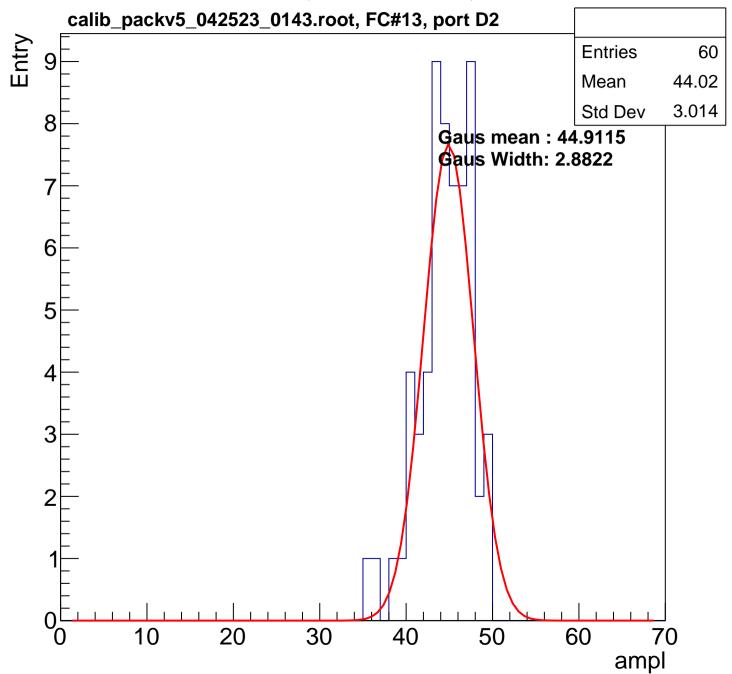


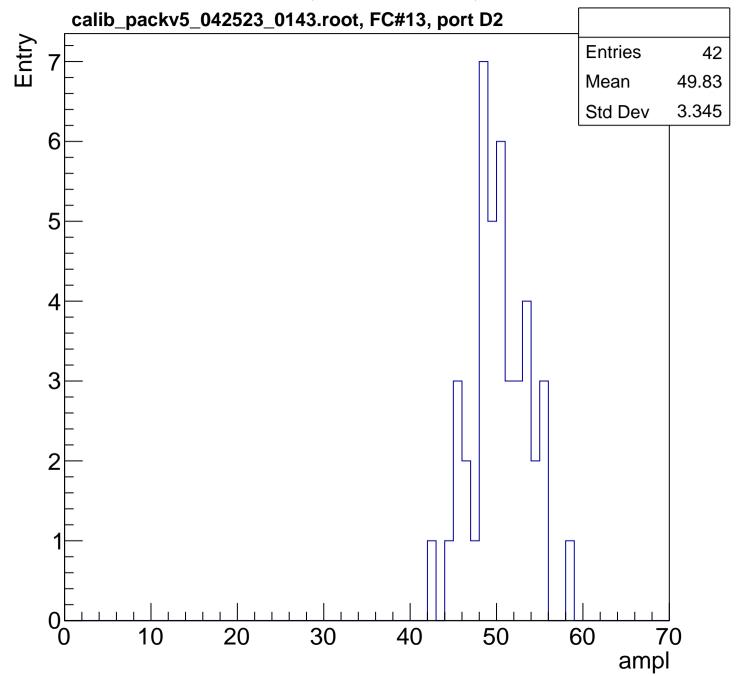


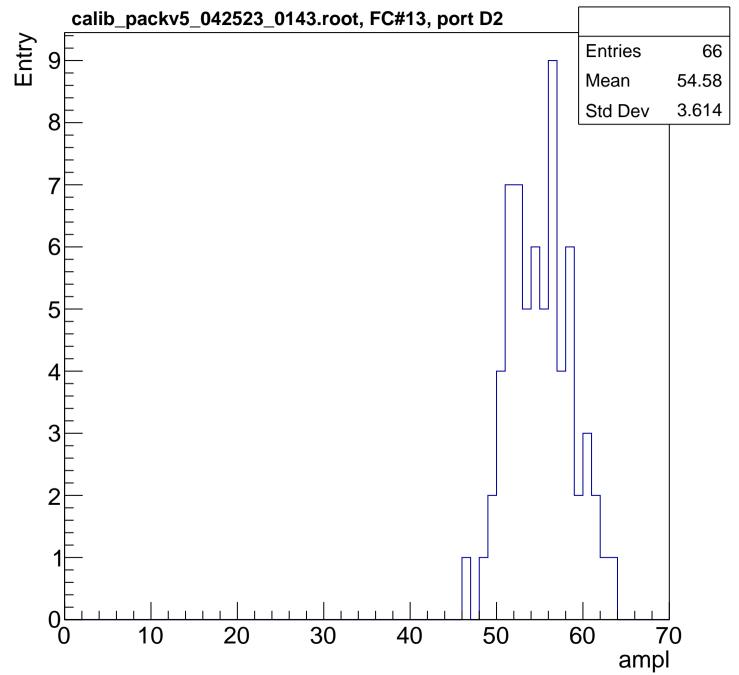


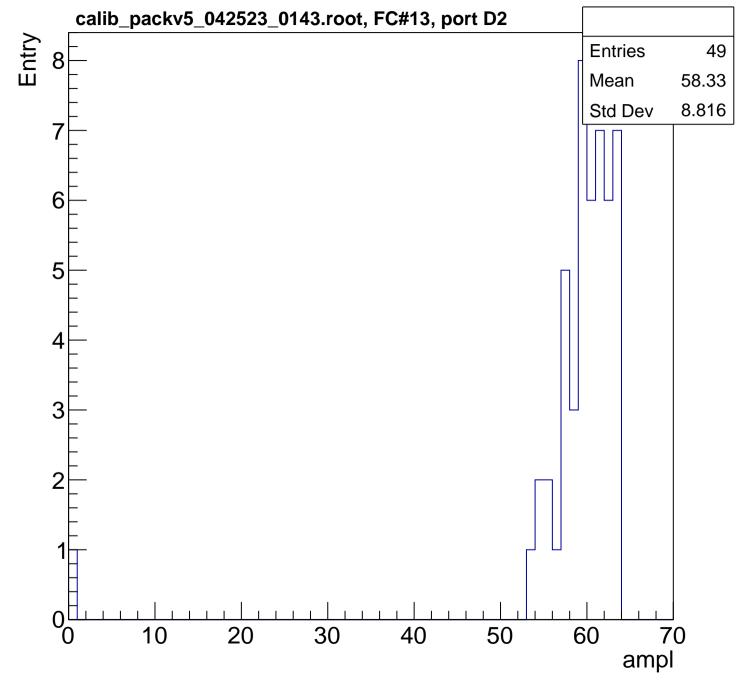


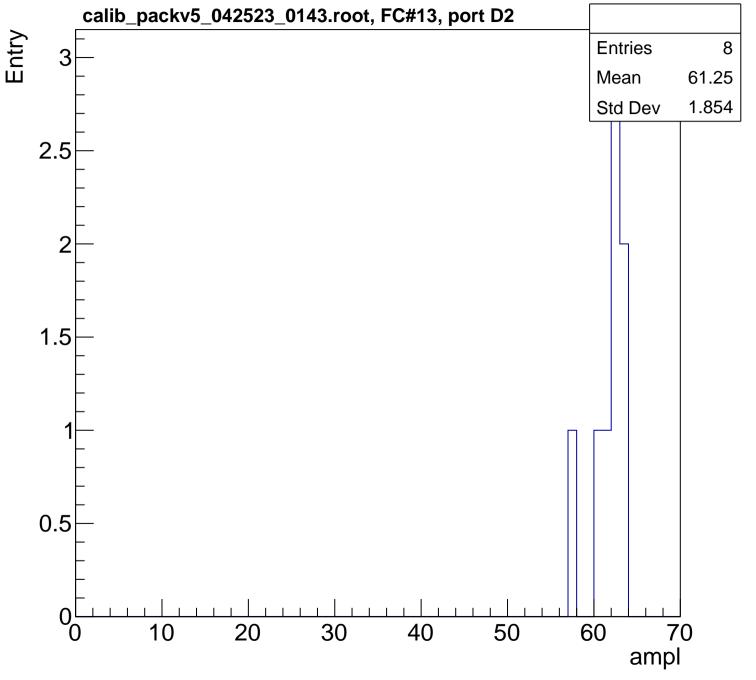












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