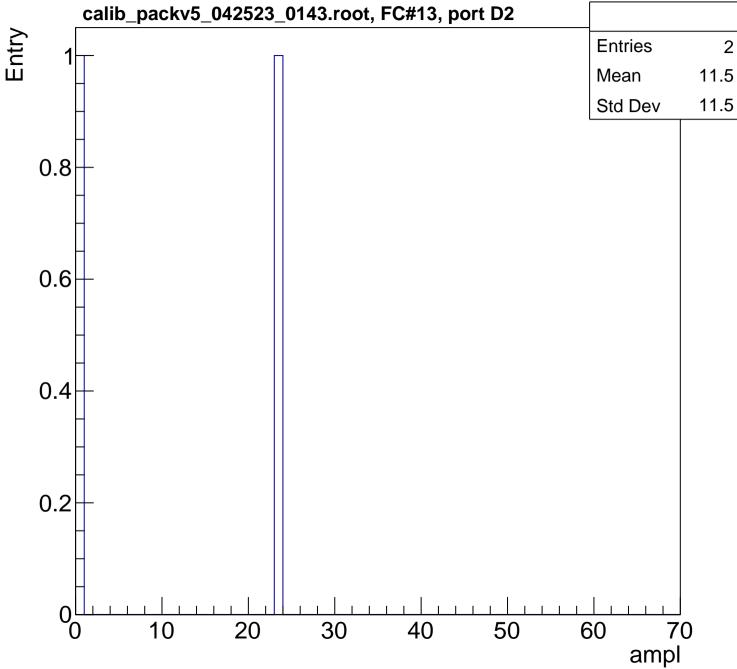
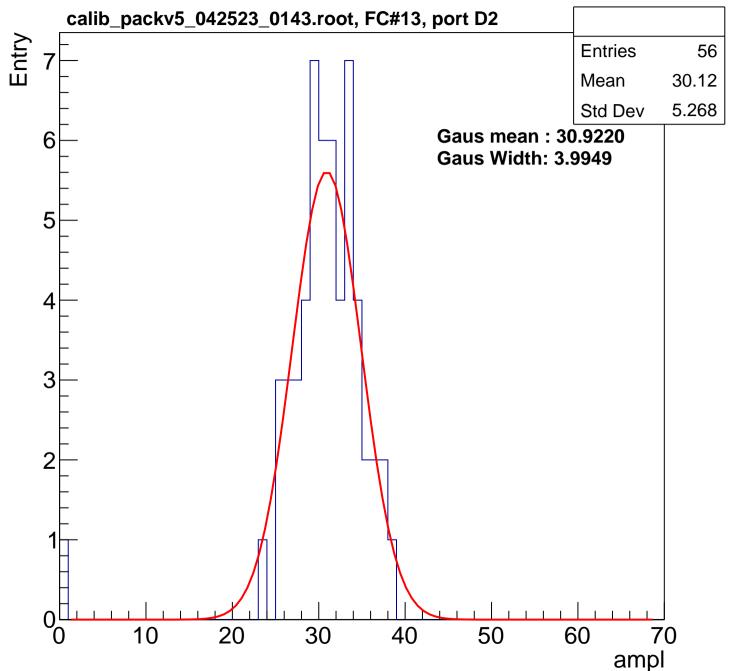
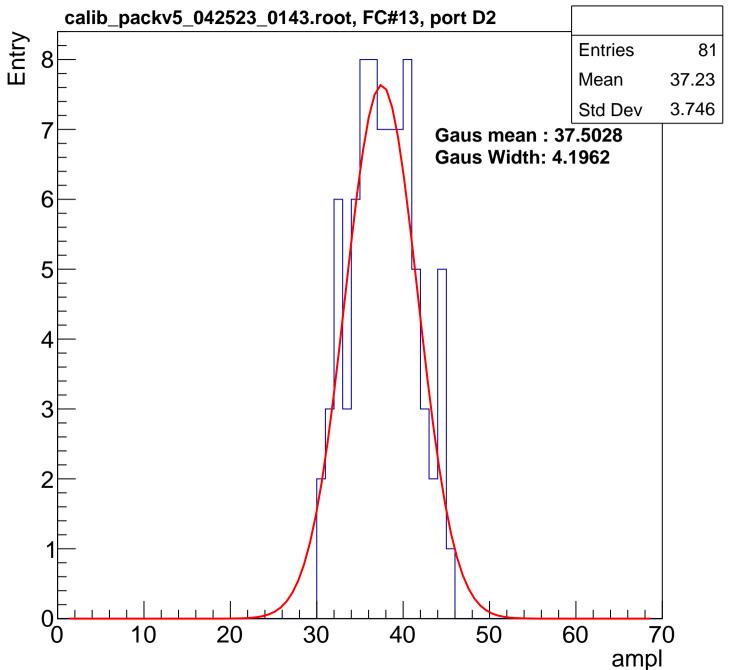
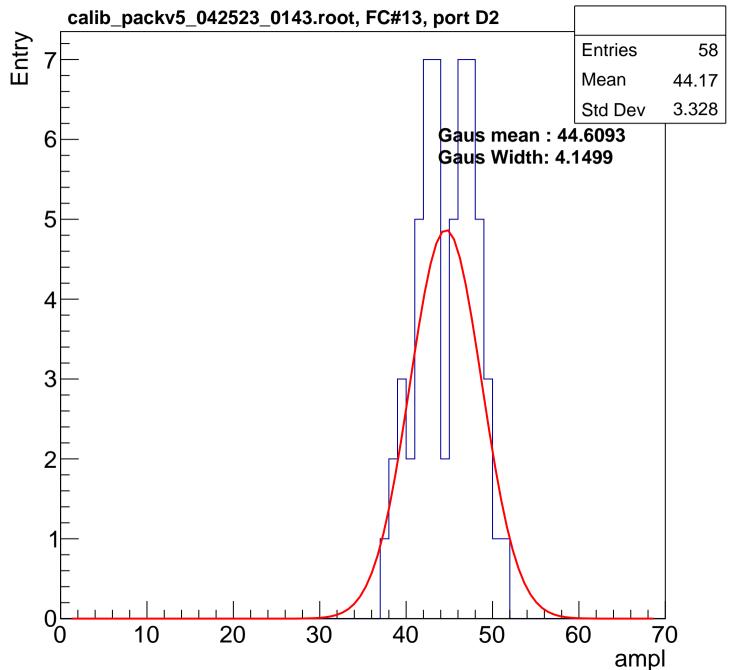


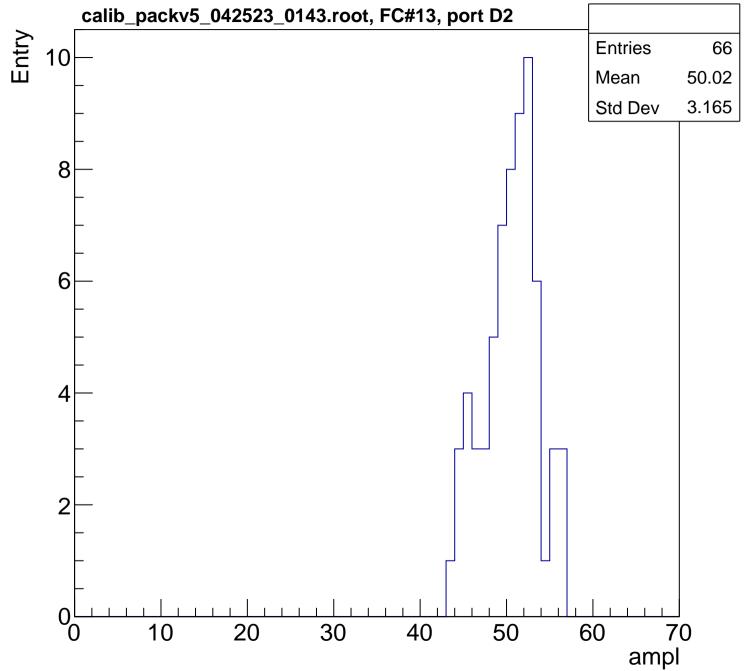
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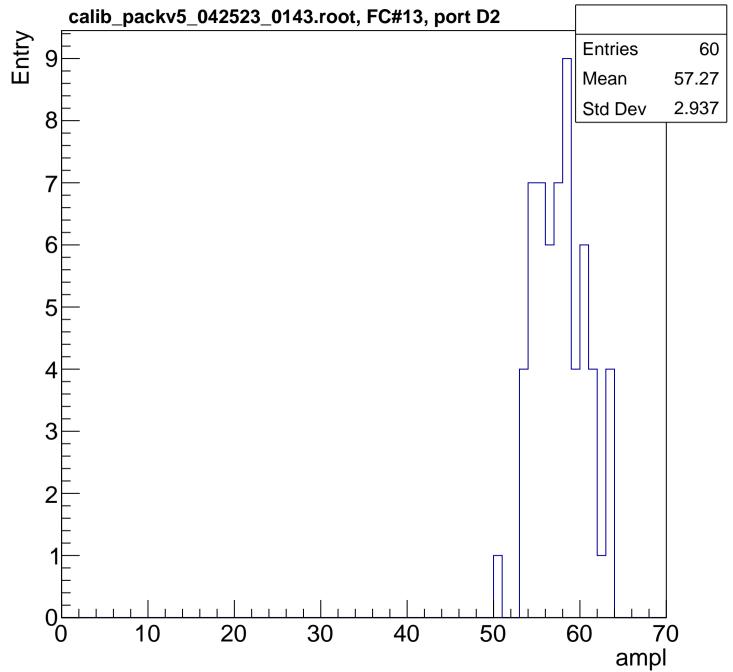


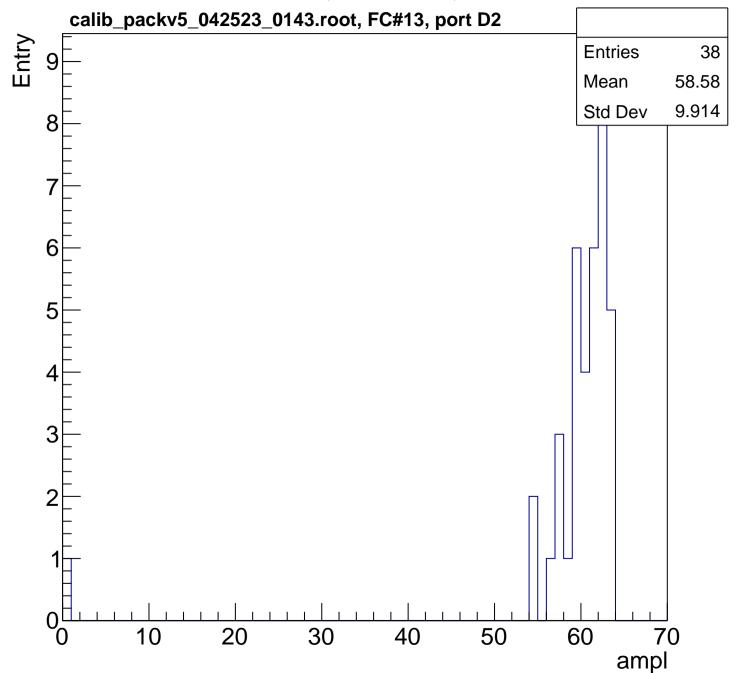


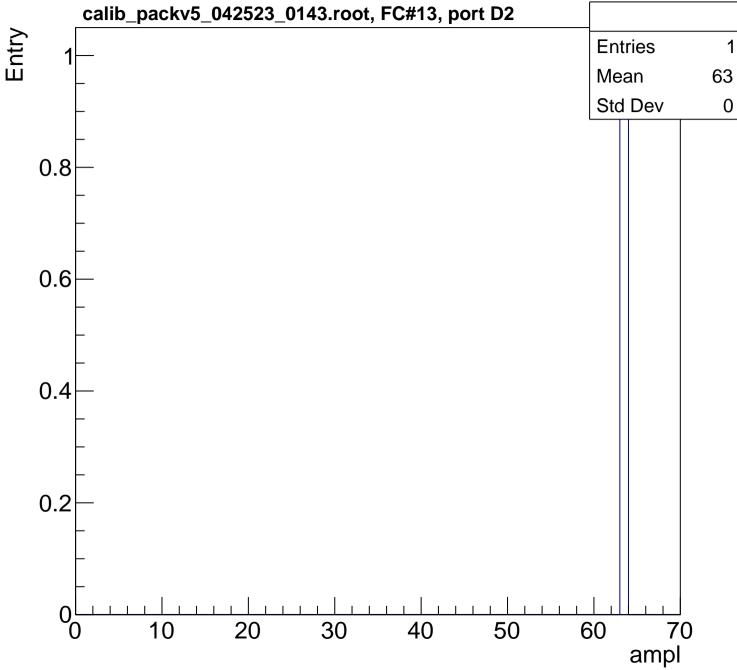


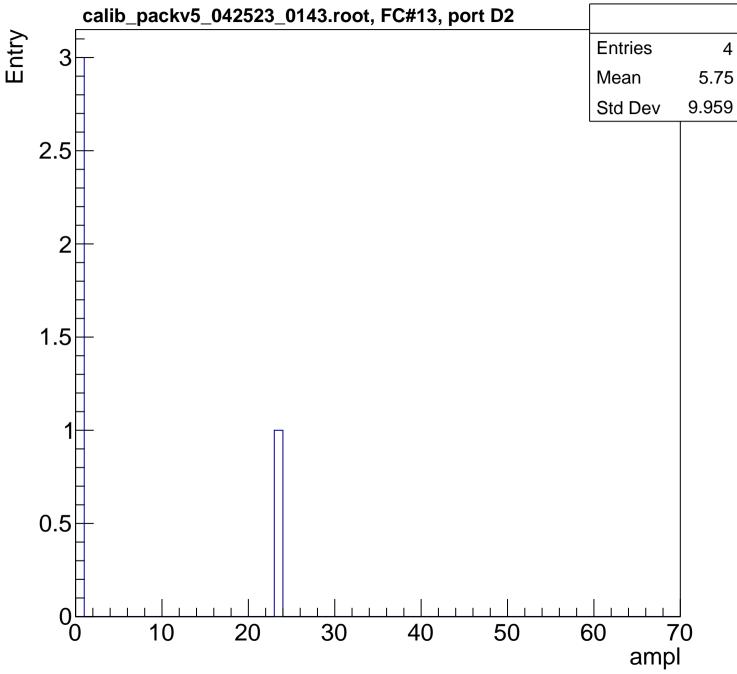


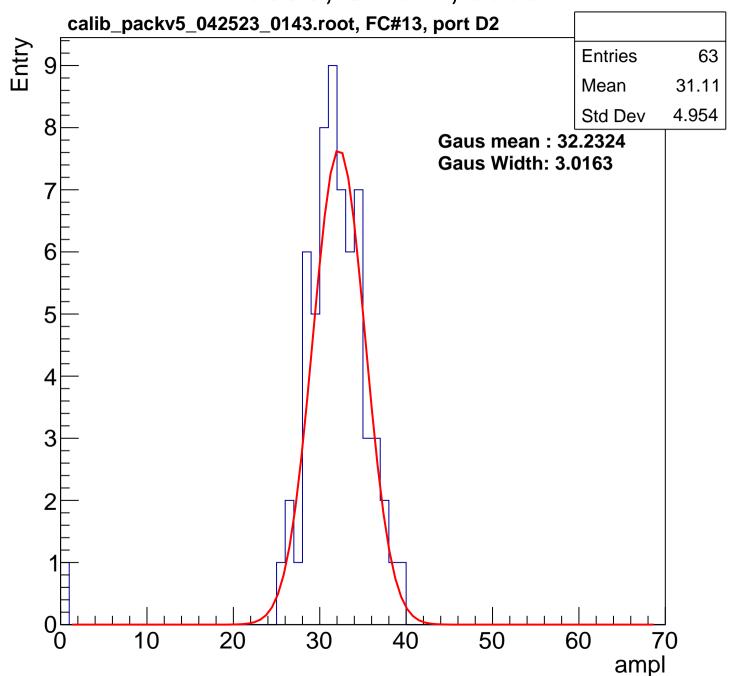


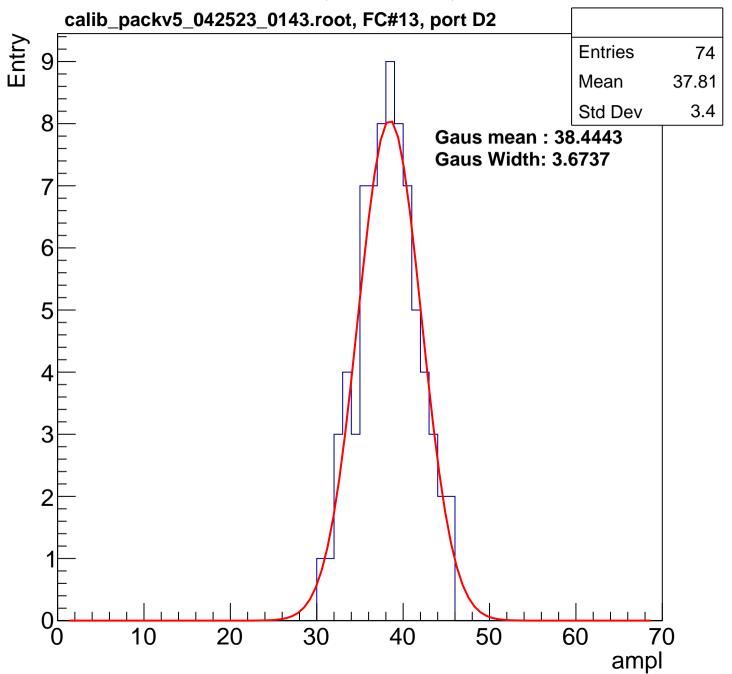


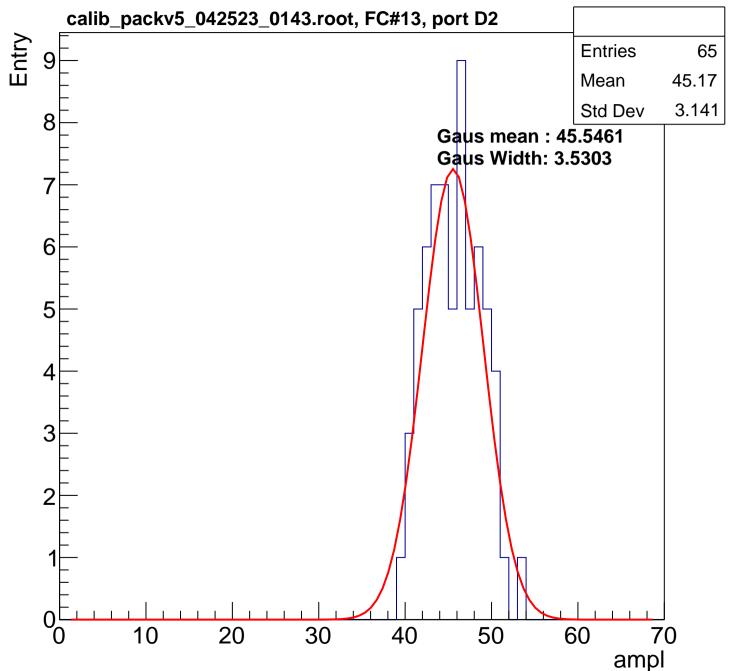


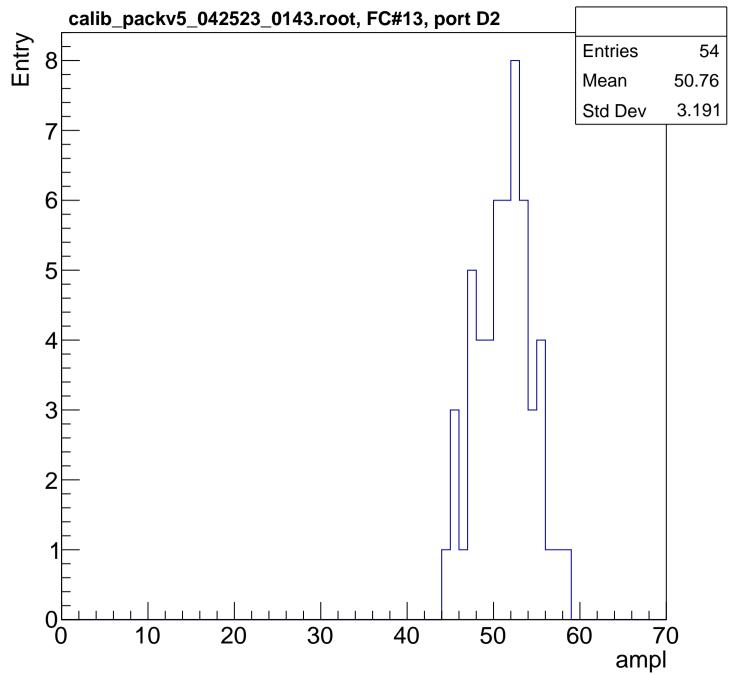


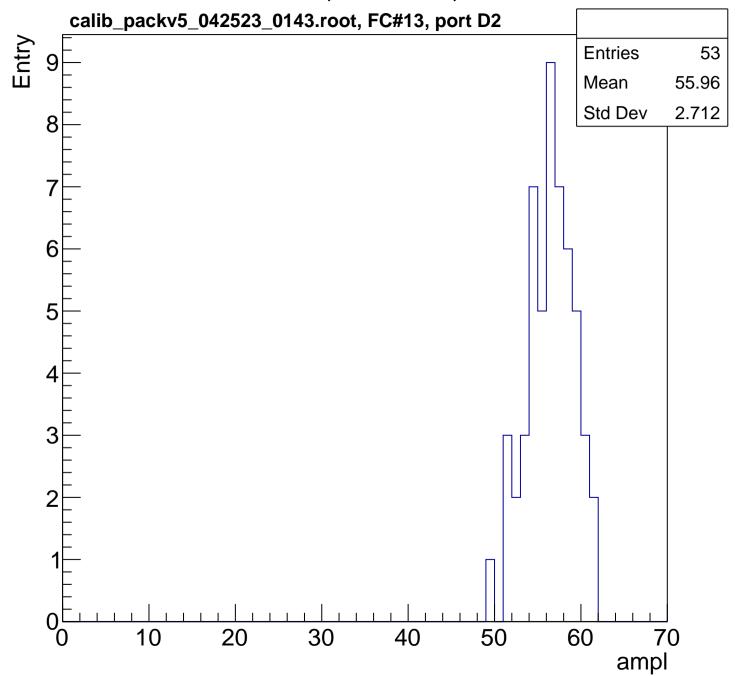


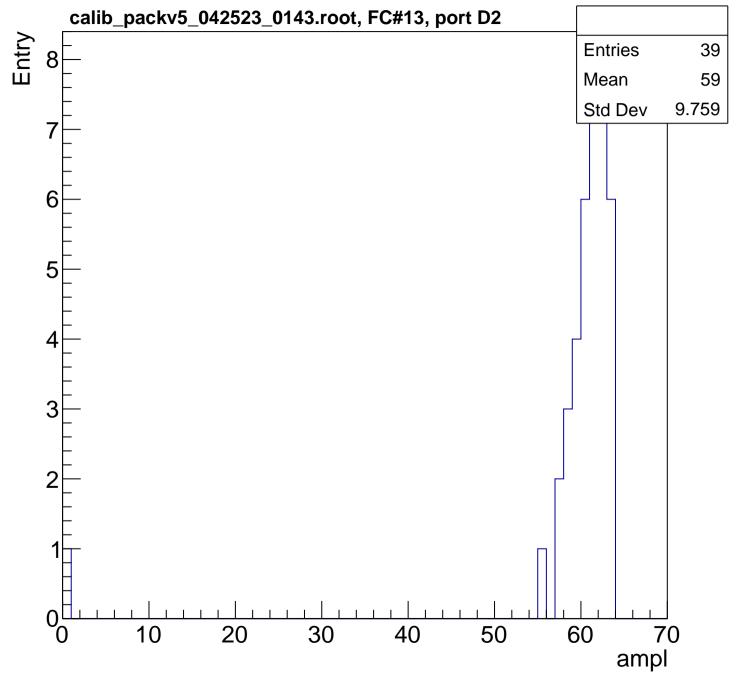


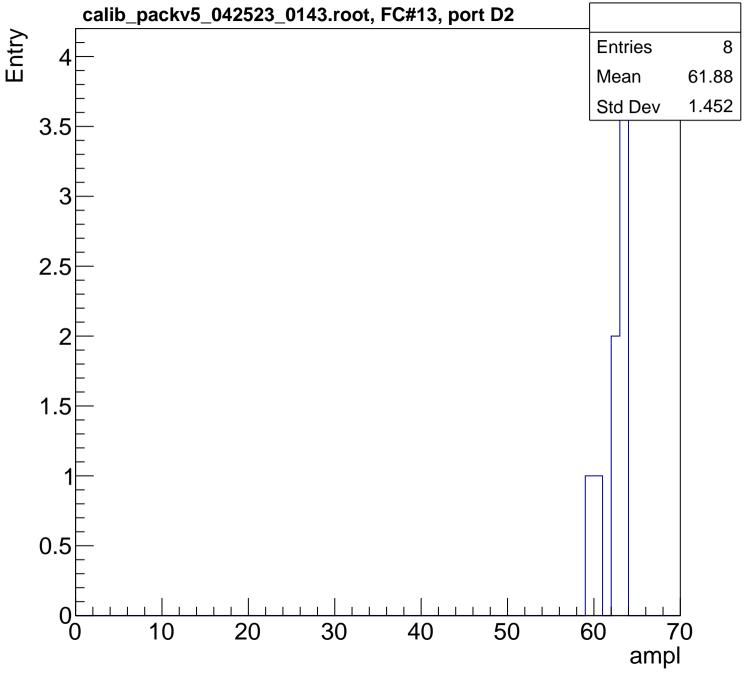


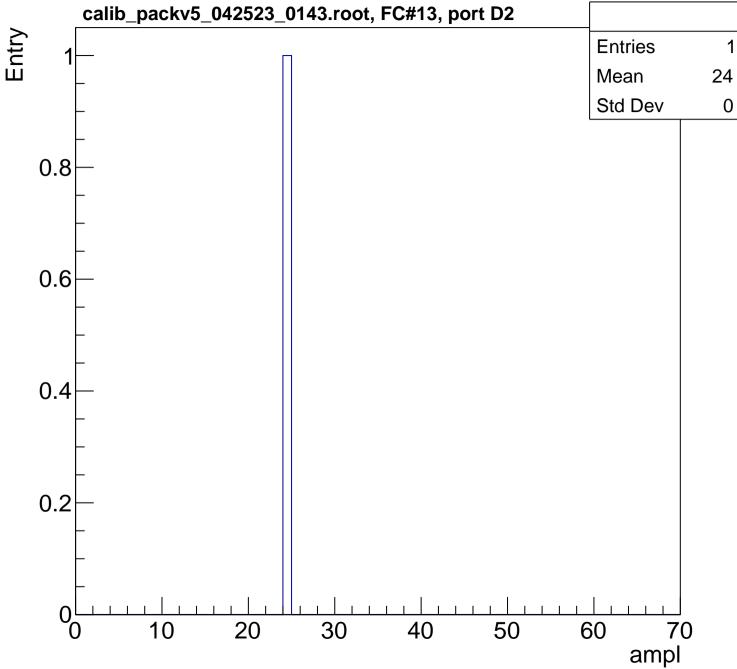


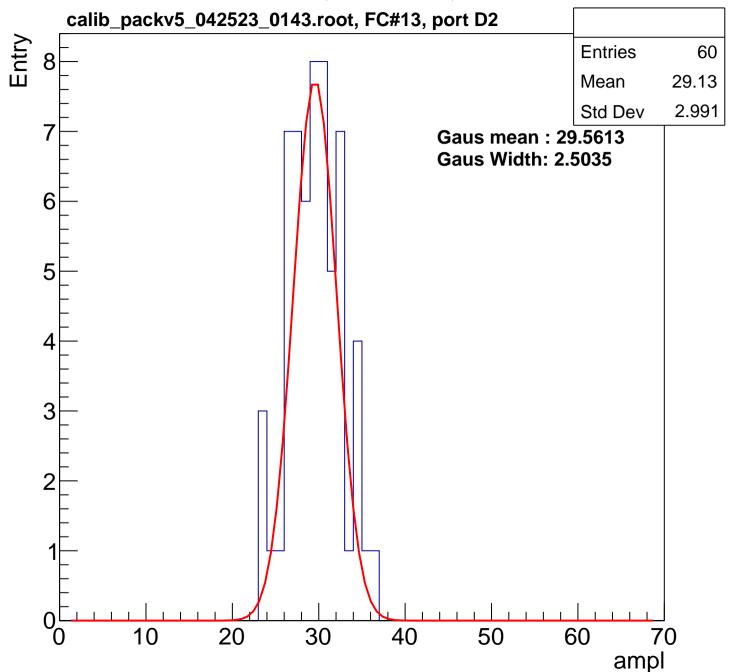


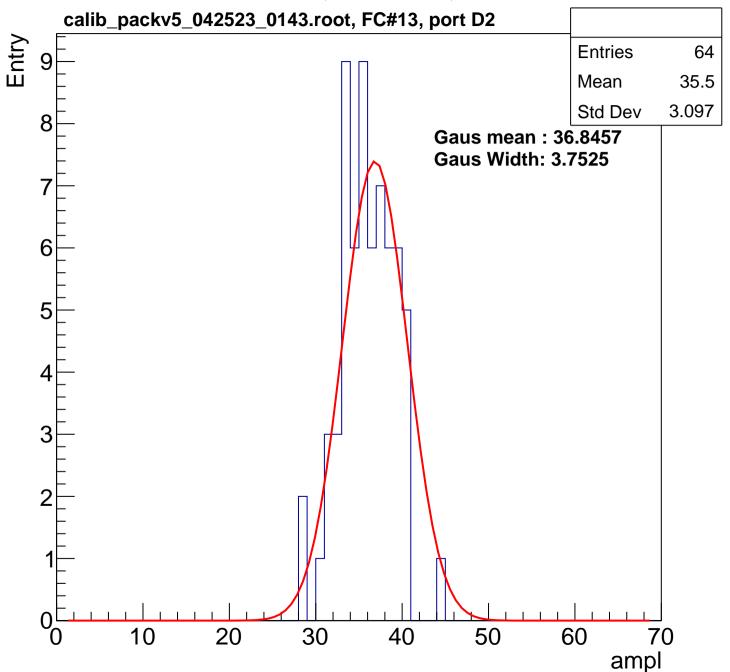


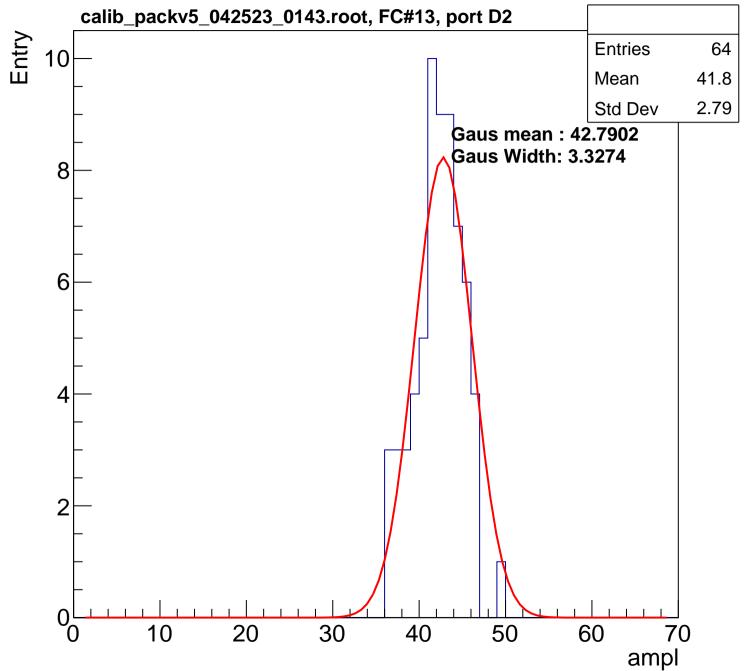


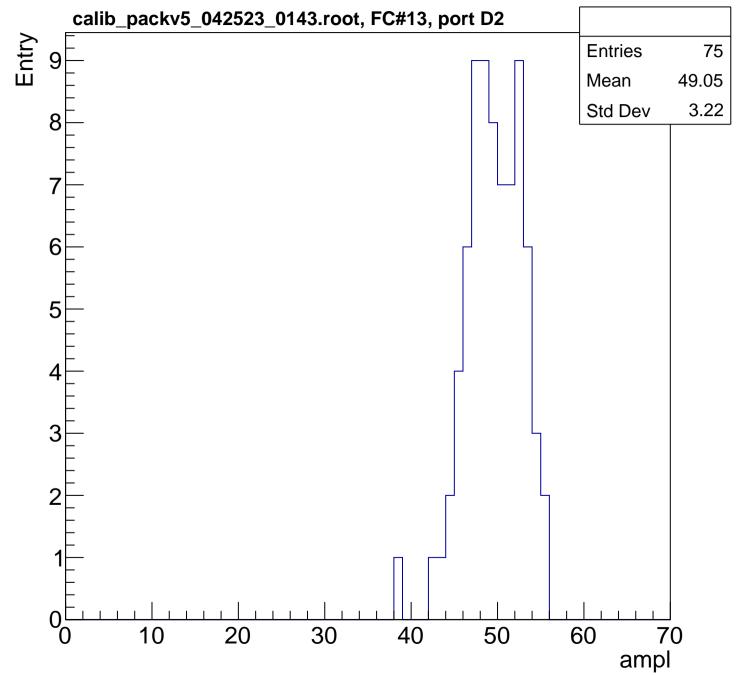


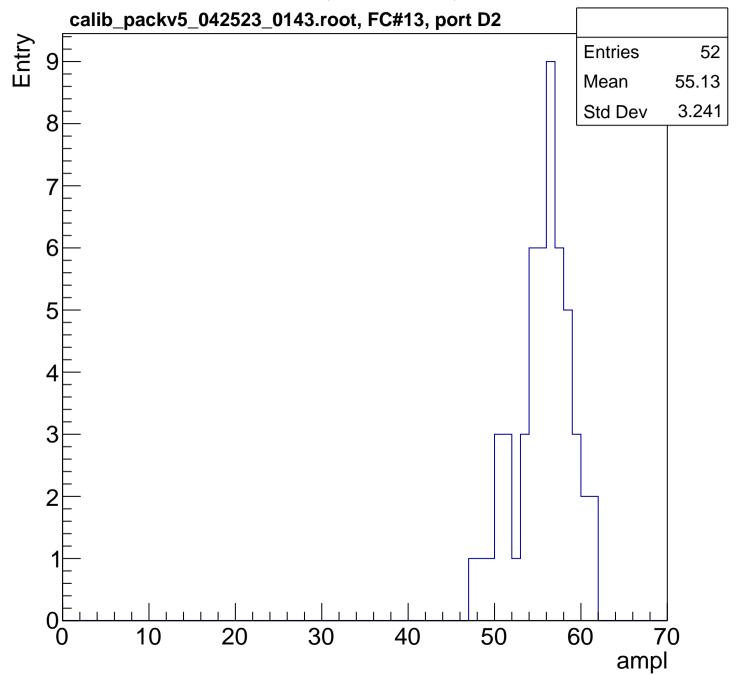


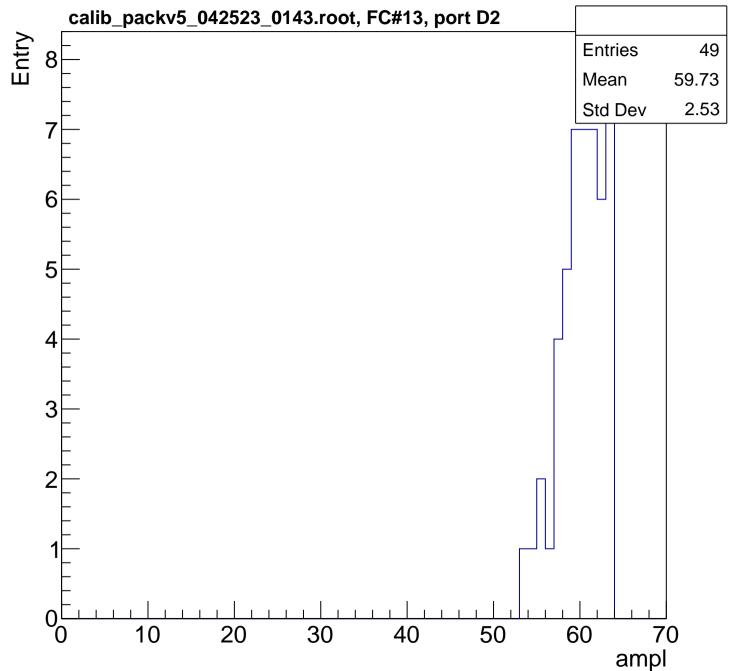


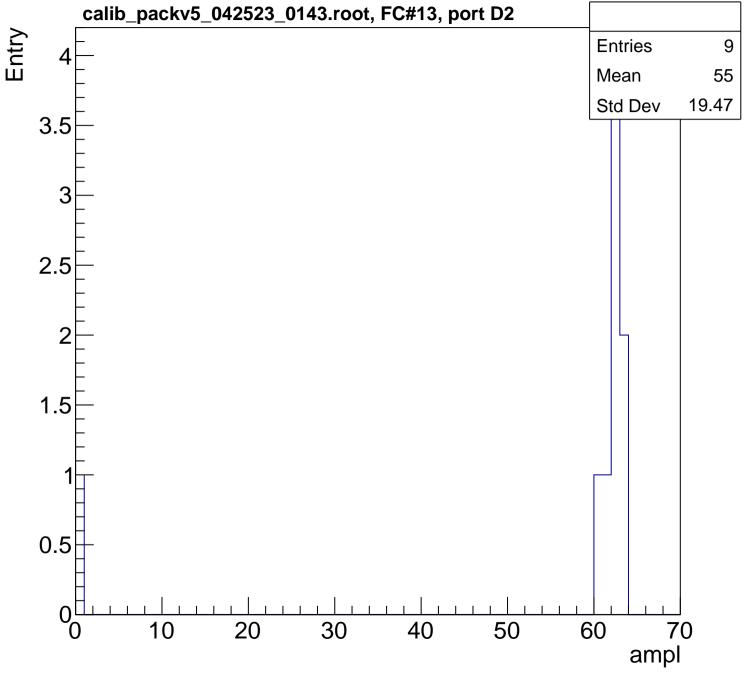




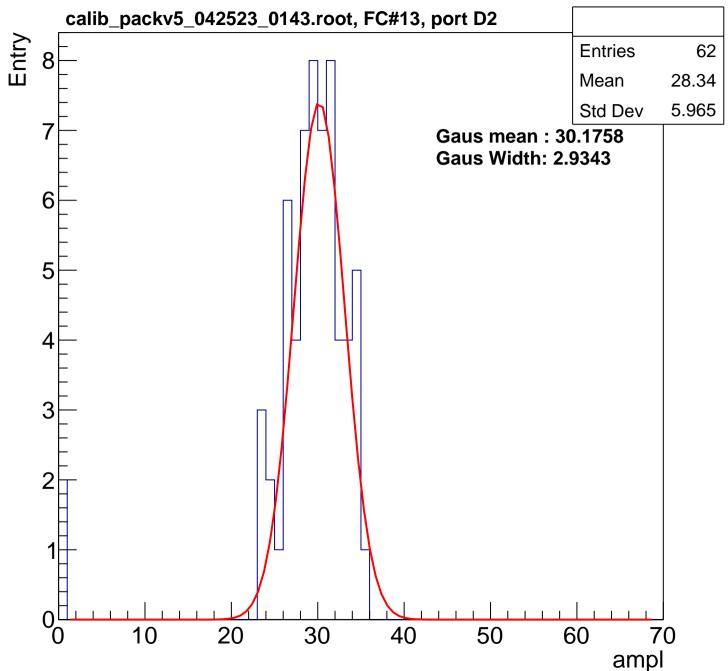


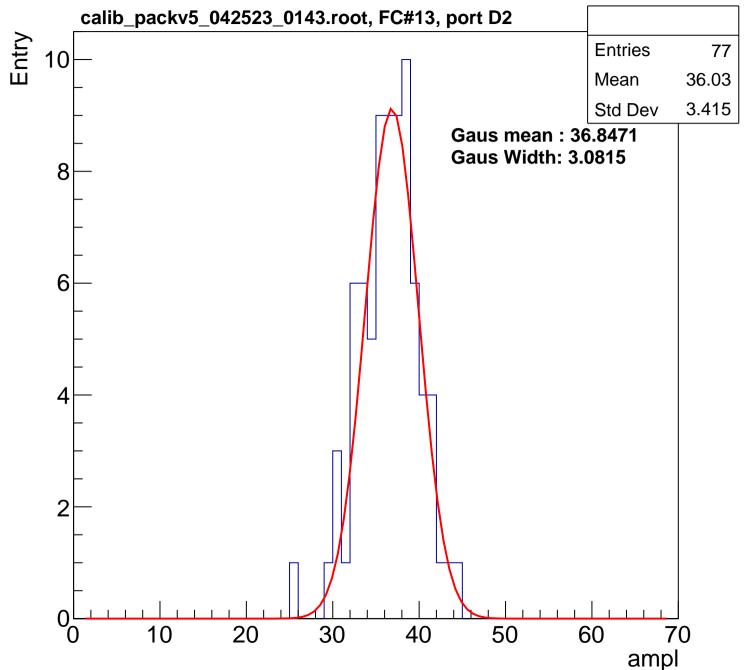


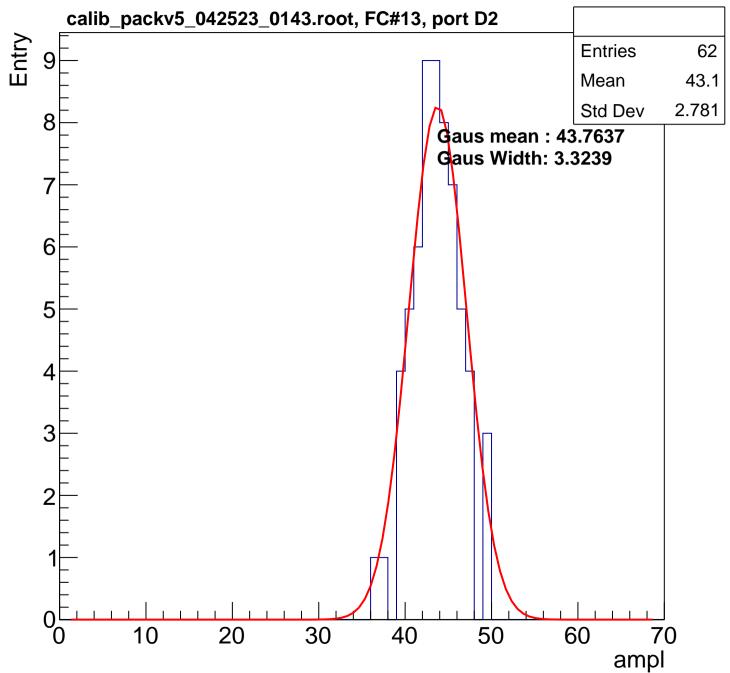


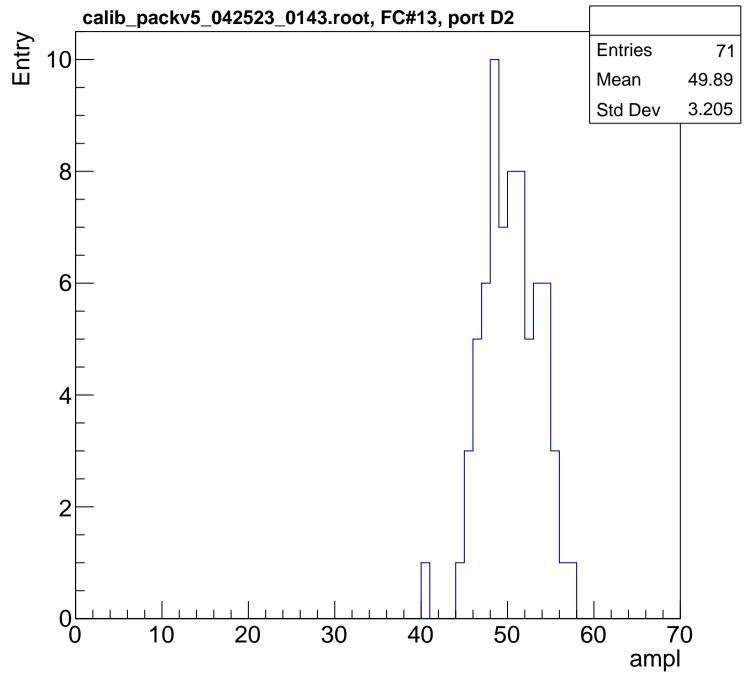


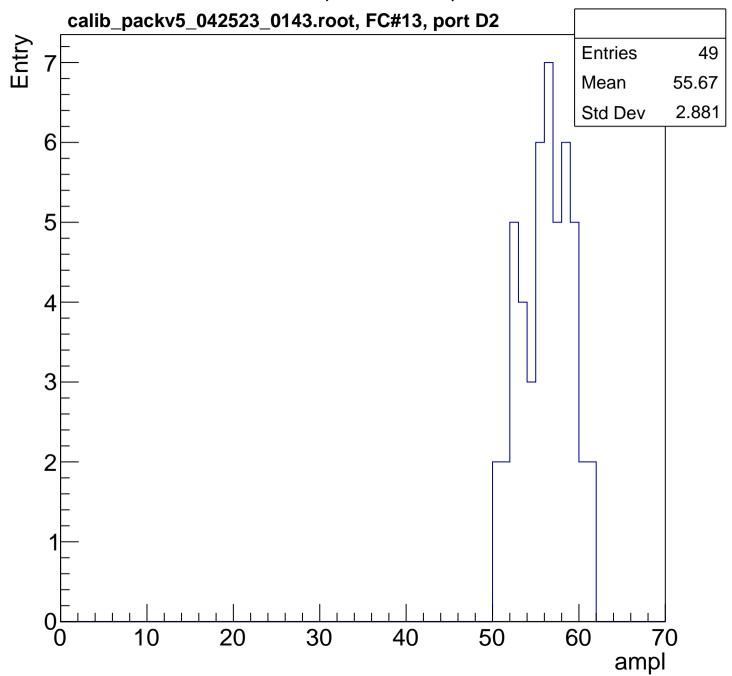
B1L003S, U7-ch5, adc7 calib_packv5_042523_0143.root, FC#13, port D2 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

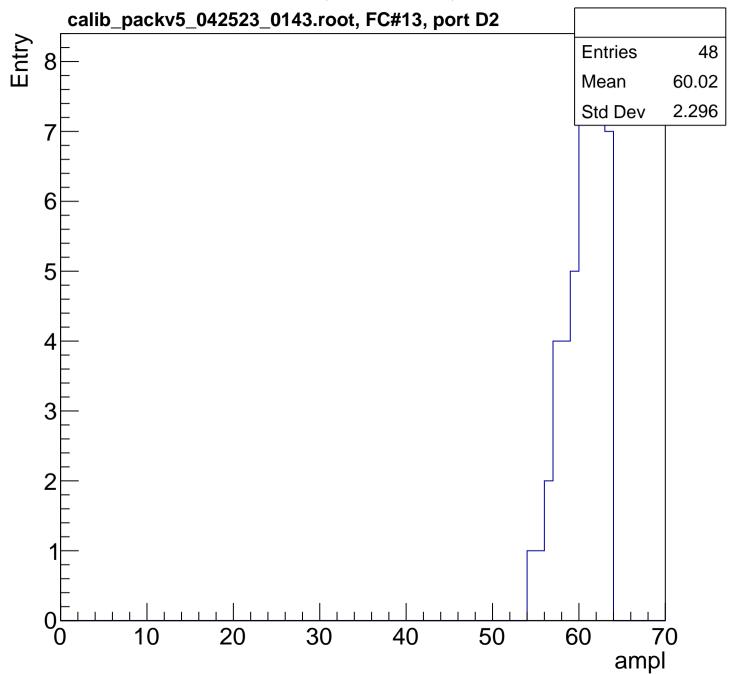


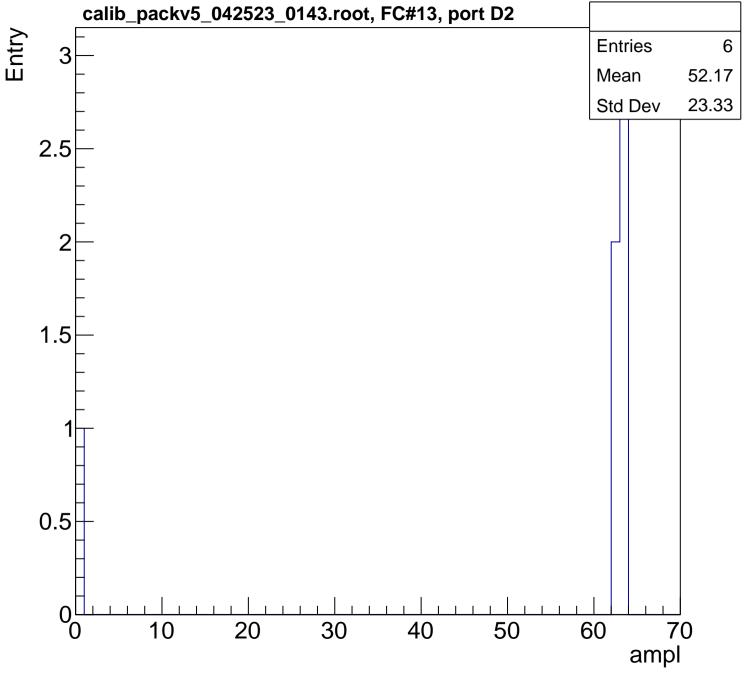




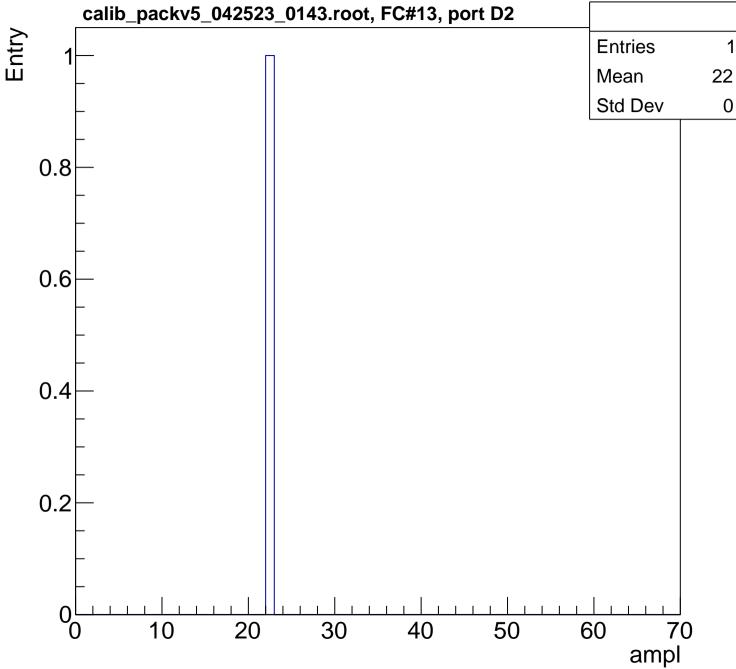


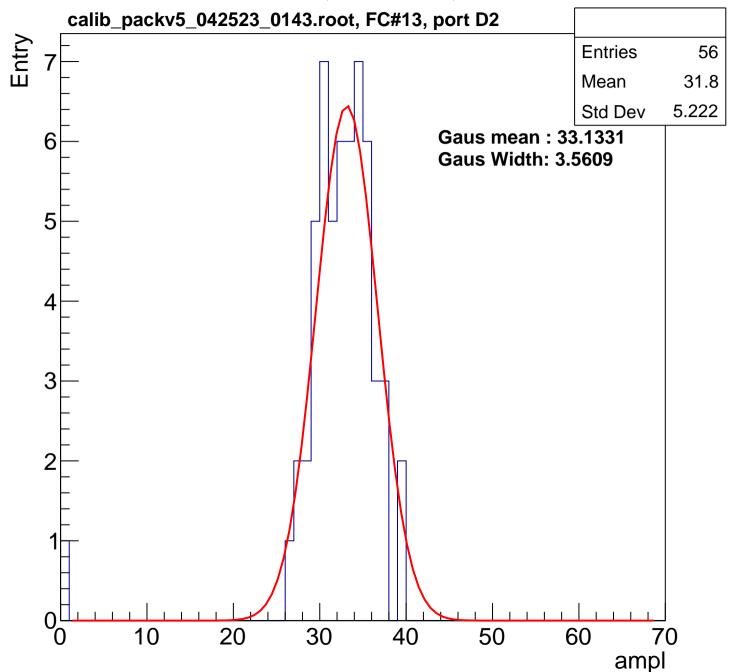


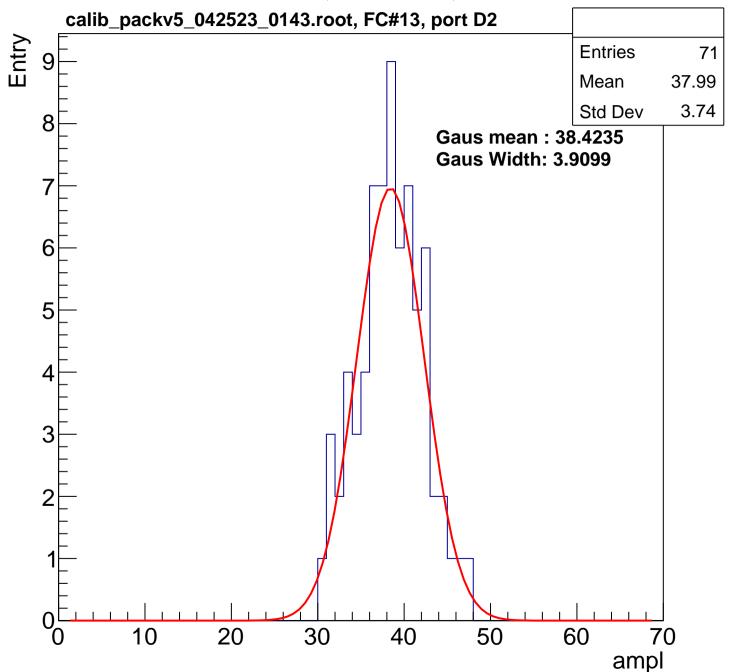


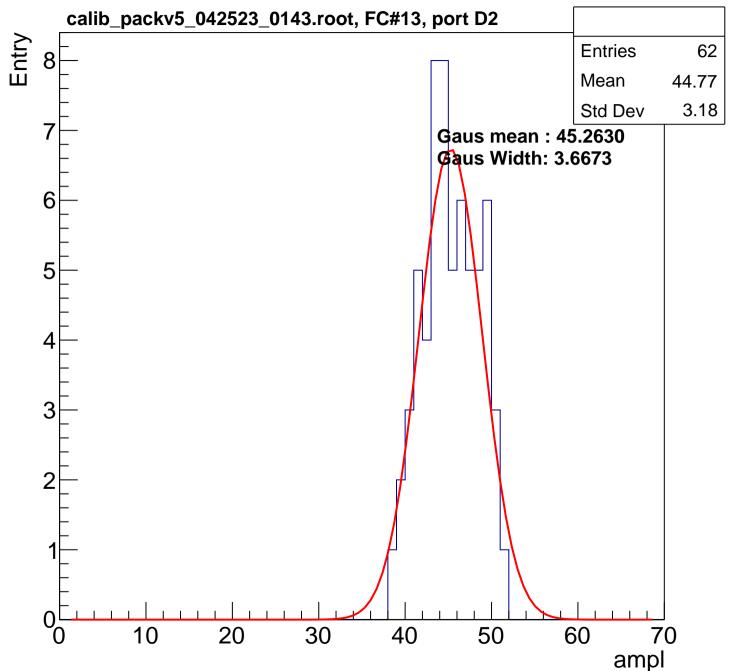


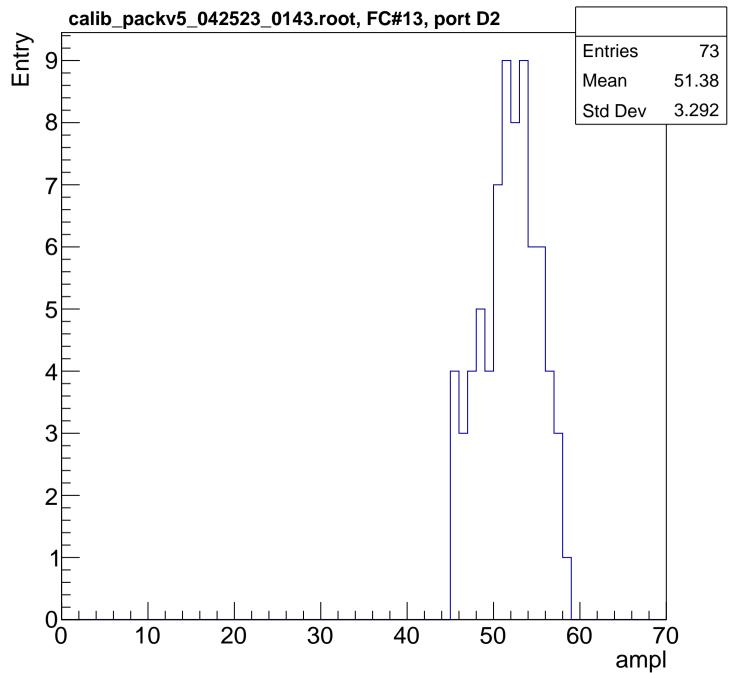
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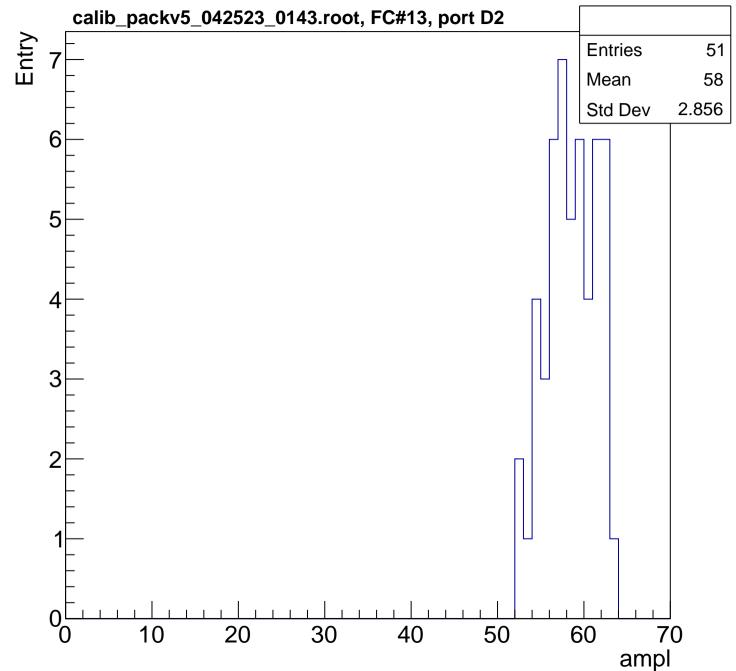


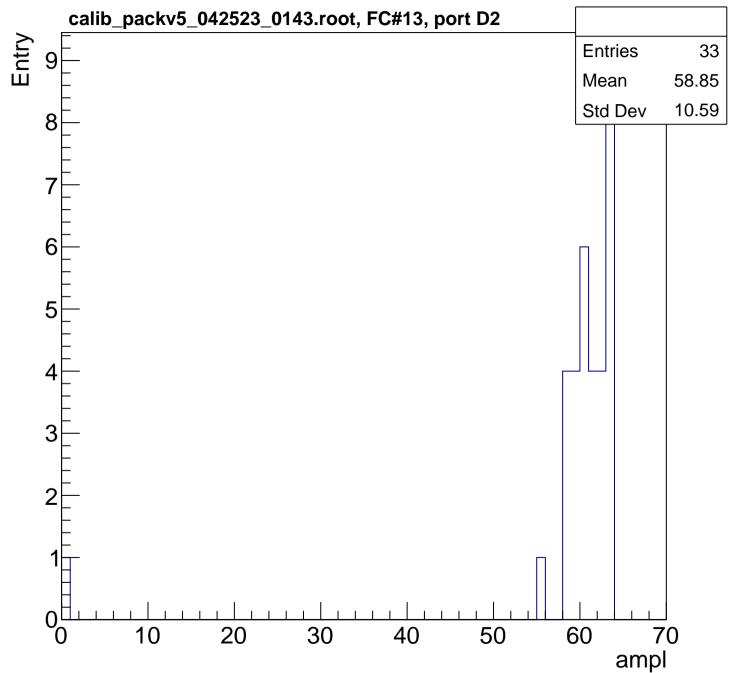






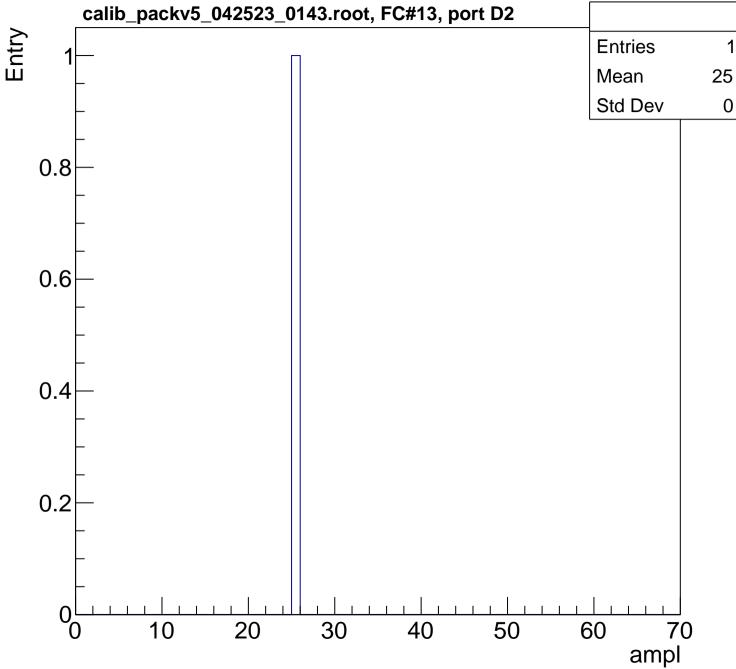


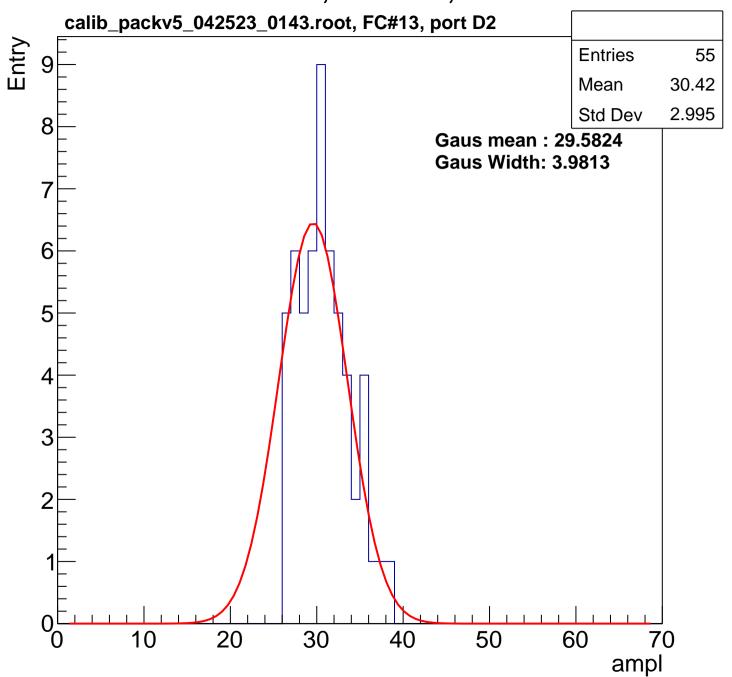


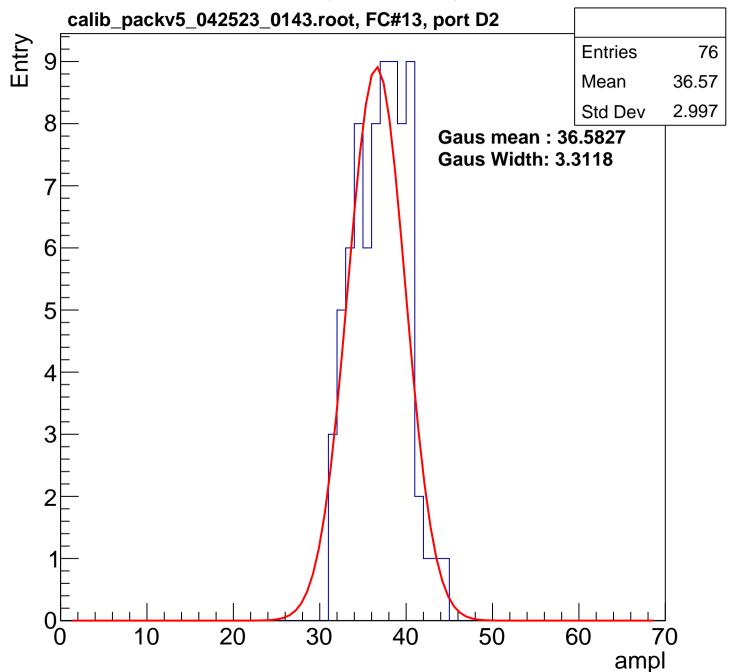


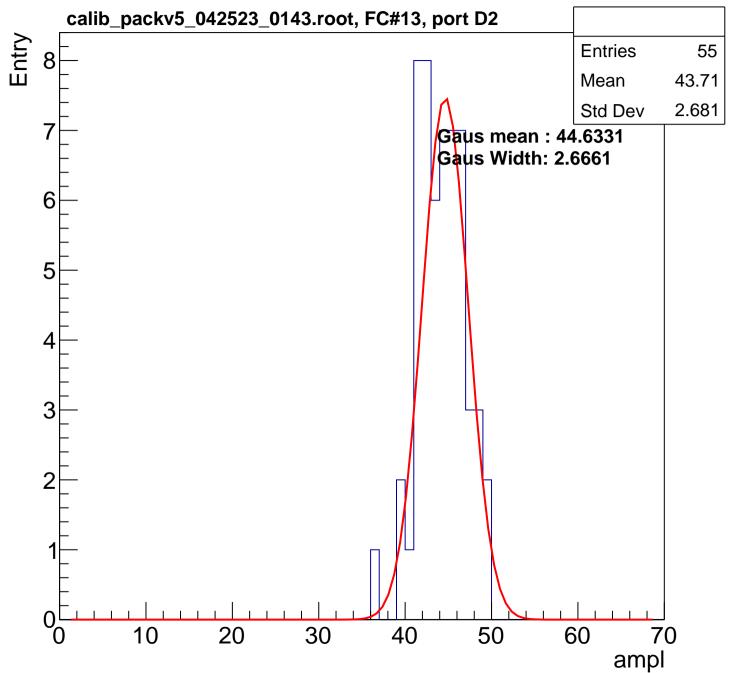


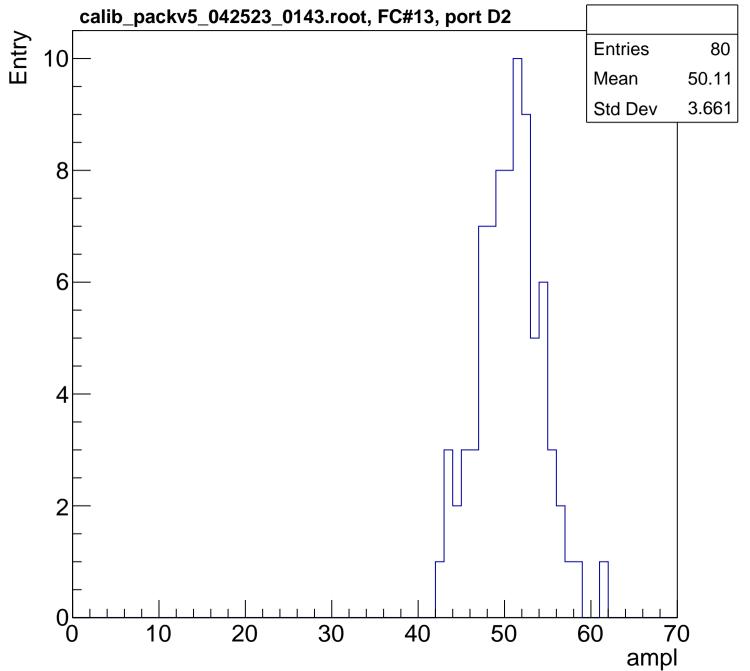
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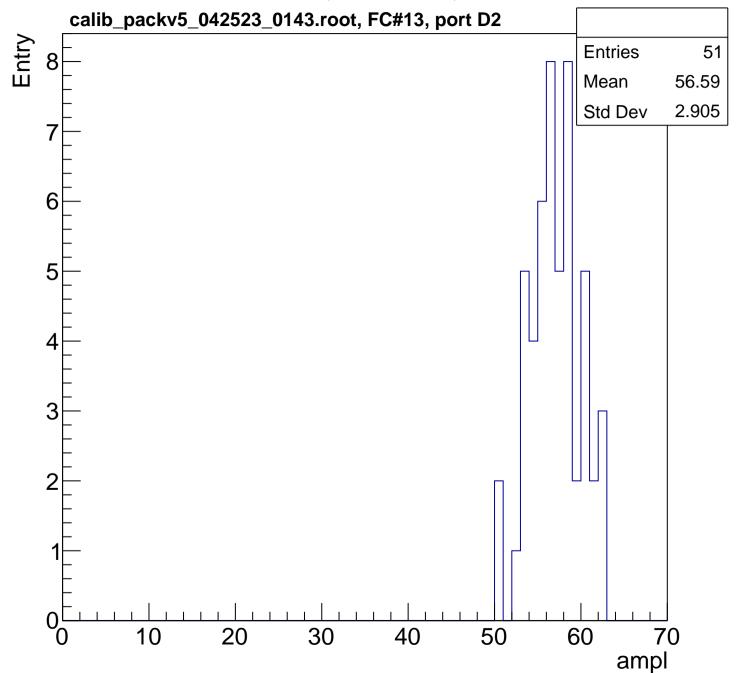


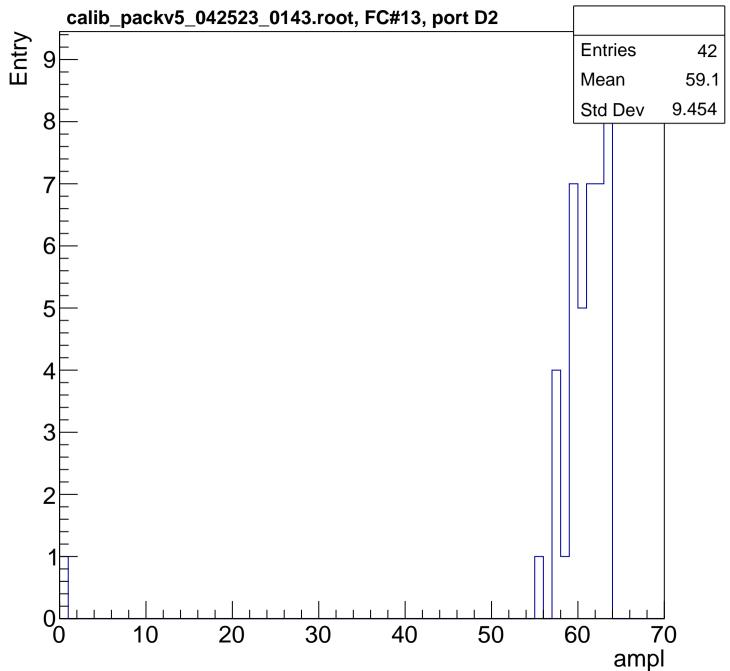


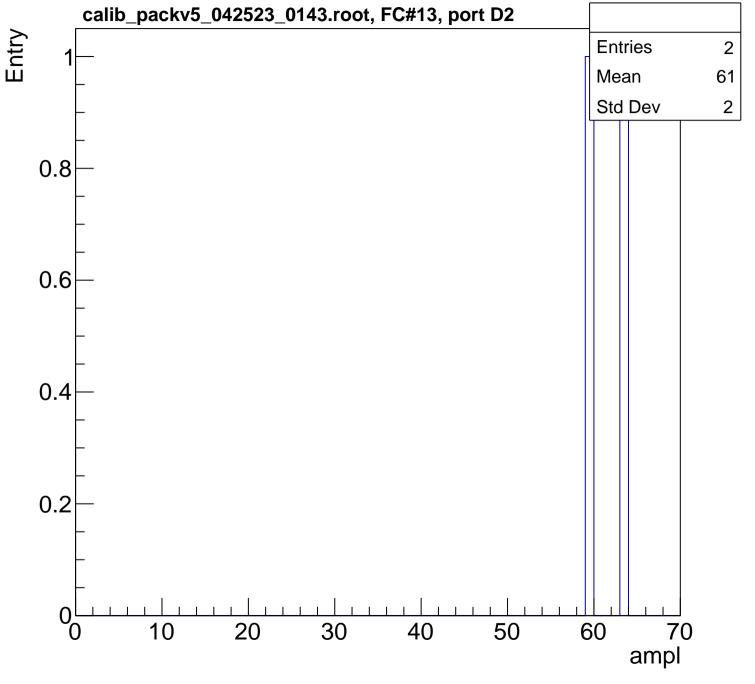




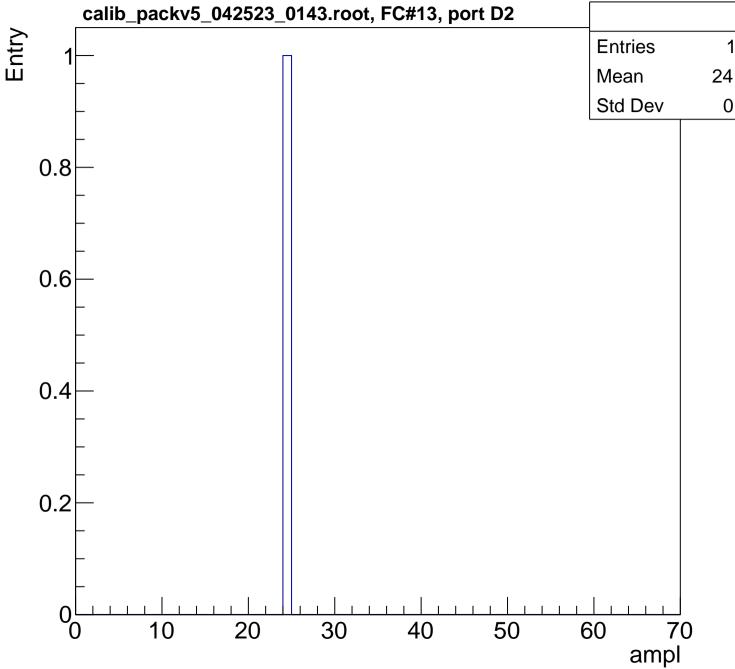


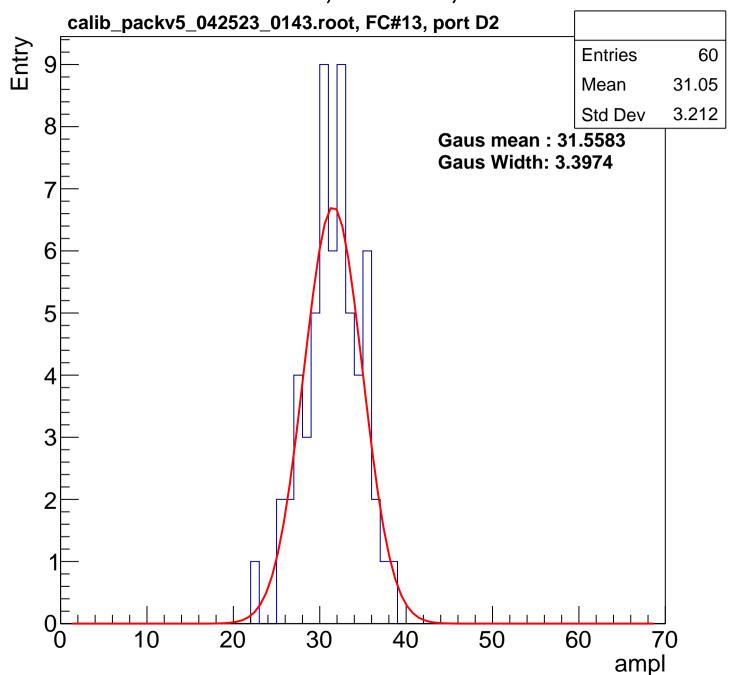


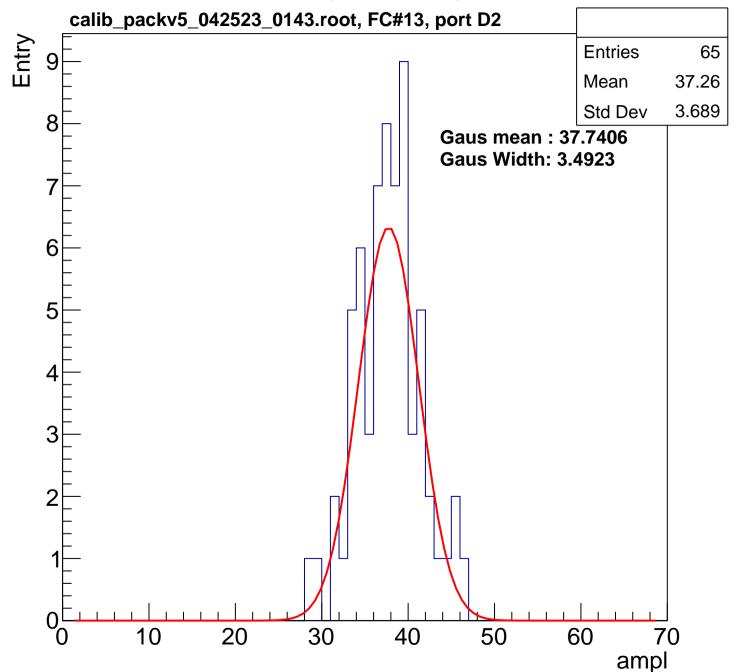


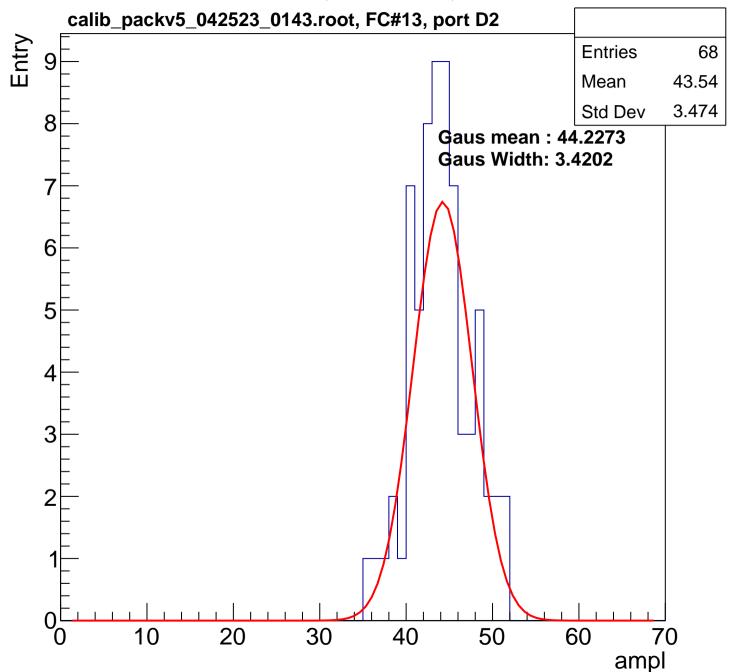


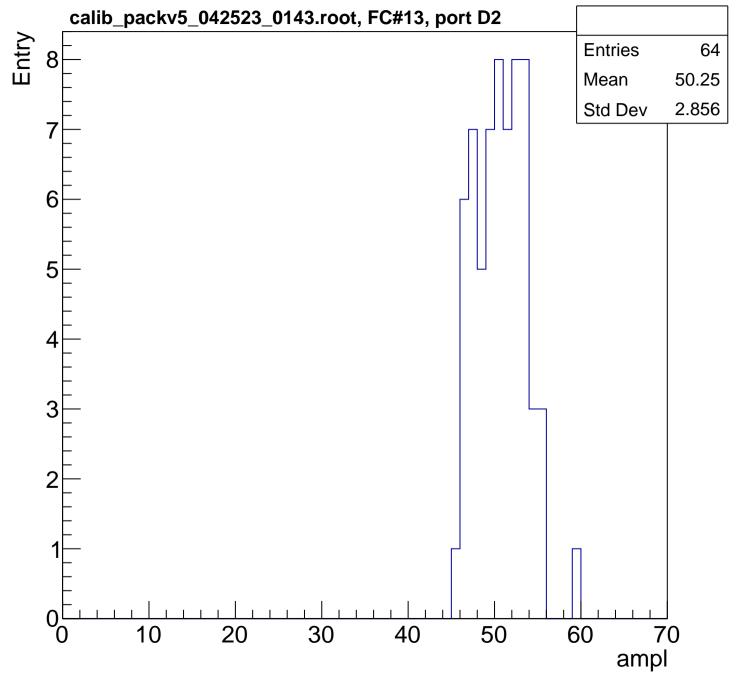
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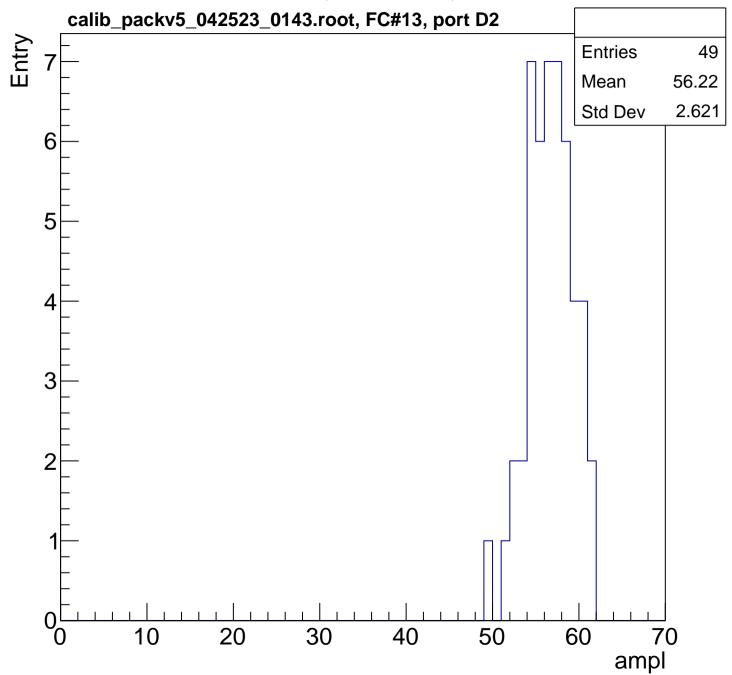


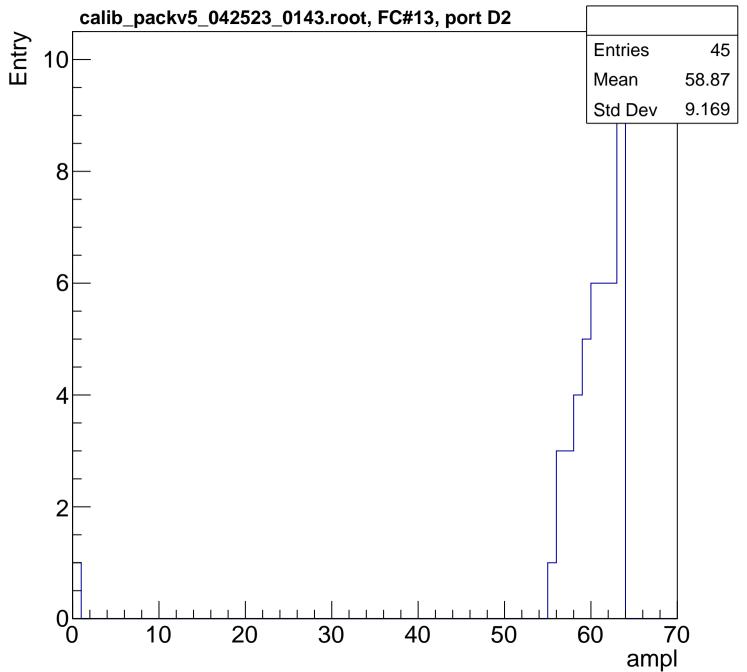


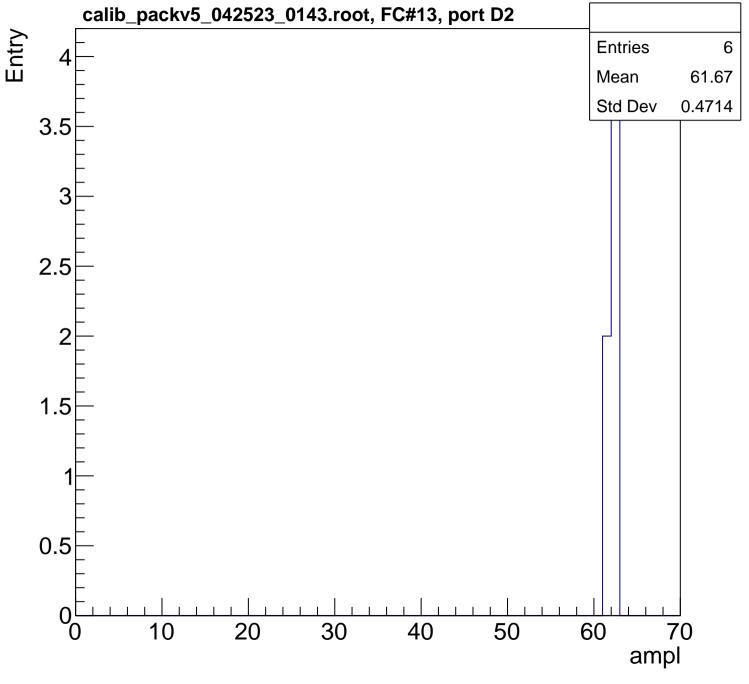


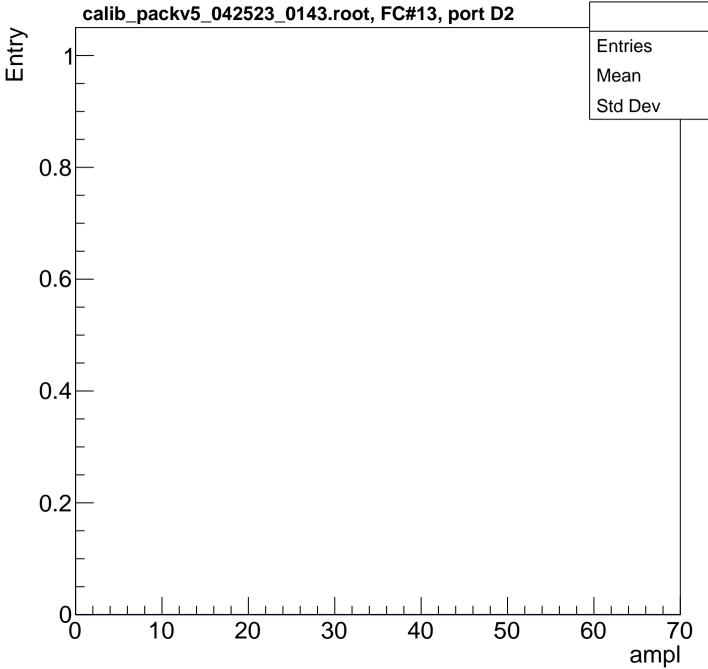


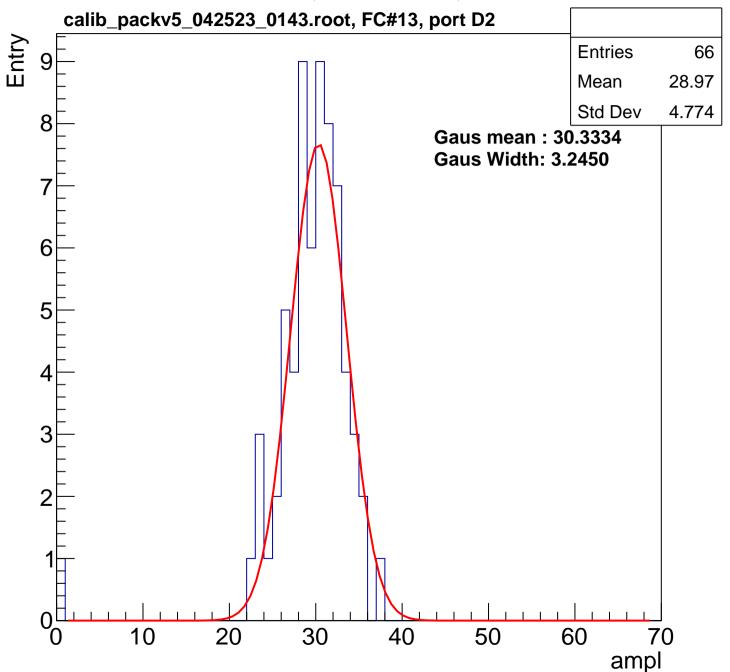


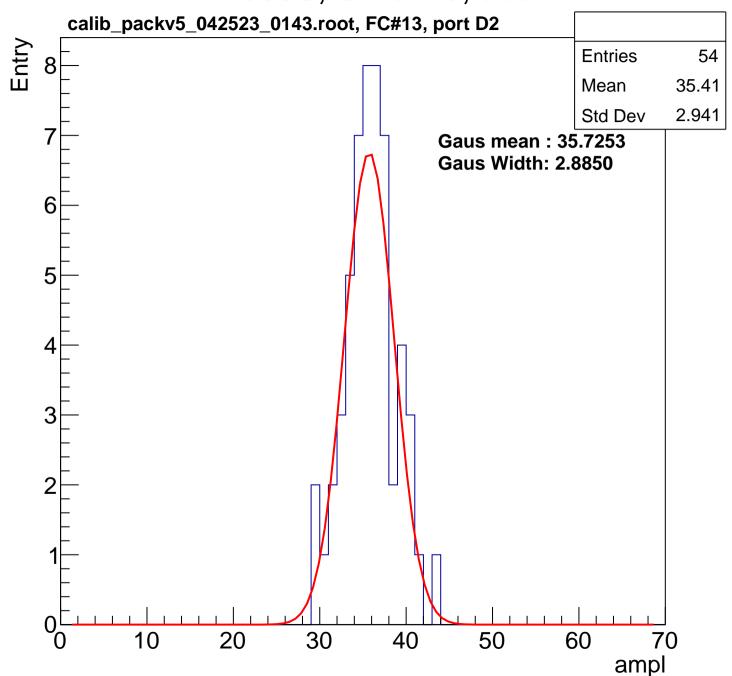


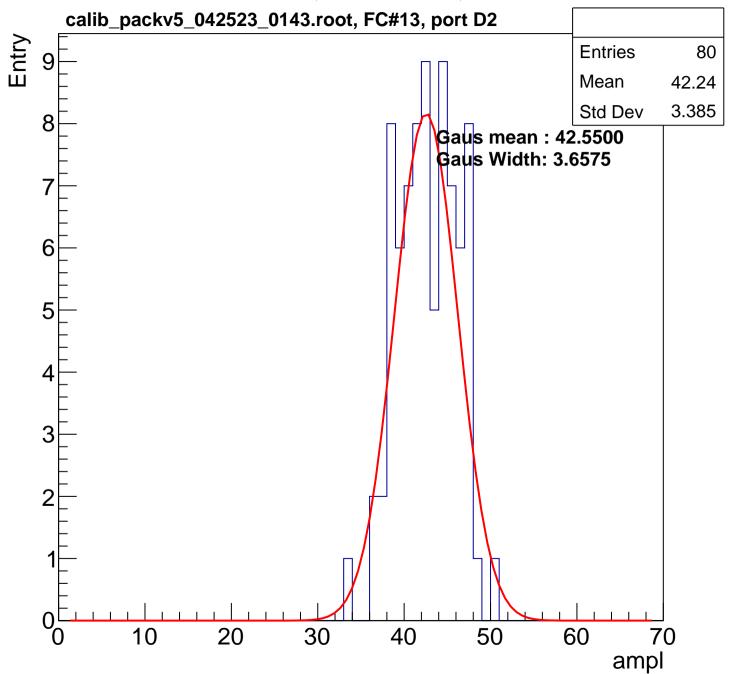


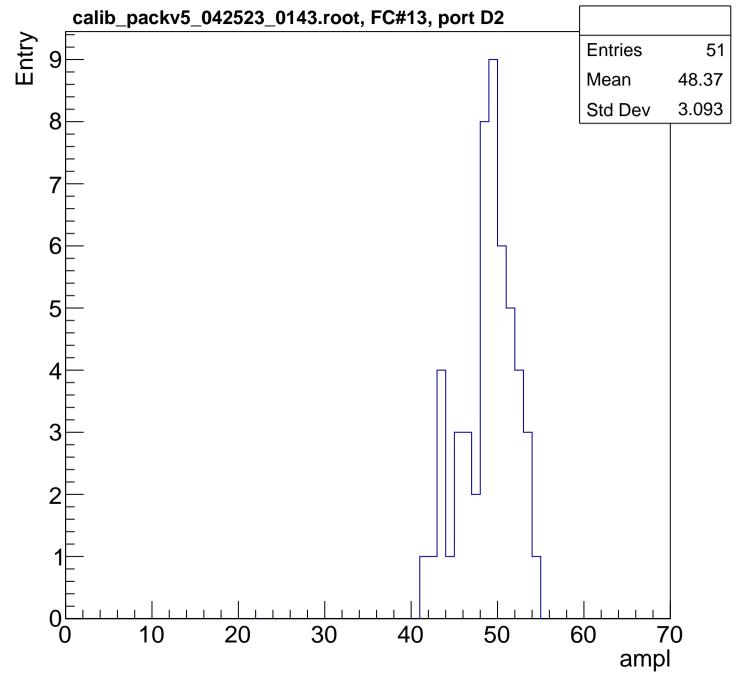


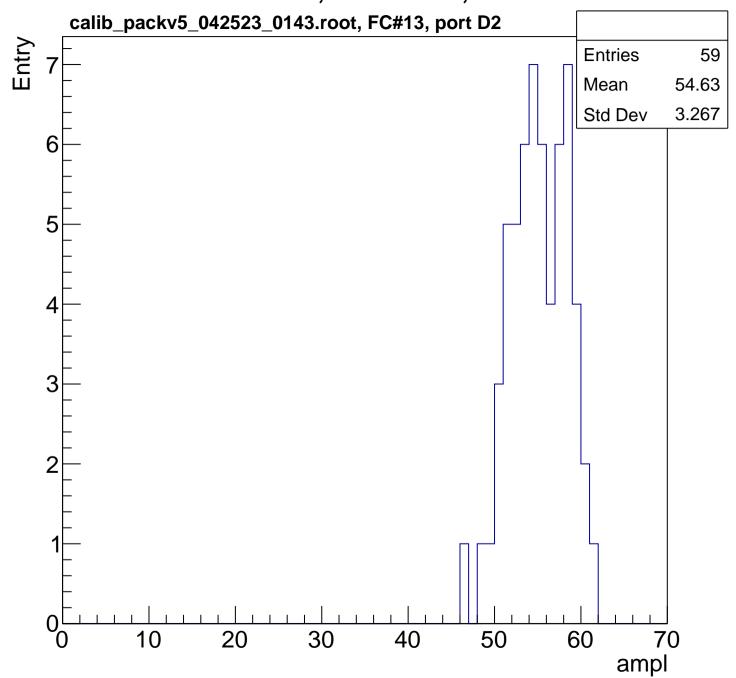


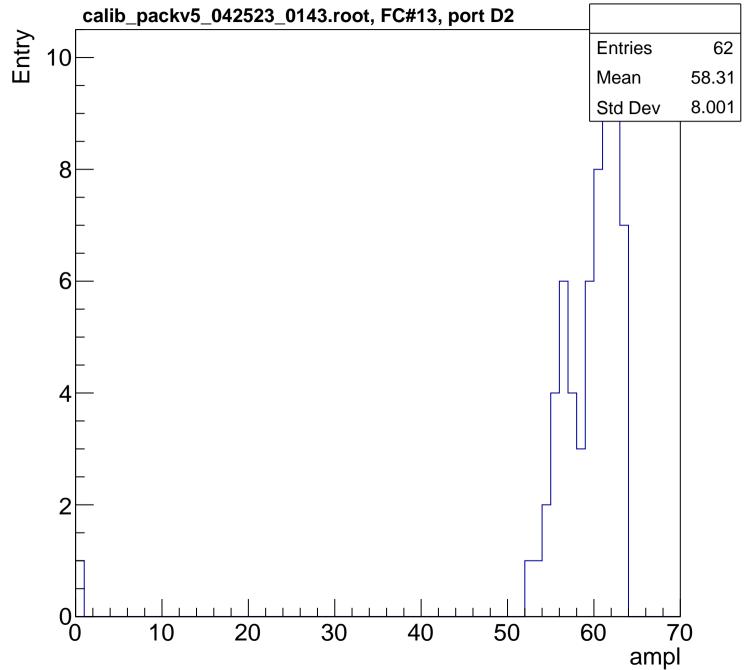


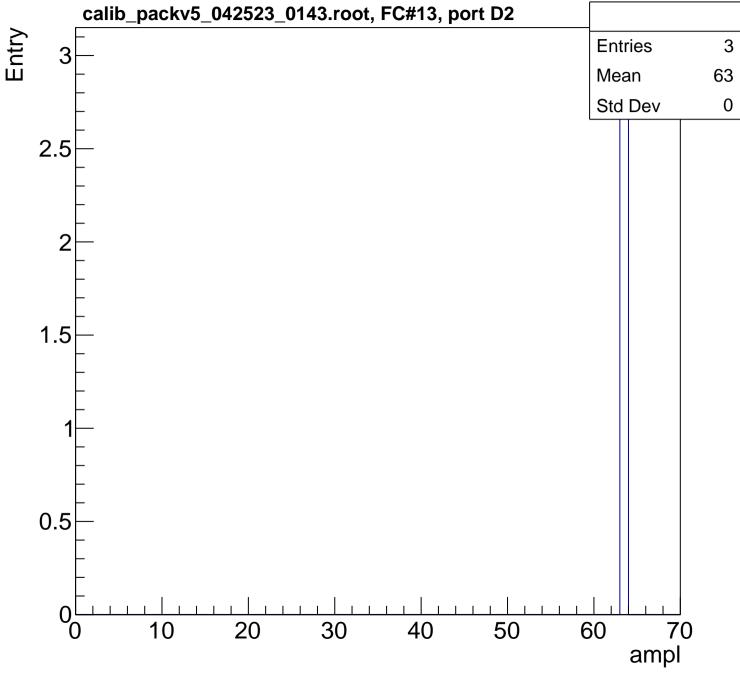




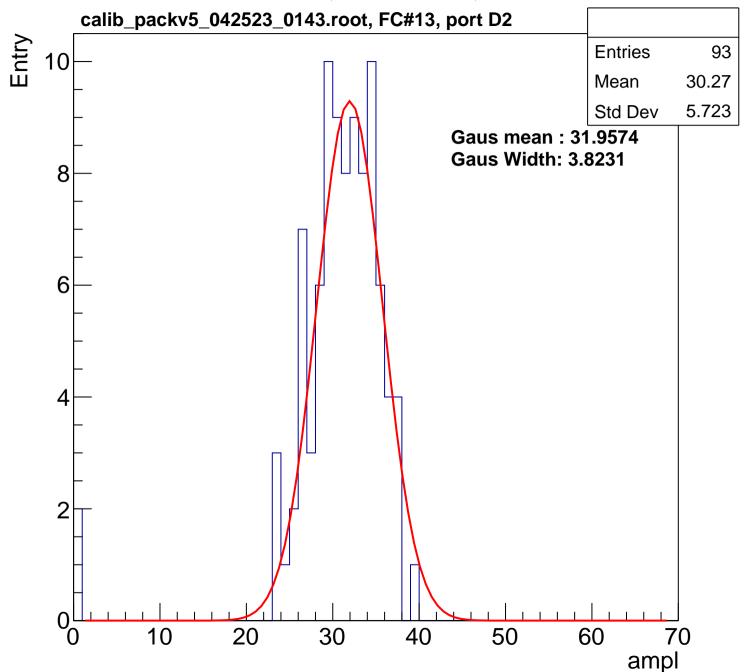


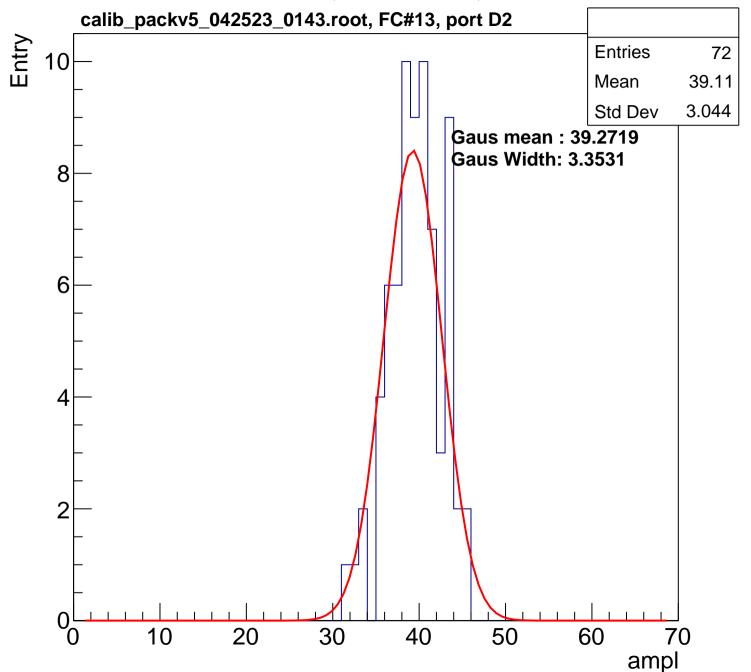


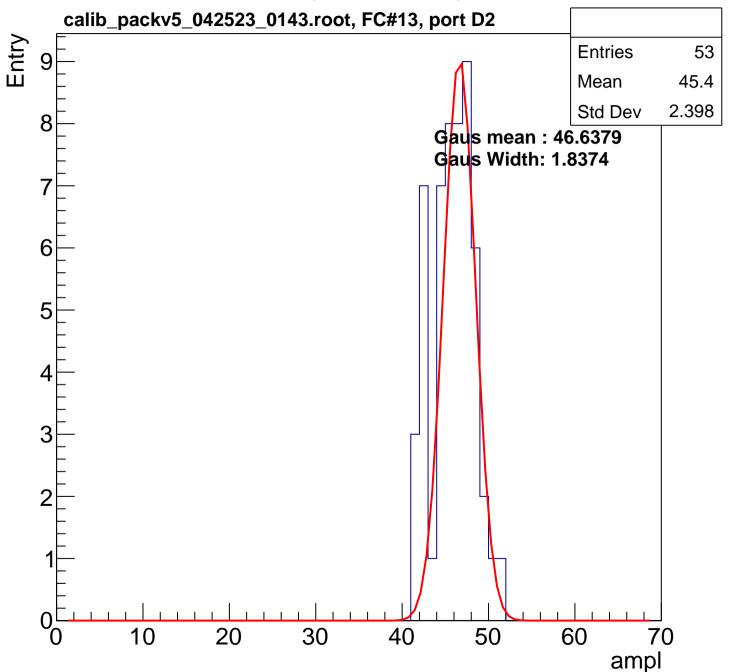


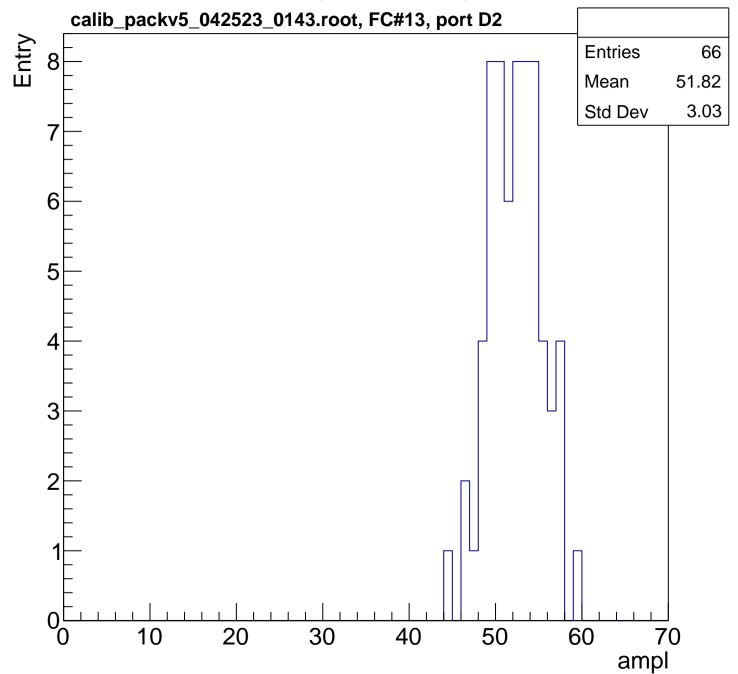


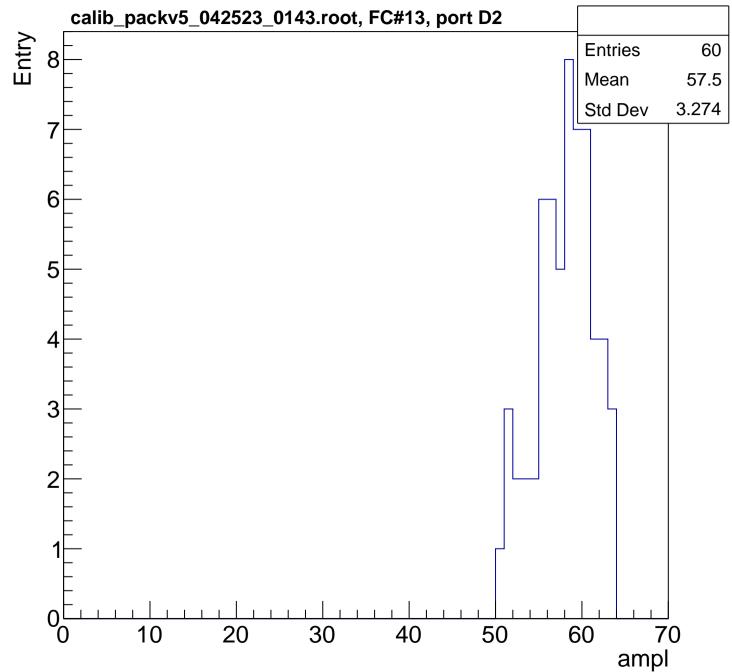


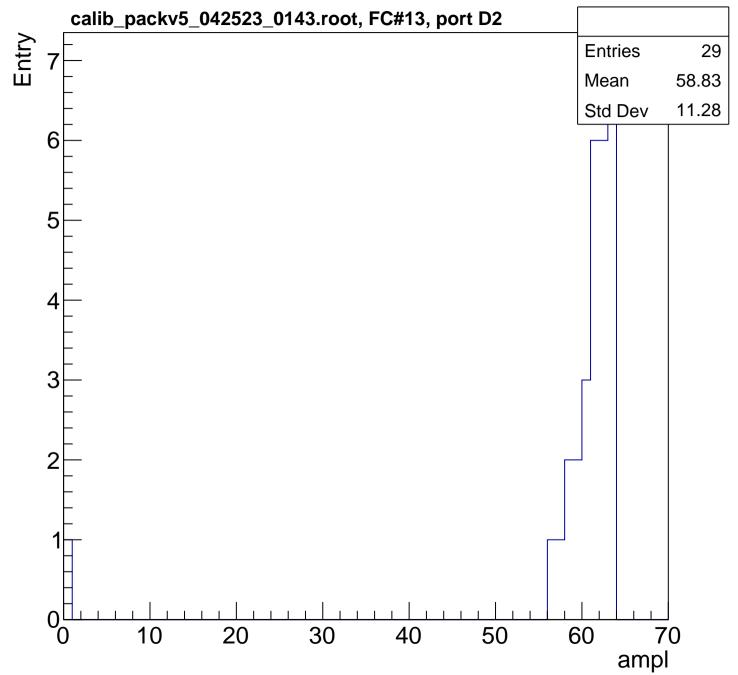


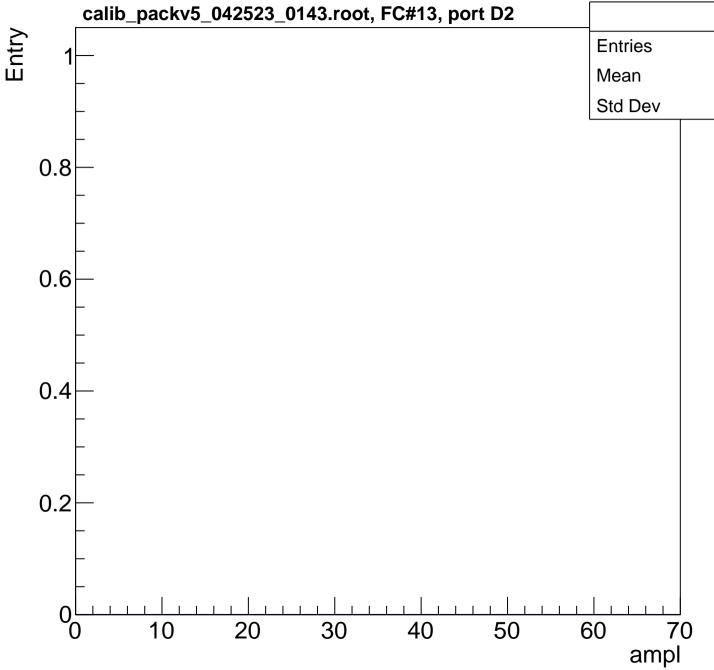


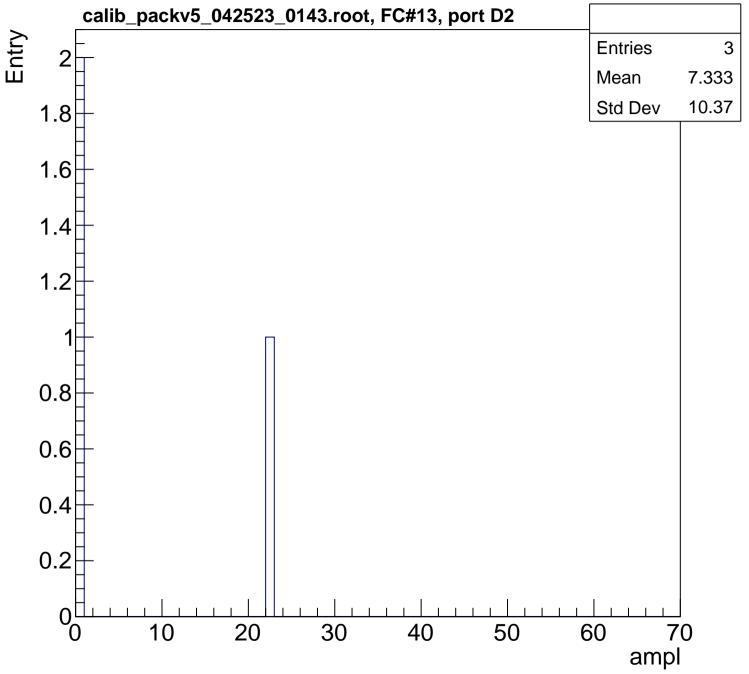


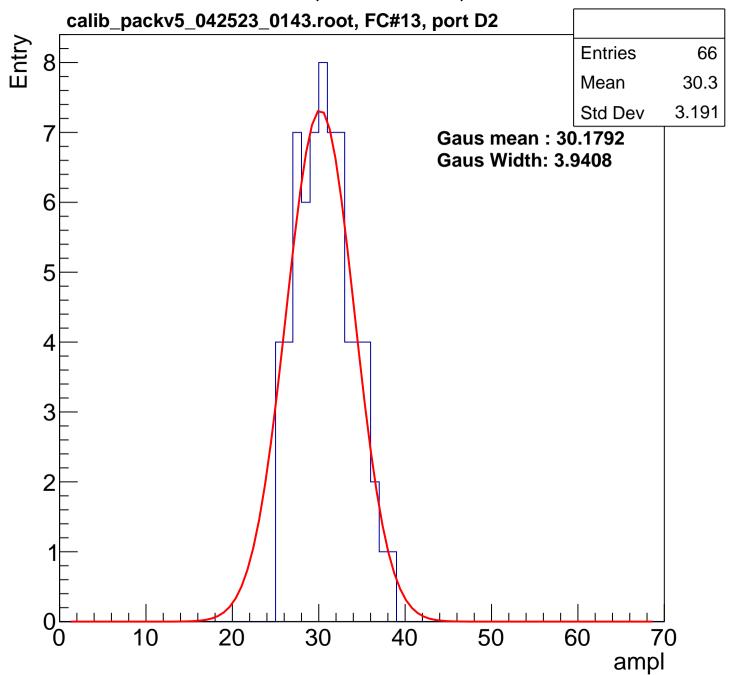


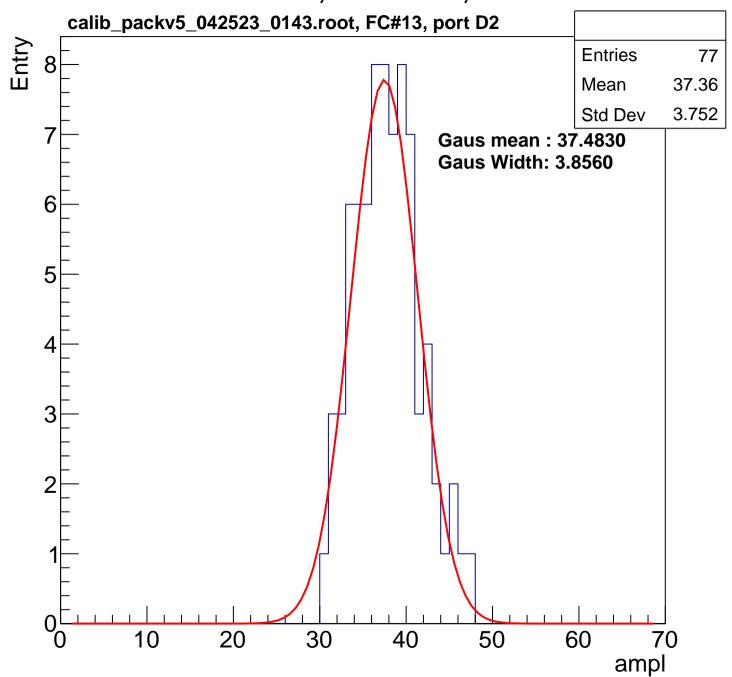


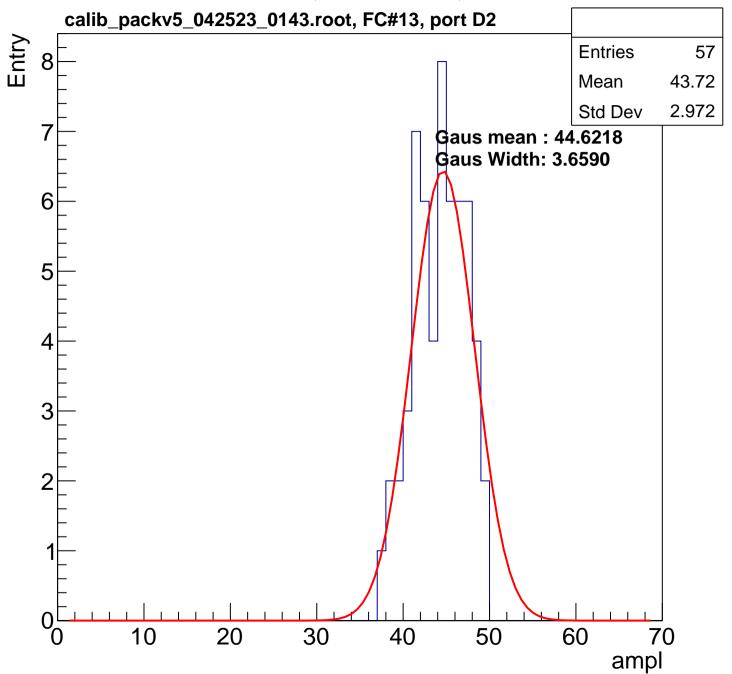


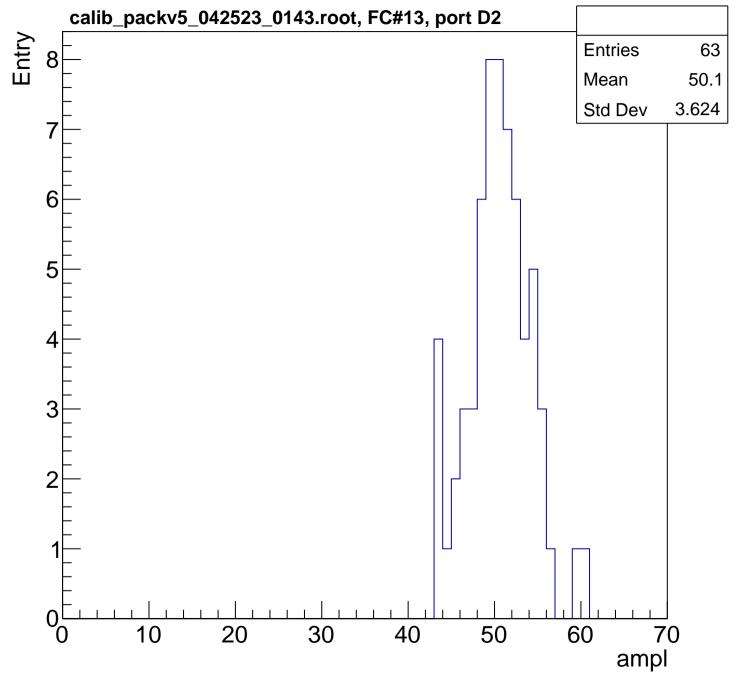


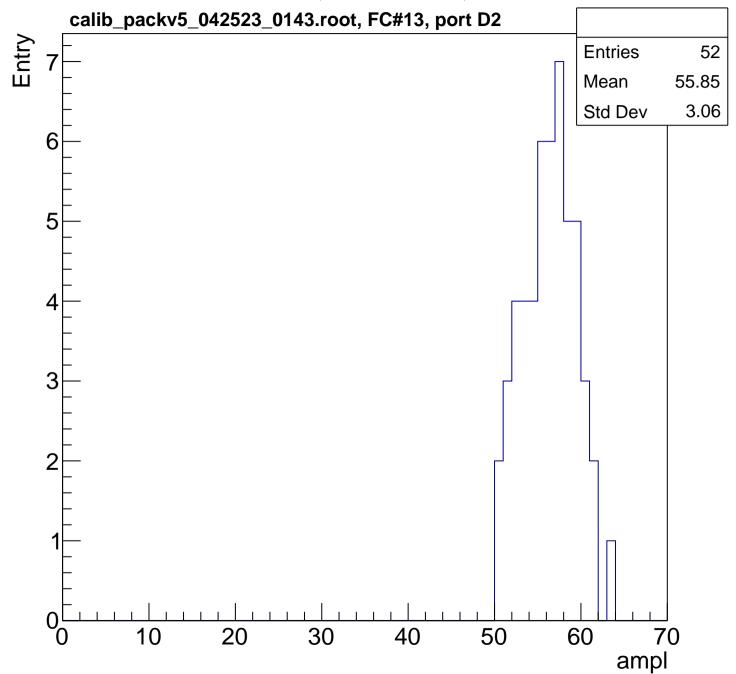


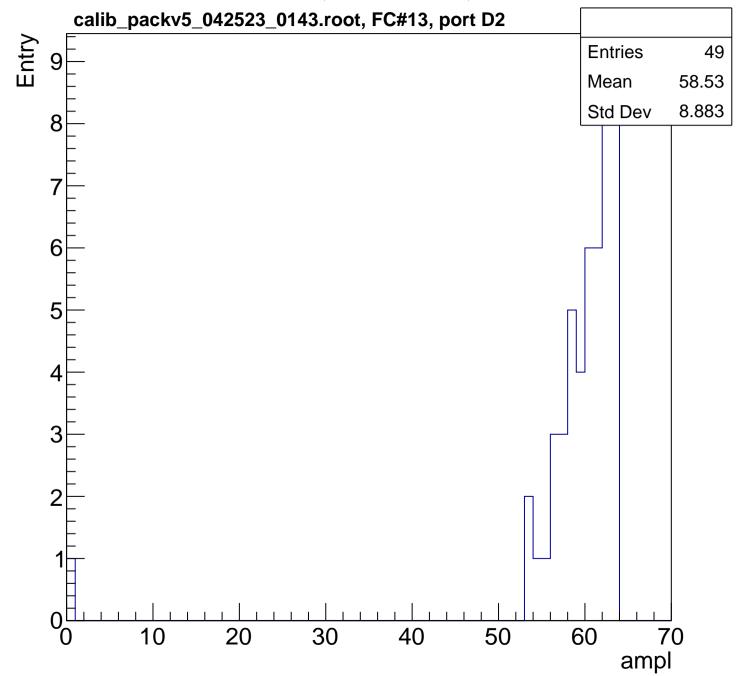


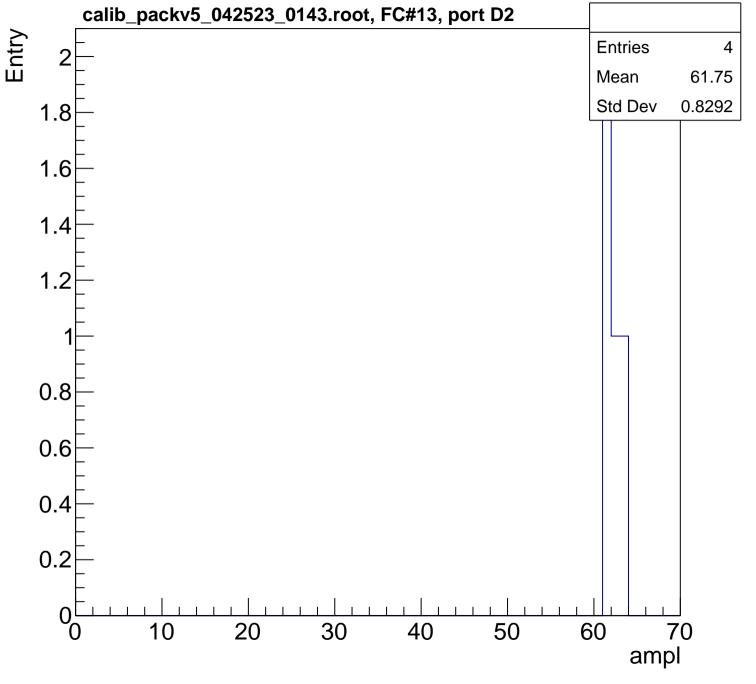




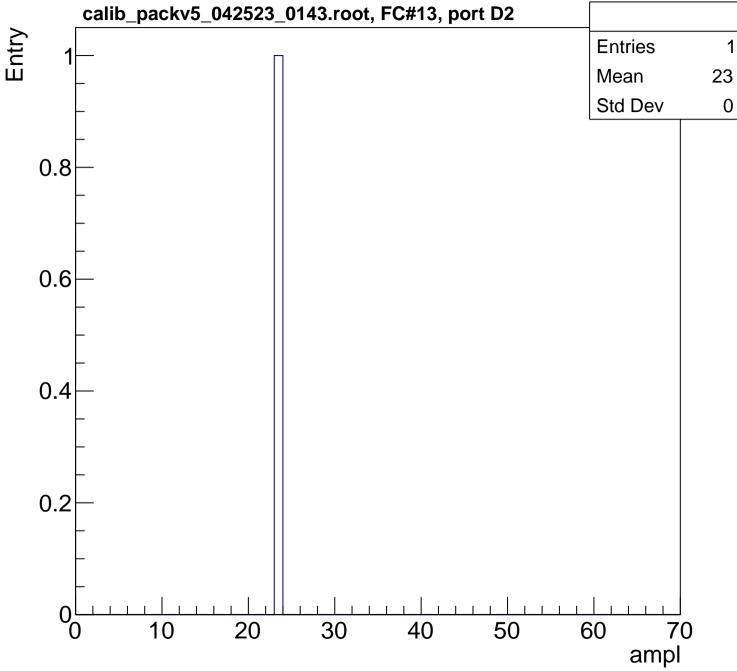


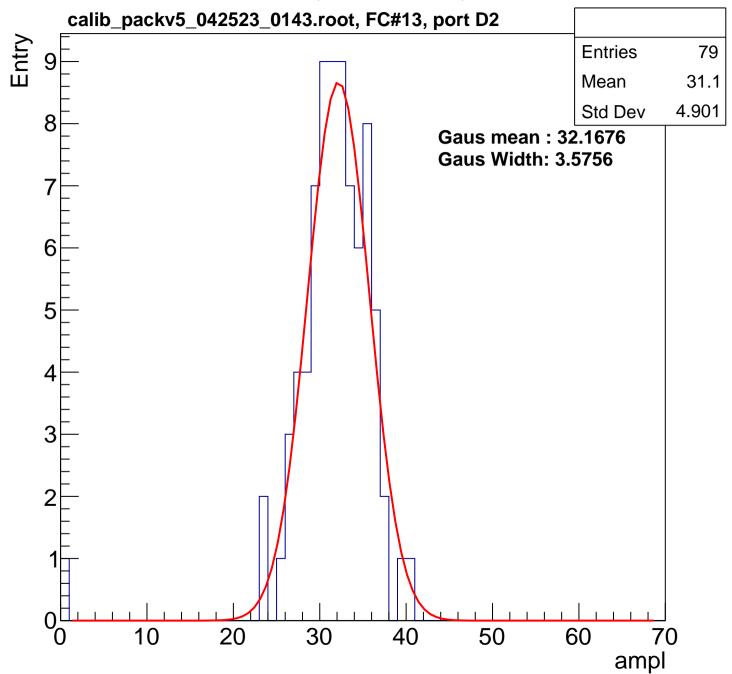


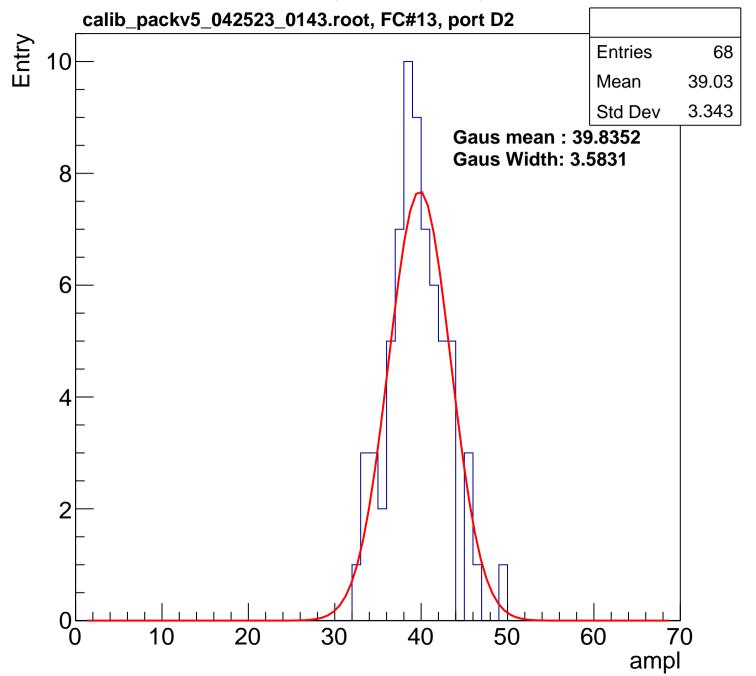


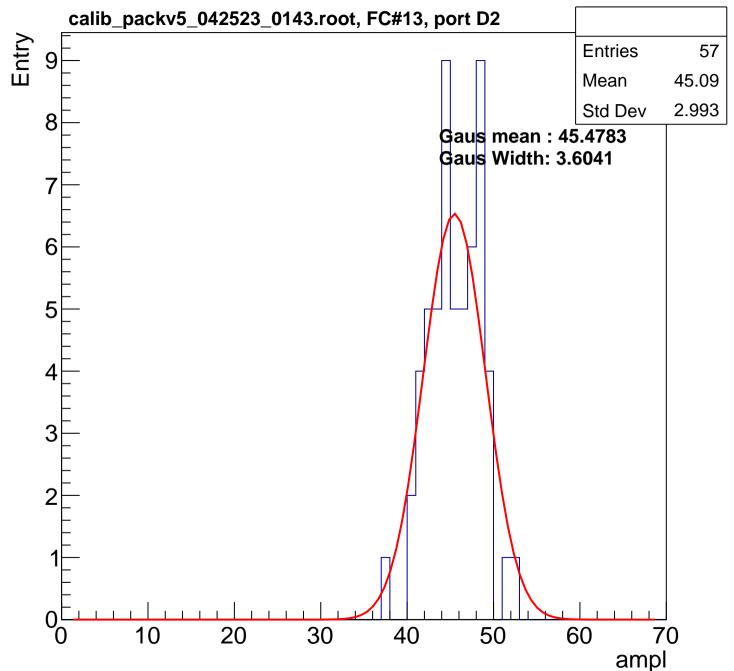


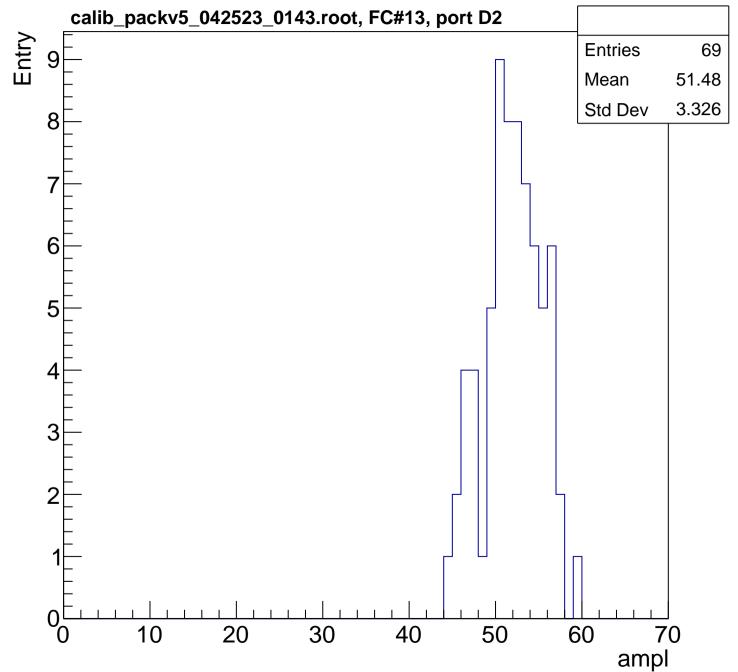
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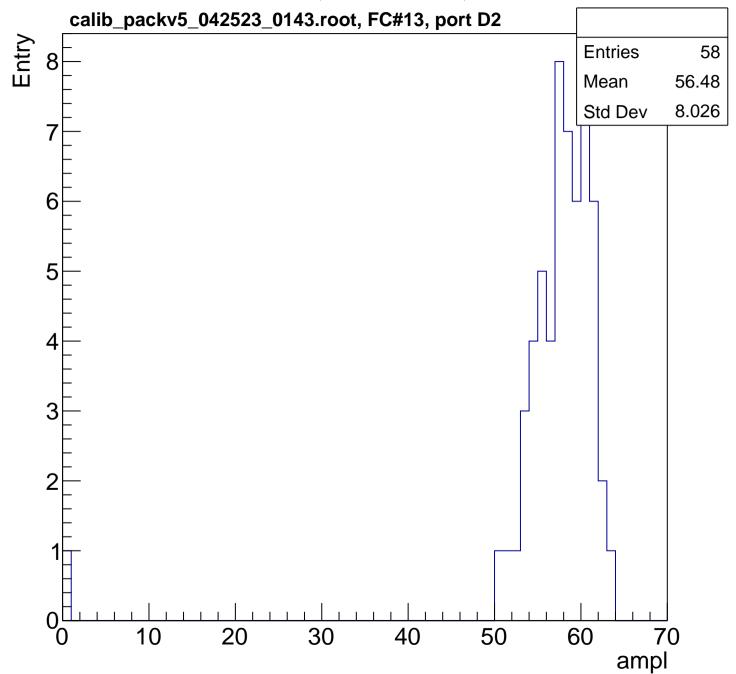


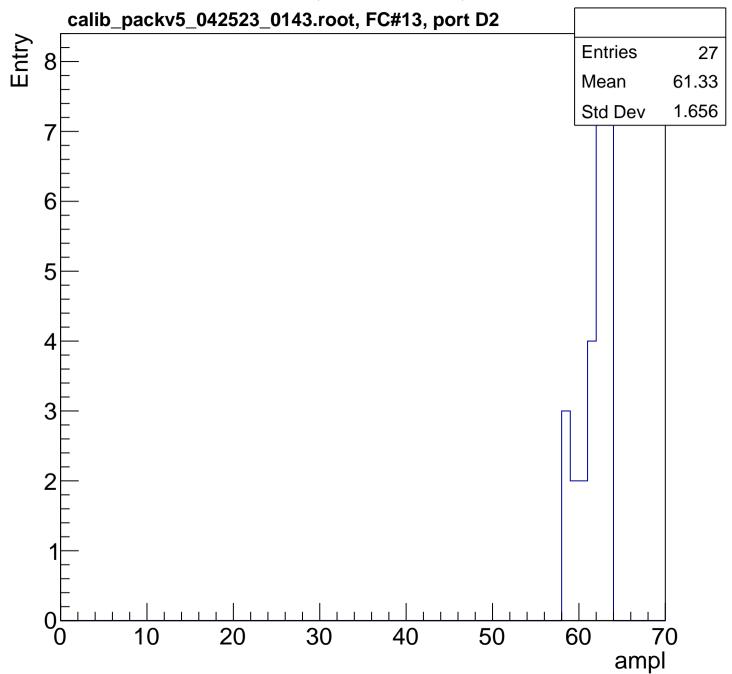


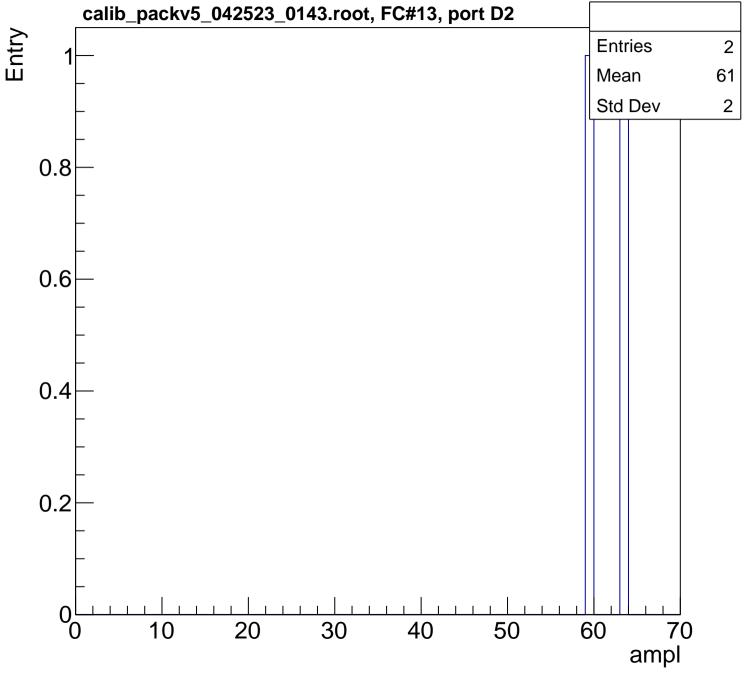




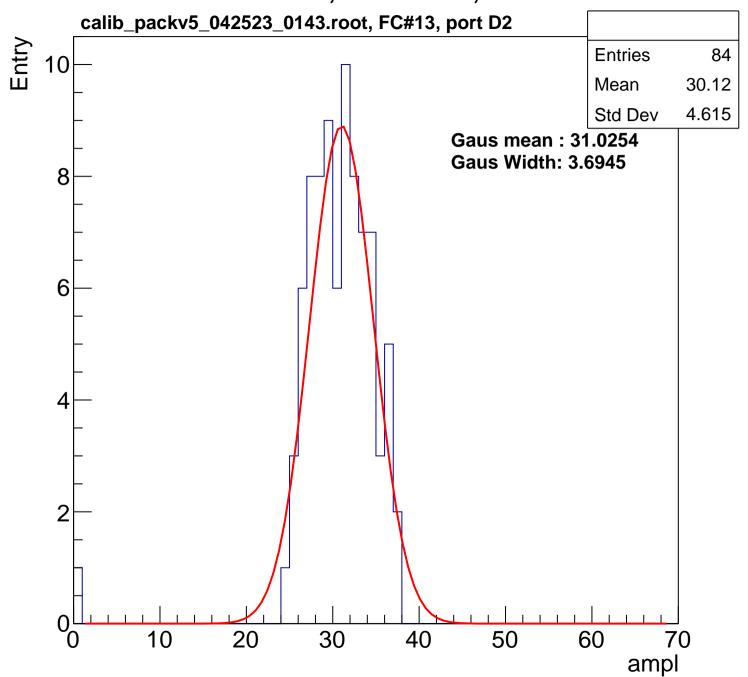


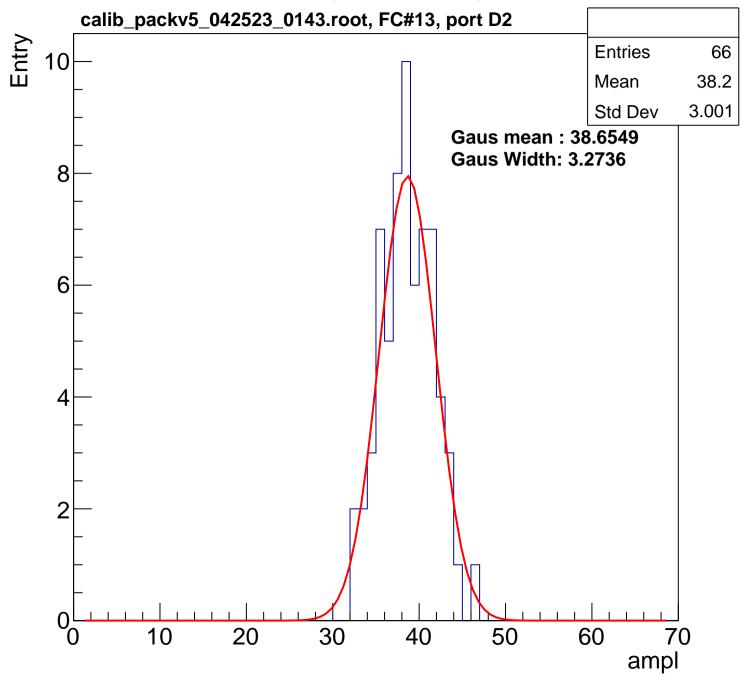


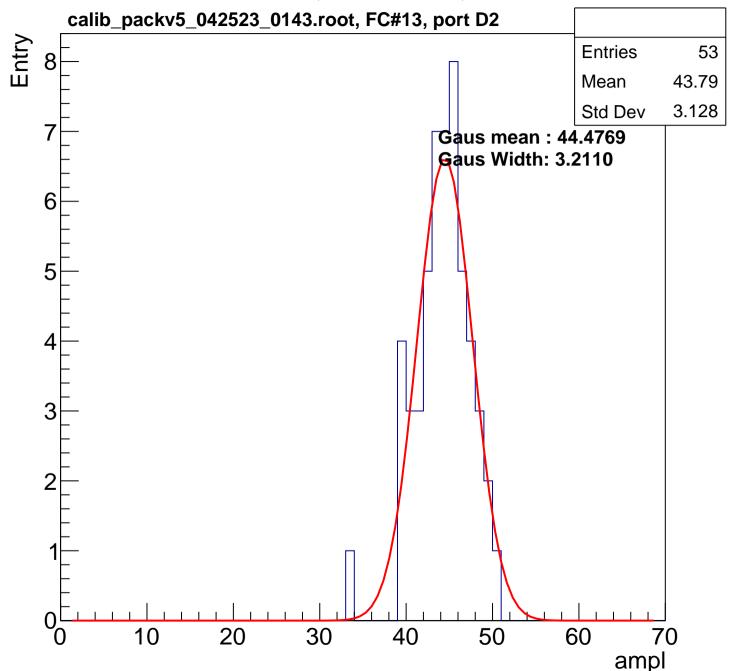


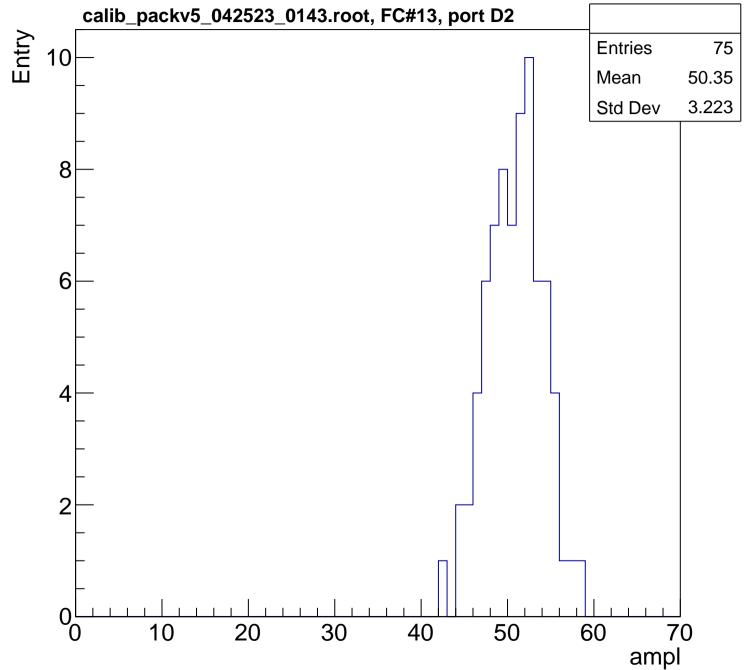


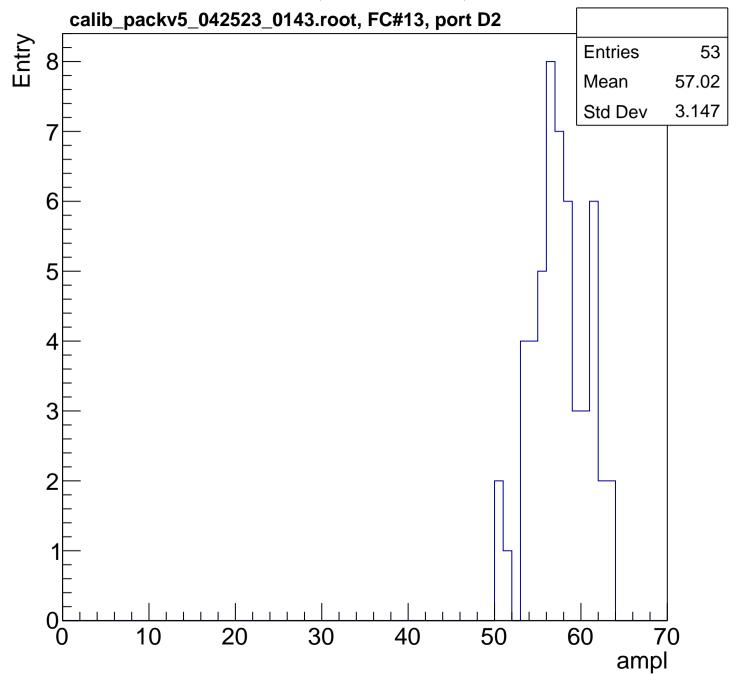
B1L003S, U7-ch13, adc7 calib_packv5_042523_0143.root, FC#13, port D2 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

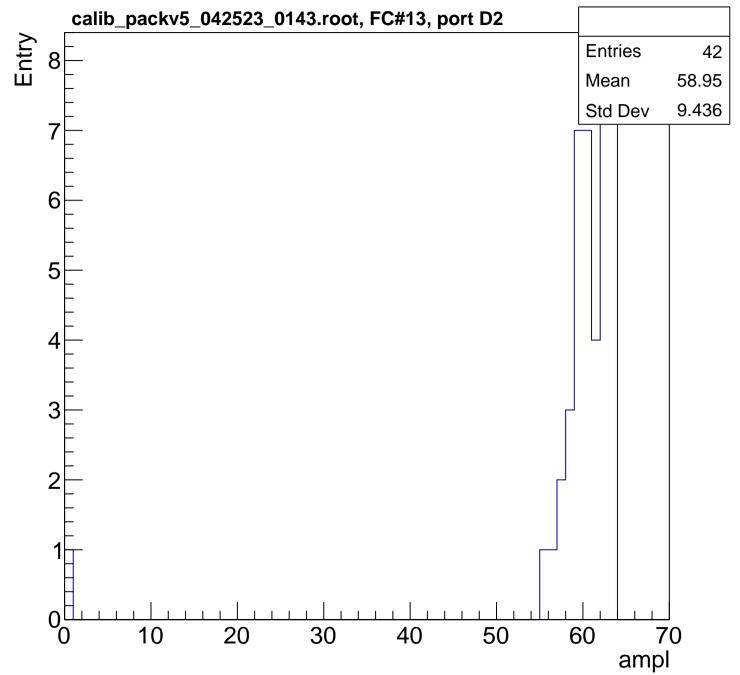


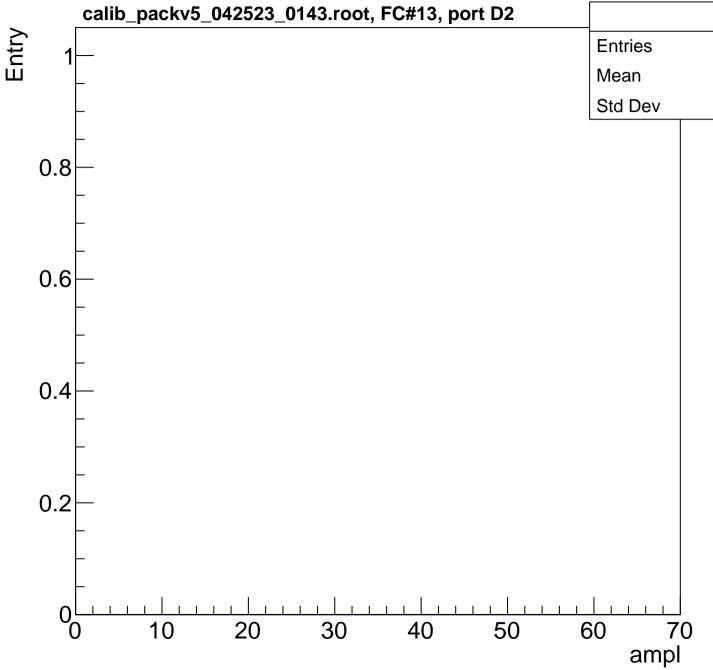




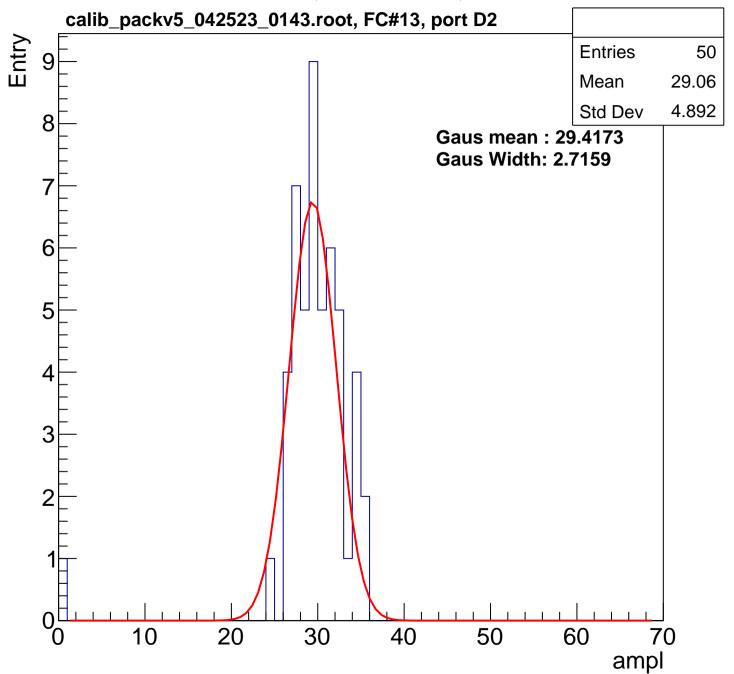


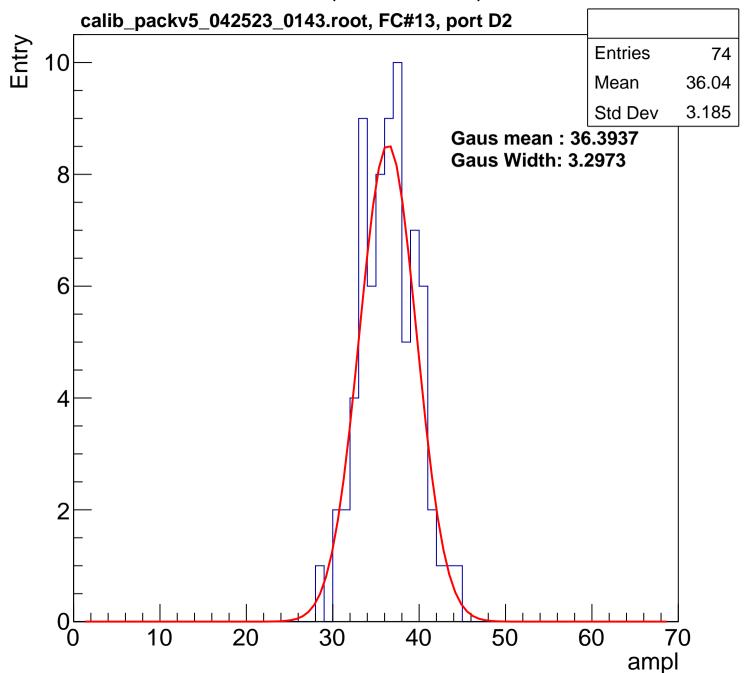


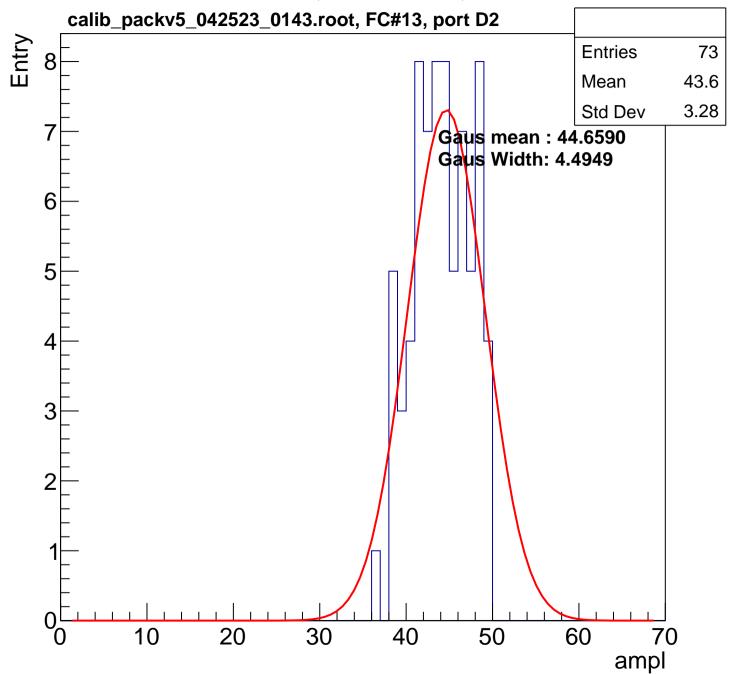


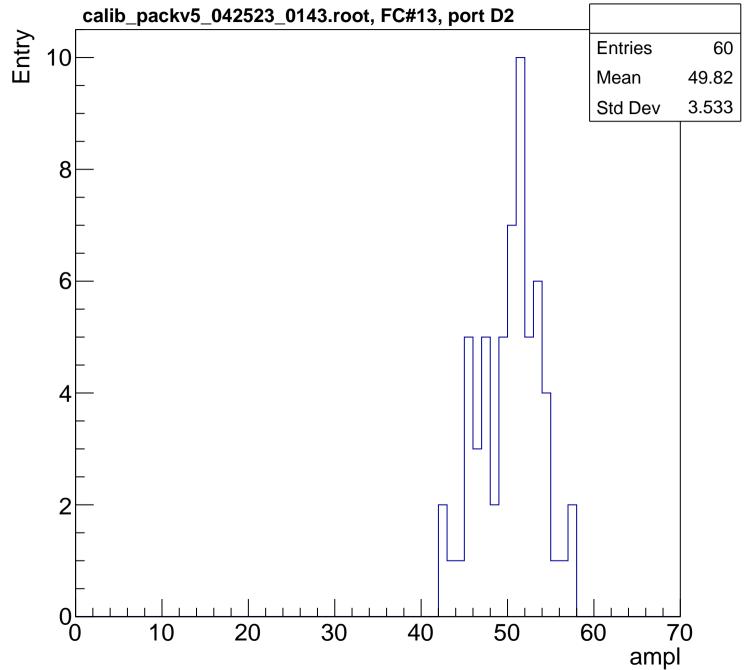


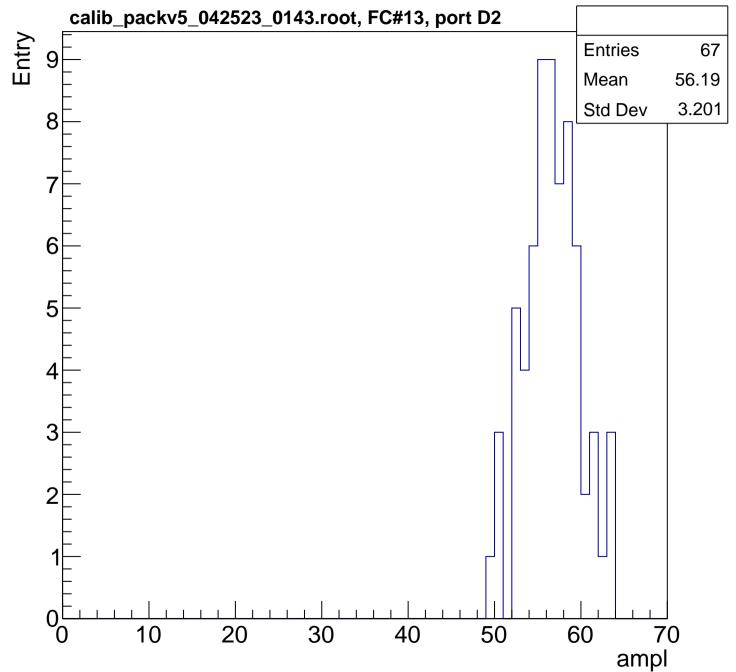


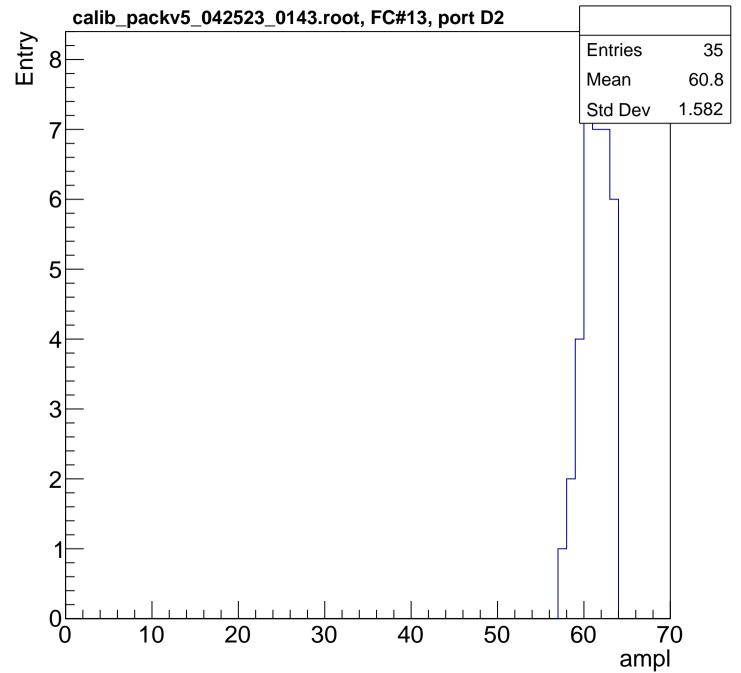


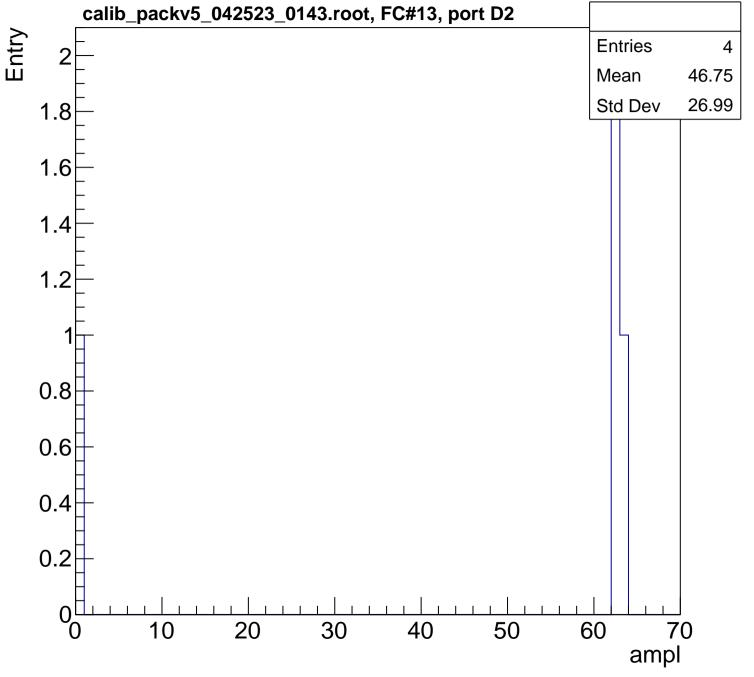




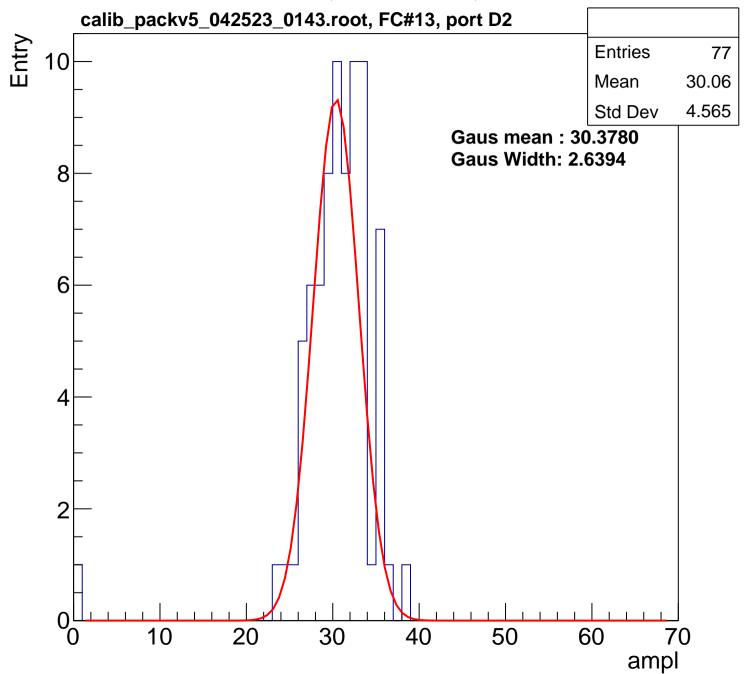


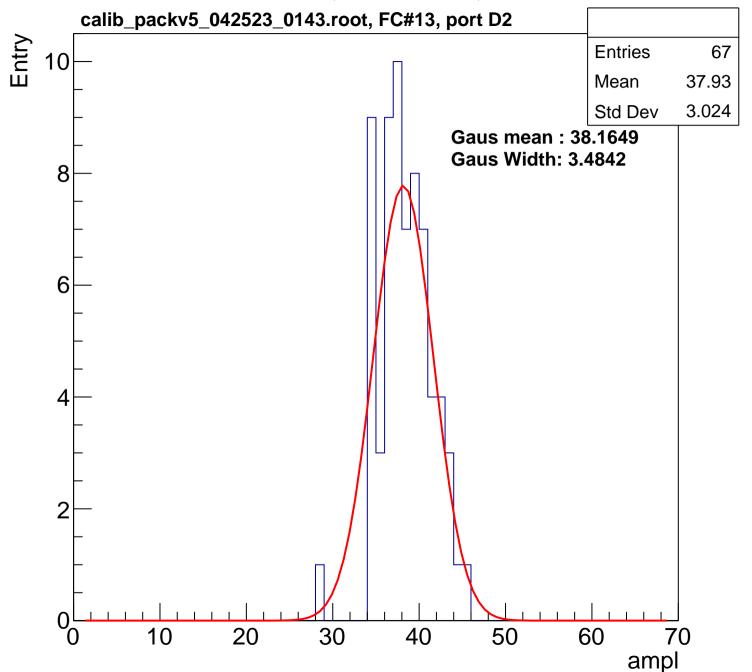


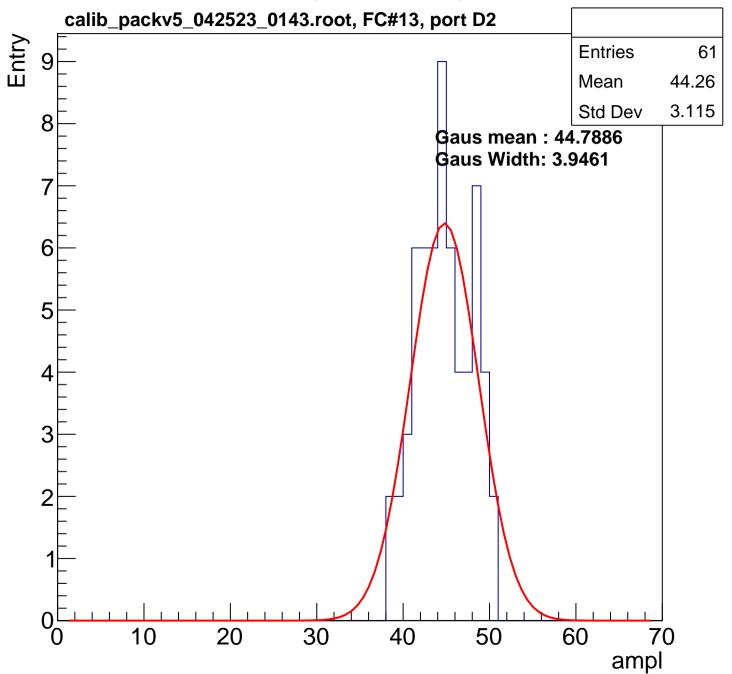


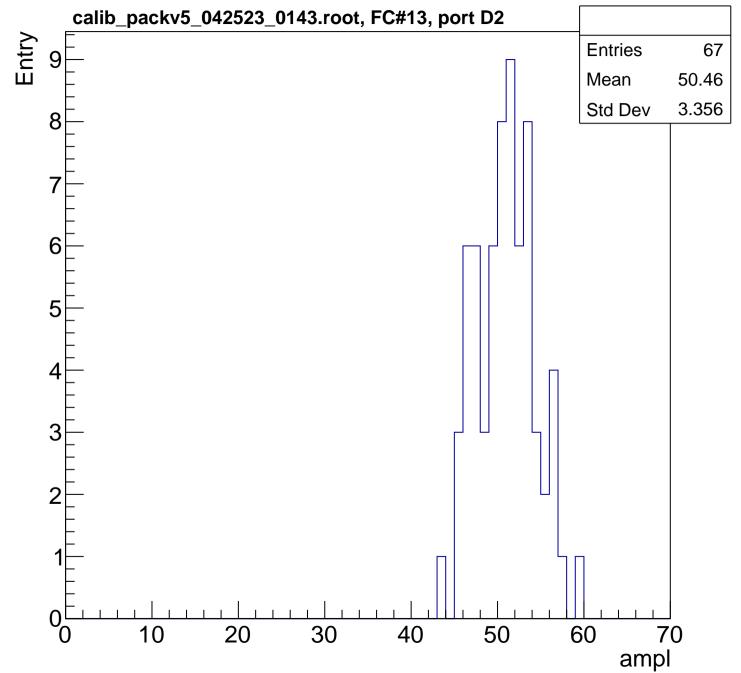


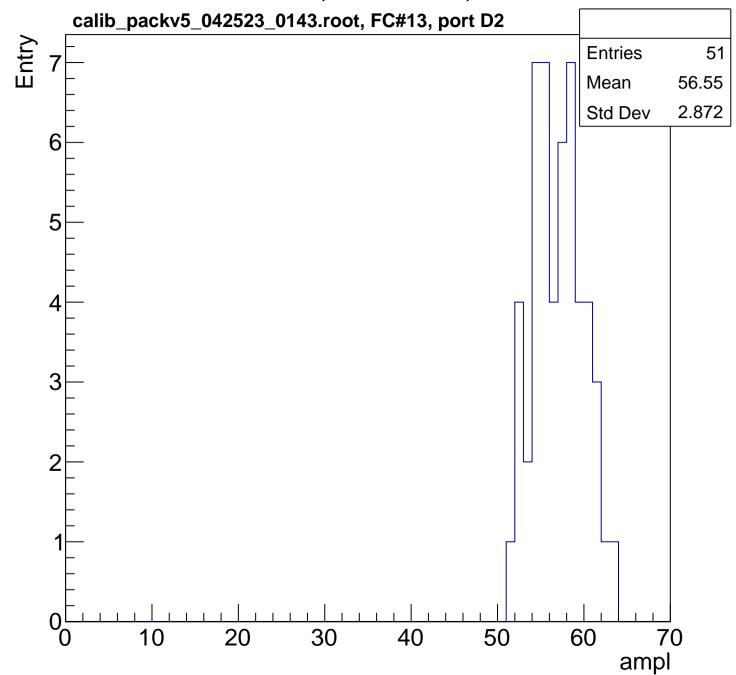
B1L003S, U7-ch15, adc7 calib_packv5_042523_0143.root, FC#13, port D2 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

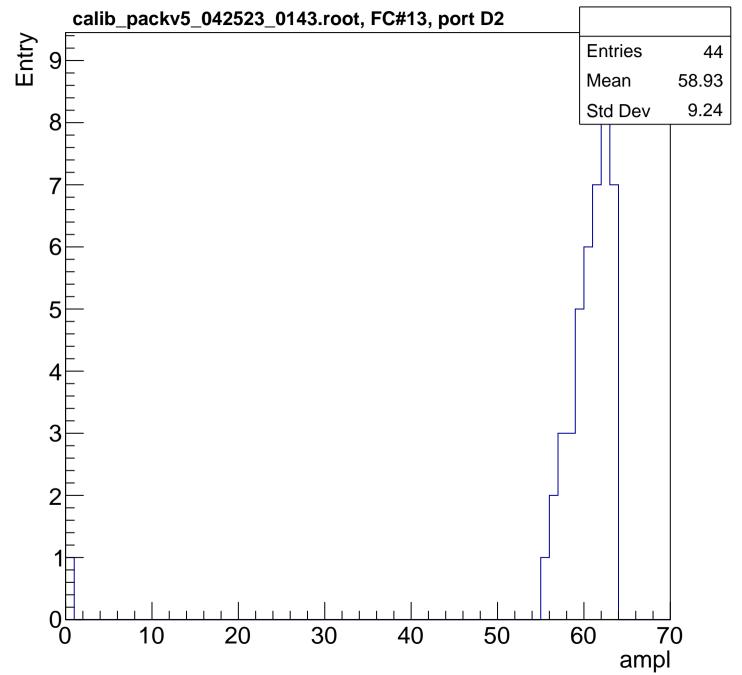


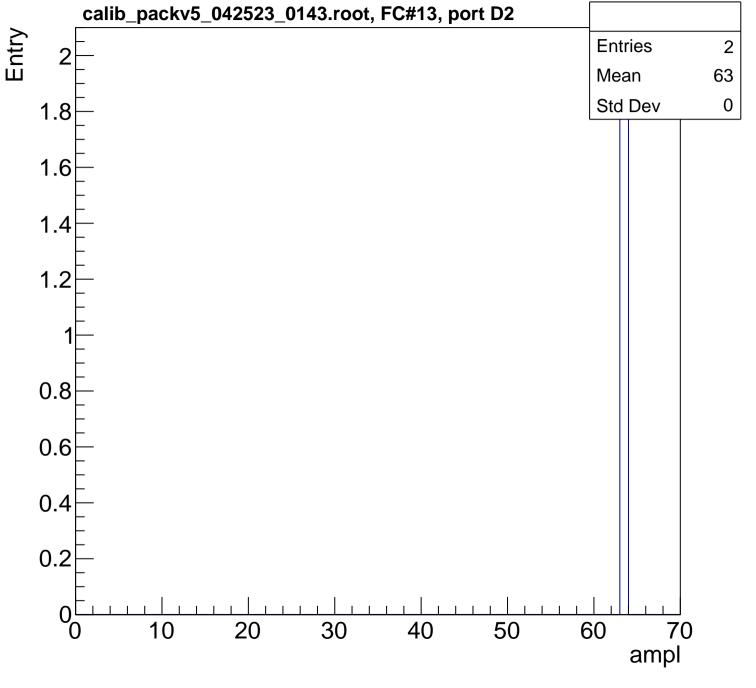




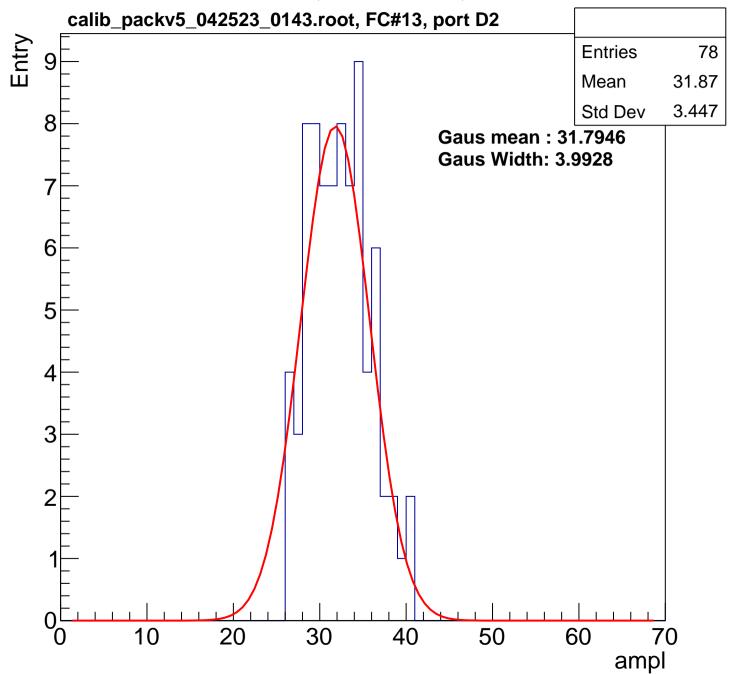


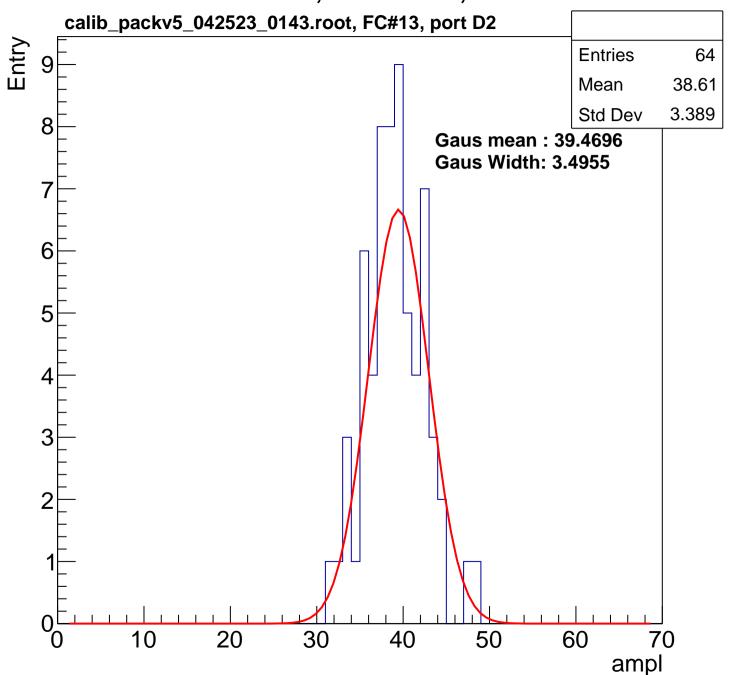


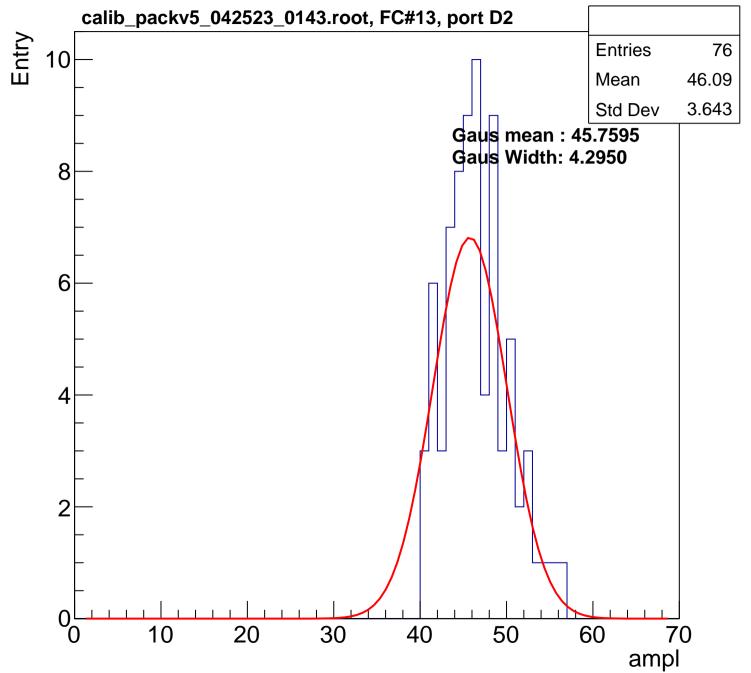


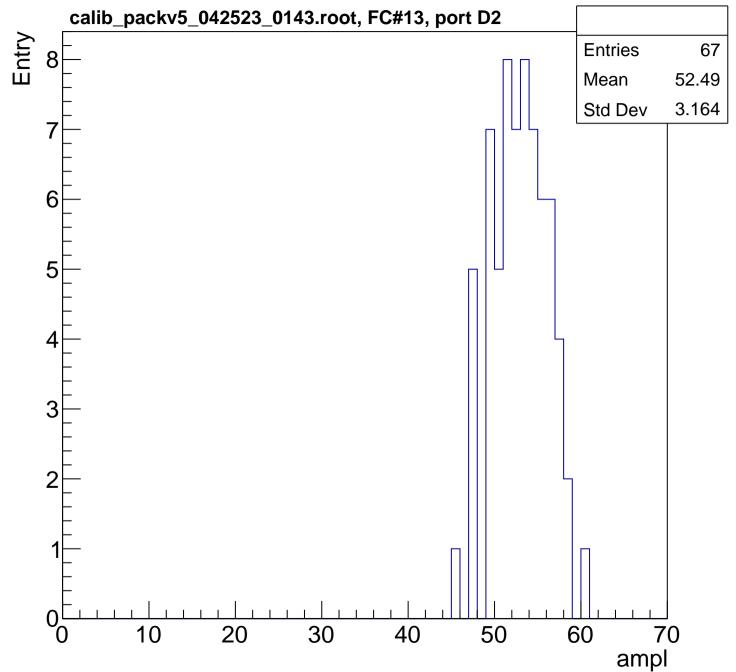


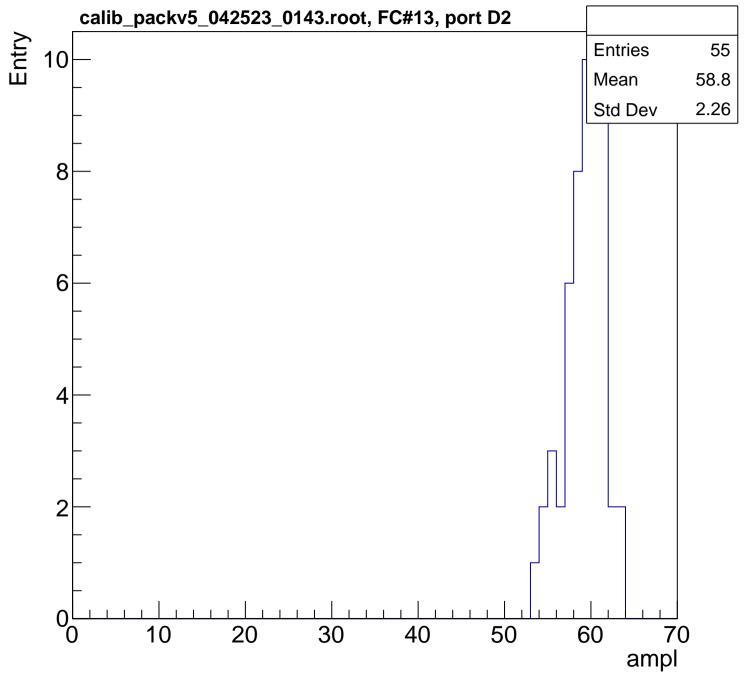
B1L003S, U7-ch16, adc7 calib_packv5_042523_0143.root, FC#13, port D2 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

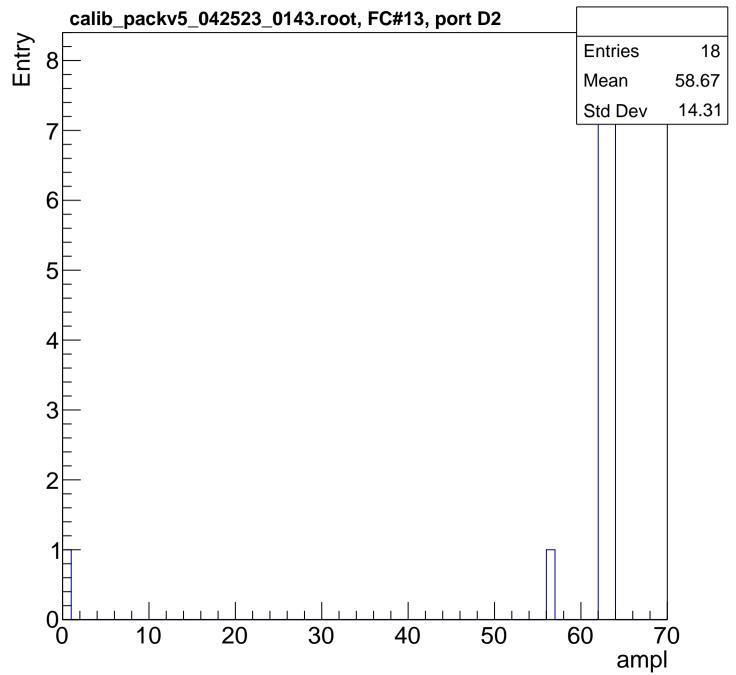


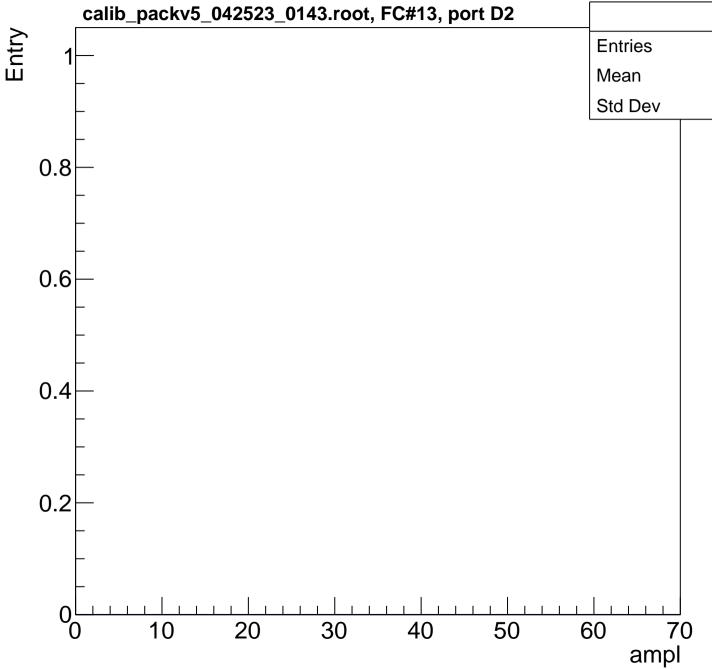




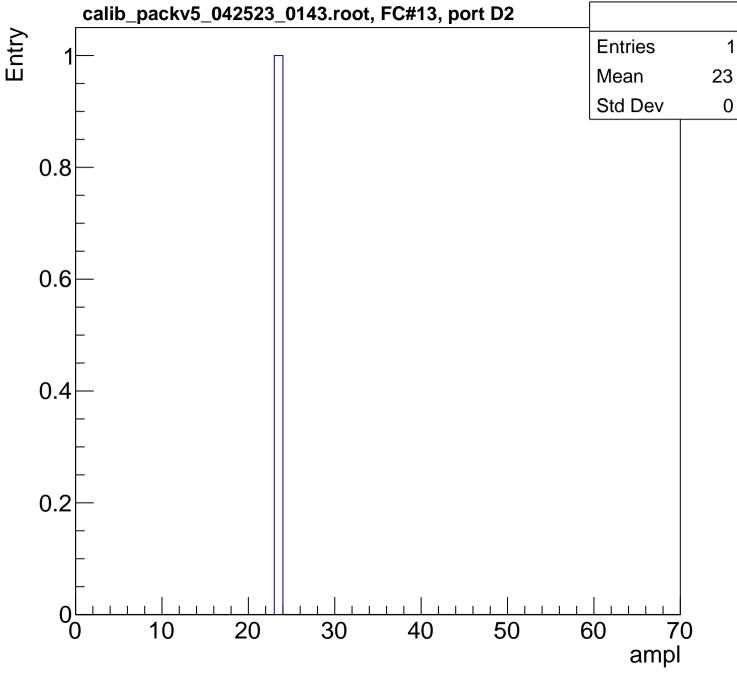


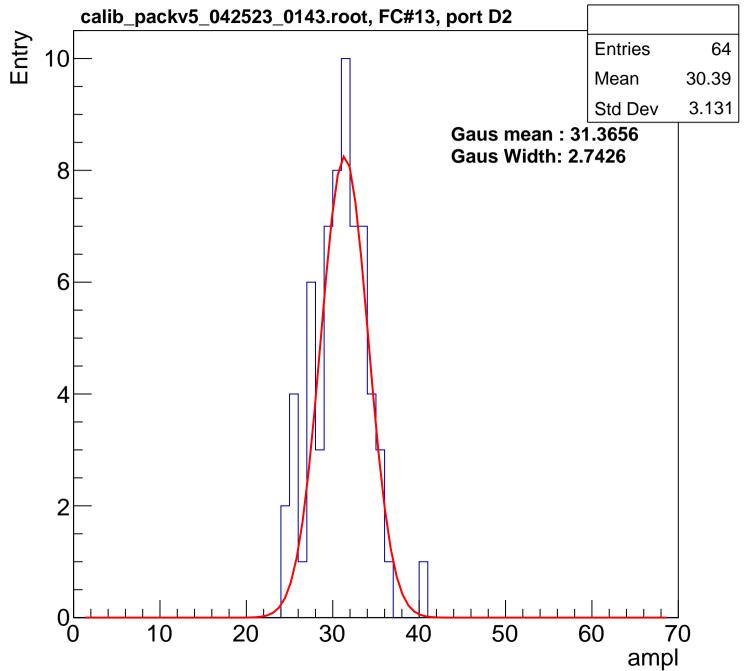


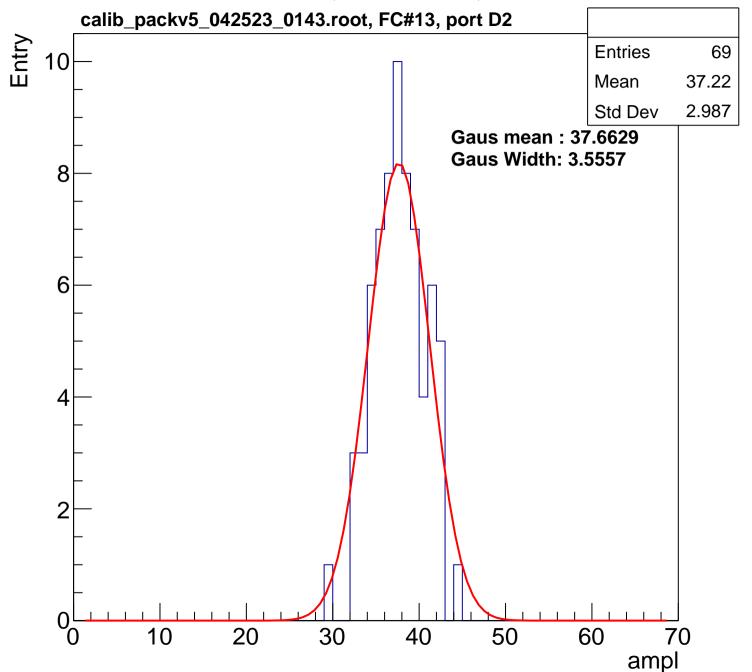


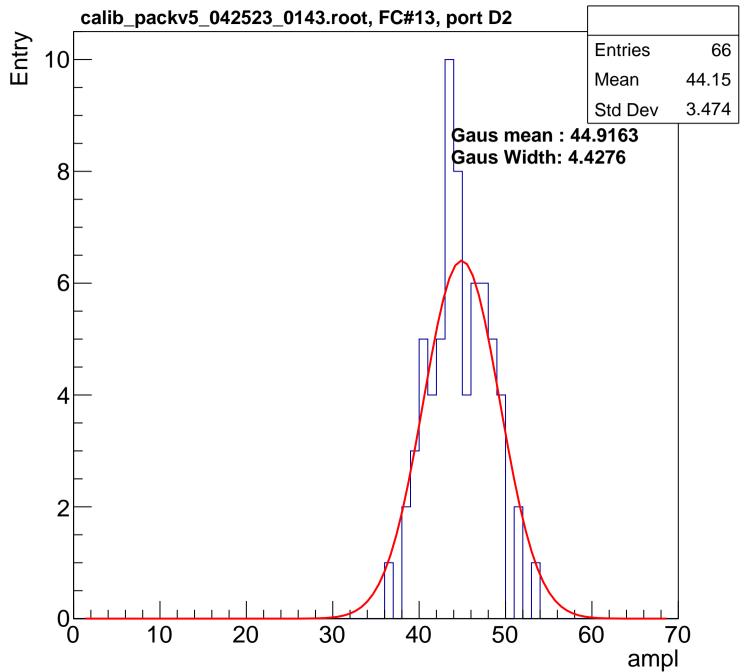


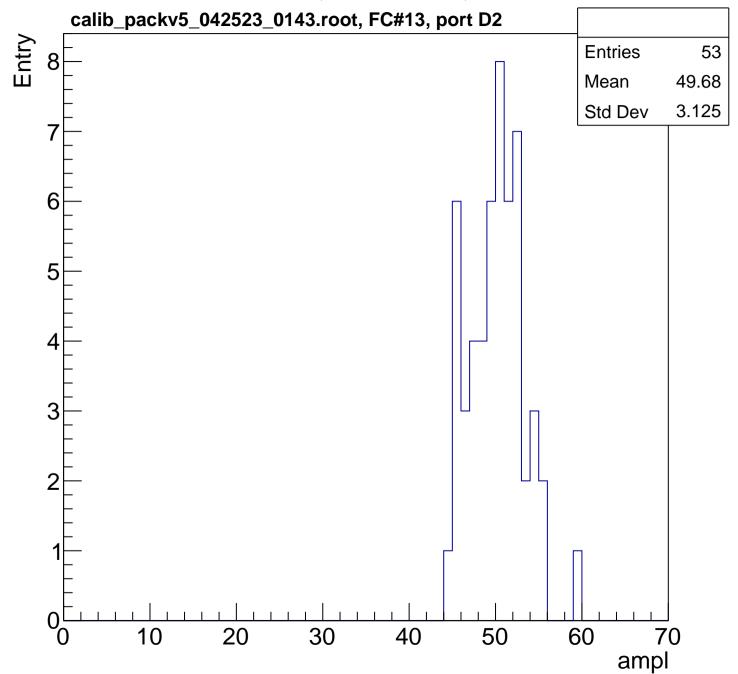
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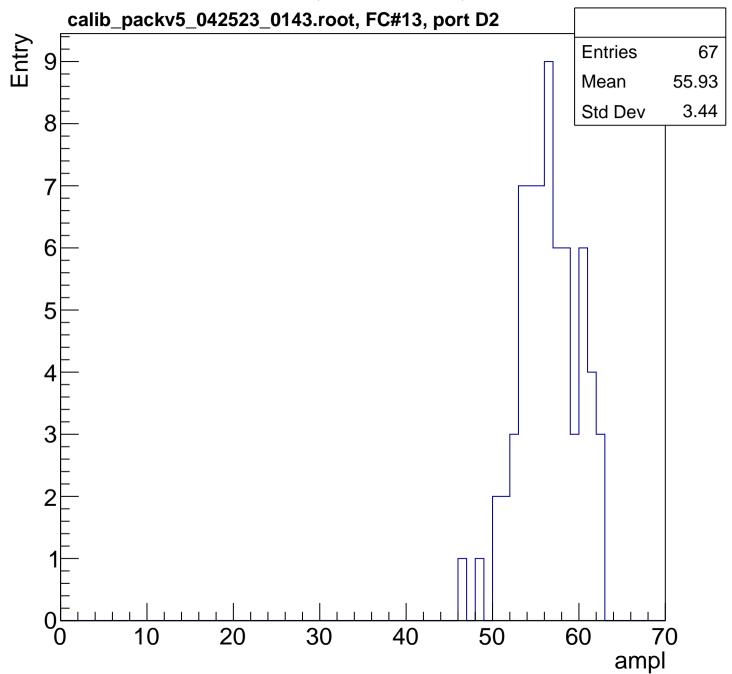


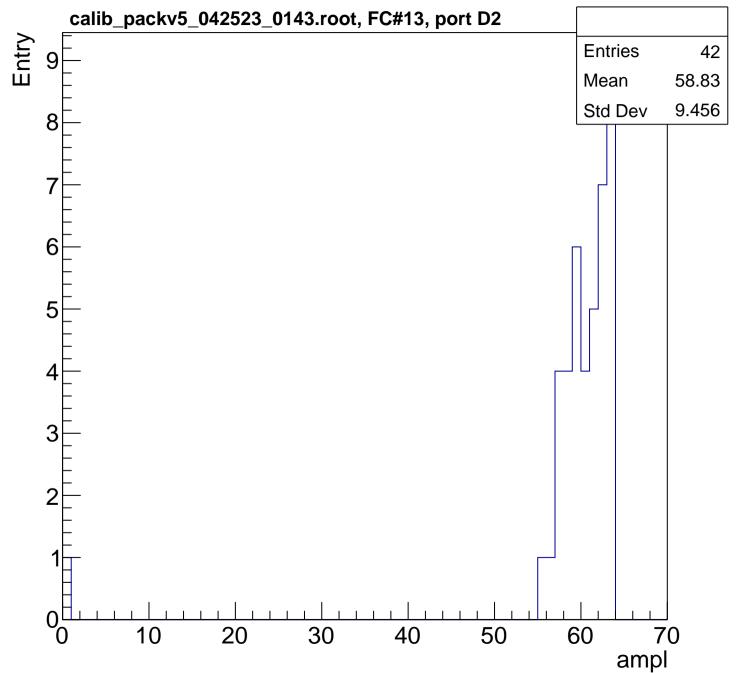


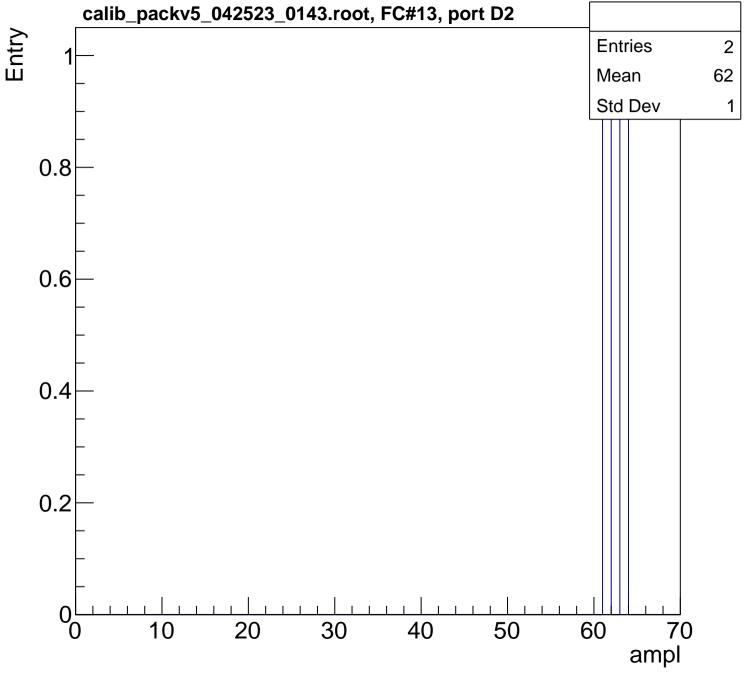


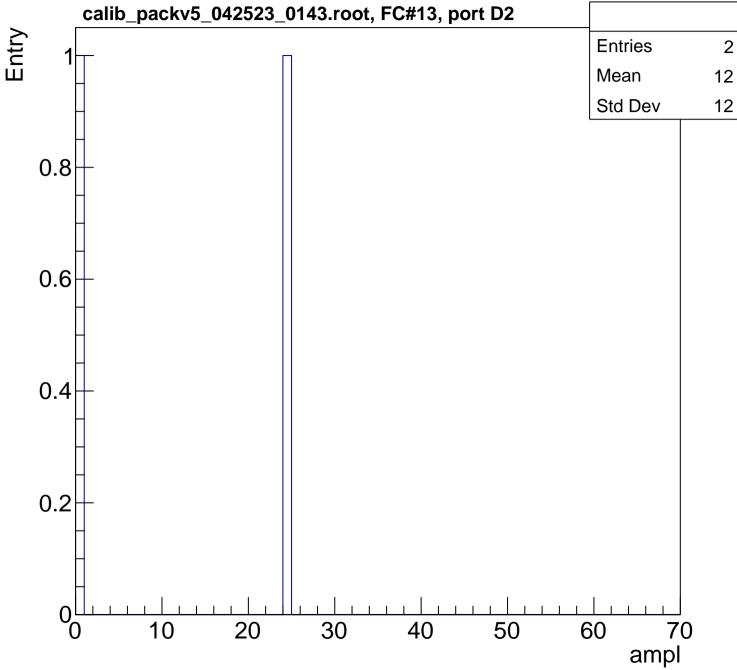


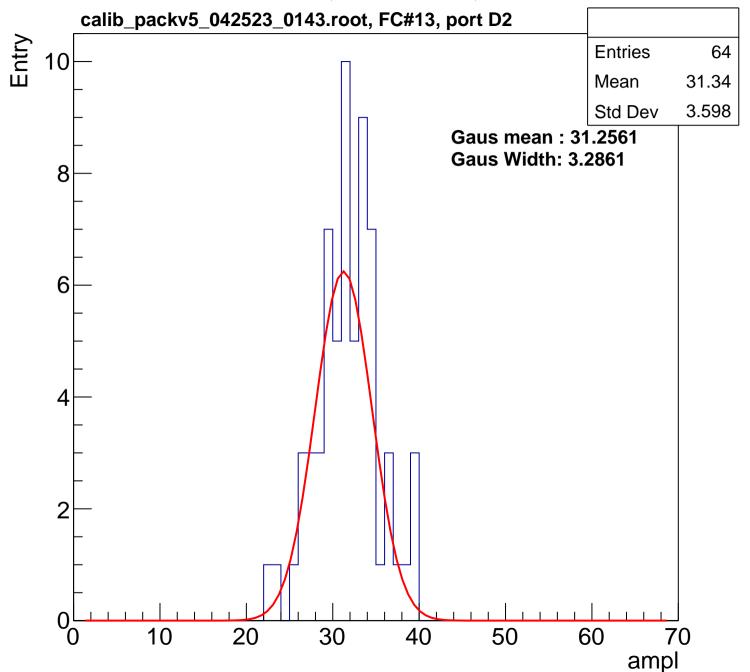


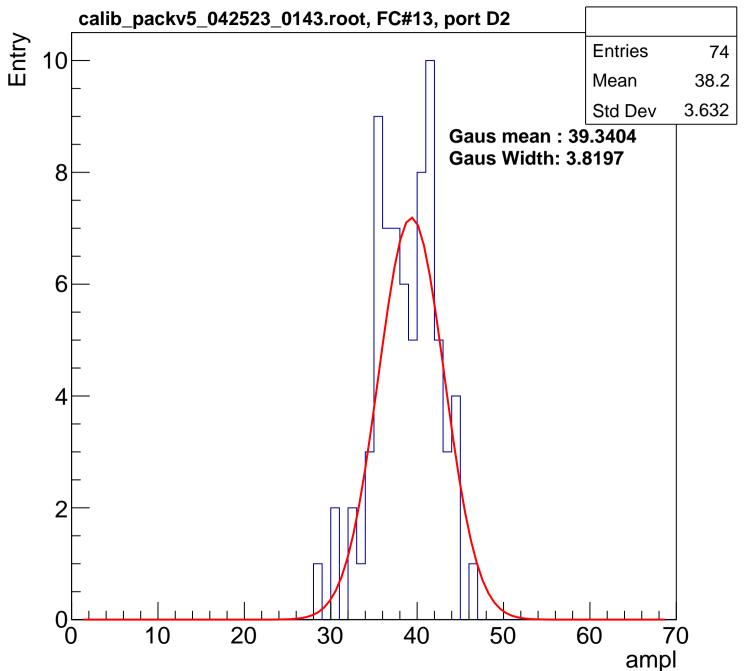


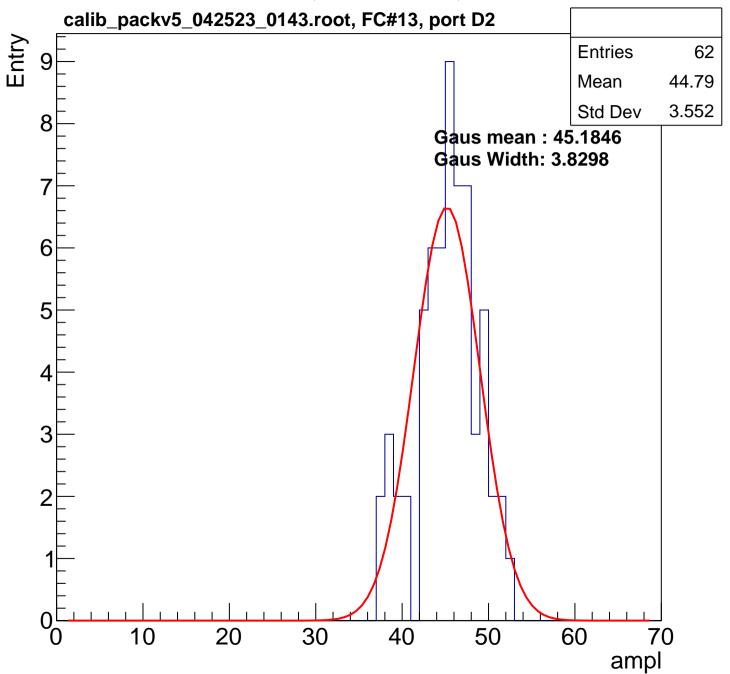


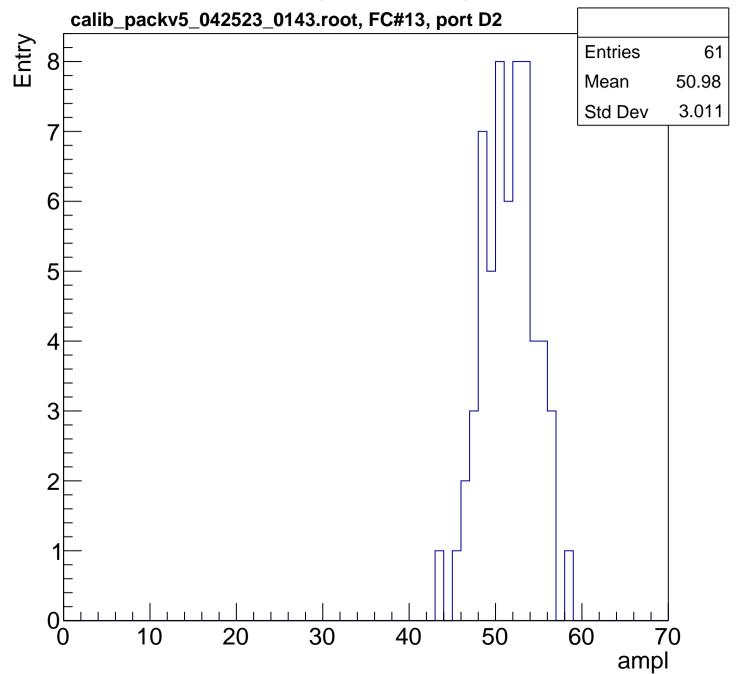


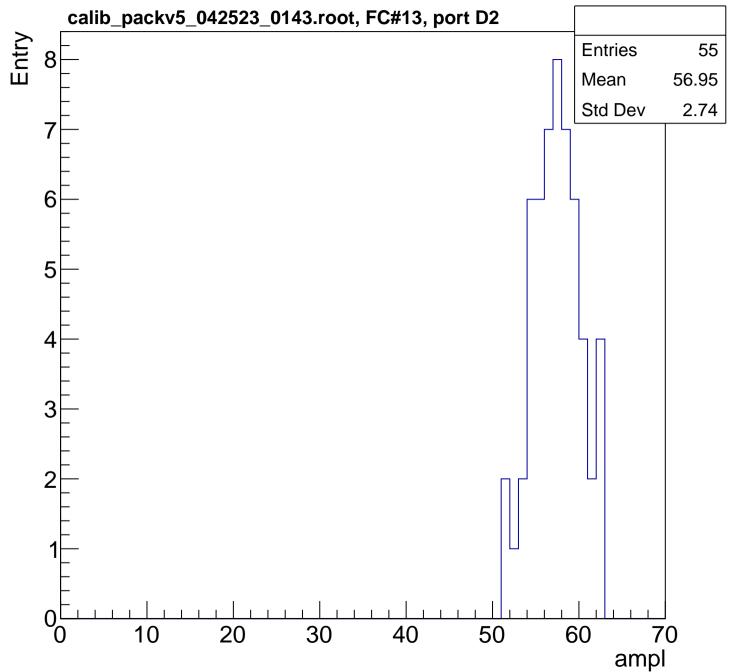


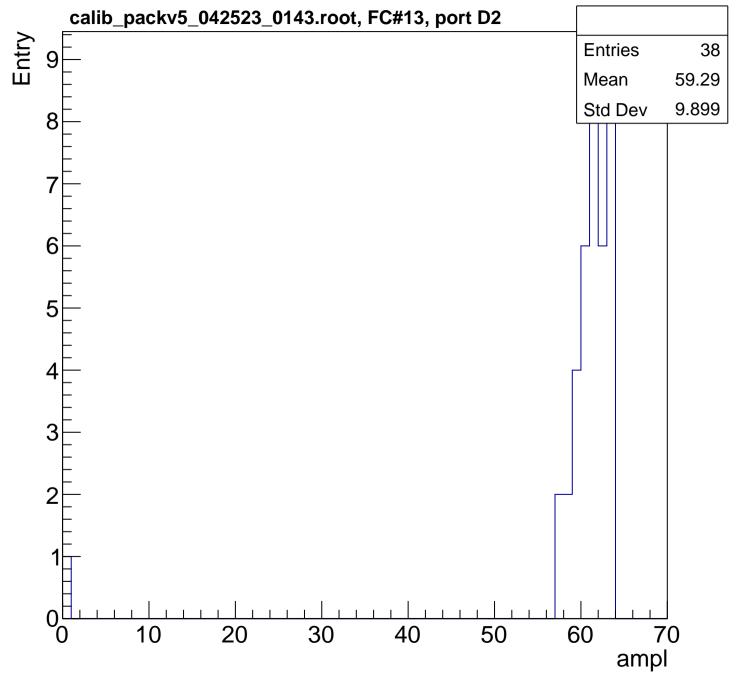


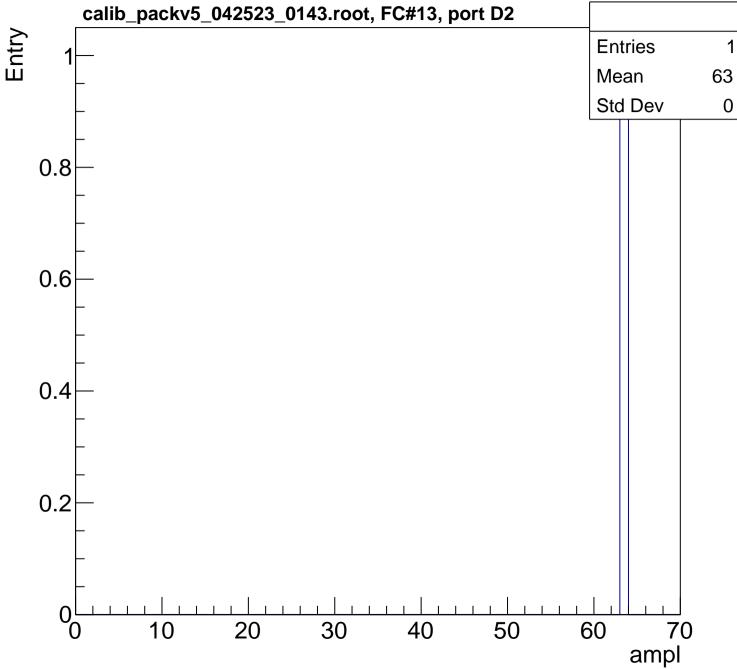




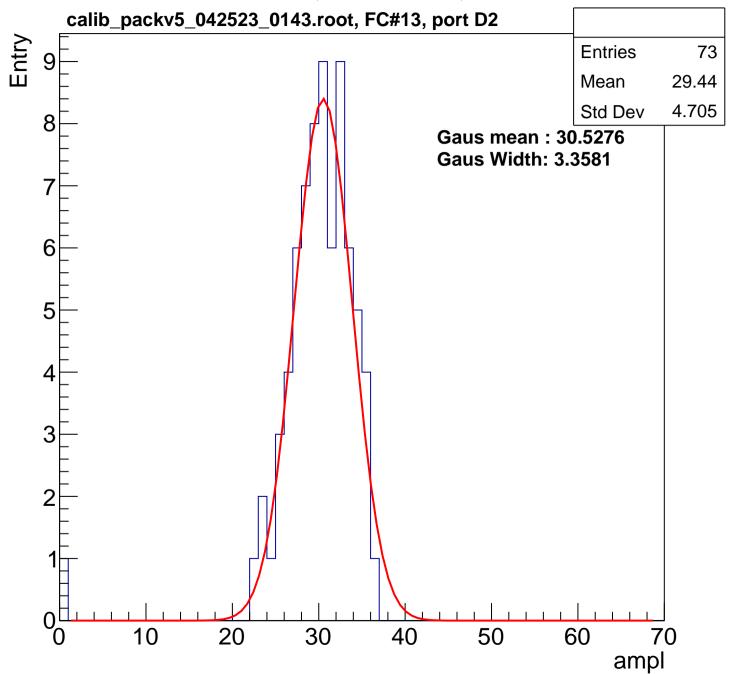


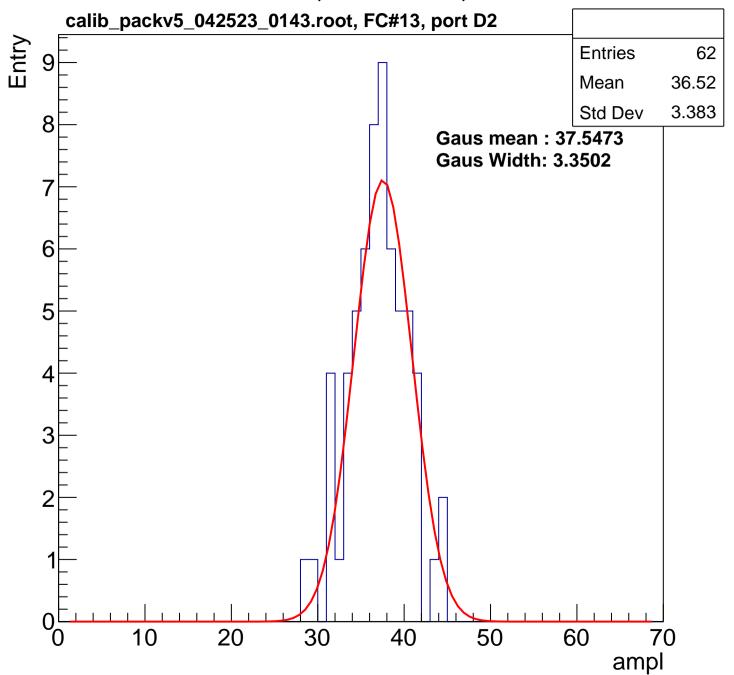


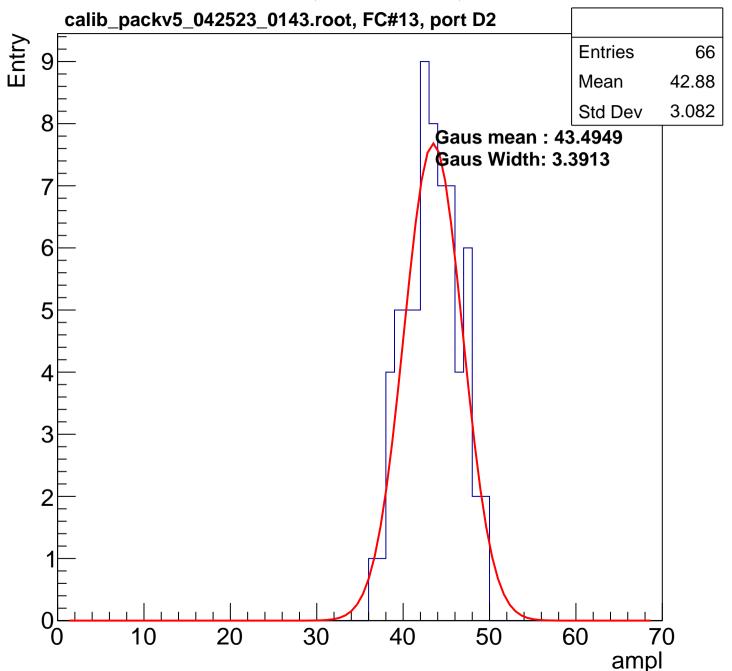


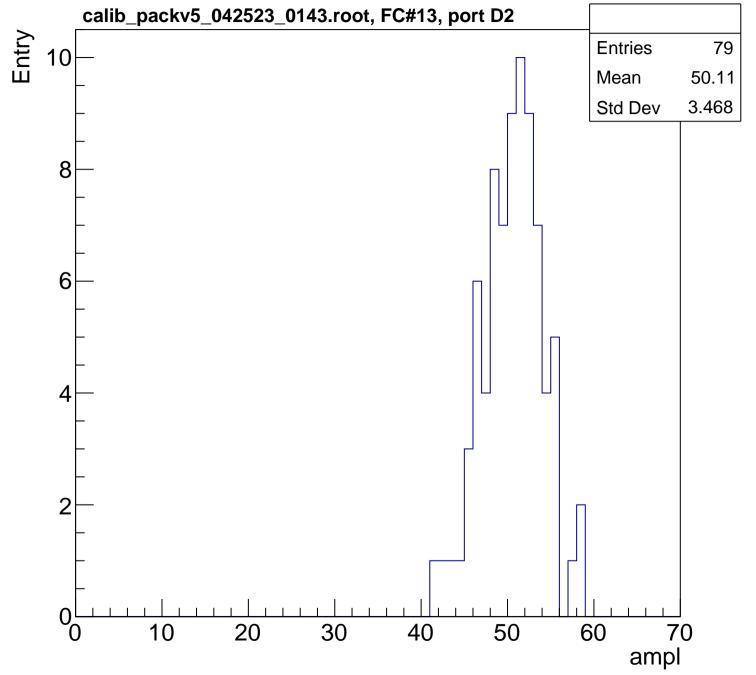


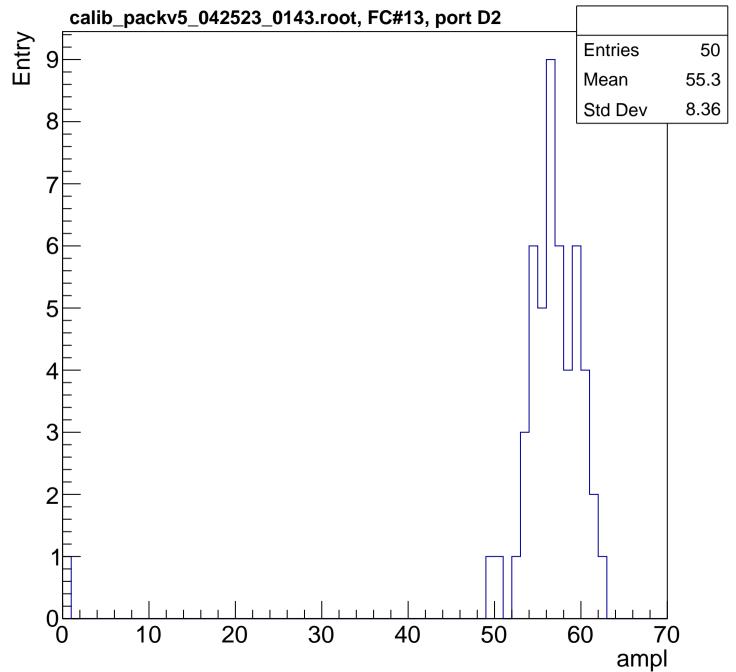


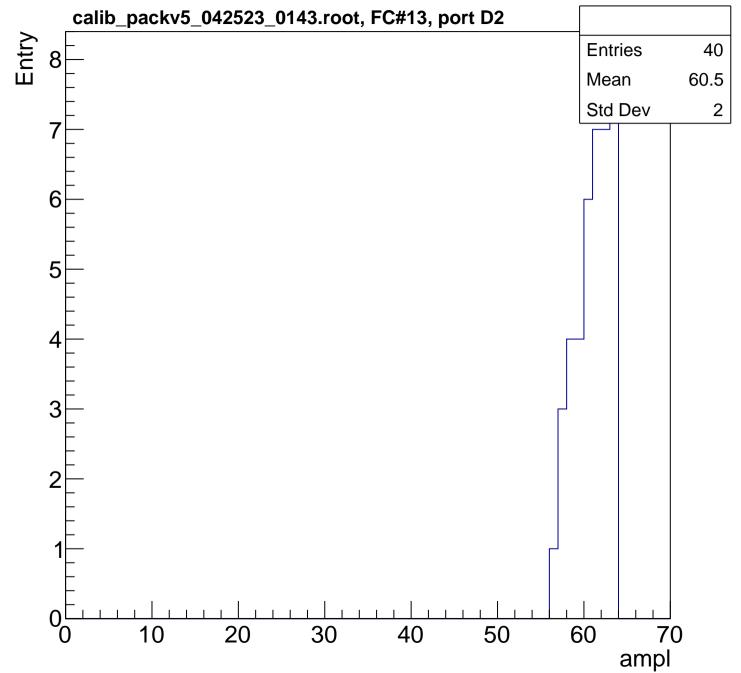


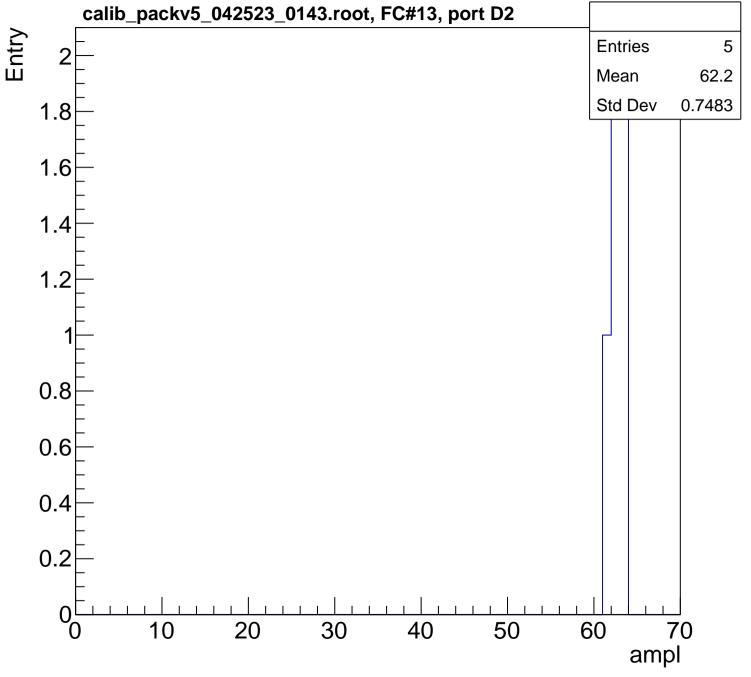




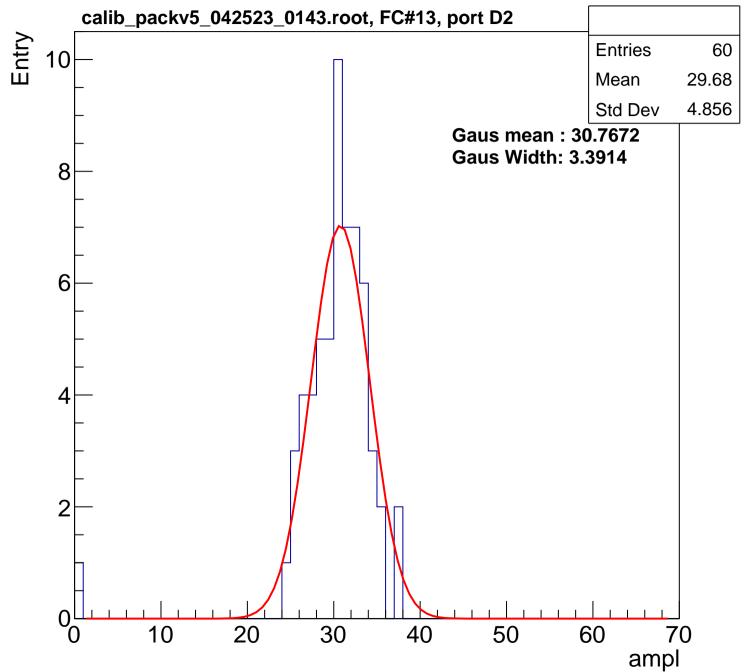


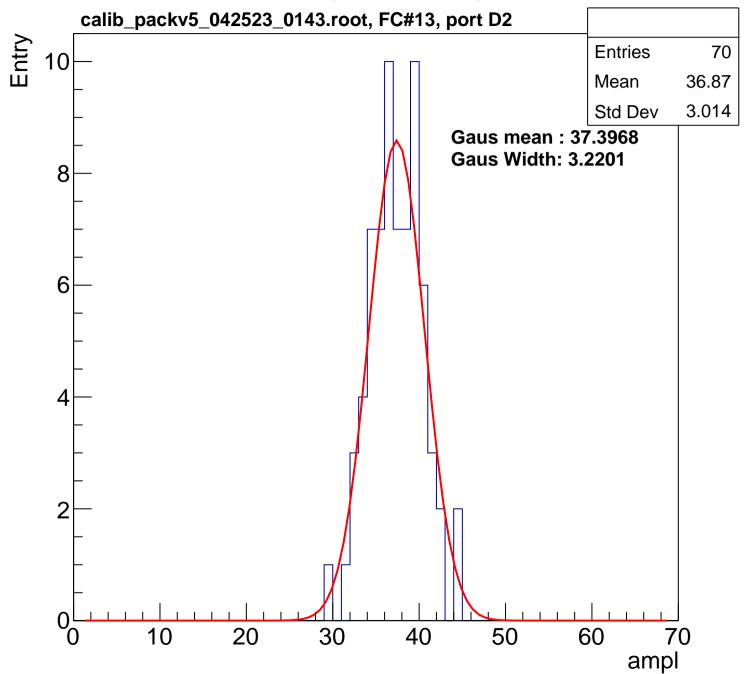


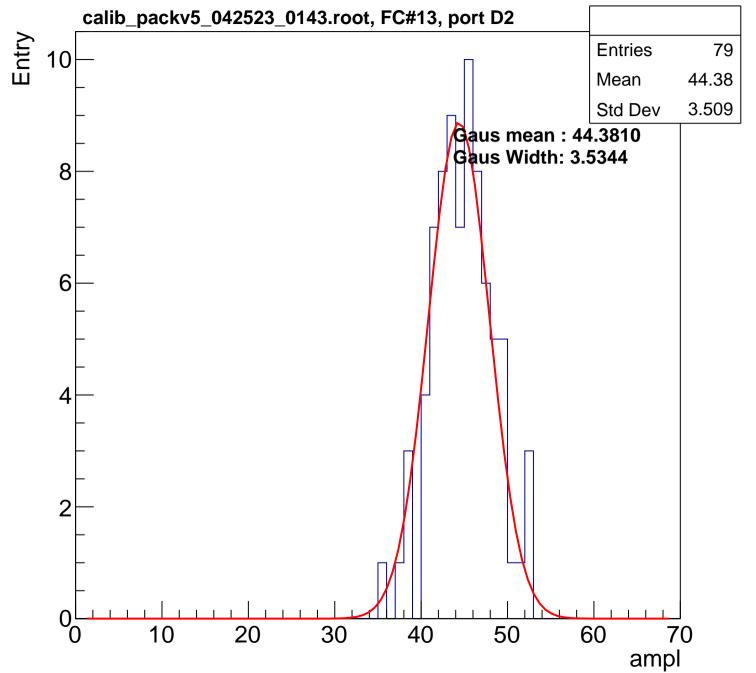


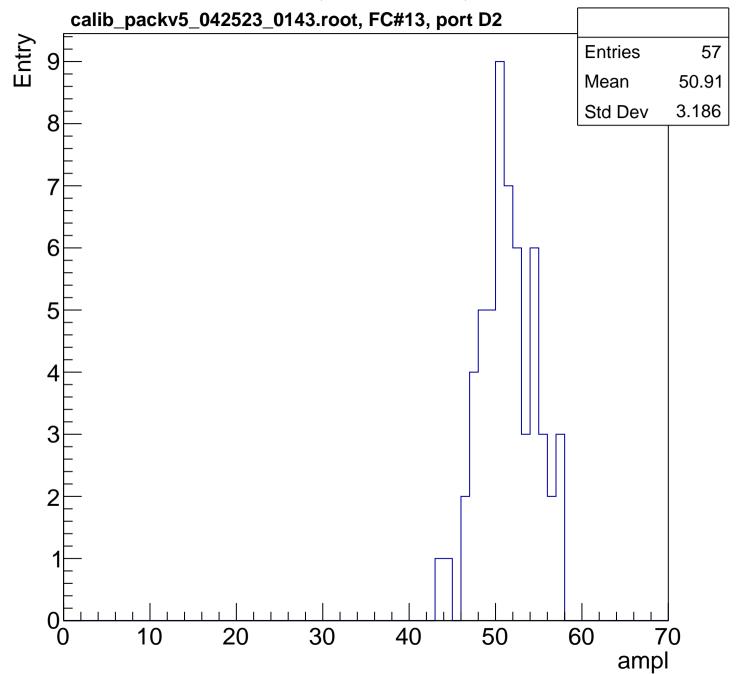


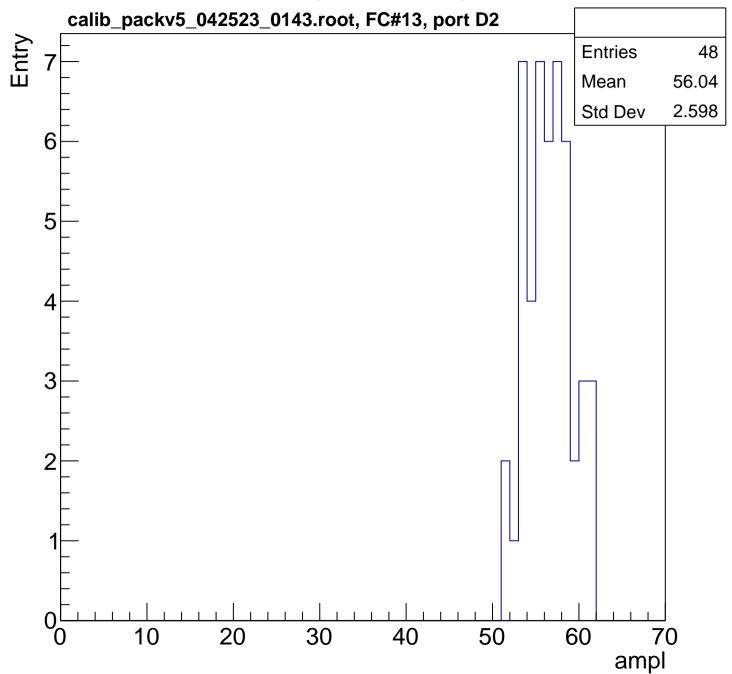
B1L003S, U7-ch20, adc7 calib_packv5_042523_0143.root, FC#13, port D2 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

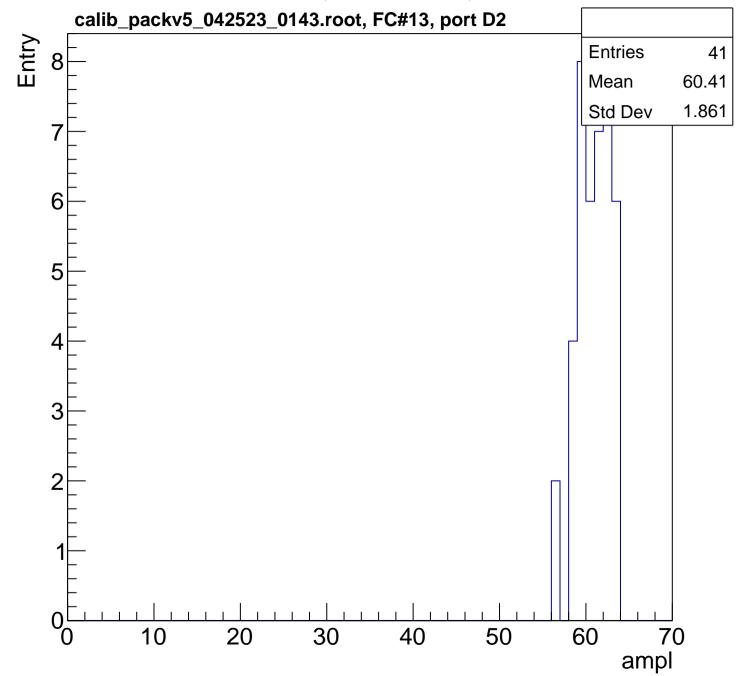


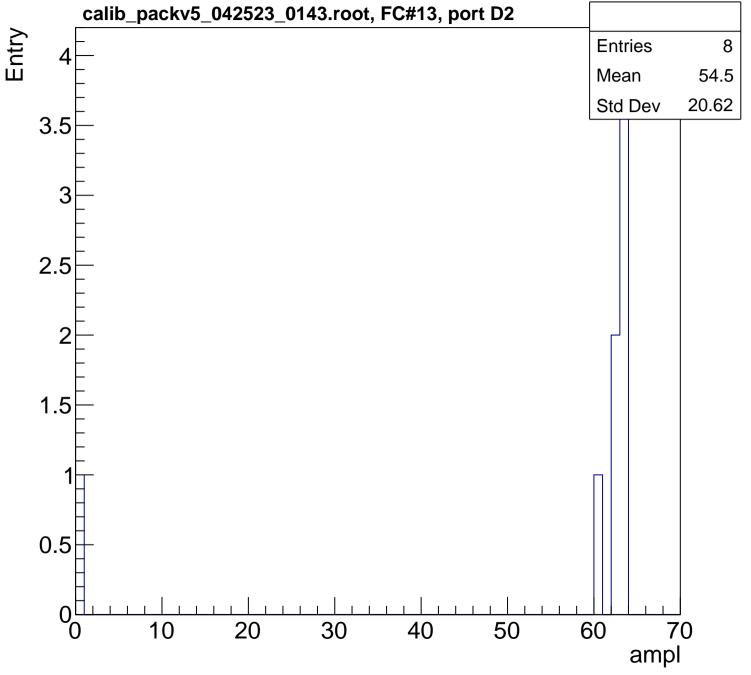




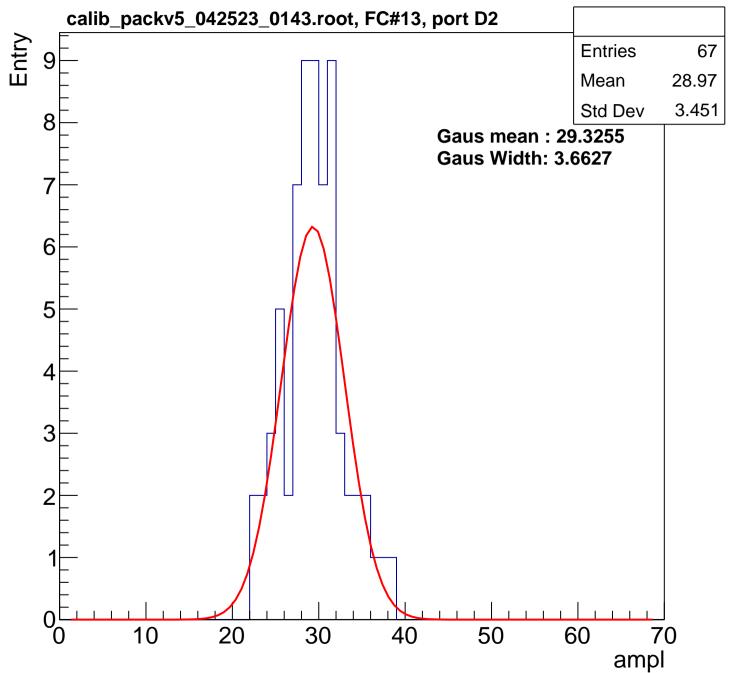


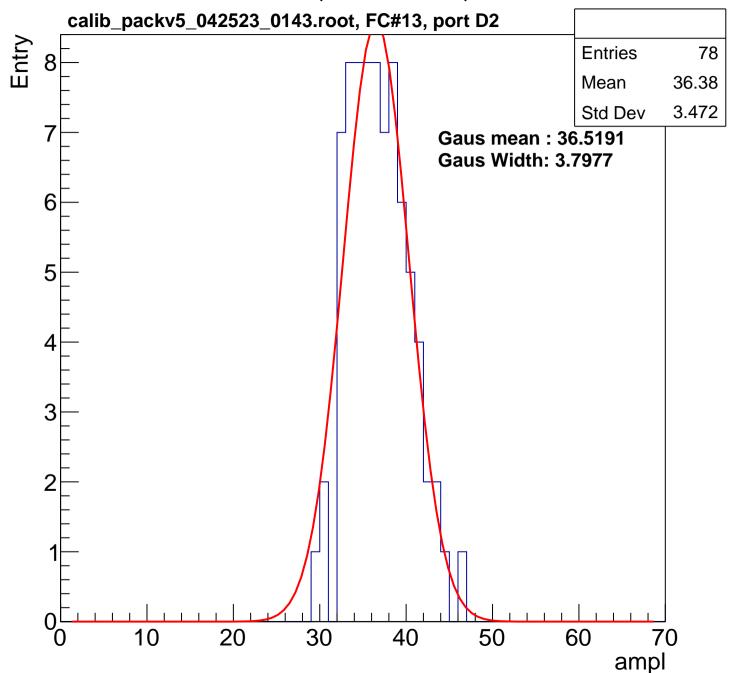


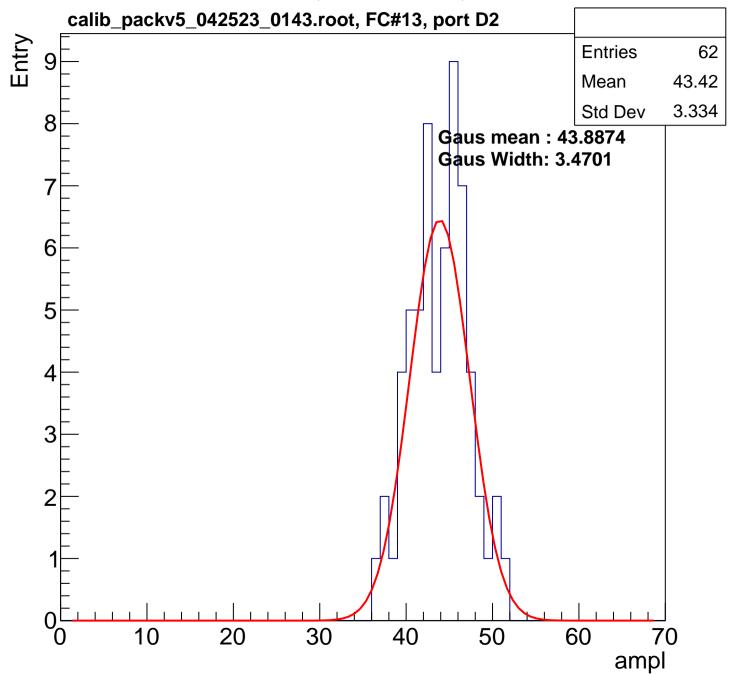


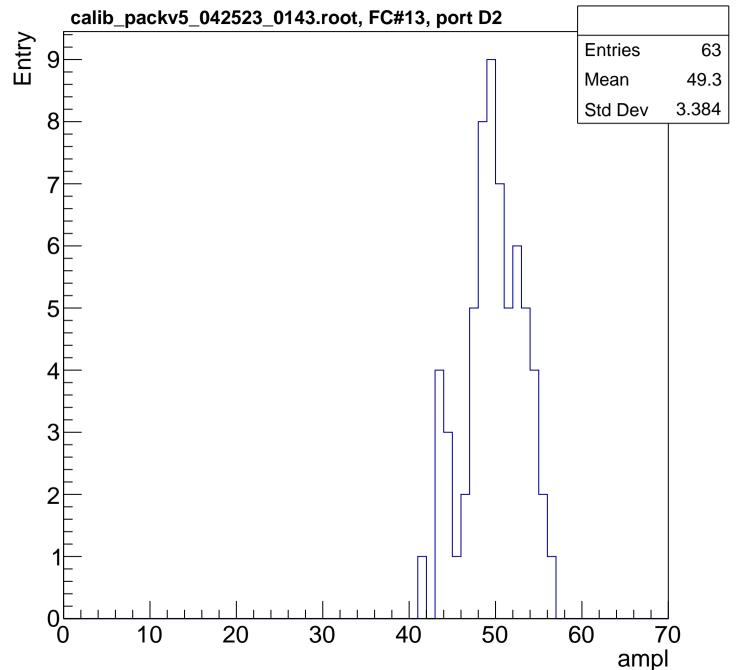


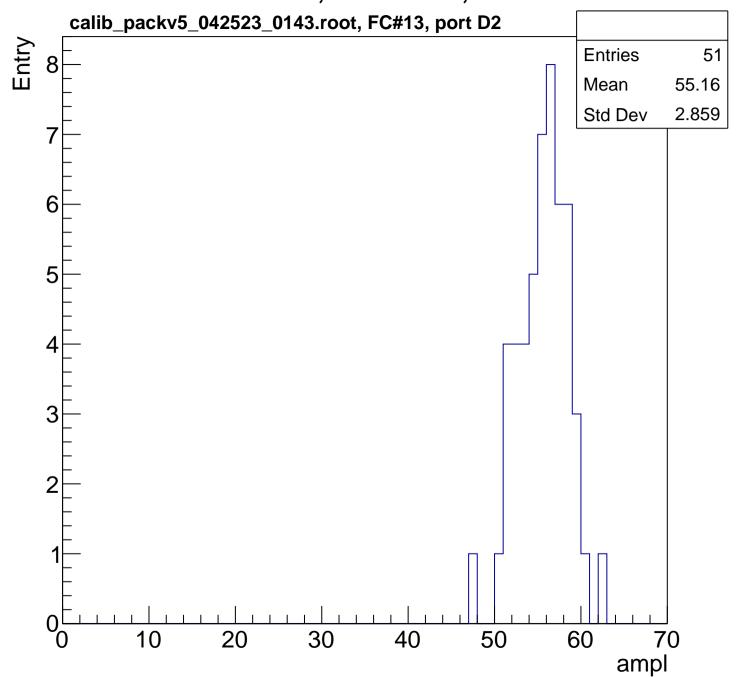


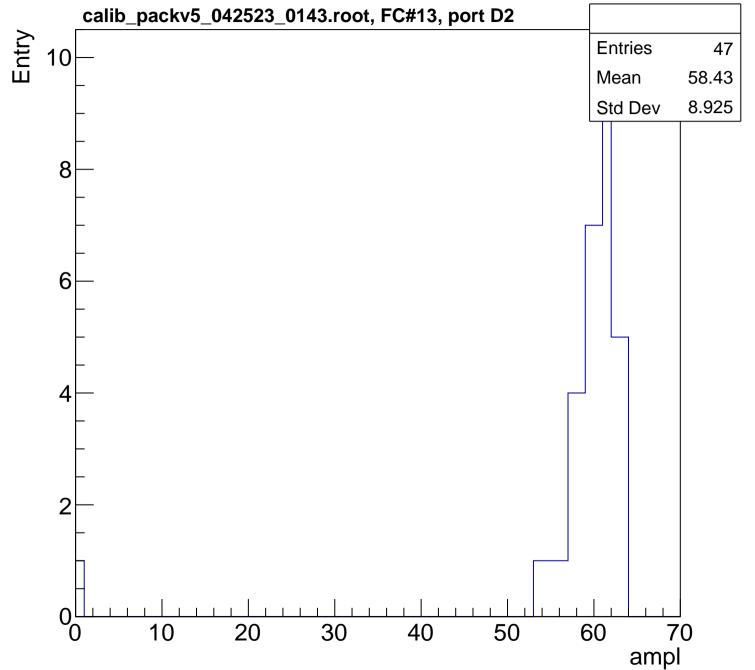


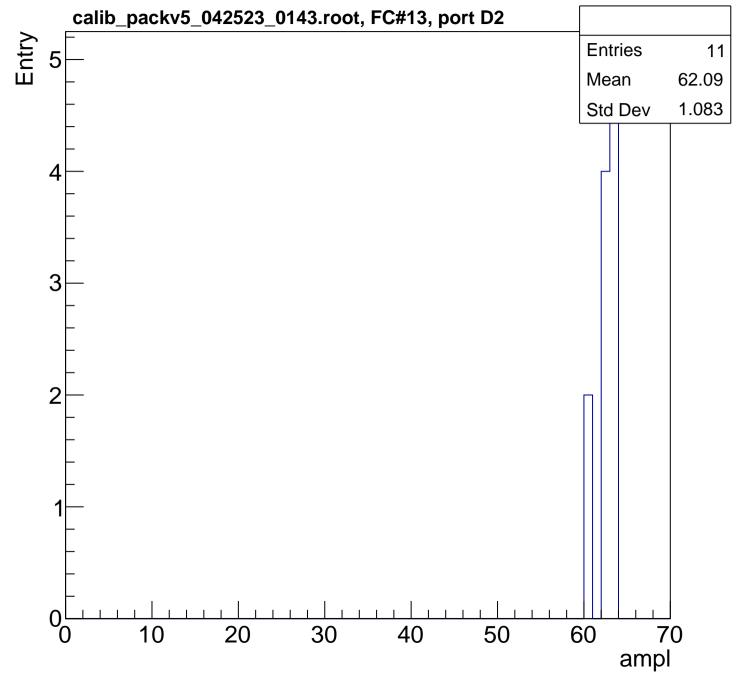


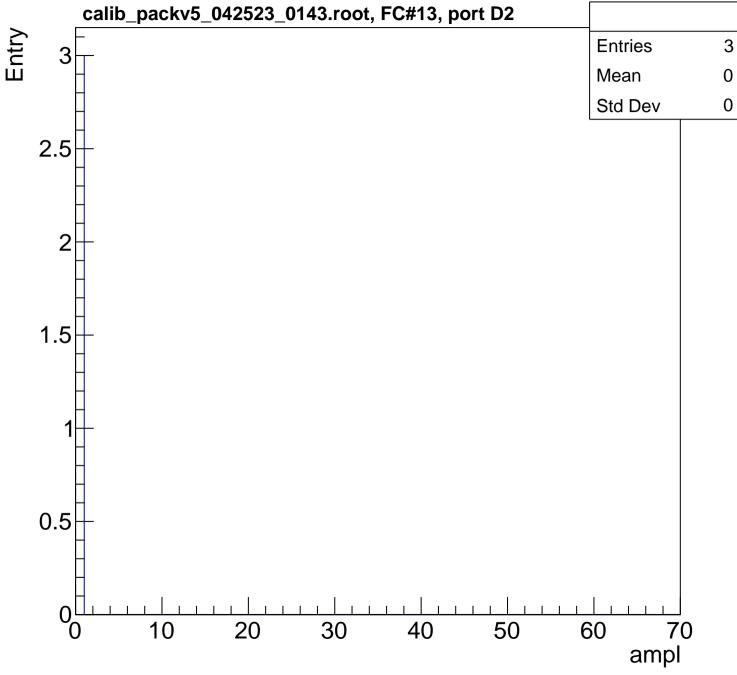


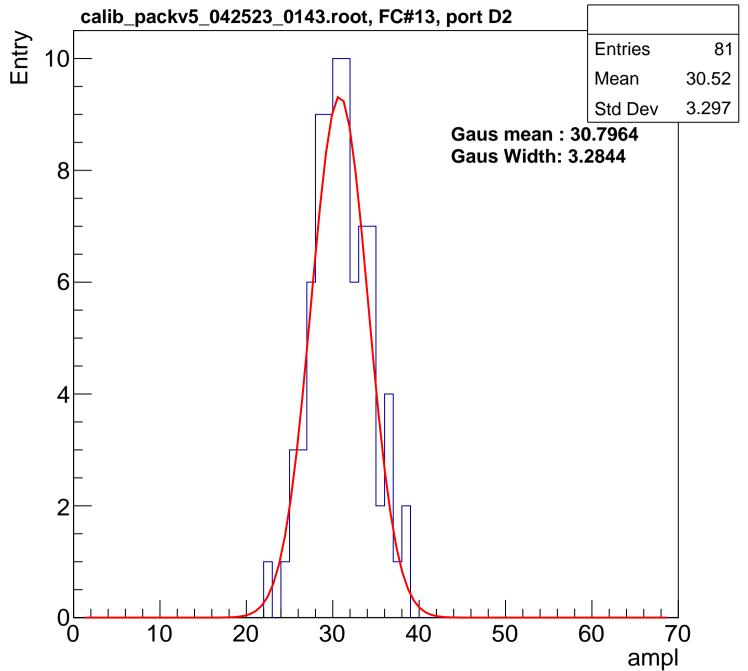


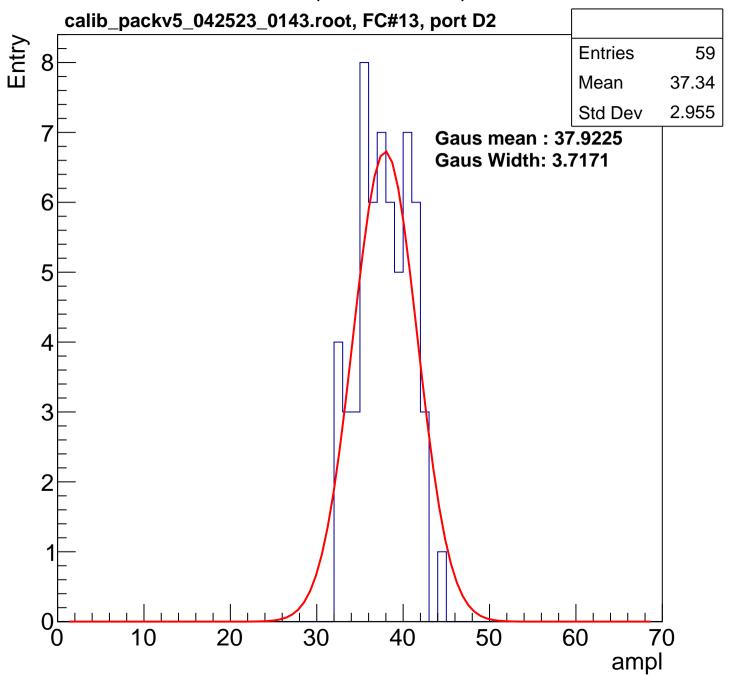


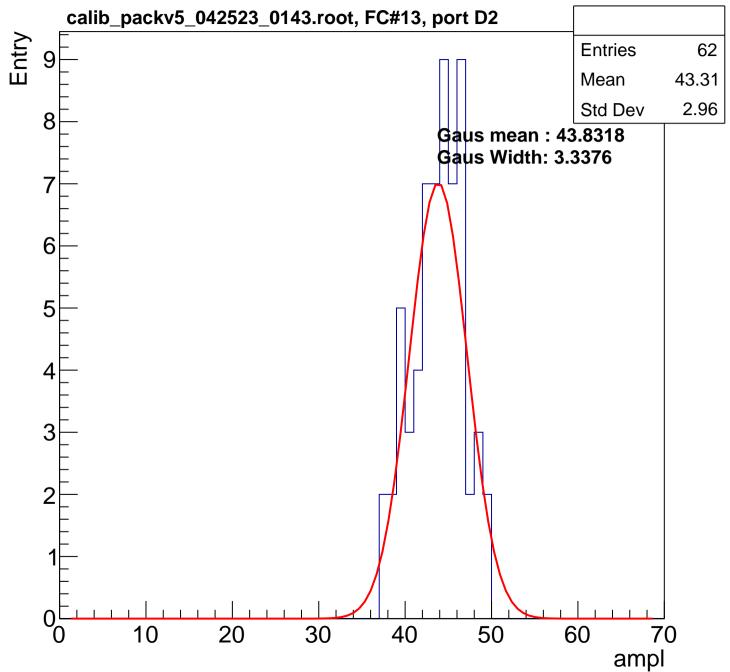


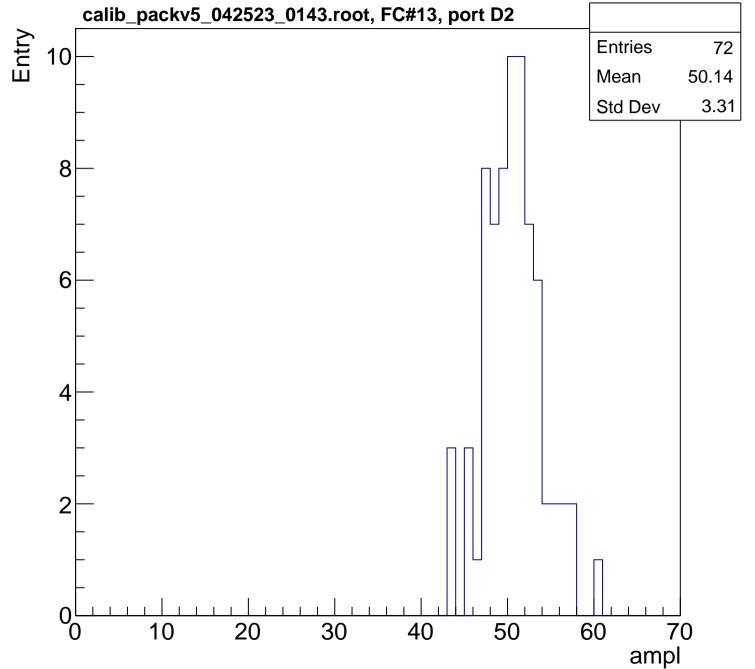


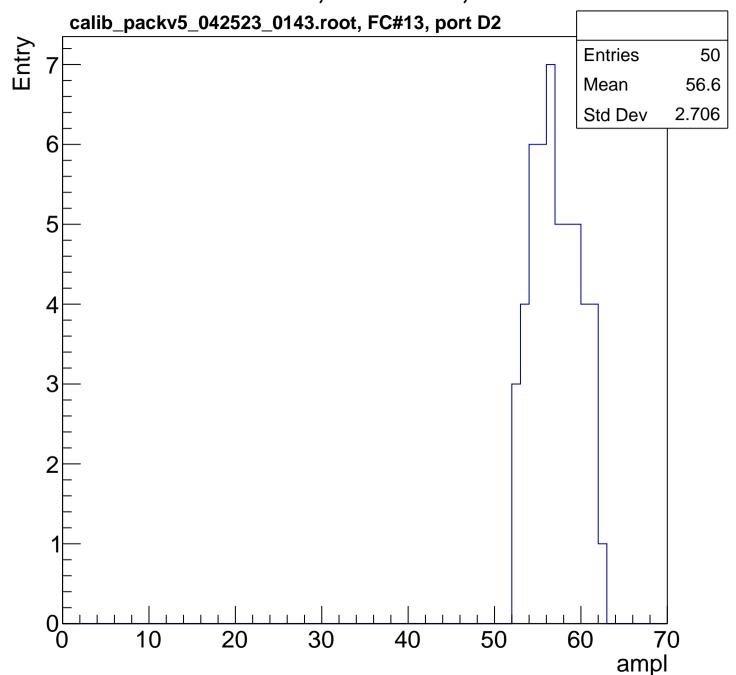


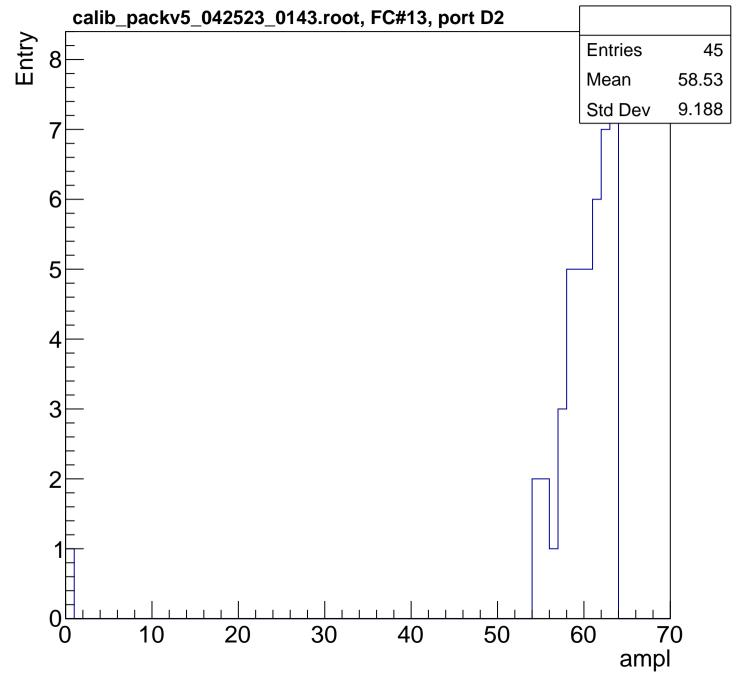


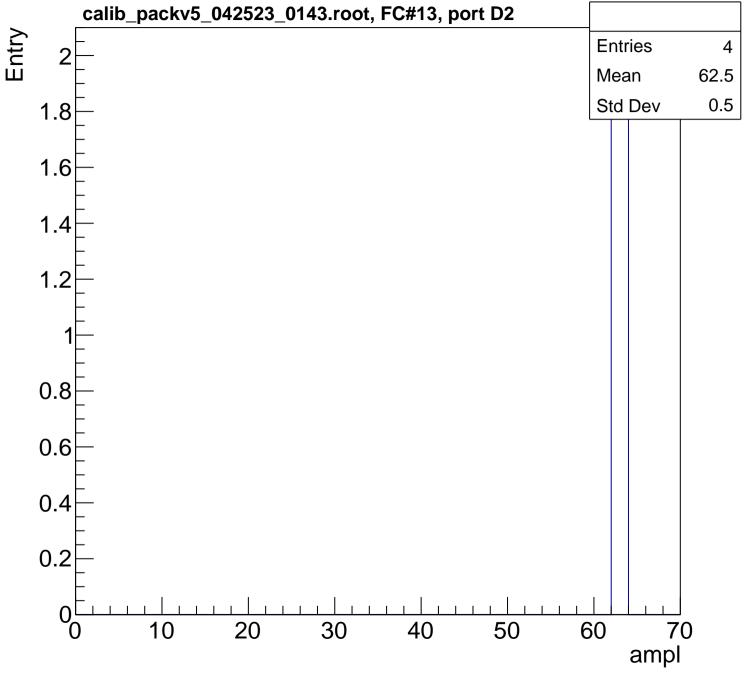


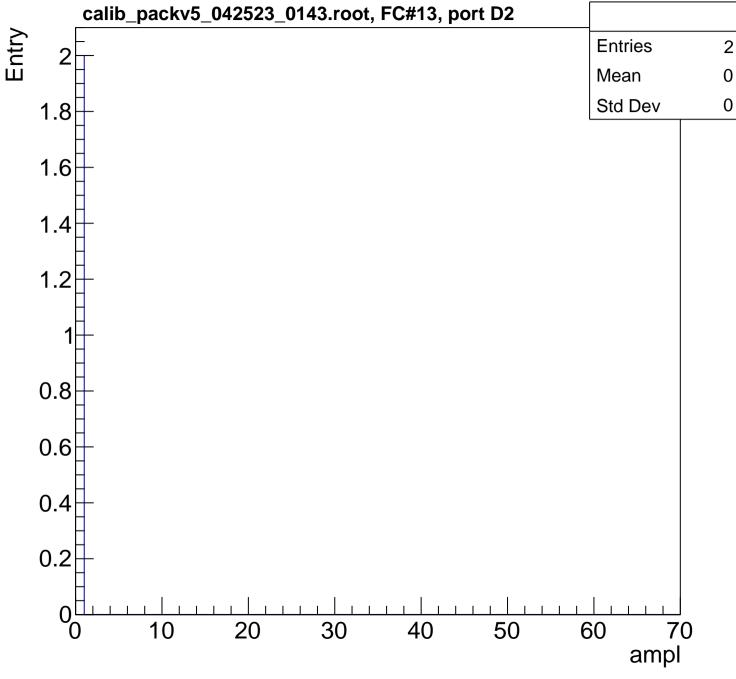


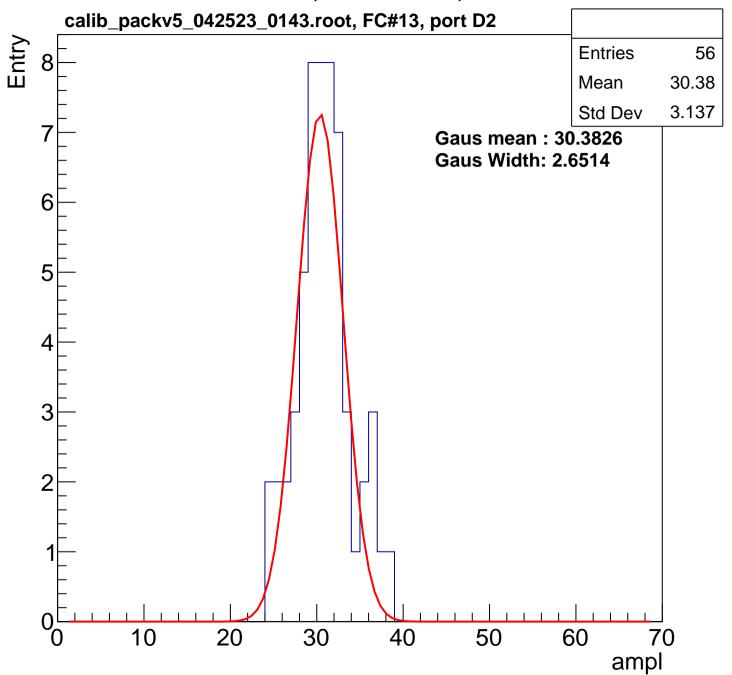


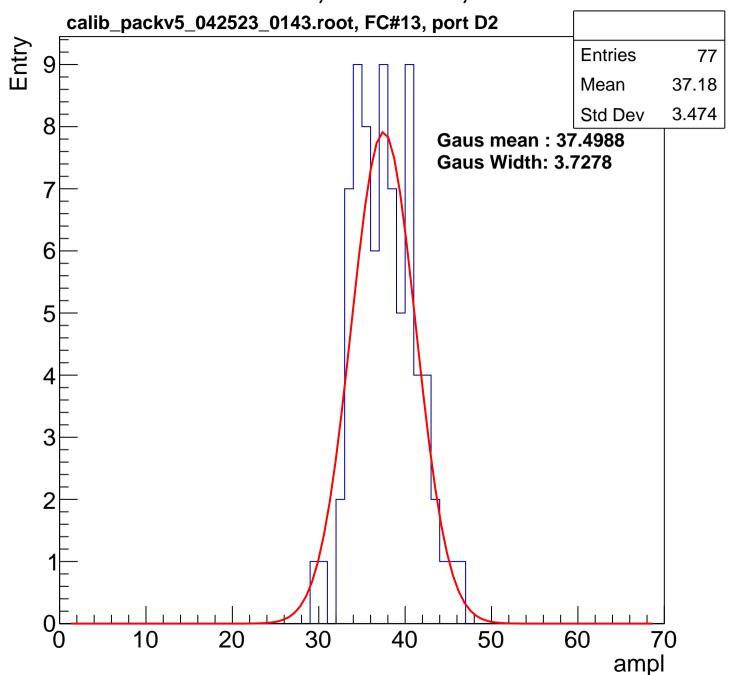


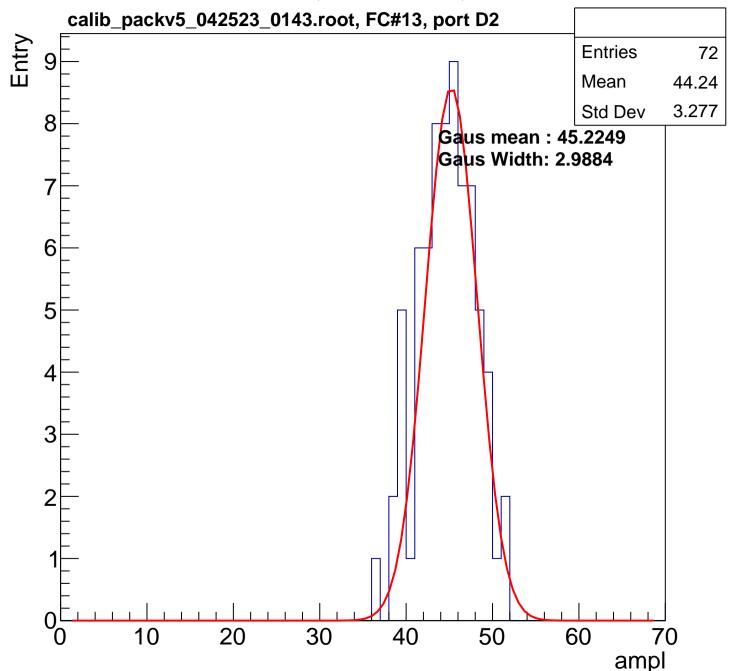


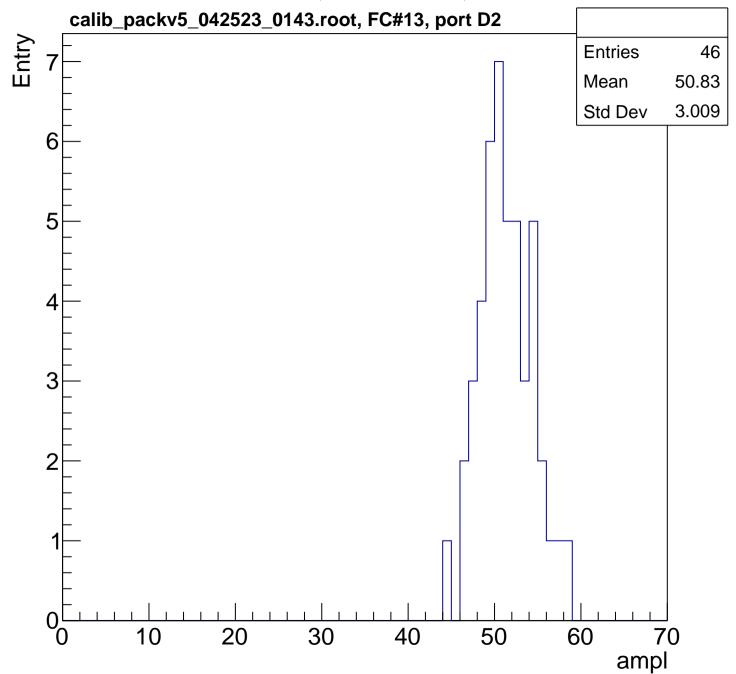


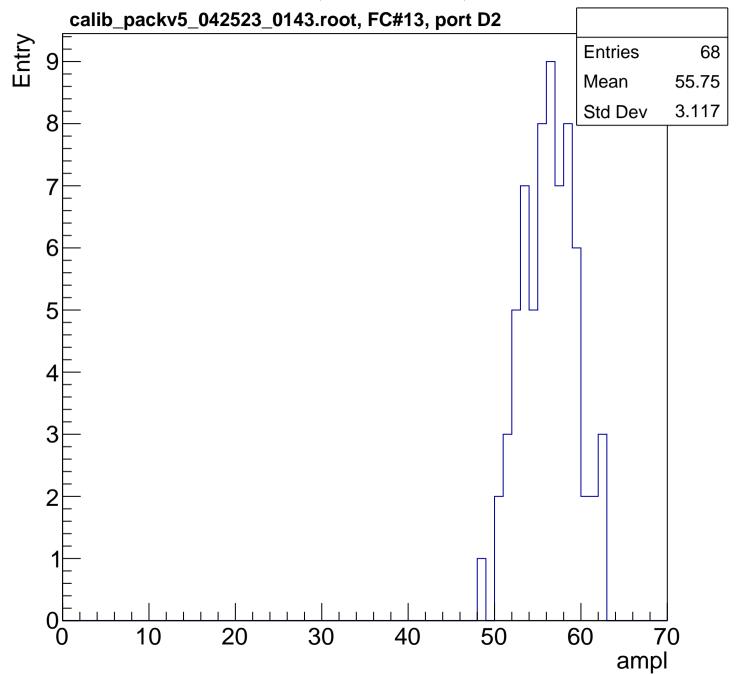


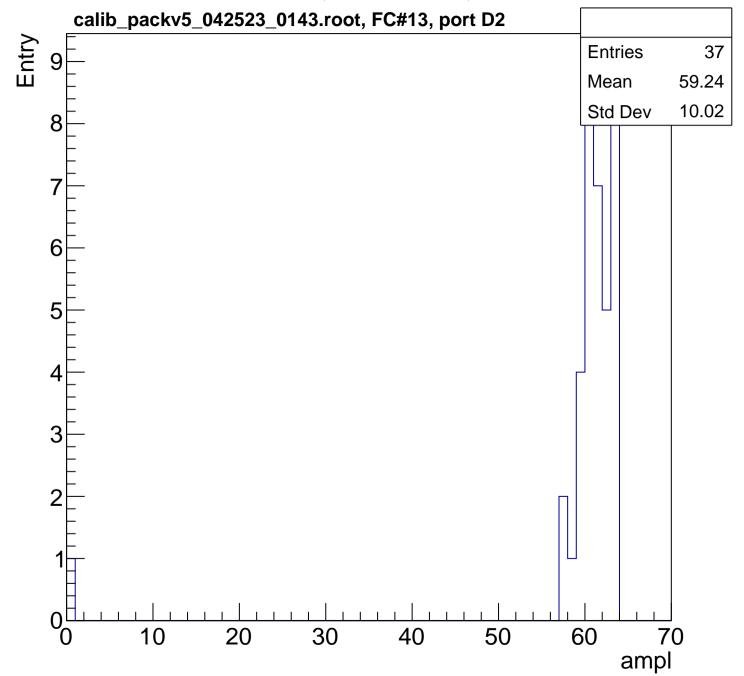


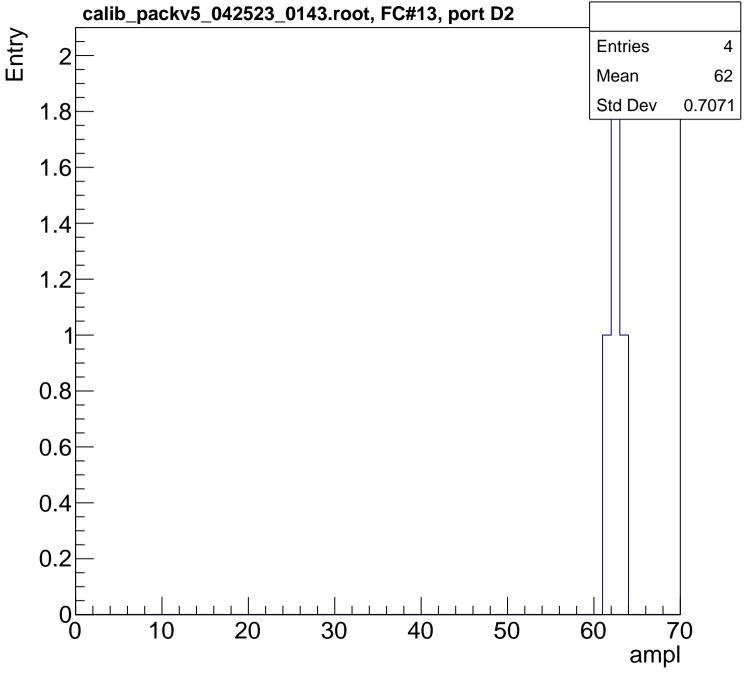


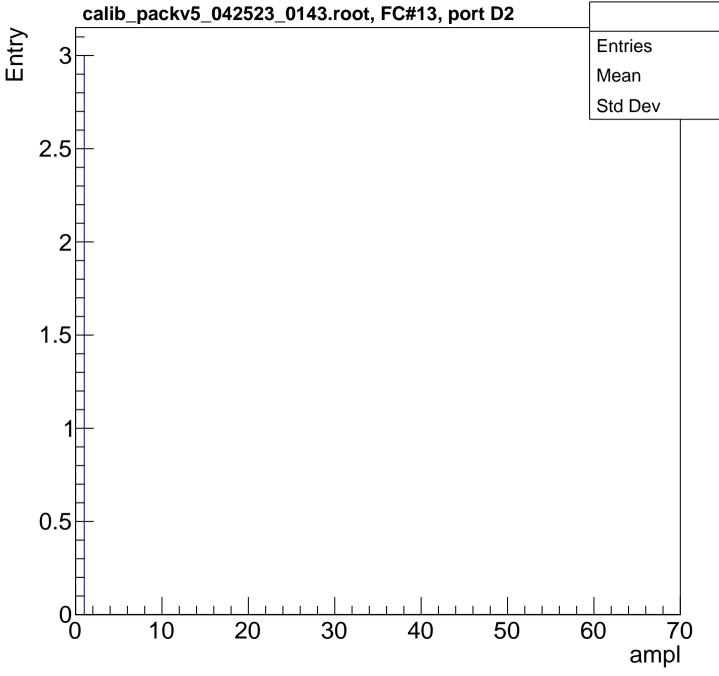


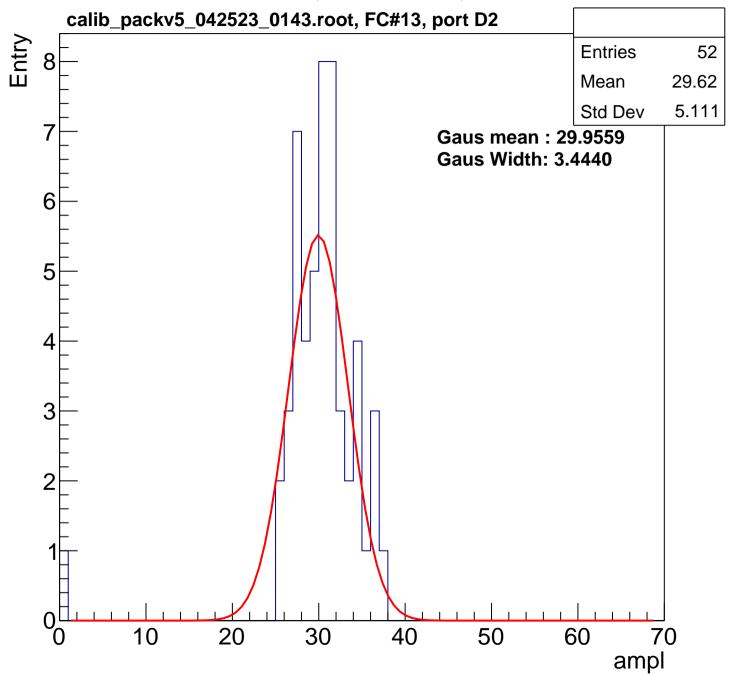


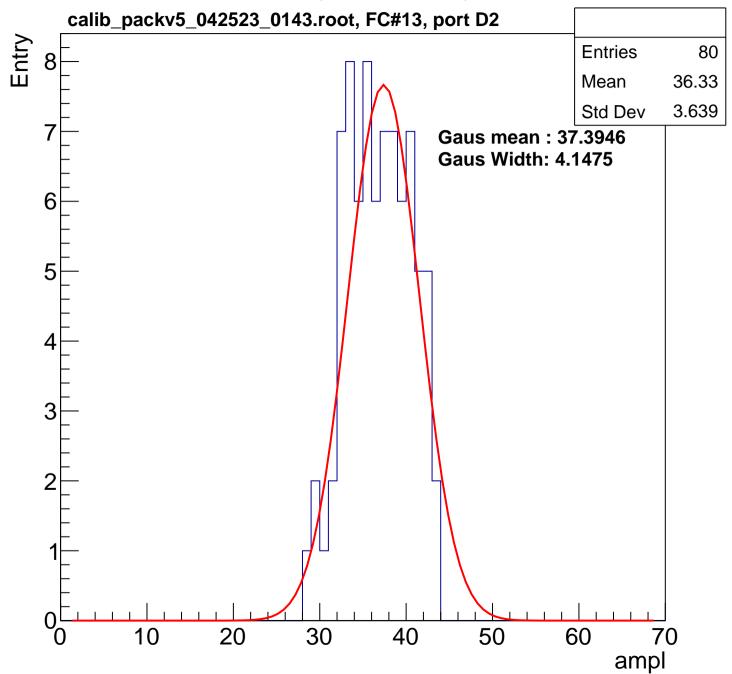


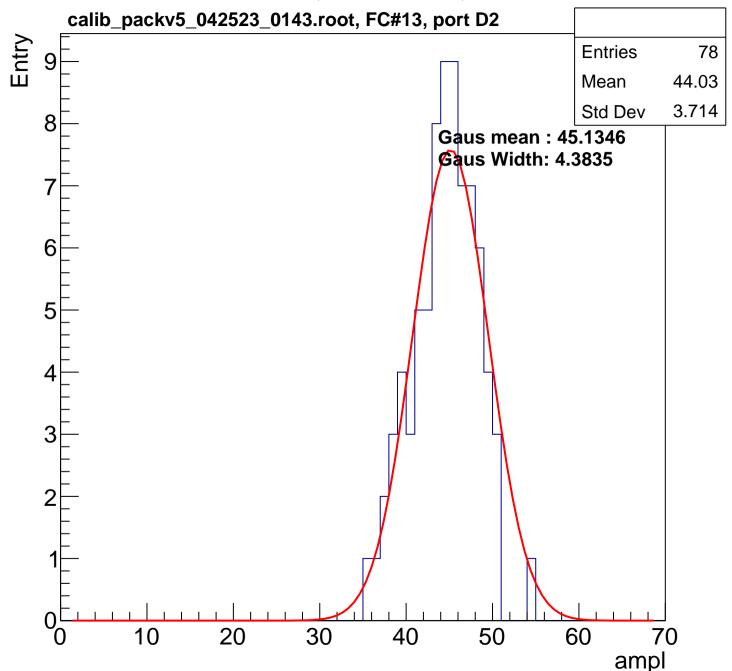


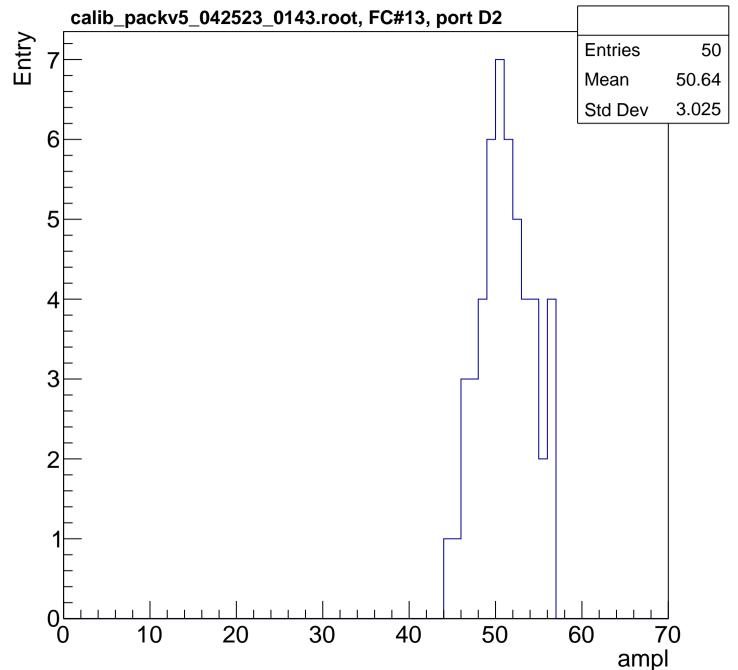


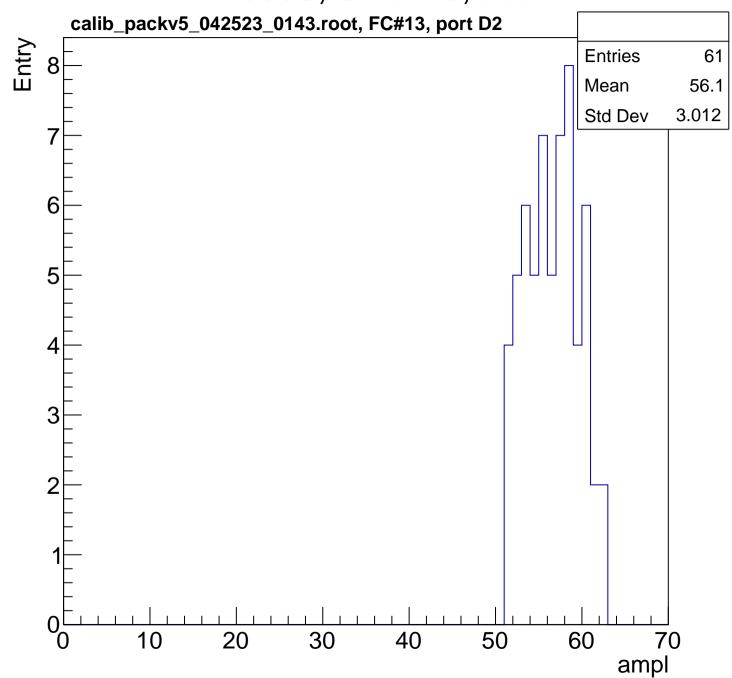


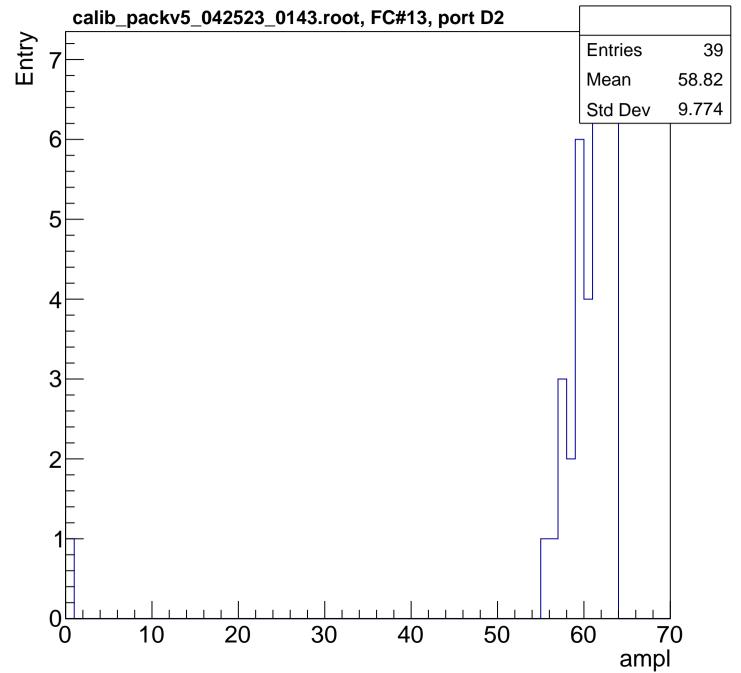


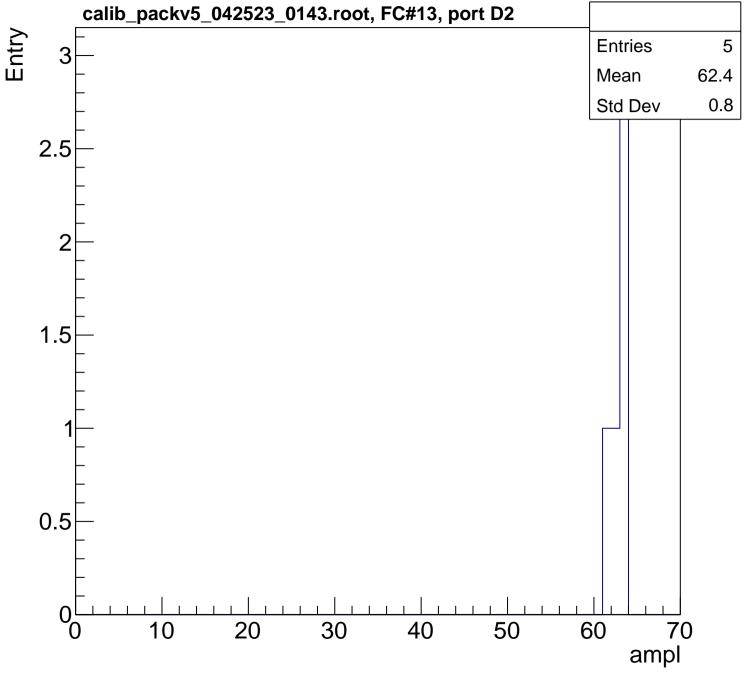


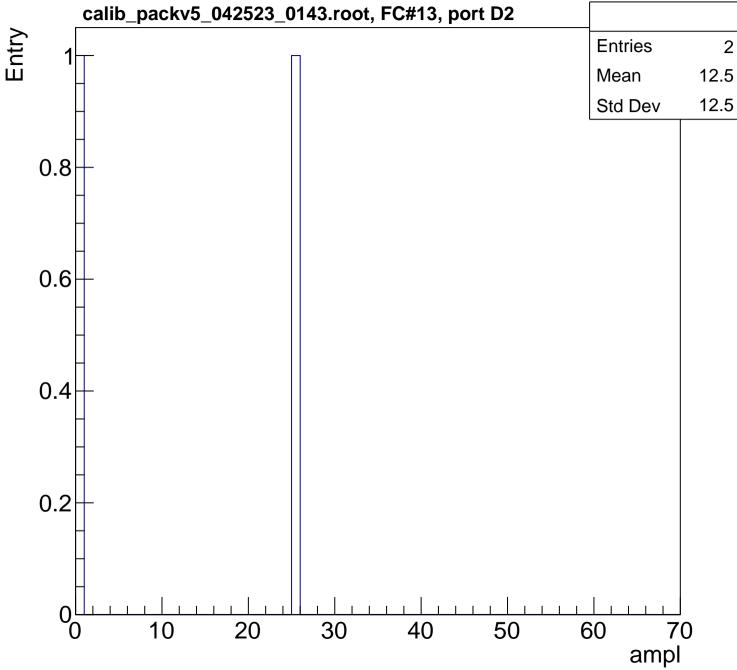


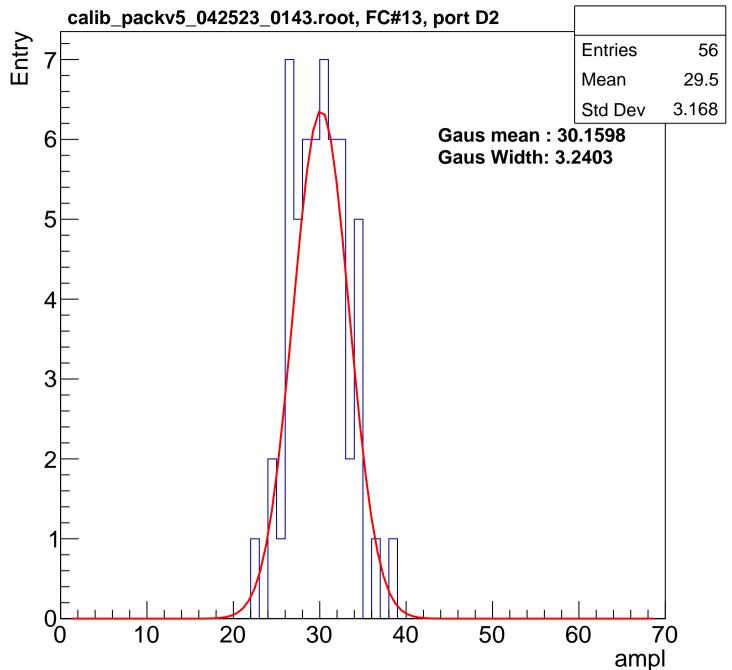


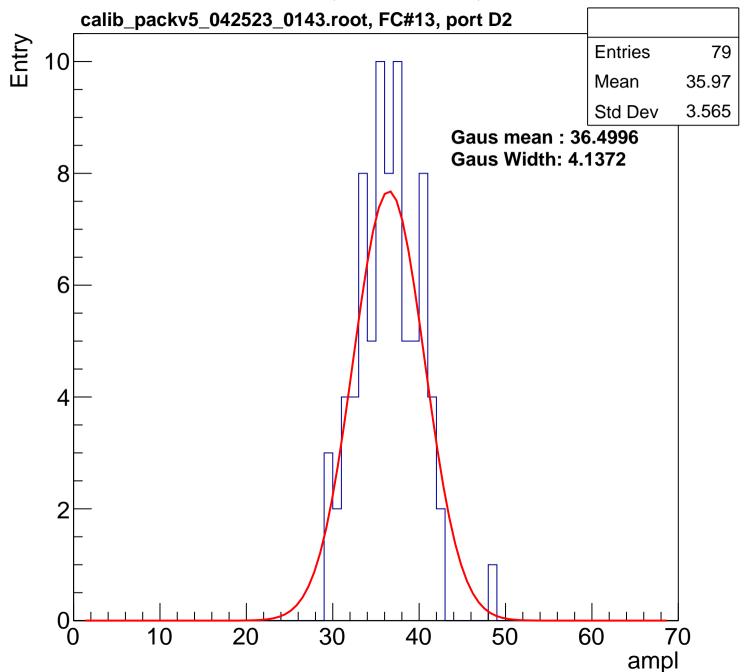


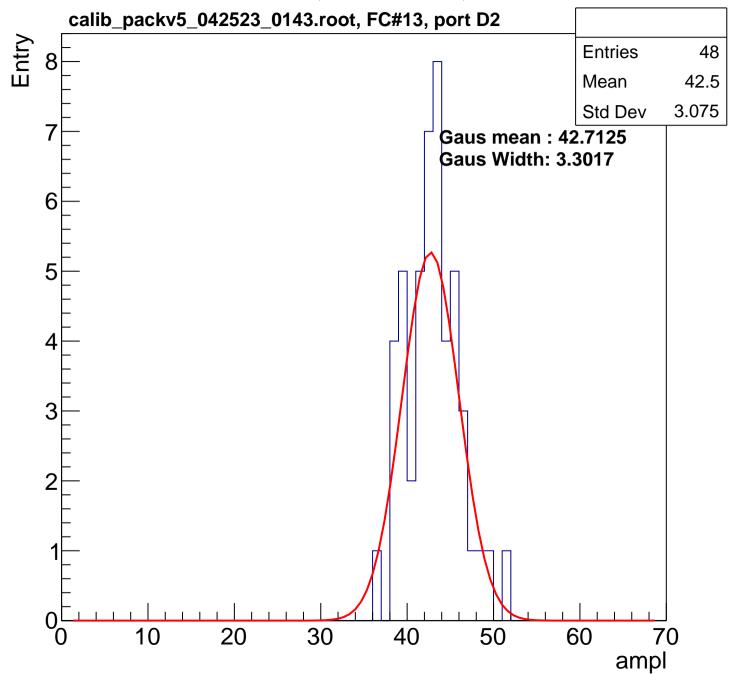


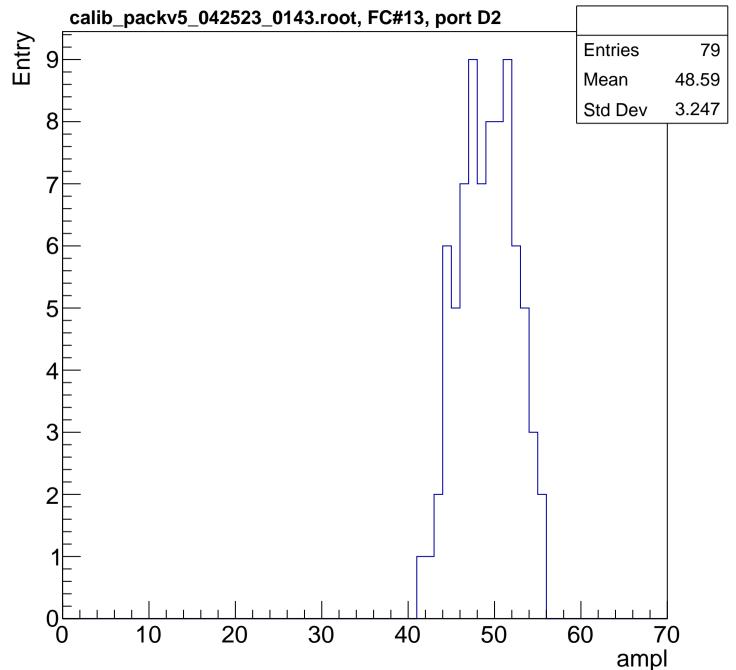


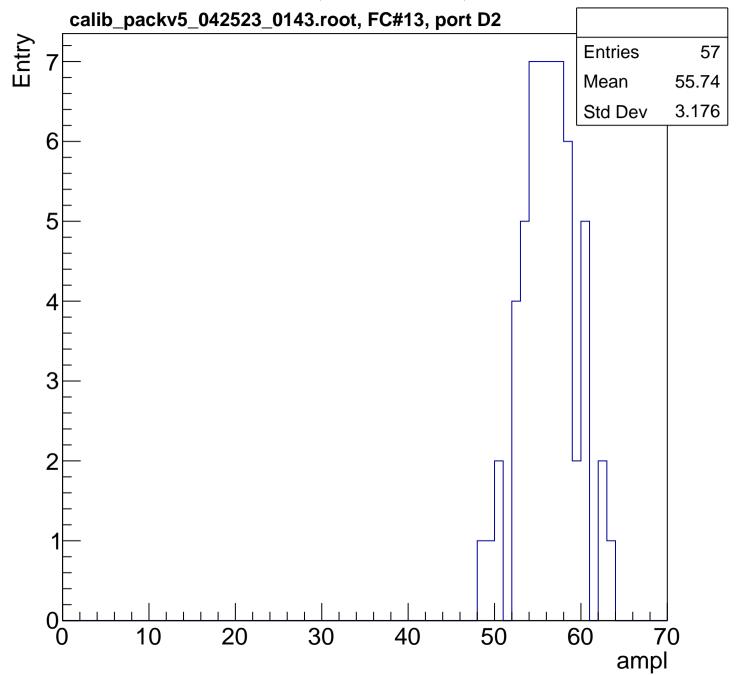


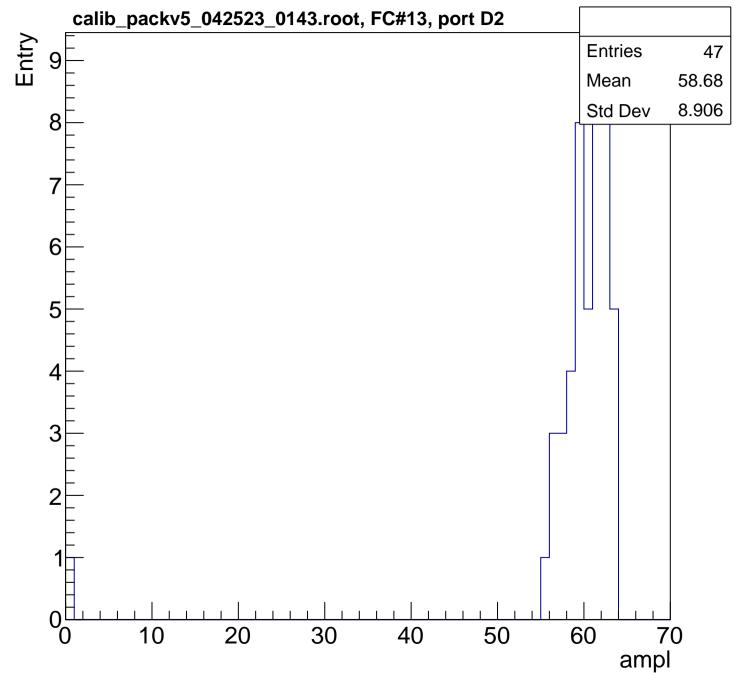


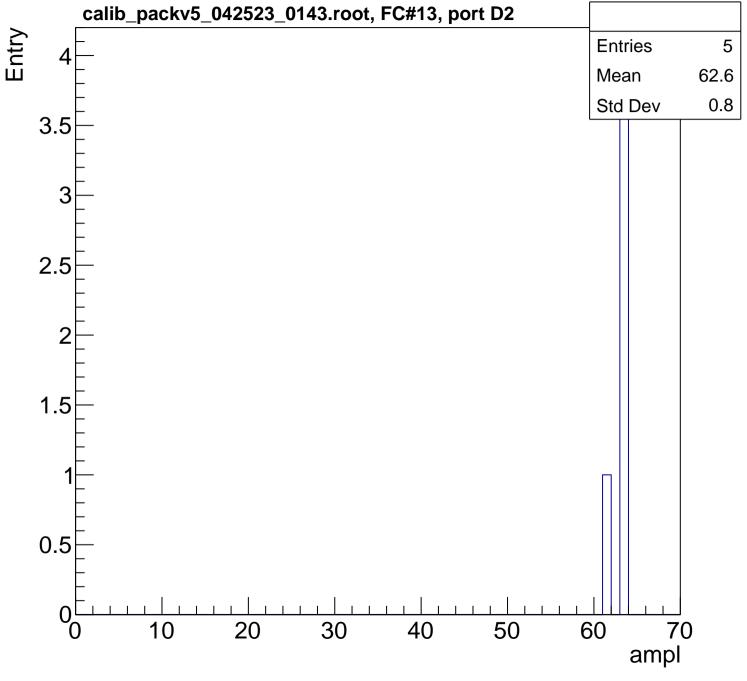


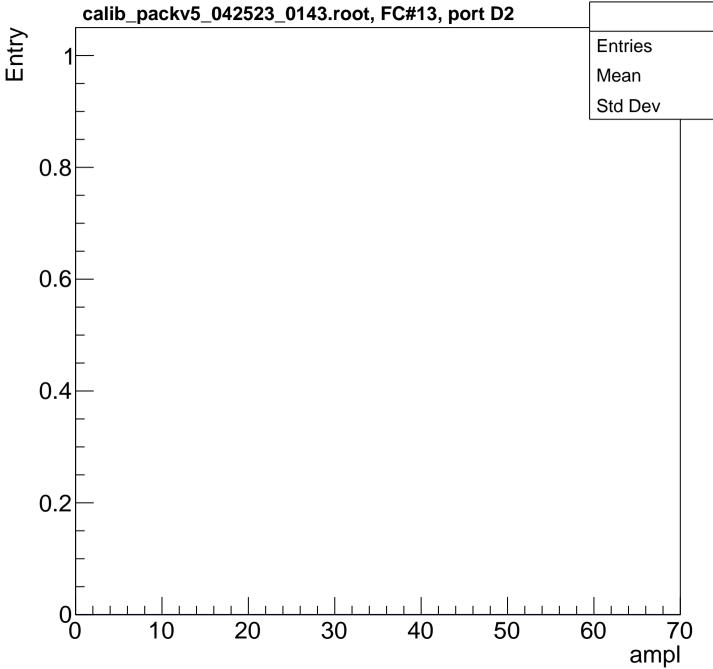


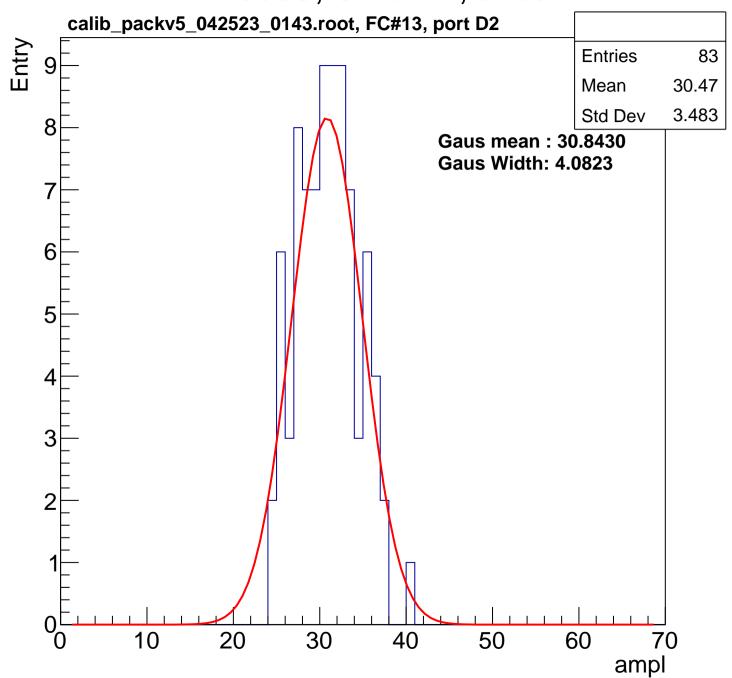


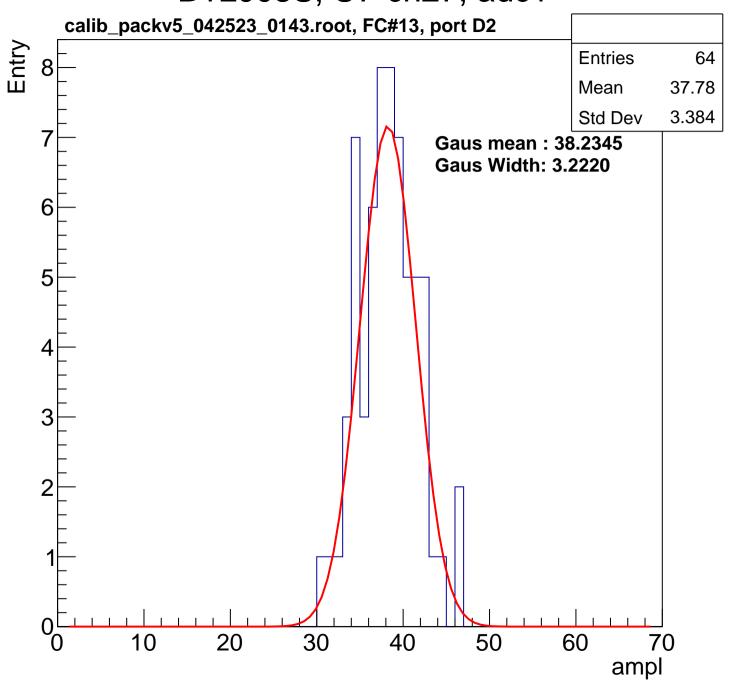


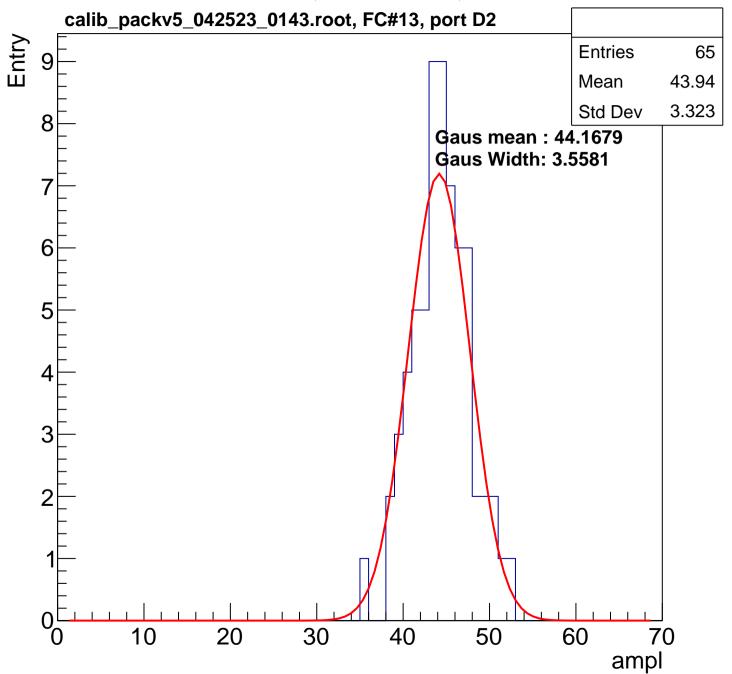


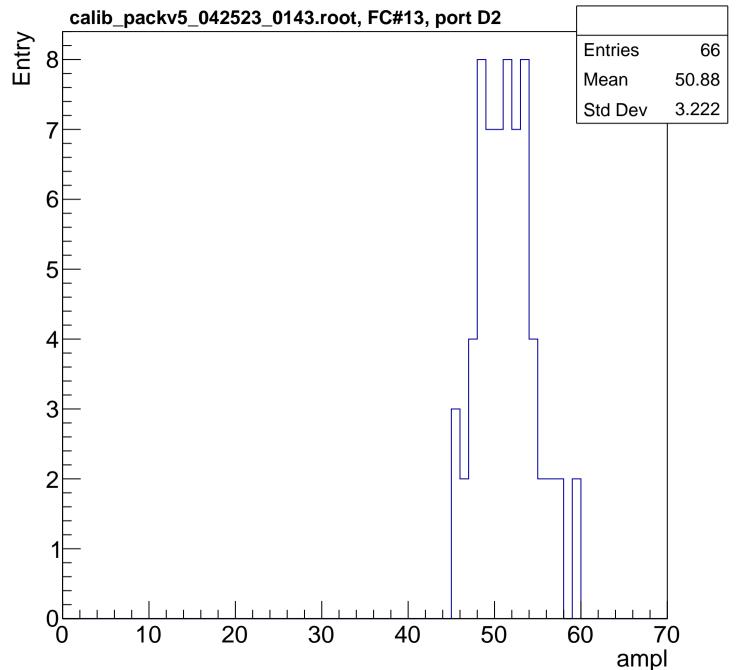


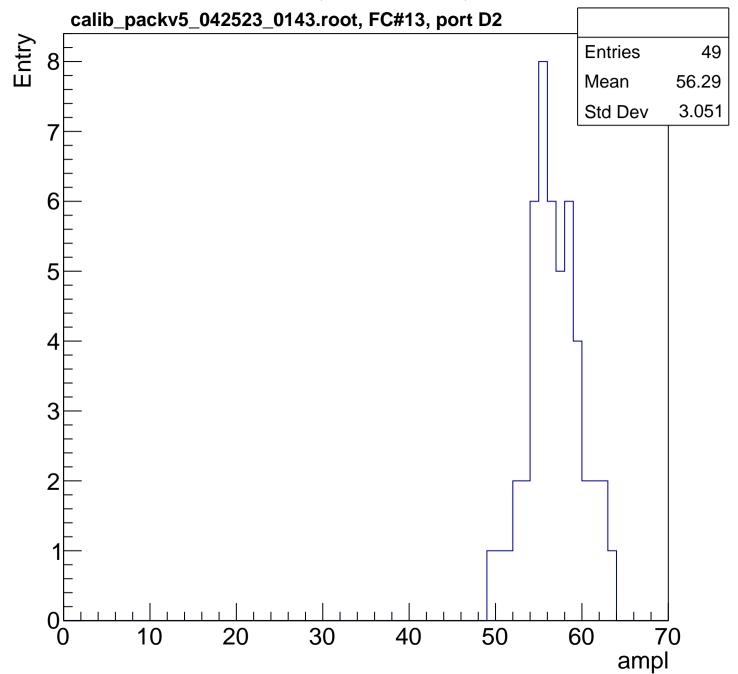


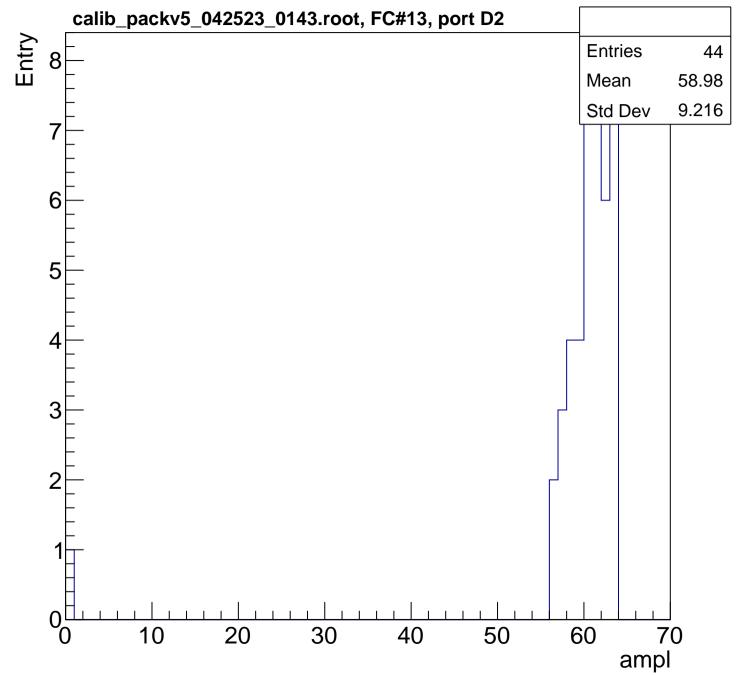


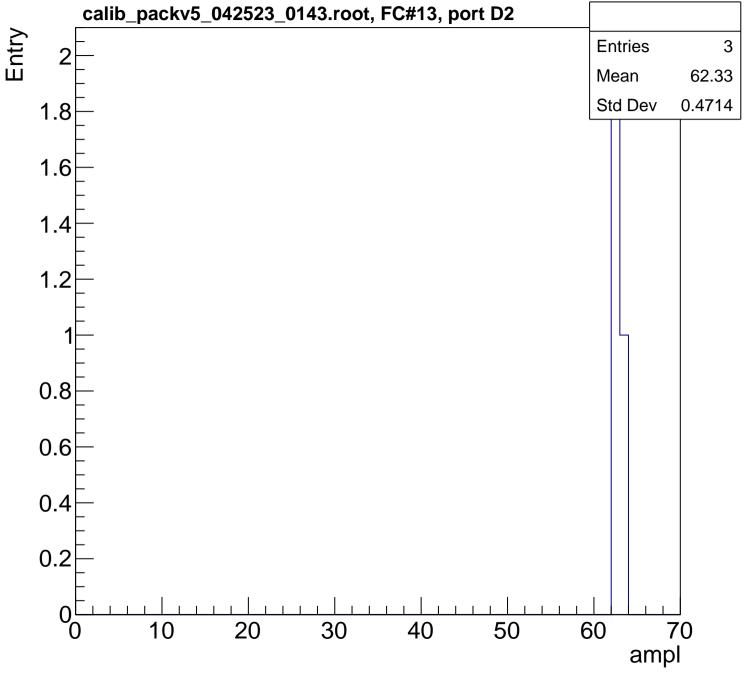




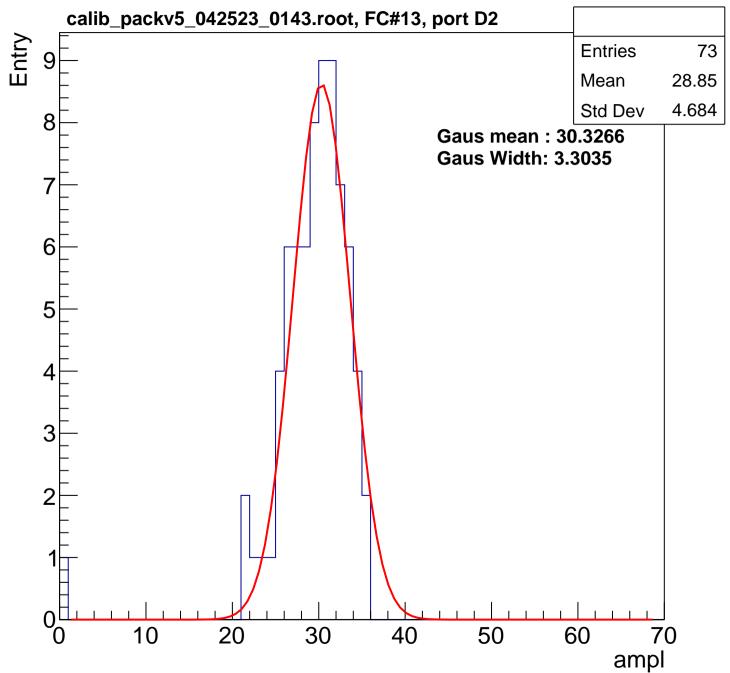


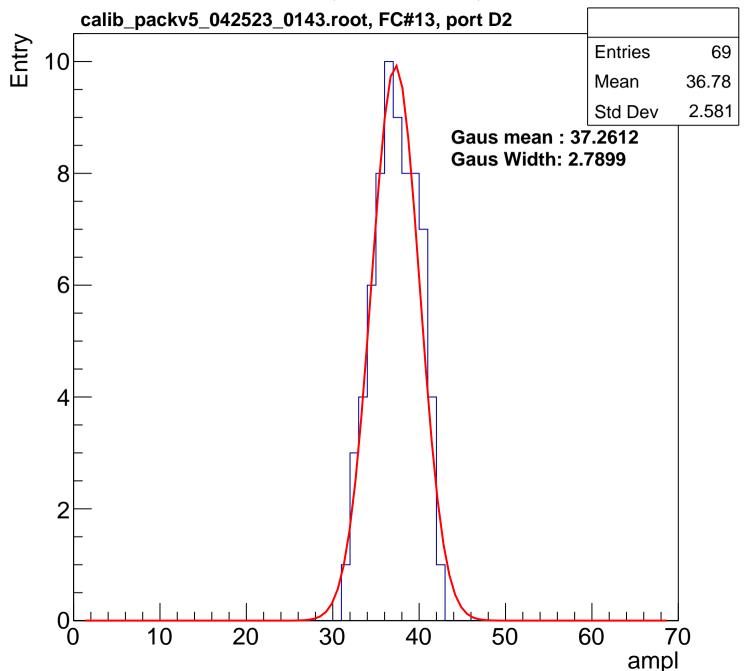


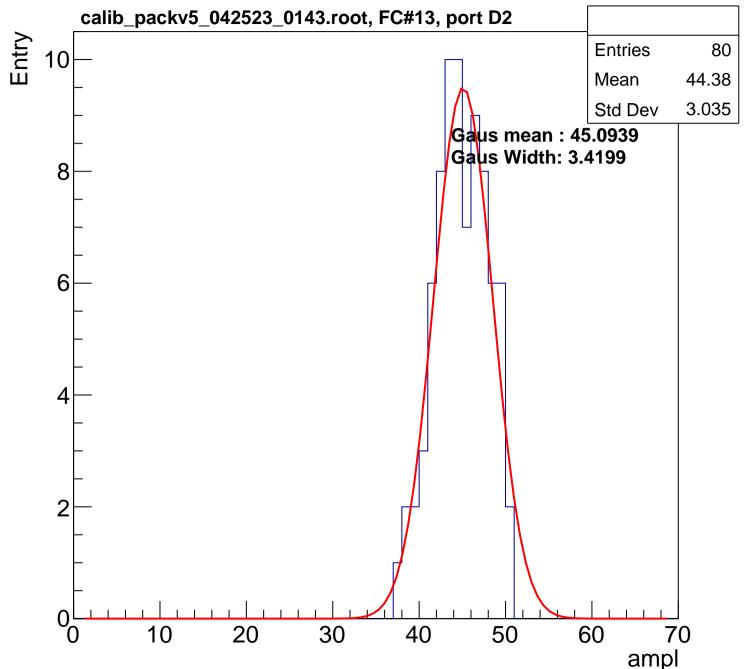


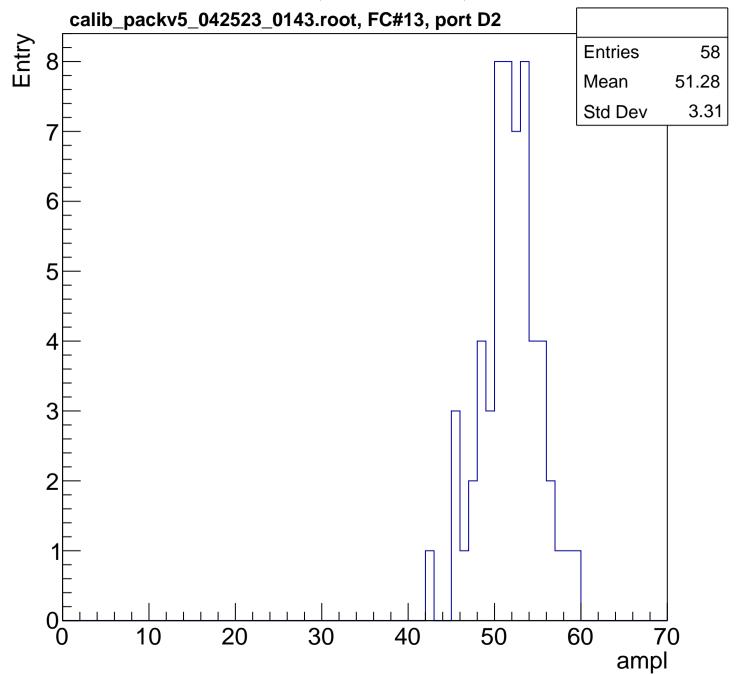


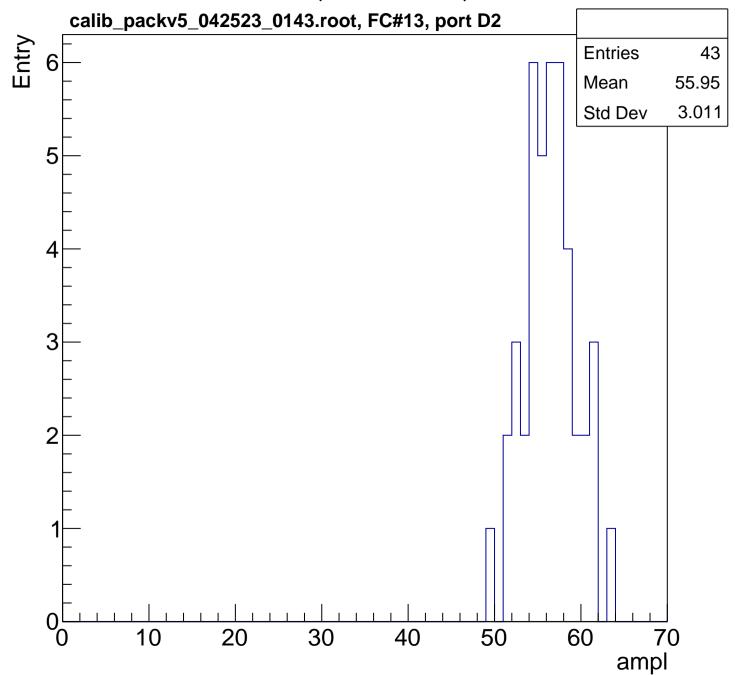
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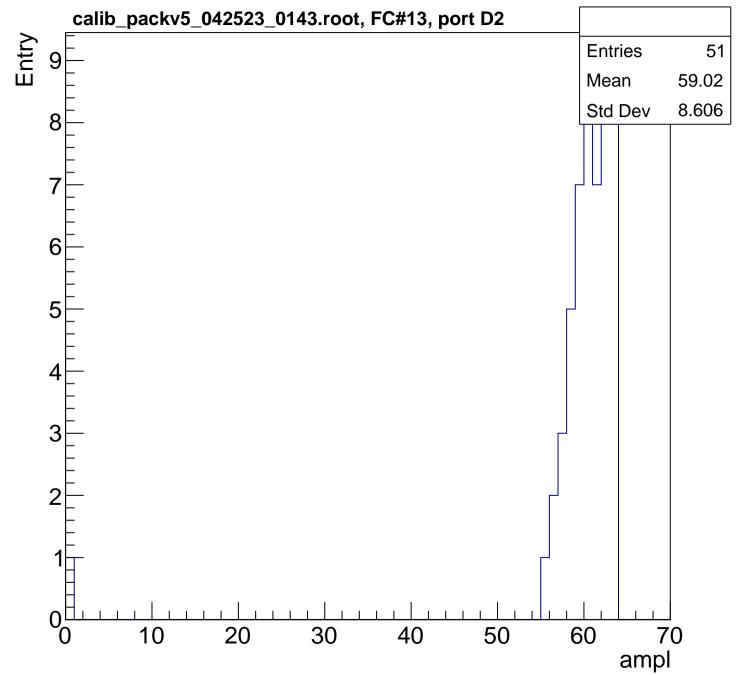


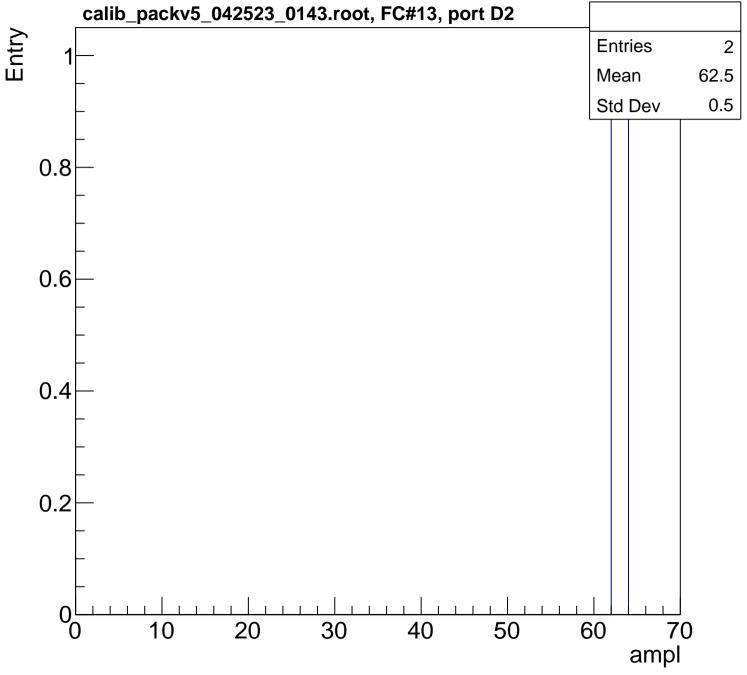




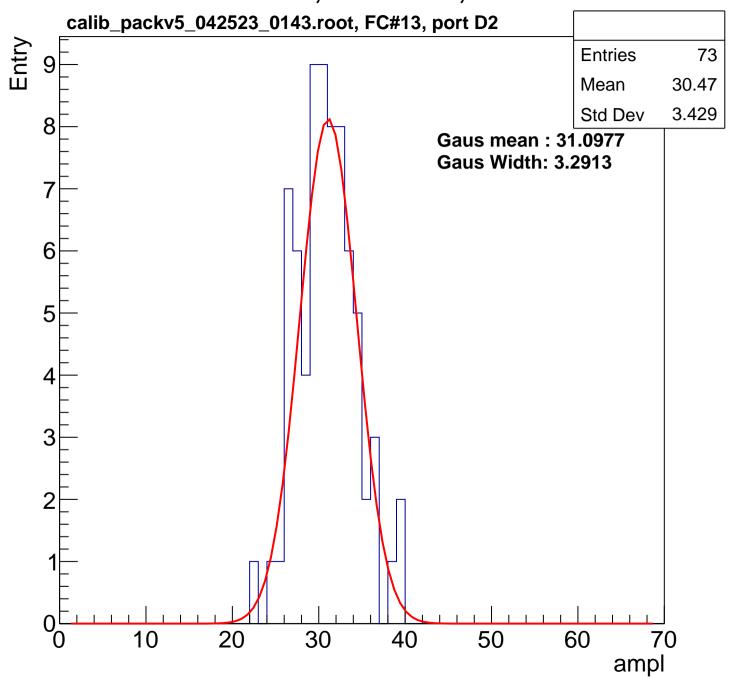


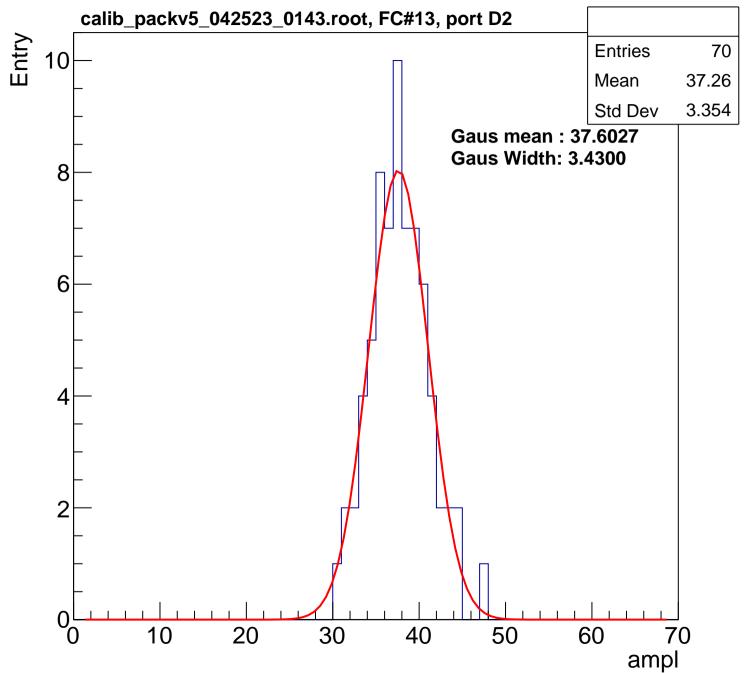


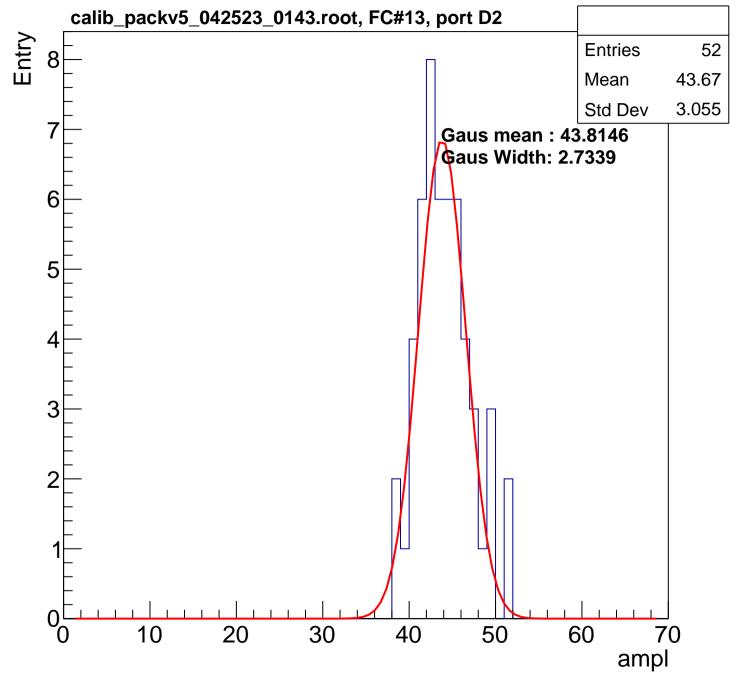


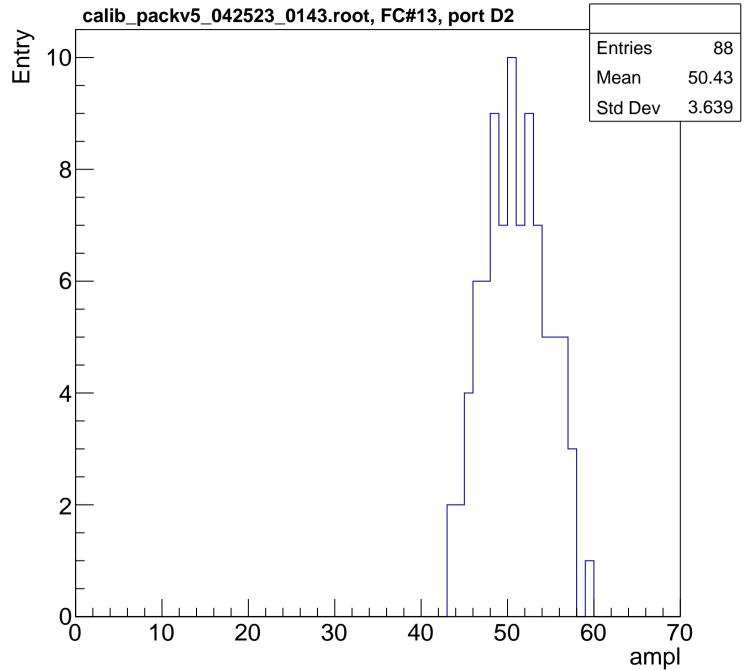


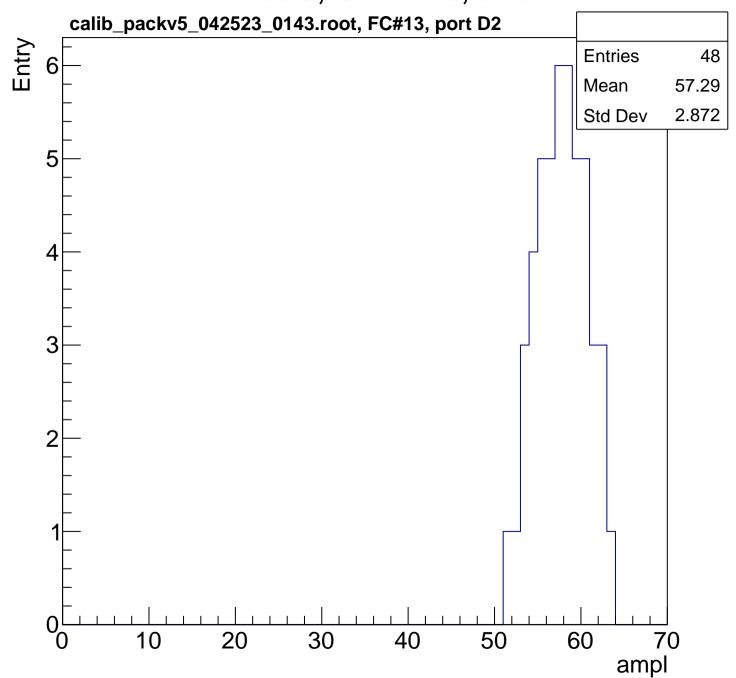
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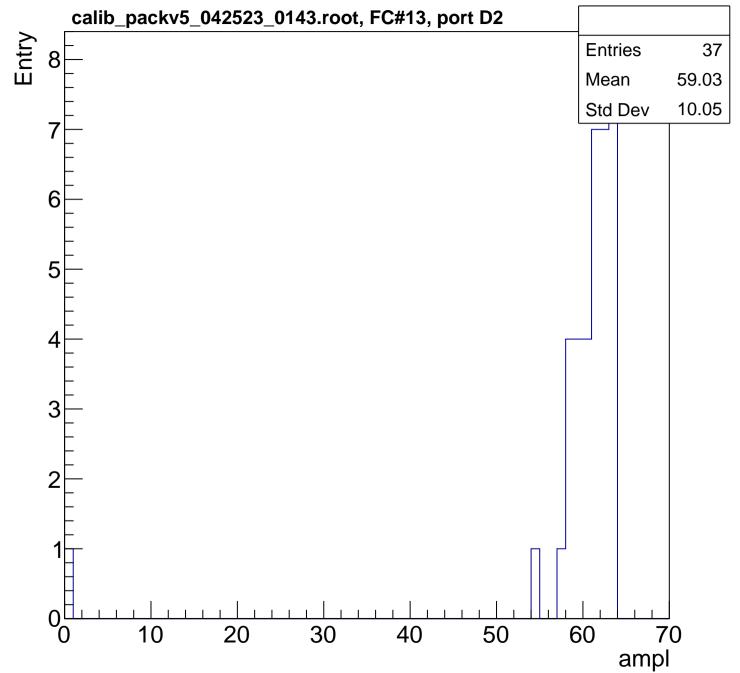


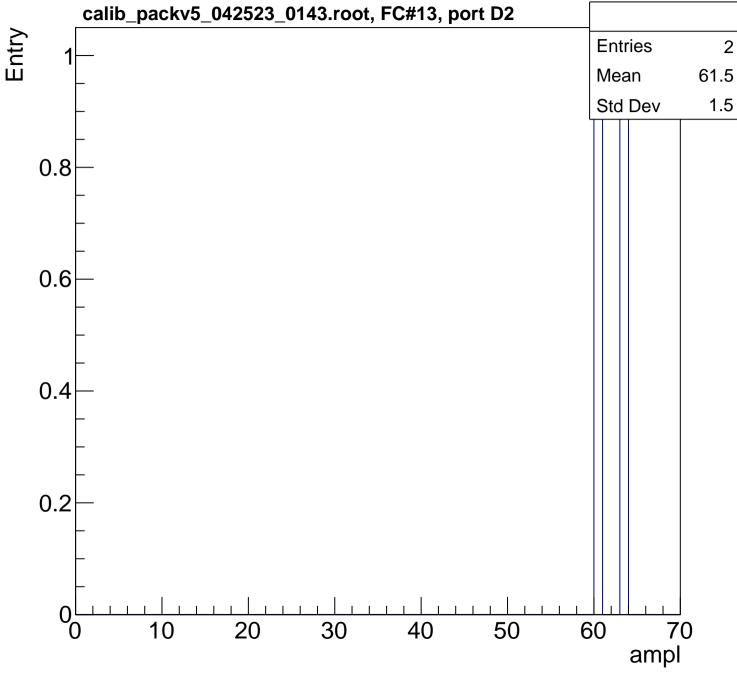




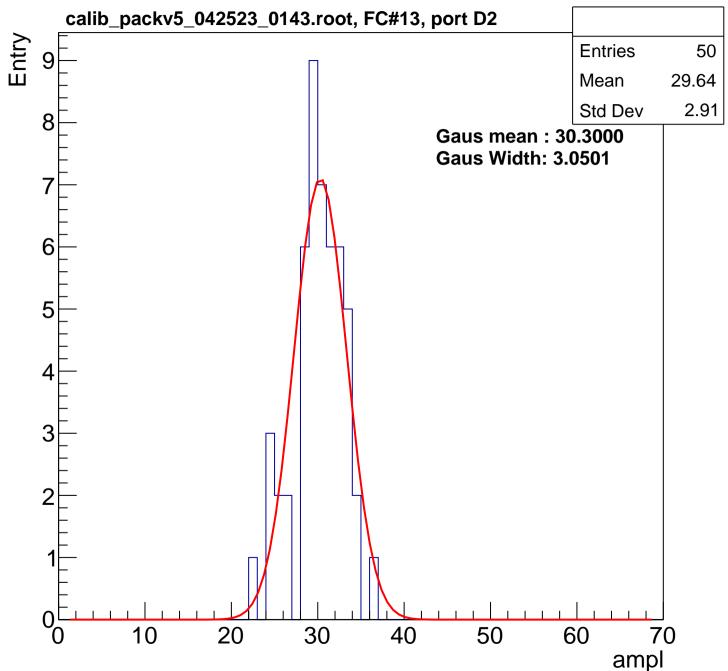


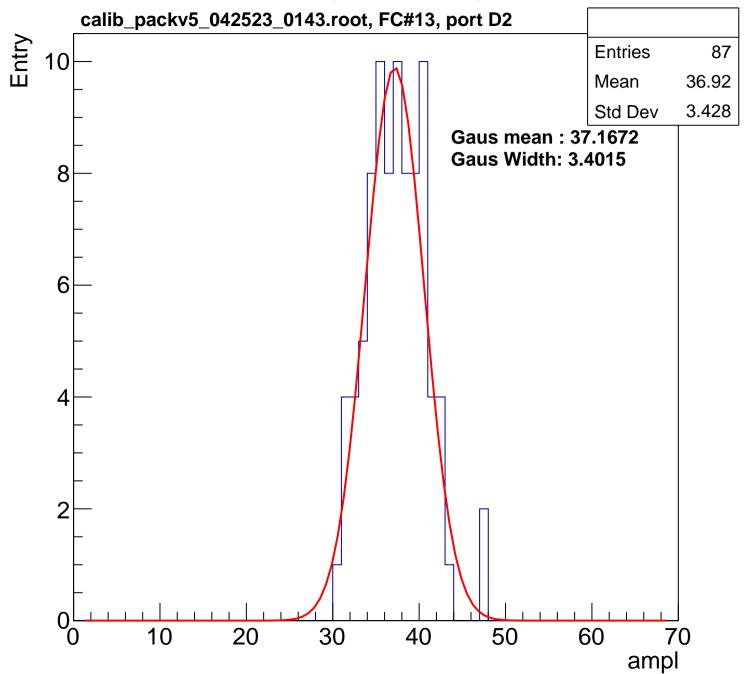


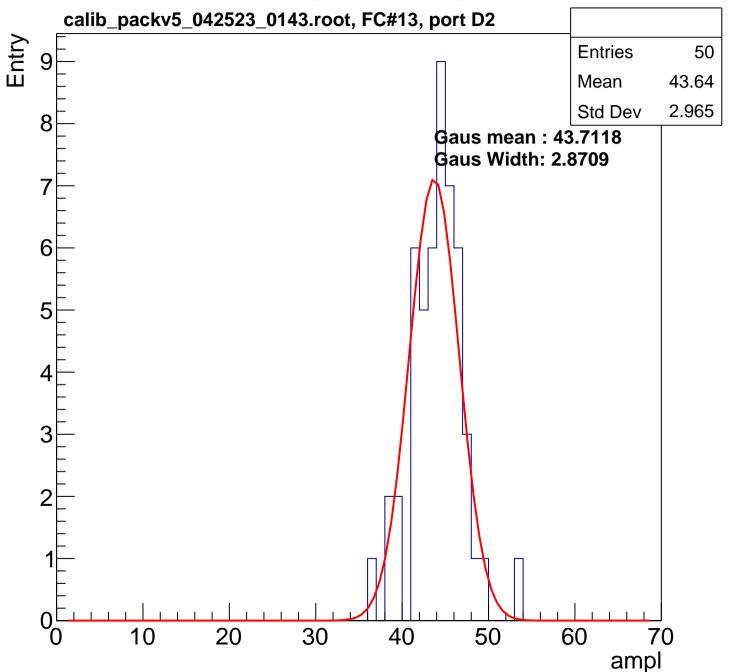


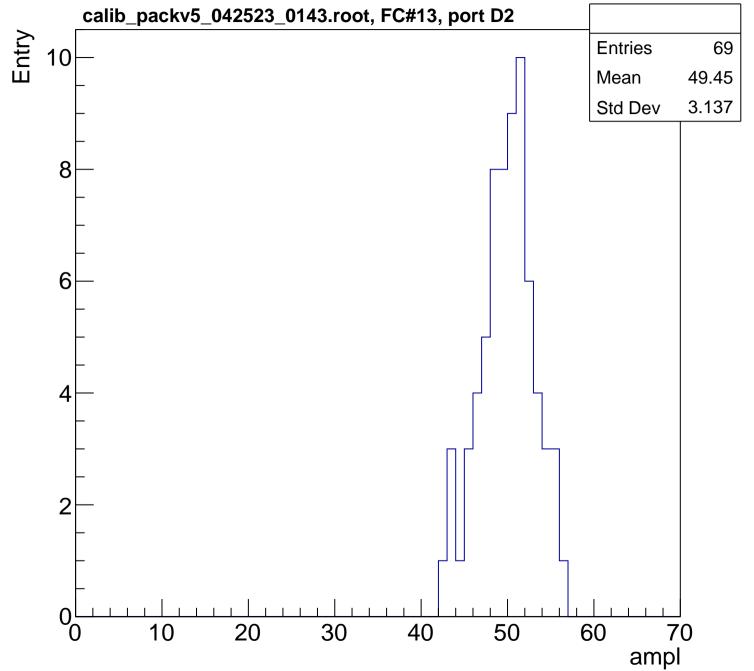


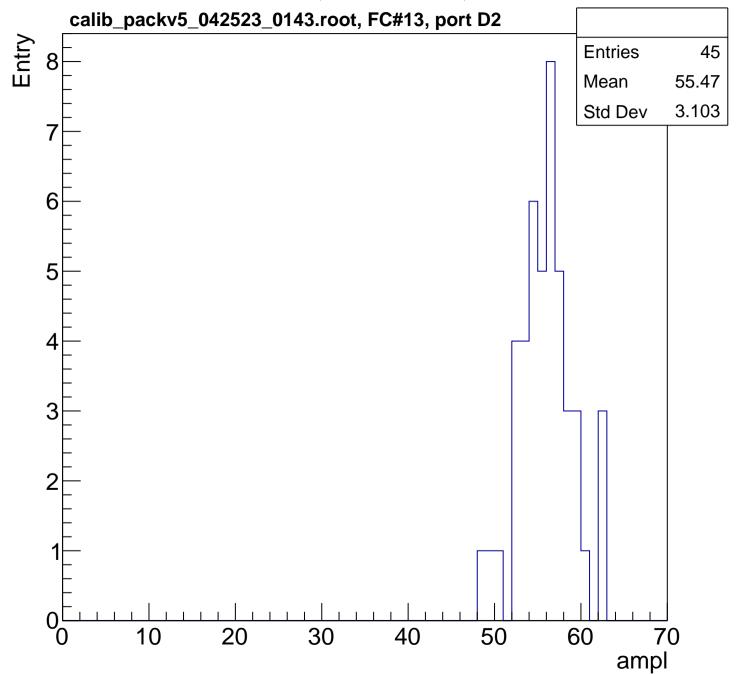


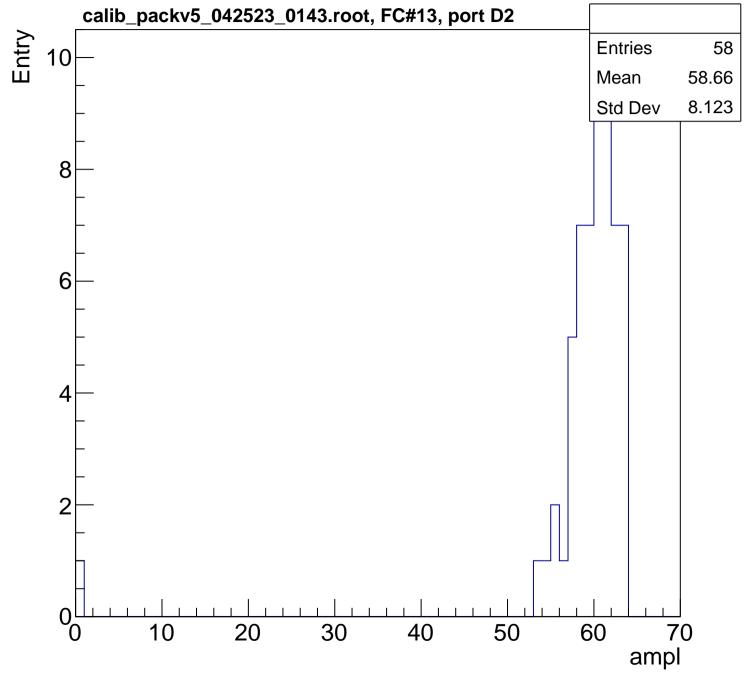


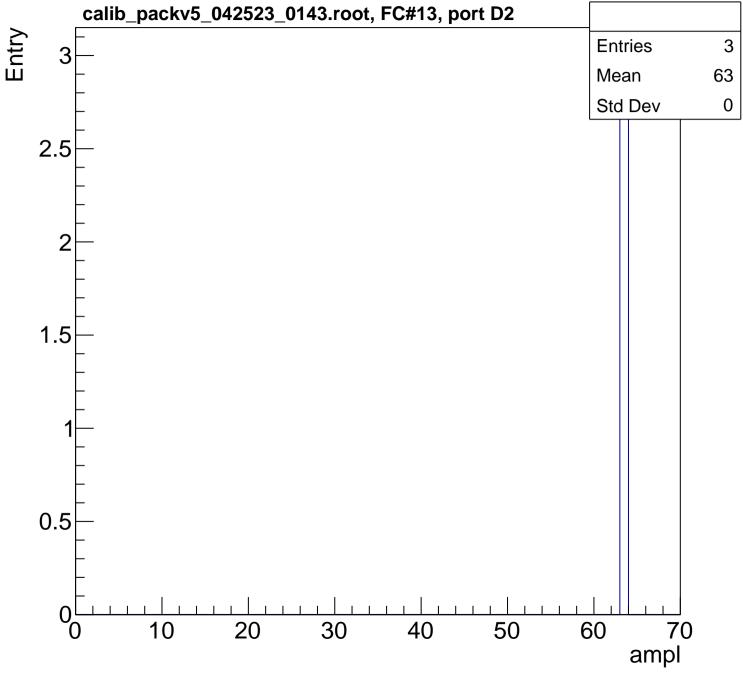




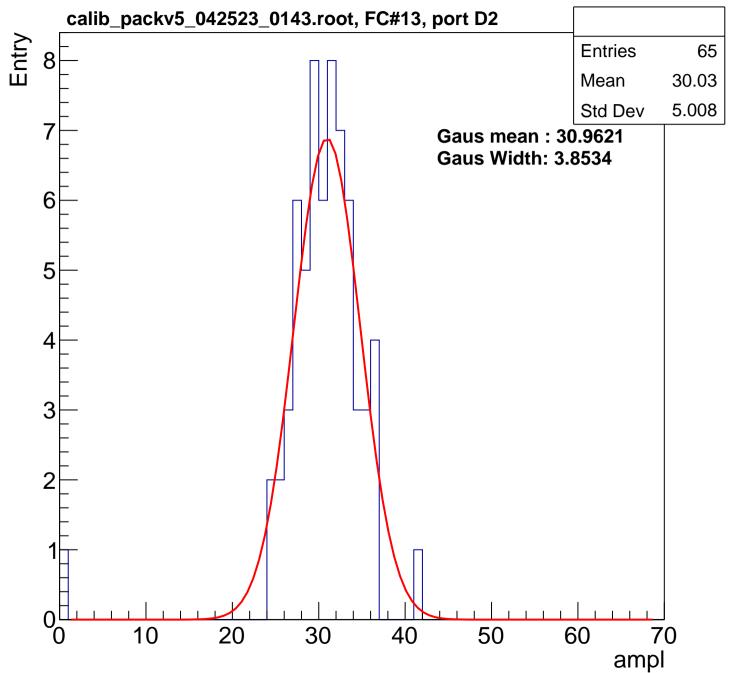


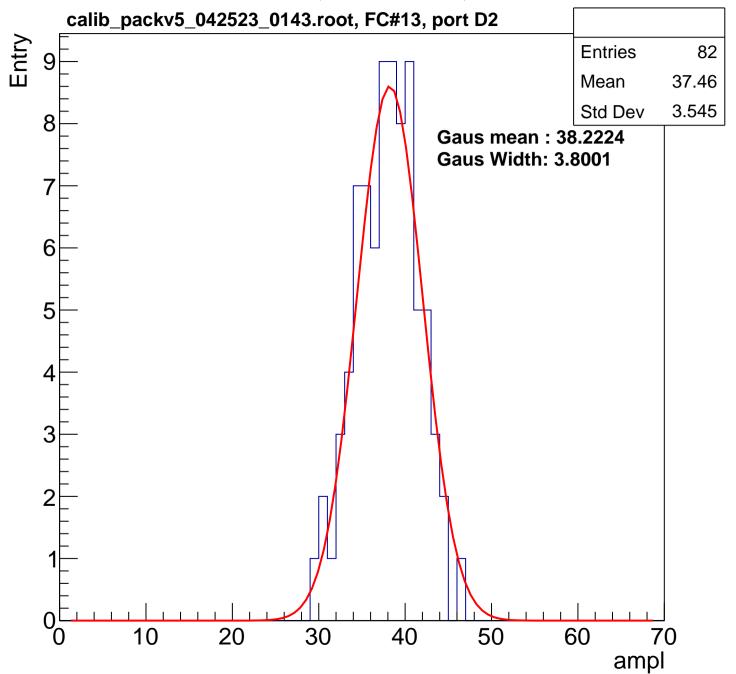


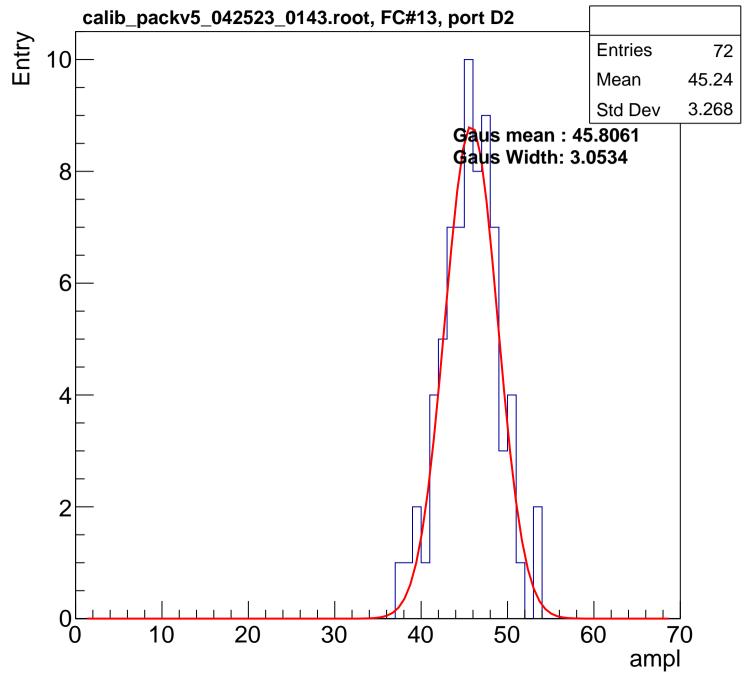


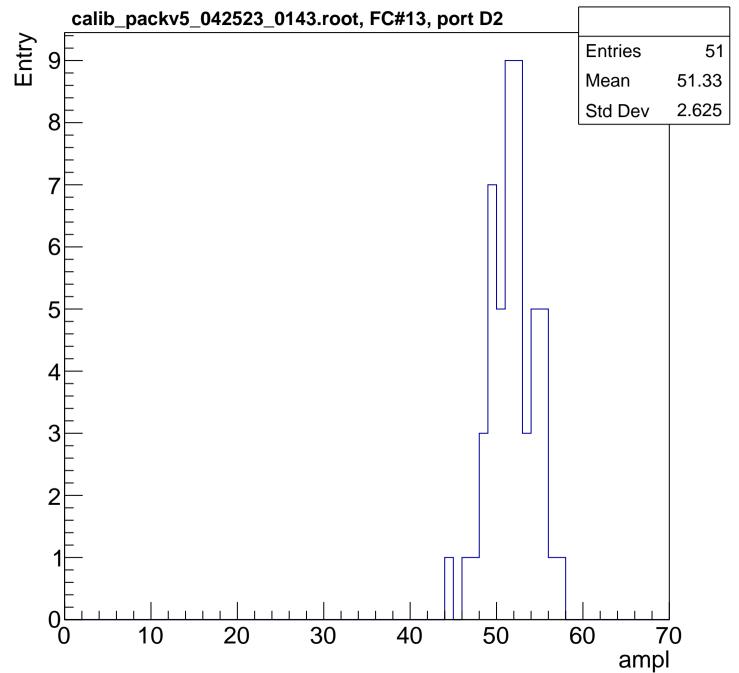


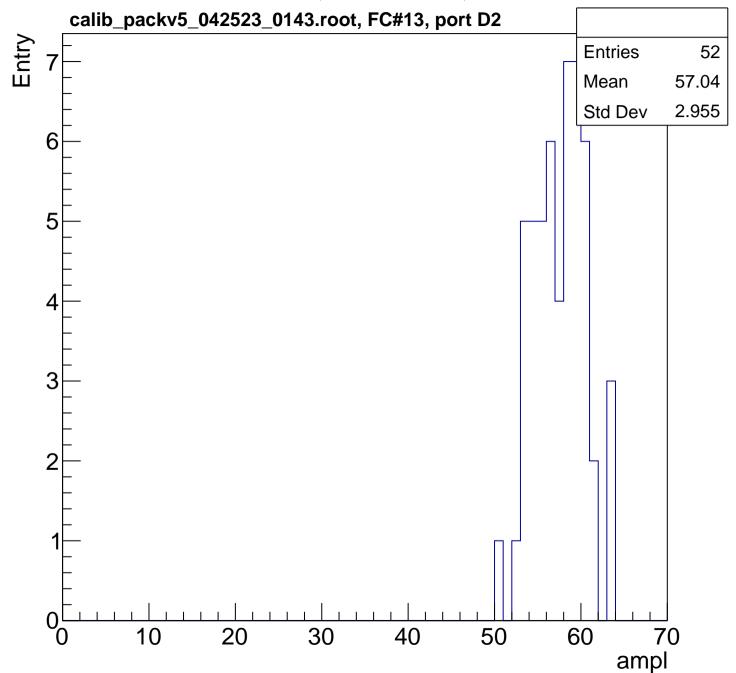


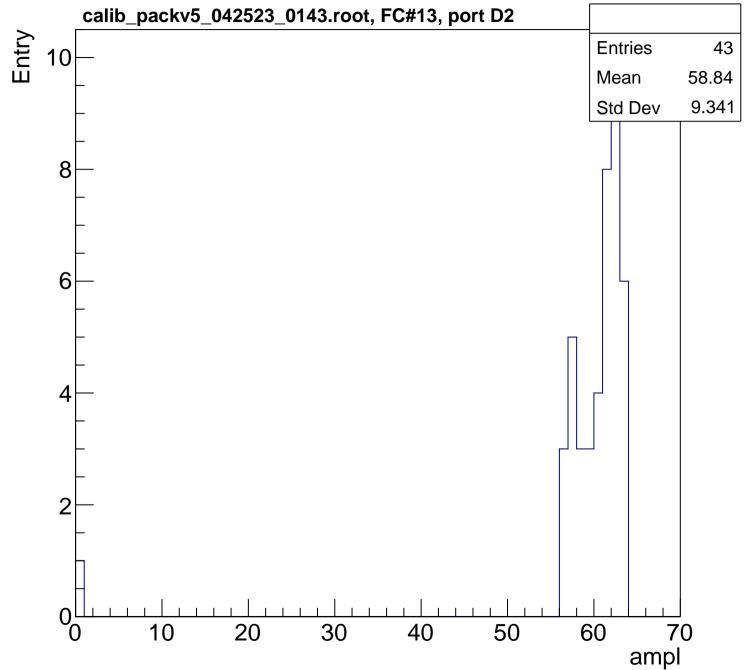


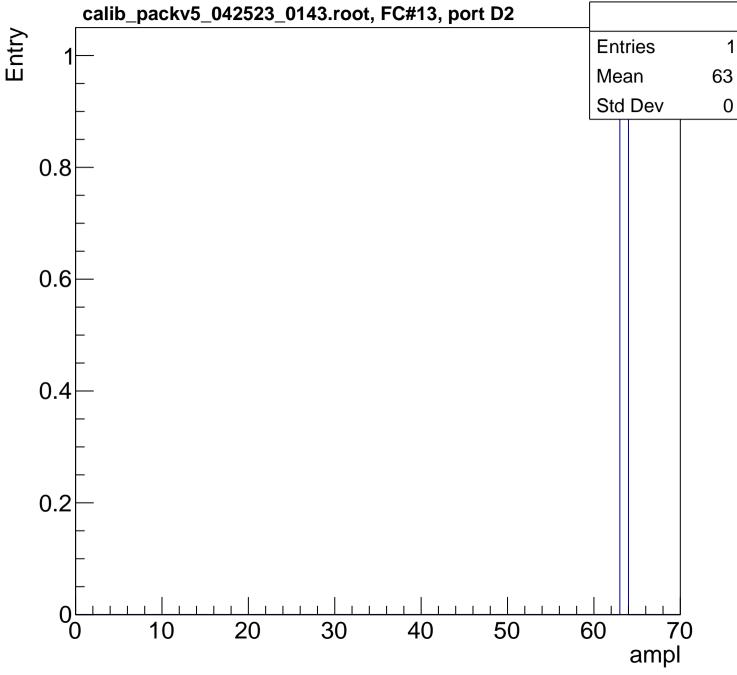


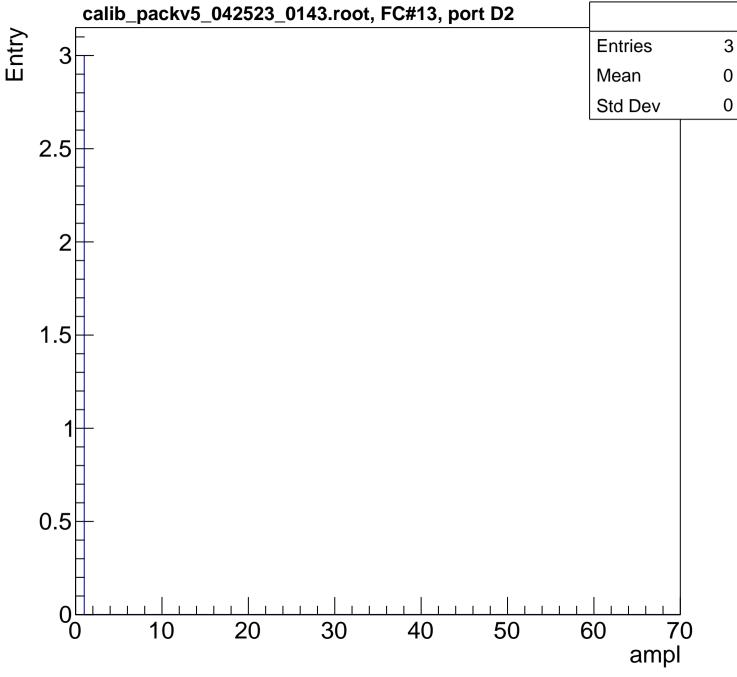


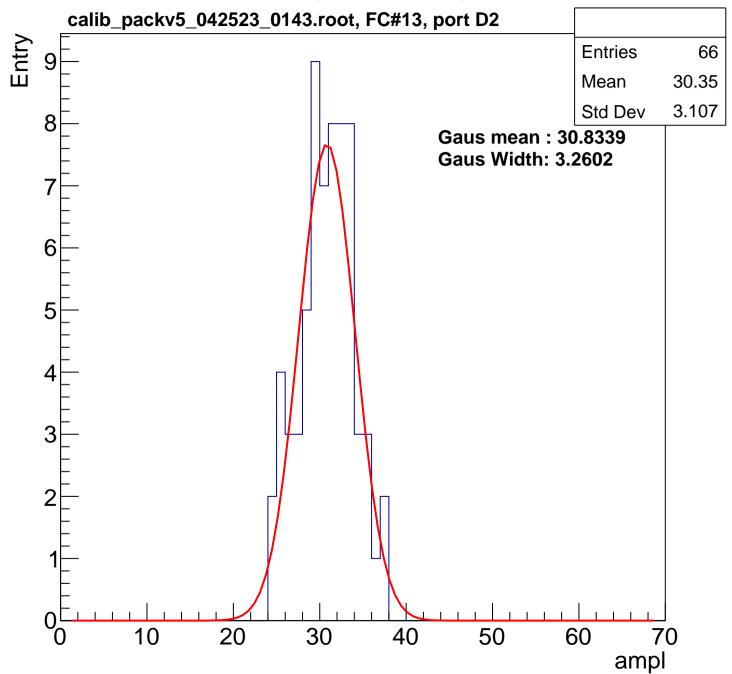


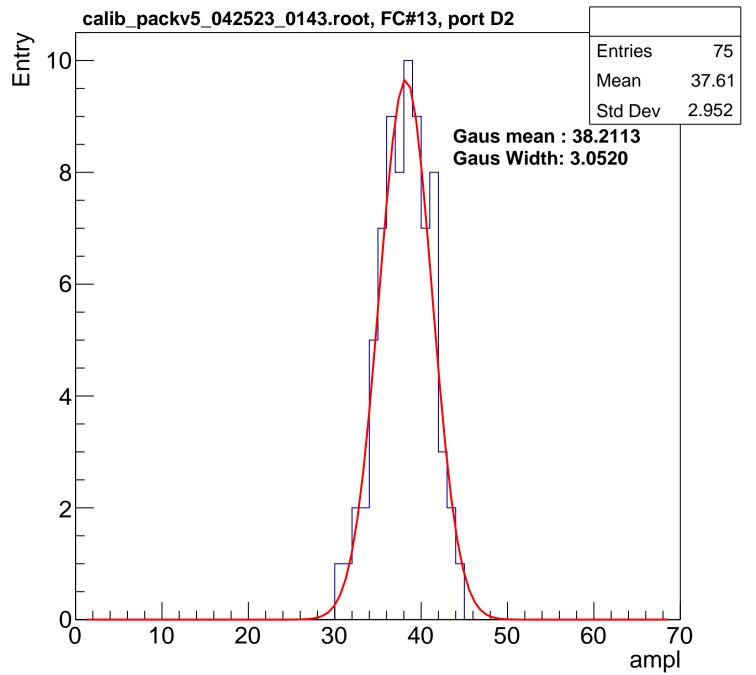


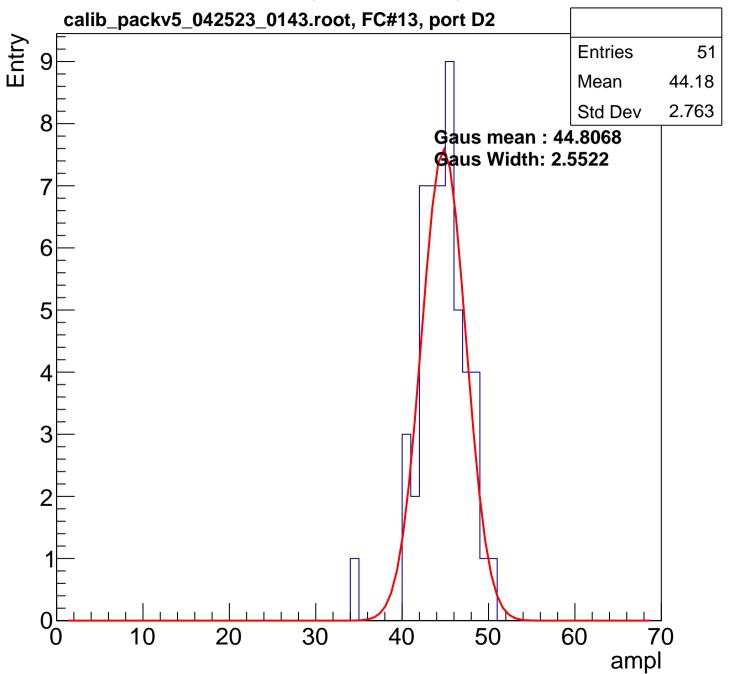


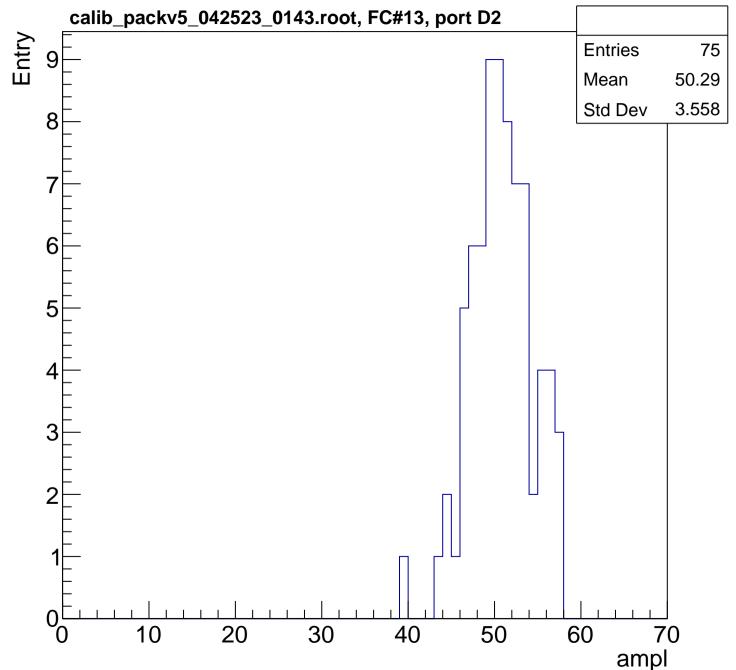


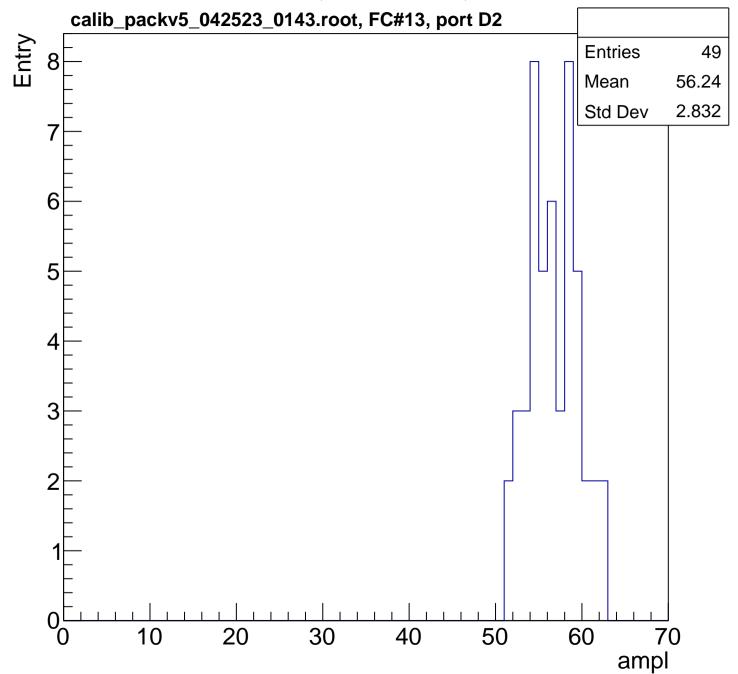


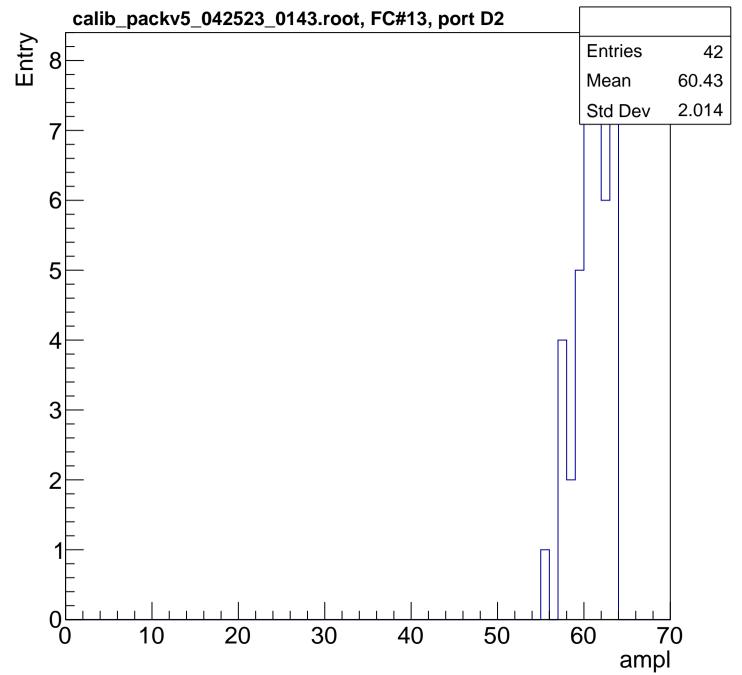


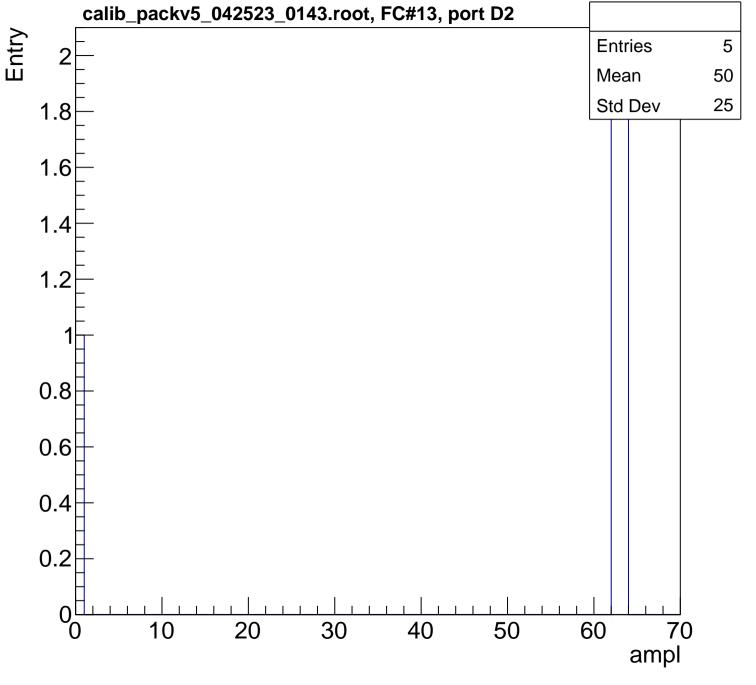




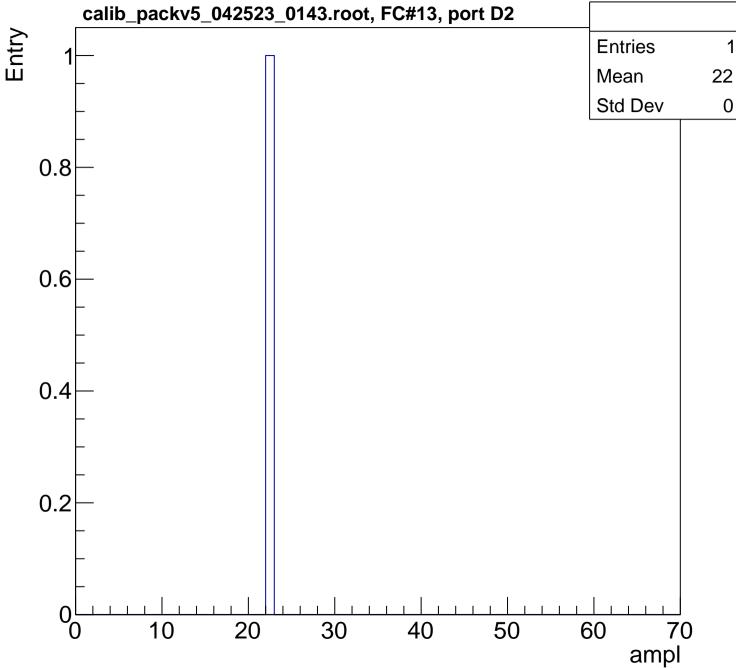


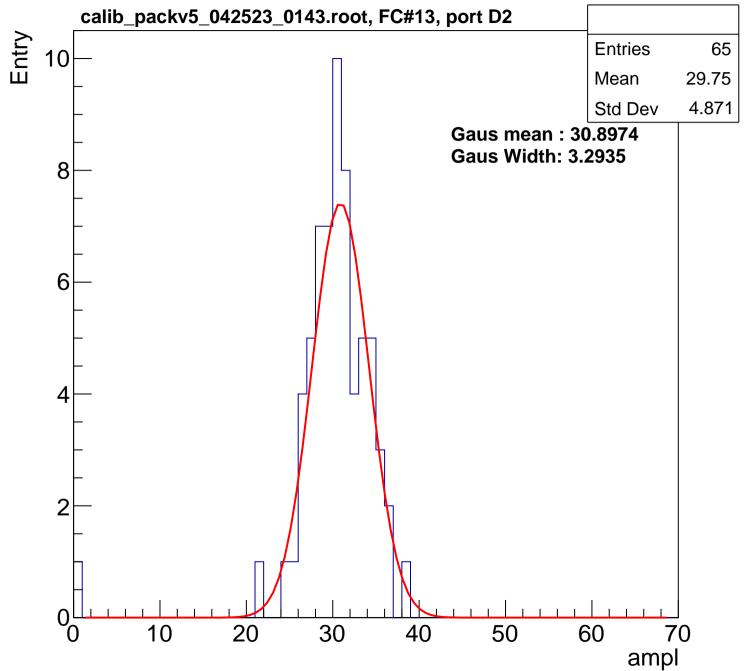


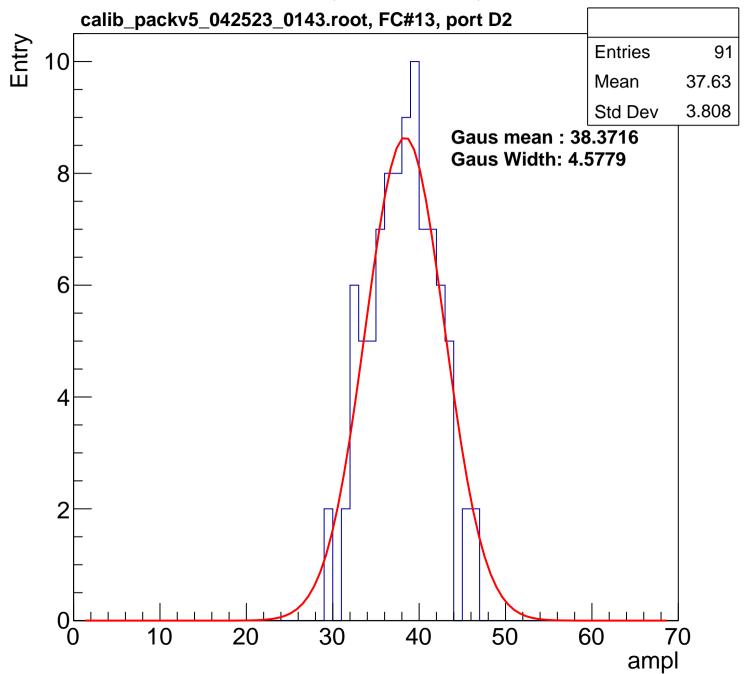


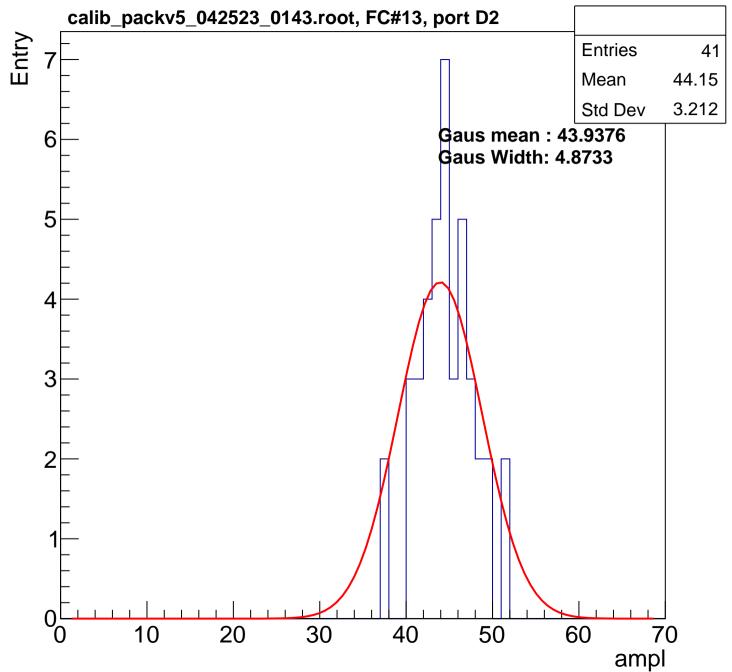


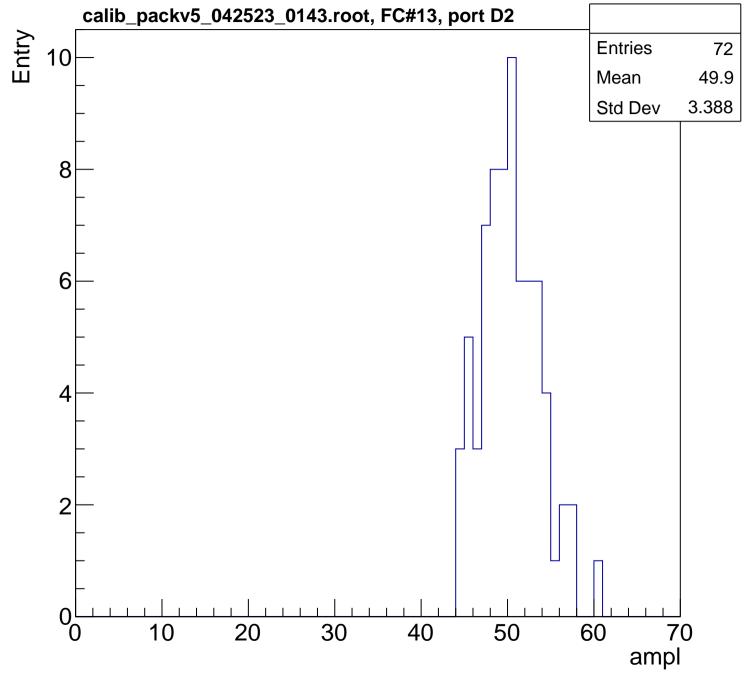
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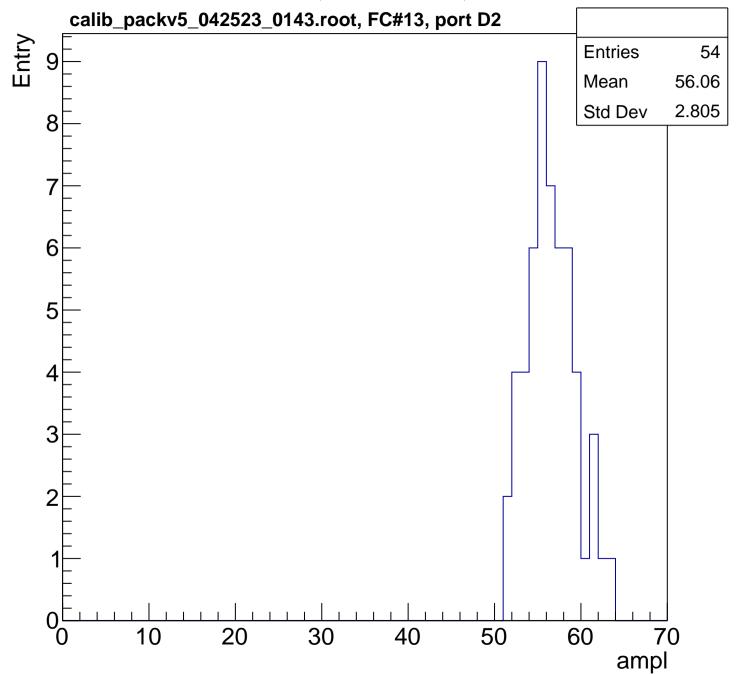


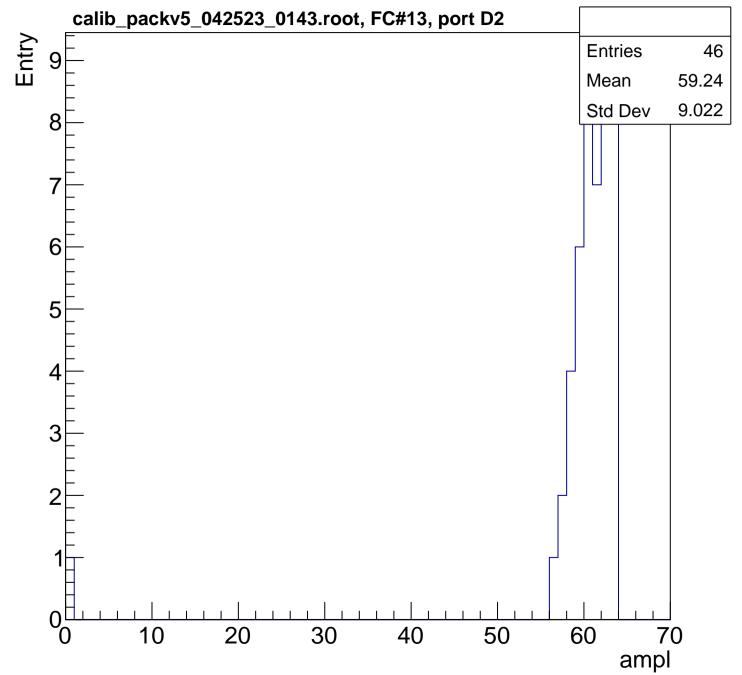


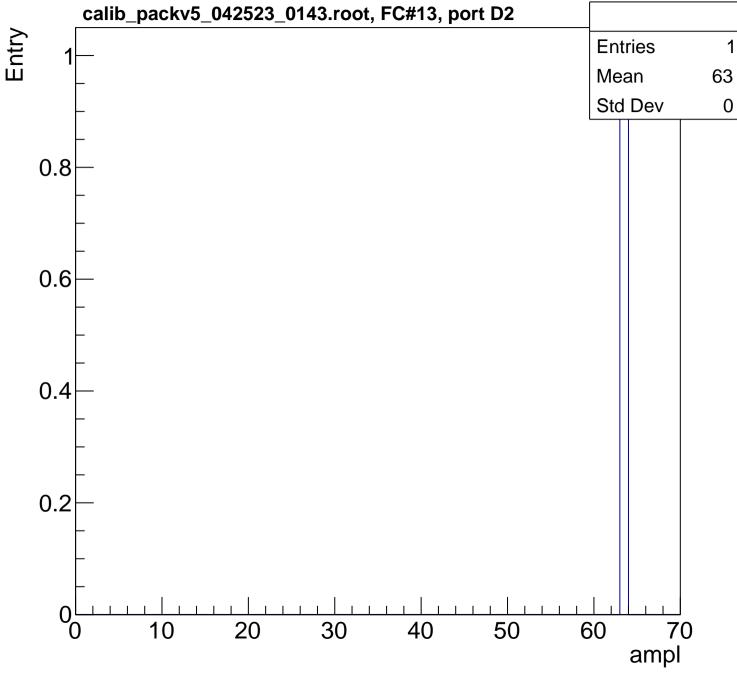


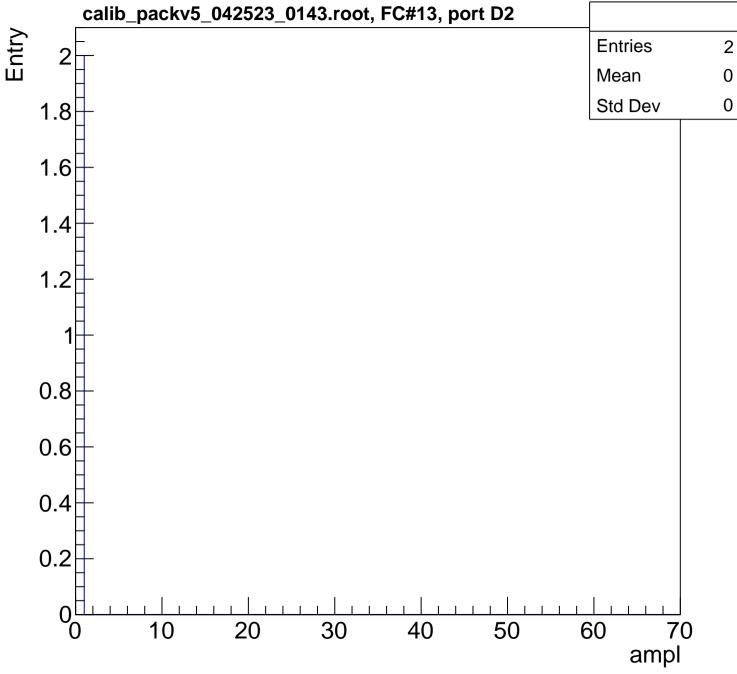


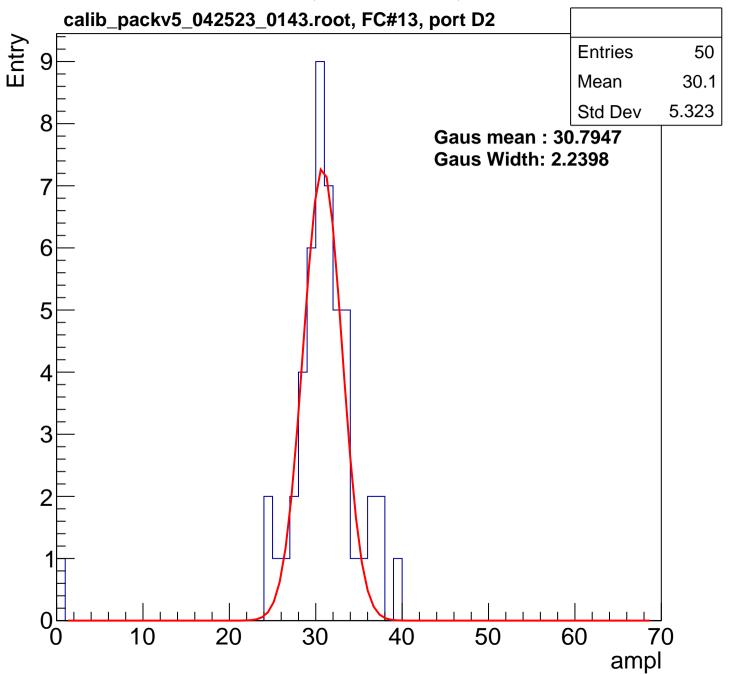


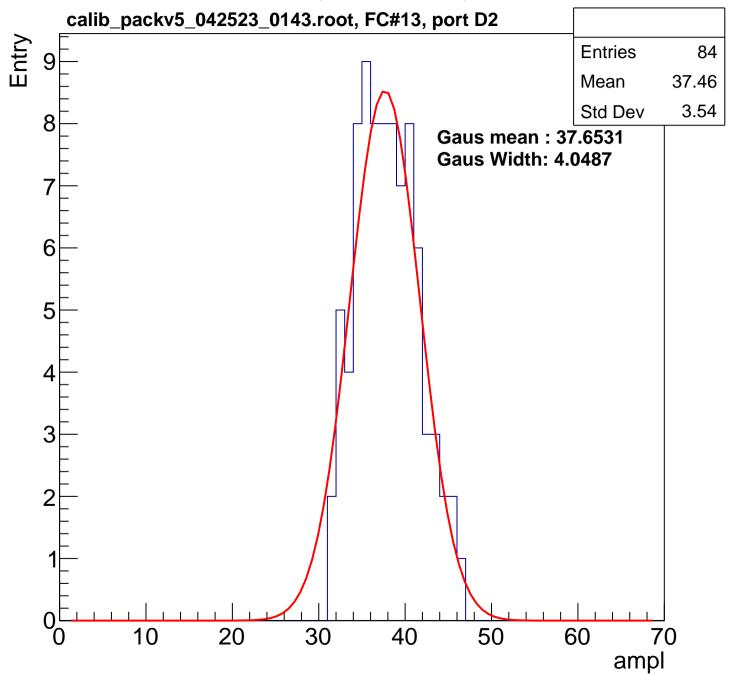


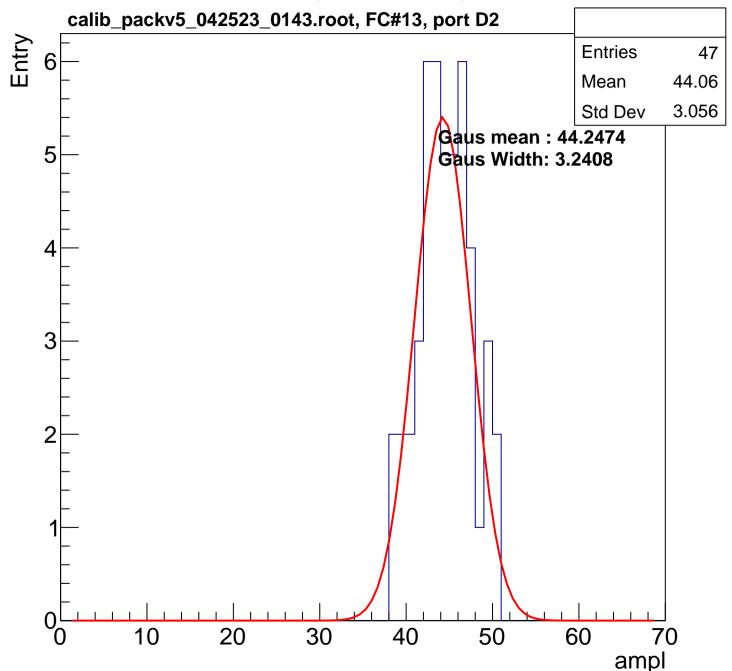


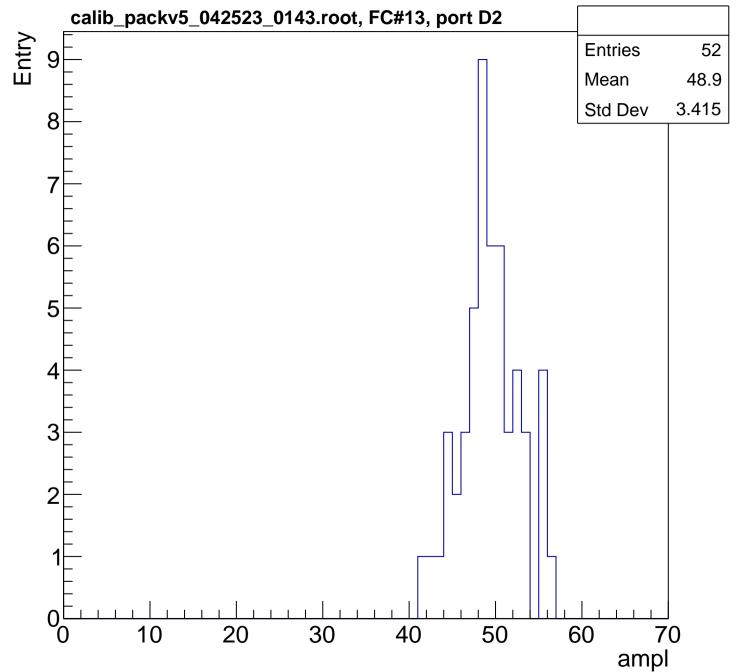


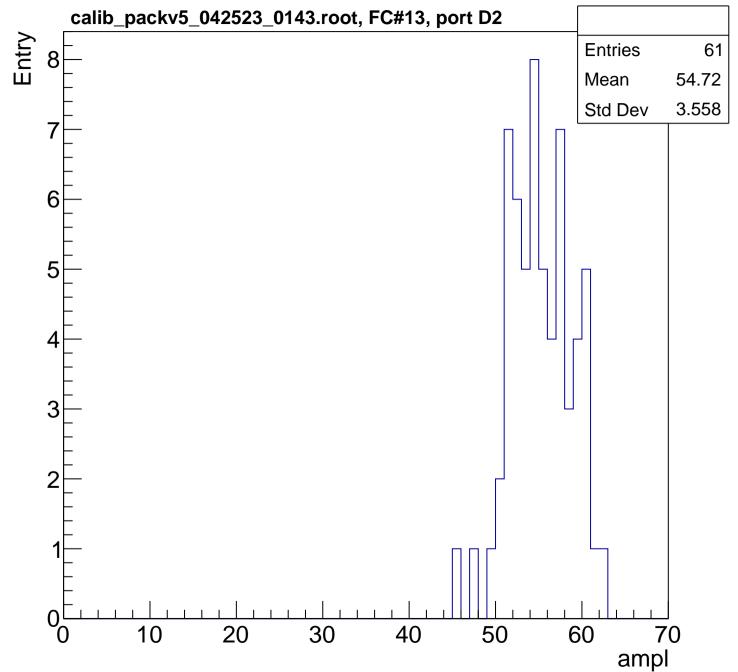


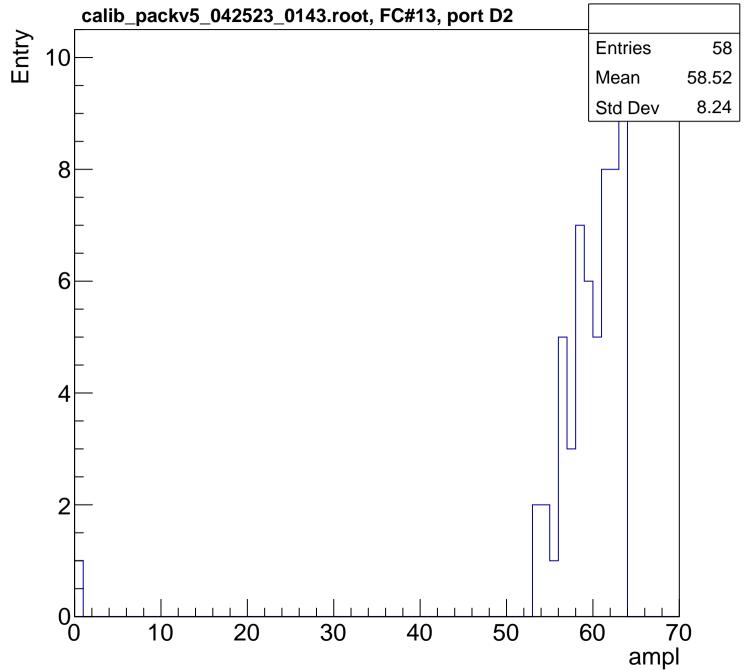


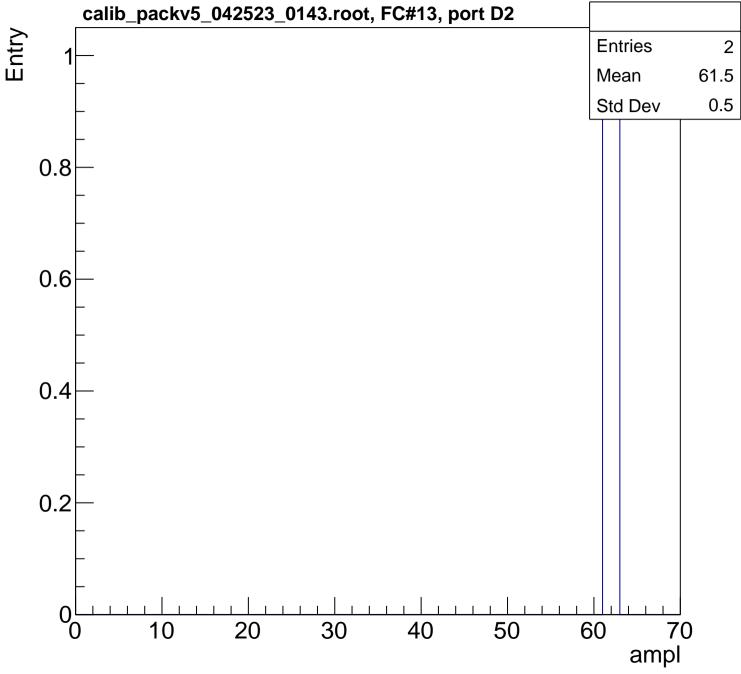




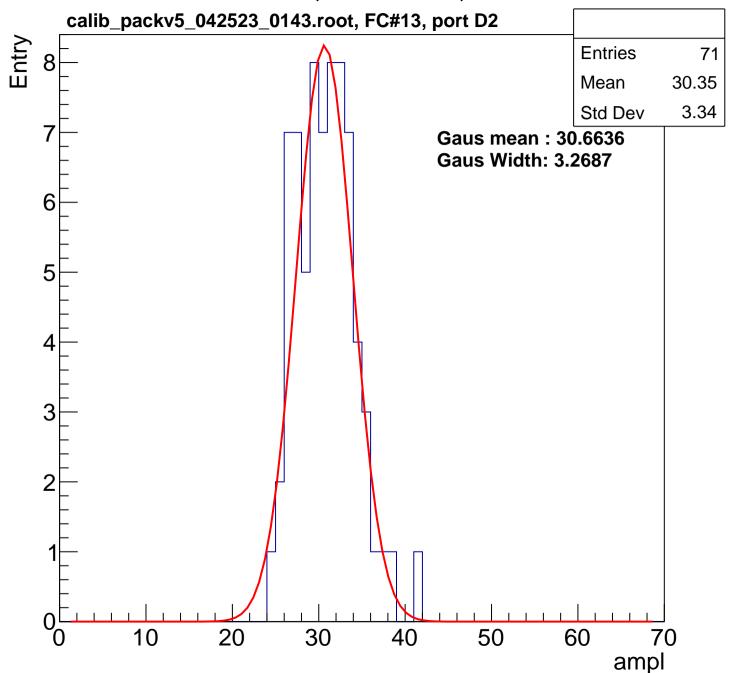


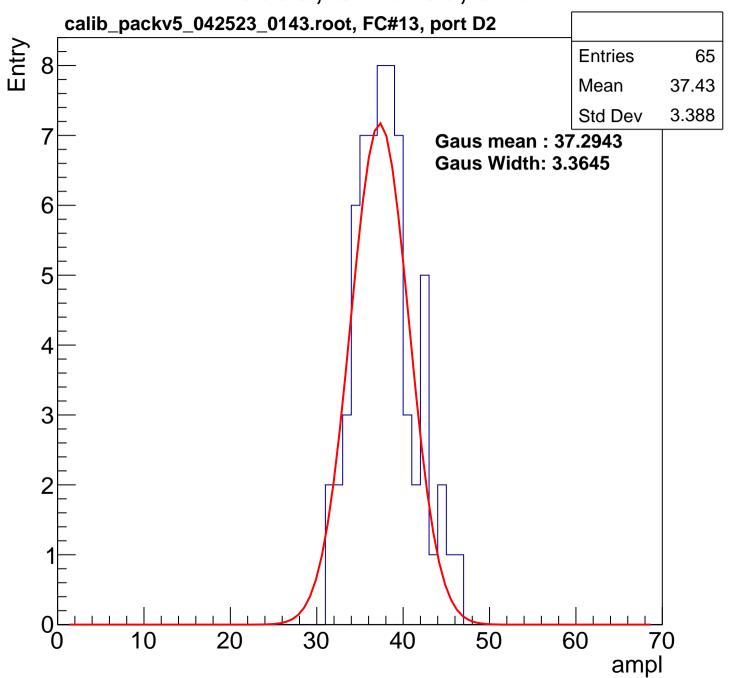


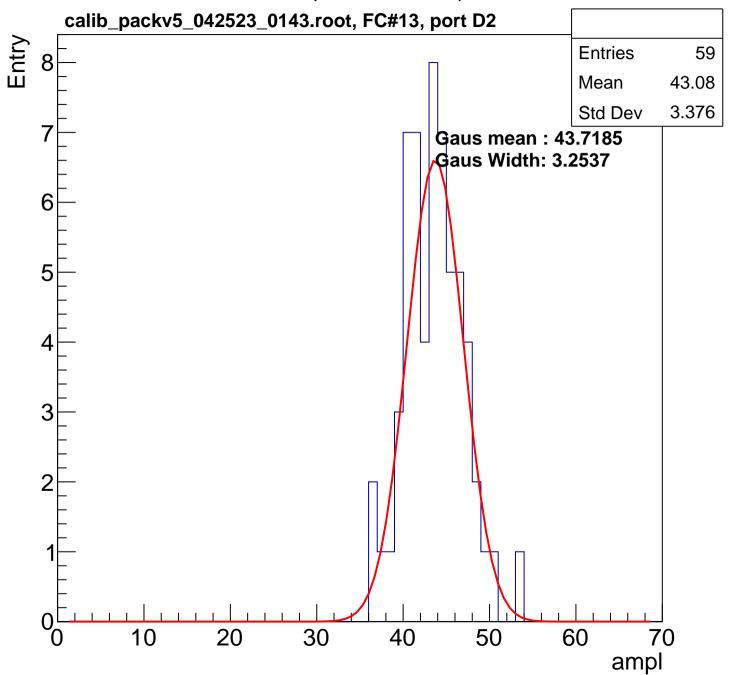


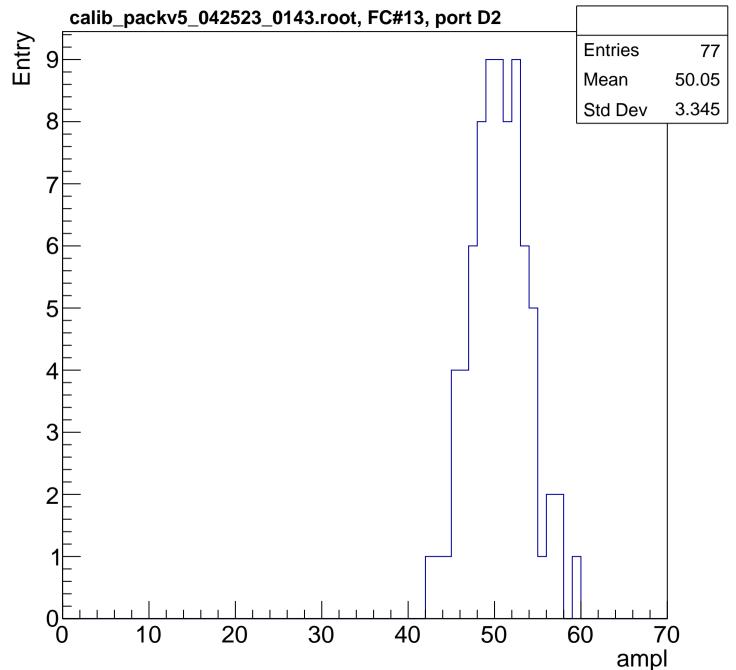


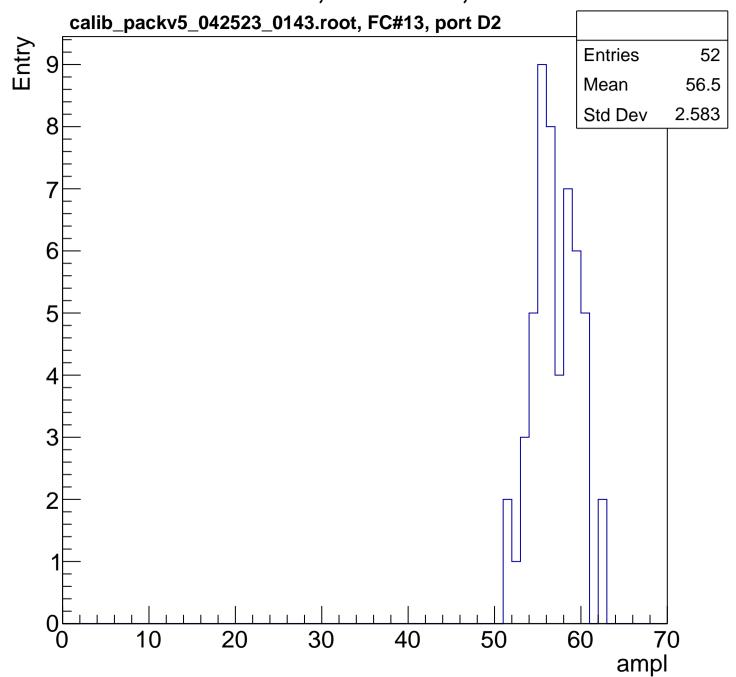
B1L003S, U7-ch34, adc7 calib_packv5_042523_0143.root, FC#13, port D2 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

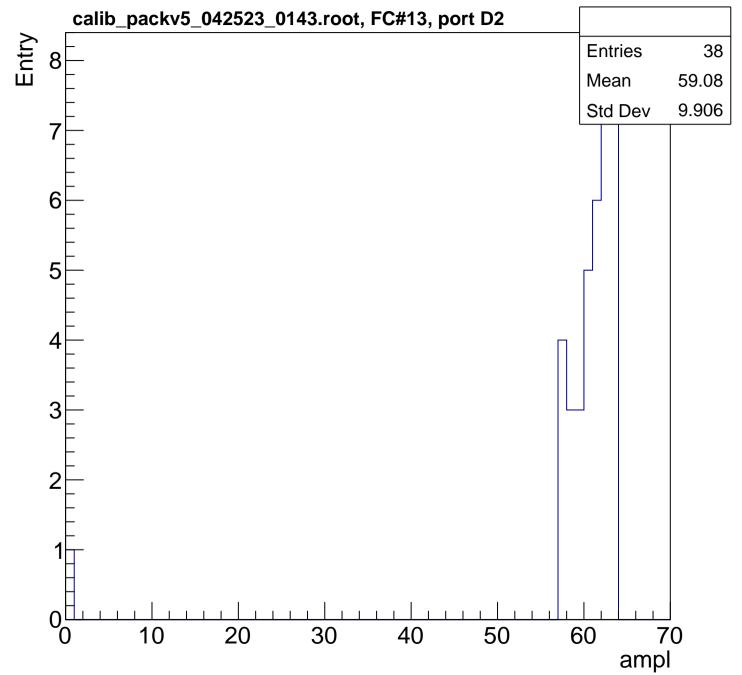


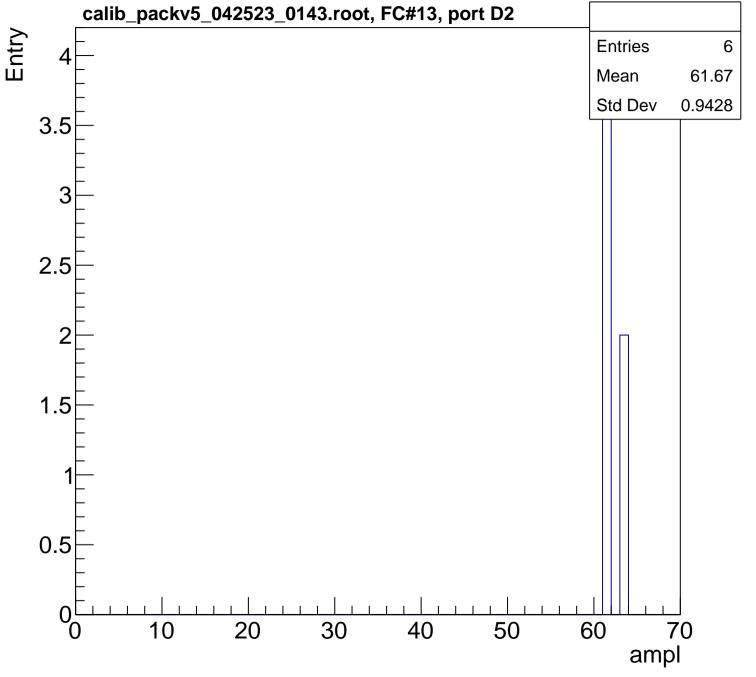




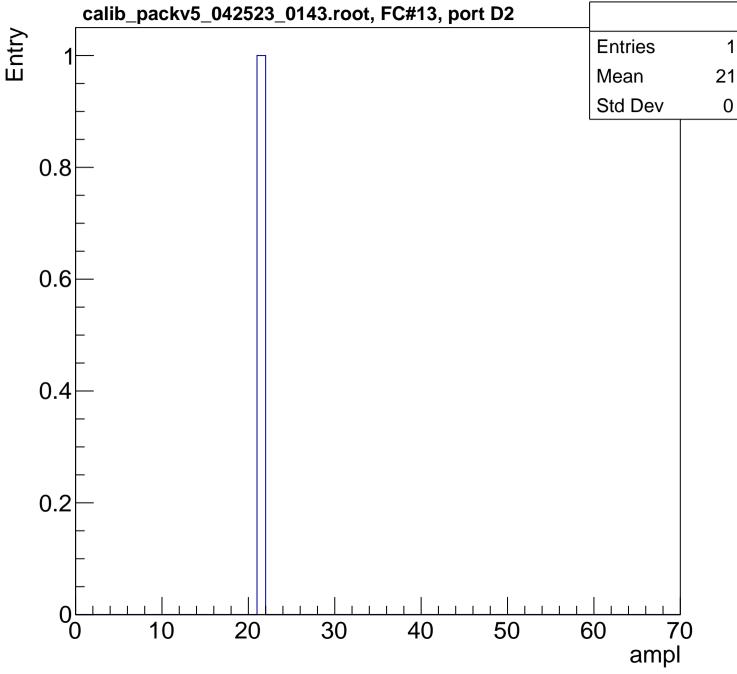


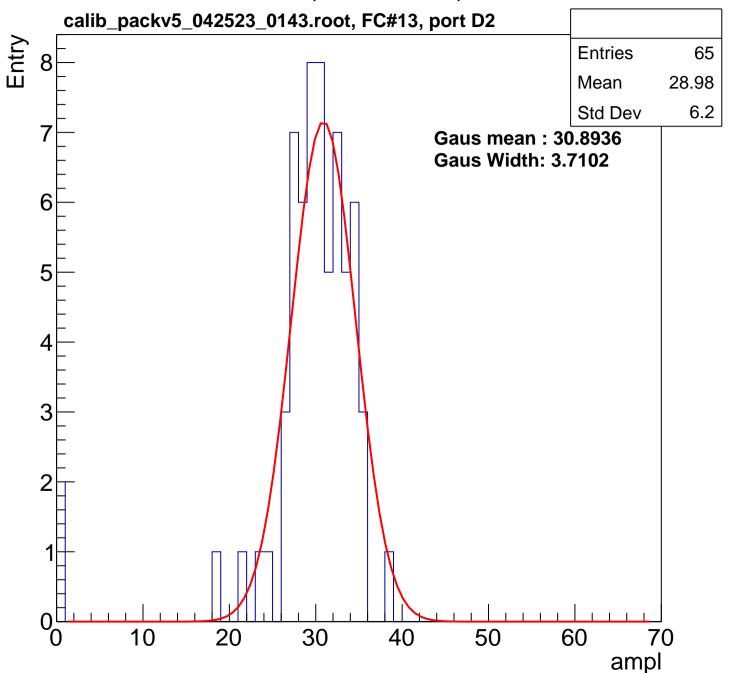


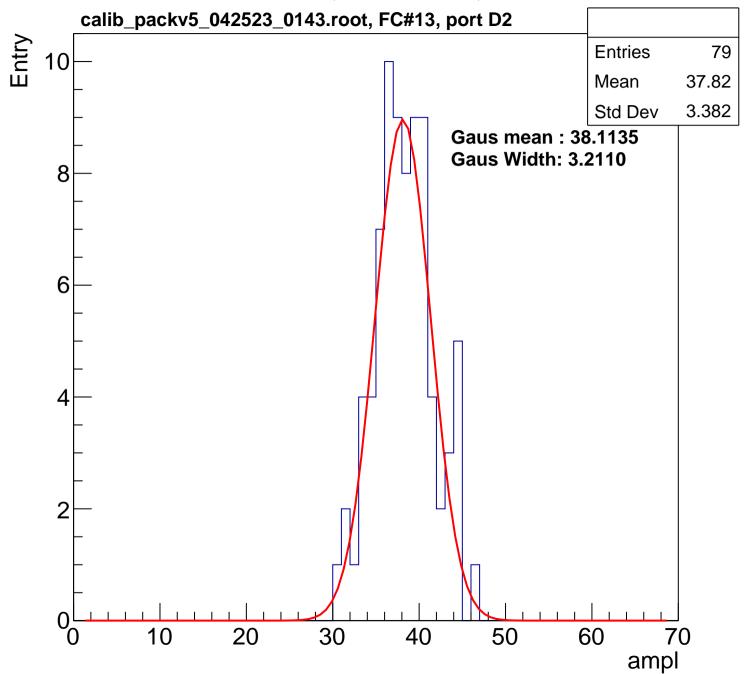


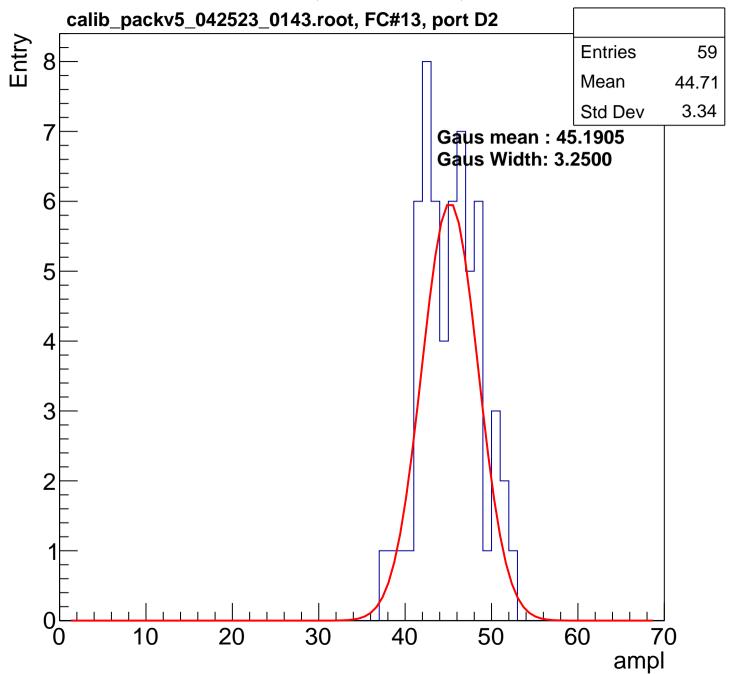


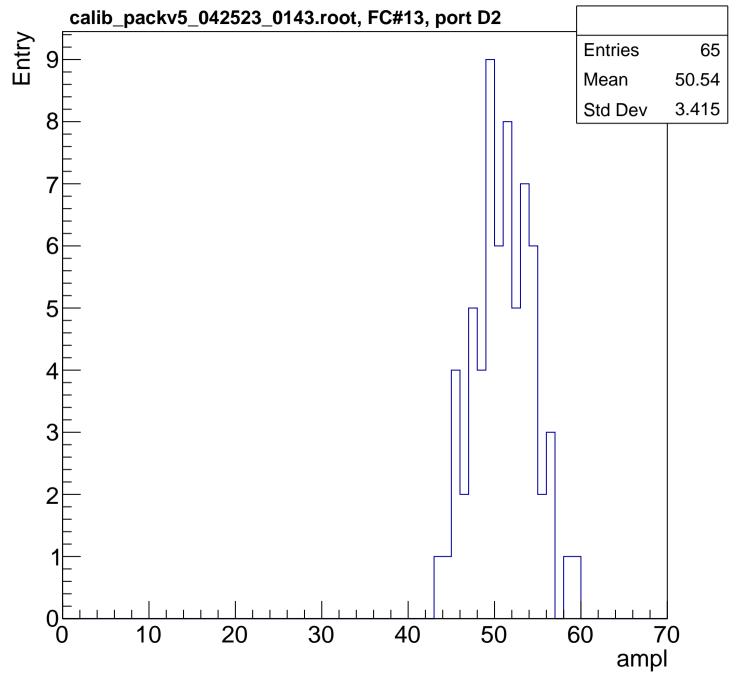
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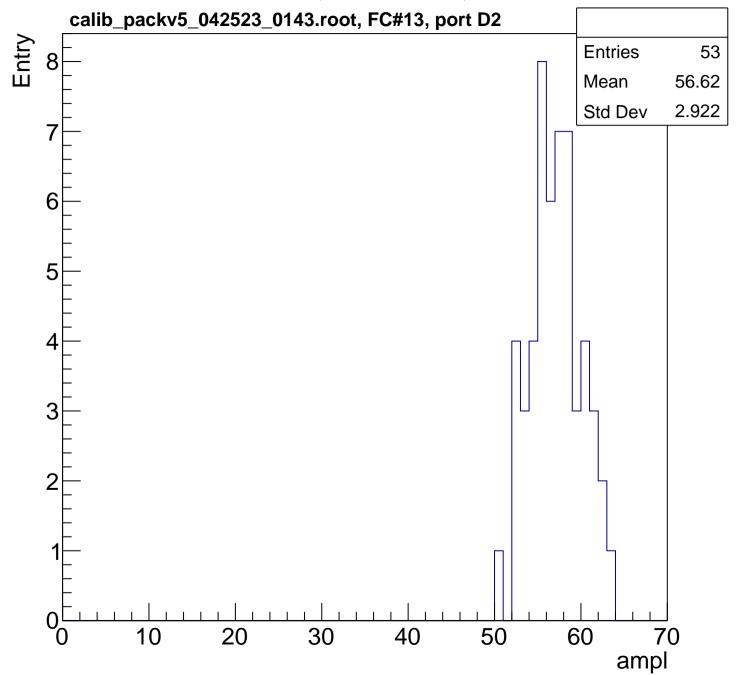


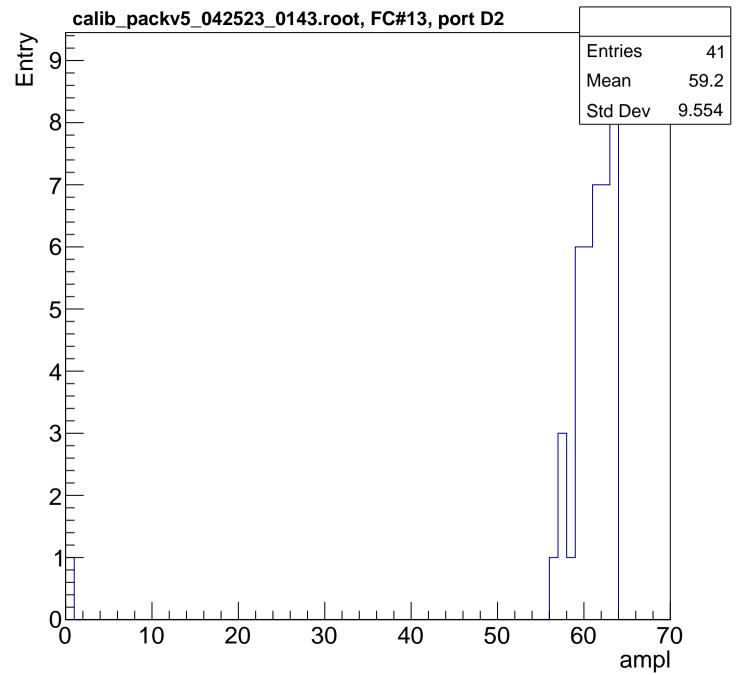


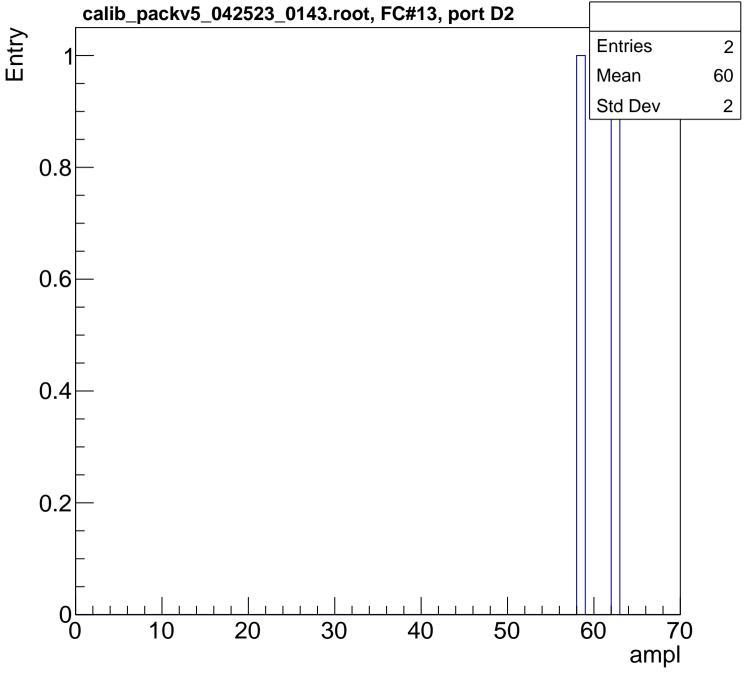




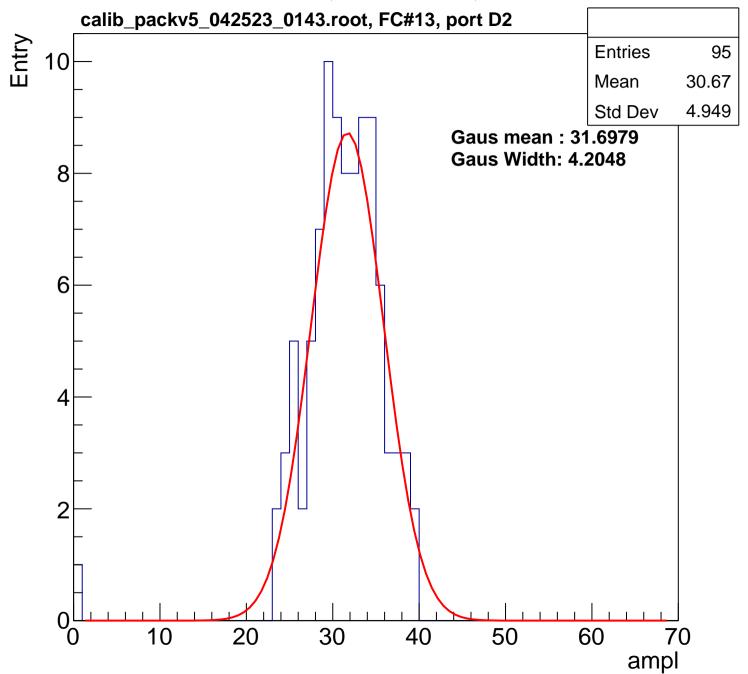


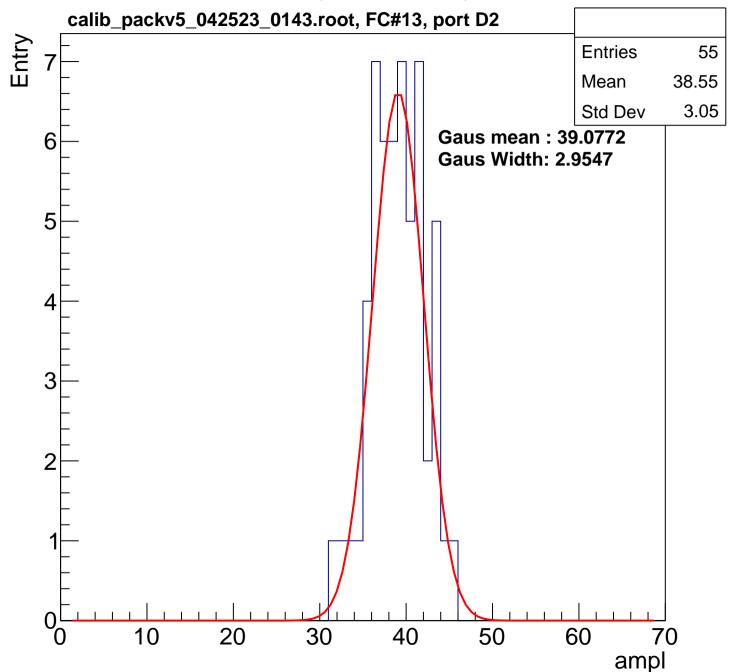


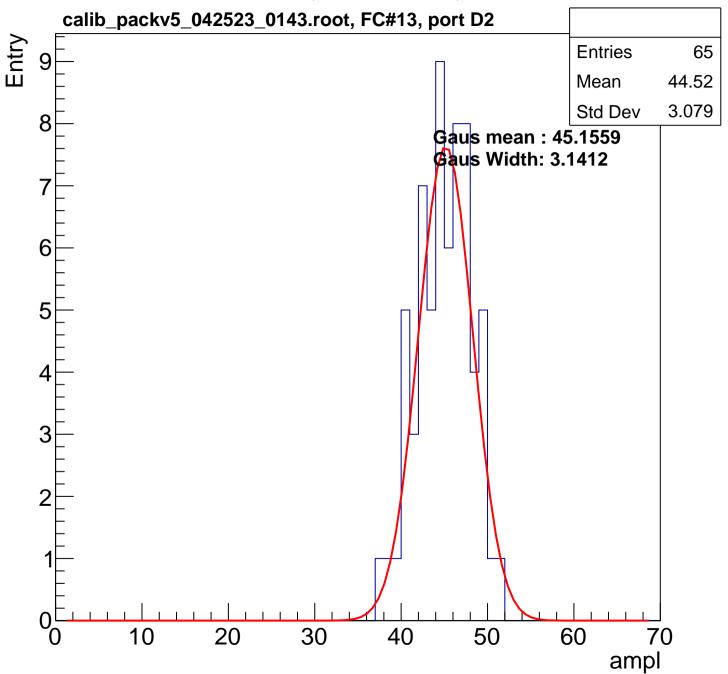


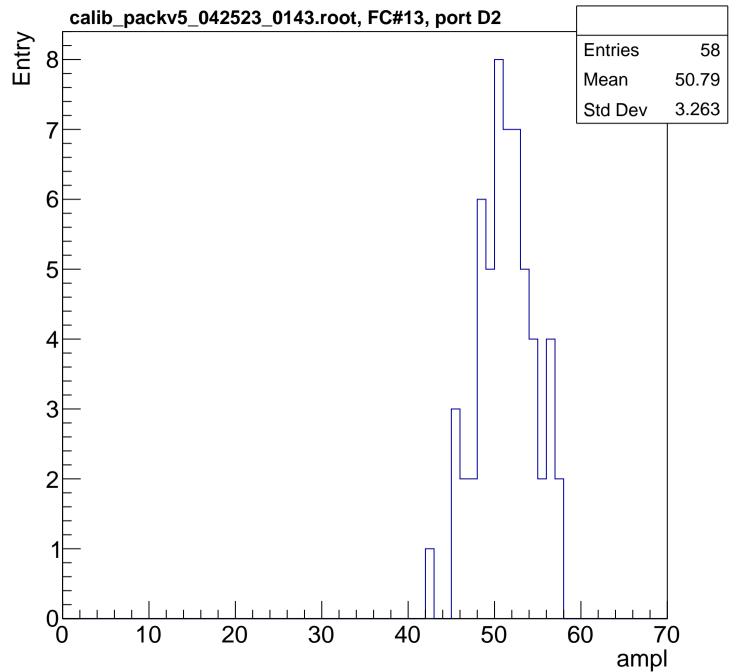


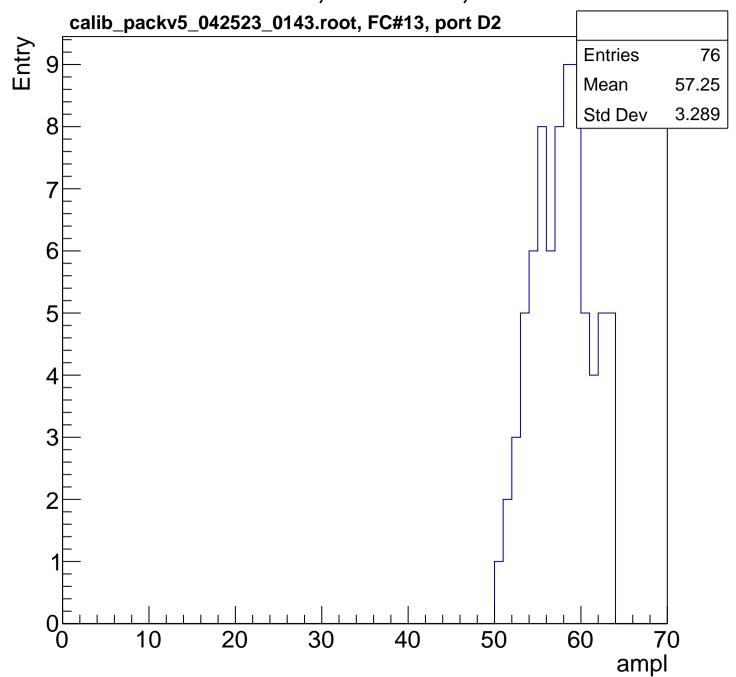
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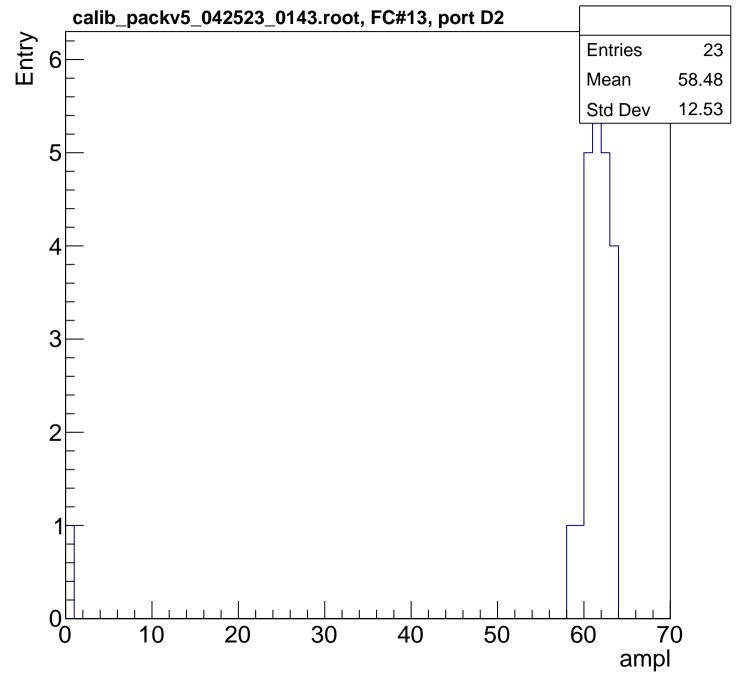


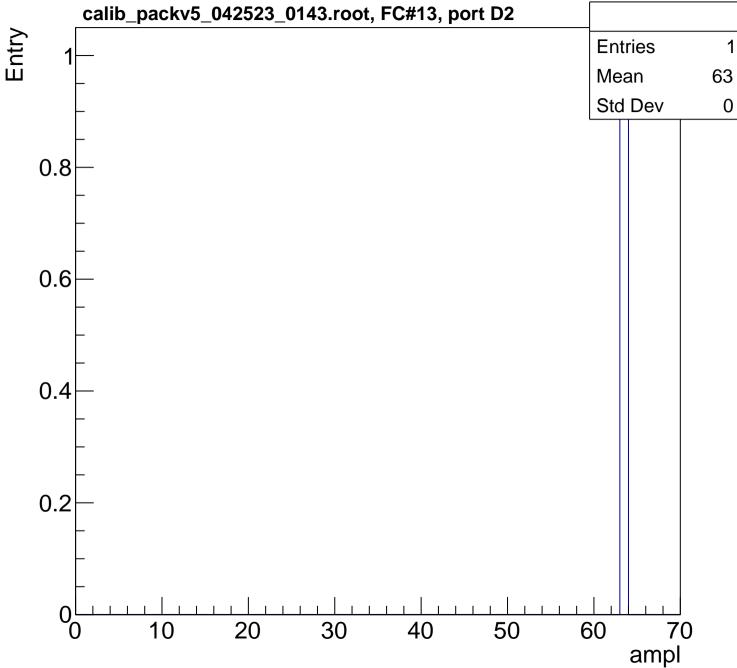




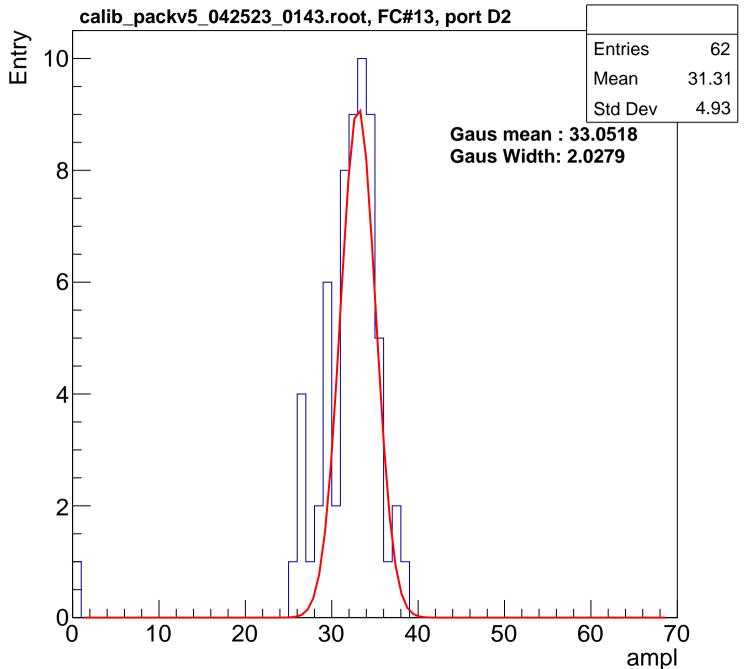


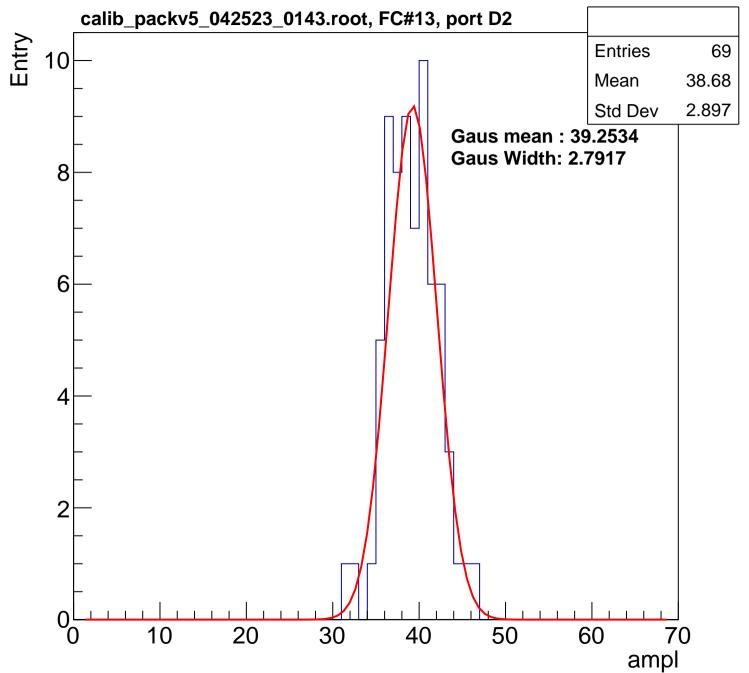


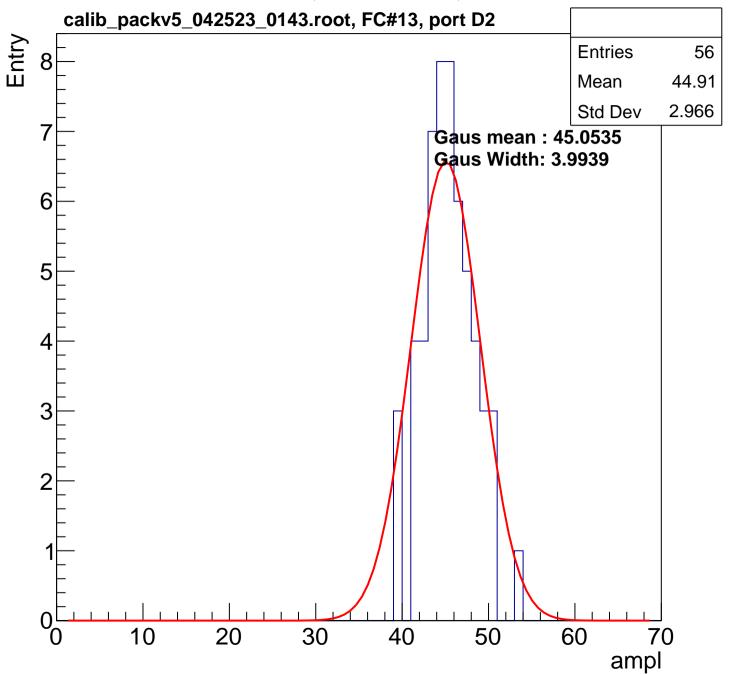


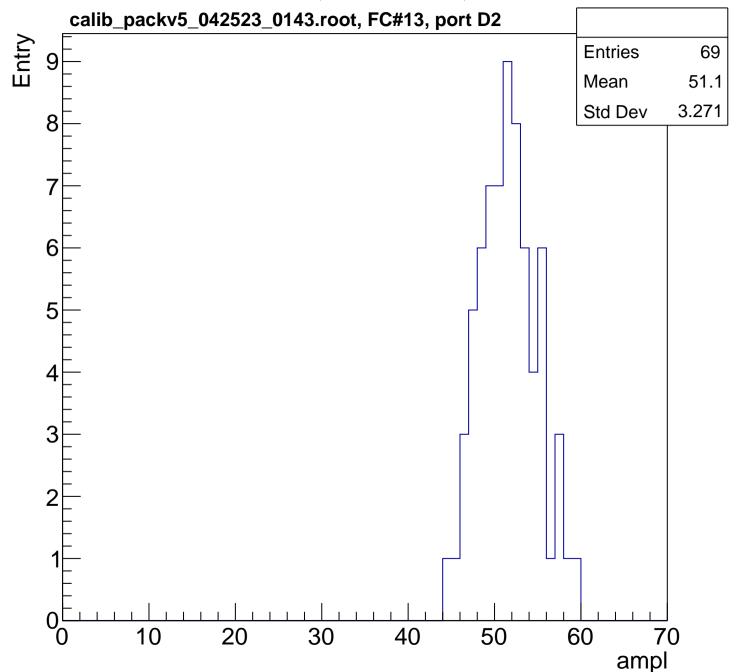


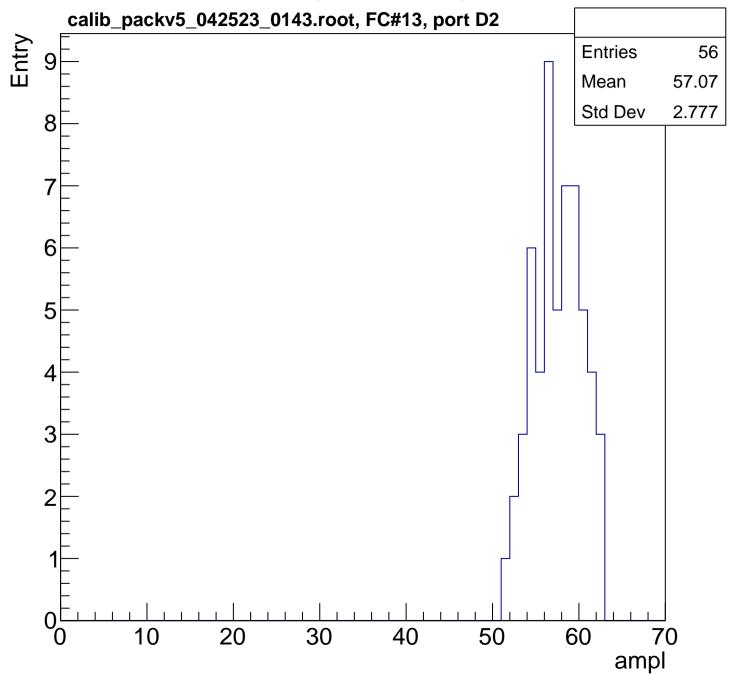
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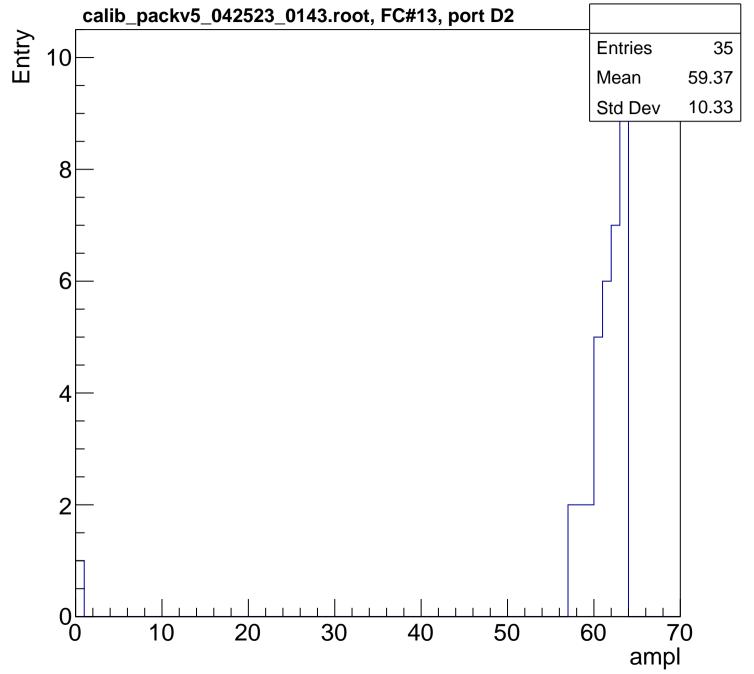


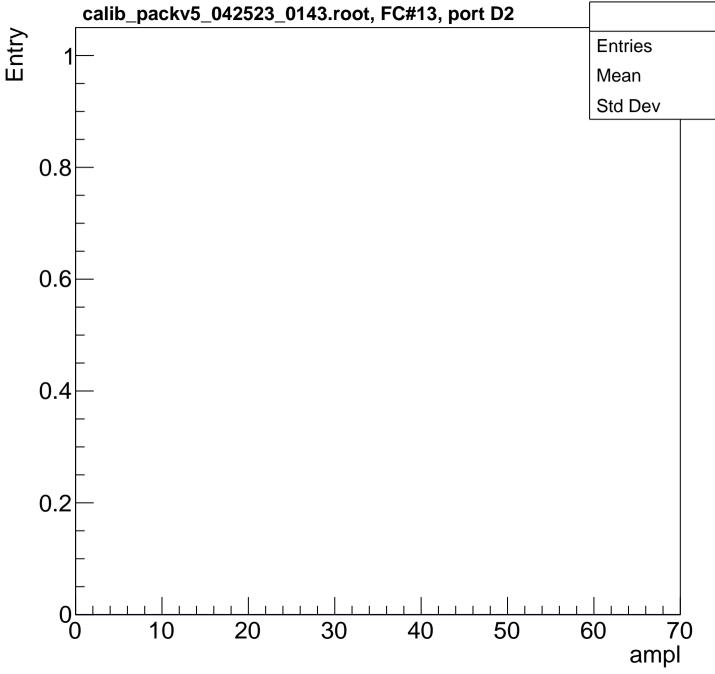


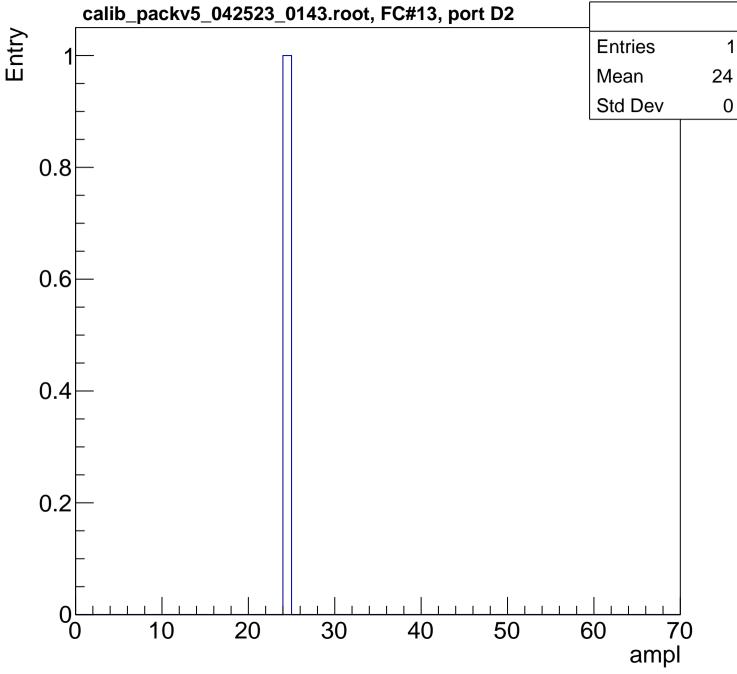


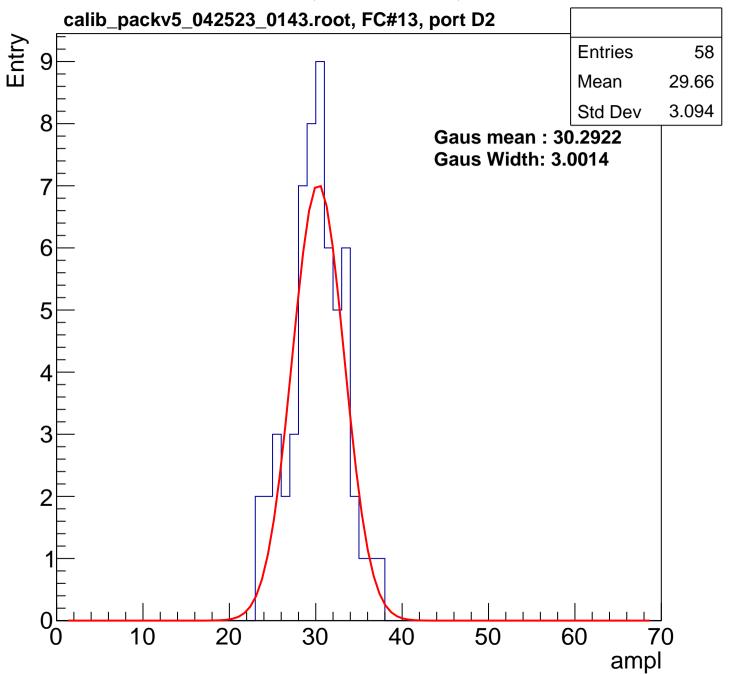


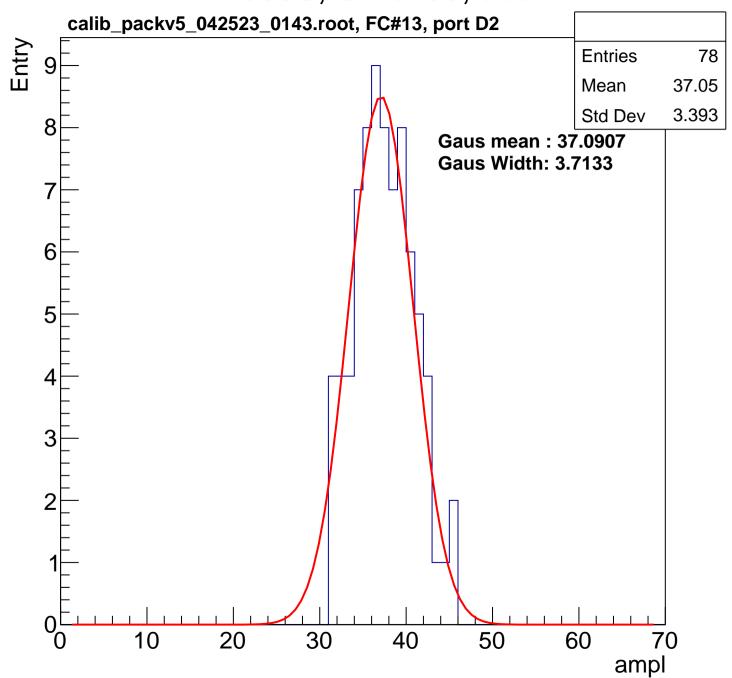


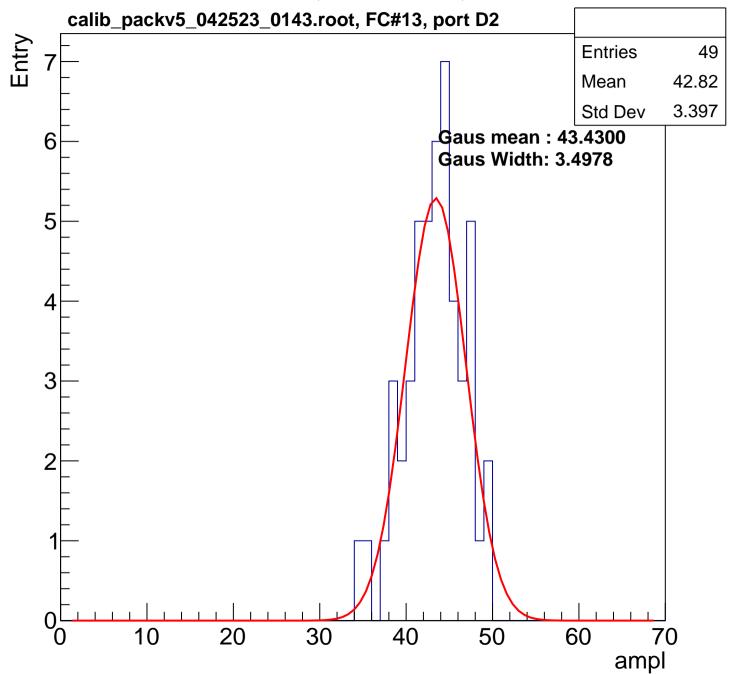


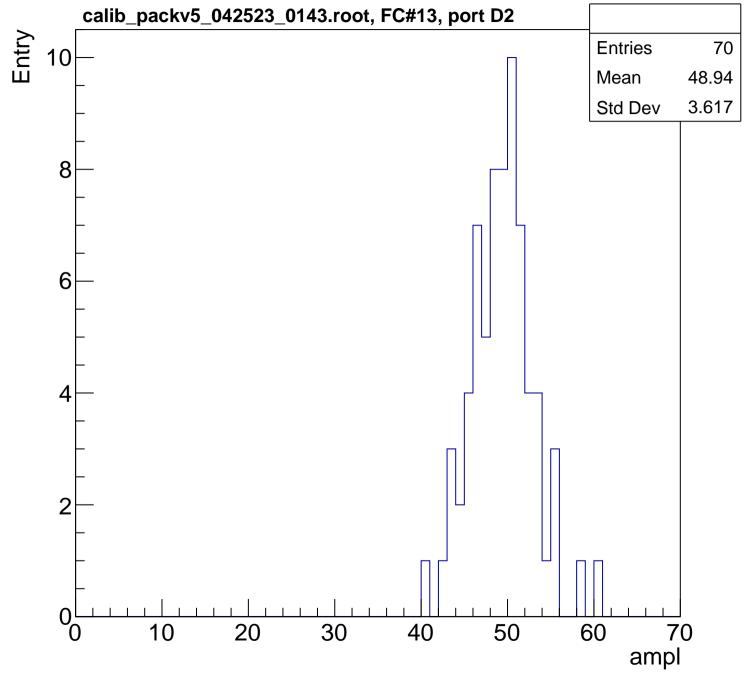


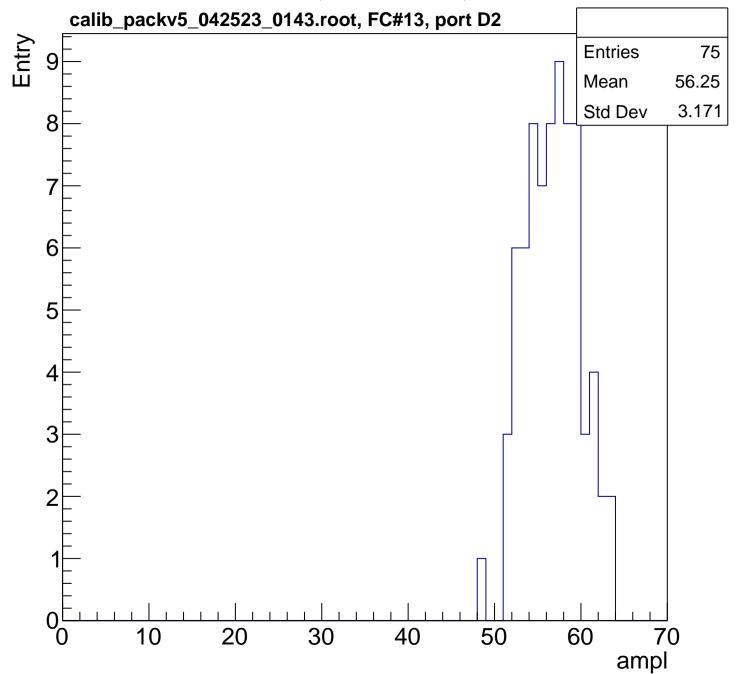


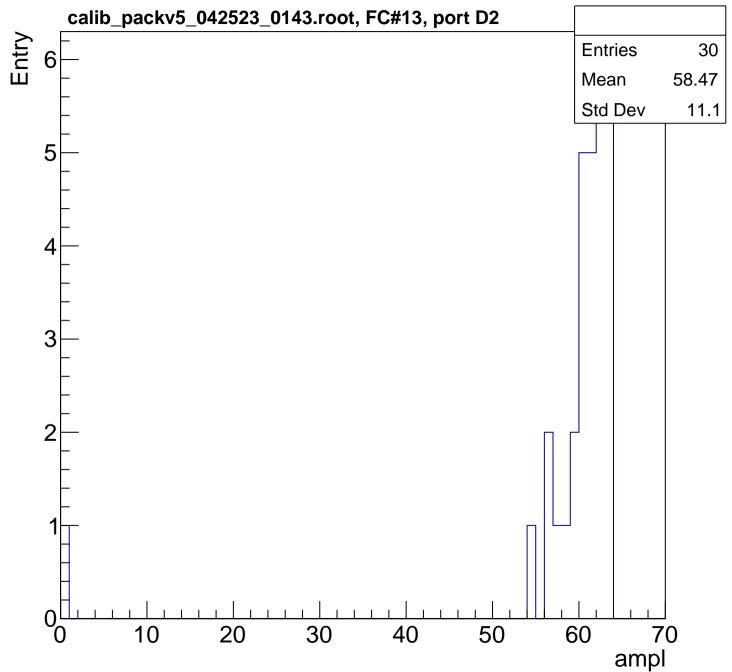


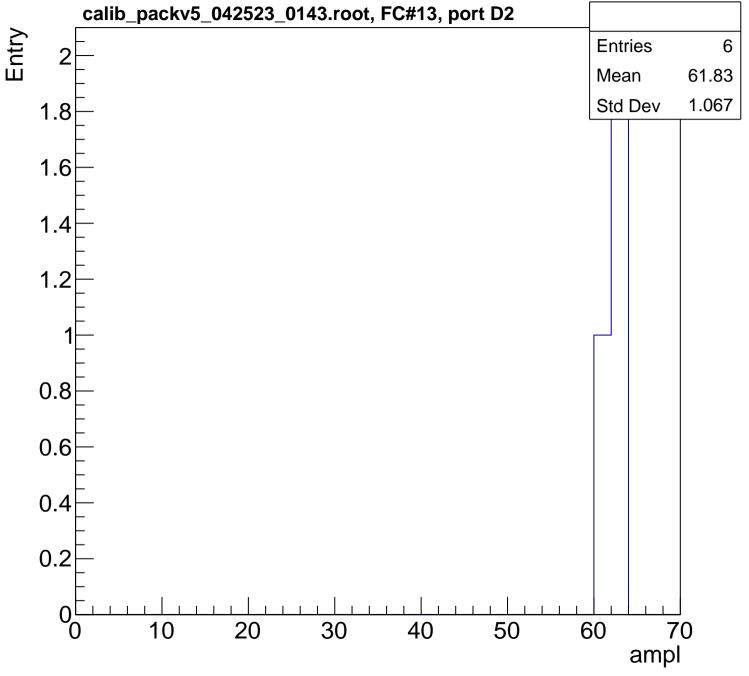




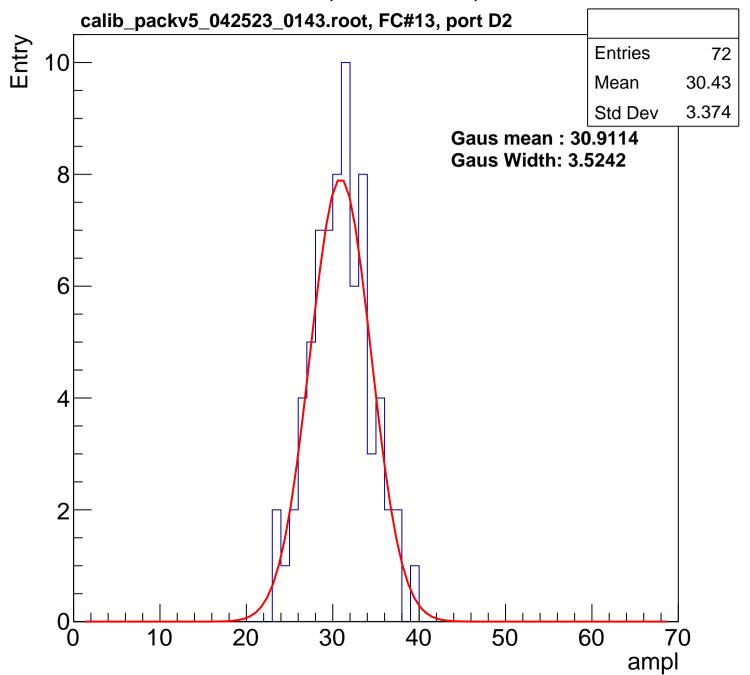


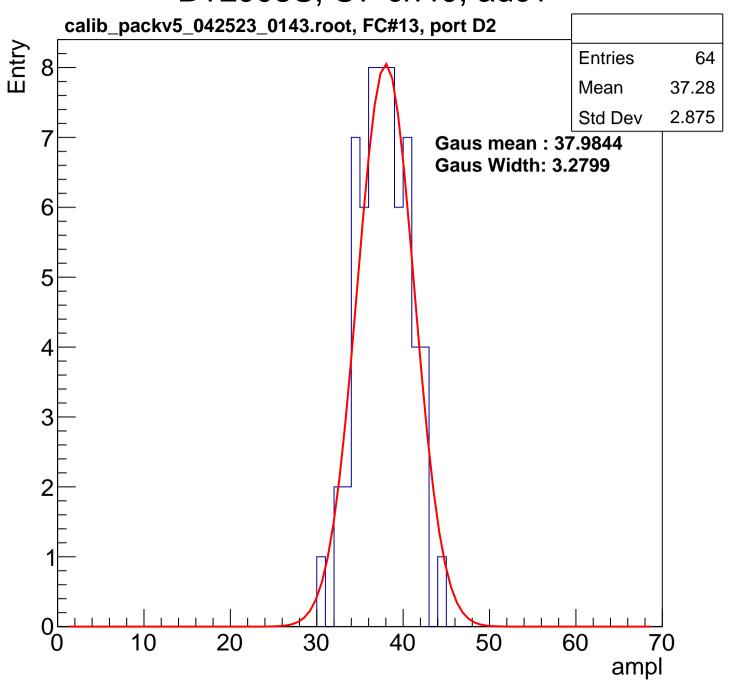


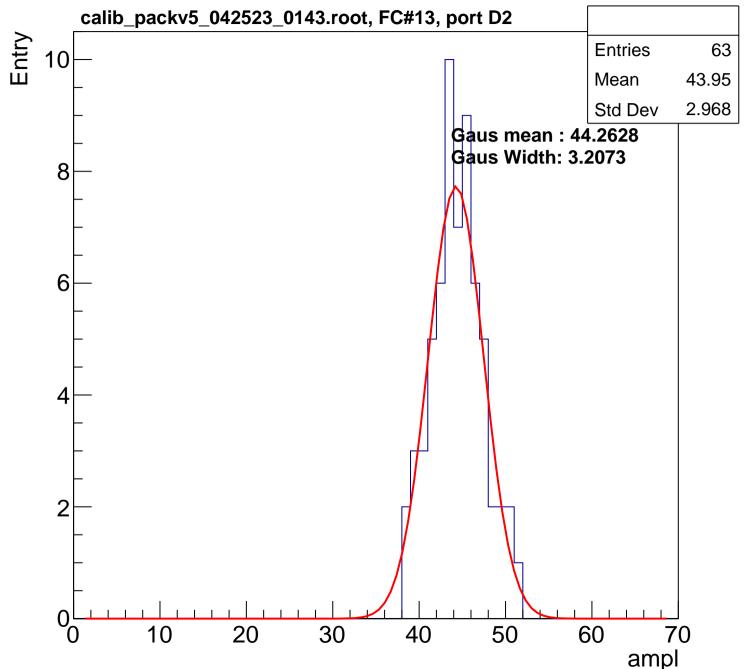


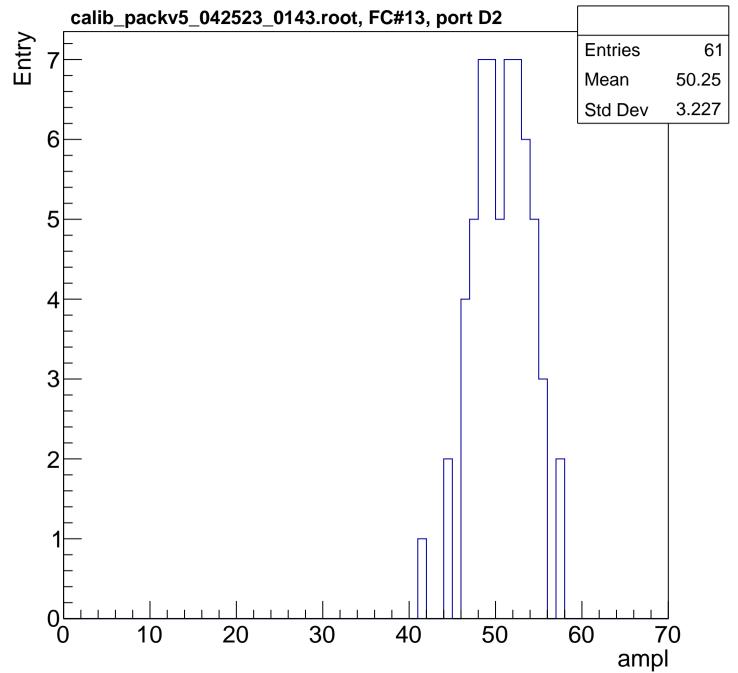


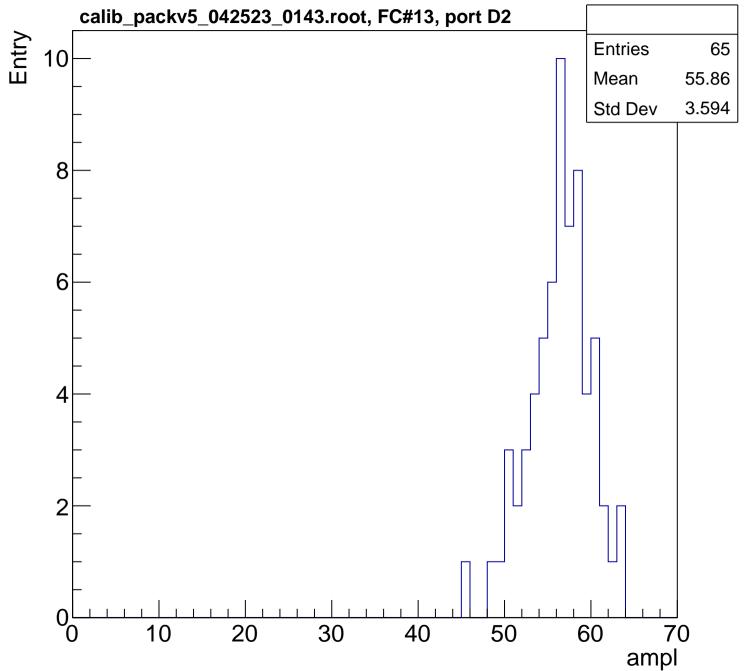
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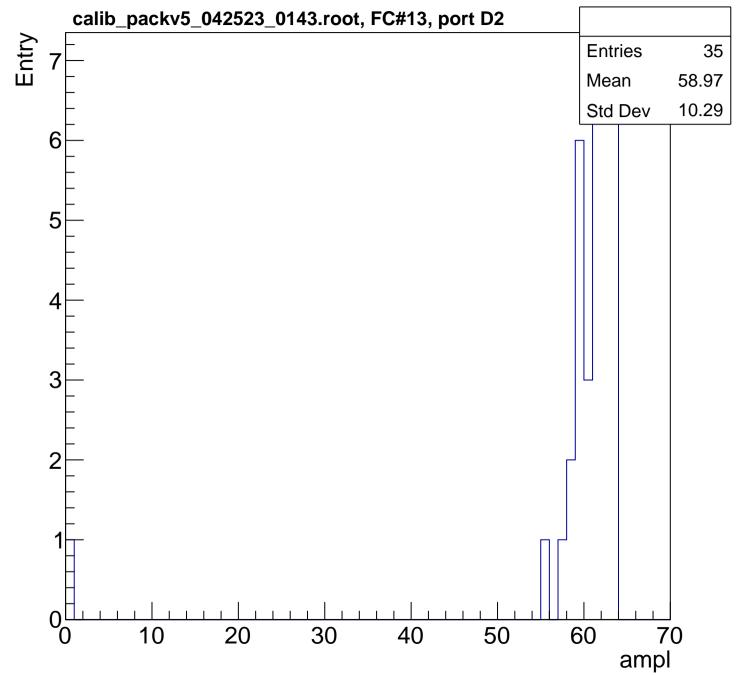


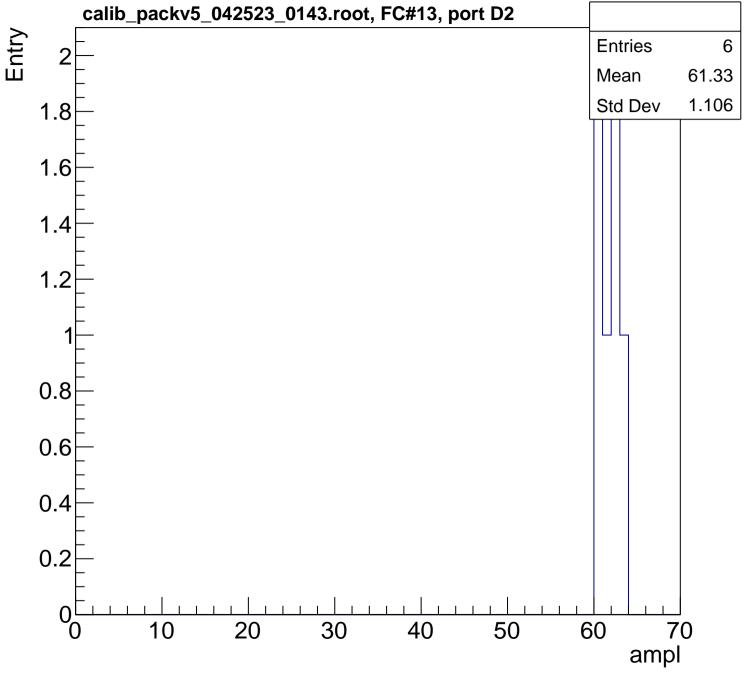


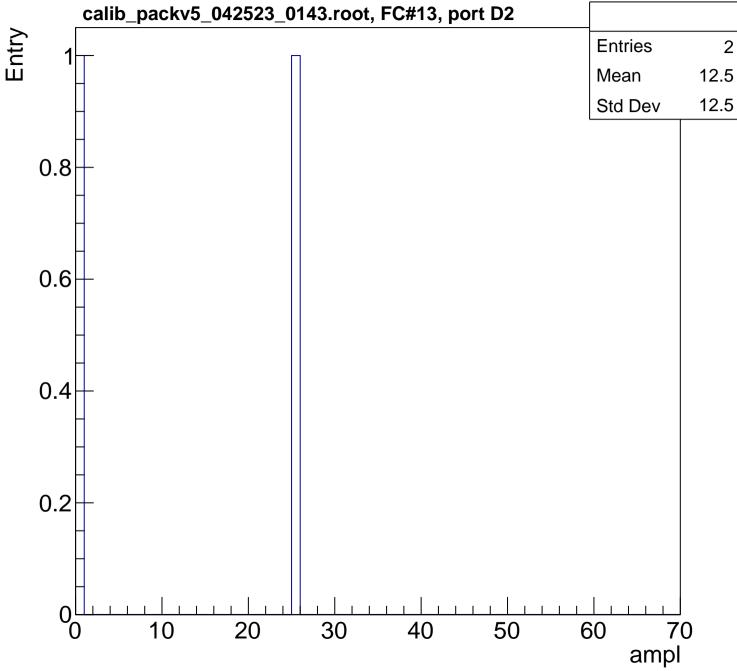


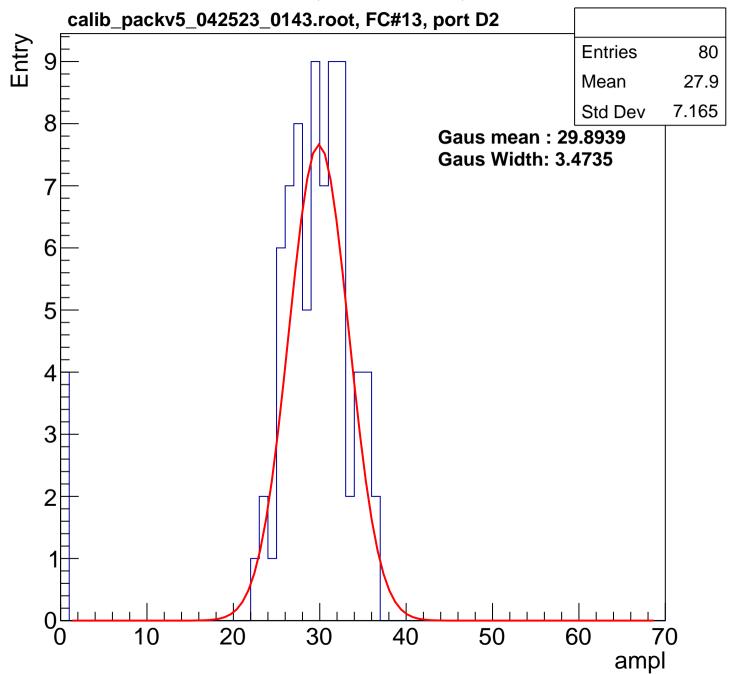


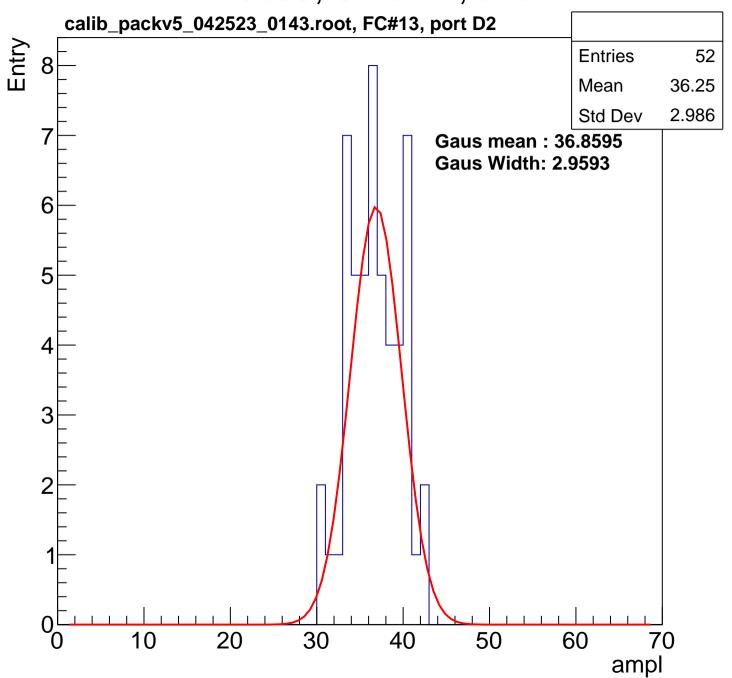


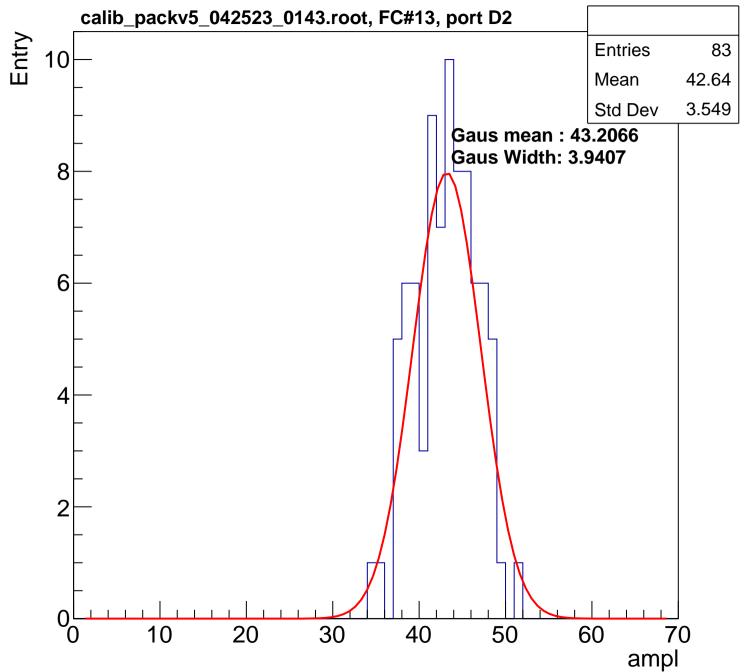


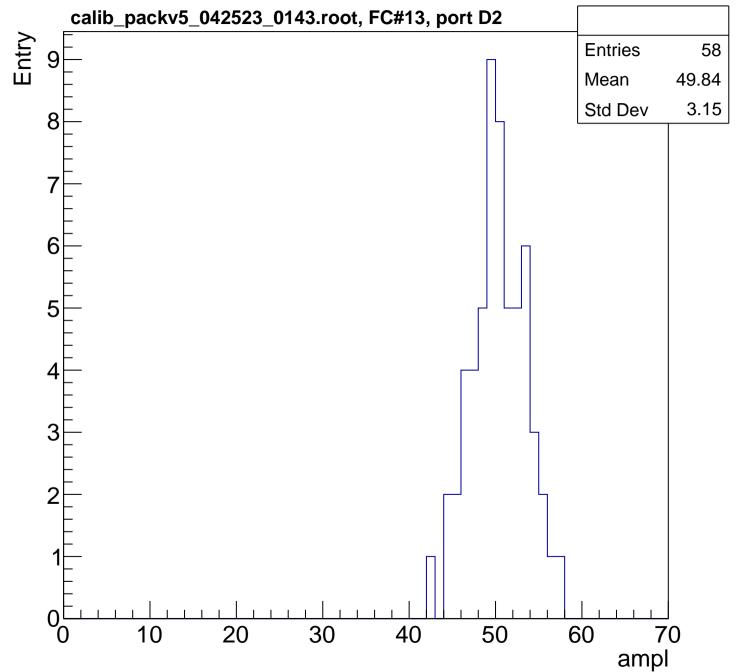


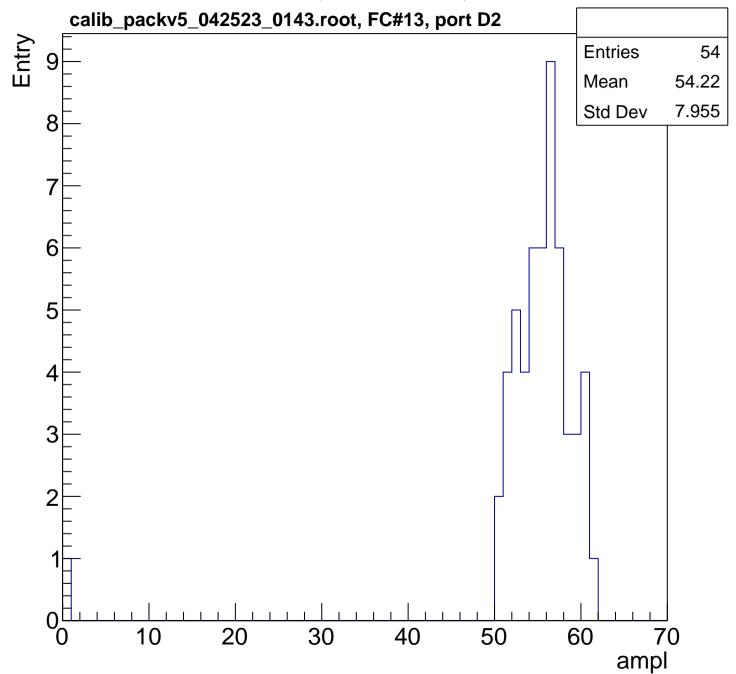


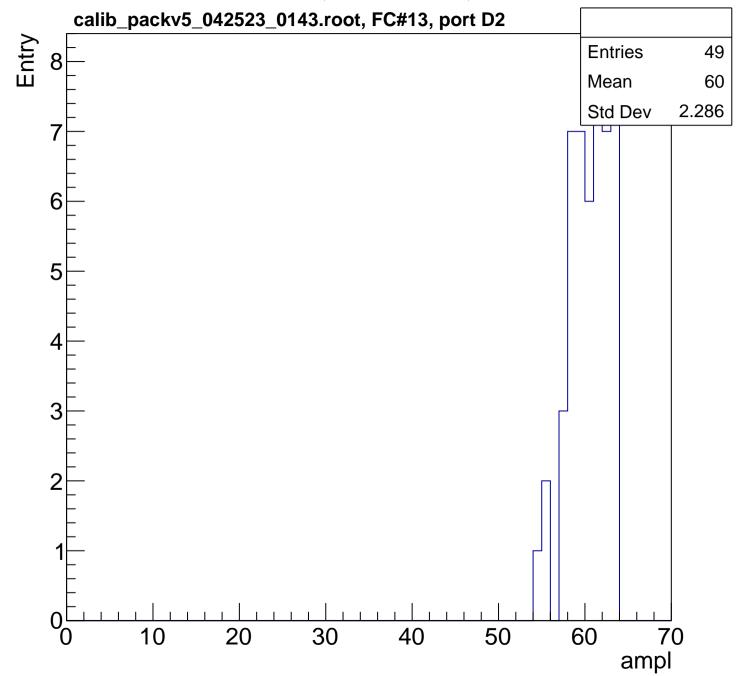


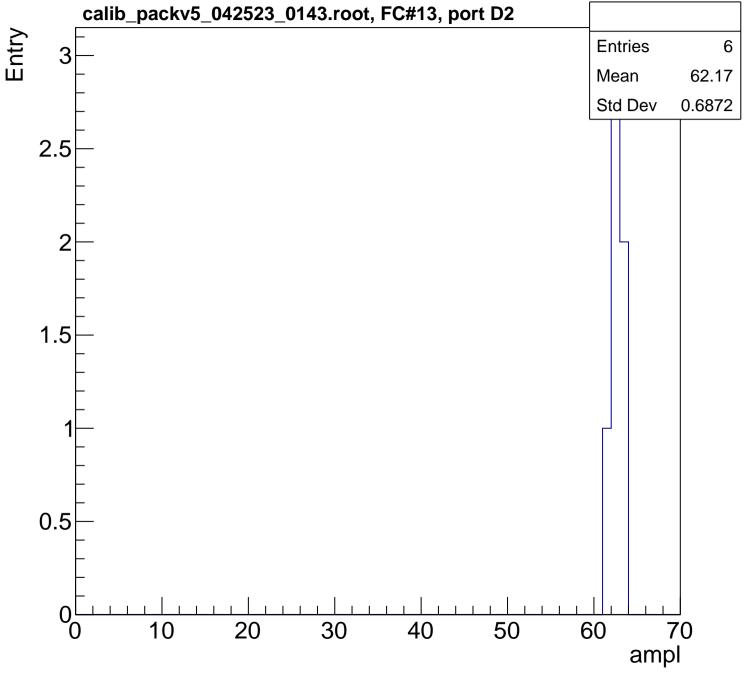




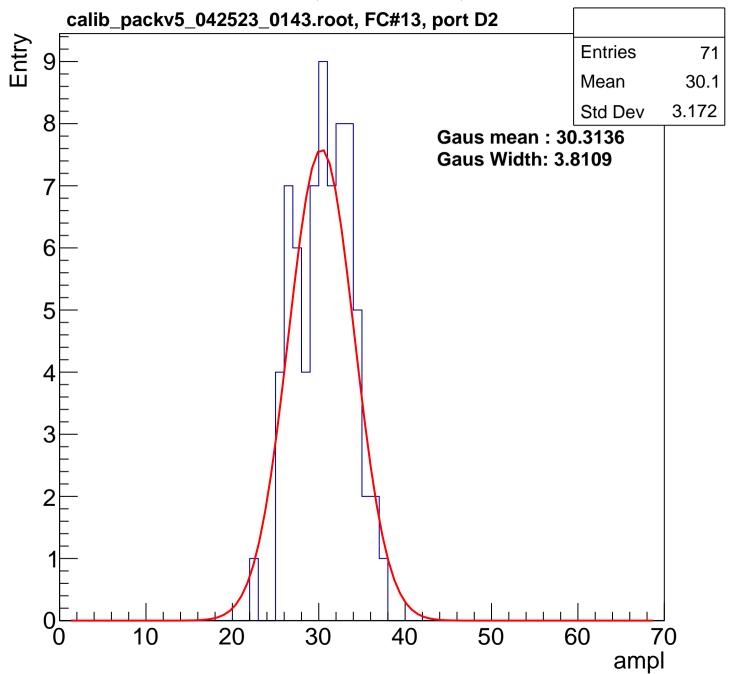


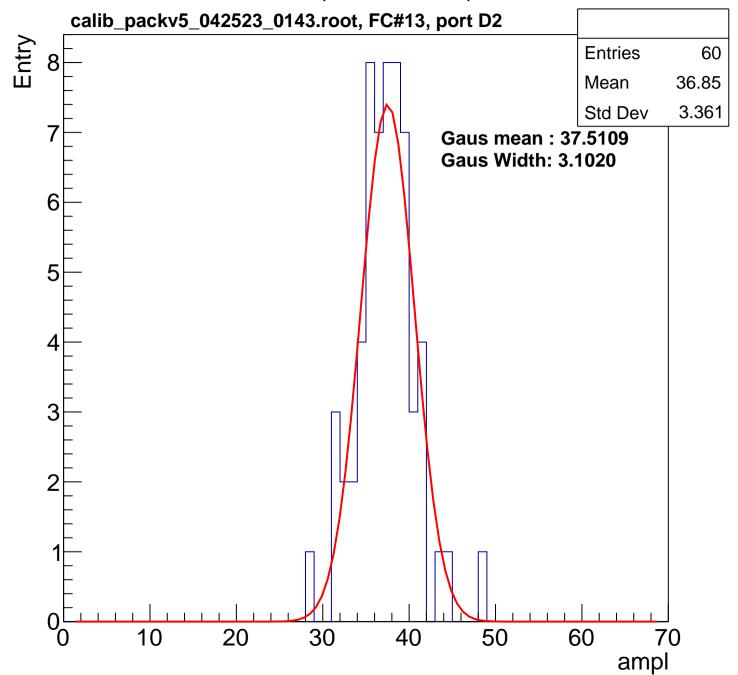


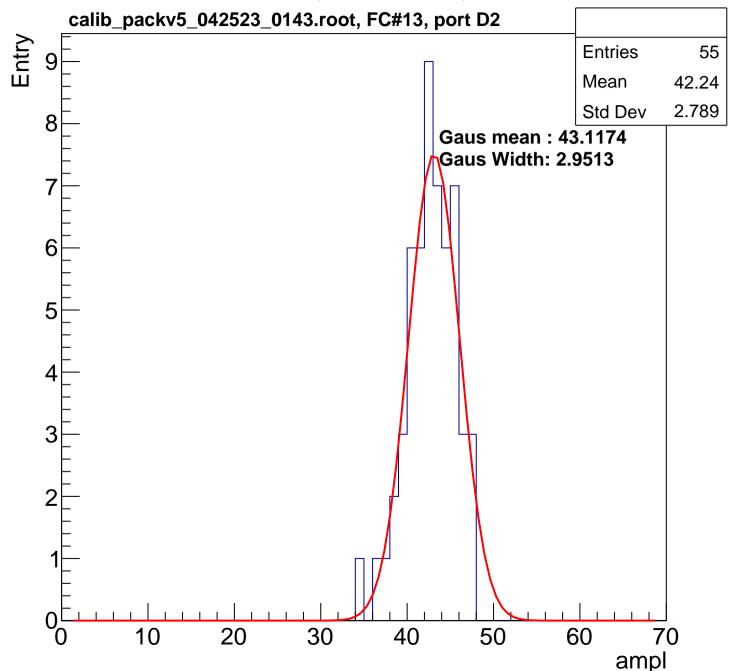


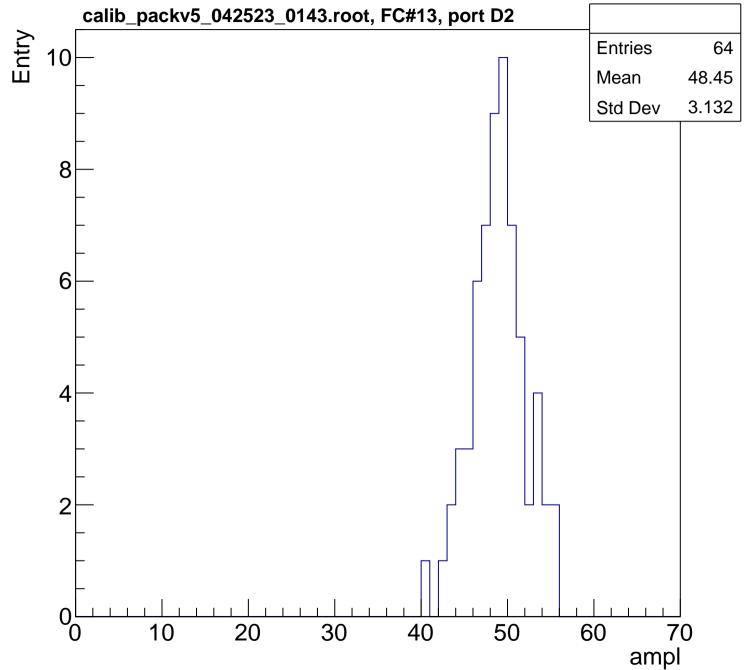


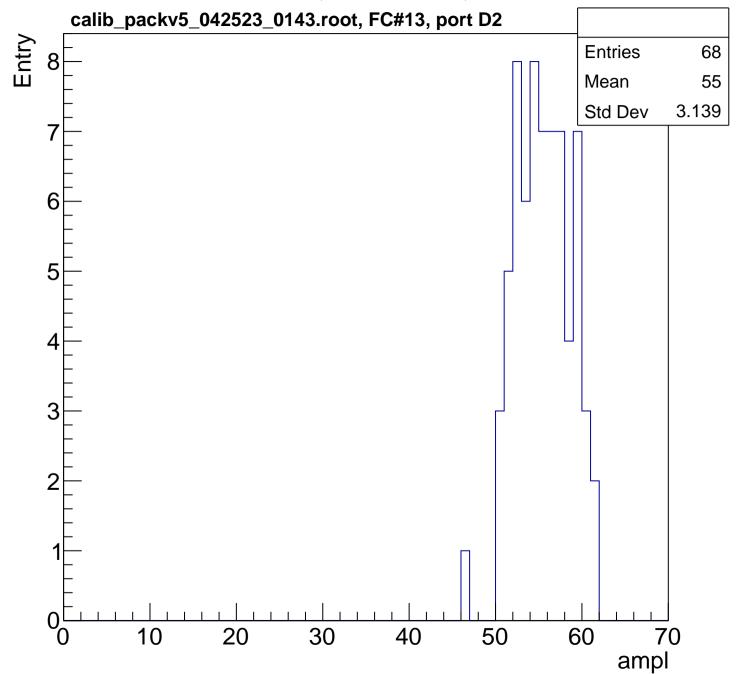
B1L003S, U7-ch41, adc7 calib_packv5_042523_0143.root, FC#13, port D2 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

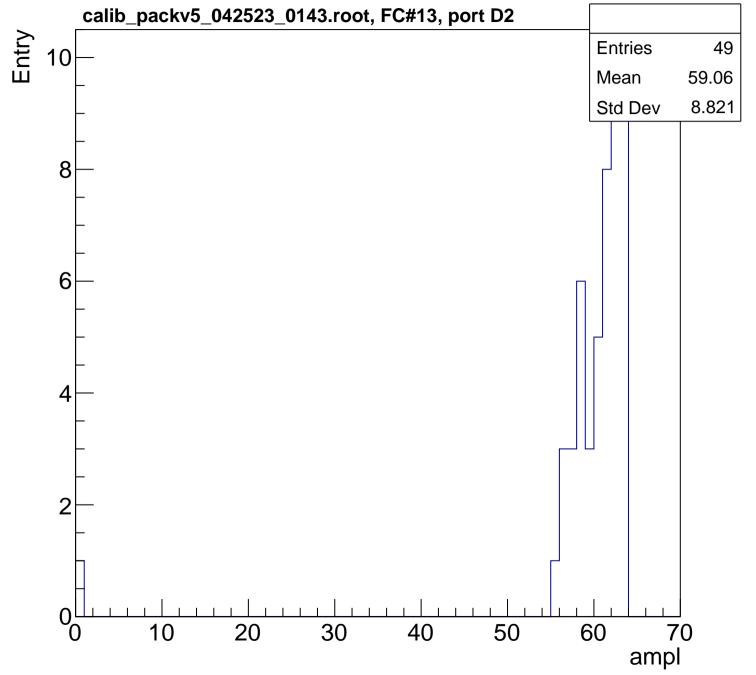


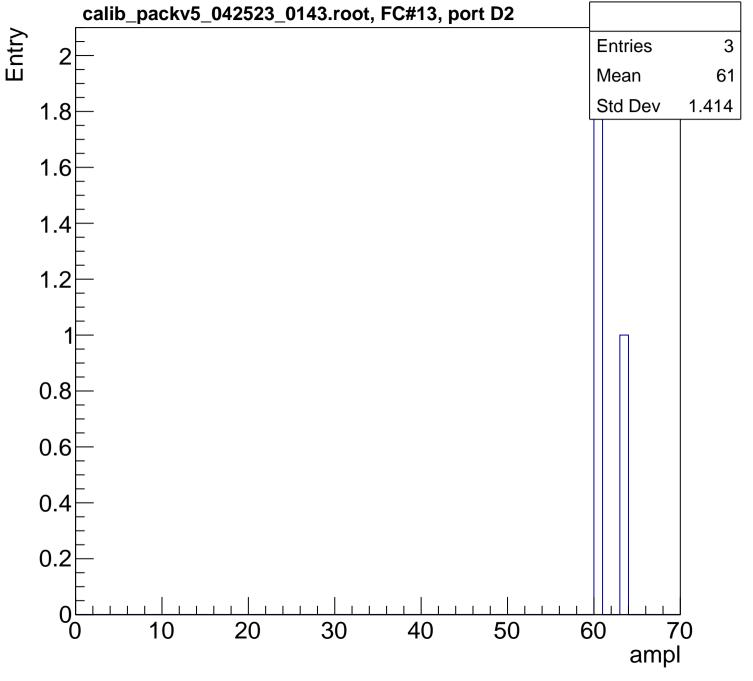




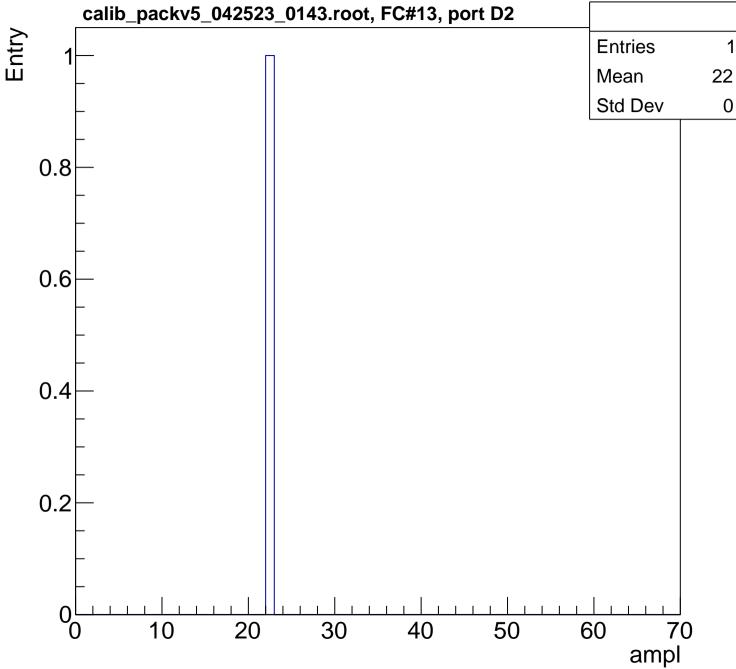


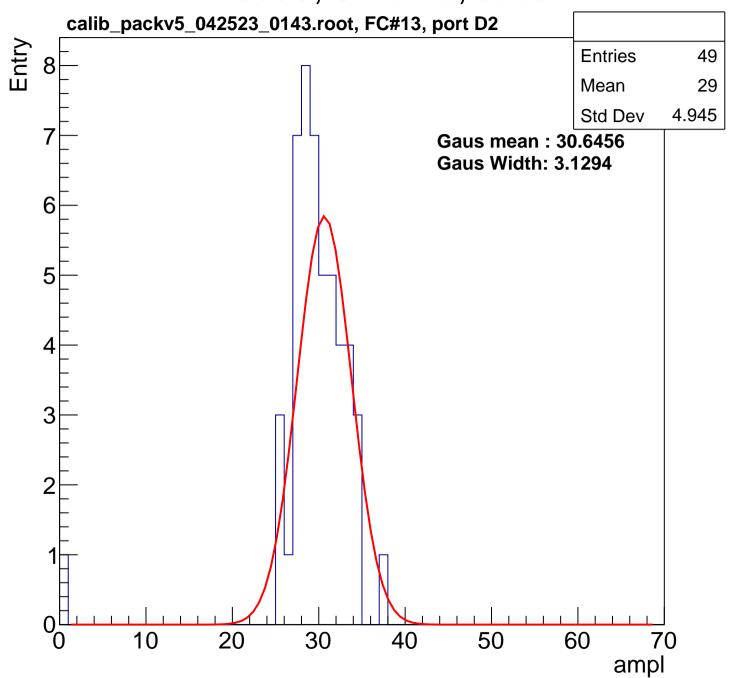


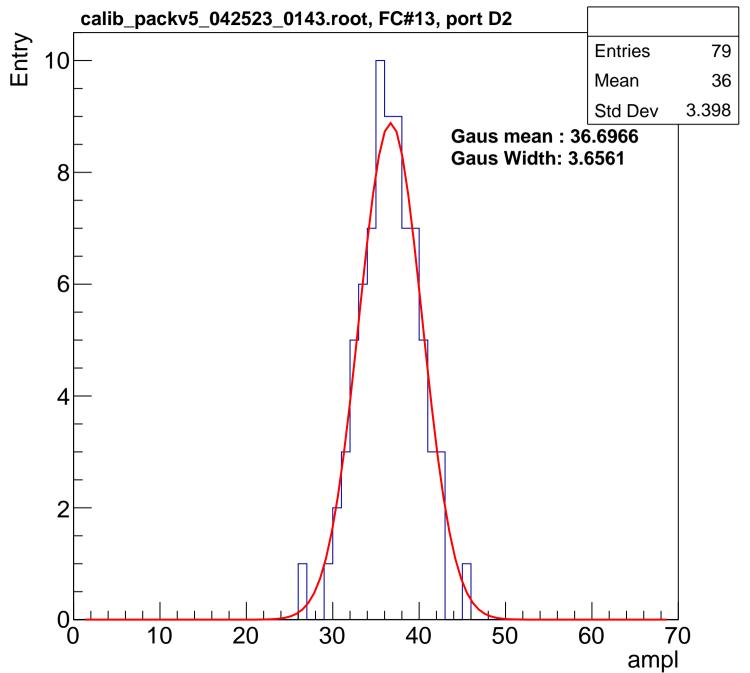


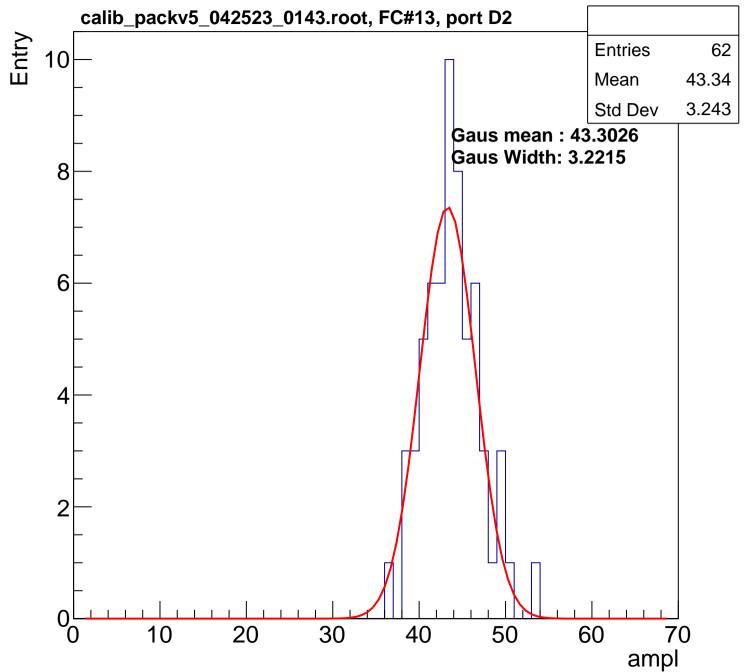


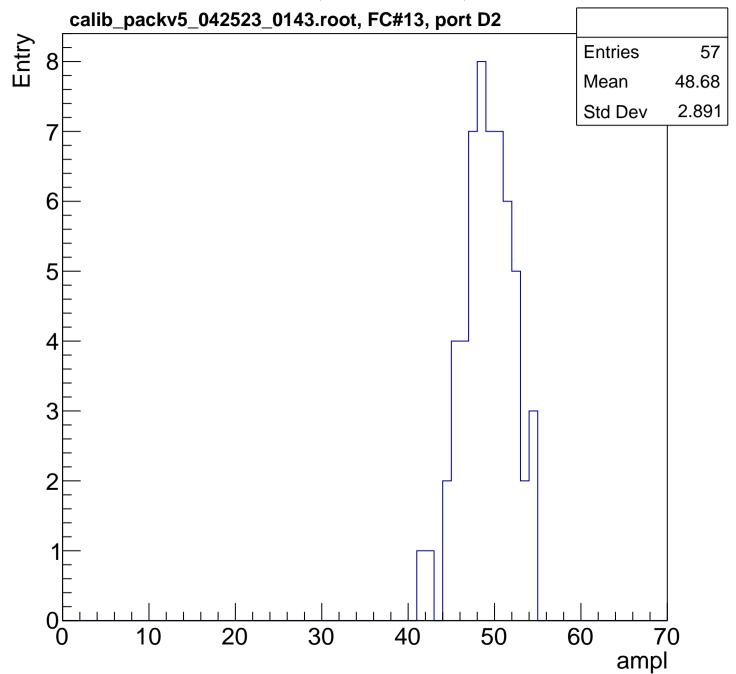
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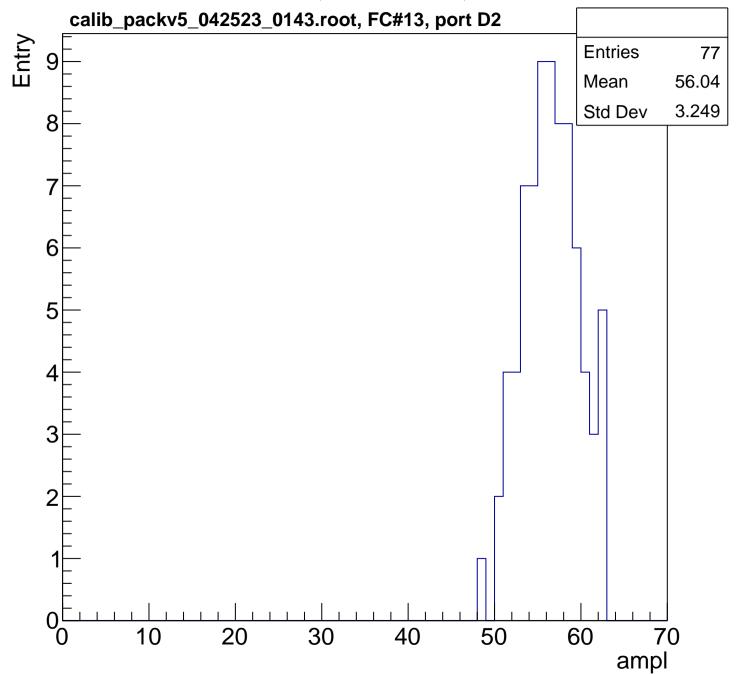


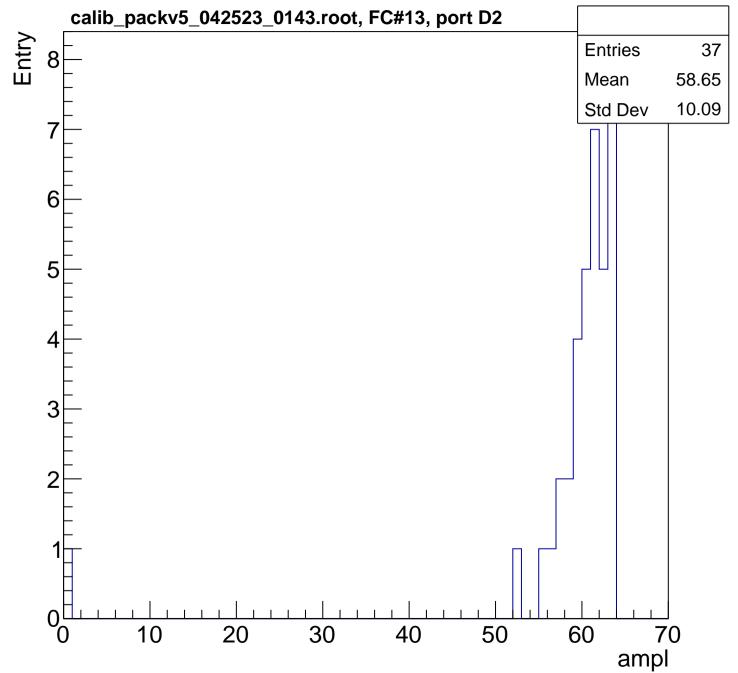


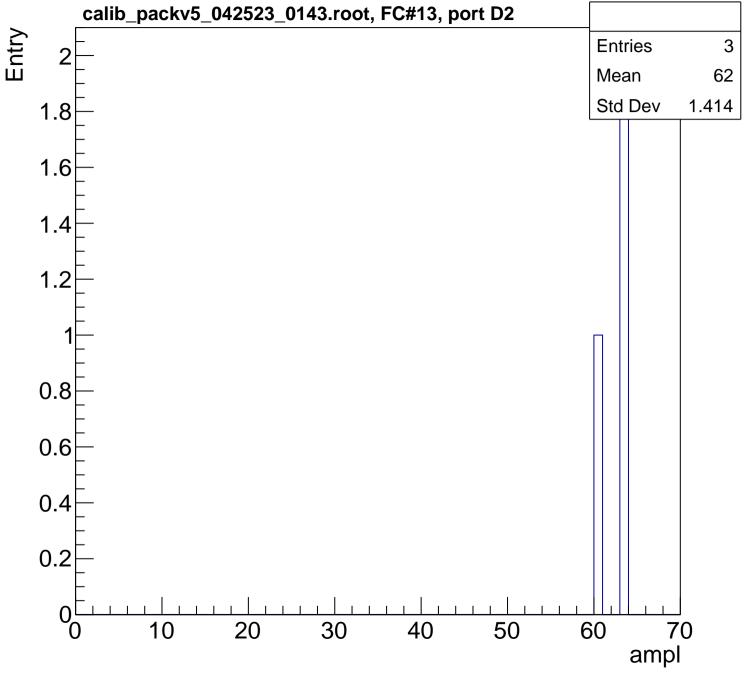




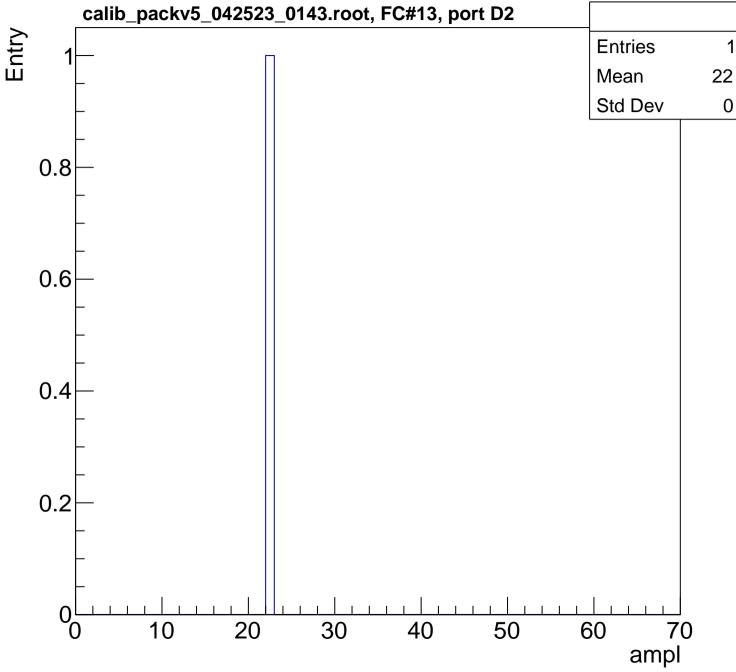


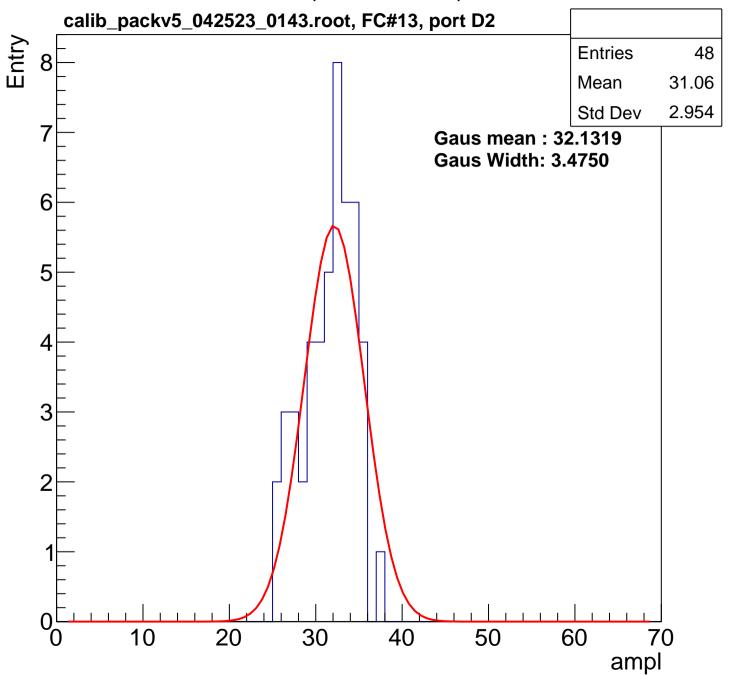


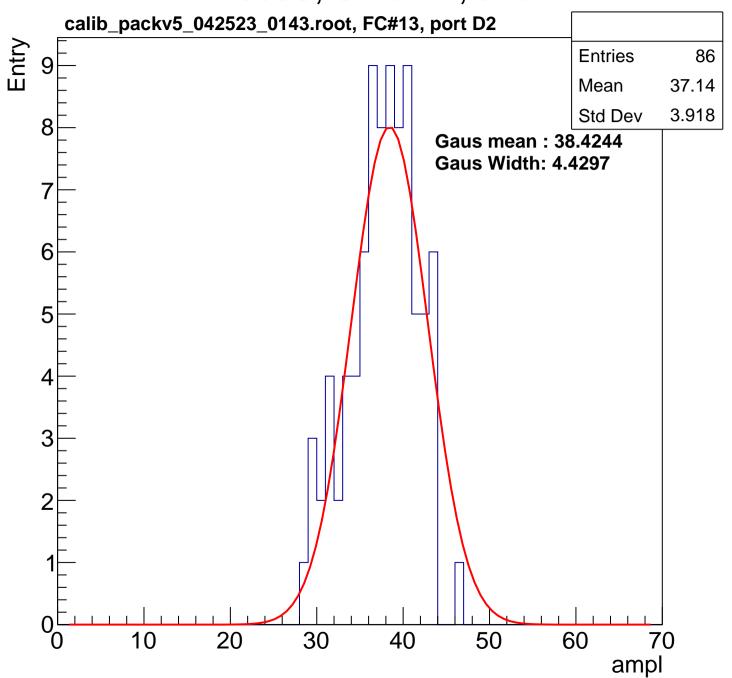


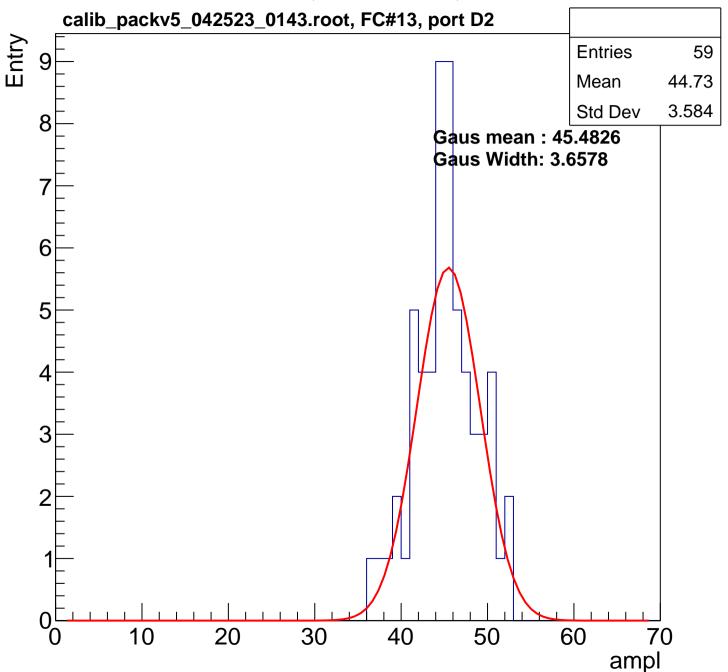


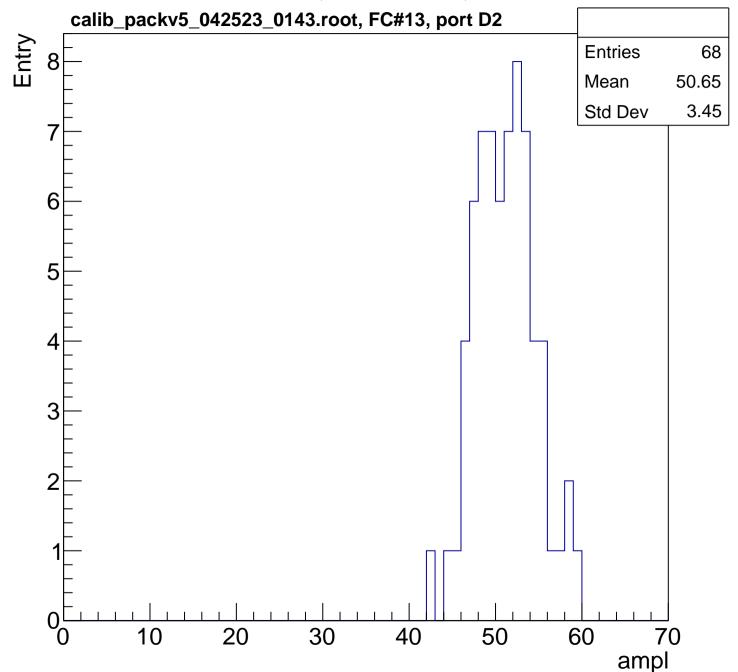
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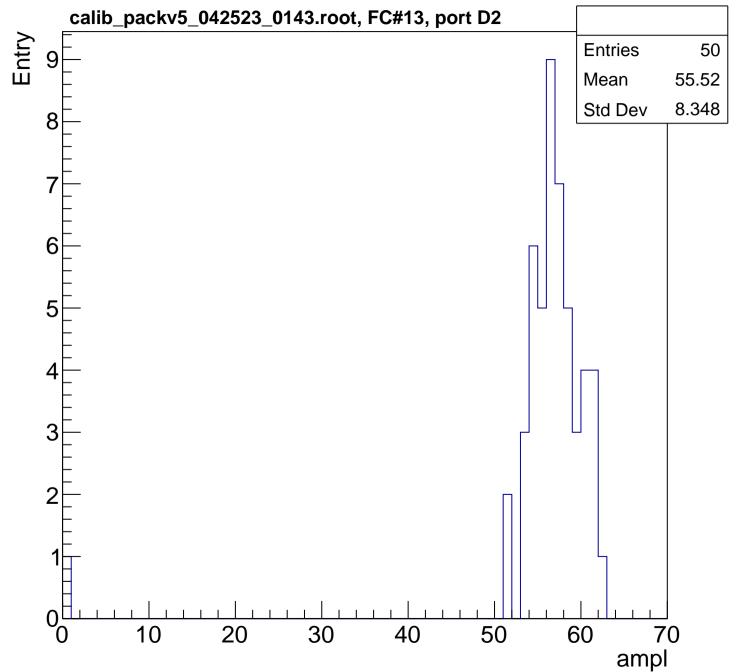


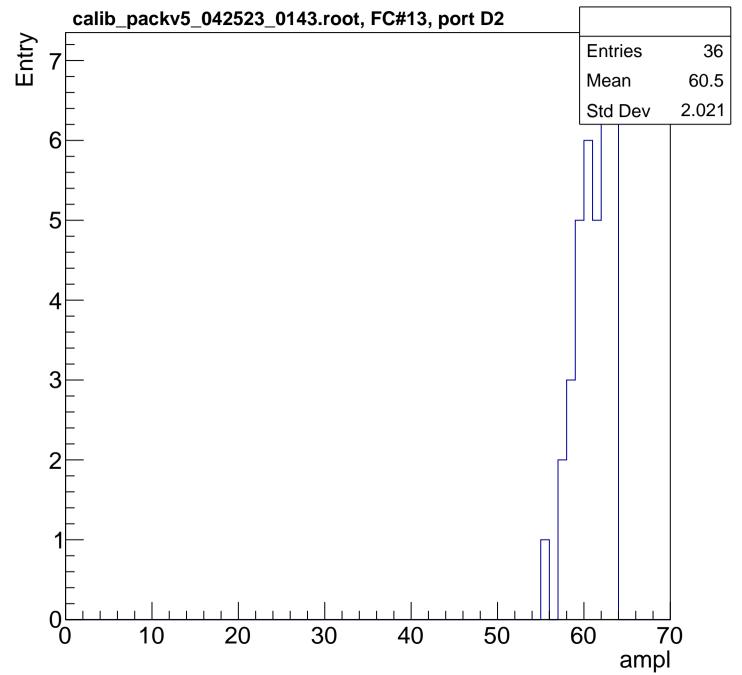


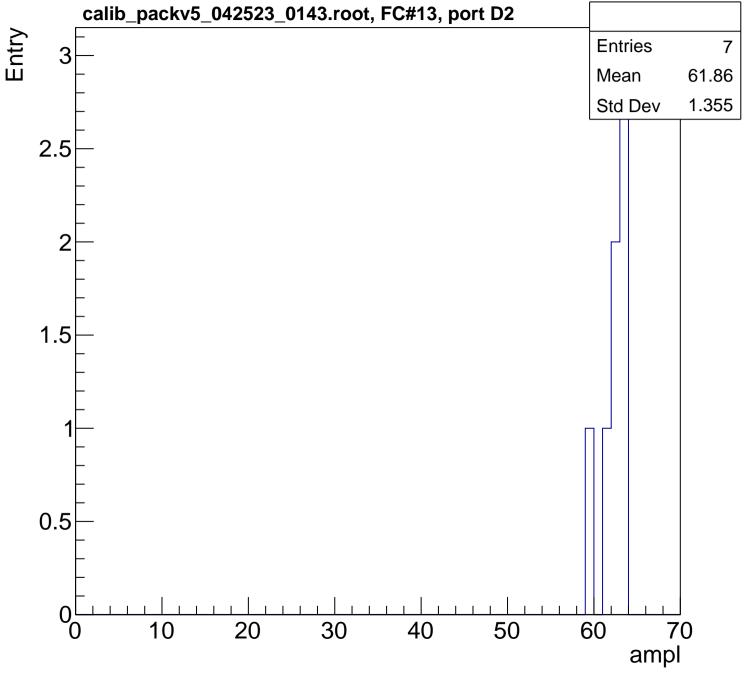


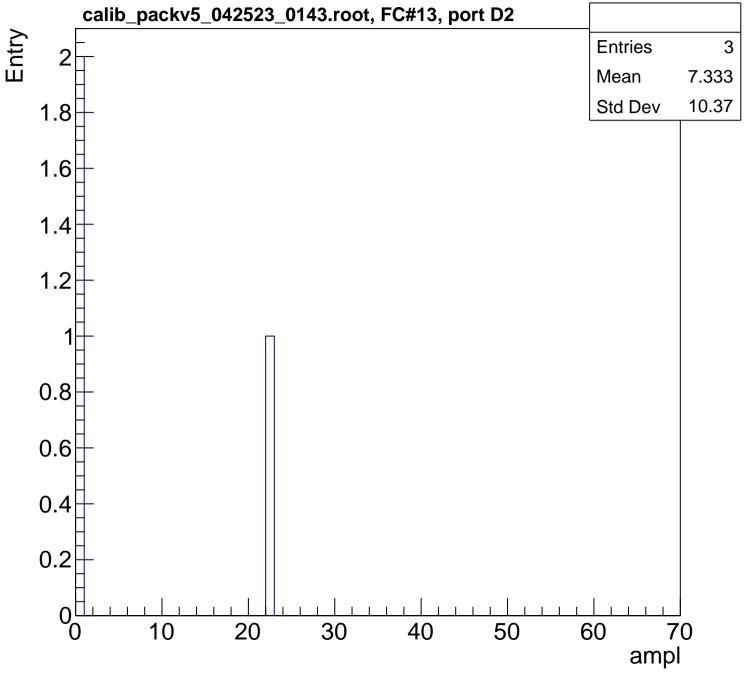


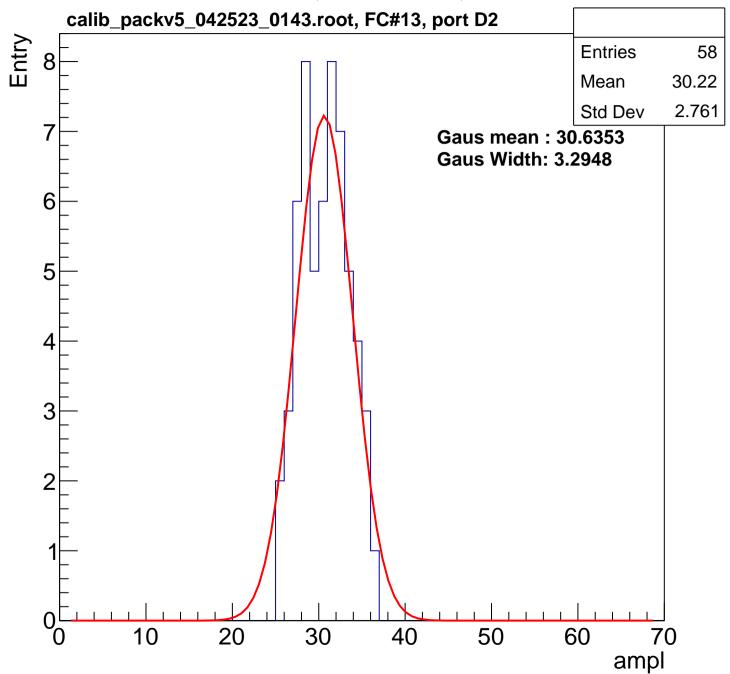


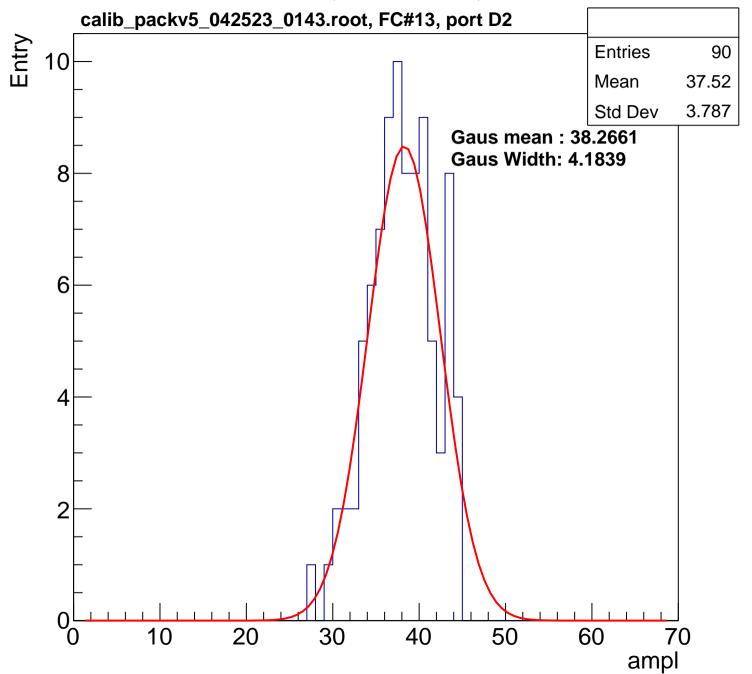


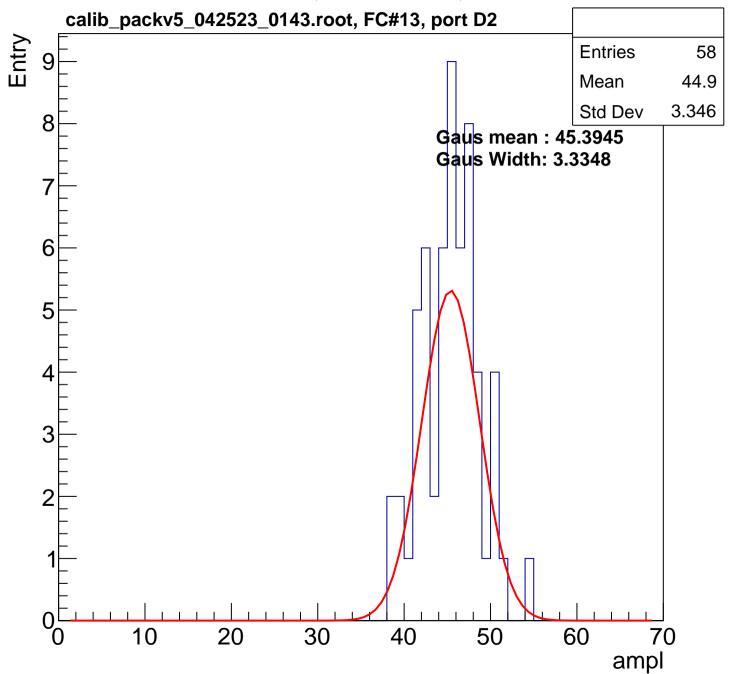


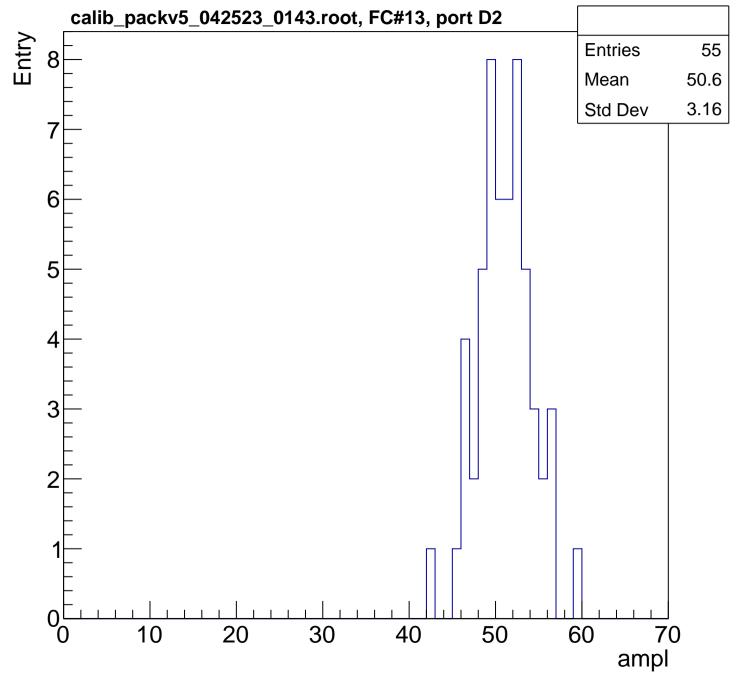


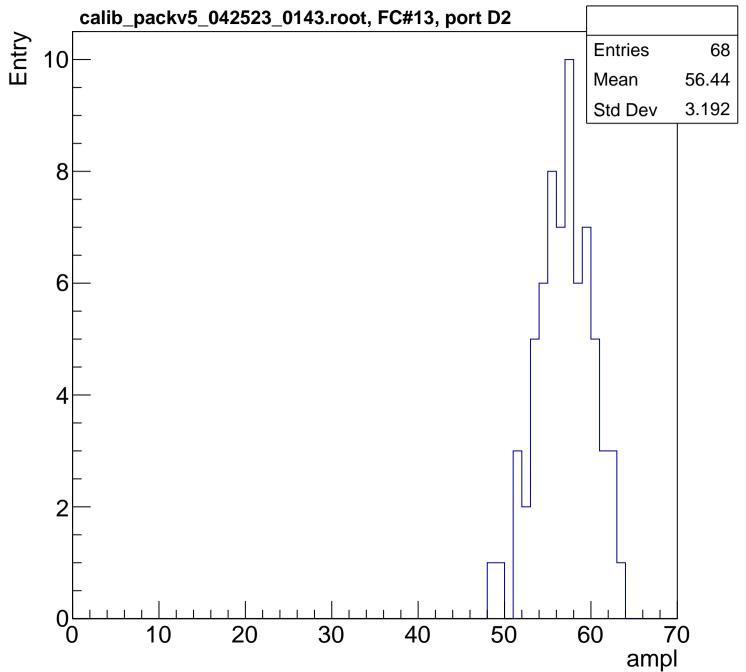


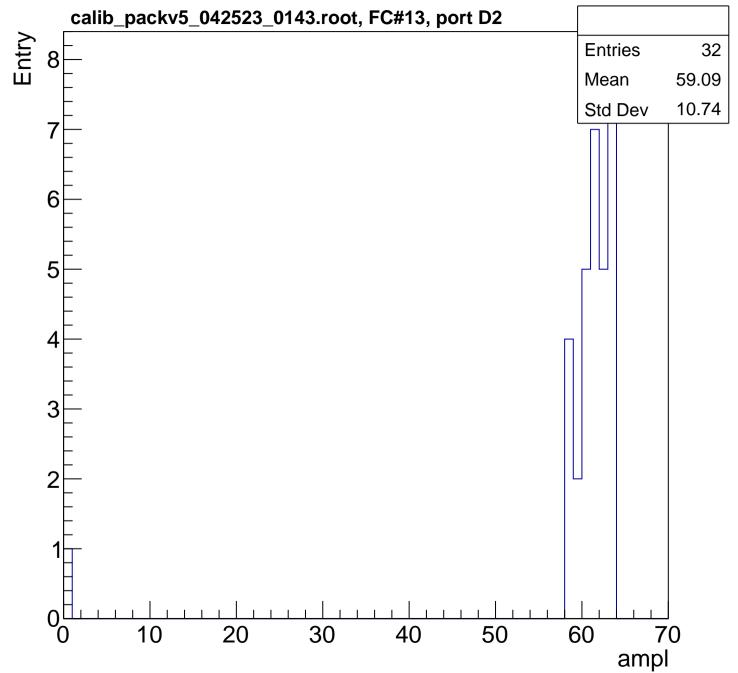


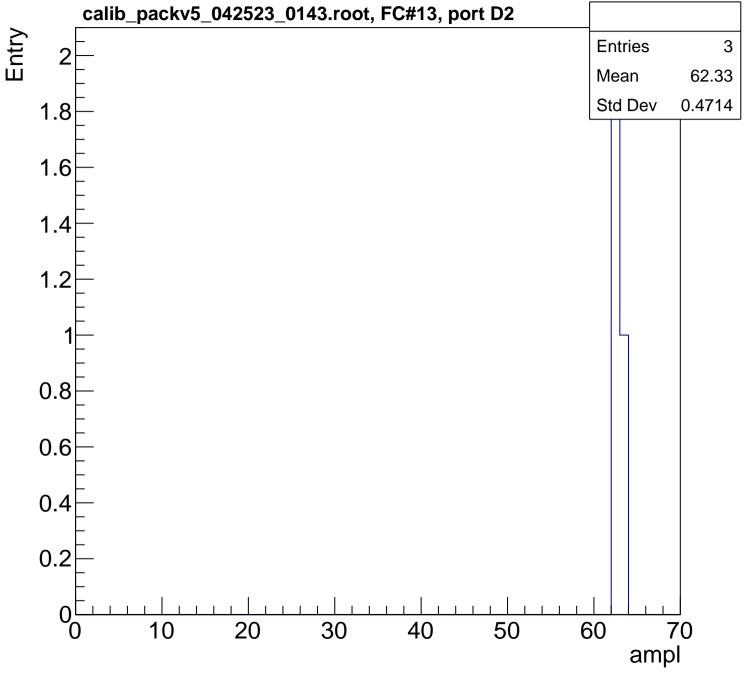


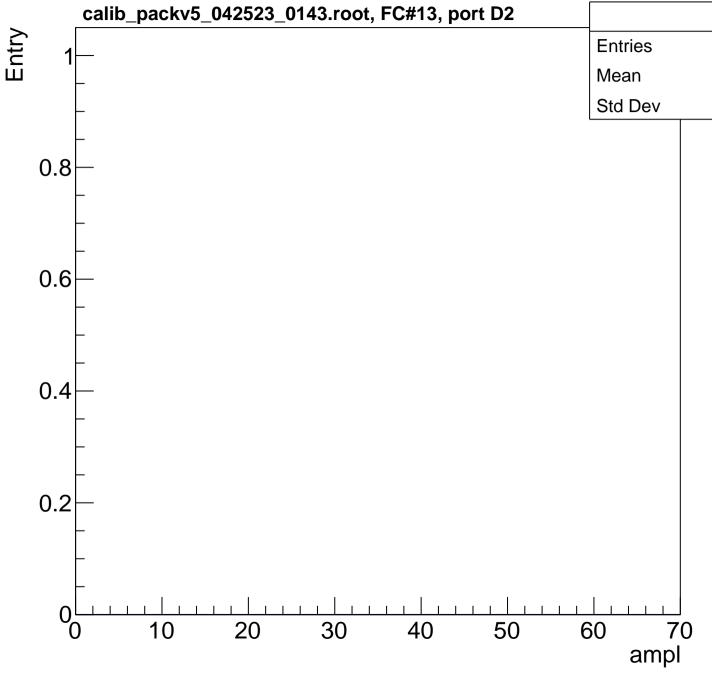


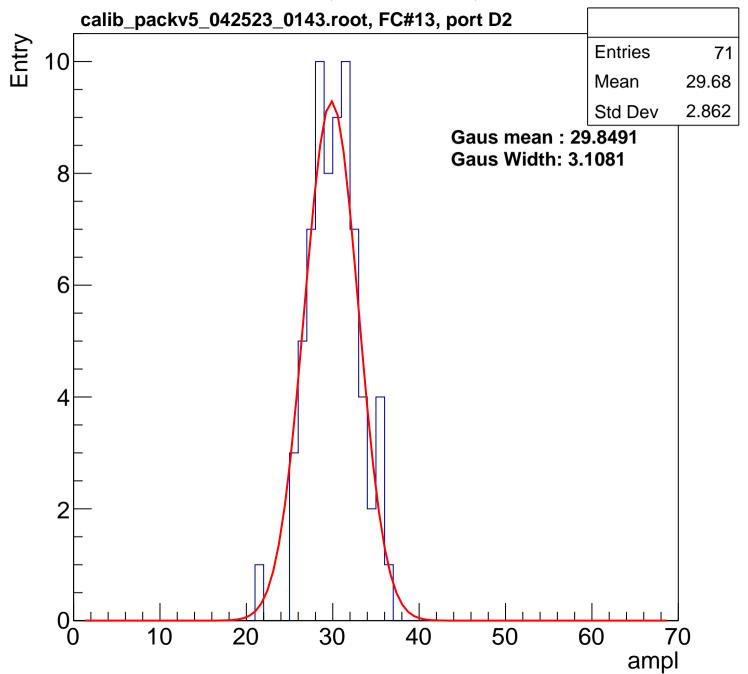


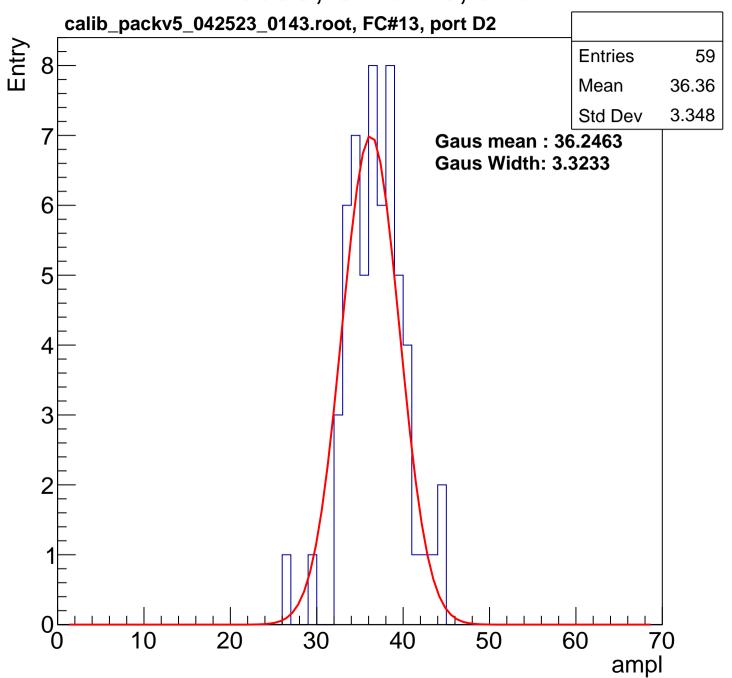


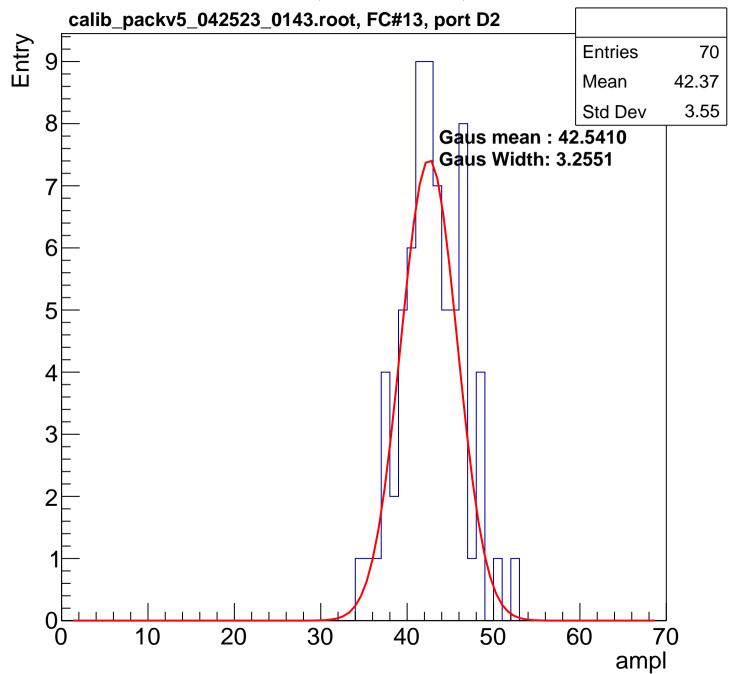


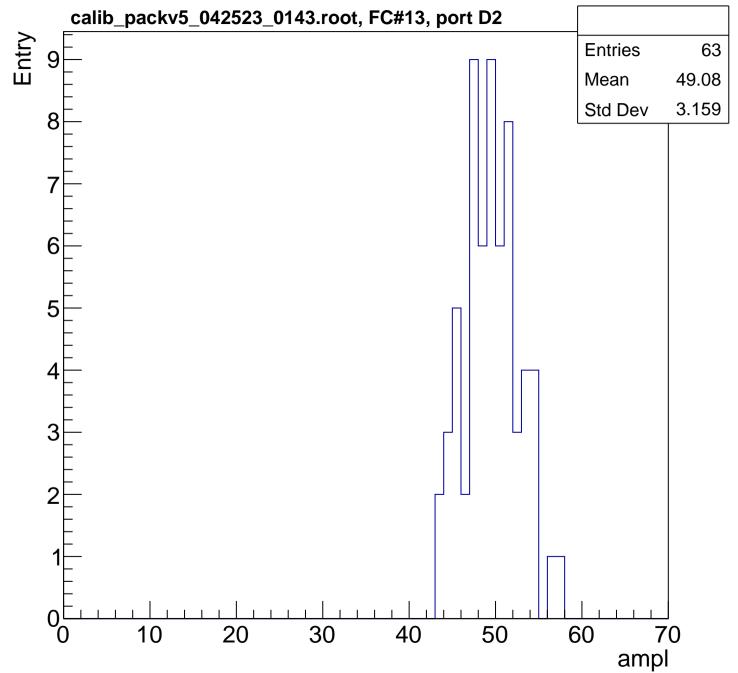


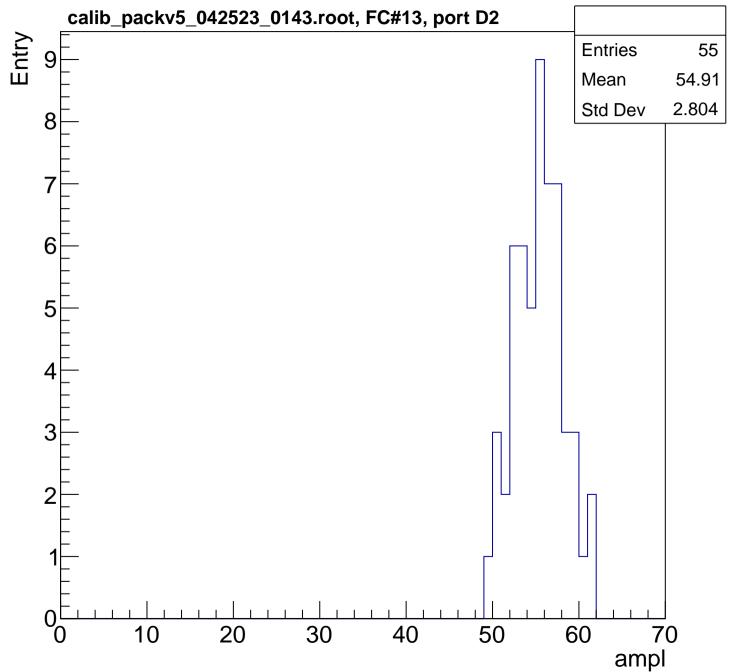


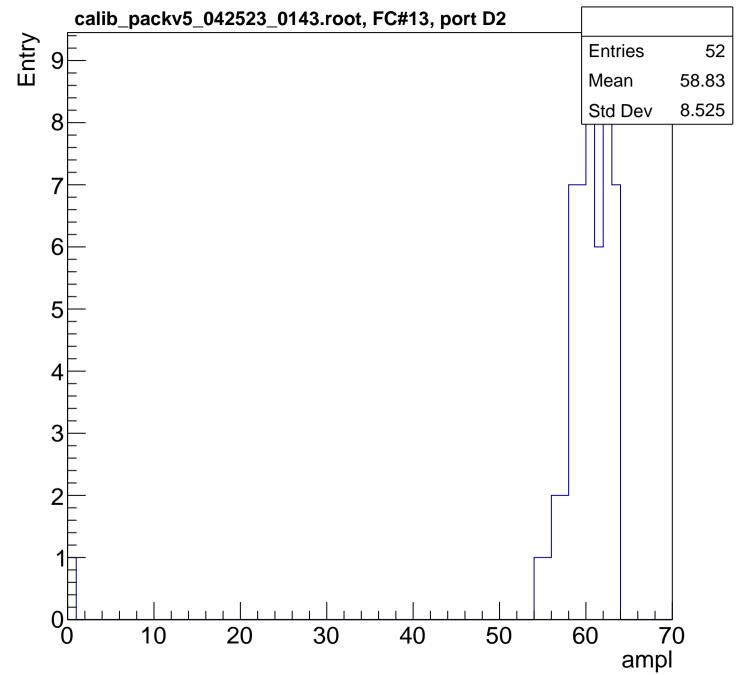


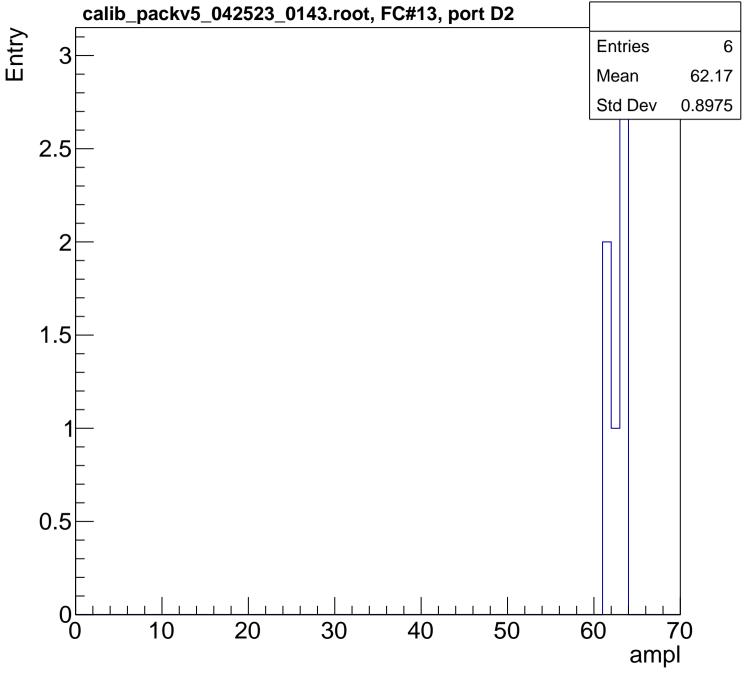




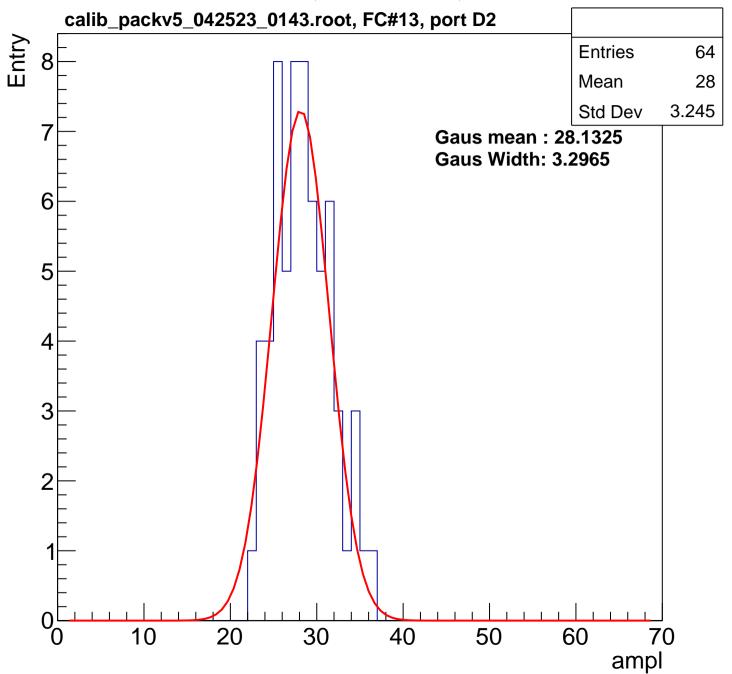


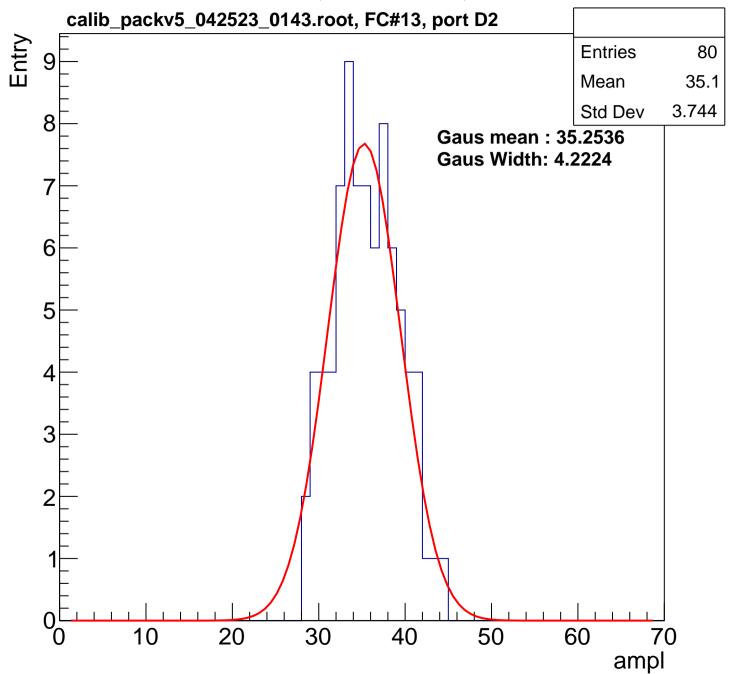


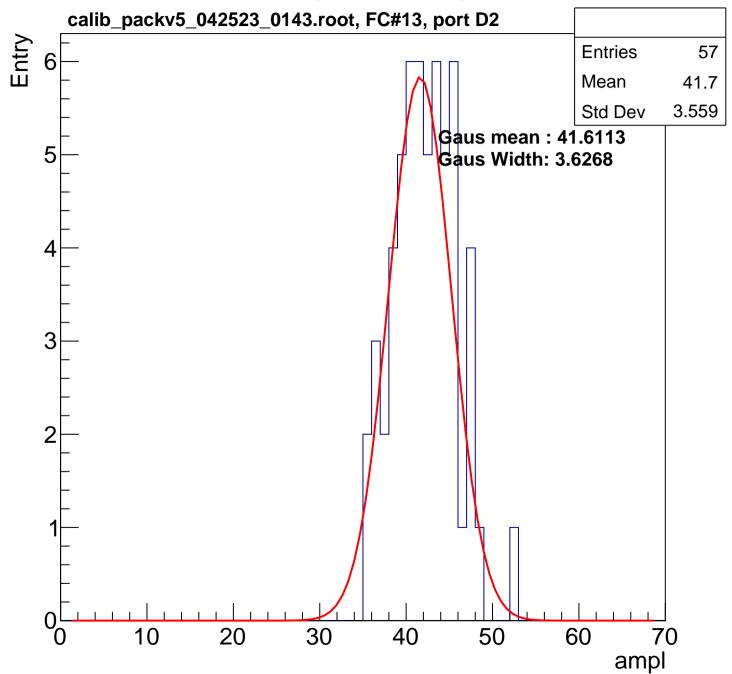


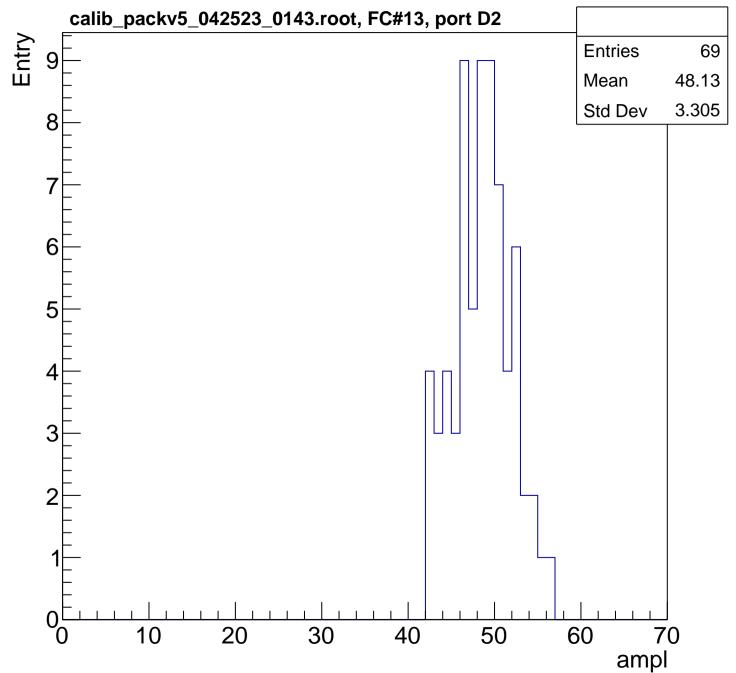


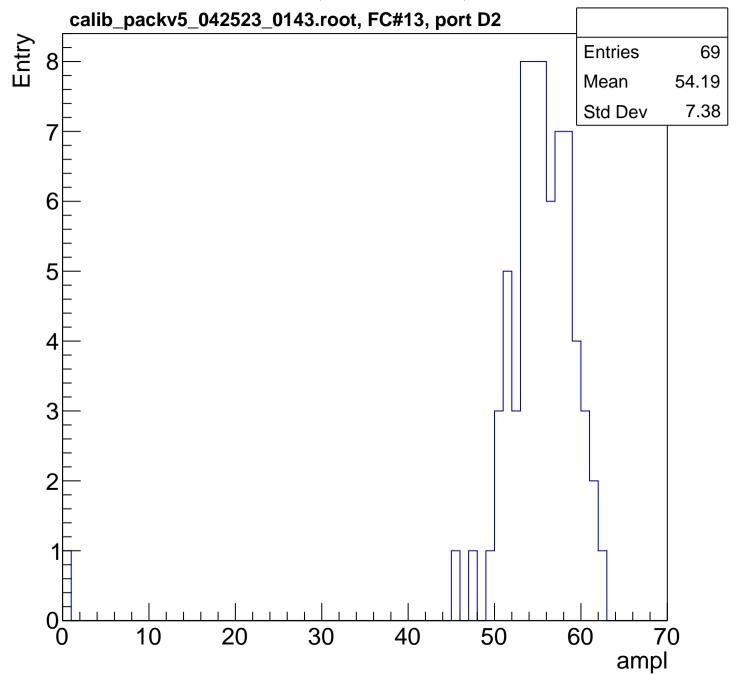
B1L003S, U7-ch46, adc7 calib_packv5_042523_0143.root, FC#13, port D2 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

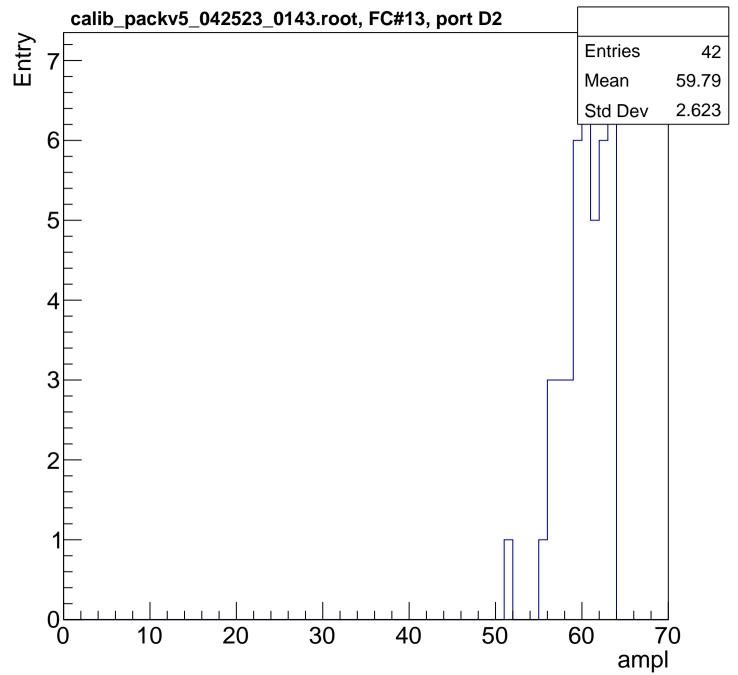


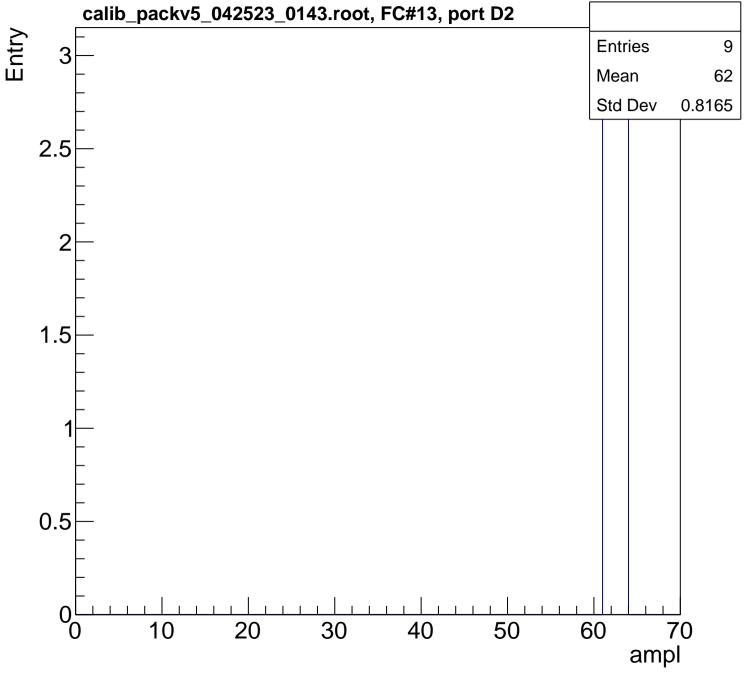




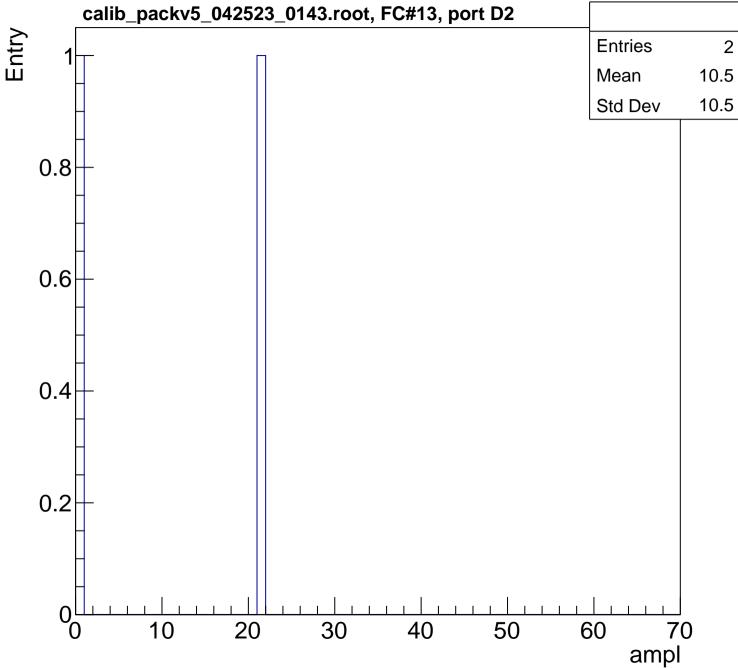


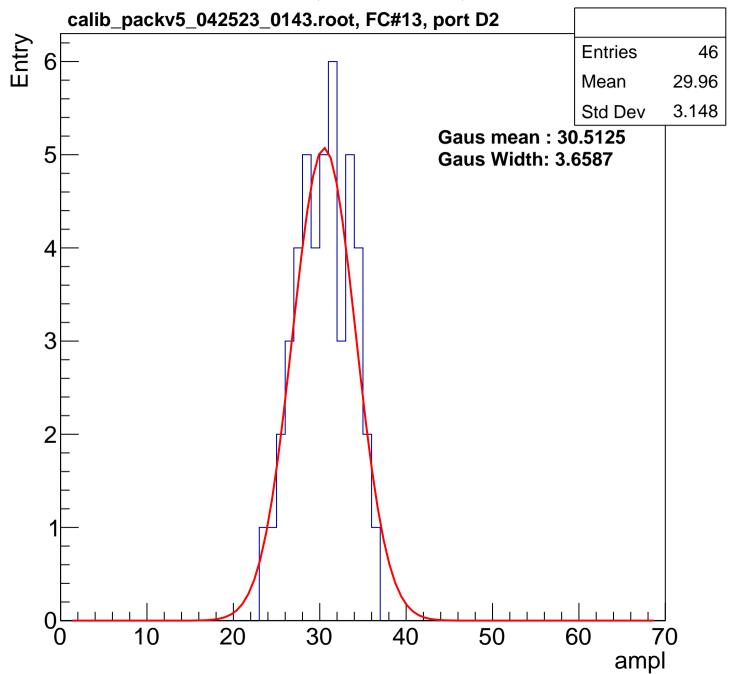


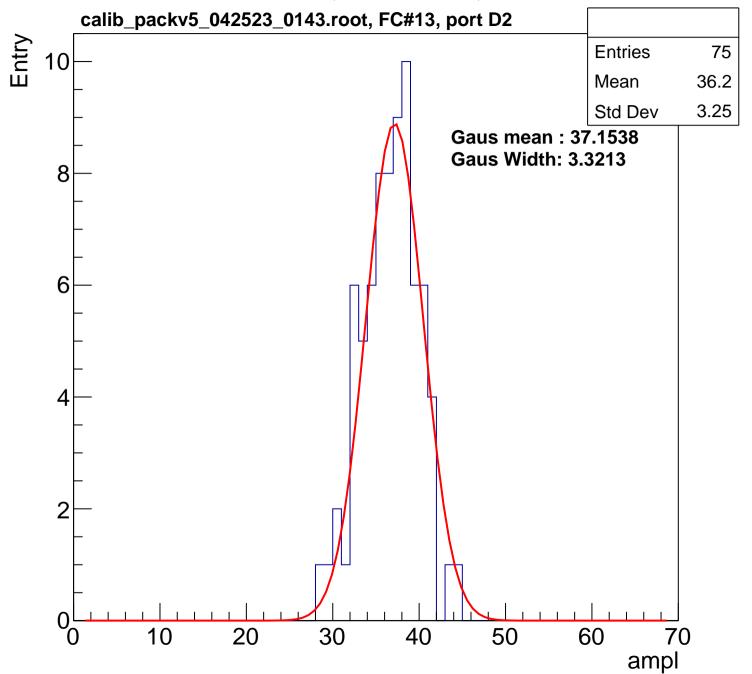


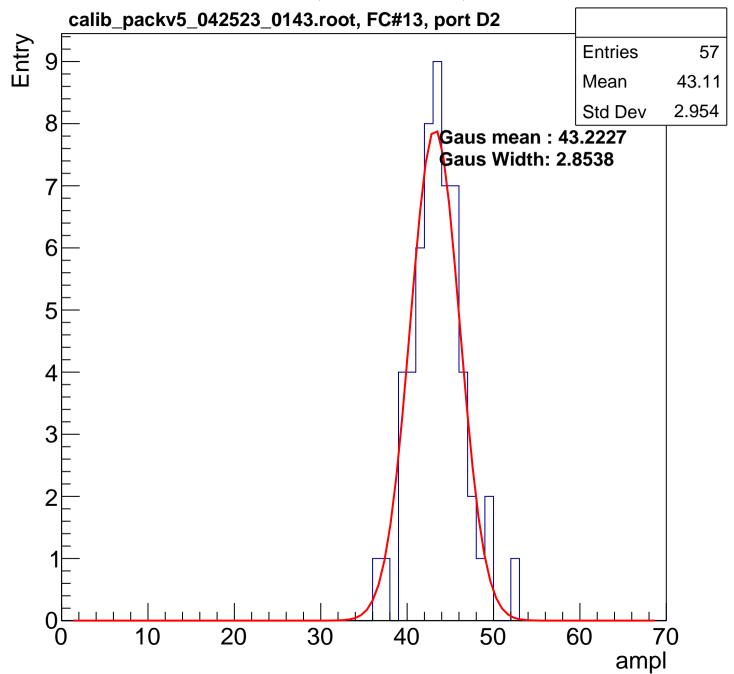


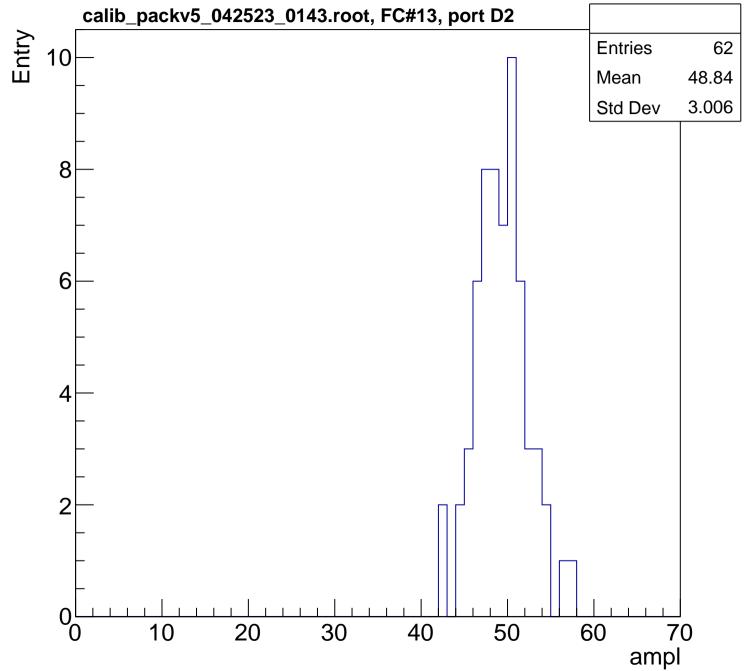
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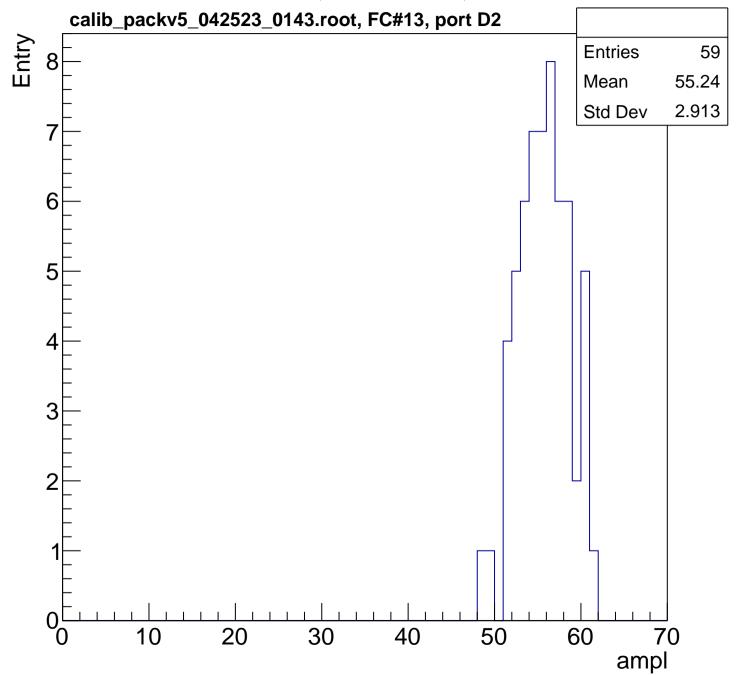


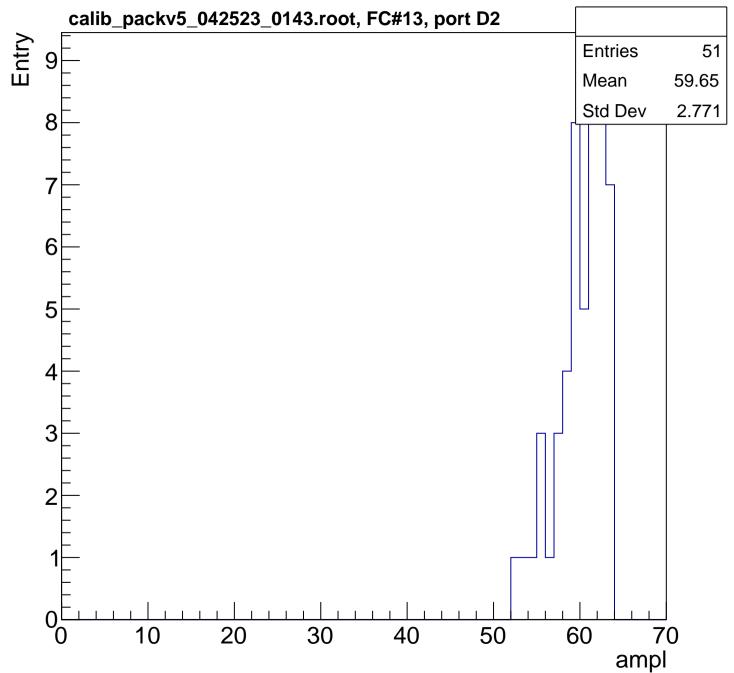


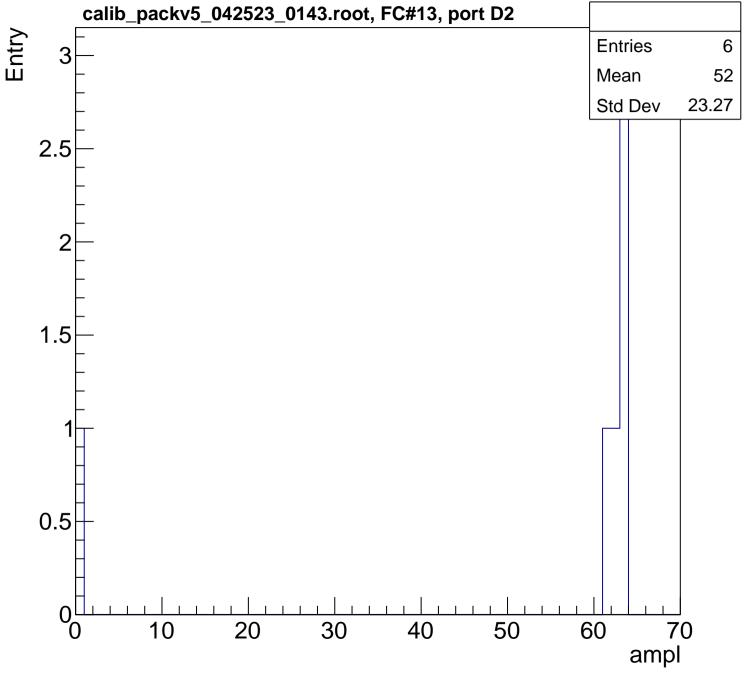




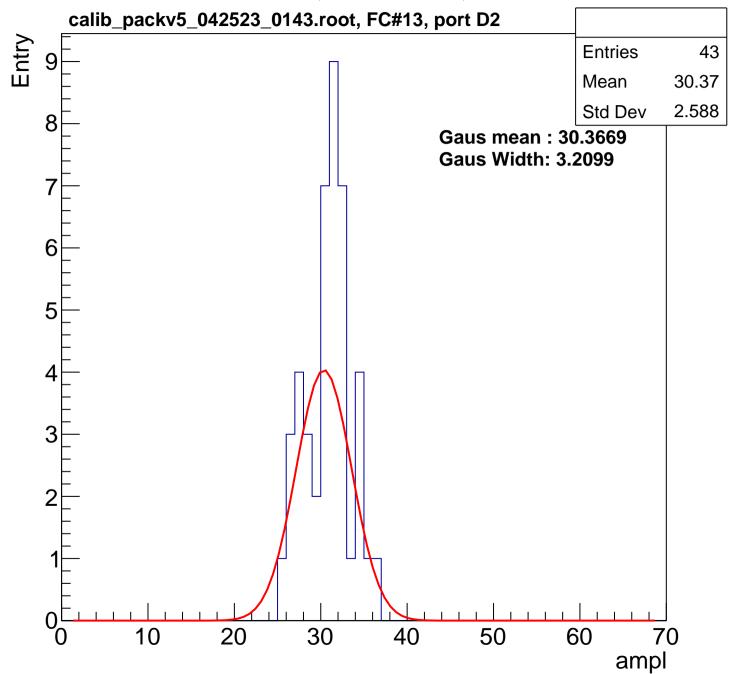


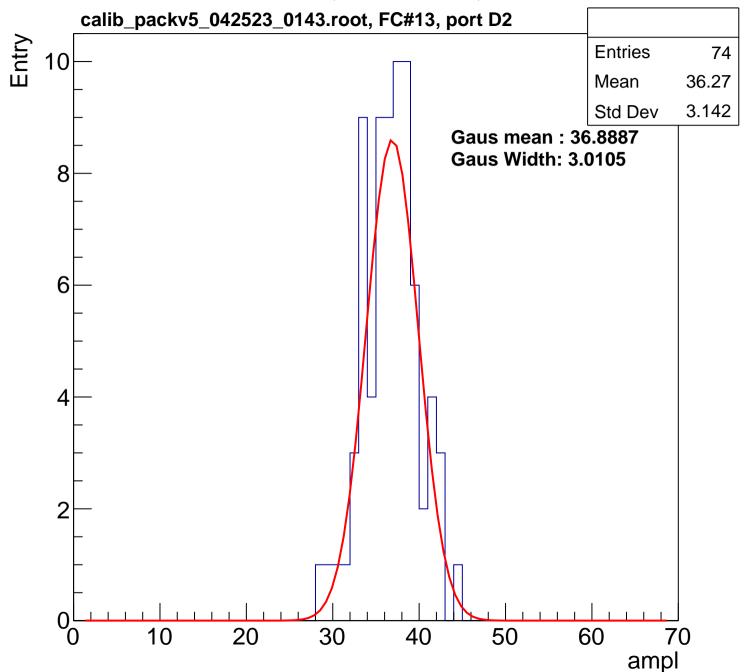


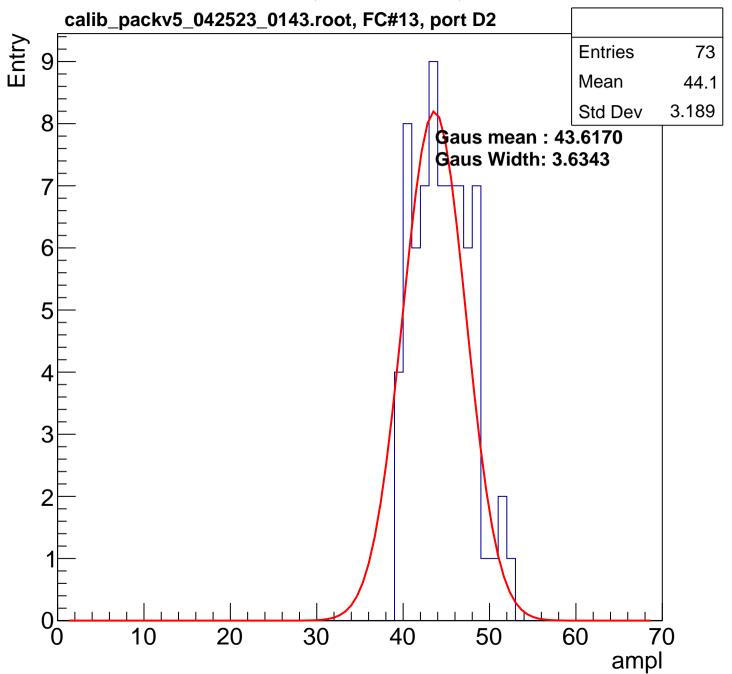


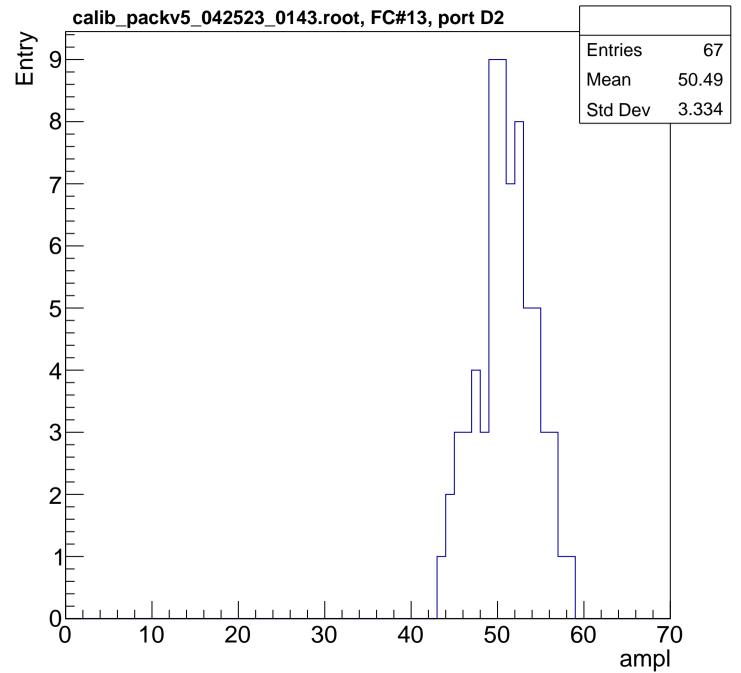


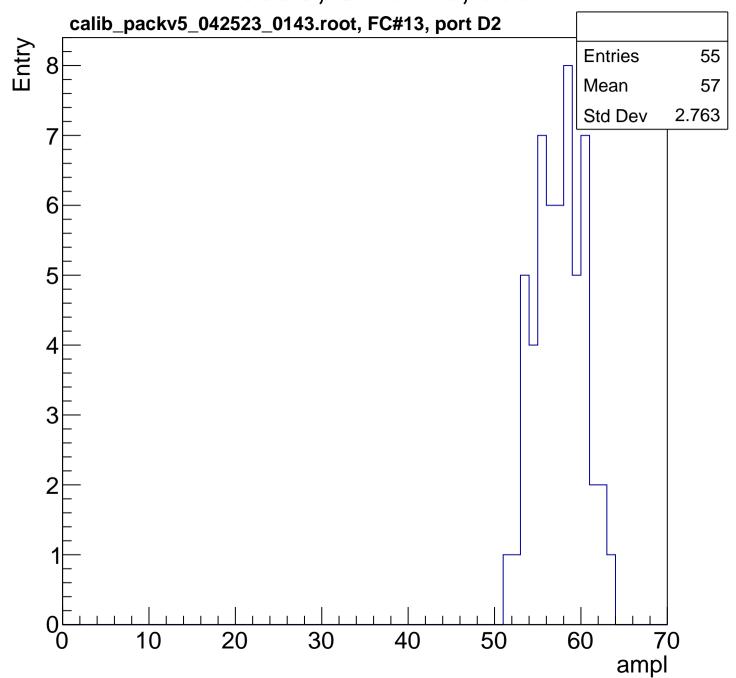


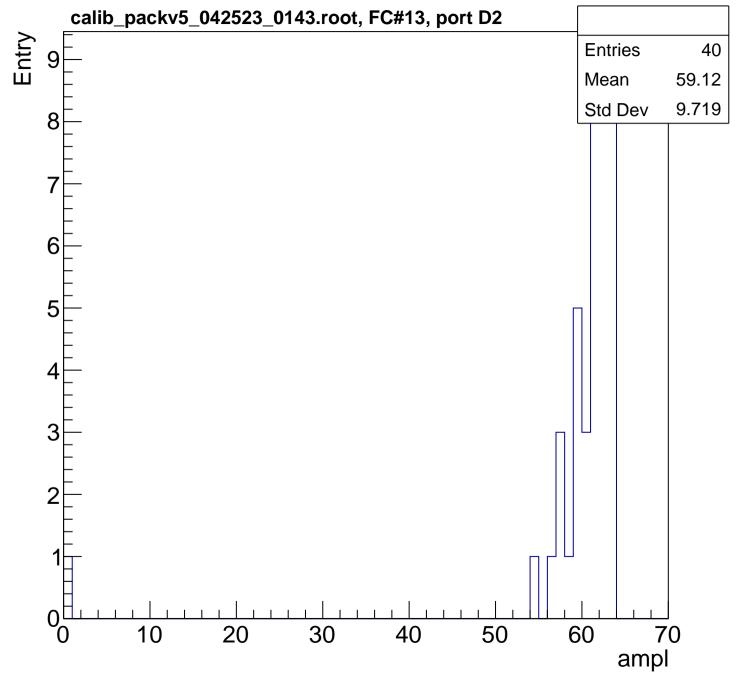


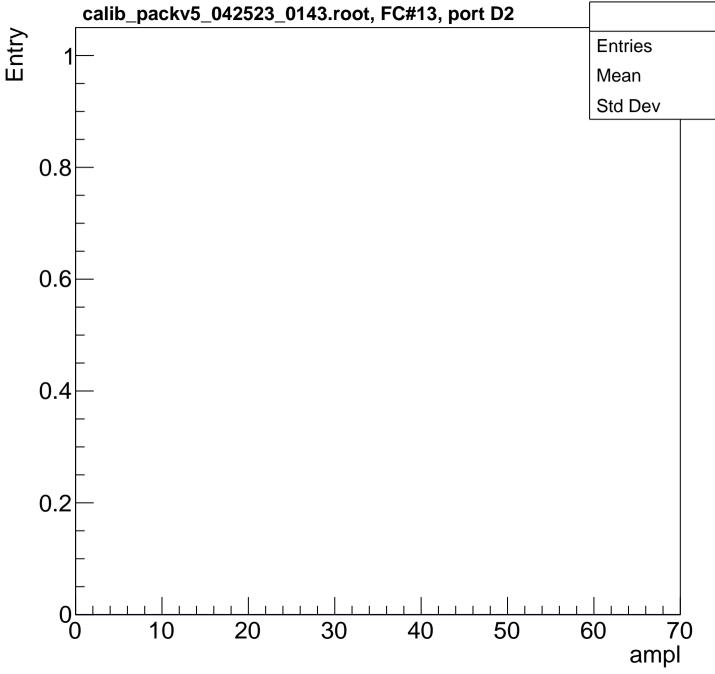




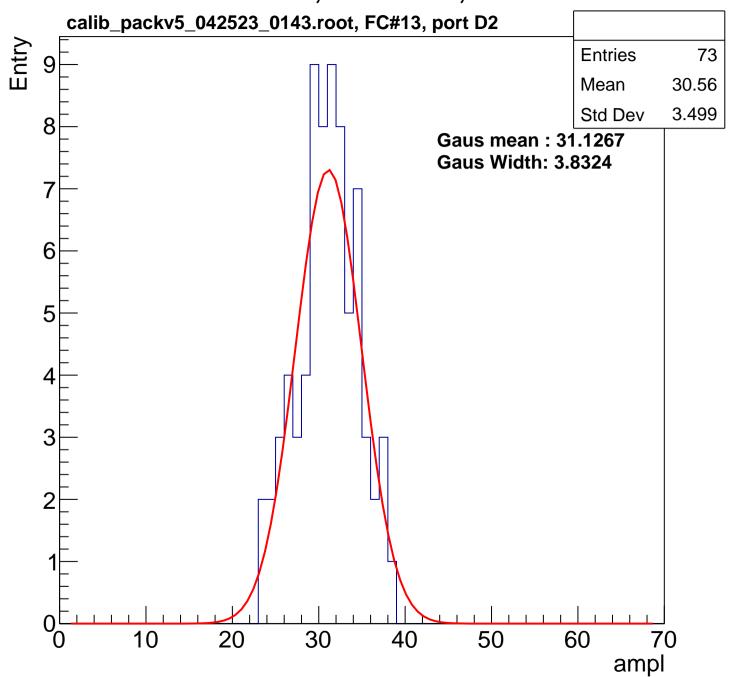


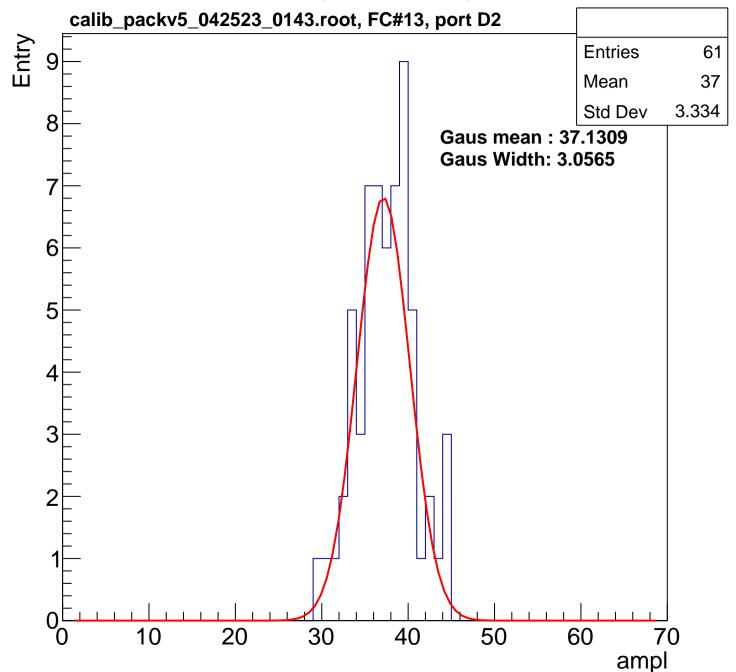


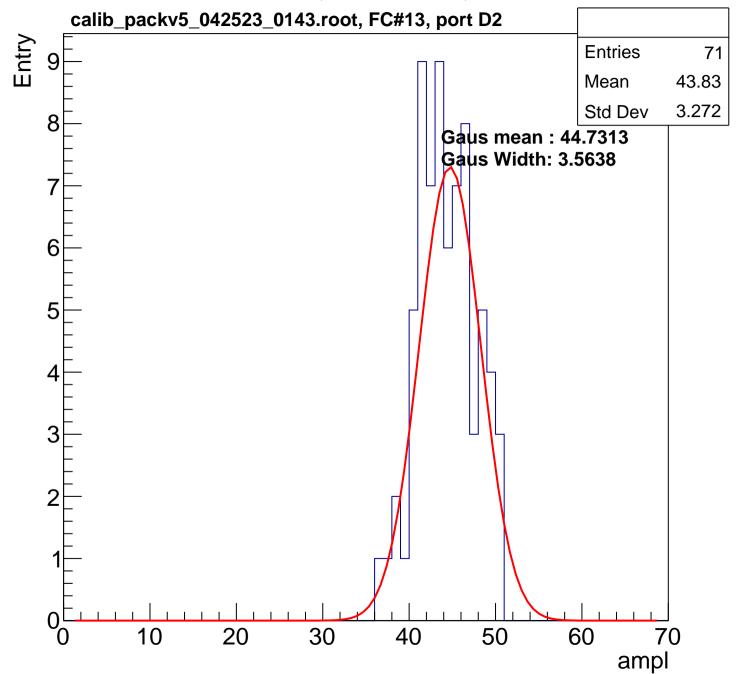


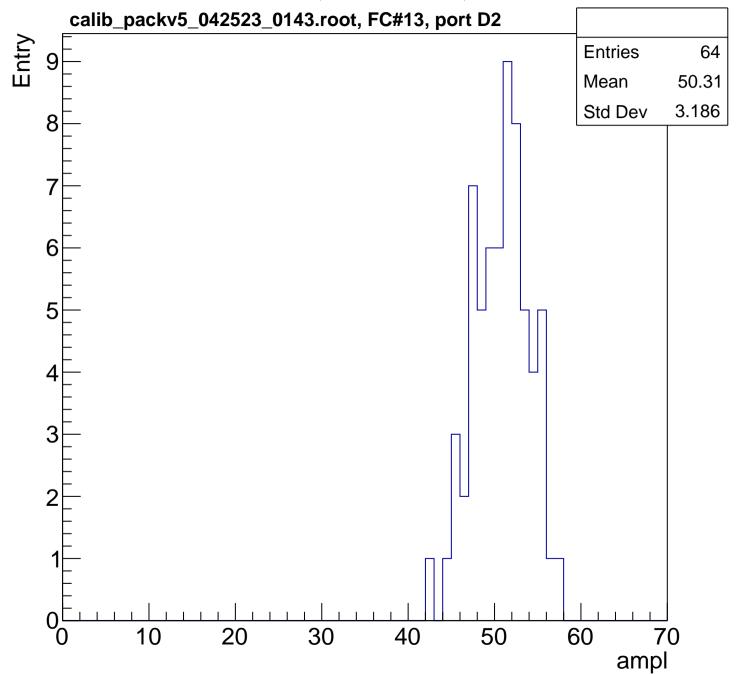


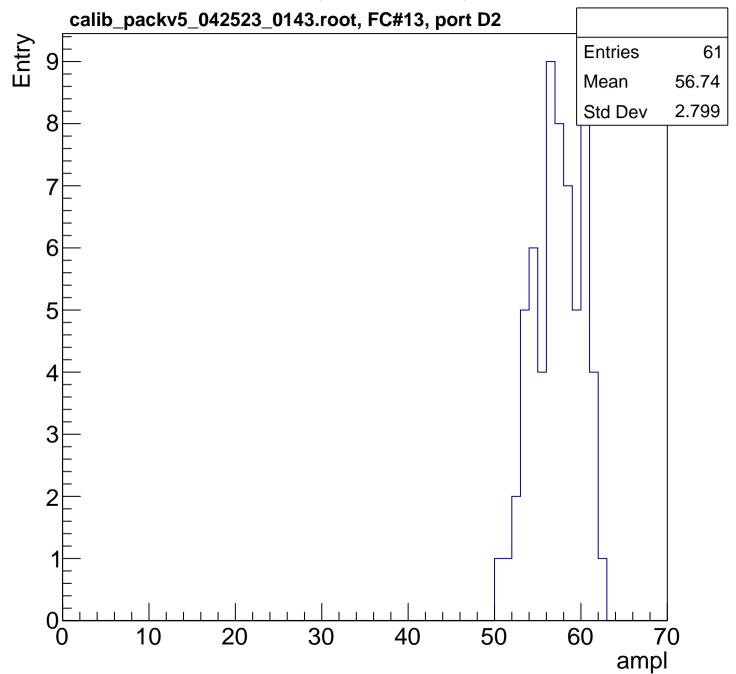


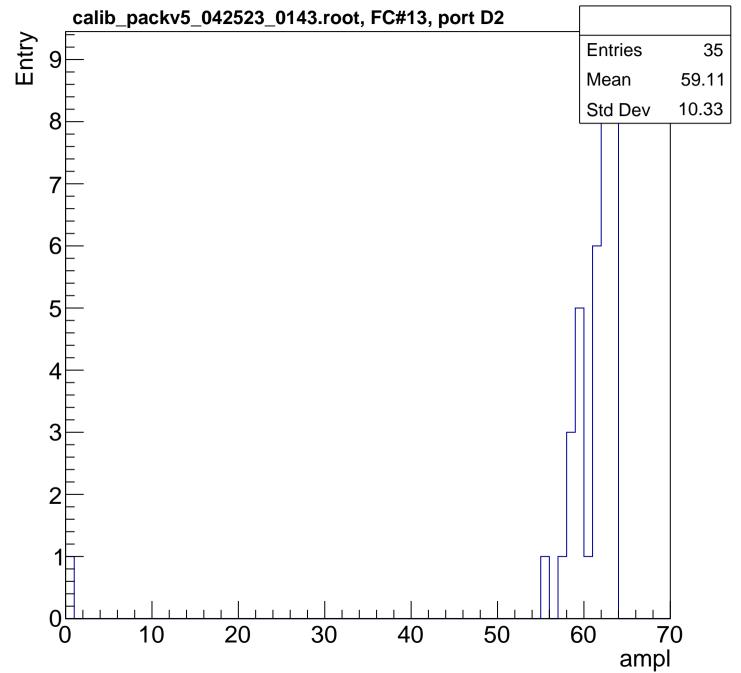


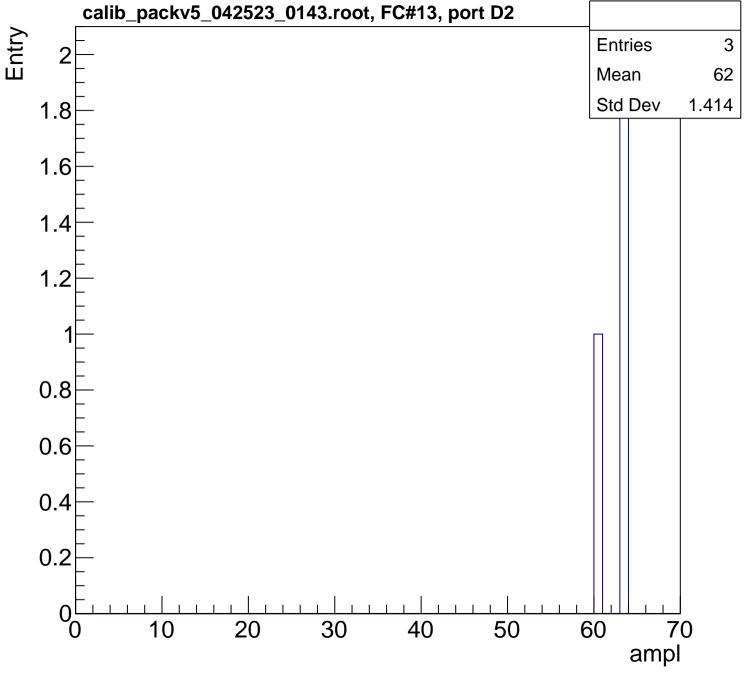




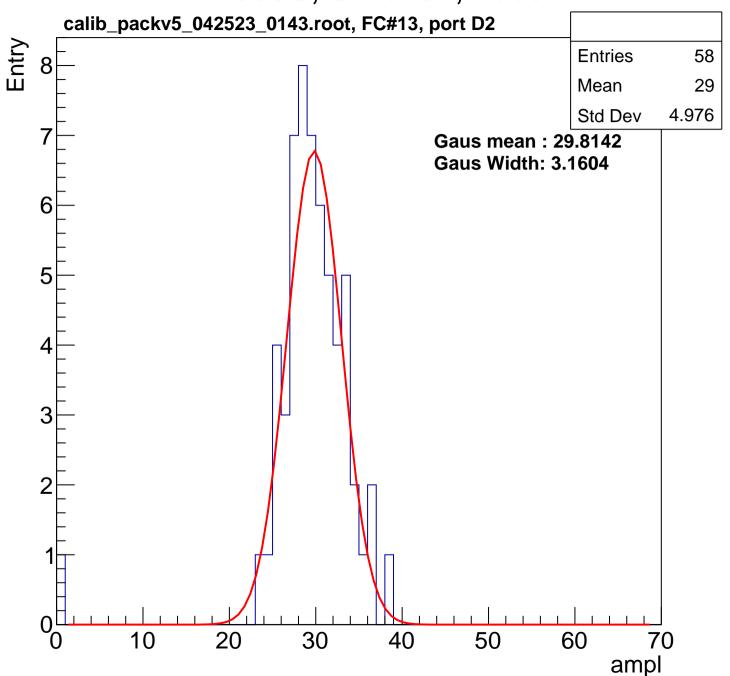


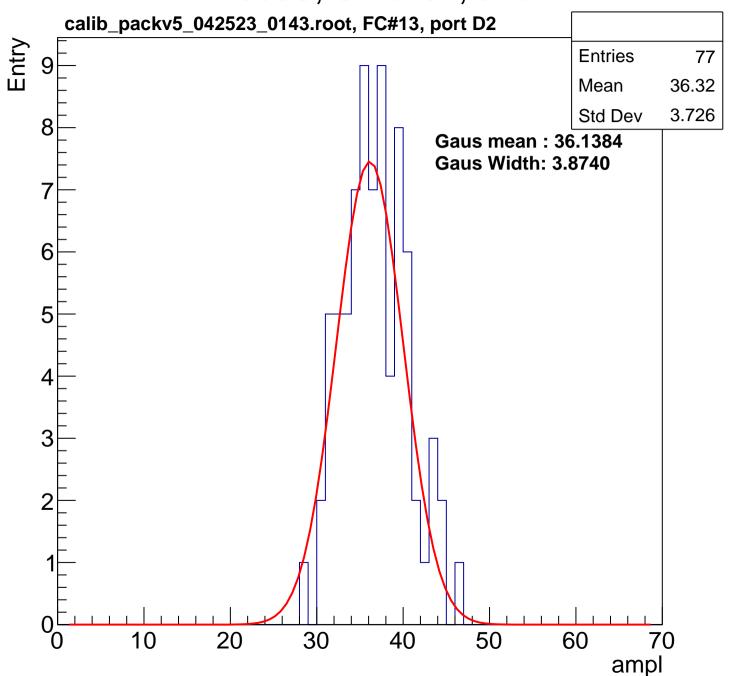


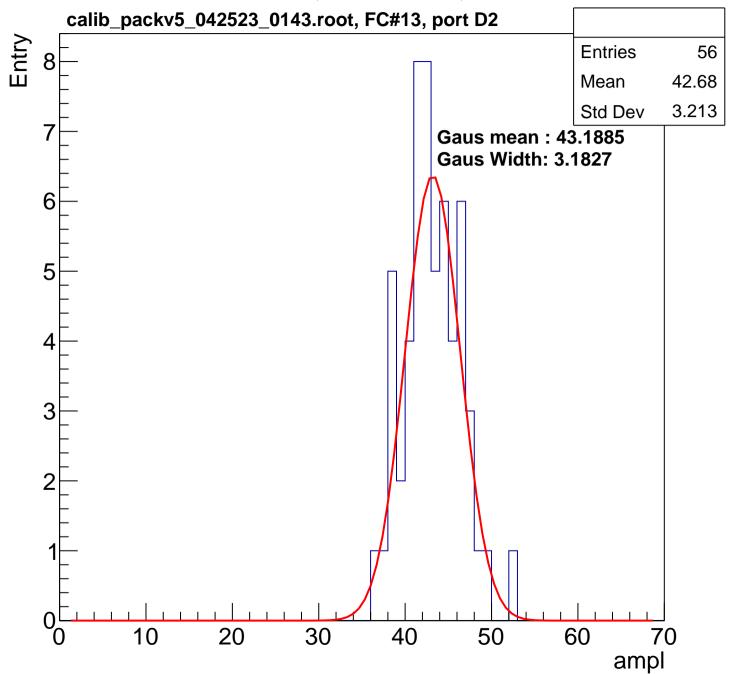


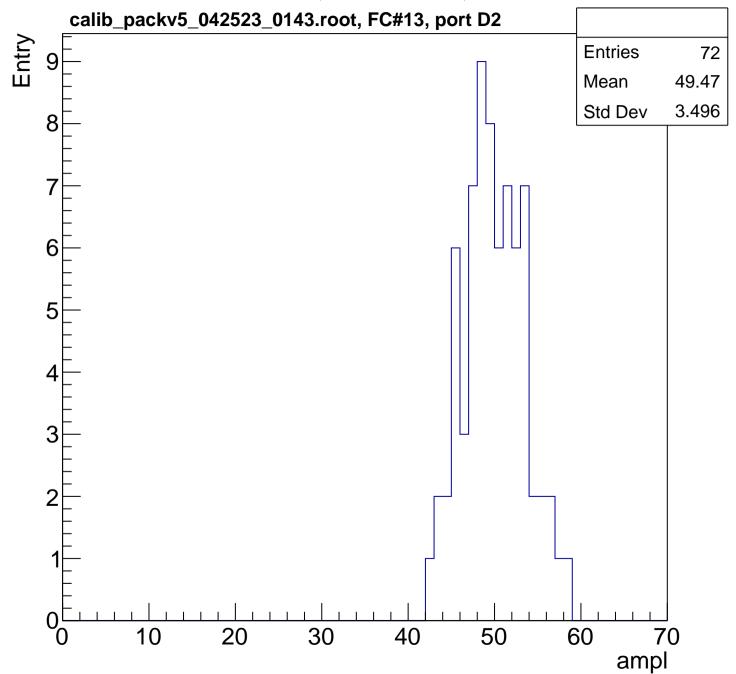


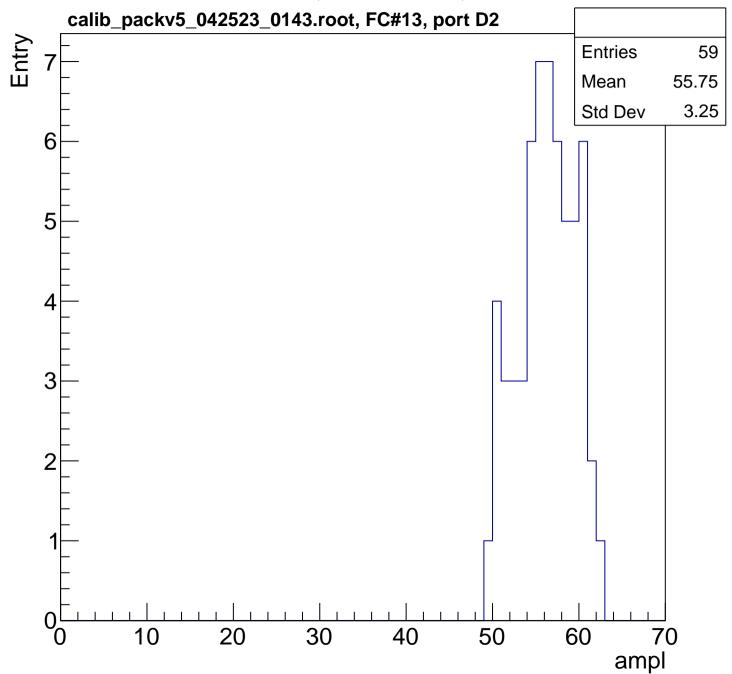
B1L003S, U7-ch50, adc7 calib_packv5_042523_0143.root, FC#13, port D2 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

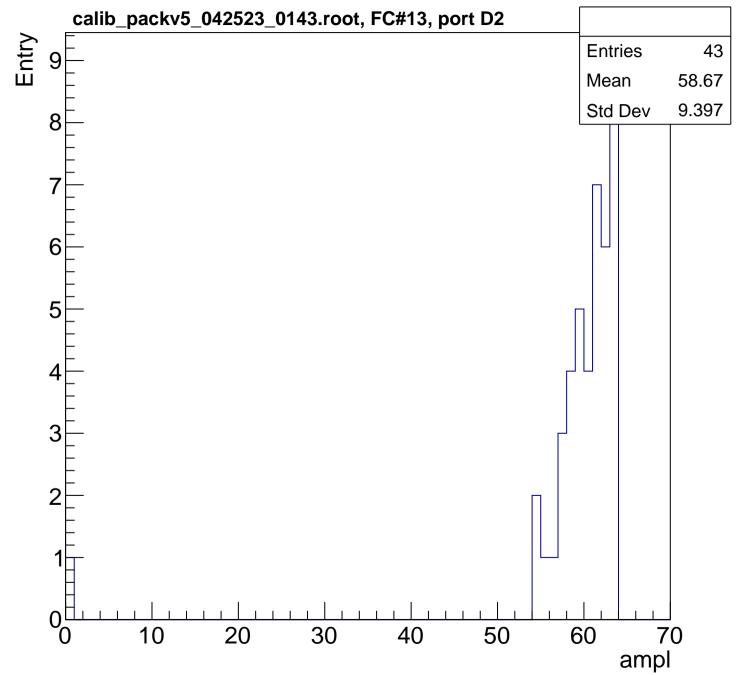


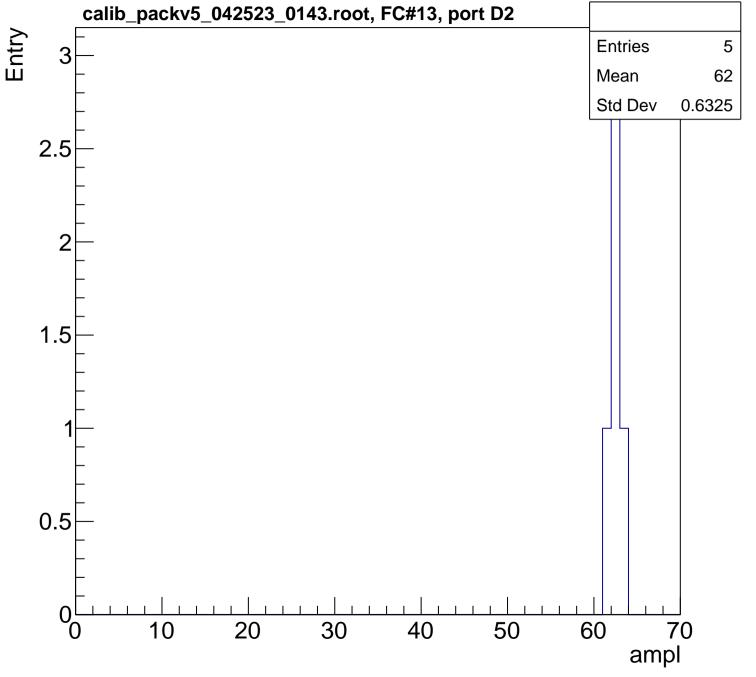


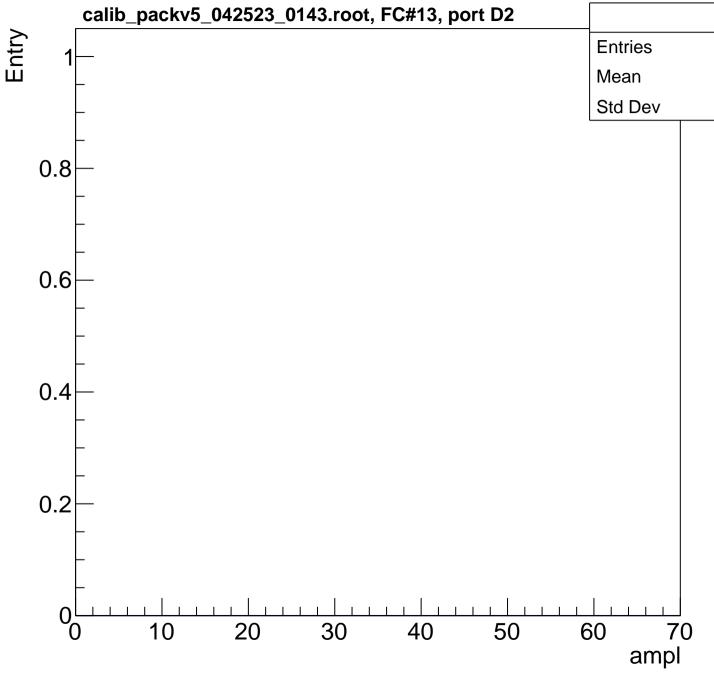


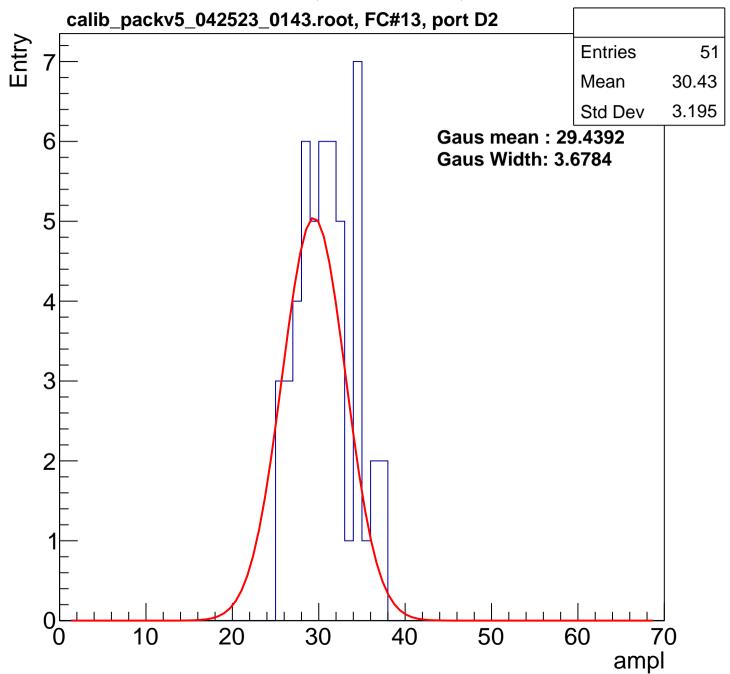


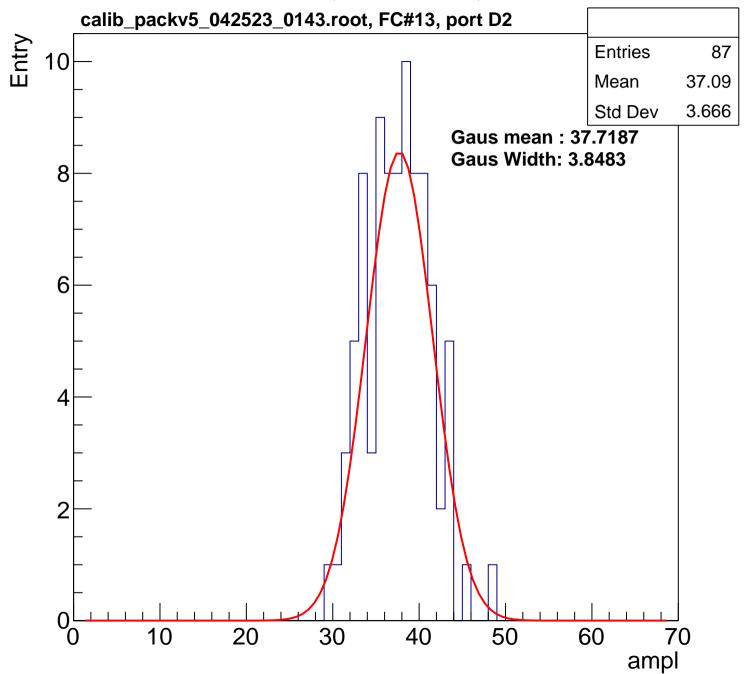


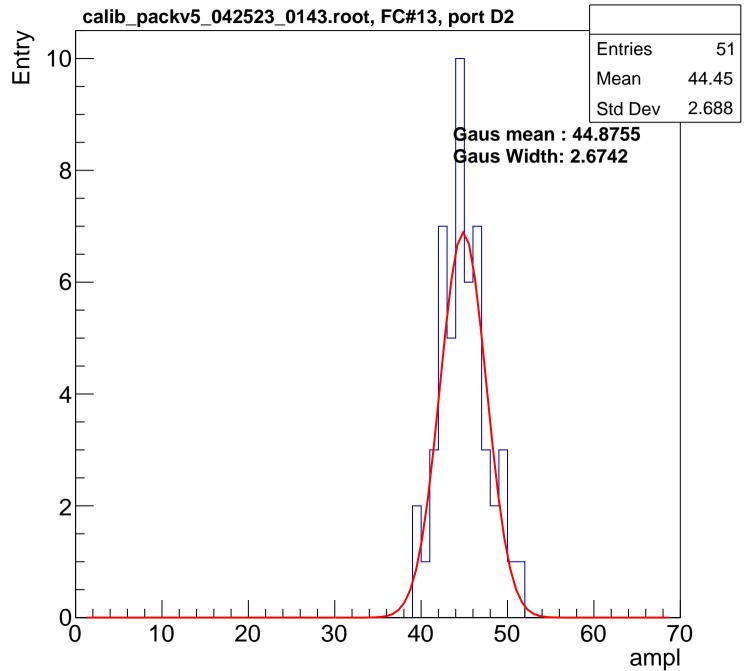


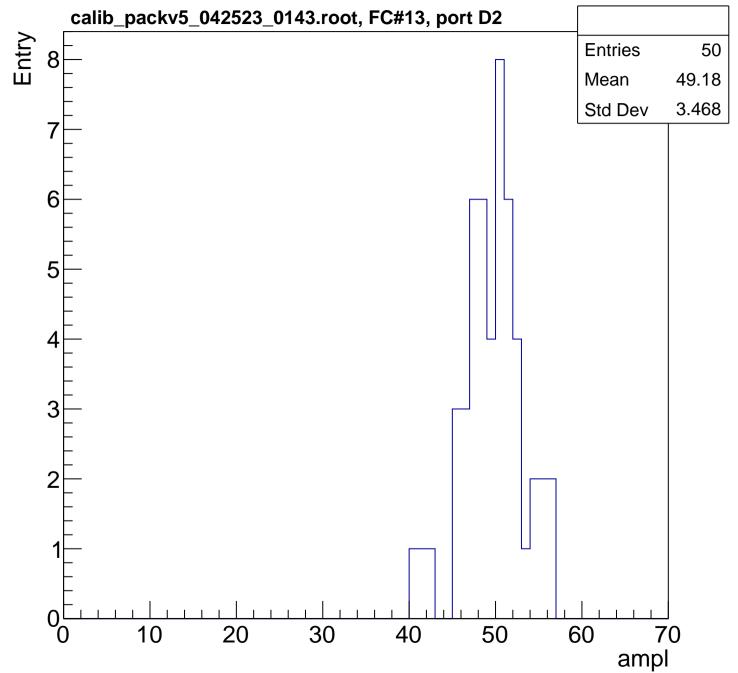


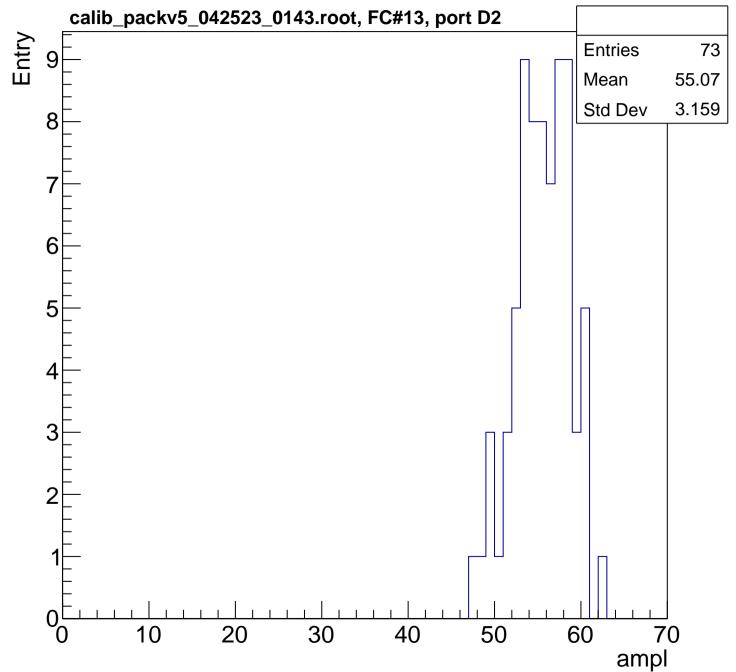


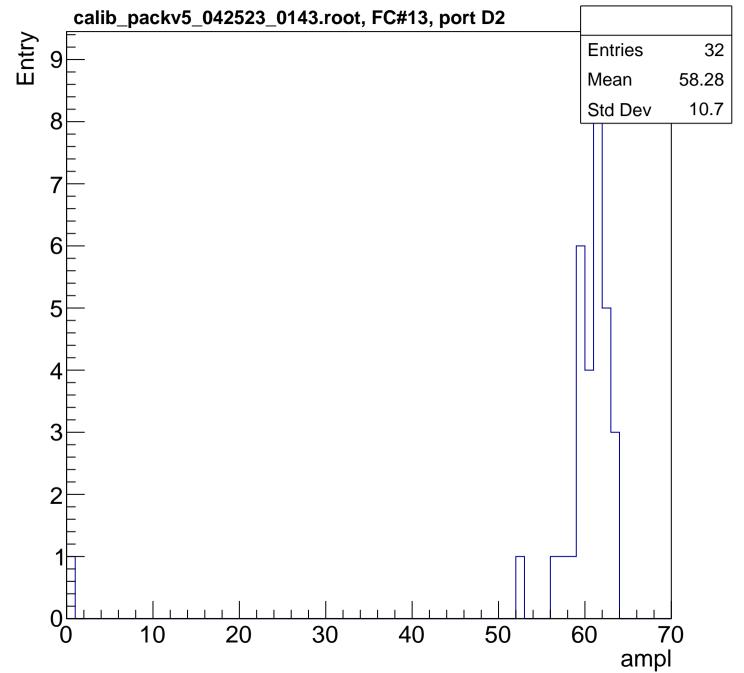


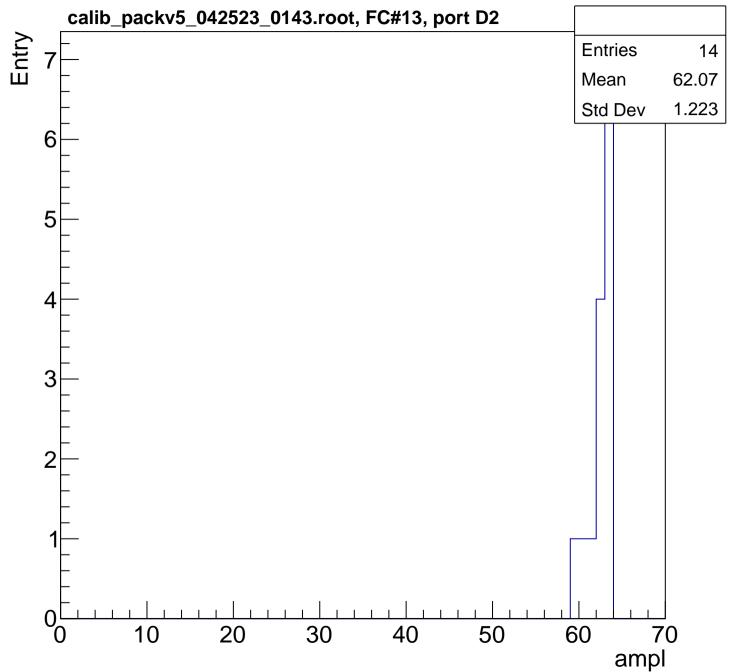




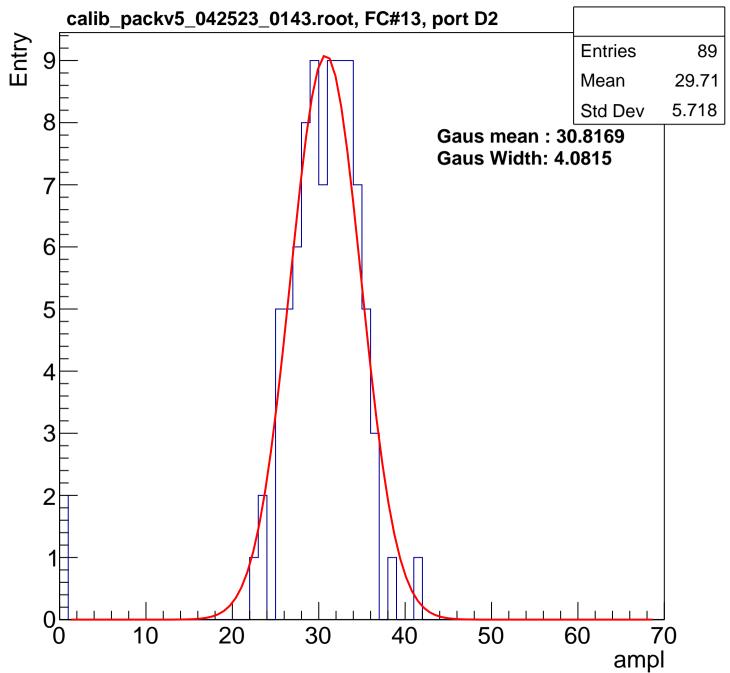


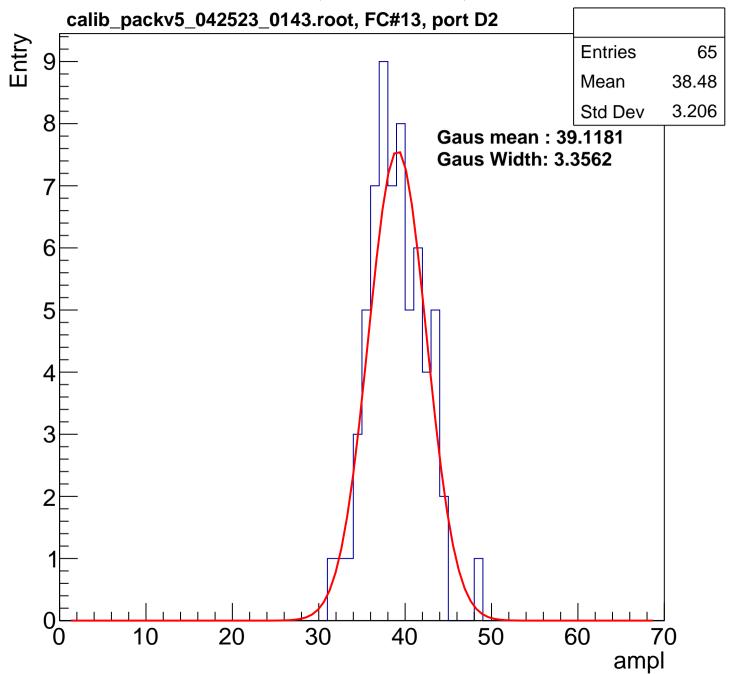


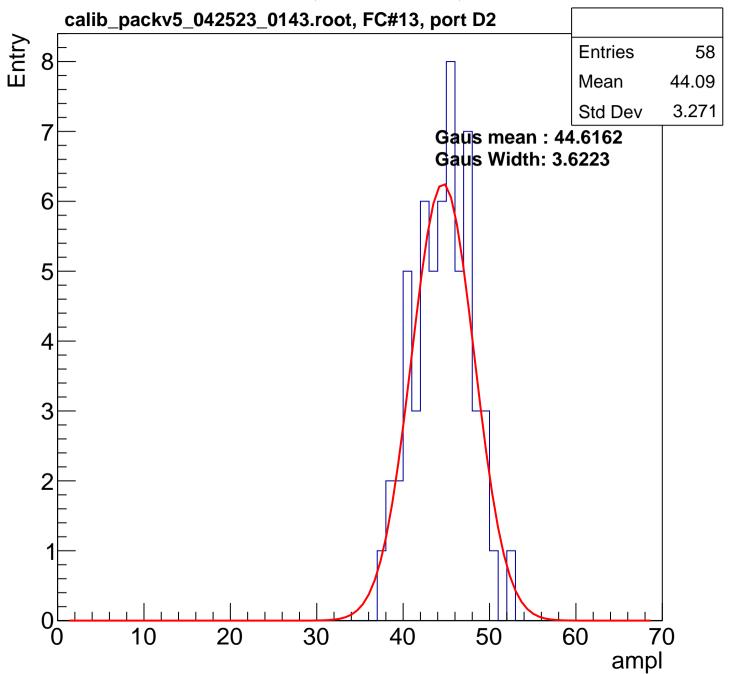


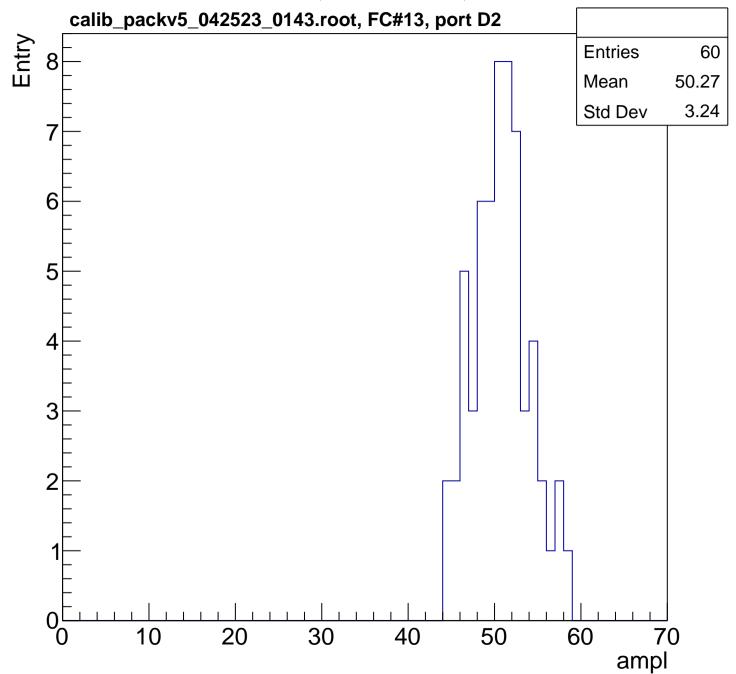


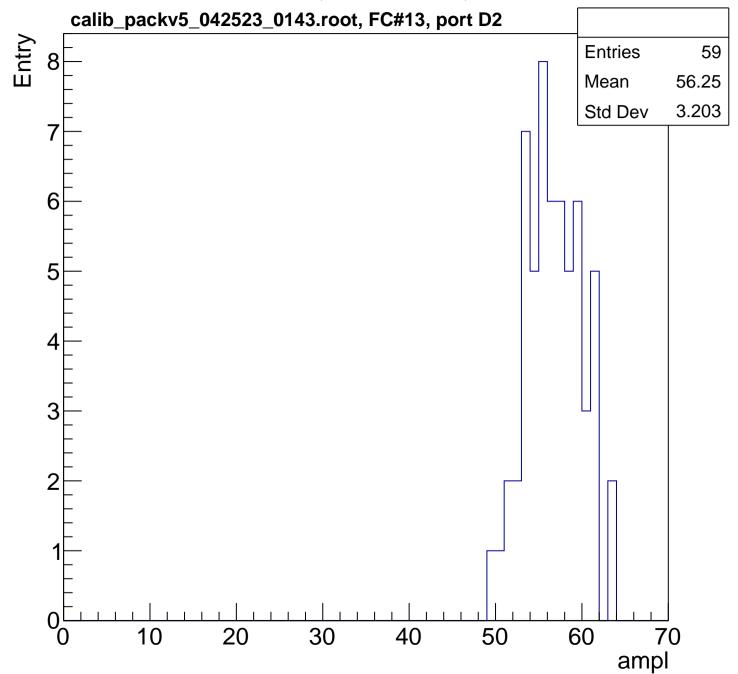
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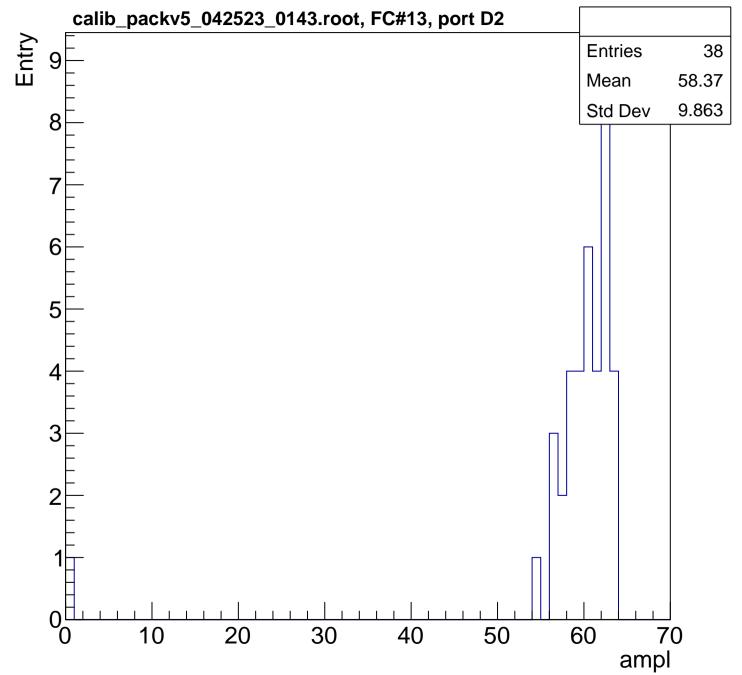


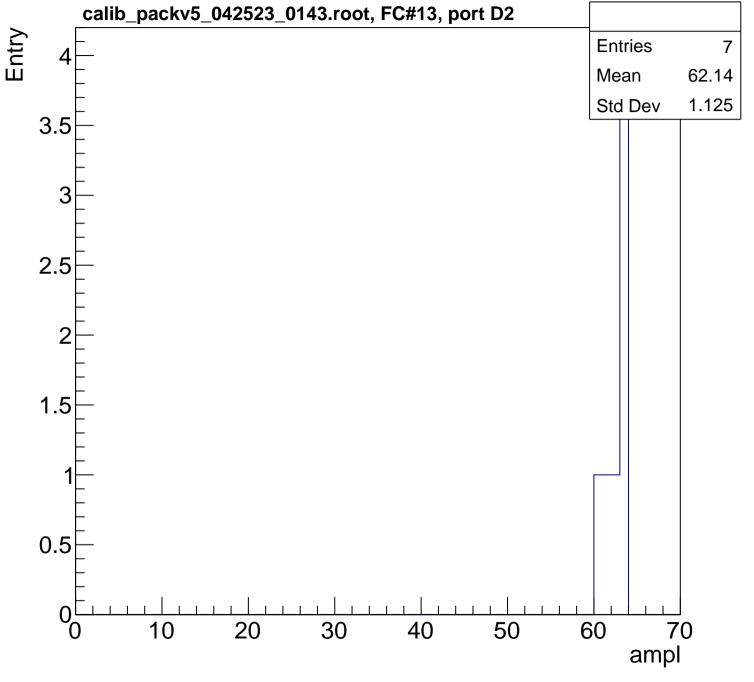




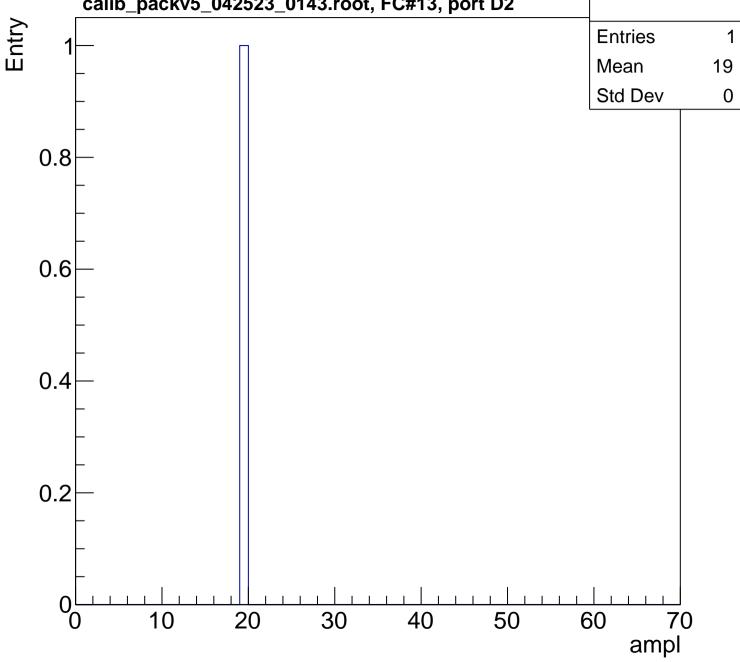


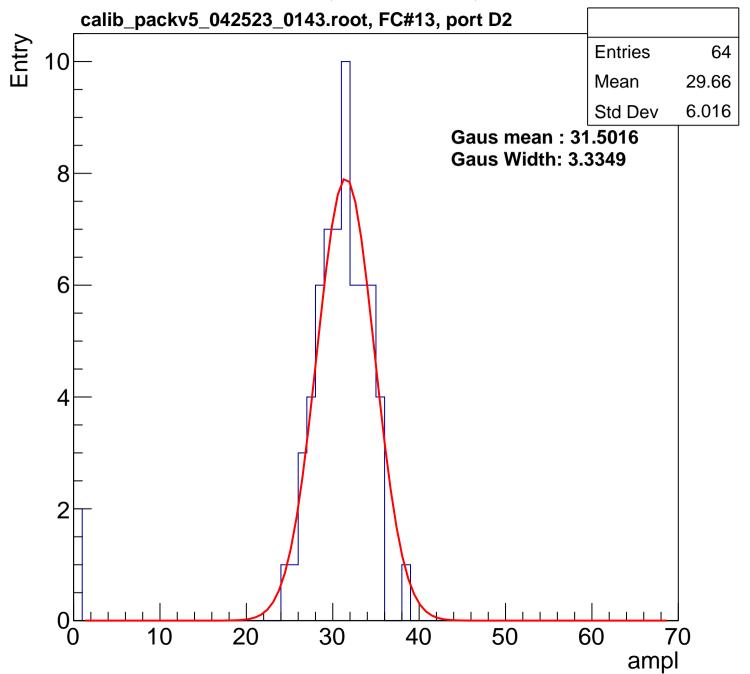


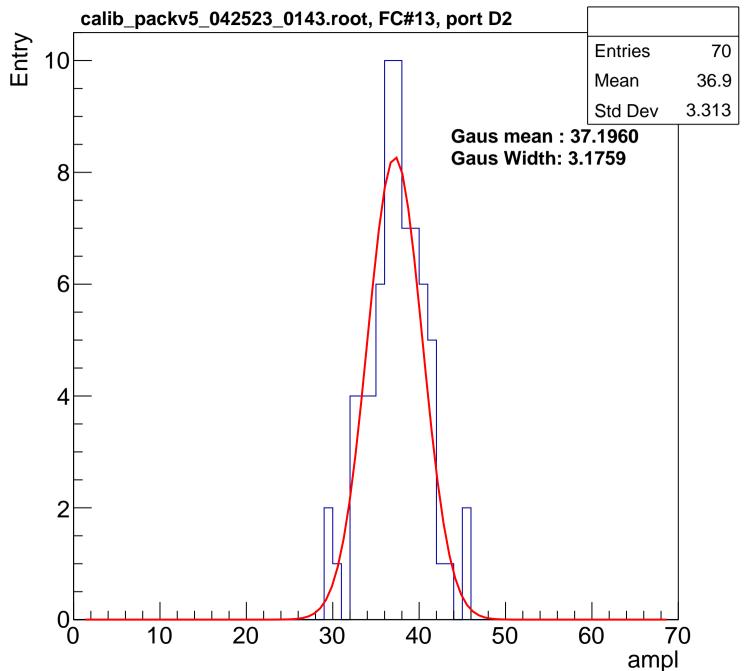


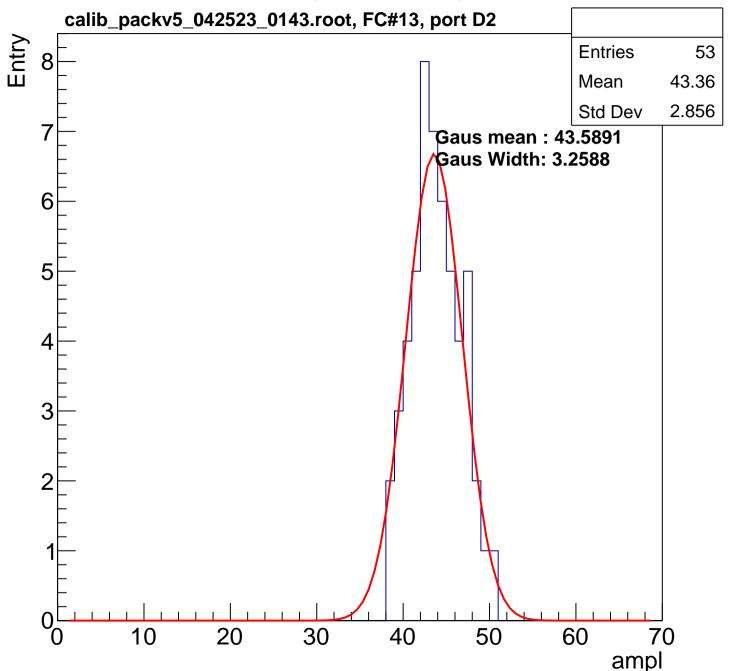


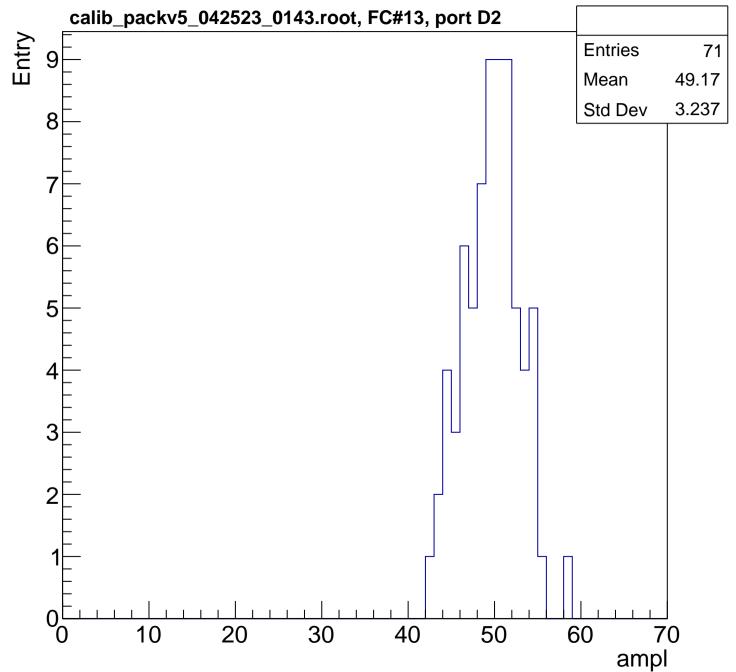
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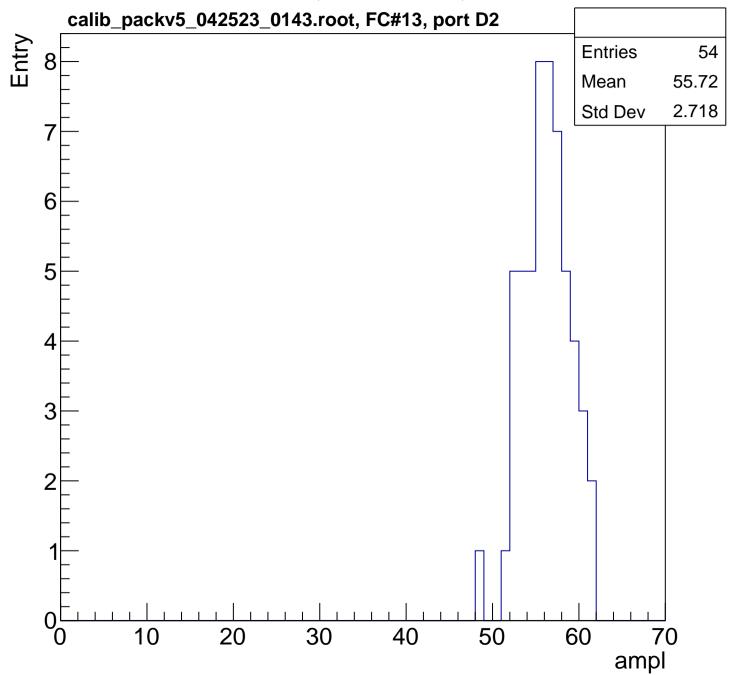


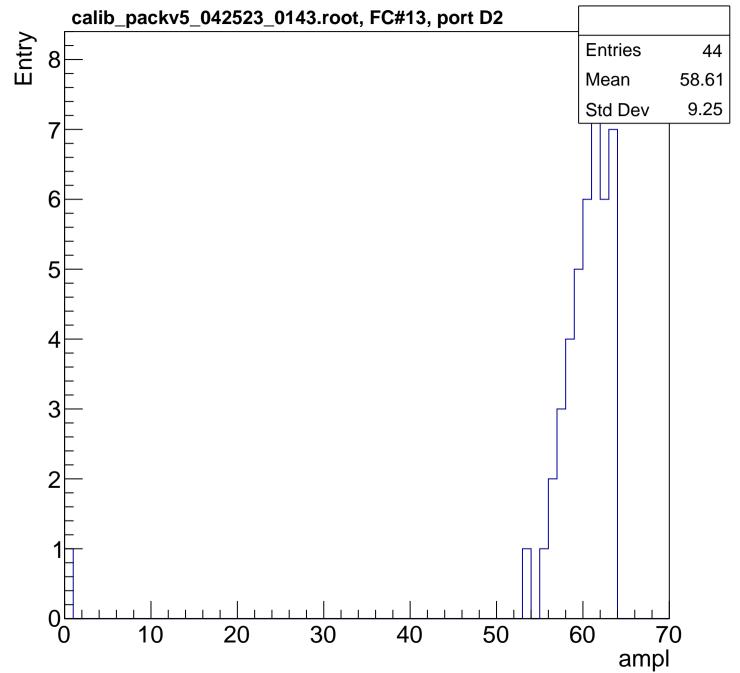


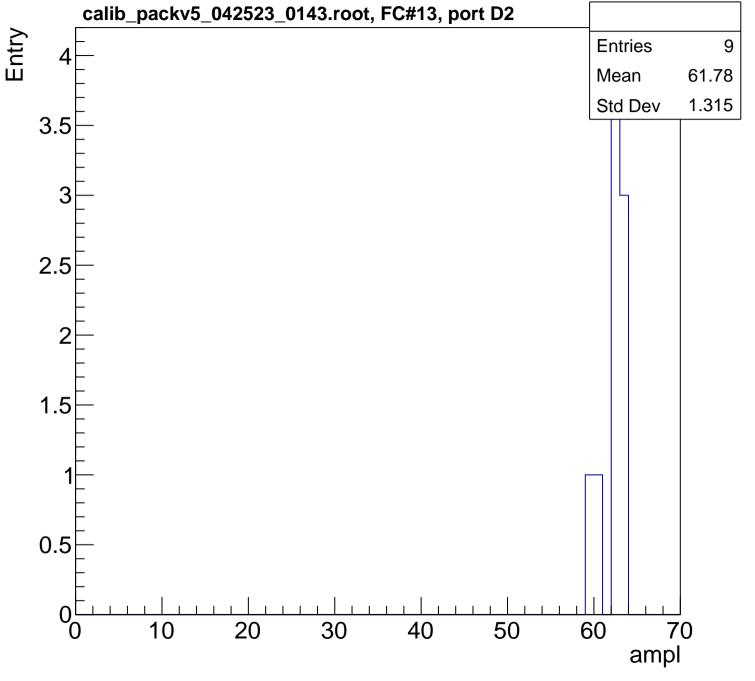


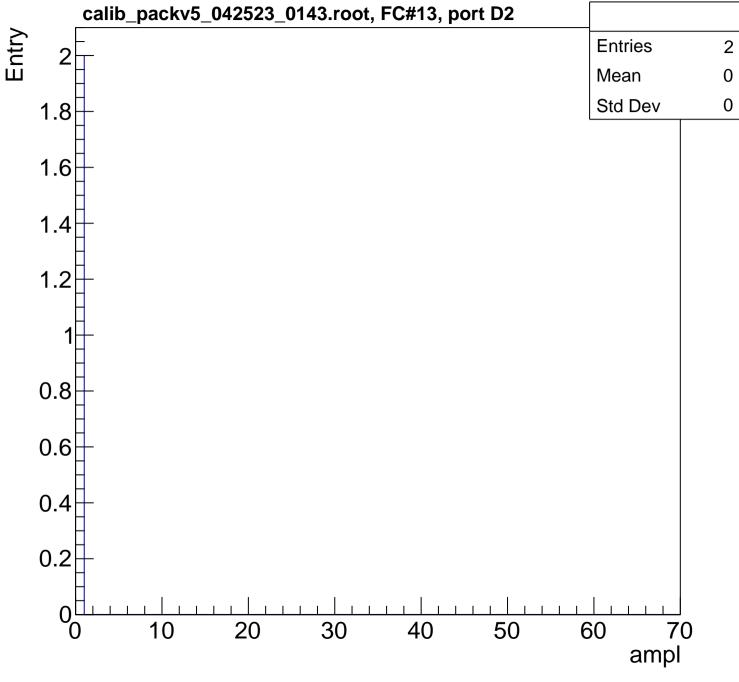


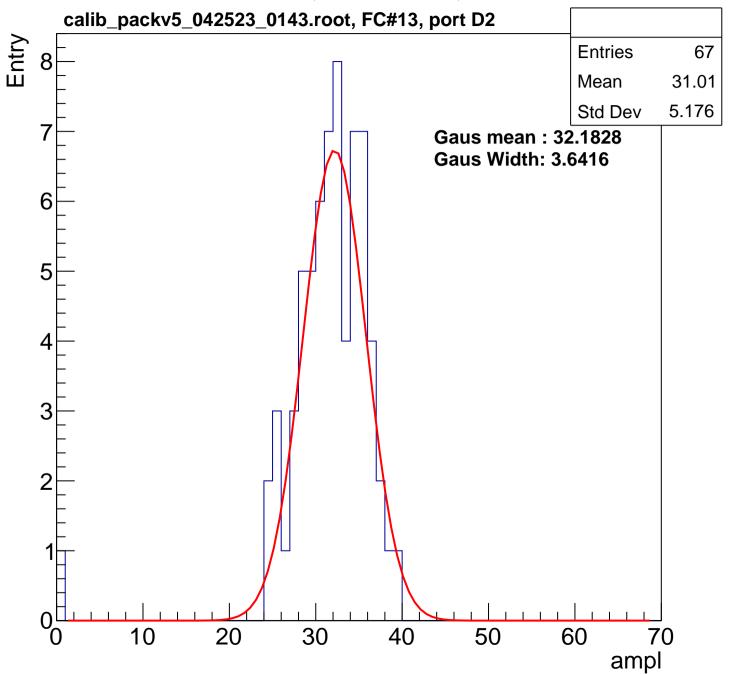


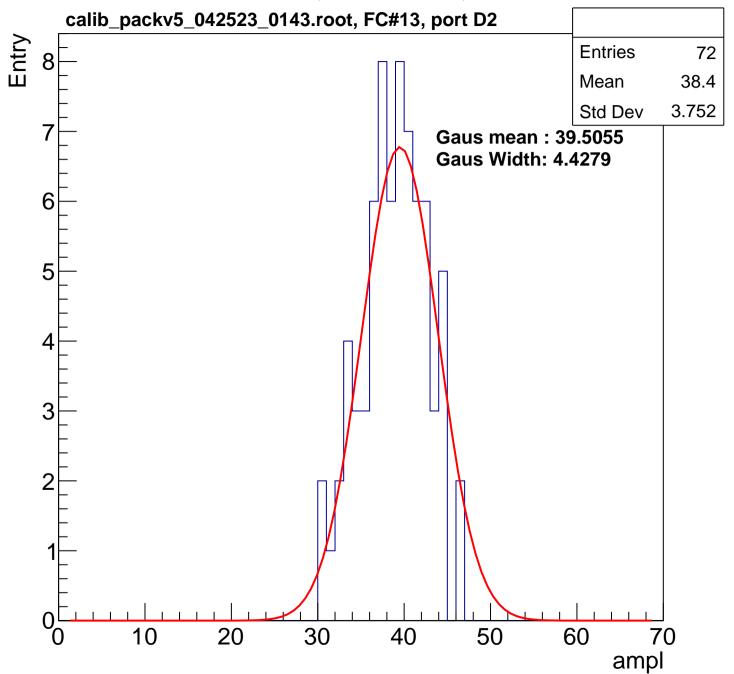


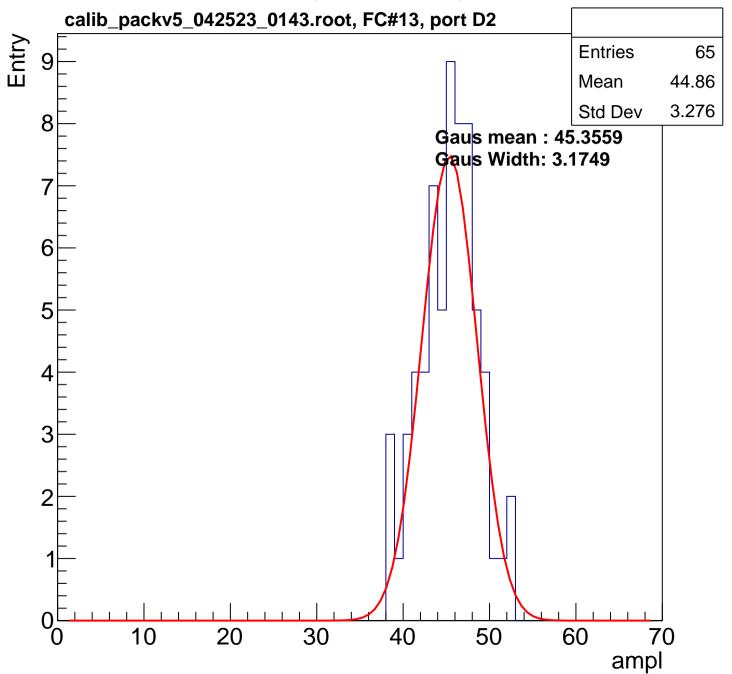


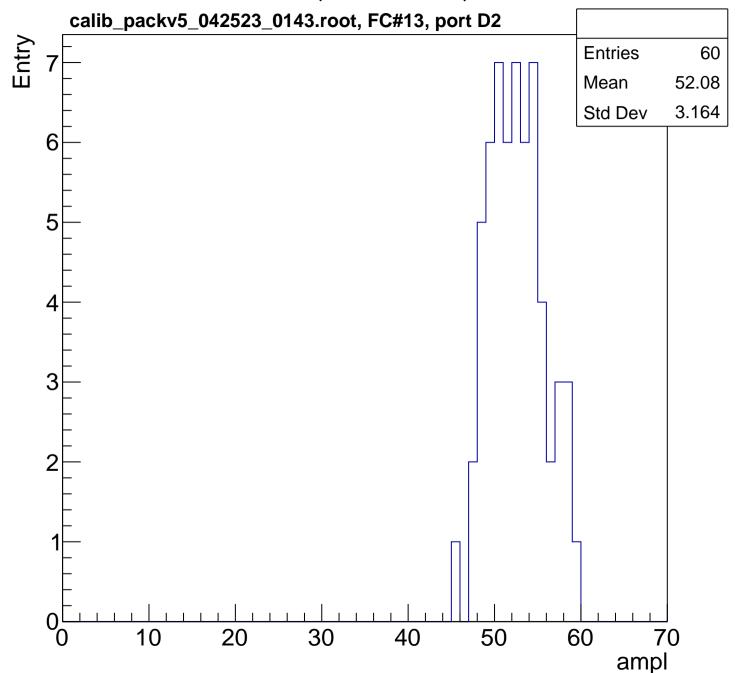


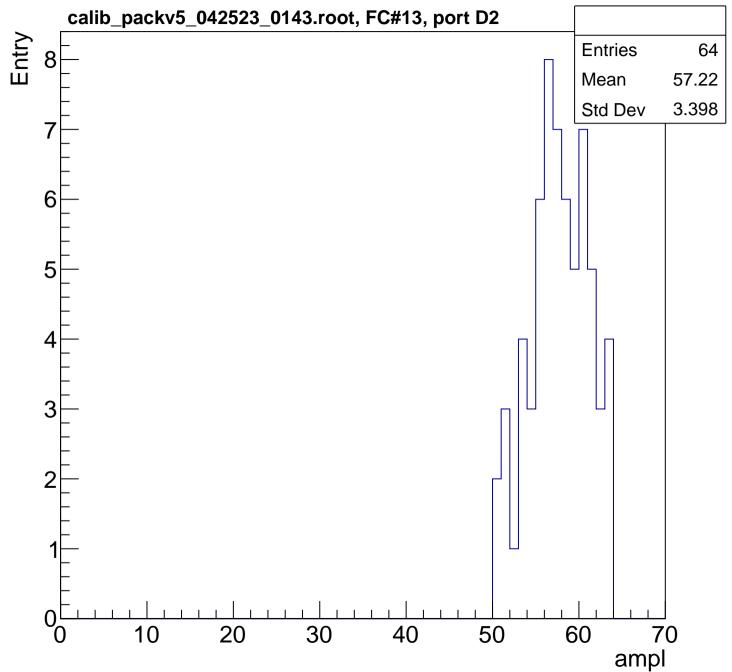


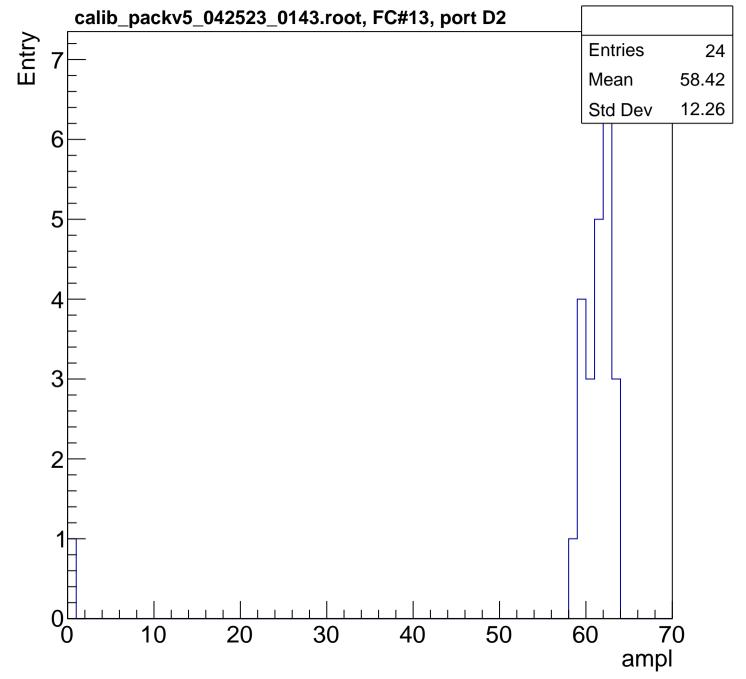


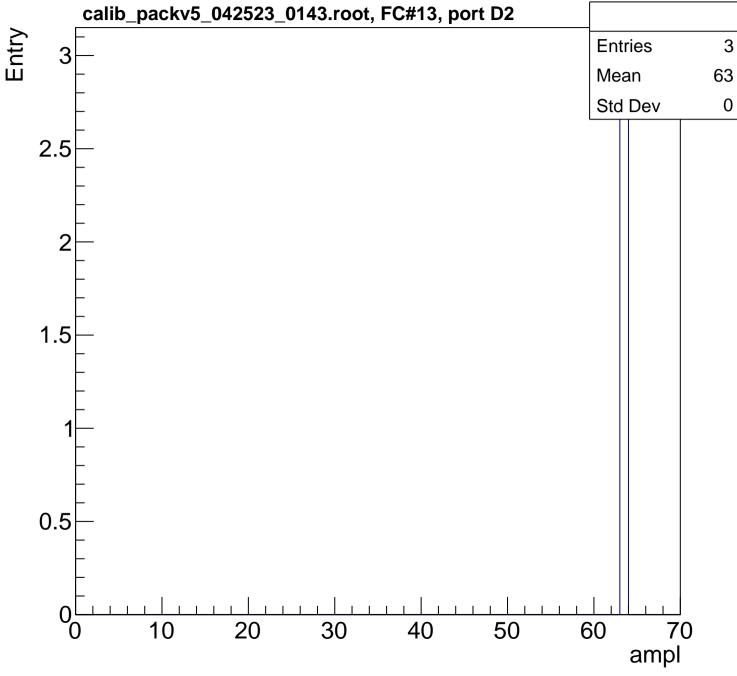


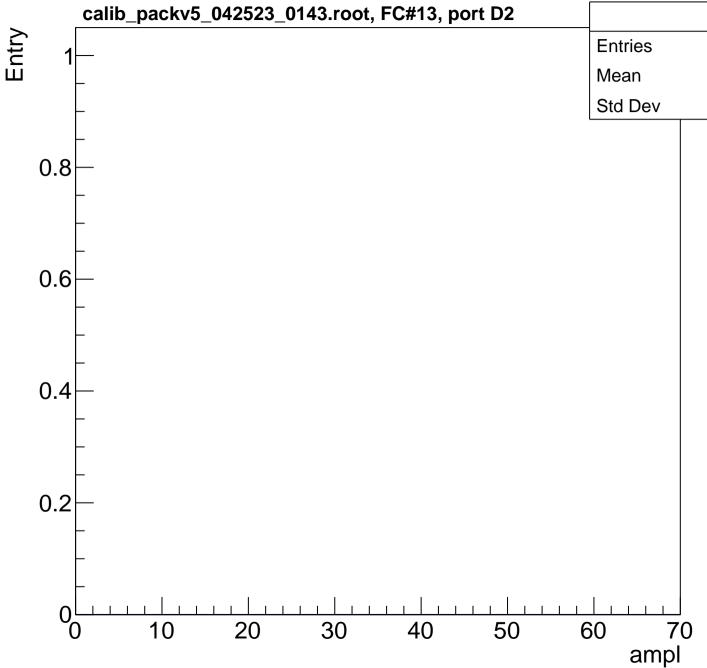


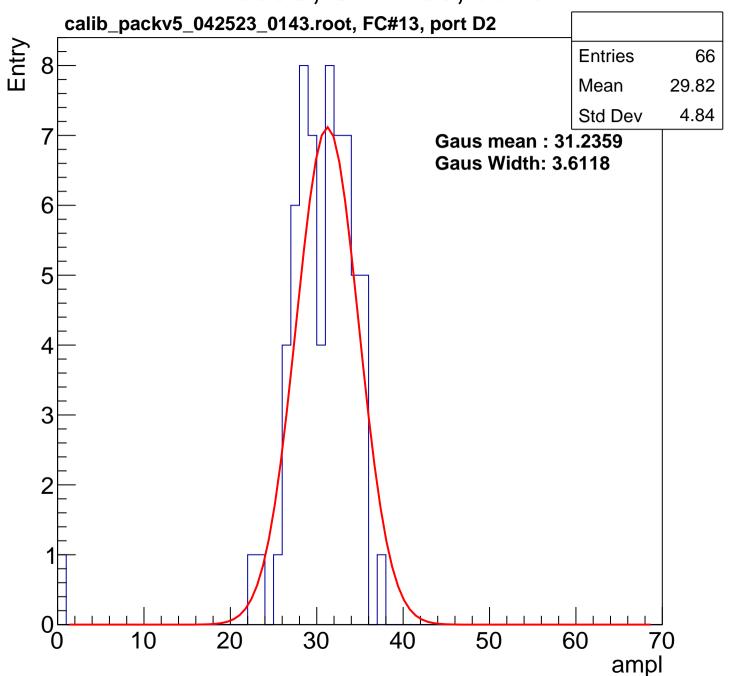


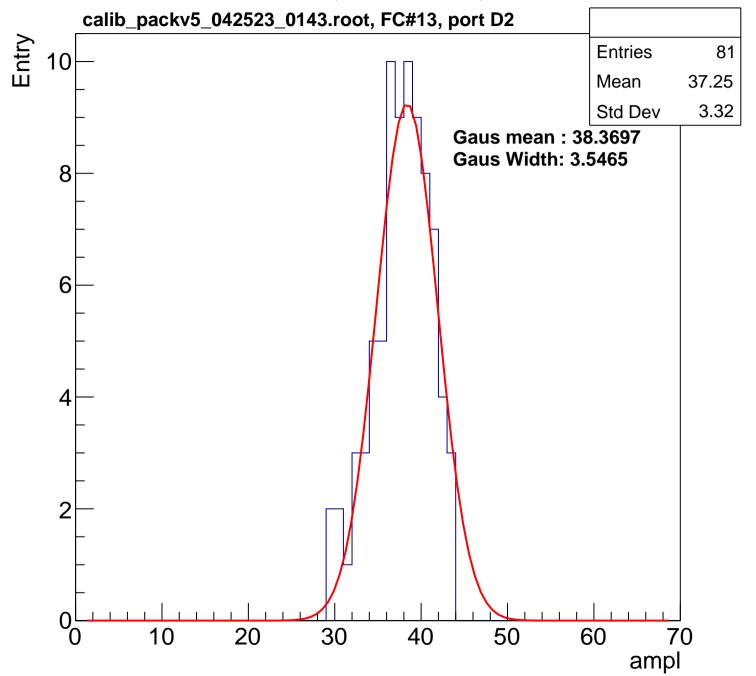


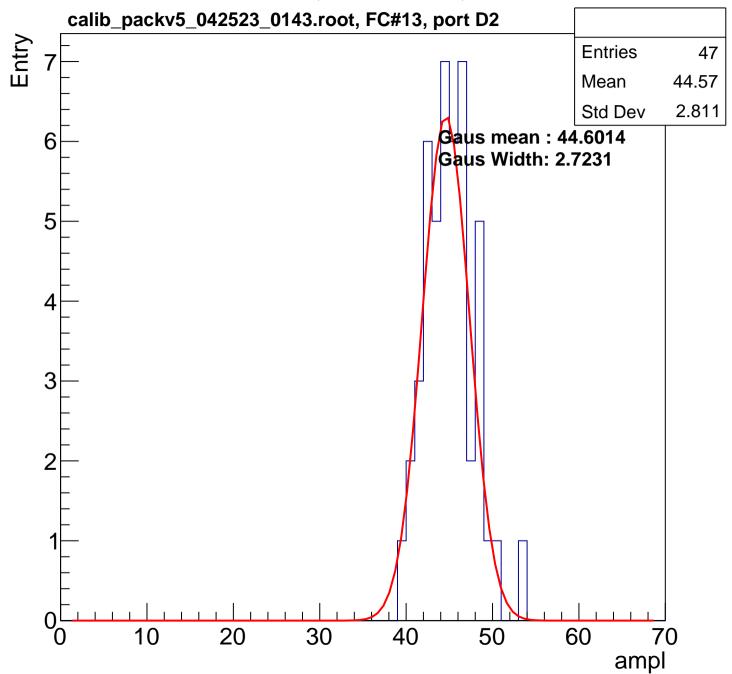


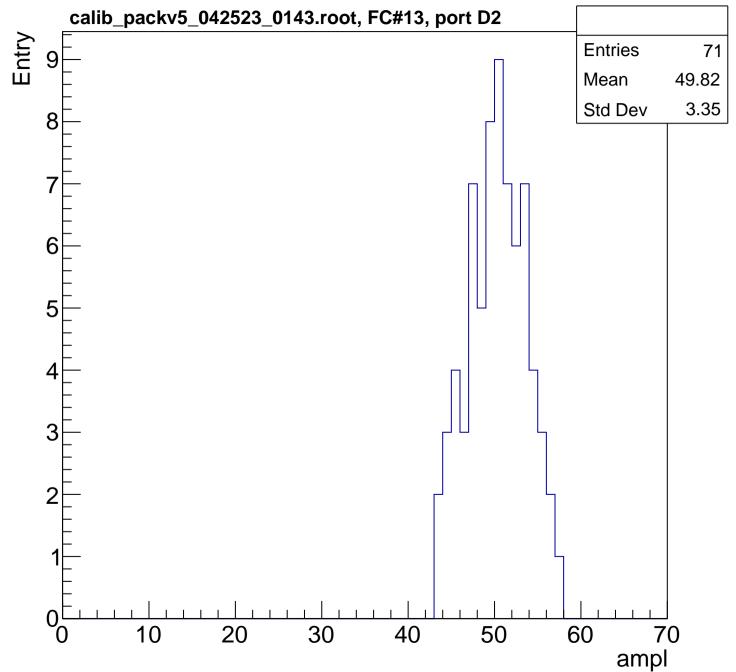


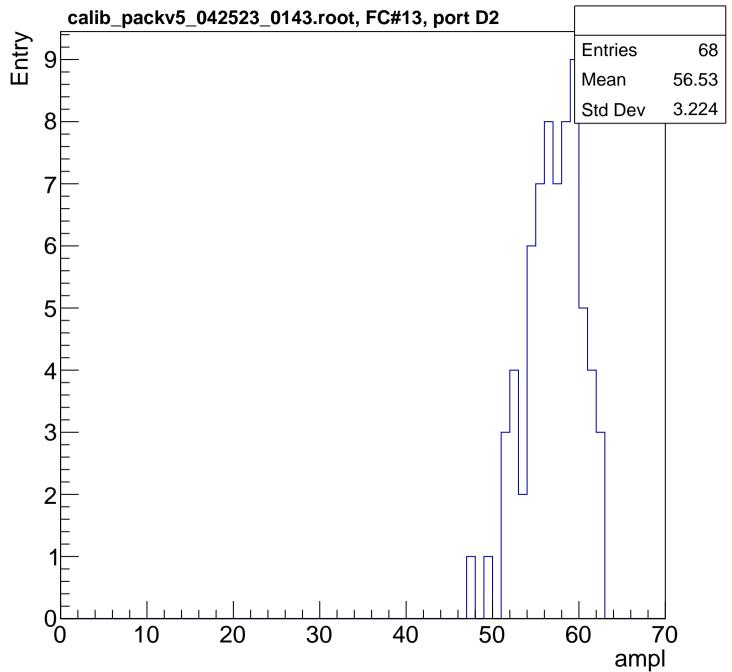


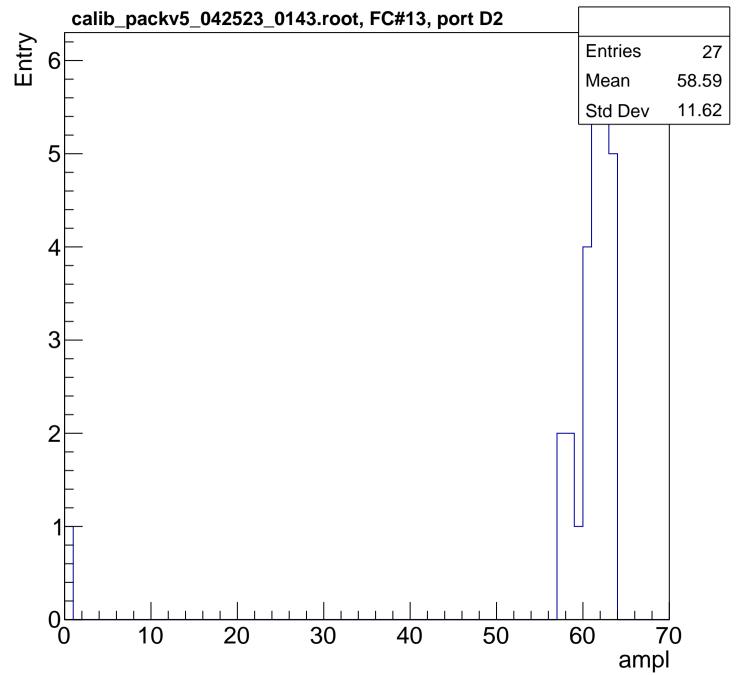


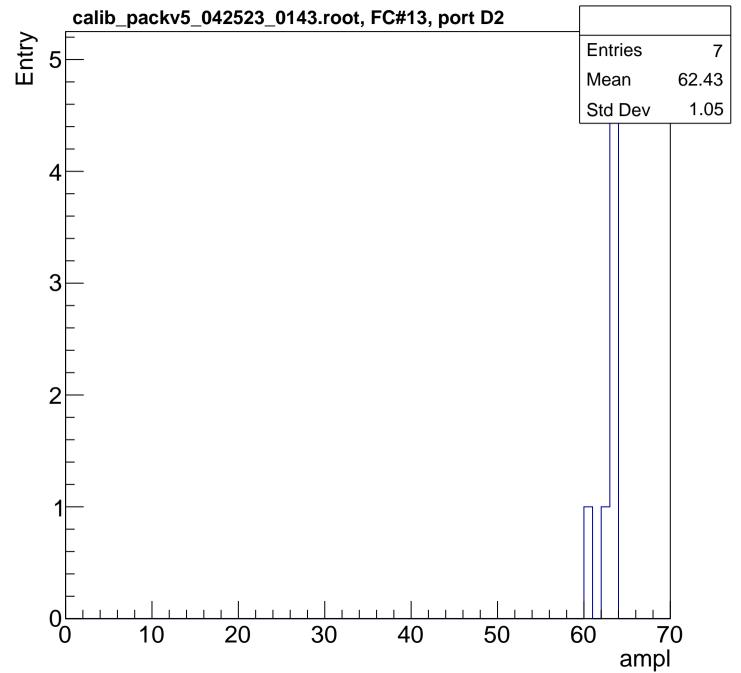




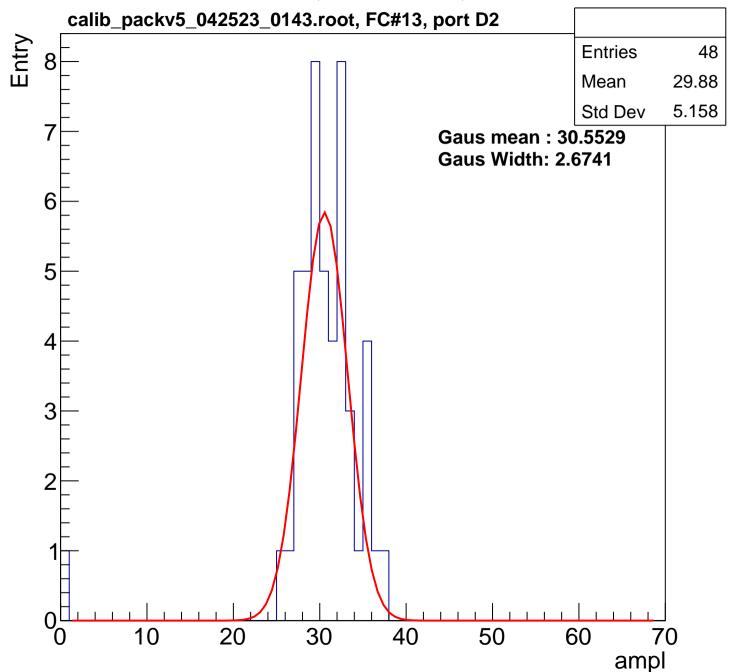


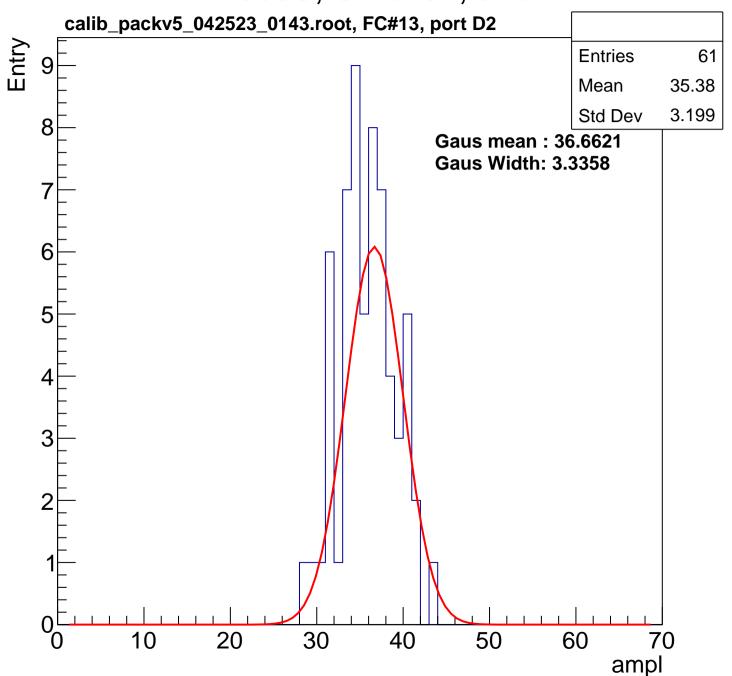


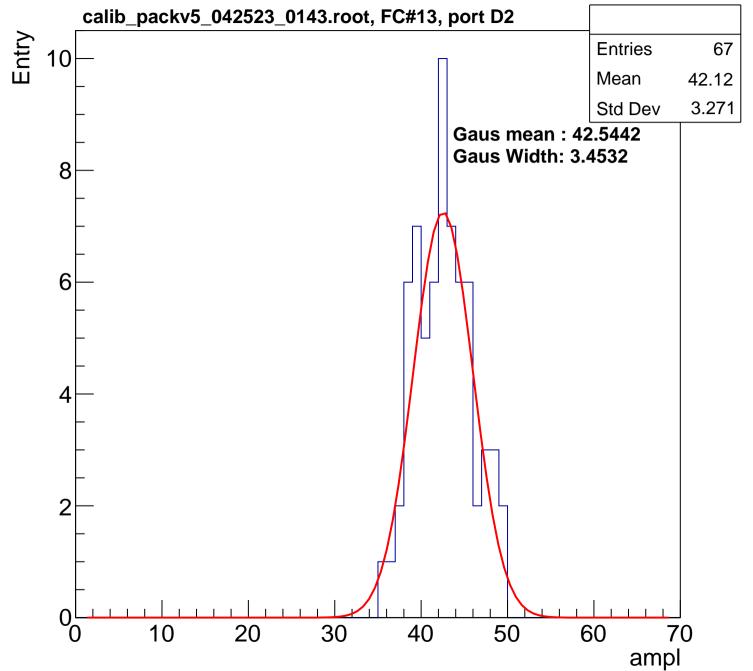


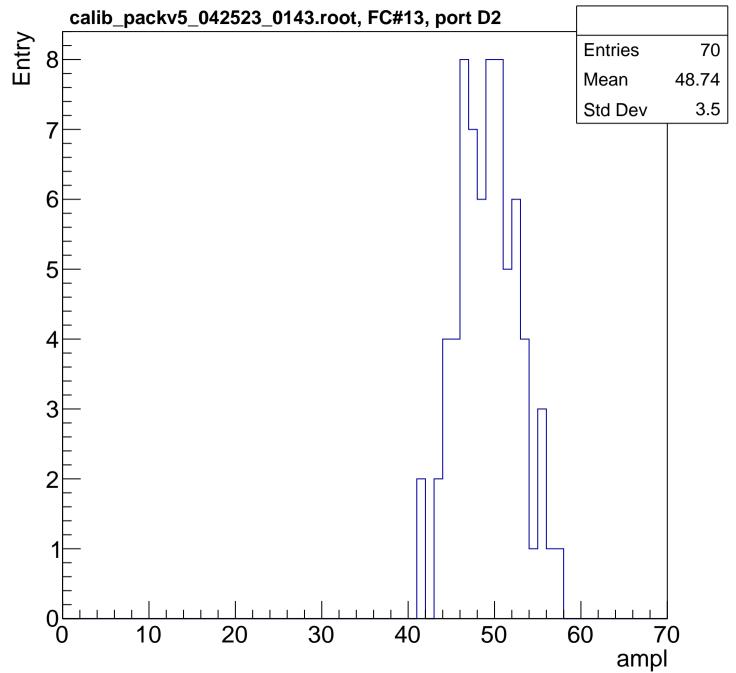


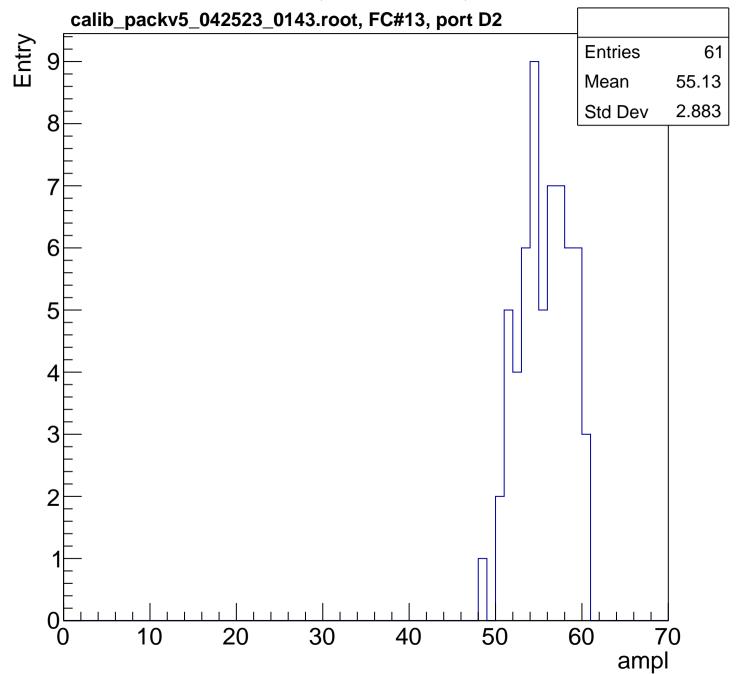


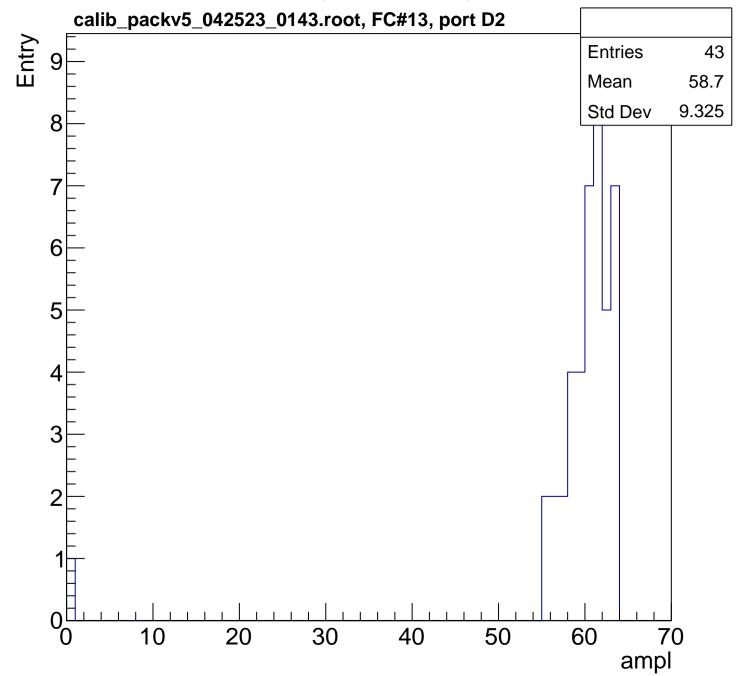


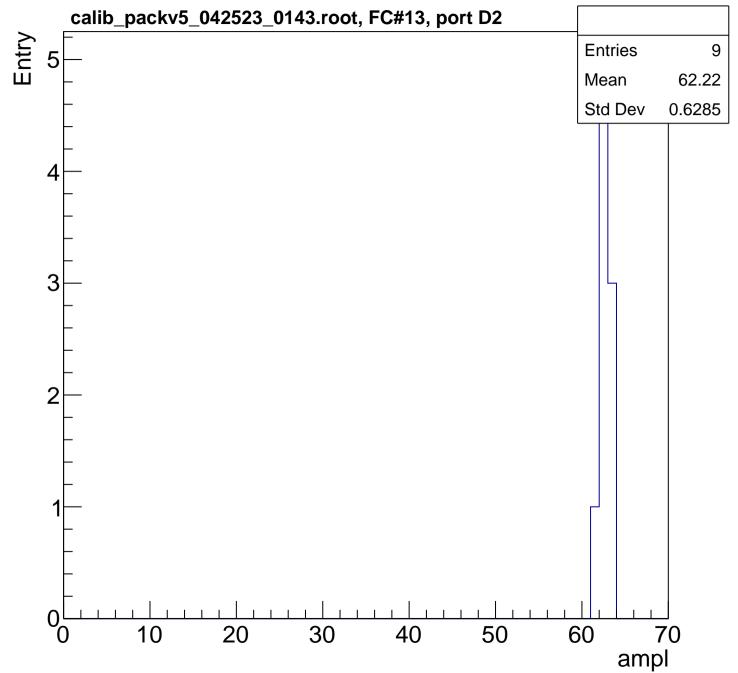


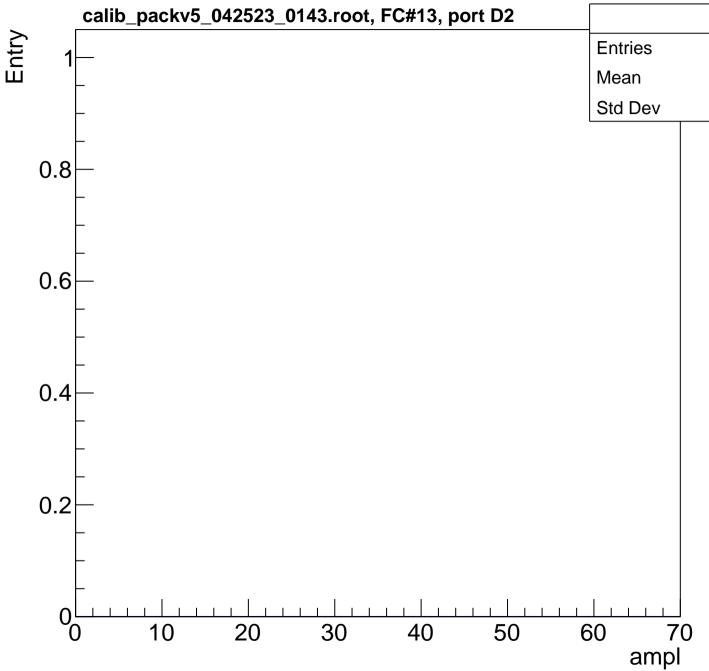


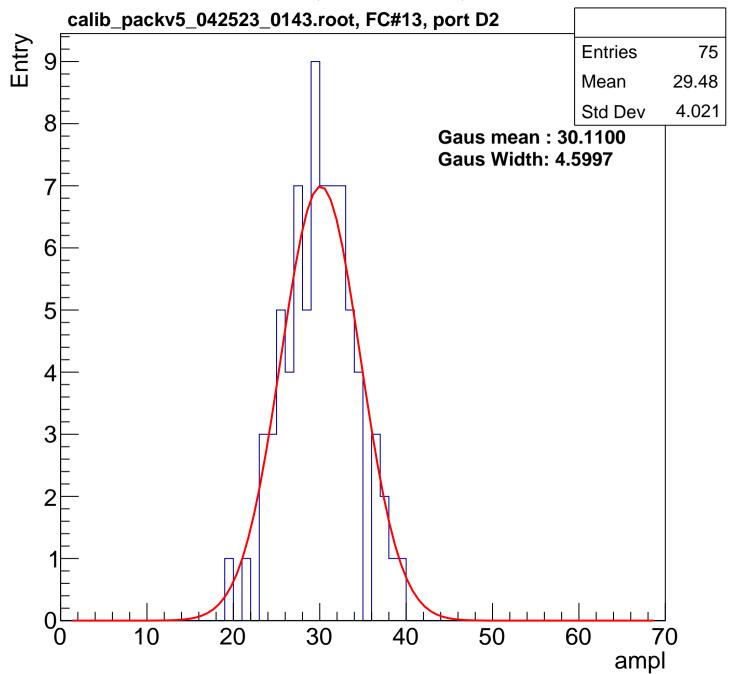


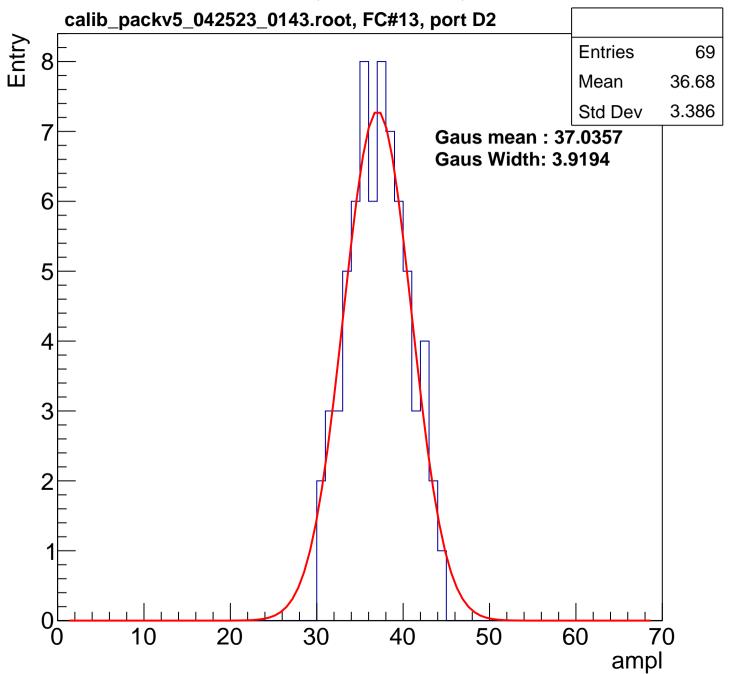


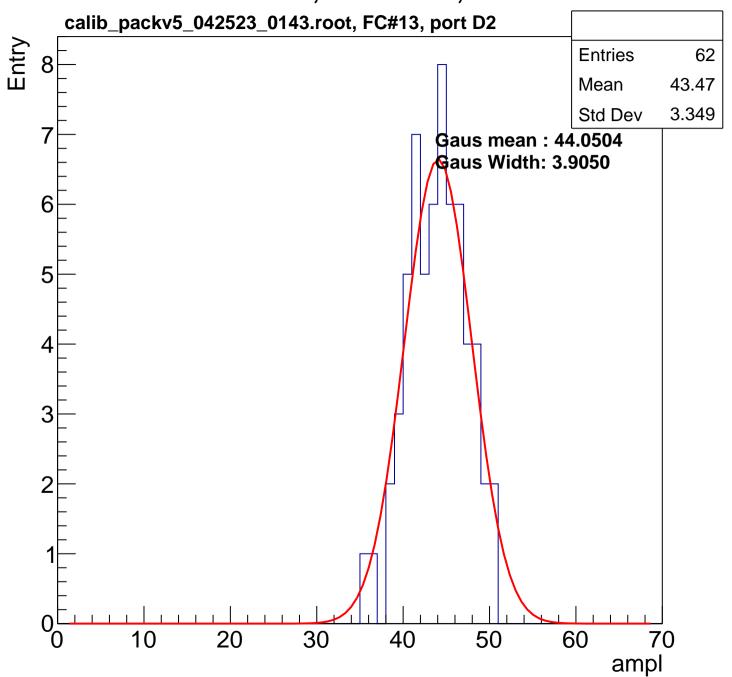


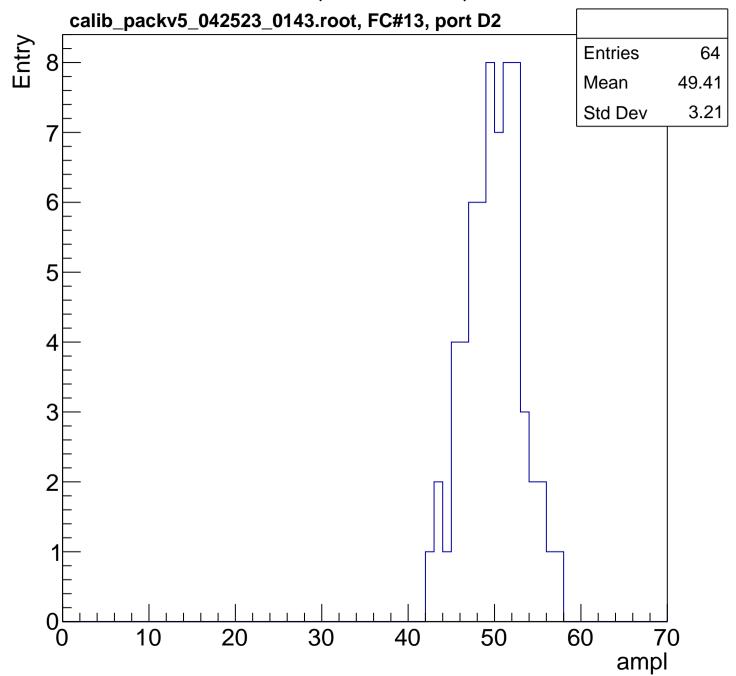


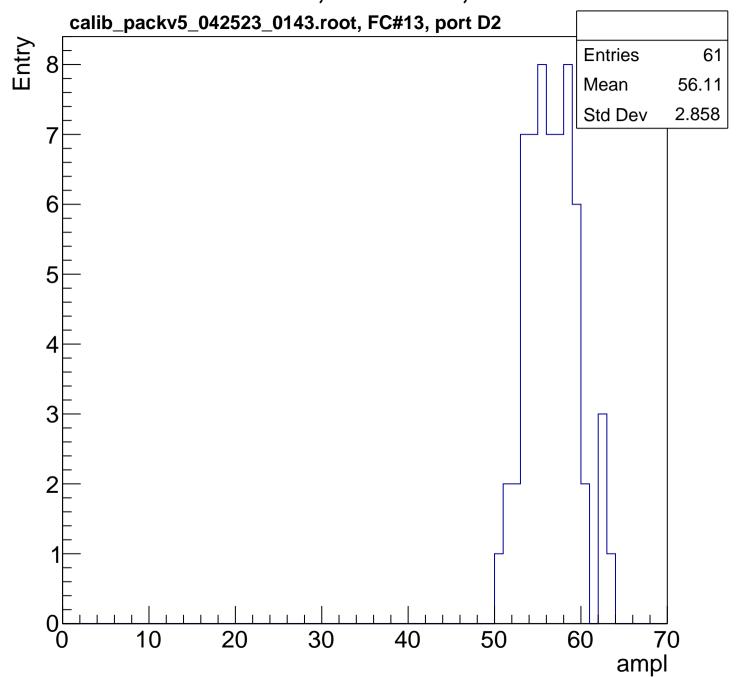


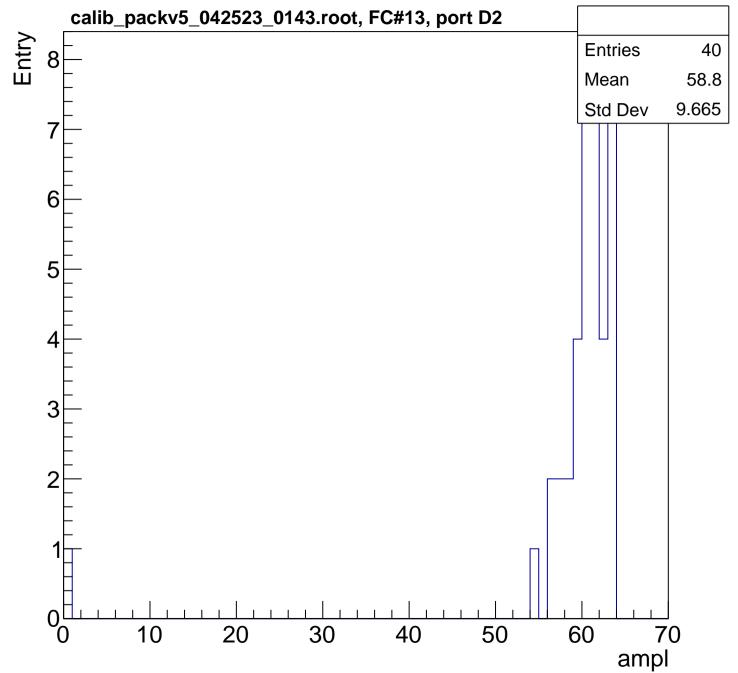


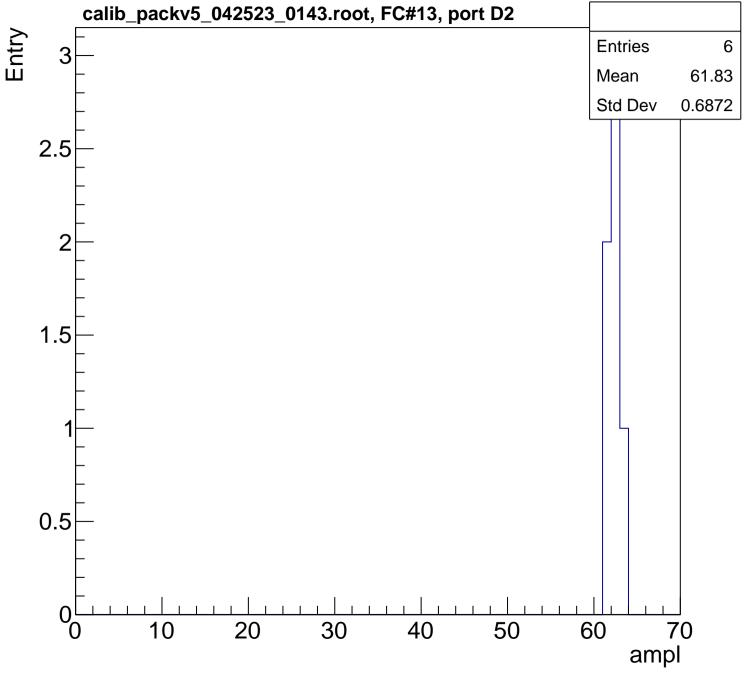




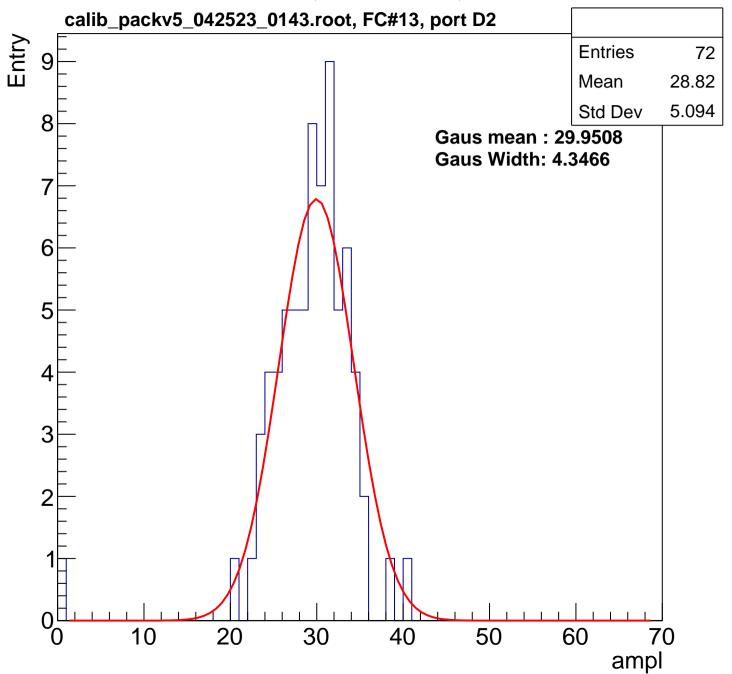


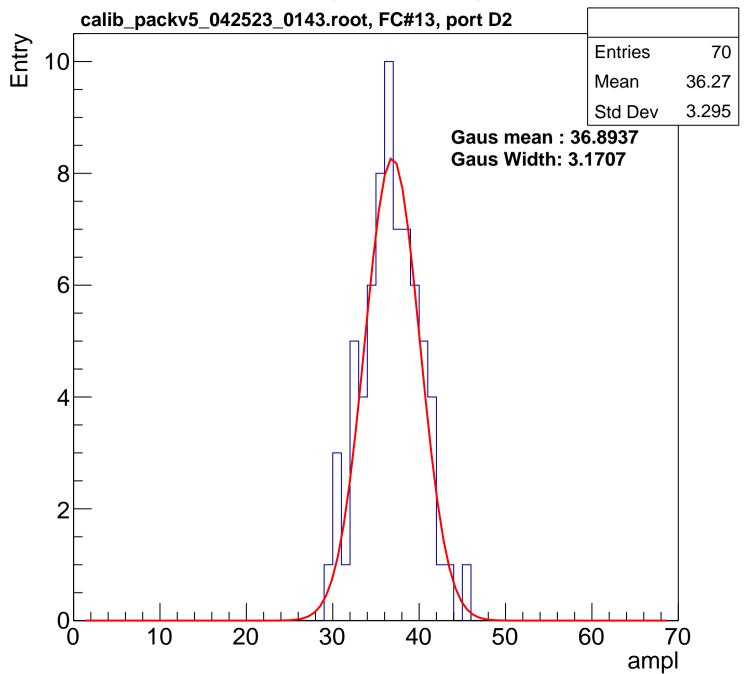


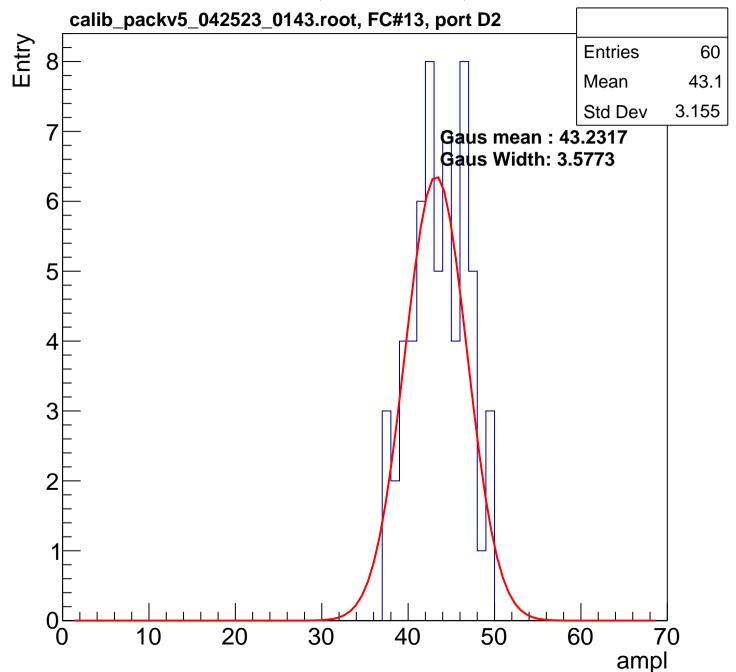


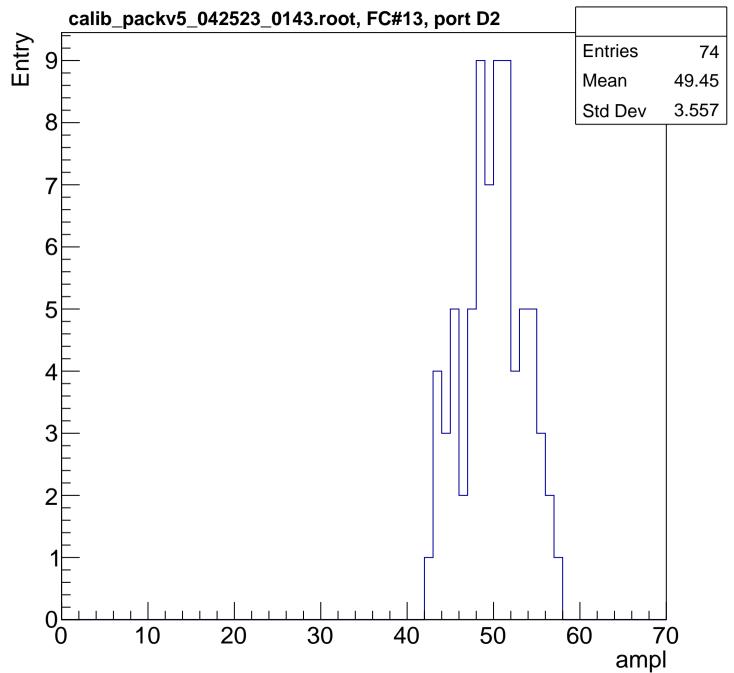


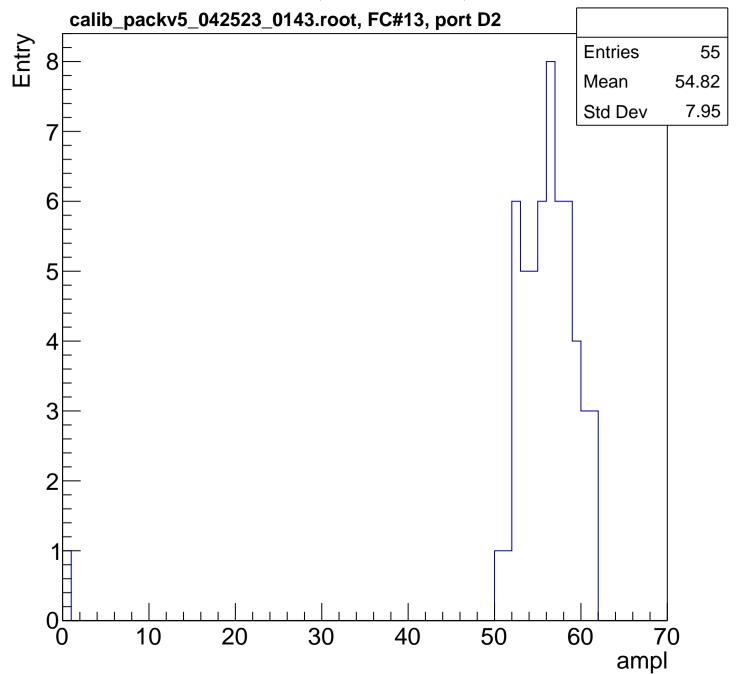


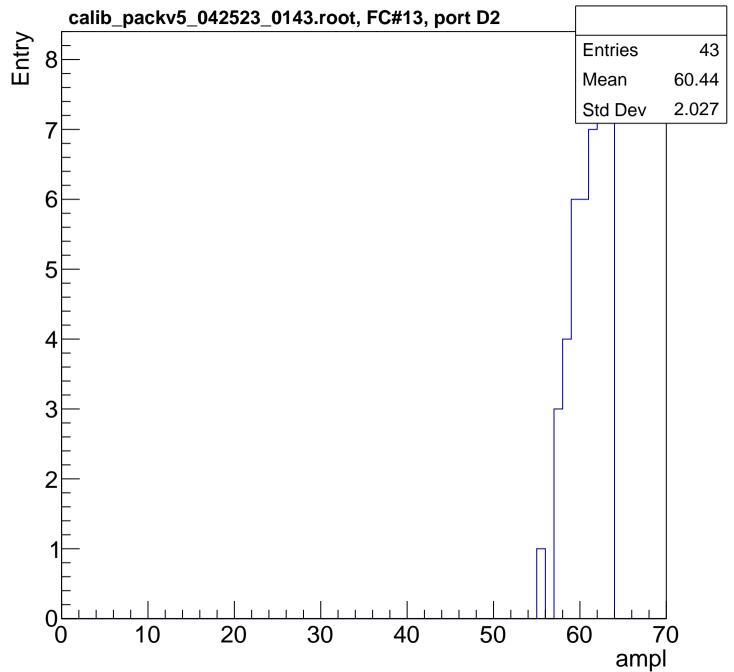


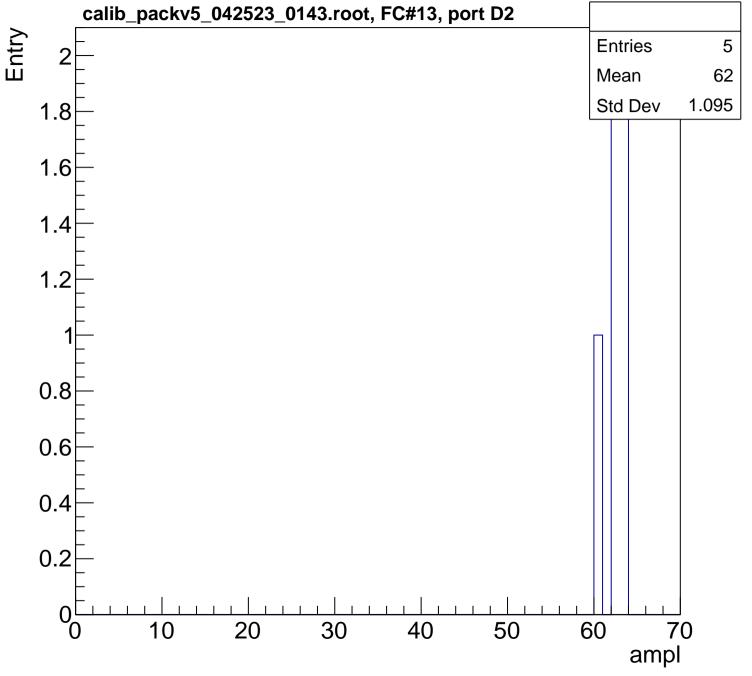




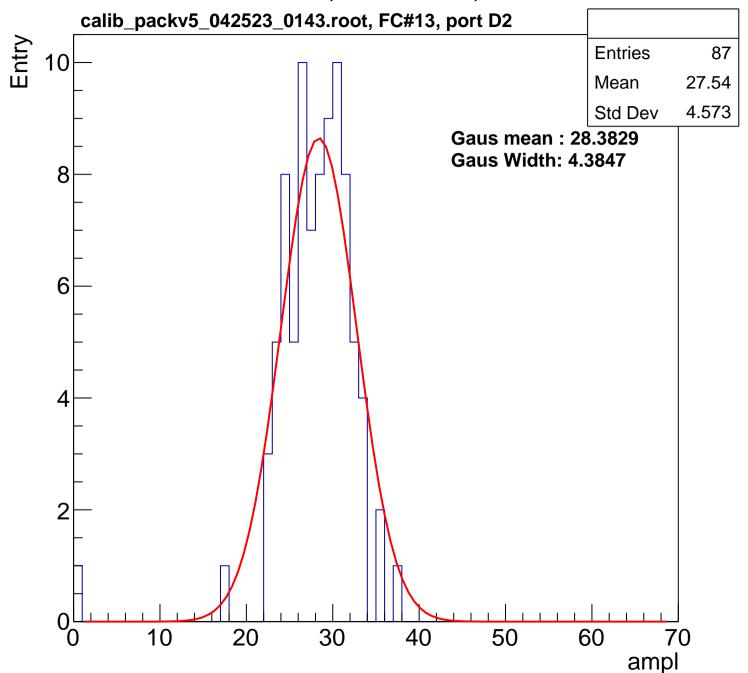


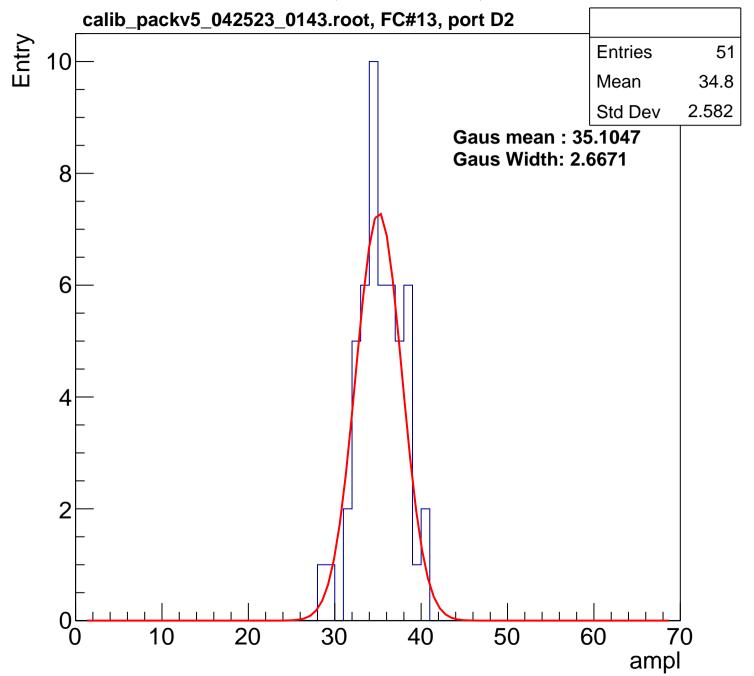


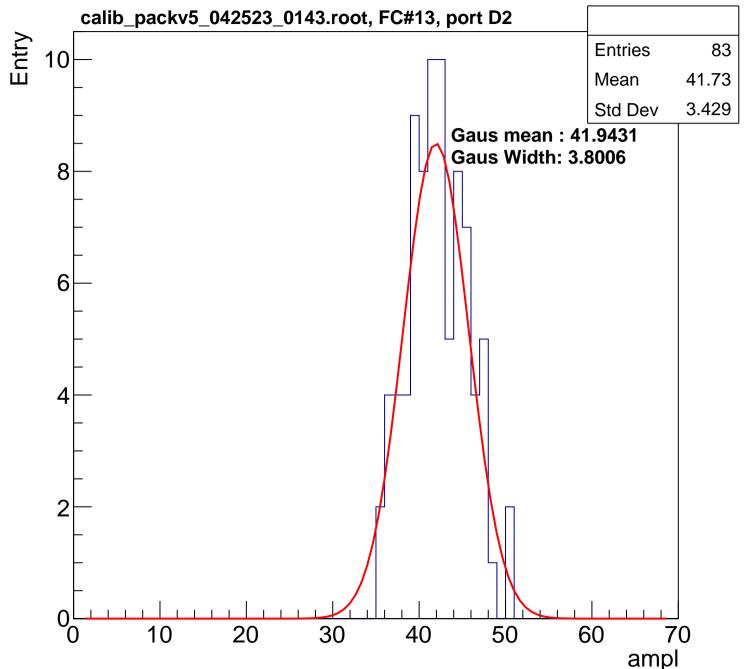


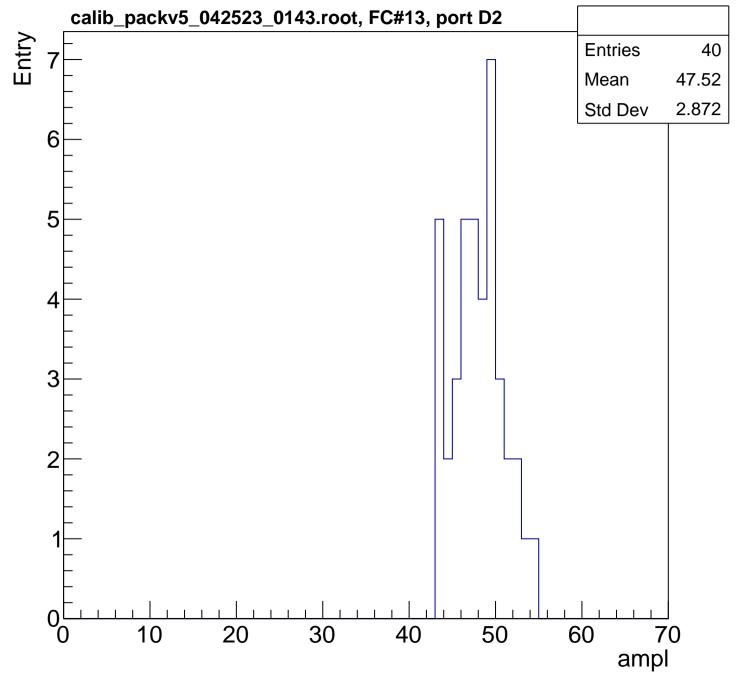


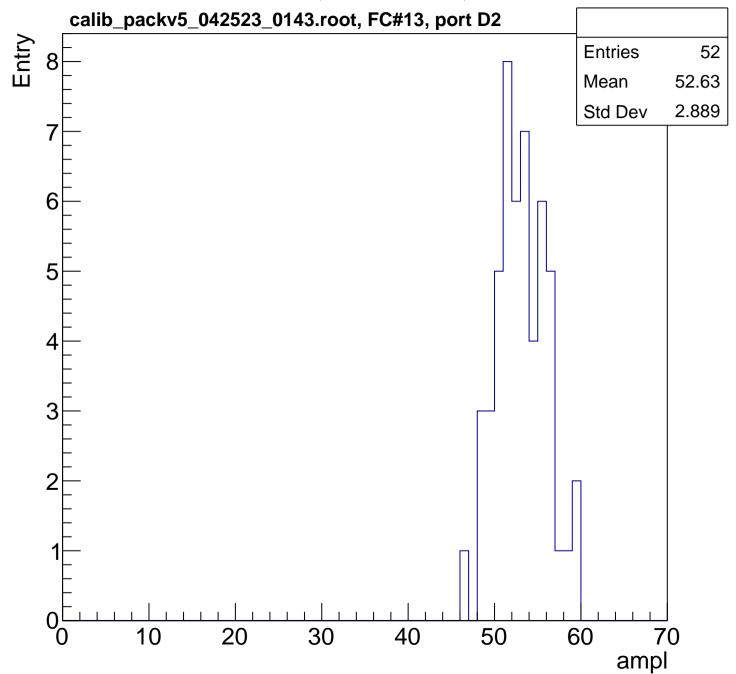


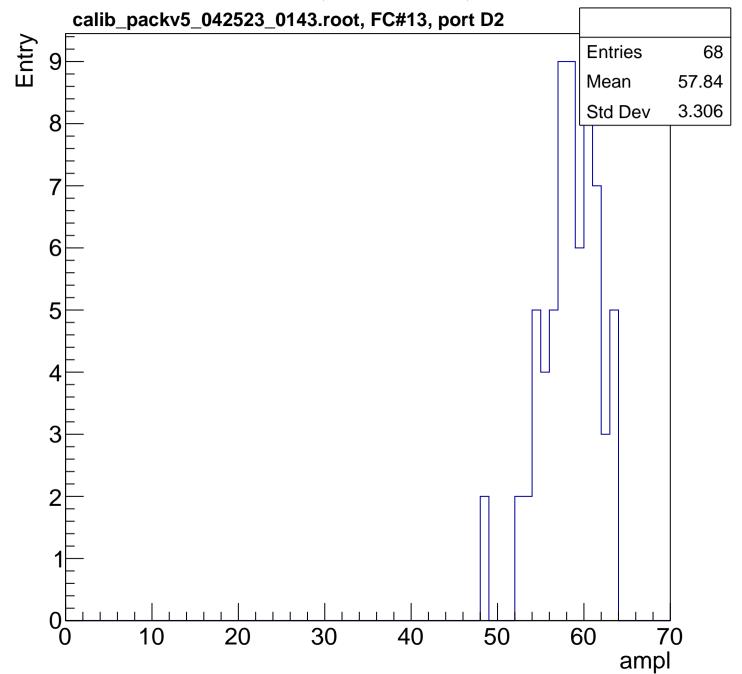


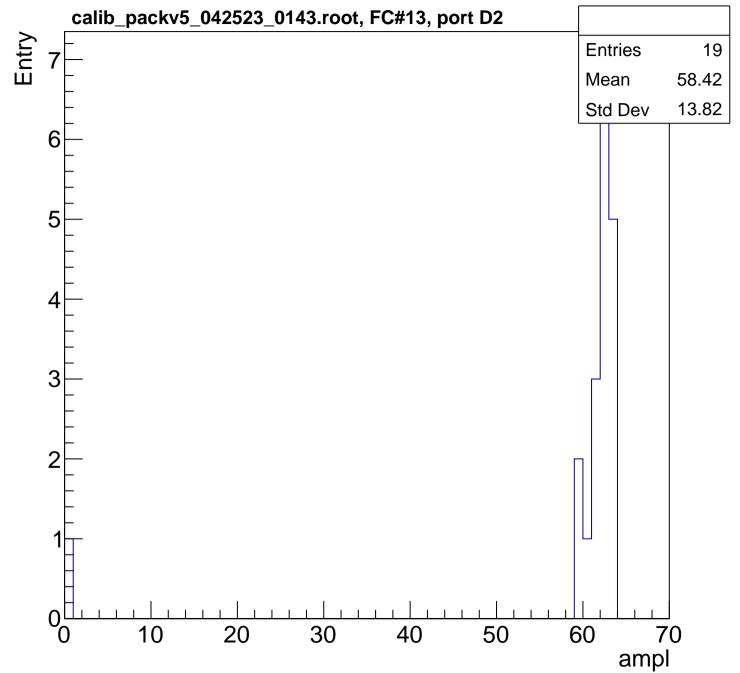




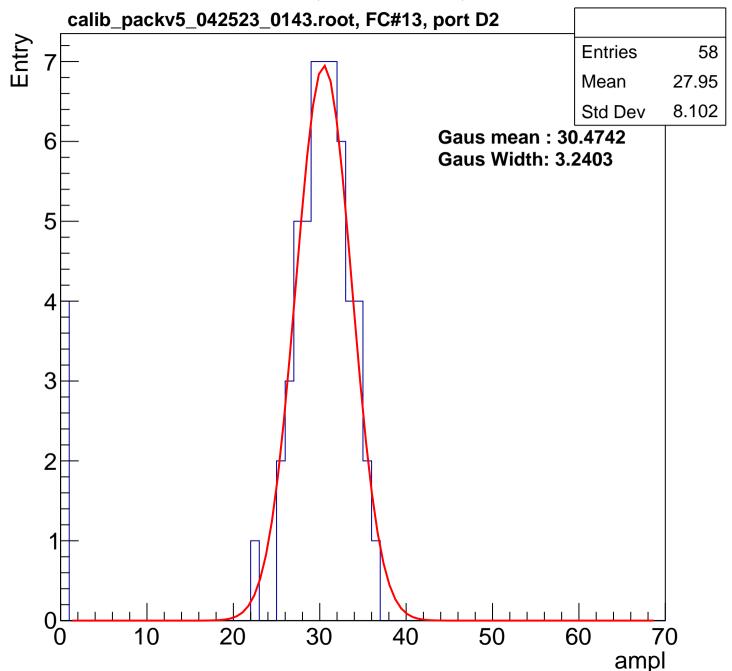


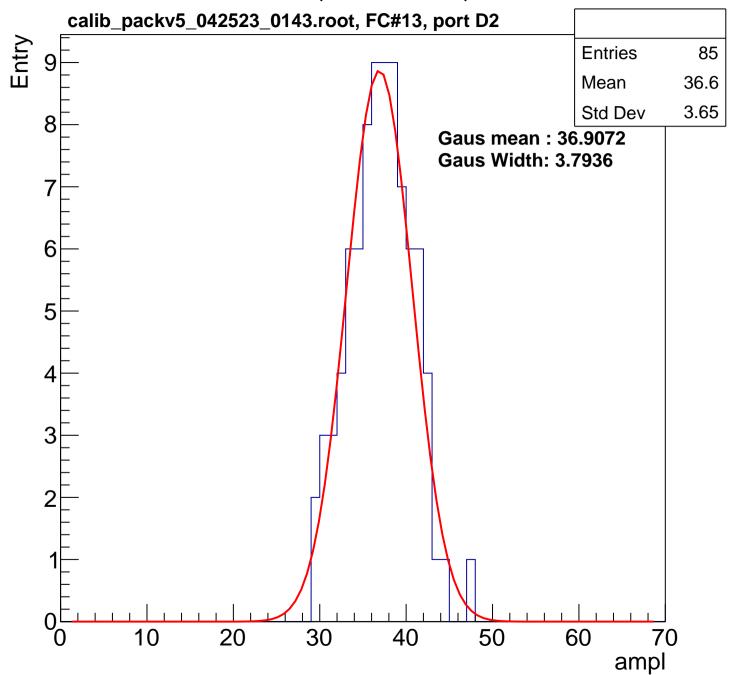


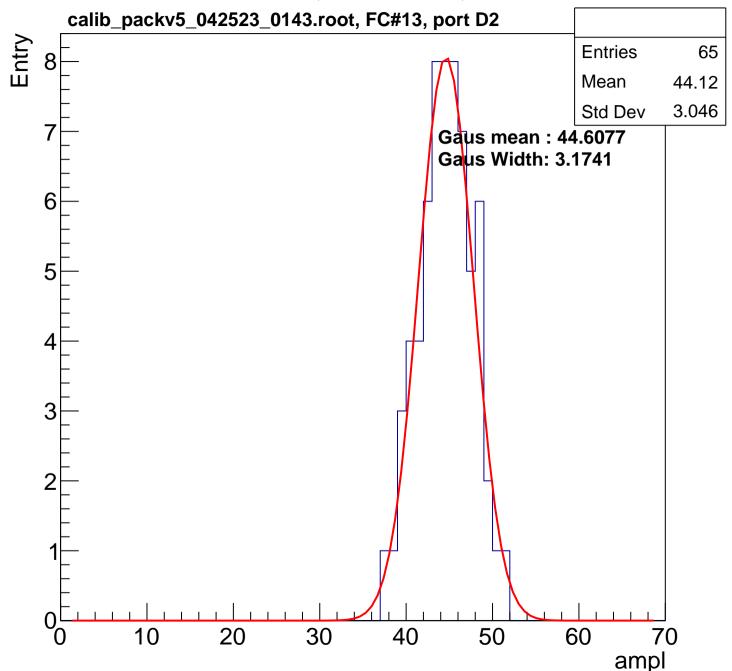


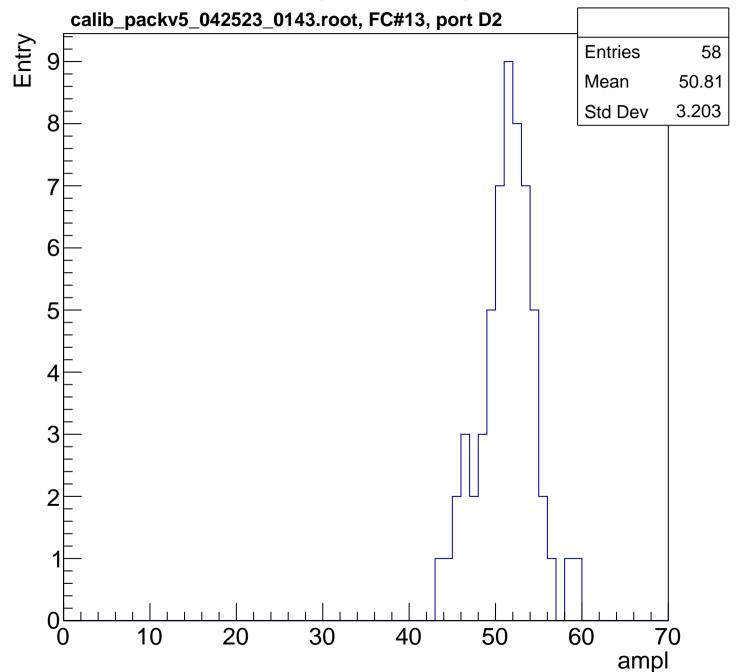


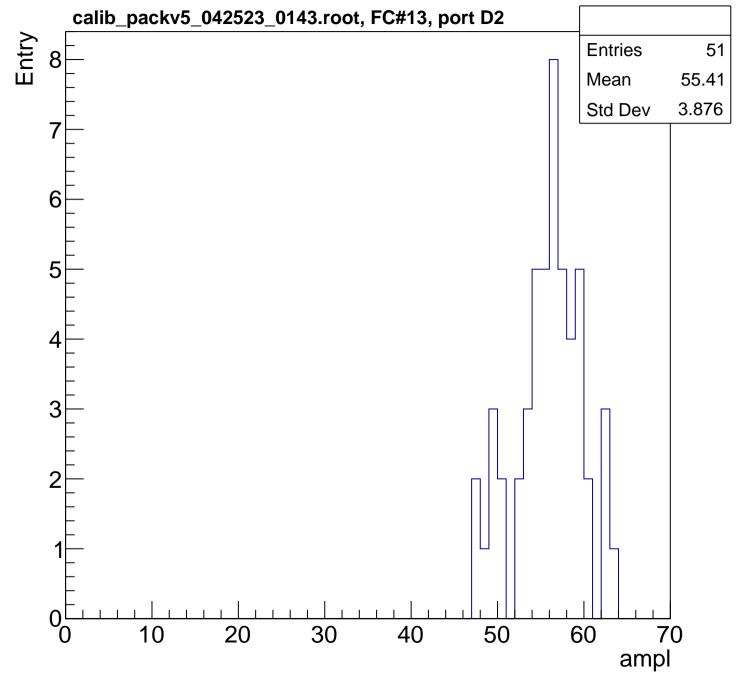


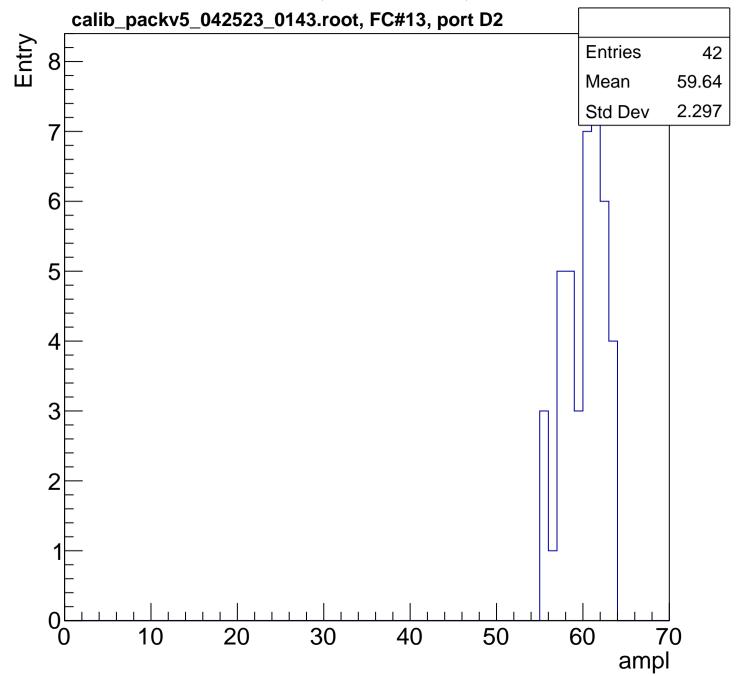


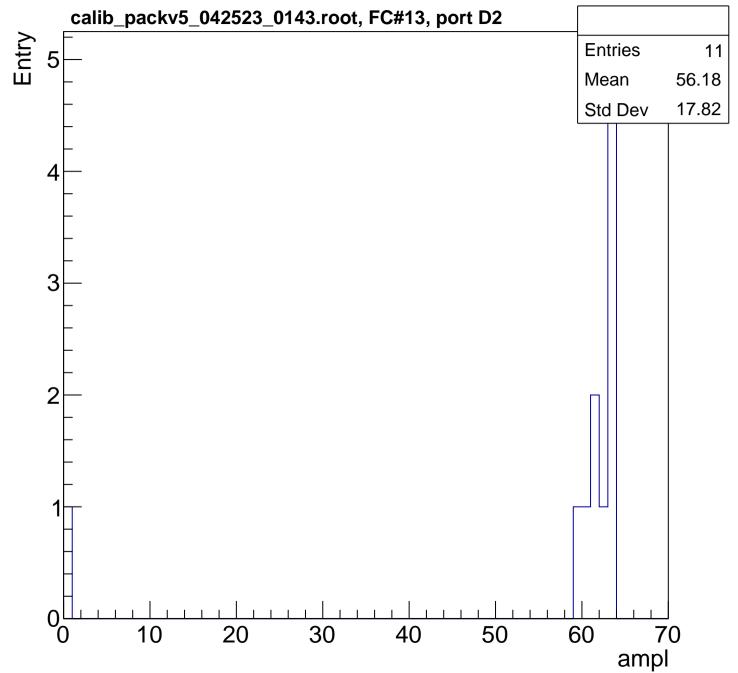


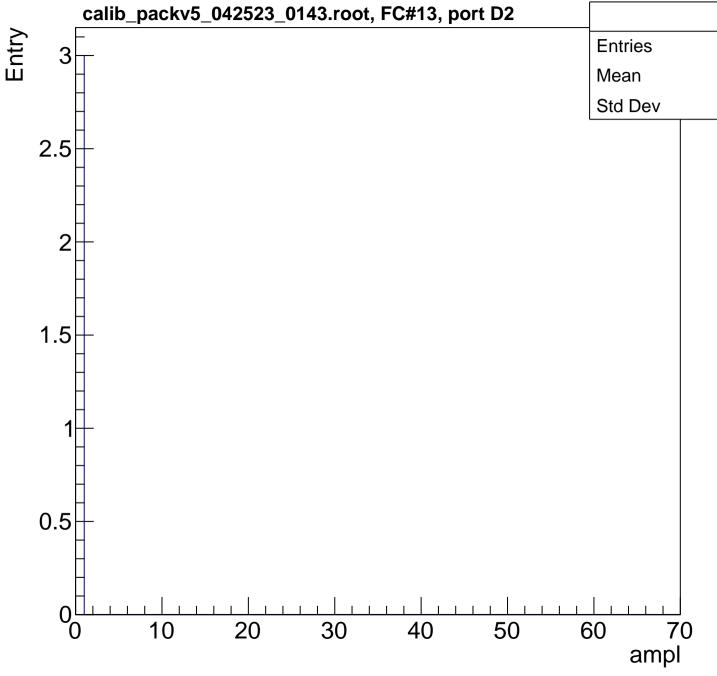


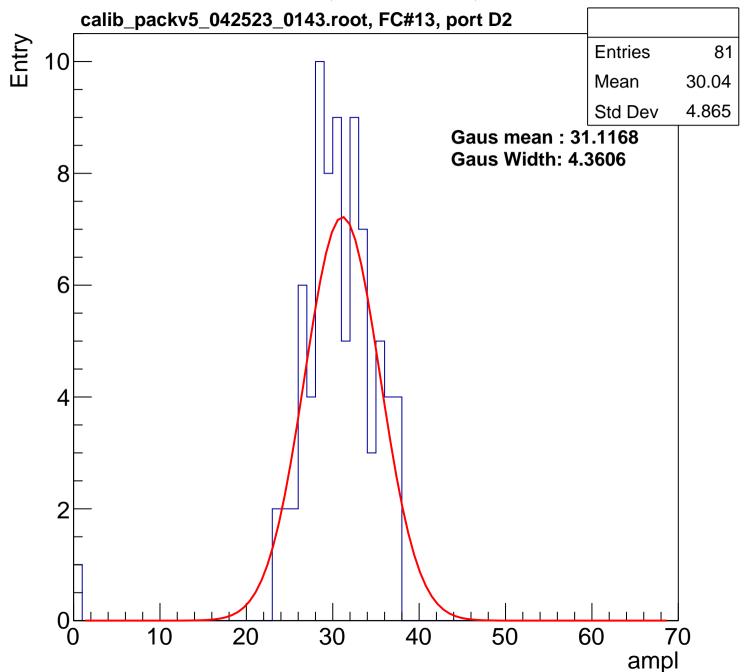


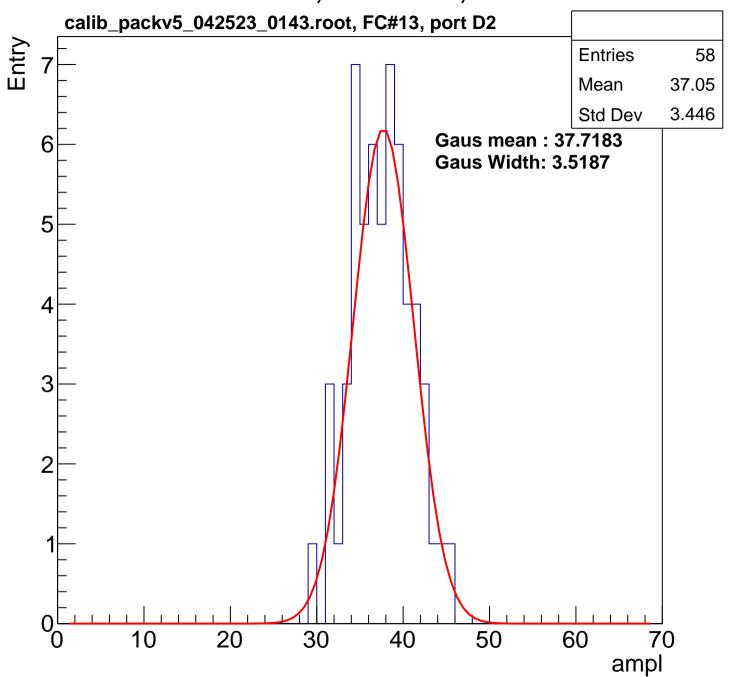


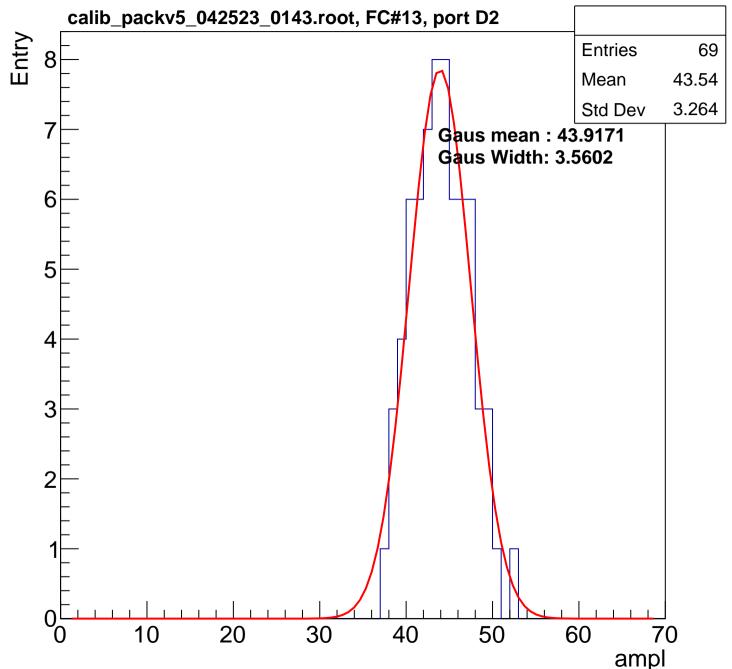


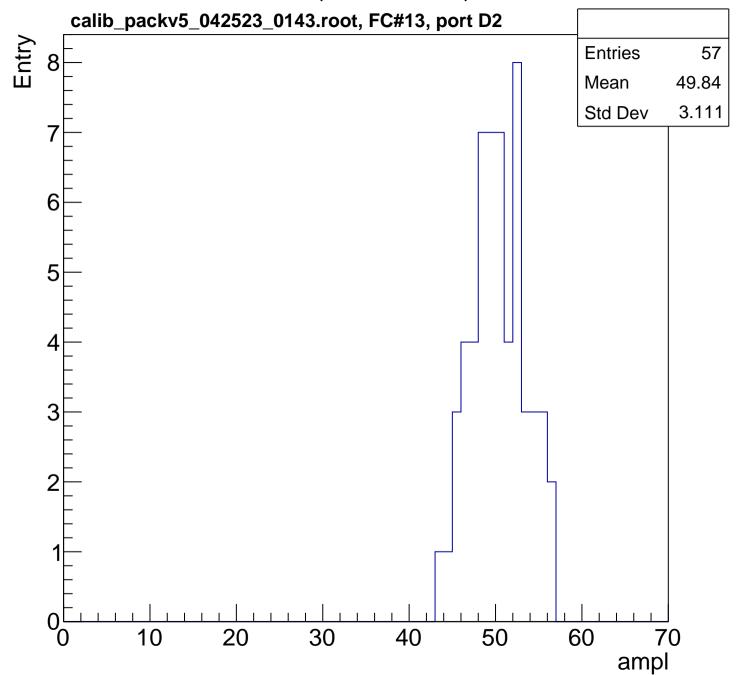


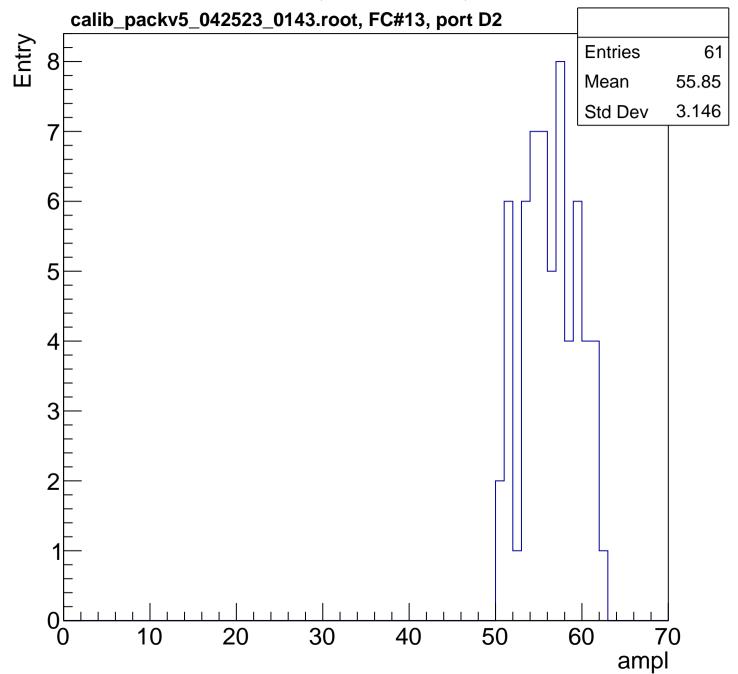


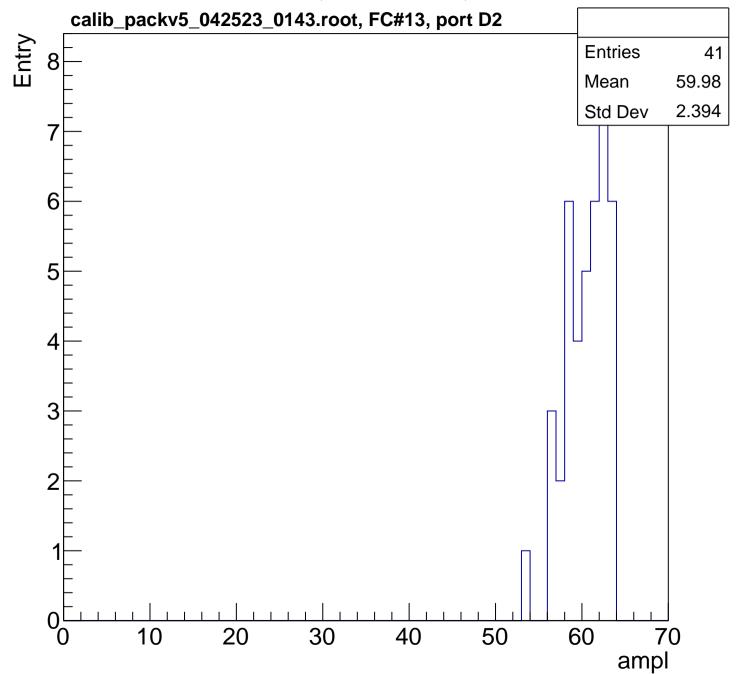


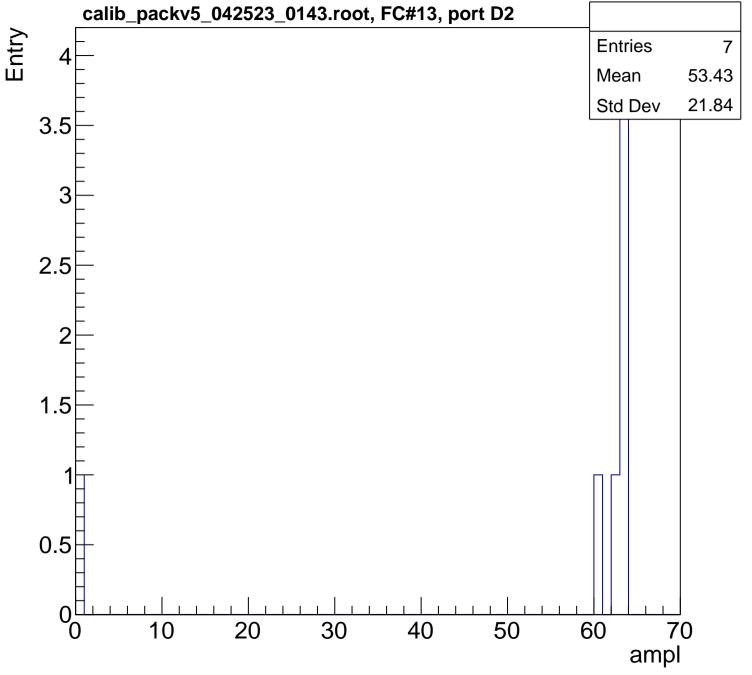




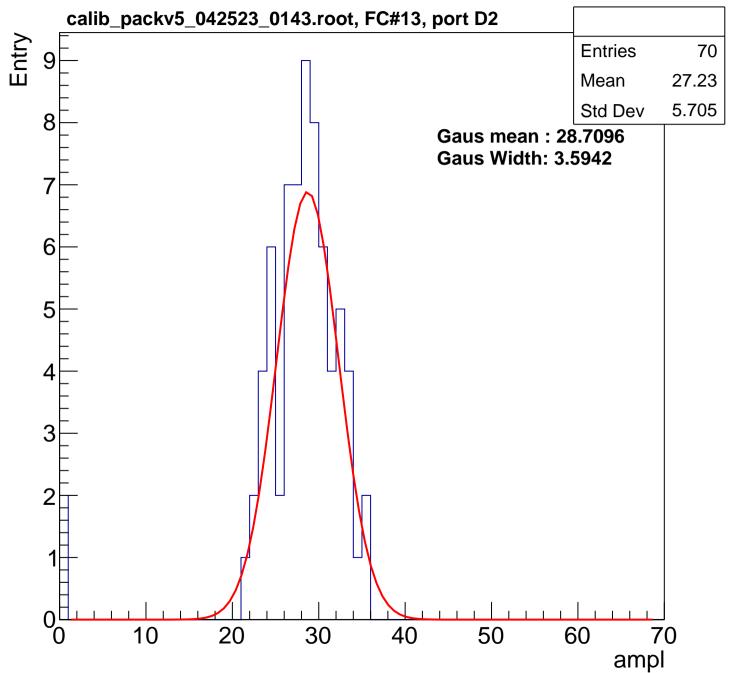


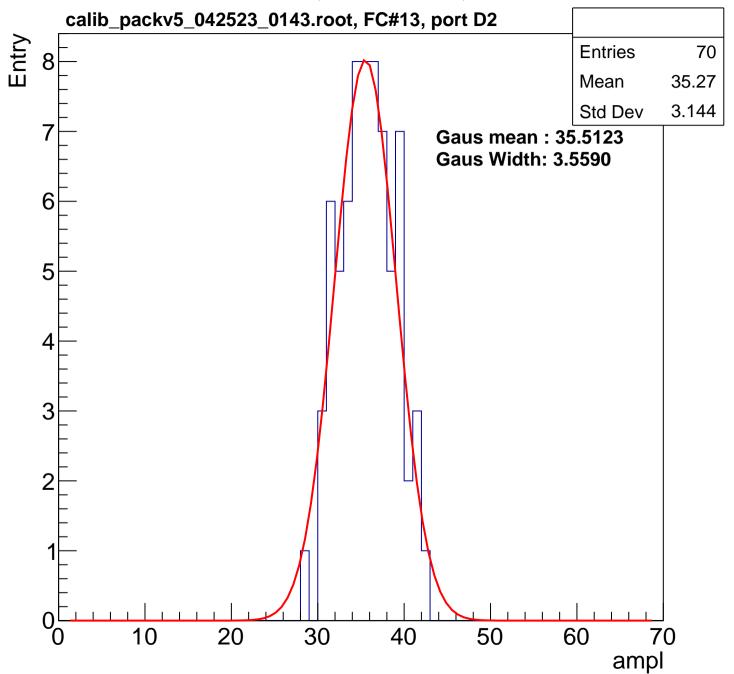


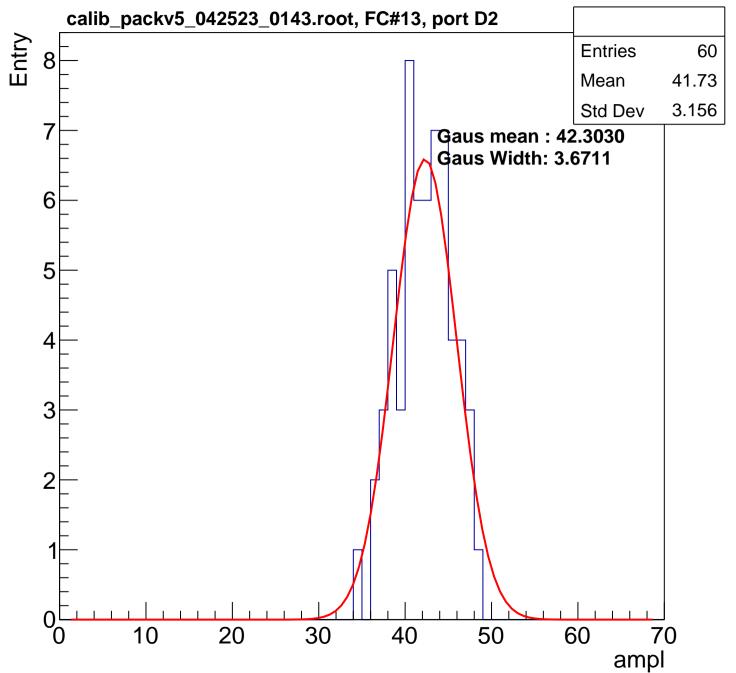


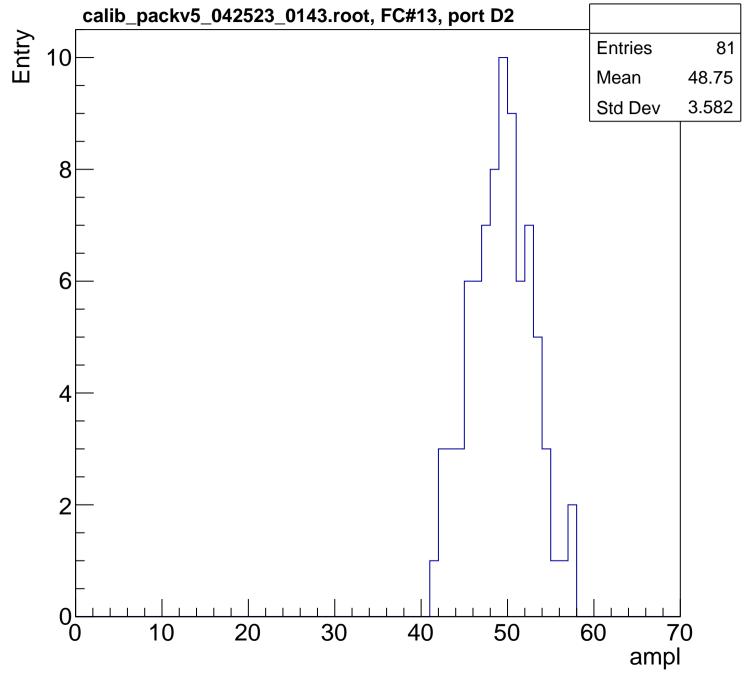


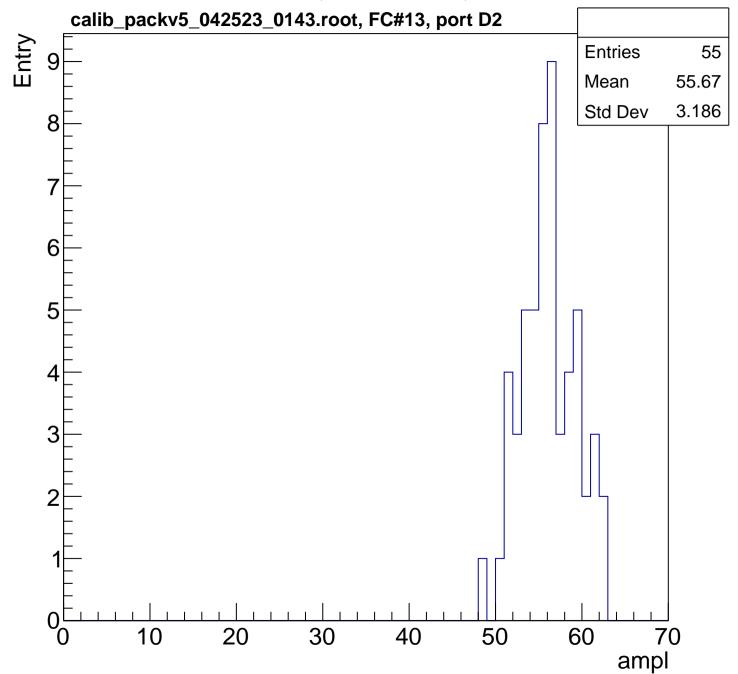


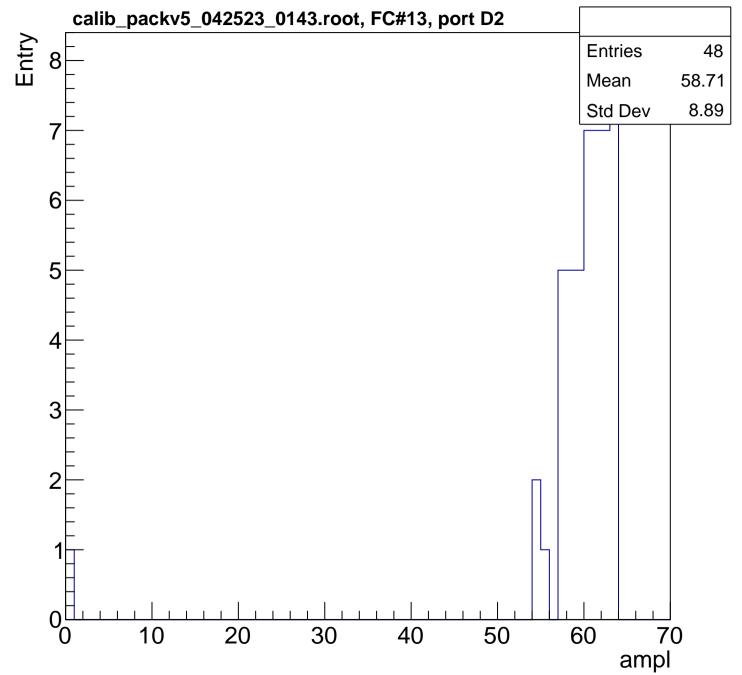


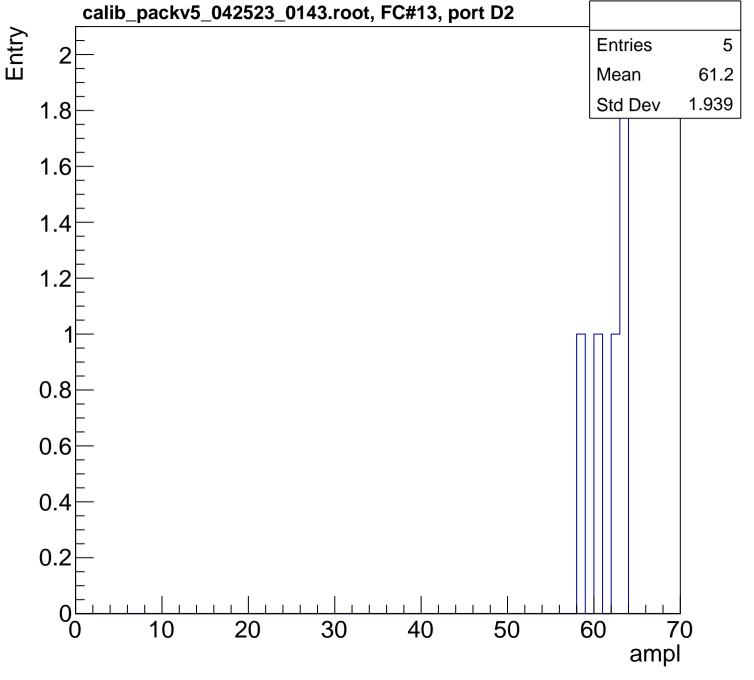




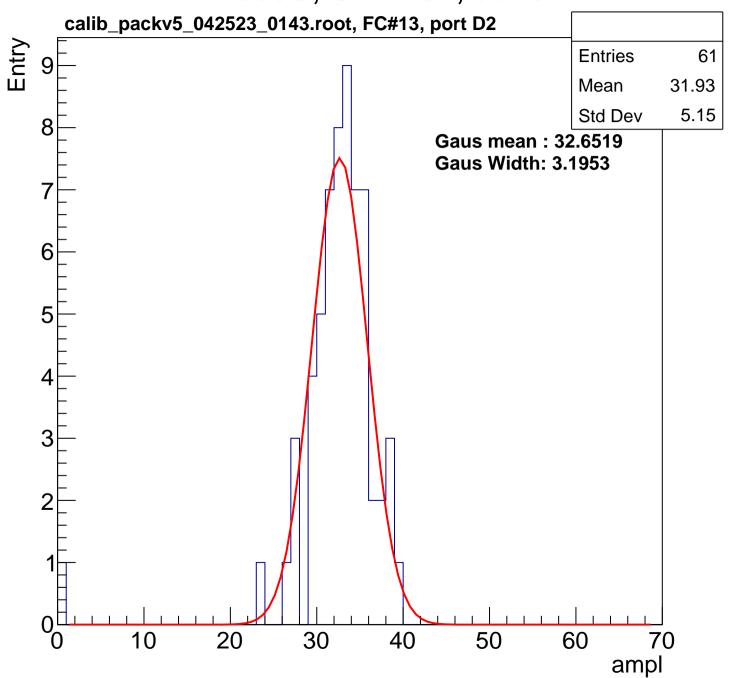


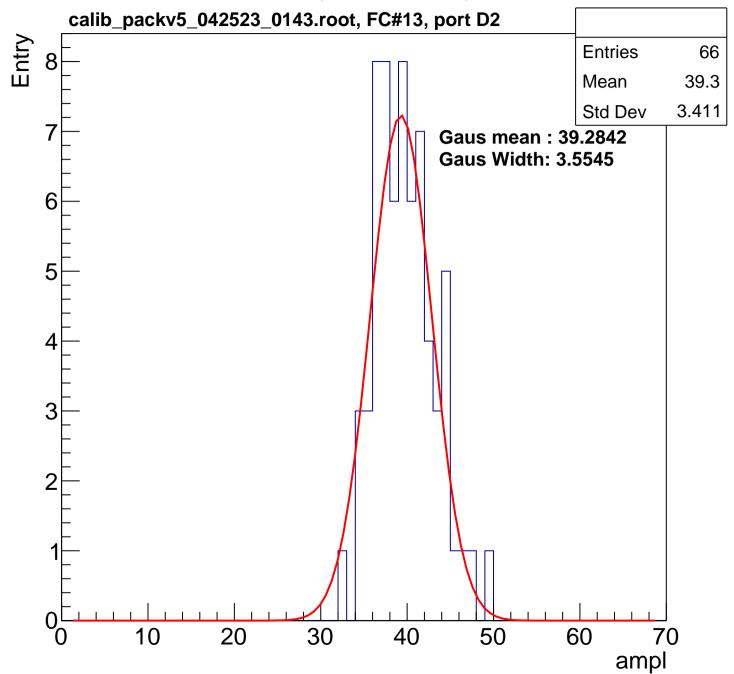


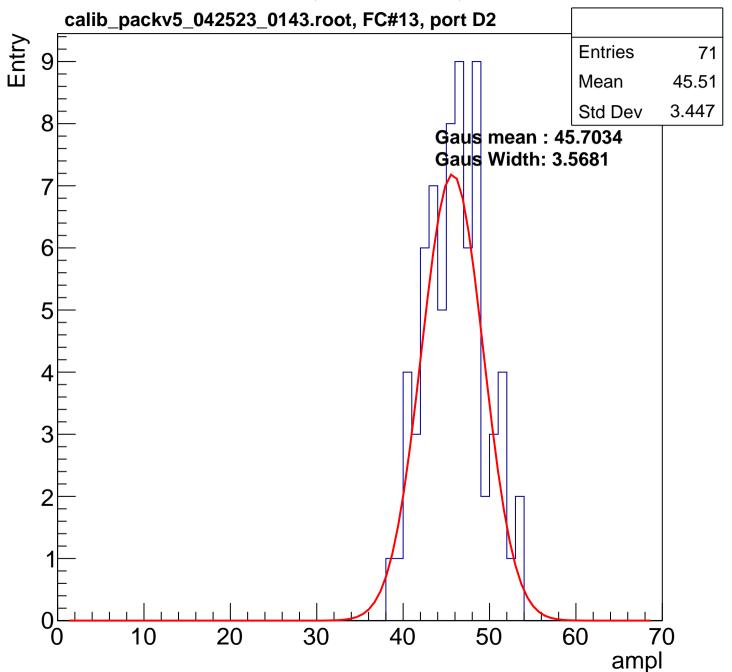


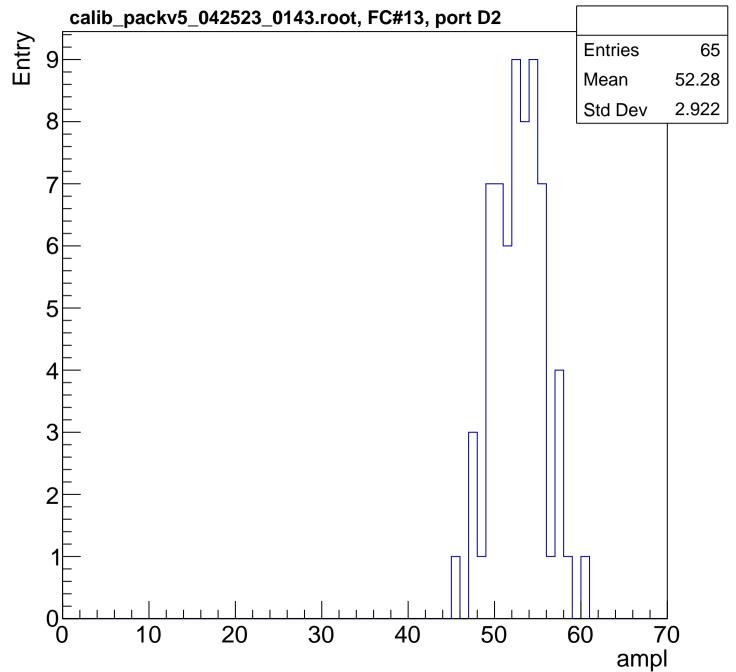


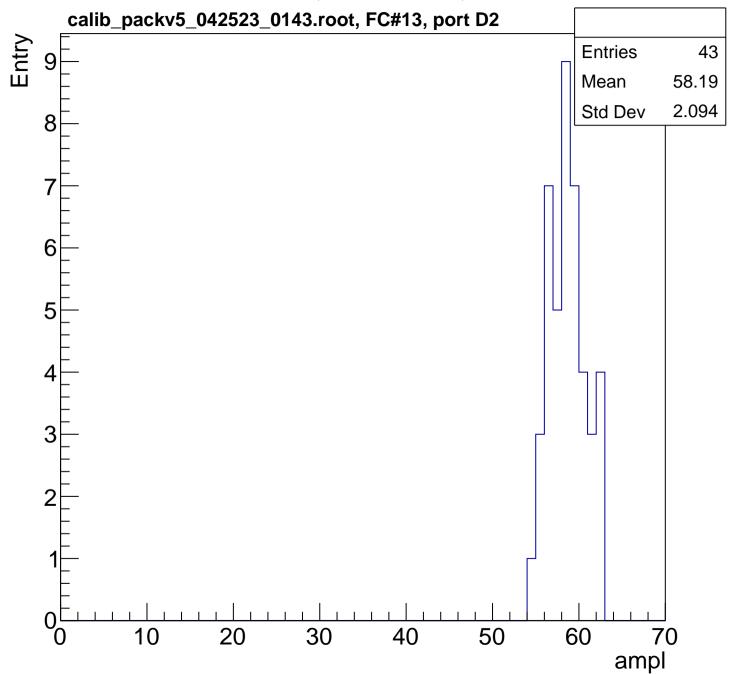


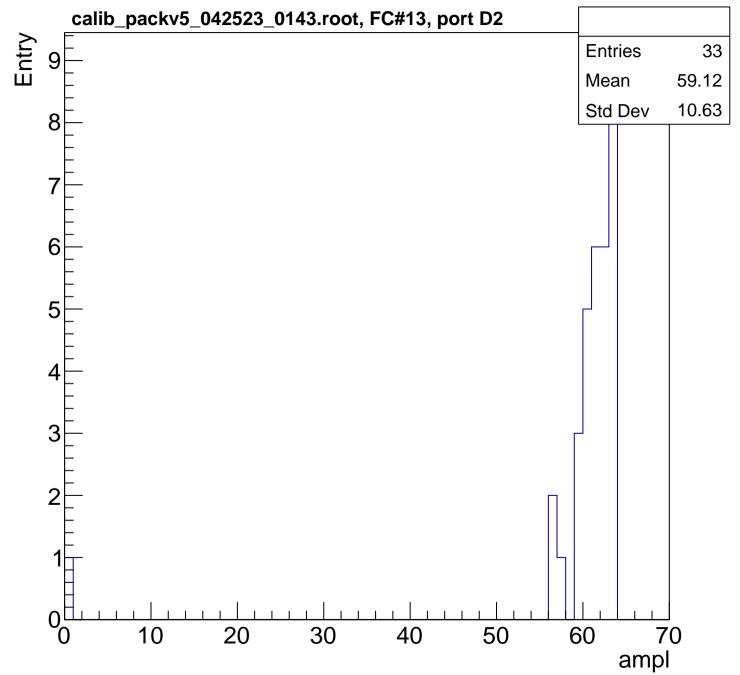


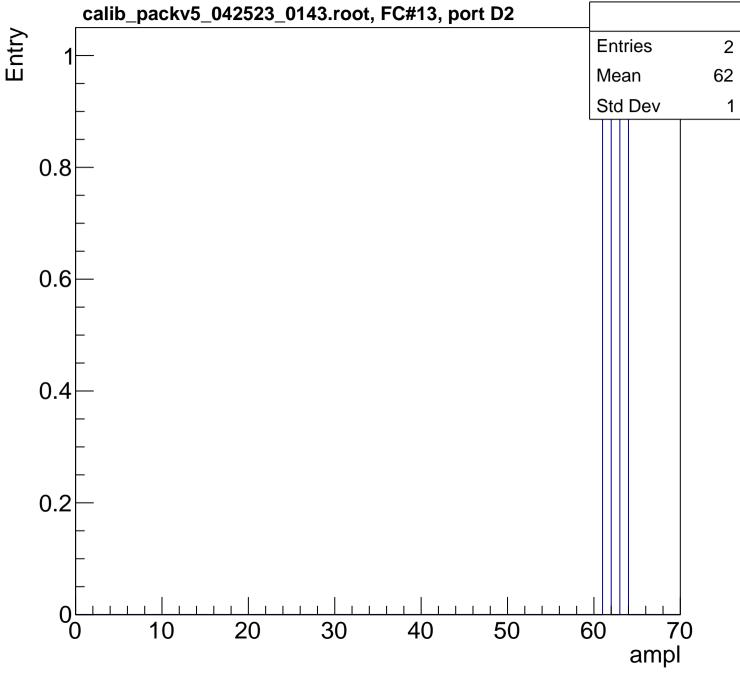




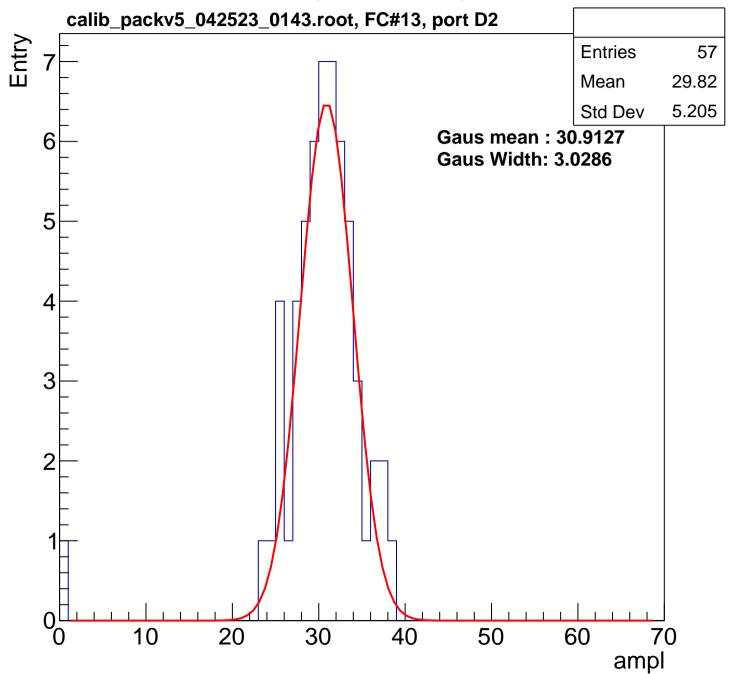


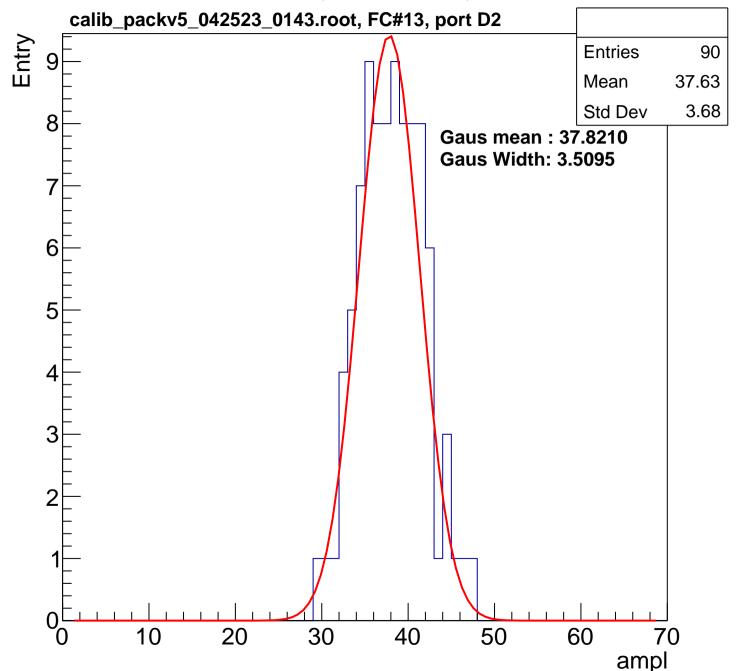


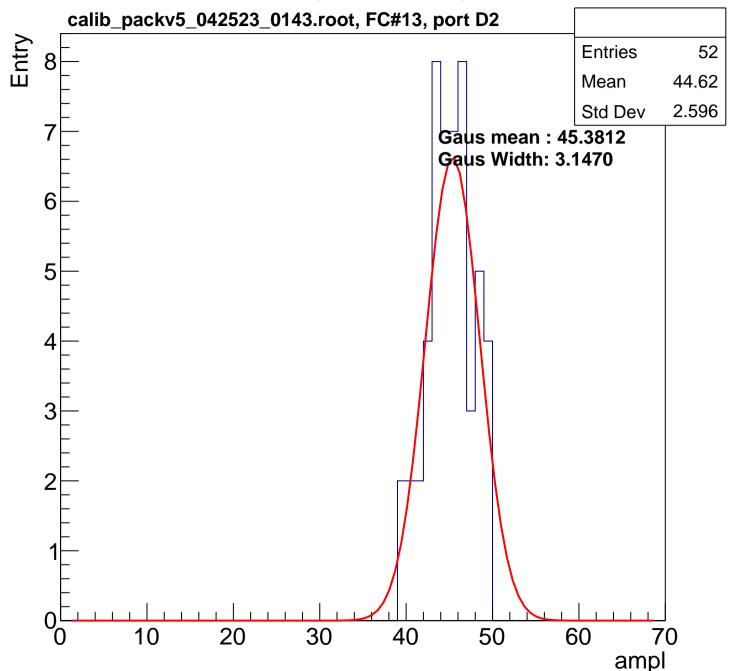


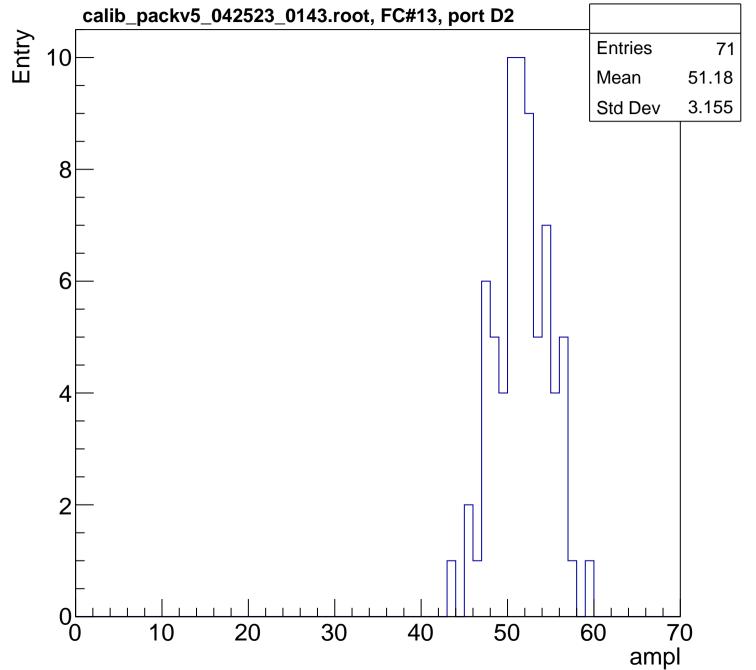


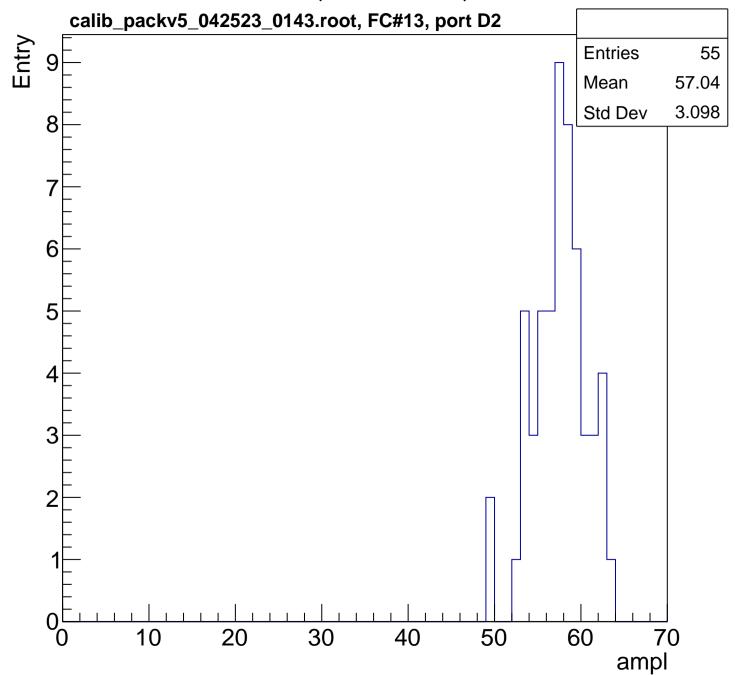
B1L003S, U7-ch64, adc7 calib_packv5_042523_0143.root, FC#13, port D2 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

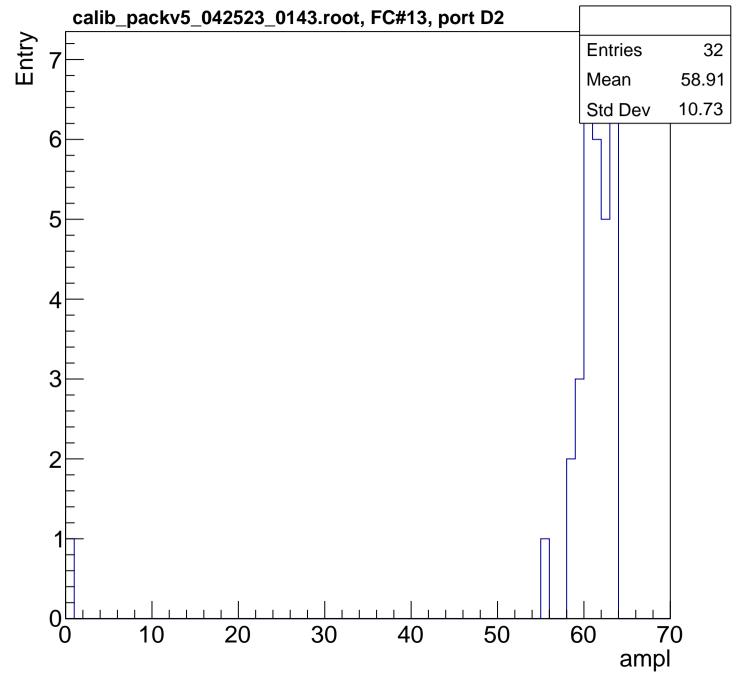


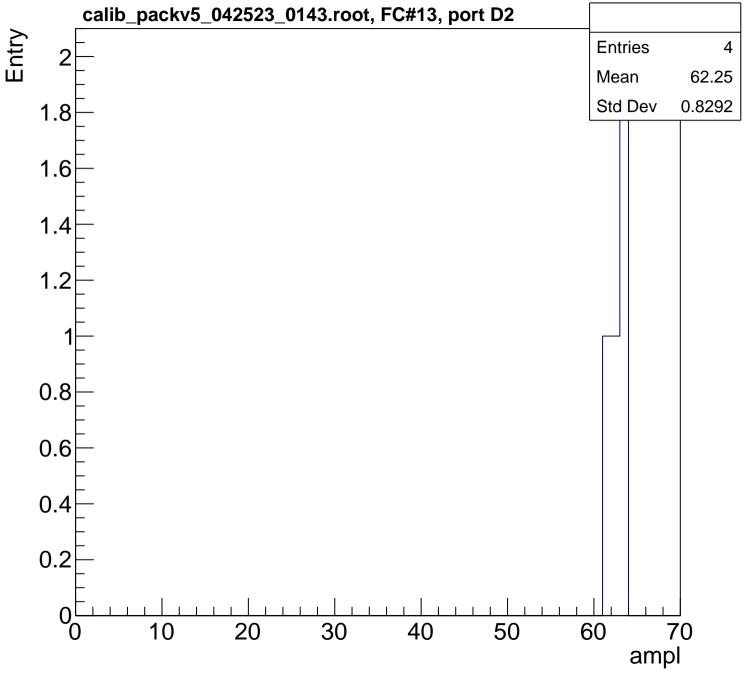




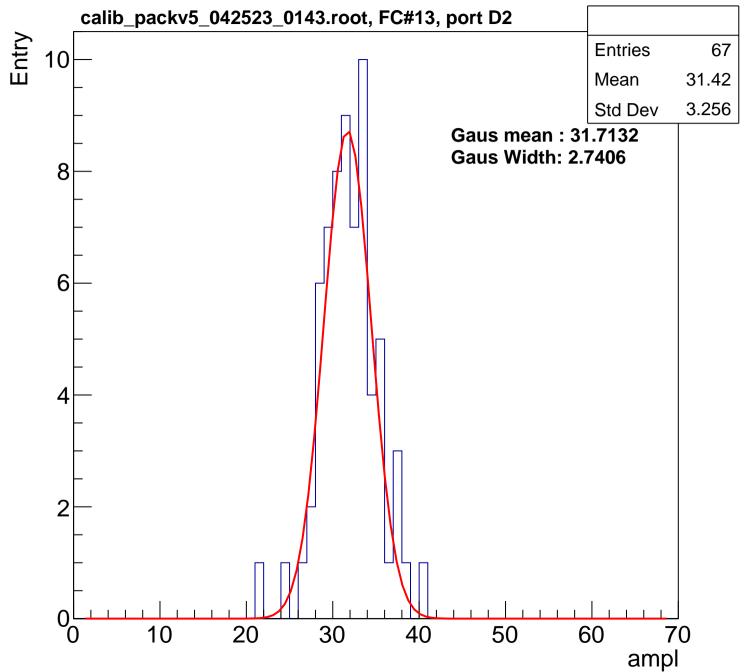


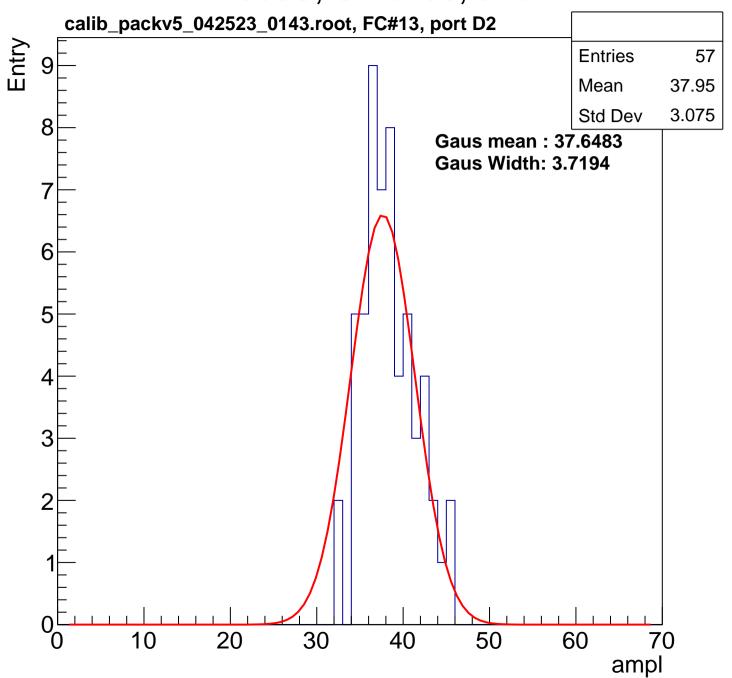


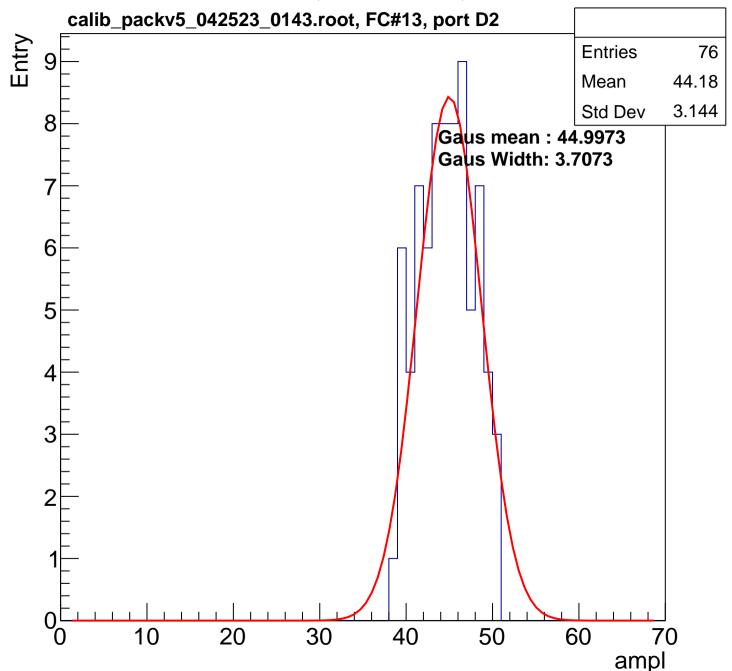


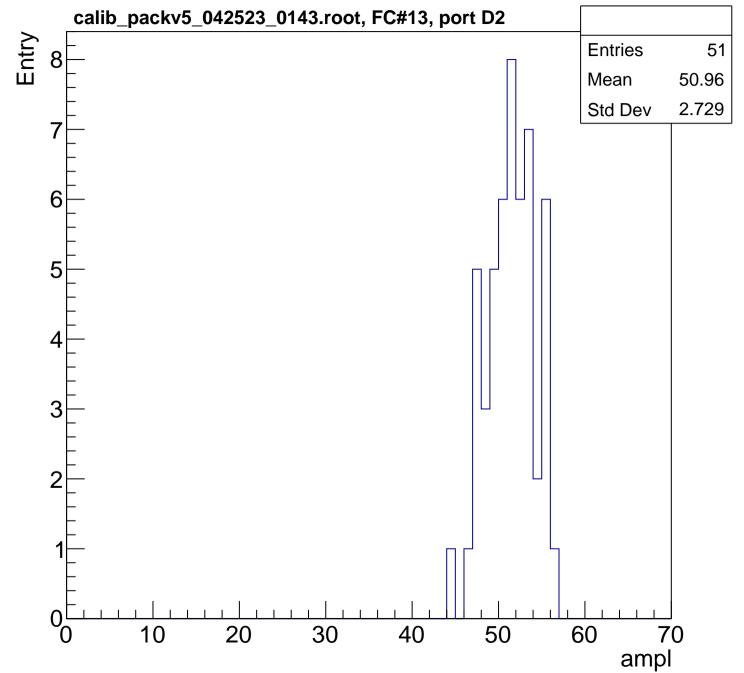


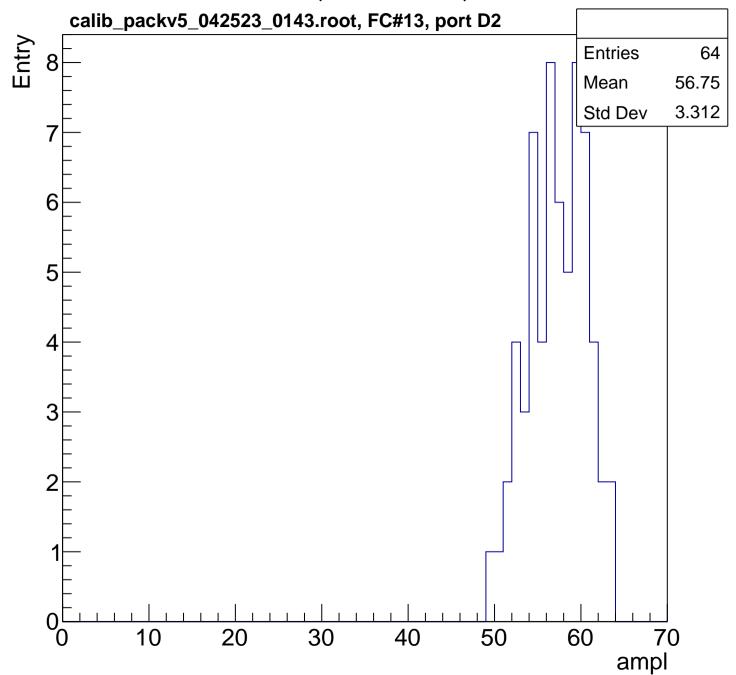


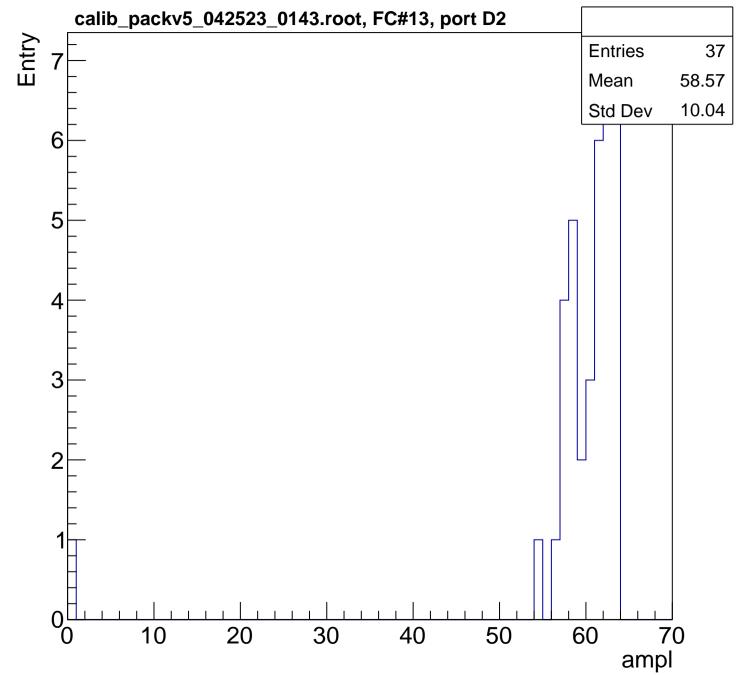


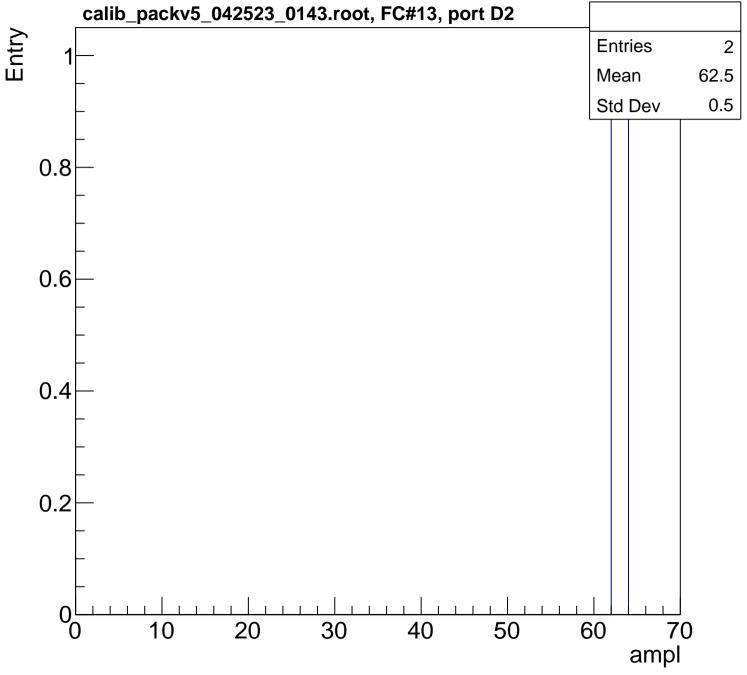




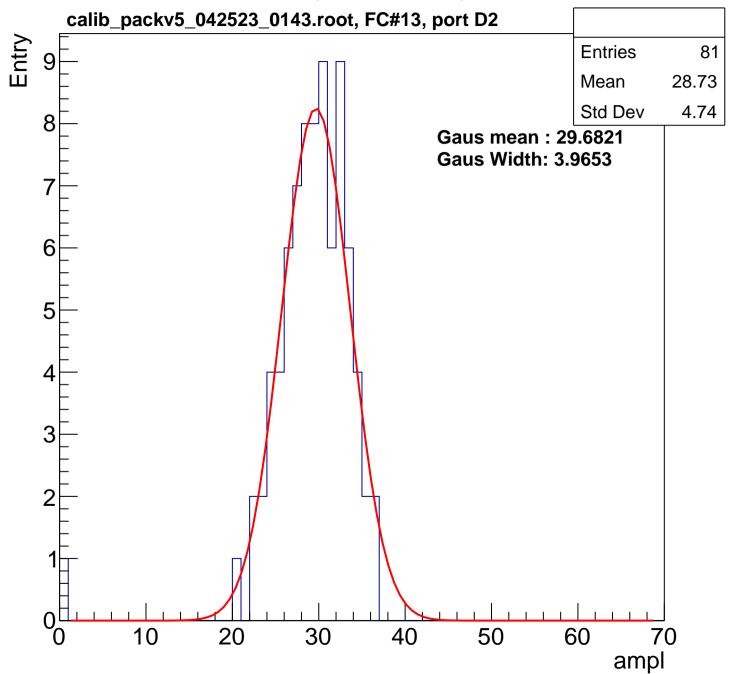


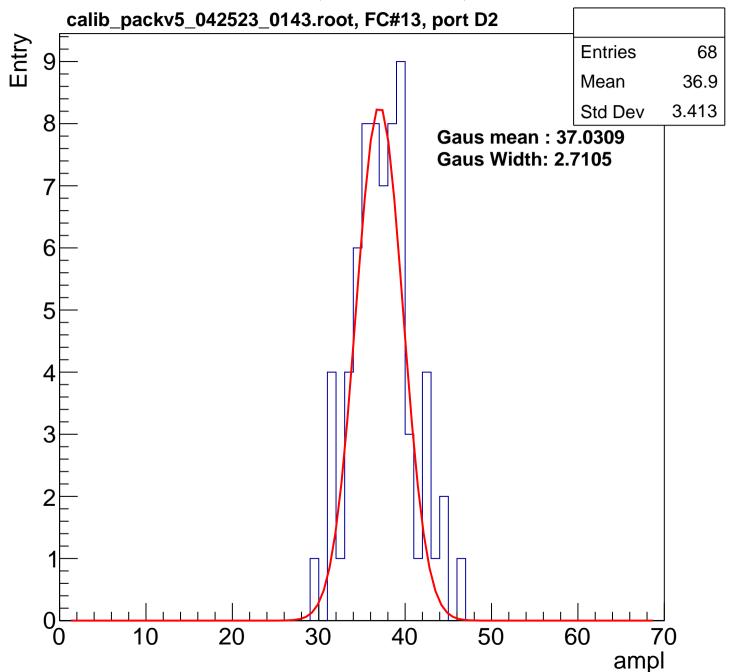


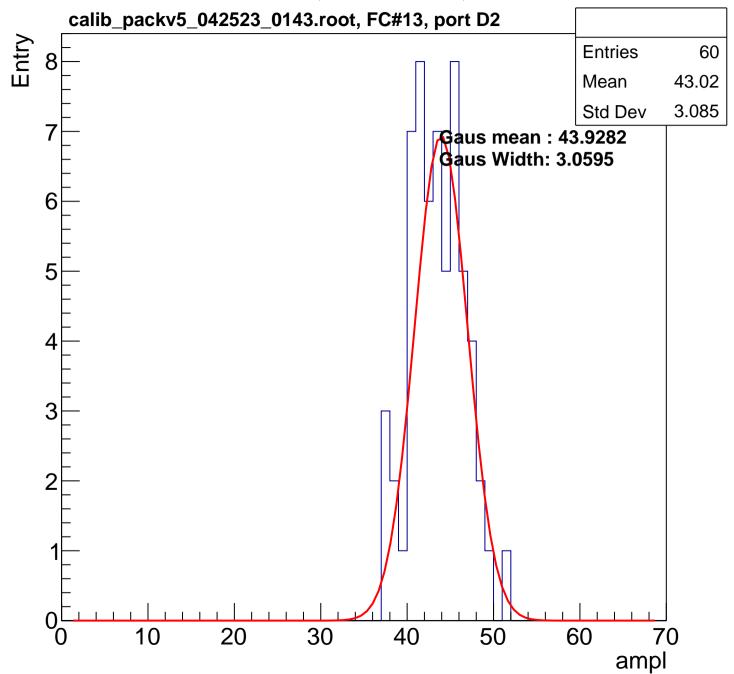


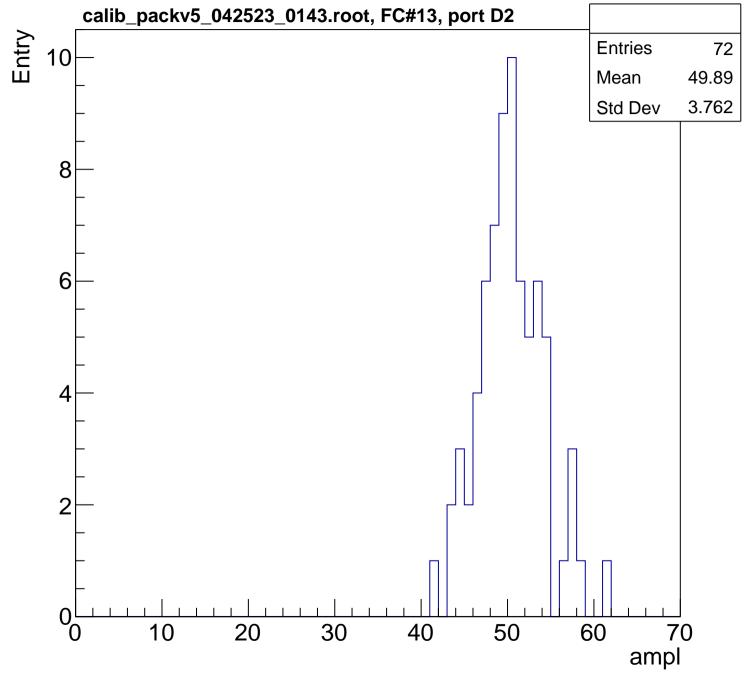


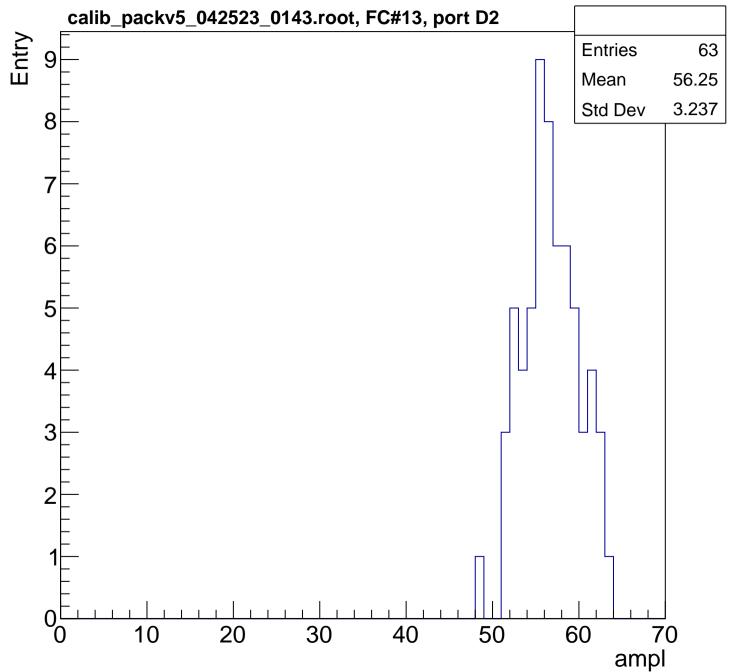
B1L003S, U7-ch66, adc7 calib_packv5_042523_0143.root, FC#13, port D2 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

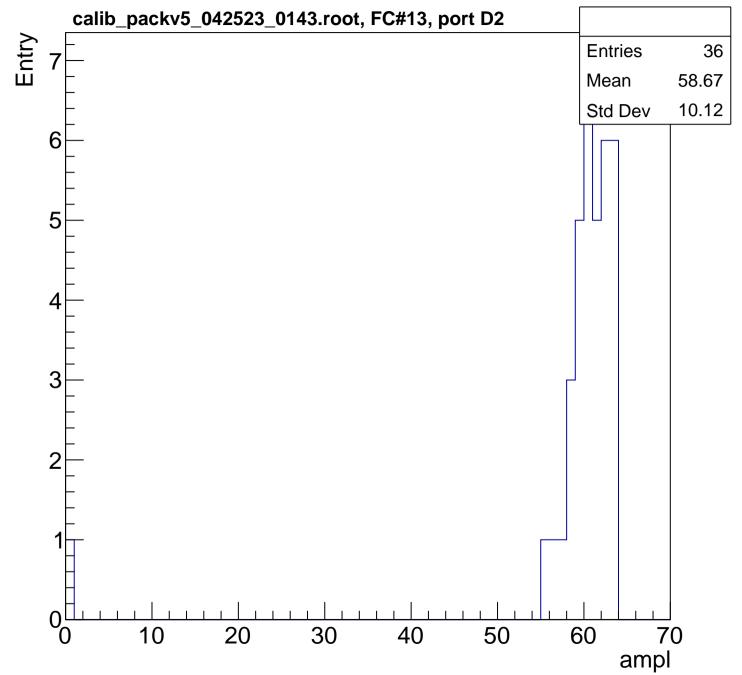


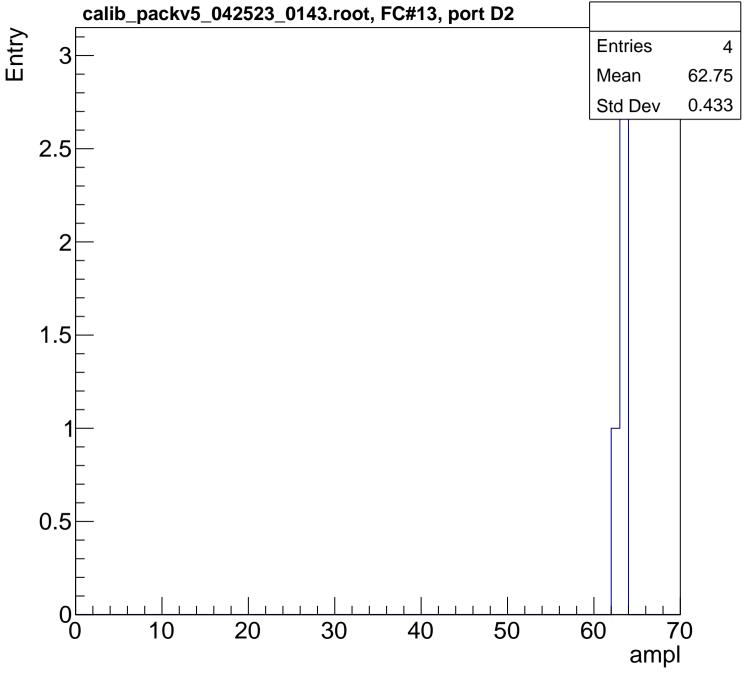




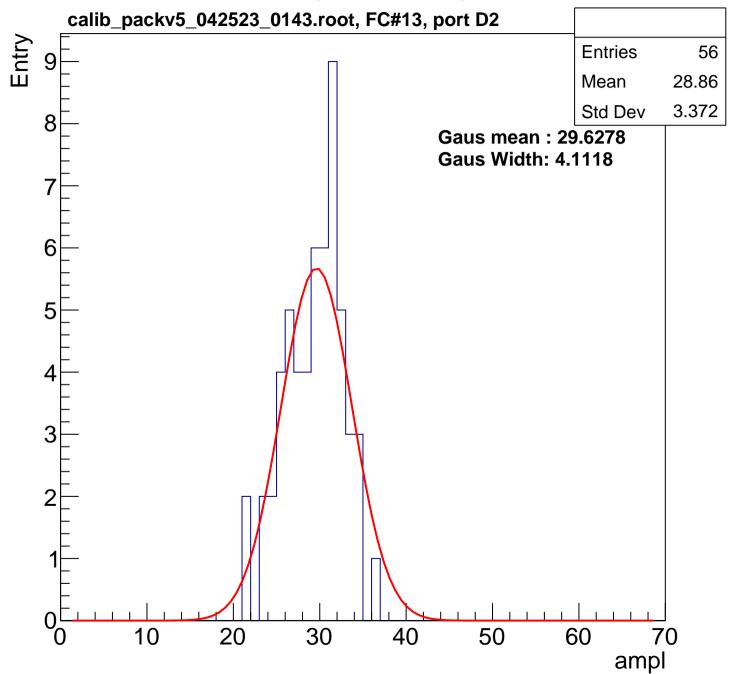


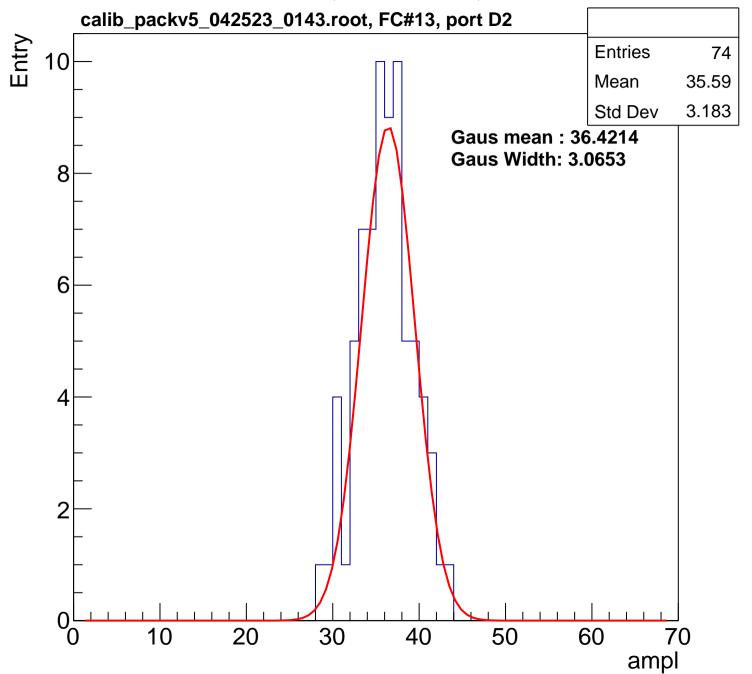


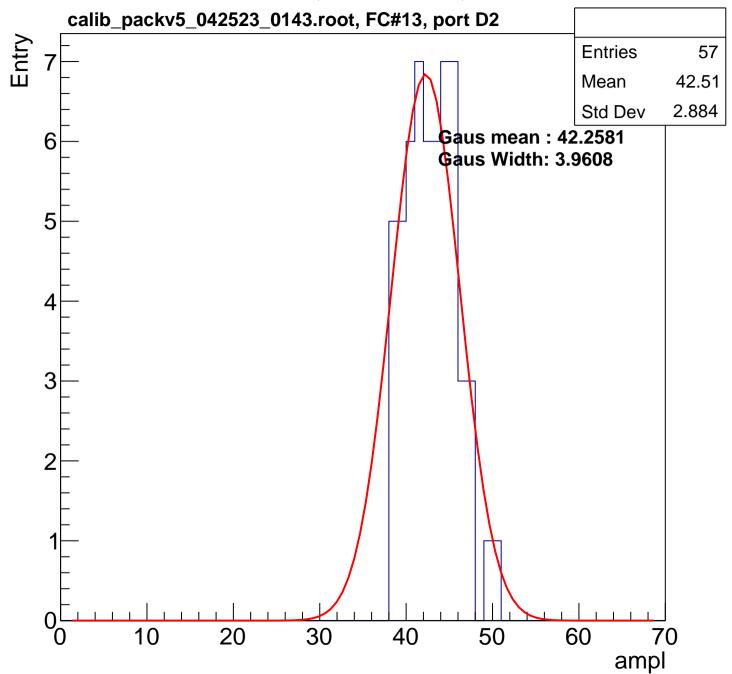


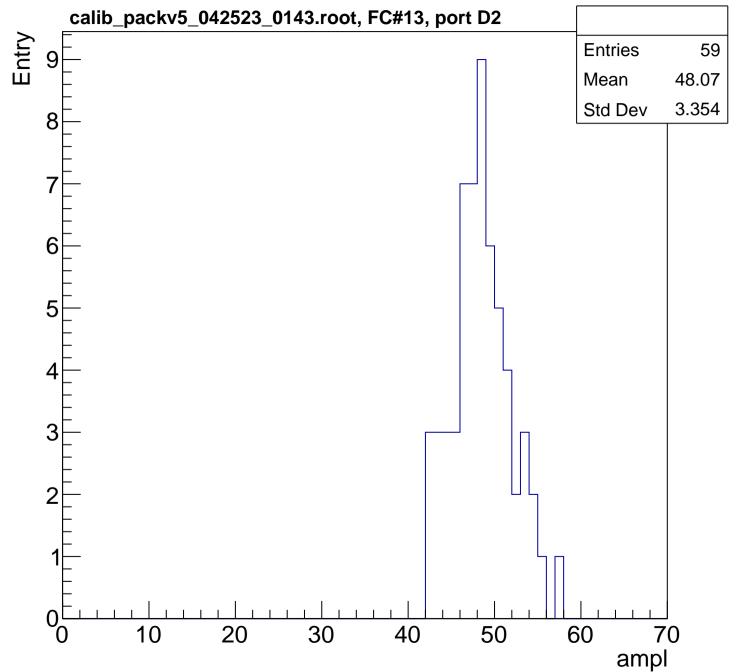


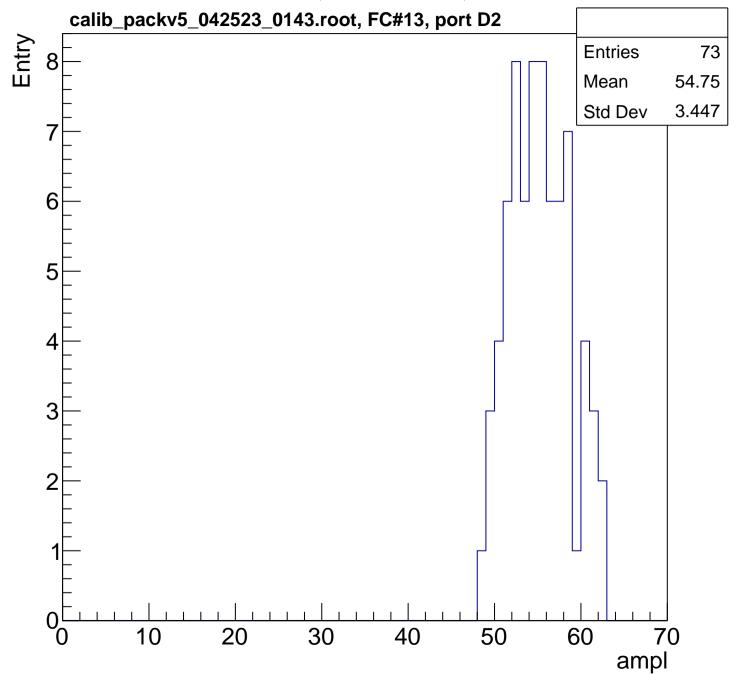


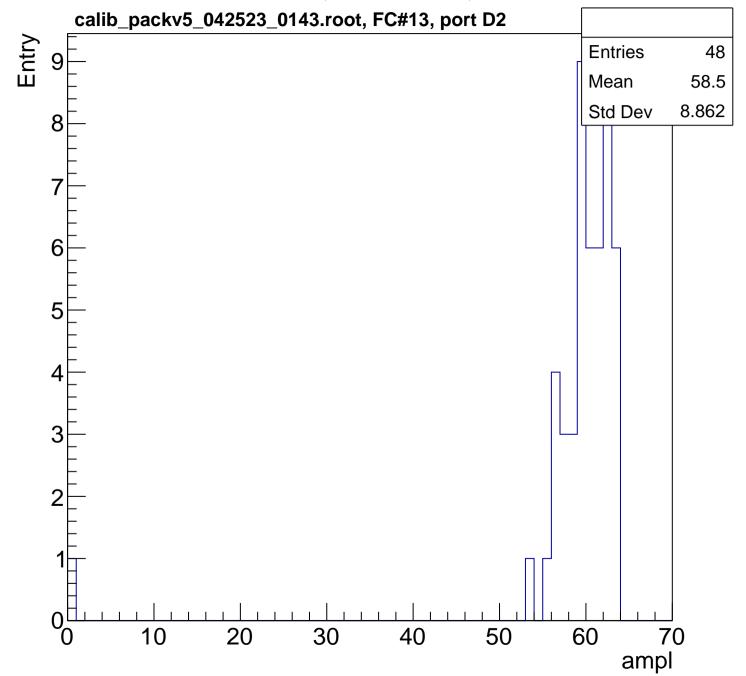


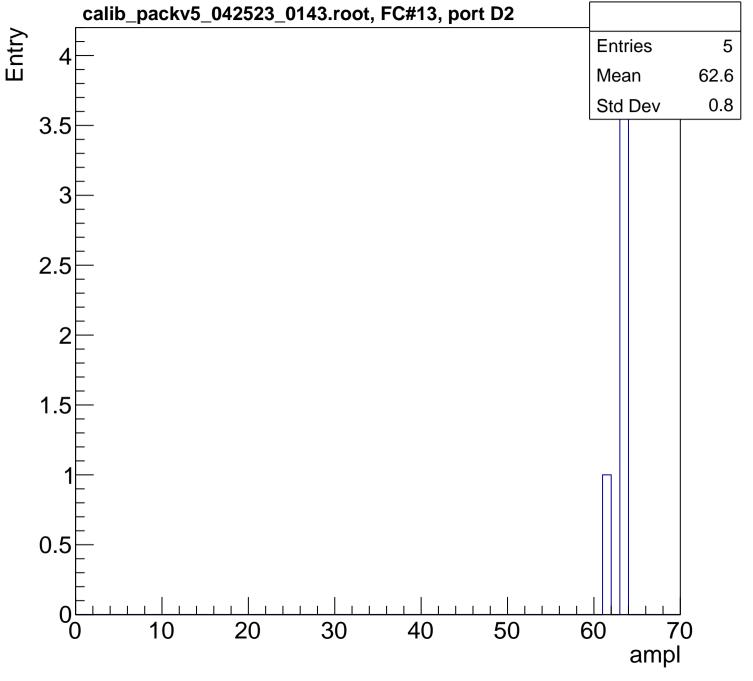




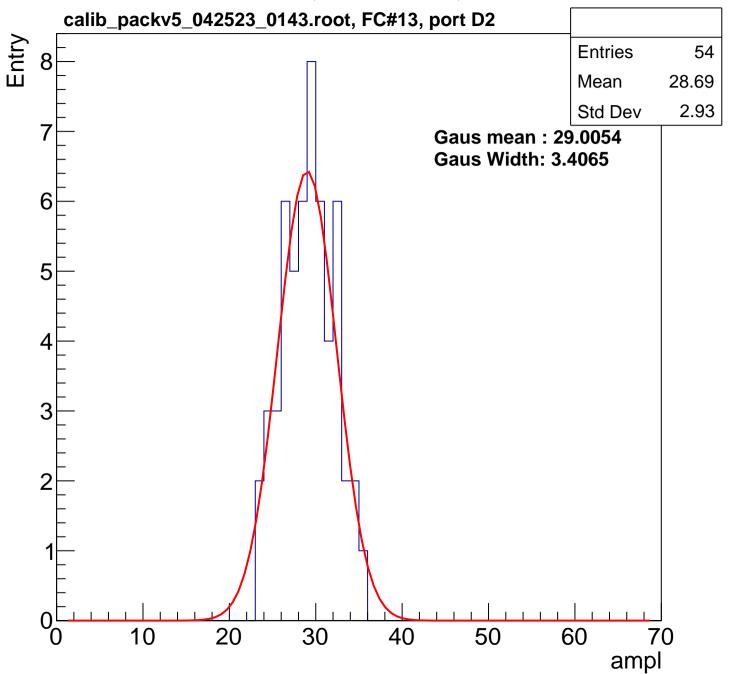


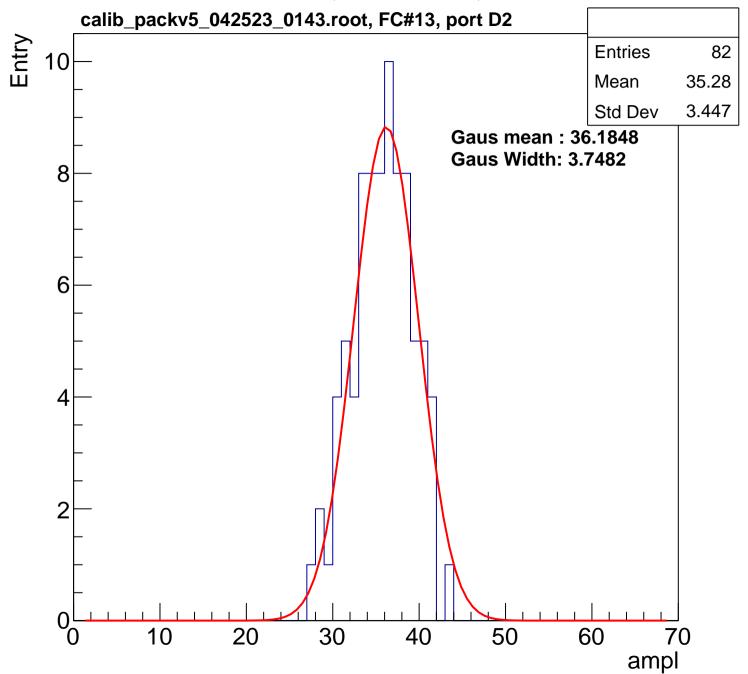


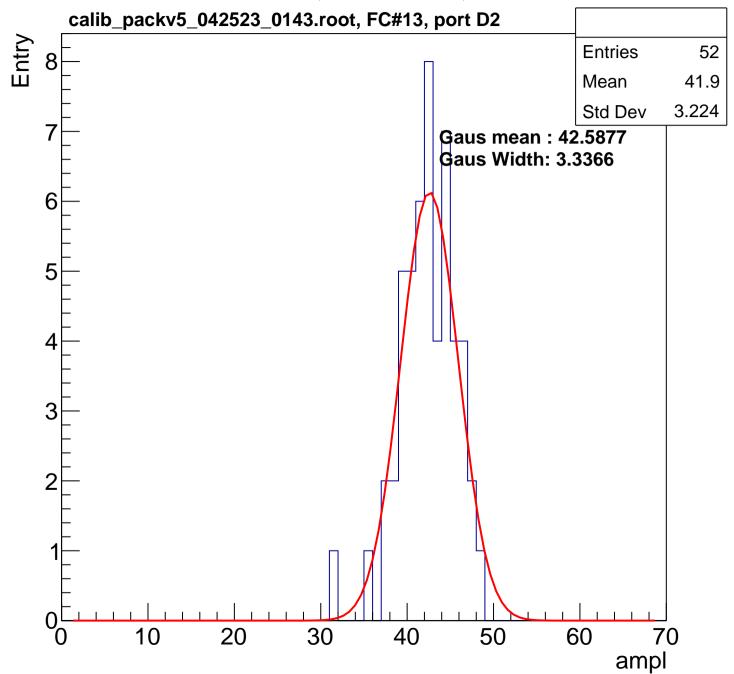


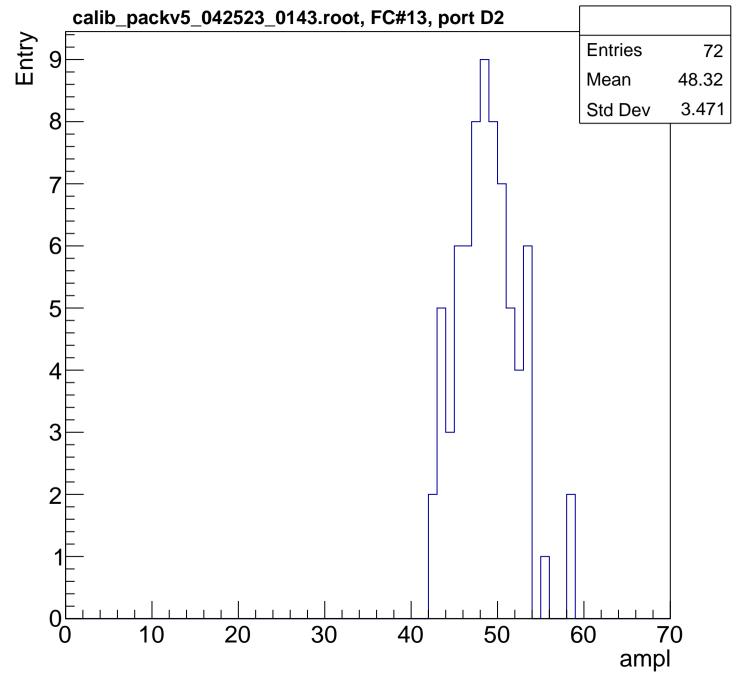


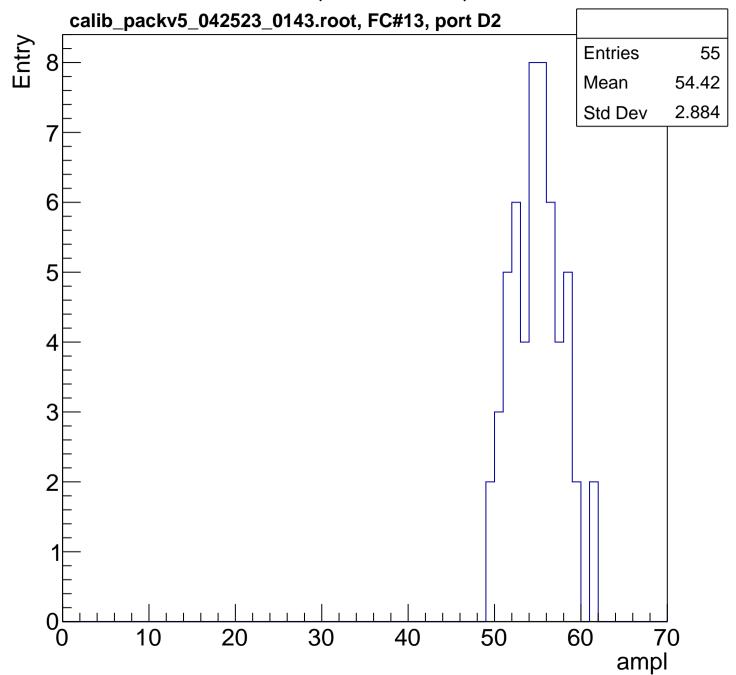
B1L003S, U7-ch68, adc7 calib_packv5_042523_0143.root, FC#13, port D2 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

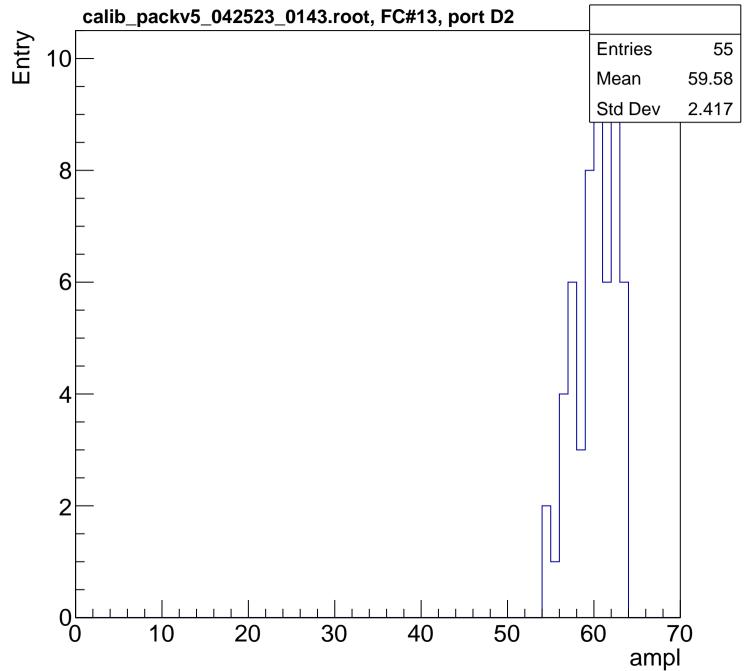


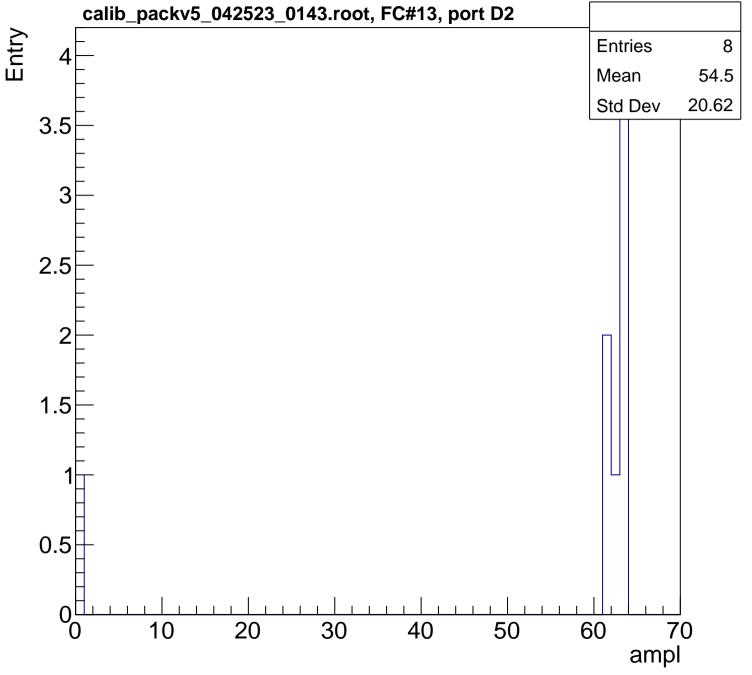




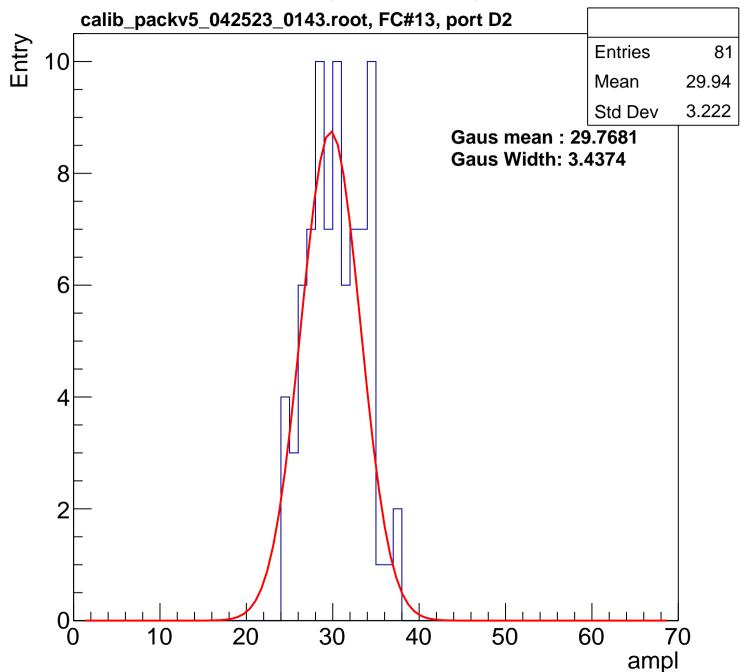


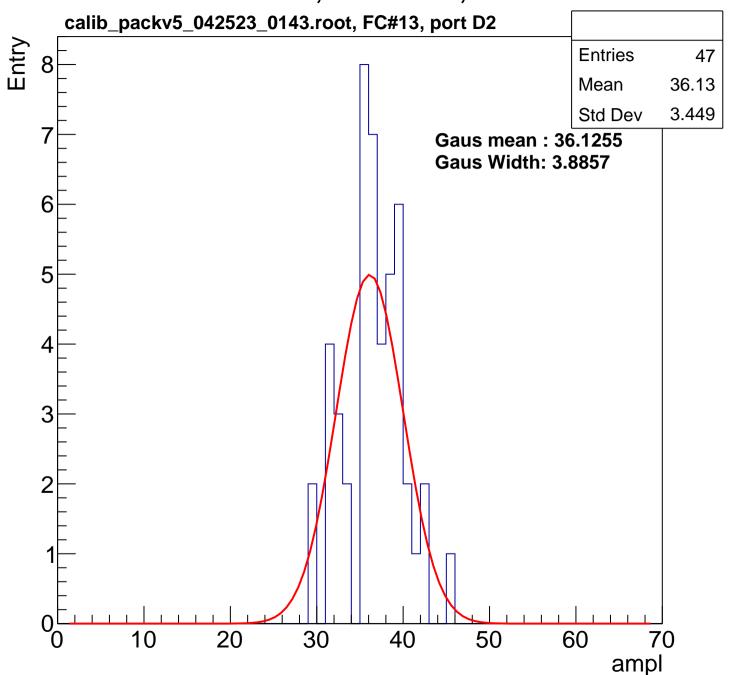


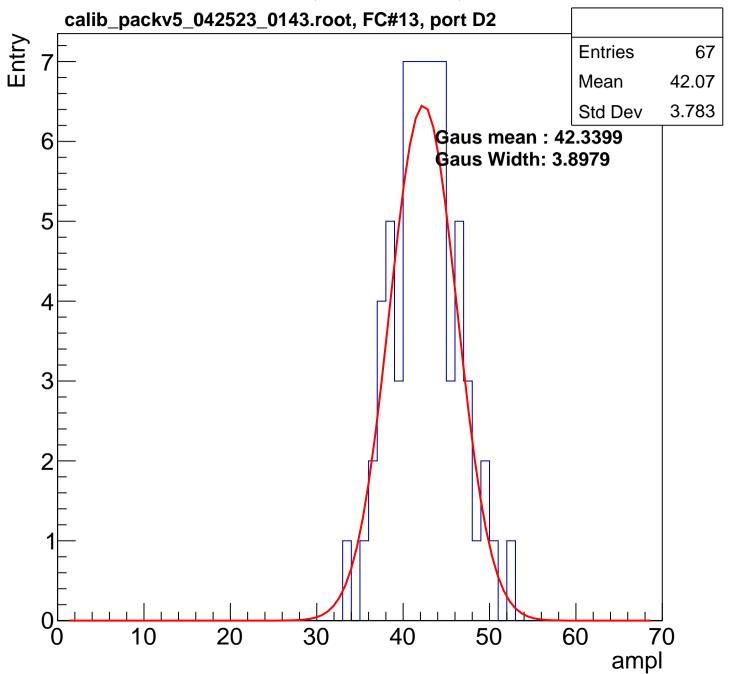


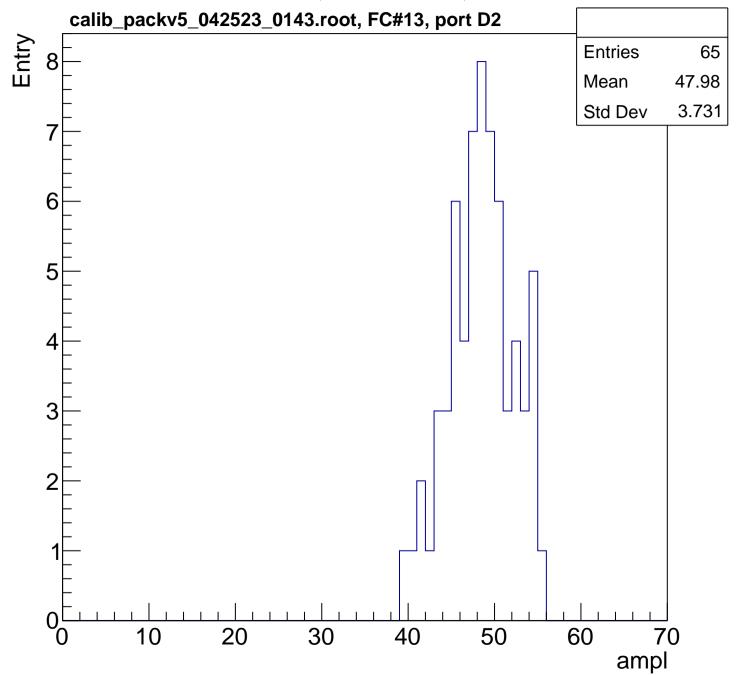


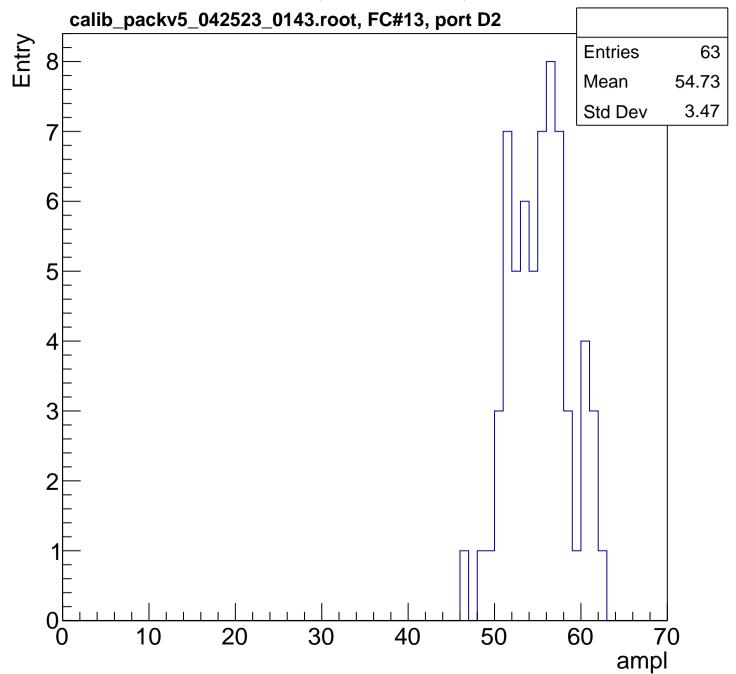


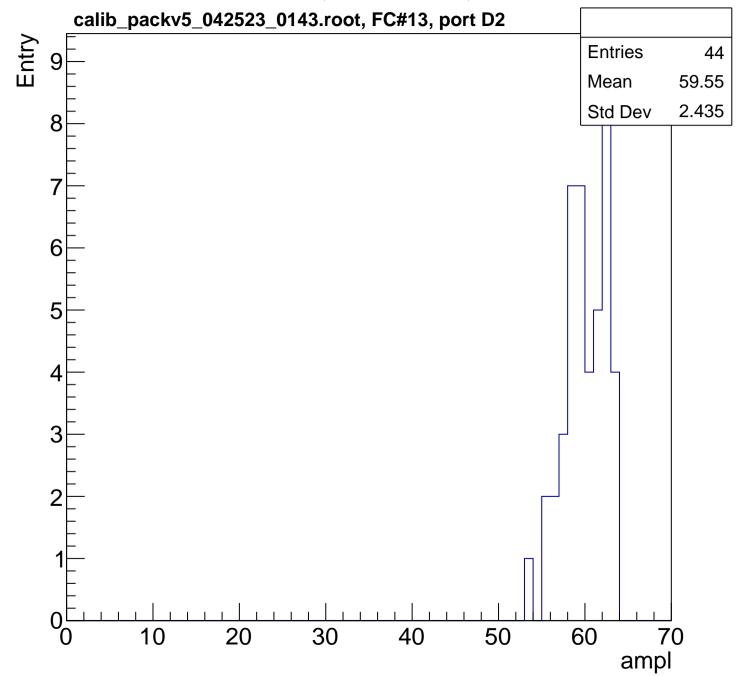


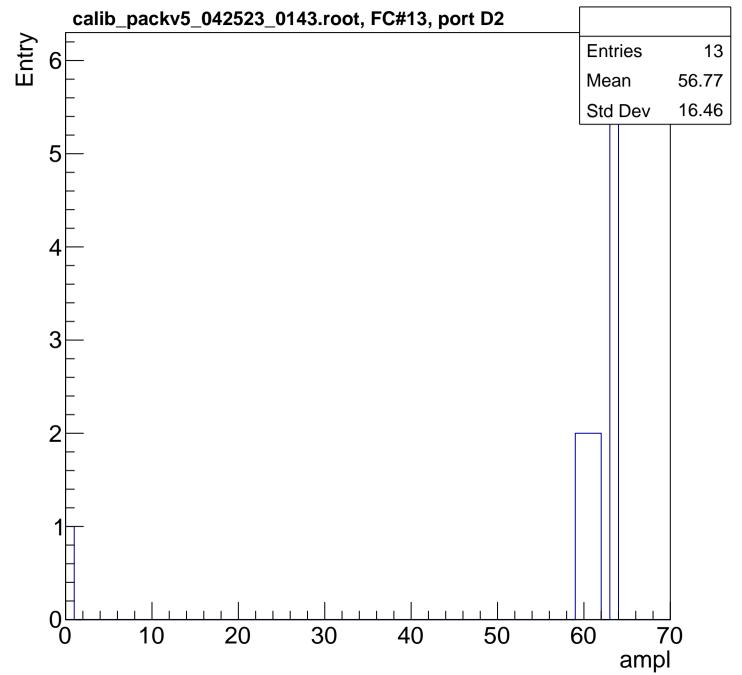




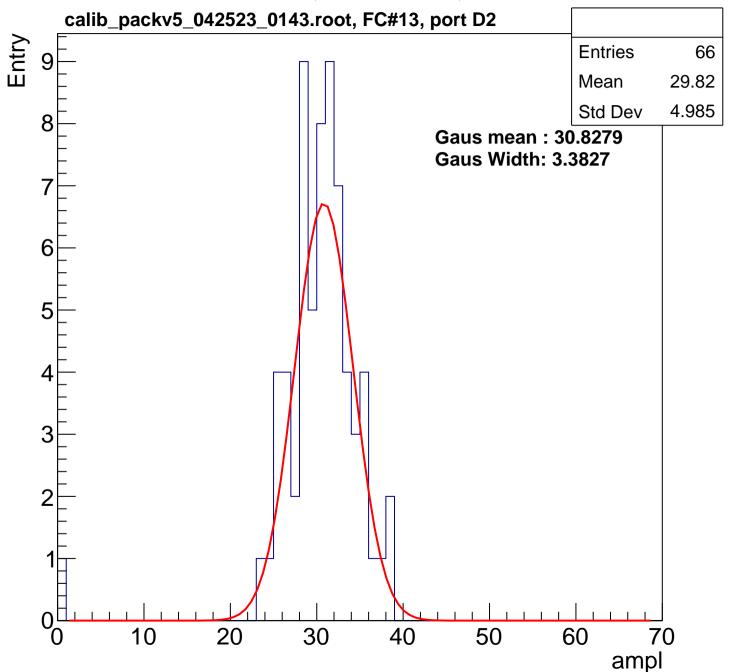


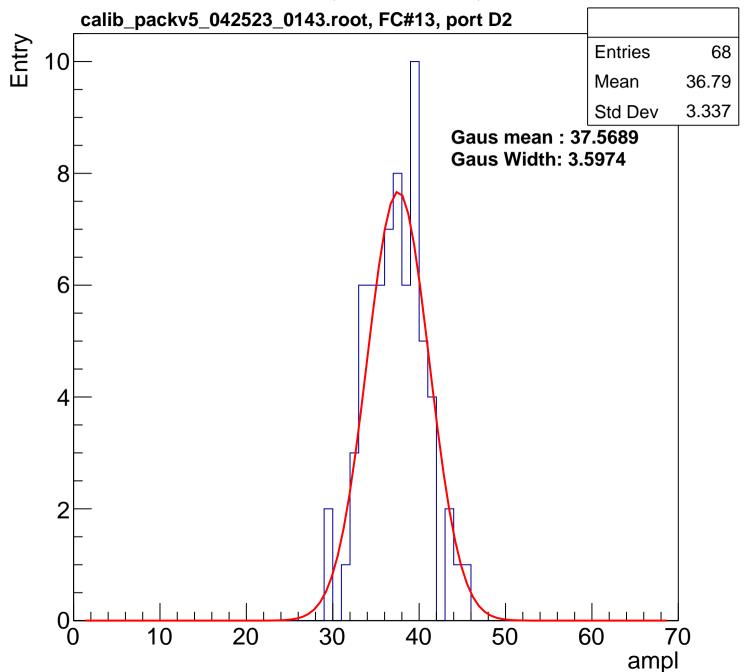


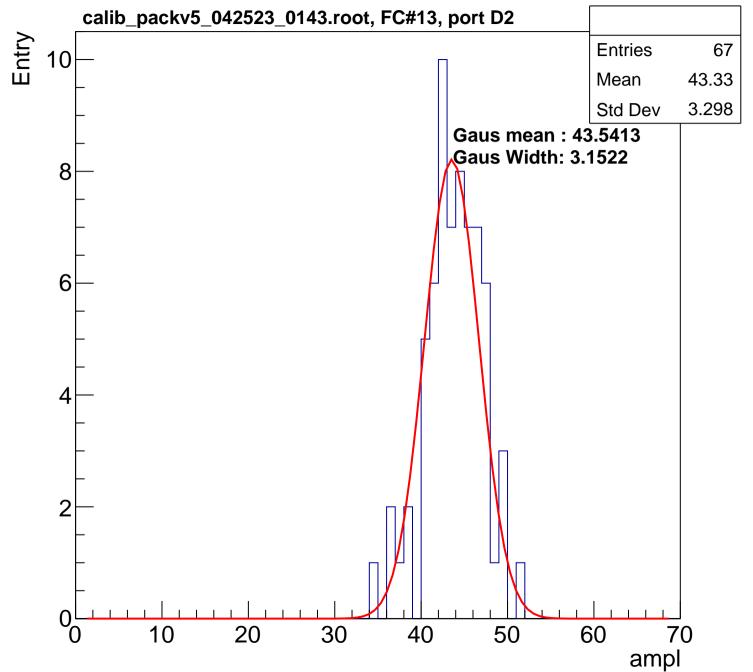


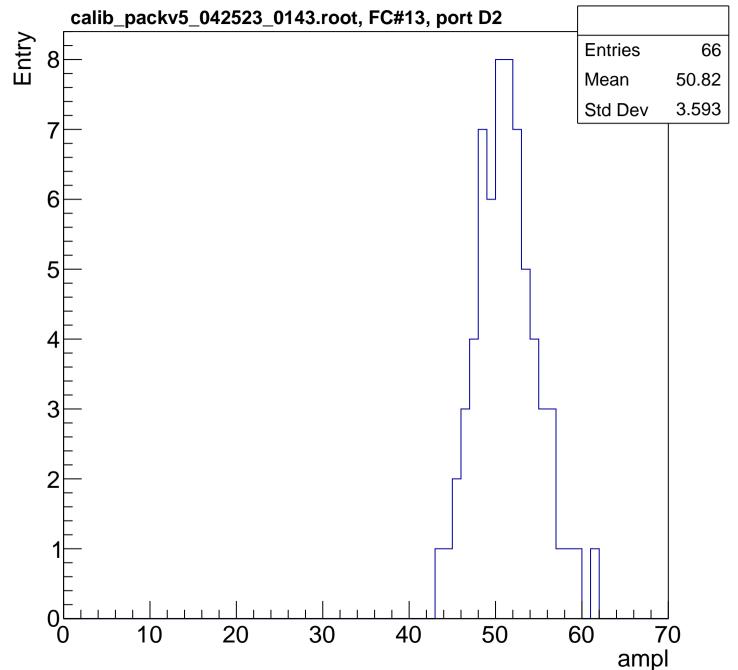


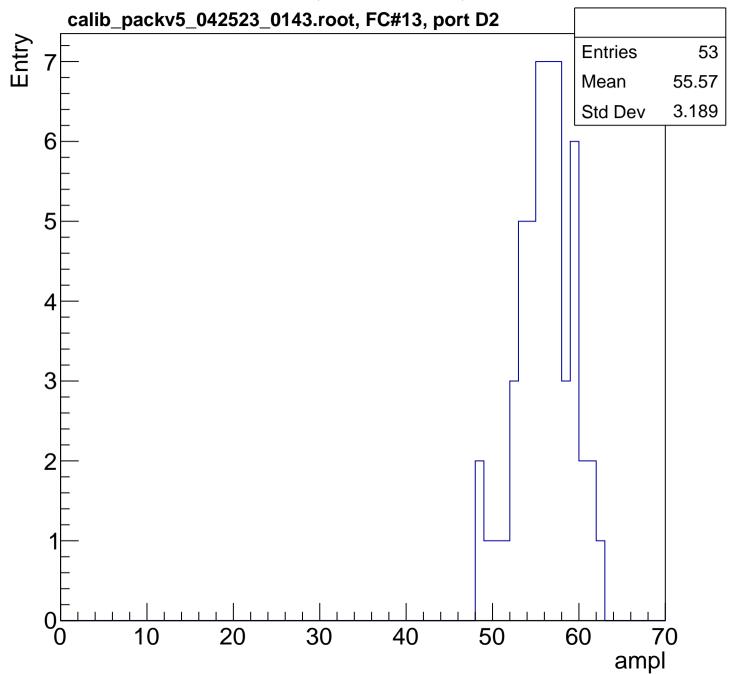


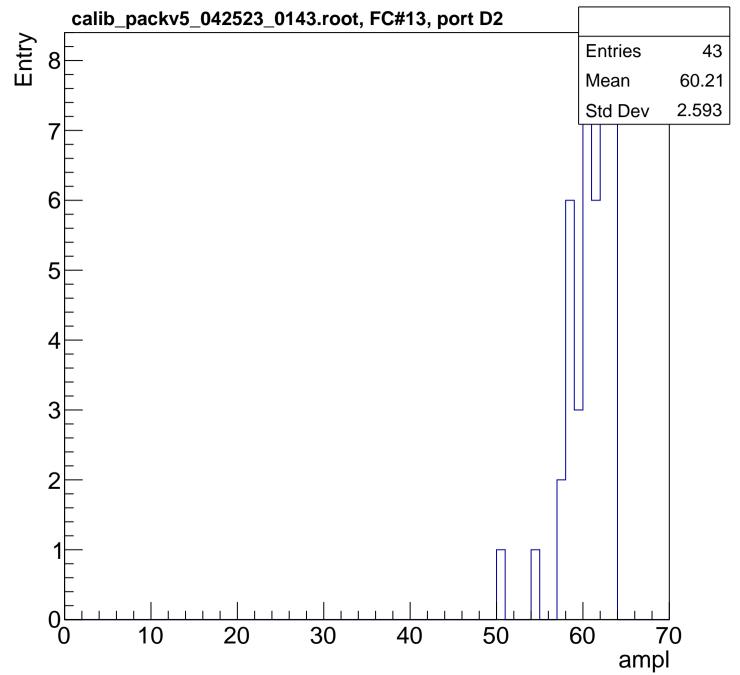


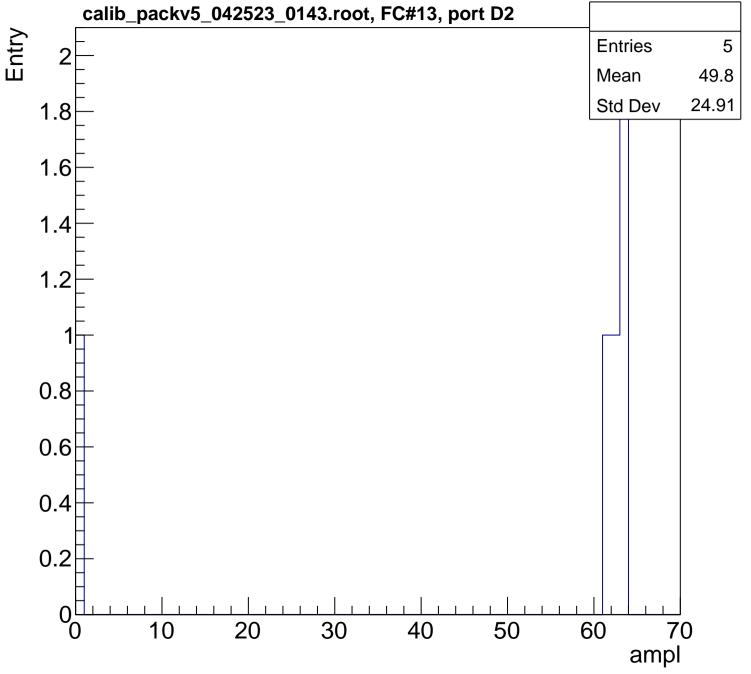




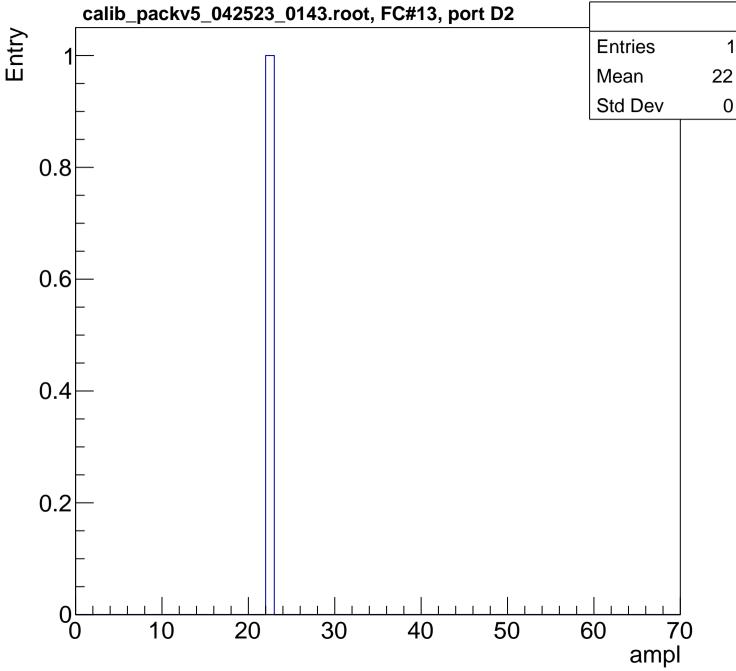


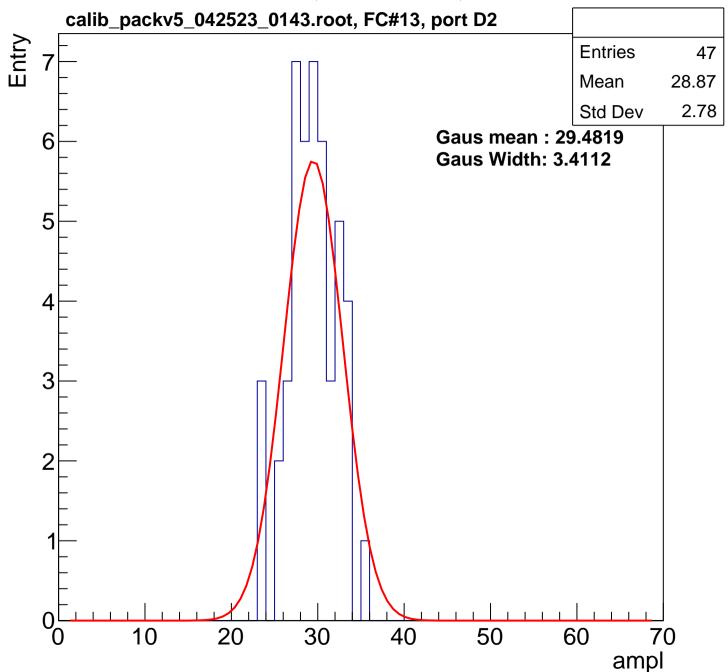


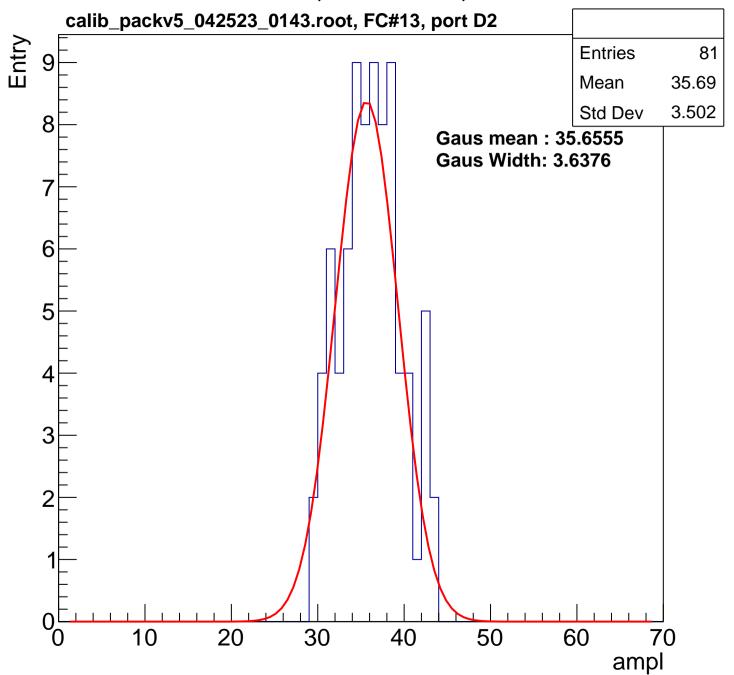


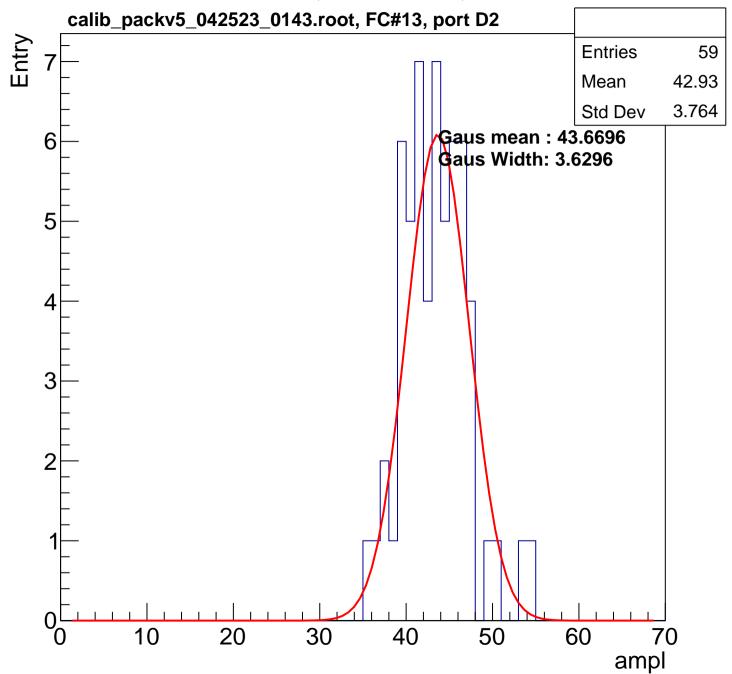


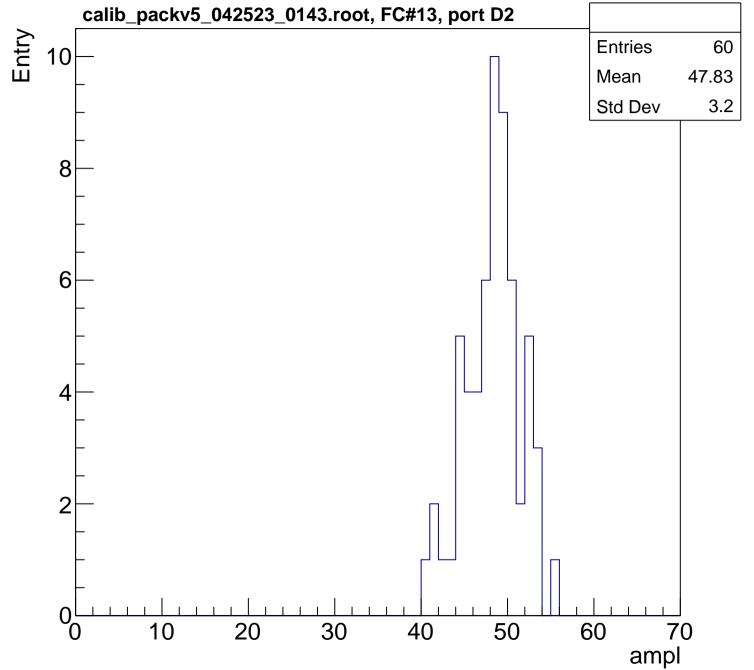
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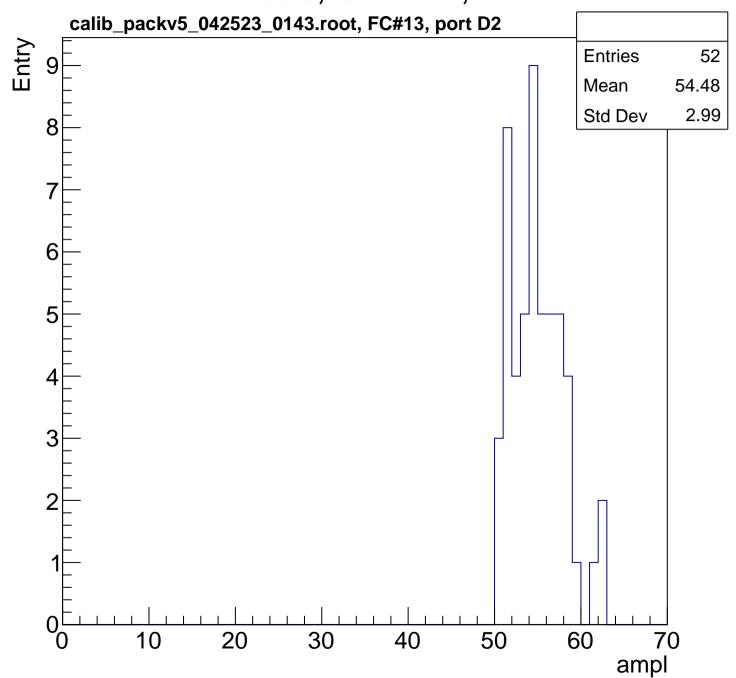


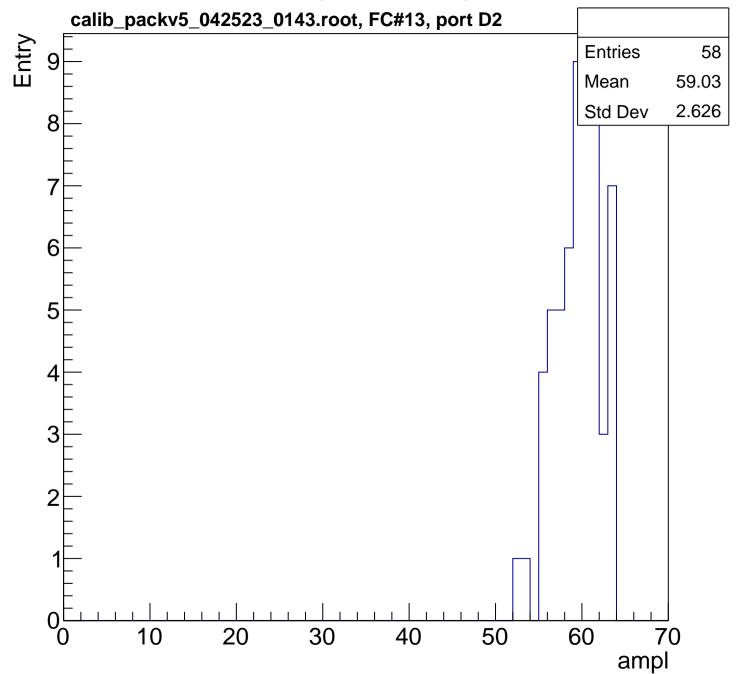


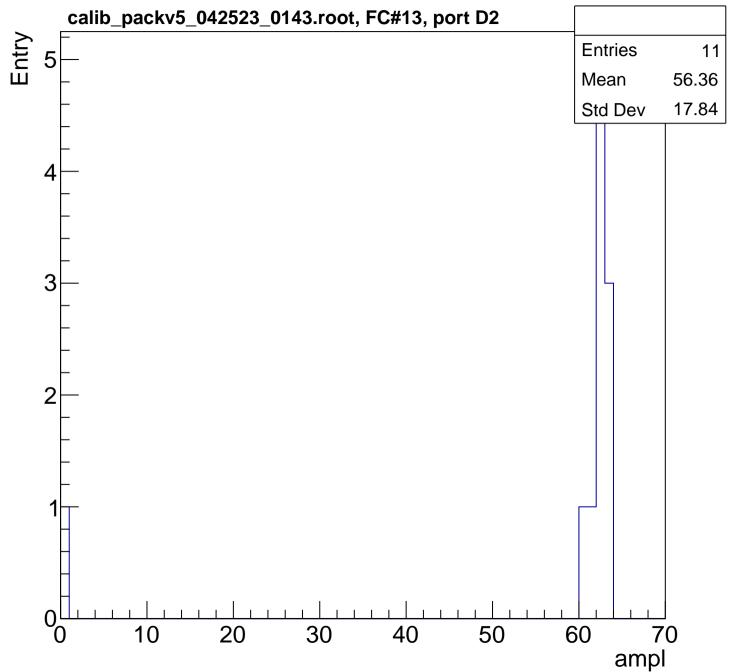




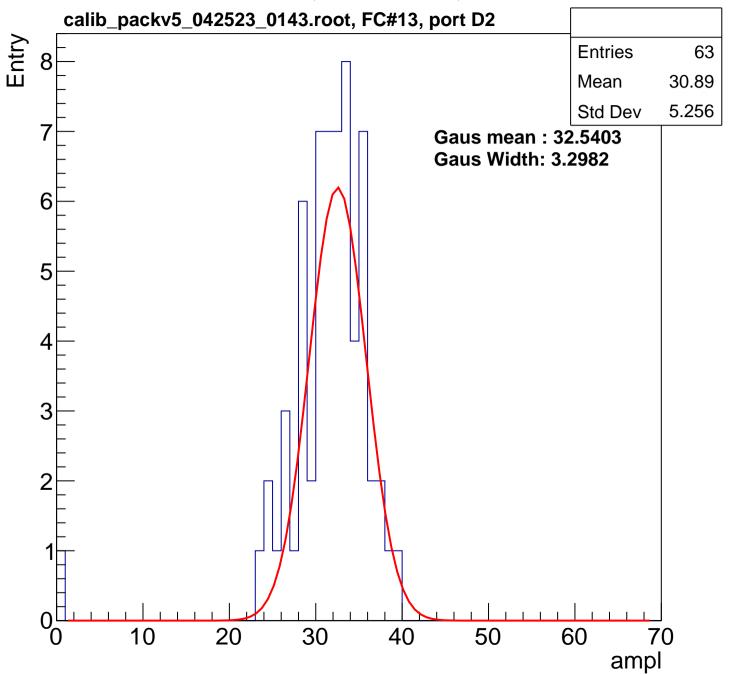


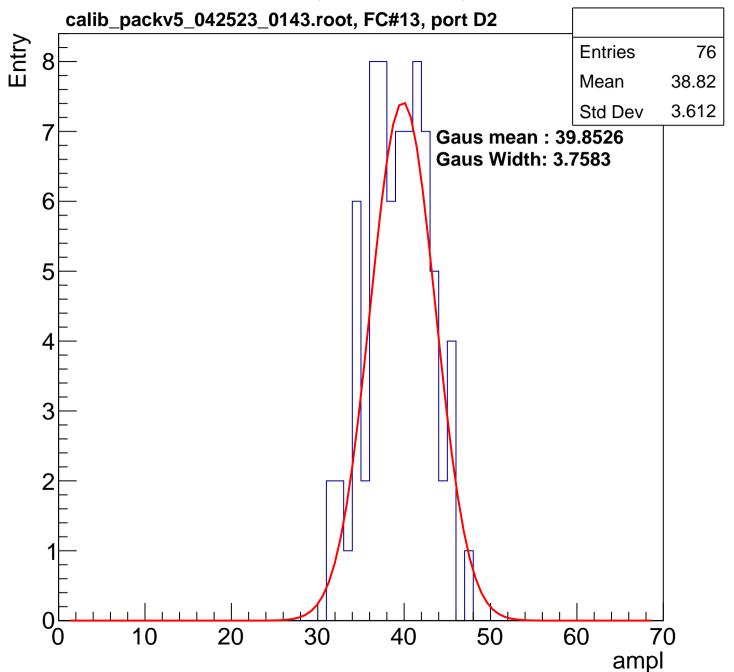


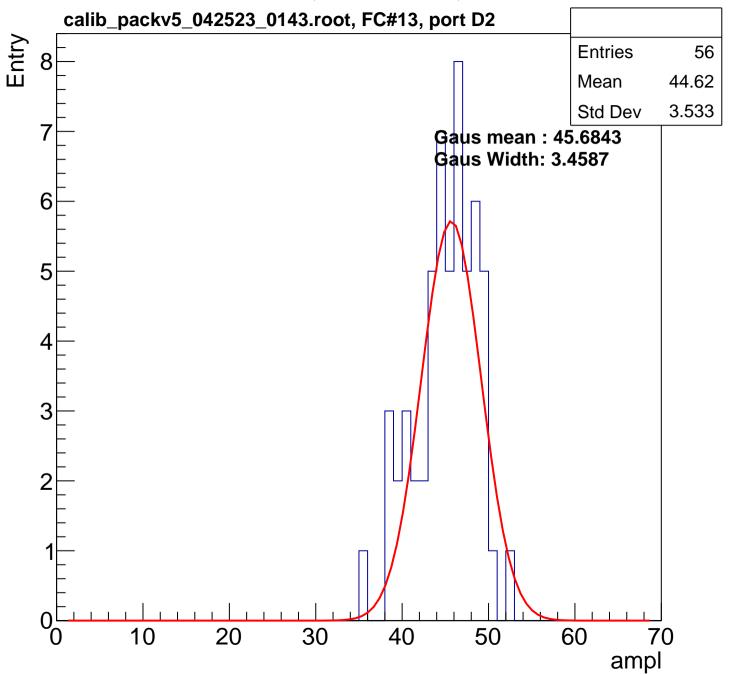


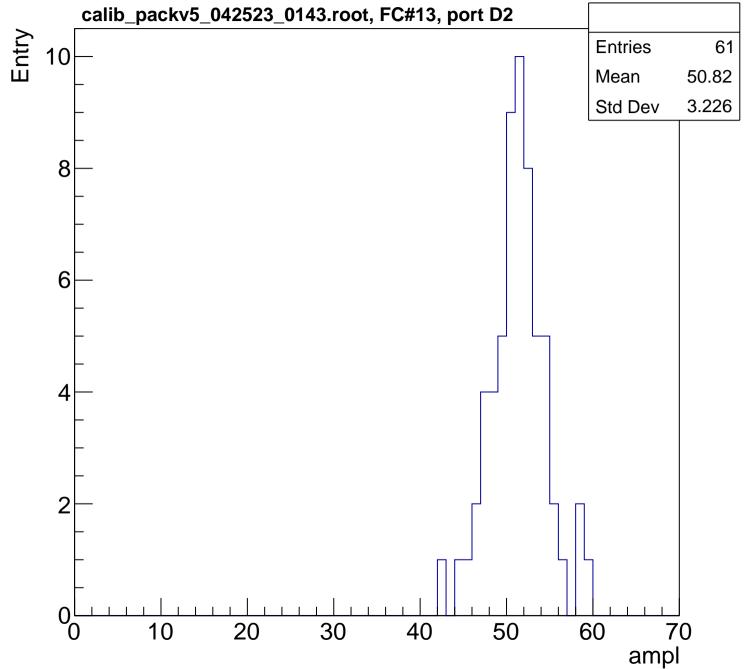


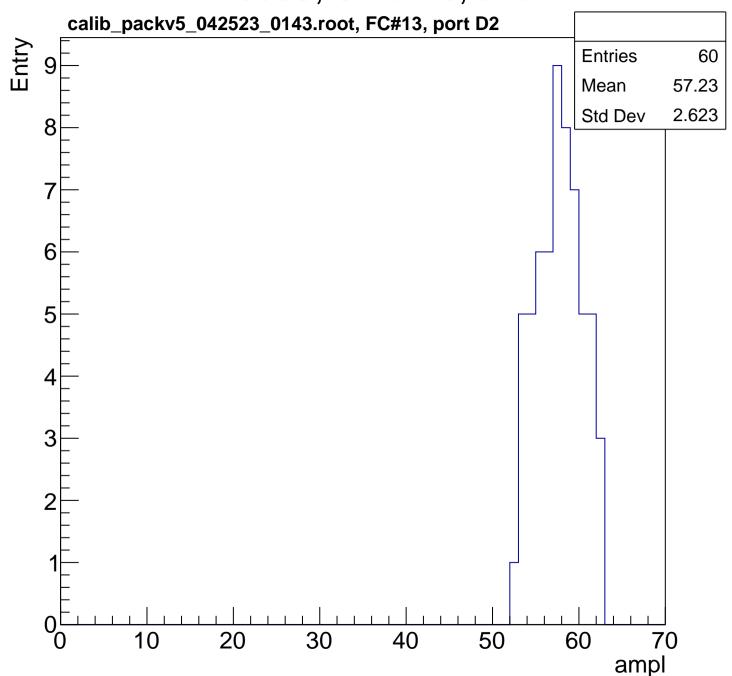
B1L003S, U7-ch72, adc7 calib_packv5_042523_0143.root, FC#13, port D2 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

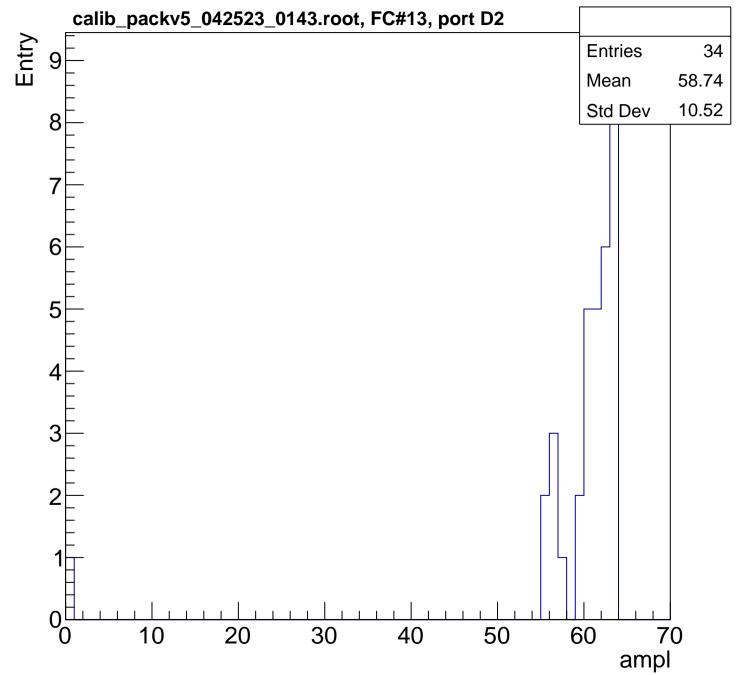


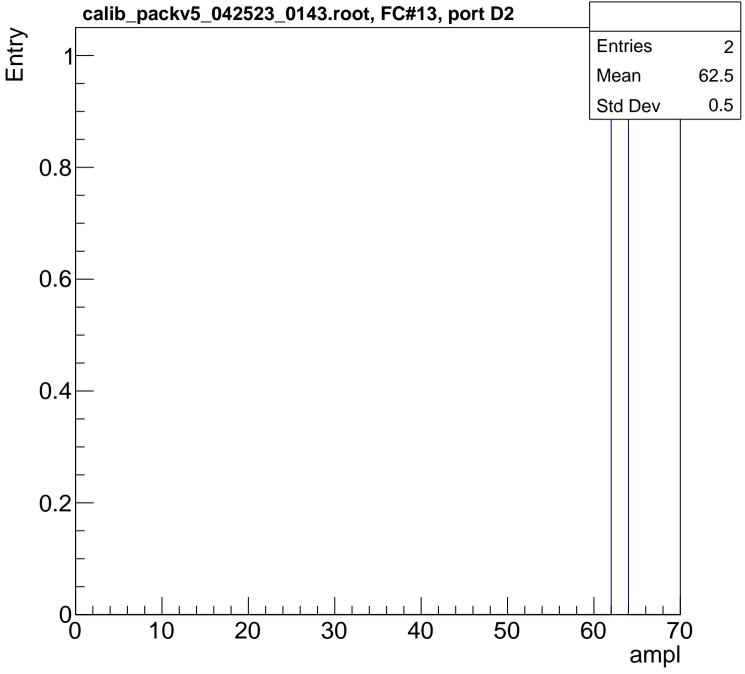




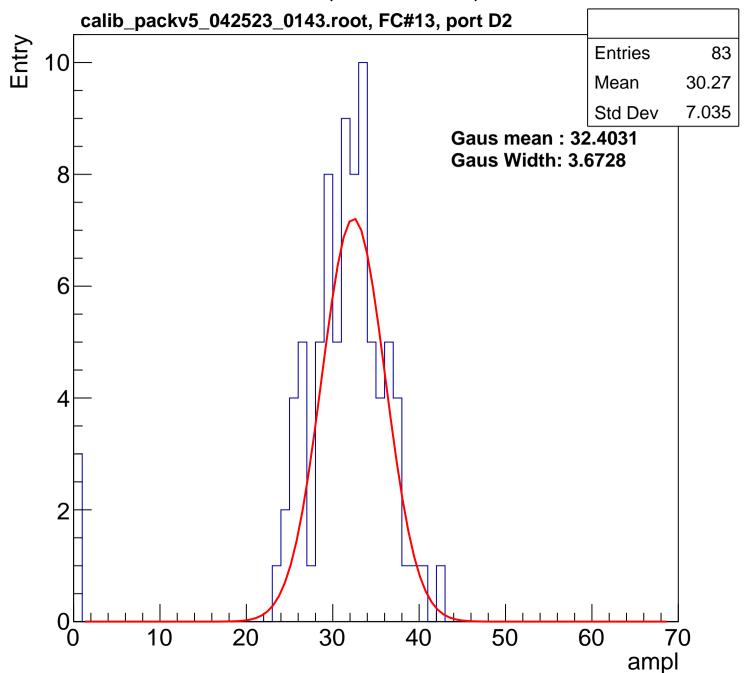


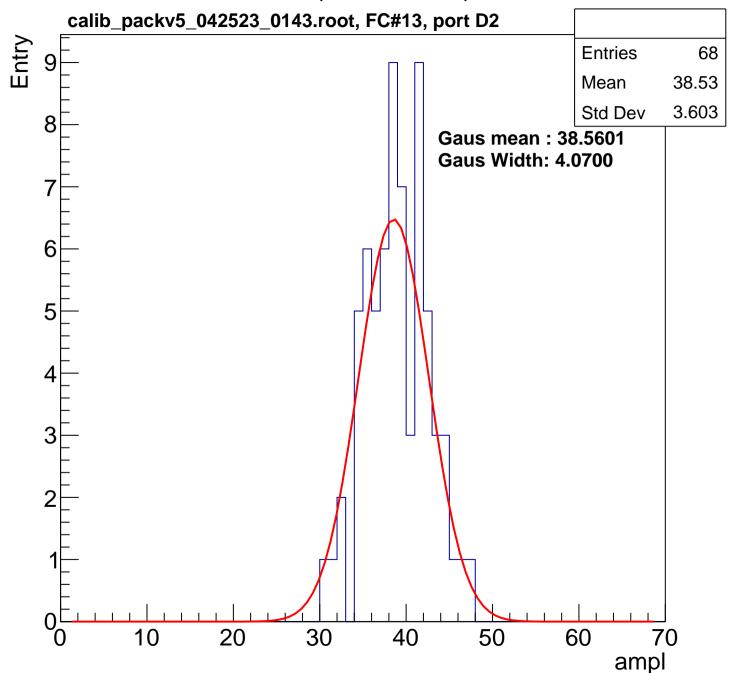


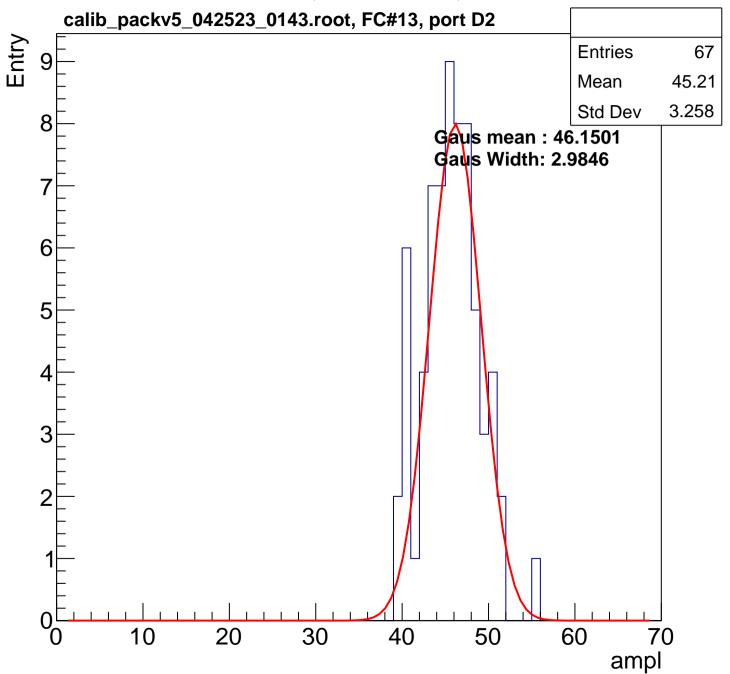


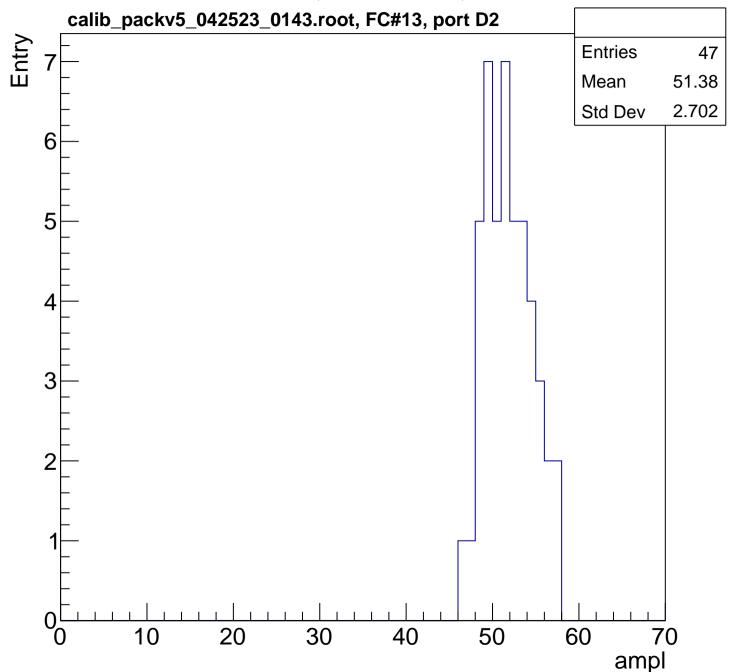


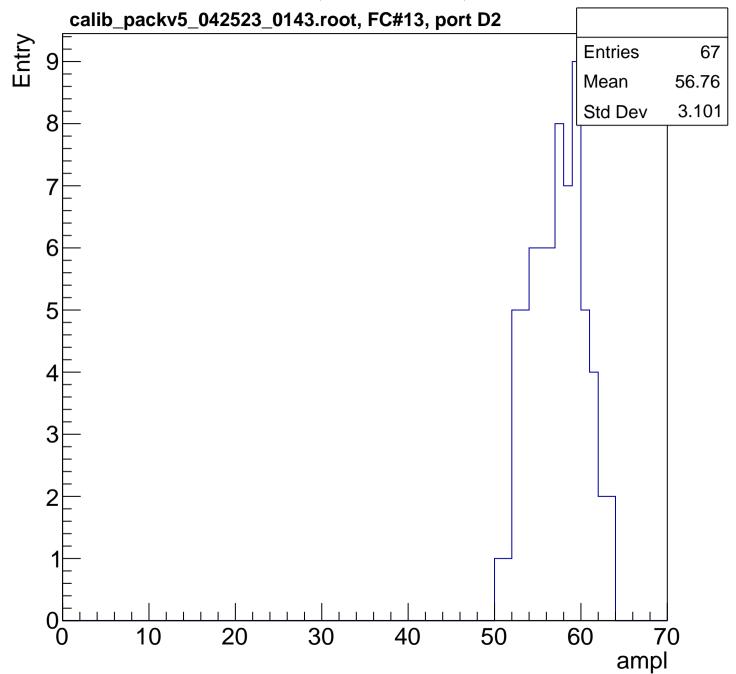


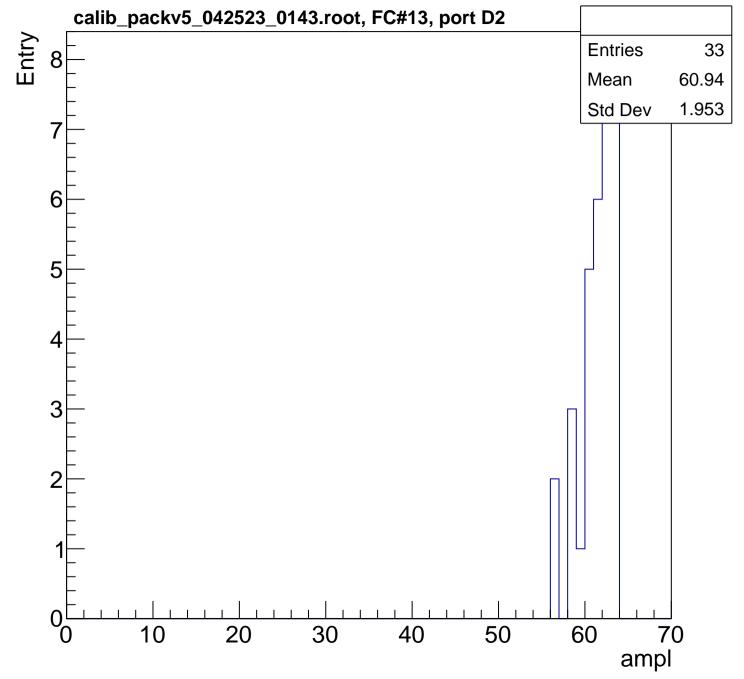




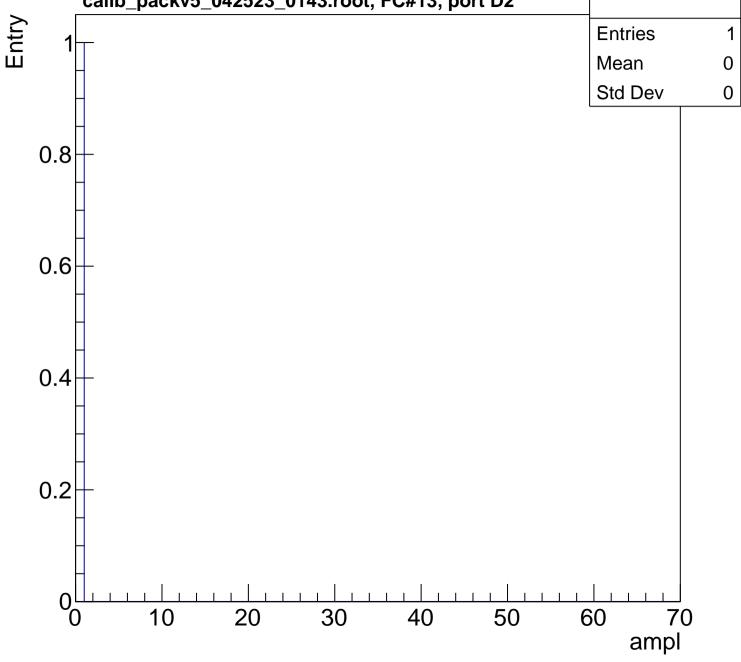




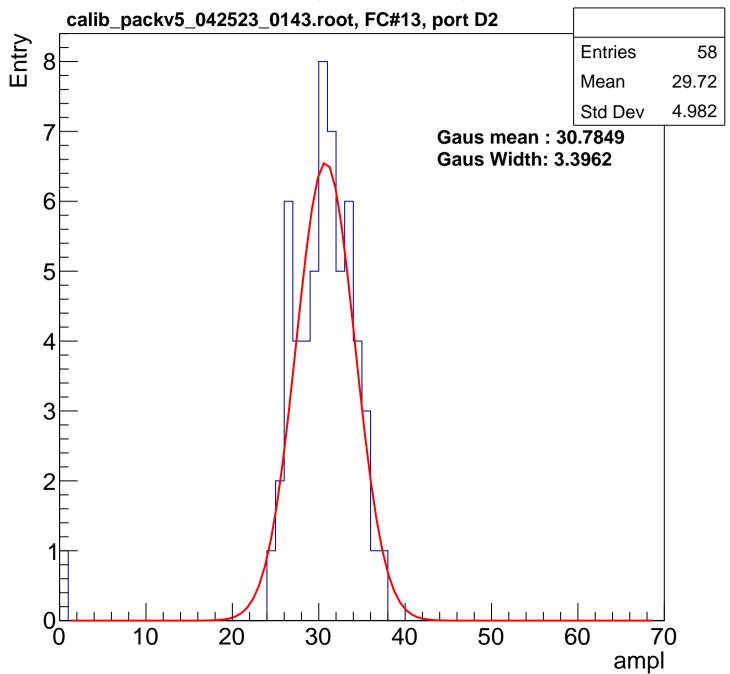


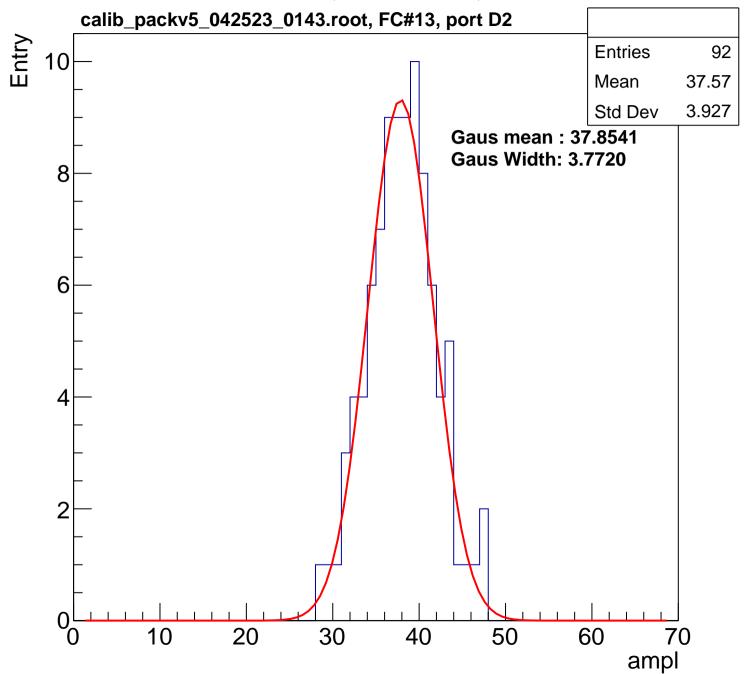


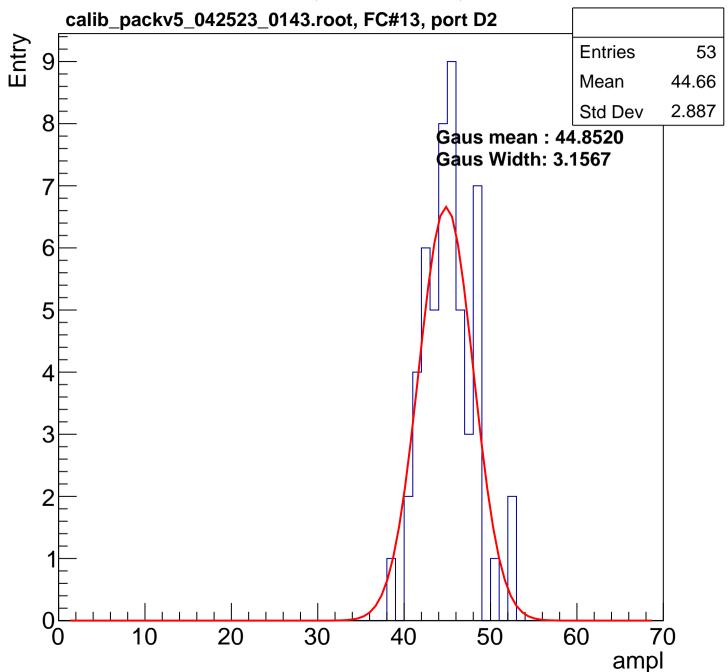
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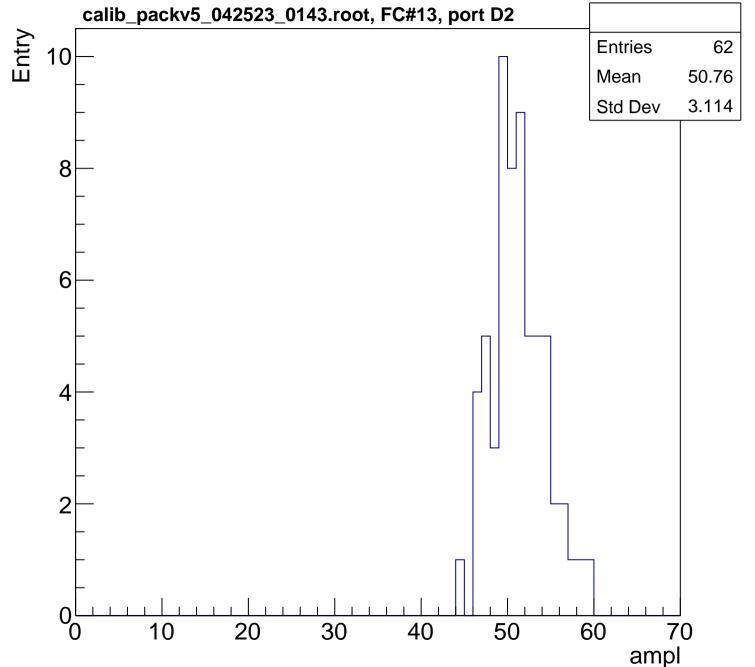


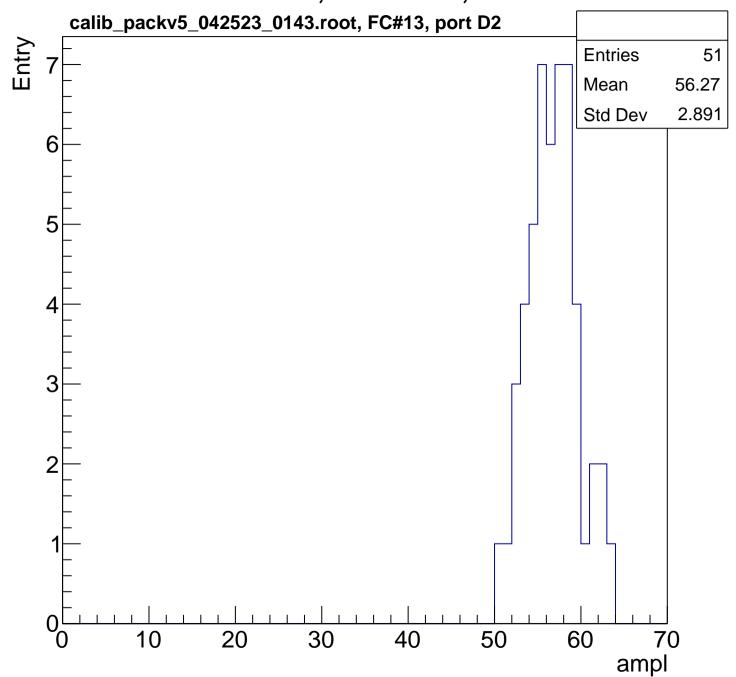
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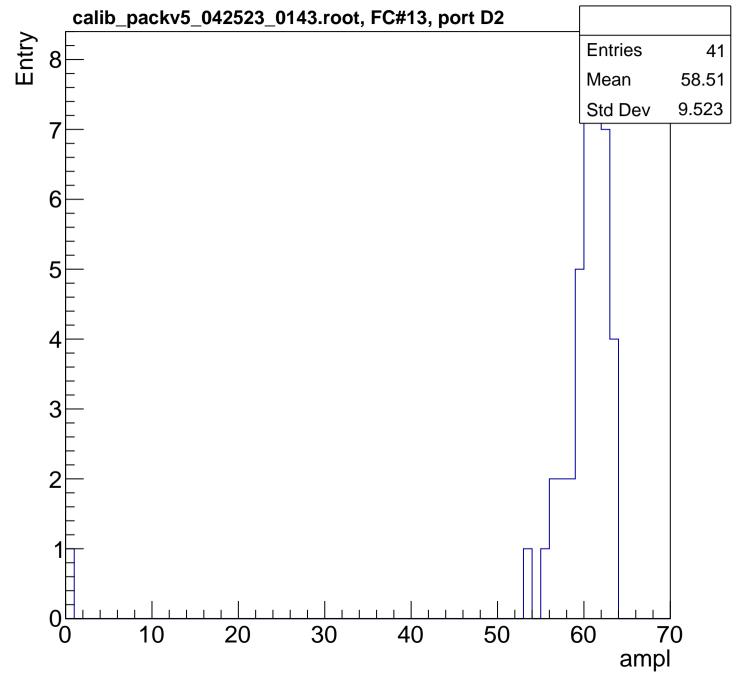


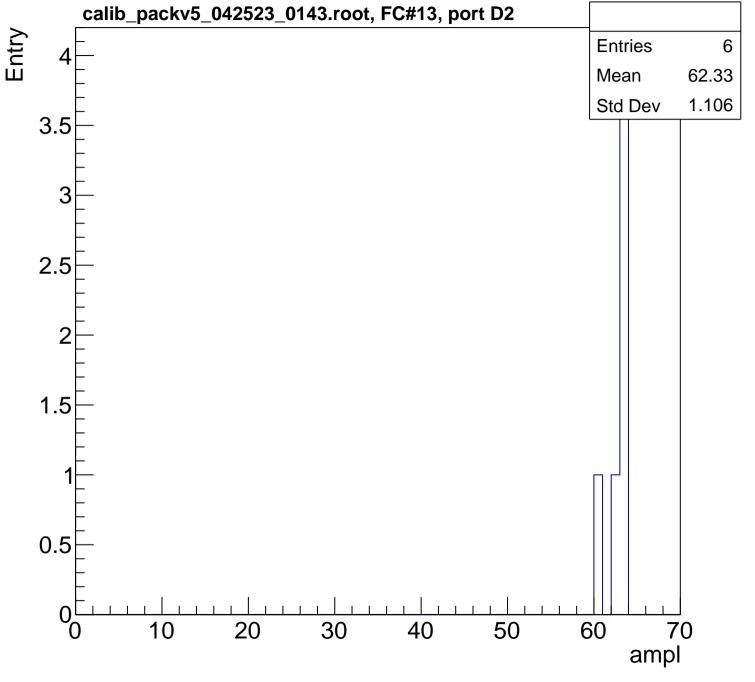


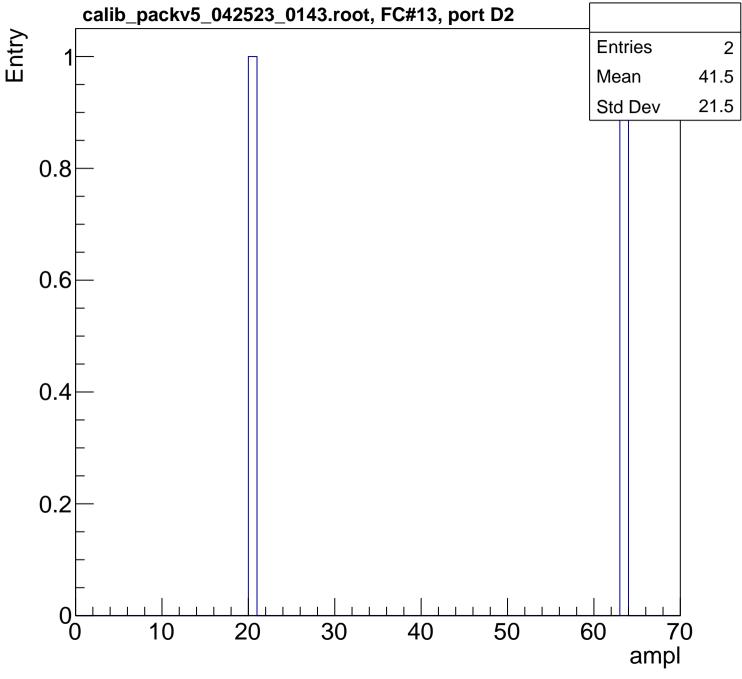


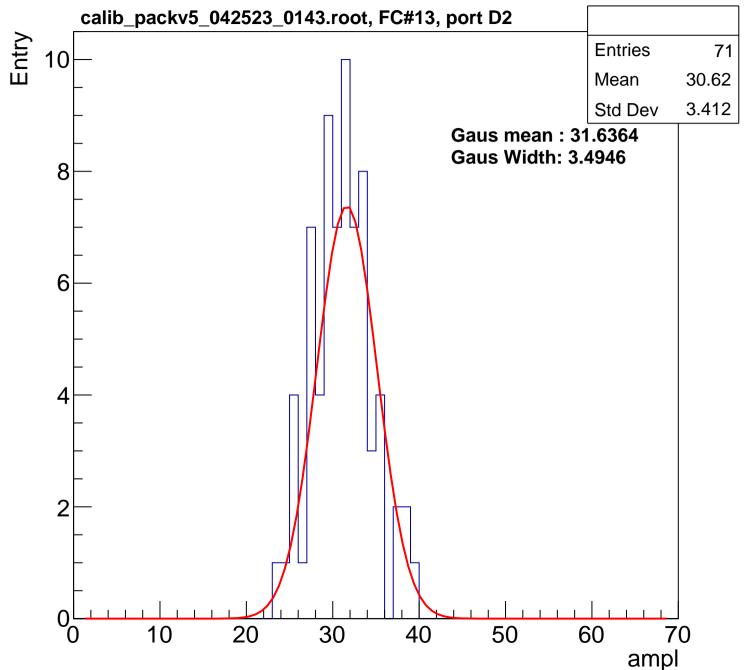


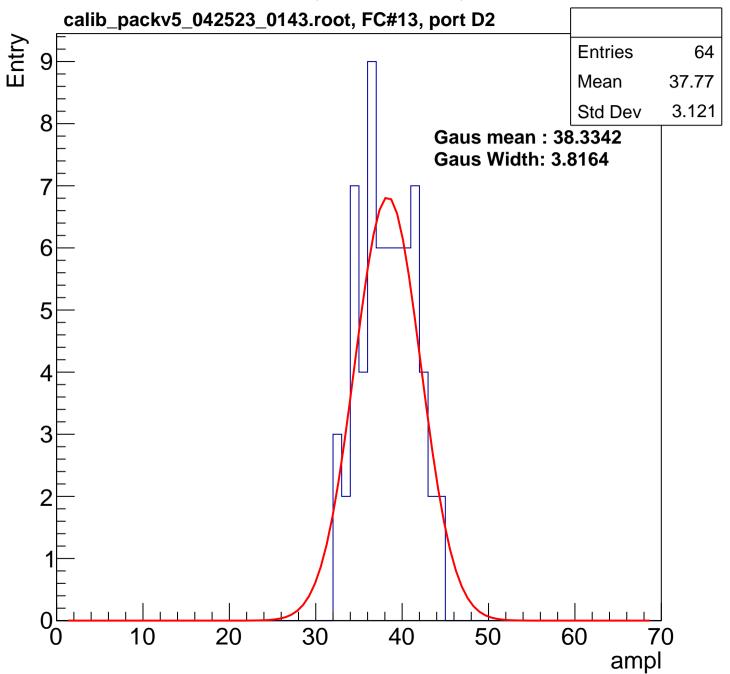


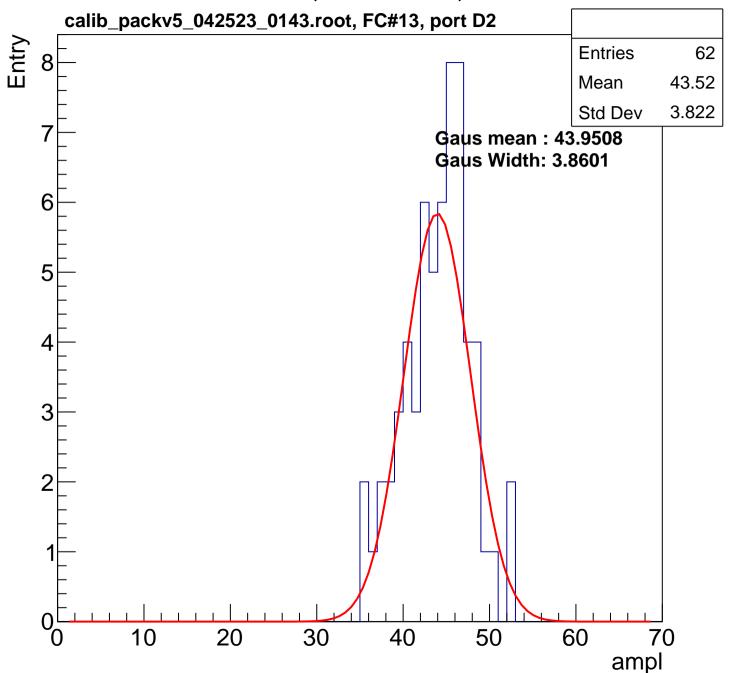


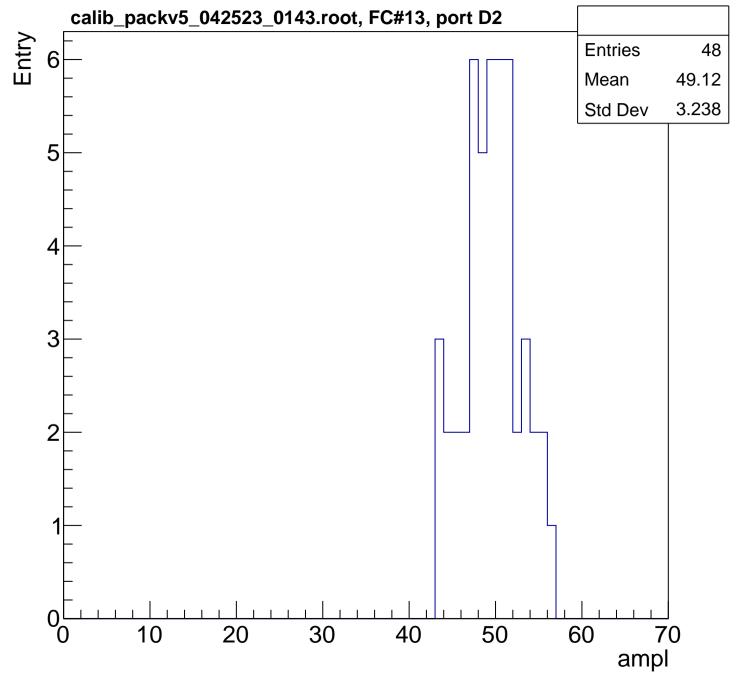


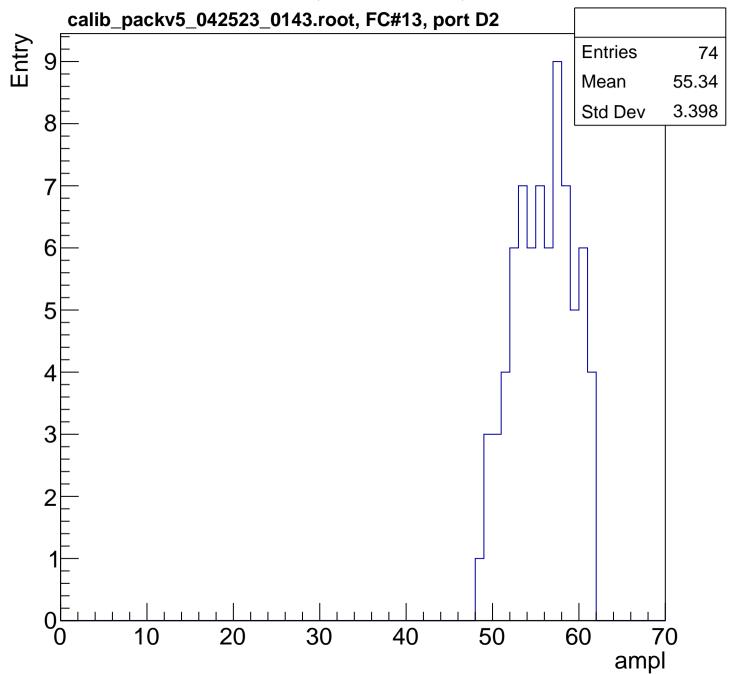


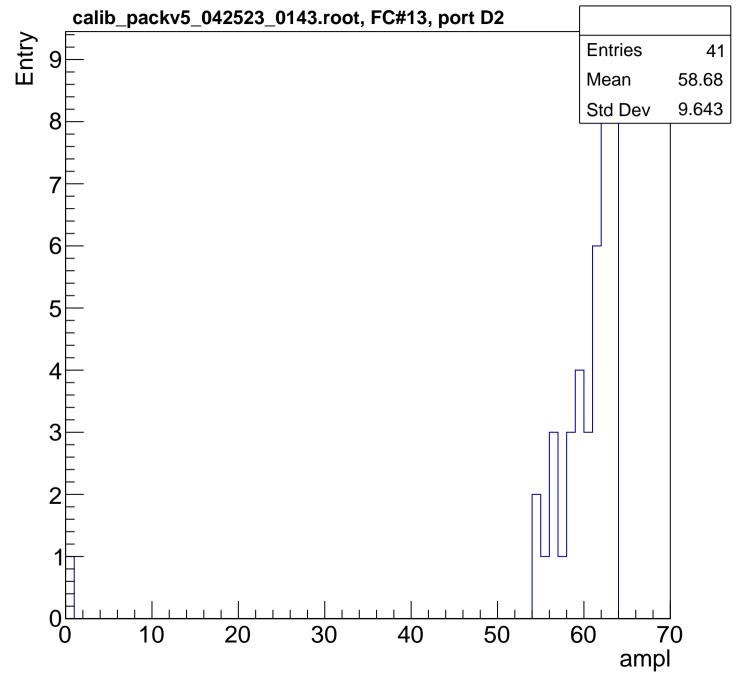


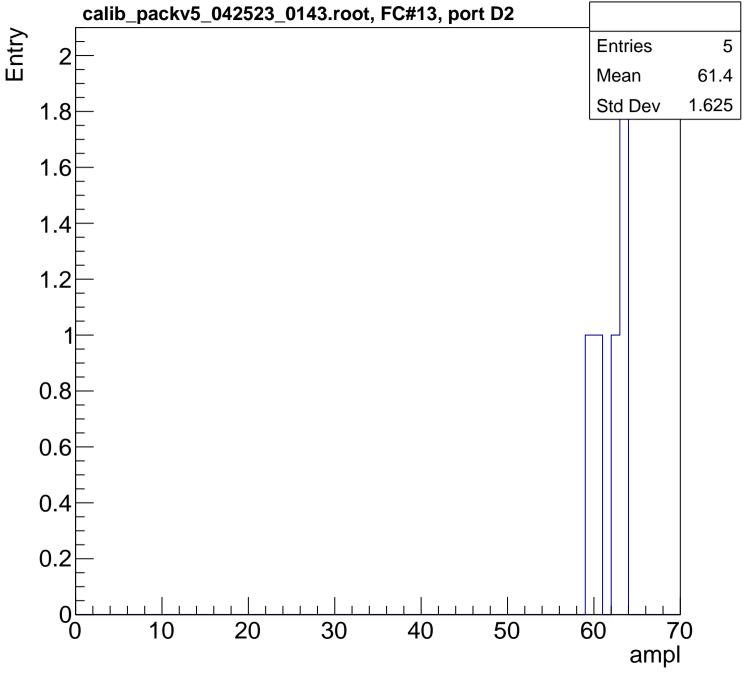




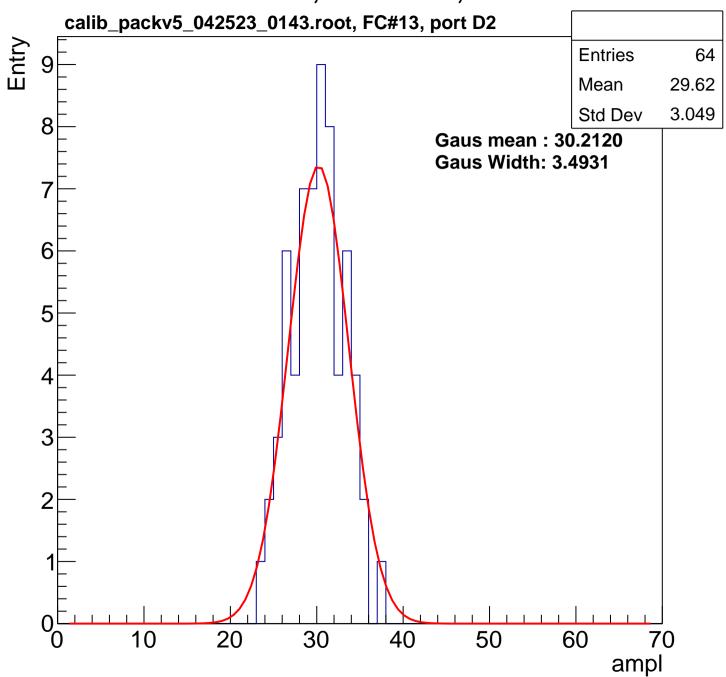


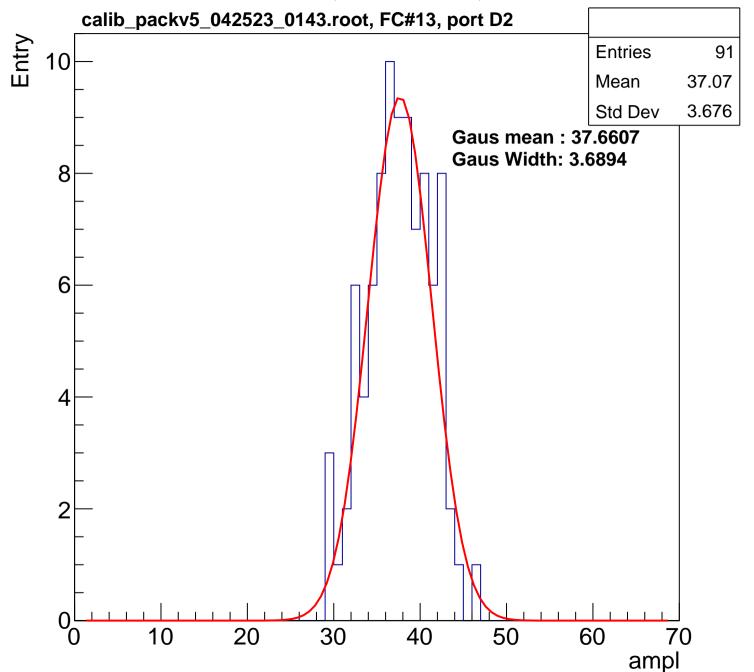


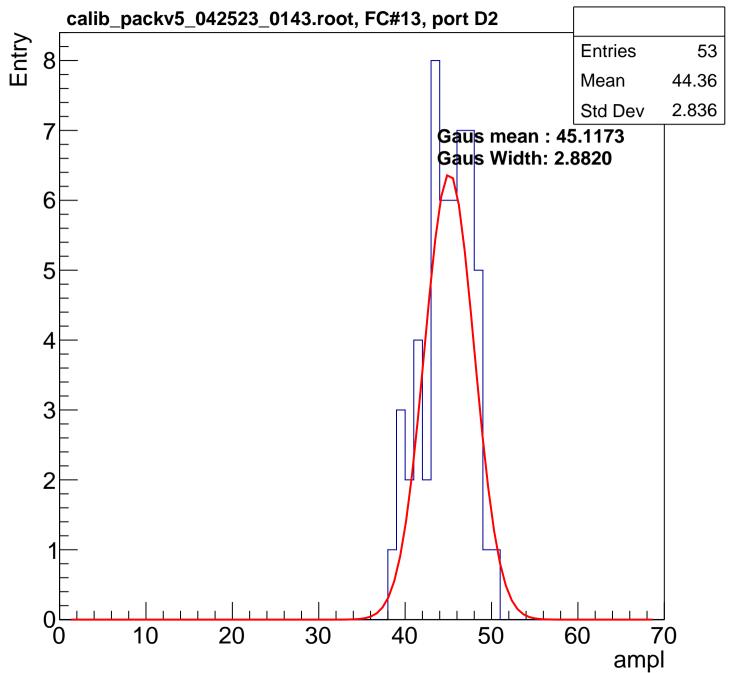


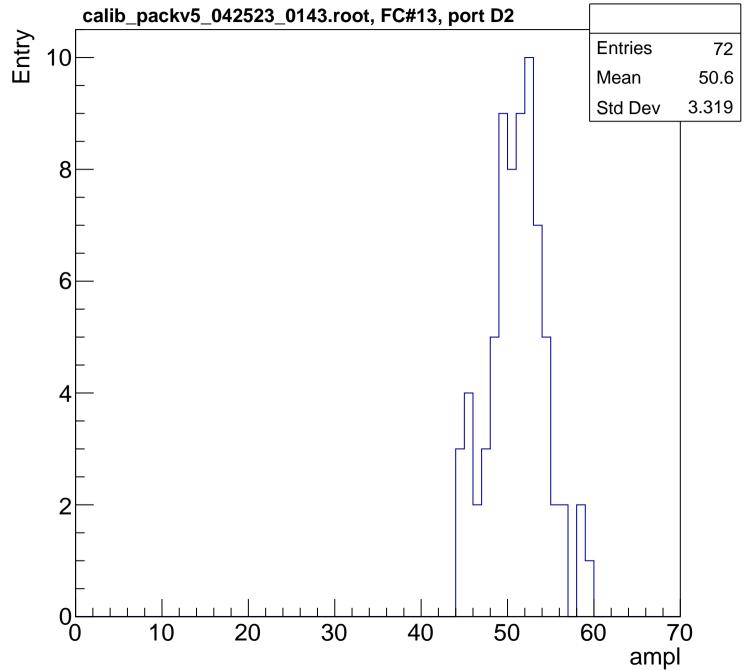


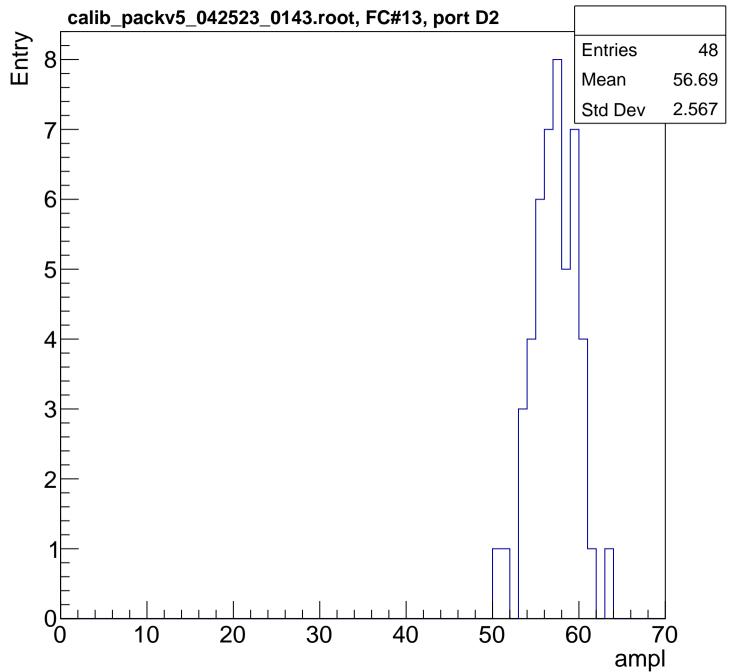


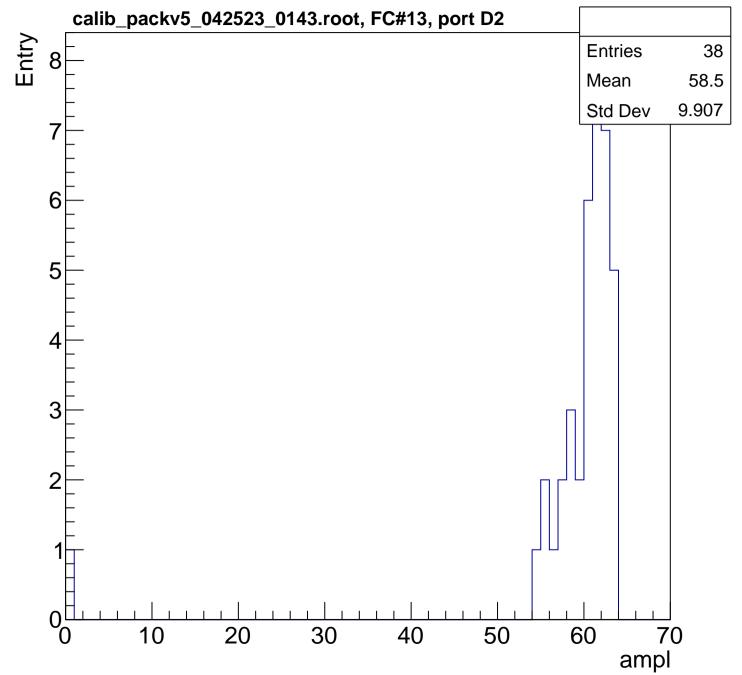


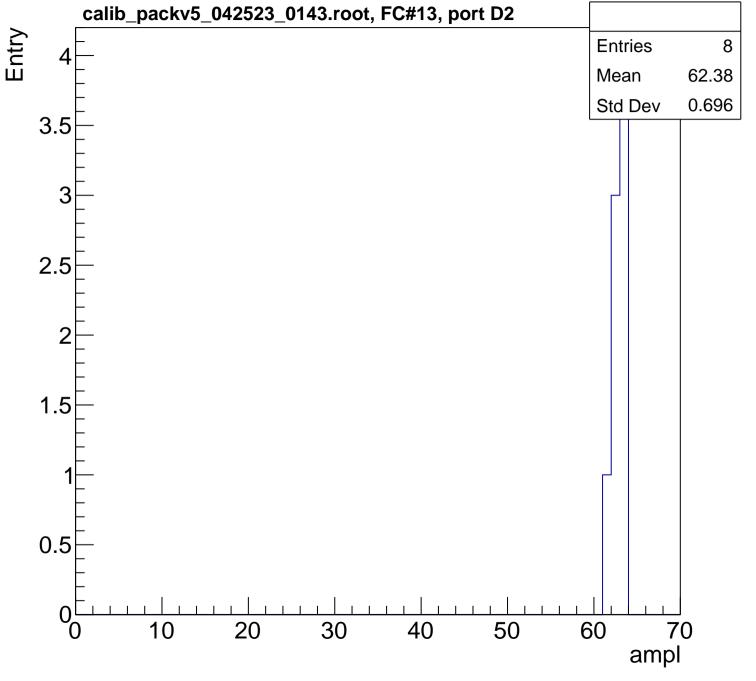


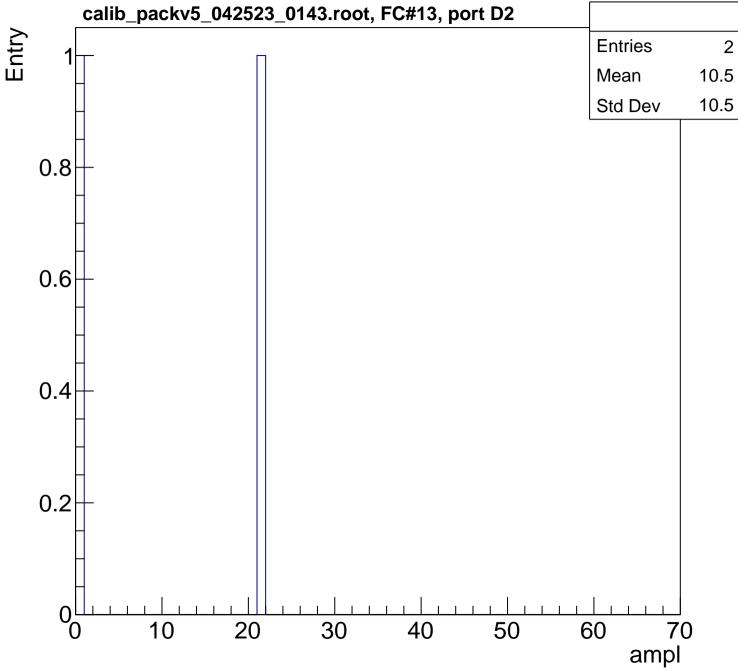


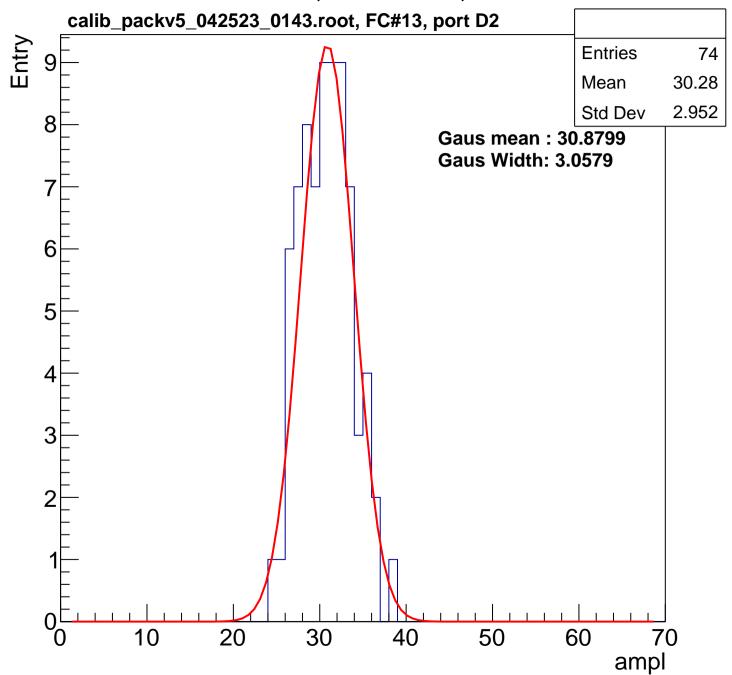


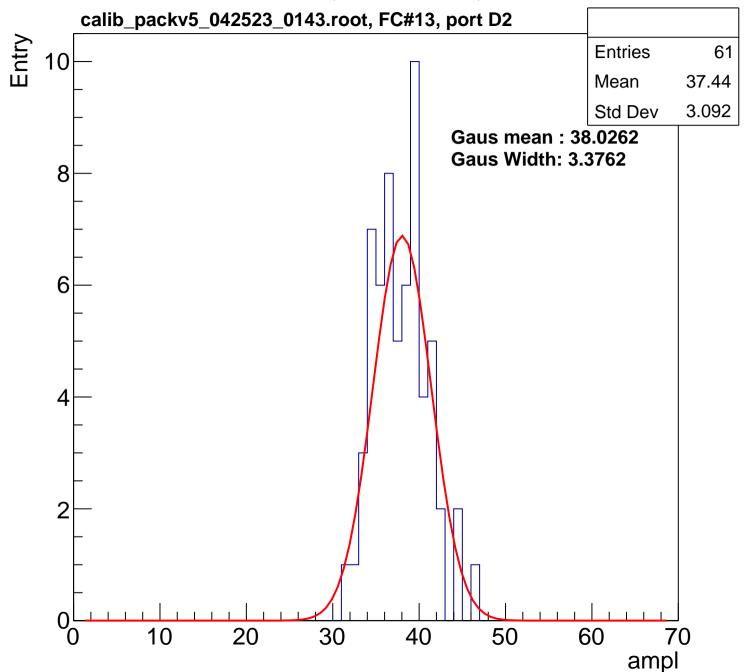


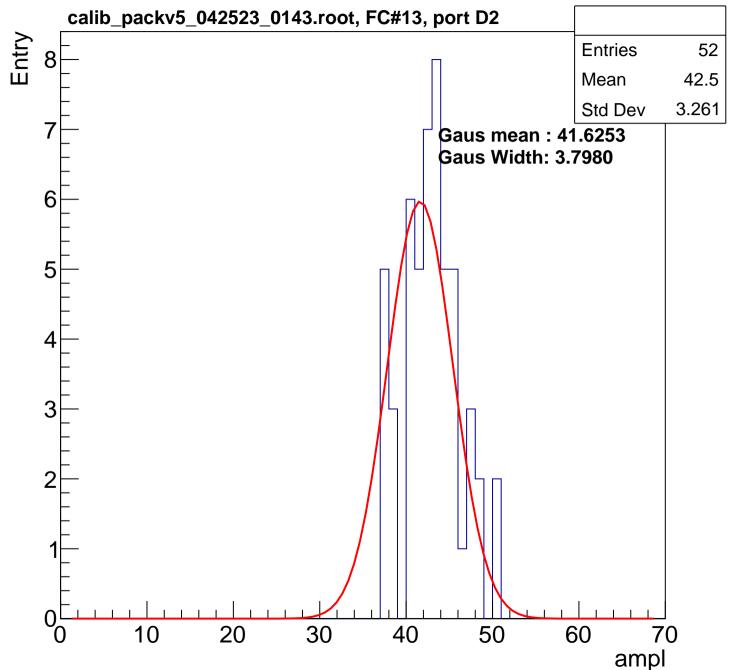


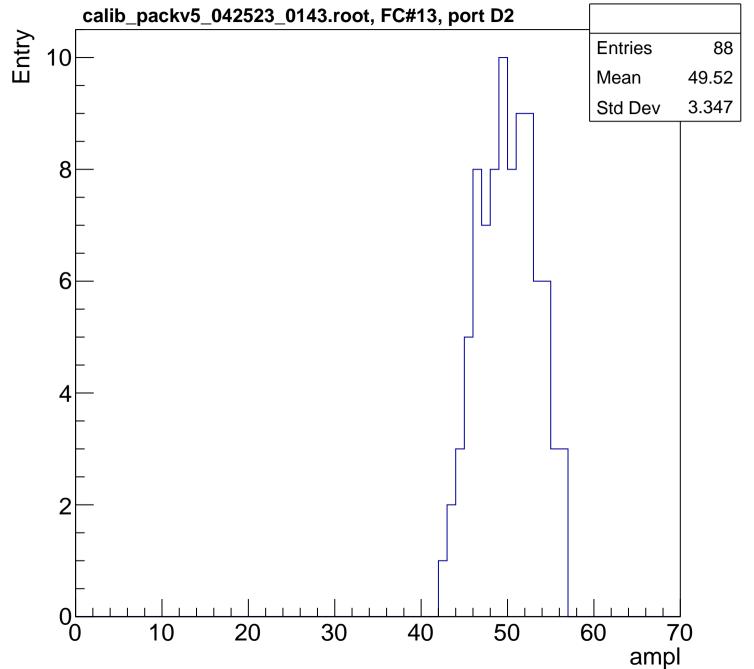


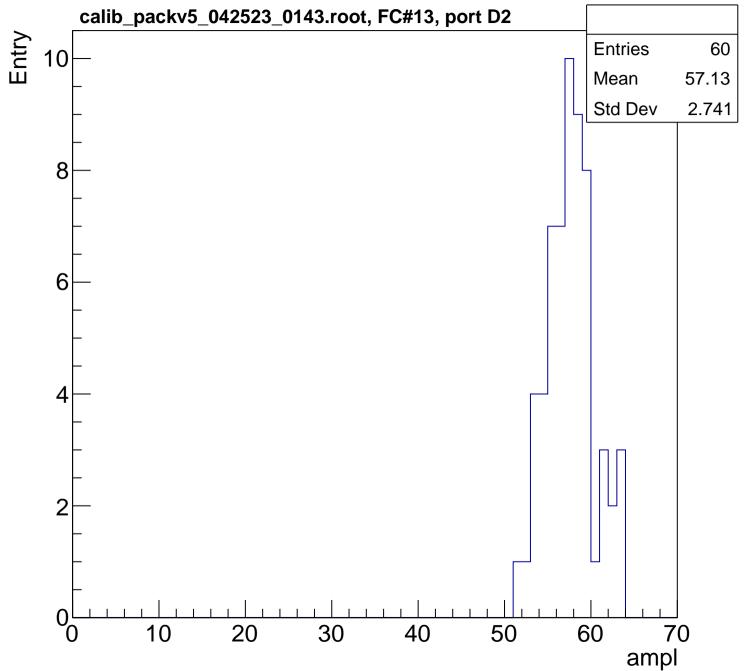


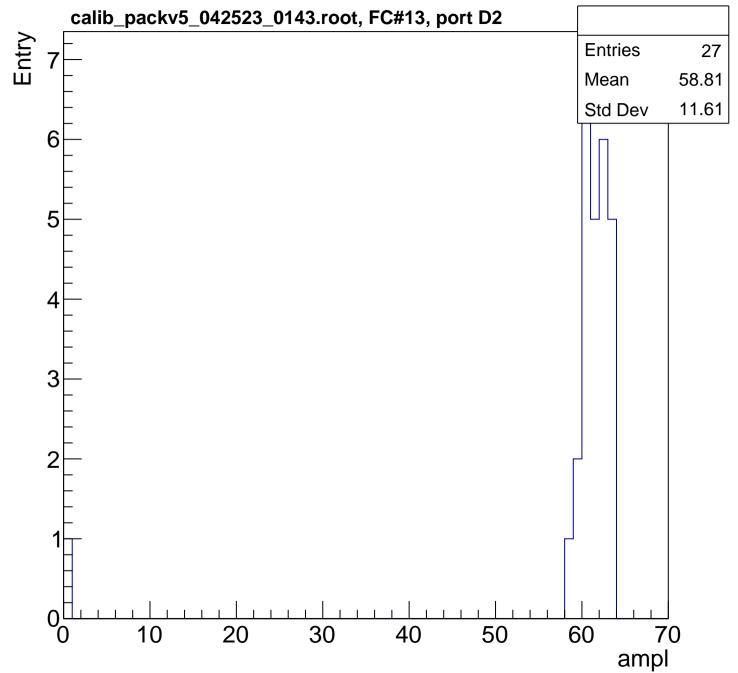


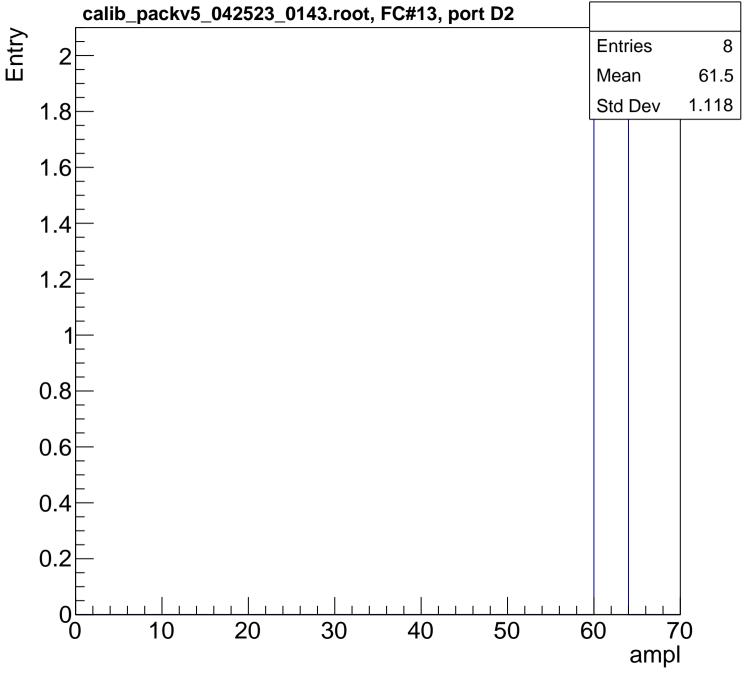




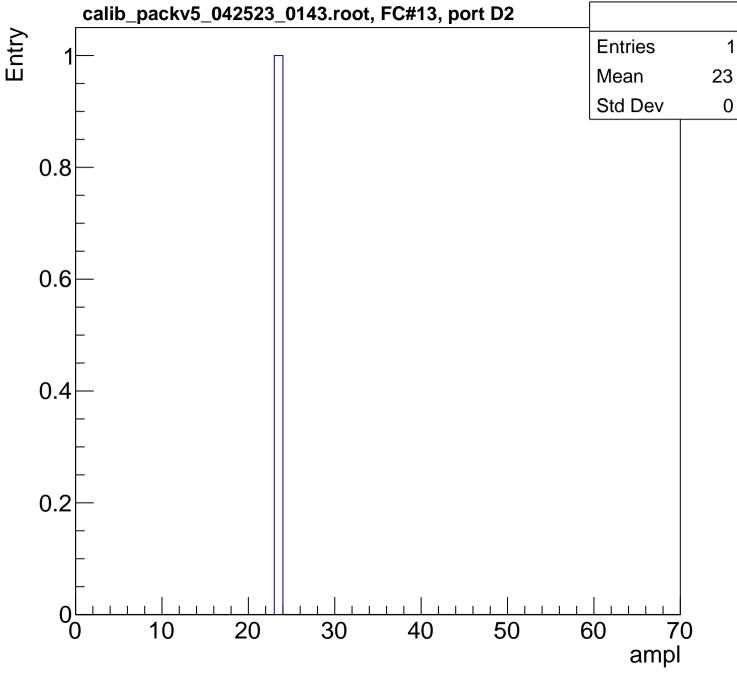


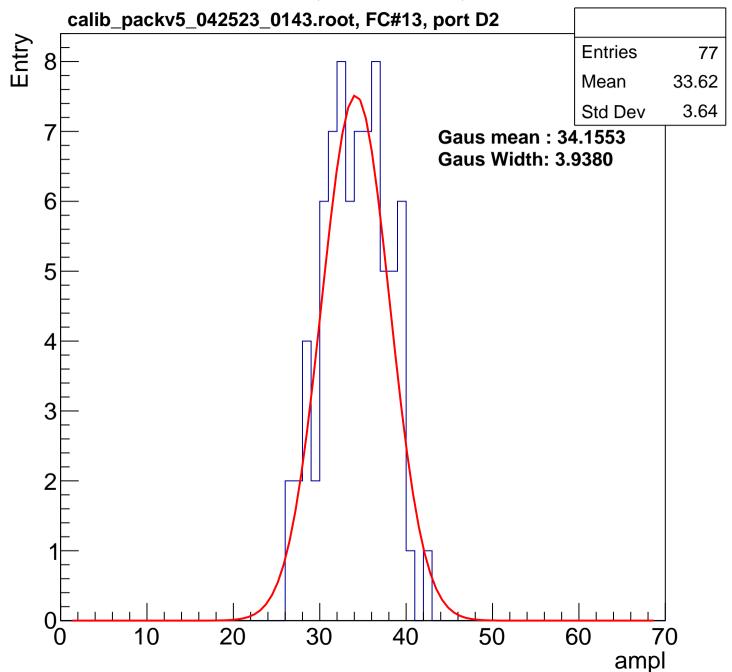


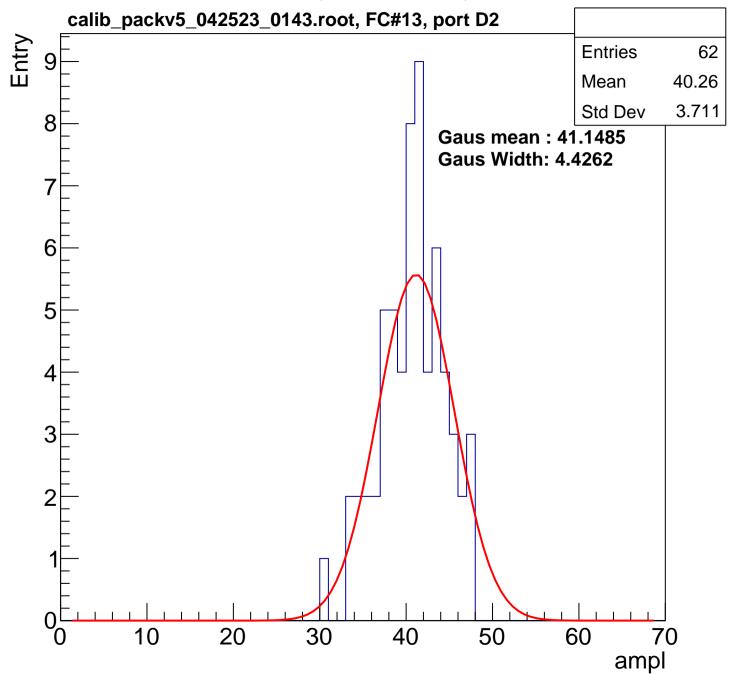


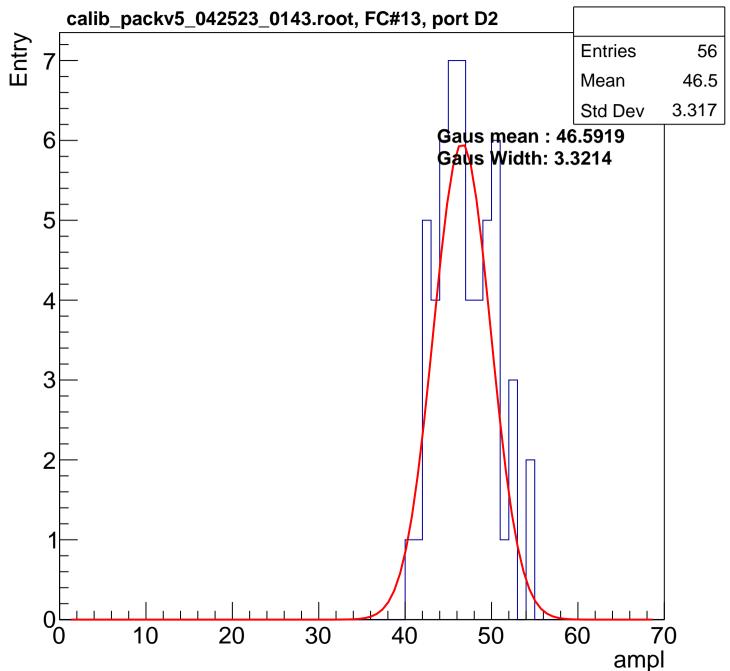


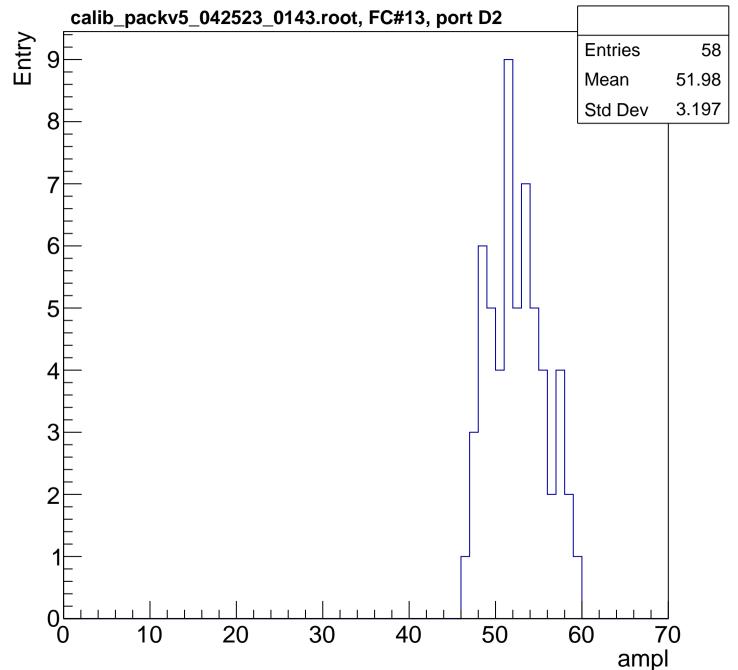
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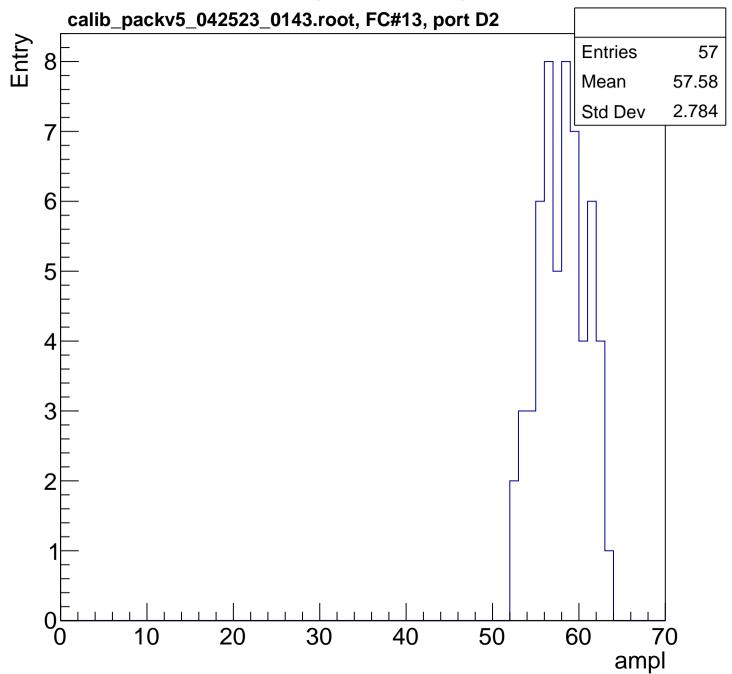


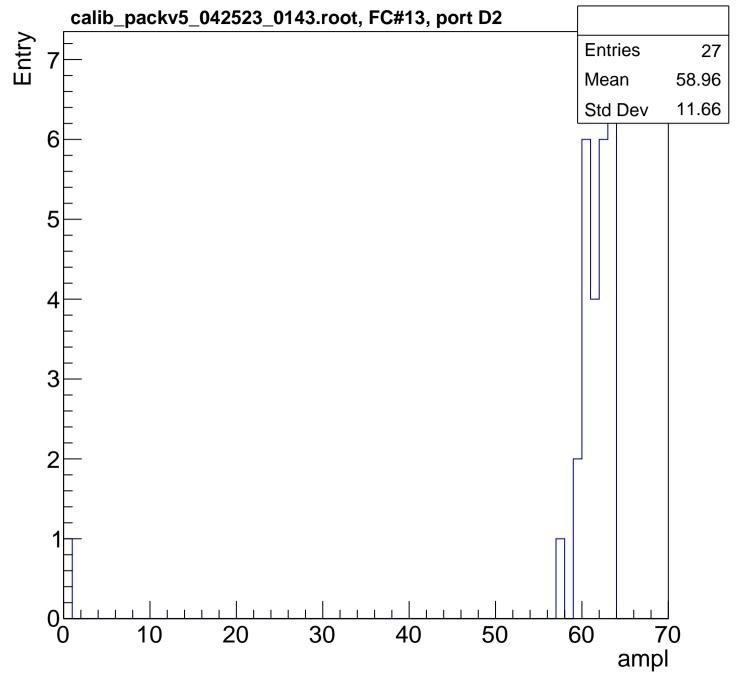


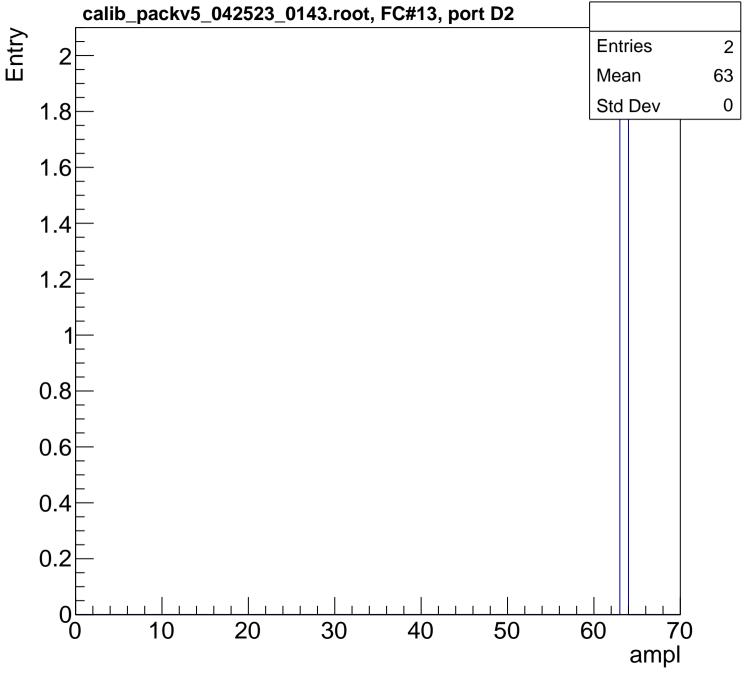




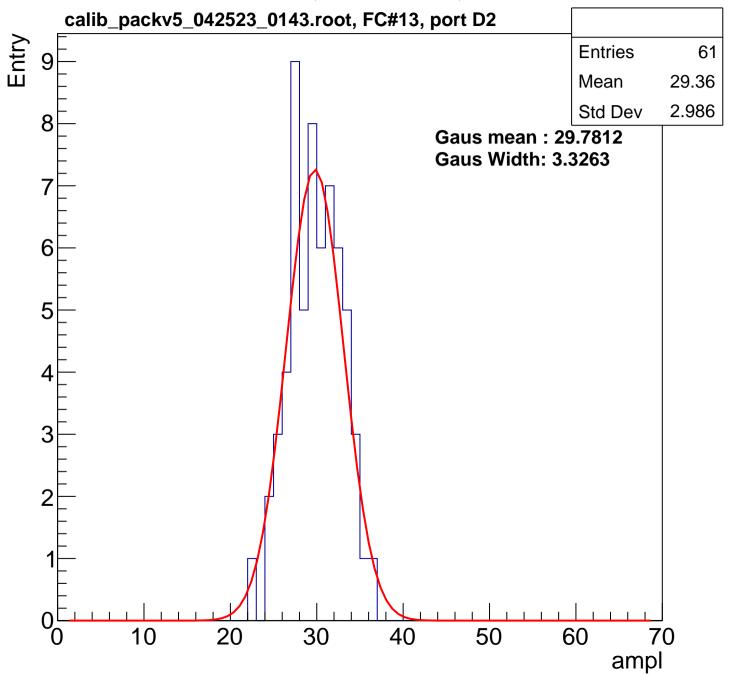


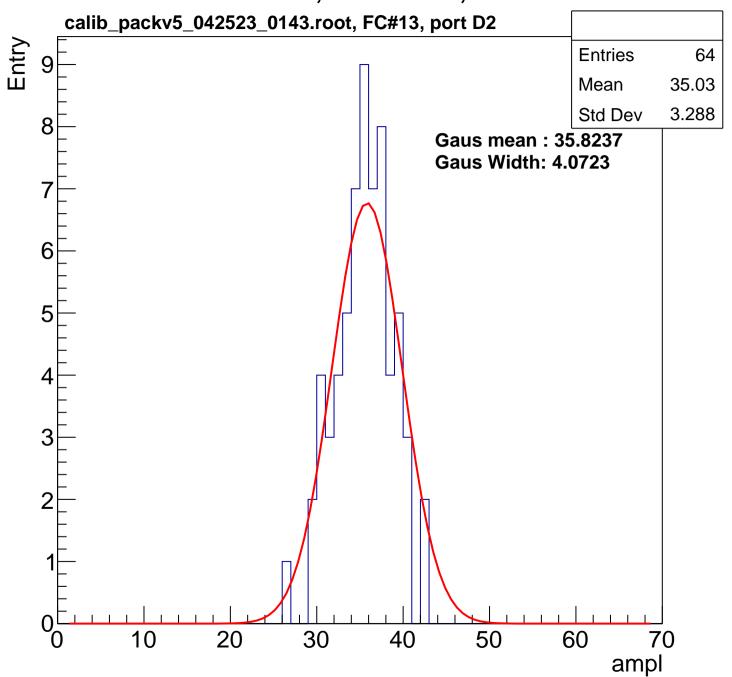


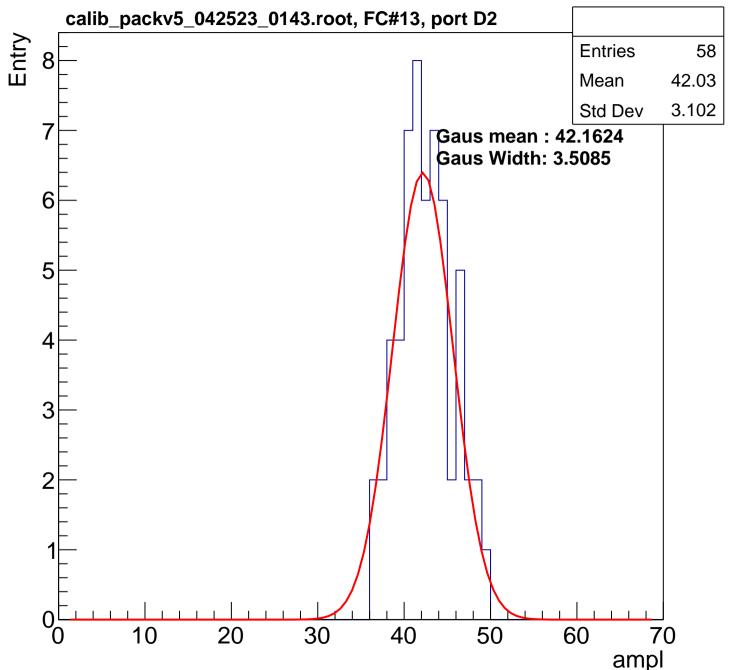


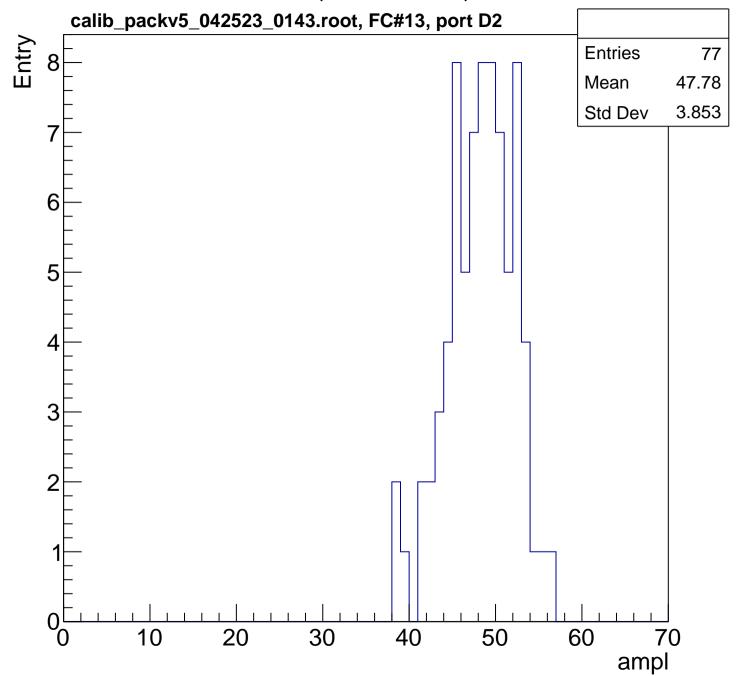


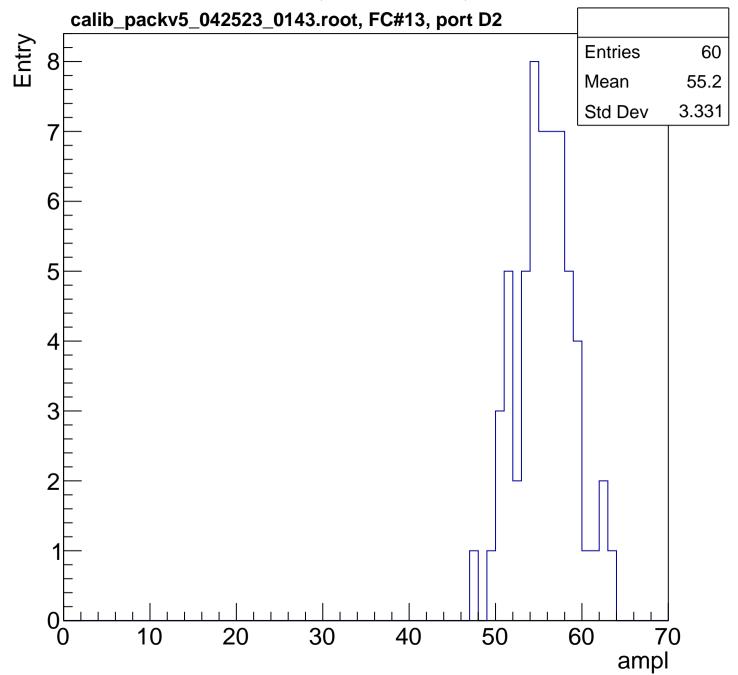


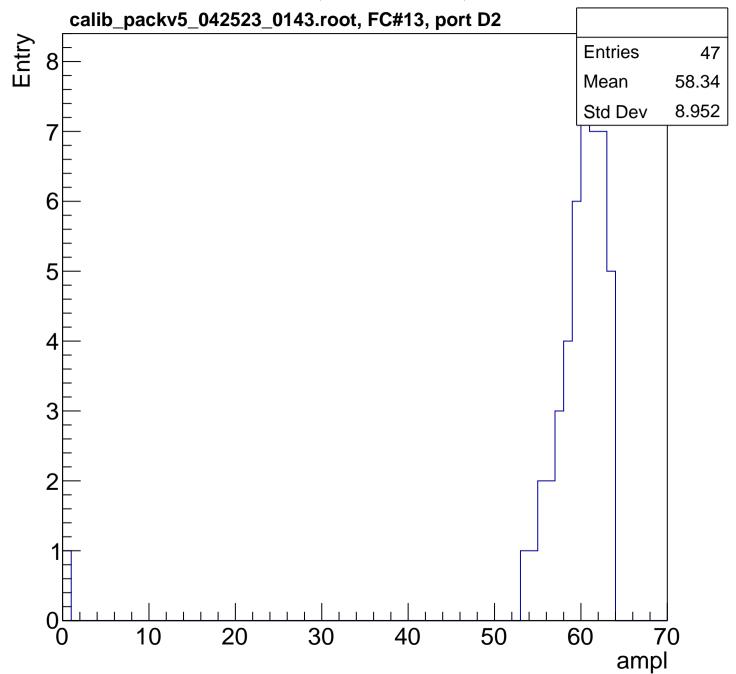


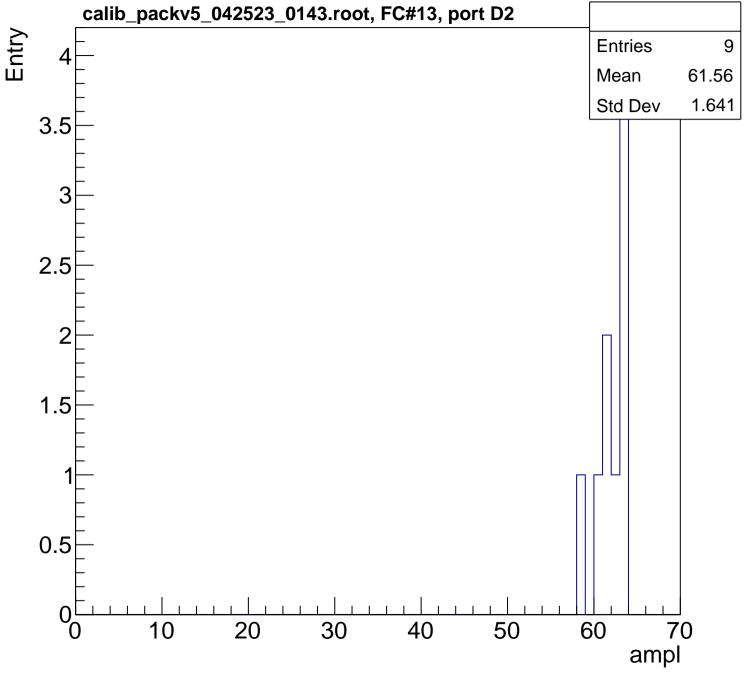


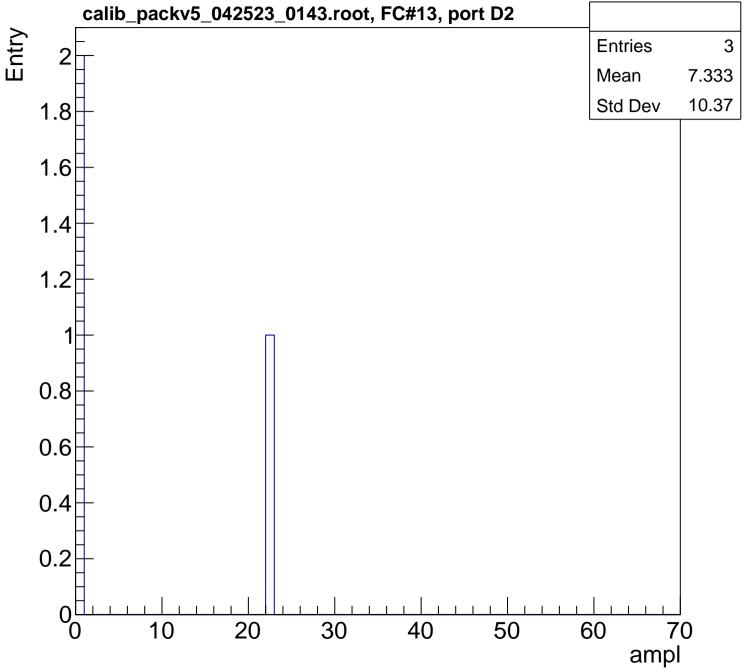


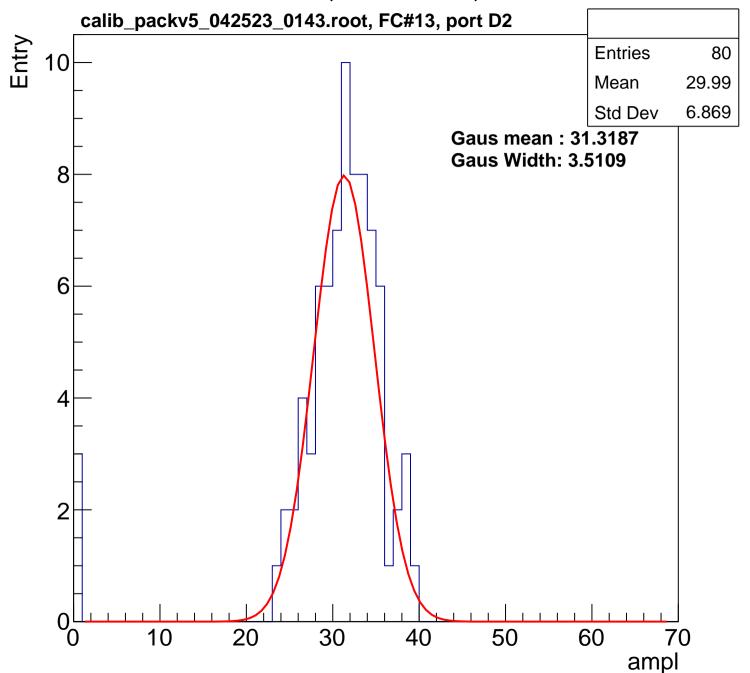


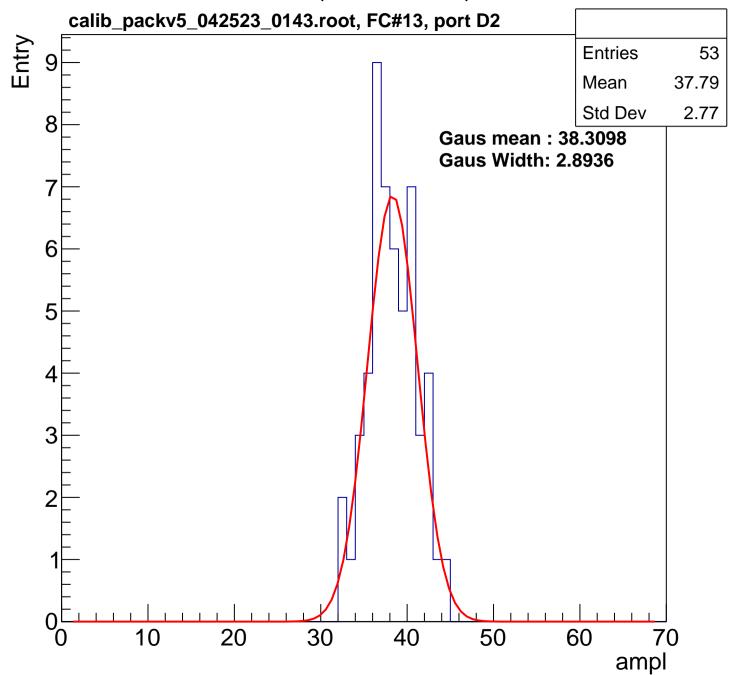


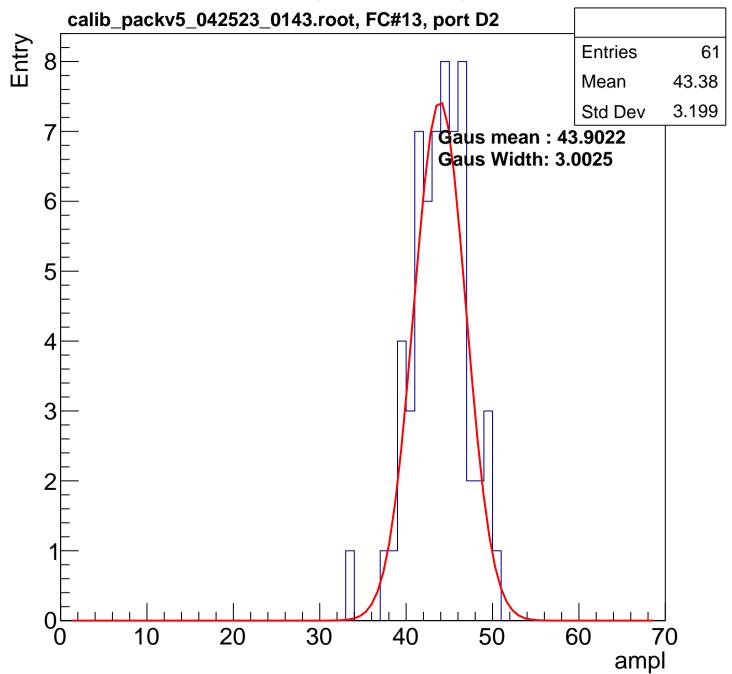


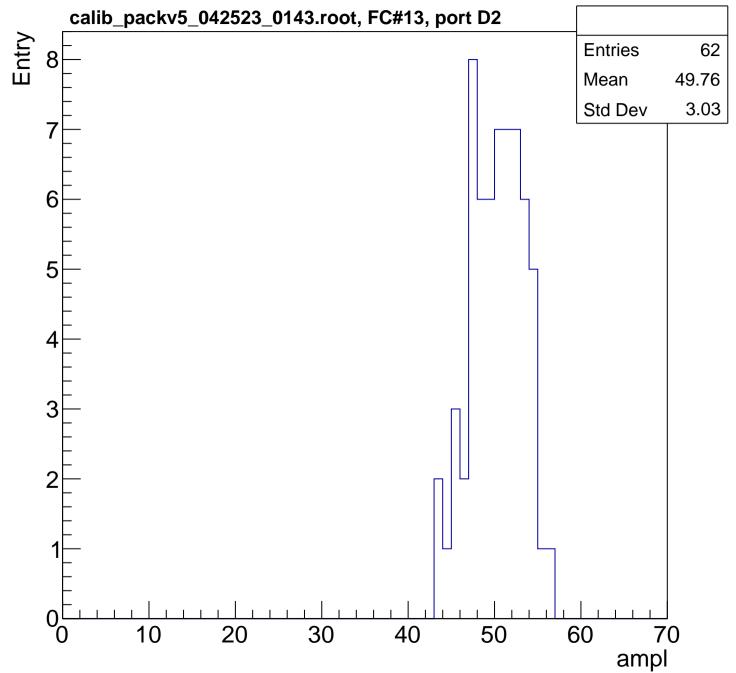


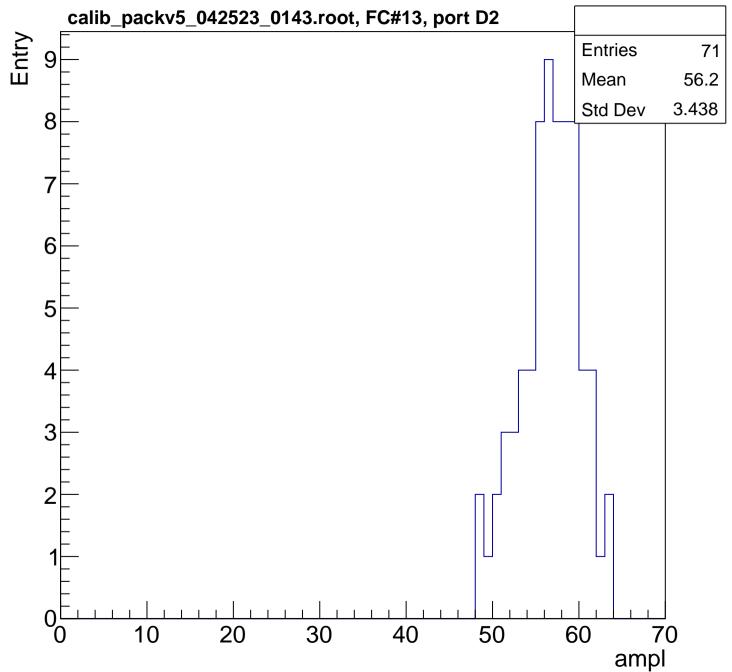


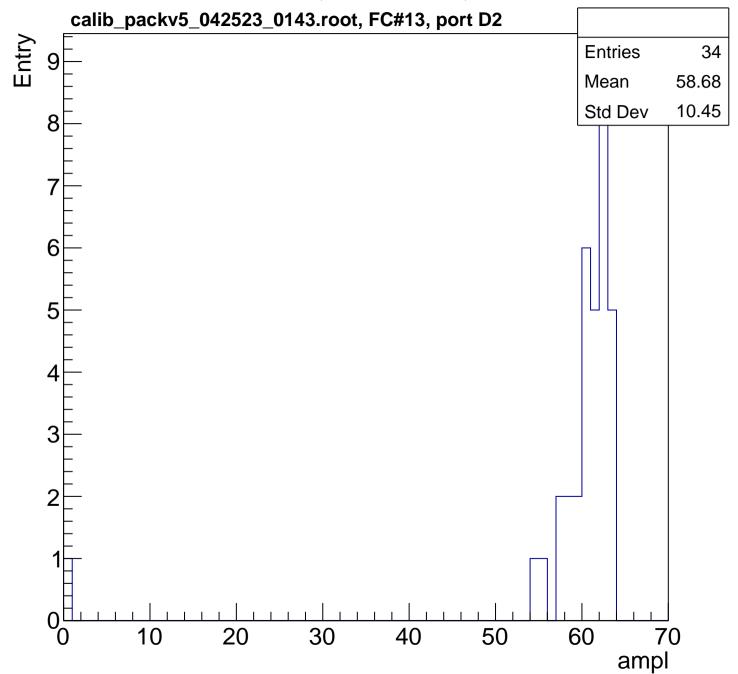


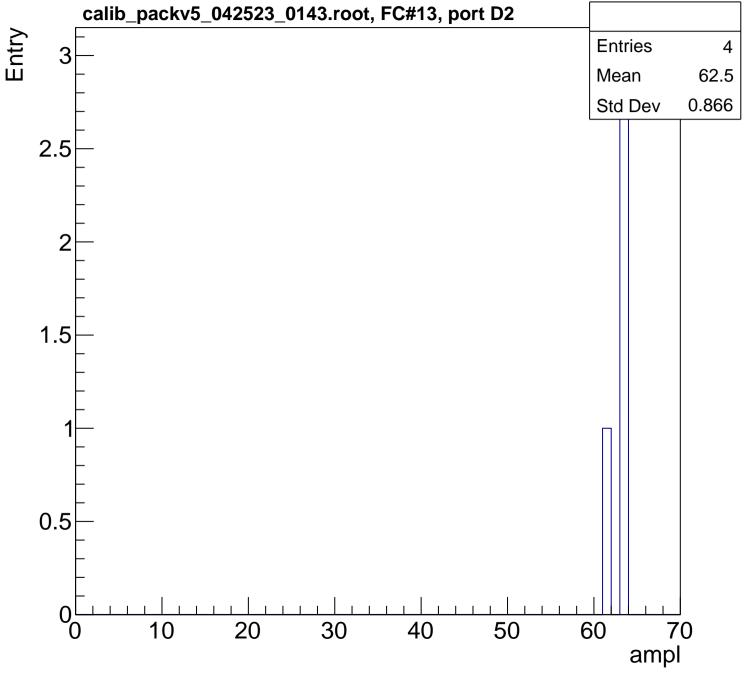


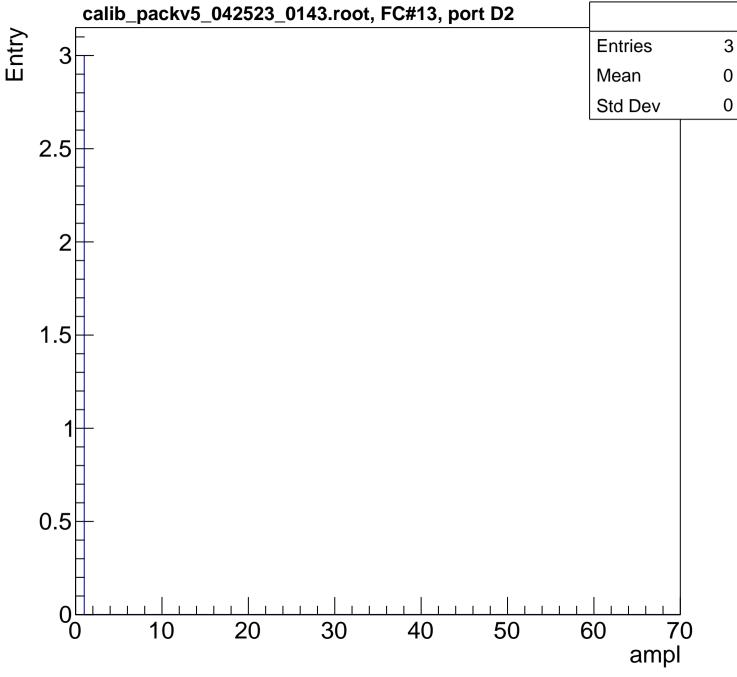


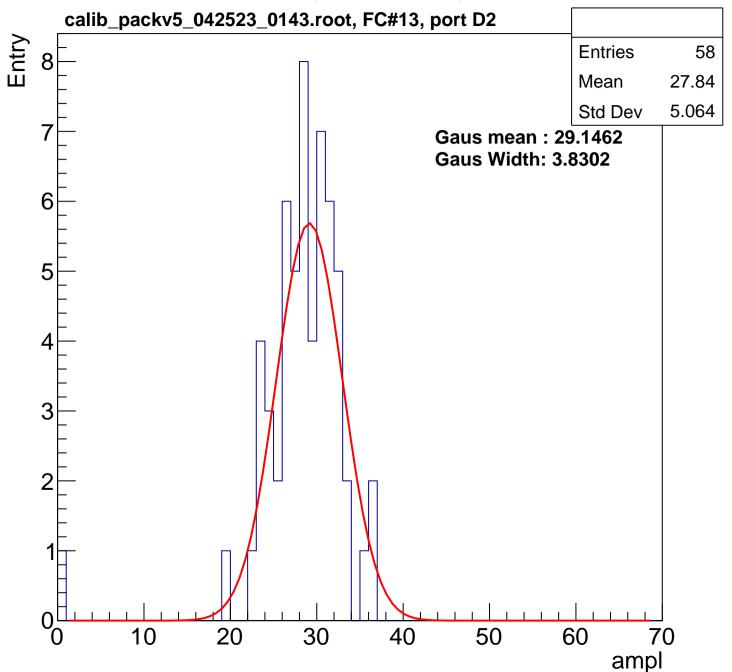


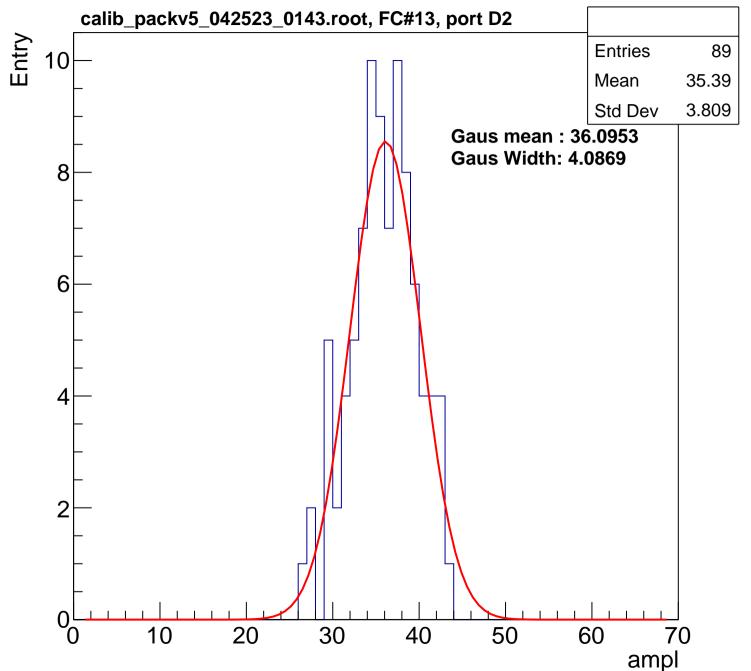


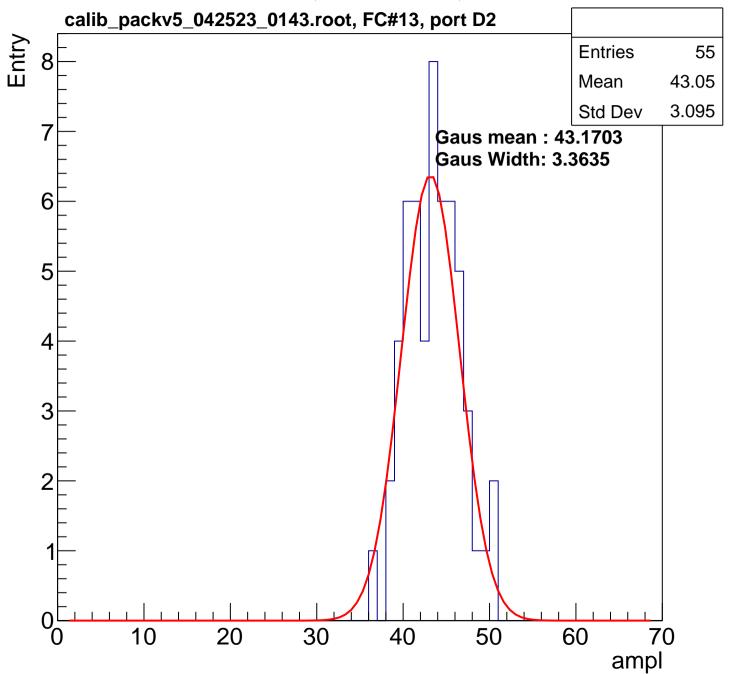


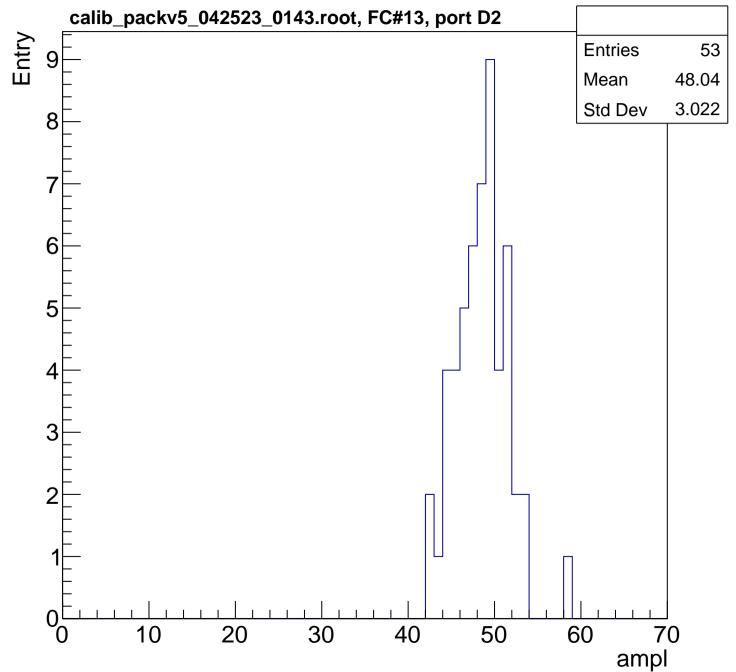


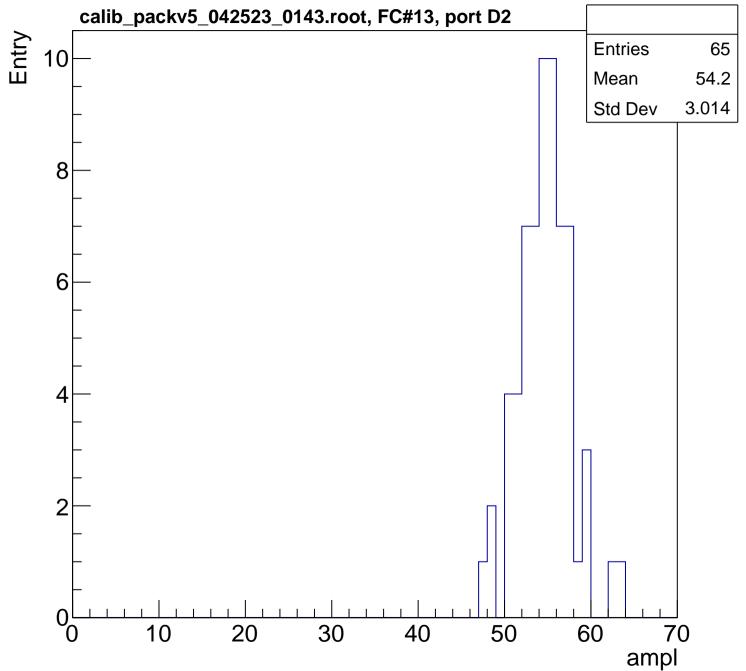


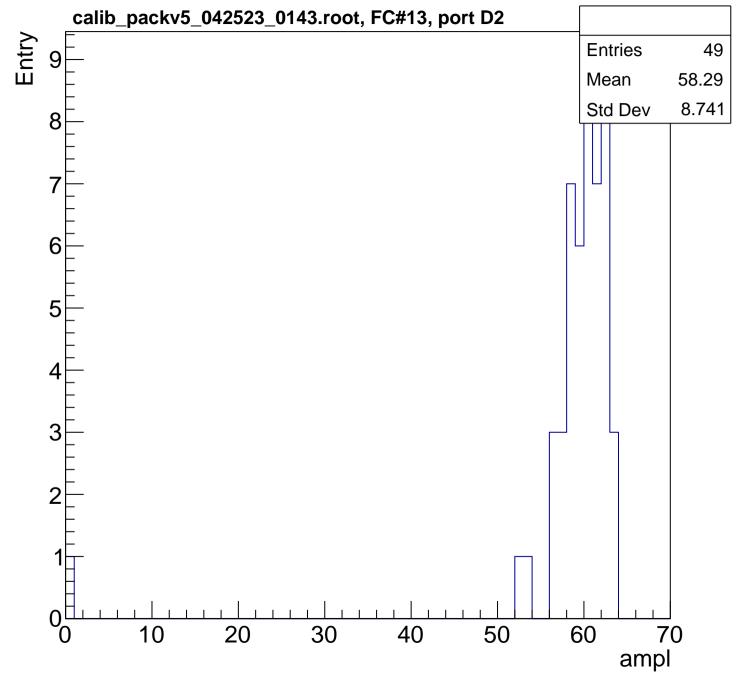


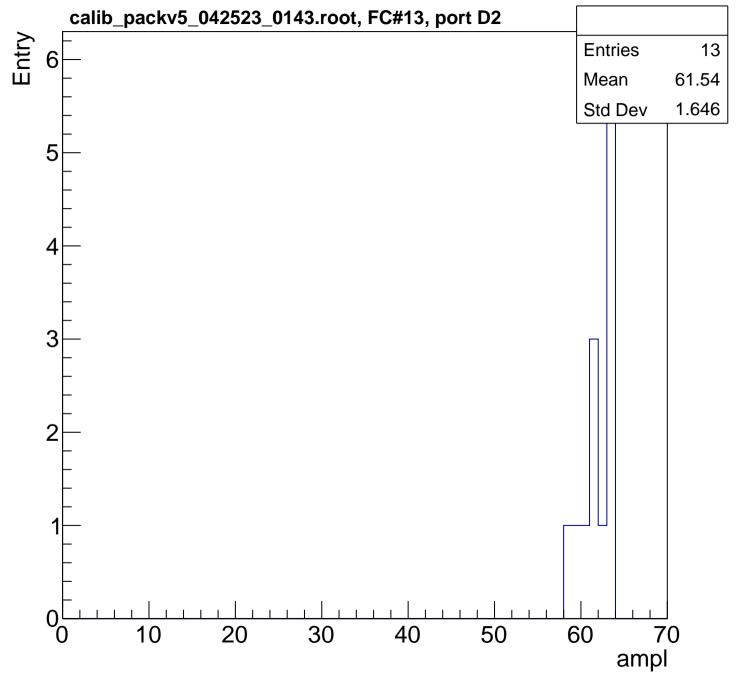




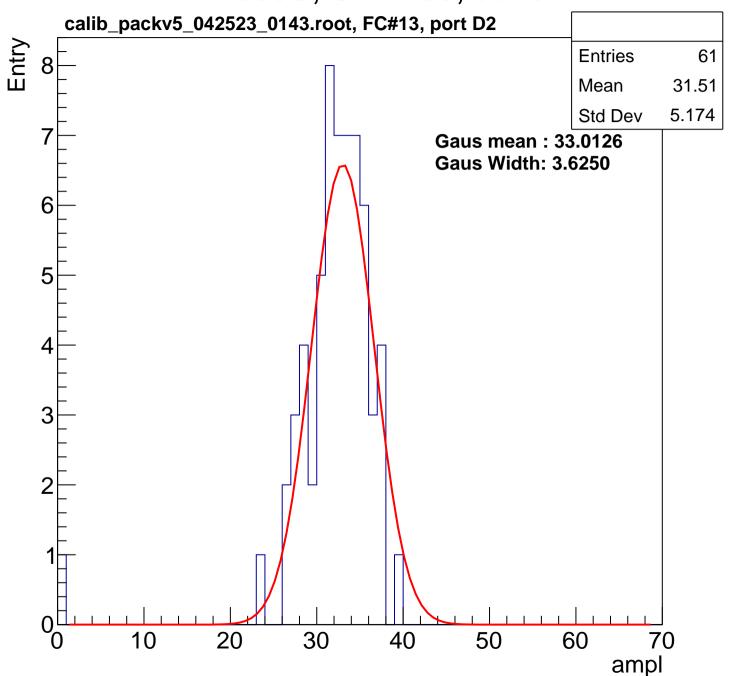


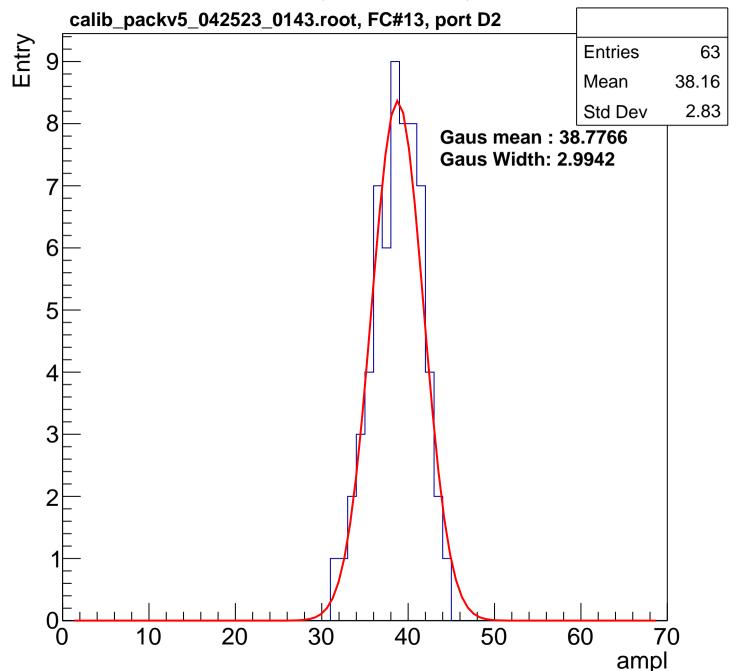


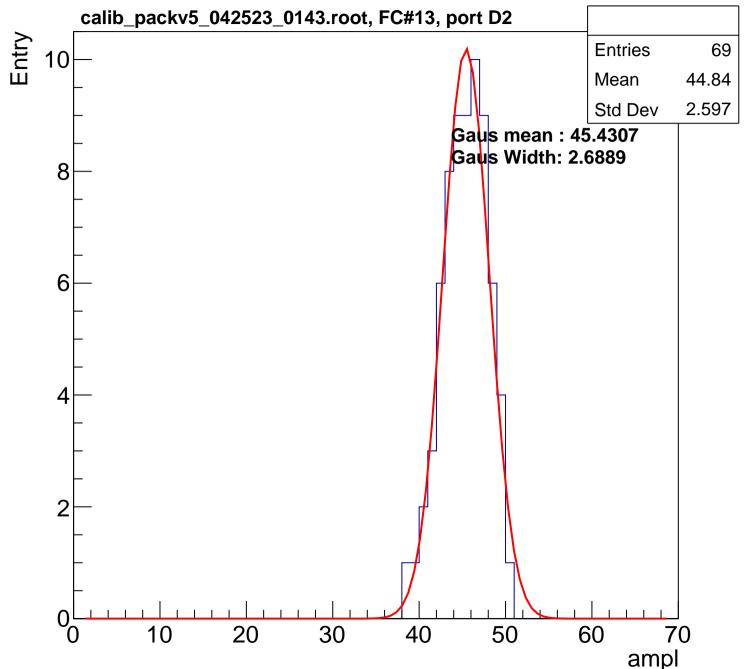


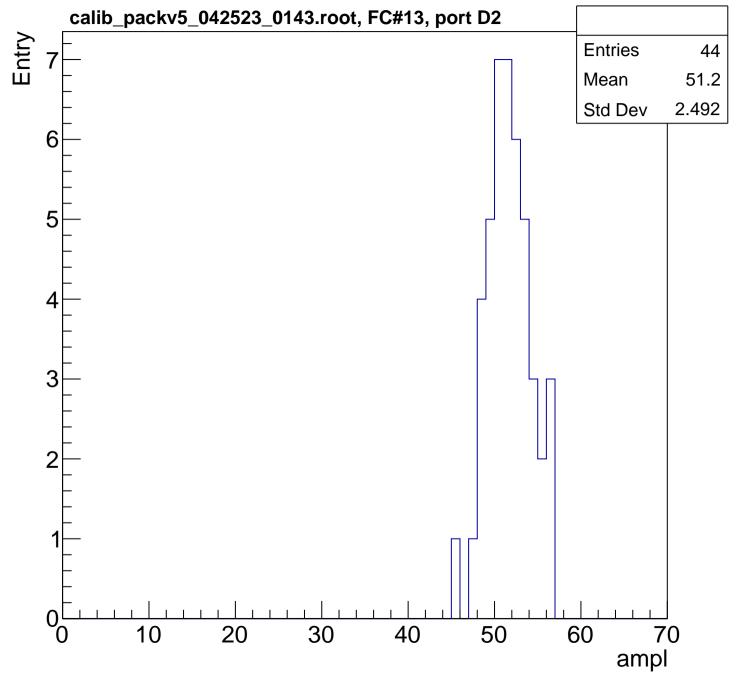


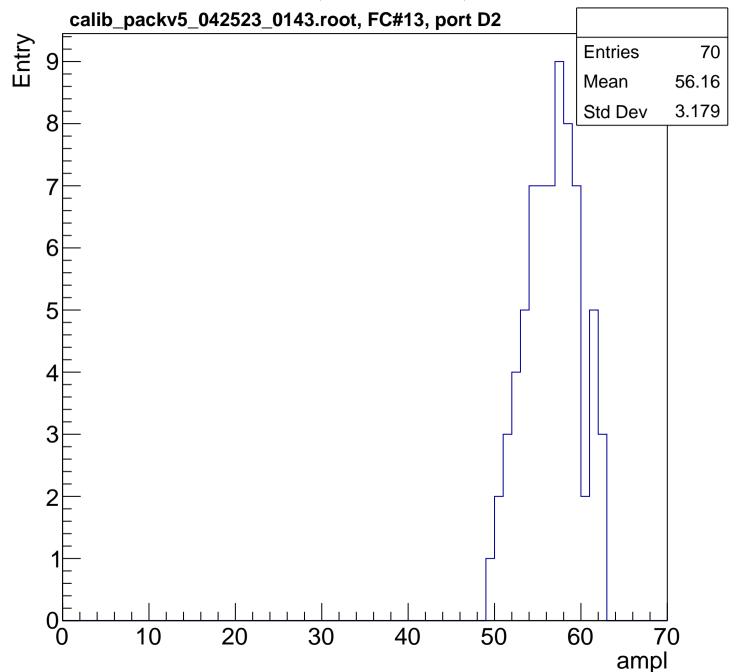
B1L003S, U7-ch82, adc7 calib_packv5_042523_0143.root, FC#13, port D2 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

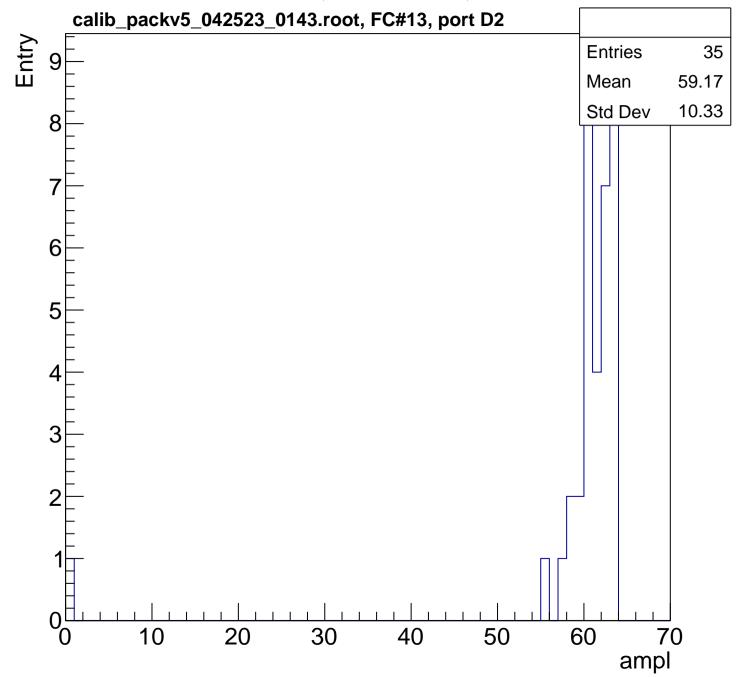


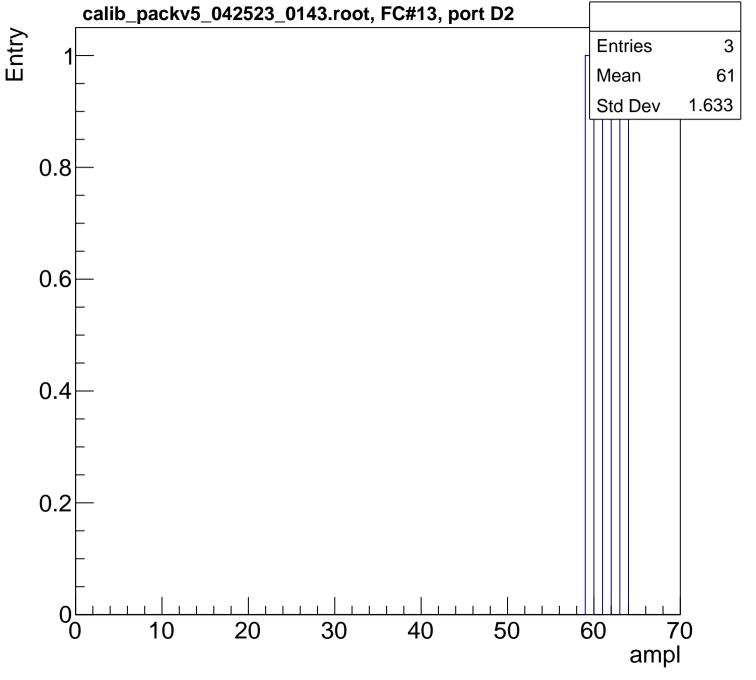




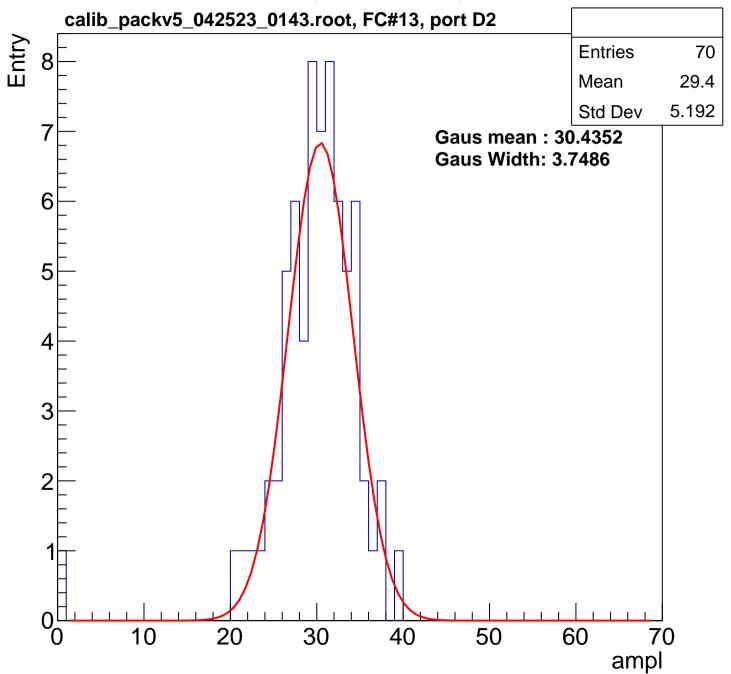


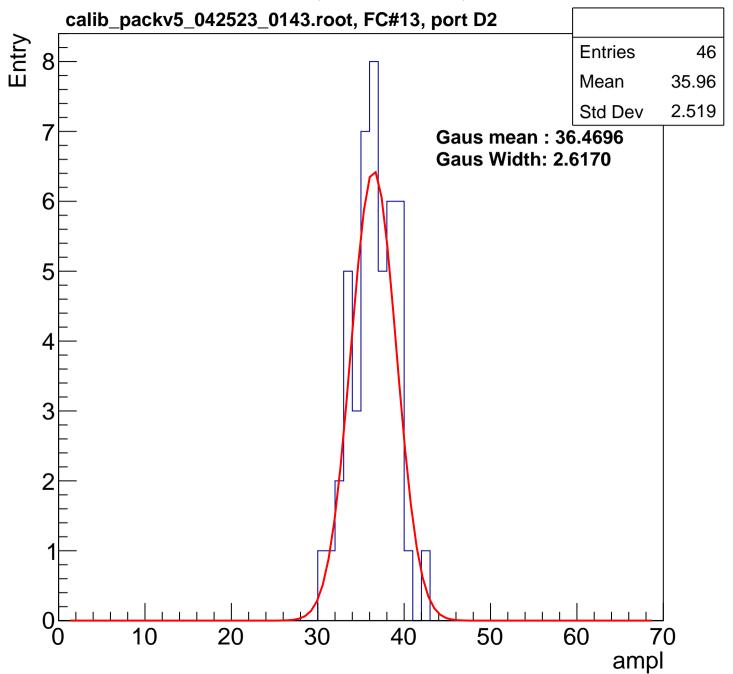


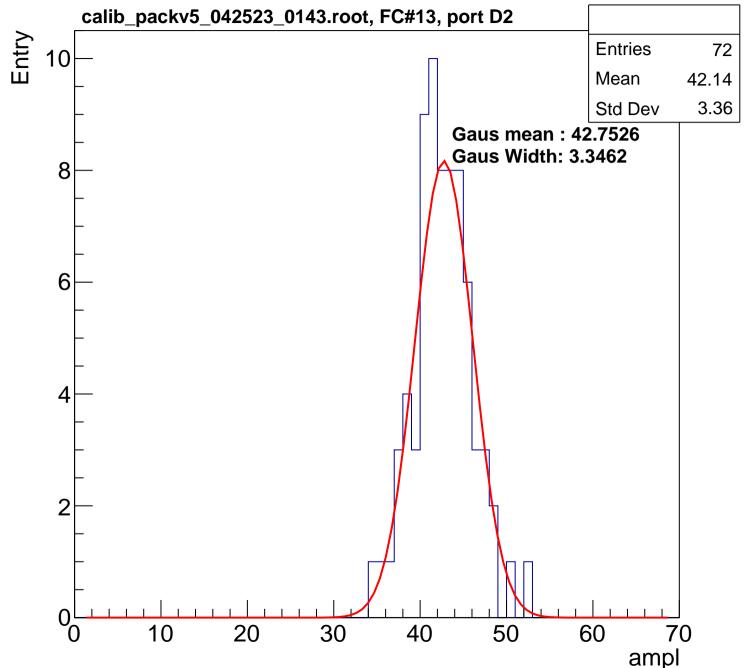


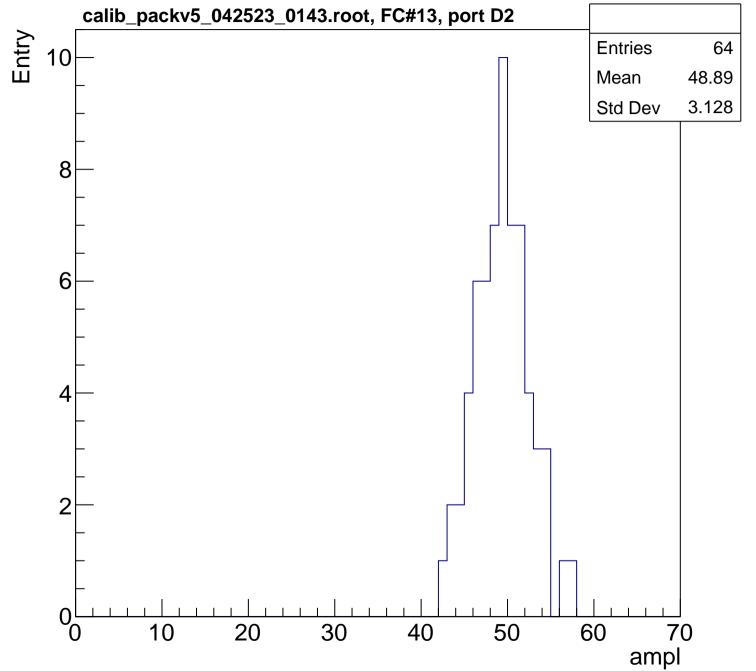


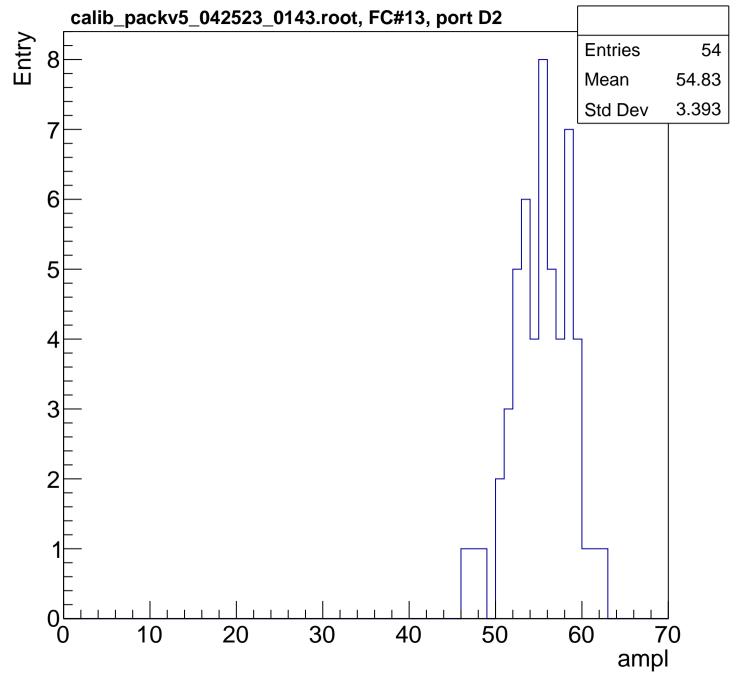


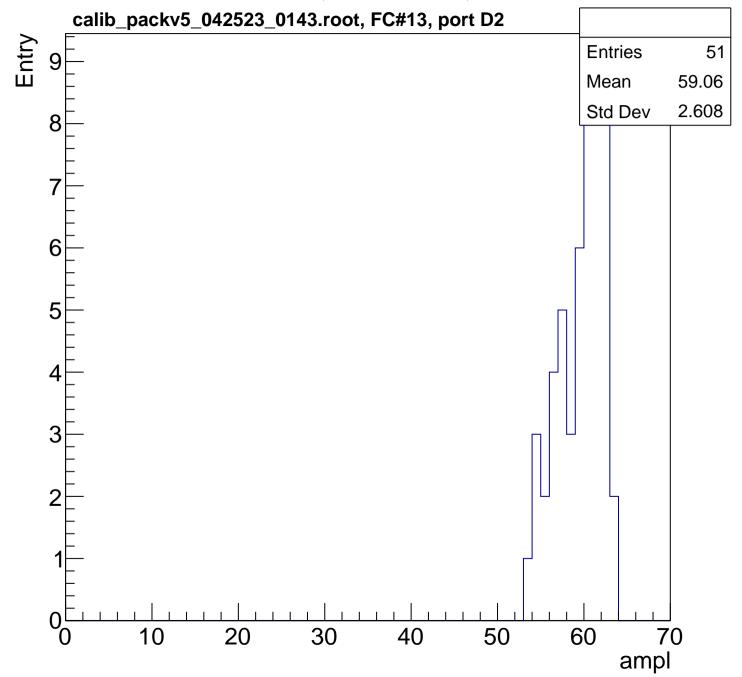


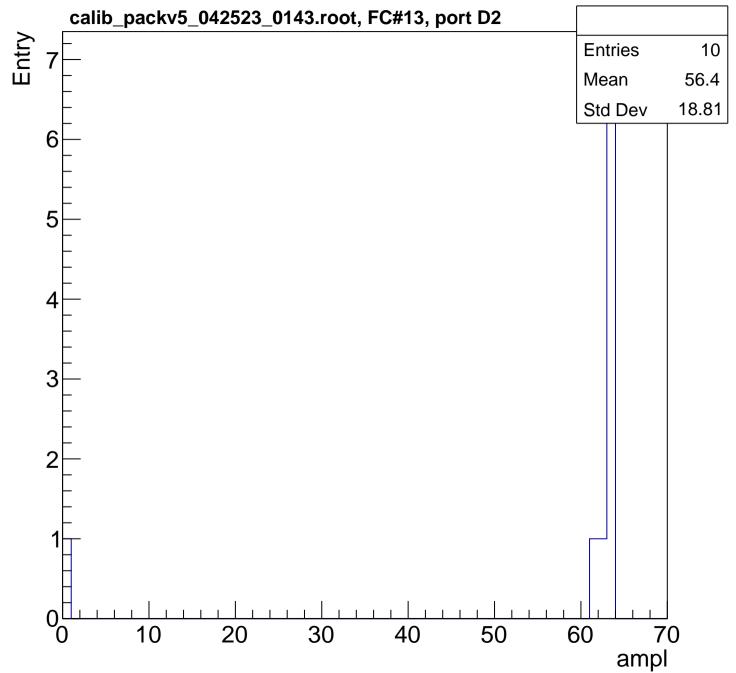


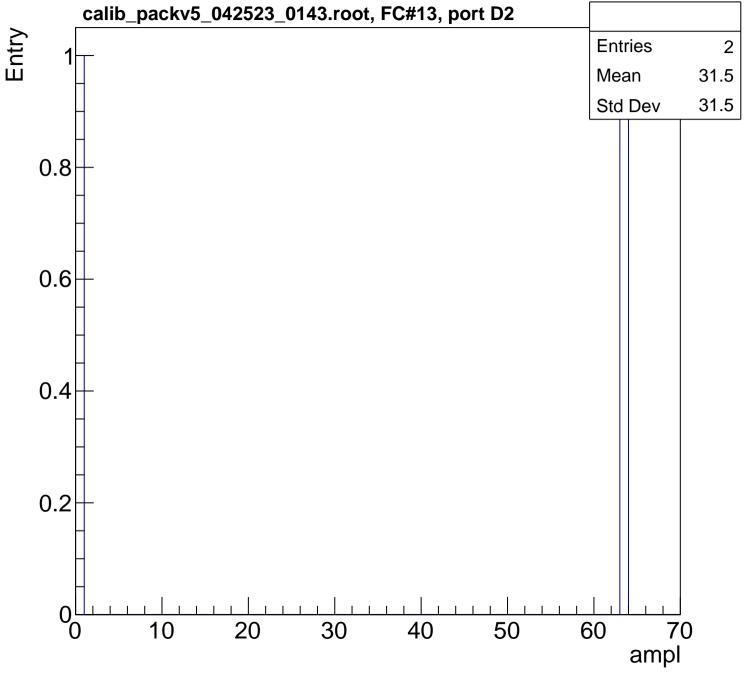


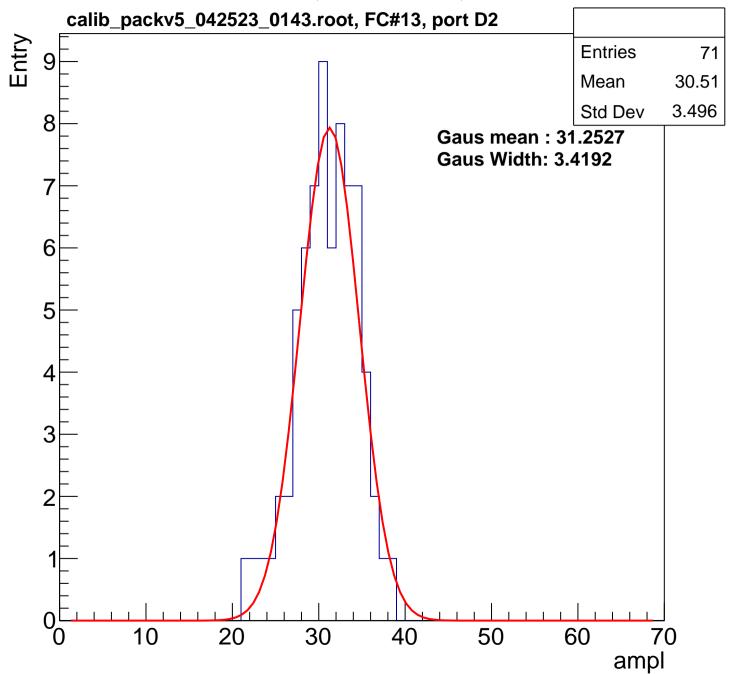


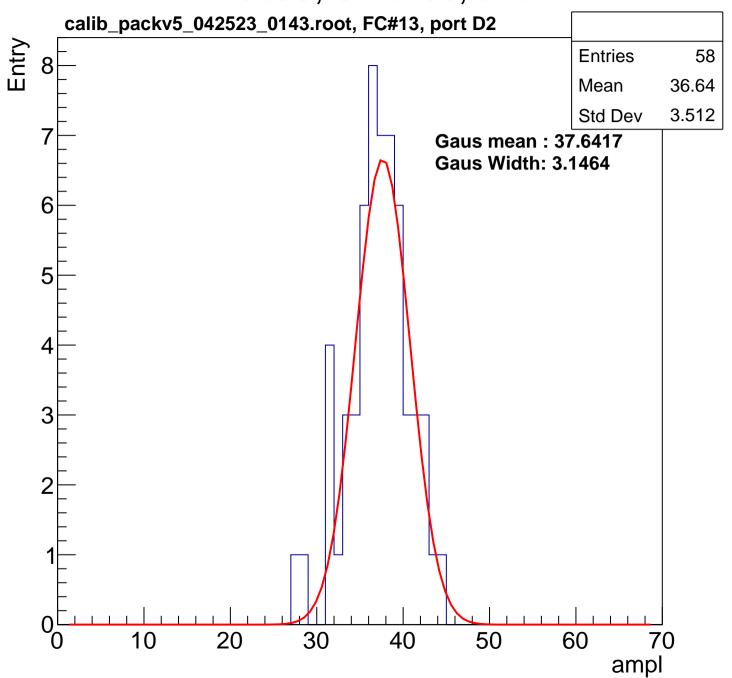


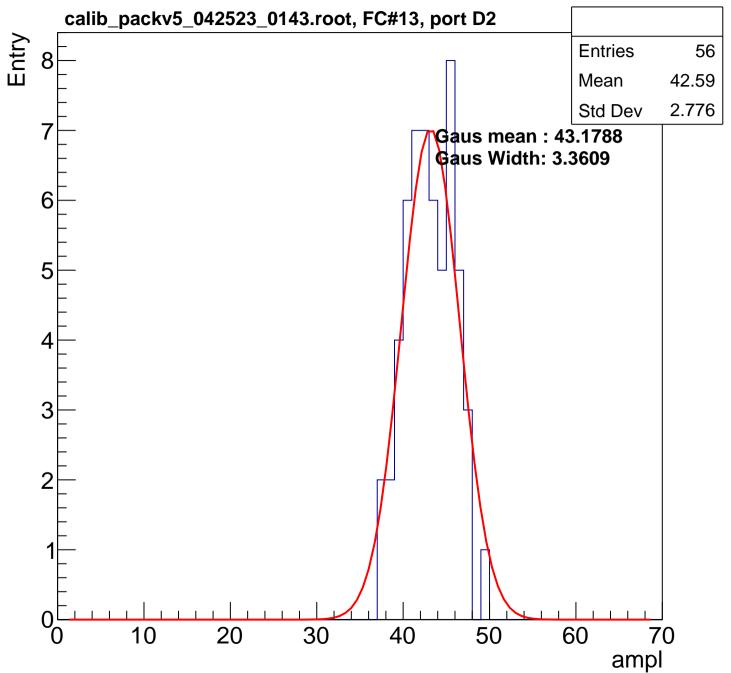


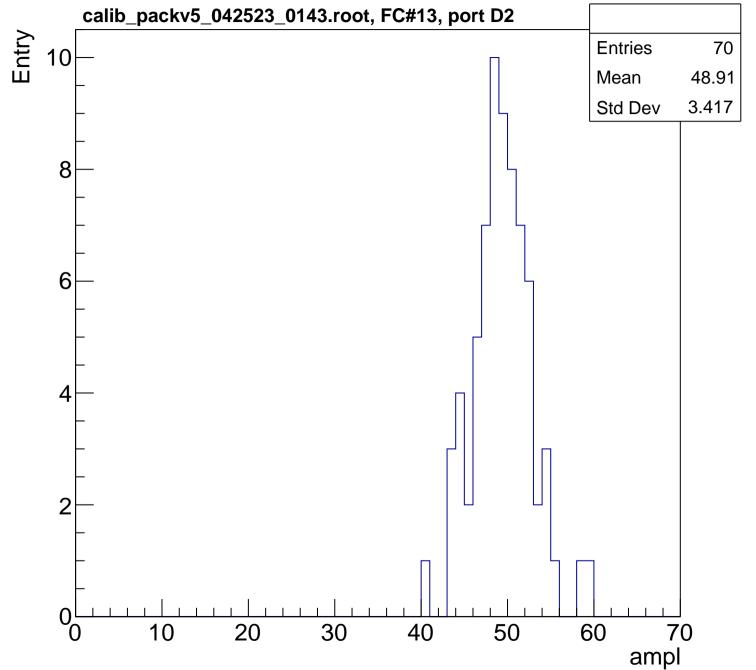


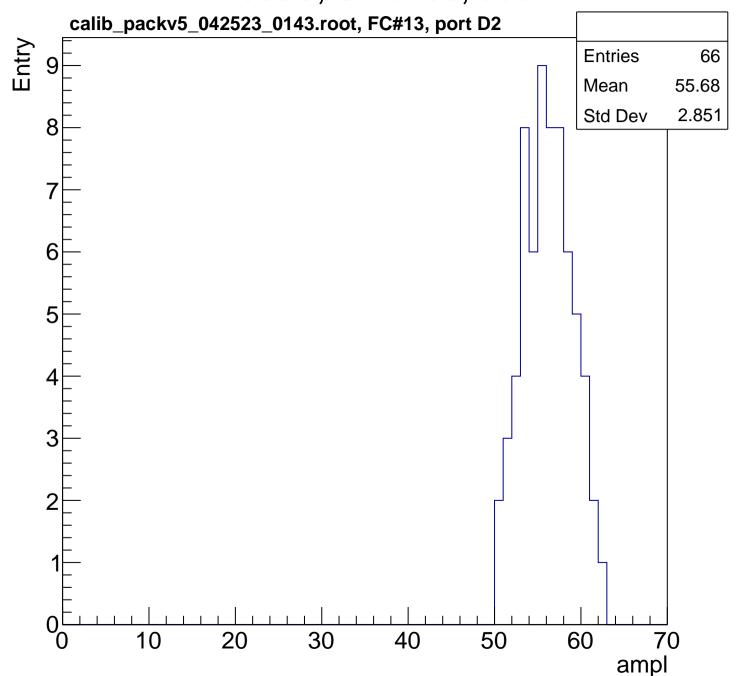


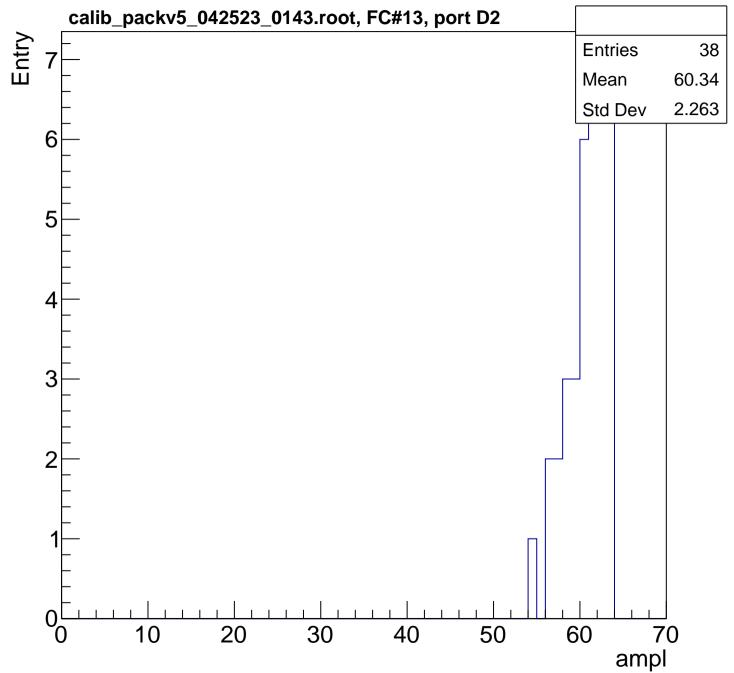


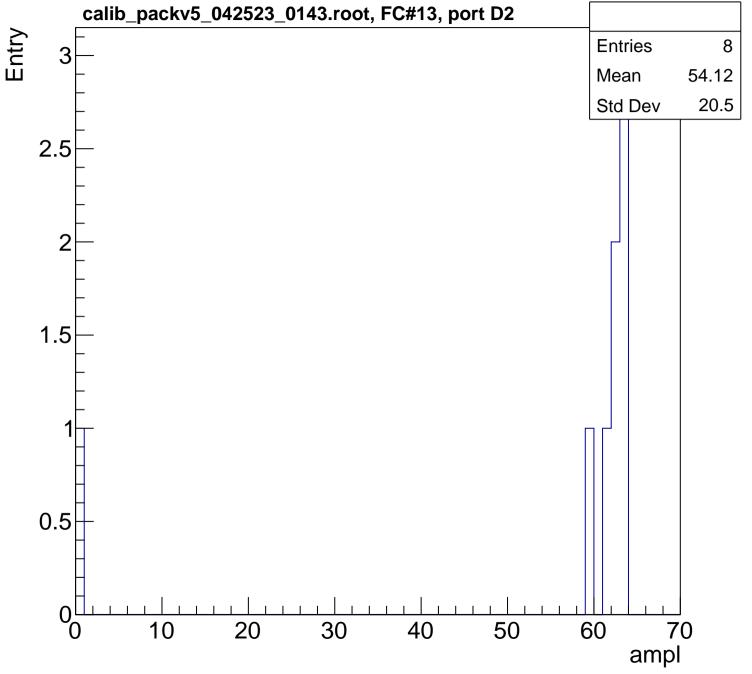


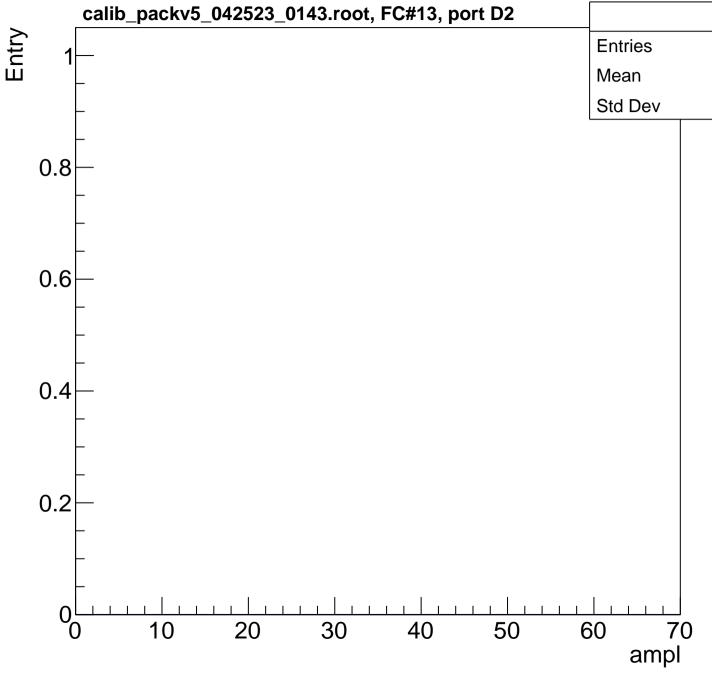


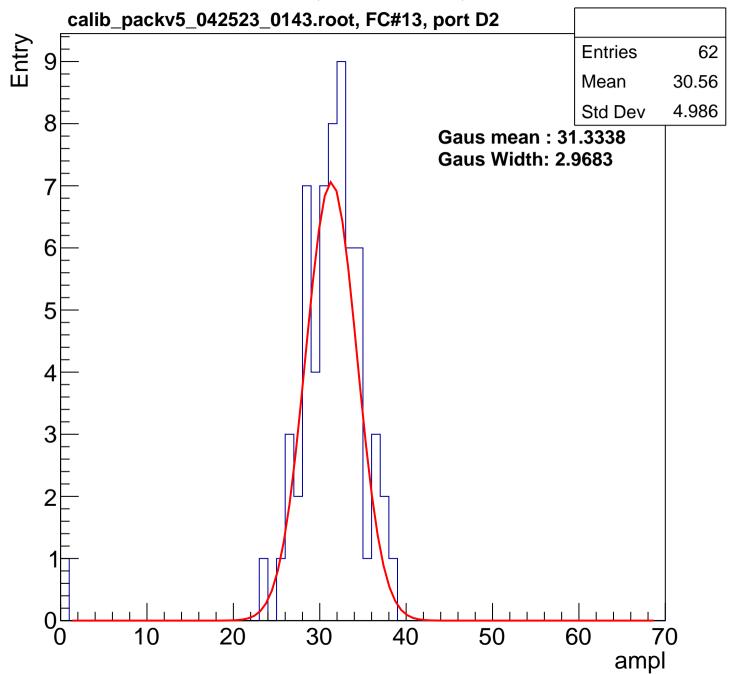


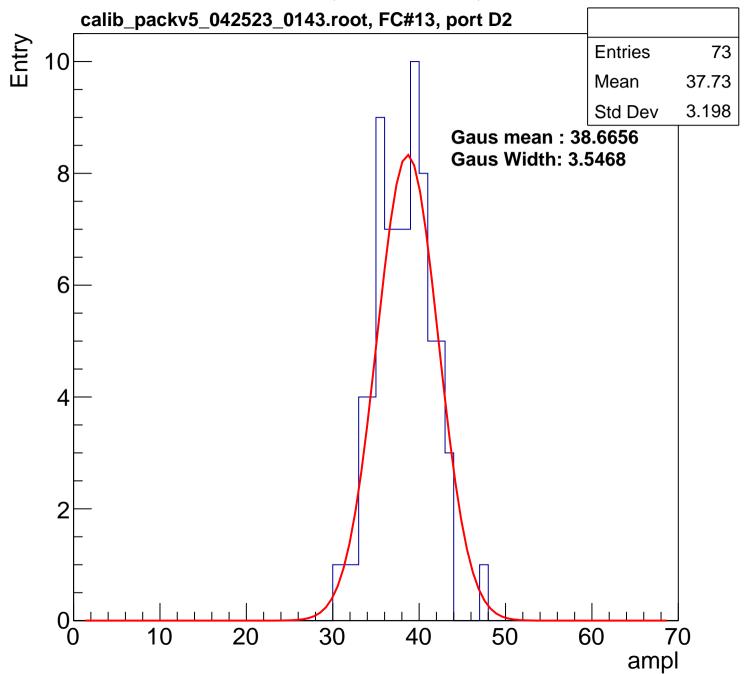


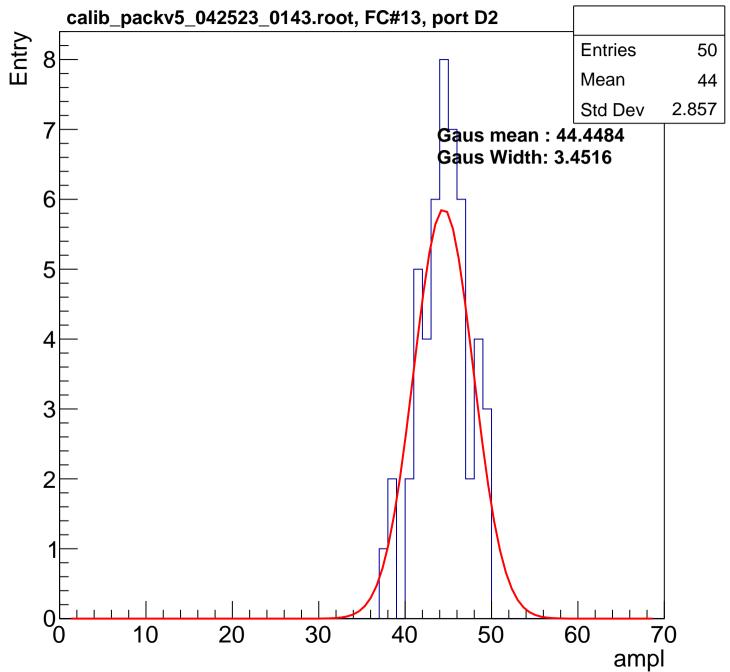


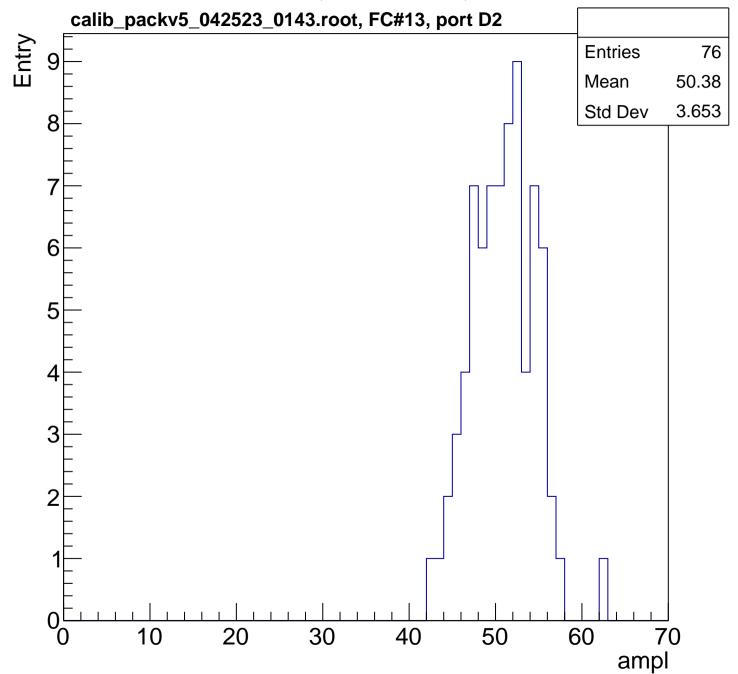


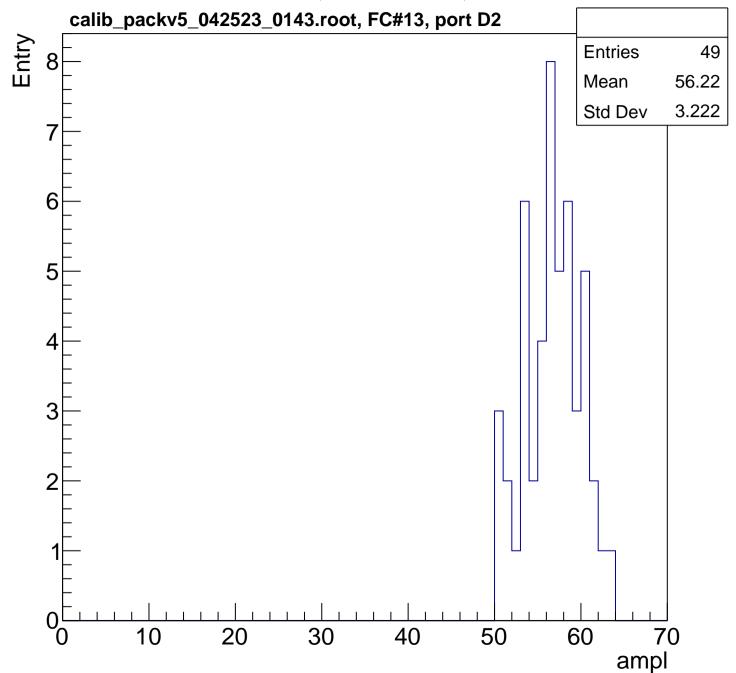


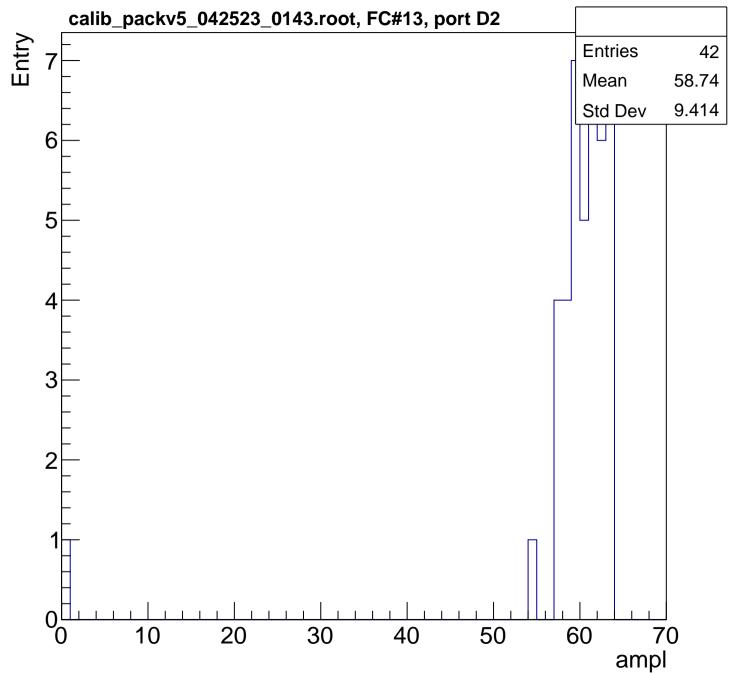


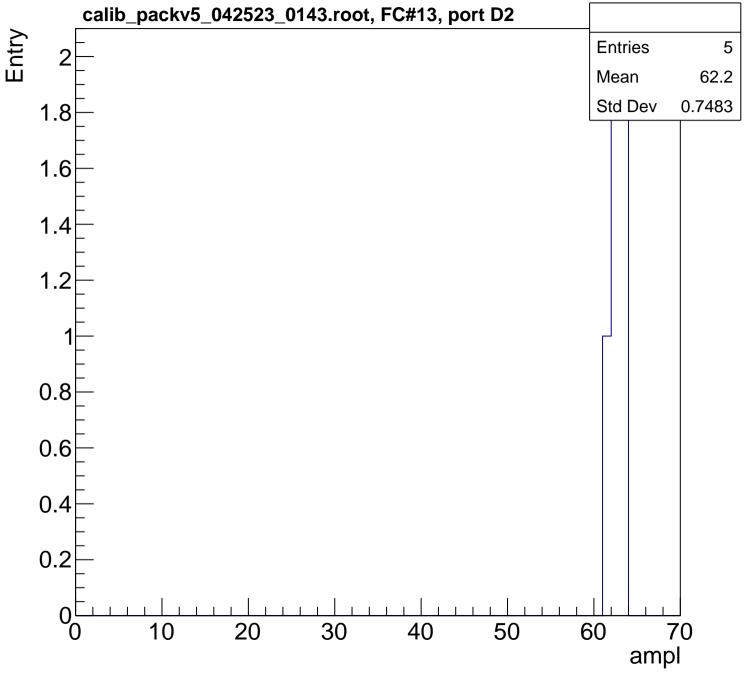


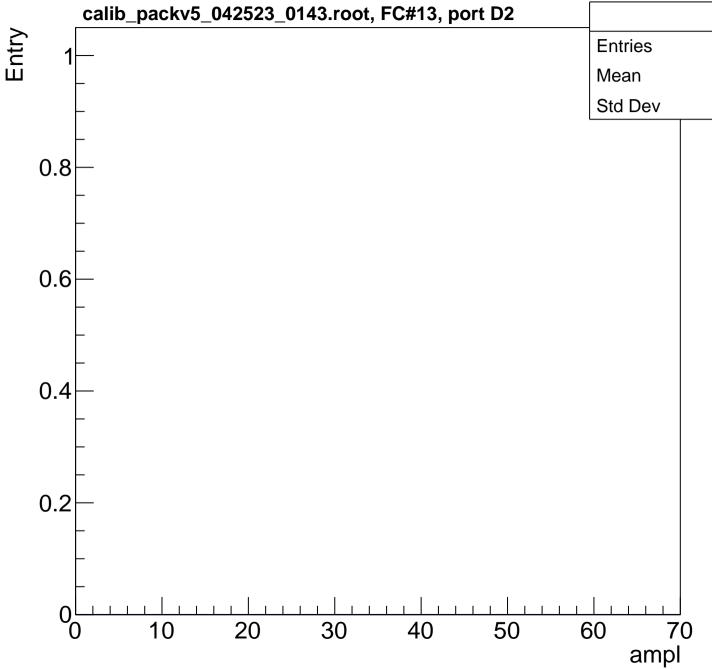


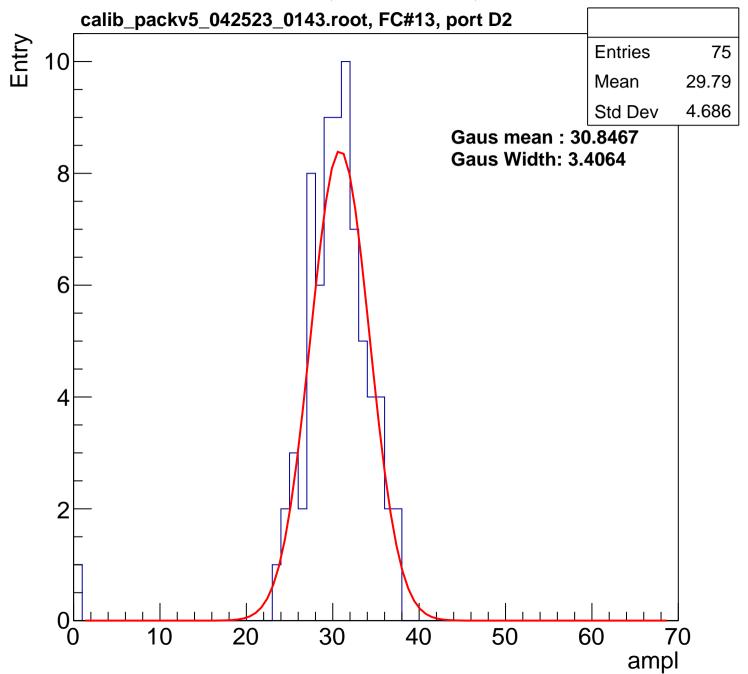


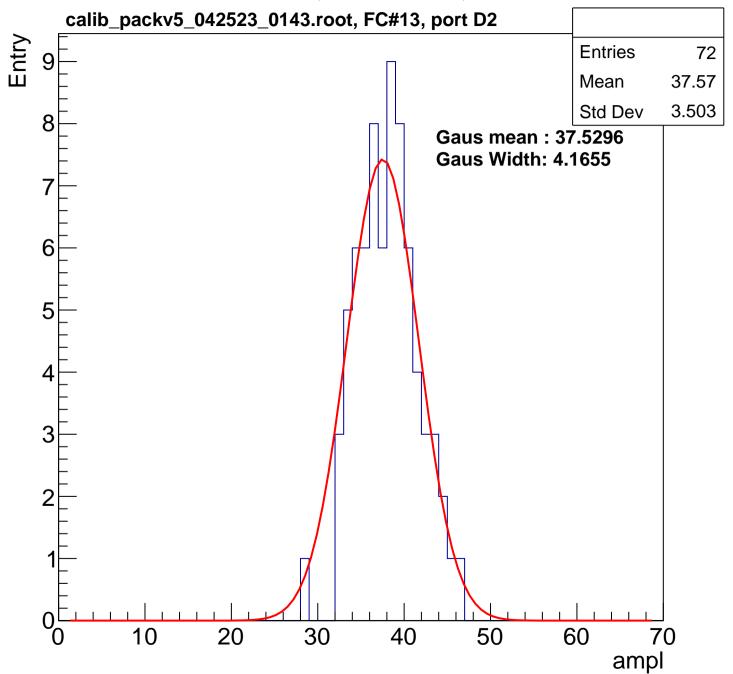


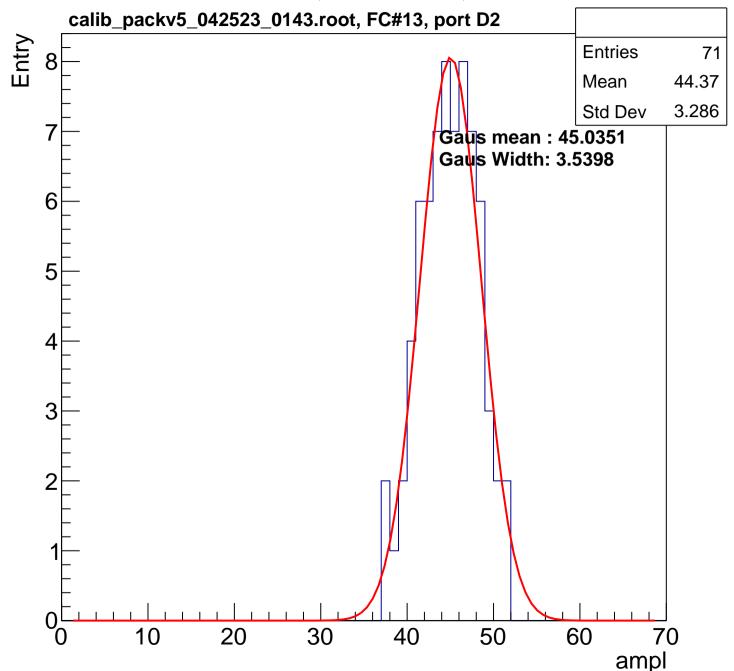


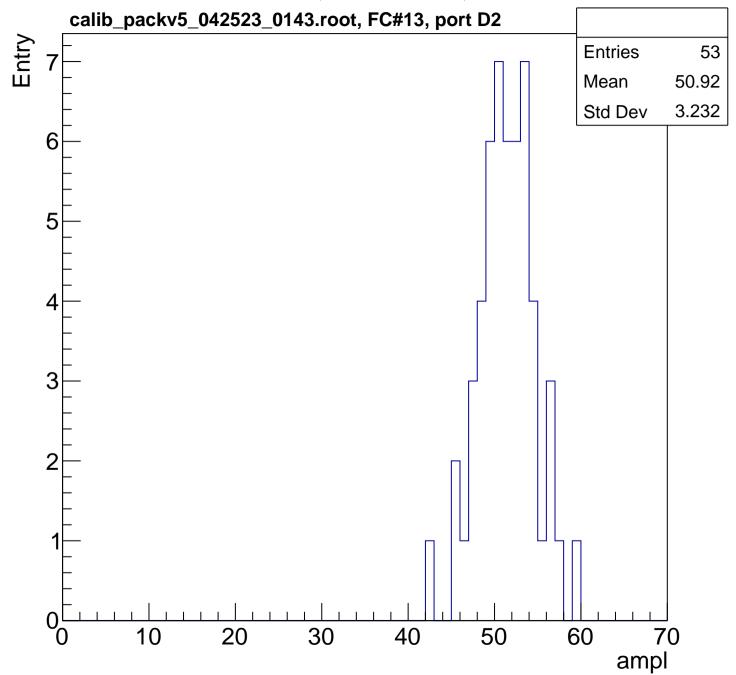


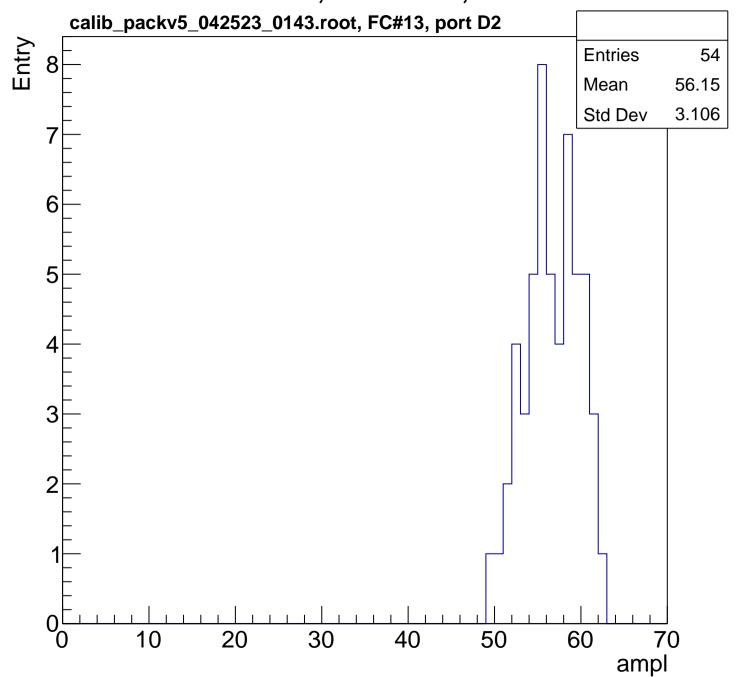


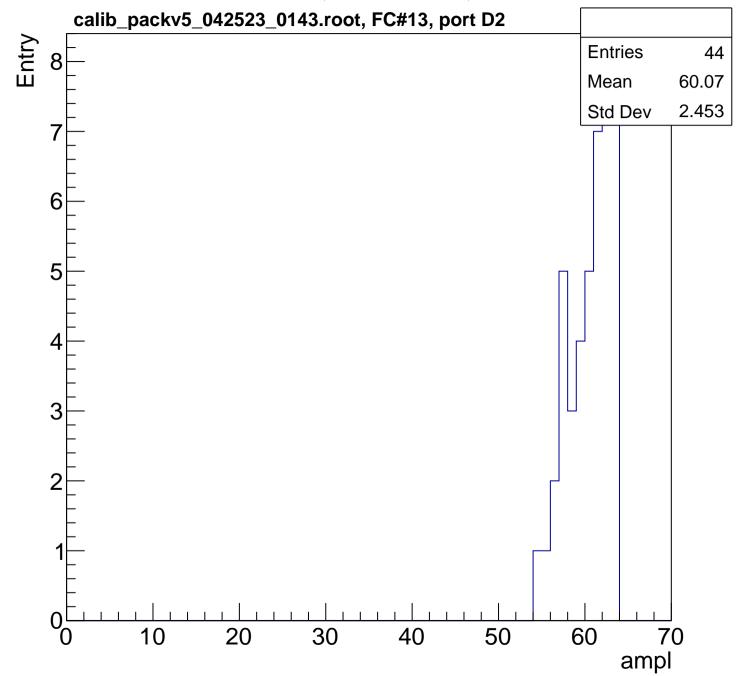


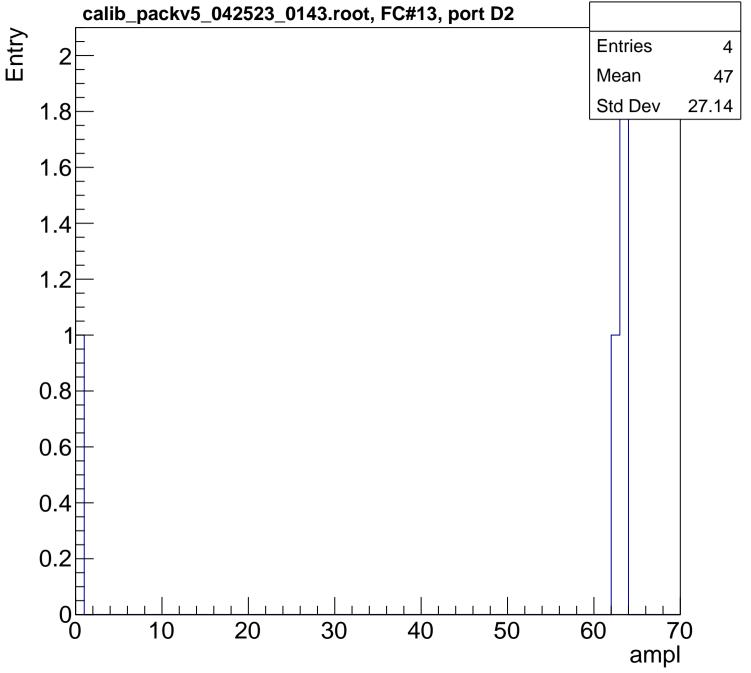




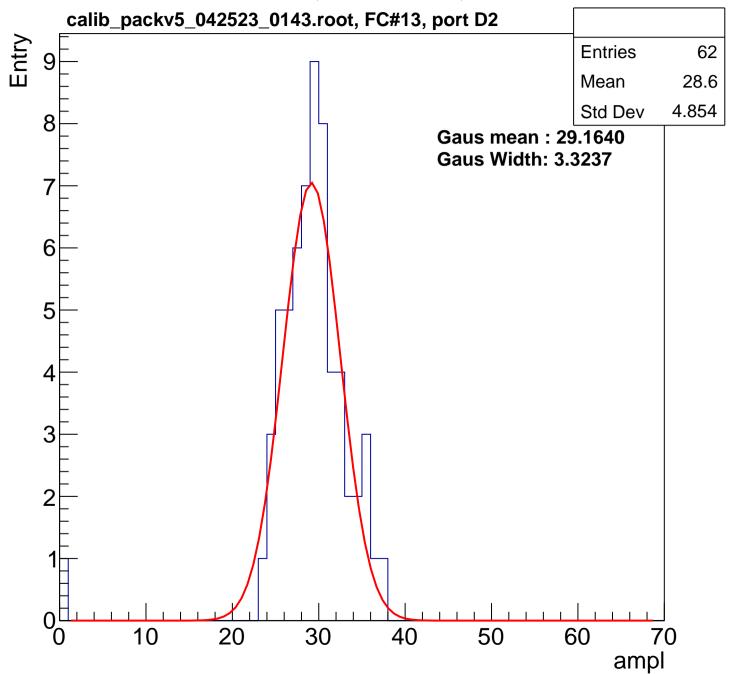


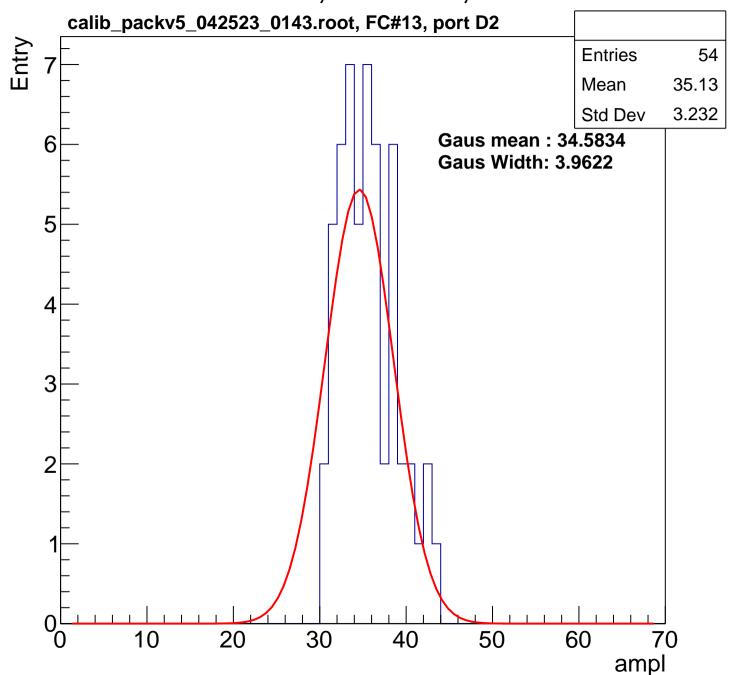


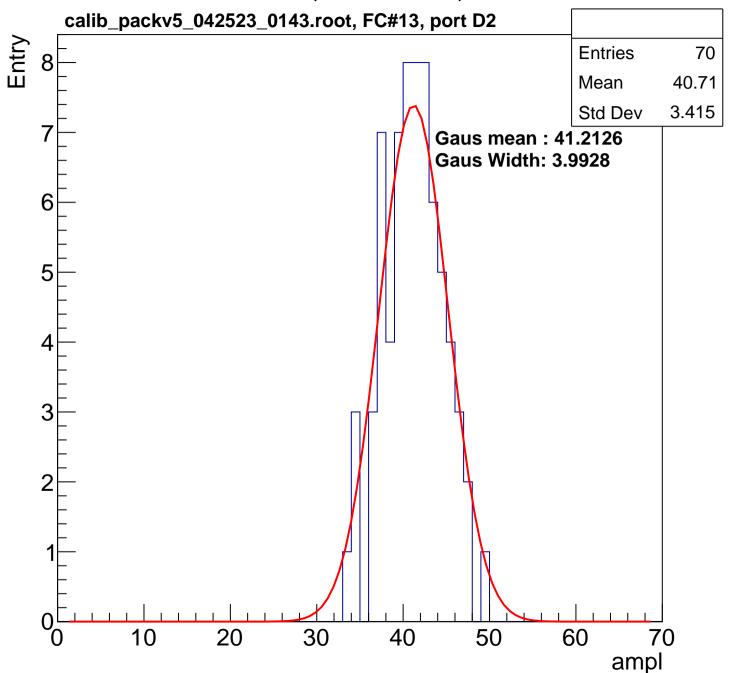


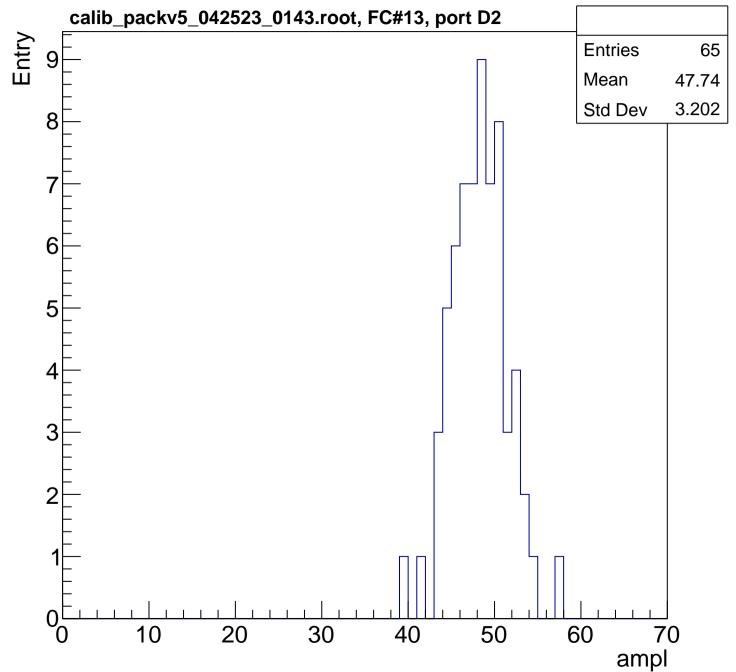


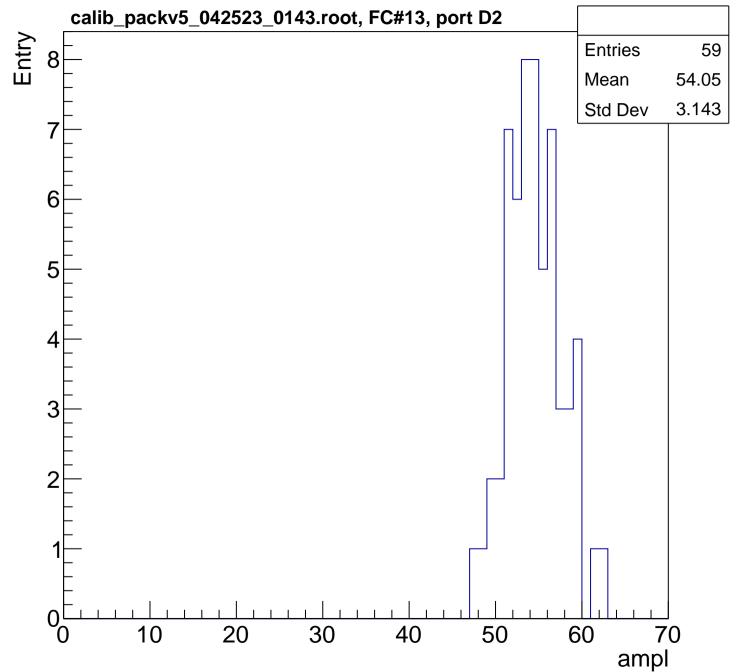
B1L003S, U7-ch87, adc7 calib_packv5_042523_0143.root, FC#13, port D2 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

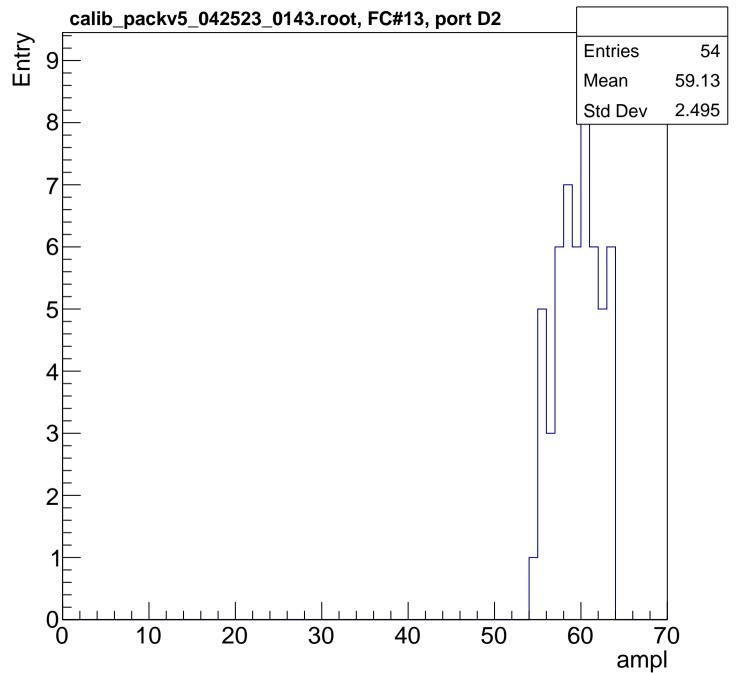


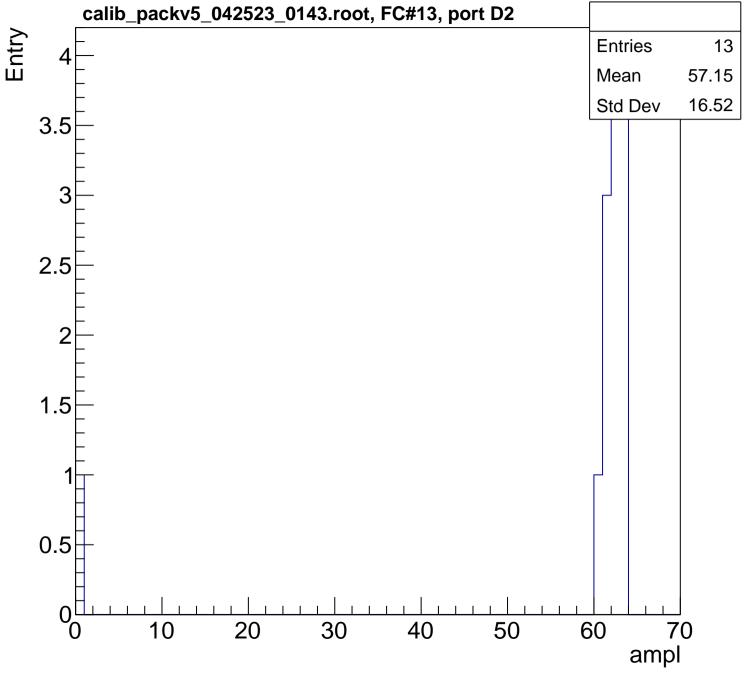


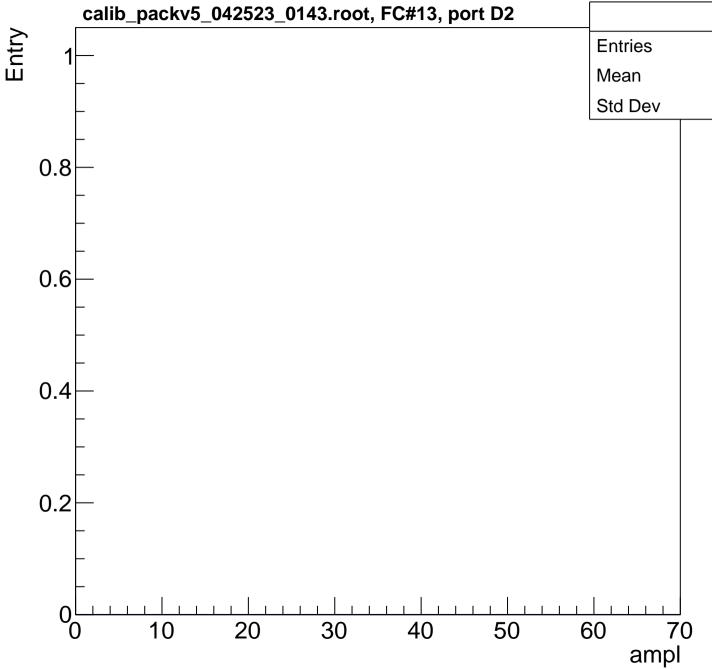


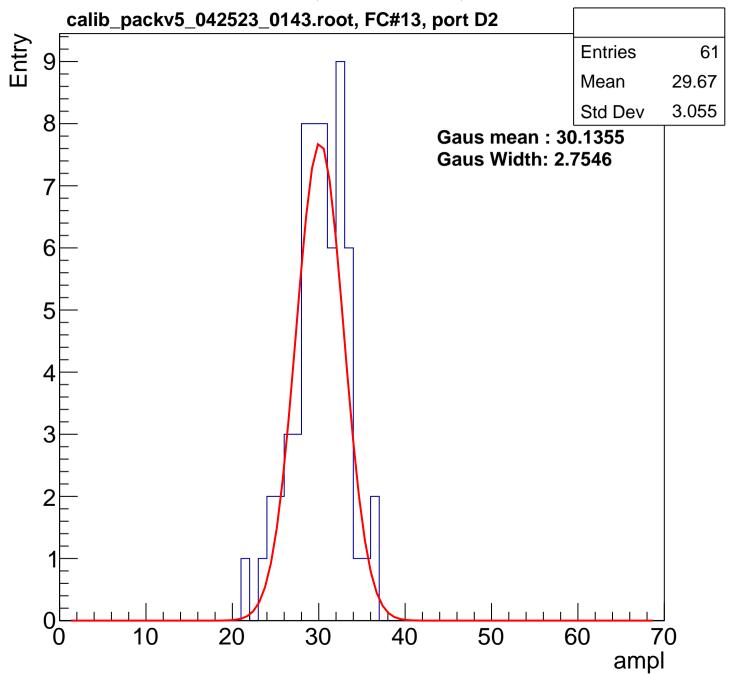


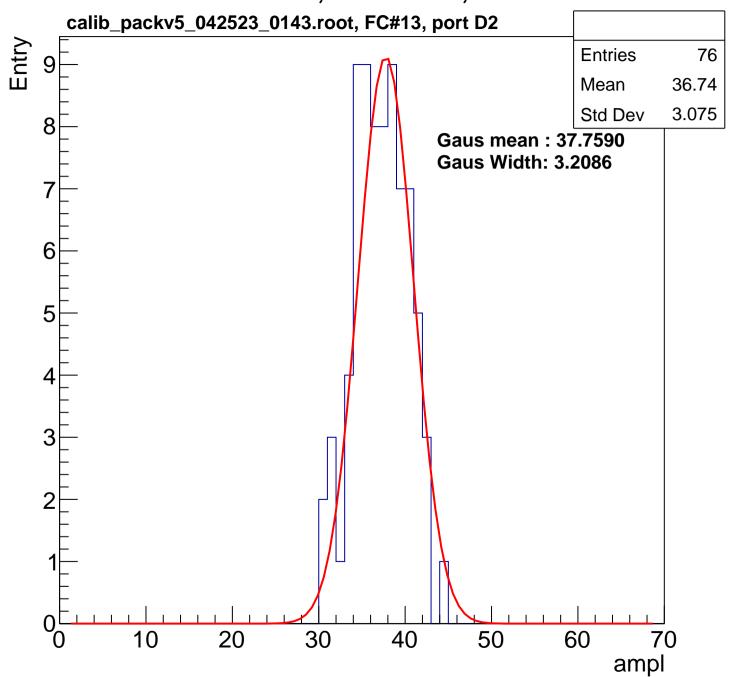


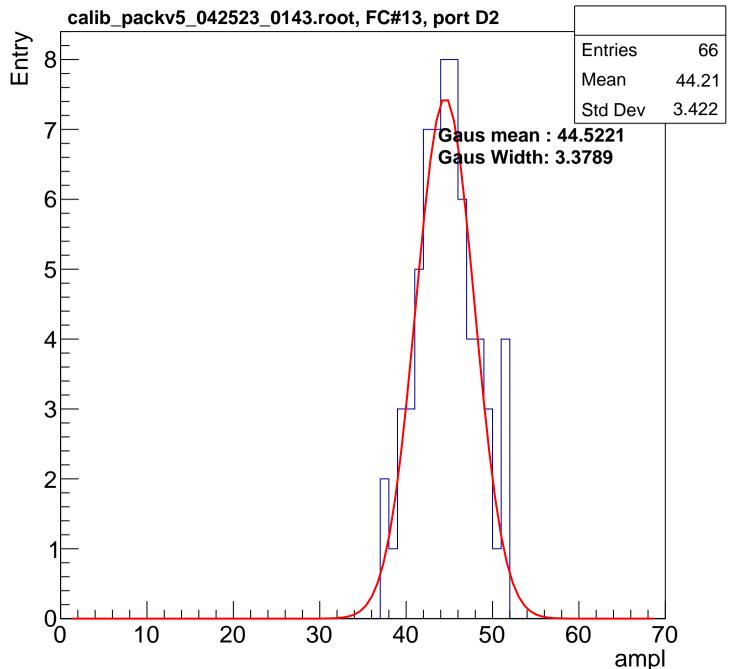


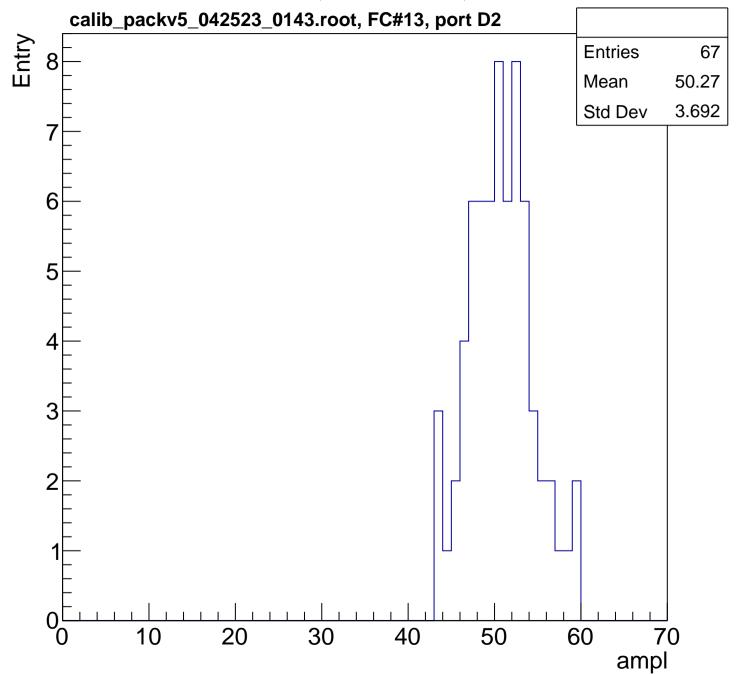


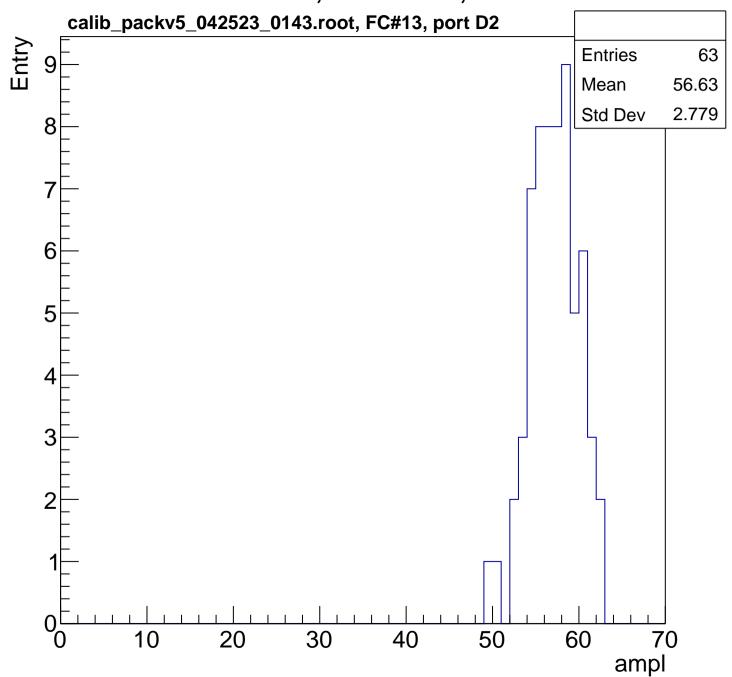


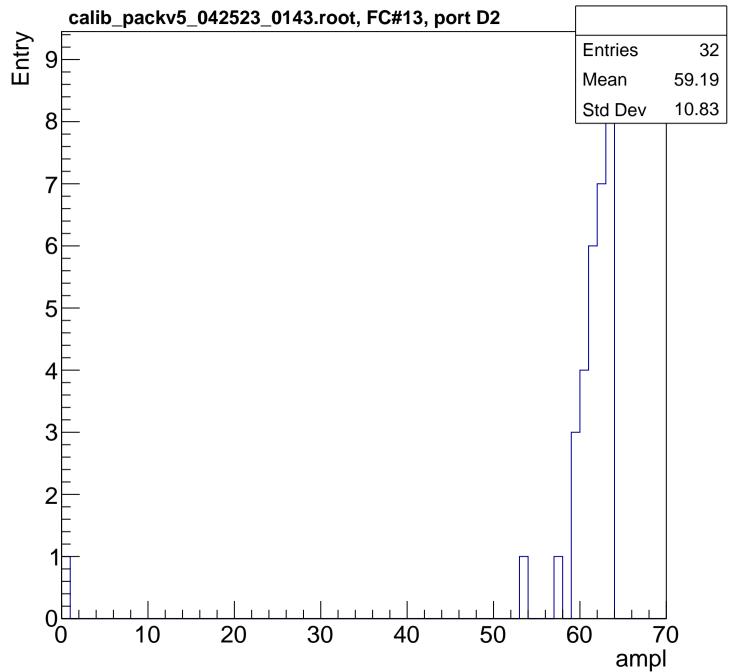


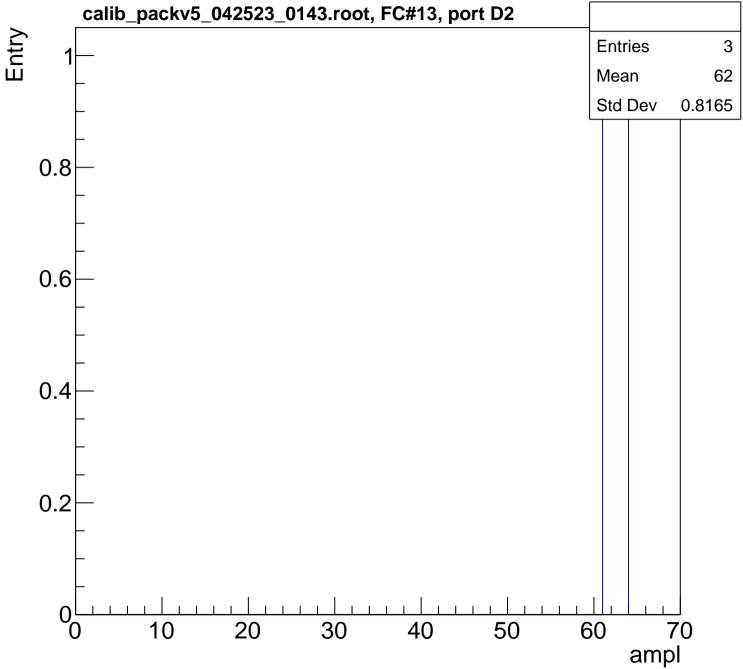




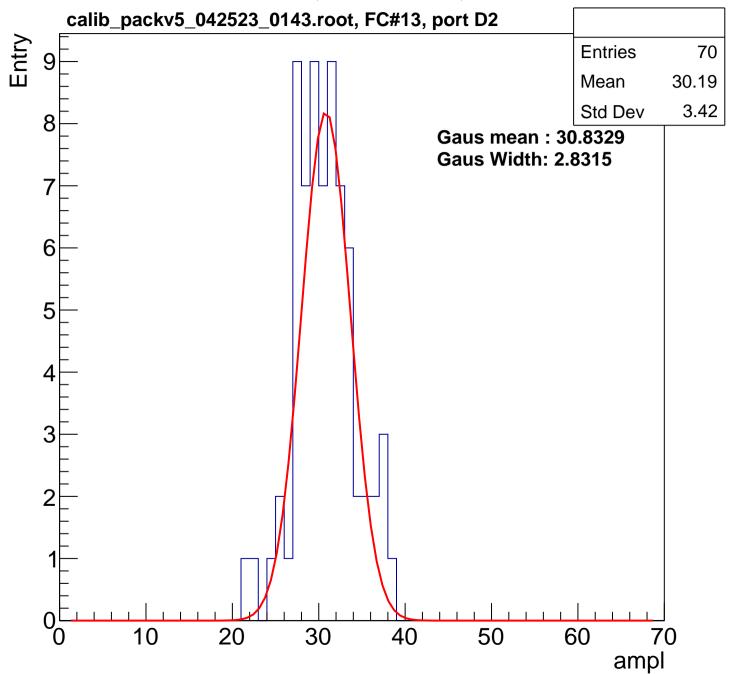


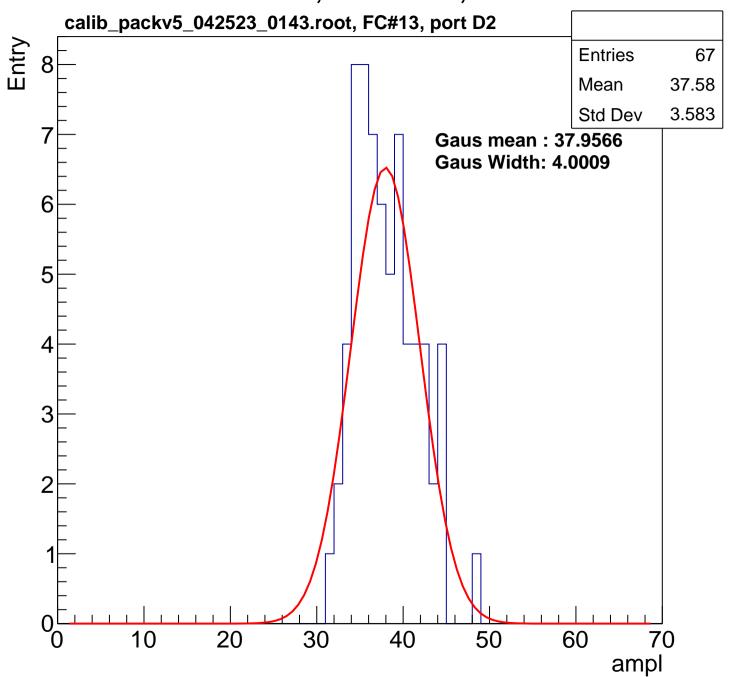


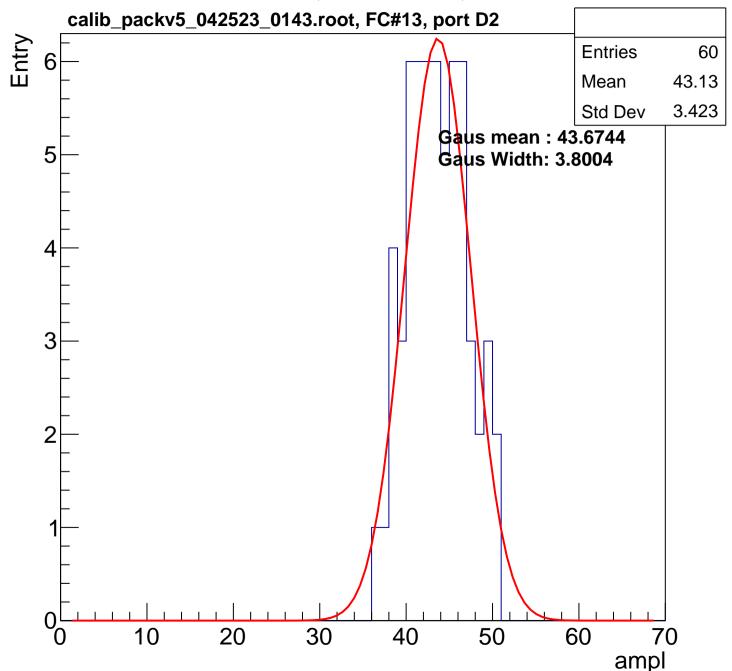


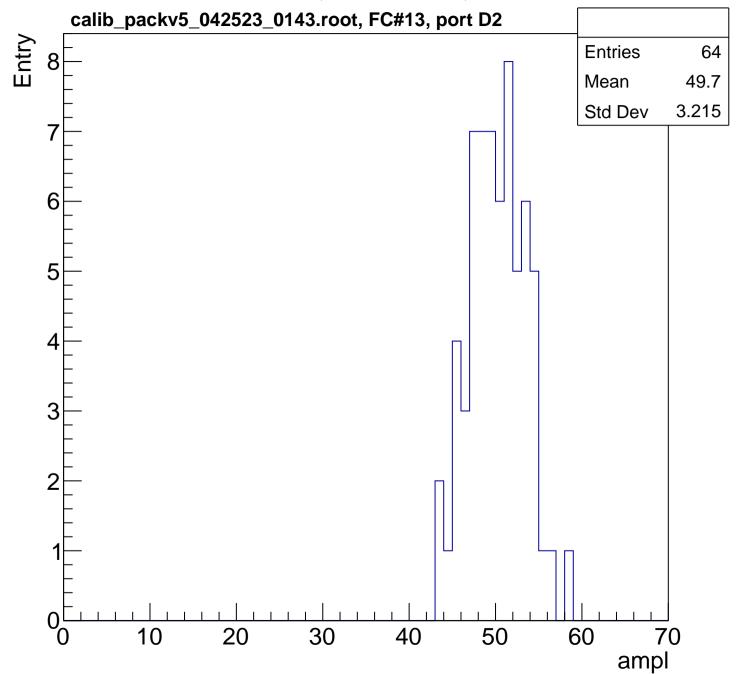


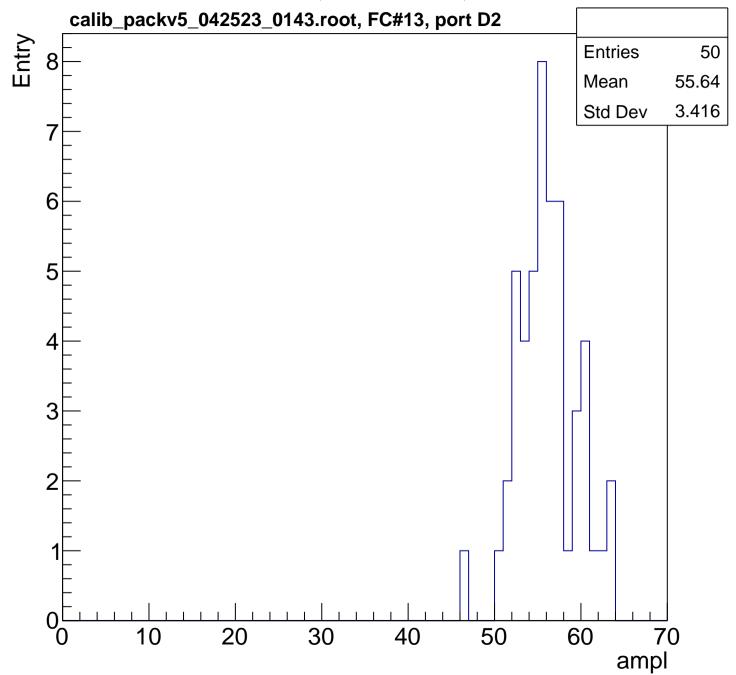


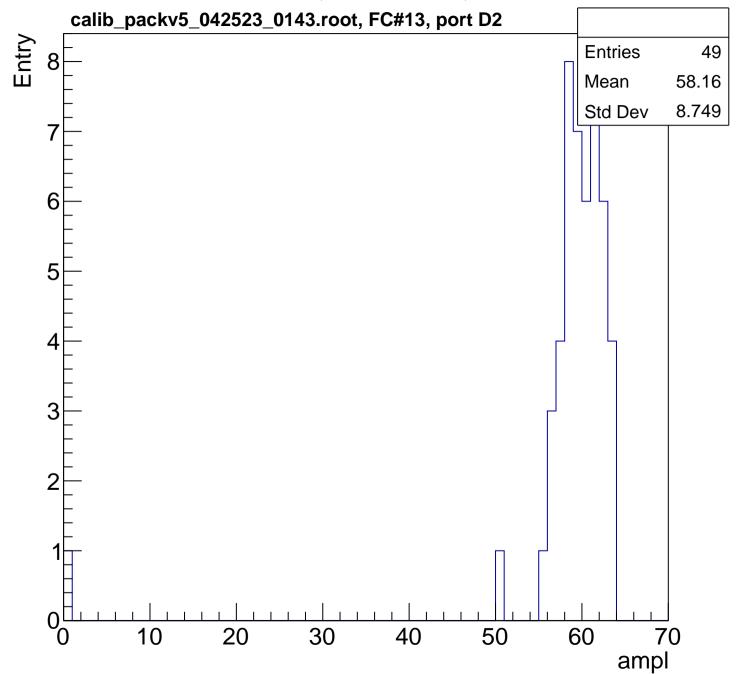


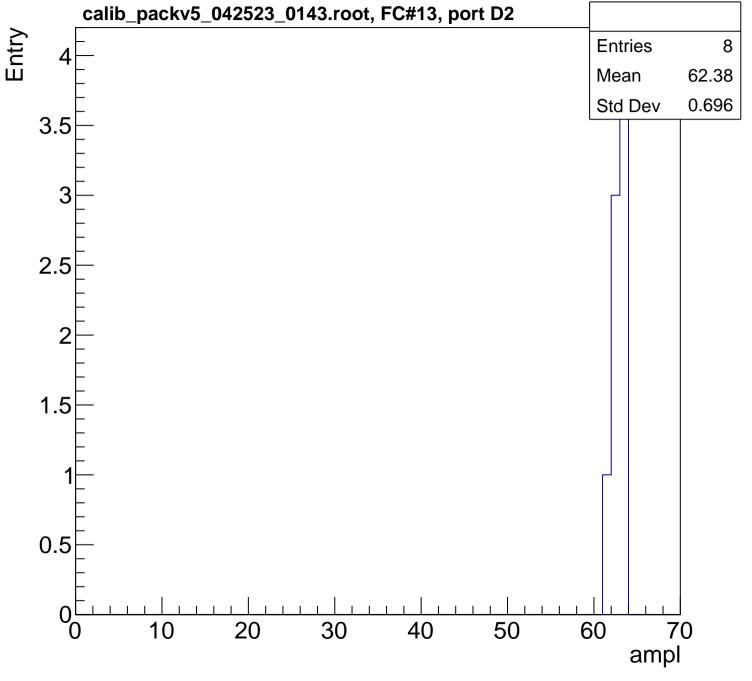


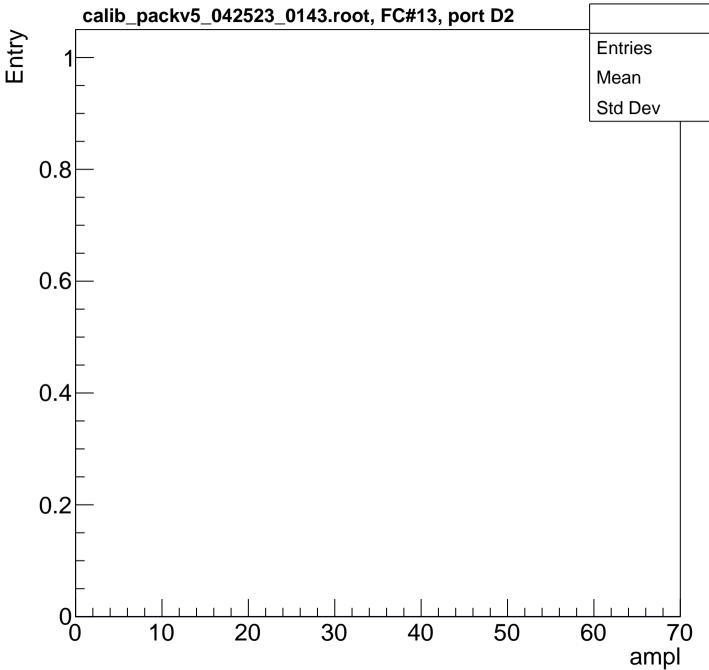


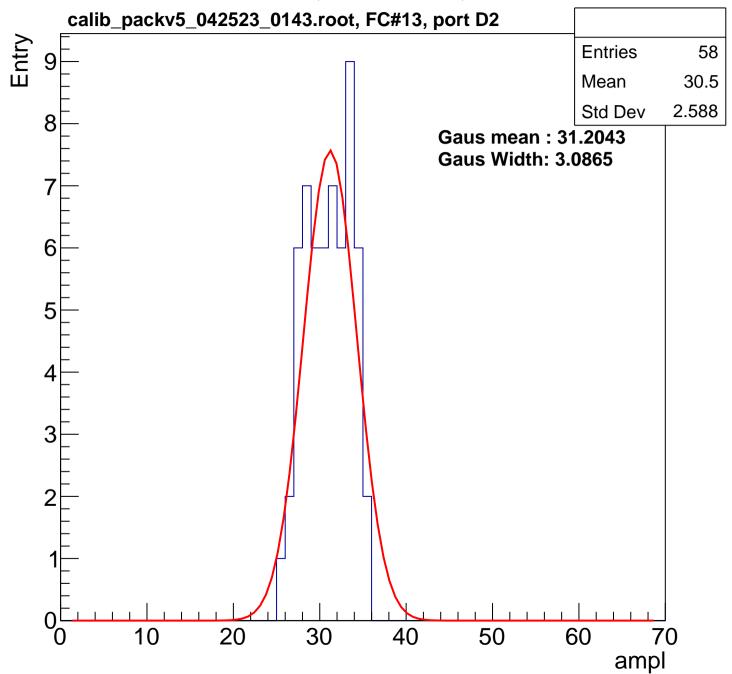


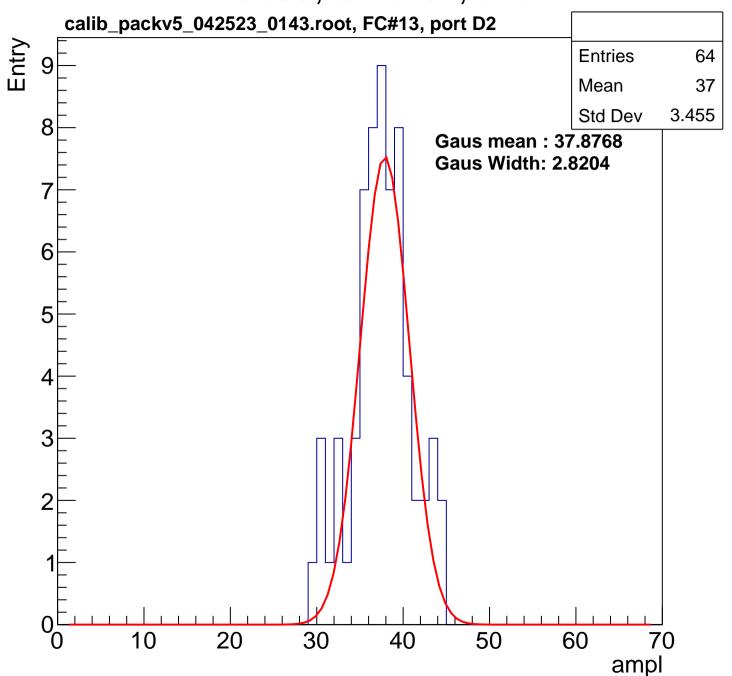


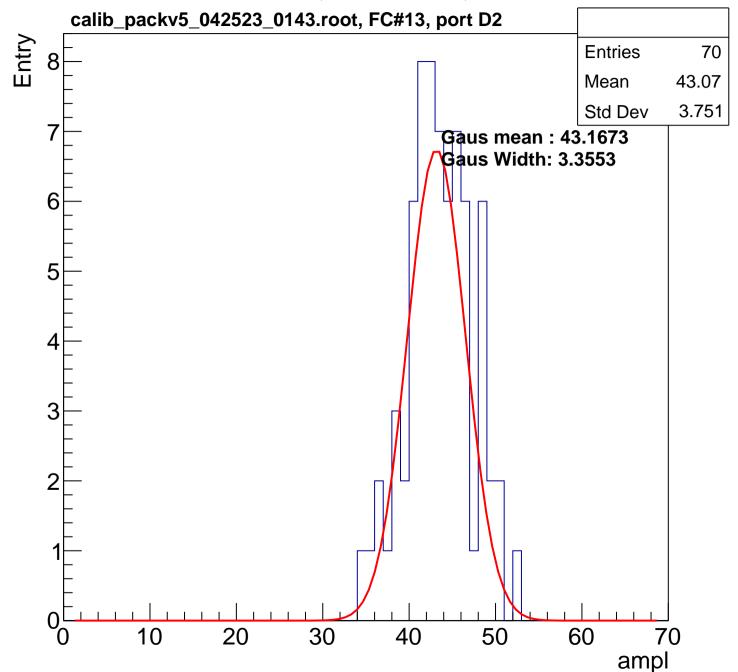


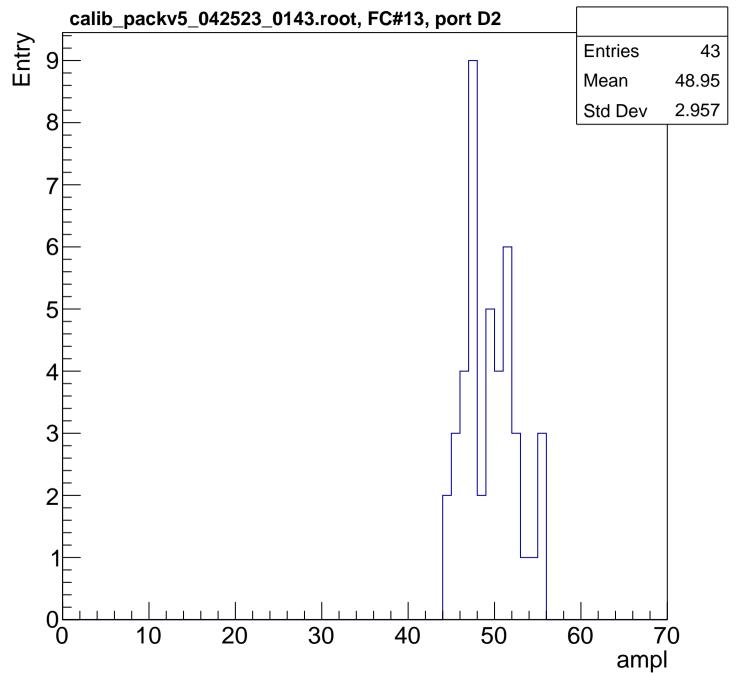


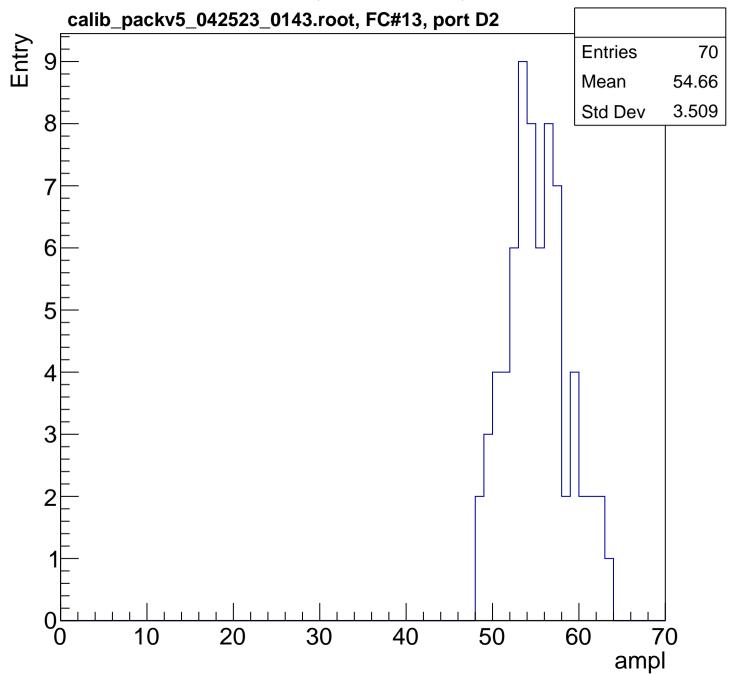


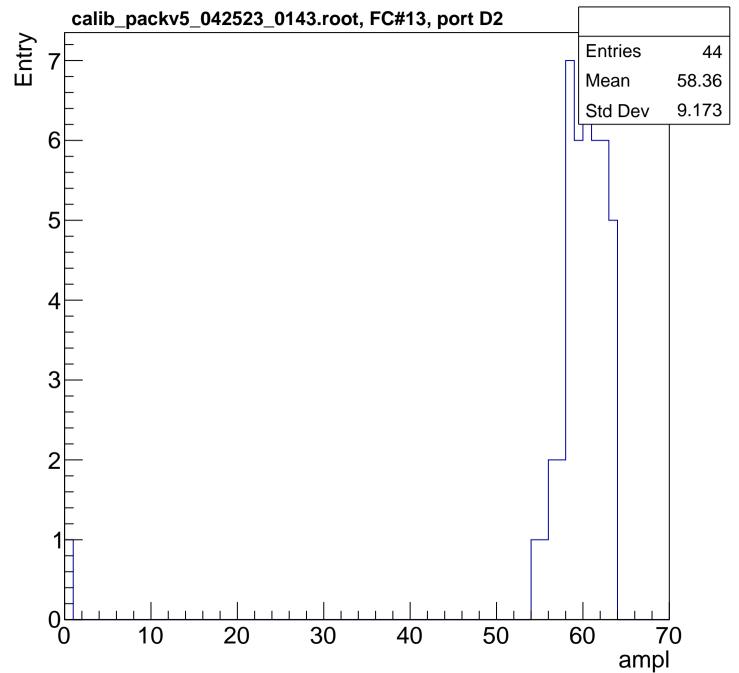


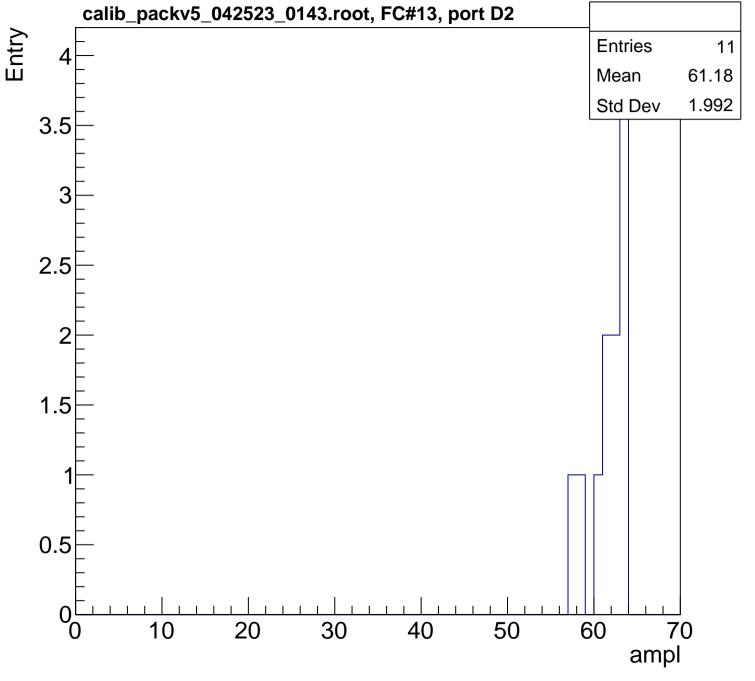




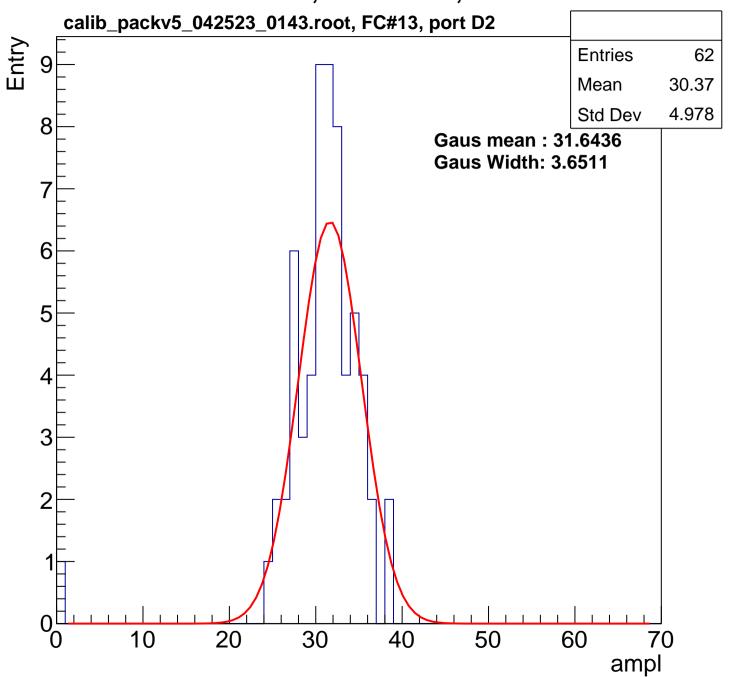


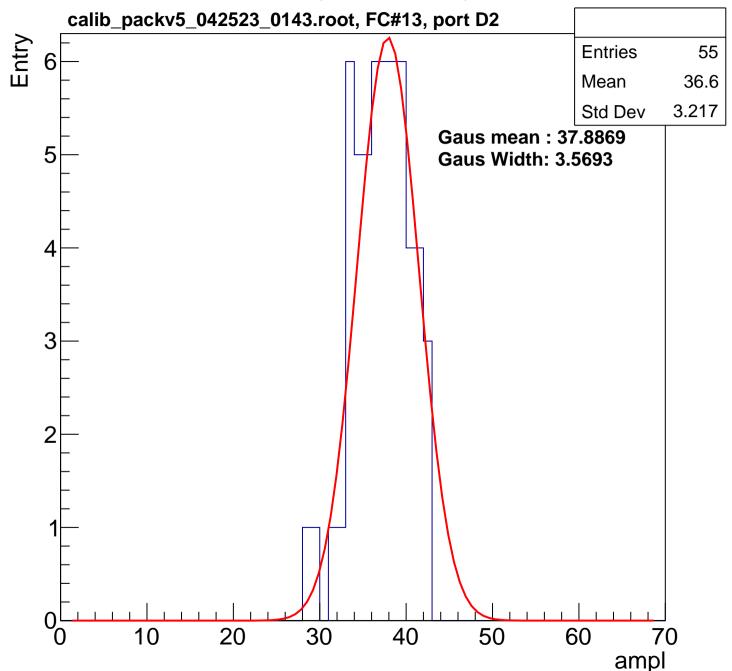


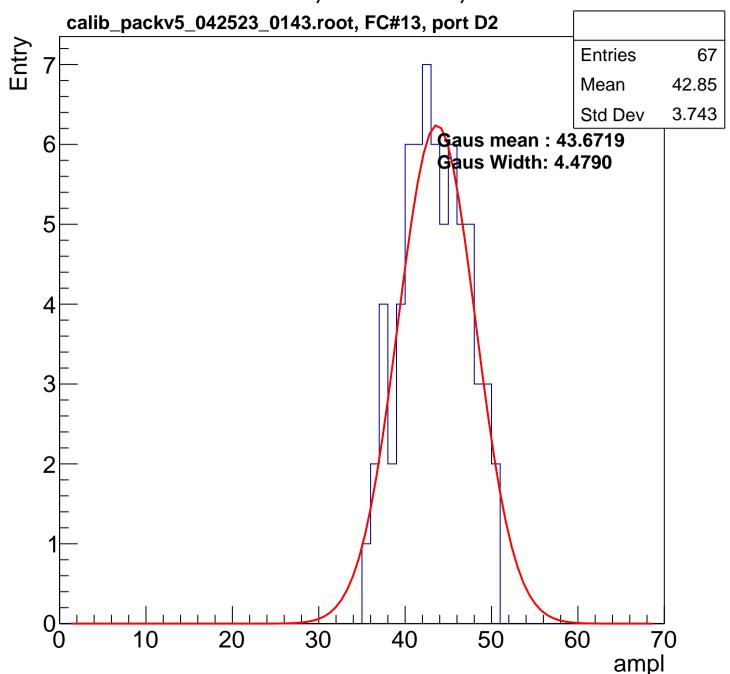


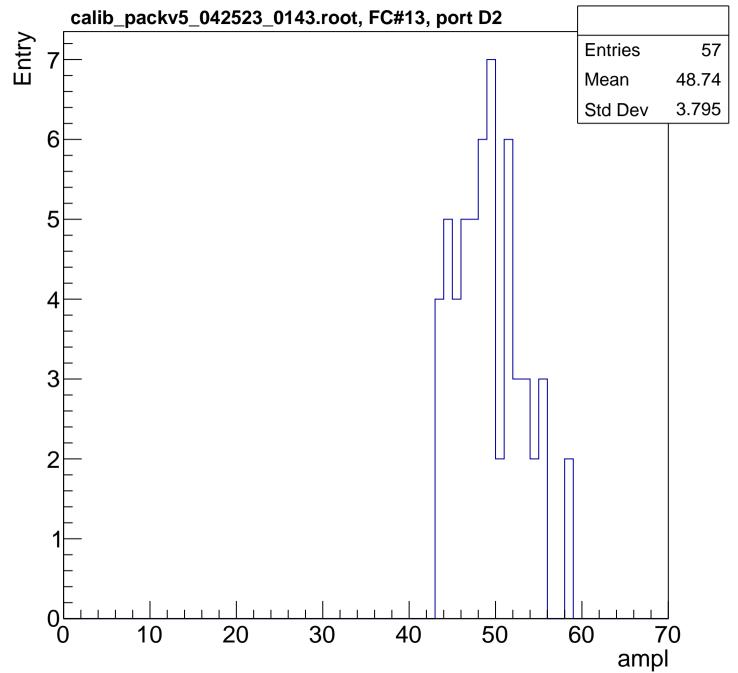


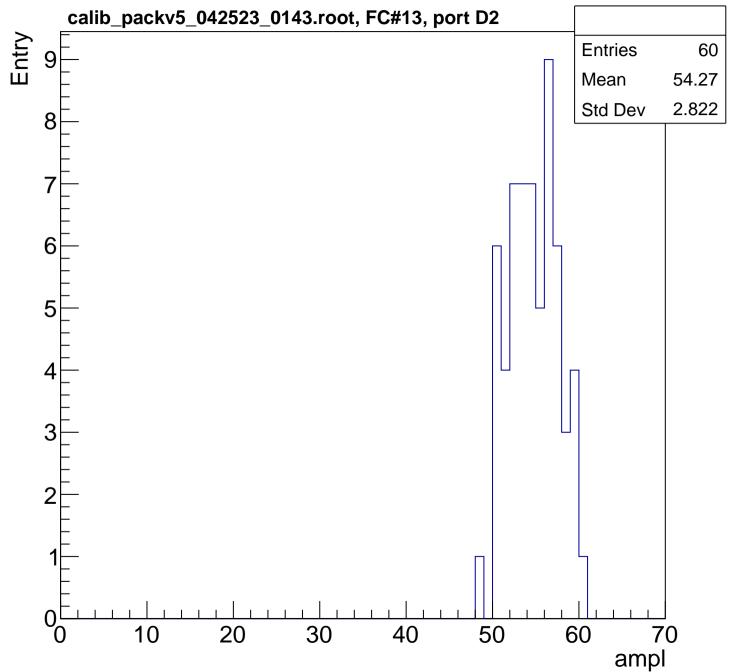
B1L003S, U7-ch91, adc7 calib_packv5_042523_0143.root, FC#13, port D2 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

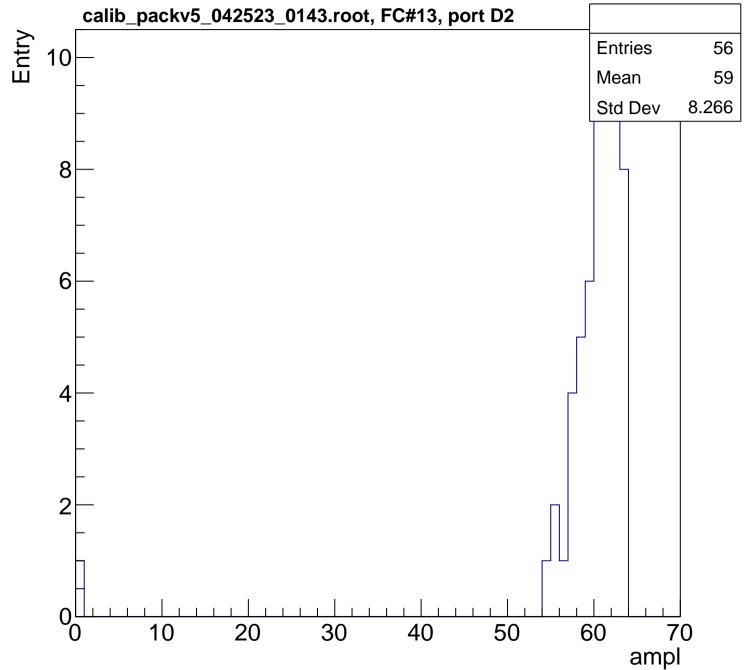


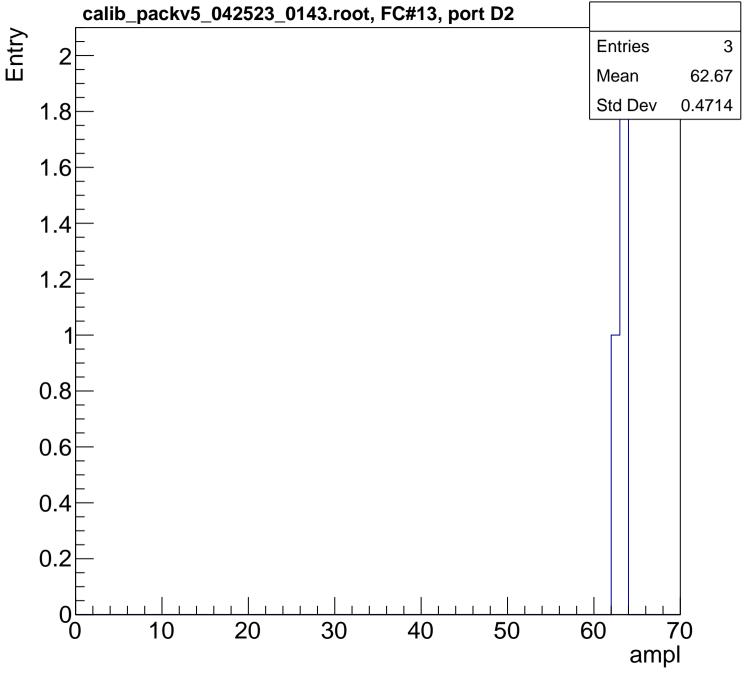




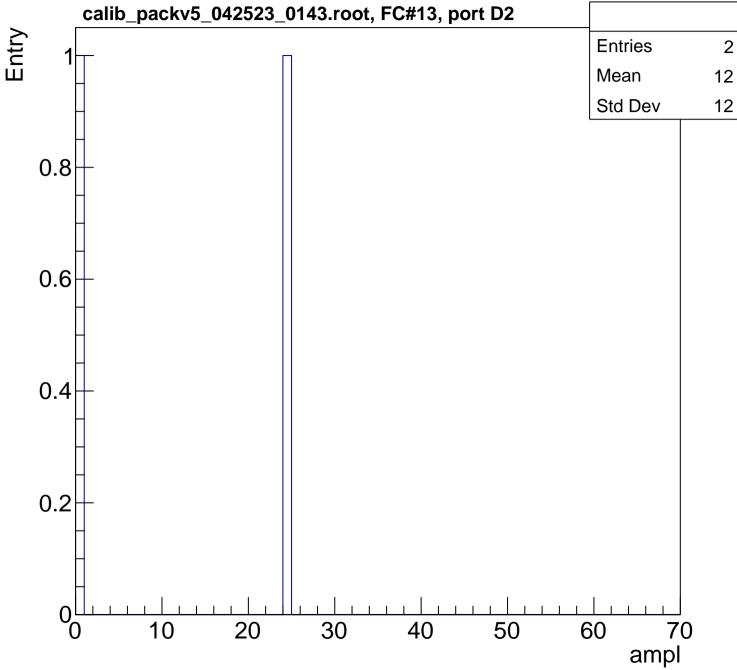


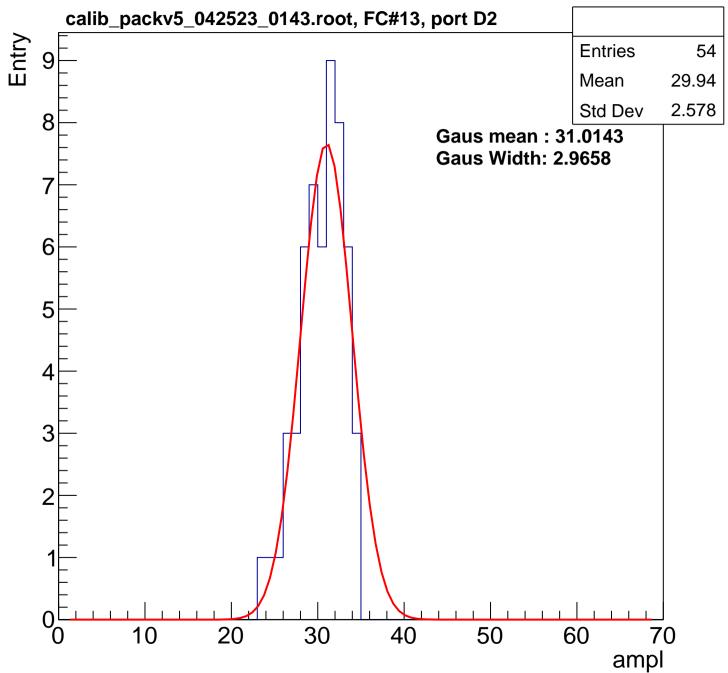


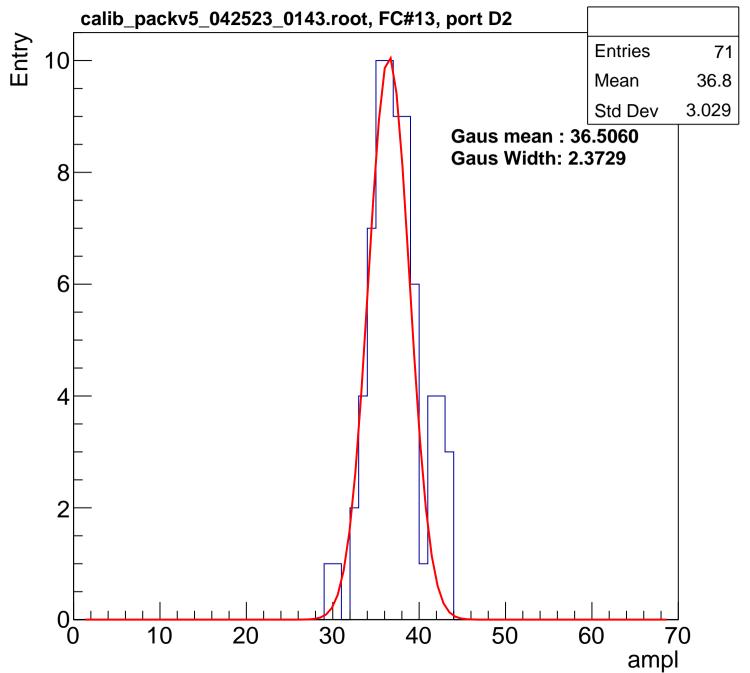


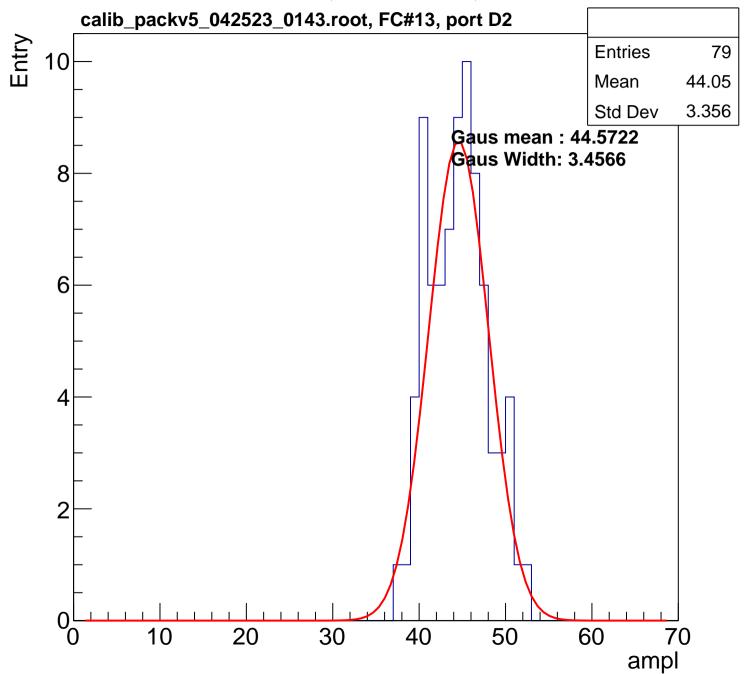


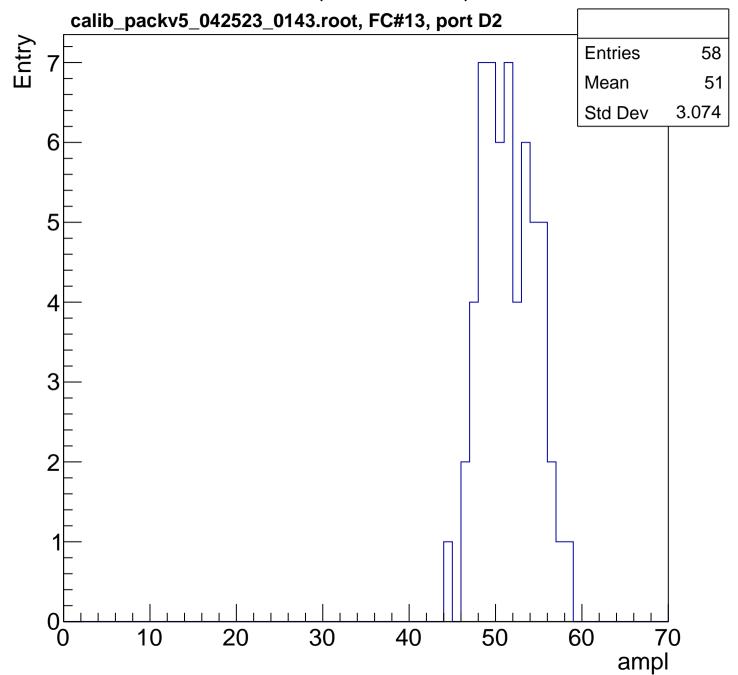
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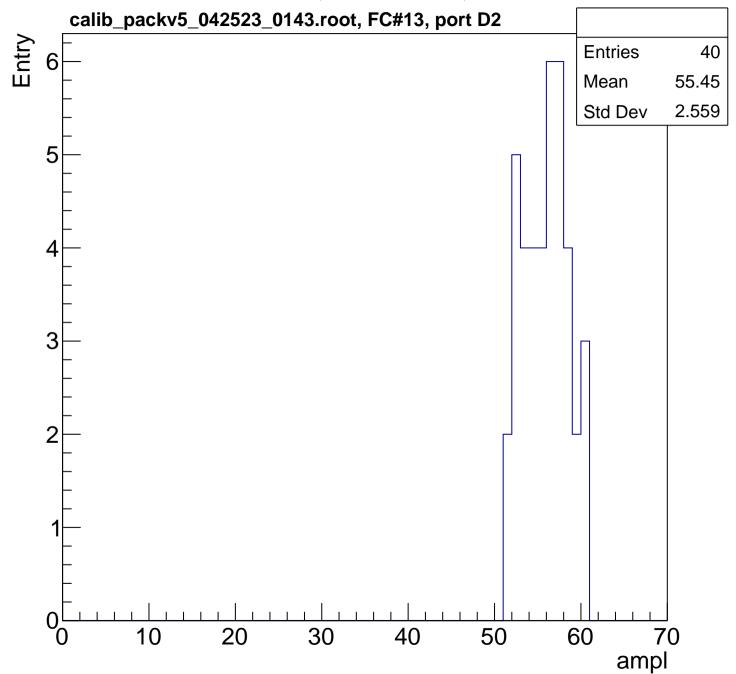


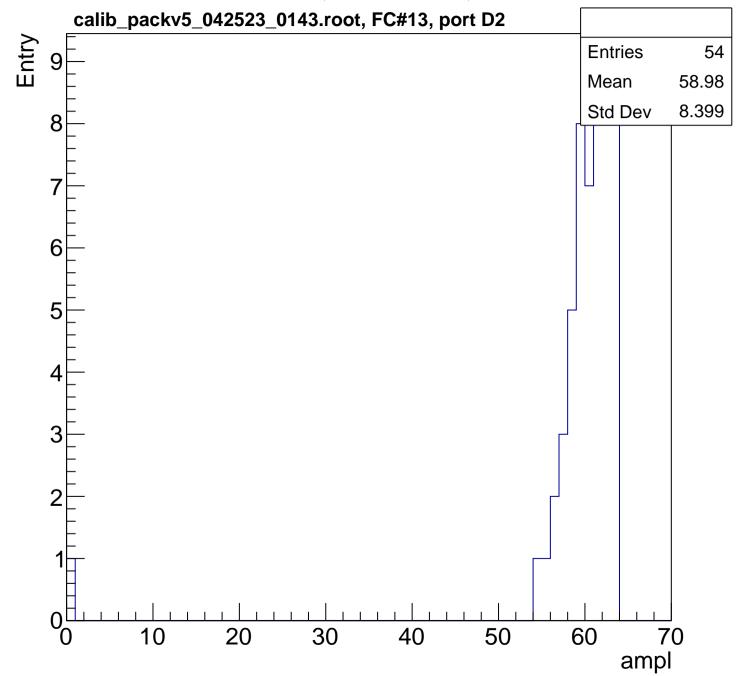


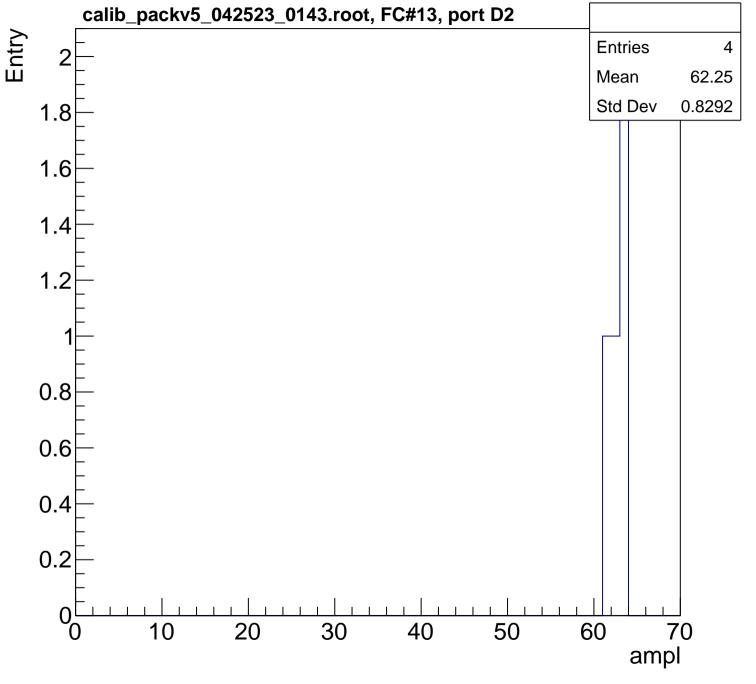


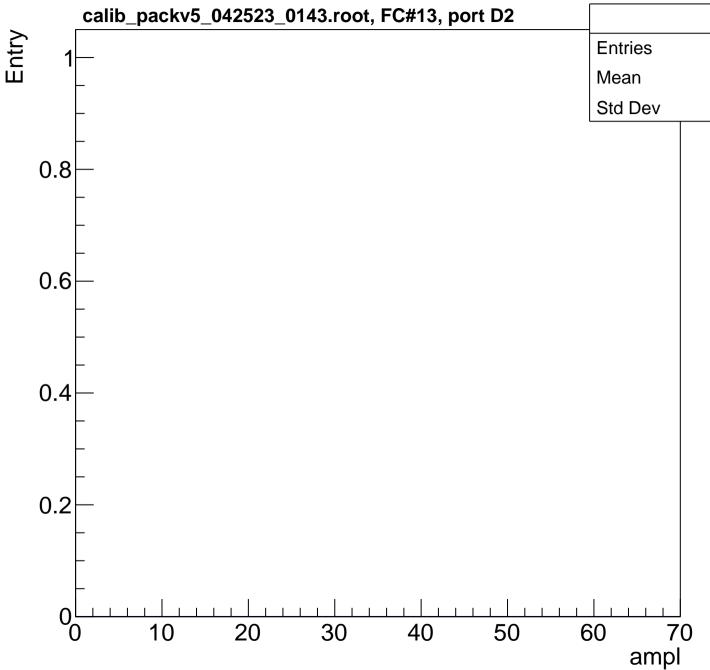


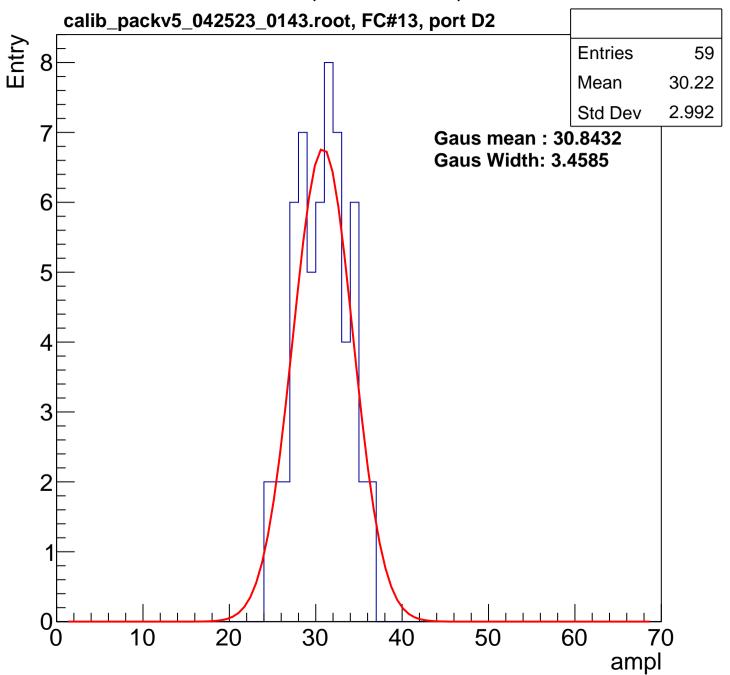


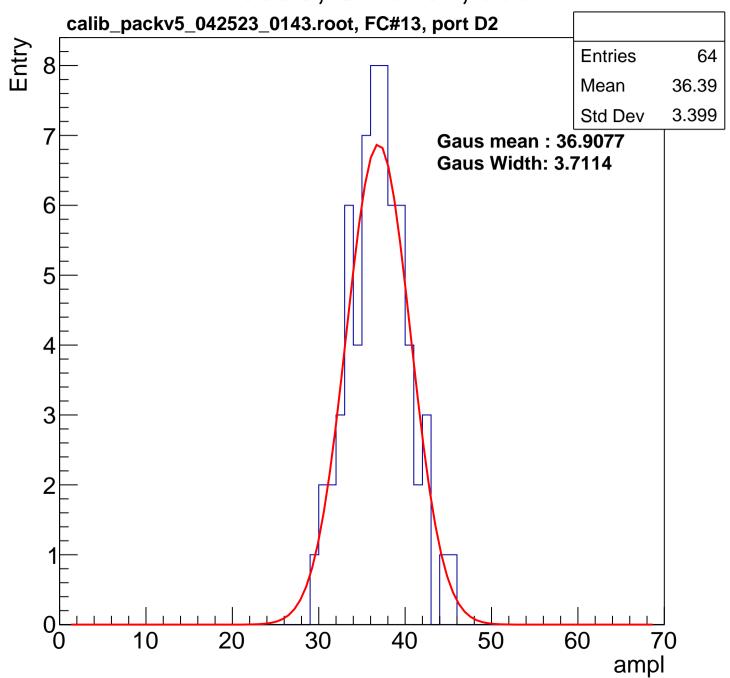


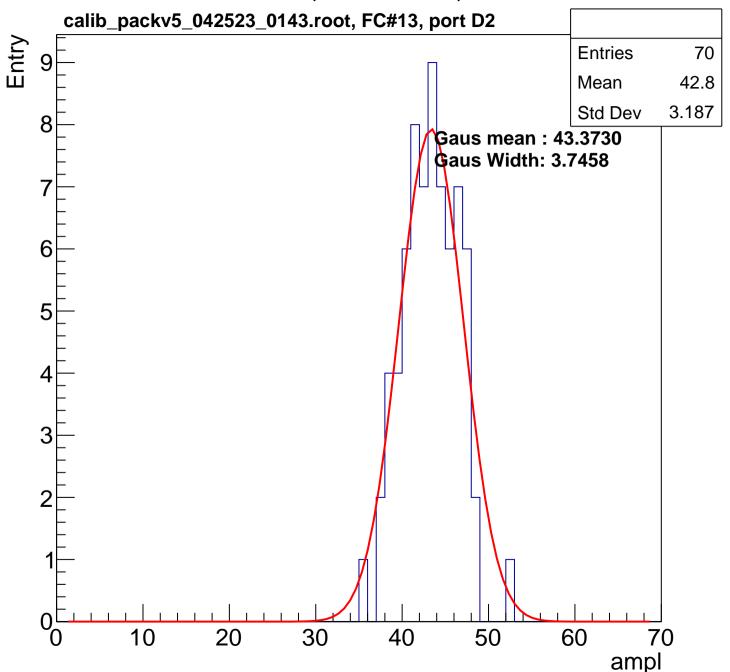


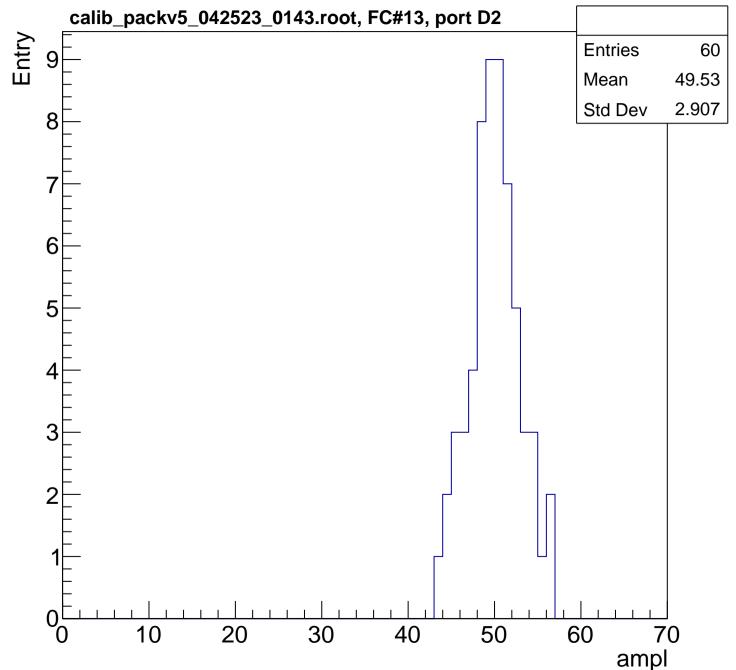


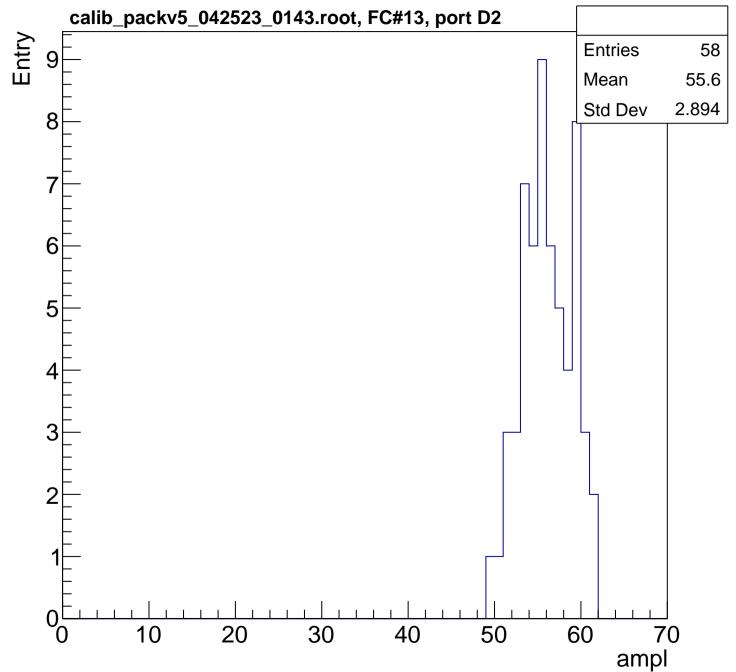


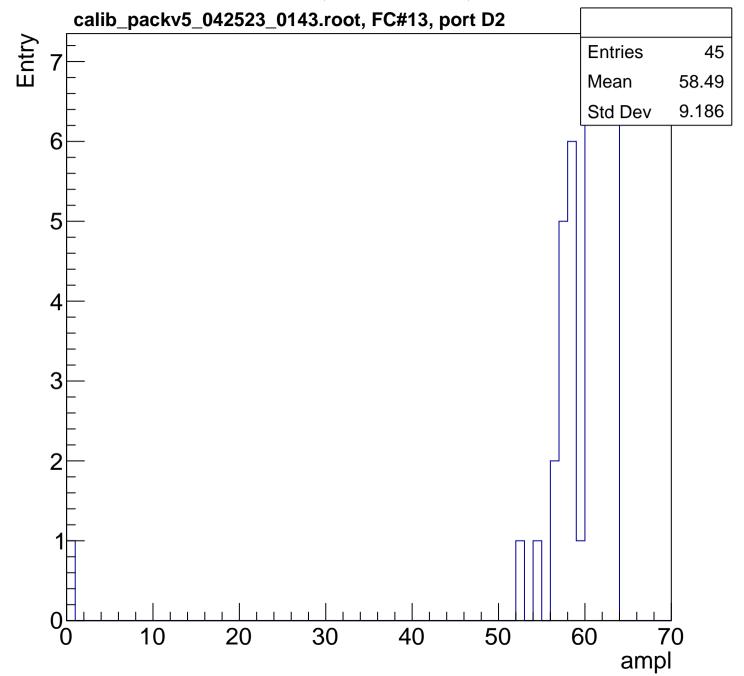


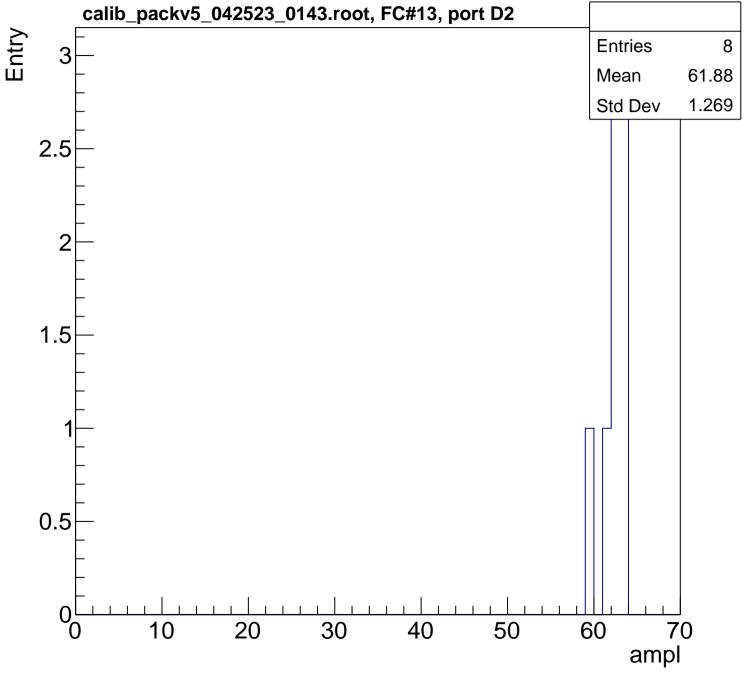




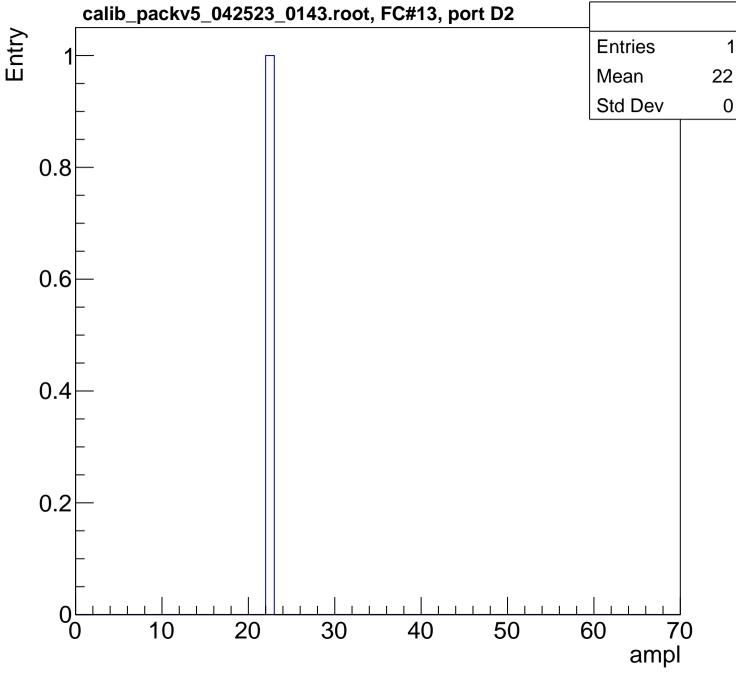


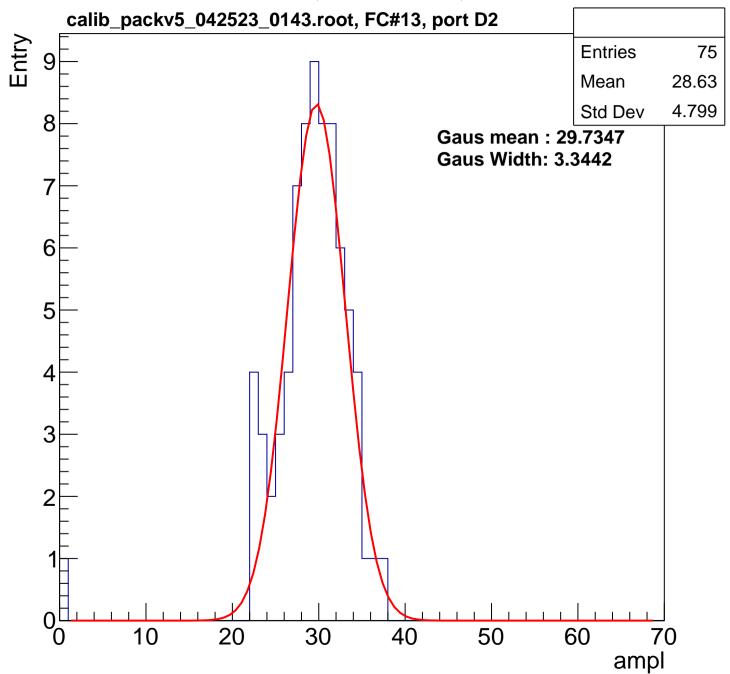


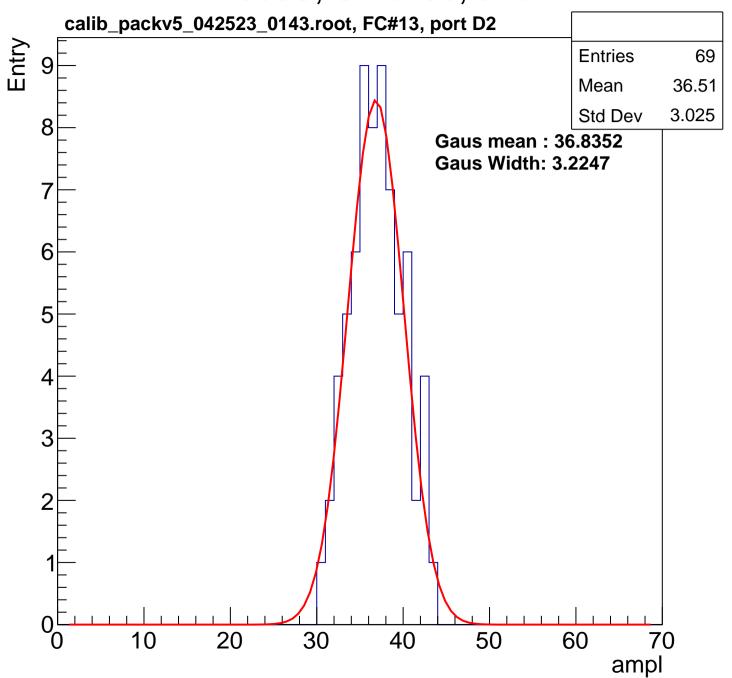


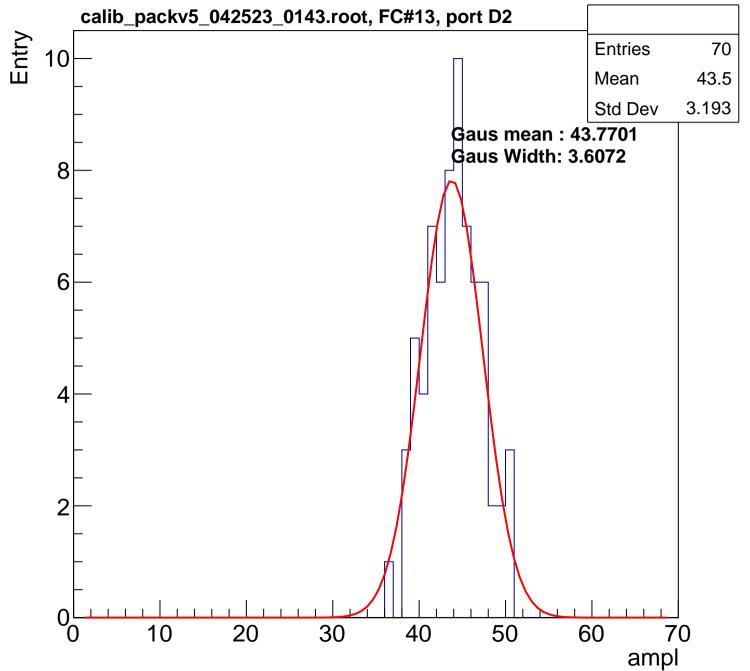


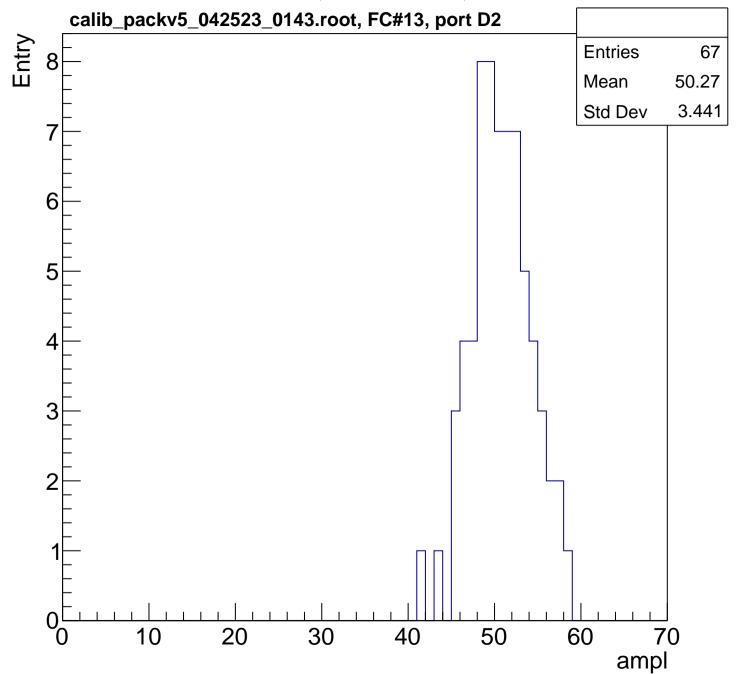
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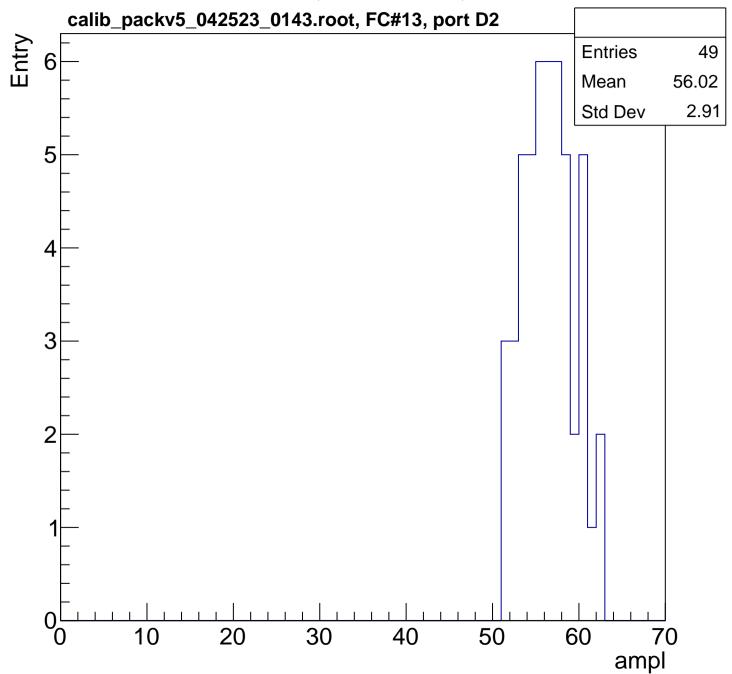


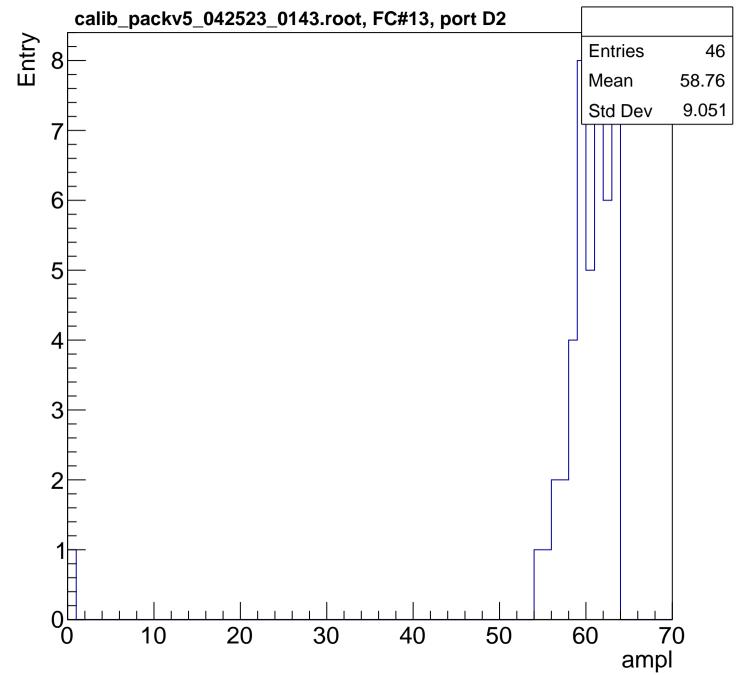


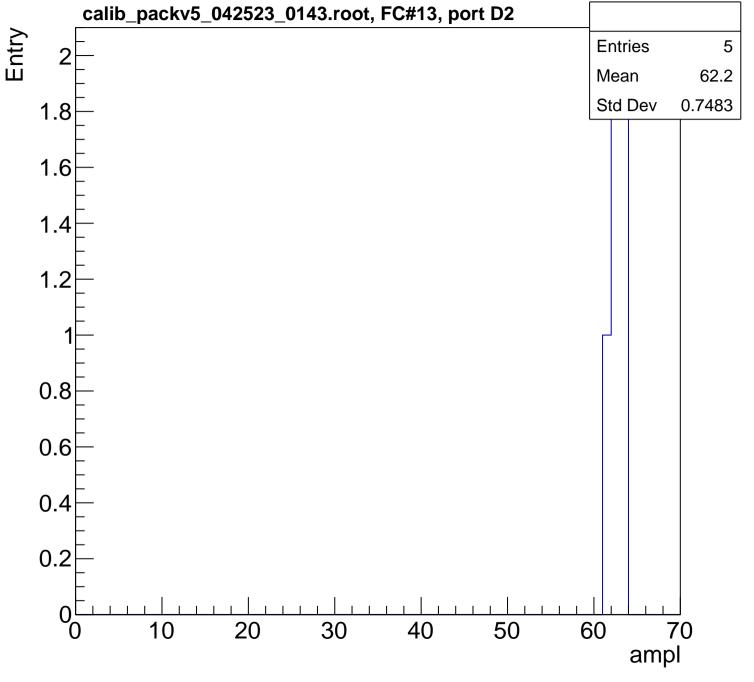


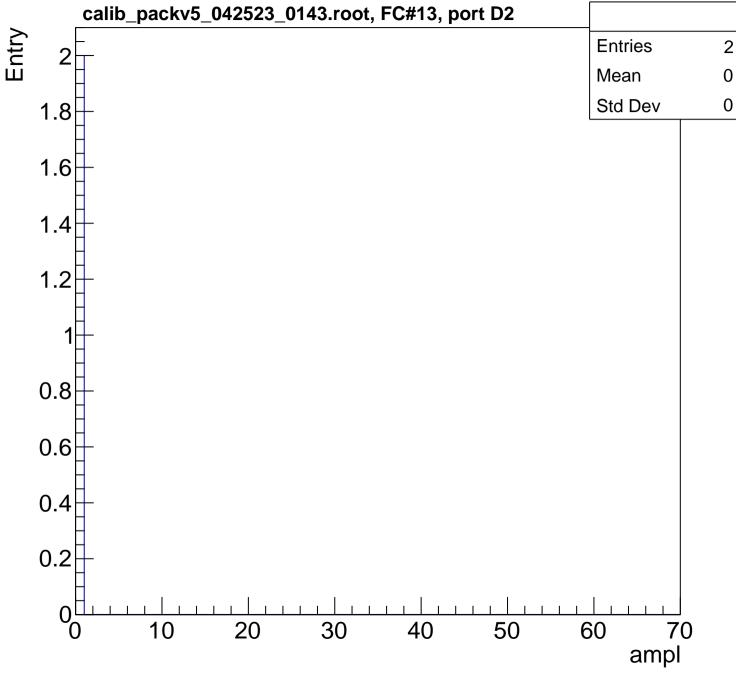


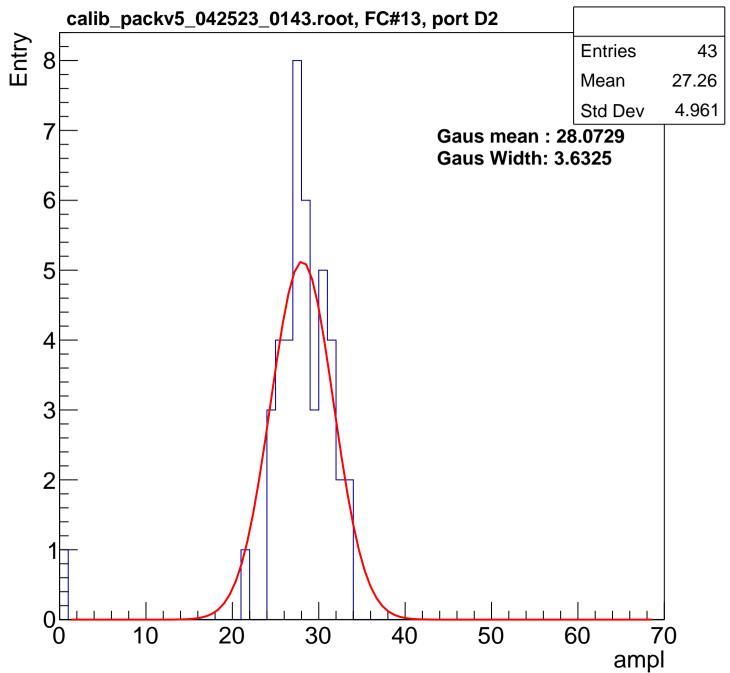


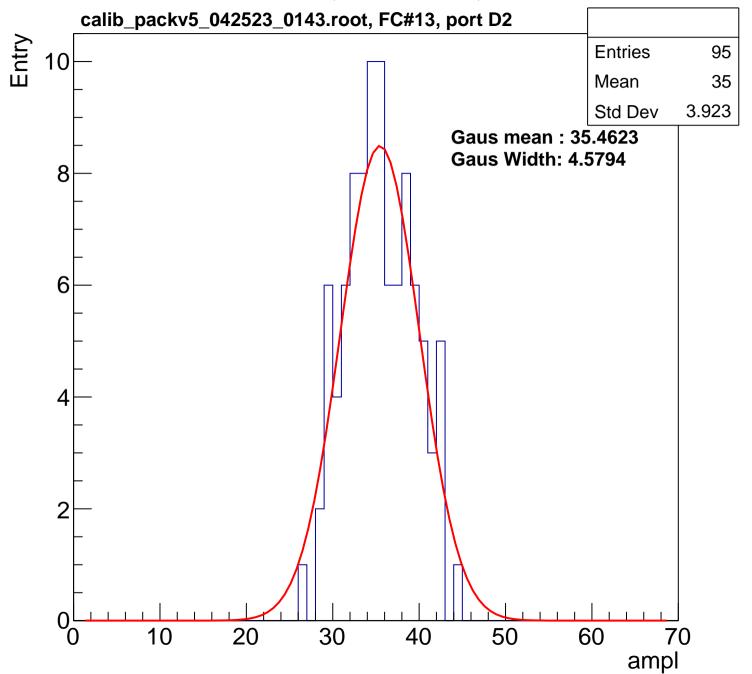


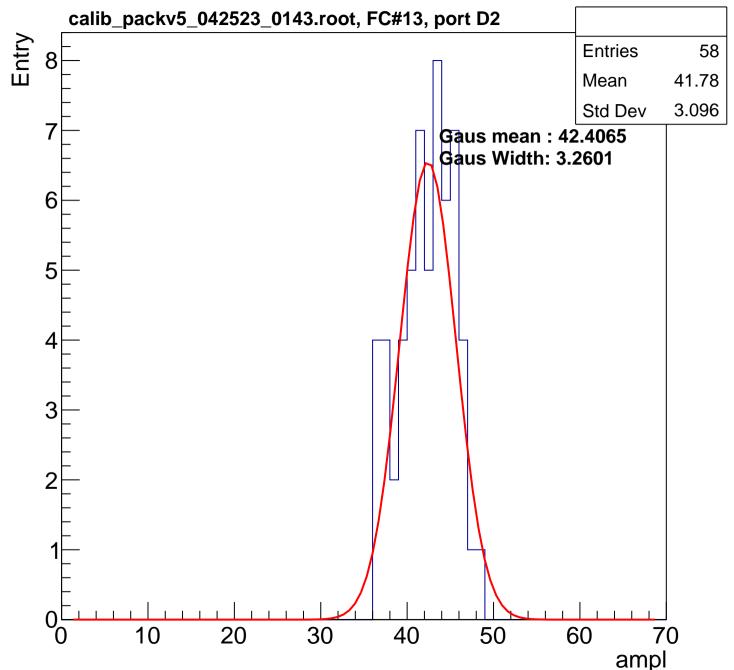


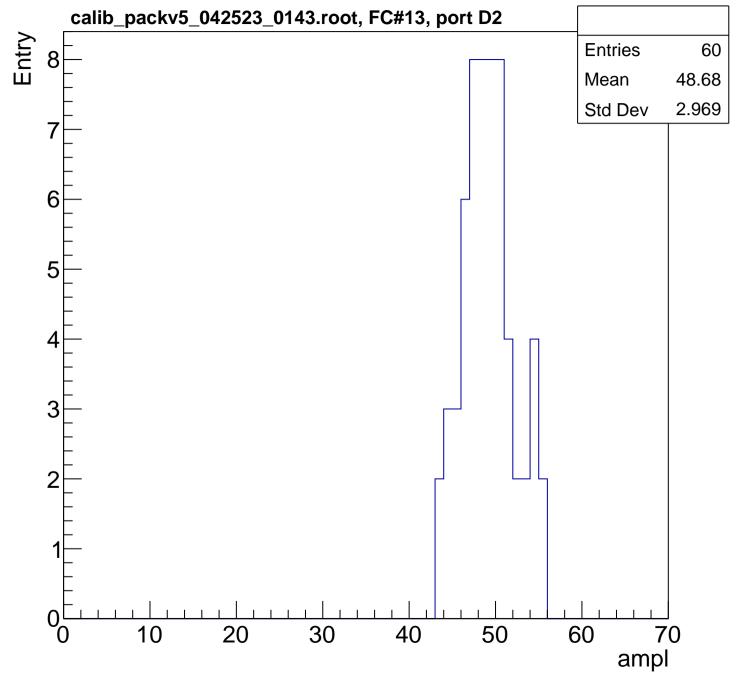


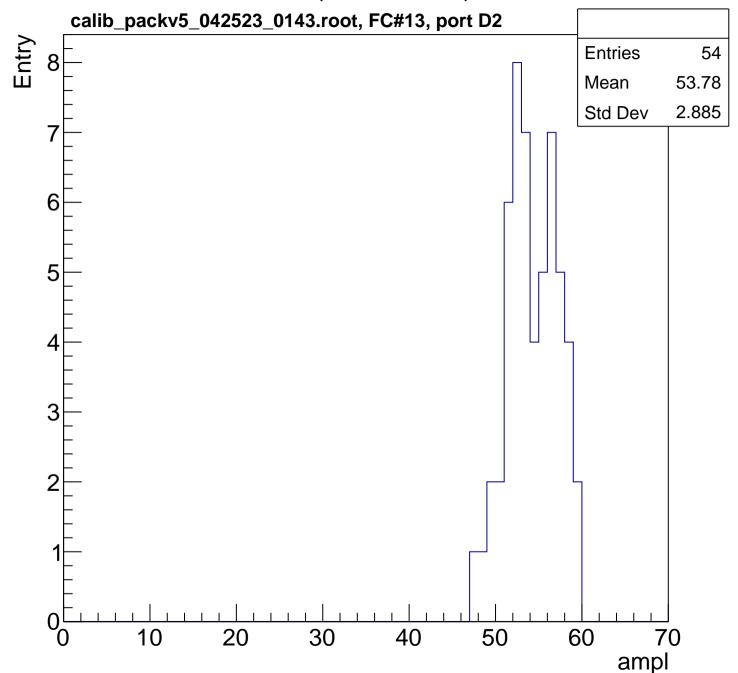


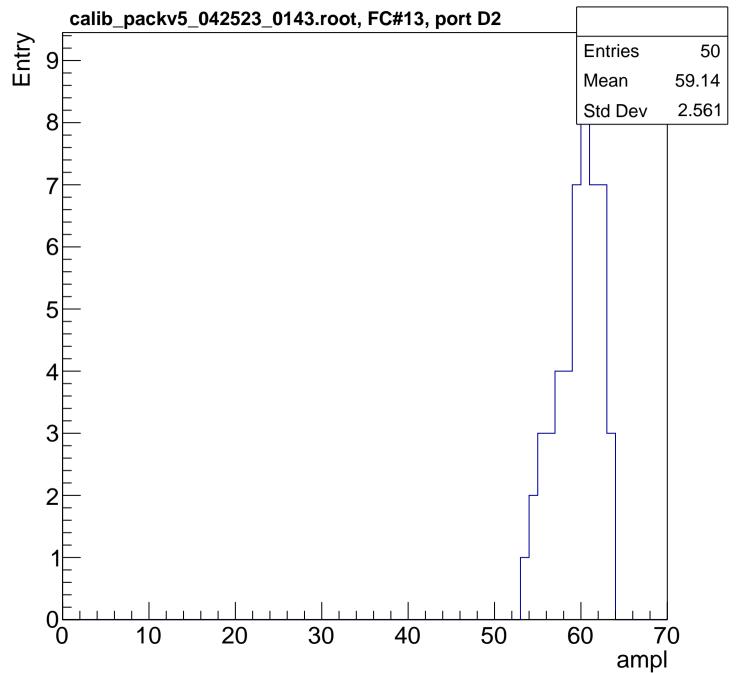


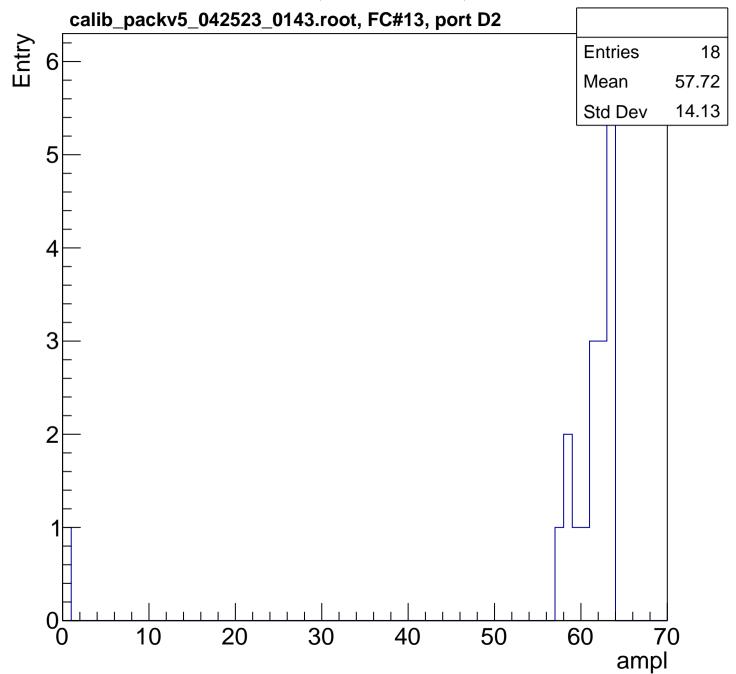


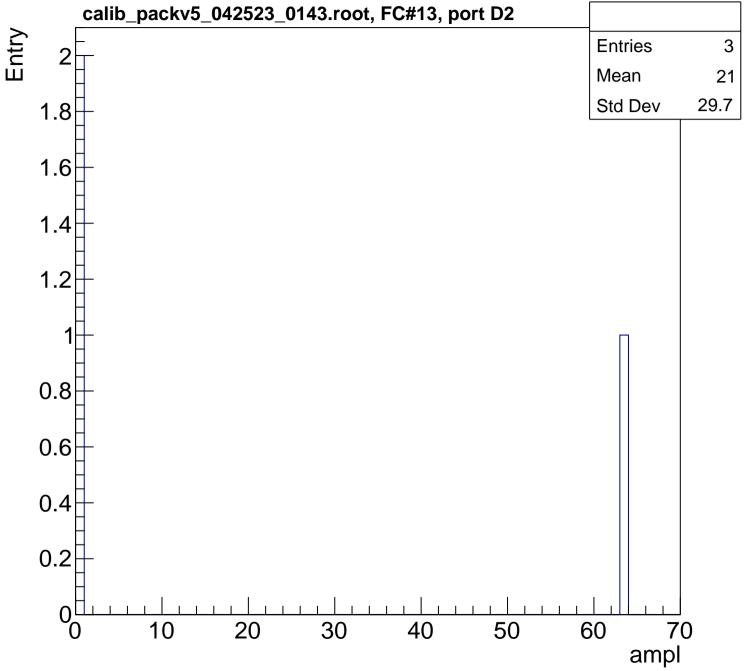


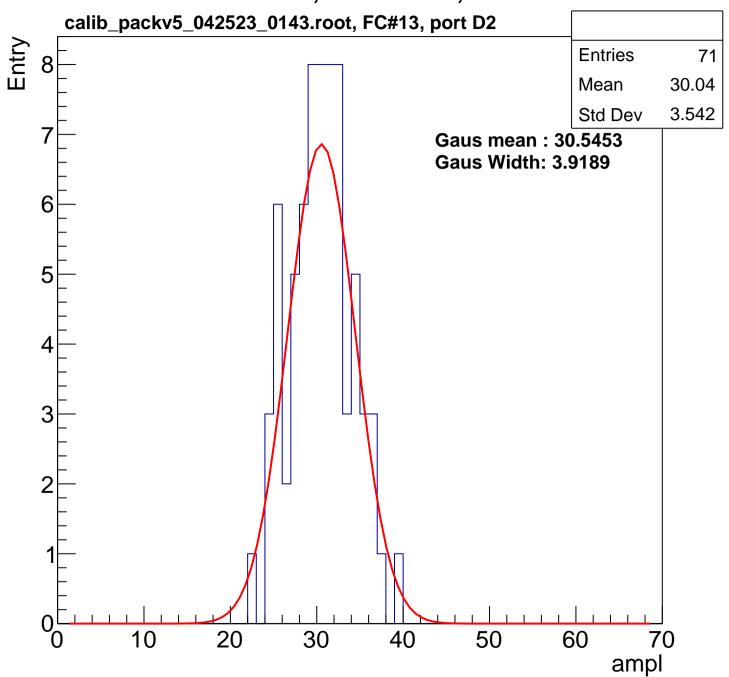


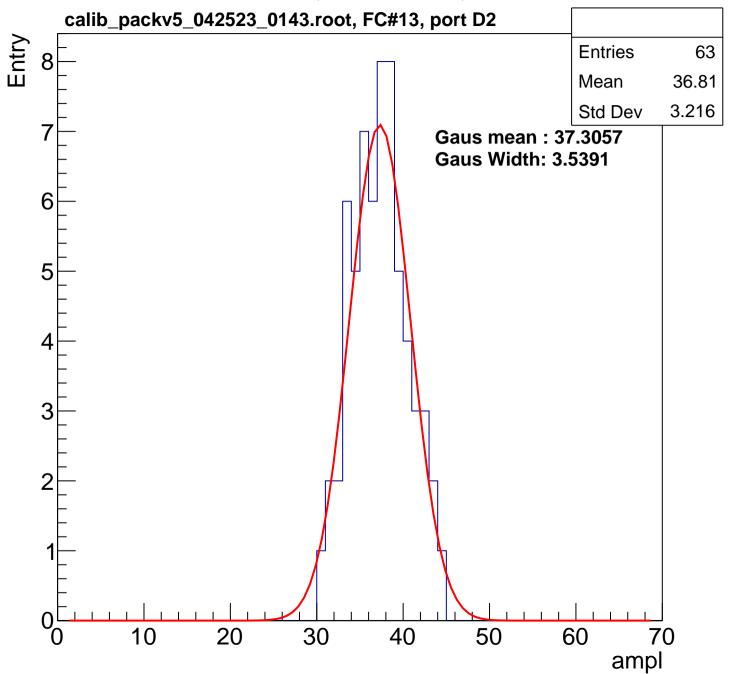


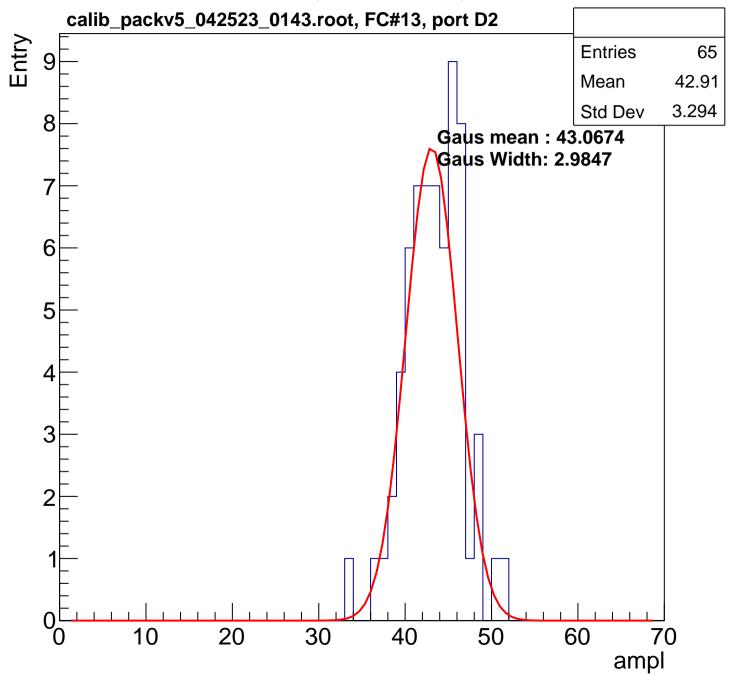


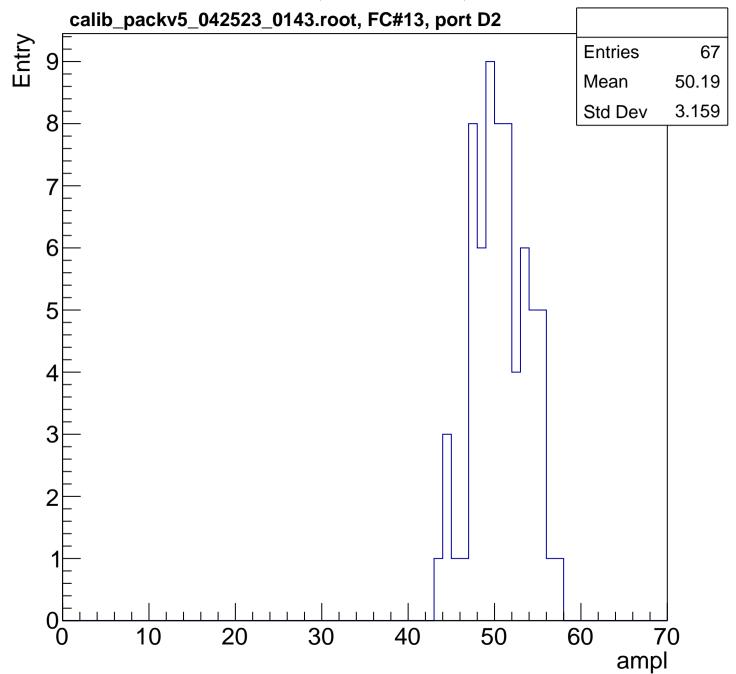


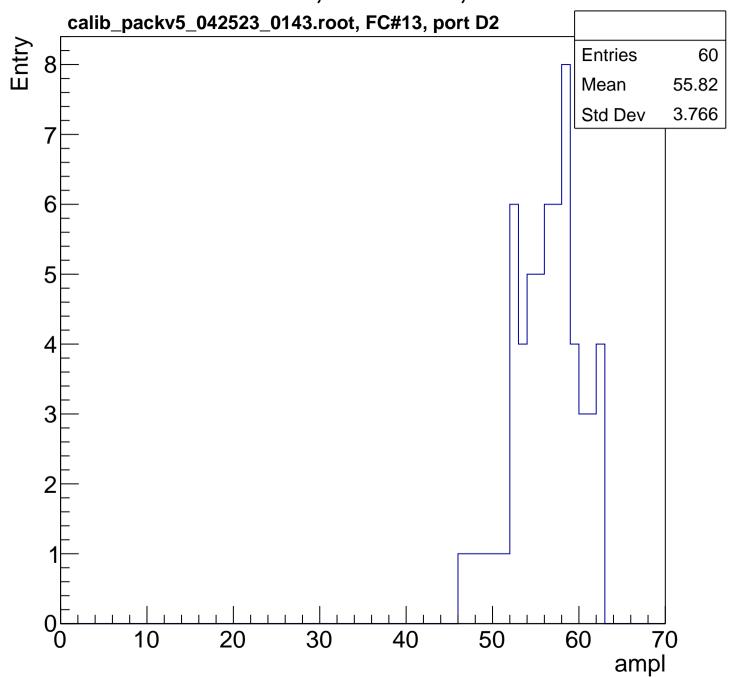


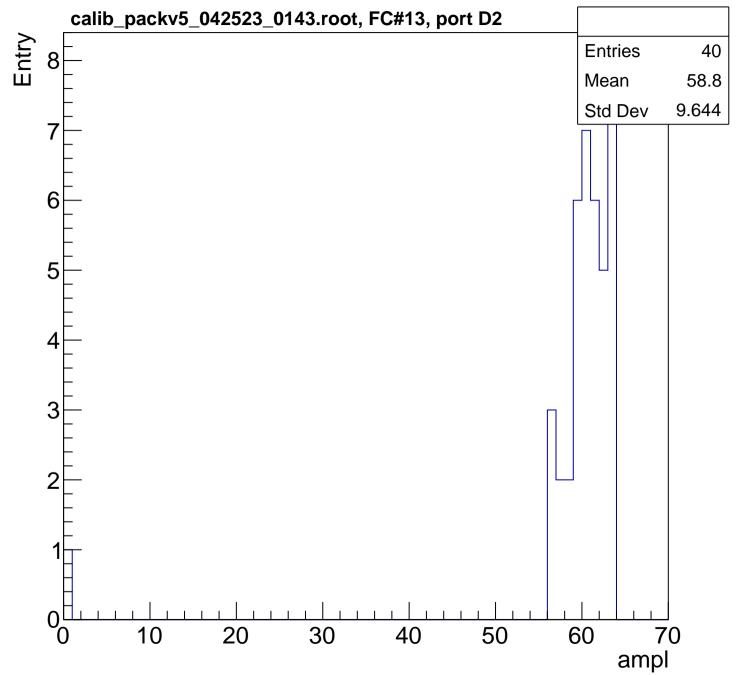


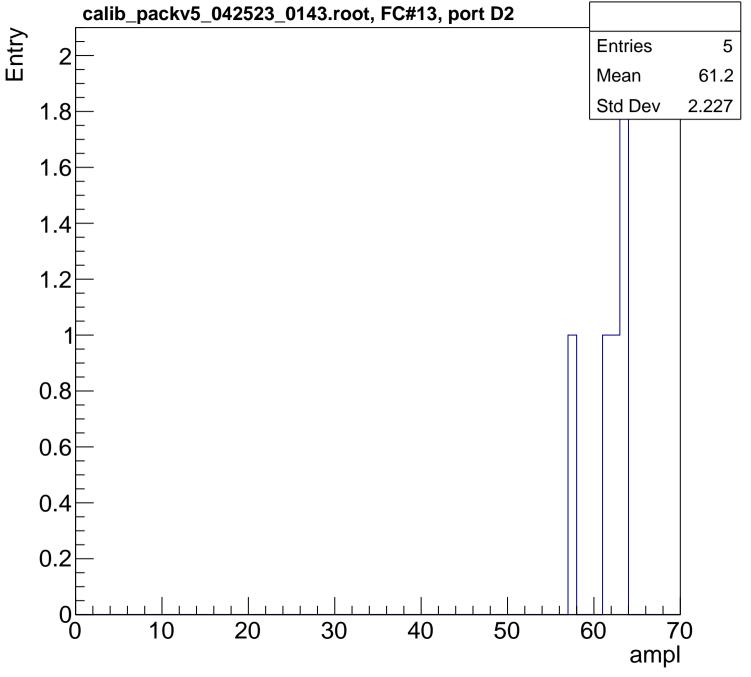




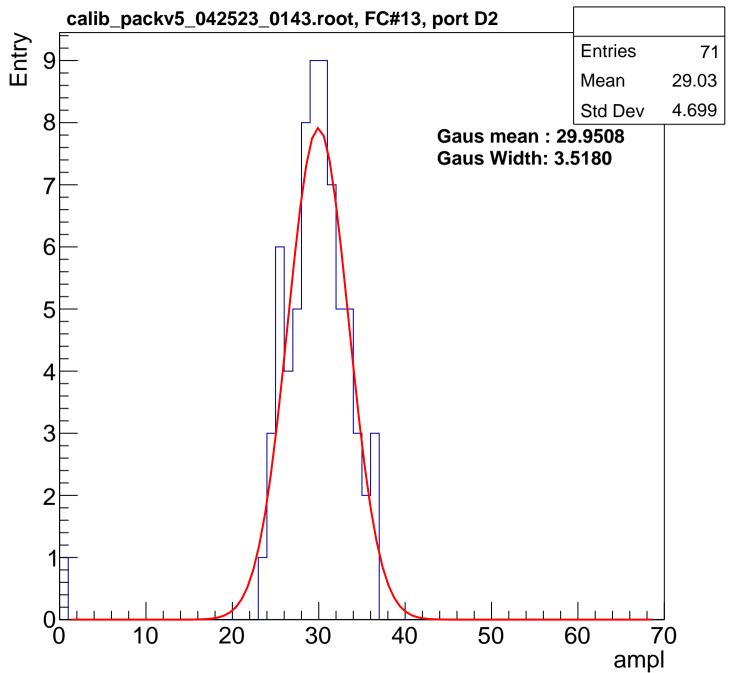


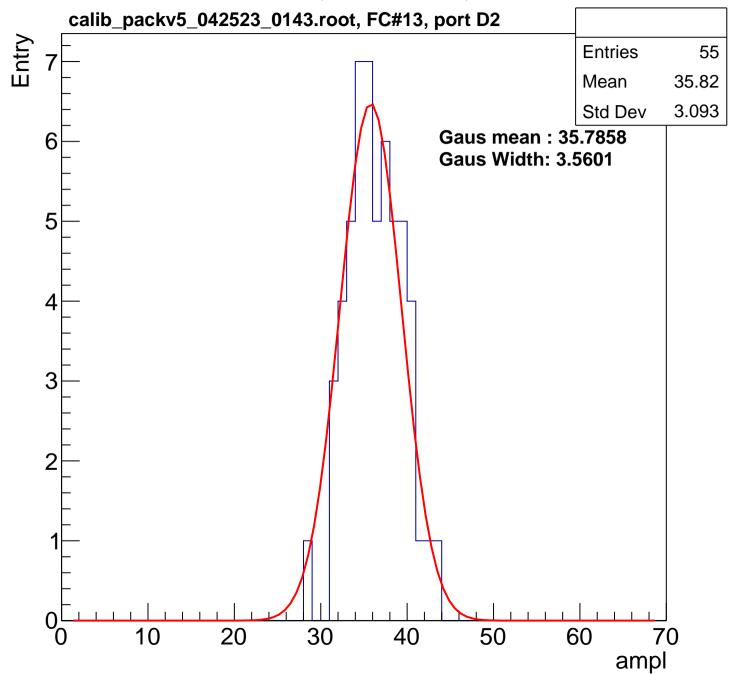


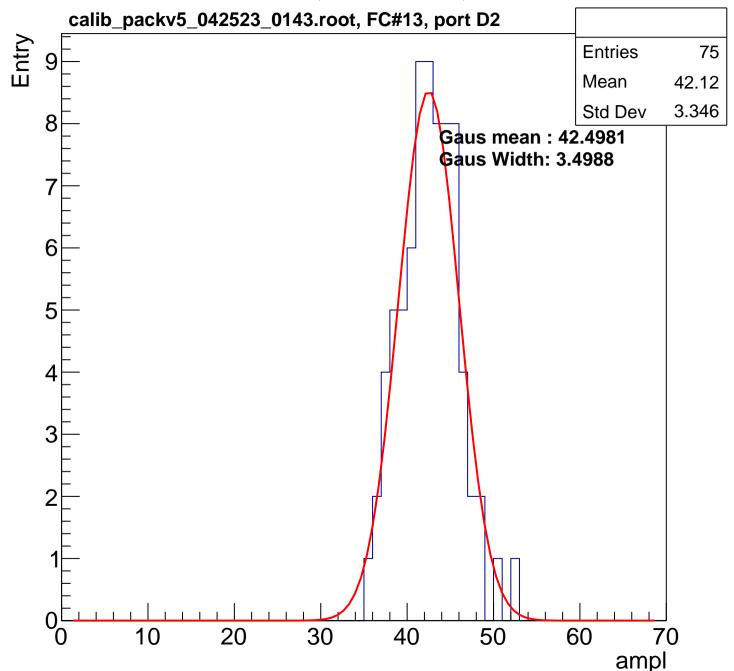


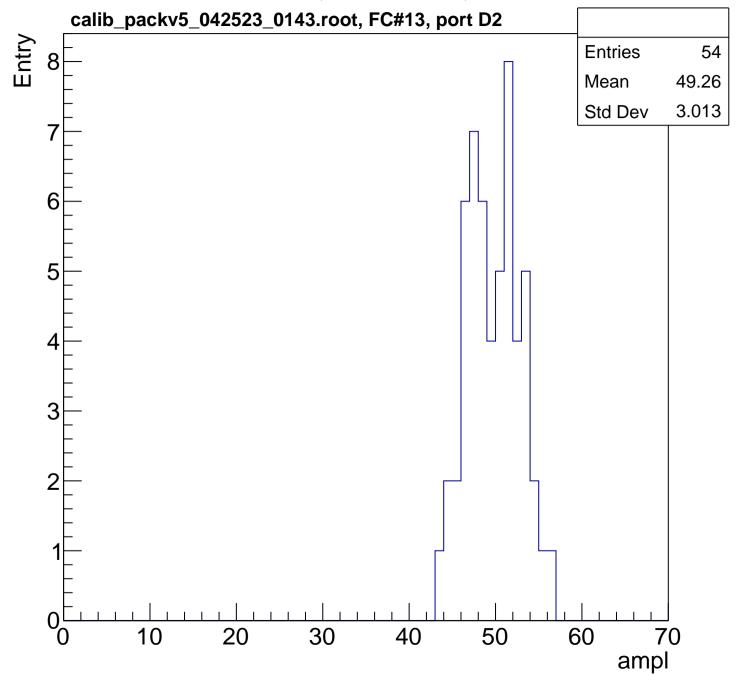


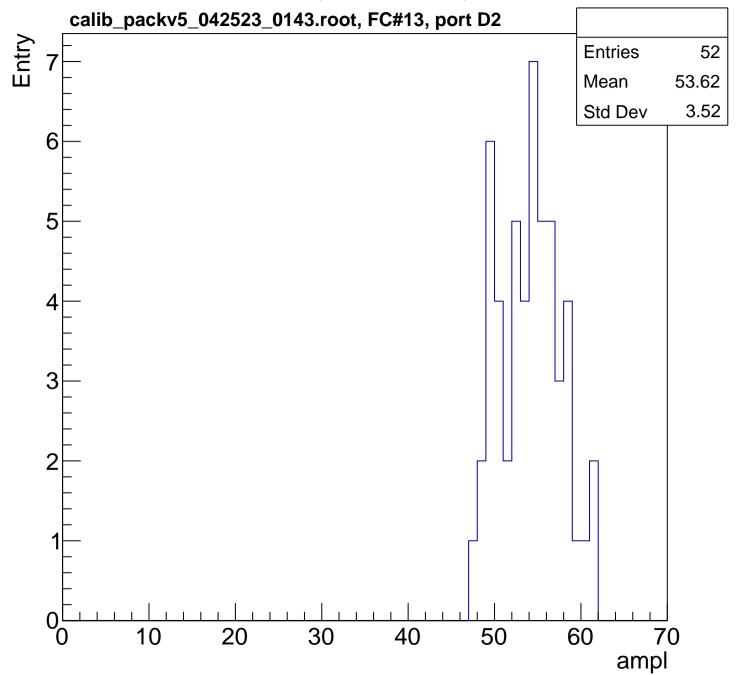


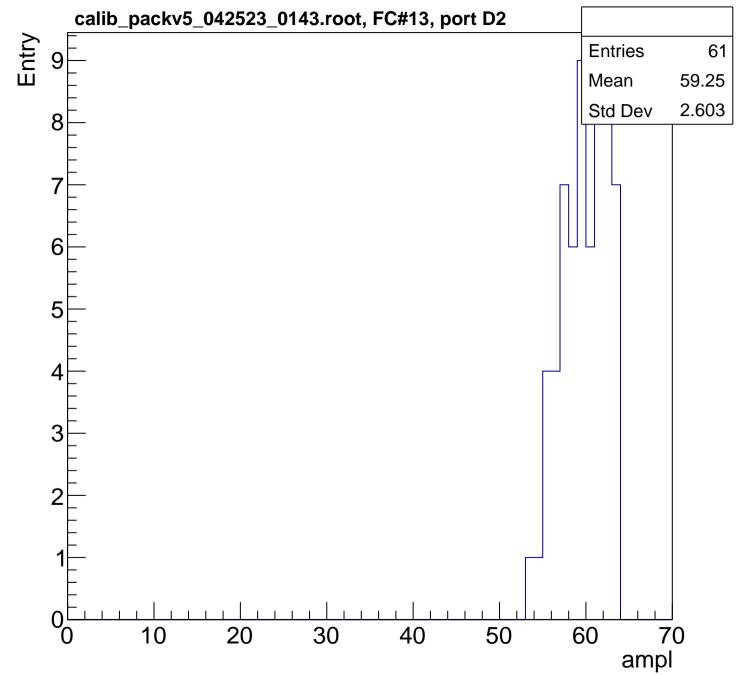


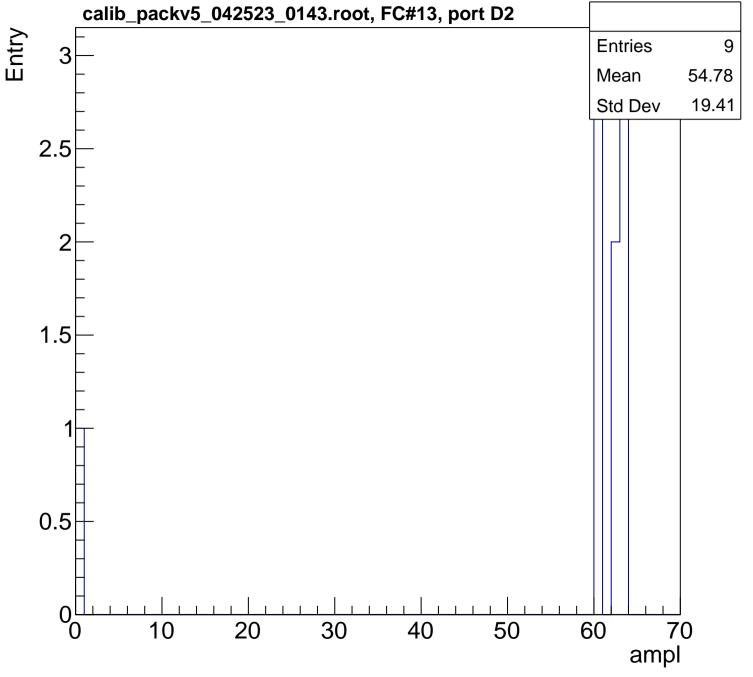


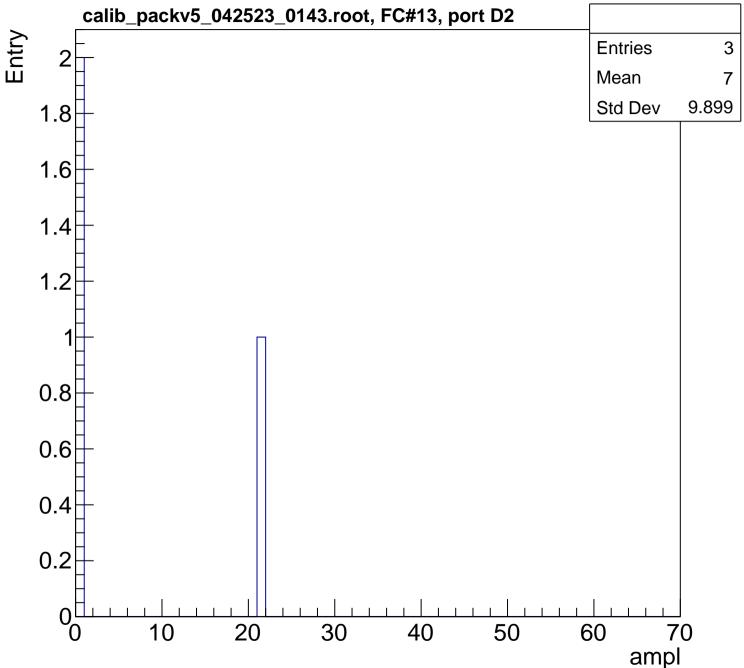


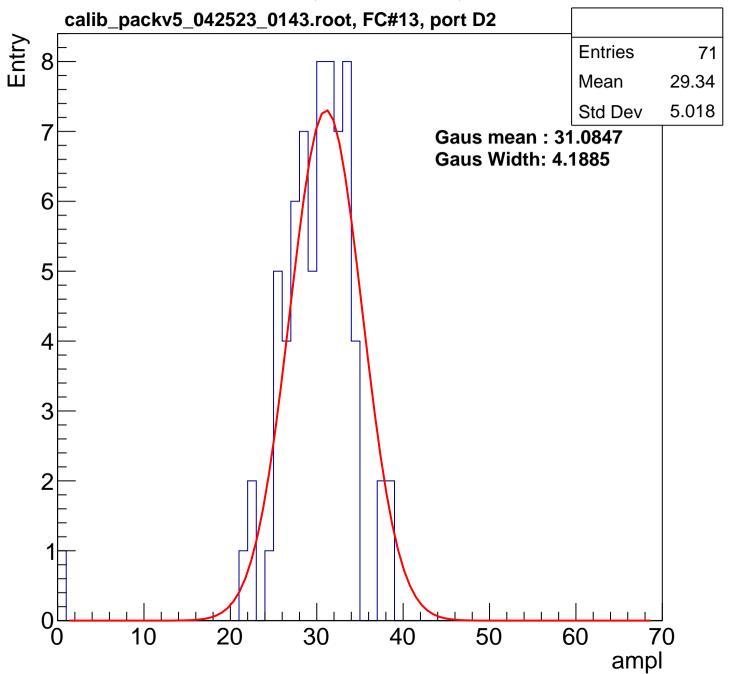


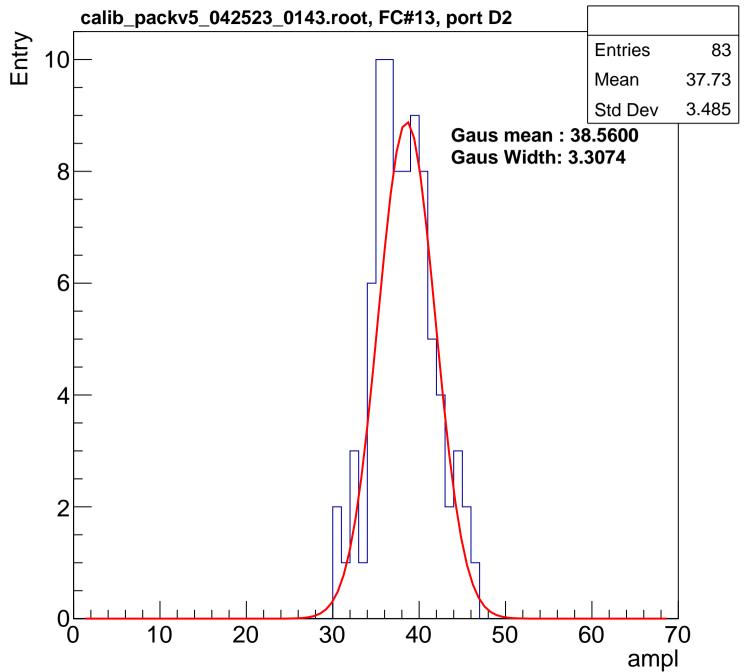


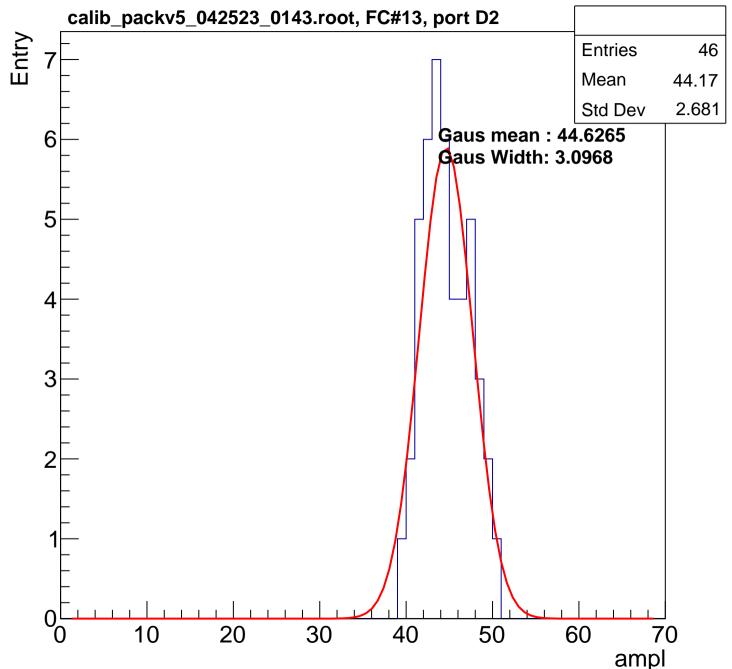


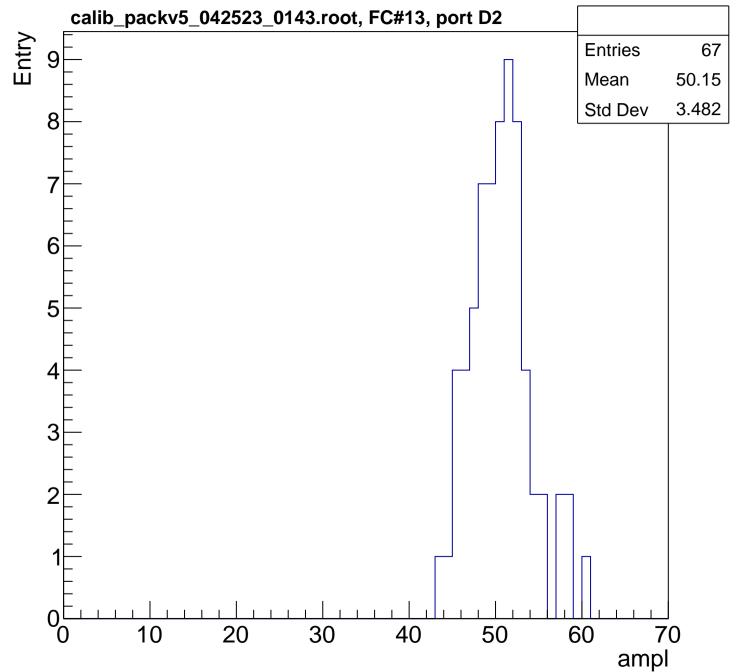


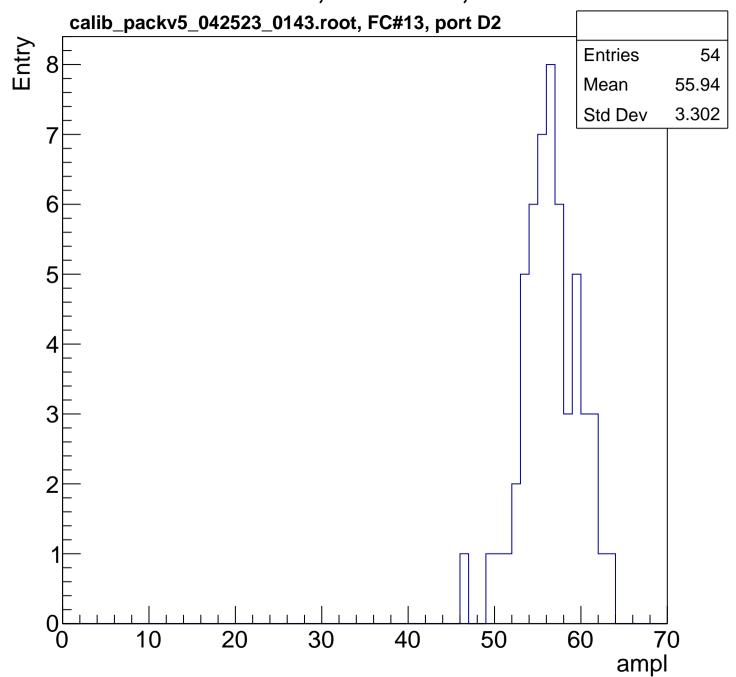


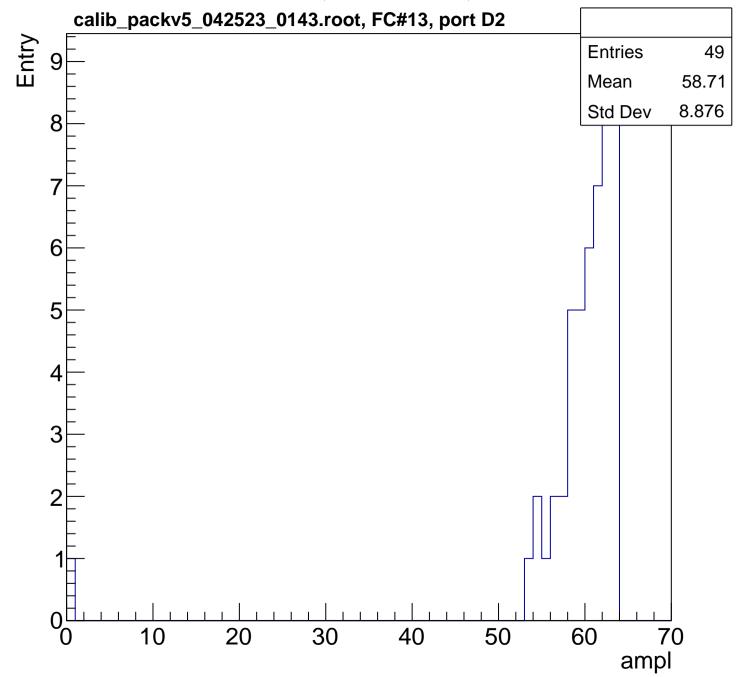




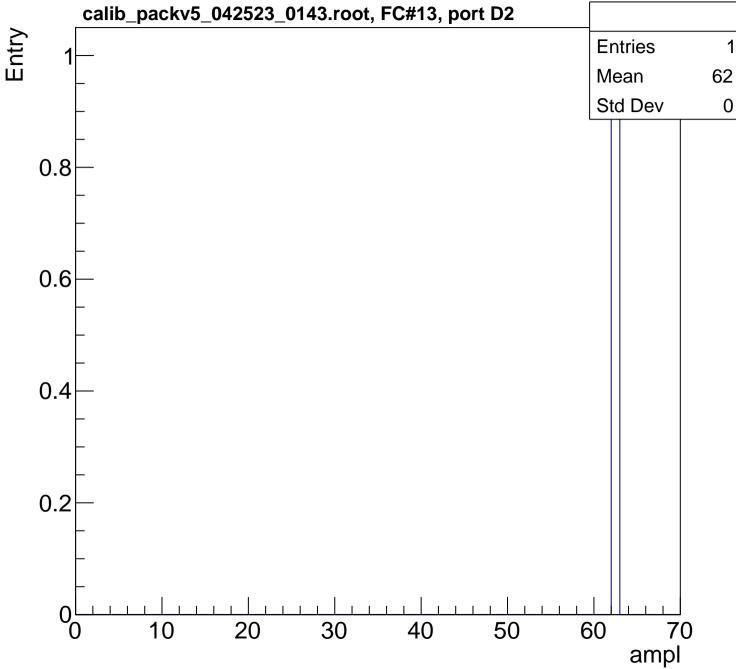




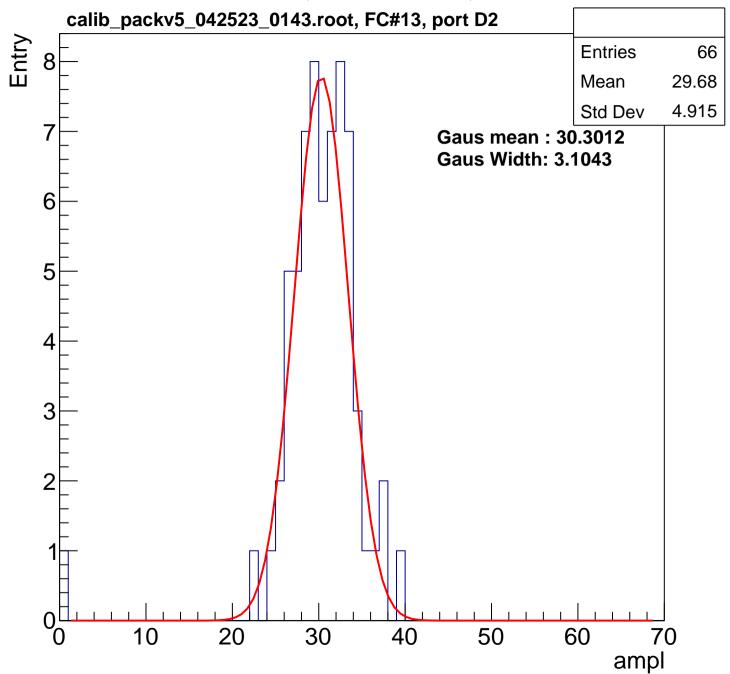


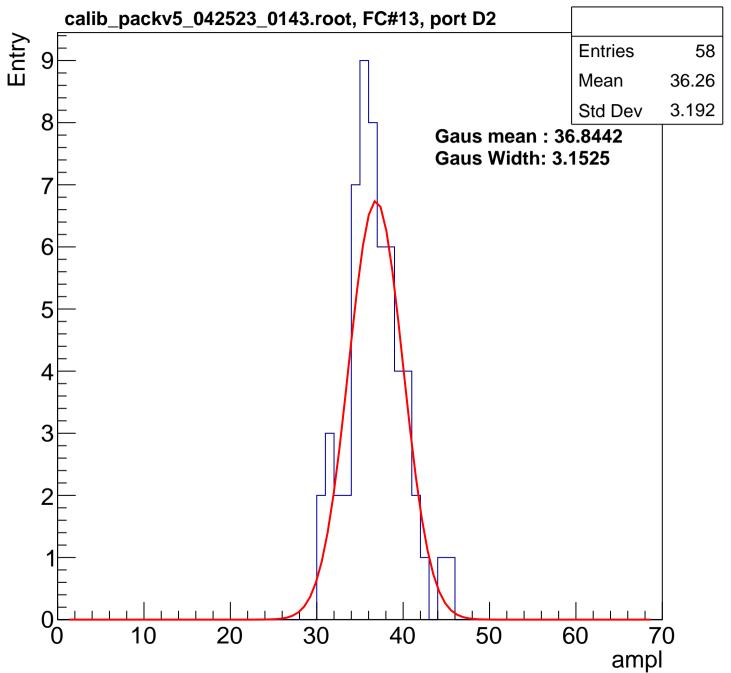


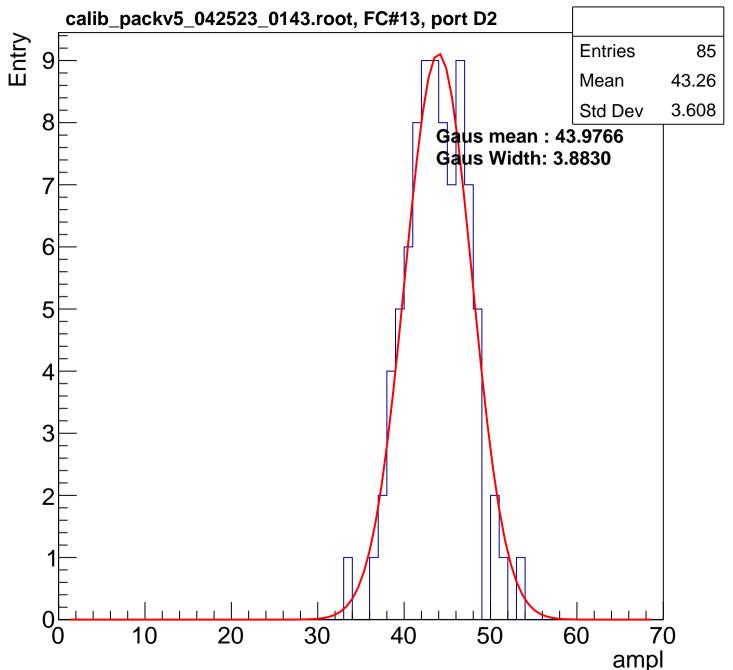
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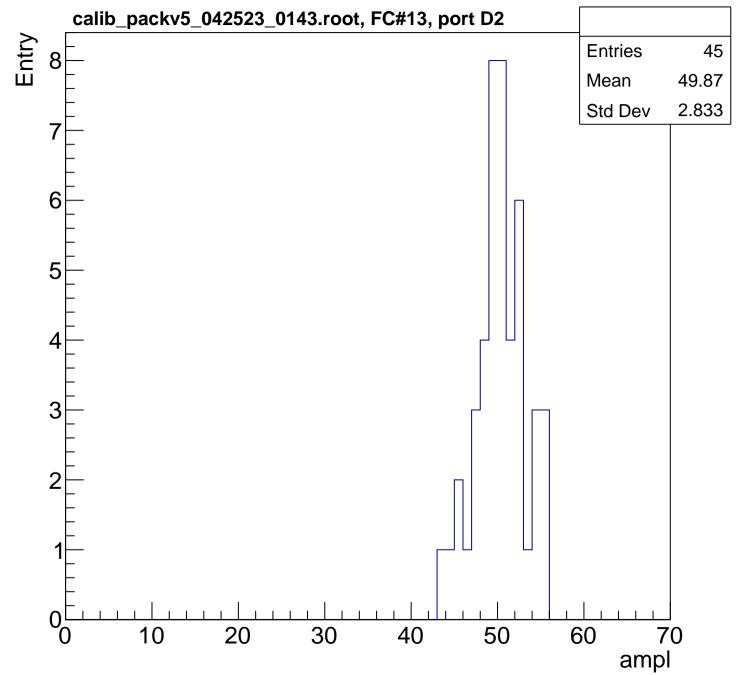


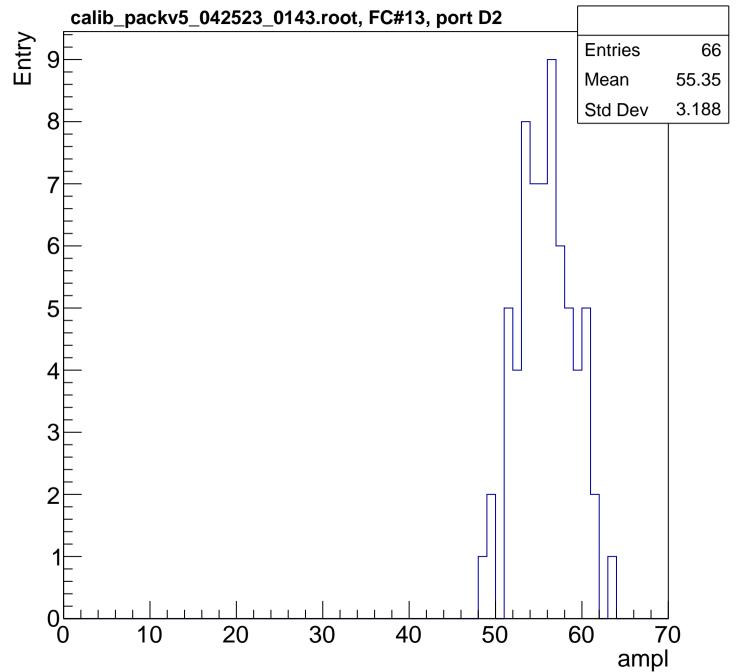
B1L003S, U7-ch99, adc7 calib_packv5_042523_0143.root, FC#13, port D2 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

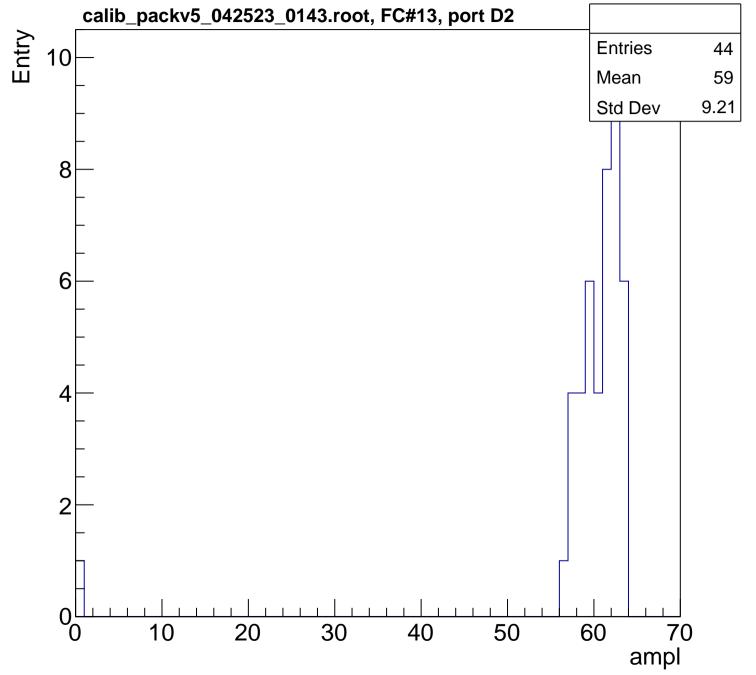


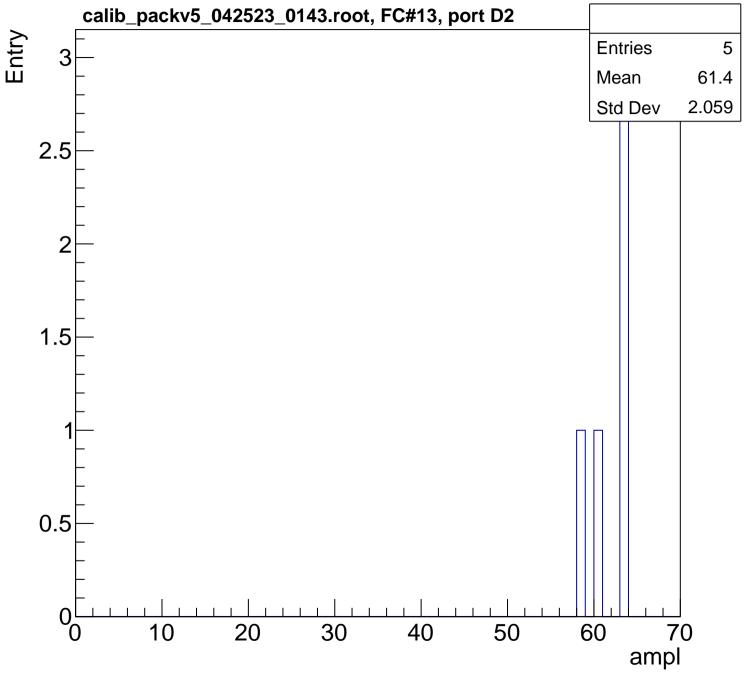




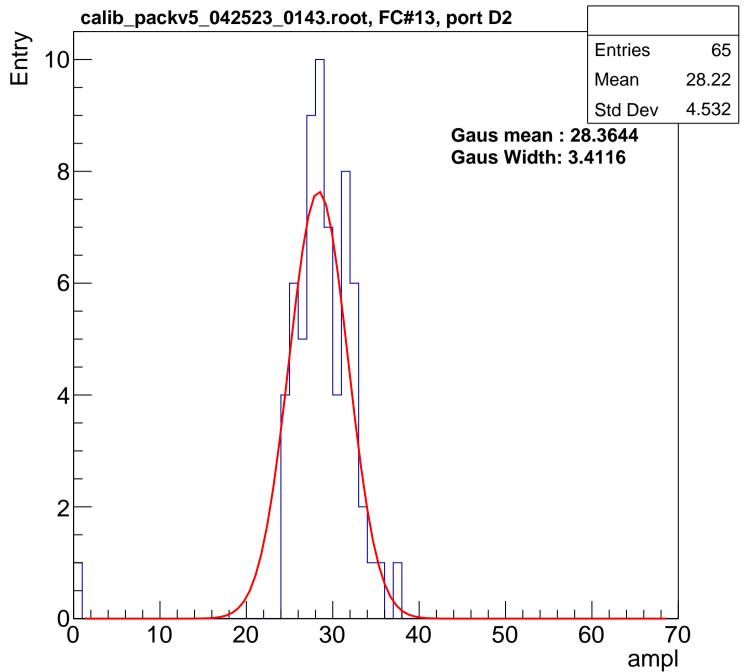


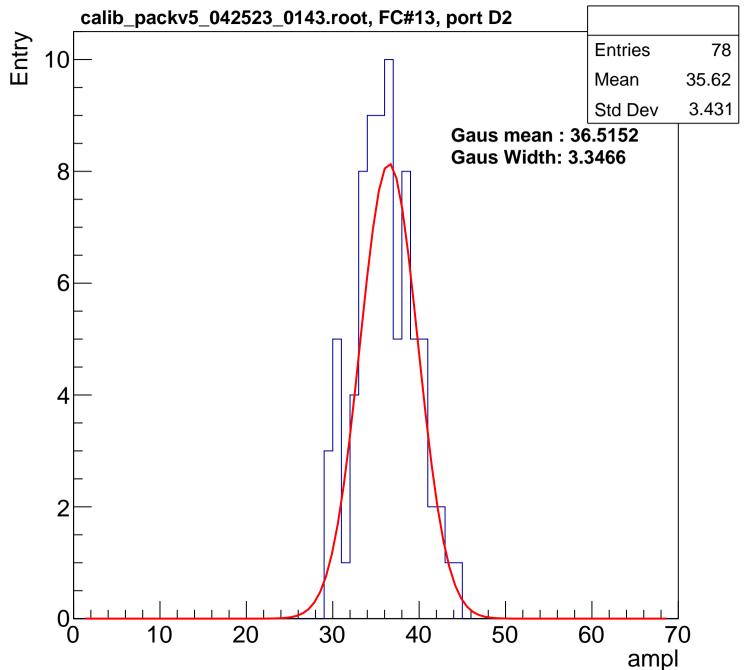


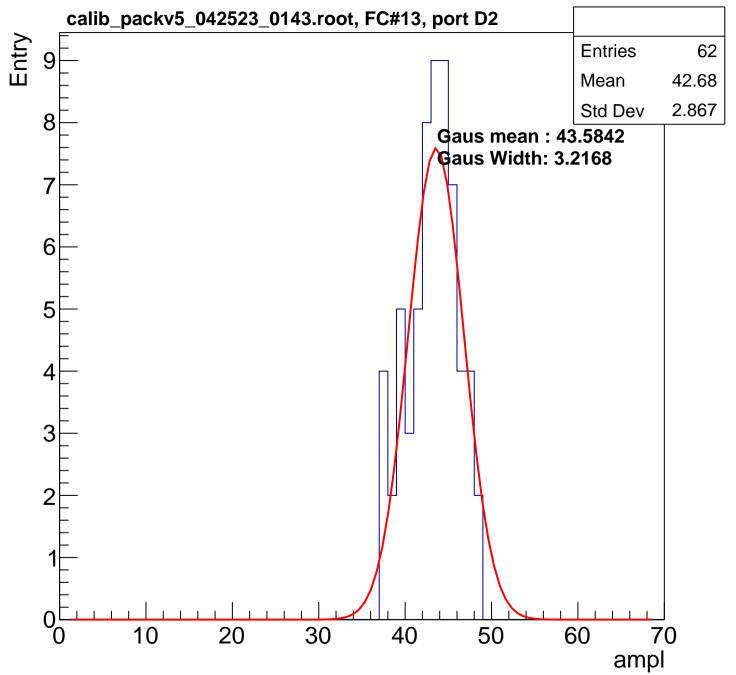


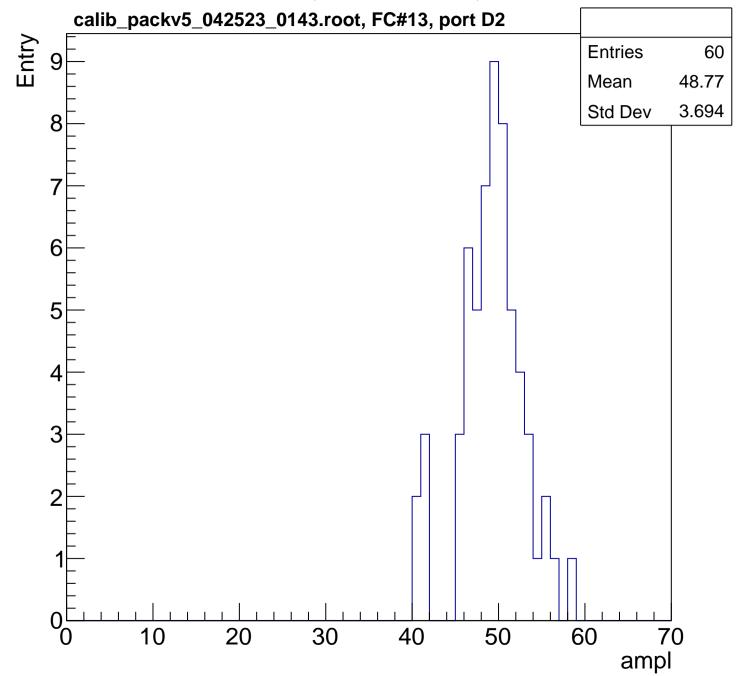


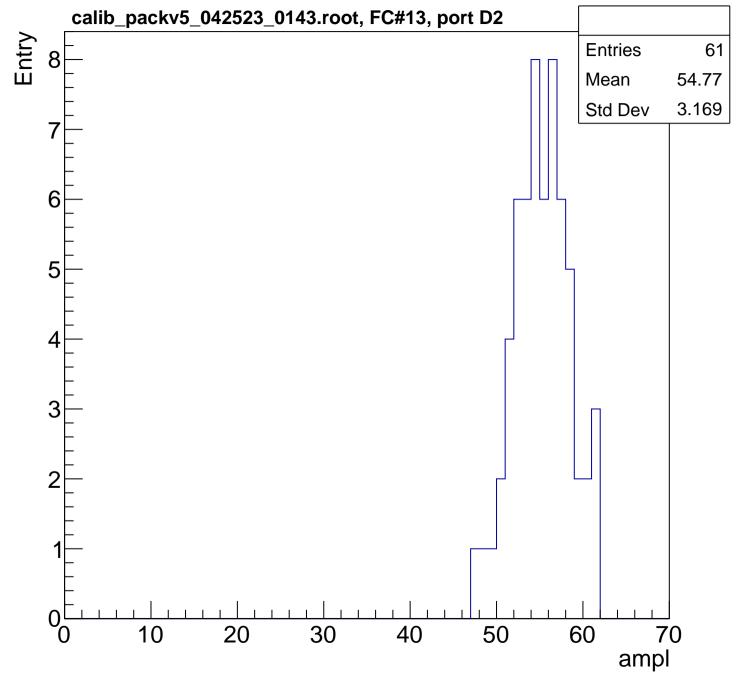


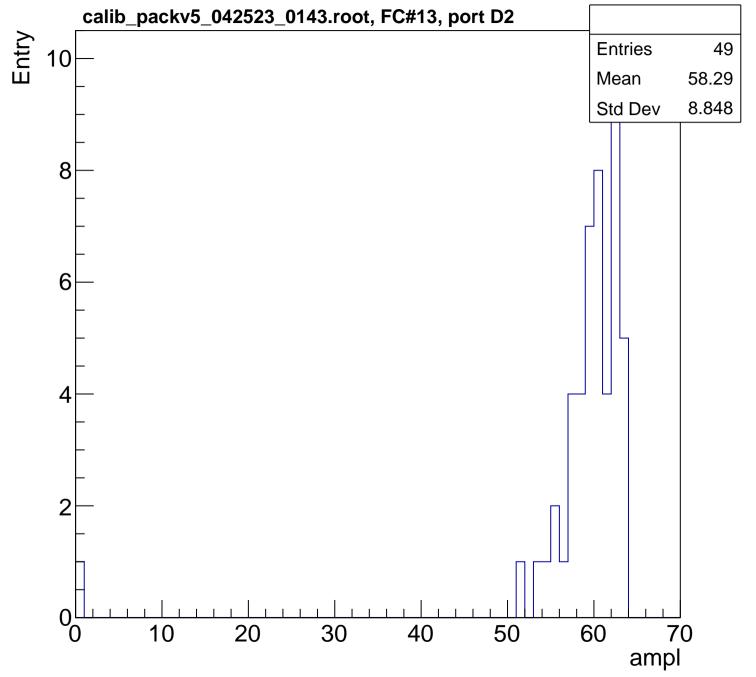


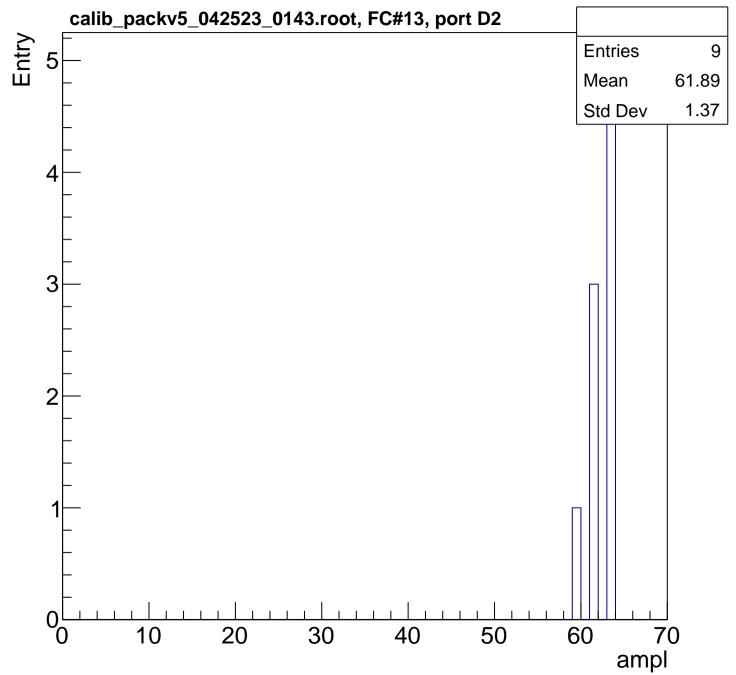




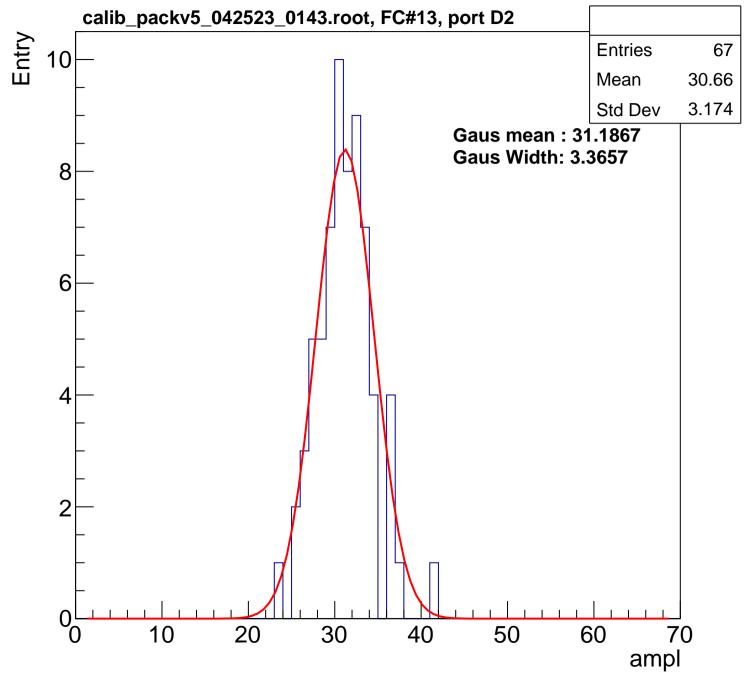


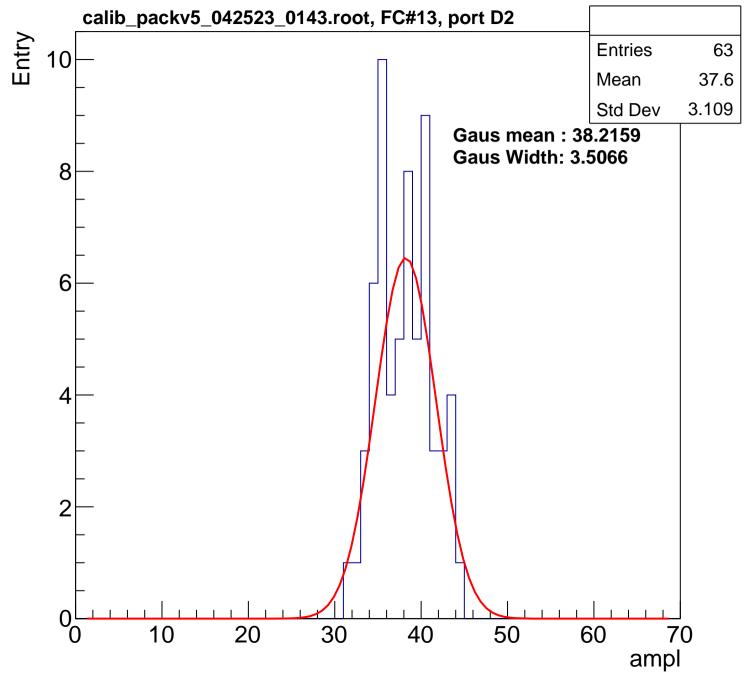


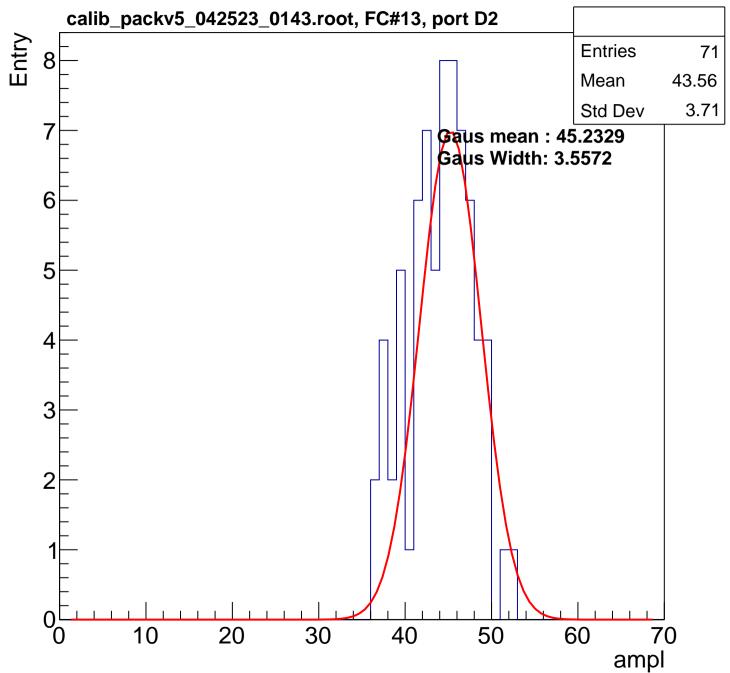


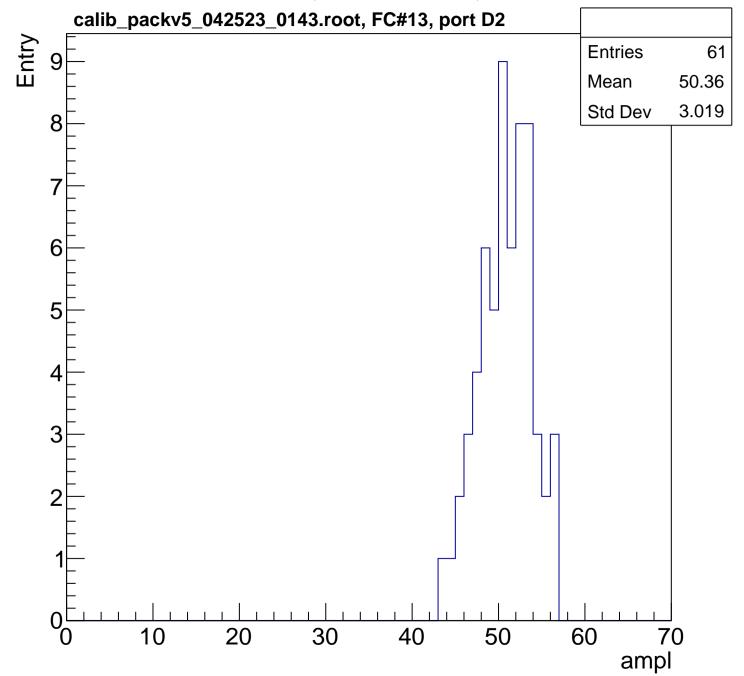


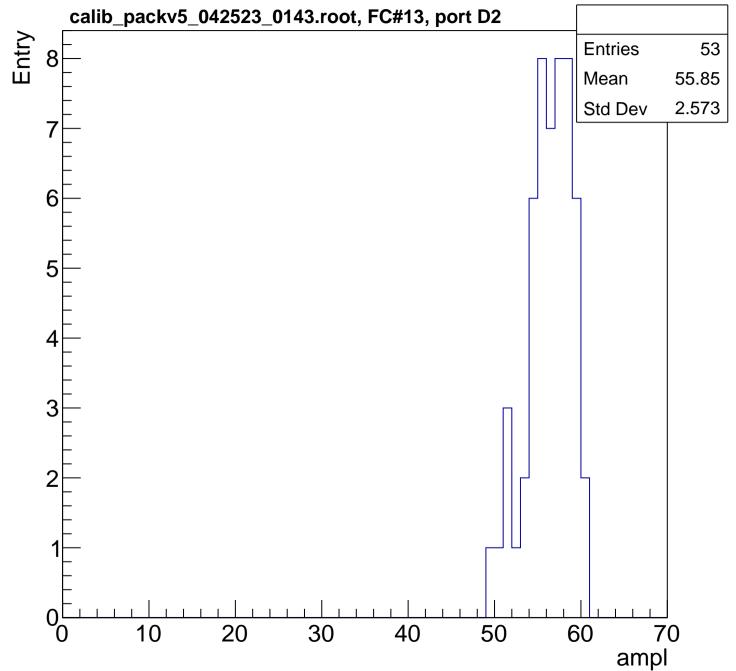


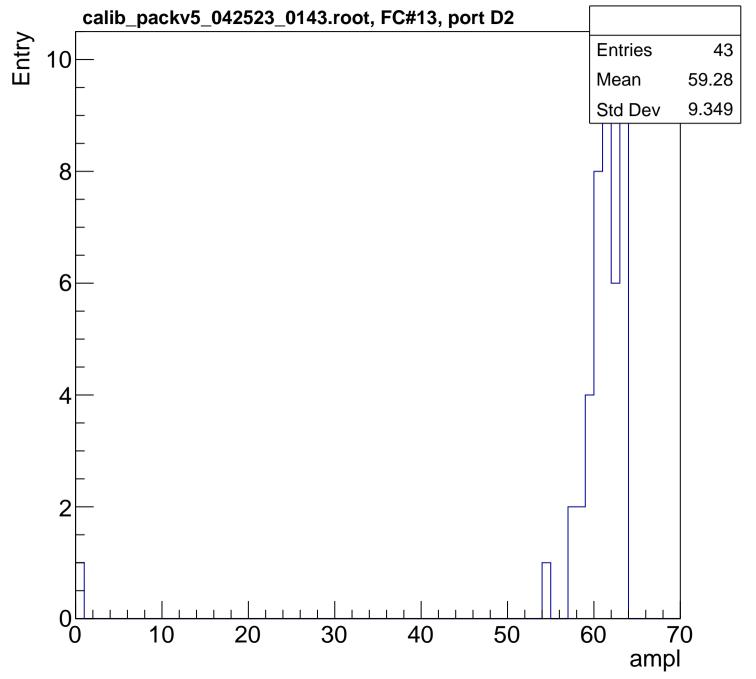


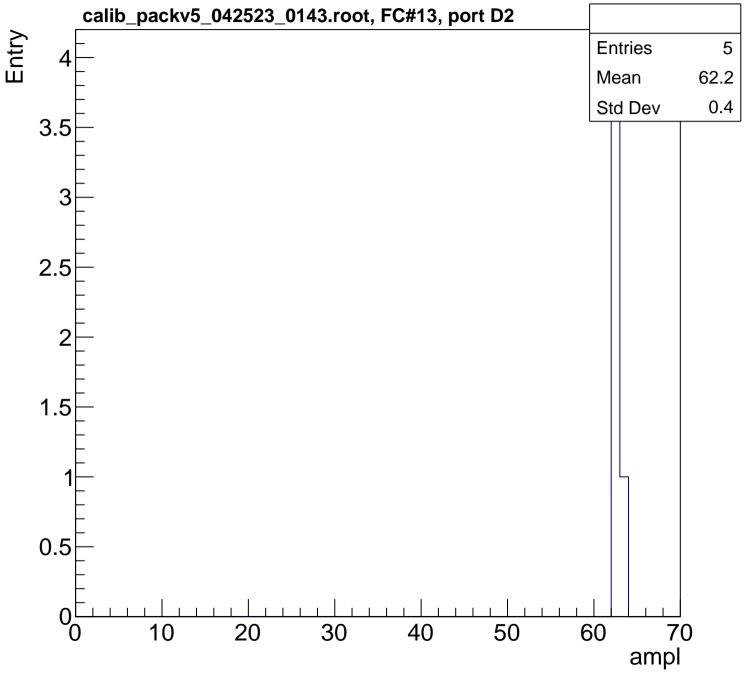


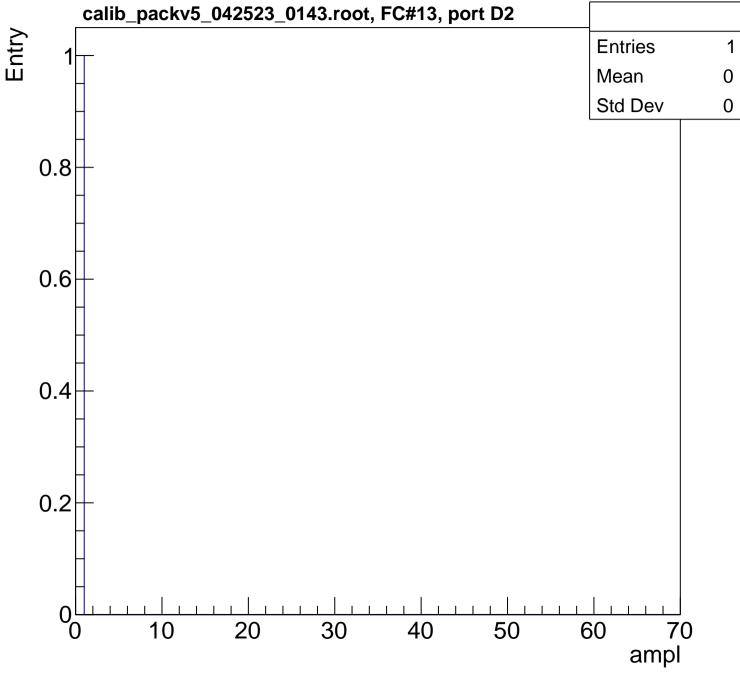


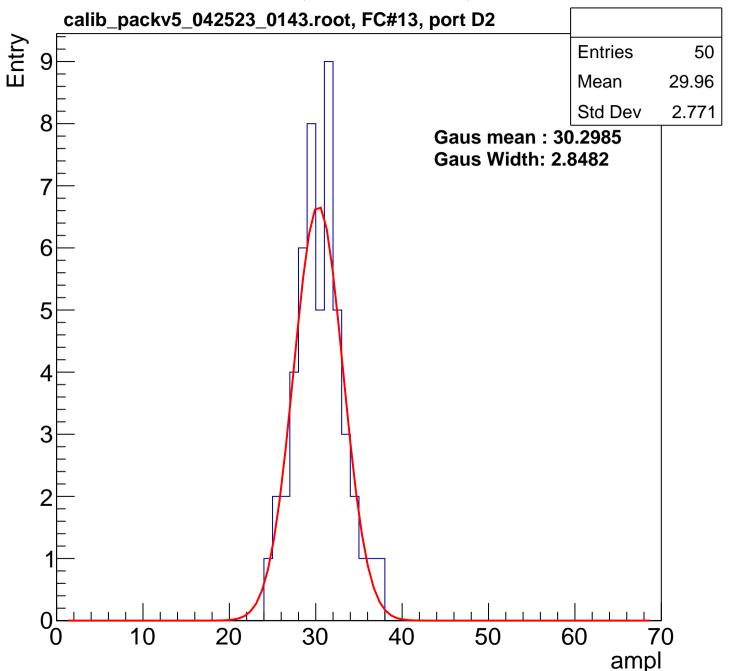


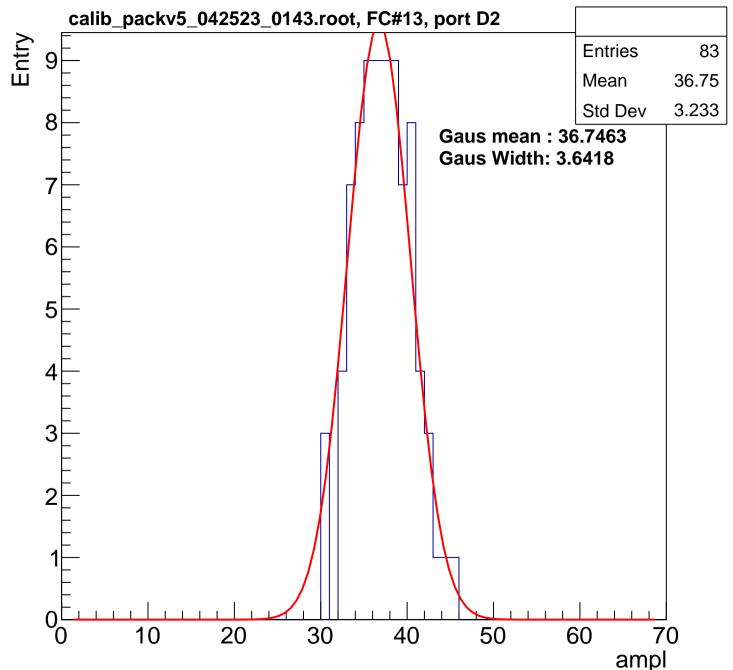


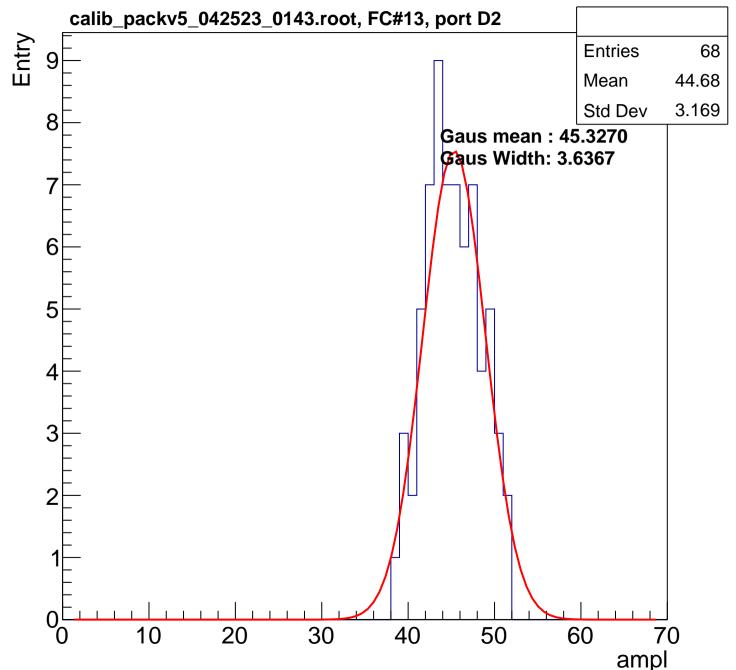


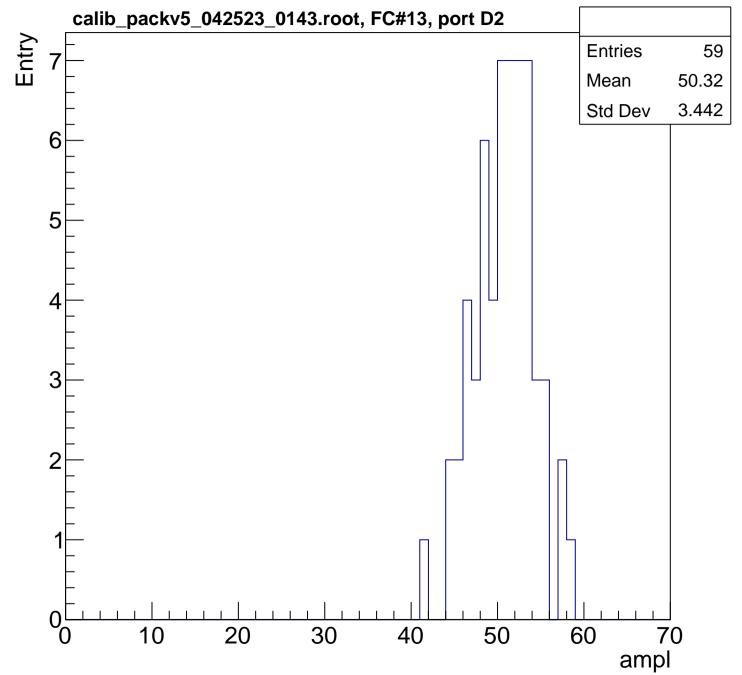


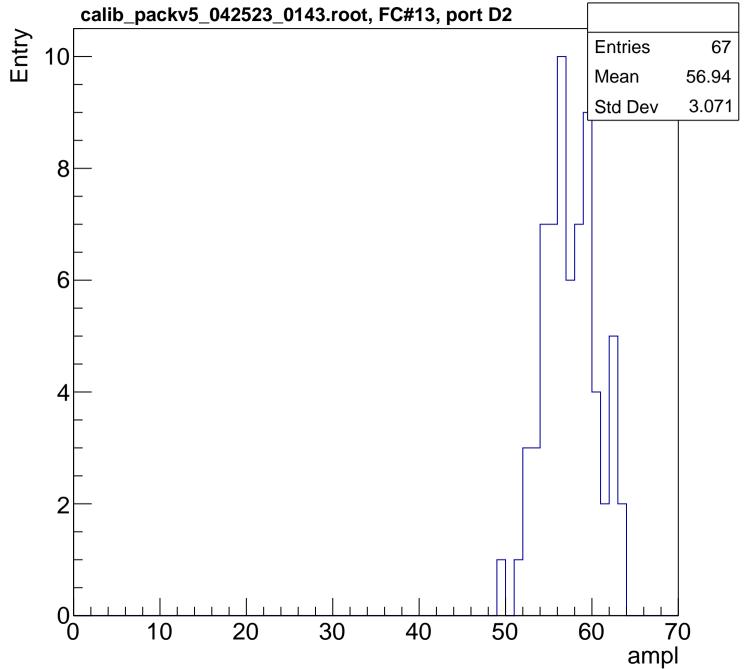


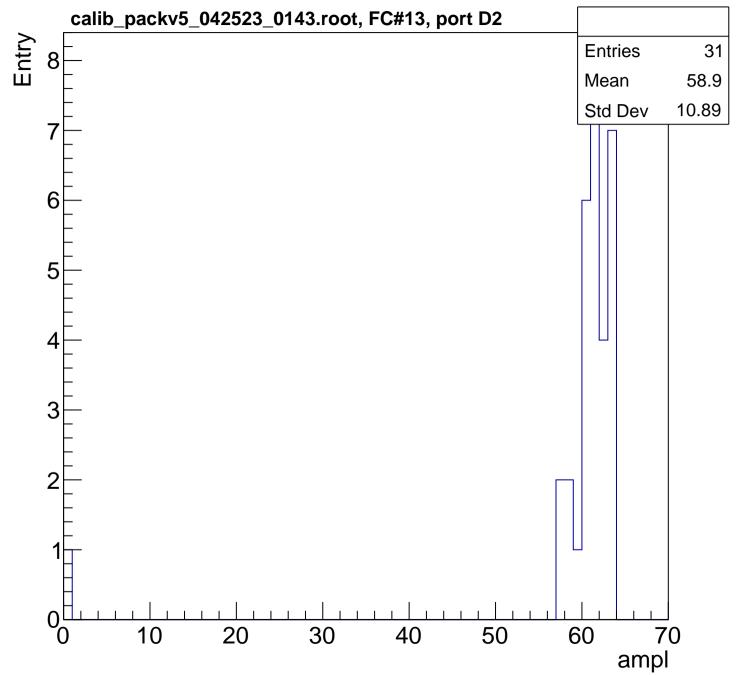


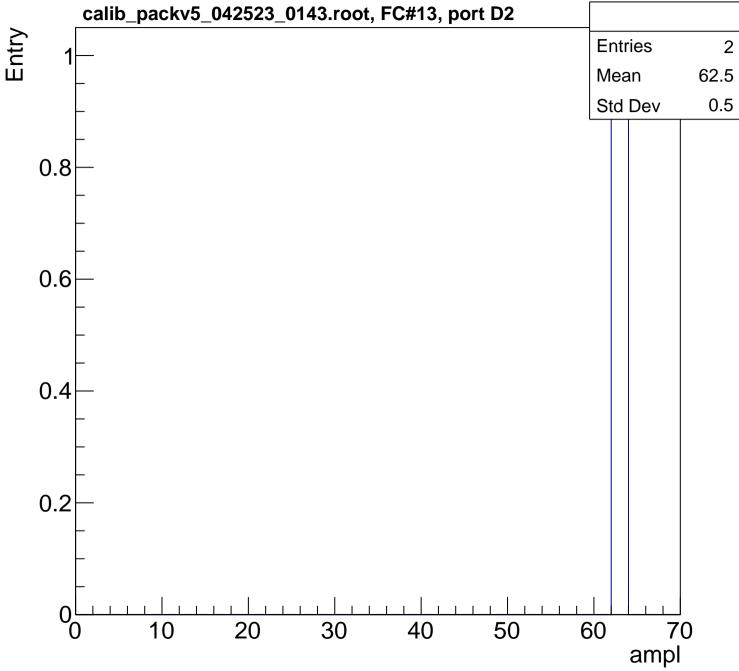




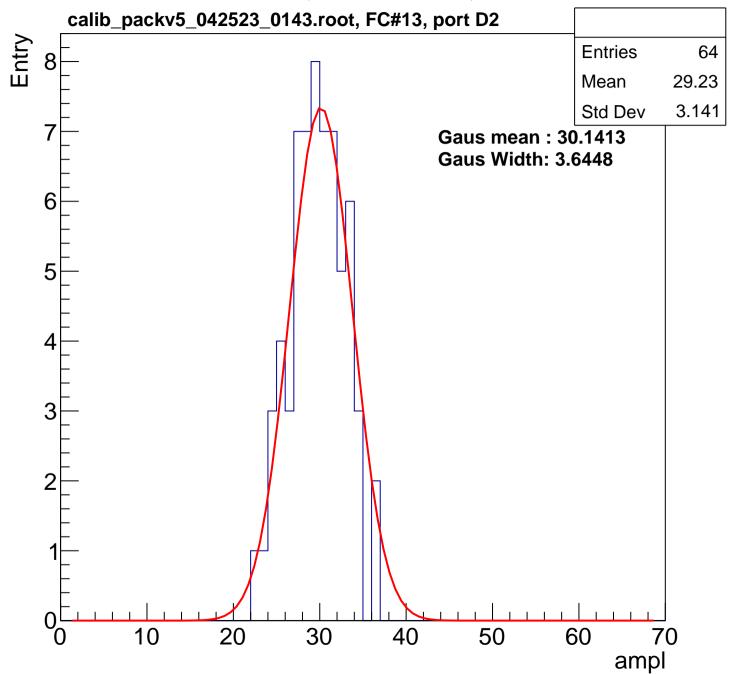


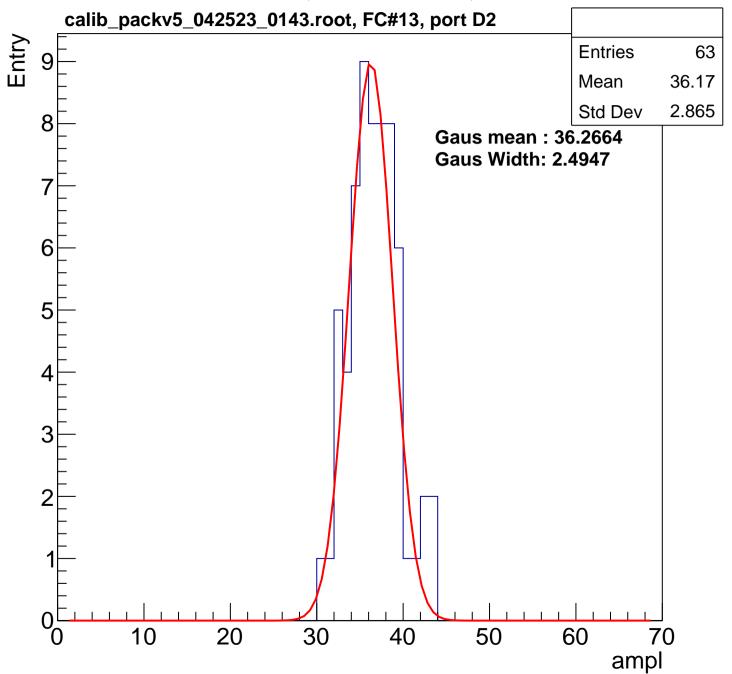


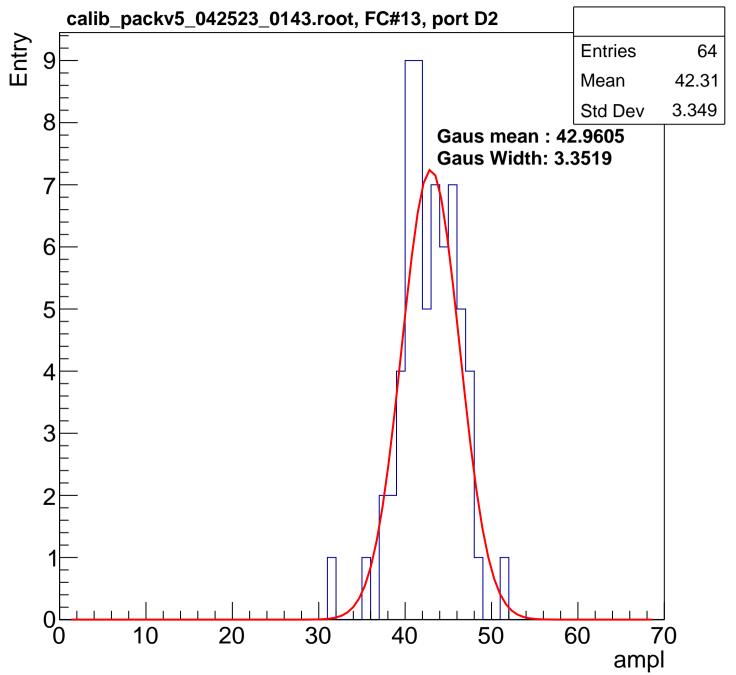


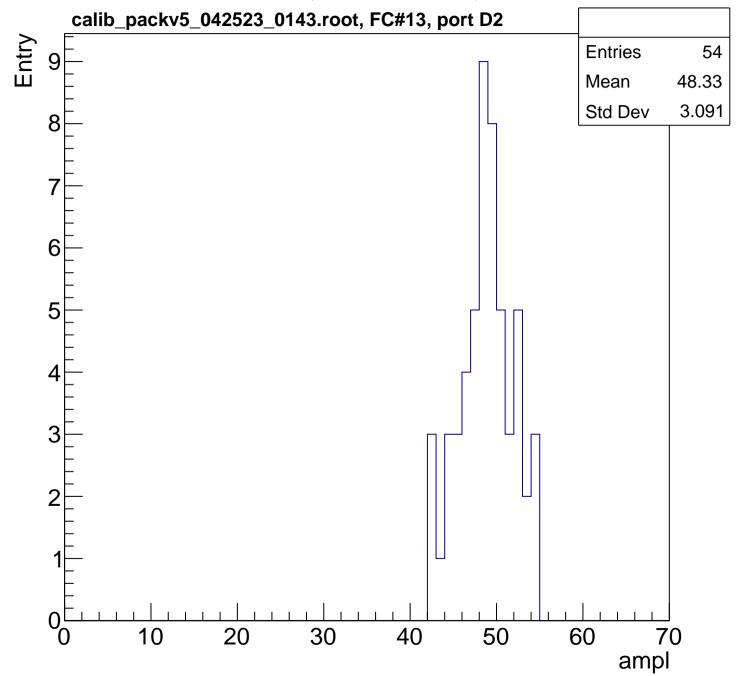


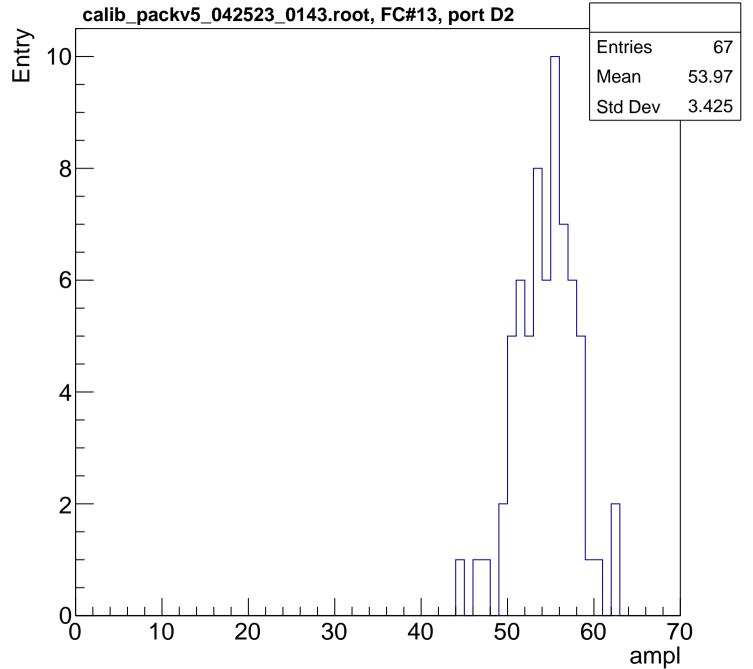


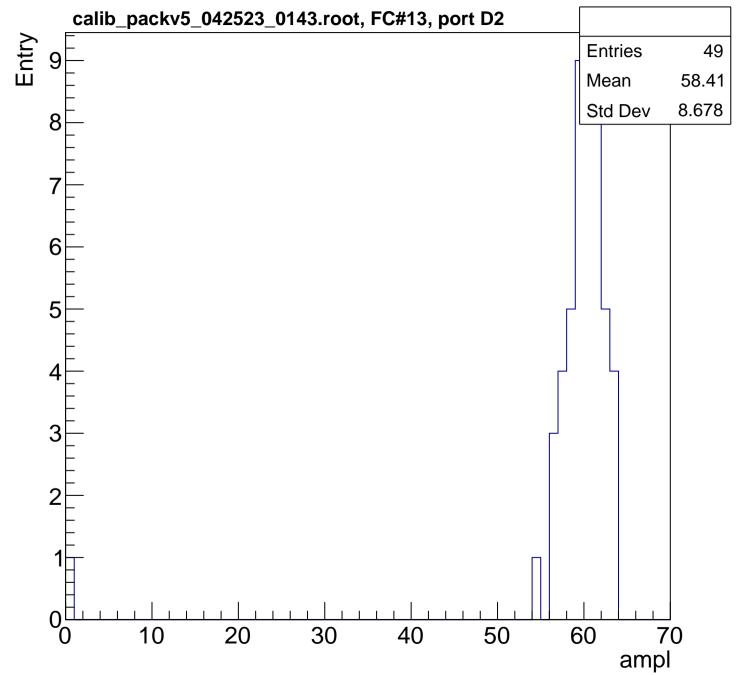


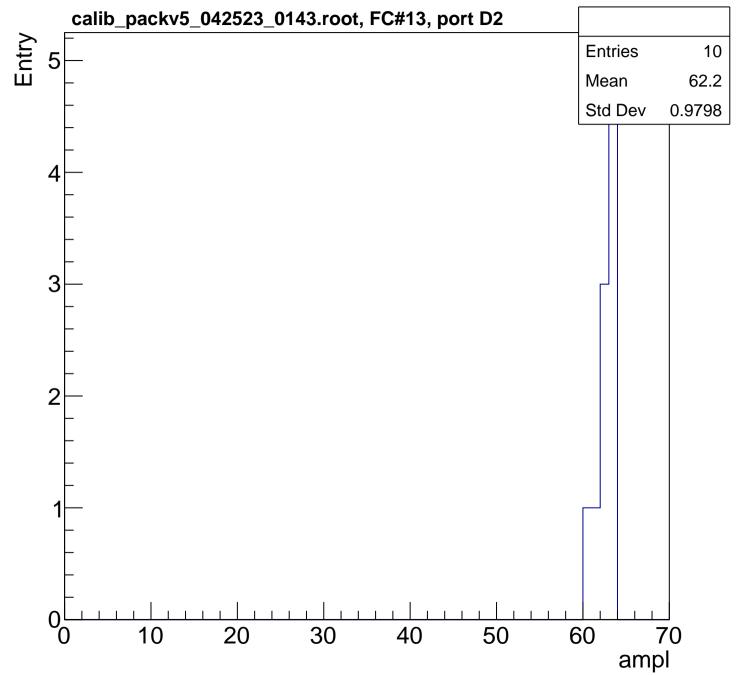




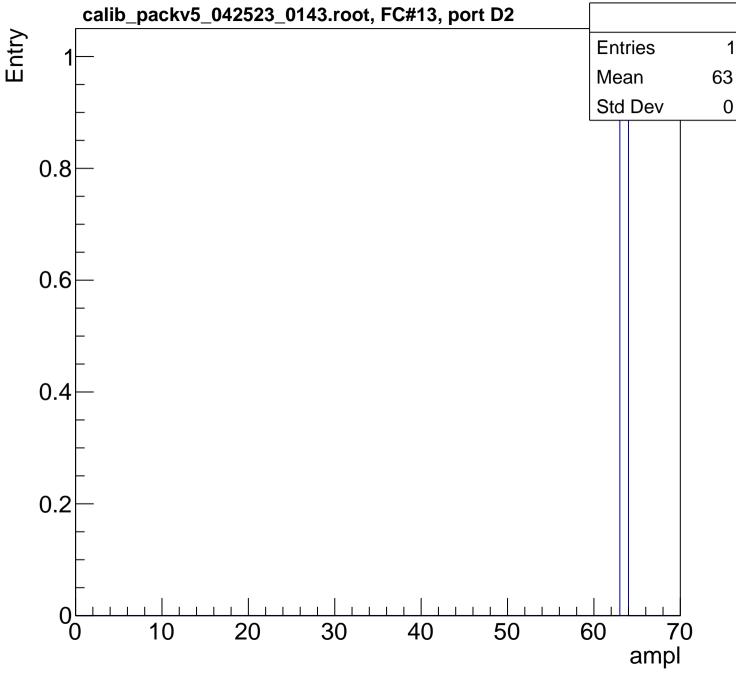


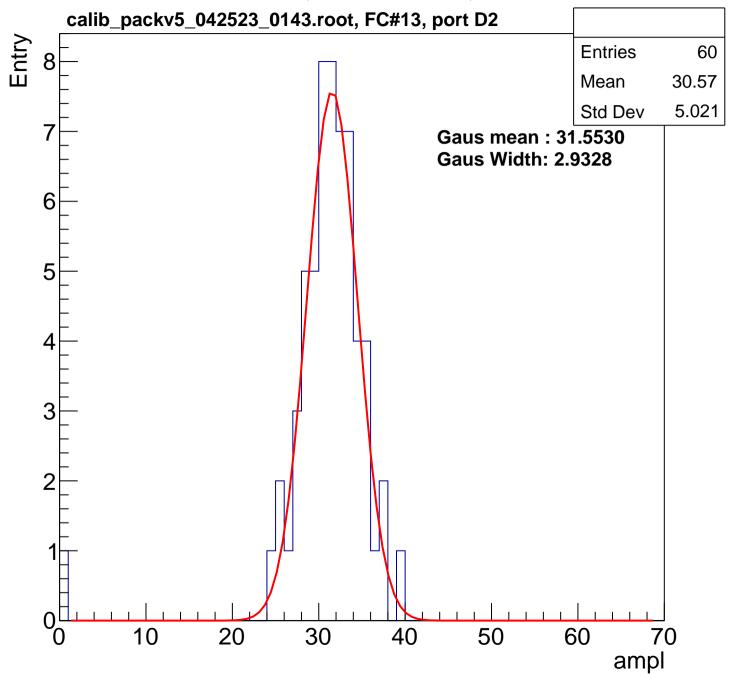


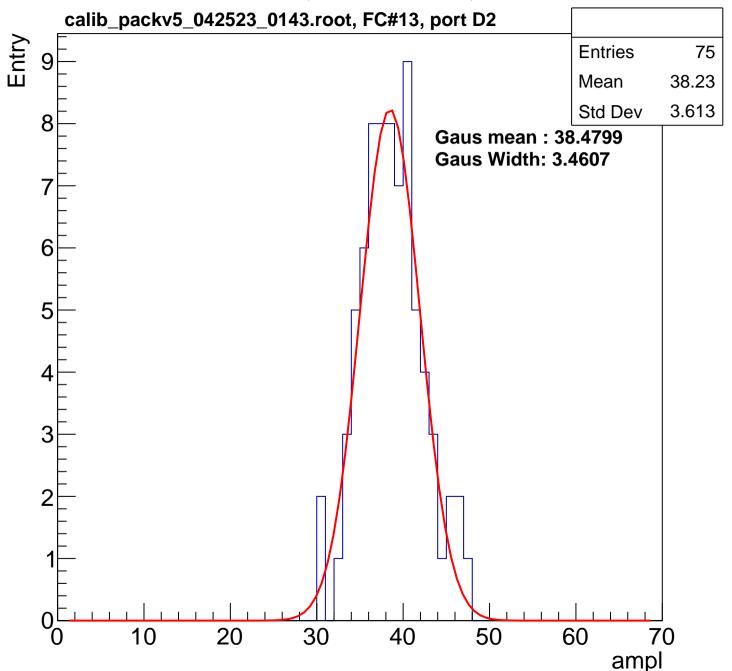


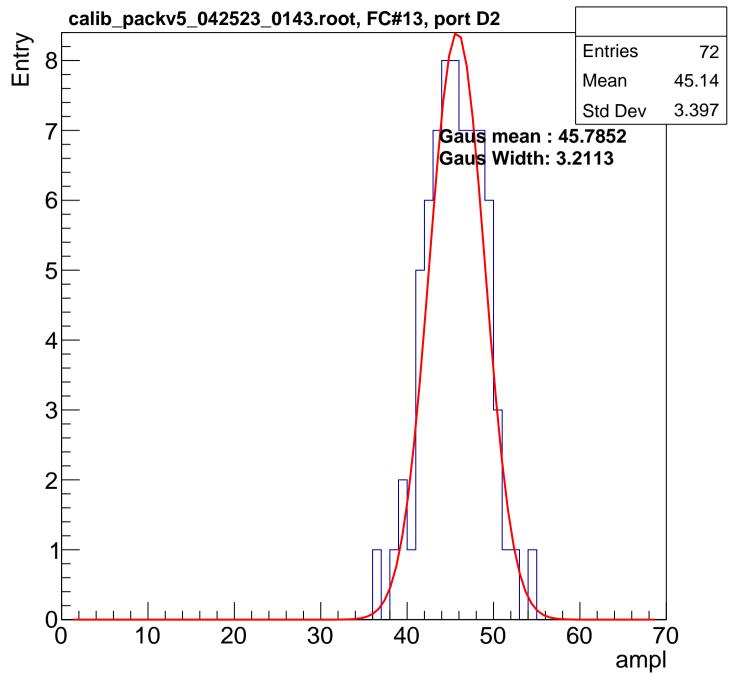


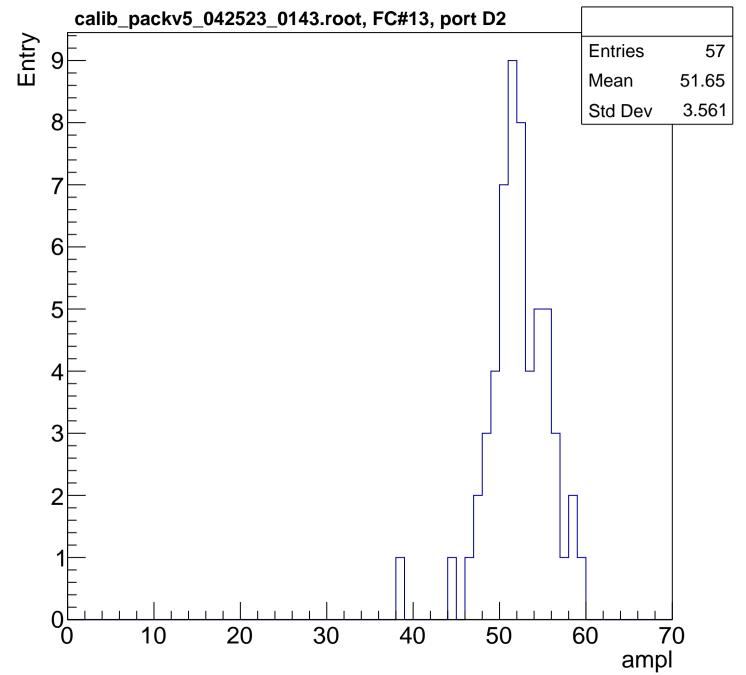
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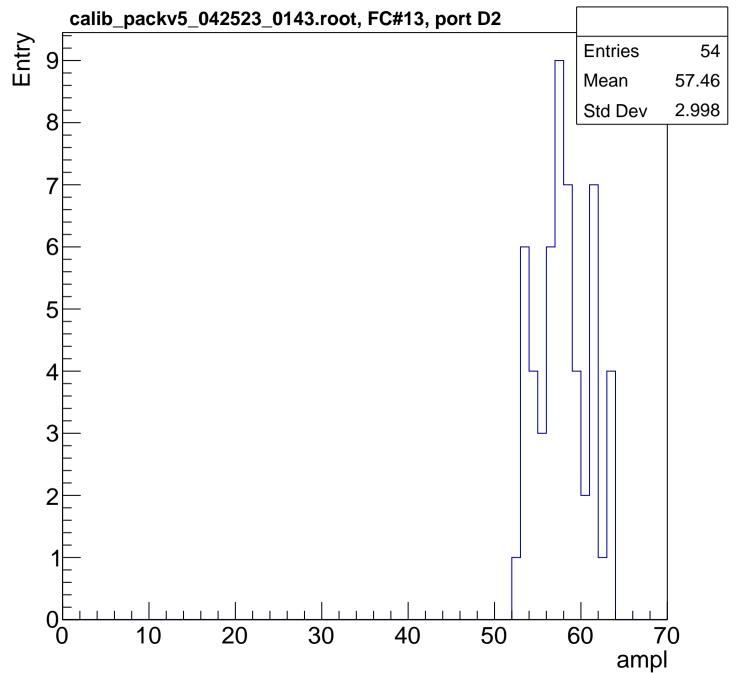


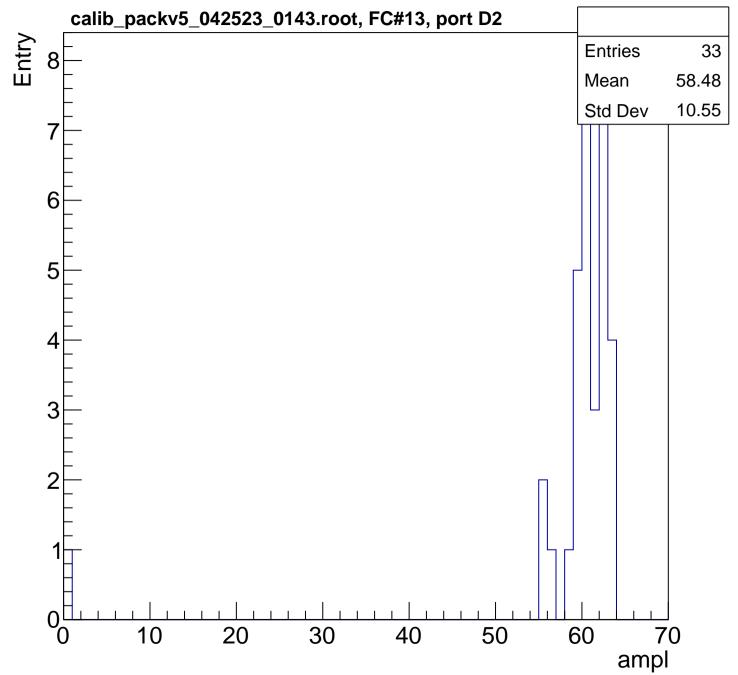


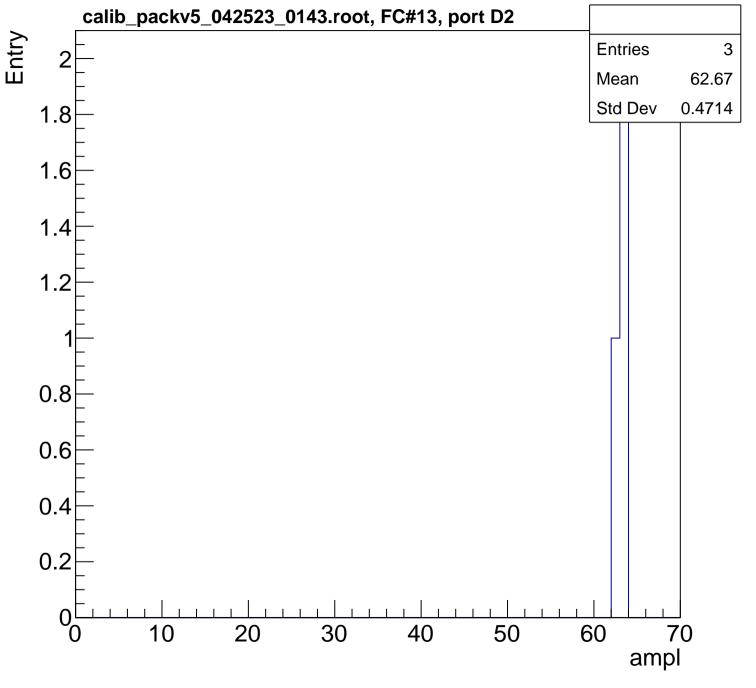




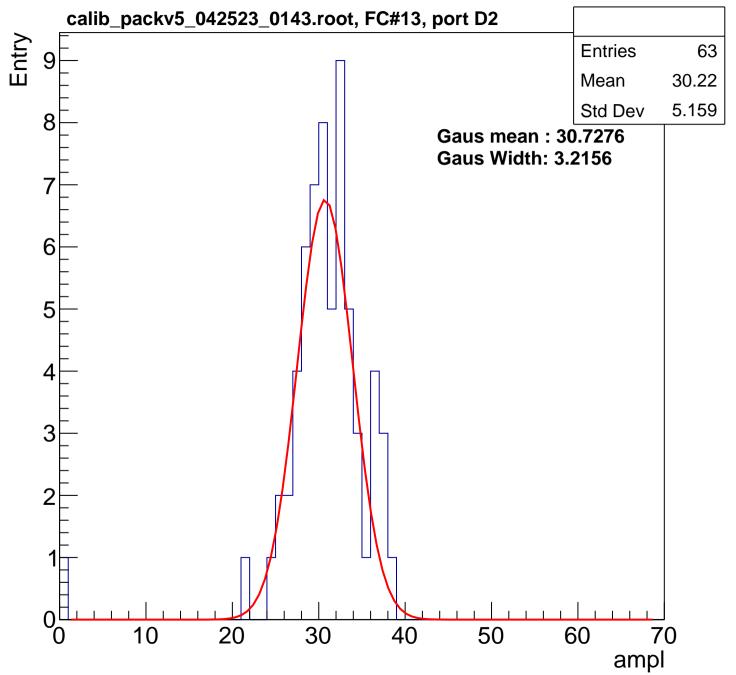


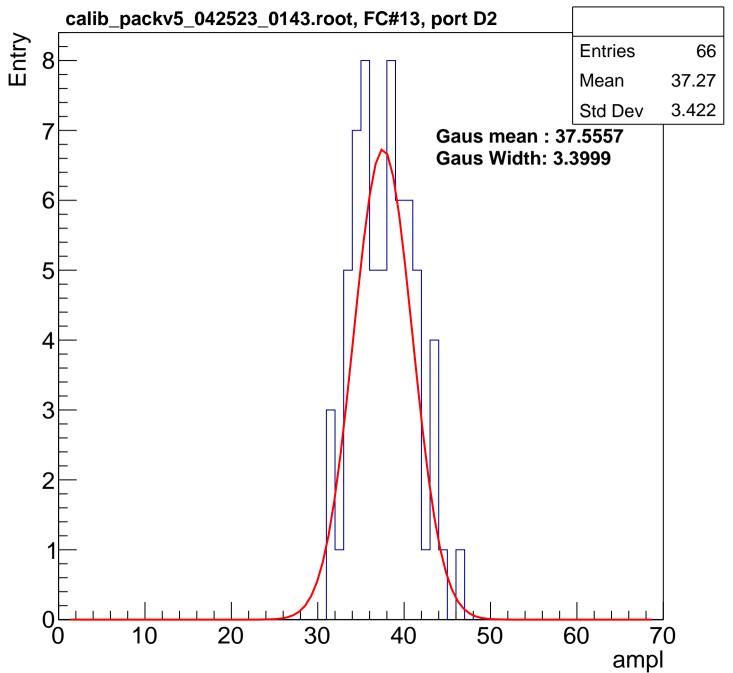


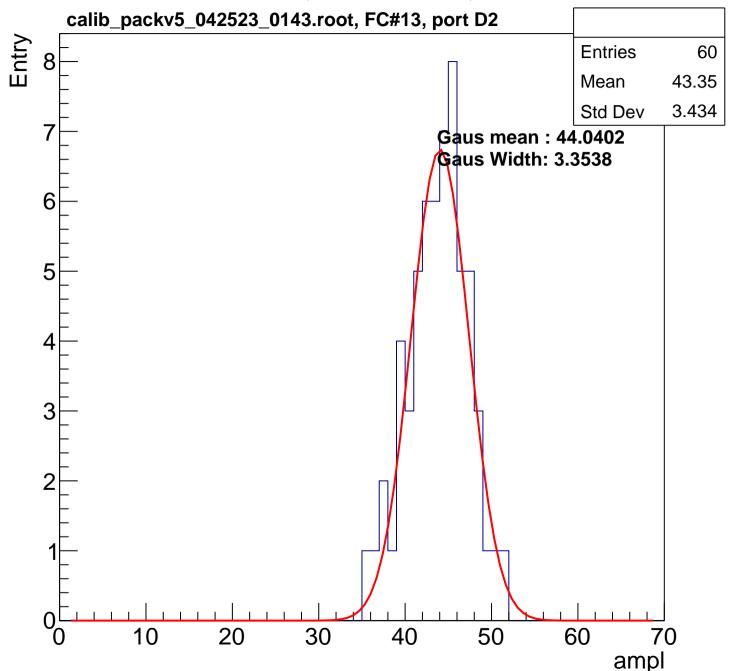


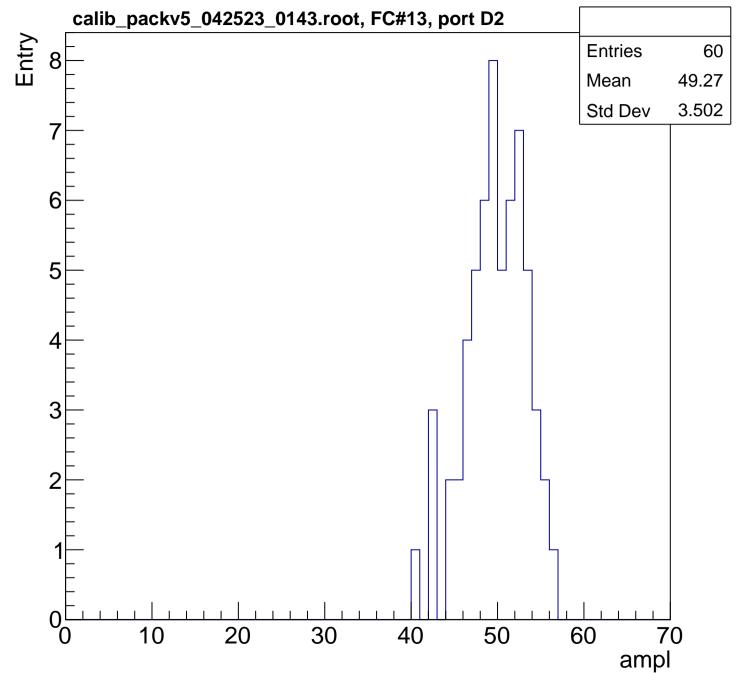


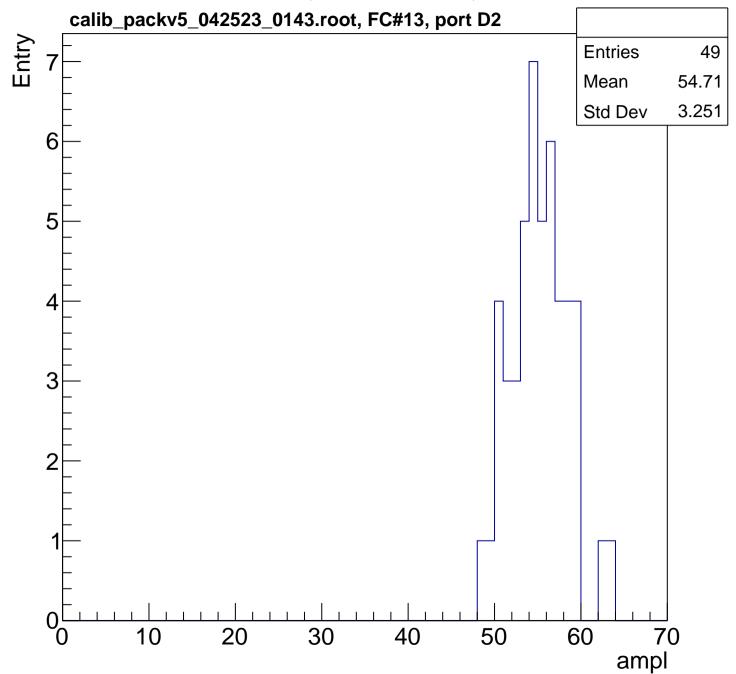


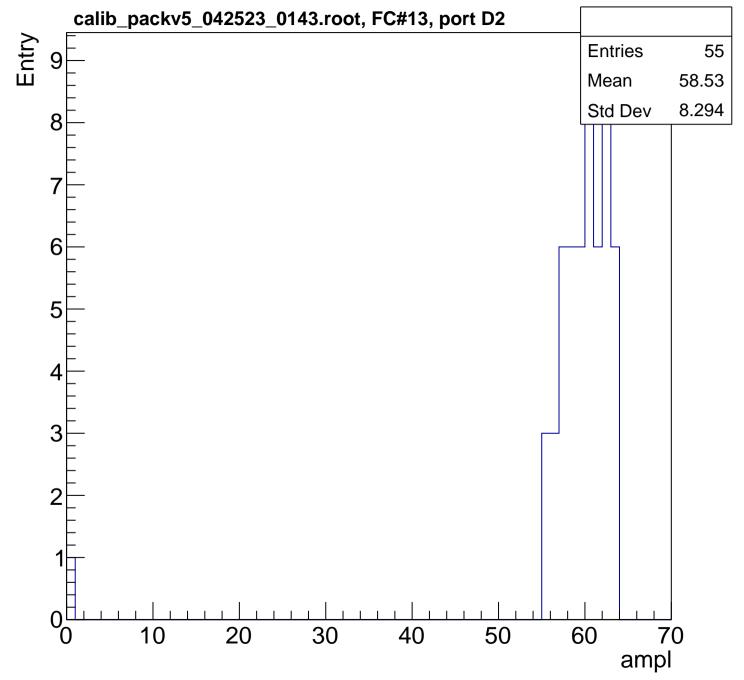


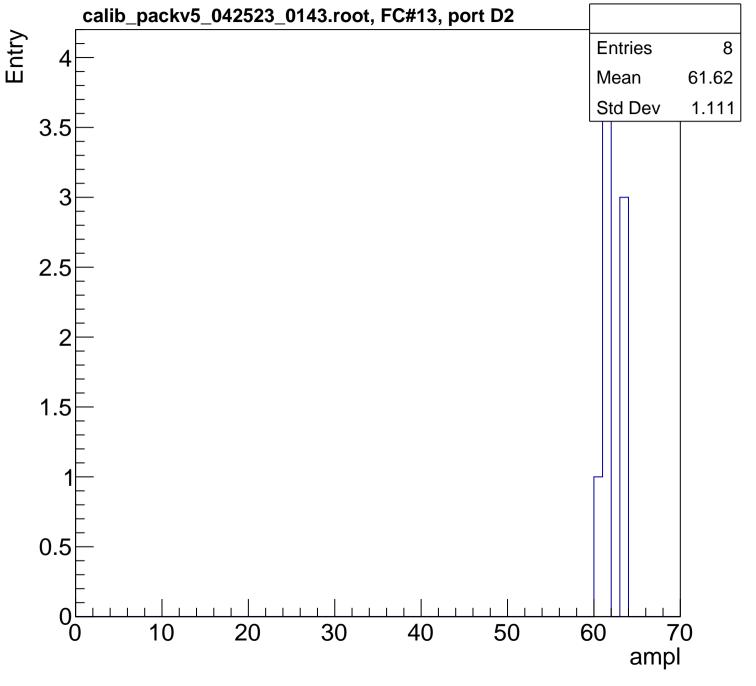


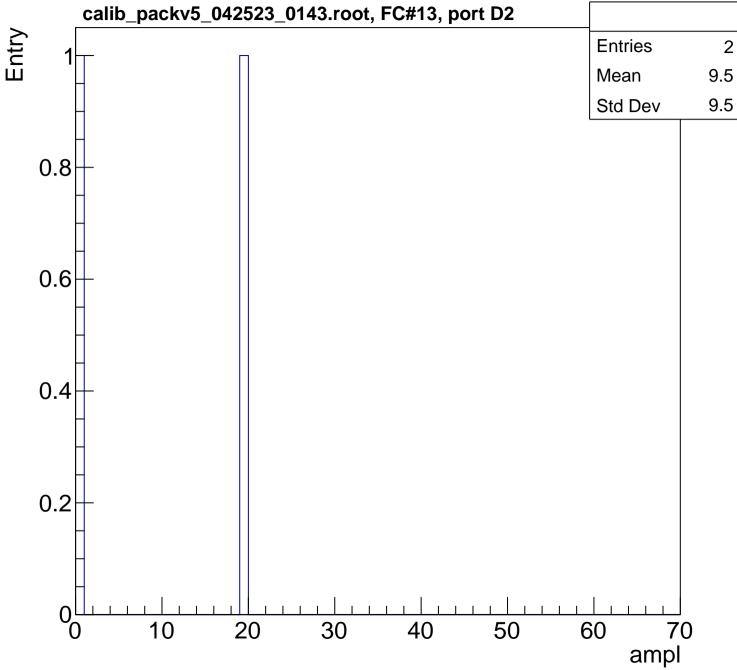


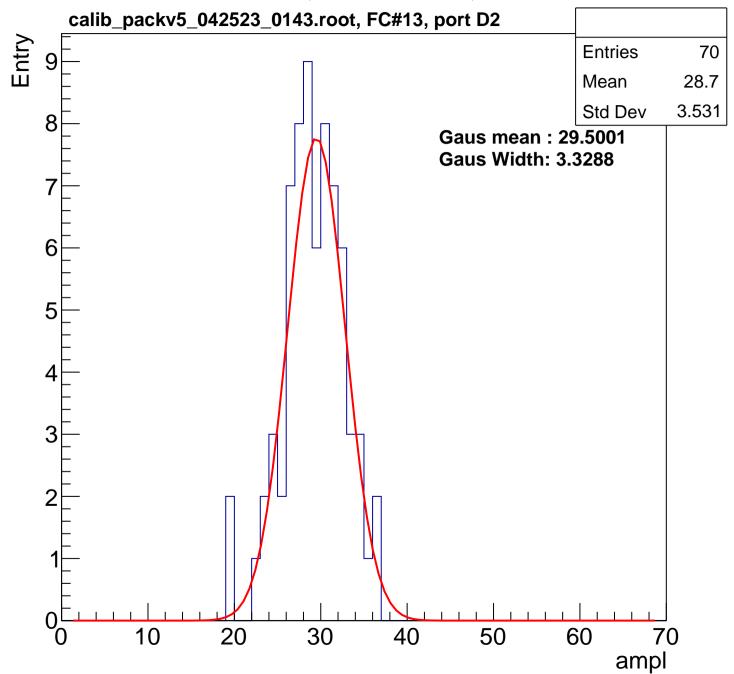


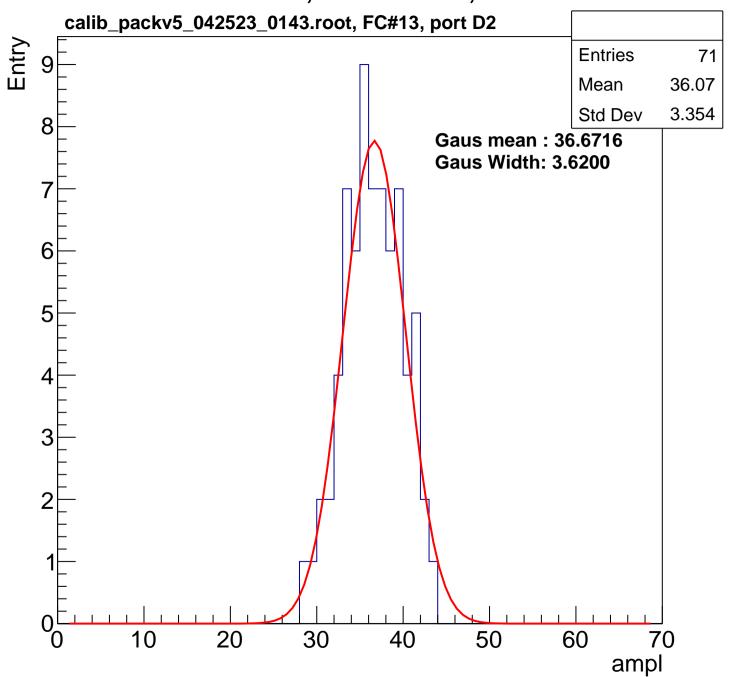


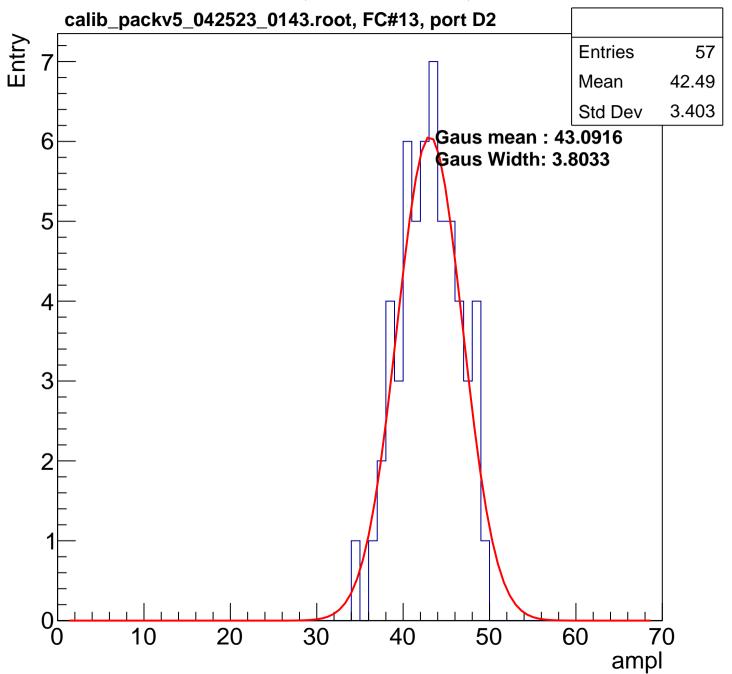


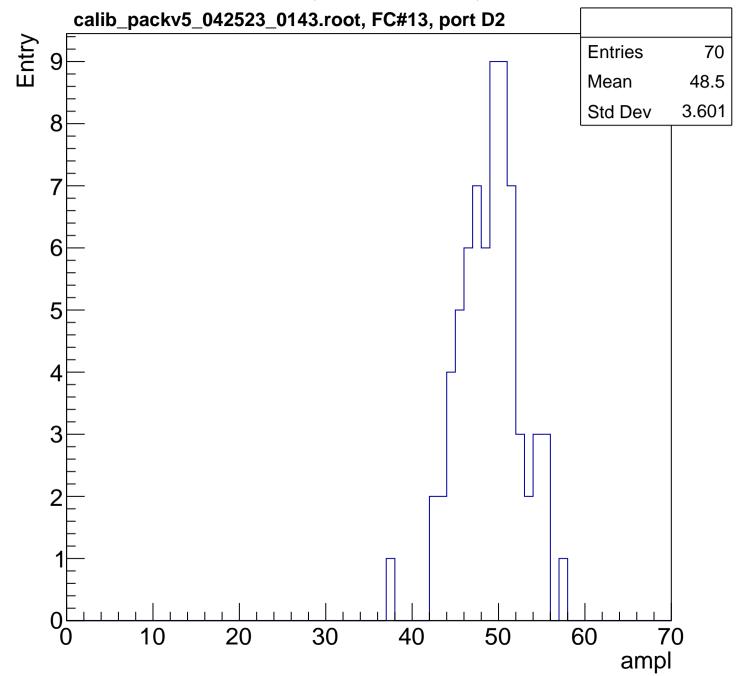


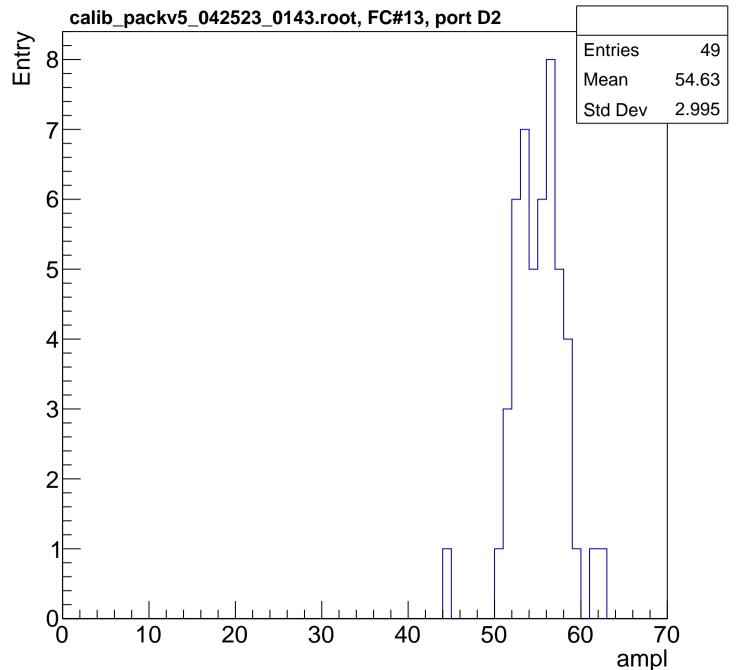


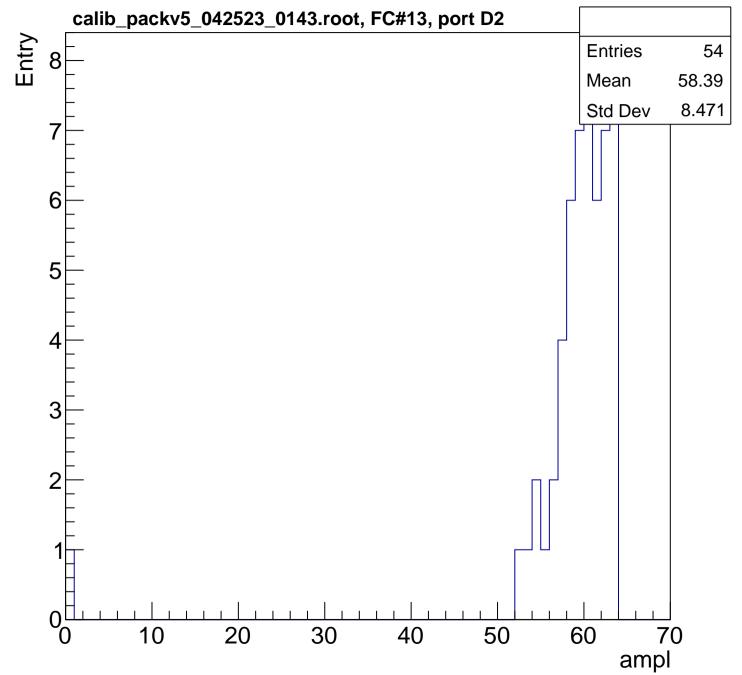


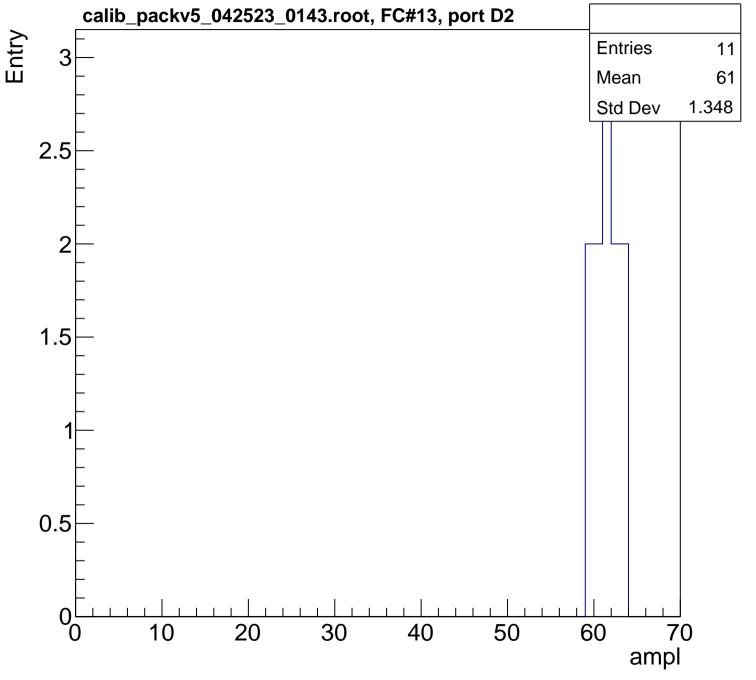


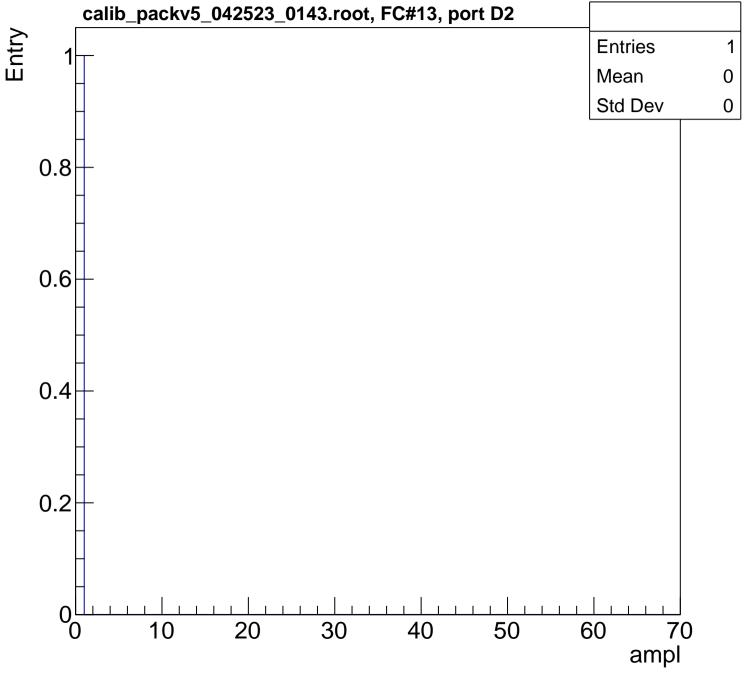


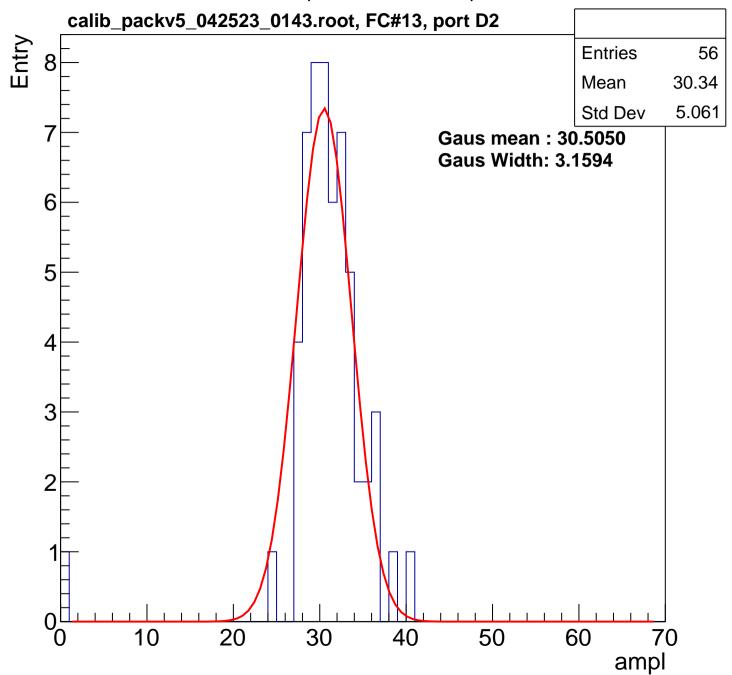


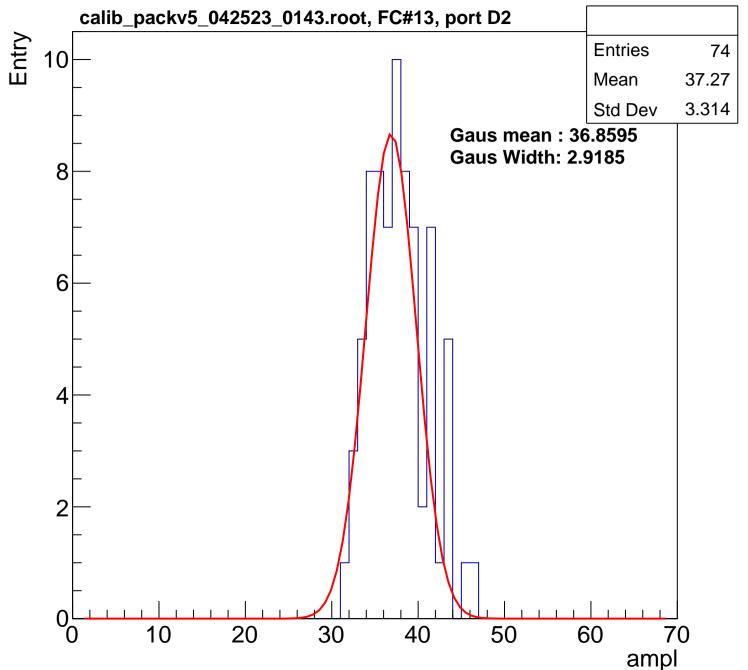


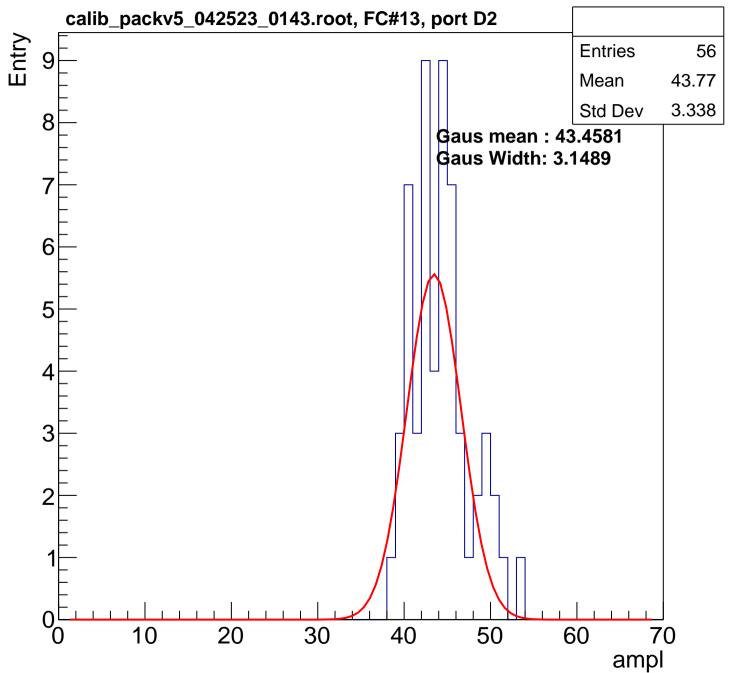


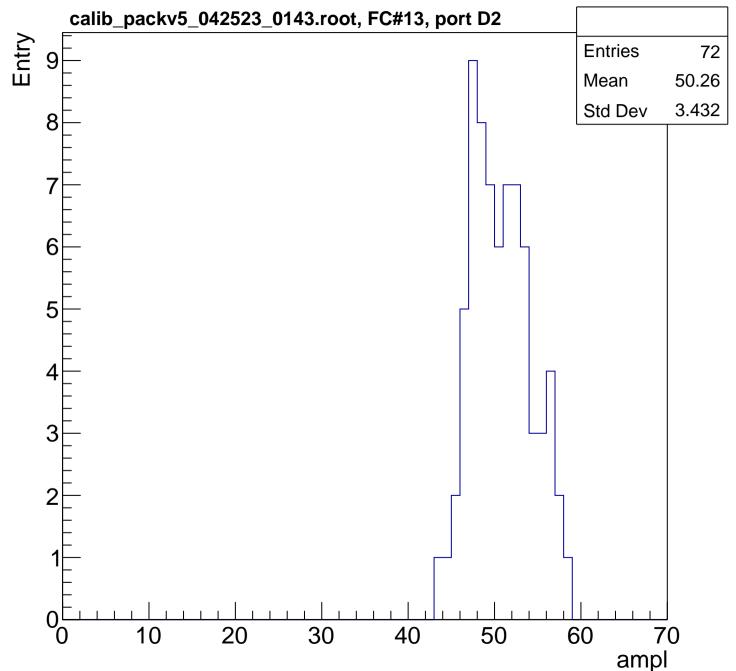


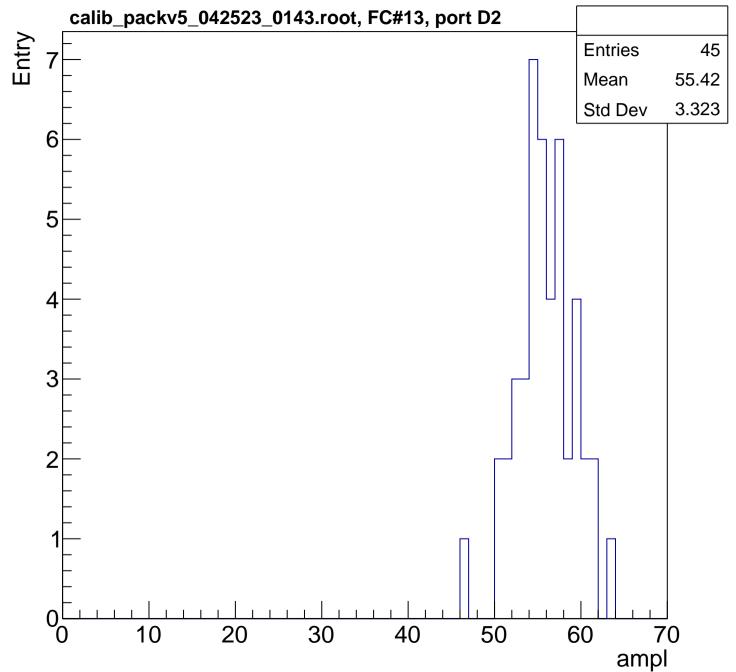


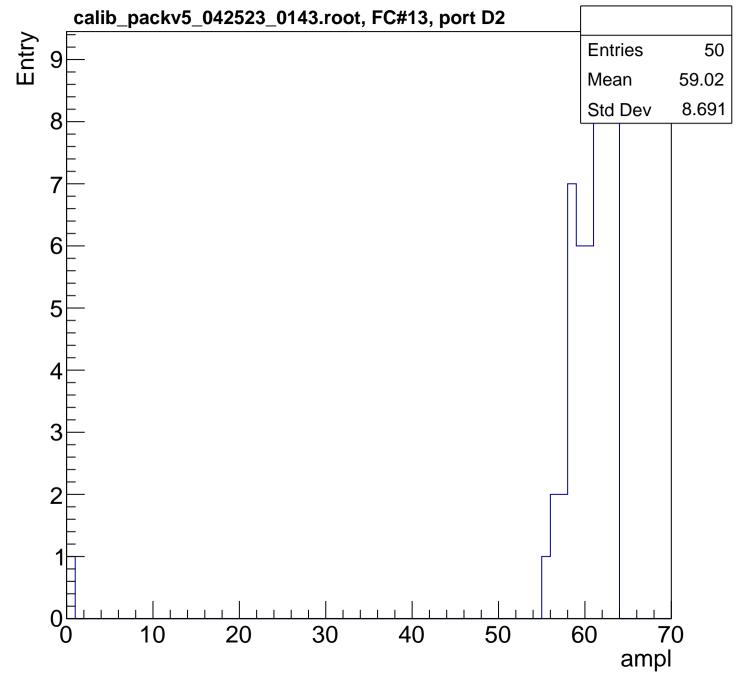


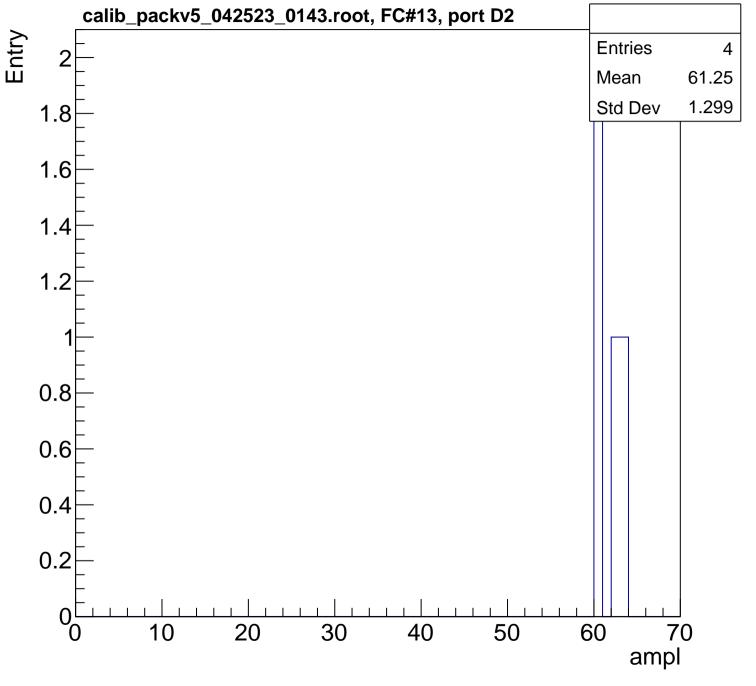


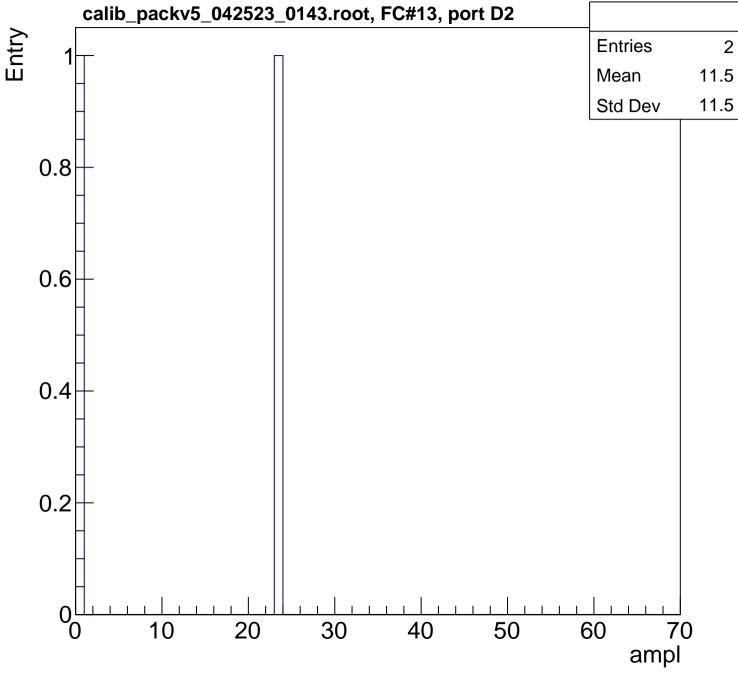


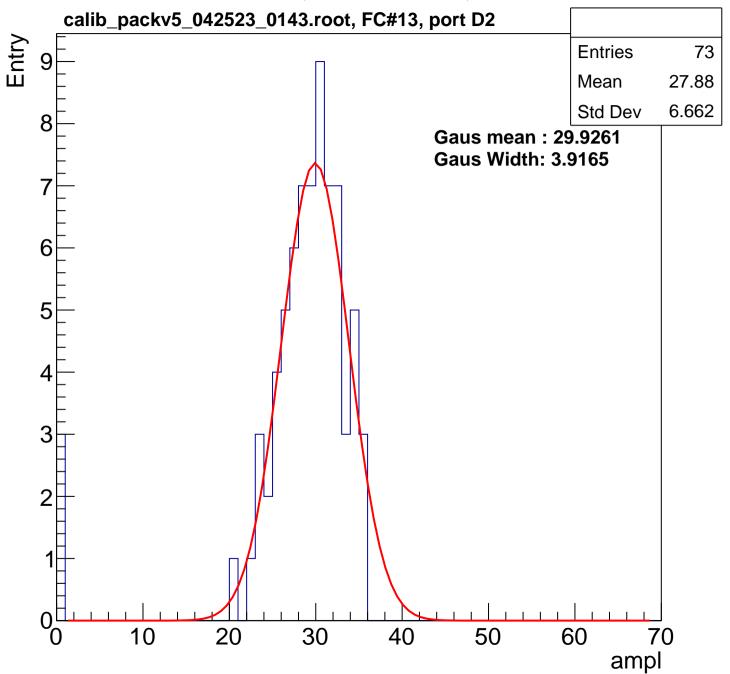


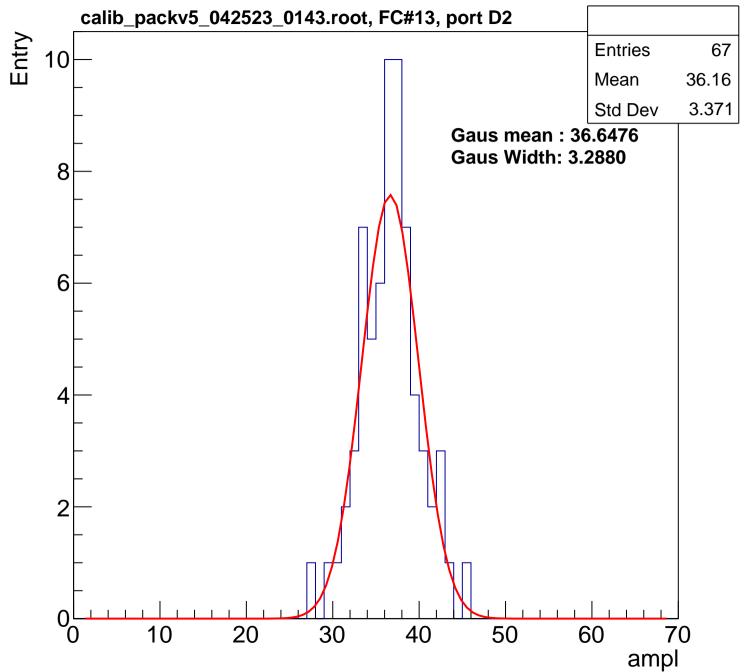


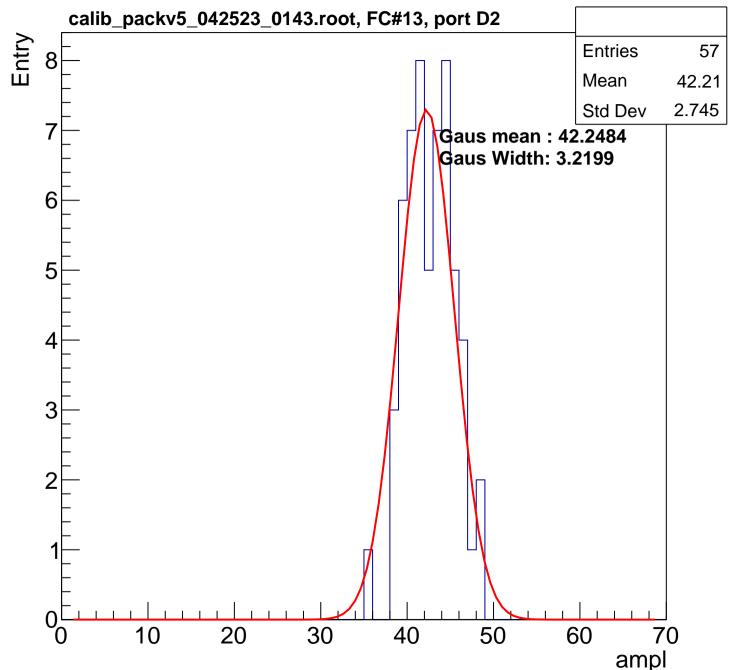


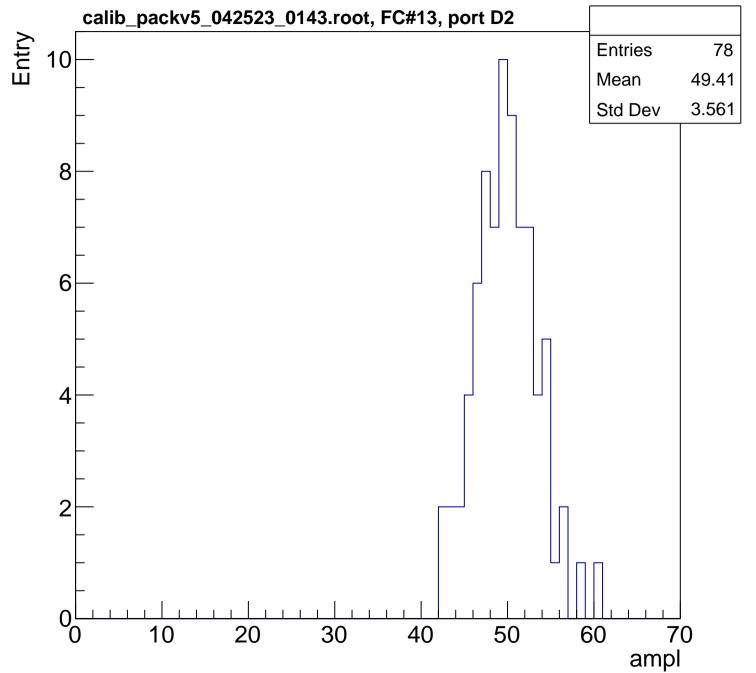


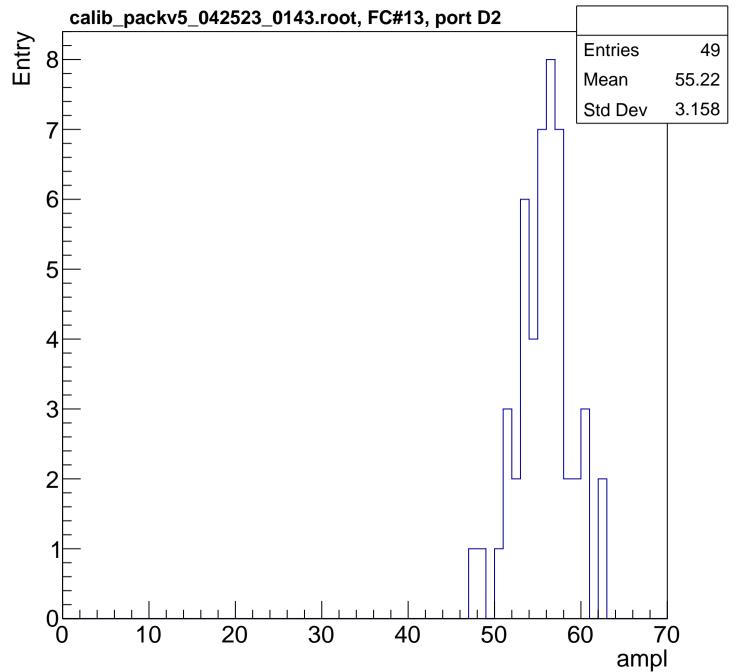


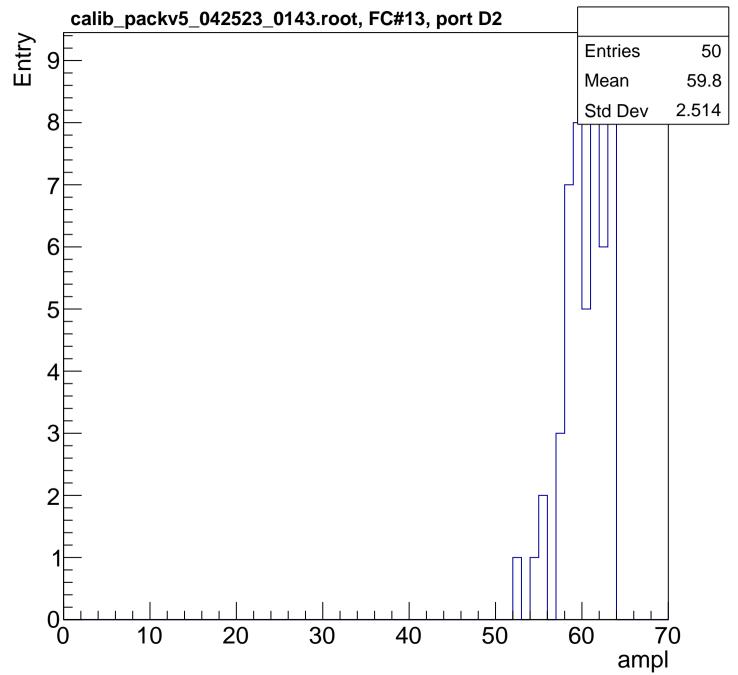


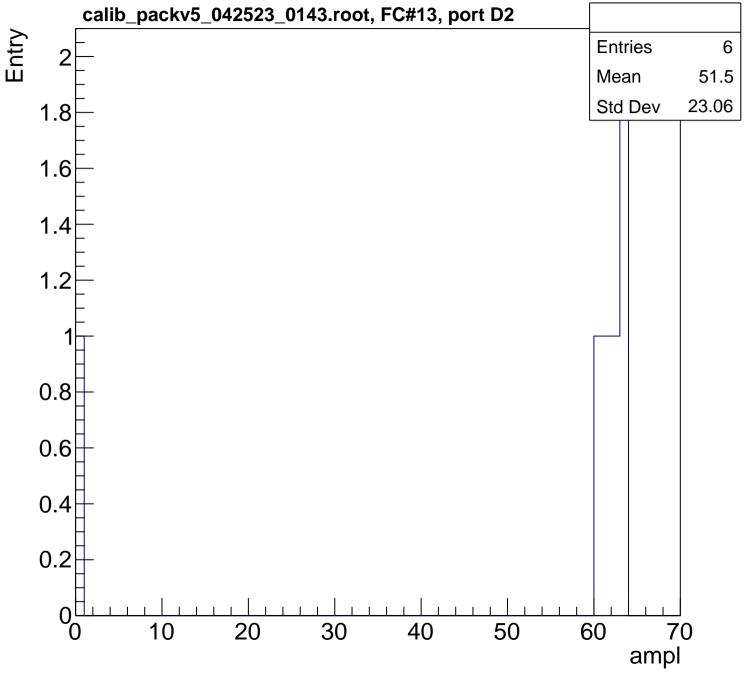


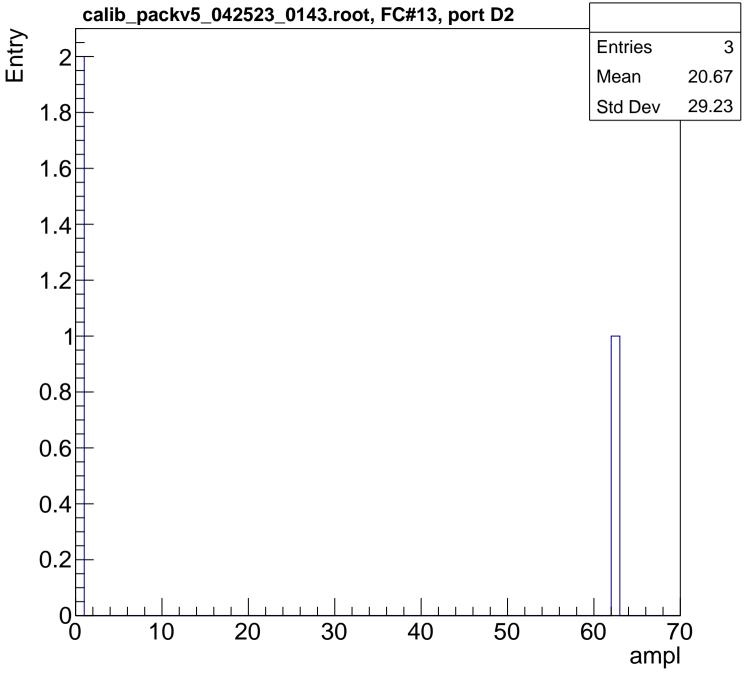


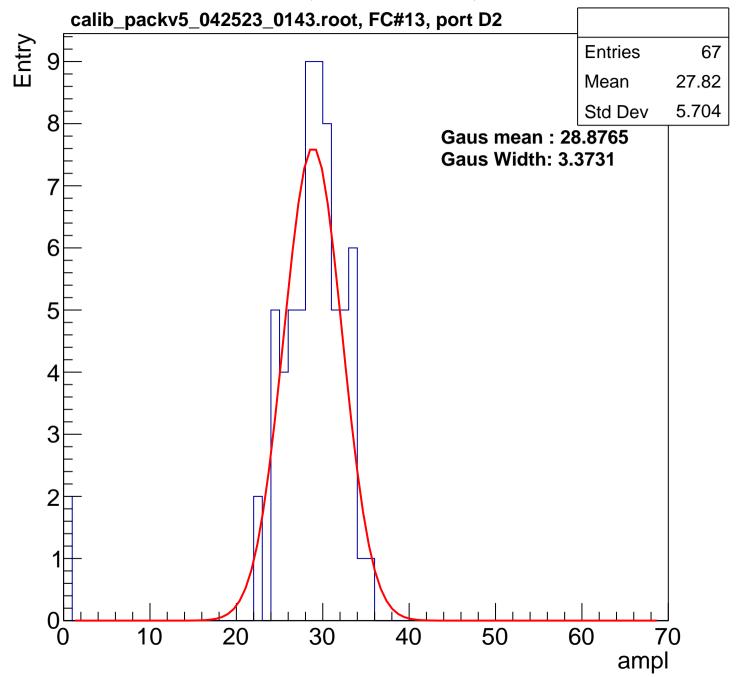


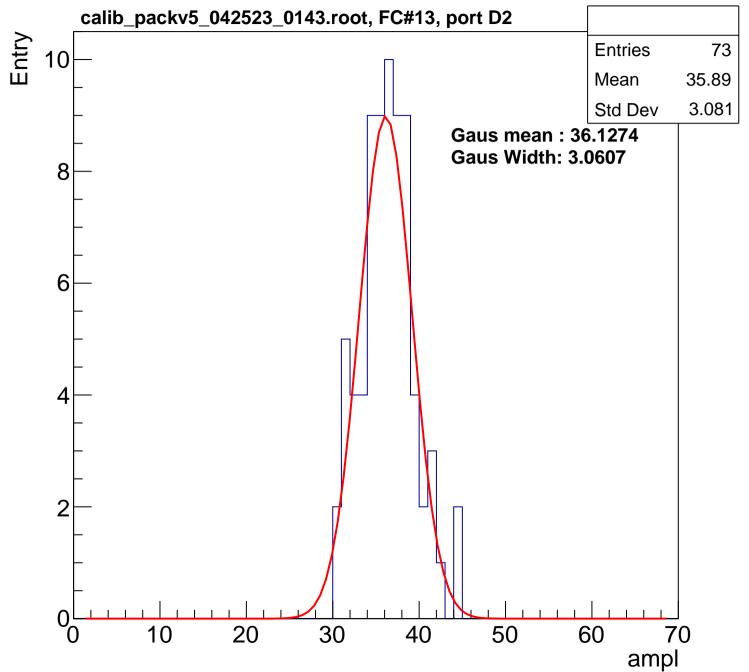


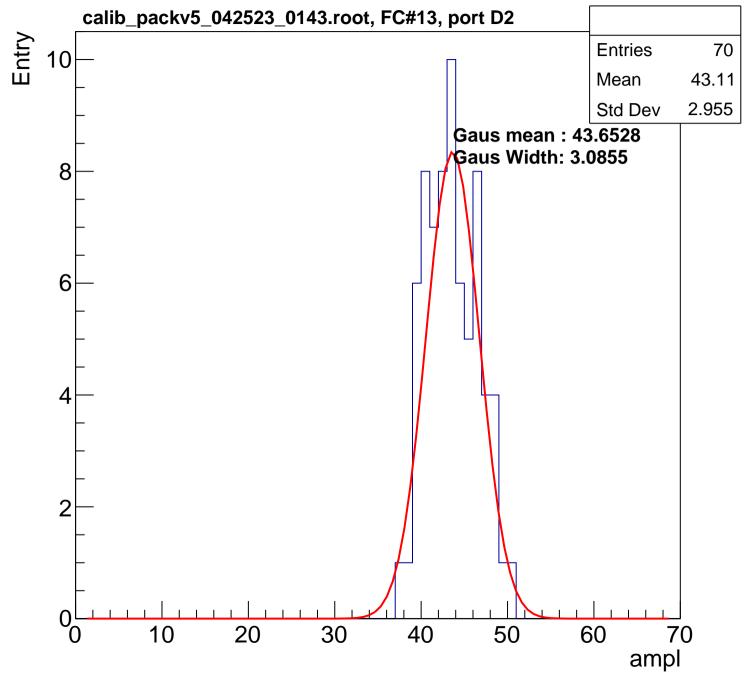


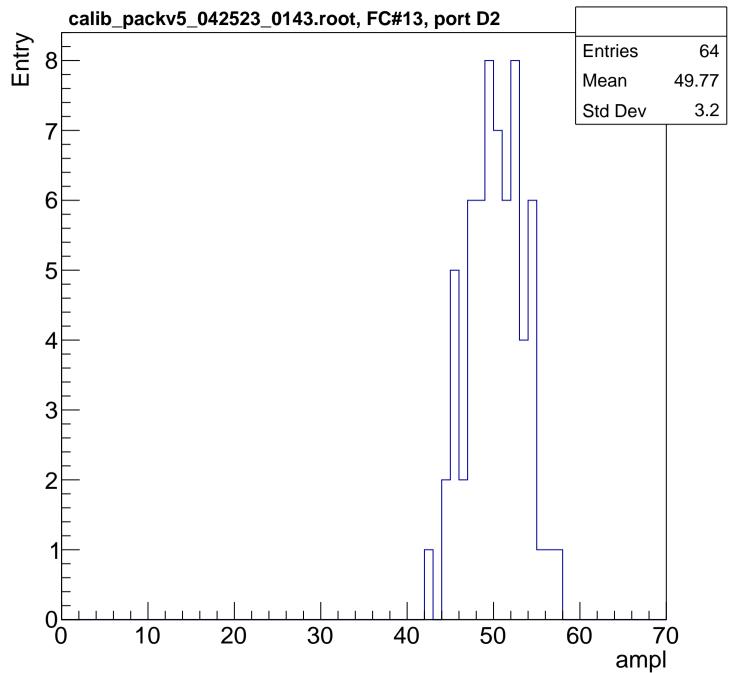


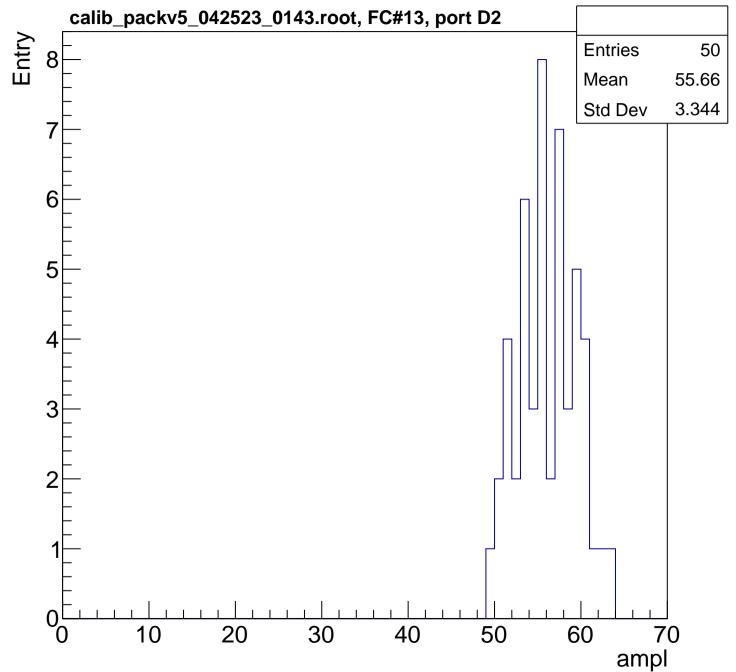


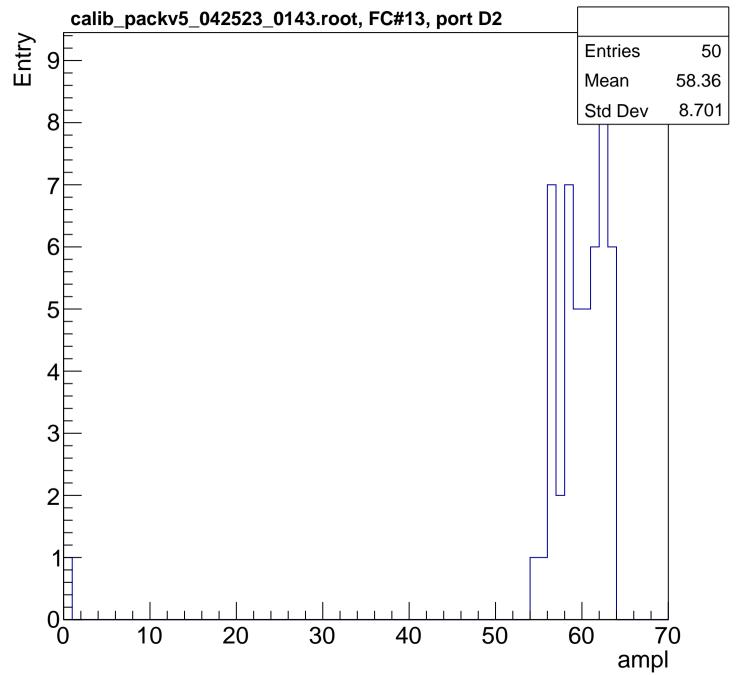


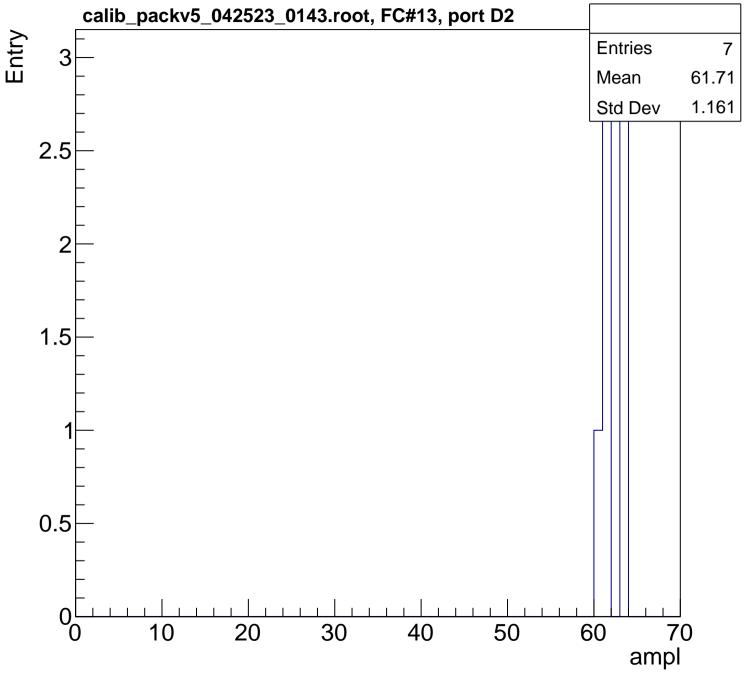


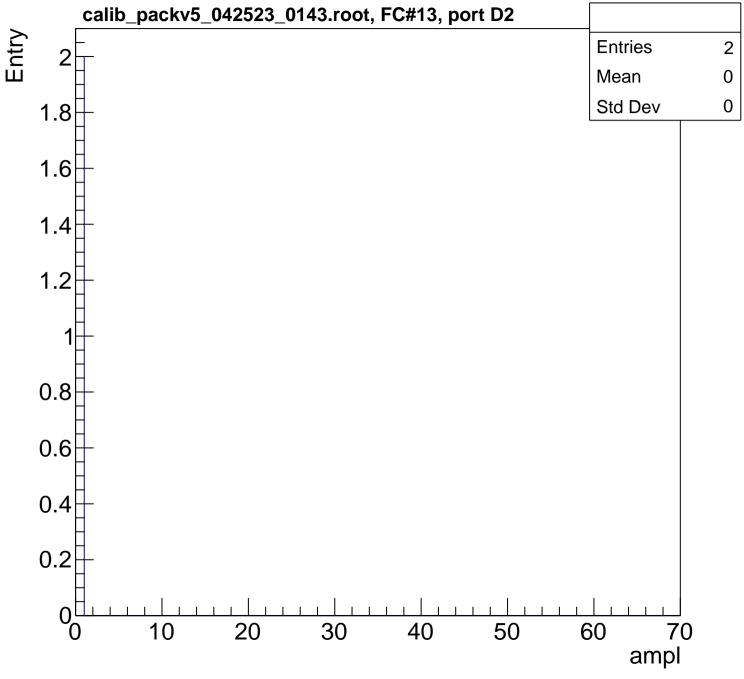


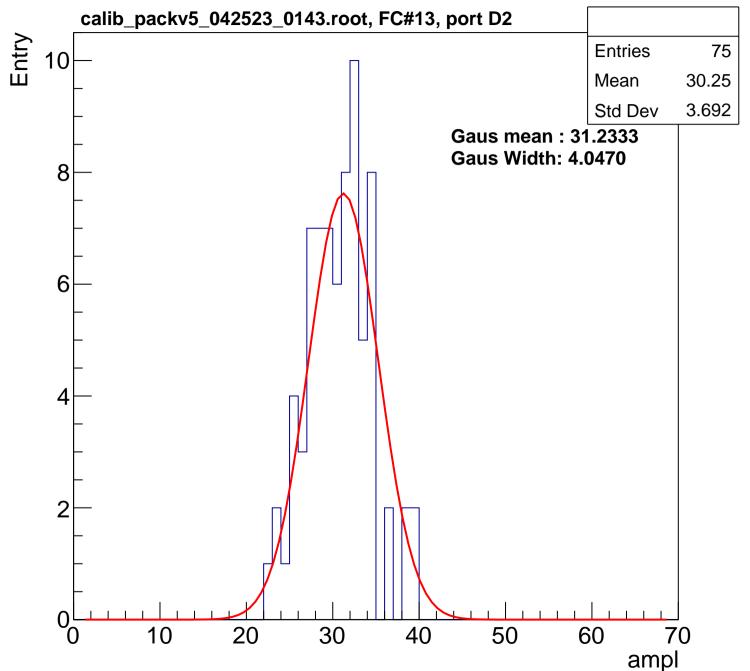


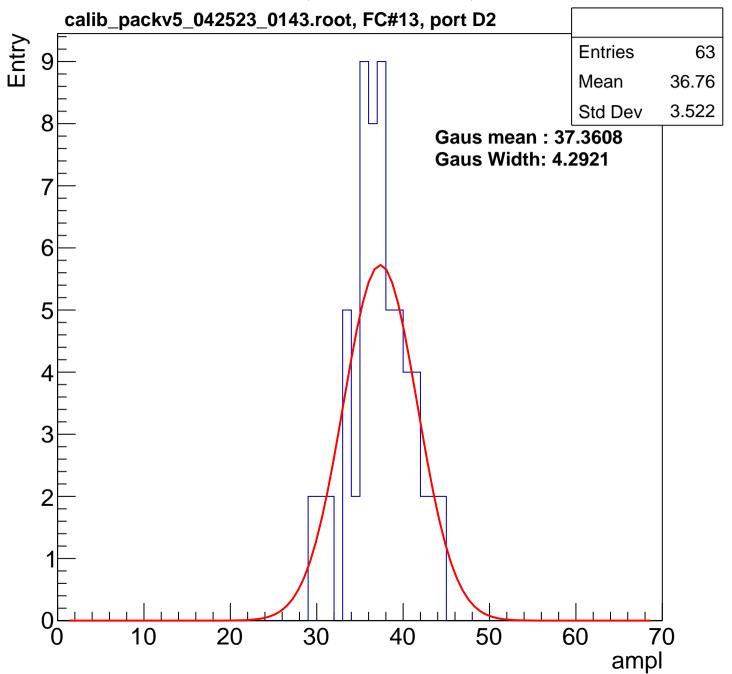


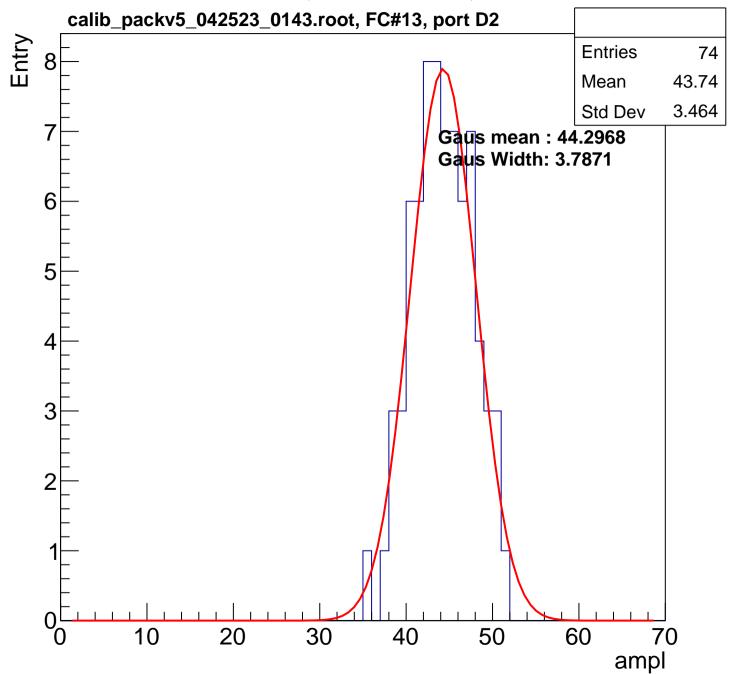


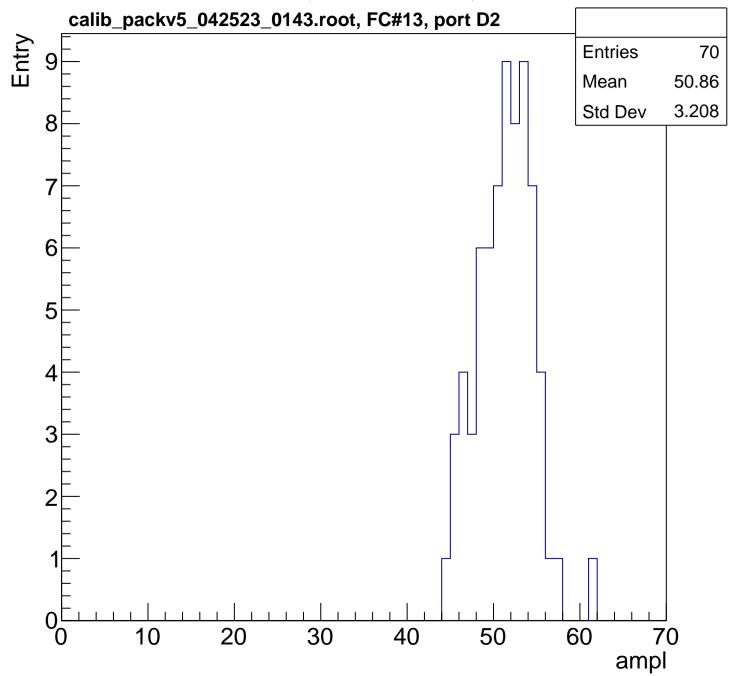


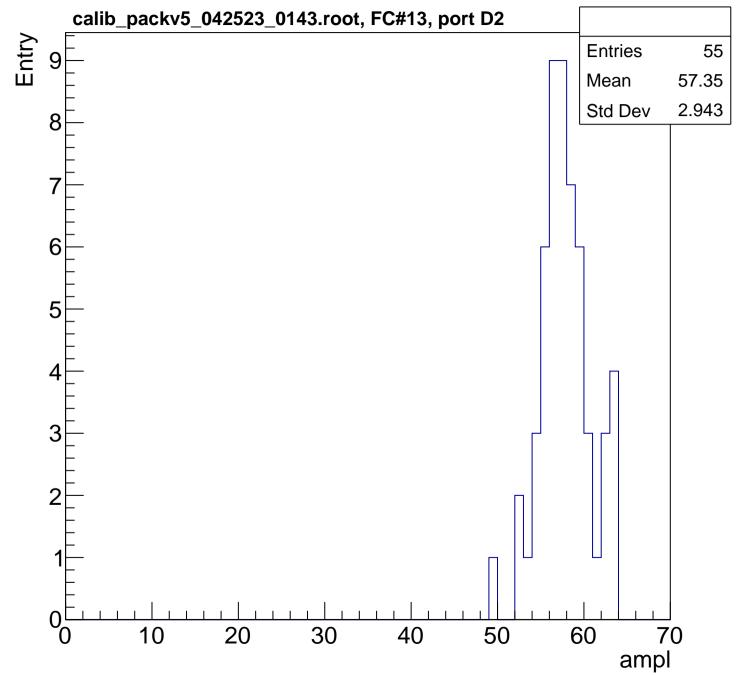


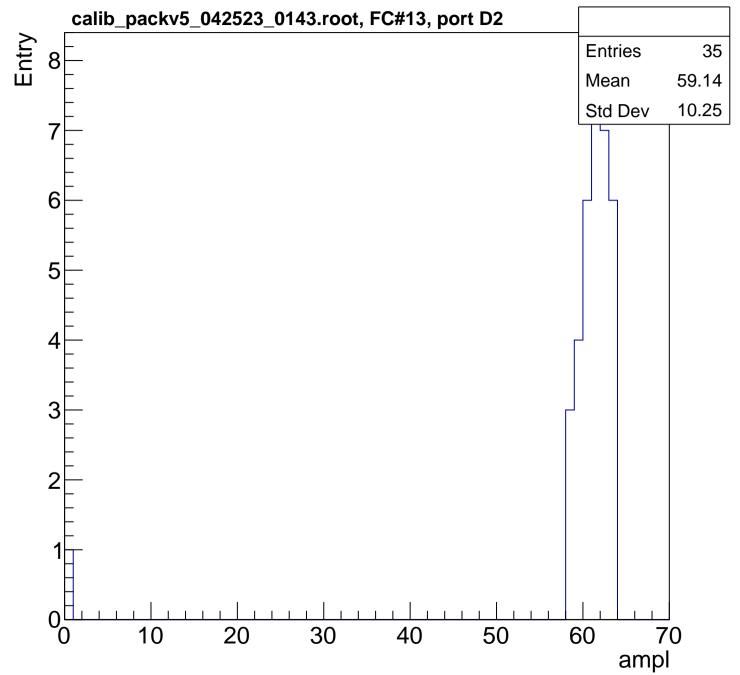












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