

B1L100S, U3-ch0

calib_packv5_042523_0143.root, FC#4, port A2

Entries	374
Mean	44.56
Std Dev	11.36

Turn on : 27.0156

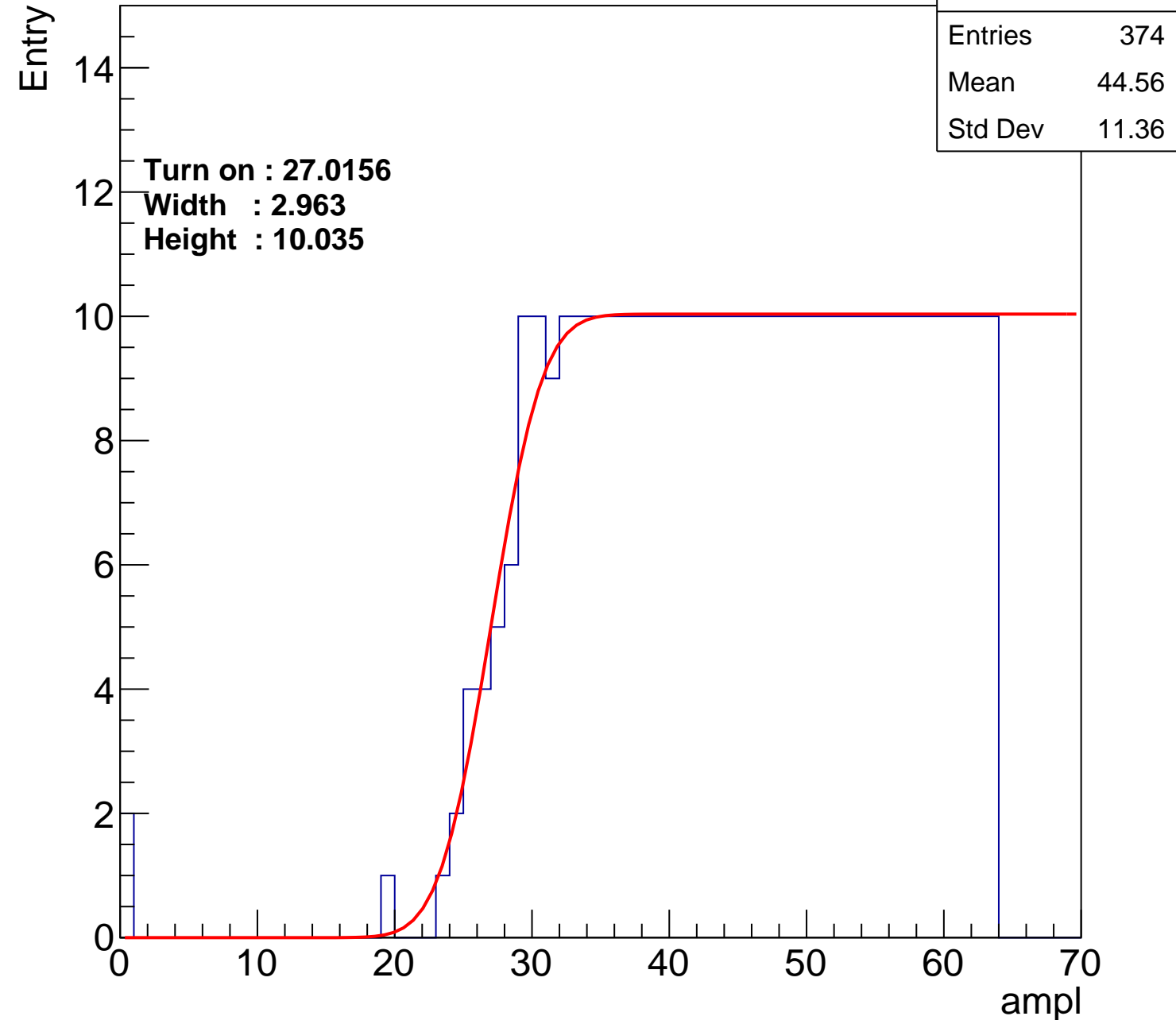
Width : 2.963

Height : 10.035

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U3-ch1

calib_packv5_042523_0143.root, FC#4, port A2

Entries	361
Mean	45.06
Std Dev	11.43

Turn on : 28.6090

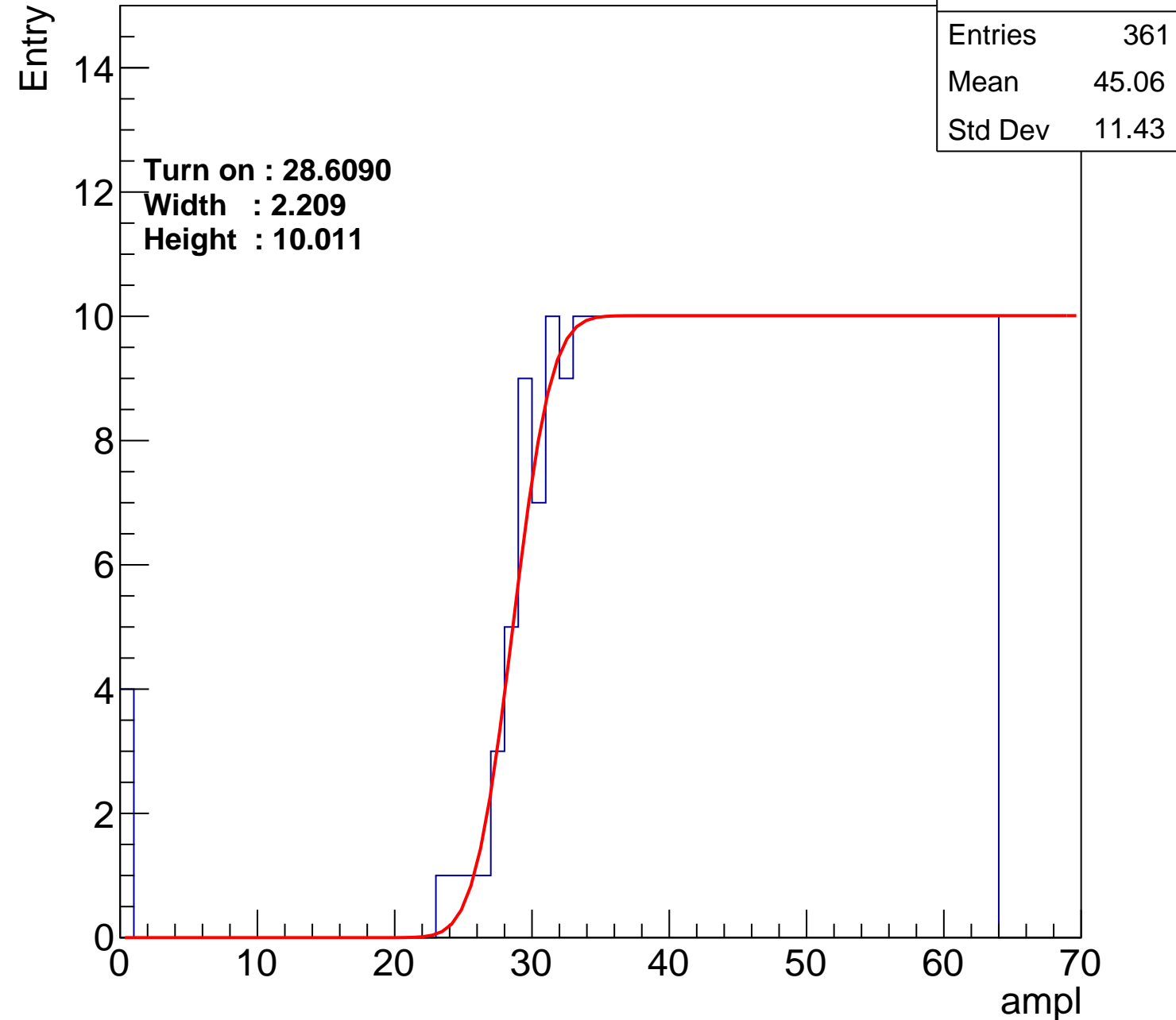
Width : 2.209

Height : 10.011

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U3-ch2

calib_packv5_042523_0143.root, FC#4, port A2

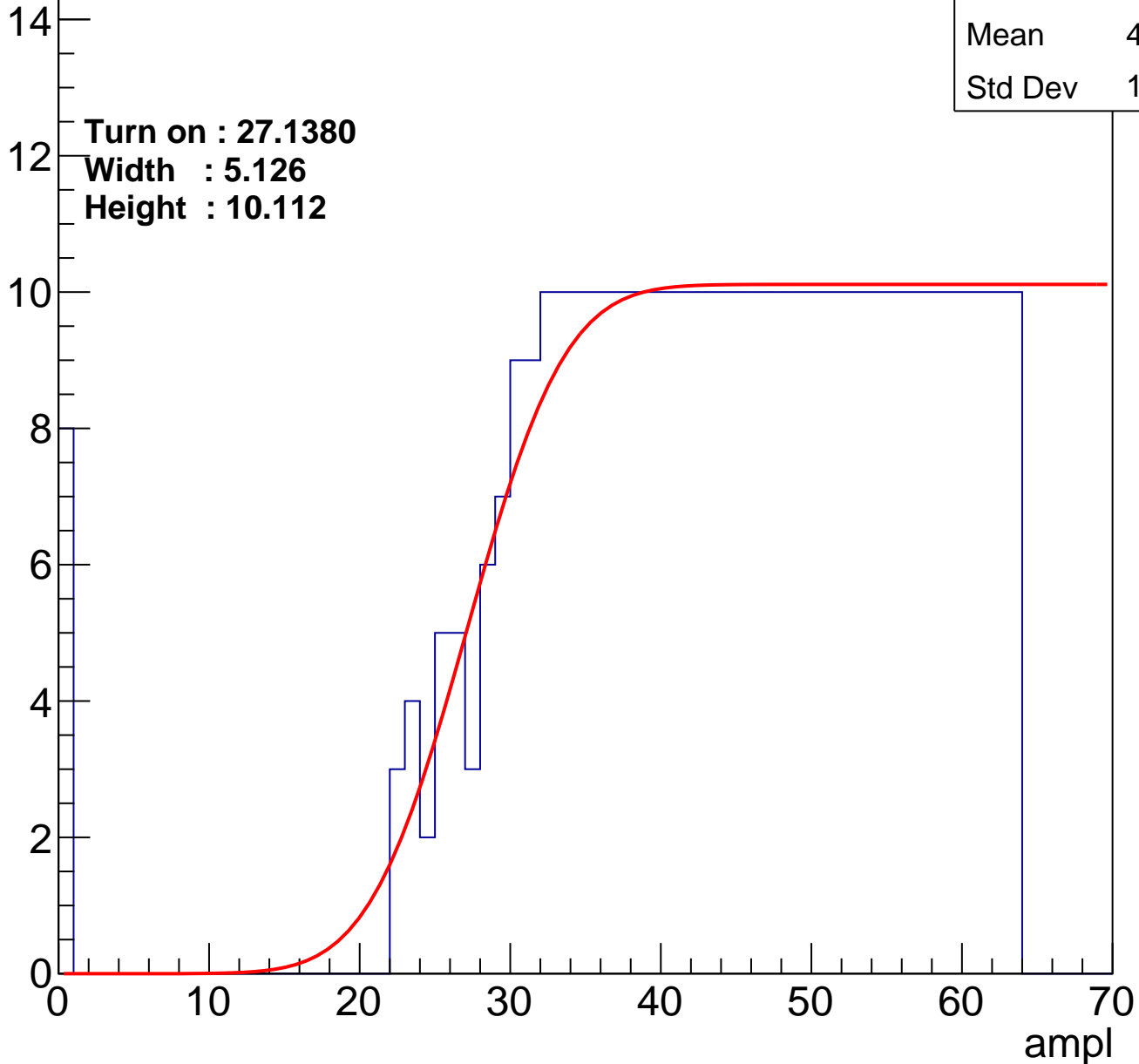
Entries	381
Mean	43.73
Std Dev	12.69

Turn on : 27.1380

Width : 5.126

Height : 10.112

Entry



B1L100S, U3-ch3

calib_packv5_042523_0143.root, FC#4, port A2

Entries	364
Mean	44.8
Std Dev	11.68

Turn on : 28.5531

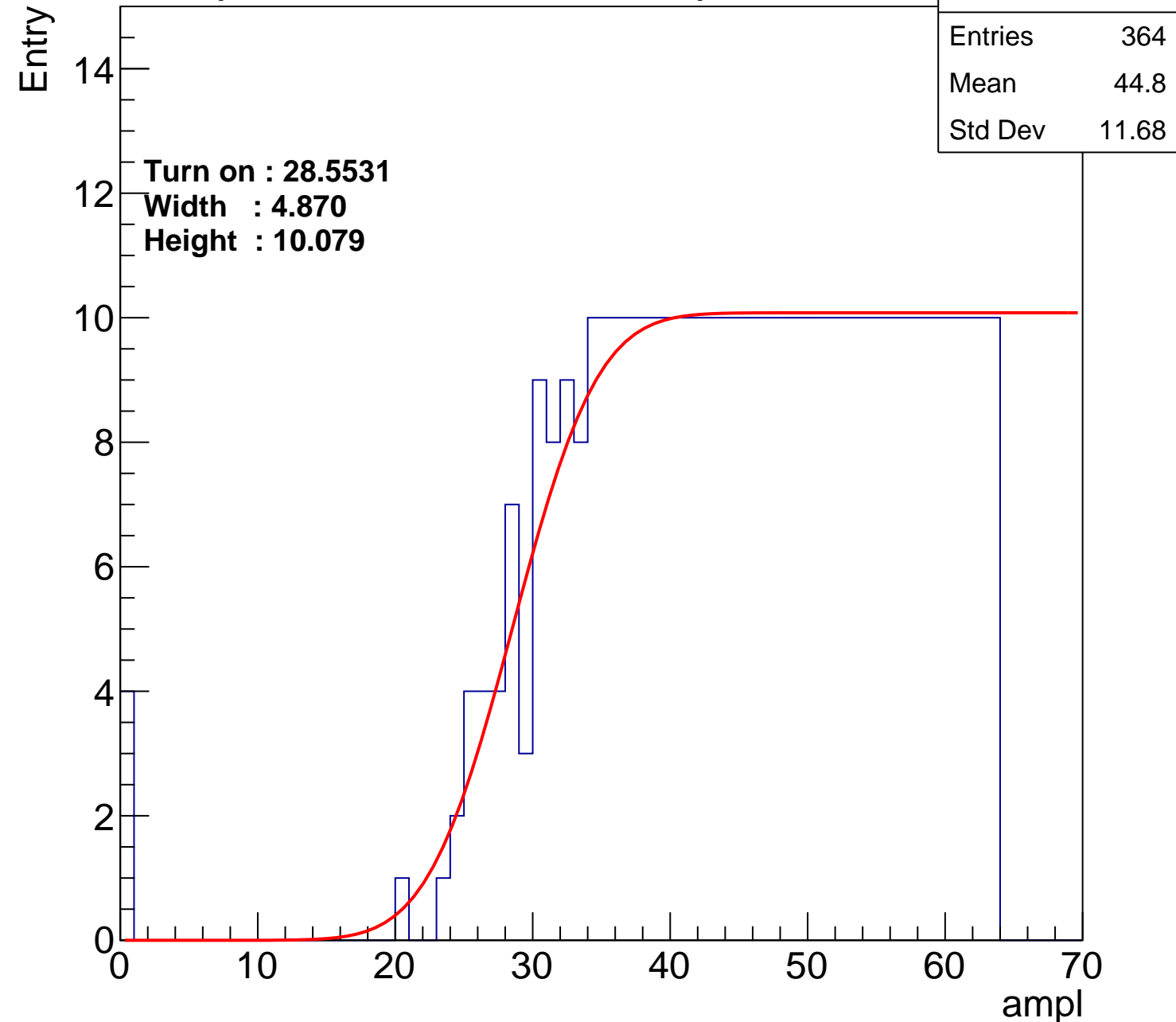
Width : 4.870

Height : 10.079

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U3-ch4

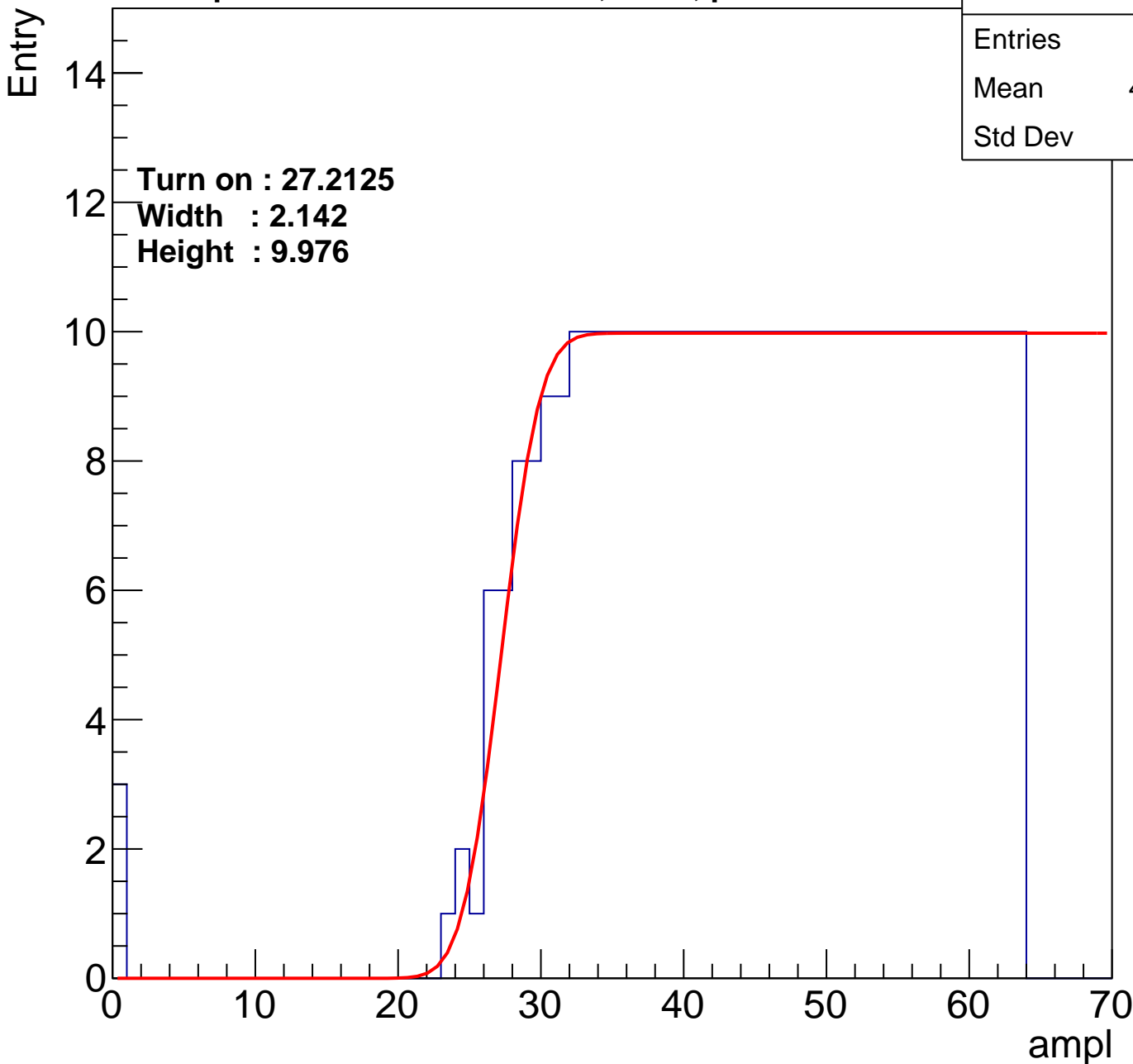
calib_packv5_042523_0143.root, FC#4, port A2

Entries	373
Mean	44.55
Std Dev	11.5

Turn on : 27.2125

Width : 2.142

Height : 9.976



B1L100S, U3-ch5

calib_packv5_042523_0143.root, FC#4, port A2

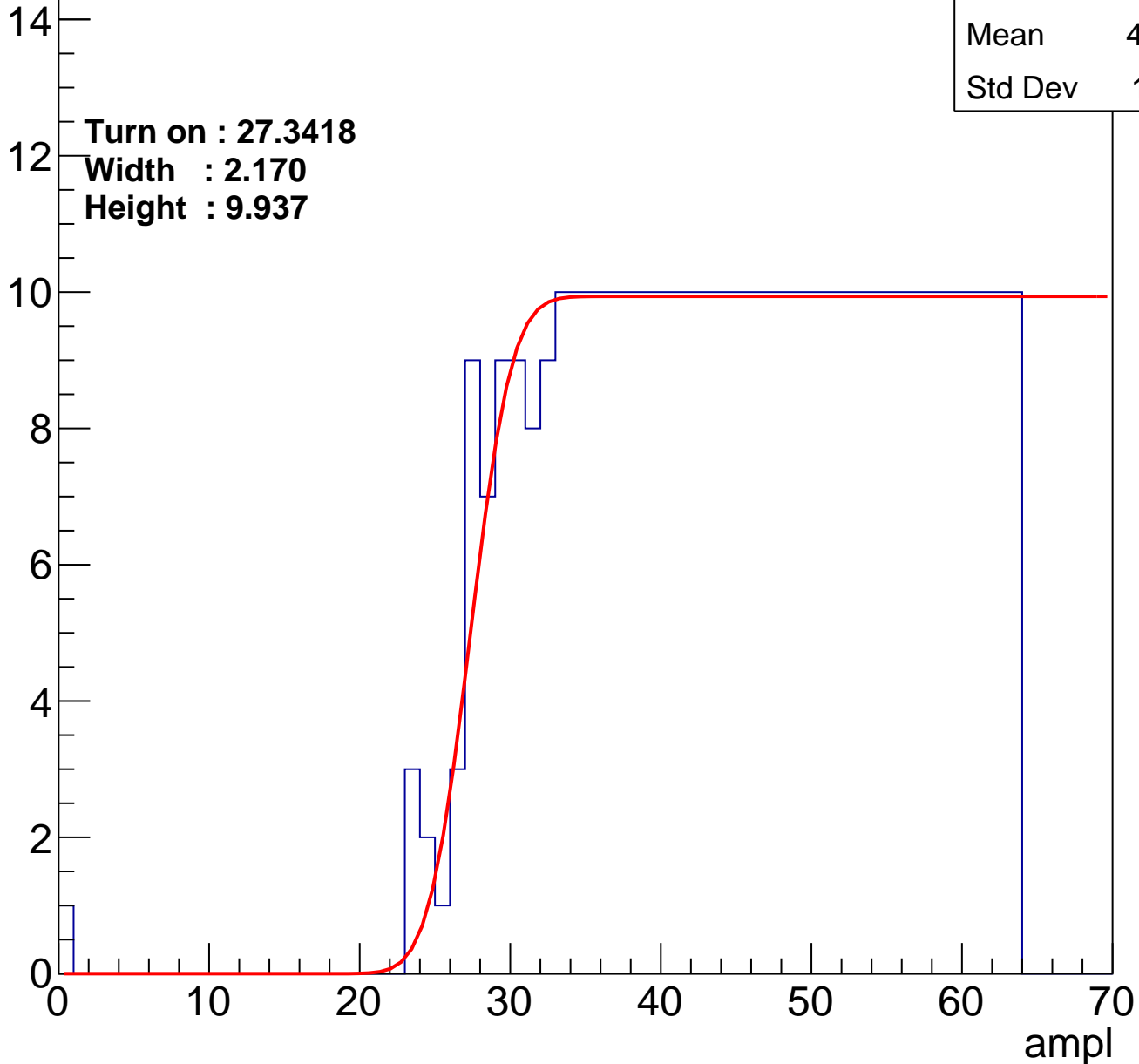
Entries	371
Mean	44.76
Std Dev	11.11

Turn on : 27.3418

Width : 2.170

Height : 9.937

Entry



B1L100S, U3-ch6

calib_packv5_042523_0143.root, FC#4, port A2

Entries	389
Mean	43.72
Std Dev	12.04

Turn on : 25.4636

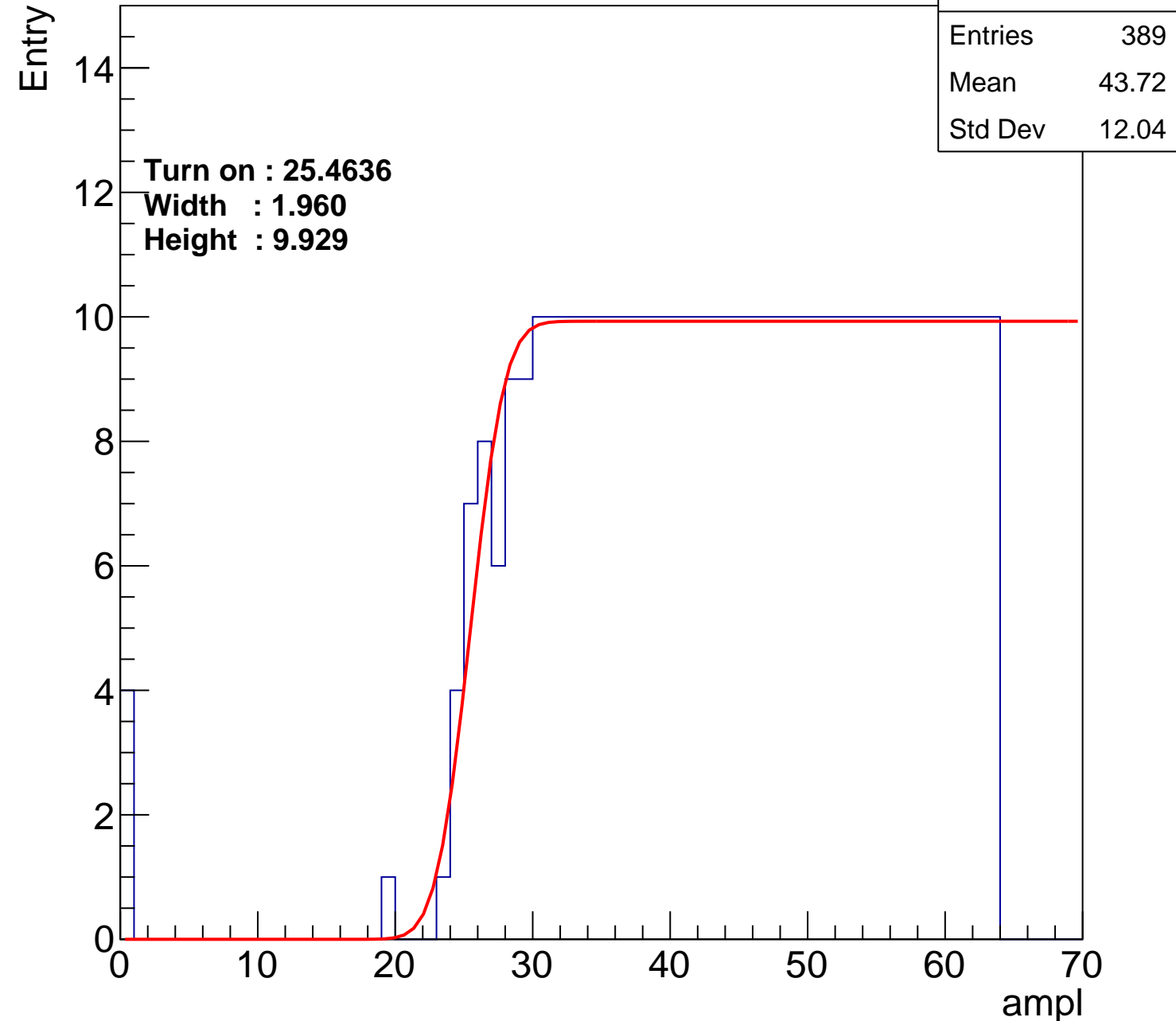
Width : 1.960

Height : 9.929

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U3-ch7

calib_packv5_042523_0143.root, FC#4, port A2

Entries	369
Mean	44.67
Std Dev	11.61

Turn on : 28.1067

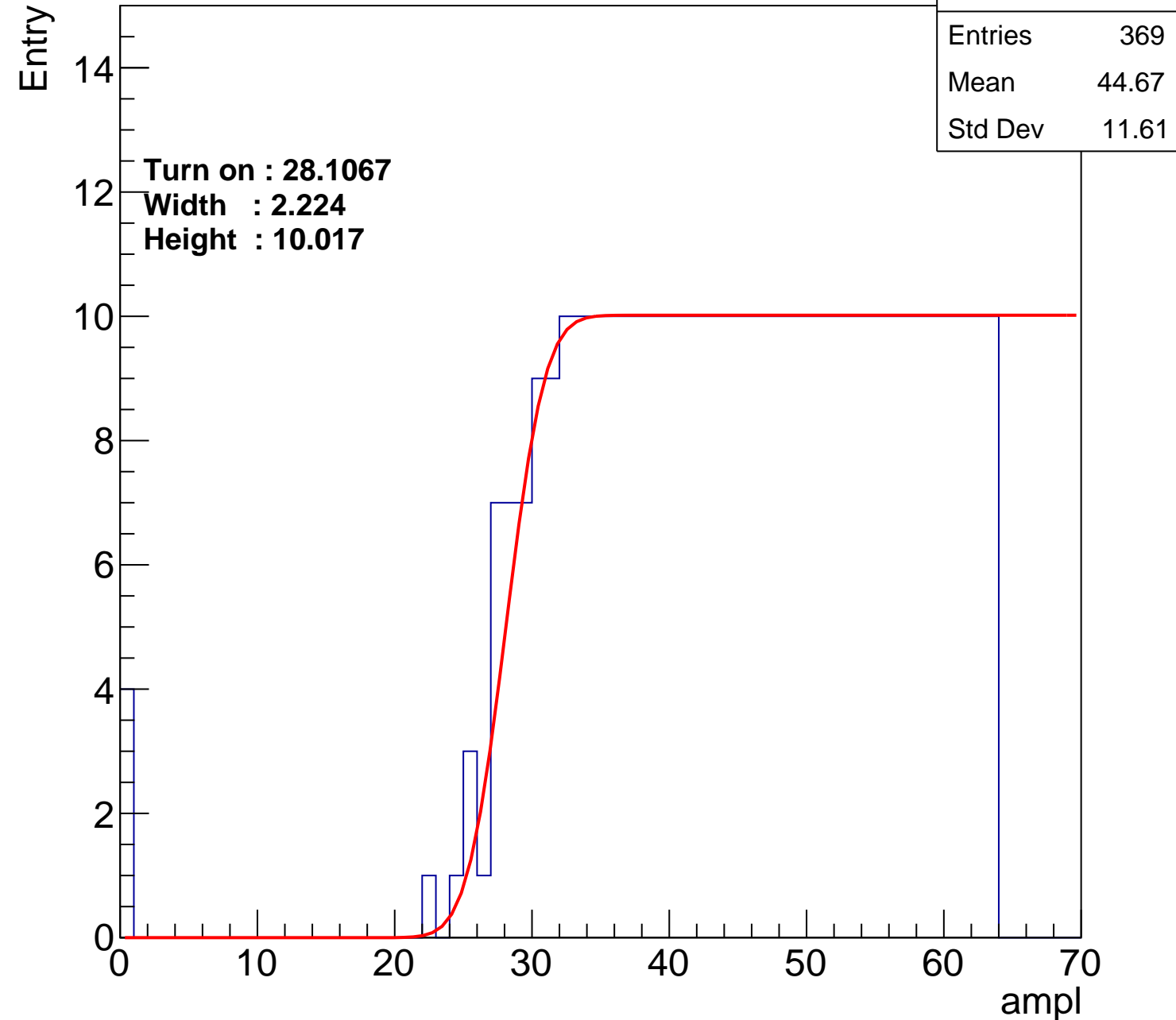
Width : 2.224

Height : 10.017

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U3-ch8

calib_packv5_042523_0143.root, FC#4, port A2

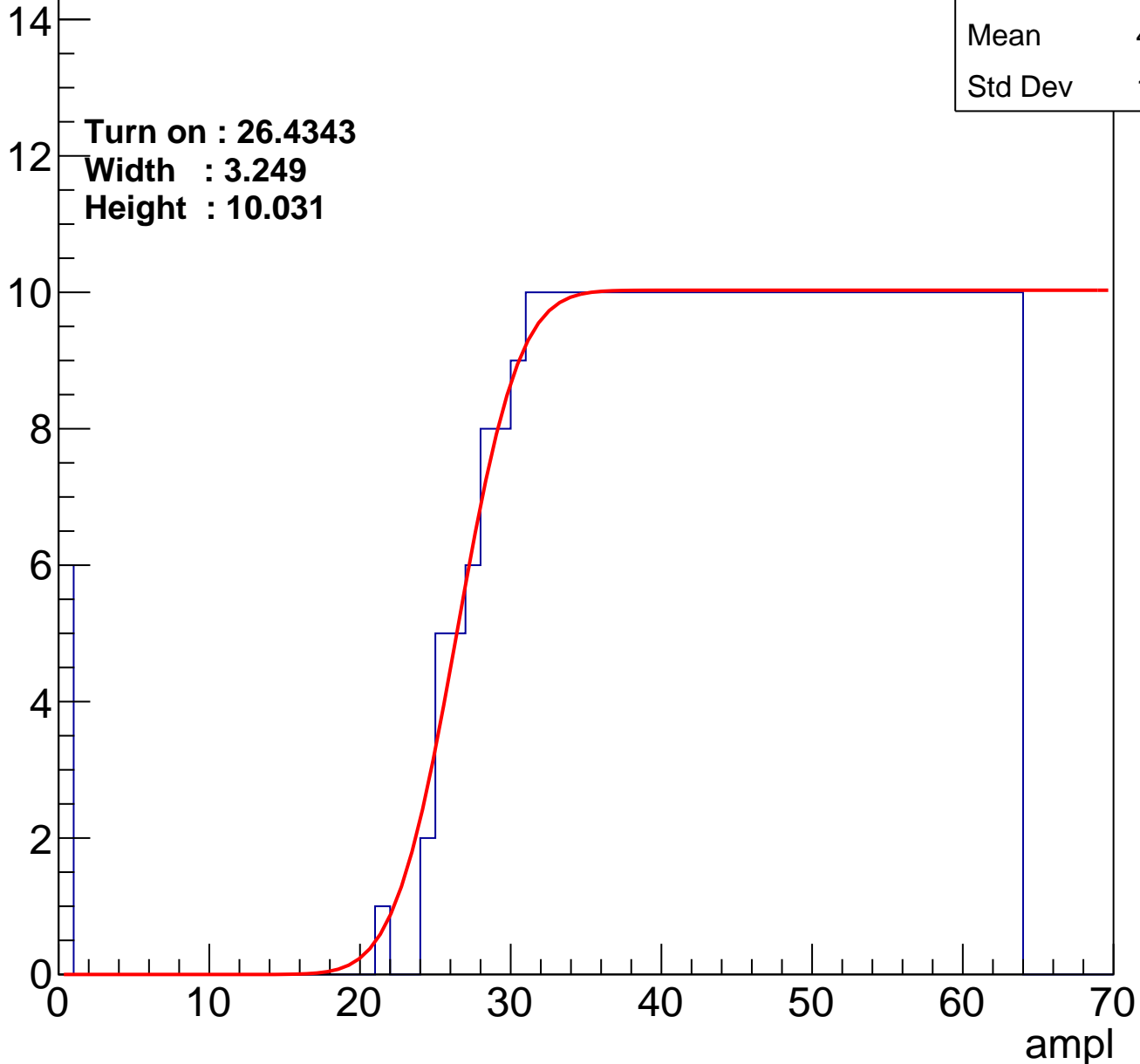
Entries	380
Mean	44.01
Std Dev	12.21

Turn on : 26.4343

Width : 3.249

Height : 10.031

Entry



B1L100S, U3-ch9

calib_packv5_042523_0143.root, FC#4, port A2

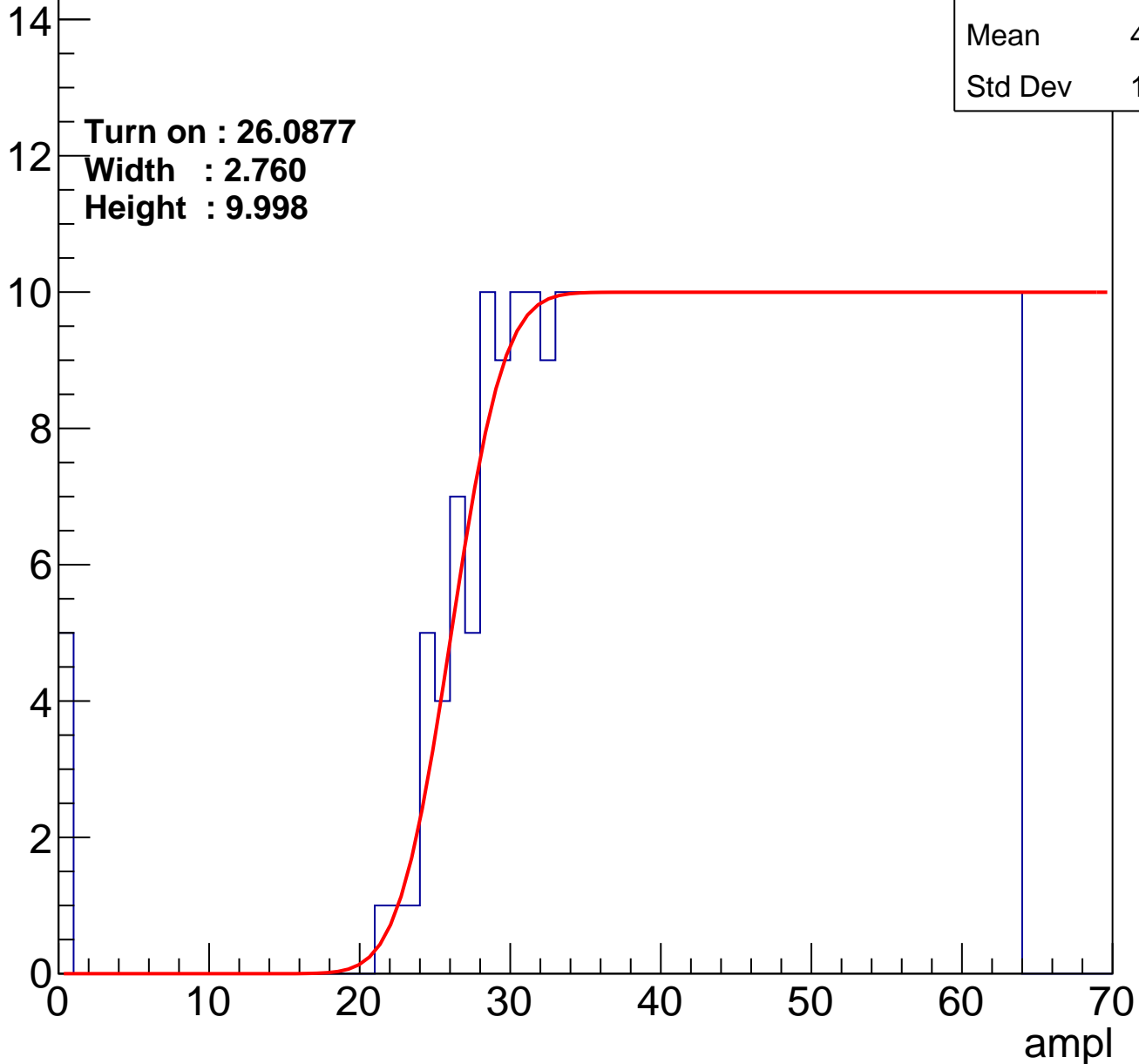
Entries	387
Mean	43.73
Std Dev	12.19

Turn on : 26.0877

Width : 2.760

Height : 9.998

Entry



B1L100S, U3-ch10

calib_packv5_042523_0143.root, FC#4, port A2

Entries	418
Mean	42.32
Std Dev	12.72

Turn on : 22.5469

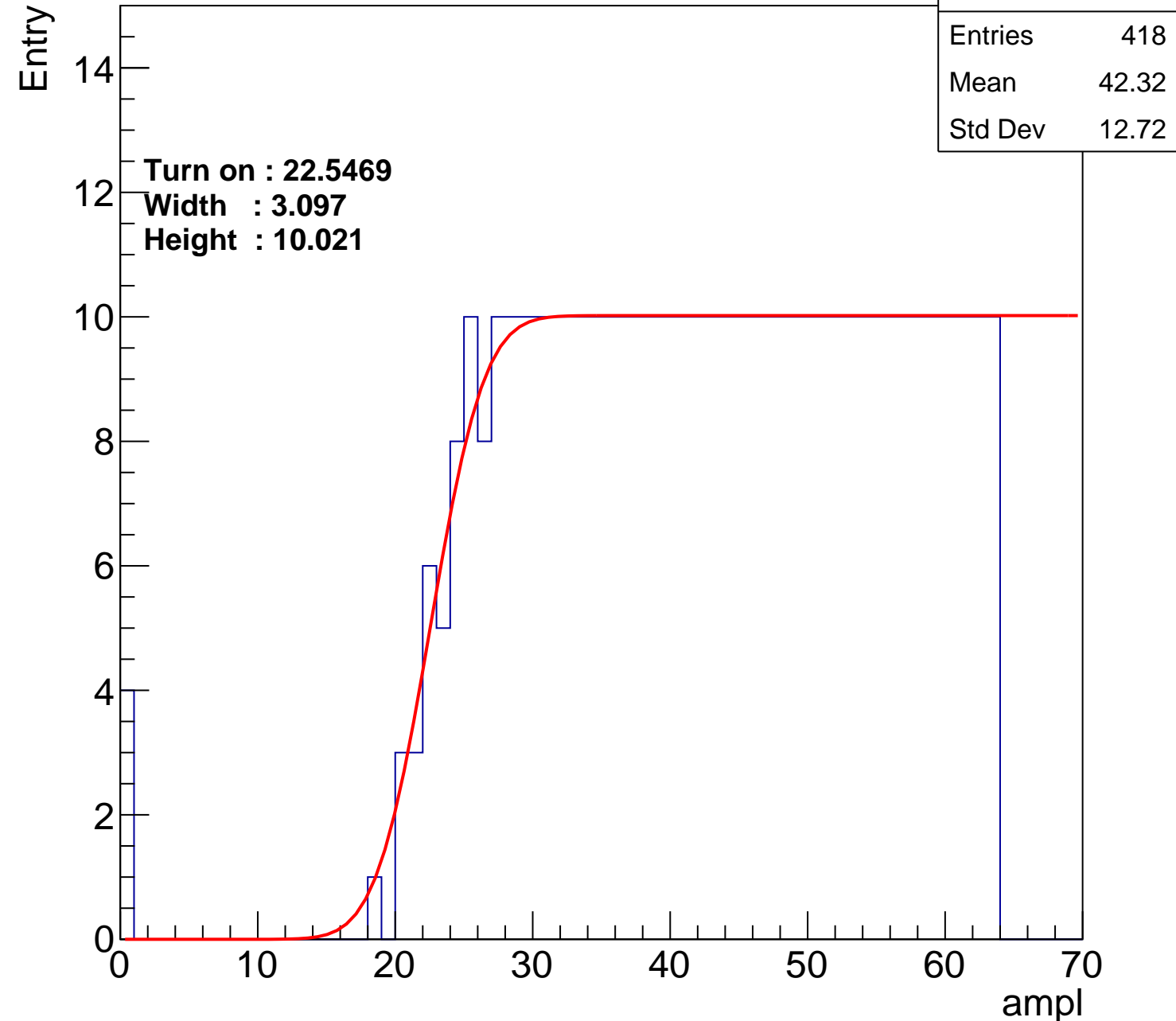
Width : 3.097

Height : 10.021

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U3-ch11

calib_packv5_042523_0143.root, FC#4, port A2

Entries	361
Mean	45.09
Std Dev	11.29

Turn on : 28.4186

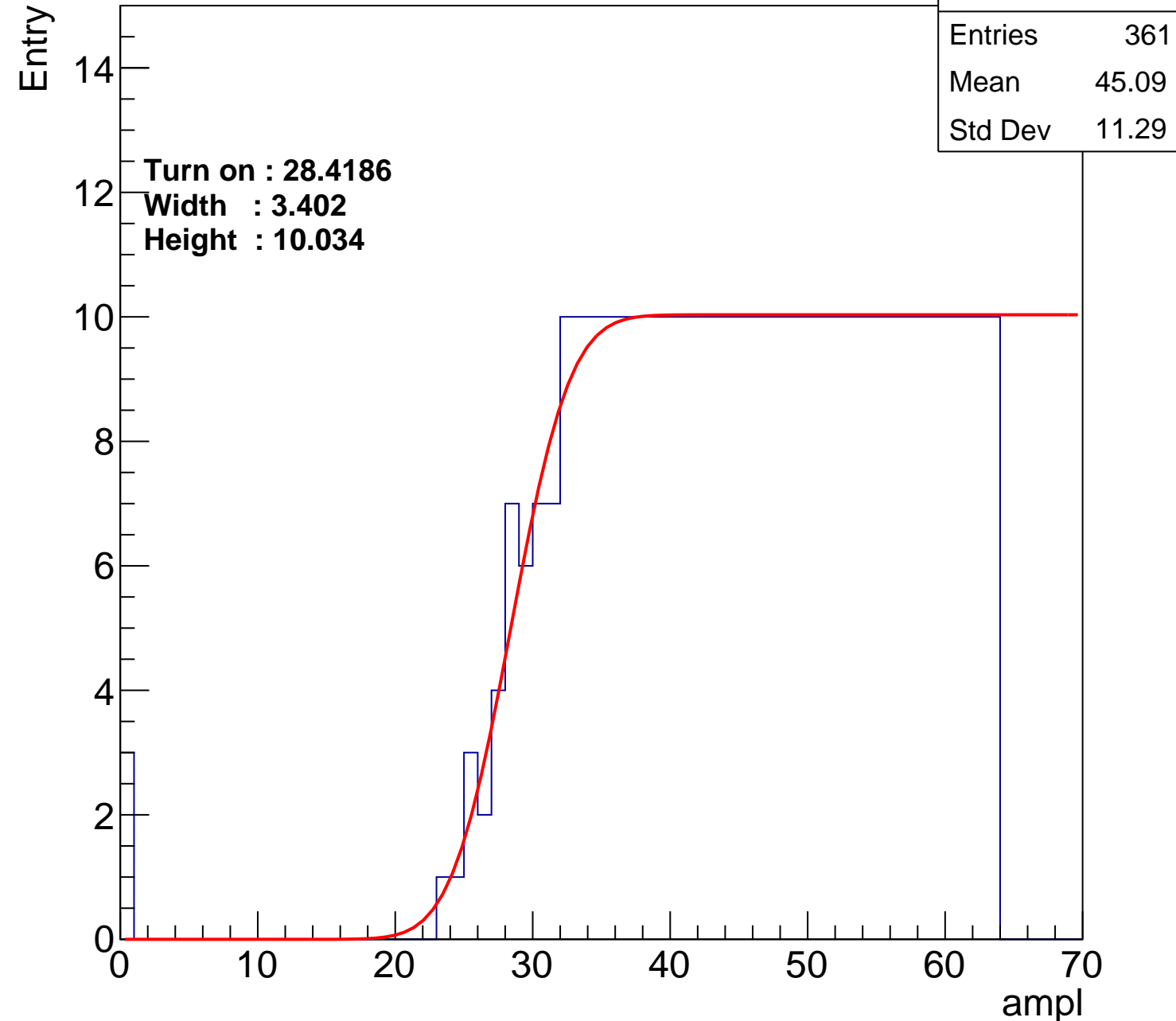
Width : 3.402

Height : 10.034

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U3-ch12

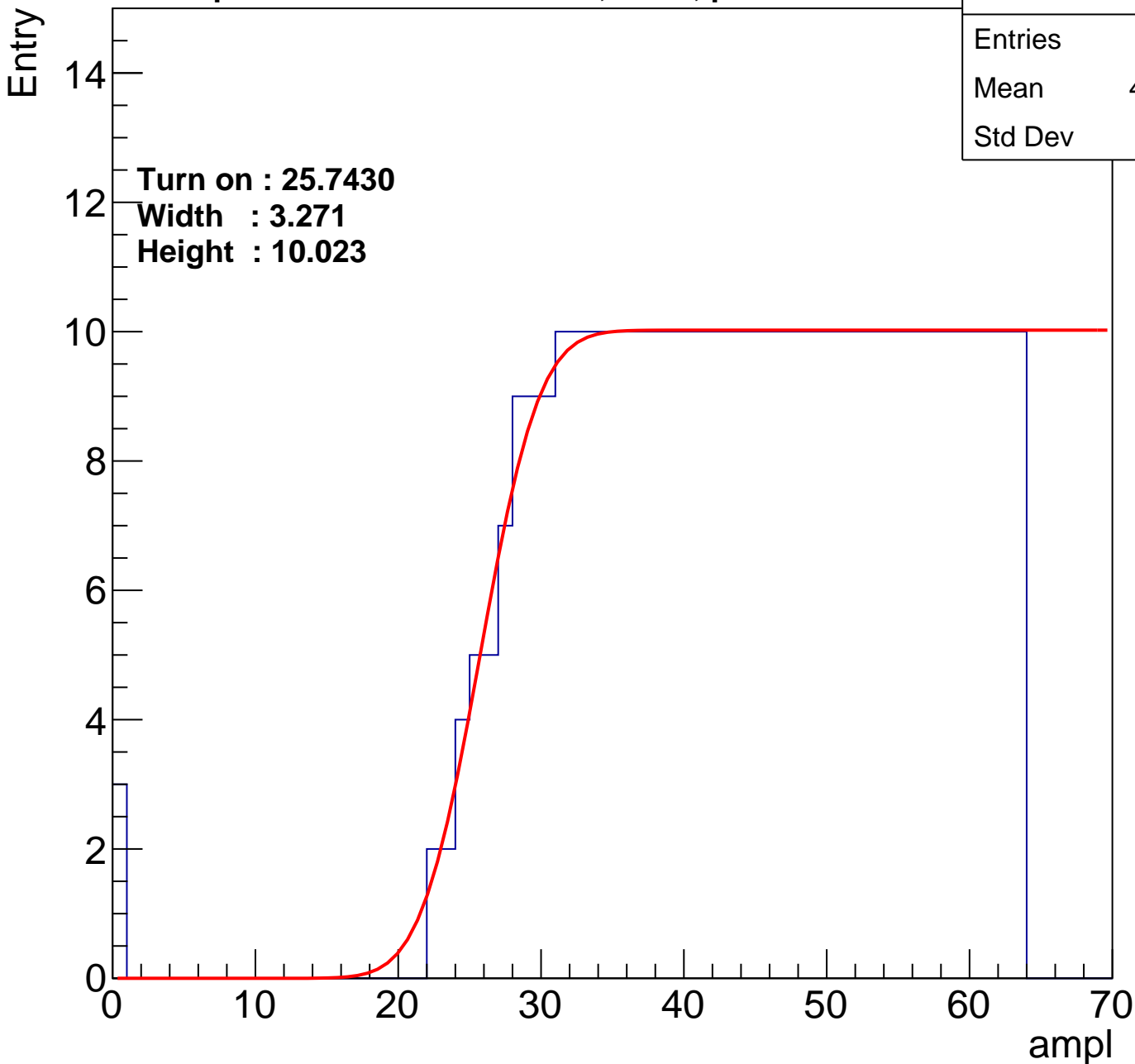
calib_packv5_042523_0143.root, FC#4, port A2

Turn on : 25.7430

Width : 3.271

Height : 10.023

Entries	385
Mean	43.96
Std Dev	11.81



B1L100S, U3-ch13

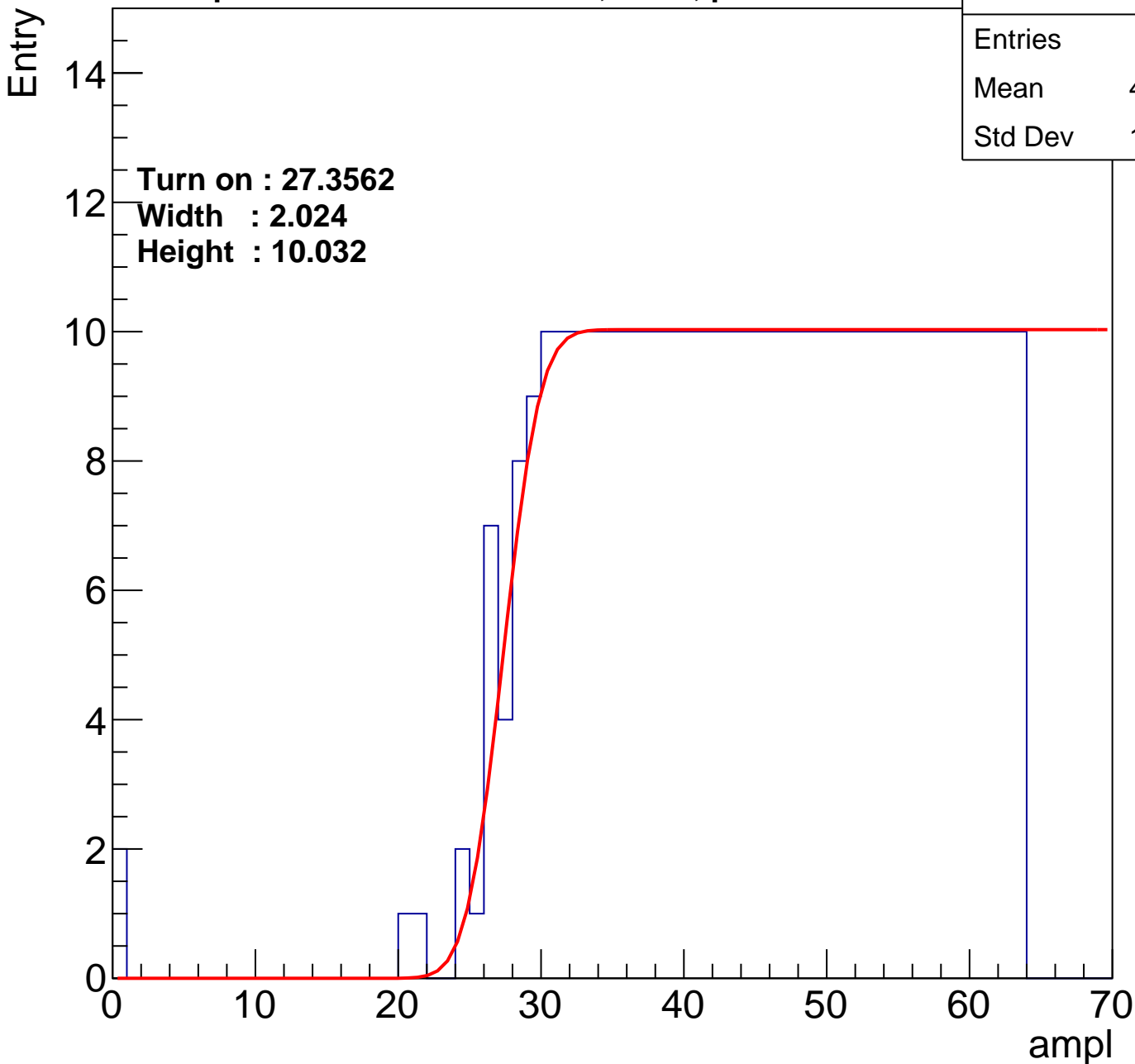
calib_packv5_042523_0143.root, FC#4, port A2

Entries	375
Mean	44.53
Std Dev	11.36

Turn on : 27.3562

Width : 2.024

Height : 10.032



B1L100S, U3-ch14

calib_packv5_042523_0143.root, FC#4, port A2

Entries	385
Mean	43.81
Std Dev	12.16

Turn on : 25.7180

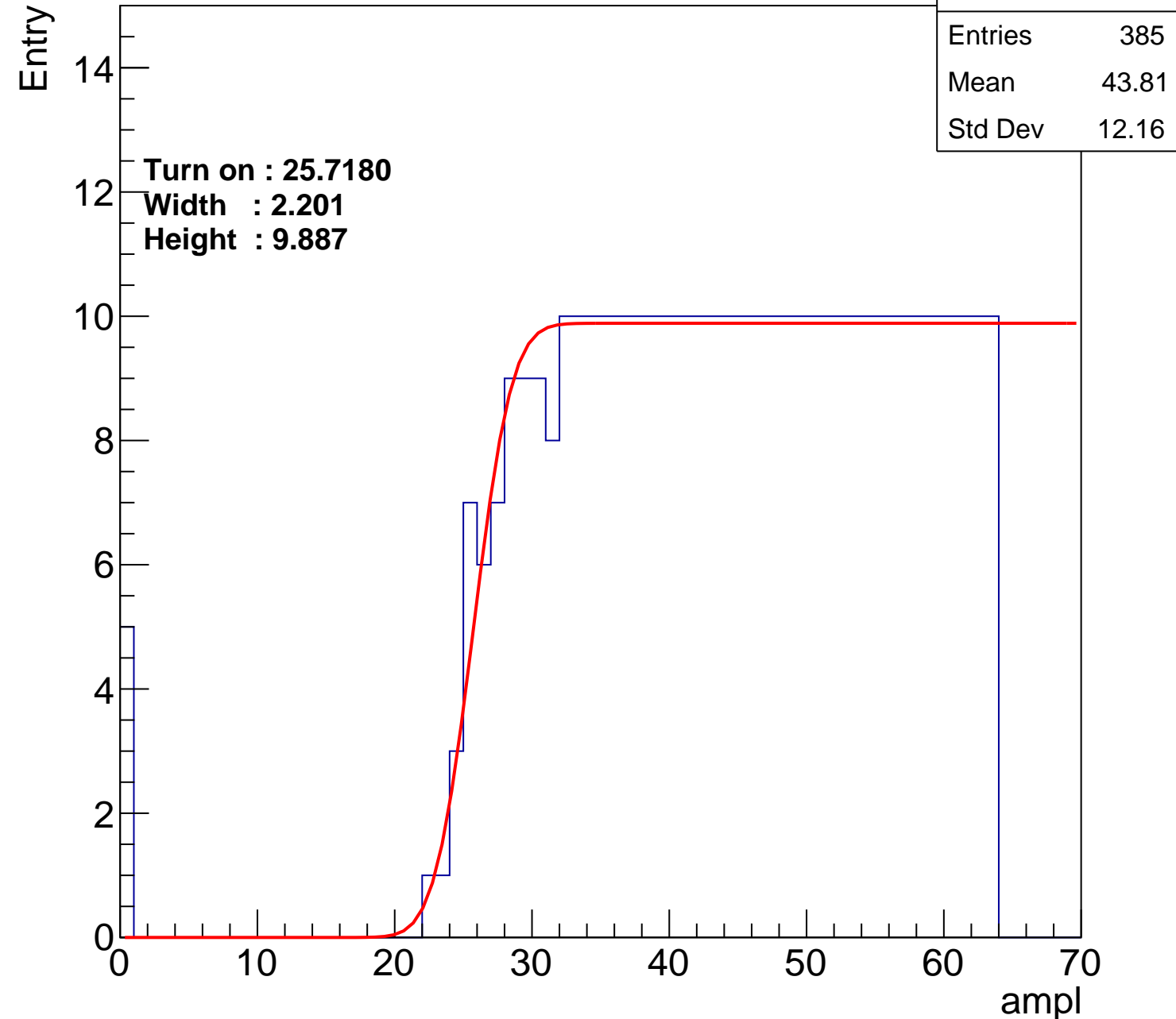
Width : 2.201

Height : 9.887

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U3-ch15

calib_packv5_042523_0143.root, FC#4, port A2

Entries	391
Mean	43.73
Std Dev	11.79

Turn on : 25.9611

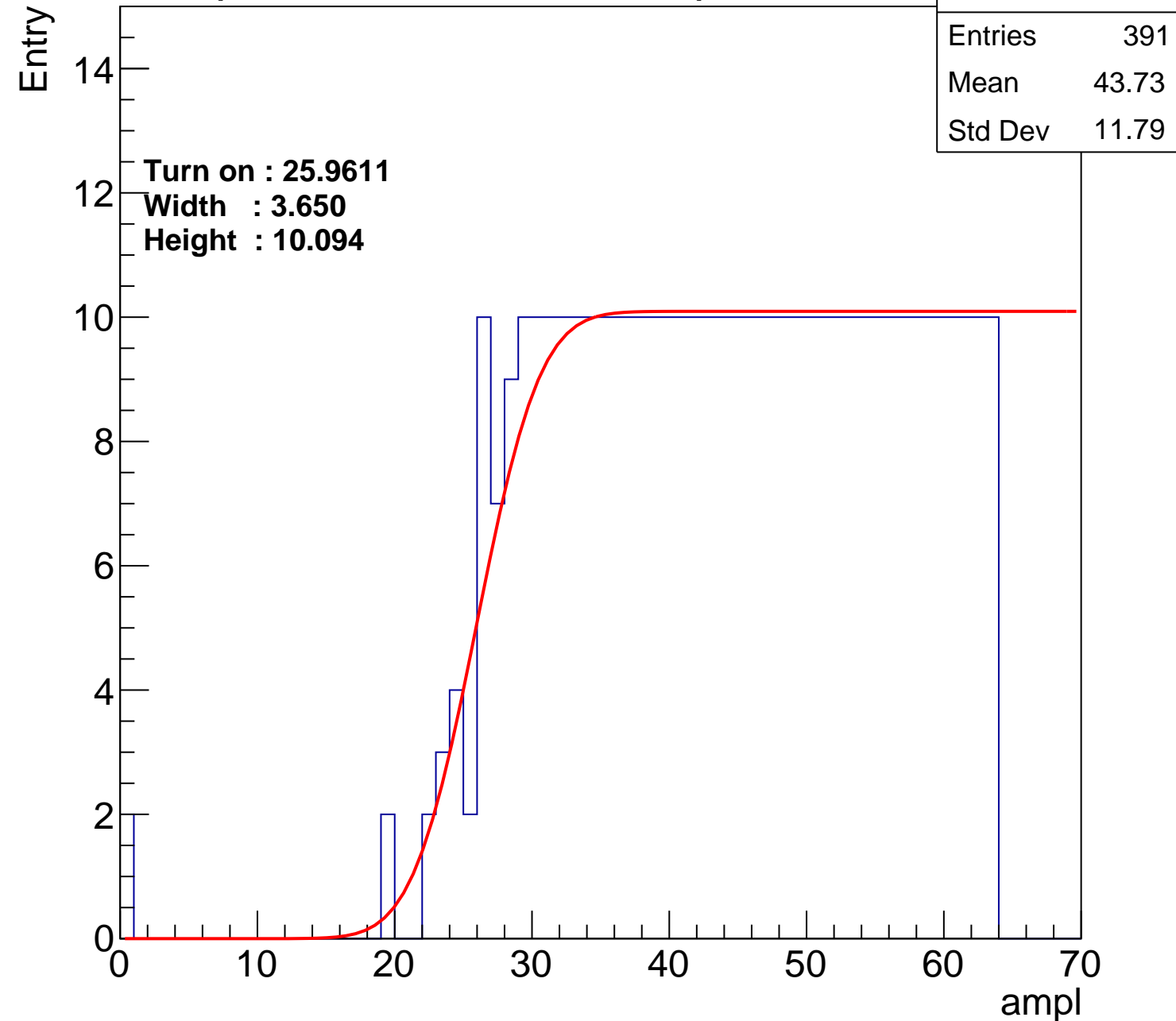
Width : 3.650

Height : 10.094

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U3-ch16

calib_packv5_042523_0143.root, FC#4, port A2

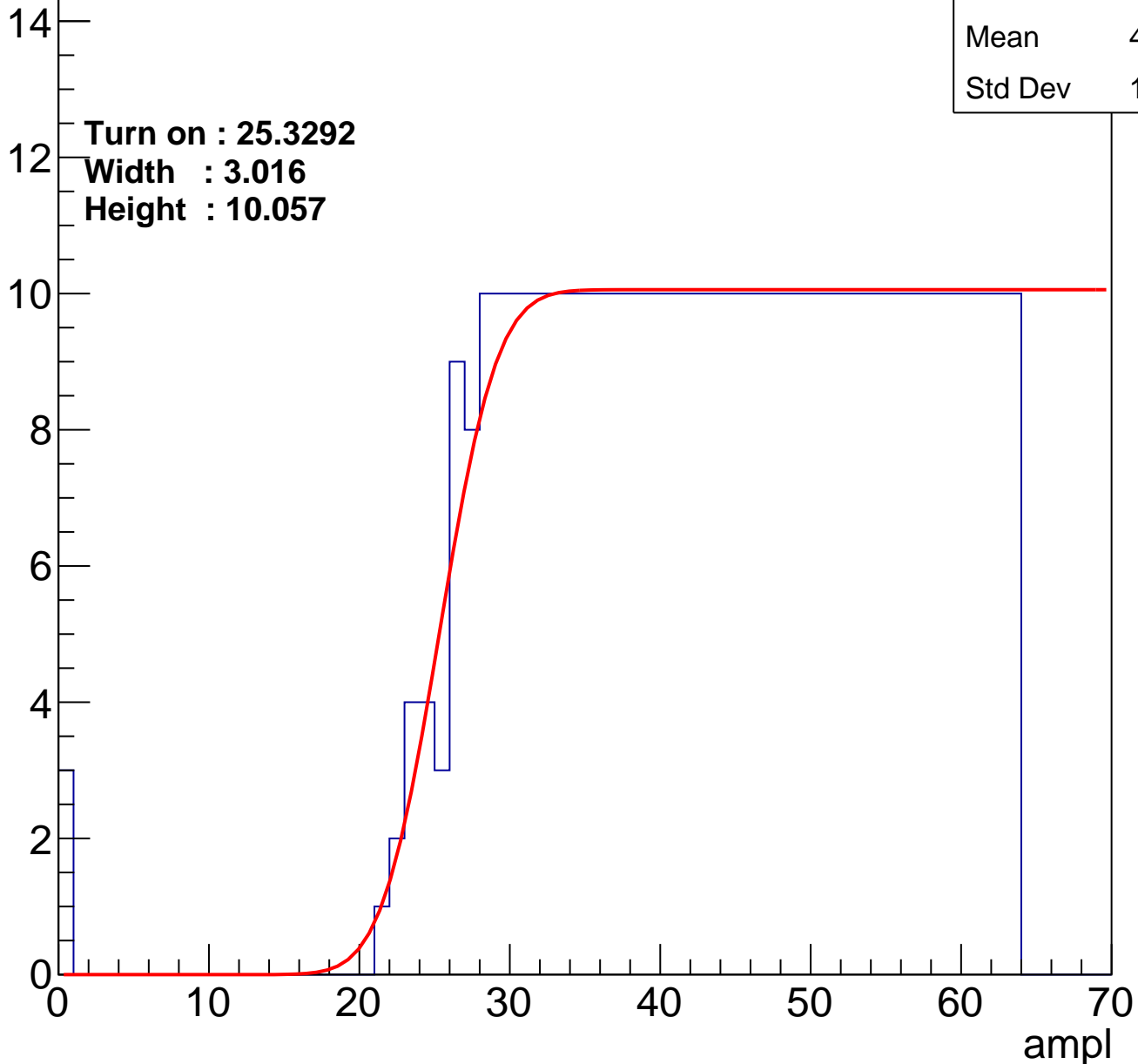
Entries	394
Mean	43.55
Std Dev	11.98

Turn on : 25.3292

Width : 3.016

Height : 10.057

Entry



B1L100S, U3-ch17

calib_packv5_042523_0143.root, FC#4, port A2

Entries	377
Mean	44.31
Std Dev	11.75

Turn on : 26.7981

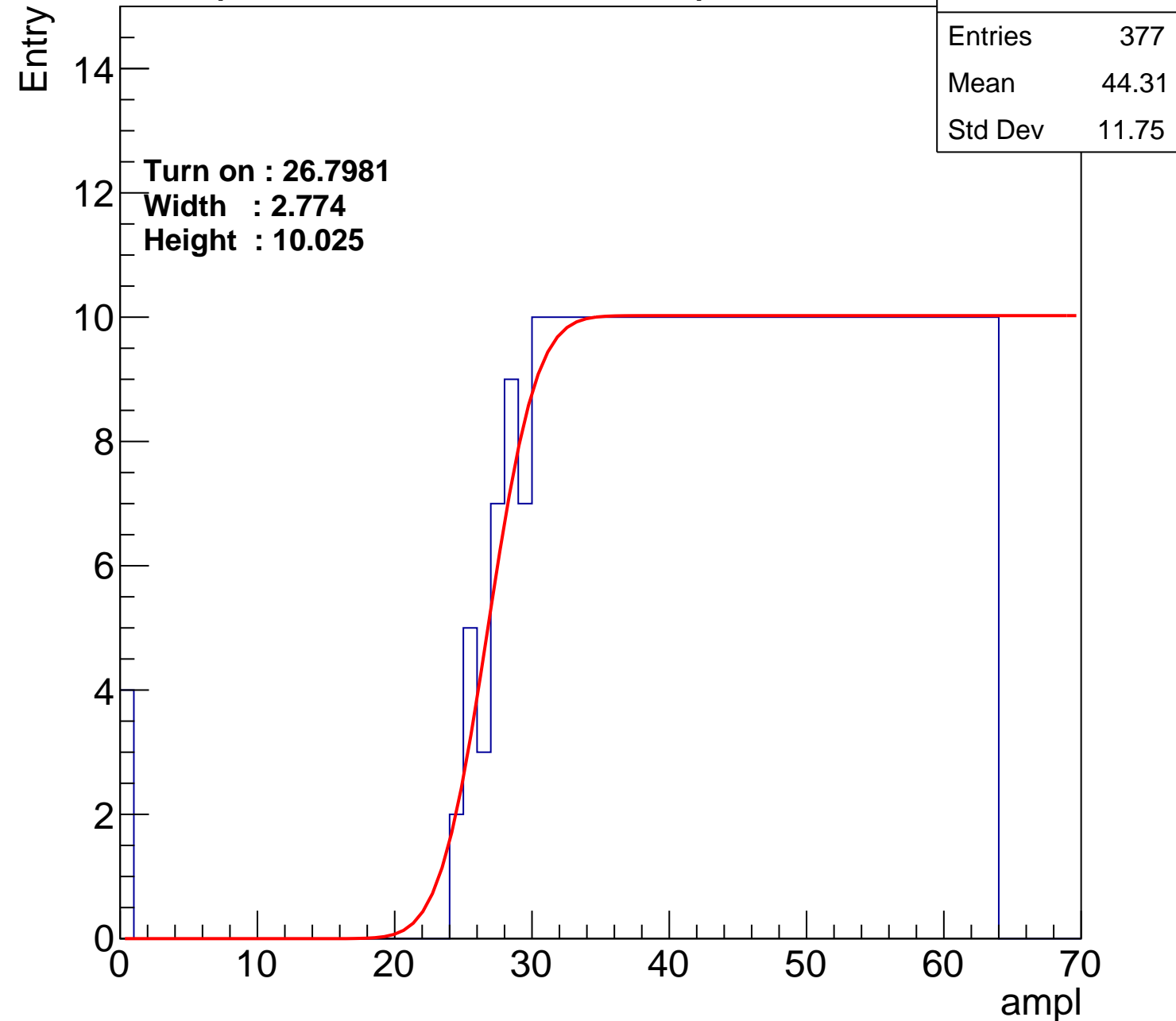
Width : 2.774

Height : 10.025

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U3-ch18

calib_packv5_042523_0143.root, FC#4, port A2

Entries	385
Mean	43.94
Std Dev	11.84

Turn on : 25.9835

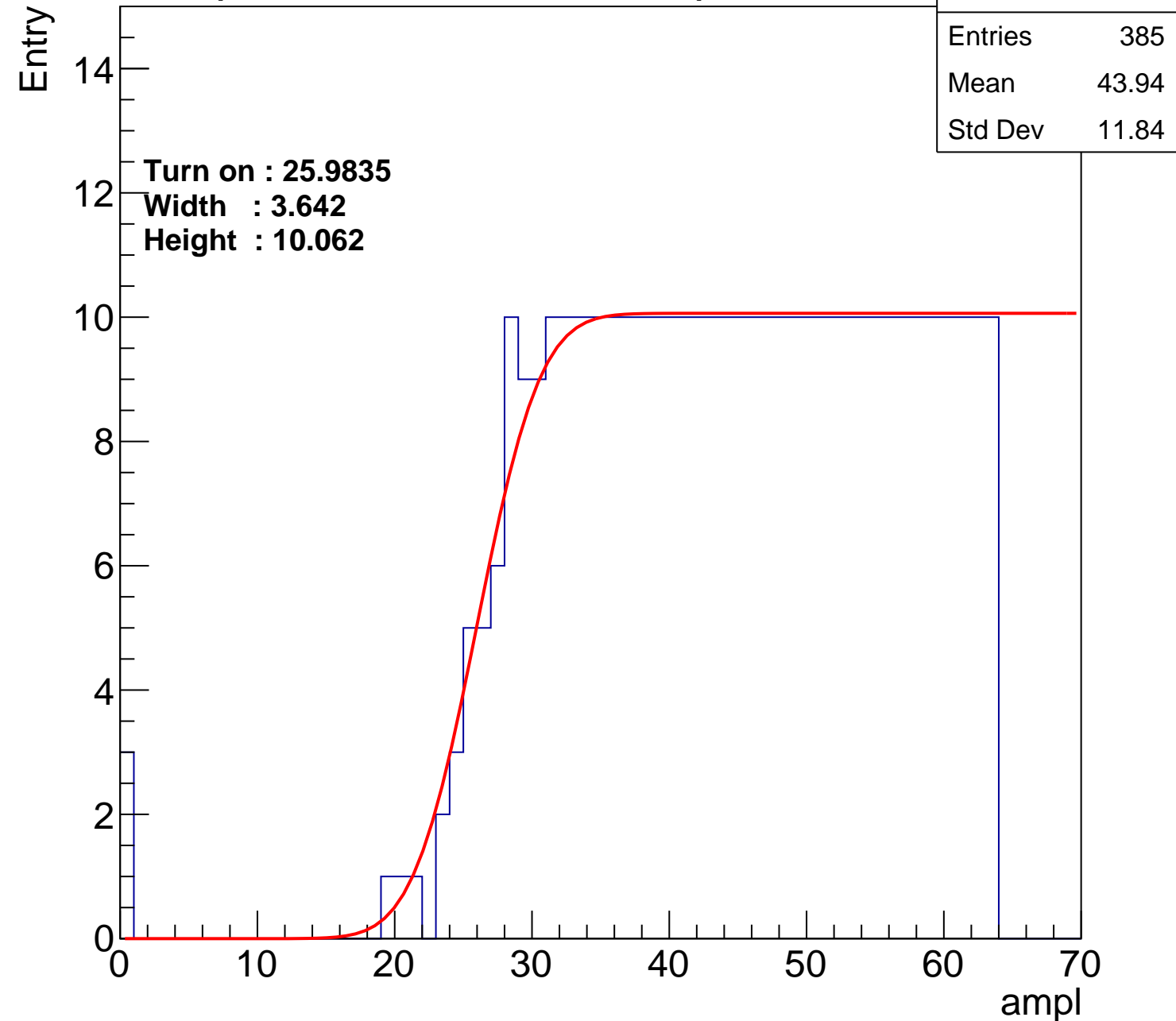
Width : 3.642

Height : 10.062

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U3-ch19

calib_packv5_042523_0143.root, FC#4, port A2

Entries	371
Mean	44.71
Std Dev	11.25

Turn on : 26.8909

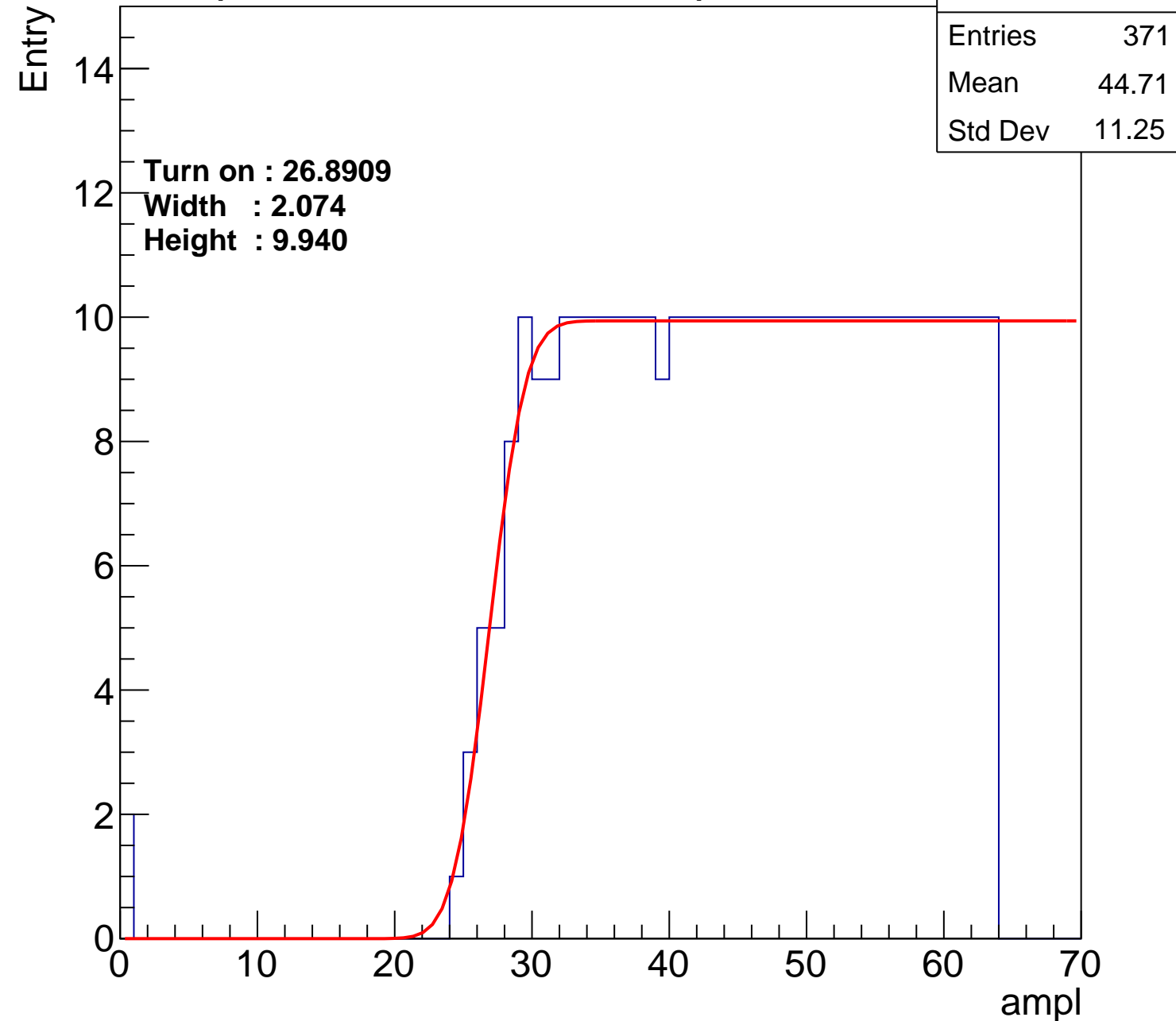
Width : 2.074

Height : 9.940

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U3-ch20

calib_packv5_042523_0143.root, FC#4, port A2

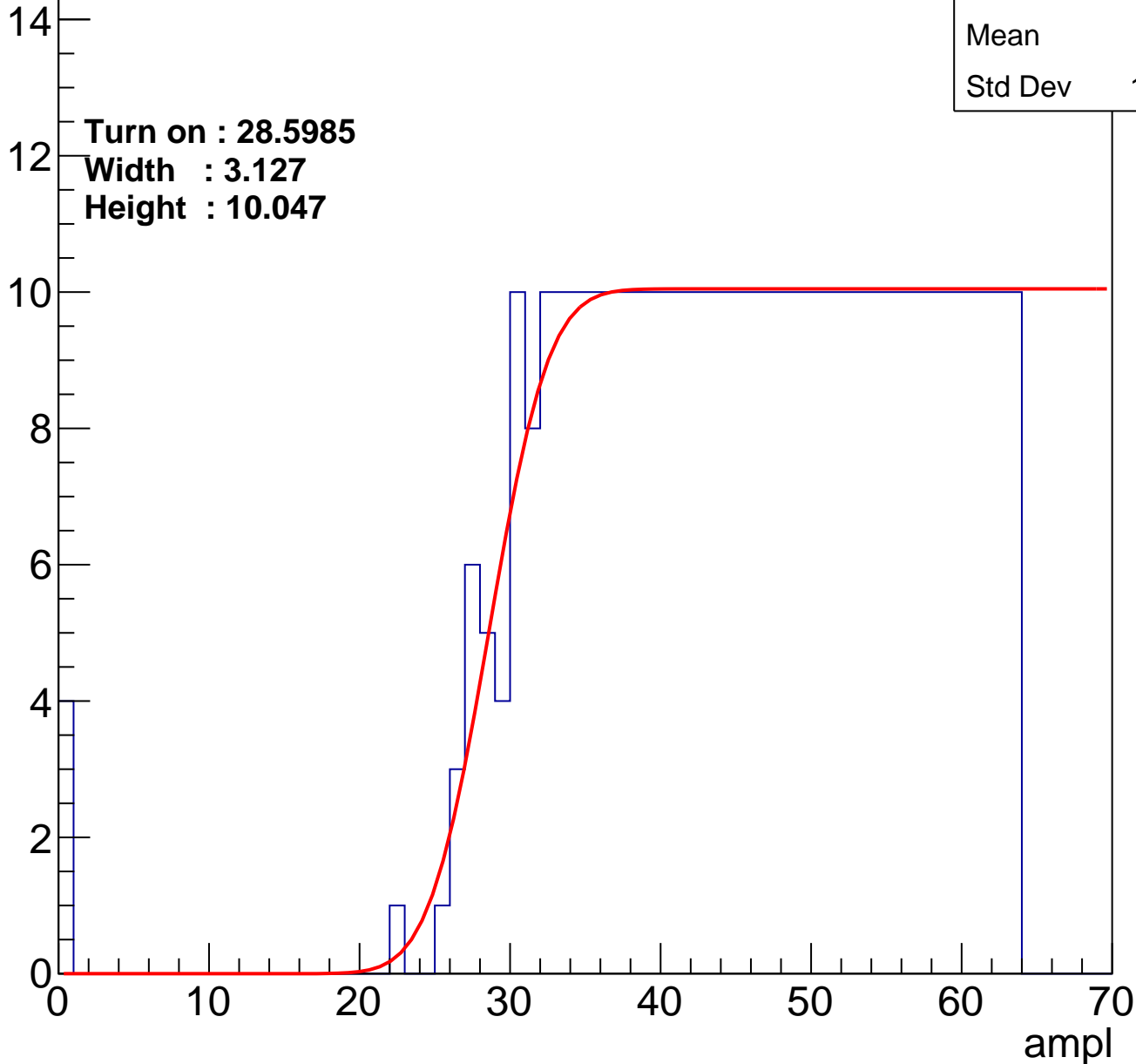
Entries	362
Mean	45
Std Dev	11.47

Turn on : 28.5985

Width : 3.127

Height : 10.047

Entry



B1L100S, U3-ch21

calib_packv5_042523_0143.root, FC#4, port A2

Entries	362
Mean	45.19
Std Dev	10.99

Turn on : 27.3988

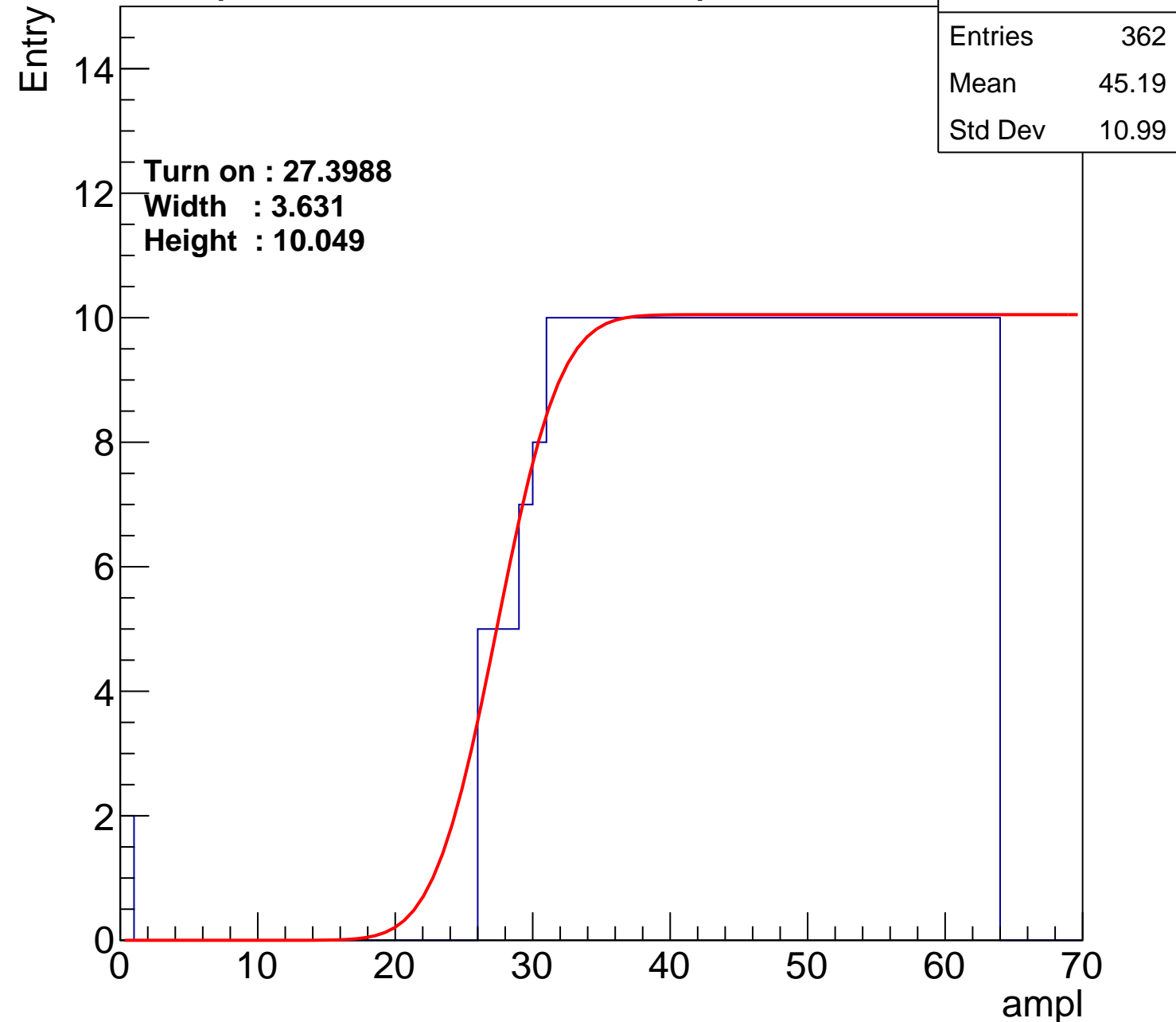
Width : 3.631

Height : 10.049

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U3-ch22

calib_packv5_042523_0143.root, FC#4, port A2

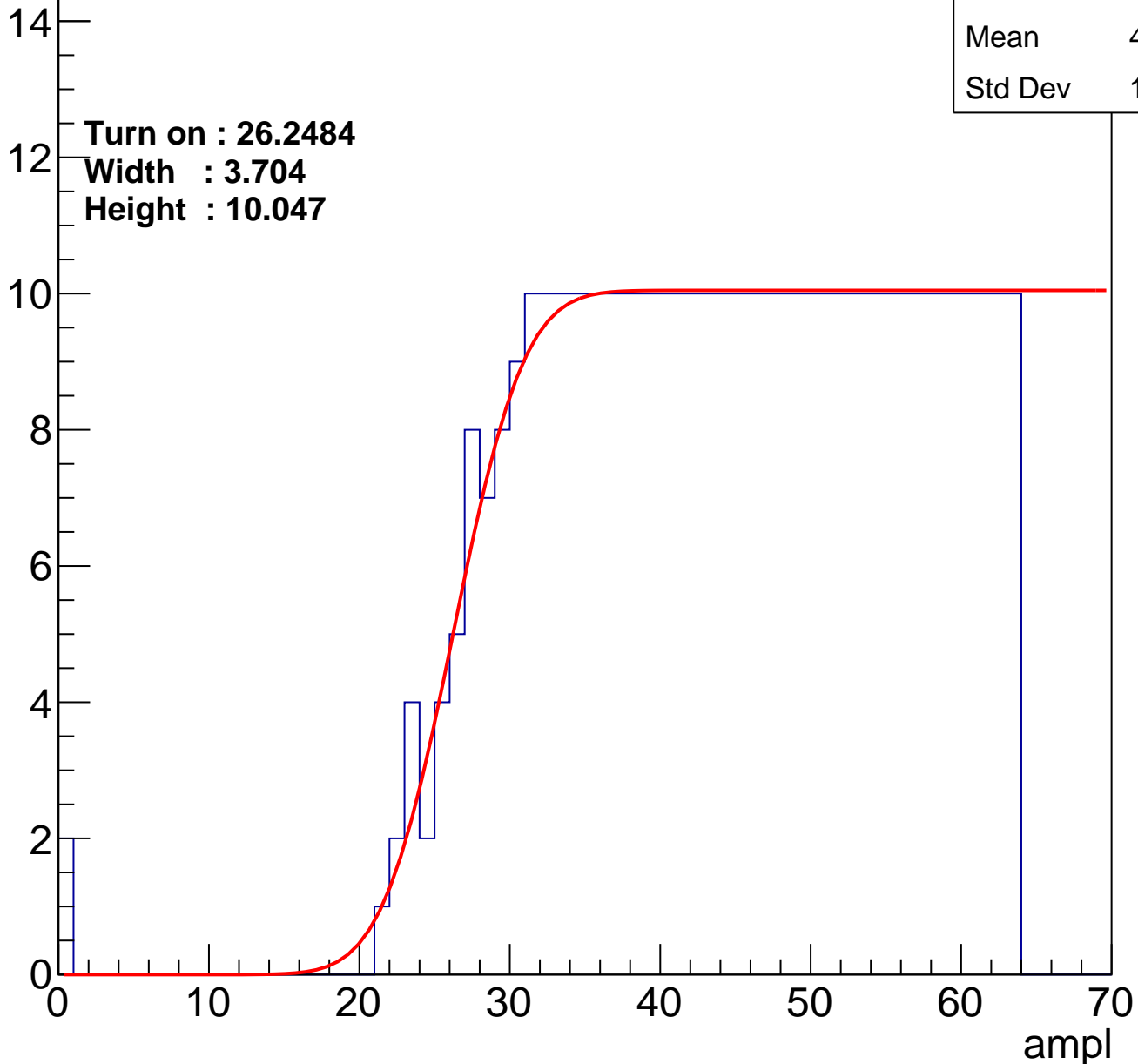
Entries	382
Mean	44.13
Std Dev	11.62

Turn on : 26.2484

Width : 3.704

Height : 10.047

Entry



B1L100S, U3-ch23

calib_packv5_042523_0143.root, FC#4, port A2

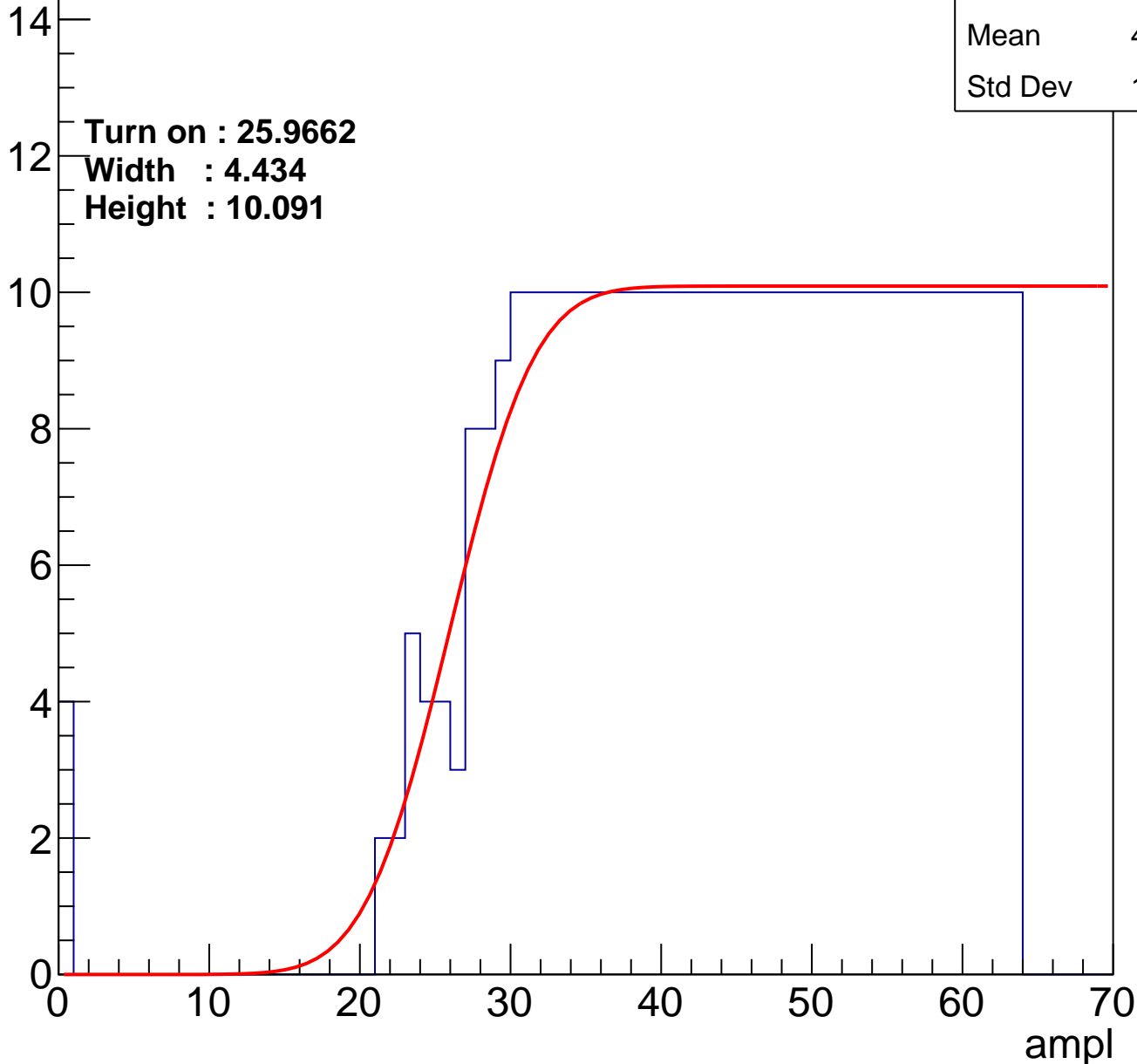
Entries	389
Mean	43.67
Std Dev	12.12

Turn on : 25.9662

Width : 4.434

Height : 10.091

Entry



B1L100S, U3-ch24

calib_packv5_042523_0143.root, FC#4, port A2

Entries	388
Mean	43.86
Std Dev	11.74

Turn on : 25.4041

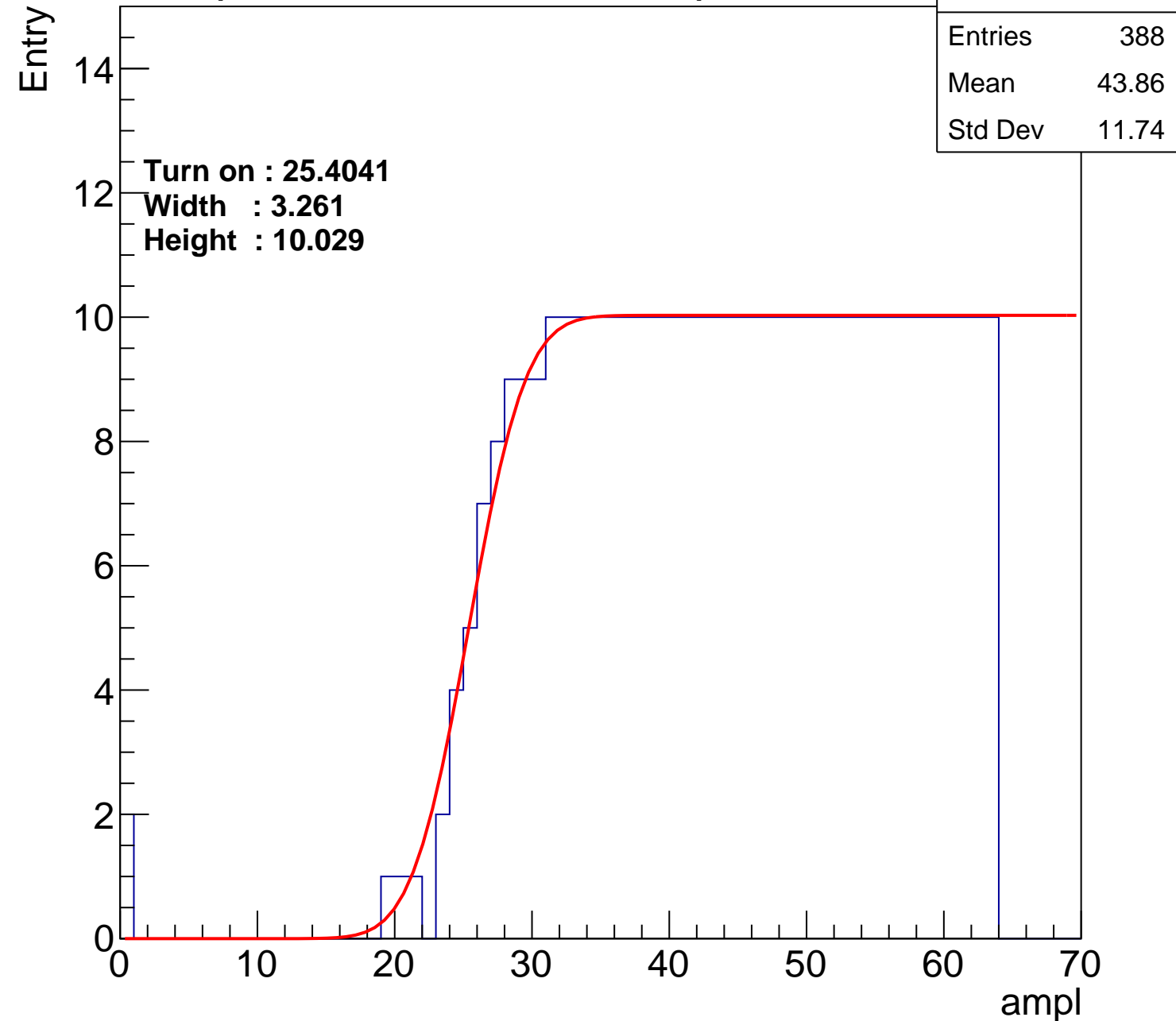
Width : 3.261

Height : 10.029

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U3-ch25

calib_packv5_042523_0143.root, FC#4, port A2

Entries	364
Mean	44.91
Std Dev	11.42

Turn on : 28.3562

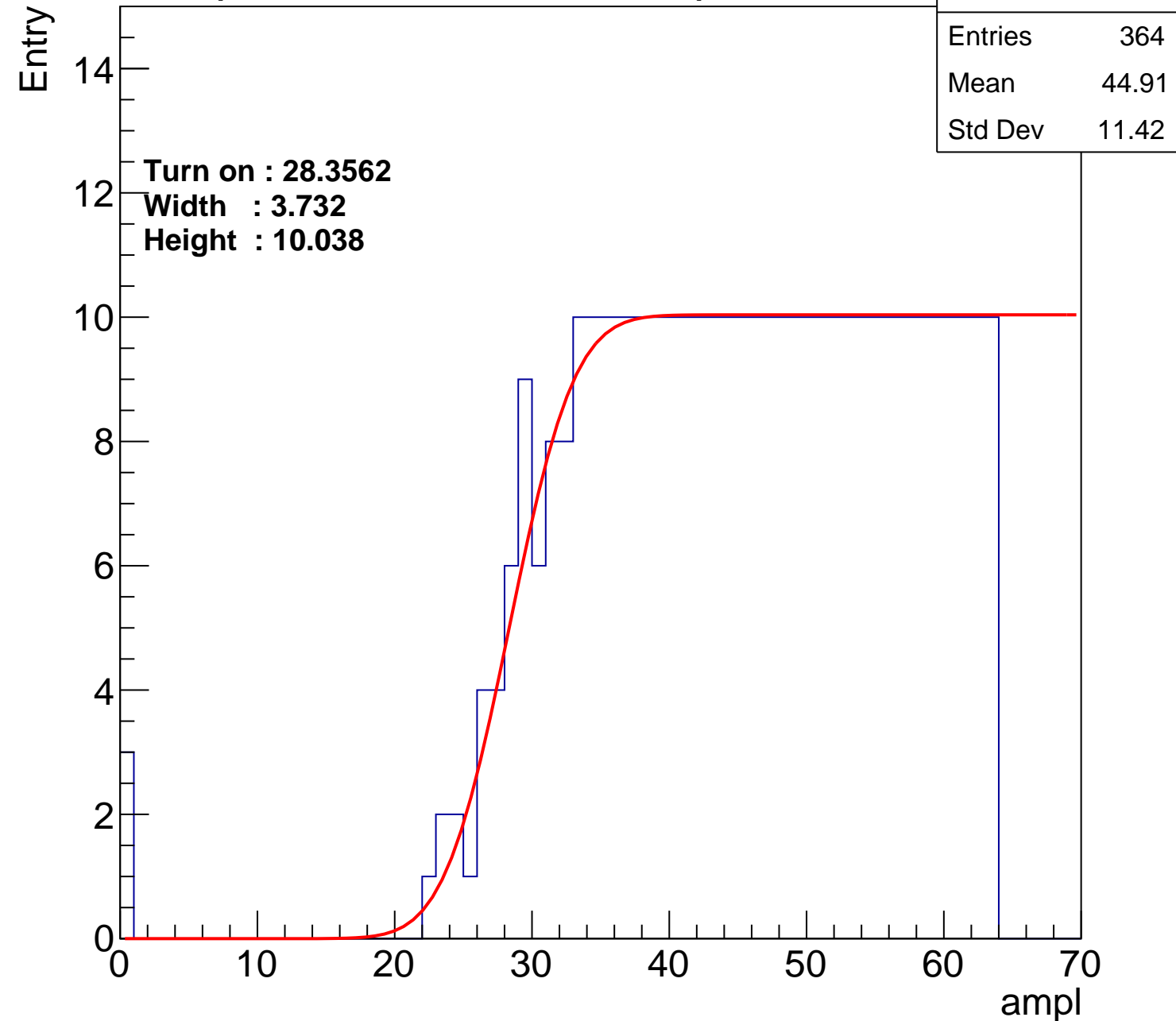
Width : 3.732

Height : 10.038

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U3-ch26

calib_packv5_042523_0143.root, FC#4, port A2

Entries	391
Mean	43.53
Std Dev	12.29

Turn on : 25.7634

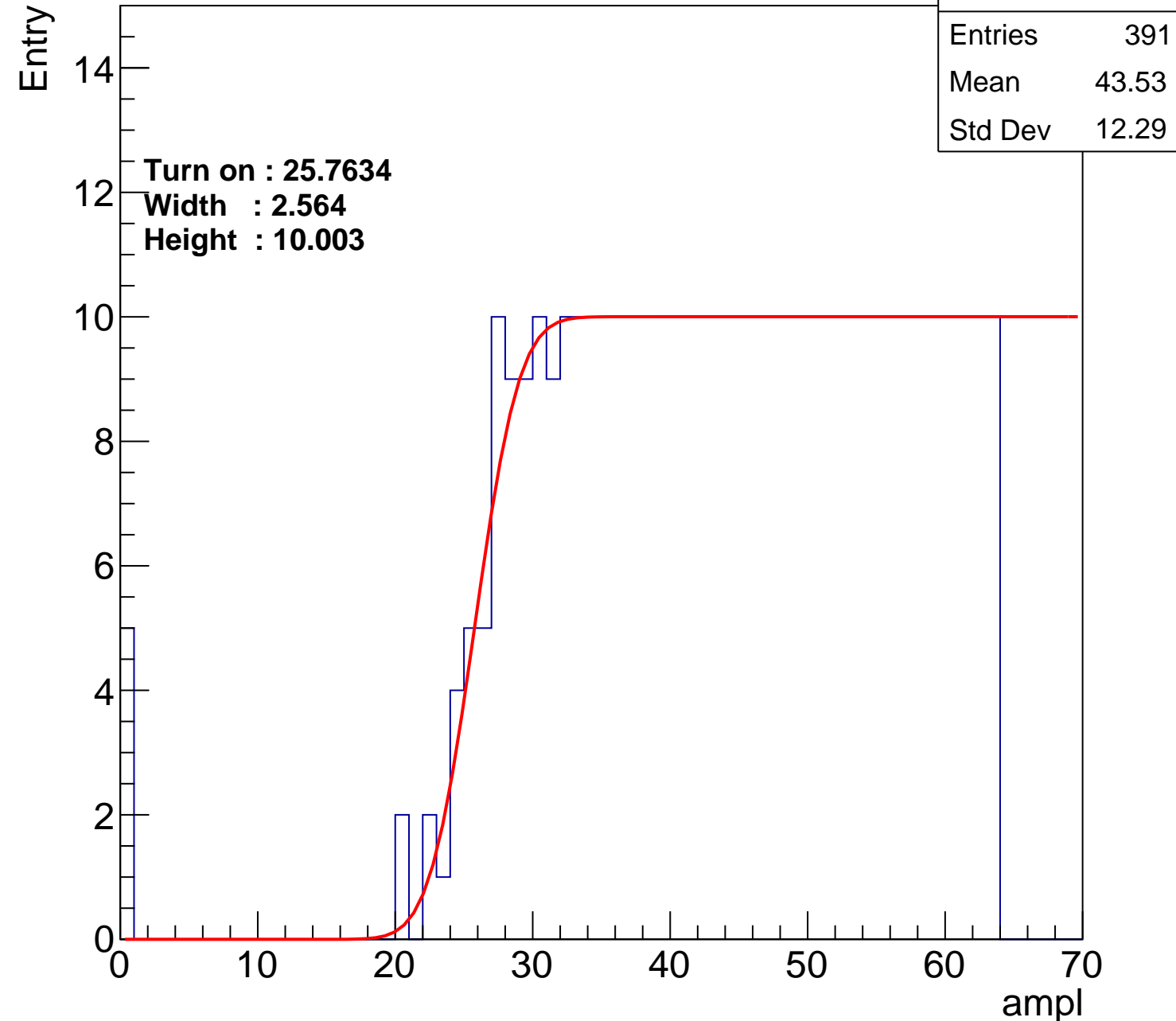
Width : 2.564

Height : 10.003

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U3-ch27

calib_packv5_042523_0143.root, FC#4, port A2

Entries	373
Mean	44.49
Std Dev	11.69

Turn on : 27.2315

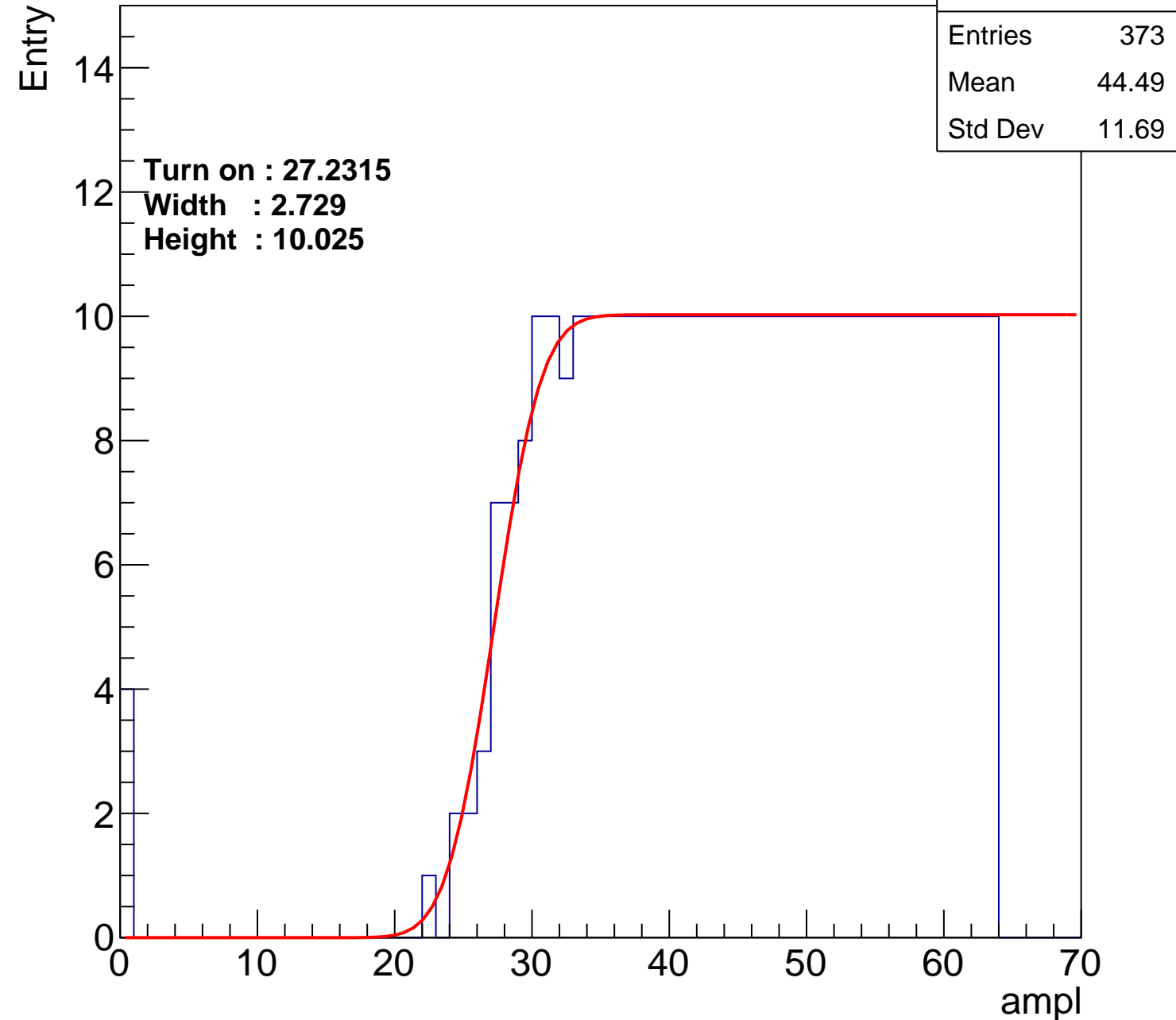
Width : 2.729

Height : 10.025

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U3-ch28

calib_packv5_042523_0143.root, FC#4, port A2

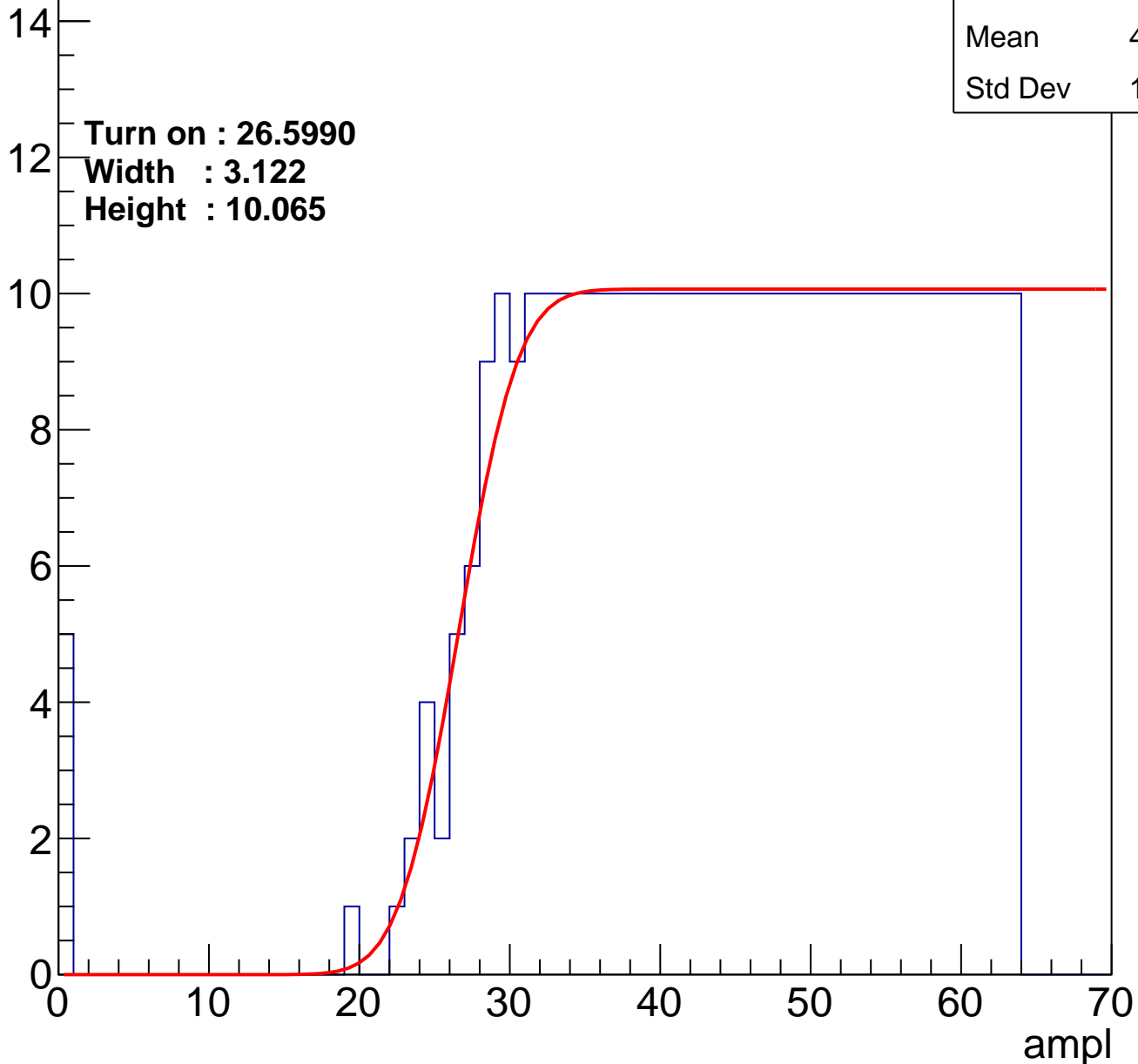
Entries	384
Mean	43.87
Std Dev	12.14

Turn on : 26.5990

Width : 3.122

Height : 10.065

Entry



B1L100S, U3-ch29

calib_packv5_042523_0143.root, FC#4, port A2

Entries	382
Mean	44.05
Std Dev	11.81

Turn on : 25.9557

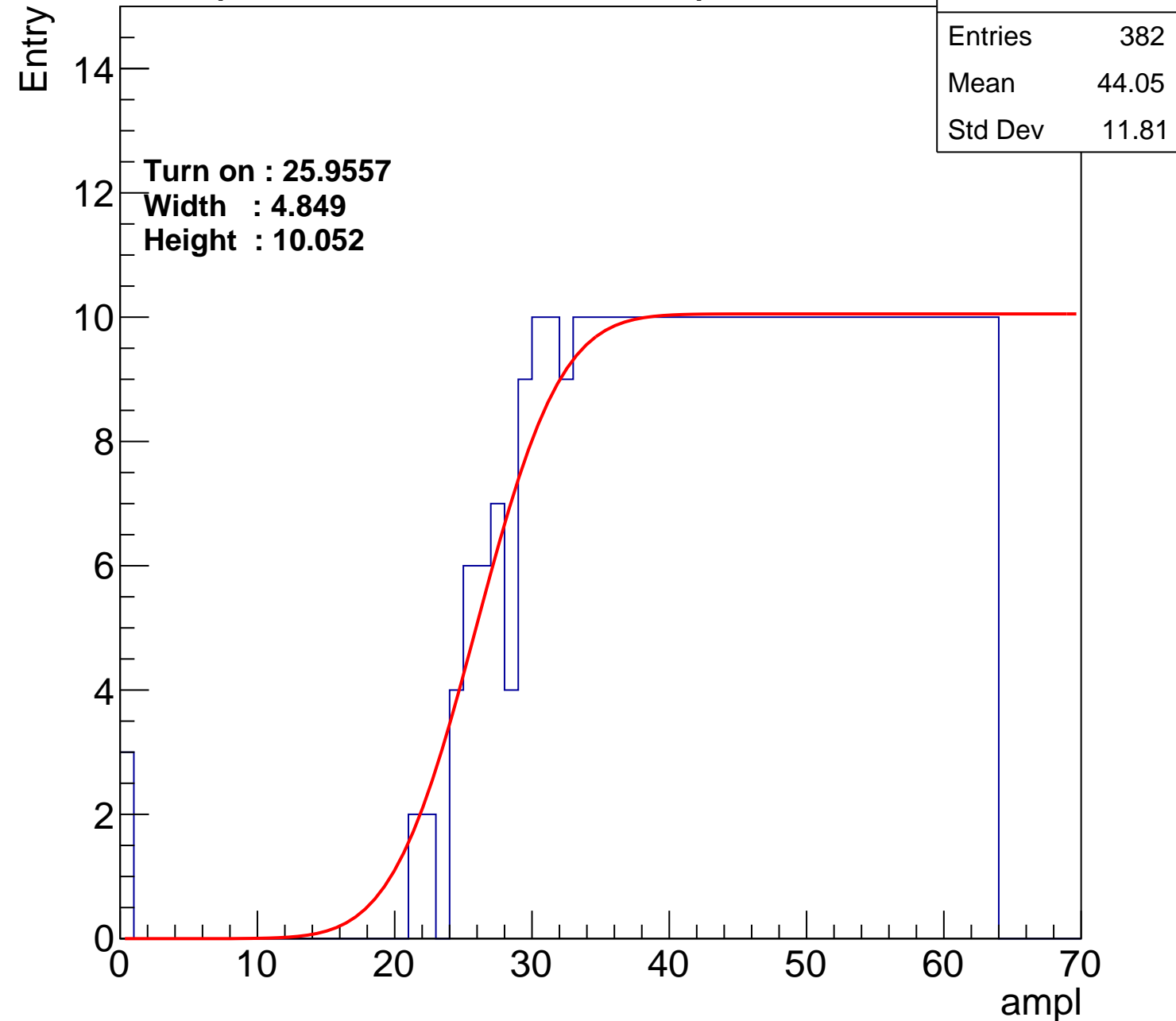
Width : 4.849

Height : 10.052

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U3-ch30

calib_packv5_042523_0143.root, FC#4, port A2

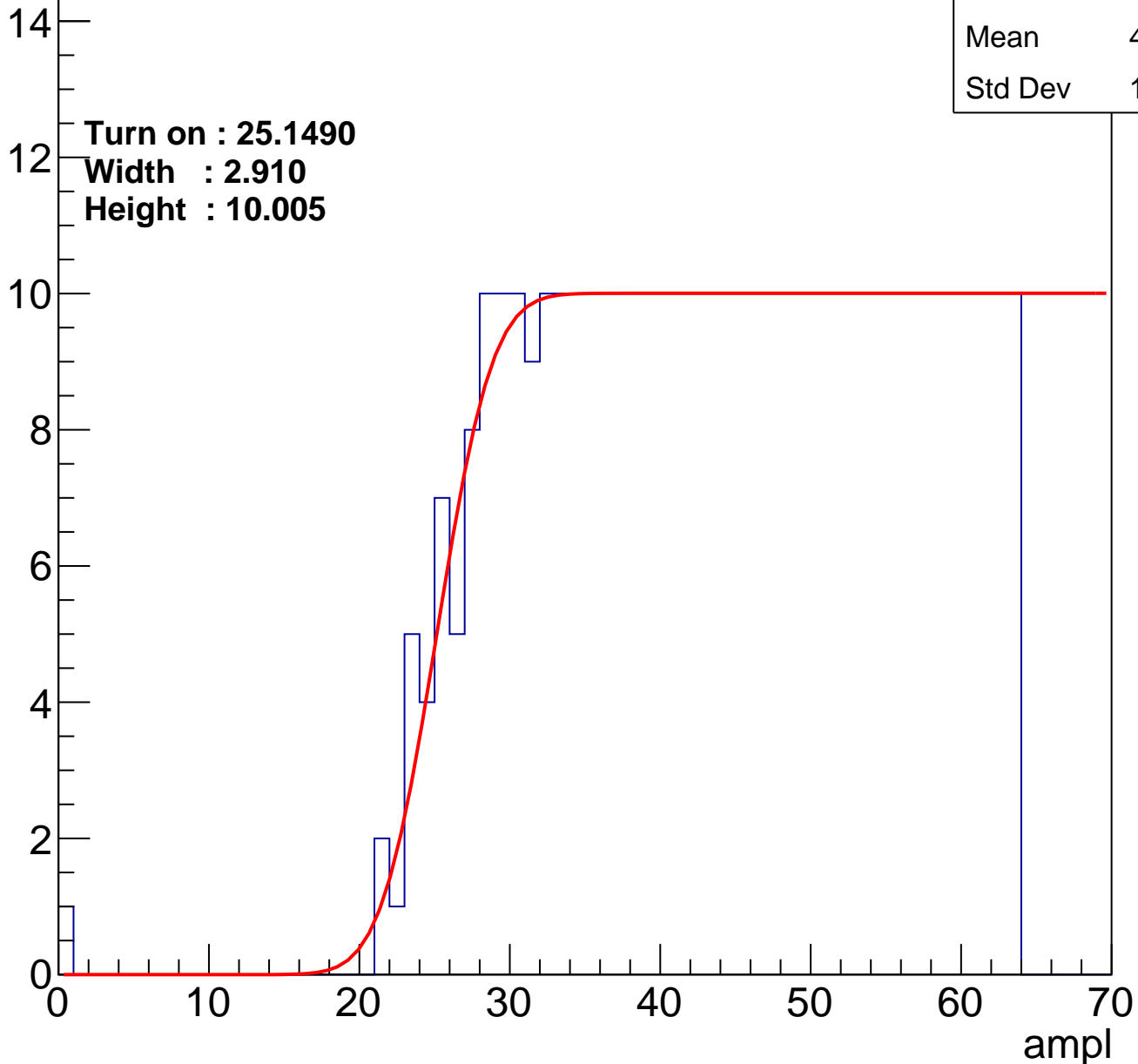
Entries	392
Mean	43.74
Std Dev	11.65

Turn on : 25.1490

Width : 2.910

Height : 10.005

Entry



B1L100S, U3-ch31

calib_packv5_042523_0143.root, FC#4, port A2

Entries	376
Mean	44.52
Std Dev	11.23

Turn on : 26.7891

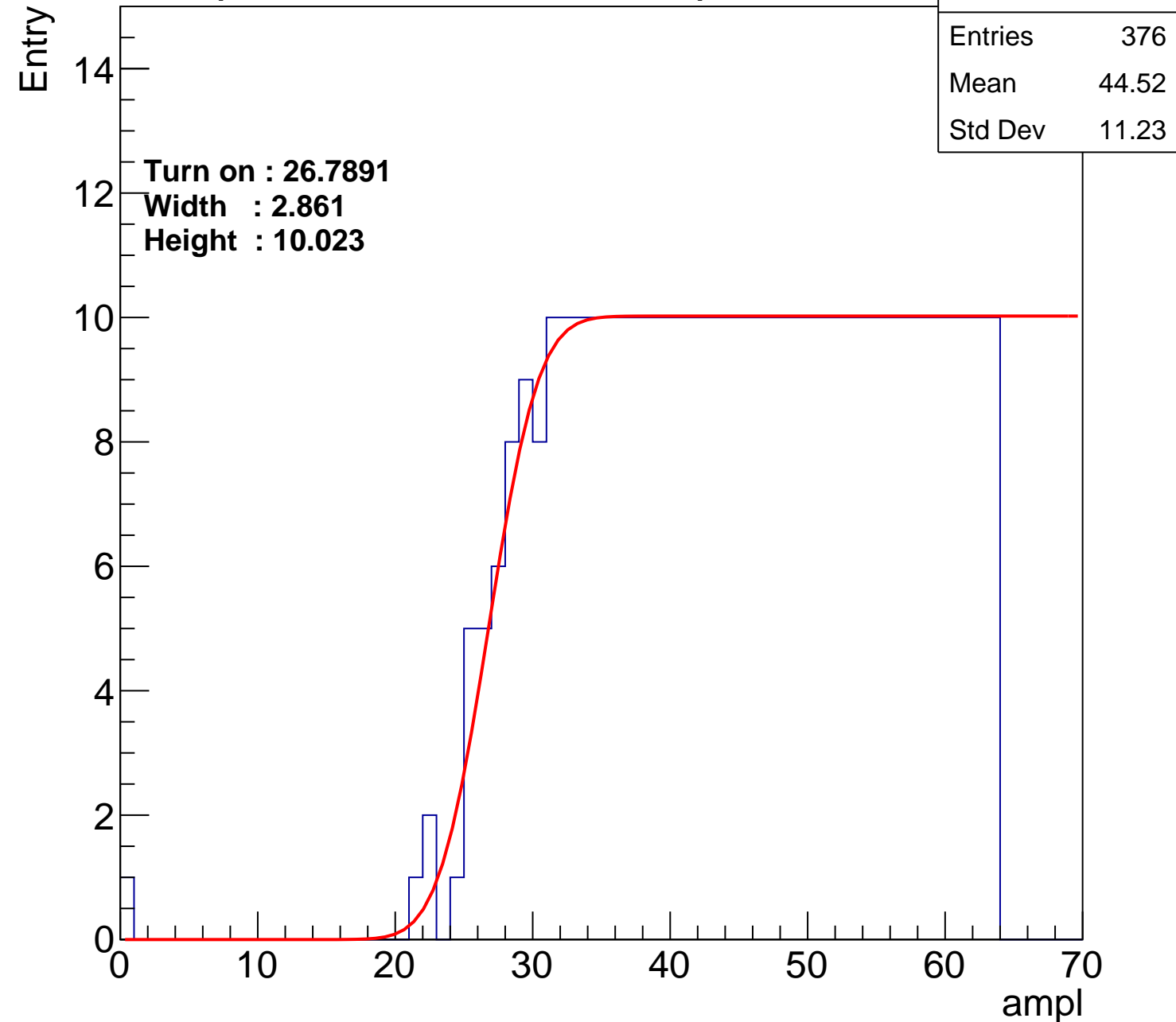
Width : 2.861

Height : 10.023

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U3-ch32

calib_packv5_042523_0143.root, FC#4, port A2

Entries	387
Mean	43.77
Std Dev	12.07

Turn on : 26.0495

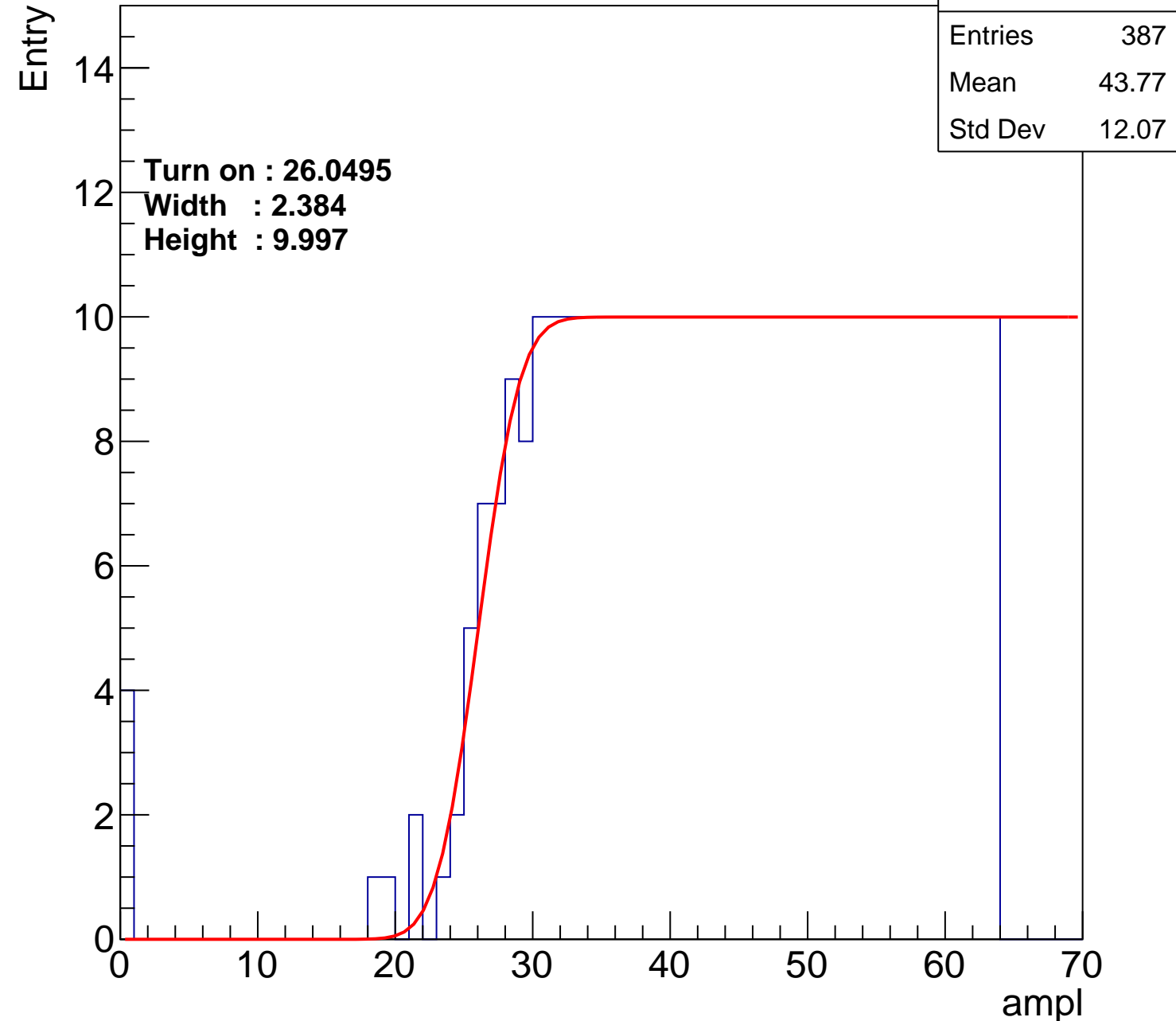
Width : 2.384

Height : 9.997

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U3-ch33

calib_packv5_042523_0143.root, FC#4, port A2

Entries	381
Mean	44.17
Std Dev	11.69

Turn on : 26.3131

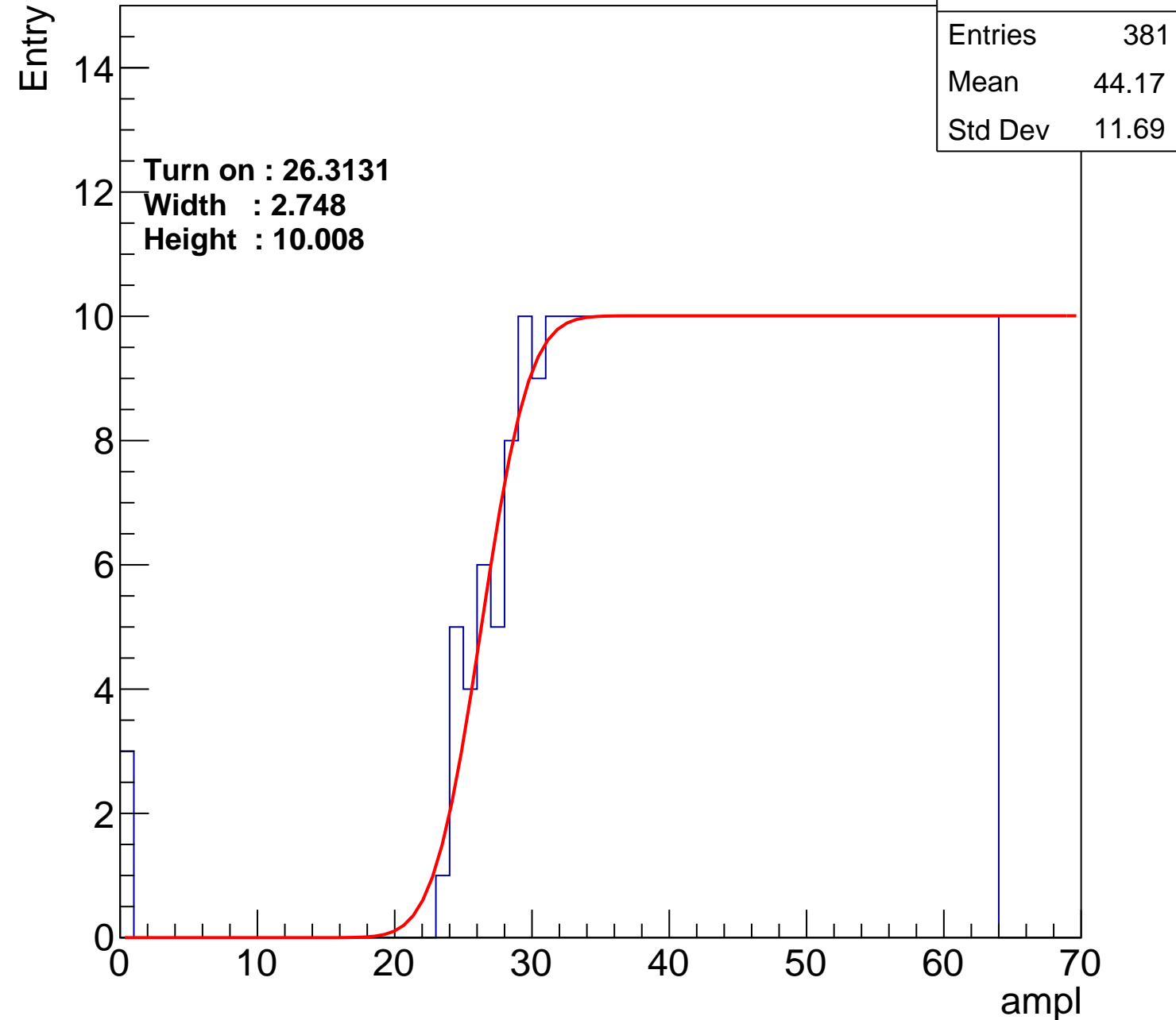
Width : 2.748

Height : 10.008

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U3-ch34

calib_packv5_042523_0143.root, FC#4, port A2

Entries	397
Mean	43.35
Std Dev	12.21

Turn on : 24.7602

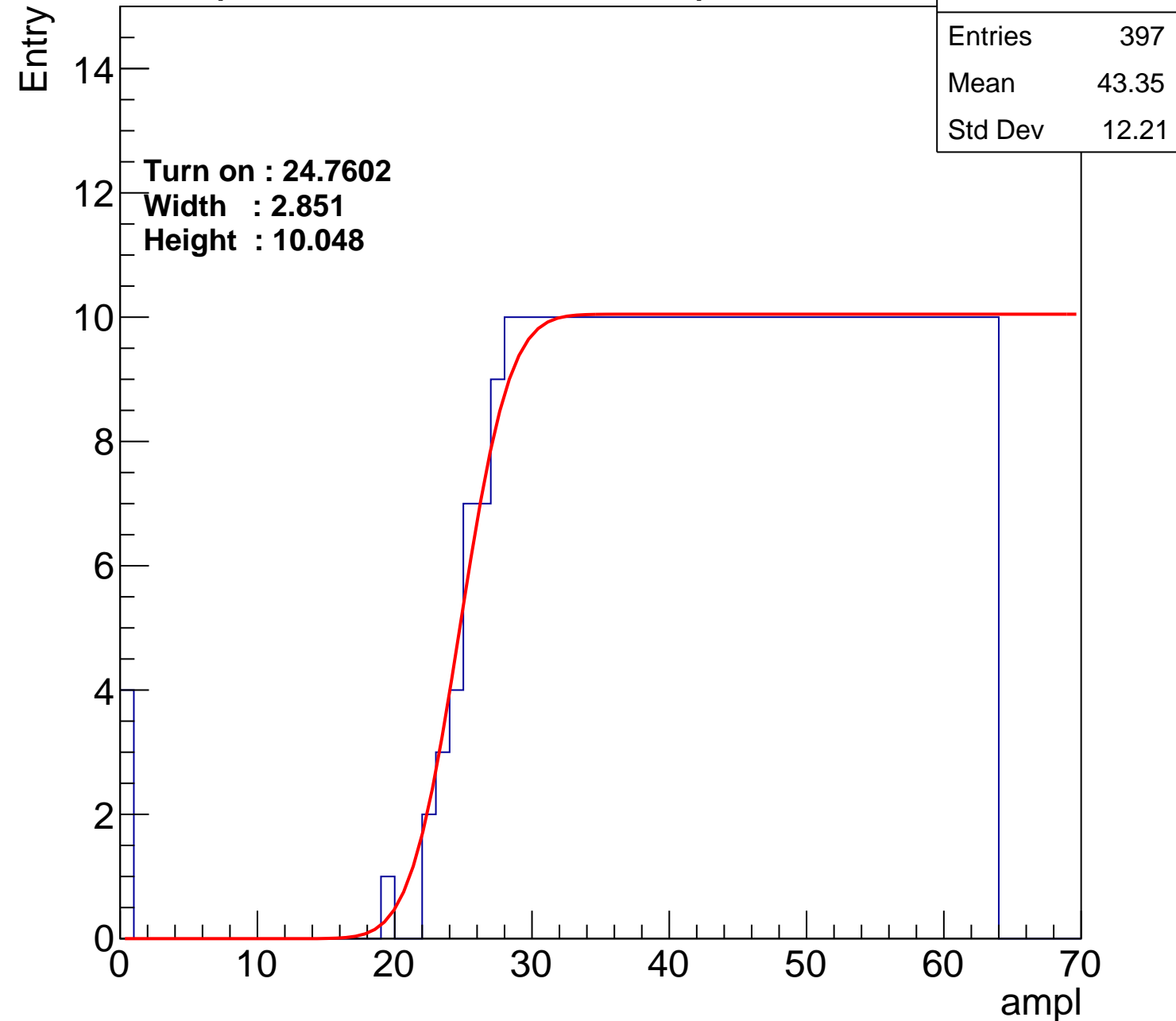
Width : 2.851

Height : 10.048

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U3-ch35

calib_packv5_042523_0143.root, FC#4, port A2

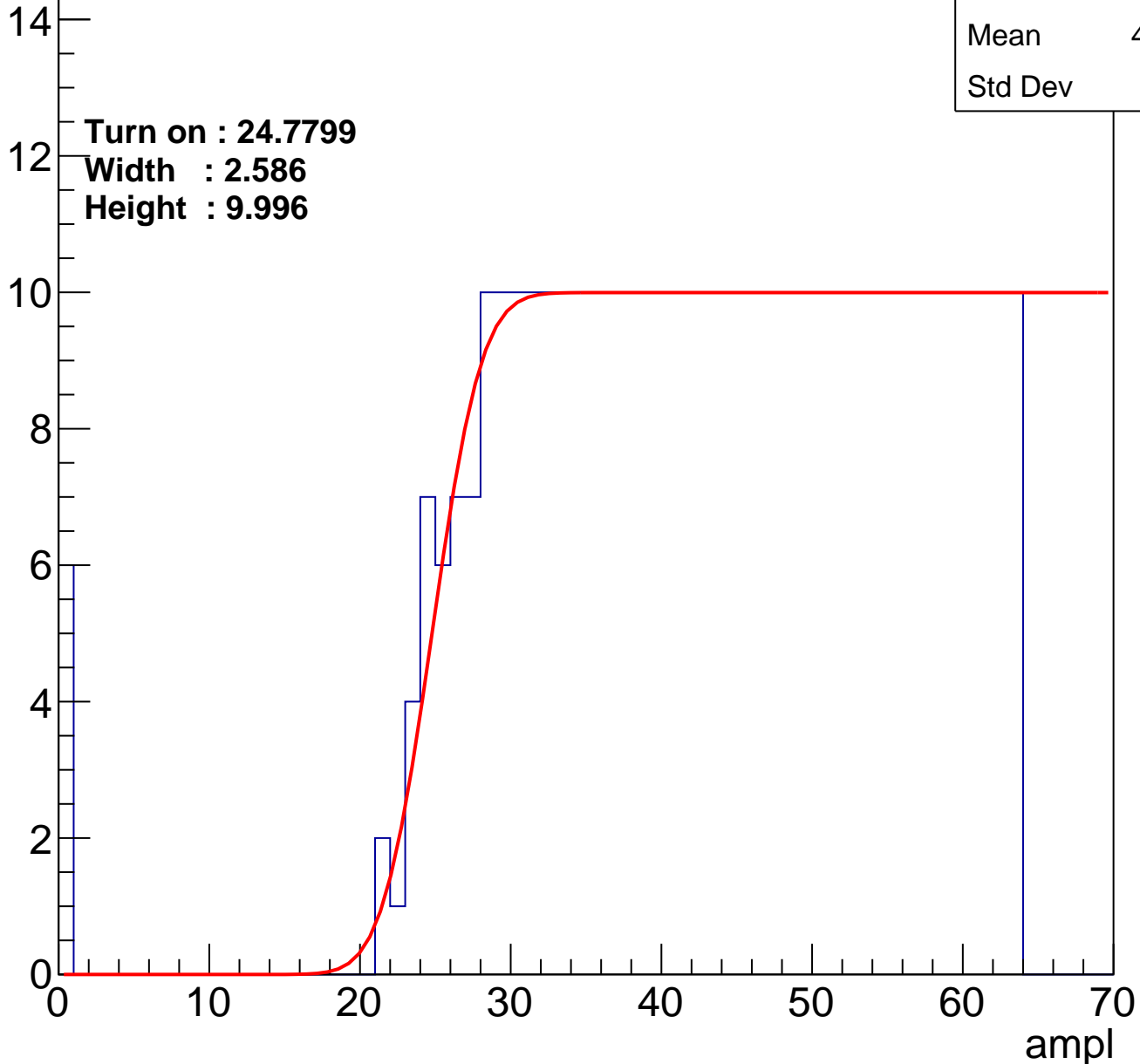
Entries	400
Mean	43.06
Std Dev	12.6

Turn on : 24.7799

Width : 2.586

Height : 9.996

Entry



B1L100S, U3-ch36

calib_packv5_042523_0143.root, FC#4, port A2

Entries	397
Mean	43.45
Std Dev	11.91

Turn on : 24.4600

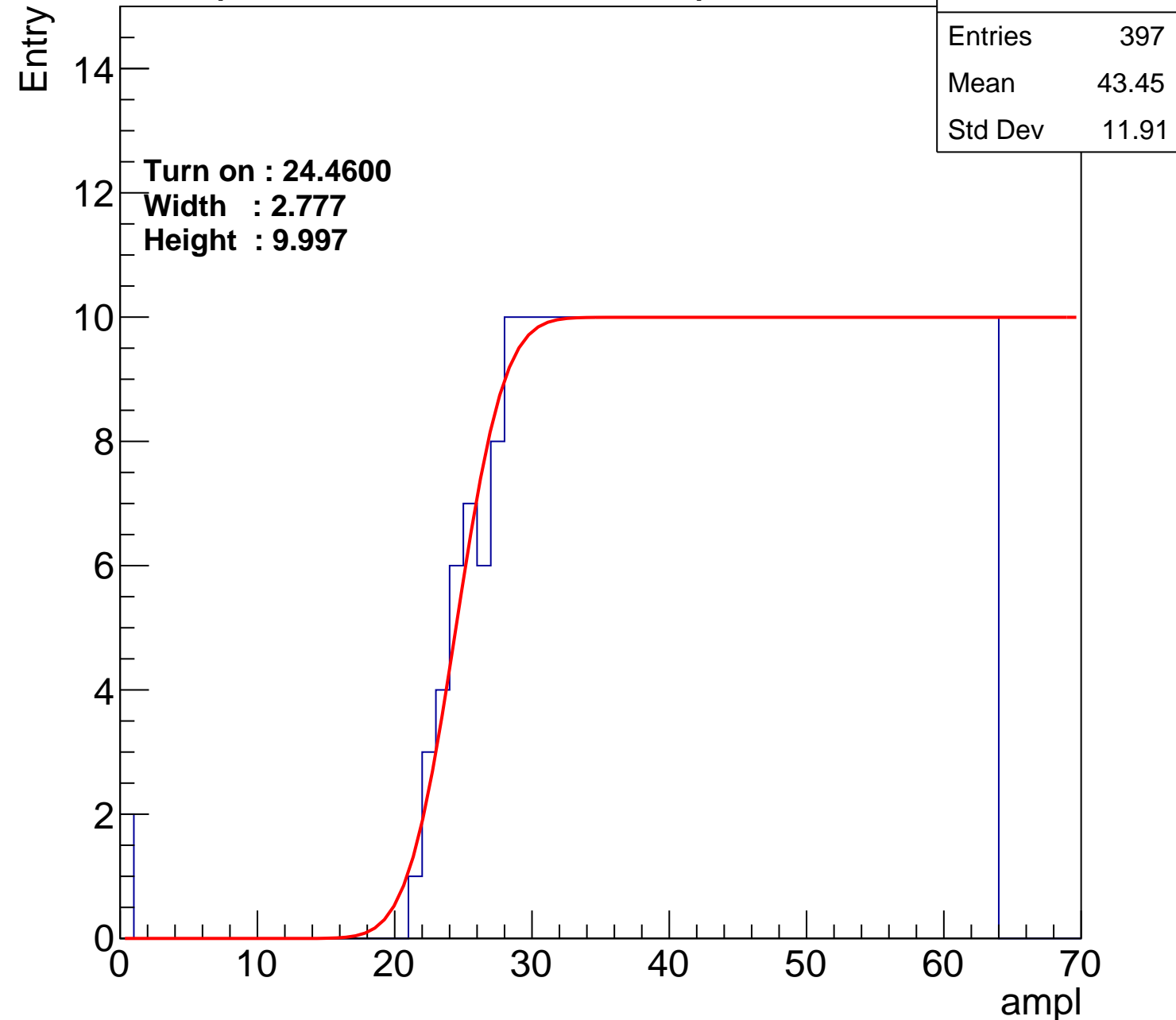
Width : 2.777

Height : 9.997

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U3-ch37

calib_packv5_042523_0143.root, FC#4, port A2

Entries	387
Mean	43.97
Std Dev	11.6

Turn on : 25.5643

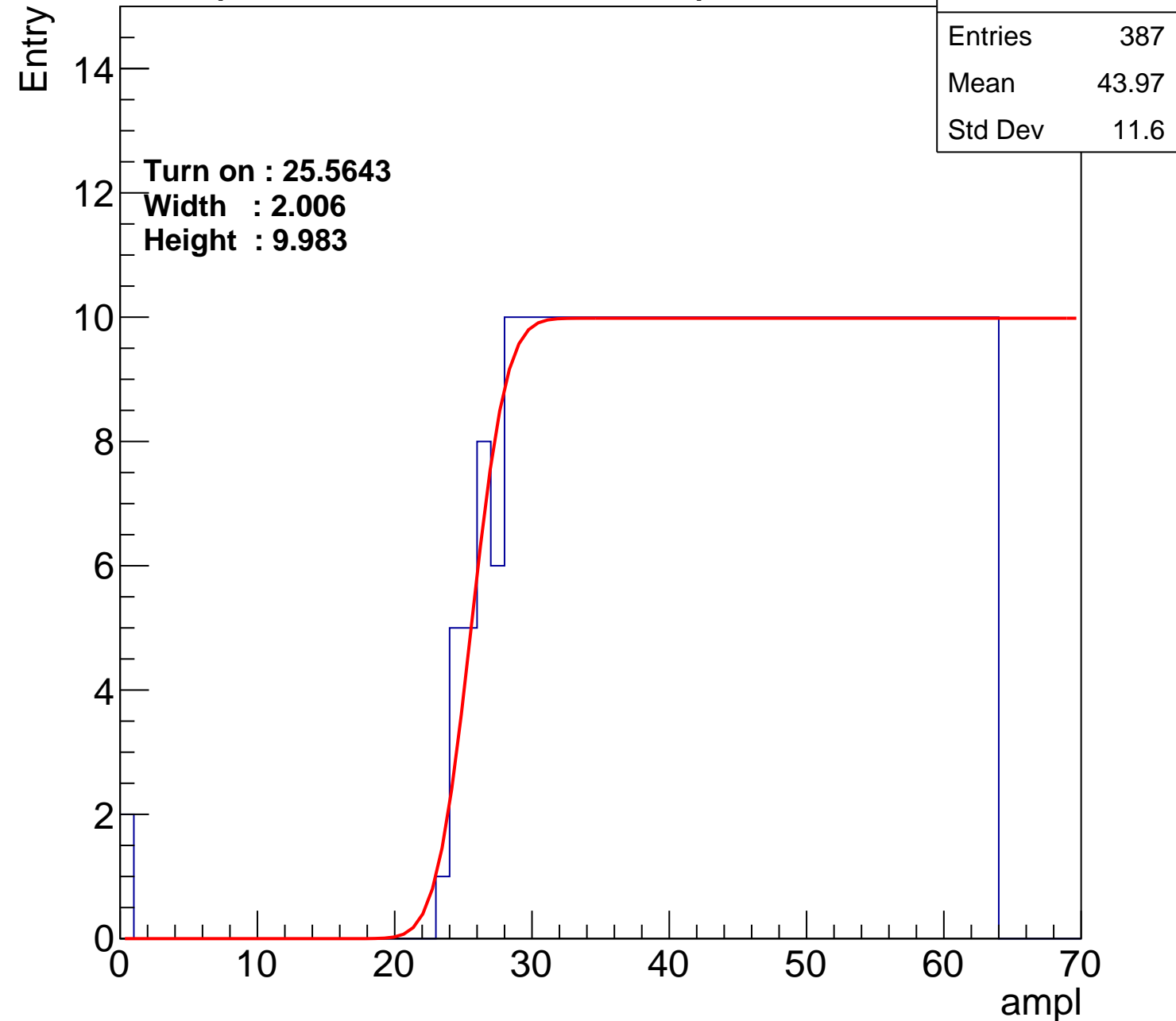
Width : 2.006

Height : 9.983

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U3-ch38

calib_packv5_042523_0143.root, FC#4, port A2

Entry

Entries	394
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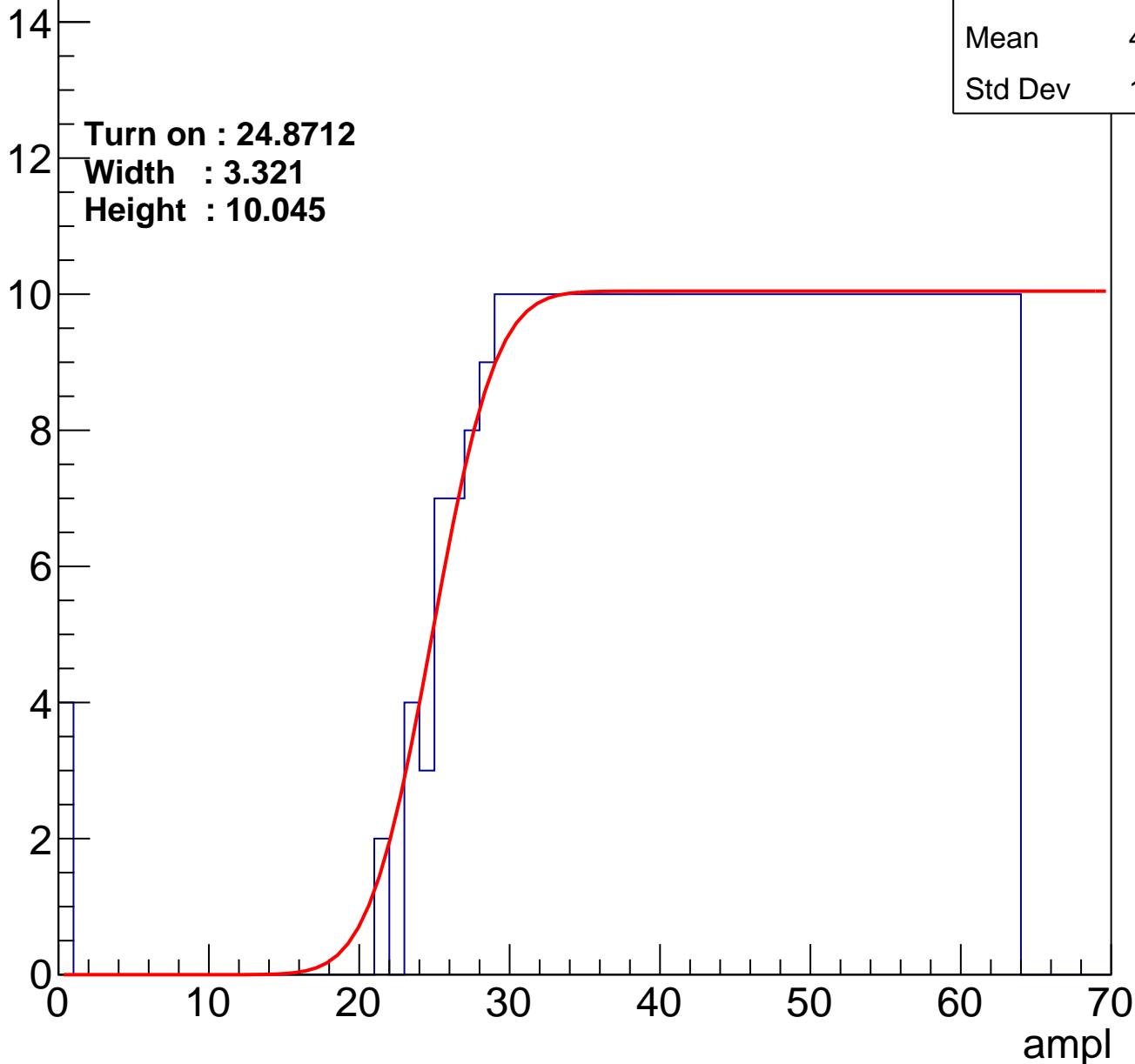
Mean	43.48
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Std Dev	12.15
---------	-------

Turn on : 24.8712

Width : 3.321

Height : 10.045



B1L100S, U3-ch39

calib_packv5_042523_0143.root, FC#4, port A2

Entries	388
Mean	43.79
Std Dev	11.99

Turn on : 25.7907

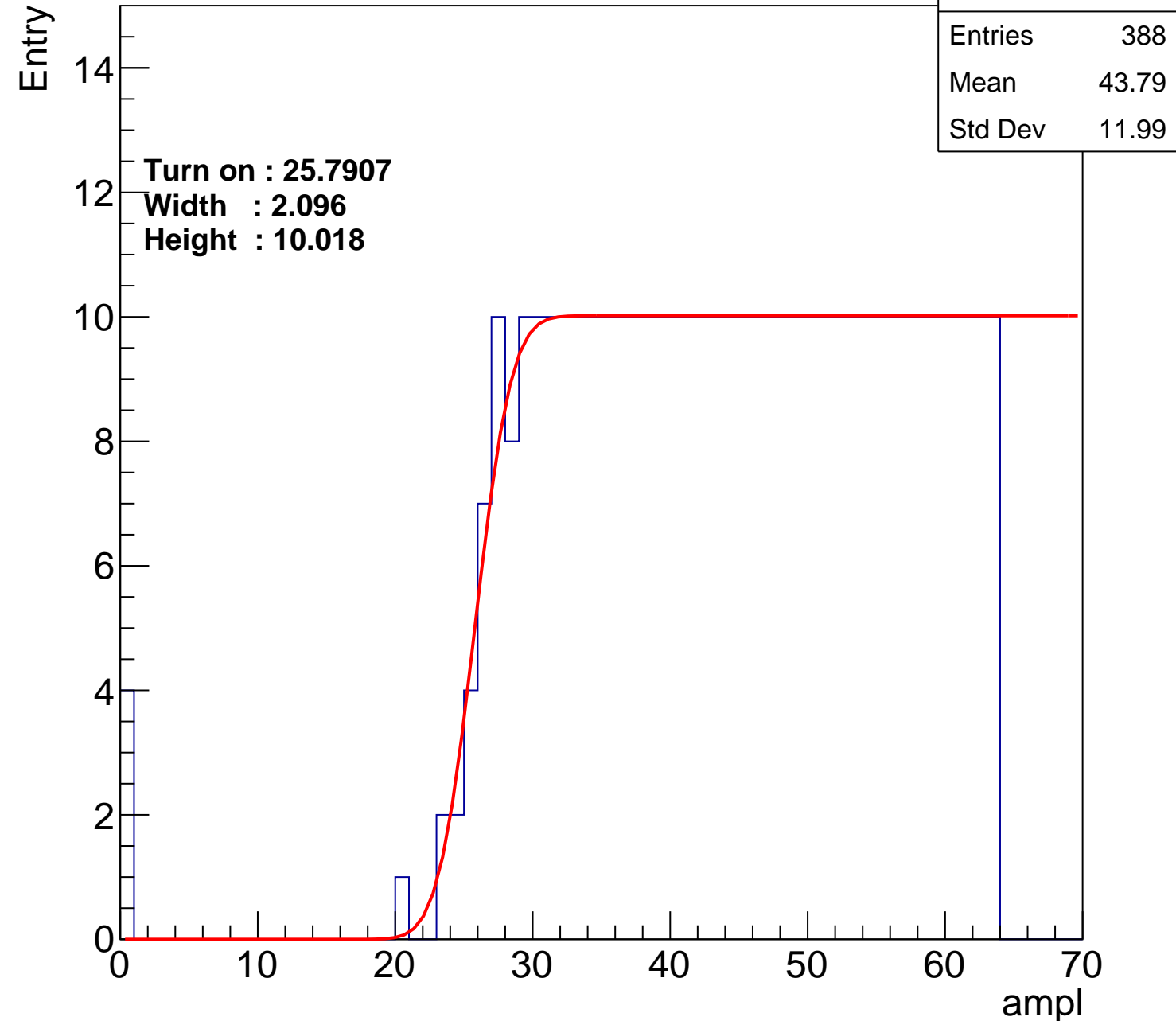
Width : 2.096

Height : 10.018

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U3-ch40

calib_packv5_042523_0143.root, FC#4, port A2

Entries	390
Mean	43.58
Std Dev	12.27

Turn on : 25.5683

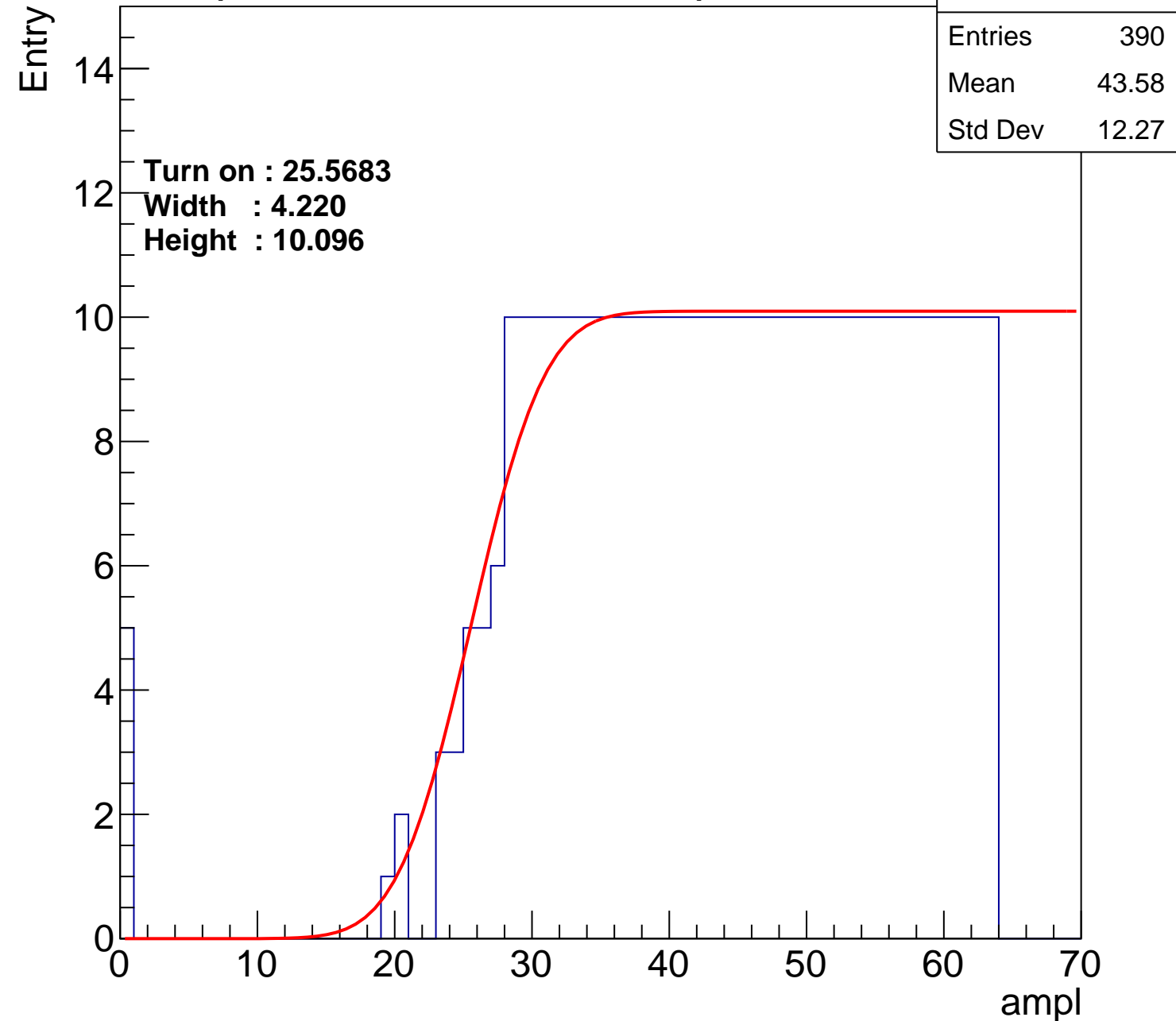
Width : 4.220

Height : 10.096

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U3-ch41

calib_packv5_042523_0143.root, FC#4, port A2

Entries	381
Mean	44.07
Std Dev	11.91

Turn on : 26.0126

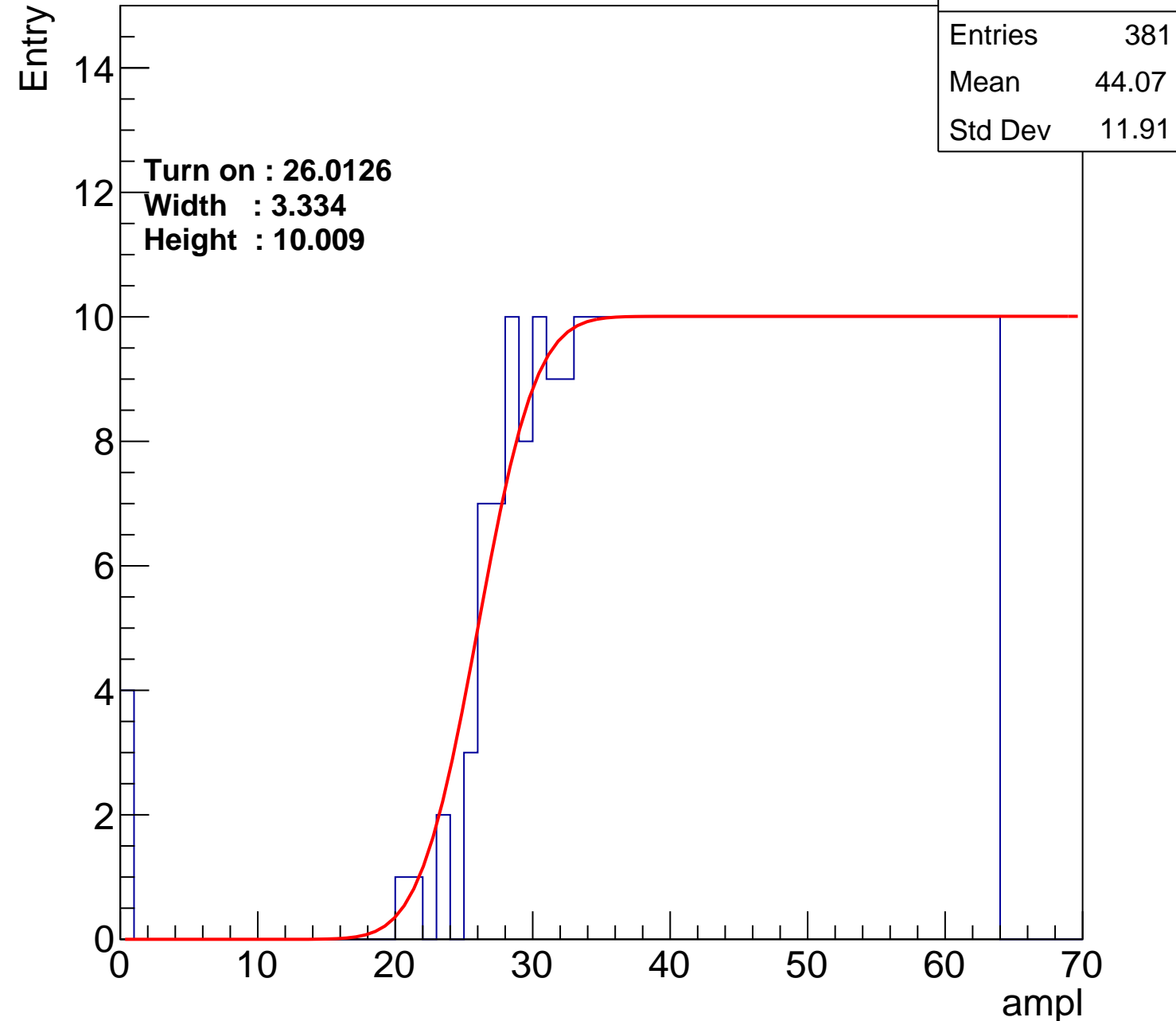
Width : 3.334

Height : 10.009

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U3-ch42

calib_packv5_042523_0143.root, FC#4, port A2

Entries	400
Mean	43.2
Std Dev	12.22

Turn on : 24.5486

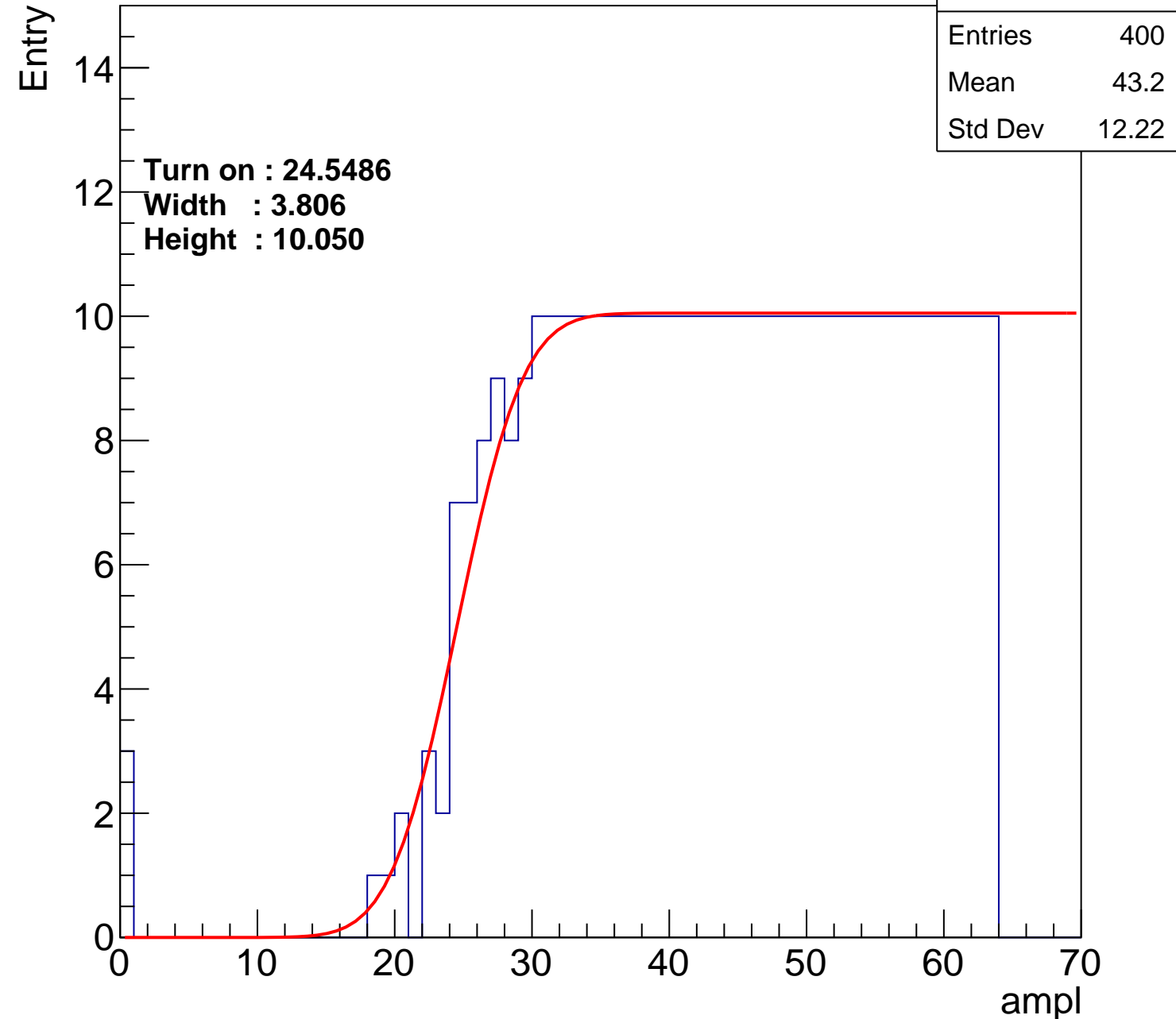
Width : 3.806

Height : 10.050

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U3-ch43

calib_packv5_042523_0143.root, FC#4, port A2

Entries	370
Mean	44.85
Std Dev	11.01

Turn on : 27.5044

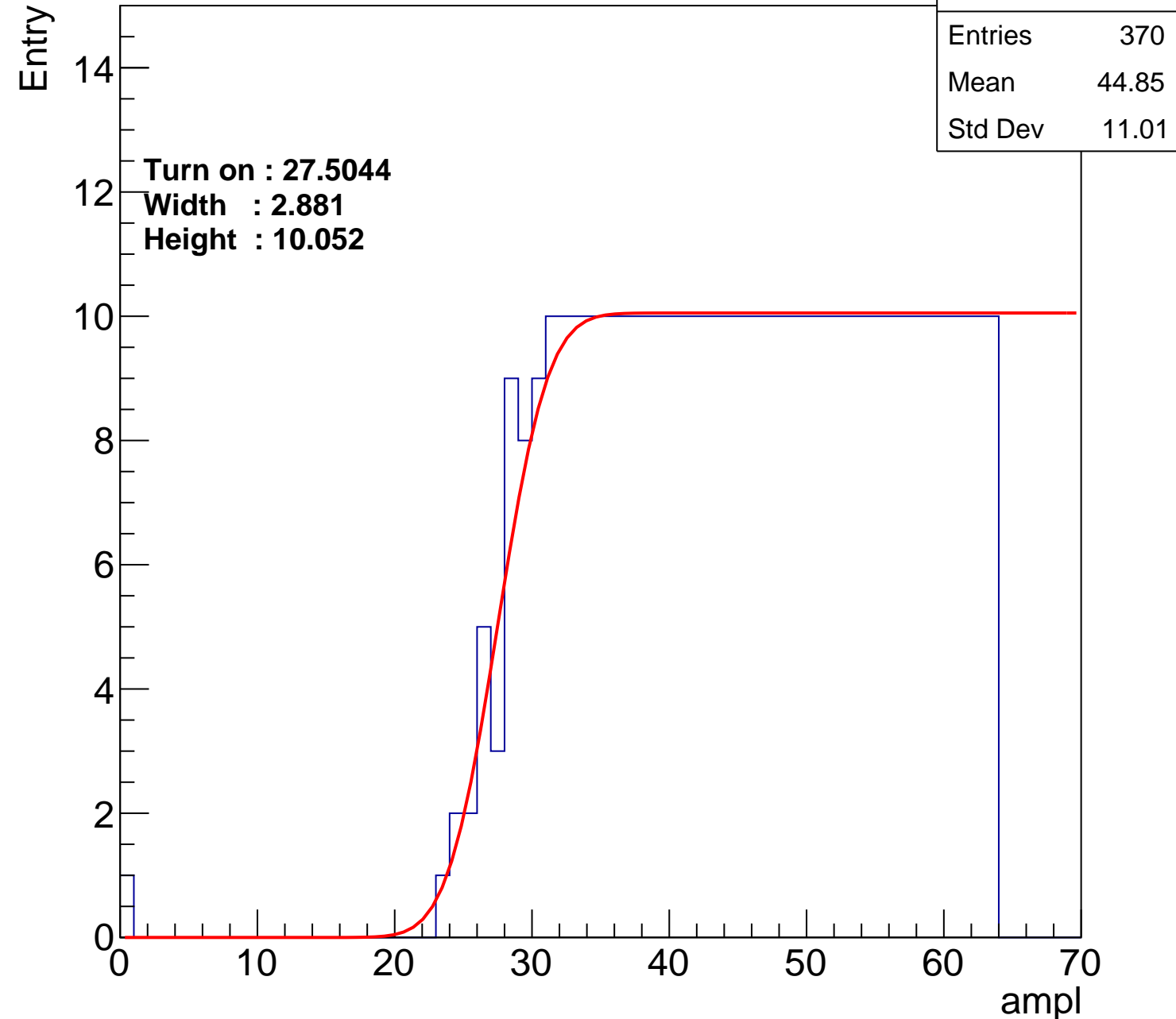
Width : 2.881

Height : 10.052

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U3-ch44

calib_packv5_042523_0143.root, FC#4, port A2

Entries	385
Mean	44.07
Std Dev	11.5

Turn on : 26.4426

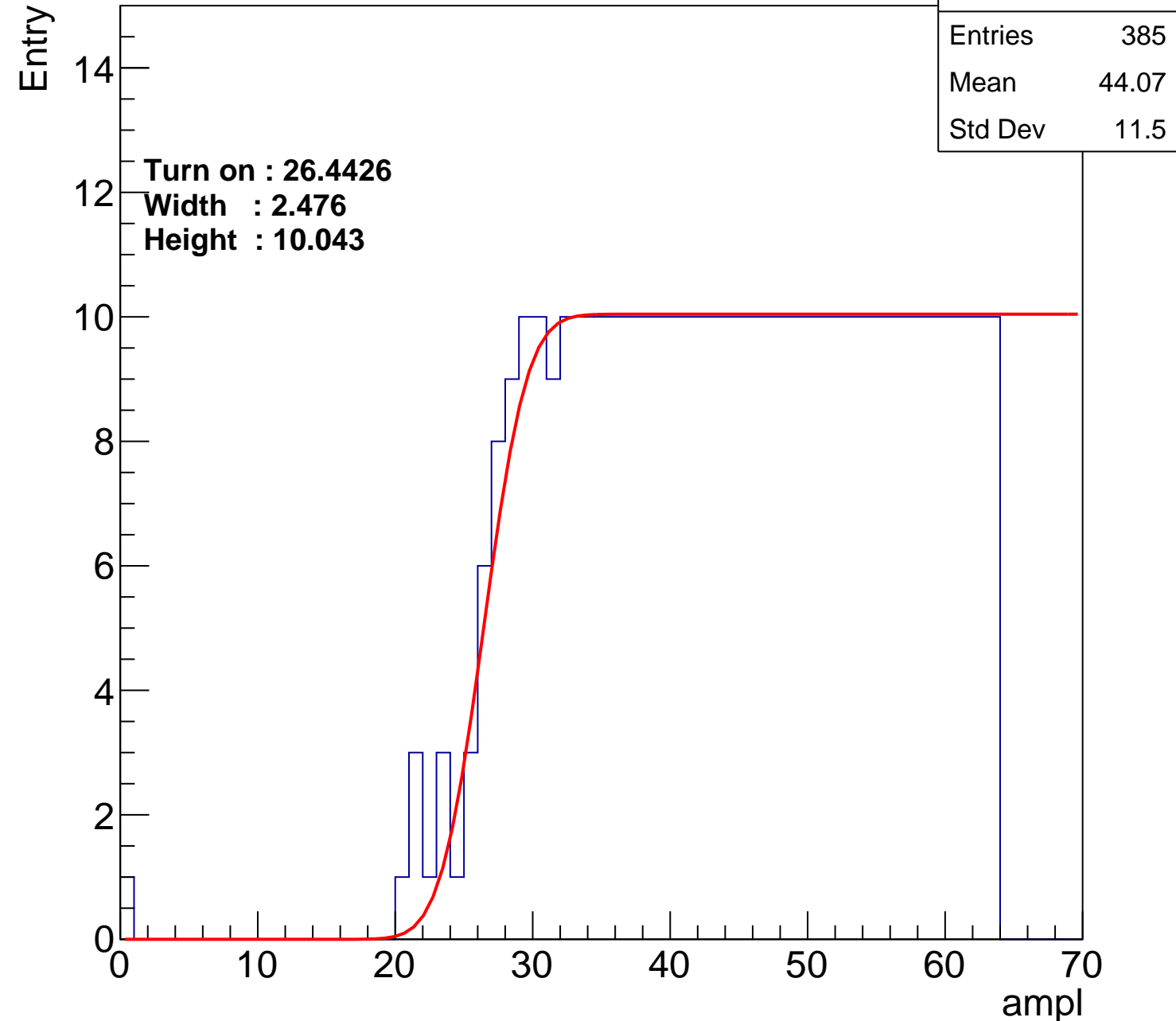
Width : 2.476

Height : 10.043

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U3-ch45

calib_packv5_042523_0143.root, FC#4, port A2

Entries	368
Mean	44.78
Std Dev	11.42

Turn on : 27.6331

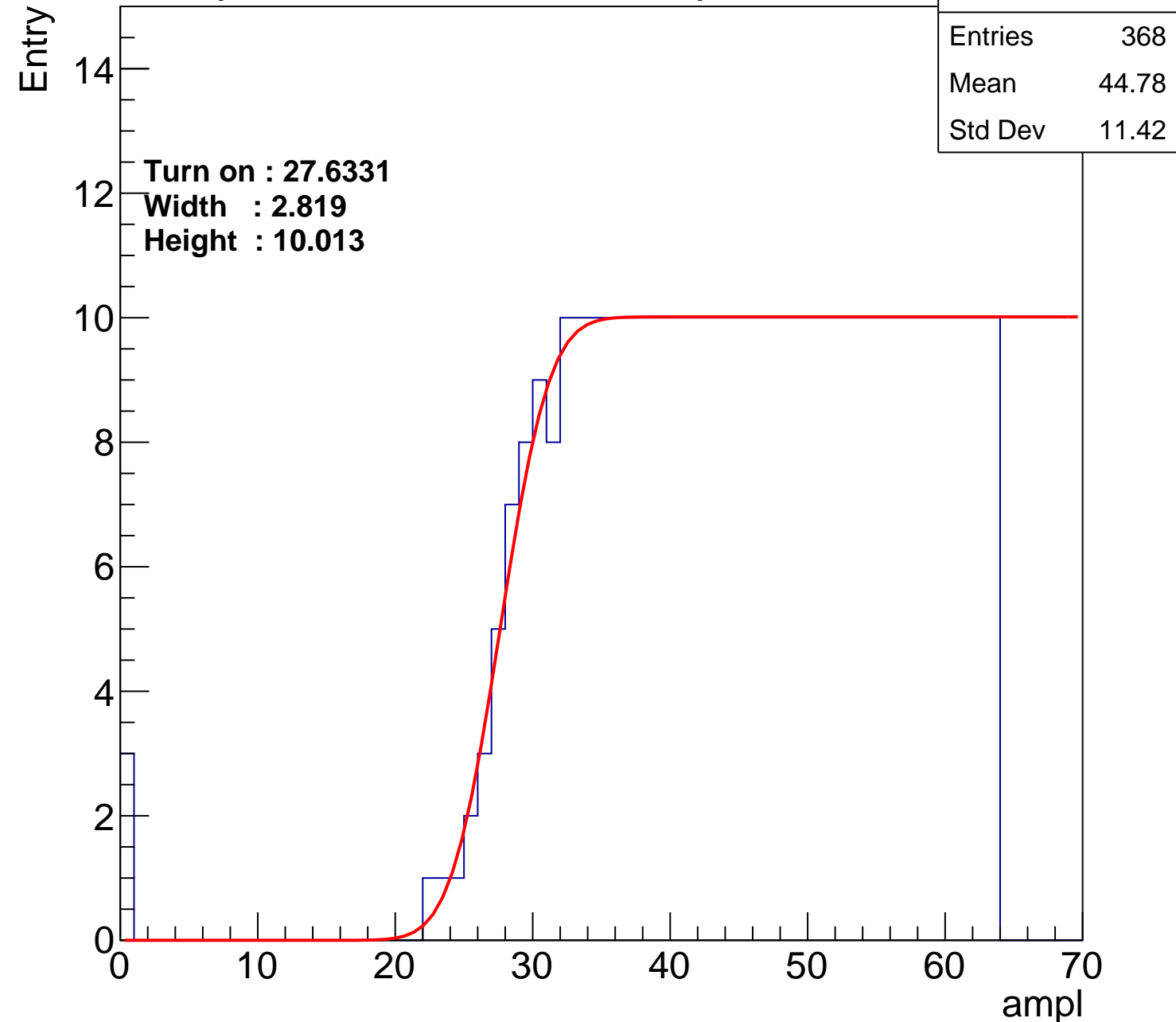
Width : 2.819

Height : 10.013

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U3-ch46

calib_packv5_042523_0143.root, FC#4, port A2

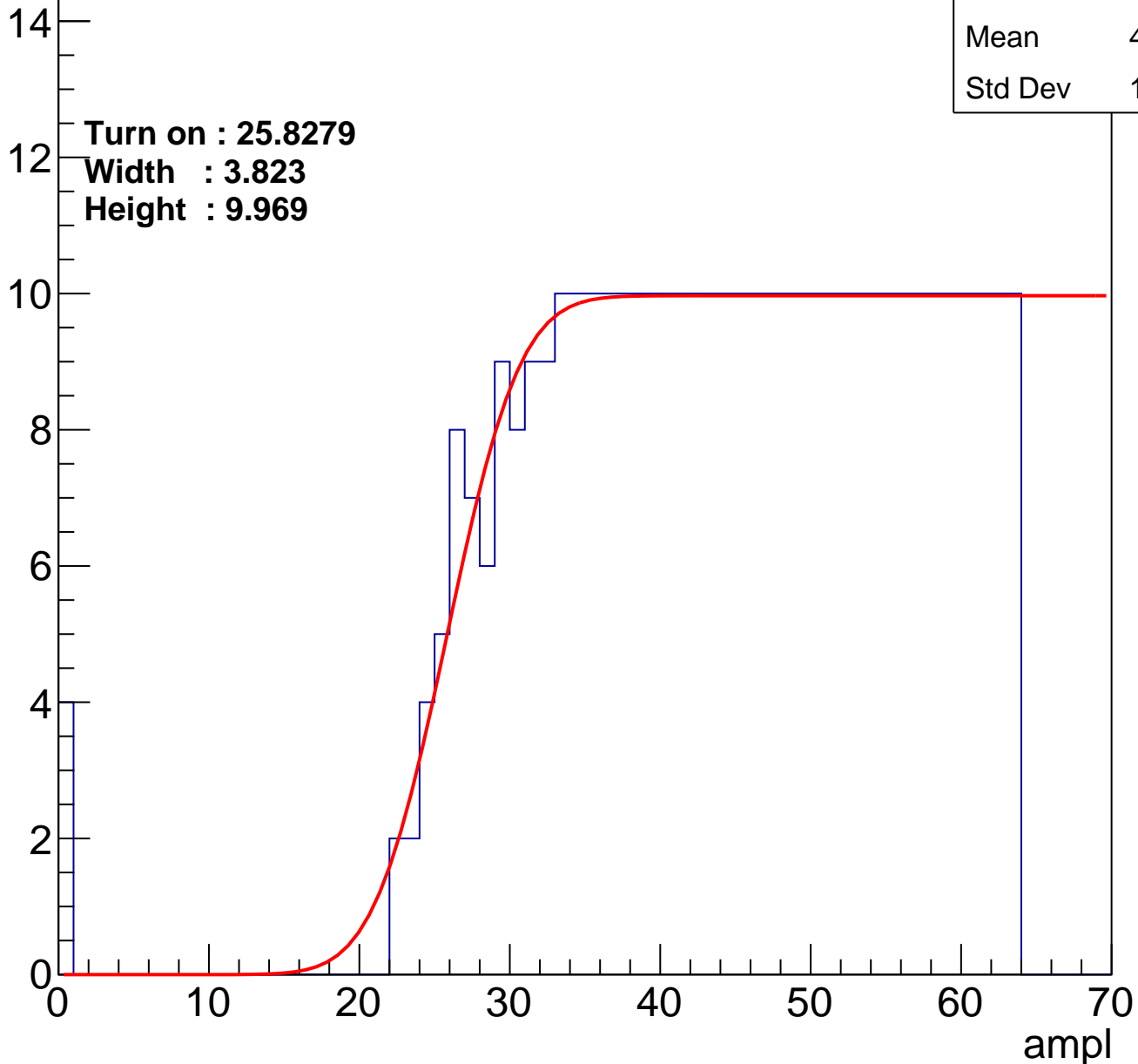
Entries	383
Mean	43.93
Std Dev	12.02

Turn on : 25.8279

Width : 3.823

Height : 9.969

Entry



B1L100S, U3-ch47

calib_packv5_042523_0143.root, FC#4, port A2

Entries	369
Mean	44.82
Std Dev	11.22

Turn on : 27.7435

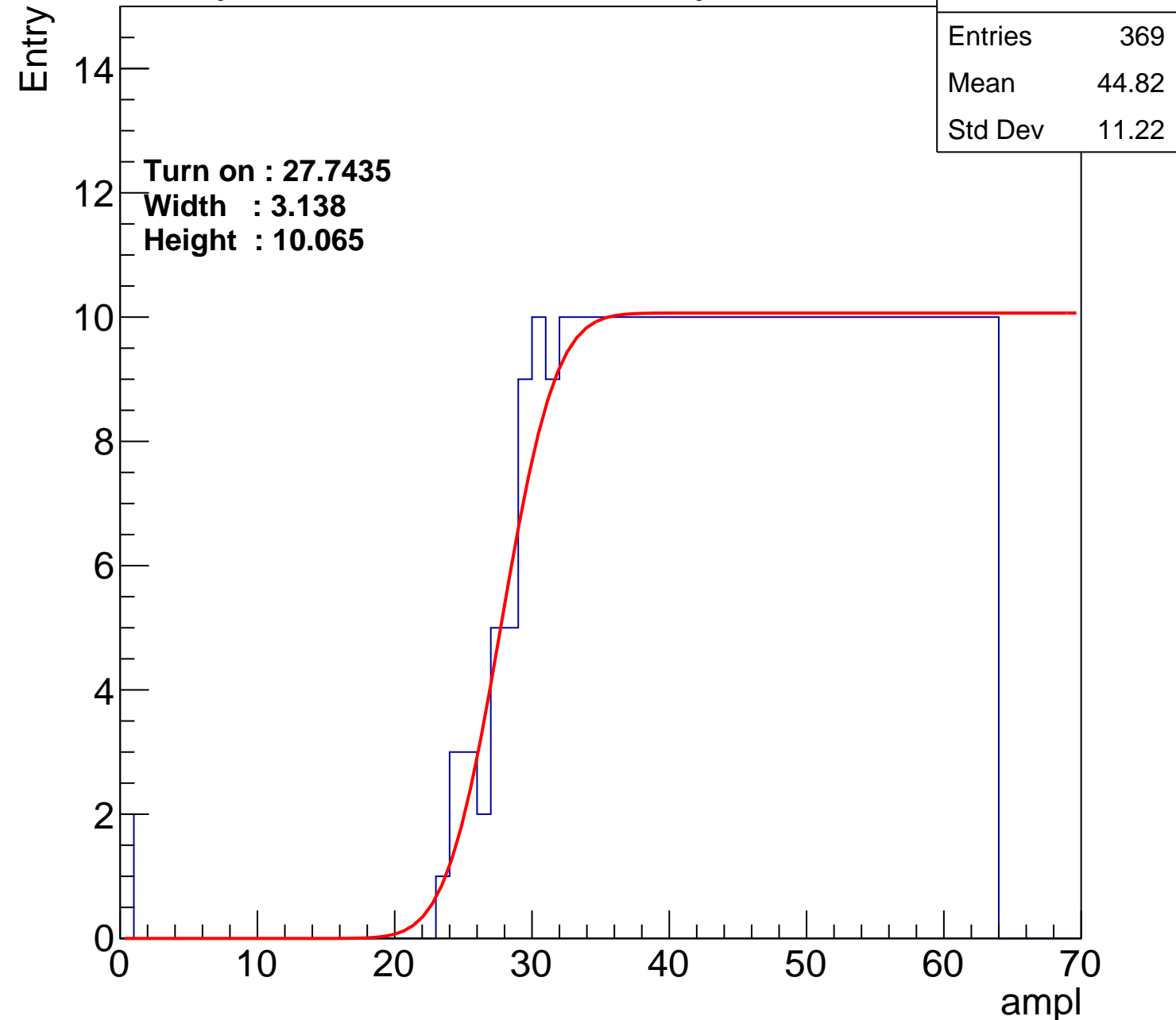
Width : 3.138

Height : 10.065

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U3-ch48

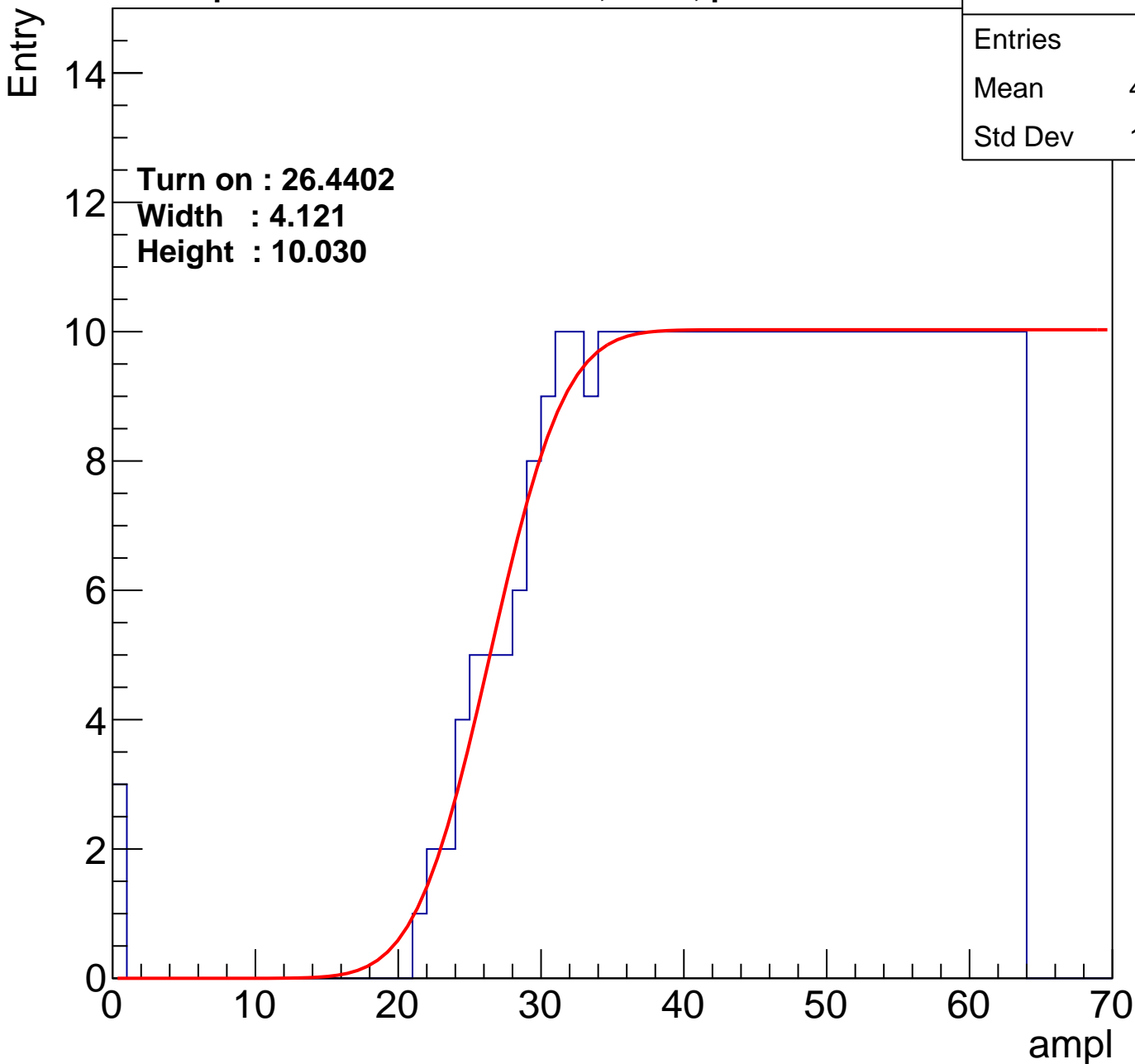
calib_packv5_042523_0143.root, FC#4, port A2

Entries	379
Mean	44.18
Std Dev	11.77

Turn on : 26.4402

Width : 4.121

Height : 10.030



B1L100S, U3-ch49

calib_packv5_042523_0143.root, FC#4, port A2

Entries	361
Mean	45.21
Std Dev	10.91

Turn on : 28.0067

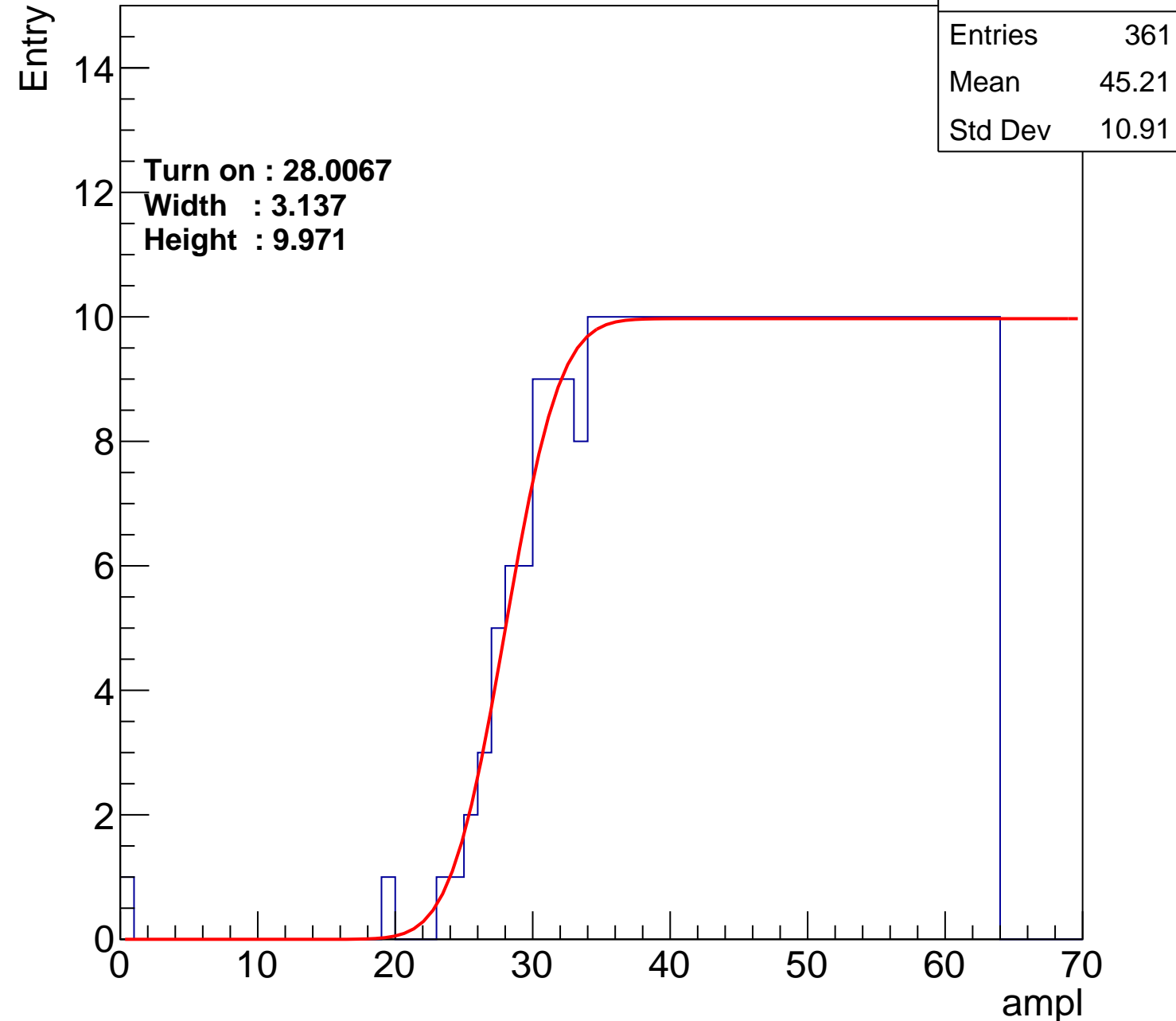
Width : 3.137

Height : 9.971

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U3-ch50

calib_packv5_042523_0143.root, FC#4, port A2

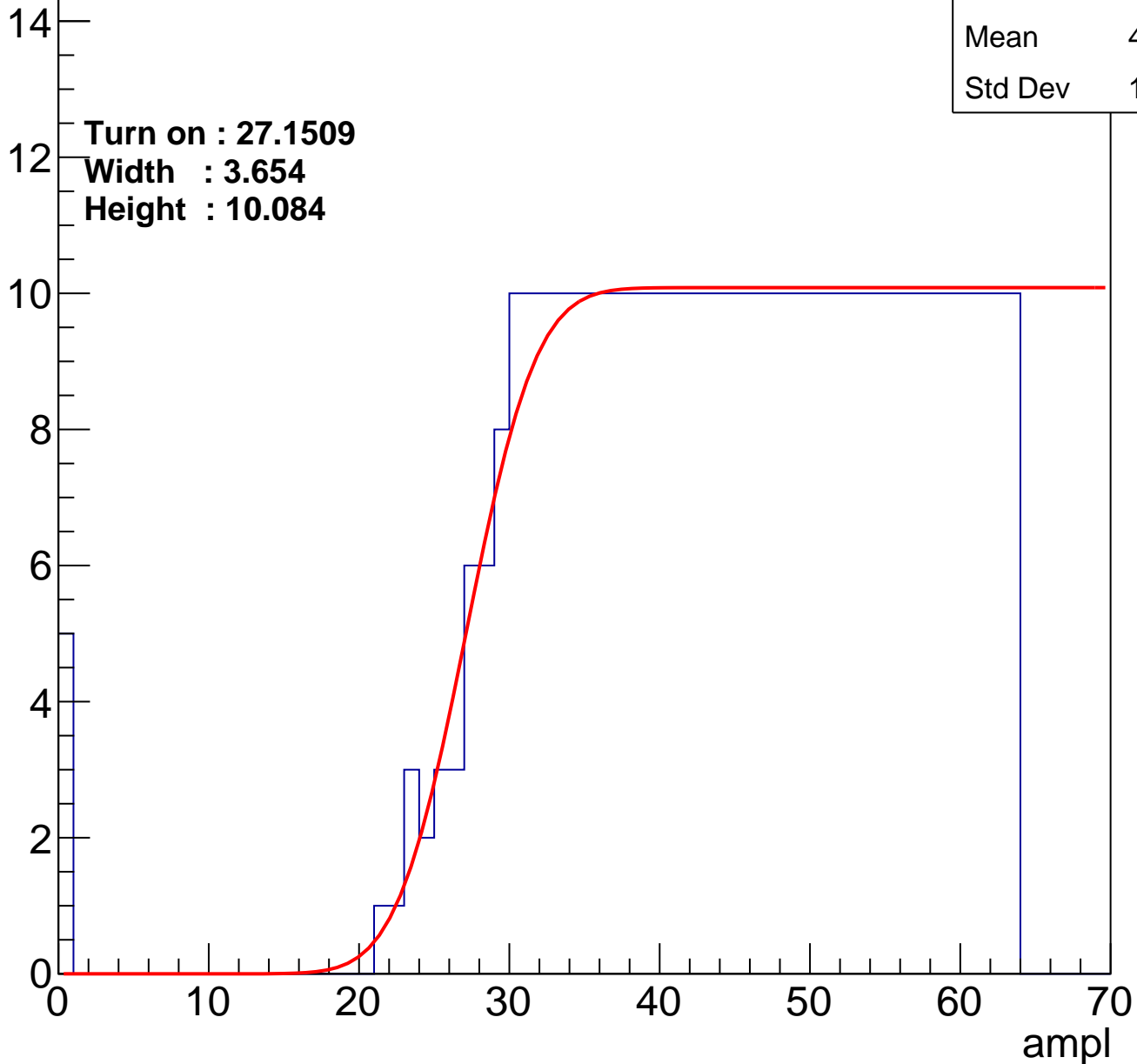
Entries	378
Mean	44.14
Std Dev	12.04

Turn on : 27.1509

Width : 3.654

Height : 10.084

Entry



B1L100S, U3-ch51

calib_packv5_042523_0143.root, FC#4, port A2

Entries	370
Mean	44.61
Std Dev	11.64

Turn on : 27.1169

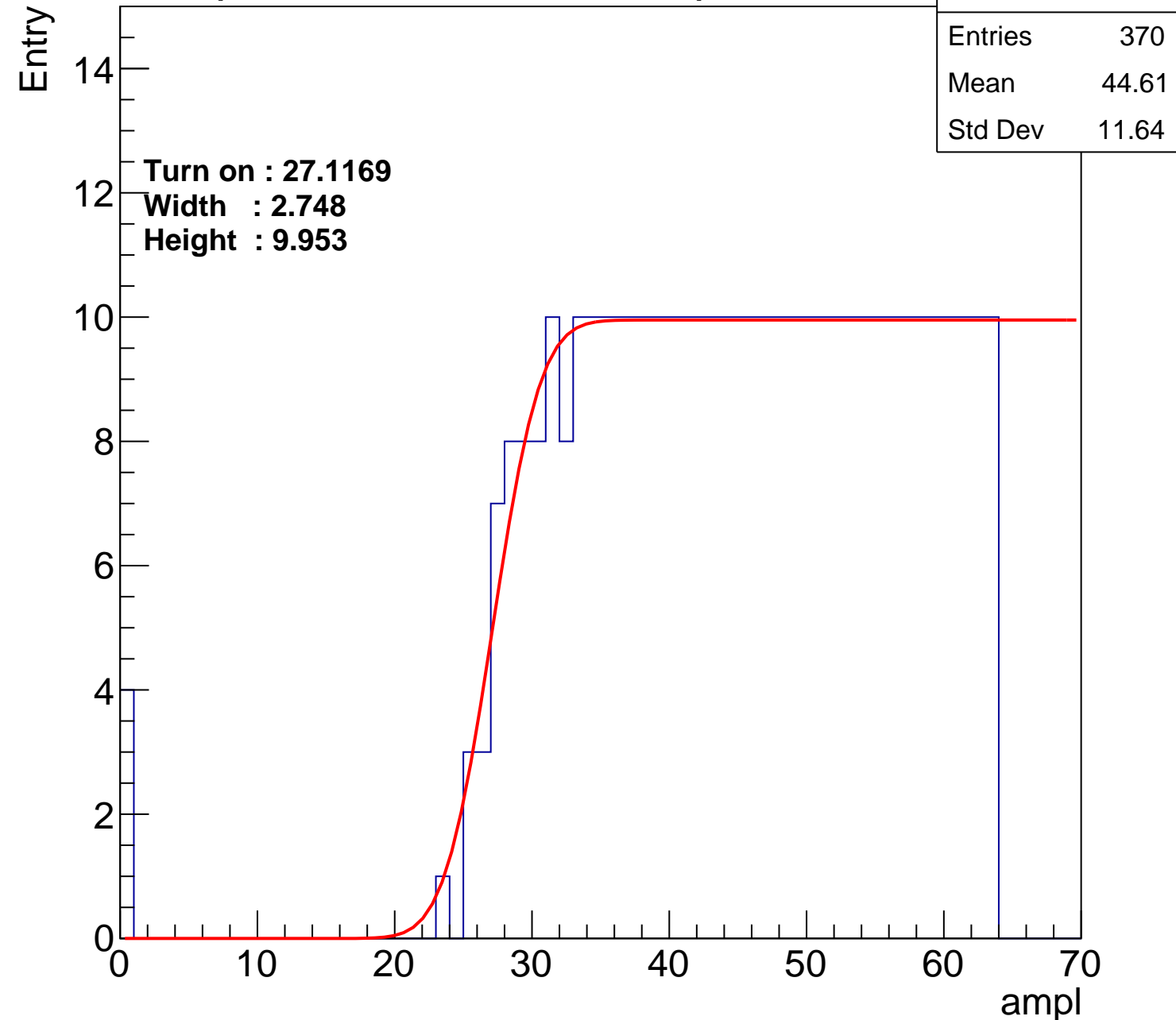
Width : 2.748

Height : 9.953

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U3-ch52

calib_packv5_042523_0143.root, FC#4, port A2

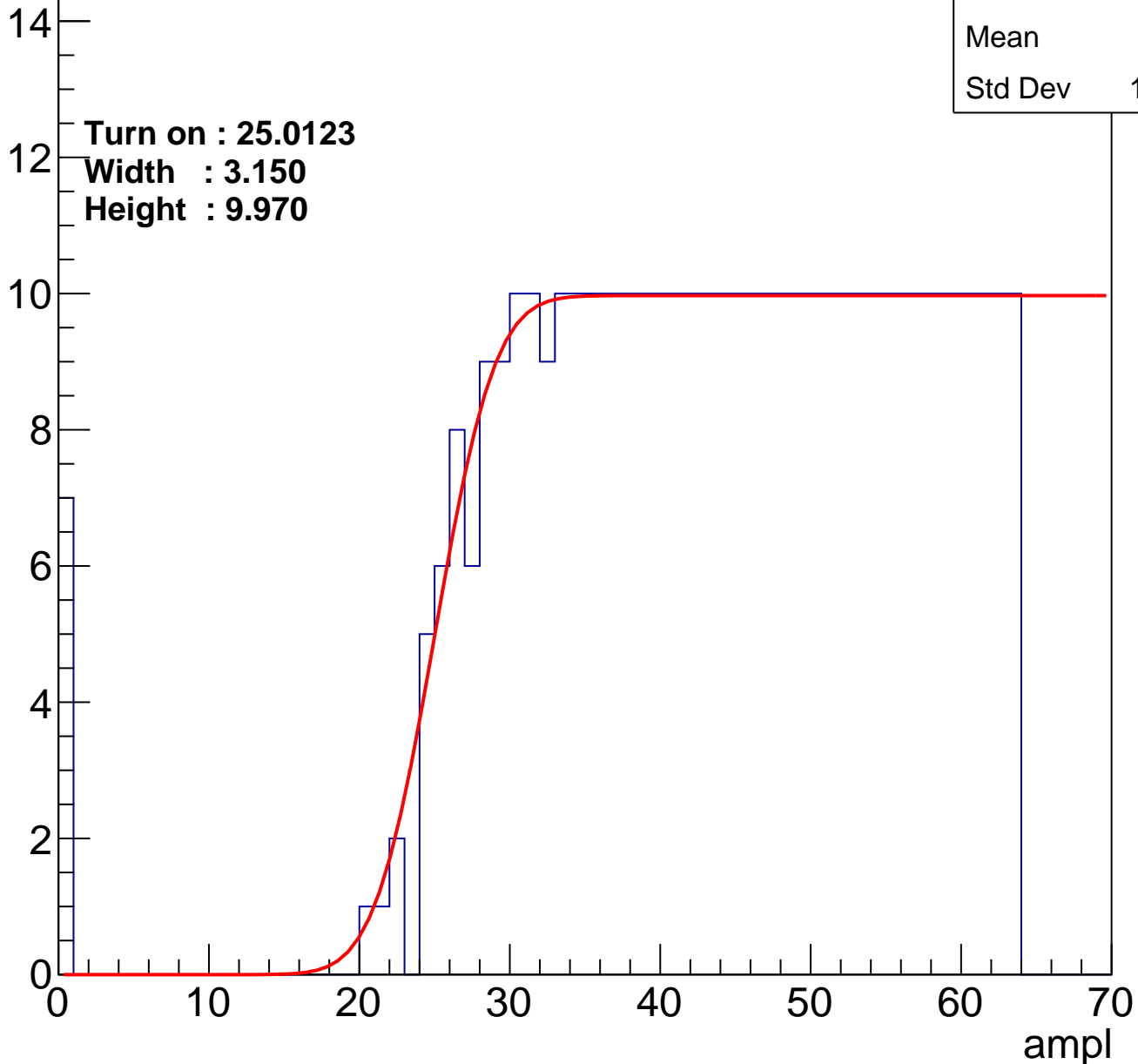
Entries	393
Mean	43.3
Std Dev	12.66

Turn on : 25.0123

Width : 3.150

Height : 9.970

Entry



B1L100S, U3-ch53

calib_packv5_042523_0143.root, FC#4, port A2

Entries	386
Mean	43.95
Std Dev	11.77

Turn on : 25.9244

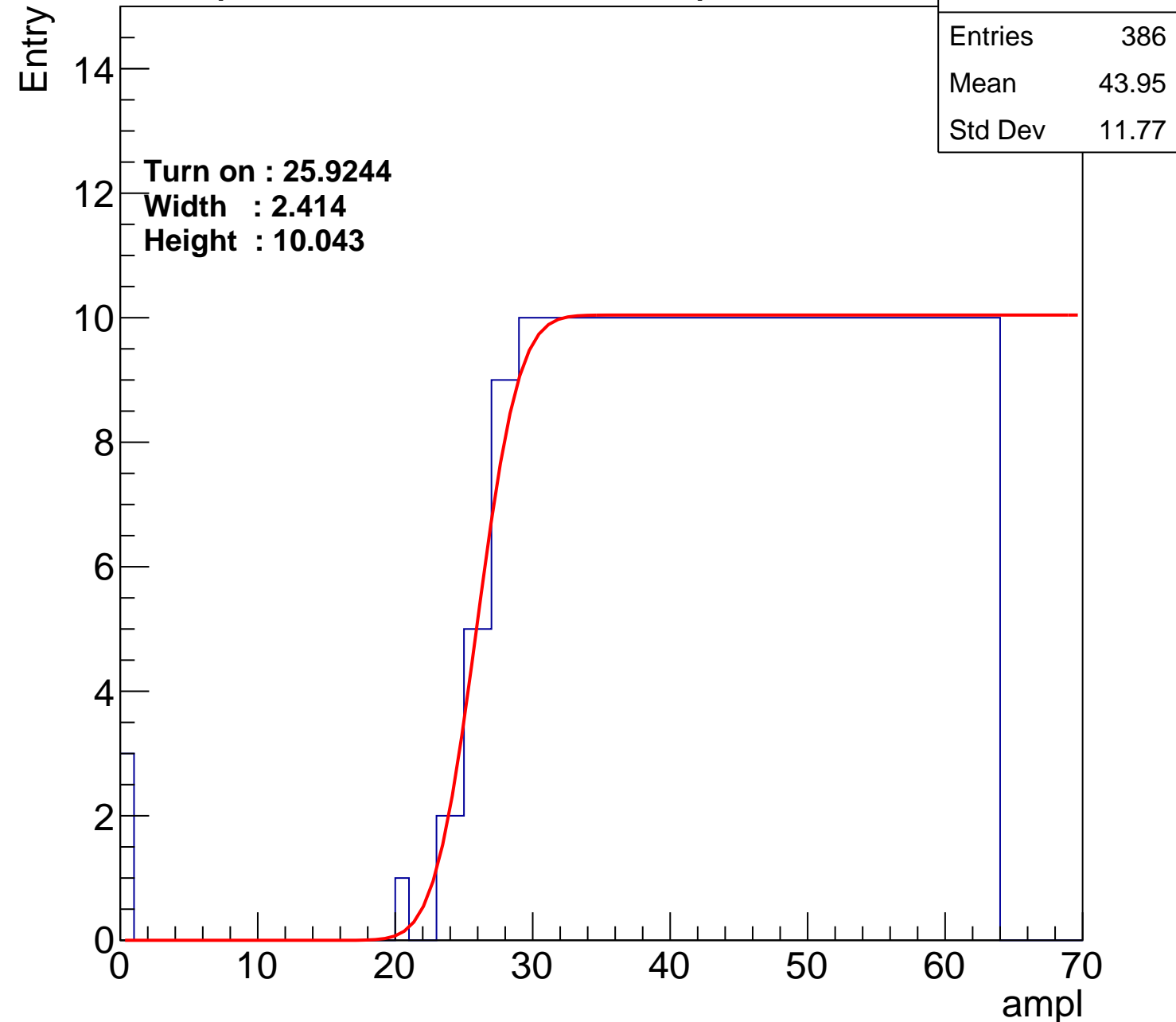
Width : 2.414

Height : 10.043

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U3-ch54

calib_packv5_042523_0143.root, FC#4, port A2

Entries	385
Mean	43.83
Std Dev	12.07

Turn on : 26.4972

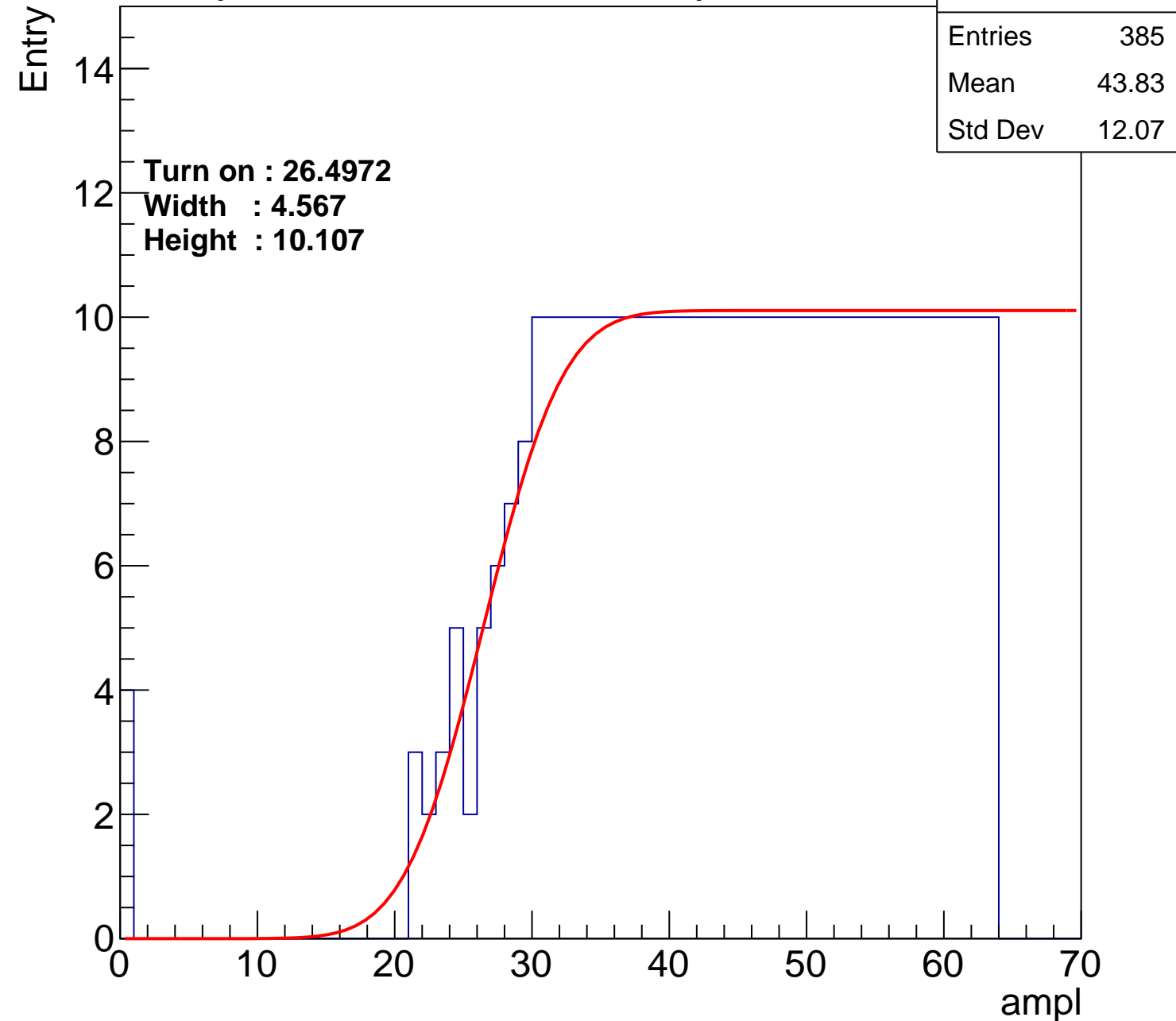
Width : 4.567

Height : 10.107

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U3-ch55

calib_packv5_042523_0143.root, FC#4, port A2

Entries	356
Mean	45.33
Std Dev	11.19

Turn on : 28.9976

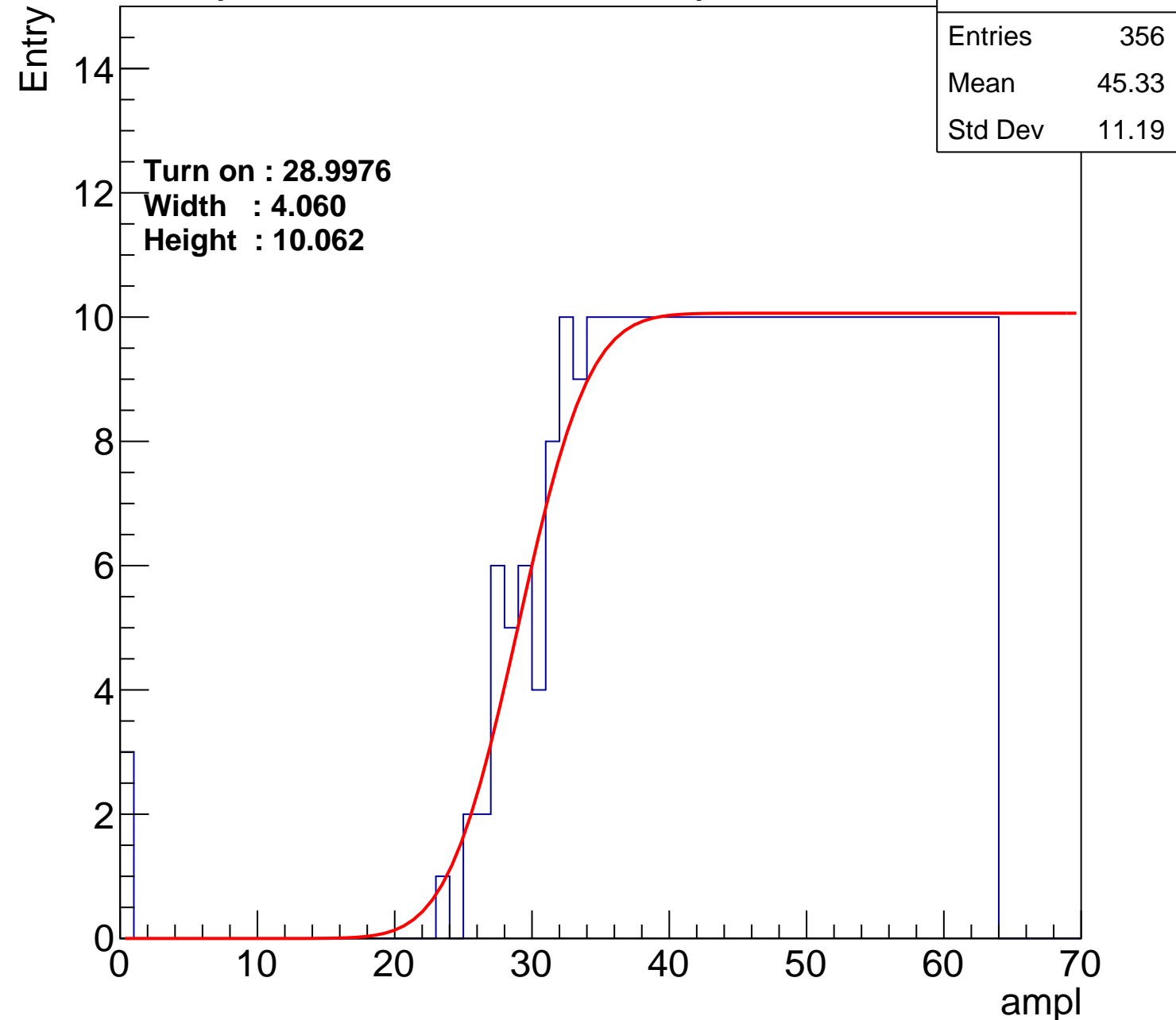
Width : 4.060

Height : 10.062

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U3-ch56

calib_packv5_042523_0143.root, FC#4, port A2

Entries	370
Mean	44.48
Std Dev	11.93

Turn on : 28.0278

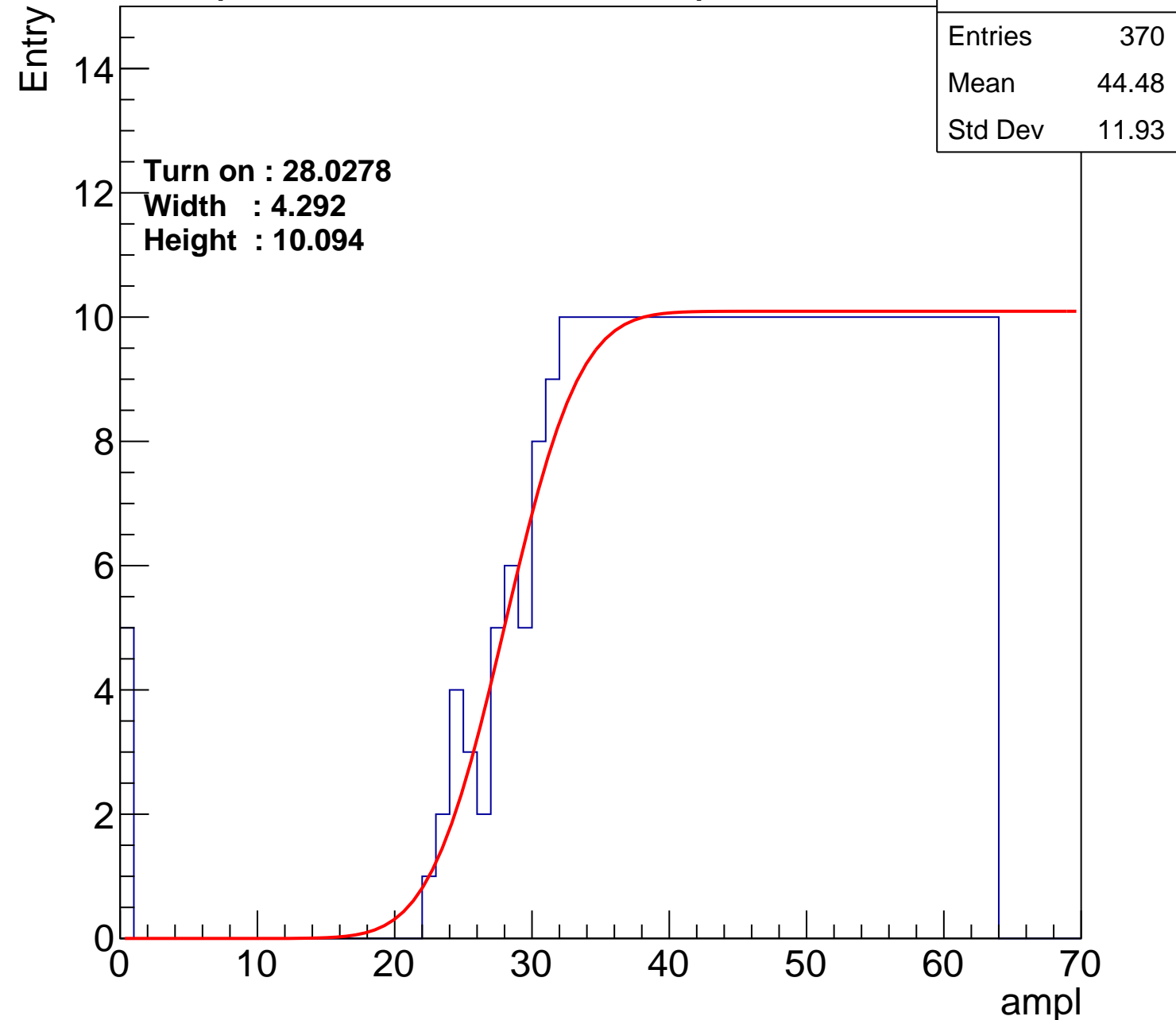
Width : 4.292

Height : 10.094

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U3-ch57

calib_packv5_042523_0143.root, FC#4, port A2

Entries	379
Mean	44.4
Std Dev	11.27

Turn on : 26.1842

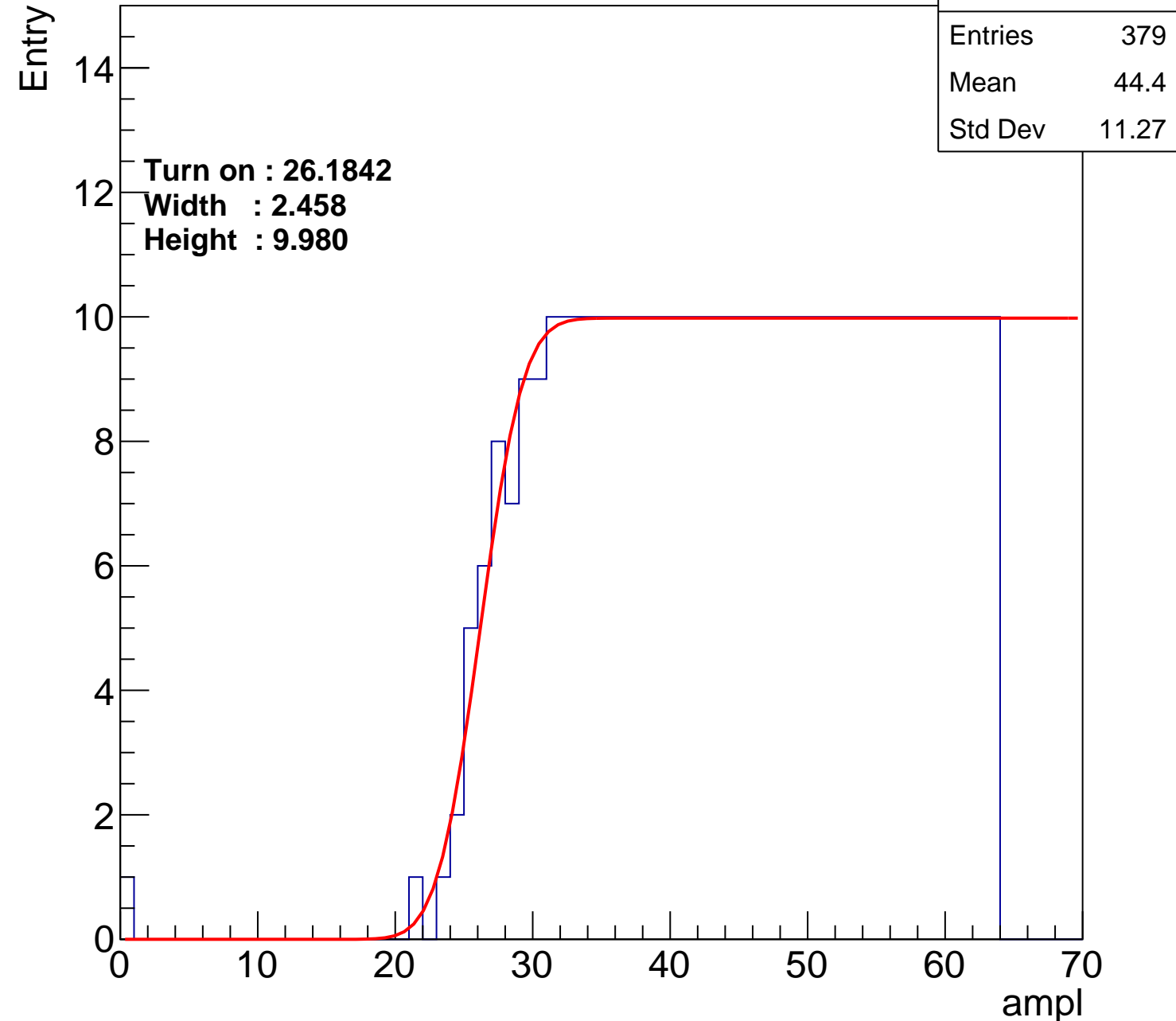
Width : 2.458

Height : 9.980

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U3-ch58

calib_packv5_042523_0143.root, FC#4, port A2

Entries	392
Mean	43.69
Std Dev	11.8

Turn on : 24.9993

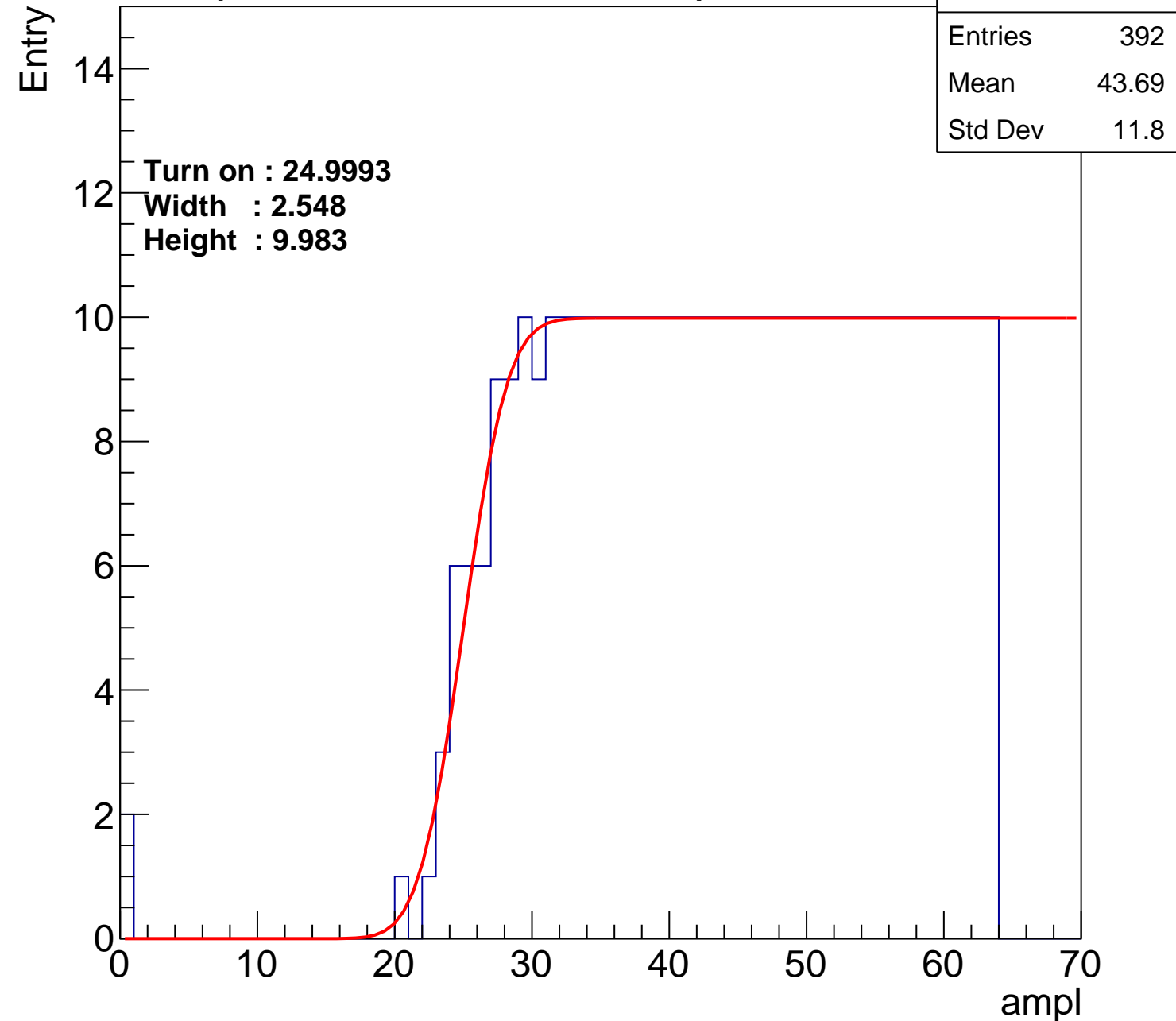
Width : 2.548

Height : 9.983

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U3-ch59

calib_packv5_042523_0143.root, FC#4, port A2

Entries	407
Mean	42.89
Std Dev	12.34

Turn on : 23.9178

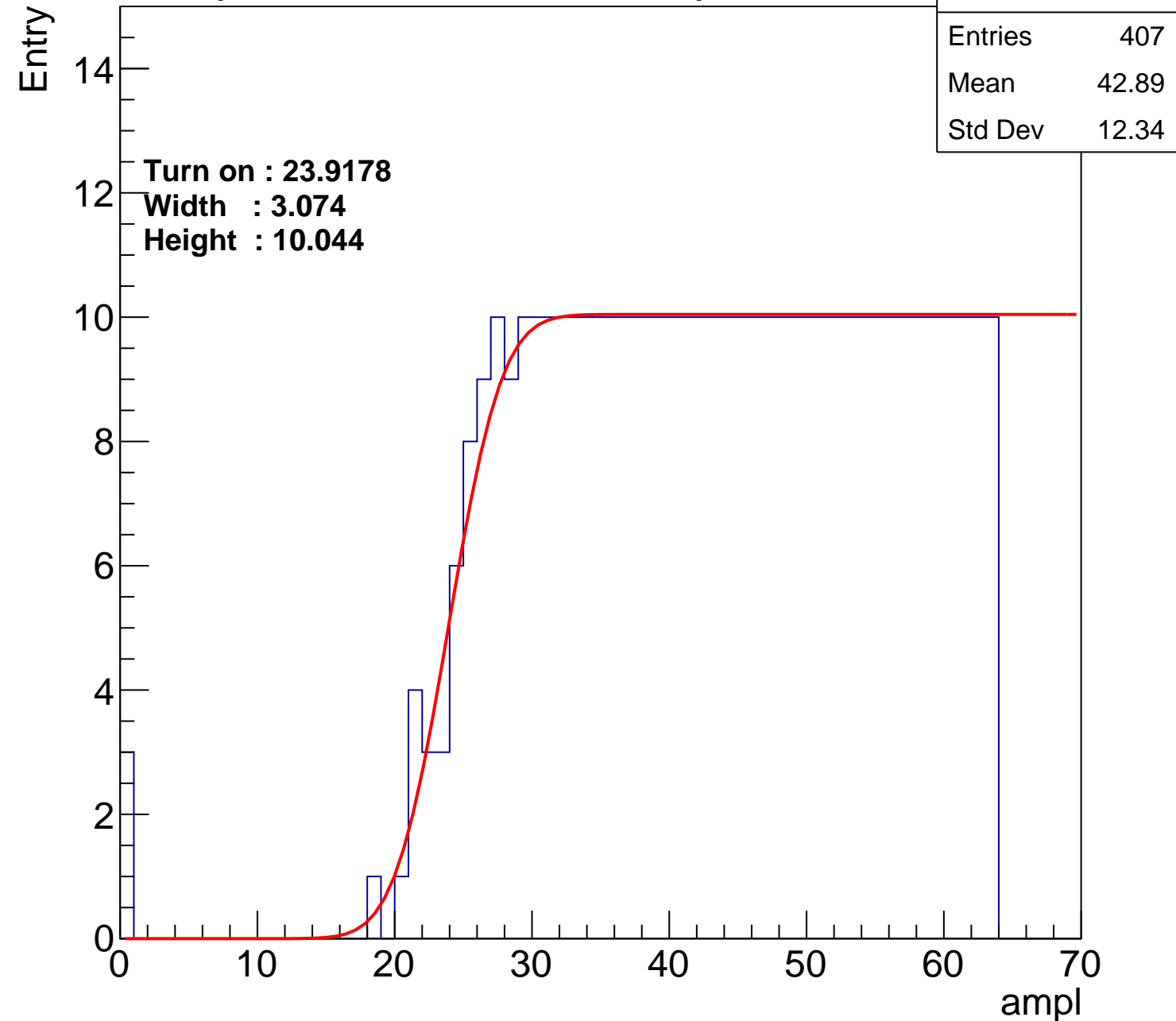
Width : 3.074

Height : 10.044

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U3-ch60

calib_packv5_042523_0143.root, FC#4, port A2

Entries	391
Mean	43.57
Std Dev	12.23

Turn on : 25.6008

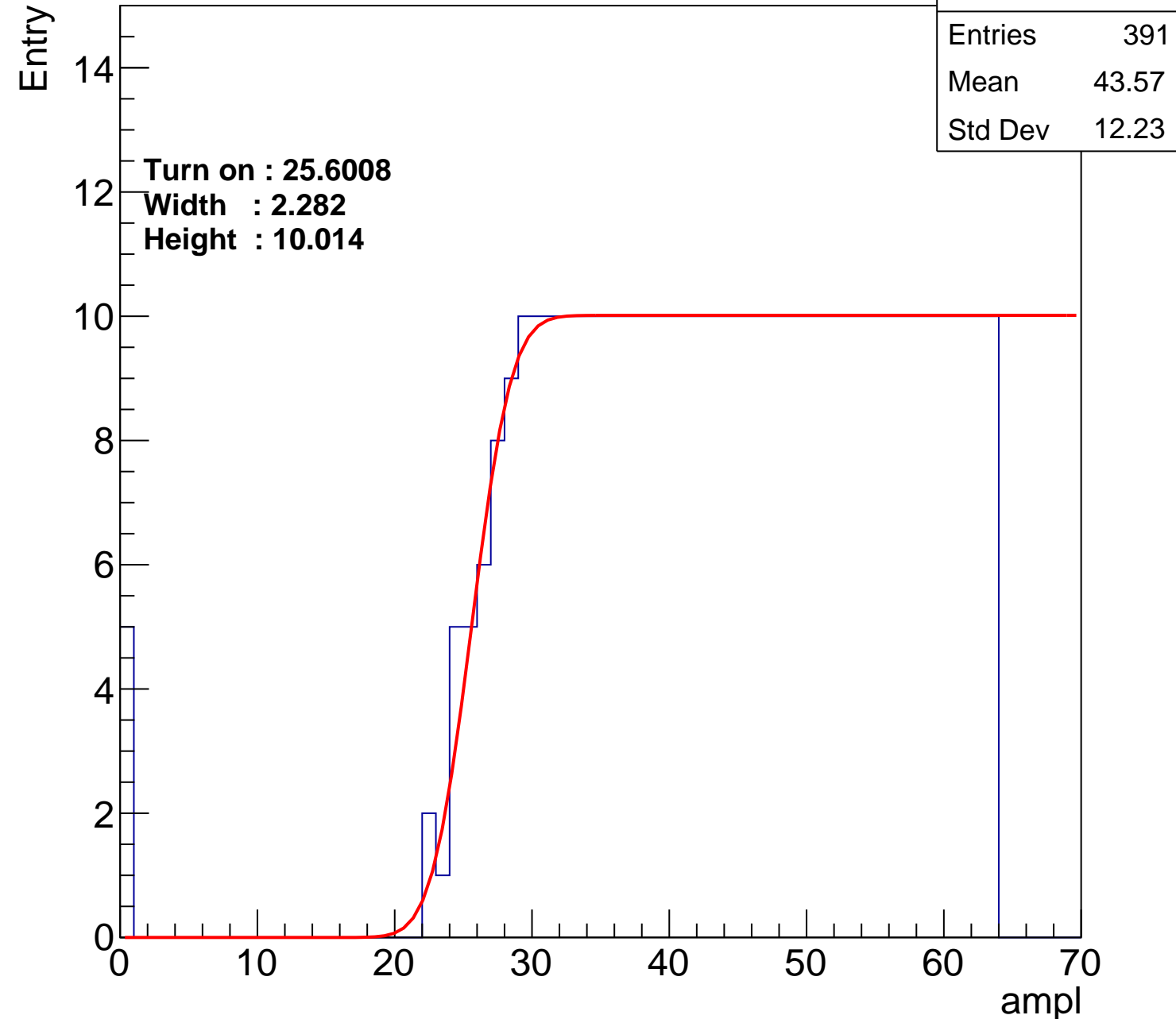
Width : 2.282

Height : 10.014

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U3-ch61

calib_packv5_042523_0143.root, FC#4, port A2

Entries	391
Mean	43.54
Std Dev	12.28

Turn on : 25.7691

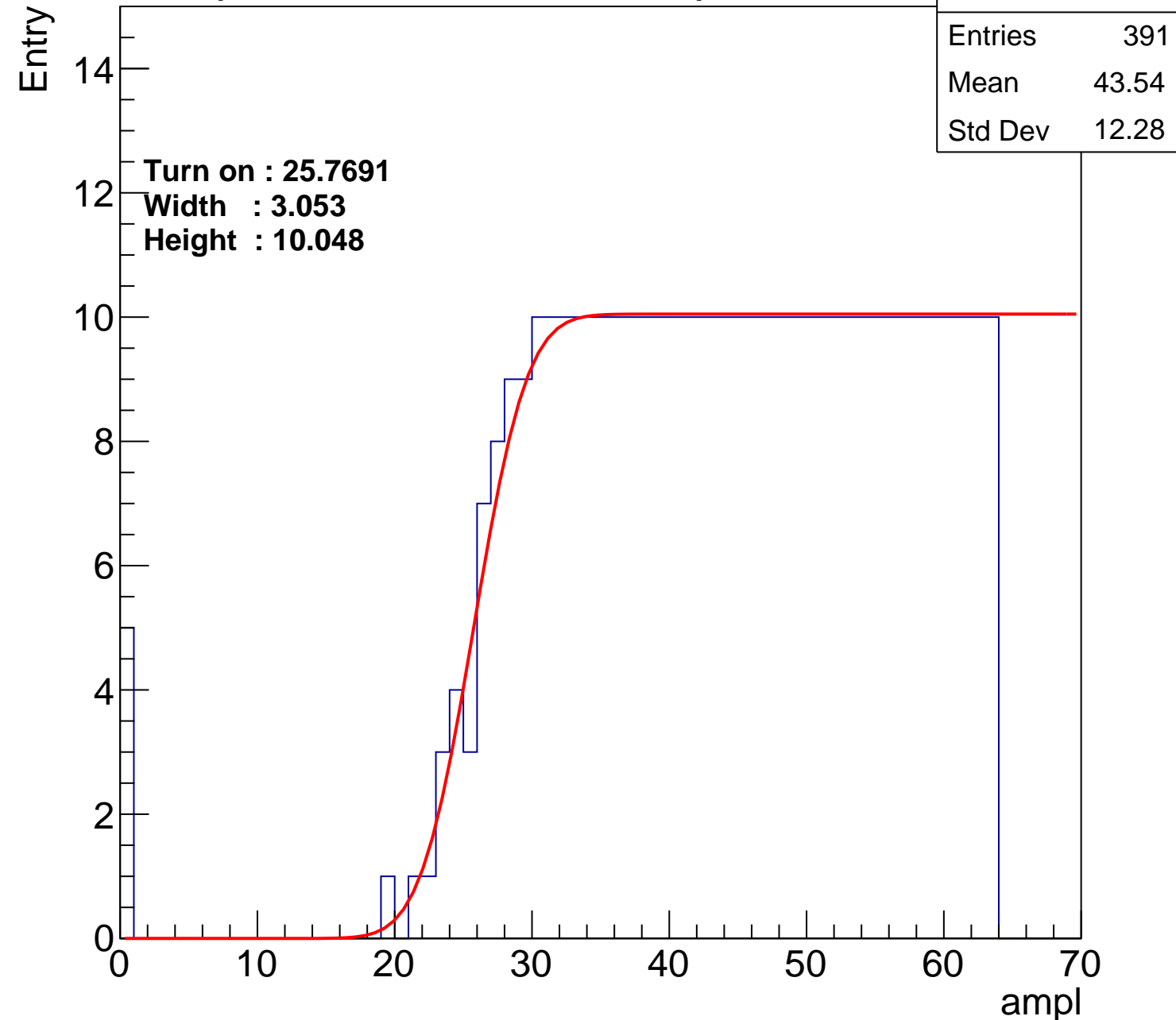
Width : 3.053

Height : 10.048

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U3-ch62

calib_packv5_042523_0143.root, FC#4, port A2

Entries	384
Mean	44.07
Std Dev	11.62

Turn on : 25.9710

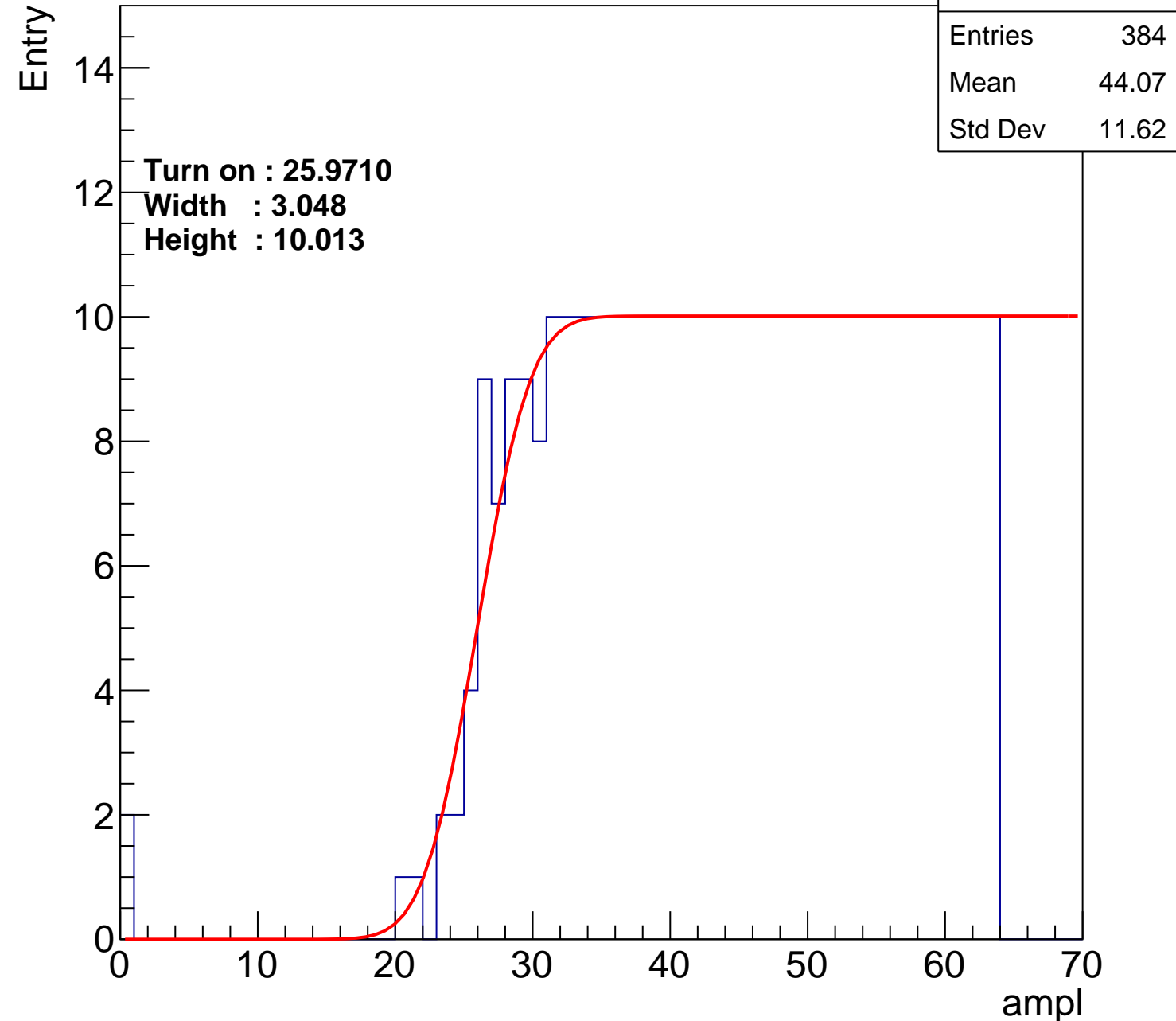
Width : 3.048

Height : 10.013

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U3-ch63

calib_packv5_042523_0143.root, FC#4, port A2

Entries	378
Mean	44.21
Std Dev	11.85

Turn on : 27.3160

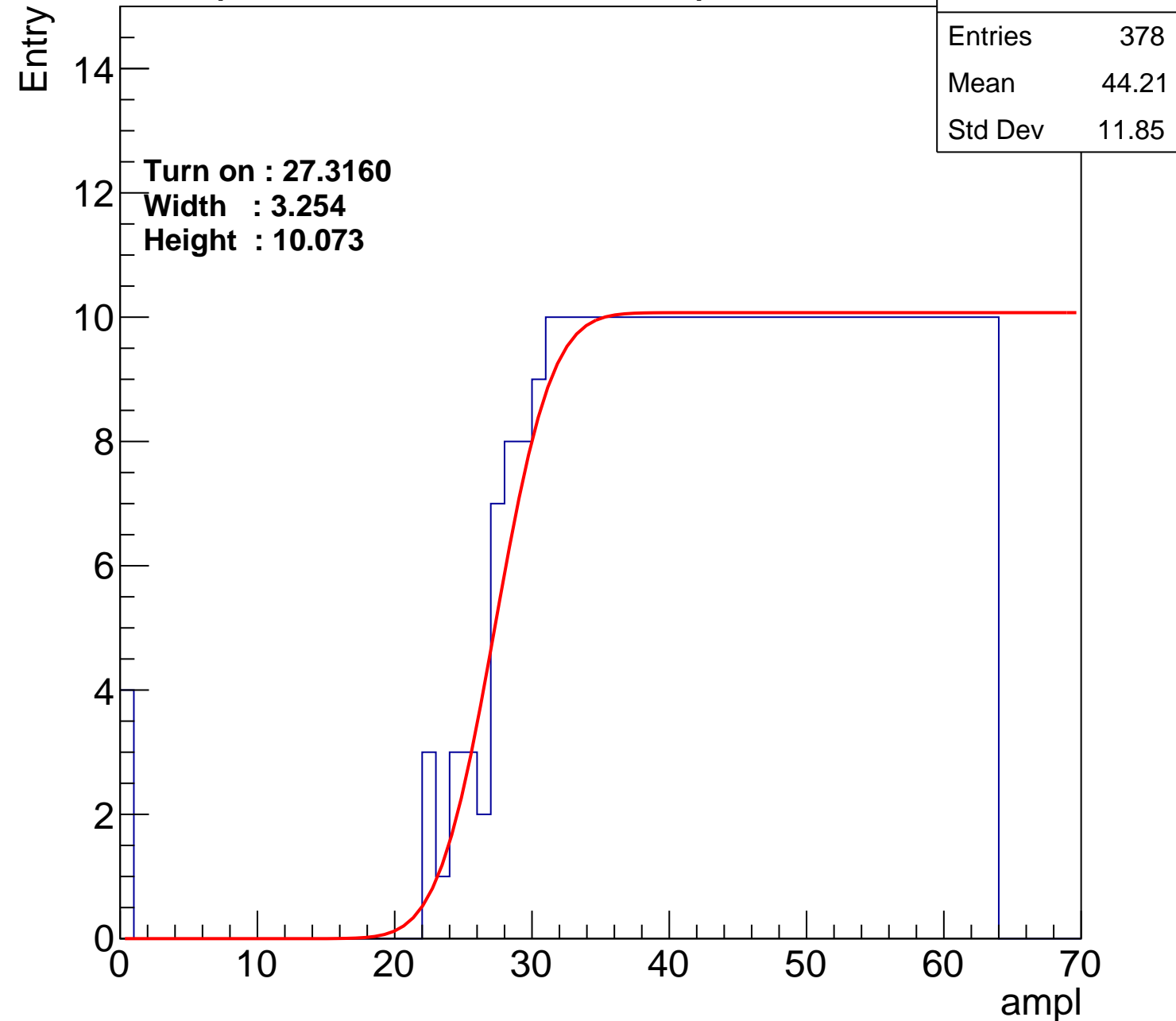
Width : 3.254

Height : 10.073

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U3-ch64

calib_packv5_042523_0143.root, FC#4, port A2

Entries	369
Mean	44.7
Std Dev	11.49

Turn on : 27.7325

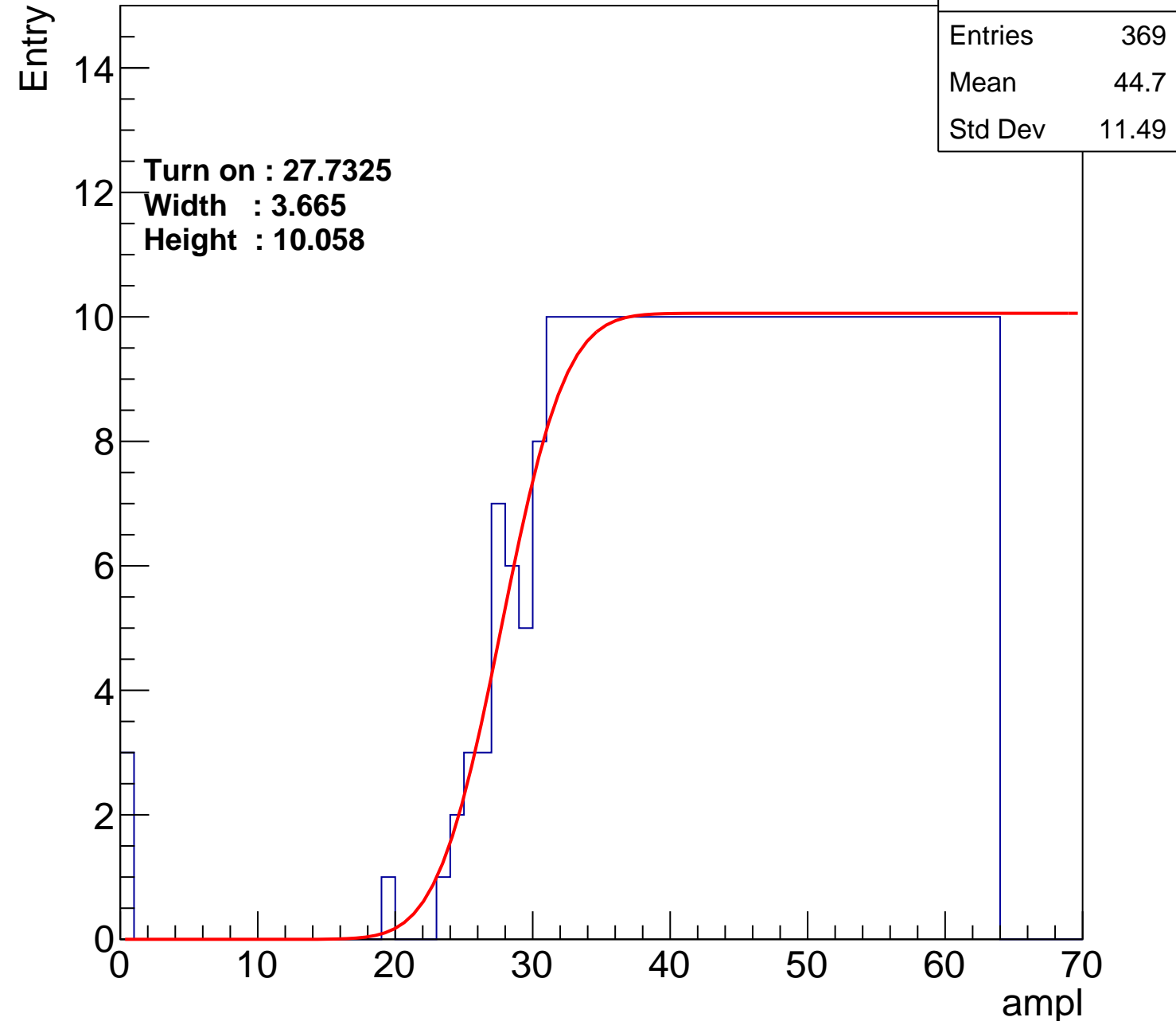
Width : 3.665

Height : 10.058

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U3-ch65

calib_packv5_042523_0143.root, FC#4, port A2

Entries	384
Mean	43.97
Std Dev	11.84

Turn on : 26.0650

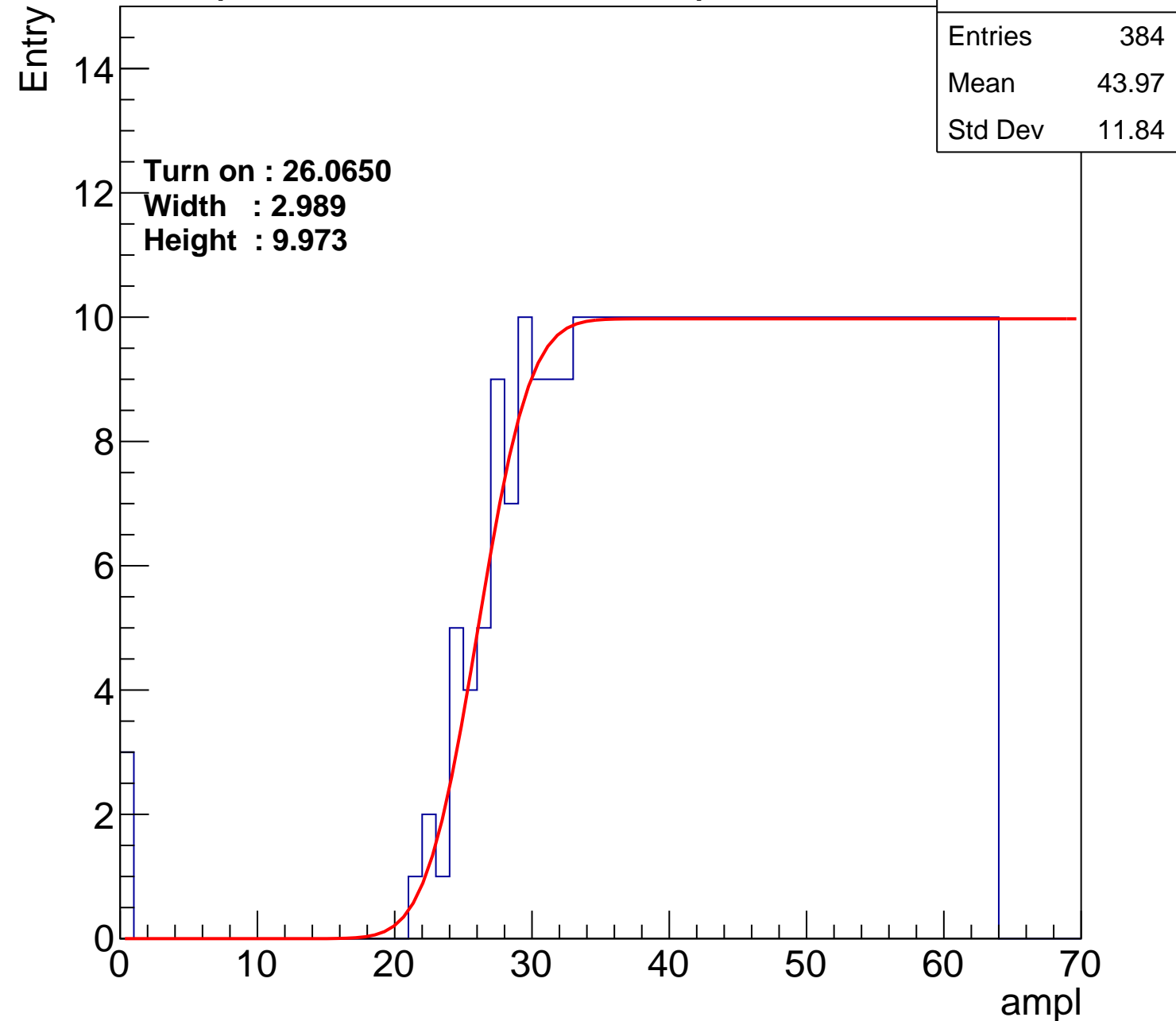
Width : 2.989

Height : 9.973

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U3-ch66

calib_packv5_042523_0143.root, FC#4, port A2

Entries	374
Mean	44.49
Std Dev	11.55

Turn on : 26.8589

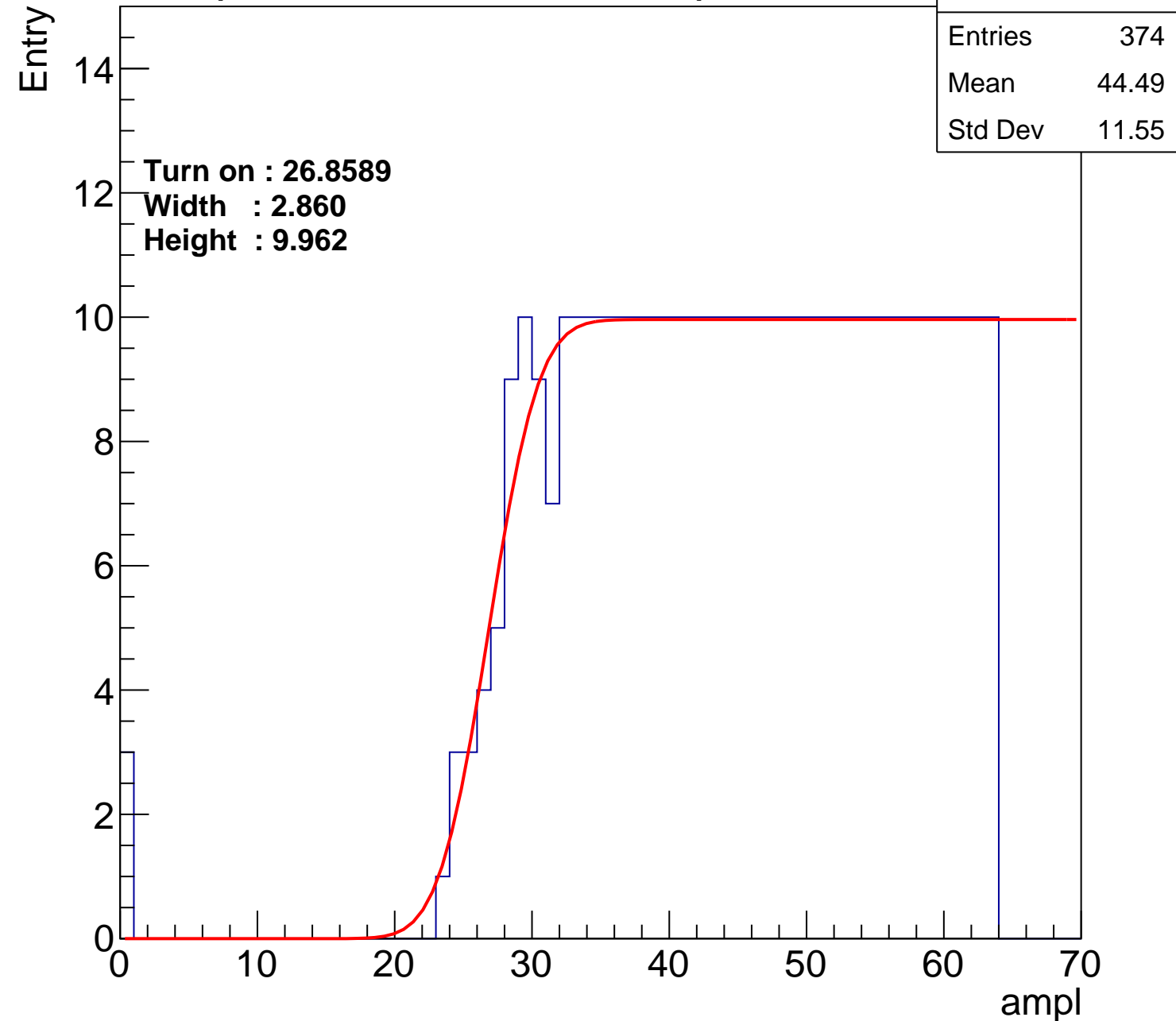
Width : 2.860

Height : 9.962

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U3-ch67

calib_packv5_042523_0143.root, FC#4, port A2

Entries	383
Mean	44.15
Std Dev	11.54

Turn on : 26.1975

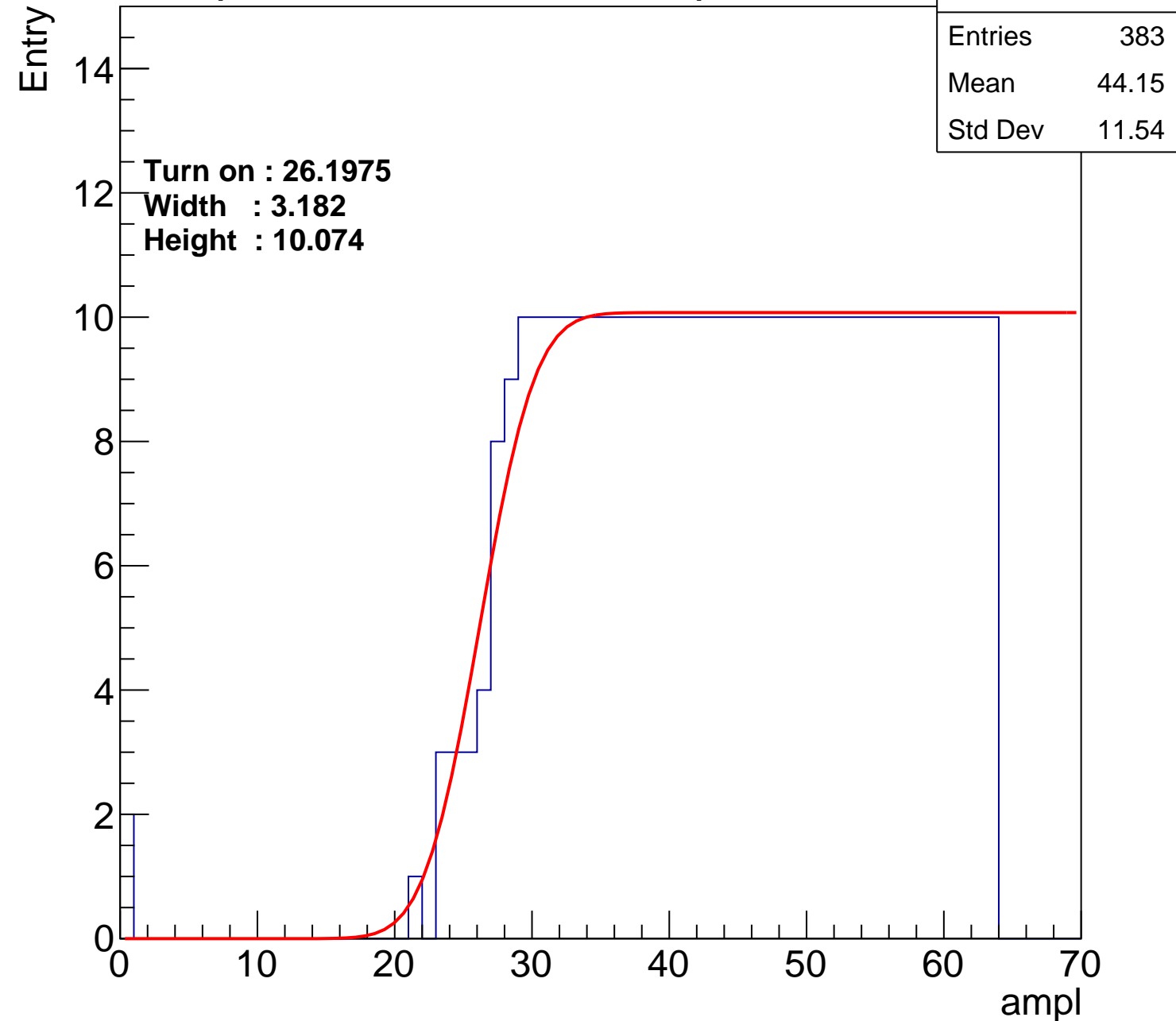
Width : 3.182

Height : 10.074

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U3-ch68

calib_packv5_042523_0143.root, FC#4, port A2

Entries	385
Mean	44.04
Std Dev	11.54

Turn on : 26.3748

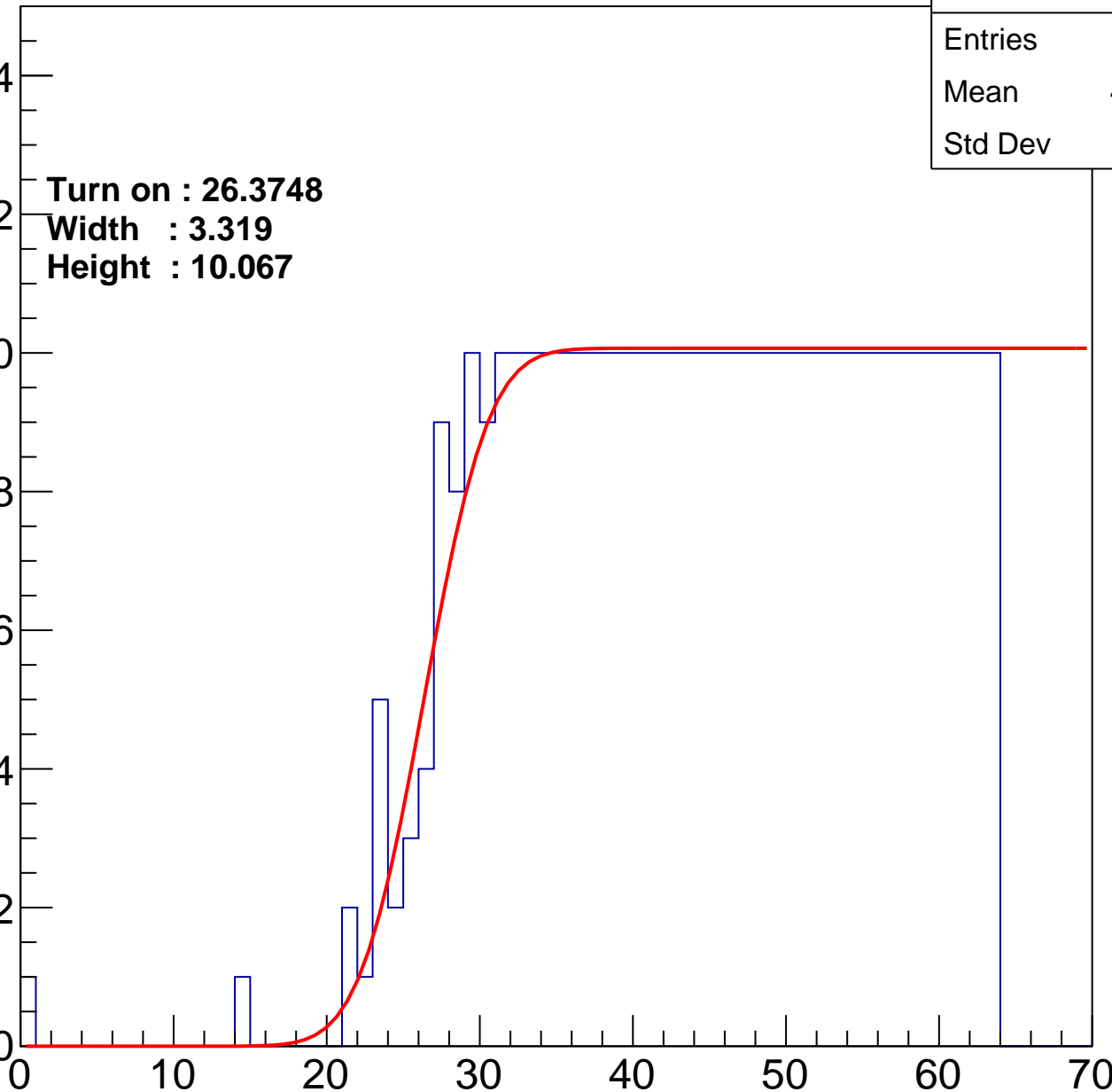
Width : 3.319

Height : 10.067

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U3-ch69

calib_packv5_042523_0143.root, FC#4, port A2

Entries	380
Mean	44.19
Std Dev	11.62

Turn on : 26.3031

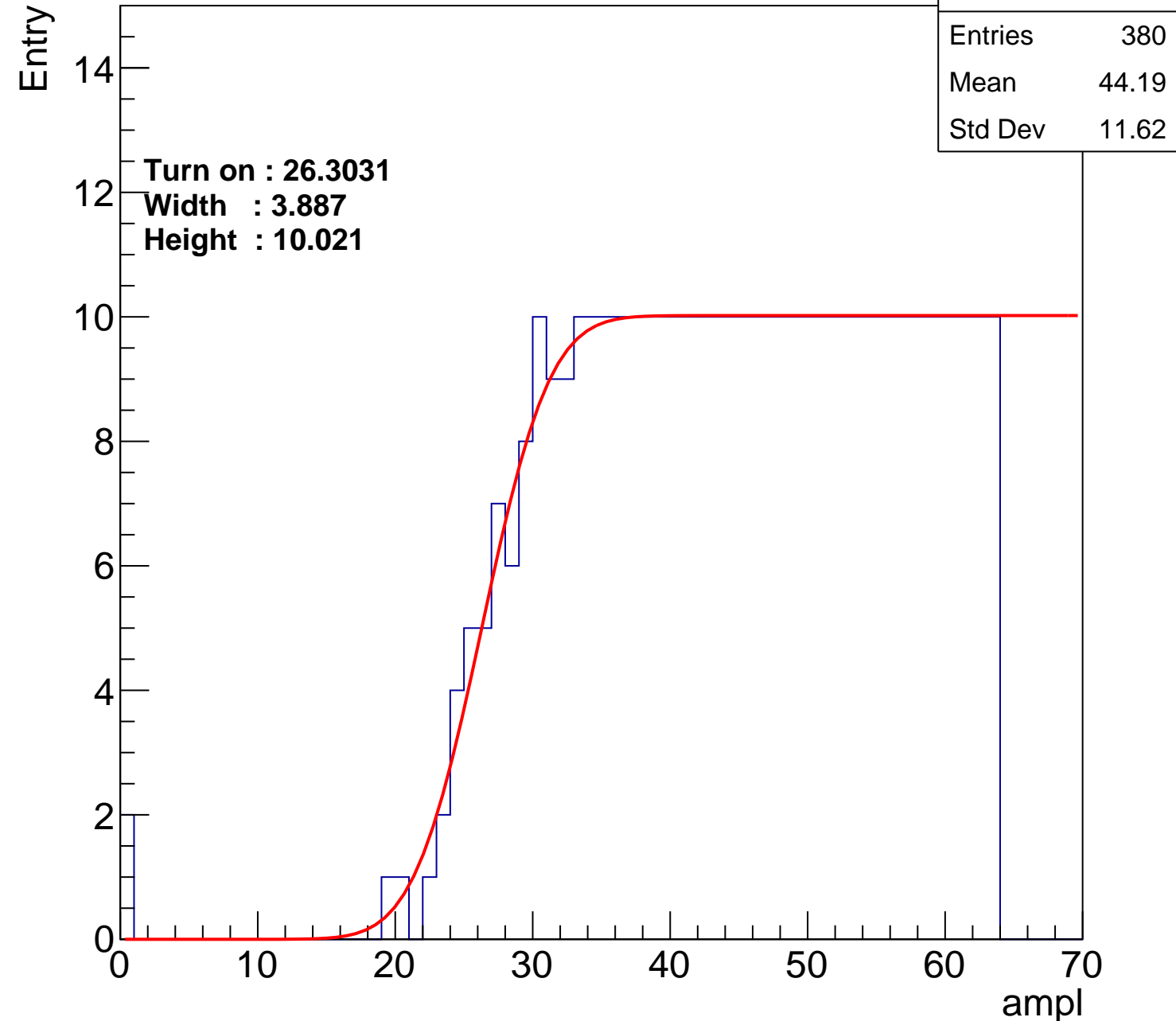
Width : 3.887

Height : 10.021

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U3-ch70

calib_packv5_042523_0143.root, FC#4, port A2

Entries	408
Mean	42.76
Std Dev	12.54

Turn on : 23.9292

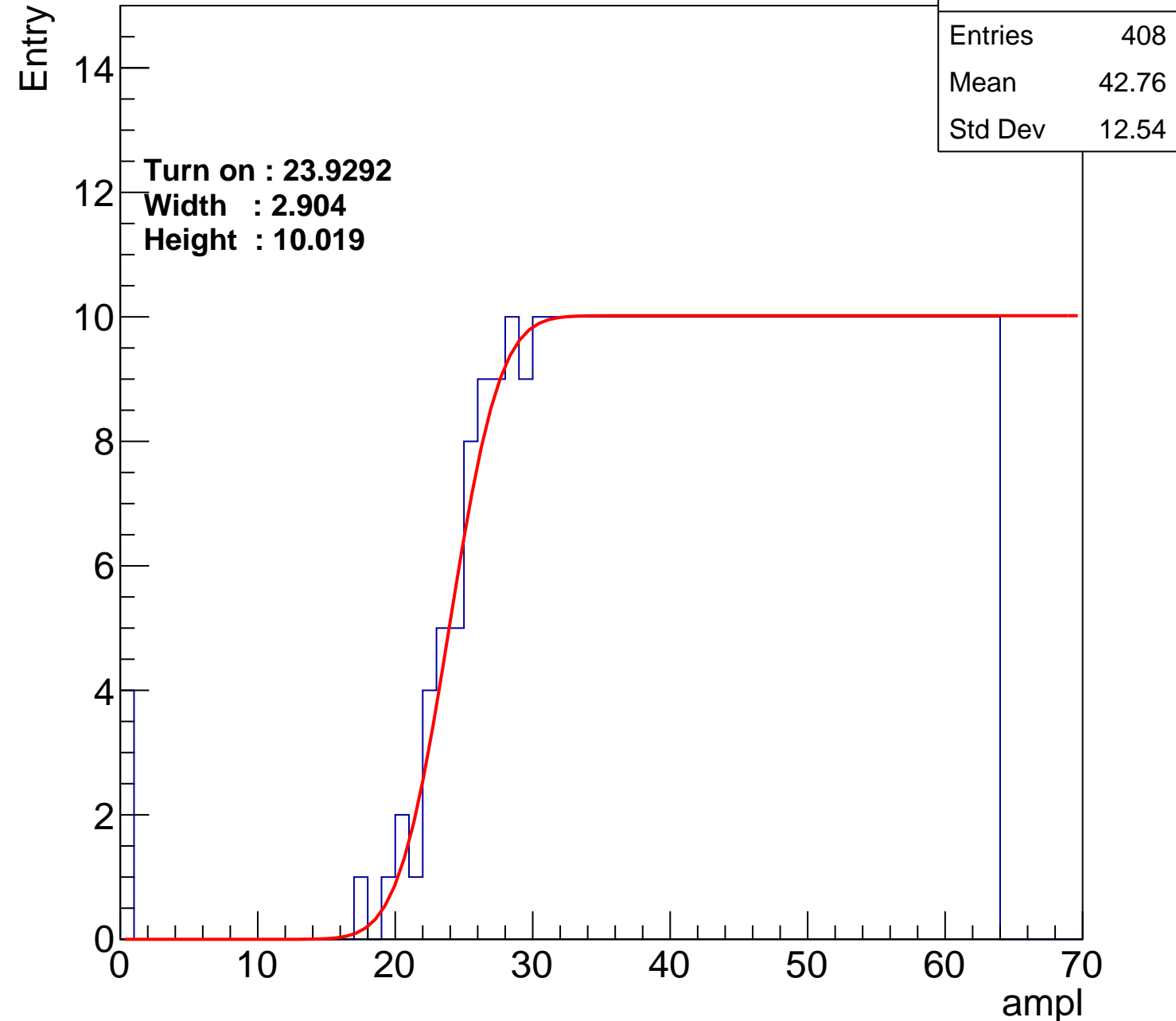
Width : 2.904

Height : 10.019

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U3-ch71

calib_packv5_042523_0143.root, FC#4, port A2

Entries	399
Mean	43.22
Std Dev	12.29

Turn on : 23.9616

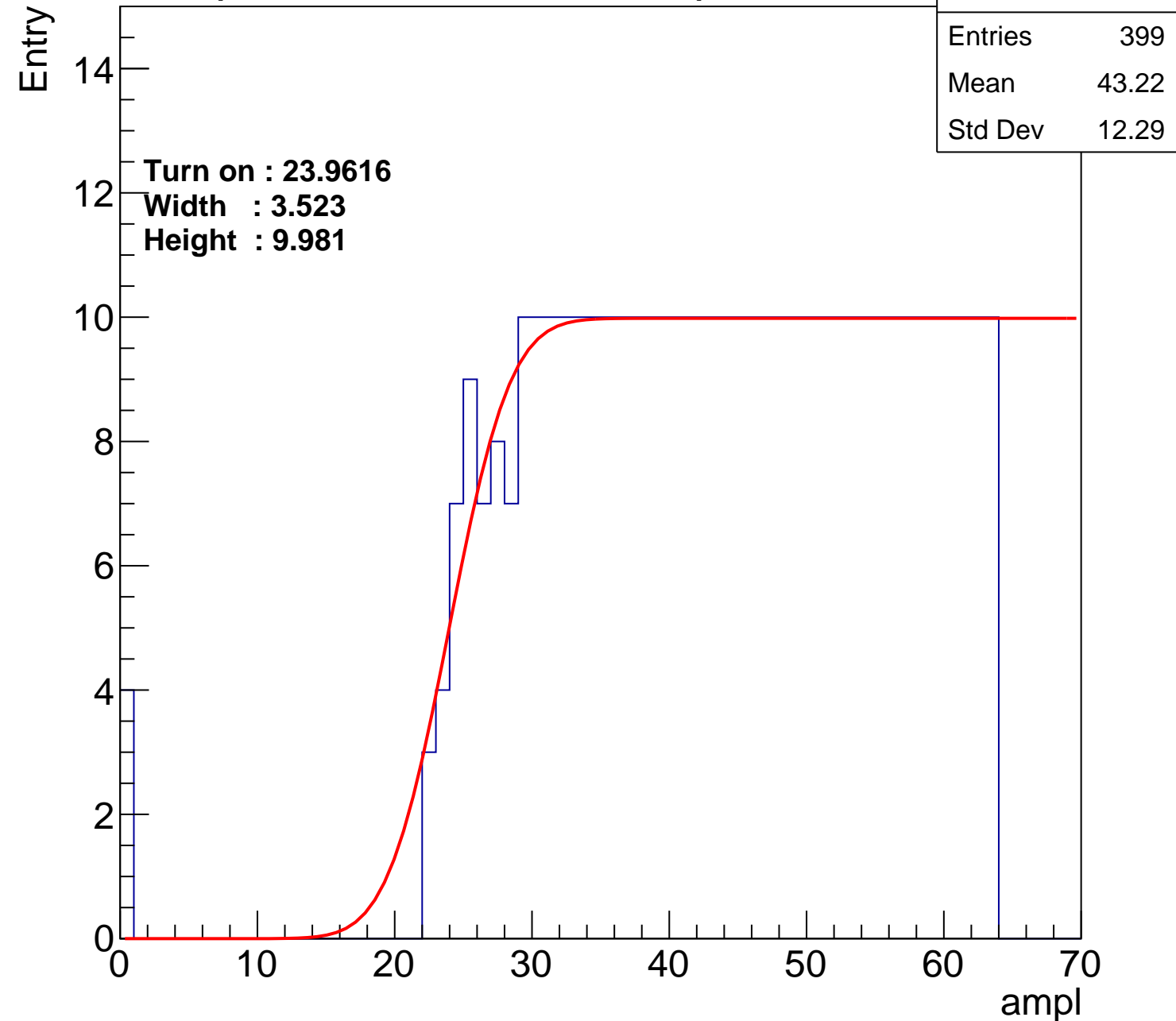
Width : 3.523

Height : 9.981

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U3-ch72

calib_packv5_042523_0143.root, FC#4, port A2

Entries	392
Mean	43.66
Std Dev	11.85

Turn on : 25.2460

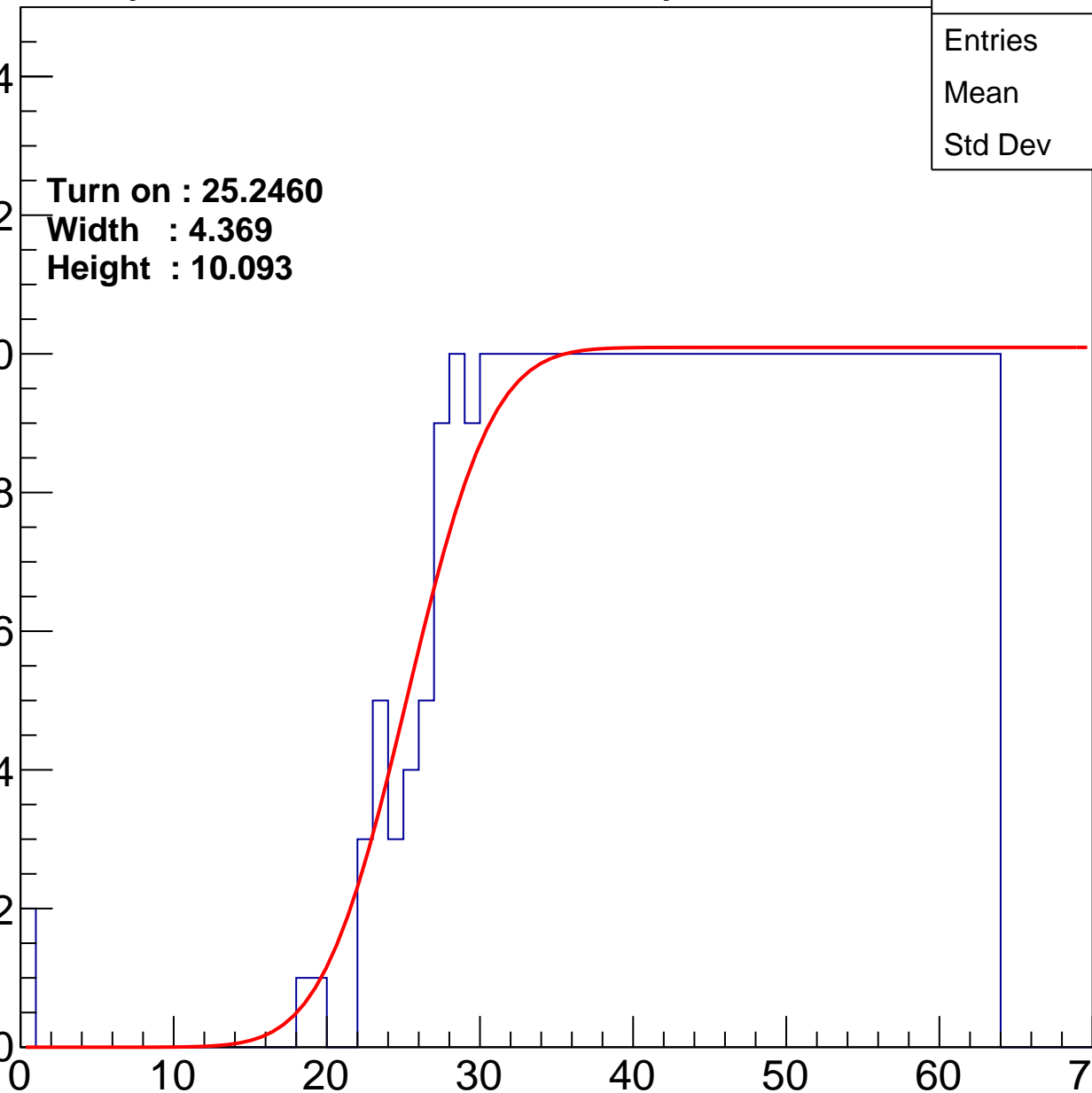
Width : 4.369

Height : 10.093

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U3-ch73

calib_packv5_042523_0143.root, FC#4, port A2

Entries	377
Mean	44.45
Std Dev	11.38

Turn on : 26.8705

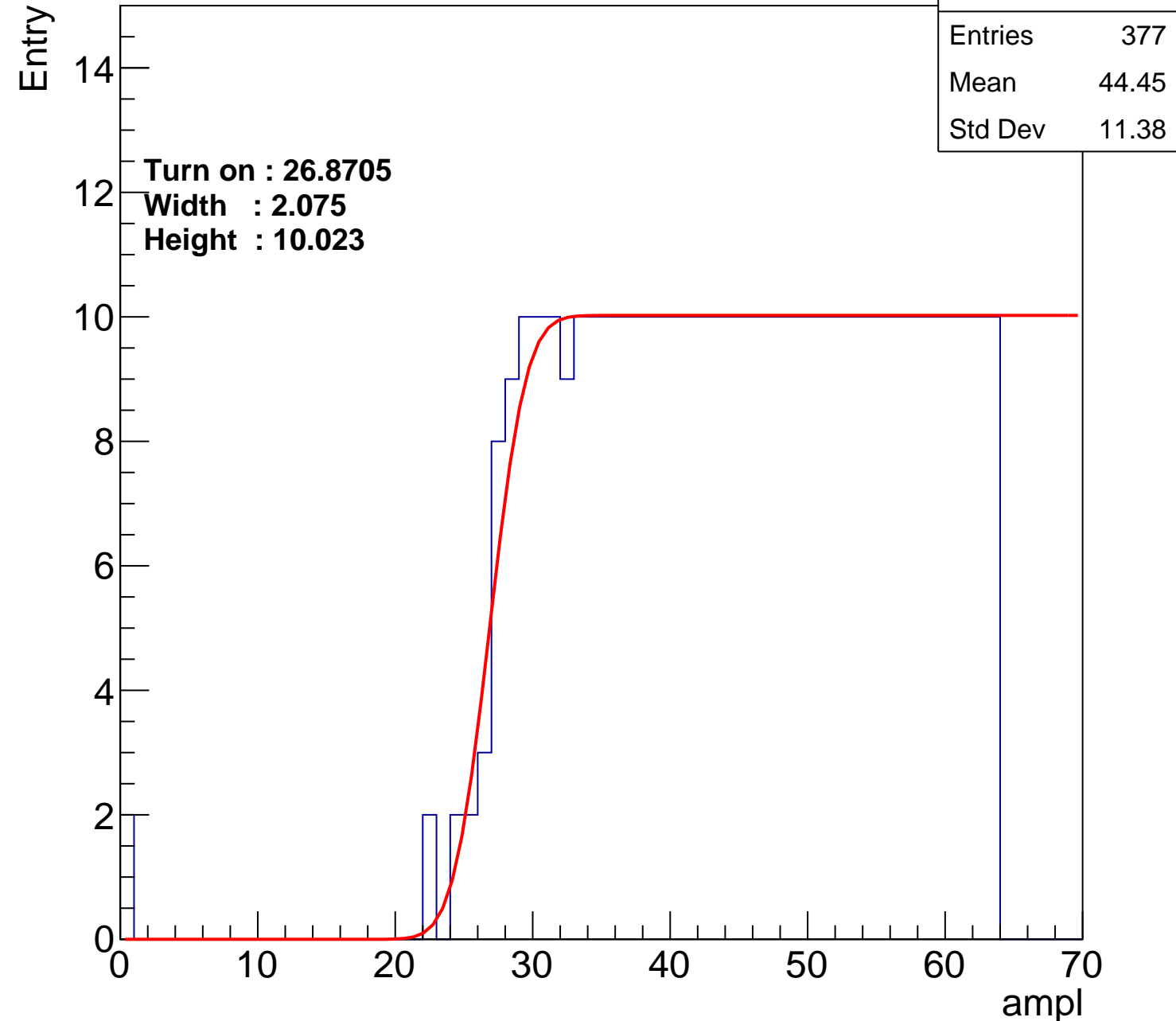
Width : 2.075

Height : 10.023

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U3-ch74

calib_packv5_042523_0143.root, FC#4, port A2

Entries	382
Mean	44.02
Std Dev	11.94

Turn on : 26.3821

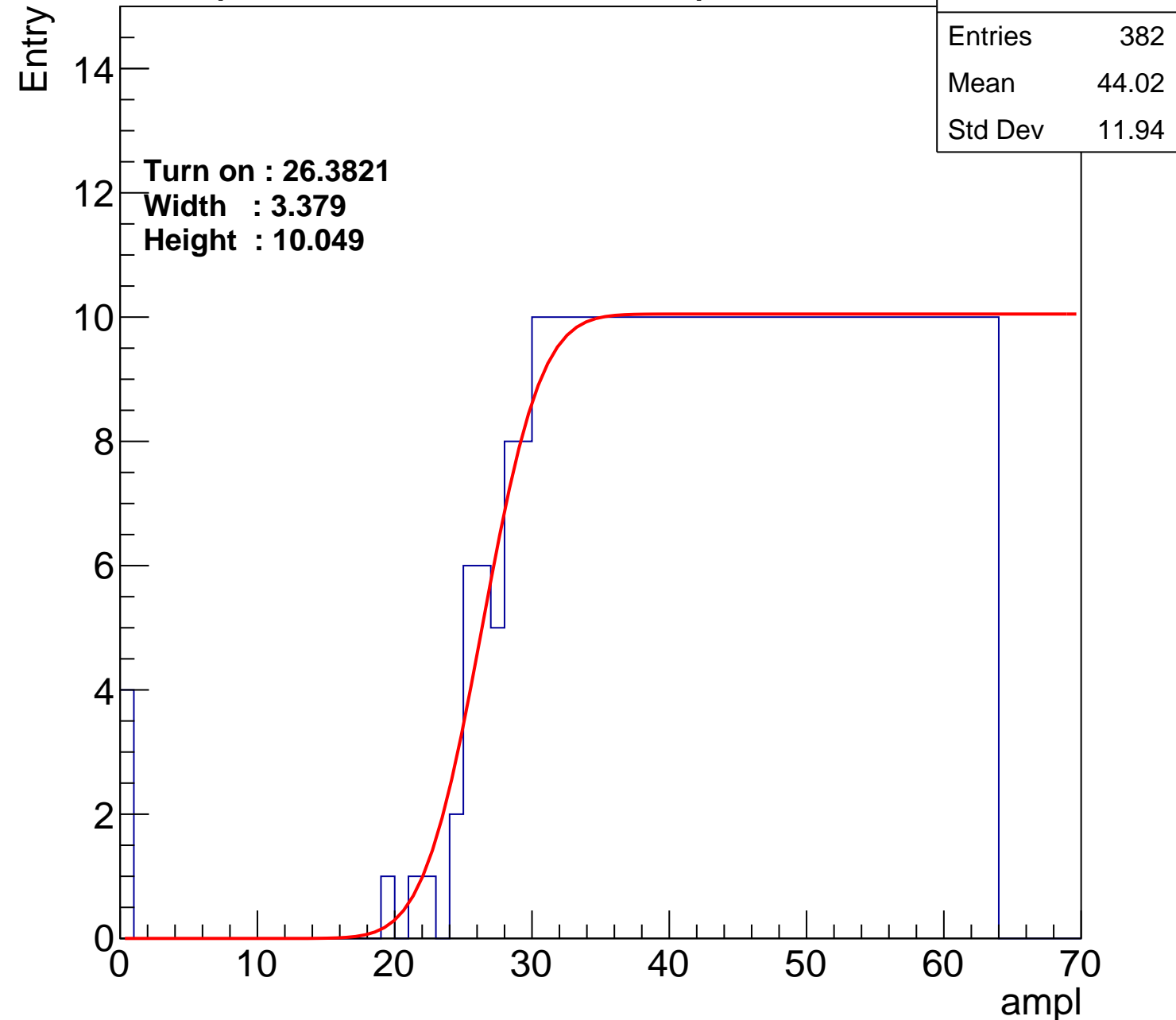
Width : 3.379

Height : 10.049

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U3-ch75

calib_packv5_042523_0143.root, FC#4, port A2

Entries	398
Mean	43.45
Std Dev	11.79

Turn on : 24.7022

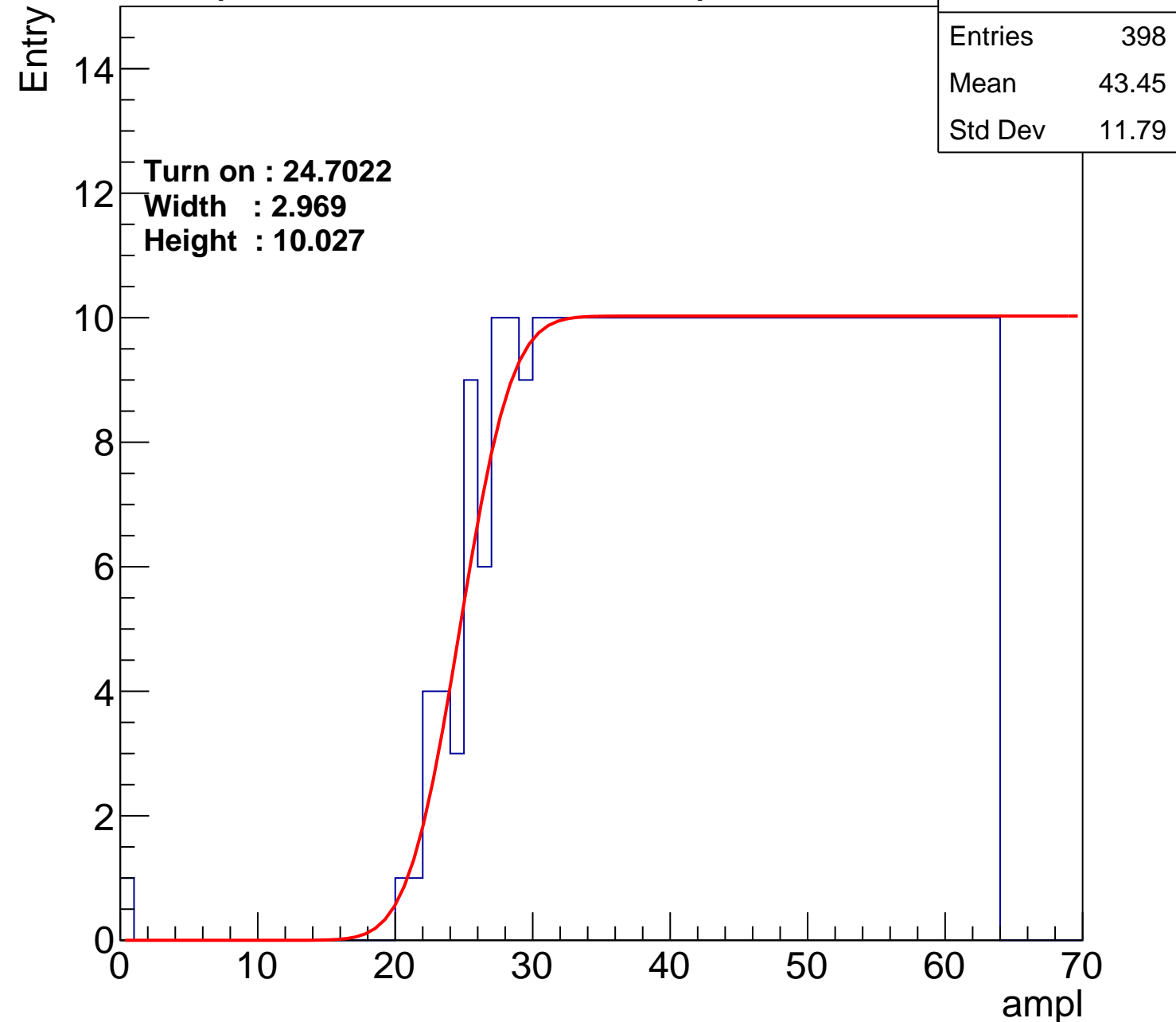
Width : 2.969

Height : 10.027

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U3-ch76

calib_packv5_042523_0143.root, FC#4, port A2

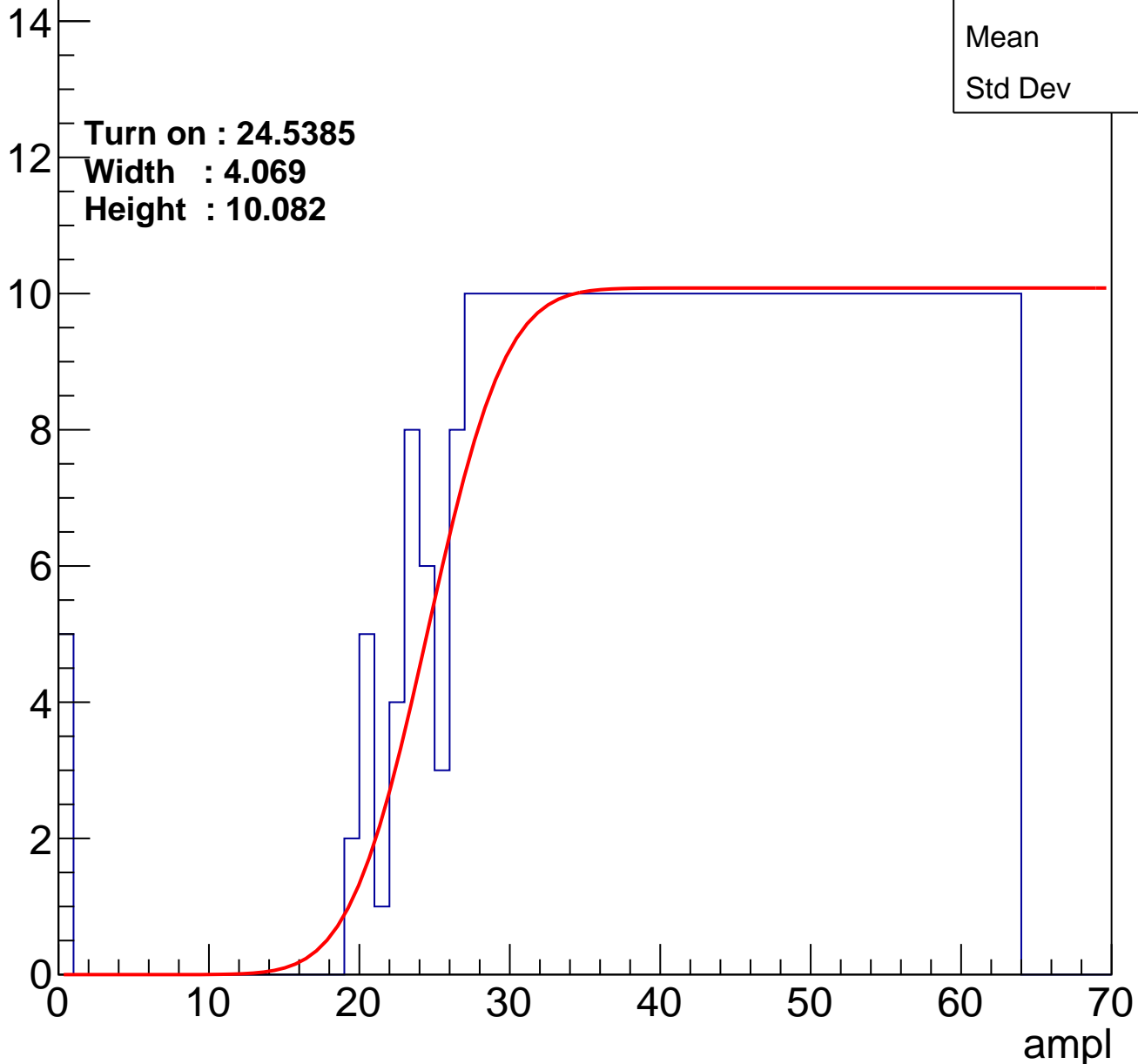
Entries	412
Mean	42.5
Std Dev	12.8

Turn on : 24.5385

Width : 4.069

Height : 10.082

Entry



B1L100S, U3-ch77

calib_packv5_042523_0143.root, FC#4, port A2

Entries	378
Mean	44.44
Std Dev	11.25

Turn on : 26.4463

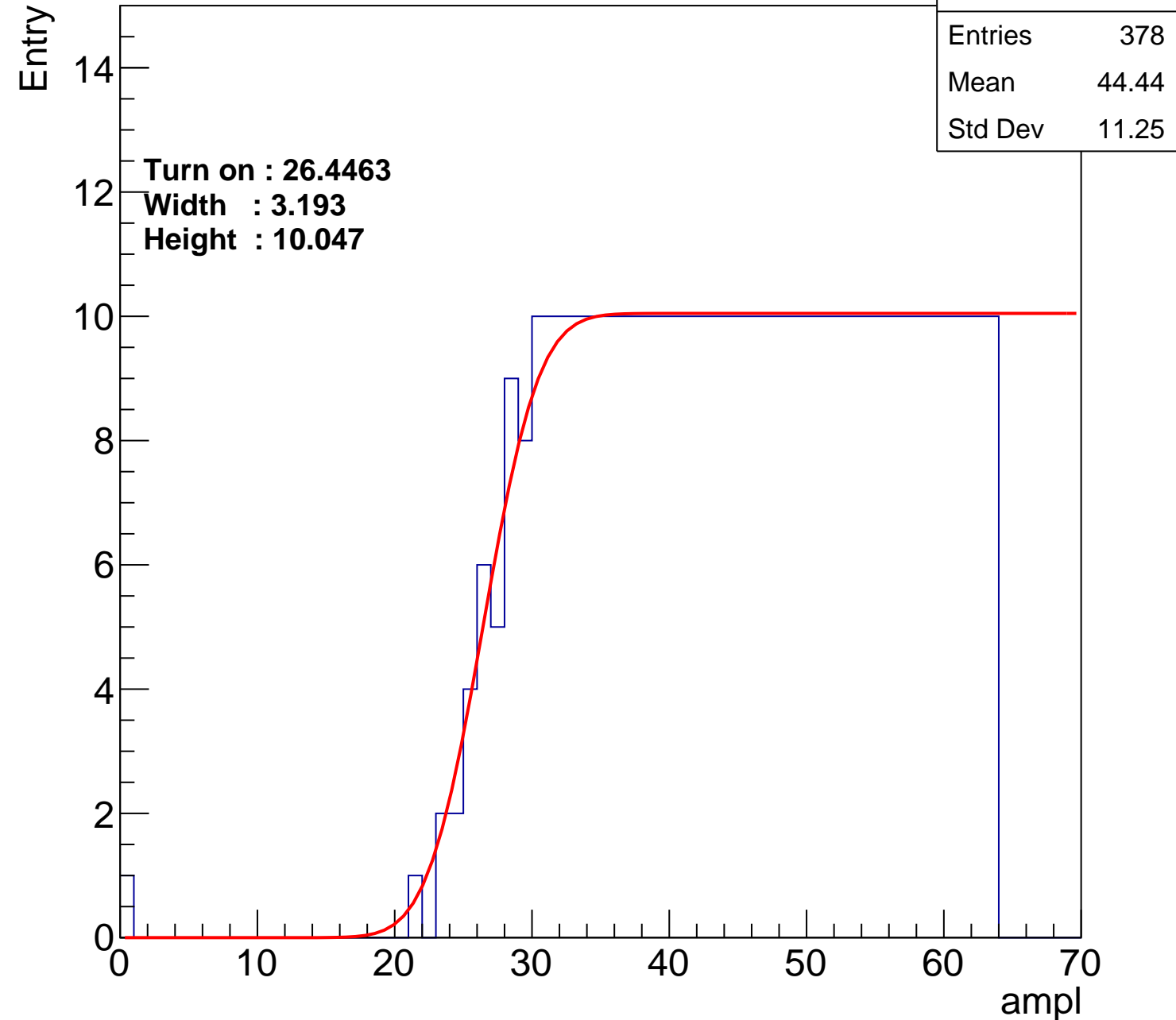
Width : 3.193

Height : 10.047

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U3-ch78

calib_packv5_042523_0143.root, FC#4, port A2

Entries	402
Mean	42.88
Std Dev	12.82

Turn on : 24.4924

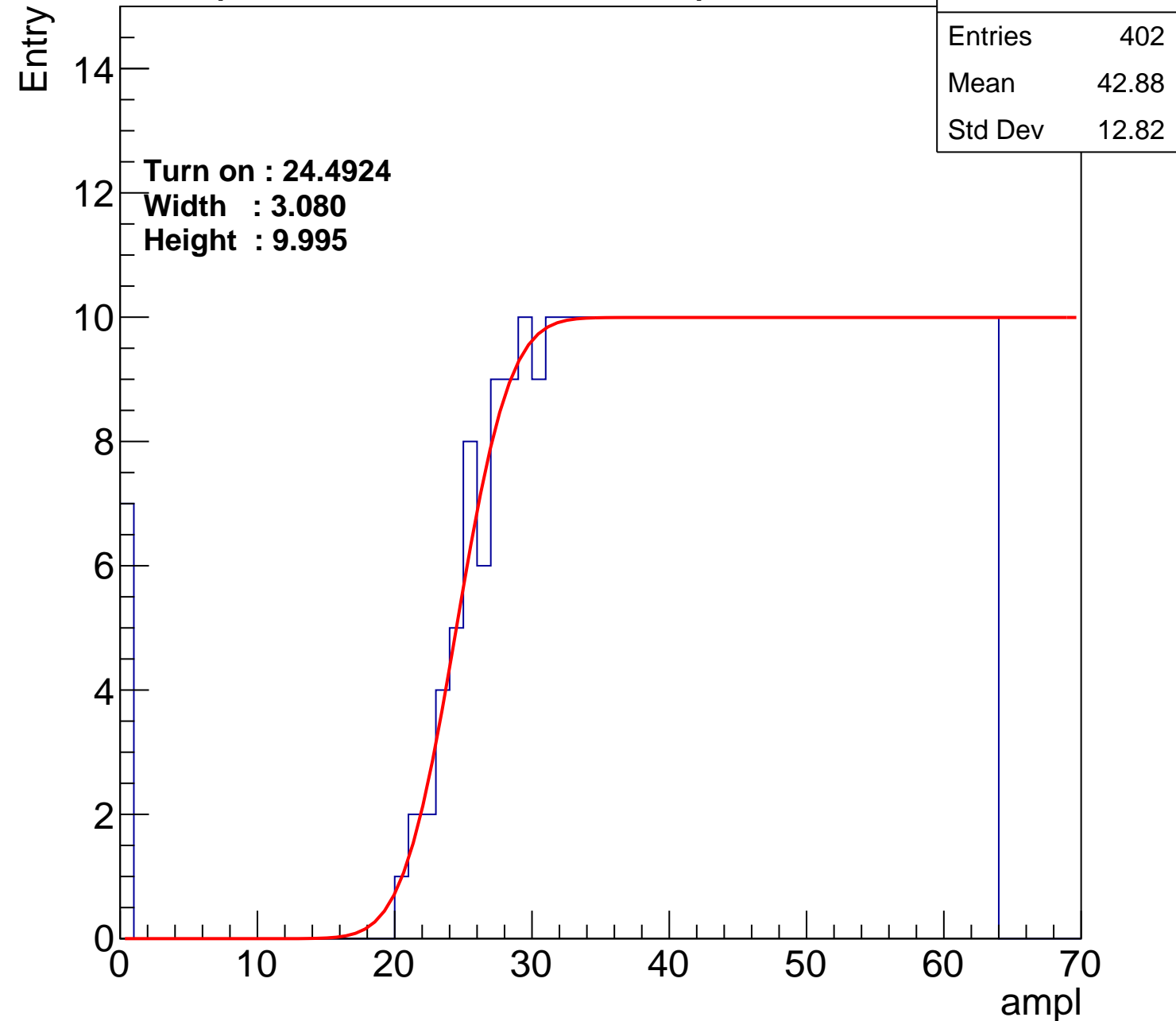
Width : 3.080

Height : 9.995

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U3-ch79

calib_packv5_042523_0143.root, FC#4, port A2

Entries	378
Mean	44.41
Std Dev	11.3

Turn on : 26.4877

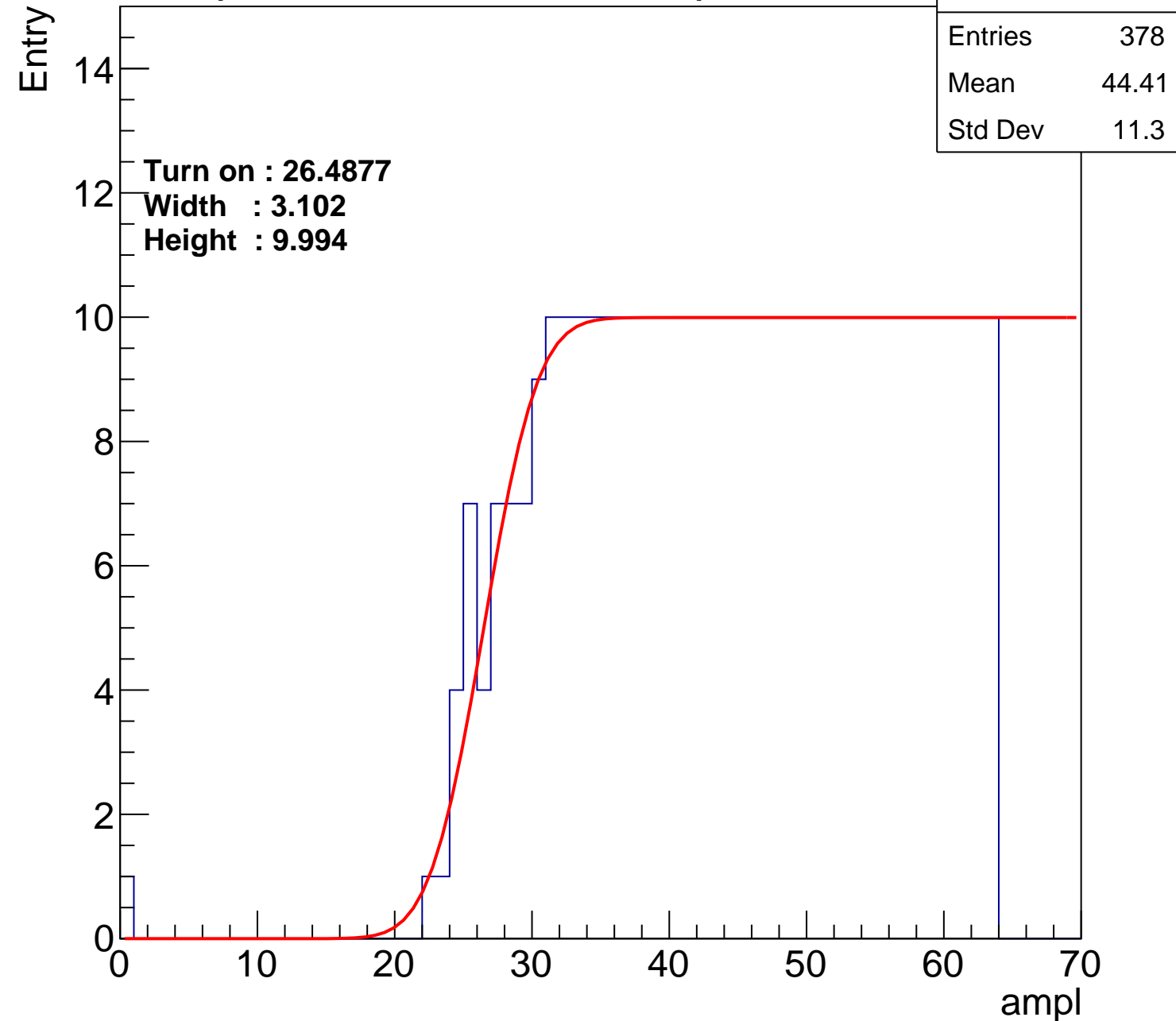
Width : 3.102

Height : 9.994

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U3-ch80

calib_packv5_042523_0143.root, FC#4, port A2

Entries	381
Mean	44.16
Std Dev	11.62

Turn on : 25.7637

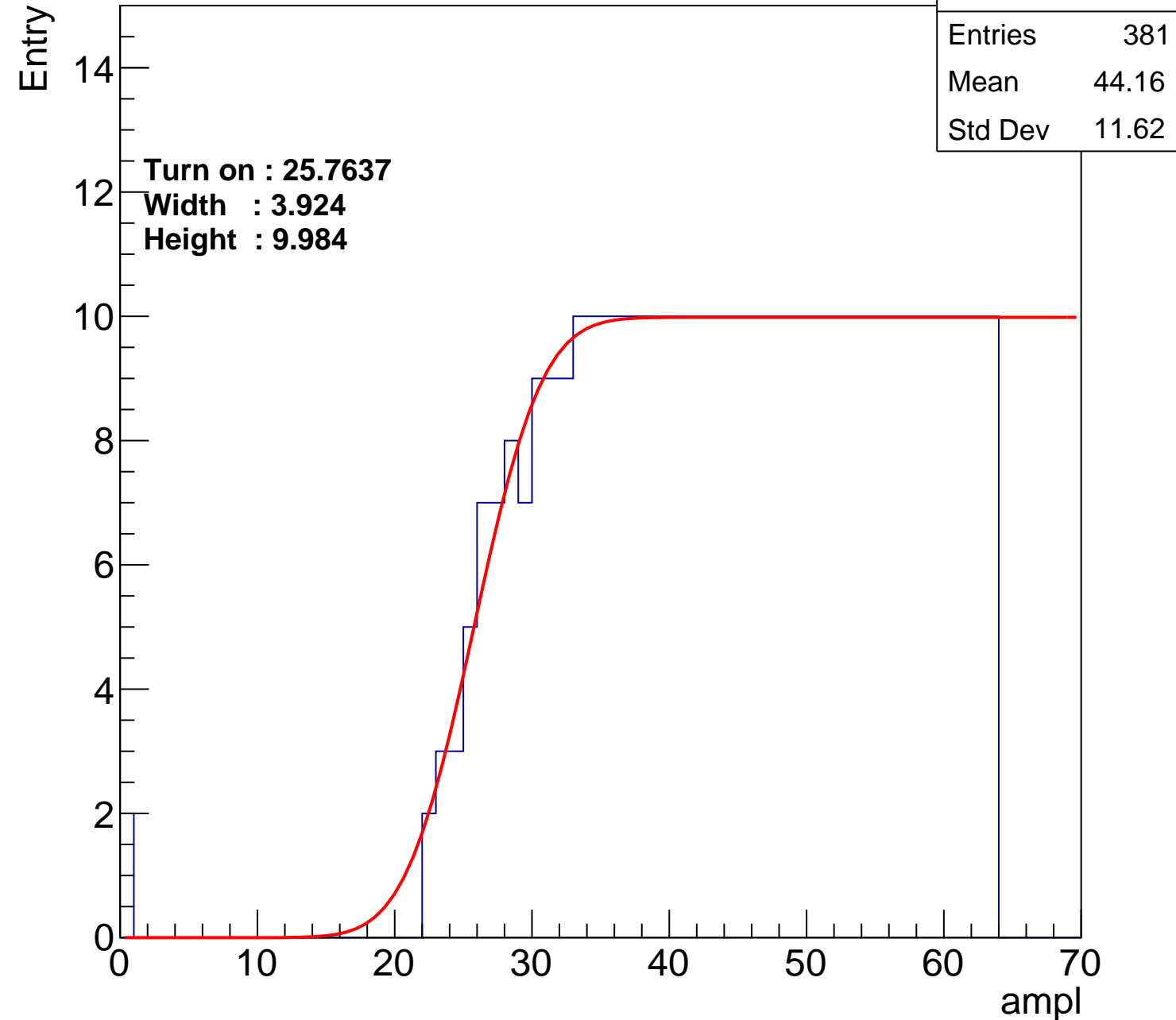
Width : 3.924

Height : 9.984

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U3-ch81

calib_packv5_042523_0143.root, FC#4, port A2

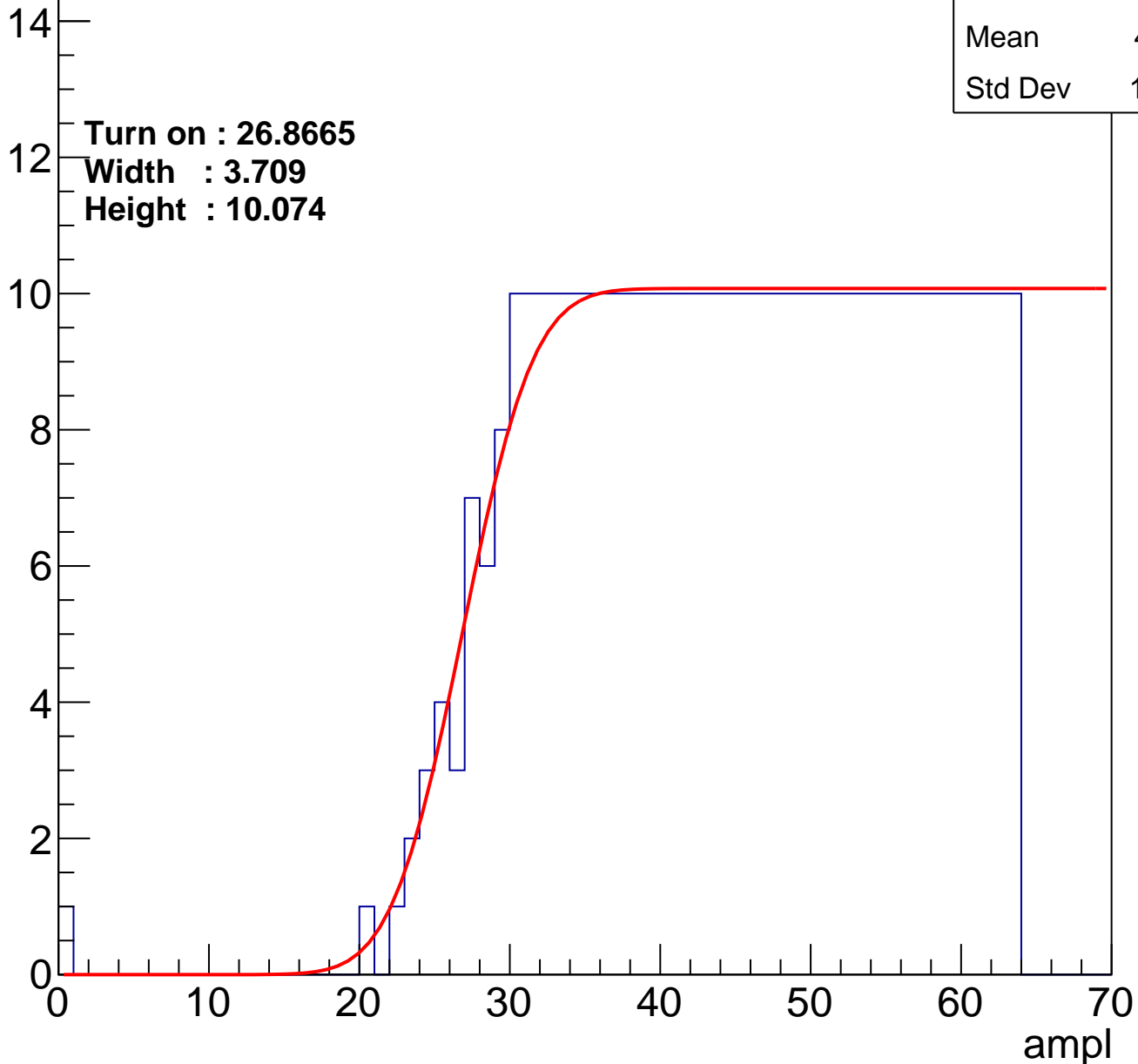
Entries	376
Mean	44.51
Std Dev	11.25

Turn on : 26.8665

Width : 3.709

Height : 10.074

Entry



B1L100S, U3-ch82

calib_packv5_042523_0143.root, FC#4, port A2

Entries	373
Mean	44.65
Std Dev	11.28

Turn on : 27.0311

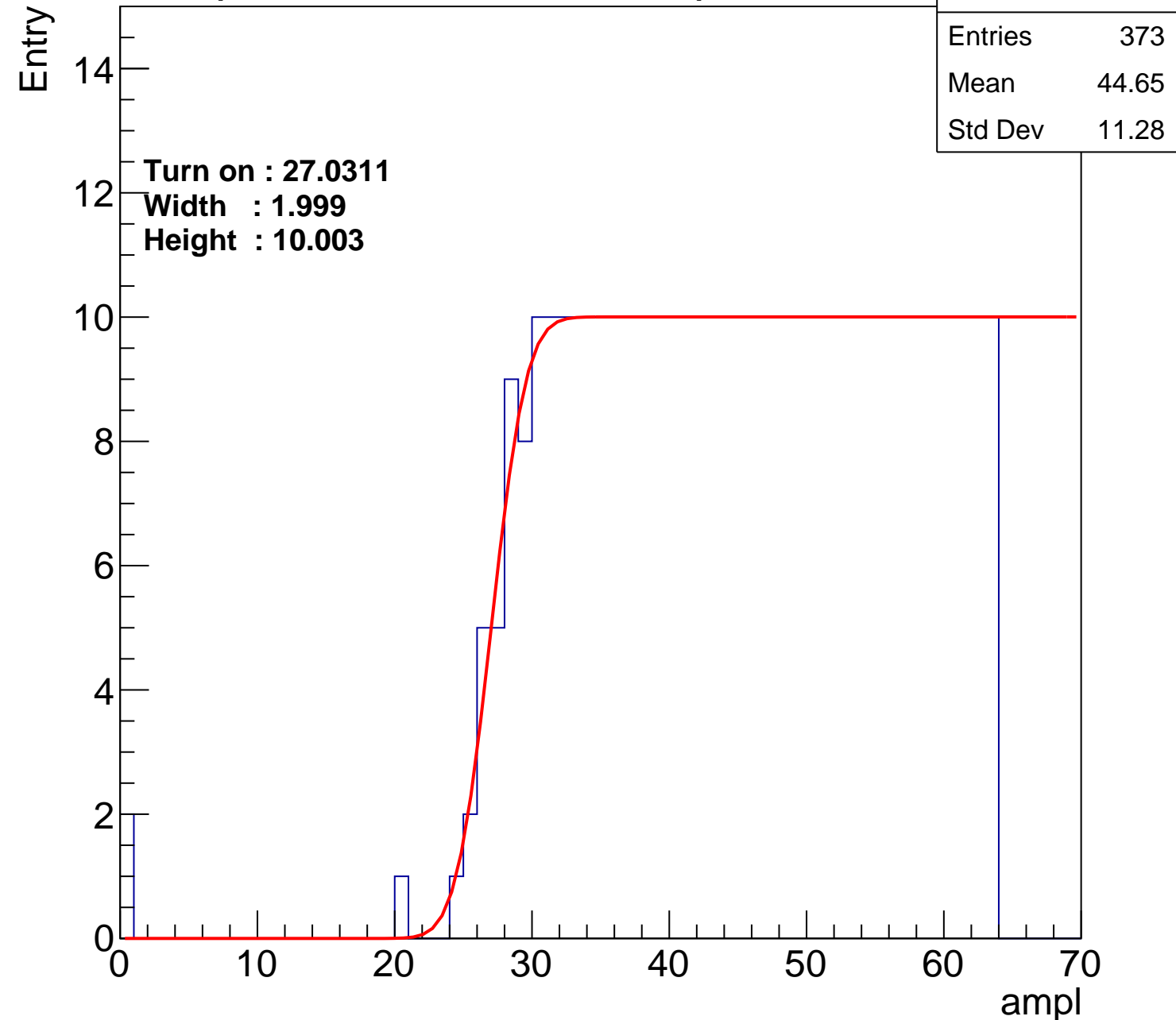
Width : 1.999

Height : 10.003

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U3-ch83

calib_packv5_042523_0143.root, FC#4, port A2

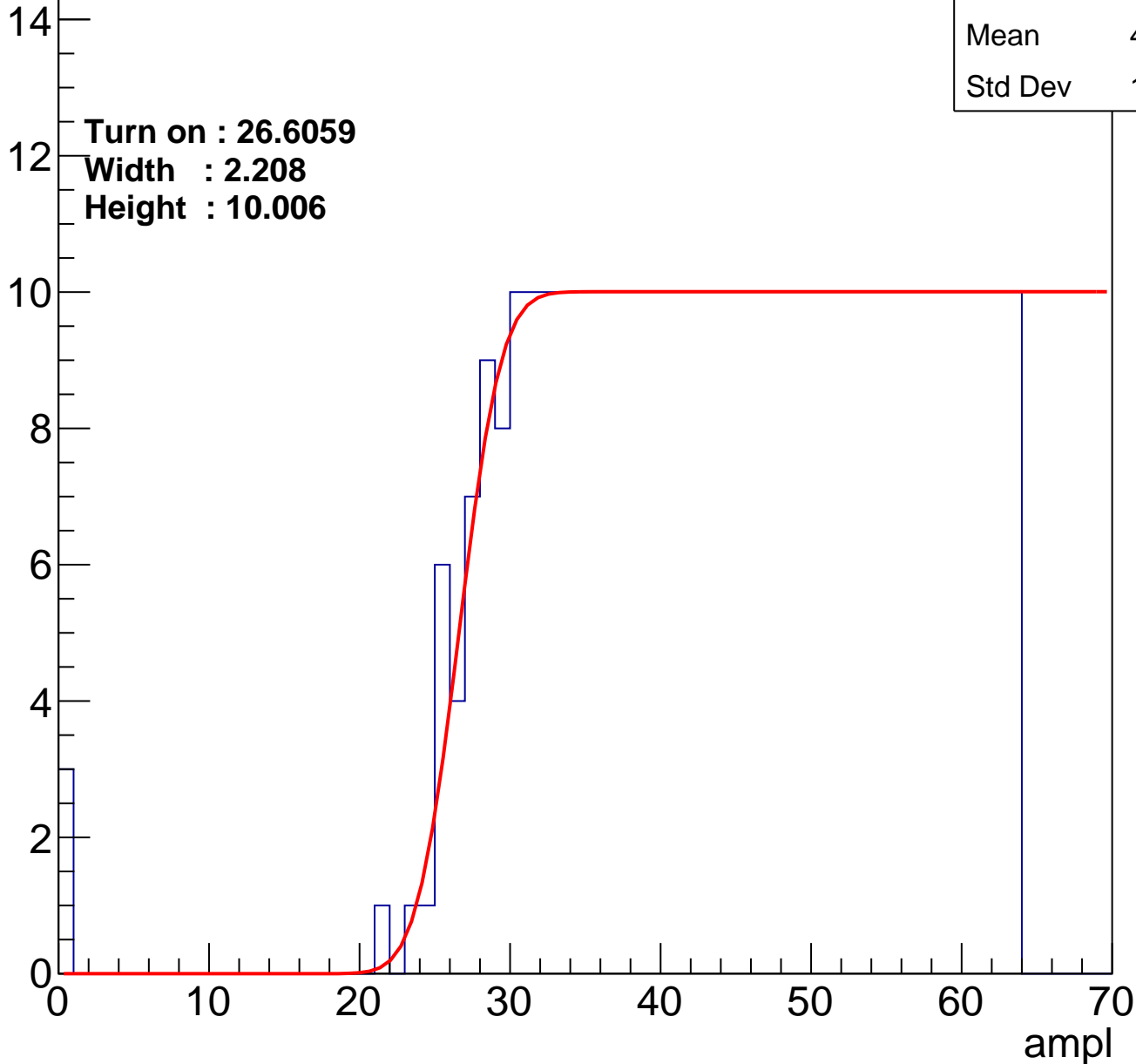
Entries	380
Mean	44.22
Std Dev	11.65

Turn on : 26.6059

Width : 2.208

Height : 10.006

Entry



B1L100S, U3-ch84

calib_packv5_042523_0143.root, FC#4, port A2

Entries	380
Mean	44.27
Std Dev	11.5

Turn on : 26.3371

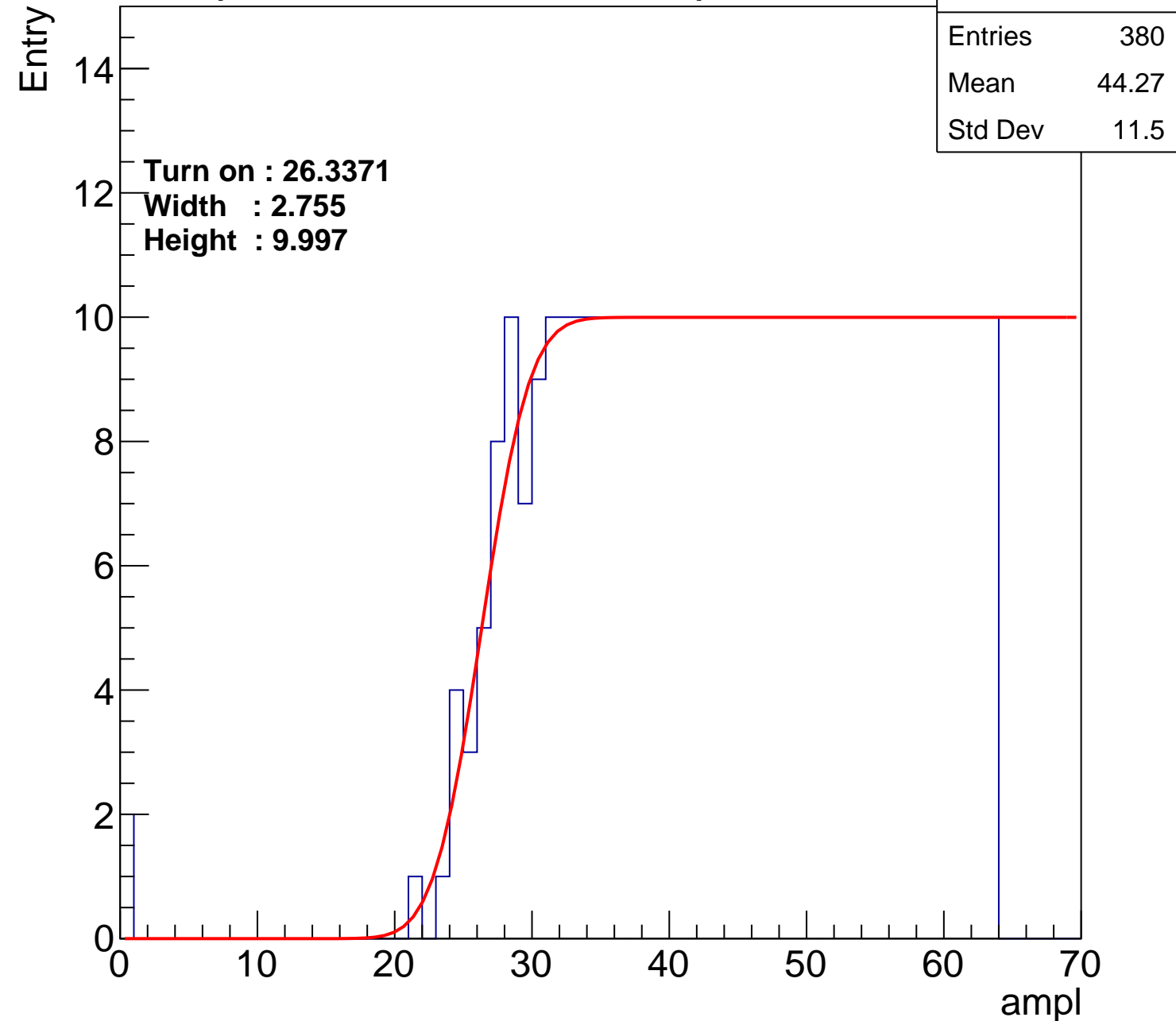
Width : 2.755

Height : 9.997

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U3-ch85

calib_packv5_042523_0143.root, FC#4, port A2

Entries	393
Mean	43.46
Std Dev	12.24

Turn on : 25.7226

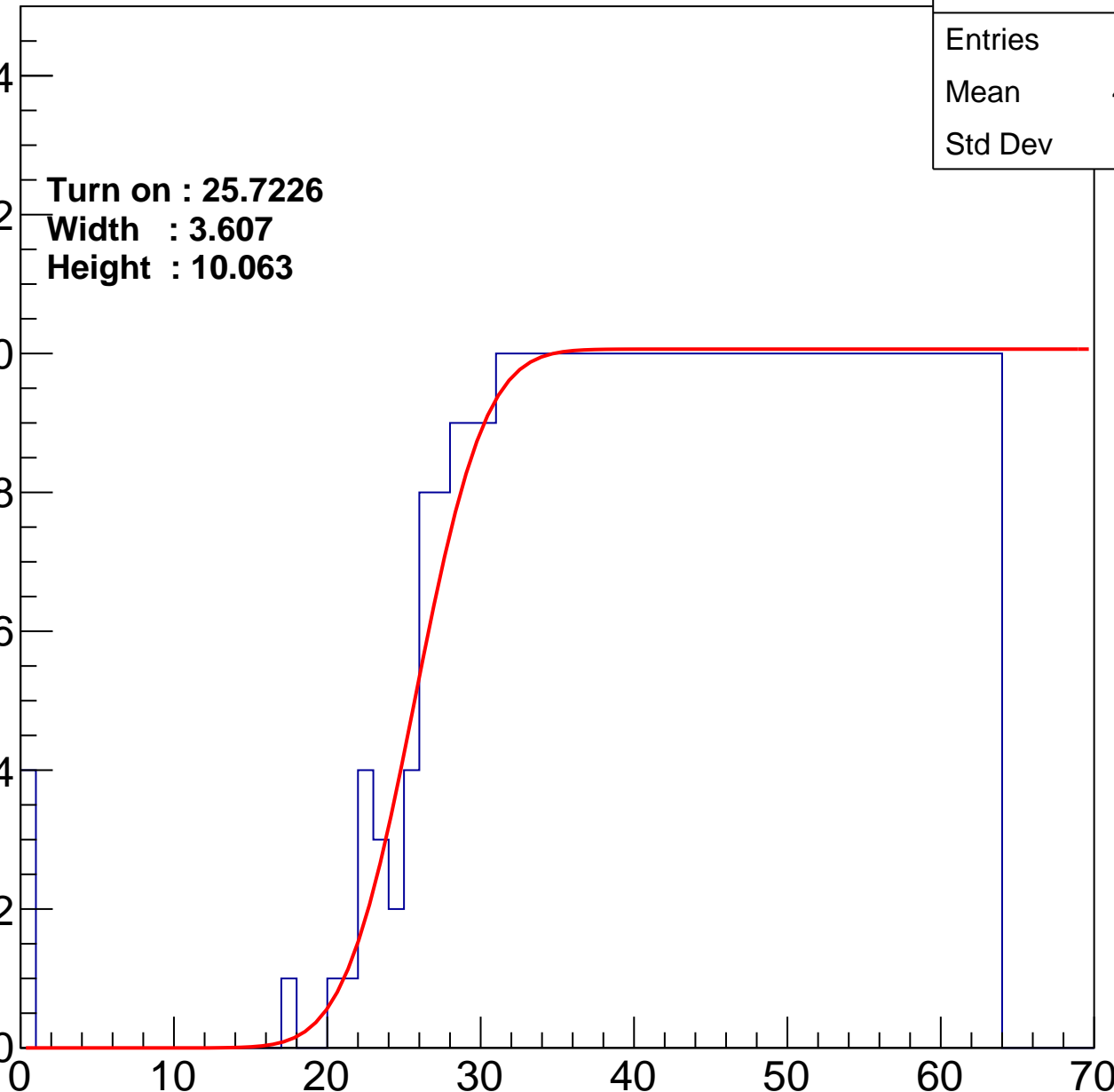
Width : 3.607

Height : 10.063

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U3-ch86

calib_packv5_042523_0143.root, FC#4, port A2

Entries	382
Mean	44.09
Std Dev	11.76

Turn on : 26.5713

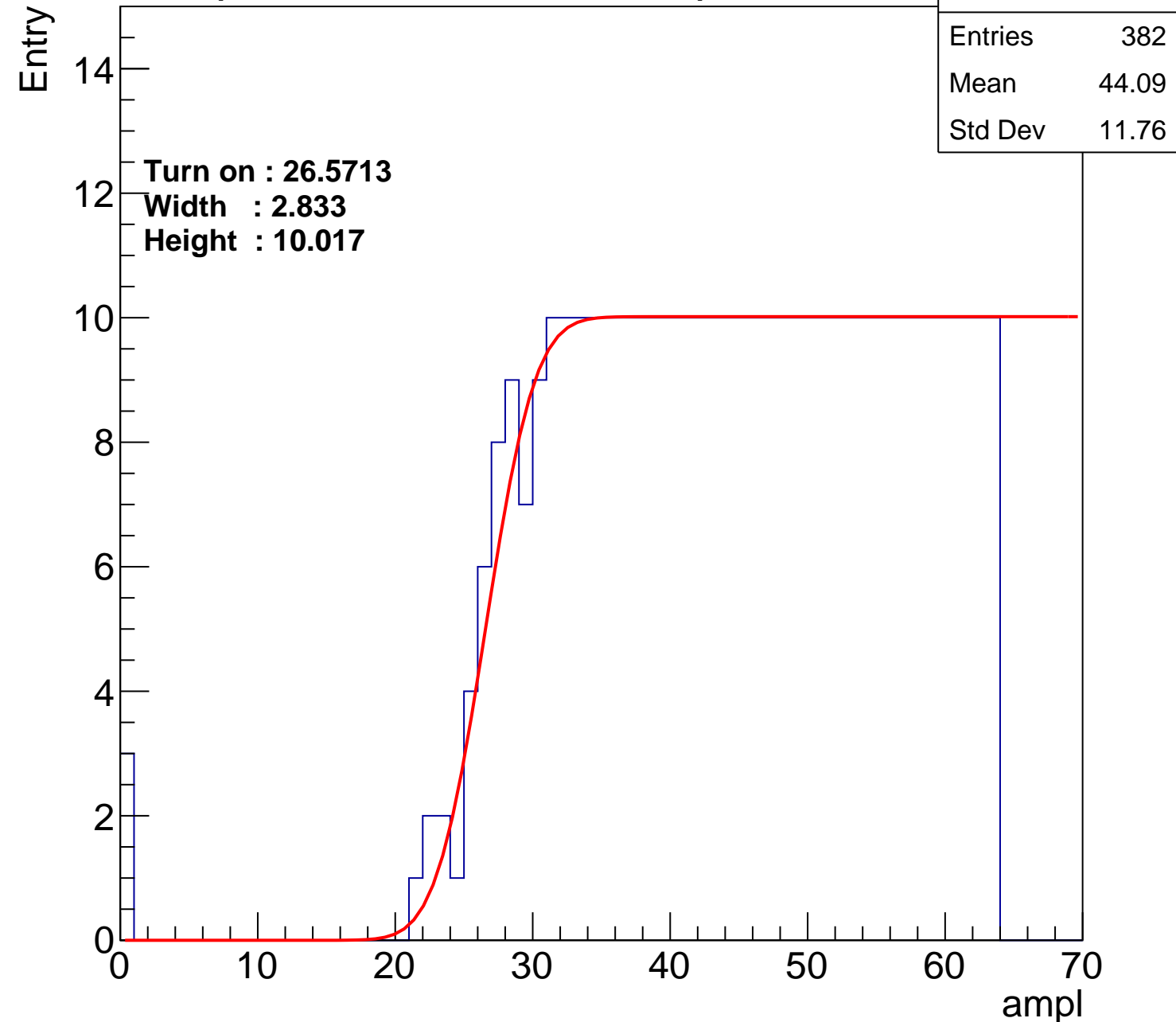
Width : 2.833

Height : 10.017

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U3-ch87

calib_packv5_042523_0143.root, FC#4, port A2

Entries	371
Mean	44.37
Std Dev	12.11

Turn on : 27.4922

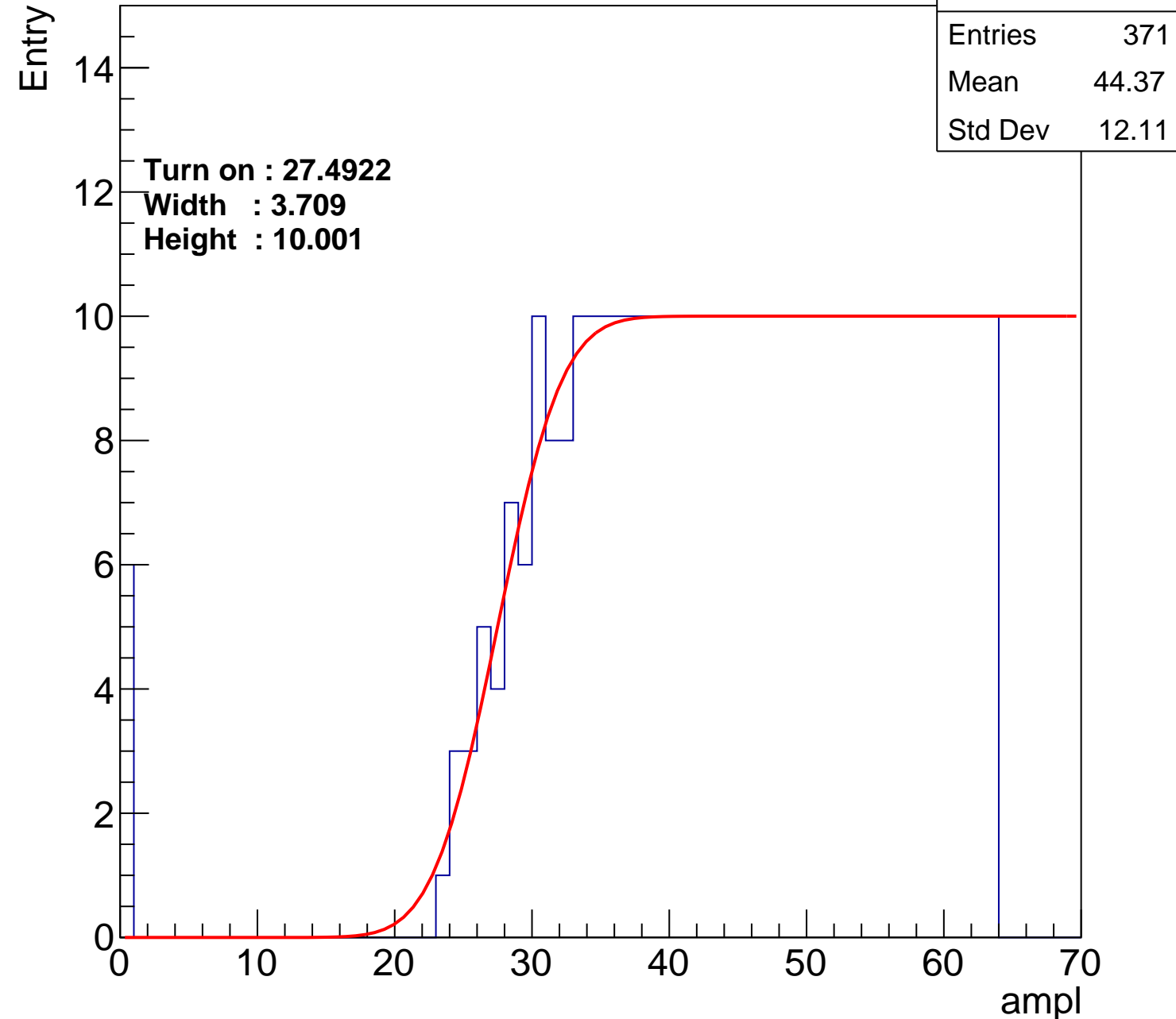
Width : 3.709

Height : 10.001

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U3-ch88

calib_packv5_042523_0143.root, FC#4, port A2

Entries	388
Mean	43.95
Std Dev	11.53

Turn on : 25.7557

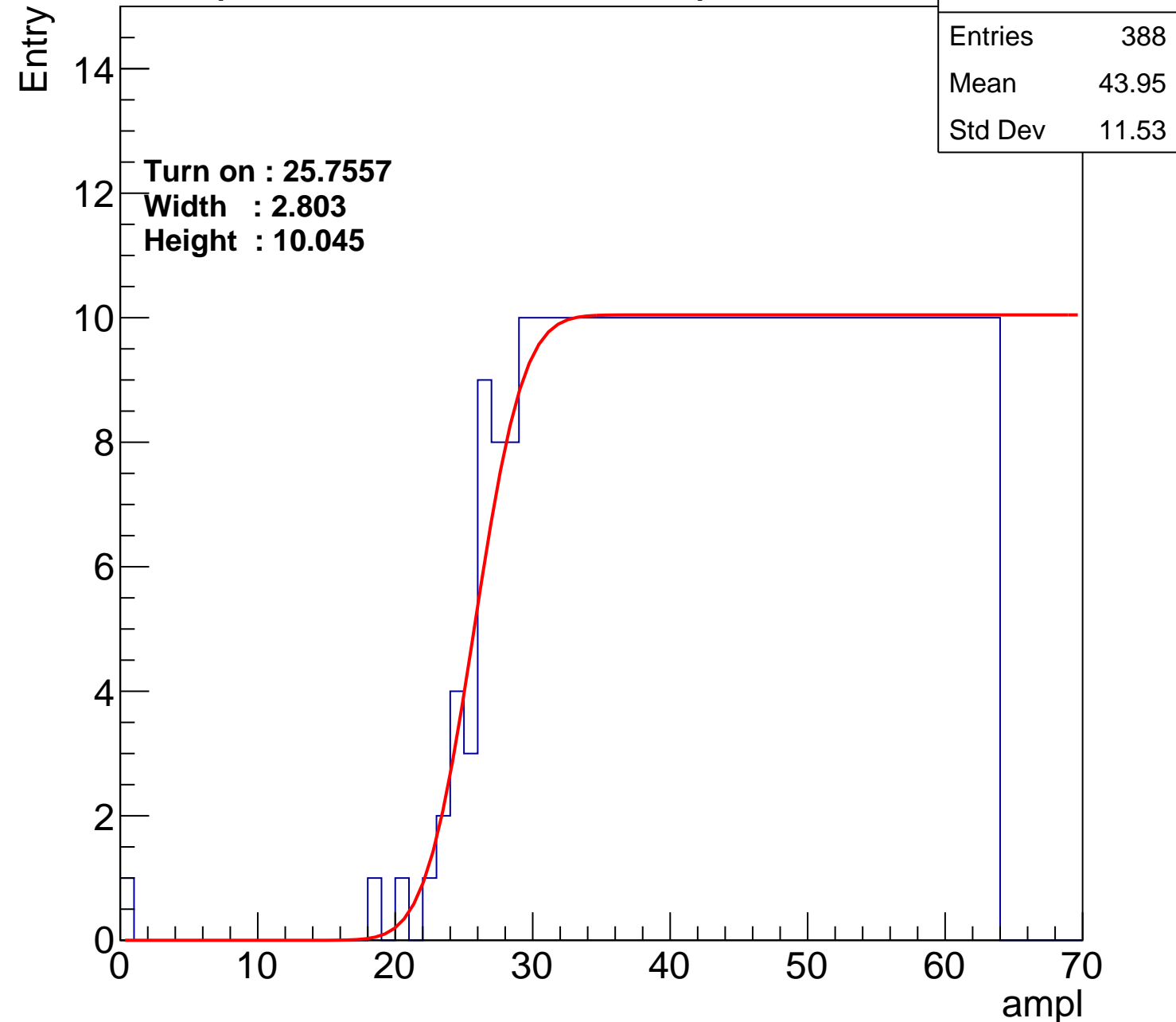
Width : 2.803

Height : 10.045

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U3-ch89

calib_packv5_042523_0143.root, FC#4, port A2

Entries	392
Mean	43.48
Std Dev	12.32

Turn on : 25.4634

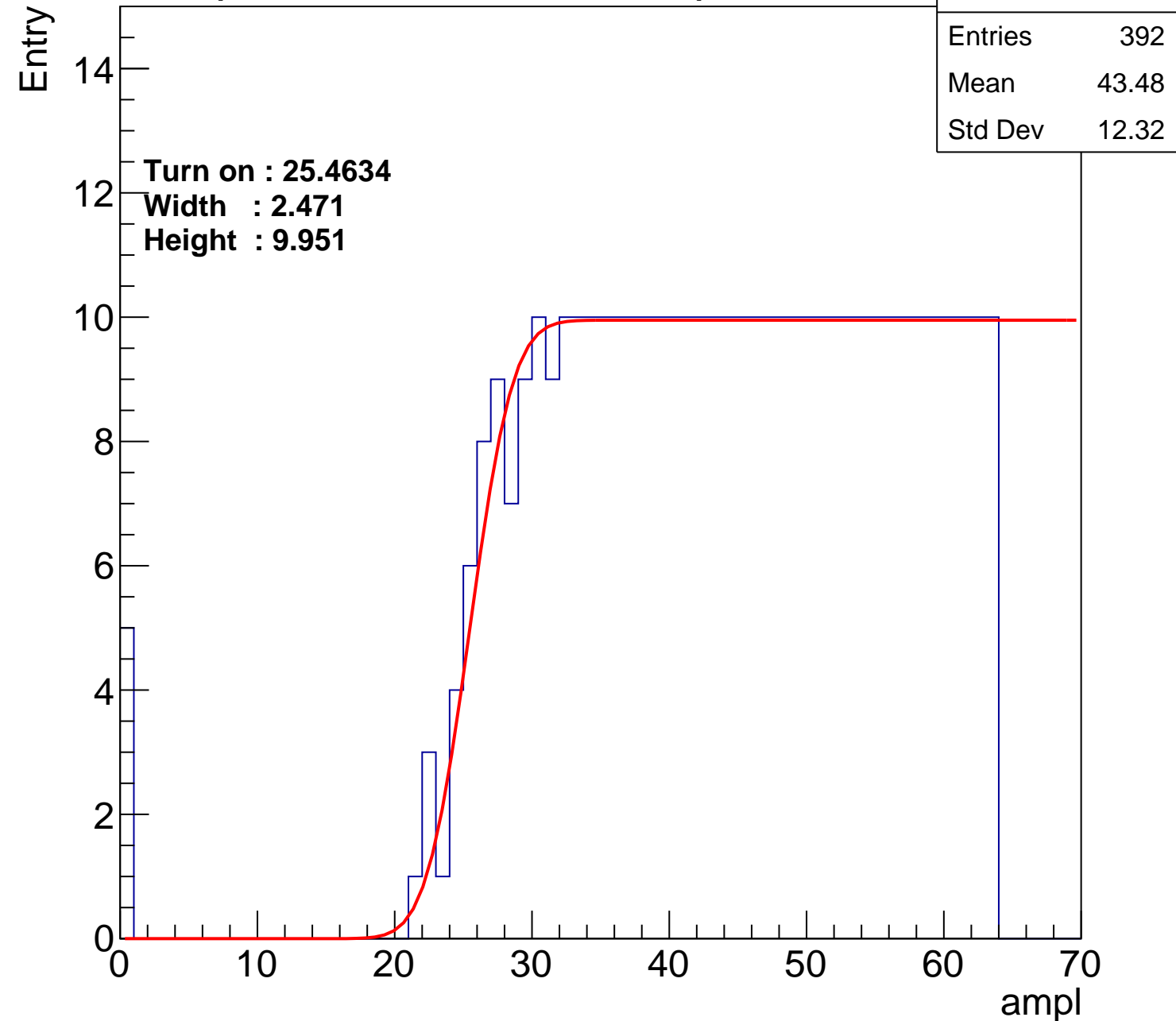
Width : 2.471

Height : 9.951

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U3-ch90

calib_packv5_042523_0143.root, FC#4, port A2

Entries	381
Mean	44.19
Std Dev	11.6

Turn on : 26.7436

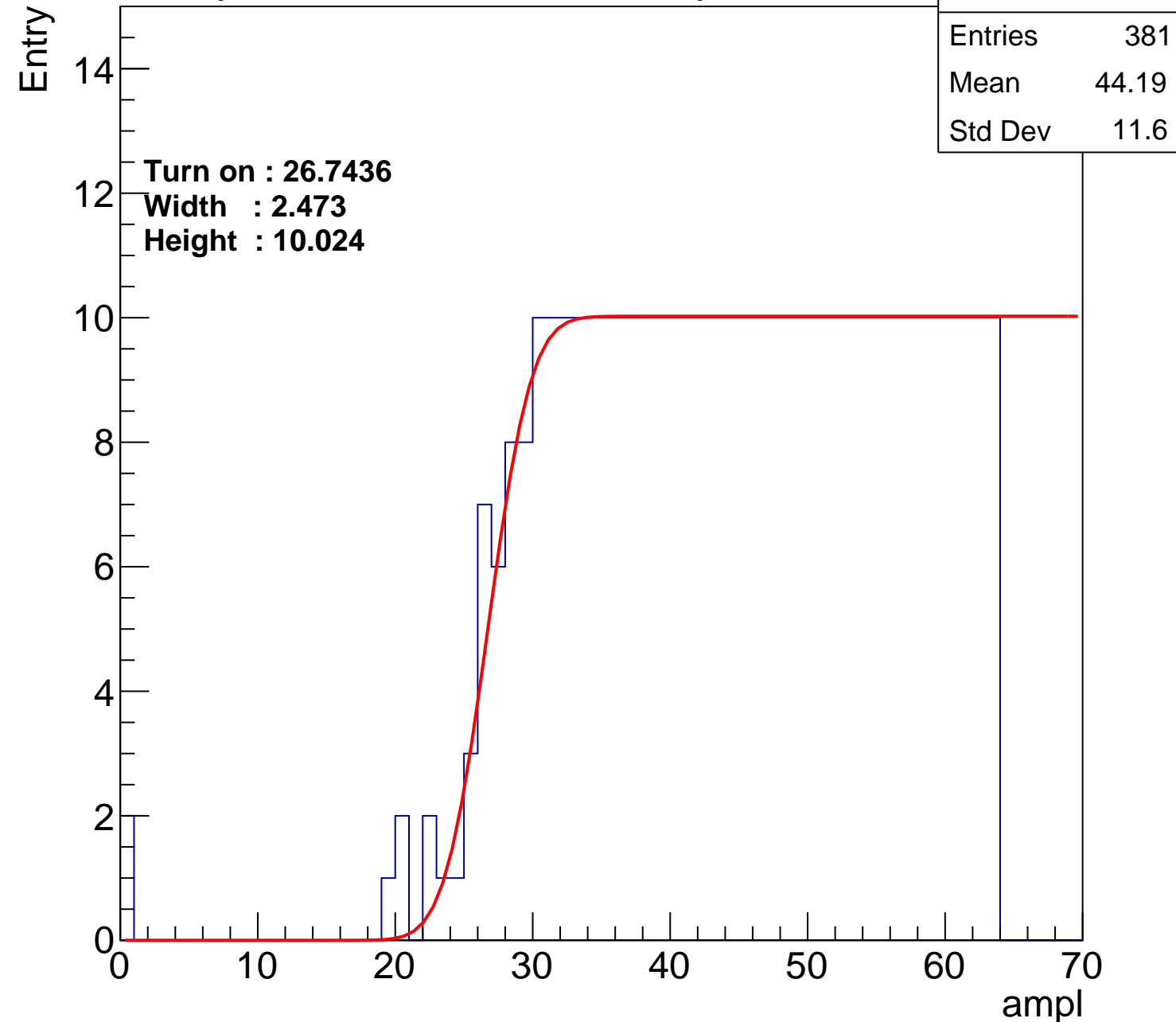
Width : 2.473

Height : 10.024

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U3-ch91

calib_packv5_042523_0143.root, FC#4, port A2

Entries	362
Mean	45.15
Std Dev	11.04

Turn on : 27.9636

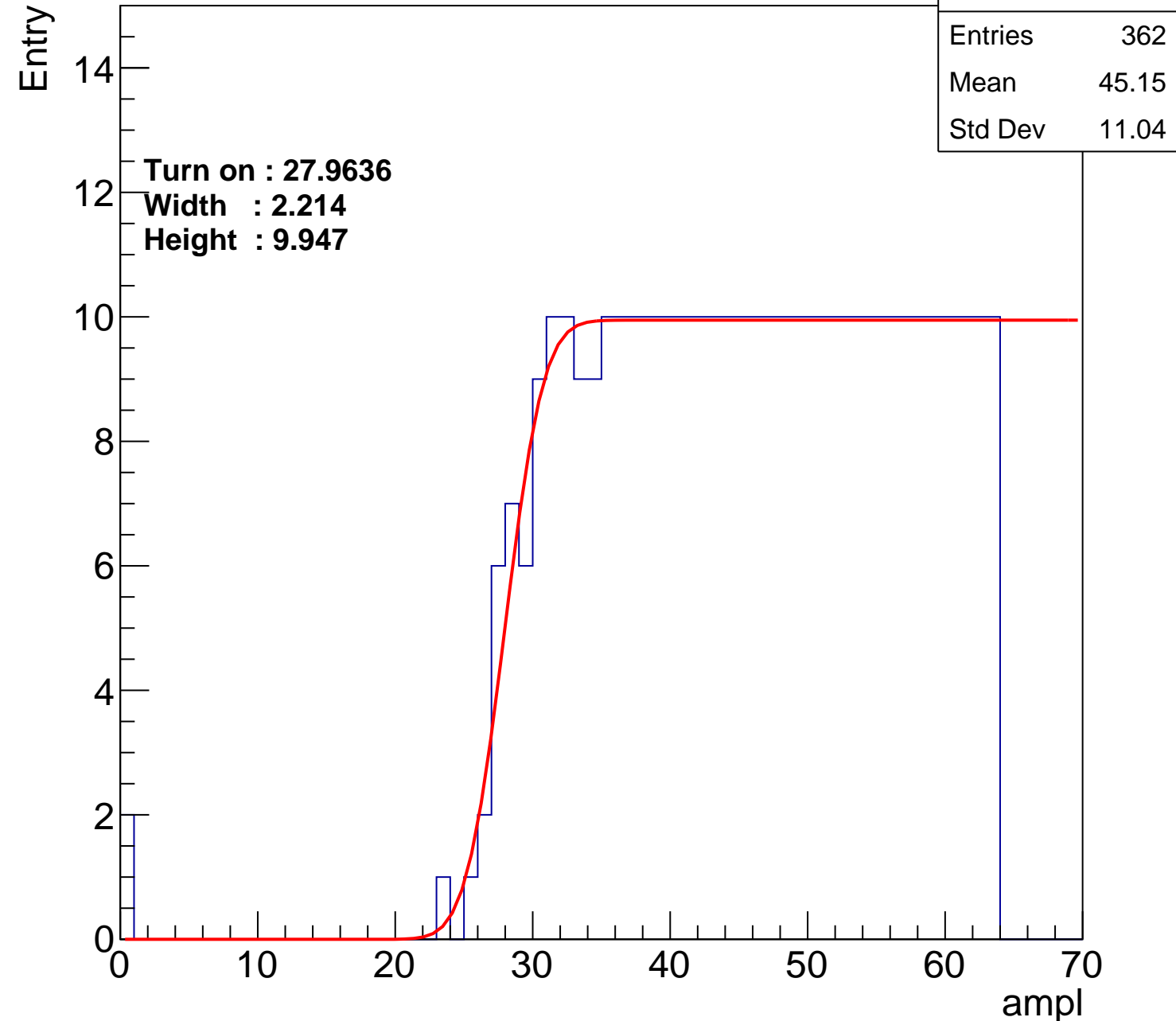
Width : 2.214

Height : 9.947

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U3-ch92

calib_packv5_042523_0143.root, FC#4, port A2

Entries	381
Mean	44.16
Std Dev	11.7

Turn on : 25.6250

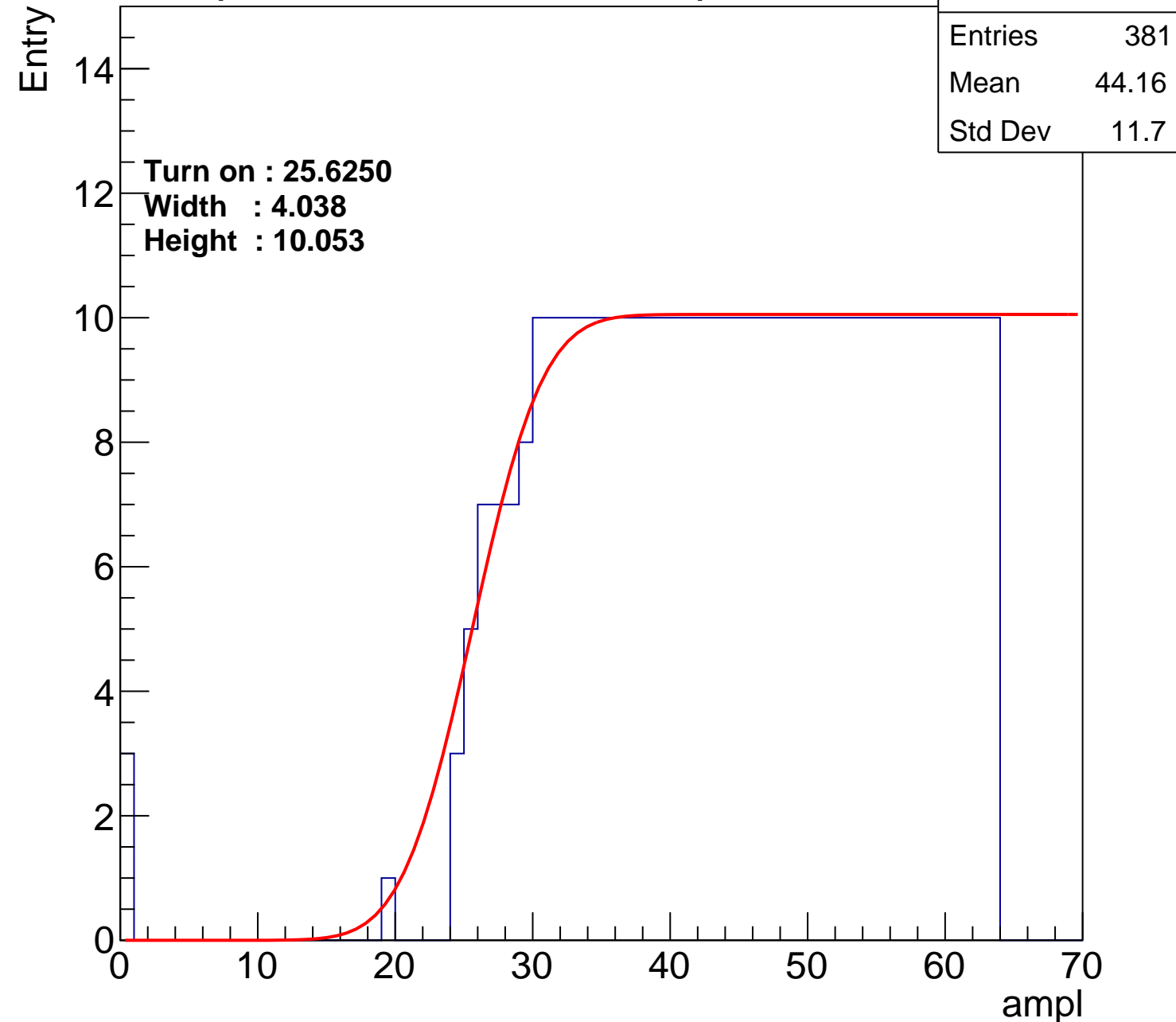
Width : 4.038

Height : 10.053

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U3-ch93

calib_packv5_042523_0143.root, FC#4, port A2

Entries	386
Mean	43.72
Std Dev	12.33

Turn on : 26.3547

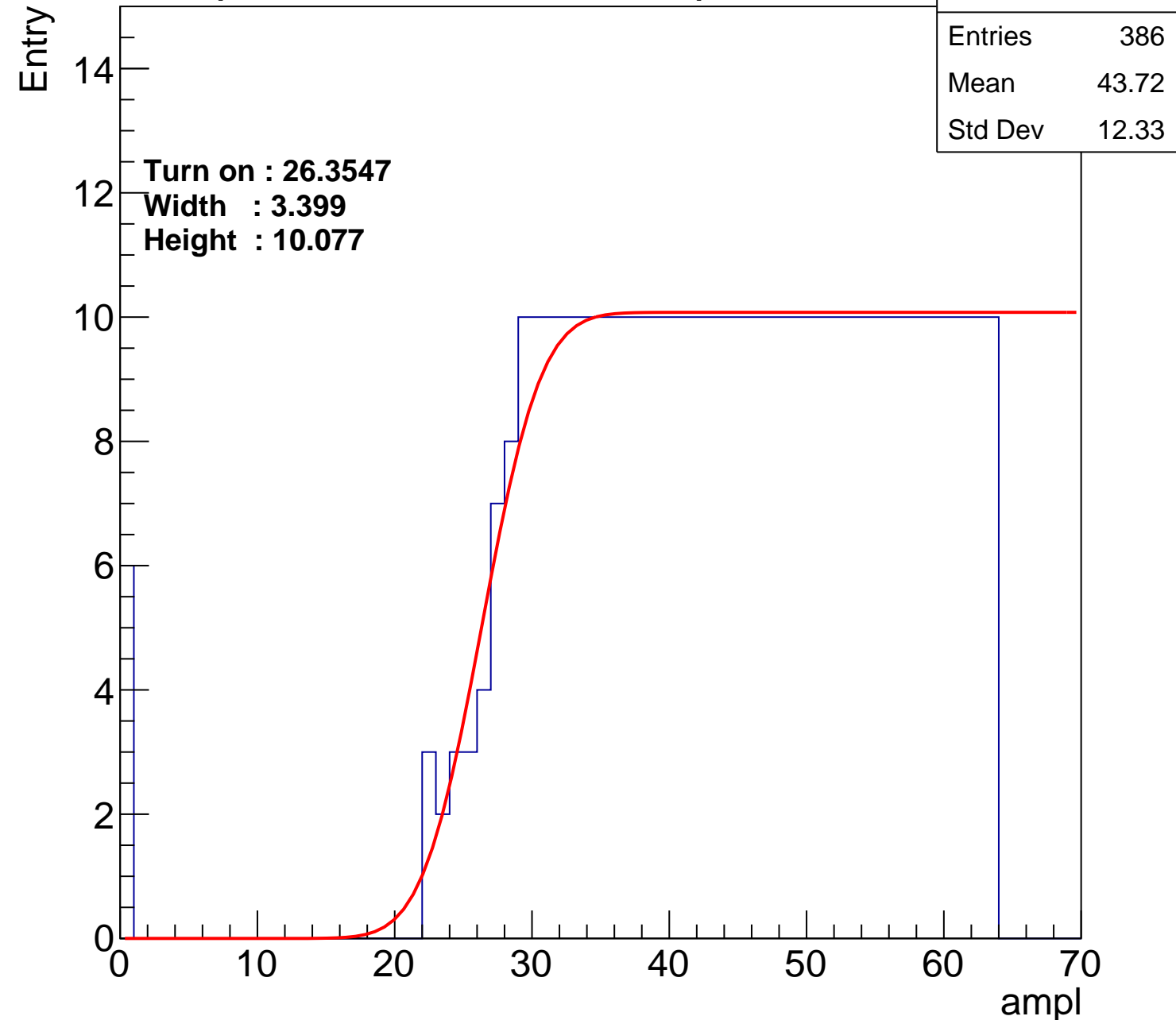
Width : 3.399

Height : 10.077

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U3-ch94

calib_packv5_042523_0143.root, FC#4, port A2

Entries	373
Mean	44.25
Std Dev	12.21

Turn on : 27.2453

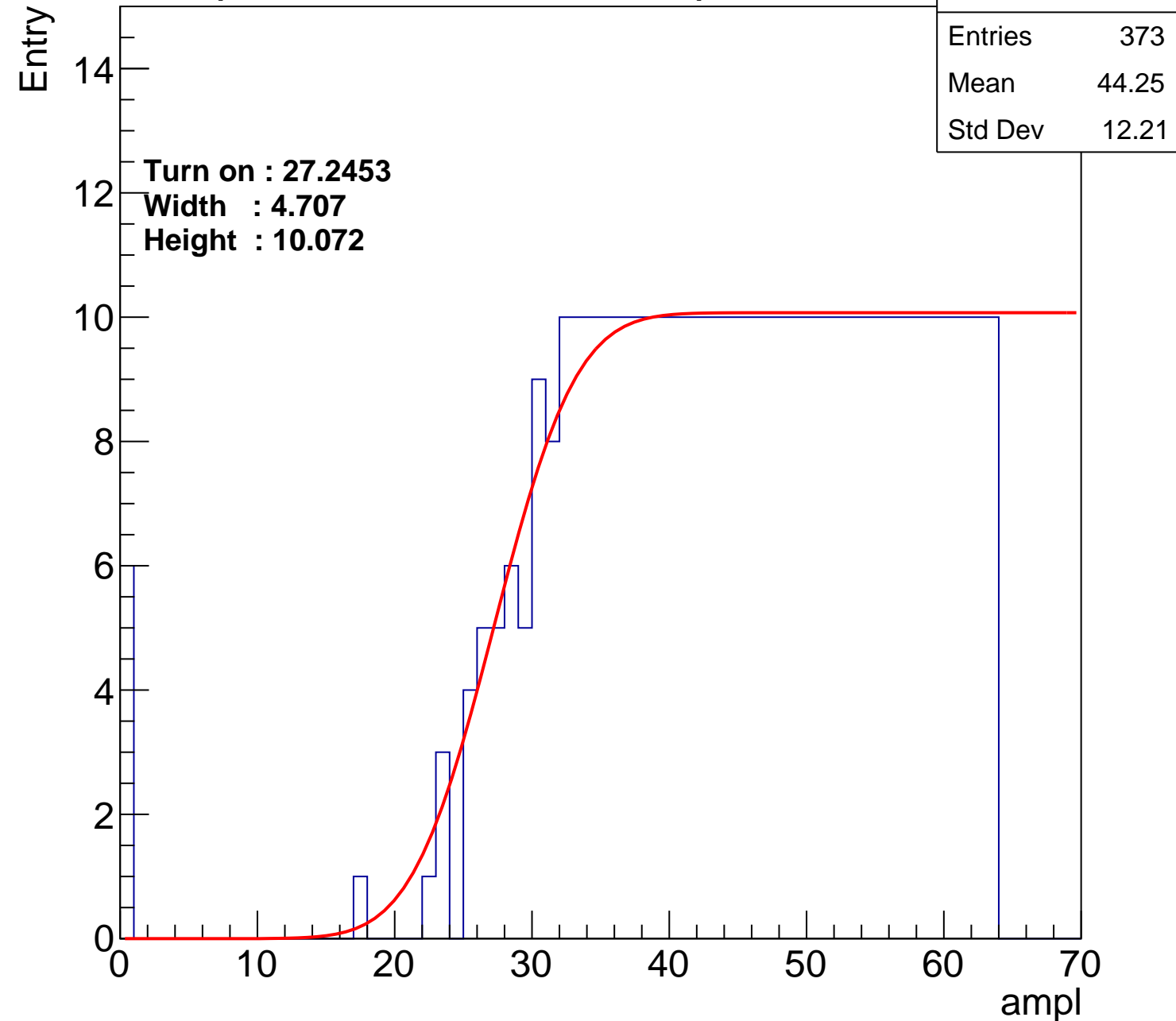
Width : 4.707

Height : 10.072

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U3-ch95

calib_packv5_042523_0143.root, FC#4, port A2

Entries	379
Mean	44.22
Std Dev	11.71

Turn on : 26.4870

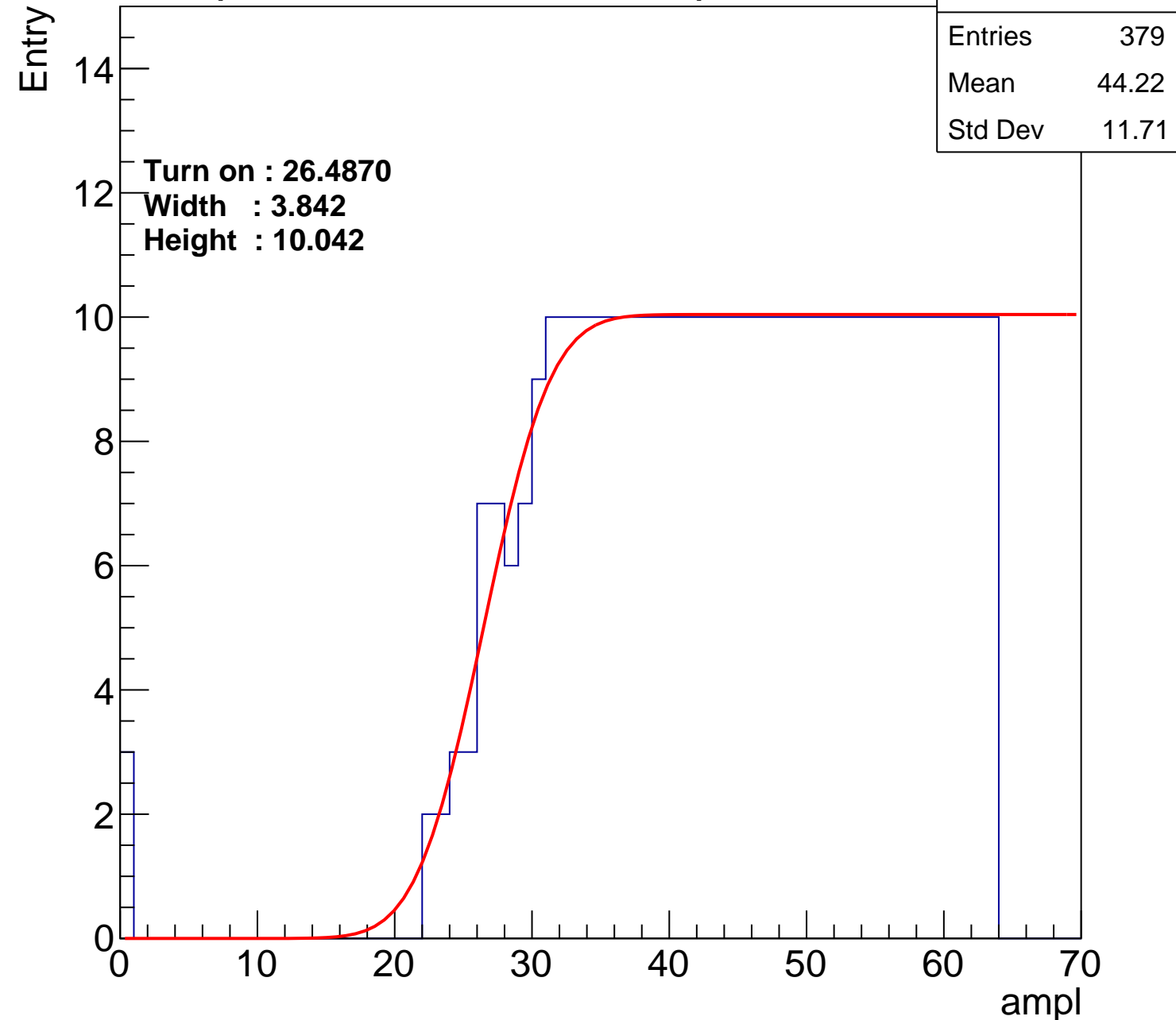
Width : 3.842

Height : 10.042

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U3-ch96

calib_packv5_042523_0143.root, FC#4, port A2

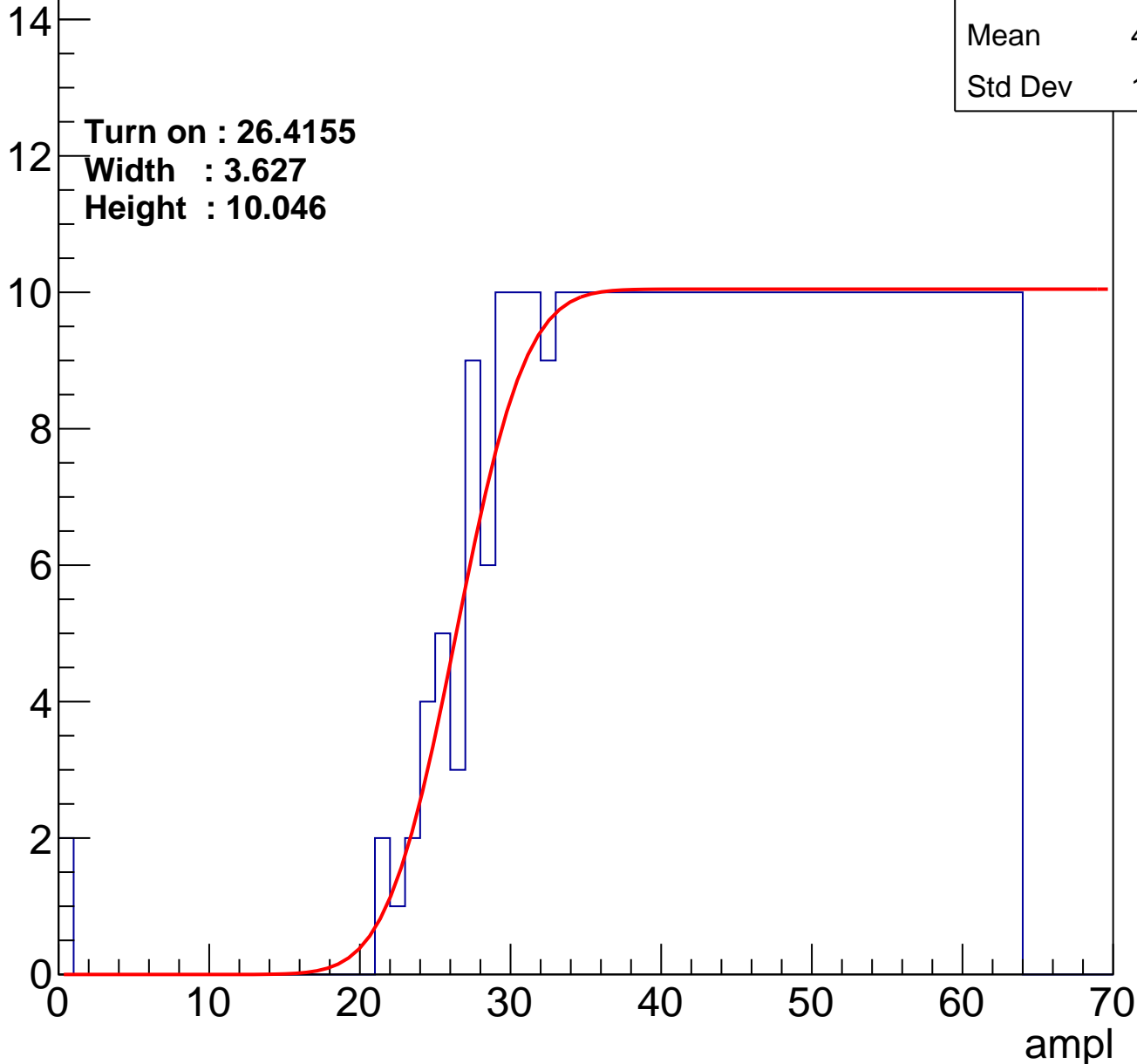
Entries	383
Mean	44.09
Std Dev	11.63

Turn on : 26.4155

Width : 3.627

Height : 10.046

Entry



B1L100S, U3-ch97

calib_packv5_042523_0143.root, FC#4, port A2

Entries	376
Mean	44.34
Std Dev	11.76

Turn on : 26.4167

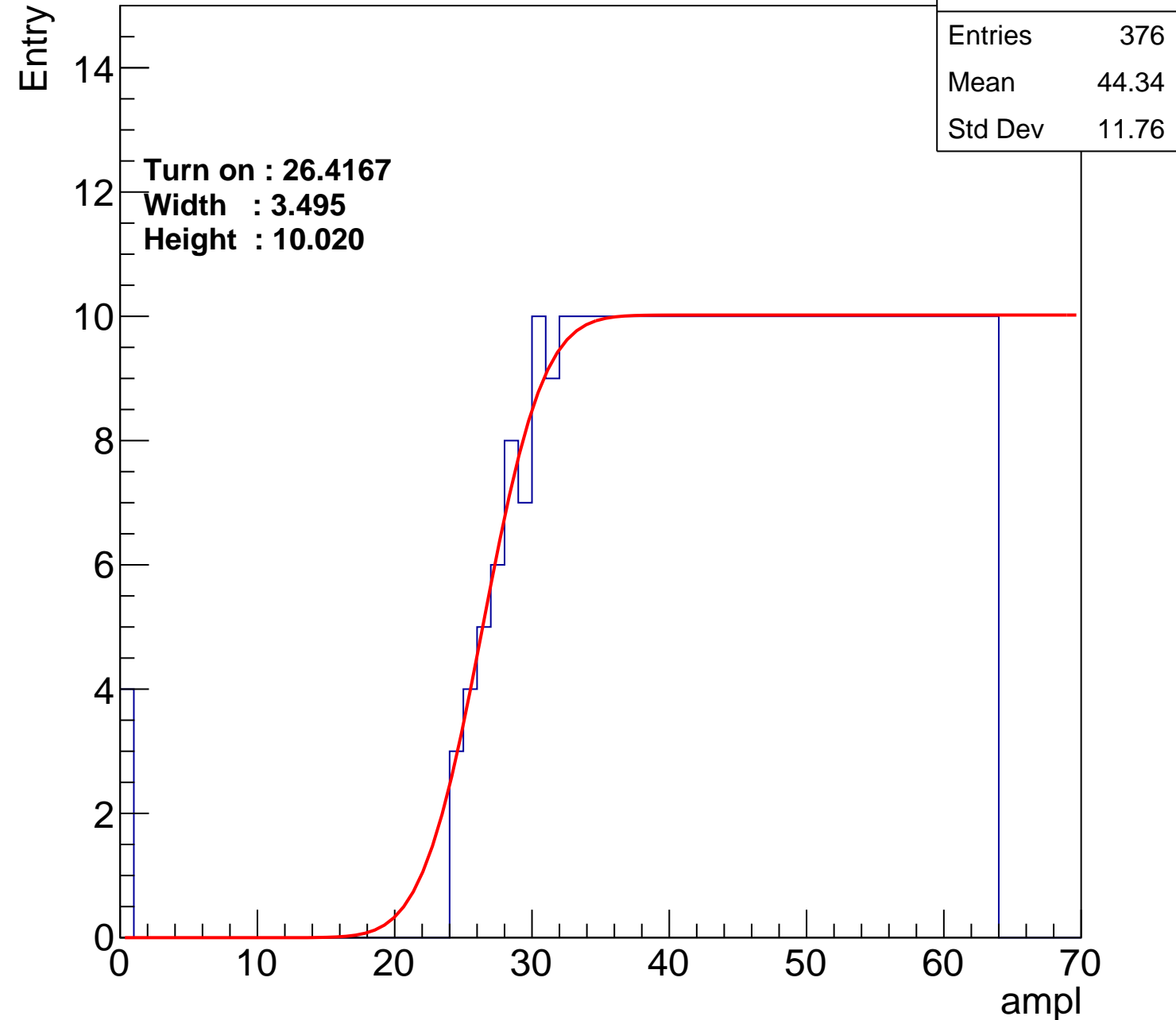
Width : 3.495

Height : 10.020

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U3-ch98

calib_packv5_042523_0143.root, FC#4, port A2

Entries	376
Mean	44.36
Std Dev	11.64

Turn on : 26.9190

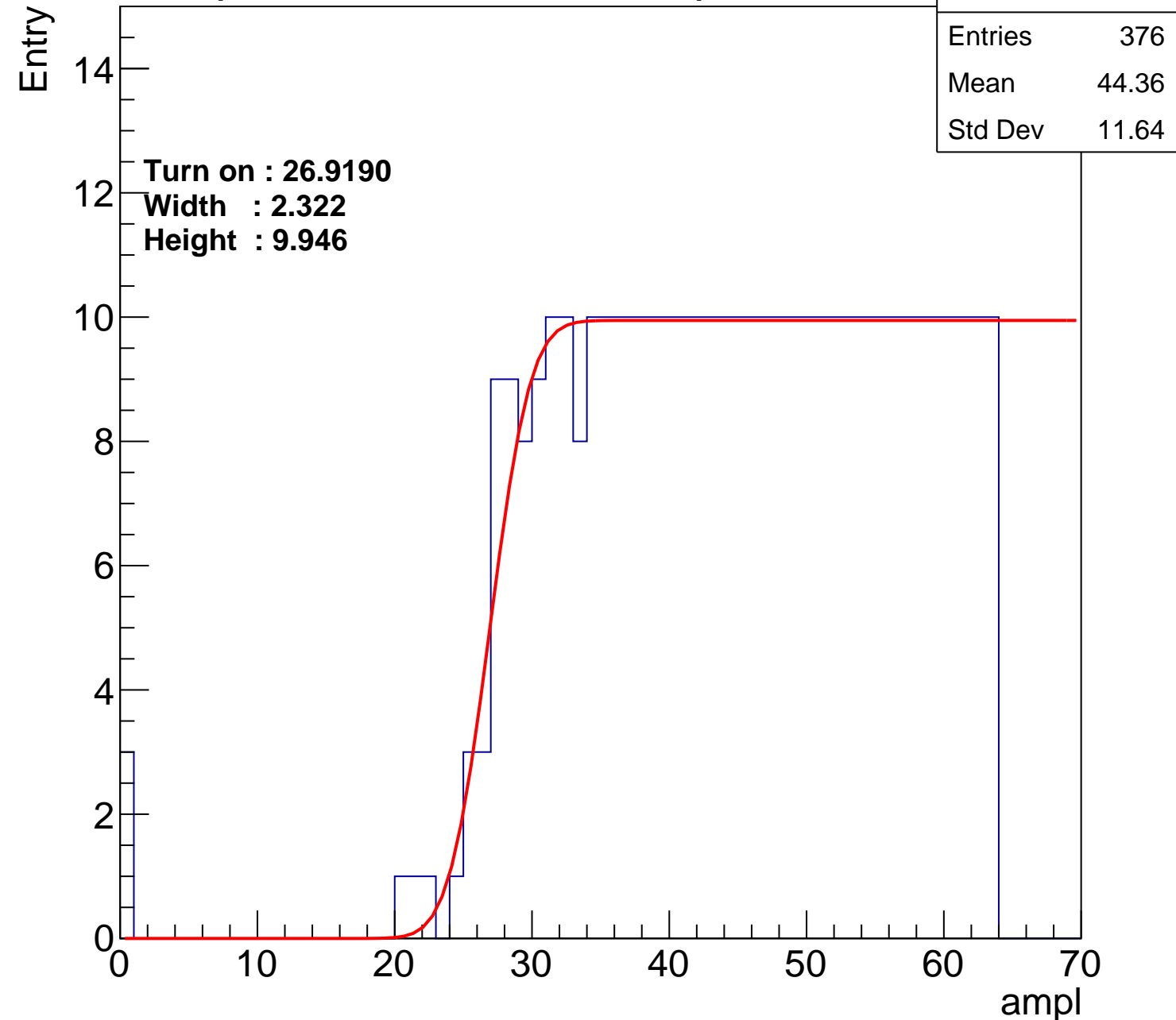
Width : 2.322

Height : 9.946

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U3-ch99

calib_packv5_042523_0143.root, FC#4, port A2

Entries	383
Mean	44.05
Std Dev	11.69

Turn on : 26.0411

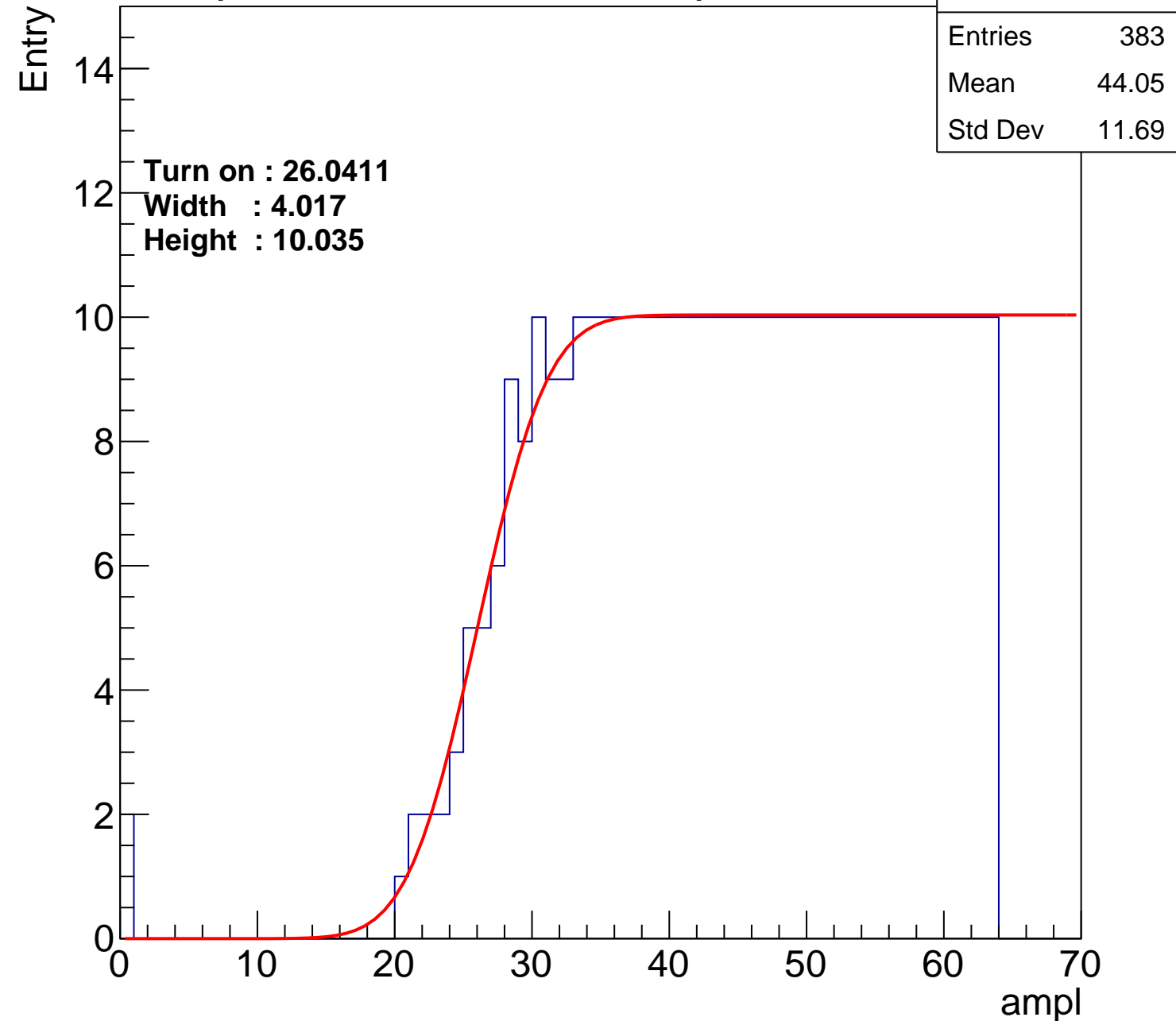
Width : 4.017

Height : 10.035

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U3-ch100

calib_packv5_042523_0143.root, FC#4, port A2

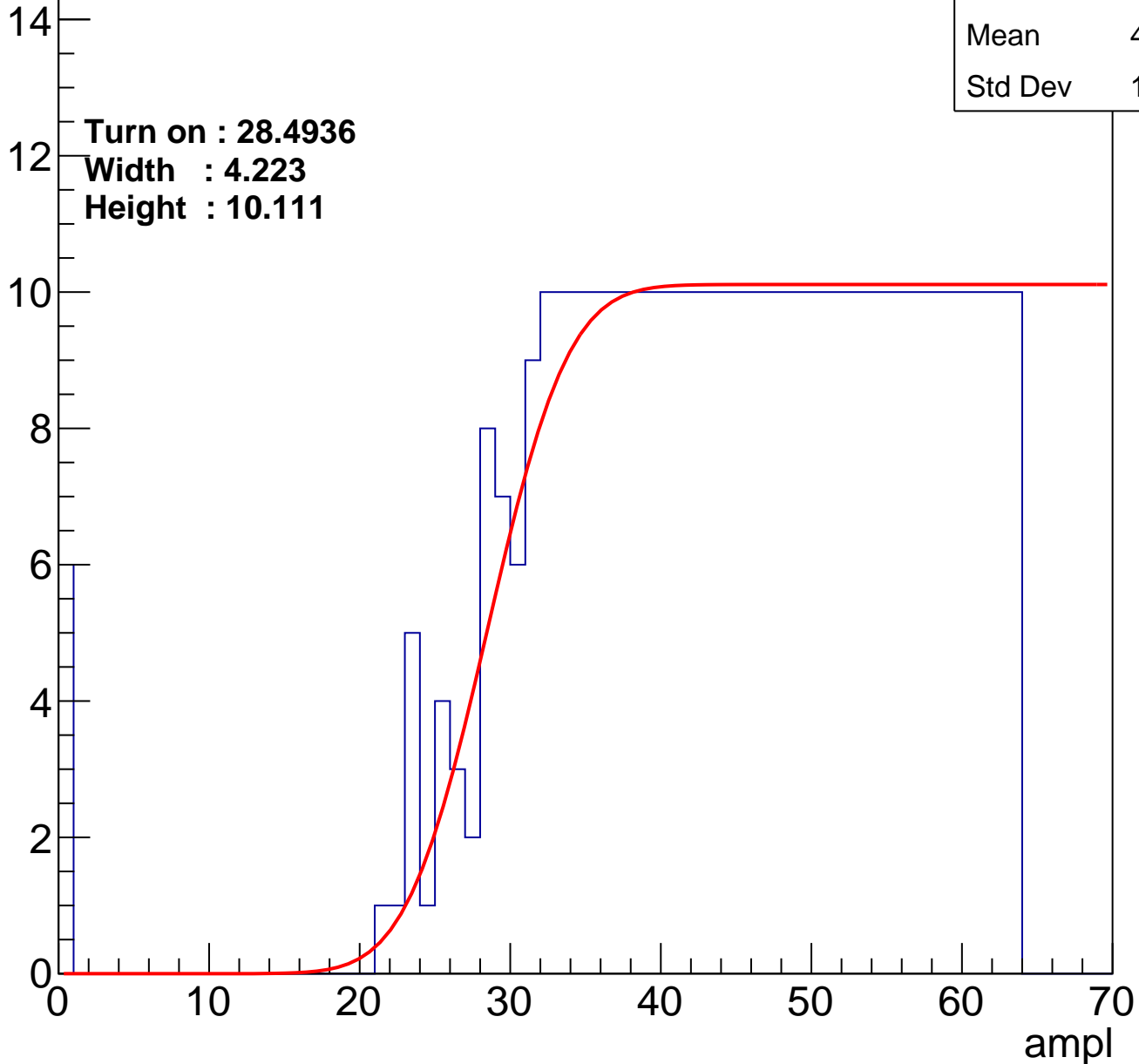
Entries	373
Mean	44.24
Std Dev	12.22

Turn on : 28.4936

Width : 4.223

Height : 10.111

Entry



B1L100S, U3-ch101

calib_packv5_042523_0143.root, FC#4, port A2

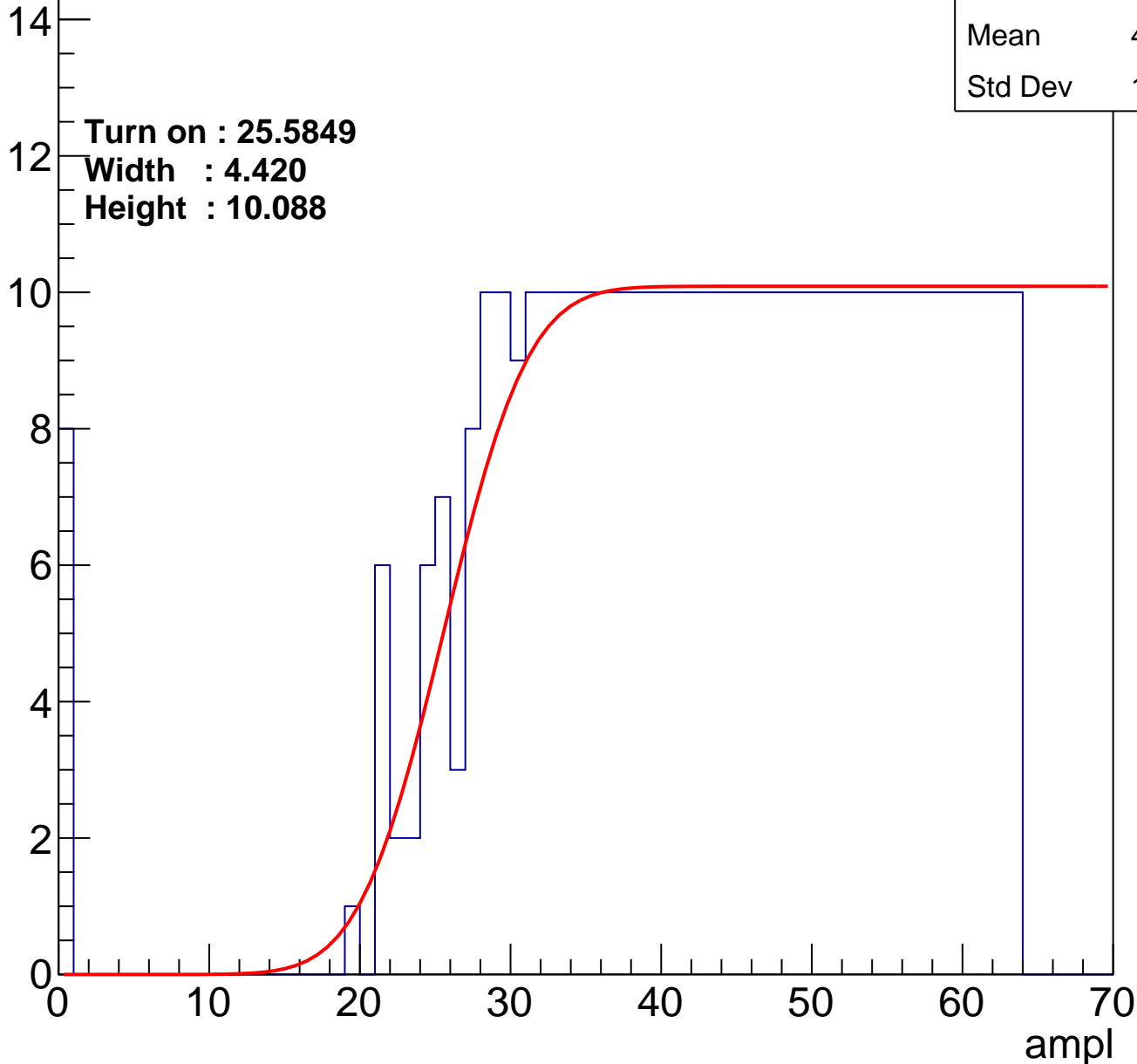
Entries	402
Mean	42.78
Std Dev	13.03

Turn on : 25.5849

Width : 4.420

Height : 10.088

Entry



B1L100S, U3-ch102

calib_packv5_042523_0143.root, FC#4, port A2

Entries	390
Mean	43.69
Std Dev	11.97

Turn on : 25.2392

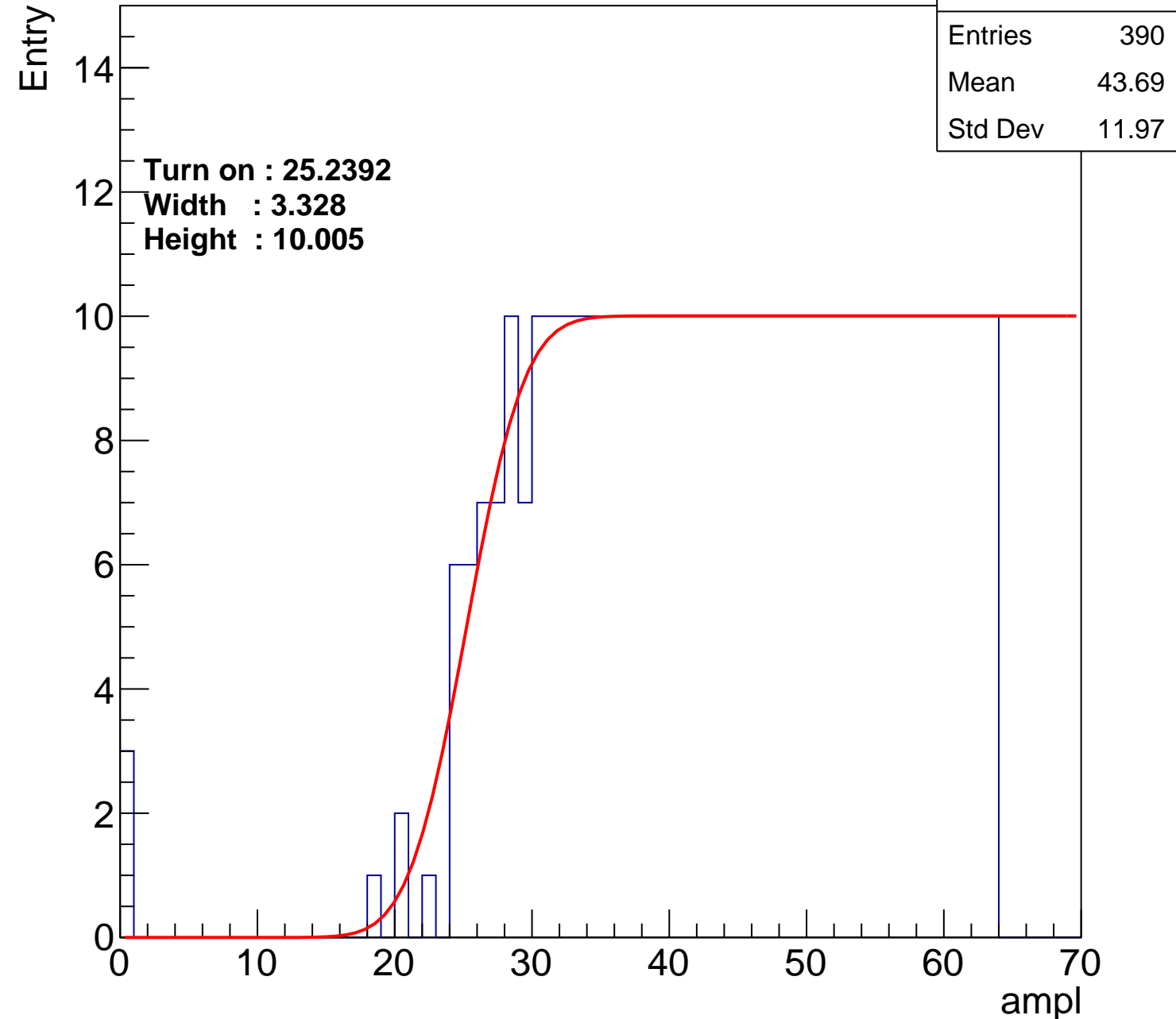
Width : 3.328

Height : 10.005

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U3-ch103

calib_packv5_042523_0143.root, FC#4, port A2

Entries	380
Mean	44.07
Std Dev	11.95

Turn on : 26.5354

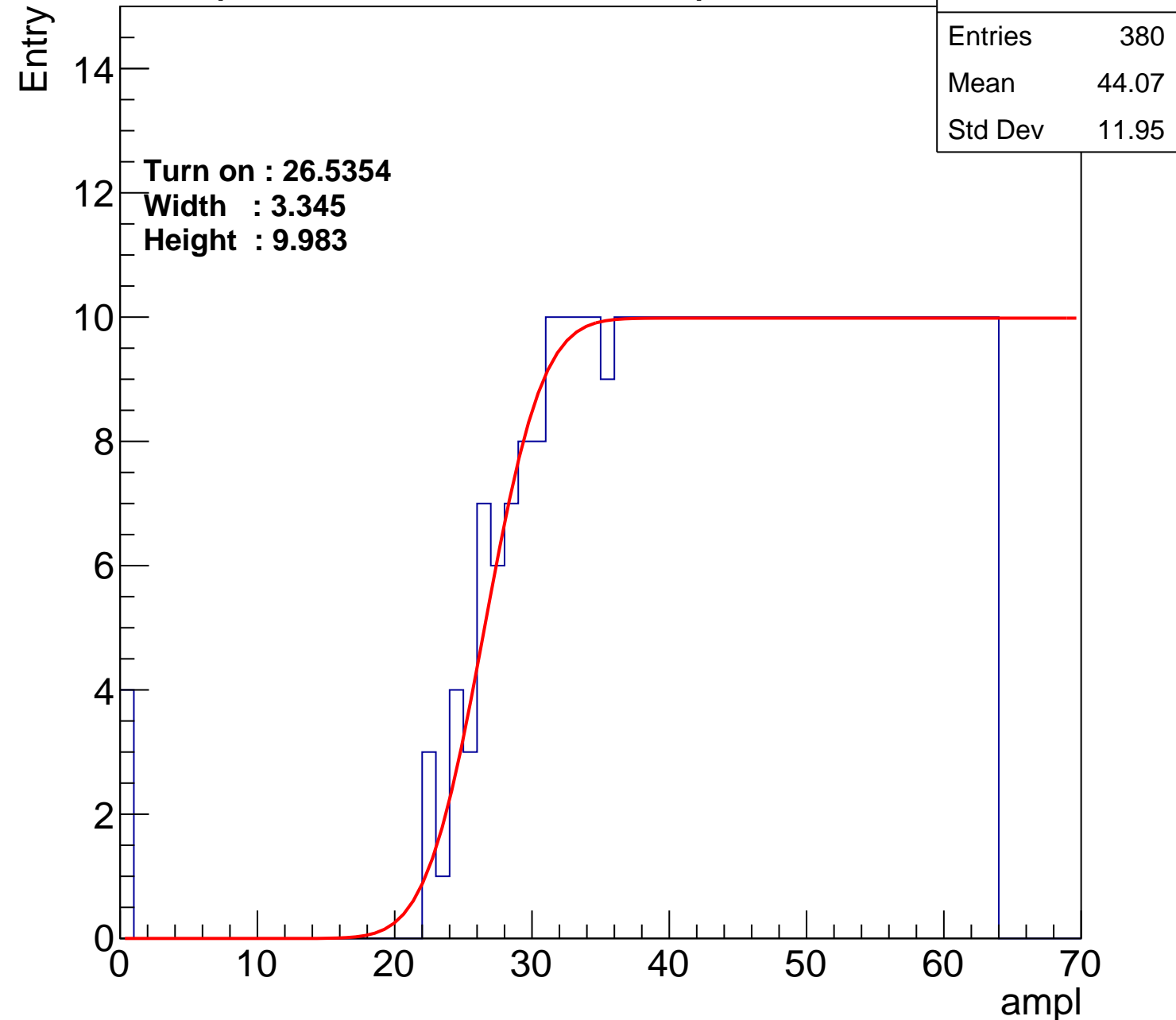
Width : 3.345

Height : 9.983

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U3-ch104

calib_packv5_042523_0143.root, FC#4, port A2

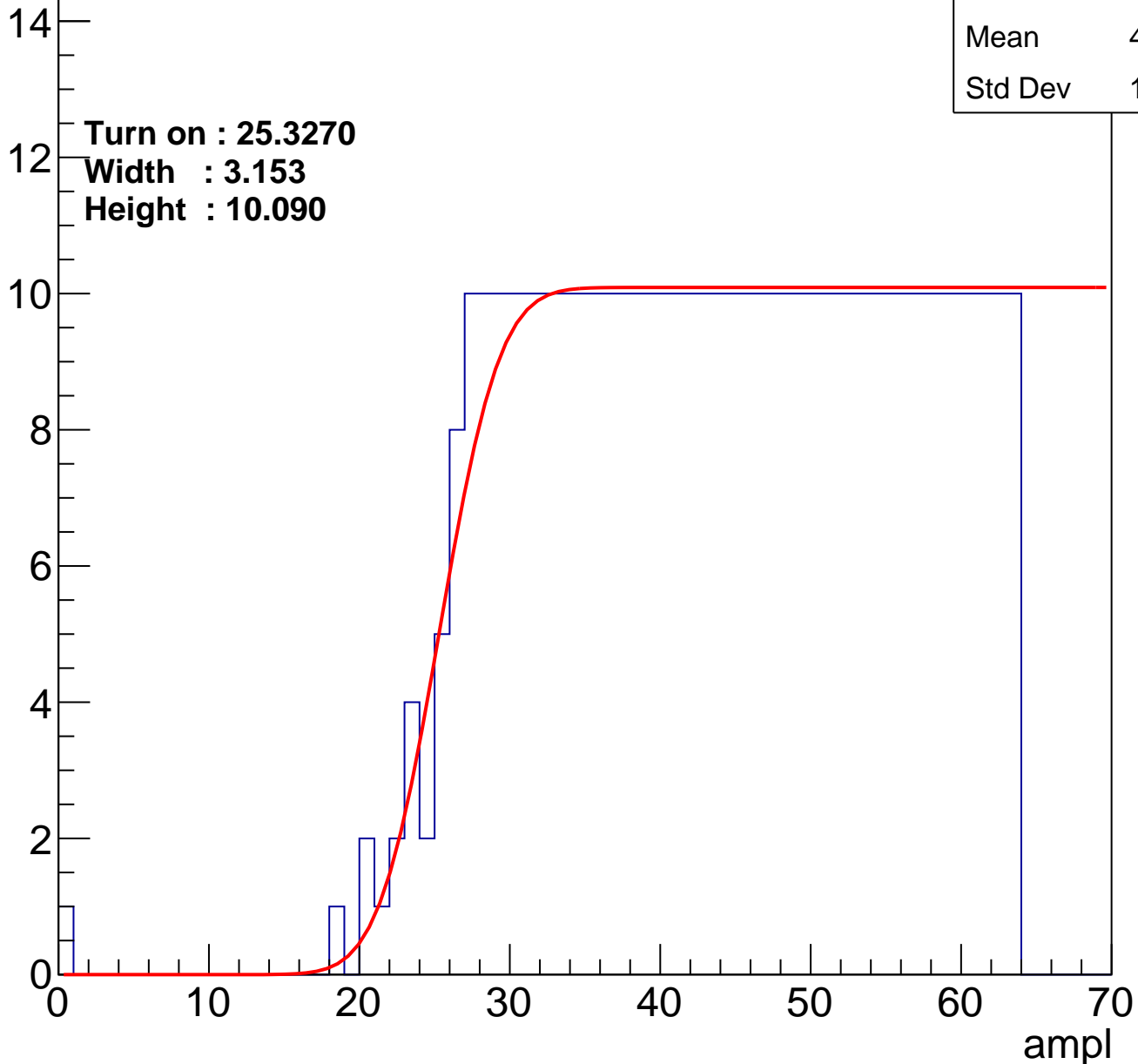
Entries	396
Mean	43.55
Std Dev	11.75

Turn on : 25.3270

Width : 3.153

Height : 10.090

Entry



B1L100S, U3-ch105

calib_packv5_042523_0143.root, FC#4, port A2

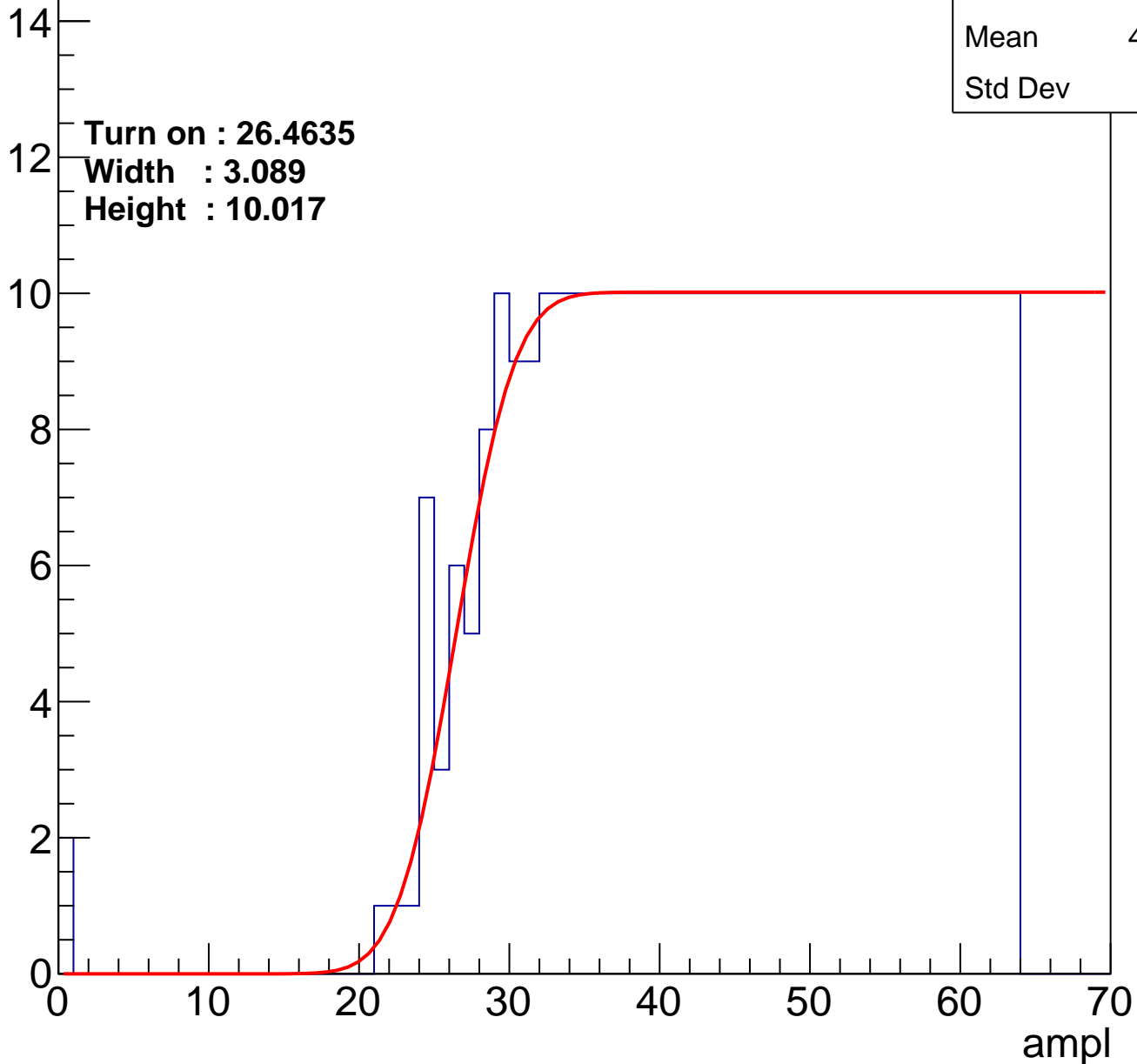
Entries	382
Mean	44.14
Std Dev	11.6

Turn on : 26.4635

Width : 3.089

Height : 10.017

Entry



B1L100S, U3-ch106

calib_packv5_042523_0143.root, FC#4, port A2

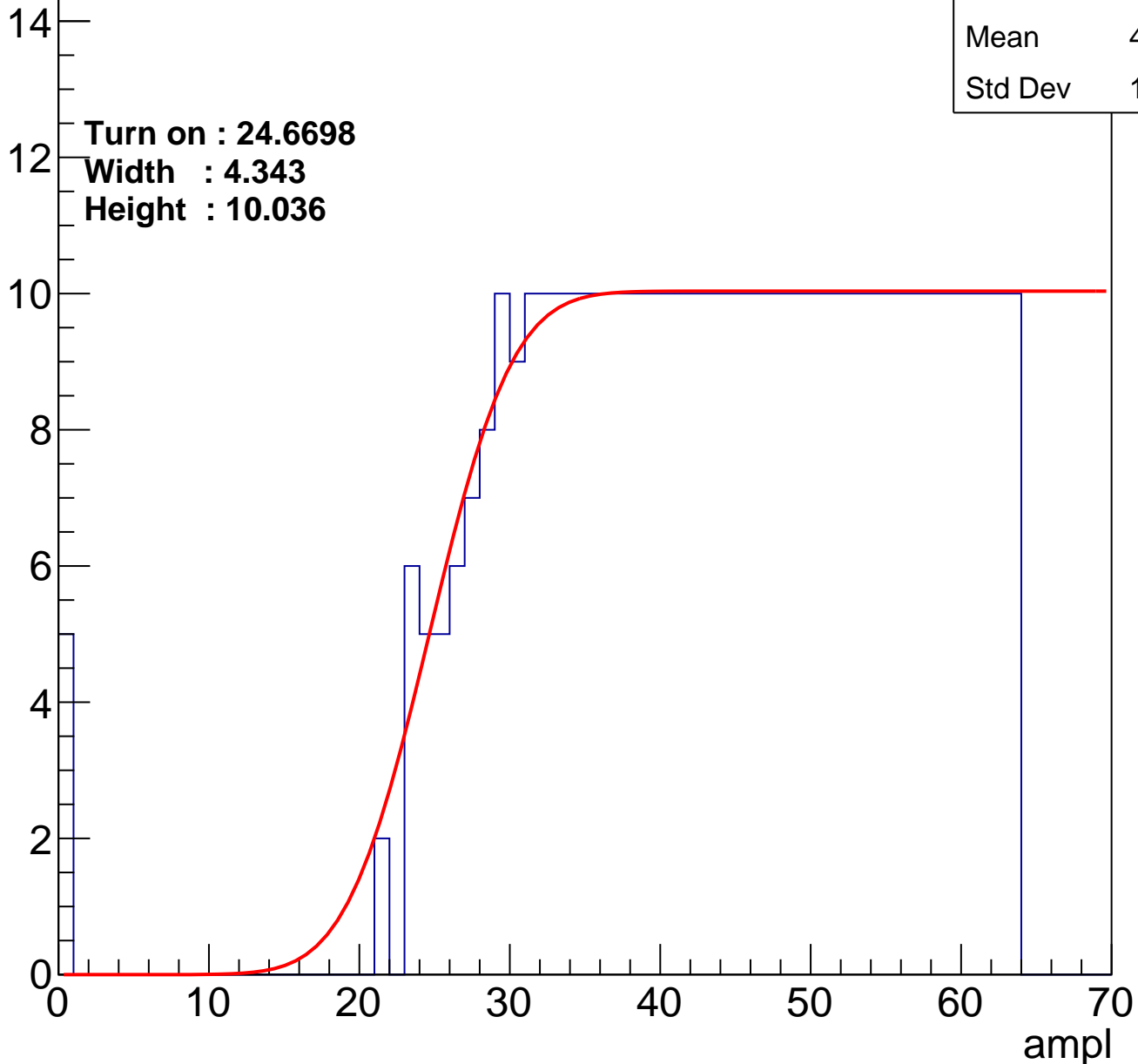
Entries	393
Mean	43.42
Std Dev	12.35

Turn on : 24.6698

Width : 4.343

Height : 10.036

Entry



B1L100S, U3-ch107

calib_packv5_042523_0143.root, FC#4, port A2

Entries	389
Mean	43.67
Std Dev	12.12

Turn on : 25.6241

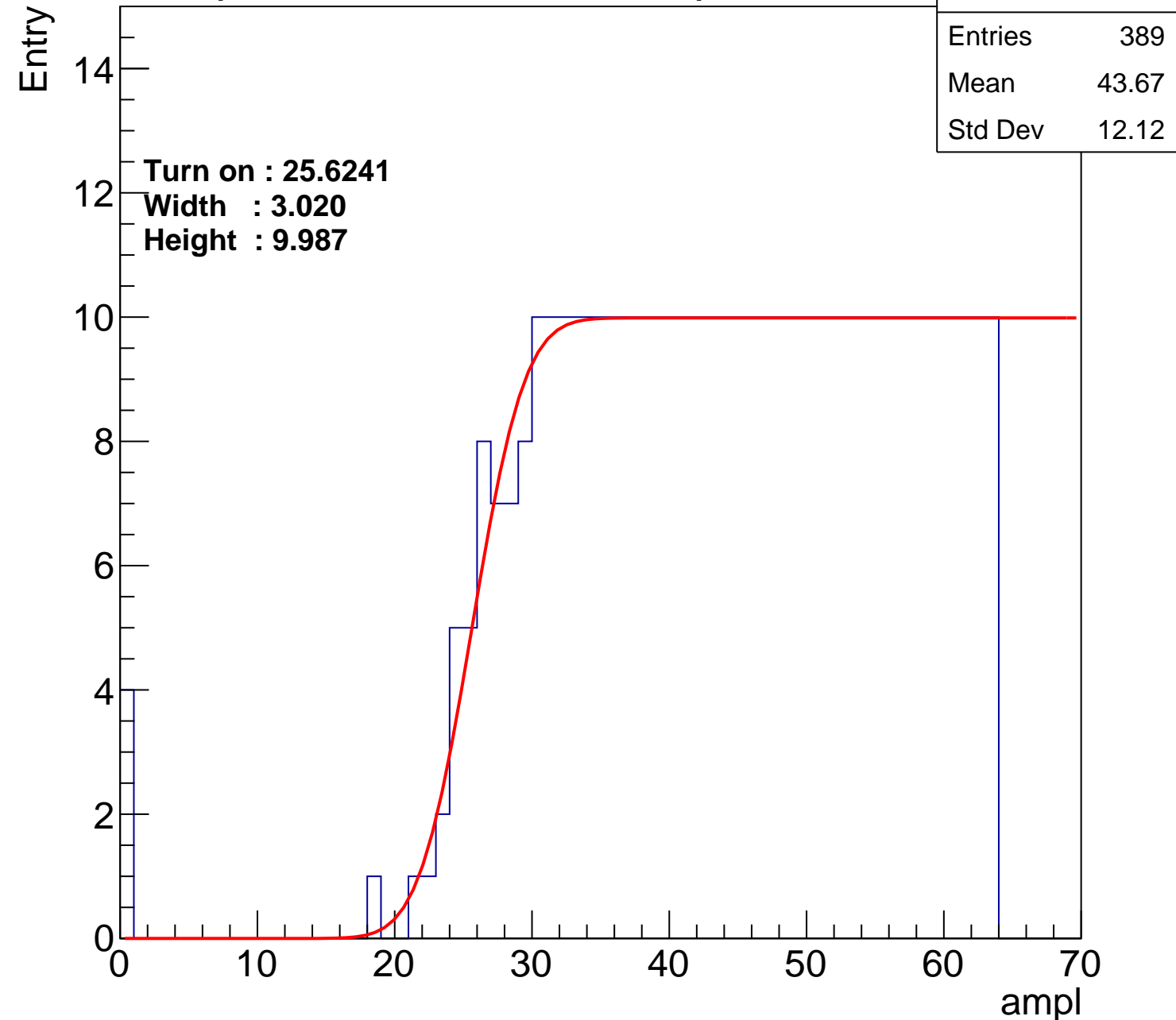
Width : 3.020

Height : 9.987

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U3-ch108

calib_packv5_042523_0143.root, FC#4, port A2

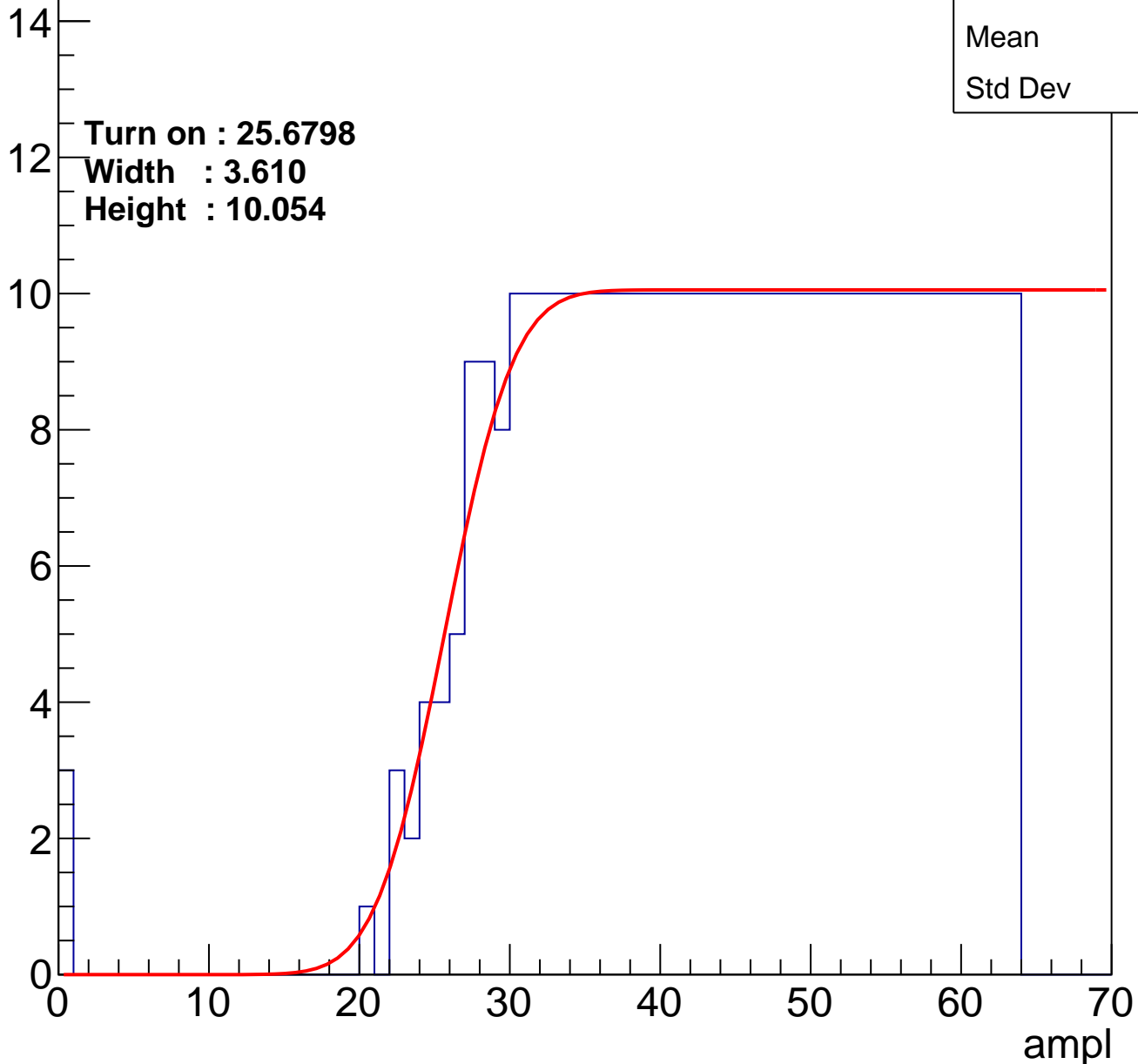
Entries	388
Mean	43.8
Std Dev	11.9

Turn on : 25.6798

Width : 3.610

Height : 10.054

Entry



B1L100S, U3-ch109

calib_packv5_042523_0143.root, FC#4, port A2

Entries	388
Mean	43.79
Std Dev	11.91

Turn on : 26.0144

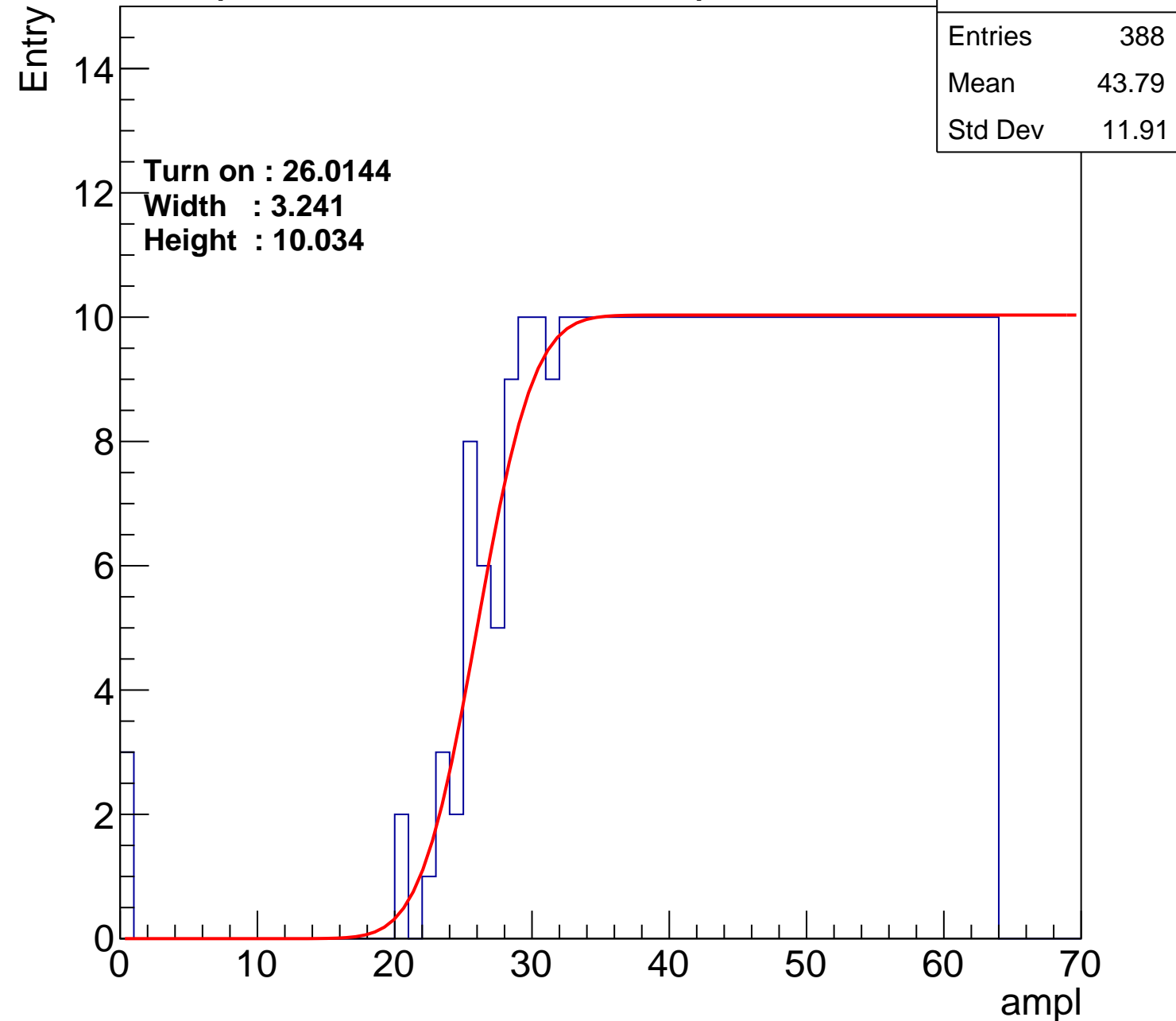
Width : 3.241

Height : 10.034

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U3-ch110

calib_packv5_042523_0143.root, FC#4, port A2

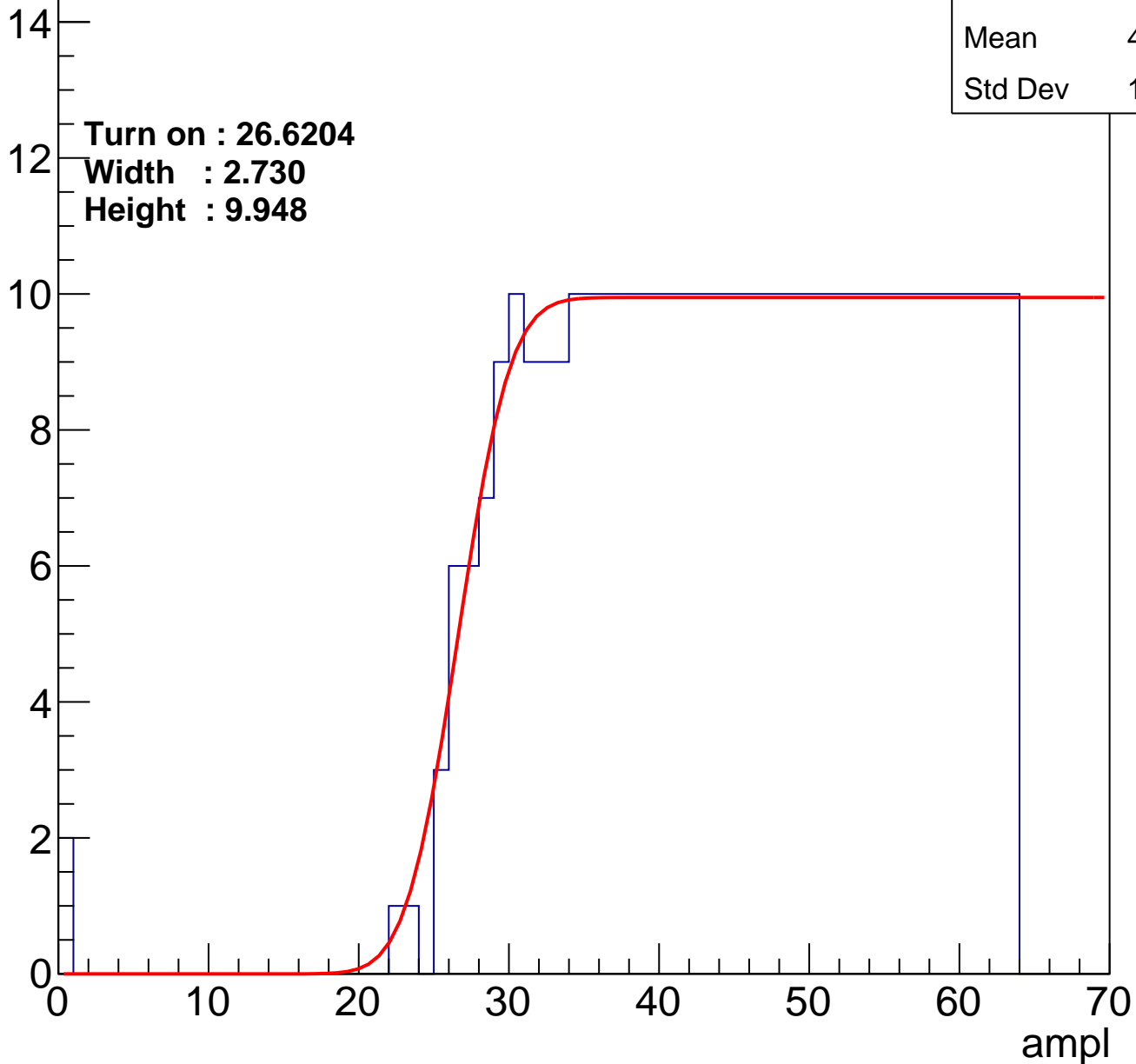
Entries	372
Mean	44.65
Std Dev	11.32

Turn on : 26.6204

Width : 2.730

Height : 9.948

Entry



B1L100S, U3-ch111

calib_packv5_042523_0143.root, FC#4, port A2

Entries	375
Mean	44.41
Std Dev	11.62

Turn on : 26.7955

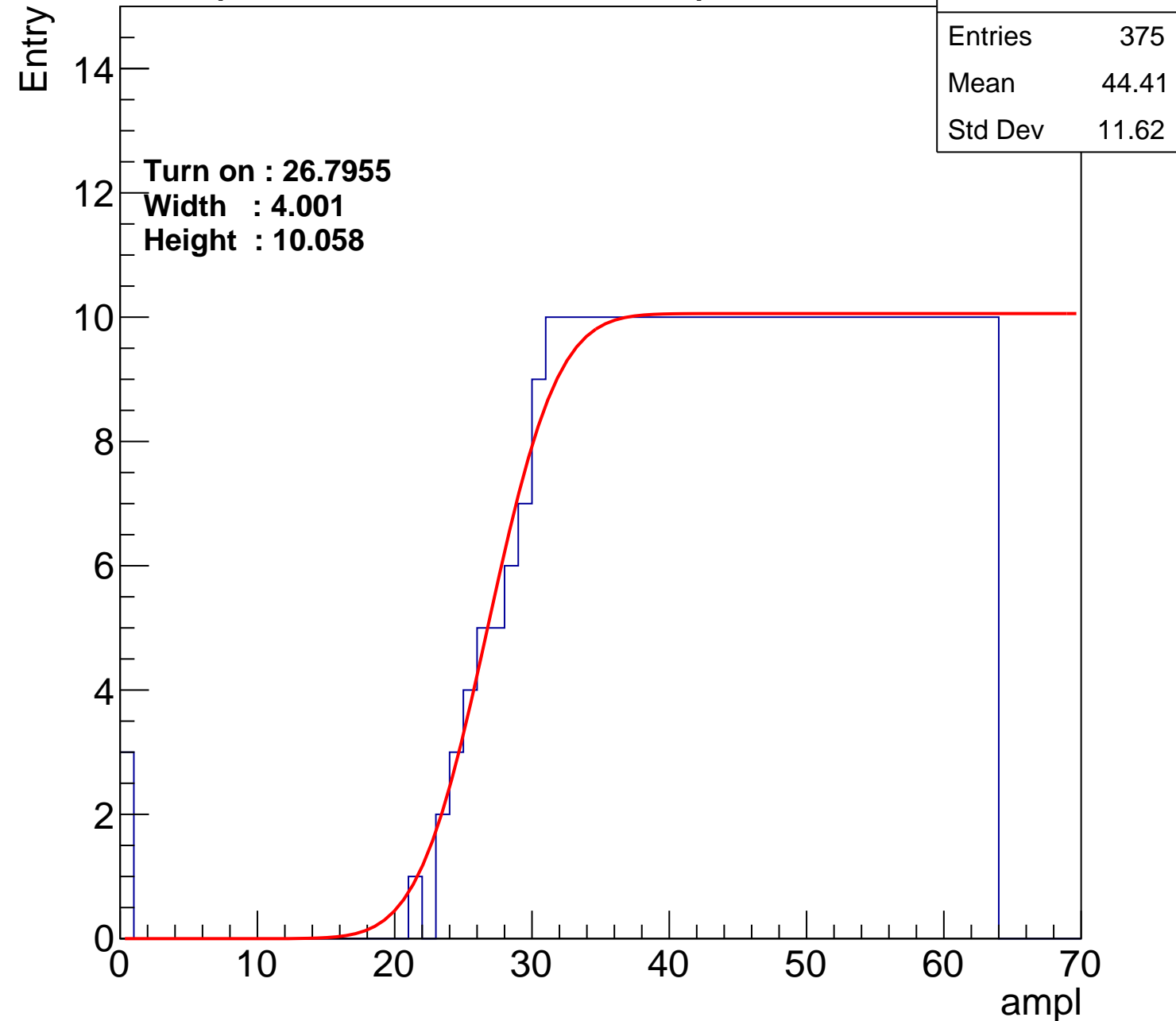
Width : 4.001

Height : 10.058

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U3-ch112

calib_packv5_042523_0143.root, FC#4, port A2

Entries	381
Mean	44.17
Std Dev	11.68

Turn on : 26.3657

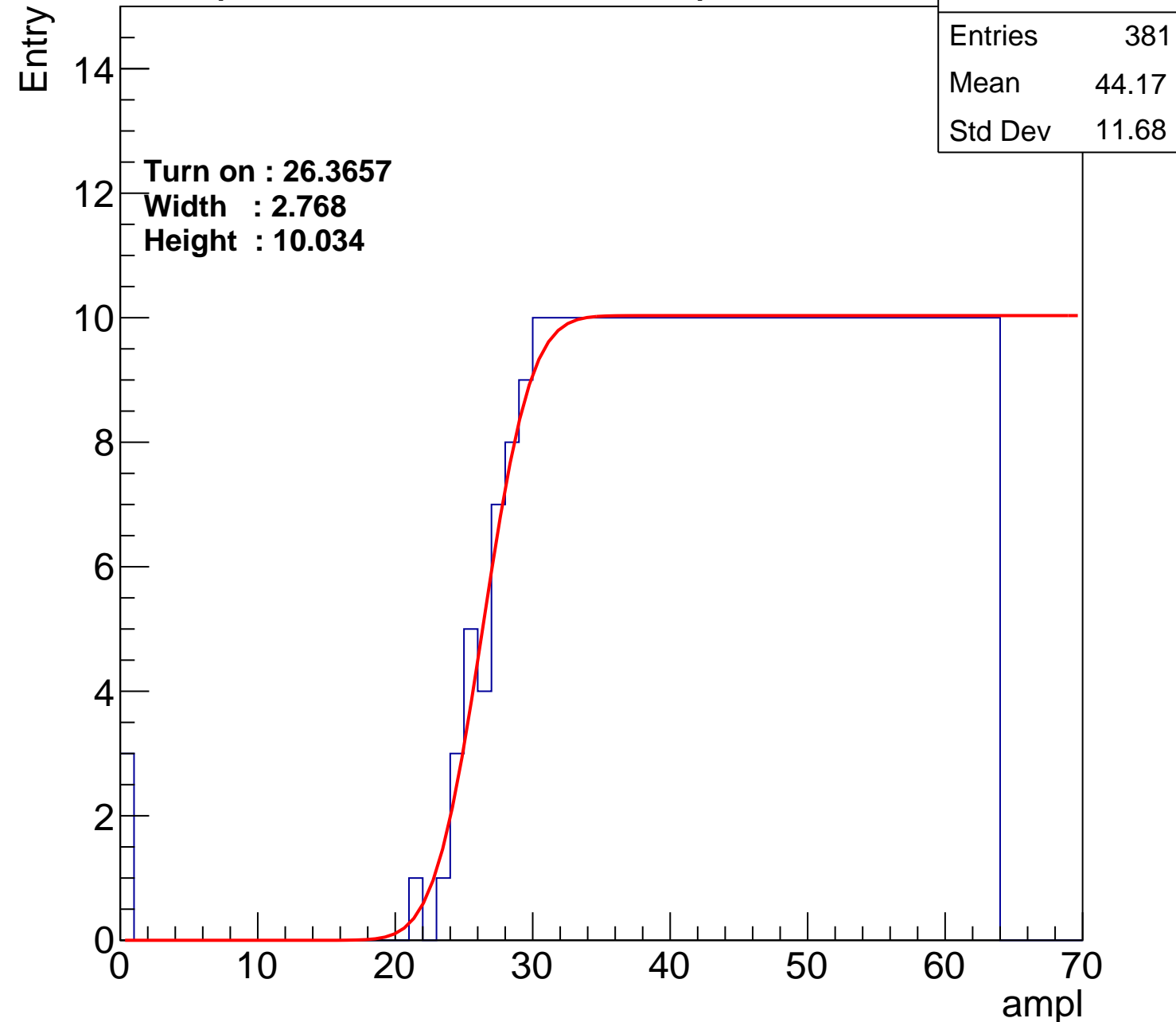
Width : 2.768

Height : 10.034

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U3-ch113

calib_packv5_042523_0143.root, FC#4, port A2

Entries	358
Mean	45.17
Std Dev	11.41

Turn on : 28.6489

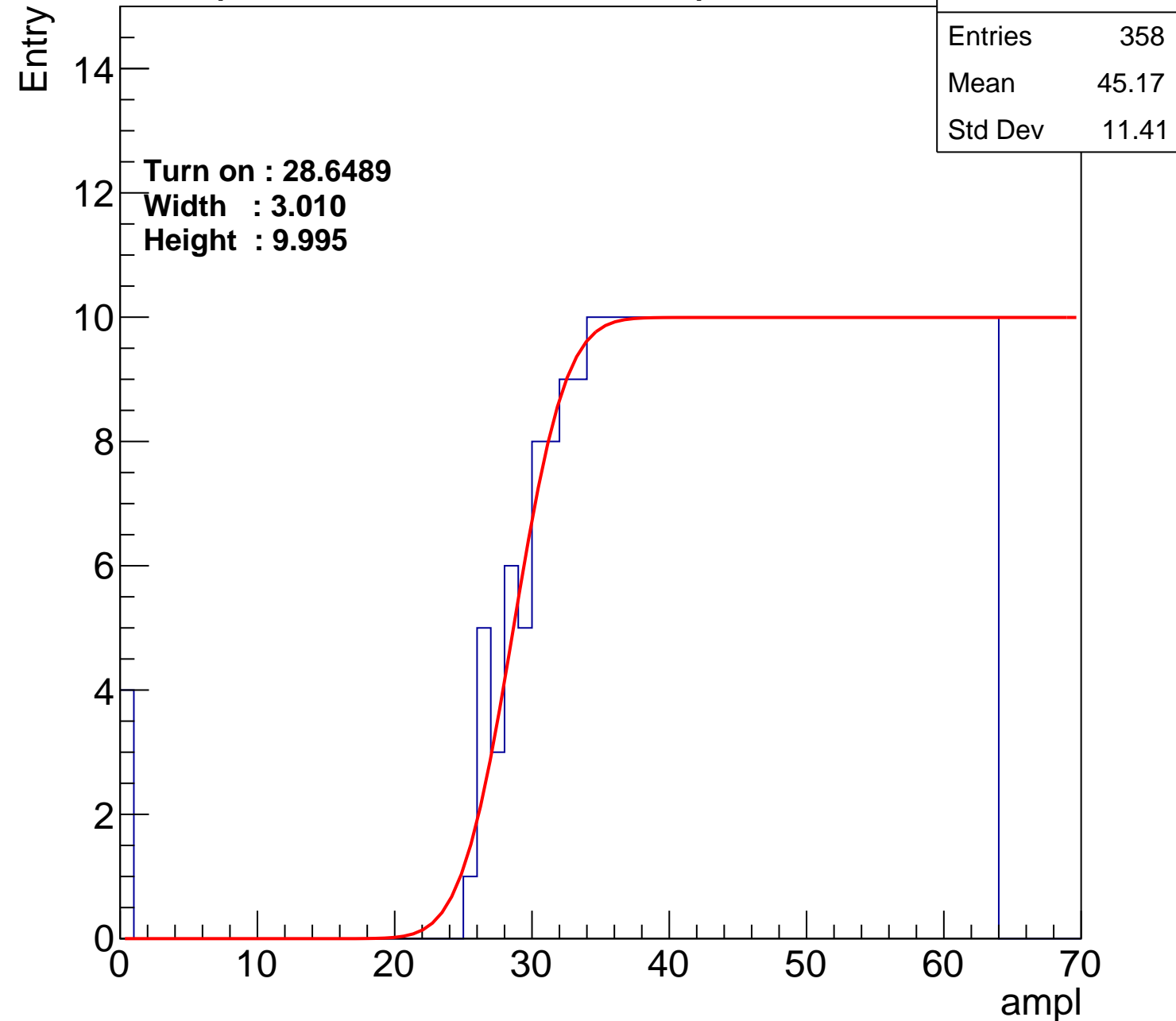
Width : 3.010

Height : 9.995

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U3-ch114

calib_packv5_042523_0143.root, FC#4, port A2

Entries	375
Mean	44.37
Std Dev	11.76

Turn on : 27.4560

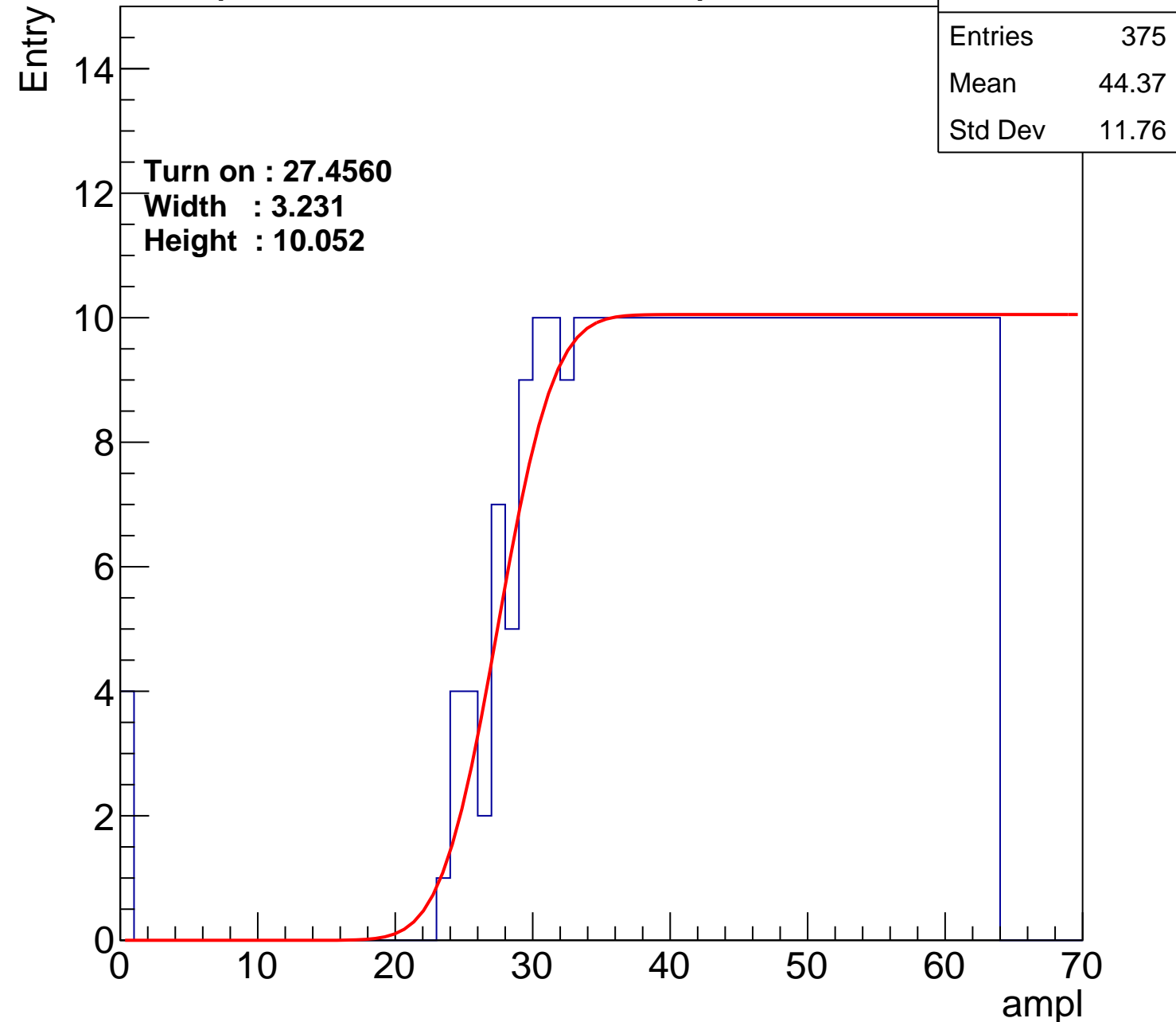
Width : 3.231

Height : 10.052

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U3-ch115

calib_packv5_042523_0143.root, FC#4, port A2

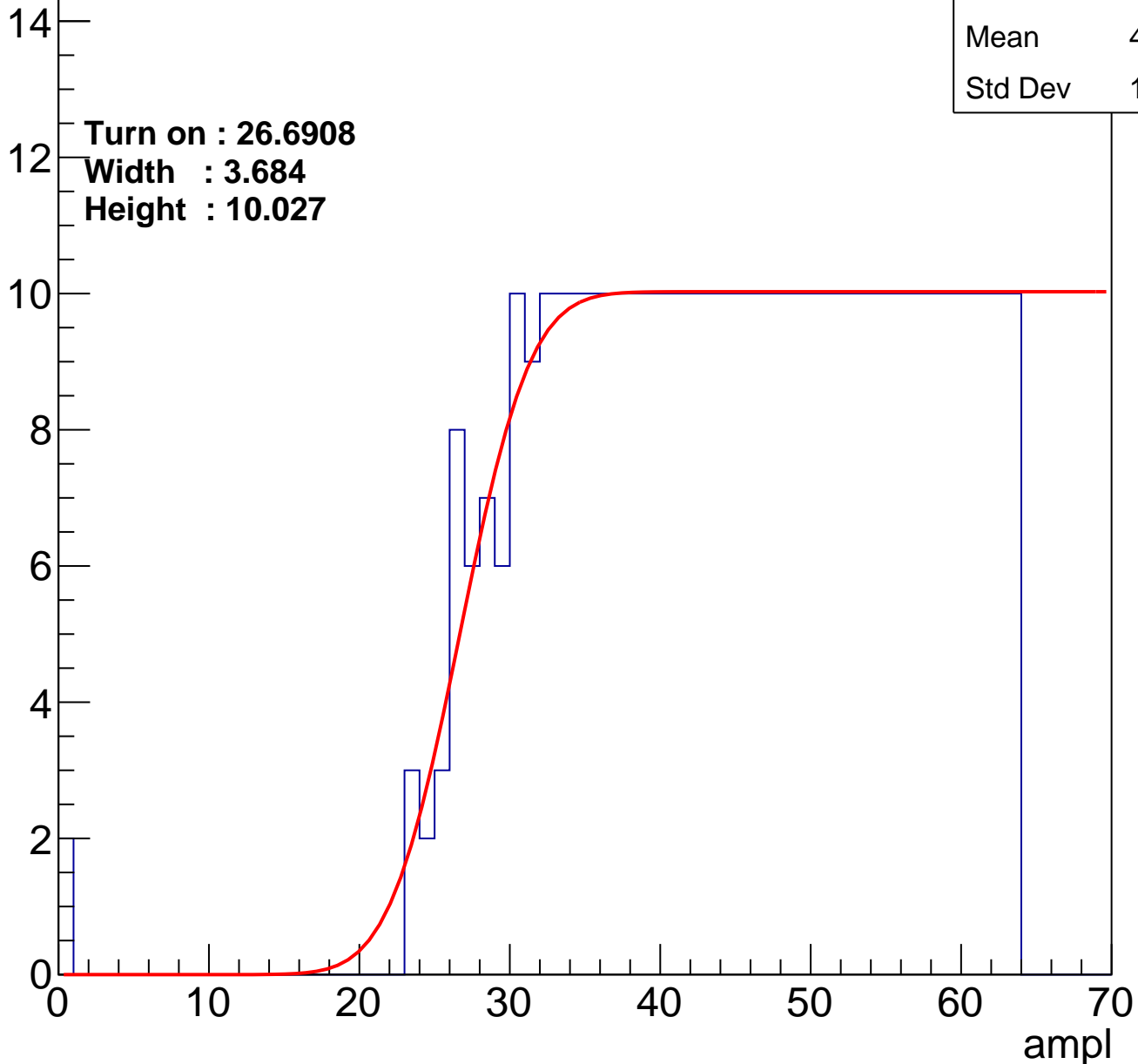
Entries	376
Mean	44.44
Std Dev	11.43

Turn on : 26.6908

Width : 3.684

Height : 10.027

Entry



B1L100S, U3-ch116

calib_packv5_042523_0143.root, FC#4, port A2

Entries	400
Mean	43.21
Std Dev	12.2

Turn on : 24.6746

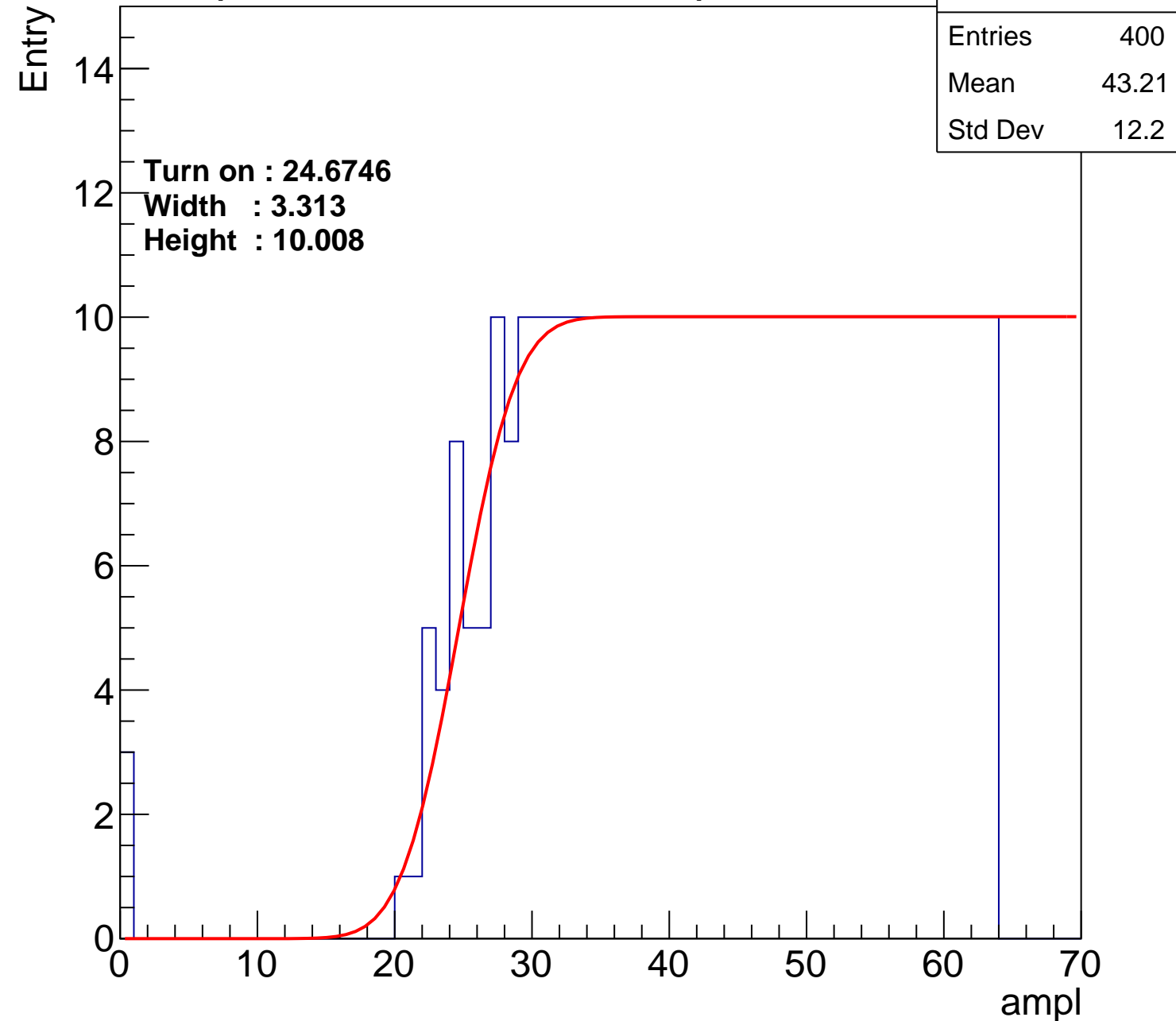
Width : 3.313

Height : 10.008

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U3-ch117

calib_packv5_042523_0143.root, FC#4, port A2

Entries	376
Mean	44.46
Std Dev	11.41

Turn on : 26.6718

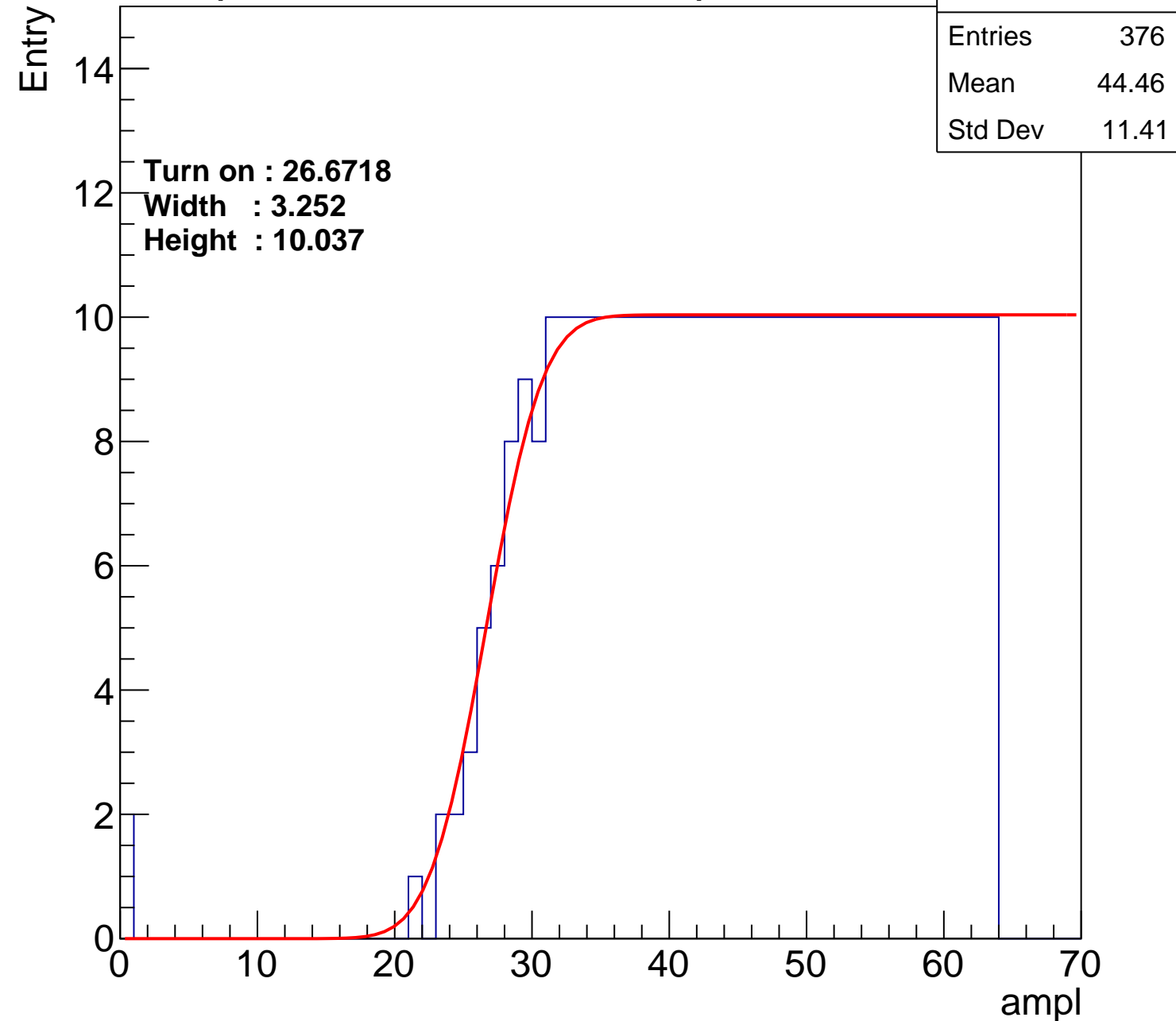
Width : 3.252

Height : 10.037

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U3-ch118

calib_packv5_042523_0143.root, FC#4, port A2

Entries	366
Mean	45.06
Std Dev	10.9

Turn on : 28.0345

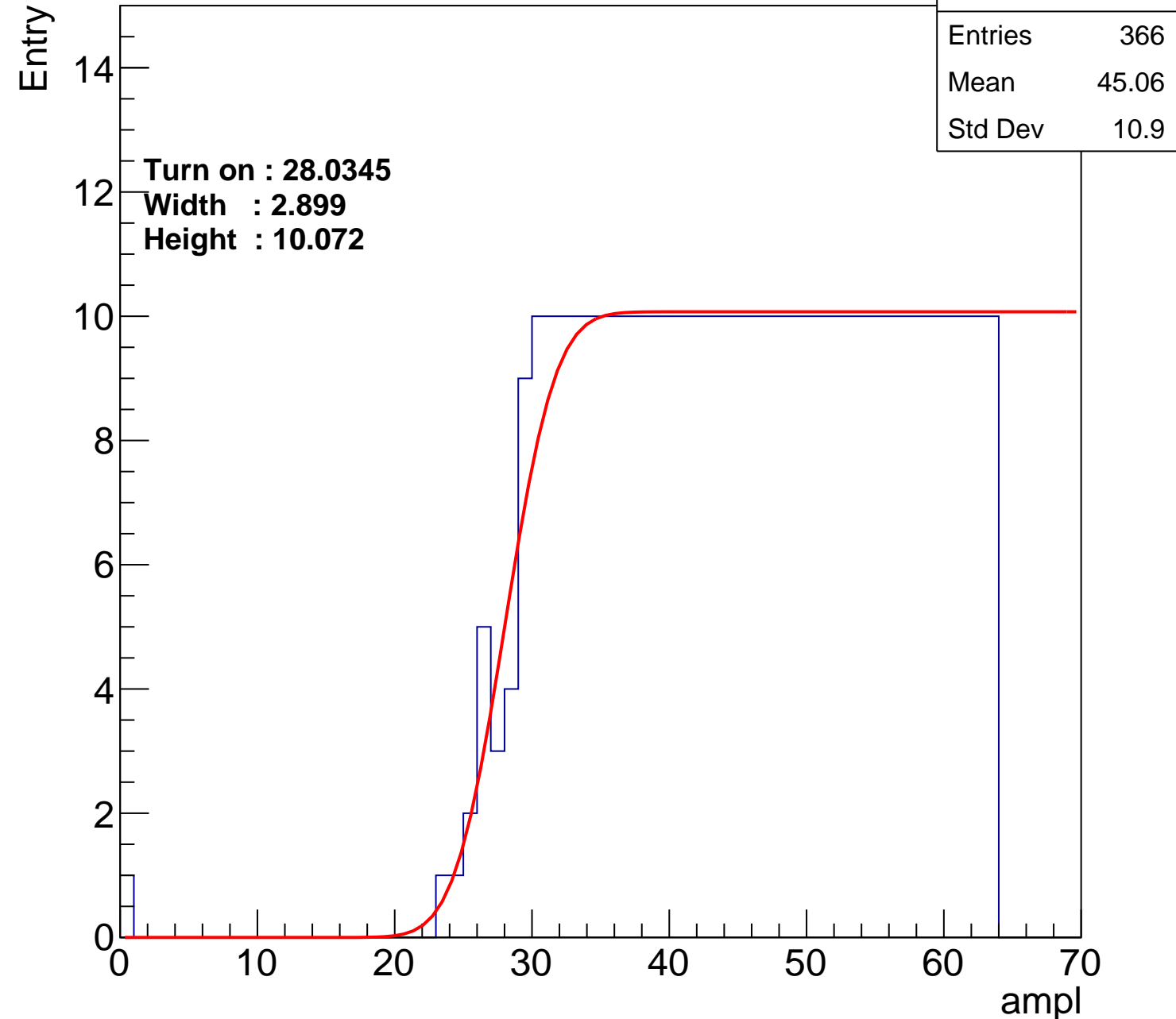
Width : 2.899

Height : 10.072

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U3-ch119

calib_packv5_042523_0143.root, FC#4, port A2

Entries	376
Mean	44.45
Std Dev	11.43

Turn on : 27.6456

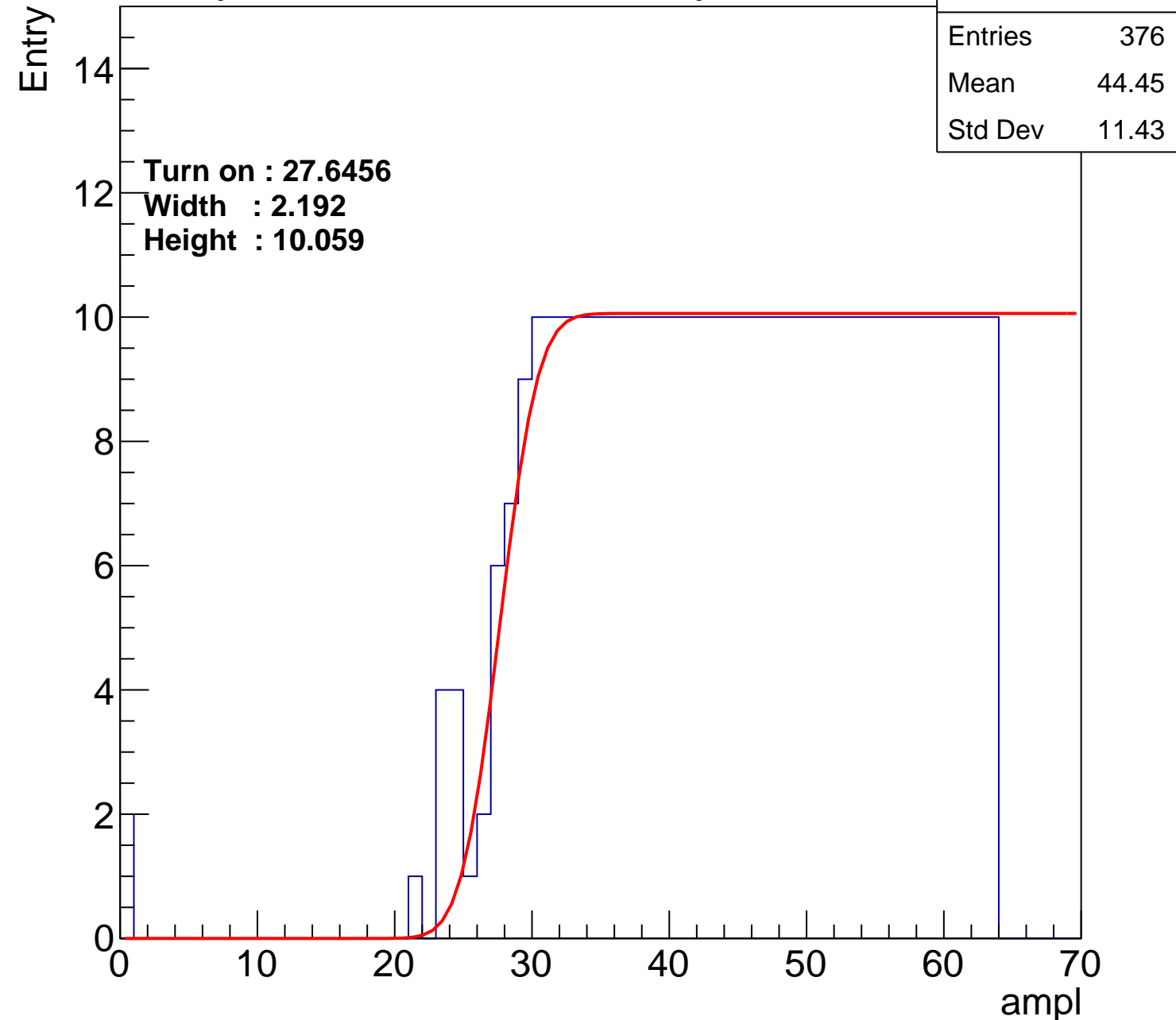
Width : 2.192

Height : 10.059

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U3-ch120

calib_packv5_042523_0143.root, FC#4, port A2

Entries	365
Mean	45.09
Std Dev	10.9

Turn on : 27.8488

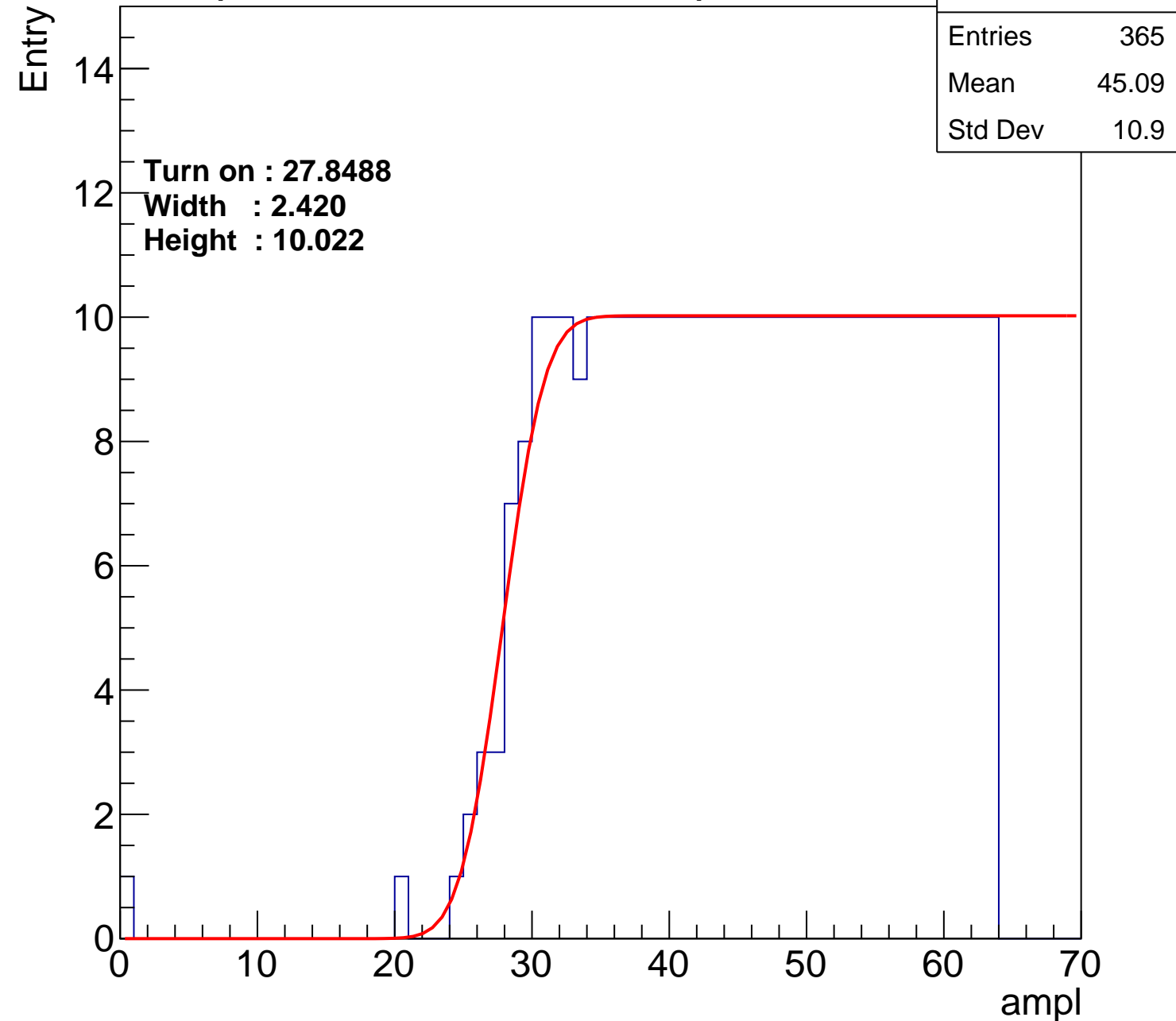
Width : 2.420

Height : 10.022

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U3-ch121

calib_packv5_042523_0143.root, FC#4, port A2

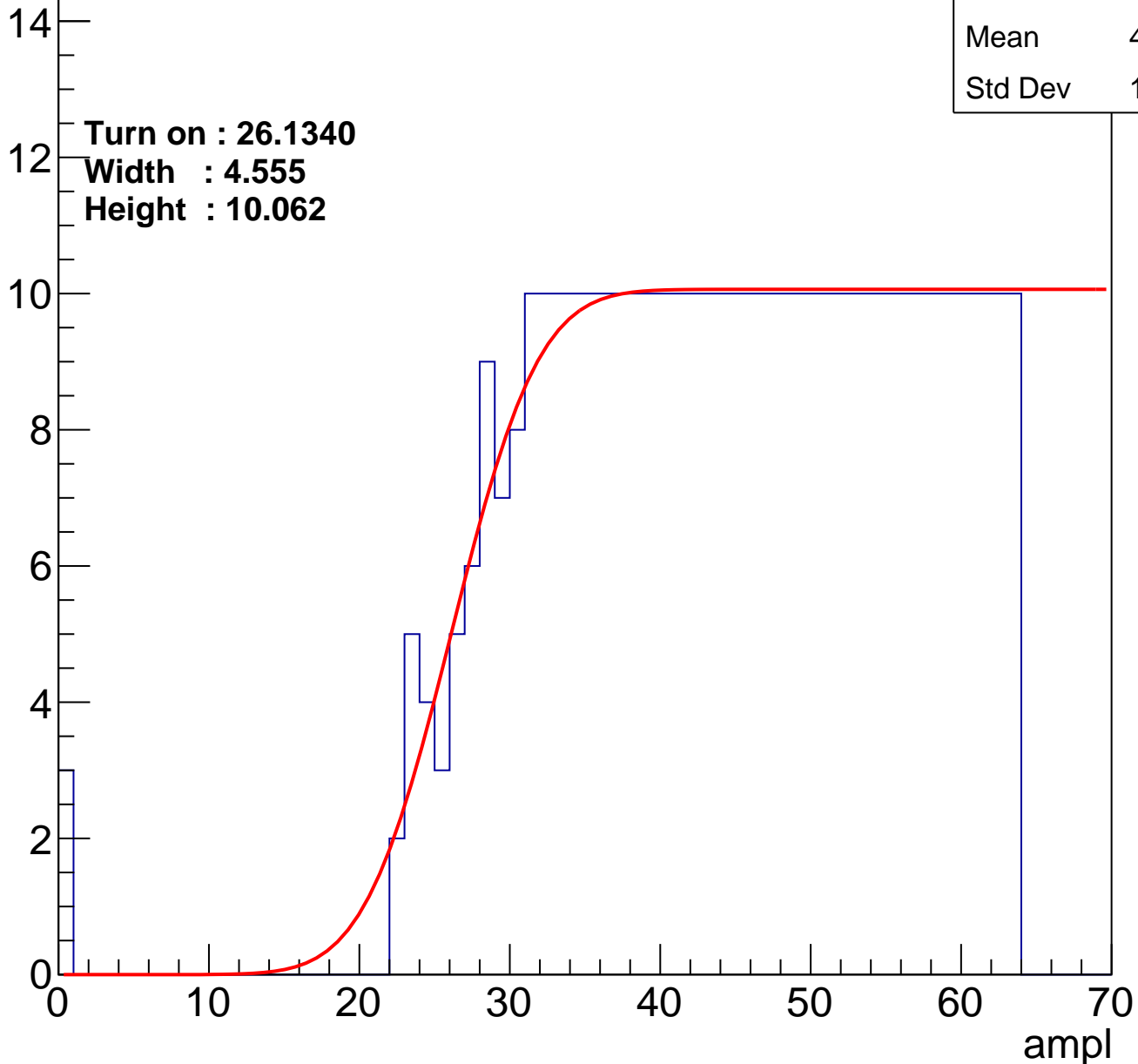
Entries	382
Mean	44.05
Std Dev	11.82

Turn on : 26.1340

Width : 4.555

Height : 10.062

Entry



B1L100S, U3-ch122

calib_packv5_042523_0143.root, FC#4, port A2

Entries	389
Mean	43.62
Std Dev	12.25

Turn on : 25.7992

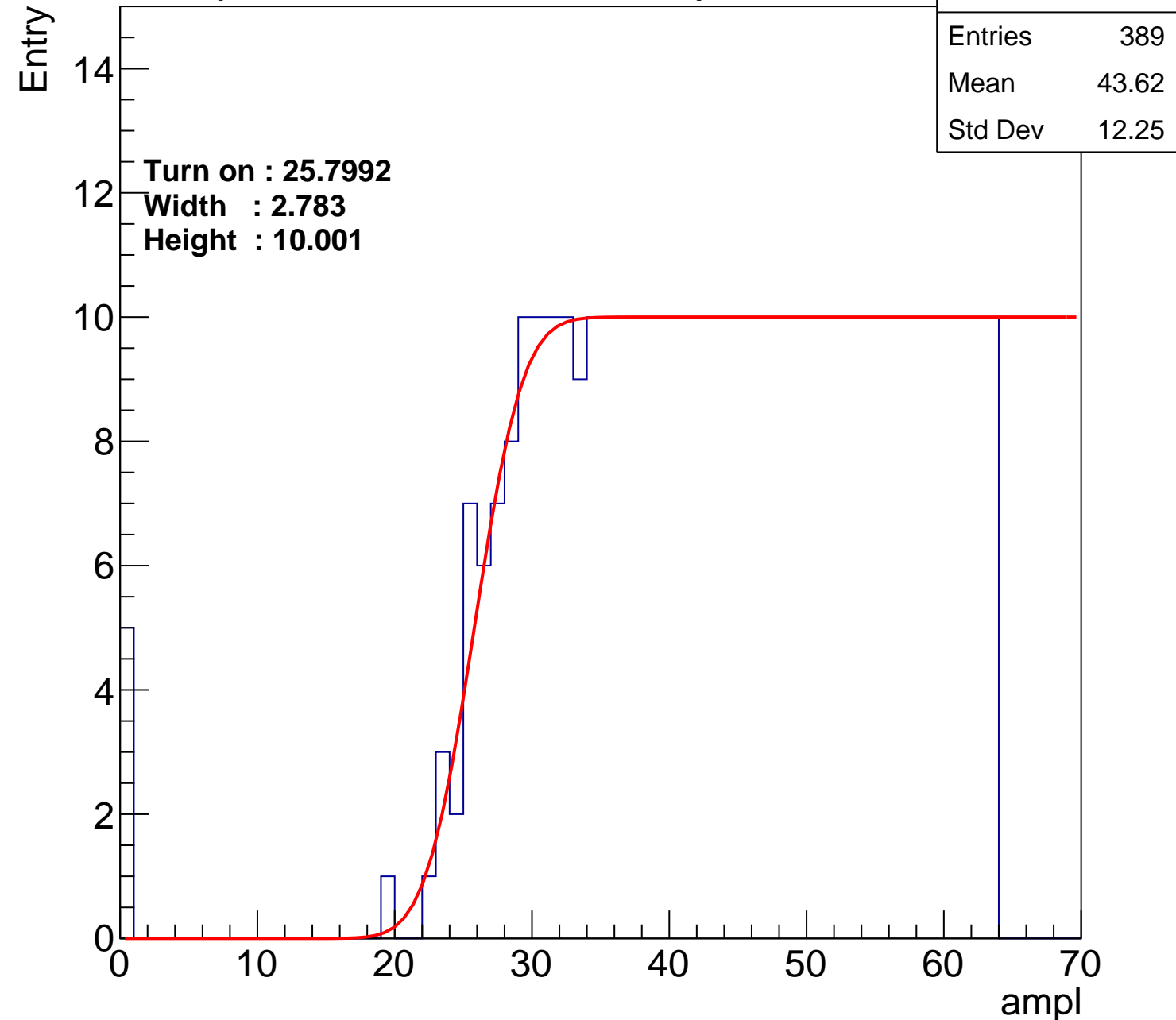
Width : 2.783

Height : 10.001

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U3-ch123

calib_packv5_042523_0143.root, FC#4, port A2

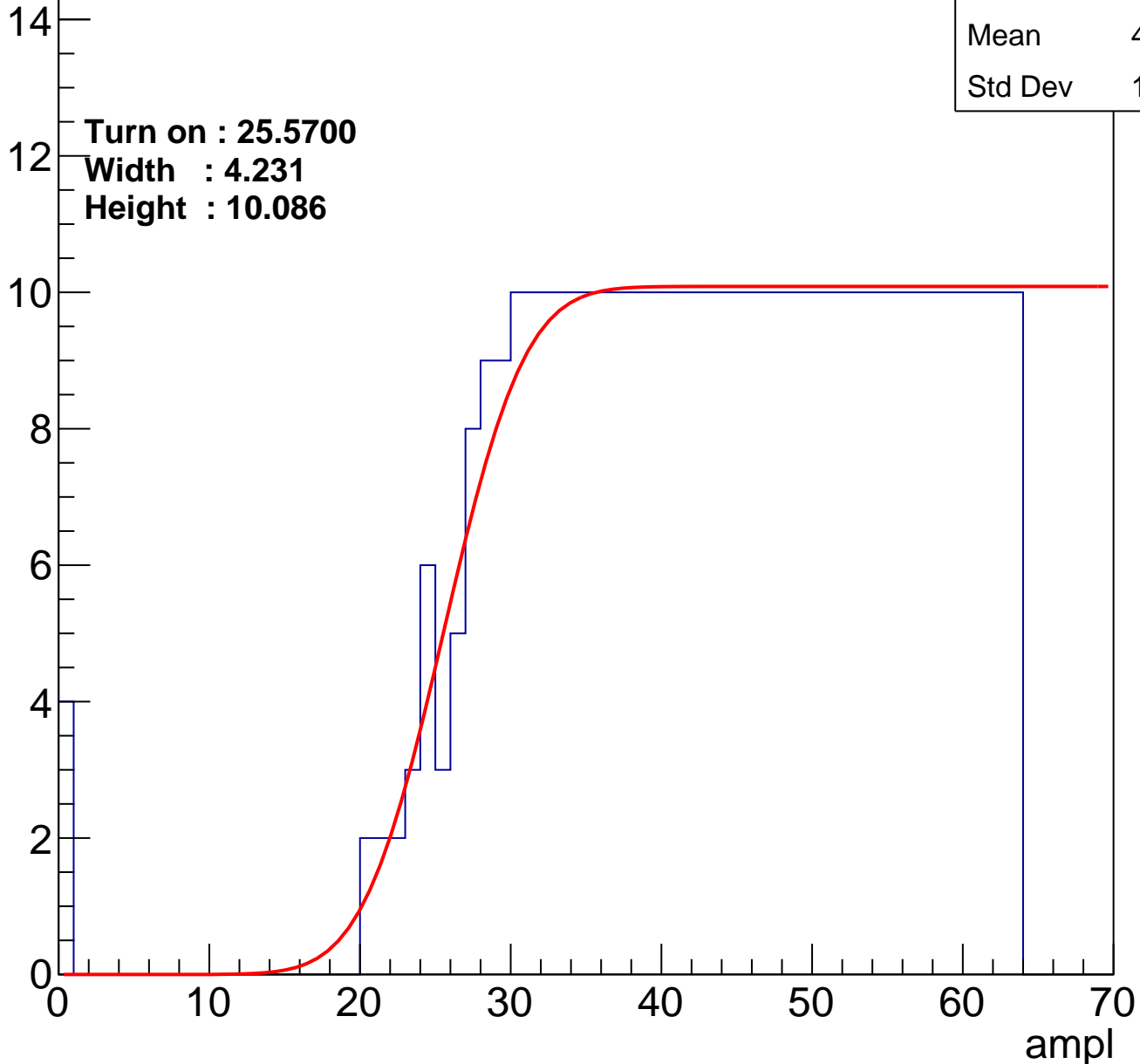
Entries	393
Mean	43.47
Std Dev	12.22

Turn on : 25.5700

Width : 4.231

Height : 10.086

Entry



B1L100S, U3-ch124

calib_packv5_042523_0143.root, FC#4, port A2

Entries	377
Mean	44.48
Std Dev	11.25

Turn on : 26.6603

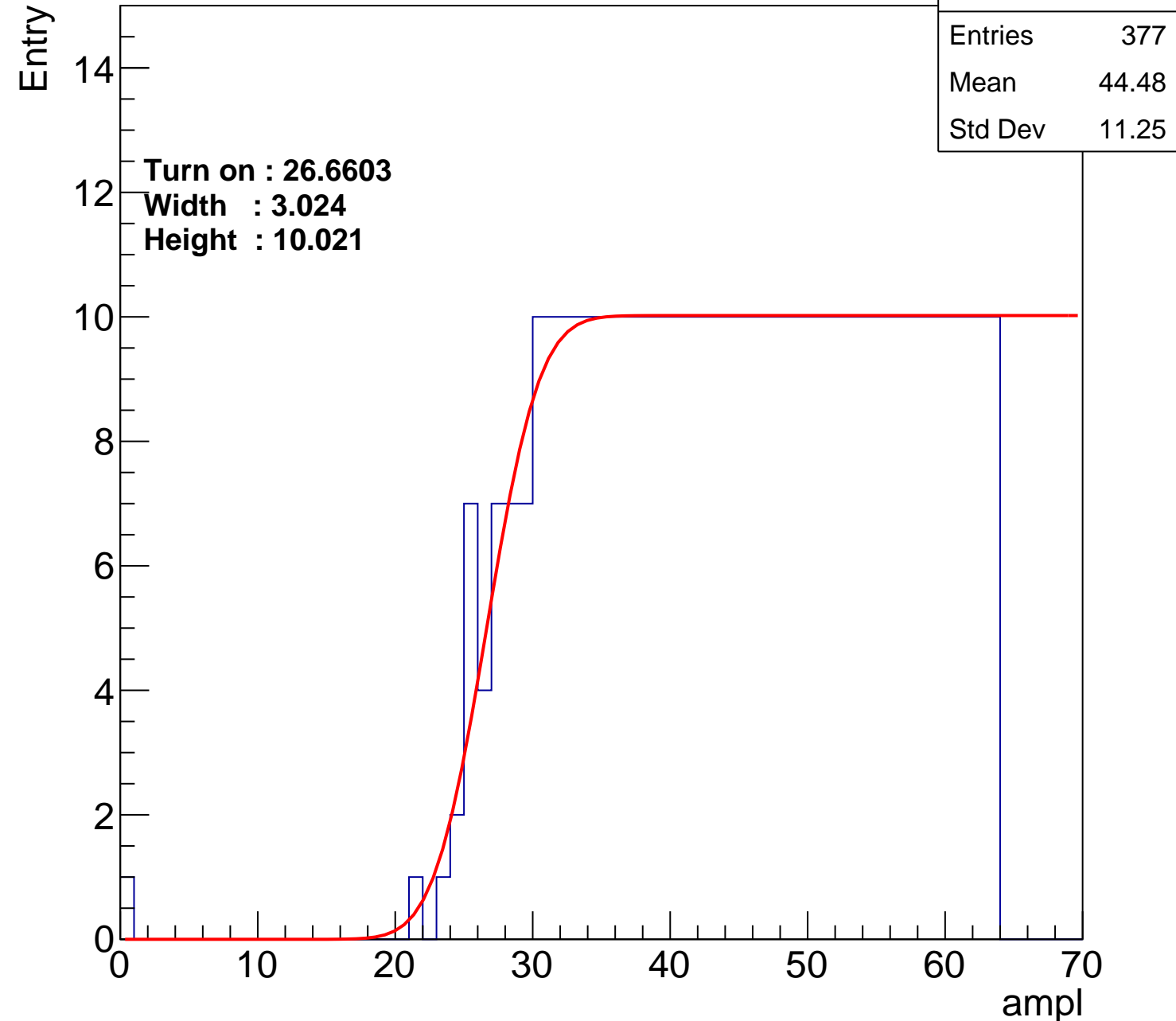
Width : 3.024

Height : 10.021

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U3-ch125

calib_packv5_042523_0143.root, FC#4, port A2

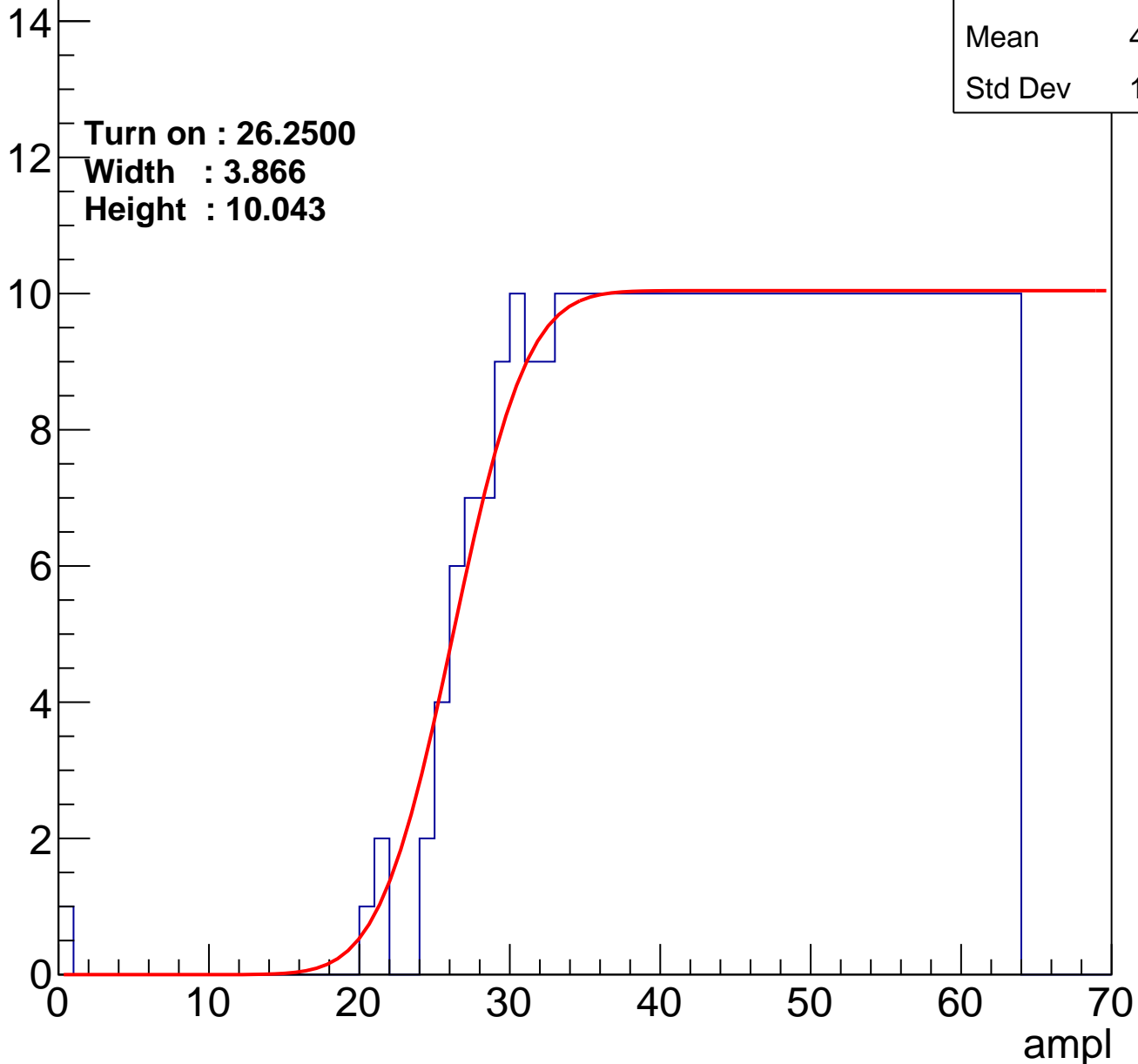
Entries	377
Mean	44.45
Std Dev	11.29

Turn on : 26.2500

Width : 3.866

Height : 10.043

Entry



B1L100S, U3-ch126

calib_packv5_042523_0143.root, FC#4, port A2

Entries	394
Mean	43.44
Std Dev	12.22

Turn on : 25.2945

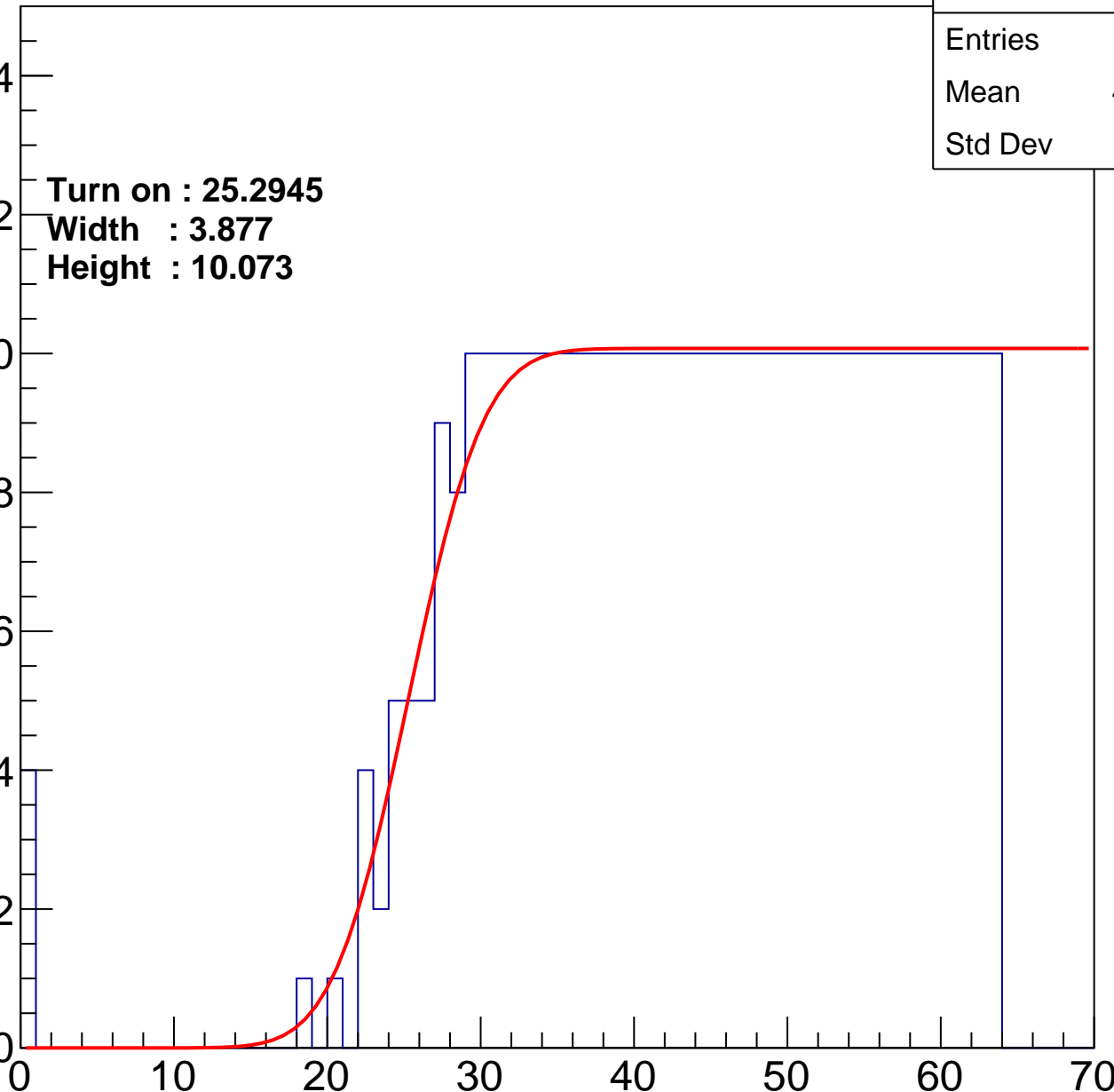
Width : 3.877

Height : 10.073

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U3-ch127

calib_packv5_042523_0143.root, FC#4, port A2

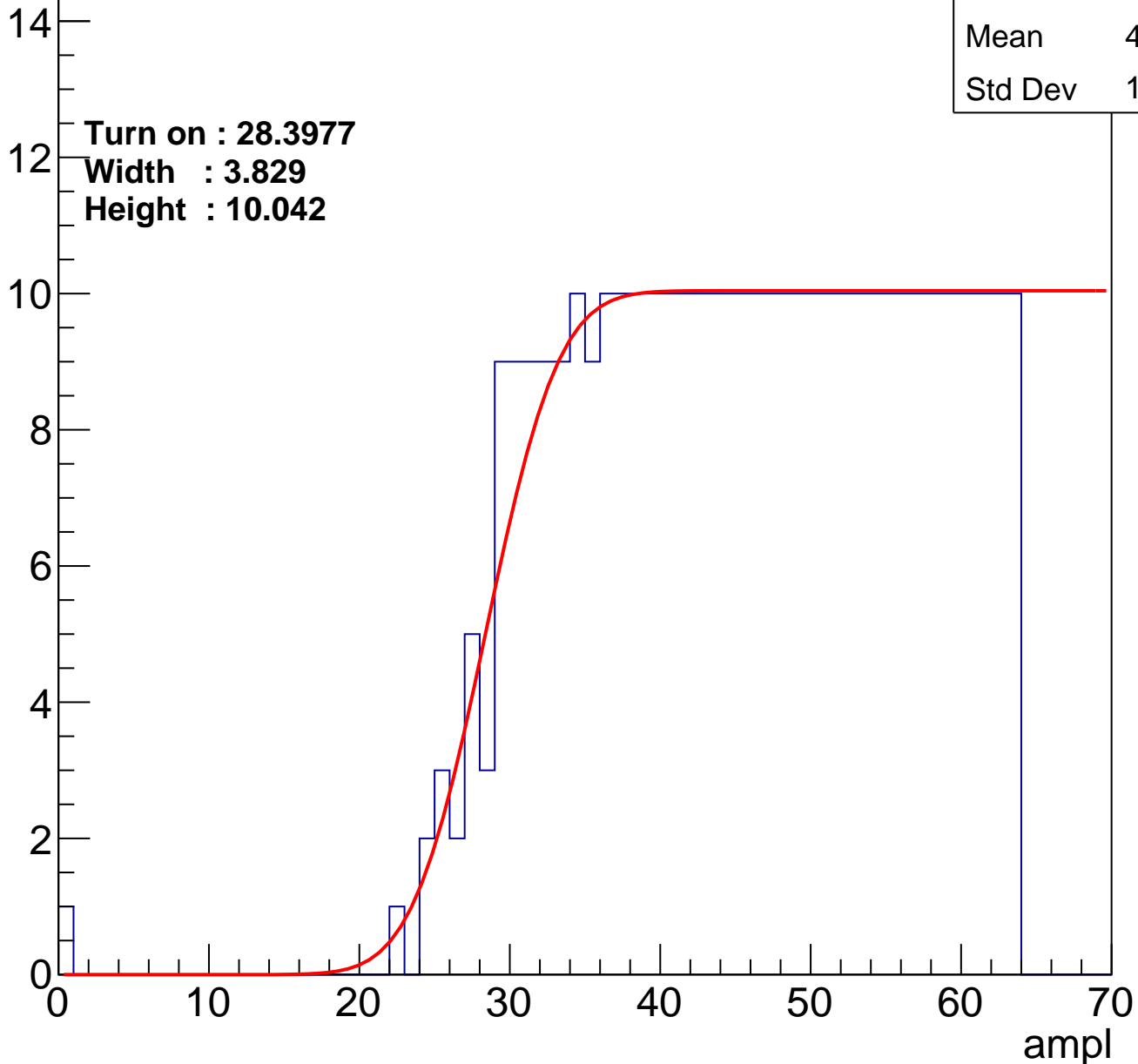
Entries	361
Mean	45.22
Std Dev	10.89

Turn on : 28.3977

Width : 3.829

Height : 10.042

Entry



B1L100S, U3-ch127

calib_packv5_042523_0143.root, FC#4, port A2

Entries	361
Mean	45.22
Std Dev	10.89

Turn on : 28.3977

Width : 3.829

Height : 10.042

Entry

14
12
10
8
6
4
2
0

ampl

