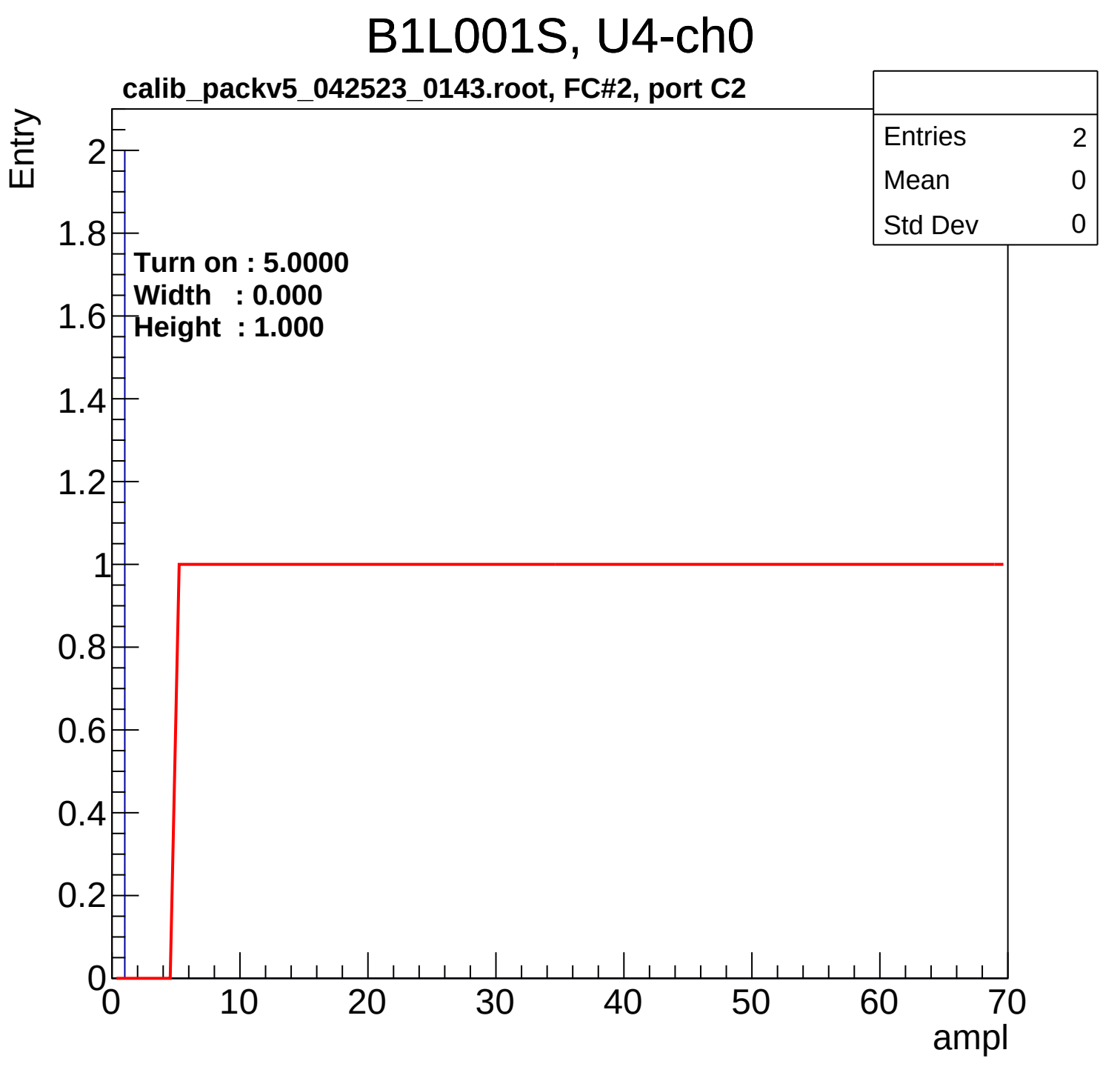
B1L001S, U4-ch0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
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40
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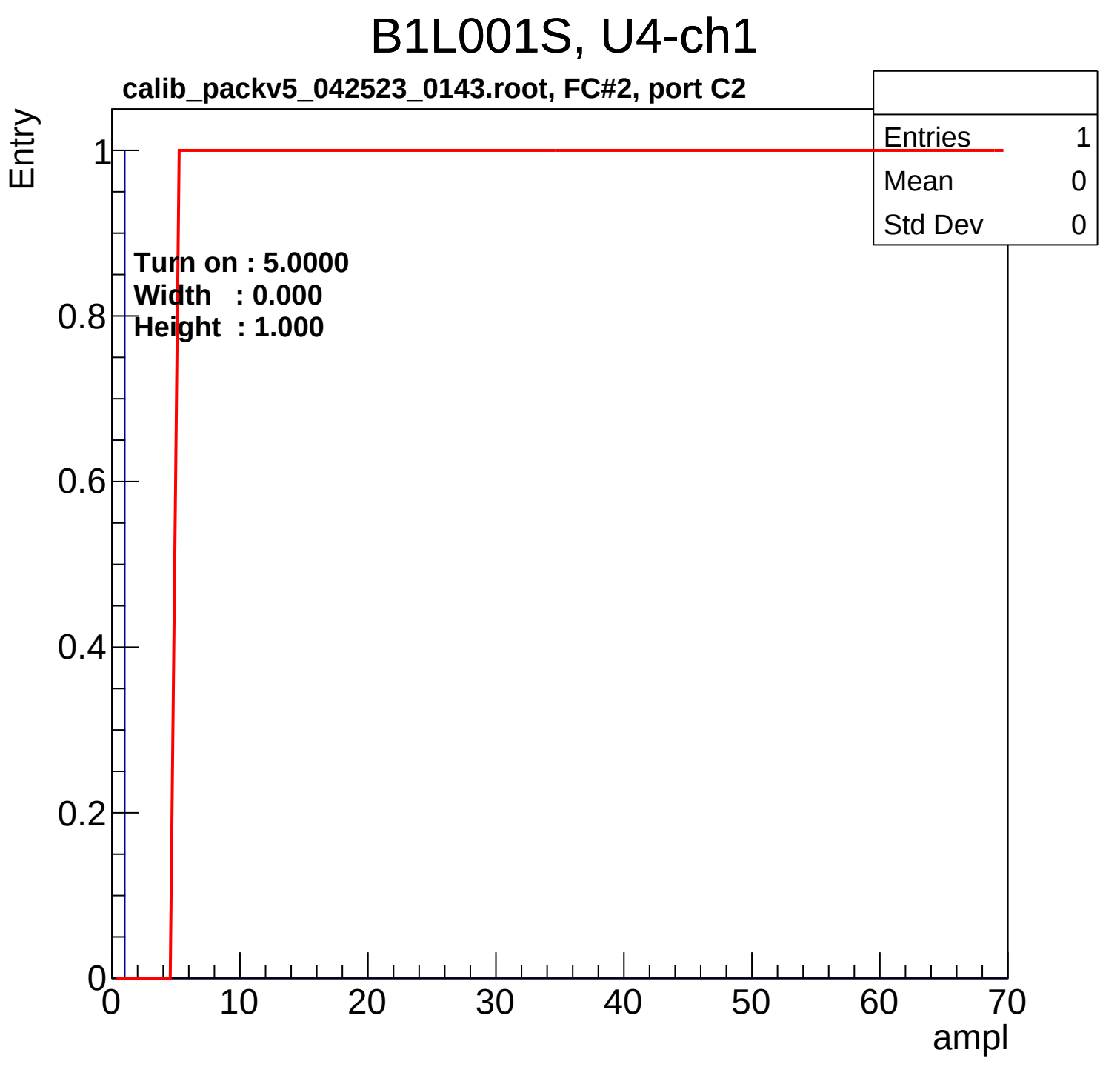
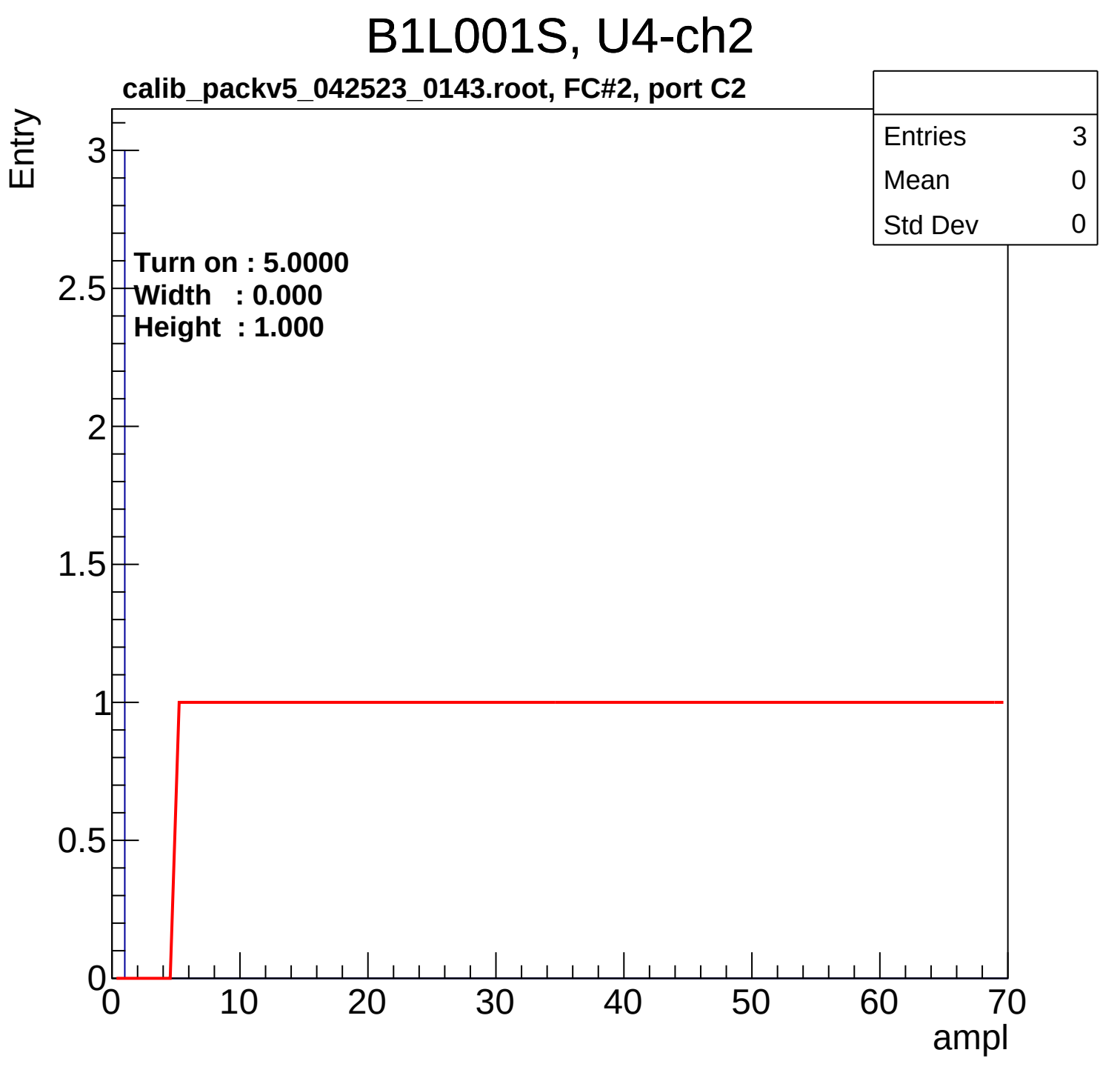
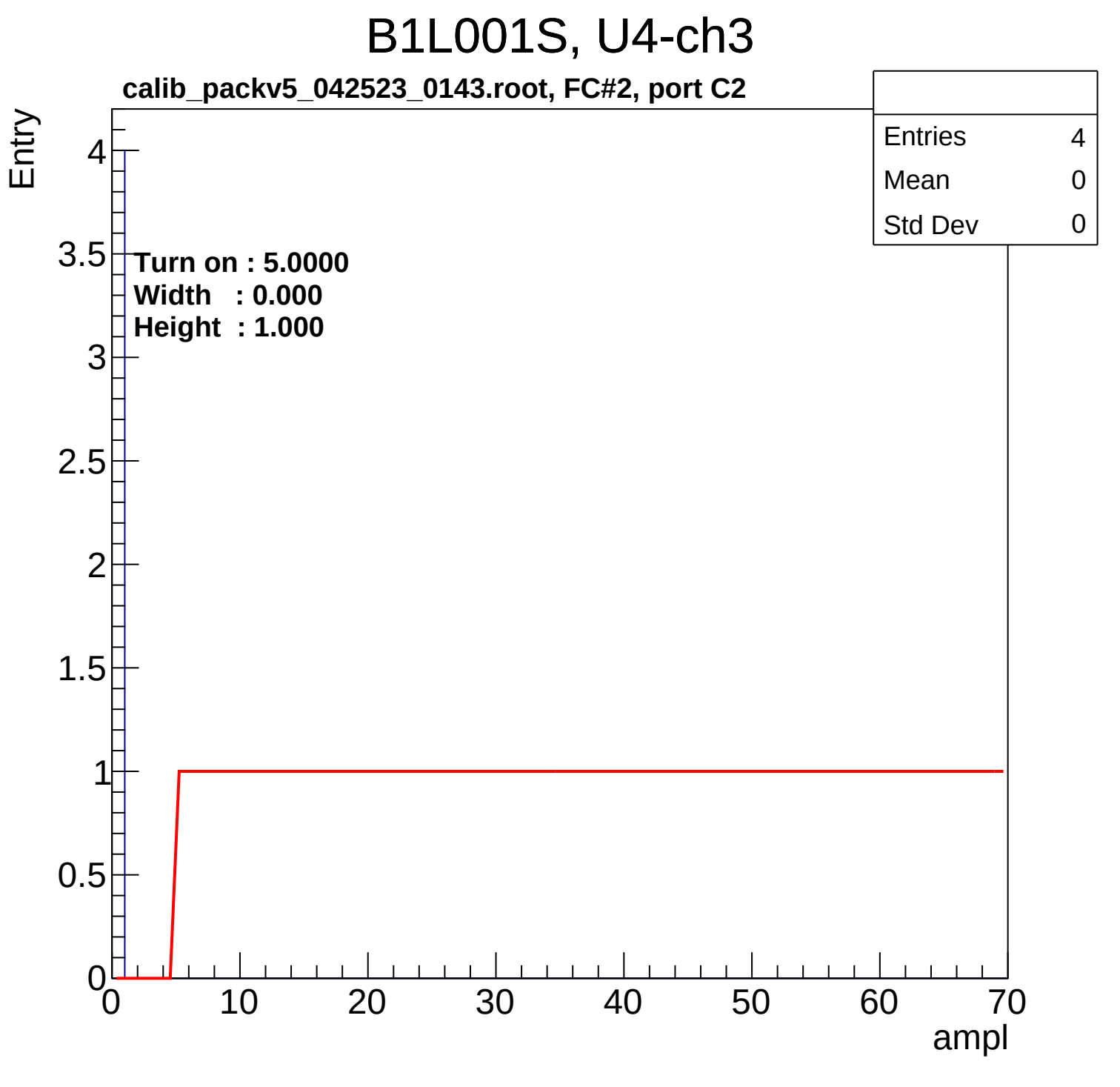
60
70


B1L001S, U4-ch1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L001S, U4-ch2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 3
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L001S, U4-ch3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 4
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
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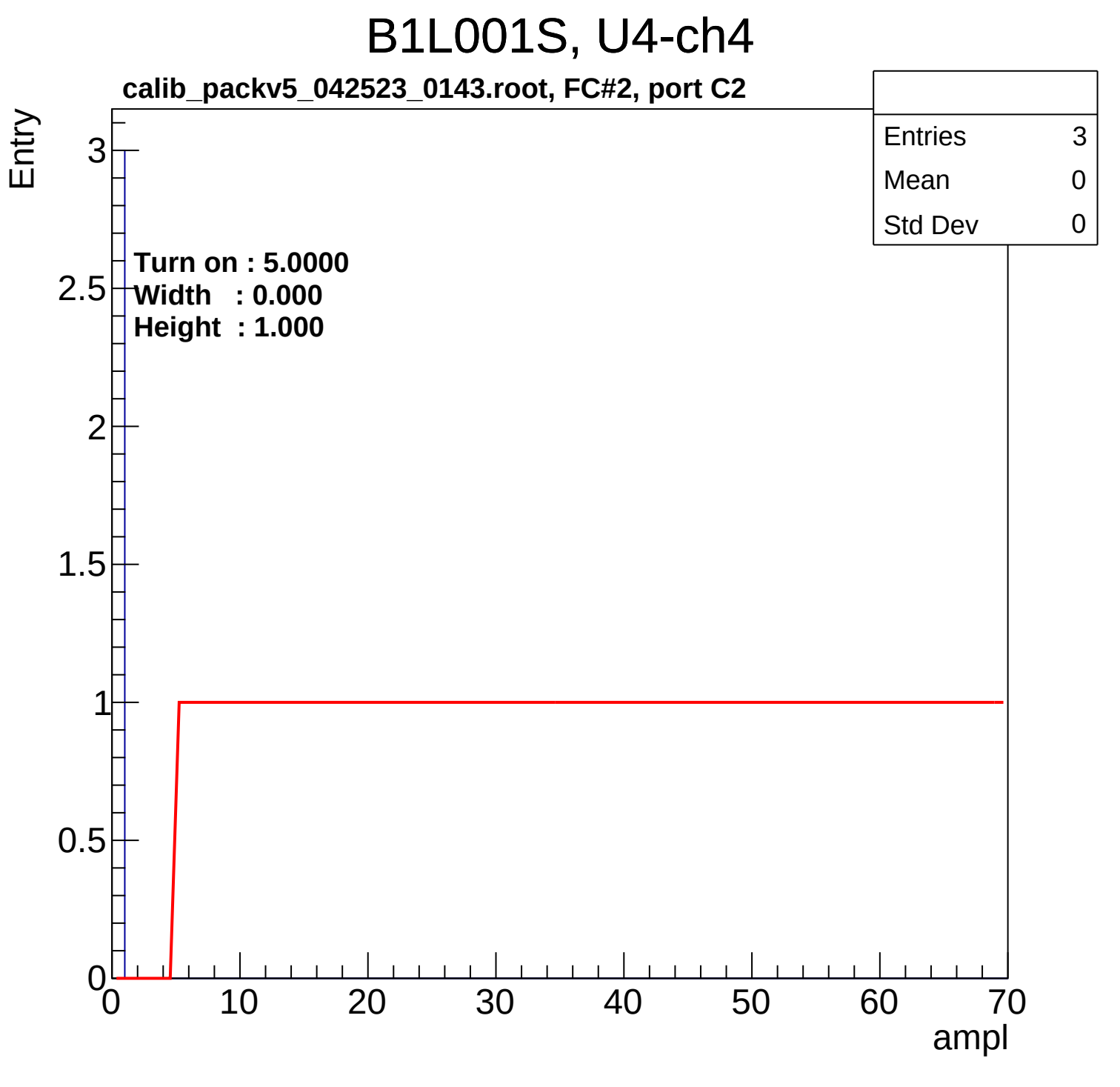
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L001S, U4-ch4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 3
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
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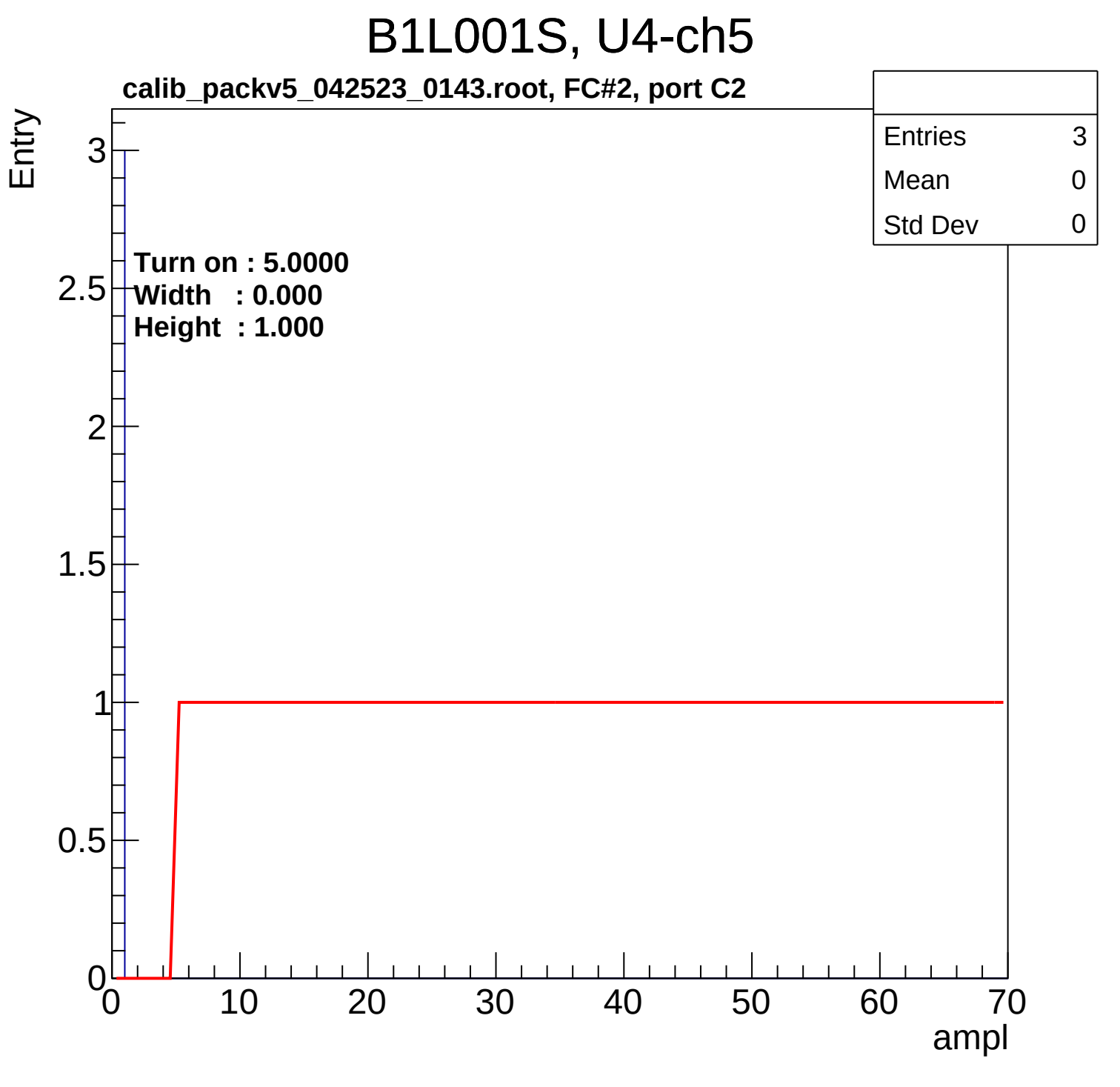
B1L001S, U4-ch5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 3
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
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40
50
60
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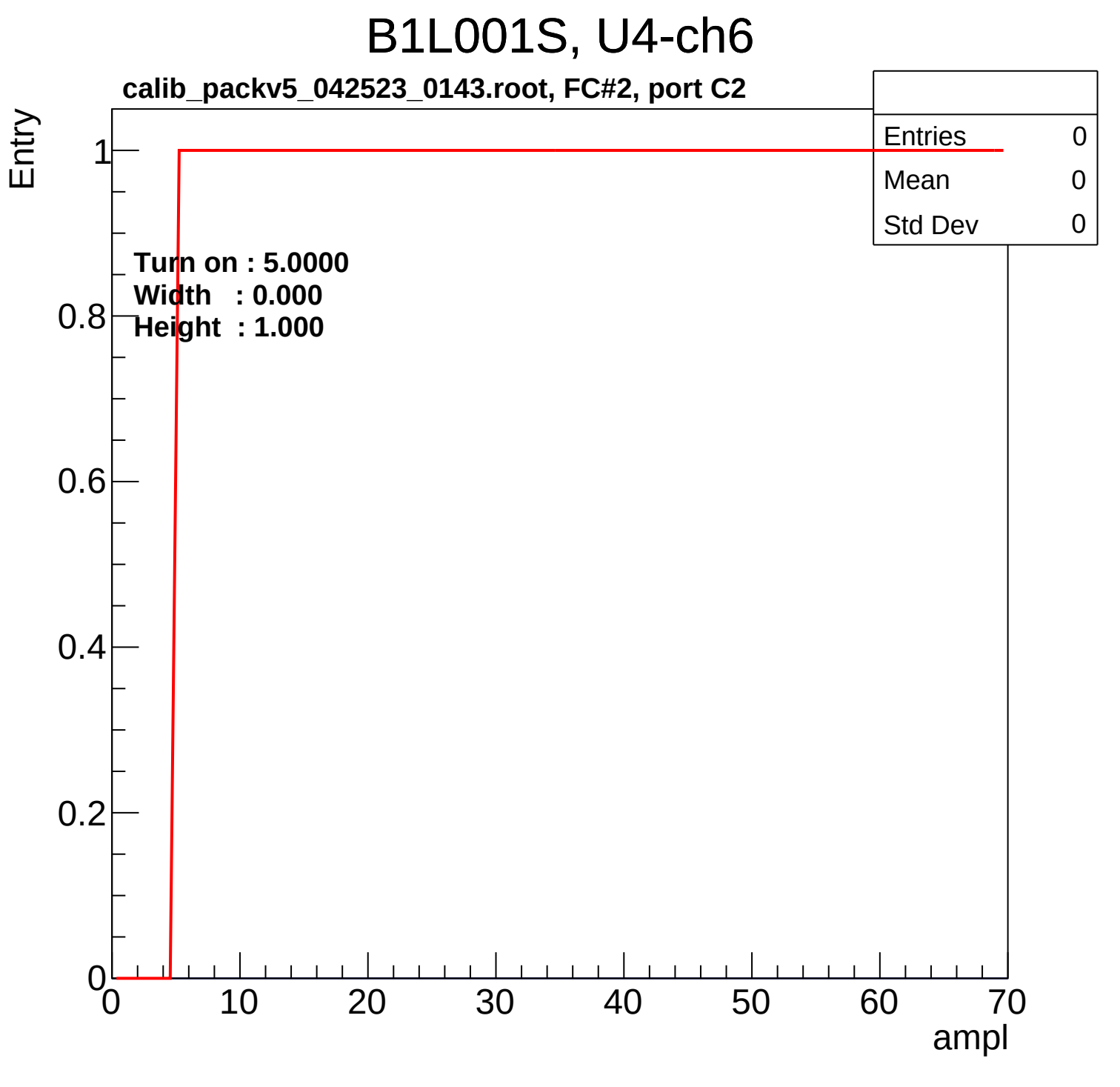
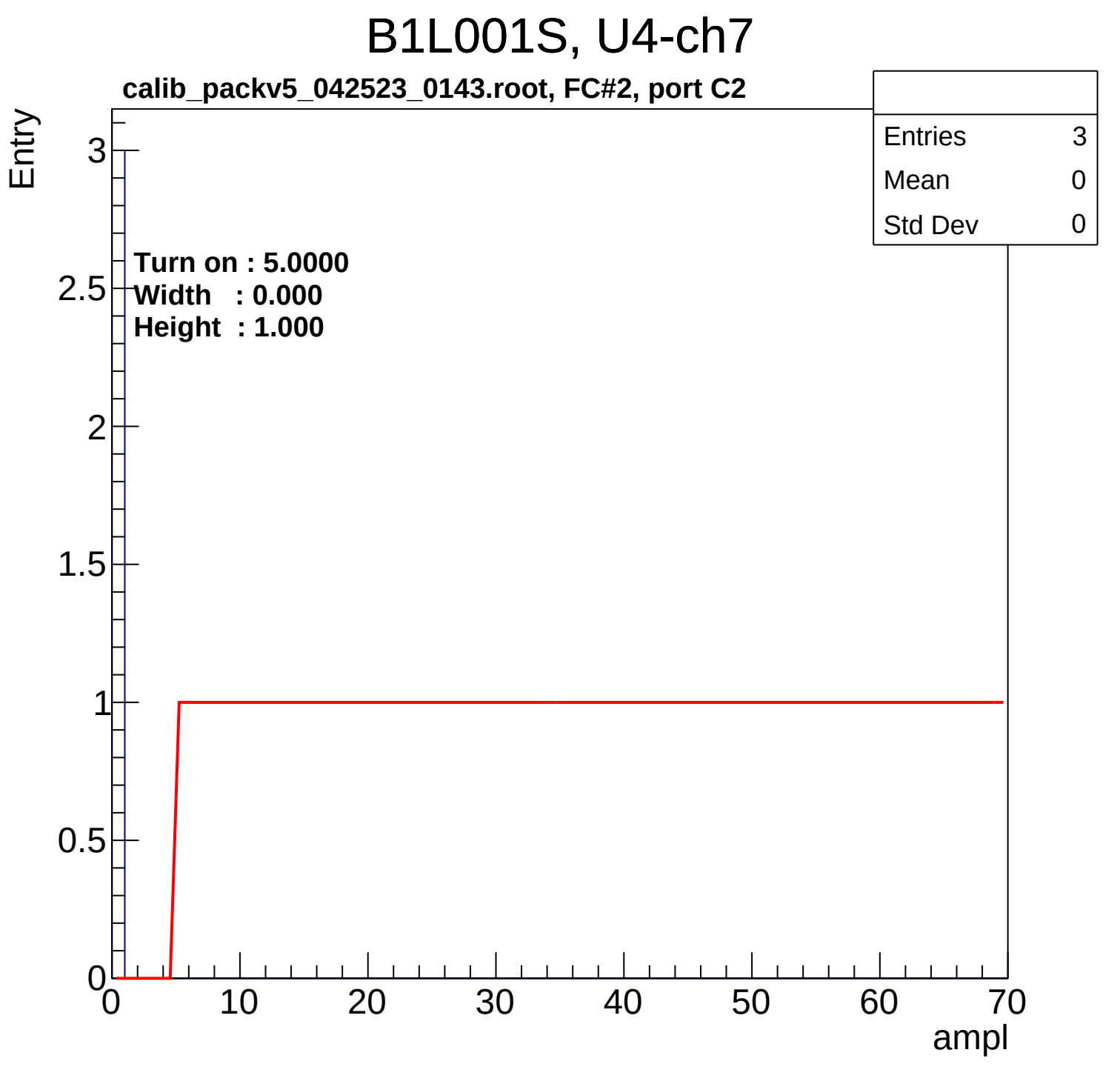
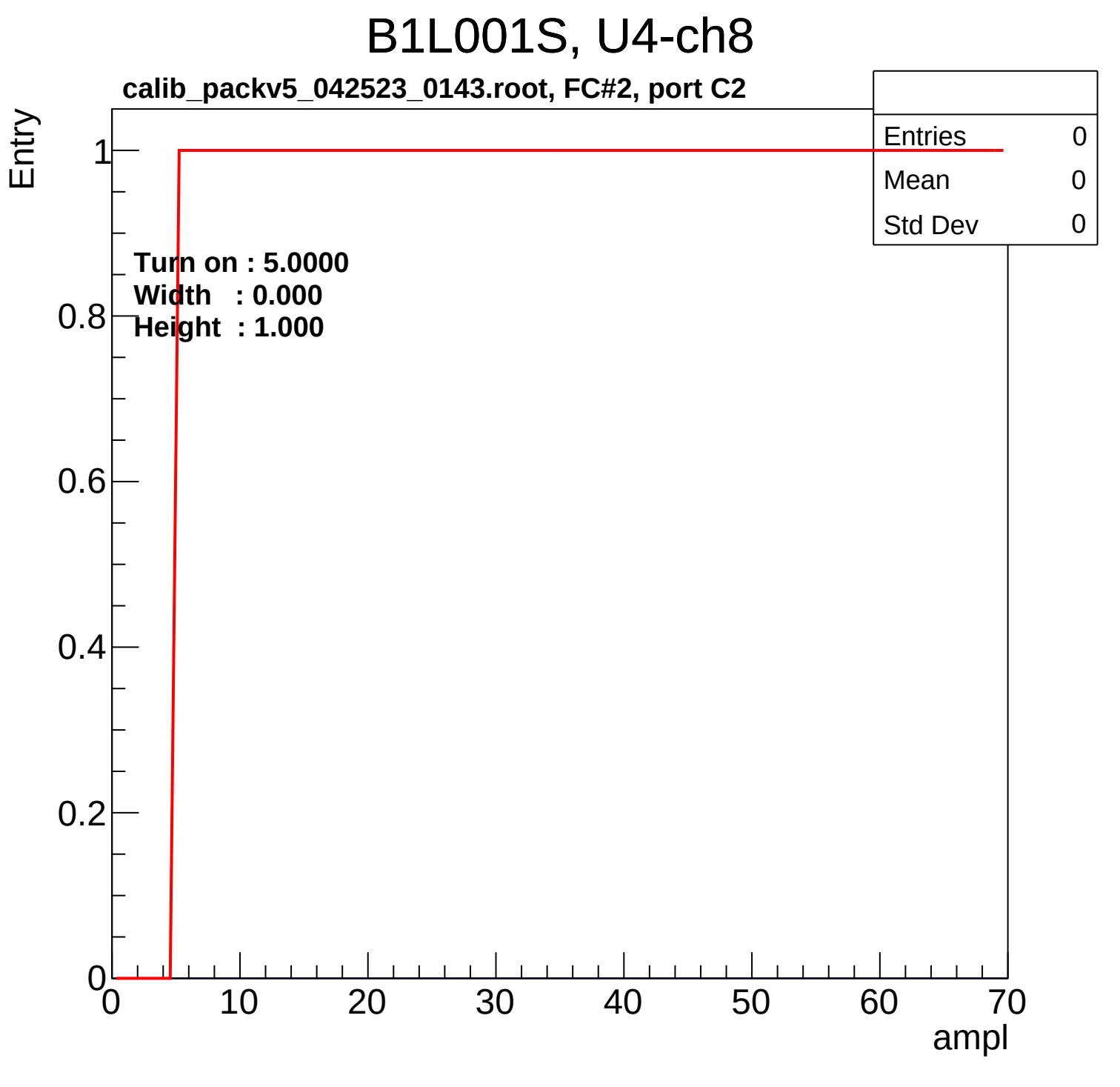
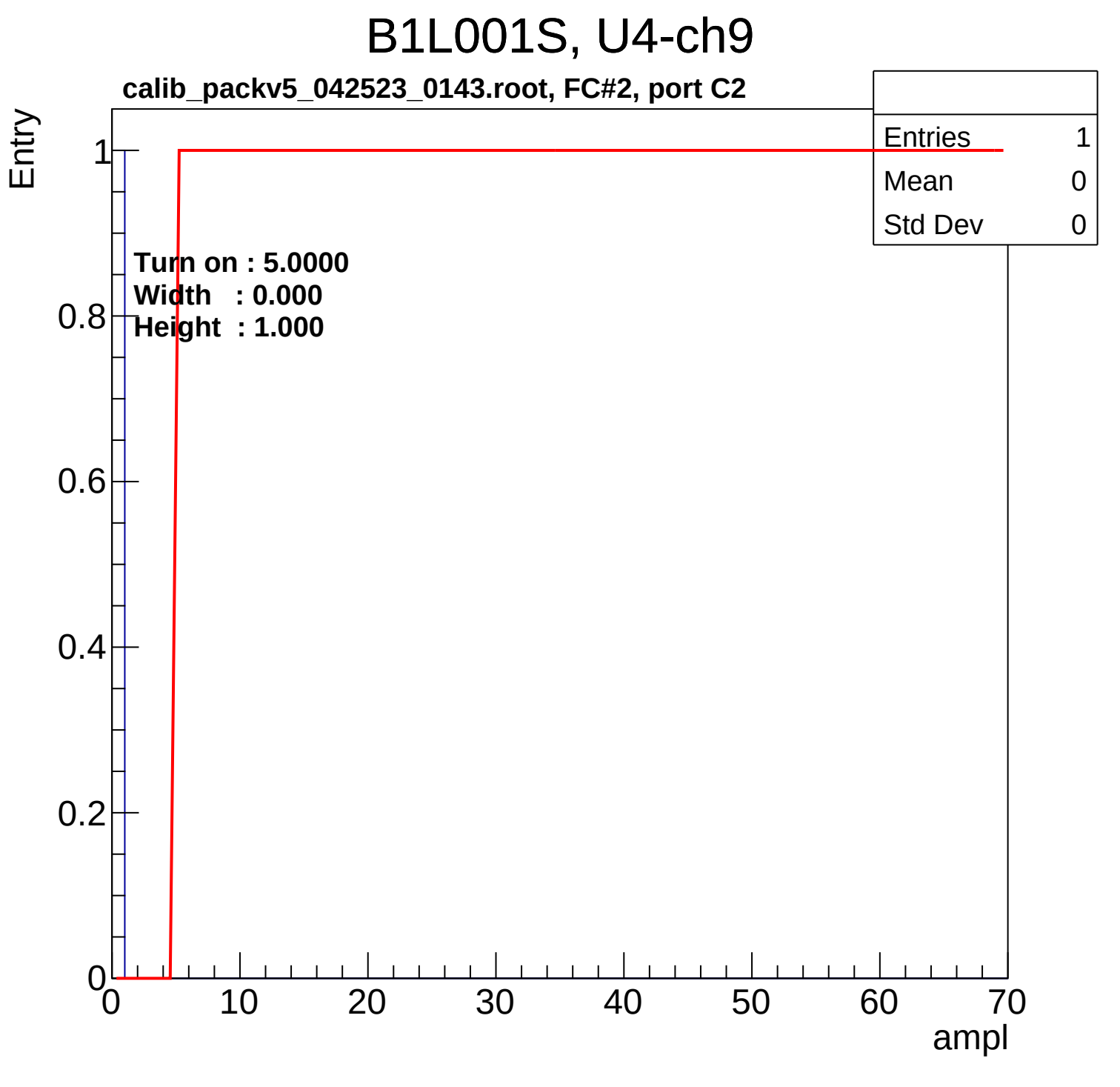
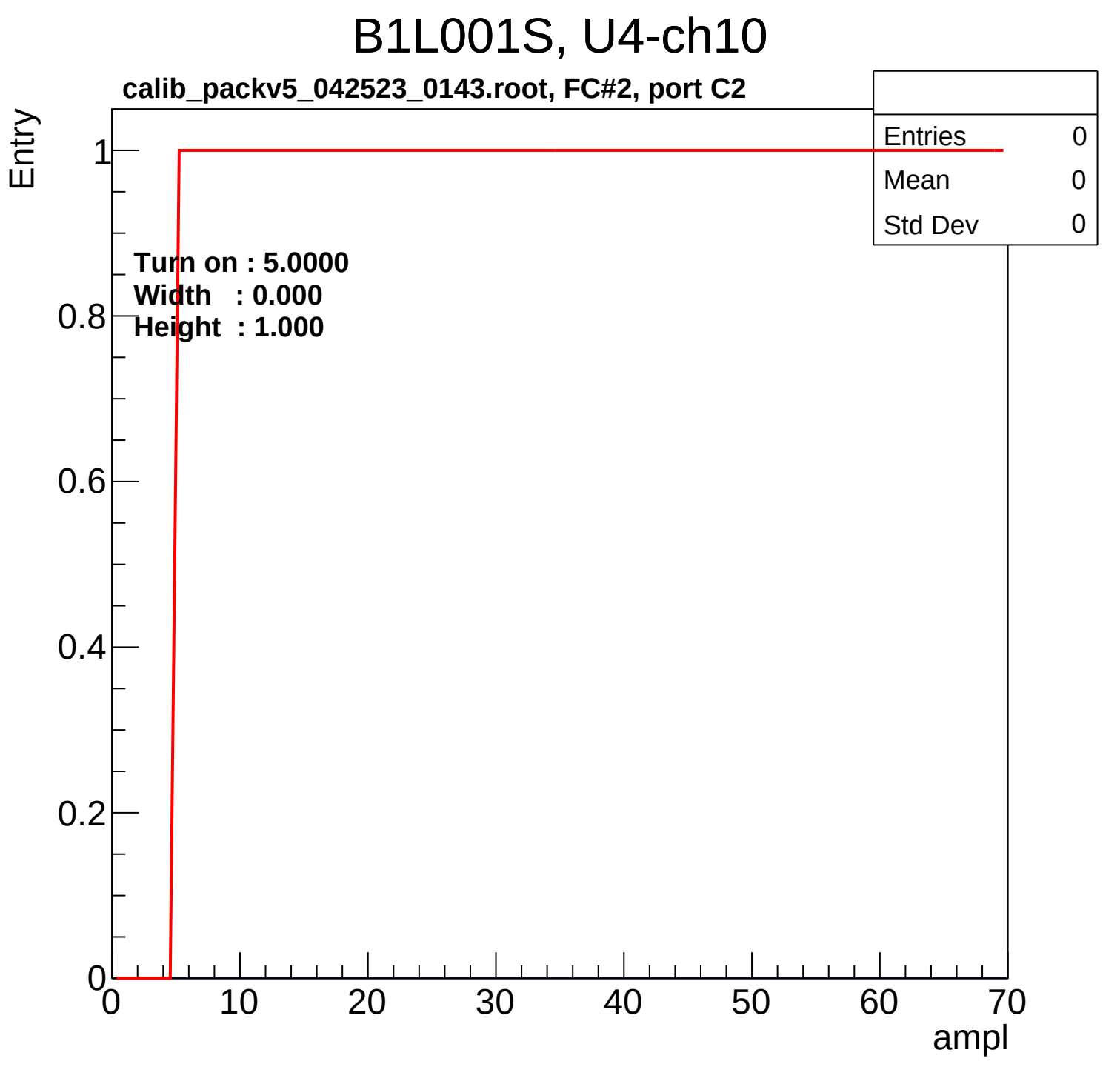
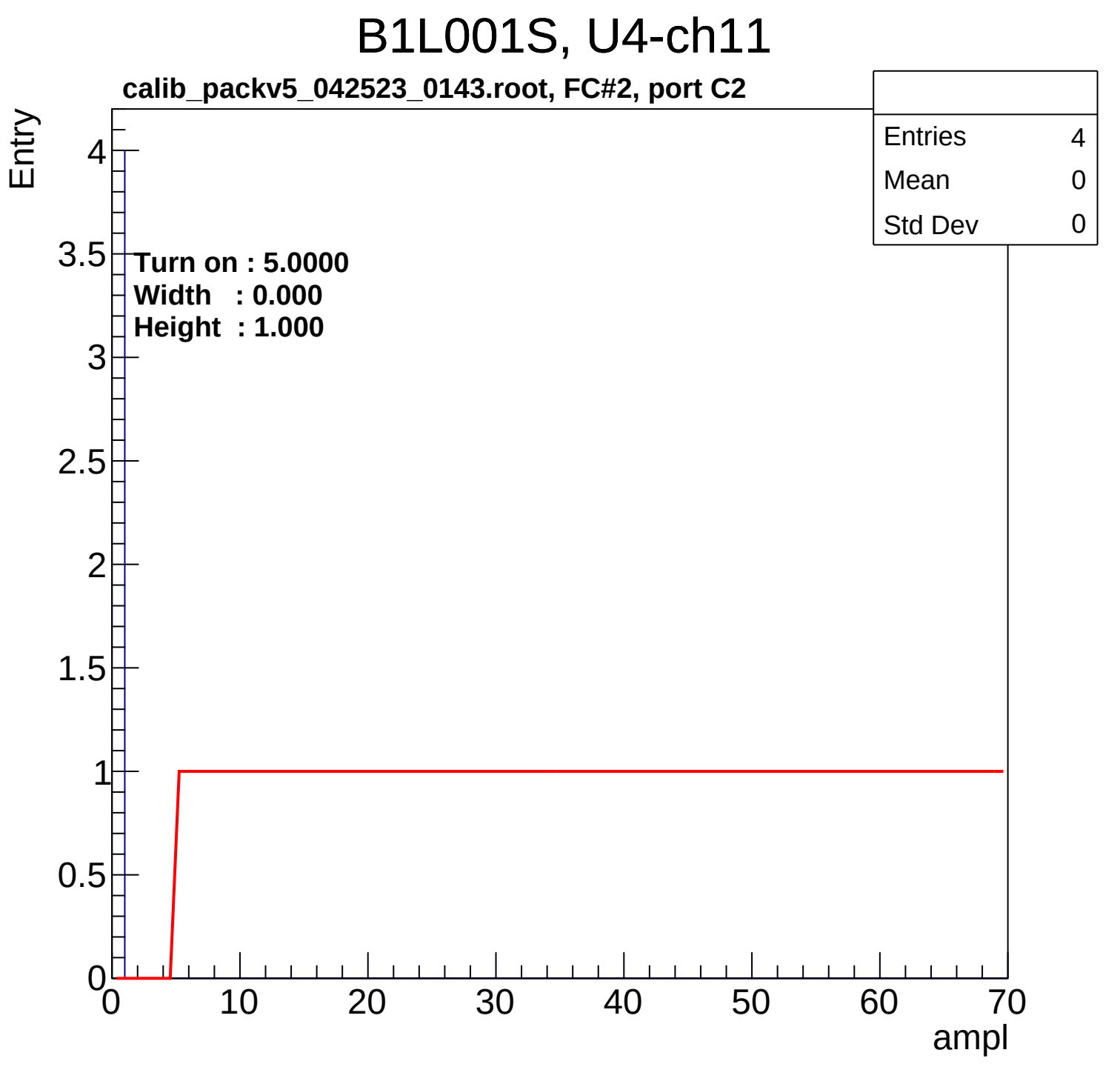

B1L001S, U4-ch6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L001S, U4-ch7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 3
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L001S, U4-ch8
calib_packv5_042523_0143.root, FC#2, port C2
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L001S, U4-ch9
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L001S, U4-ch10
calib_packv5_042523_0143.root, FC#2, port C2
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L001S, U4-ch11
calib_packv5_042523_0143.root, FC#2, port C2
Entries 4
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
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20
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40
50
60
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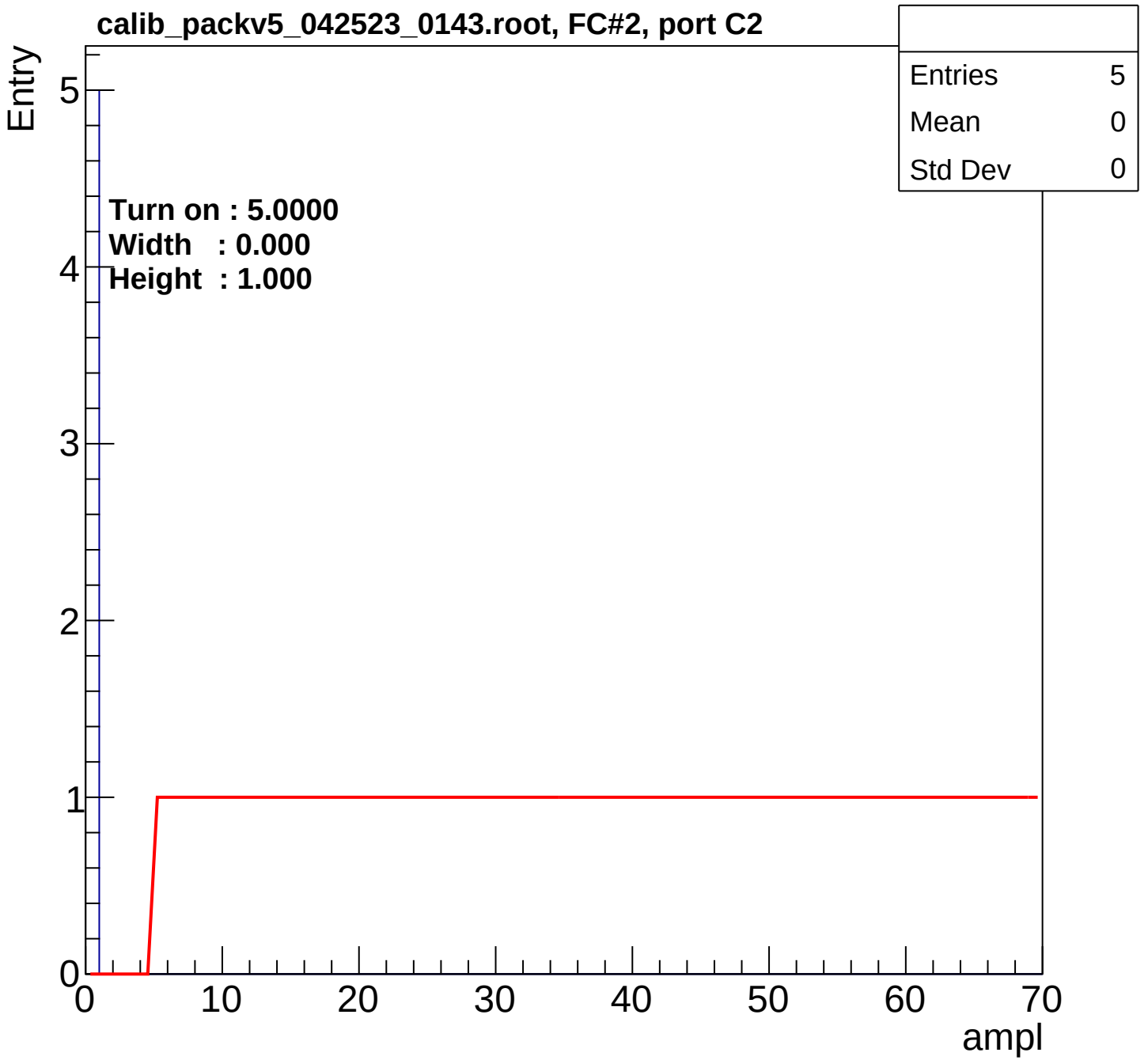
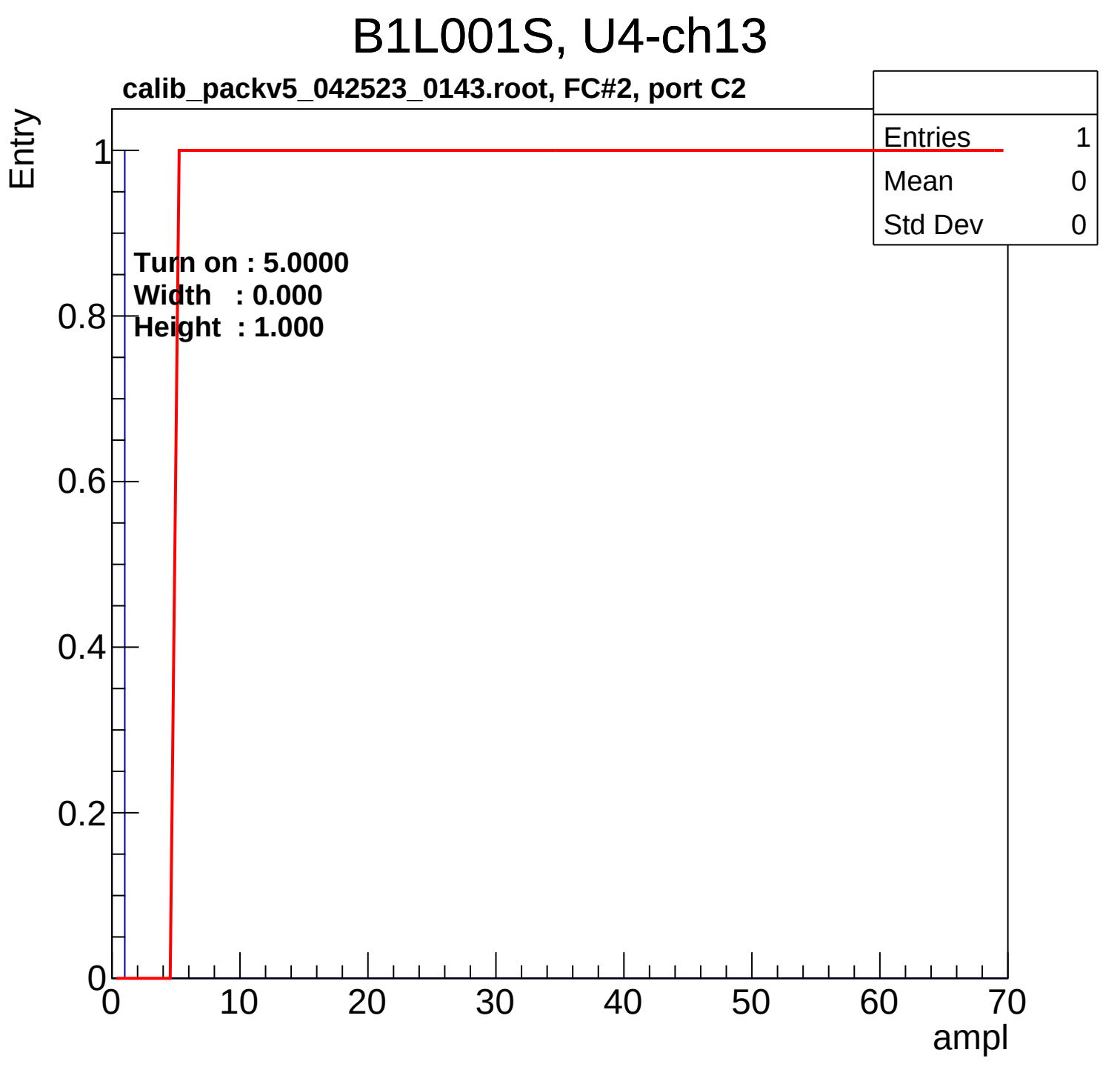
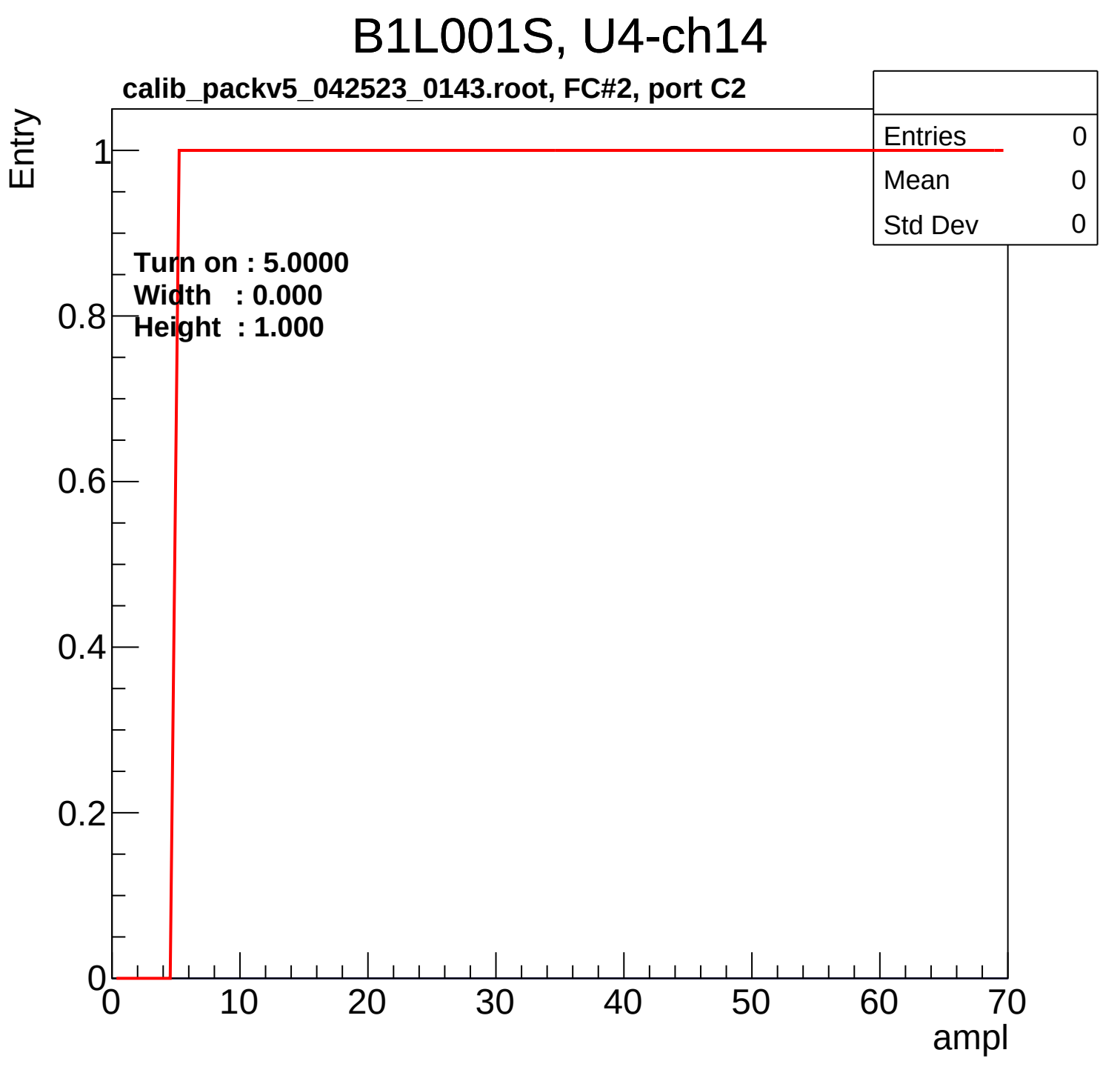

B1L001S, U4-ch12
calib_packv5_042523_0143.root, FC#2, port C2
Entries 5
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L001S, U4-ch13
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L001S, U4-ch14
calib_packv5_042523_0143.root, FC#2, port C2
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
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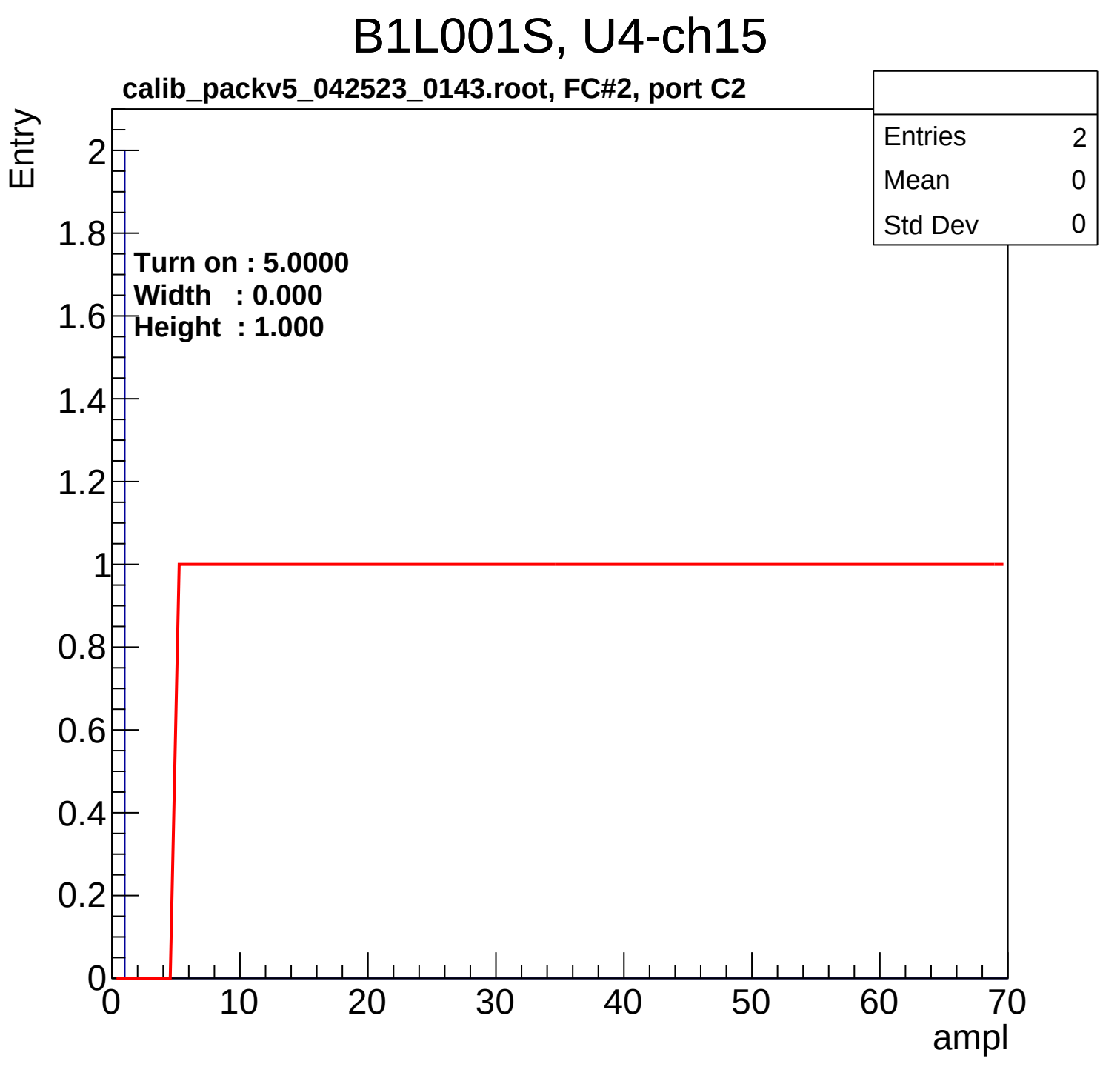
0
0
10
20
30
40
50
60
70
ampl


B1L001S, U4-ch15
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
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60
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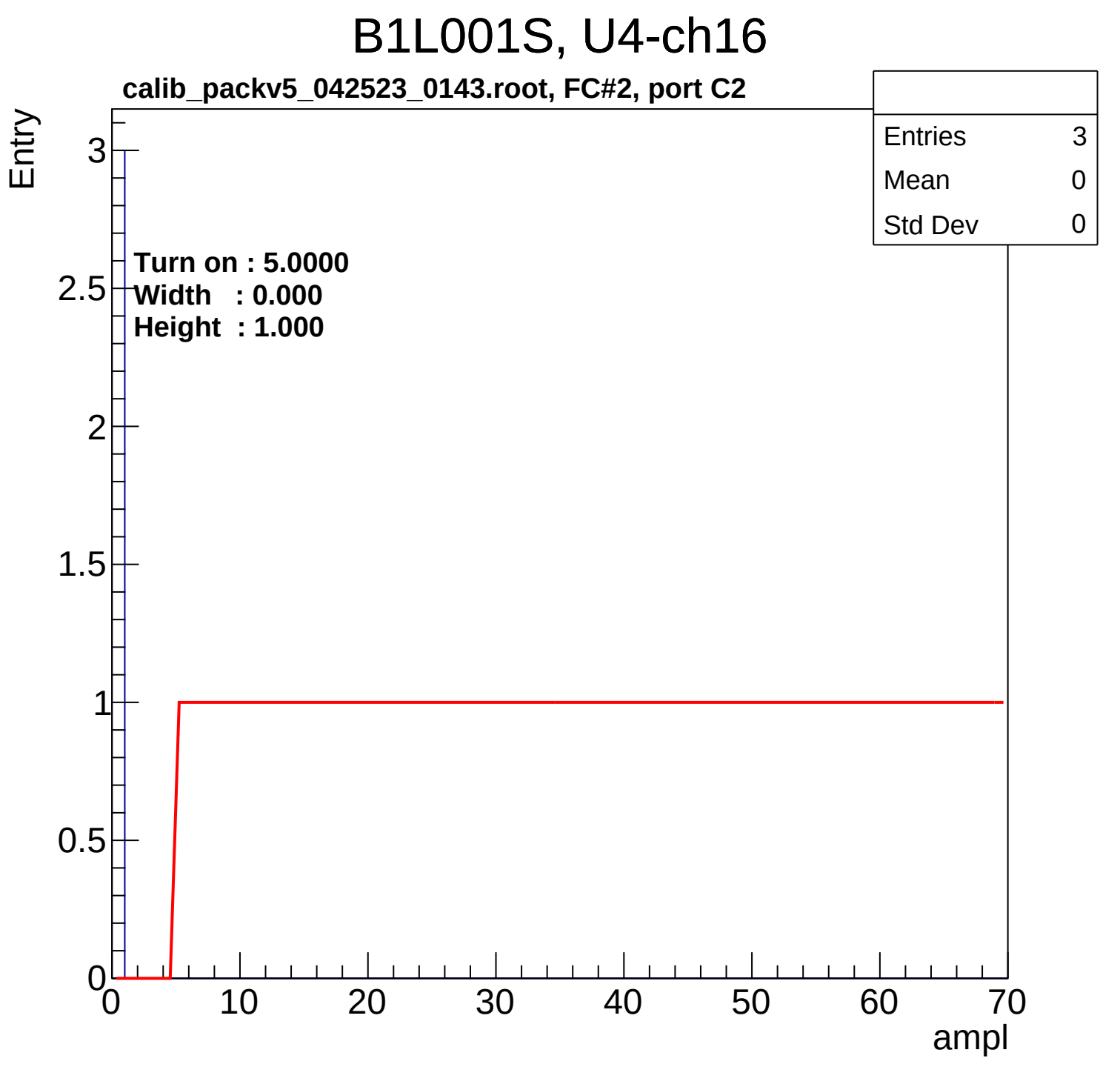
B1L001S, U4-ch16
calib_packv5_042523_0143.root, FC#2, port C2
Entries 3
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
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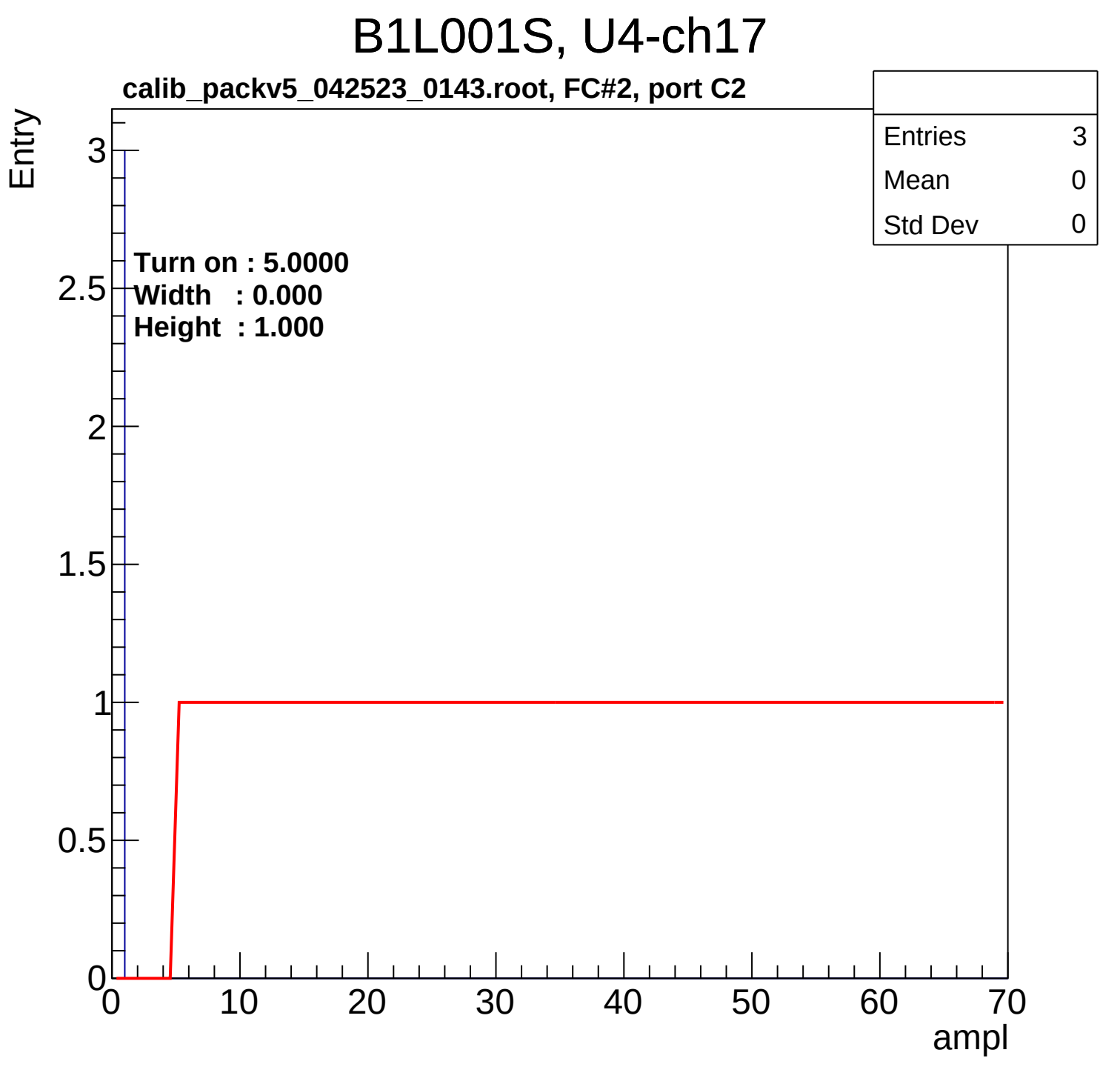
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L001S, U4-ch17
calib_packv5_042523_0143.root, FC#2, port C2
Entries 3
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
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20
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60
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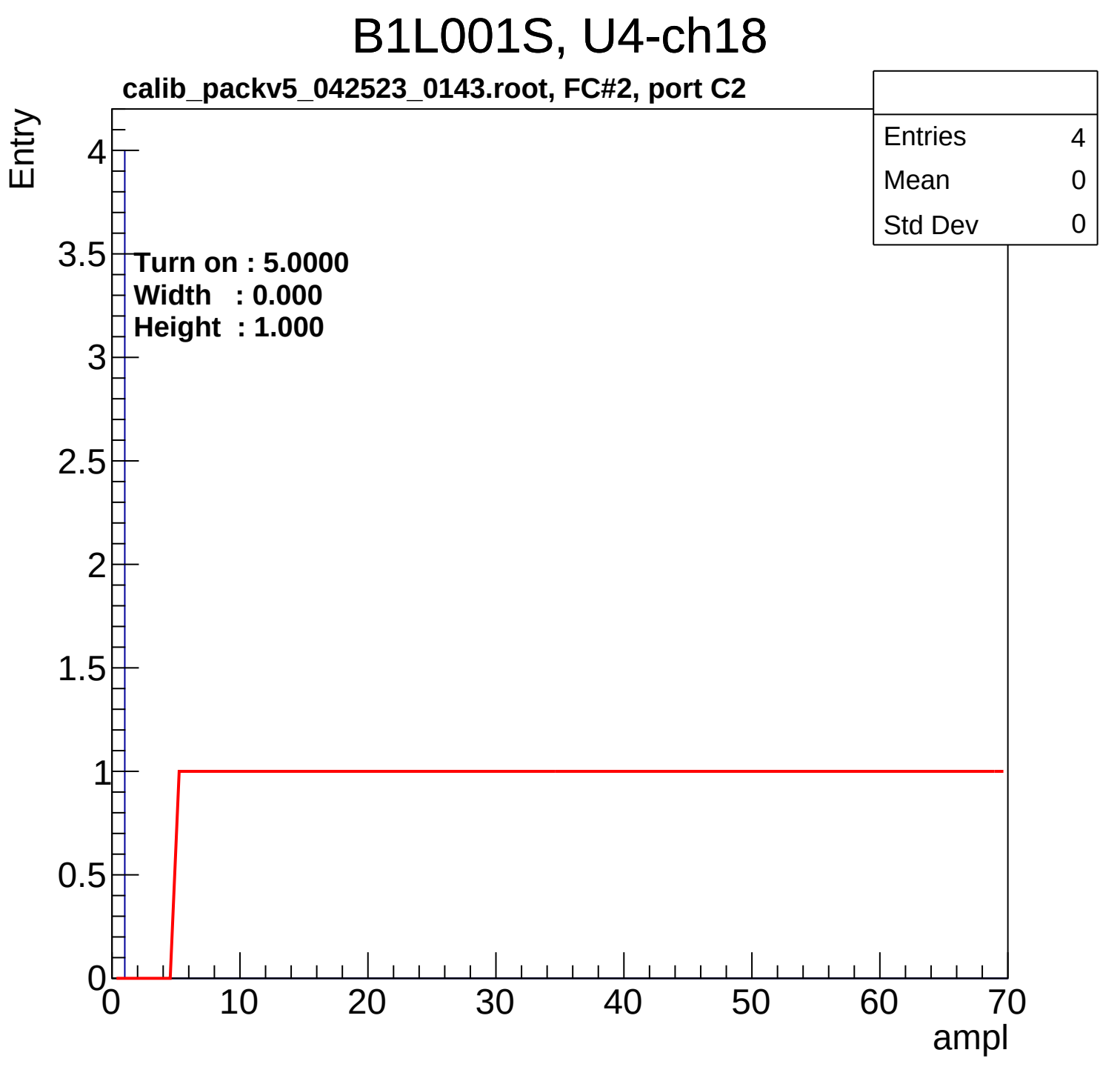
B1L001S, U4-ch18
calib_packv5_042523_0143.root, FC#2, port C2
Entries 4
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
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0.5
1
1.5
2
2.5
3
3.5
4
0
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20
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40
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60
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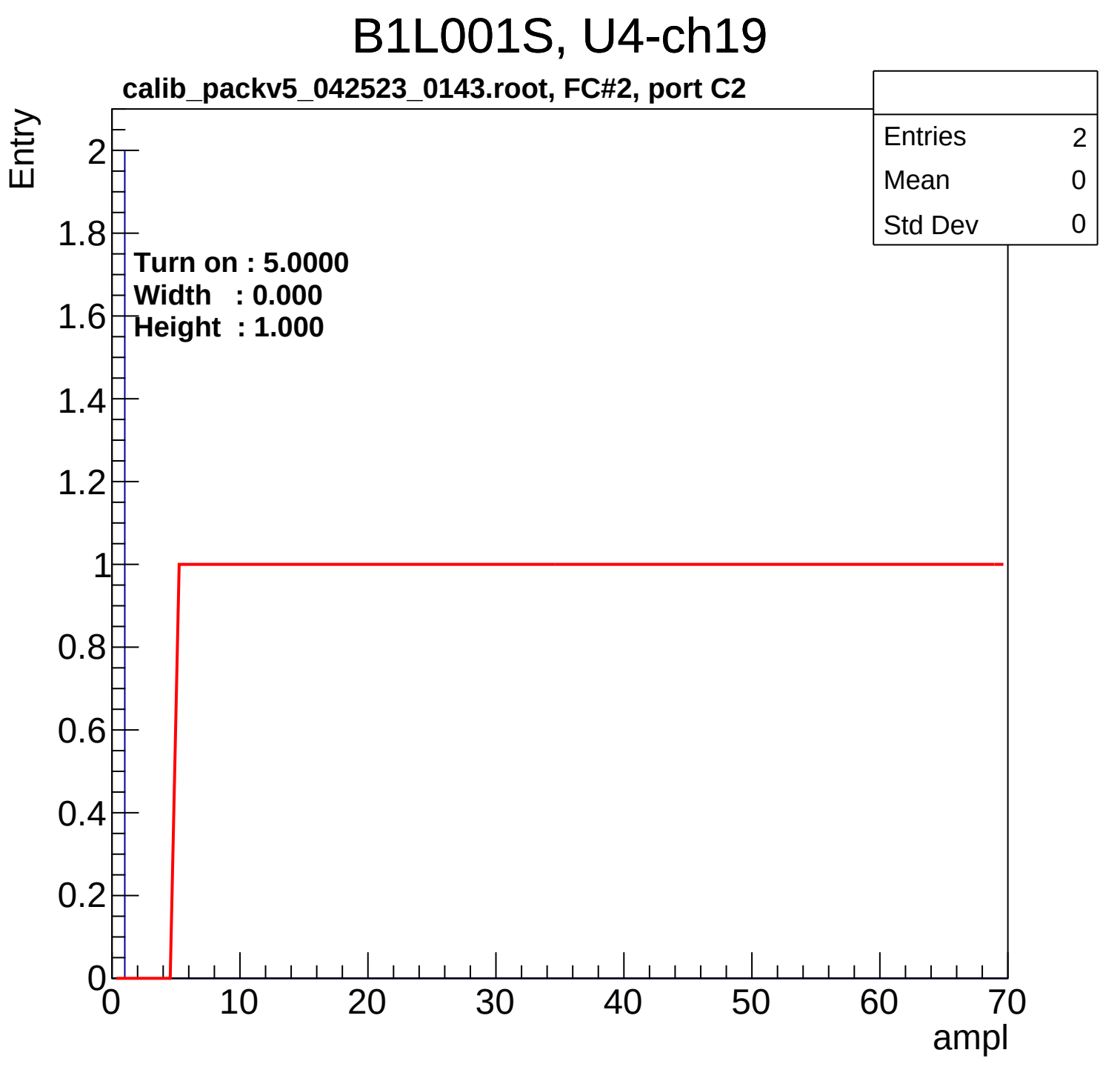
B1L001S, U4-ch19
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
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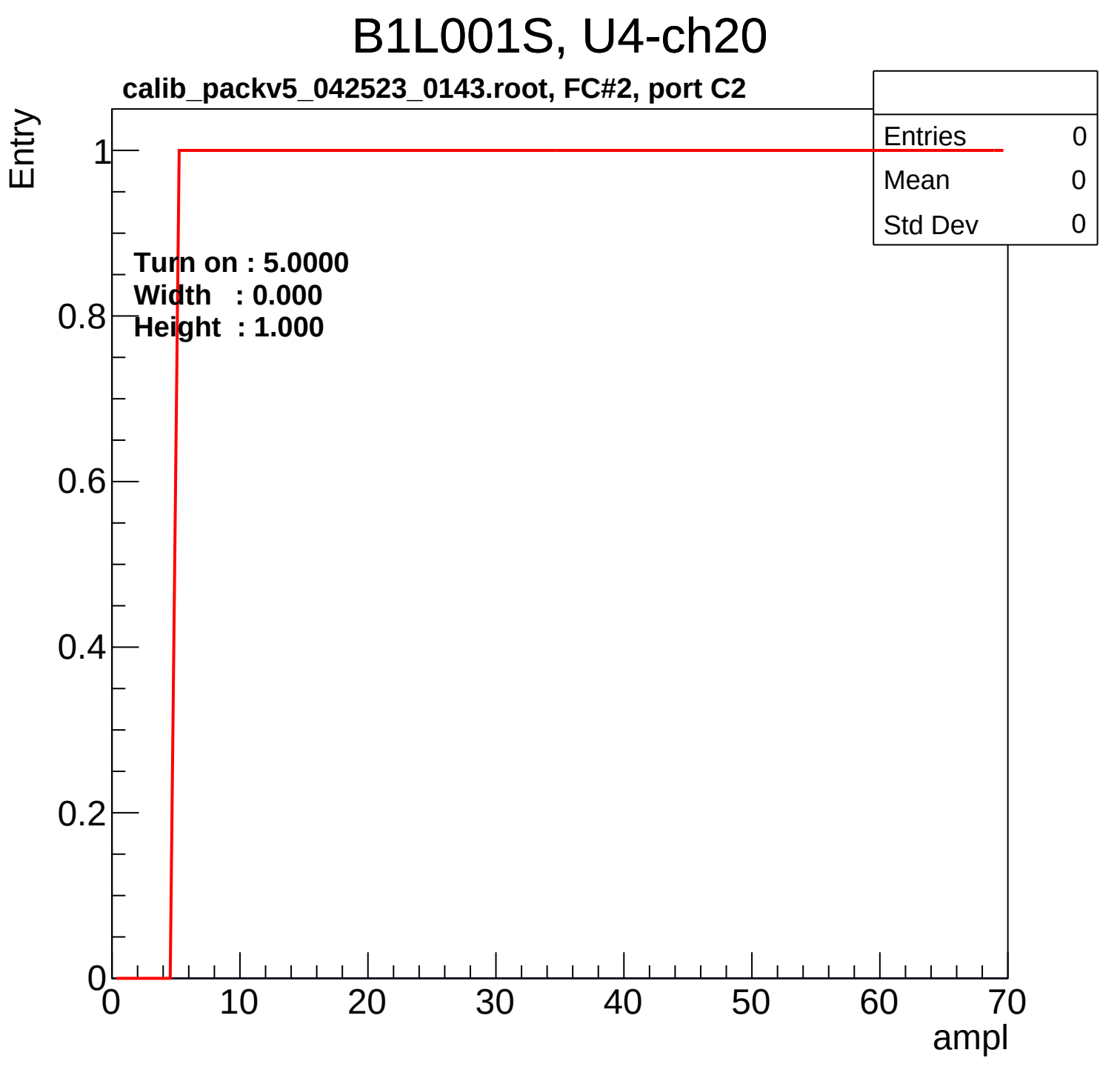
B1L001S, U4-ch20
calib_packv5_042523_0143.root, FC#2, port C2
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
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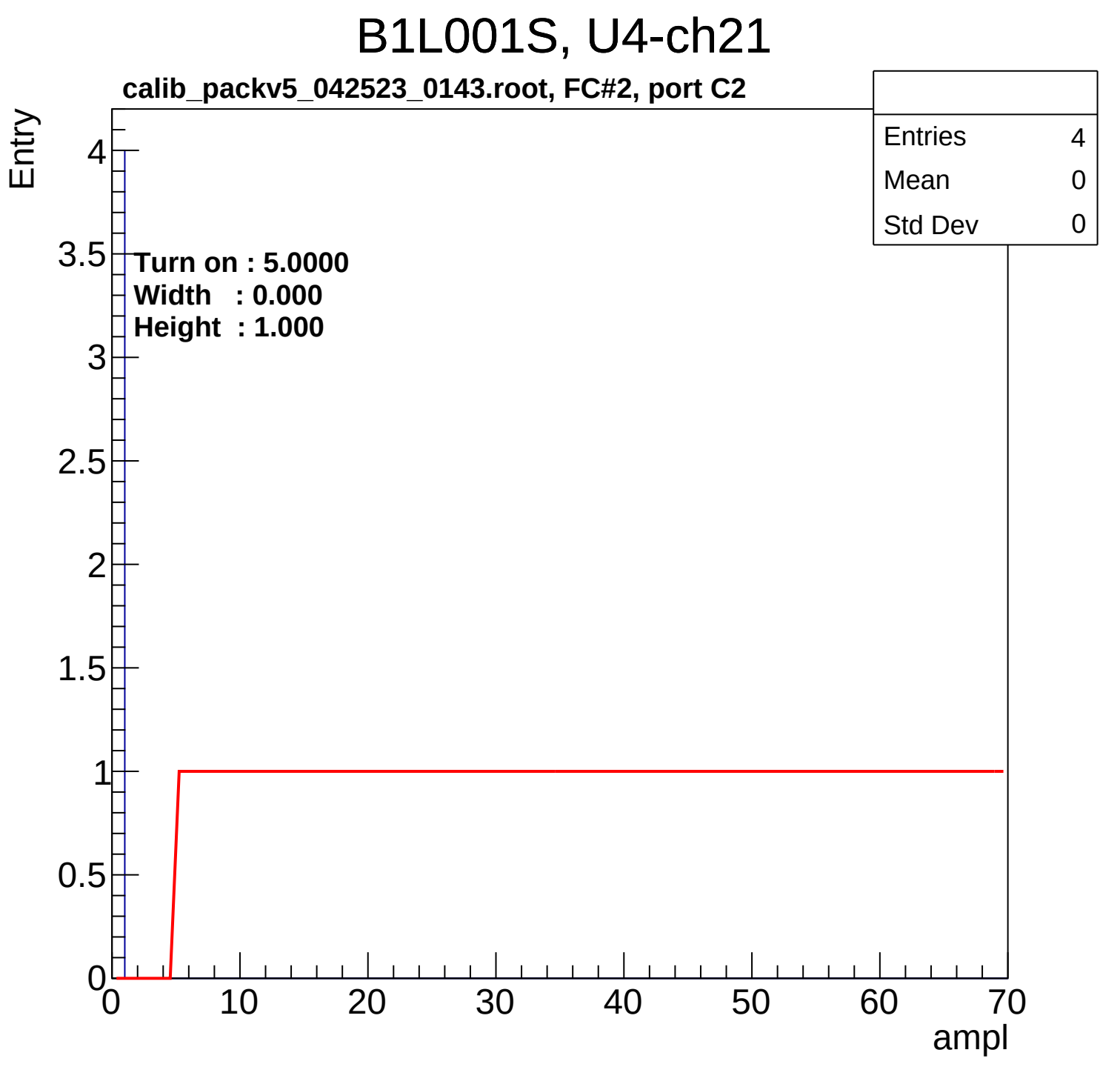
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L001S, U4-ch21
calib_packv5_042523_0143.root, FC#2, port C2
Entries 4
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
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1
1.5
2
2.5
3
3.5
4
0
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20
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40
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60
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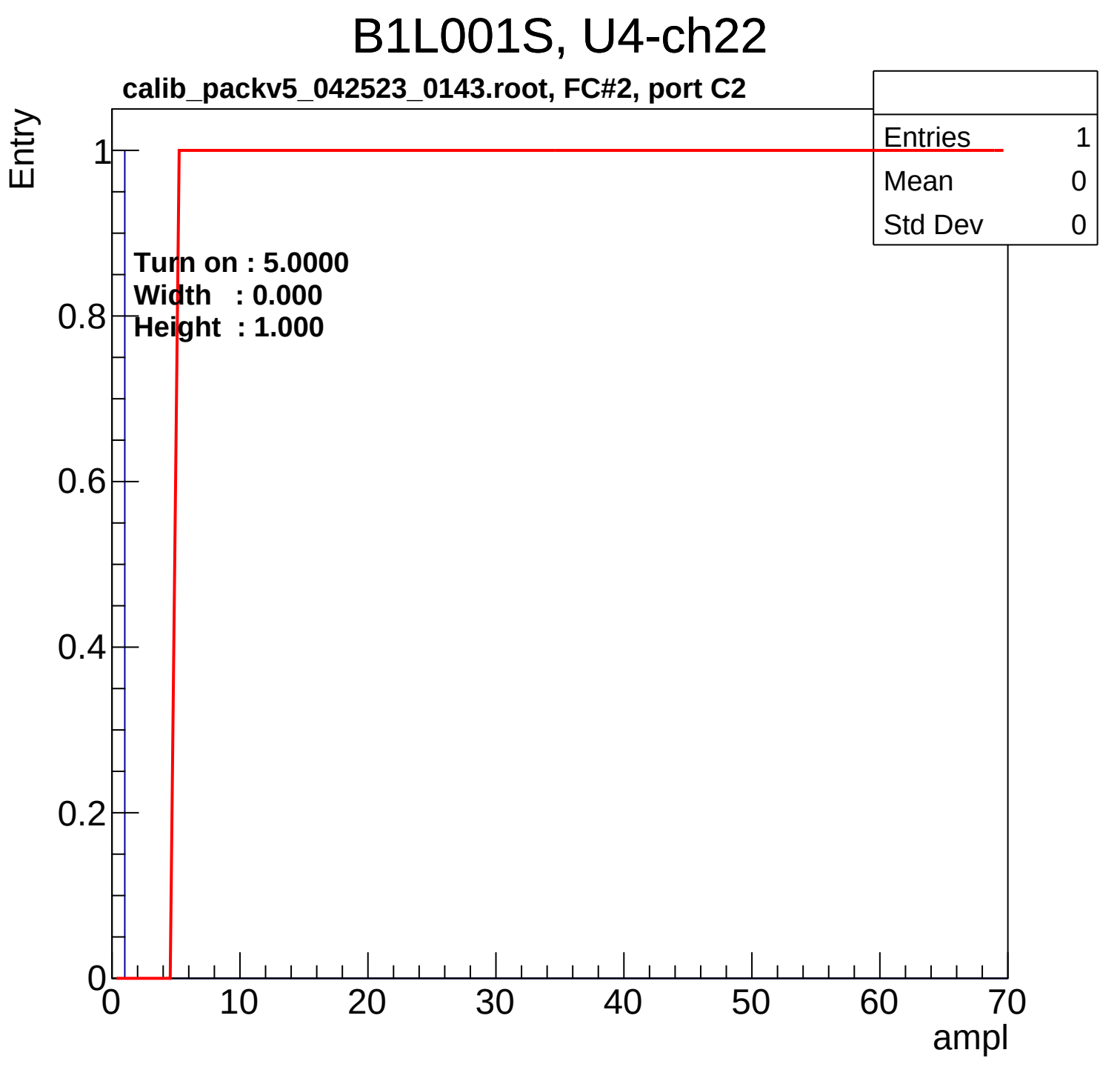
B1L001S, U4-ch22
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
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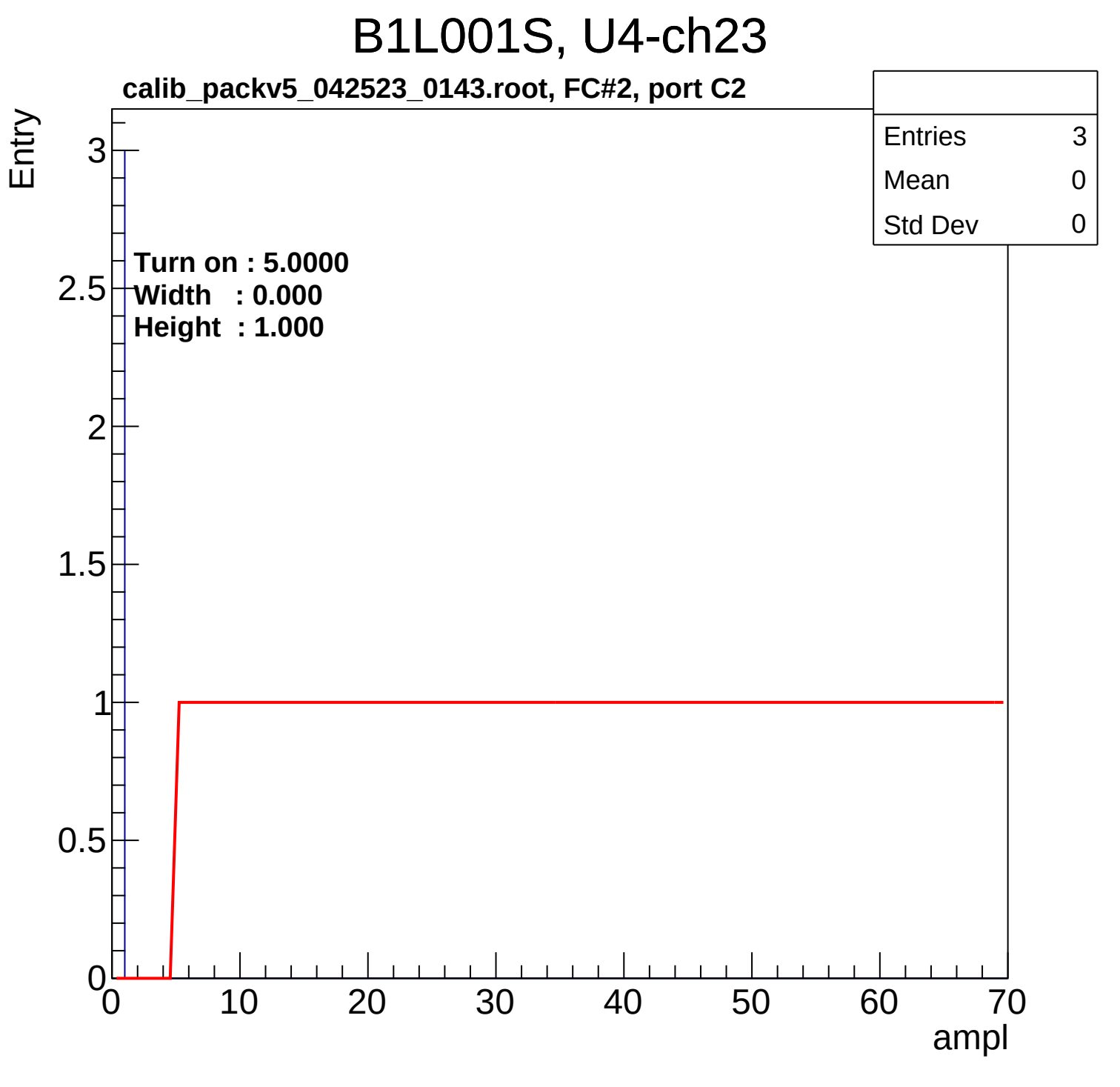
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L001S, U4-ch23
calib_packv5_042523_0143.root, FC#2, port C2
Entries 3
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
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20
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40
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60
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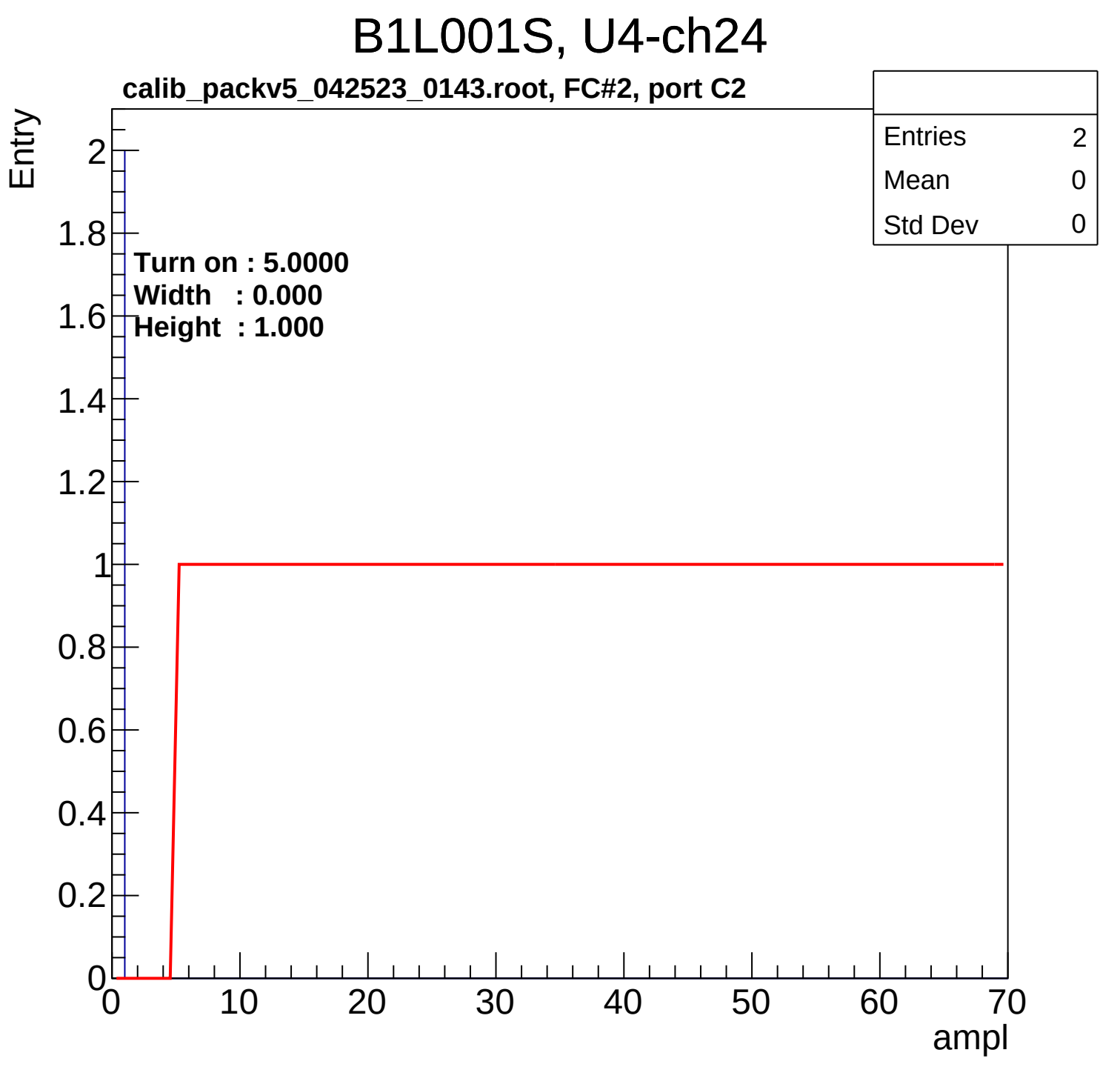
B1L001S, U4-ch24
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
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40
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60
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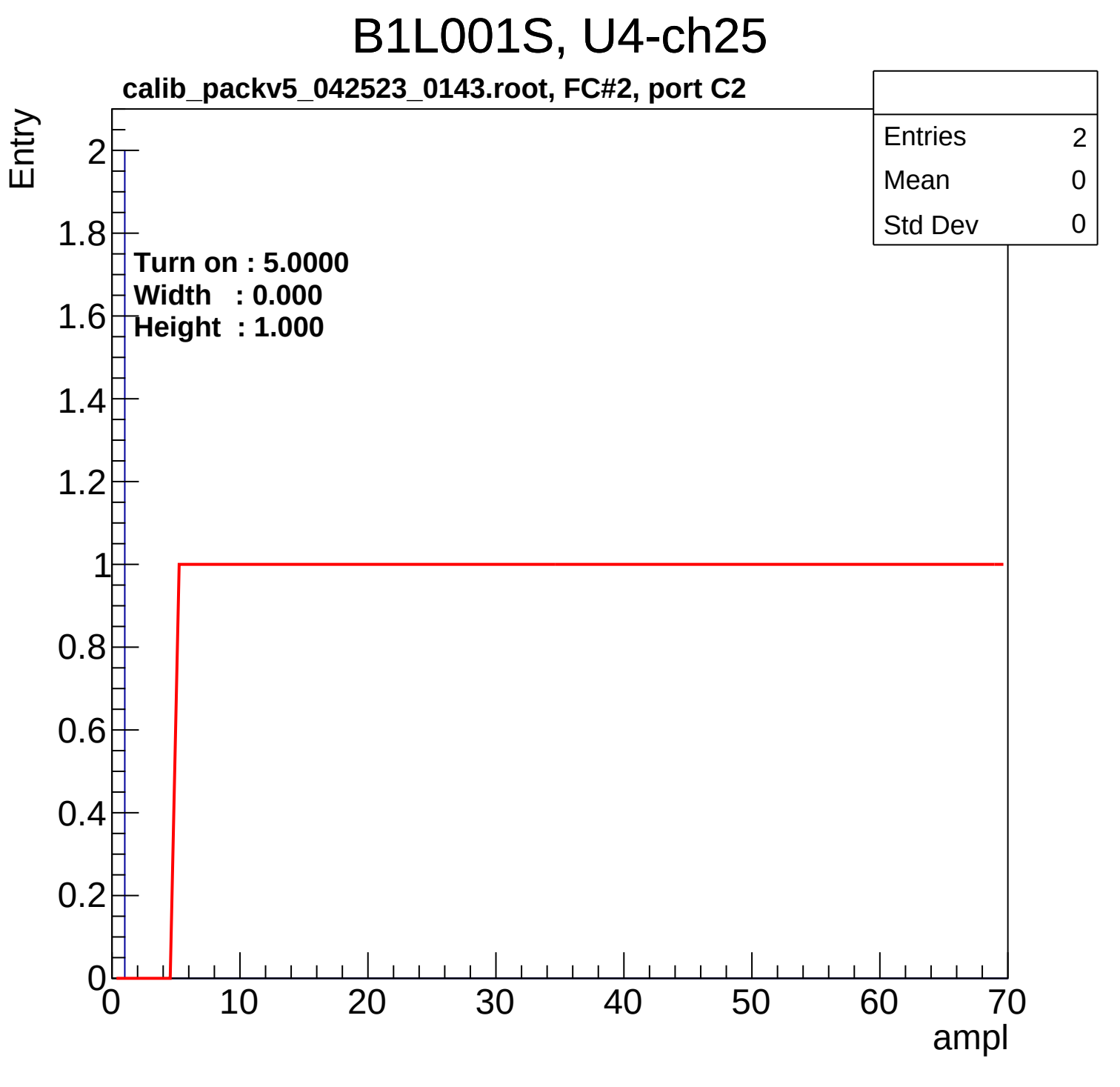
B1L001S, U4-ch25
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
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60
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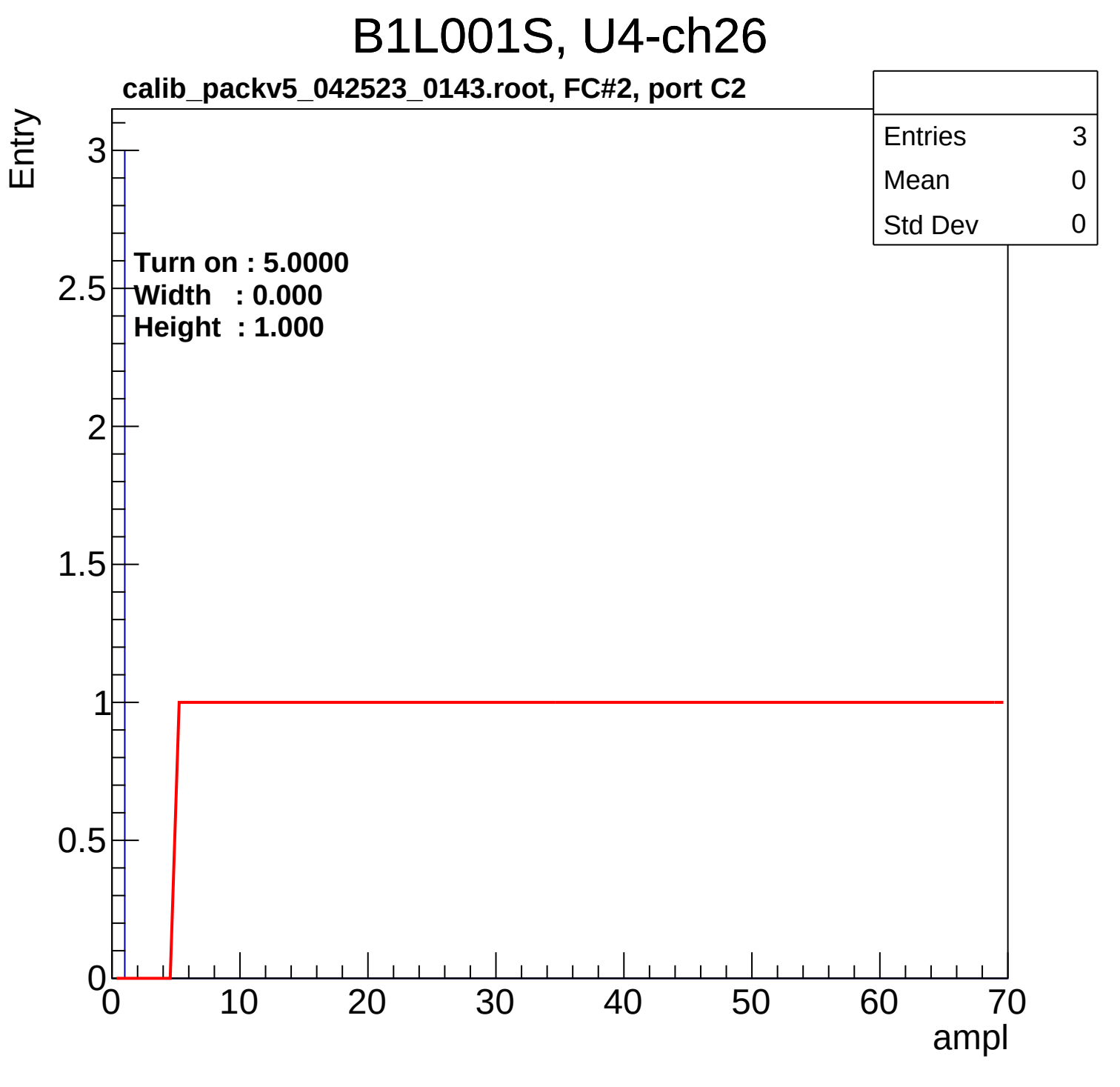
B1L001S, U4-ch26
calib_packv5_042523_0143.root, FC#2, port C2
Entries 3
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
10
20
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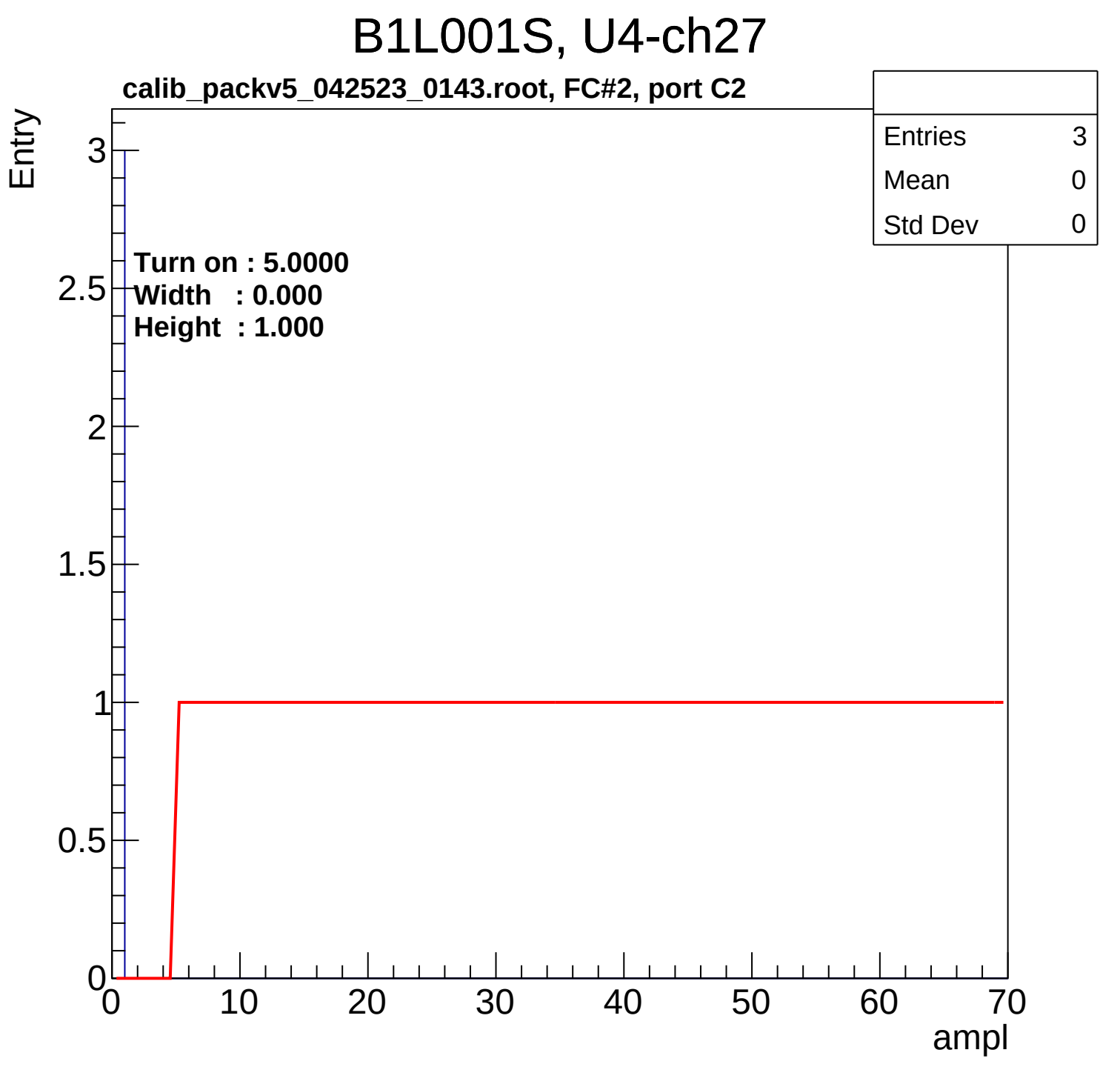
40
50
60
70


B1L001S, U4-ch27
calib_packv5_042523_0143.root, FC#2, port C2
Entries 3
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
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20
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60
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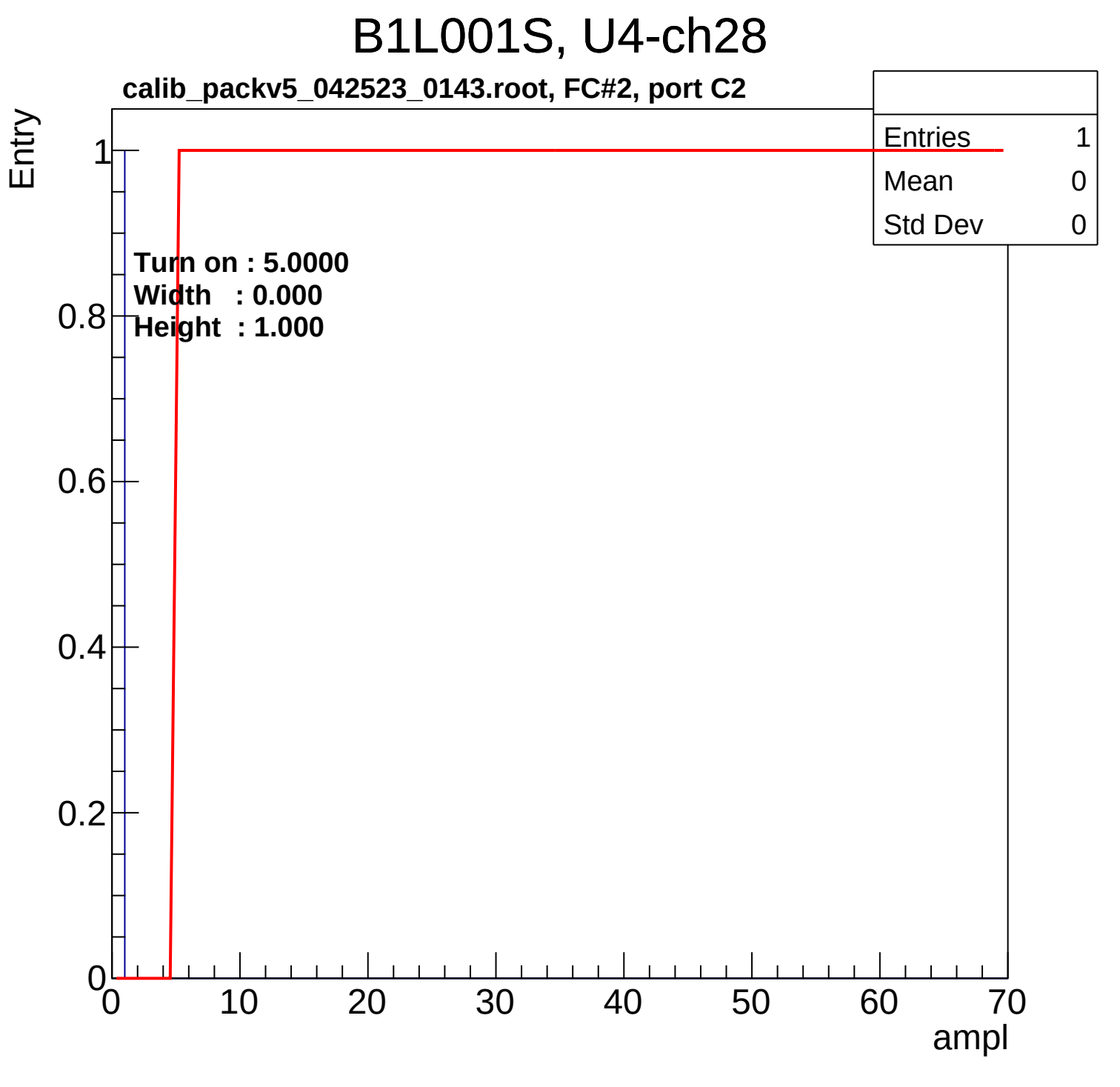
B1L001S, U4-ch28
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
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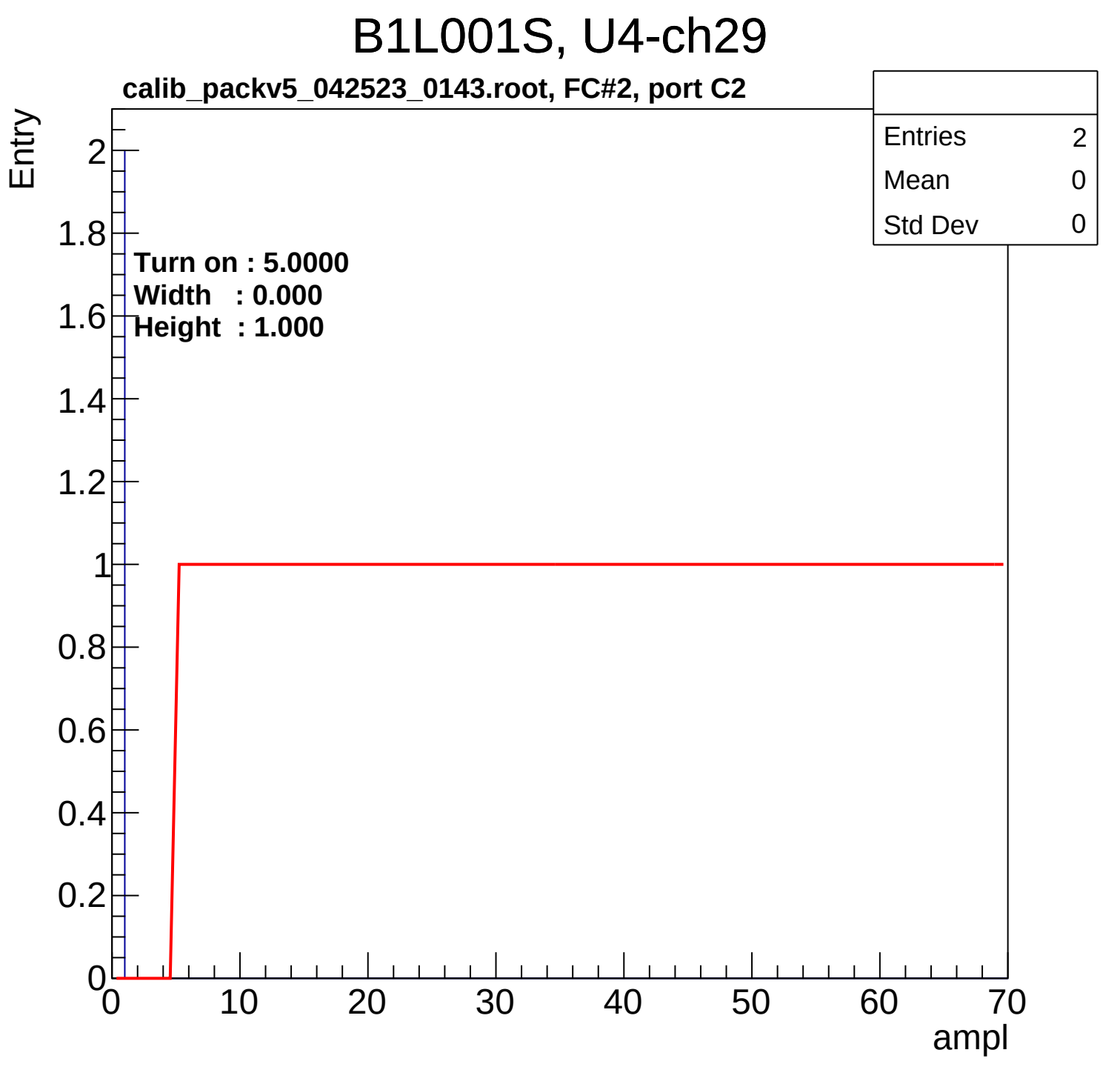
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L001S, U4-ch29
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
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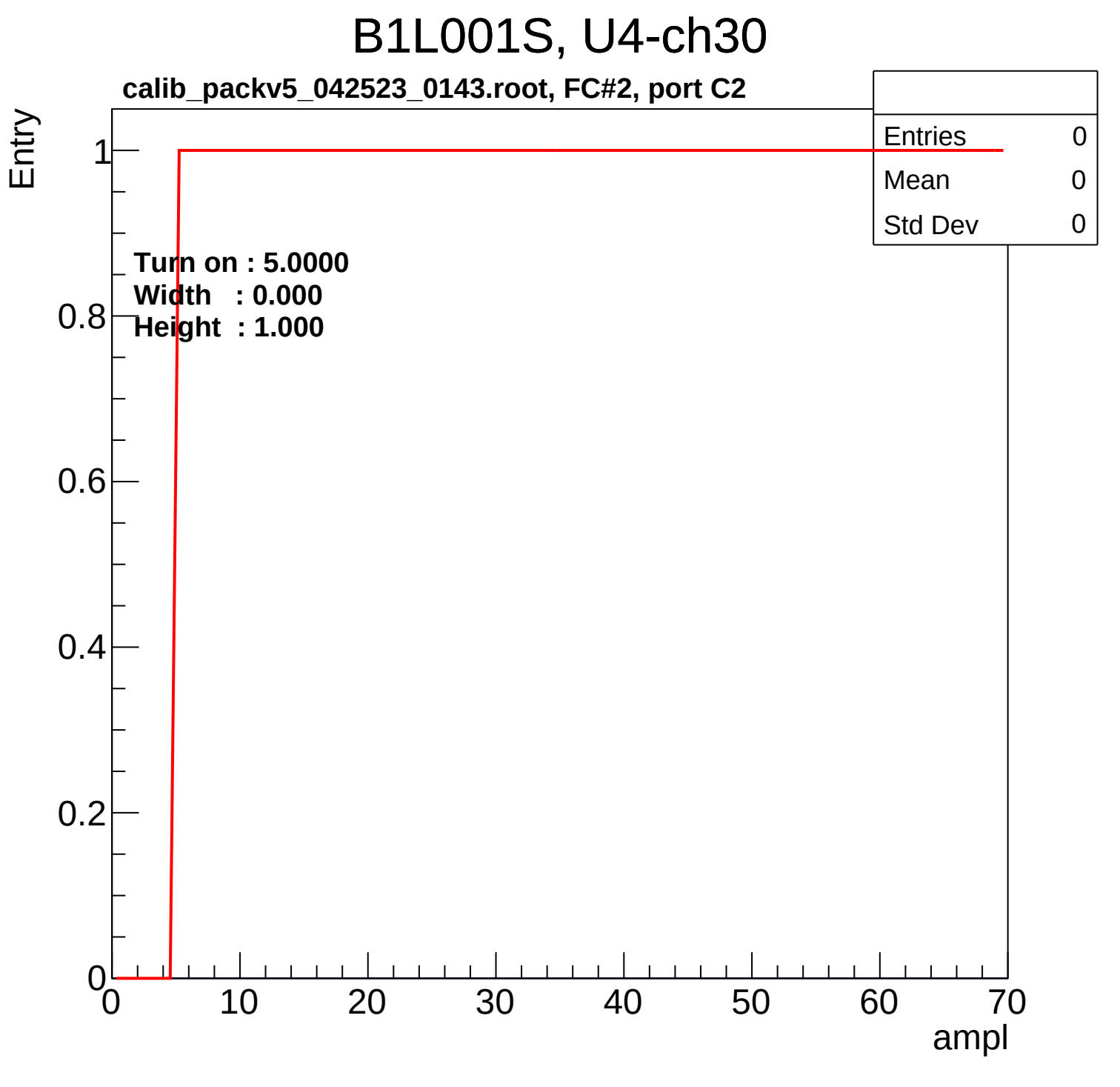
B1L001S, U4-ch30
calib_packv5_042523_0143.root, FC#2, port C2
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
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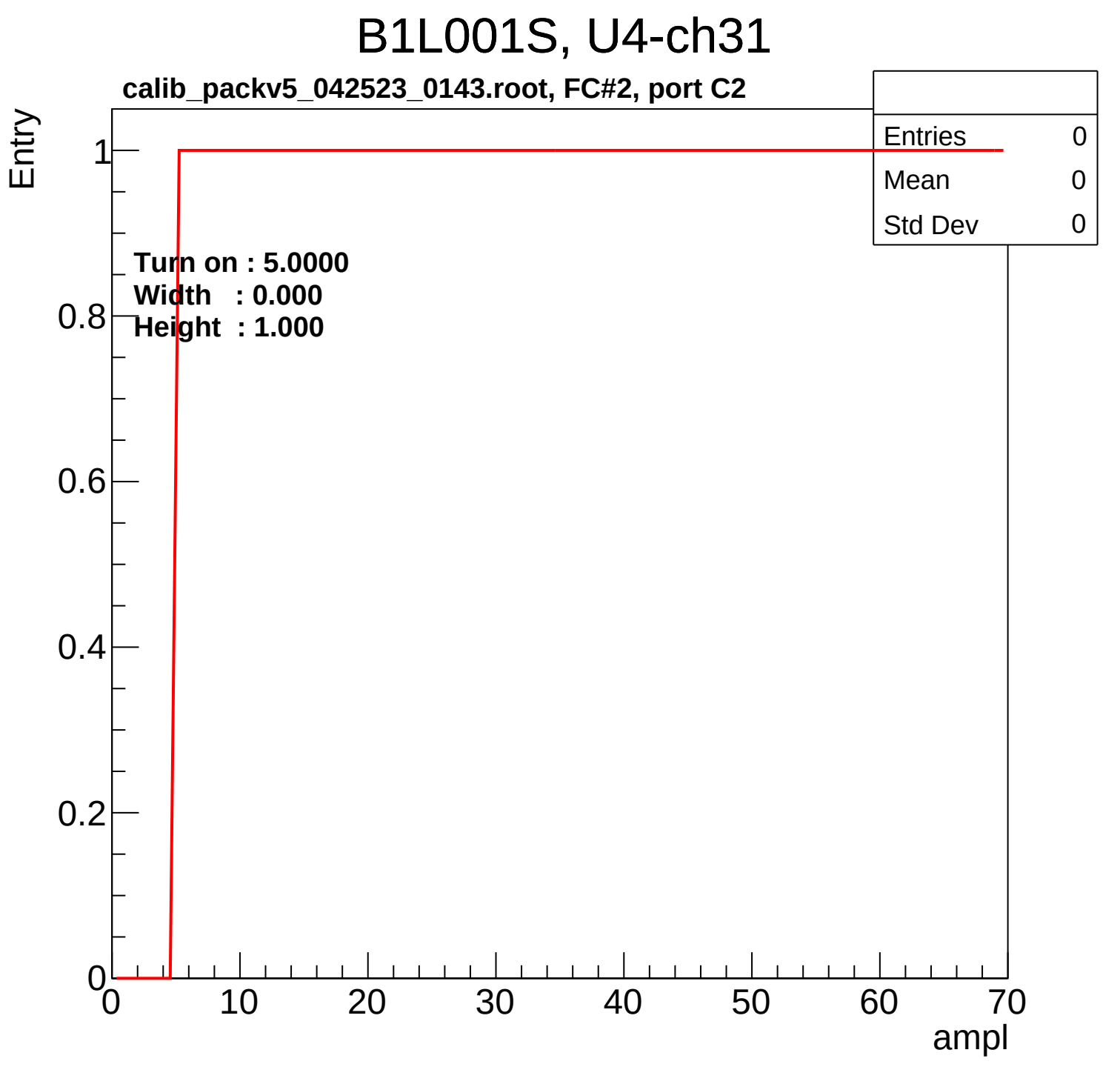
70
ampl


B1L001S, U4-ch31
calib_packv5_042523_0143.root, FC#2, port C2
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
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0.8
0.6
0.4
0.2
0
0
10
20
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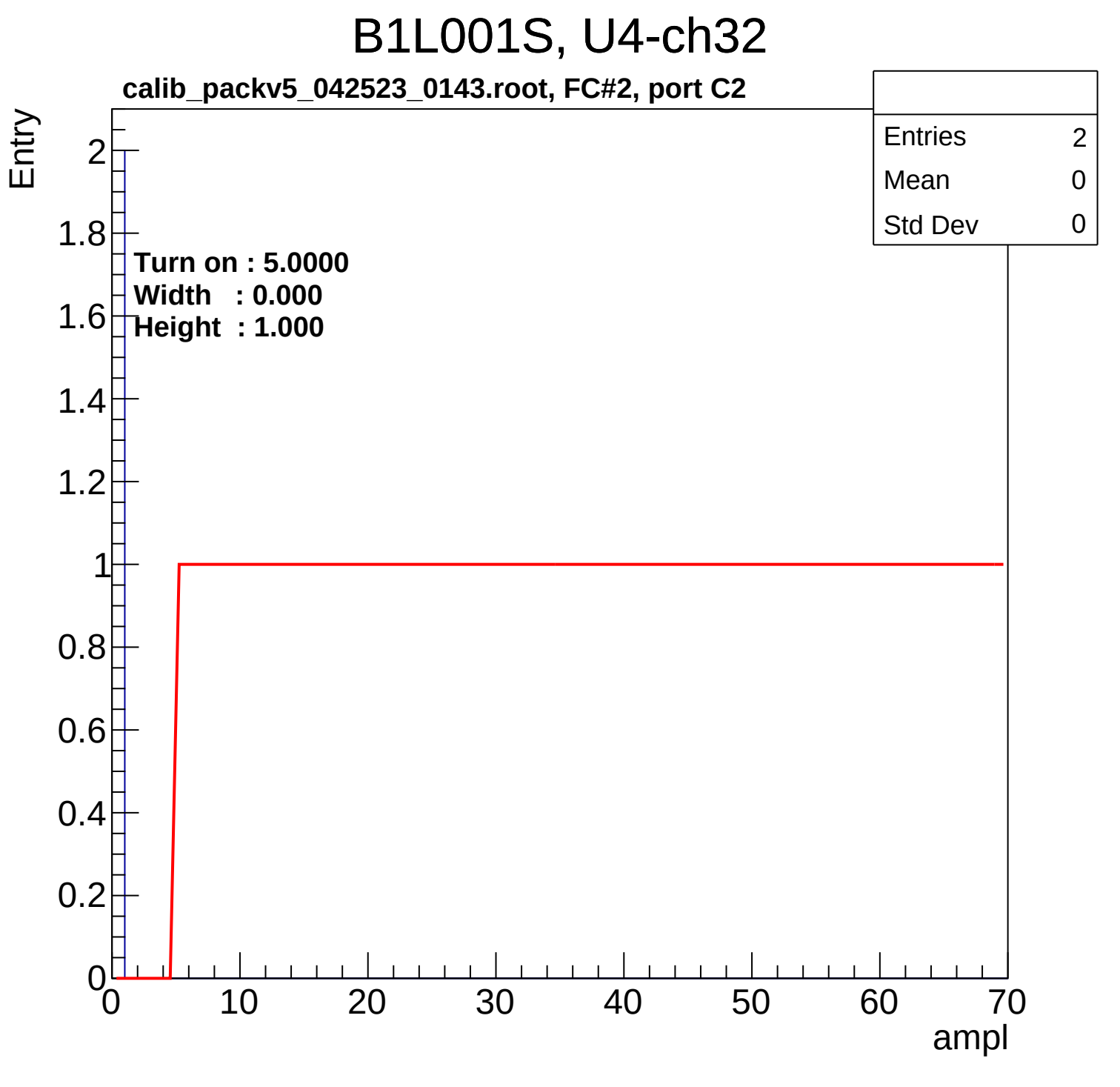
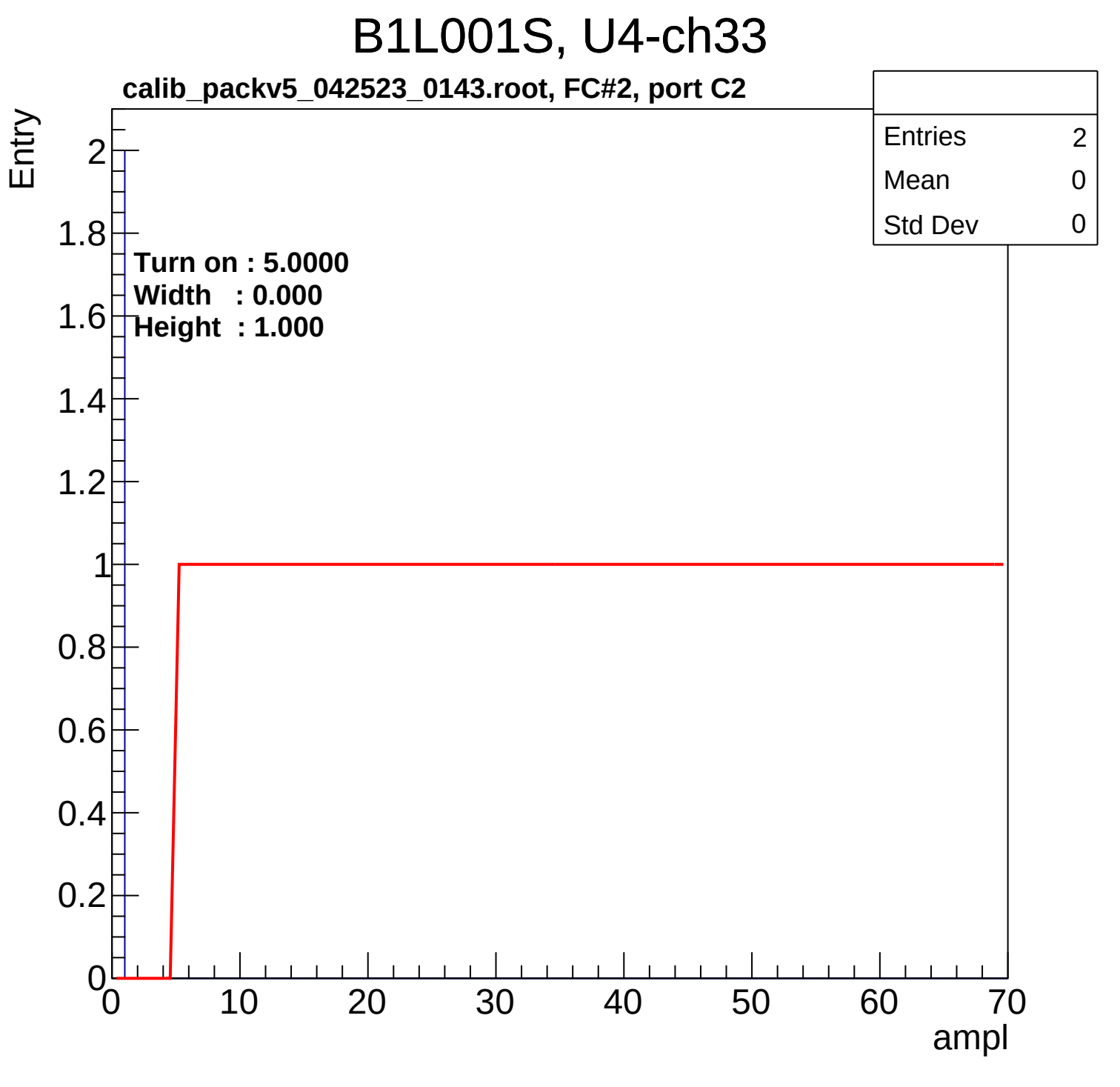
50
60
70
ampl


B1L001S, U4-ch32
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L001S, U4-ch33
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
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60
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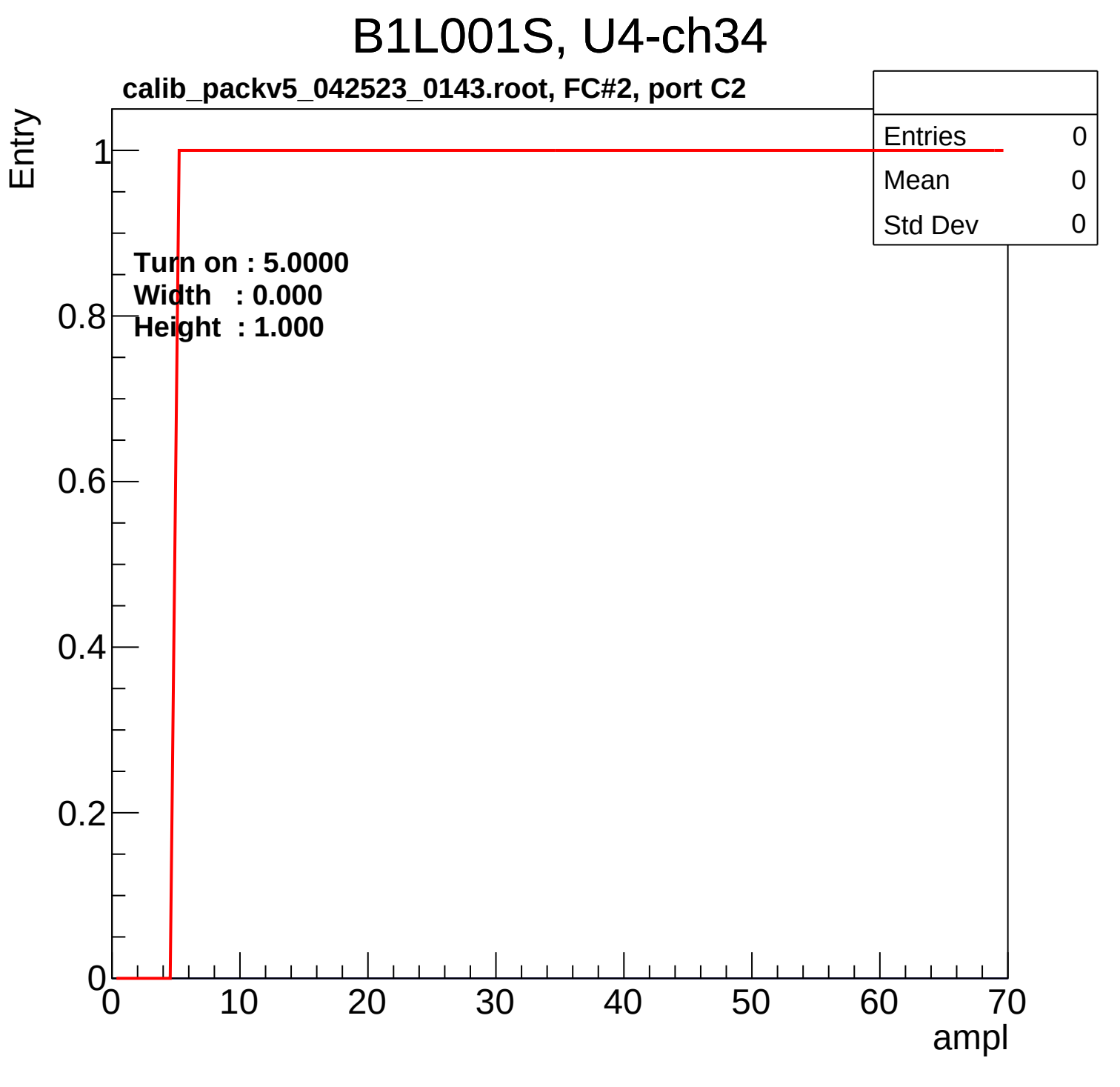
B1L001S, U4-ch34
calib_packv5_042523_0143.root, FC#2, port C2
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
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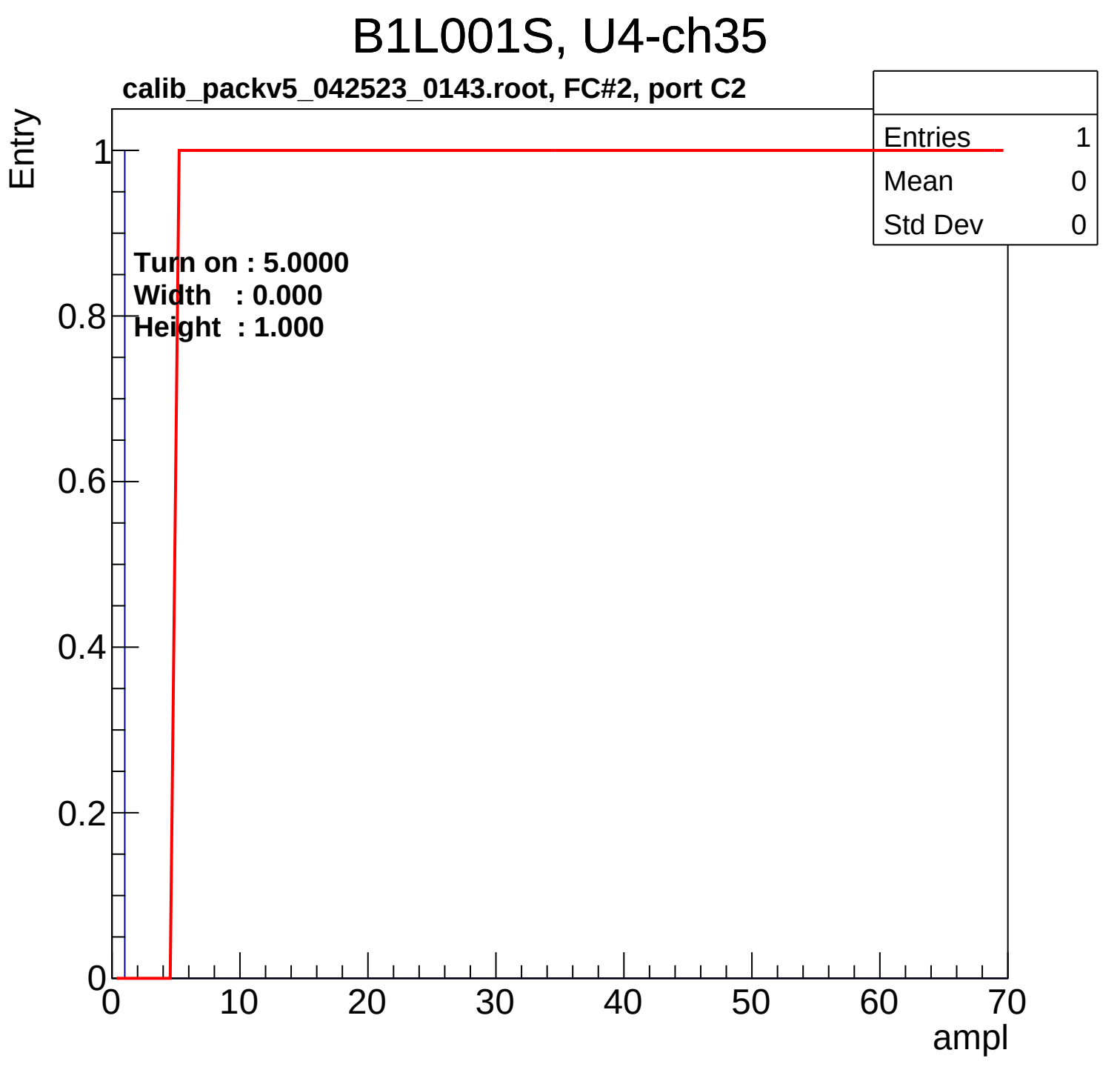
50
60
70
ampl


B1L001S, U4-ch35
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
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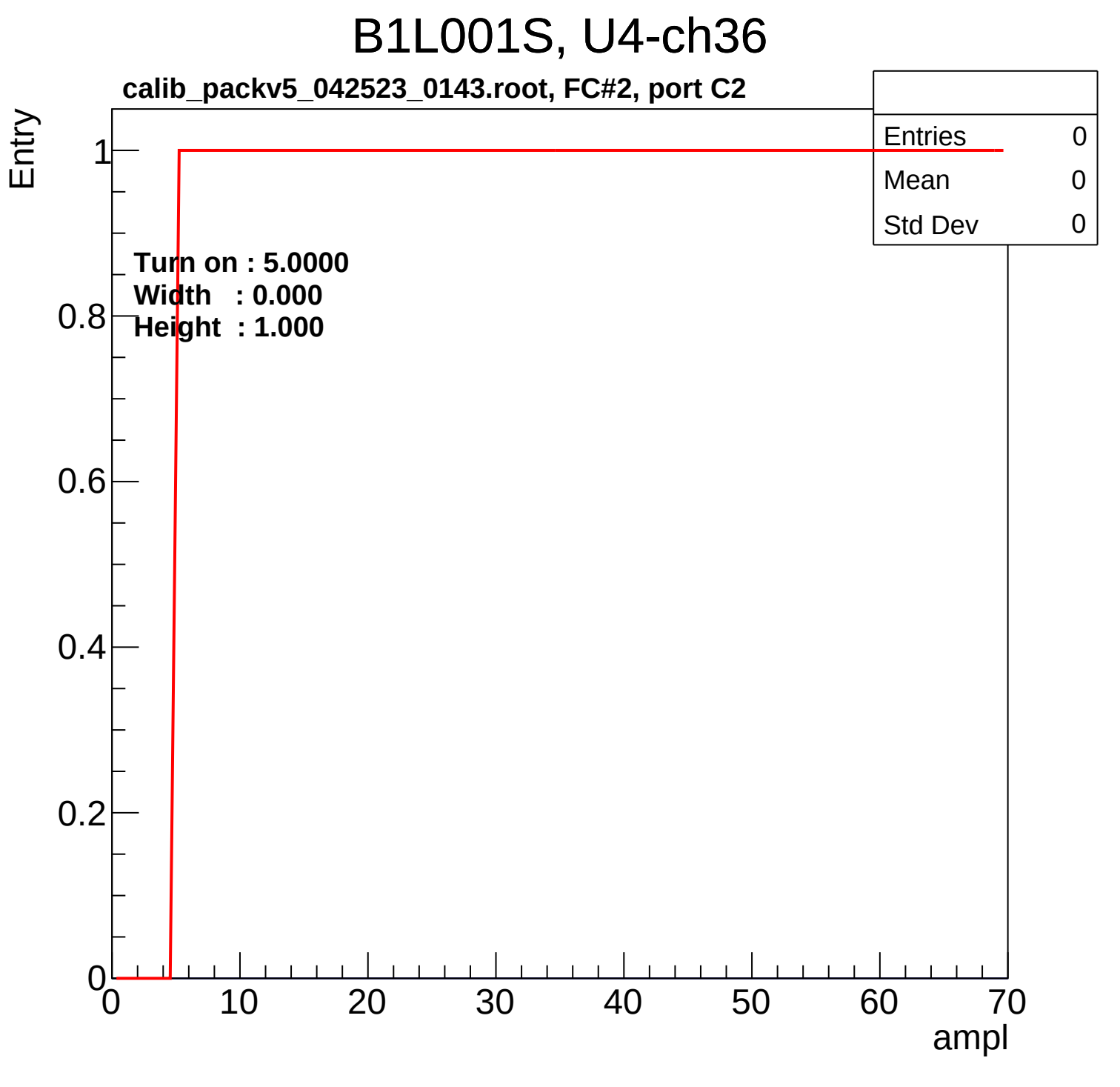
40
50
60
70
ampl


B1L001S, U4-ch36
calib_packv5_042523_0143.root, FC#2, port C2
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
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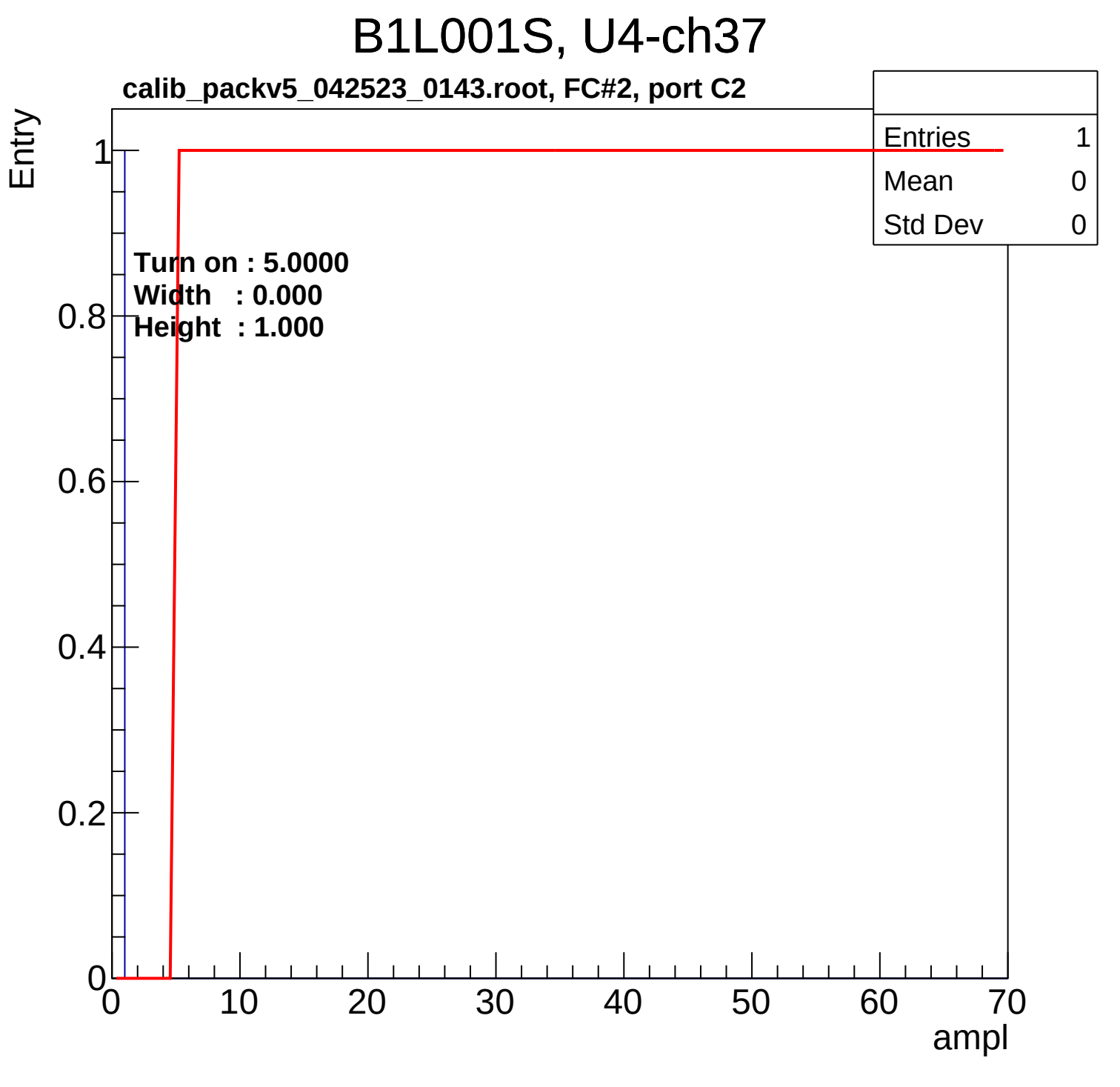
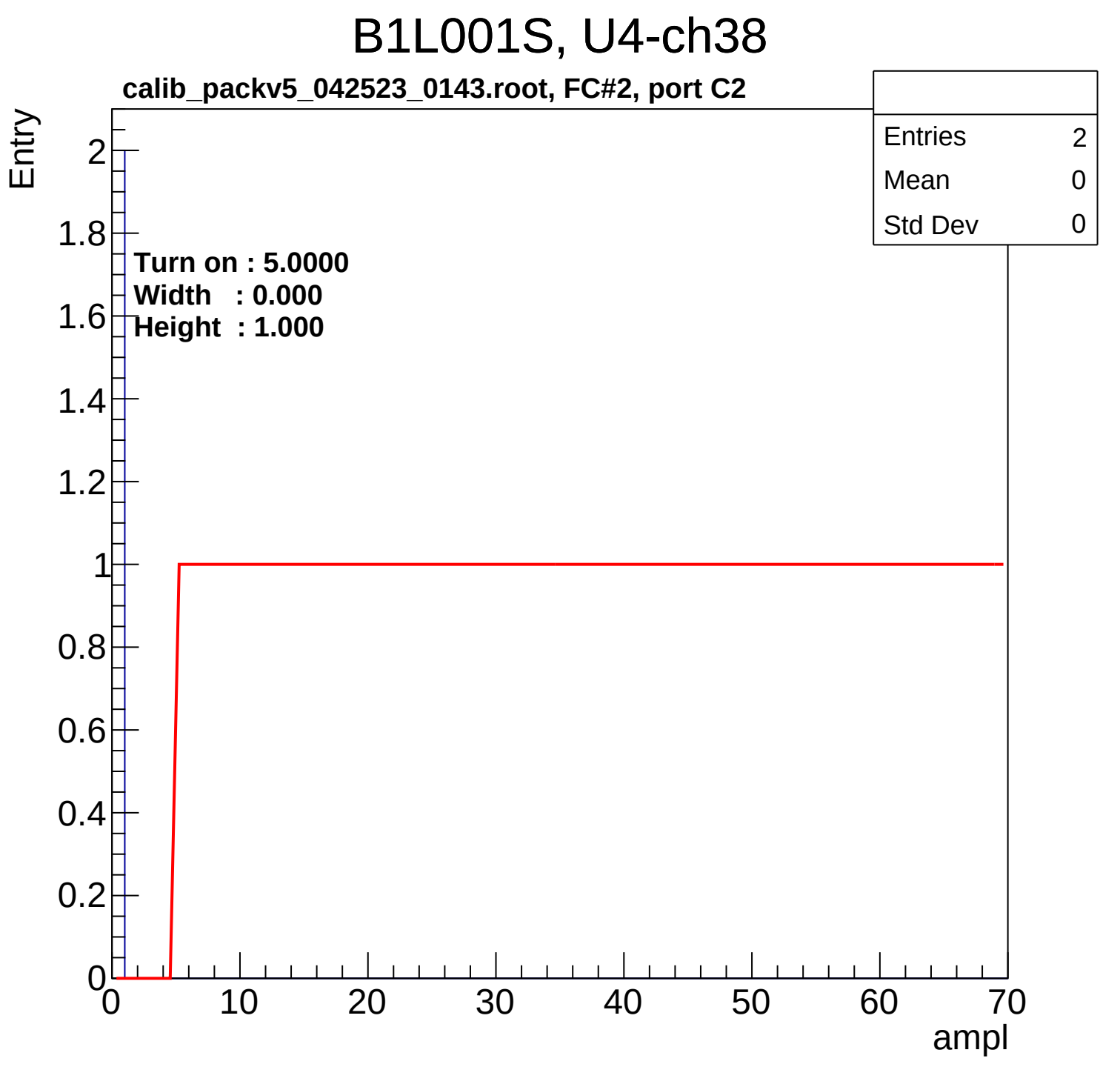
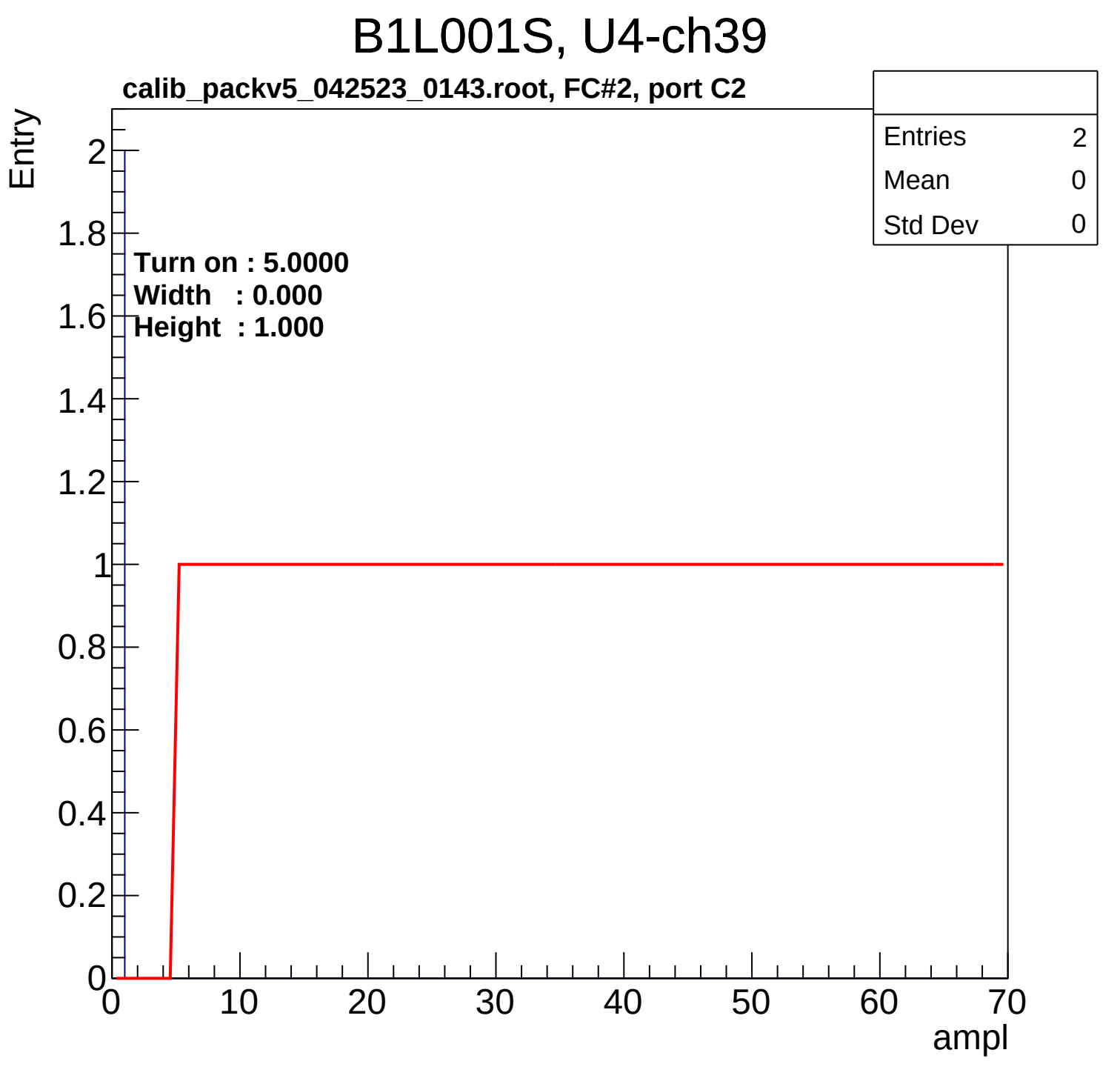
50
60
70
ampl


B1L001S, U4-ch37
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L001S, U4-ch38
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L001S, U4-ch39
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
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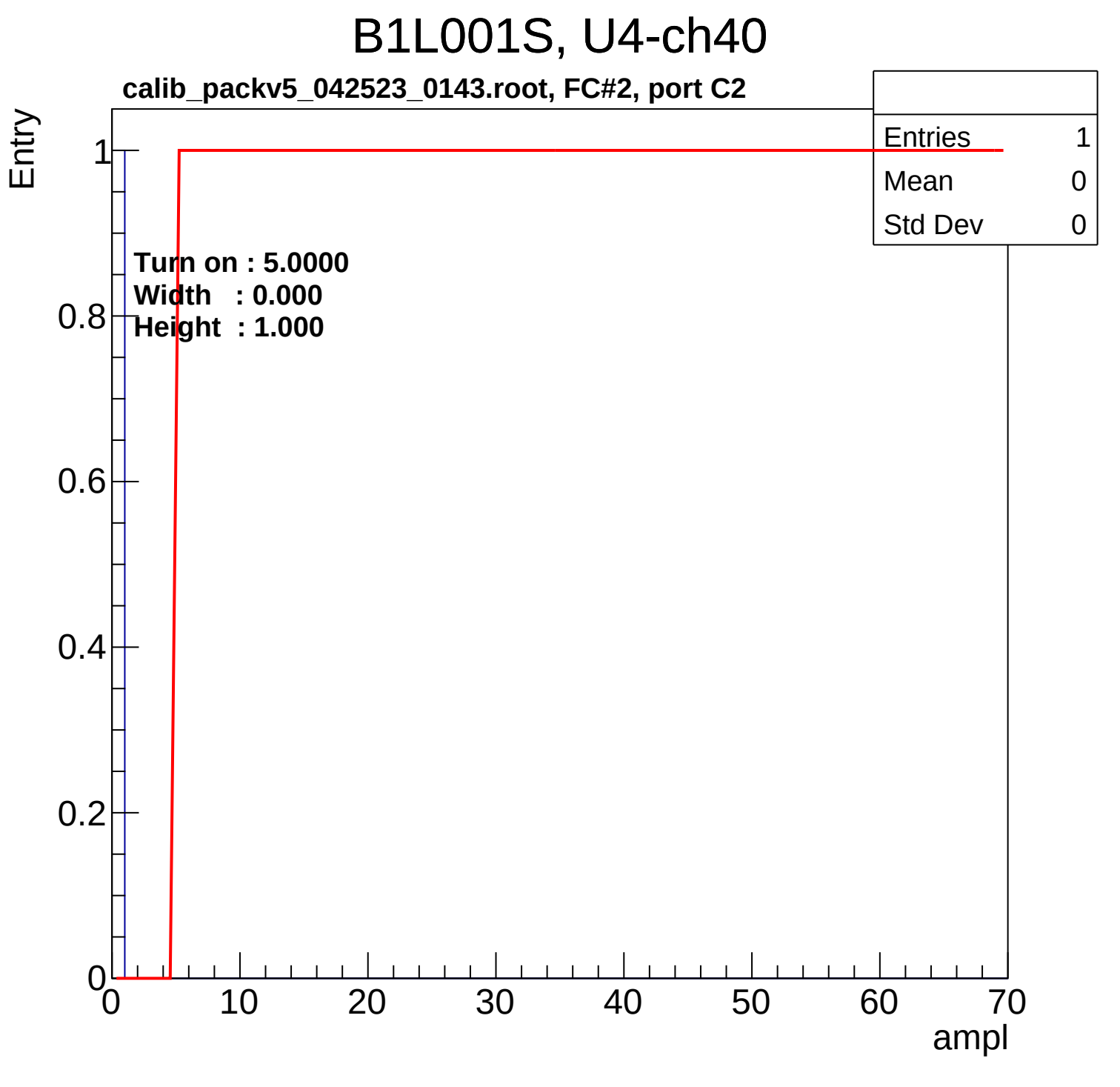
B1L001S, U4-ch40
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
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60
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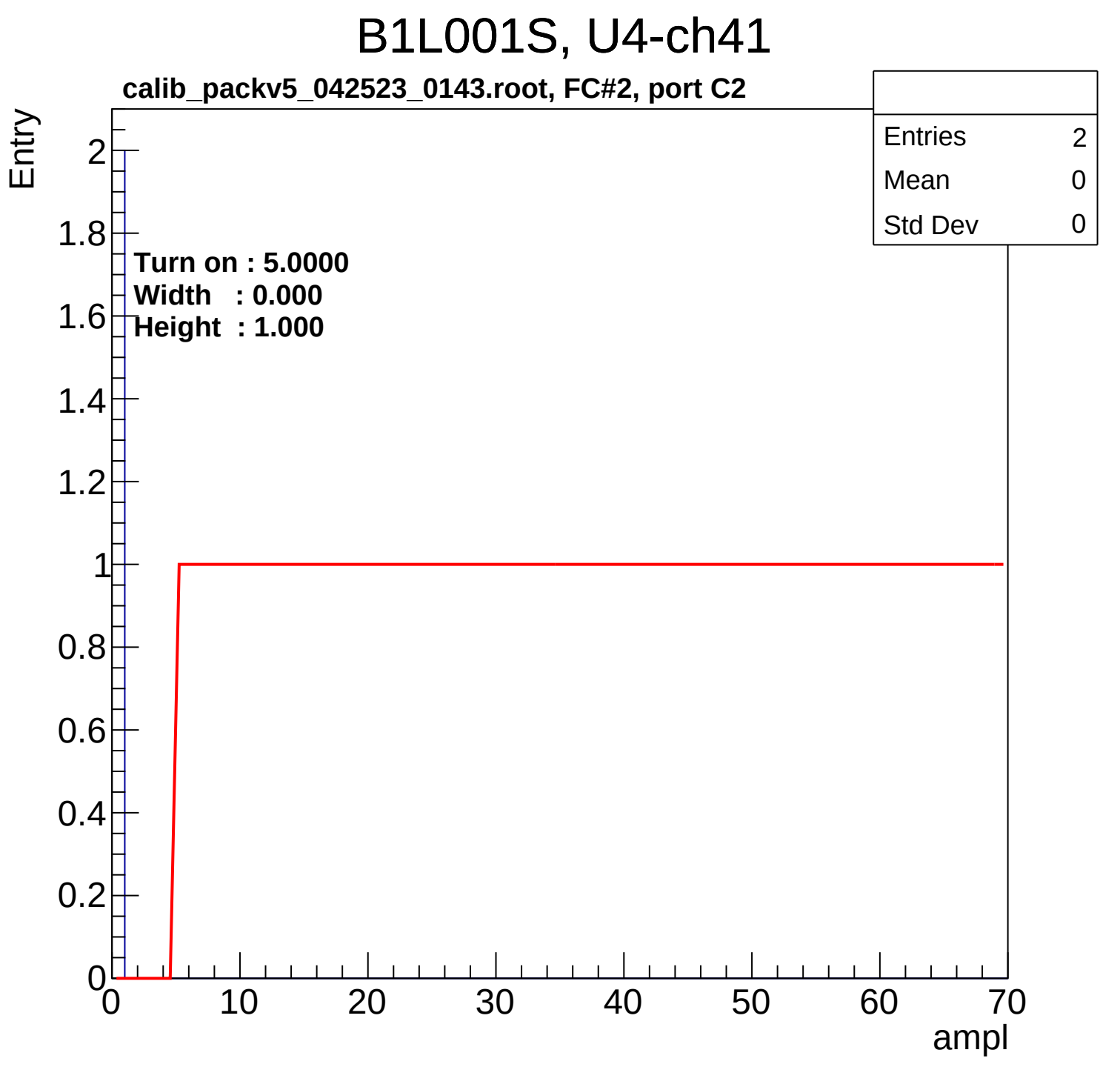
B1L001S, U4-ch41
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
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60
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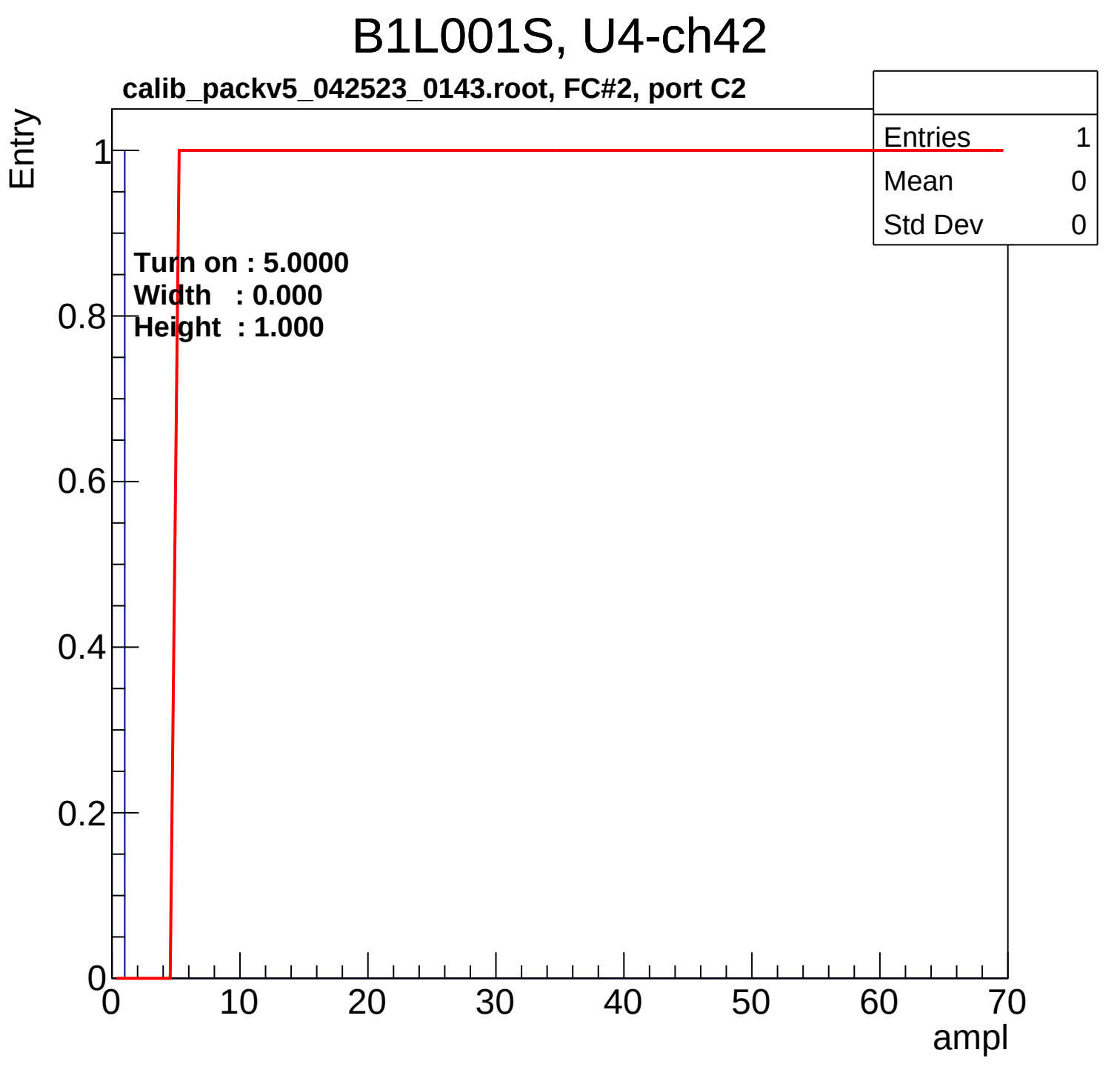
B1L001S, U4-ch42
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
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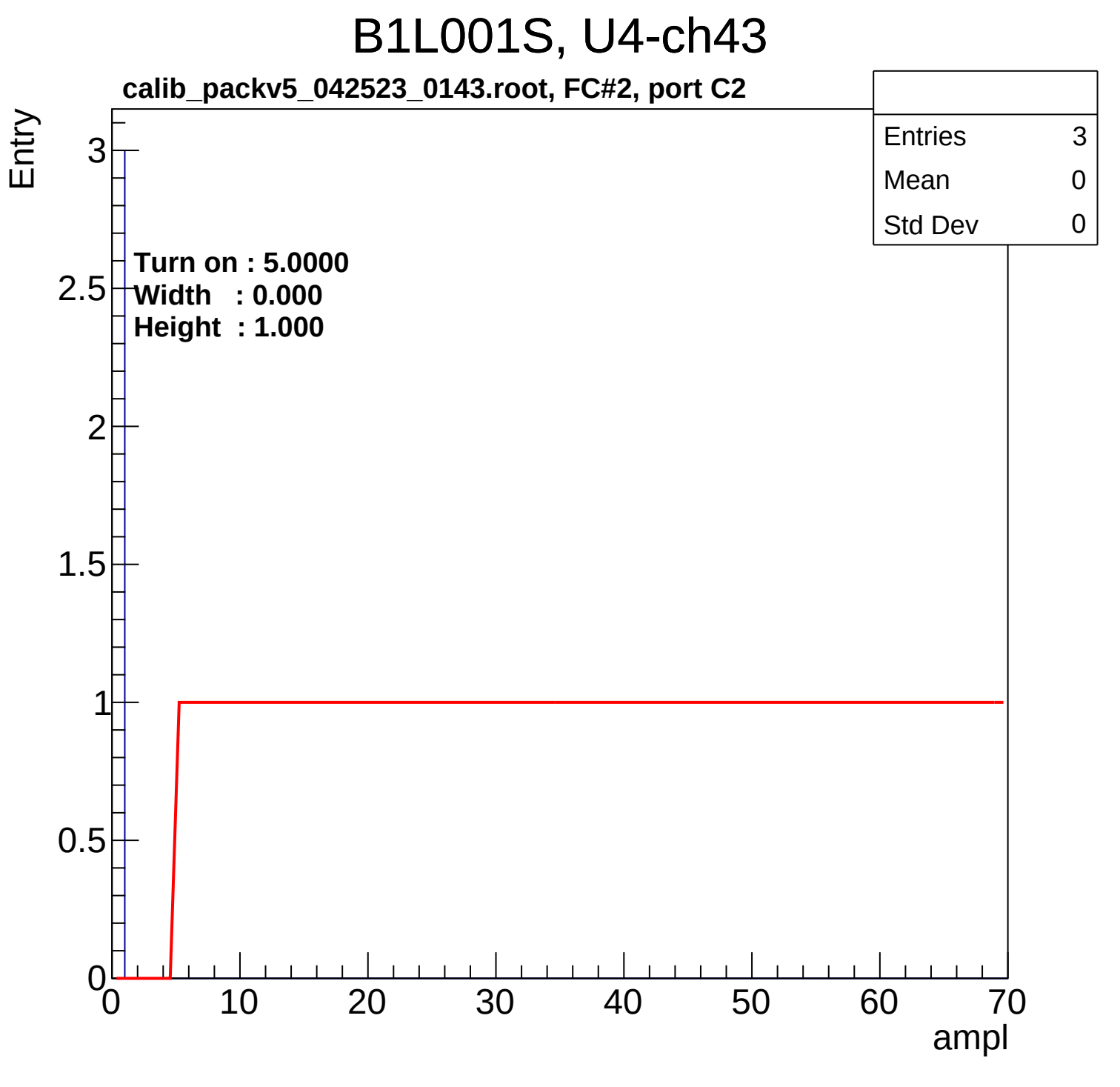
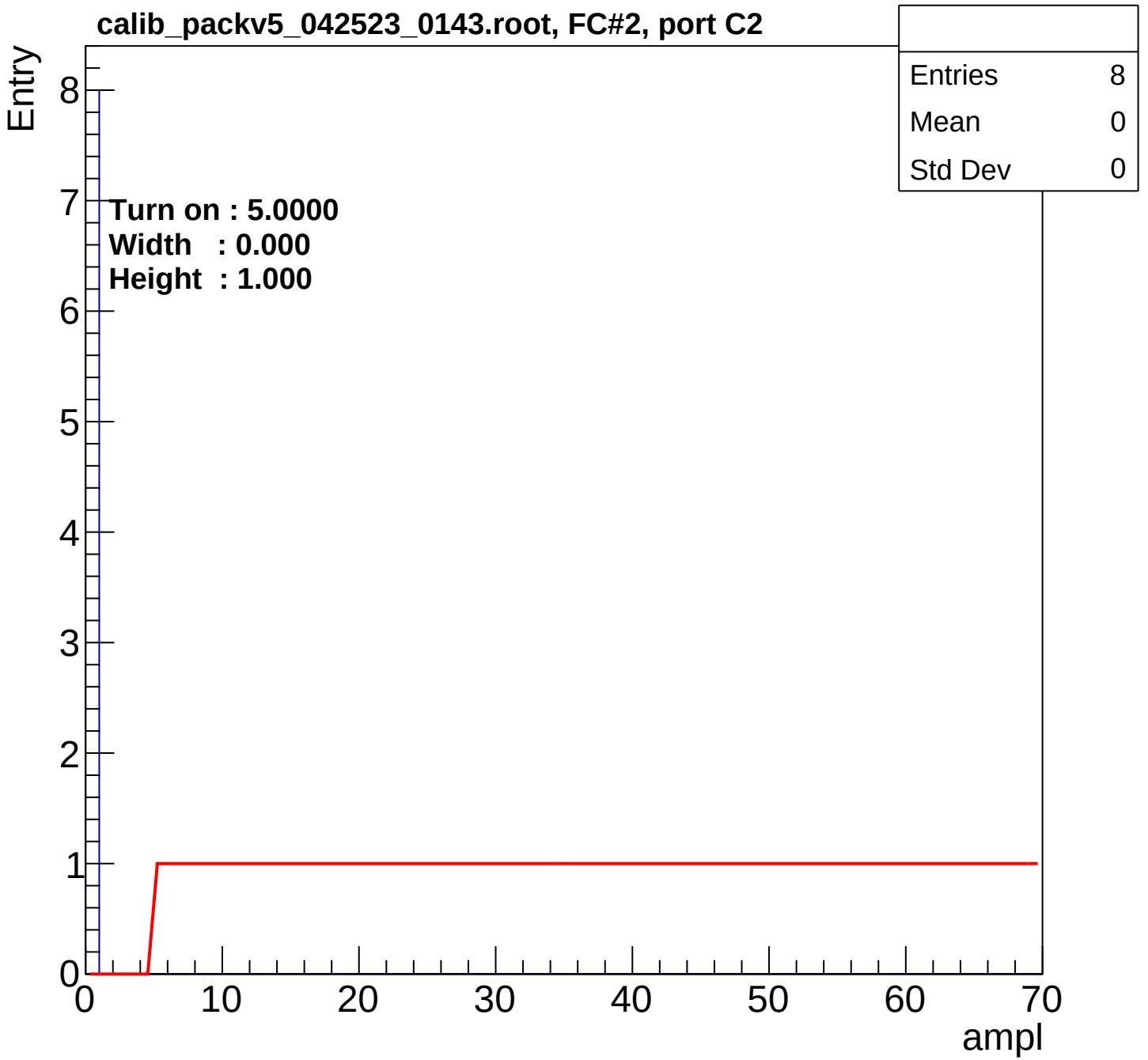
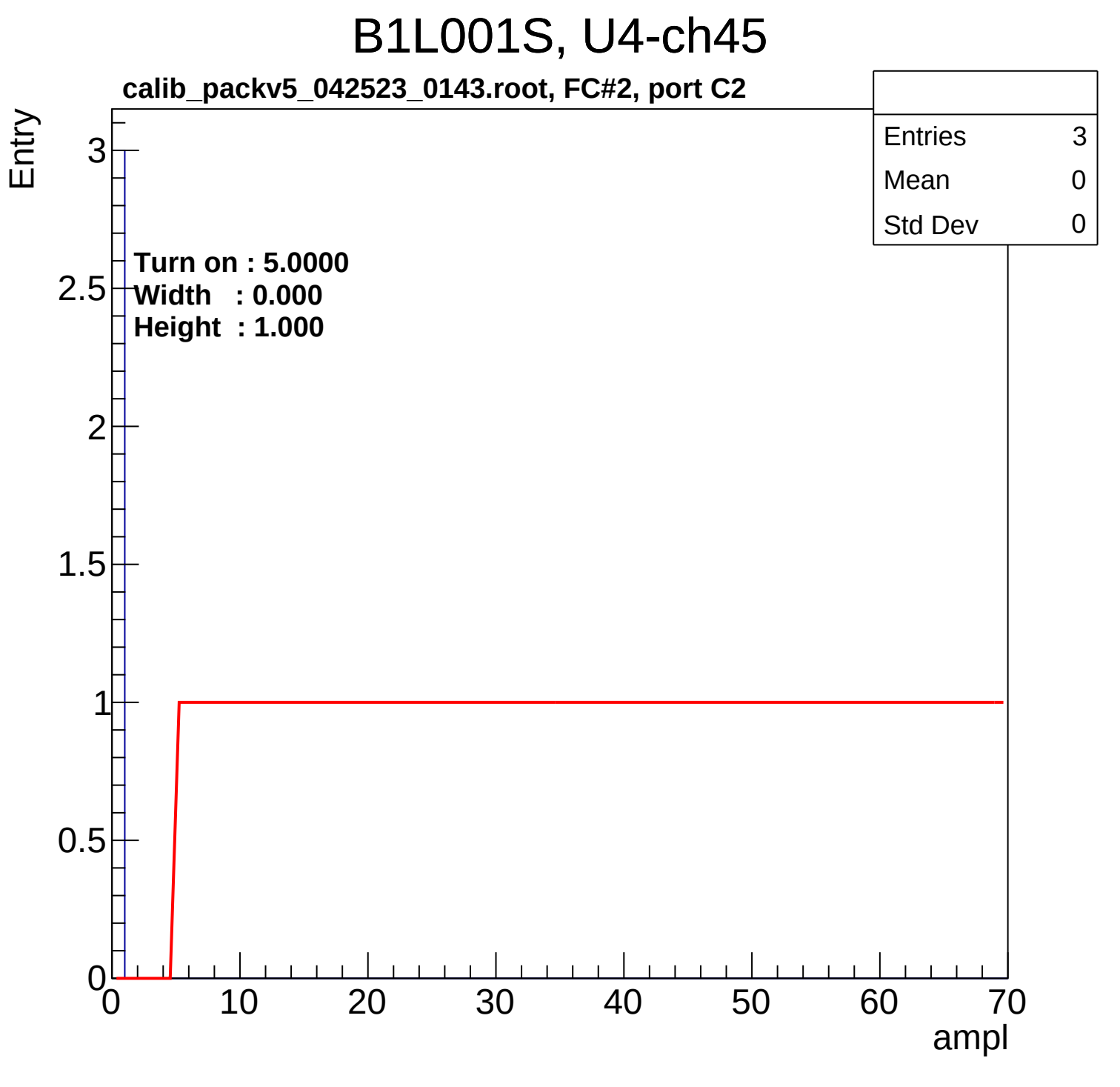
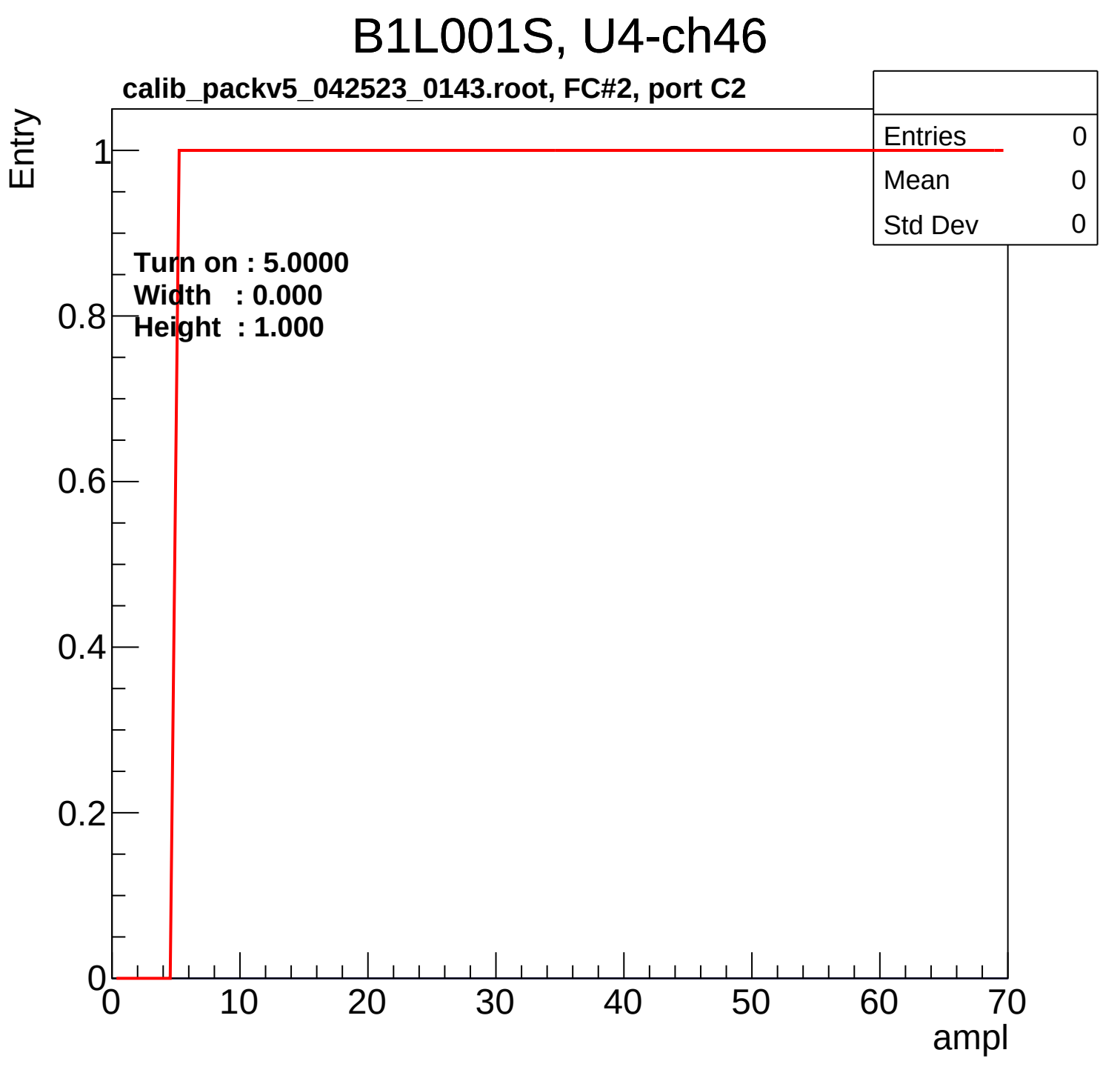
0
0
10
20
30
40
50
60
70
ampl


B1L001S, U4-ch43
calib_packv5_042523_0143.root, FC#2, port C2
Entries 3
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L001S, U4-ch44
calib_packv5_042523_0143.root, FC#2, port C2
Entries 8
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L001S, U4-ch45
calib_packv5_042523_0143.root, FC#2, port C2
Entries 3
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L001S, U4-ch46
calib_packv5_042523_0143.root, FC#2, port C2
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
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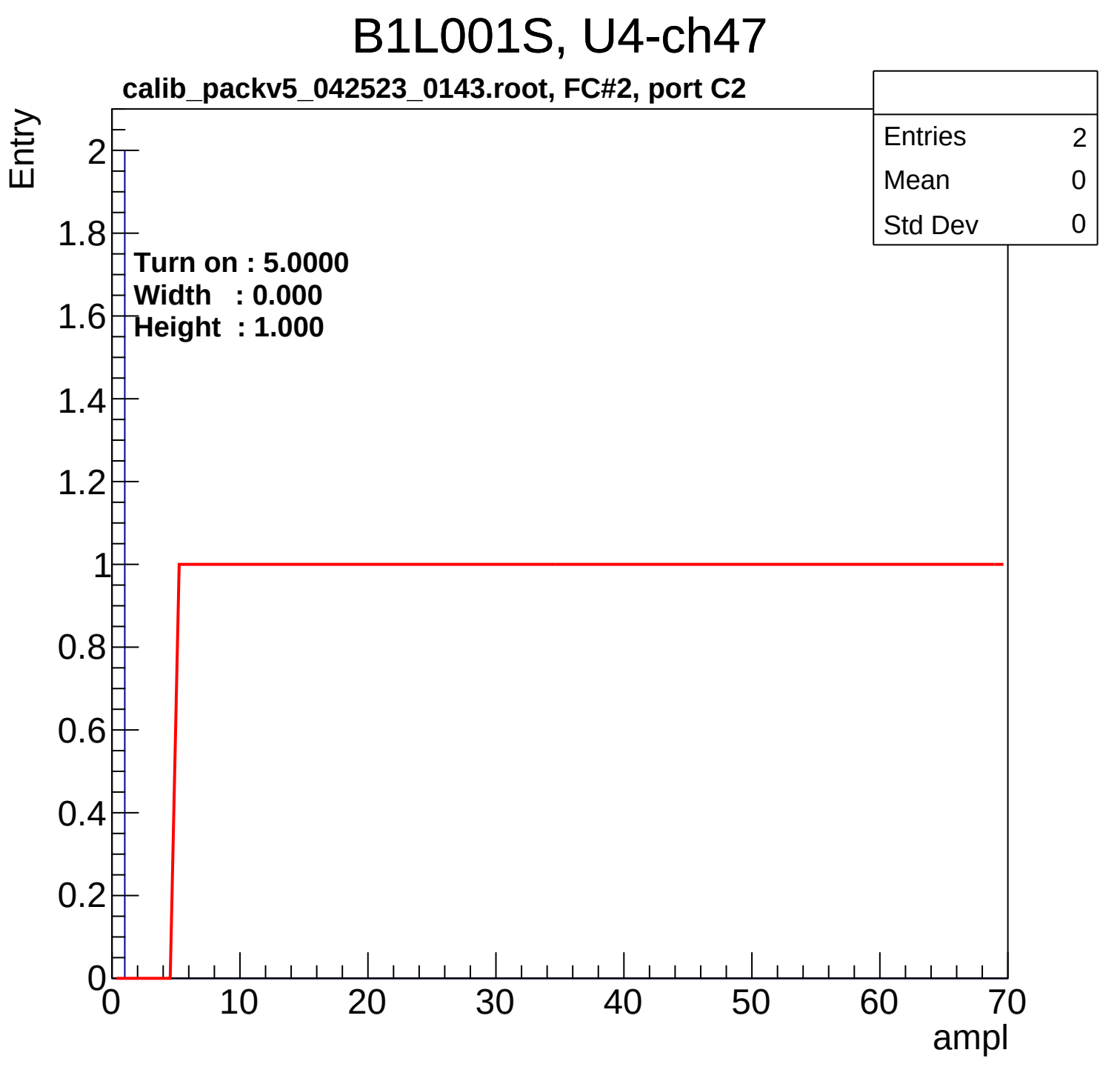
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L001S, U4-ch47
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
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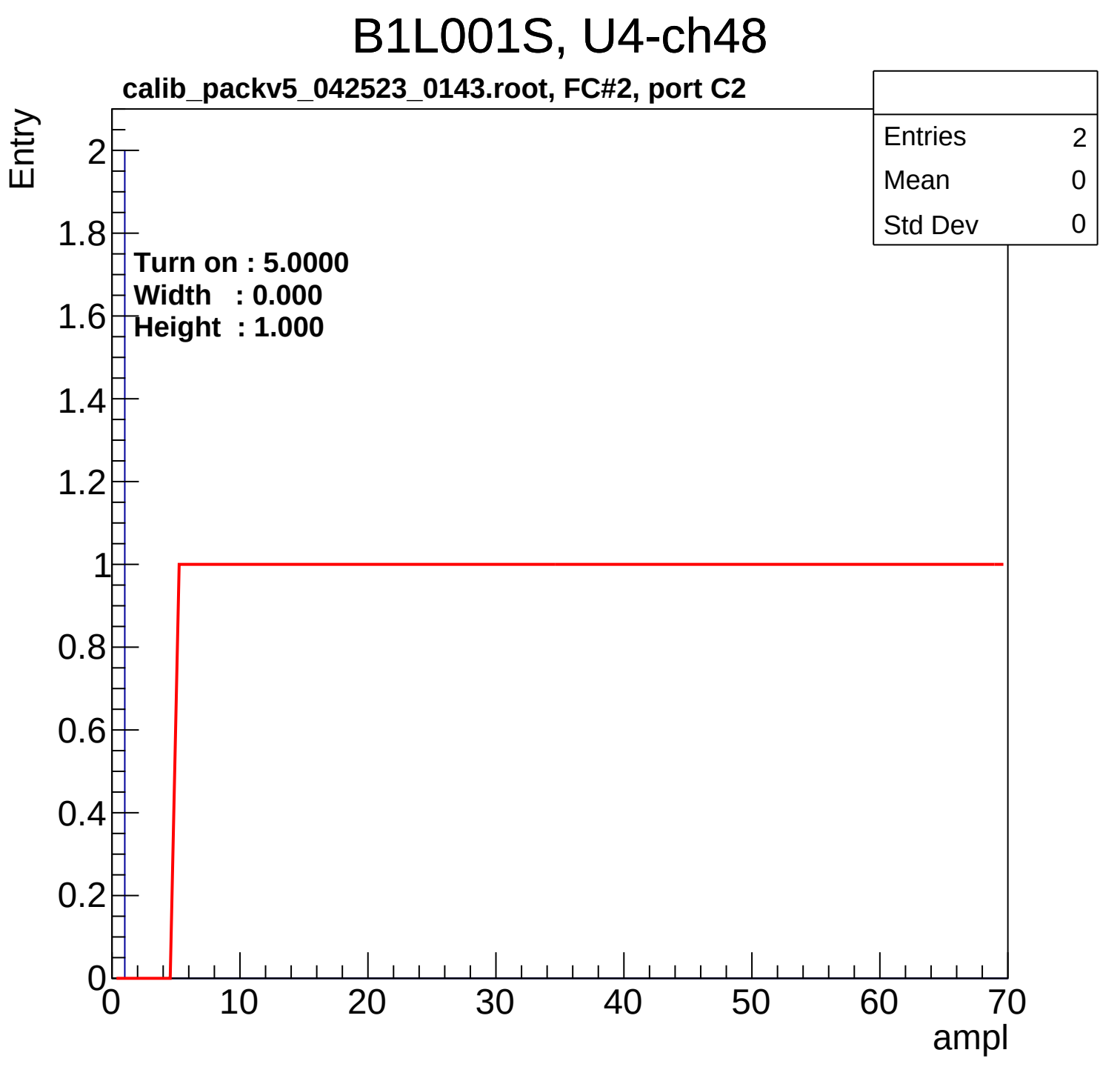
20
30
40
50
60
70


B1L001S, U4-ch48
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
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20
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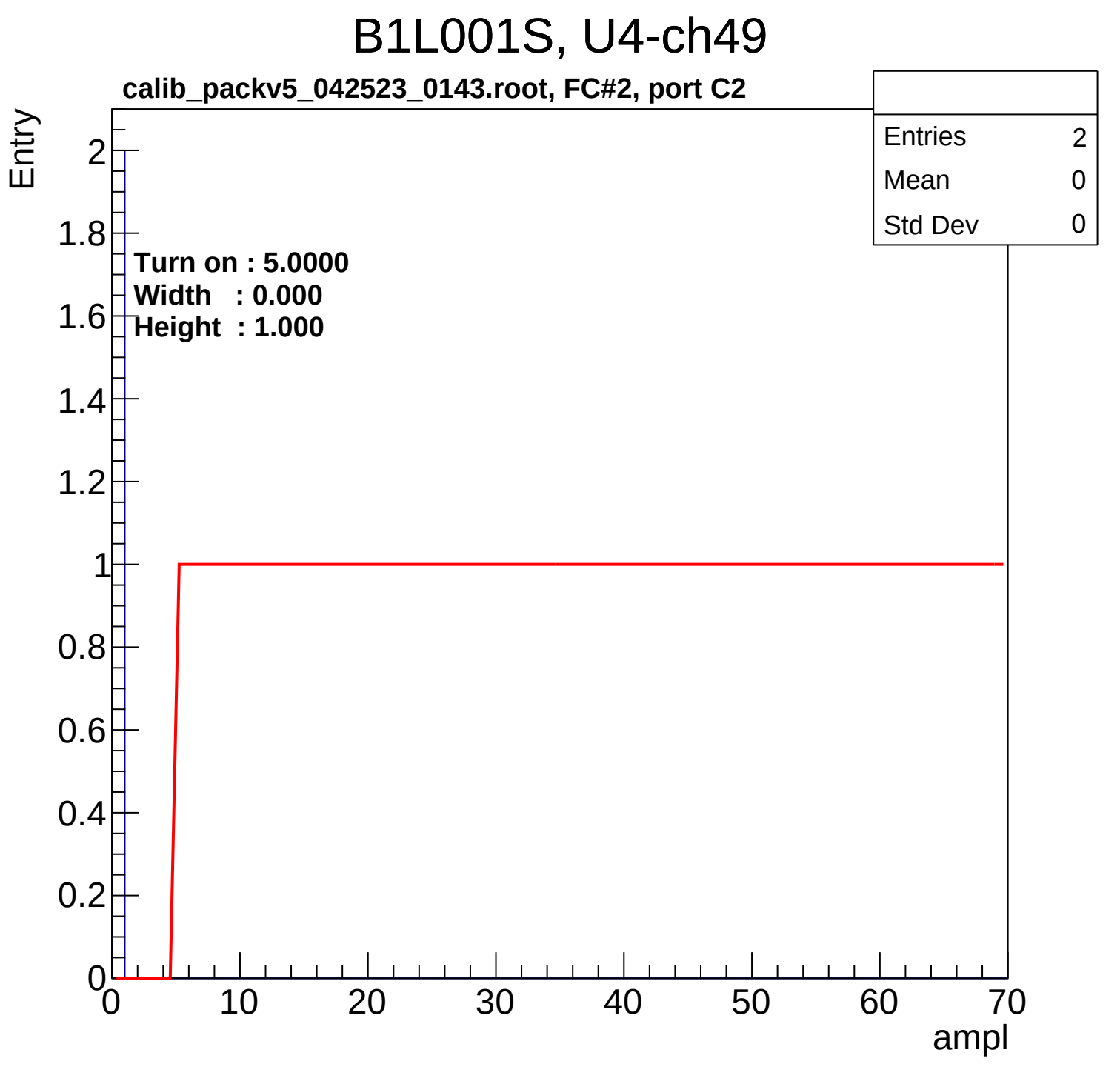
B1L001S, U4-ch49
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
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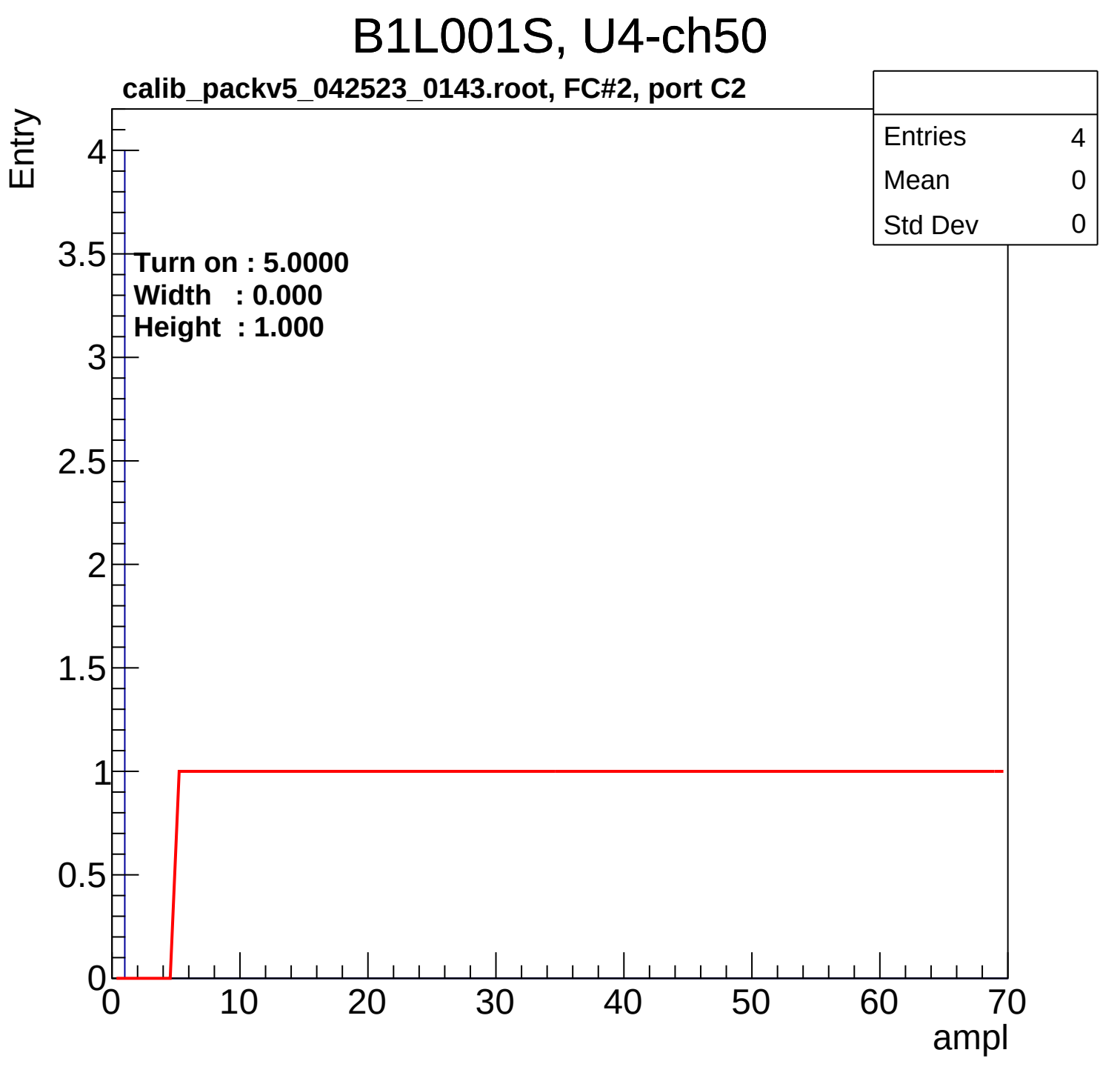
B1L001S, U4-ch50
calib_packv5_042523_0143.root, FC#2, port C2
Entries 4
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
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1
1.5
2
2.5
3
3.5
4
0
10
20
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40
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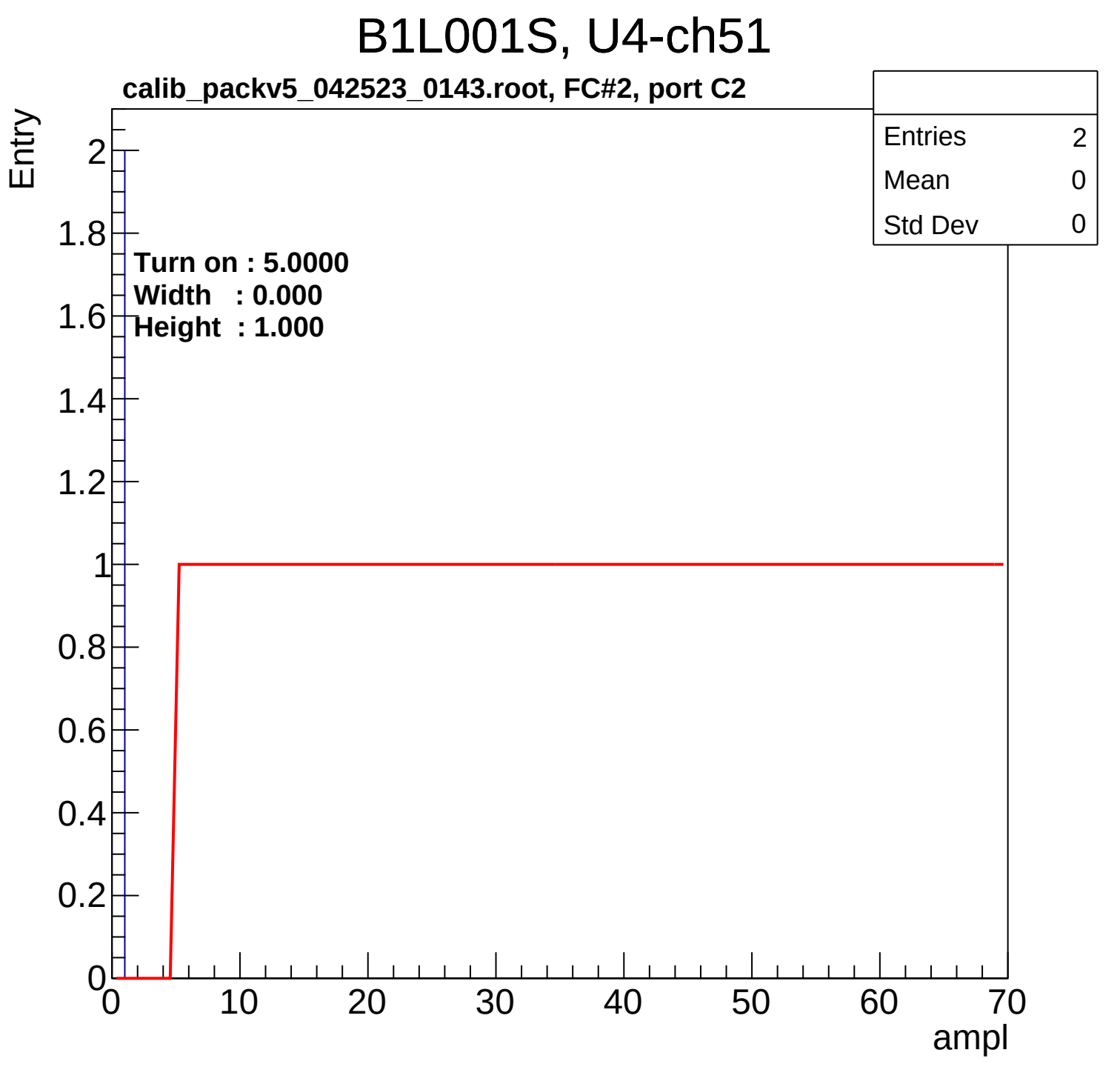
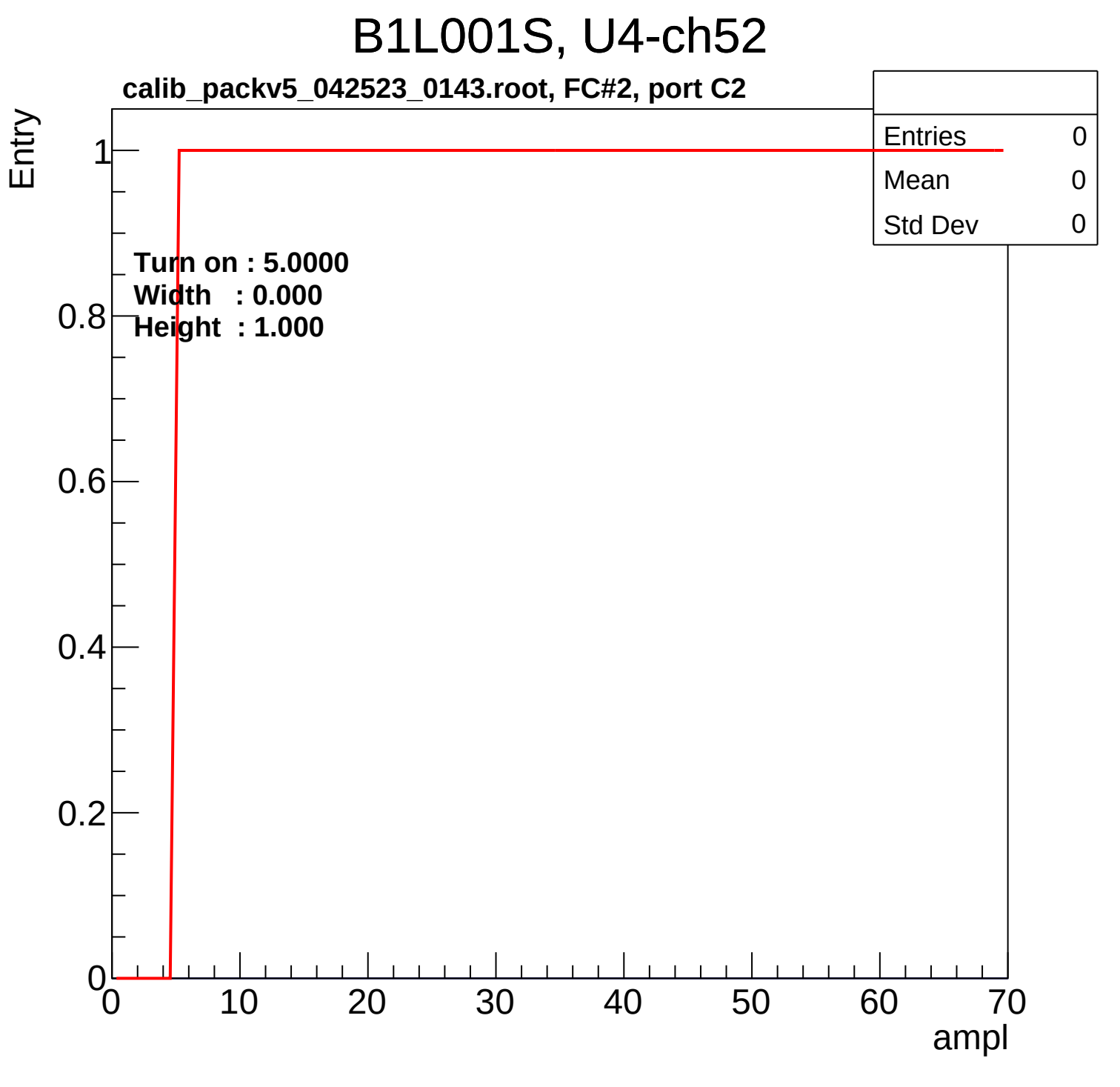
60
70


B1L001S, U4-ch51
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L001S, U4-ch52
calib_packv5_042523_0143.root, FC#2, port C2
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
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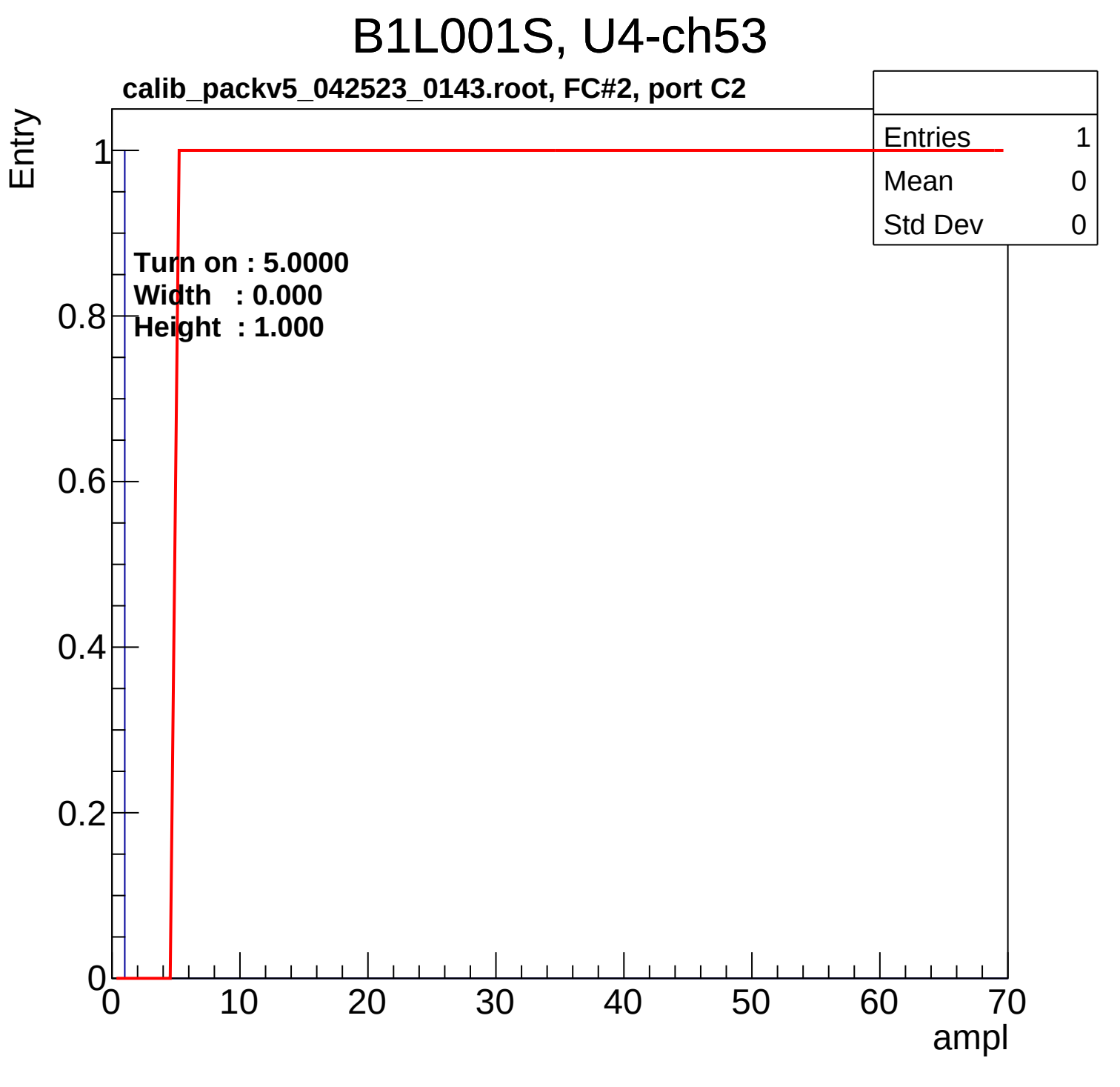
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L001S, U4-ch53
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
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40
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60
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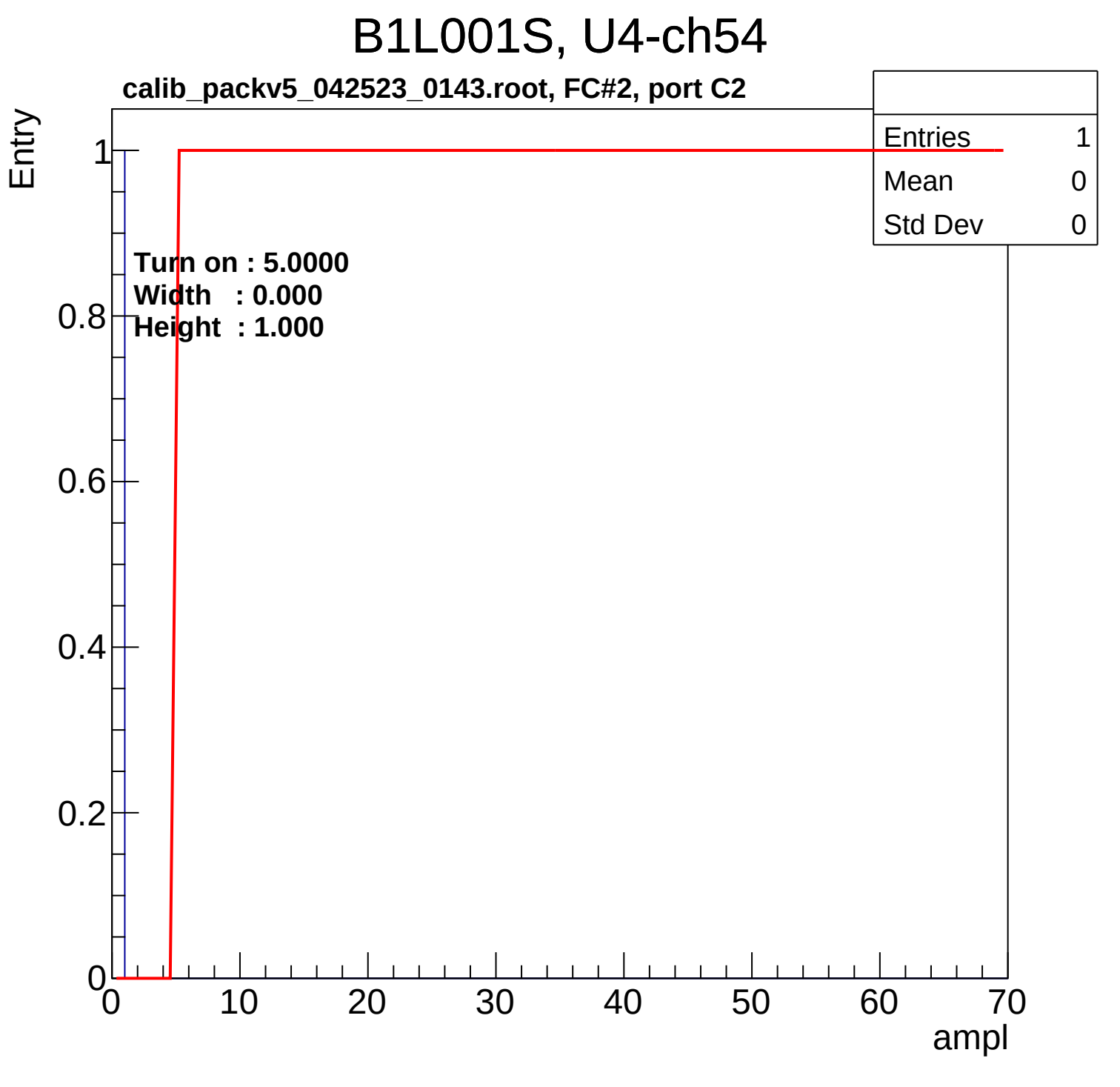
B1L001S, U4-ch54
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
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0.8
0.6
0.4
0.2
0
0
10
20
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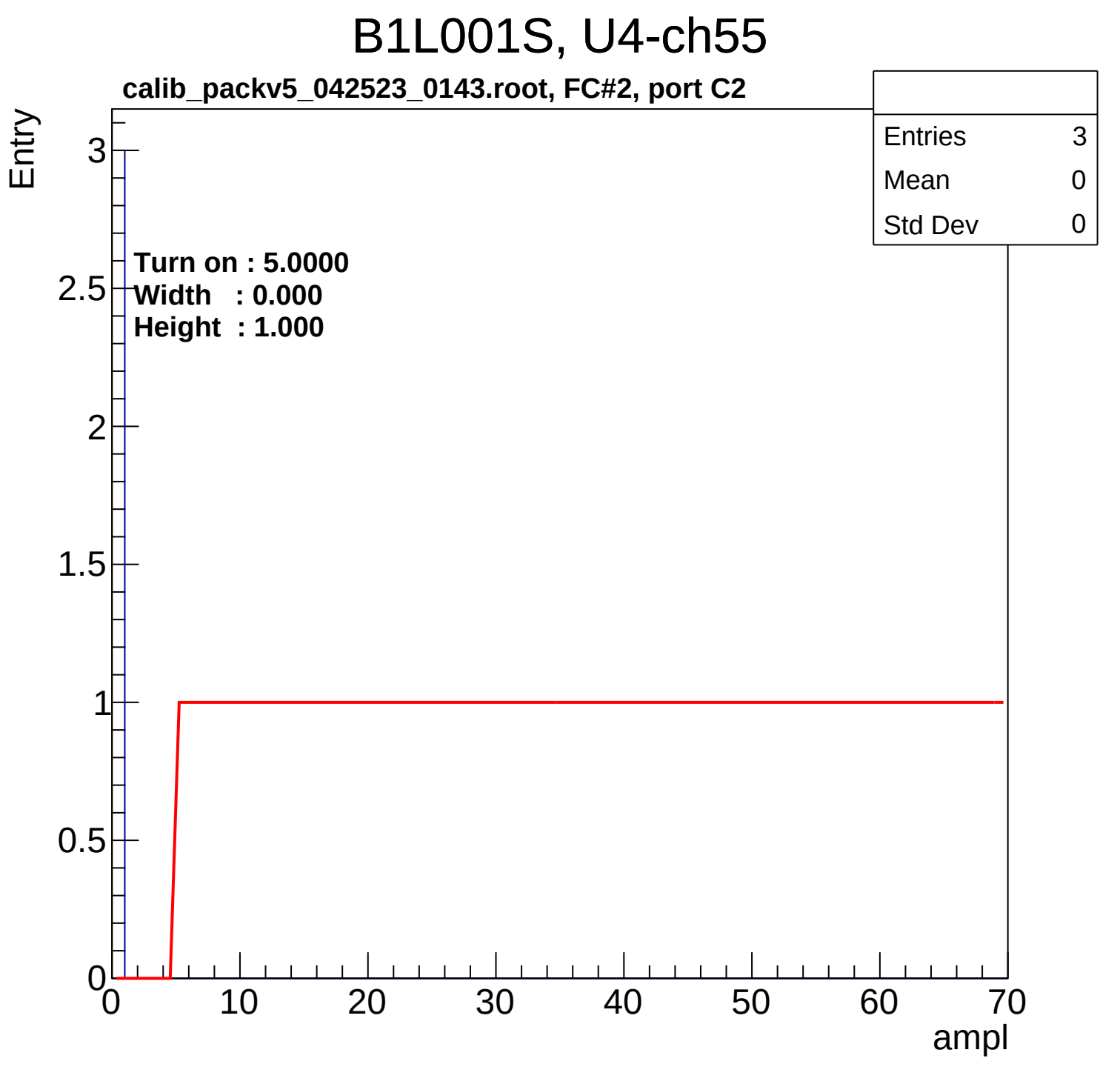
40
50
60
70
ampl


B1L001S, U4-ch55
calib_packv5_042523_0143.root, FC#2, port C2
Entries 3
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
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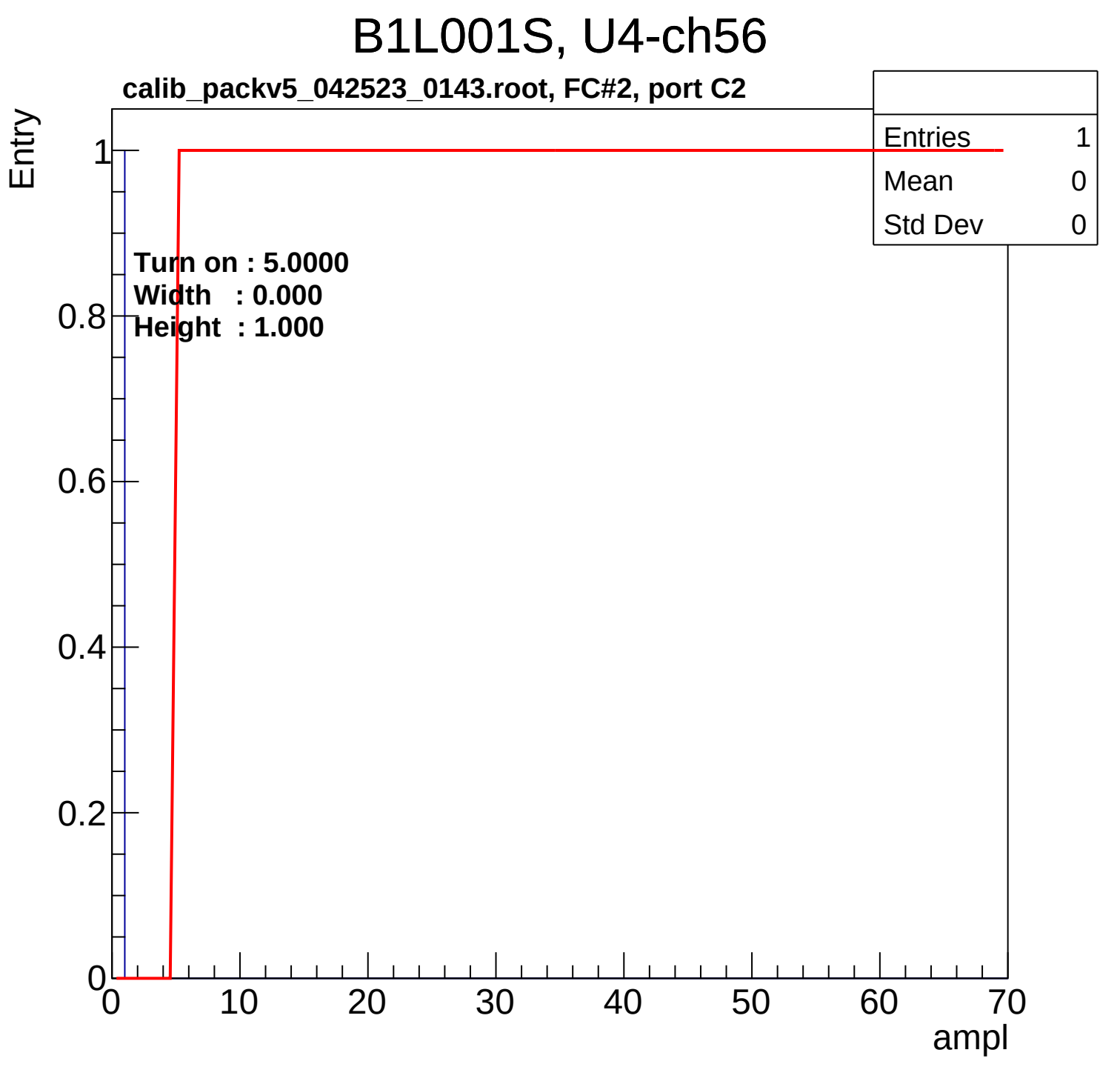
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L001S, U4-ch56
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
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0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
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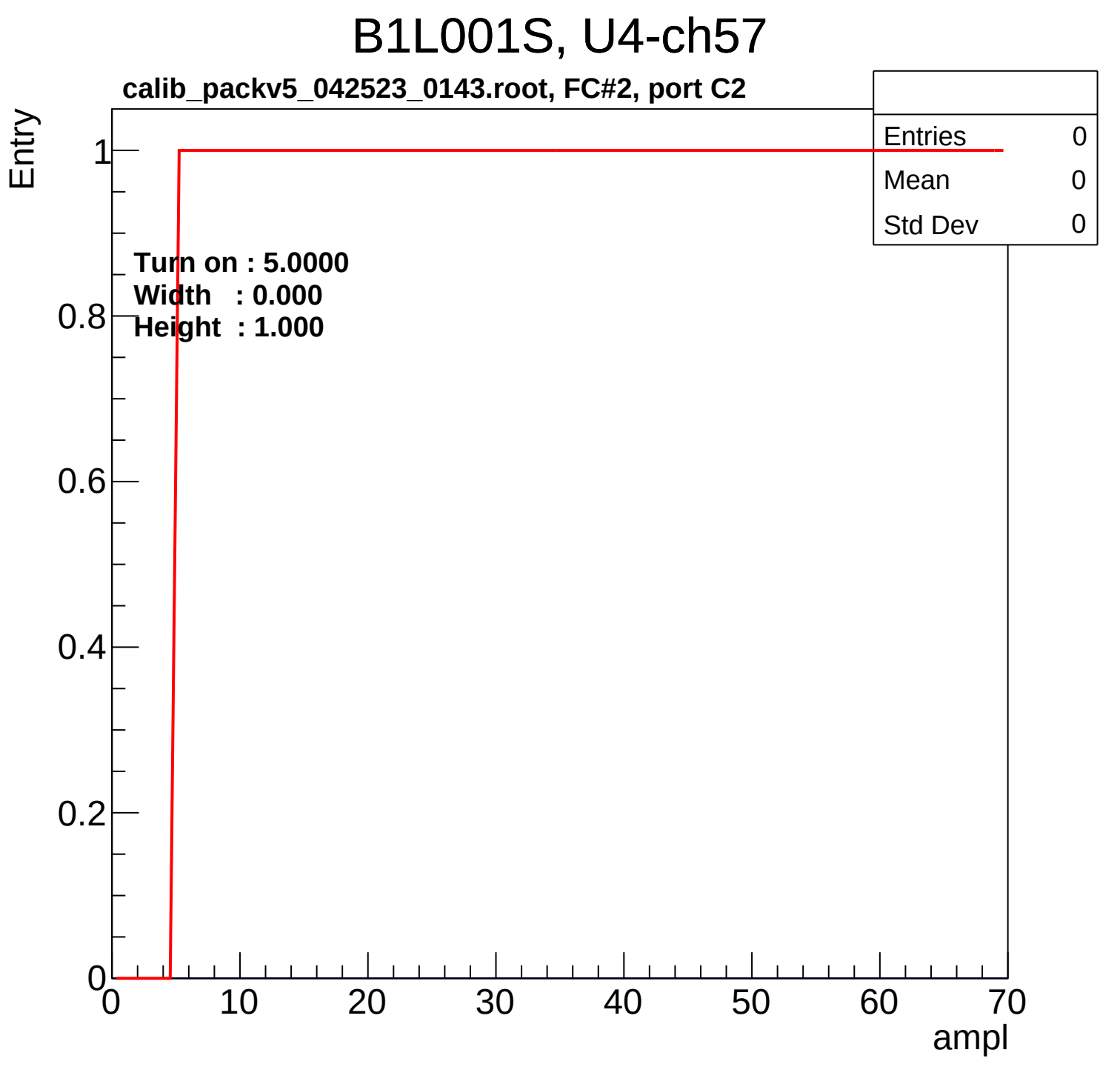
B1L001S, U4-ch57
calib_packv5_042523_0143.root, FC#2, port C2
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
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0.4
0.2
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20
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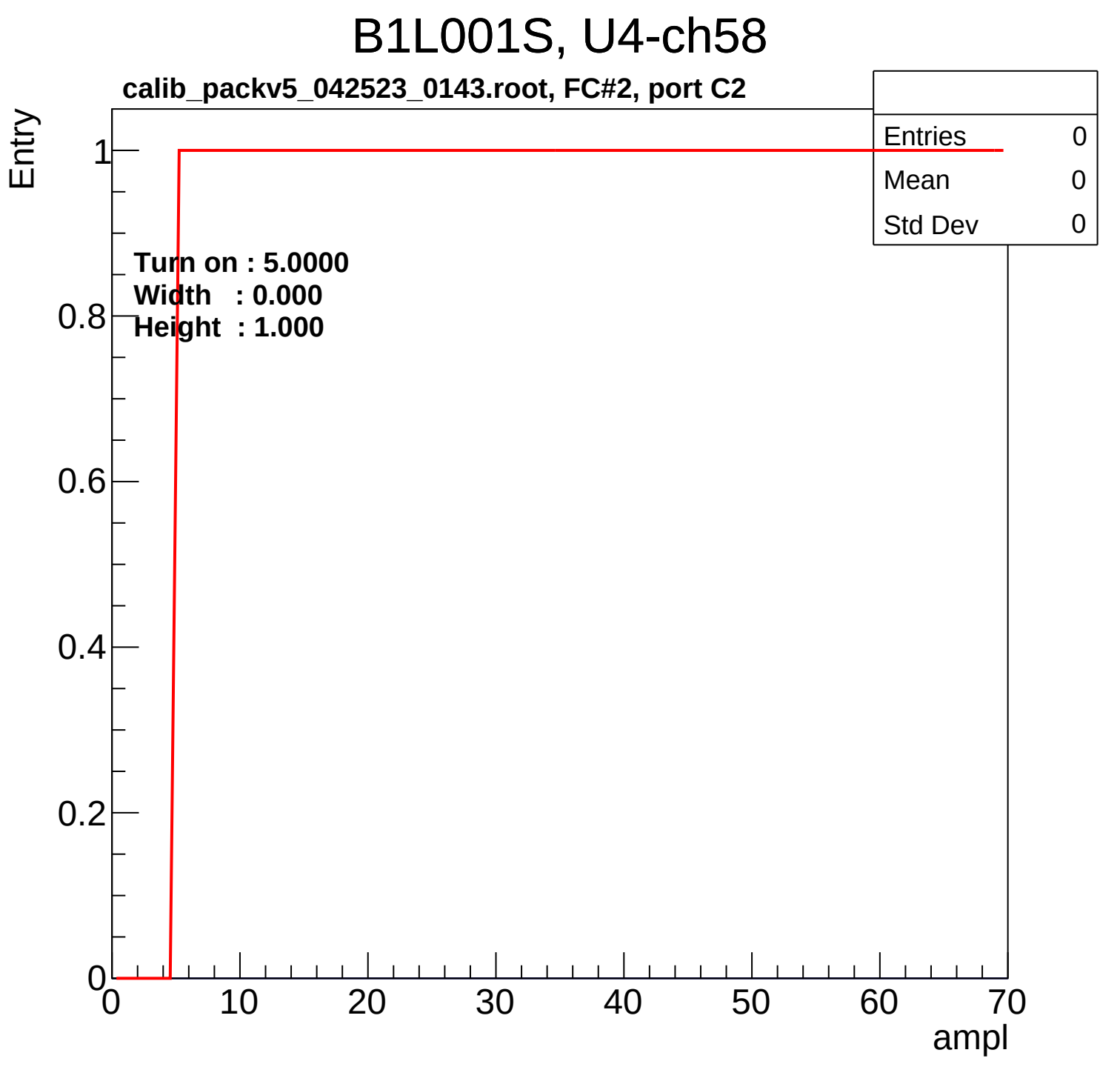
ampl


B1L001S, U4-ch58
calib_packv5_042523_0143.root, FC#2, port C2
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
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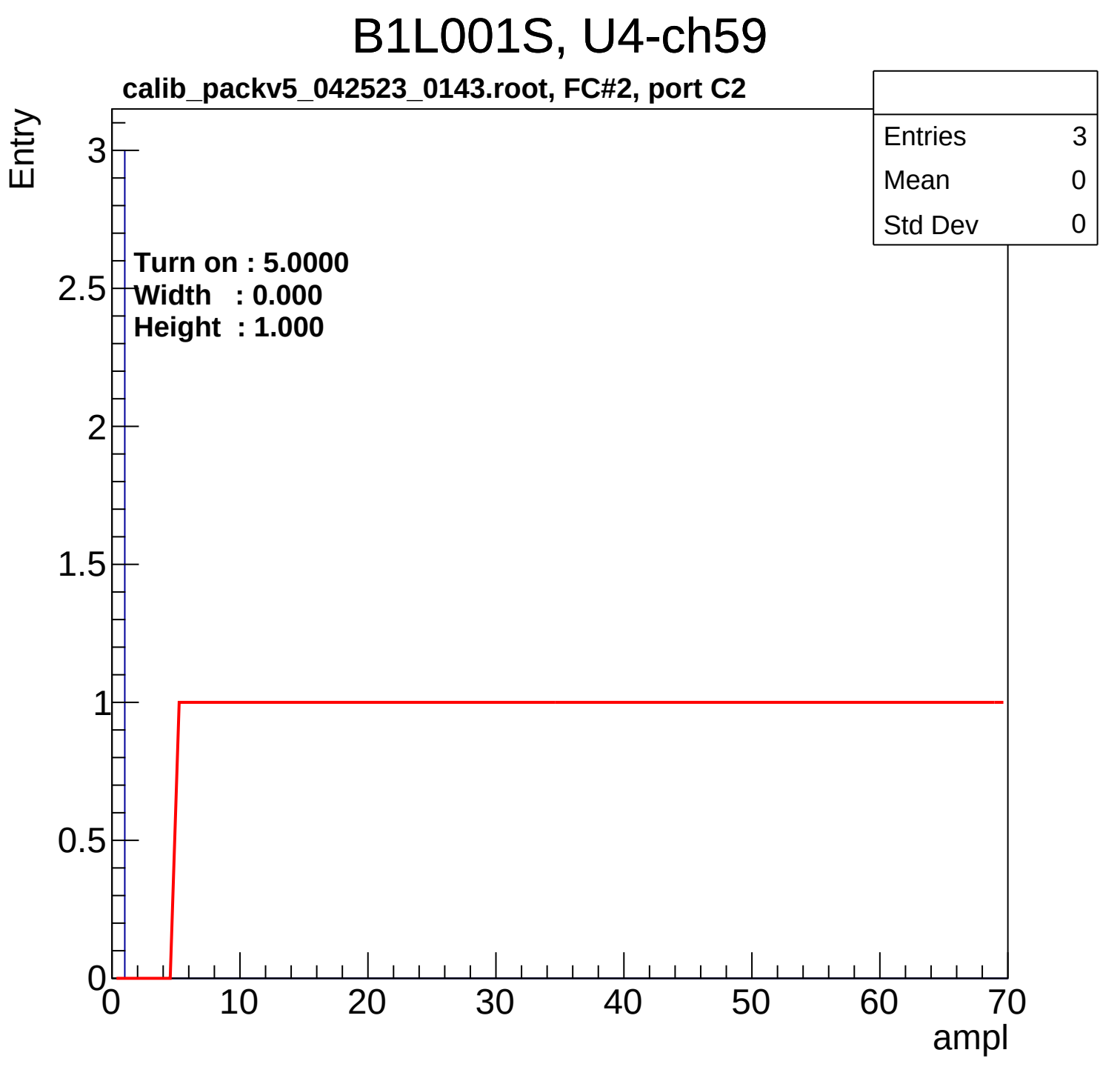
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L001S, U4-ch59
calib_packv5_042523_0143.root, FC#2, port C2
Entries 3
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
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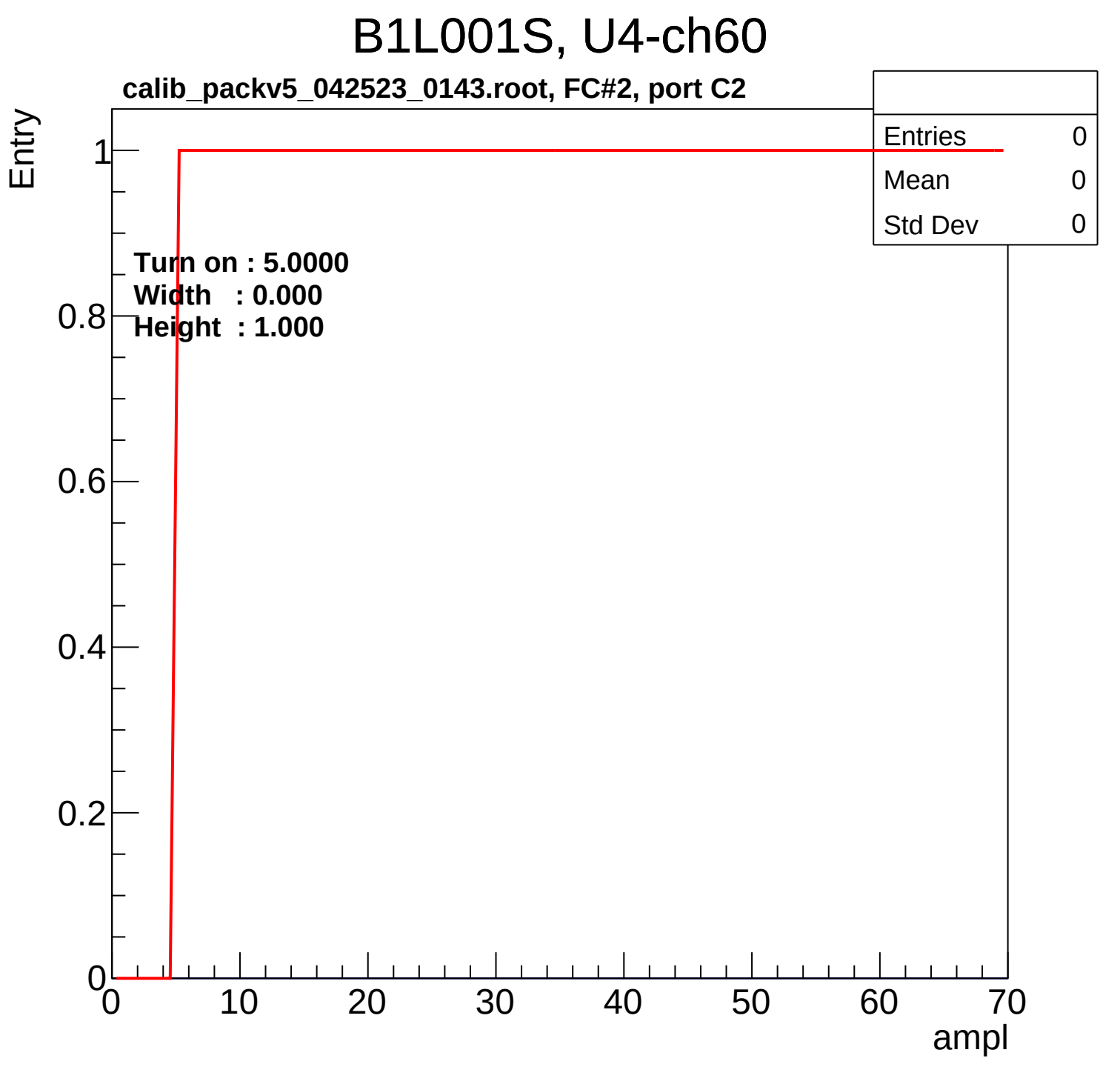
B1L001S, U4-ch60
calib_packv5_042523_0143.root, FC#2, port C2
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
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0.6
0.4
0.2
0
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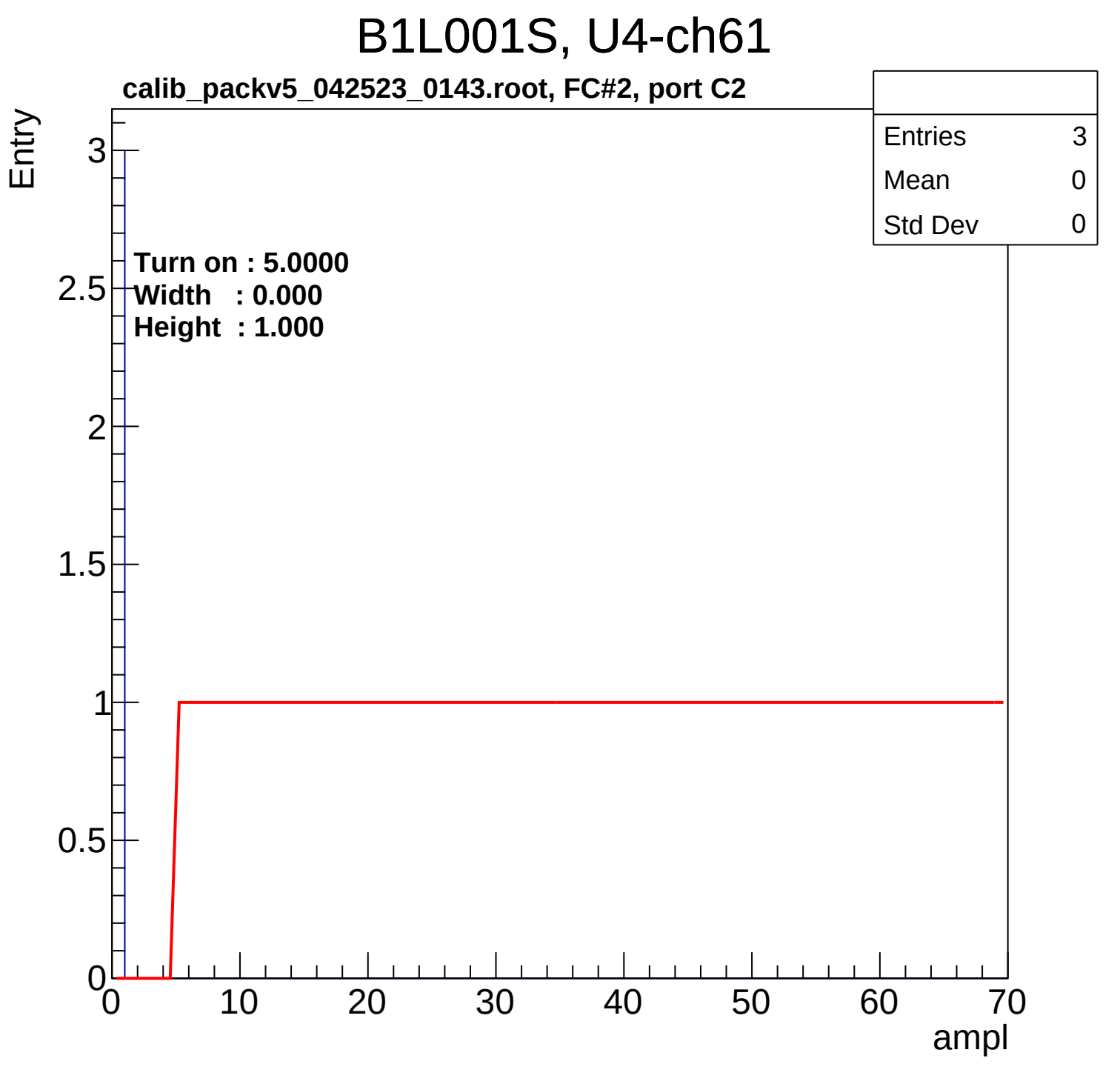
ampl


B1L001S, U4-ch61
calib_packv5_042523_0143.root, FC#2, port C2
Entries 3
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
10
20
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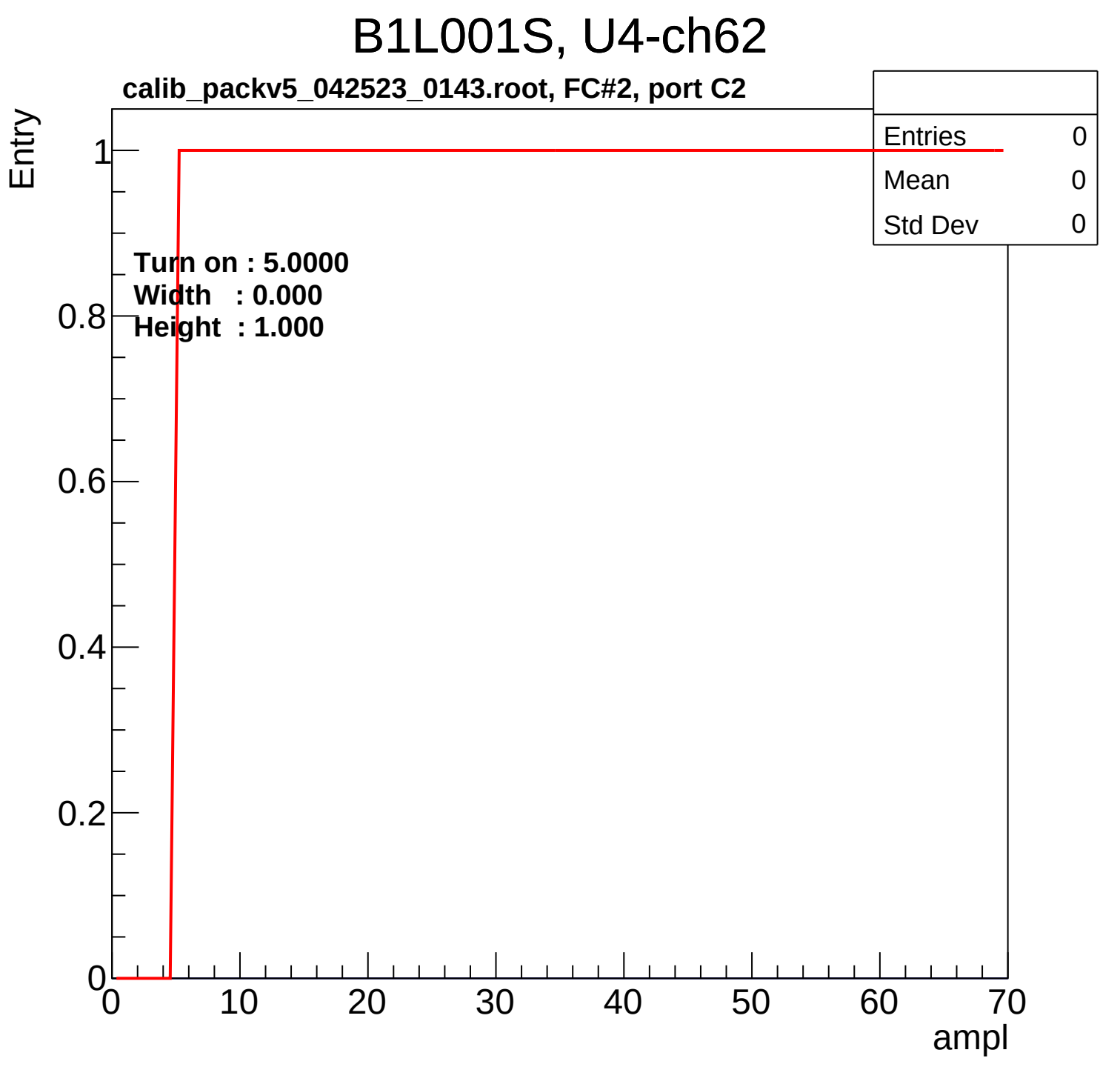
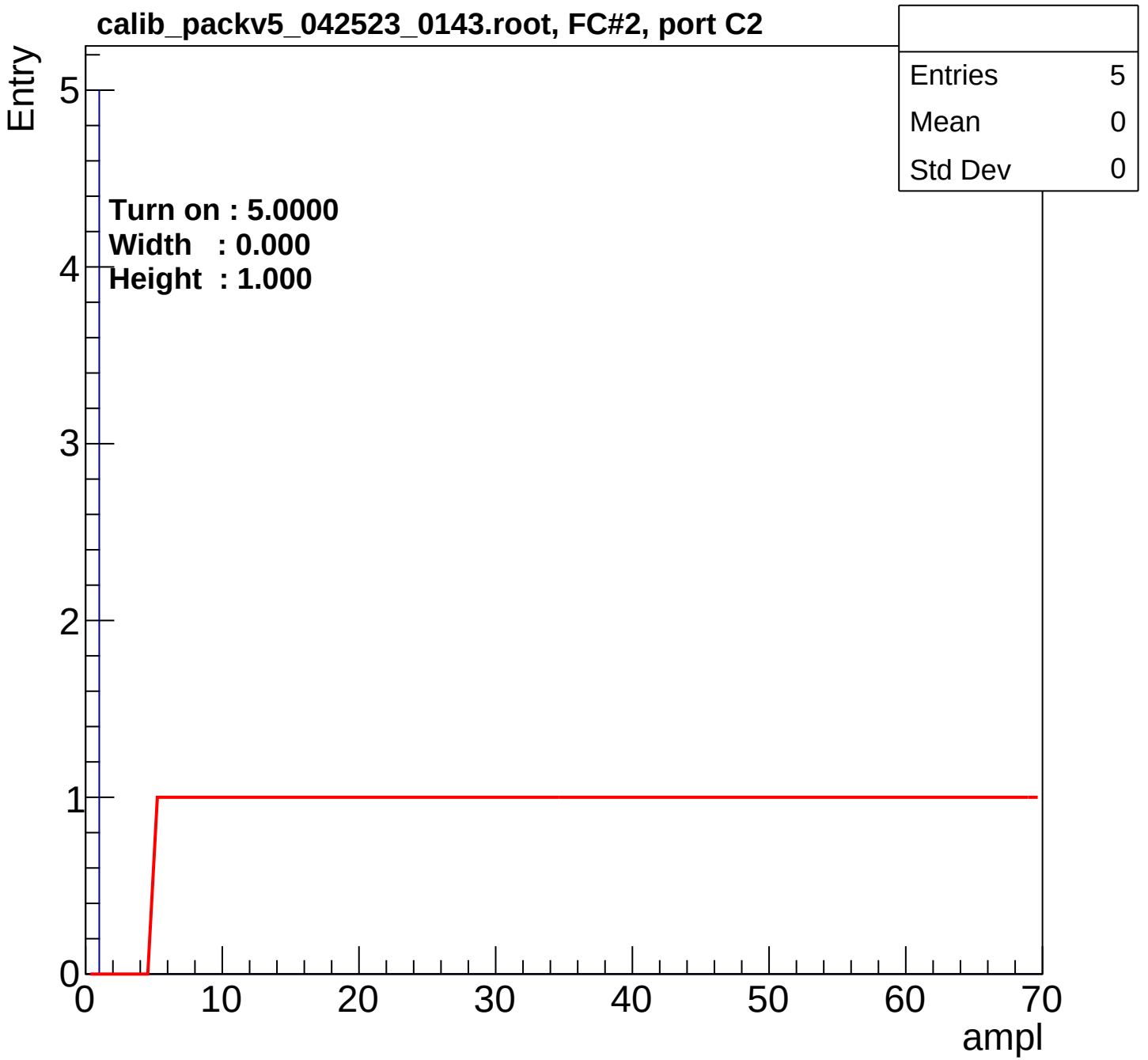
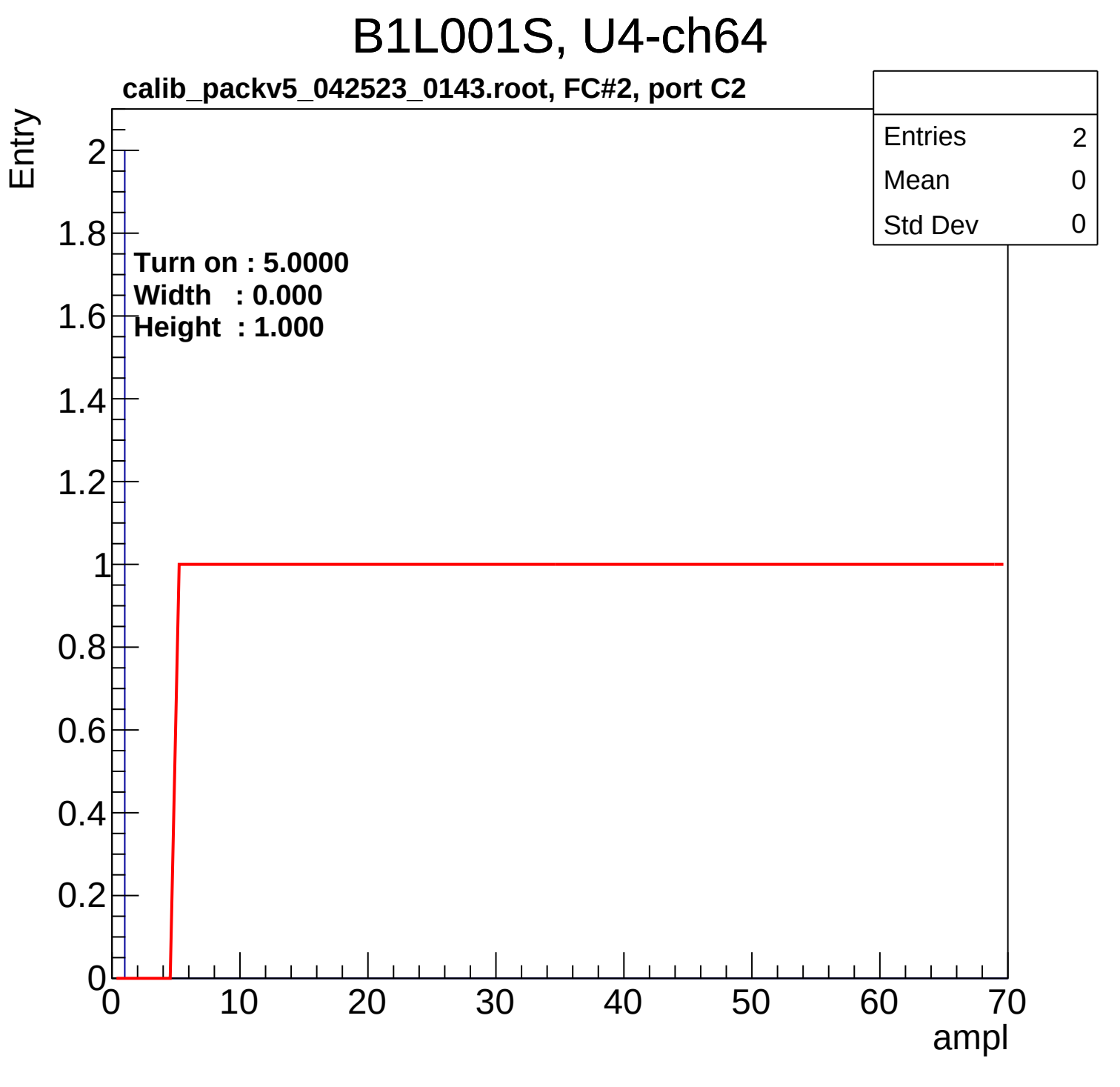
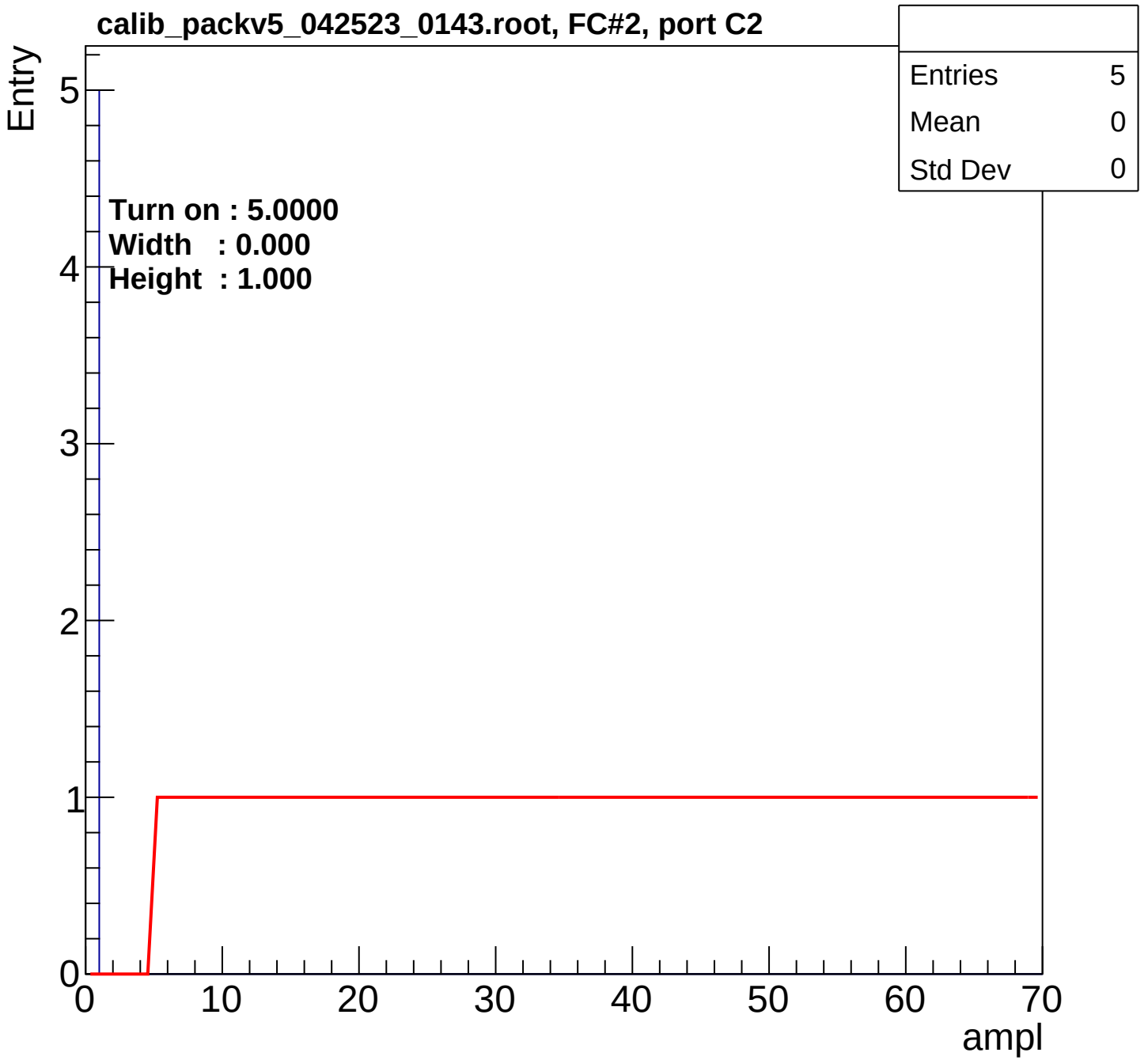
40
50
60
70


B1L001S, U4-ch62
calib_packv5_042523_0143.root, FC#2, port C2
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L001S, U4-ch63
calib_packv5_042523_0143.root, FC#2, port C2
Entries 5
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L001S, U4-ch64
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L001S, U4-ch65
calib_packv5_042523_0143.root, FC#2, port C2
Entries 5
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
0
1
2
3
4
5
0
10
20
30
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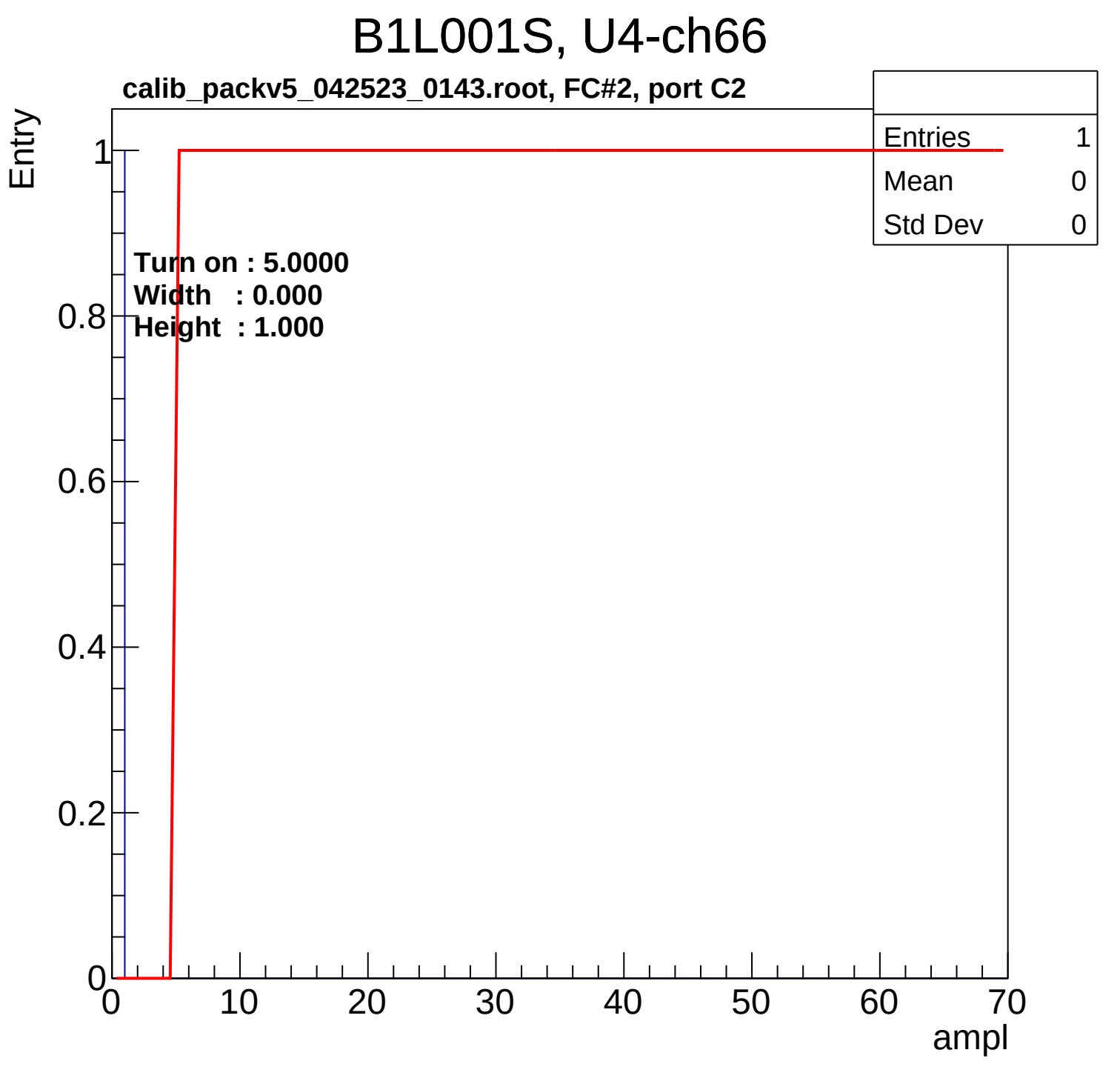
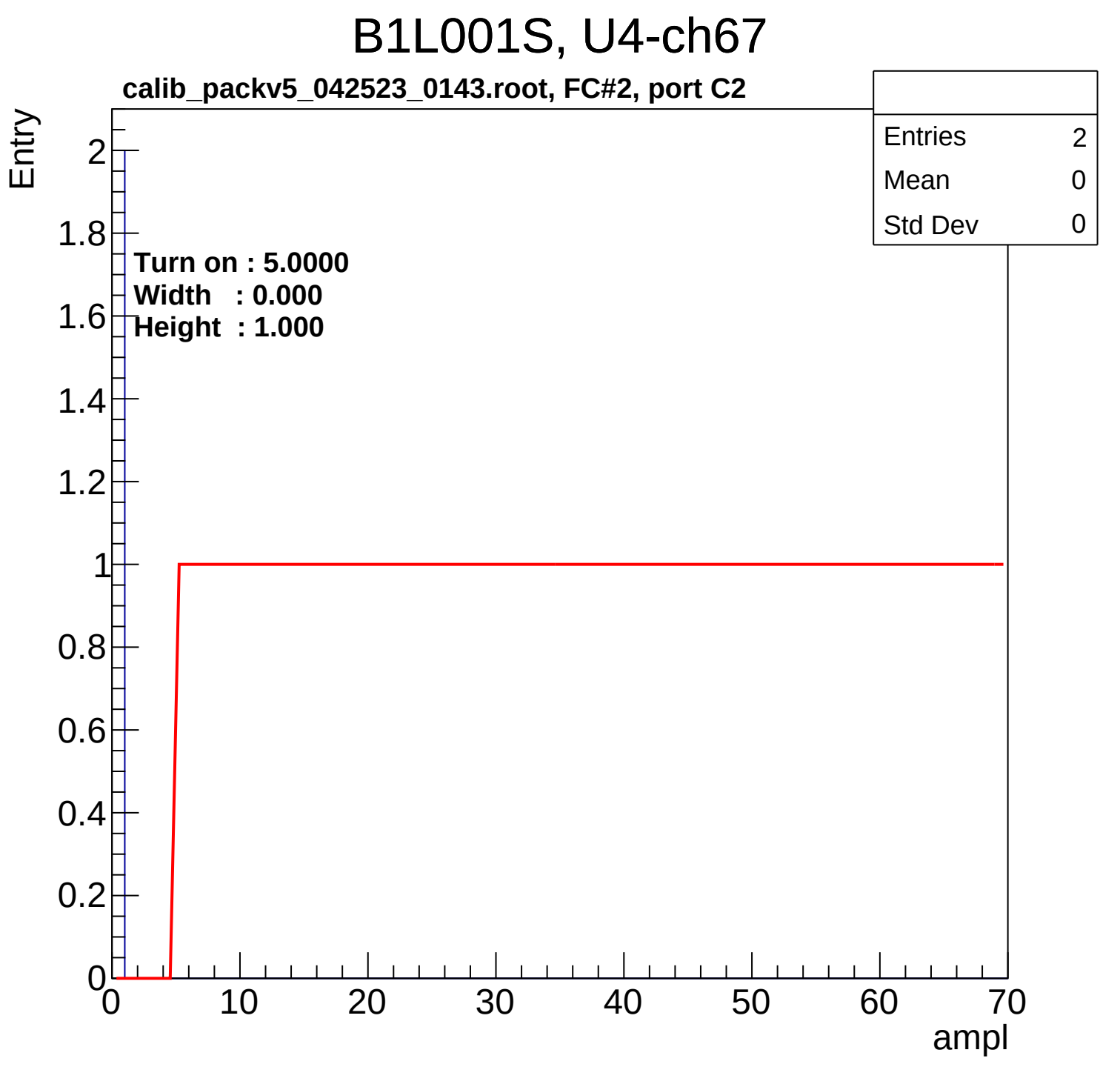
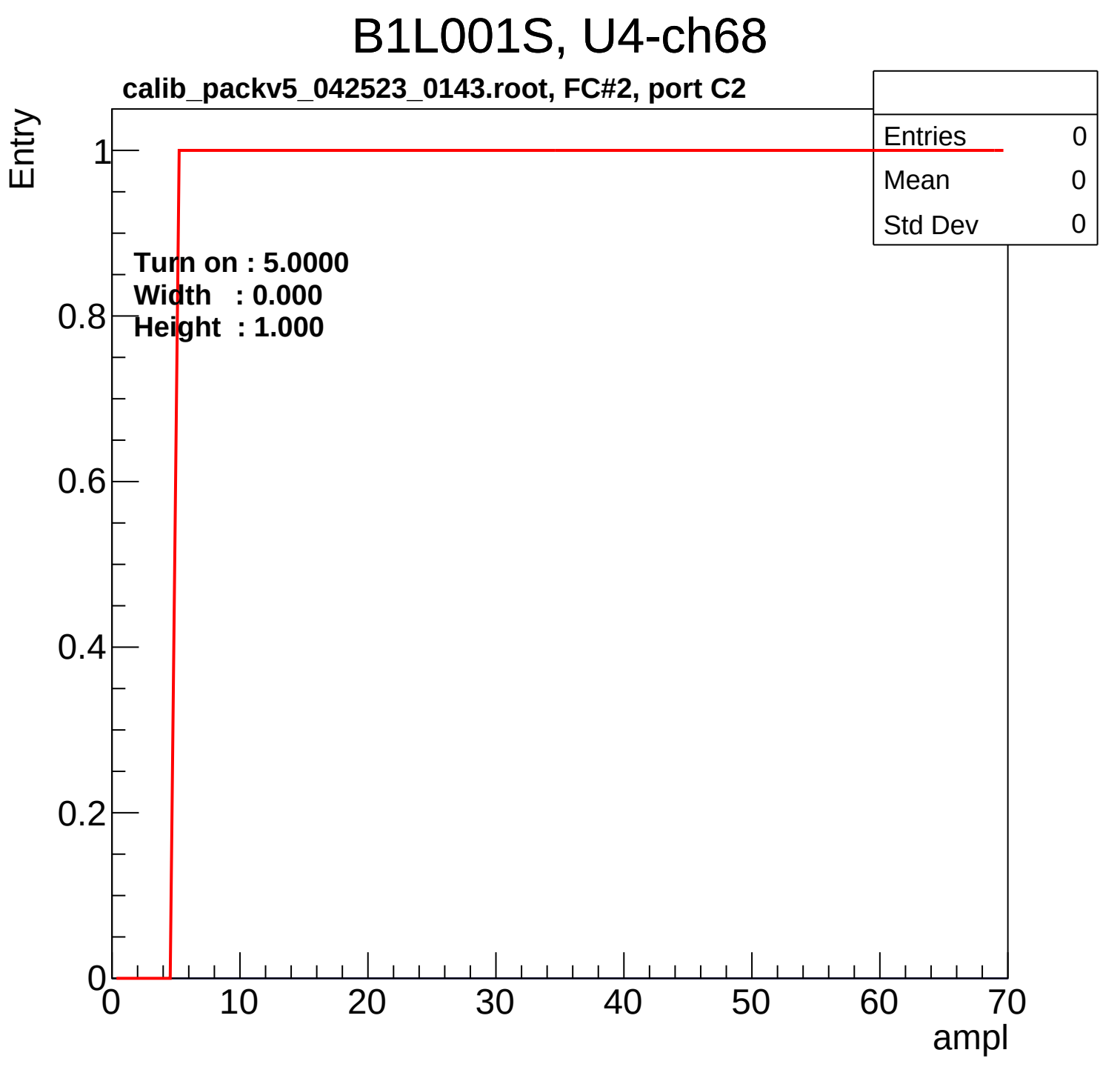
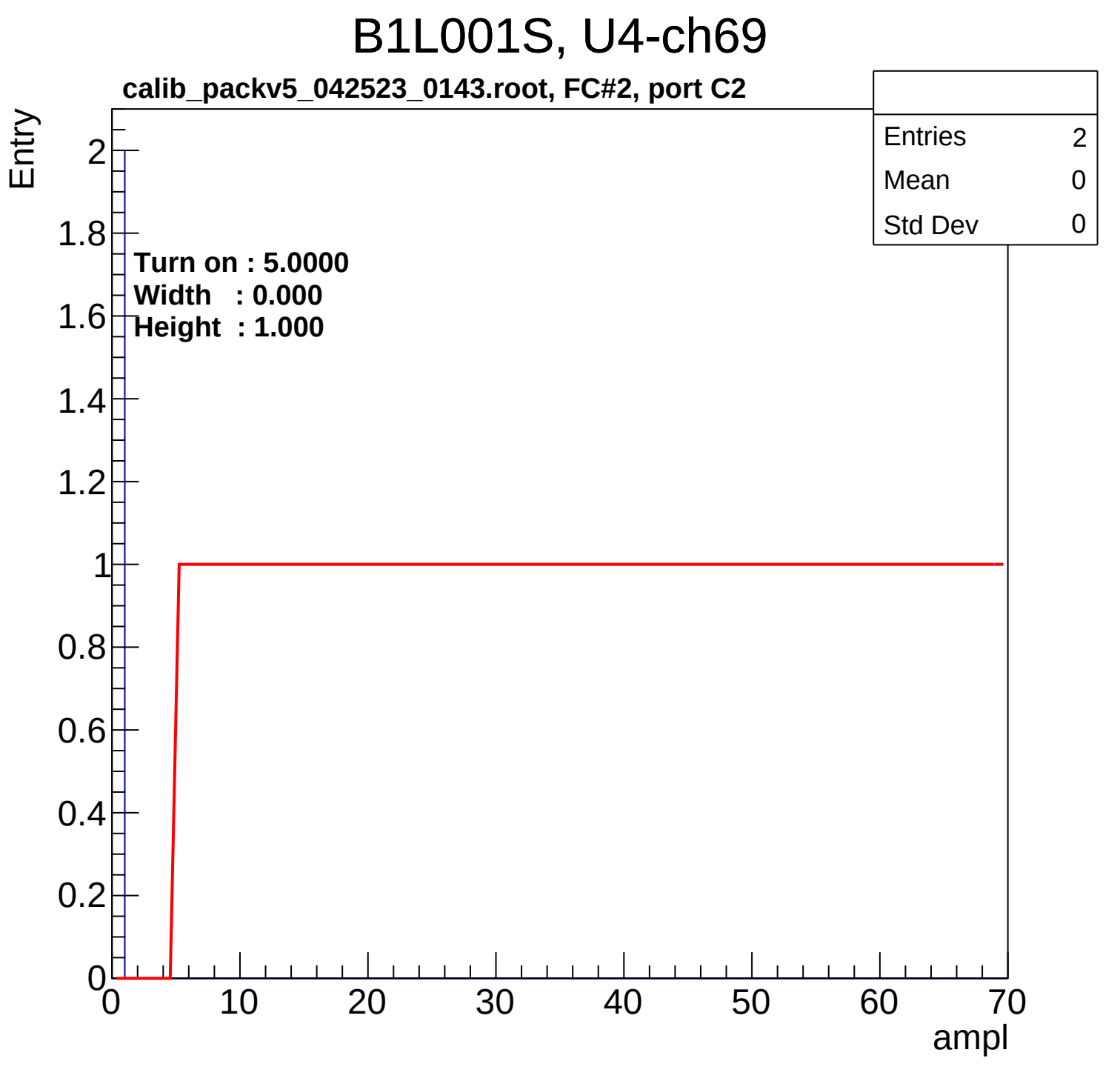
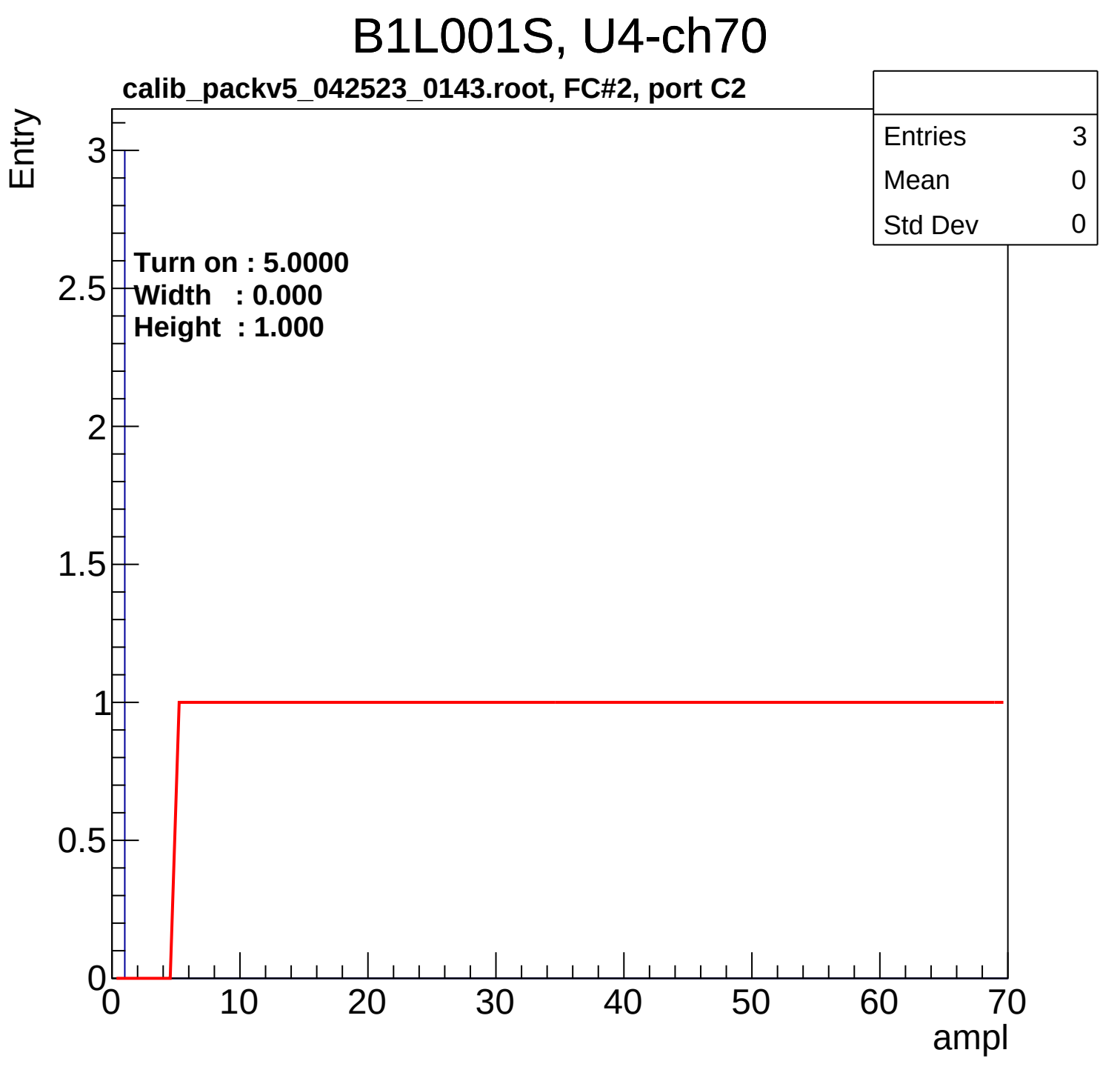
50
60
70
ampl


B1L001S, U4-ch66
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L001S, U4-ch67
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L001S, U4-ch68
calib_packv5_042523_0143.root, FC#2, port C2
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L001S, U4-ch69
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L001S, U4-ch70
calib_packv5_042523_0143.root, FC#2, port C2
Entries 3
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
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60
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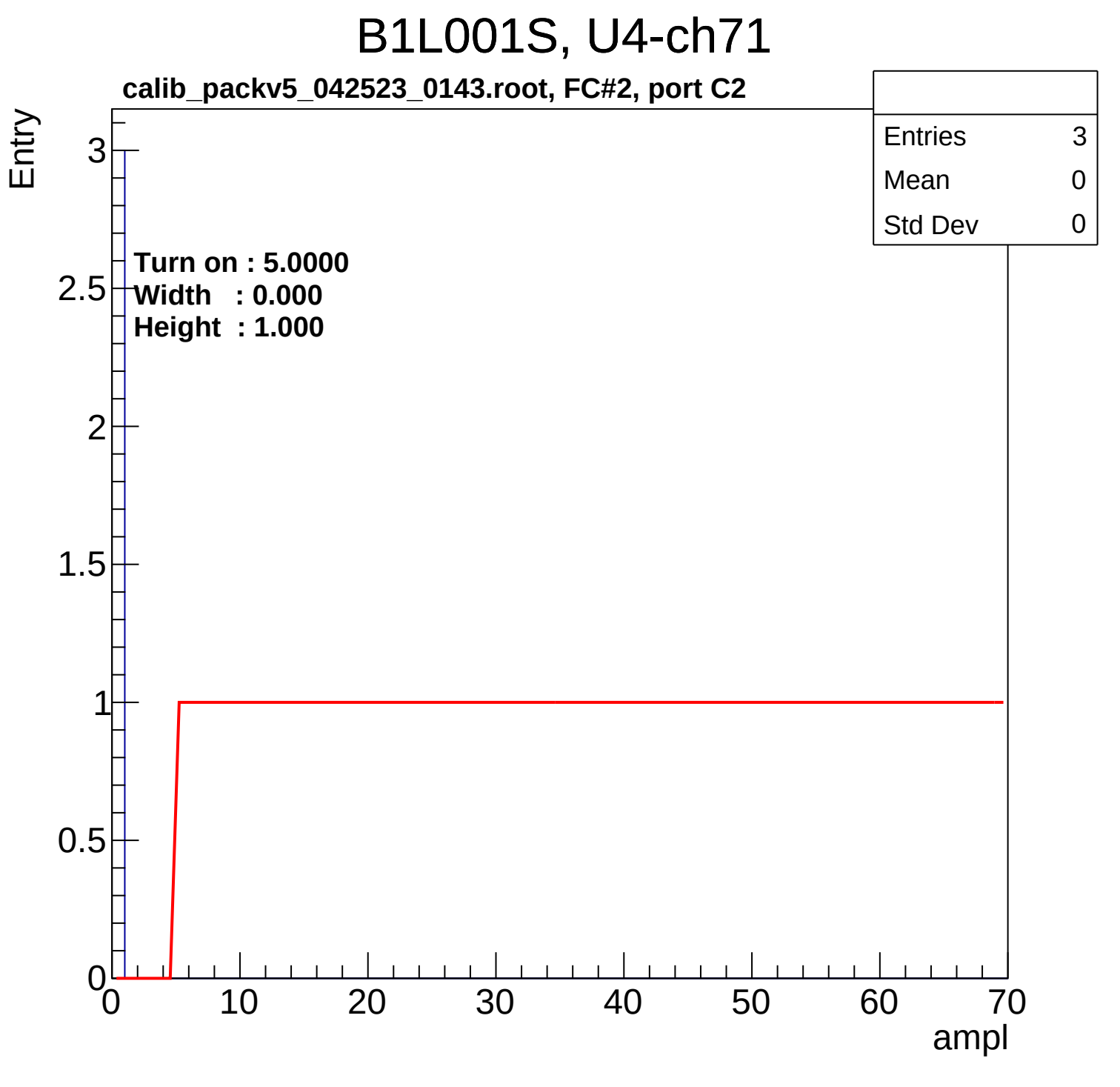
B1L001S, U4-ch71
calib_packv5_042523_0143.root, FC#2, port C2
Entries 3
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
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40
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60
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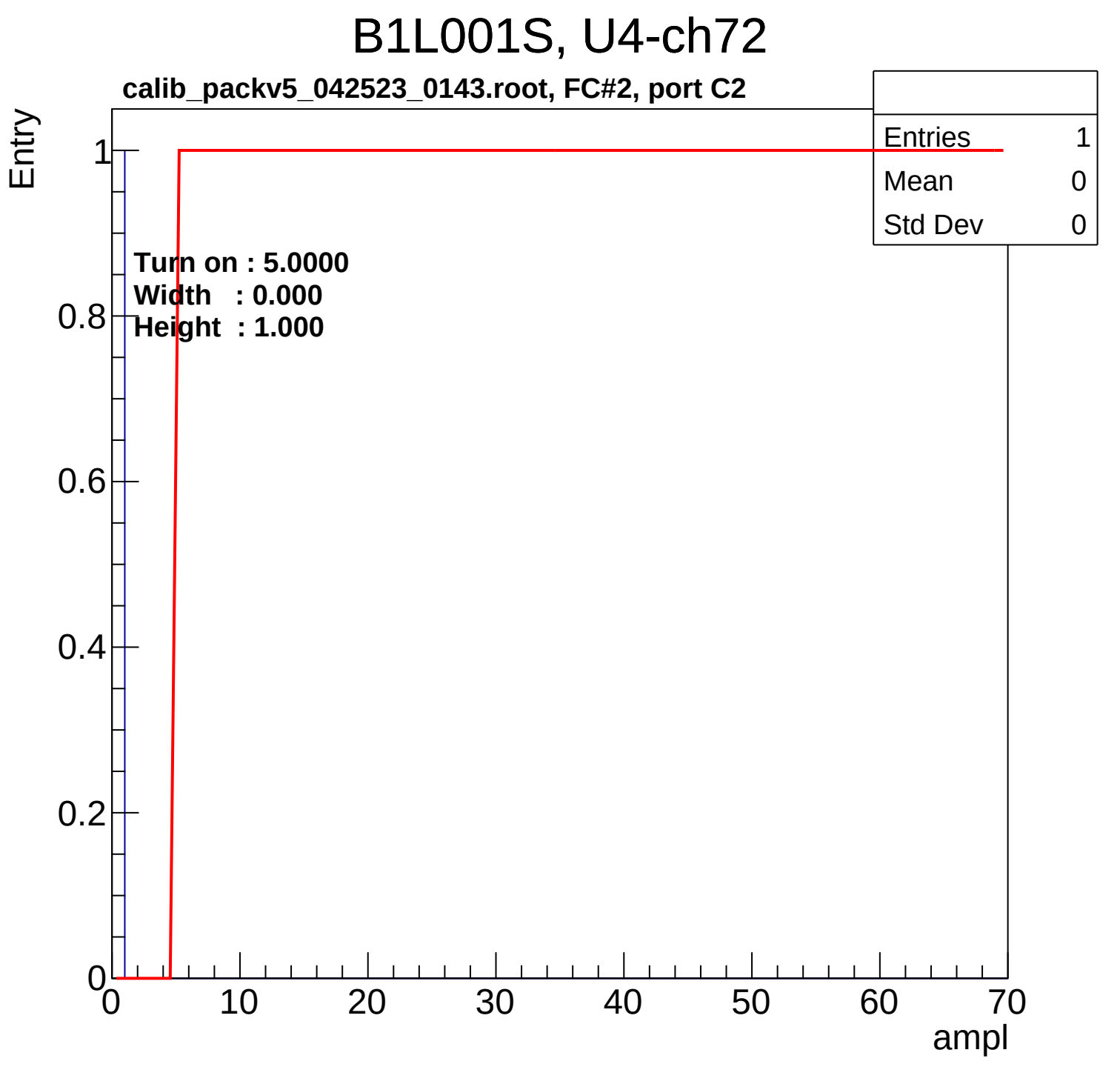
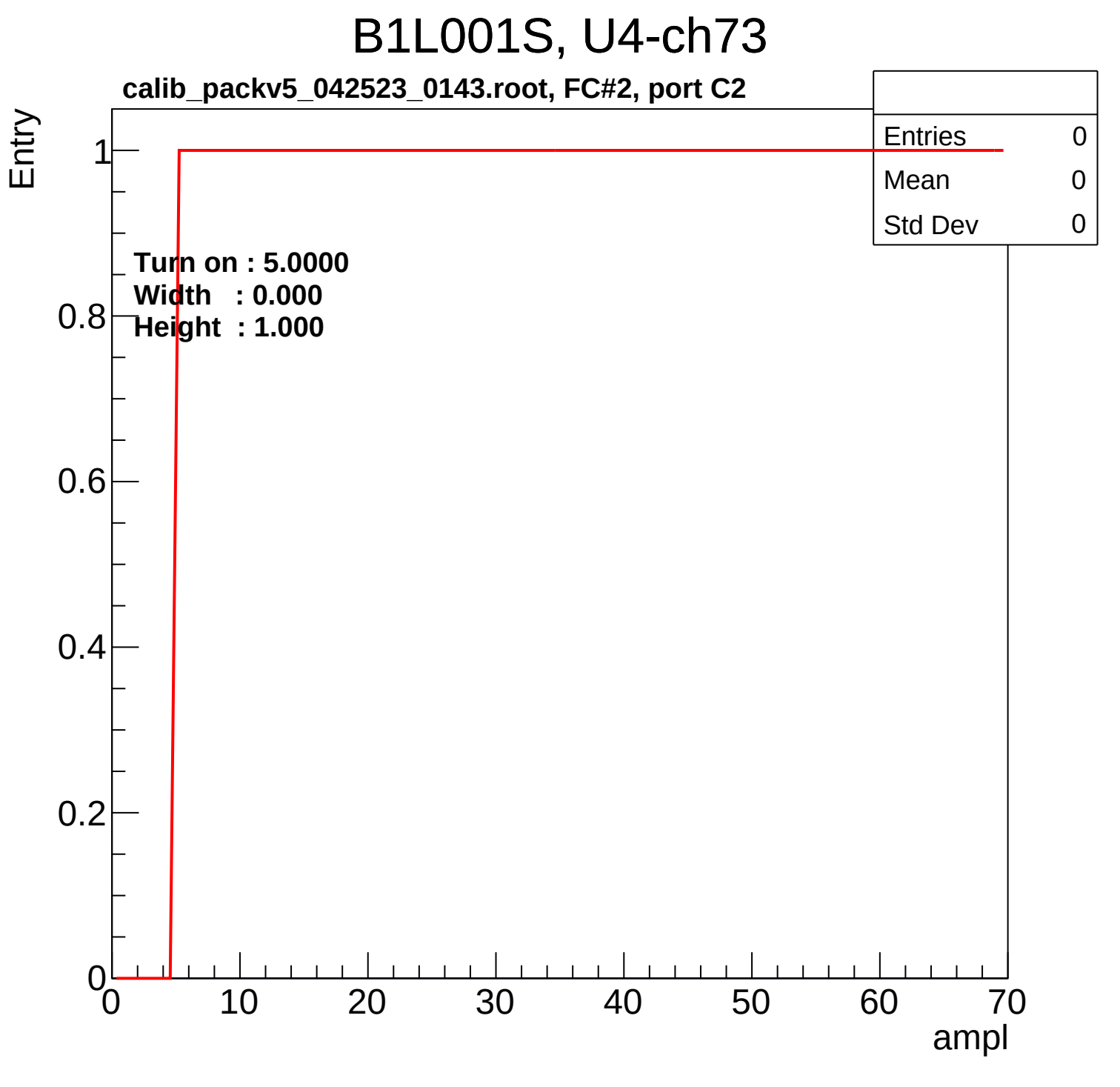

B1L001S, U4-ch72
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L001S, U4-ch73
calib_packv5_042523_0143.root, FC#2, port C2
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
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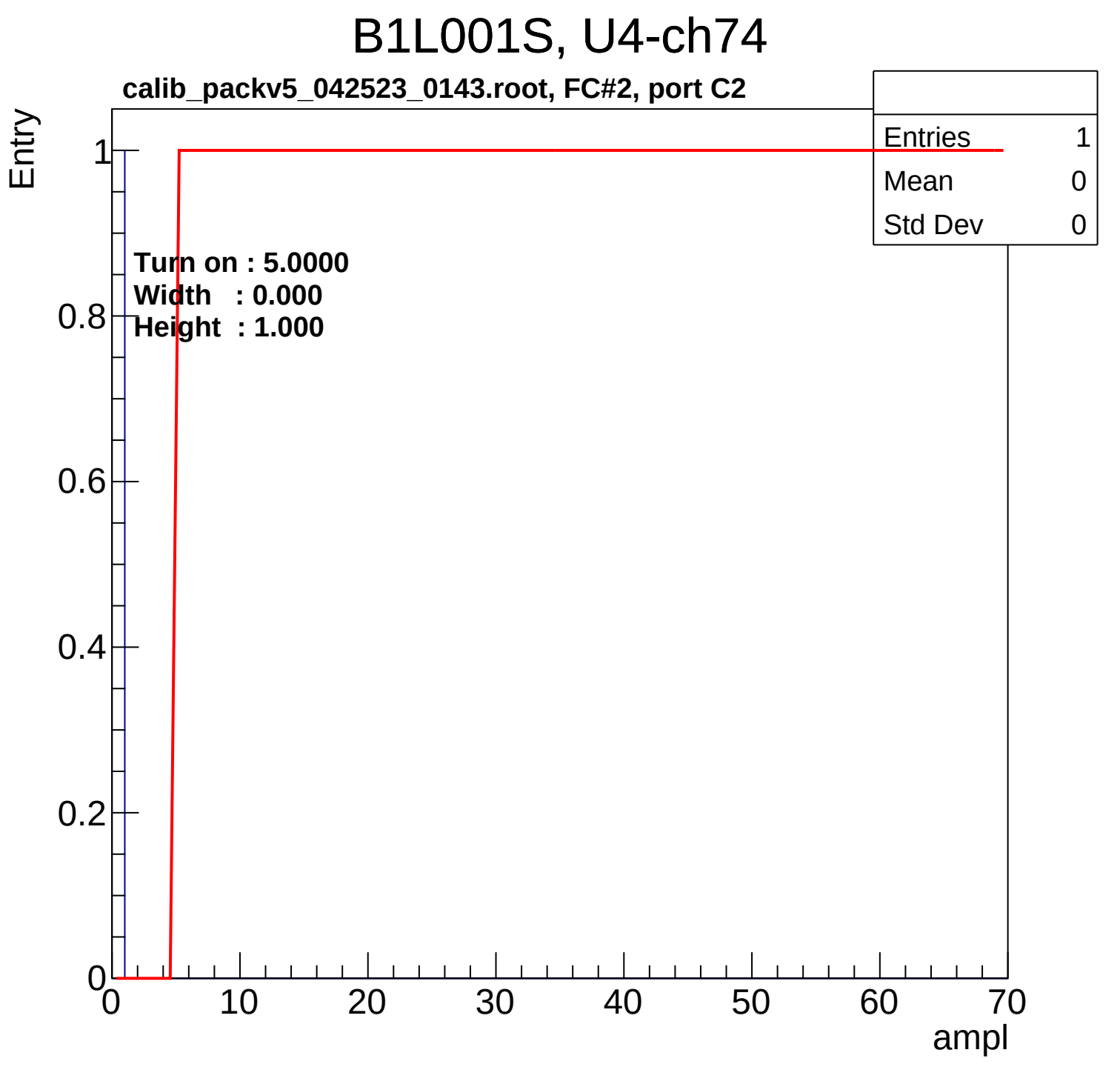
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L001S, U4-ch74
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
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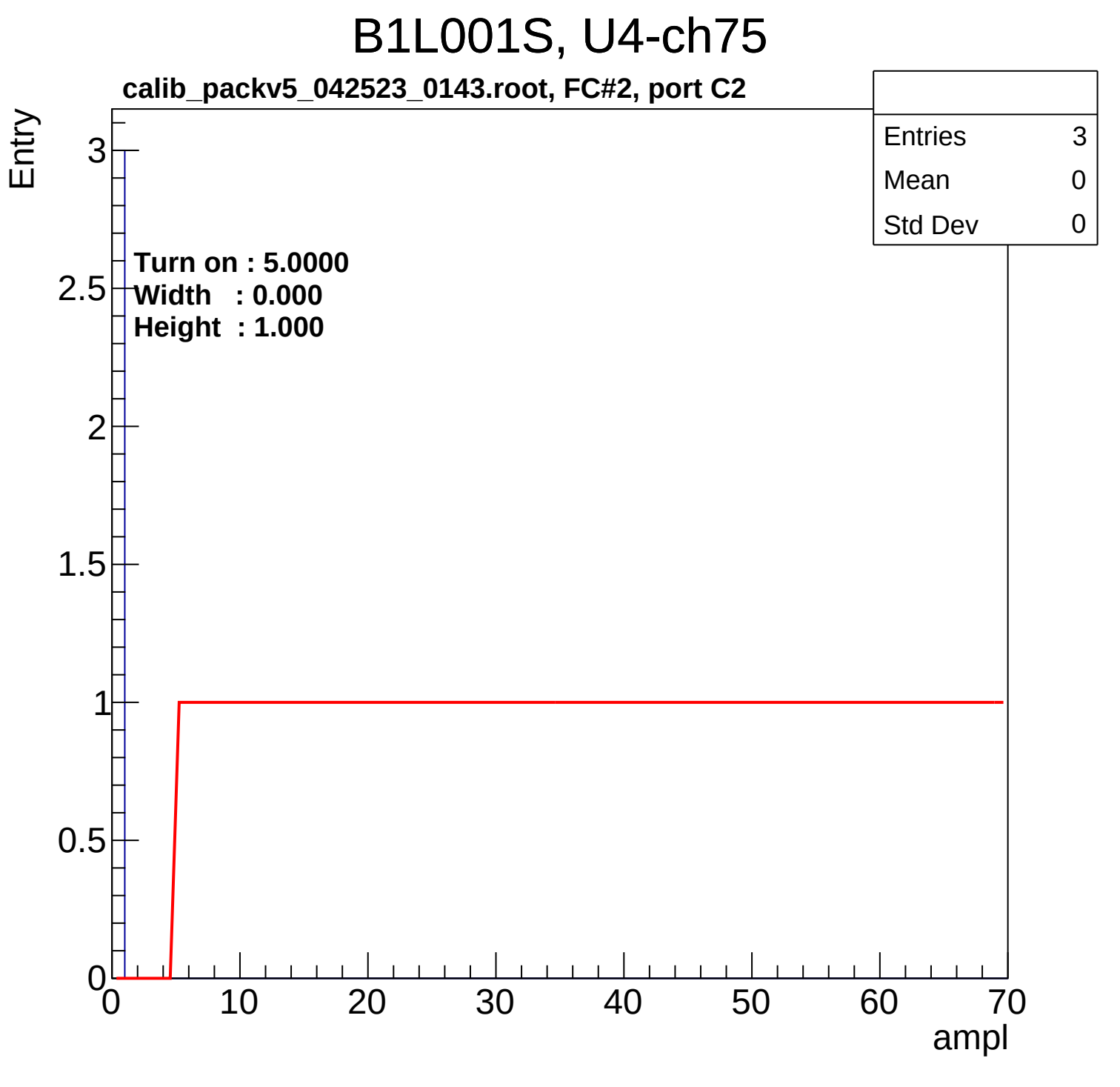
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L001S, U4-ch75
calib_packv5_042523_0143.root, FC#2, port C2
Entries 3
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
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20
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40
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60
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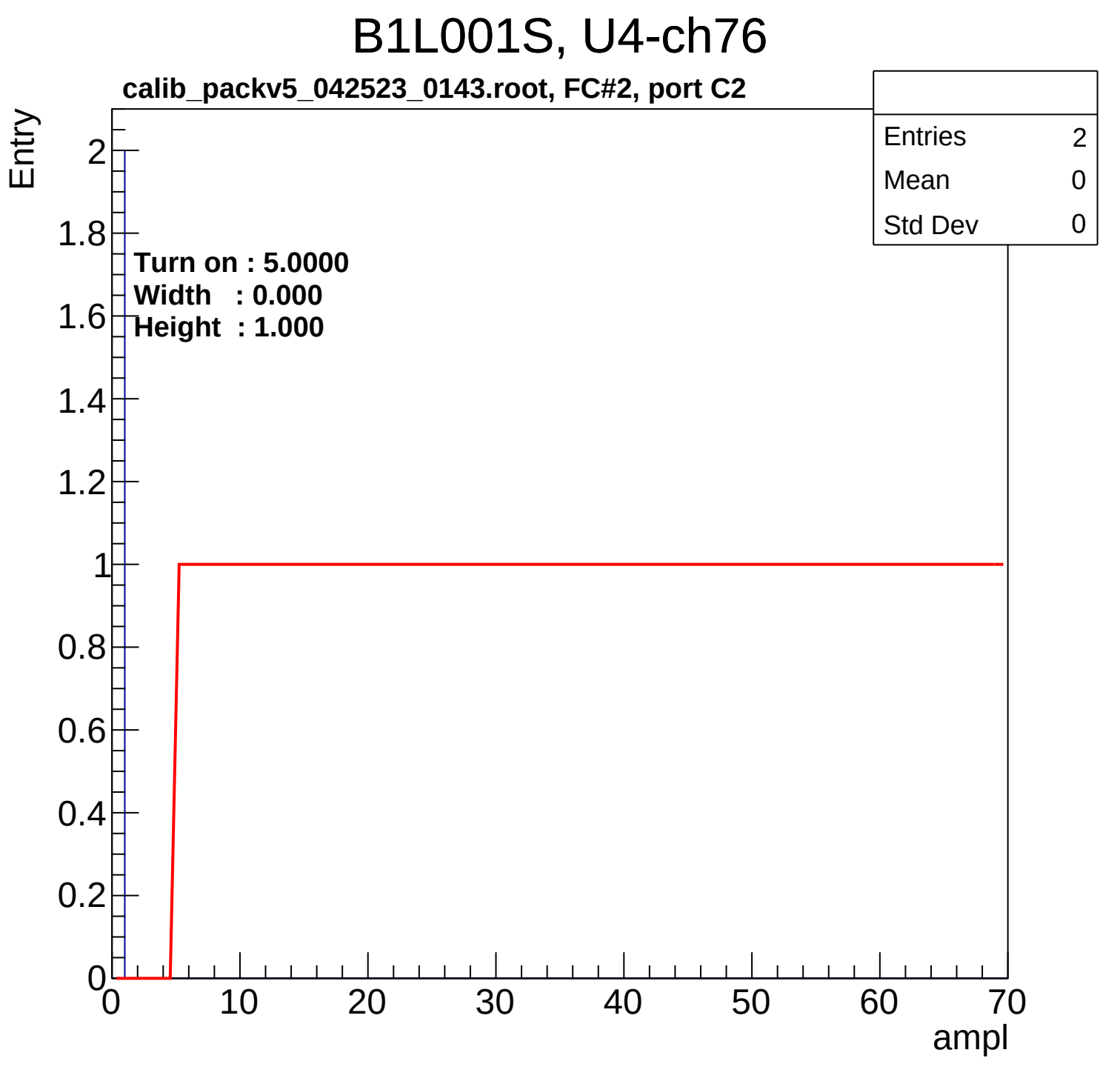
B1L001S, U4-ch76
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
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60
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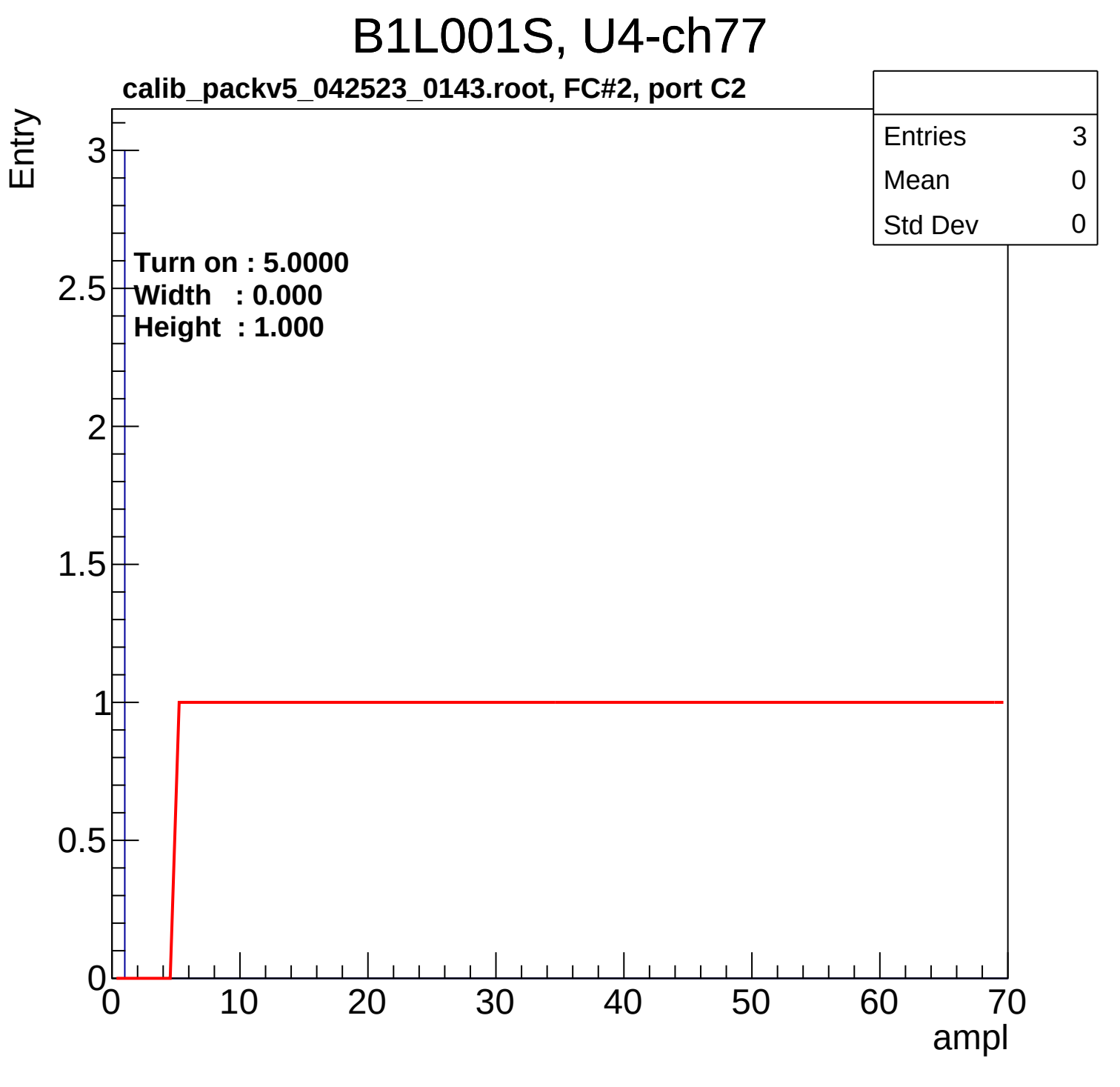
B1L001S, U4-ch77
calib_packv5_042523_0143.root, FC#2, port C2
Entries 3
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
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1
1.5
2
2.5
3
0
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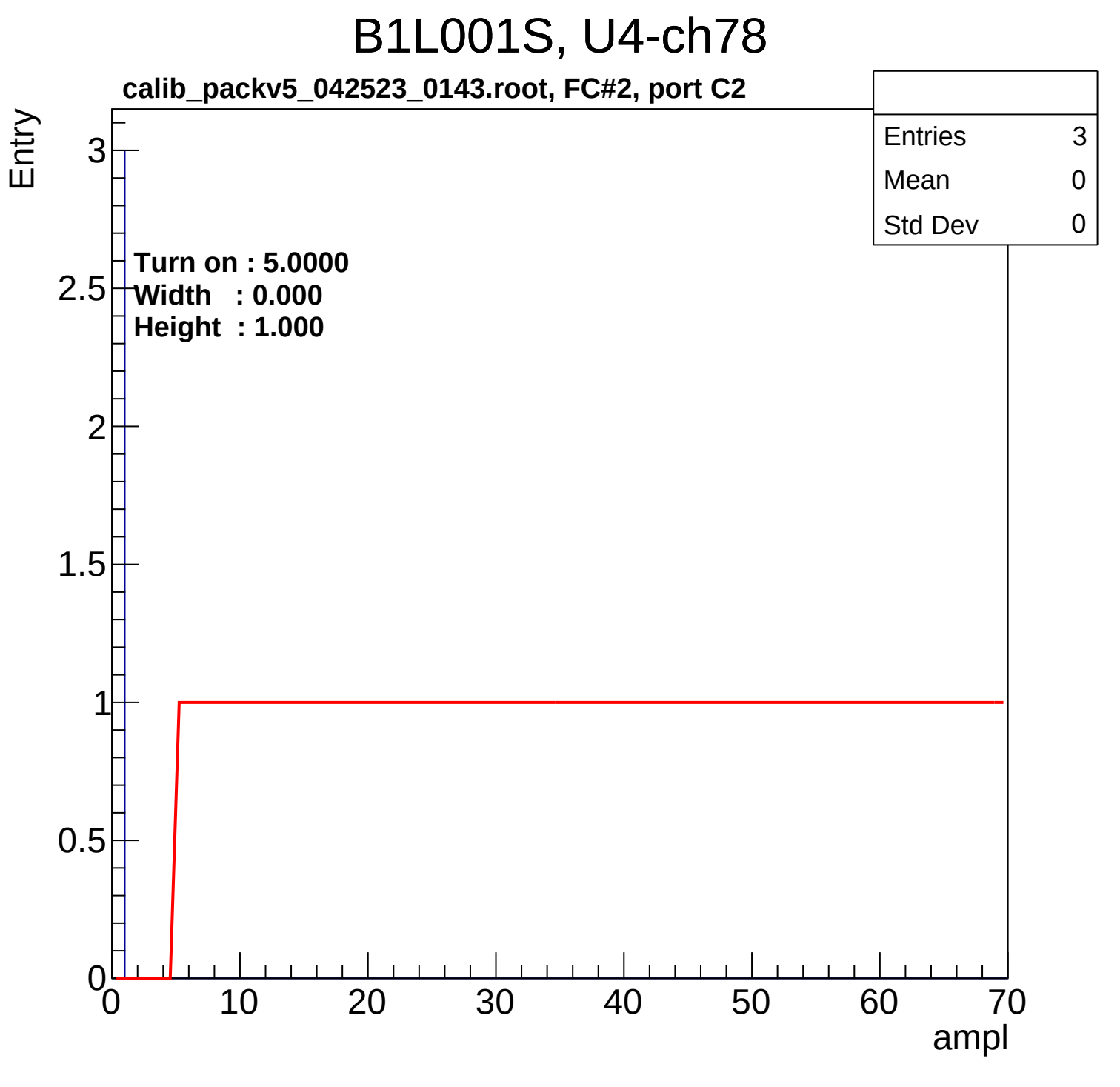
B1L001S, U4-ch78
calib_packv5_042523_0143.root, FC#2, port C2
Entries 3
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
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1
1.5
2
2.5
3
0
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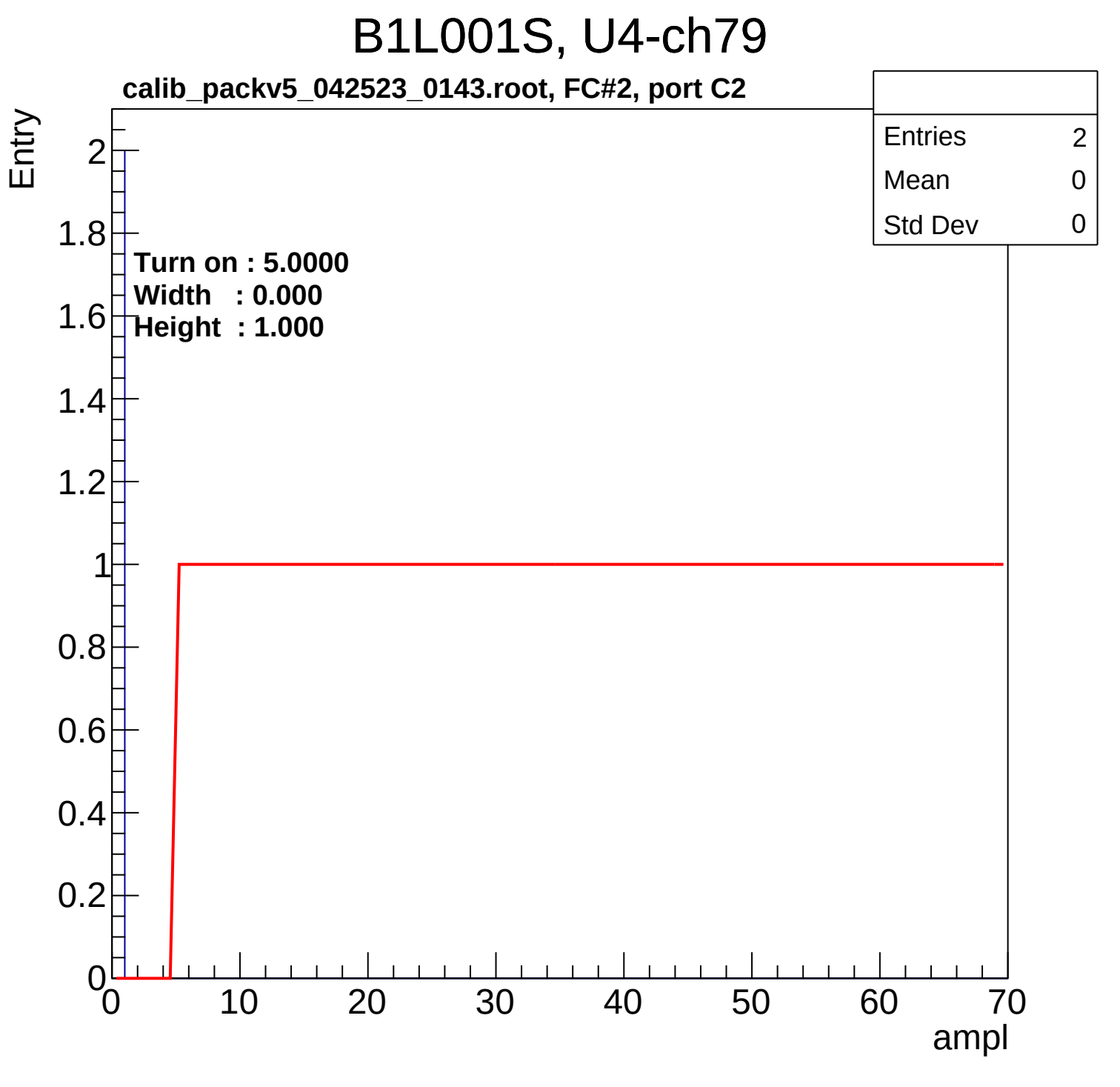
B1L001S, U4-ch79
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
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1.2
1.4
1.6
1.8
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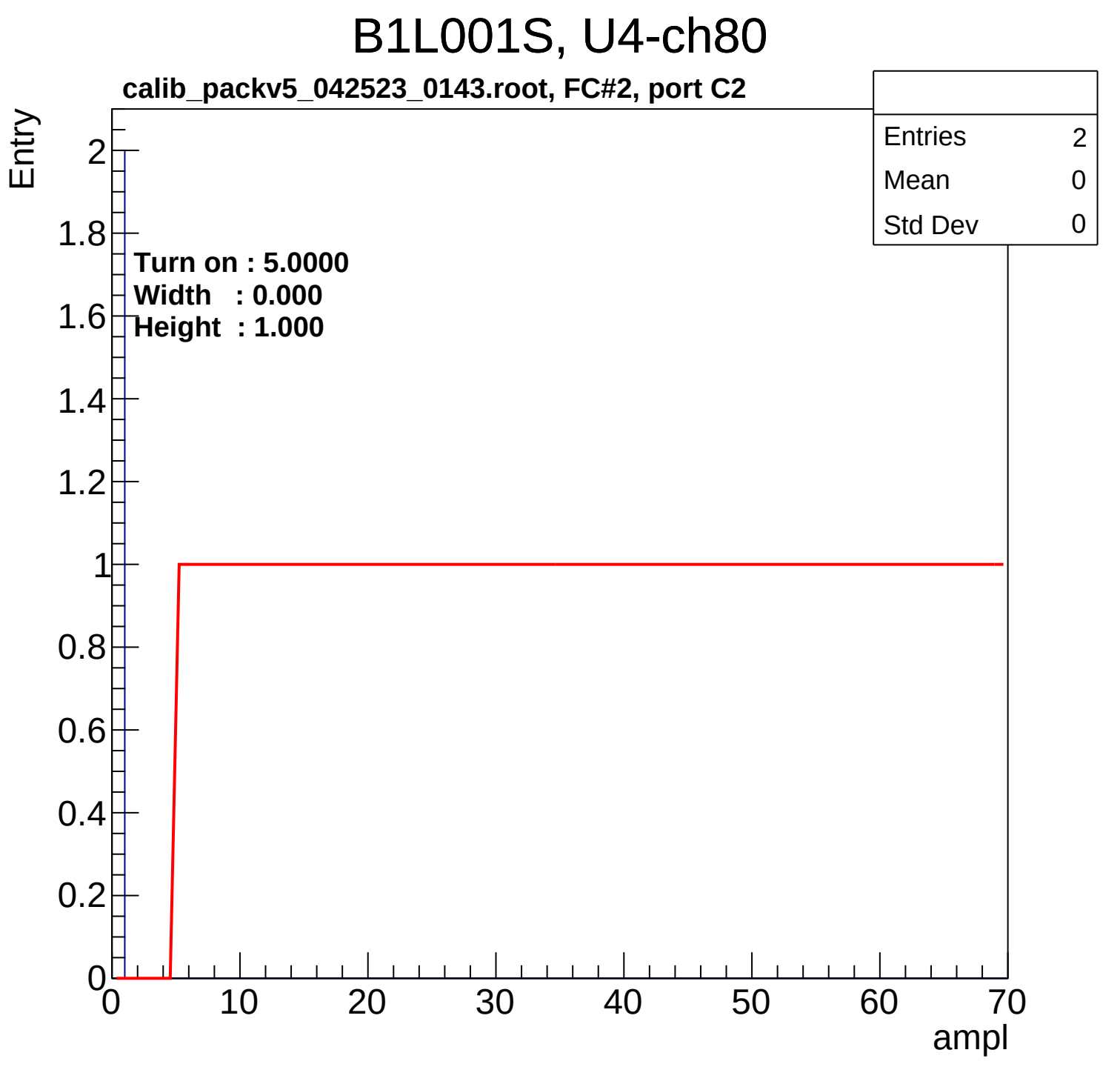
B1L001S, U4-ch80
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
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0.2
0.4
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1.2
1.4
1.6
1.8
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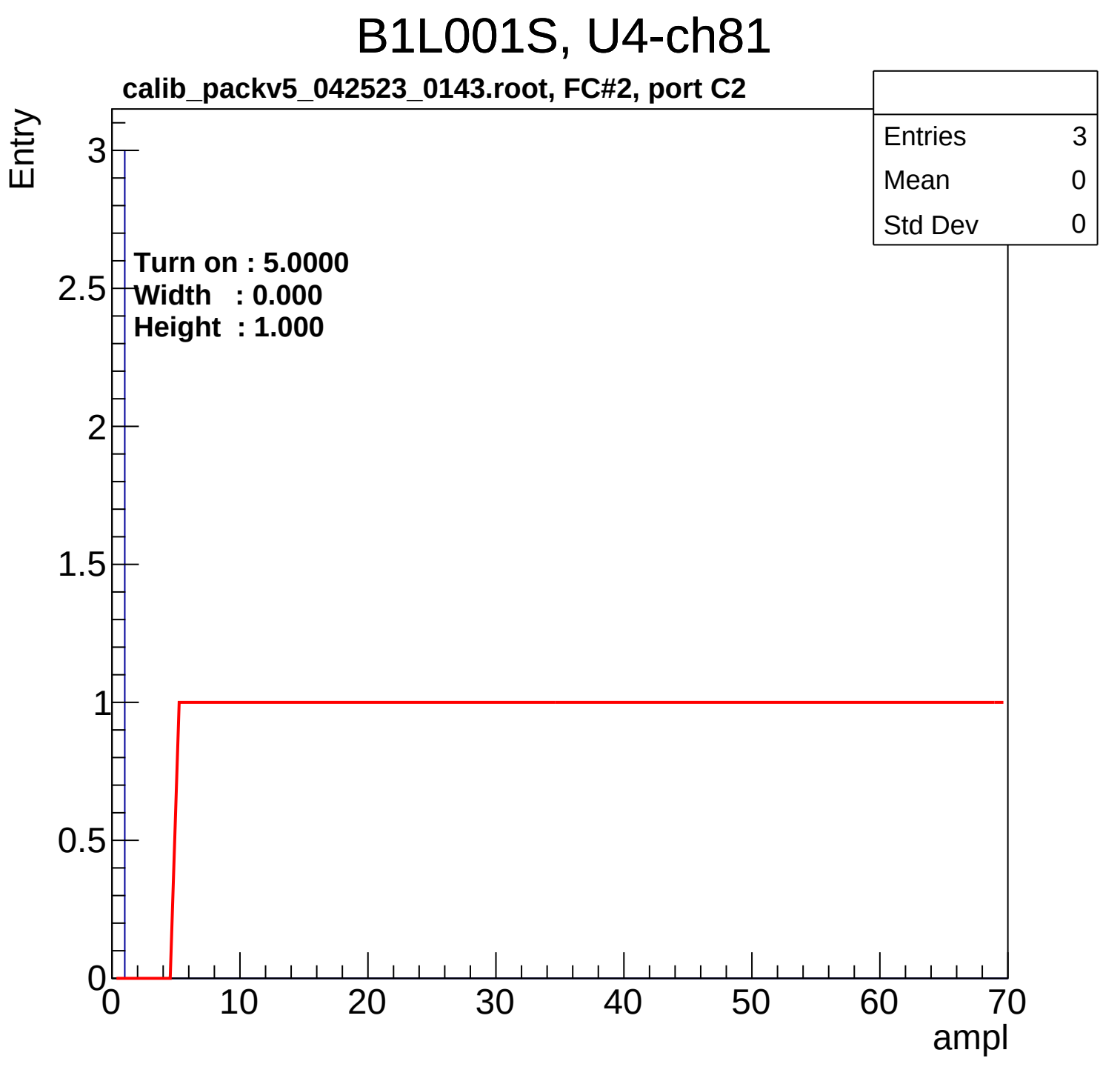
B1L001S, U4-ch81
calib_packv5_042523_0143.root, FC#2, port C2
Entries 3
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
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20
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60
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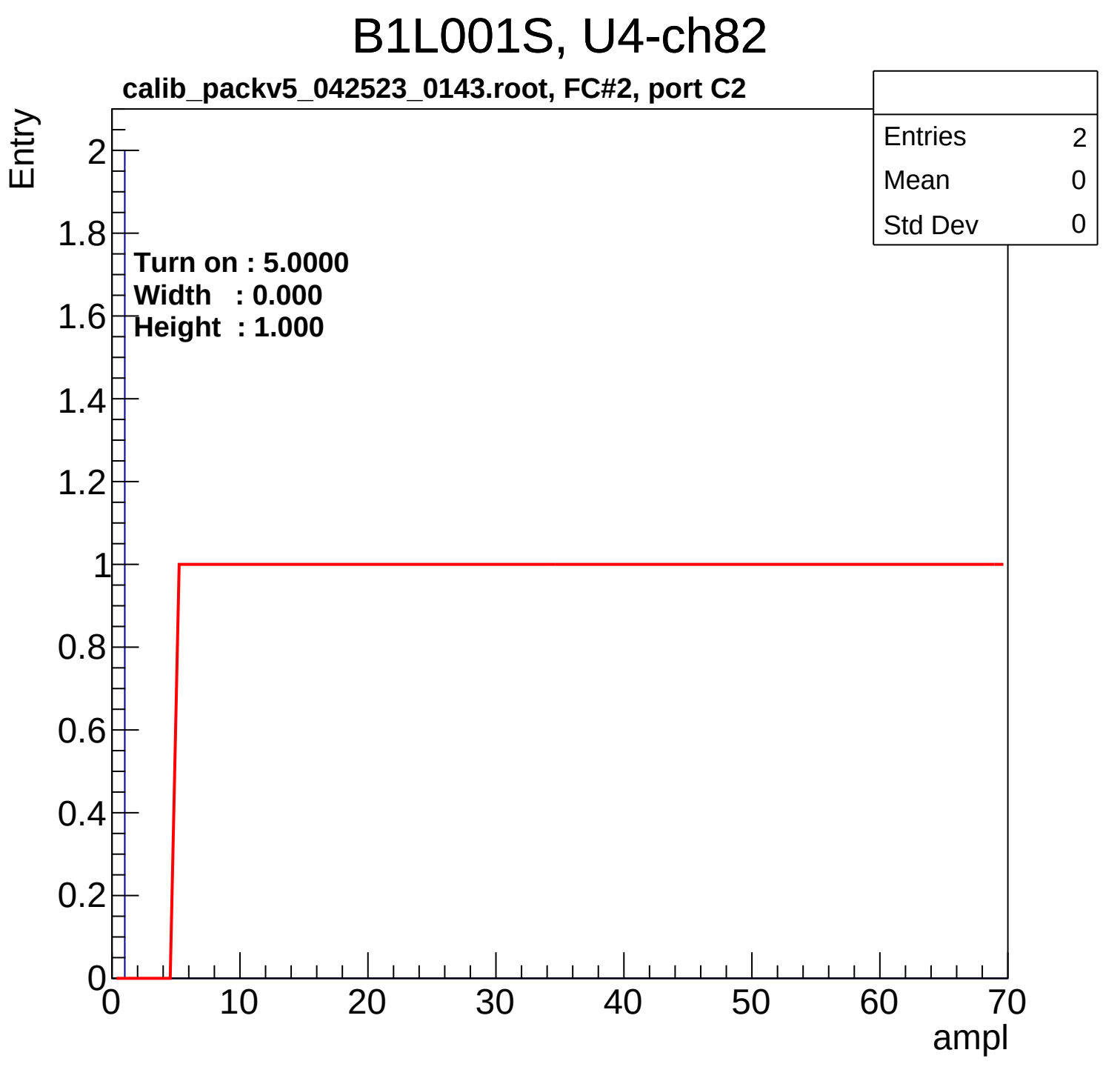
B1L001S, U4-ch82
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
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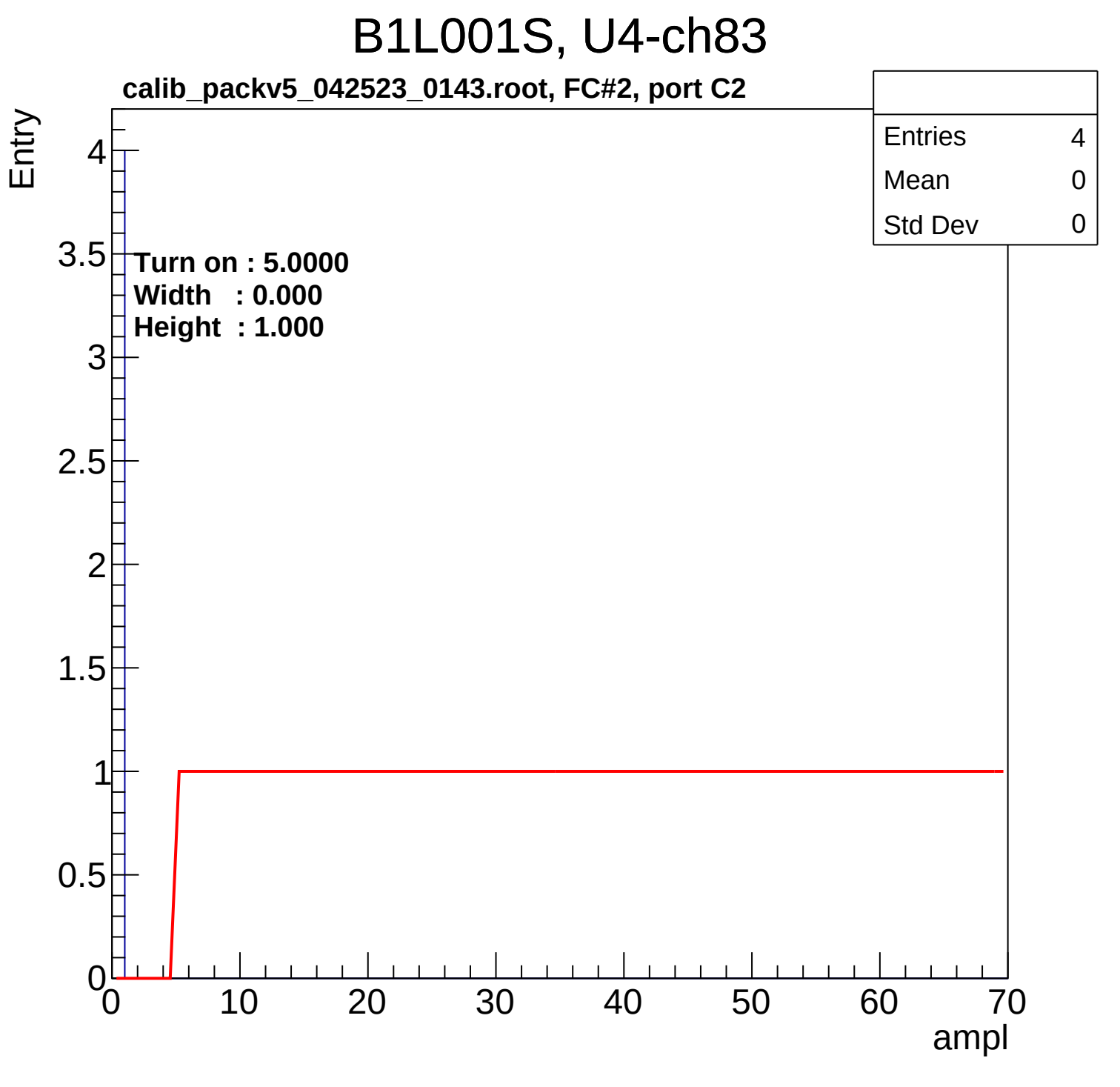
B1L001S, U4-ch83
calib_packv5_042523_0143.root, FC#2, port C2
Entries 4
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
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1.5
2
2.5
3
3.5
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40
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60
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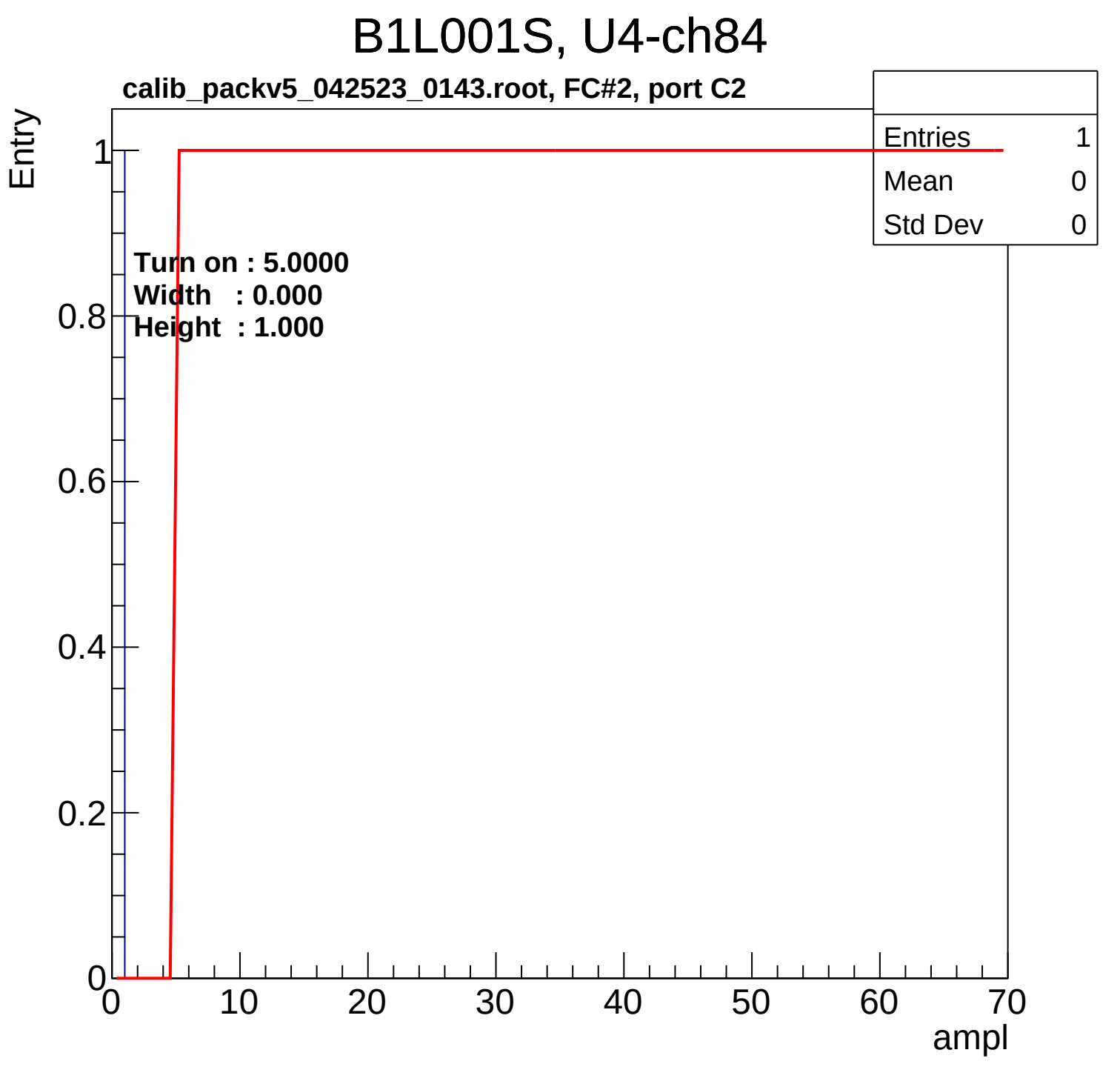
B1L001S, U4-ch84
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
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0.6
0.4
0.2
0
0
10
20
30
40
50
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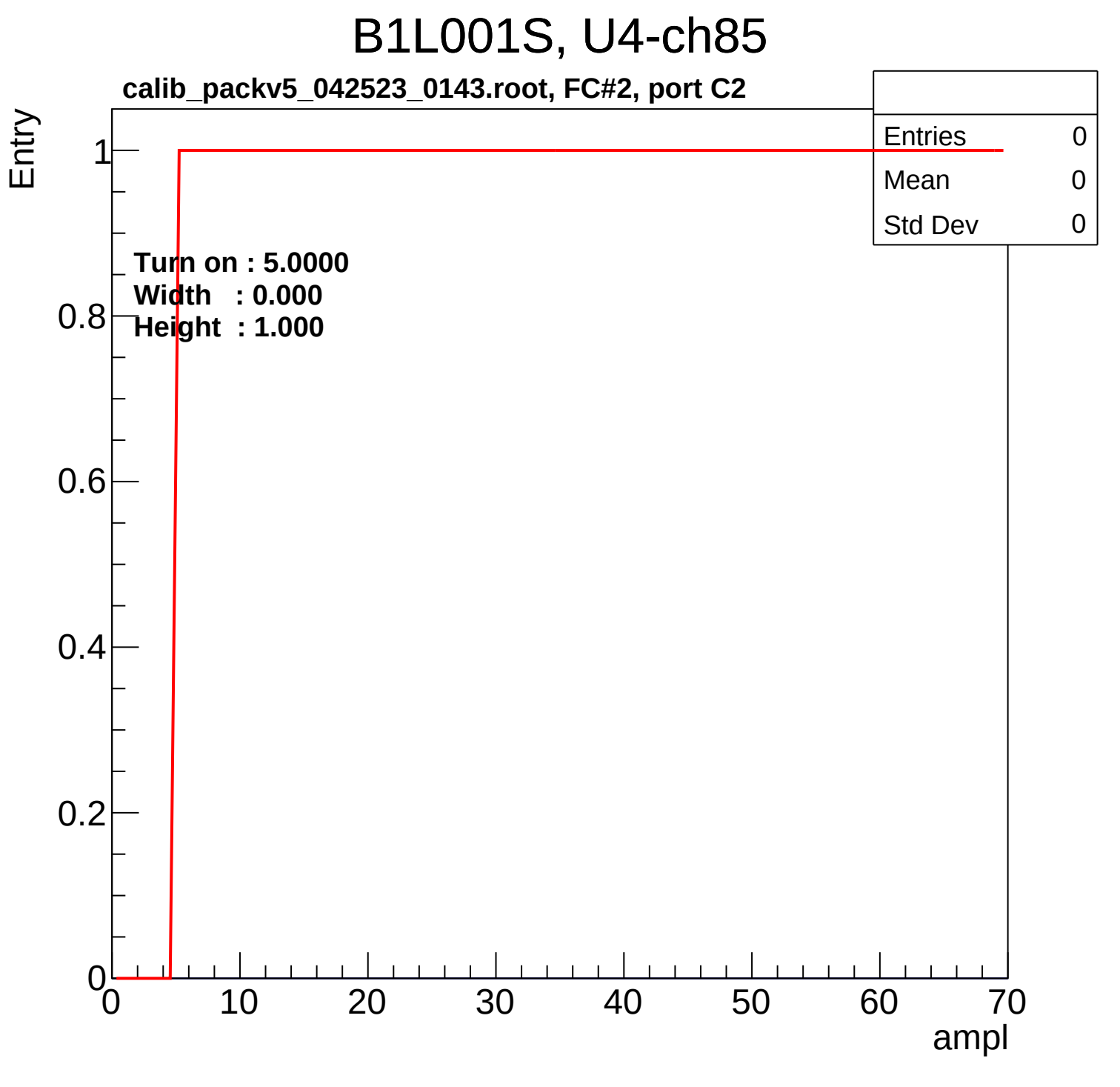
70
ampl


B1L001S, U4-ch85
calib_packv5_042523_0143.root, FC#2, port C2
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
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0.6
0.4
0.2
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20
30
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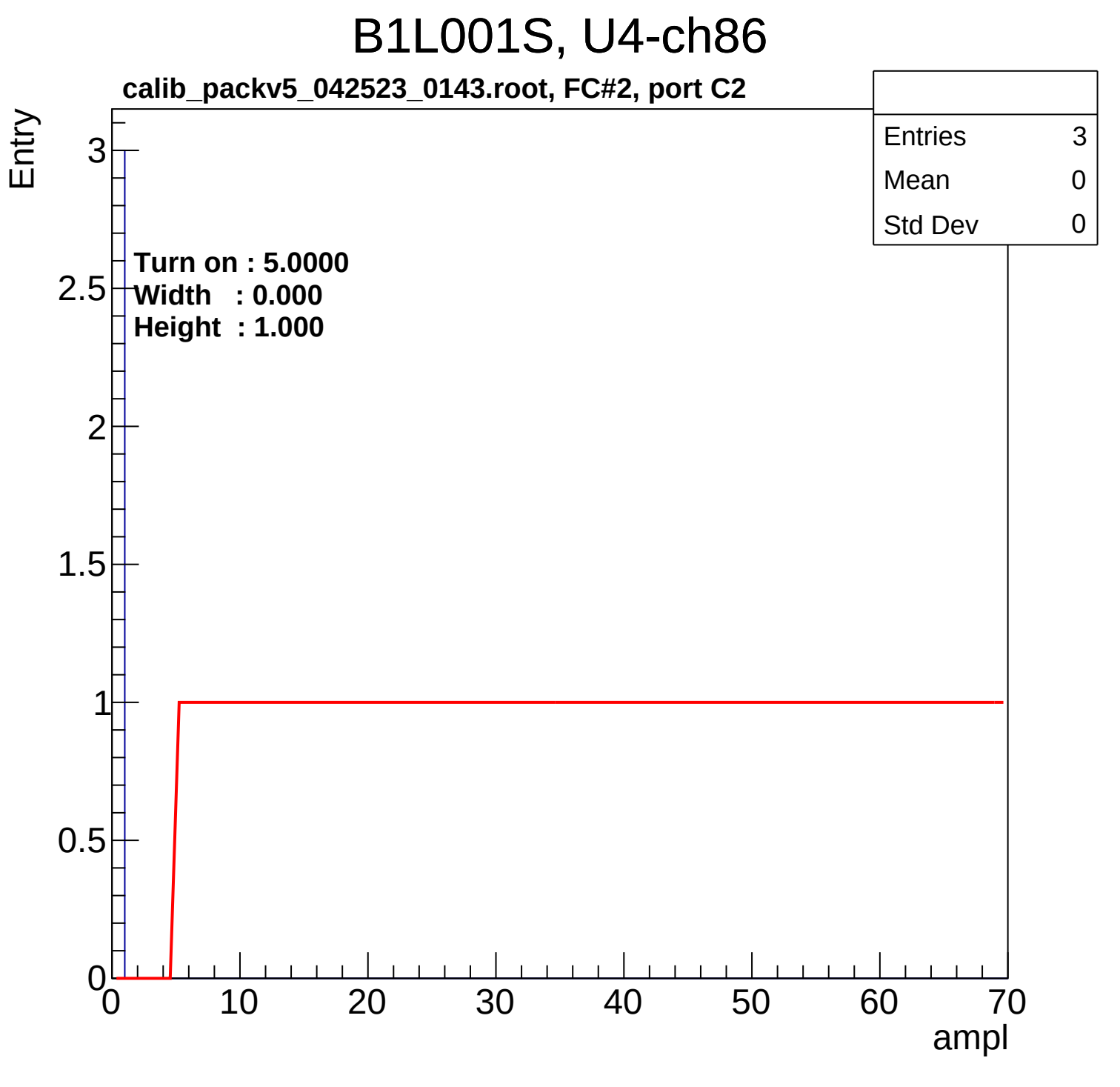
50
60
70
ampl


B1L001S, U4-ch86
calib_packv5_042523_0143.root, FC#2, port C2
Entries 3
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
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1
1.5
2
2.5
3
0
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20
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60
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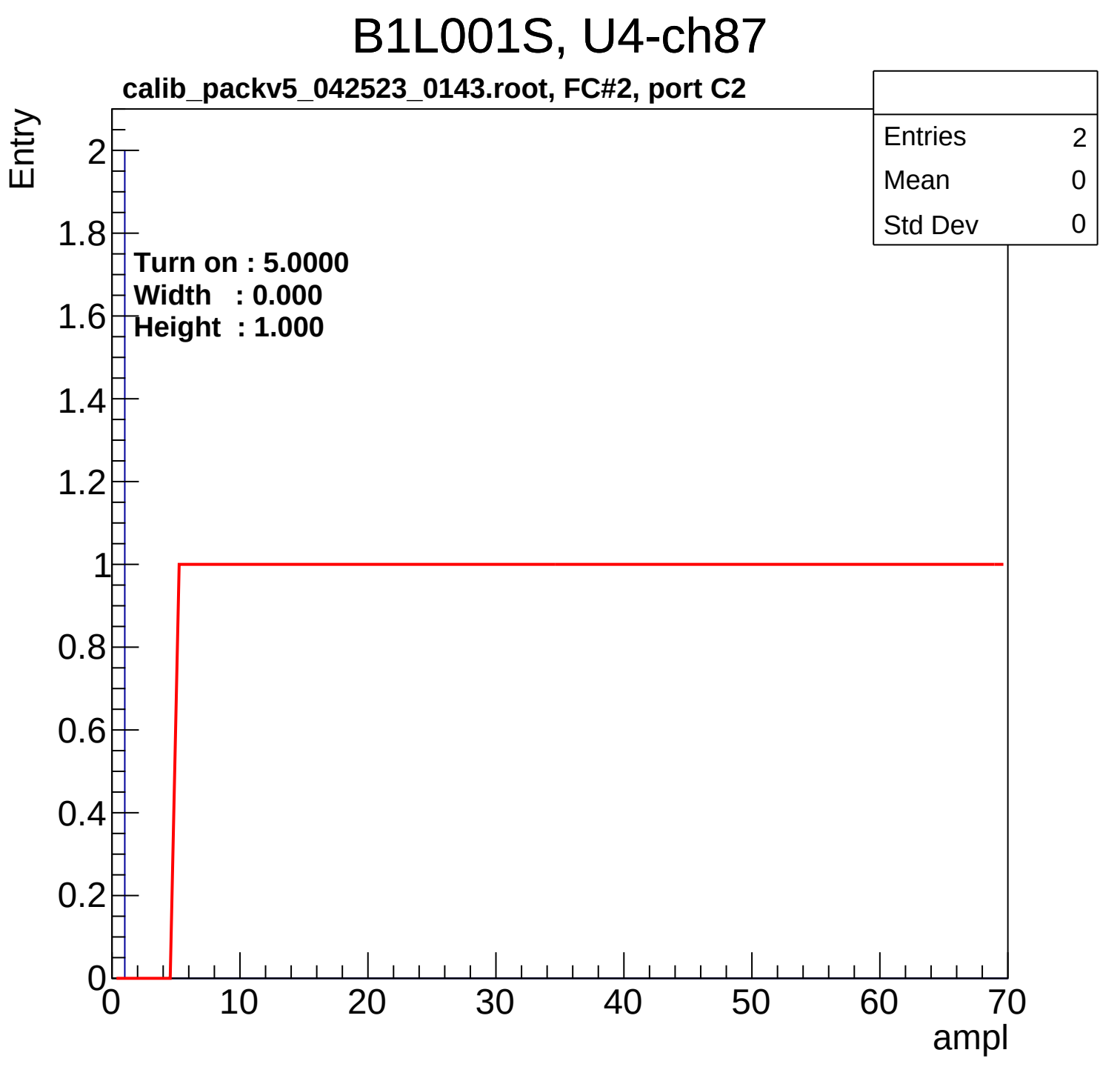
B1L001S, U4-ch87
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
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0.4
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1.2
1.4
1.6
1.8
2
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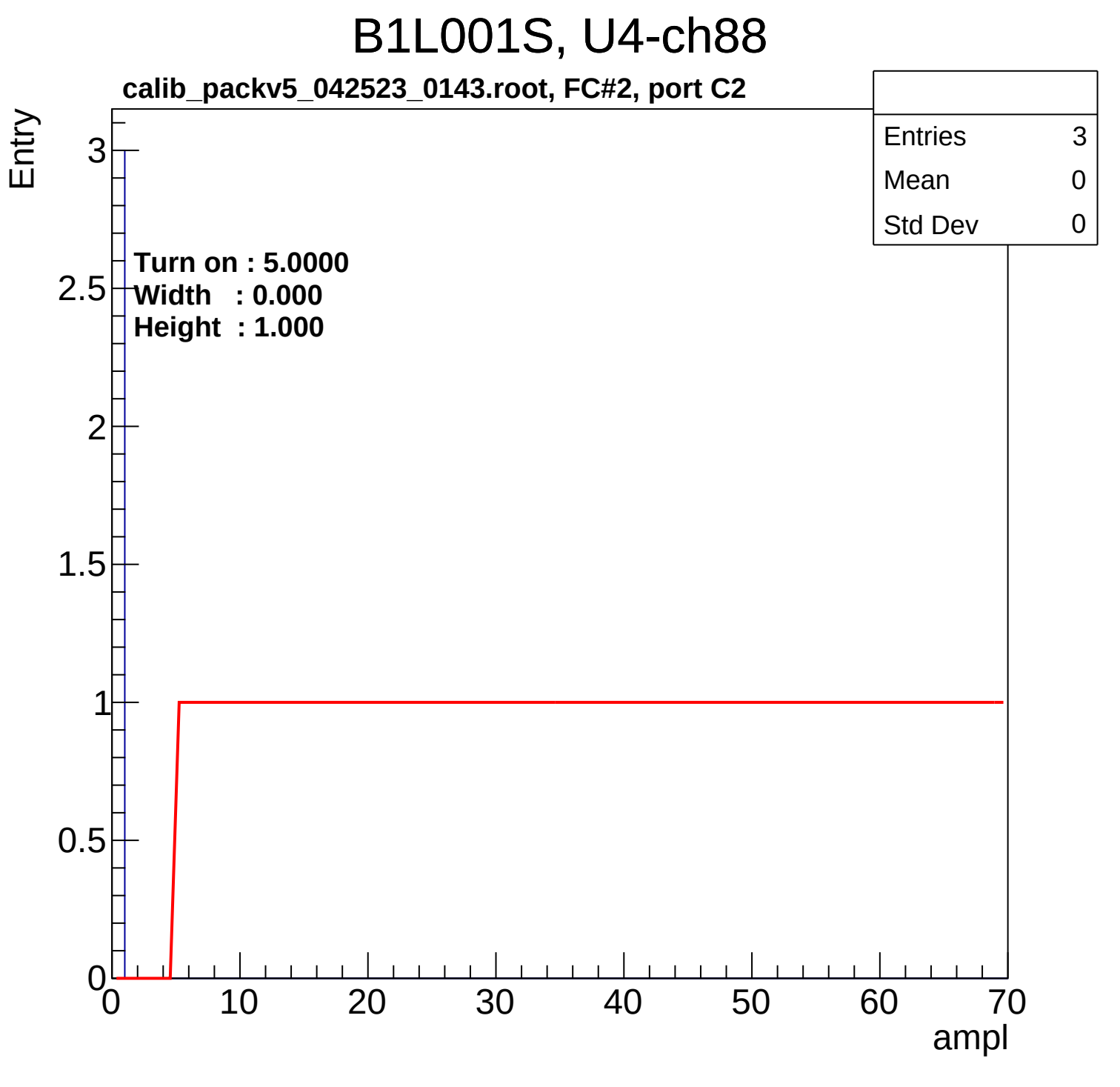
B1L001S, U4-ch88
calib_packv5_042523_0143.root, FC#2, port C2
Entries 3
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
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1
1.5
2
2.5
3
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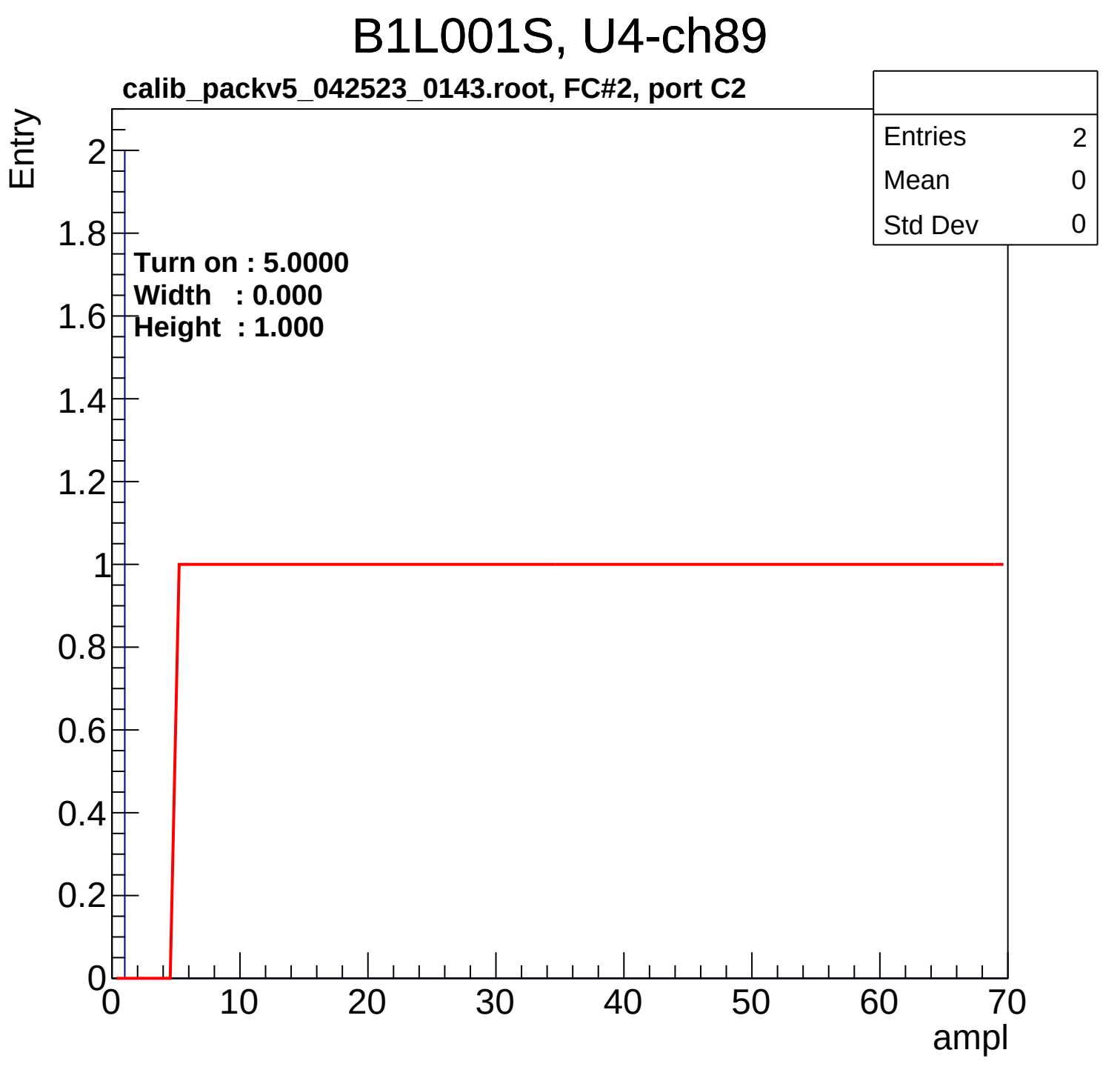
B1L001S, U4-ch89
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
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0.2
0.4
0.6
0.8
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1.2
1.4
1.6
1.8
2
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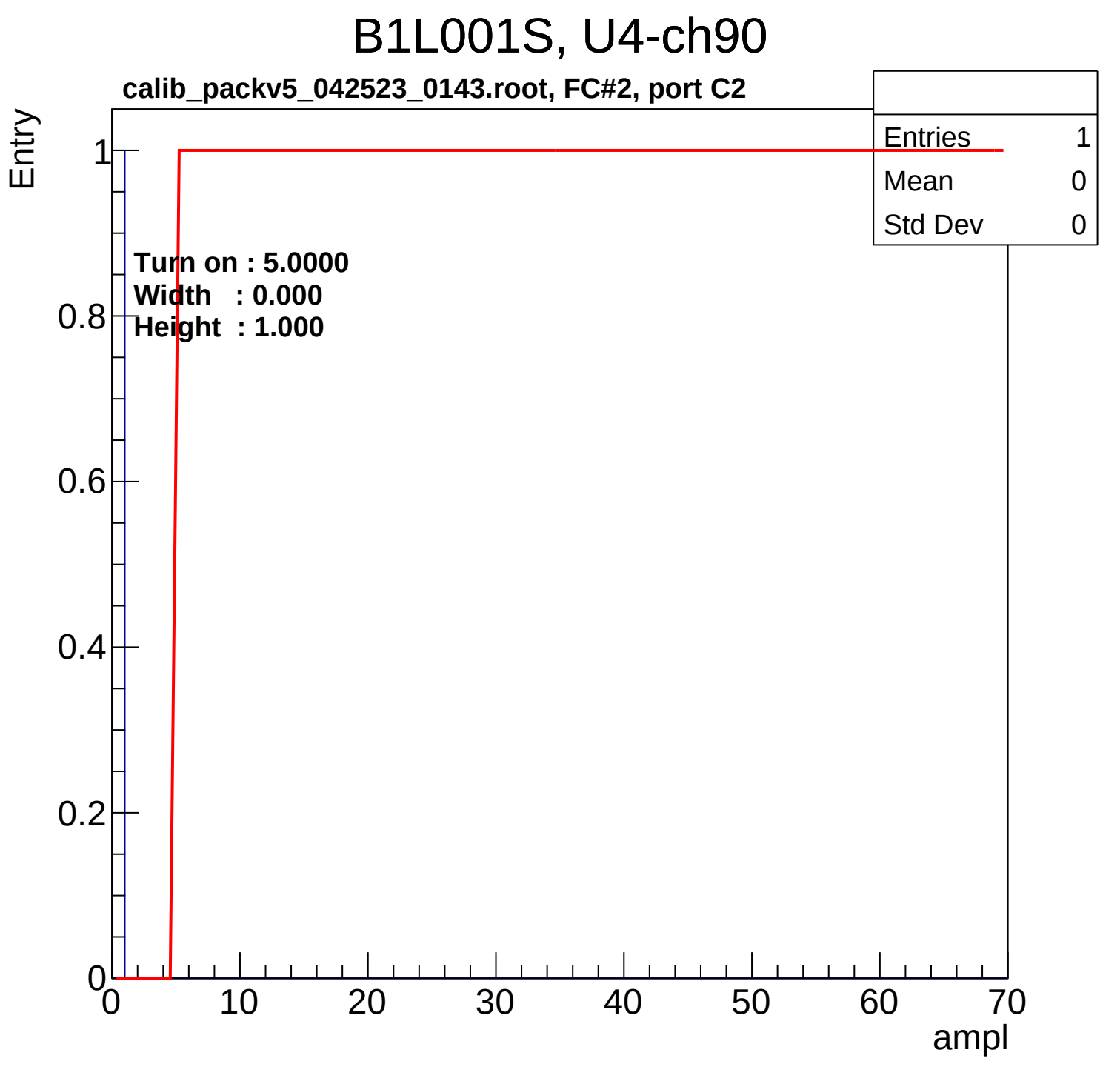
B1L001S, U4-ch90
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
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0.8
0.6
0.4
0.2
0
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10
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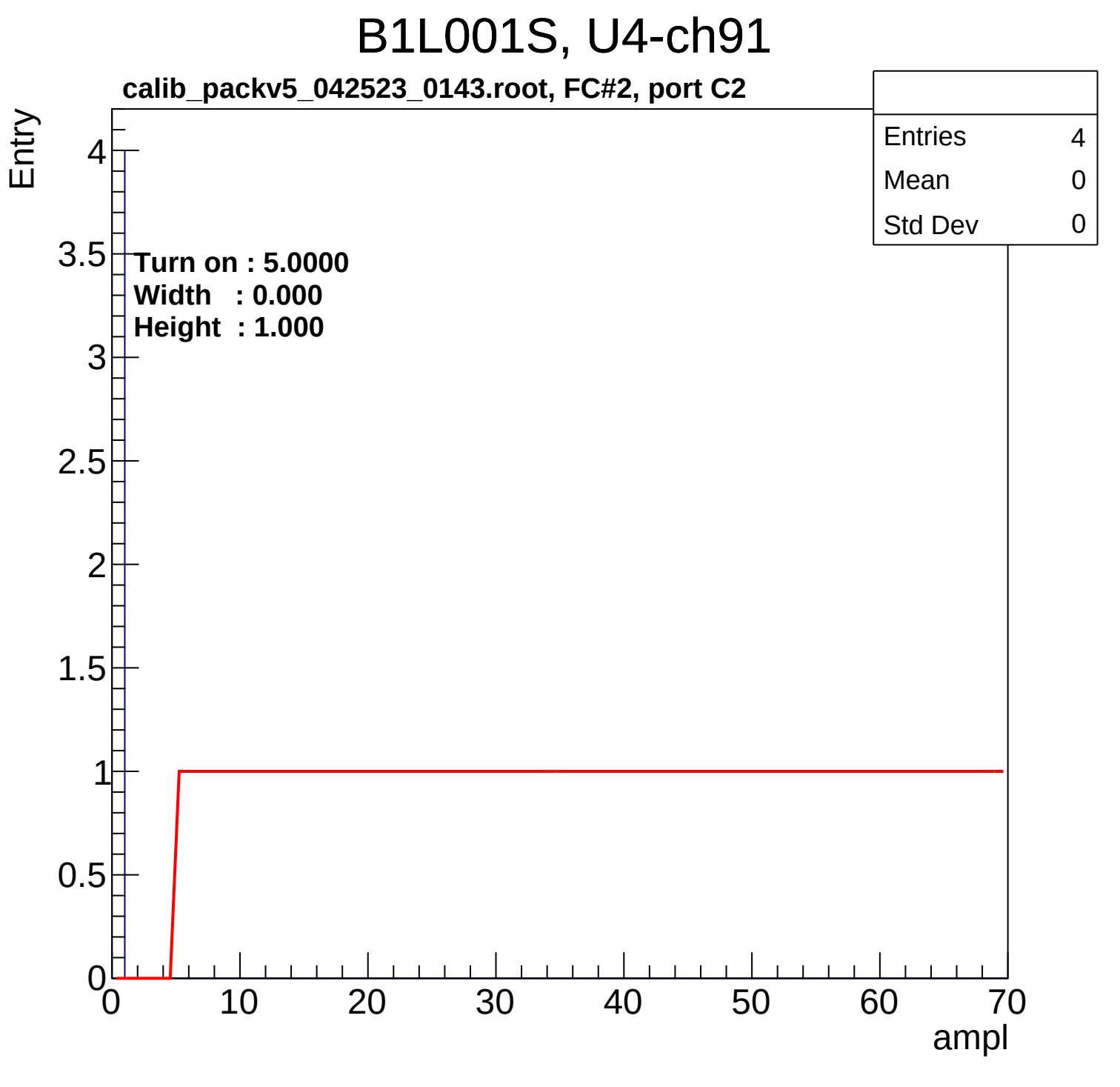
ampl


B1L001S, U4-ch91
calib_packv5_042523_0143.root, FC#2, port C2
Entries 4
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
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0.5
1
1.5
2
2.5
3
3.5
4
0
10
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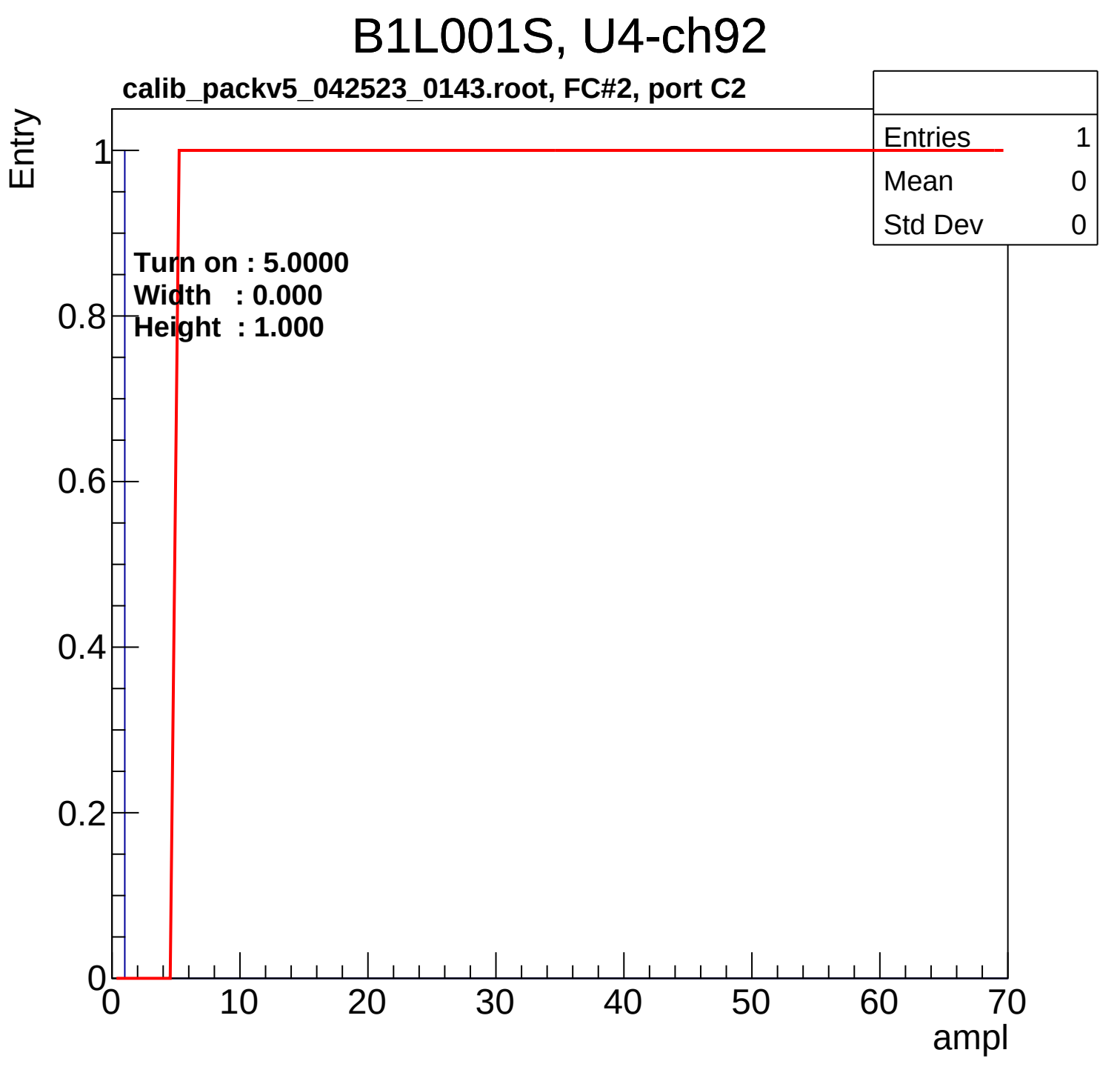
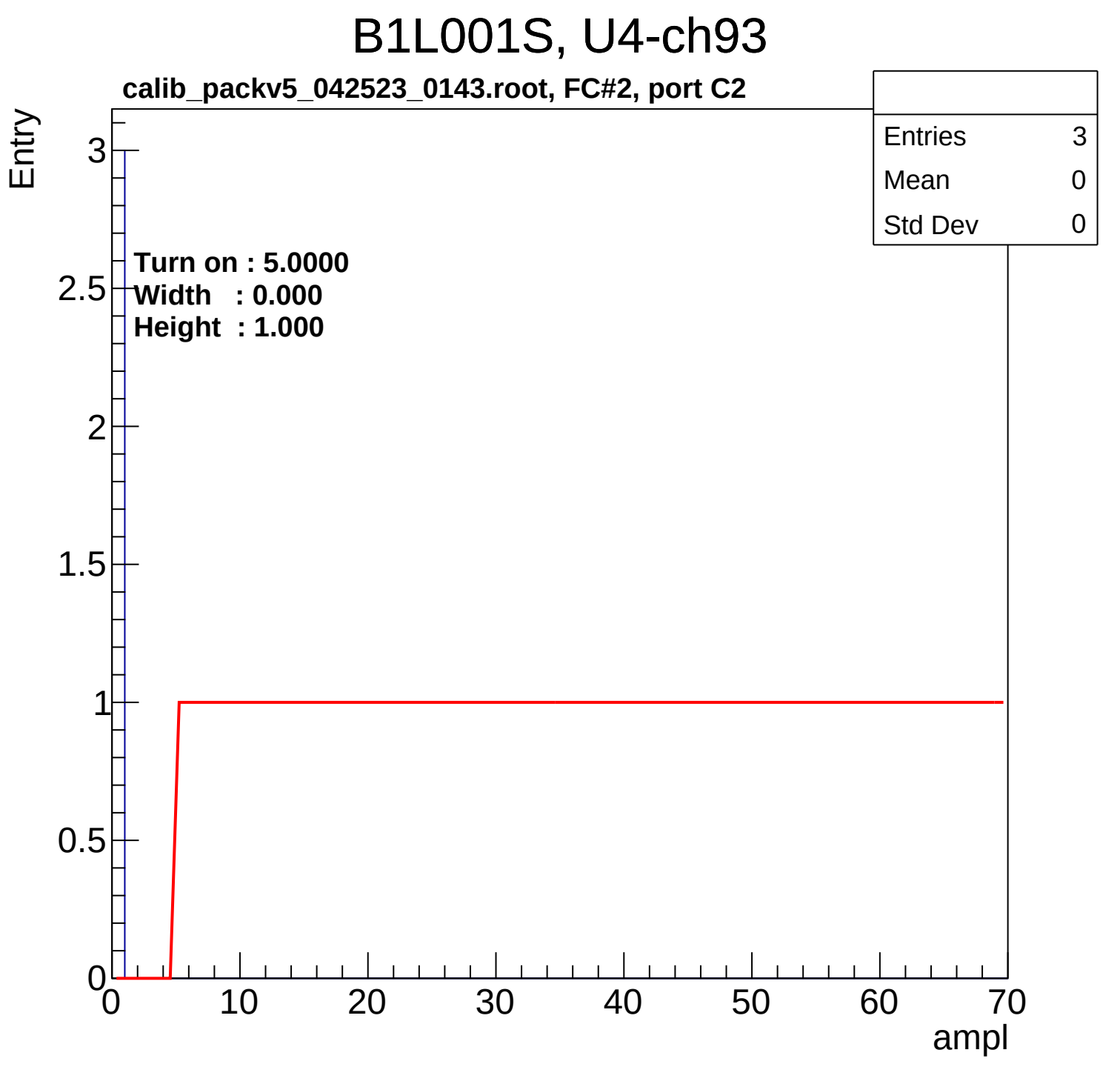
40
50
60
70


B1L001S, U4-ch92
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70


B1L001S, U4-ch93
calib_packv5_042523_0143.root, FC#2, port C2
Entries 3
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
10
20
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40
50
60
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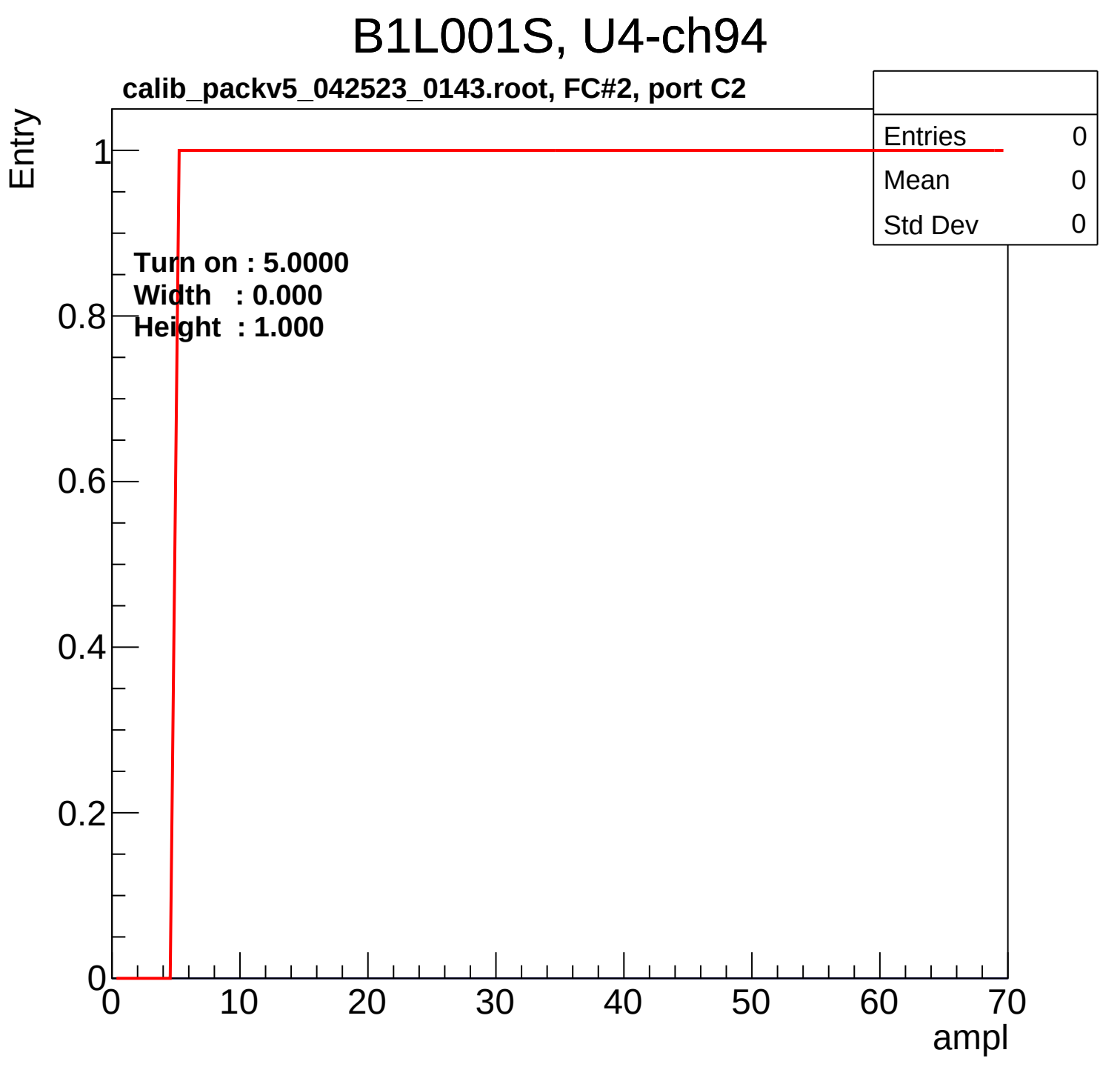
B1L001S, U4-ch94
calib_packv5_042523_0143.root, FC#2, port C2
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
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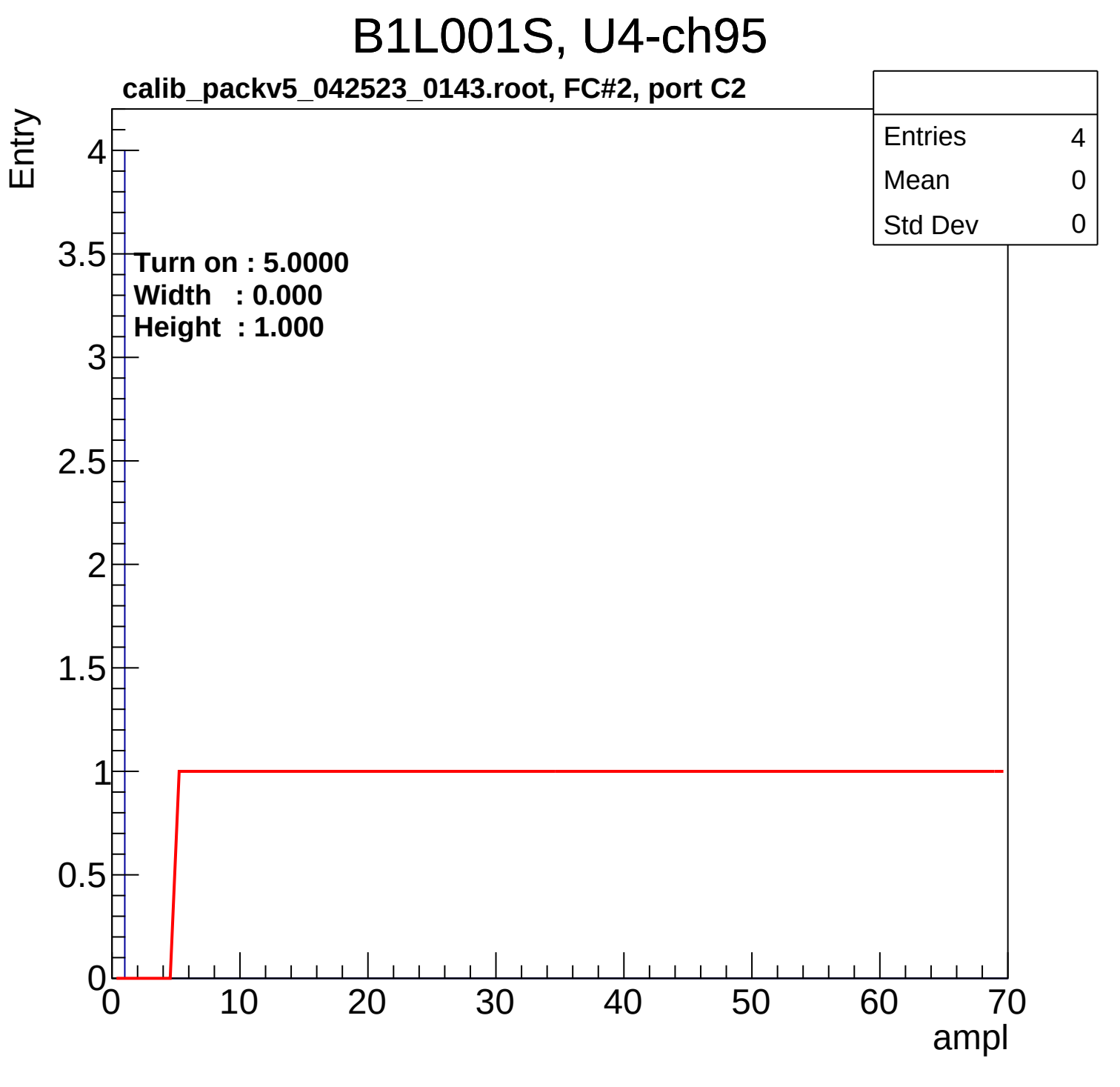
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L001S, U4-ch95
calib_packv5_042523_0143.root, FC#2, port C2
Entries 4
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
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0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
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40
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60
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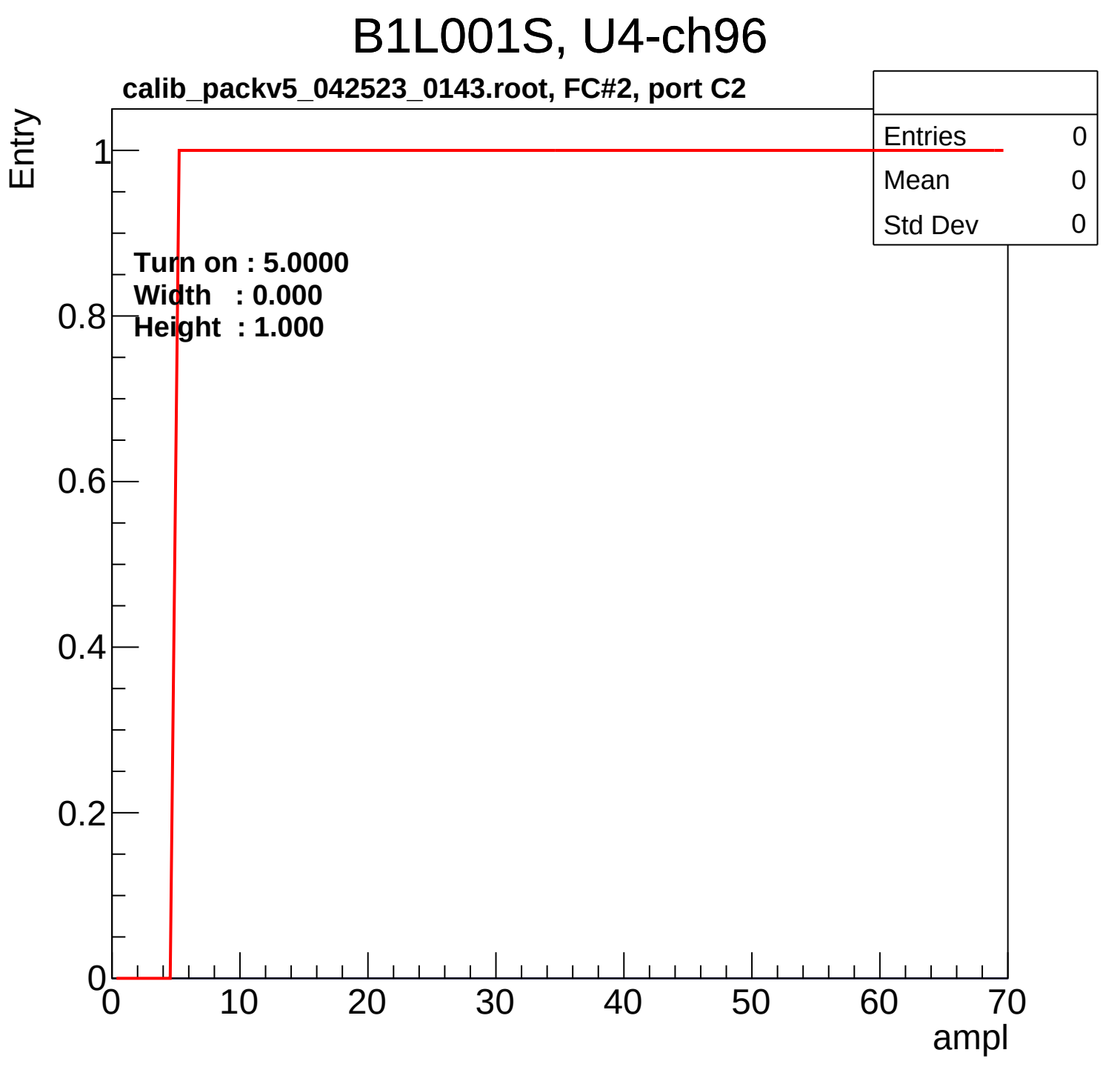
B1L001S, U4-ch96
calib_packv5_042523_0143.root, FC#2, port C2
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
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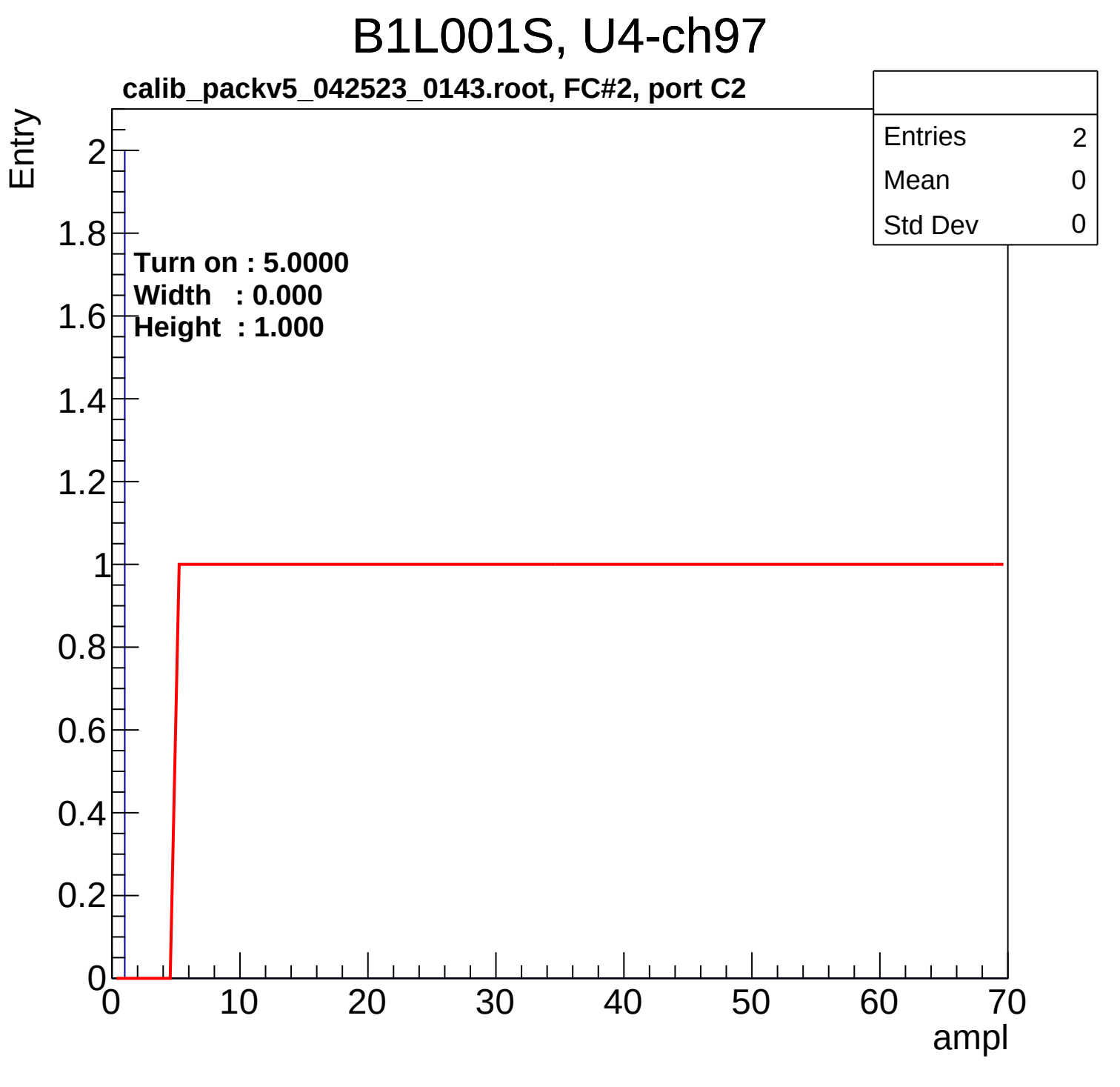
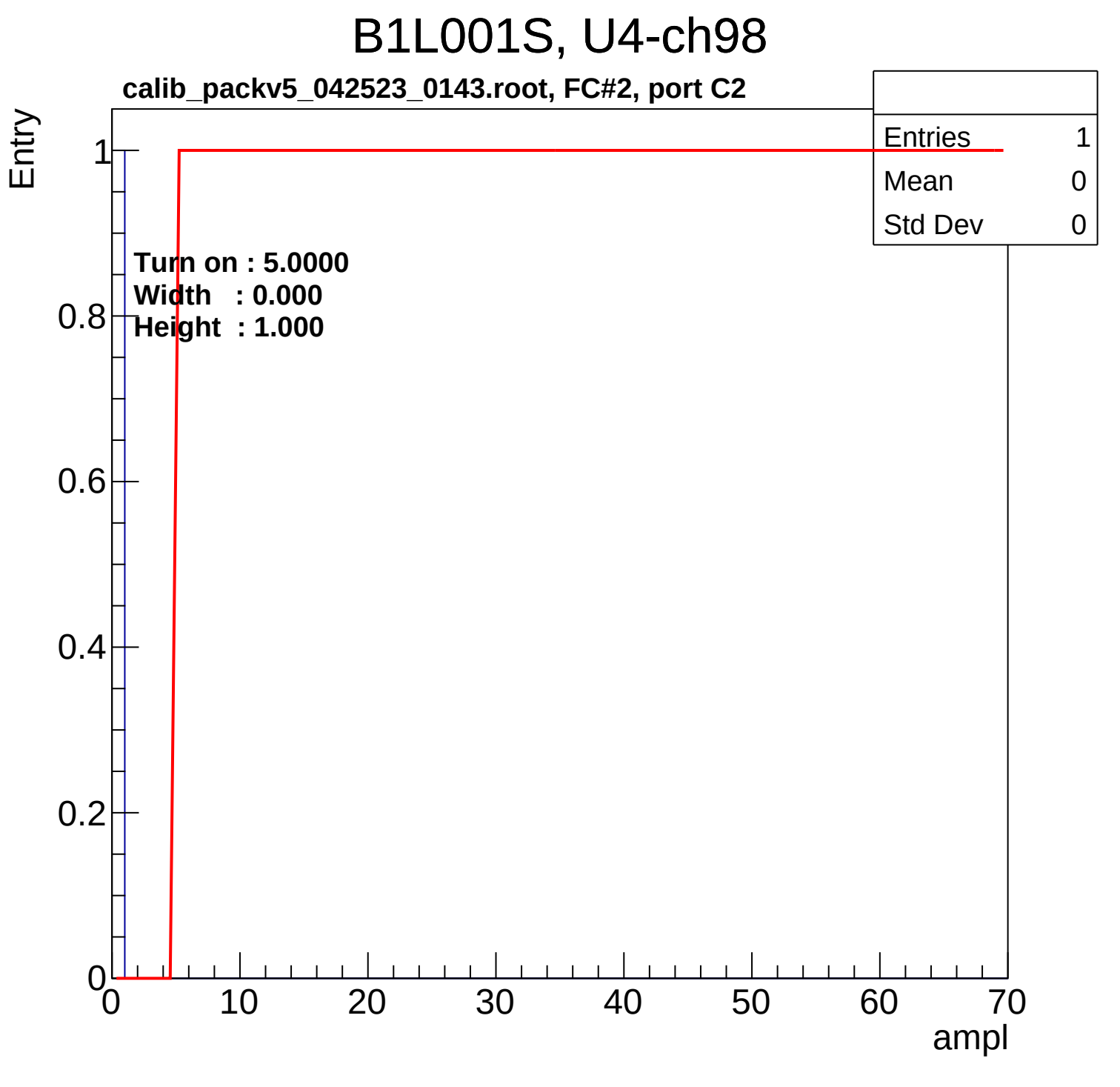
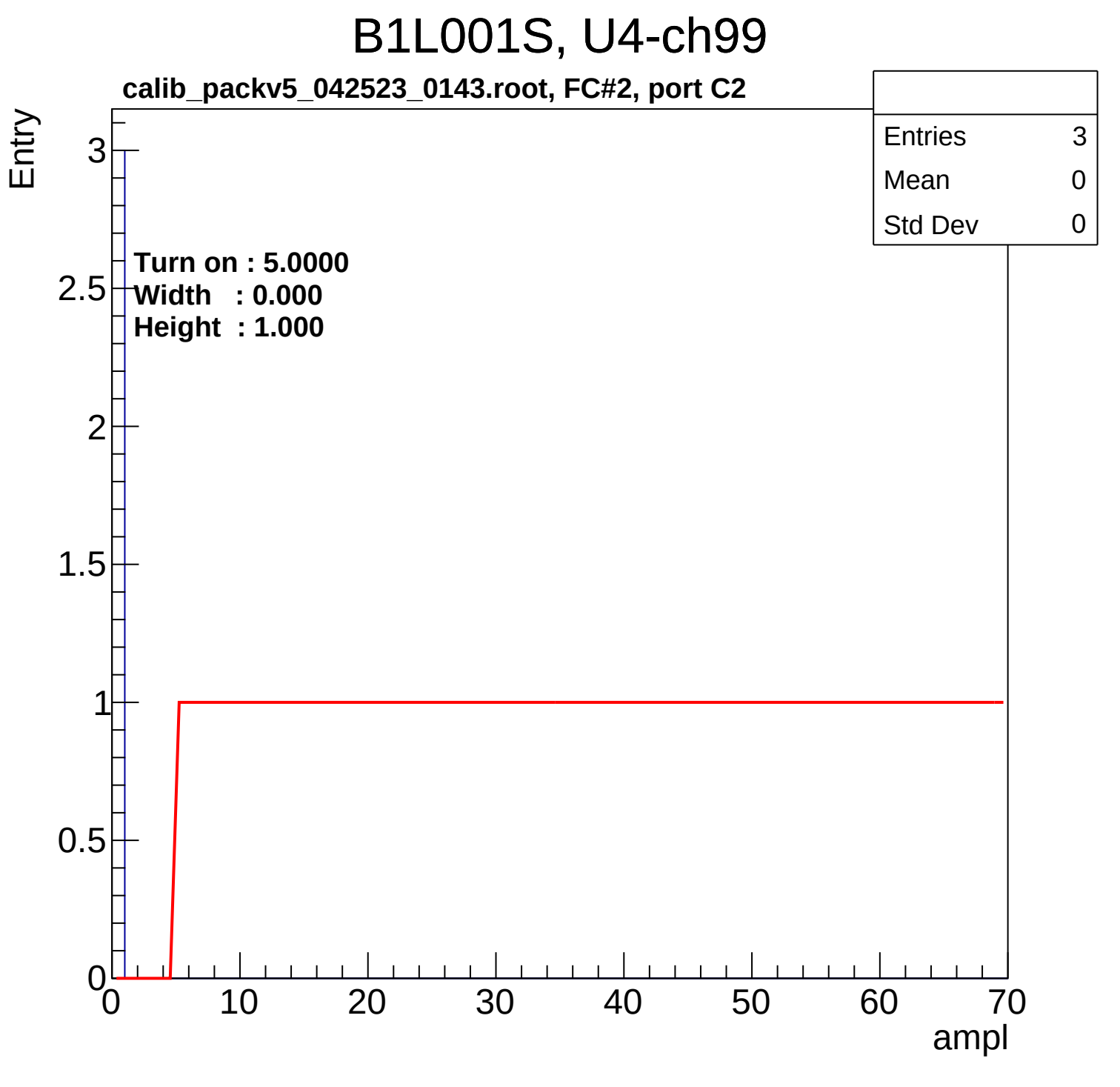
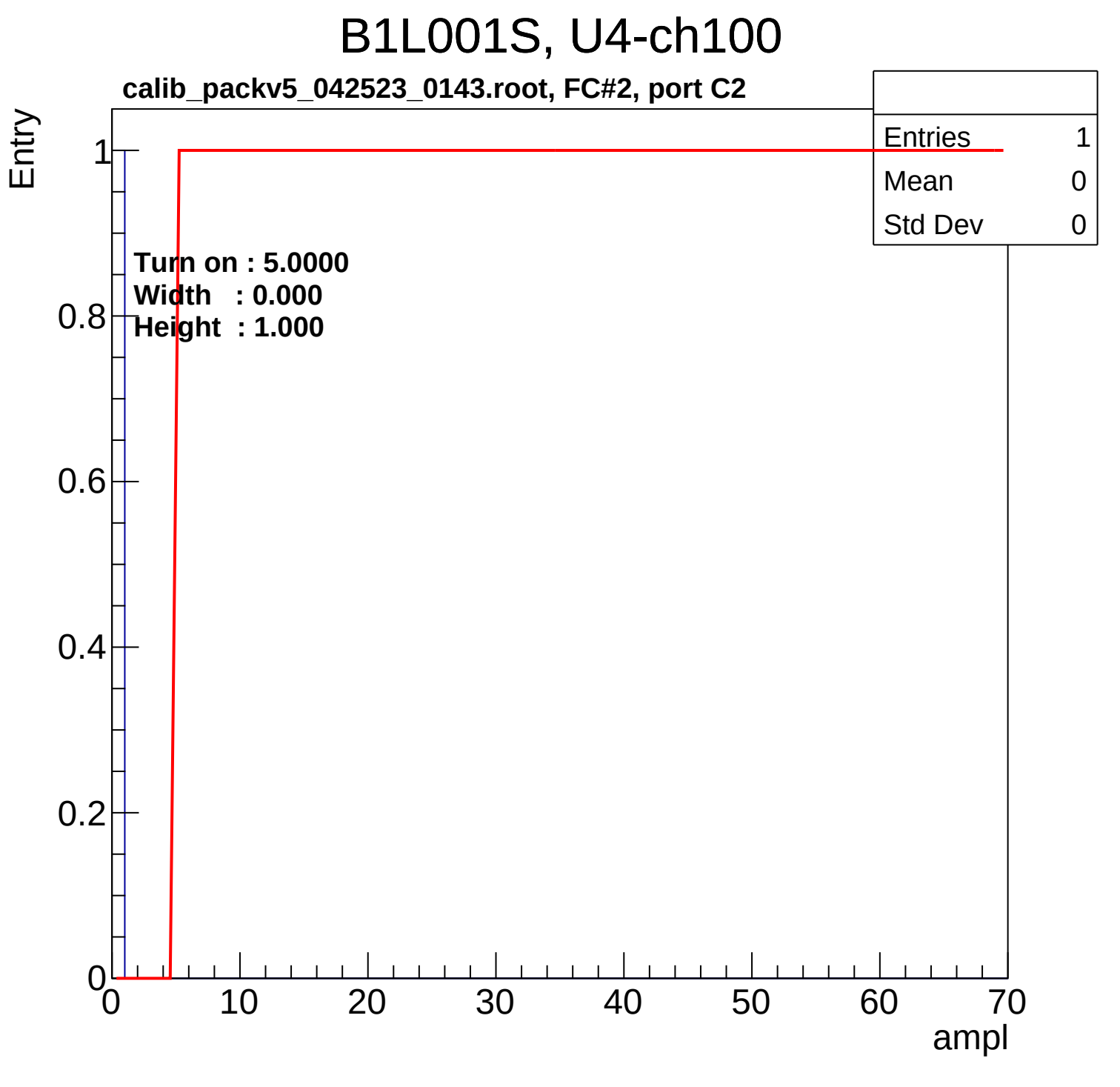
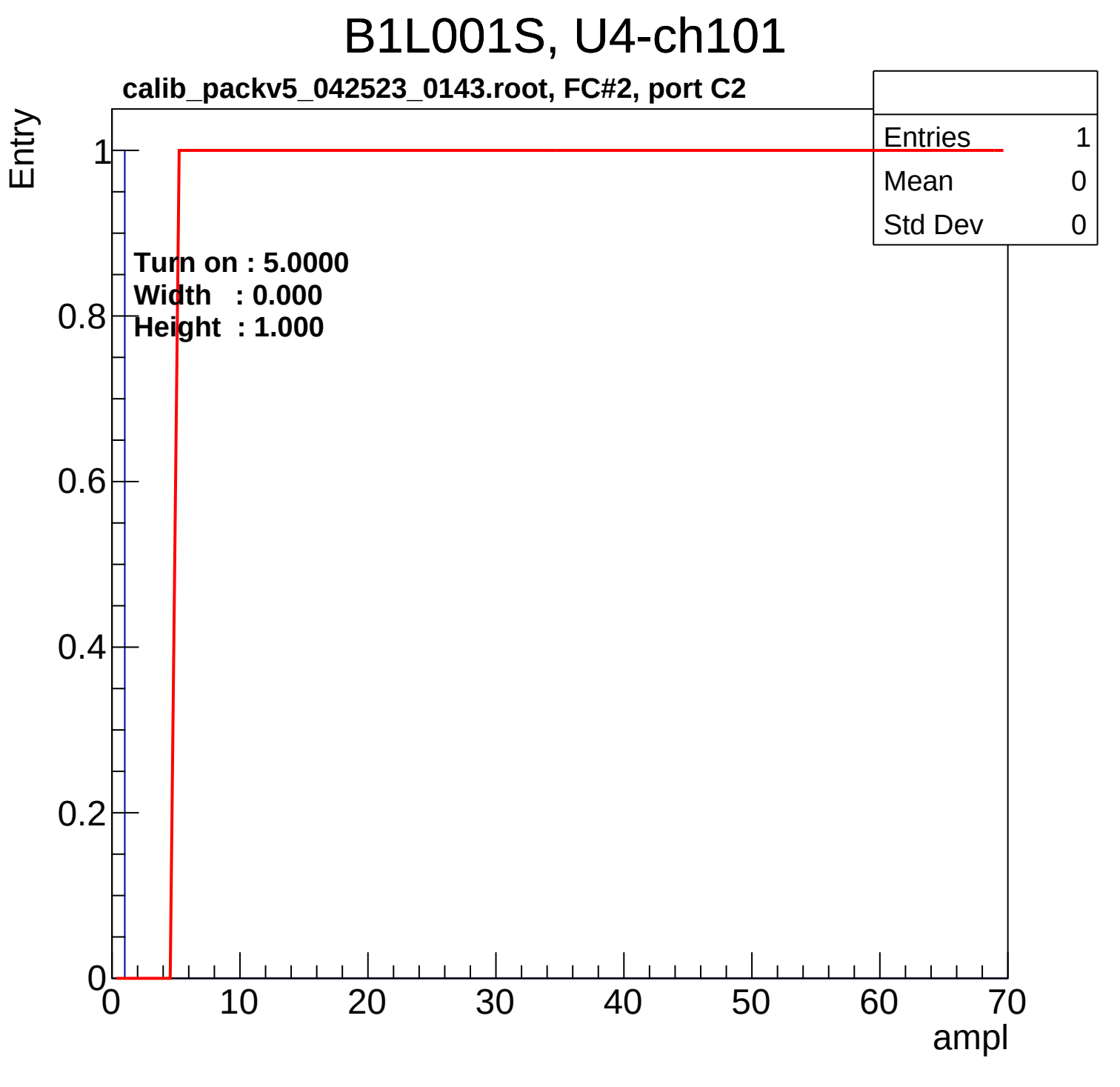
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L001S, U4-ch97
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L001S, U4-ch98
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L001S, U4-ch99
calib_packv5_042523_0143.root, FC#2, port C2
Entries 3
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L001S, U4-ch100
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L001S, U4-ch101
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
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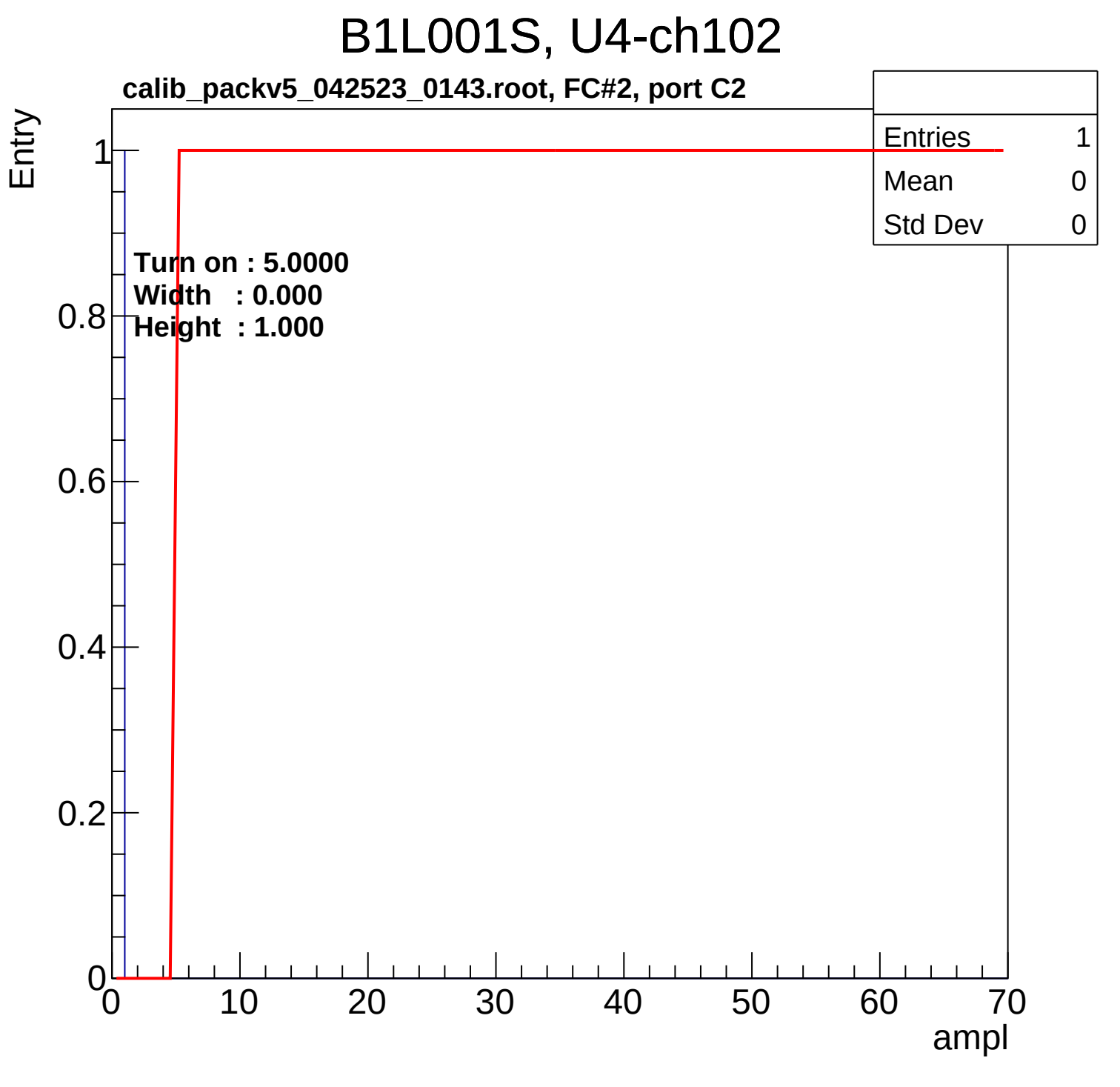
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L001S, U4-ch102
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
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0.4
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1
0
10
20
30
40
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60
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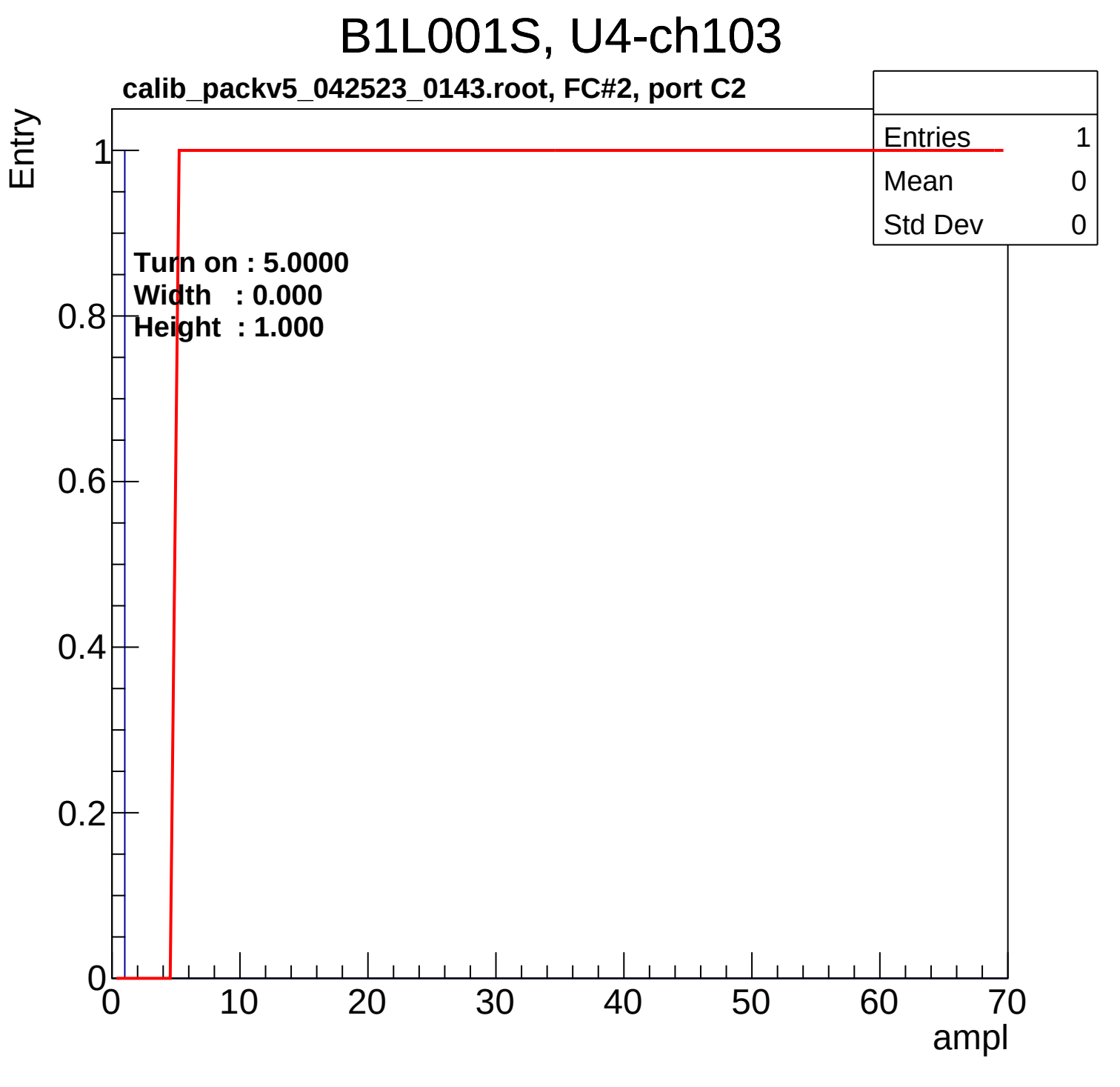
B1L001S, U4-ch103
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
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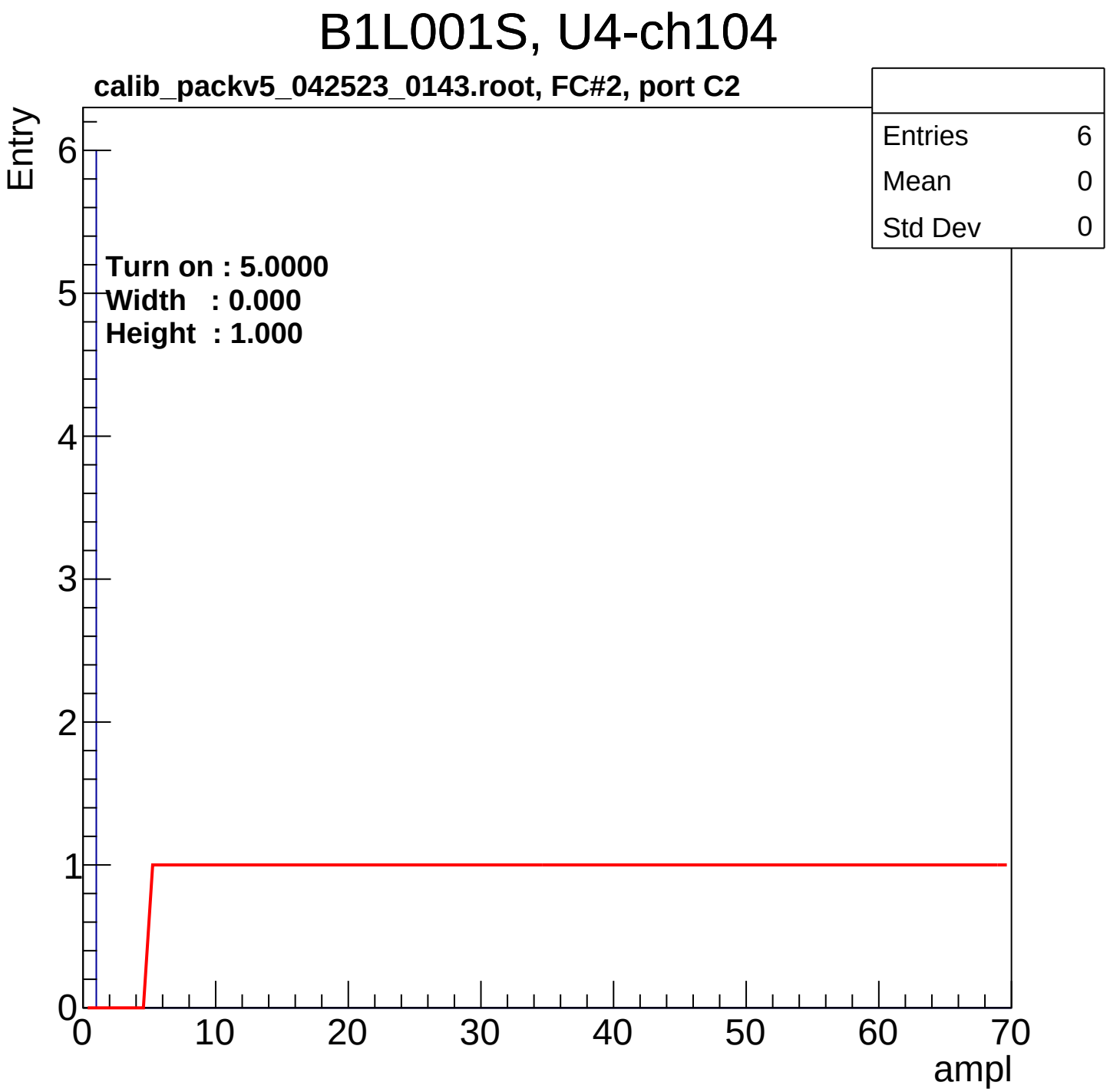
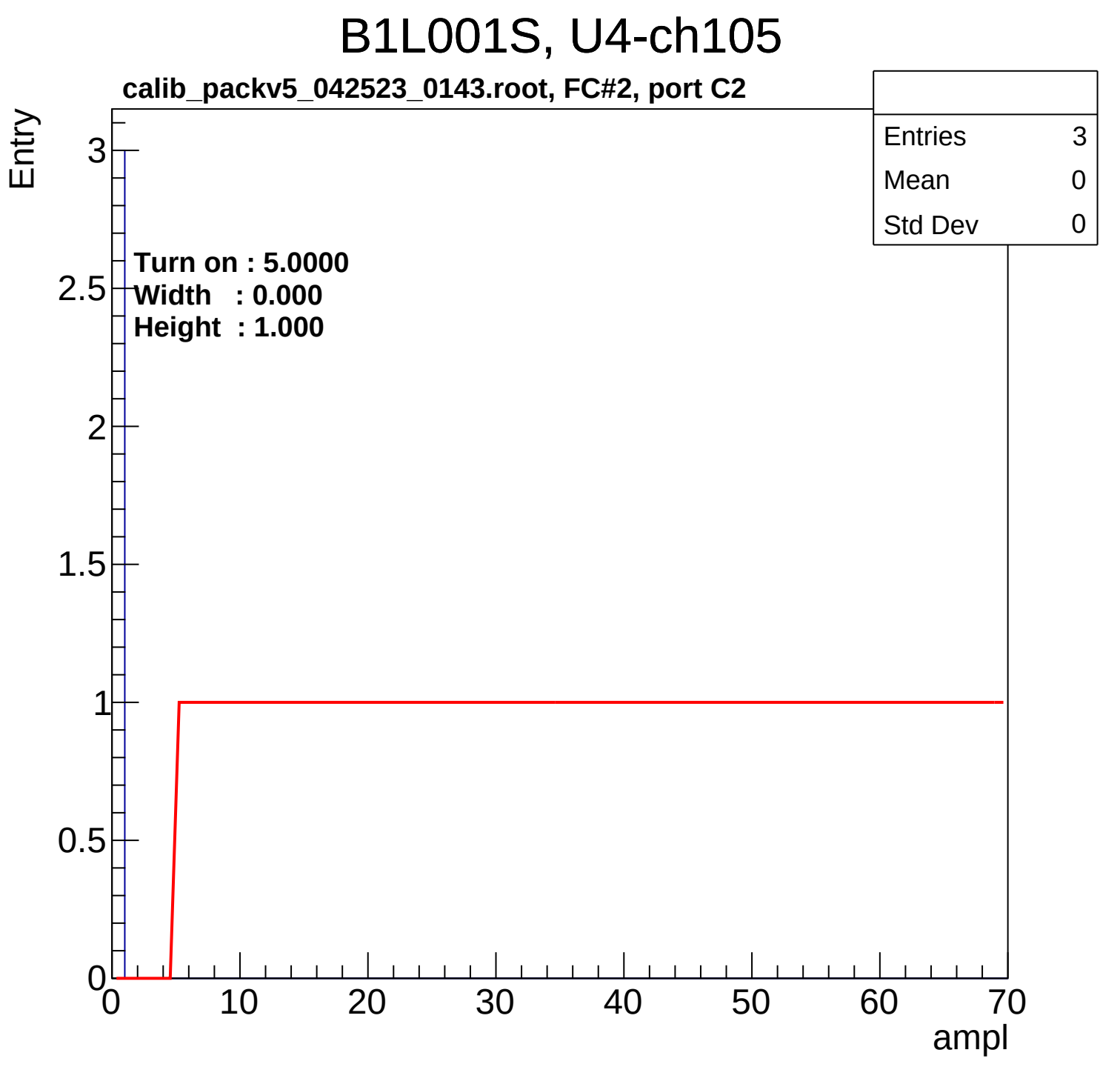
0
0
10
20
30
40
50
60
70
ampl


B1L001S, U4-ch104
calib_packv5_042523_0143.root, FC#2, port C2
Entries 6
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L001S, U4-ch105
calib_packv5_042523_0143.root, FC#2, port C2
Entries 3
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
10
20
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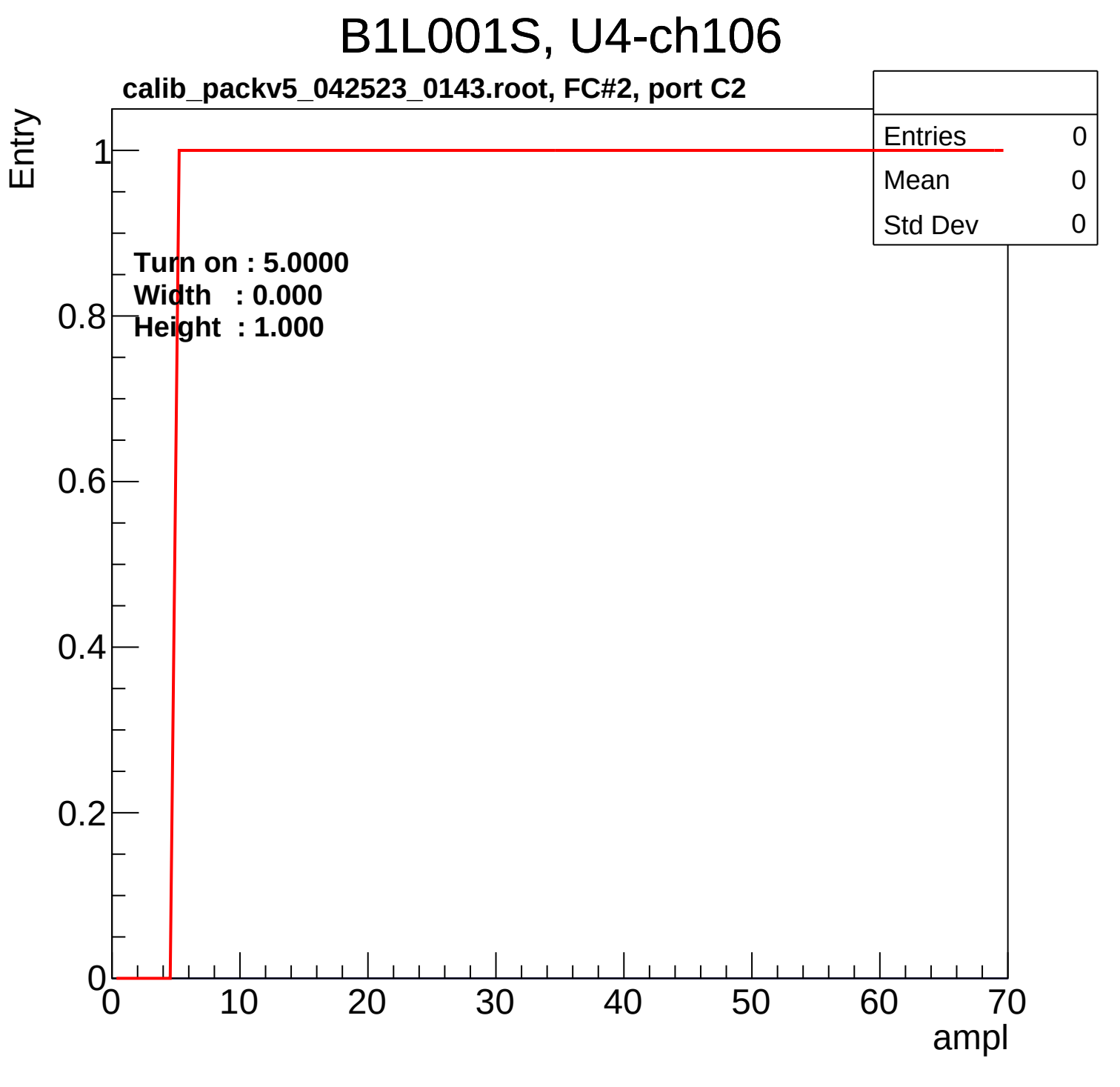
40
50
60
70


B1L001S, U4-ch106
calib_packv5_042523_0143.root, FC#2, port C2
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
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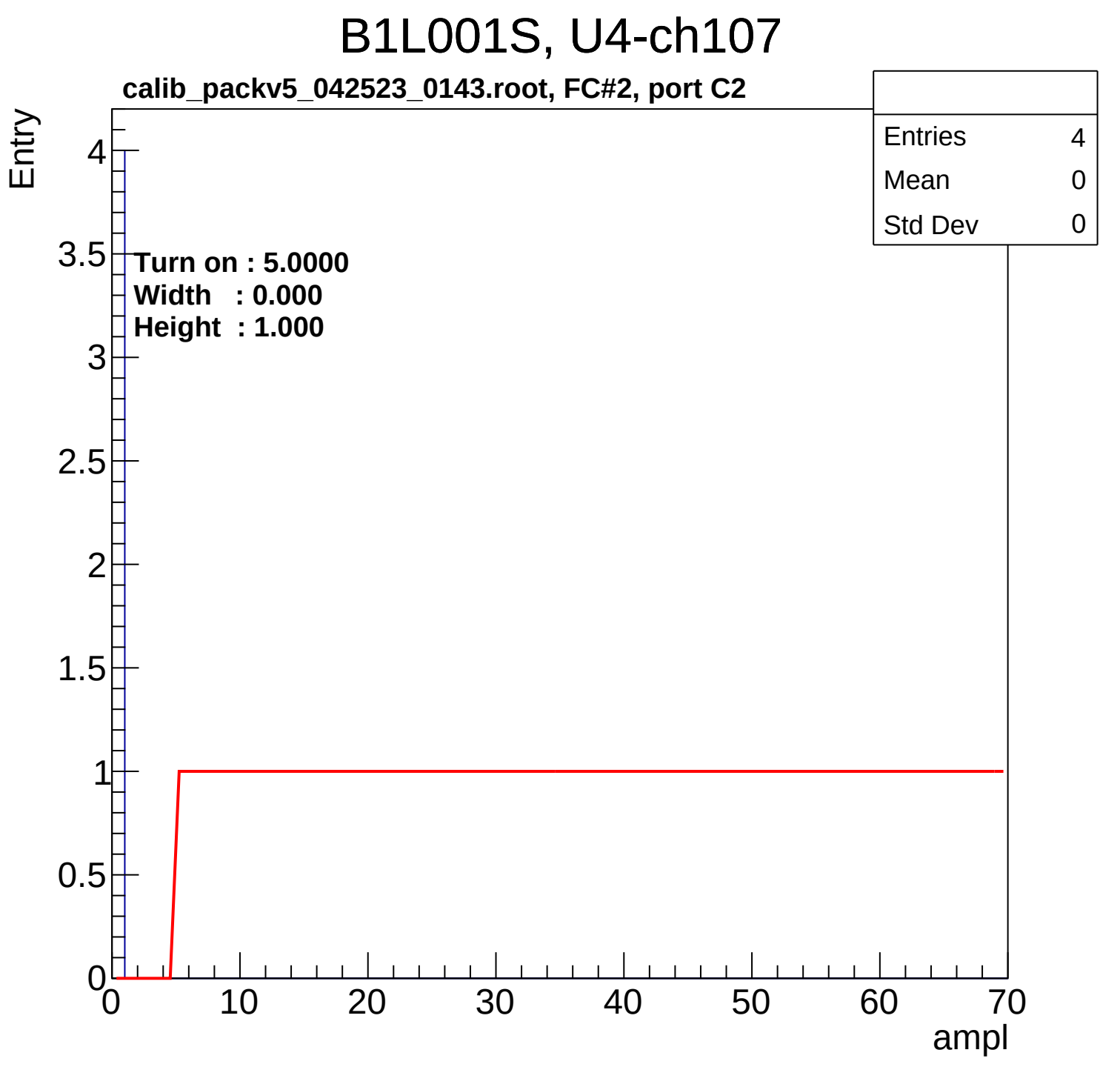
0
0
10
20
30
40
50
60
70
ampl


B1L001S, U4-ch107
calib_packv5_042523_0143.root, FC#2, port C2
Entries 4
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
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1
1.5
2
2.5
3
3.5
4
0
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20
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40
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60
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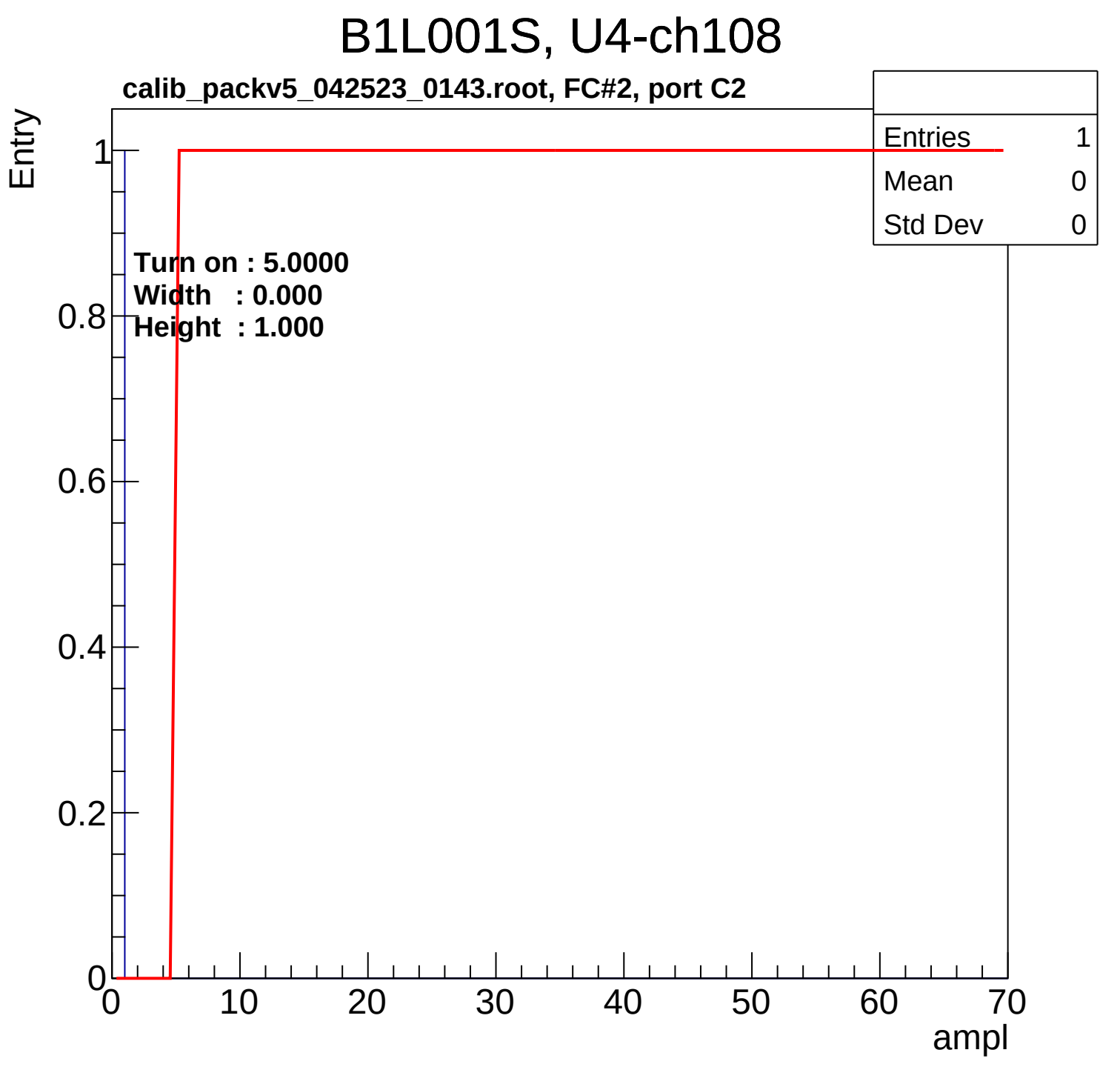
B1L001S, U4-ch108
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
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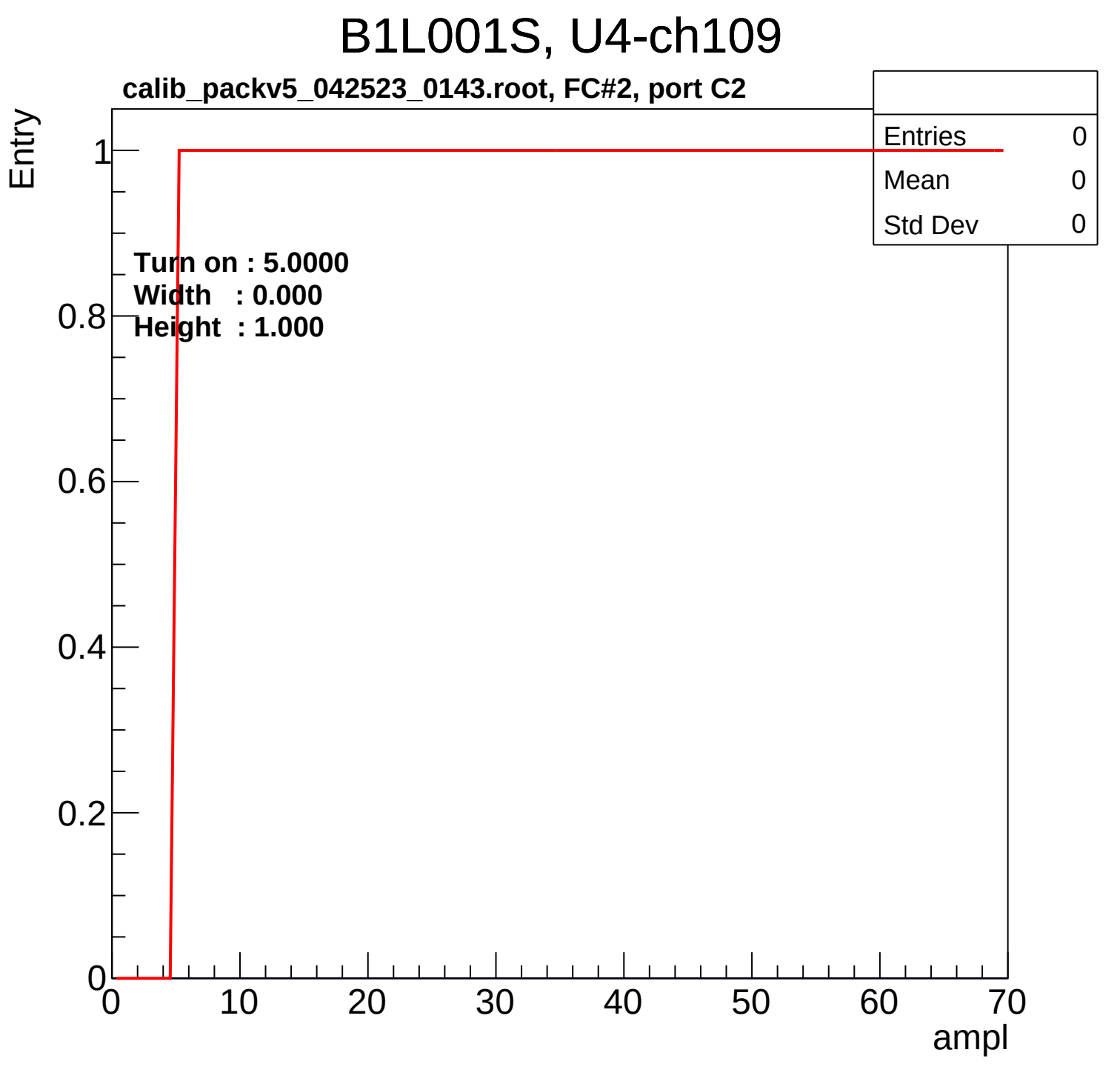
B1L001S, U4-ch109
calib_packv5_042523_0143.root, FC#2, port C2
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
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0.4
0.6
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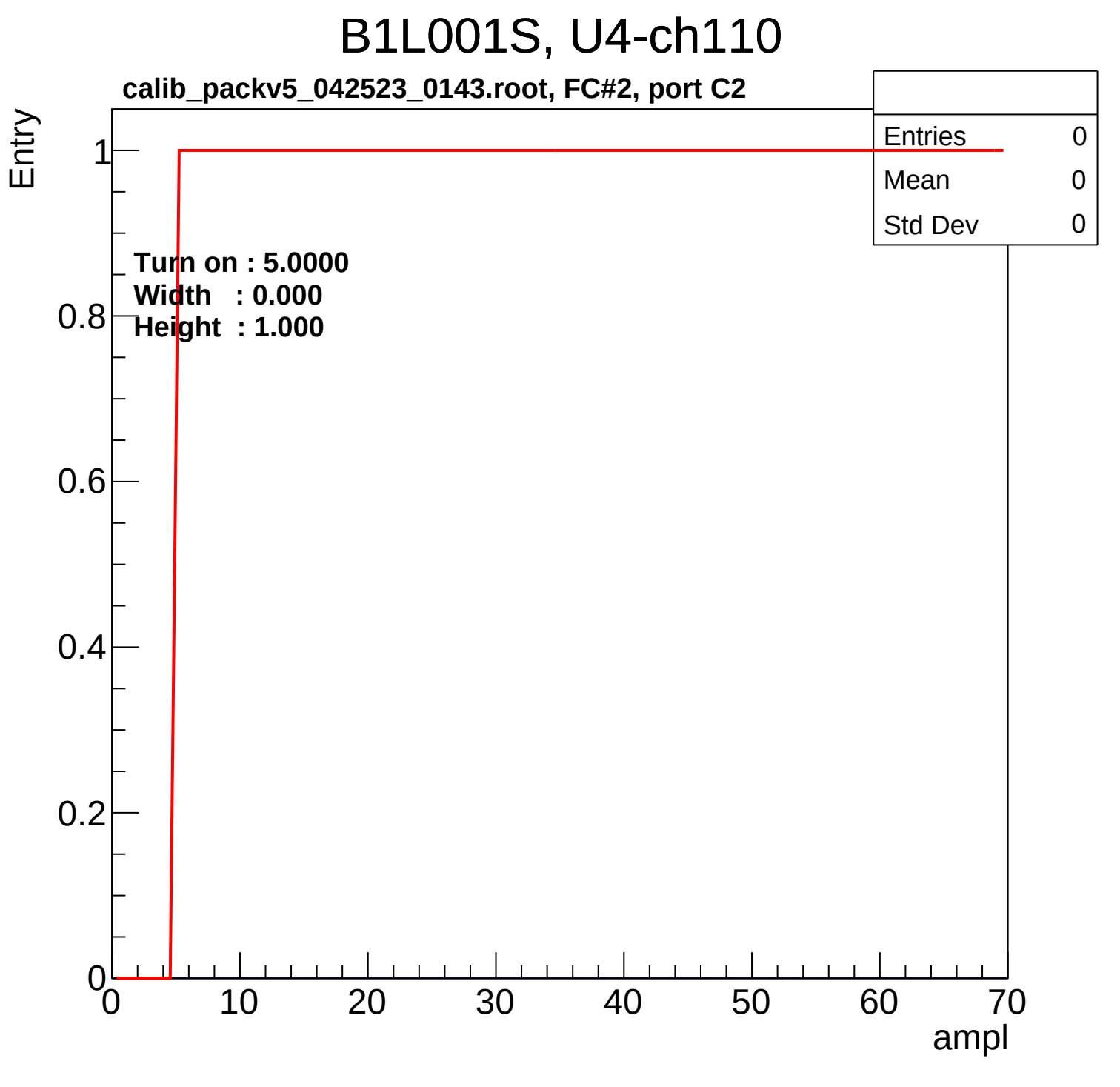
B1L001S, U4-ch110
calib_packv5_042523_0143.root, FC#2, port C2
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
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0.6
0.4
0.2
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20
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50
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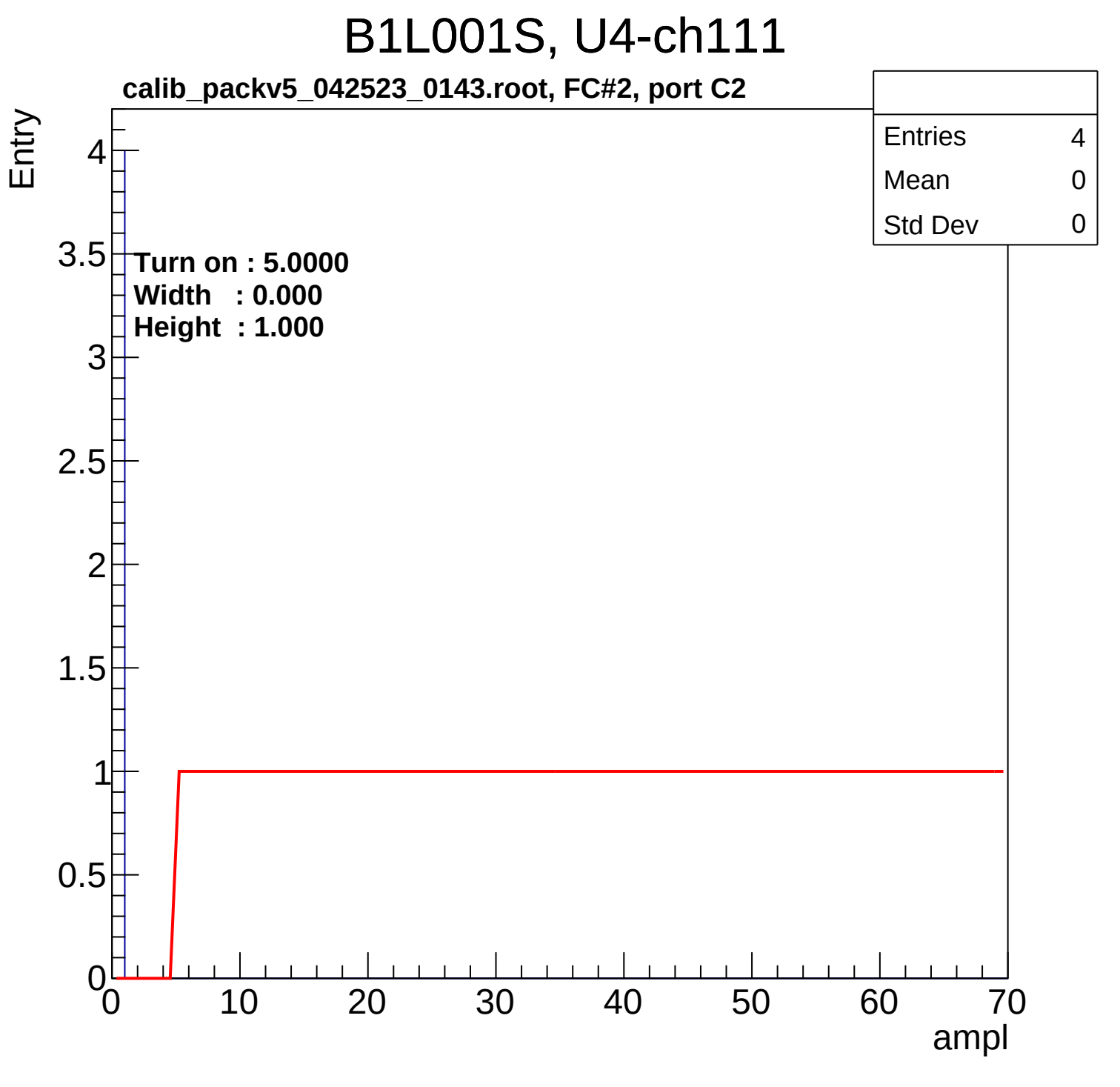
70
ampl


B1L001S, U4-ch111
calib_packv5_042523_0143.root, FC#2, port C2
Entries 4
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
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1.5
2
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3.5
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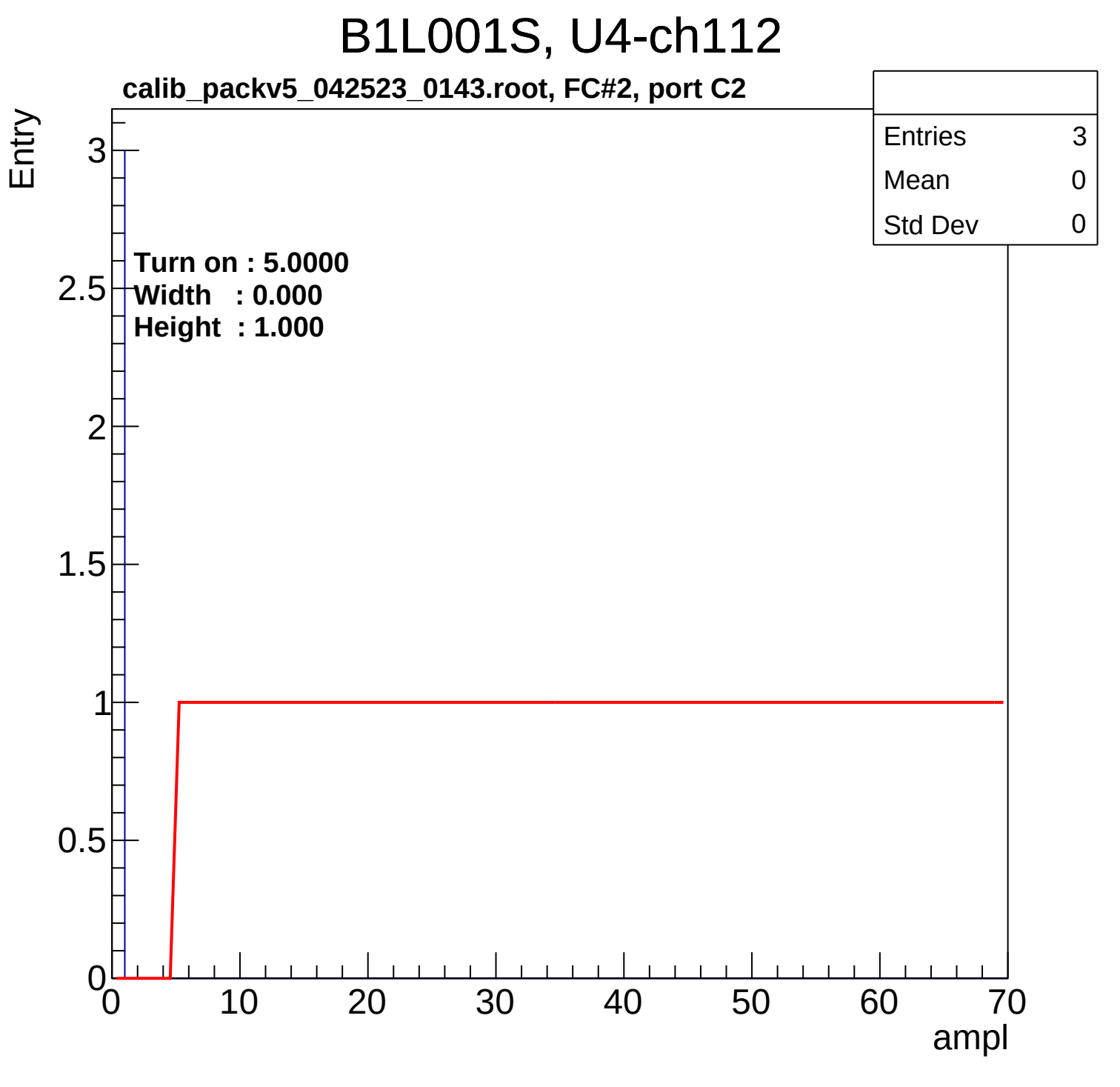
B1L001S, U4-ch112
calib_packv5_042523_0143.root, FC#2, port C2
Entries 3
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
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20
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40
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60
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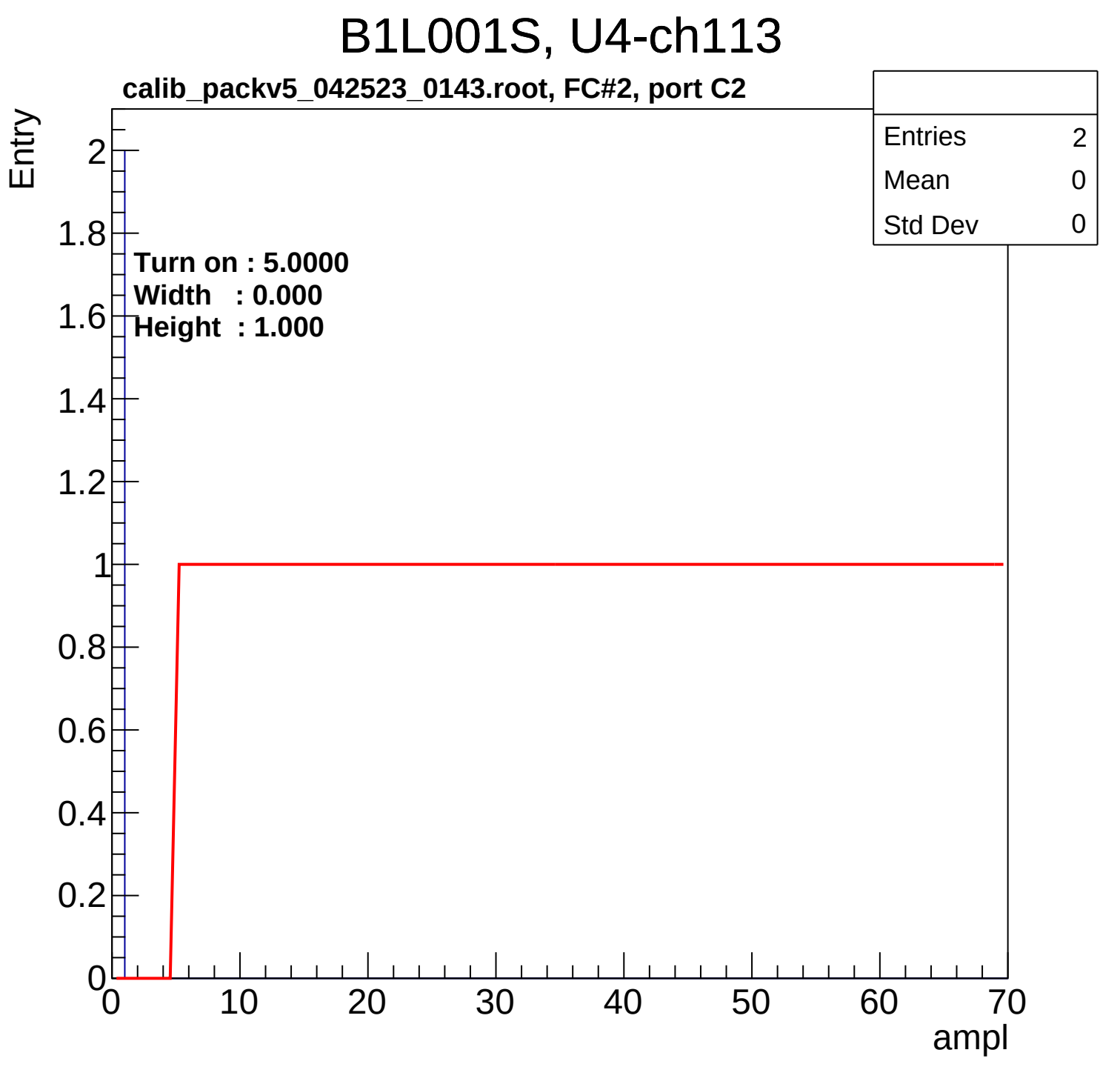
B1L001S, U4-ch113
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
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1
1.2
1.4
1.6
1.8
2
0
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40
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60
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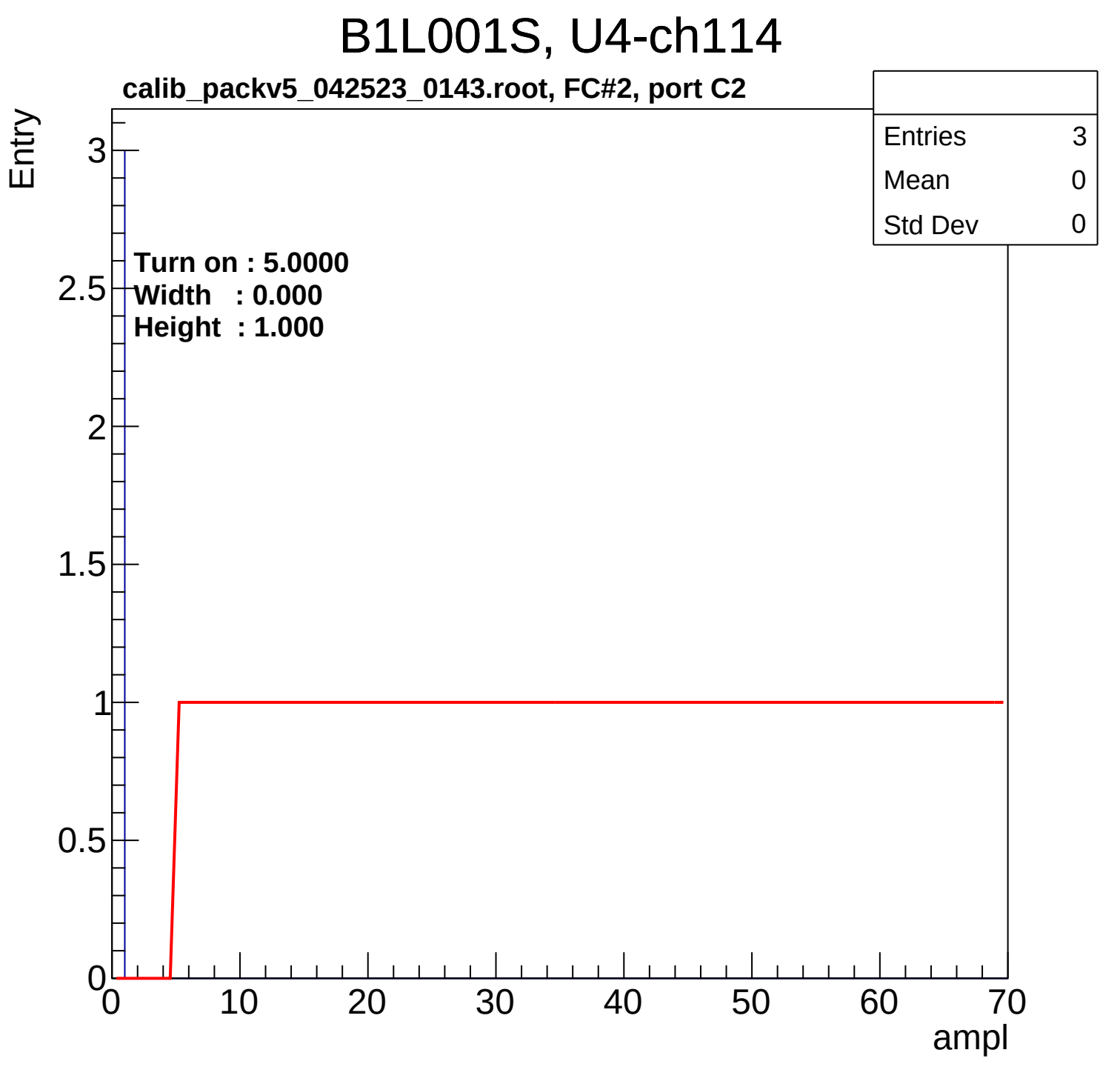
B1L001S, U4-ch114
calib_packv5_042523_0143.root, FC#2, port C2
Entries 3
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
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1
1.5
2
2.5
3
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20
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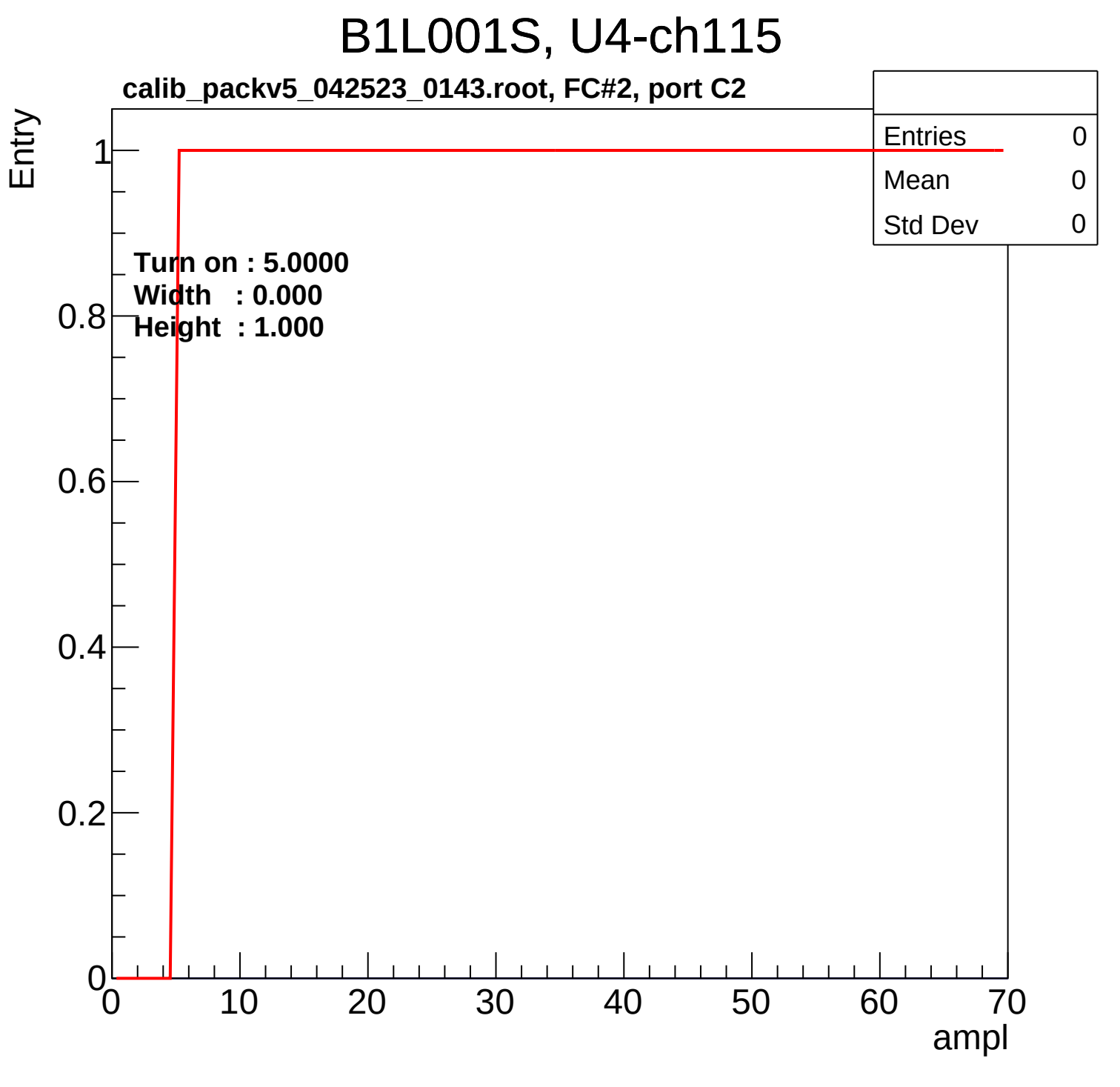
B1L001S, U4-ch115
calib_packv5_042523_0143.root, FC#2, port C2
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
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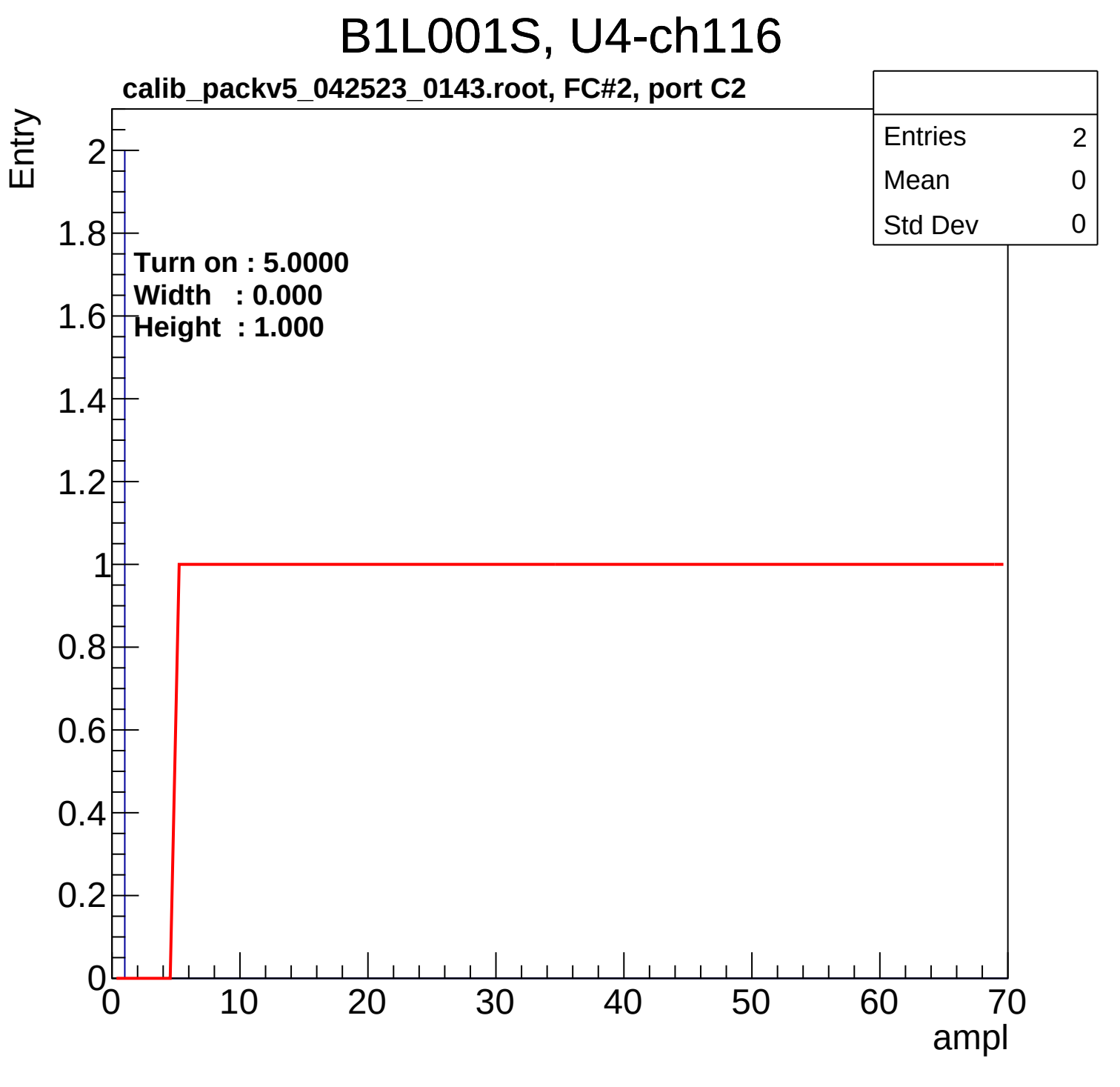
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L001S, U4-ch116
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
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20
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60
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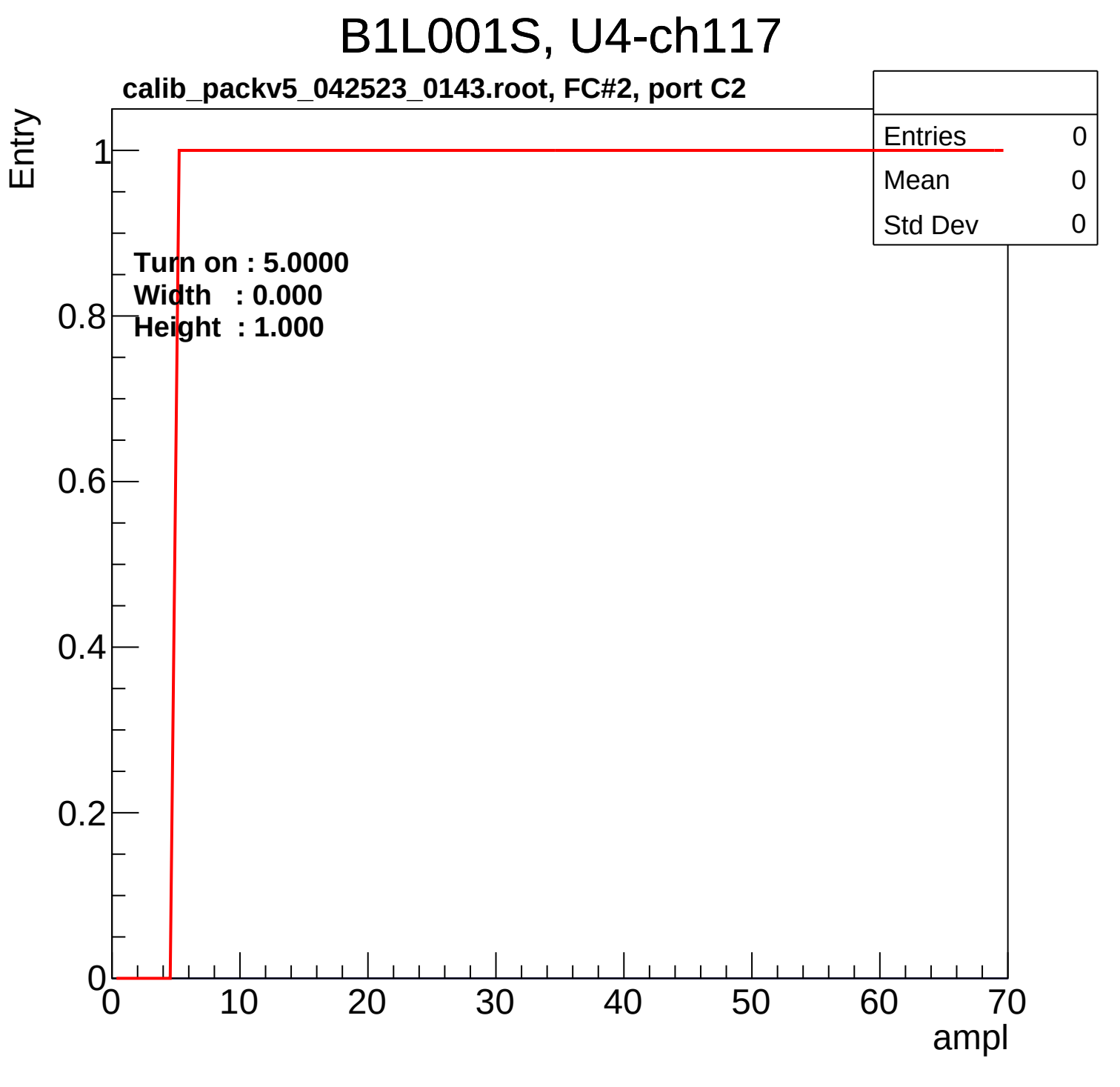
B1L001S, U4-ch117
calib_packv5_042523_0143.root, FC#2, port C2
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
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0.6
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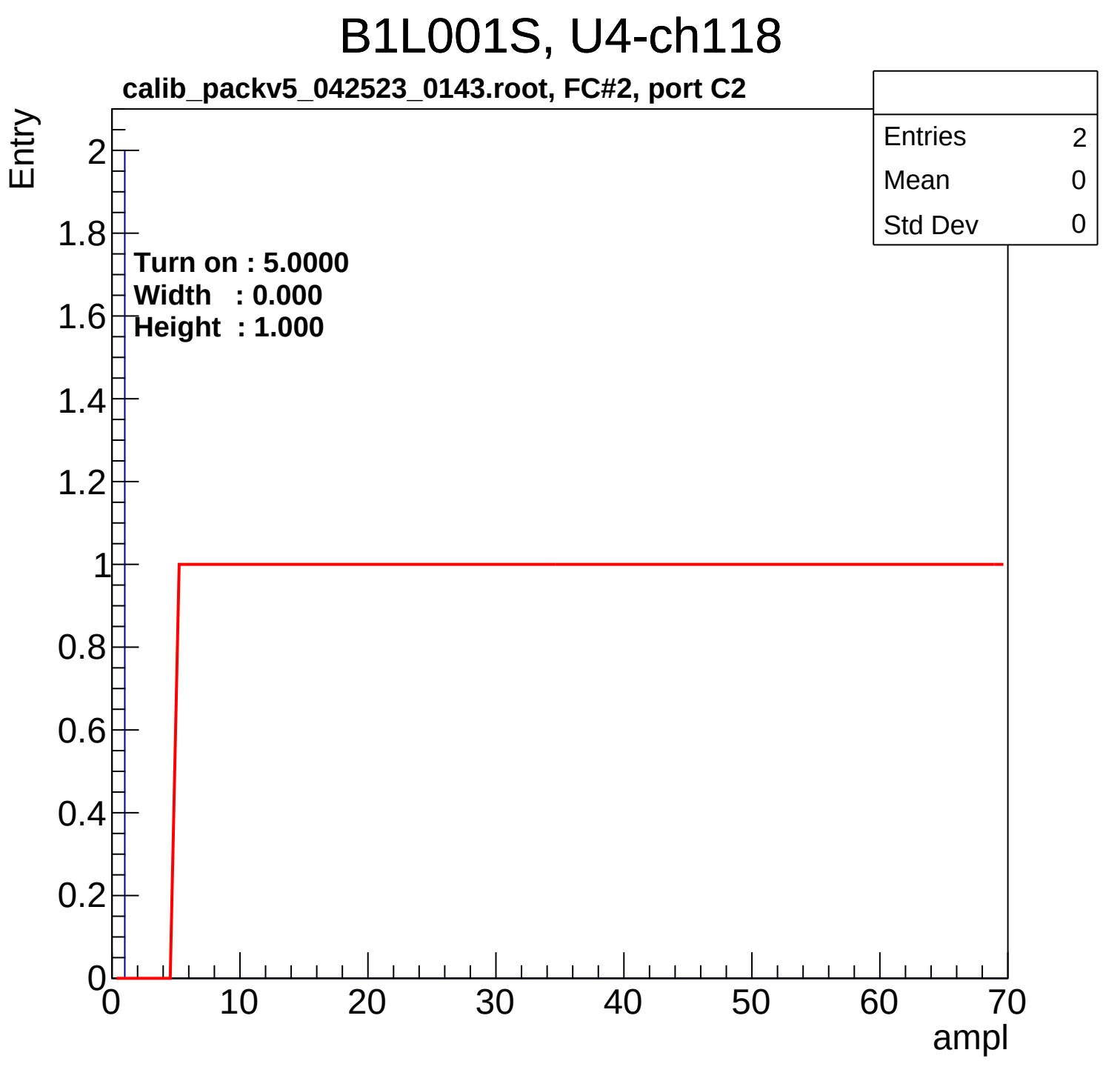
B1L001S, U4-ch118
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
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0.2
0.4
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1.2
1.4
1.6
1.8
2
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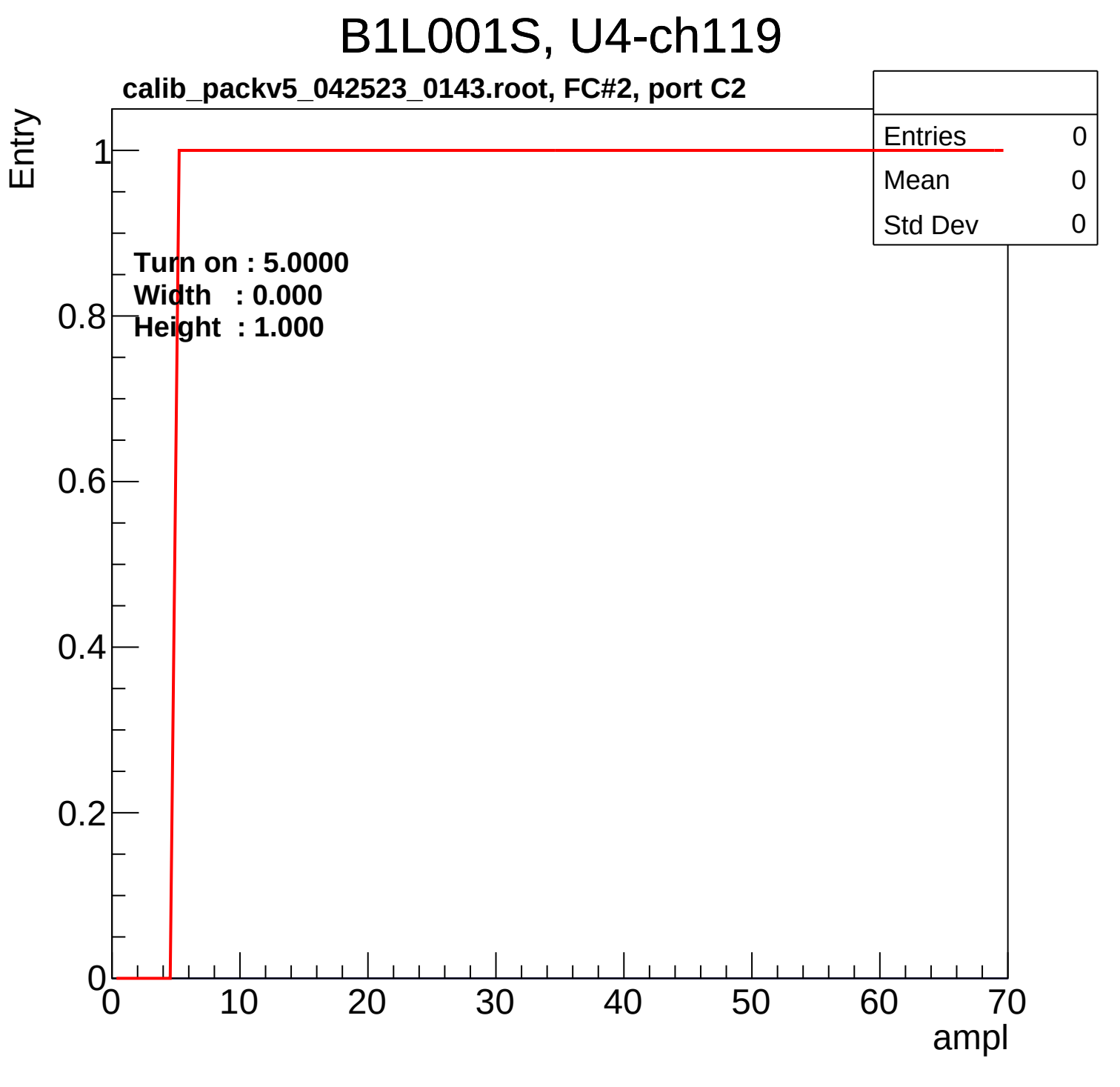
B1L001S, U4-ch119
calib_packv5_042523_0143.root, FC#2, port C2
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
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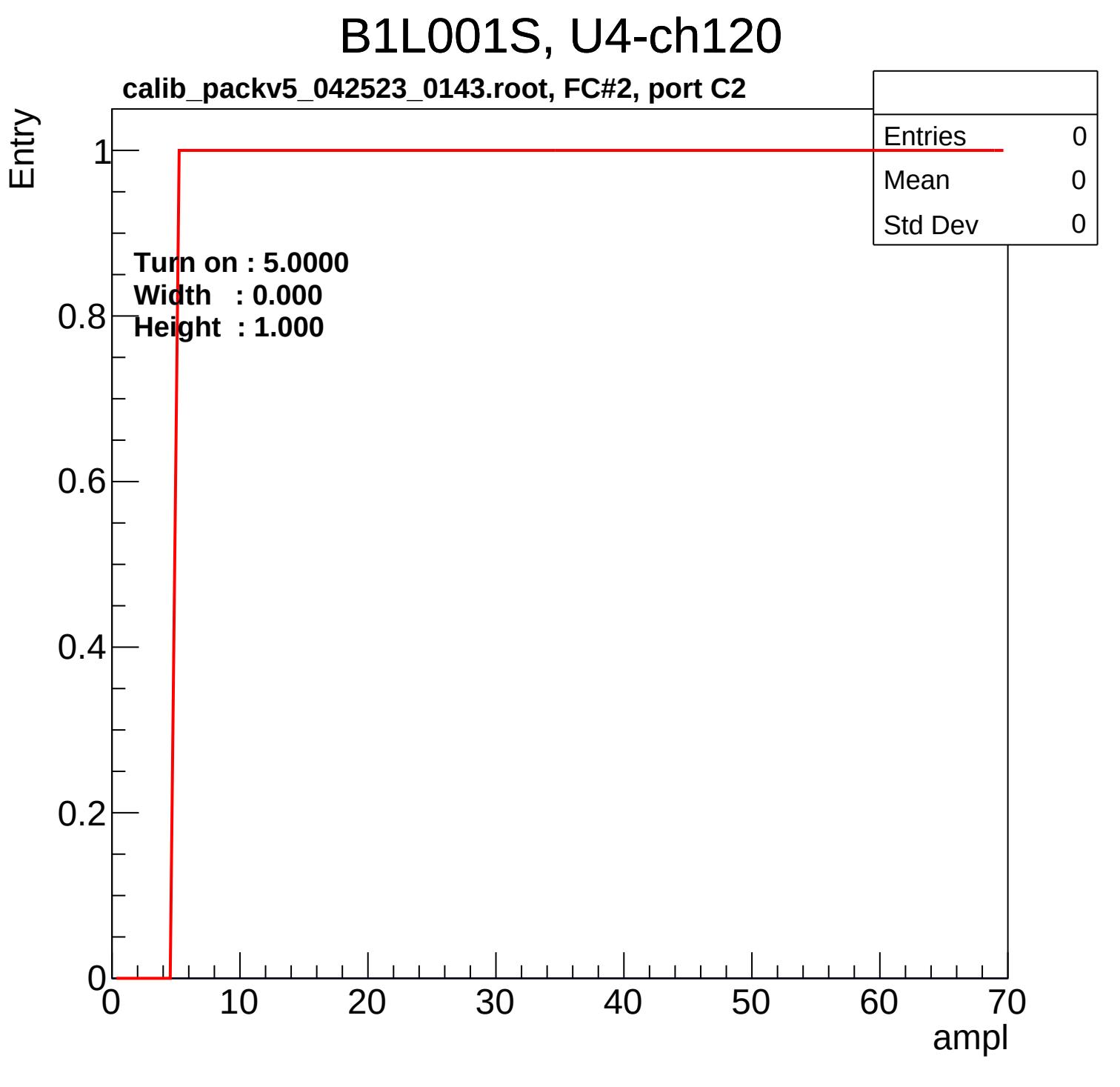
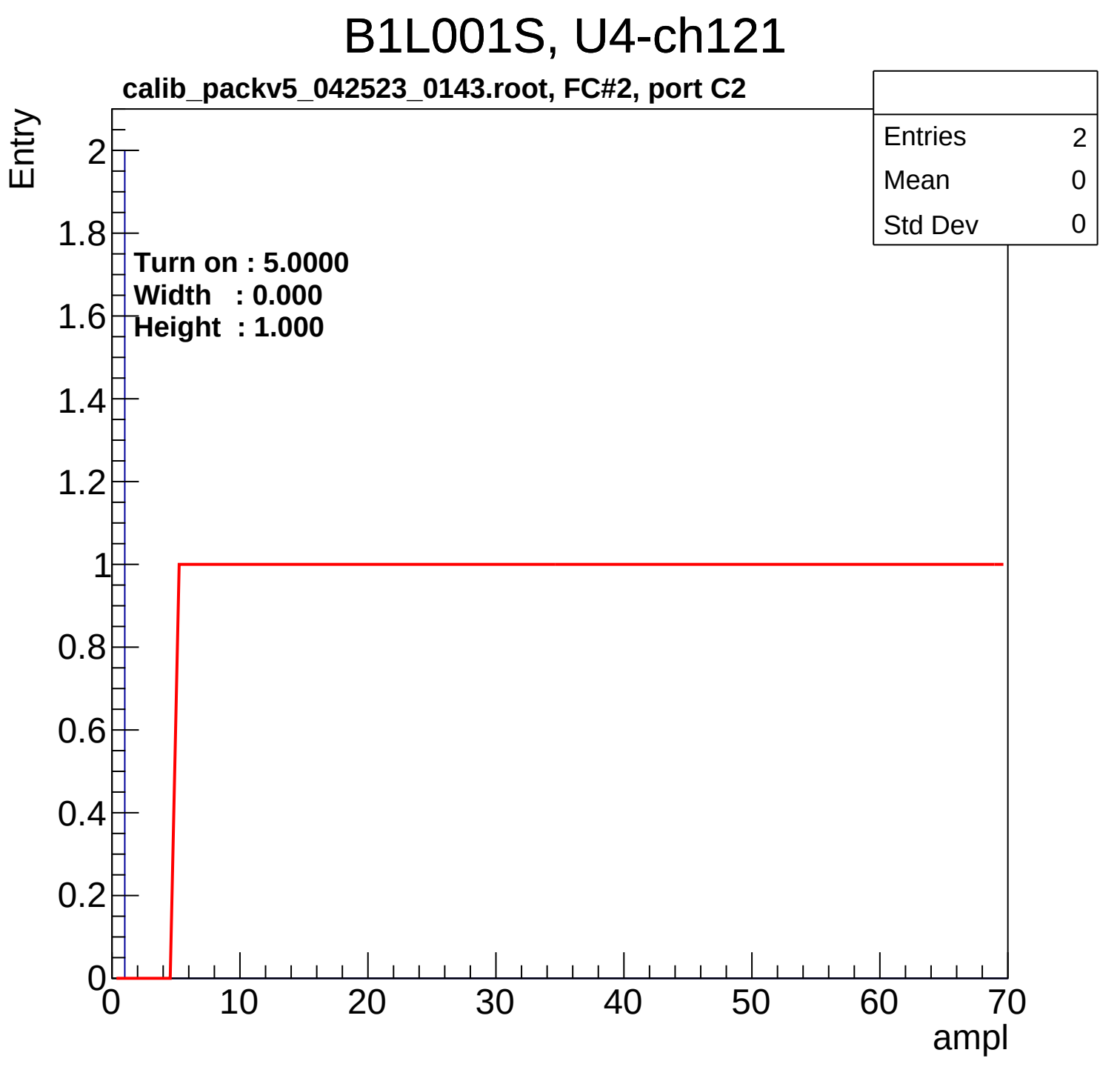
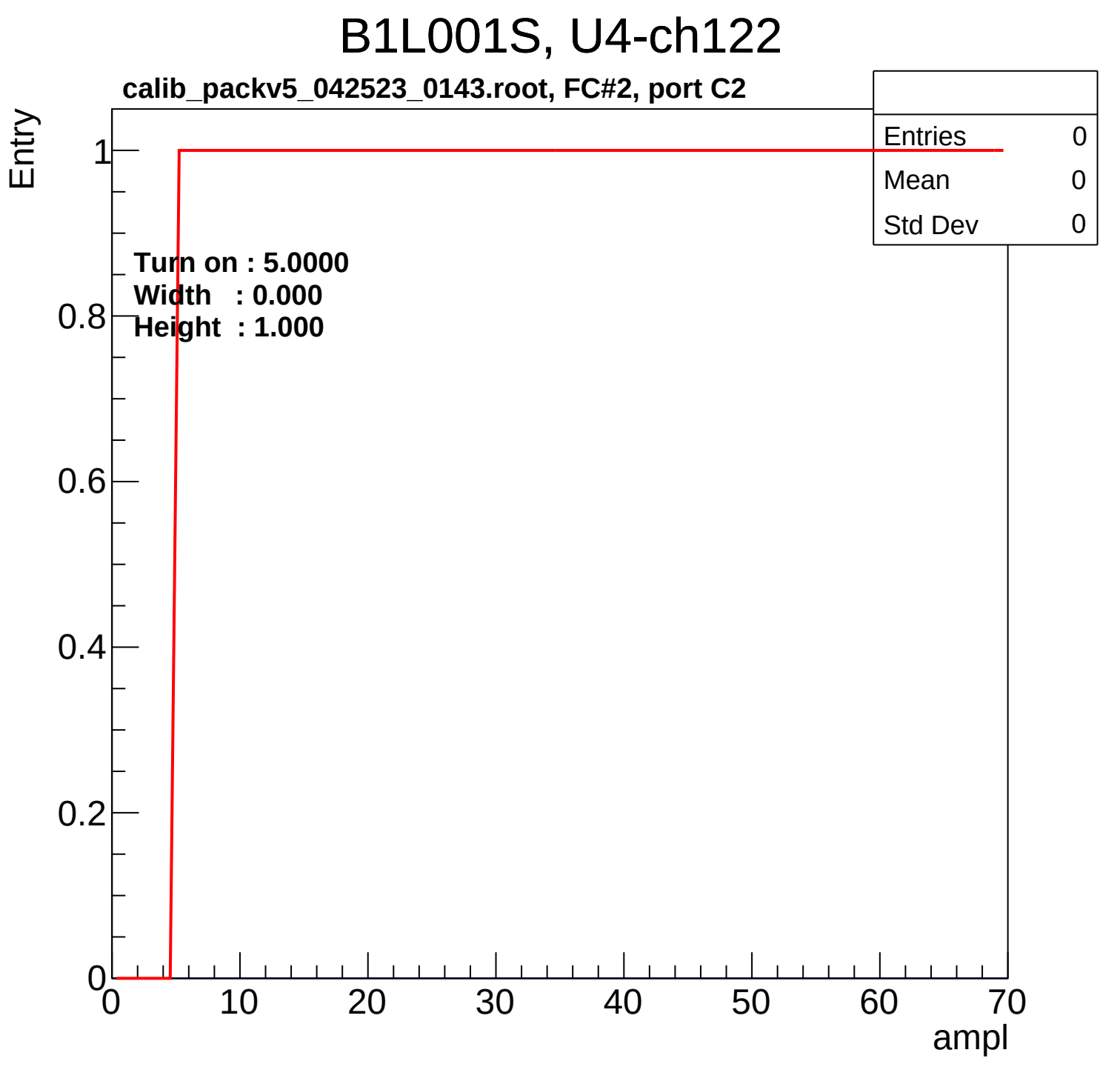
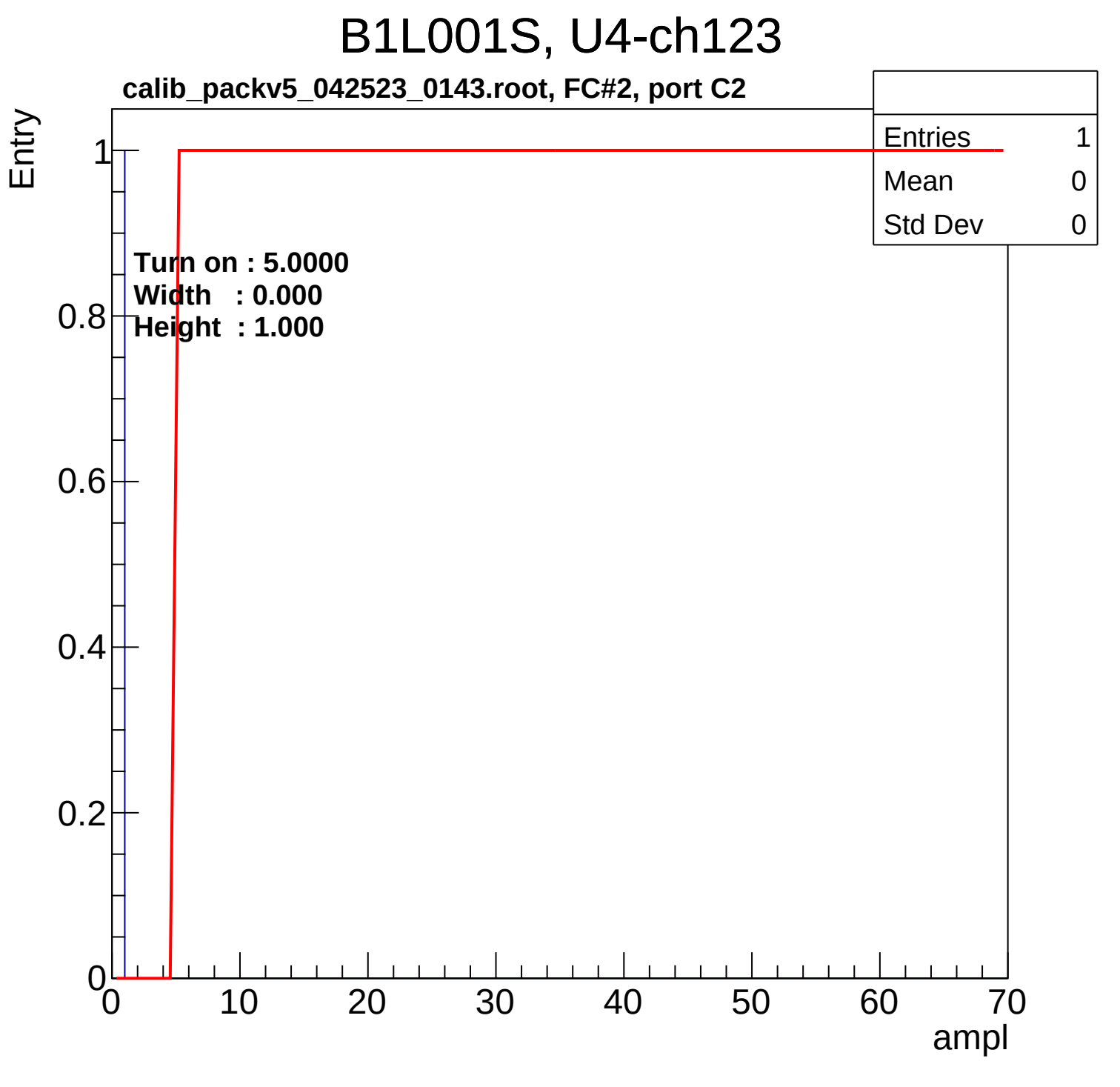
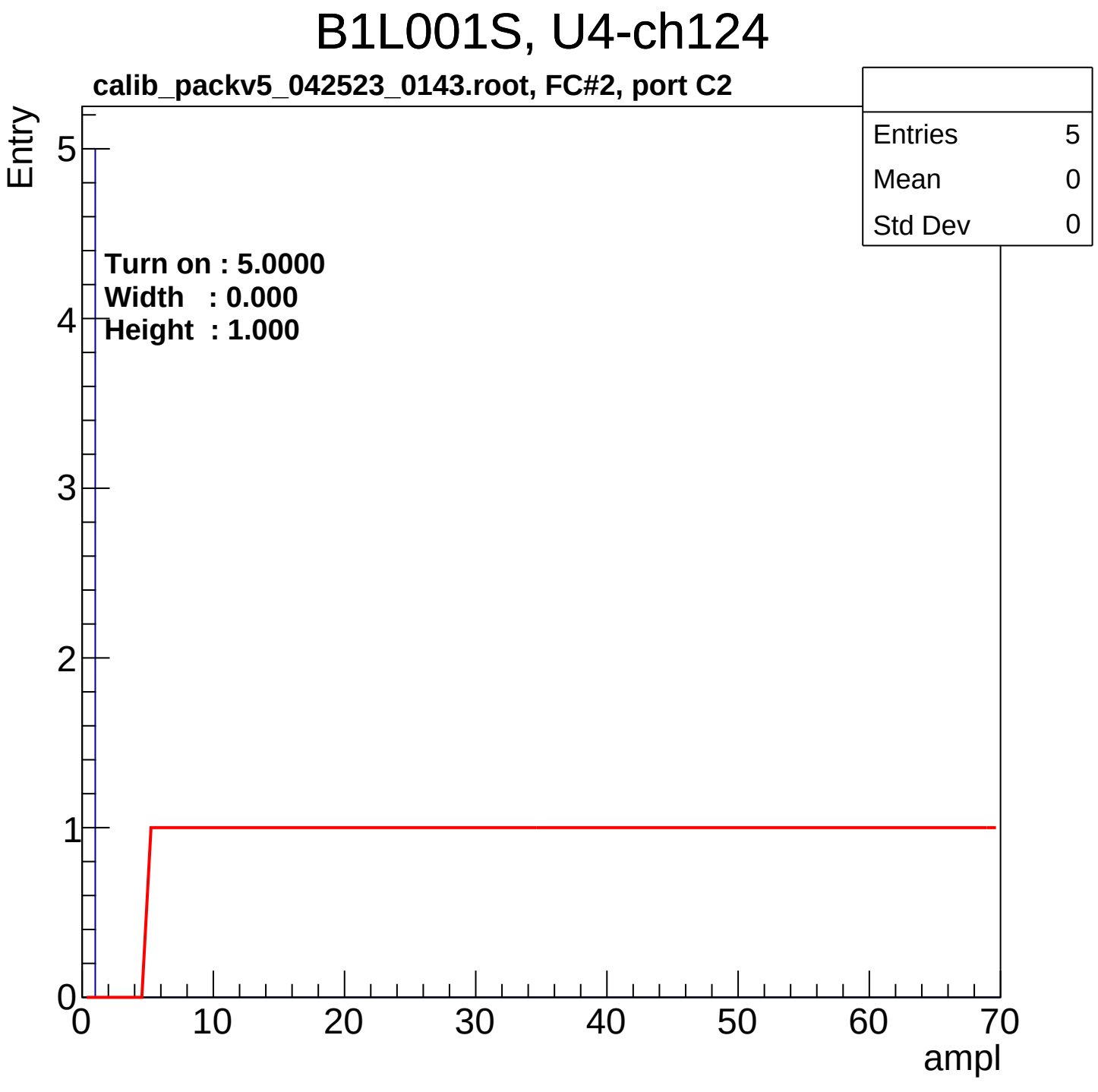
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

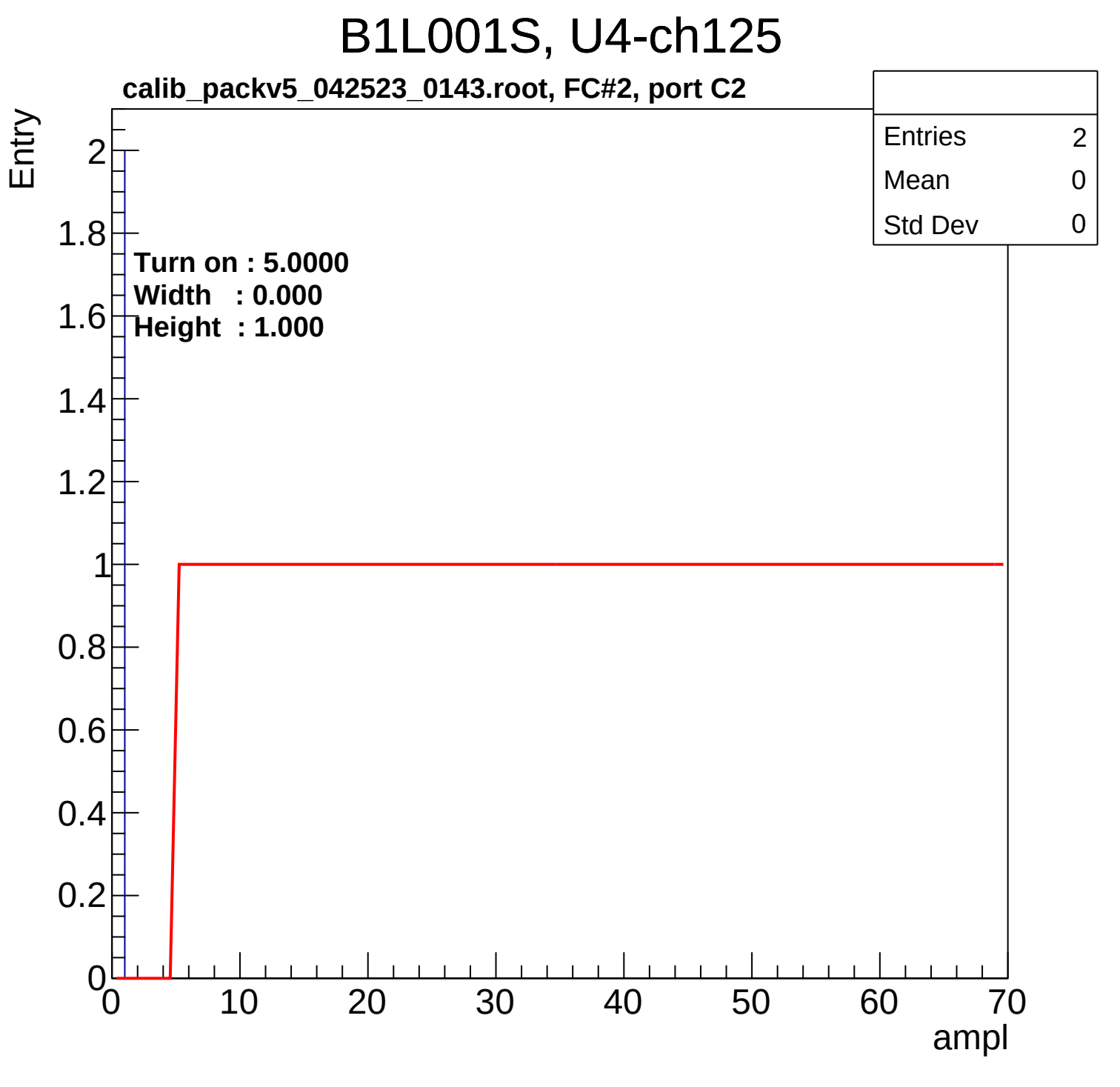

B1L001S, U4-ch120
calib_packv5_042523_0143.root, FC#2, port C2
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70

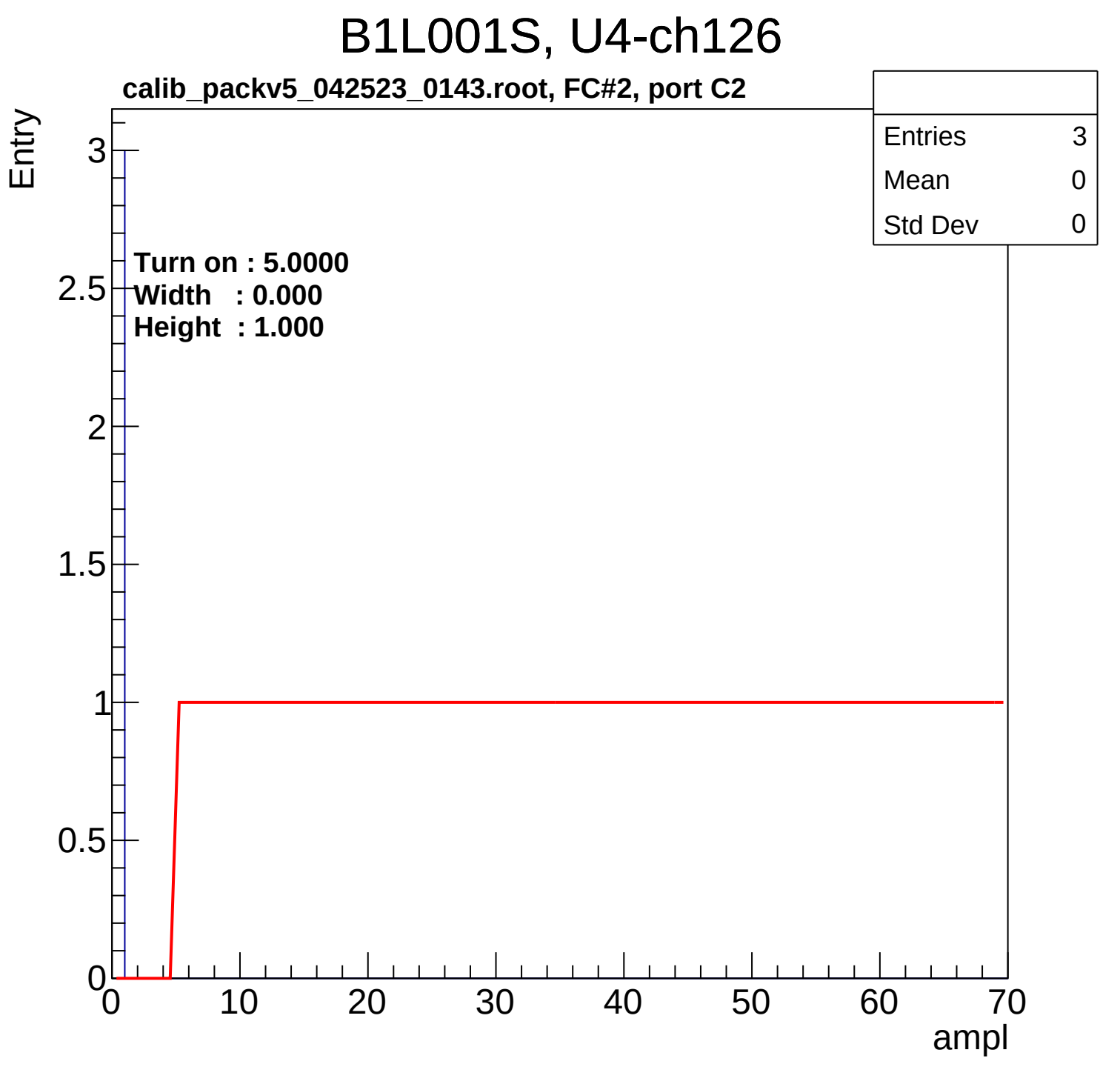

B1L001S, U4-ch121
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

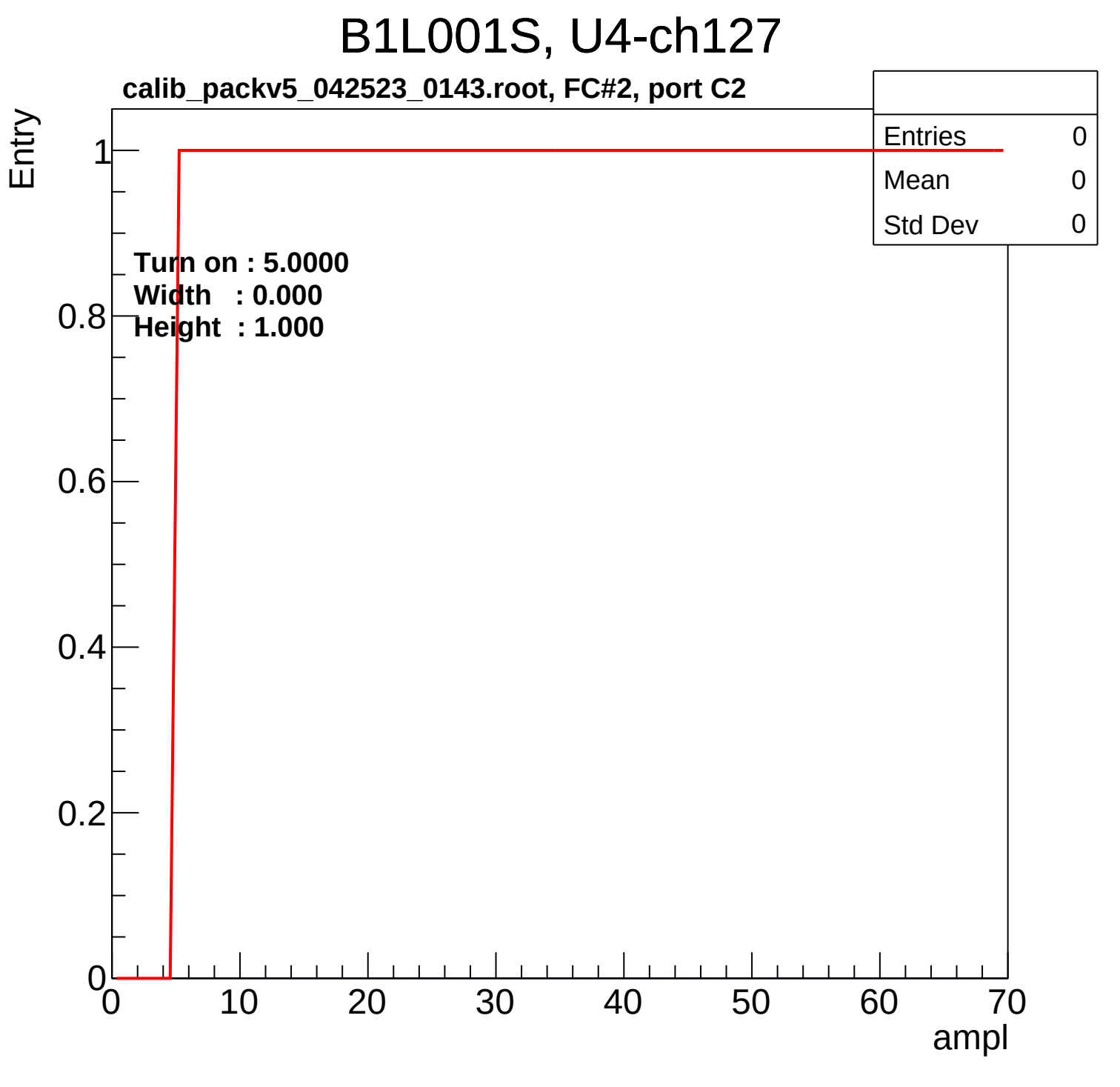

B1L001S, U4-ch122
calib_packv5_042523_0143.root, FC#2, port C2
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

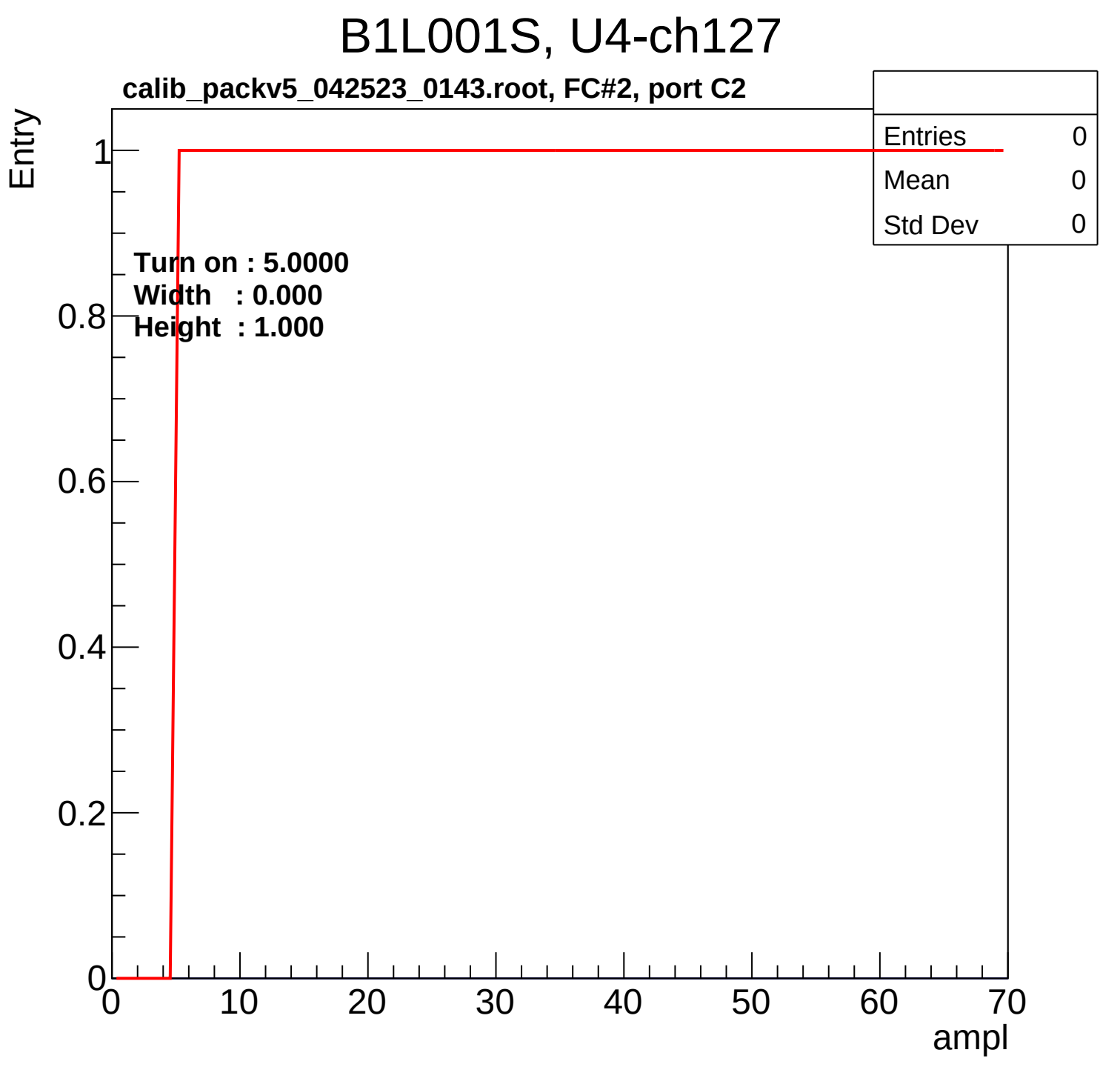

B1L001S, U4-ch123
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70


B1L001S, U4-ch124
calib_packv5_042523_0143.root, FC#2, port C2
Entries 5
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L001S, U4-ch125
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L001S, U4-ch126
calib_packv5_042523_0143.root, FC#2, port C2
Entries 3
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L001S, U4-ch127
calib_packv5_042523_0143.root, FC#2, port C2
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70


B1L001S, U4-ch127
calib_packv5_042523_0143.root, FC#2, port C2
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70