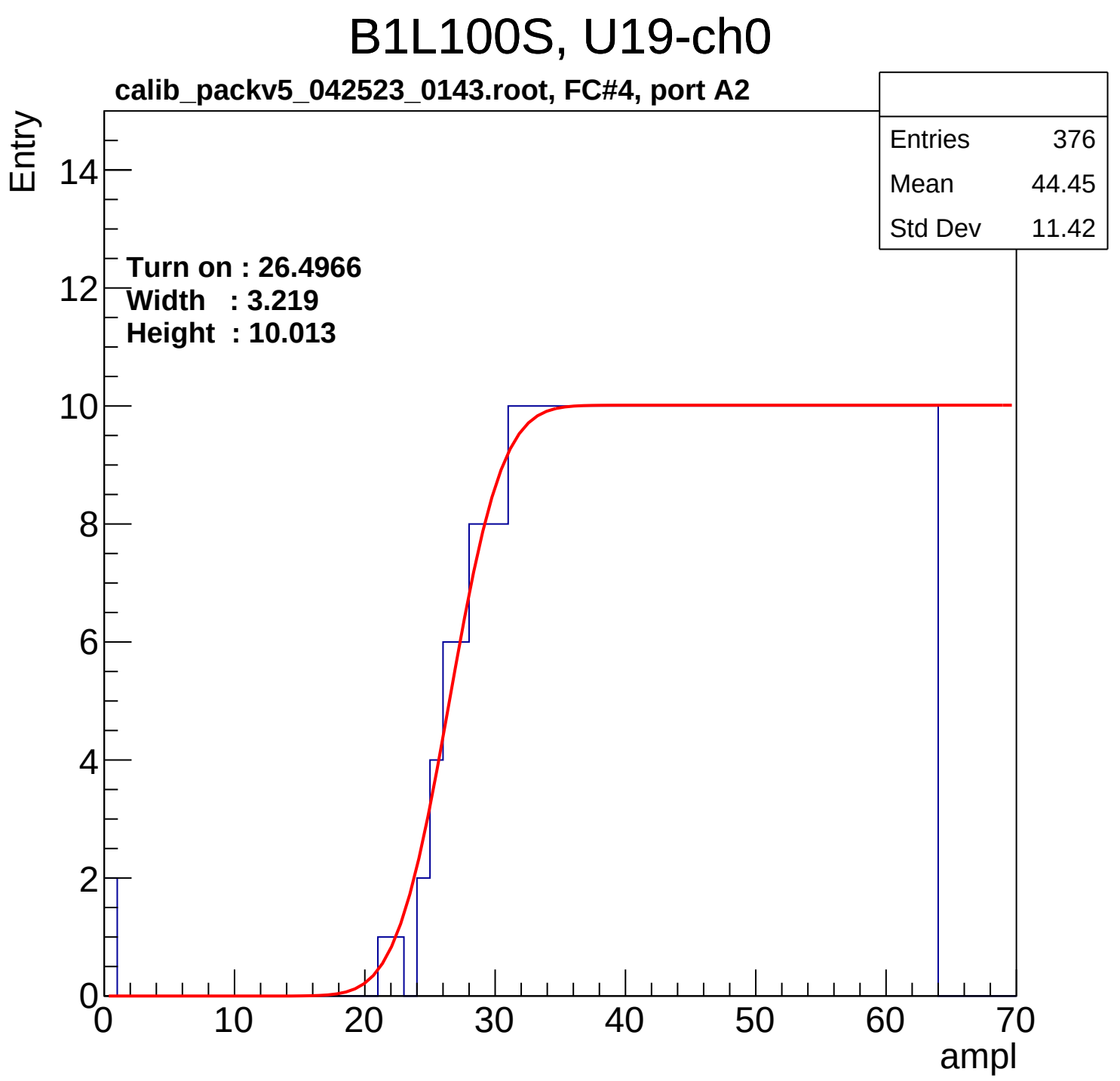
B1L100S, U19-ch0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 376
Mean 44.45
Std Dev 11.42
Turn on : 26.4966
Width : 3.219
Height : 10.013
Entry
ampl
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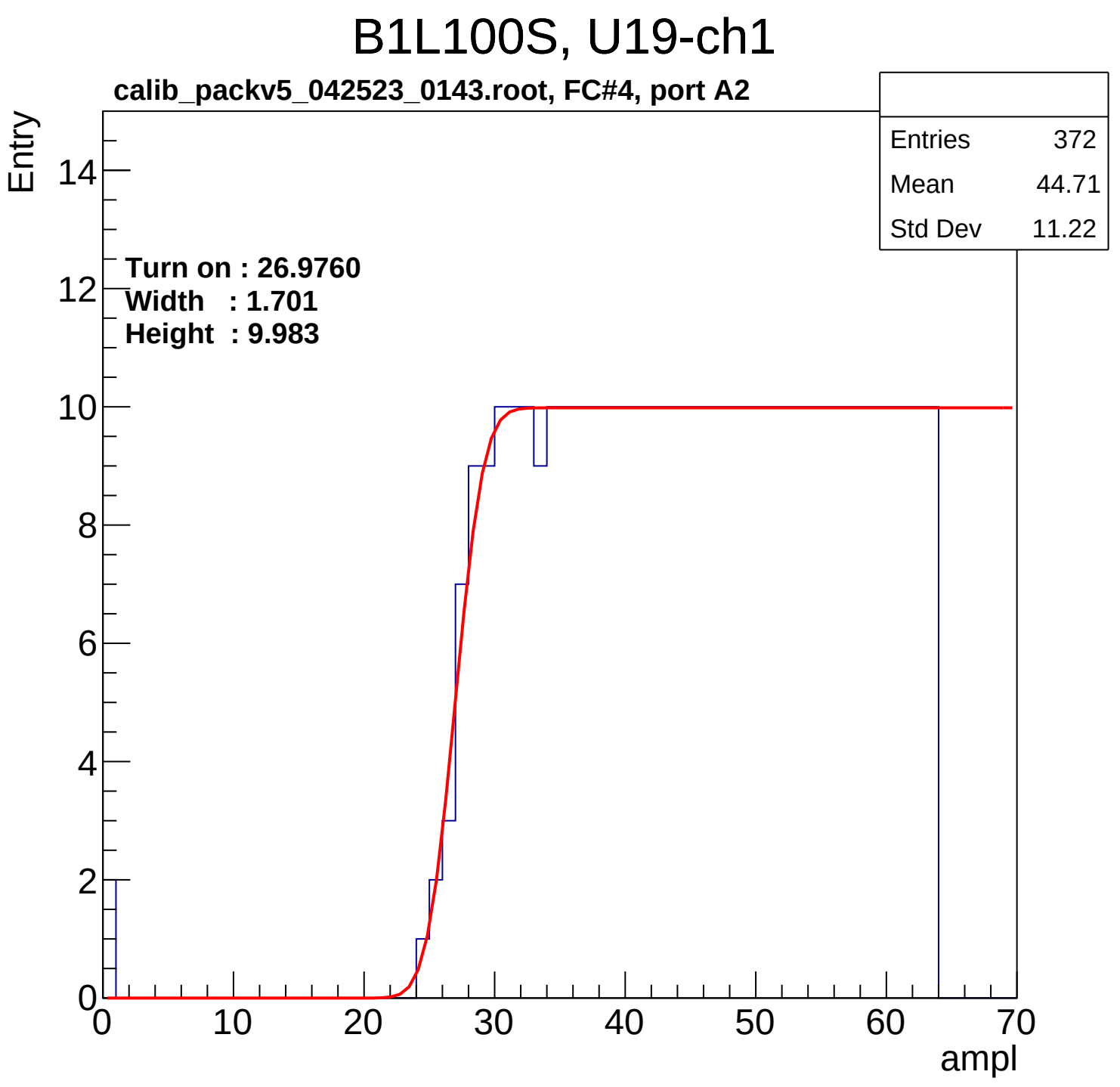
B1L100S, U19-ch1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 372
Mean 44.71
Std Dev 11.22
Turn on : 26.9760
Width : 1.701
Height : 9.983
Entry
ampl
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4
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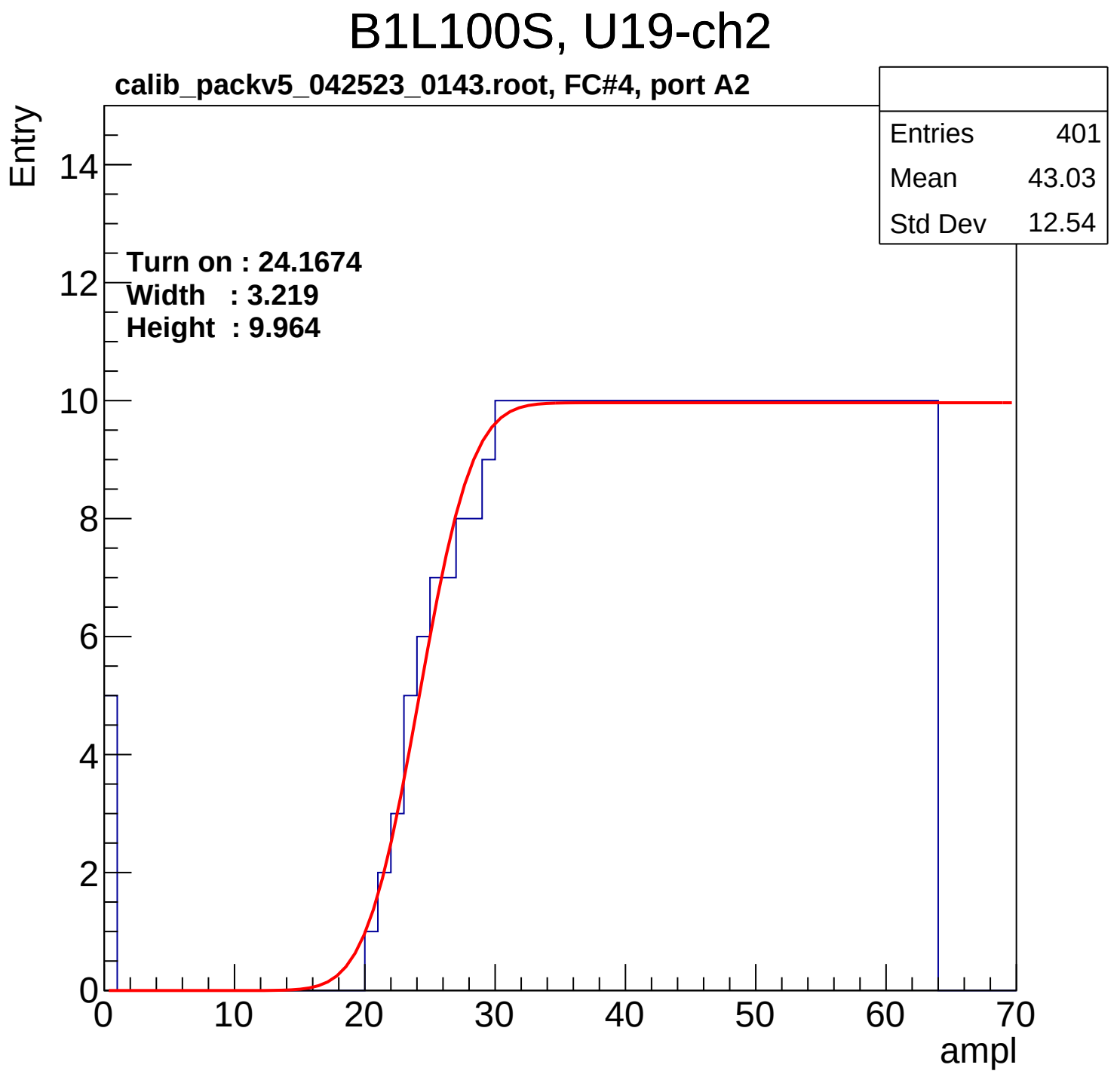
B1L100S, U19-ch2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 401
Mean 43.03
Std Dev 12.54
Turn on : 24.1674
Width : 3.219
Height : 9.964
Entry
ampl
0
2
4
6
8
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0
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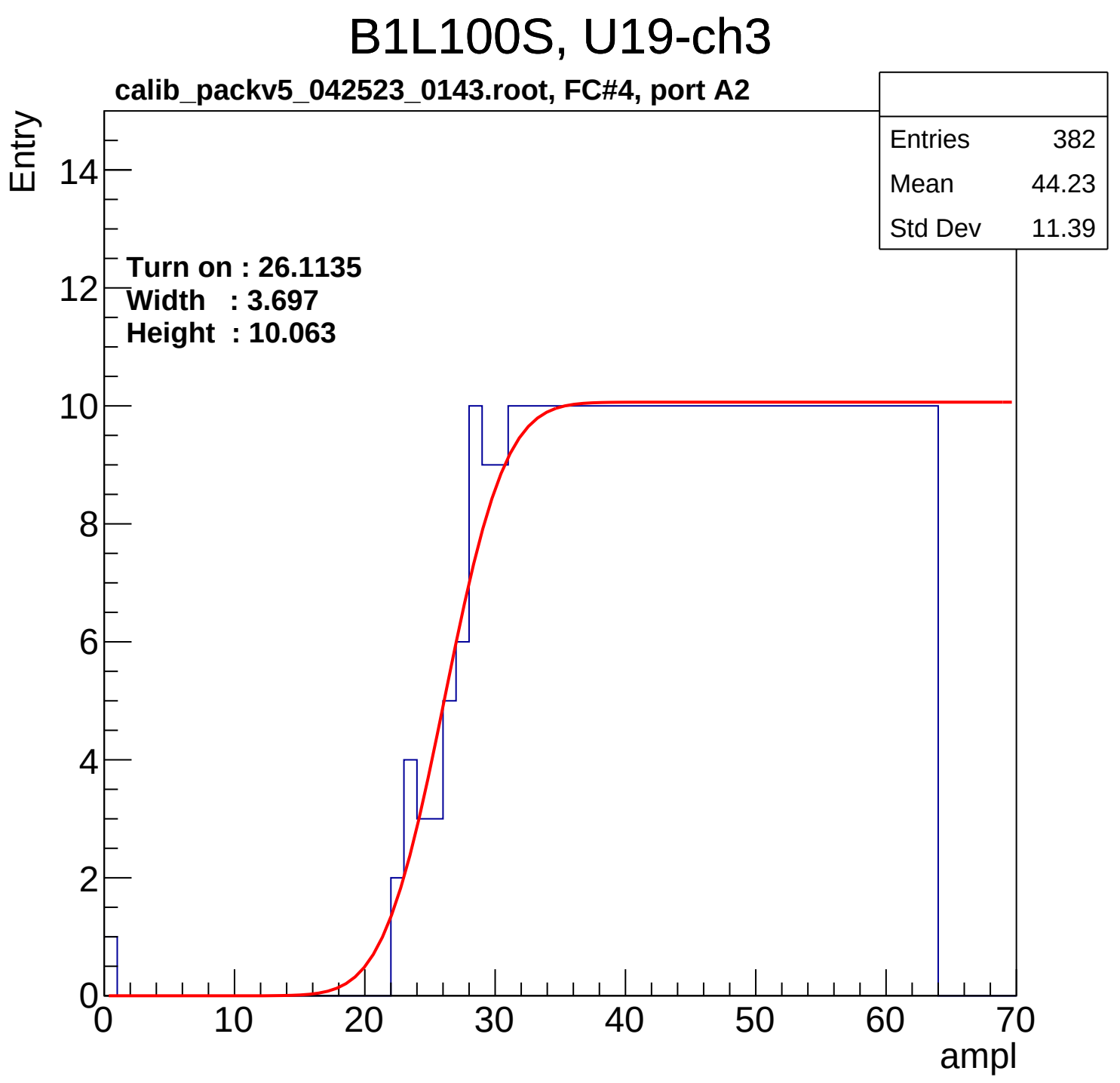
B1L100S, U19-ch3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 382
Mean 44.23
Std Dev 11.39
Turn on : 26.1135
Width : 3.697
Height : 10.063
Entry
ampl
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2
4
6
8
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12
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0
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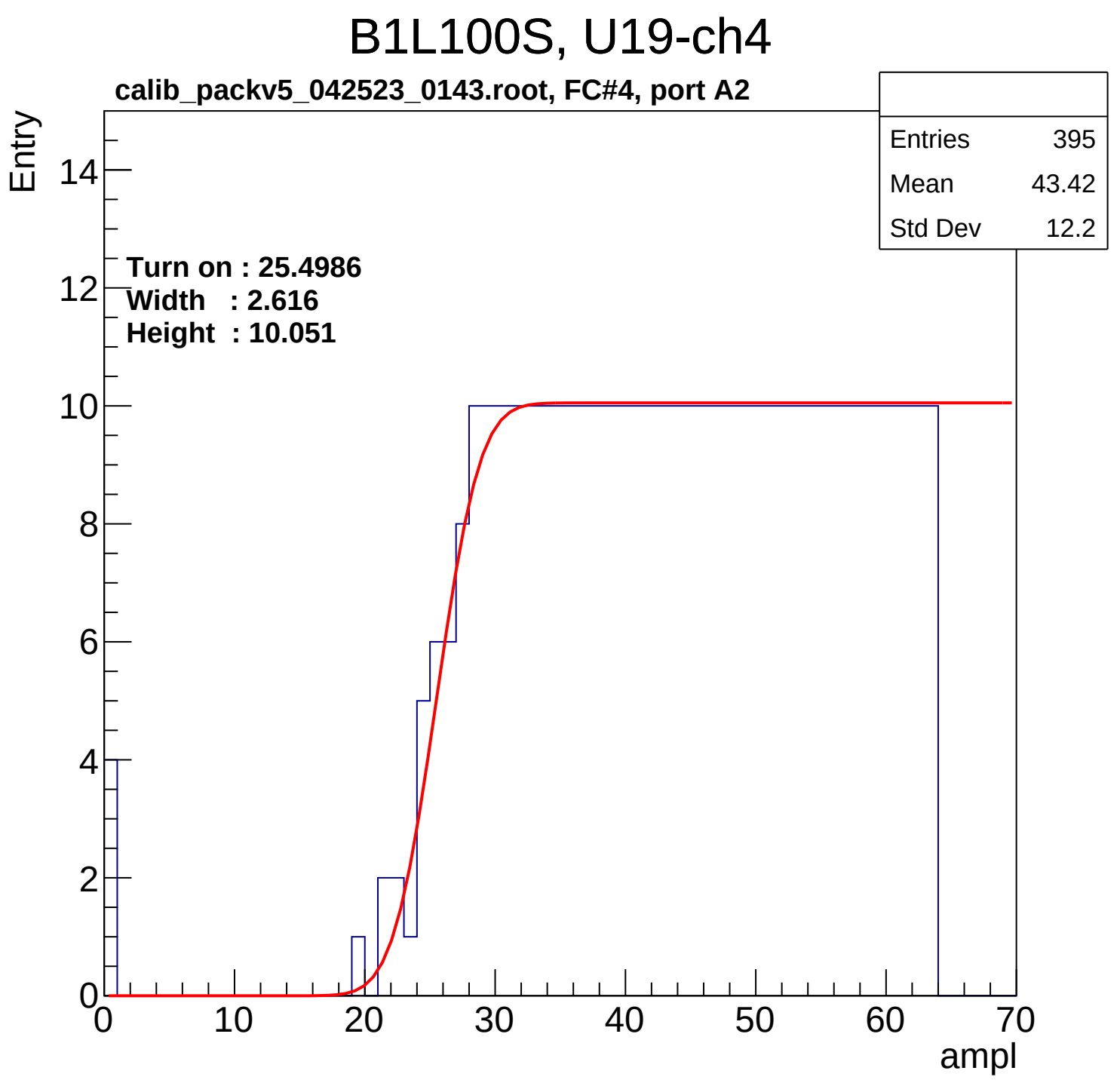
B1L100S, U19-ch4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 395
Mean 43.42
Std Dev 12.2
Turn on : 25.4986
Width : 2.616
Height : 10.051
Entry
ampl
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2
4
6
8
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0
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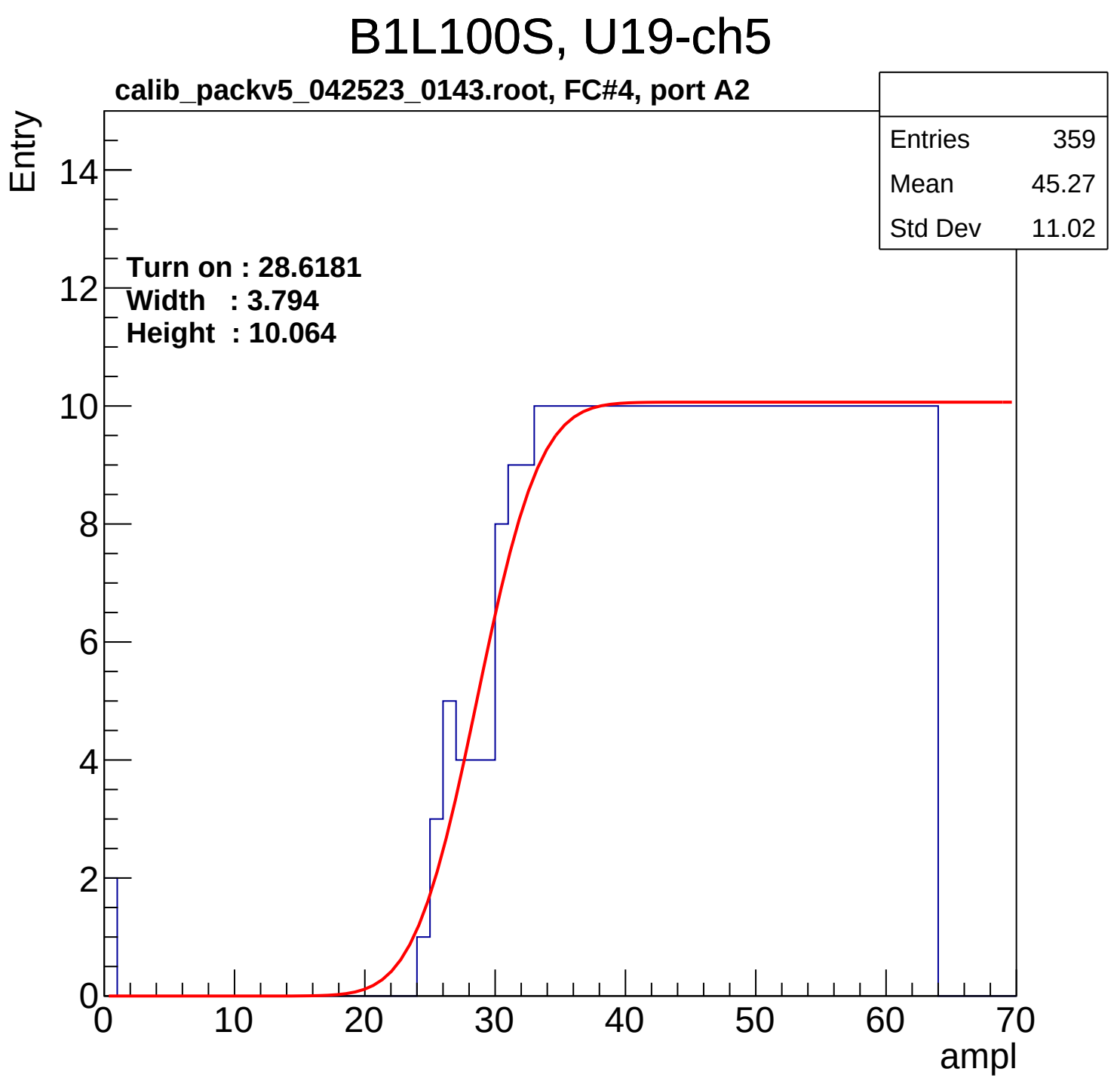
B1L100S, U19-ch5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 359
Mean 45.27
Std Dev 11.02
Turn on : 28.6181
Width : 3.794
Height : 10.064
Entry
ampl
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4
6
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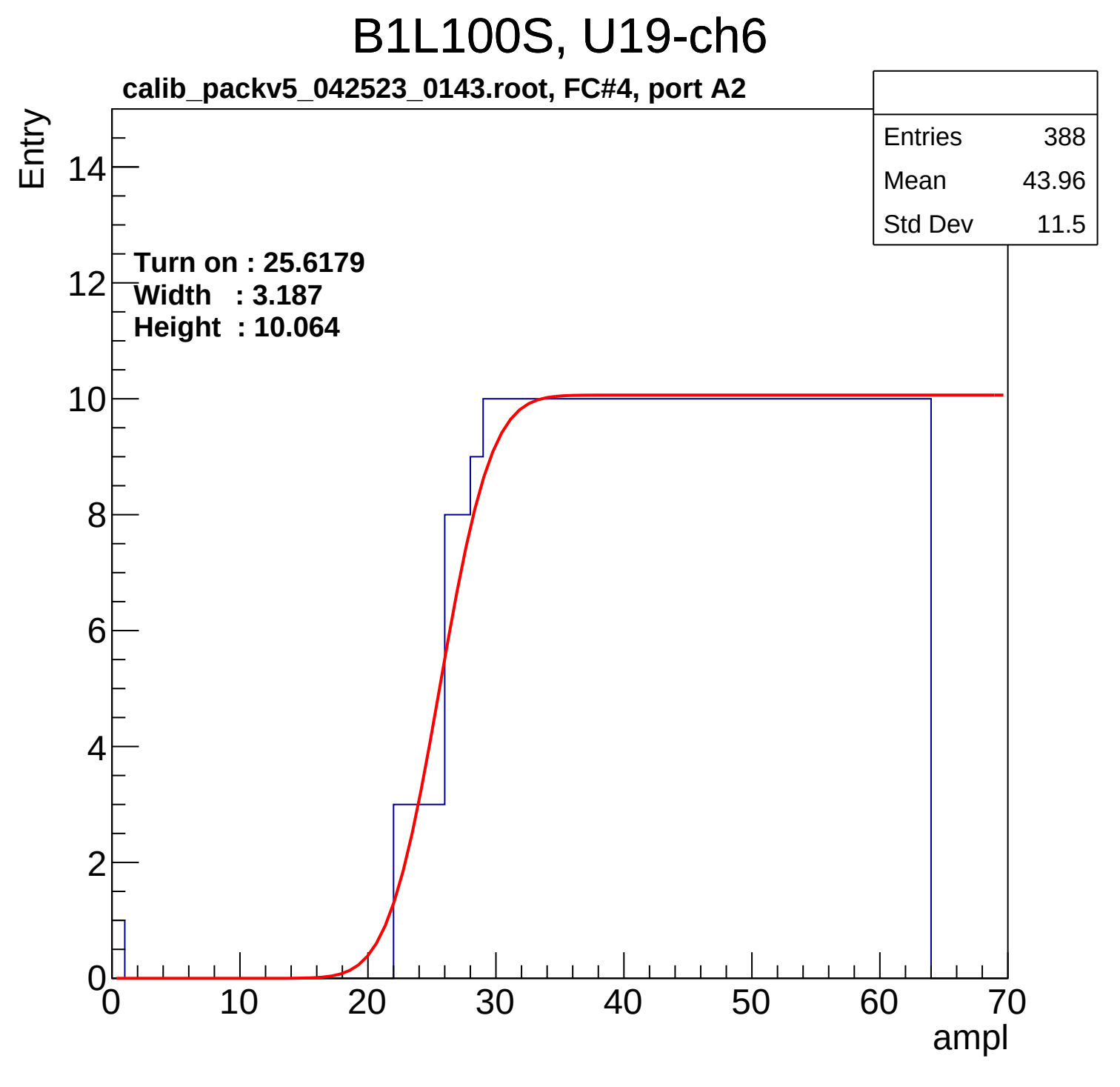
B1L100S, U19-ch6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 388
Mean 43.96
Std Dev 11.5
Turn on : 25.6179
Width : 3.187
Height : 10.064
Entry
ampl
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6
8
10
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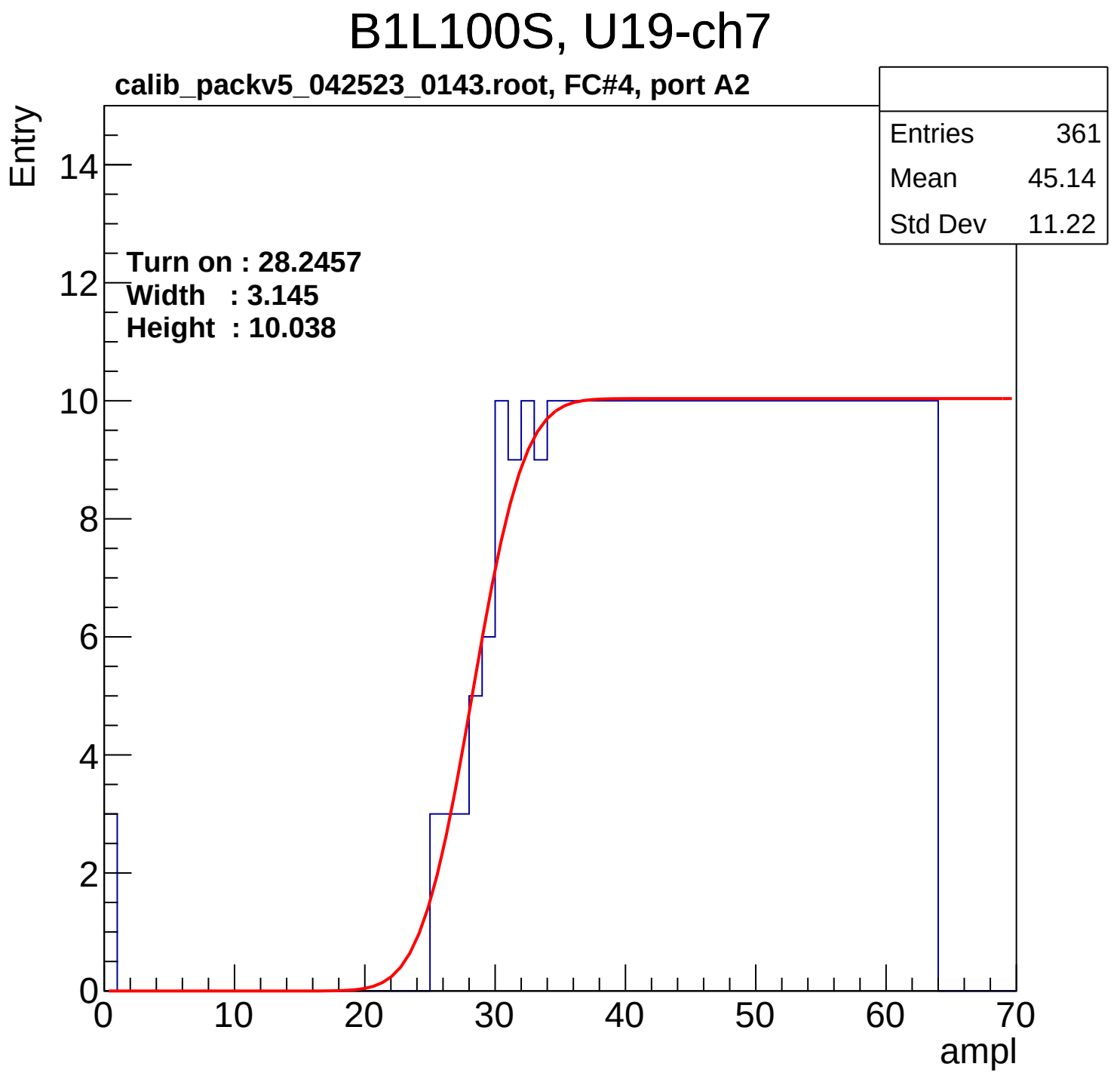
B1L100S, U19-ch7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 361
Mean 45.14
Std Dev 11.22
Turn on : 28.2457
Width : 3.145
Height : 10.038
Entry
ampl
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2
4
6
8
10
12
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0
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40
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60
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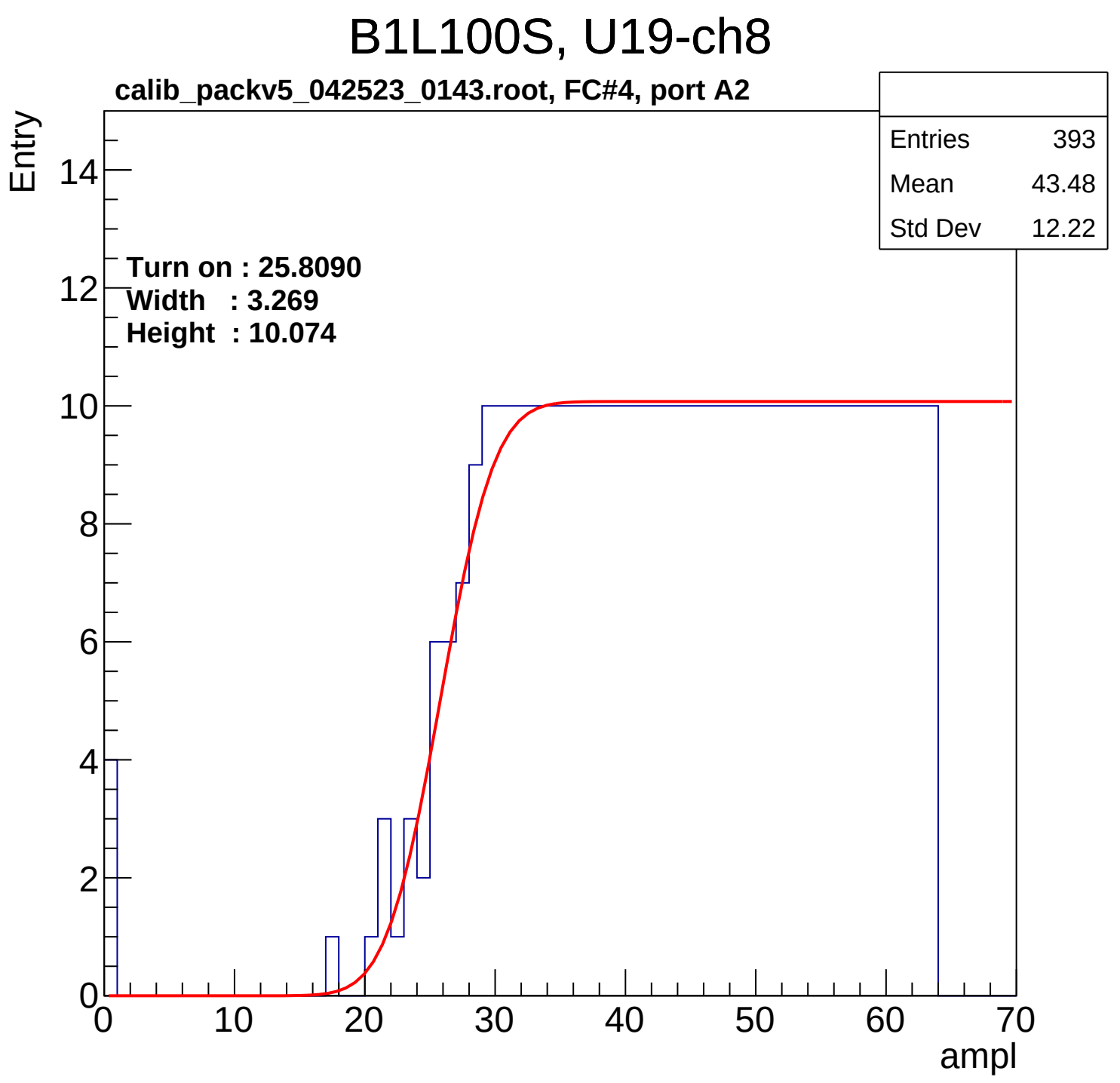
B1L100S, U19-ch8
calib_packv5_042523_0143.root, FC#4, port A2
Entries 393
Mean 43.48
Std Dev 12.22
Turn on : 25.8090
Width : 3.269
Height : 10.074
Entry
ampl
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2
4
6
8
10
12
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0
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20
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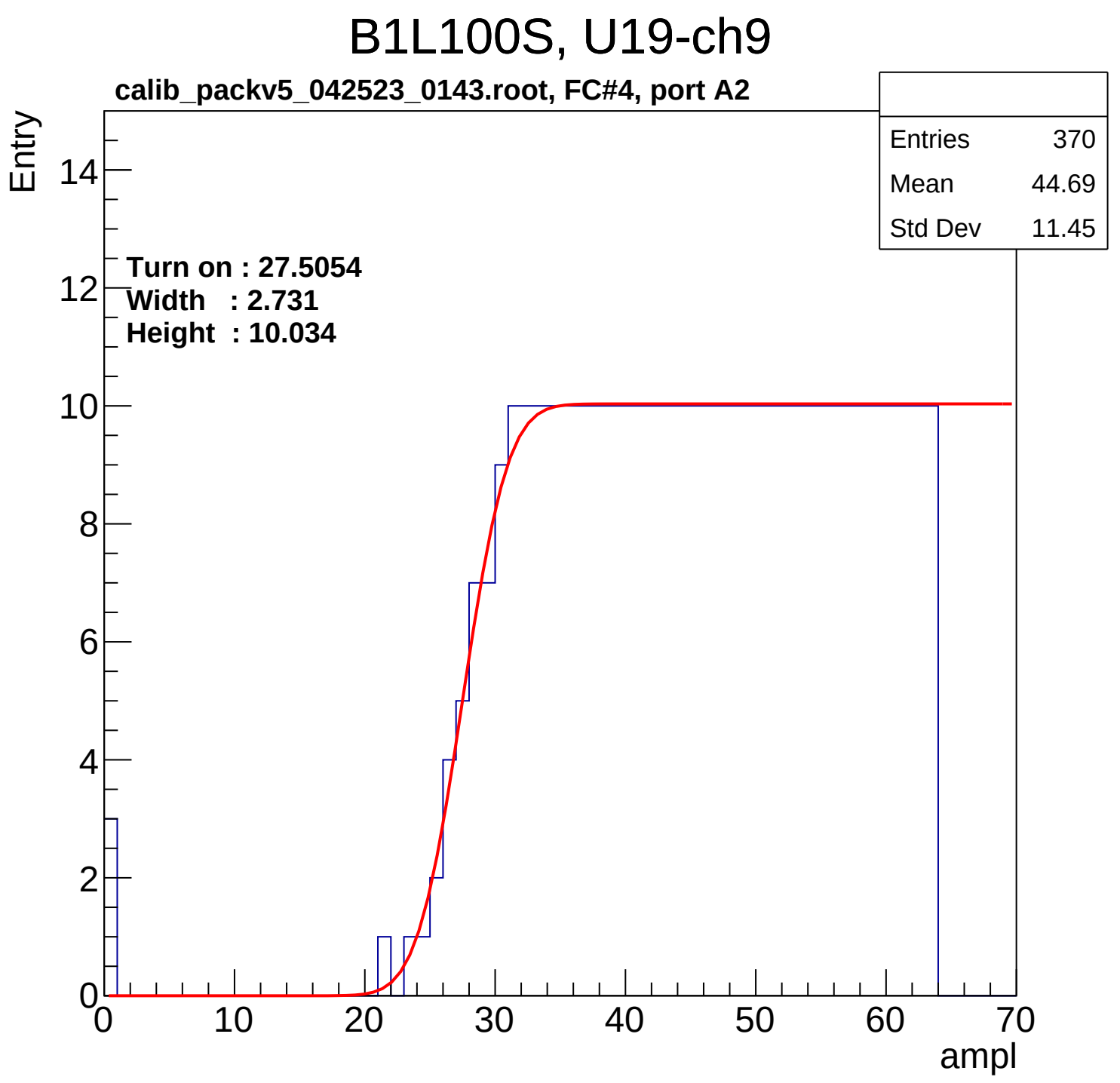
B1L100S, U19-ch9
calib_packv5_042523_0143.root, FC#4, port A2
Entries 370
Mean 44.69
Std Dev 11.45
Turn on : 27.5054
Width : 2.731
Height : 10.034
Entry
ampl
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2
4
6
8
10
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0
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60
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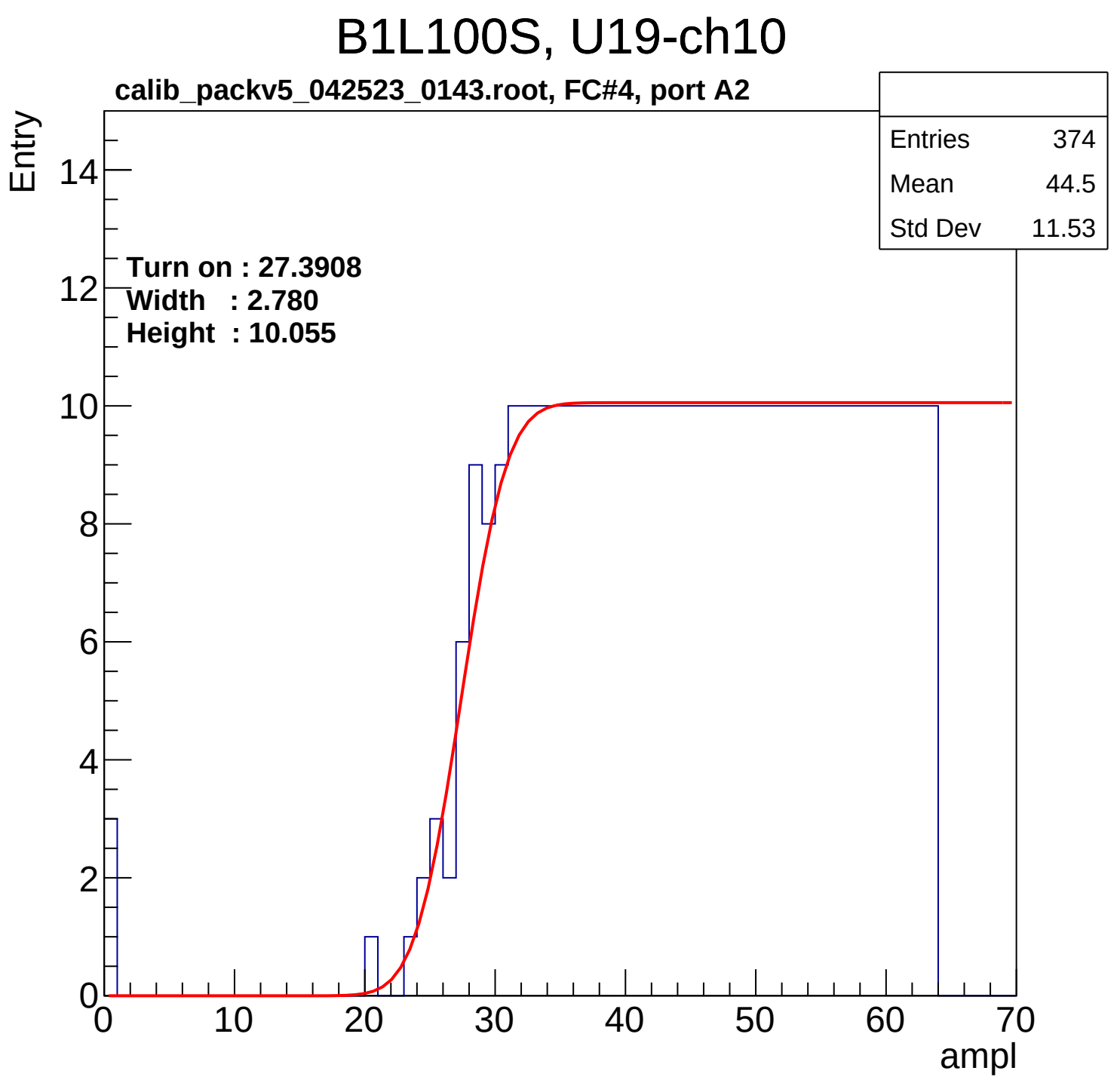
B1L100S, U19-ch10
calib_packv5_042523_0143.root, FC#4, port A2
Entries 374
Mean 44.5
Std Dev 11.53
Turn on : 27.3908
Width : 2.780
Height : 10.055
Entry
ampl
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2
4
6
8
10
12
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0
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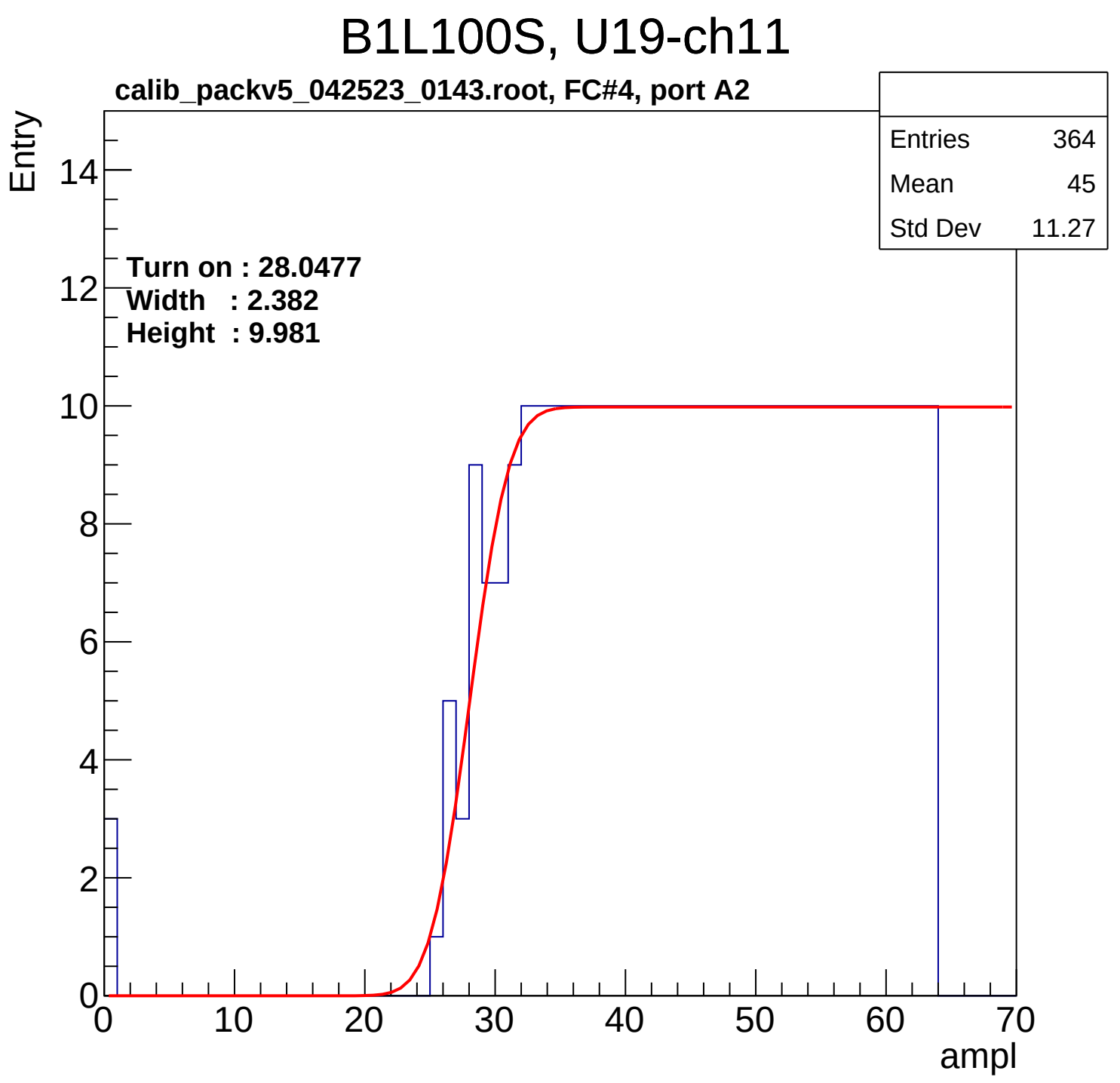
B1L100S, U19-ch11
calib_packv5_042523_0143.root, FC#4, port A2
Entries 364
Mean 45
Std Dev 11.27
Turn on : 28.0477
Width : 2.382
Height : 9.981
Entry
ampl
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6
8
10
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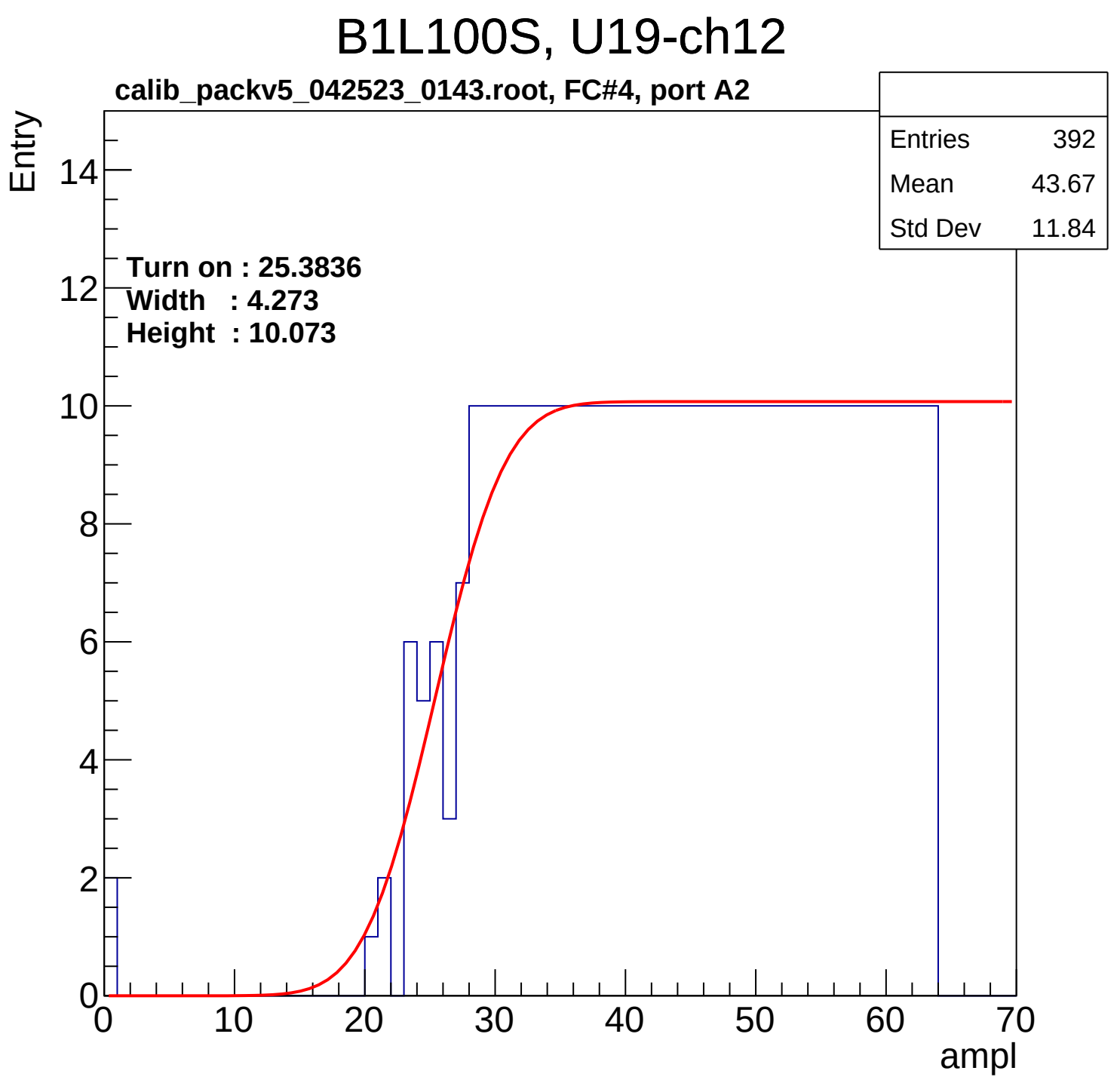
B1L100S, U19-ch12
calib_packv5_042523_0143.root, FC#4, port A2
Entries 392
Mean 43.67
Std Dev 11.84
Turn on : 25.3836
Width : 4.273
Height : 10.073
Entry
ampl
0
2
4
6
8
10
12
14
0
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20
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60
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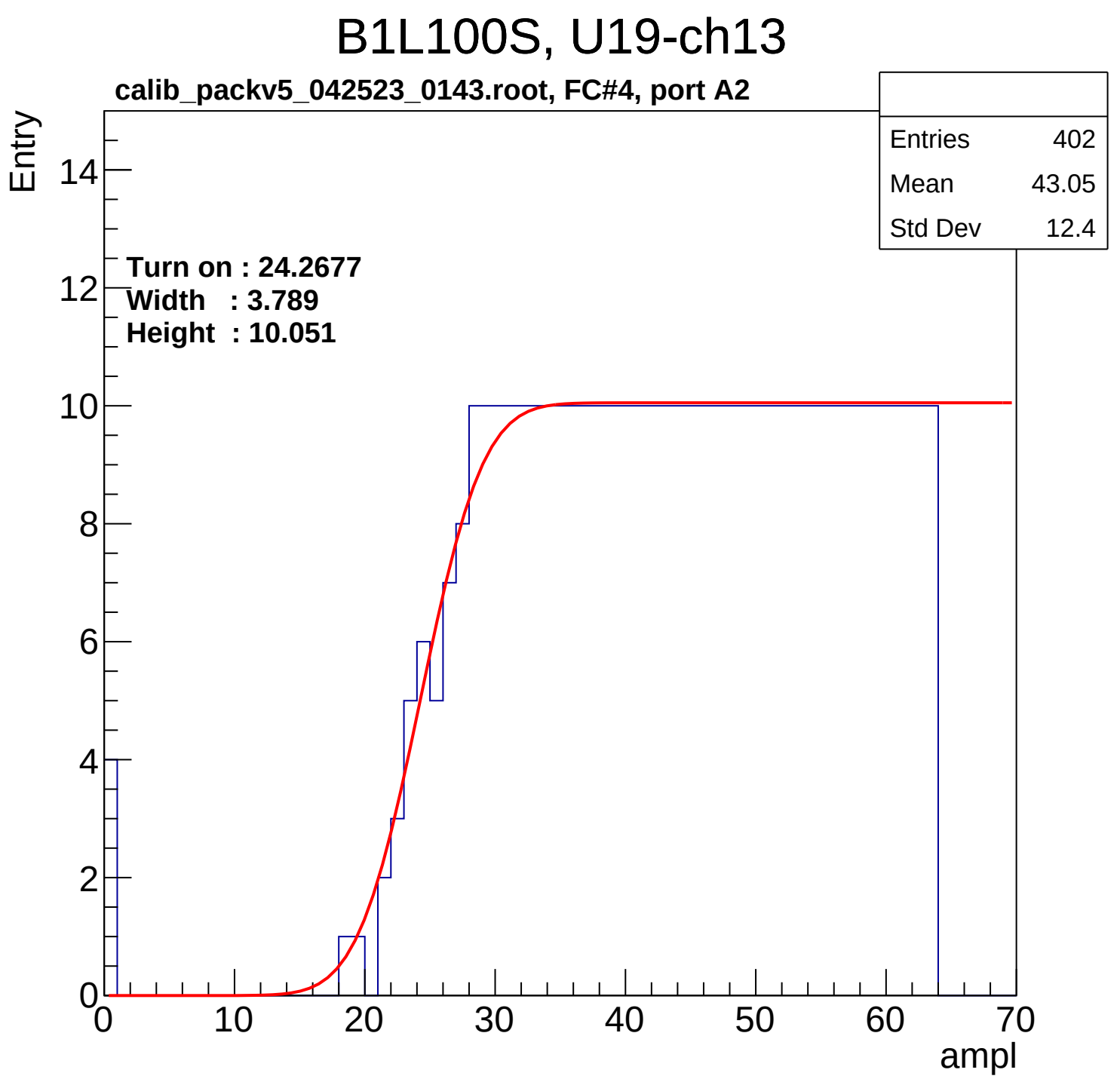
B1L100S, U19-ch13
calib_packv5_042523_0143.root, FC#4, port A2
Entries 402
Mean 43.05
Std Dev 12.4
Turn on : 24.2677
Width : 3.789
Height : 10.051
Entry
ampl
0
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4
6
8
10
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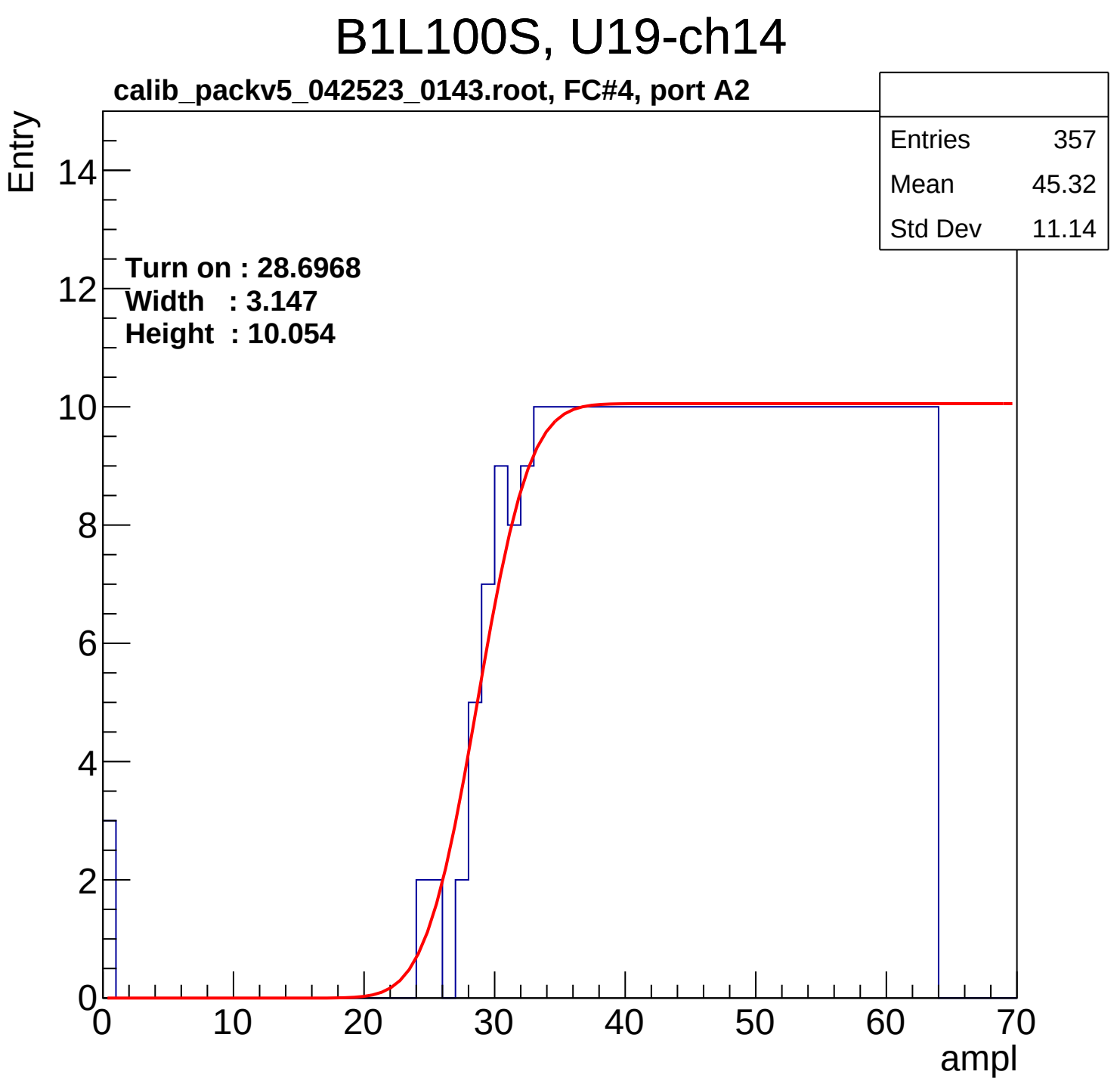
B1L100S, U19-ch14
calib_packv5_042523_0143.root, FC#4, port A2
Entries 357
Mean 45.32
Std Dev 11.14
Turn on : 28.6968
Width : 3.147
Height : 10.054
Entry
ampl
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6
8
10
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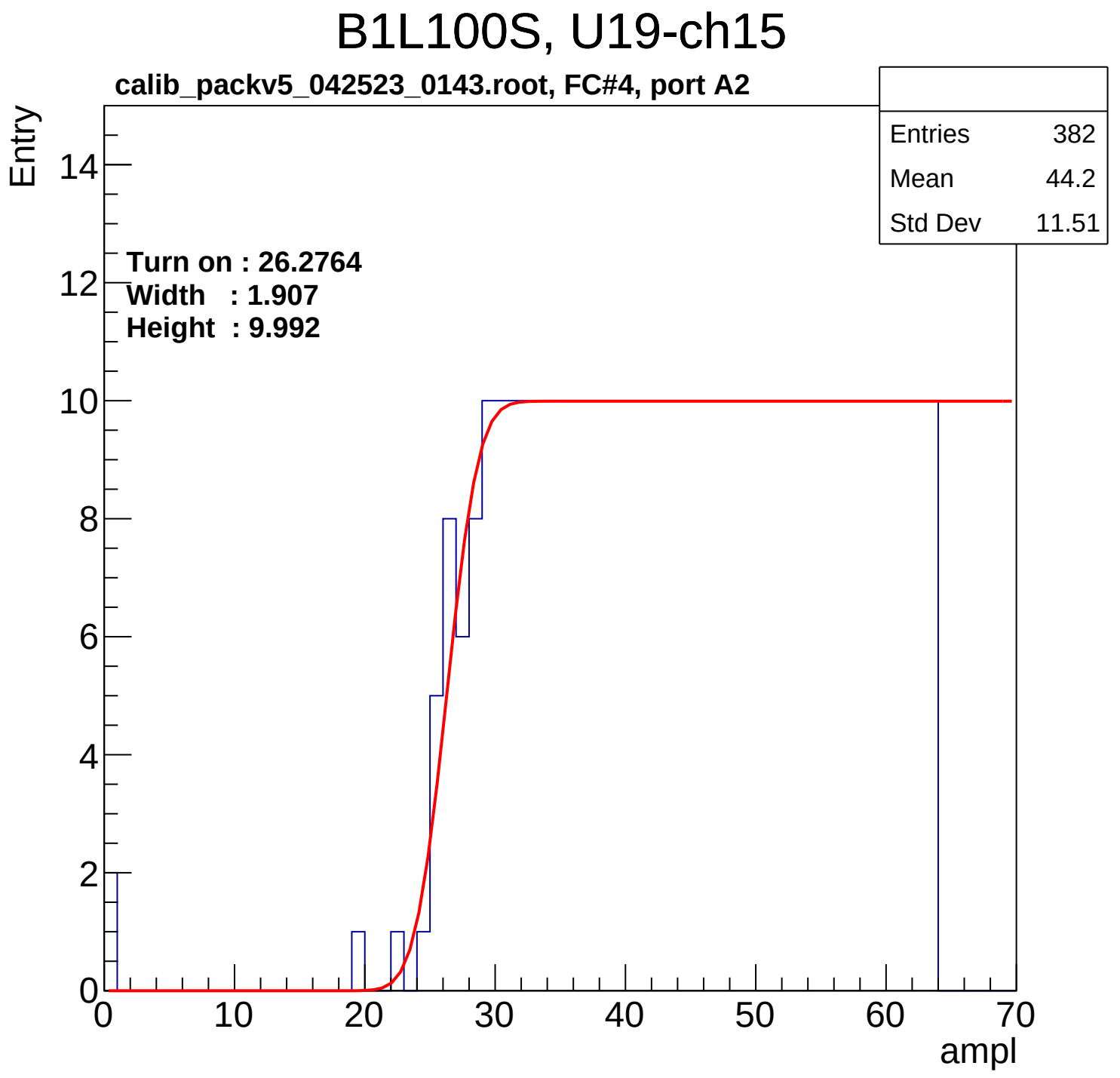
B1L100S, U19-ch15
calib_packv5_042523_0143.root, FC#4, port A2
Entries 382
Mean 44.2
Std Dev 11.51
Turn on : 26.2764
Width : 1.907
Height : 9.992
Entry
ampl
0
2
4
6
8
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0
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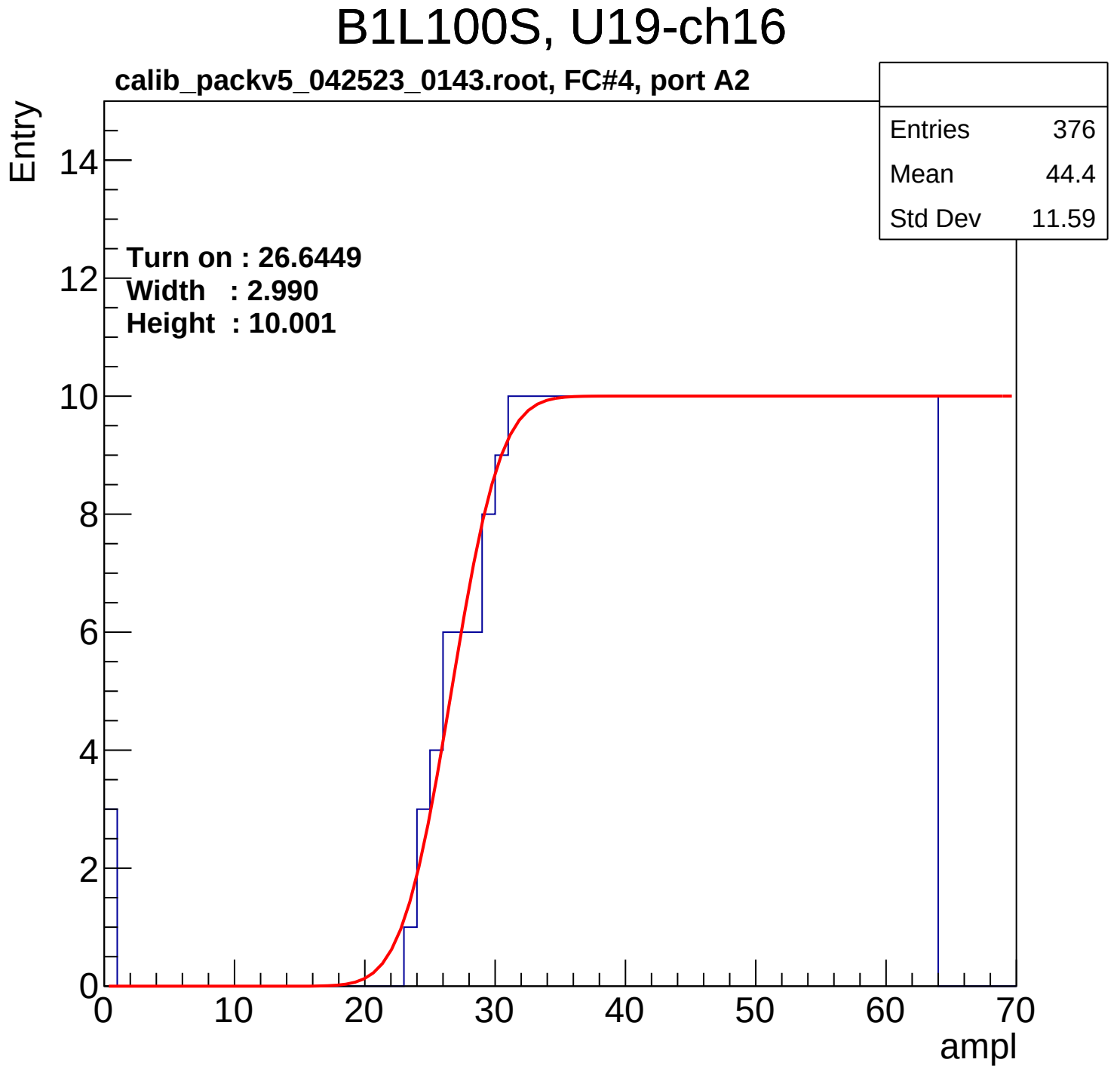
B1L100S, U19-ch16
calib_packv5_042523_0143.root, FC#4, port A2
Entries 376
Mean 44.4
Std Dev 11.59
Turn on : 26.6449
Width : 2.990
Height : 10.001
Entry
ampl
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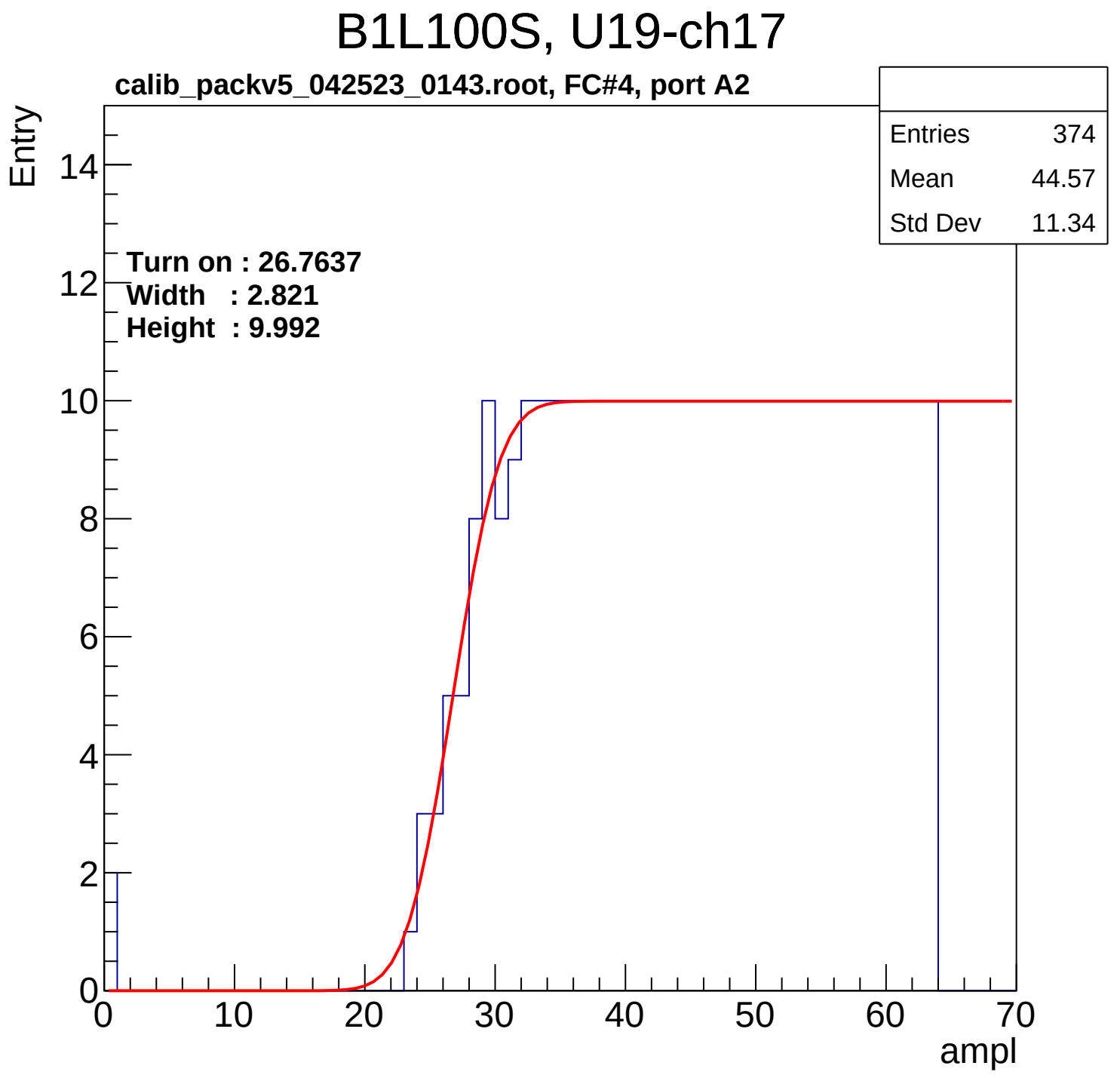
B1L100S, U19-ch17
calib_packv5_042523_0143.root, FC#4, port A2
Entries 374
Mean 44.57
Std Dev 11.34
Turn on : 26.7637
Width : 2.821
Height : 9.992
Entry
ampl
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6
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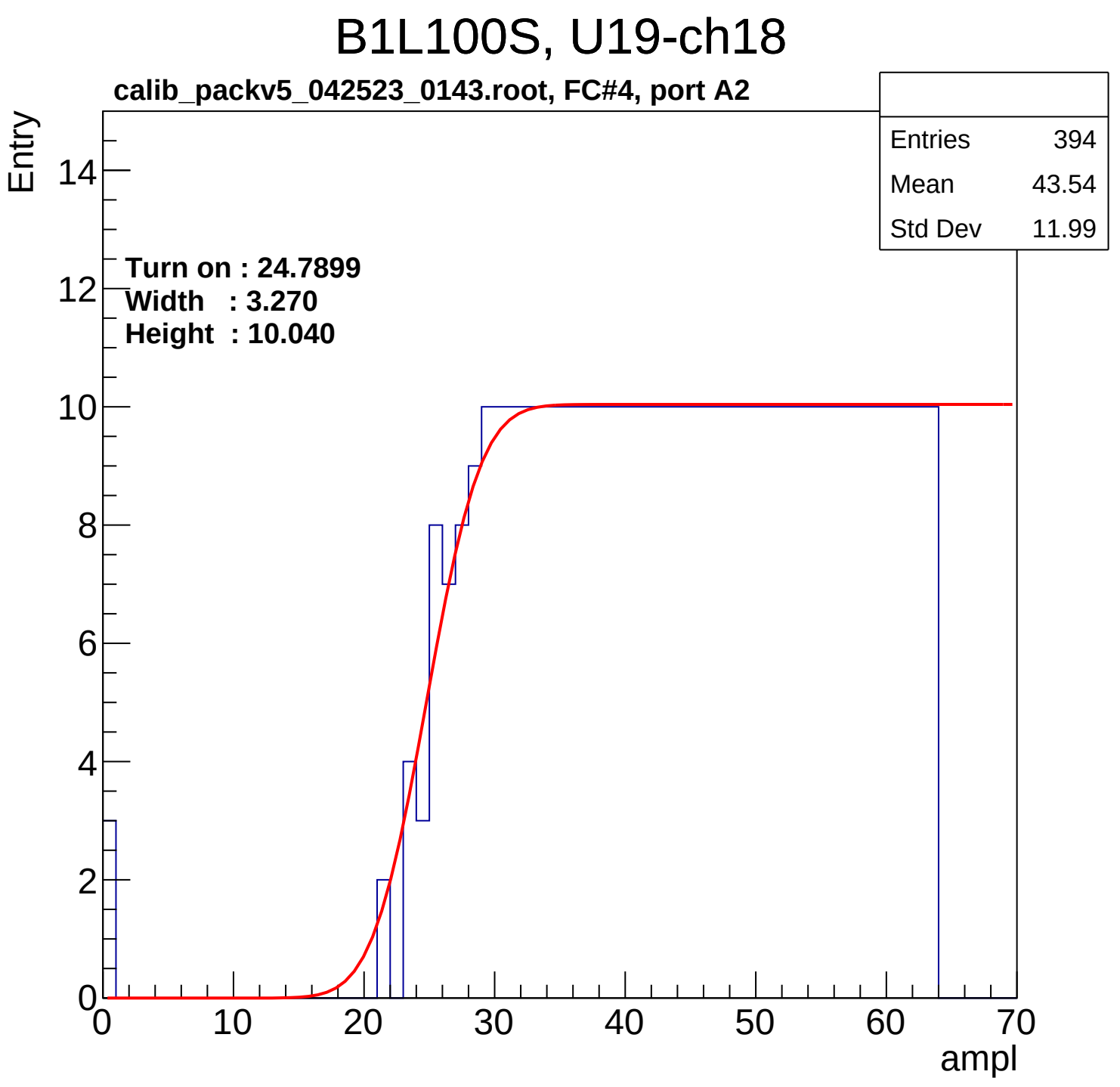
B1L100S, U19-ch18
calib_packv5_042523_0143.root, FC#4, port A2
Entries 394
Mean 43.54
Std Dev 11.99
Turn on : 24.7899
Width : 3.270
Height : 10.040
Entry
ampl
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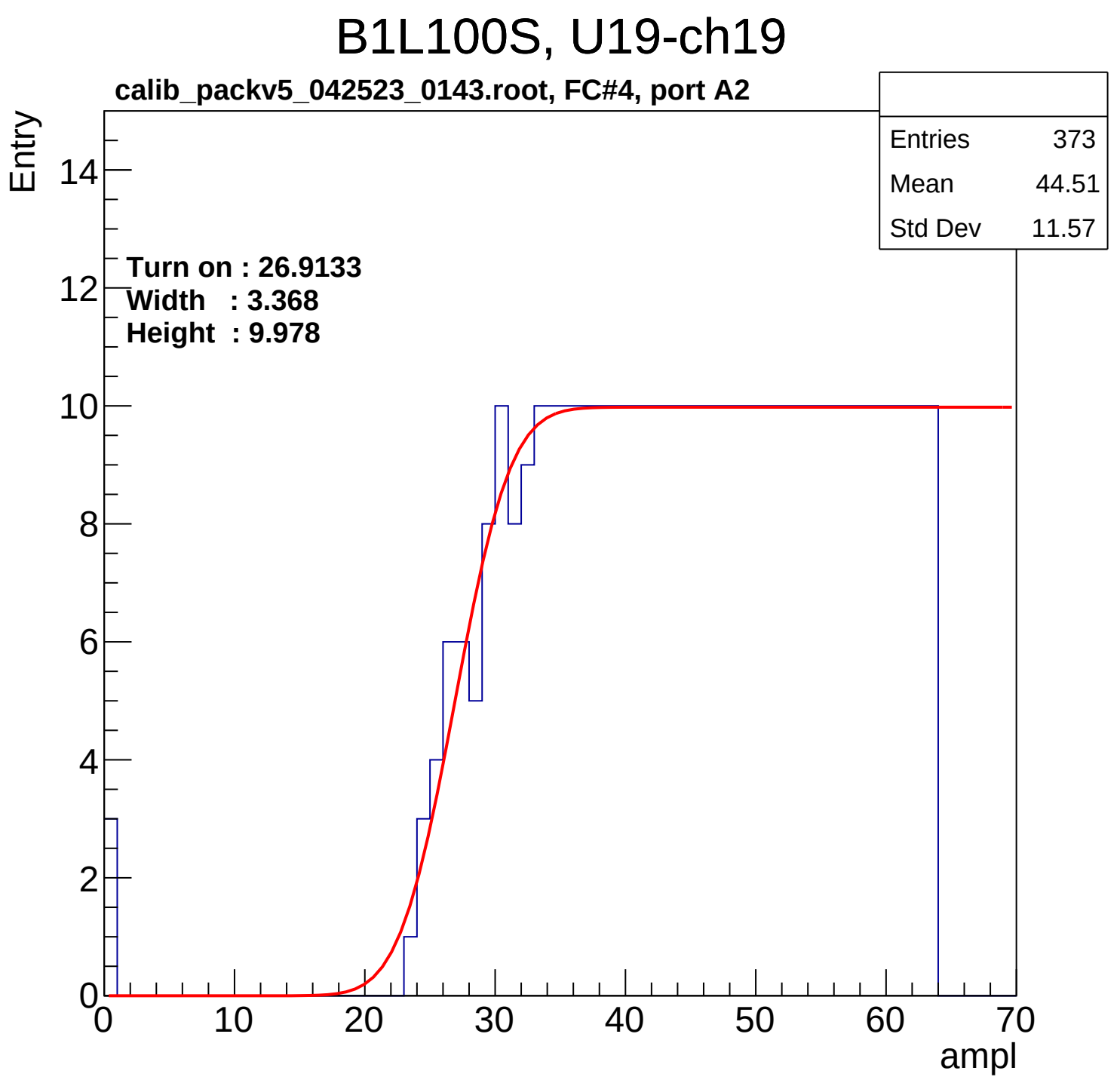
B1L100S, U19-ch19
calib_packv5_042523_0143.root, FC#4, port A2
Entries 373
Mean 44.51
Std Dev 11.57
Turn on : 26.9133
Width : 3.368
Height : 9.978
Entry
ampl
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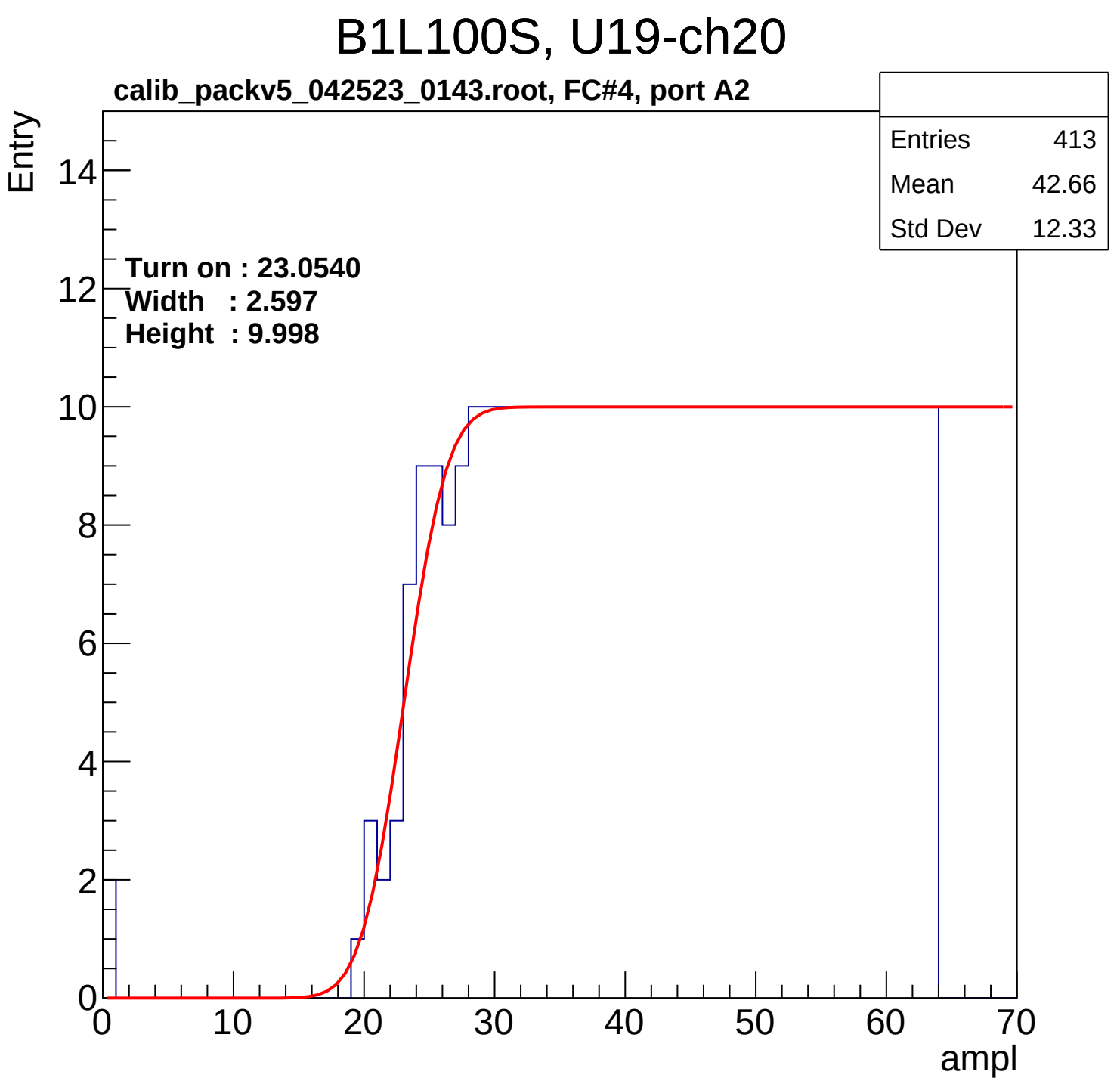
B1L100S, U19-ch20
calib_packv5_042523_0143.root, FC#4, port A2
Entries 413
Mean 42.66
Std Dev 12.33
Turn on : 23.0540
Width : 2.597
Height : 9.998
Entry
ampl
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2
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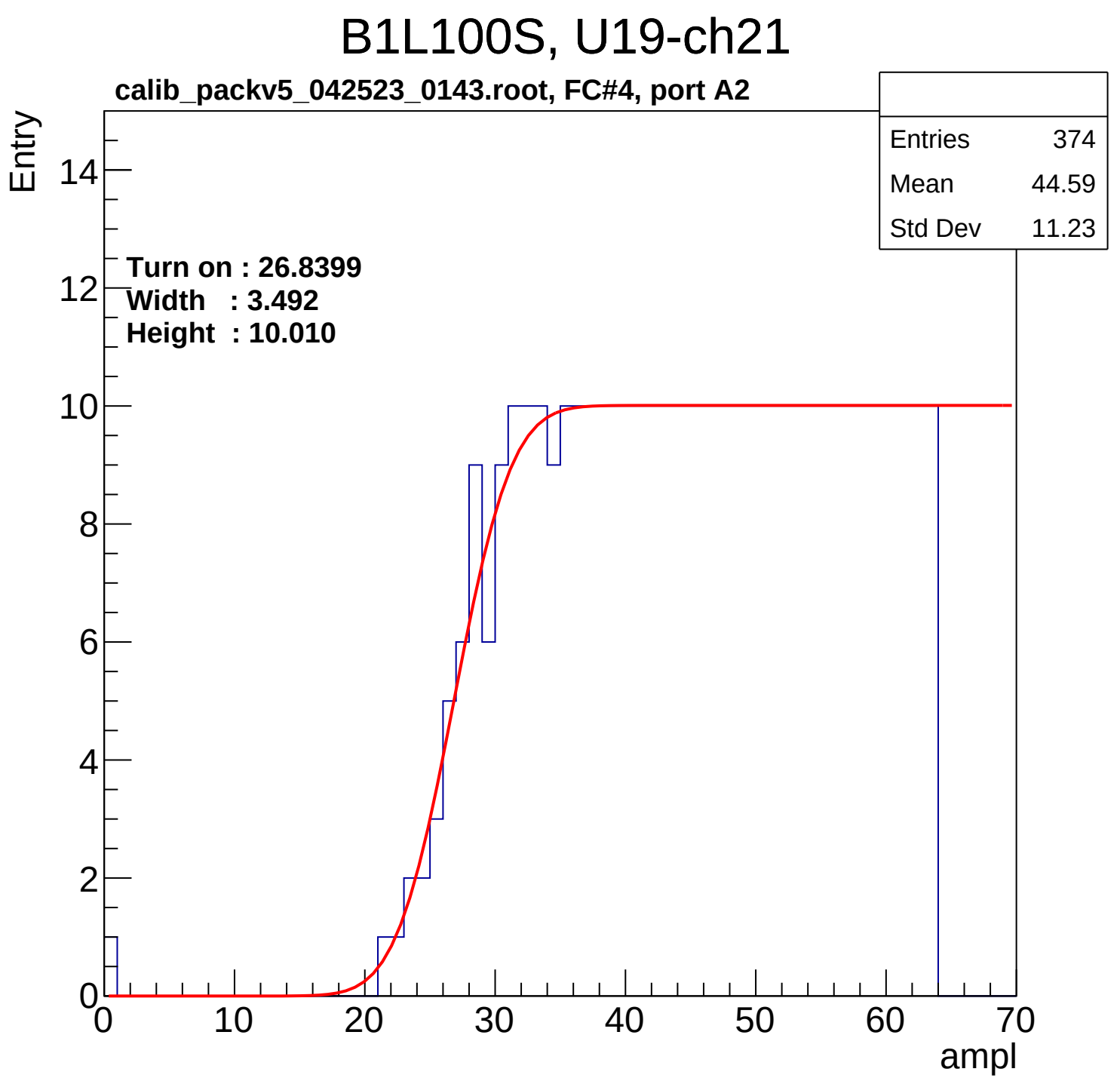
B1L100S, U19-ch21
calib_packv5_042523_0143.root, FC#4, port A2
Entries 374
Mean 44.59
Std Dev 11.23
Turn on : 26.8399
Width : 3.492
Height : 10.010
Entry
ampl
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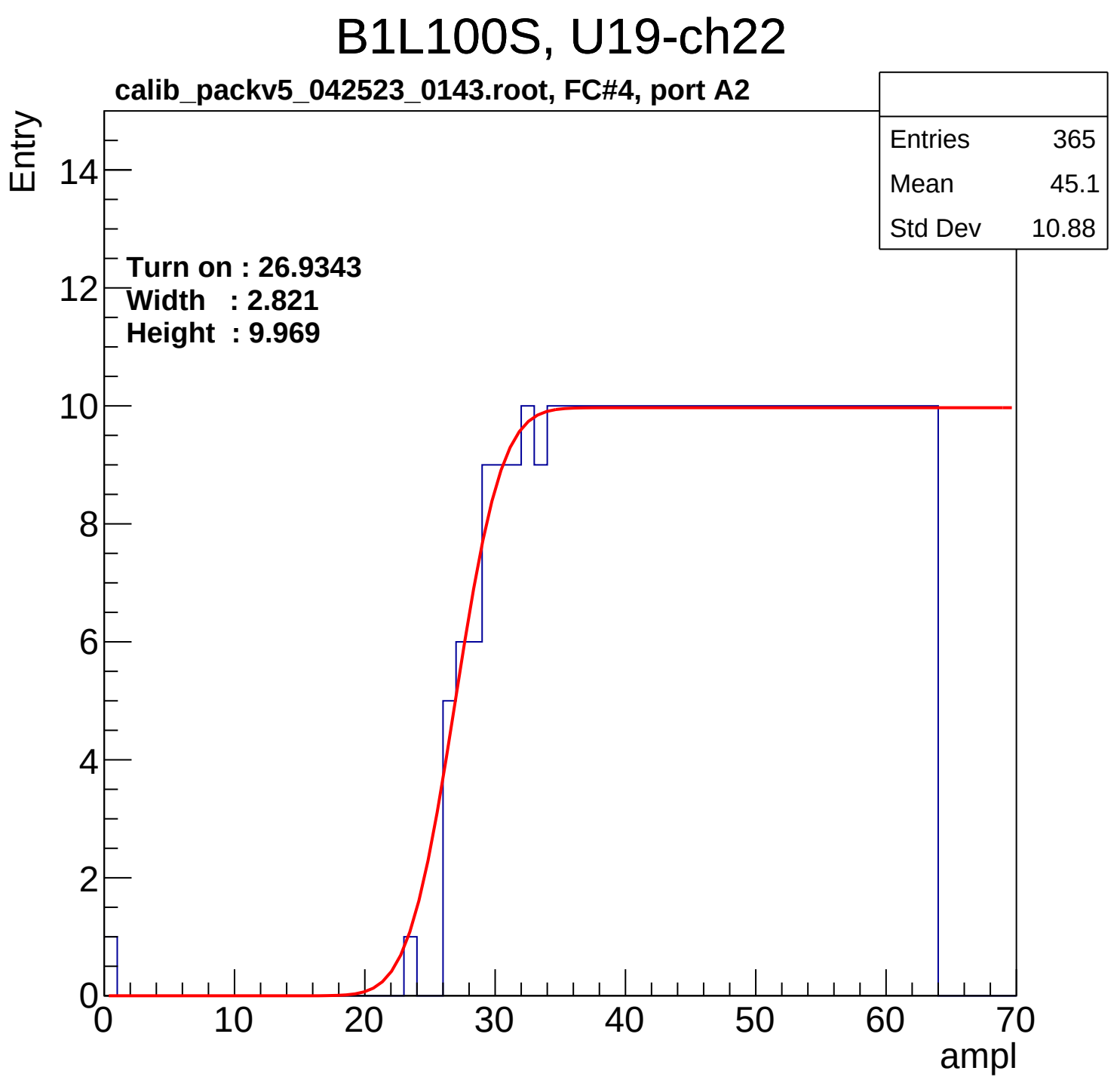
B1L100S, U19-ch22
calib_packv5_042523_0143.root, FC#4, port A2
Entries 365
Mean 45.1
Std Dev 10.88
Turn on : 26.9343
Width : 2.821
Height : 9.969
Entry
ampl
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2
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6
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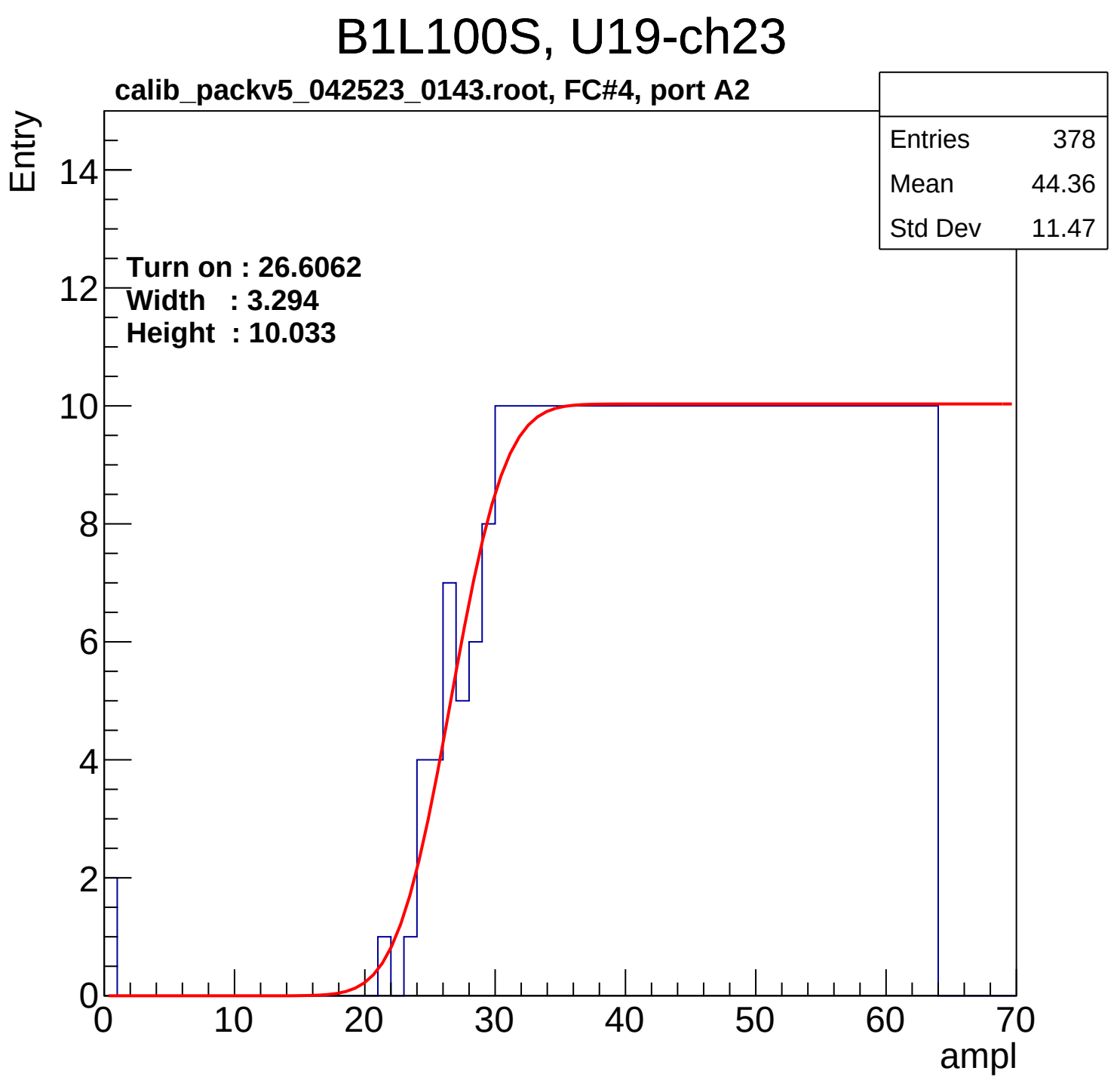
B1L100S, U19-ch23
calib_packv5_042523_0143.root, FC#4, port A2
Entries 378
Mean 44.36
Std Dev 11.47
Turn on : 26.6062
Width : 3.294
Height : 10.033
Entry
ampl
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2
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6
8
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60
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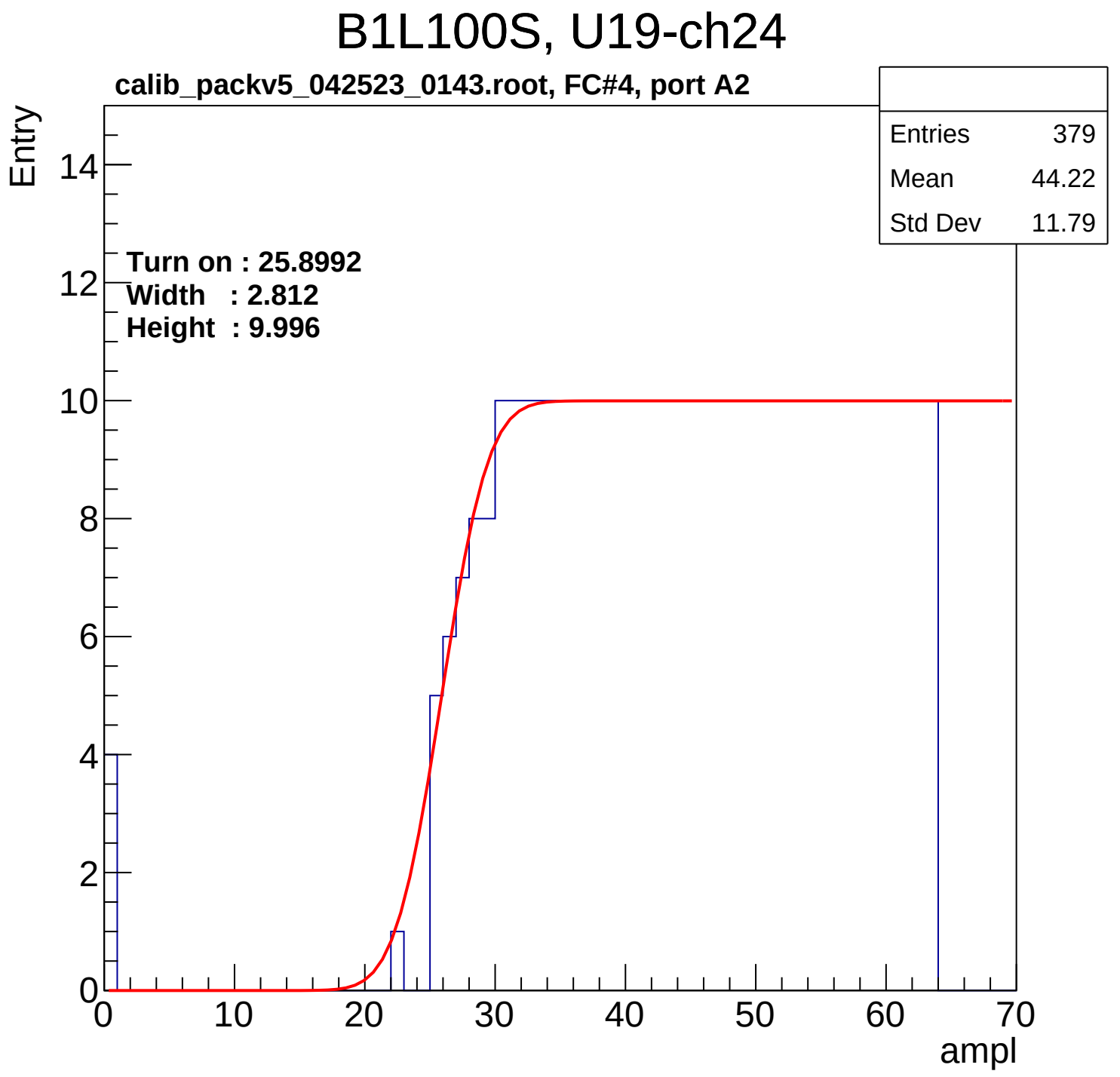
B1L100S, U19-ch24
calib_packv5_042523_0143.root, FC#4, port A2
Entries 379
Mean 44.22
Std Dev 11.79
Turn on : 25.8992
Width : 2.812
Height : 9.996
Entry
ampl
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6
8
10
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0
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60
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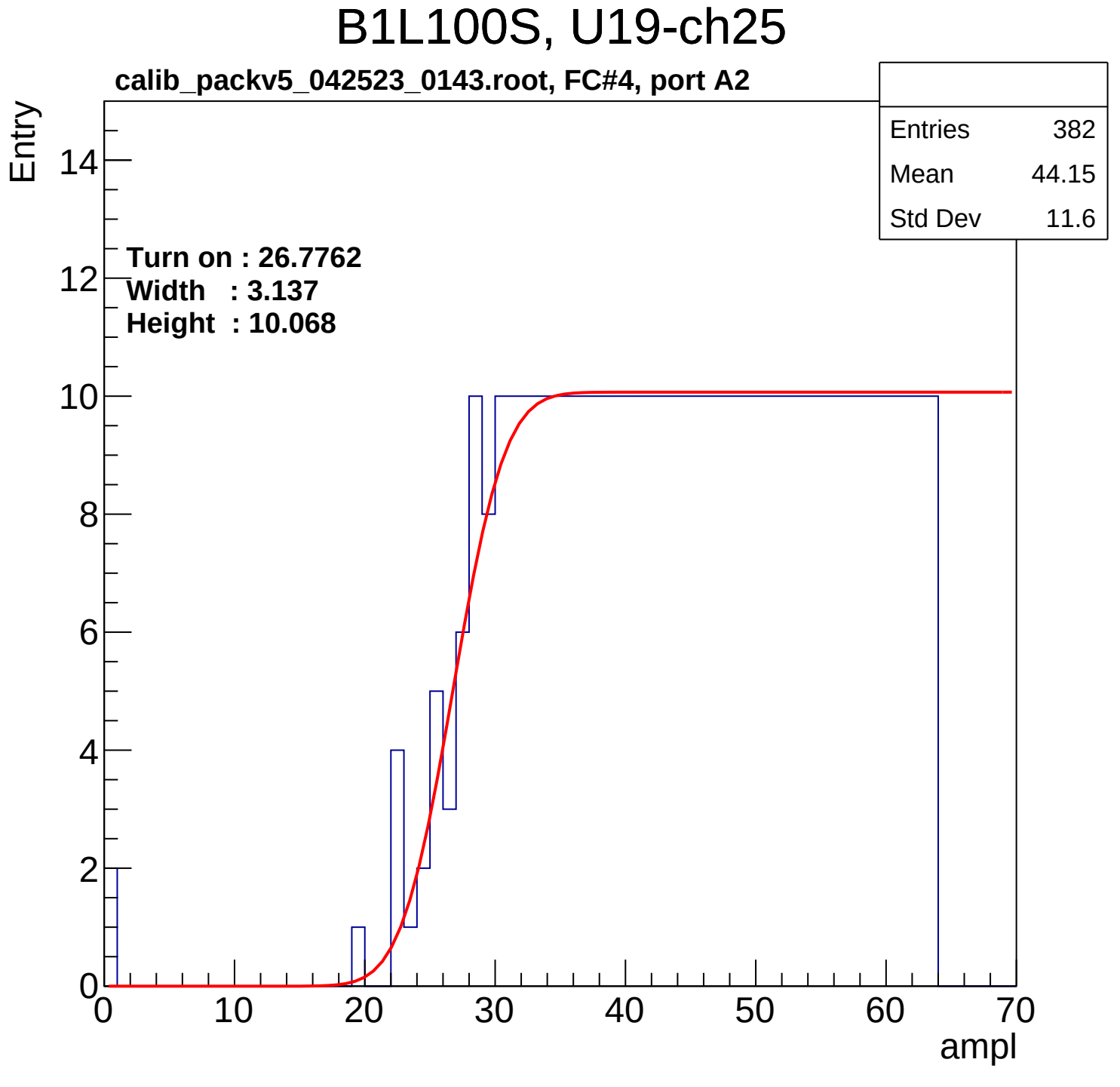
B1L100S, U19-ch25
calib_packv5_042523_0143.root, FC#4, port A2
Entries 382
Mean 44.15
Std Dev 11.6
Turn on : 26.7762
Width : 3.137
Height : 10.068
Entry
ampl
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6
8
10
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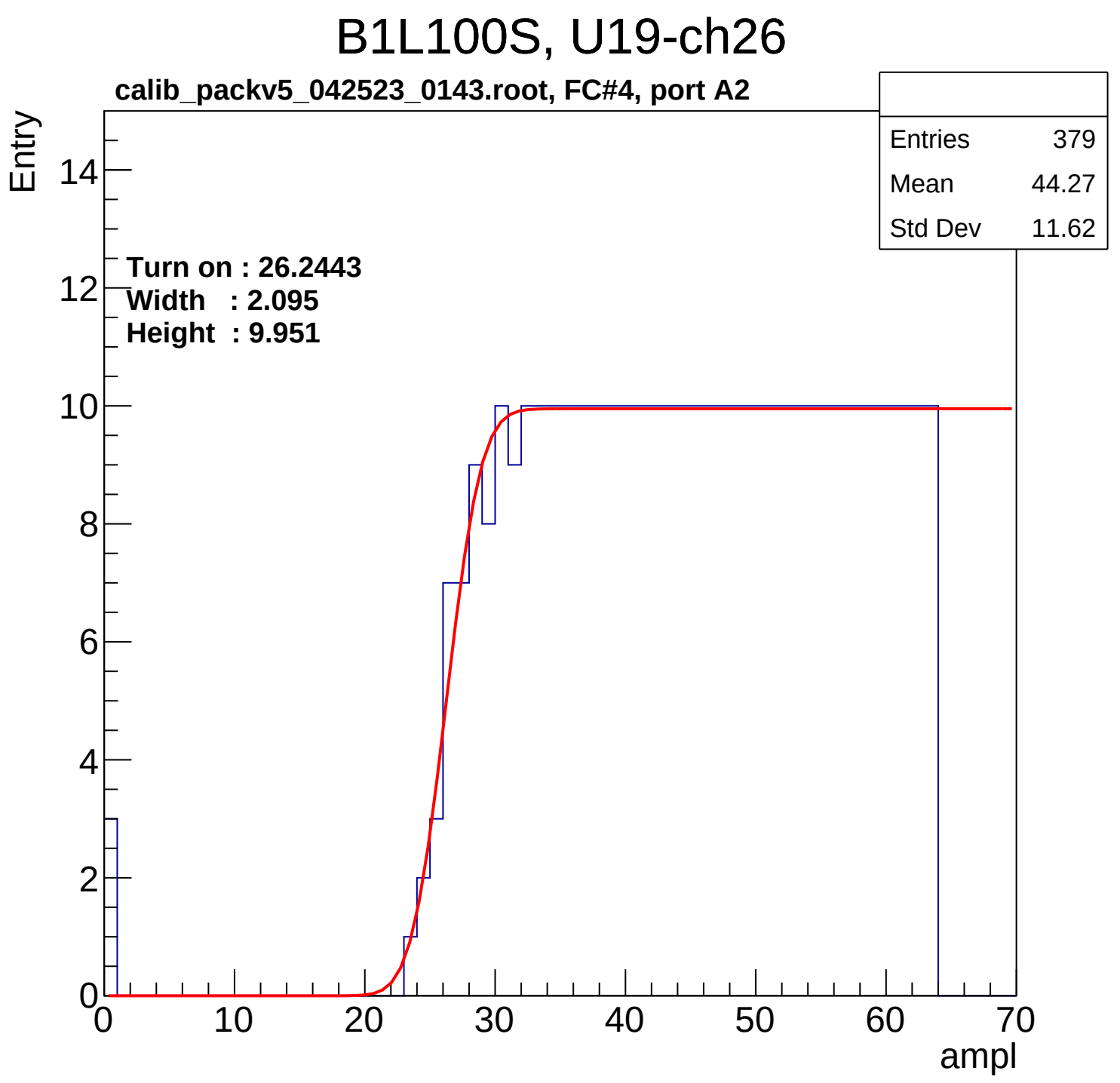
B1L100S, U19-ch26
calib_packv5_042523_0143.root, FC#4, port A2
Entries 379
Mean 44.27
Std Dev 11.62
Turn on : 26.2443
Width : 2.095
Height : 9.951
Entry
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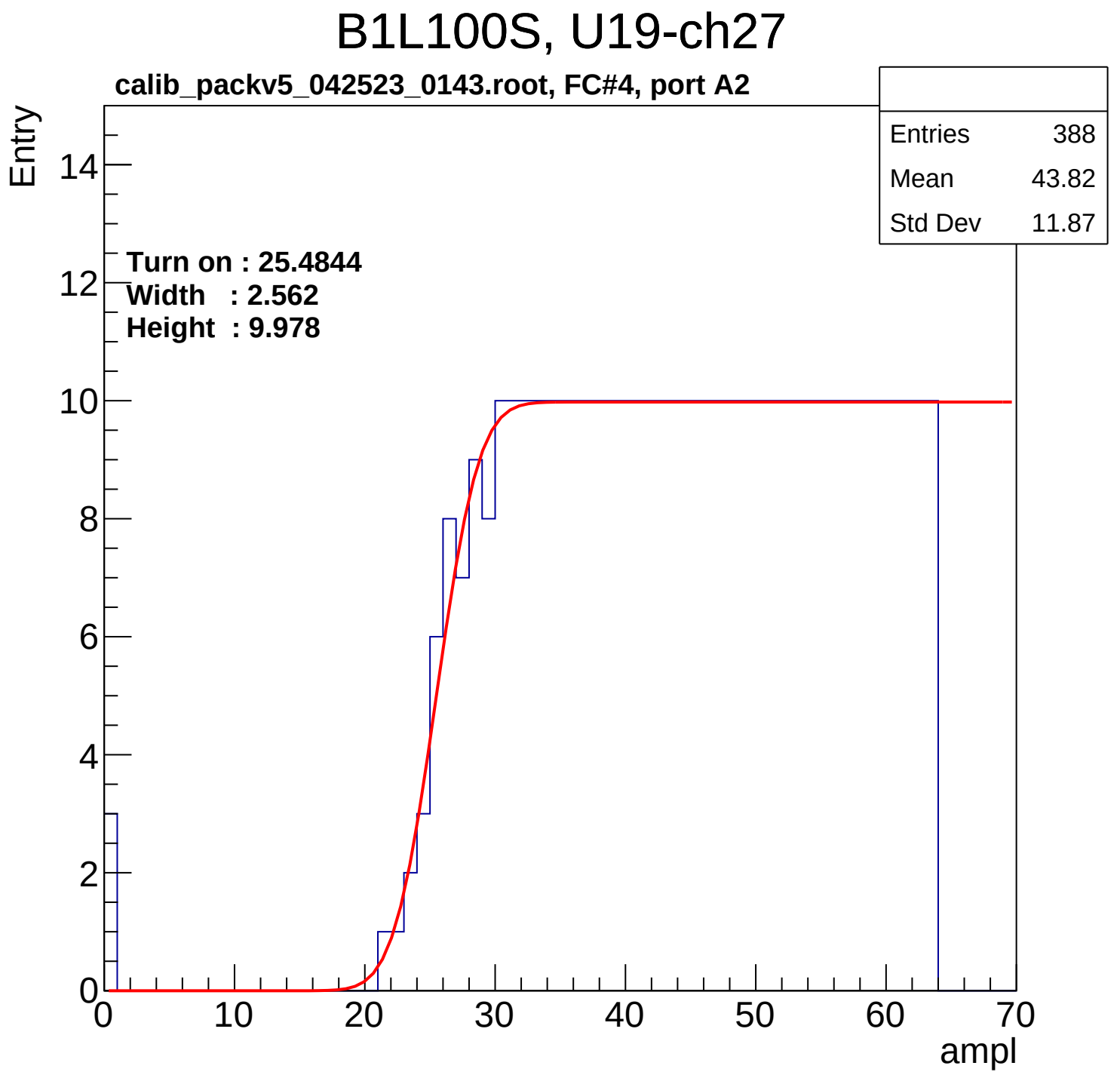
B1L100S, U19-ch27
calib_packv5_042523_0143.root, FC#4, port A2
Entries 388
Mean 43.82
Std Dev 11.87
Turn on : 25.4844
Width : 2.562
Height : 9.978
Entry
ampl
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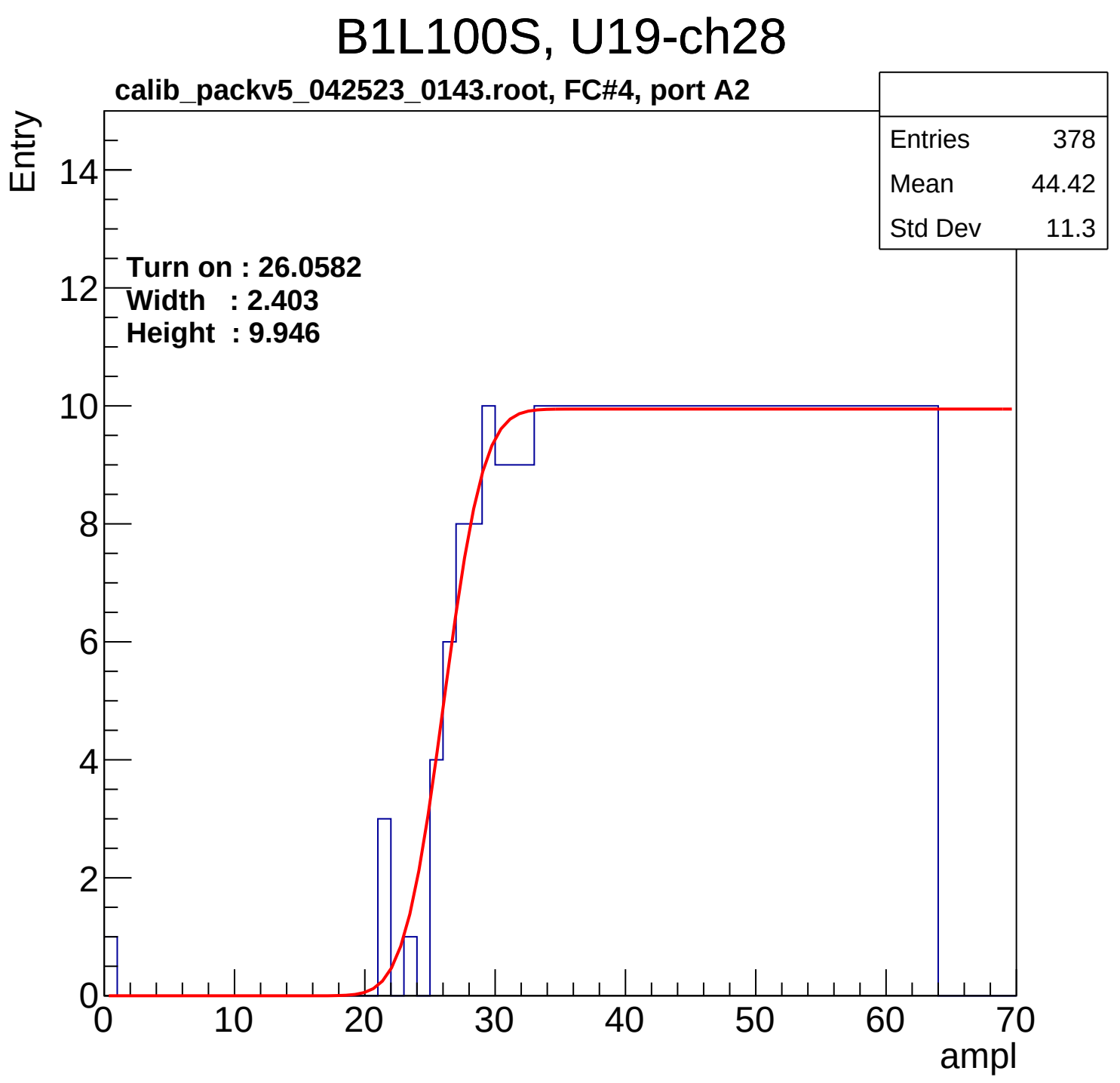
B1L100S, U19-ch28
calib_packv5_042523_0143.root, FC#4, port A2
Entries 378
Mean 44.42
Std Dev 11.3
Turn on : 26.0582
Width : 2.403
Height : 9.946
Entry
ampl
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4
6
8
10
12
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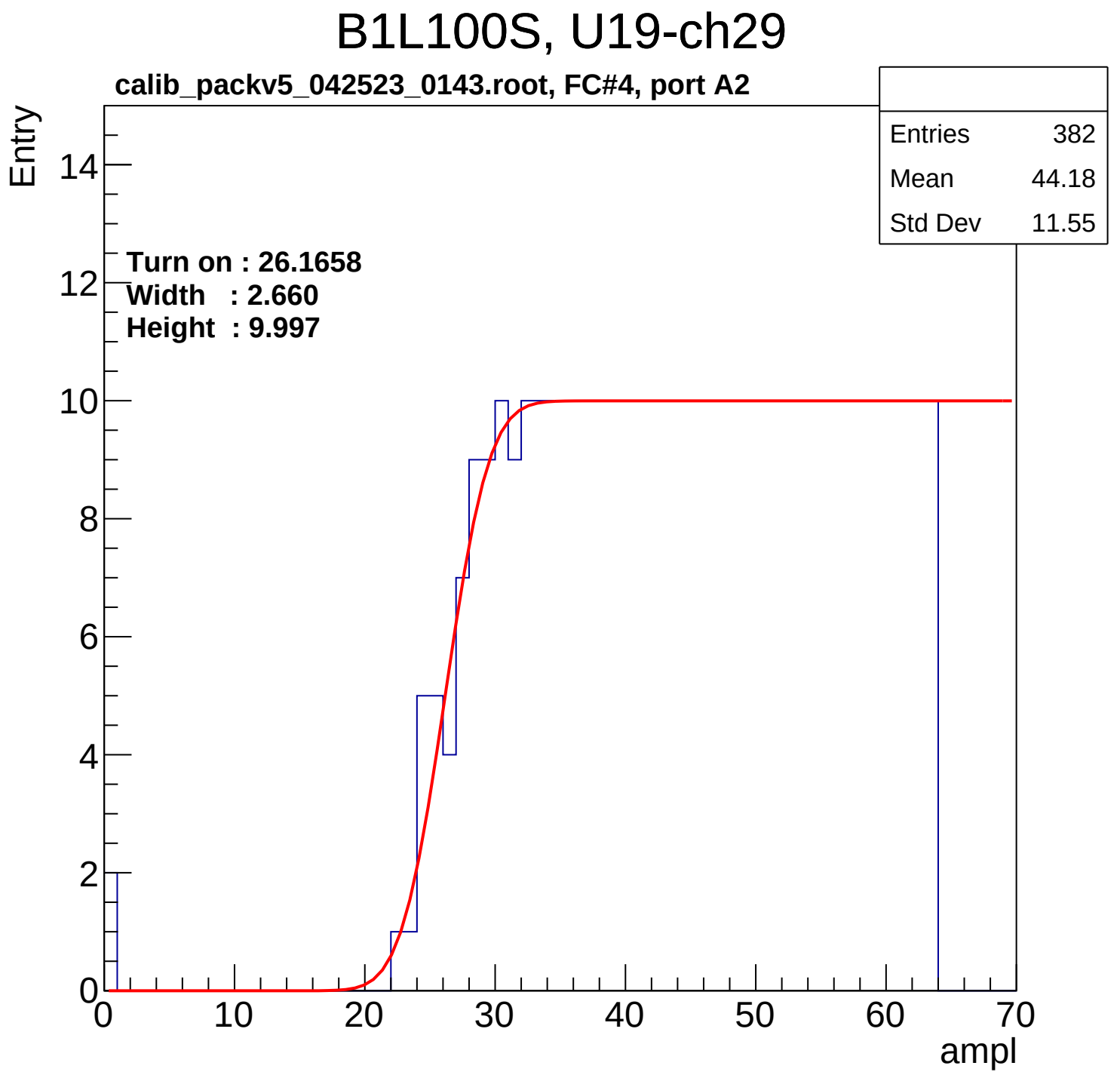
B1L100S, U19-ch29
calib_packv5_042523_0143.root, FC#4, port A2
Entries 382
Mean 44.18
Std Dev 11.55
Turn on : 26.1658
Width : 2.660
Height : 9.997
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ampl
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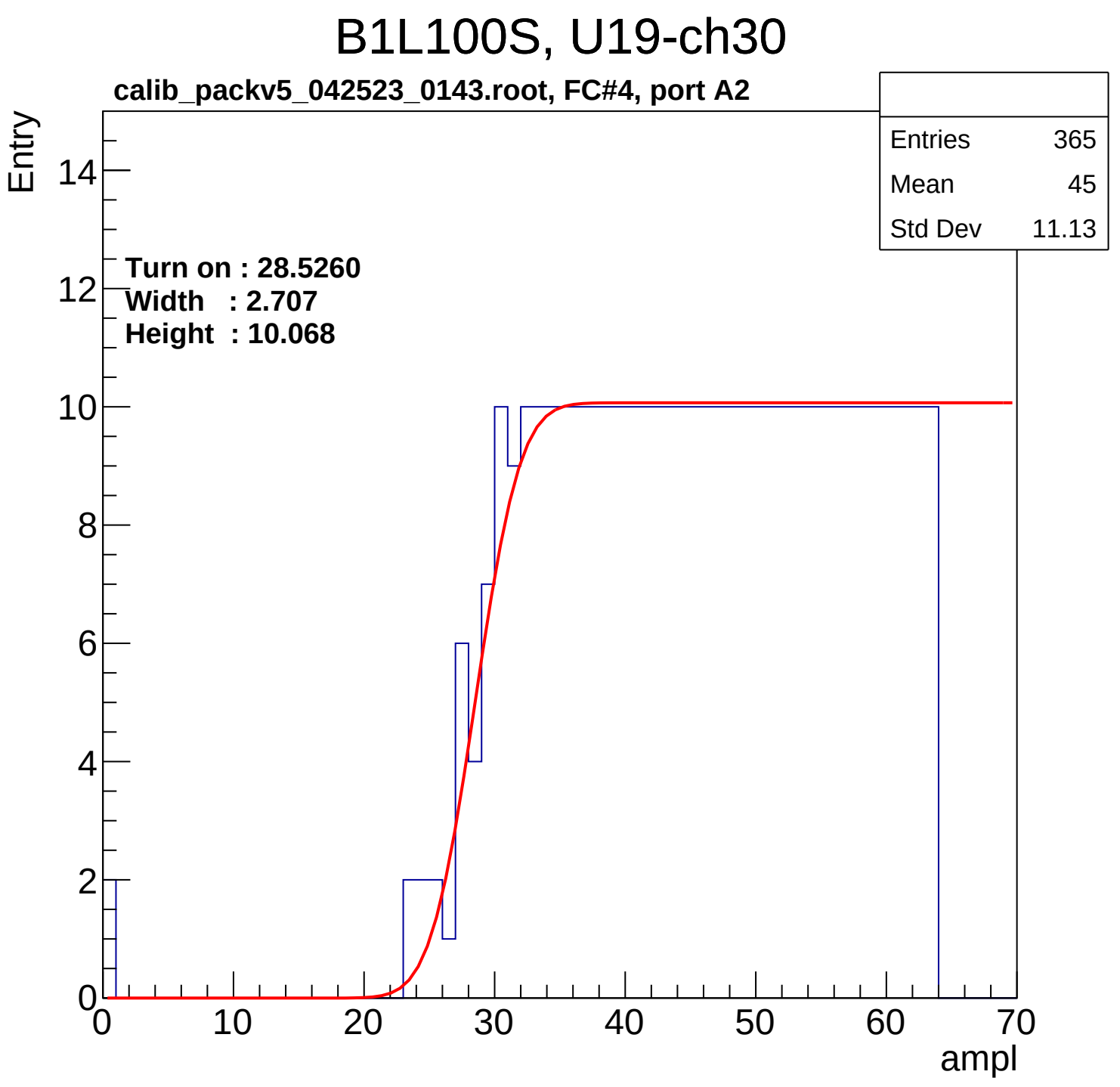
B1L100S, U19-ch30
calib_packv5_042523_0143.root, FC#4, port A2
Entries 365
Mean 45
Std Dev 11.13
Turn on : 28.5260
Width : 2.707
Height : 10.068
Entry
ampl
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4
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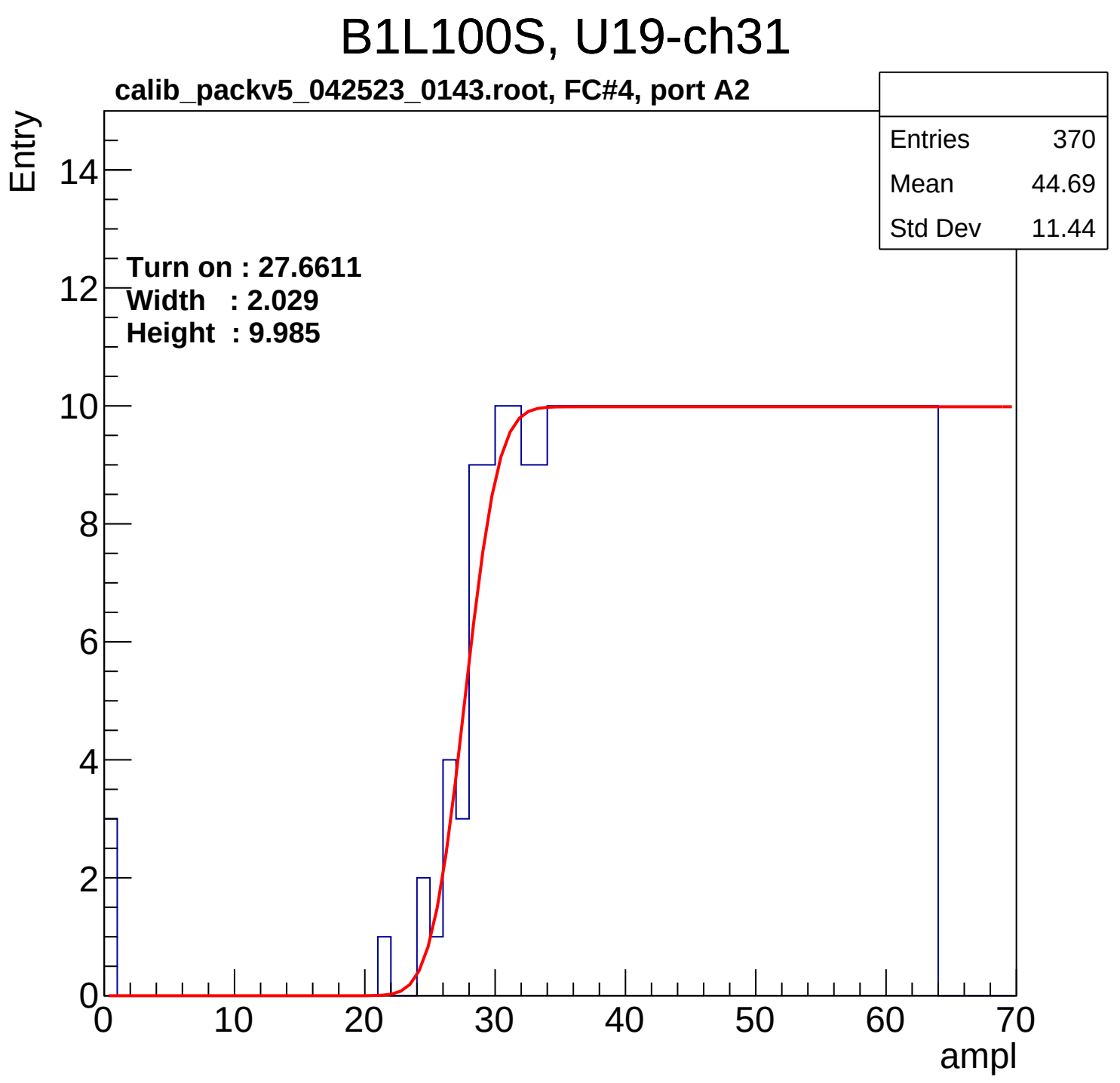
B1L100S, U19-ch31
calib_packv5_042523_0143.root, FC#4, port A2
Entries 370
Mean 44.69
Std Dev 11.44
Turn on : 27.6611
Width : 2.029
Height : 9.985
Entry
ampl
0
2
4
6
8
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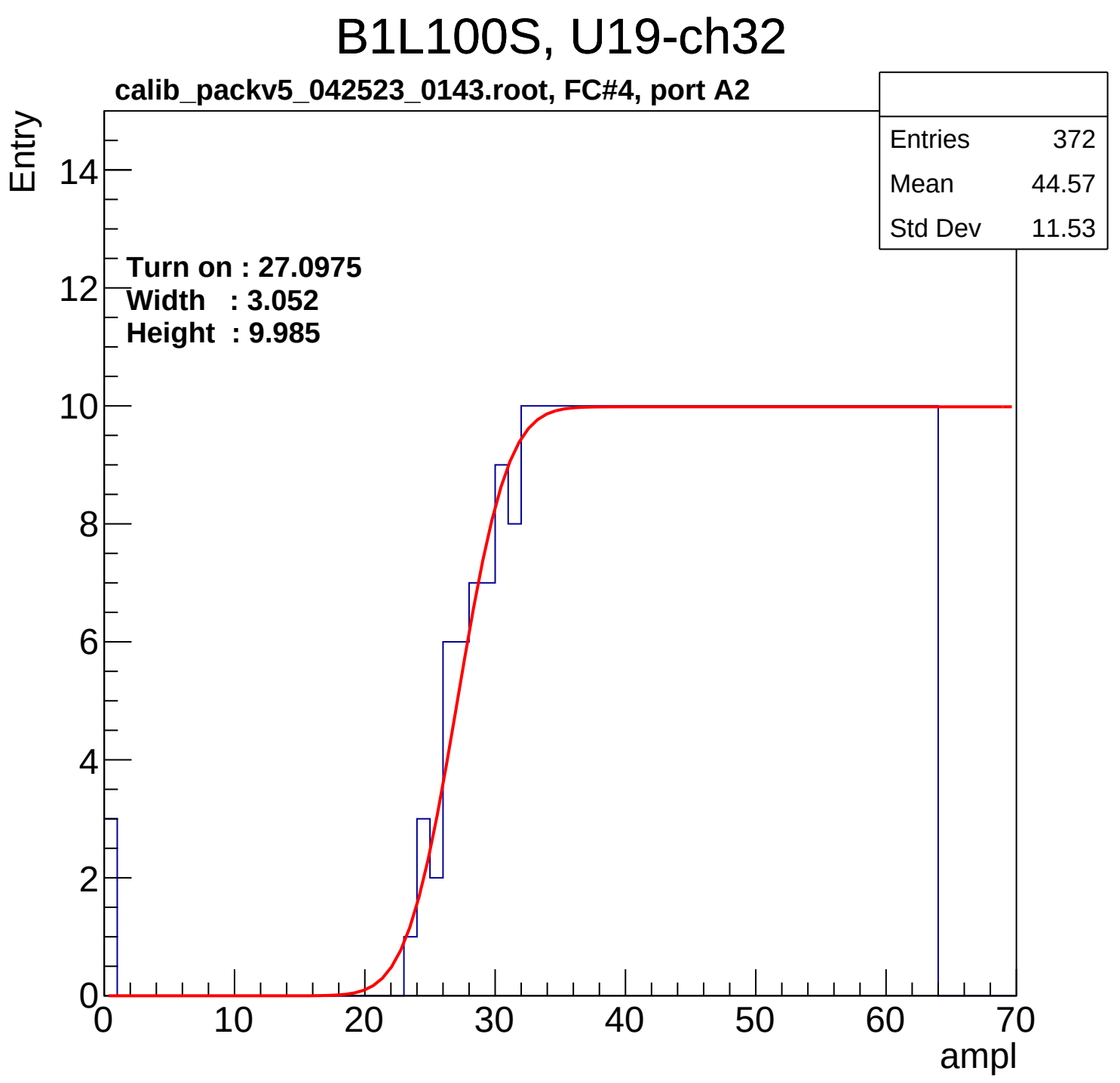
B1L100S, U19-ch32
calib_packv5_042523_0143.root, FC#4, port A2
Entries 372
Mean 44.57
Std Dev 11.53
Turn on : 27.0975
Width : 3.052
Height : 9.985
Entry
ampl
0
2
4
6
8
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12
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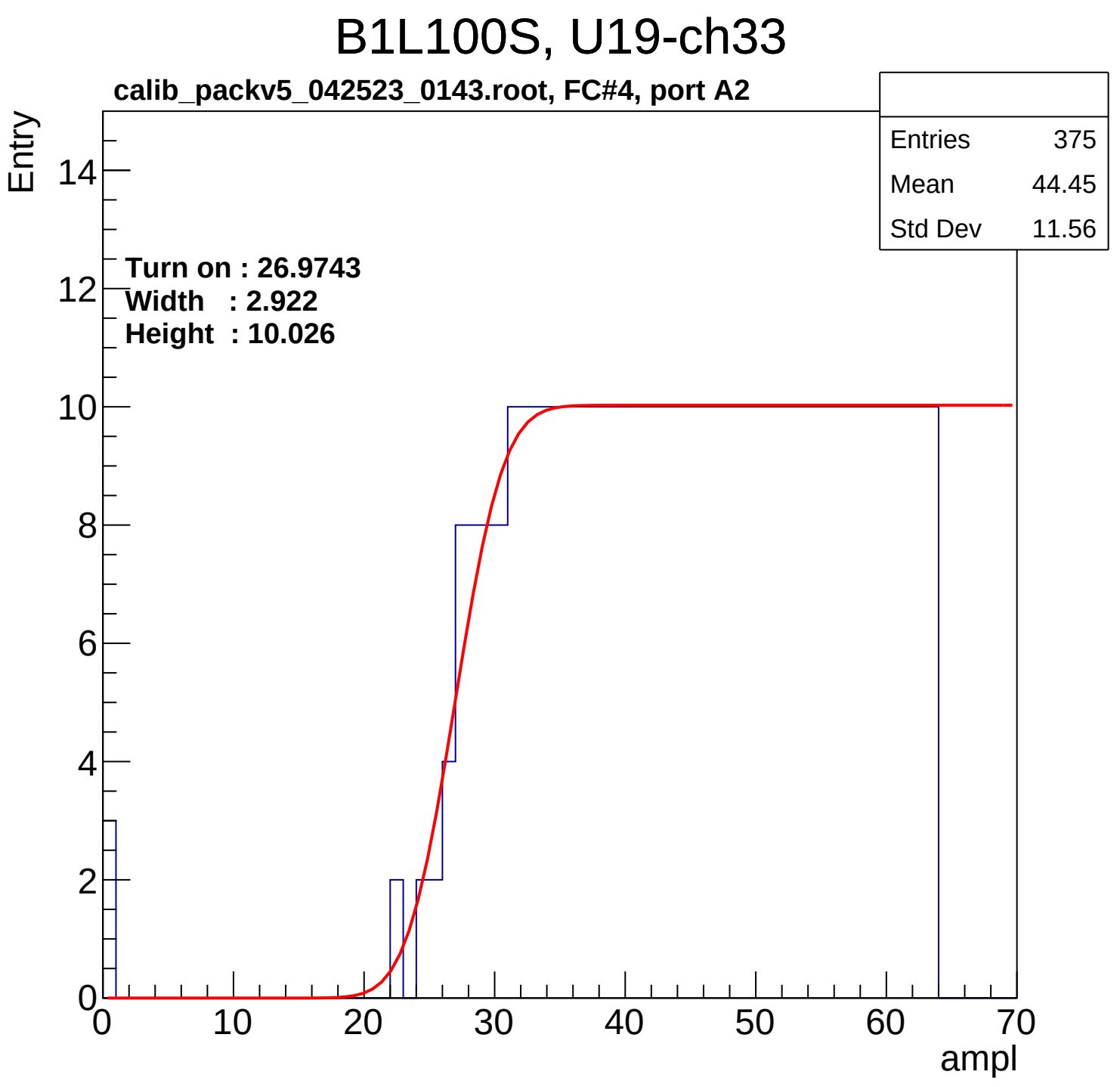
B1L100S, U19-ch33
calib_packv5_042523_0143.root, FC#4, port A2
Entries 375
Mean 44.45
Std Dev 11.56
Turn on : 26.9743
Width : 2.922
Height : 10.026
Entry
ampl
0
2
4
6
8
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12
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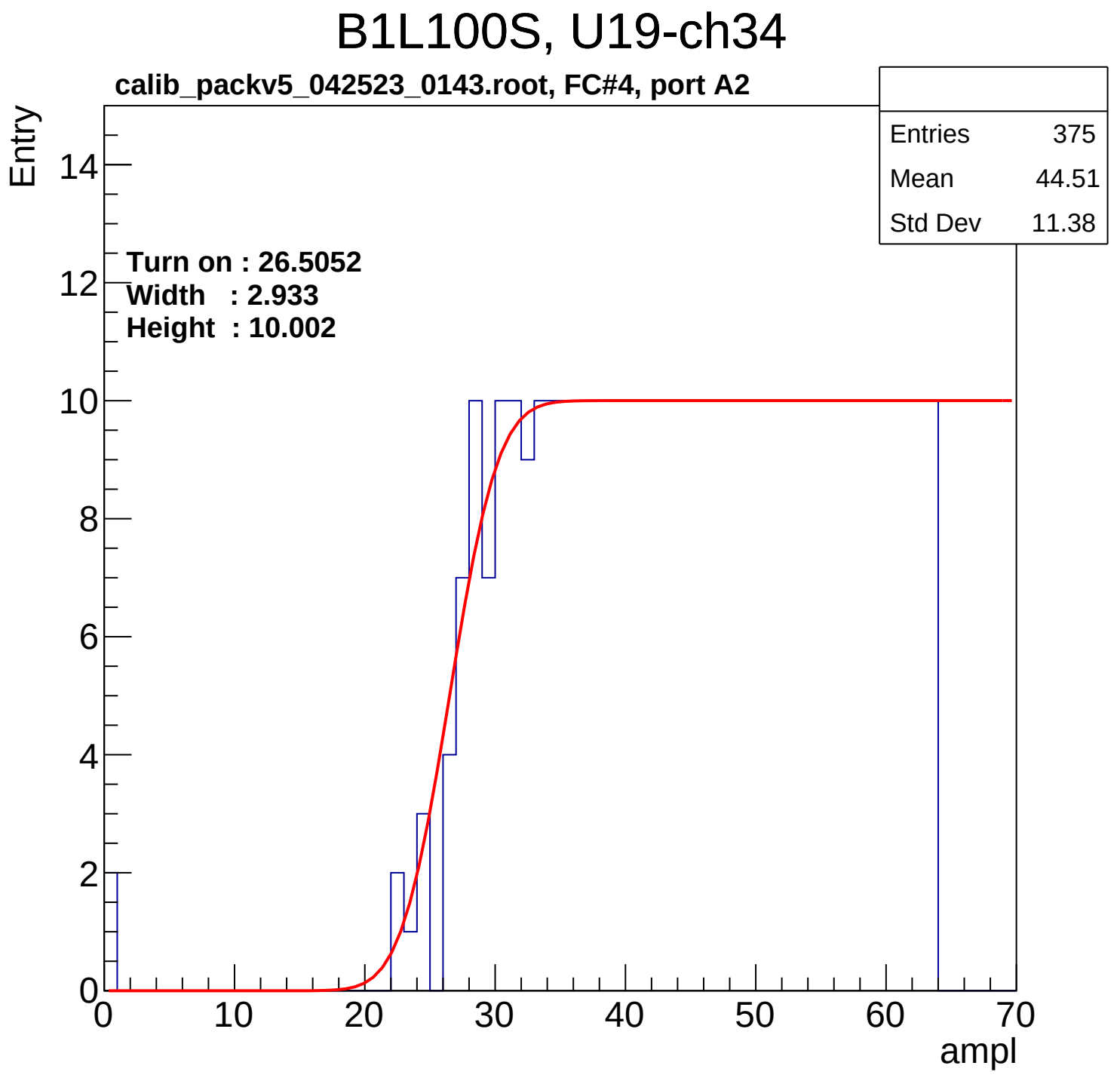
B1L100S, U19-ch34
calib_packv5_042523_0143.root, FC#4, port A2
Entries 375
Mean 44.51
Std Dev 11.38
Turn on : 26.5052
Width : 2.933
Height : 10.002
Entry
ampl
0
2
4
6
8
10
12
14
0
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60
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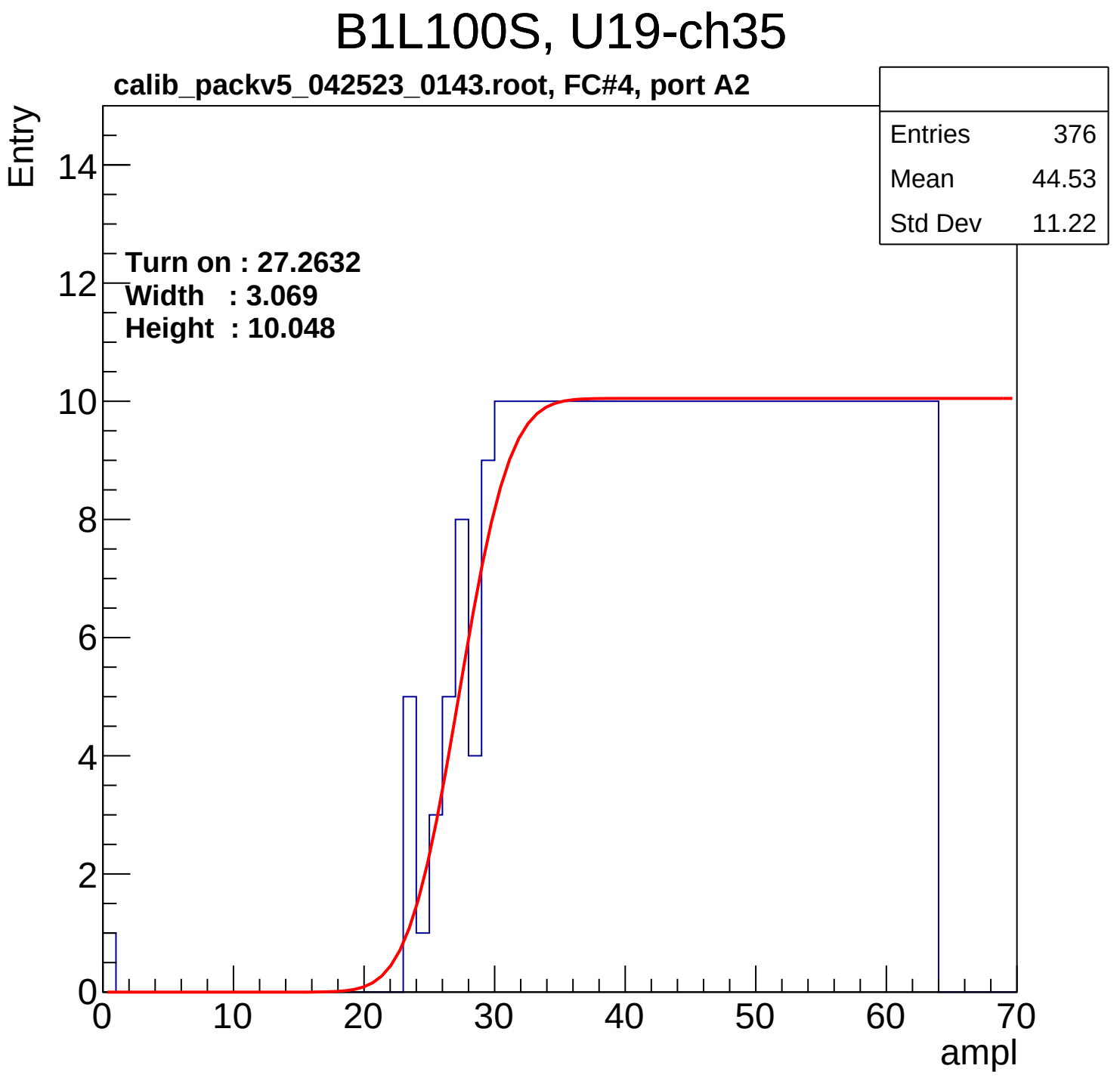
B1L100S, U19-ch35
calib_packv5_042523_0143.root, FC#4, port A2
Entries 376
Mean 44.53
Std Dev 11.22
Turn on : 27.2632
Width : 3.069
Height : 10.048
Entry
ampl
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4
6
8
10
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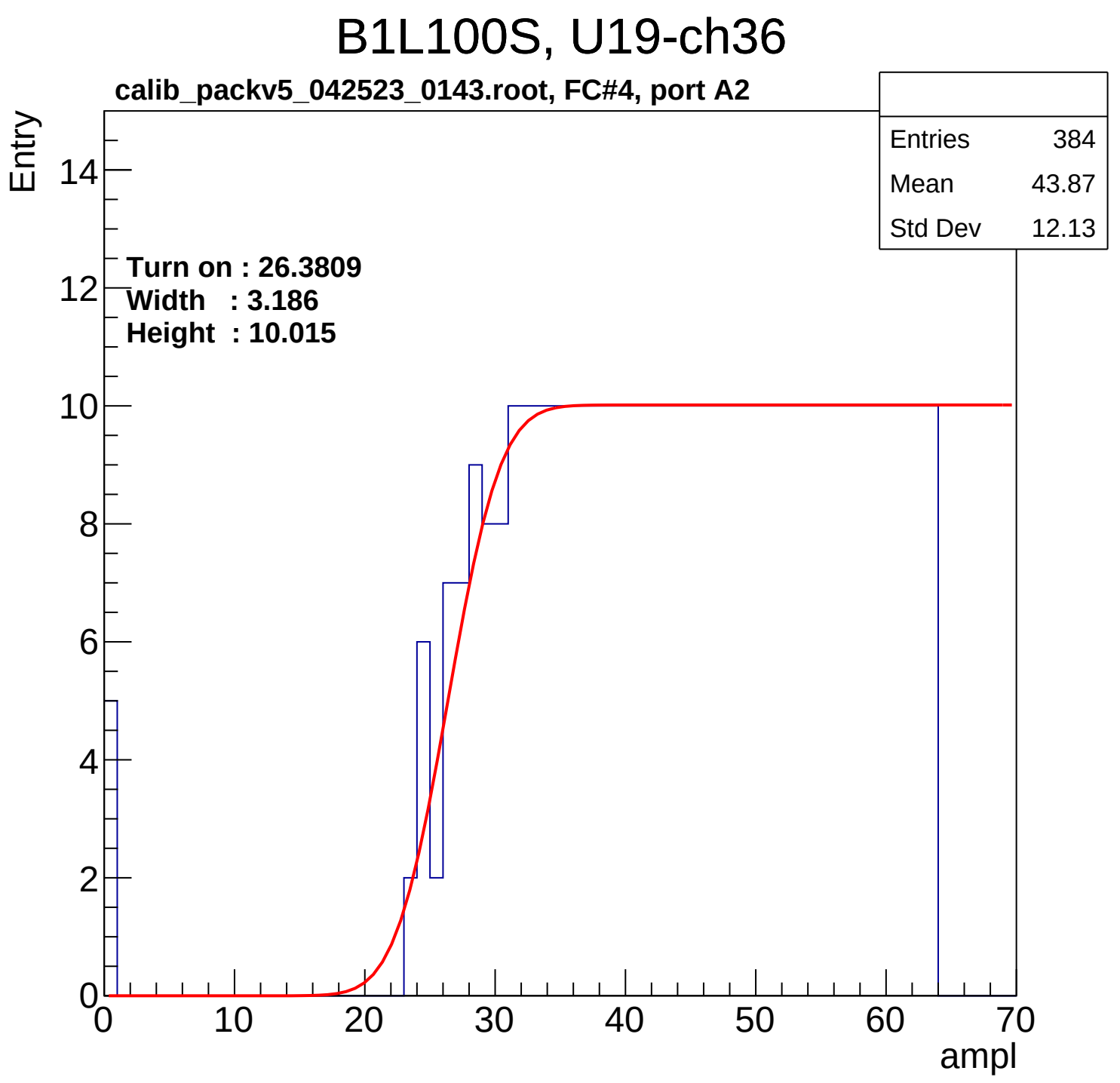
B1L100S, U19-ch36
calib_packv5_042523_0143.root, FC#4, port A2
Entries 384
Mean 43.87
Std Dev 12.13
Turn on : 26.3809
Width : 3.186
Height : 10.015
Entry
ampl
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4
6
8
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60
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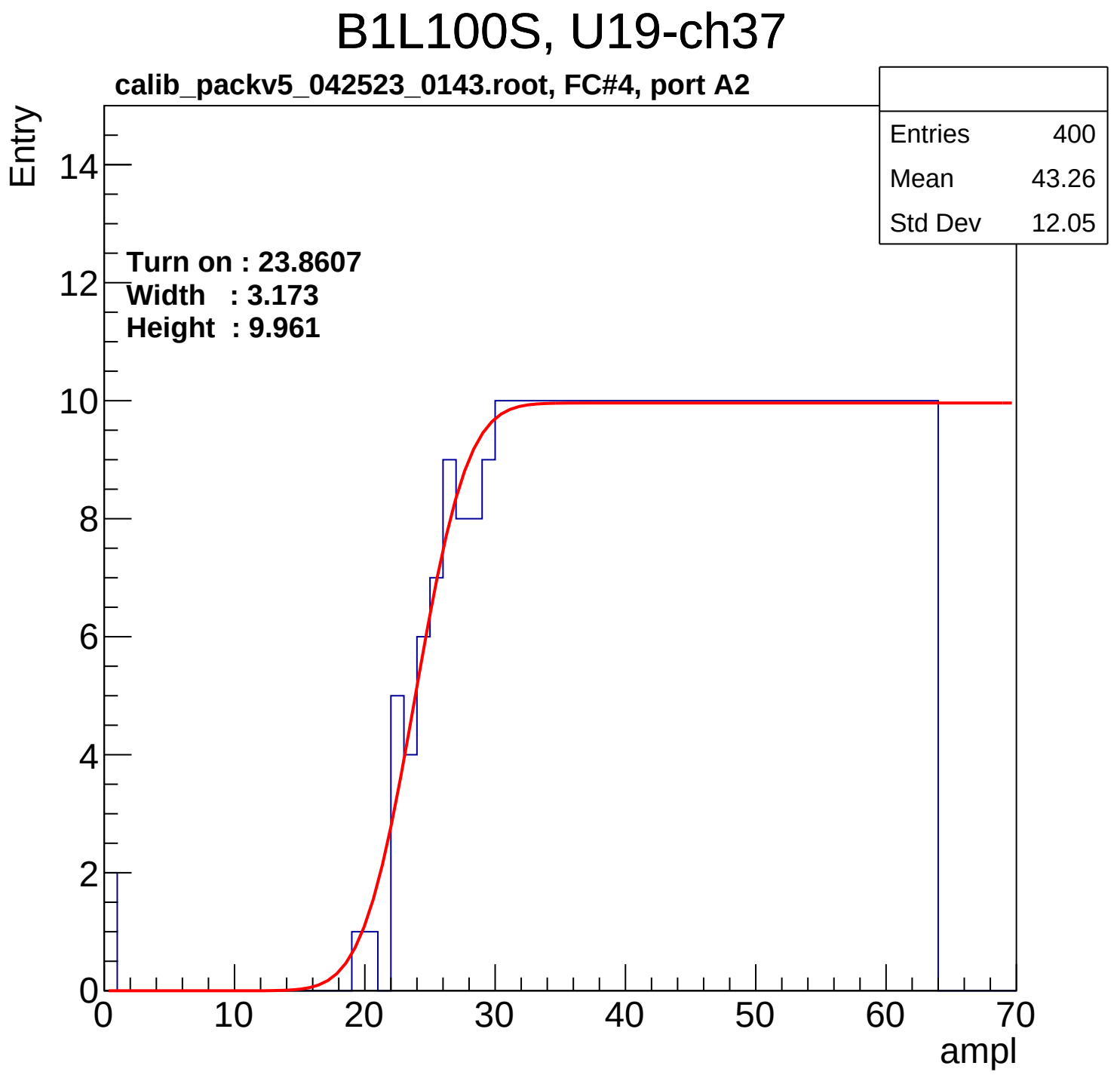
B1L100S, U19-ch37
calib_packv5_042523_0143.root, FC#4, port A2
Entries 400
Mean 43.26
Std Dev 12.05
Turn on : 23.8607
Width : 3.173
Height : 9.961
Entry
ampl
0
2
4
6
8
10
12
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0
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60
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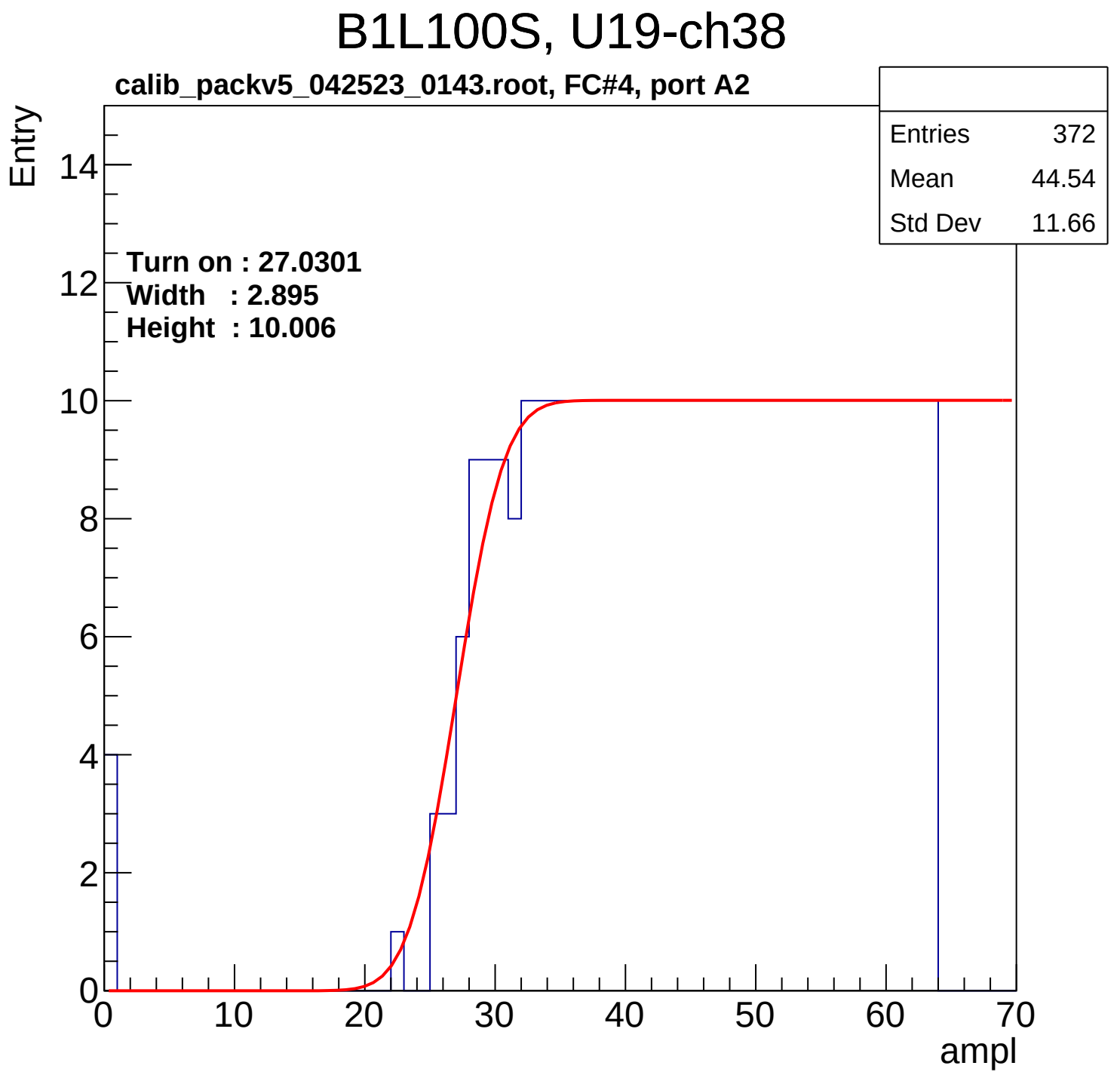
B1L100S, U19-ch38
calib_packv5_042523_0143.root, FC#4, port A2
Entries 372
Mean 44.54
Std Dev 11.66
Turn on : 27.0301
Width : 2.895
Height : 10.006
Entry
ampl
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6
8
10
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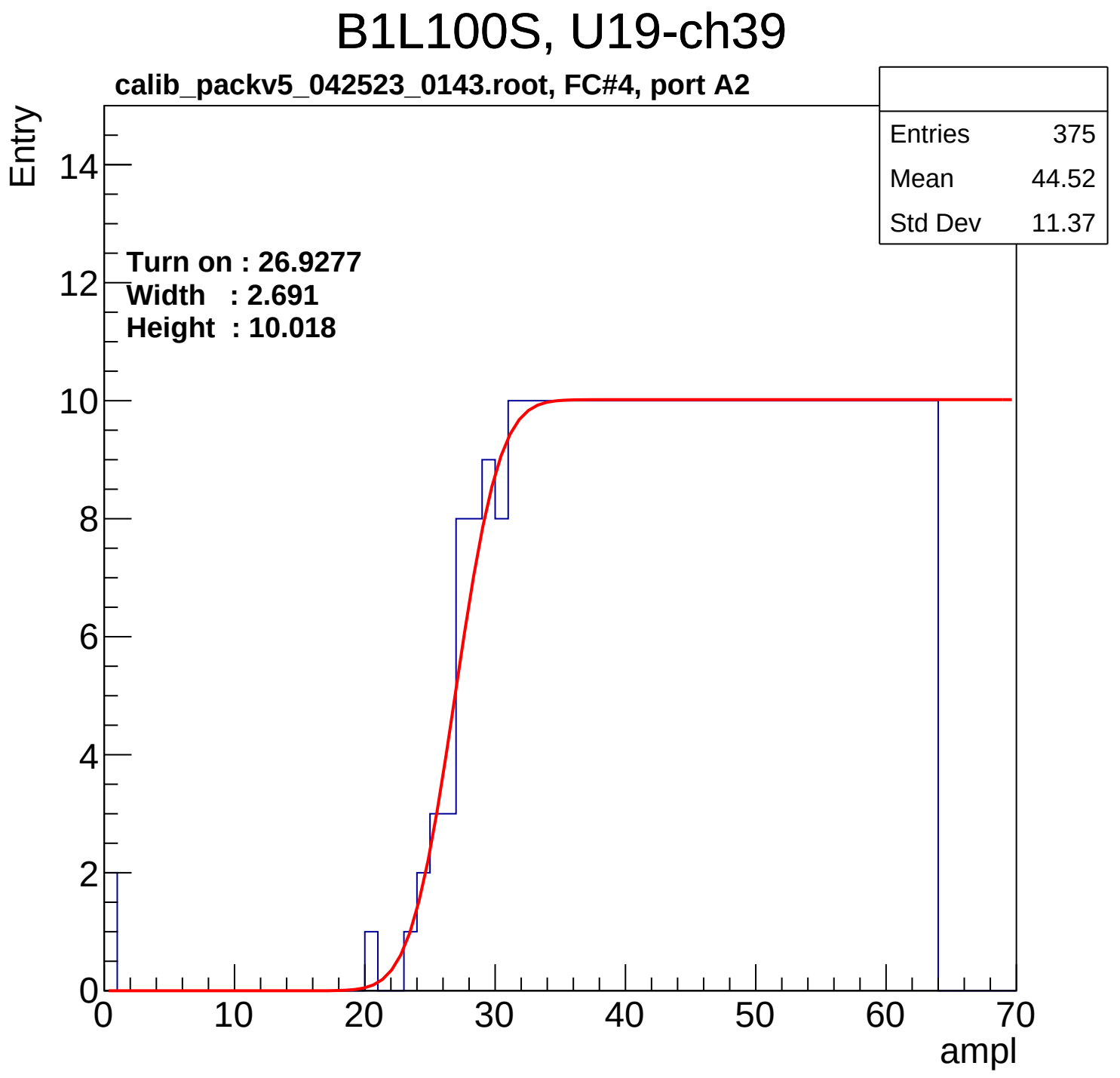
B1L100S, U19-ch39
calib_packv5_042523_0143.root, FC#4, port A2
Entries 375
Mean 44.52
Std Dev 11.37
Turn on : 26.9277
Width : 2.691
Height : 10.018
Entry
ampl
0
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6
8
10
12
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0
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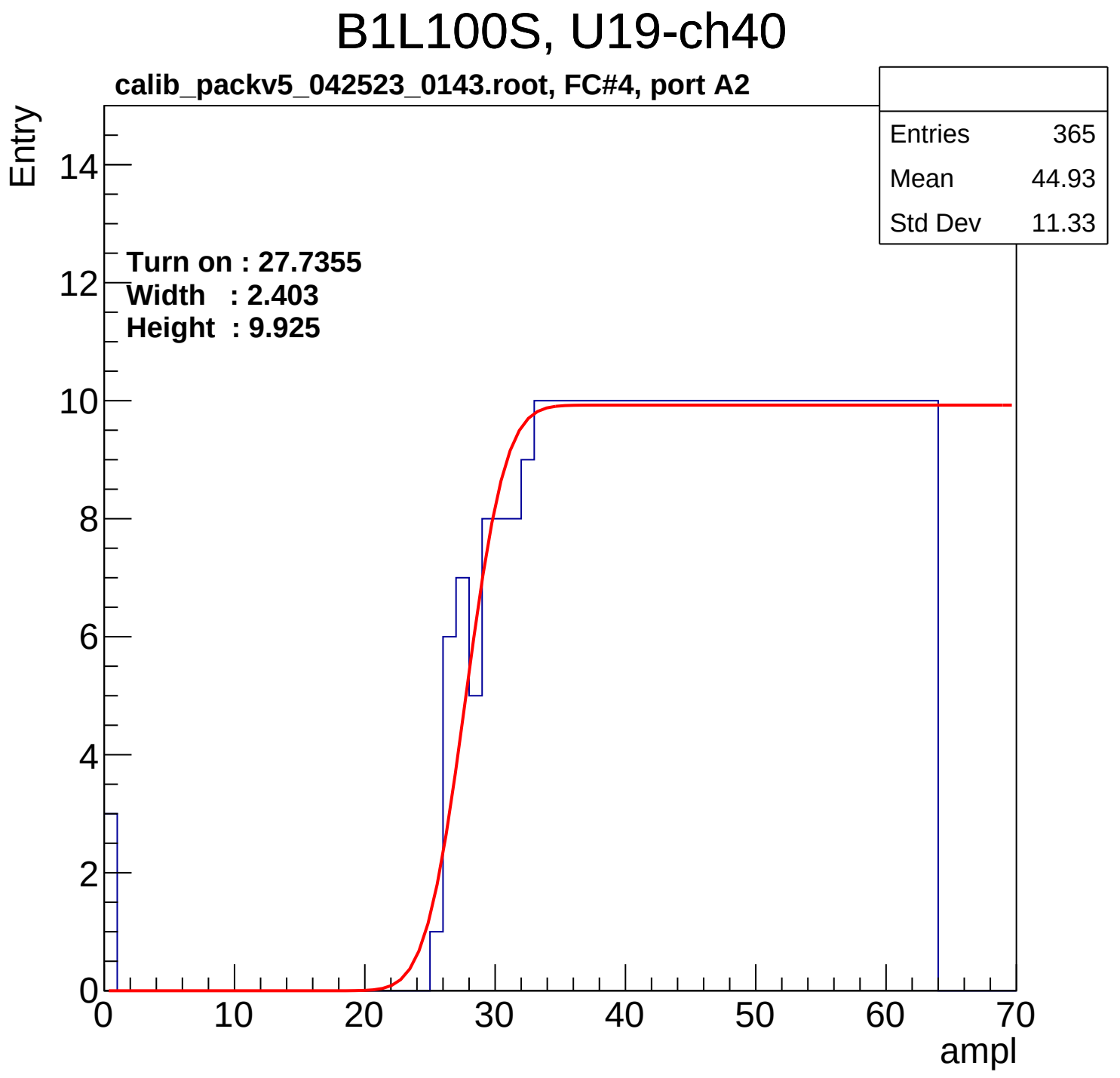
B1L100S, U19-ch40
calib_packv5_042523_0143.root, FC#4, port A2
Entries 365
Mean 44.93
Std Dev 11.33
Turn on : 27.7355
Width : 2.403
Height : 9.925
Entry
ampl
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6
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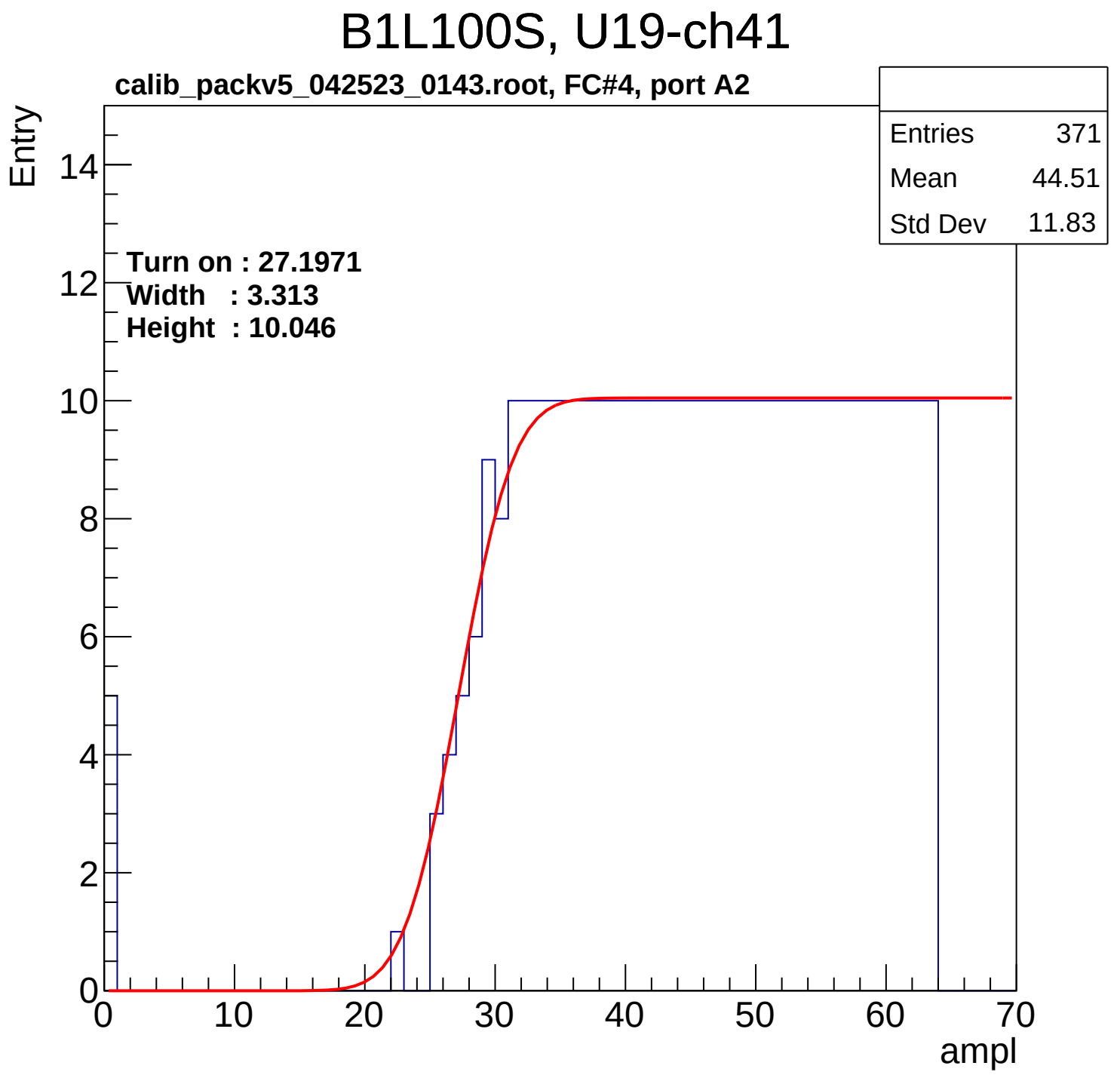
B1L100S, U19-ch41
calib_packv5_042523_0143.root, FC#4, port A2
Entries 371
Mean 44.51
Std Dev 11.83
Turn on : 27.1971
Width : 3.313
Height : 10.046
Entry
ampl
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6
8
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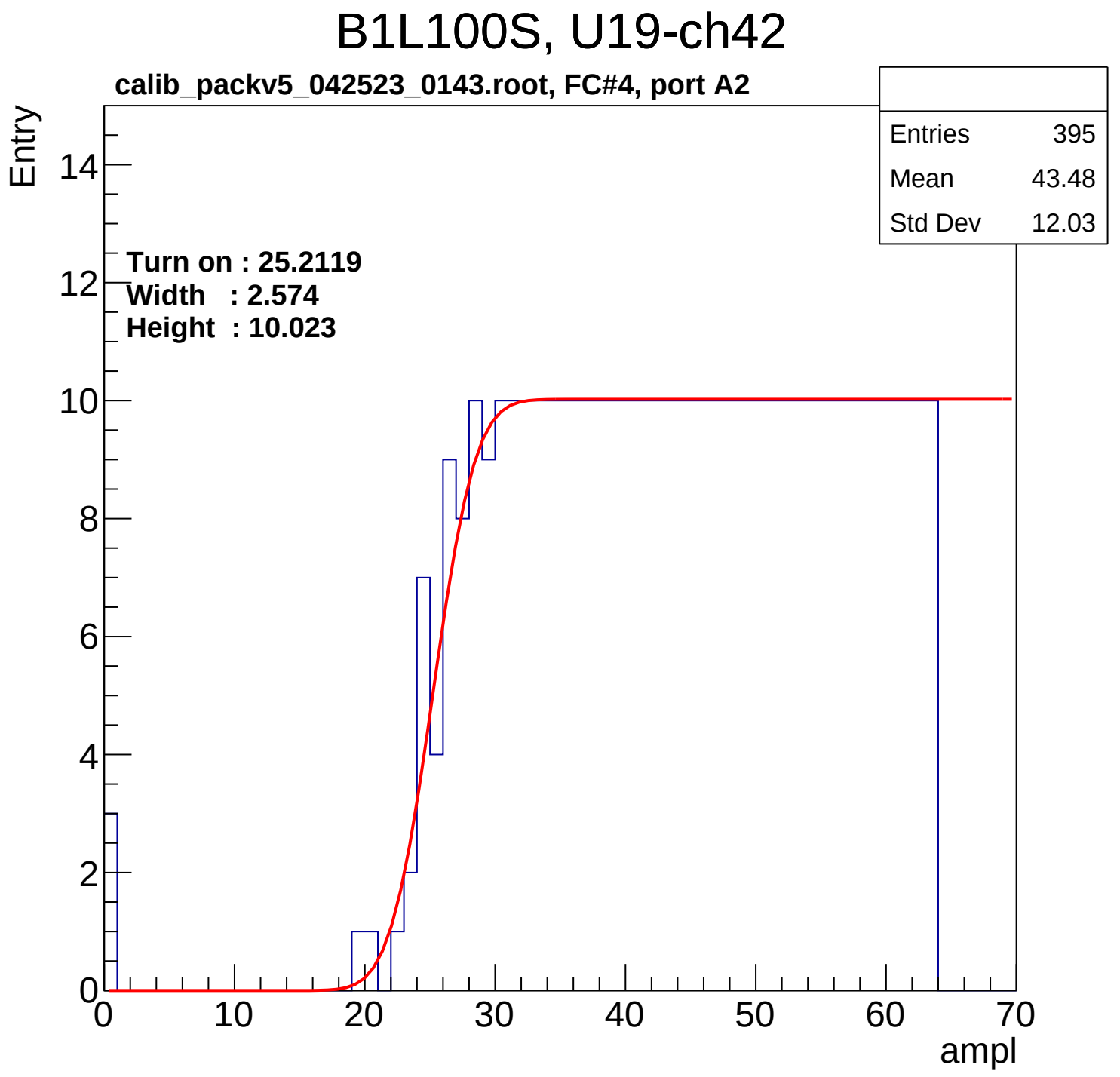
B1L100S, U19-ch42
calib_packv5_042523_0143.root, FC#4, port A2
Entries 395
Mean 43.48
Std Dev 12.03
Turn on : 25.2119
Width : 2.574
Height : 10.023
Entry
ampl
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4
6
8
10
12
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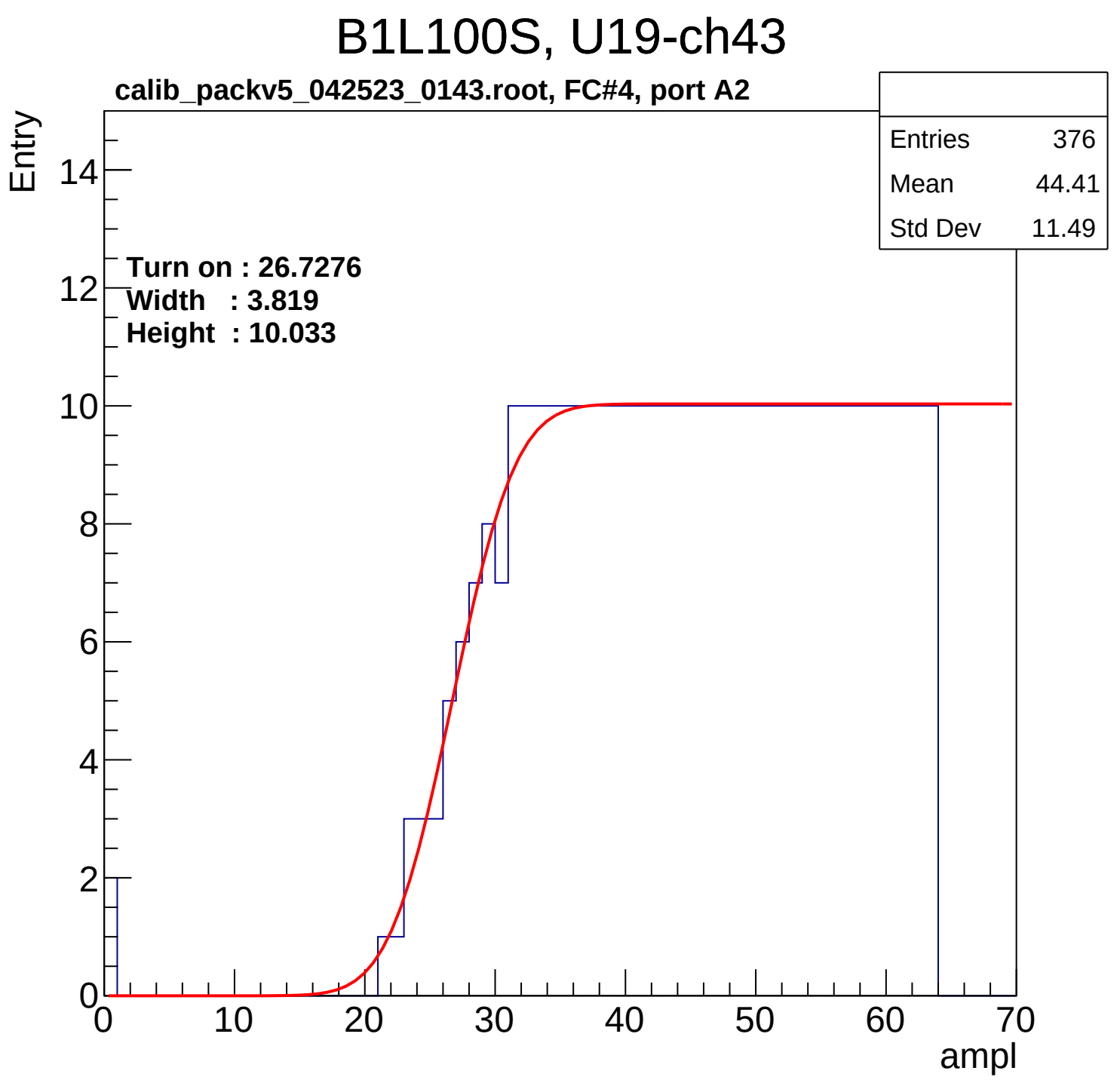
B1L100S, U19-ch43
calib_packv5_042523_0143.root, FC#4, port A2
Entries 376
Mean 44.41
Std Dev 11.49
Turn on : 26.7276
Width : 3.819
Height : 10.033
Entry
ampl
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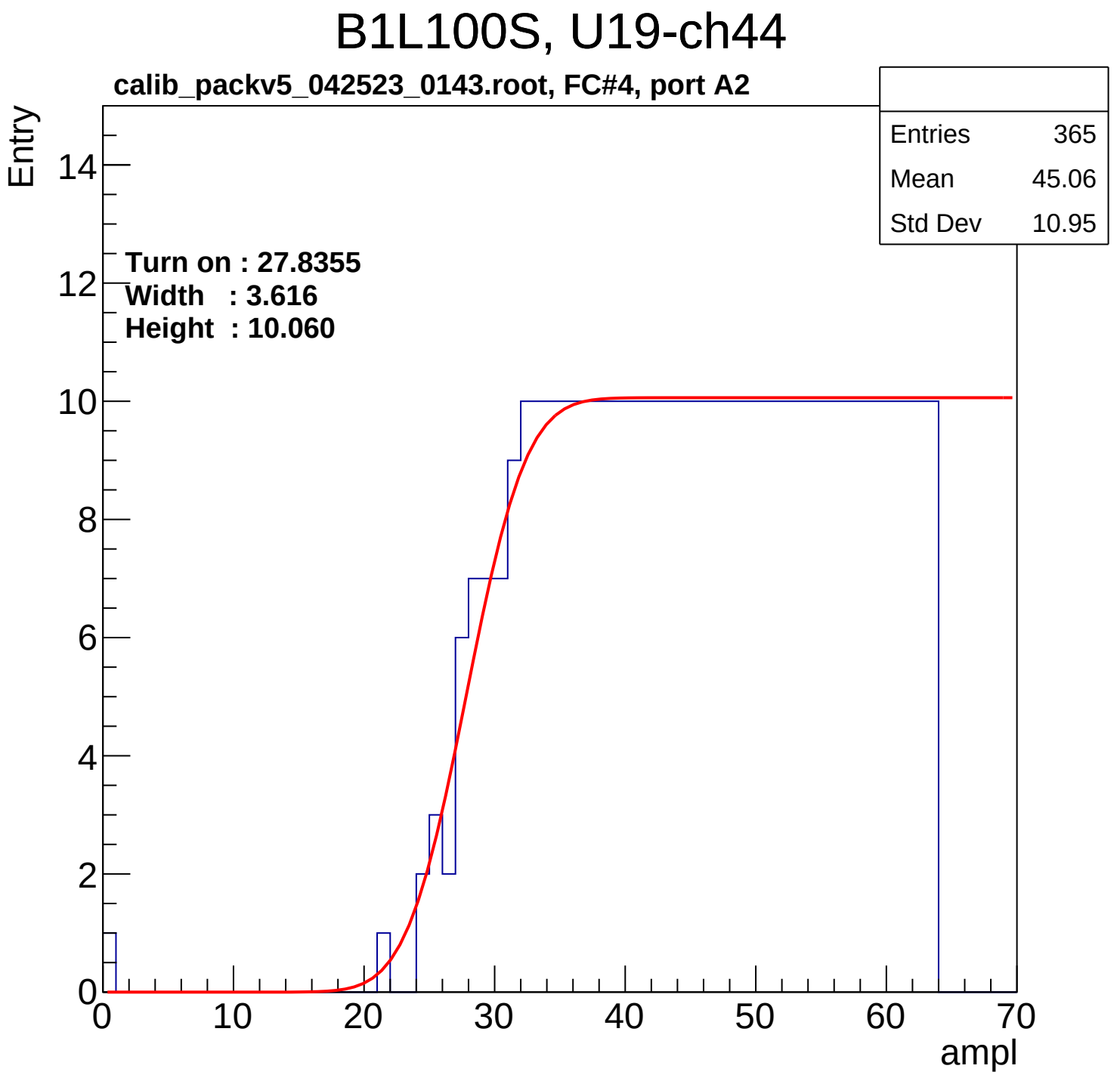
B1L100S, U19-ch44
calib_packv5_042523_0143.root, FC#4, port A2
Entries 365
Mean 45.06
Std Dev 10.95
Turn on : 27.8355
Width : 3.616
Height : 10.060
Entry
ampl
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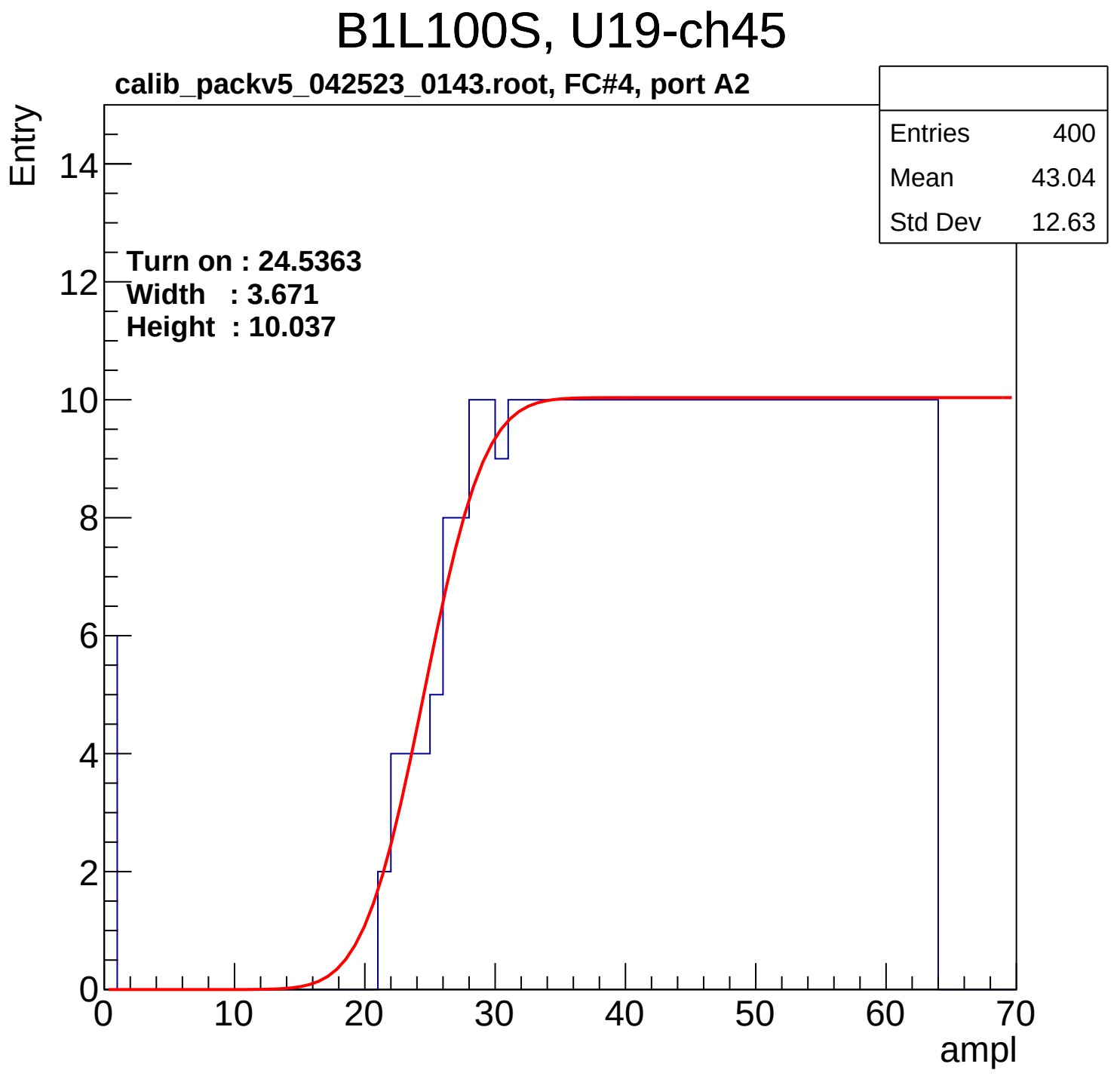
B1L100S, U19-ch45
calib_packv5_042523_0143.root, FC#4, port A2
Entries 400
Mean 43.04
Std Dev 12.63
Turn on : 24.5363
Width : 3.671
Height : 10.037
Entry
ampl
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8
10
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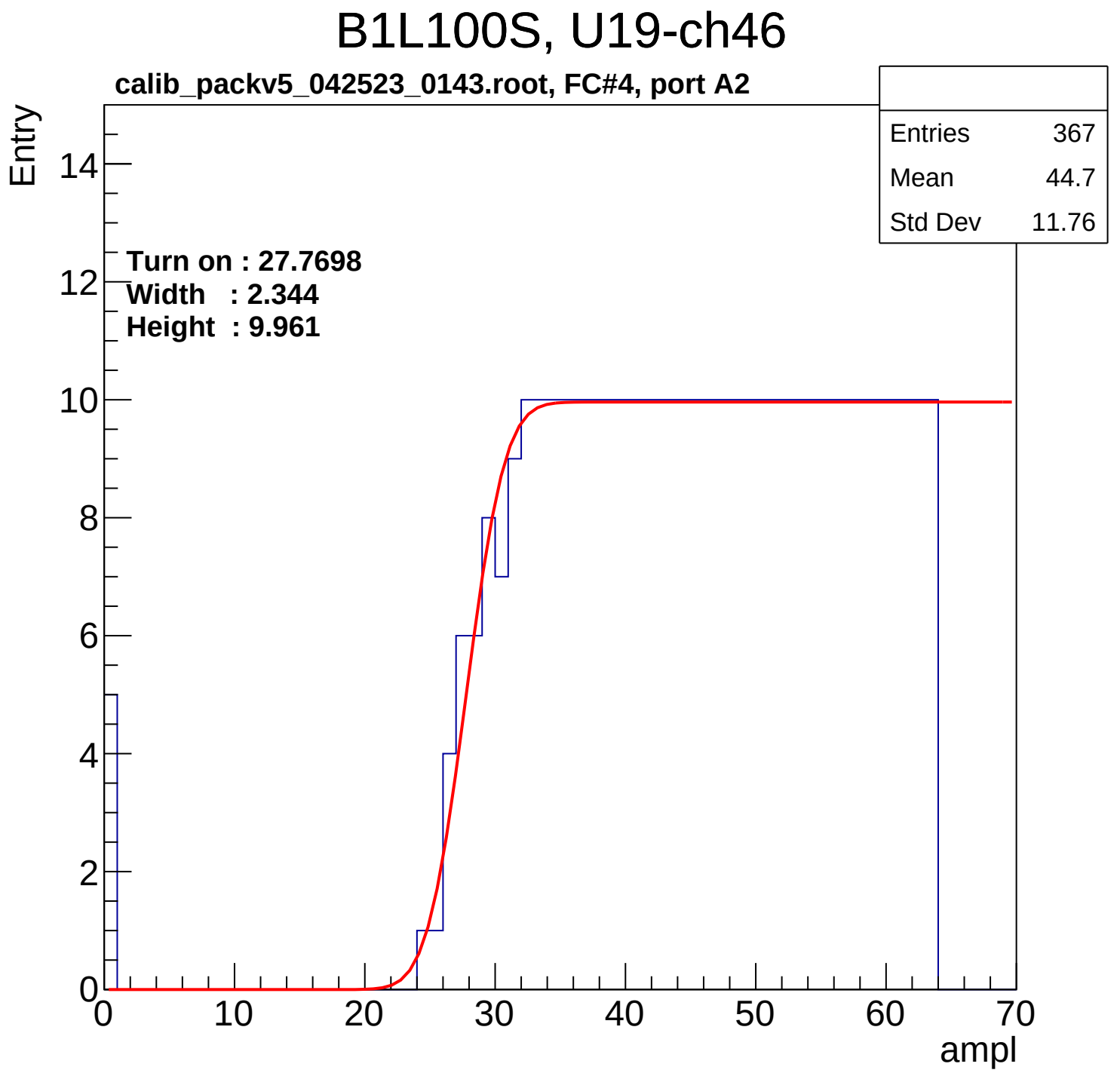
B1L100S, U19-ch46
calib_packv5_042523_0143.root, FC#4, port A2
Entries 367
Mean 44.7
Std Dev 11.76
Turn on : 27.7698
Width : 2.344
Height : 9.961
Entry
ampl
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2
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6
8
10
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0
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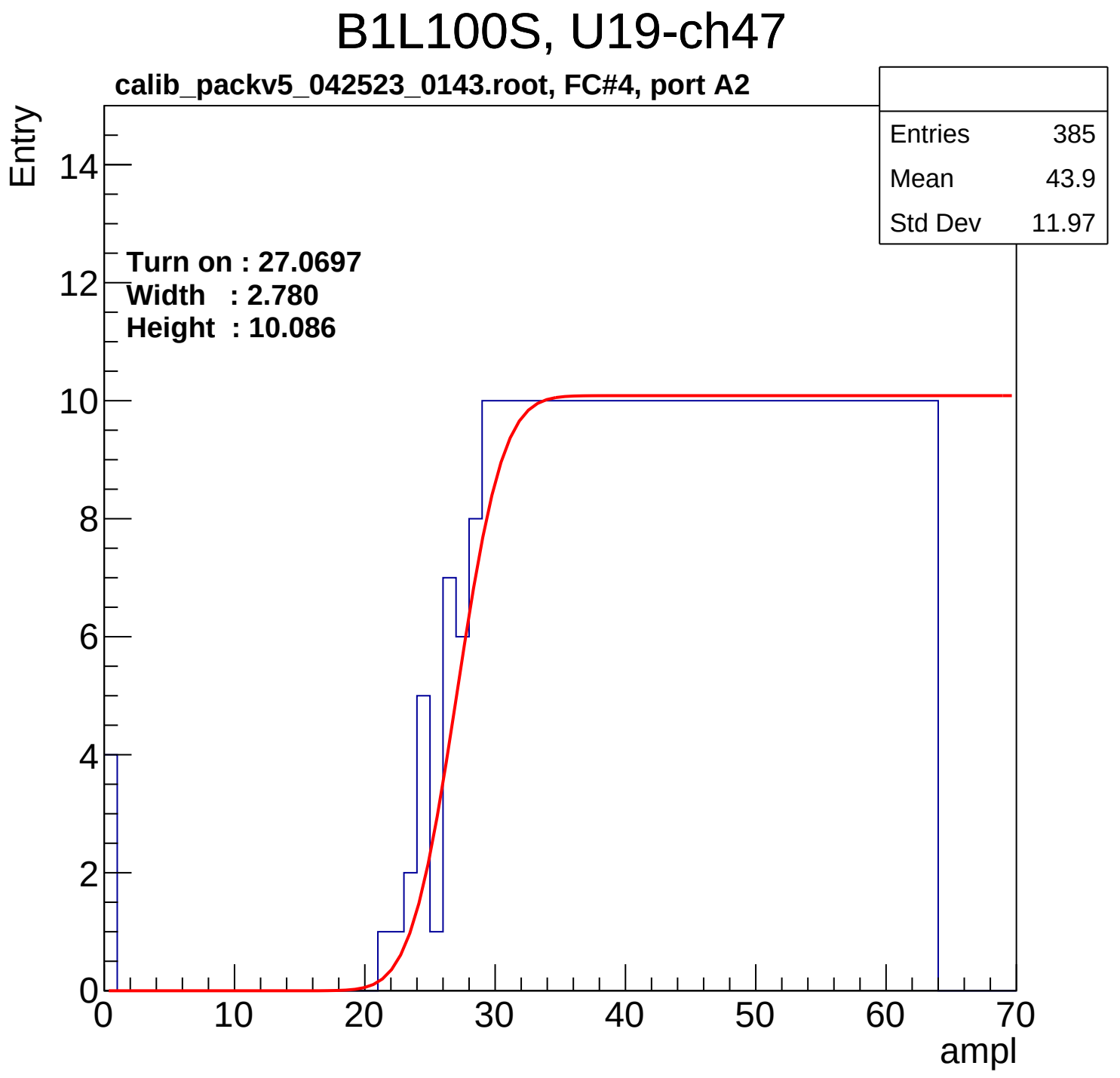
B1L100S, U19-ch47
calib_packv5_042523_0143.root, FC#4, port A2
Entries 385
Mean 43.9
Std Dev 11.97
Turn on : 27.0697
Width : 2.780
Height : 10.086
Entry
ampl
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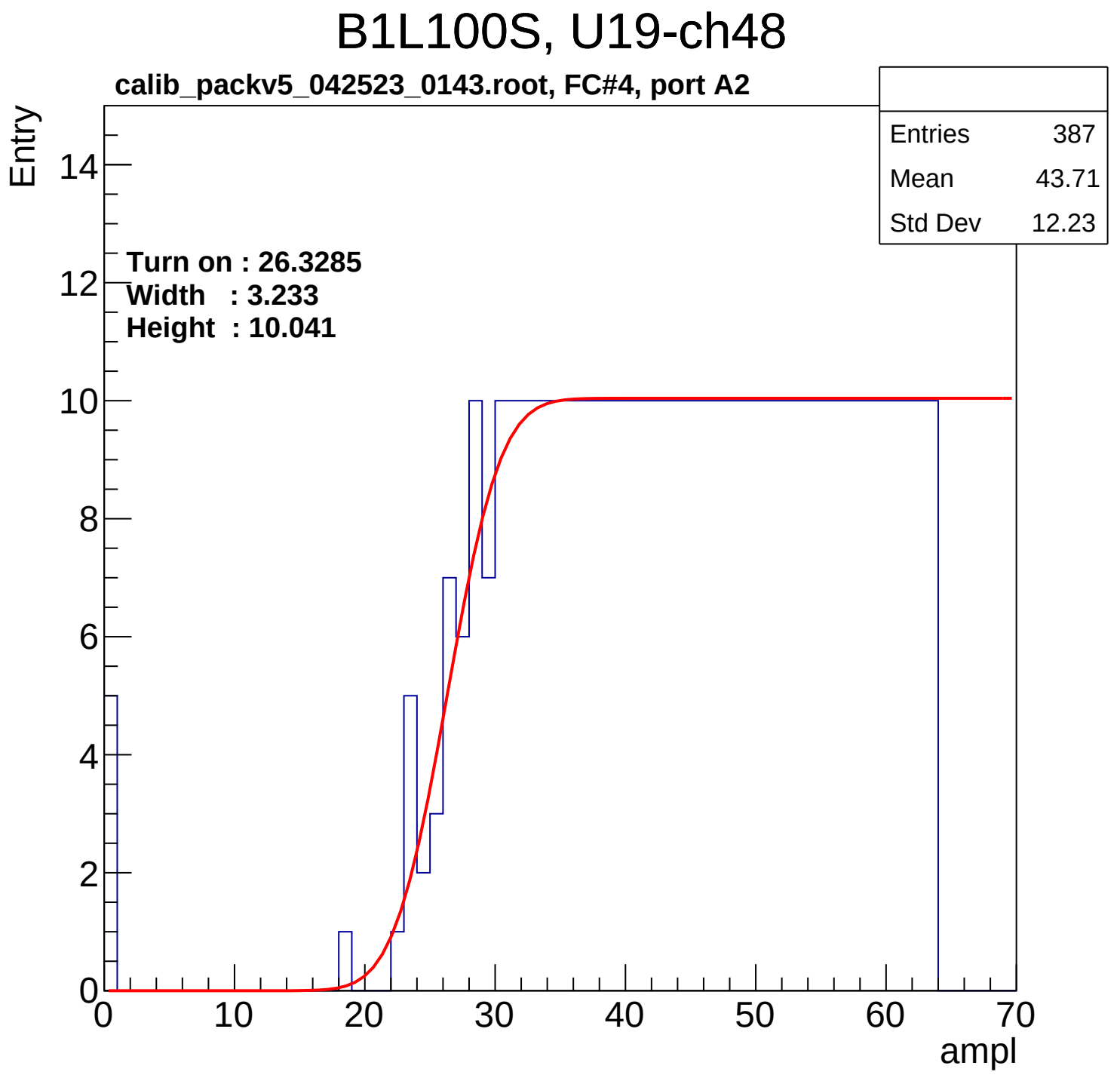
B1L100S, U19-ch48
calib_packv5_042523_0143.root, FC#4, port A2
Entries 387
Mean 43.71
Std Dev 12.23
Turn on : 26.3285
Width : 3.233
Height : 10.041
Entry
ampl
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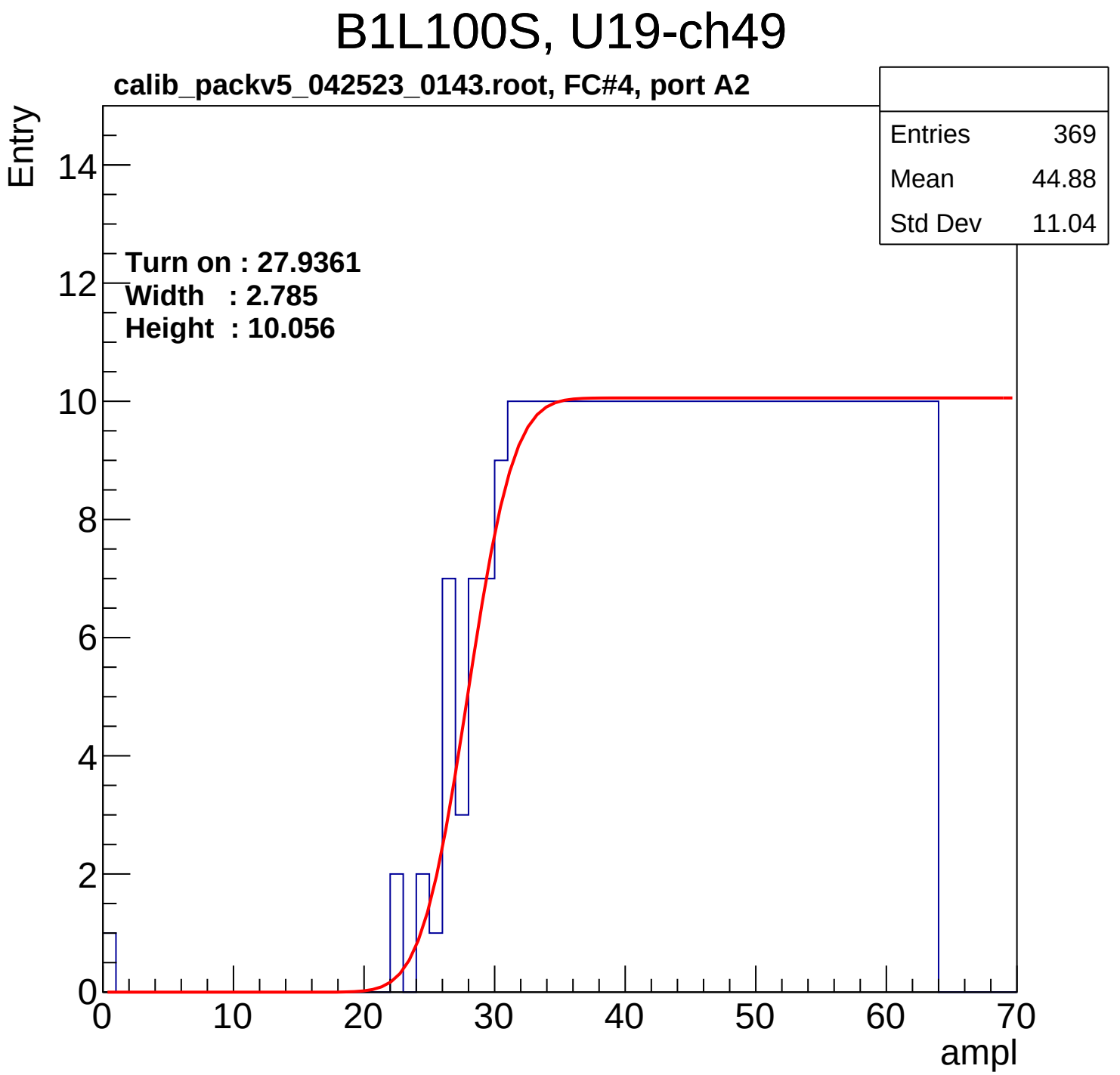
B1L100S, U19-ch49
calib_packv5_042523_0143.root, FC#4, port A2
Entries 369
Mean 44.88
Std Dev 11.04
Turn on : 27.9361
Width : 2.785
Height : 10.056
Entry
ampl
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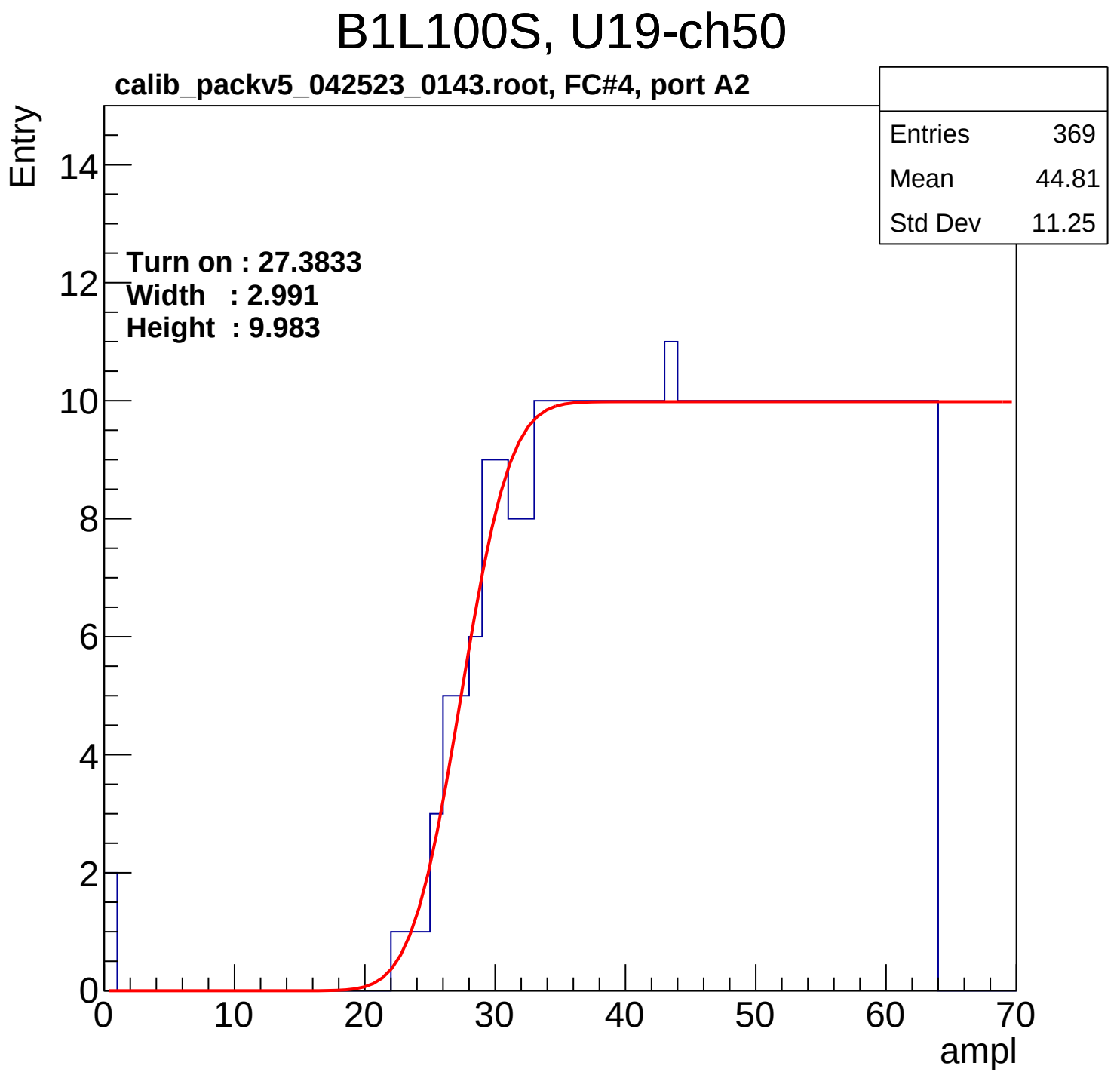
B1L100S, U19-ch50
calib_packv5_042523_0143.root, FC#4, port A2
Entries 369
Mean 44.81
Std Dev 11.25
Turn on : 27.3833
Width : 2.991
Height : 9.983
Entry
ampl
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6
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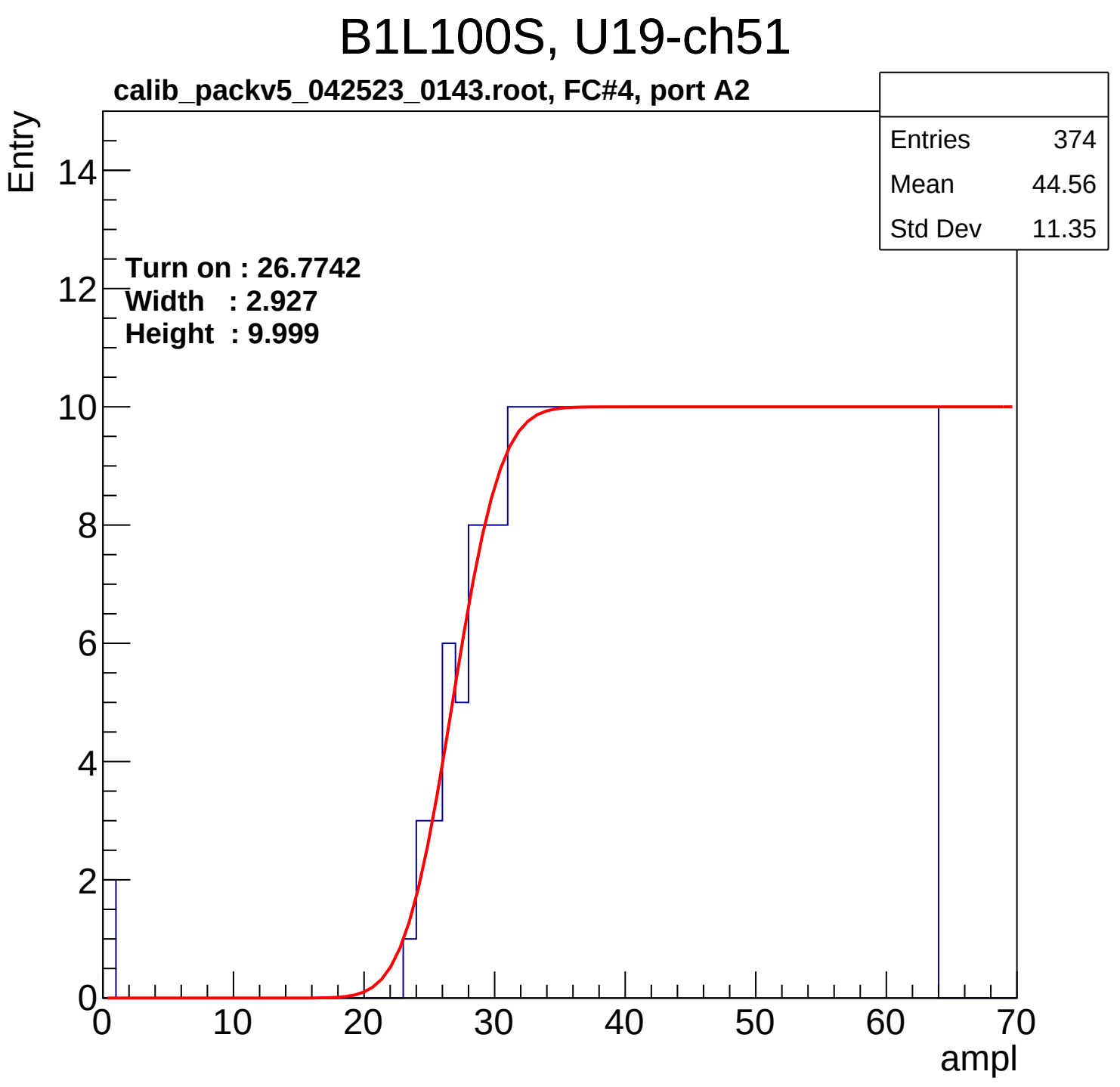
B1L100S, U19-ch51
calib_packv5_042523_0143.root, FC#4, port A2
Entries 374
Mean 44.56
Std Dev 11.35
Turn on : 26.7742
Width : 2.927
Height : 9.999
Entry
ampl
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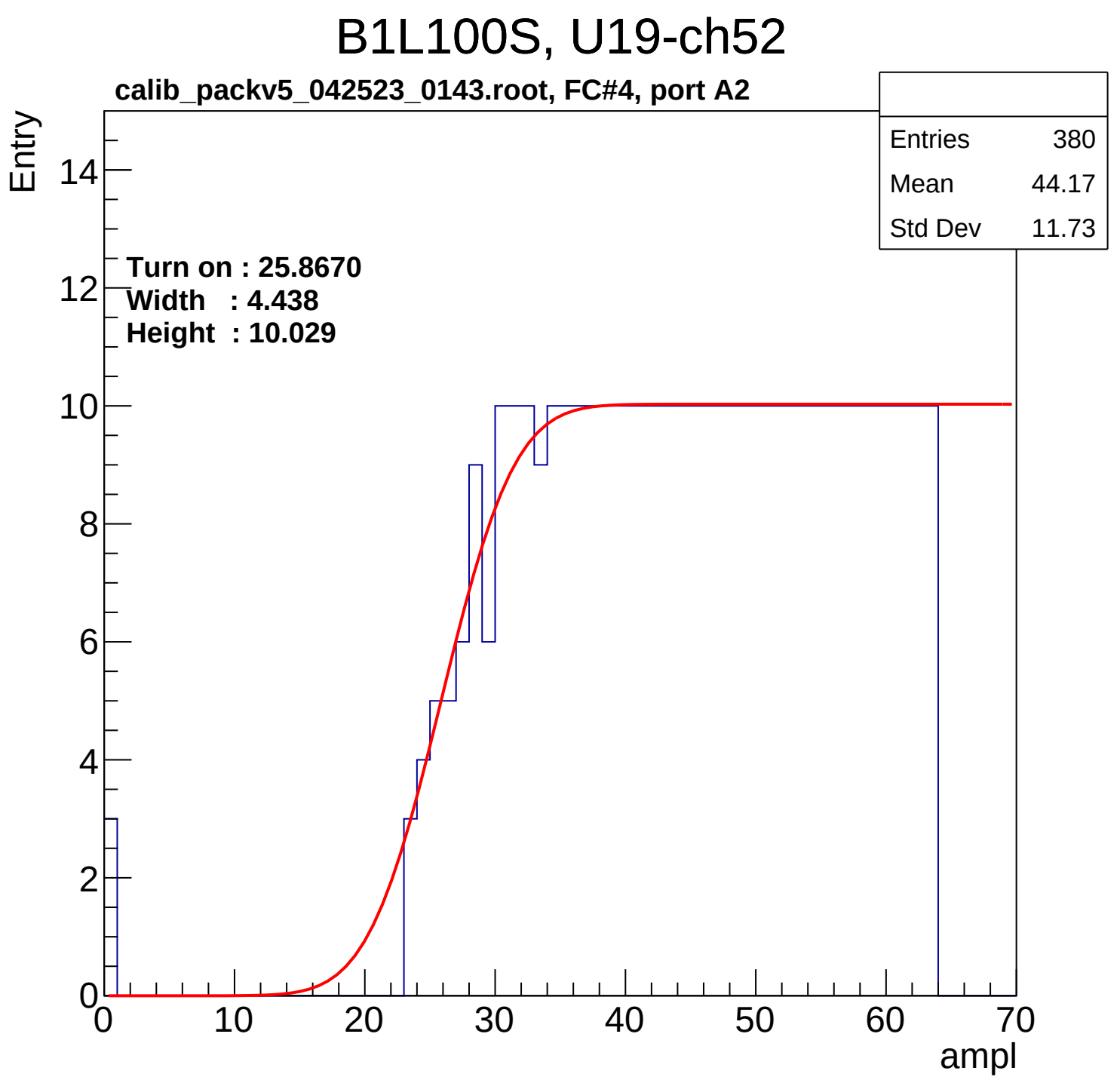
B1L100S, U19-ch52
calib_packv5_042523_0143.root, FC#4, port A2
Entries 380
Mean 44.17
Std Dev 11.73
Turn on : 25.8670
Width : 4.438
Height : 10.029
Entry
ampl
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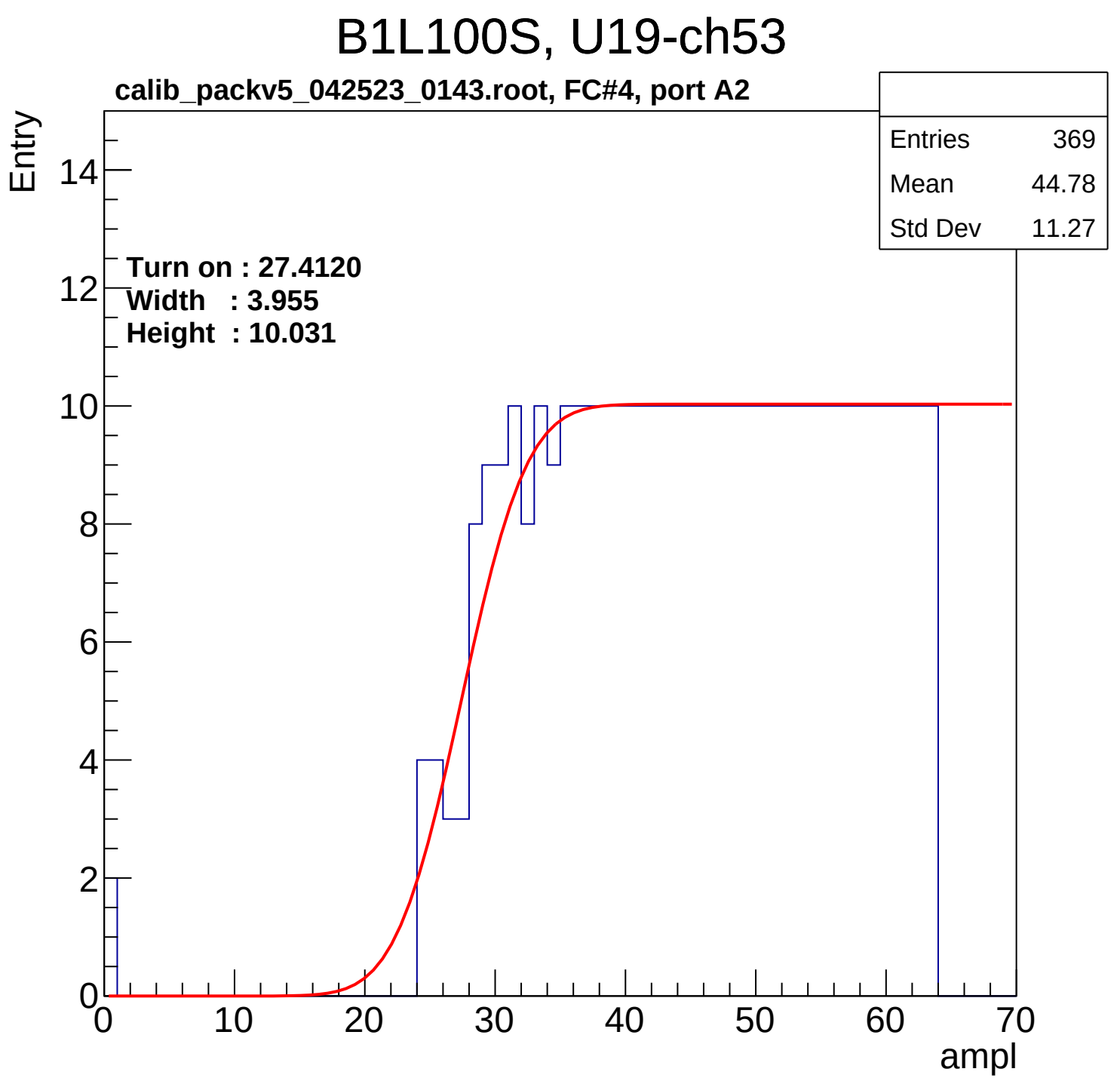
B1L100S, U19-ch53
calib_packv5_042523_0143.root, FC#4, port A2
Entries 369
Mean 44.78
Std Dev 11.27
Turn on : 27.4120
Width : 3.955
Height : 10.031
Entry
ampl
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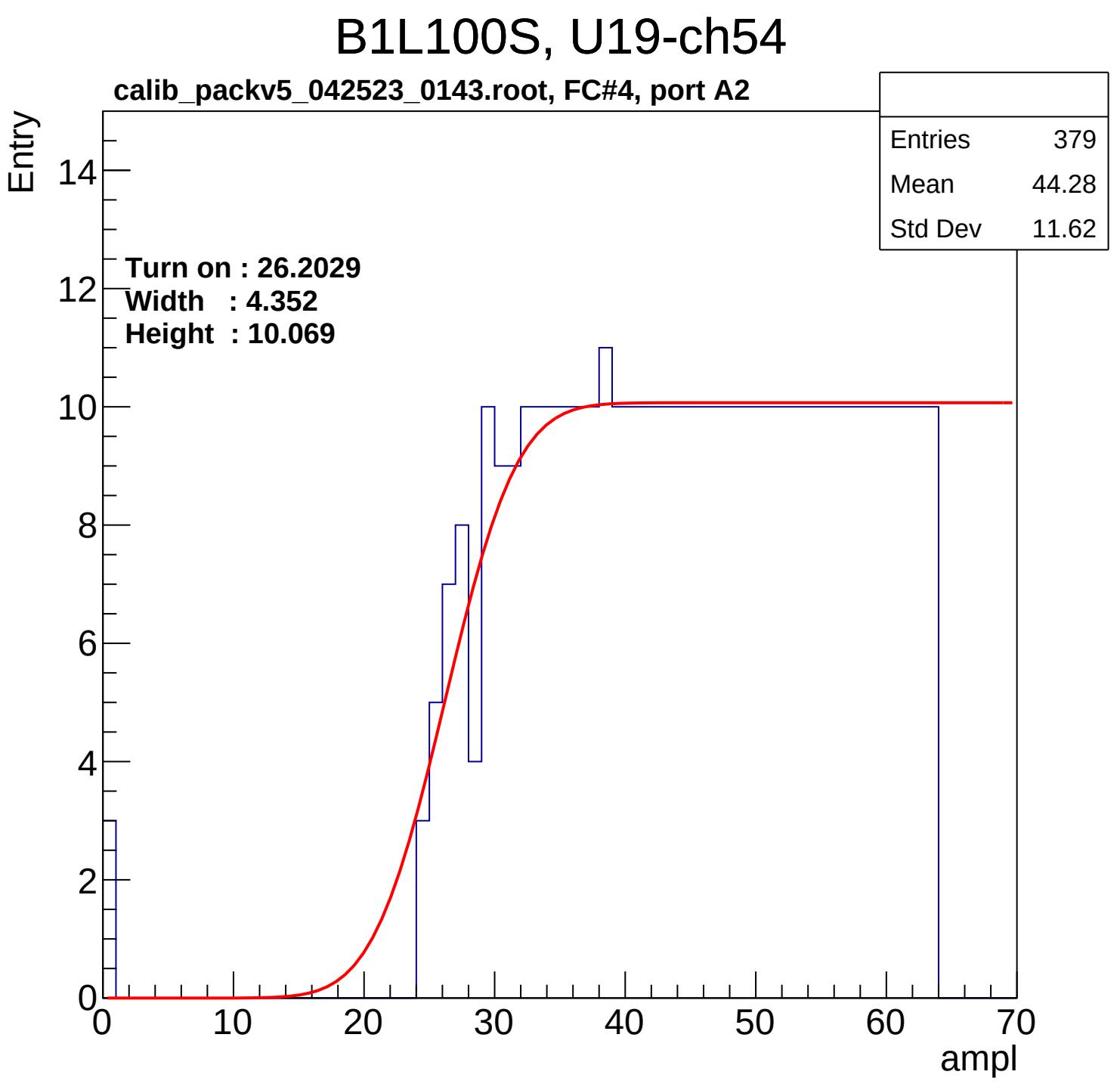
B1L100S, U19-ch54
calib_packv5_042523_0143.root, FC#4, port A2
Entries 379
Mean 44.28
Std Dev 11.62
Turn on : 26.2029
Width : 4.352
Height : 10.069
Entry
ampl
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2
4
6
8
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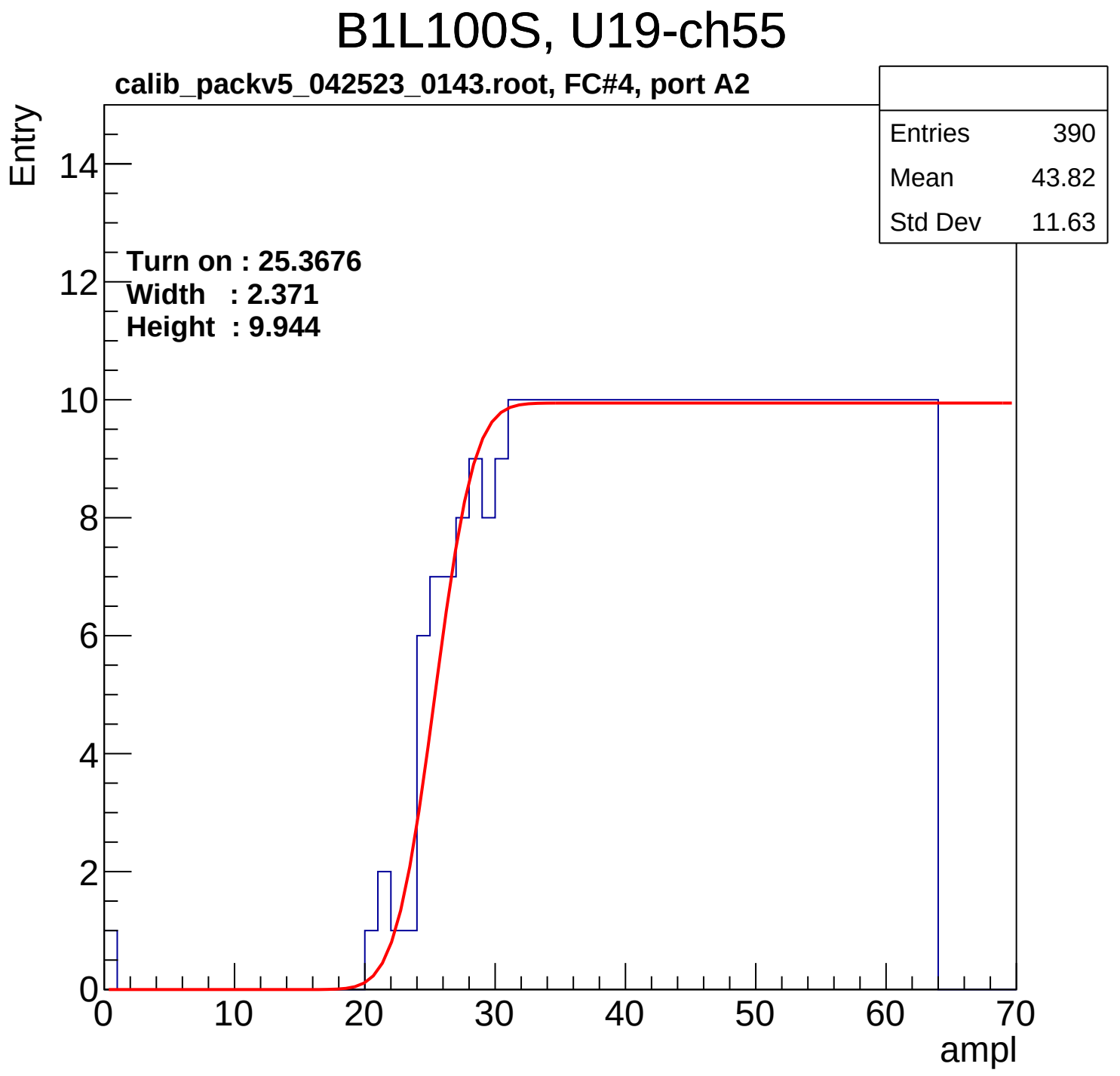
B1L100S, U19-ch55
calib_packv5_042523_0143.root, FC#4, port A2
Entries 390
Mean 43.82
Std Dev 11.63
Turn on : 25.3676
Width : 2.371
Height : 9.944
Entry
ampl
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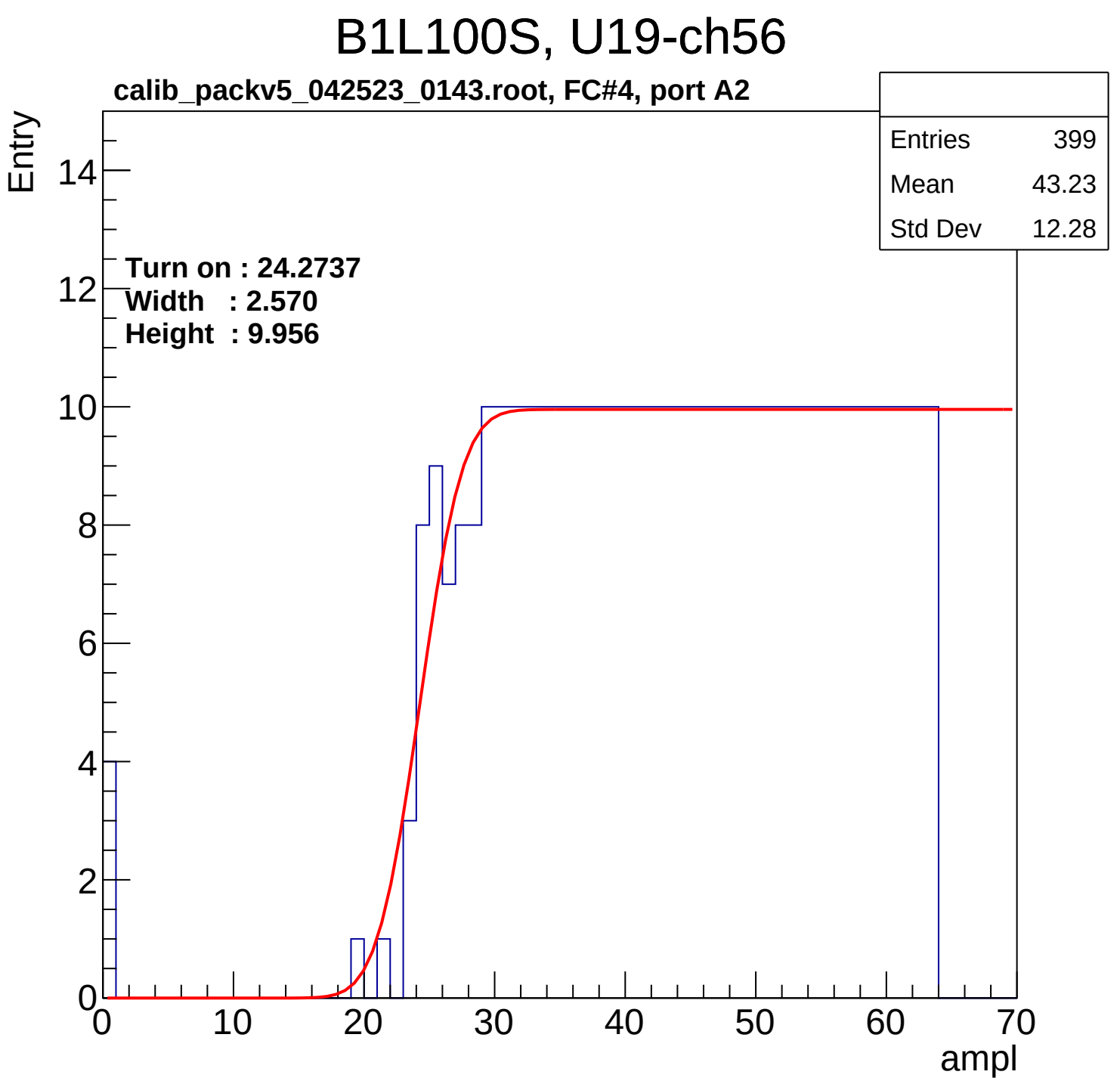
B1L100S, U19-ch56
calib_packv5_042523_0143.root, FC#4, port A2
Entries 399
Mean 43.23
Std Dev 12.28
Turn on : 24.2737
Width : 2.570
Height : 9.956
Entry
ampl
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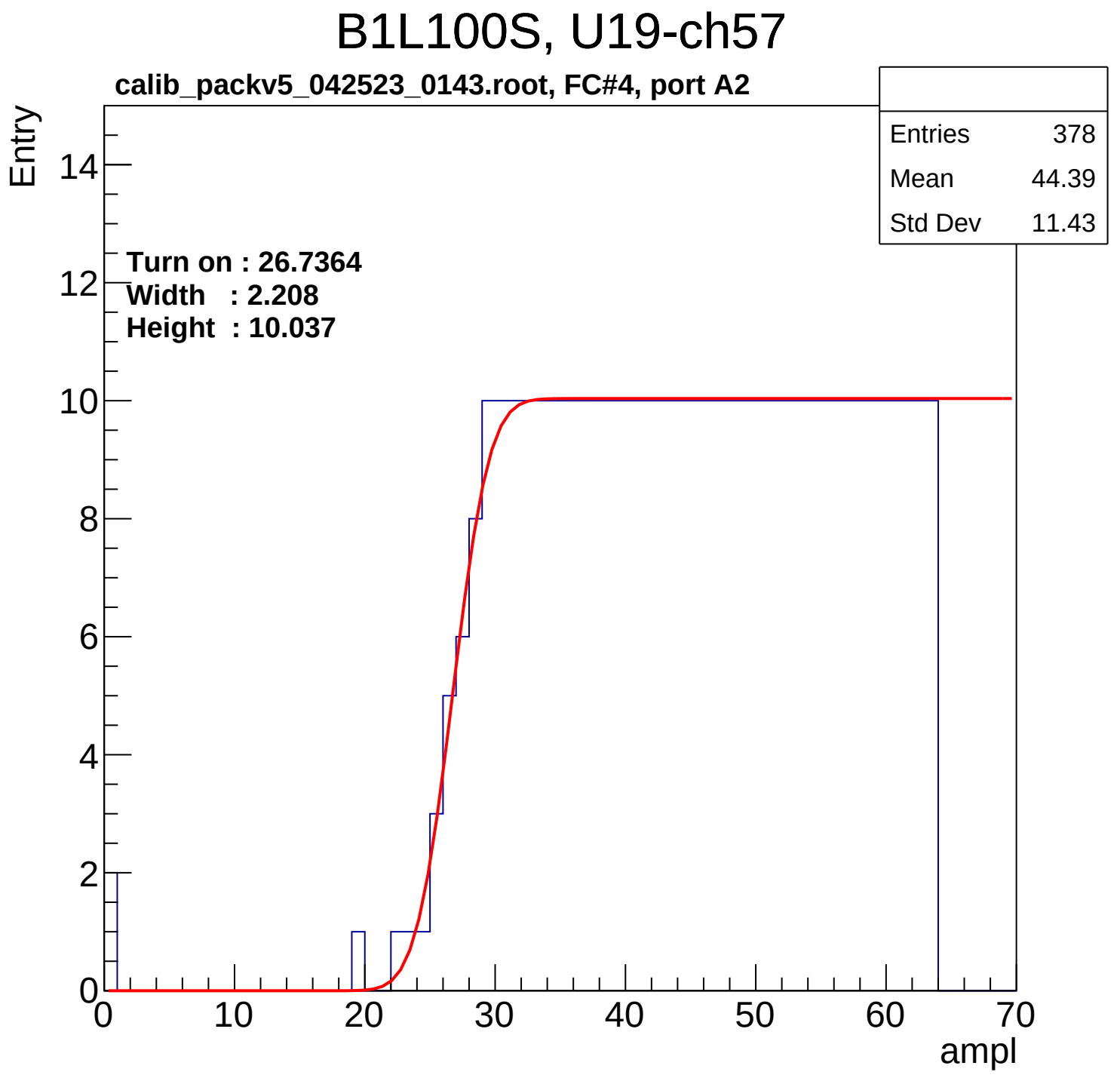
B1L100S, U19-ch57
calib_packv5_042523_0143.root, FC#4, port A2
Entries 378
Mean 44.39
Std Dev 11.43
Turn on : 26.7364
Width : 2.208
Height : 10.037
Entry
ampl
0
2
4
6
8
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12
14
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20
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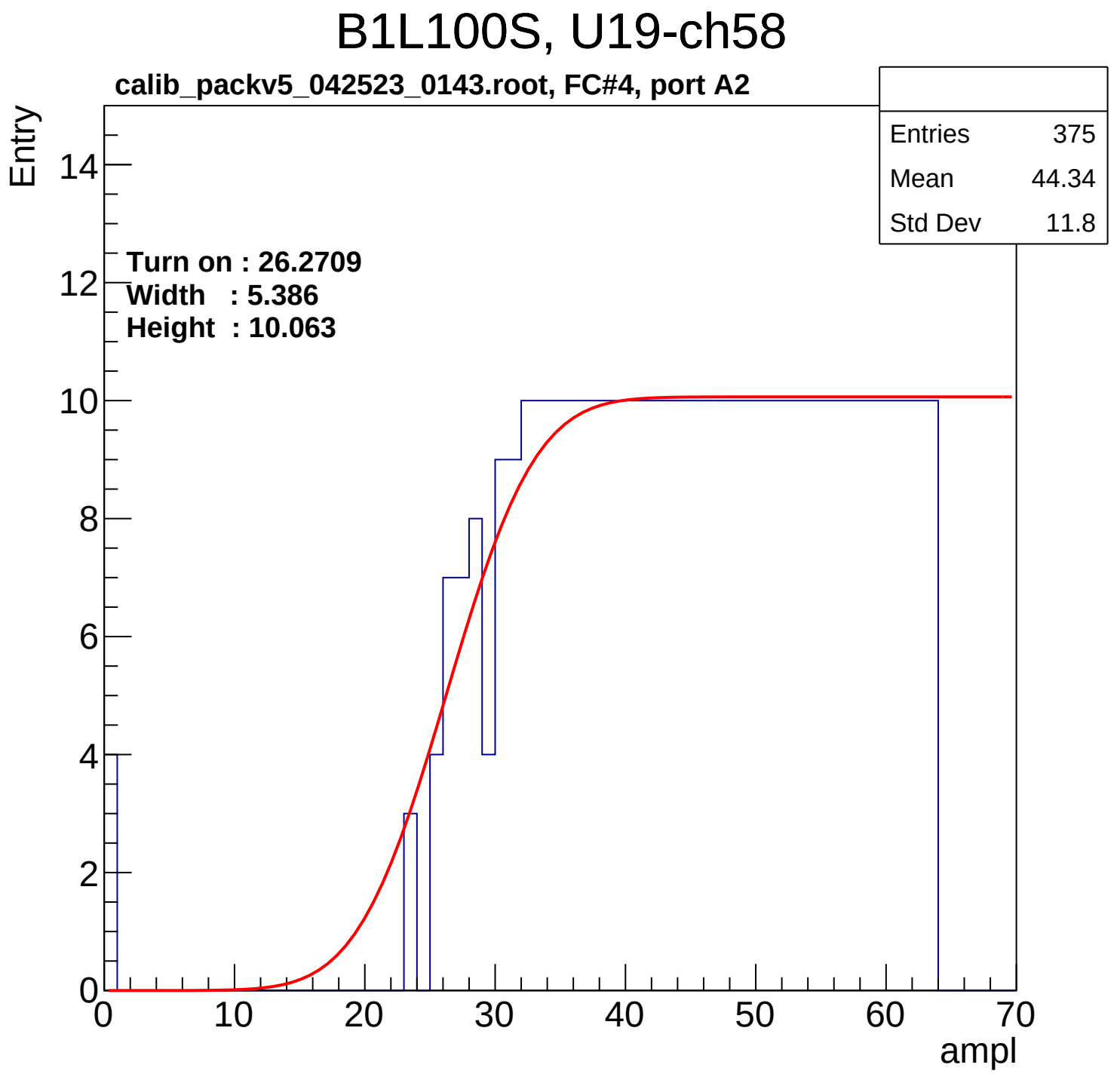
B1L100S, U19-ch58
calib_packv5_042523_0143.root, FC#4, port A2
Entries 375
Mean 44.34
Std Dev 11.8
Turn on : 26.2709
Width : 5.386
Height : 10.063
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ampl
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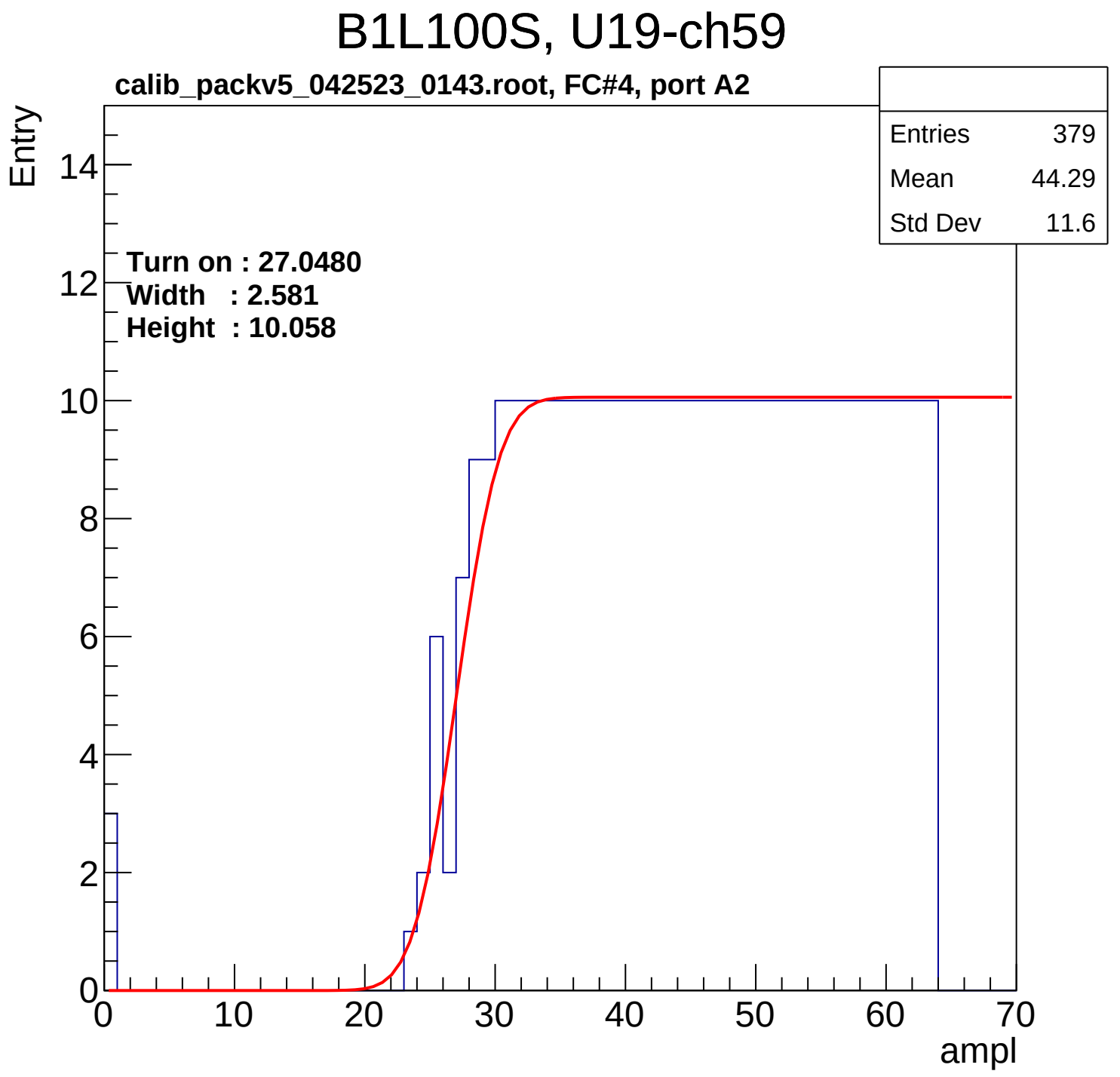
B1L100S, U19-ch59
calib_packv5_042523_0143.root, FC#4, port A2
Entries 379
Mean 44.29
Std Dev 11.6
Turn on : 27.0480
Width : 2.581
Height : 10.058
Entry
ampl
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6
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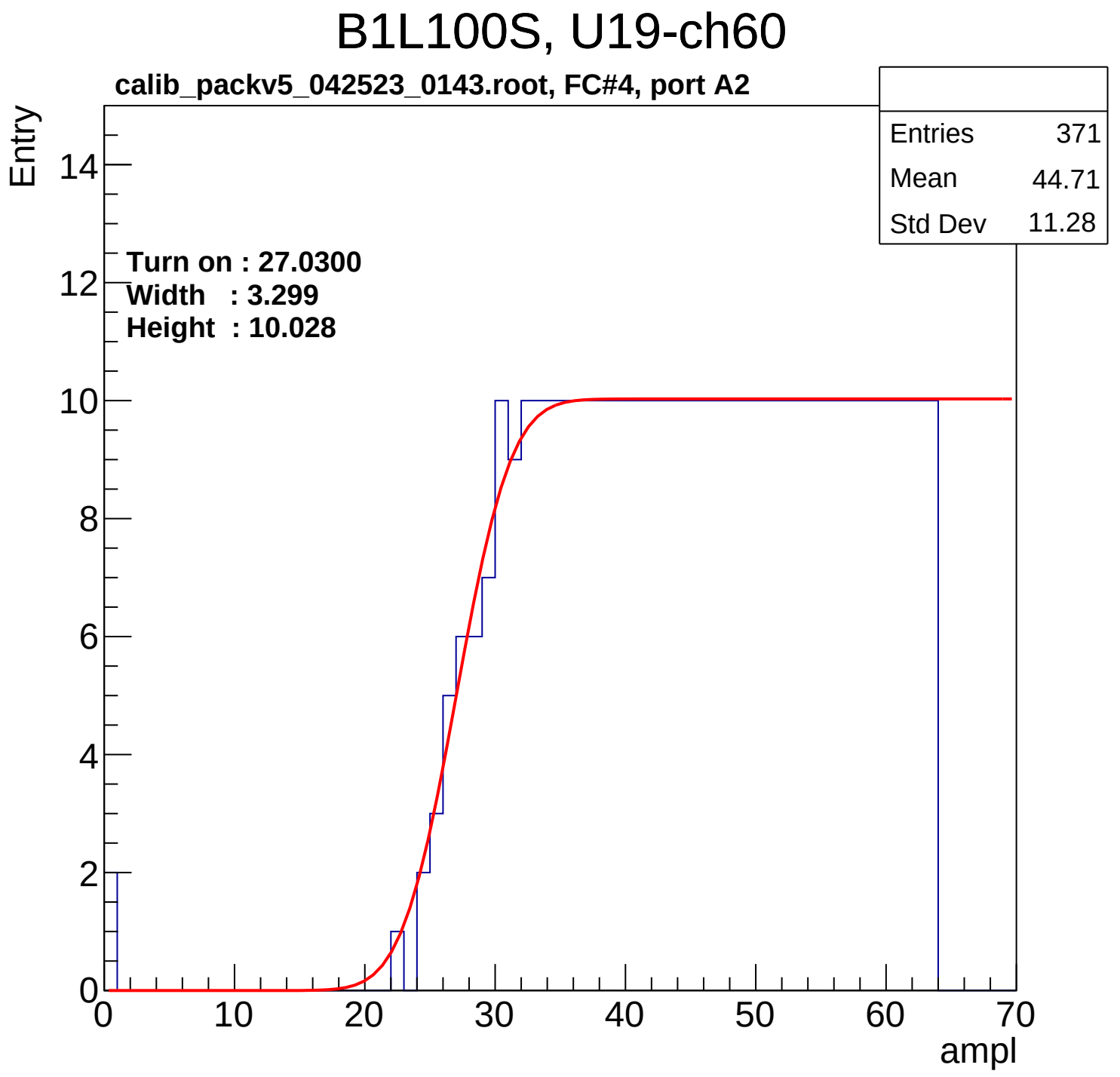
B1L100S, U19-ch60
calib_packv5_042523_0143.root, FC#4, port A2
Entries 371
Mean 44.71
Std Dev 11.28
Turn on : 27.0300
Width : 3.299
Height : 10.028
Entry
ampl
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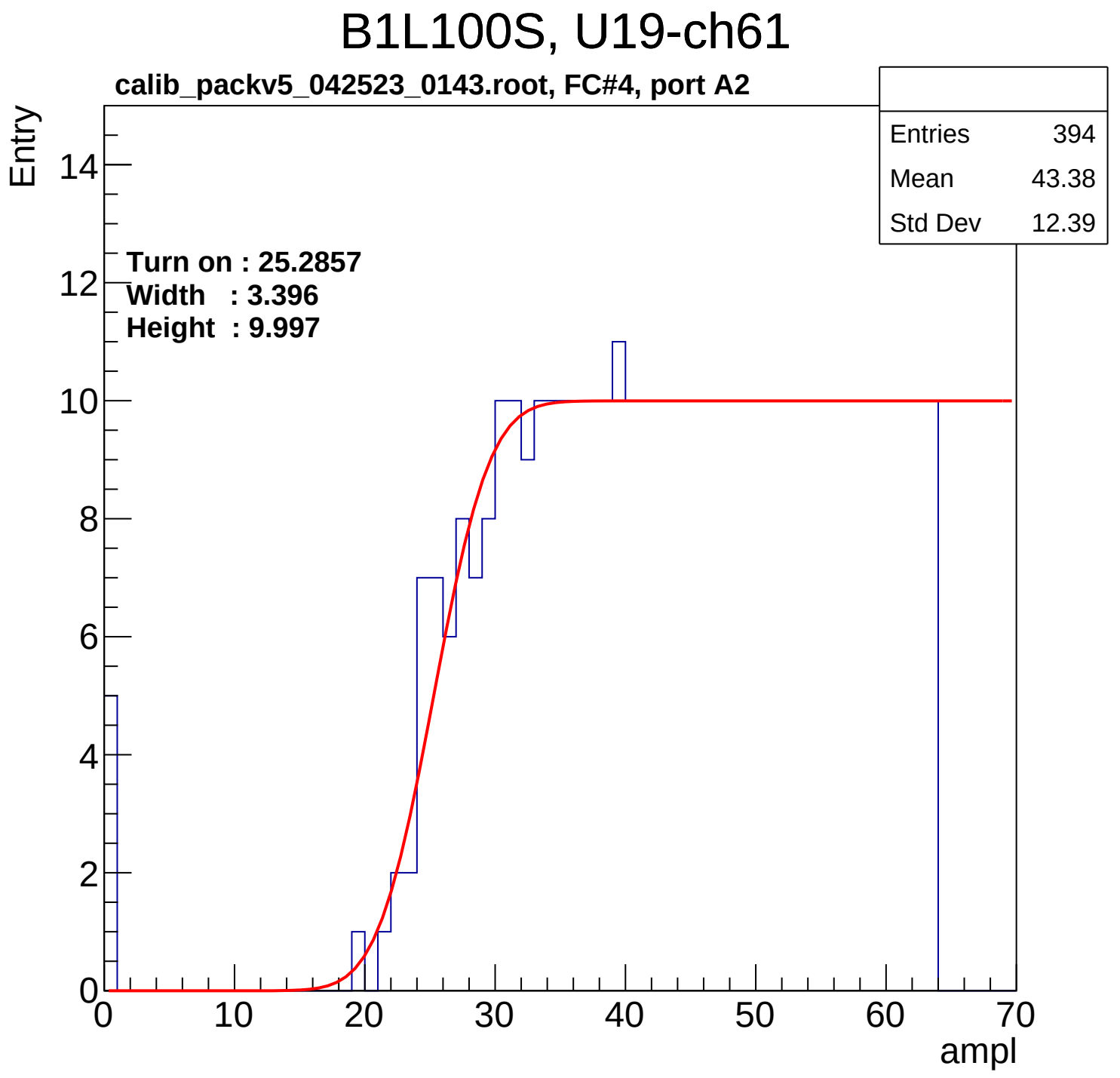
B1L100S, U19-ch61
calib_packv5_042523_0143.root, FC#4, port A2
Entries 394
Mean 43.38
Std Dev 12.39
Turn on : 25.2857
Width : 3.396
Height : 9.997
Entry
ampl
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4
6
8
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0
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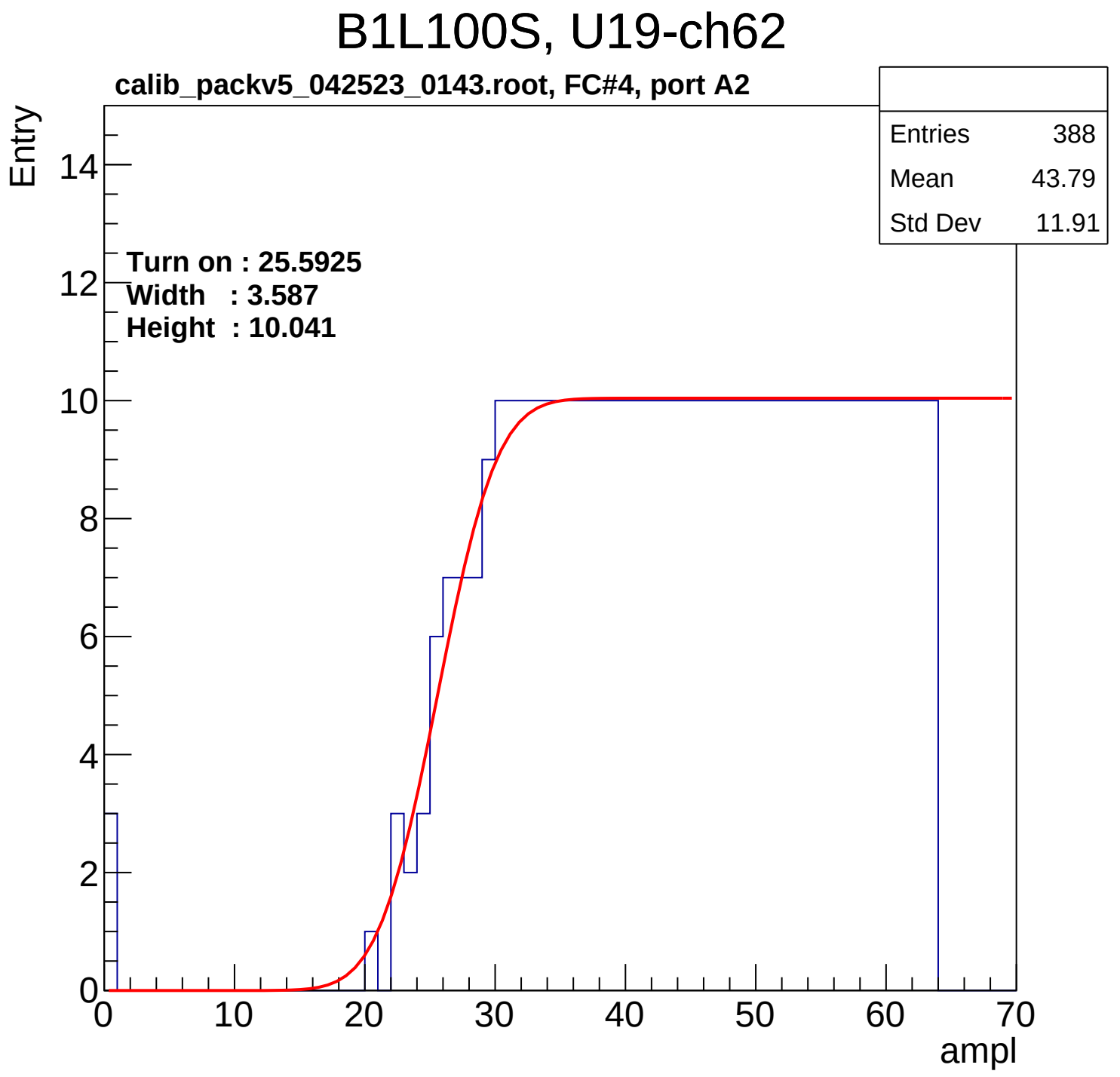
B1L100S, U19-ch62
calib_packv5_042523_0143.root, FC#4, port A2
Entries 388
Mean 43.79
Std Dev 11.91
Turn on : 25.5925
Width : 3.587
Height : 10.041
Entry
ampl
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4
6
8
10
12
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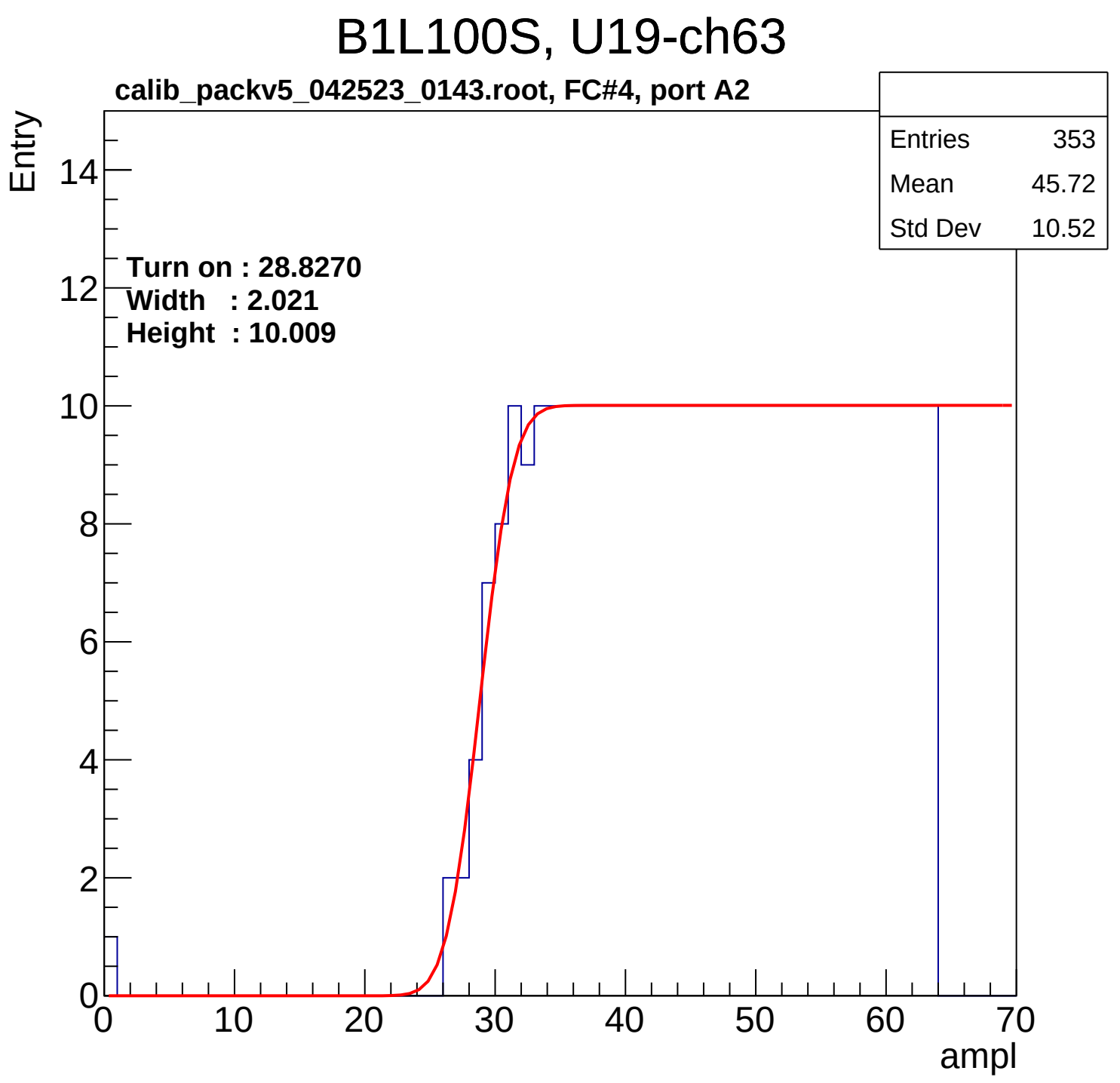
B1L100S, U19-ch63
calib_packv5_042523_0143.root, FC#4, port A2
Entries 353
Mean 45.72
Std Dev 10.52
Turn on : 28.8270
Width : 2.021
Height : 10.009
Entry
ampl
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6
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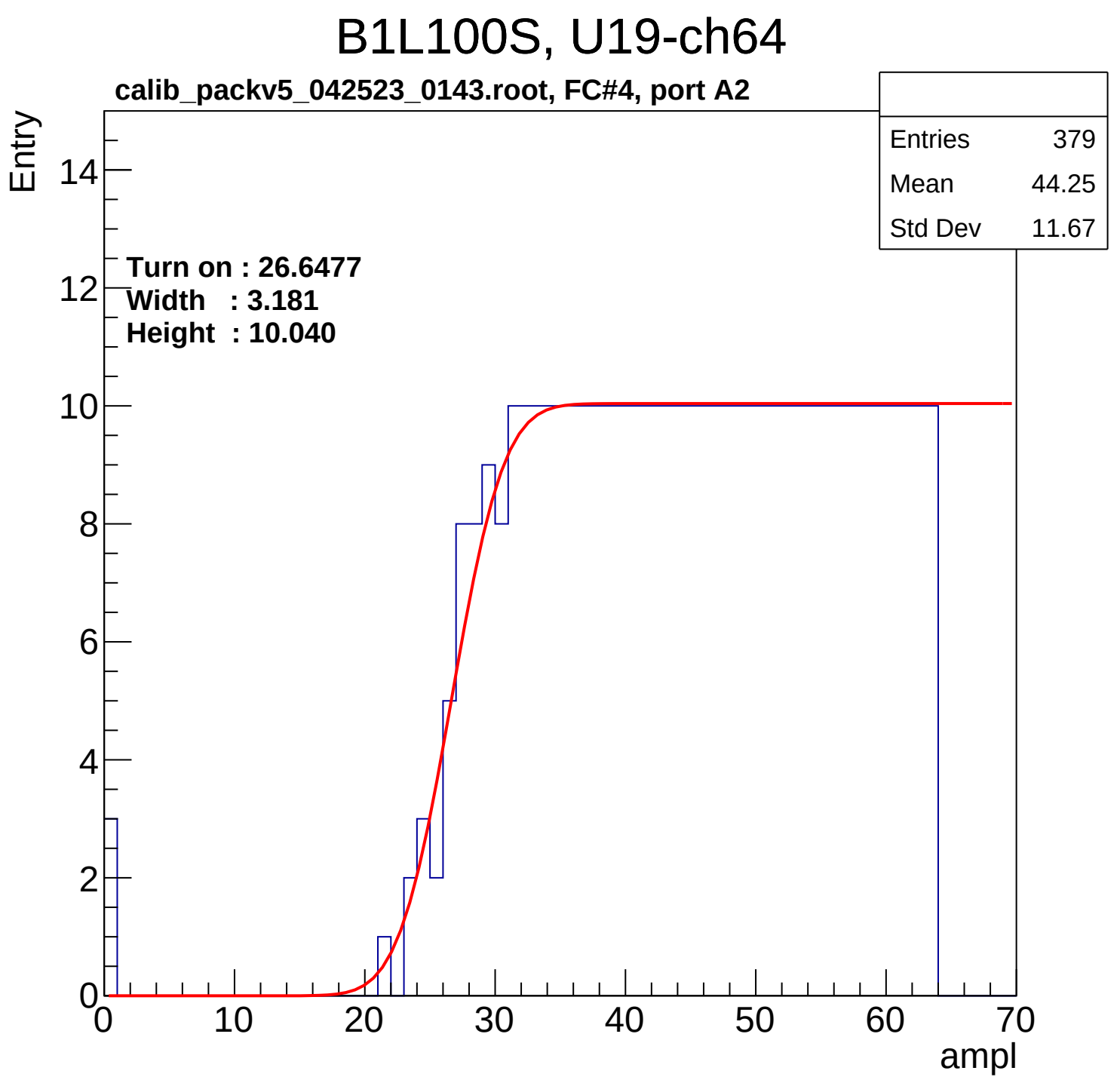
B1L100S, U19-ch64
calib_packv5_042523_0143.root, FC#4, port A2
Entries 379
Mean 44.25
Std Dev 11.67
Turn on : 26.6477
Width : 3.181
Height : 10.040
Entry
ampl
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6
8
10
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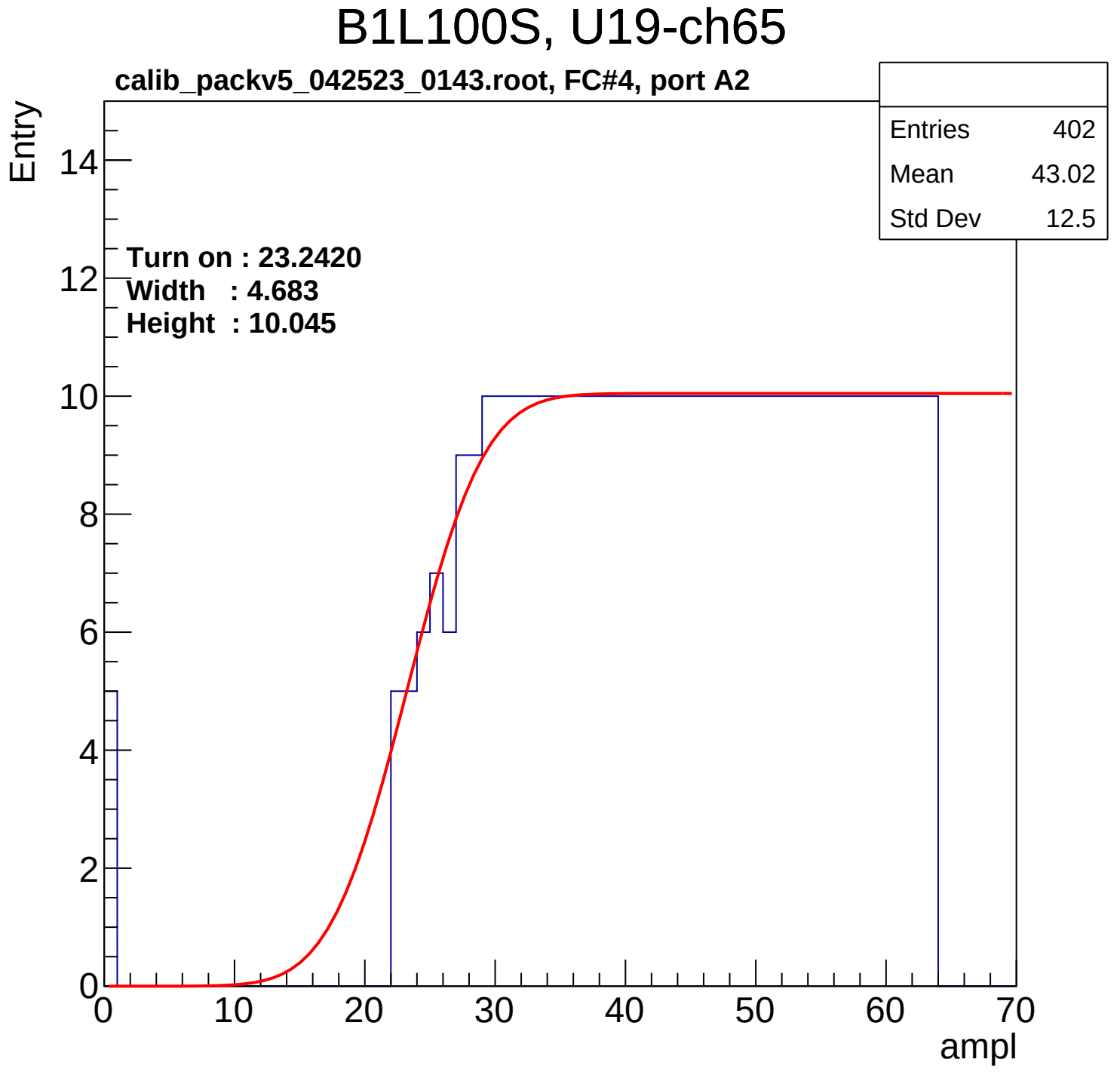
B1L100S, U19-ch65
calib_packv5_042523_0143.root, FC#4, port A2
Entries 402
Mean 43.02
Std Dev 12.5
Turn on : 23.2420
Width : 4.683
Height : 10.045
Entry
ampl
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4
6
8
10
12
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0
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60
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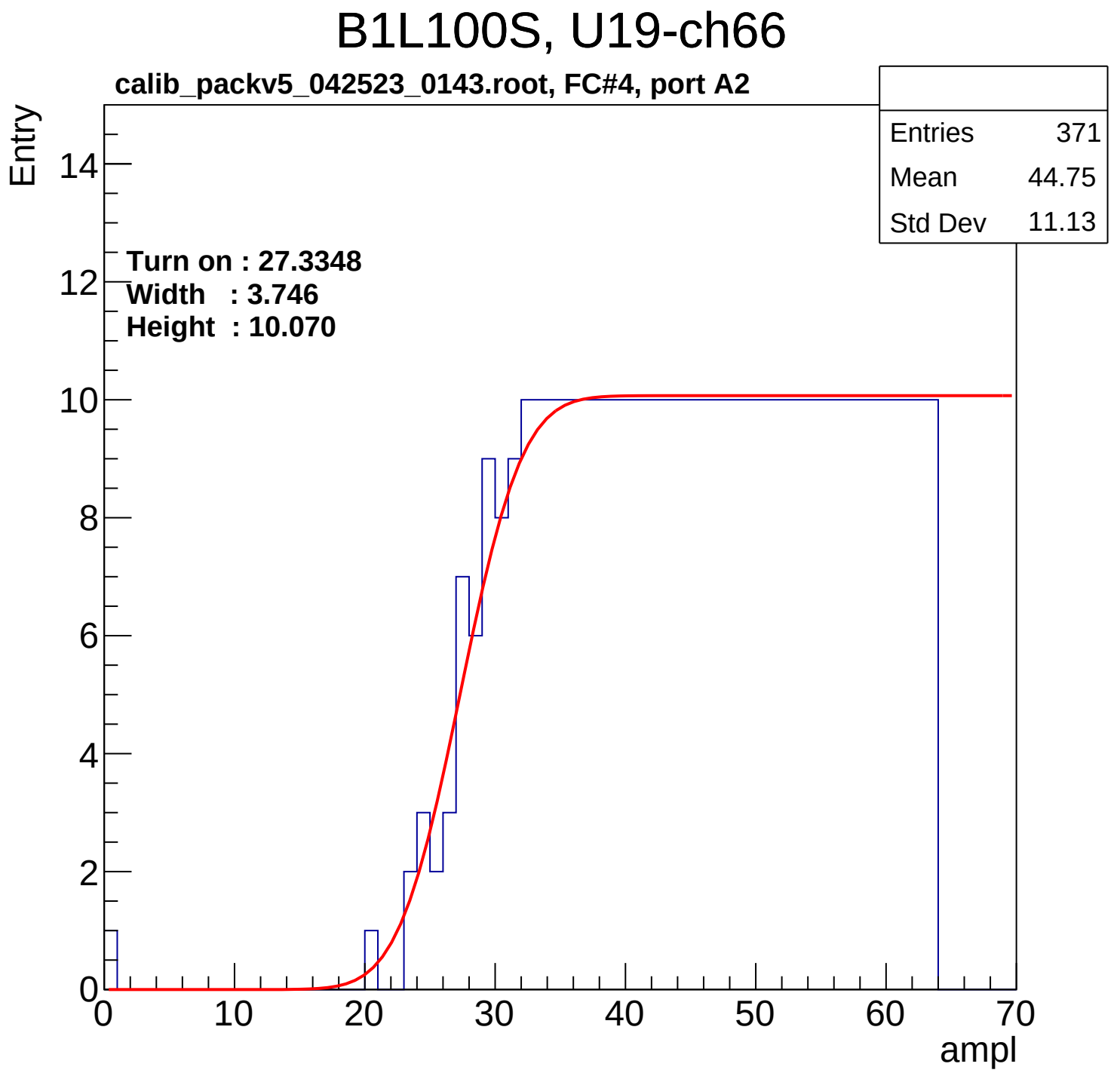
B1L100S, U19-ch66
calib_packv5_042523_0143.root, FC#4, port A2
Entries 371
Mean 44.75
Std Dev 11.13
Turn on : 27.3348
Width : 3.746
Height : 10.070
Entry
ampl
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6
8
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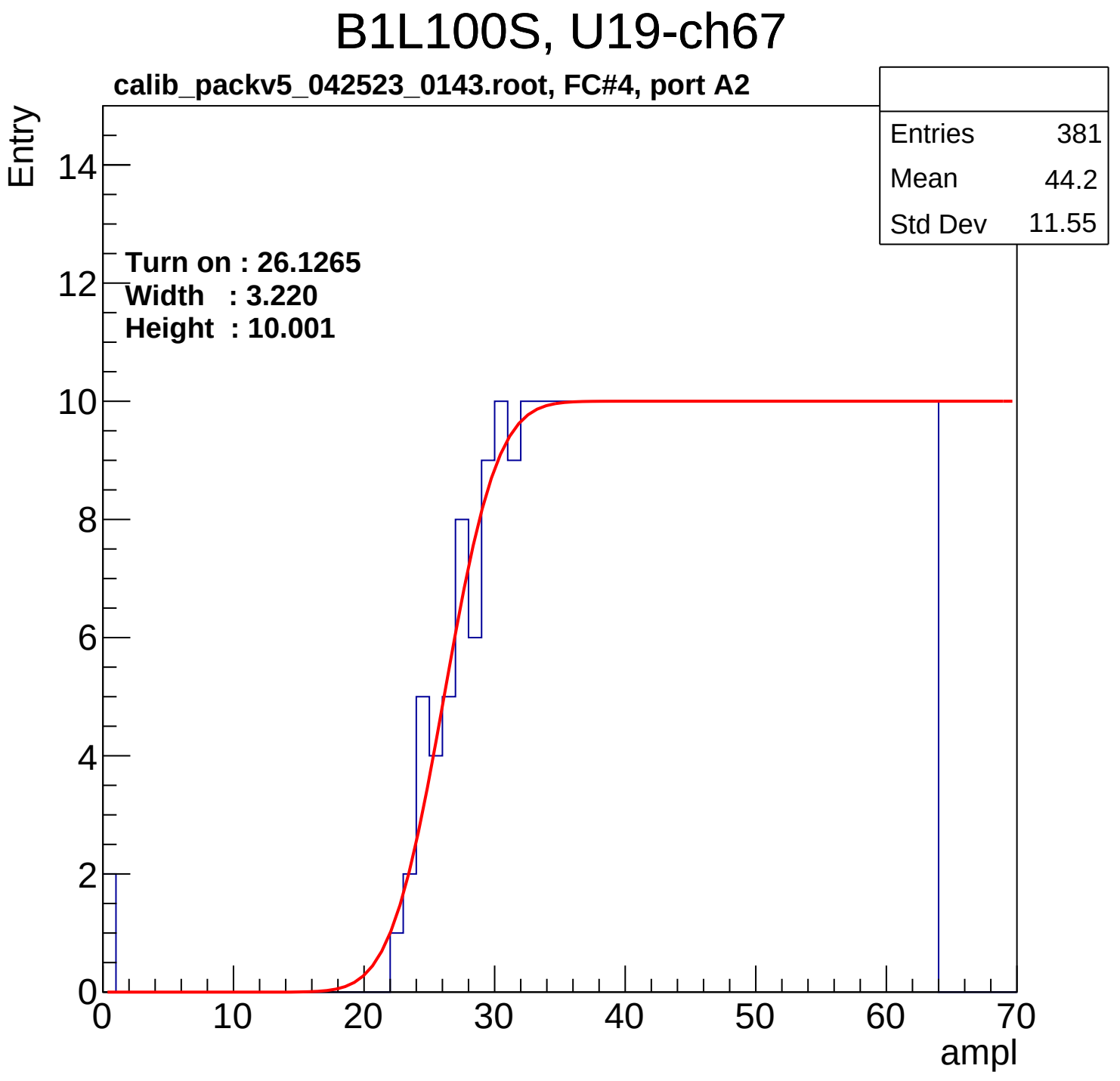
B1L100S, U19-ch67
calib_packv5_042523_0143.root, FC#4, port A2
Entries 381
Mean 44.2
Std Dev 11.55
Turn on : 26.1265
Width : 3.220
Height : 10.001
Entry
ampl
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6
8
10
12
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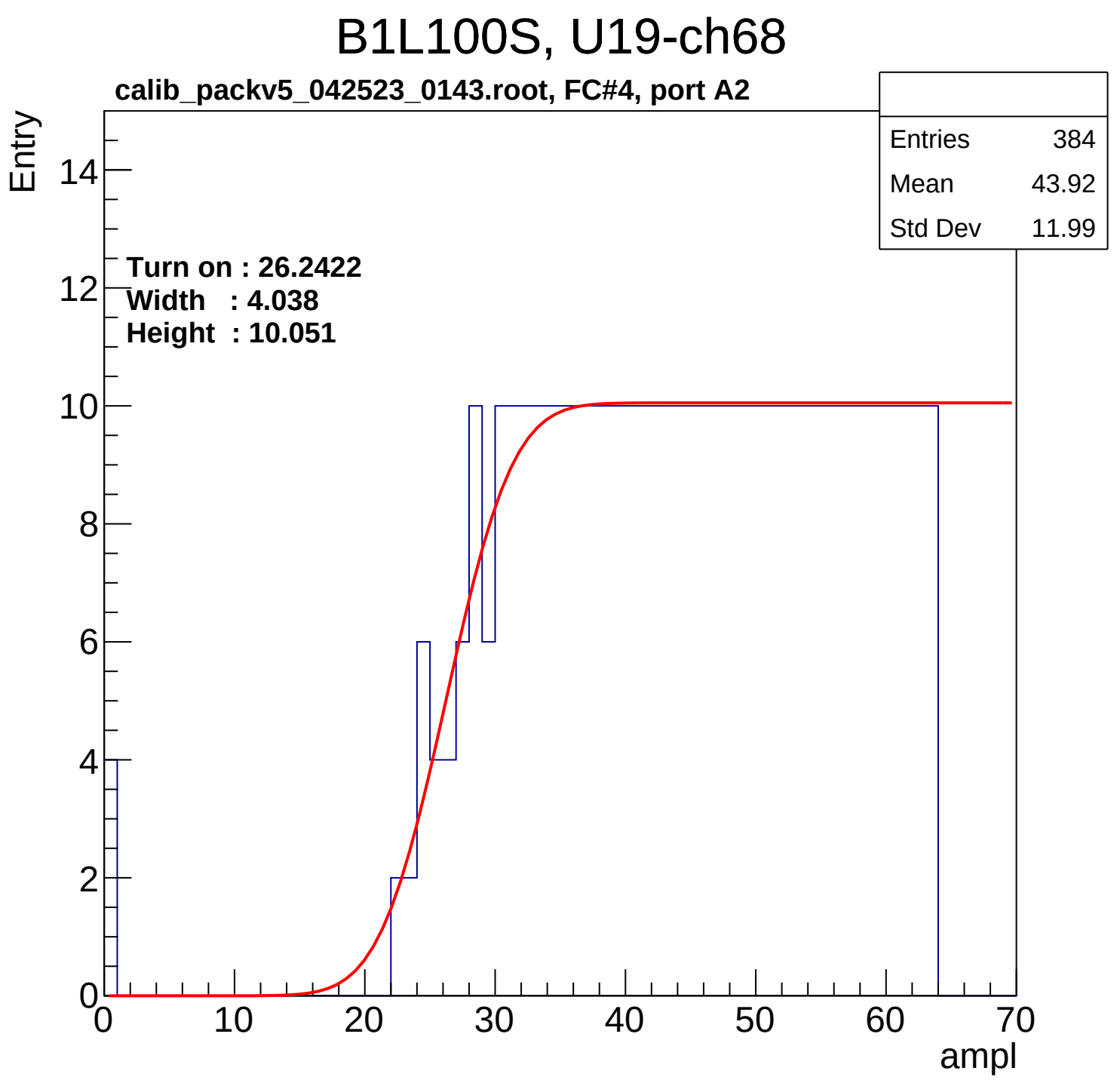
B1L100S, U19-ch68
calib_packv5_042523_0143.root, FC#4, port A2
Entries 384
Mean 43.92
Std Dev 11.99
Turn on : 26.2422
Width : 4.038
Height : 10.051
Entry
ampl
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8
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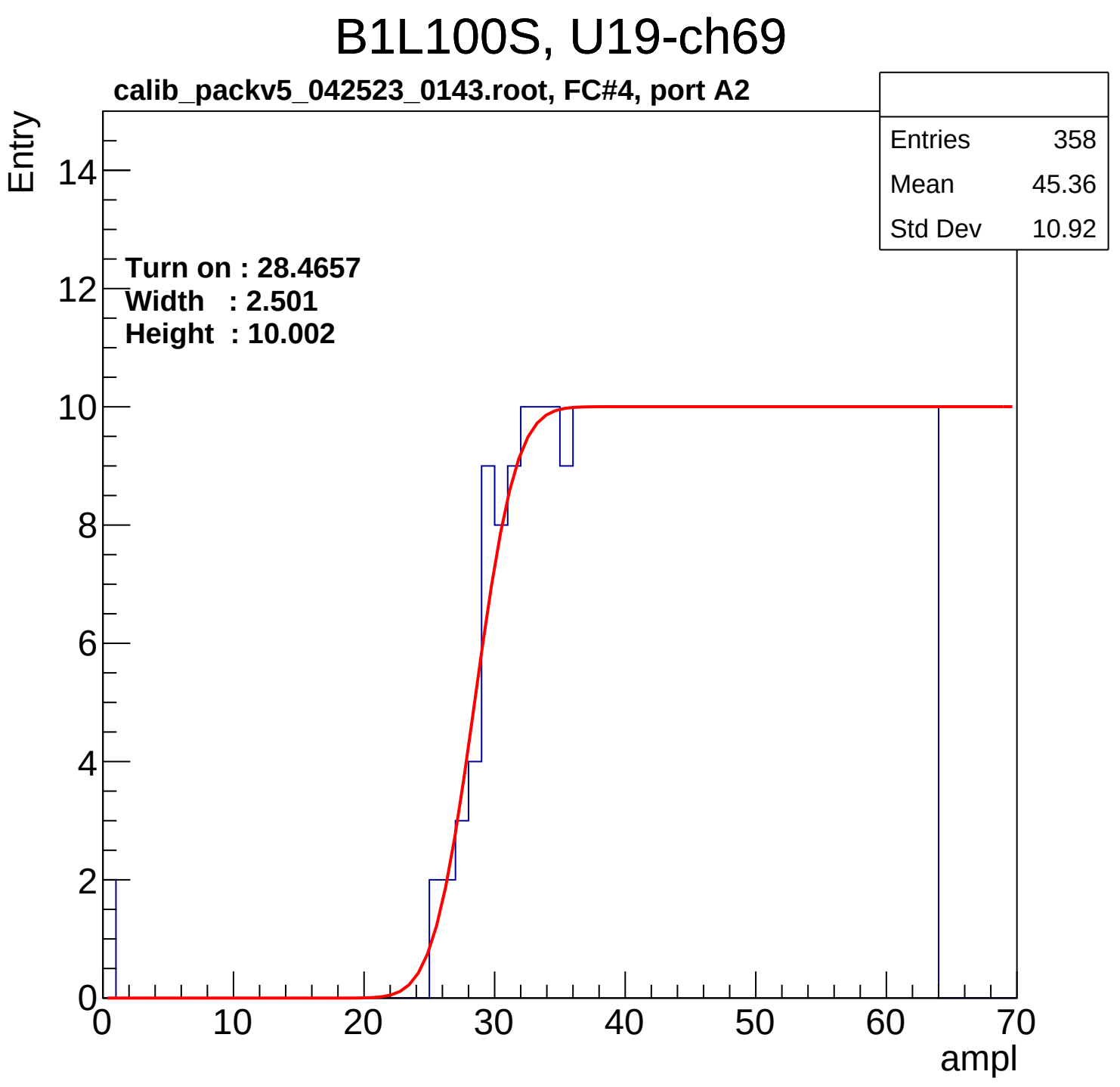
B1L100S, U19-ch69
calib_packv5_042523_0143.root, FC#4, port A2
Entries 358
Mean 45.36
Std Dev 10.92
Turn on : 28.4657
Width : 2.501
Height : 10.002
Entry
ampl
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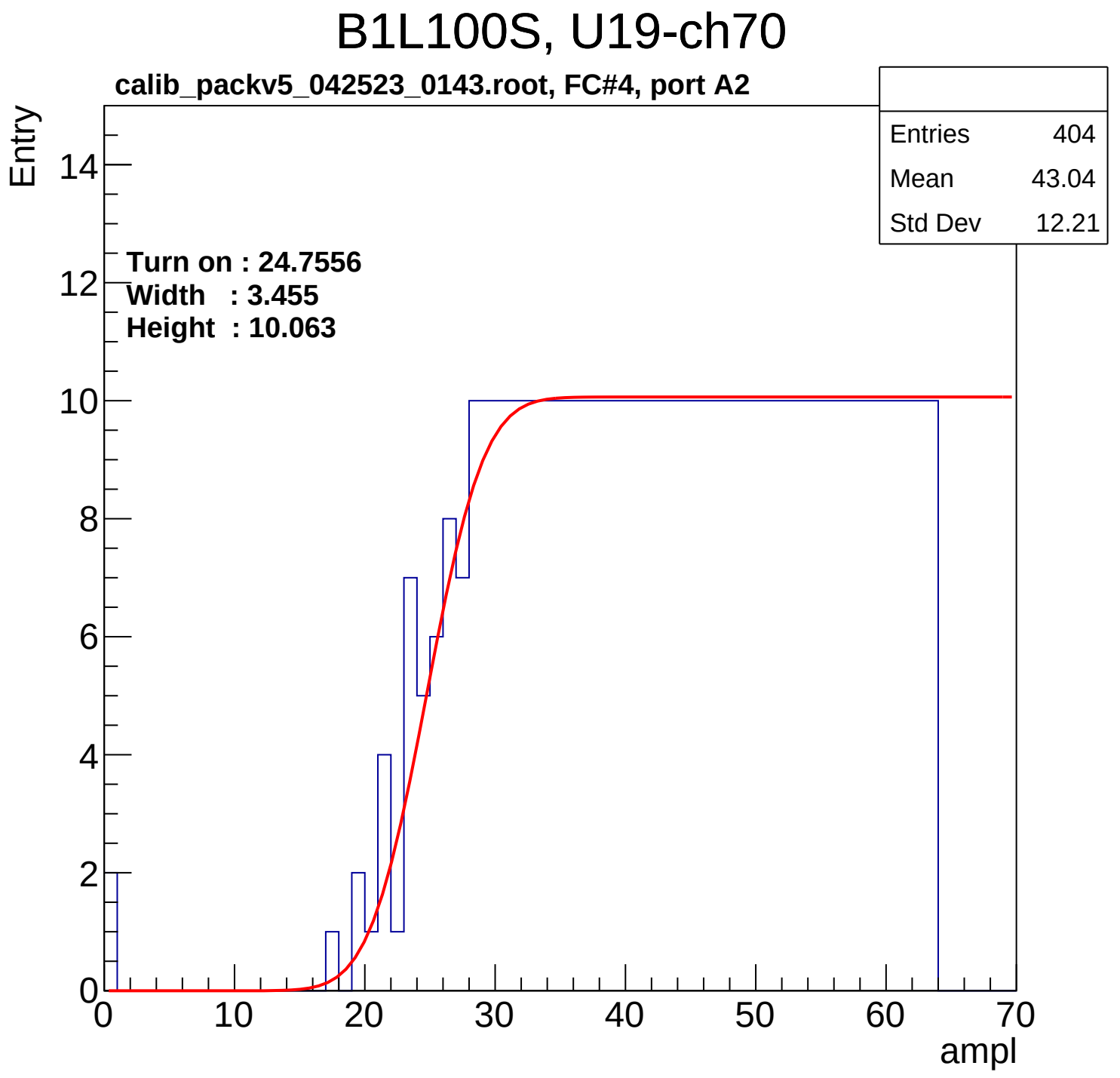
B1L100S, U19-ch70
calib_packv5_042523_0143.root, FC#4, port A2
Entries 404
Mean 43.04
Std Dev 12.21
Turn on : 24.7556
Width : 3.455
Height : 10.063
Entry
ampl
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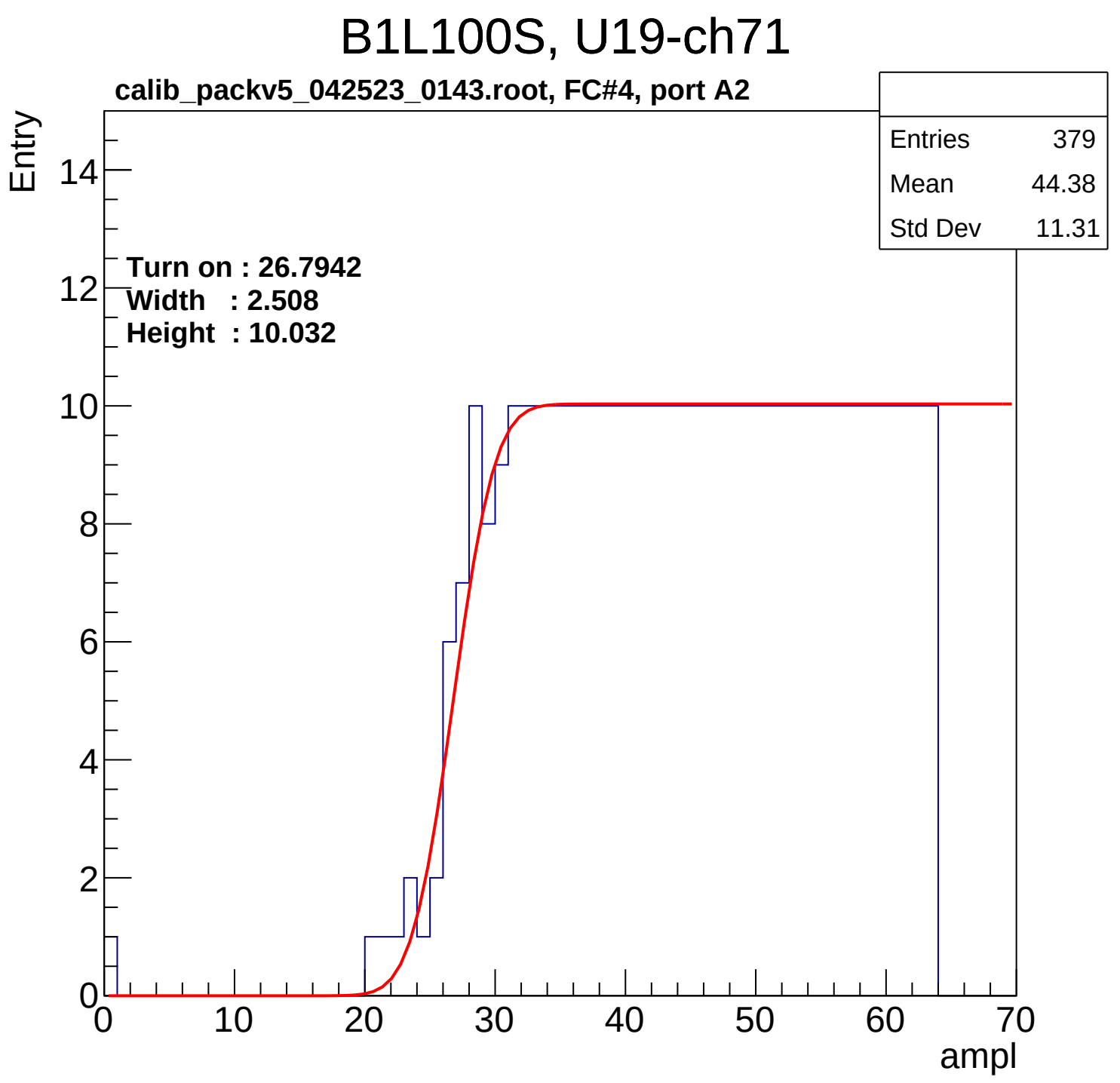
B1L100S, U19-ch71
calib_packv5_042523_0143.root, FC#4, port A2
Entries 379
Mean 44.38
Std Dev 11.31
Turn on : 26.7942
Width : 2.508
Height : 10.032
Entry
ampl
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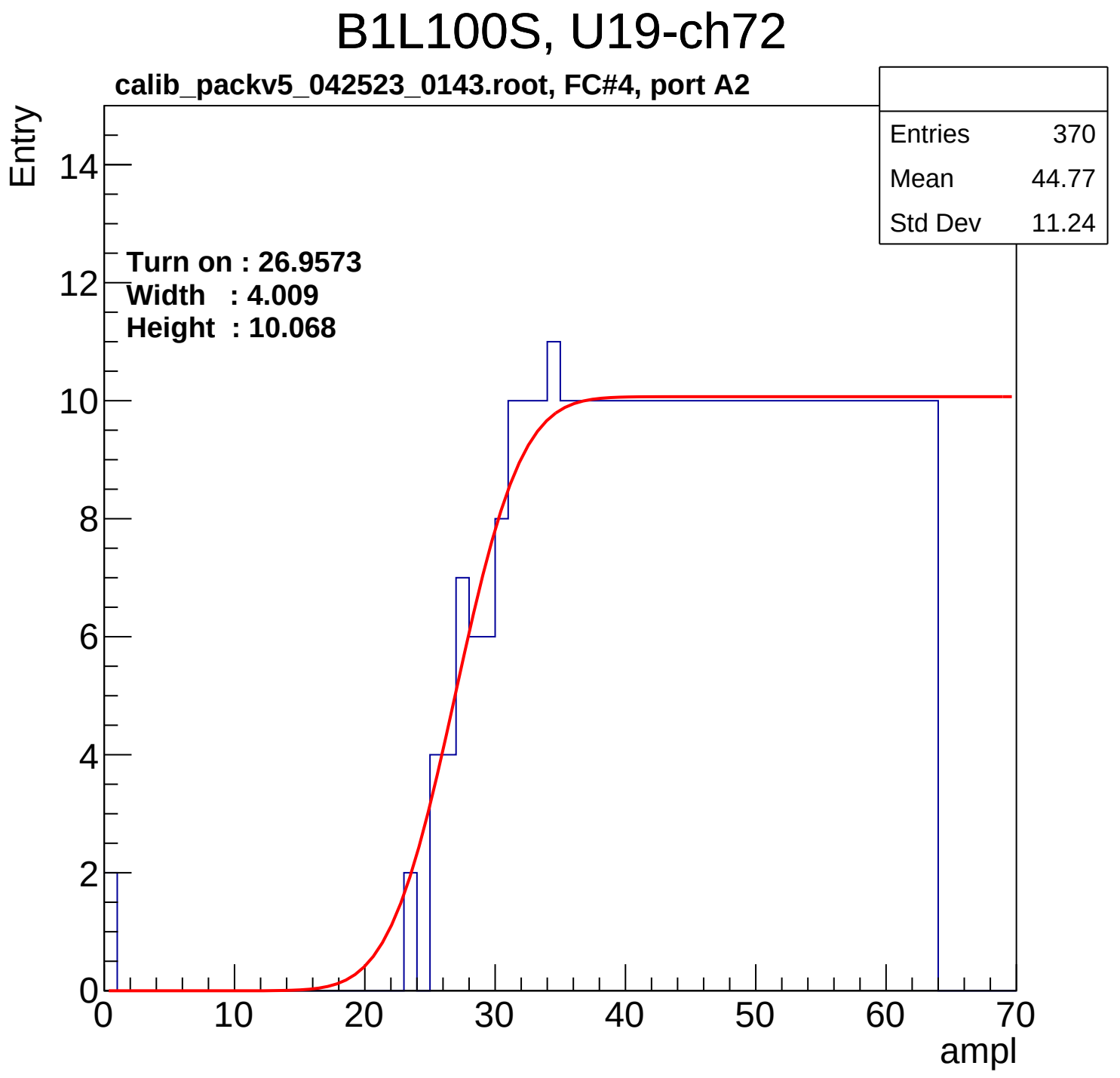
B1L100S, U19-ch72
calib_packv5_042523_0143.root, FC#4, port A2
Entries 370
Mean 44.77
Std Dev 11.24
Turn on : 26.9573
Width : 4.009
Height : 10.068
Entry
ampl
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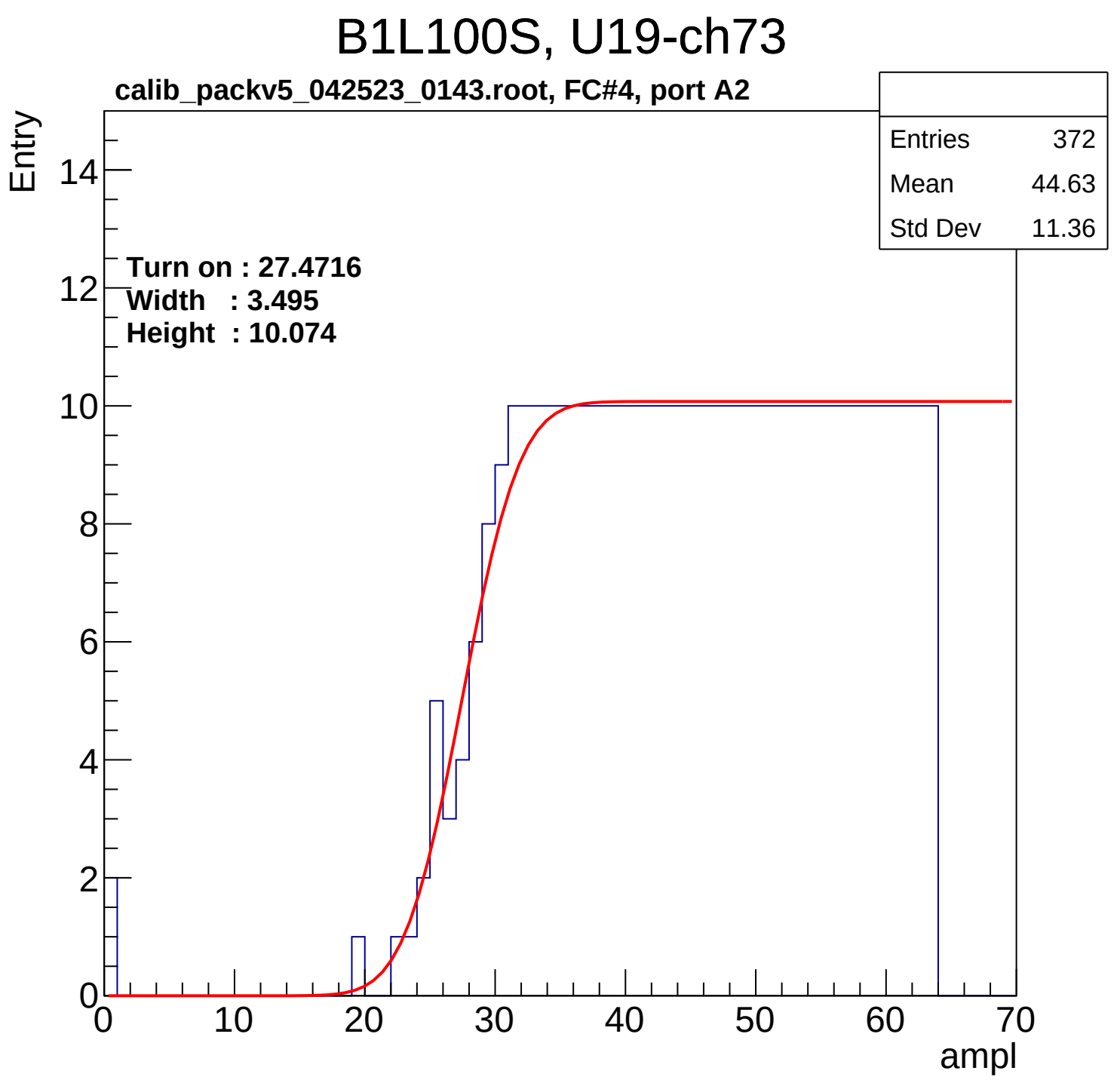
B1L100S, U19-ch73
calib_packv5_042523_0143.root, FC#4, port A2
Entries 372
Mean 44.63
Std Dev 11.36
Turn on : 27.4716
Width : 3.495
Height : 10.074
Entry
ampl
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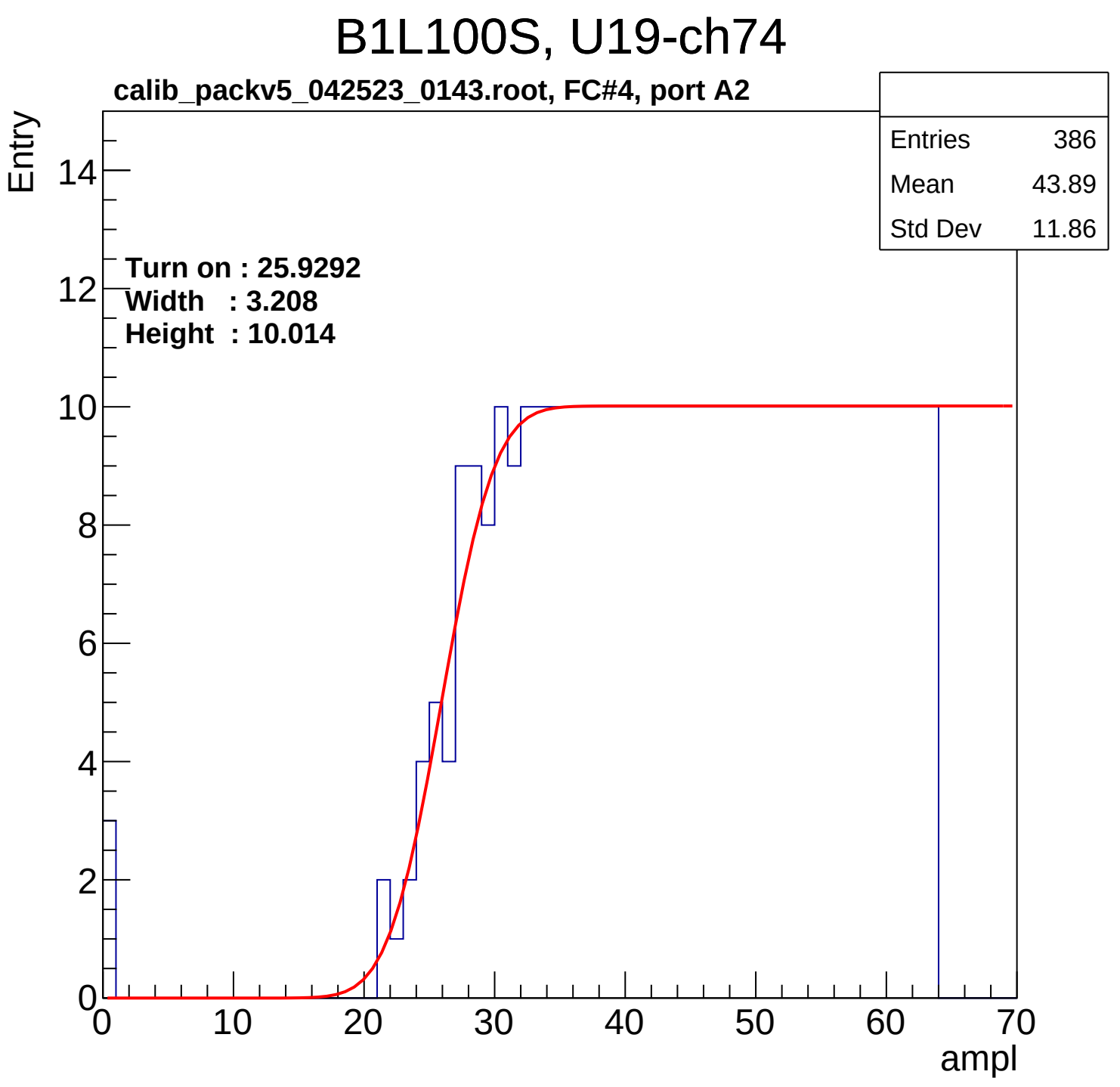
B1L100S, U19-ch74
calib_packv5_042523_0143.root, FC#4, port A2
Entries 386
Mean 43.89
Std Dev 11.86
Turn on : 25.9292
Width : 3.208
Height : 10.014
Entry
ampl
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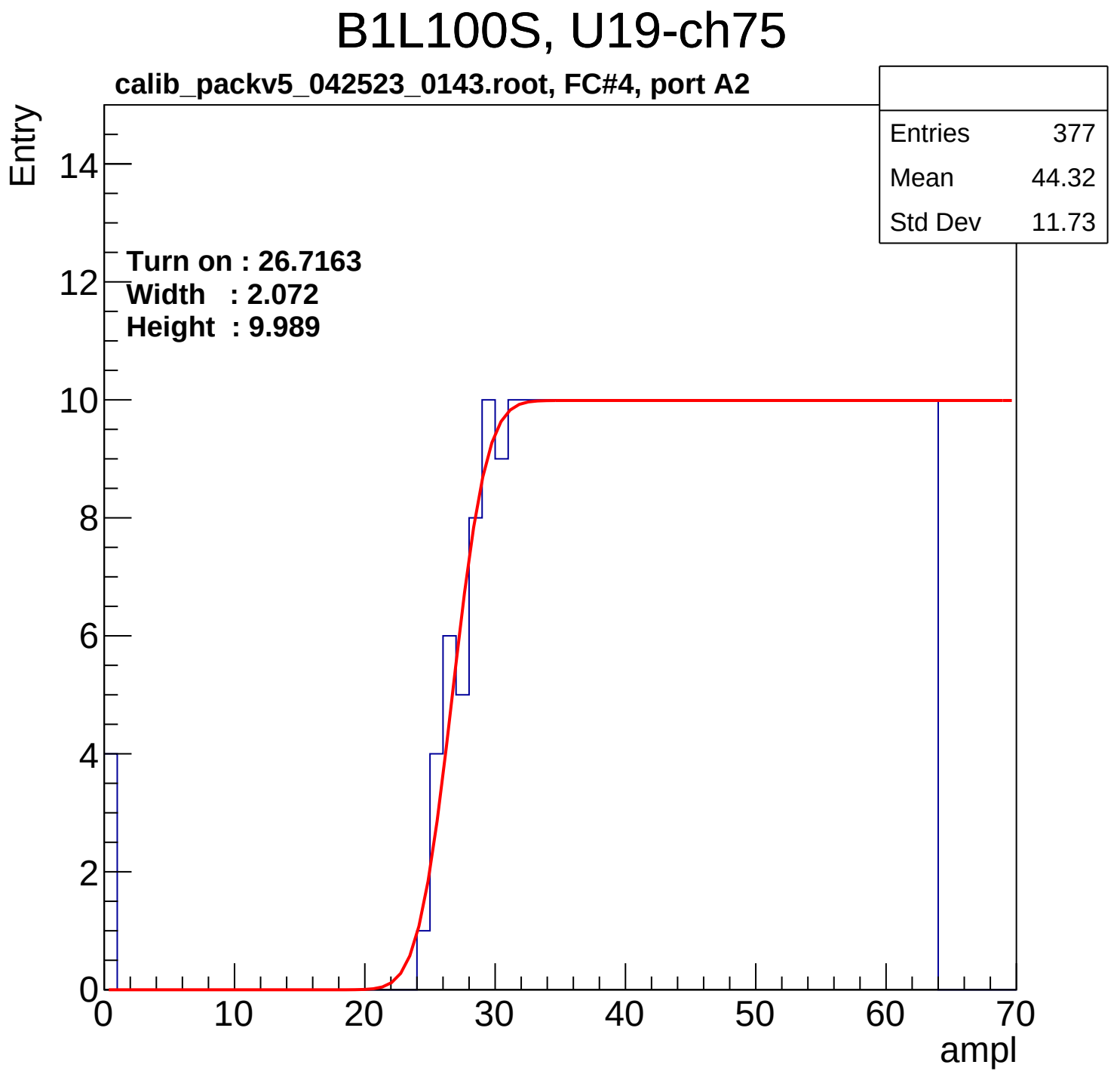
B1L100S, U19-ch75
calib_packv5_042523_0143.root, FC#4, port A2
Entries 377
Mean 44.32
Std Dev 11.73
Turn on : 26.7163
Width : 2.072
Height : 9.989
Entry
ampl
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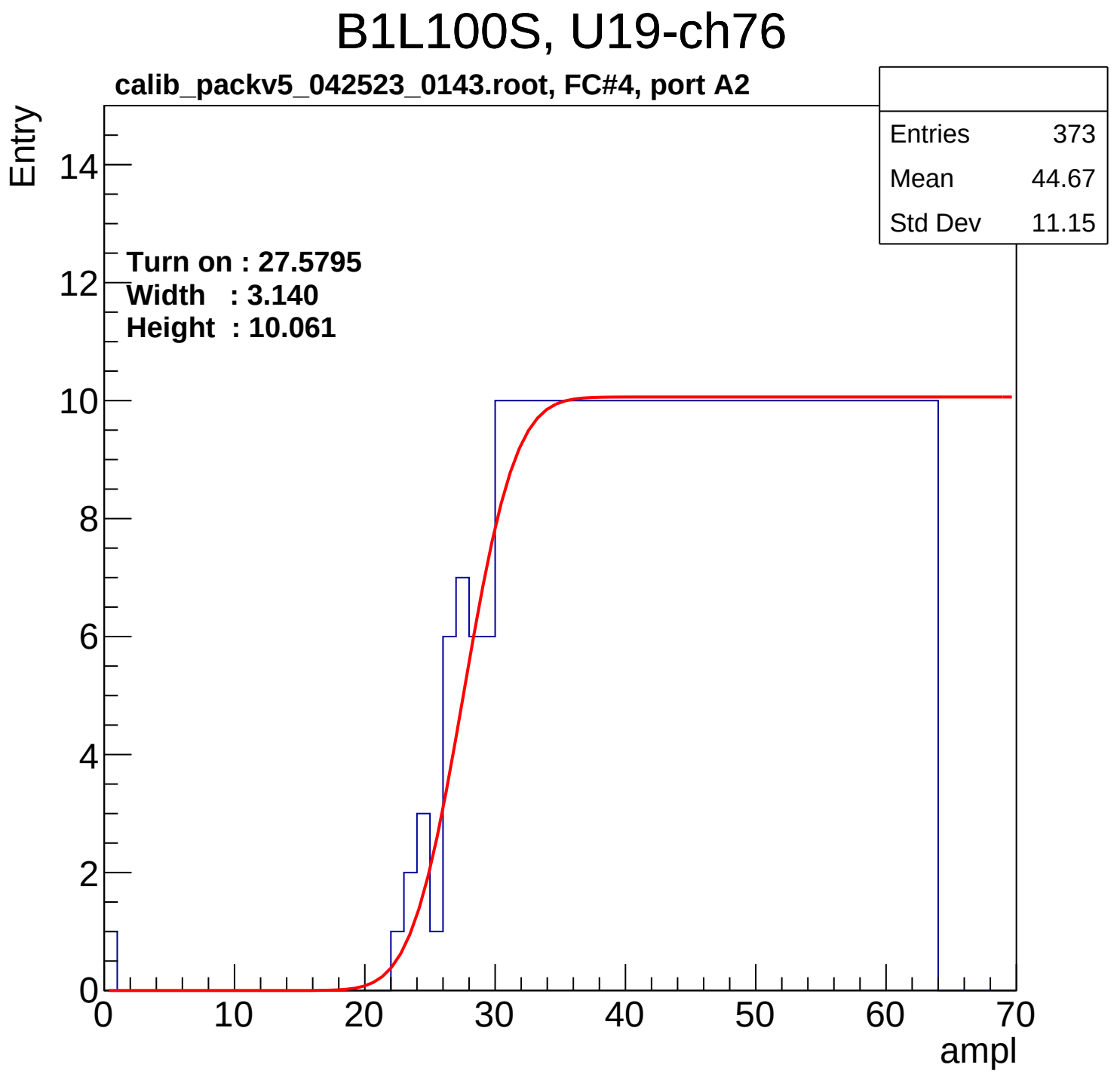
B1L100S, U19-ch76
calib_packv5_042523_0143.root, FC#4, port A2
Entries 373
Mean 44.67
Std Dev 11.15
Turn on : 27.5795
Width : 3.140
Height : 10.061
Entry
ampl
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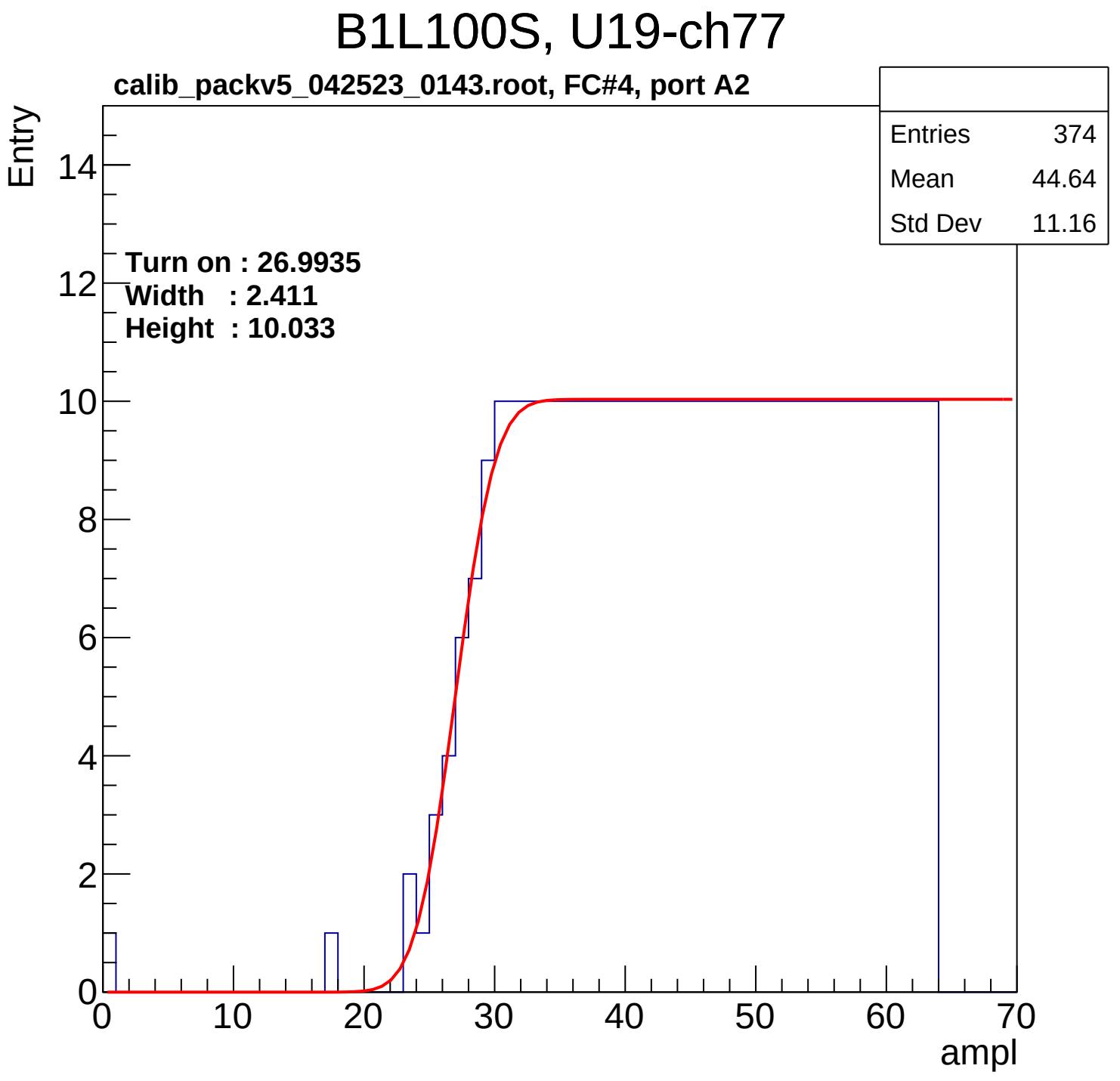
B1L100S, U19-ch77
calib_packv5_042523_0143.root, FC#4, port A2
Entries 374
Mean 44.64
Std Dev 11.16
Turn on : 26.9935
Width : 2.411
Height : 10.033
Entry
ampl
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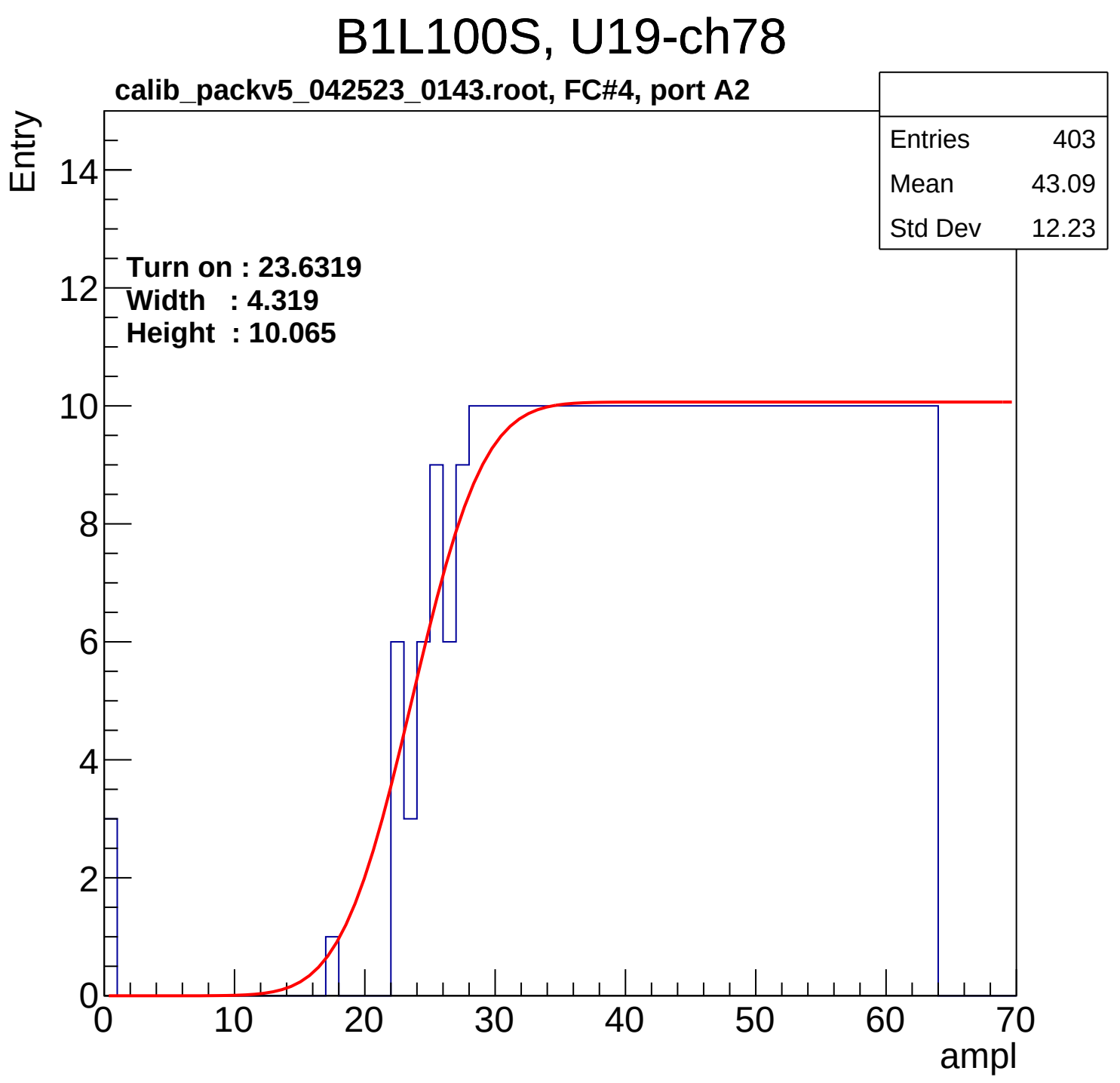
B1L100S, U19-ch78
calib_packv5_042523_0143.root, FC#4, port A2
Entries 403
Mean 43.09
Std Dev 12.23
Turn on : 23.6319
Width : 4.319
Height : 10.065
Entry
ampl
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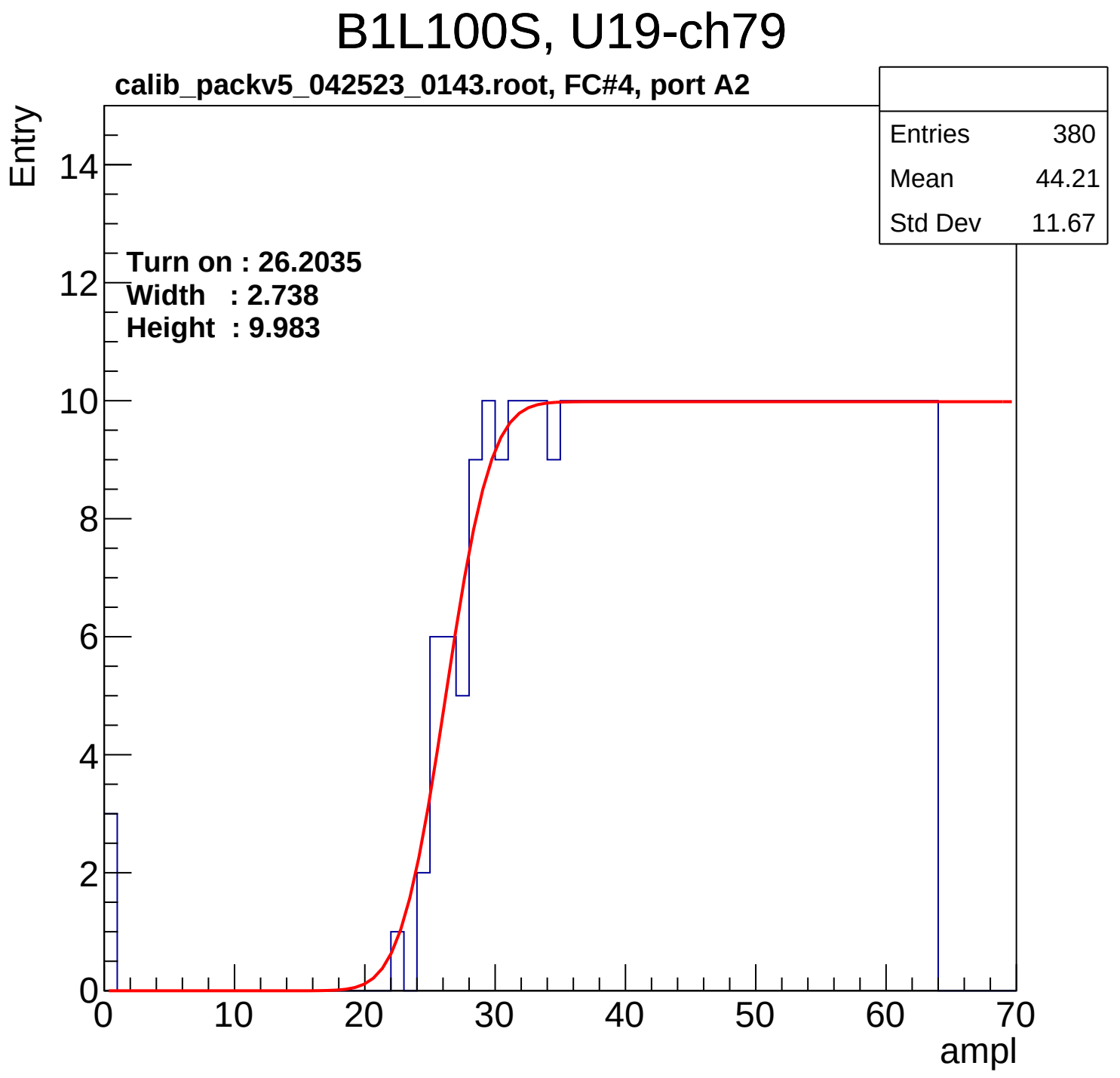
B1L100S, U19-ch79
calib_packv5_042523_0143.root, FC#4, port A2
Entries 380
Mean 44.21
Std Dev 11.67
Turn on : 26.2035
Width : 2.738
Height : 9.983
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ampl
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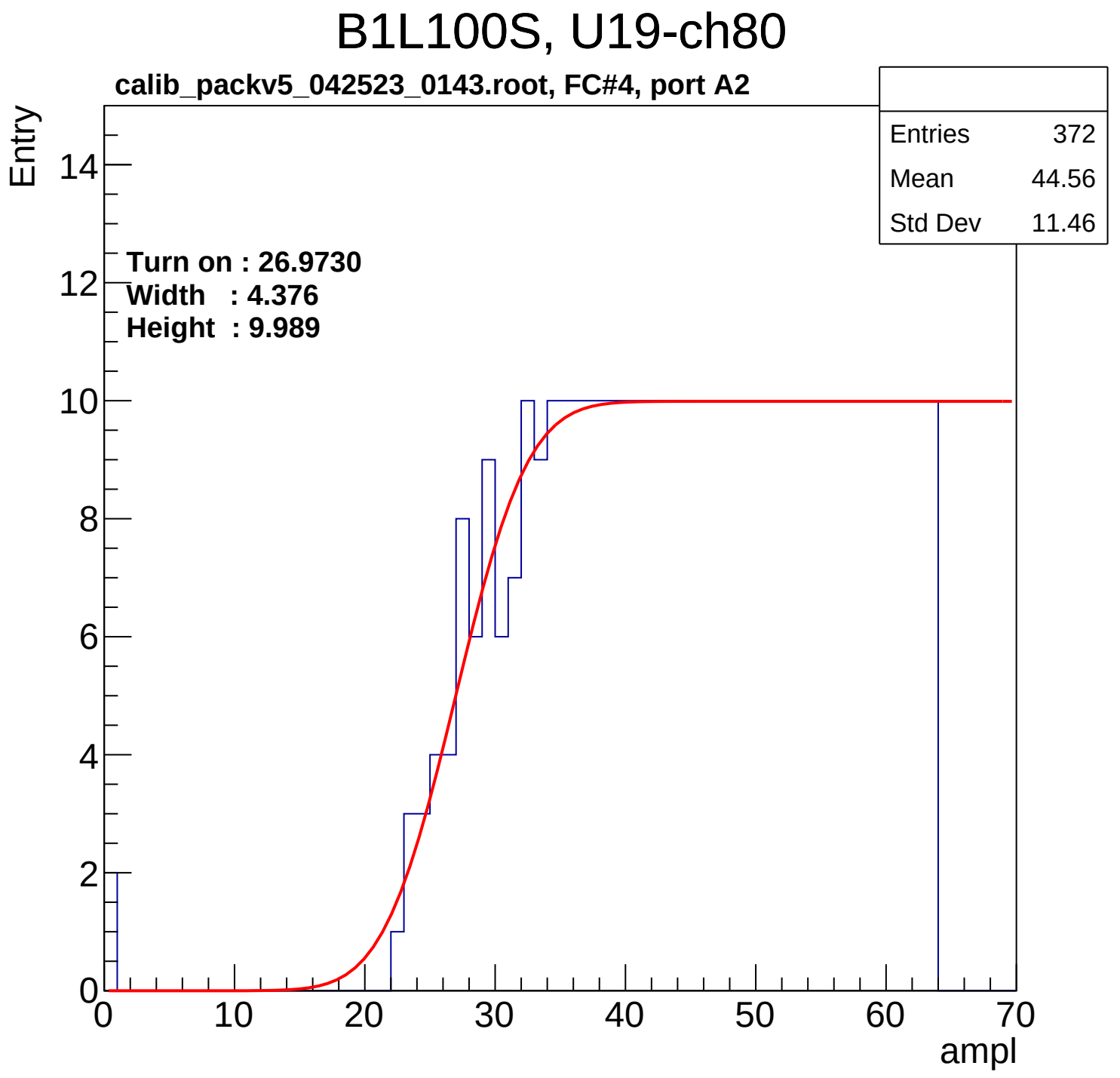
B1L100S, U19-ch80
calib_packv5_042523_0143.root, FC#4, port A2
Entries 372
Mean 44.56
Std Dev 11.46
Turn on : 26.9730
Width : 4.376
Height : 9.989
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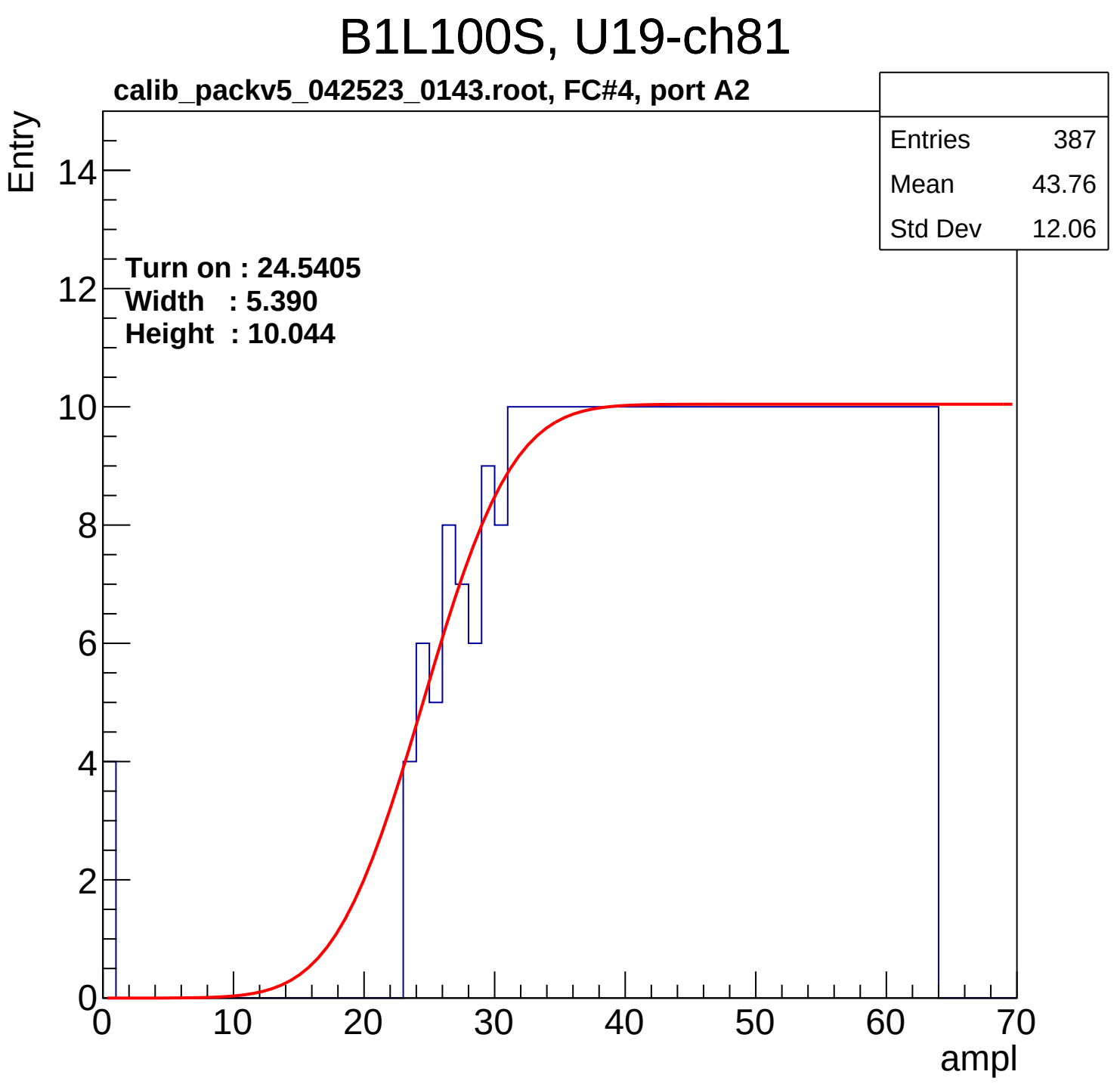
B1L100S, U19-ch81
calib_packv5_042523_0143.root, FC#4, port A2
Entries 387
Mean 43.76
Std Dev 12.06
Turn on : 24.5405
Width : 5.390
Height : 10.044
Entry
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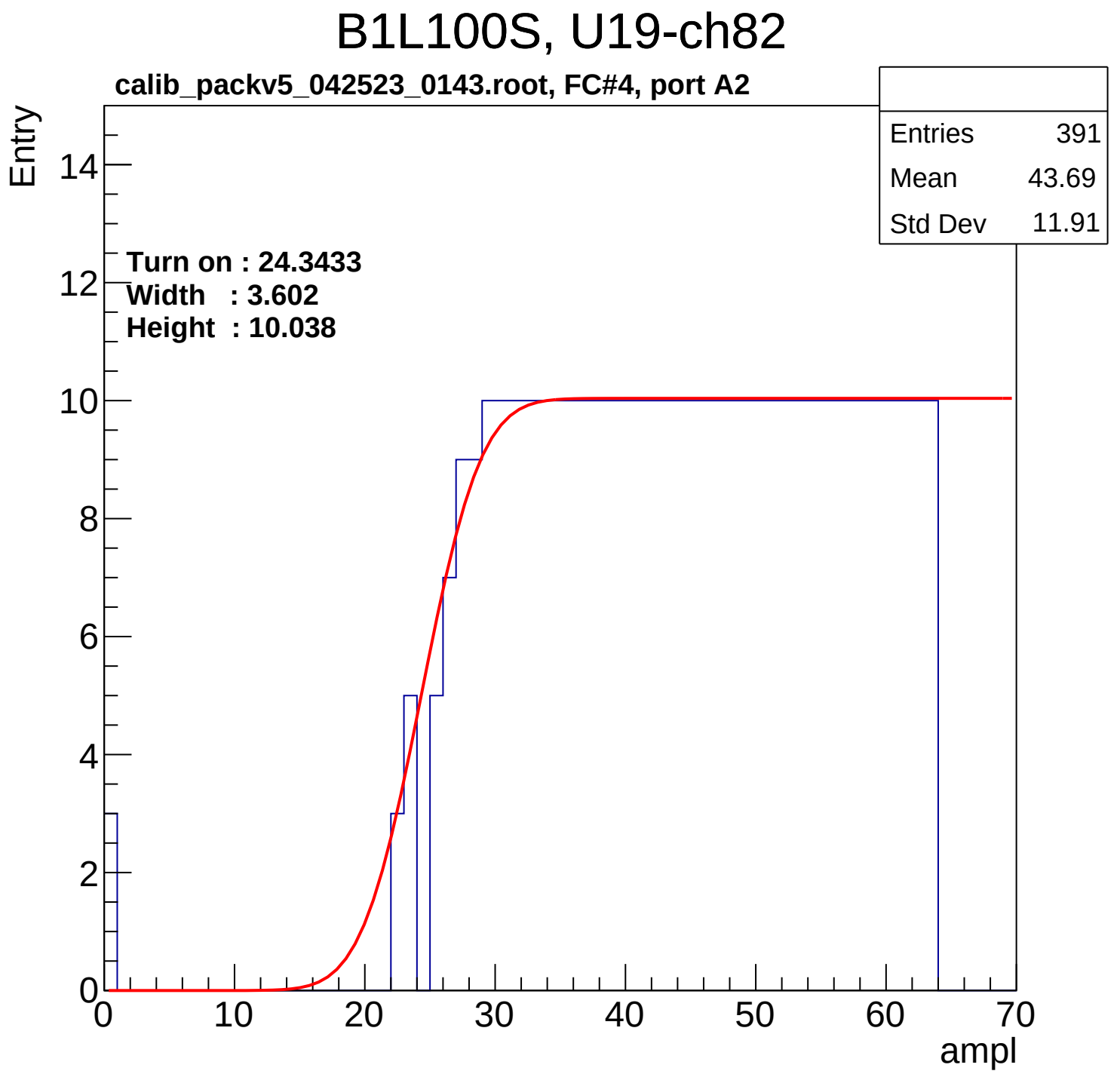
B1L100S, U19-ch82
calib_packv5_042523_0143.root, FC#4, port A2
Entries 391
Mean 43.69
Std Dev 11.91
Turn on : 24.3433
Width : 3.602
Height : 10.038
Entry
ampl
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6
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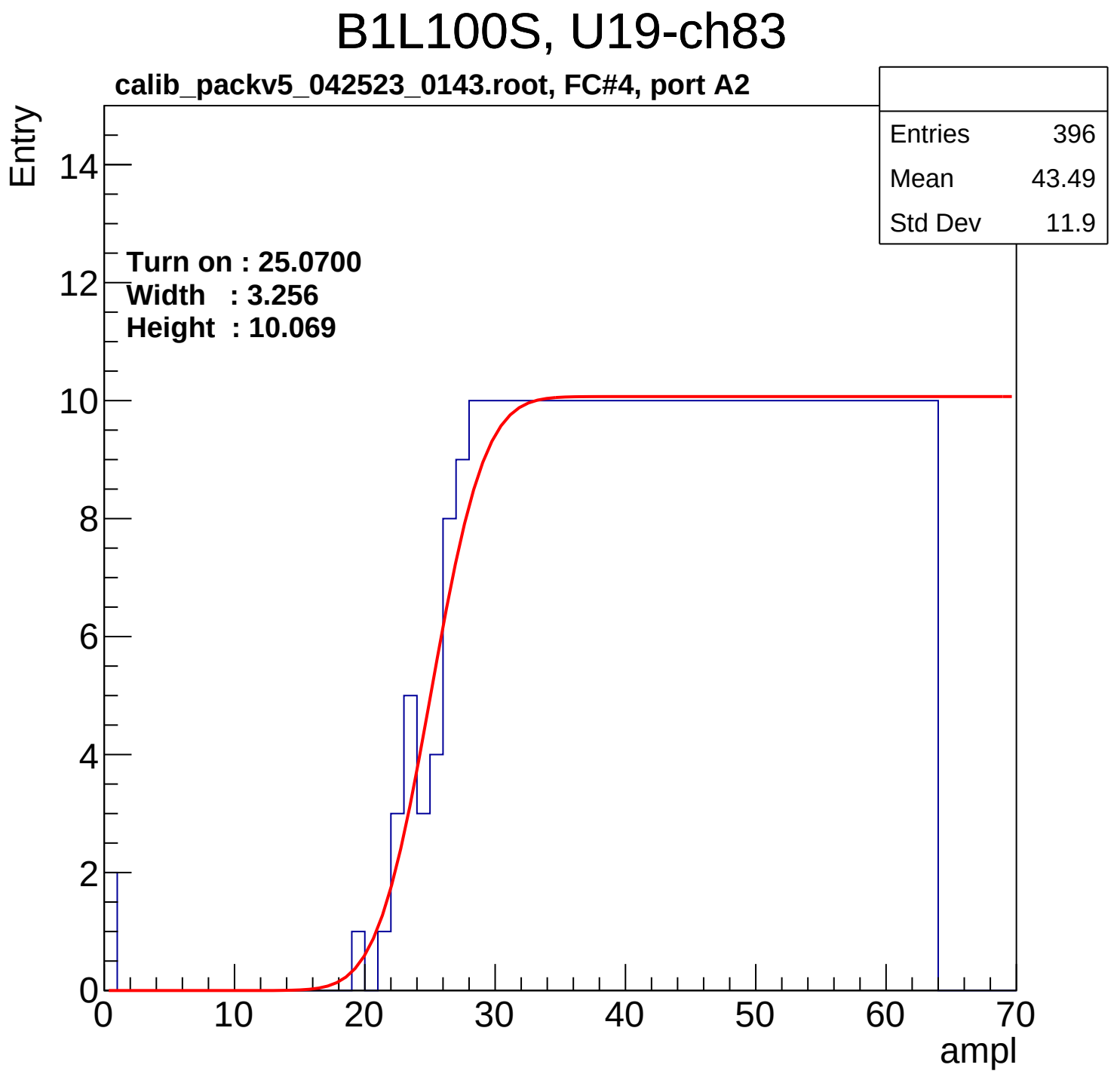
B1L100S, U19-ch83
calib_packv5_042523_0143.root, FC#4, port A2
Entries 396
Mean 43.49
Std Dev 11.9
Turn on : 25.0700
Width : 3.256
Height : 10.069
Entry
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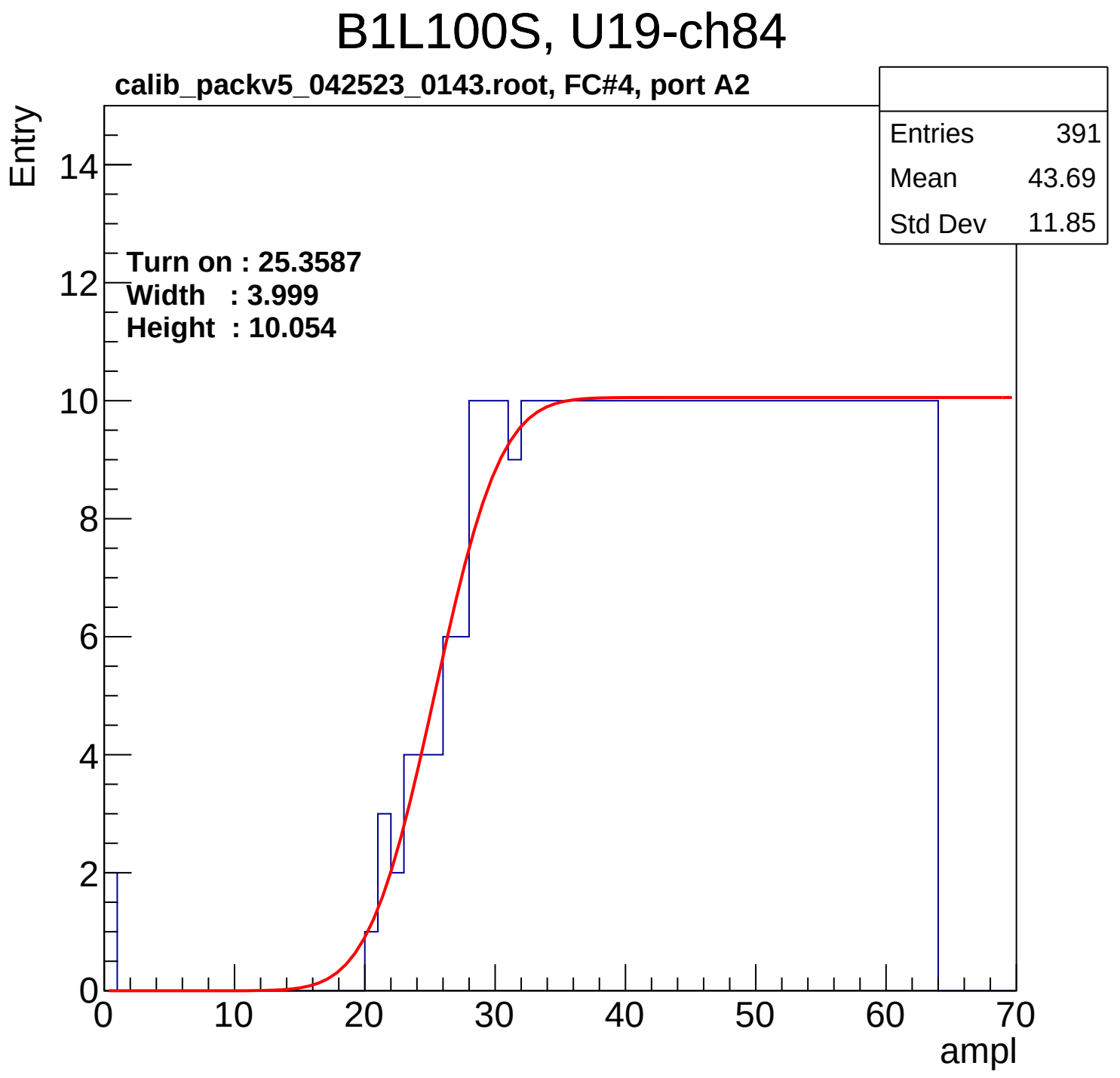
B1L100S, U19-ch84
calib_packv5_042523_0143.root, FC#4, port A2
Entries 391
Mean 43.69
Std Dev 11.85
Turn on : 25.3587
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Height : 10.054
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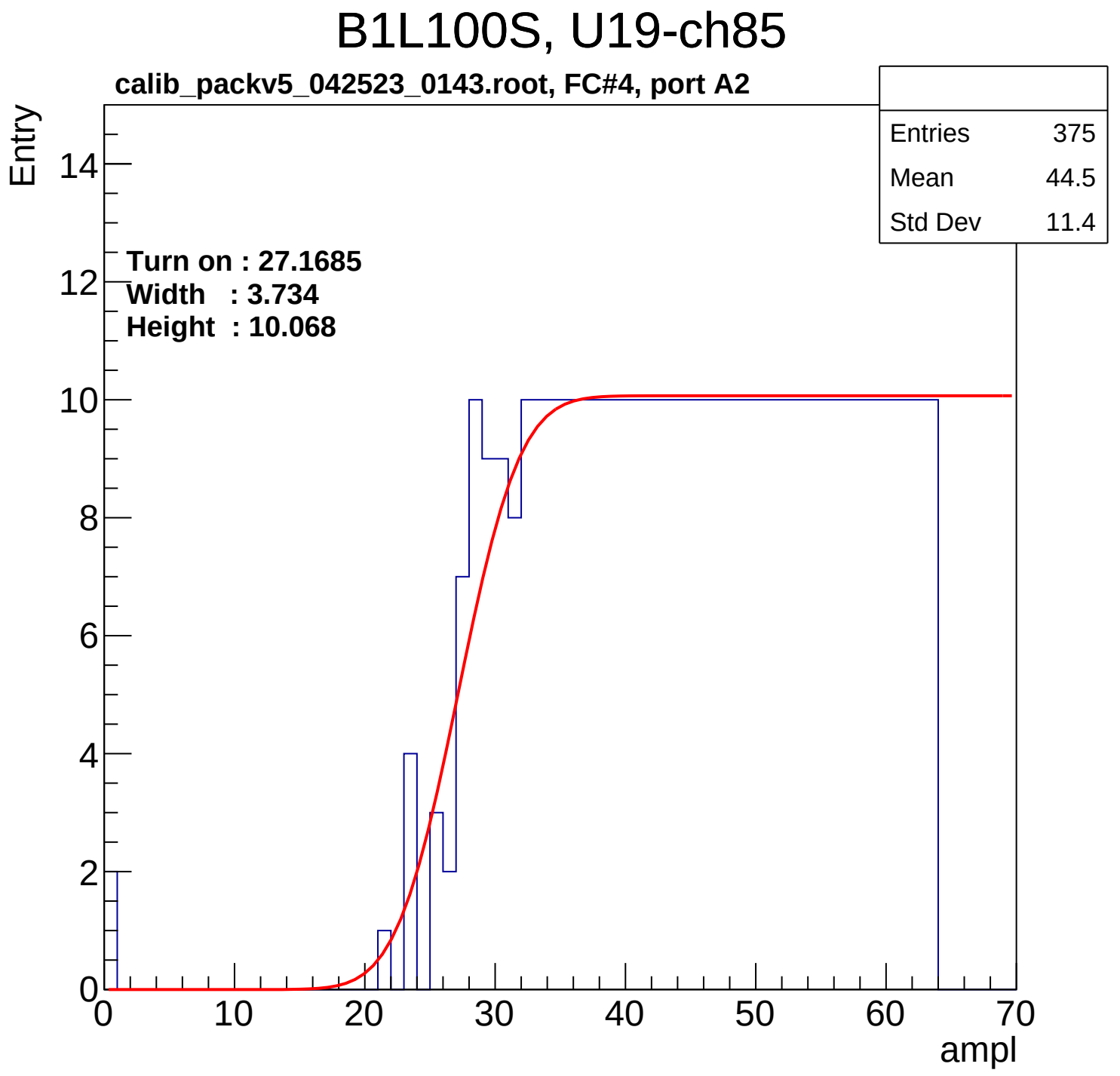
B1L100S, U19-ch85
calib_packv5_042523_0143.root, FC#4, port A2
Entries 375
Mean 44.5
Std Dev 11.4
Turn on : 27.1685
Width : 3.734
Height : 10.068
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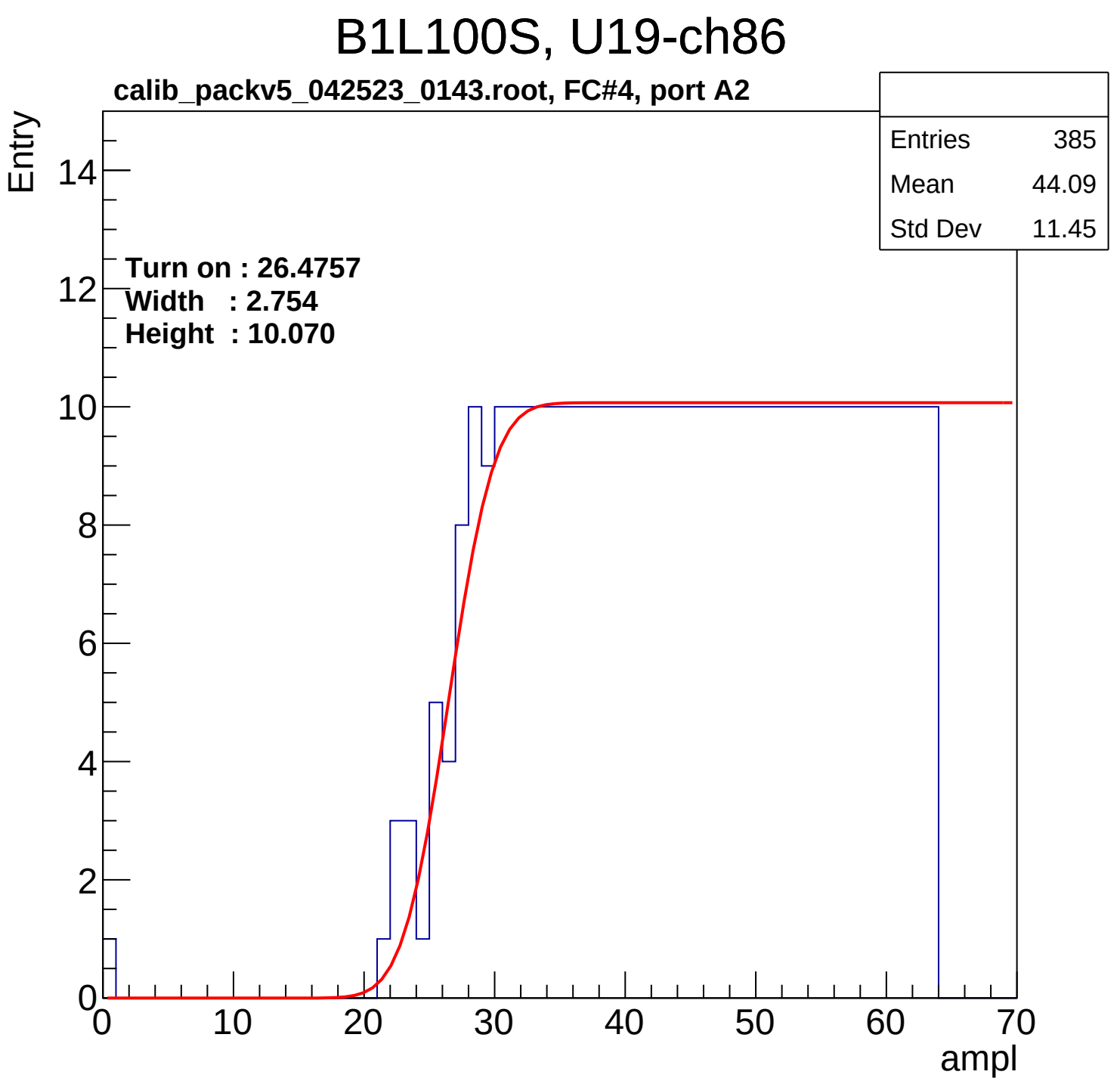
B1L100S, U19-ch86
calib_packv5_042523_0143.root, FC#4, port A2
Entries 385
Mean 44.09
Std Dev 11.45
Turn on : 26.4757
Width : 2.754
Height : 10.070
Entry
ampl
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4
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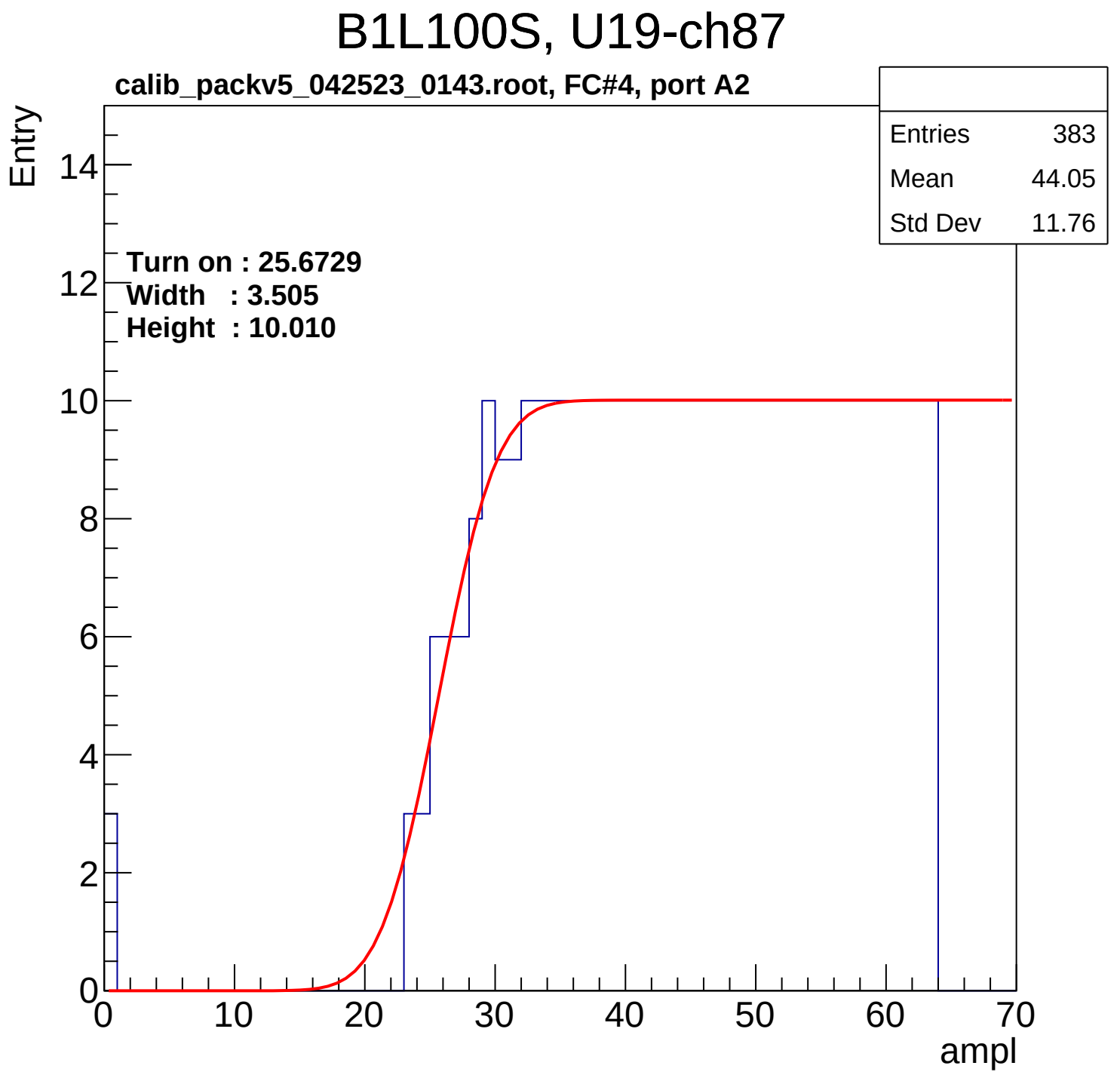
B1L100S, U19-ch87
calib_packv5_042523_0143.root, FC#4, port A2
Entries 383
Mean 44.05
Std Dev 11.76
Turn on : 25.6729
Width : 3.505
Height : 10.010
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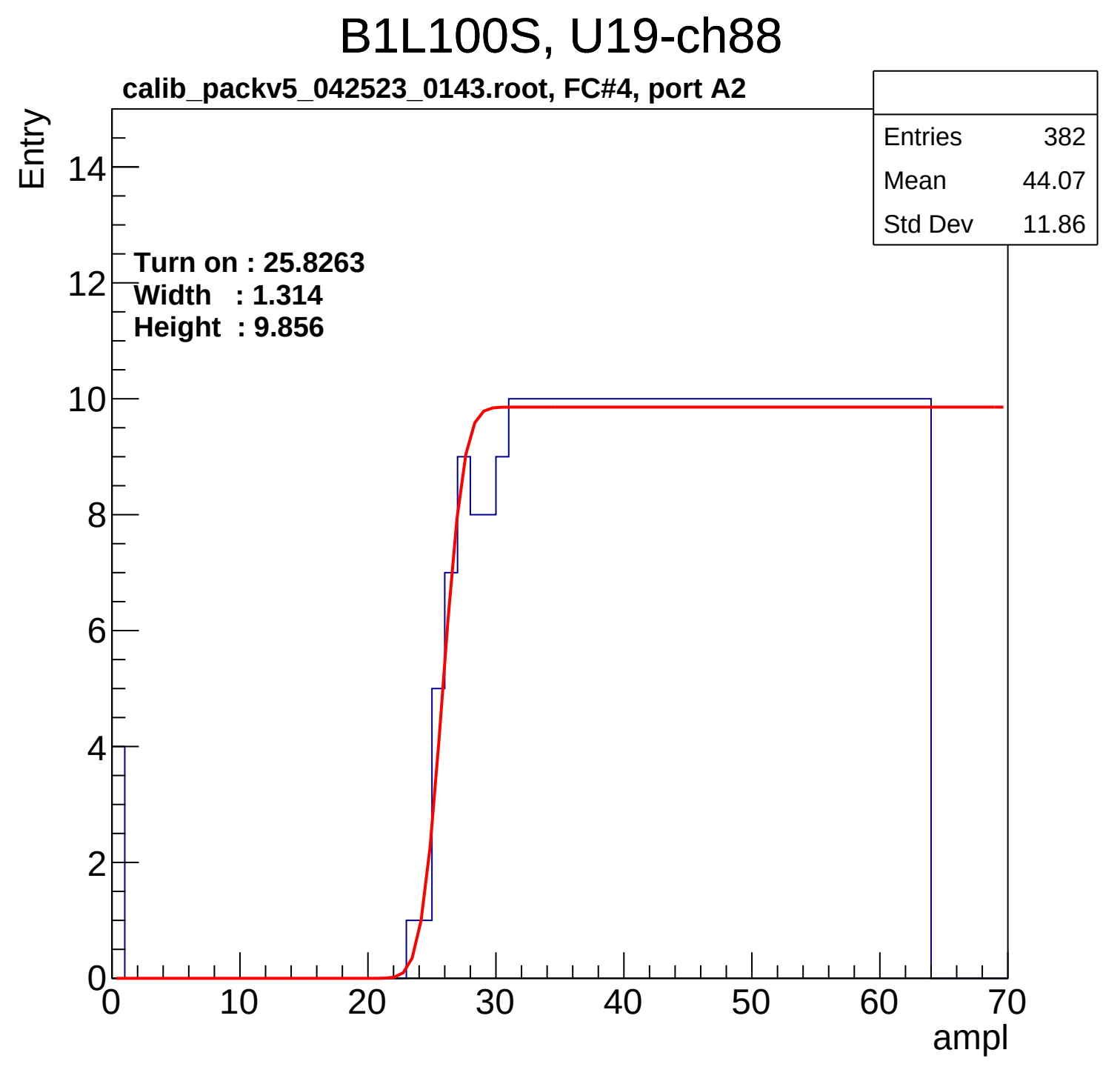
B1L100S, U19-ch88
calib_packv5_042523_0143.root, FC#4, port A2
Entries 382
Mean 44.07
Std Dev 11.86
Turn on : 25.8263
Width : 1.314
Height : 9.856
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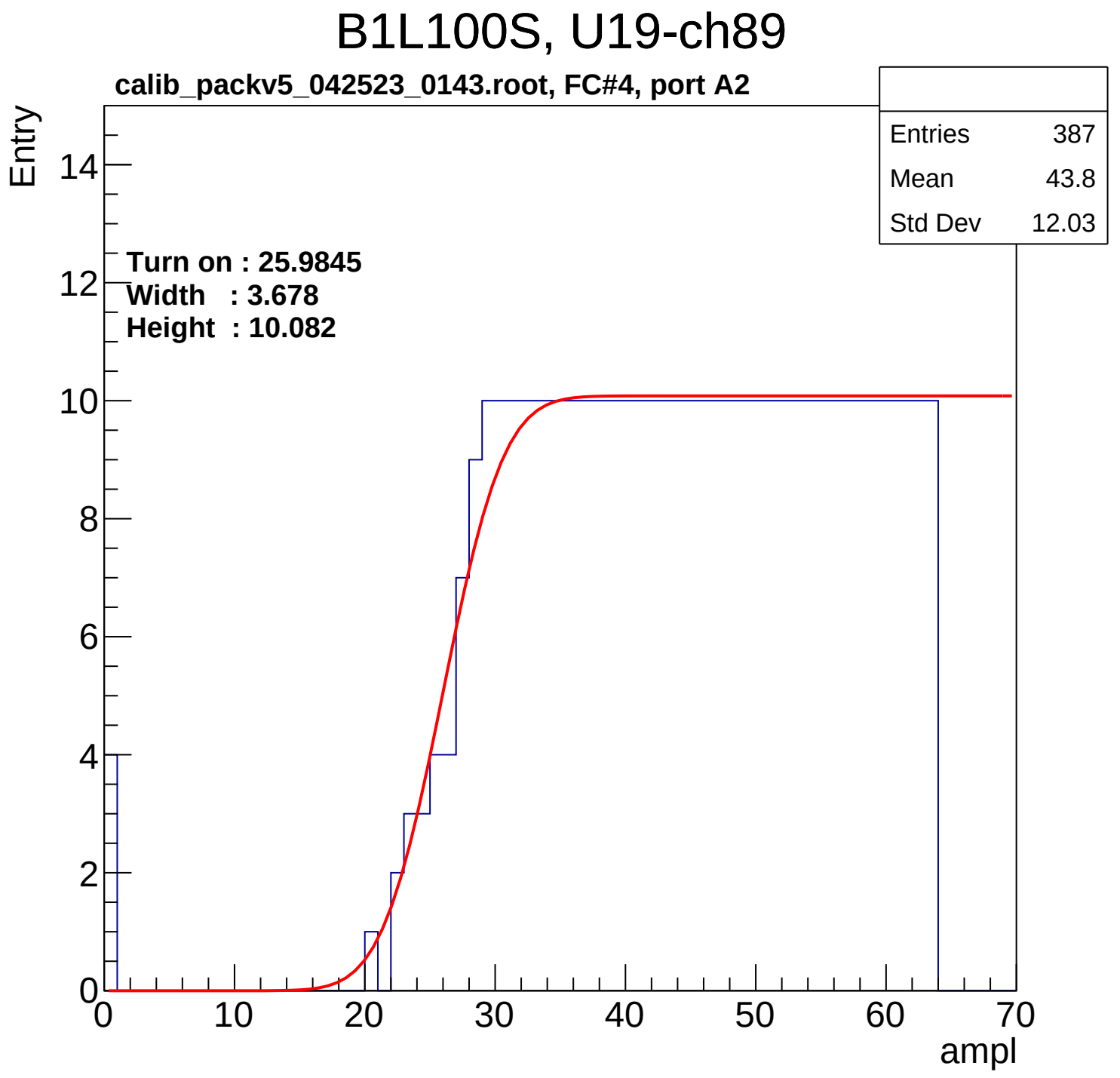
B1L100S, U19-ch89
calib_packv5_042523_0143.root, FC#4, port A2
Entries 387
Mean 43.8
Std Dev 12.03
Turn on : 25.9845
Width : 3.678
Height : 10.082
Entry
ampl
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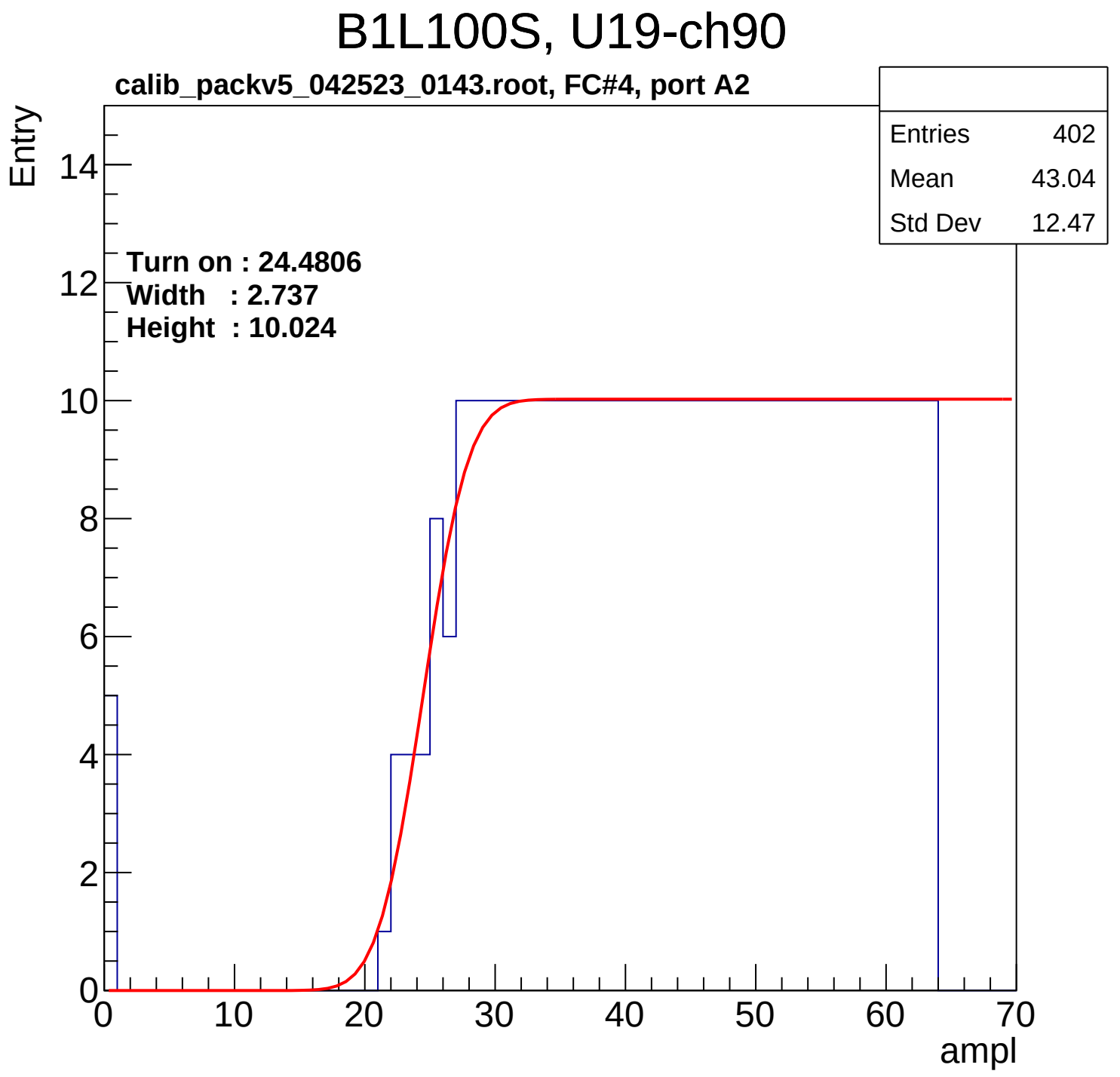
B1L100S, U19-ch90
calib_packv5_042523_0143.root, FC#4, port A2
Entries 402
Mean 43.04
Std Dev 12.47
Turn on : 24.4806
Width : 2.737
Height : 10.024
Entry
ampl
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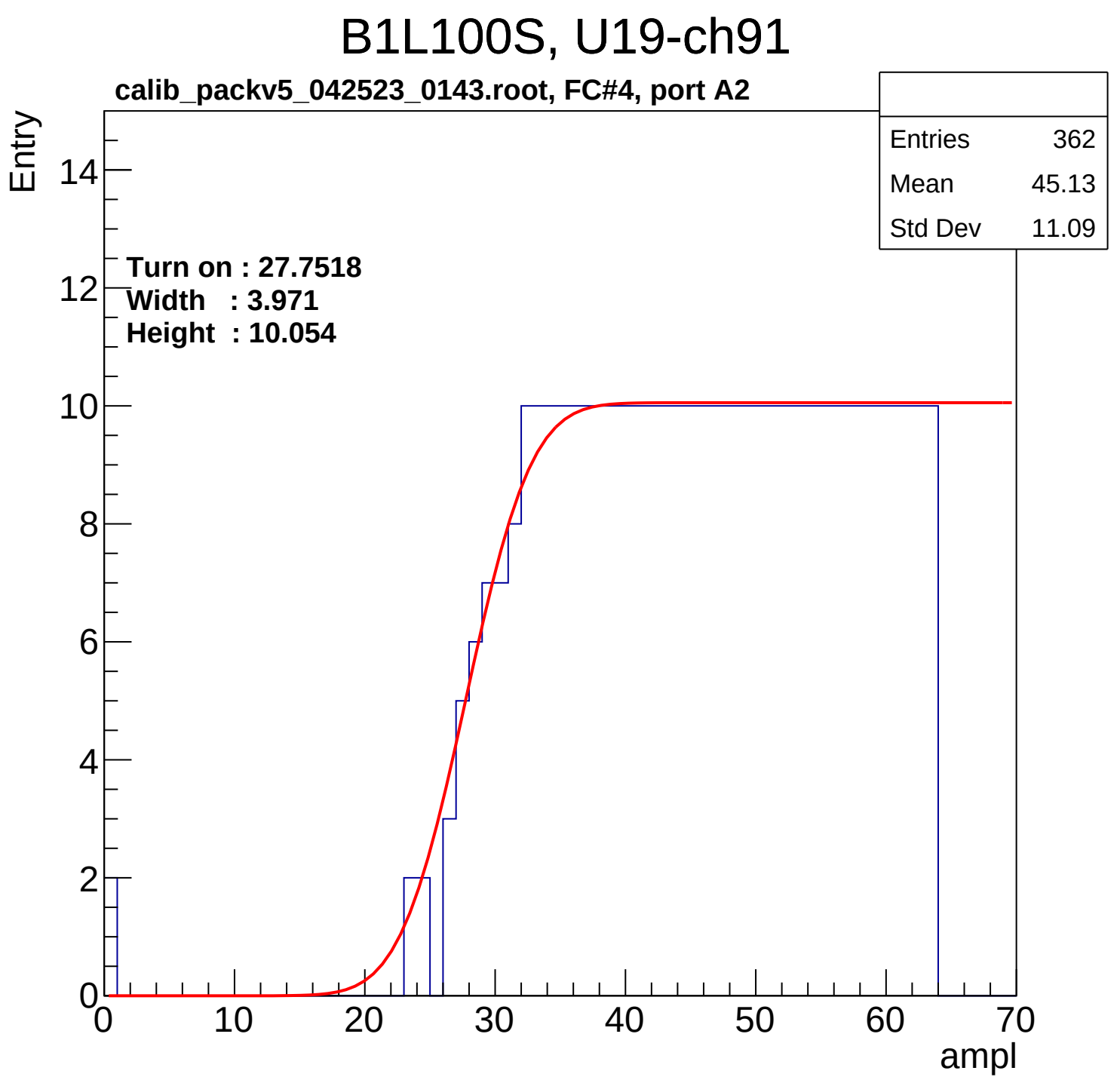
B1L100S, U19-ch91
calib_packv5_042523_0143.root, FC#4, port A2
Entries 362
Mean 45.13
Std Dev 11.09
Turn on : 27.7518
Width : 3.971
Height : 10.054
Entry
ampl
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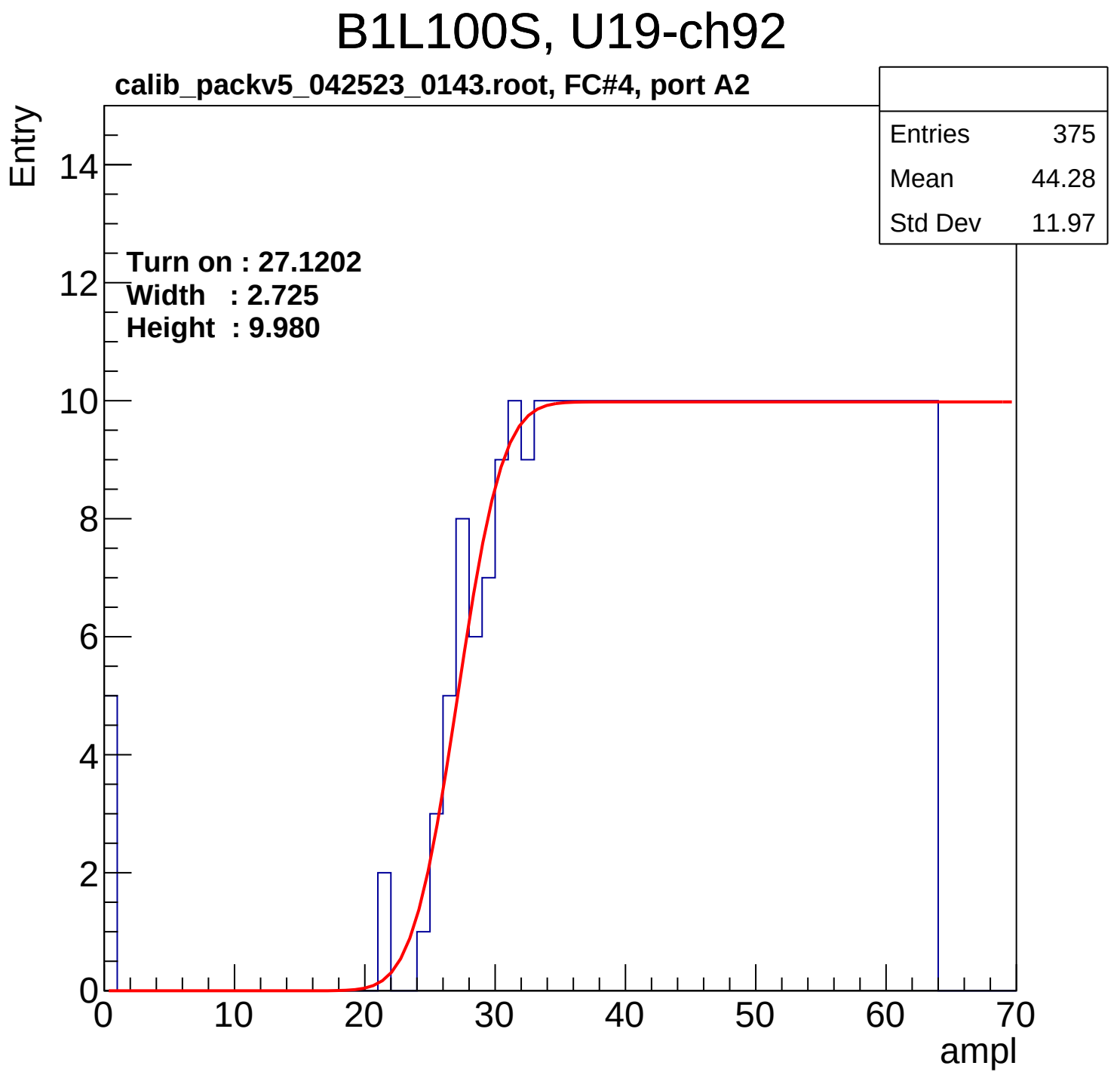
B1L100S, U19-ch92
calib_packv5_042523_0143.root, FC#4, port A2
Entries 375
Mean 44.28
Std Dev 11.97
Turn on : 27.1202
Width : 2.725
Height : 9.980
Entry
ampl
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4
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8
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0
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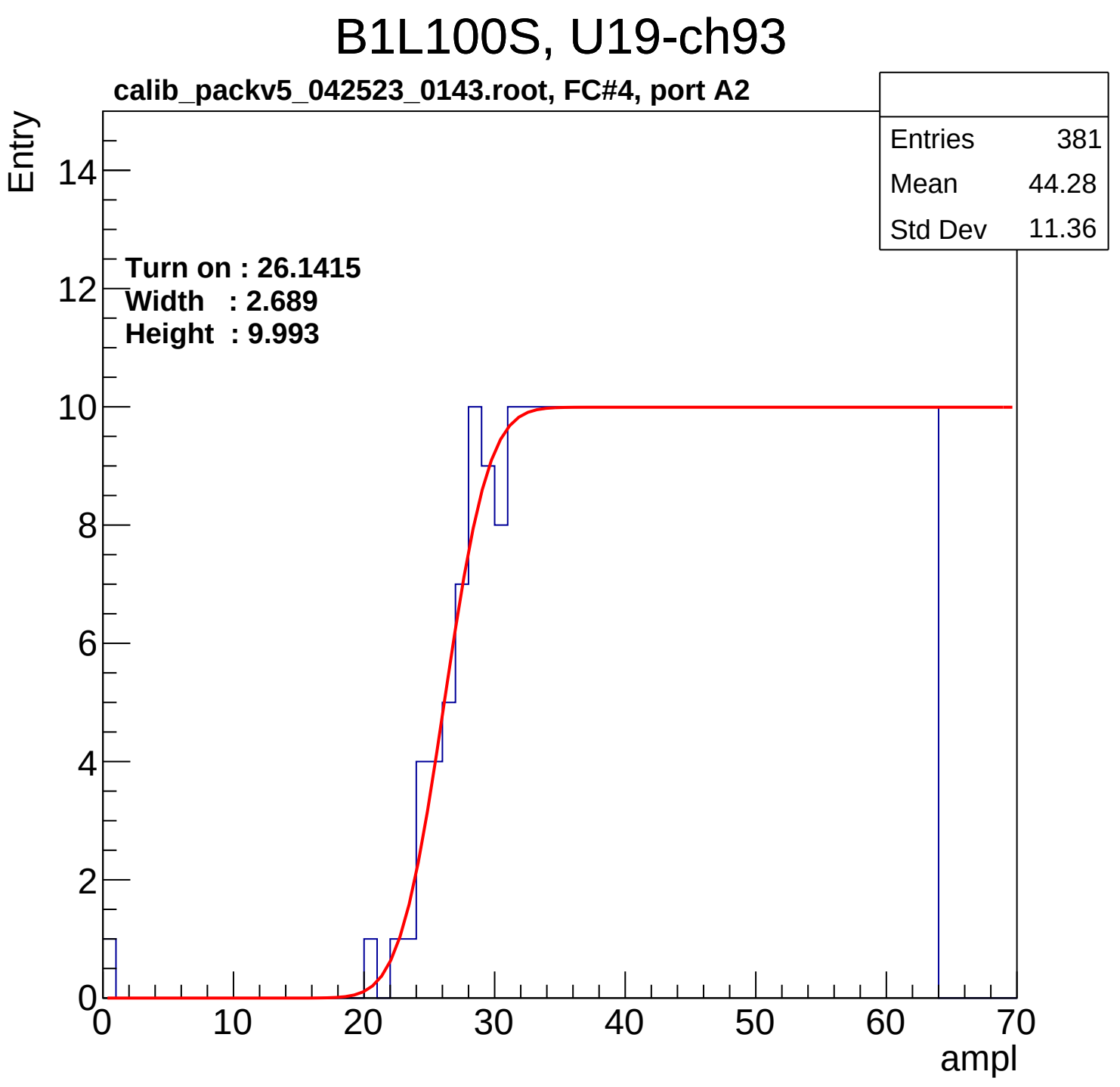
B1L100S, U19-ch93
calib_packv5_042523_0143.root, FC#4, port A2
Entries 381
Mean 44.28
Std Dev 11.36
Turn on : 26.1415
Width : 2.689
Height : 9.993
Entry
ampl
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2
4
6
8
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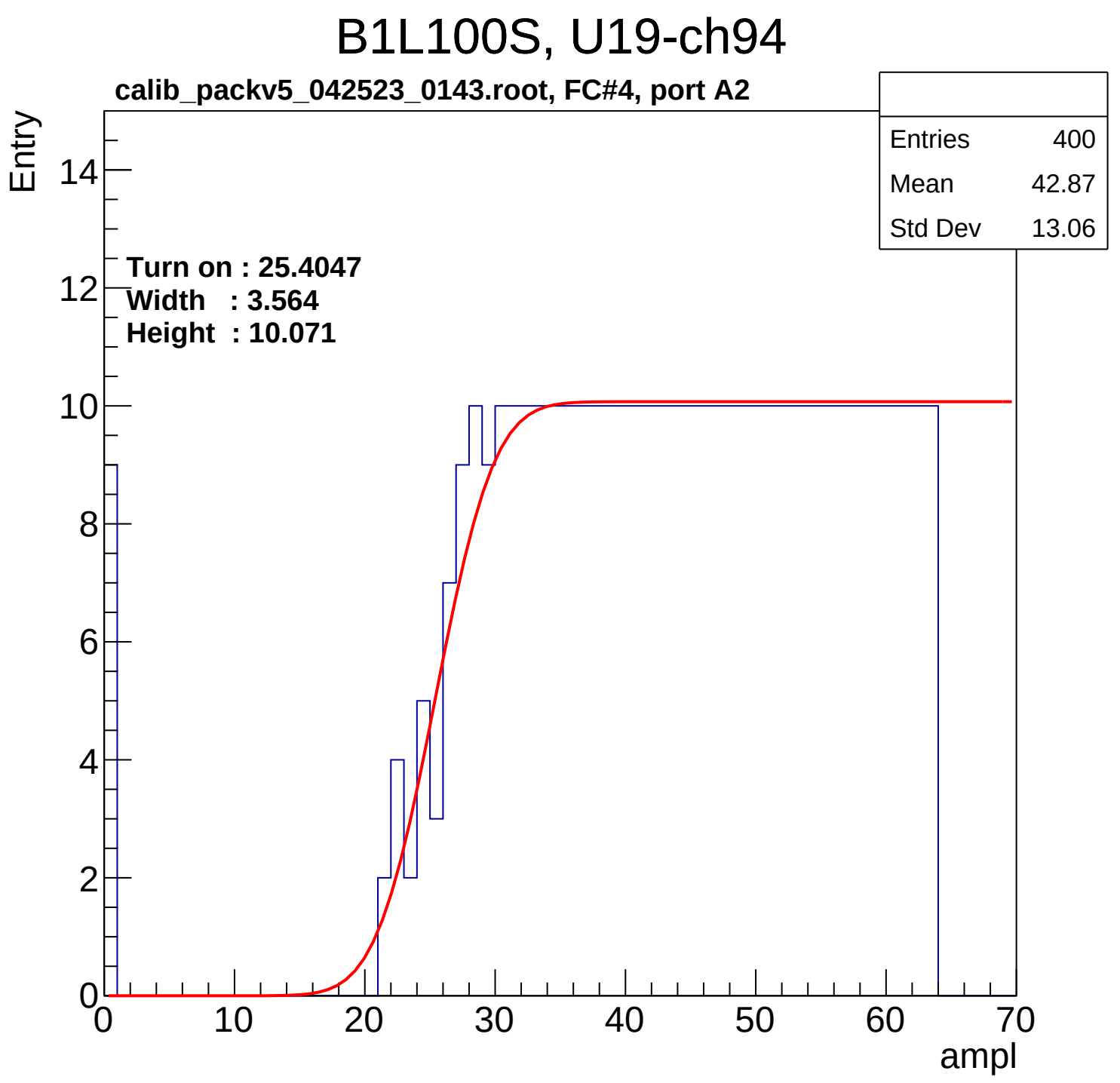
B1L100S, U19-ch94
calib_packv5_042523_0143.root, FC#4, port A2
Entries 400
Mean 42.87
Std Dev 13.06
Turn on : 25.4047
Width : 3.564
Height : 10.071
Entry
ampl
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6
8
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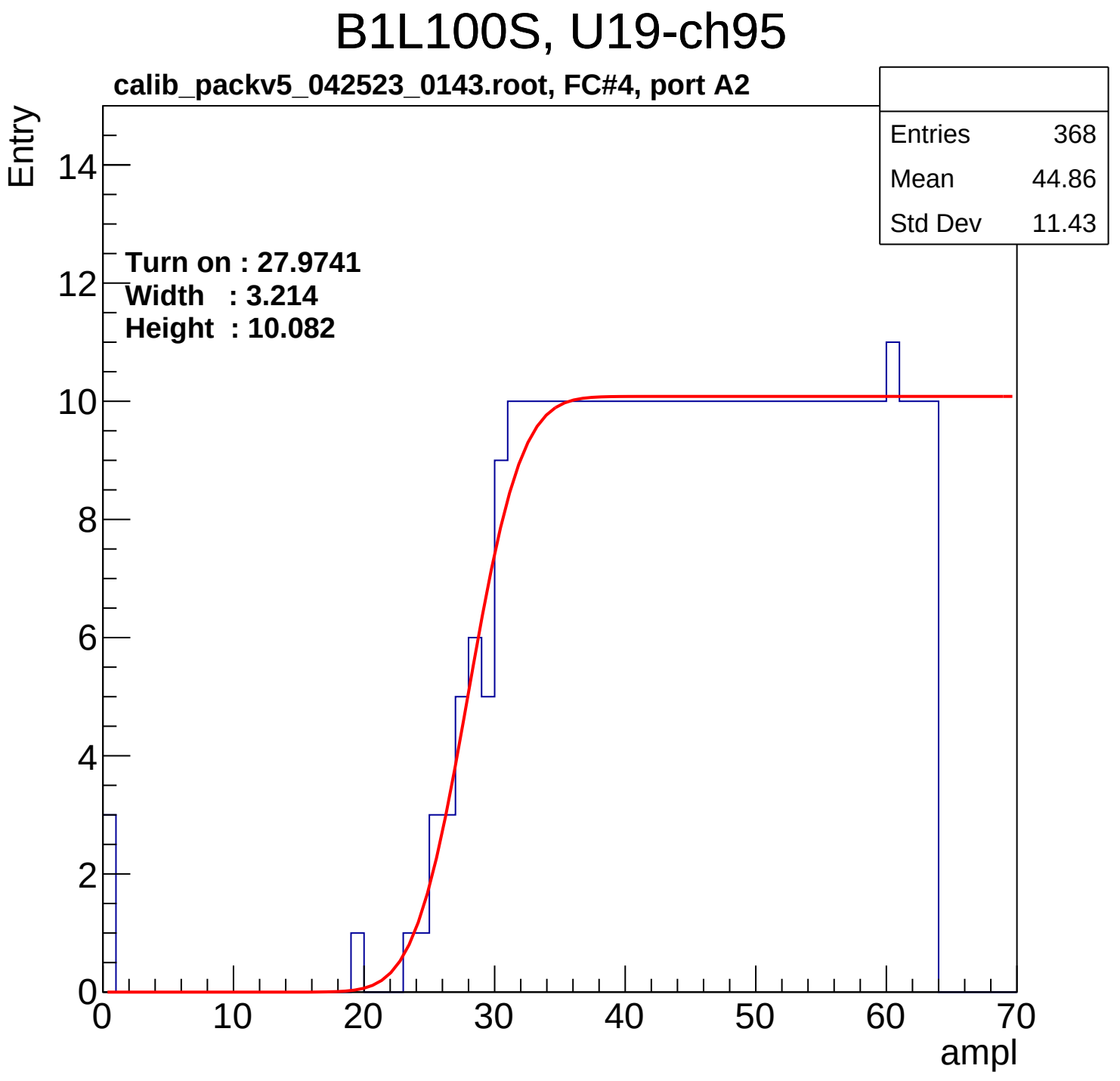
B1L100S, U19-ch95
calib_packv5_042523_0143.root, FC#4, port A2
Entries 368
Mean 44.86
Std Dev 11.43
Turn on : 27.9741
Width : 3.214
Height : 10.082
Entry
ampl
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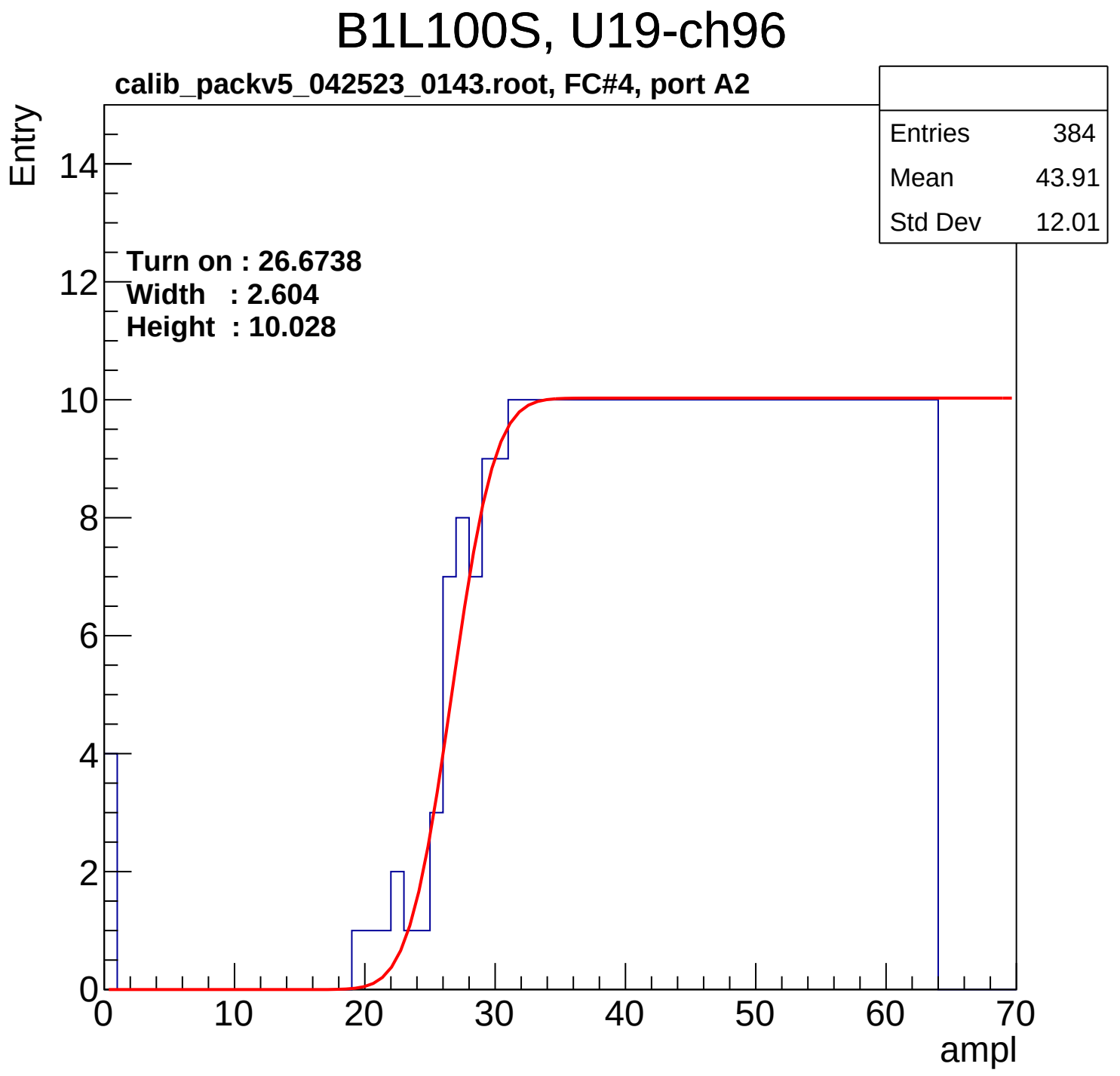
B1L100S, U19-ch96
calib_packv5_042523_0143.root, FC#4, port A2
Entries 384
Mean 43.91
Std Dev 12.01
Turn on : 26.6738
Width : 2.604
Height : 10.028
Entry
ampl
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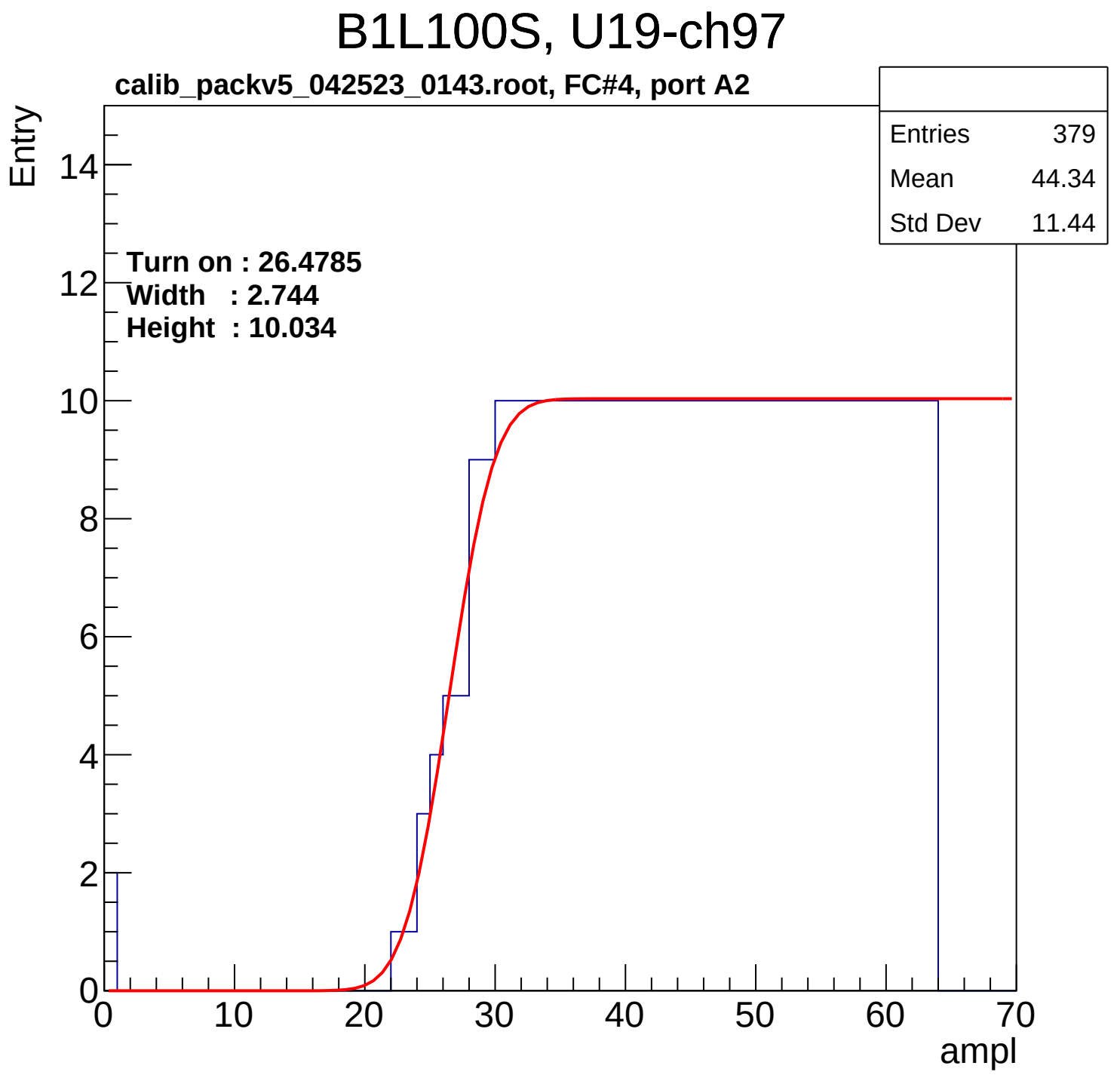
B1L100S, U19-ch97
calib_packv5_042523_0143.root, FC#4, port A2
Entries 379
Mean 44.34
Std Dev 11.44
Turn on : 26.4785
Width : 2.744
Height : 10.034
Entry
ampl
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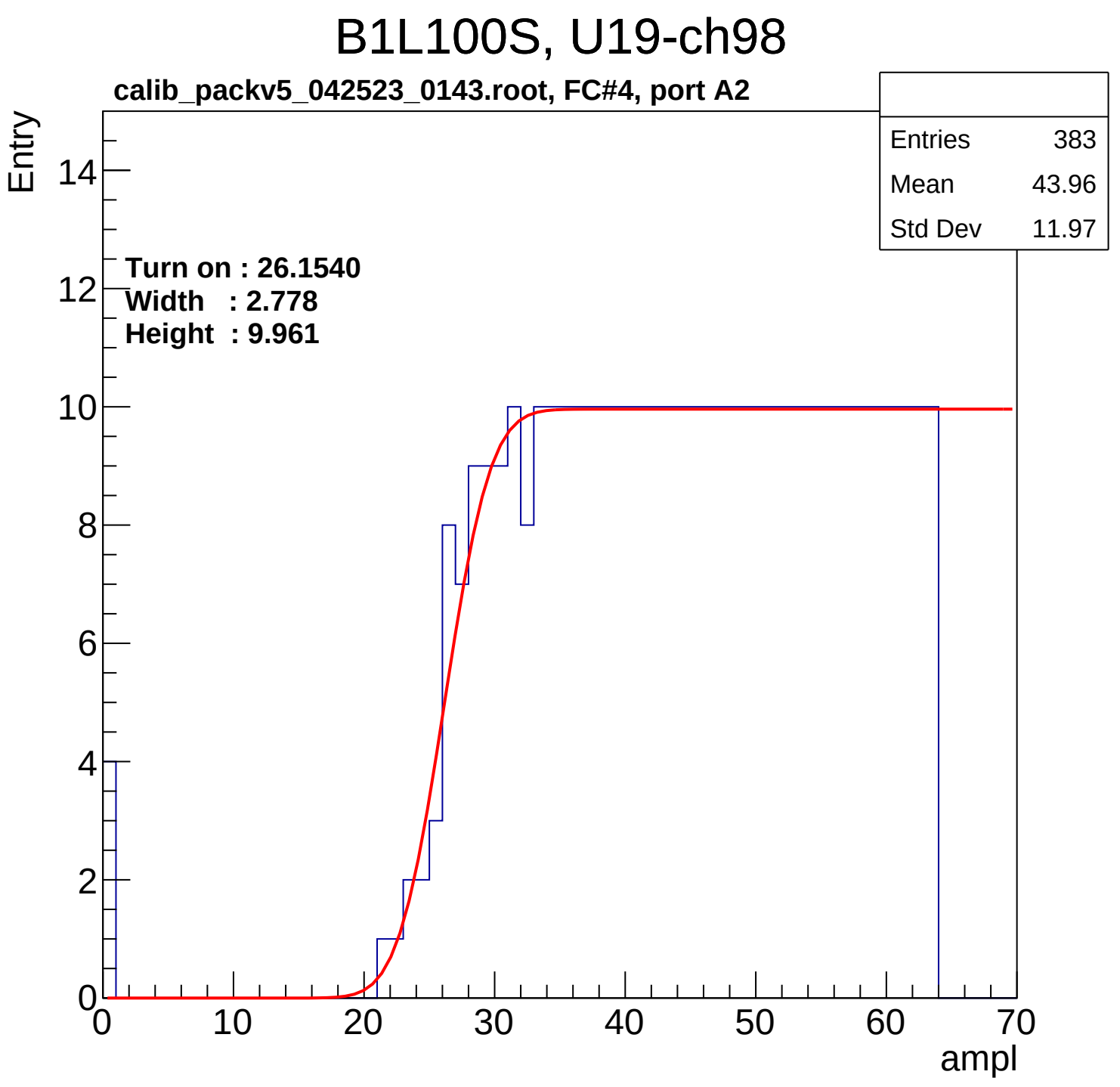
B1L100S, U19-ch98
calib_packv5_042523_0143.root, FC#4, port A2
Entries 383
Mean 43.96
Std Dev 11.97
Turn on : 26.1540
Width : 2.778
Height : 9.961
Entry
ampl
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8
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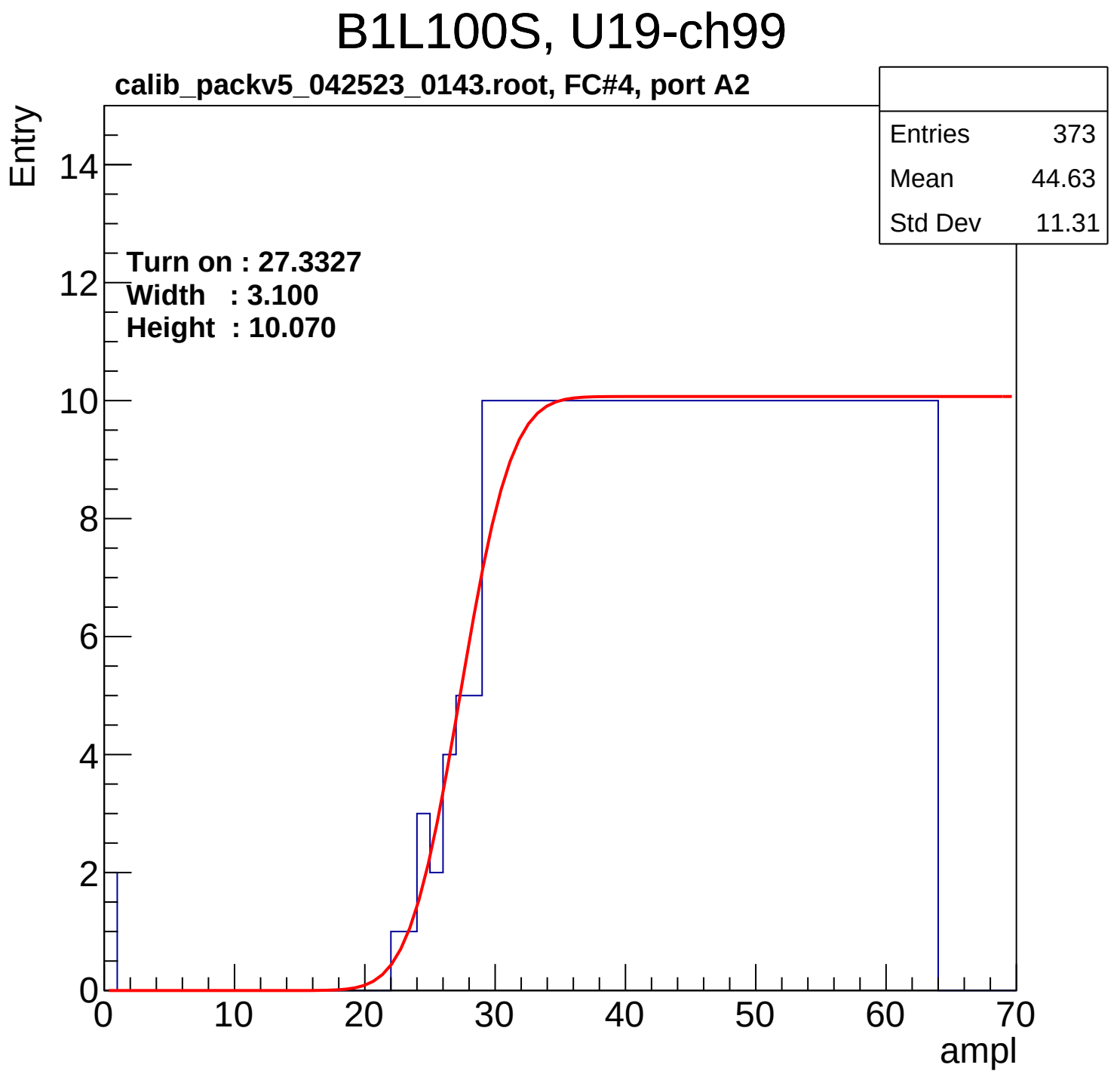
B1L100S, U19-ch99
calib_packv5_042523_0143.root, FC#4, port A2
Entries 373
Mean 44.63
Std Dev 11.31
Turn on : 27.3327
Width : 3.100
Height : 10.070
Entry
ampl
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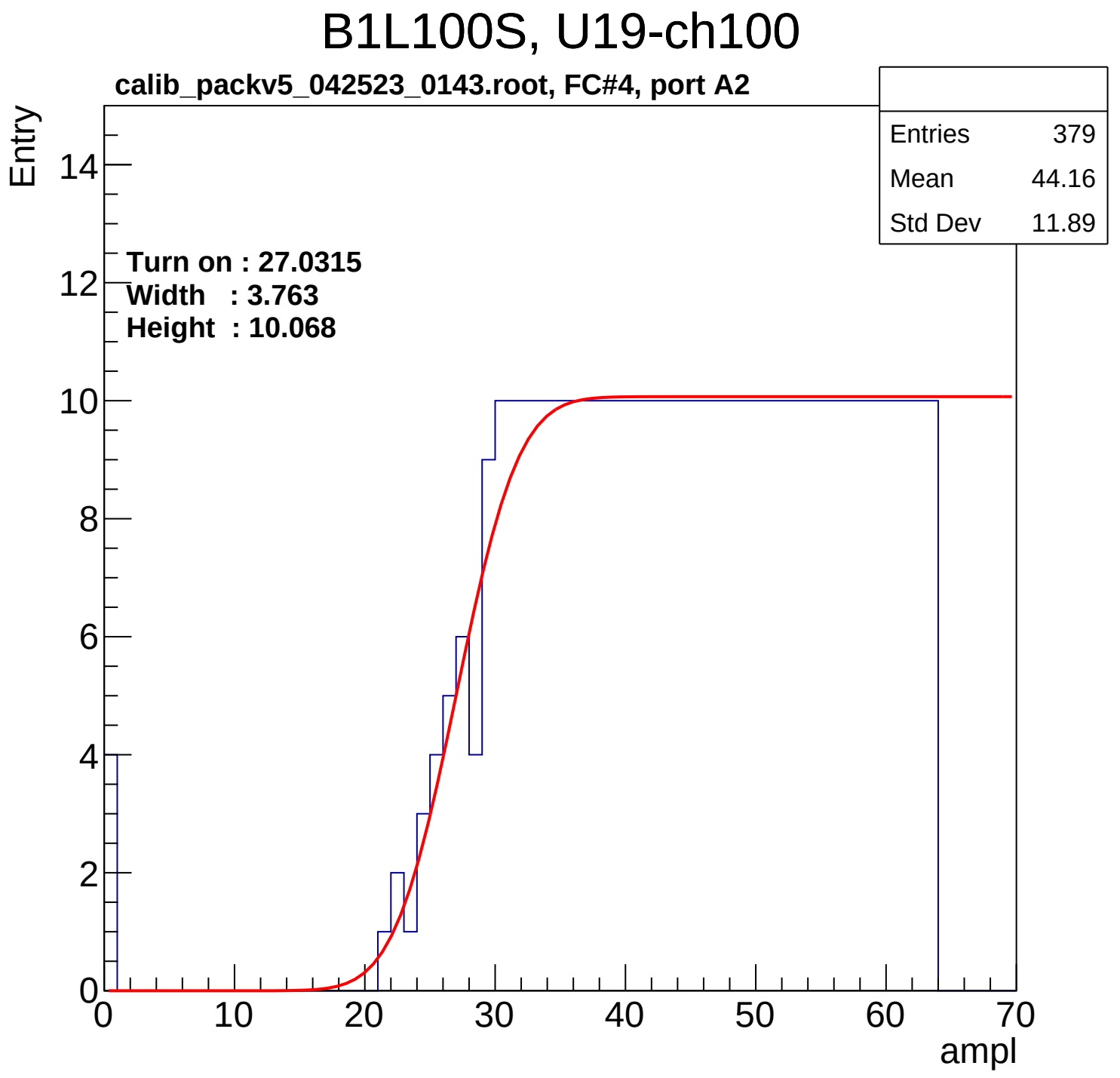
B1L100S, U19-ch100
calib_packv5_042523_0143.root, FC#4, port A2
Entries 379
Mean 44.16
Std Dev 11.89
Turn on : 27.0315
Width : 3.763
Height : 10.068
Entry
ampl
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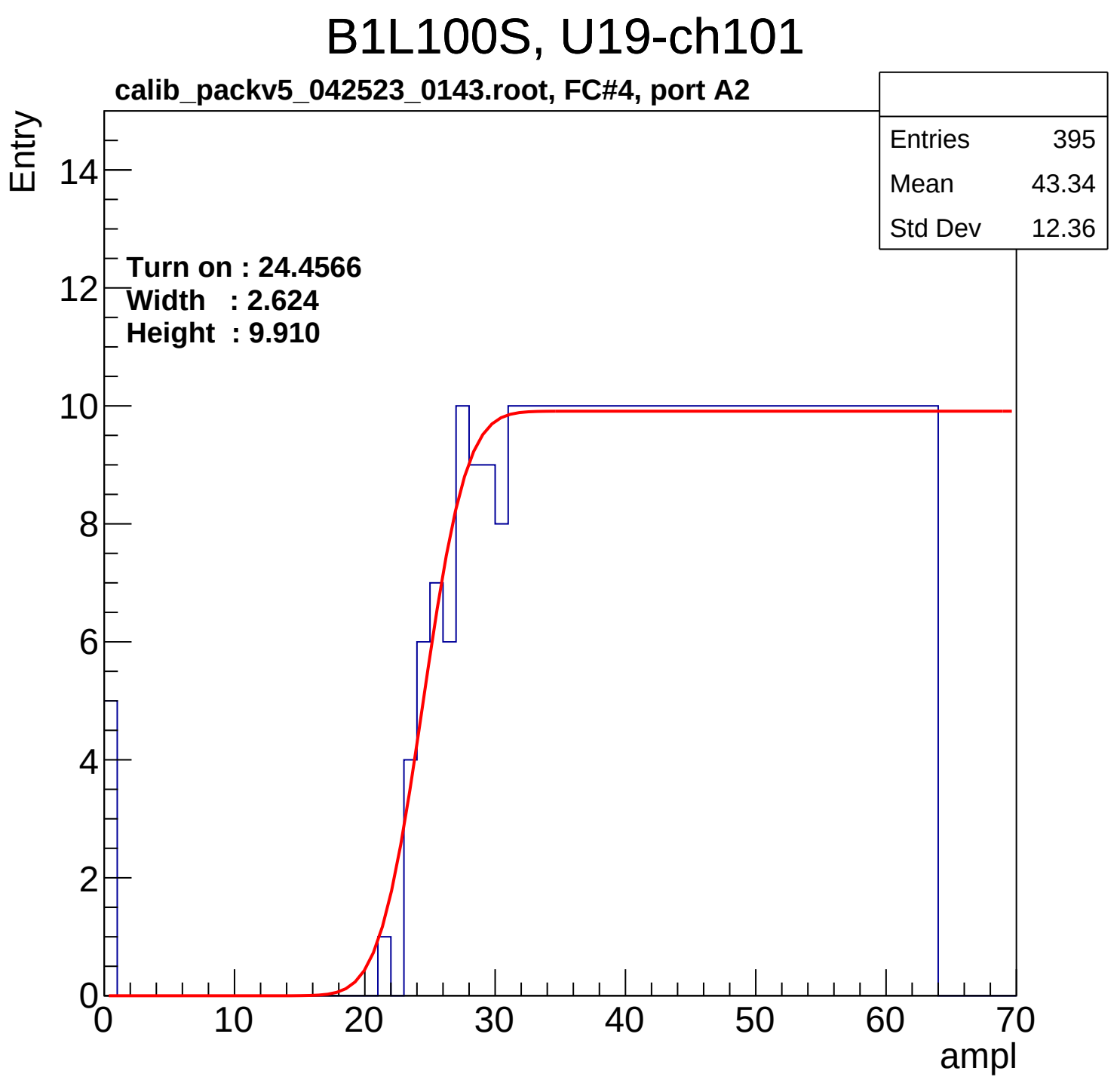
B1L100S, U19-ch101
calib_packv5_042523_0143.root, FC#4, port A2
Entries 395
Mean 43.34
Std Dev 12.36
Turn on : 24.4566
Width : 2.624
Height : 9.910
Entry
ampl
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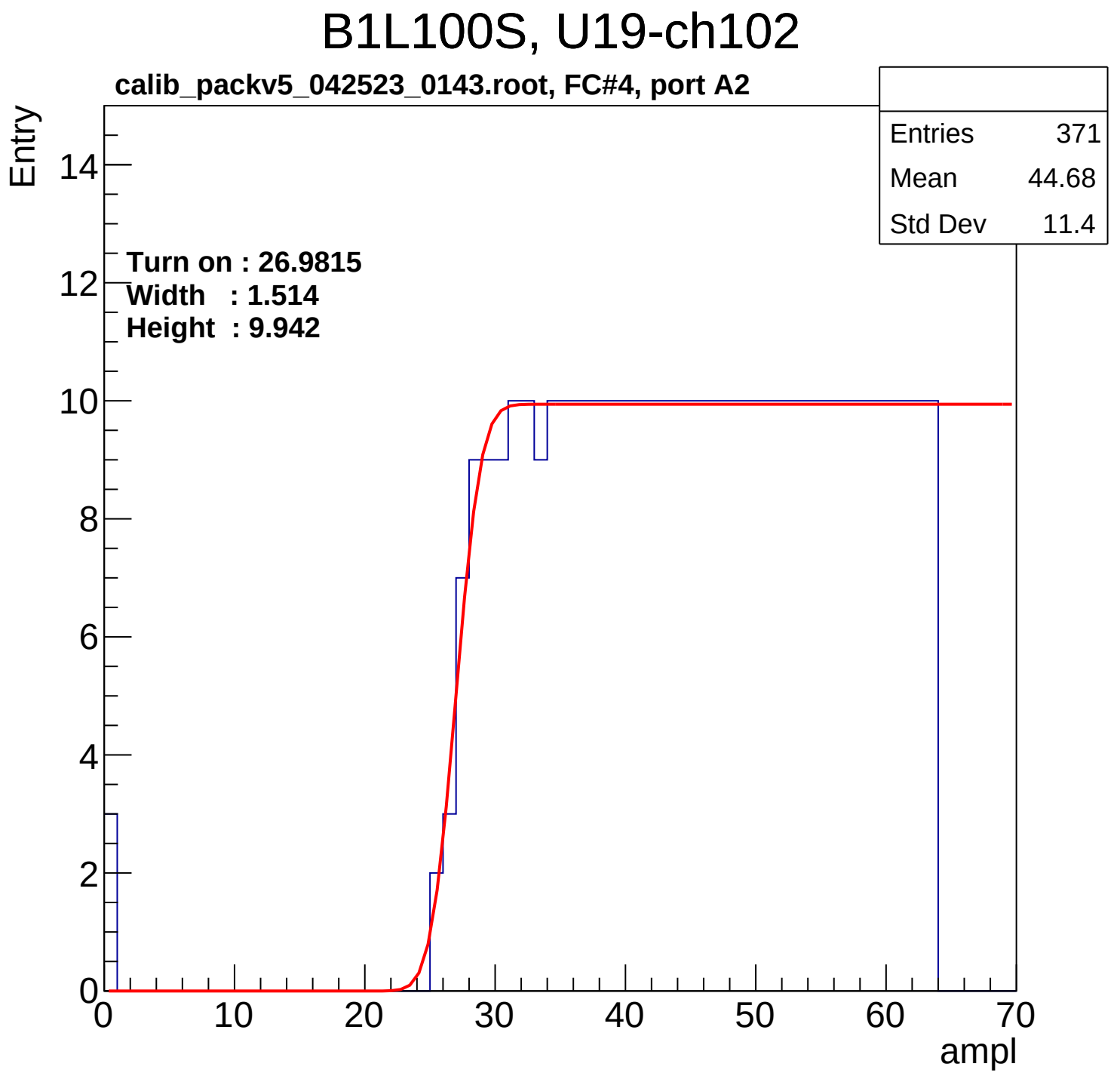
B1L100S, U19-ch102
calib_packv5_042523_0143.root, FC#4, port A2
Entries 371
Mean 44.68
Std Dev 11.4
Turn on : 26.9815
Width : 1.514
Height : 9.942
Entry
ampl
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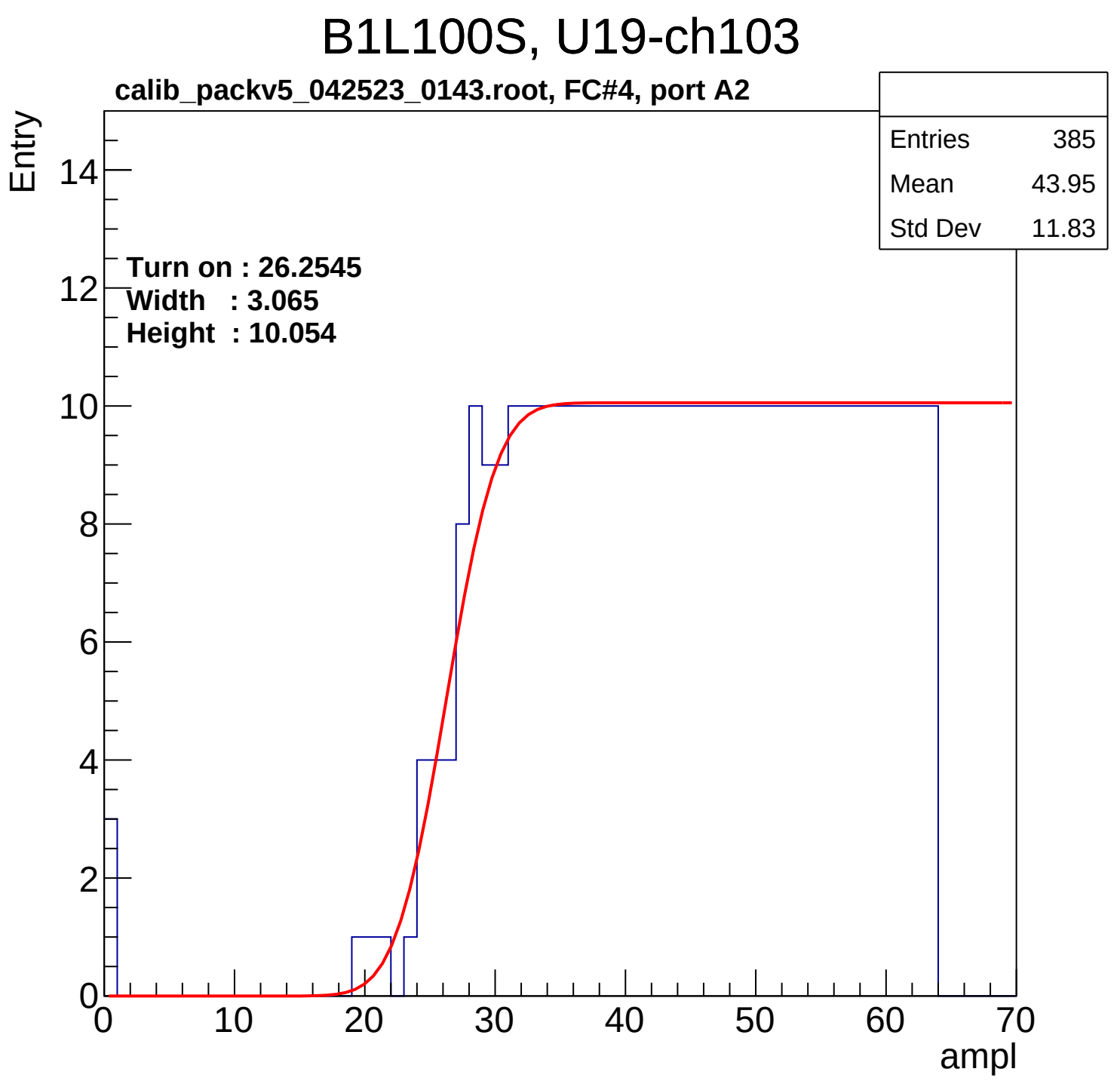
B1L100S, U19-ch103
calib_packv5_042523_0143.root, FC#4, port A2
Entries 385
Mean 43.95
Std Dev 11.83
Turn on : 26.2545
Width : 3.065
Height : 10.054
Entry
ampl
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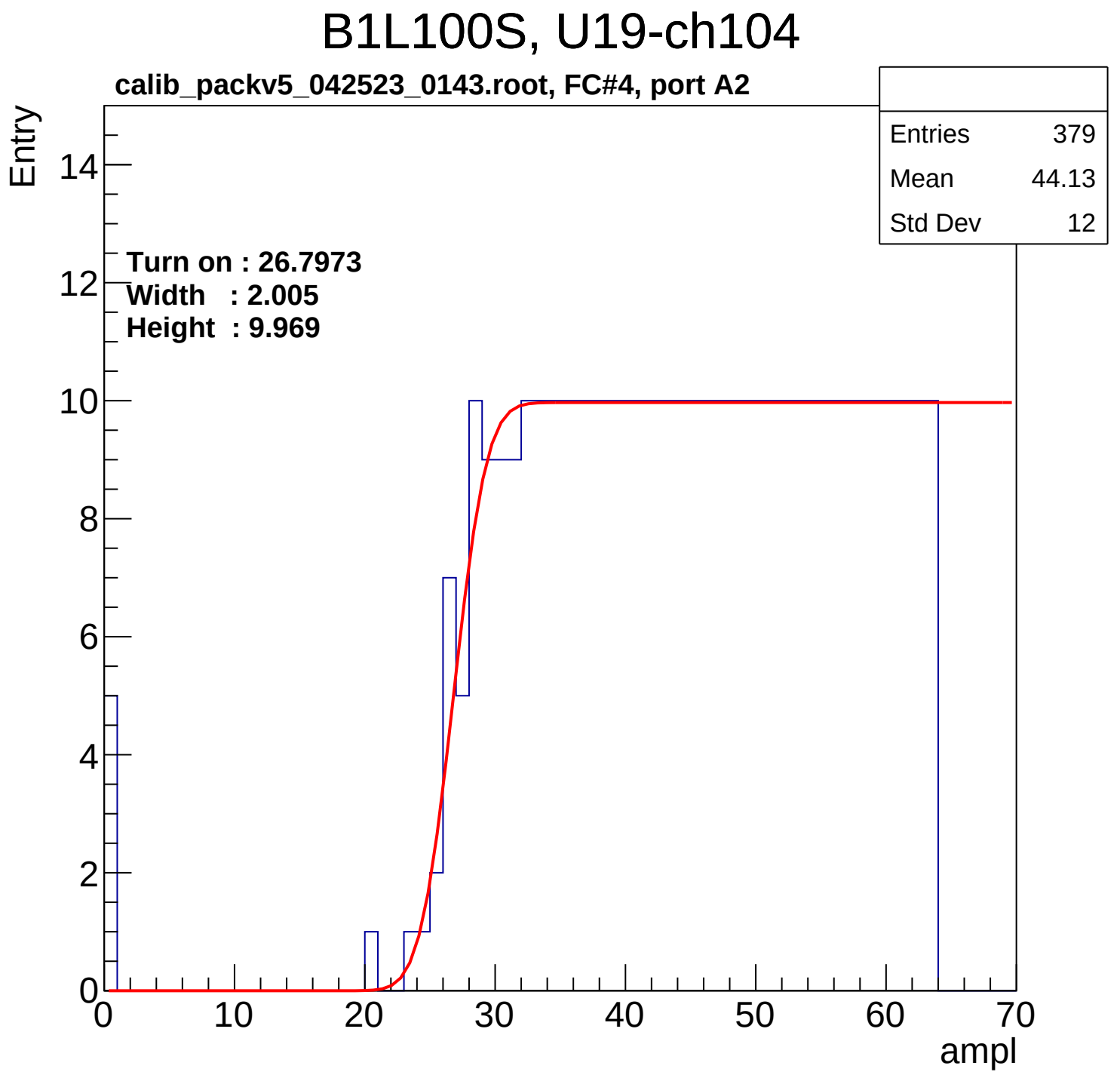
B1L100S, U19-ch104
calib_packv5_042523_0143.root, FC#4, port A2
Entries 379
Mean 44.13
Std Dev 12
Turn on : 26.7973
Width : 2.005
Height : 9.969
Entry
ampl
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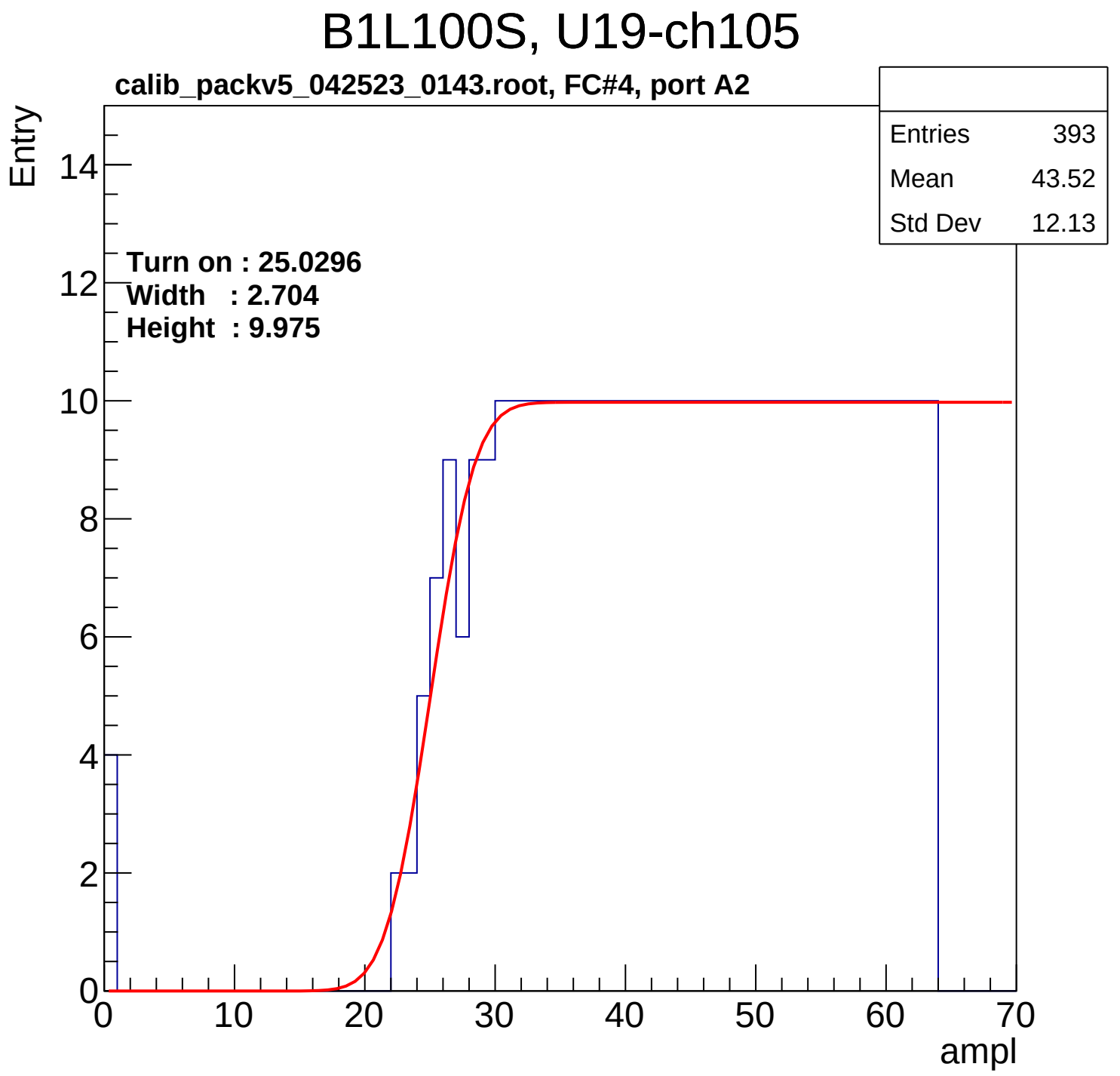
B1L100S, U19-ch105
calib_packv5_042523_0143.root, FC#4, port A2
Entries 393
Mean 43.52
Std Dev 12.13
Turn on : 25.0296
Width : 2.704
Height : 9.975
Entry
ampl
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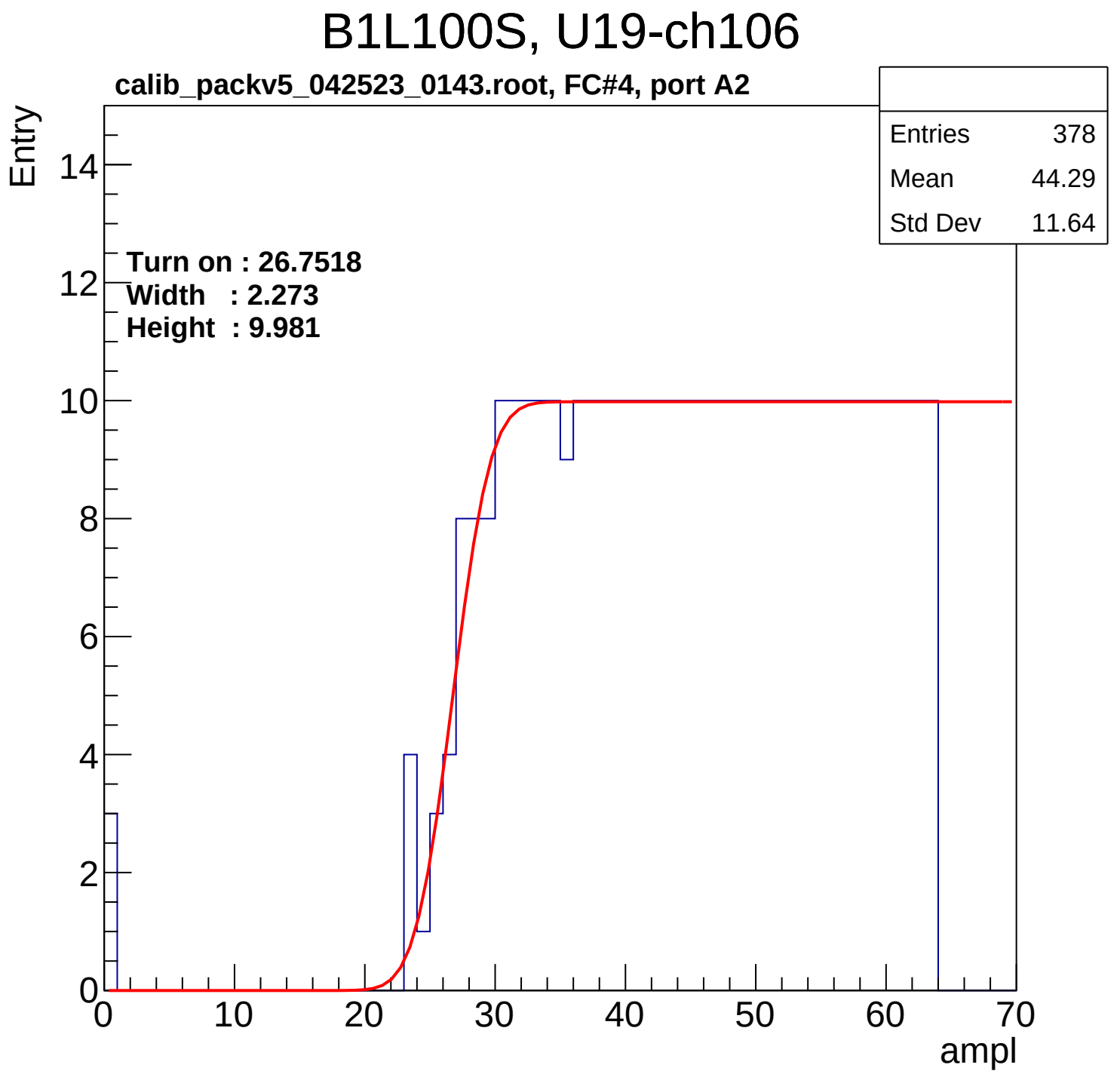
B1L100S, U19-ch106
calib_packv5_042523_0143.root, FC#4, port A2
Entries 378
Mean 44.29
Std Dev 11.64
Turn on : 26.7518
Width : 2.273
Height : 9.981
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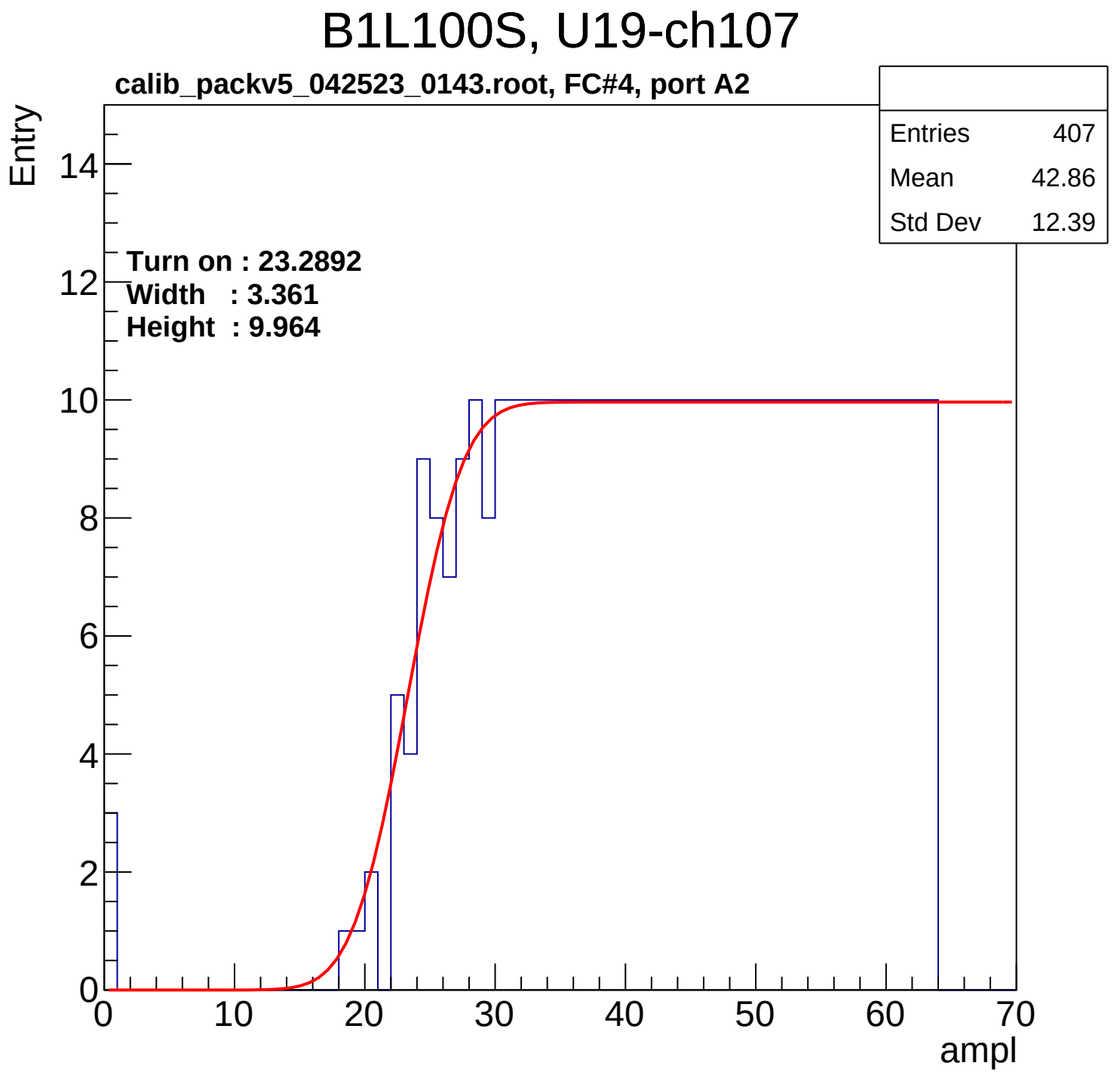
B1L100S, U19-ch107
calib_packv5_042523_0143.root, FC#4, port A2
Entries 407
Mean 42.86
Std Dev 12.39
Turn on : 23.2892
Width : 3.361
Height : 9.964
Entry
ampl
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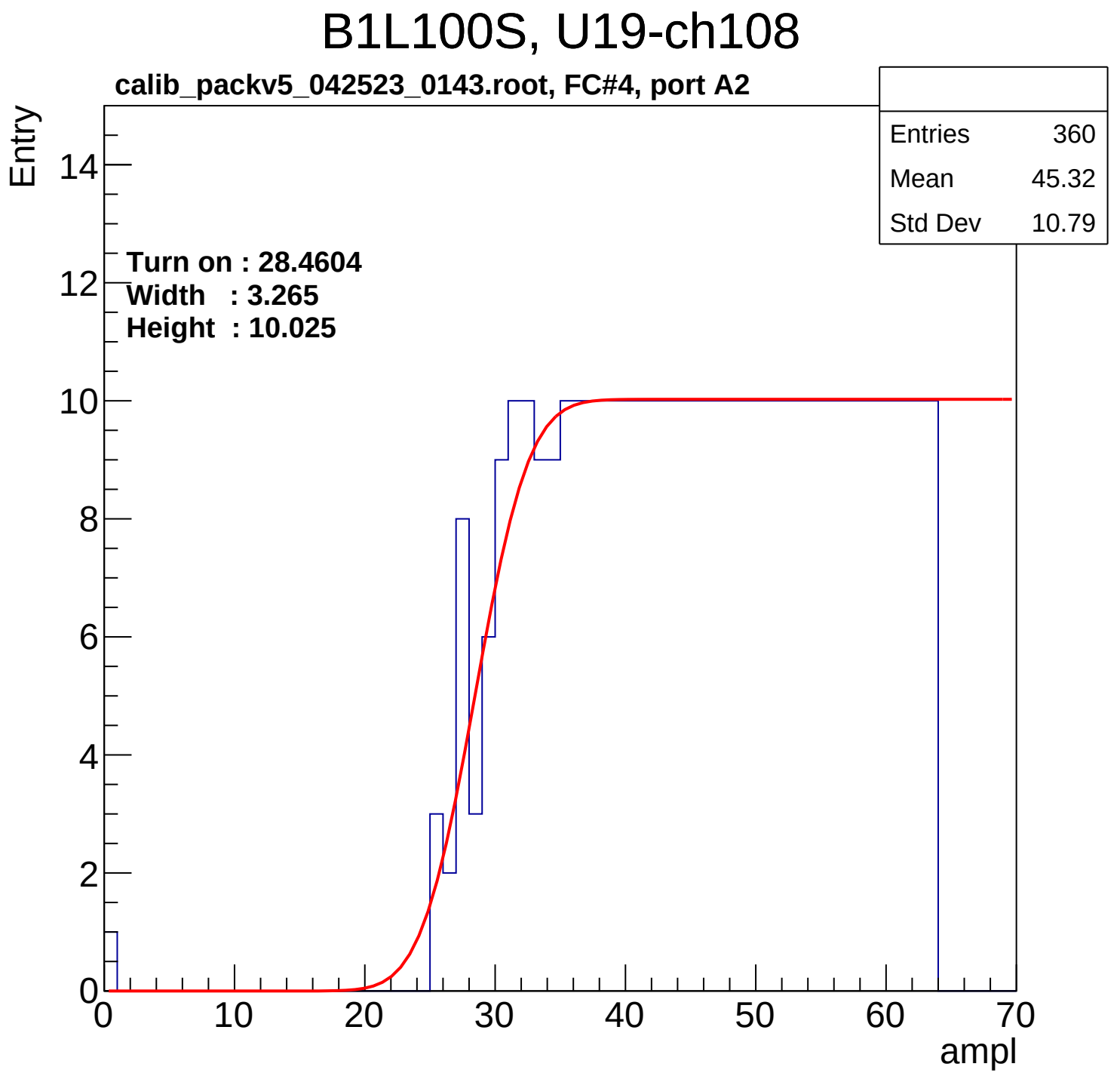
B1L100S, U19-ch108
calib_packv5_042523_0143.root, FC#4, port A2
Entries 360
Mean 45.32
Std Dev 10.79
Turn on : 28.4604
Width : 3.265
Height : 10.025
Entry
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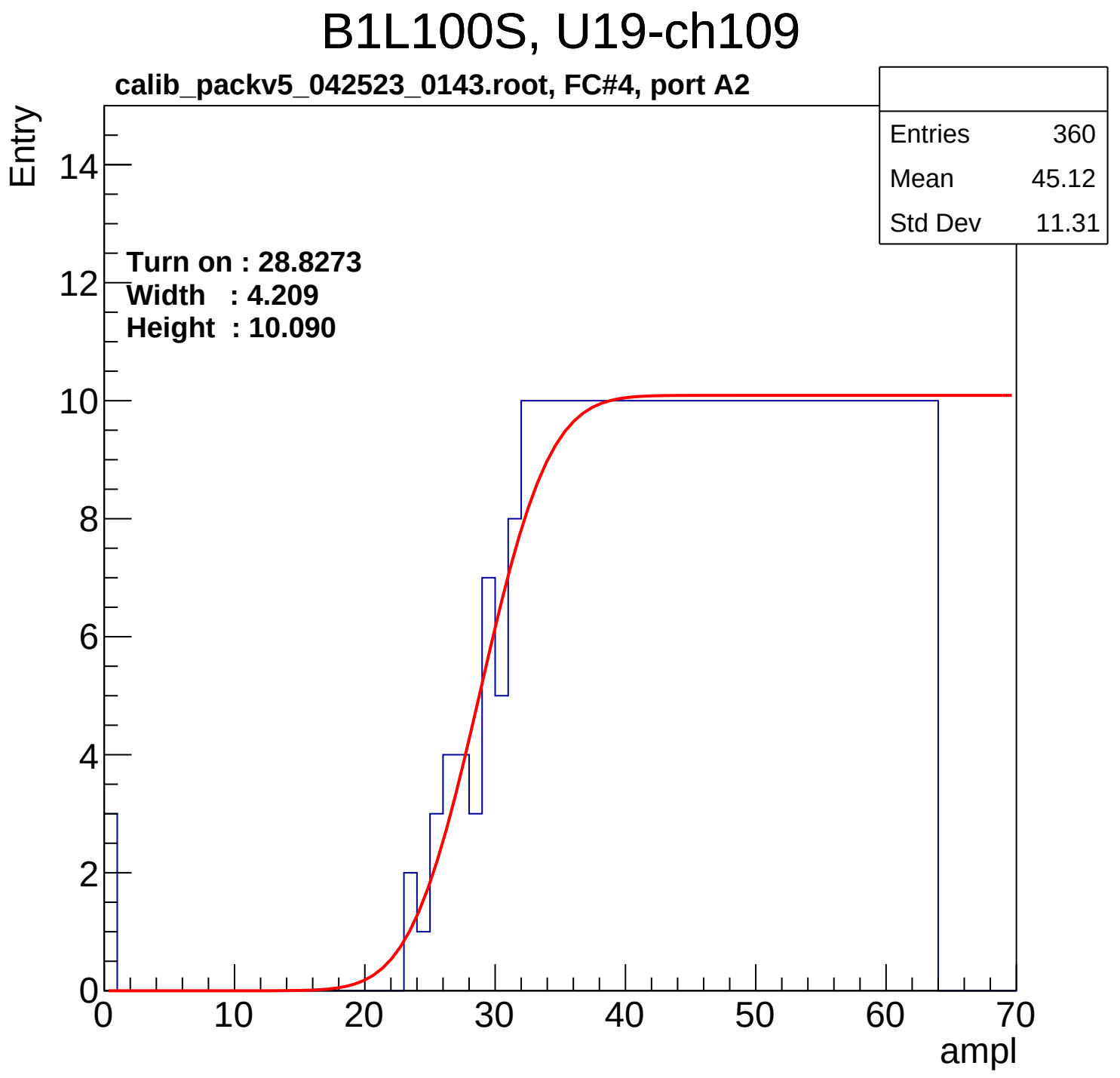
B1L100S, U19-ch109
calib_packv5_042523_0143.root, FC#4, port A2
Entries 360
Mean 45.12
Std Dev 11.31
Turn on : 28.8273
Width : 4.209
Height : 10.090
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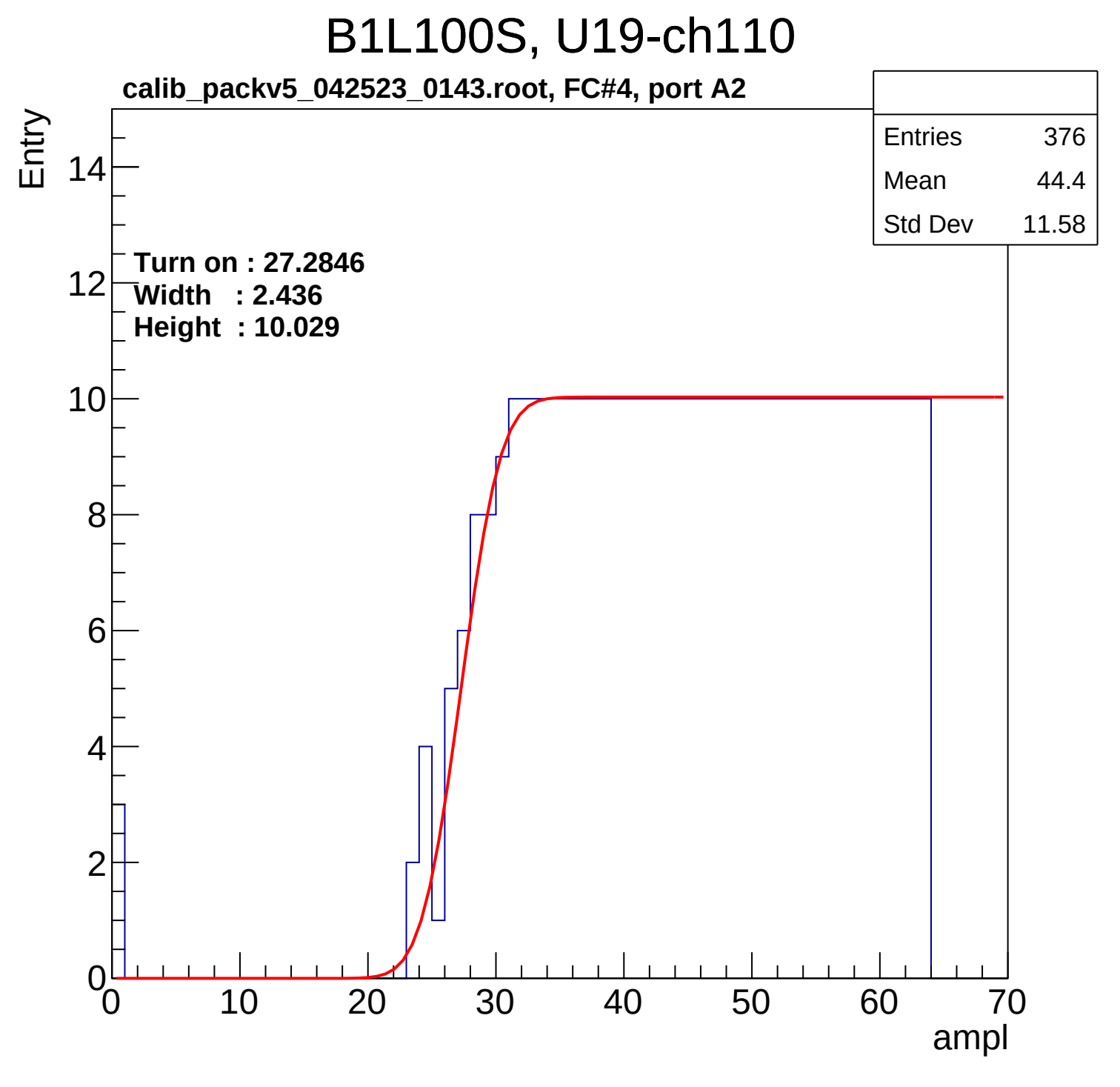
B1L100S, U19-ch110
calib_packv5_042523_0143.root, FC#4, port A2
Entries 376
Mean 44.4
Std Dev 11.58
Turn on : 27.2846
Width : 2.436
Height : 10.029
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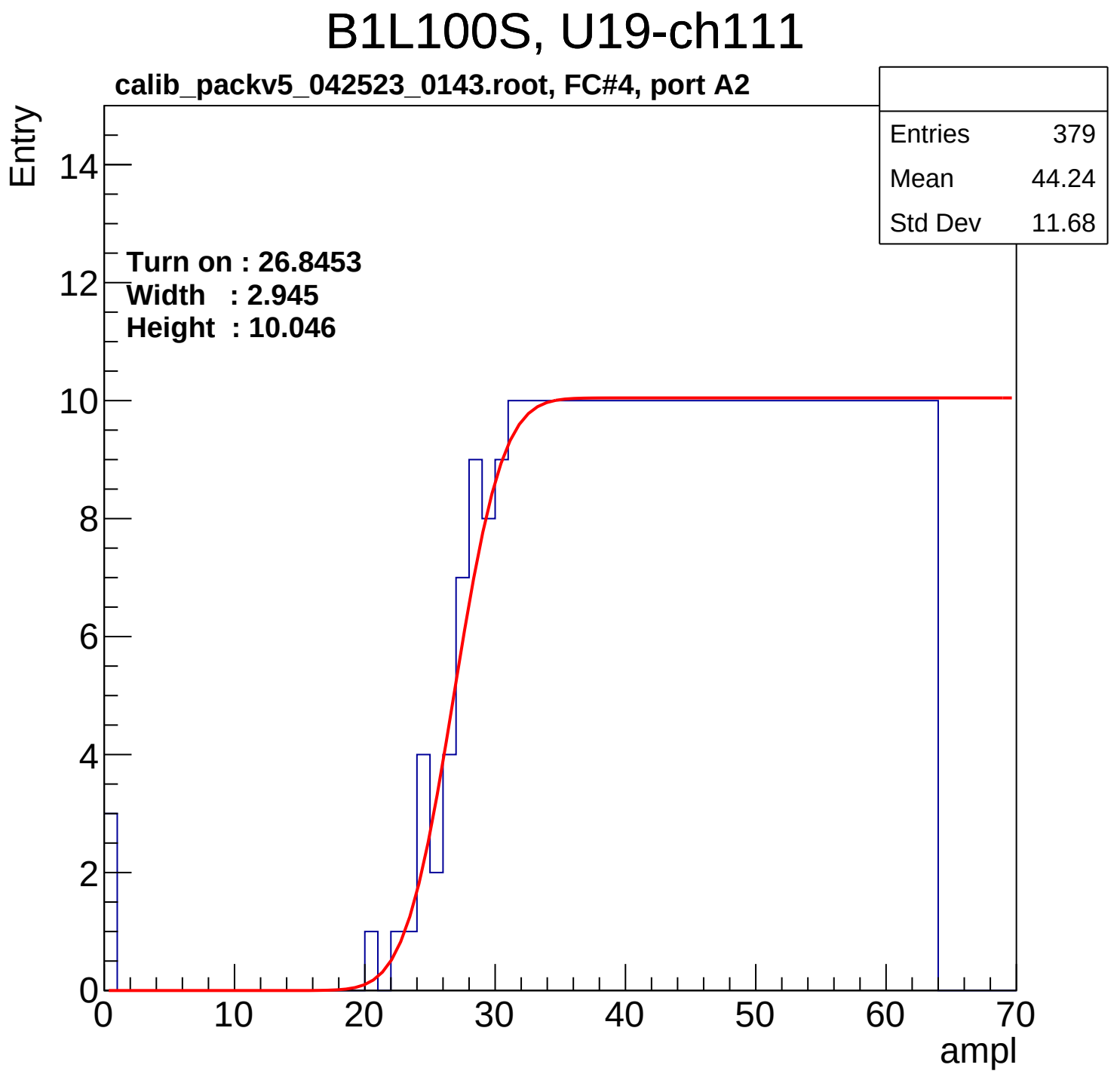
B1L100S, U19-ch111
calib_packv5_042523_0143.root, FC#4, port A2
Entries 379
Mean 44.24
Std Dev 11.68
Turn on : 26.8453
Width : 2.945
Height : 10.046
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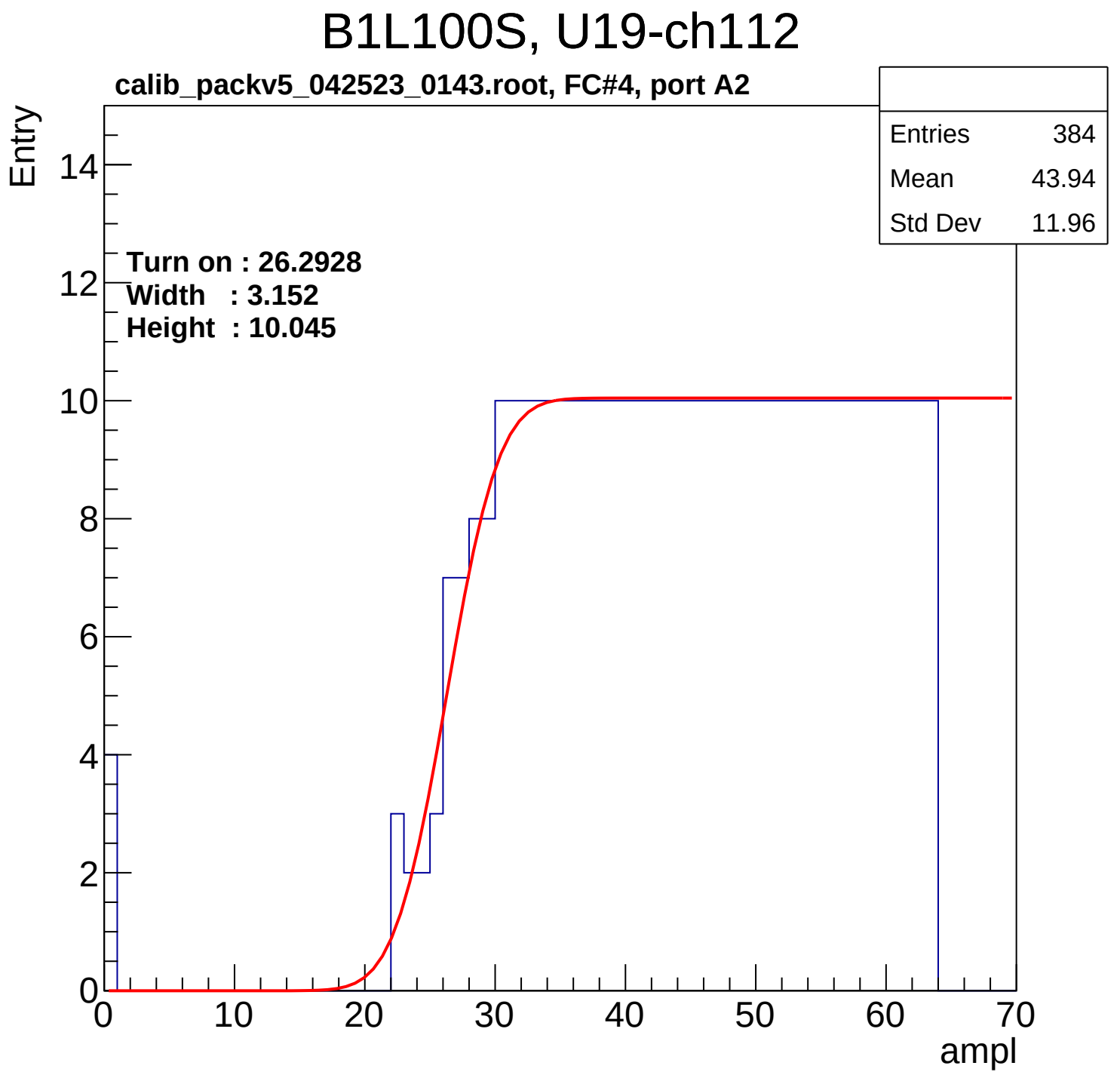
B1L100S, U19-ch112
calib_packv5_042523_0143.root, FC#4, port A2
Entries 384
Mean 43.94
Std Dev 11.96
Turn on : 26.2928
Width : 3.152
Height : 10.045
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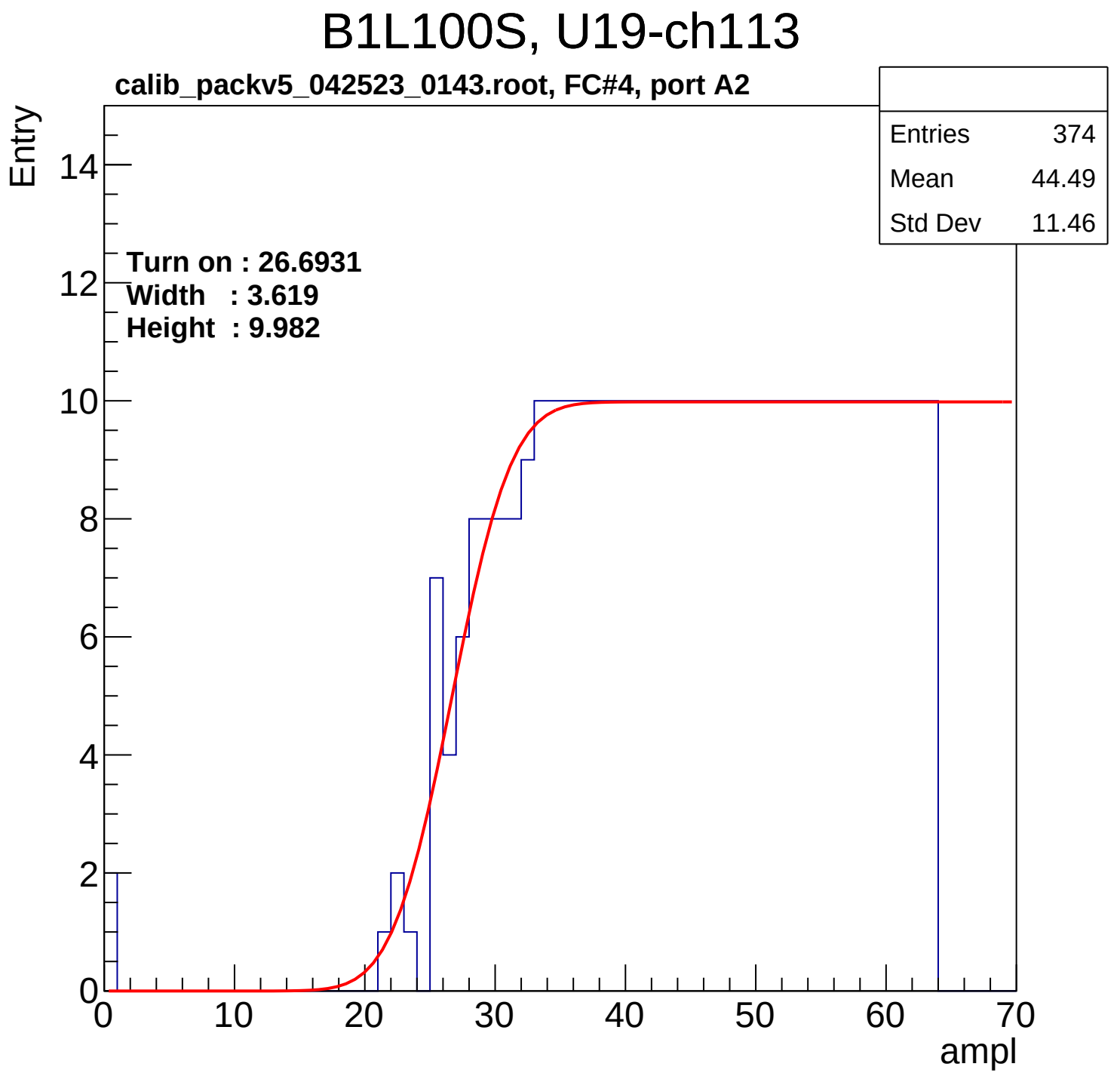
B1L100S, U19-ch113
calib_packv5_042523_0143.root, FC#4, port A2
Entries 374
Mean 44.49
Std Dev 11.46
Turn on : 26.6931
Width : 3.619
Height : 9.982
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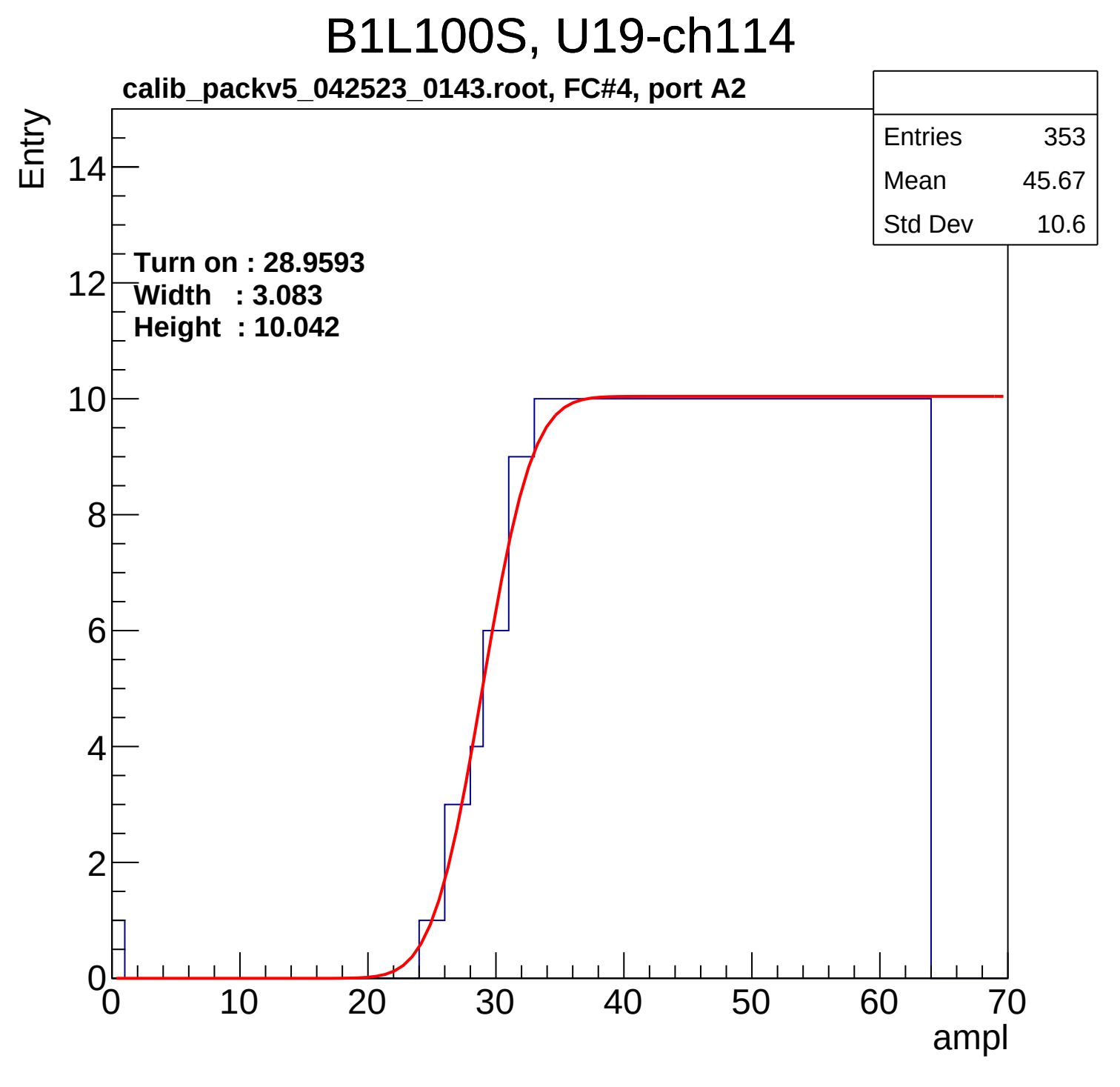
B1L100S, U19-ch114
calib_packv5_042523_0143.root, FC#4, port A2
Entries 353
Mean 45.67
Std Dev 10.6
Turn on : 28.9593
Width : 3.083
Height : 10.042
Entry
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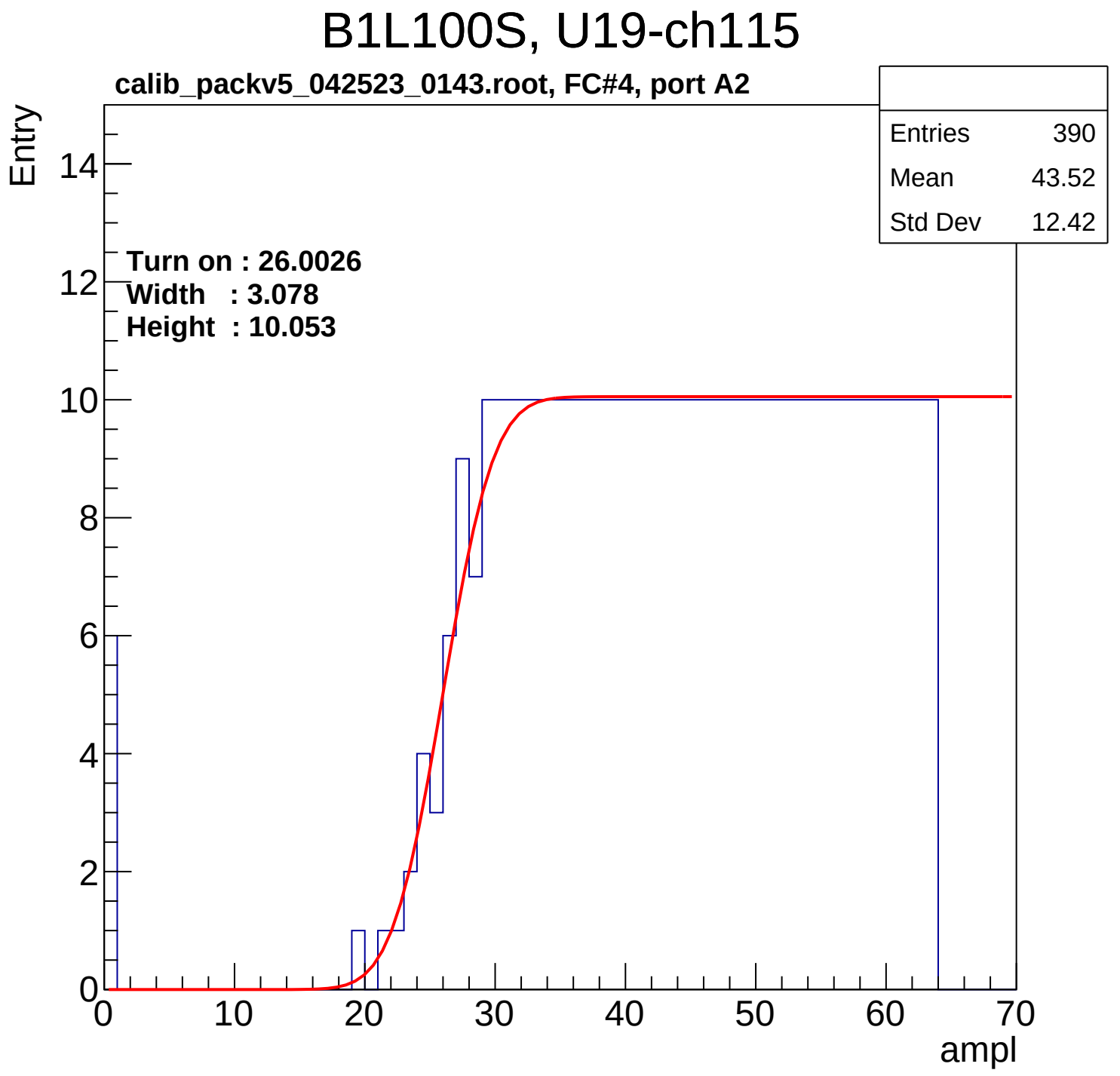
B1L100S, U19-ch115
calib_packv5_042523_0143.root, FC#4, port A2
Entries 390
Mean 43.52
Std Dev 12.42
Turn on : 26.0026
Width : 3.078
Height : 10.053
Entry
ampl
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4
6
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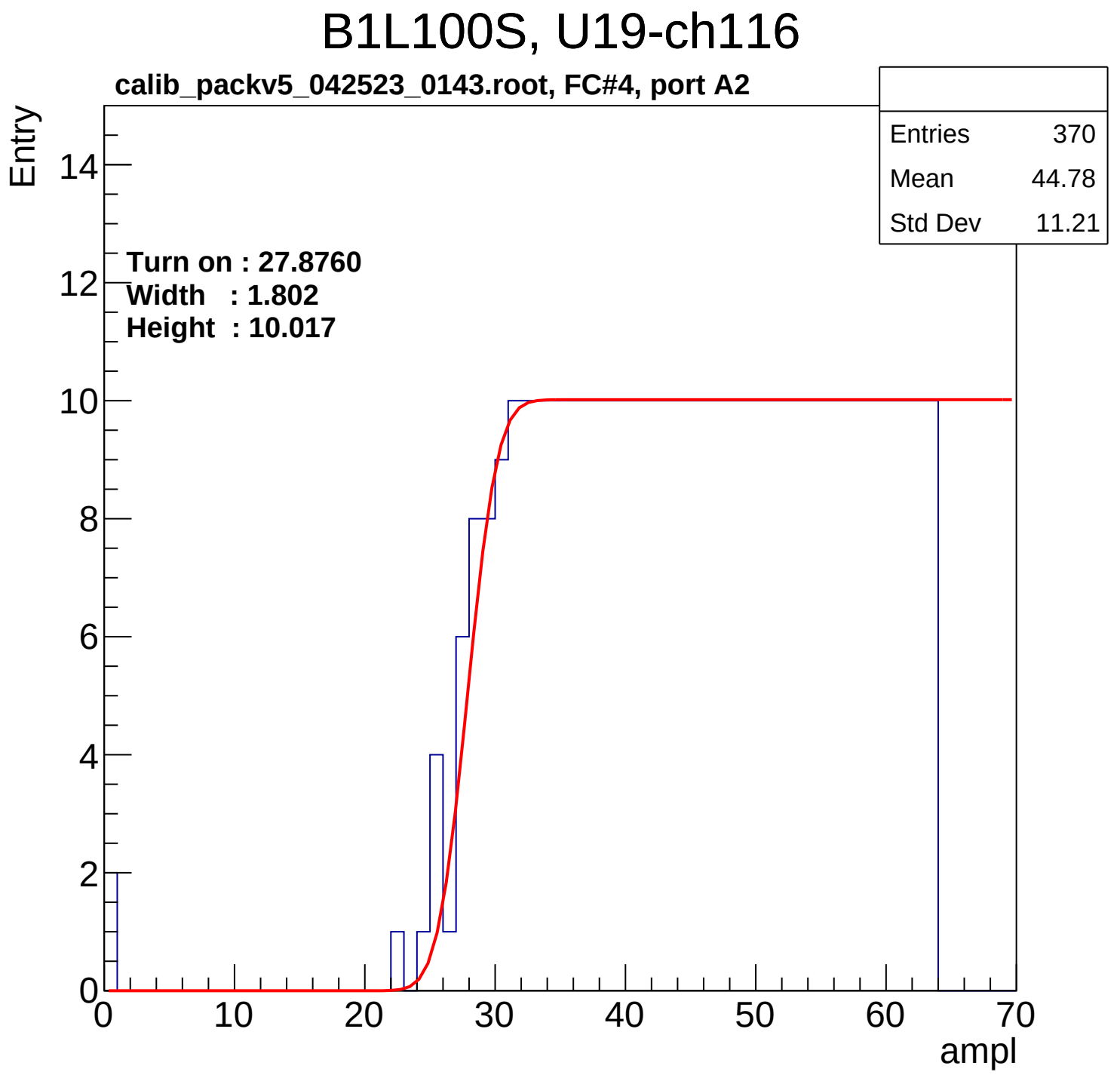
B1L100S, U19-ch116
calib_packv5_042523_0143.root, FC#4, port A2
Entries 370
Mean 44.78
Std Dev 11.21
Turn on : 27.8760
Width : 1.802
Height : 10.017
Entry
ampl
0
2
4
6
8
10
12
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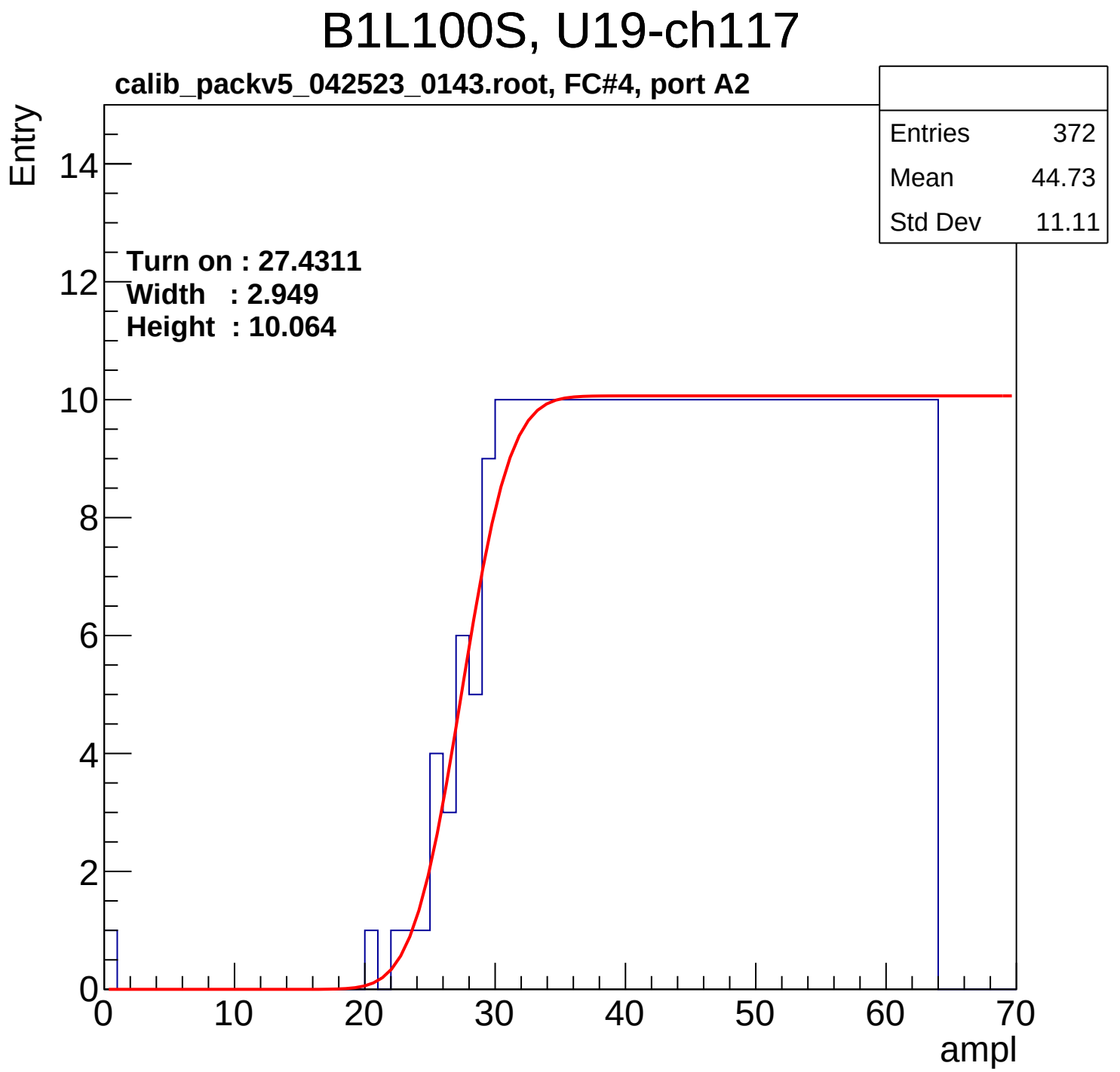
B1L100S, U19-ch117
calib_packv5_042523_0143.root, FC#4, port A2
Entries 372
Mean 44.73
Std Dev 11.11
Turn on : 27.4311
Width : 2.949
Height : 10.064
Entry
ampl
0
2
4
6
8
10
12
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0
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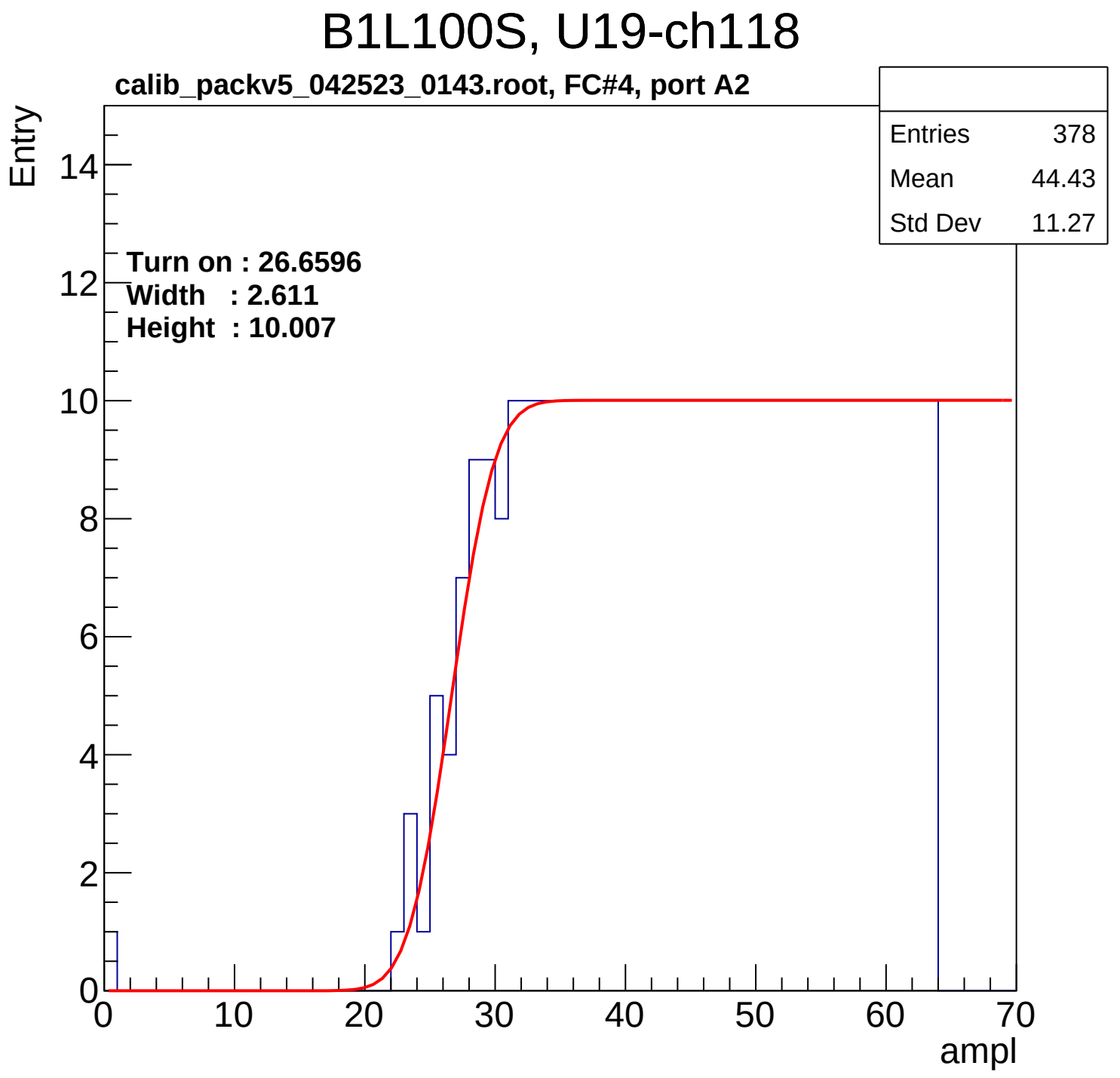
B1L100S, U19-ch118
calib_packv5_042523_0143.root, FC#4, port A2
Entries 378
Mean 44.43
Std Dev 11.27
Turn on : 26.6596
Width : 2.611
Height : 10.007
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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40
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60
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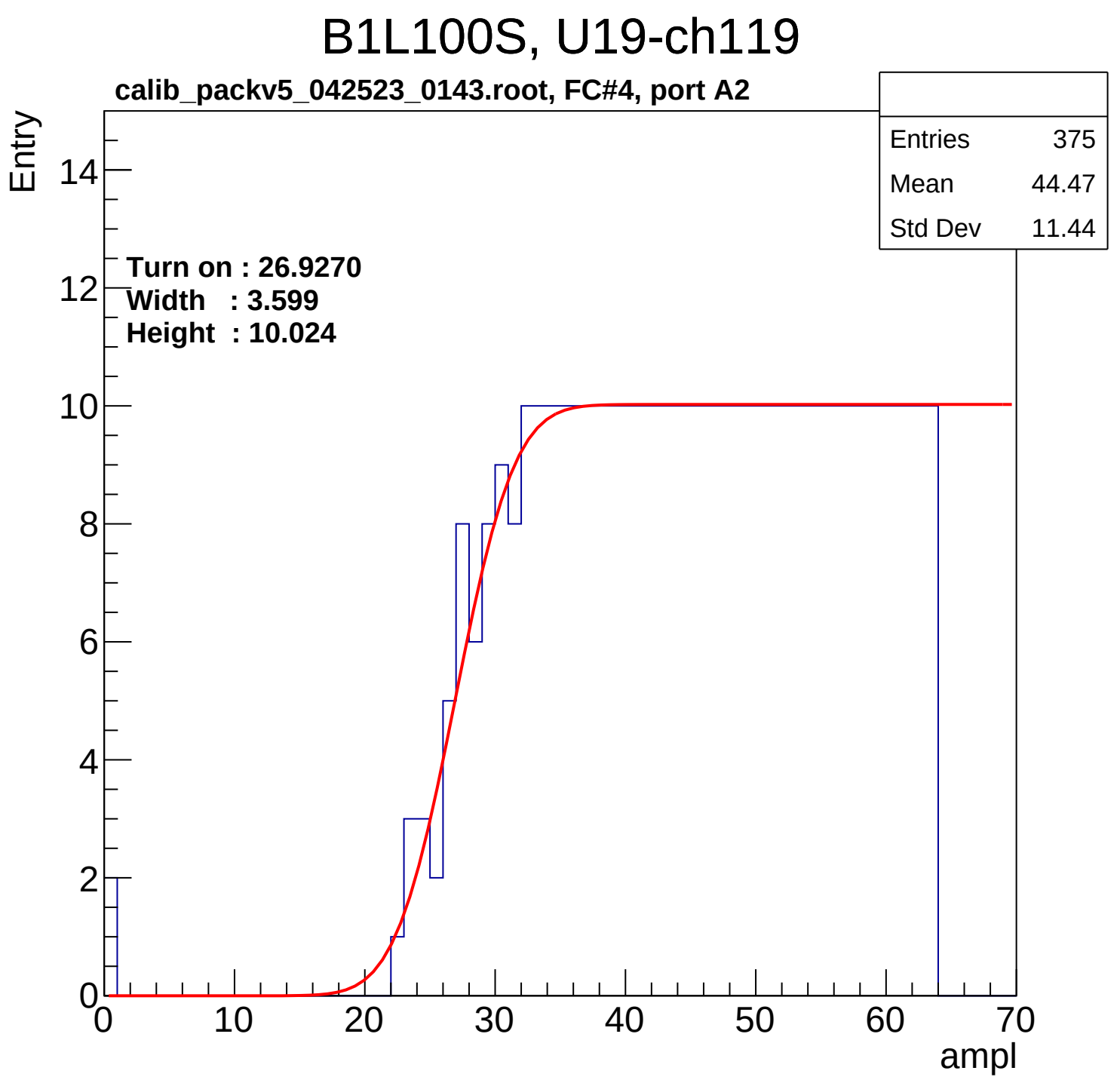
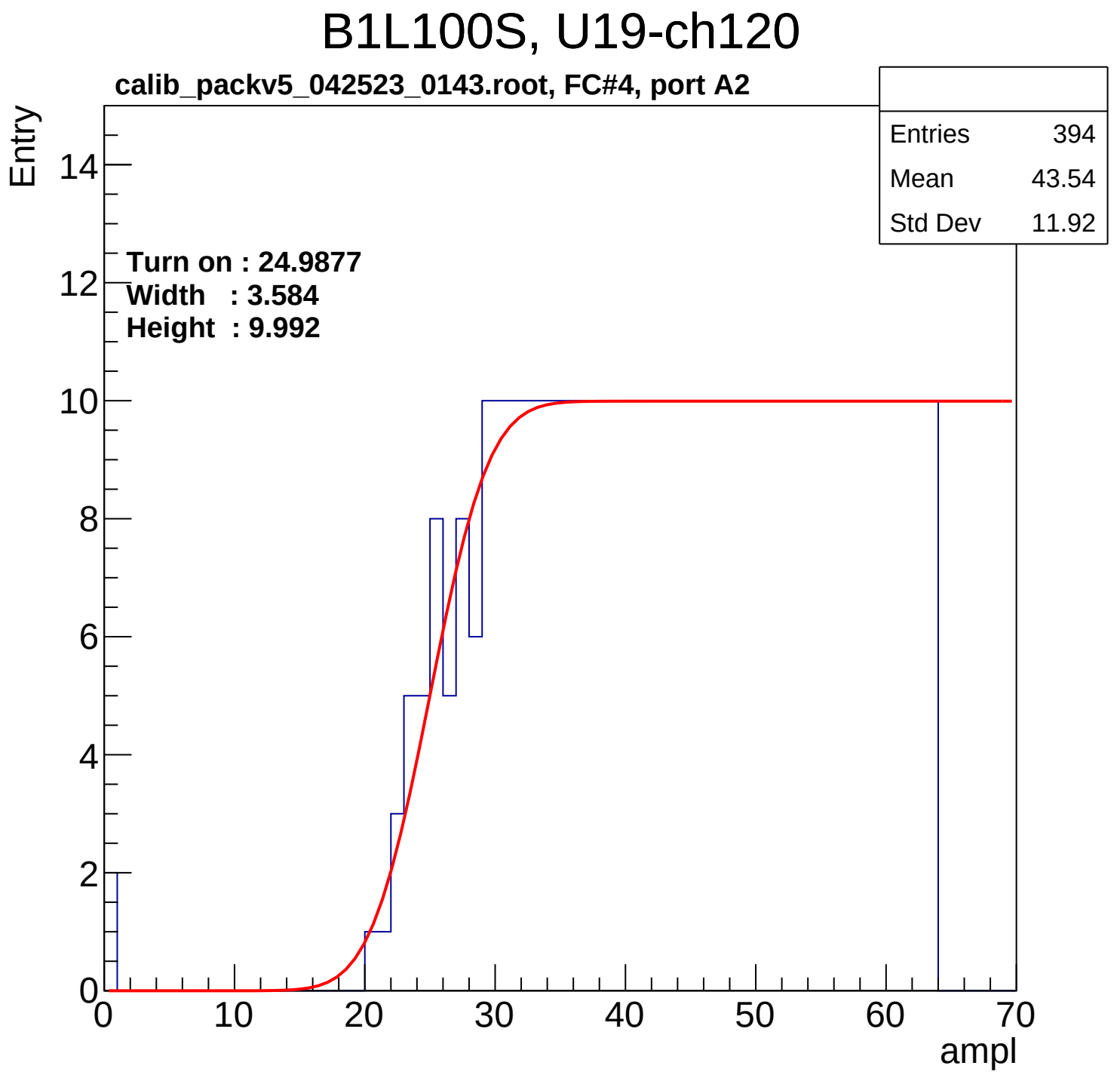

B1L100S, U19-ch119
calib_packv5_042523_0143.root, FC#4, port A2
Entries 375
Mean 44.47
Std Dev 11.44
Turn on : 26.9270
Width : 3.599
Height : 10.024
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L100S, U19-ch120
calib_packv5_042523_0143.root, FC#4, port A2
Entries 394
Mean 43.54
Std Dev 11.92
Turn on : 24.9877
Width : 3.584
Height : 9.992
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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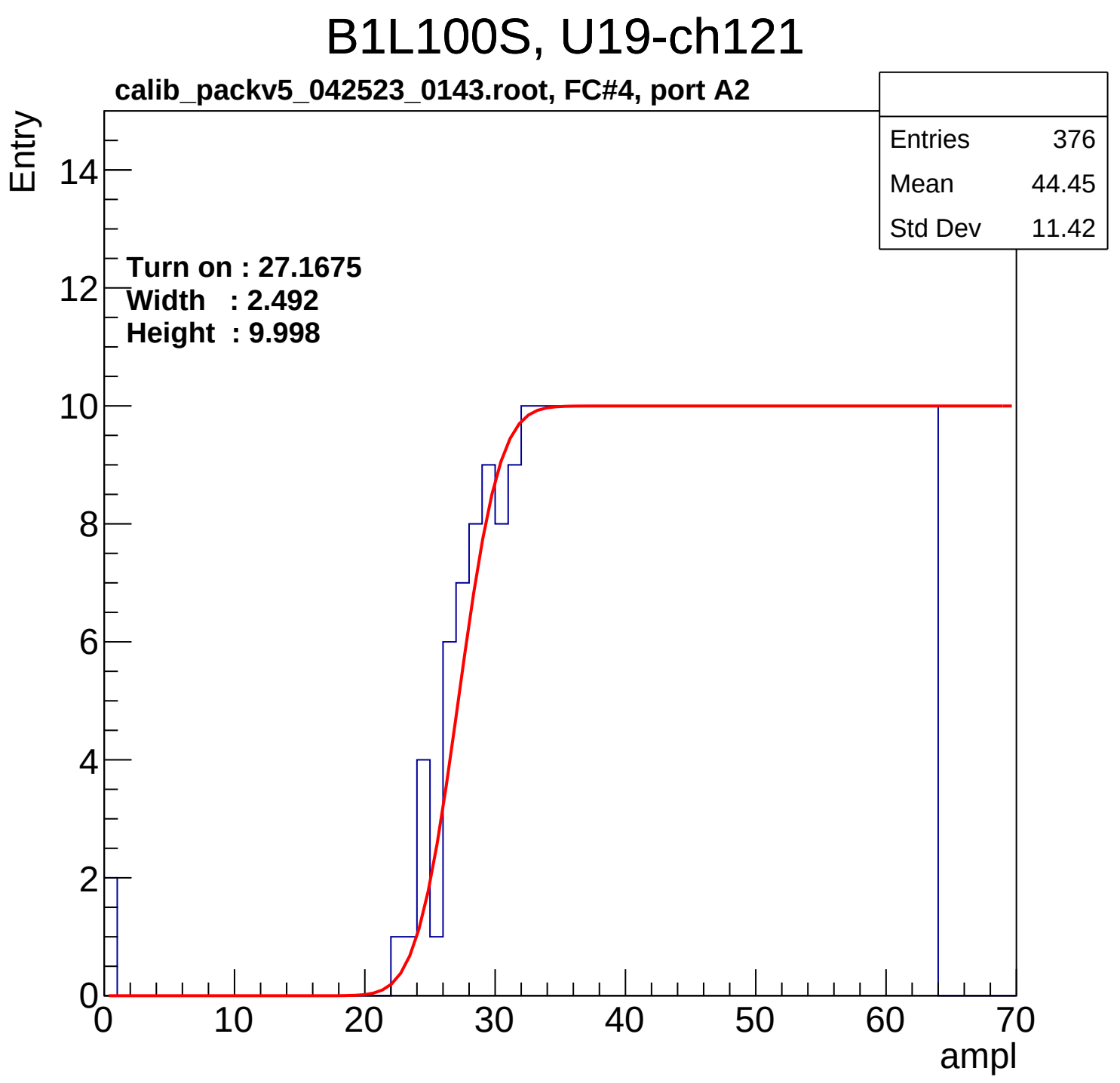
B1L100S, U19-ch121
calib_packv5_042523_0143.root, FC#4, port A2
Entries 376
Mean 44.45
Std Dev 11.42
Turn on : 27.1675
Width : 2.492
Height : 9.998
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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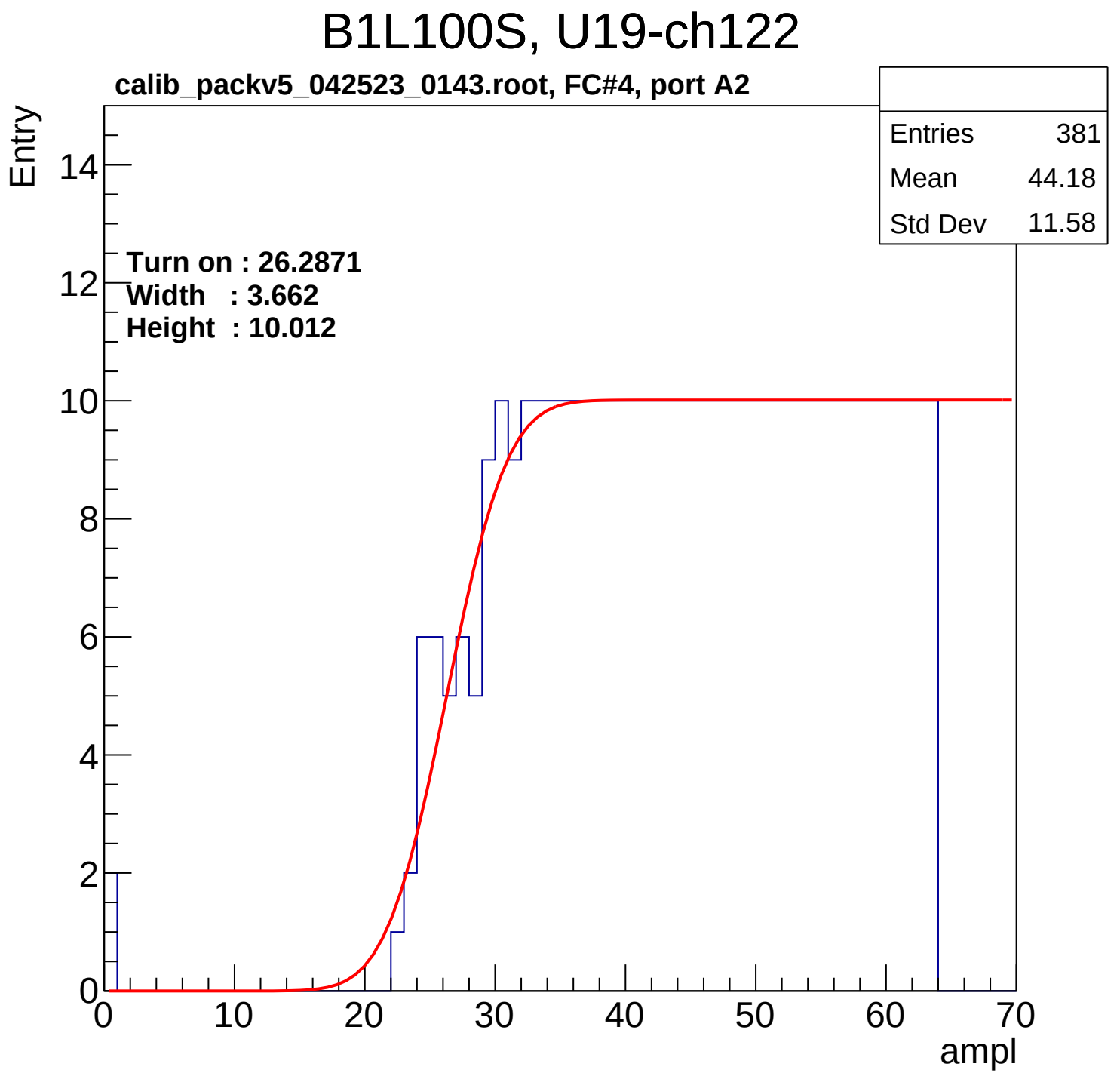
B1L100S, U19-ch122
calib_packv5_042523_0143.root, FC#4, port A2
Entries 381
Mean 44.18
Std Dev 11.58
Turn on : 26.2871
Width : 3.662
Height : 10.012
Entry
ampl
0
2
4
6
8
10
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0
10
20
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40
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60
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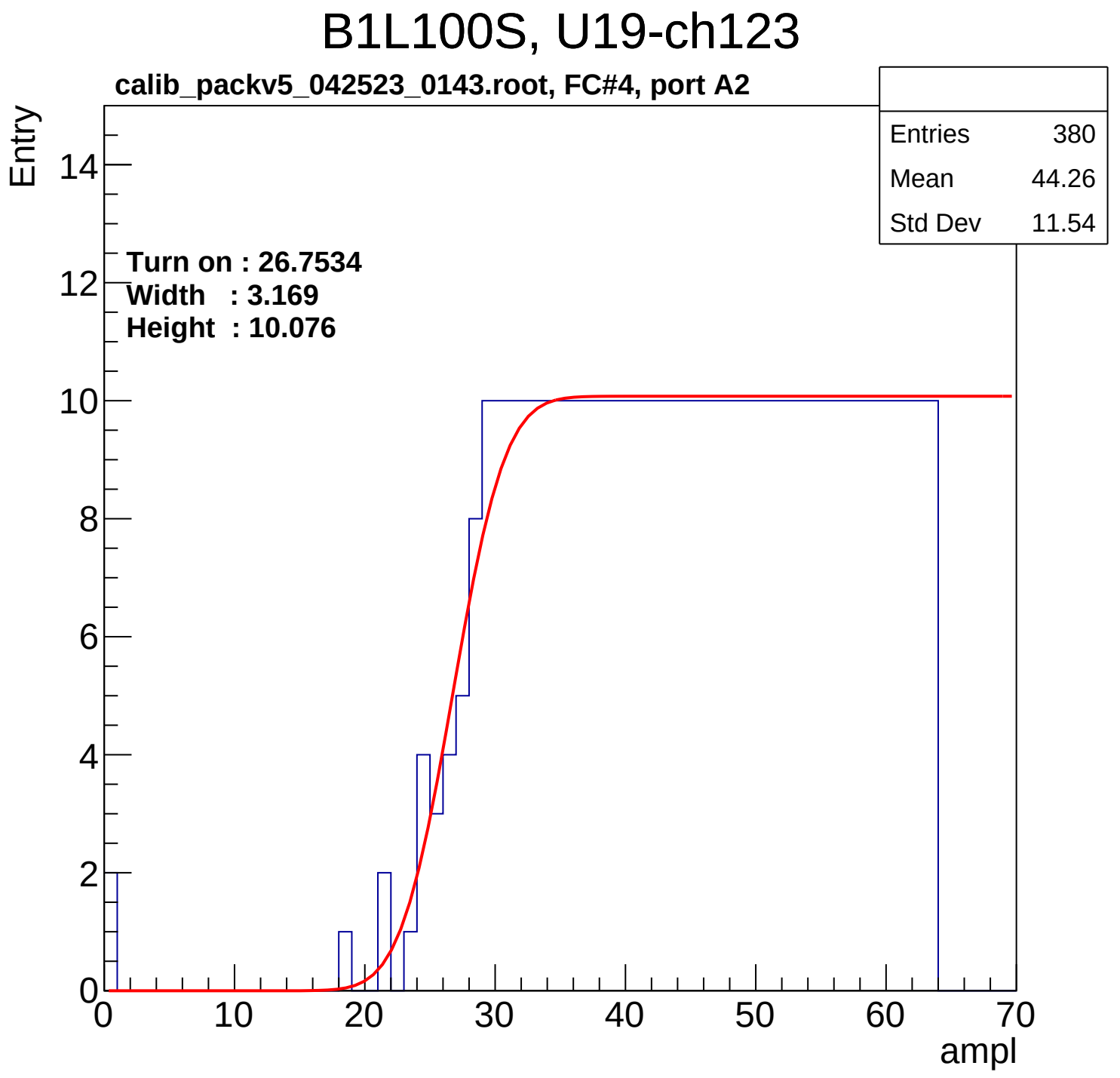
B1L100S, U19-ch123
calib_packv5_042523_0143.root, FC#4, port A2
Entries 380
Mean 44.26
Std Dev 11.54
Turn on : 26.7534
Width : 3.169
Height : 10.076
Entry
ampl
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2
4
6
8
10
12
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0
10
20
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40
50
60
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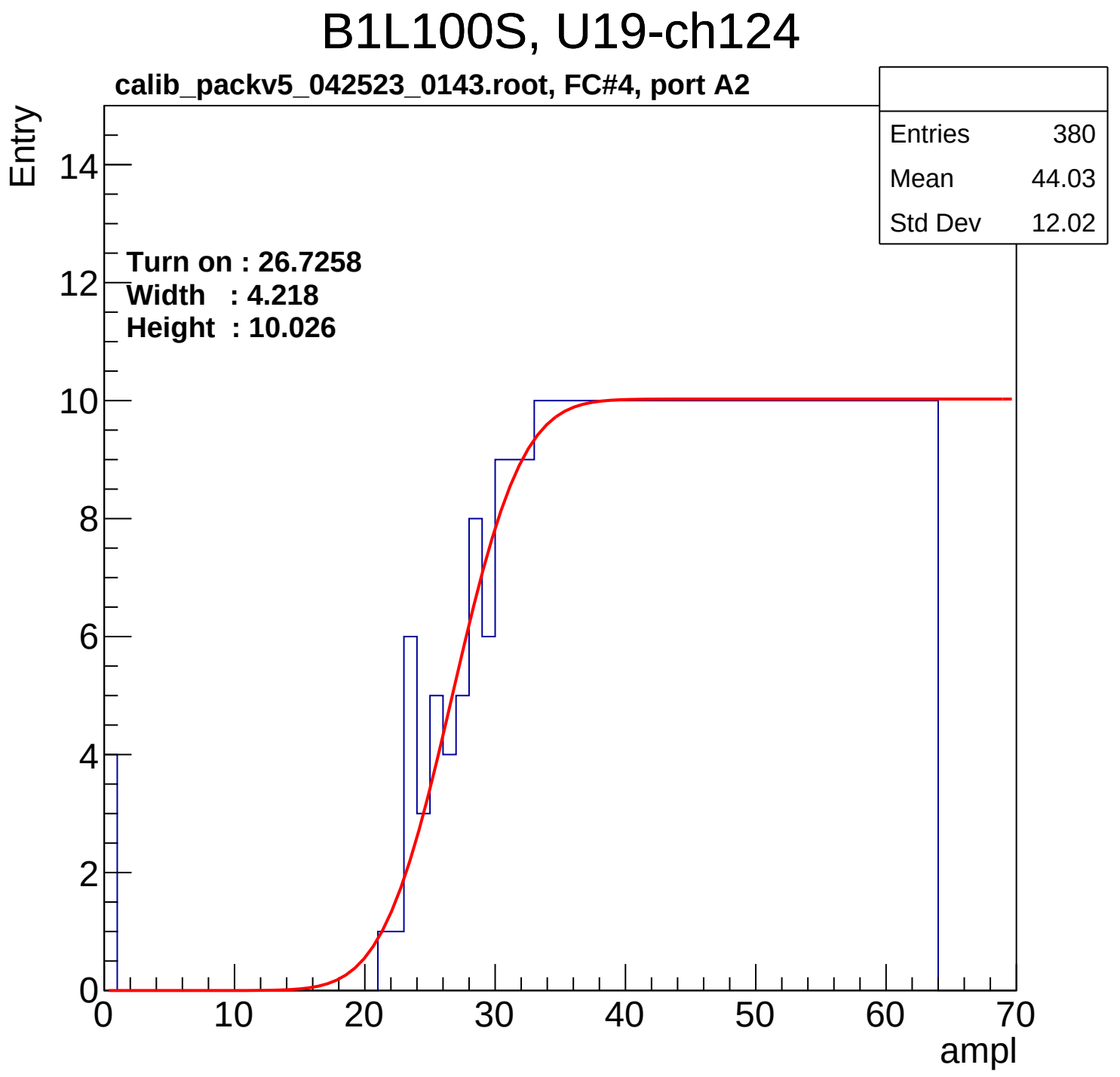
B1L100S, U19-ch124
calib_packv5_042523_0143.root, FC#4, port A2
Entries 380
Mean 44.03
Std Dev 12.02
Turn on : 26.7258
Width : 4.218
Height : 10.026
Entry
ampl
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2
4
6
8
10
12
14
0
10
20
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40
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60
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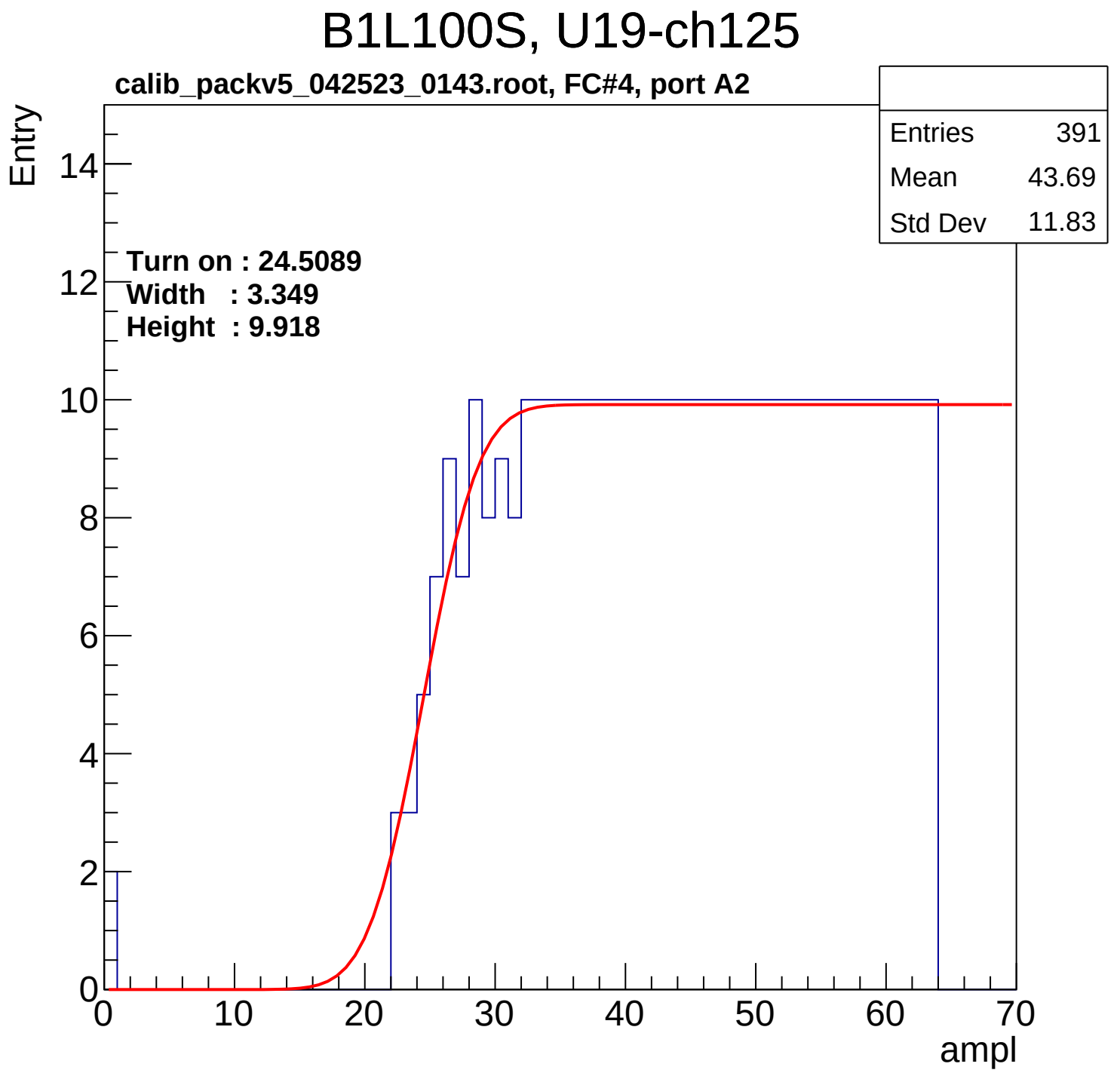
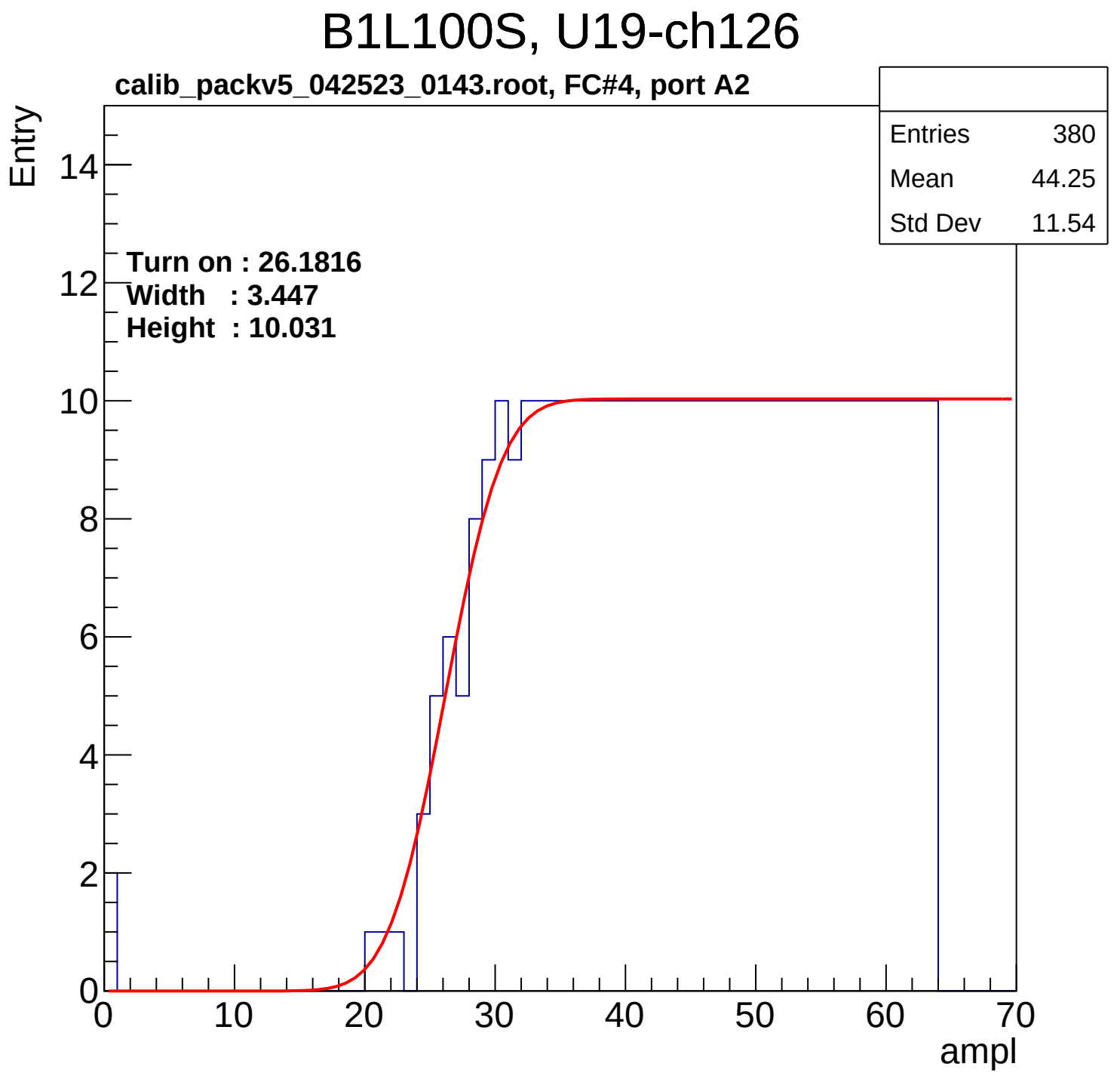

B1L100S, U19-ch125
calib_packv5_042523_0143.root, FC#4, port A2
Entries 391
Mean 43.69
Std Dev 11.83
Turn on : 24.5089
Width : 3.349
Height : 9.918
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L100S, U19-ch126
calib_packv5_042523_0143.root, FC#4, port A2
Entries 380
Mean 44.25
Std Dev 11.54
Turn on : 26.1816
Width : 3.447
Height : 10.031
Entry
ampl
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6
8
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0
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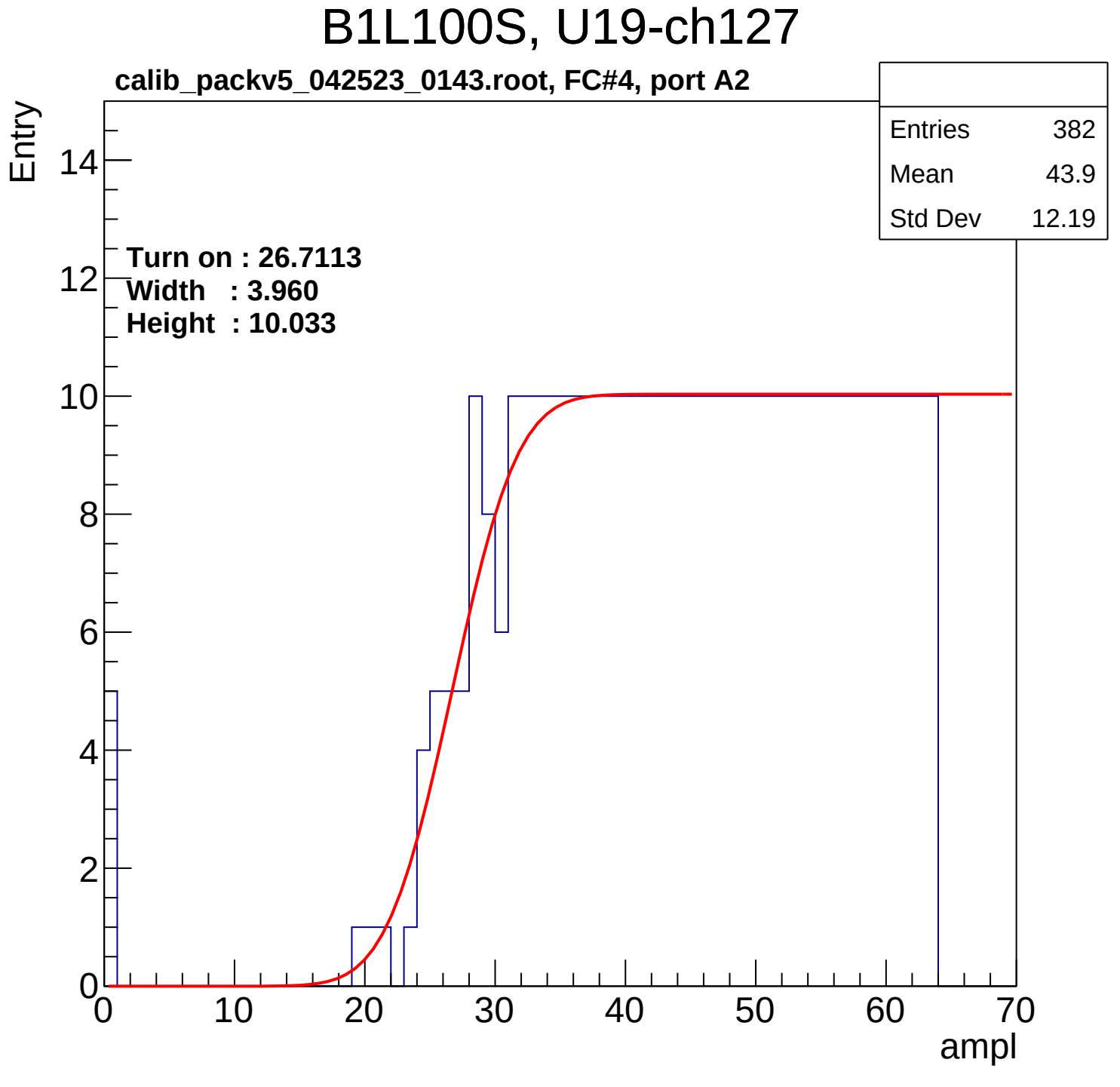
B1L100S, U19-ch127
calib_packv5_042523_0143.root, FC#4, port A2
Entries 382
Mean 43.9
Std Dev 12.19
Turn on : 26.7113
Width : 3.960
Height : 10.033
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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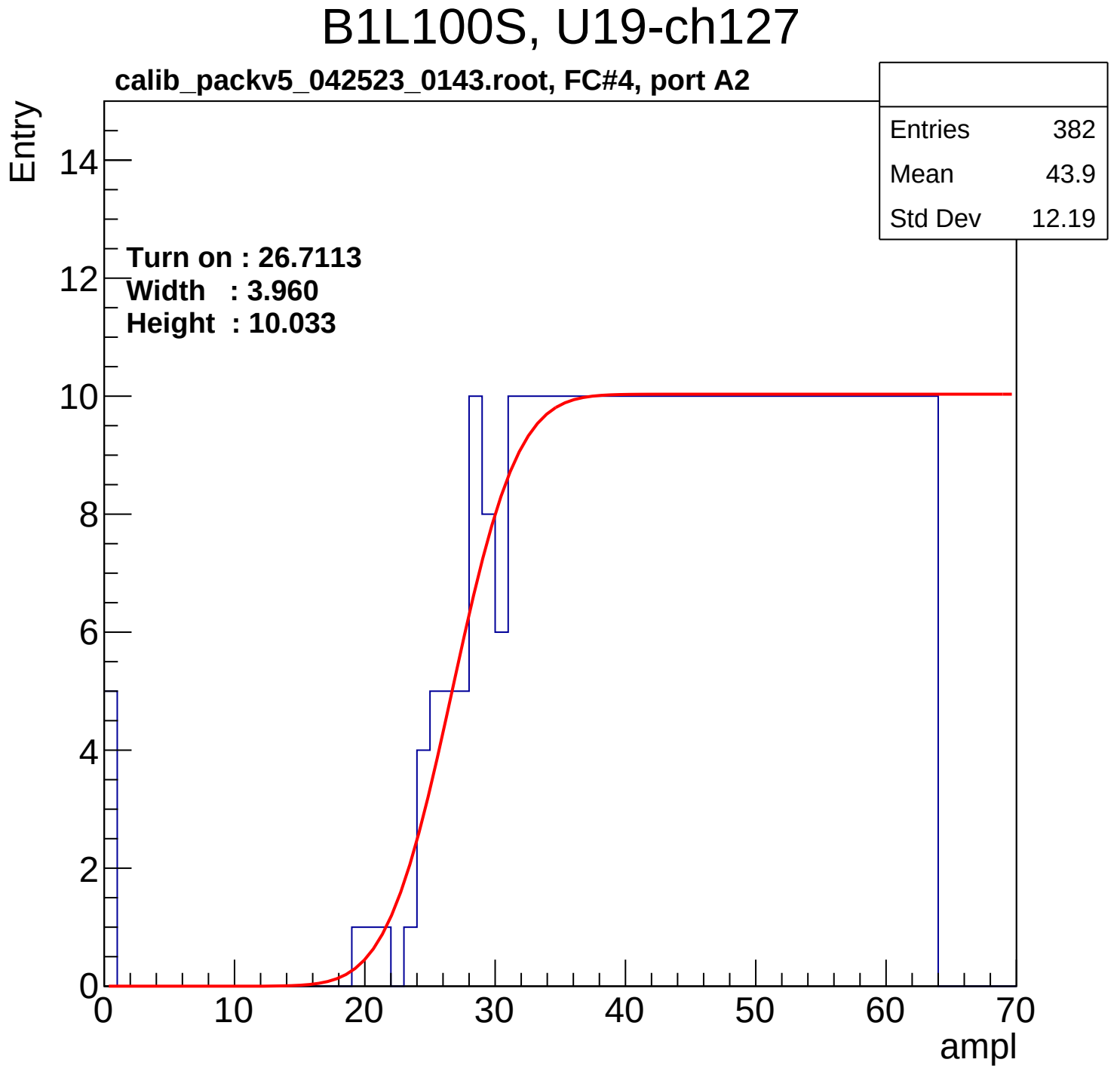
B1L100S, U19-ch127
calib_packv5_042523_0143.root, FC#4, port A2
Entries 382
Mean 43.9
Std Dev 12.19
Turn on : 26.7113
Width : 3.960
Height : 10.033
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70