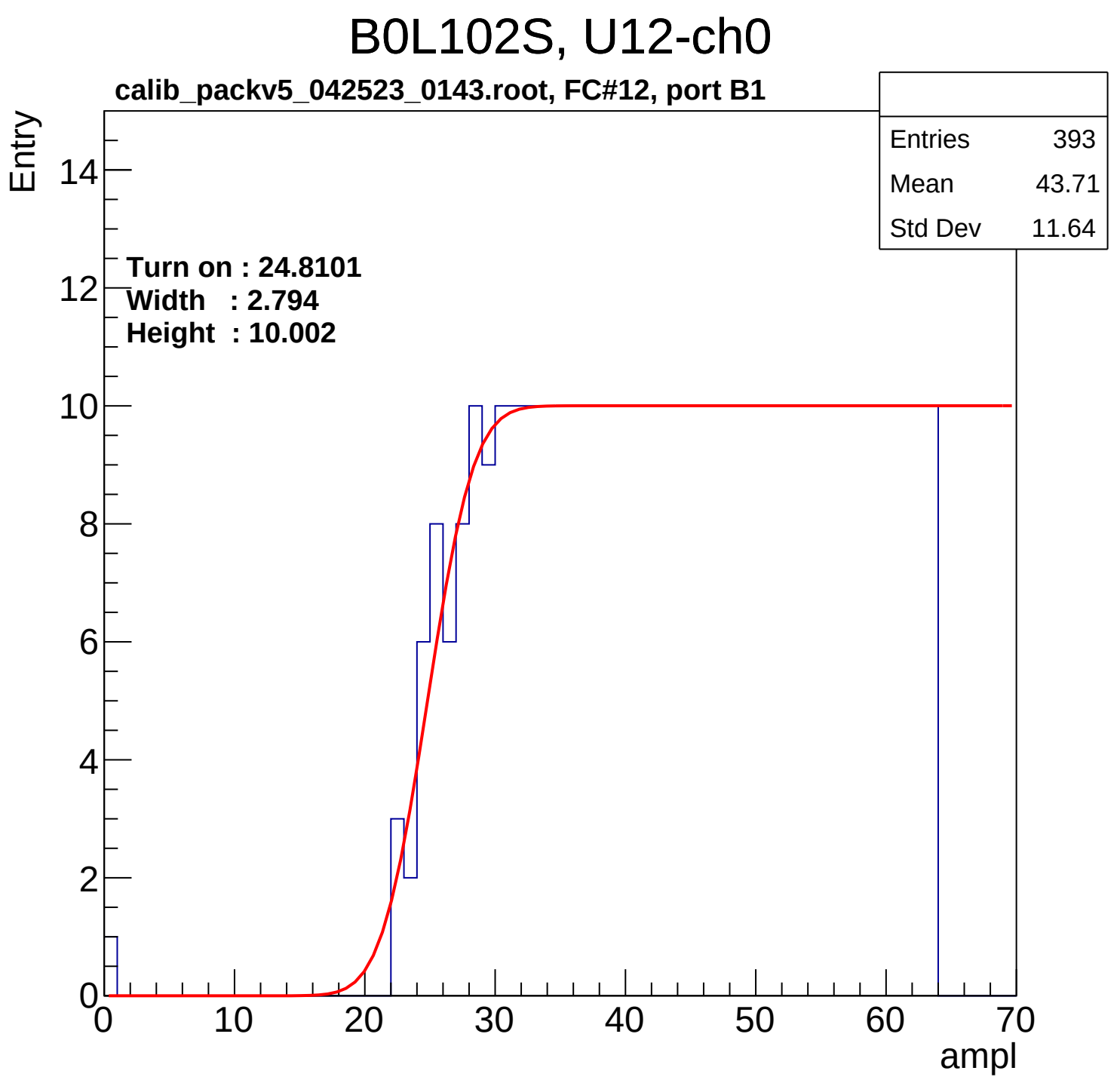
B0L102S, U12-ch0
calib_packv5_042523_0143.root, FC#12, port B1
Entries 393
Mean 43.71
Std Dev 11.64
Turn on : 24.8101
Width : 2.794
Height : 10.002
Entry
ampl
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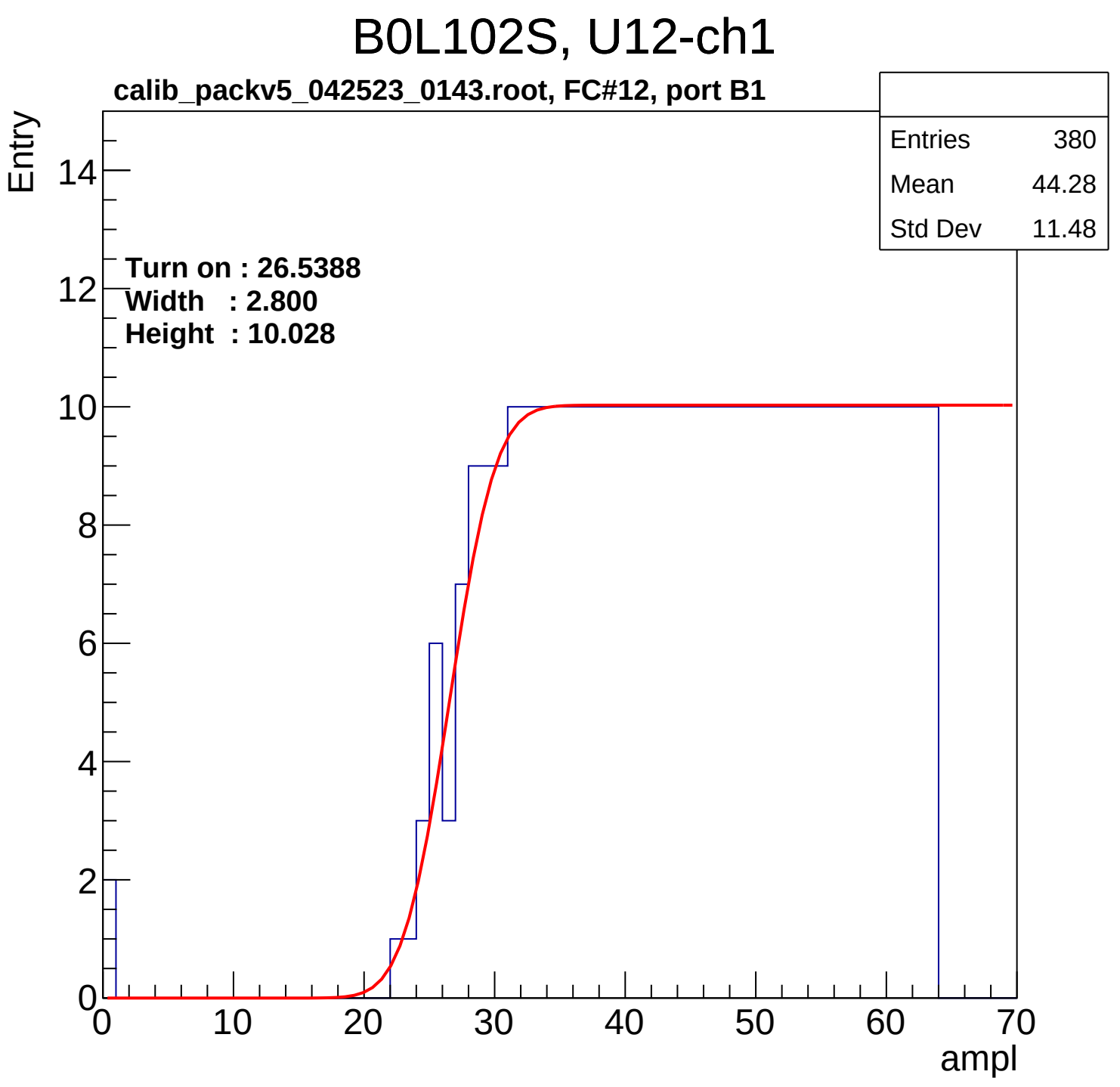
B0L102S, U12-ch1
calib_packv5_042523_0143.root, FC#12, port B1
Entries 380
Mean 44.28
Std Dev 11.48
Turn on : 26.5388
Width : 2.800
Height : 10.028
Entry
ampl
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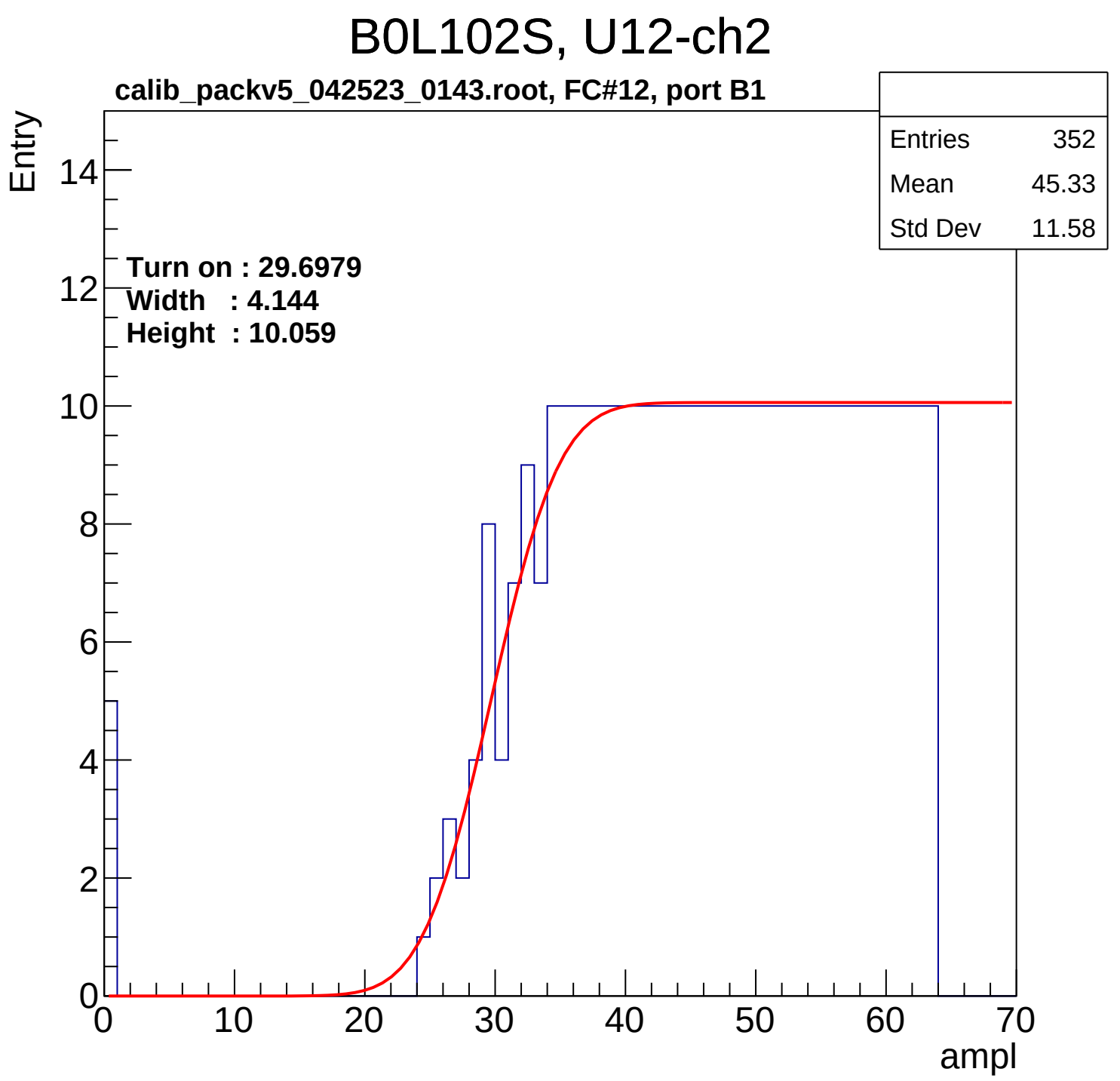
B0L102S, U12-ch2
calib_packv5_042523_0143.root, FC#12, port B1
Entries 352
Mean 45.33
Std Dev 11.58
Turn on : 29.6979
Width : 4.144
Height : 10.059
Entry
ampl
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2
4
6
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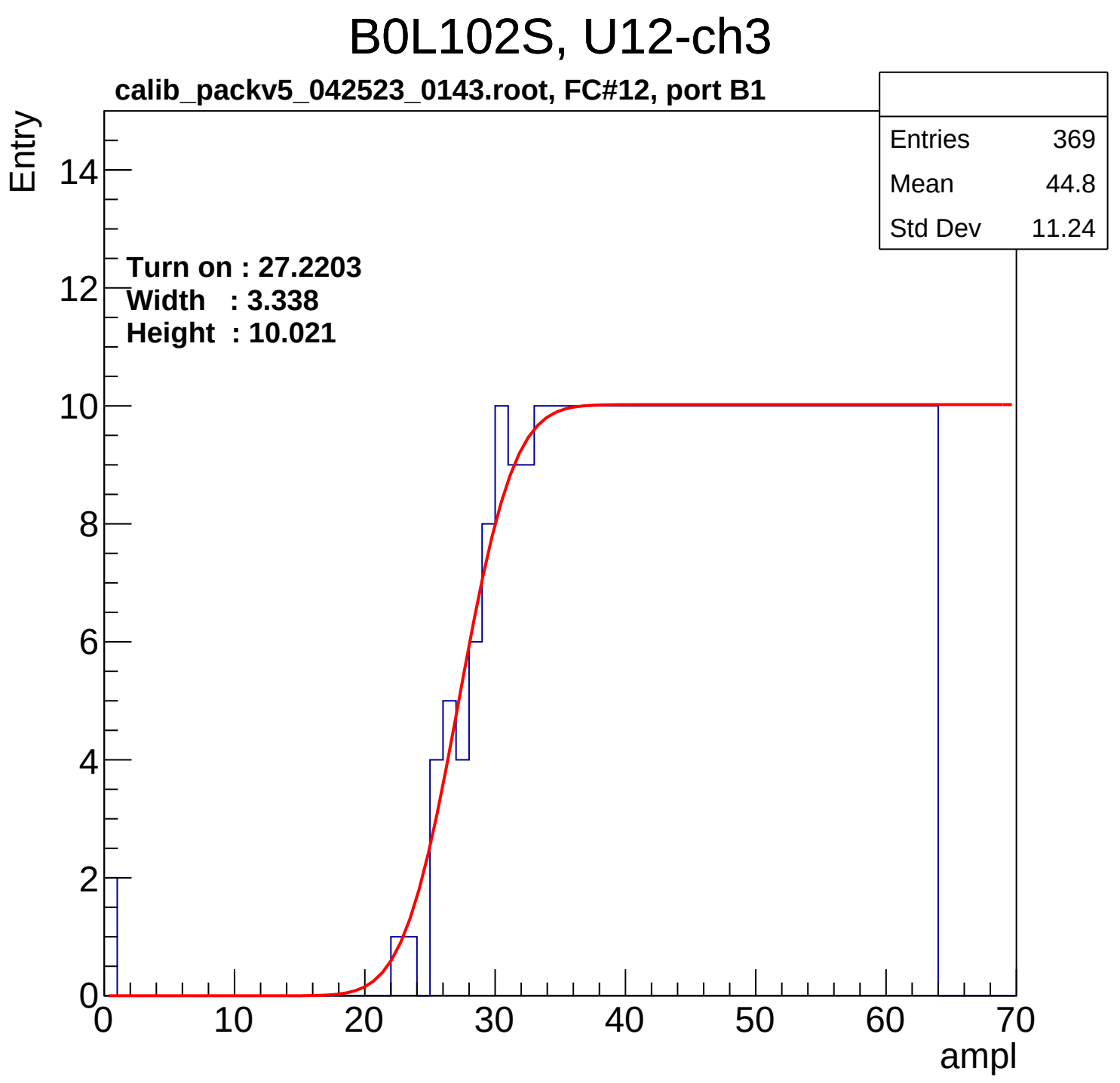
B0L102S, U12-ch3
calib_packv5_042523_0143.root, FC#12, port B1
Entries 369
Mean 44.8
Std Dev 11.24
Turn on : 27.2203
Width : 3.338
Height : 10.021
Entry
ampl
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2
4
6
8
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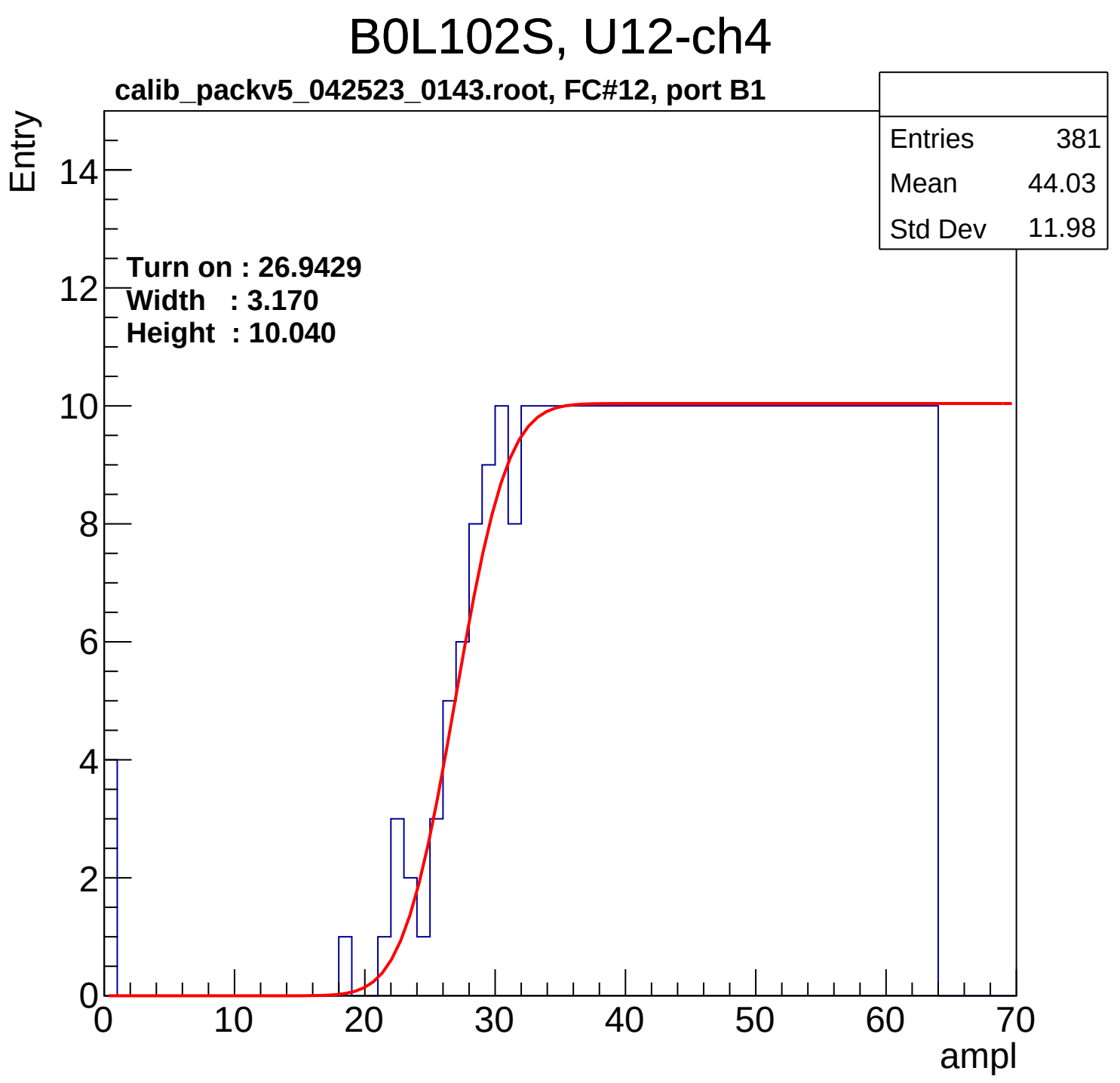
B0L102S, U12-ch4
calib_packv5_042523_0143.root, FC#12, port B1
Entries 381
Mean 44.03
Std Dev 11.98
Turn on : 26.9429
Width : 3.170
Height : 10.040
Entry
ampl
0
2
4
6
8
10
12
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0
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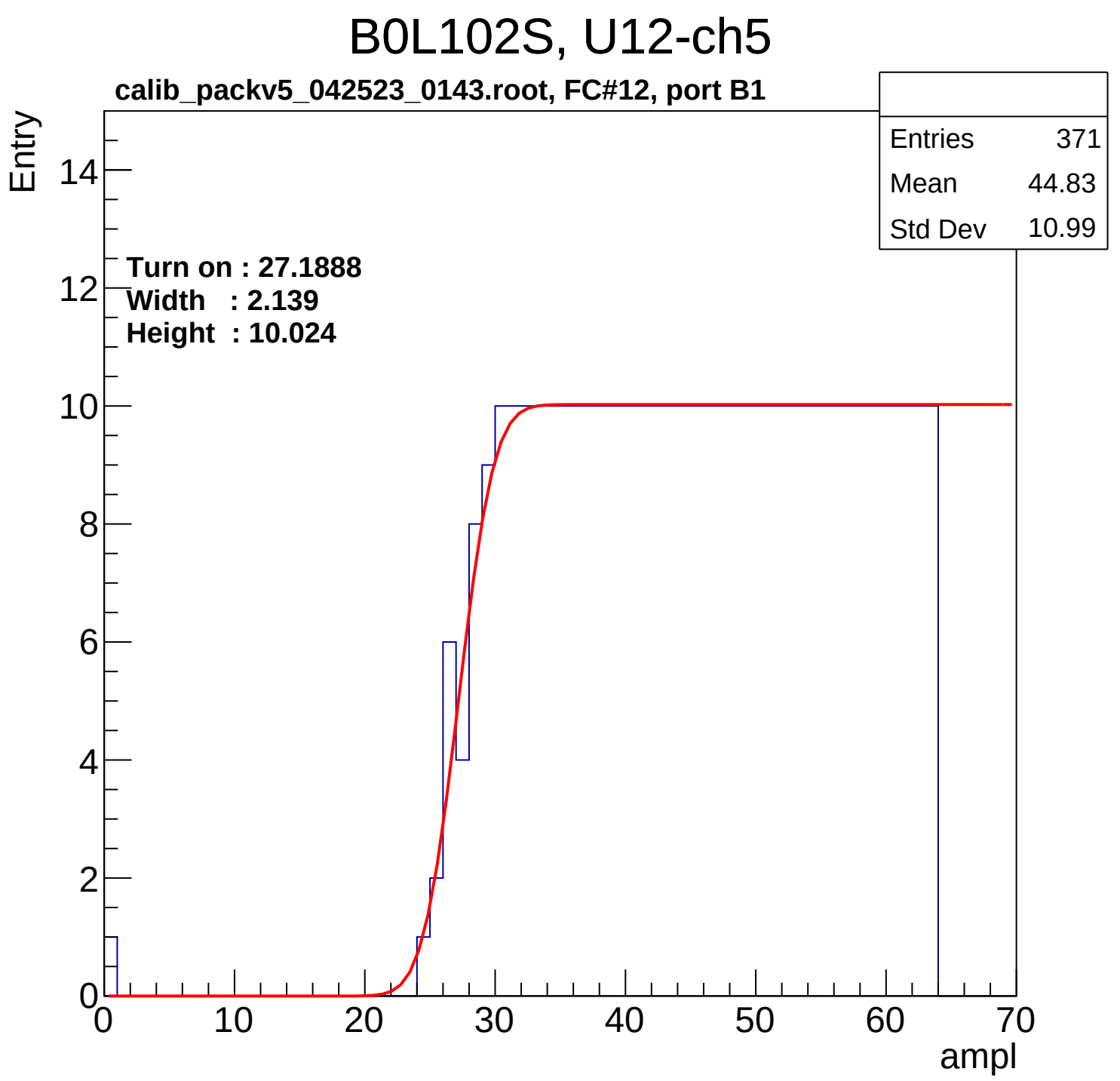
B0L102S, U12-ch5
calib_packv5_042523_0143.root, FC#12, port B1
Entries 371
Mean 44.83
Std Dev 10.99
Turn on : 27.1888
Width : 2.139
Height : 10.024
Entry
ampl
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2
4
6
8
10
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0
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60
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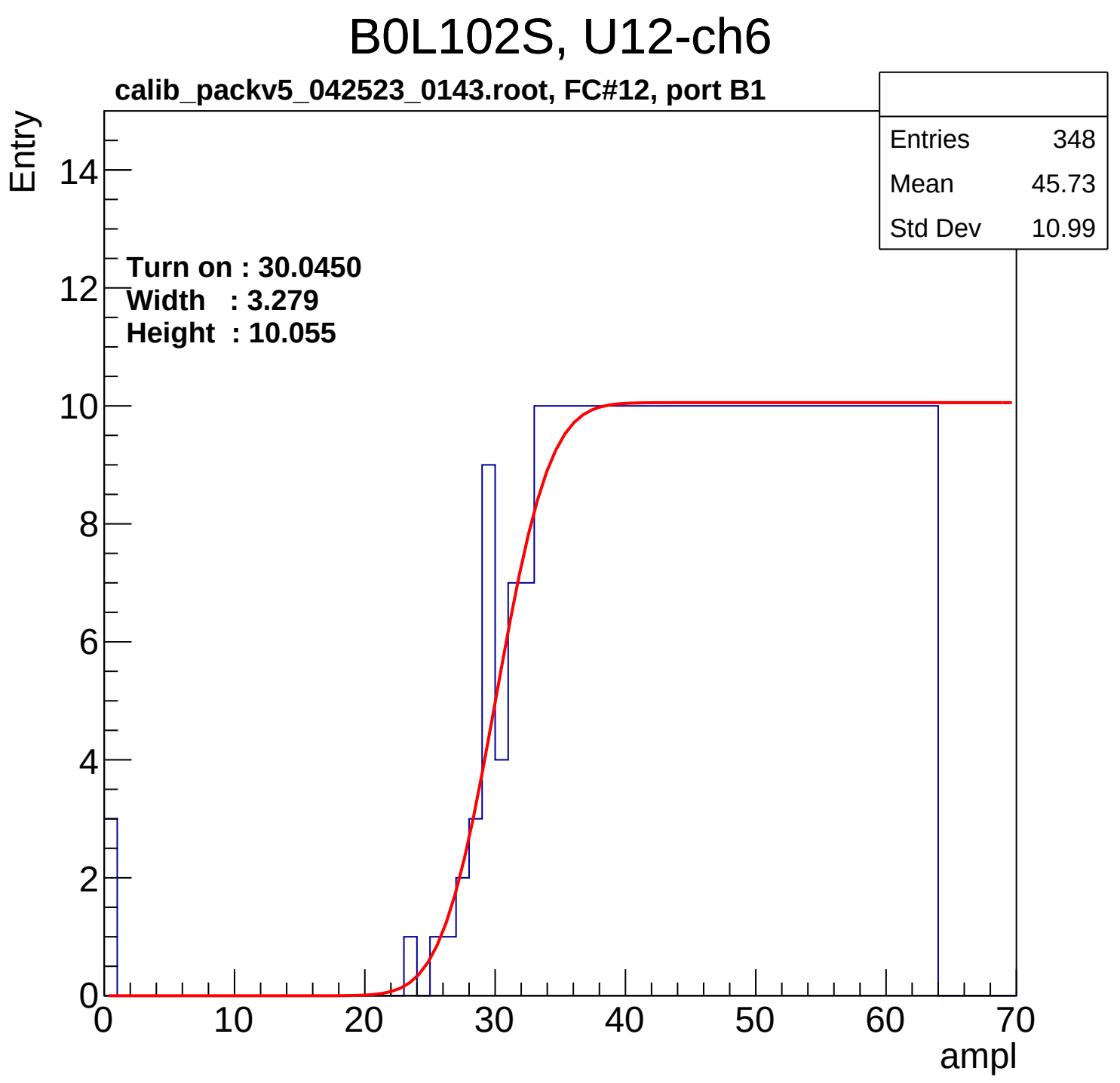
B0L102S, U12-ch6
calib_packv5_042523_0143.root, FC#12, port B1
Entries 348
Mean 45.73
Std Dev 10.99
Turn on : 30.0450
Width : 3.279
Height : 10.055
Entry
ampl
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2
4
6
8
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0
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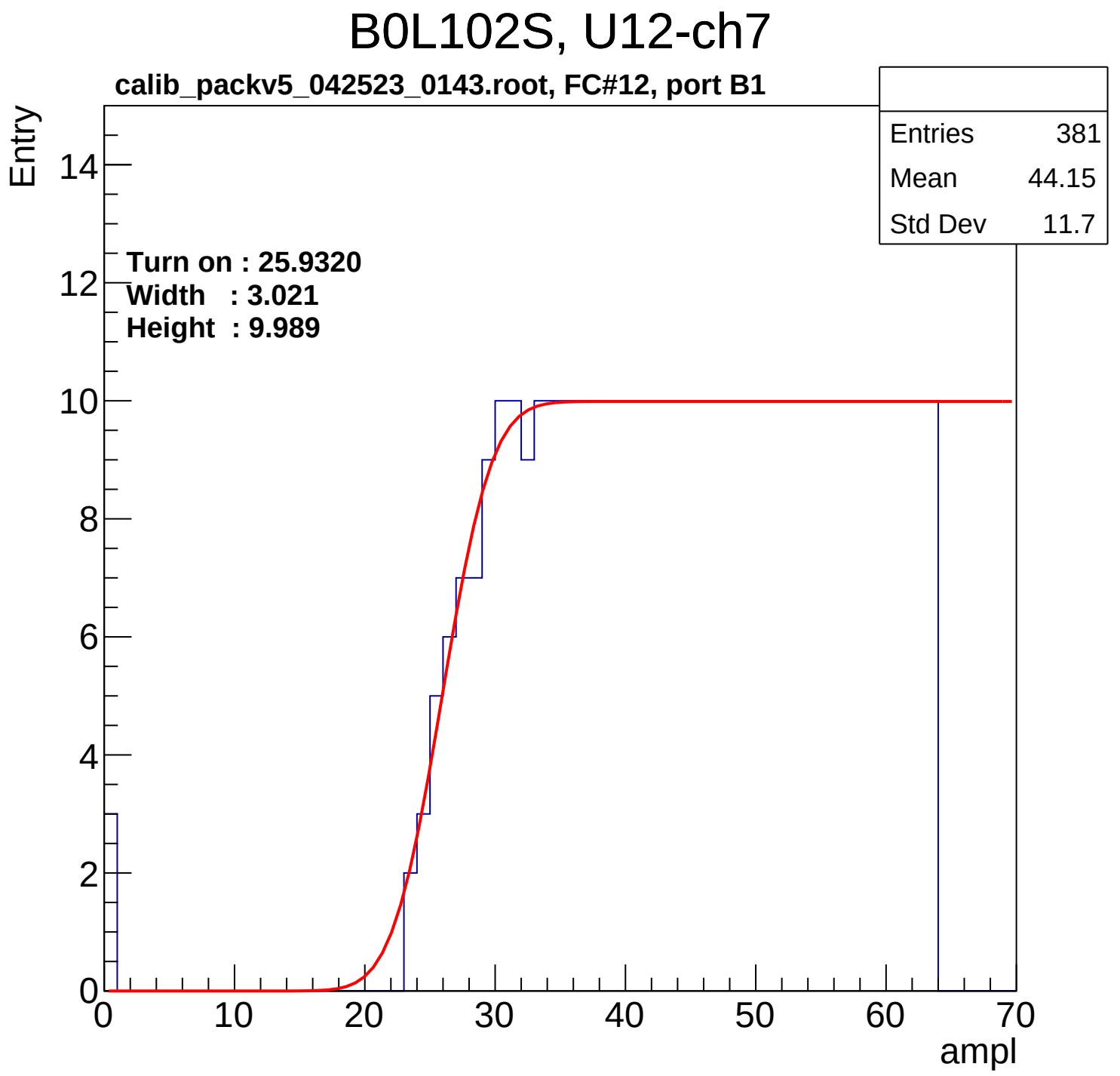
B0L102S, U12-ch7
calib_packv5_042523_0143.root, FC#12, port B1
Entries 381
Mean 44.15
Std Dev 11.7
Turn on : 25.9320
Width : 3.021
Height : 9.989
Entry
ampl
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2
4
6
8
10
12
14
0
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20
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60
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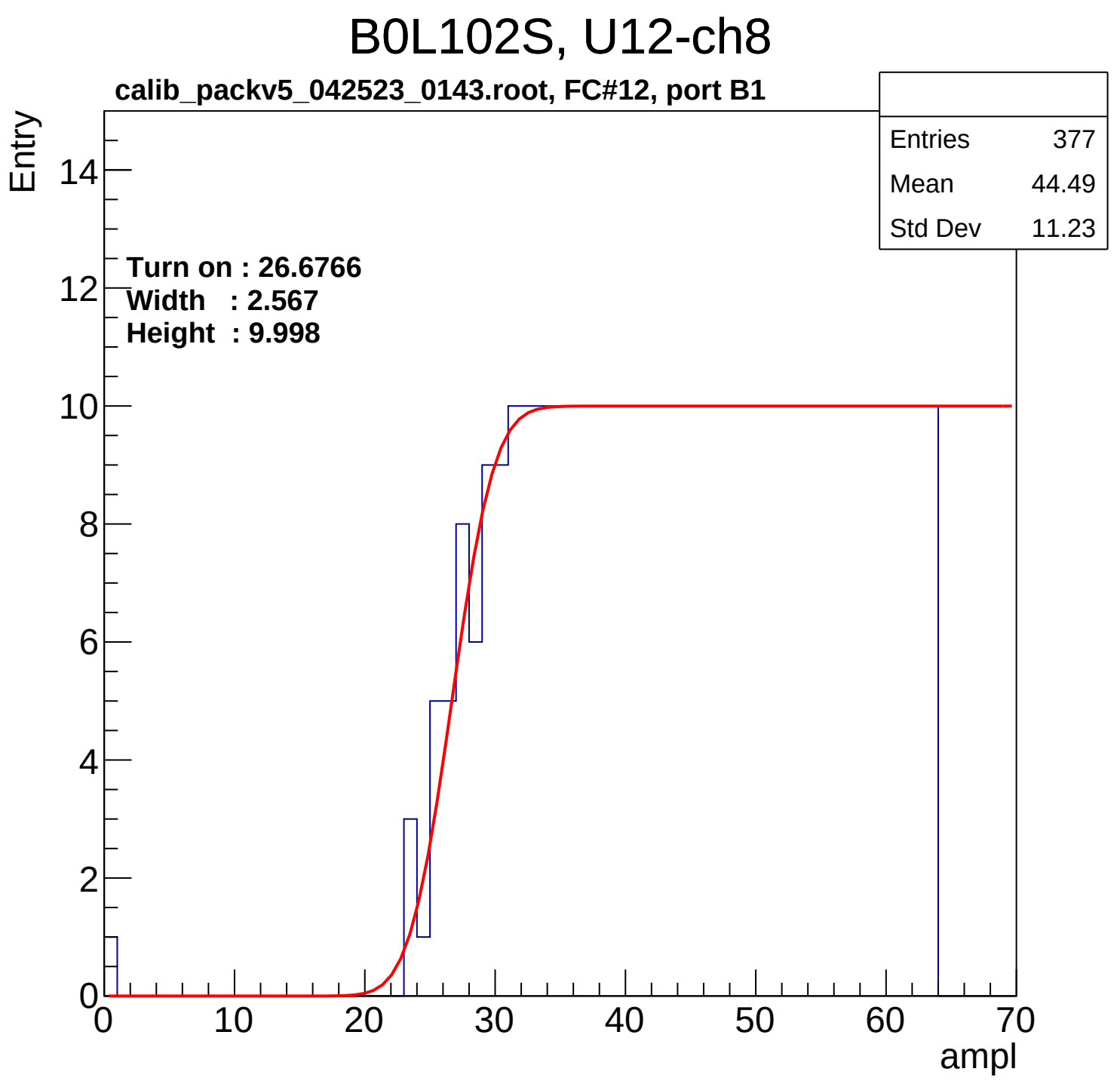
B0L102S, U12-ch8
calib_packv5_042523_0143.root, FC#12, port B1
Entries 377
Mean 44.49
Std Dev 11.23
Turn on : 26.6766
Width : 2.567
Height : 9.998
Entry
ampl
0
2
4
6
8
10
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0
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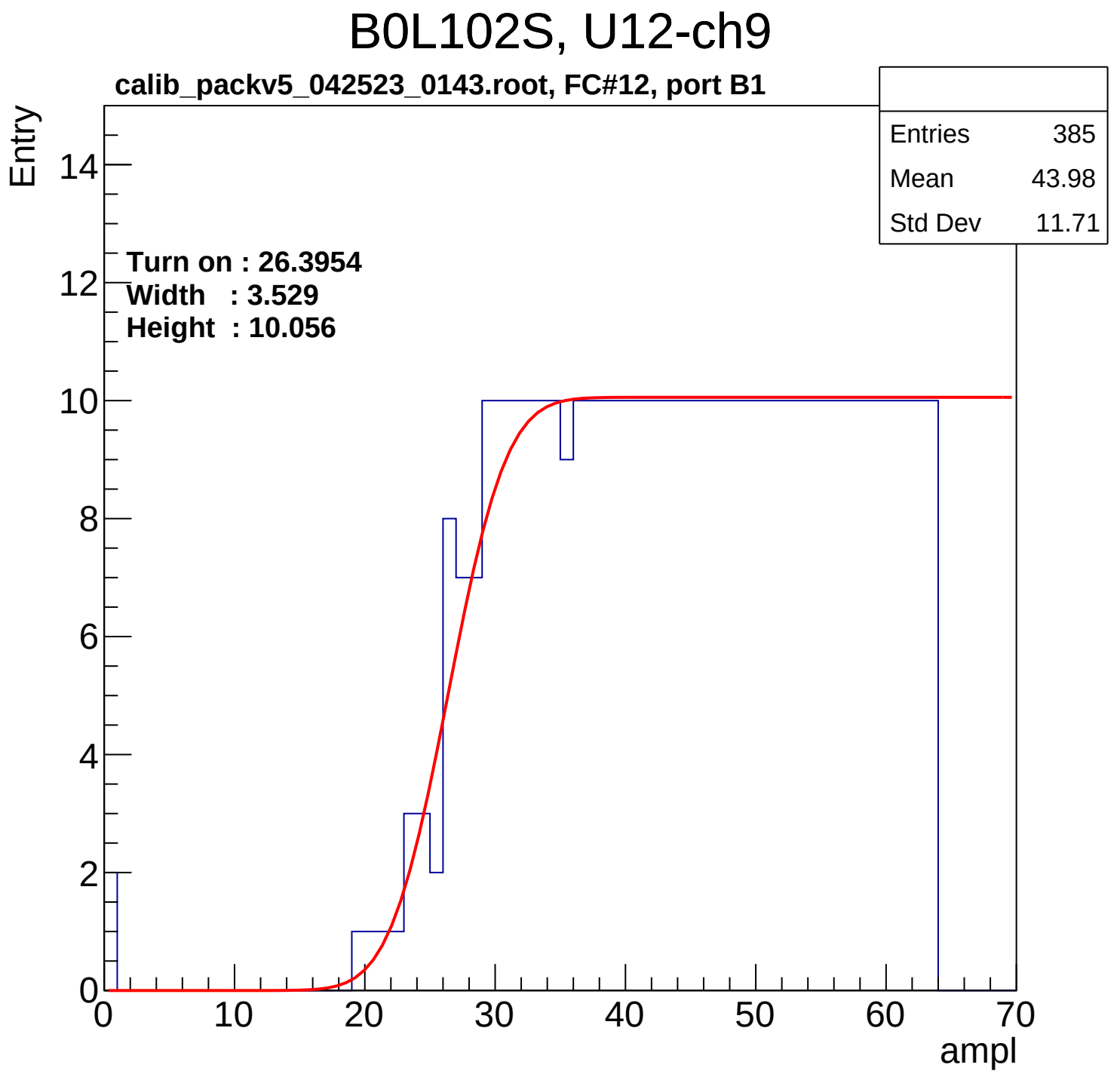
B0L102S, U12-ch9
calib_packv5_042523_0143.root, FC#12, port B1
Entries 385
Mean 43.98
Std Dev 11.71
Turn on : 26.3954
Width : 3.529
Height : 10.056
Entry
ampl
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2
4
6
8
10
12
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0
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60
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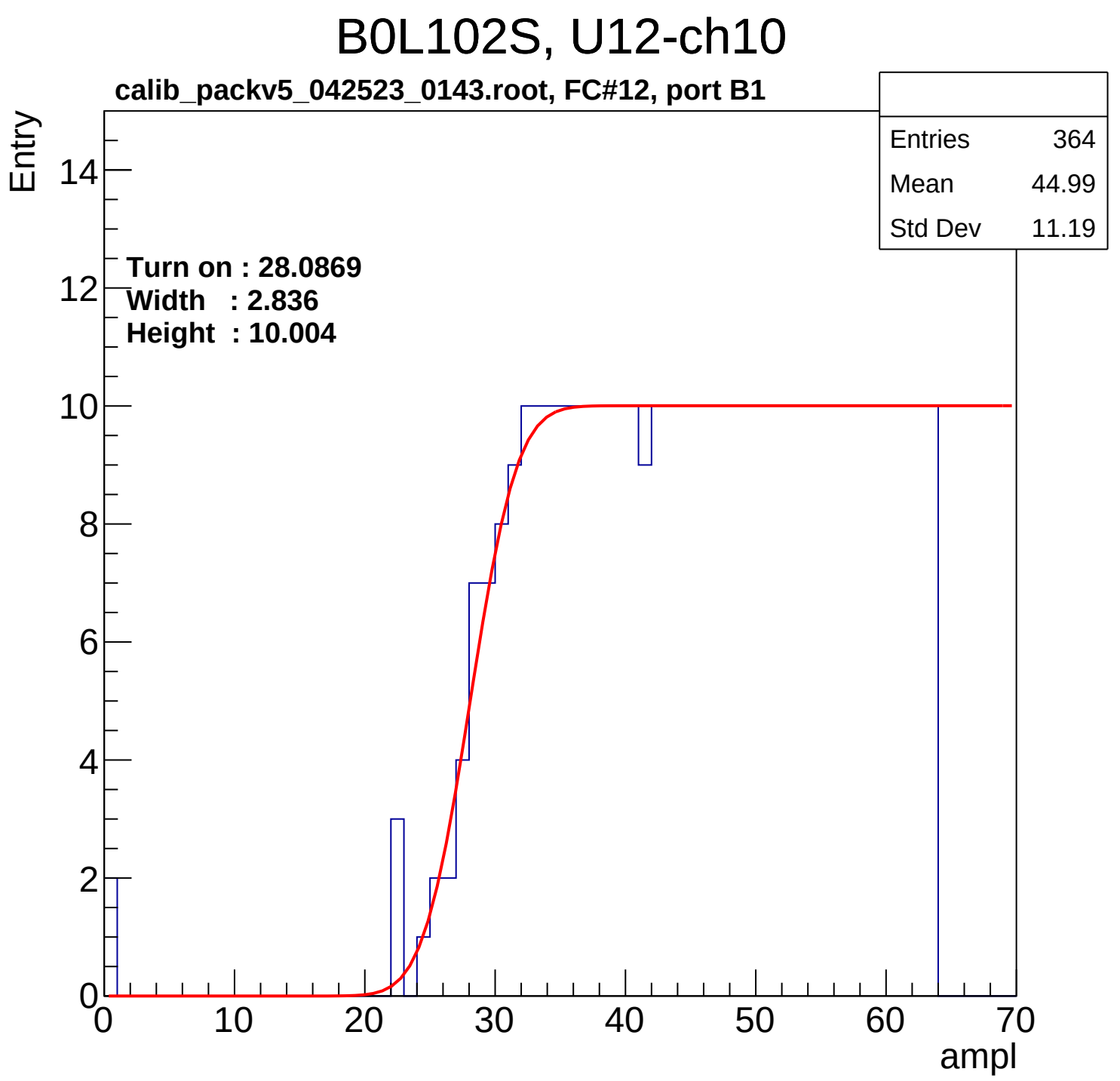
B0L102S, U12-ch10
calib_packv5_042523_0143.root, FC#12, port B1
Entries 364
Mean 44.99
Std Dev 11.19
Turn on : 28.0869
Width : 2.836
Height : 10.004
Entry
ampl
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2
4
6
8
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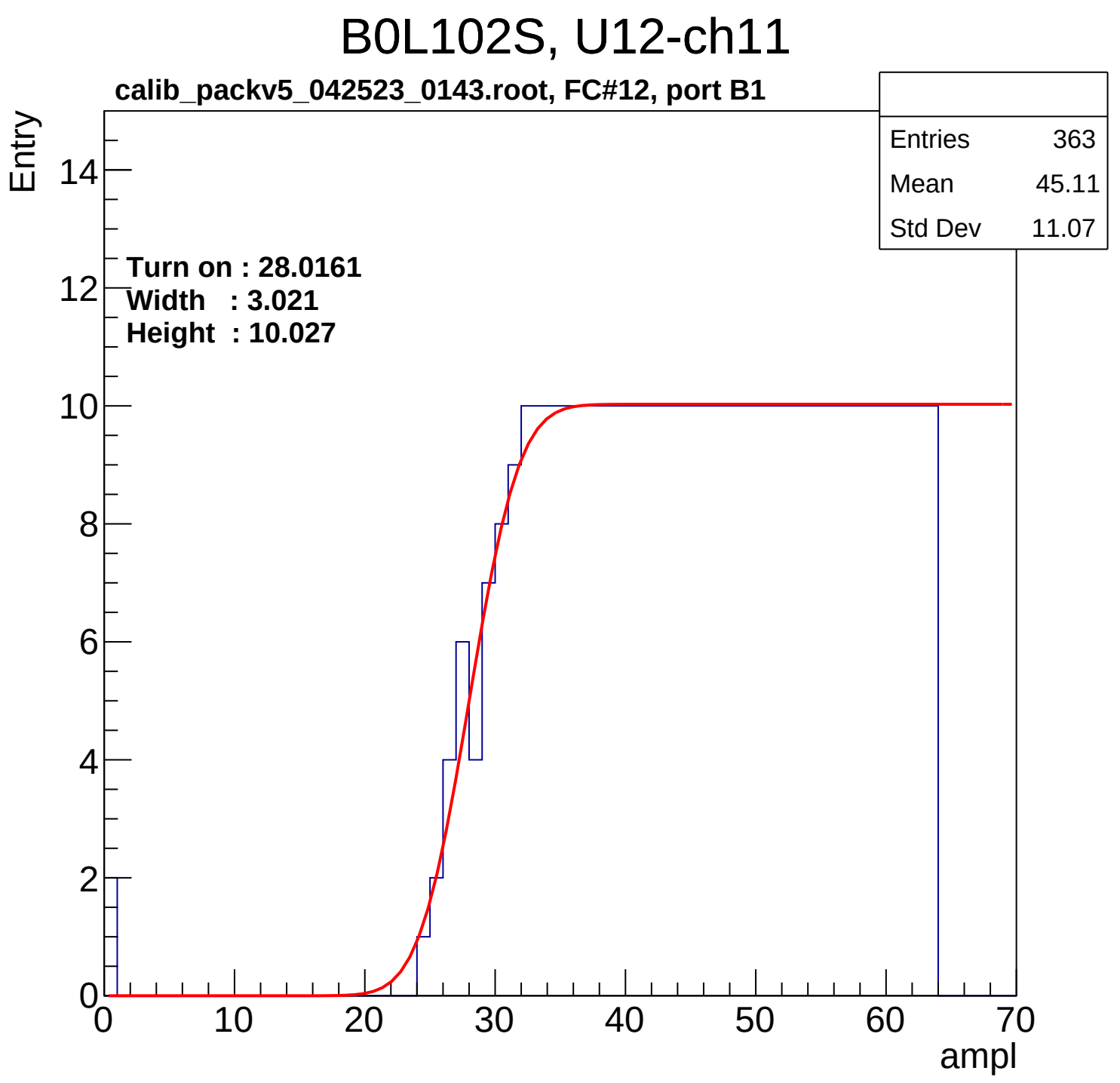
B0L102S, U12-ch11
calib_packv5_042523_0143.root, FC#12, port B1
Entries 363
Mean 45.11
Std Dev 11.07
Turn on : 28.0161
Width : 3.021
Height : 10.027
Entry
ampl
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2
4
6
8
10
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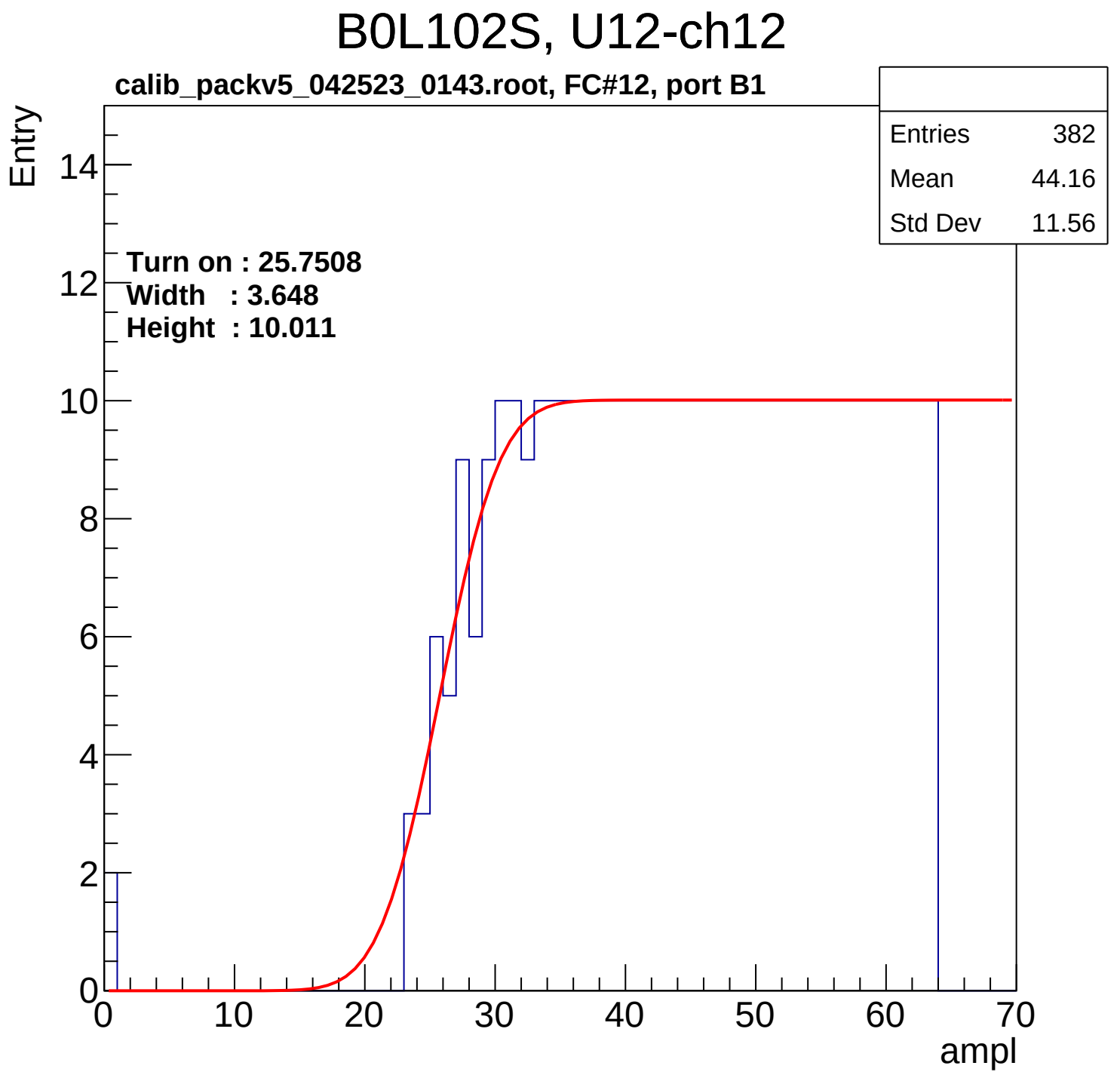
B0L102S, U12-ch12
calib_packv5_042523_0143.root, FC#12, port B1
Entries 382
Mean 44.16
Std Dev 11.56
Turn on : 25.7508
Width : 3.648
Height : 10.011
Entry
ampl
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4
6
8
10
12
14
0
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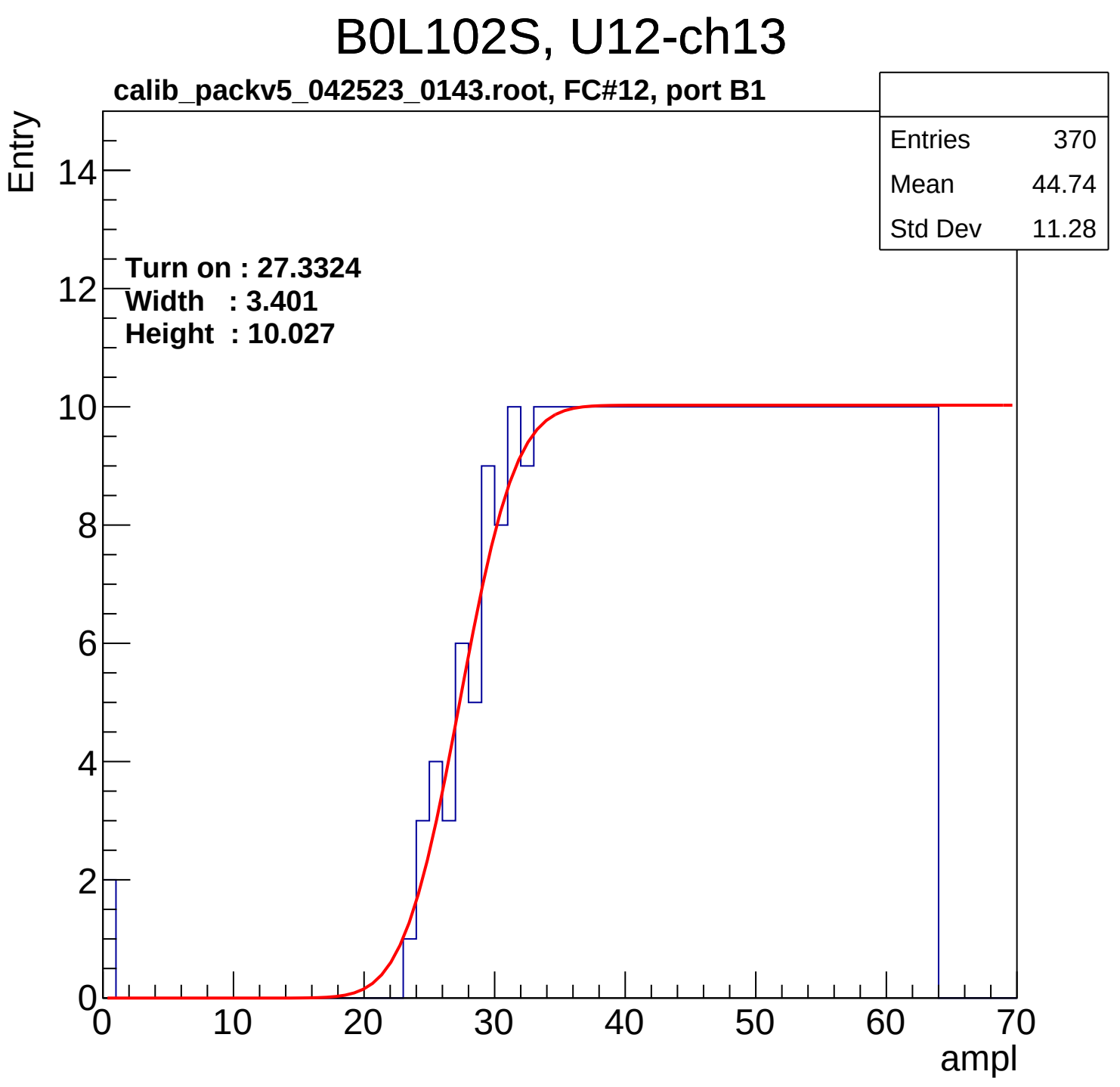
B0L102S, U12-ch13
calib_packv5_042523_0143.root, FC#12, port B1
Entries 370
Mean 44.74
Std Dev 11.28
Turn on : 27.3324
Width : 3.401
Height : 10.027
Entry
ampl
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4
6
8
10
12
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0
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60
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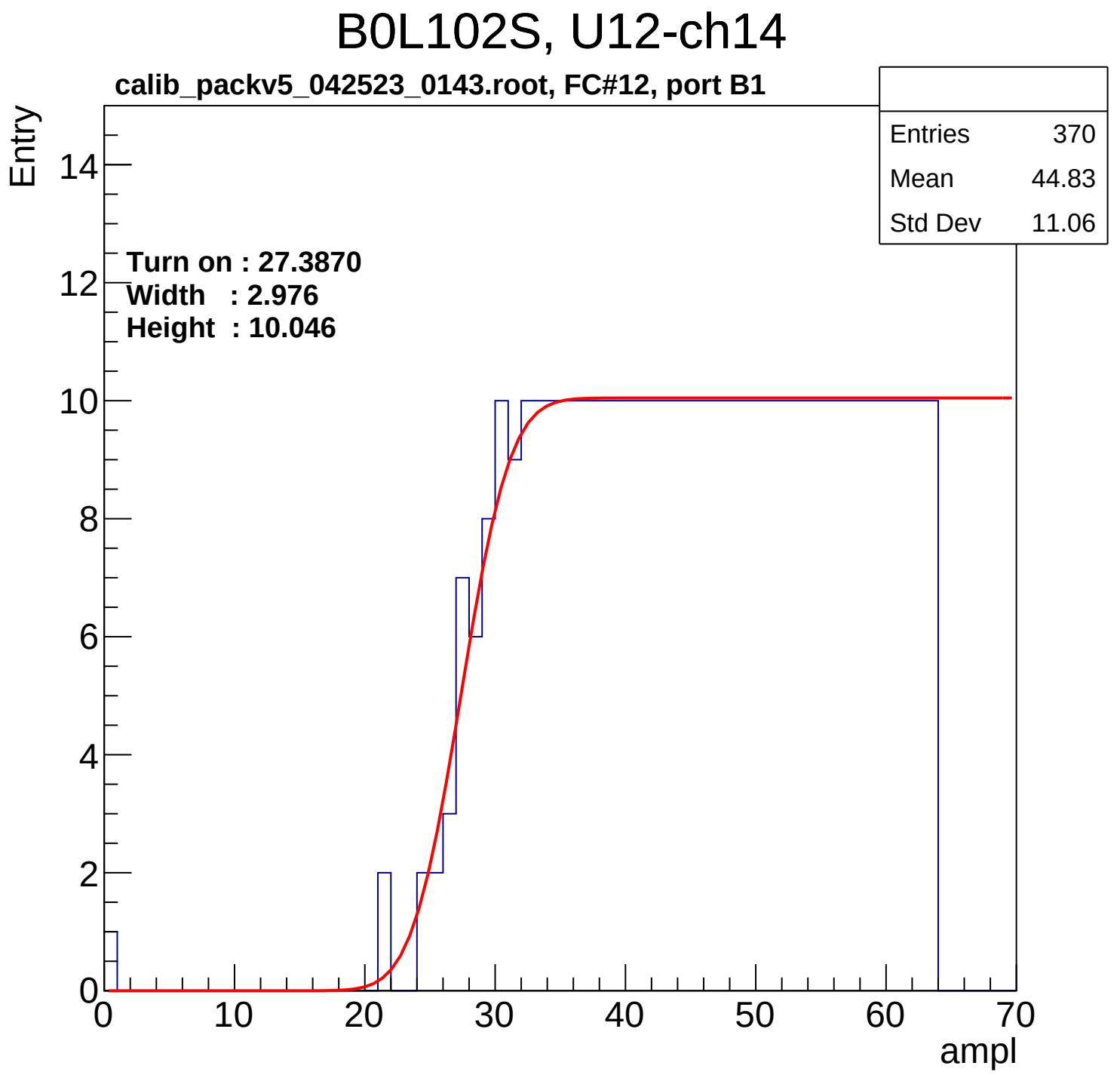
B0L102S, U12-ch14
calib_packv5_042523_0143.root, FC#12, port B1
Entries 370
Mean 44.83
Std Dev 11.06
Turn on : 27.3870
Width : 2.976
Height : 10.046
Entry
ampl
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6
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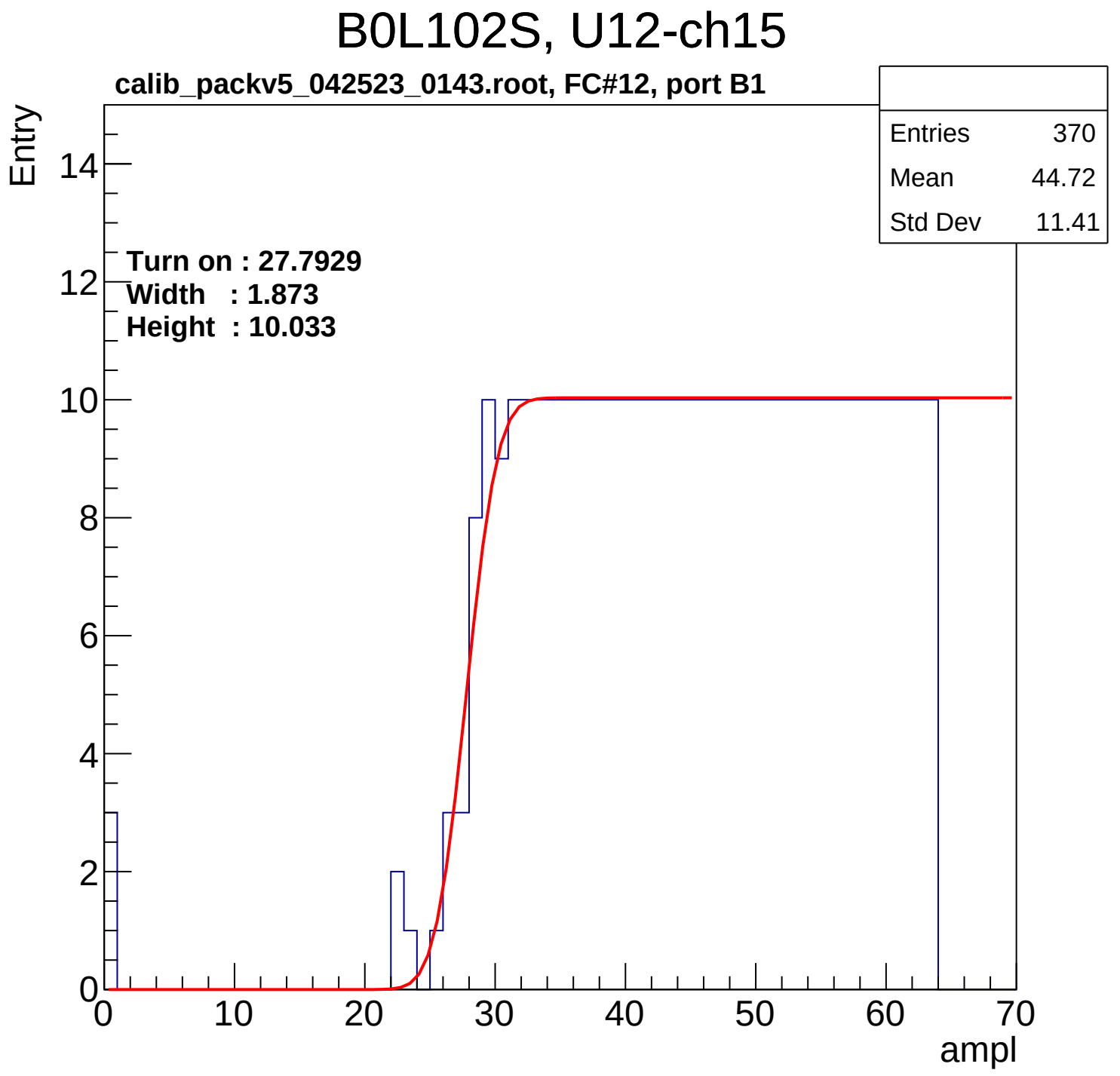
B0L102S, U12-ch15
calib_packv5_042523_0143.root, FC#12, port B1
Entries 370
Mean 44.72
Std Dev 11.41
Turn on : 27.7929
Width : 1.873
Height : 10.033
Entry
ampl
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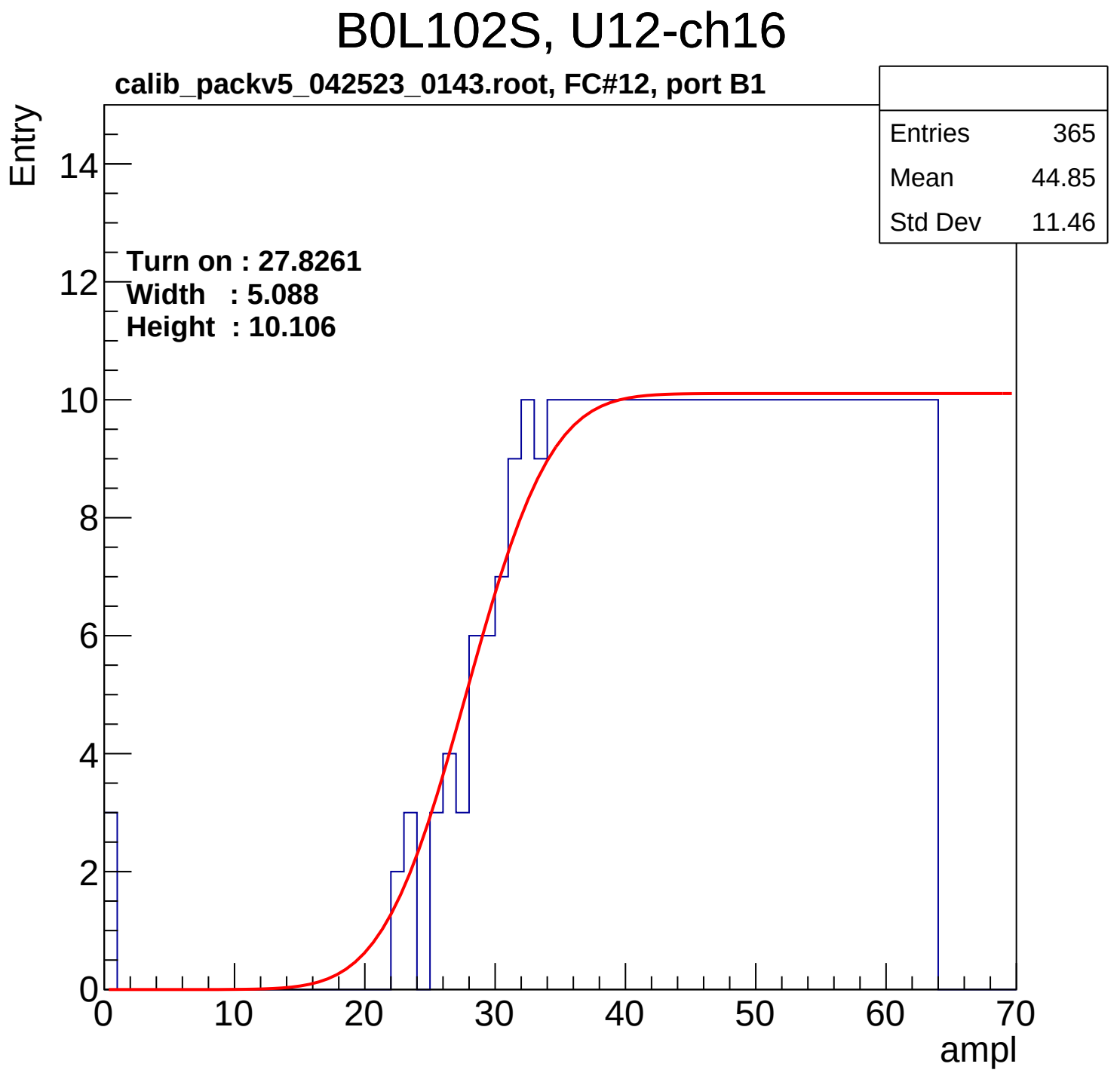
B0L102S, U12-ch16
calib_packv5_042523_0143.root, FC#12, port B1
Entries 365
Mean 44.85
Std Dev 11.46
Turn on : 27.8261
Width : 5.088
Height : 10.106
Entry
ampl
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8
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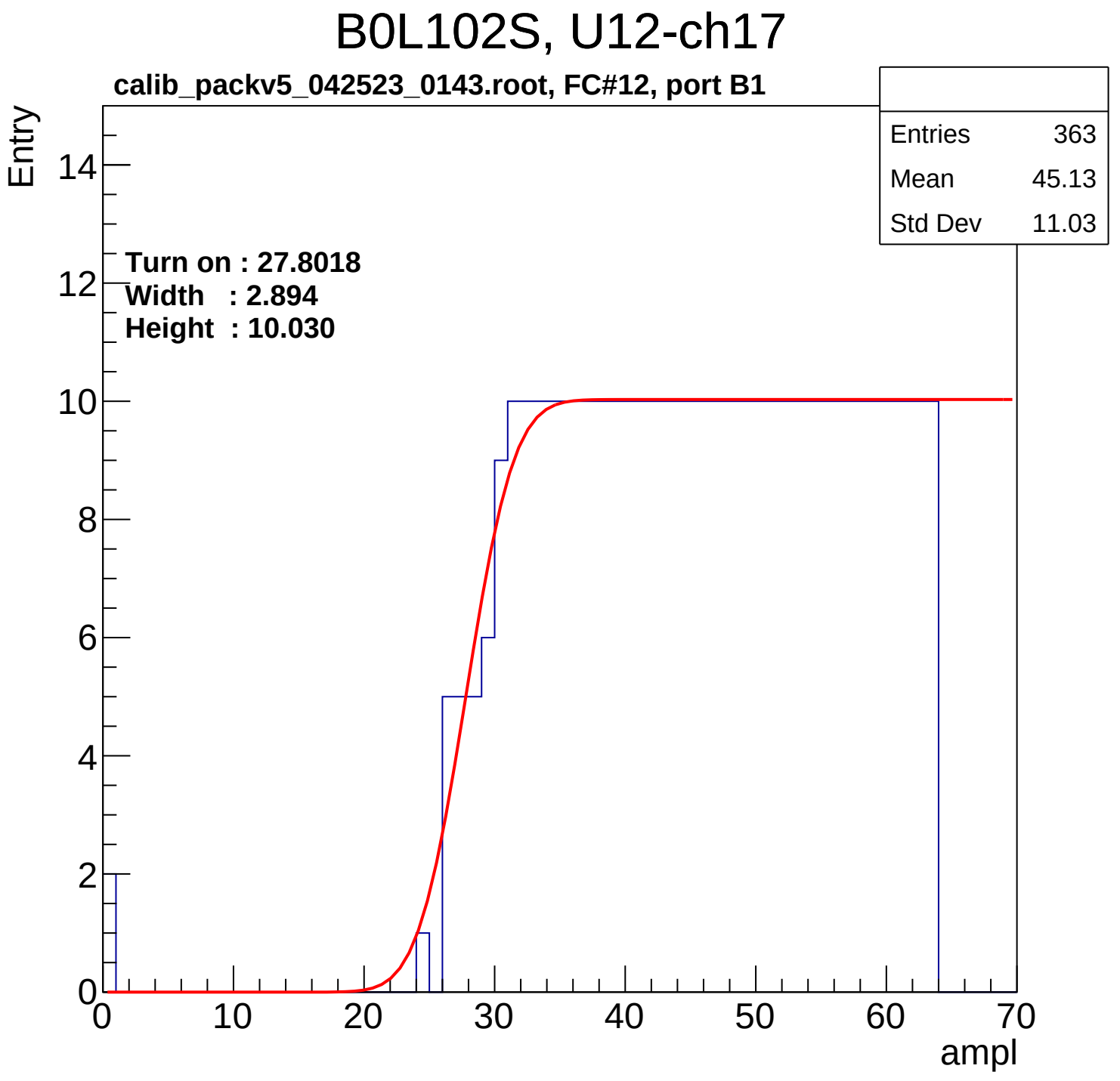
B0L102S, U12-ch17
calib_packv5_042523_0143.root, FC#12, port B1
Entries 363
Mean 45.13
Std Dev 11.03
Turn on : 27.8018
Width : 2.894
Height : 10.030
Entry
ampl
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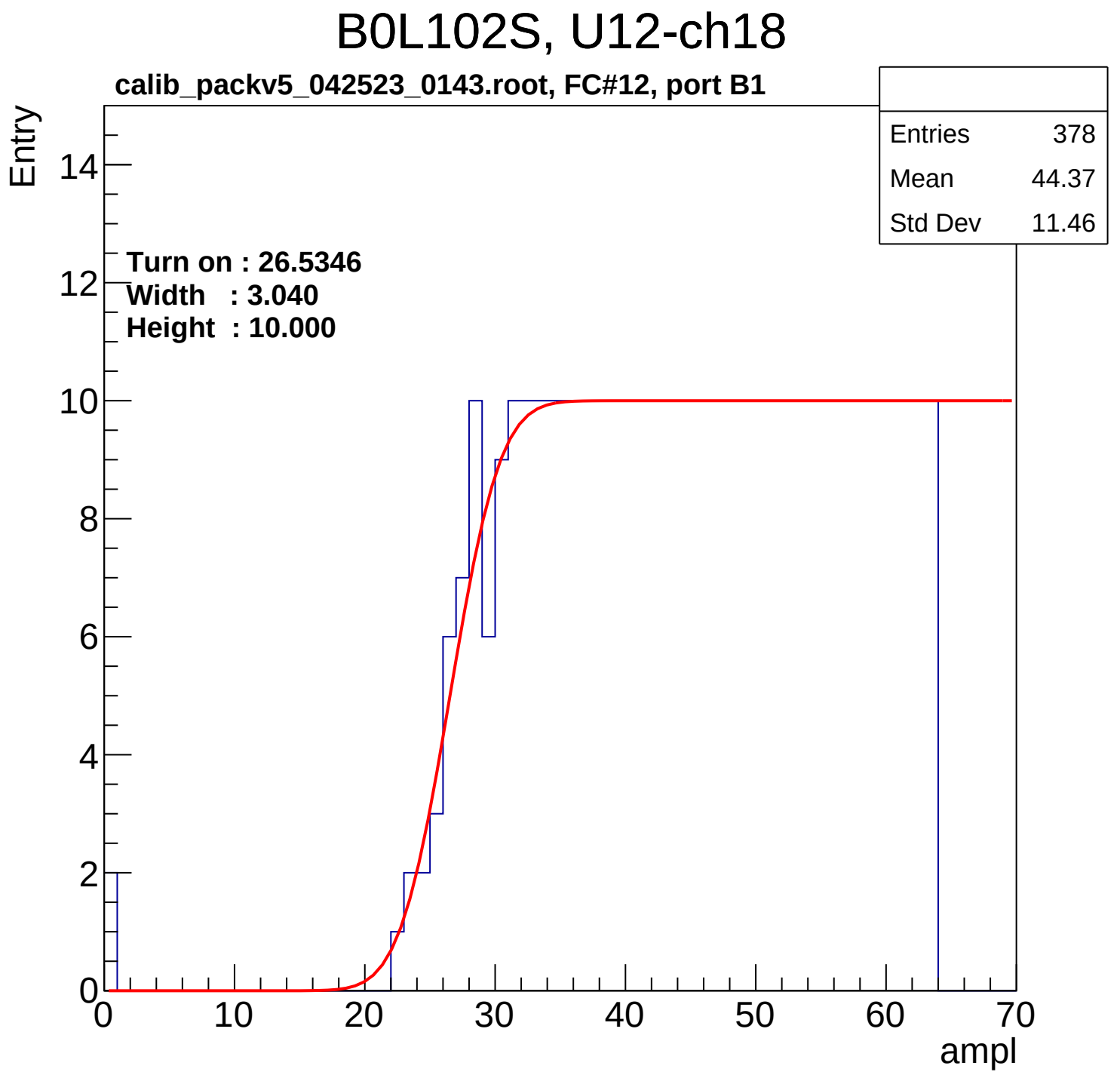
B0L102S, U12-ch18
calib_packv5_042523_0143.root, FC#12, port B1
Entries 378
Mean 44.37
Std Dev 11.46
Turn on : 26.5346
Width : 3.040
Height : 10.000
Entry
ampl
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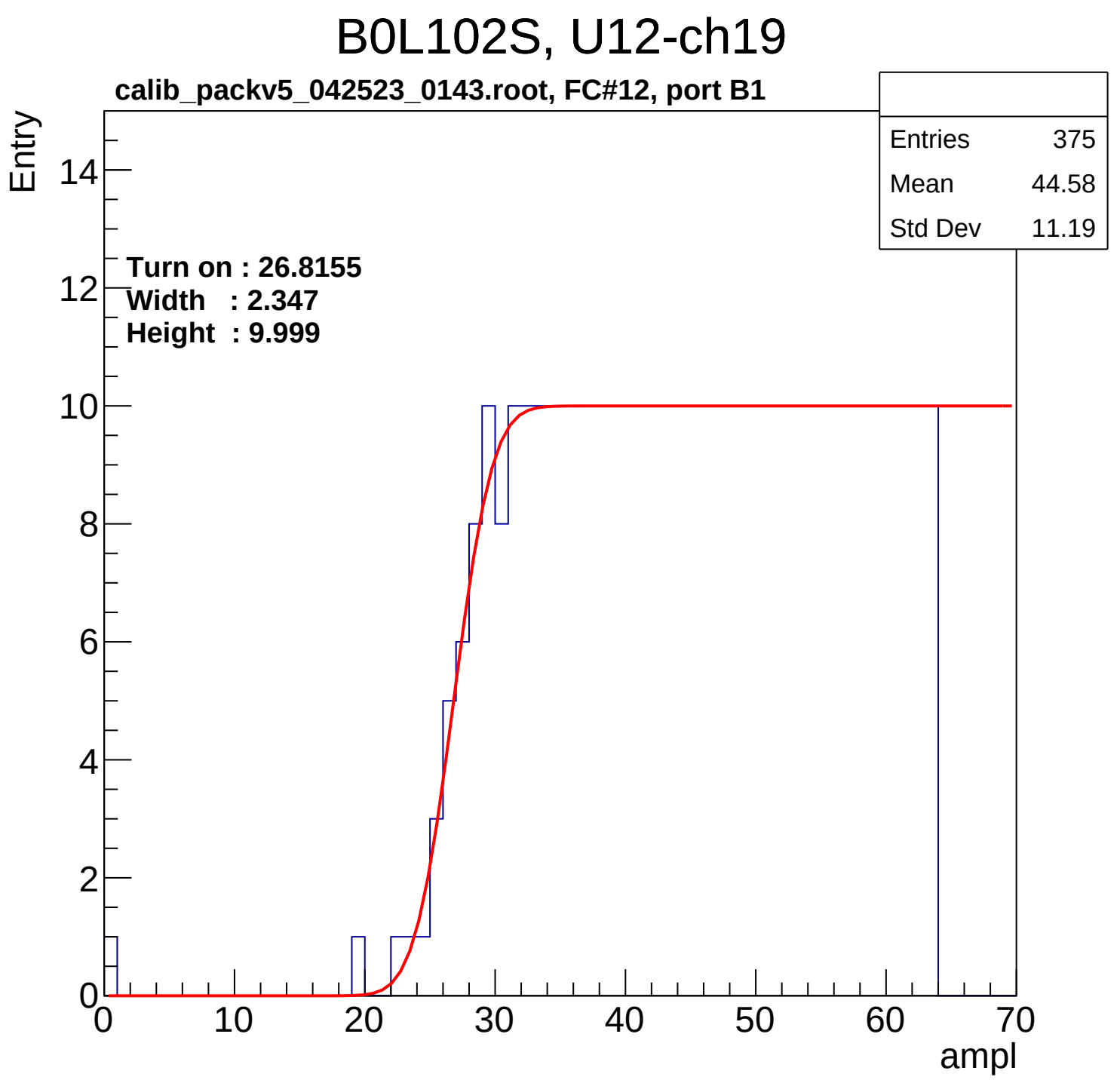
B0L102S, U12-ch19
calib_packv5_042523_0143.root, FC#12, port B1
Entries 375
Mean 44.58
Std Dev 11.19
Turn on : 26.8155
Width : 2.347
Height : 9.999
Entry
ampl
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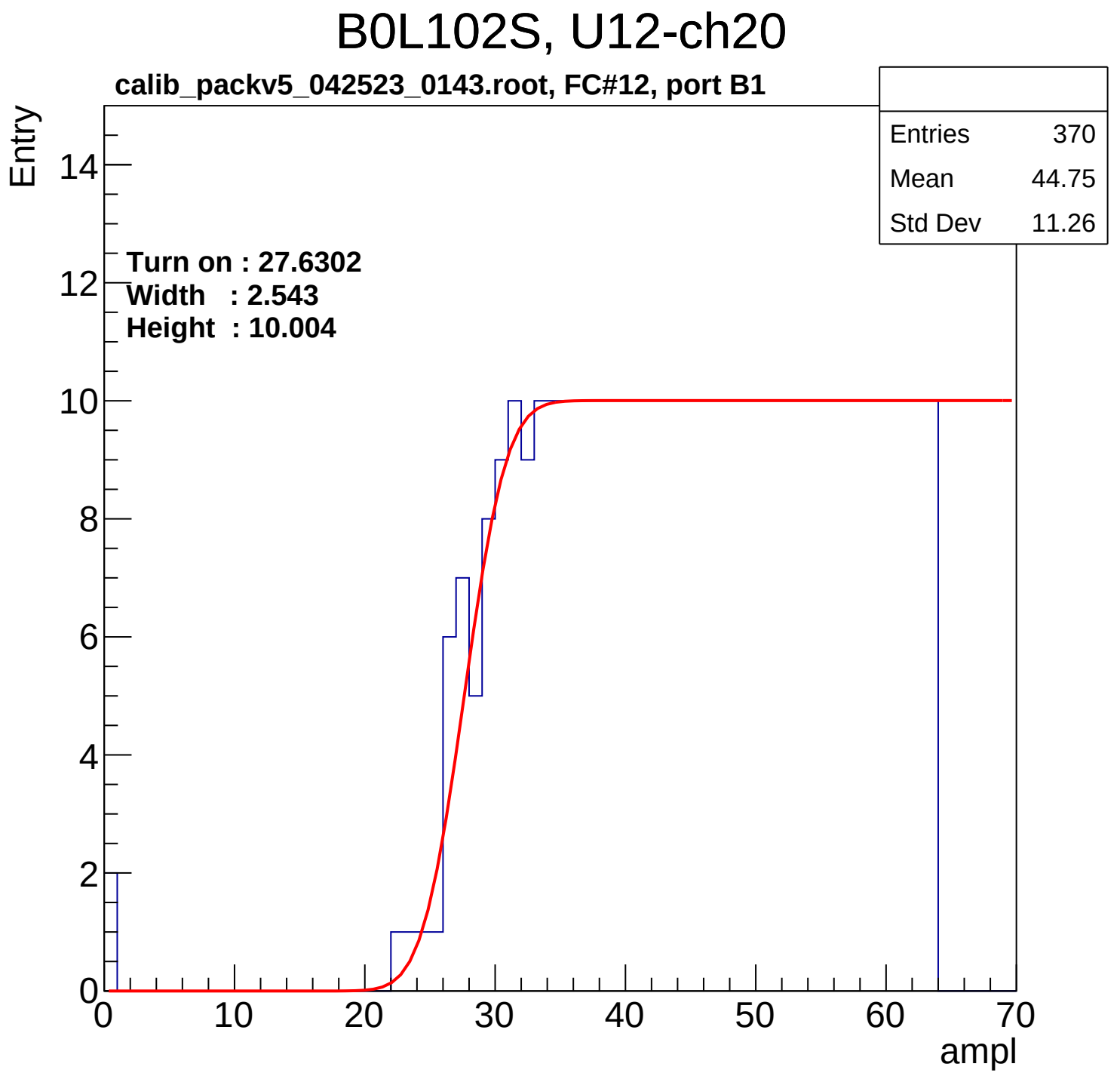
B0L102S, U12-ch20
calib_packv5_042523_0143.root, FC#12, port B1
Entries 370
Mean 44.75
Std Dev 11.26
Turn on : 27.6302
Width : 2.543
Height : 10.004
Entry
ampl
0
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8
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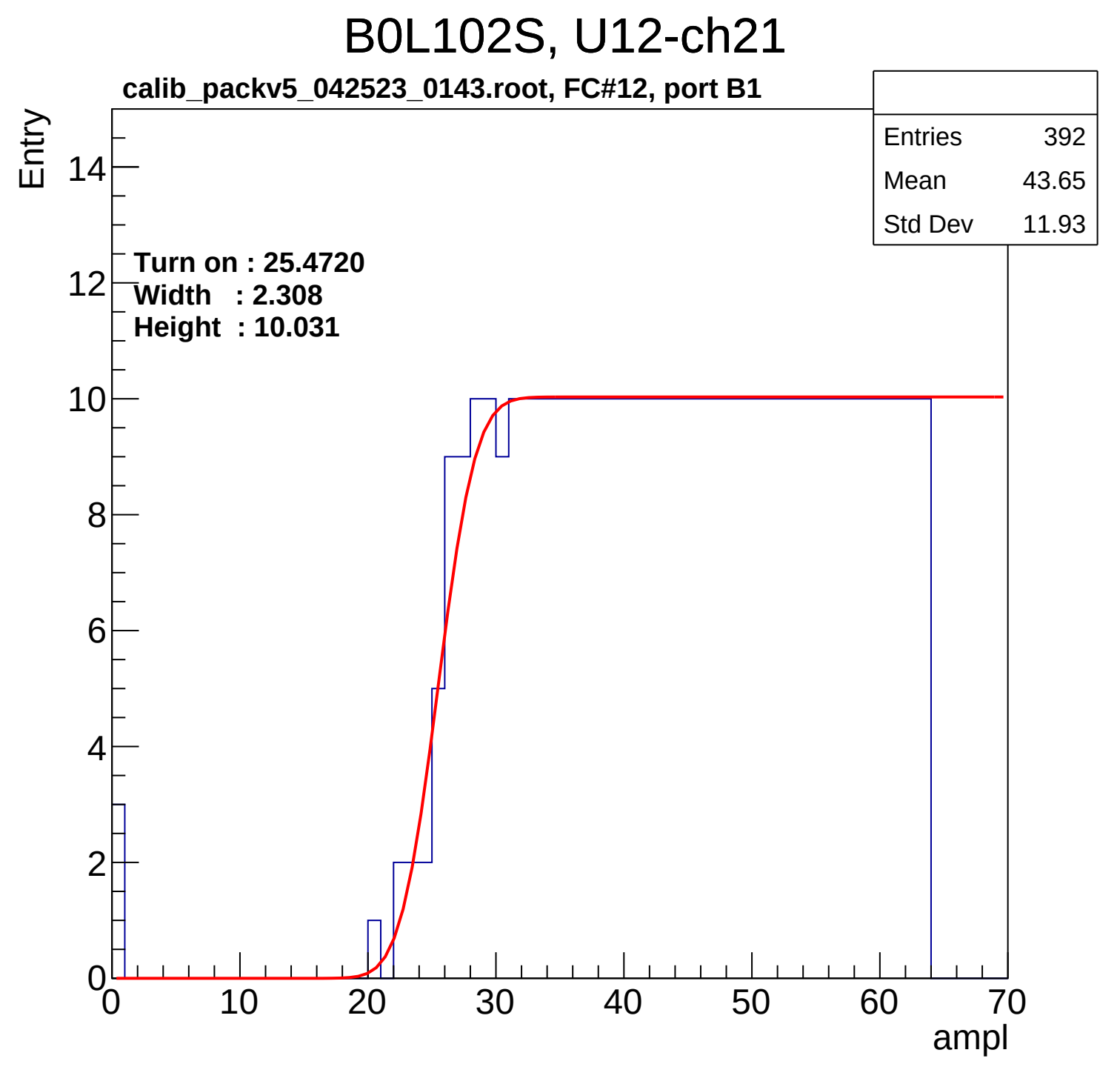
B0L102S, U12-ch21
calib_packv5_042523_0143.root, FC#12, port B1
Entries 392
Mean 43.65
Std Dev 11.93
Turn on : 25.4720
Width : 2.308
Height : 10.031
Entry
ampl
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2
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0
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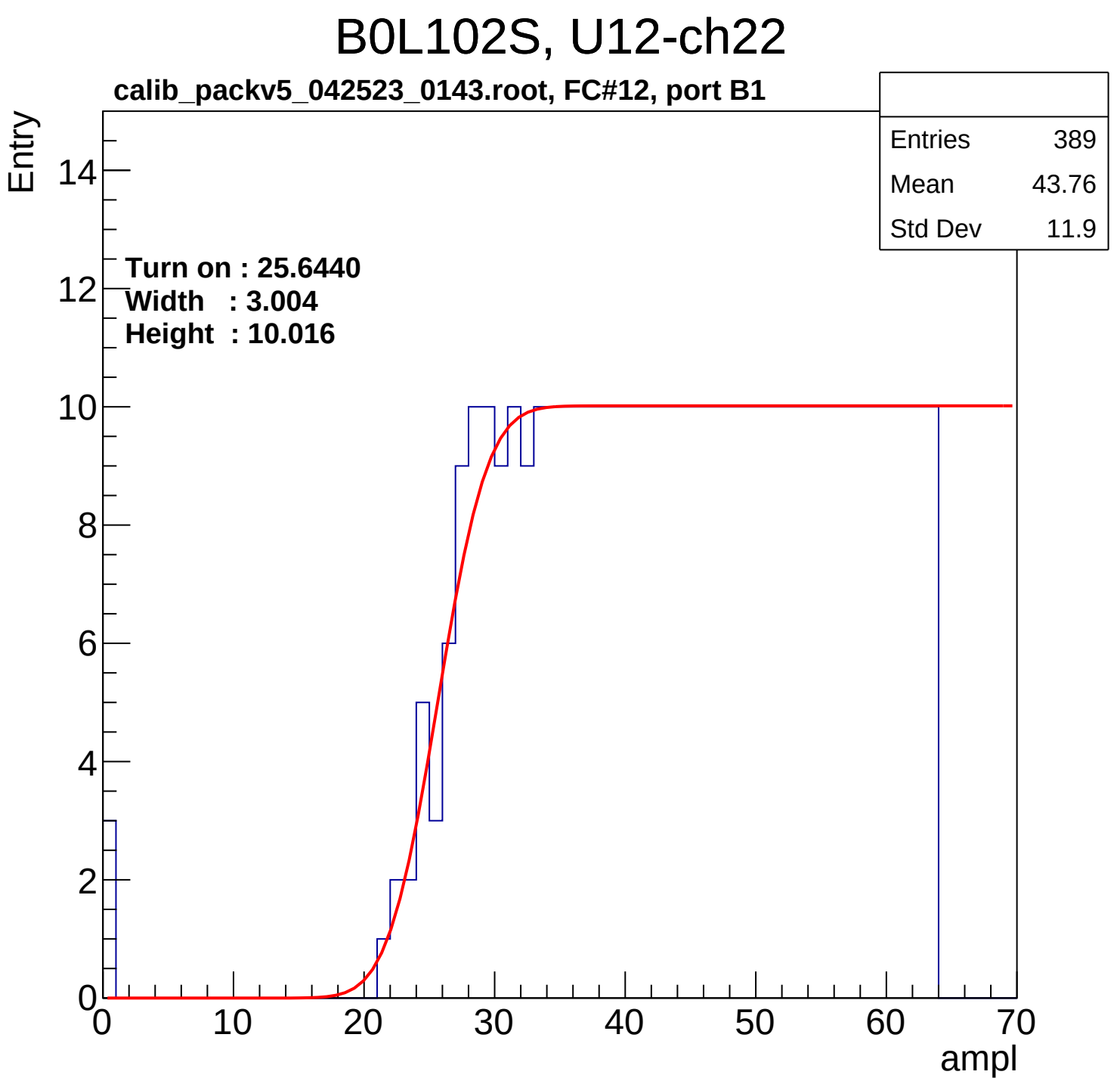
B0L102S, U12-ch22
calib_packv5_042523_0143.root, FC#12, port B1
Entries 389
Mean 43.76
Std Dev 11.9
Turn on : 25.6440
Width : 3.004
Height : 10.016
Entry
ampl
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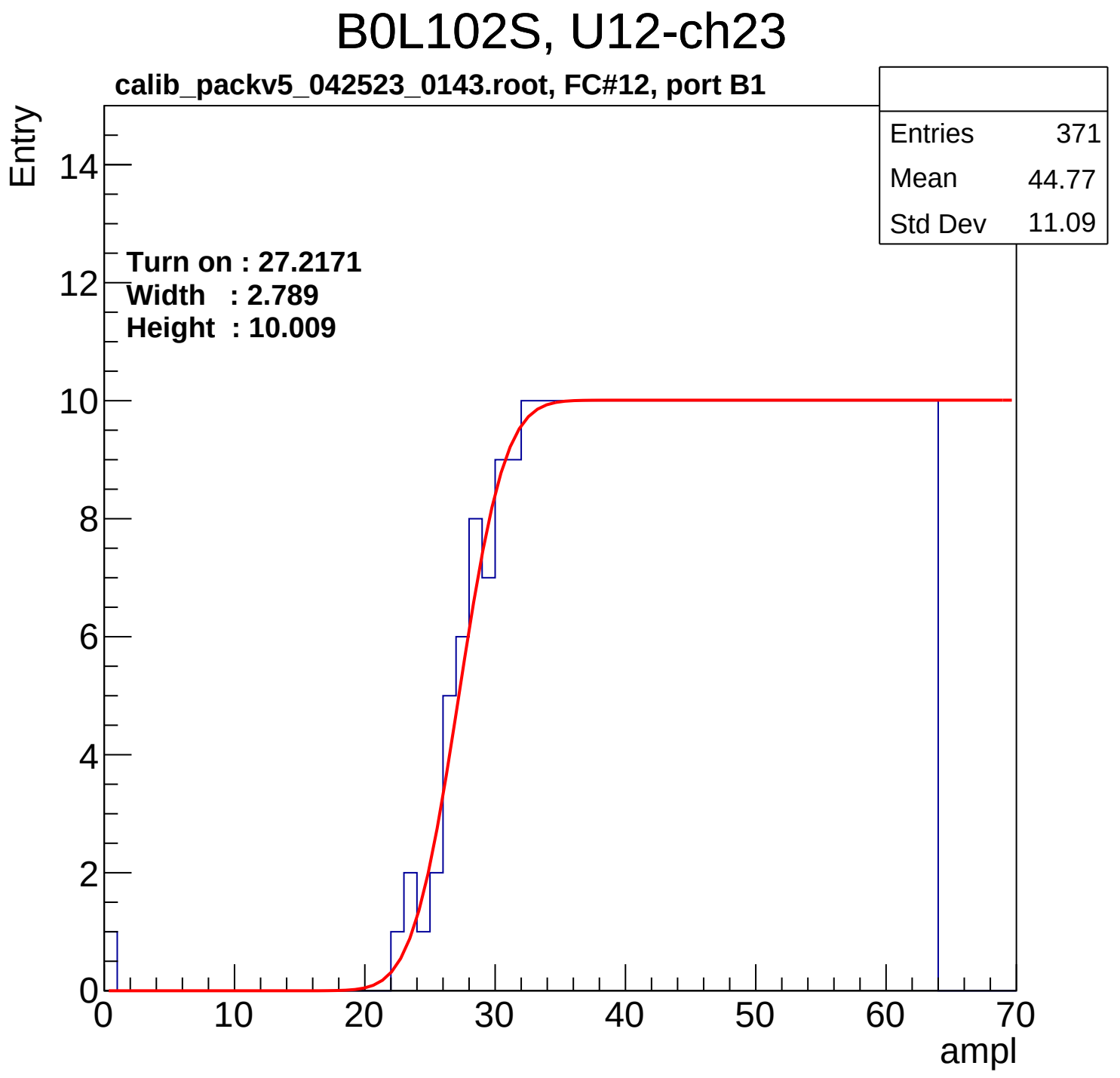
B0L102S, U12-ch23
calib_packv5_042523_0143.root, FC#12, port B1
Entries 371
Mean 44.77
Std Dev 11.09
Turn on : 27.2171
Width : 2.789
Height : 10.009
Entry
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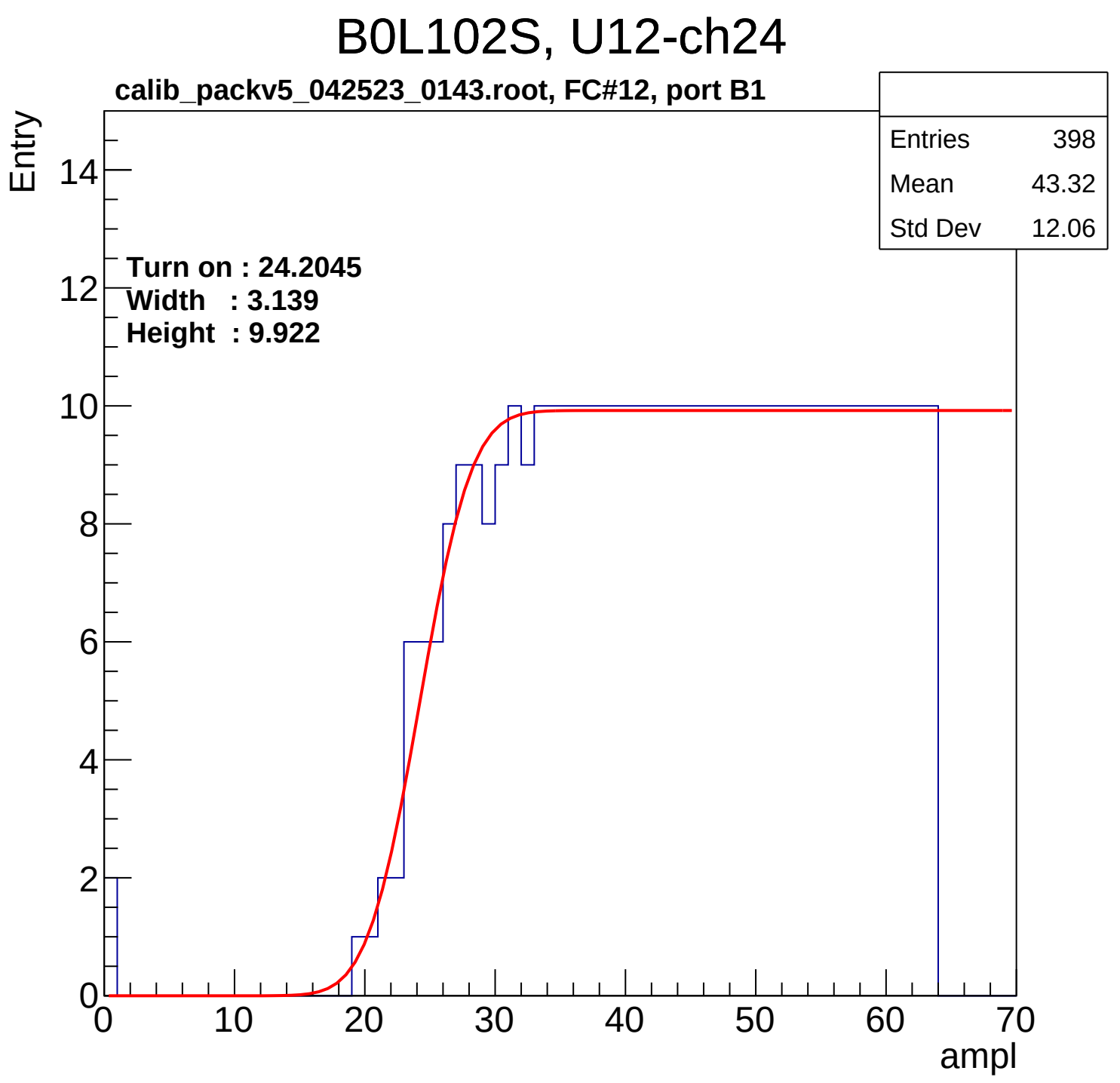
B0L102S, U12-ch24
calib_packv5_042523_0143.root, FC#12, port B1
Entries 398
Mean 43.32
Std Dev 12.06
Turn on : 24.2045
Width : 3.139
Height : 9.922
Entry
ampl
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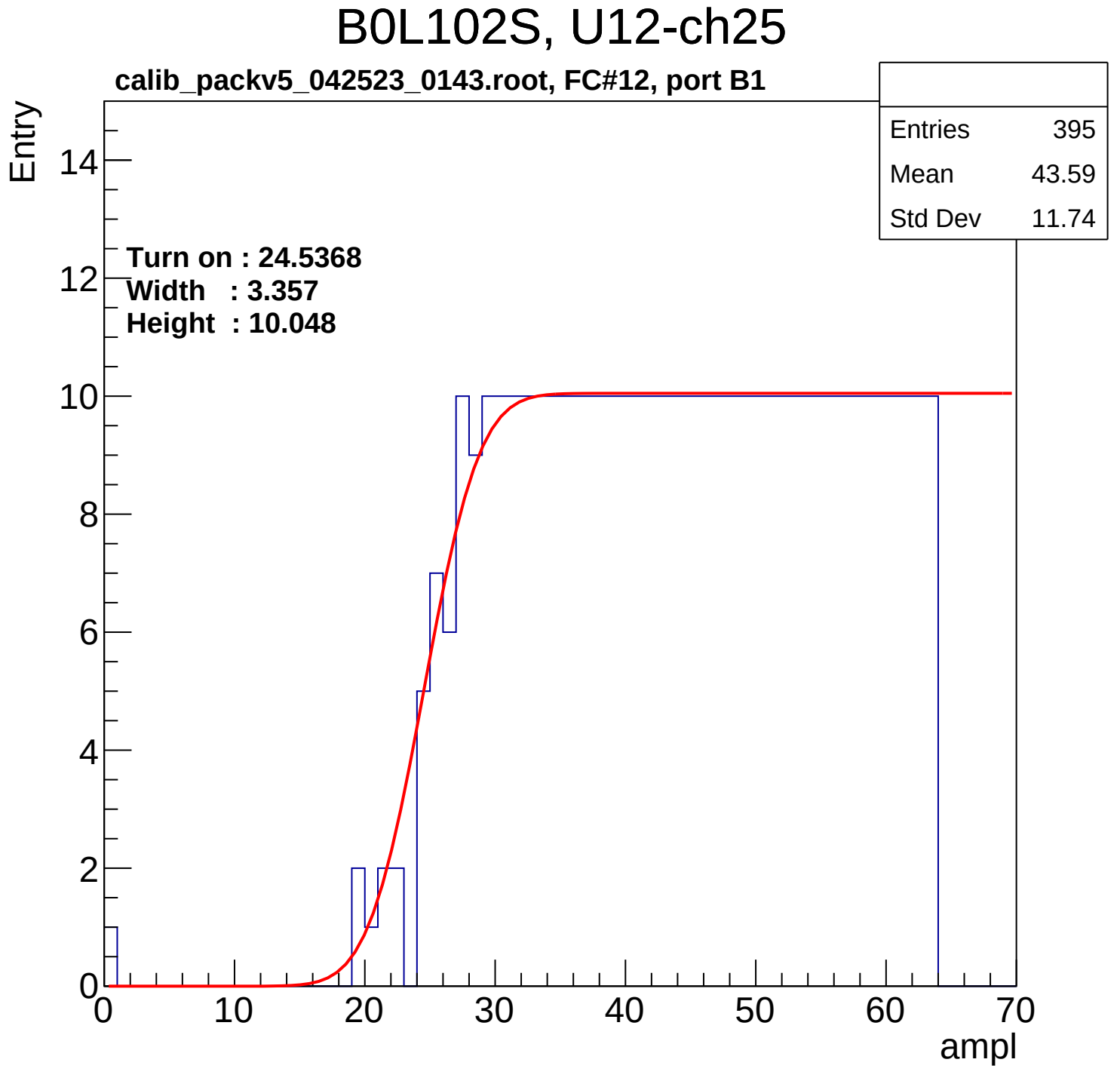
B0L102S, U12-ch25
calib_packv5_042523_0143.root, FC#12, port B1
Entries 395
Mean 43.59
Std Dev 11.74
Turn on : 24.5368
Width : 3.357
Height : 10.048
Entry
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8
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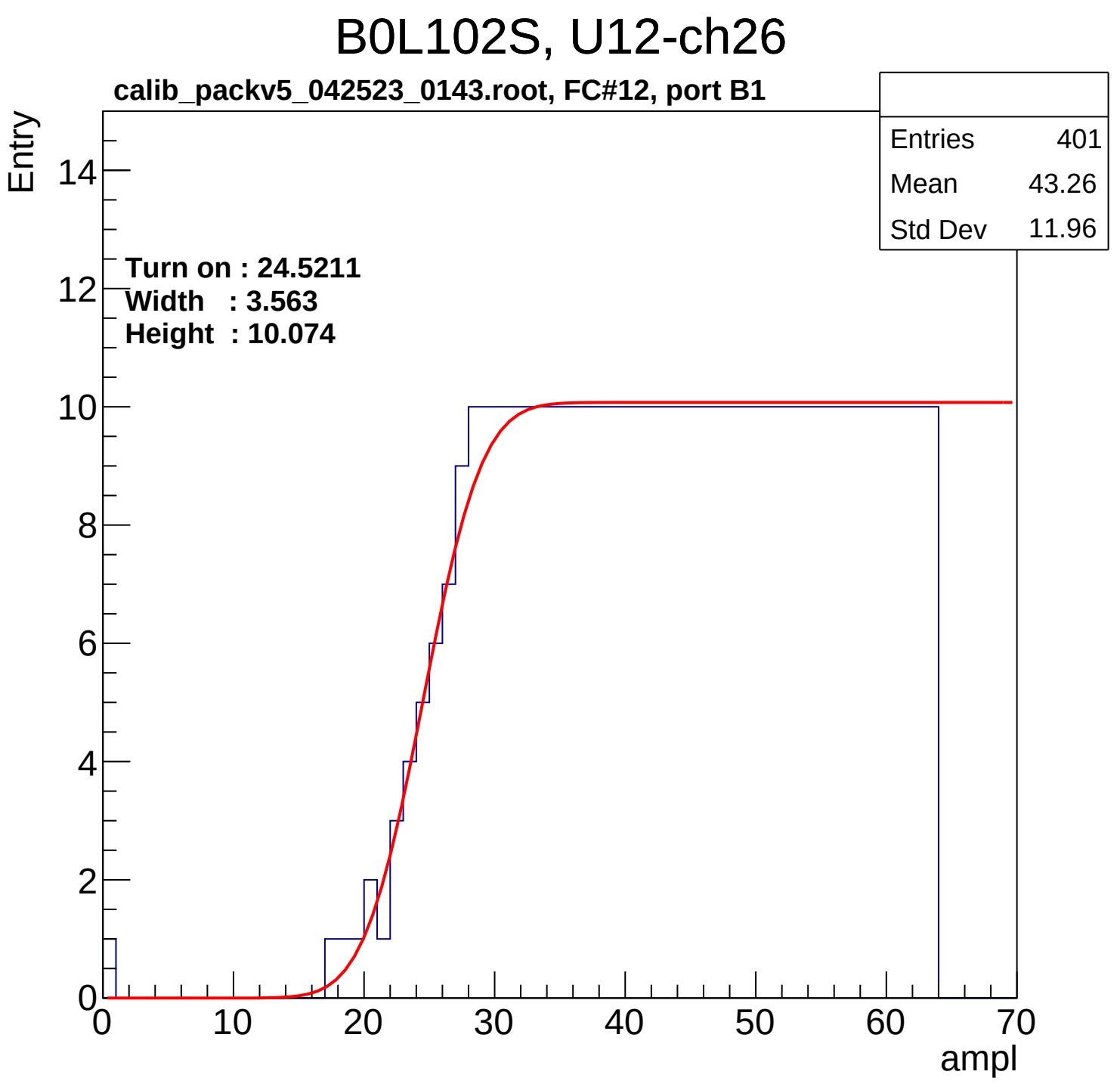
B0L102S, U12-ch26
calib_packv5_042523_0143.root, FC#12, port B1
Entries 401
Mean 43.26
Std Dev 11.96
Turn on : 24.5211
Width : 3.563
Height : 10.074
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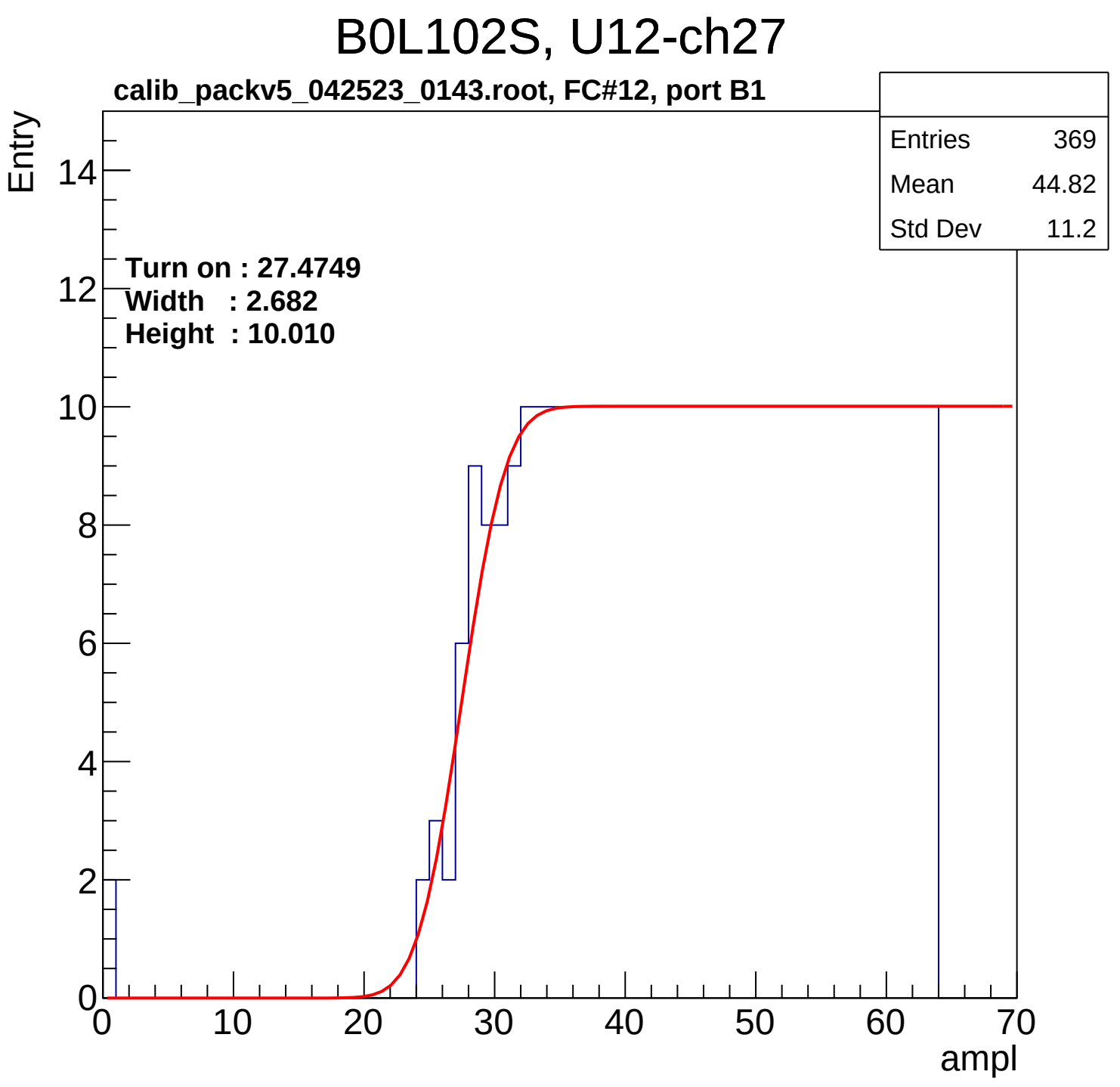
B0L102S, U12-ch27
calib_packv5_042523_0143.root, FC#12, port B1
Entries 369
Mean 44.82
Std Dev 11.2
Turn on : 27.4749
Width : 2.682
Height : 10.010
Entry
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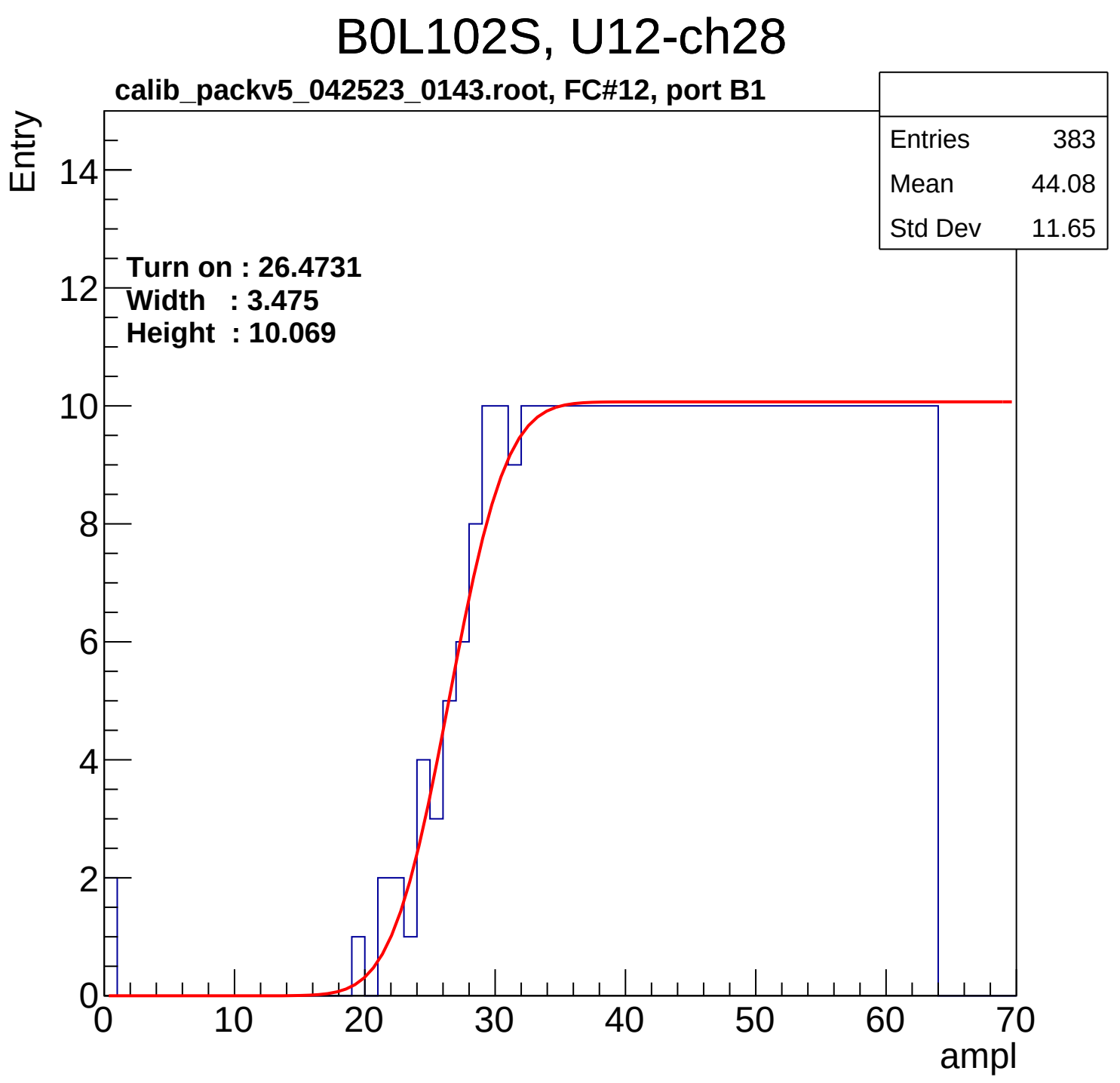
B0L102S, U12-ch28
calib_packv5_042523_0143.root, FC#12, port B1
Entries 383
Mean 44.08
Std Dev 11.65
Turn on : 26.4731
Width : 3.475
Height : 10.069
Entry
ampl
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4
6
8
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12
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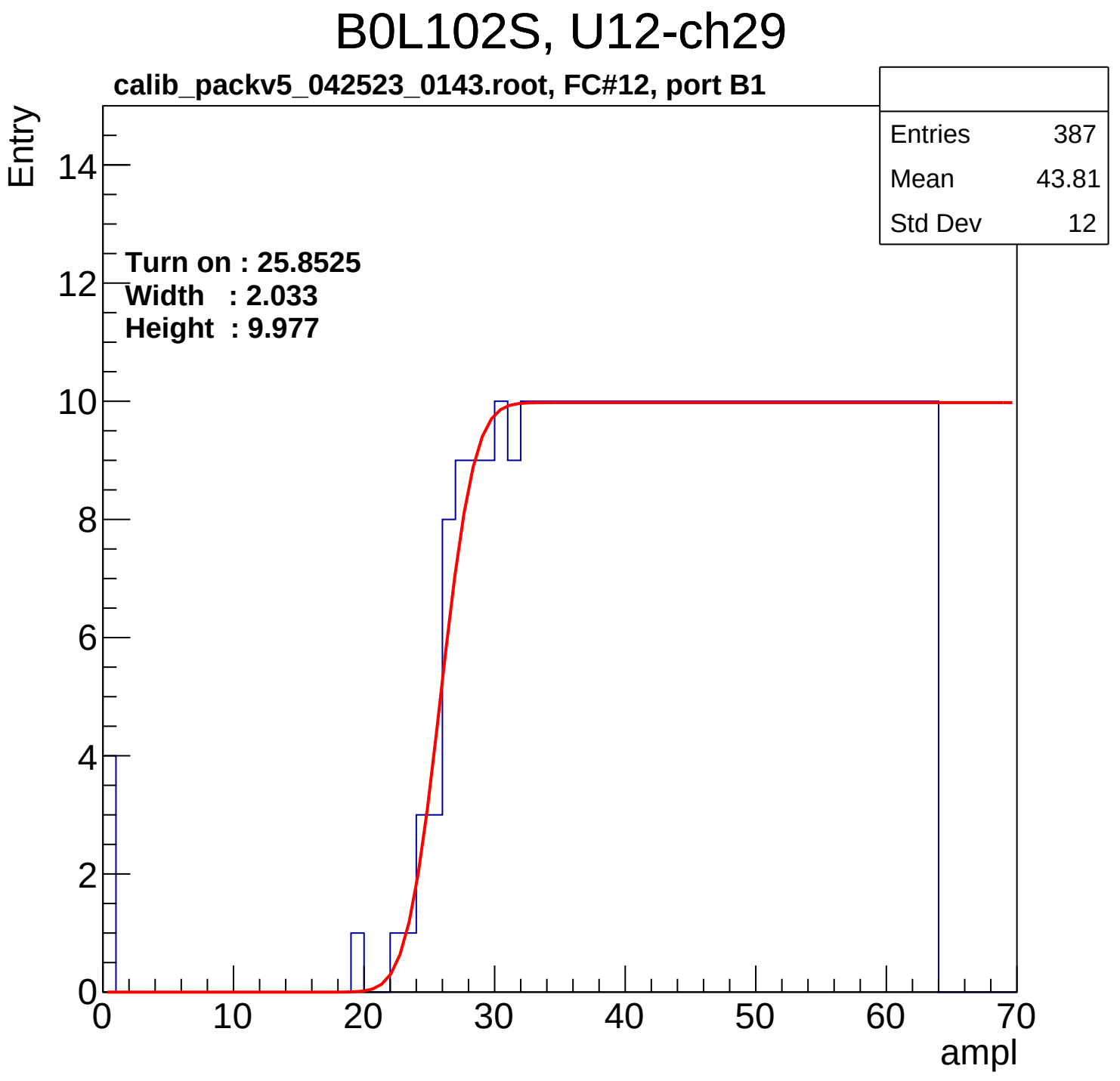
B0L102S, U12-ch29
calib_packv5_042523_0143.root, FC#12, port B1
Entries 387
Mean 43.81
Std Dev 12
Turn on : 25.8525
Width : 2.033
Height : 9.977
Entry
ampl
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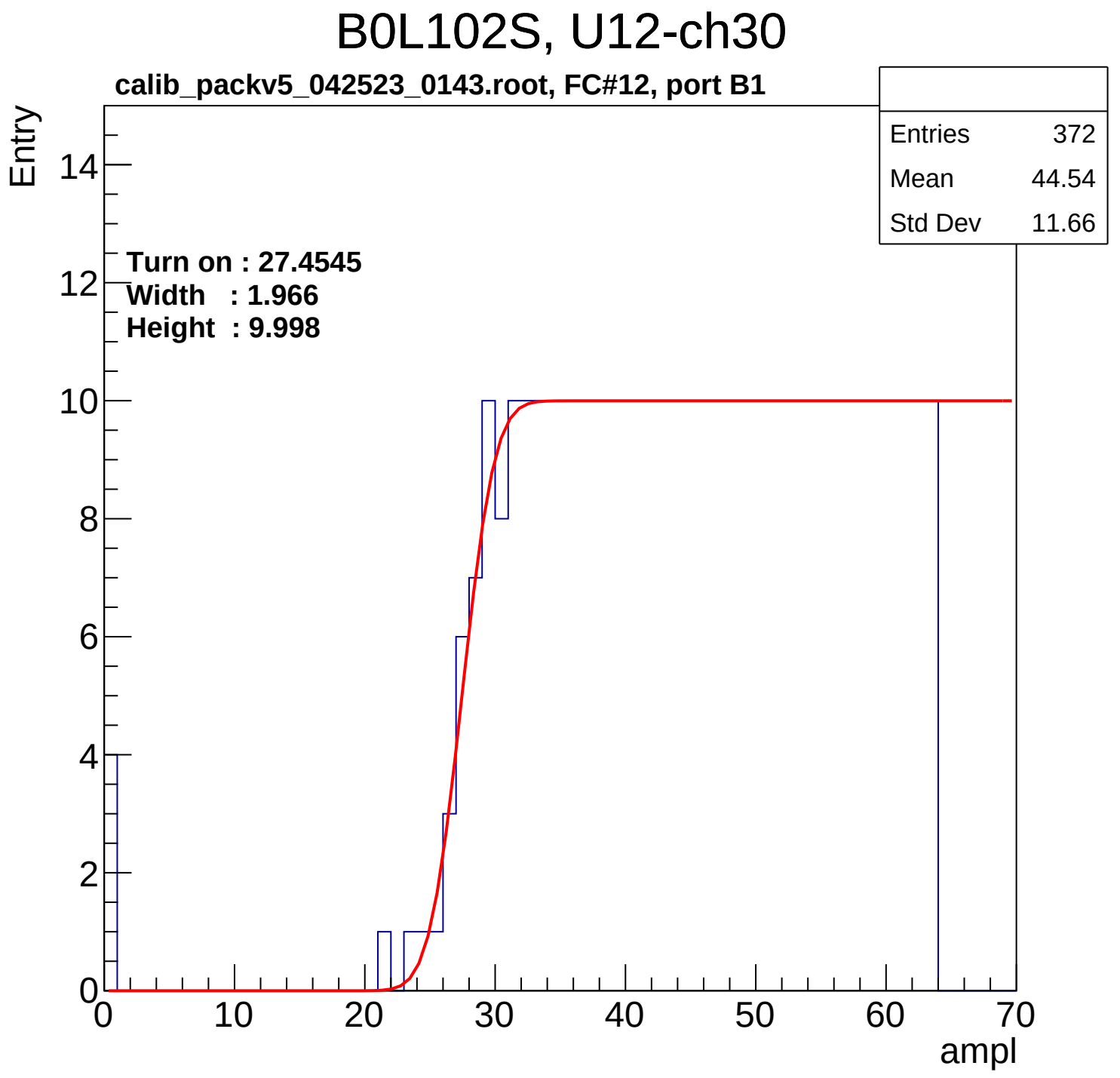
B0L102S, U12-ch30
calib_packv5_042523_0143.root, FC#12, port B1
Entries 372
Mean 44.54
Std Dev 11.66
Turn on : 27.4545
Width : 1.966
Height : 9.998
Entry
ampl
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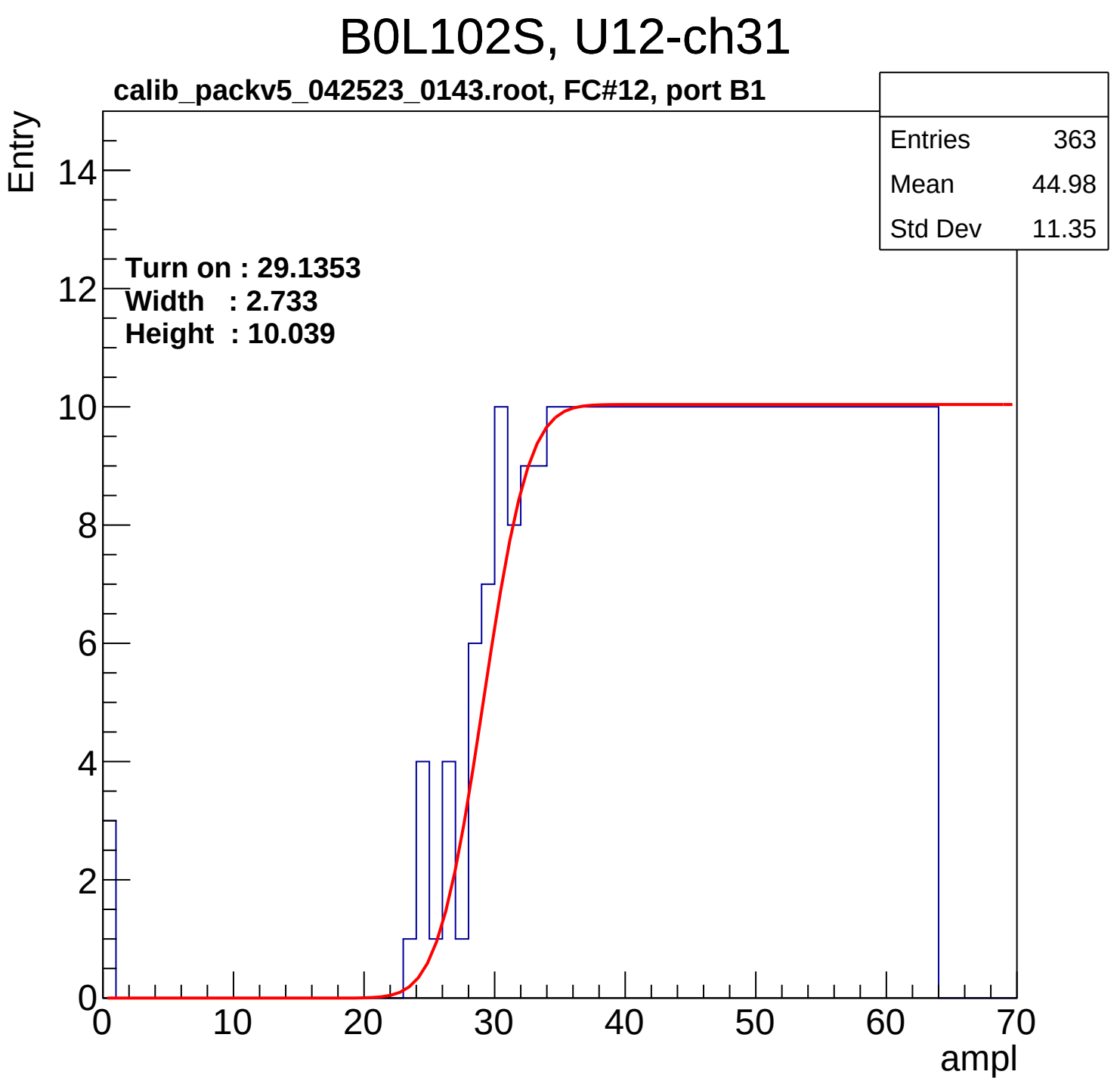
B0L102S, U12-ch31
calib_packv5_042523_0143.root, FC#12, port B1
Entries 363
Mean 44.98
Std Dev 11.35
Turn on : 29.1353
Width : 2.733
Height : 10.039
Entry
ampl
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2
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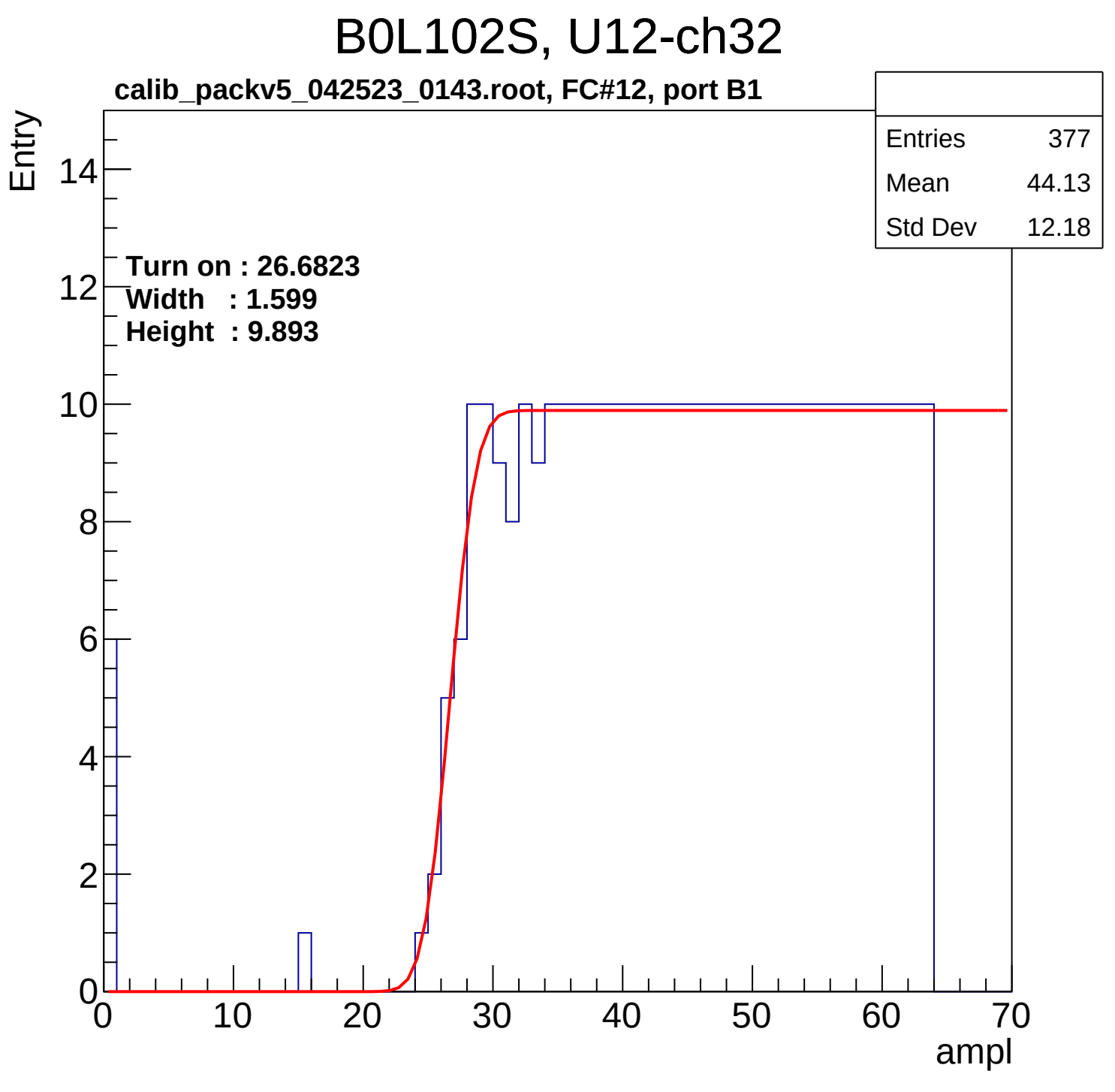
B0L102S, U12-ch32
calib_packv5_042523_0143.root, FC#12, port B1
Entries 377
Mean 44.13
Std Dev 12.18
Turn on : 26.6823
Width : 1.599
Height : 9.893
Entry
ampl
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2
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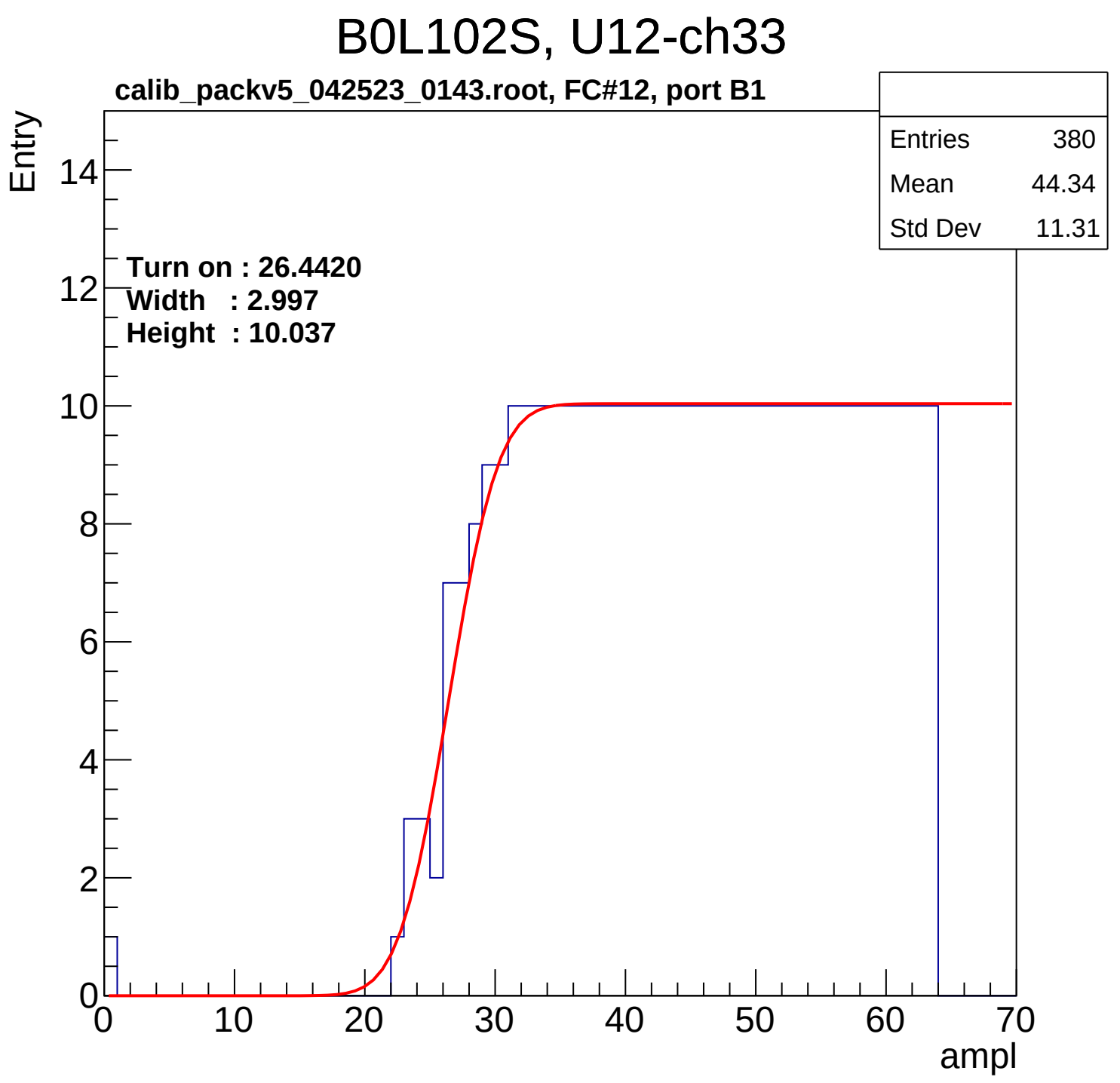
B0L102S, U12-ch33
calib_packv5_042523_0143.root, FC#12, port B1
Entries 380
Mean 44.34
Std Dev 11.31
Turn on : 26.4420
Width : 2.997
Height : 10.037
Entry
ampl
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2
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6
8
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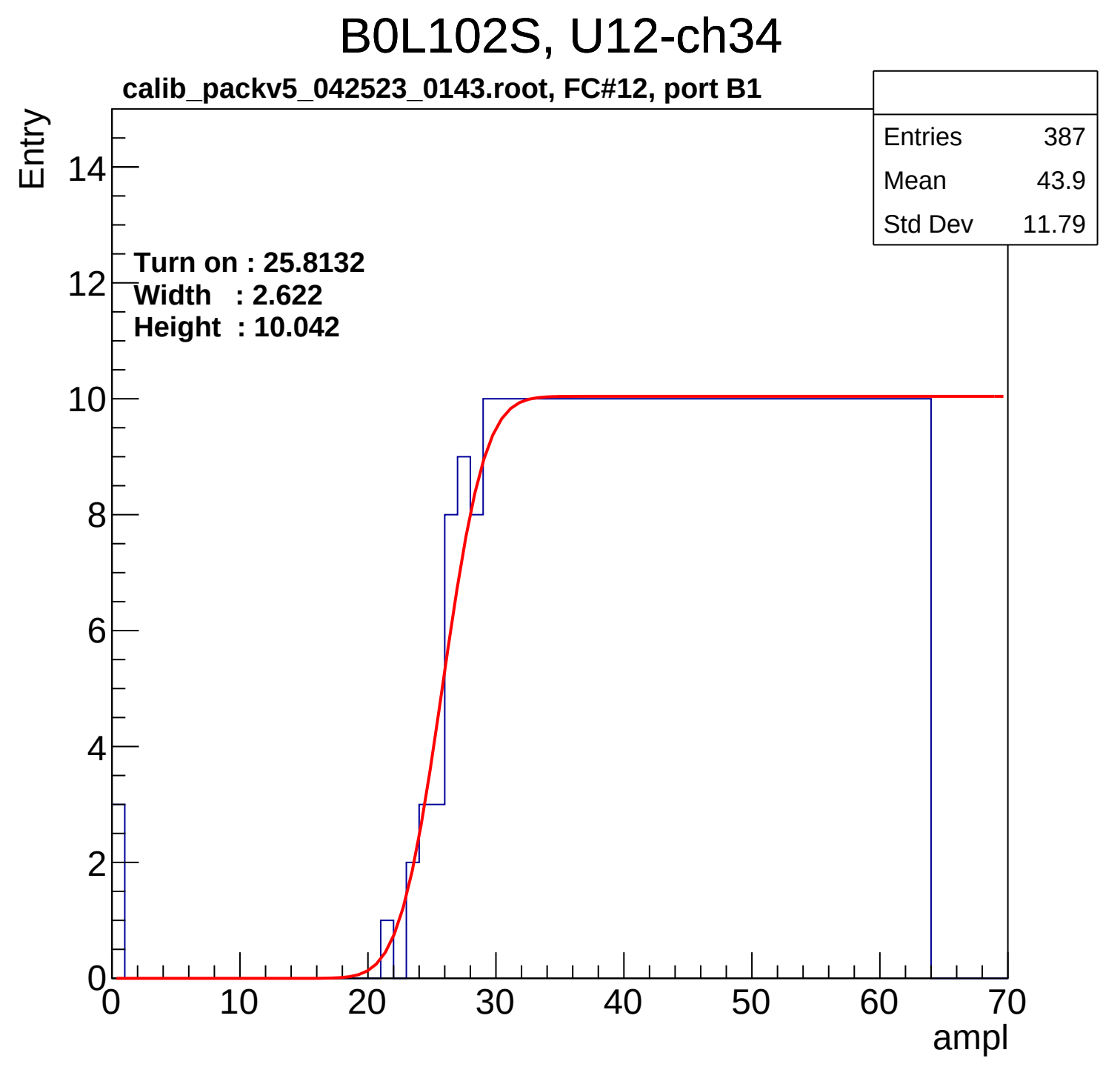
B0L102S, U12-ch34
calib_packv5_042523_0143.root, FC#12, port B1
Entries 387
Mean 43.9
Std Dev 11.79
Turn on : 25.8132
Width : 2.622
Height : 10.042
Entry
ampl
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2
4
6
8
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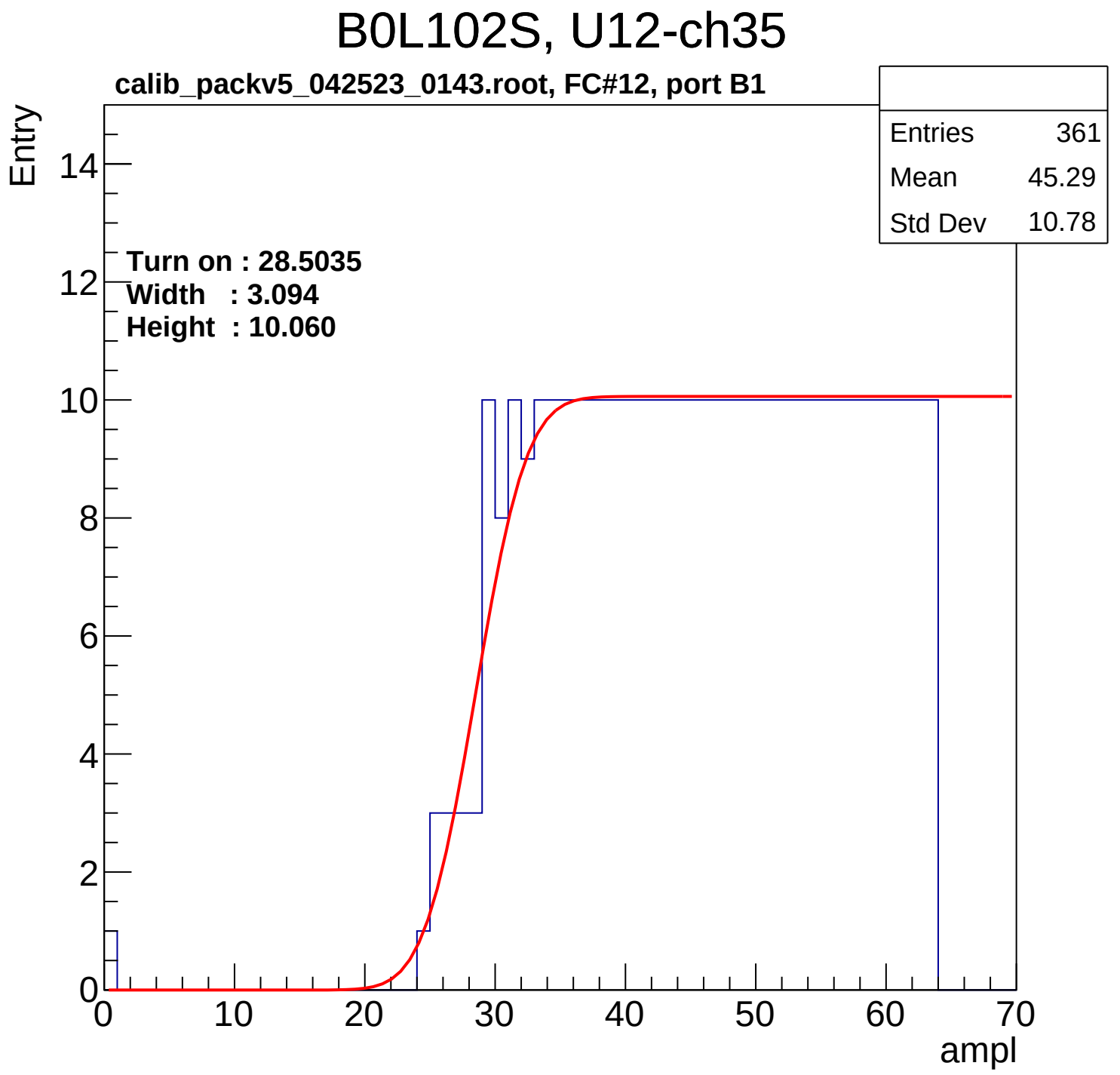
B0L102S, U12-ch35
calib_packv5_042523_0143.root, FC#12, port B1
Entries 361
Mean 45.29
Std Dev 10.78
Turn on : 28.5035
Width : 3.094
Height : 10.060
Entry
ampl
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6
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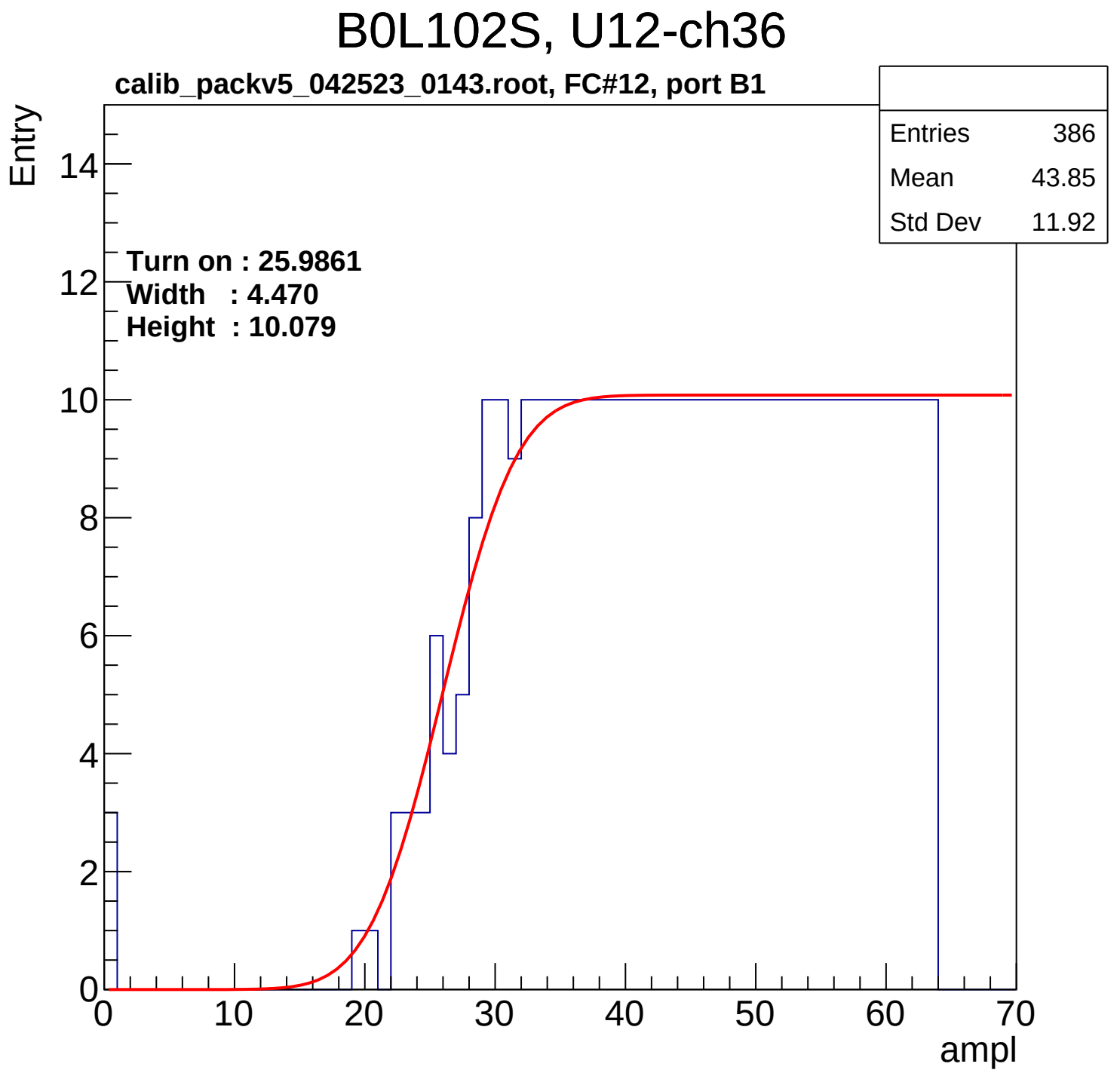
B0L102S, U12-ch36
calib_packv5_042523_0143.root, FC#12, port B1
Entries 386
Mean 43.85
Std Dev 11.92
Turn on : 25.9861
Width : 4.470
Height : 10.079
Entry
ampl
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2
4
6
8
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60
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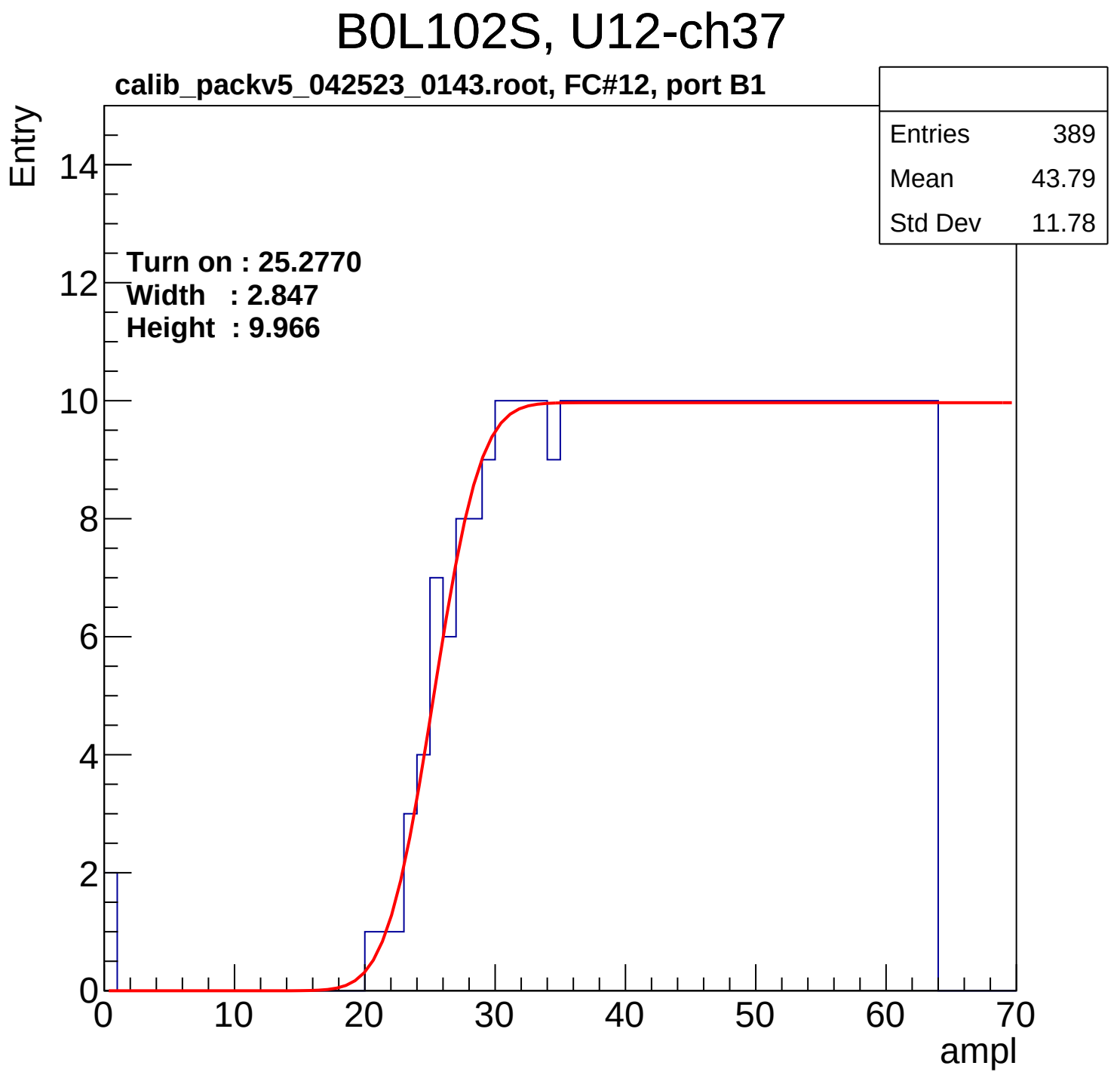
B0L102S, U12-ch37
calib_packv5_042523_0143.root, FC#12, port B1
Entries 389
Mean 43.79
Std Dev 11.78
Turn on : 25.2770
Width : 2.847
Height : 9.966
Entry
ampl
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2
4
6
8
10
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0
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60
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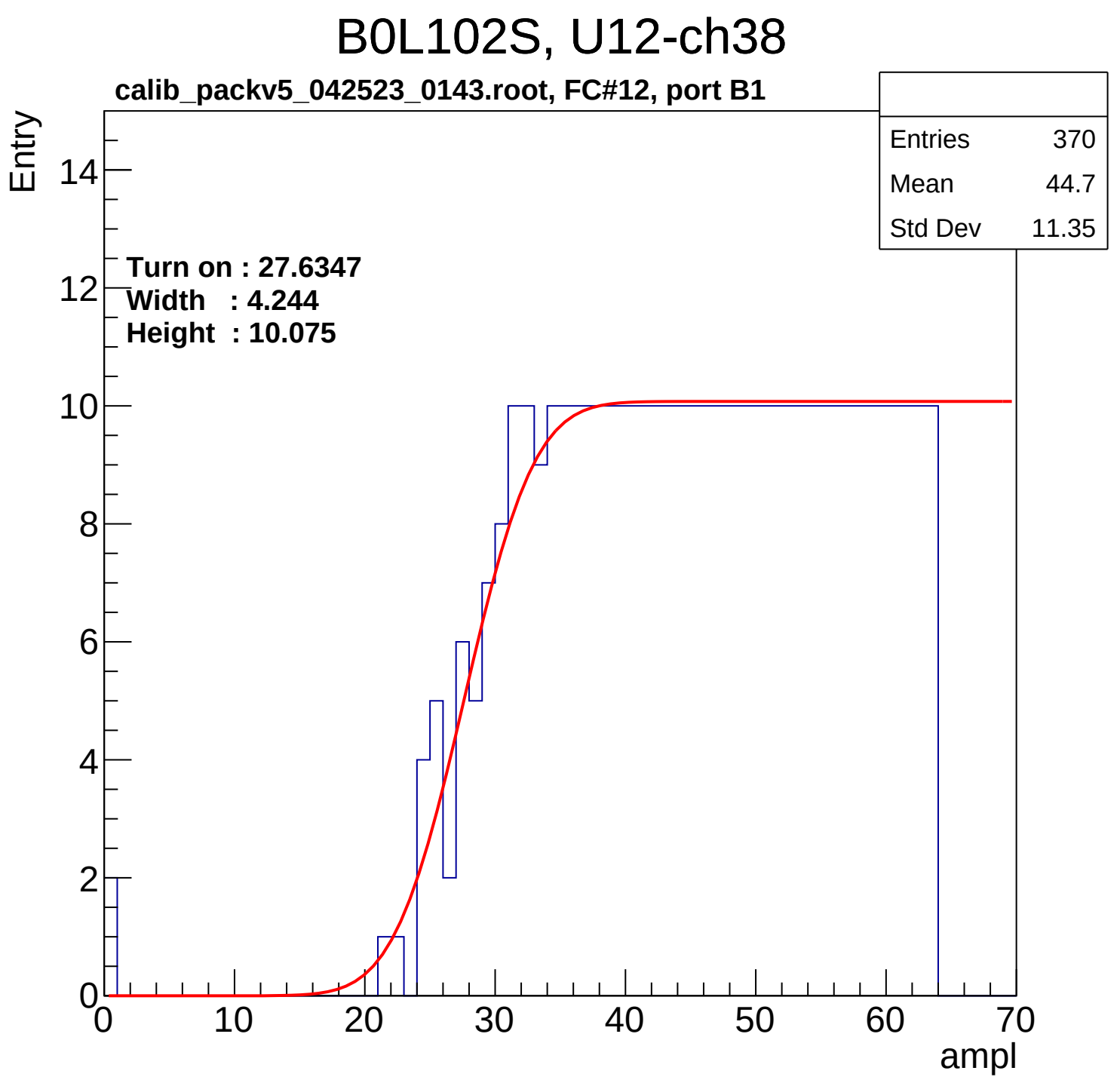
B0L102S, U12-ch38
calib_packv5_042523_0143.root, FC#12, port B1
Entries 370
Mean 44.7
Std Dev 11.35
Turn on : 27.6347
Width : 4.244
Height : 10.075
Entry
ampl
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6
8
10
12
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0
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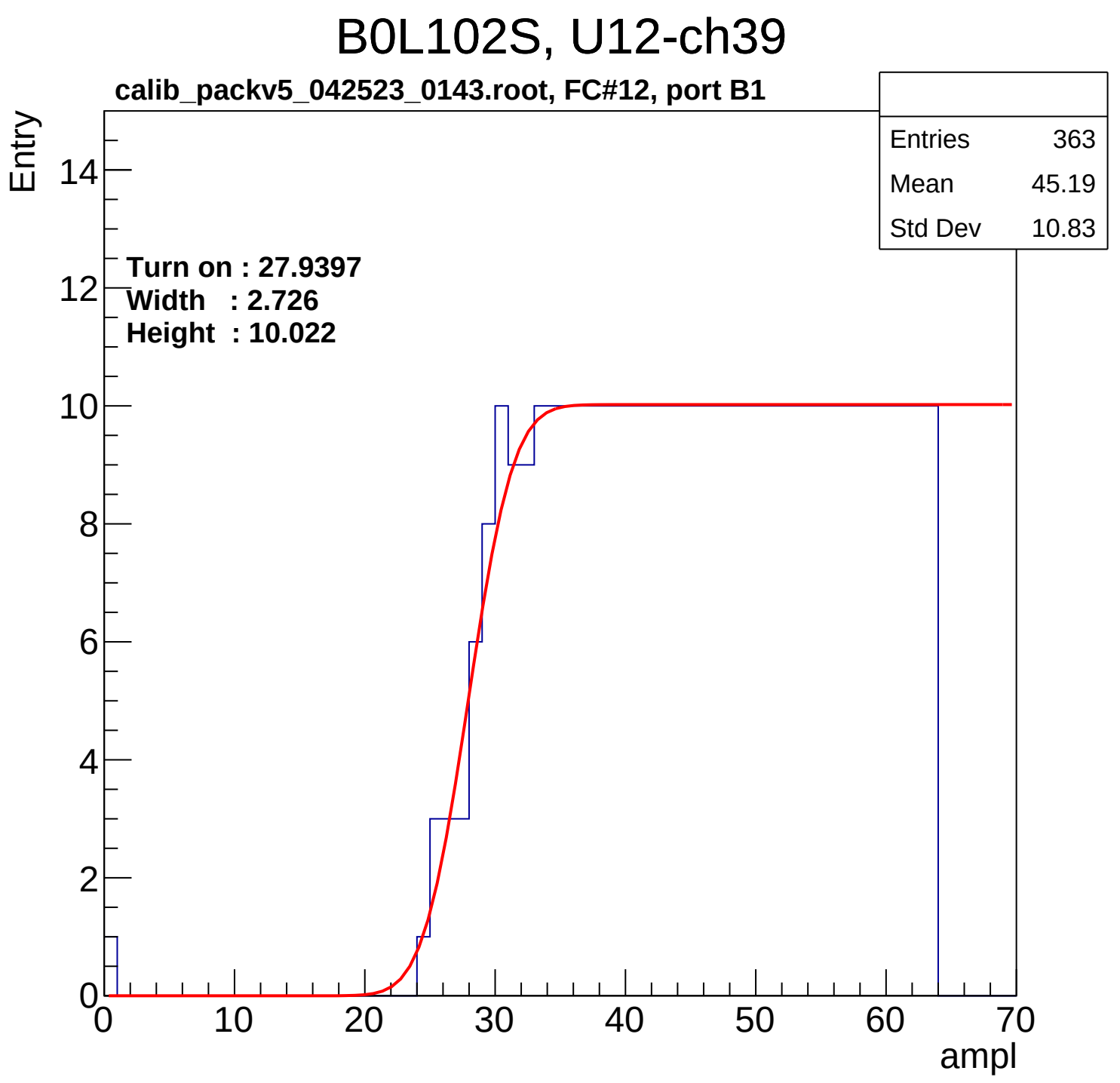
B0L102S, U12-ch39
calib_packv5_042523_0143.root, FC#12, port B1
Entries 363
Mean 45.19
Std Dev 10.83
Turn on : 27.9397
Width : 2.726
Height : 10.022
Entry
ampl
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6
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0
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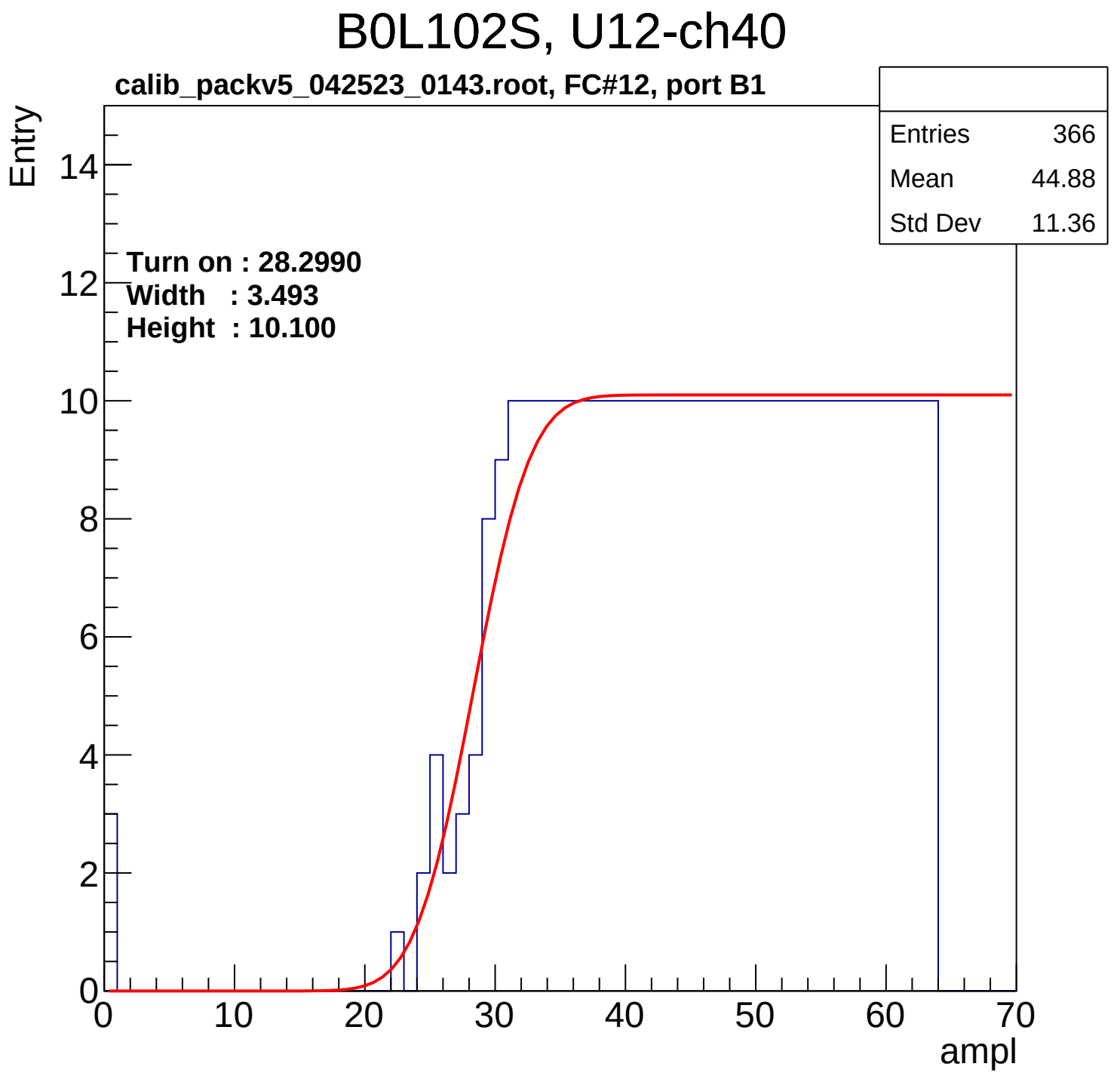
B0L102S, U12-ch40
calib_packv5_042523_0143.root, FC#12, port B1
Entries 366
Mean 44.88
Std Dev 11.36
Turn on : 28.2990
Width : 3.493
Height : 10.100
Entry
ampl
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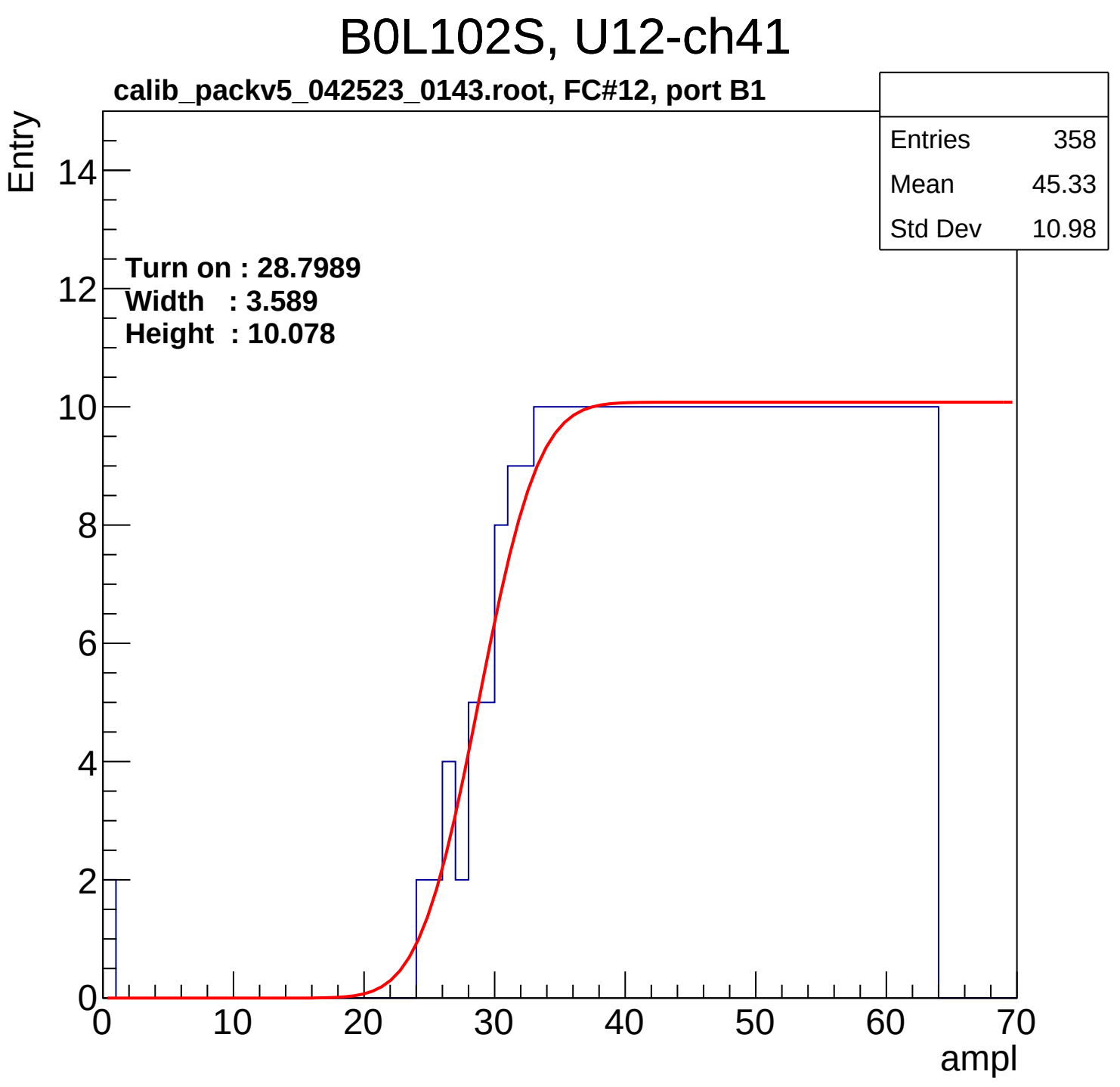
B0L102S, U12-ch41
calib_packv5_042523_0143.root, FC#12, port B1
Entries 358
Mean 45.33
Std Dev 10.98
Turn on : 28.7989
Width : 3.589
Height : 10.078
Entry
ampl
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4
6
8
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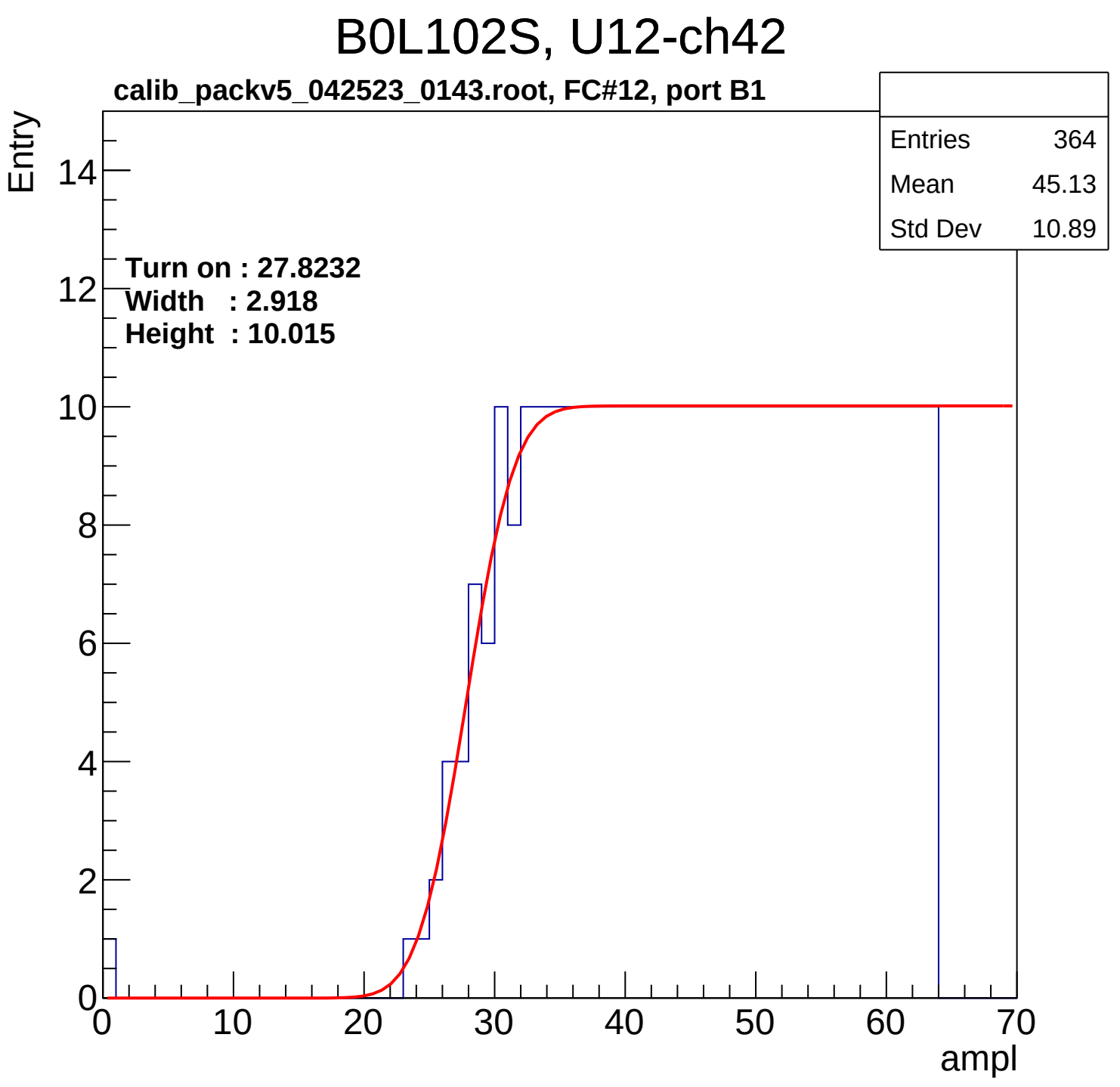
B0L102S, U12-ch42
calib_packv5_042523_0143.root, FC#12, port B1
Entries 364
Mean 45.13
Std Dev 10.89
Turn on : 27.8232
Width : 2.918
Height : 10.015
Entry
ampl
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2
4
6
8
10
12
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0
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20
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40
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60
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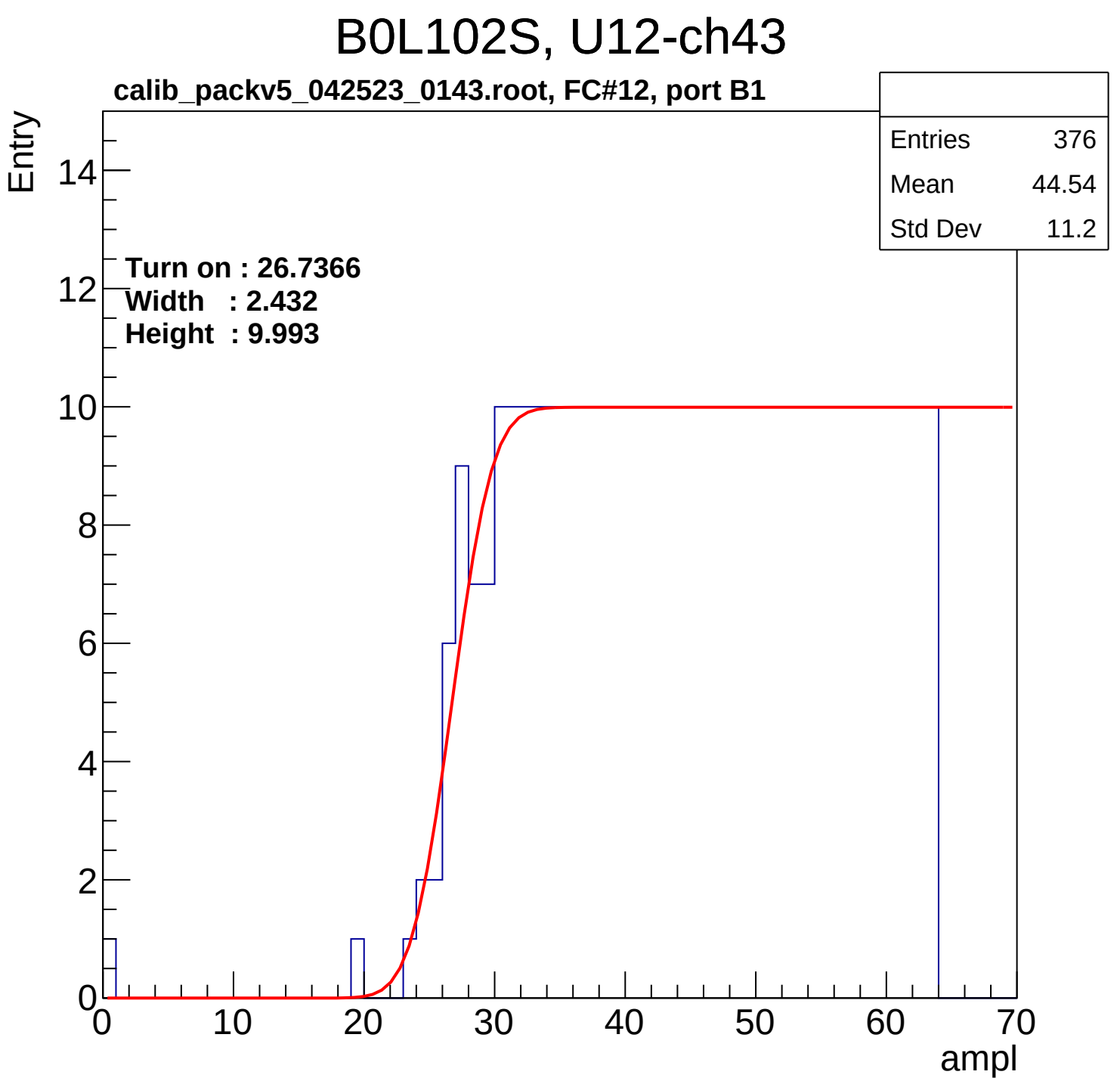
B0L102S, U12-ch43
calib_packv5_042523_0143.root, FC#12, port B1
Entries 376
Mean 44.54
Std Dev 11.2
Turn on : 26.7366
Width : 2.432
Height : 9.993
Entry
ampl
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6
8
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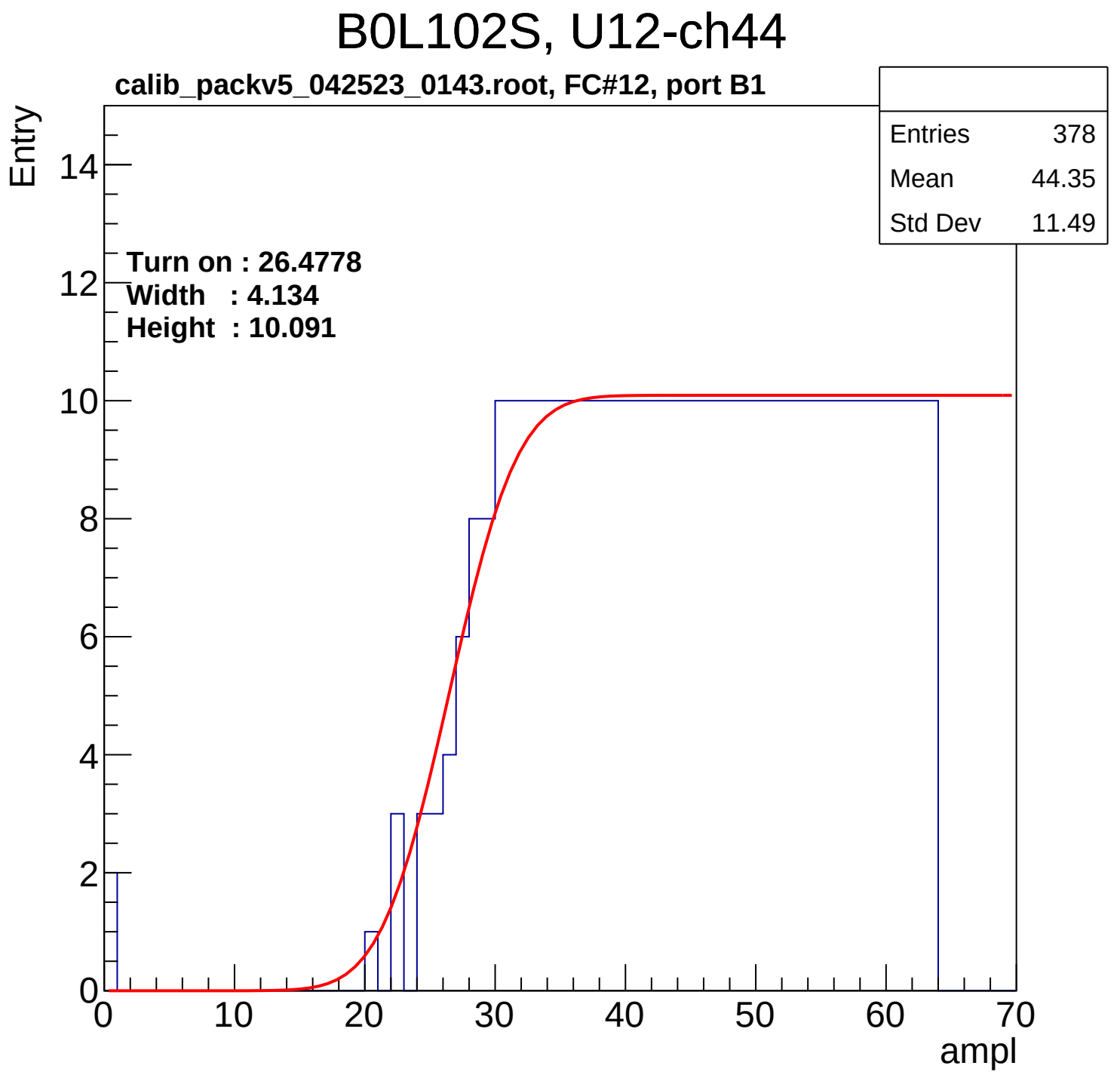
B0L102S, U12-ch44
calib_packv5_042523_0143.root, FC#12, port B1
Entries 378
Mean 44.35
Std Dev 11.49
Turn on : 26.4778
Width : 4.134
Height : 10.091
Entry
ampl
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6
8
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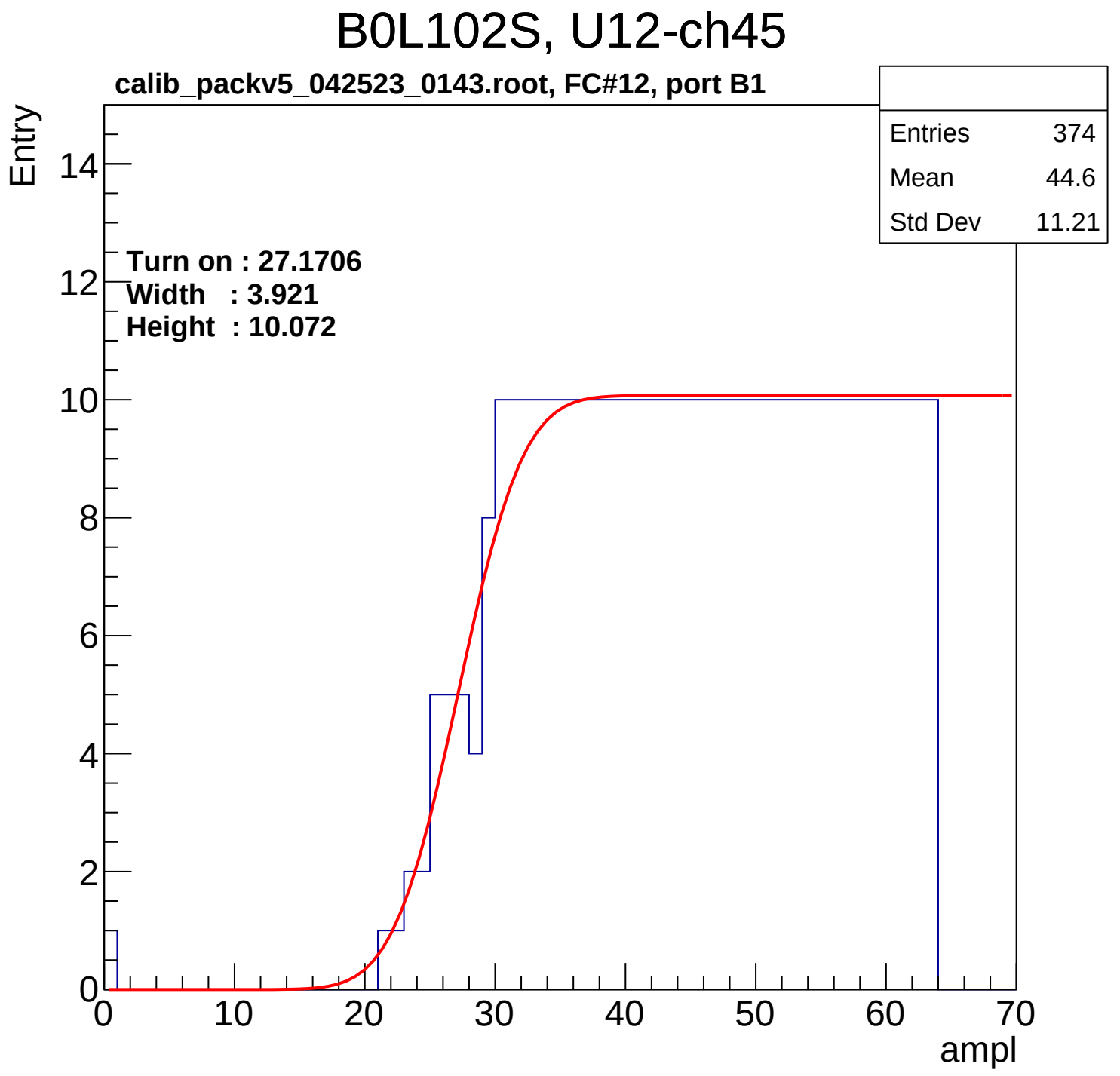
B0L102S, U12-ch45
calib_packv5_042523_0143.root, FC#12, port B1
Entries 374
Mean 44.6
Std Dev 11.21
Turn on : 27.1706
Width : 3.921
Height : 10.072
Entry
ampl
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8
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0
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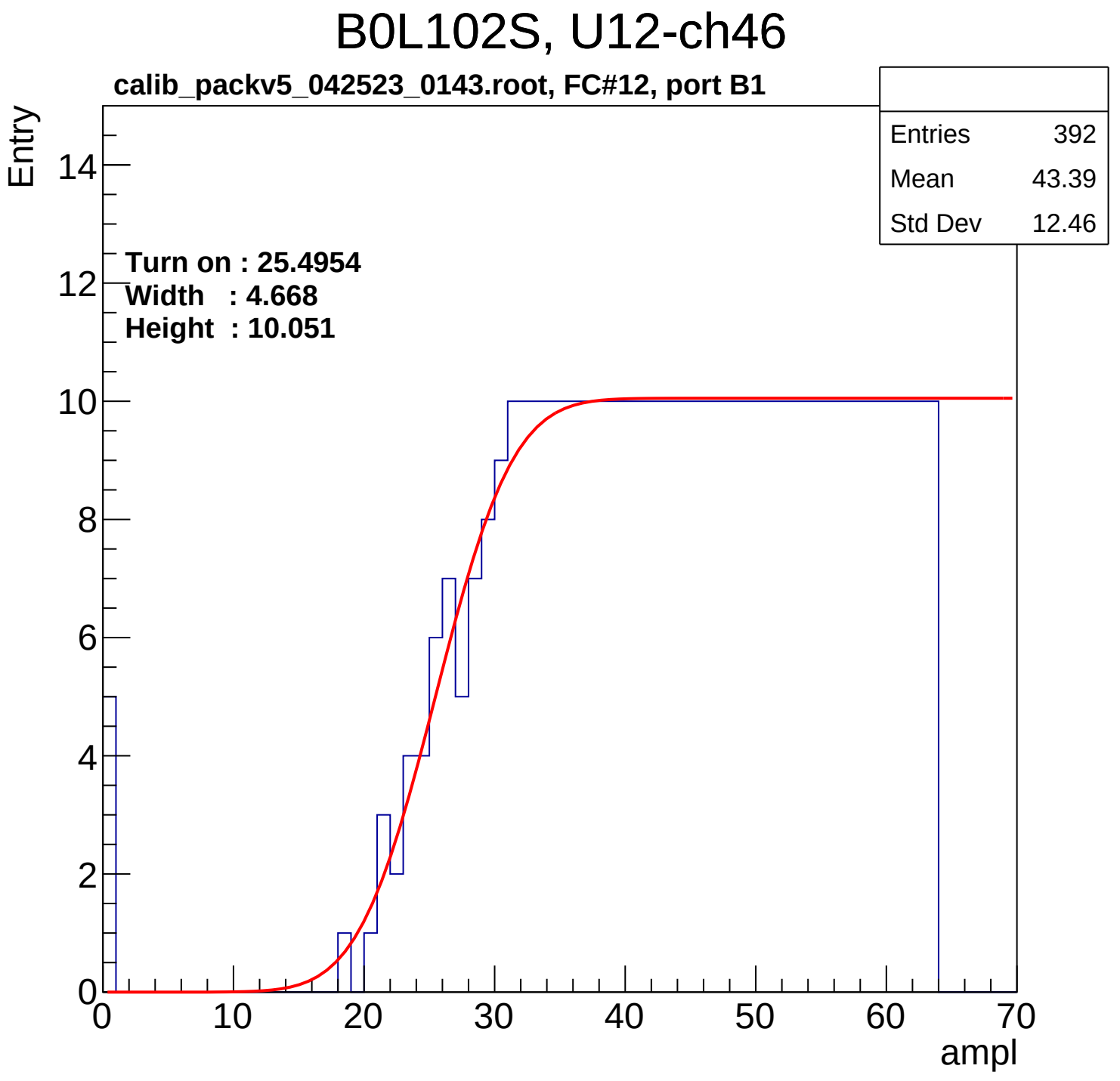
B0L102S, U12-ch46
calib_packv5_042523_0143.root, FC#12, port B1
Entries 392
Mean 43.39
Std Dev 12.46
Turn on : 25.4954
Width : 4.668
Height : 10.051
Entry
ampl
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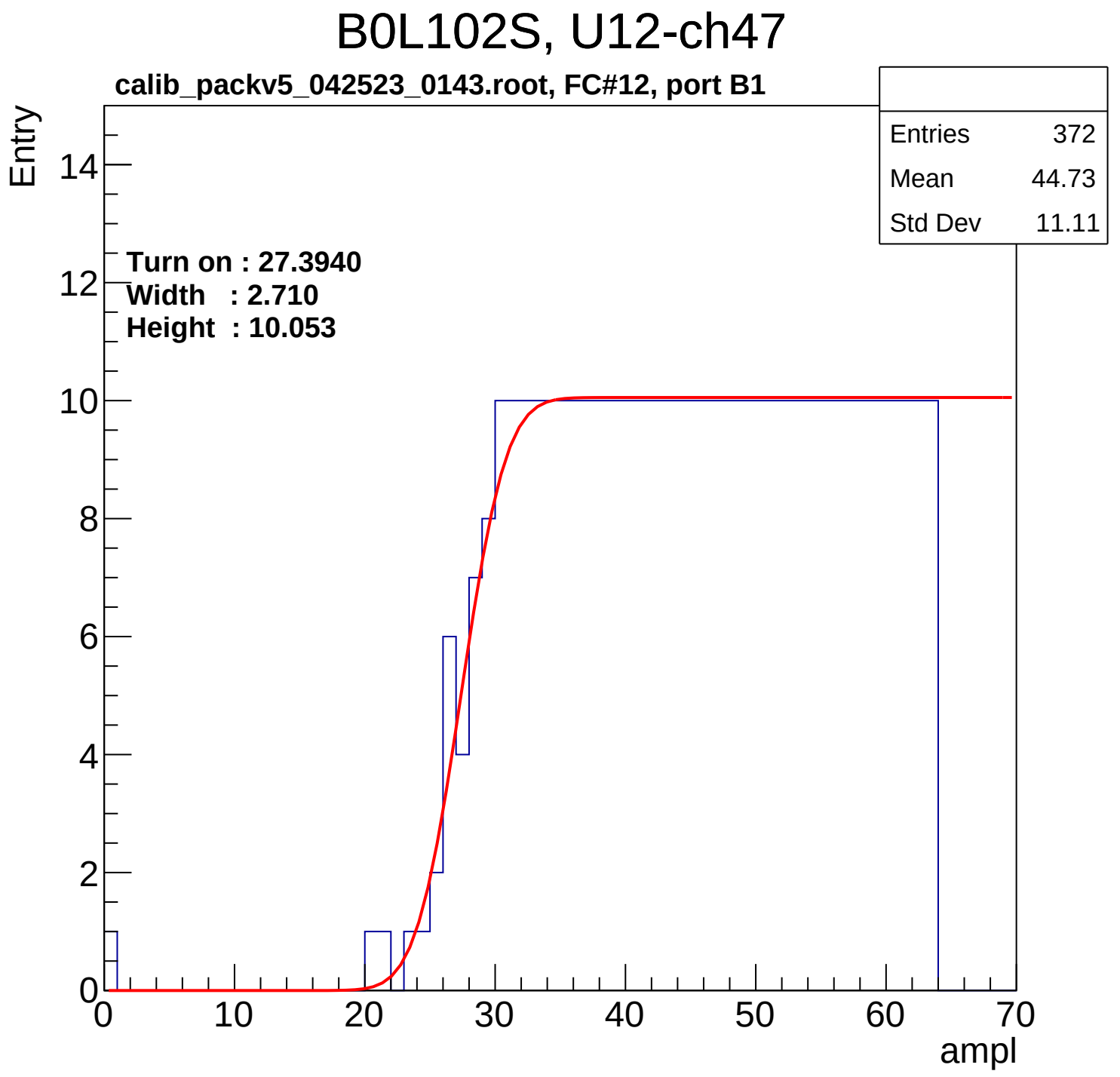
B0L102S, U12-ch47
calib_packv5_042523_0143.root, FC#12, port B1
Entries 372
Mean 44.73
Std Dev 11.11
Turn on : 27.3940
Width : 2.710
Height : 10.053
Entry
ampl
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8
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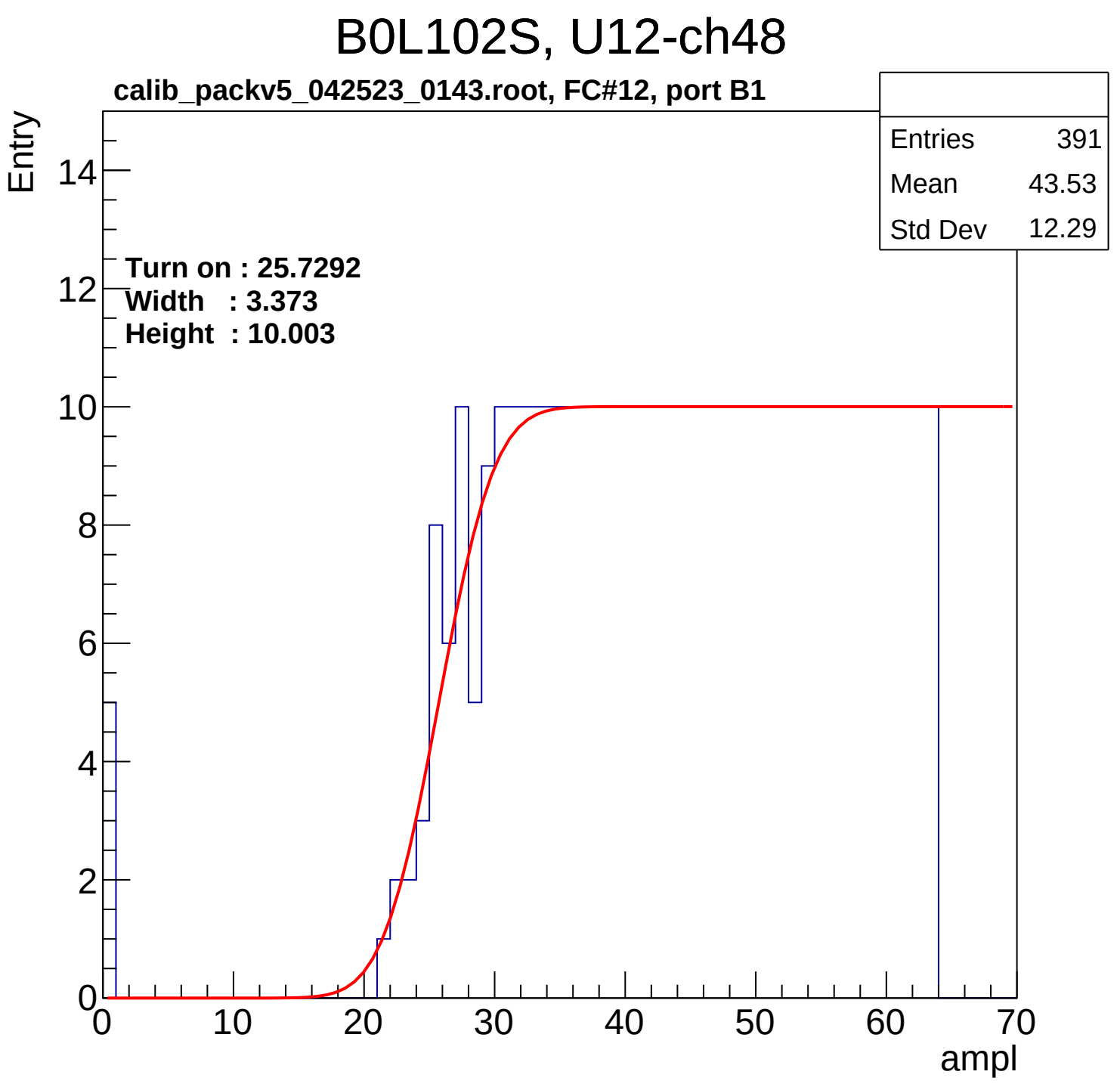
B0L102S, U12-ch48
calib_packv5_042523_0143.root, FC#12, port B1
Entries 391
Mean 43.53
Std Dev 12.29
Turn on : 25.7292
Width : 3.373
Height : 10.003
Entry
ampl
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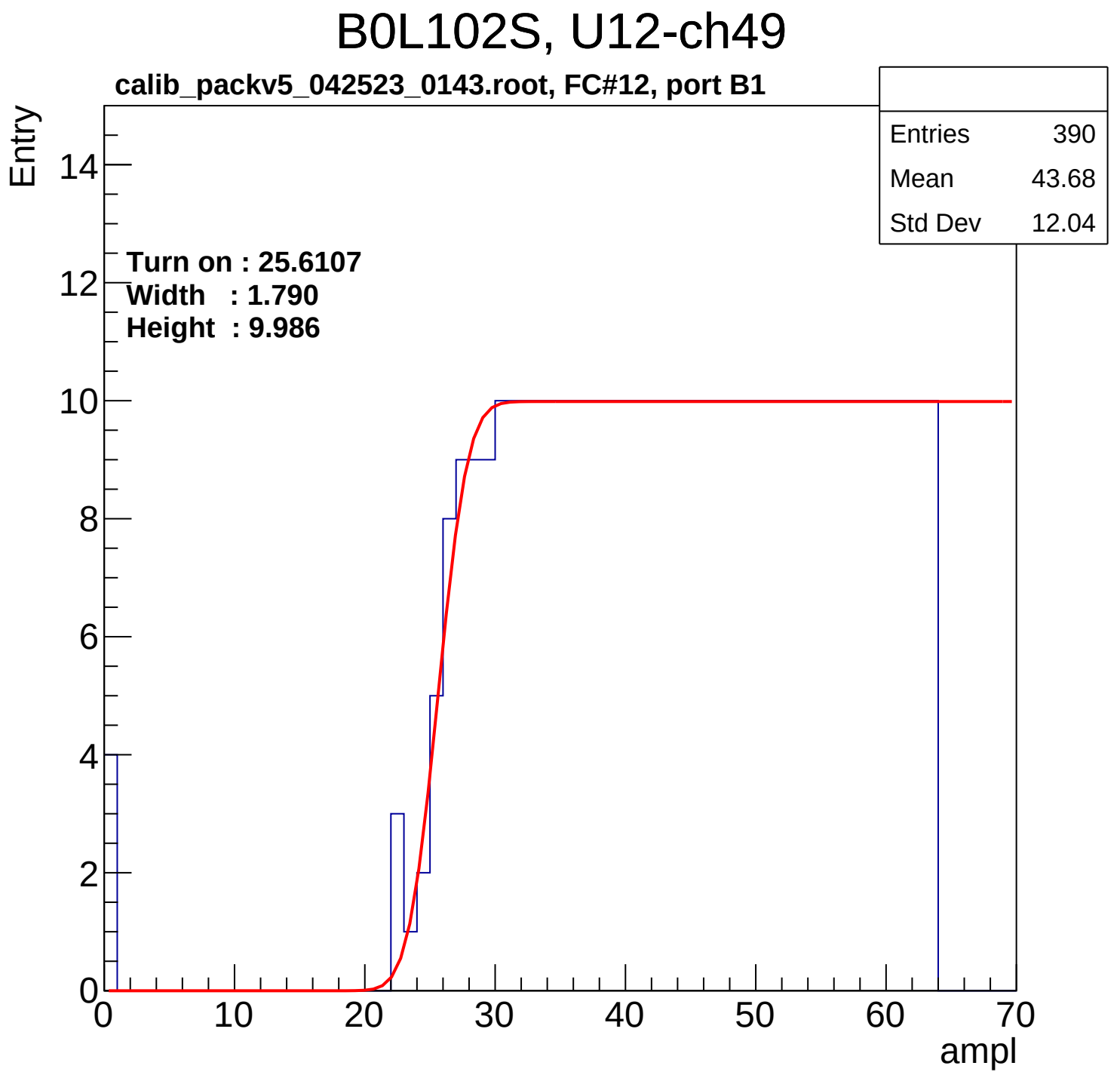
B0L102S, U12-ch49
calib_packv5_042523_0143.root, FC#12, port B1
Entries 390
Mean 43.68
Std Dev 12.04
Turn on : 25.6107
Width : 1.790
Height : 9.986
Entry
ampl
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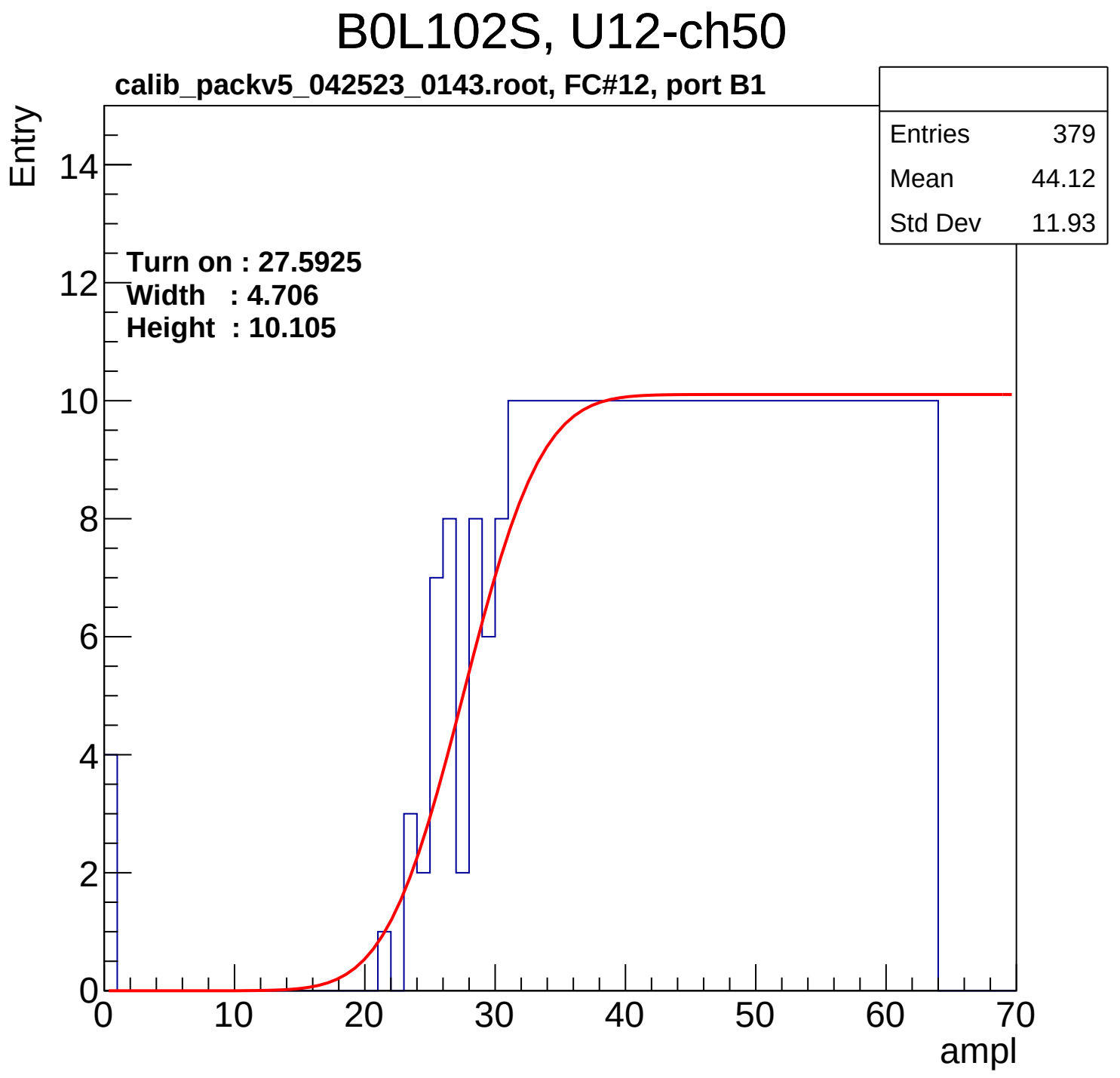
B0L102S, U12-ch50
calib_packv5_042523_0143.root, FC#12, port B1
Entries 379
Mean 44.12
Std Dev 11.93
Turn on : 27.5925
Width : 4.706
Height : 10.105
Entry
ampl
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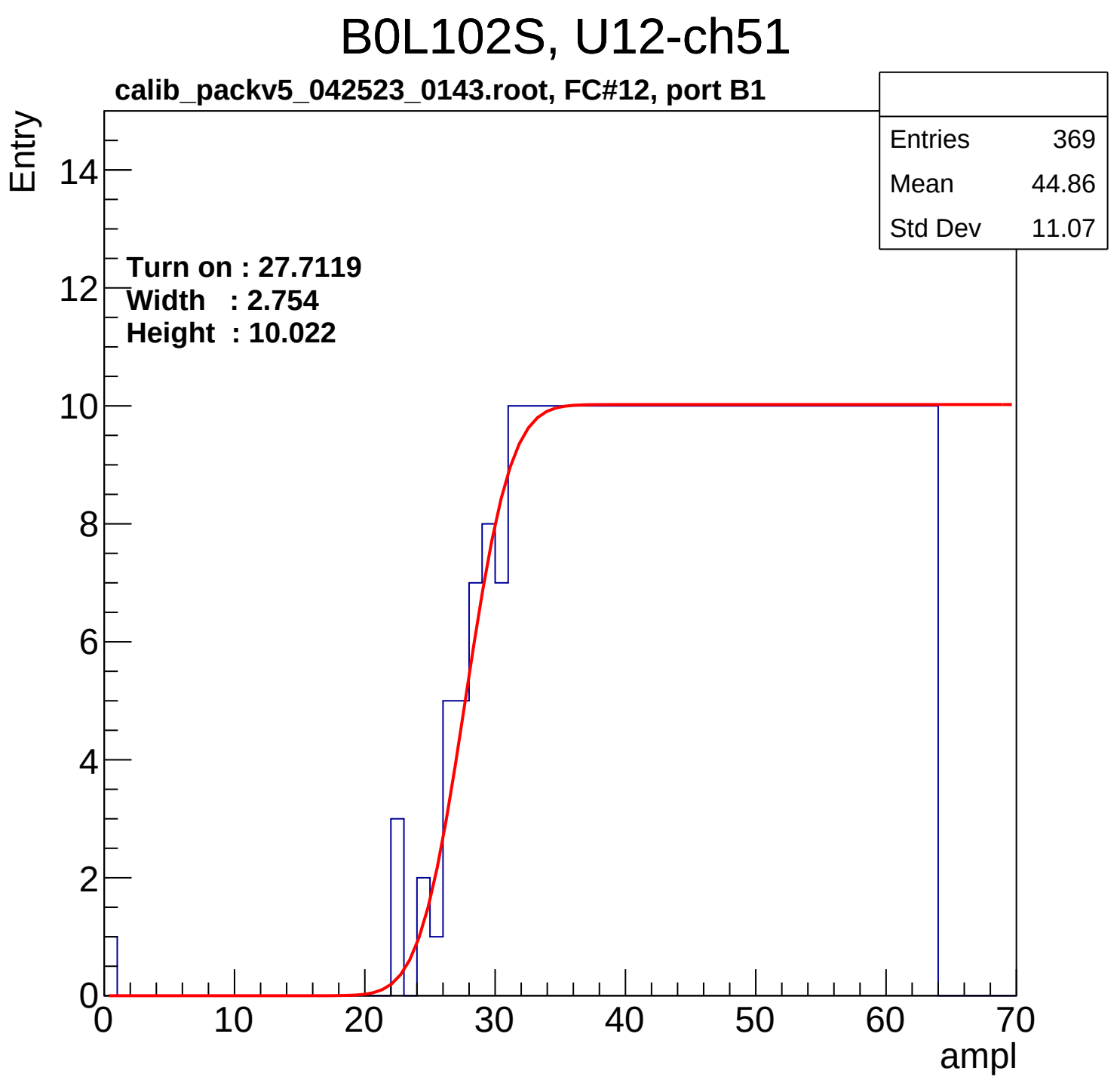
B0L102S, U12-ch51
calib_packv5_042523_0143.root, FC#12, port B1
Entries 369
Mean 44.86
Std Dev 11.07
Turn on : 27.7119
Width : 2.754
Height : 10.022
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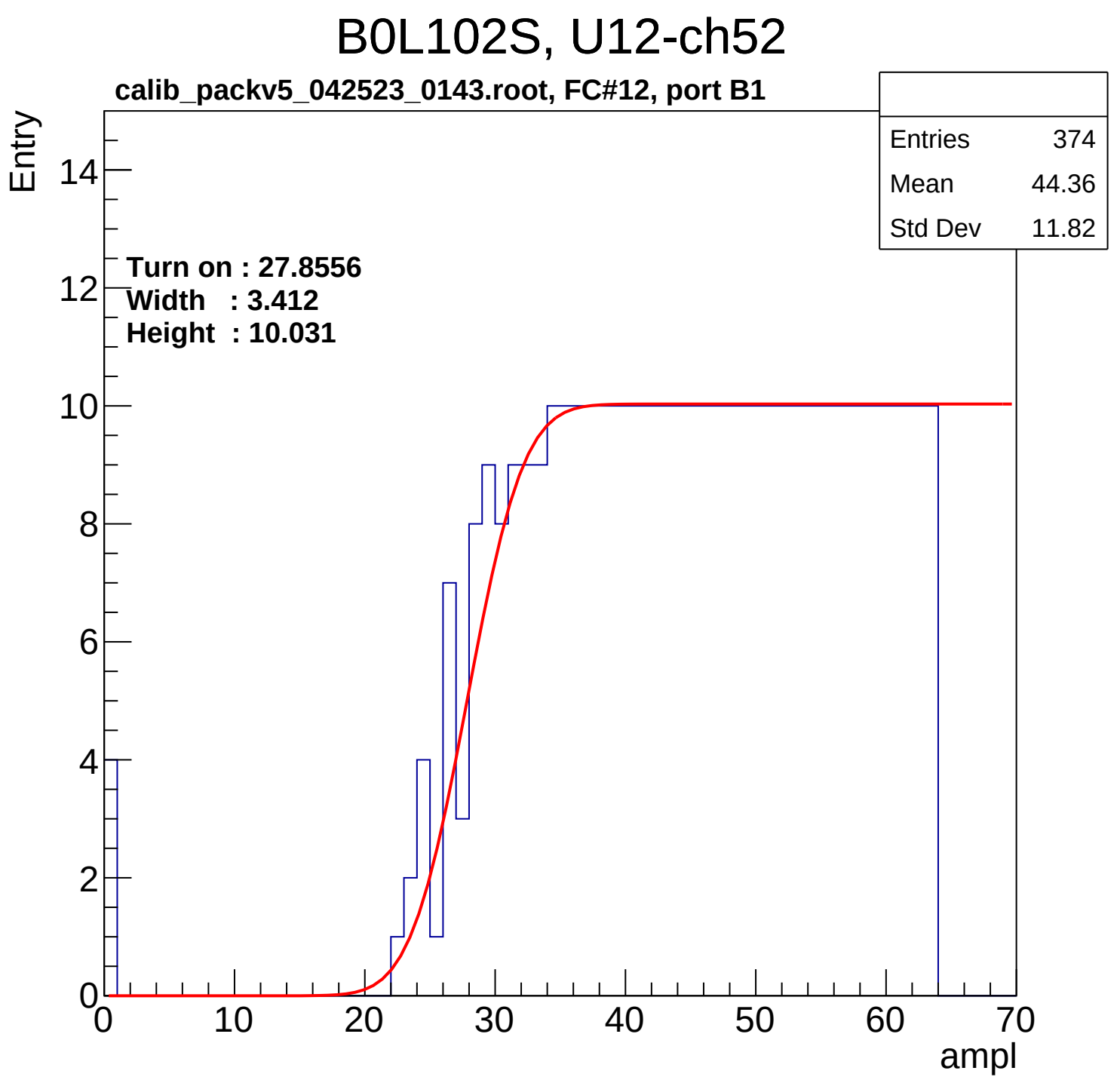
B0L102S, U12-ch52
calib_packv5_042523_0143.root, FC#12, port B1
Entries 374
Mean 44.36
Std Dev 11.82
Turn on : 27.8556
Width : 3.412
Height : 10.031
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ampl
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6
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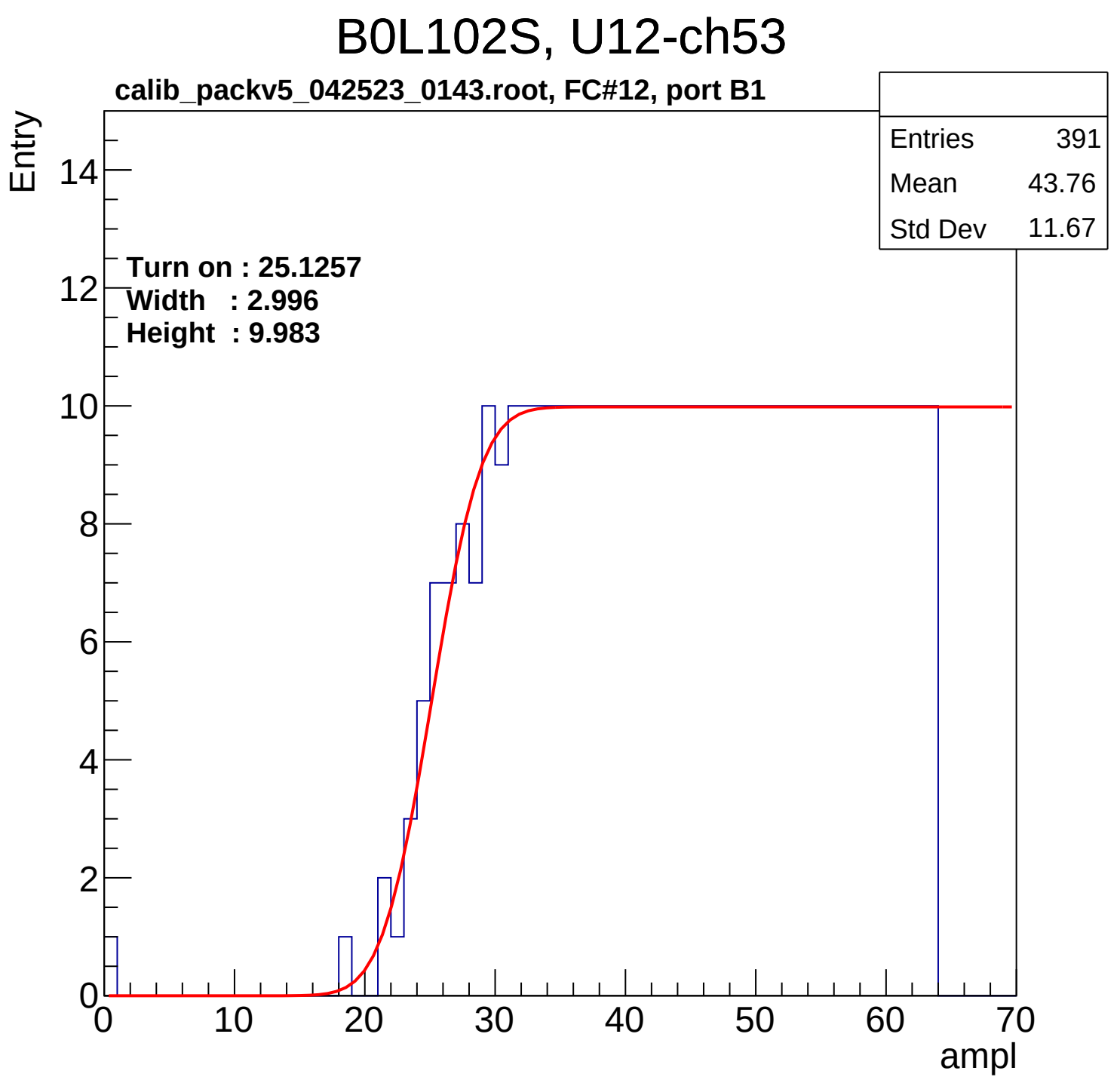
B0L102S, U12-ch53
calib_packv5_042523_0143.root, FC#12, port B1
Entries 391
Mean 43.76
Std Dev 11.67
Turn on : 25.1257
Width : 2.996
Height : 9.983
Entry
ampl
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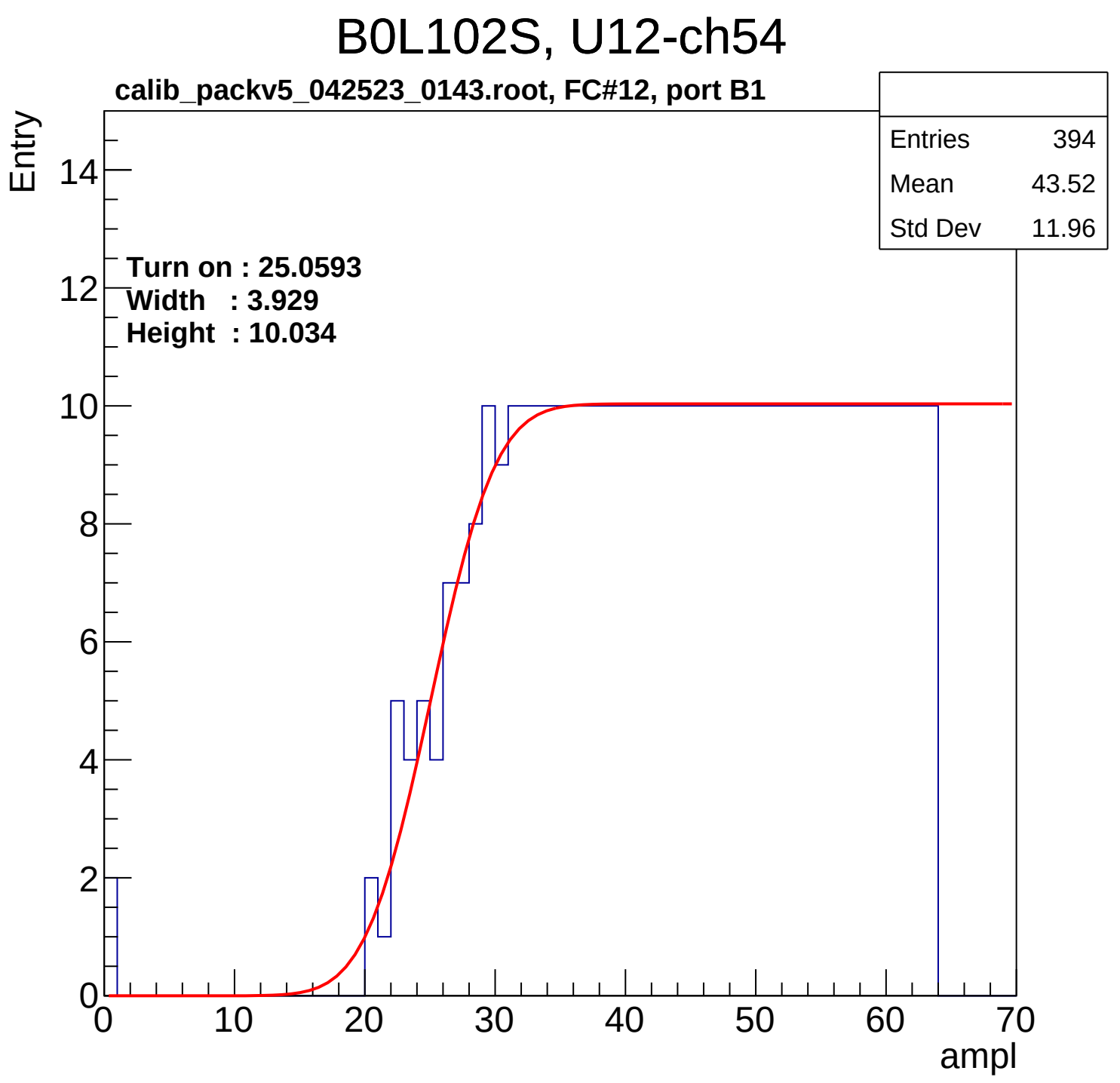
B0L102S, U12-ch54
calib_packv5_042523_0143.root, FC#12, port B1
Entries 394
Mean 43.52
Std Dev 11.96
Turn on : 25.0593
Width : 3.929
Height : 10.034
Entry
ampl
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6
8
10
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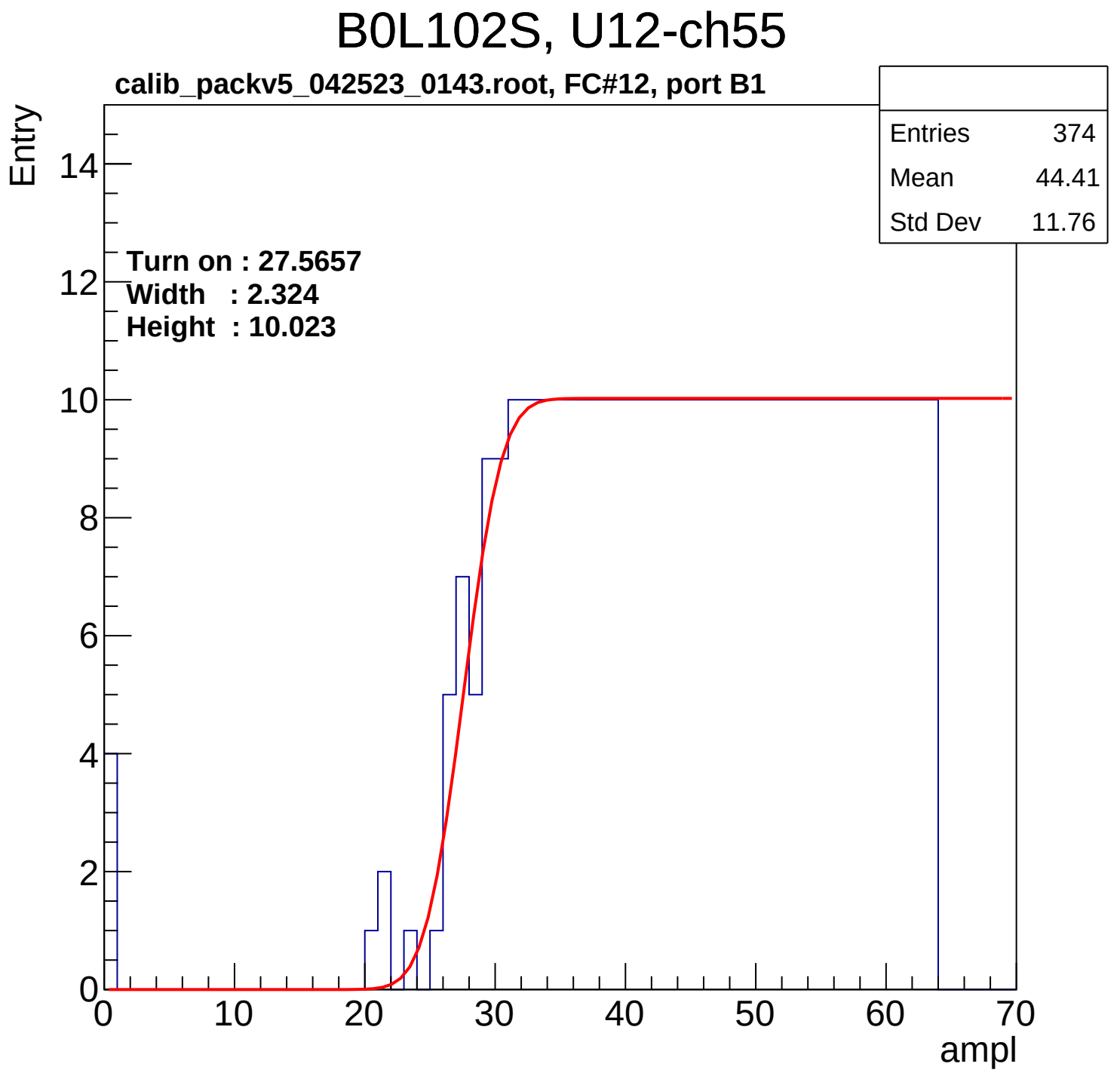
B0L102S, U12-ch55
calib_packv5_042523_0143.root, FC#12, port B1
Entries 374
Mean 44.41
Std Dev 11.76
Turn on : 27.5657
Width : 2.324
Height : 10.023
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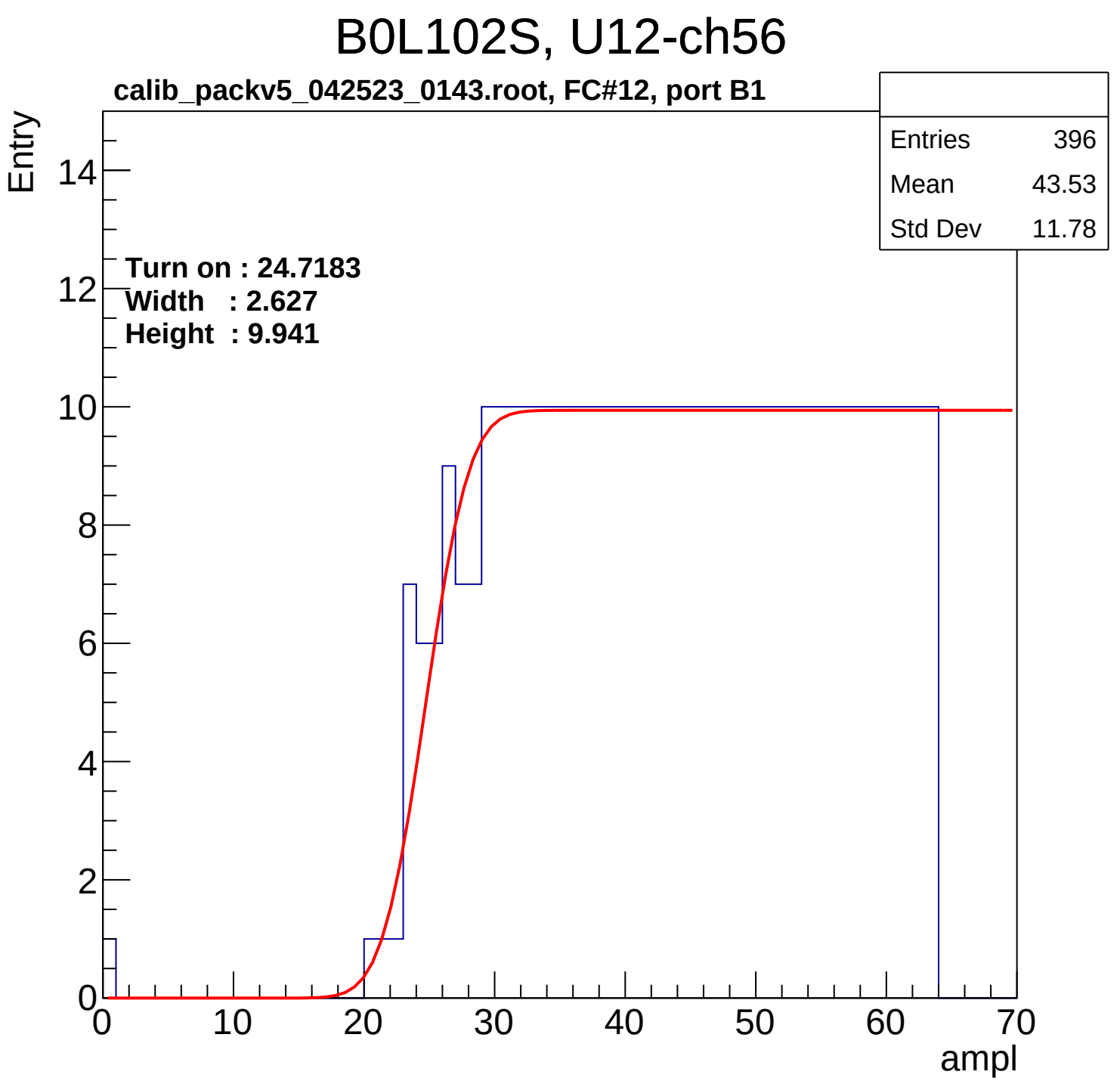
B0L102S, U12-ch56
calib_packv5_042523_0143.root, FC#12, port B1
Entries 396
Mean 43.53
Std Dev 11.78
Turn on : 24.7183
Width : 2.627
Height : 9.941
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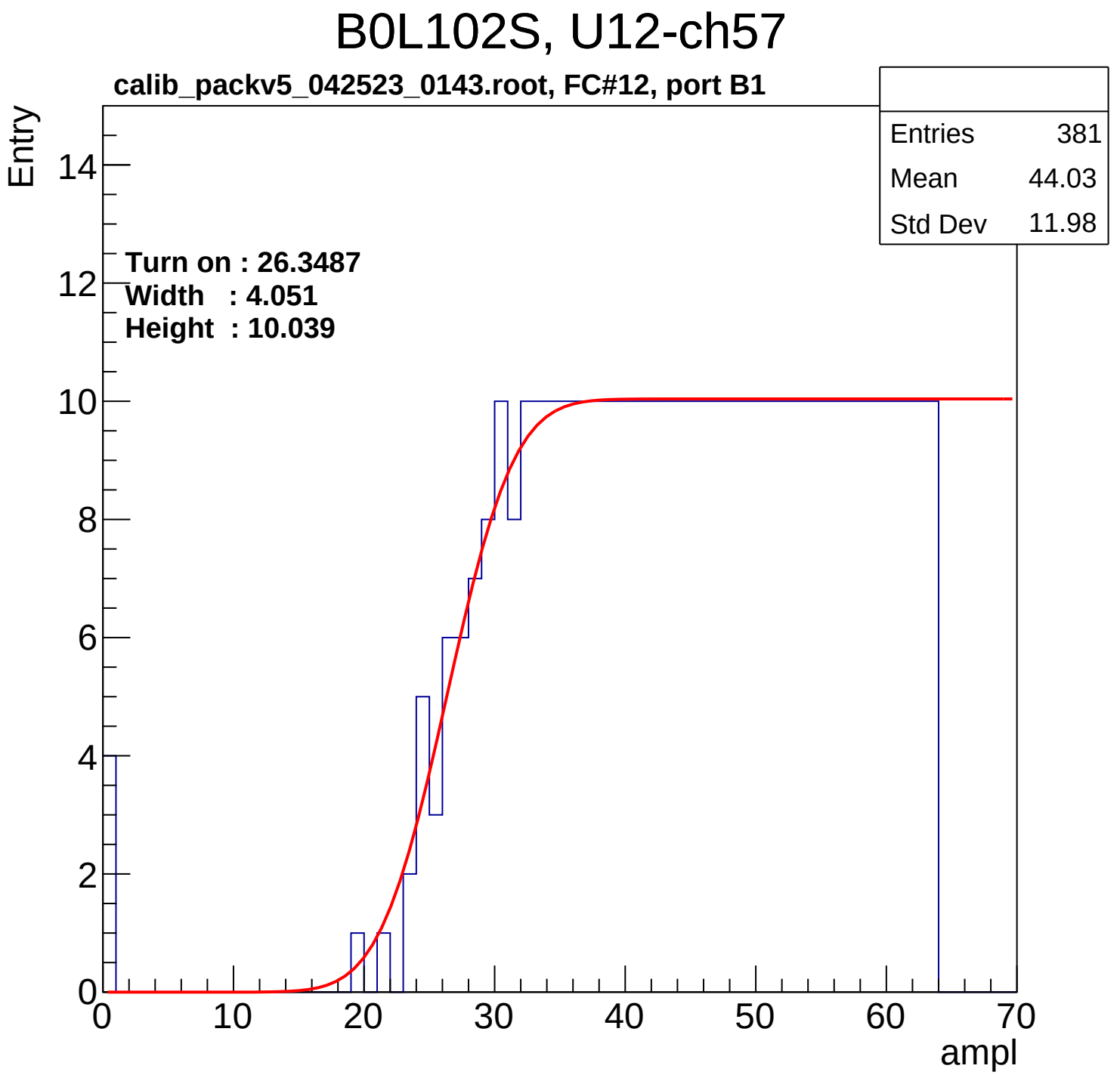
B0L102S, U12-ch57
calib_packv5_042523_0143.root, FC#12, port B1
Entries 381
Mean 44.03
Std Dev 11.98
Turn on : 26.3487
Width : 4.051
Height : 10.039
Entry
ampl
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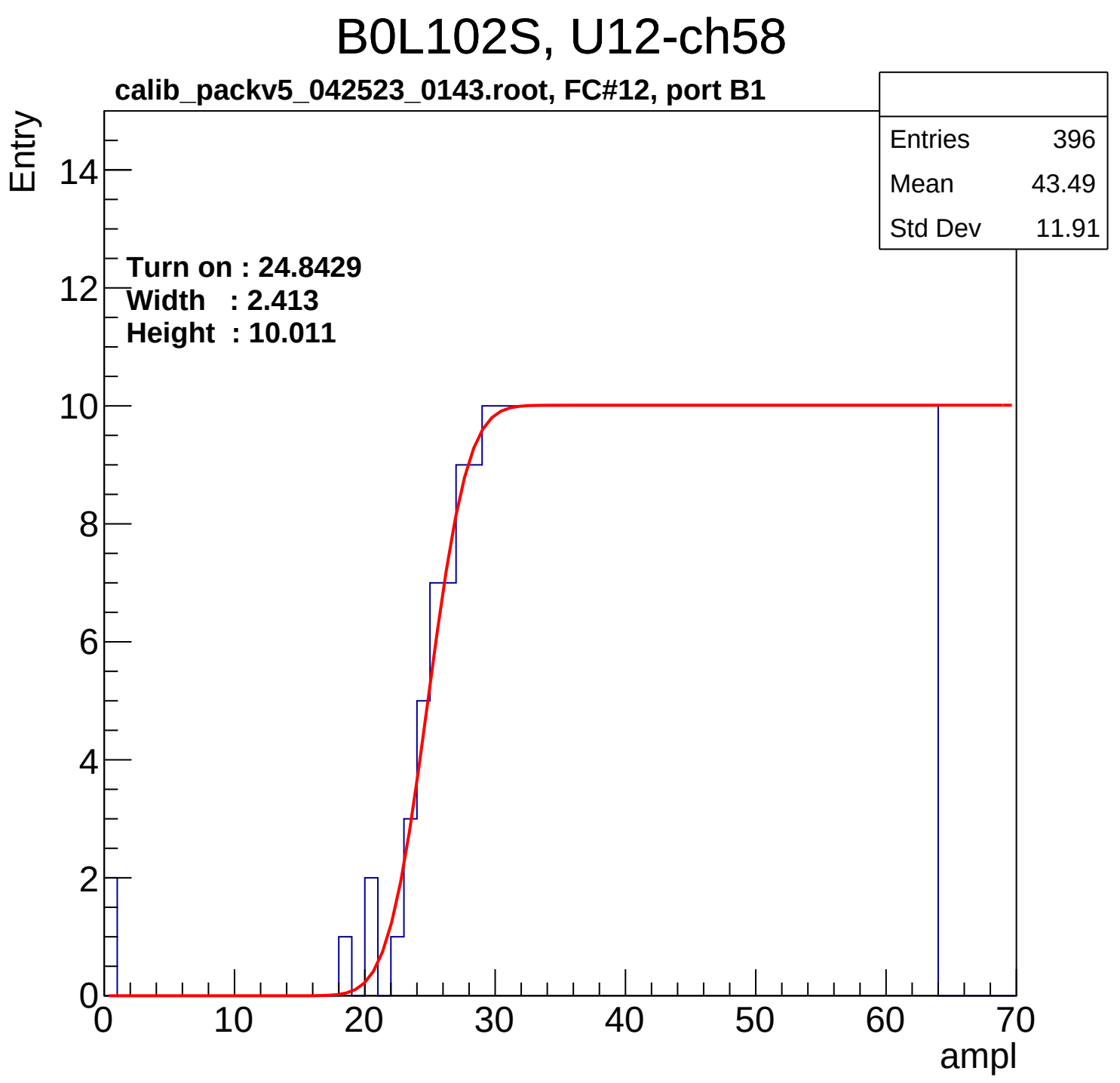
B0L102S, U12-ch58
calib_packv5_042523_0143.root, FC#12, port B1
Entries 396
Mean 43.49
Std Dev 11.91
Turn on : 24.8429
Width : 2.413
Height : 10.011
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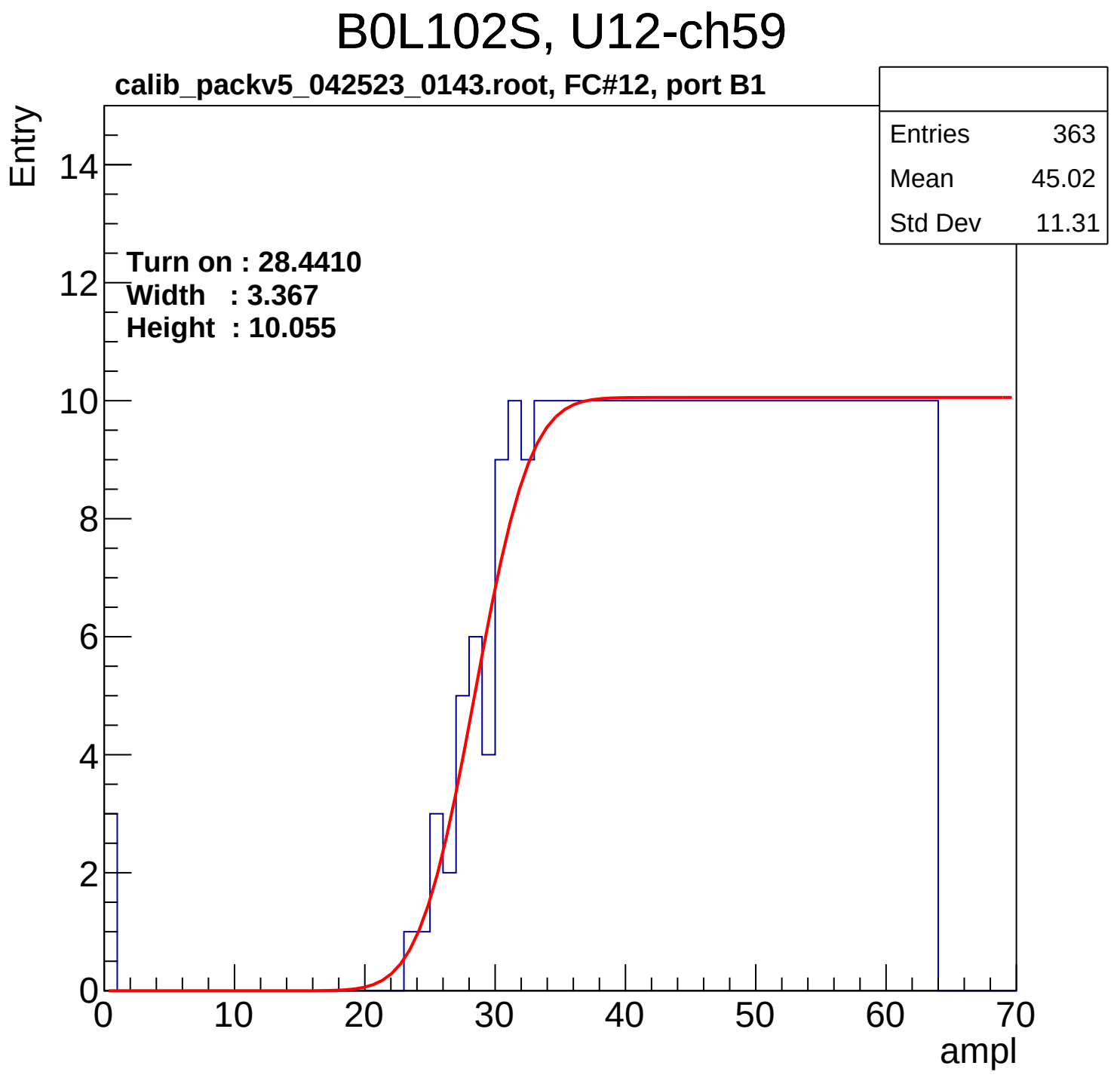
B0L102S, U12-ch59
calib_packv5_042523_0143.root, FC#12, port B1
Entries 363
Mean 45.02
Std Dev 11.31
Turn on : 28.4410
Width : 3.367
Height : 10.055
Entry
ampl
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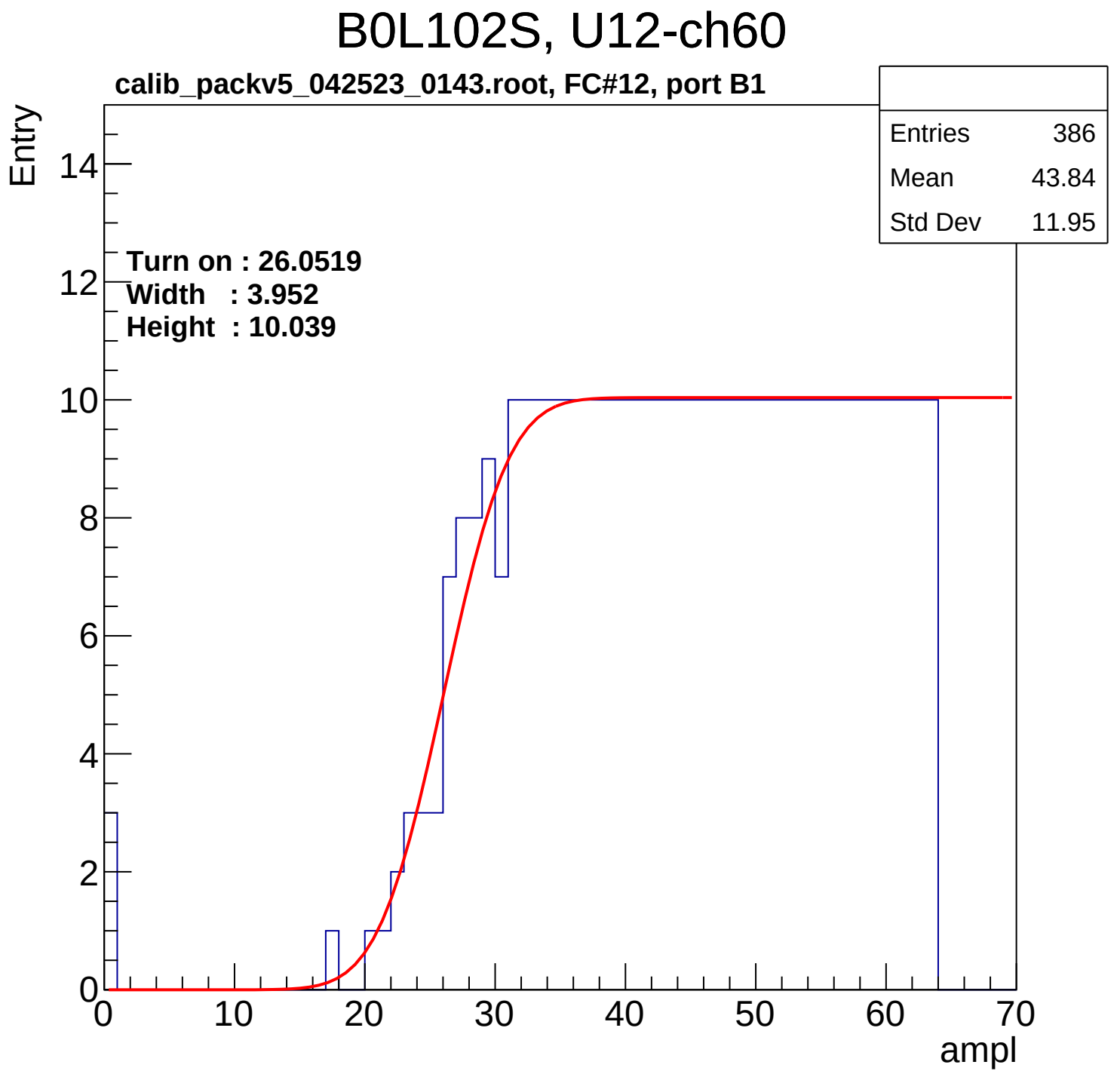
B0L102S, U12-ch60
calib_packv5_042523_0143.root, FC#12, port B1
Entries 386
Mean 43.84
Std Dev 11.95
Turn on : 26.0519
Width : 3.952
Height : 10.039
Entry
ampl
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8
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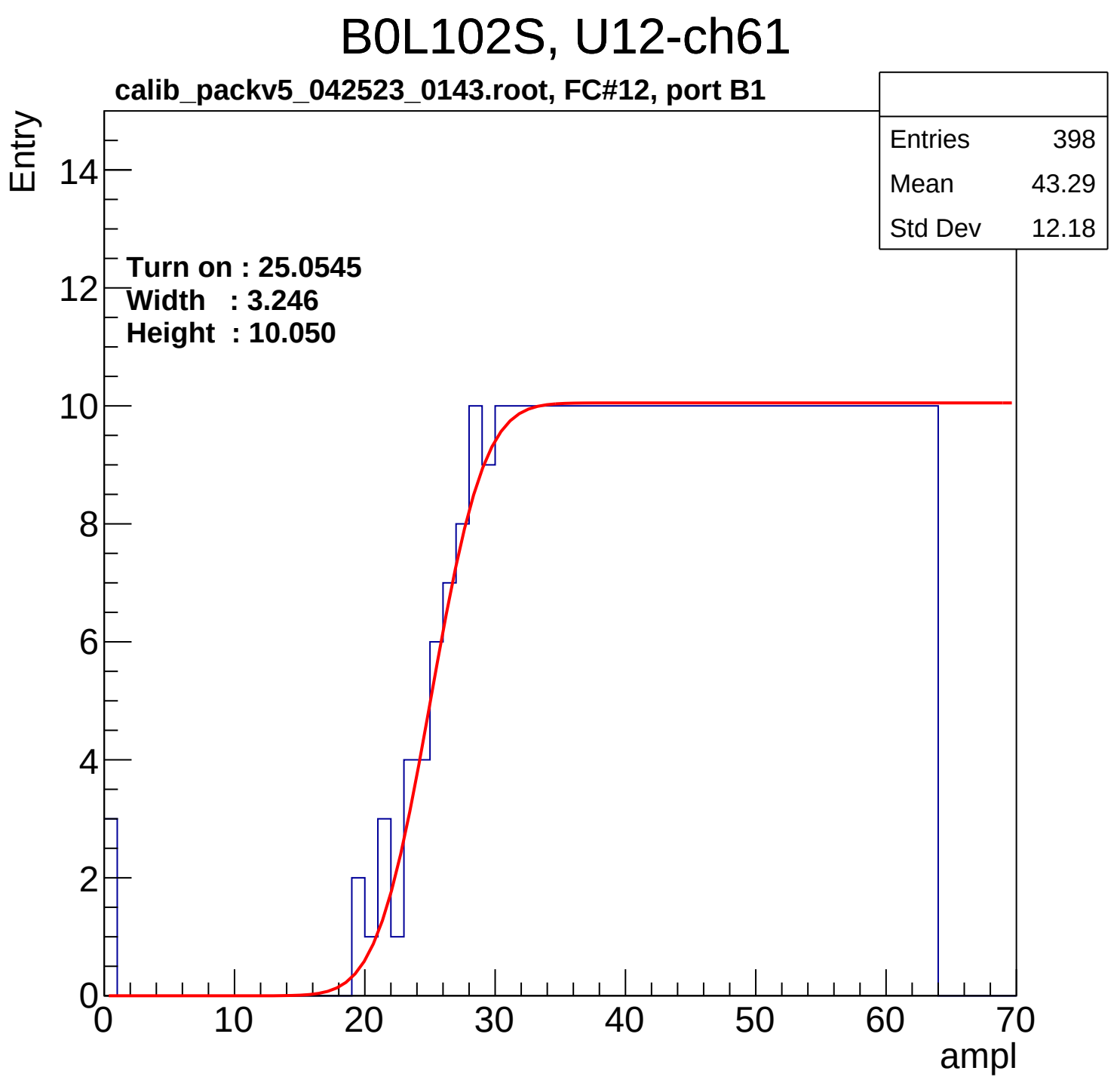
B0L102S, U12-ch61
calib_packv5_042523_0143.root, FC#12, port B1
Entries 398
Mean 43.29
Std Dev 12.18
Turn on : 25.0545
Width : 3.246
Height : 10.050
Entry
ampl
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2
4
6
8
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12
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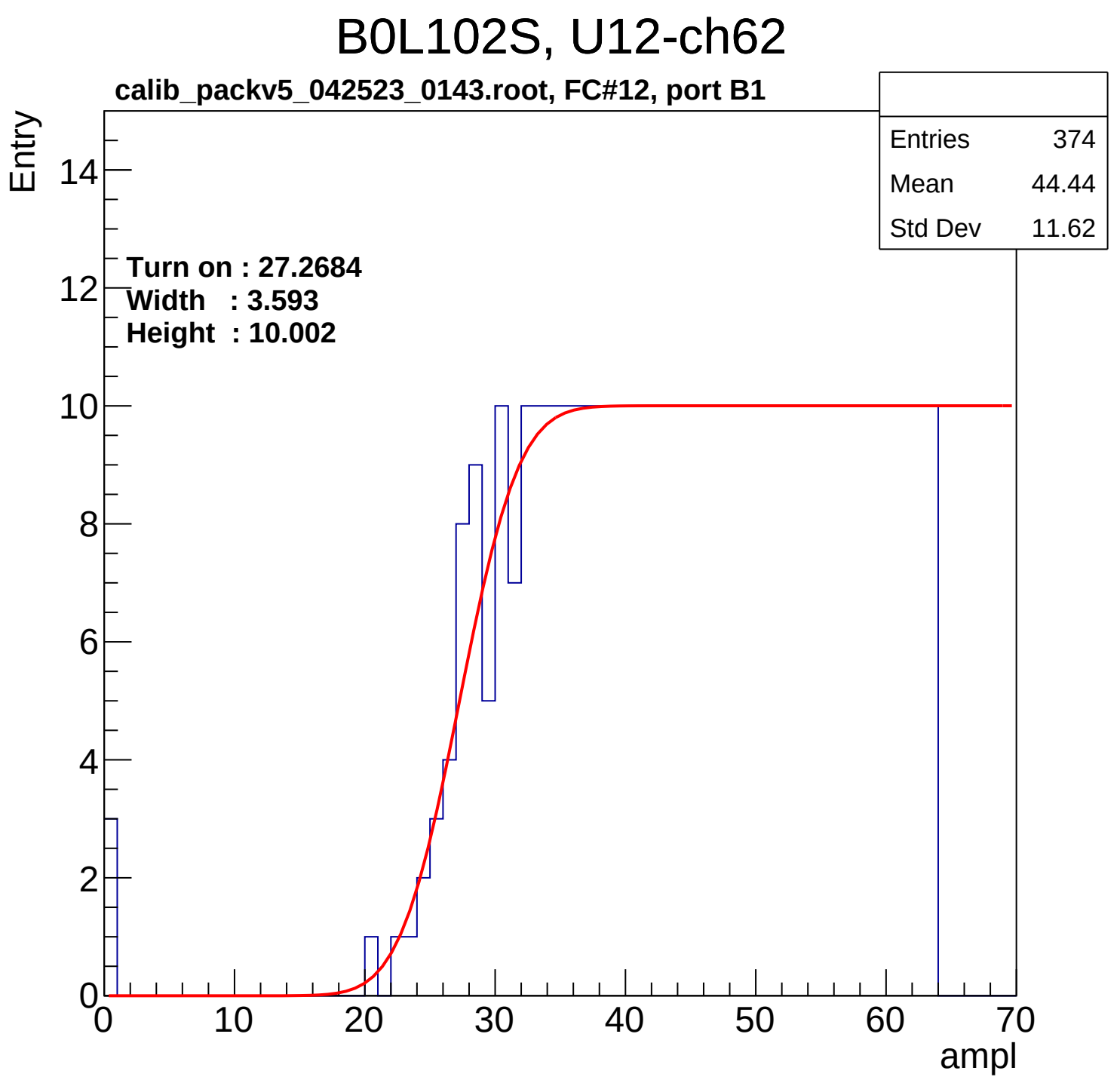
B0L102S, U12-ch62
calib_packv5_042523_0143.root, FC#12, port B1
Entries 374
Mean 44.44
Std Dev 11.62
Turn on : 27.2684
Width : 3.593
Height : 10.002
Entry
ampl
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2
4
6
8
10
12
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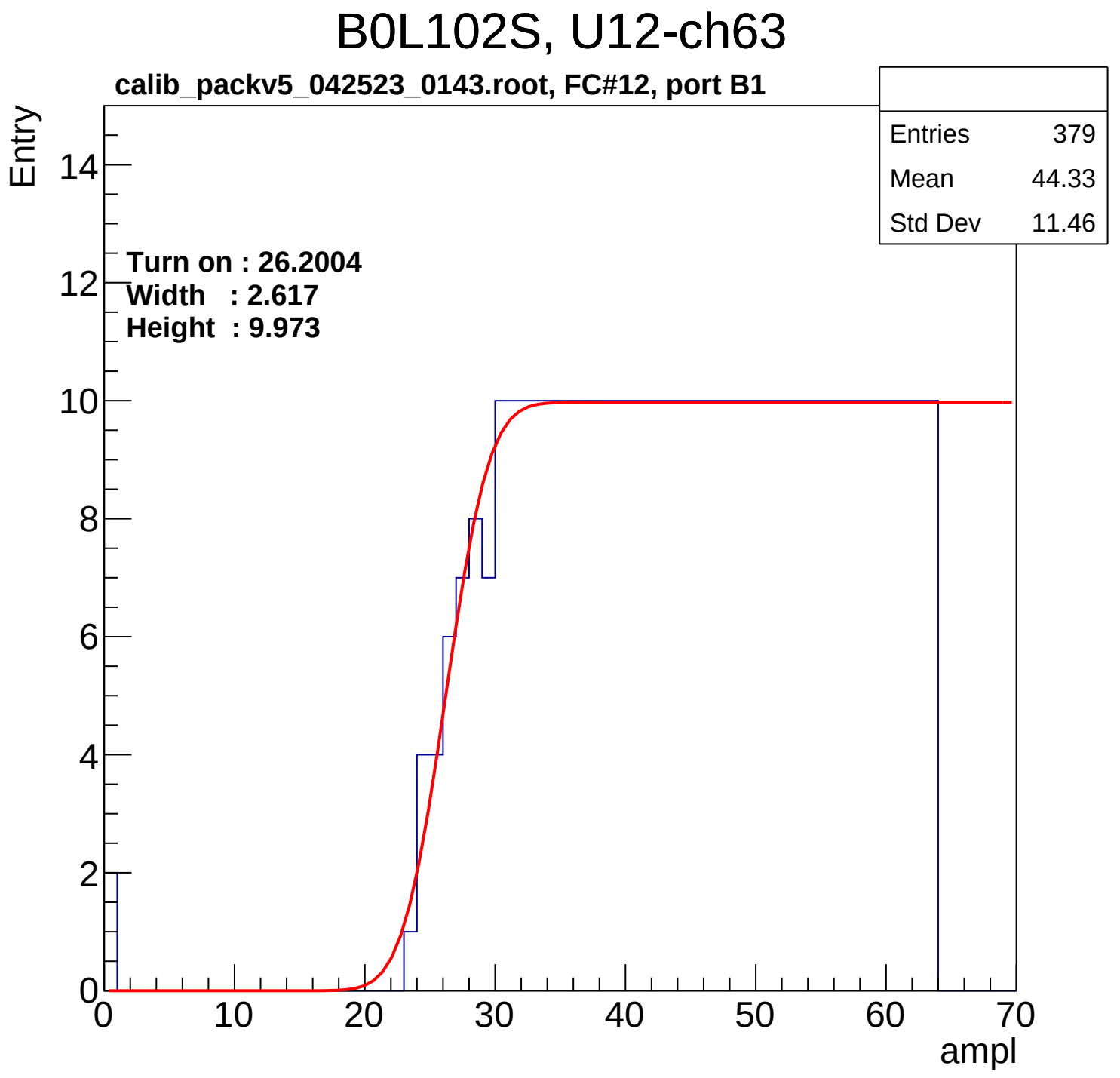
B0L102S, U12-ch63
calib_packv5_042523_0143.root, FC#12, port B1
Entries 379
Mean 44.33
Std Dev 11.46
Turn on : 26.2004
Width : 2.617
Height : 9.973
Entry
ampl
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4
6
8
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12
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0
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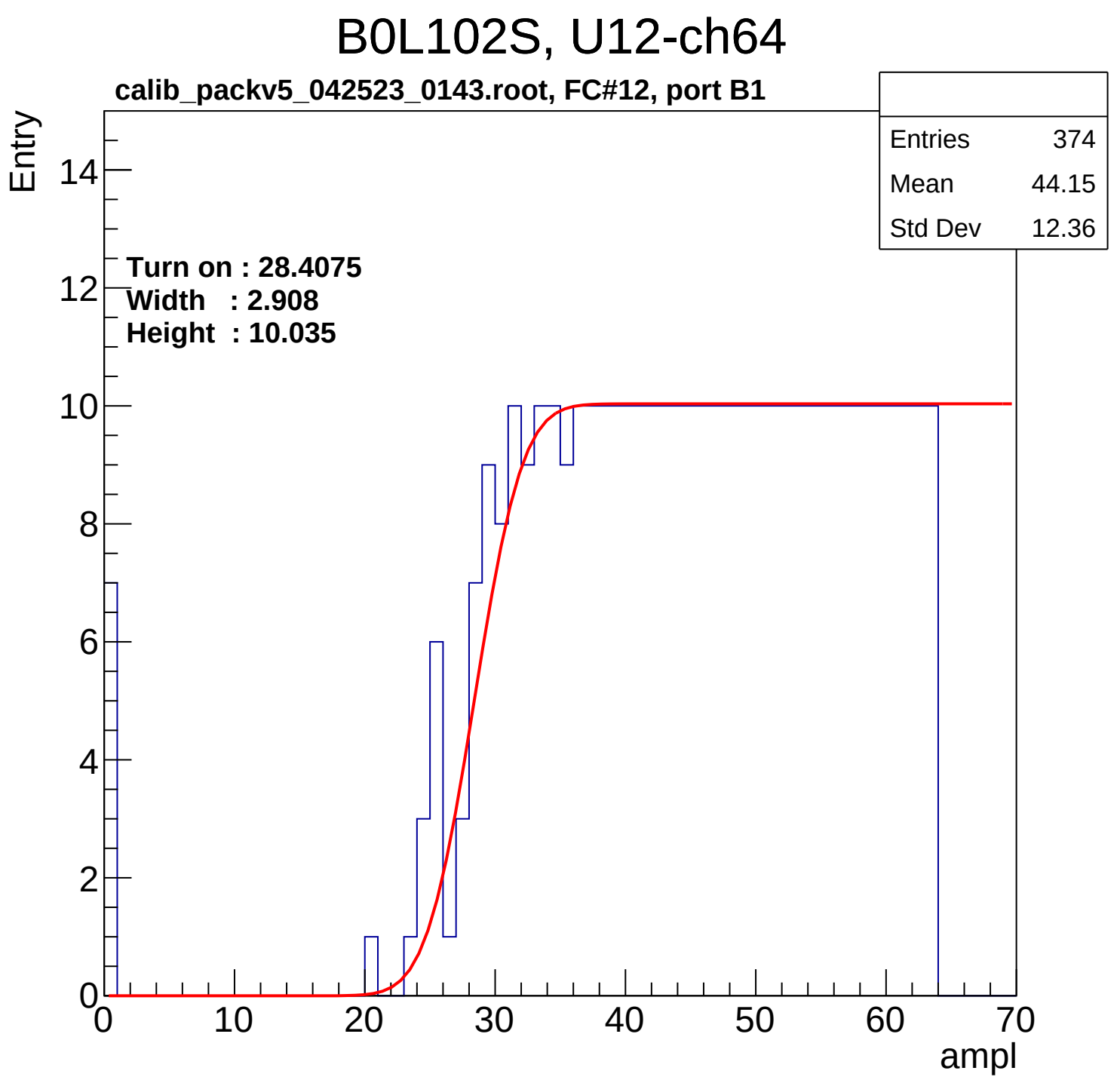
B0L102S, U12-ch64
calib_packv5_042523_0143.root, FC#12, port B1
Entries 374
Mean 44.15
Std Dev 12.36
Turn on : 28.4075
Width : 2.908
Height : 10.035
Entry
ampl
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2
4
6
8
10
12
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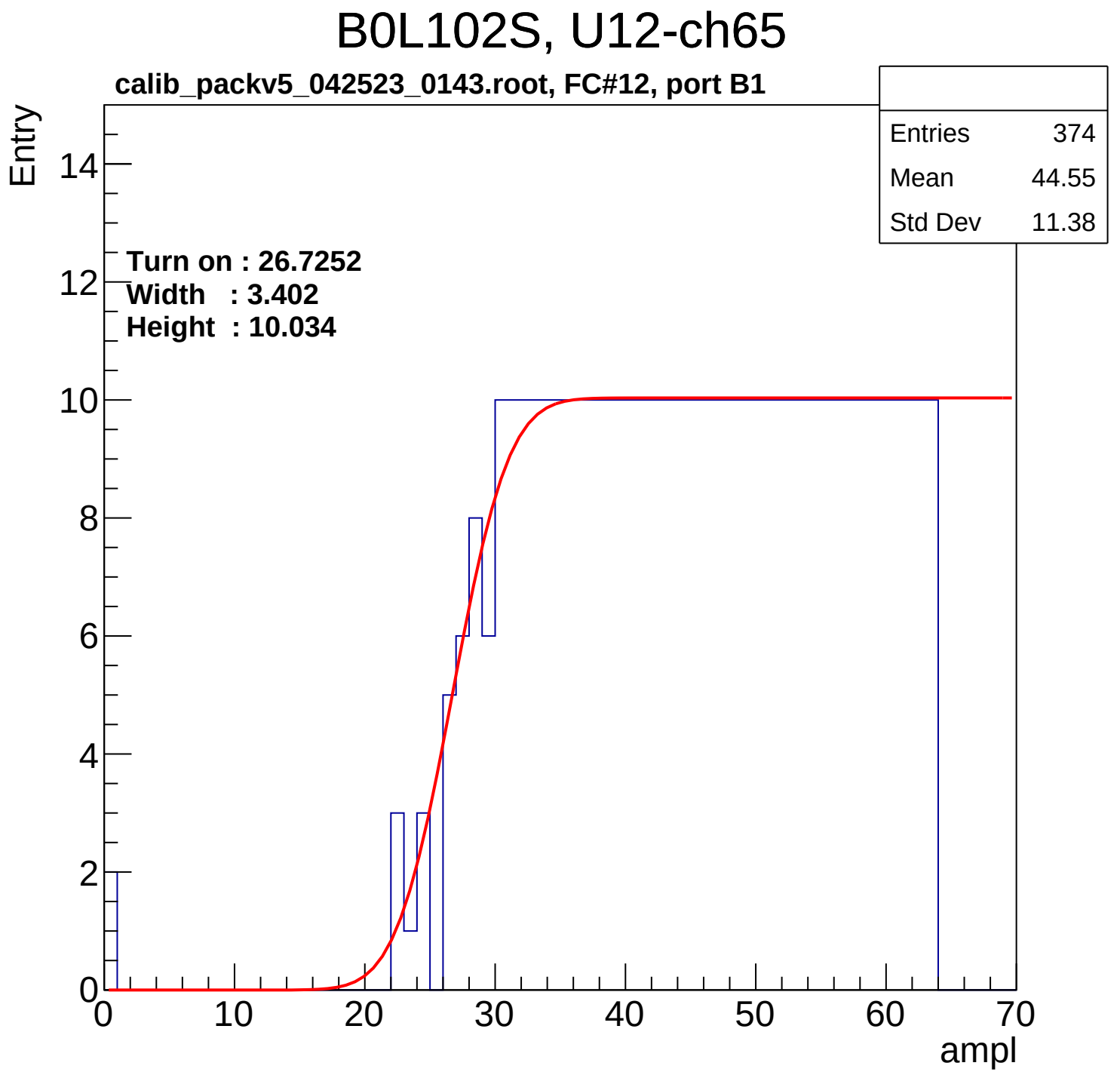
B0L102S, U12-ch65
calib_packv5_042523_0143.root, FC#12, port B1
Entries 374
Mean 44.55
Std Dev 11.38
Turn on : 26.7252
Width : 3.402
Height : 10.034
Entry
ampl
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2
4
6
8
10
12
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60
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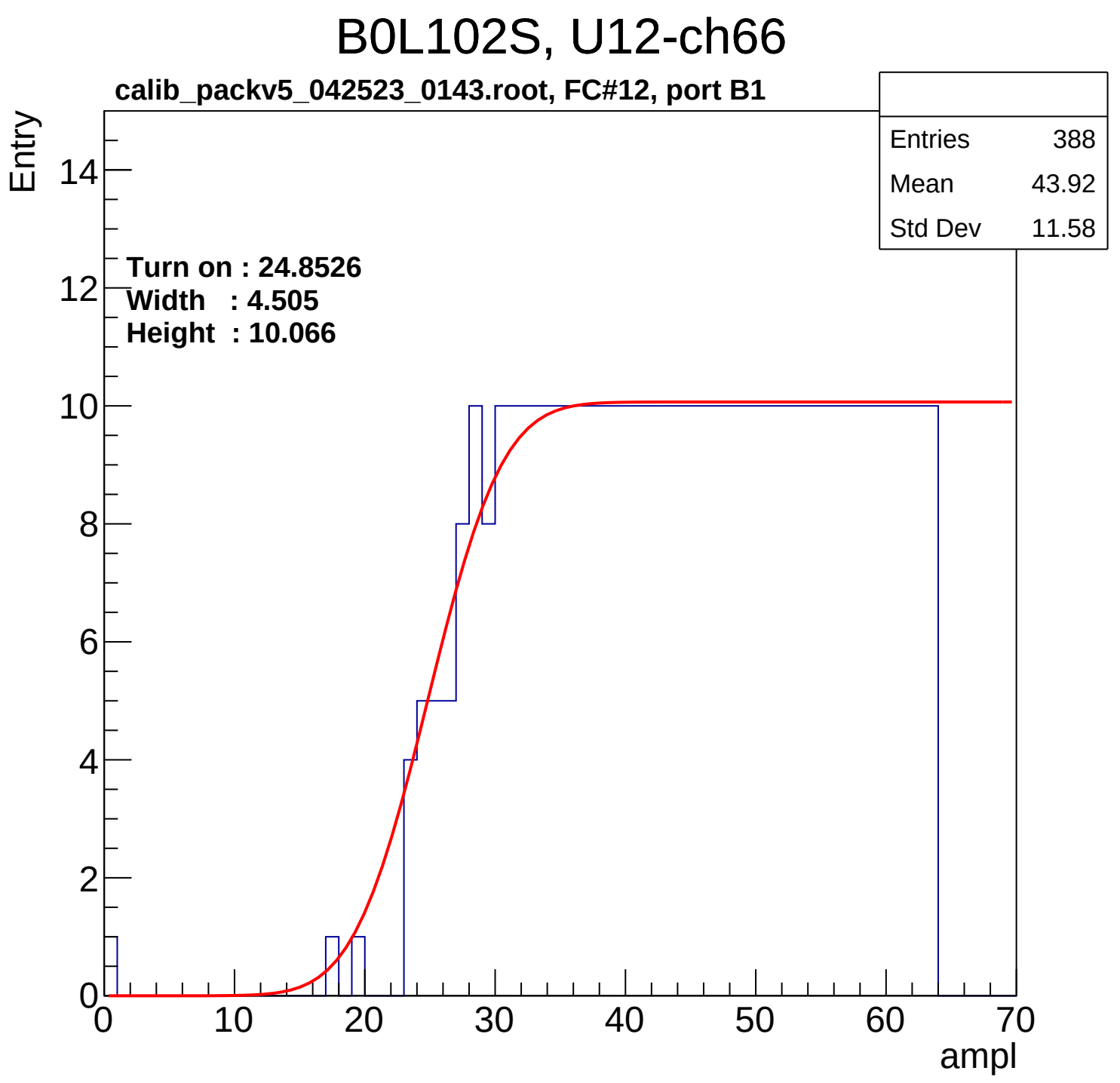
B0L102S, U12-ch66
calib_packv5_042523_0143.root, FC#12, port B1
Entries 388
Mean 43.92
Std Dev 11.58
Turn on : 24.8526
Width : 4.505
Height : 10.066
Entry
ampl
0
2
4
6
8
10
12
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0
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60
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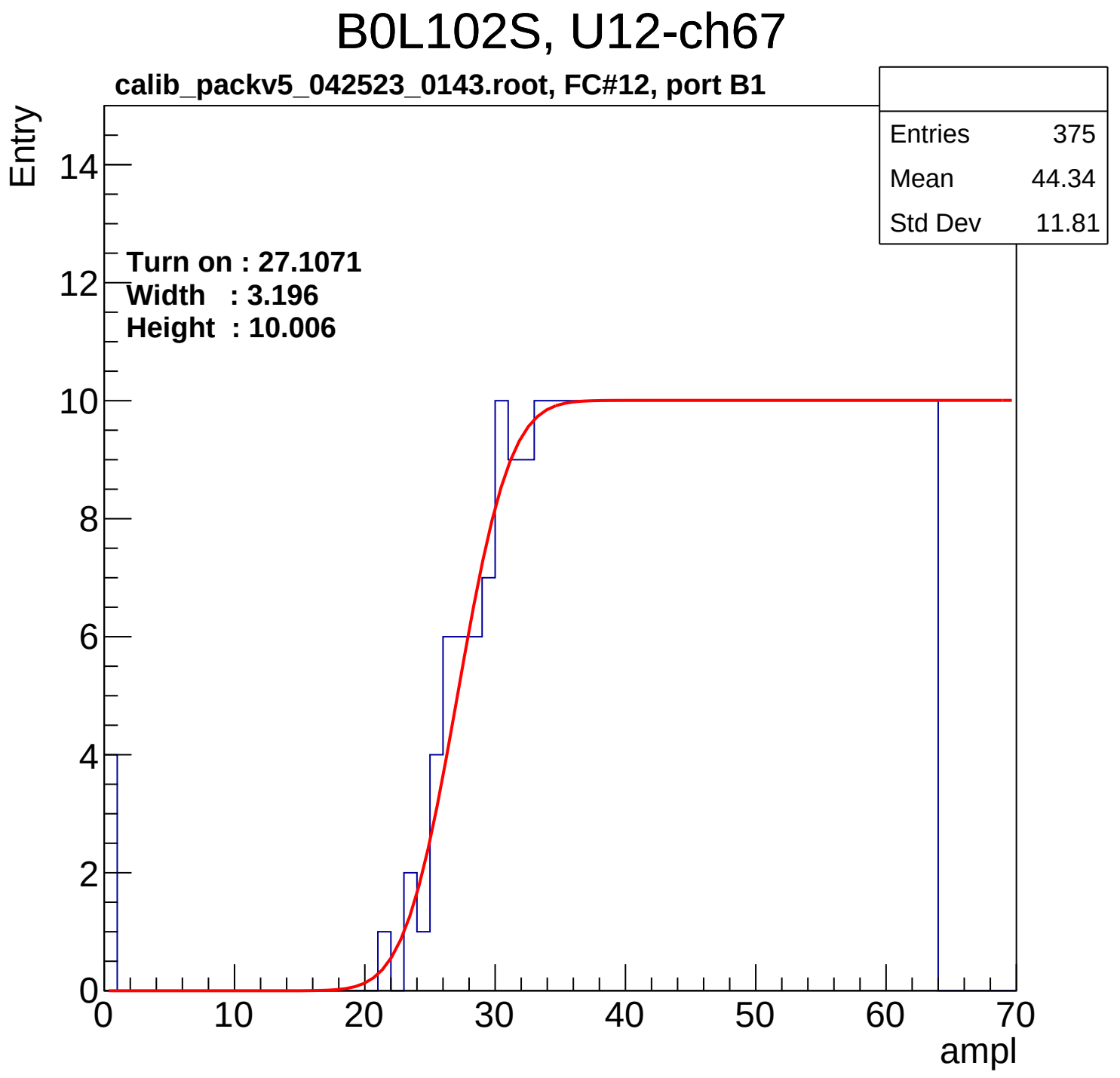
B0L102S, U12-ch67
calib_packv5_042523_0143.root, FC#12, port B1
Entries 375
Mean 44.34
Std Dev 11.81
Turn on : 27.1071
Width : 3.196
Height : 10.006
Entry
ampl
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6
8
10
12
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0
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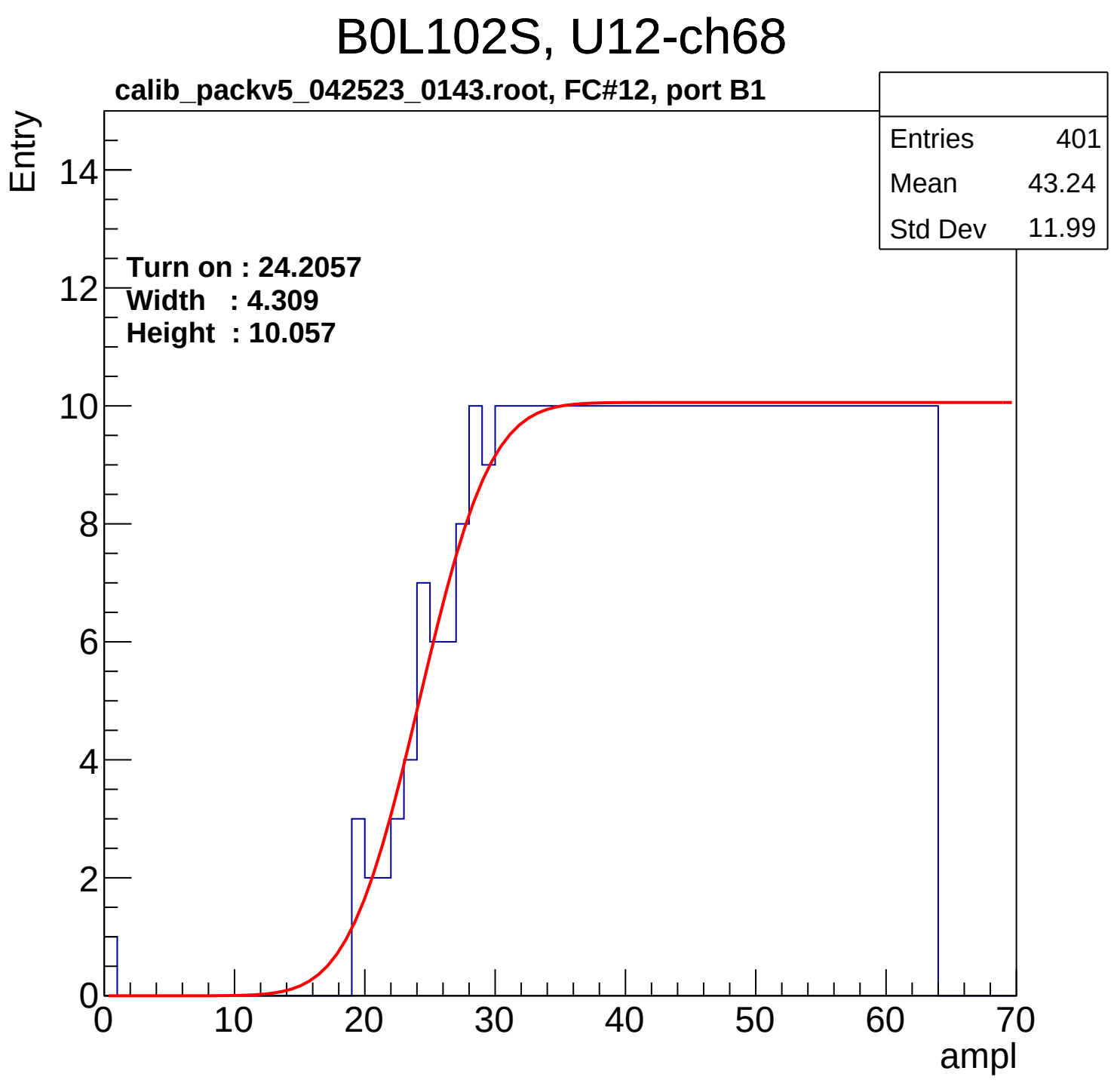
B0L102S, U12-ch68
calib_packv5_042523_0143.root, FC#12, port B1
Entries 401
Mean 43.24
Std Dev 11.99
Turn on : 24.2057
Width : 4.309
Height : 10.057
Entry
ampl
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6
8
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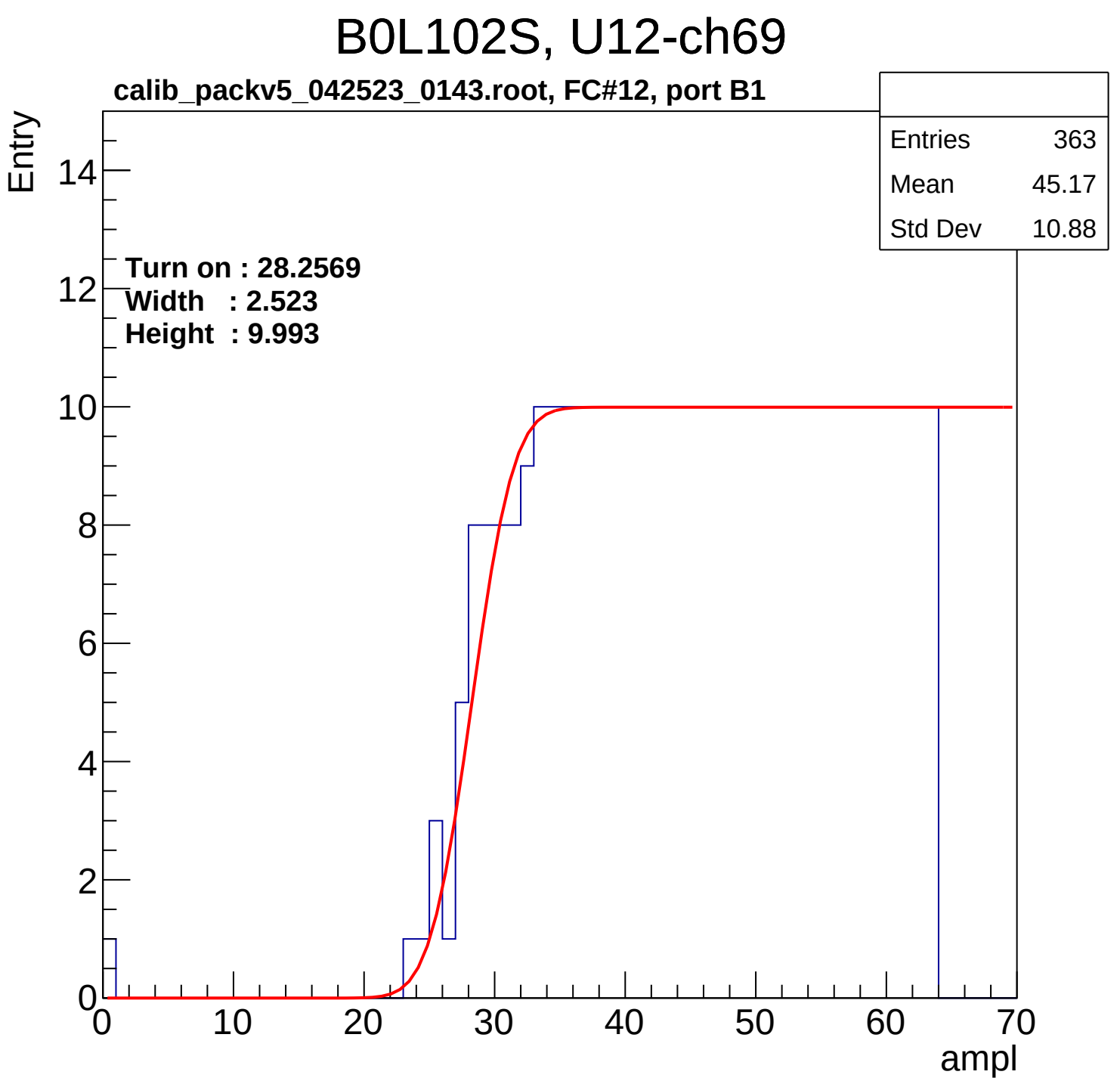
B0L102S, U12-ch69
calib_packv5_042523_0143.root, FC#12, port B1
Entries 363
Mean 45.17
Std Dev 10.88
Turn on : 28.2569
Width : 2.523
Height : 9.993
Entry
ampl
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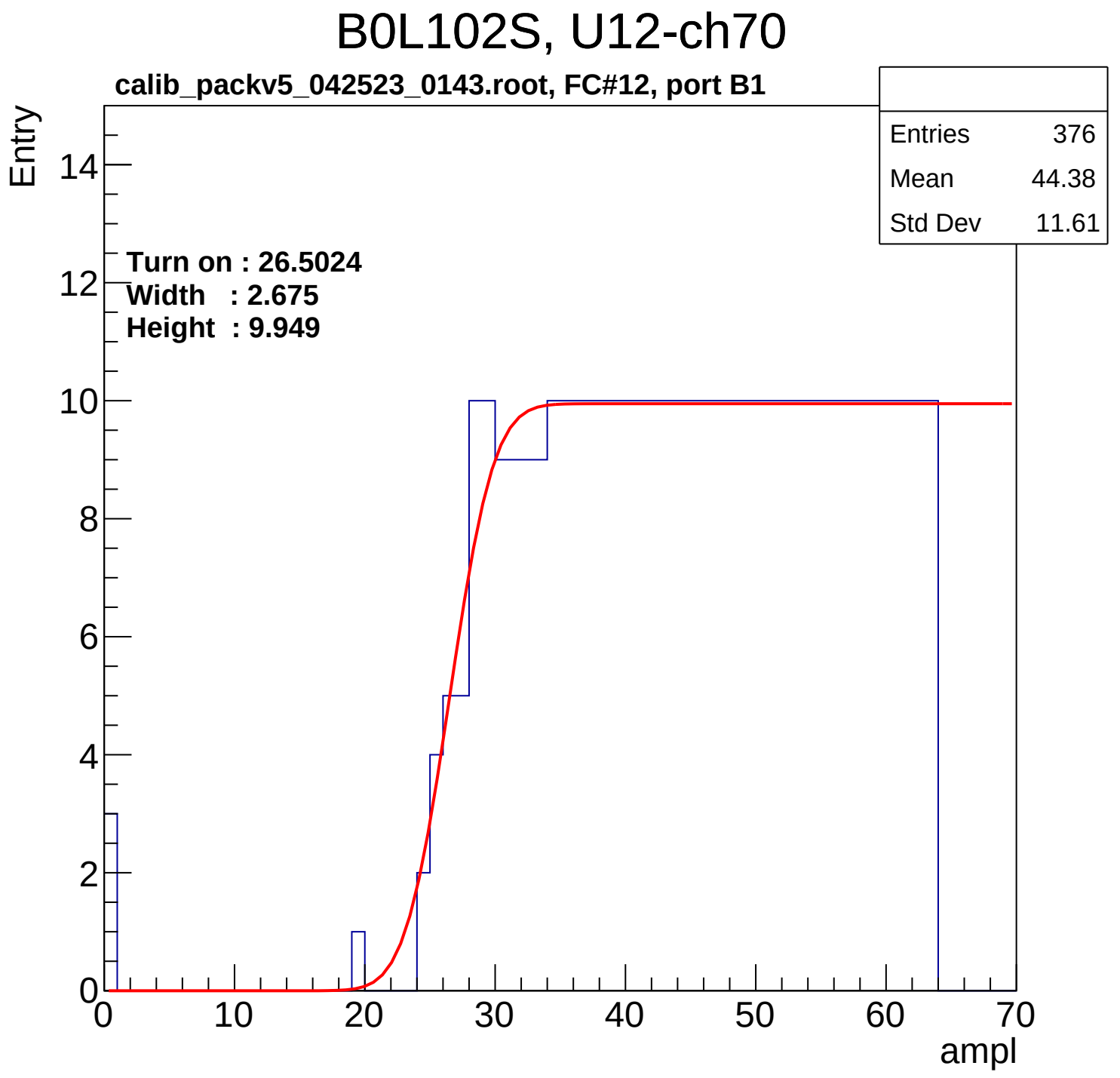
B0L102S, U12-ch70
calib_packv5_042523_0143.root, FC#12, port B1
Entries 376
Mean 44.38
Std Dev 11.61
Turn on : 26.5024
Width : 2.675
Height : 9.949
Entry
ampl
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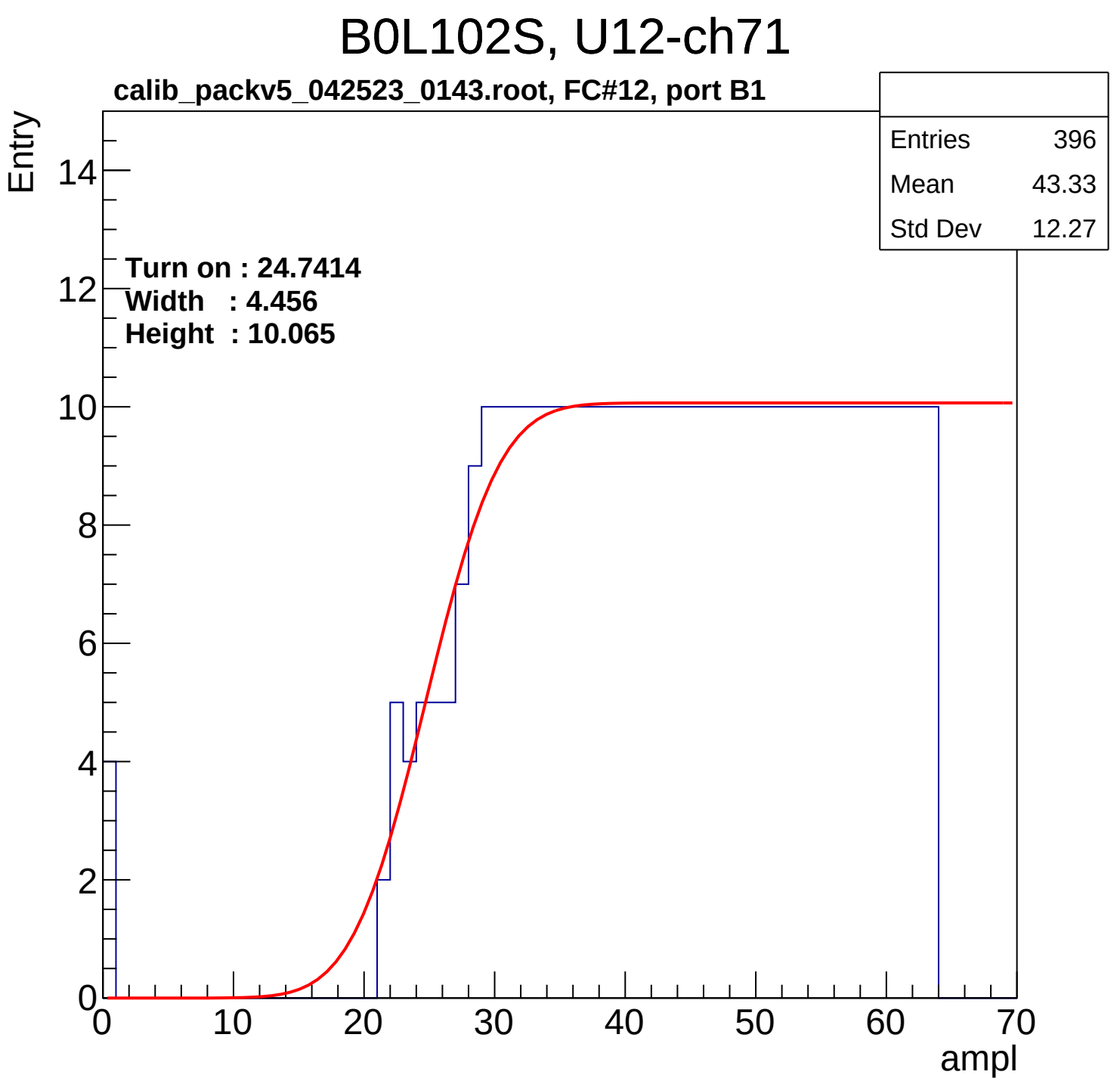
B0L102S, U12-ch71
calib_packv5_042523_0143.root, FC#12, port B1
Entries 396
Mean 43.33
Std Dev 12.27
Turn on : 24.7414
Width : 4.456
Height : 10.065
Entry
ampl
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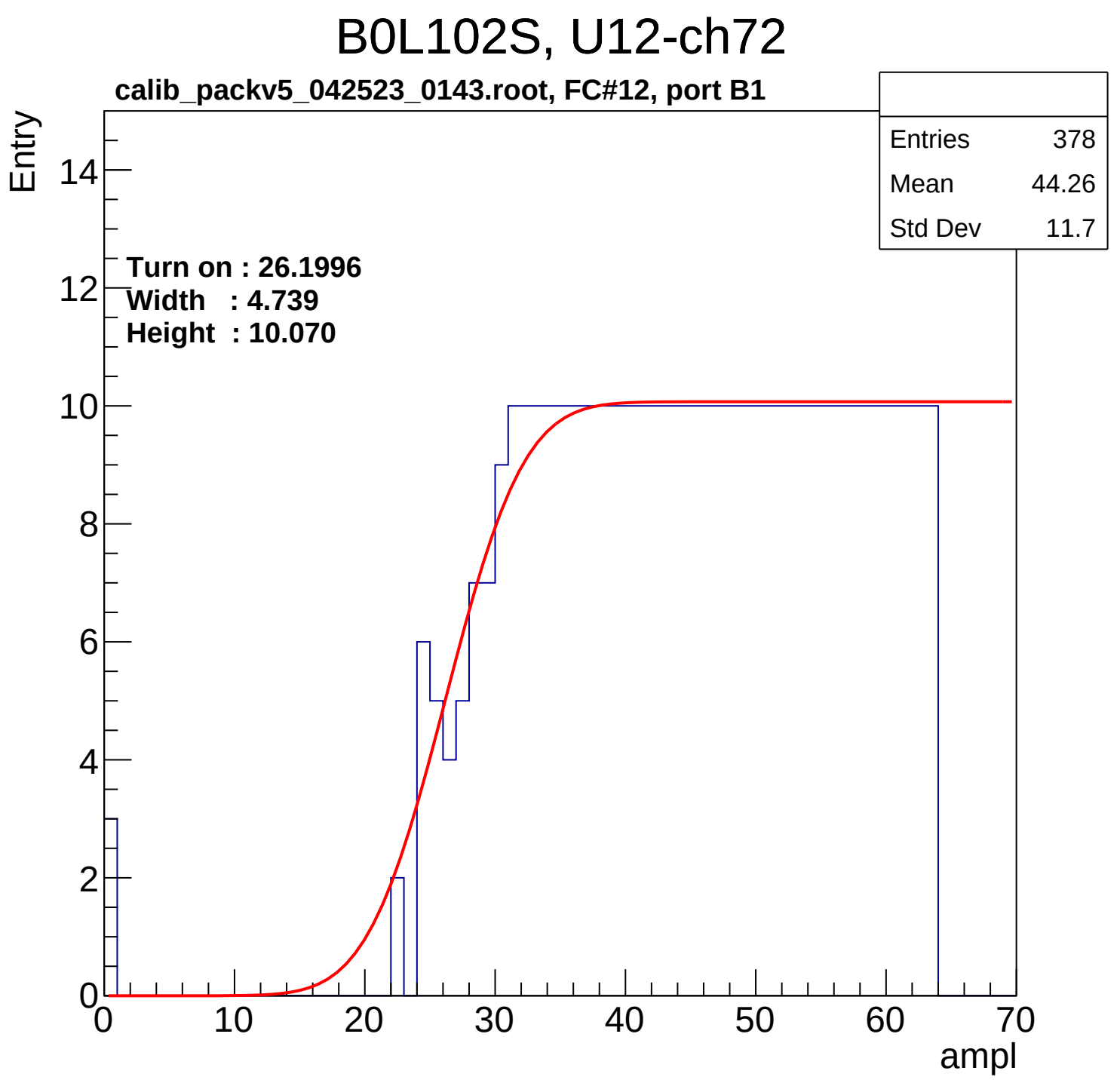
B0L102S, U12-ch72
calib_packv5_042523_0143.root, FC#12, port B1
Entries 378
Mean 44.26
Std Dev 11.7
Turn on : 26.1996
Width : 4.739
Height : 10.070
Entry
ampl
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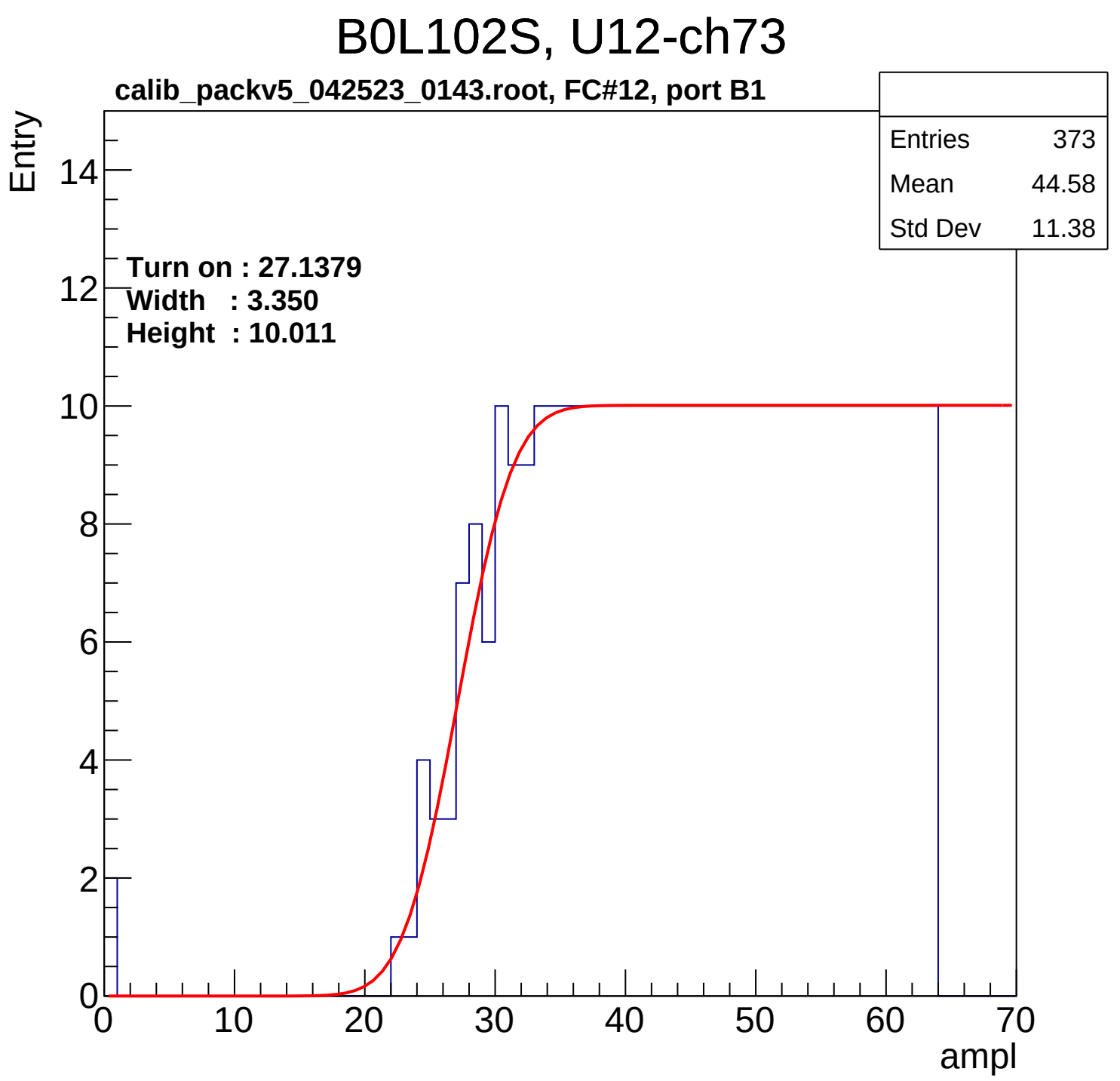
B0L102S, U12-ch73
calib_packv5_042523_0143.root, FC#12, port B1
Entries 373
Mean 44.58
Std Dev 11.38
Turn on : 27.1379
Width : 3.350
Height : 10.011
Entry
ampl
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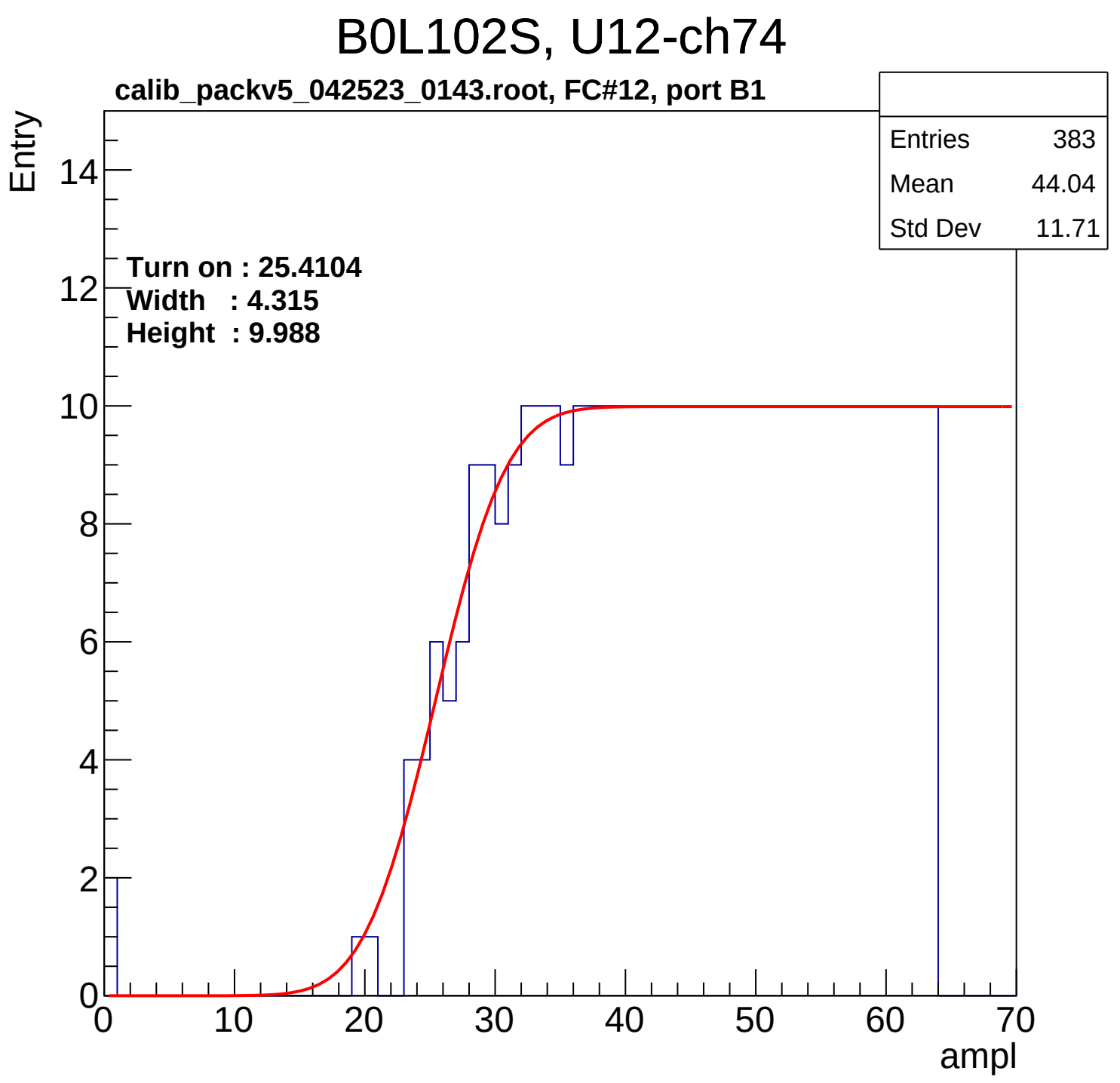
B0L102S, U12-ch74
calib_packv5_042523_0143.root, FC#12, port B1
Entries 383
Mean 44.04
Std Dev 11.71
Turn on : 25.4104
Width : 4.315
Height : 9.988
Entry
ampl
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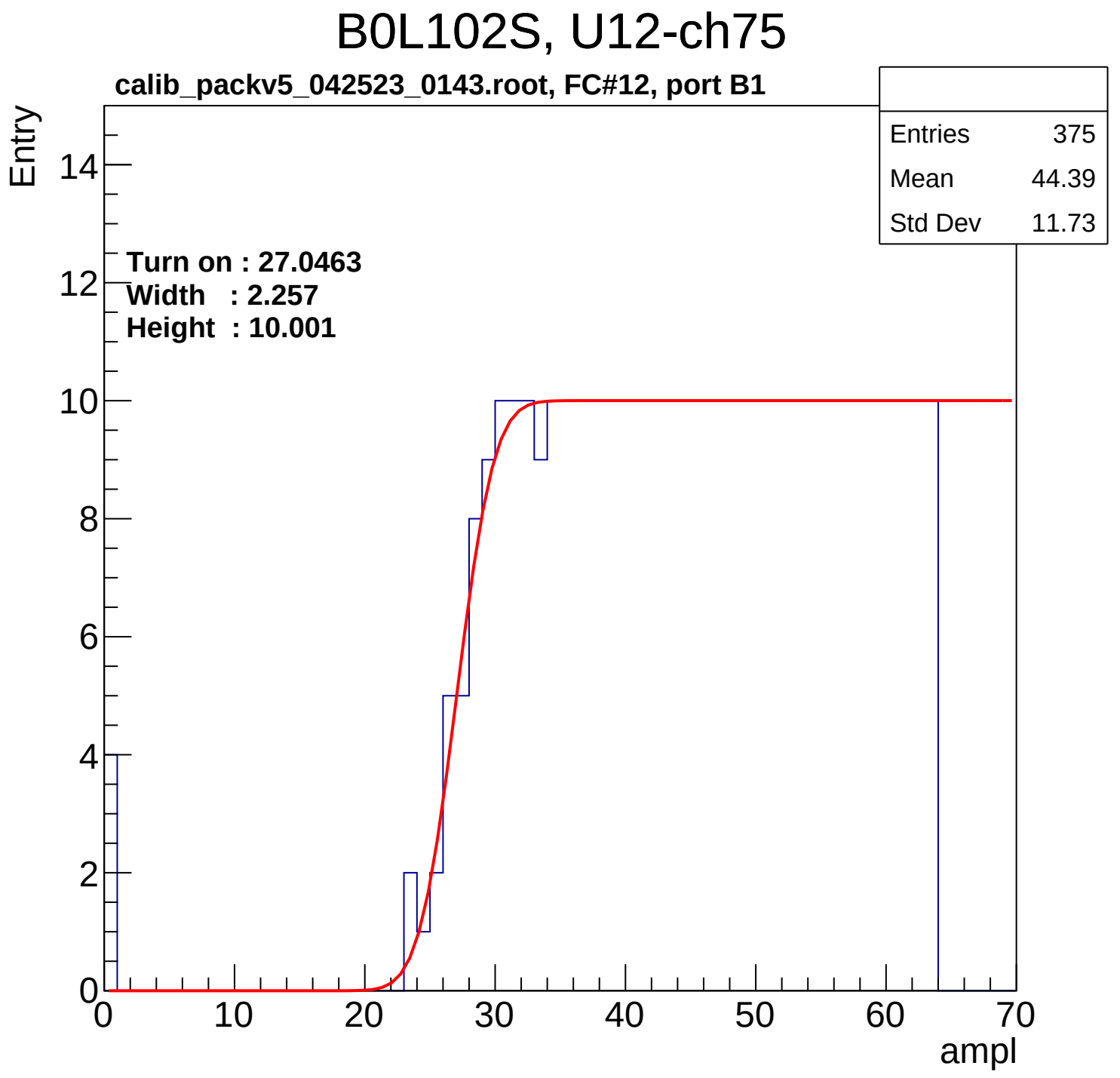
B0L102S, U12-ch75
calib_packv5_042523_0143.root, FC#12, port B1
Entries 375
Mean 44.39
Std Dev 11.73
Turn on : 27.0463
Width : 2.257
Height : 10.001
Entry
ampl
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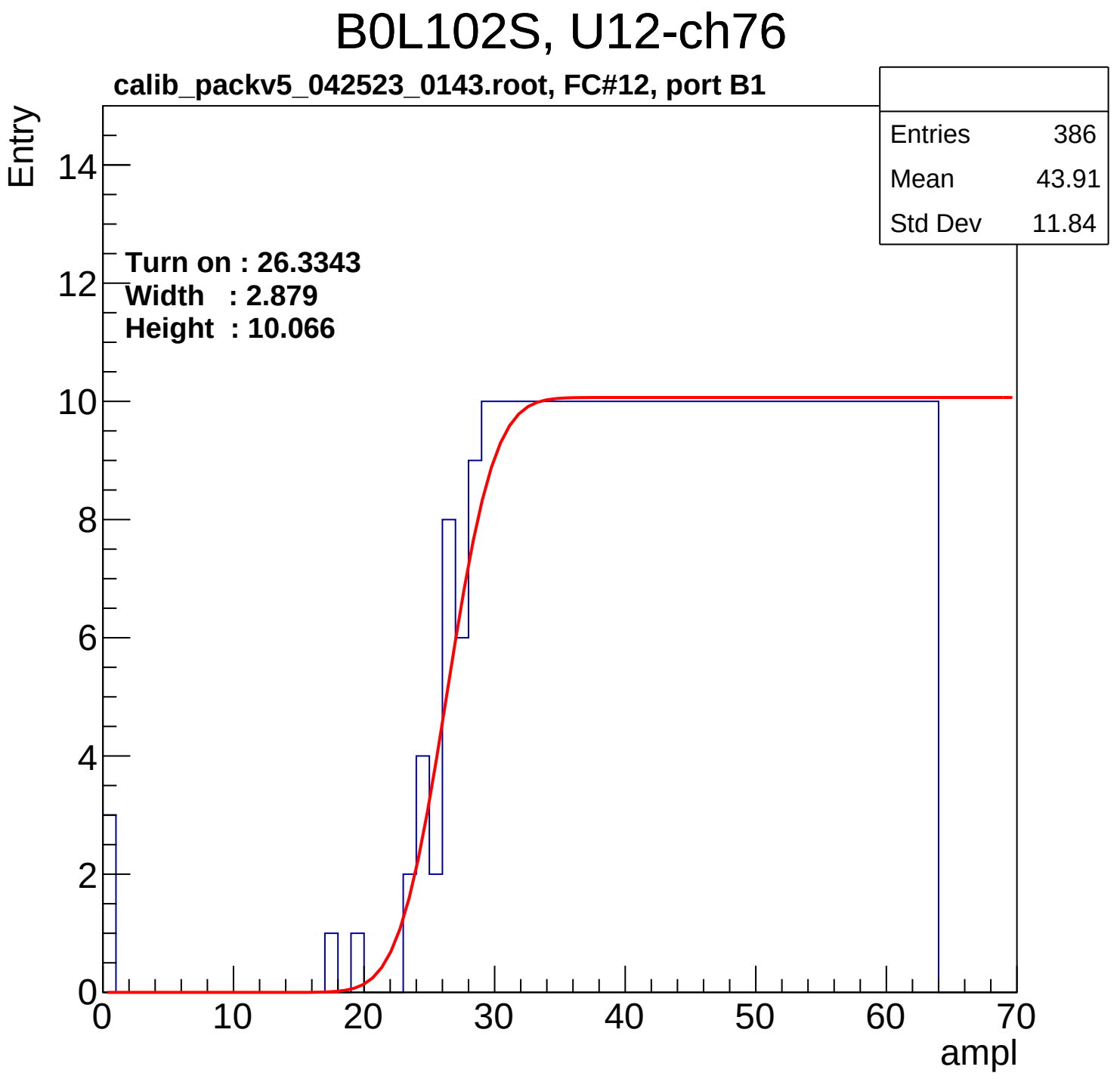
B0L102S, U12-ch76
calib_packv5_042523_0143.root, FC#12, port B1
Entries 386
Mean 43.91
Std Dev 11.84
Turn on : 26.3343
Width : 2.879
Height : 10.066
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ampl
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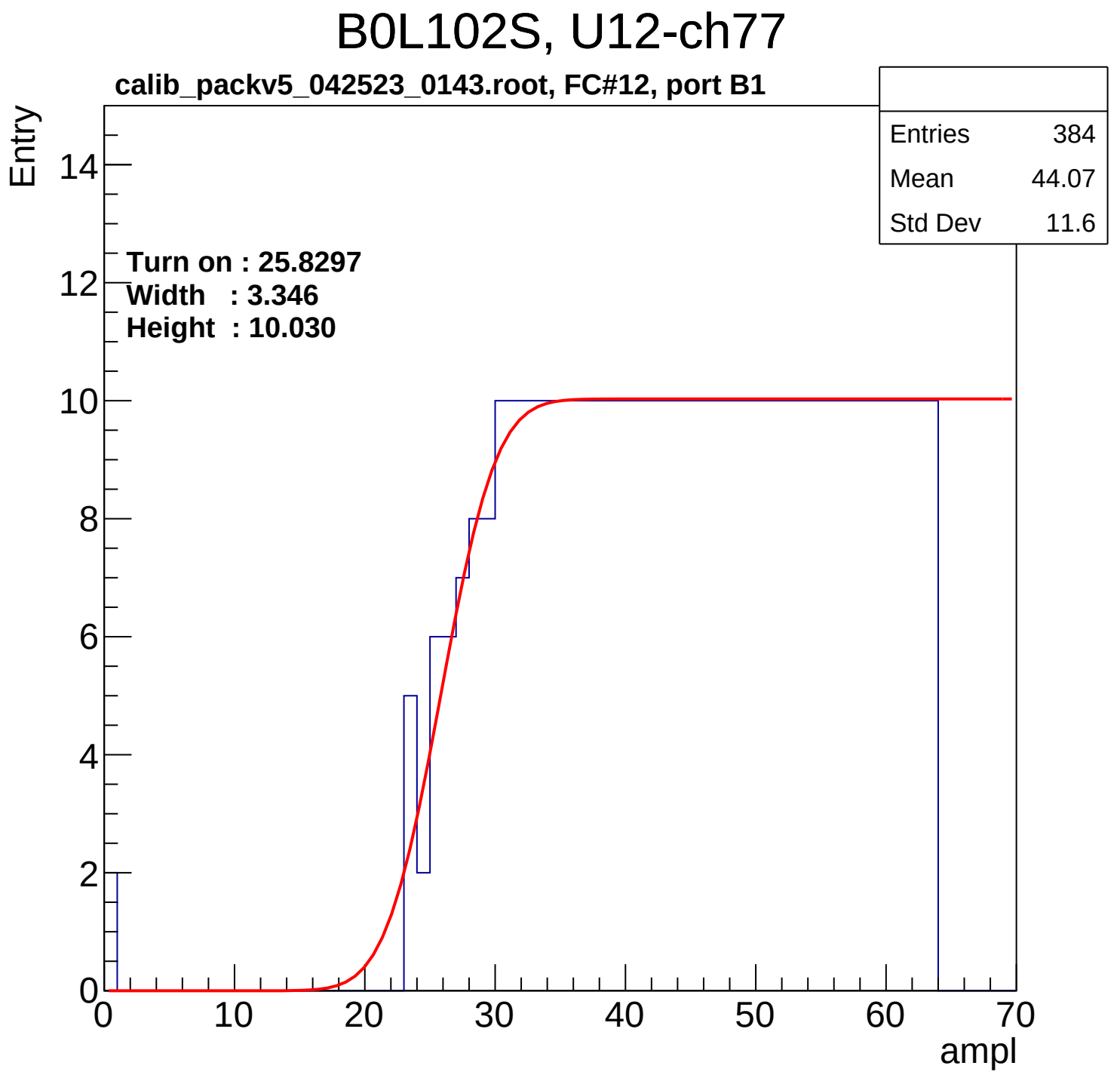
B0L102S, U12-ch77
calib_packv5_042523_0143.root, FC#12, port B1
Entries 384
Mean 44.07
Std Dev 11.6
Turn on : 25.8297
Width : 3.346
Height : 10.030
Entry
ampl
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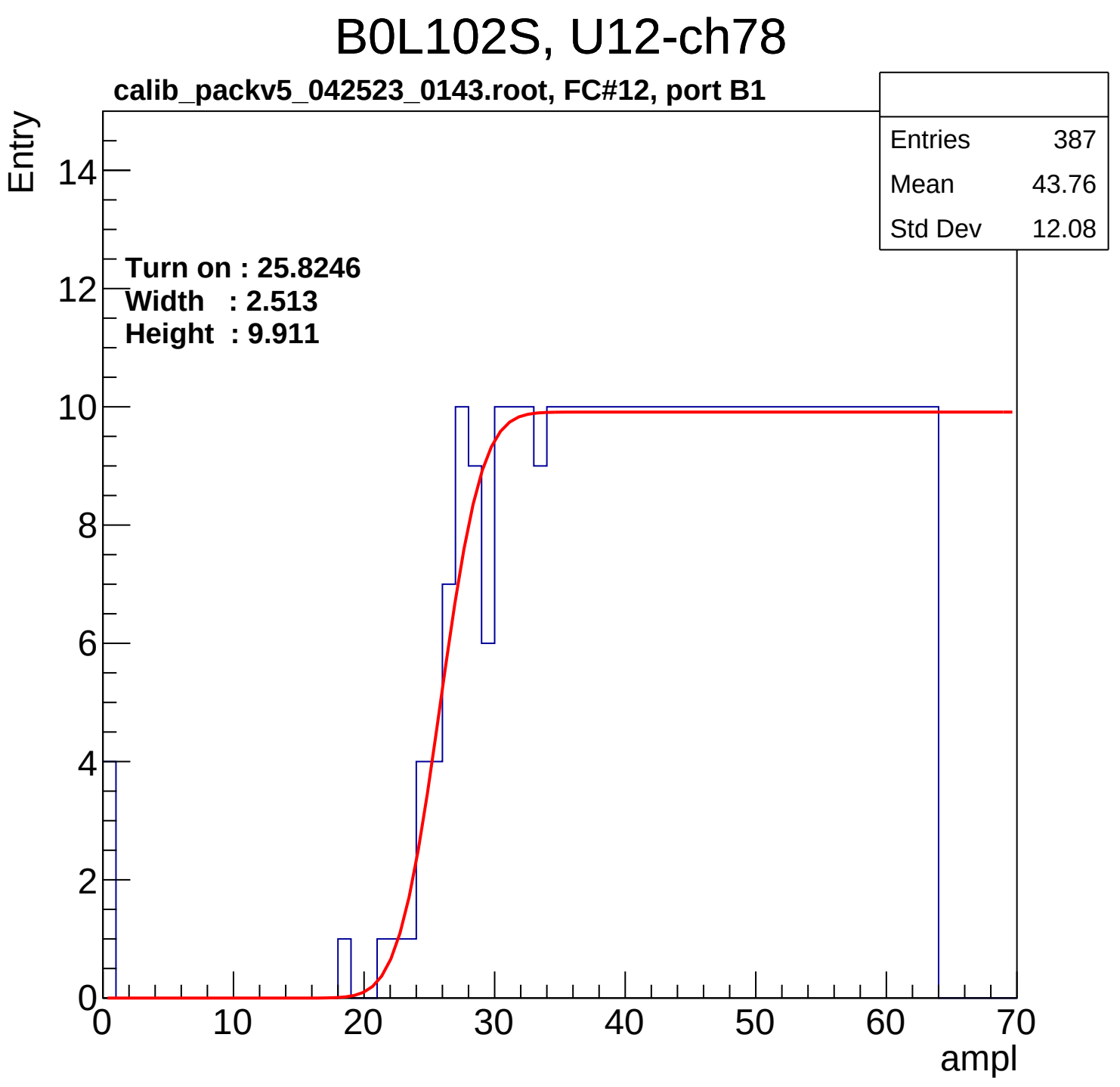
B0L102S, U12-ch78
calib_packv5_042523_0143.root, FC#12, port B1
Entries 387
Mean 43.76
Std Dev 12.08
Turn on : 25.8246
Width : 2.513
Height : 9.911
Entry
ampl
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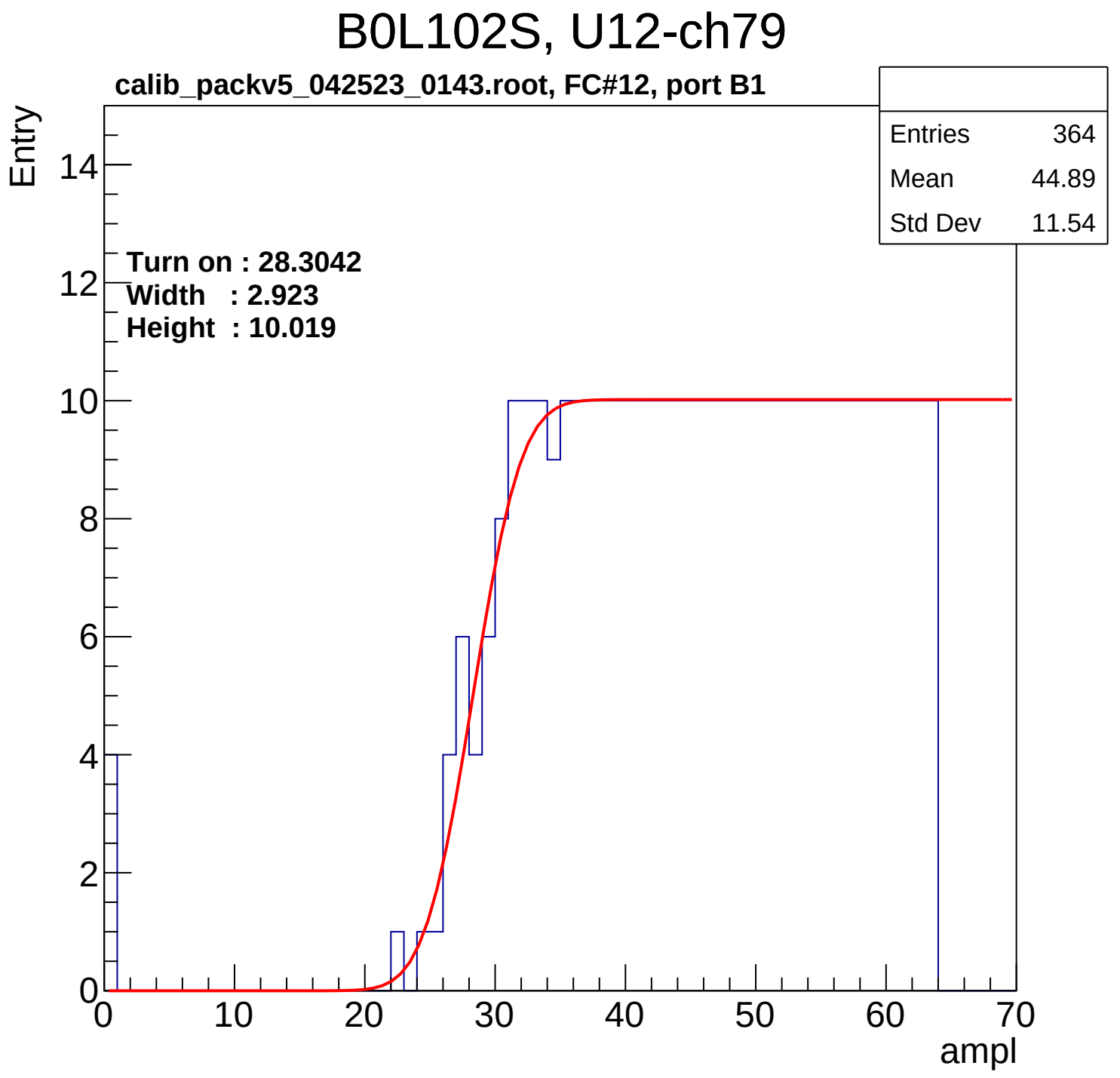
B0L102S, U12-ch79
calib_packv5_042523_0143.root, FC#12, port B1
Entries 364
Mean 44.89
Std Dev 11.54
Turn on : 28.3042
Width : 2.923
Height : 10.019
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ampl
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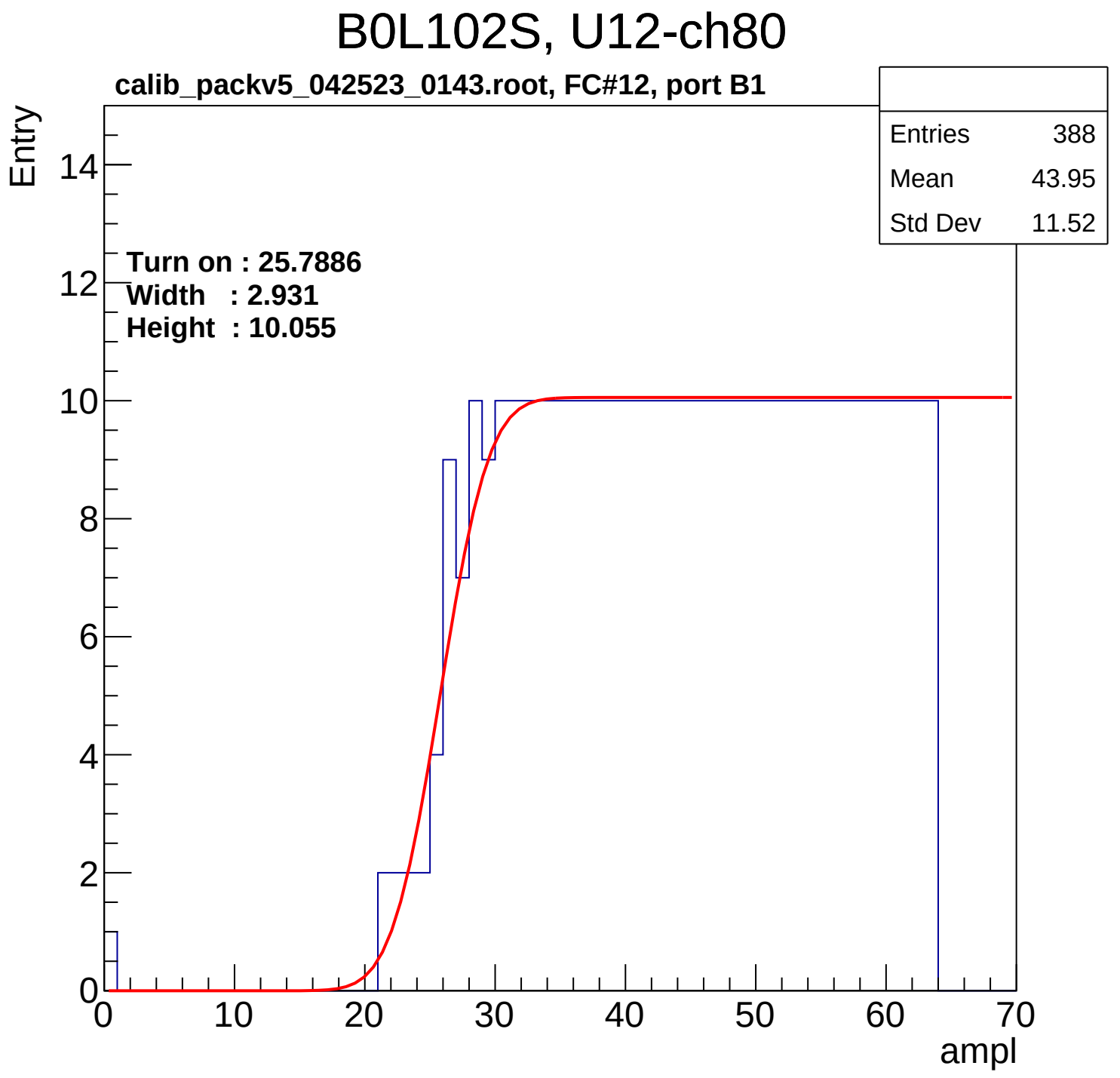
B0L102S, U12-ch80
calib_packv5_042523_0143.root, FC#12, port B1
Entries 388
Mean 43.95
Std Dev 11.52
Turn on : 25.7886
Width : 2.931
Height : 10.055
Entry
ampl
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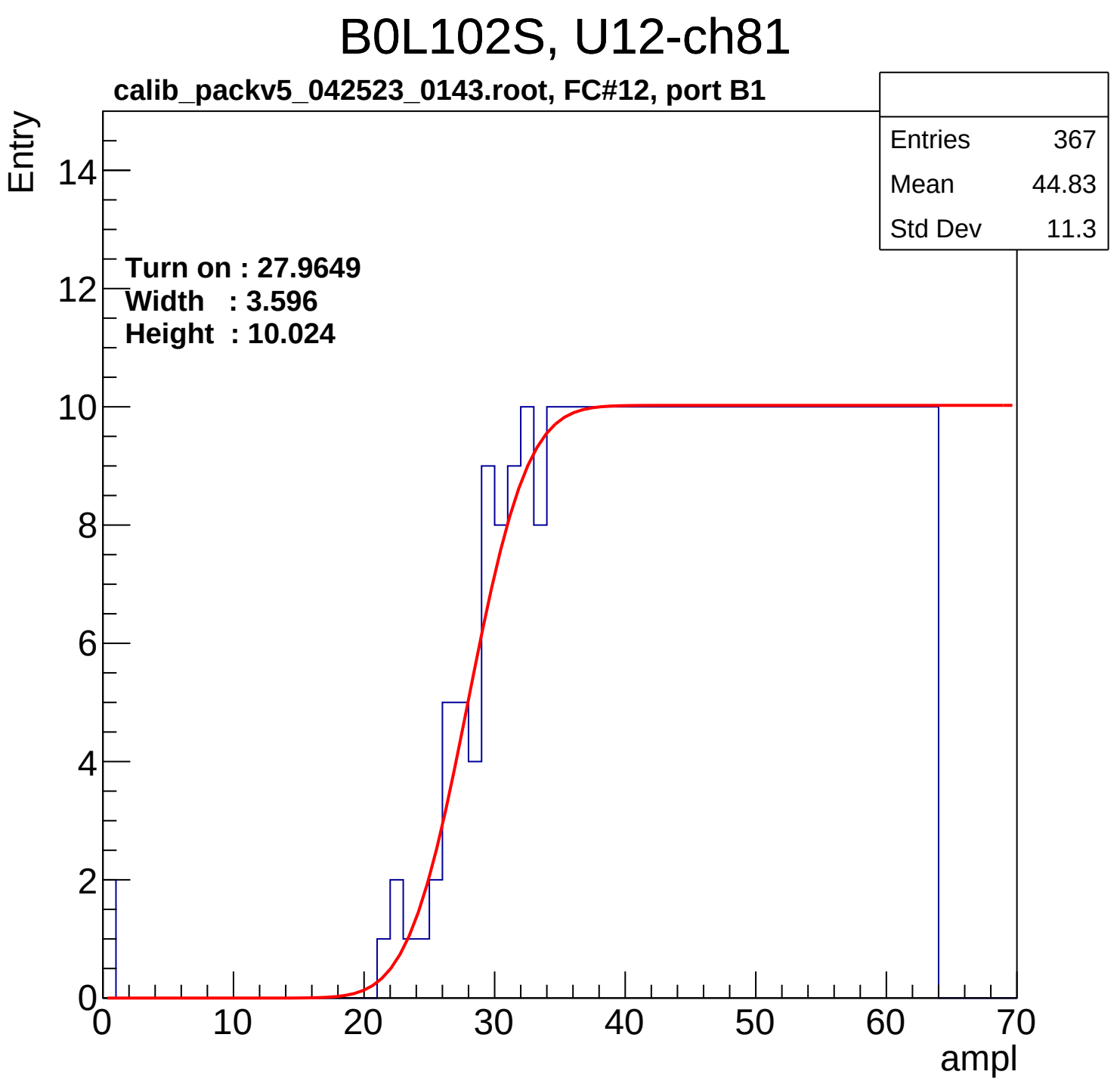
B0L102S, U12-ch81
calib_packv5_042523_0143.root, FC#12, port B1
Entries 367
Mean 44.83
Std Dev 11.3
Turn on : 27.9649
Width : 3.596
Height : 10.024
Entry
ampl
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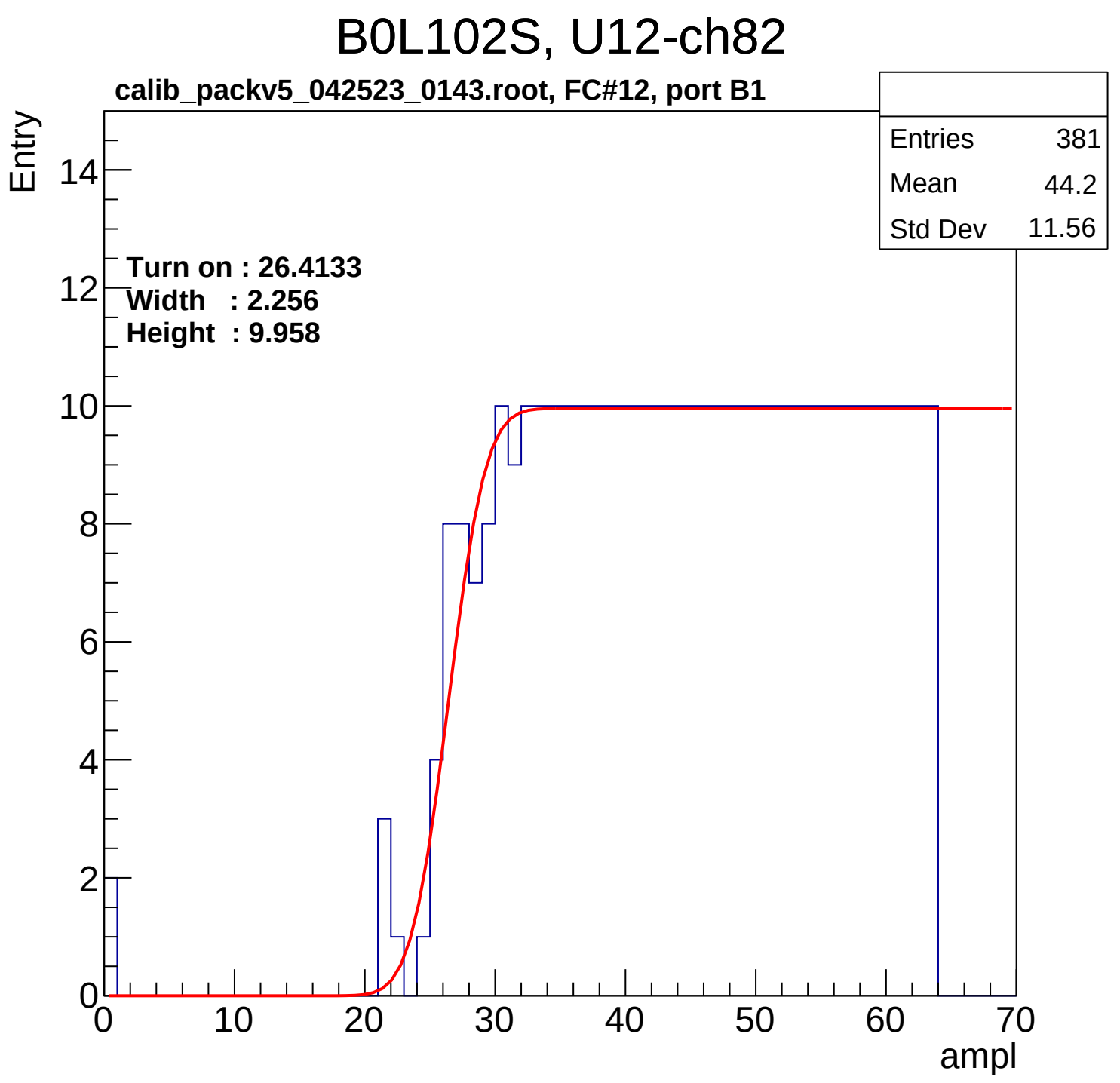
B0L102S, U12-ch82
calib_packv5_042523_0143.root, FC#12, port B1
Entries 381
Mean 44.2
Std Dev 11.56
Turn on : 26.4133
Width : 2.256
Height : 9.958
Entry
ampl
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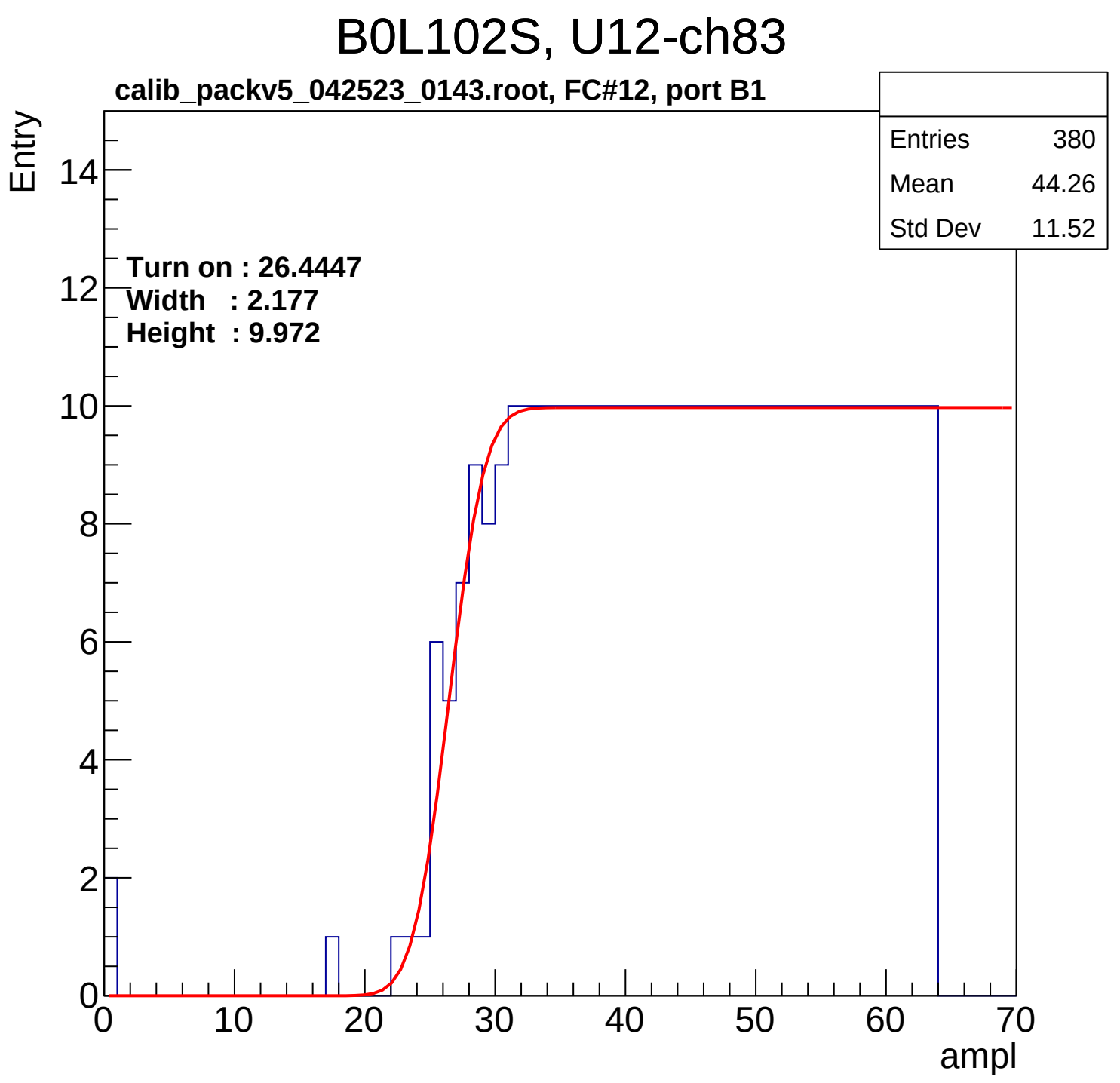
B0L102S, U12-ch83
calib_packv5_042523_0143.root, FC#12, port B1
Entries 380
Mean 44.26
Std Dev 11.52
Turn on : 26.4447
Width : 2.177
Height : 9.972
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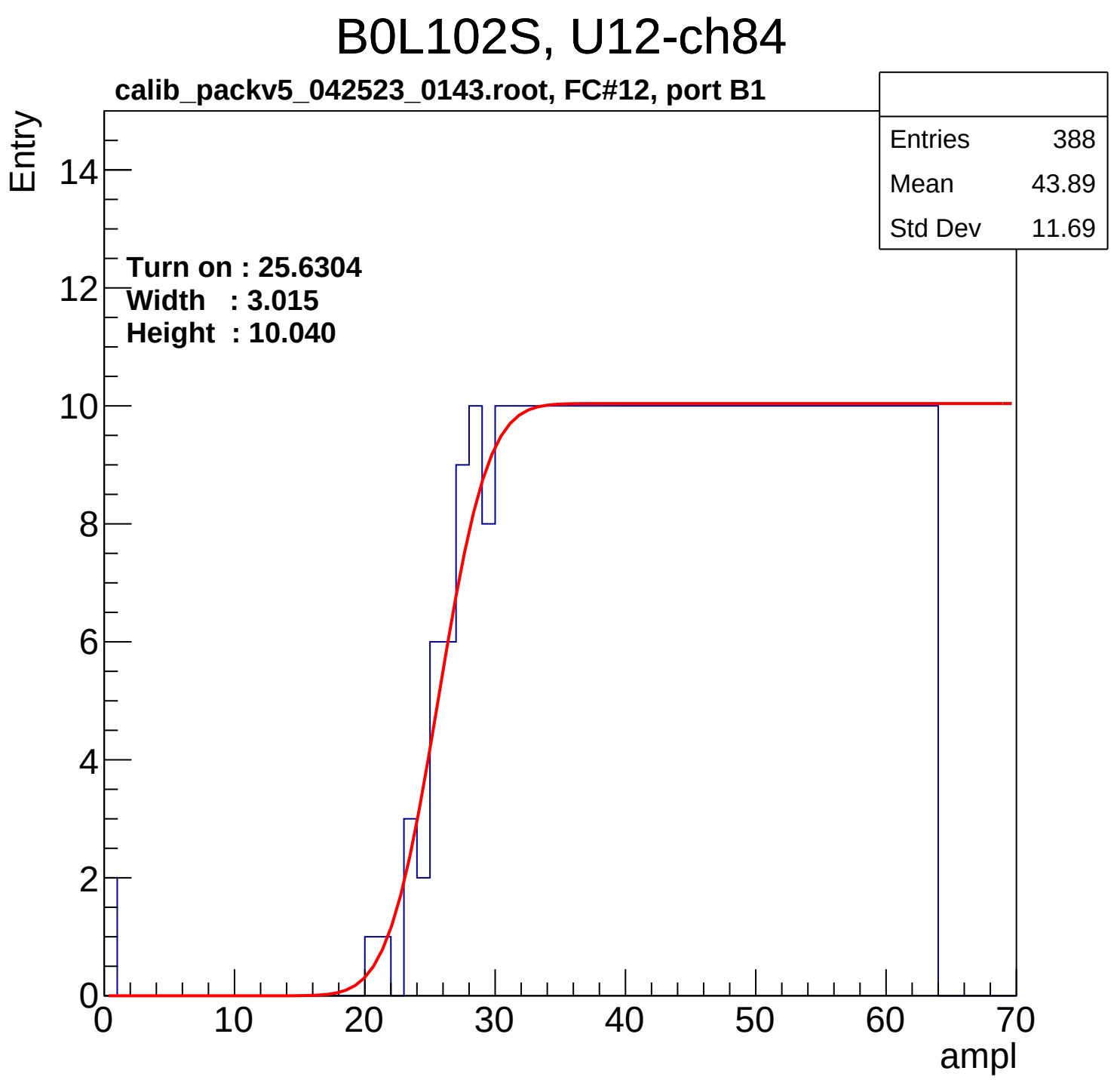
B0L102S, U12-ch84
calib_packv5_042523_0143.root, FC#12, port B1
Entries 388
Mean 43.89
Std Dev 11.69
Turn on : 25.6304
Width : 3.015
Height : 10.040
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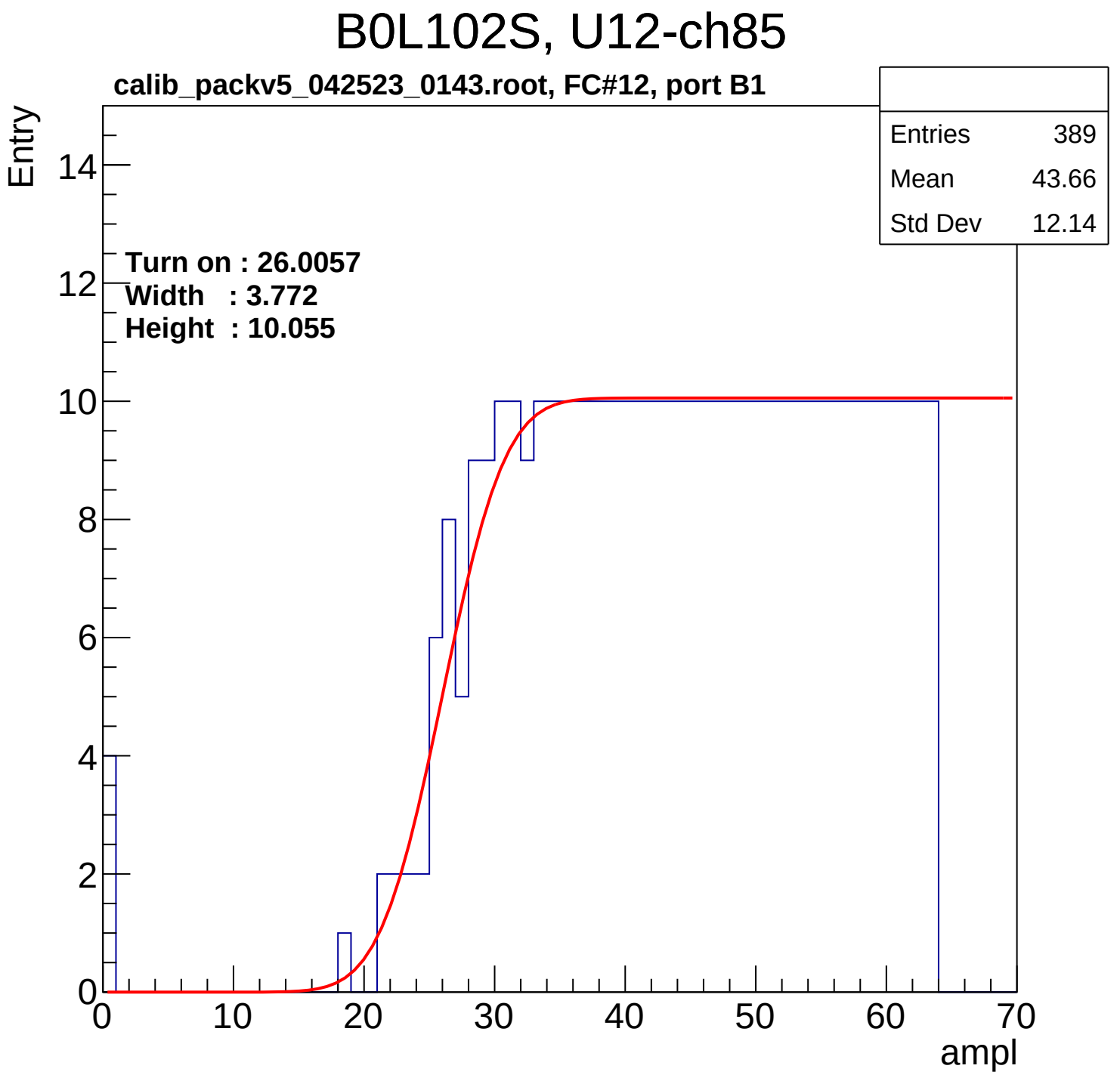
B0L102S, U12-ch85
calib_packv5_042523_0143.root, FC#12, port B1
Entries 389
Mean 43.66
Std Dev 12.14
Turn on : 26.0057
Width : 3.772
Height : 10.055
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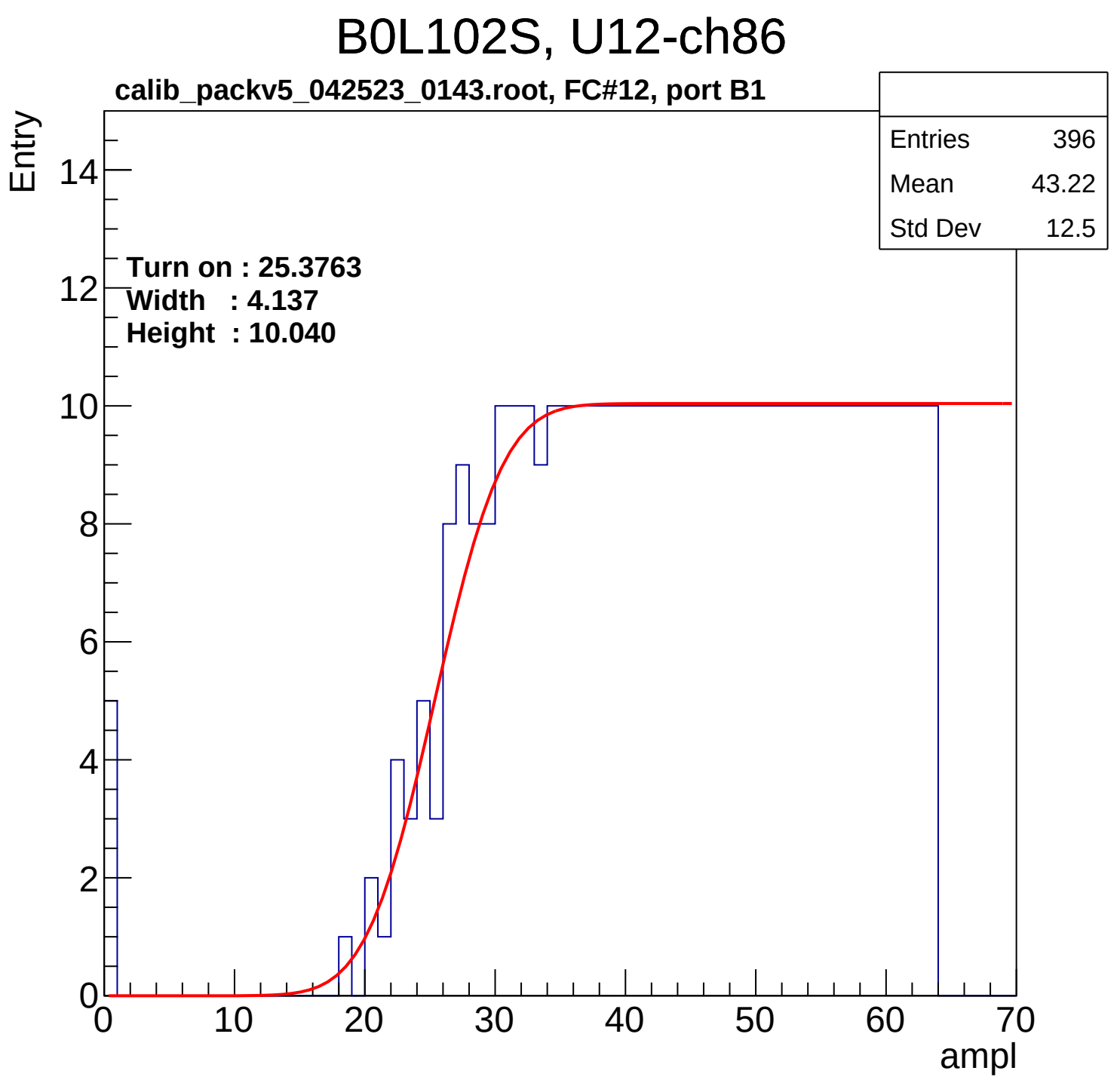
B0L102S, U12-ch86
calib_packv5_042523_0143.root, FC#12, port B1
Entries 396
Mean 43.22
Std Dev 12.5
Turn on : 25.3763
Width : 4.137
Height : 10.040
Entry
ampl
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6
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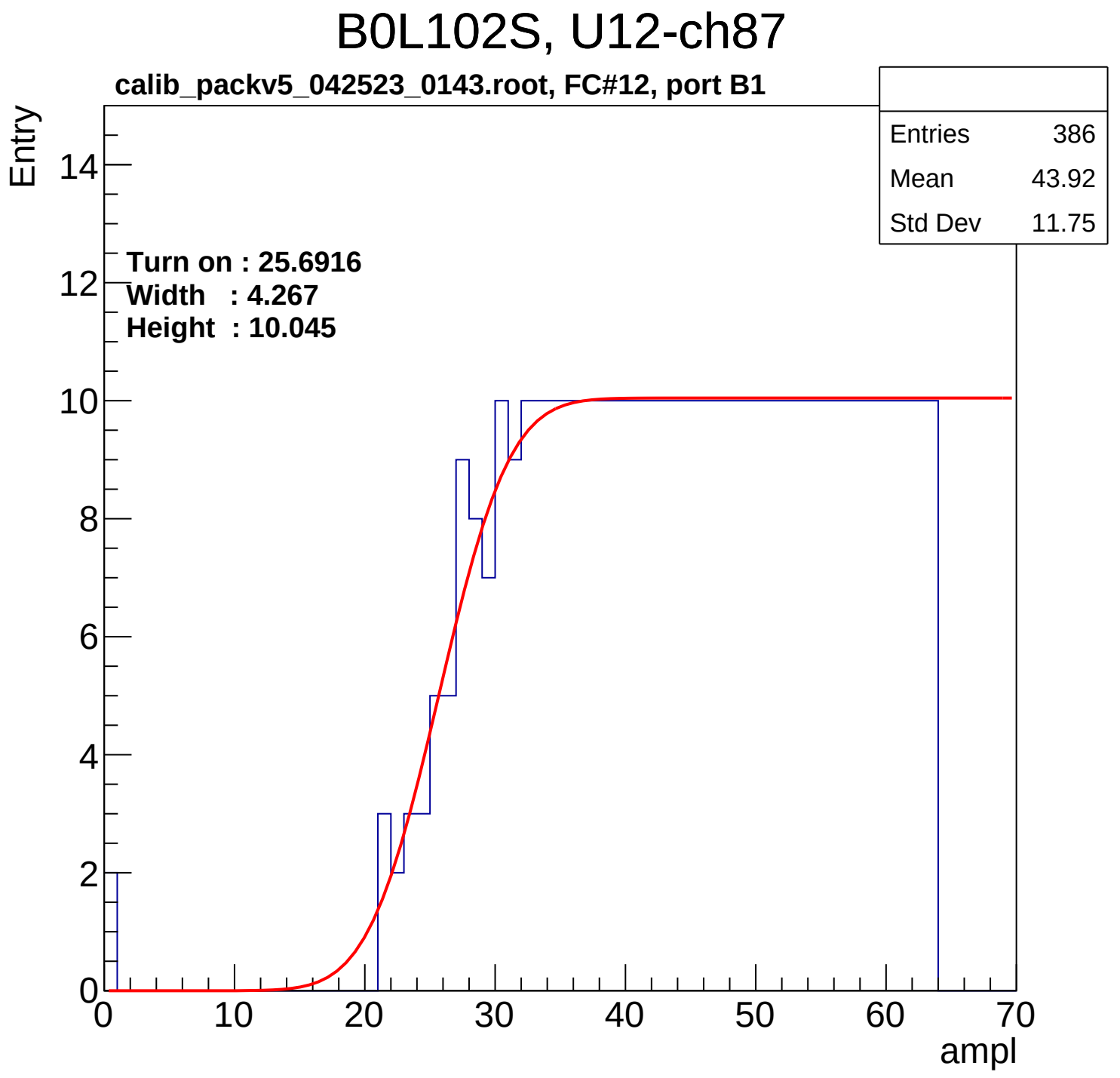
B0L102S, U12-ch87
calib_packv5_042523_0143.root, FC#12, port B1
Entries 386
Mean 43.92
Std Dev 11.75
Turn on : 25.6916
Width : 4.267
Height : 10.045
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ampl
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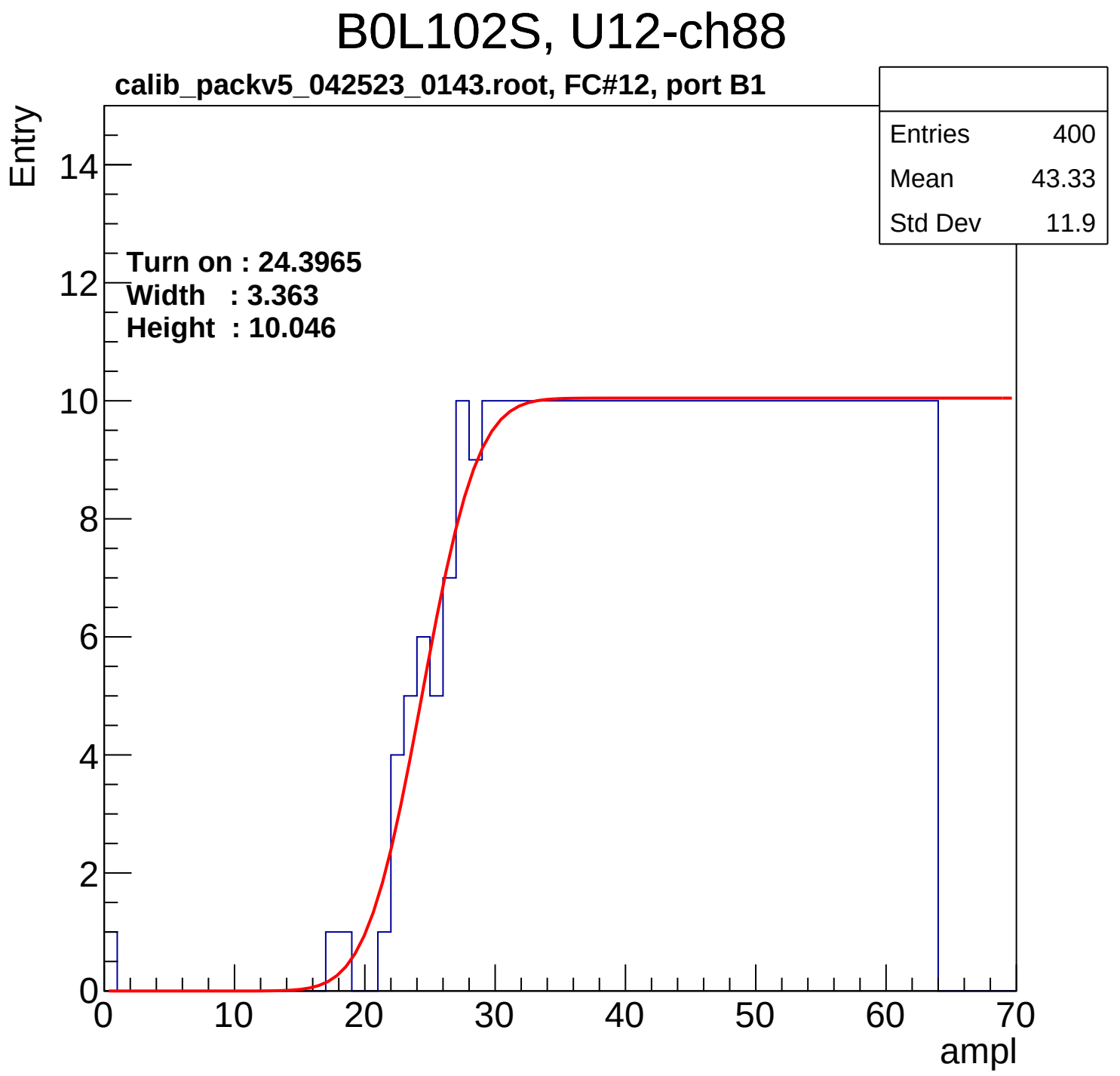
B0L102S, U12-ch88
calib_packv5_042523_0143.root, FC#12, port B1
Entries 400
Mean 43.33
Std Dev 11.9
Turn on : 24.3965
Width : 3.363
Height : 10.046
Entry
ampl
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2
4
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8
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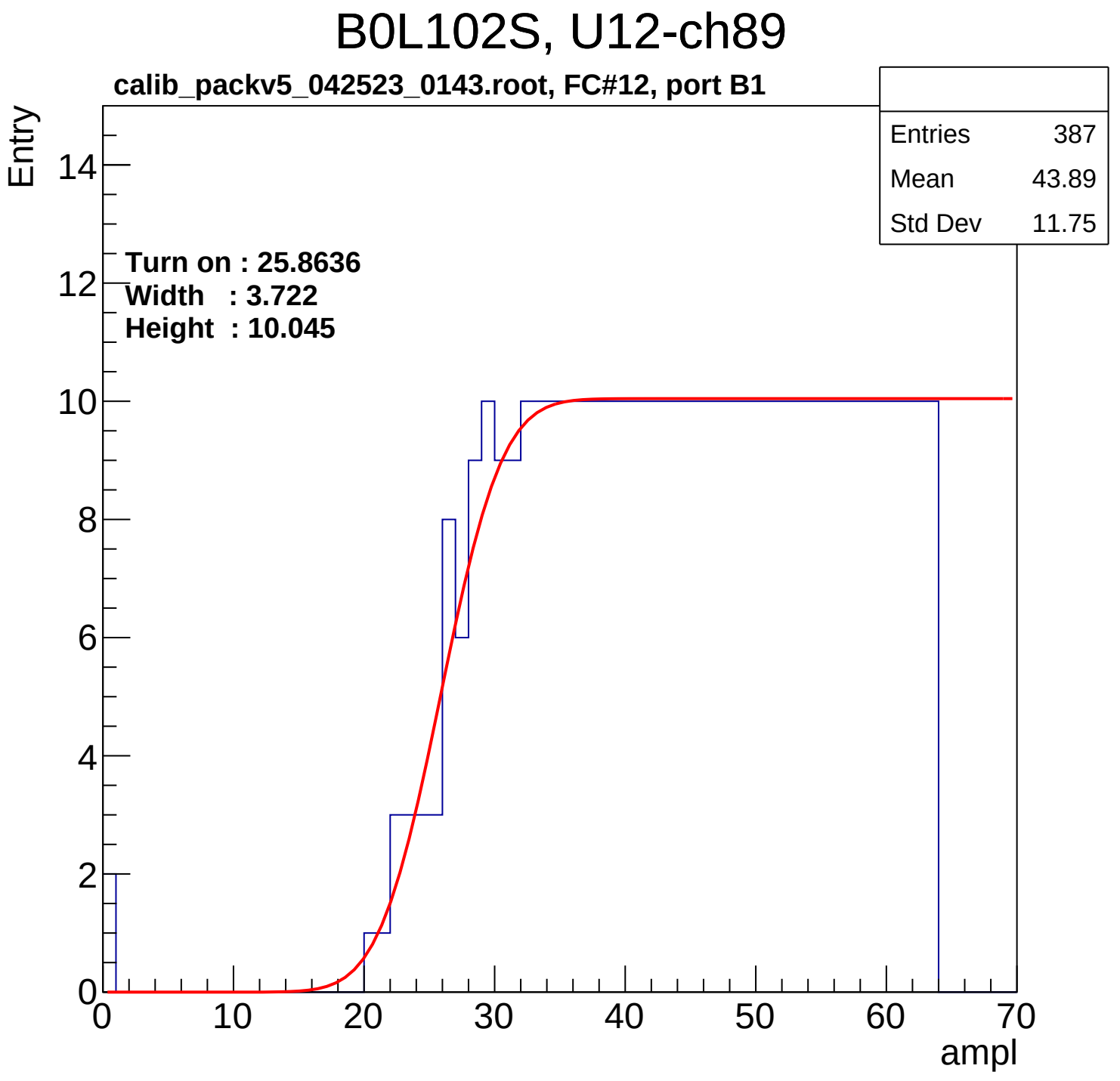
B0L102S, U12-ch89
calib_packv5_042523_0143.root, FC#12, port B1
Entries 387
Mean 43.89
Std Dev 11.75
Turn on : 25.8636
Width : 3.722
Height : 10.045
Entry
ampl
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2
4
6
8
10
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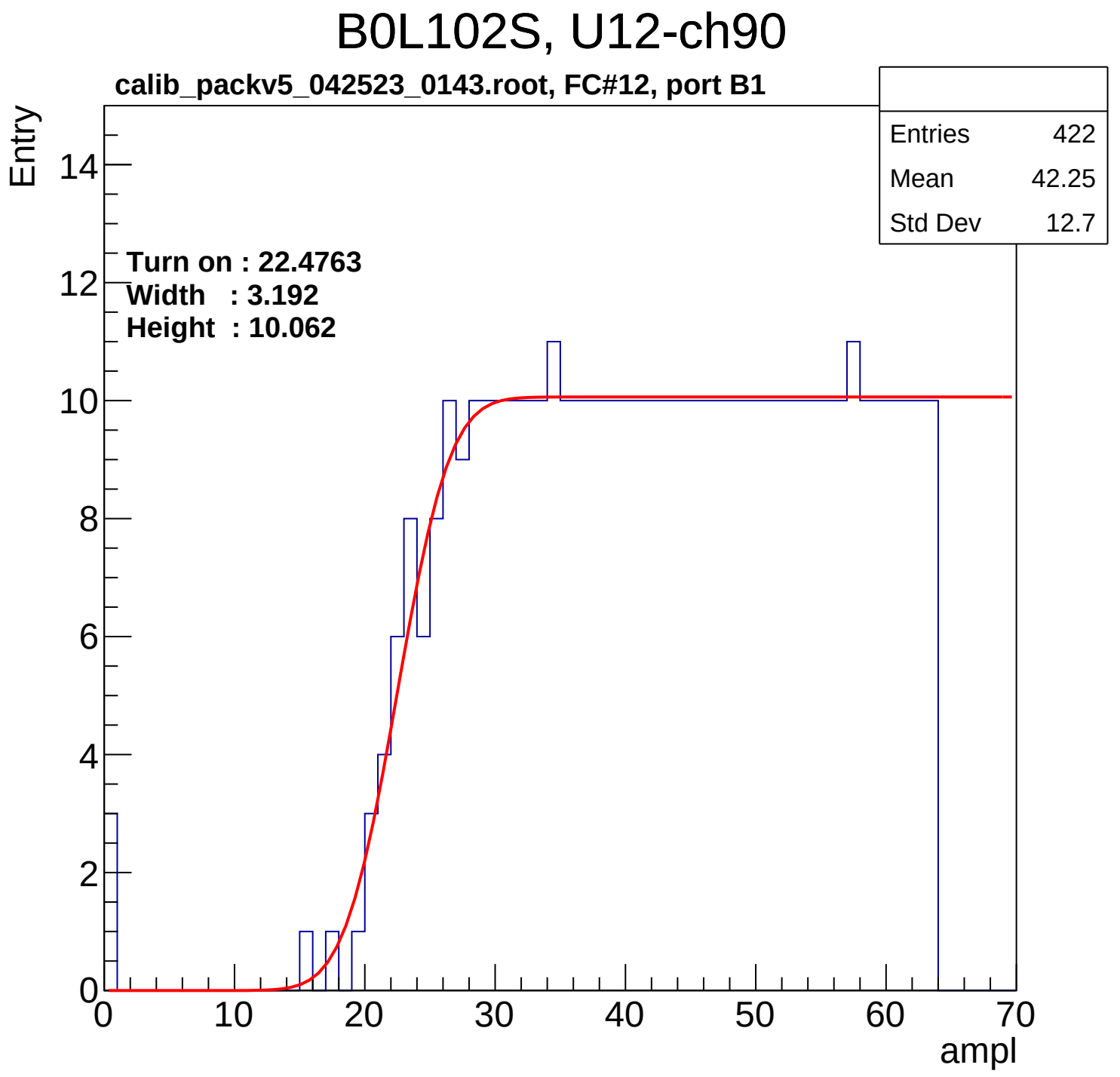
B0L102S, U12-ch90
calib_packv5_042523_0143.root, FC#12, port B1
Entries 422
Mean 42.25
Std Dev 12.7
Turn on : 22.4763
Width : 3.192
Height : 10.062
Entry
ampl
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2
4
6
8
10
12
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0
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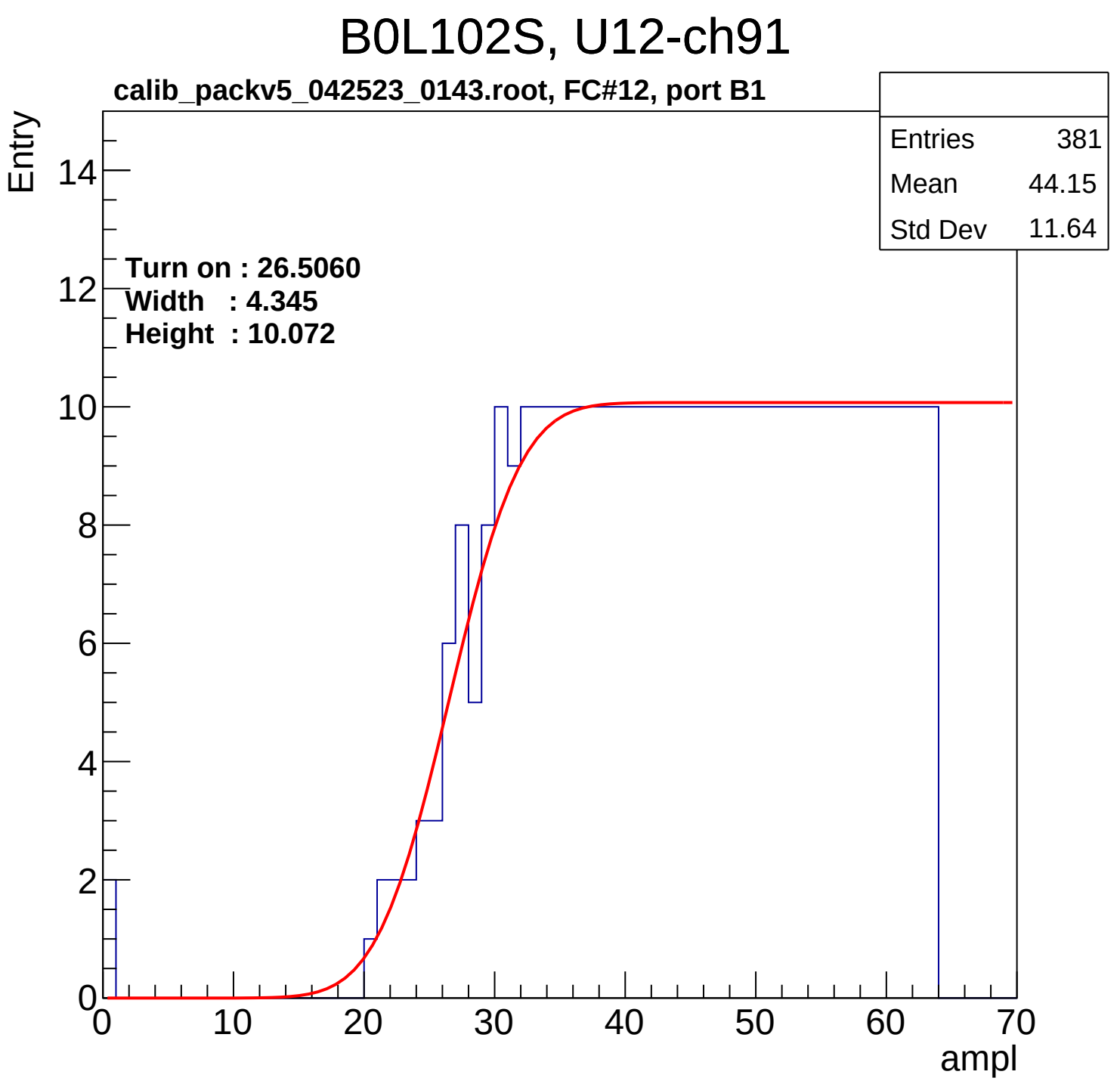
B0L102S, U12-ch91
calib_packv5_042523_0143.root, FC#12, port B1
Entries 381
Mean 44.15
Std Dev 11.64
Turn on : 26.5060
Width : 4.345
Height : 10.072
Entry
ampl
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2
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6
8
10
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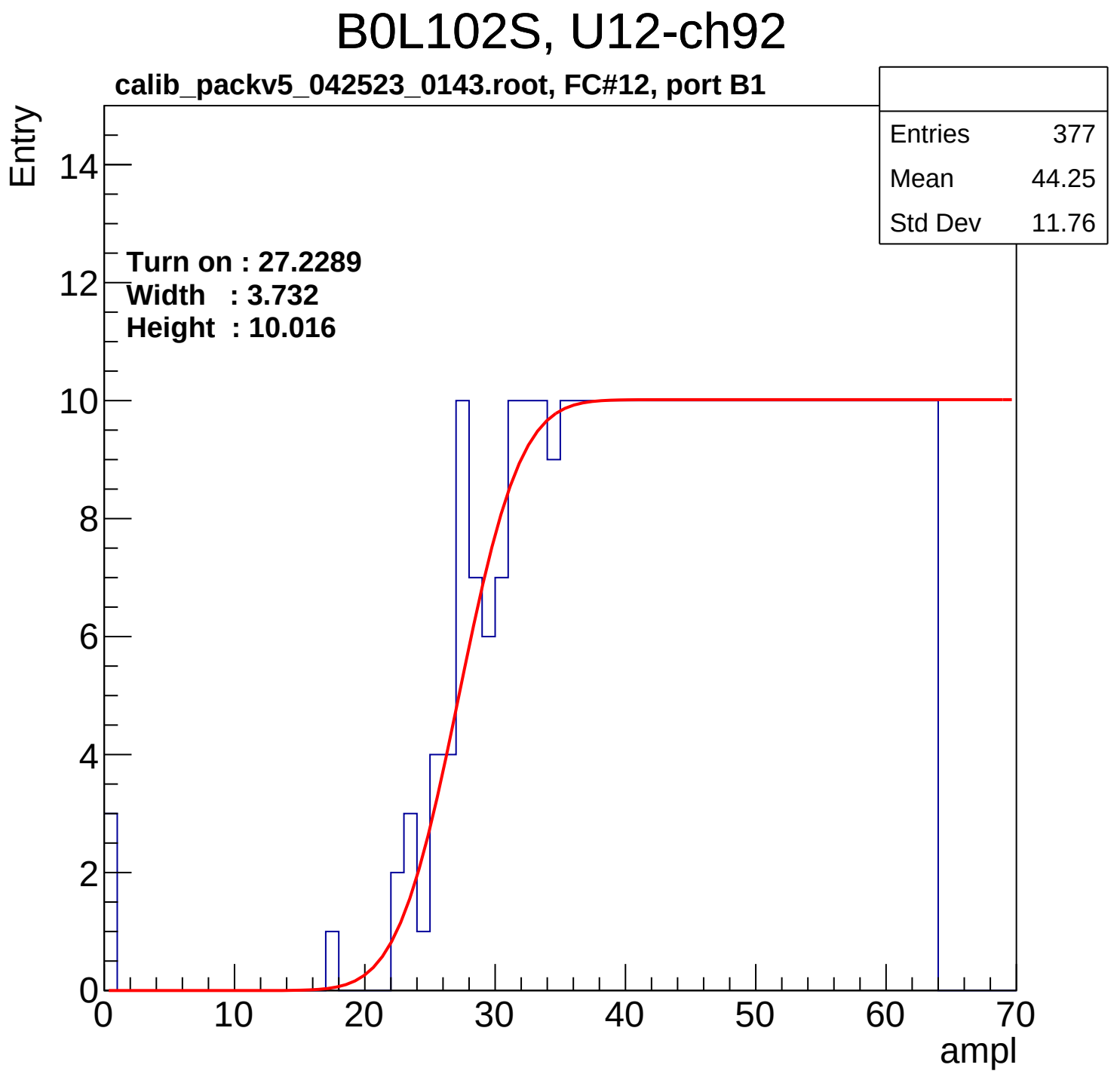
B0L102S, U12-ch92
calib_packv5_042523_0143.root, FC#12, port B1
Entries 377
Mean 44.25
Std Dev 11.76
Turn on : 27.2289
Width : 3.732
Height : 10.016
Entry
ampl
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2
4
6
8
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0
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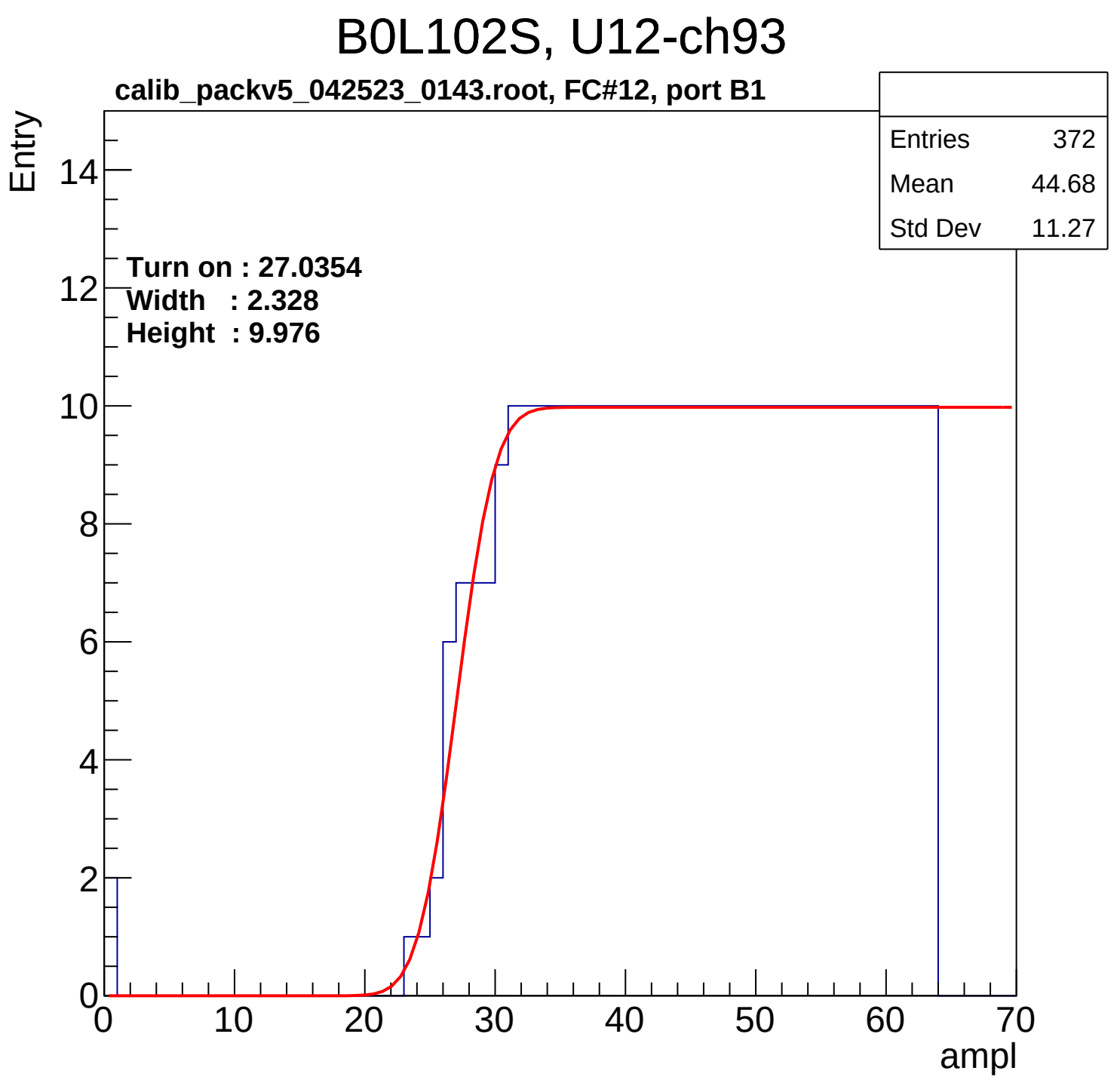
B0L102S, U12-ch93
calib_packv5_042523_0143.root, FC#12, port B1
Entries 372
Mean 44.68
Std Dev 11.27
Turn on : 27.0354
Width : 2.328
Height : 9.976
Entry
ampl
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2
4
6
8
10
12
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0
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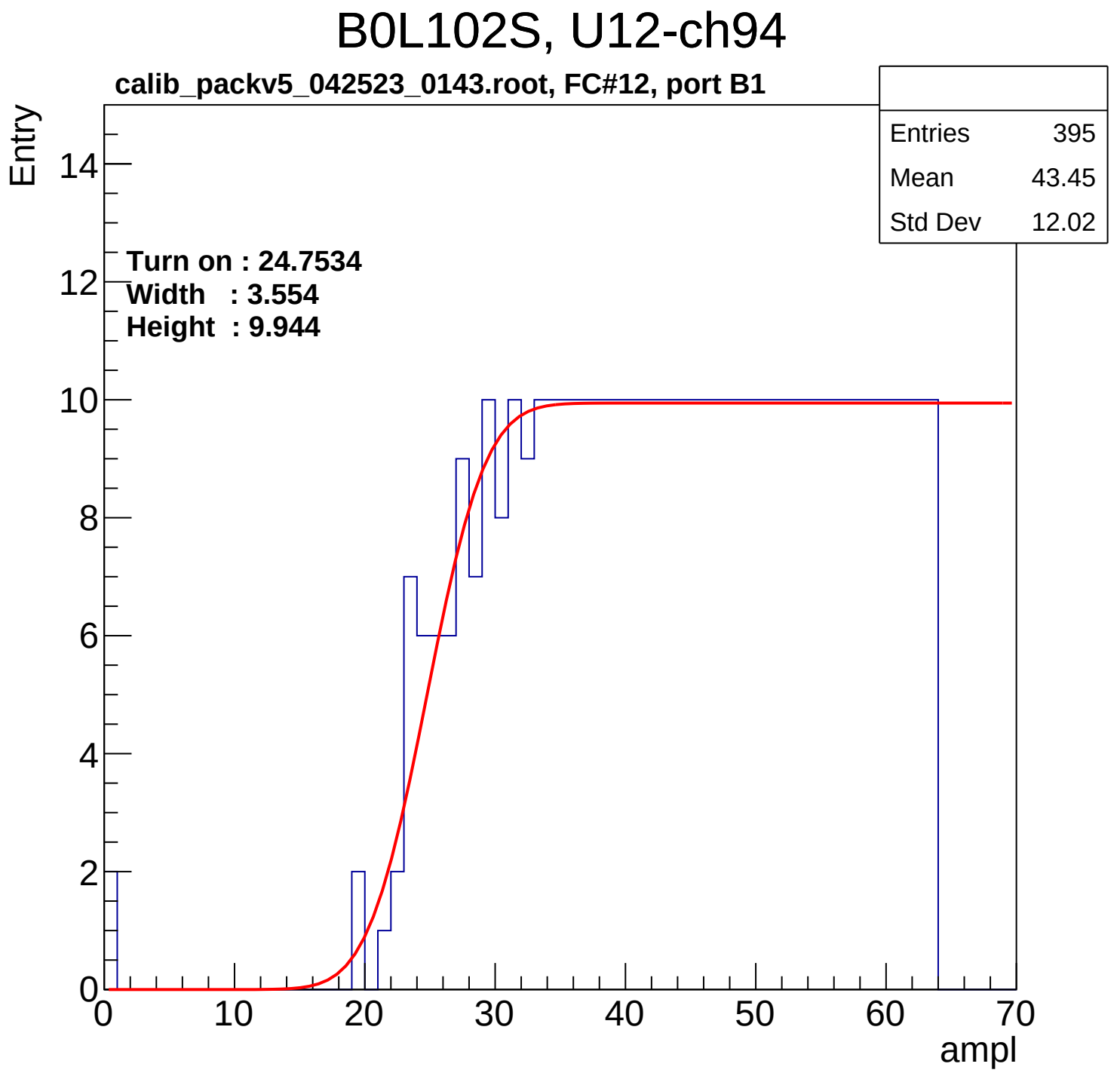
B0L102S, U12-ch94
calib_packv5_042523_0143.root, FC#12, port B1
Entries 395
Mean 43.45
Std Dev 12.02
Turn on : 24.7534
Width : 3.554
Height : 9.944
Entry
ampl
0
2
4
6
8
10
12
14
0
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20
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40
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60
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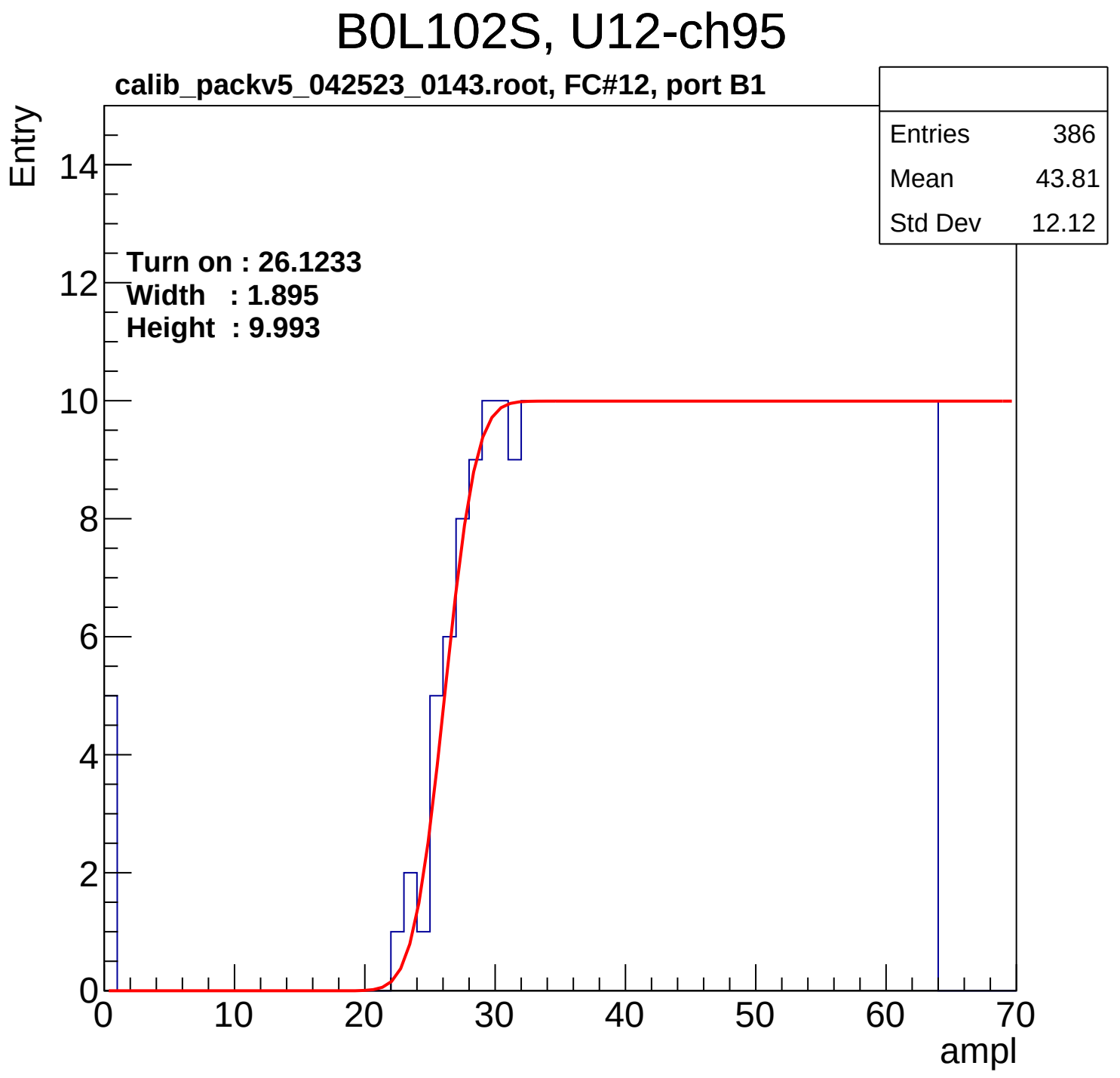
B0L102S, U12-ch95
calib_packv5_042523_0143.root, FC#12, port B1
Entries 386
Mean 43.81
Std Dev 12.12
Turn on : 26.1233
Width : 1.895
Height : 9.993
Entry
ampl
0
2
4
6
8
10
12
14
0
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20
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60
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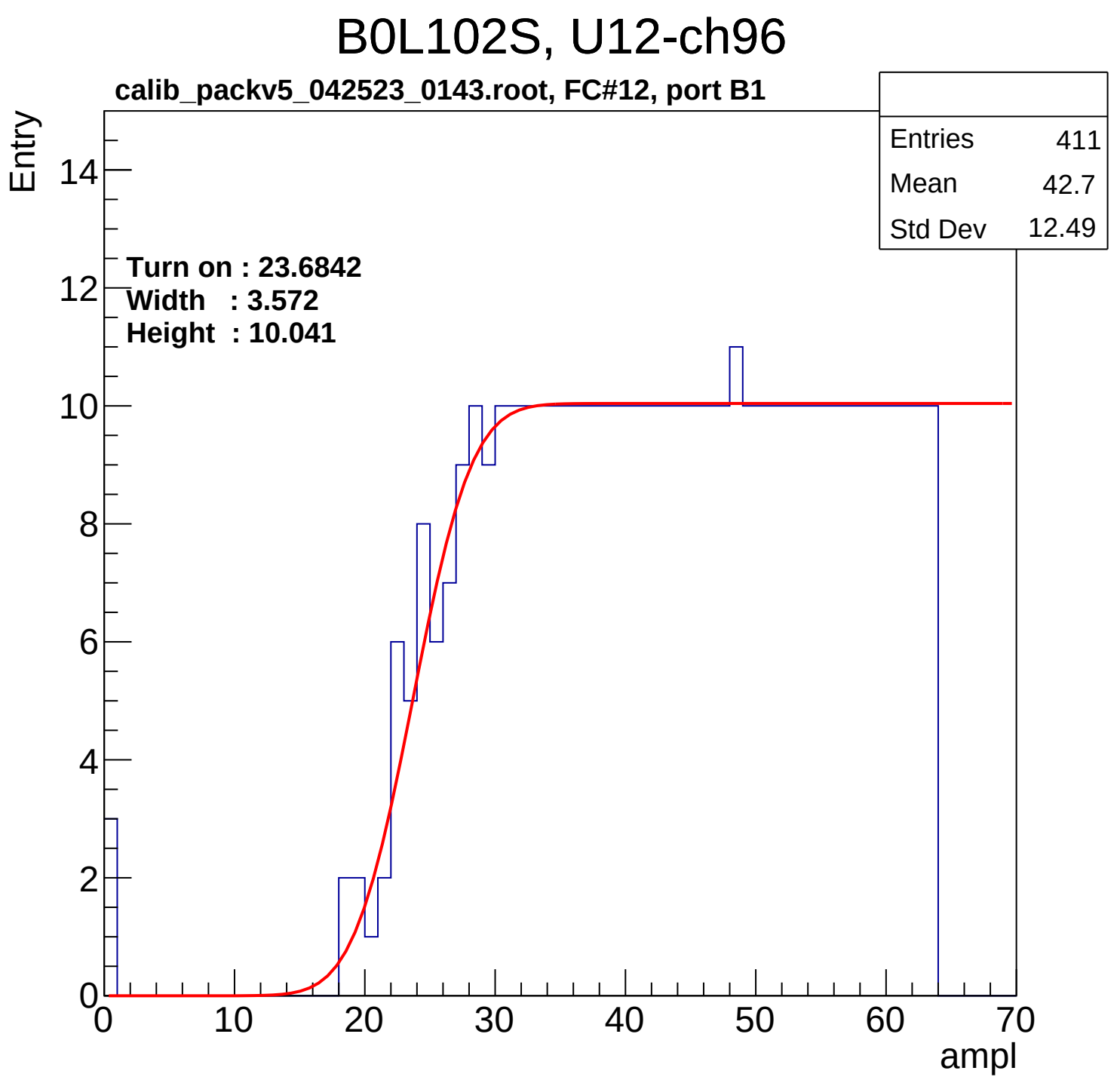
B0L102S, U12-ch96
calib_packv5_042523_0143.root, FC#12, port B1
Entries 411
Mean 42.7
Std Dev 12.49
Turn on : 23.6842
Width : 3.572
Height : 10.041
Entry
ampl
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2
4
6
8
10
12
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0
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60
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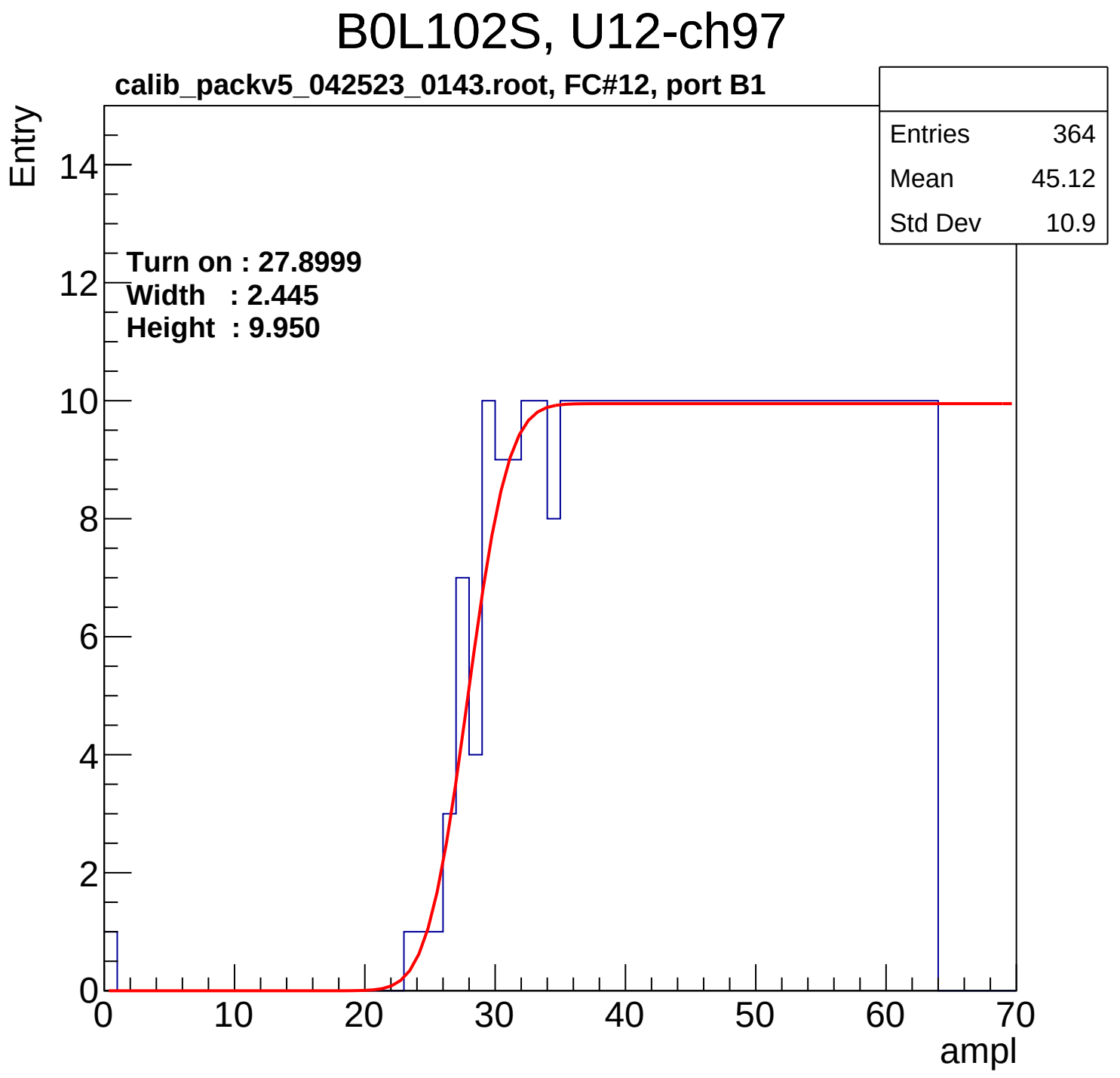
B0L102S, U12-ch97
calib_packv5_042523_0143.root, FC#12, port B1
Entries 364
Mean 45.12
Std Dev 10.9
Turn on : 27.8999
Width : 2.445
Height : 9.950
Entry
ampl
0
2
4
6
8
10
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0
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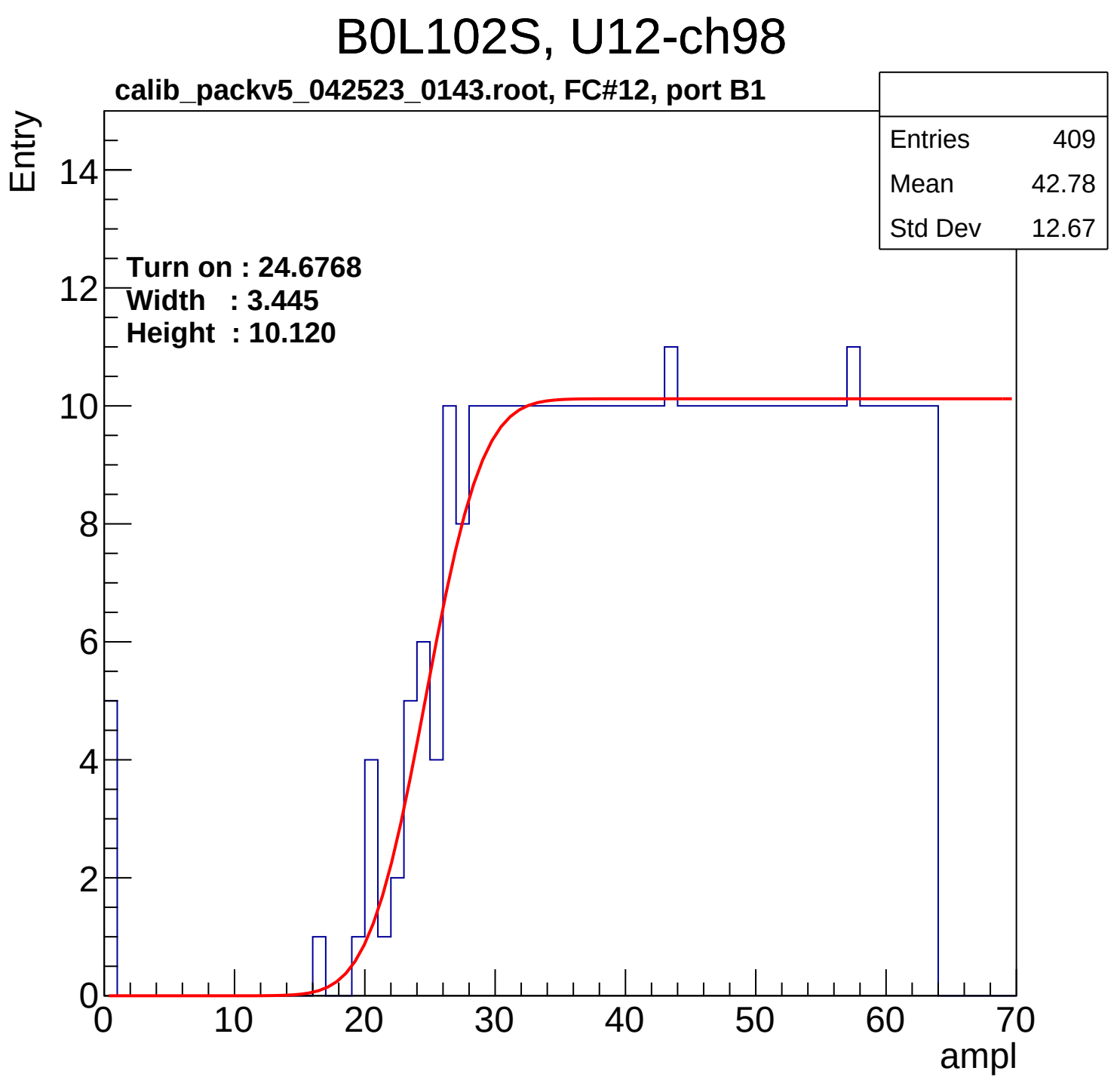
B0L102S, U12-ch98
calib_packv5_042523_0143.root, FC#12, port B1
Entries 409
Mean 42.78
Std Dev 12.67
Turn on : 24.6768
Width : 3.445
Height : 10.120
Entry
ampl
0
2
4
6
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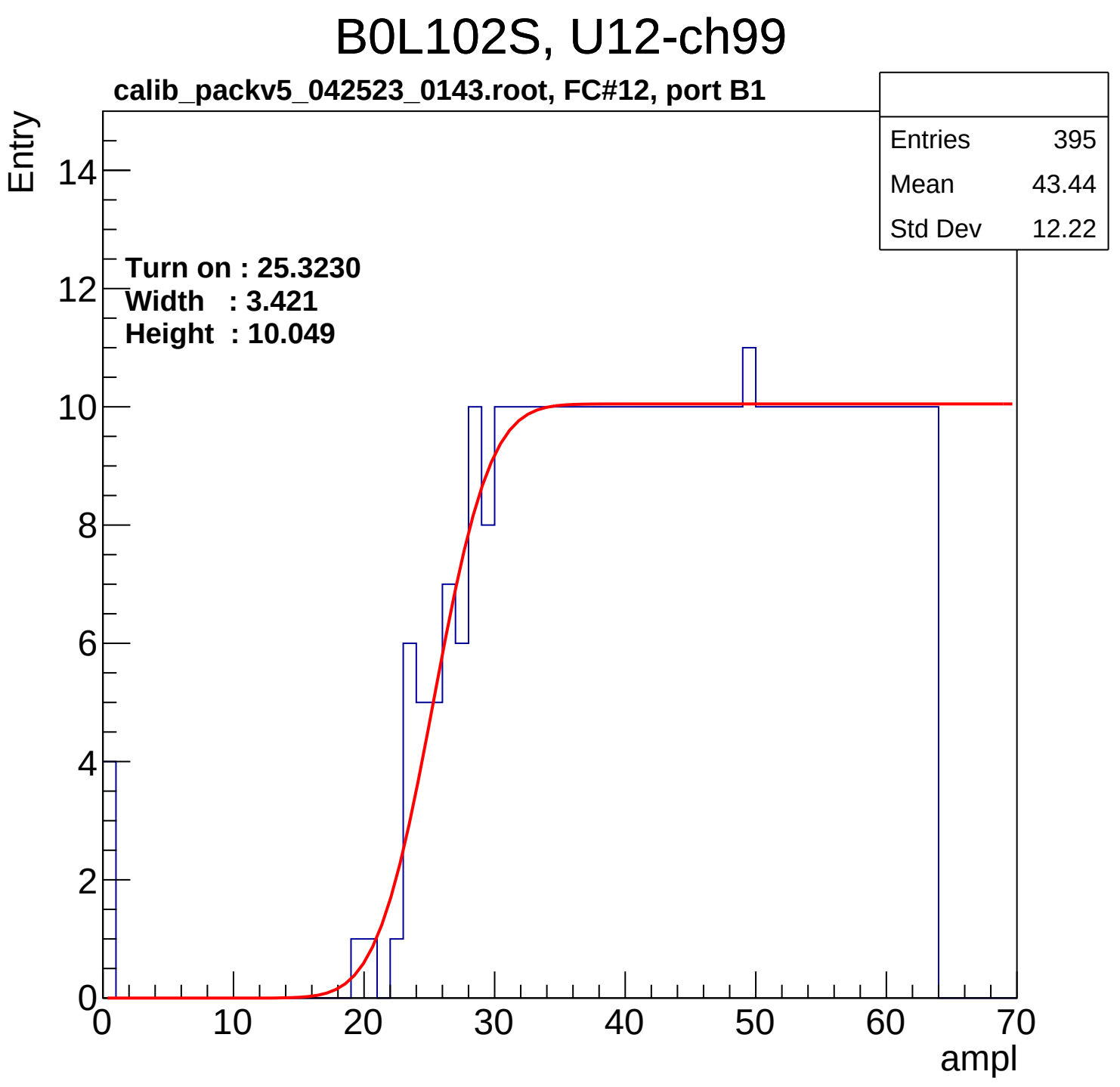
B0L102S, U12-ch99
calib_packv5_042523_0143.root, FC#12, port B1
Entries 395
Mean 43.44
Std Dev 12.22
Turn on : 25.3230
Width : 3.421
Height : 10.049
Entry
ampl
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6
8
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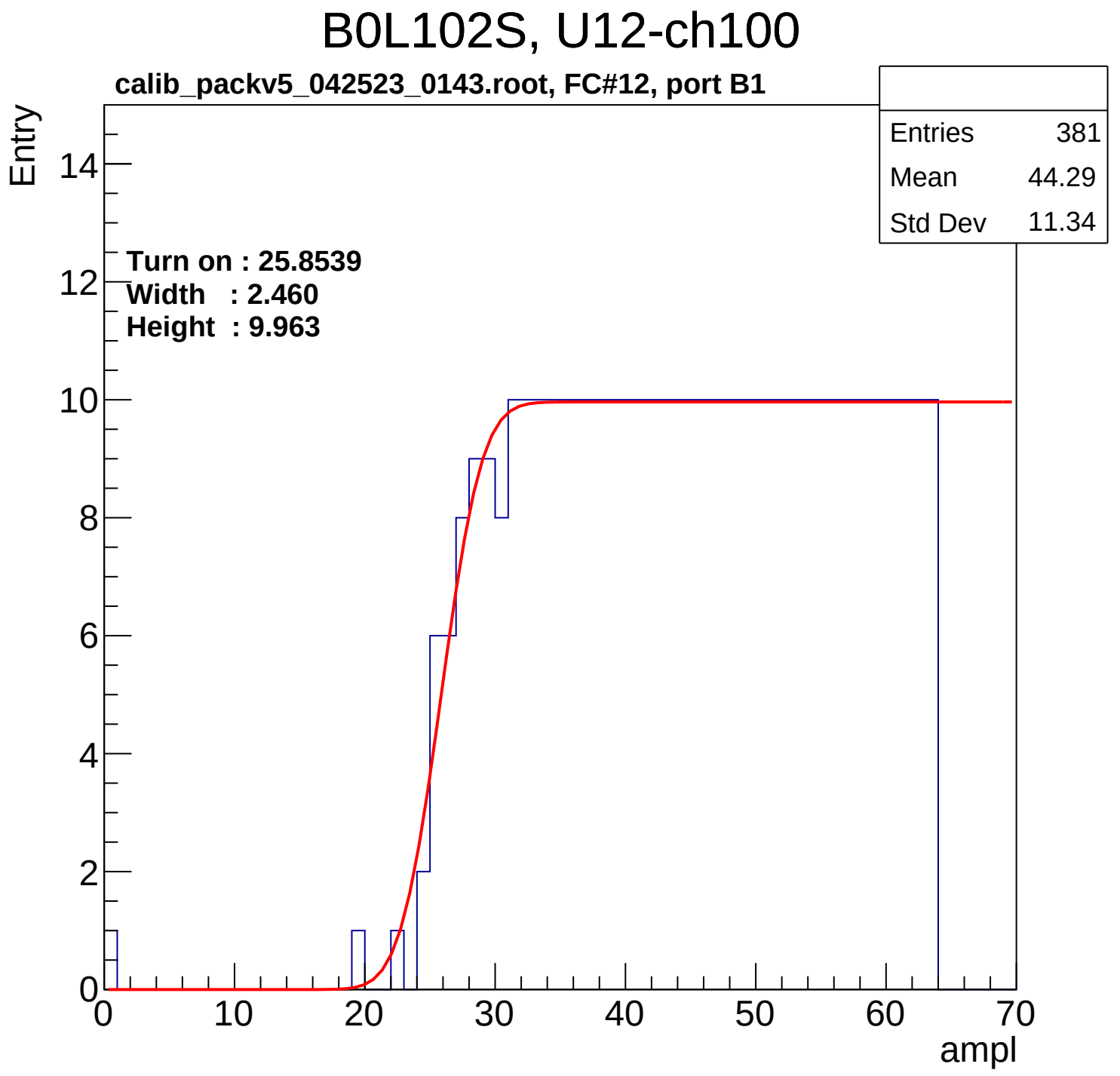
B0L102S, U12-ch100
calib_packv5_042523_0143.root, FC#12, port B1
Entries 381
Mean 44.29
Std Dev 11.34
Turn on : 25.8539
Width : 2.460
Height : 9.963
Entry
ampl
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6
8
10
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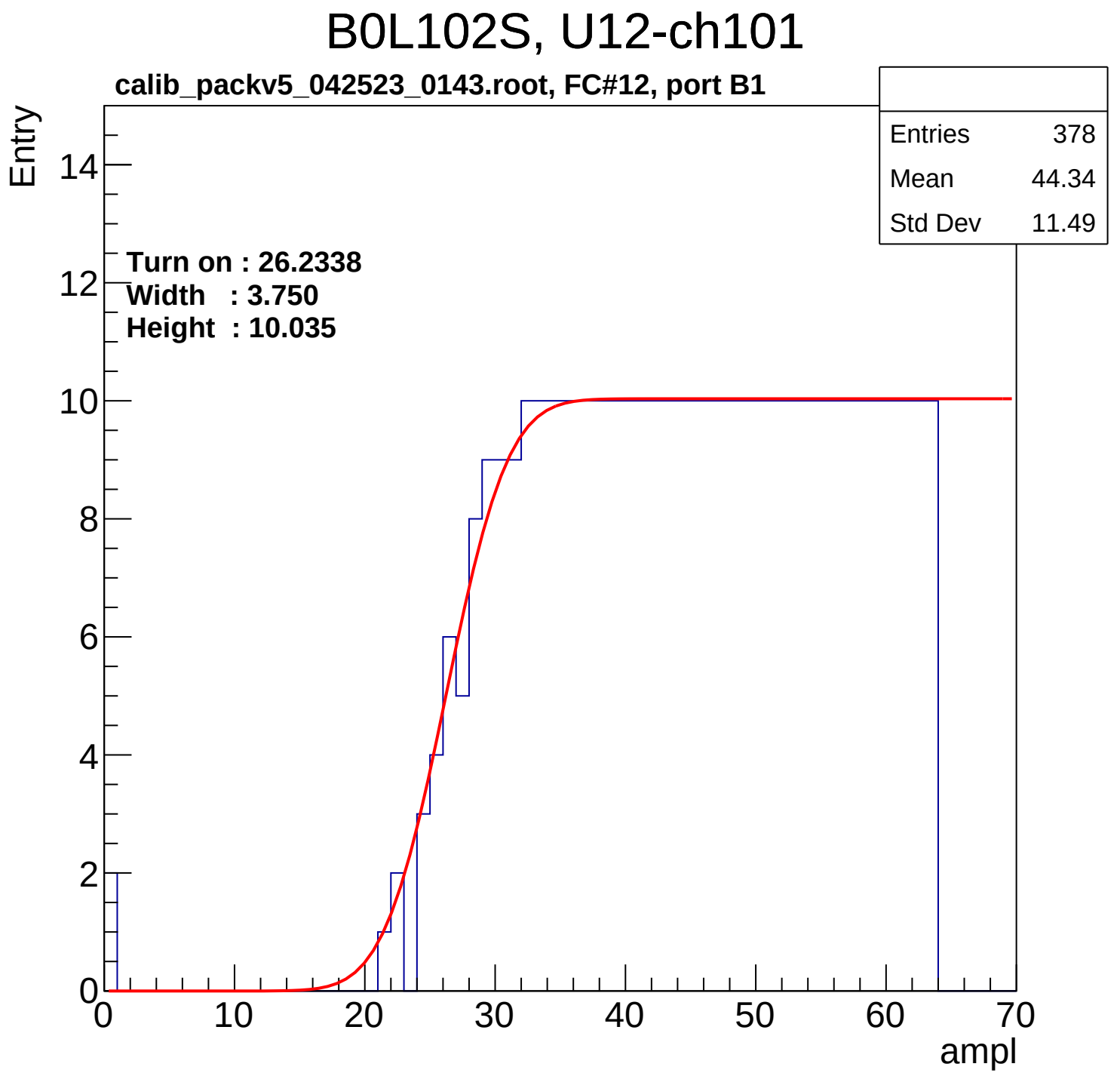
B0L102S, U12-ch101
calib_packv5_042523_0143.root, FC#12, port B1
Entries 378
Mean 44.34
Std Dev 11.49
Turn on : 26.2338
Width : 3.750
Height : 10.035
Entry
ampl
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6
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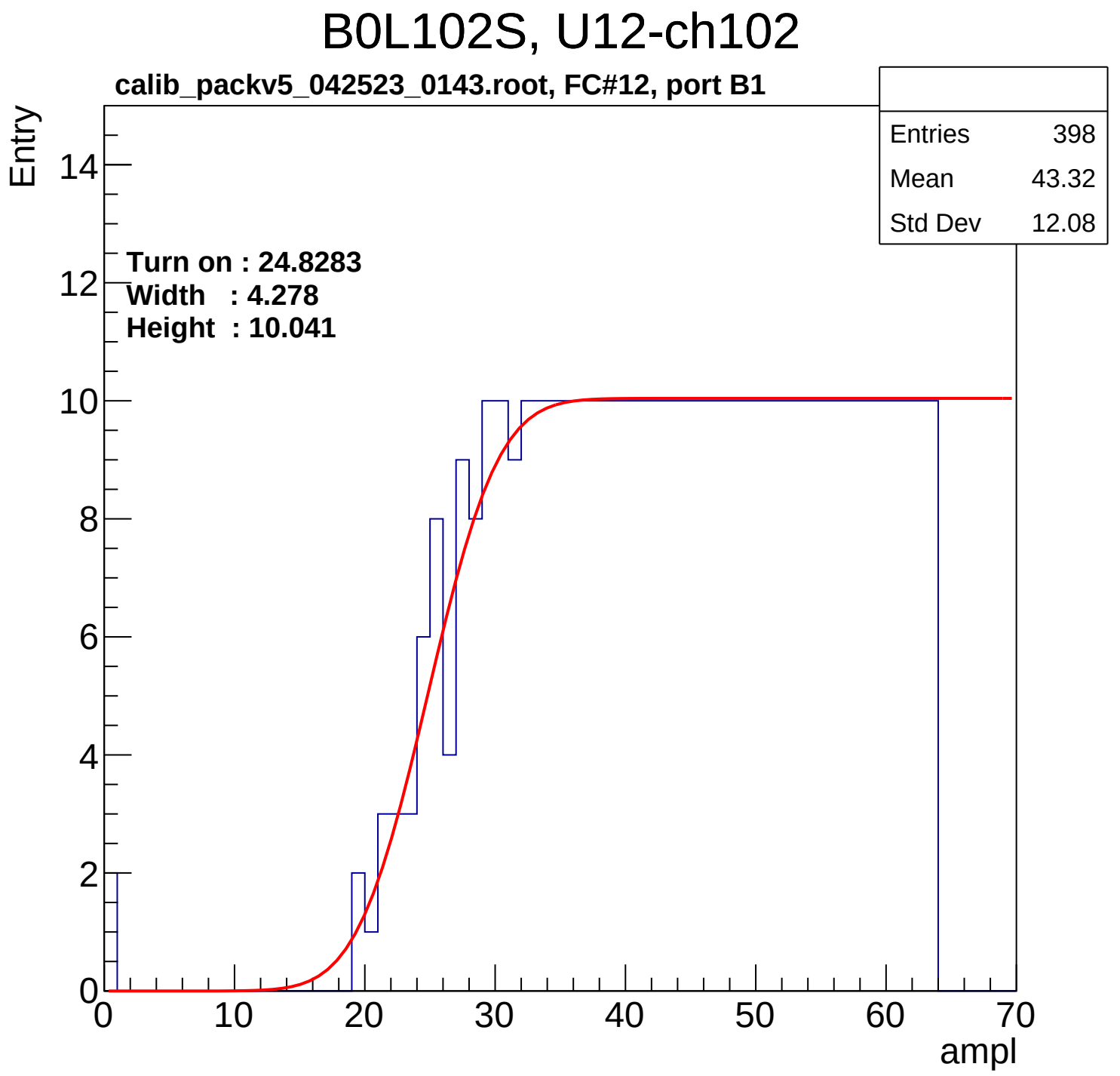
B0L102S, U12-ch102
calib_packv5_042523_0143.root, FC#12, port B1
Entries 398
Mean 43.32
Std Dev 12.08
Turn on : 24.8283
Width : 4.278
Height : 10.041
Entry
ampl
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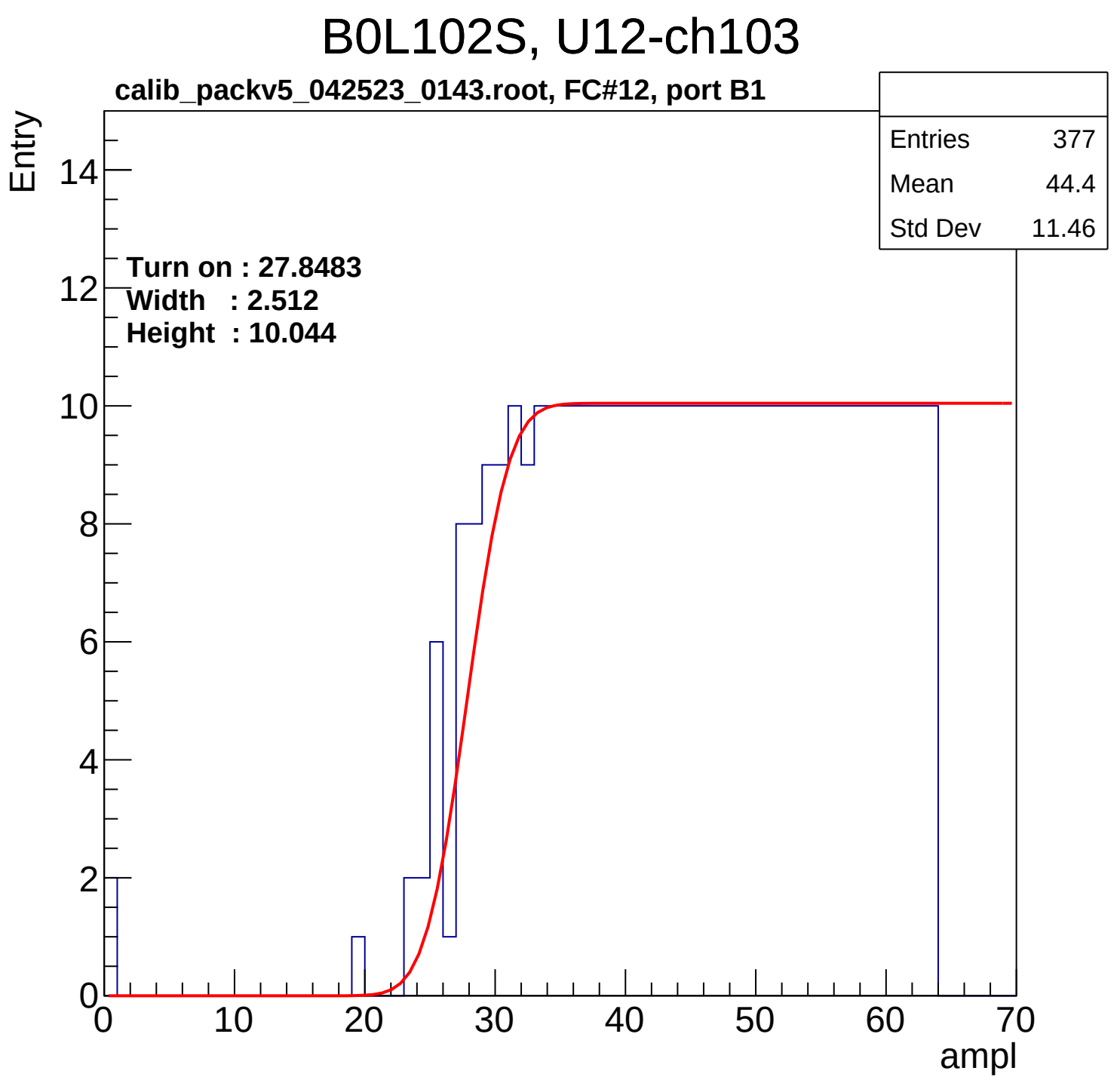
B0L102S, U12-ch103
calib_packv5_042523_0143.root, FC#12, port B1
Entries 377
Mean 44.4
Std Dev 11.46
Turn on : 27.8483
Width : 2.512
Height : 10.044
Entry
ampl
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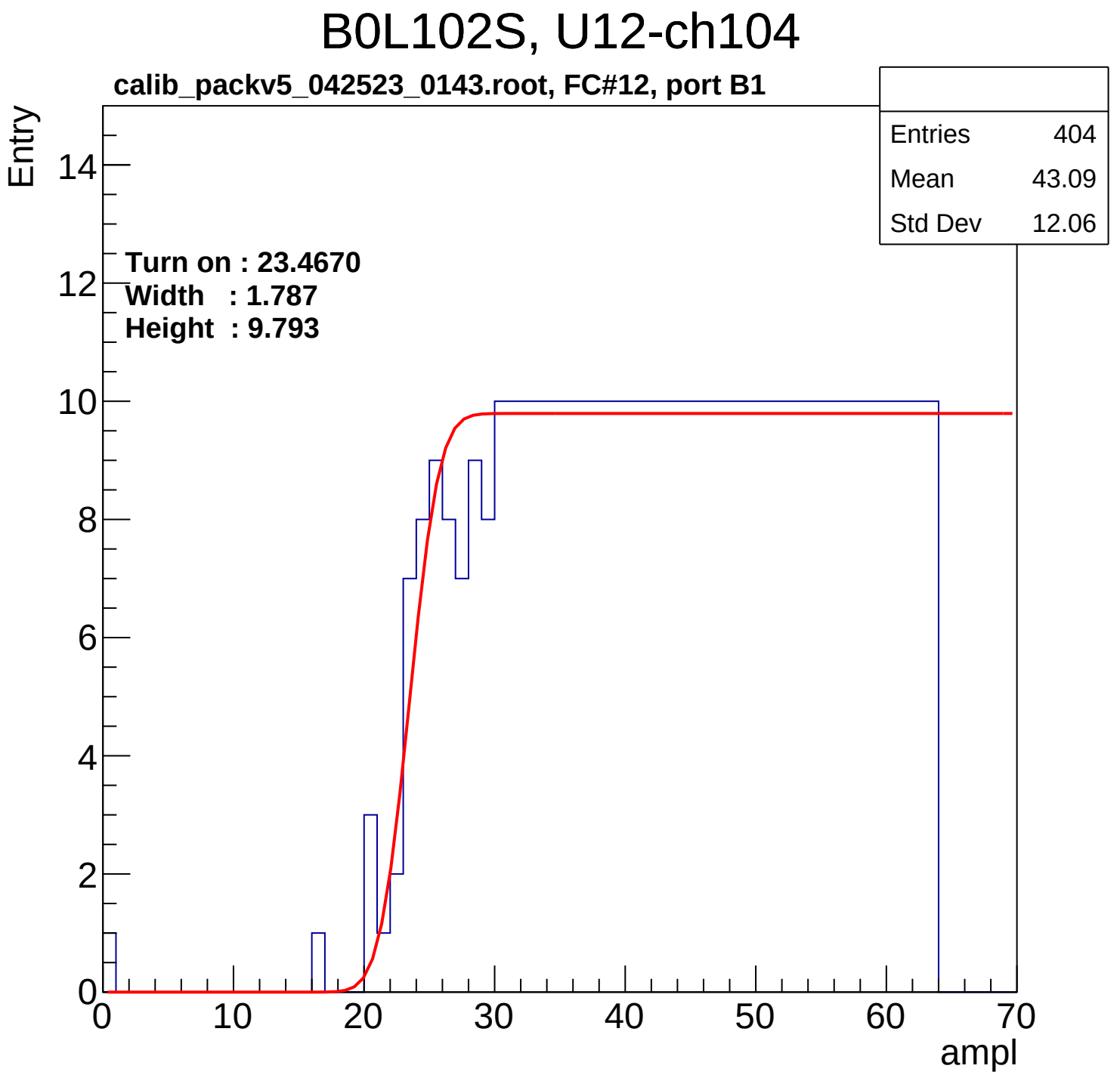
B0L102S, U12-ch104
calib_packv5_042523_0143.root, FC#12, port B1
Entries 404
Mean 43.09
Std Dev 12.06
Turn on : 23.4670
Width : 1.787
Height : 9.793
Entry
ampl
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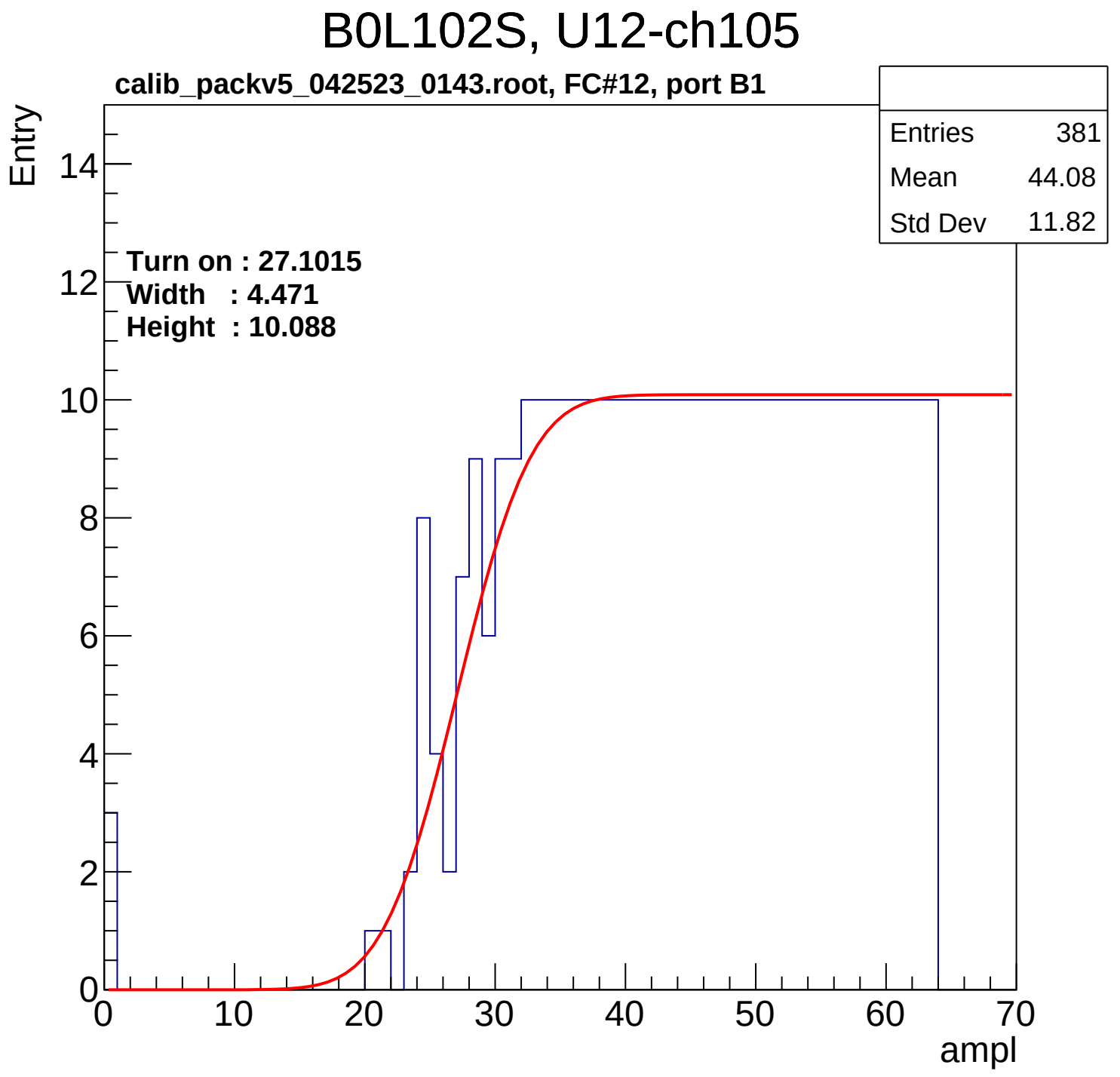
B0L102S, U12-ch105
calib_packv5_042523_0143.root, FC#12, port B1
Entries 381
Mean 44.08
Std Dev 11.82
Turn on : 27.1015
Width : 4.471
Height : 10.088
Entry
ampl
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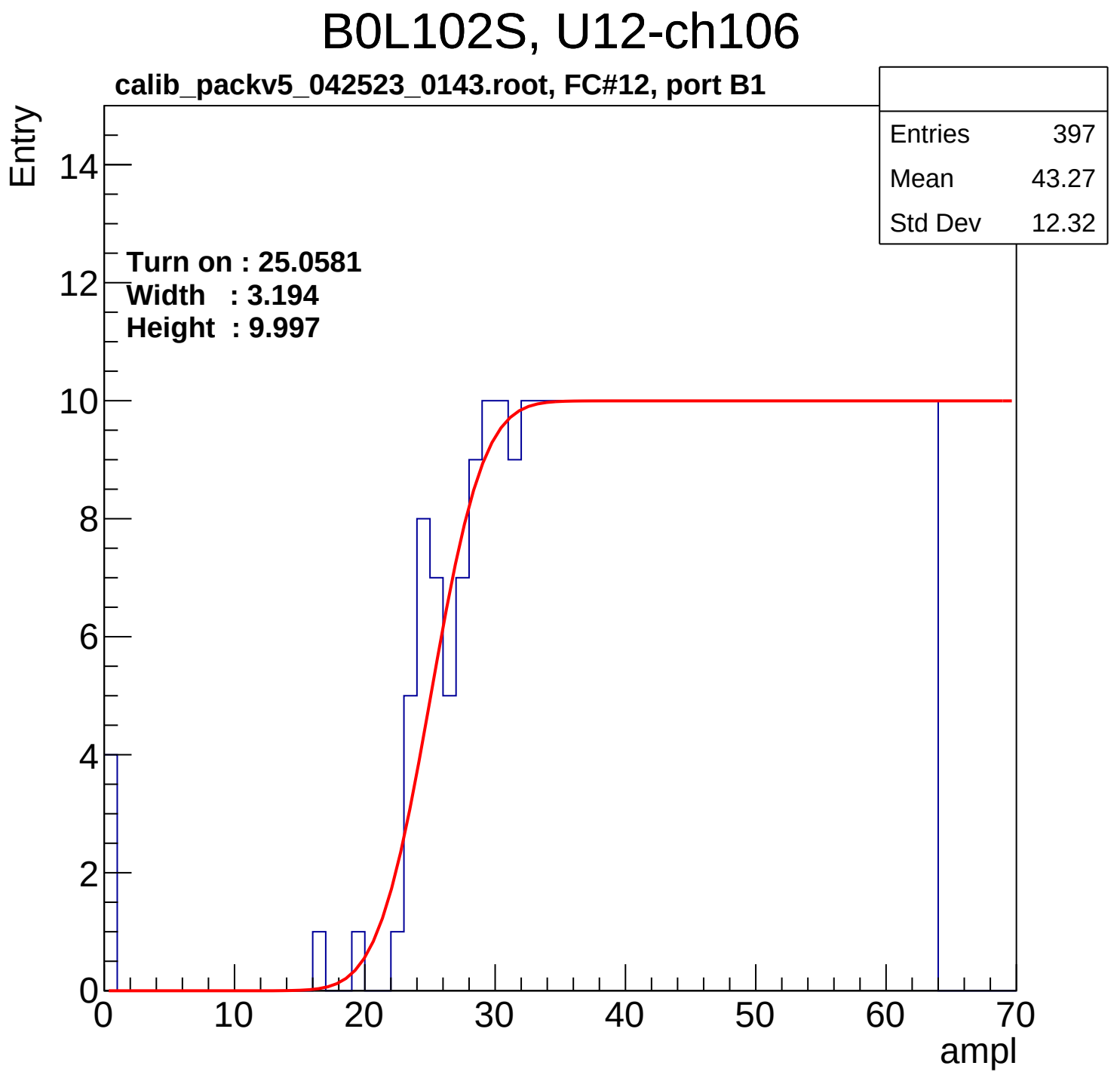
B0L102S, U12-ch106
calib_packv5_042523_0143.root, FC#12, port B1
Entries 397
Mean 43.27
Std Dev 12.32
Turn on : 25.0581
Width : 3.194
Height : 9.997
Entry
ampl
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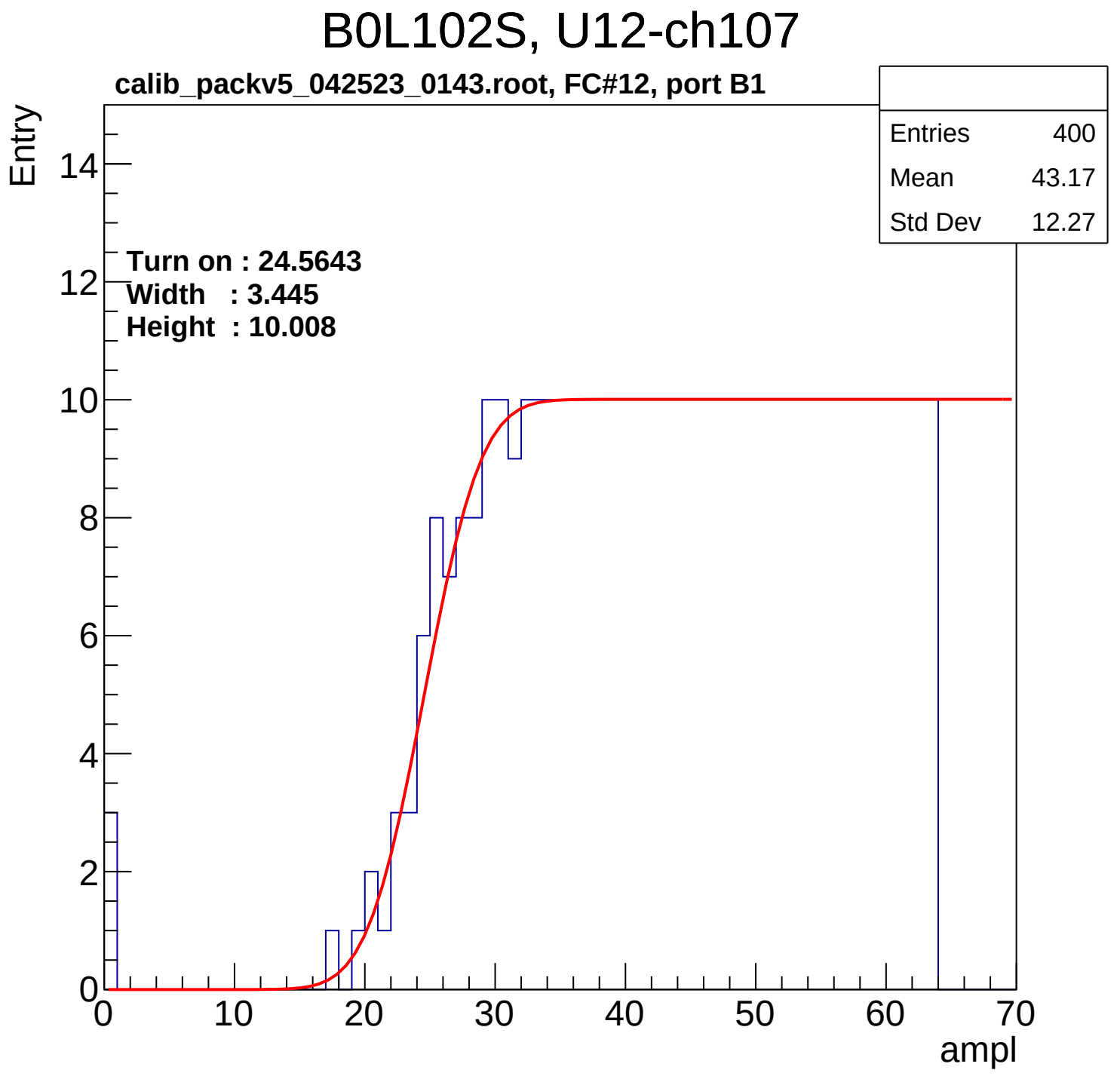
B0L102S, U12-ch107
calib_packv5_042523_0143.root, FC#12, port B1
Entries 400
Mean 43.17
Std Dev 12.27
Turn on : 24.5643
Width : 3.445
Height : 10.008
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ampl
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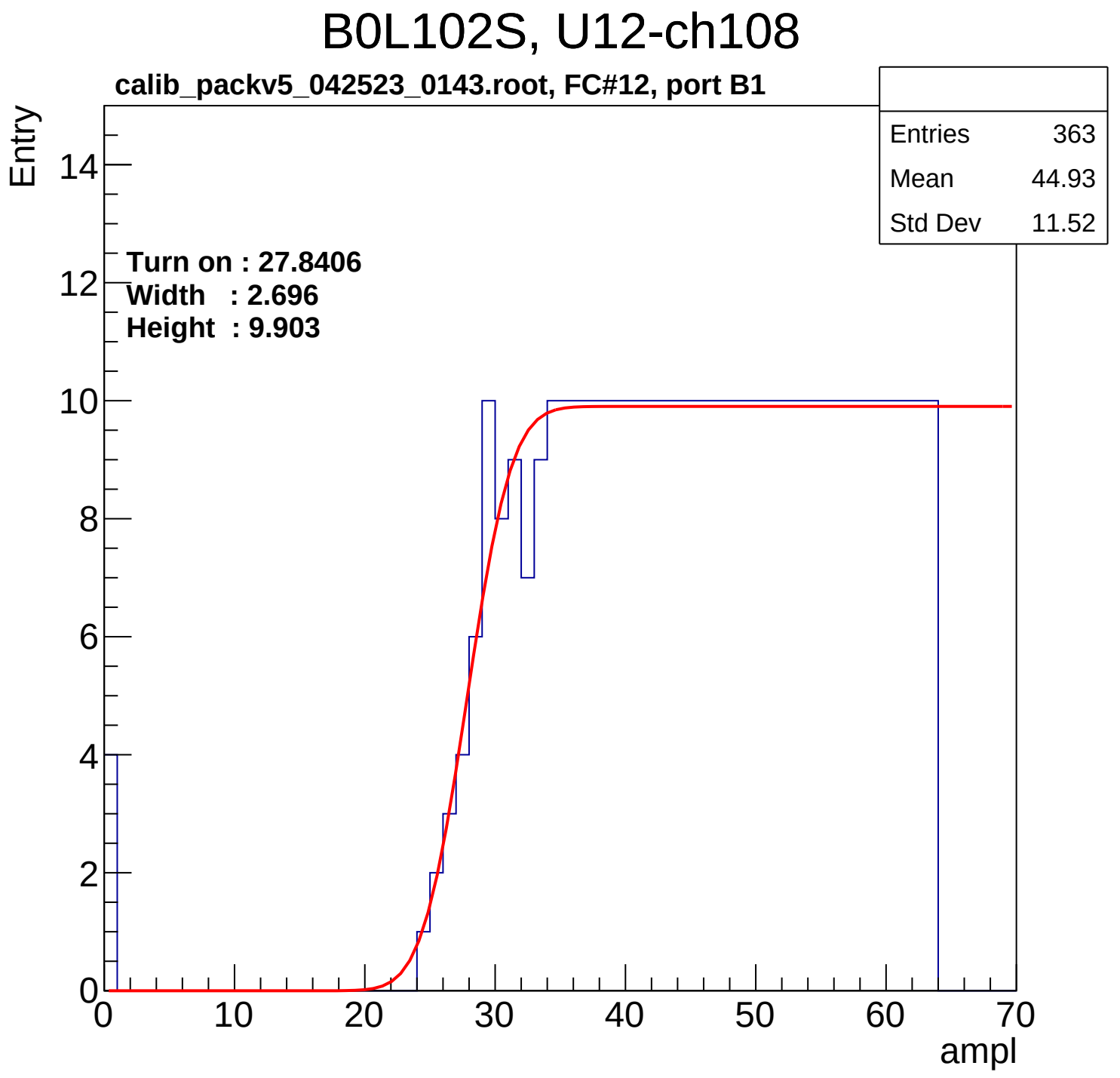
B0L102S, U12-ch108
calib_packv5_042523_0143.root, FC#12, port B1
Entries 363
Mean 44.93
Std Dev 11.52
Turn on : 27.8406
Width : 2.696
Height : 9.903
Entry
ampl
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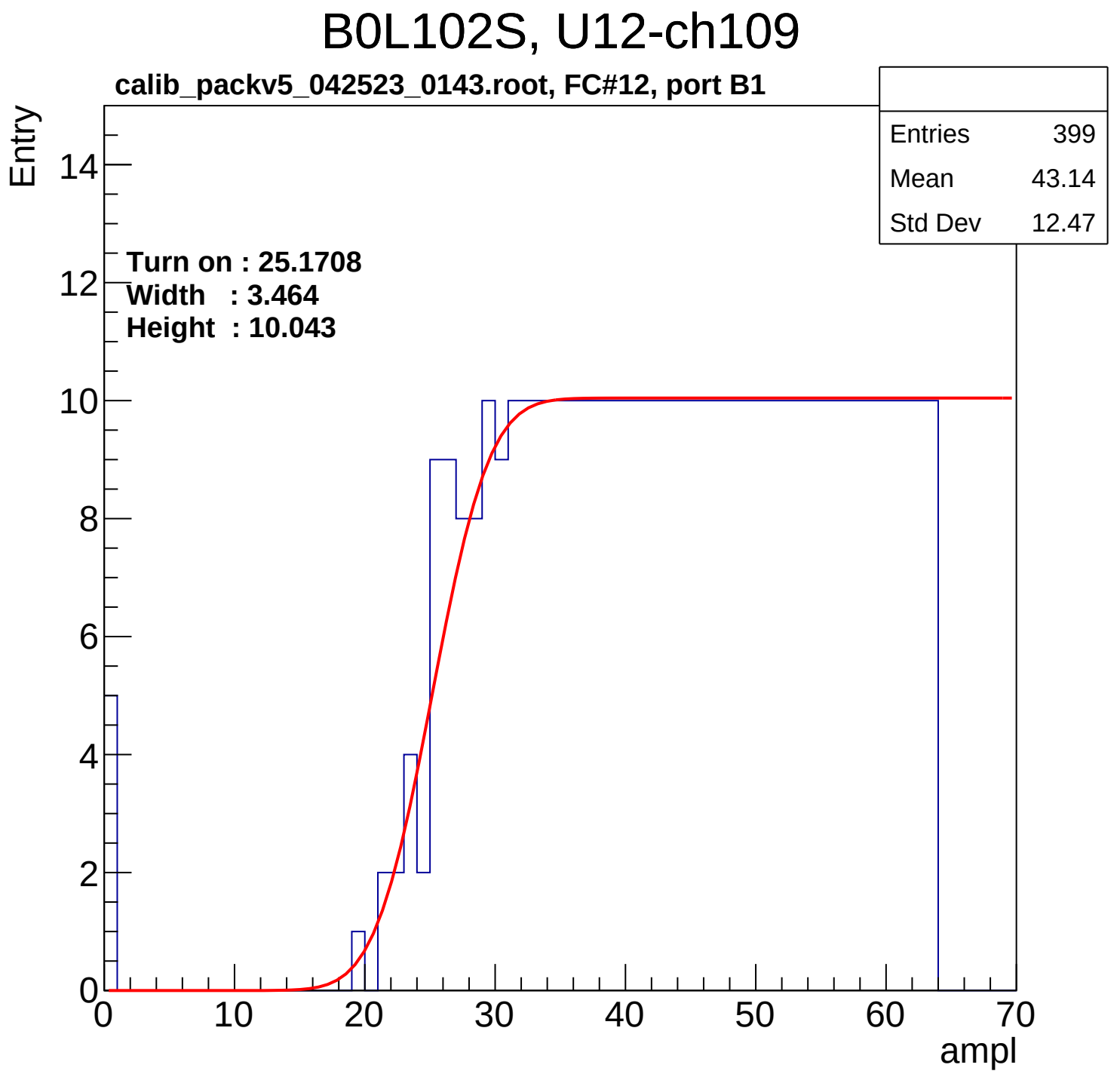
B0L102S, U12-ch109
calib_packv5_042523_0143.root, FC#12, port B1
Entries 399
Mean 43.14
Std Dev 12.47
Turn on : 25.1708
Width : 3.464
Height : 10.043
Entry
ampl
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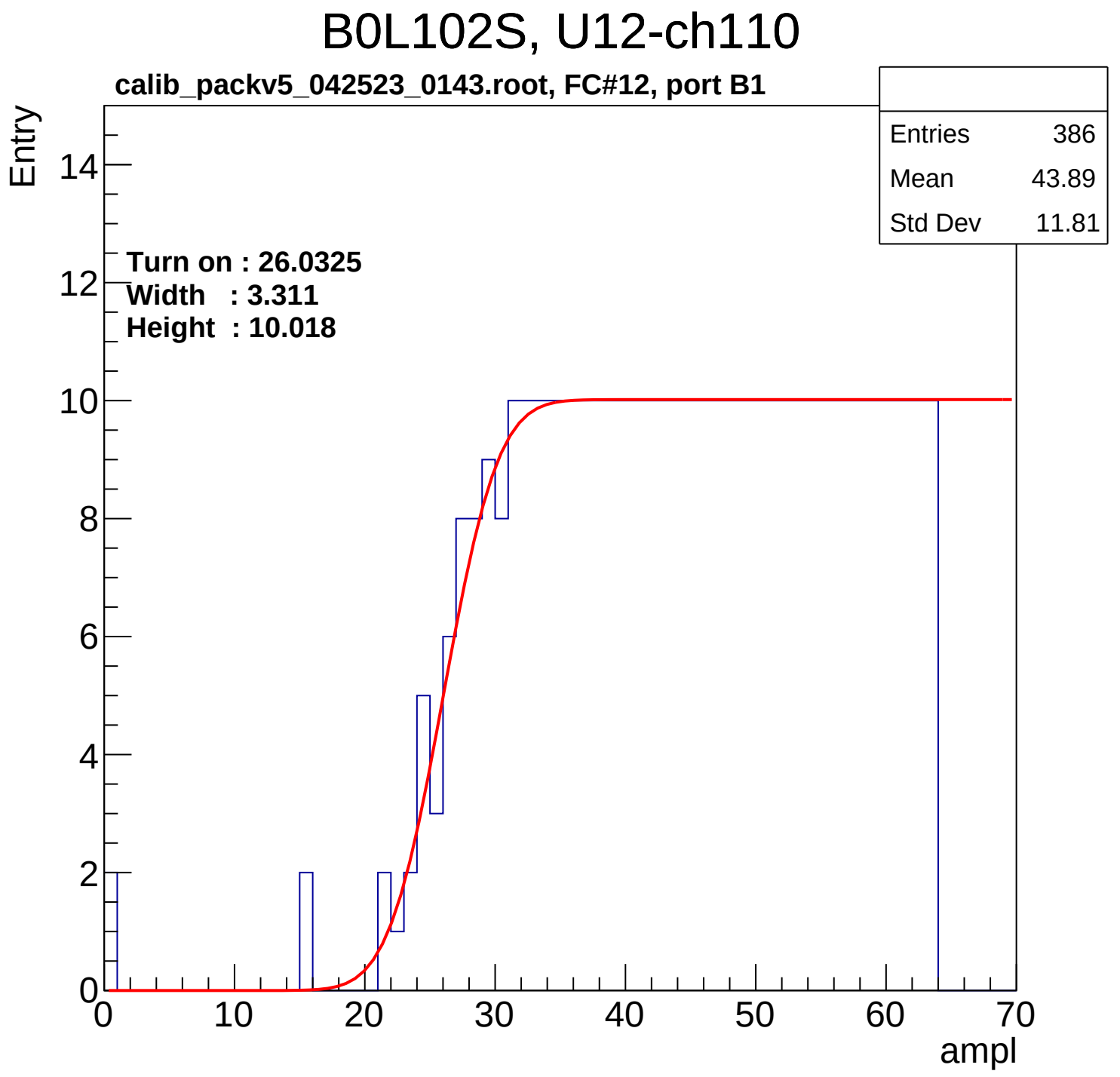
B0L102S, U12-ch110
calib_packv5_042523_0143.root, FC#12, port B1
Entries 386
Mean 43.89
Std Dev 11.81
Turn on : 26.0325
Width : 3.311
Height : 10.018
Entry
ampl
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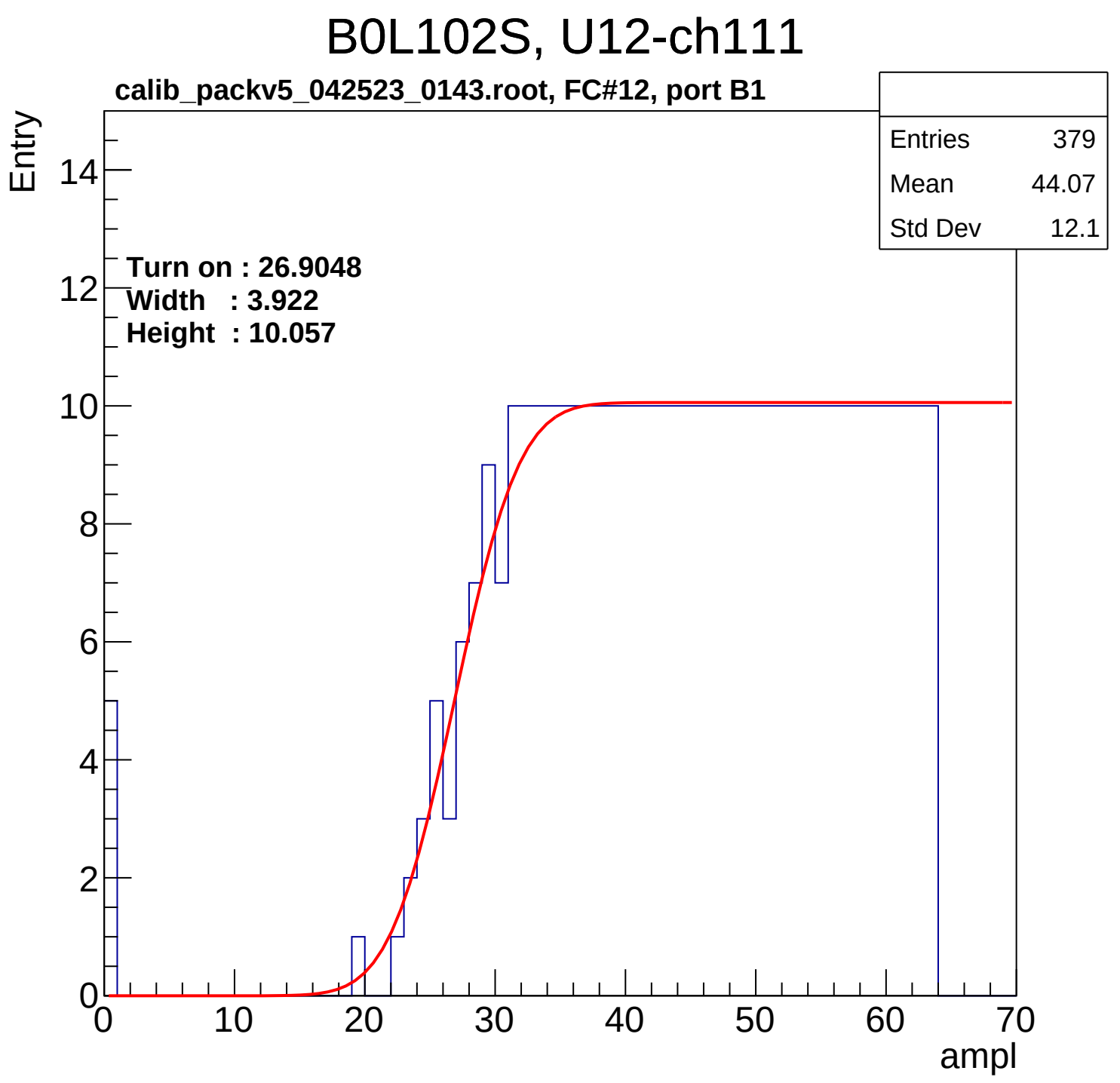
B0L102S, U12-ch111
calib_packv5_042523_0143.root, FC#12, port B1
Entries 379
Mean 44.07
Std Dev 12.1
Turn on : 26.9048
Width : 3.922
Height : 10.057
Entry
ampl
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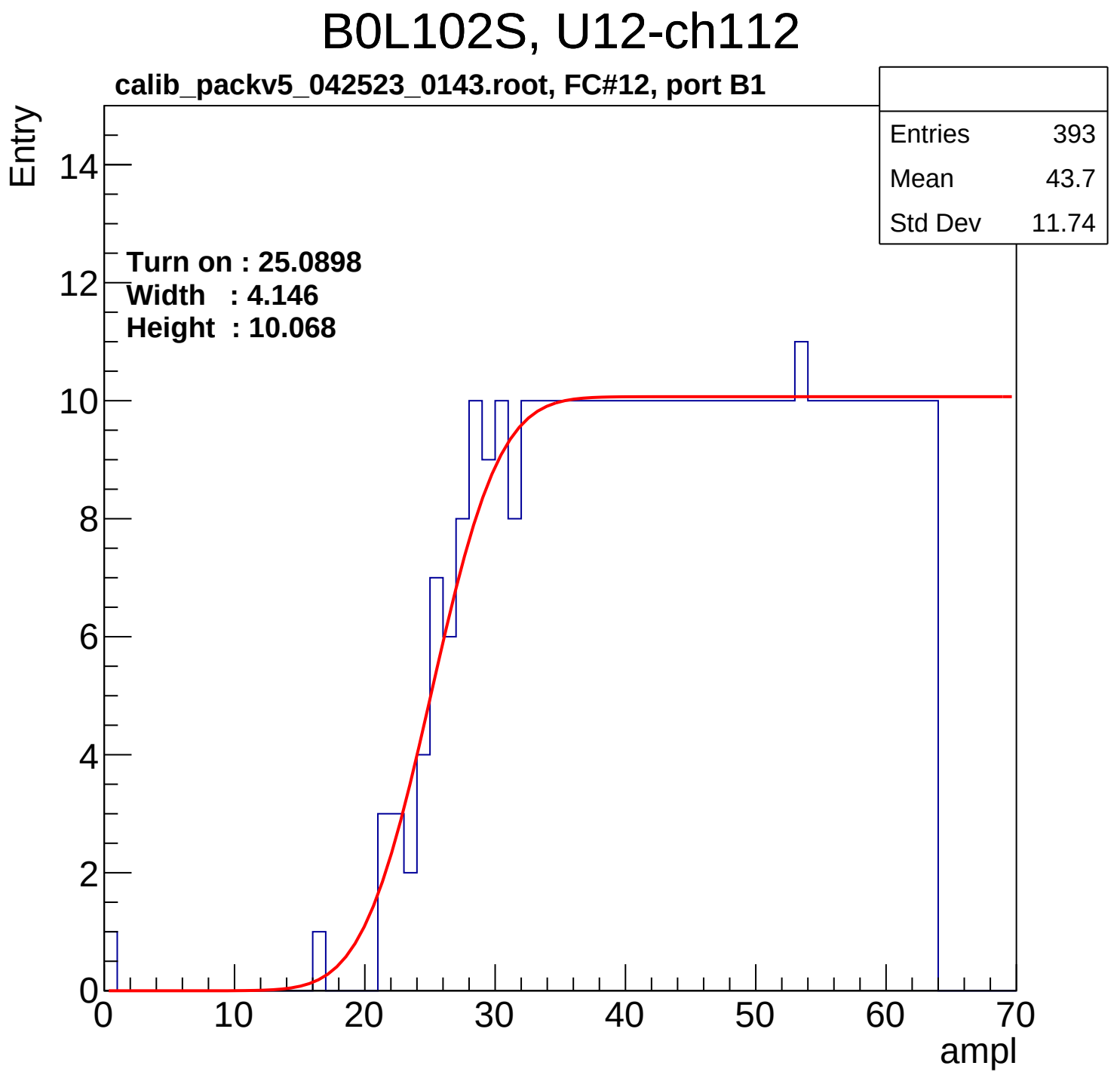
B0L102S, U12-ch112
calib_packv5_042523_0143.root, FC#12, port B1
Entries 393
Mean 43.7
Std Dev 11.74
Turn on : 25.0898
Width : 4.146
Height : 10.068
Entry
ampl
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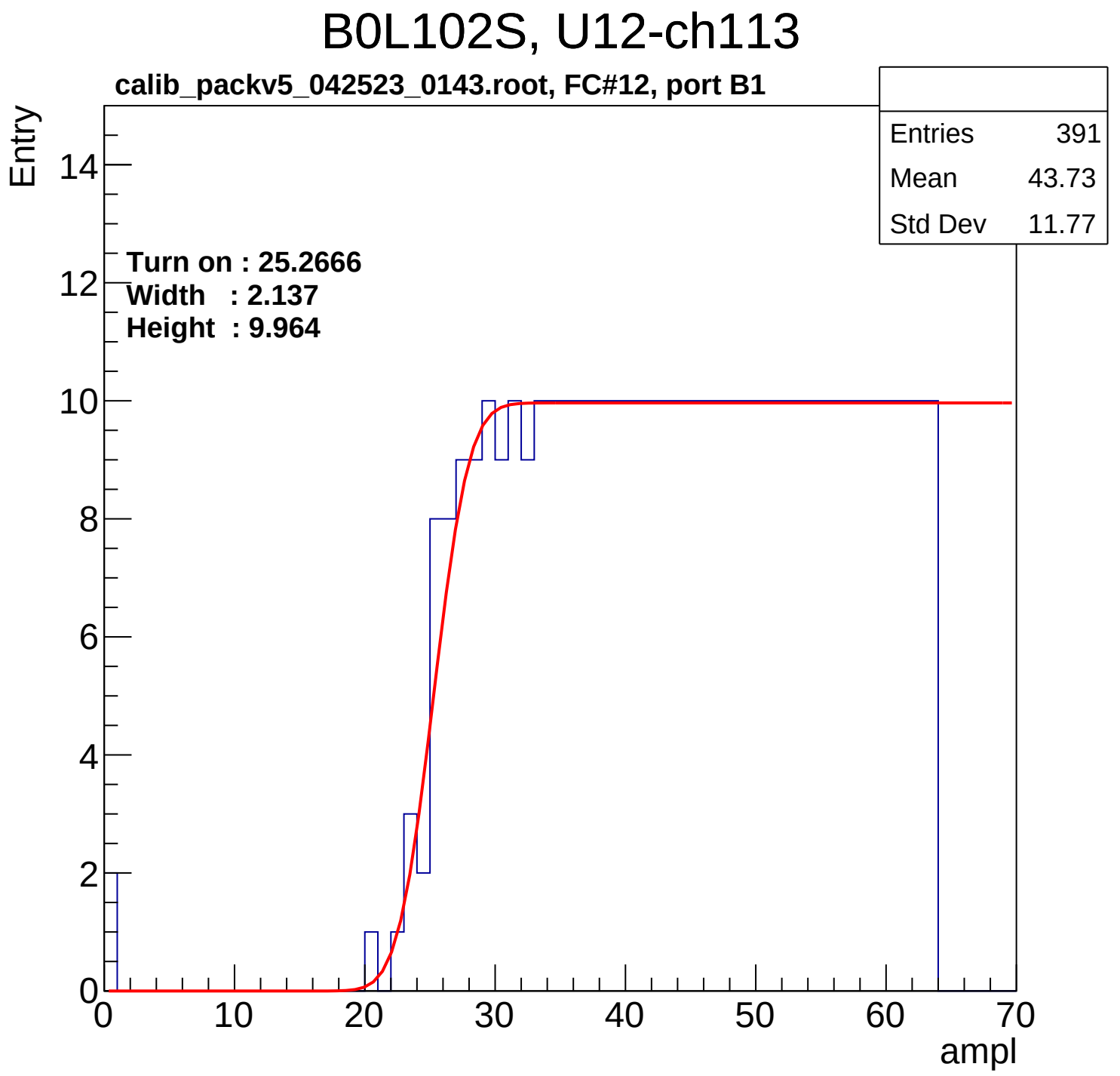
B0L102S, U12-ch113
calib_packv5_042523_0143.root, FC#12, port B1
Entries 391
Mean 43.73
Std Dev 11.77
Turn on : 25.2666
Width : 2.137
Height : 9.964
Entry
ampl
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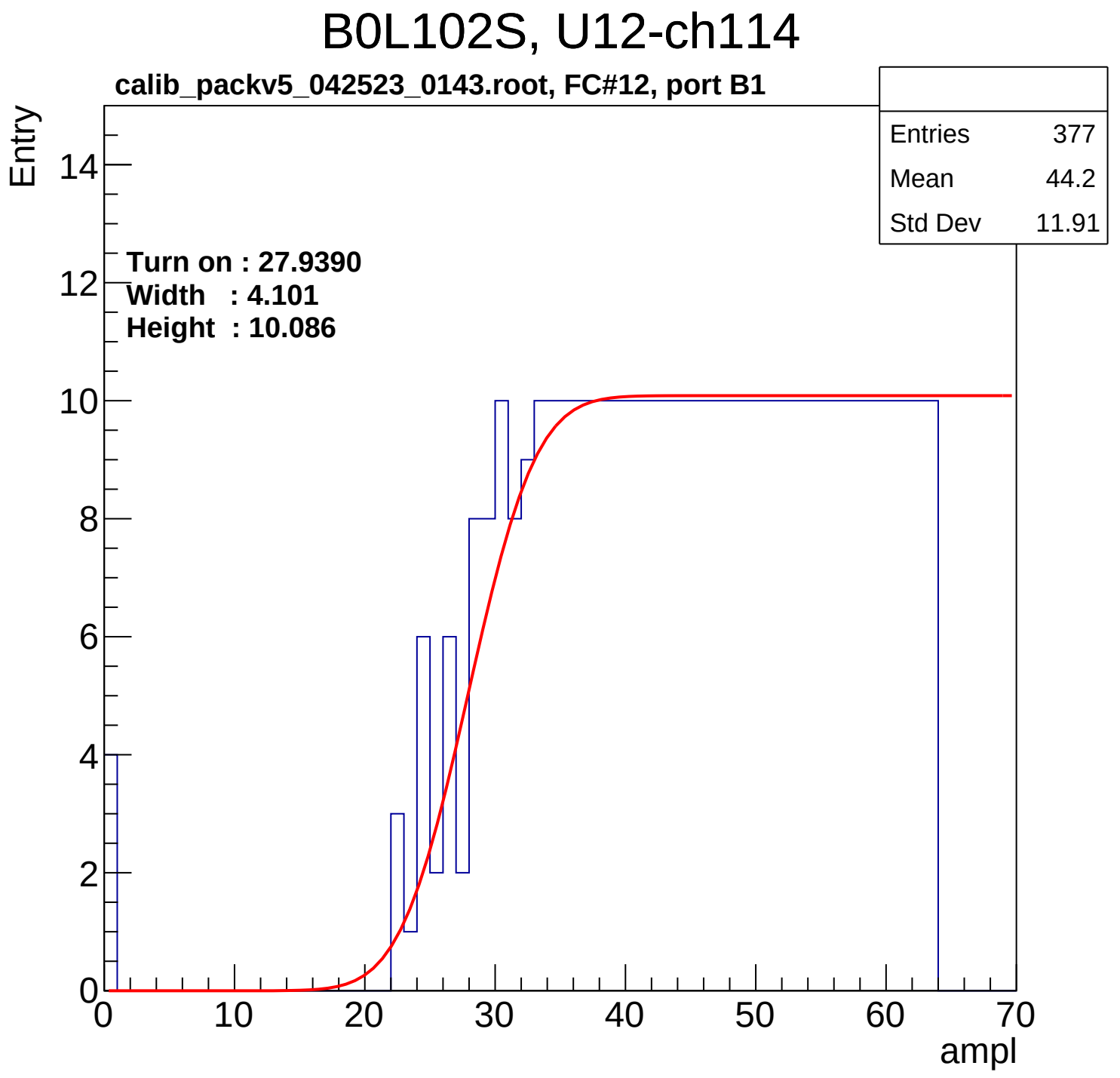
B0L102S, U12-ch114
calib_packv5_042523_0143.root, FC#12, port B1
Entries 377
Mean 44.2
Std Dev 11.91
Turn on : 27.9390
Width : 4.101
Height : 10.086
Entry
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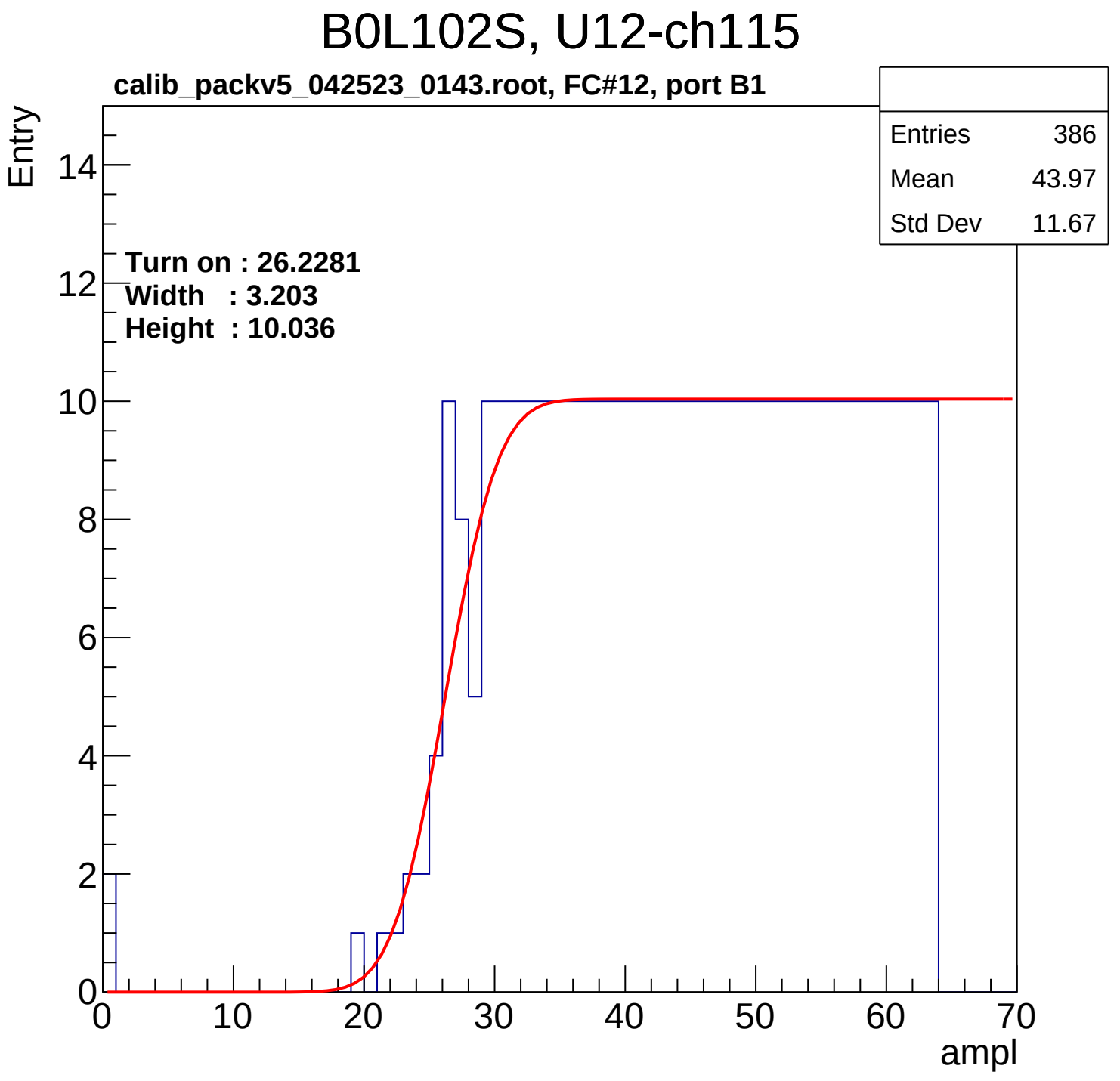
B0L102S, U12-ch115
calib_packv5_042523_0143.root, FC#12, port B1
Entries 386
Mean 43.97
Std Dev 11.67
Turn on : 26.2281
Width : 3.203
Height : 10.036
Entry
ampl
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6
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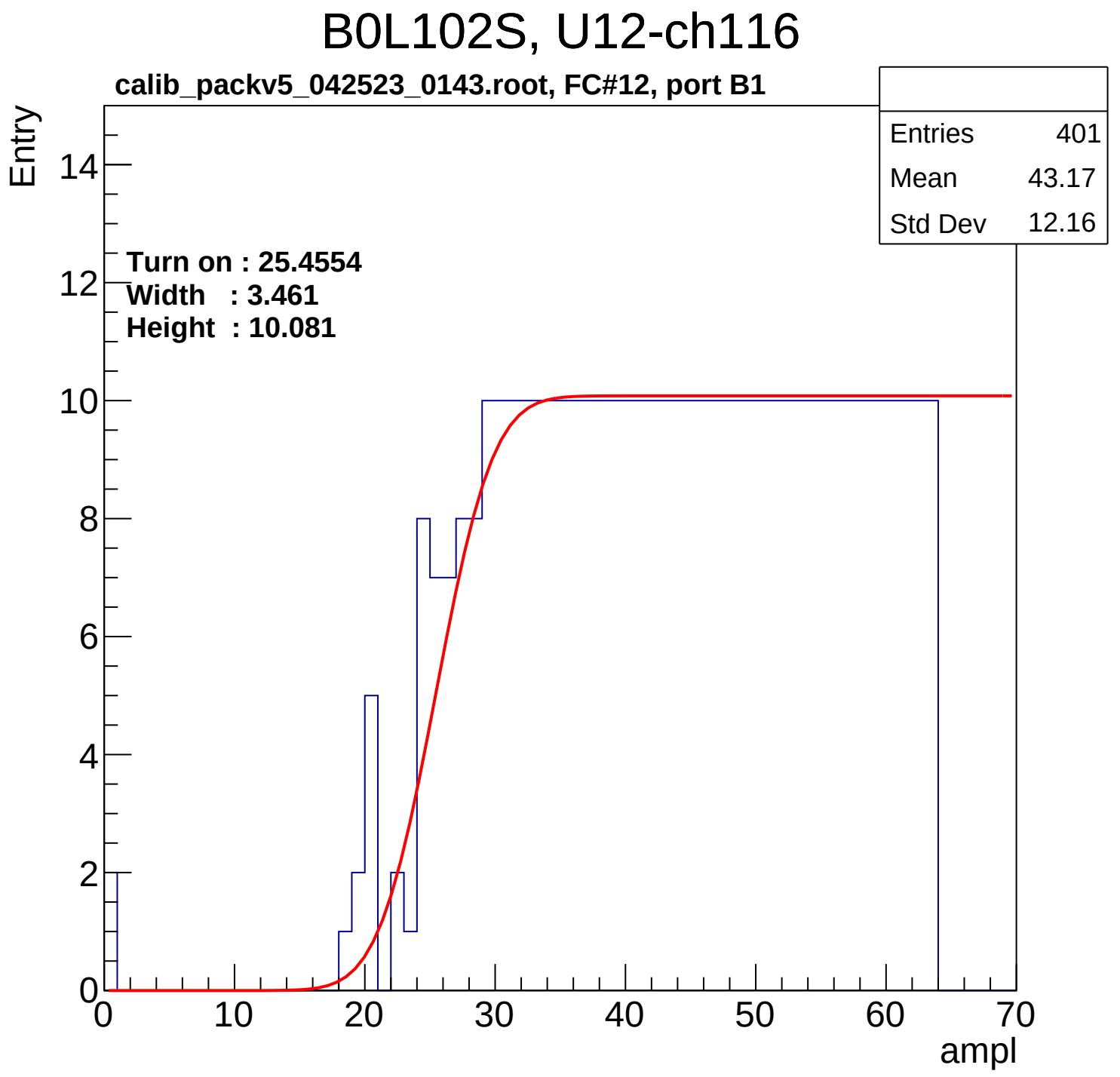
B0L102S, U12-ch116
calib_packv5_042523_0143.root, FC#12, port B1
Entries 401
Mean 43.17
Std Dev 12.16
Turn on : 25.4554
Width : 3.461
Height : 10.081
Entry
ampl
0
2
4
6
8
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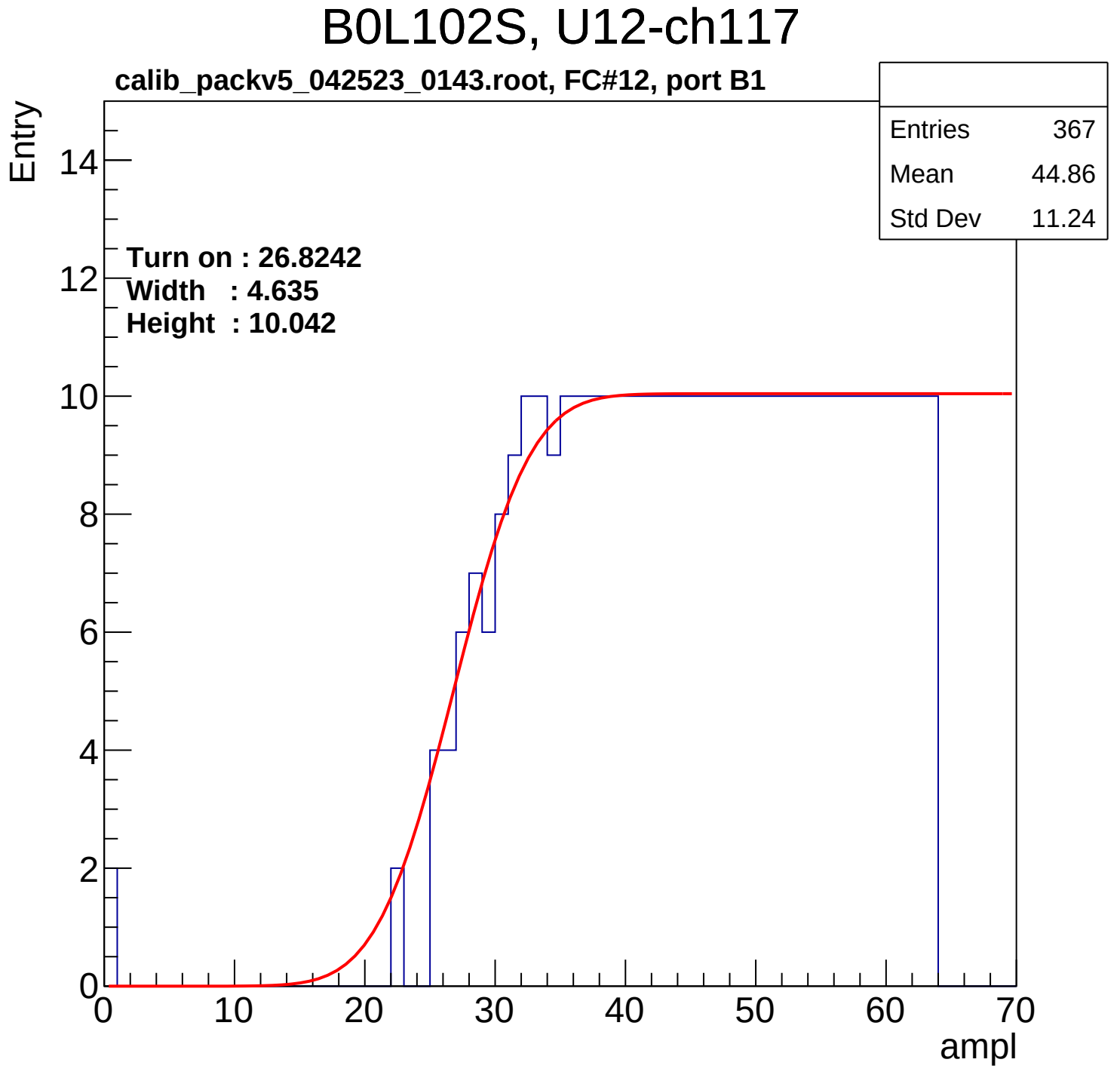
B0L102S, U12-ch117
calib_packv5_042523_0143.root, FC#12, port B1
Entries 367
Mean 44.86
Std Dev 11.24
Turn on : 26.8242
Width : 4.635
Height : 10.042
Entry
ampl
0
2
4
6
8
10
12
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0
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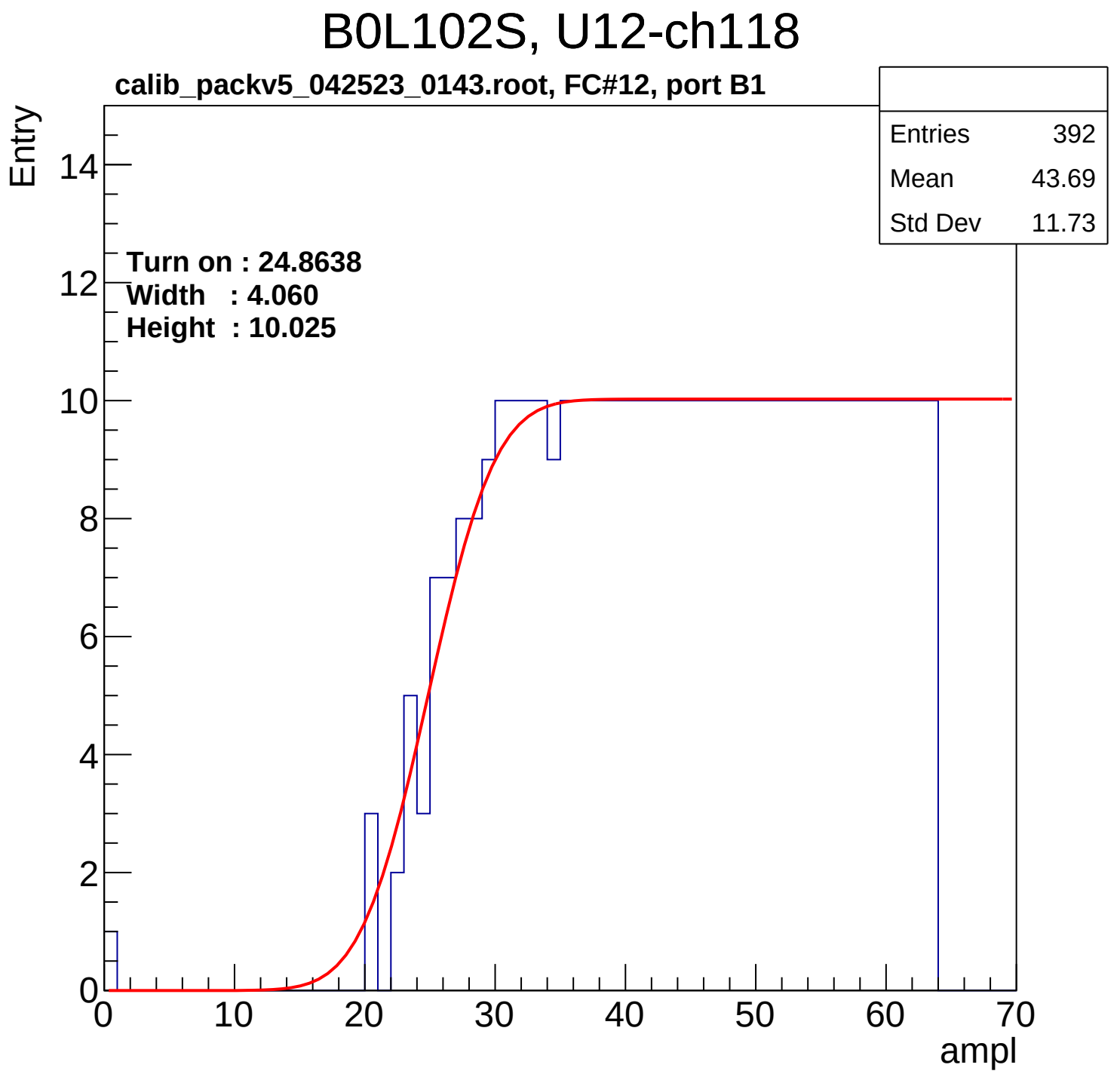
B0L102S, U12-ch118
calib_packv5_042523_0143.root, FC#12, port B1
Entries 392
Mean 43.69
Std Dev 11.73
Turn on : 24.8638
Width : 4.060
Height : 10.025
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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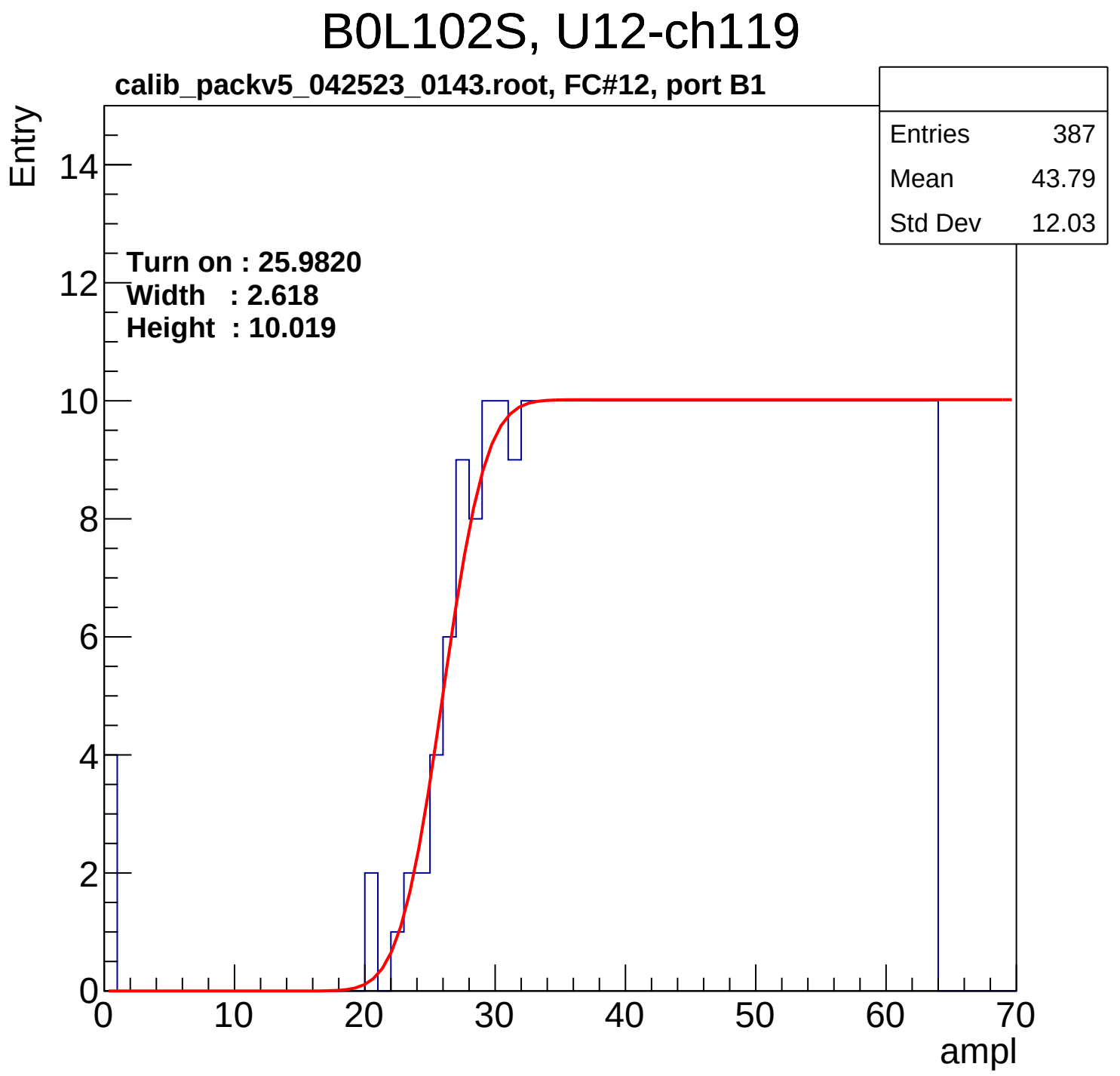
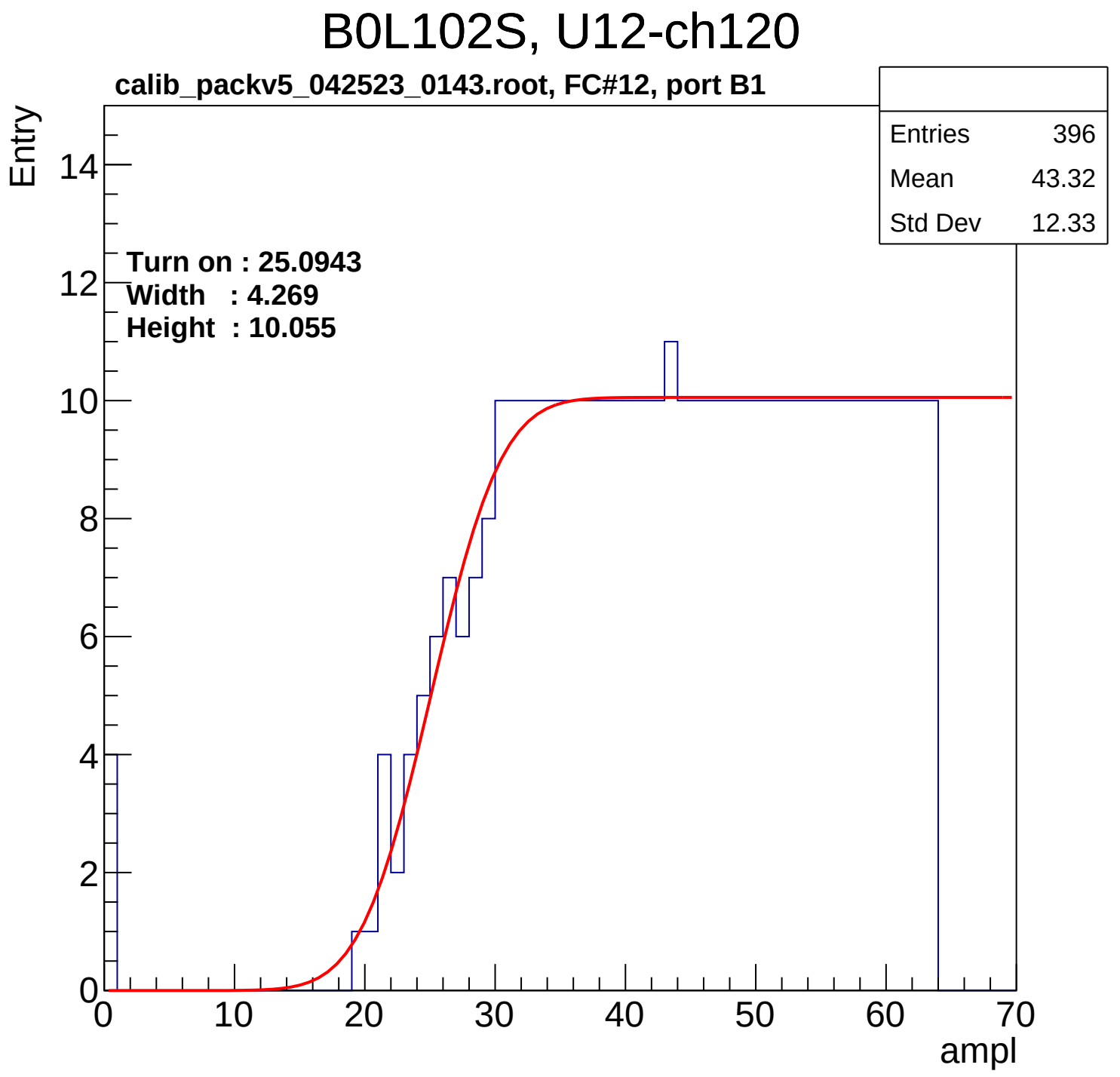

B0L102S, U12-ch119
calib_packv5_042523_0143.root, FC#12, port B1
Entries 387
Mean 43.79
Std Dev 12.03
Turn on : 25.9820
Width : 2.618
Height : 10.019
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L102S, U12-ch120
calib_packv5_042523_0143.root, FC#12, port B1
Entries 396
Mean 43.32
Std Dev 12.33
Turn on : 25.0943
Width : 4.269
Height : 10.055
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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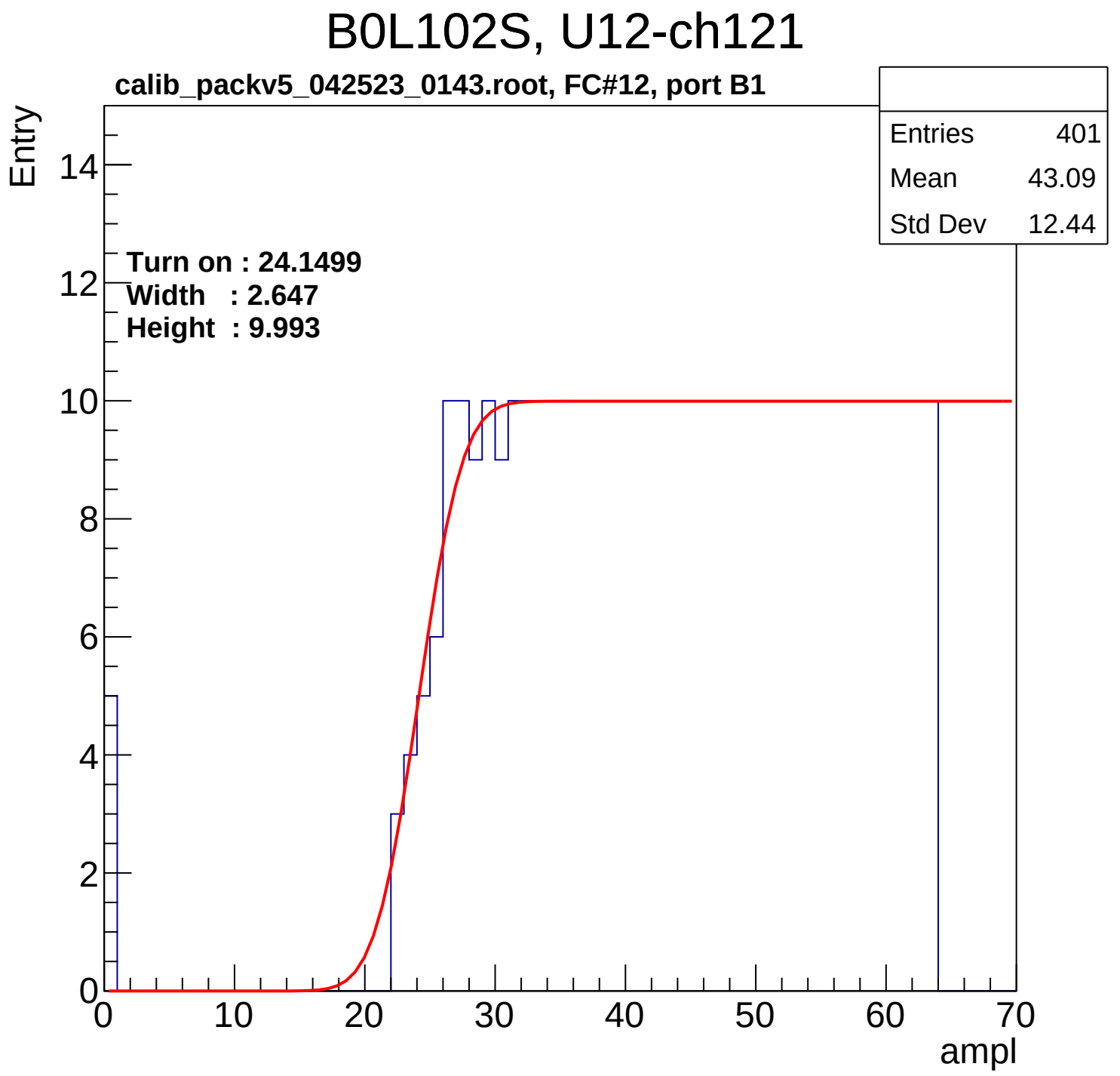
40
50
60
70


B0L102S, U12-ch121
calib_packv5_042523_0143.root, FC#12, port B1
Entries 401
Mean 43.09
Std Dev 12.44
Turn on : 24.1499
Width : 2.647
Height : 9.993
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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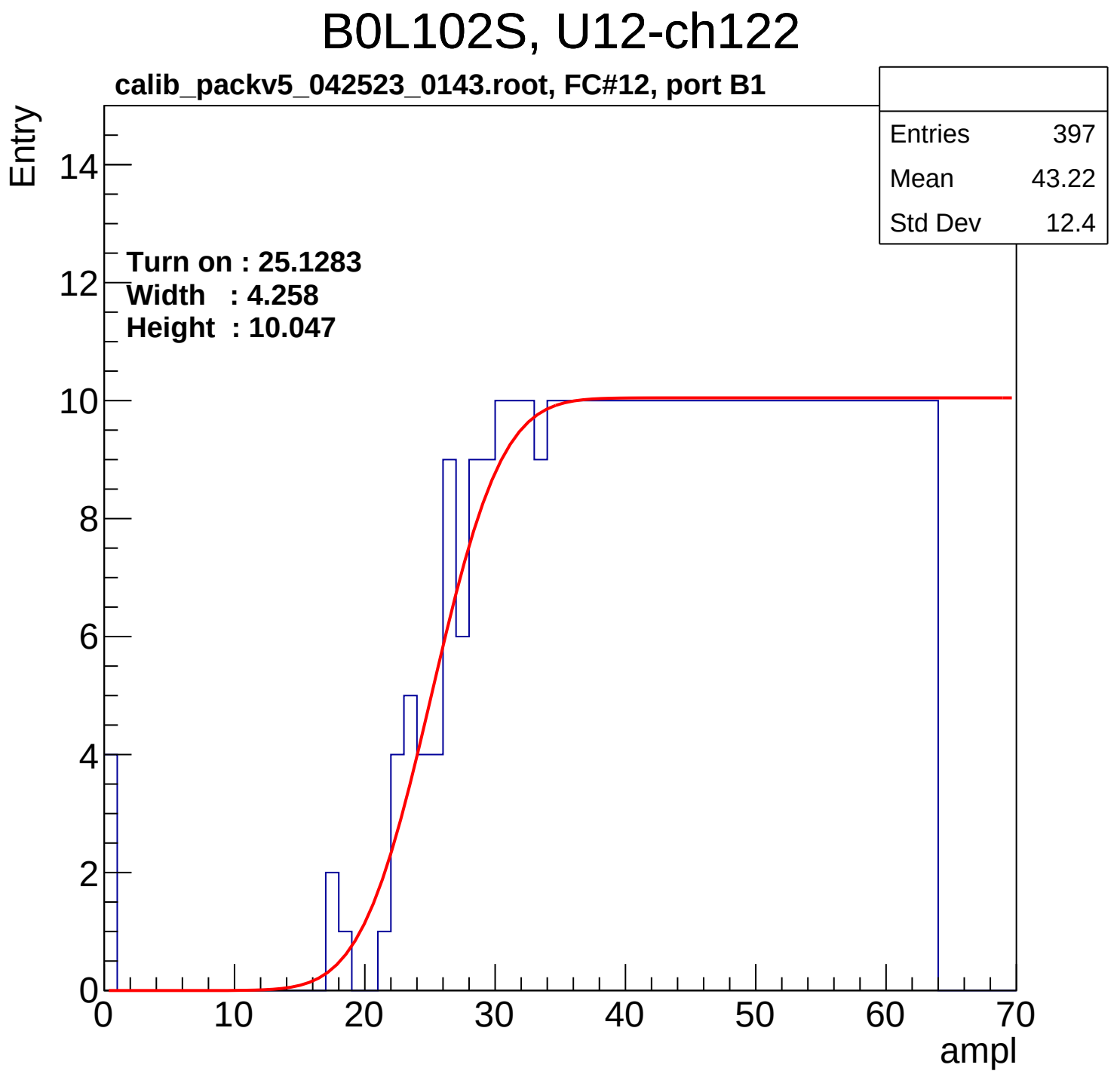
B0L102S, U12-ch122
calib_packv5_042523_0143.root, FC#12, port B1
Entries 397
Mean 43.22
Std Dev 12.4
Turn on : 25.1283
Width : 4.258
Height : 10.047
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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40
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60
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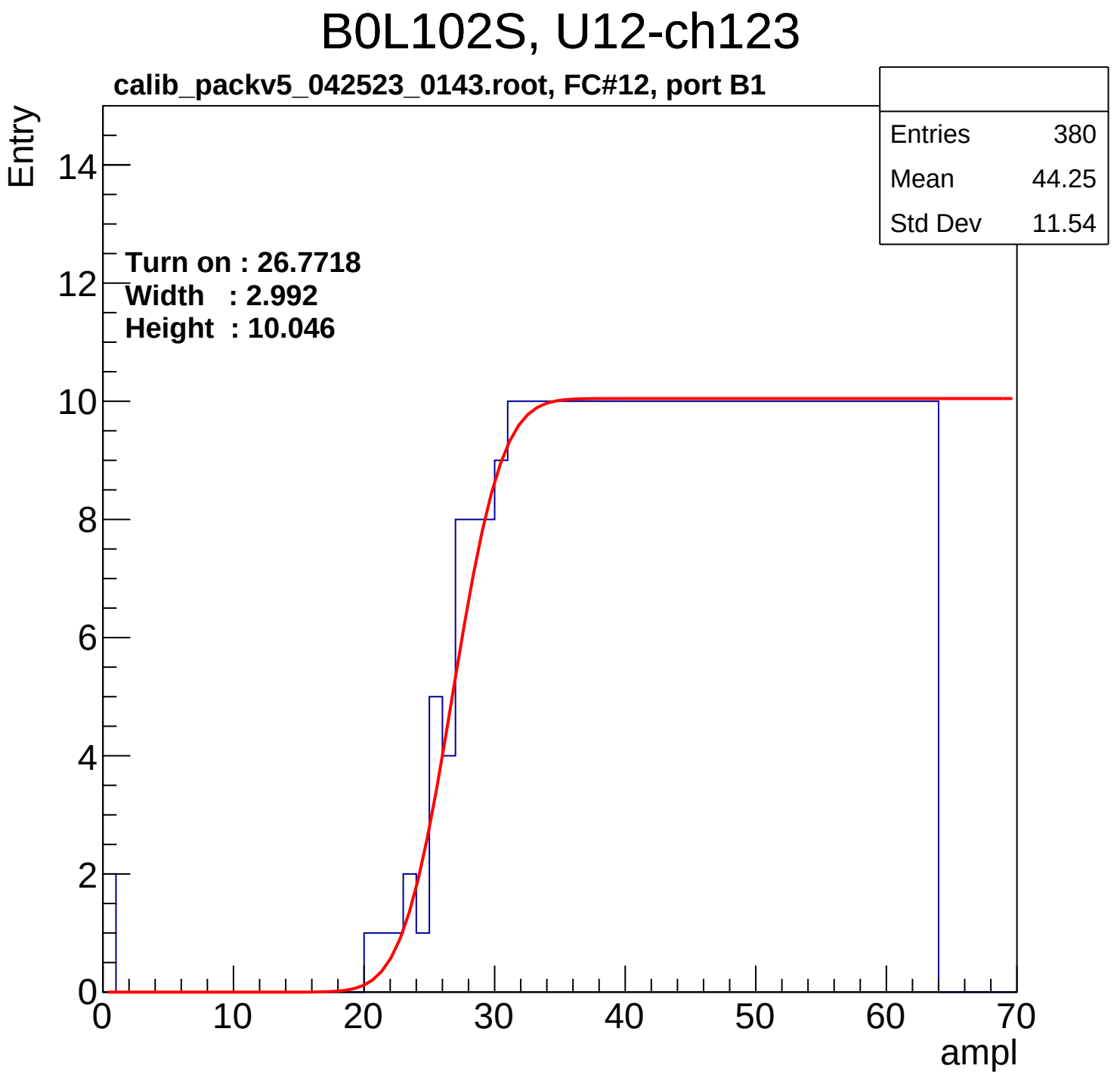
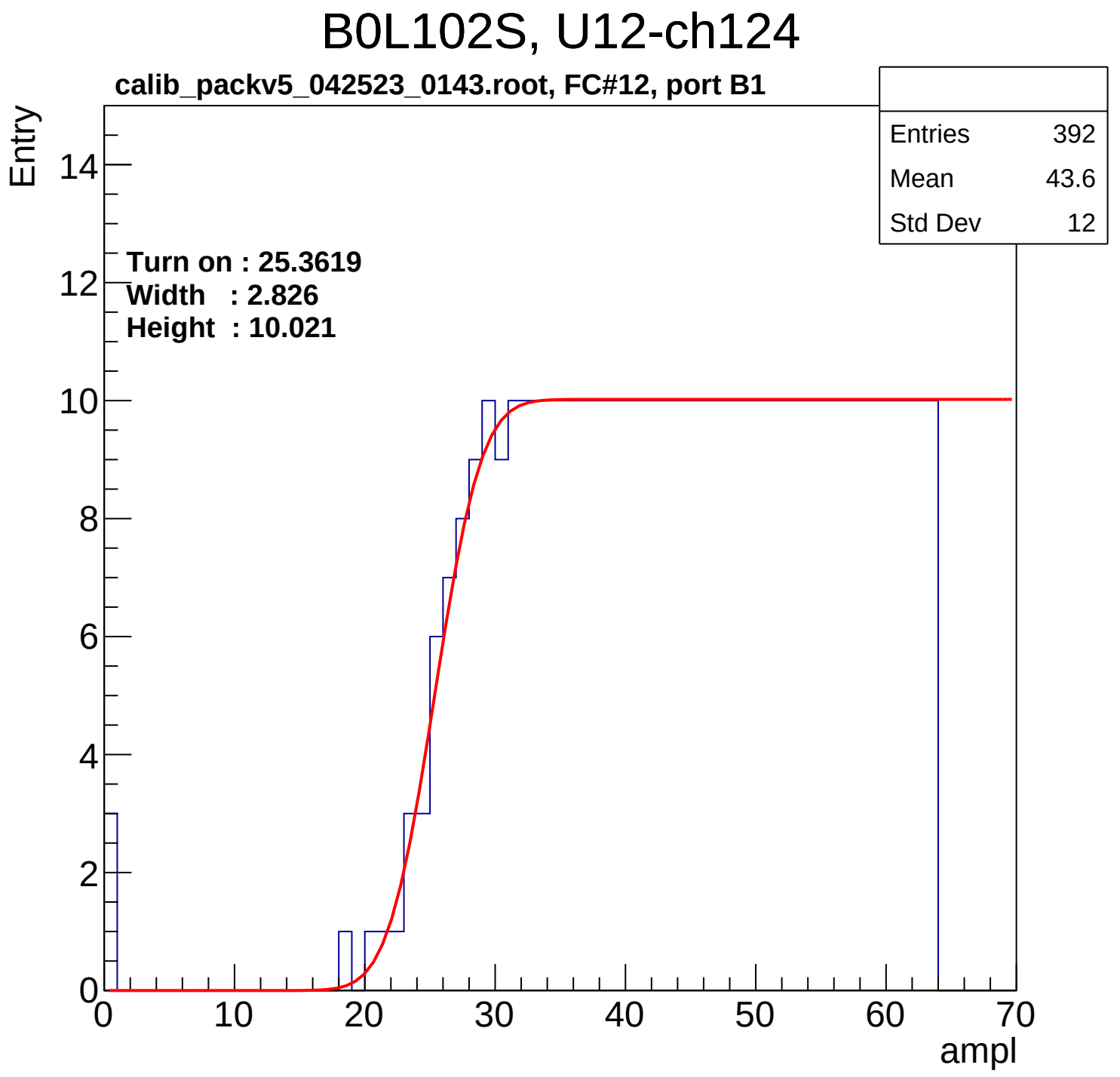
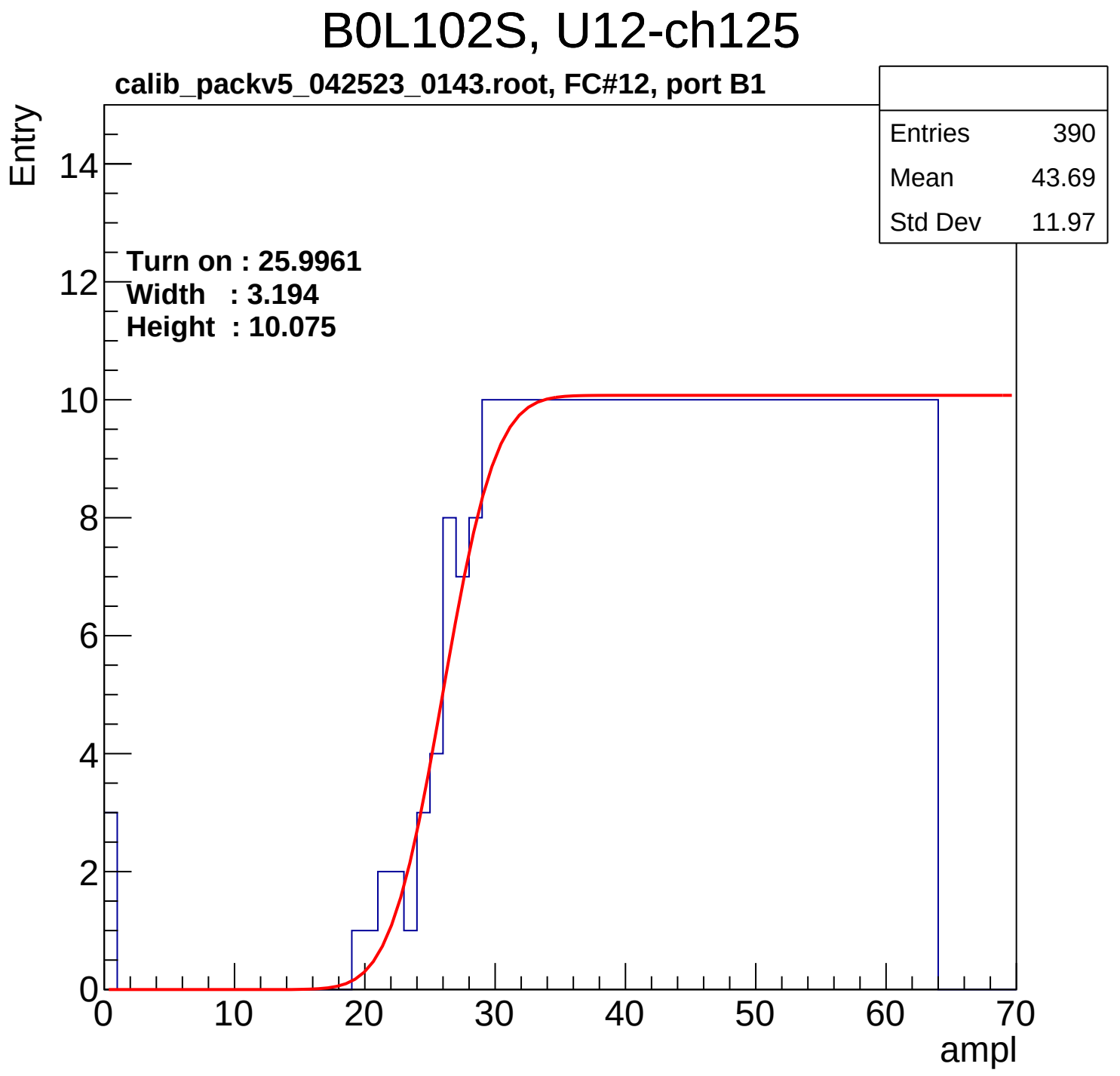

B0L102S, U12-ch123
calib_packv5_042523_0143.root, FC#12, port B1
Entries 380
Mean 44.25
Std Dev 11.54
Turn on : 26.7718
Width : 2.992
Height : 10.046
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L102S, U12-ch124
calib_packv5_042523_0143.root, FC#12, port B1
Entries 392
Mean 43.6
Std Dev 12
Turn on : 25.3619
Width : 2.826
Height : 10.021
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L102S, U12-ch125
calib_packv5_042523_0143.root, FC#12, port B1
Entries 390
Mean 43.69
Std Dev 11.97
Turn on : 25.9961
Width : 3.194
Height : 10.075
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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40
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60
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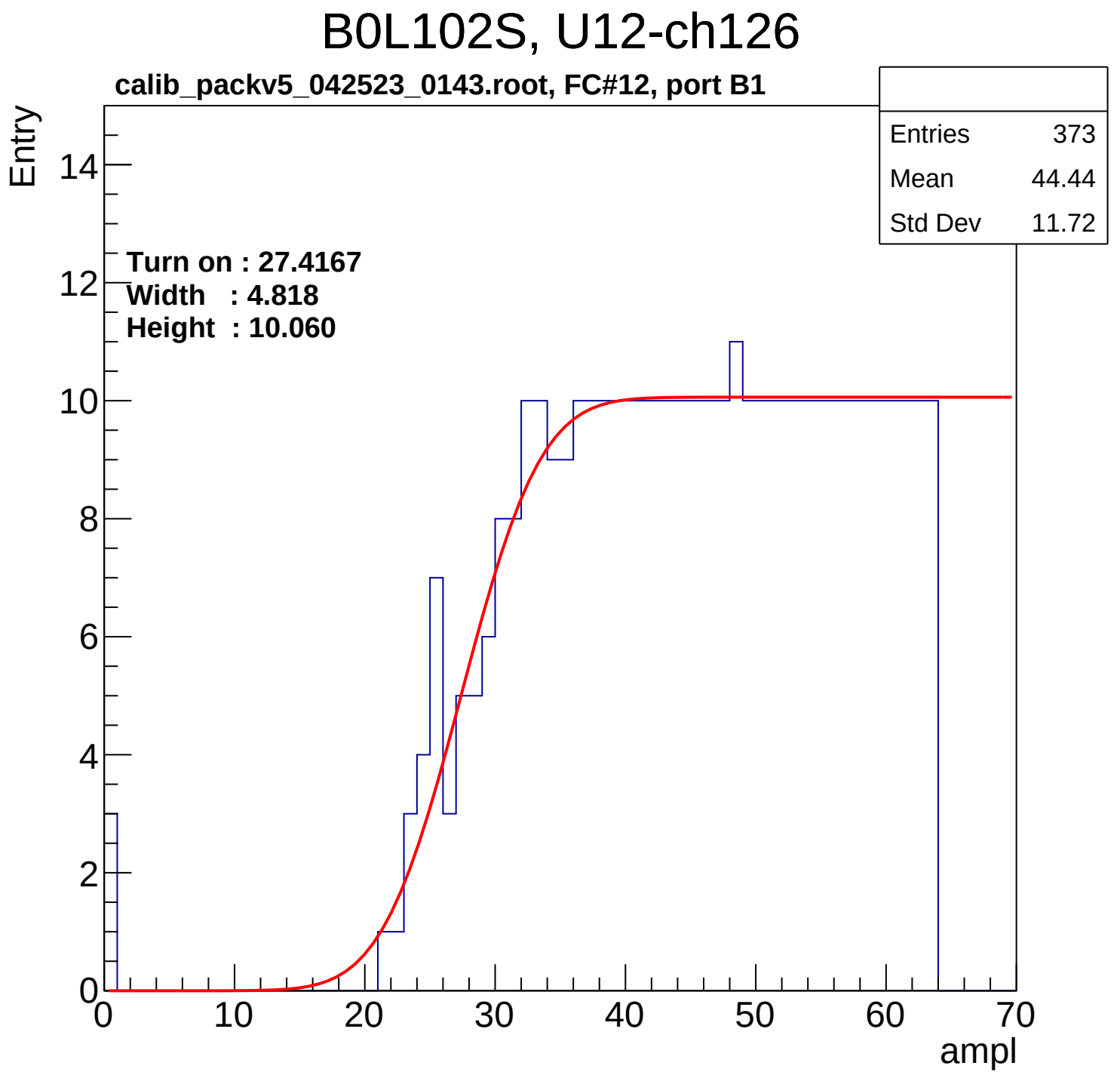
B0L102S, U12-ch126
calib_packv5_042523_0143.root, FC#12, port B1
Entries 373
Mean 44.44
Std Dev 11.72
Turn on : 27.4167
Width : 4.818
Height : 10.060
Entry
ampl
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2
4
6
8
10
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0
10
20
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40
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60
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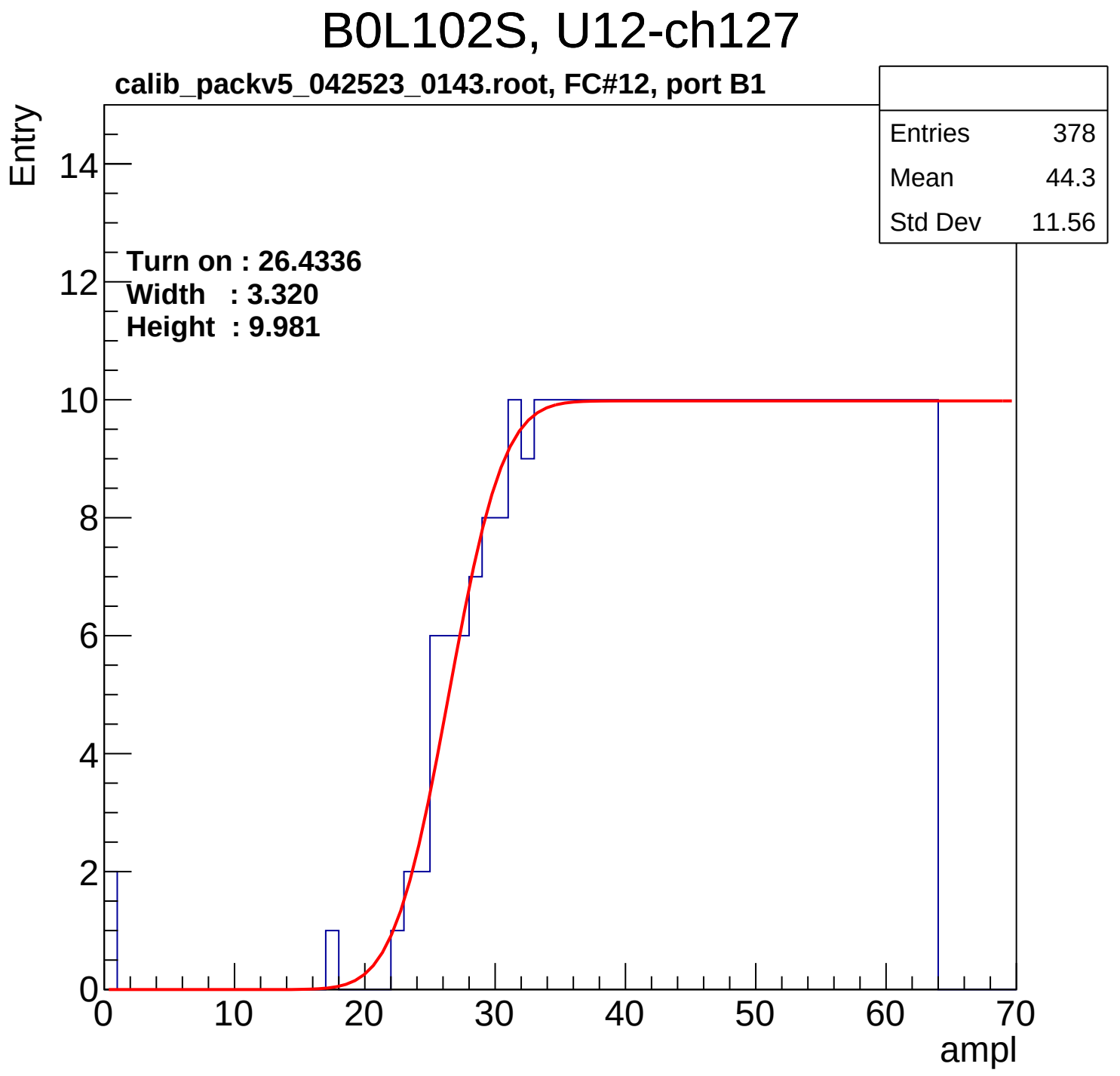
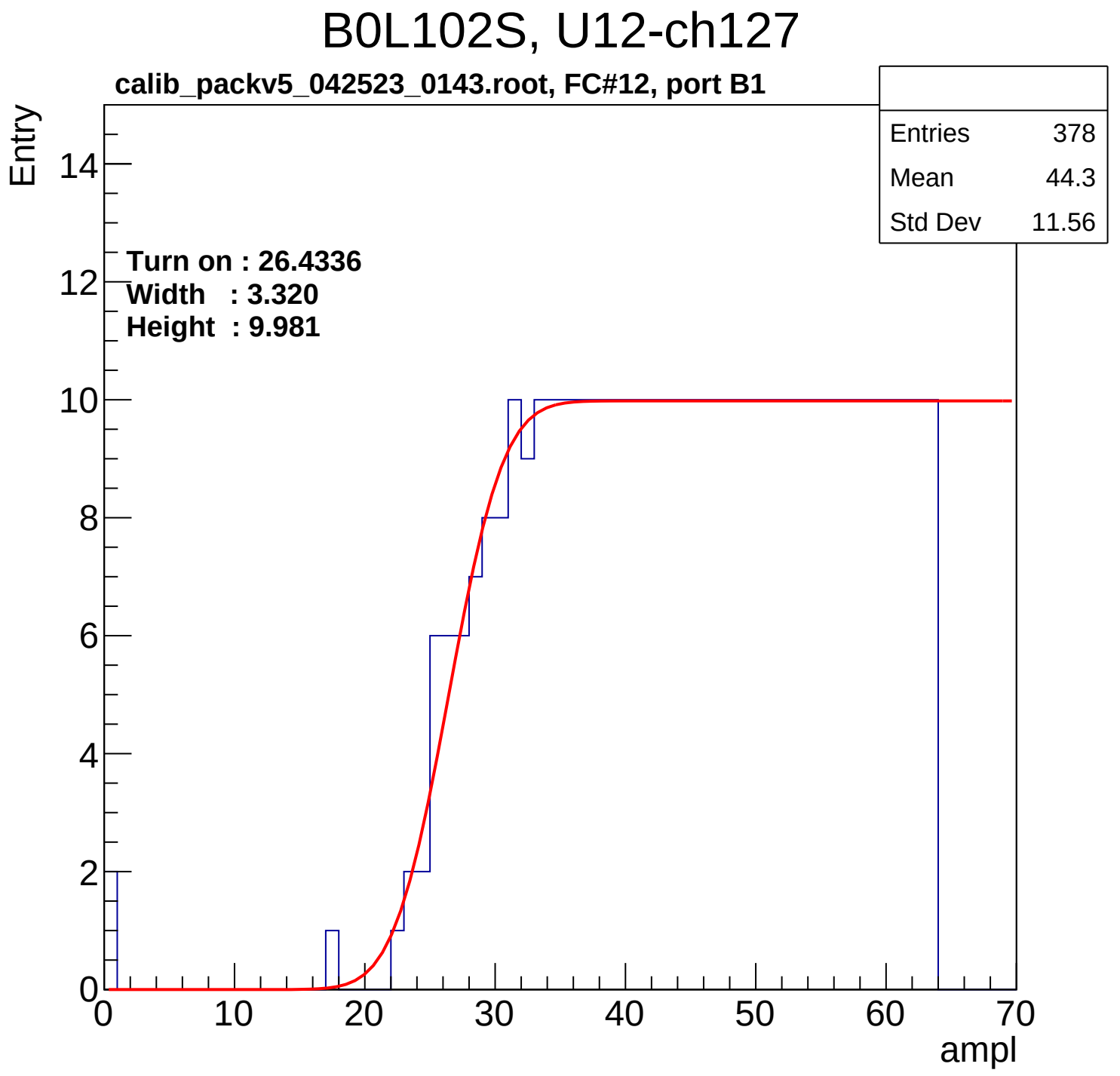

B0L102S, U12-ch127
calib_packv5_042523_0143.root, FC#12, port B1
Entries 378
Mean 44.3
Std Dev 11.56
Turn on : 26.4336
Width : 3.320
Height : 9.981
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L102S, U12-ch127
calib_packv5_042523_0143.root, FC#12, port B1
Entries 378
Mean 44.3
Std Dev 11.56
Turn on : 26.4336
Width : 3.320
Height : 9.981
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
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60
70