

B1L103S, U11-ch0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	463
Mean	37.91
Std Dev	17.77

Turn on : 23.3610

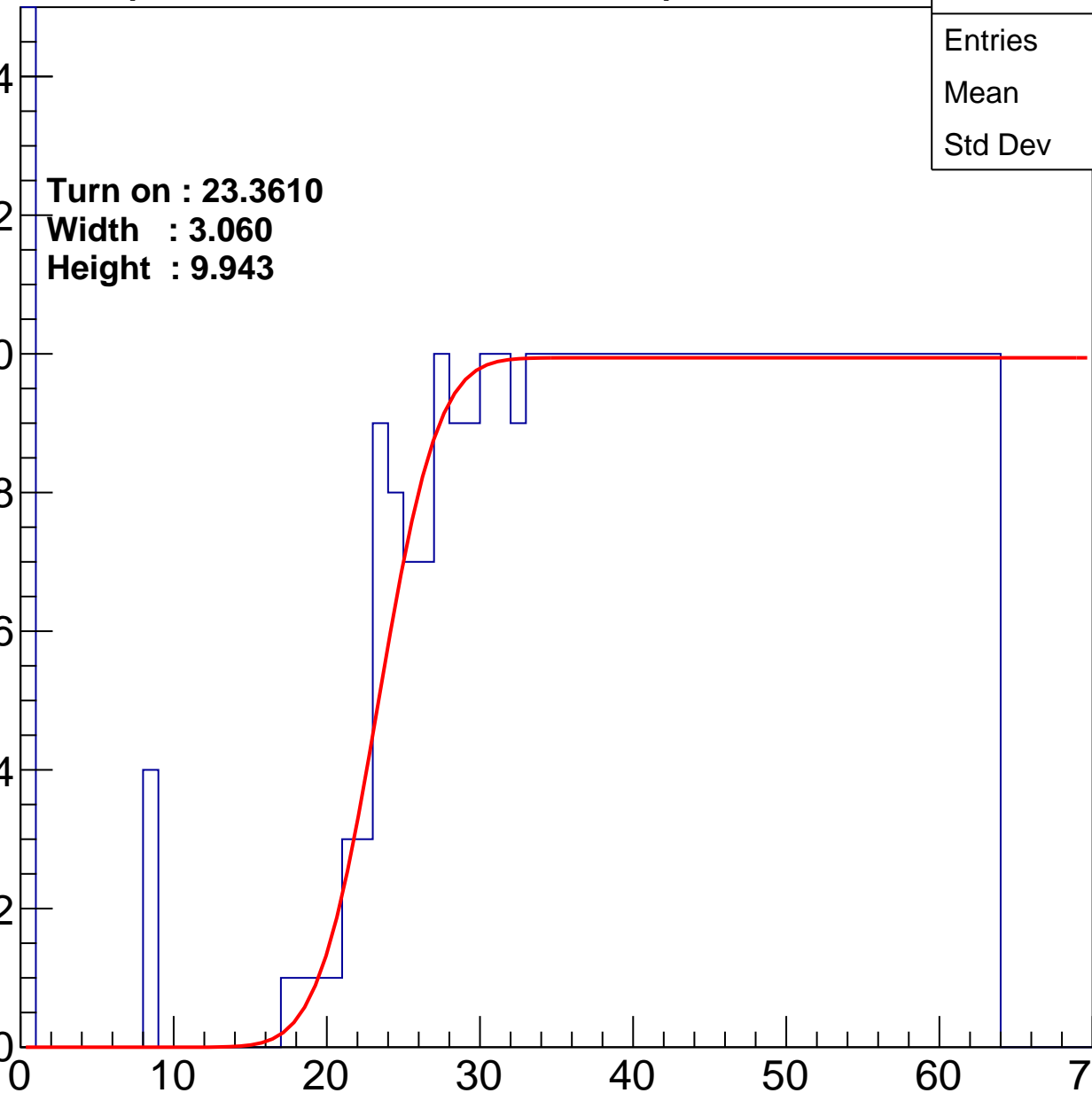
Width : 3.060

Height : 9.943

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U11-ch1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	416
Mean	40.55
Std Dev	16.42

Turn on : 26.6711

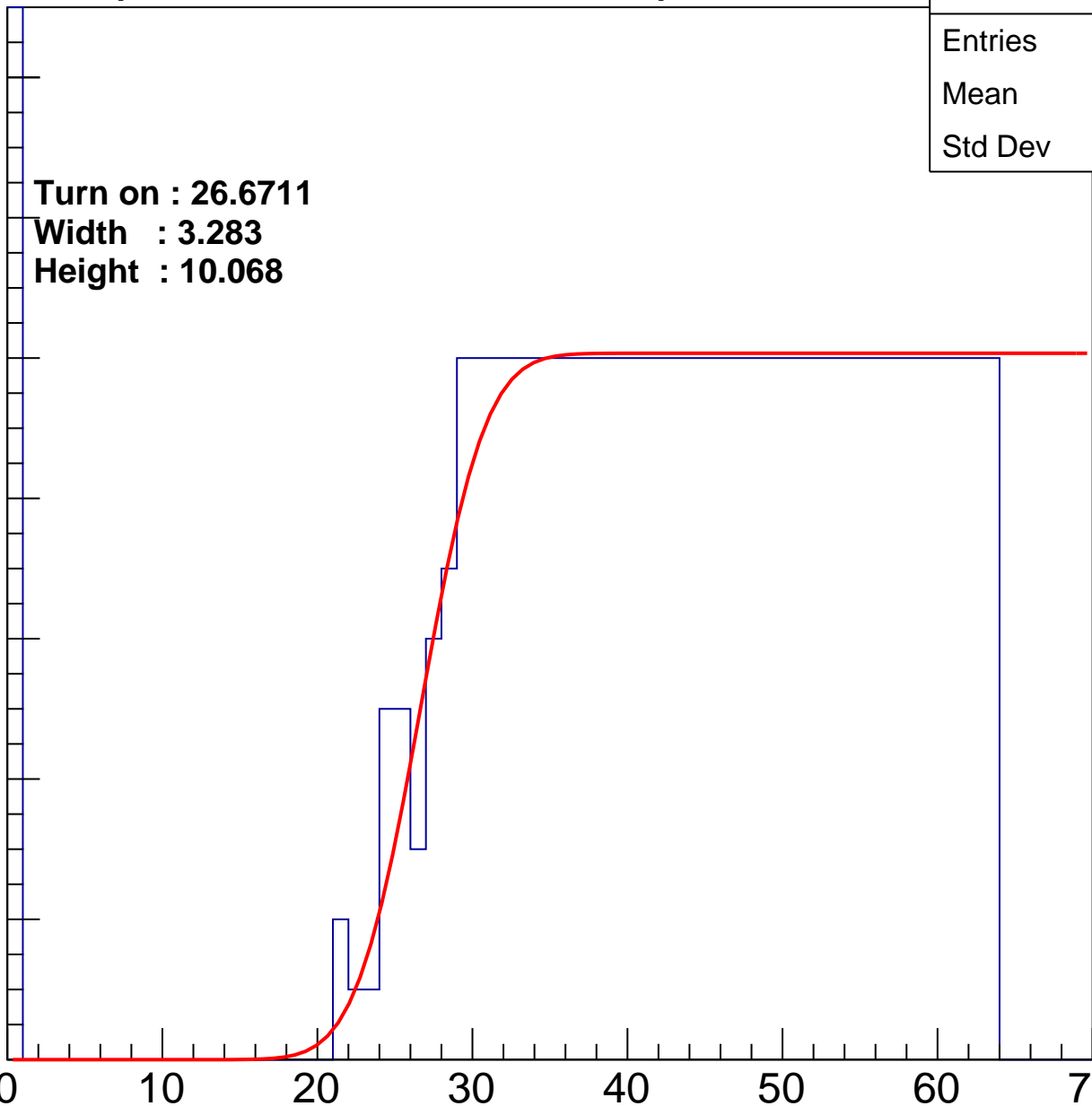
Width : 3.283

Height : 10.068

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U11-ch2

calib_packv5_041523_1651.root, FC#0, port C2

Entries	428
Mean	39.91
Std Dev	16.75

Turn on : 25.6956

Width : 2.772

Height : 10.056

Entry

14

12

10

8

6

4

2

0

0

10

20

30

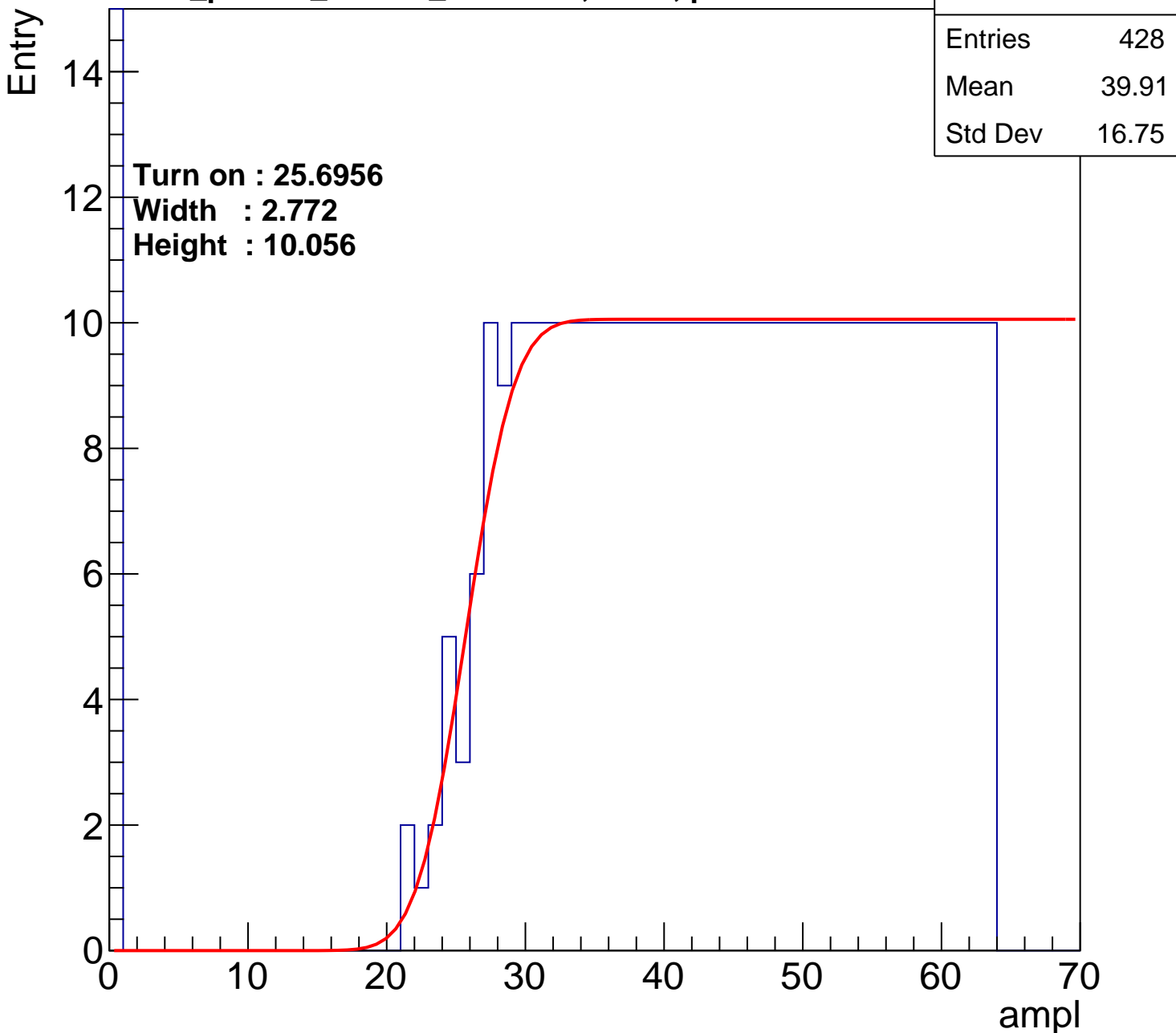
40

50

60

70

ampl



B1L103S, U11-ch3

calib_packv5_041523_1651.root, FC#0, port C2

Entries	411
Mean	40.39
Std Dev	16.96

Turn on : 27.1726

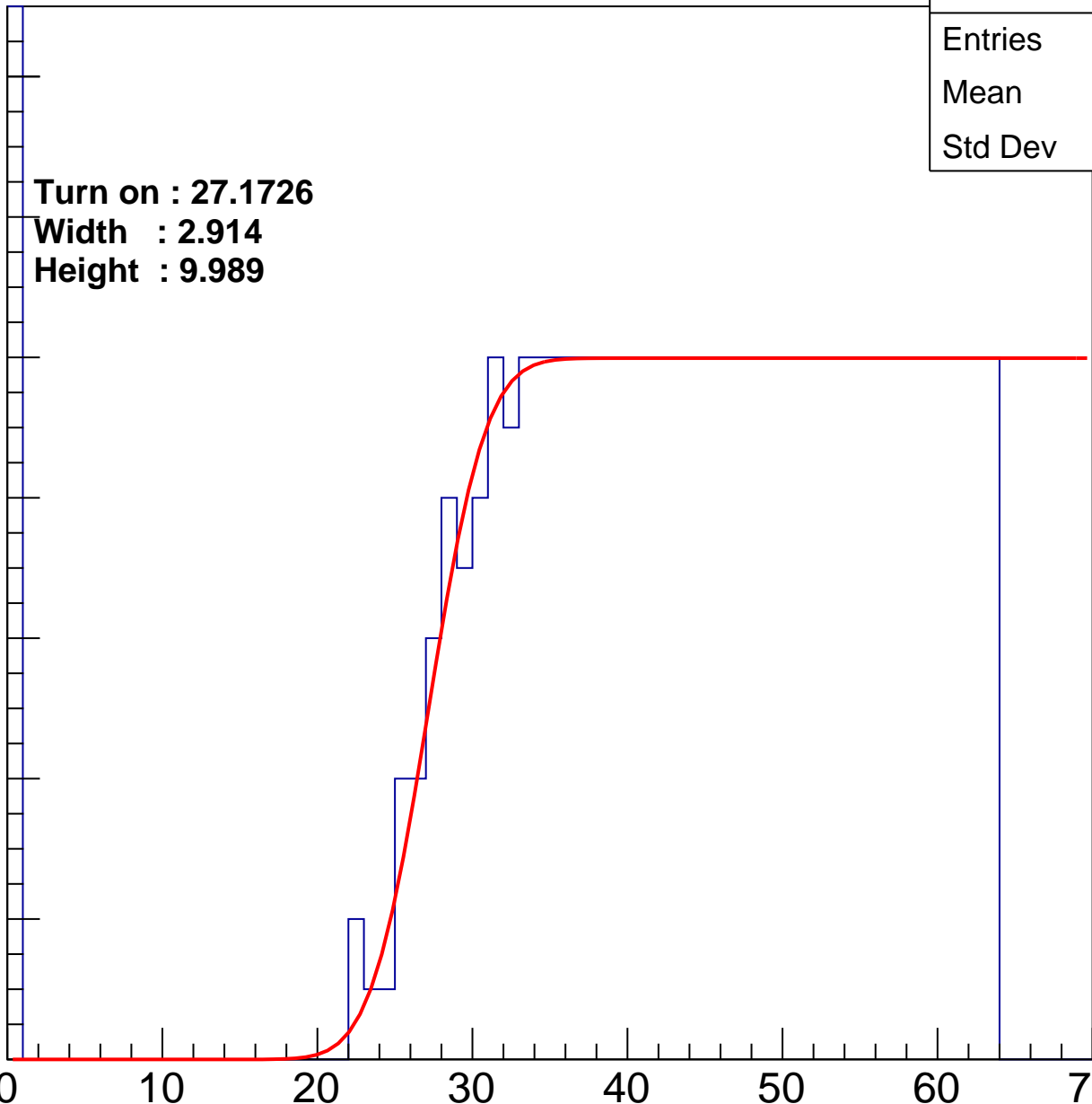
Width : 2.914

Height : 9.989

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U11-ch4

calib_packv5_041523_1651.root, FC#0, port C2

Entries	434
Mean	39.22
Std Dev	17.46

Turn on : 25.2849

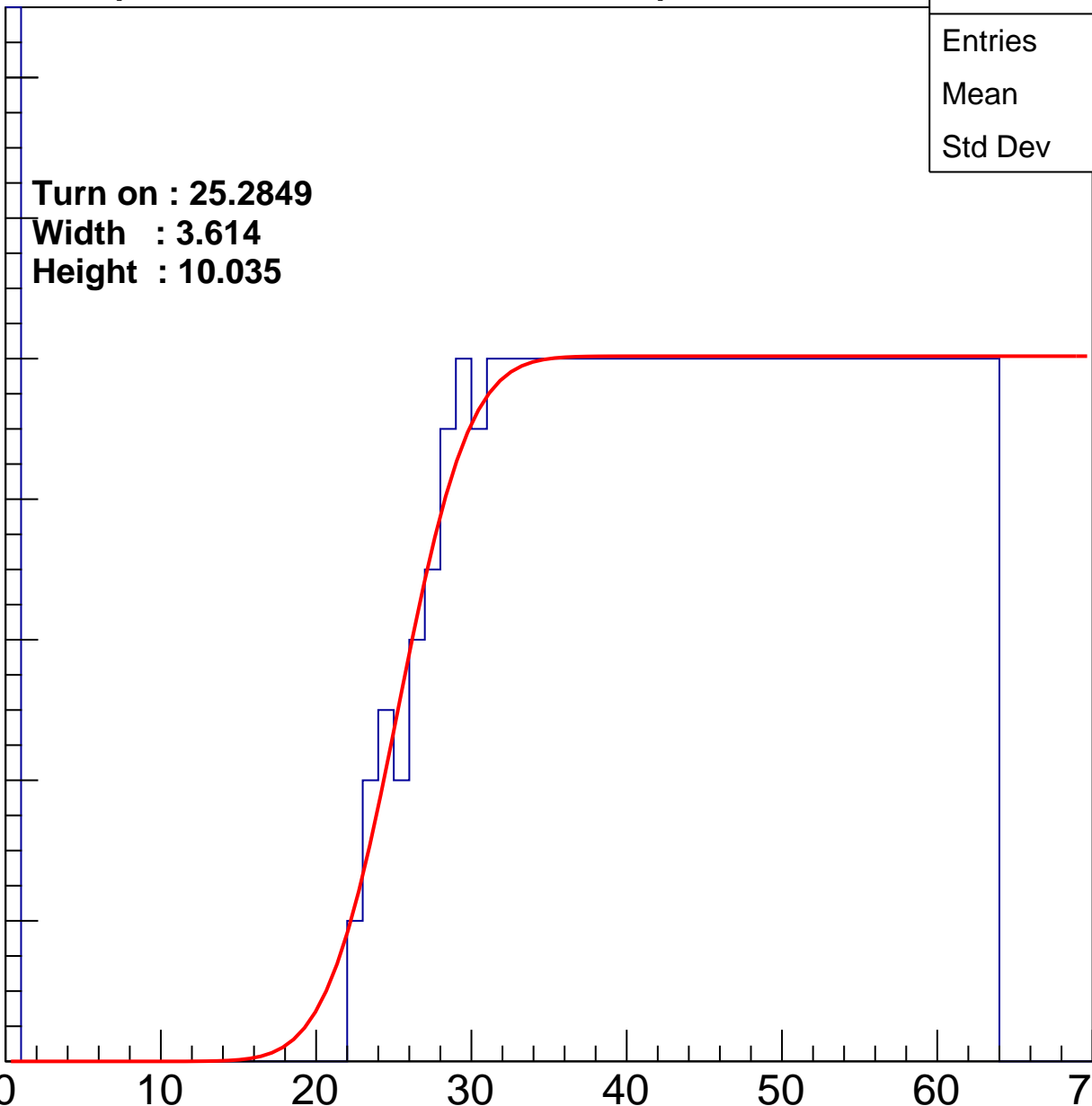
Width : 3.614

Height : 10.035

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U11-ch5

calib_packv5_041523_1651.root, FC#0, port C2

Entries	389
Mean	41.58
Std Dev	16.41

Turn on : 28.4112

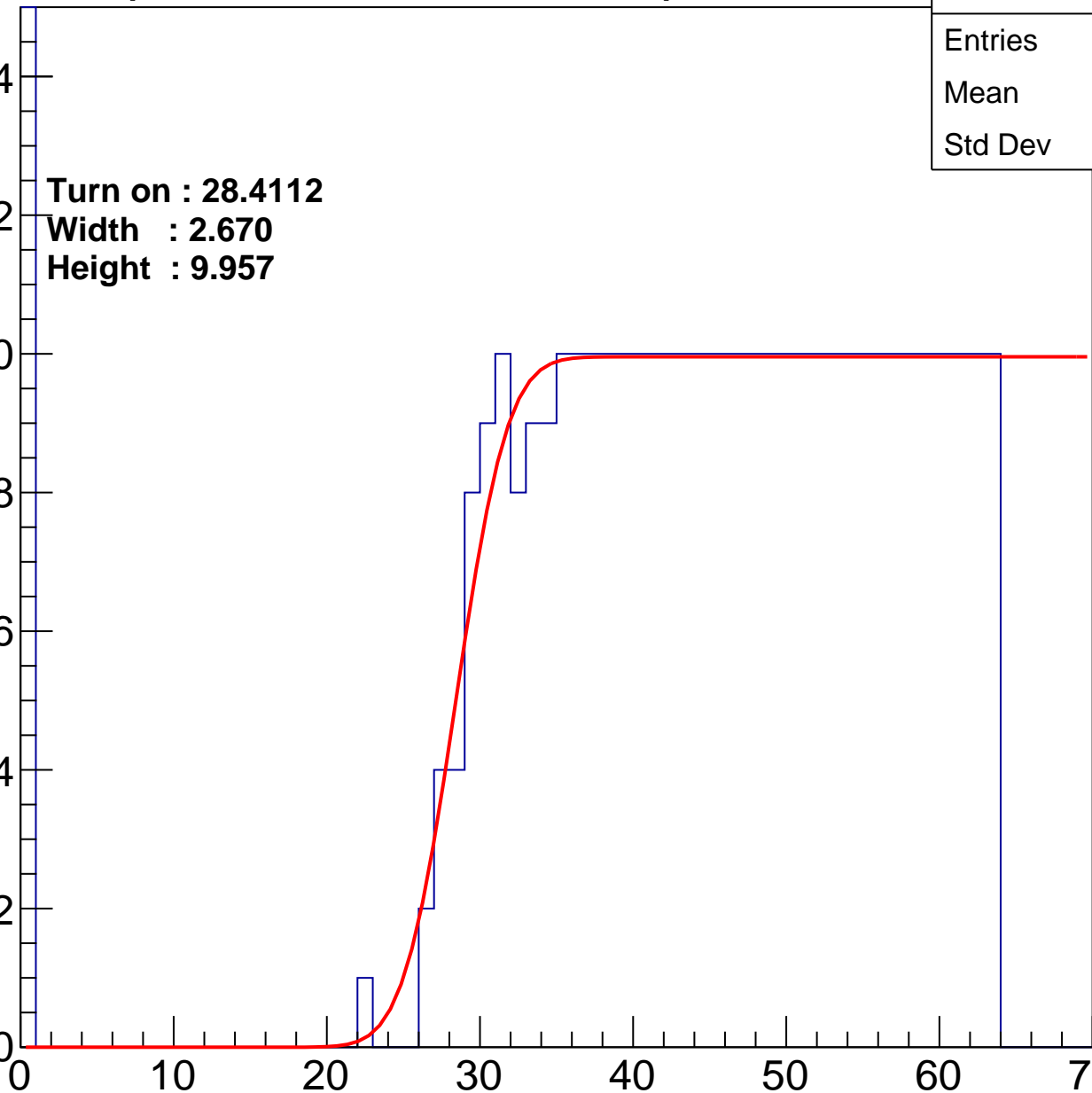
Width : 2.670

Height : 9.957

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U11-ch6

calib_packv5_041523_1651.root, FC#0, port C2

Entries	416
Mean	40.47
Std Dev	16.53

Turn on : 26.0608

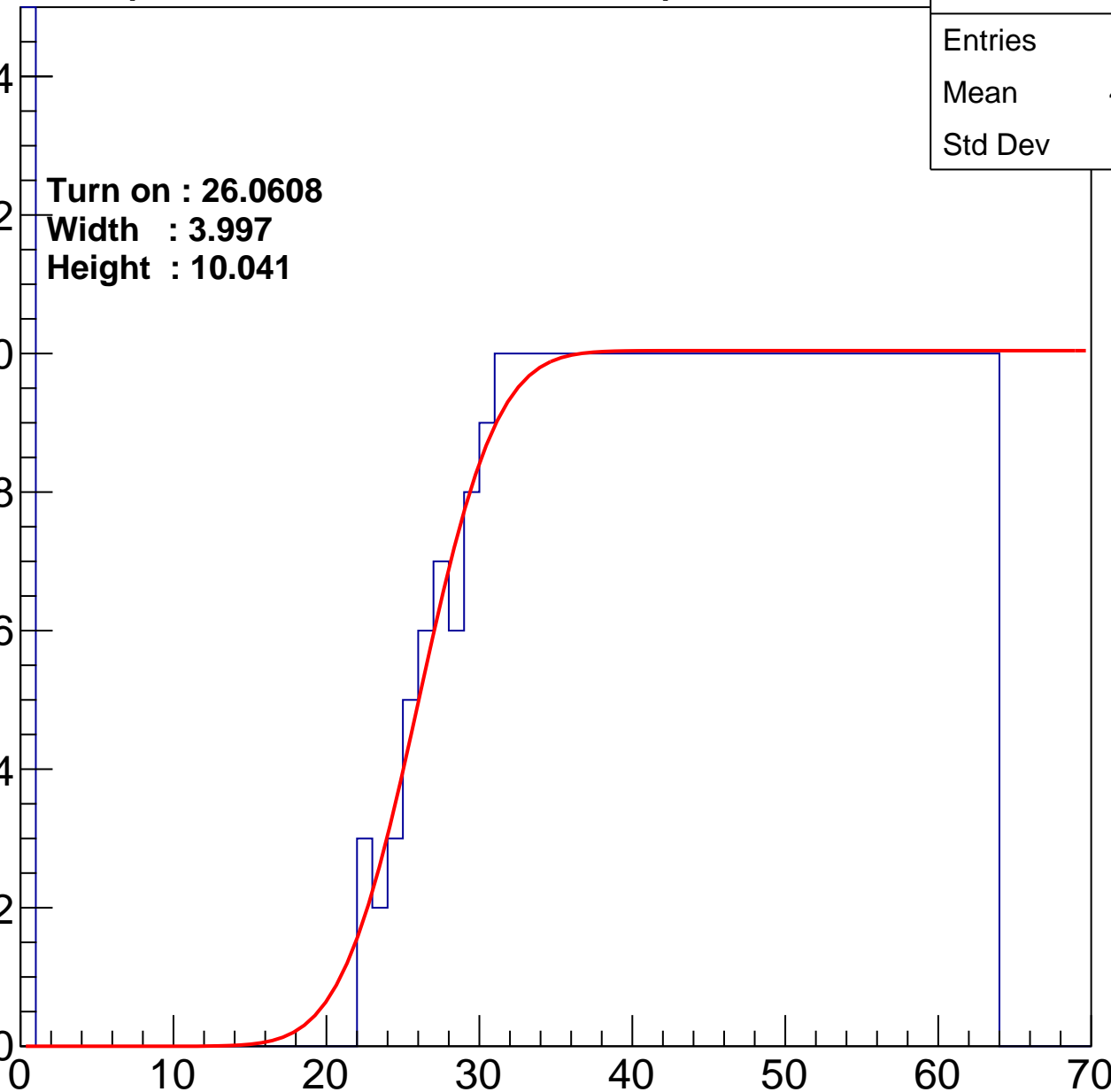
Width : 3.997

Height : 10.041

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U11-ch7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	437
Mean	39.39
Std Dev	17.02

Turn on : 25.3696

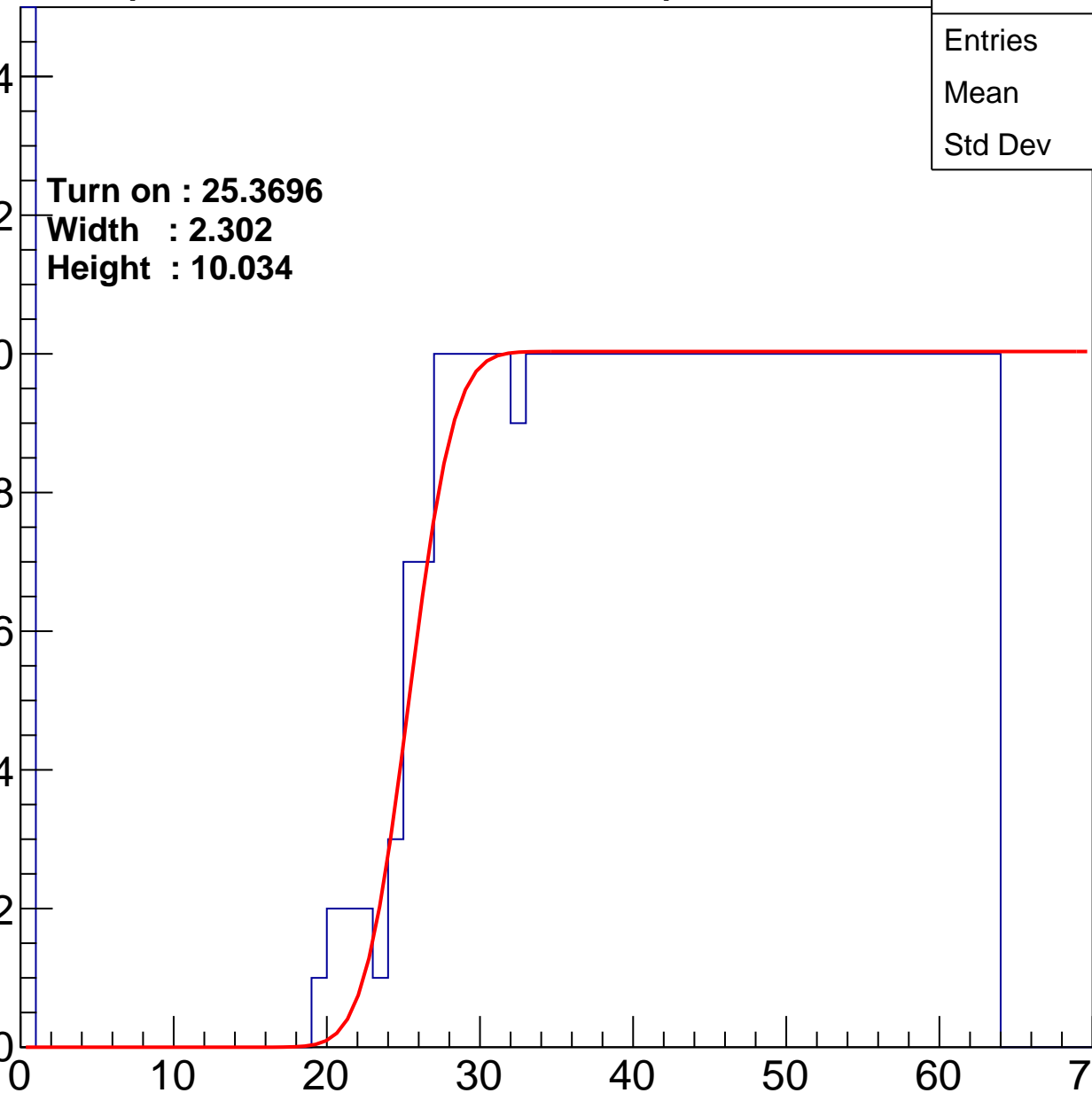
Width : 2.302

Height : 10.034

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U11-ch8

calib_packv5_041523_1651.root, FC#0, port C2

Entries	404
Mean	41.41
Std Dev	15.69

Turn on : 26.8974

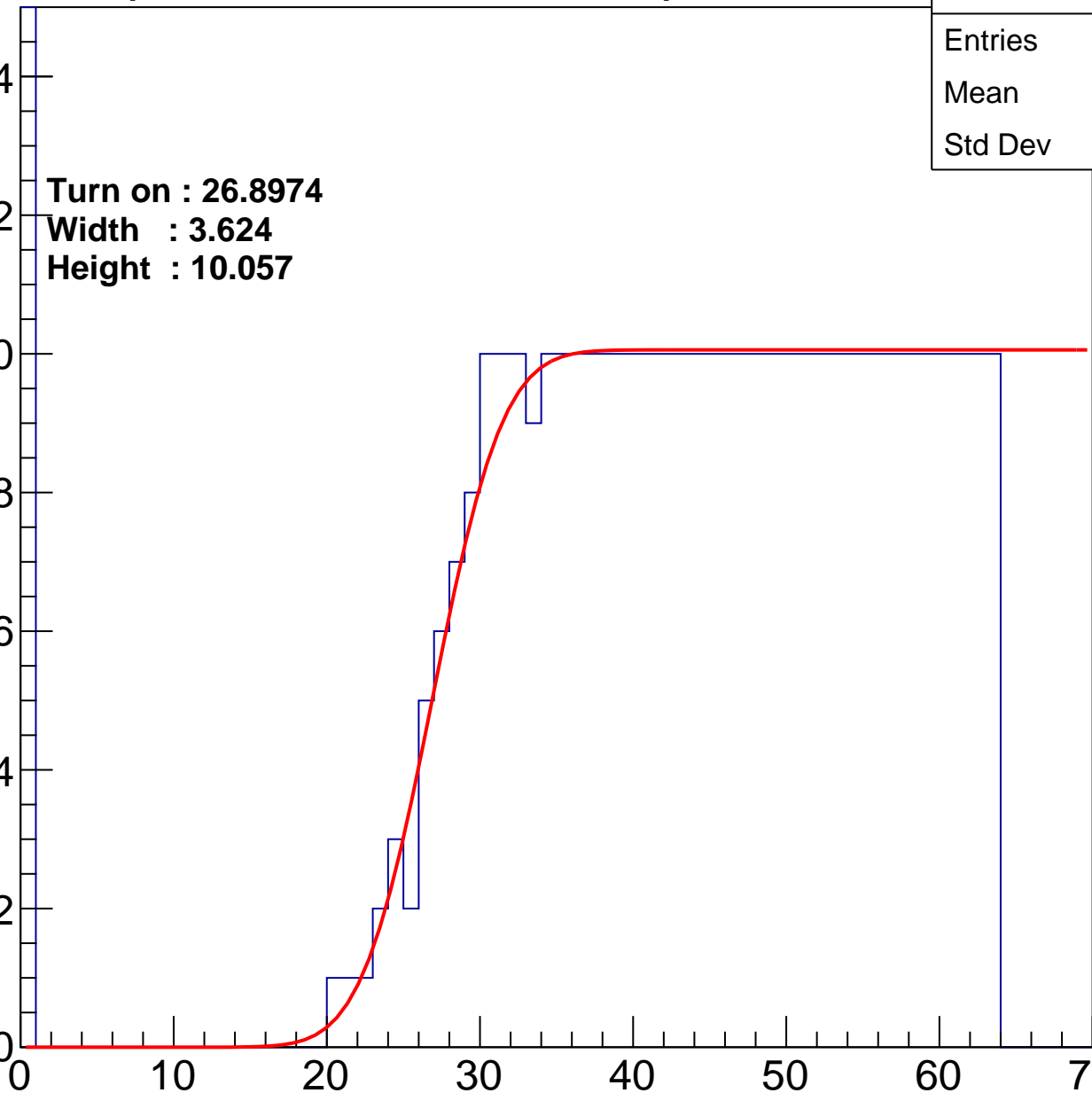
Width : 3.624

Height : 10.057

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U11-ch9

calib_packv5_041523_1651.root, FC#0, port C2

Entries	396
Mean	41.09
Std Dev	16.75

Turn on : 28.2606

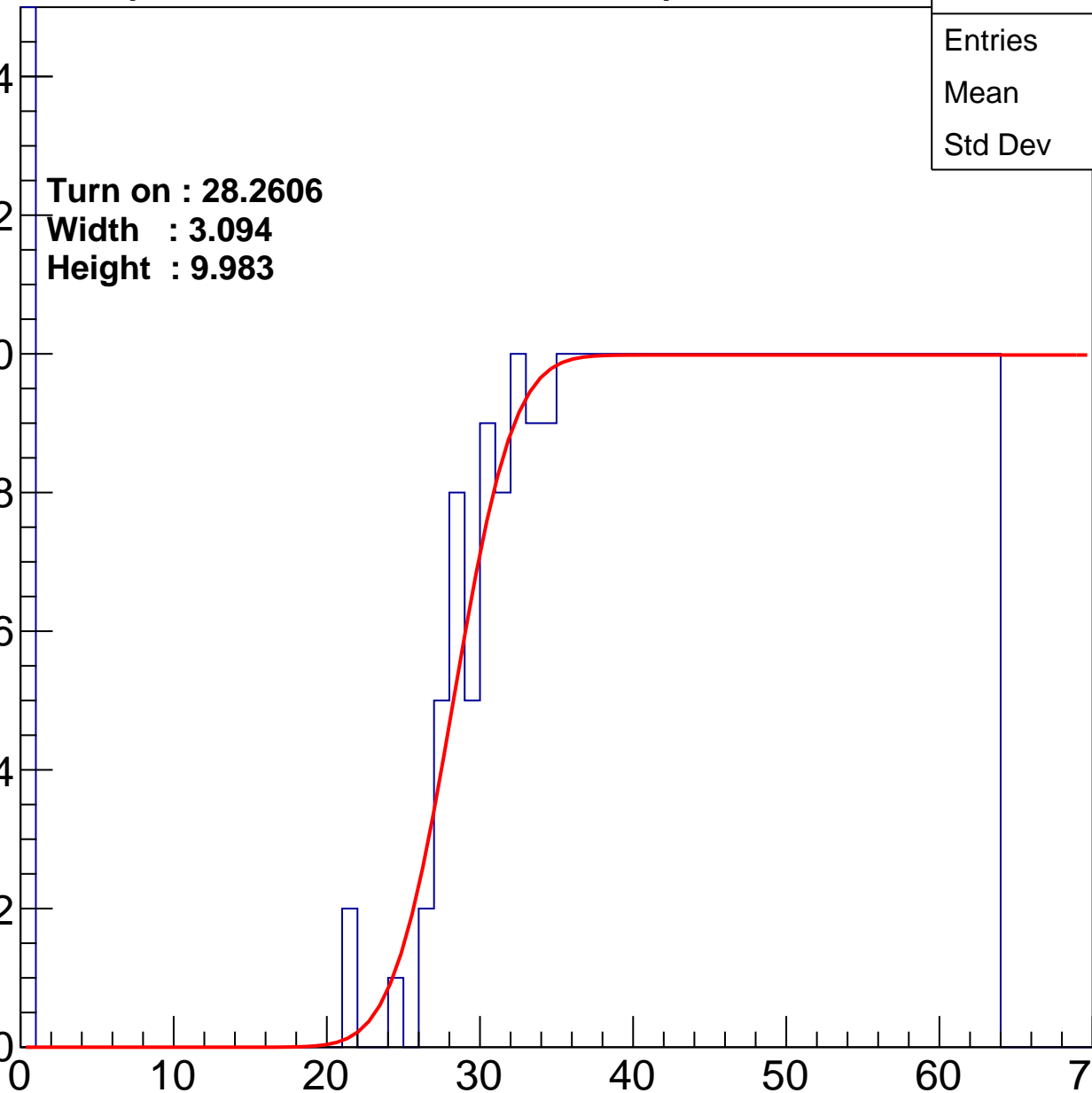
Width : 3.094

Height : 9.983

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U11-ch10

calib_packv5_041523_1651.root, FC#0, port C2

Entries	419
Mean	40.42
Std Dev	16.42

Turn on : 25.7206

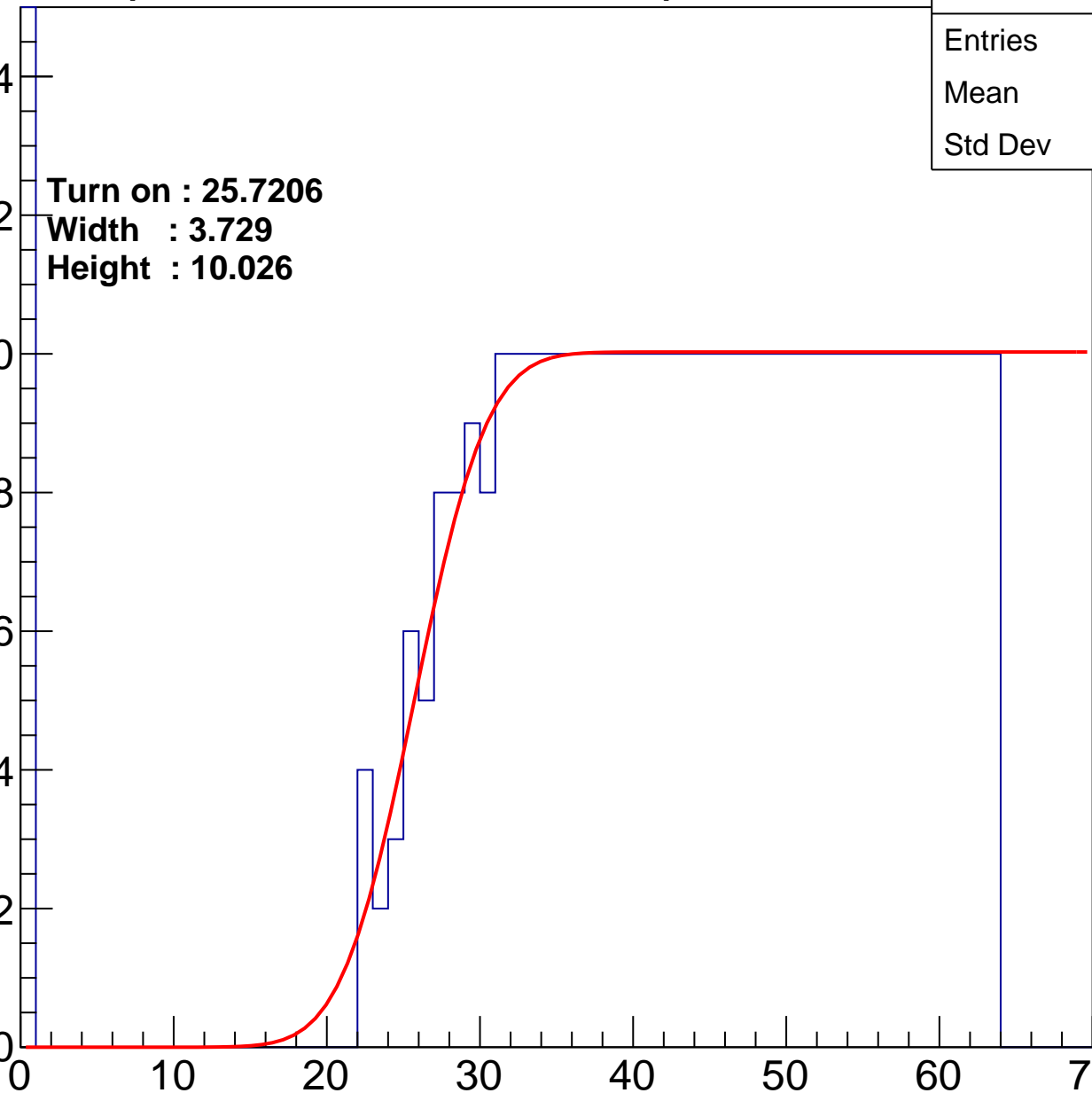
Width : 3.729

Height : 10.026

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U11-ch11

calib_packv5_041523_1651.root, FC#0, port C2

Entries	415
Mean	40.88
Std Dev	15.89

Turn on : 25.8549

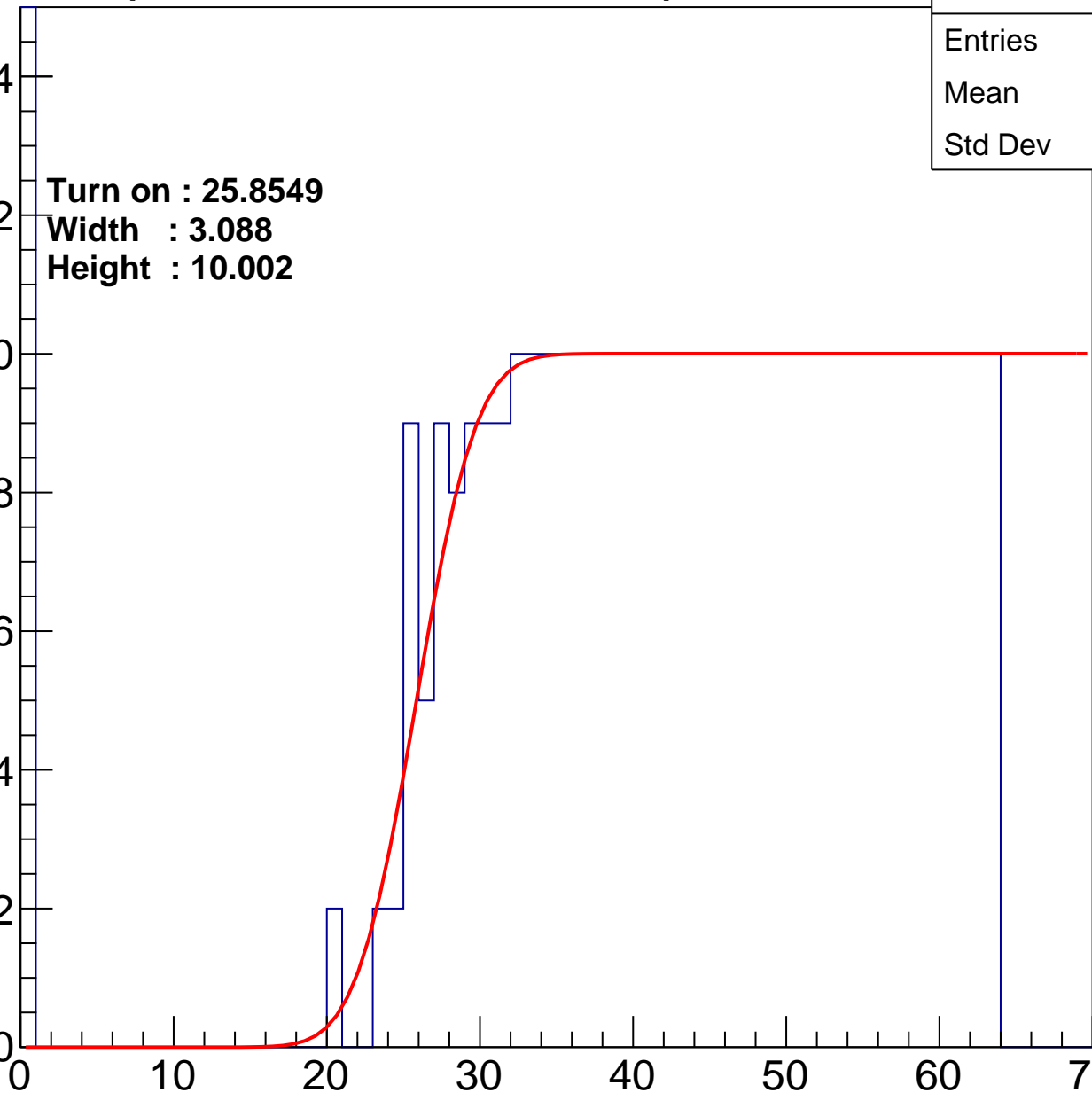
Width : 3.088

Height : 10.002

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U11-ch12

calib_packv5_041523_1651.root, FC#0, port C2

Entries	403
Mean	41.1
Std Dev	16.33

Turn on : 27.3692

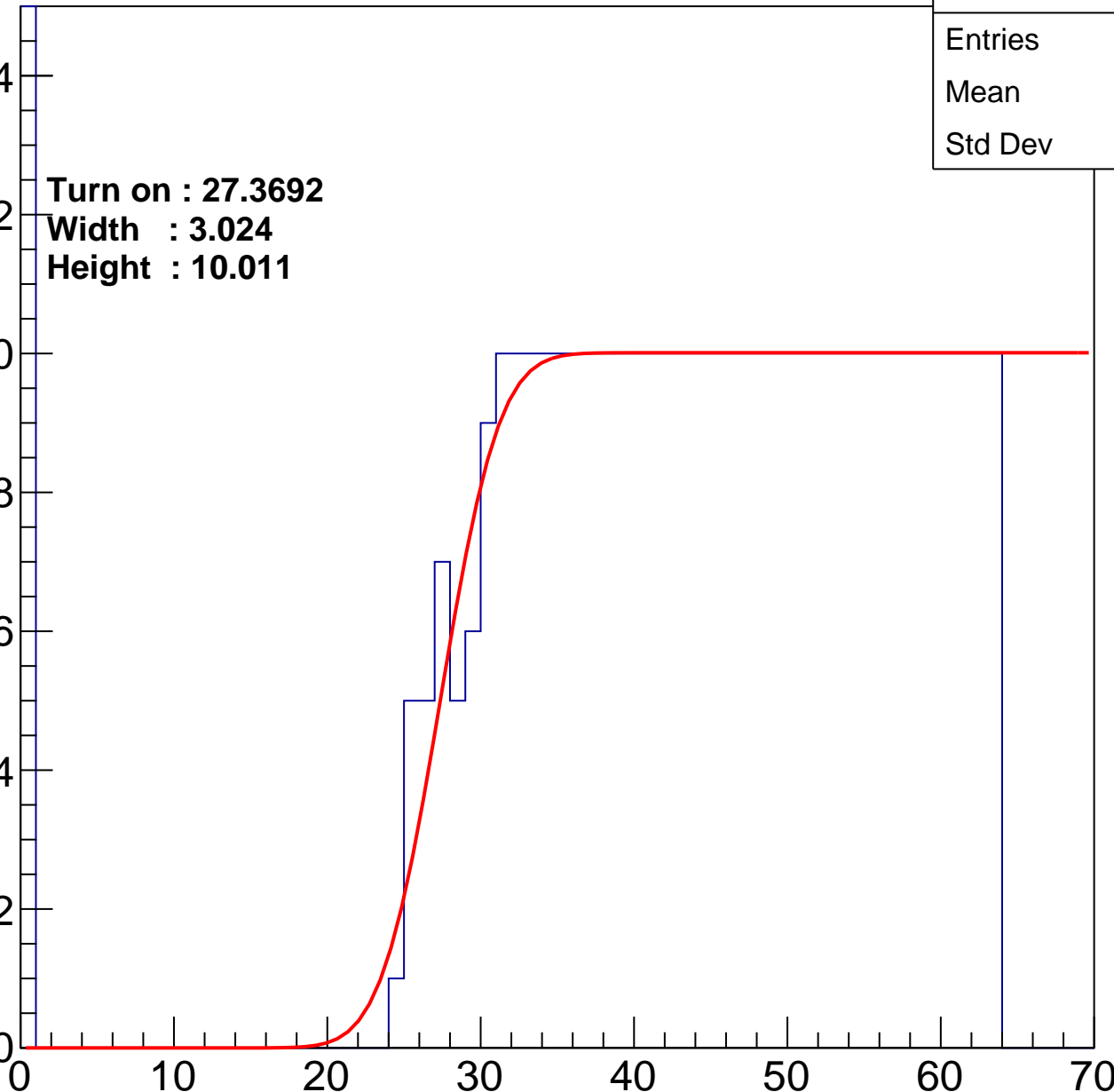
Width : 3.024

Height : 10.011

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U11-ch13

calib_packv5_041523_1651.root, FC#0, port C2

Entries	417
Mean	40.08
Std Dev	17.11

Turn on : 26.7528

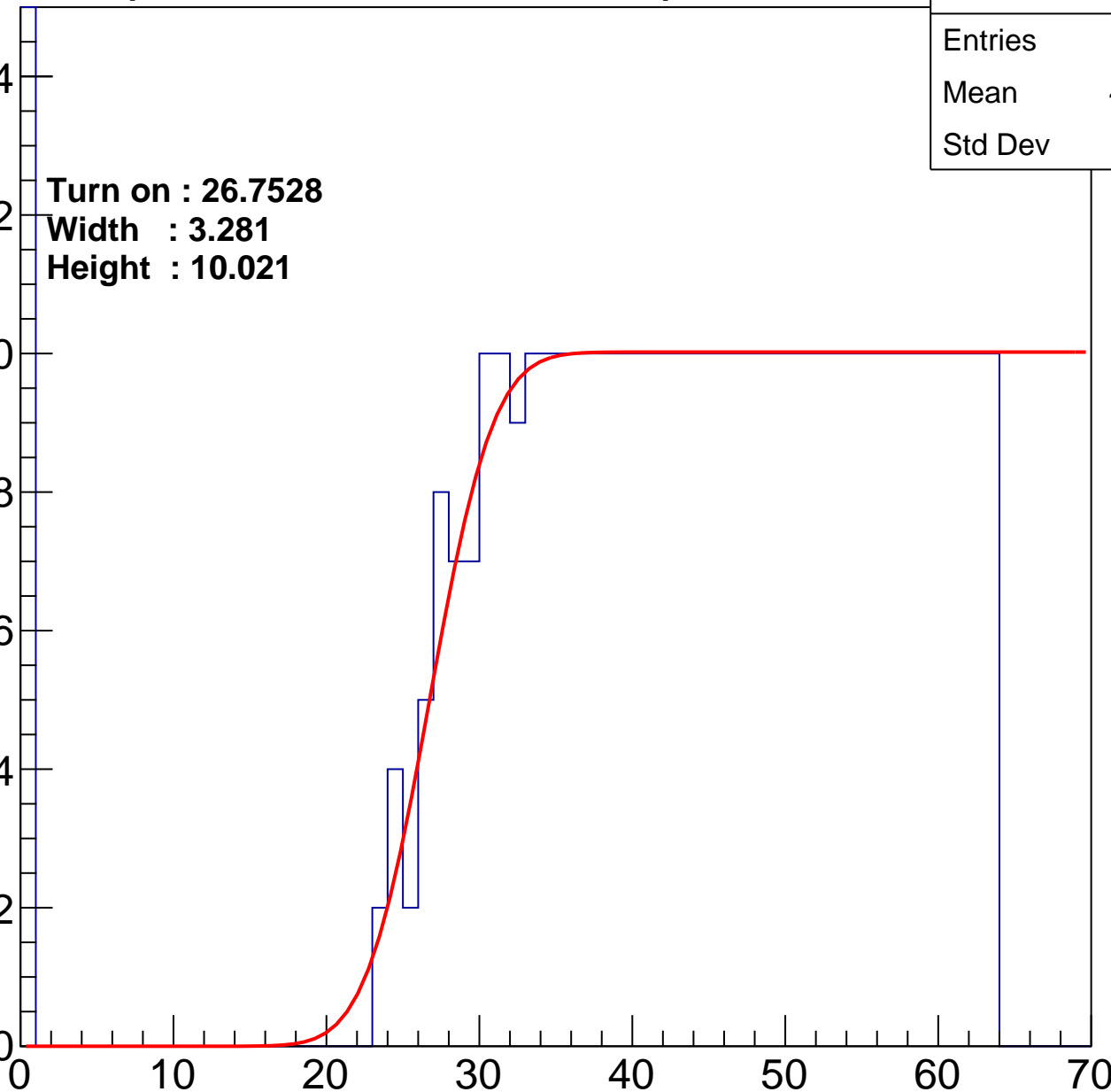
Width : 3.281

Height : 10.021

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U11-ch14

calib_packv5_041523_1651.root, FC#0, port C2

Entries	420
Mean	39.61
Std Dev	17.66

Turn on : 26.8146

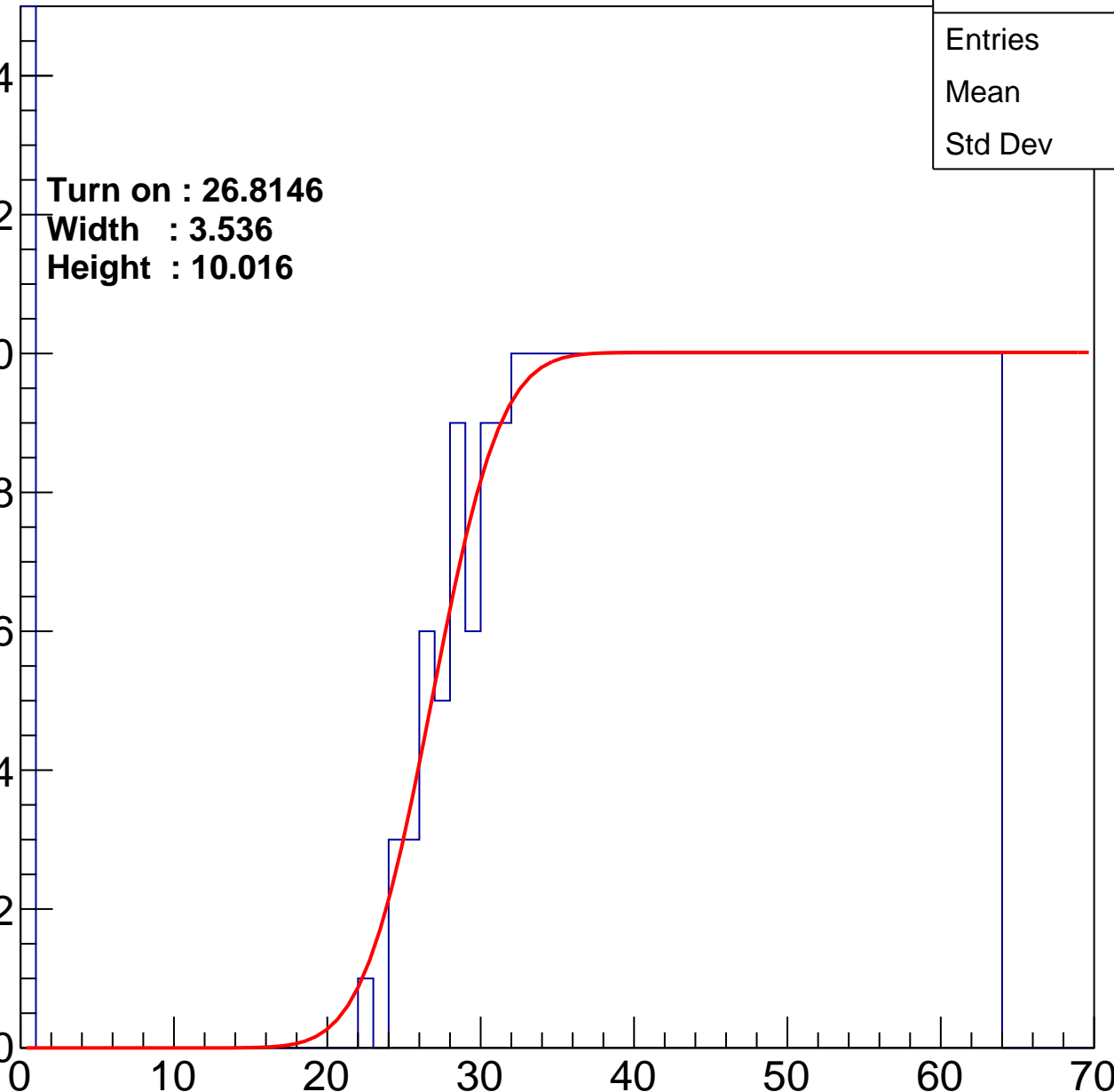
Width : 3.536

Height : 10.016

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U11-ch15

calib_packv5_041523_1651.root, FC#0, port C2

Entries	407
Mean	40.87
Std Dev	16.49

Turn on : 27.1970

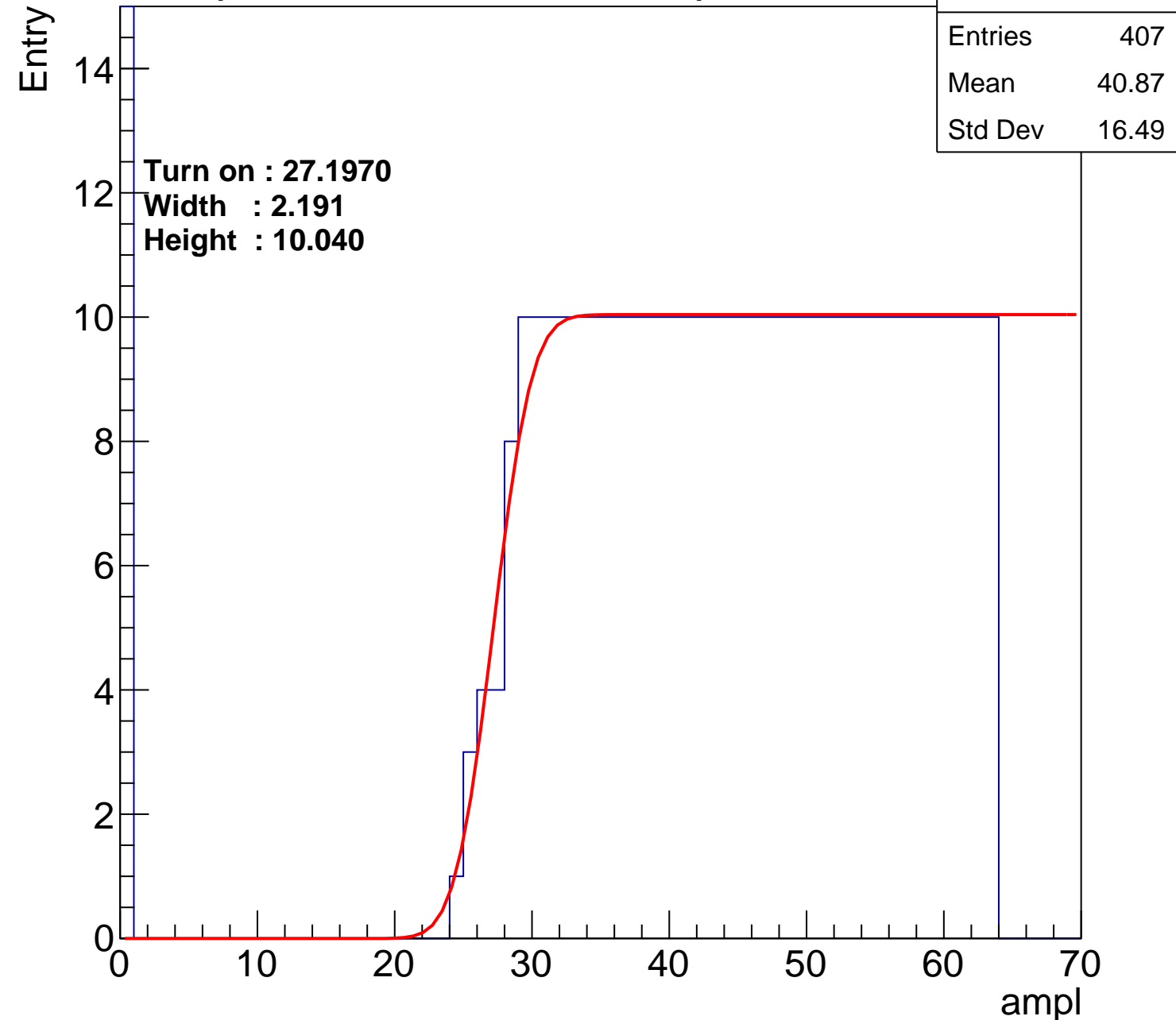
Width : 2.191

Height : 10.040

Entry

14
12
10
8
6
4
2
0

ampl

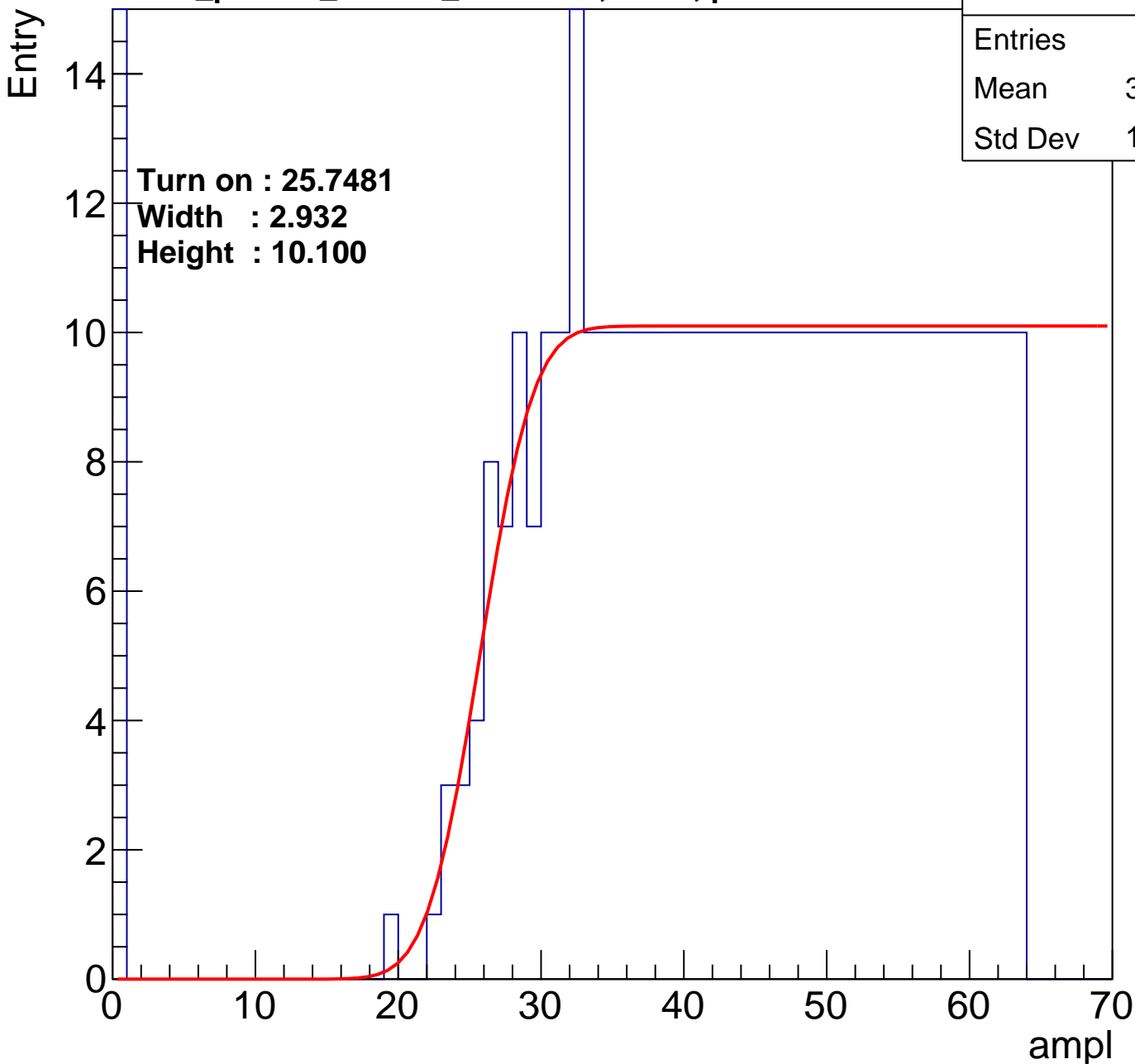


B1L103S, U11-ch16

calib_packv5_041523_1651.root, FC#0, port C2

Entries	441
Mean	38.92
Std Dev	17.62

Turn on : 25.7481
Width : 2.932
Height : 10.100



B1L103S, U11-ch17

calib_packv5_041523_1651.root, FC#0, port C2

Entries	426
Mean	39.41
Std Dev	17.62

Turn on : 26.4488

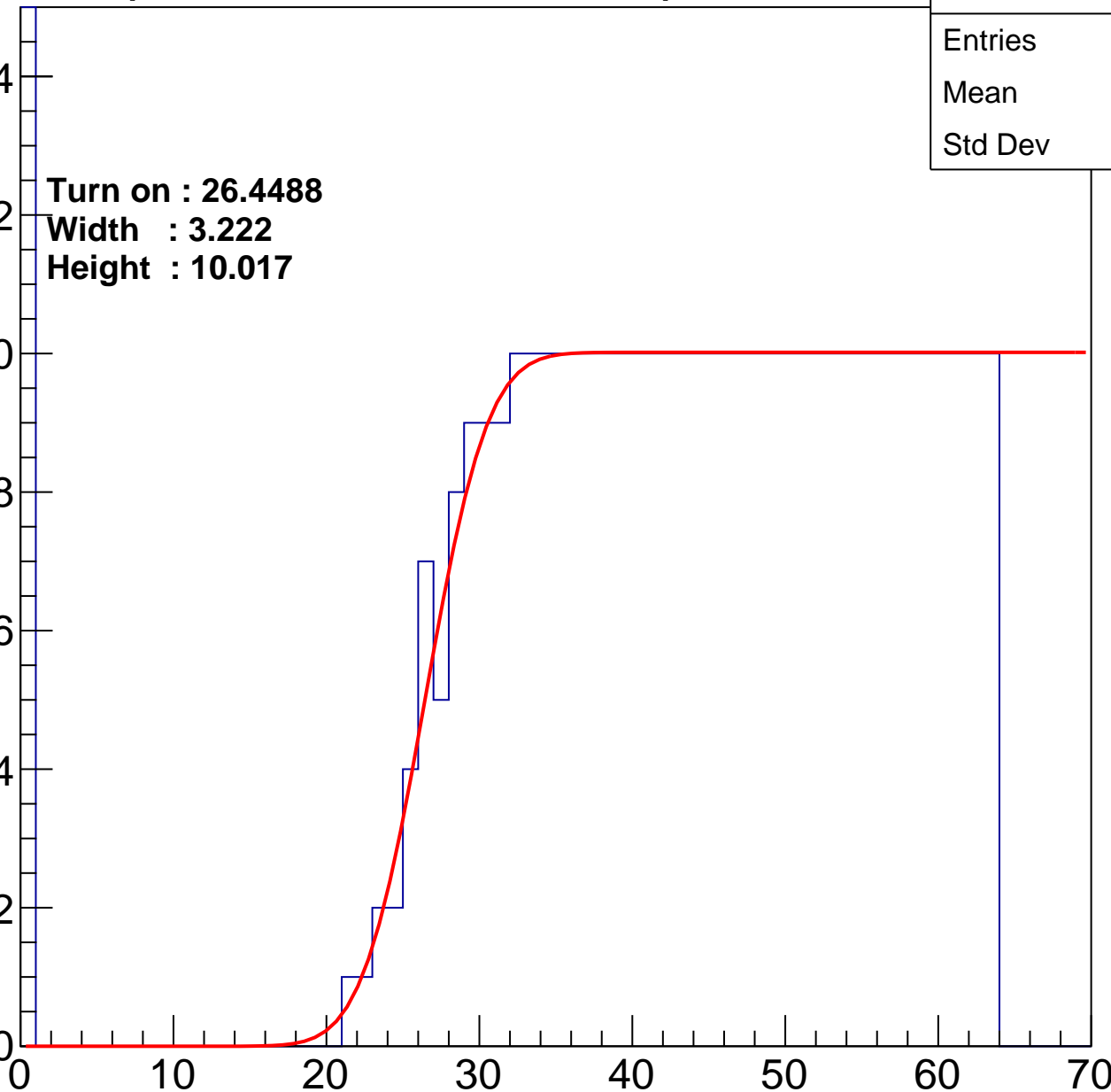
Width : 3.222

Height : 10.017

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U11-ch18

calib_packv5_041523_1651.root, FC#0, port C2

Entries	414
Mean	40.36
Std Dev	16.89

Turn on : 26.9236

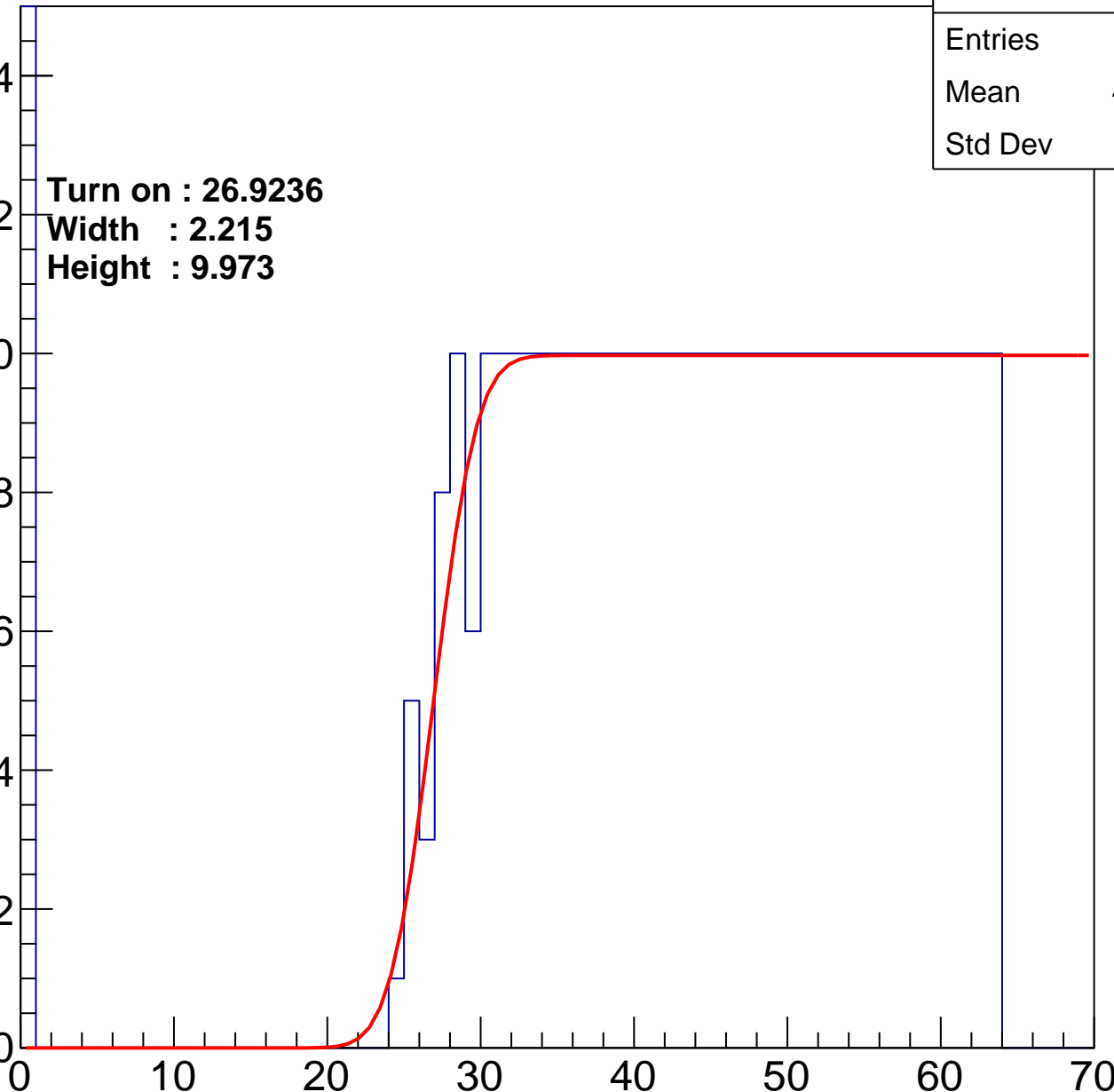
Width : 2.215

Height : 9.973

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U11-ch19

calib_packv5_041523_1651.root, FC#0, port C2

Entries	429
Mean	39.81
Std Dev	16.85

Turn on : 25.3345

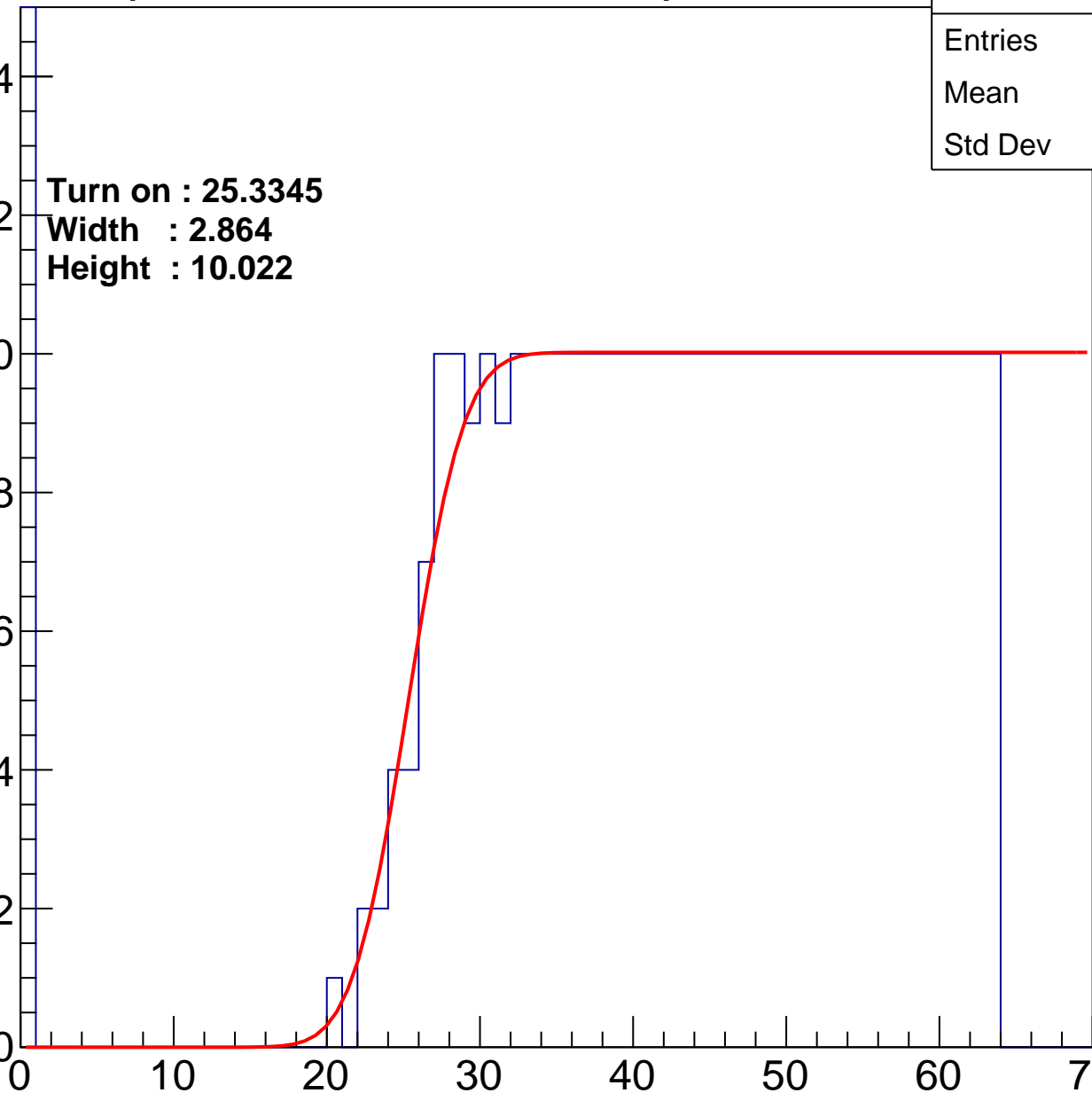
Width : 2.864

Height : 10.022

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U11-ch20

calib_packv5_041523_1651.root, FC#0, port C2

Entries	415
Mean	40.27
Std Dev	16.93

Turn on : 26.9778

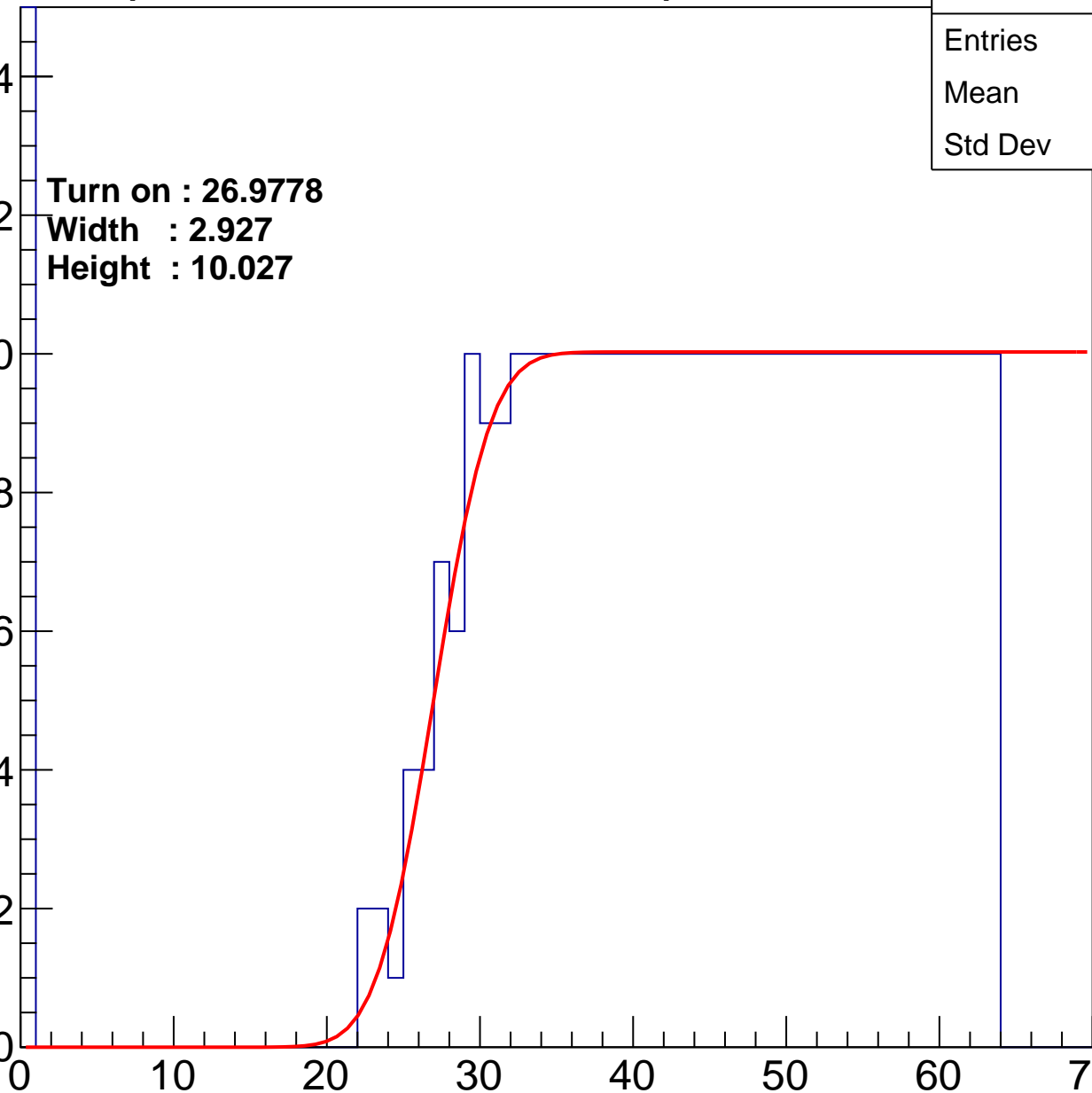
Width : 2.927

Height : 10.027

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U11-ch21

calib_packv5_041523_1651.root, FC#0, port C2

Entries	395
Mean	40.89
Std Dev	17.11

Turn on : 28.9990

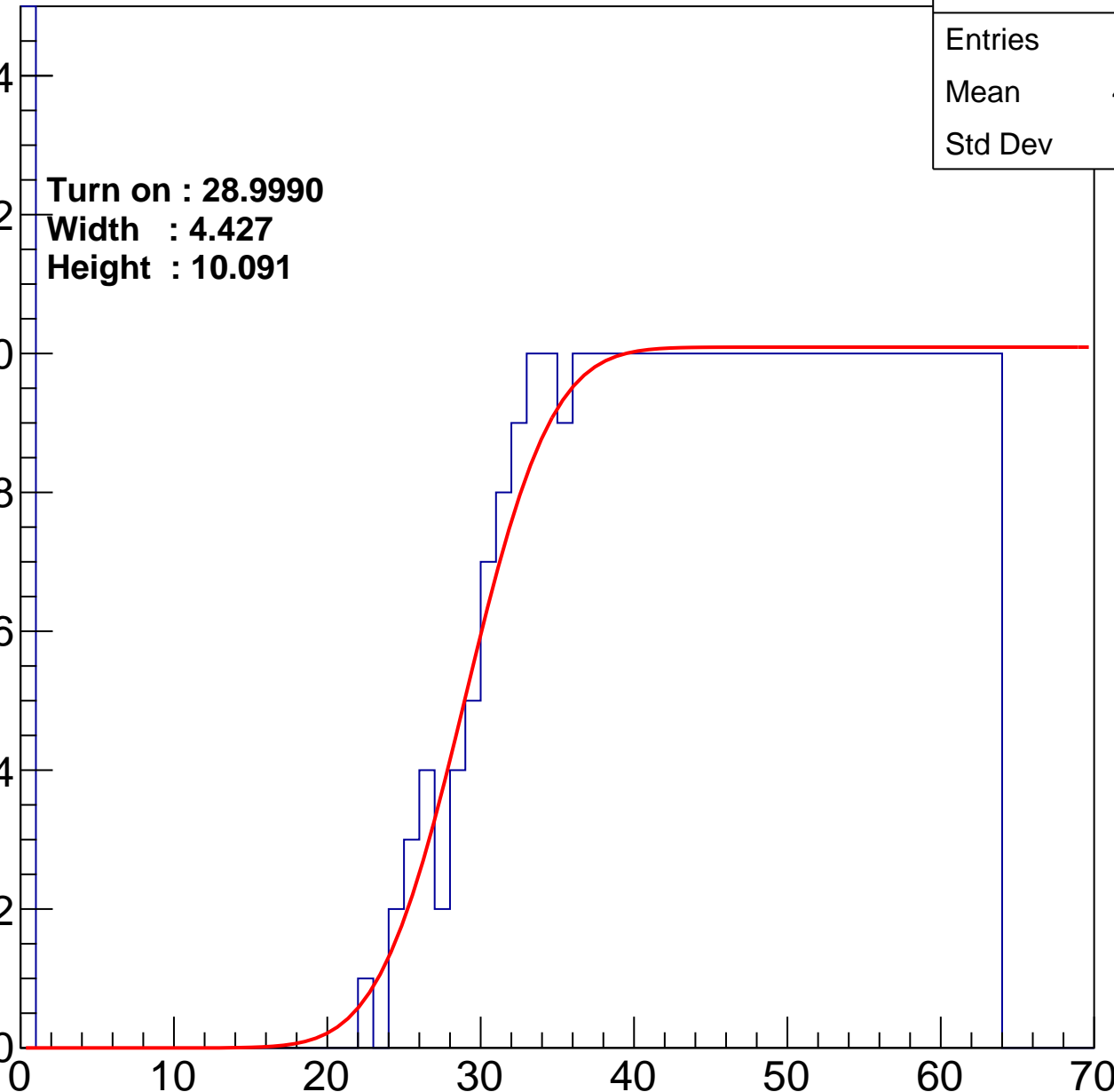
Width : 4.427

Height : 10.091

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U11-ch22

calib_packv5_041523_1651.root, FC#0, port C2

Entries	418
Mean	40.13
Std Dev	16.95

Turn on : 26.4545

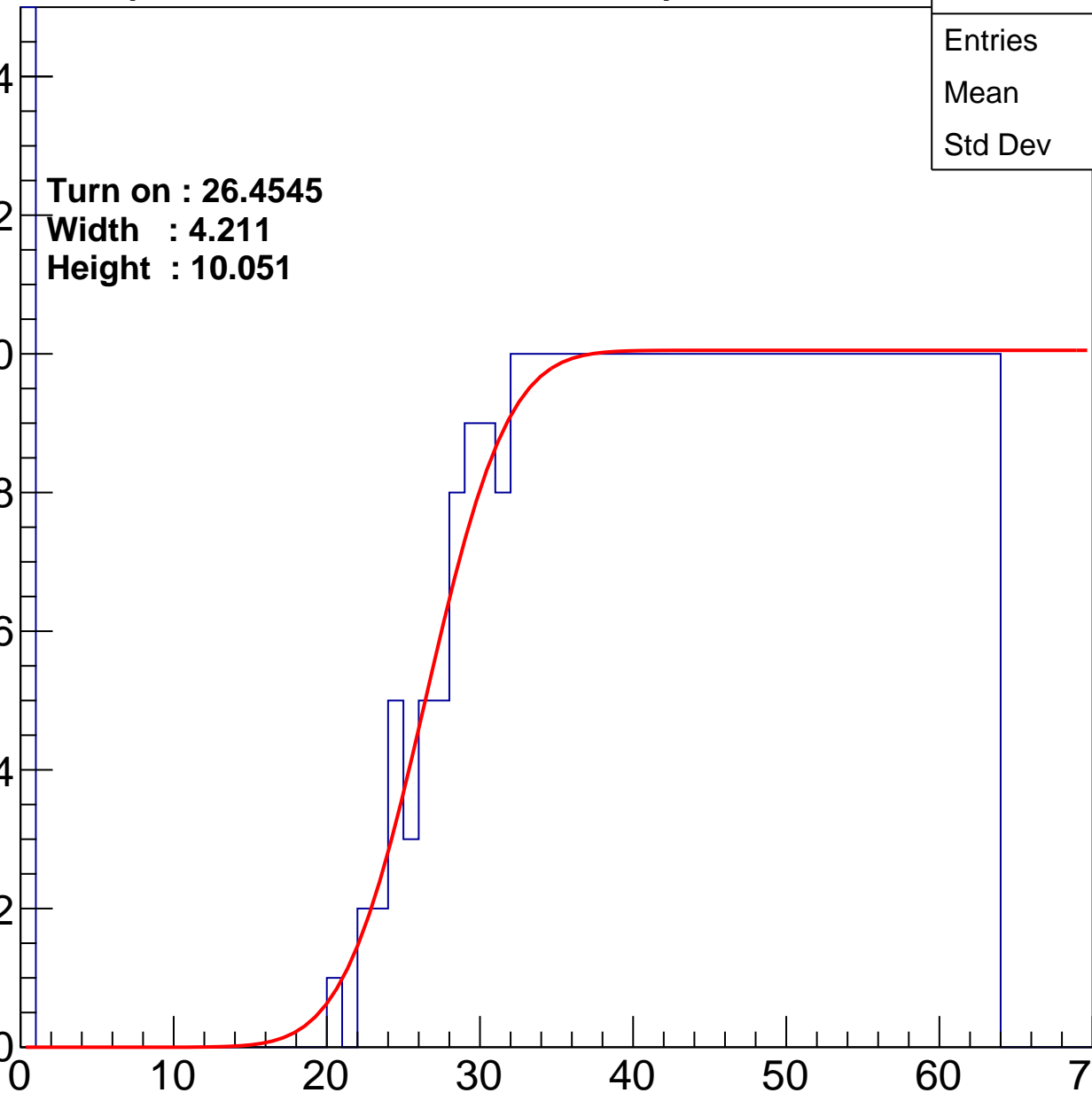
Width : 4.211

Height : 10.051

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U11-ch23

calib_packv5_041523_1651.root, FC#0, port C2

Entries	408
Mean	40.23
Std Dev	17.45

Turn on : 28.2718

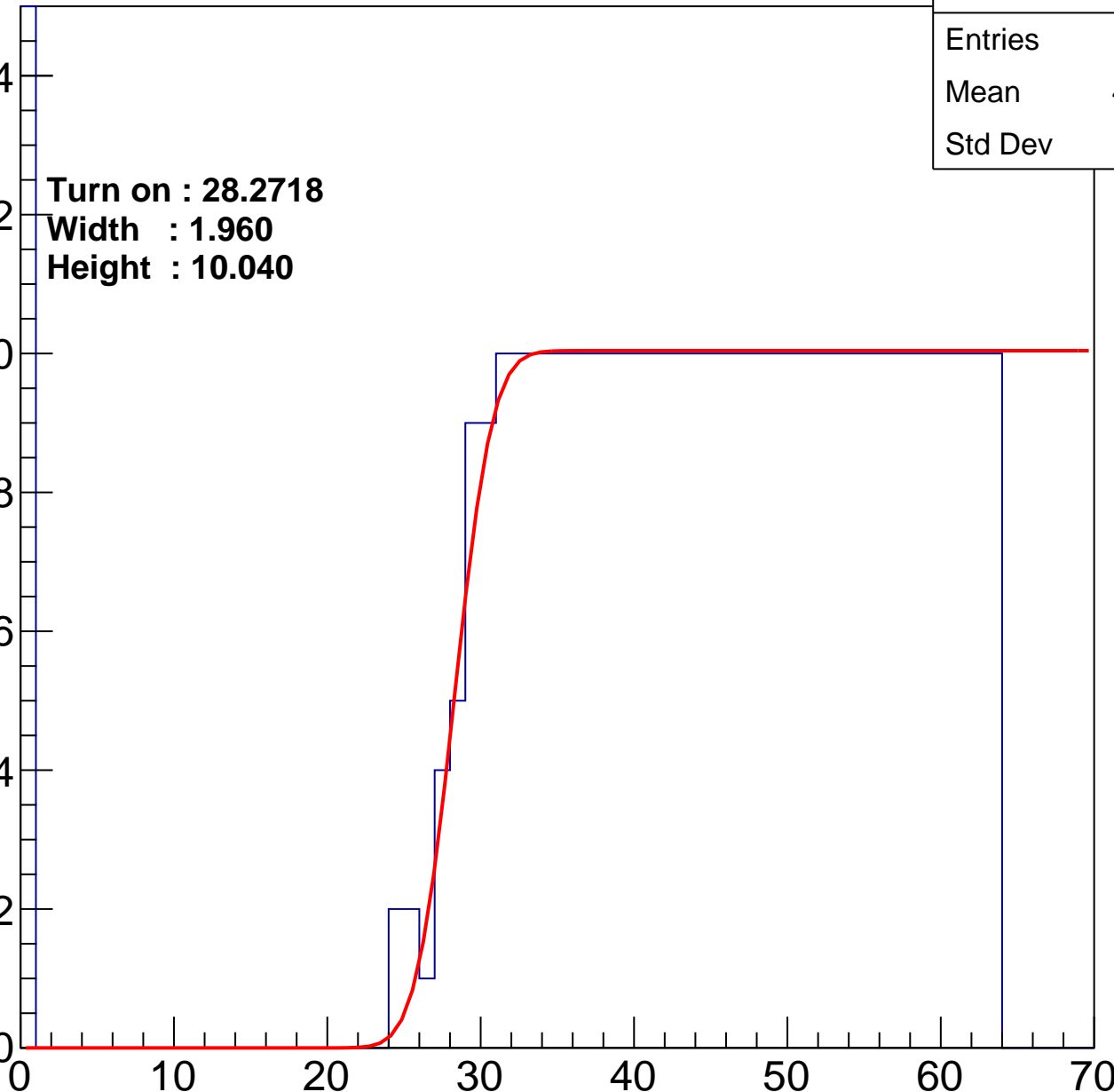
Width : 1.960

Height : 10.040

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U11-ch24

calib_packv5_041523_1651.root, FC#0, port C2

Entries	415
Mean	40.38
Std Dev	16.74

Turn on : 26.4065

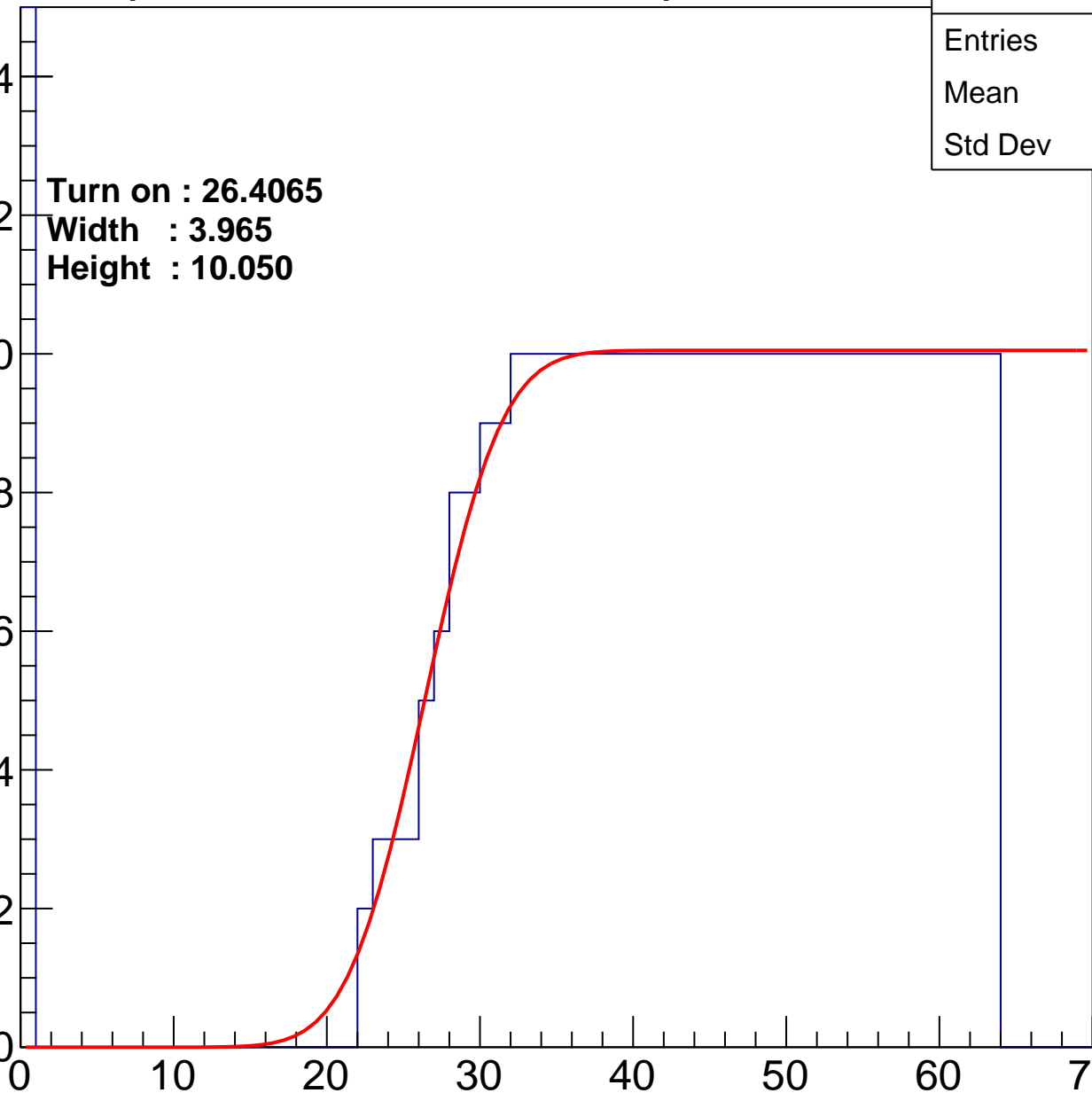
Width : 3.965

Height : 10.050

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U11-ch25

calib_packv5_041523_1651.root, FC#0, port C2

Entries	420
Mean	39.91
Std Dev	17.25

Turn on : 26.9185

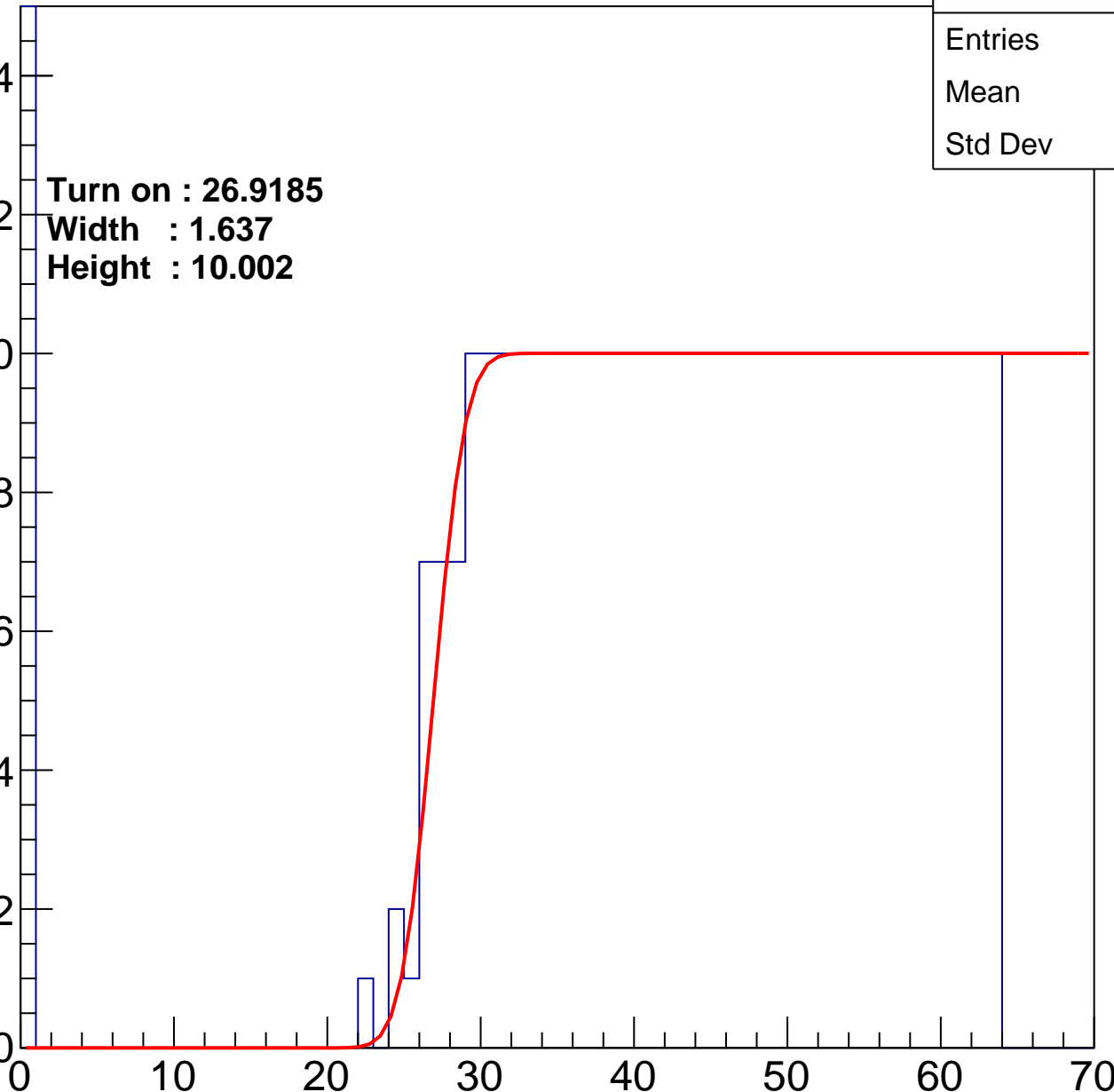
Width : 1.637

Height : 10.002

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U11-ch26

calib_packv5_041523_1651.root, FC#0, port C2

Entries	420
Mean	40.07
Std Dev	16.97

Turn on : 26.4720

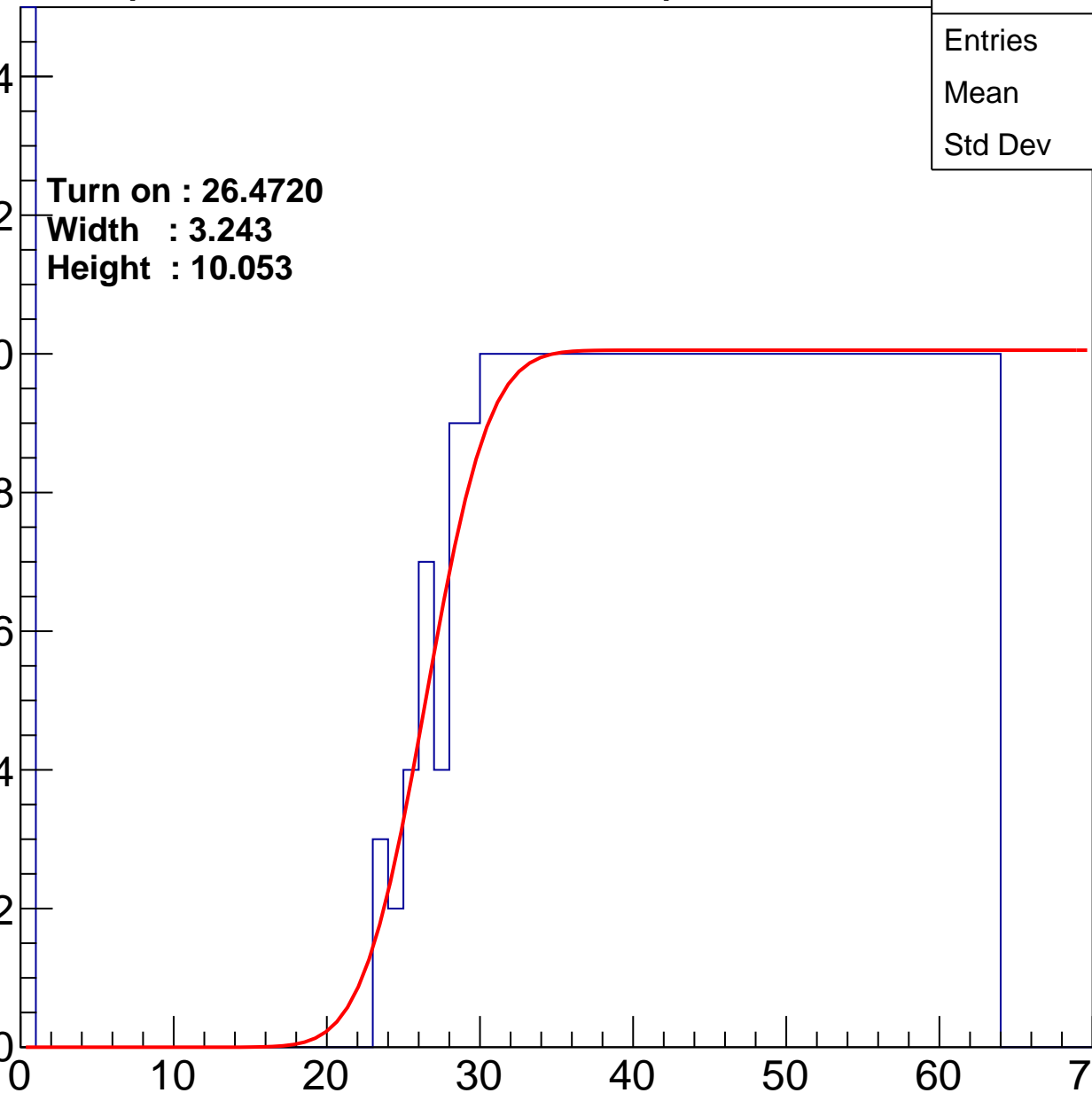
Width : 3.243

Height : 10.053

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U11-ch27

calib_packv5_041523_1651.root, FC#0, port C2

Entries	423
Mean	39.72
Std Dev	17.35

Turn on : 26.5938

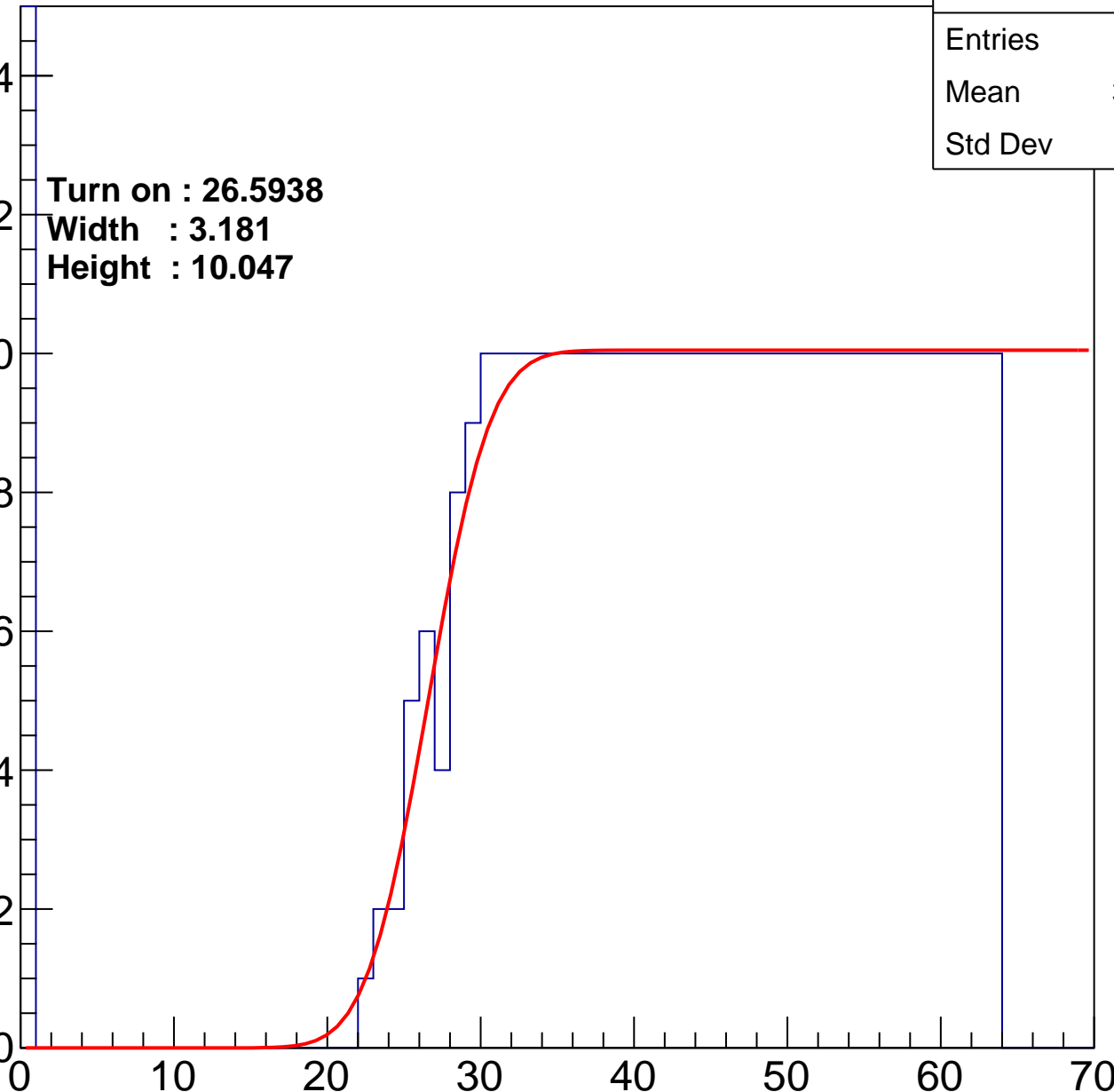
Width : 3.181

Height : 10.047

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U11-ch28

calib_packv5_041523_1651.root, FC#0, port C2

Entries	416
Mean	40.56
Std Dev	16.41

Turn on : 26.2216

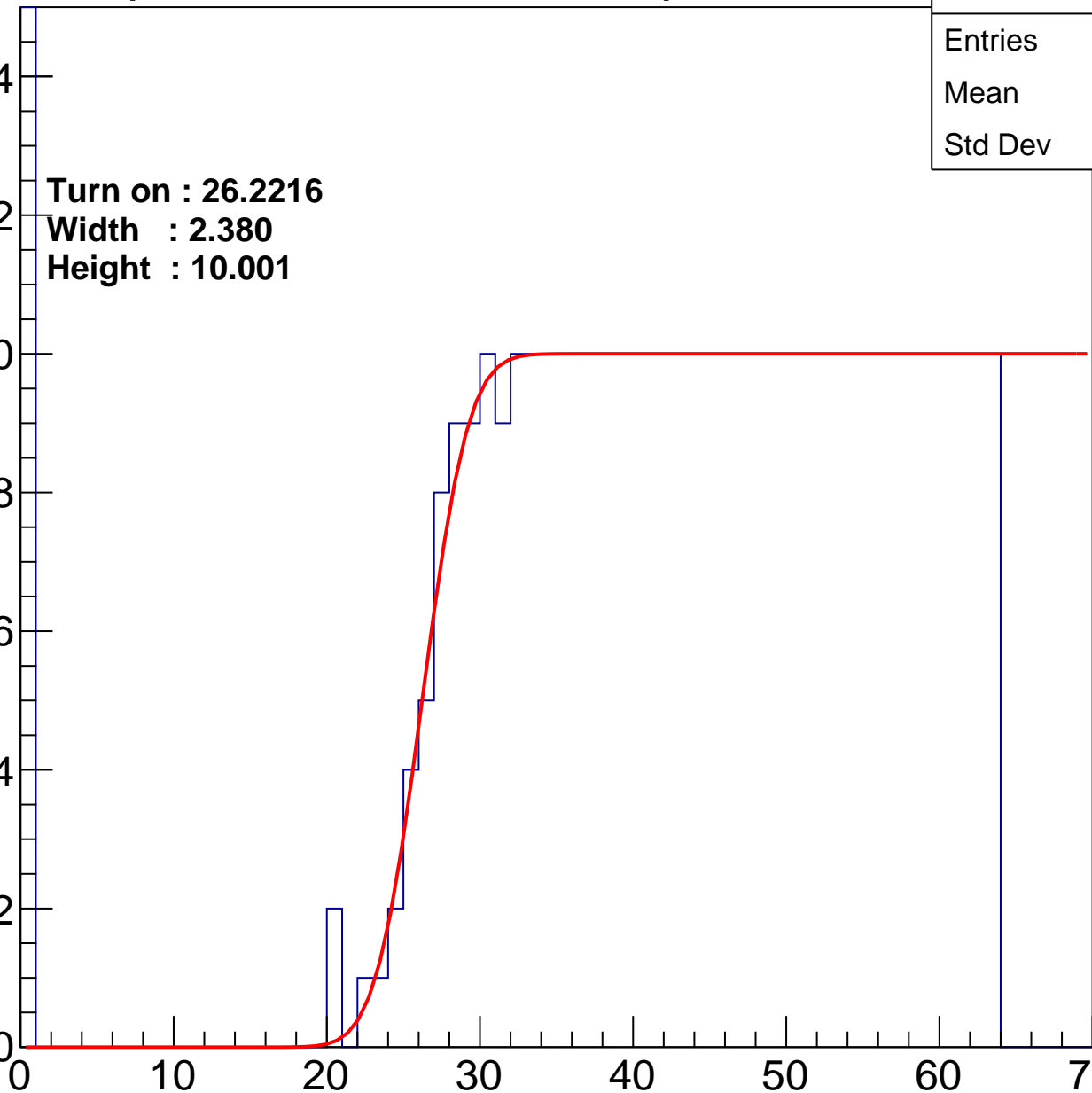
Width : 2.380

Height : 10.001

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U11-ch29

calib_packv5_041523_1651.root, FC#0, port C2

Entries	409
Mean	40.48
Std Dev	16.96

Turn on : 27.6893

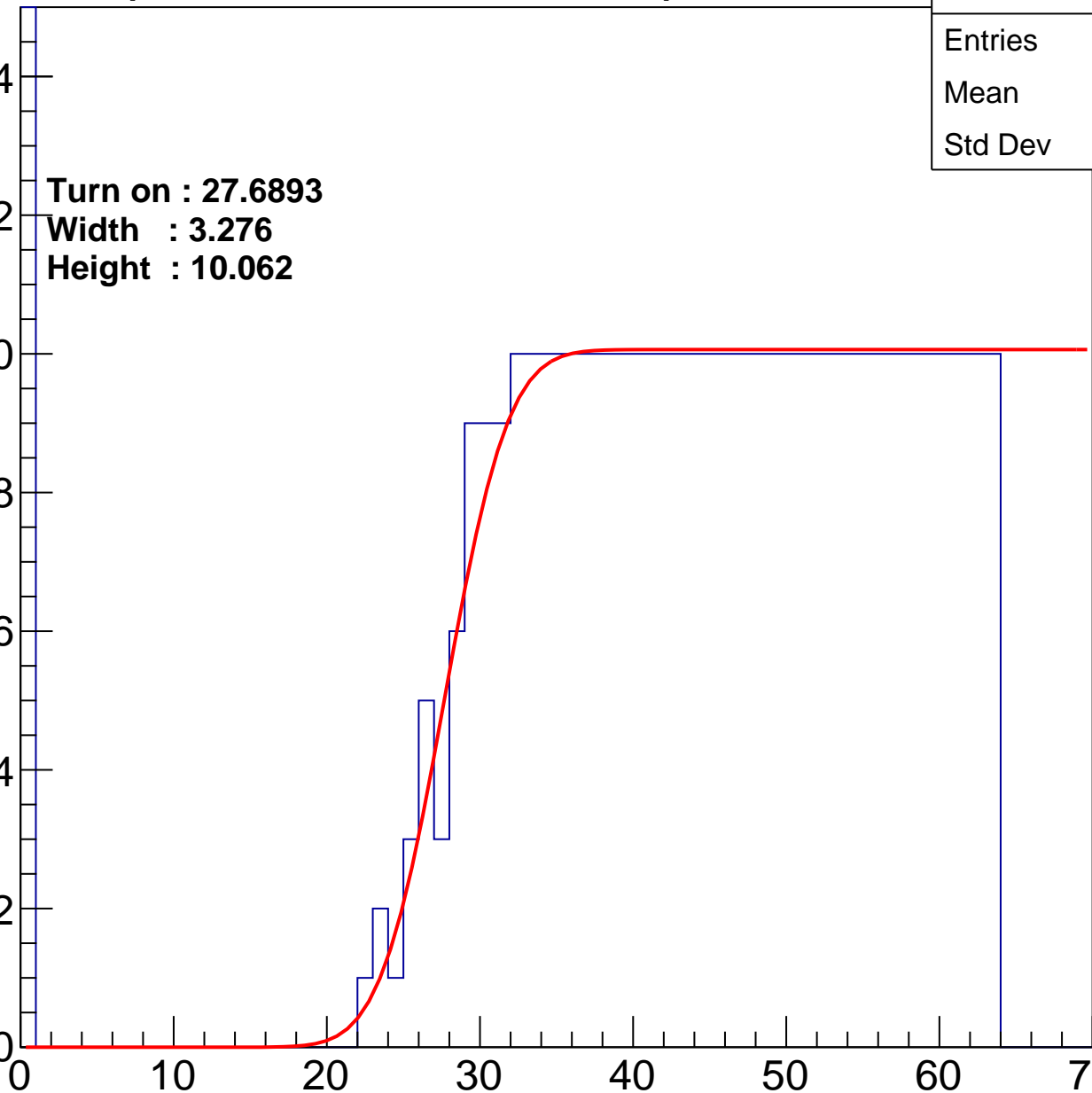
Width : 3.276

Height : 10.062

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U11-ch30

calib_packv5_041523_1651.root, FC#0, port C2

Entries	415
Mean	41.11
Std Dev	15.48

Turn on : 25.4627

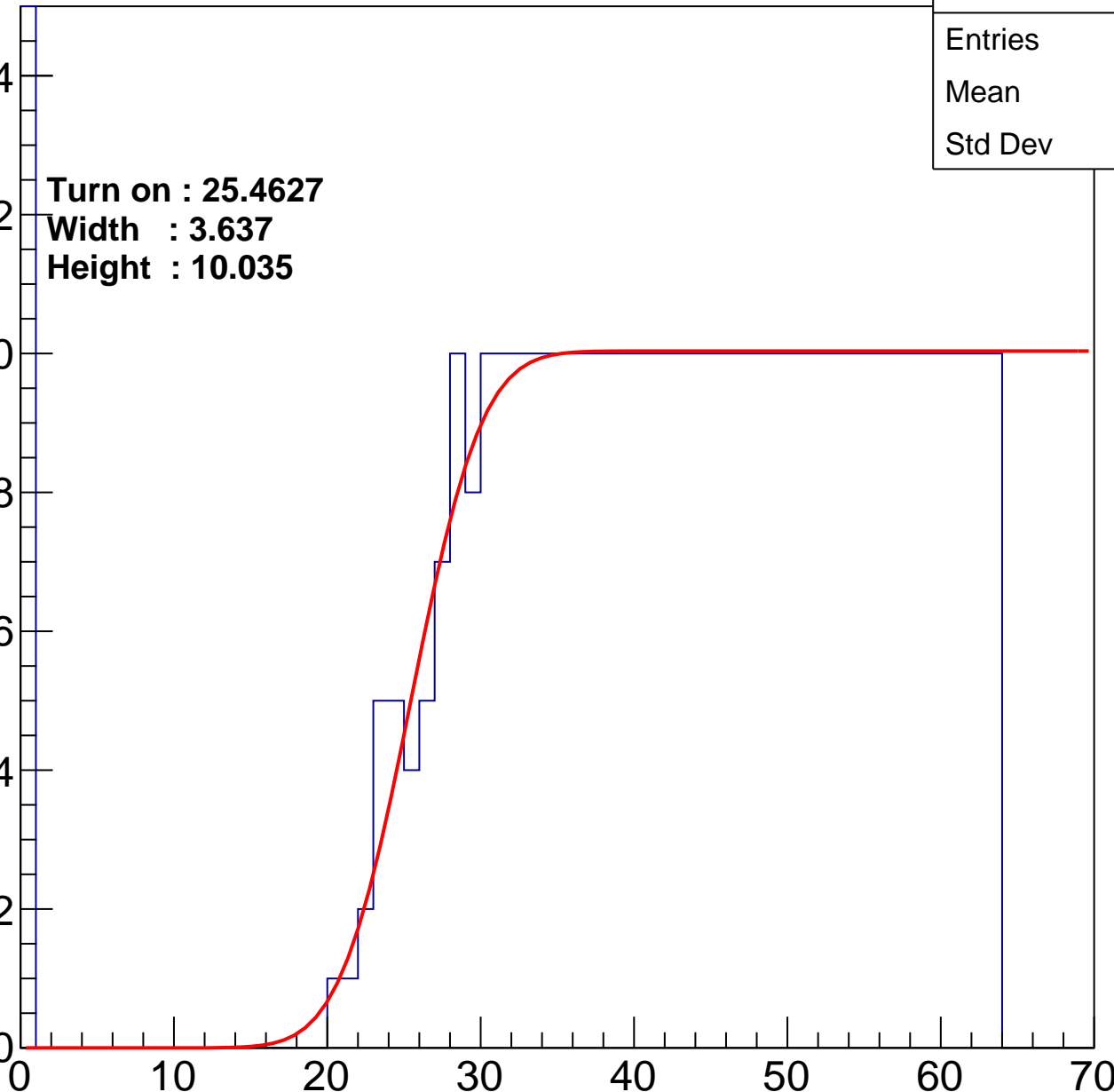
Width : 3.637

Height : 10.035

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U11-ch31

calib_packv5_041523_1651.root, FC#0, port C2

Entries	391
Mean	41.04
Std Dev	17.12

Turn on : 29.1963

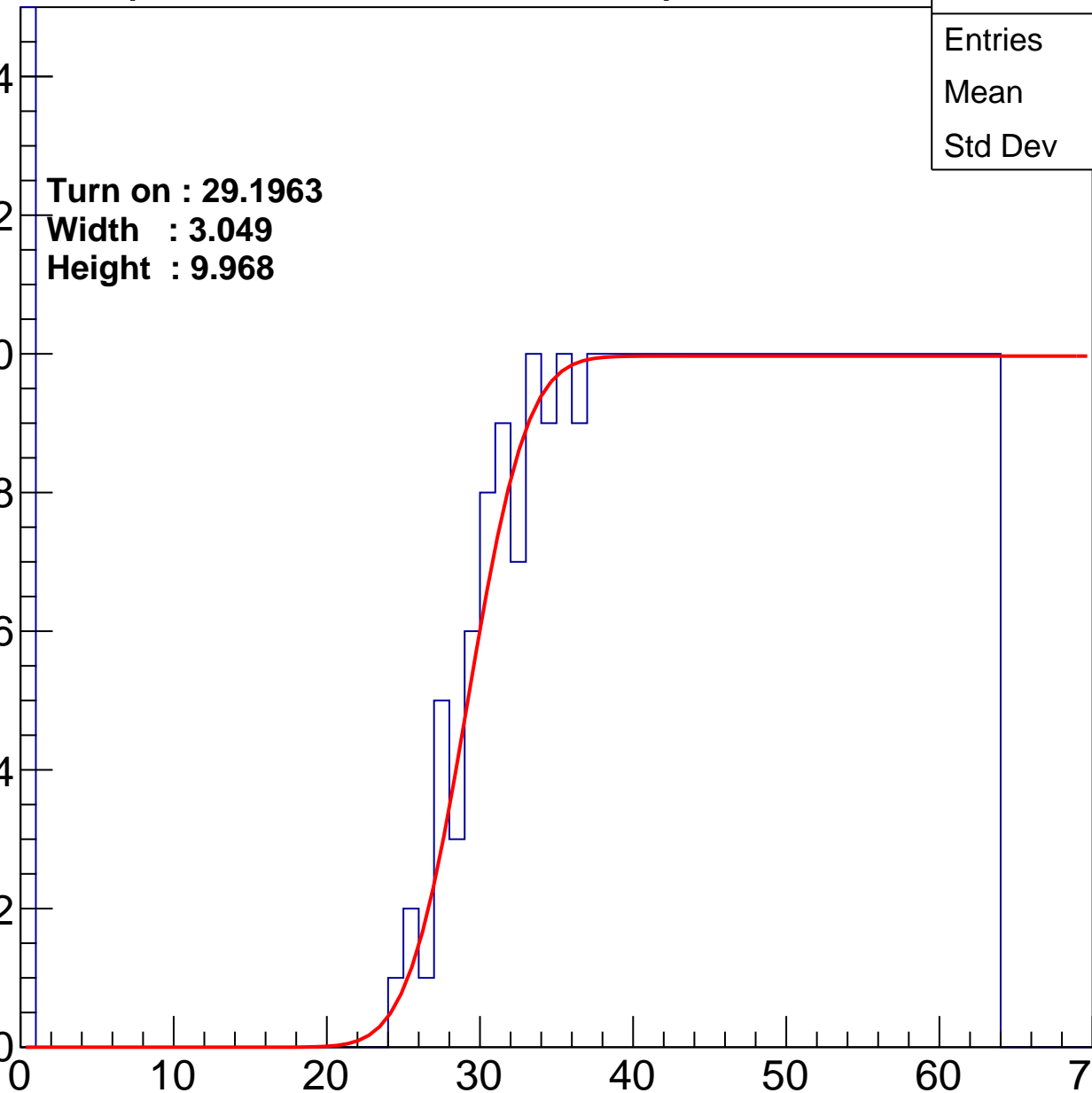
Width : 3.049

Height : 9.968

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U11-ch32

calib_packv5_041523_1651.root, FC#0, port C2

Entries	408
Mean	40.69
Std Dev	16.67

Turn on : 27.1277

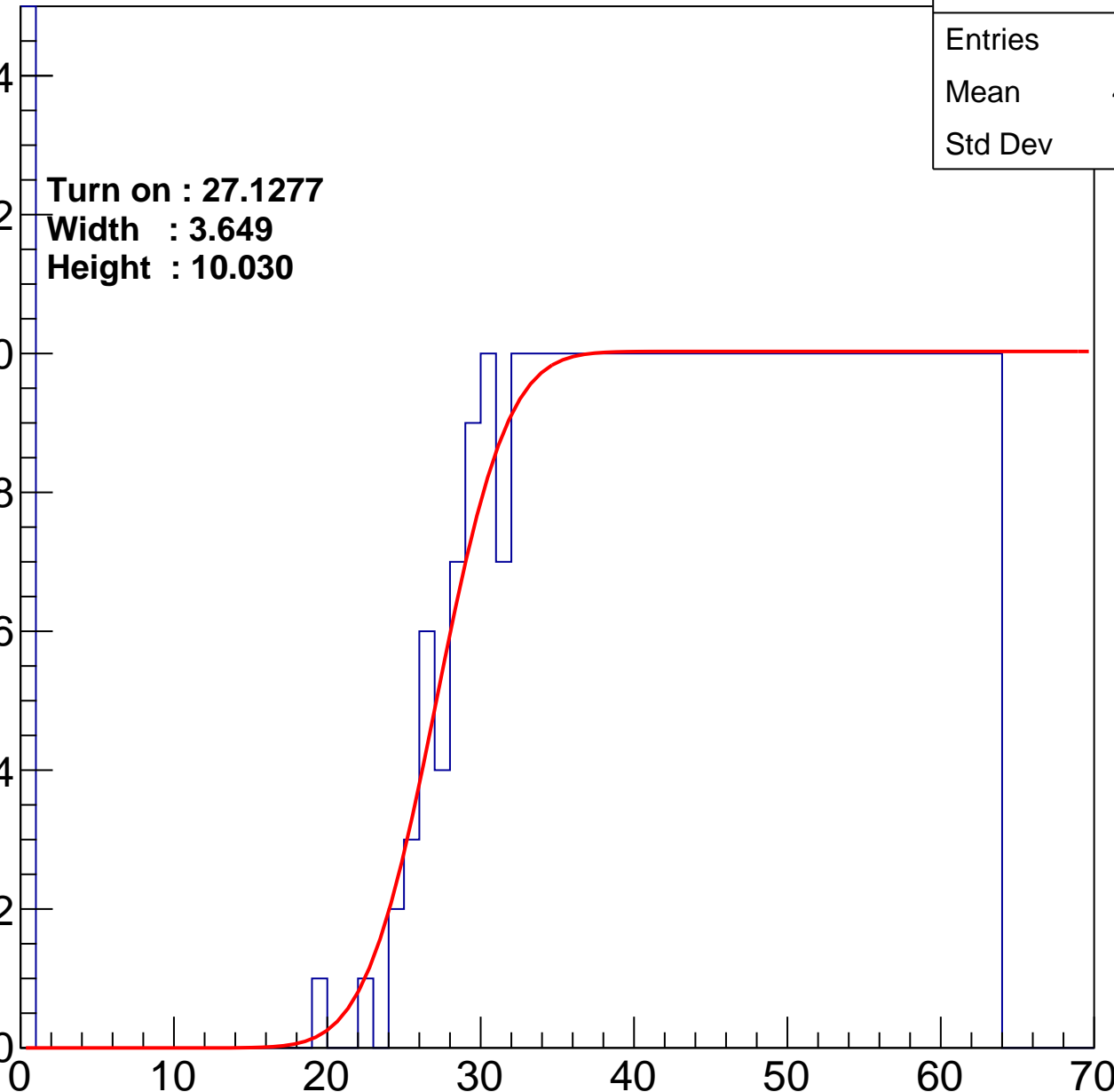
Width : 3.649

Height : 10.030

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U11-ch33

calib_packv5_041523_1651.root, FC#0, port C2

Entries	418
Mean	39.89
Std Dev	17.38

Turn on : 27.2185

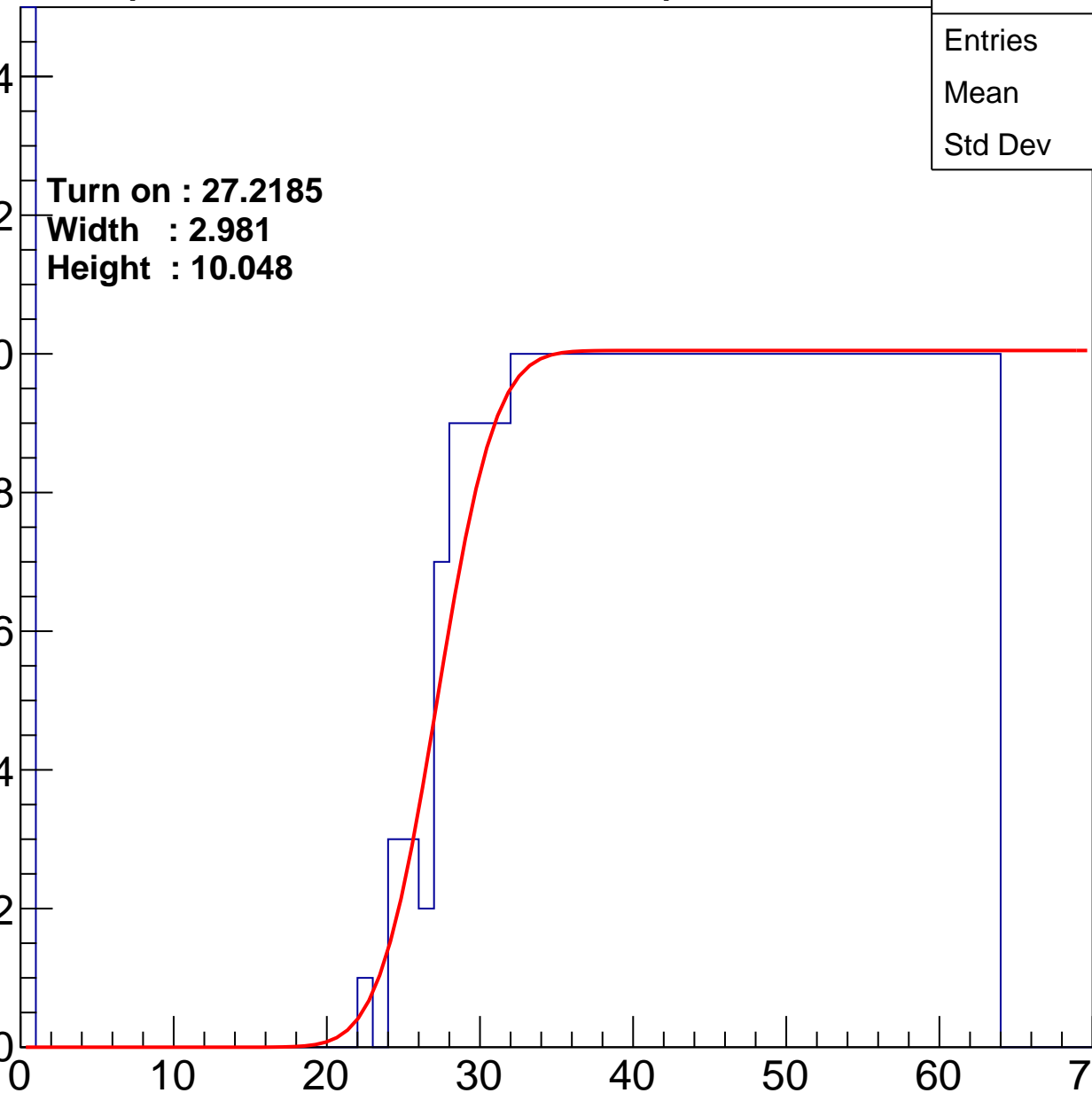
Width : 2.981

Height : 10.048

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U11-ch34

calib_packv5_041523_1651.root, FC#0, port C2

Entries	430
Mean	39.69
Std Dev	16.97

Turn on : 25.6198

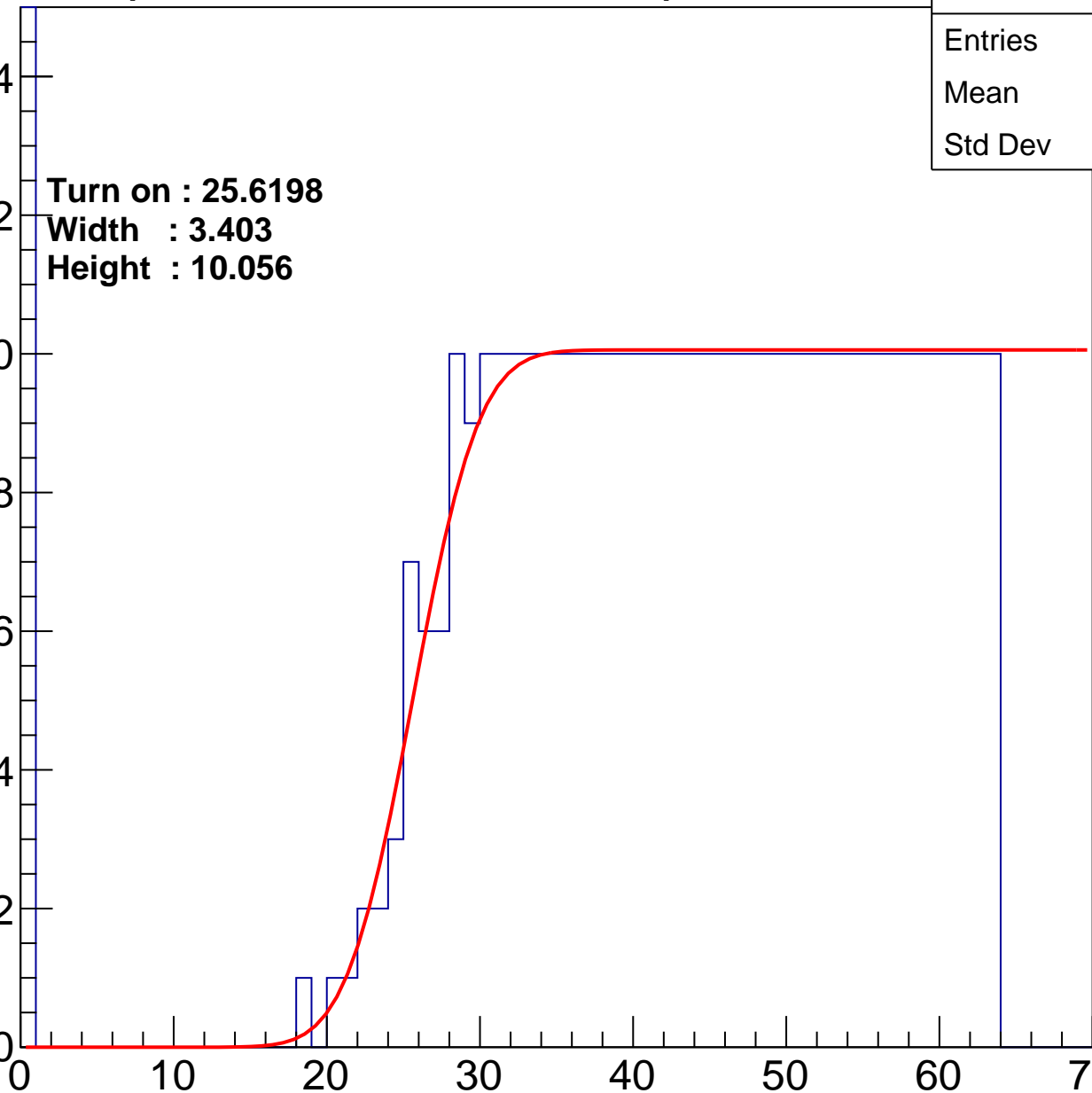
Width : 3.403

Height : 10.056

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U11-ch35

calib_packv5_041523_1651.root, FC#0, port C2

Entries	407
Mean	40.95
Std Dev	16.32

Turn on : 27.3503

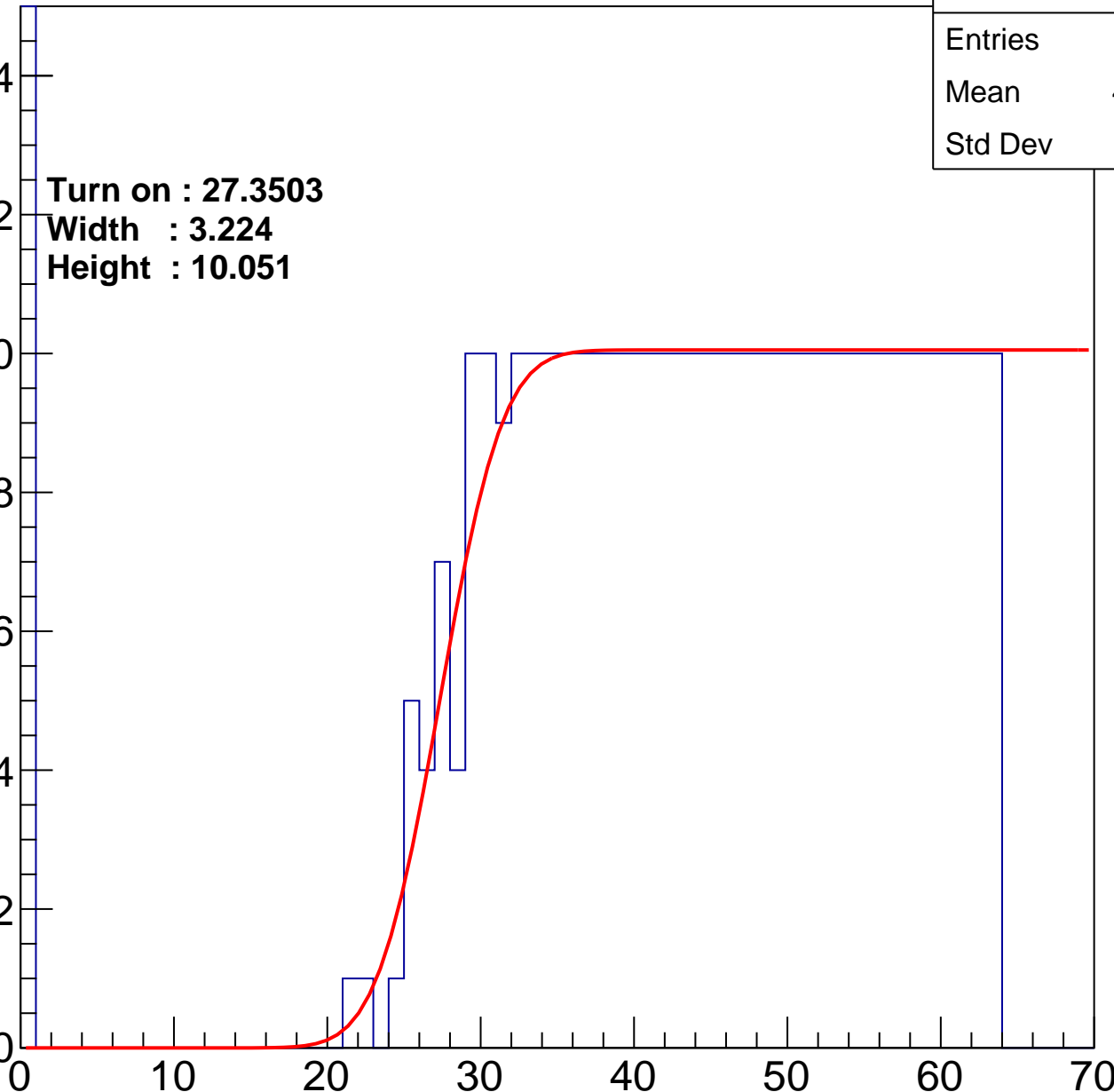
Width : 3.224

Height : 10.051

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U11-ch36

calib_packv5_041523_1651.root, FC#0, port C2

Entries	422
Mean	39.76
Std Dev	17.34

Turn on : 26.4781

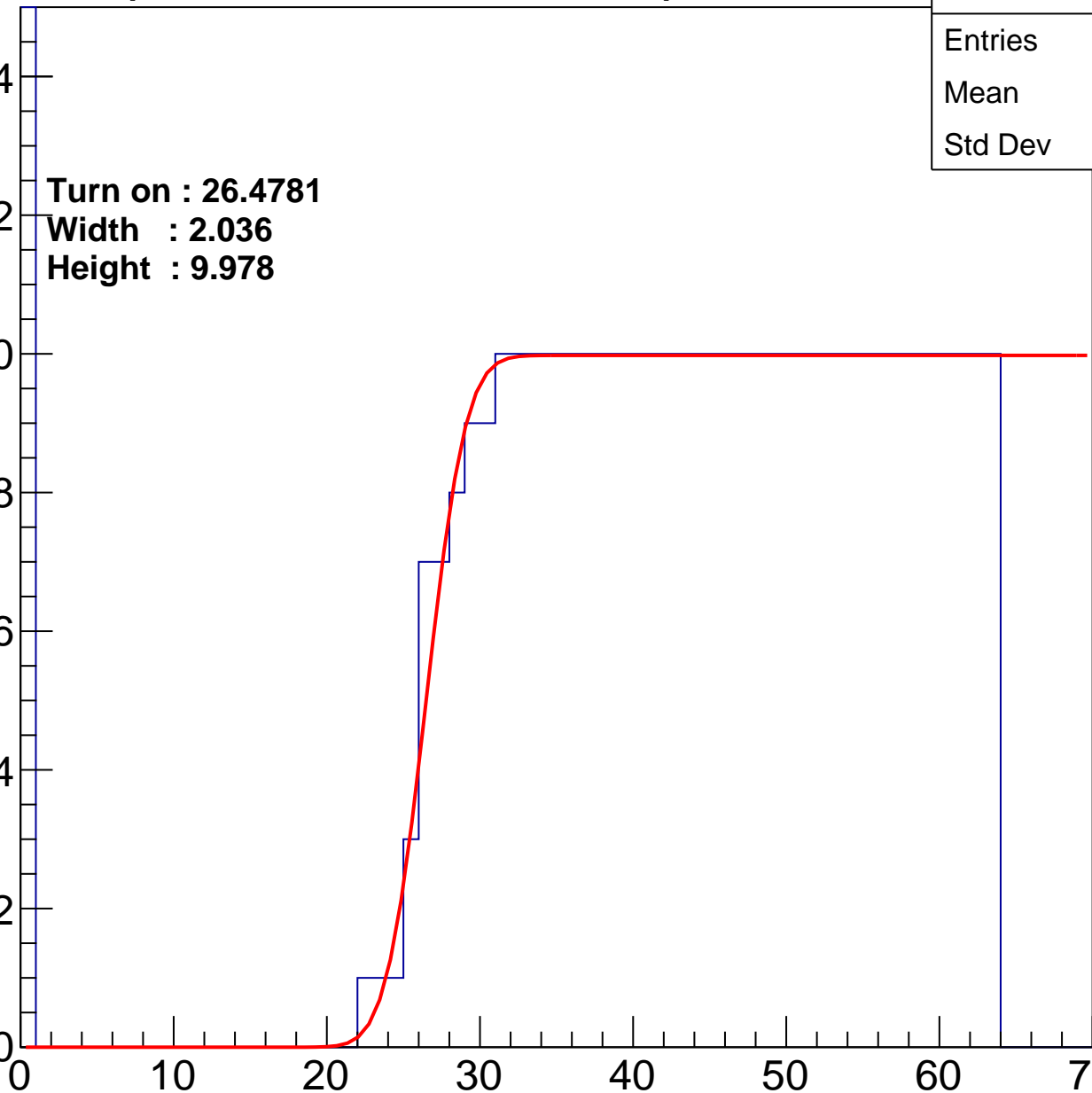
Width : 2.036

Height : 9.978

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U11-ch37

calib_packv5_041523_1651.root, FC#0, port C2

Entries	409
Mean	40.73
Std Dev	16.55

Turn on : 26.9464

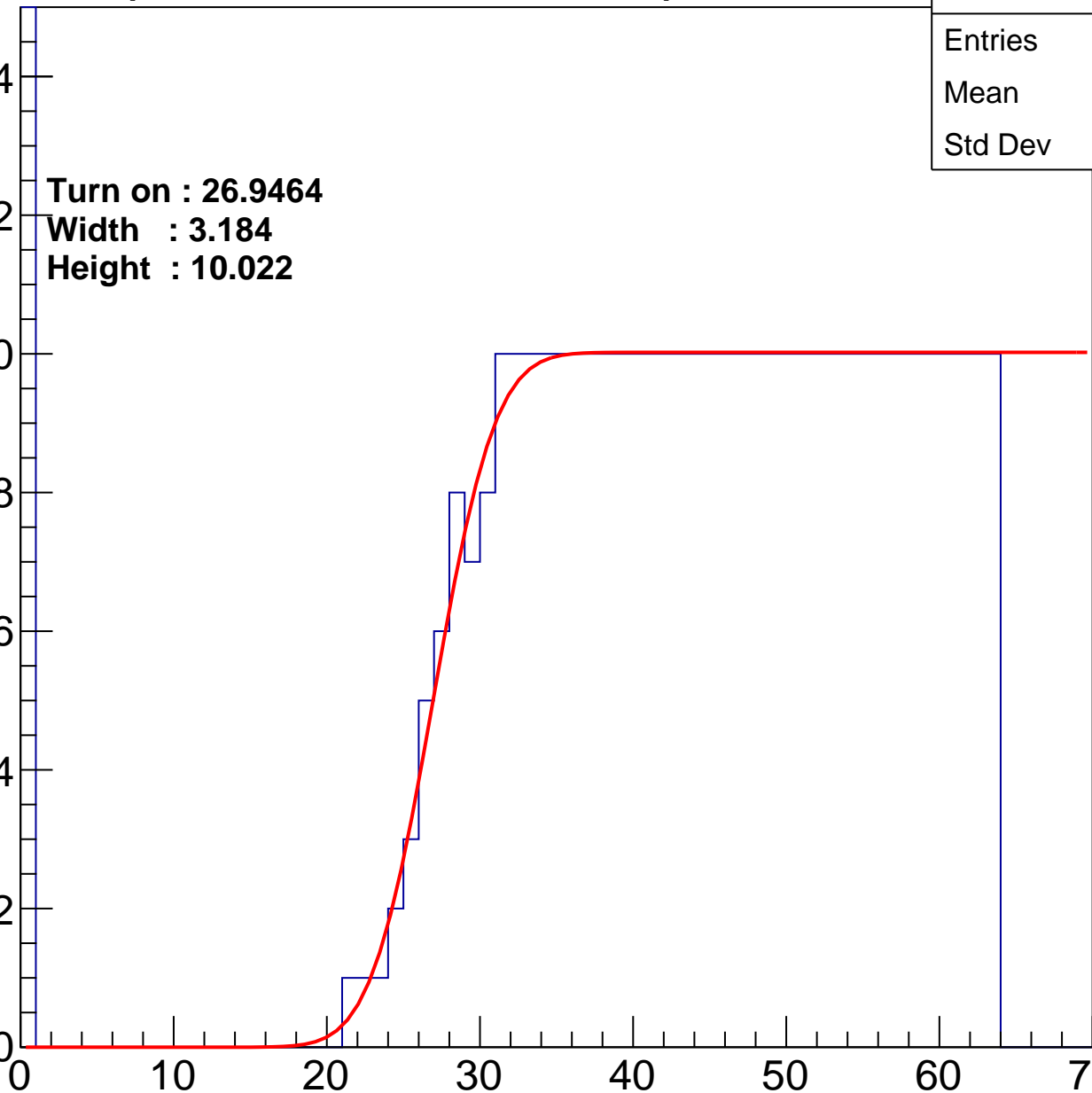
Width : 3.184

Height : 10.022

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U11-ch38

calib_packv5_041523_1651.root, FC#0, port C2

Entries	444
Mean	39.05
Std Dev	17.16

Turn on : 24.1856

Width : 2.528

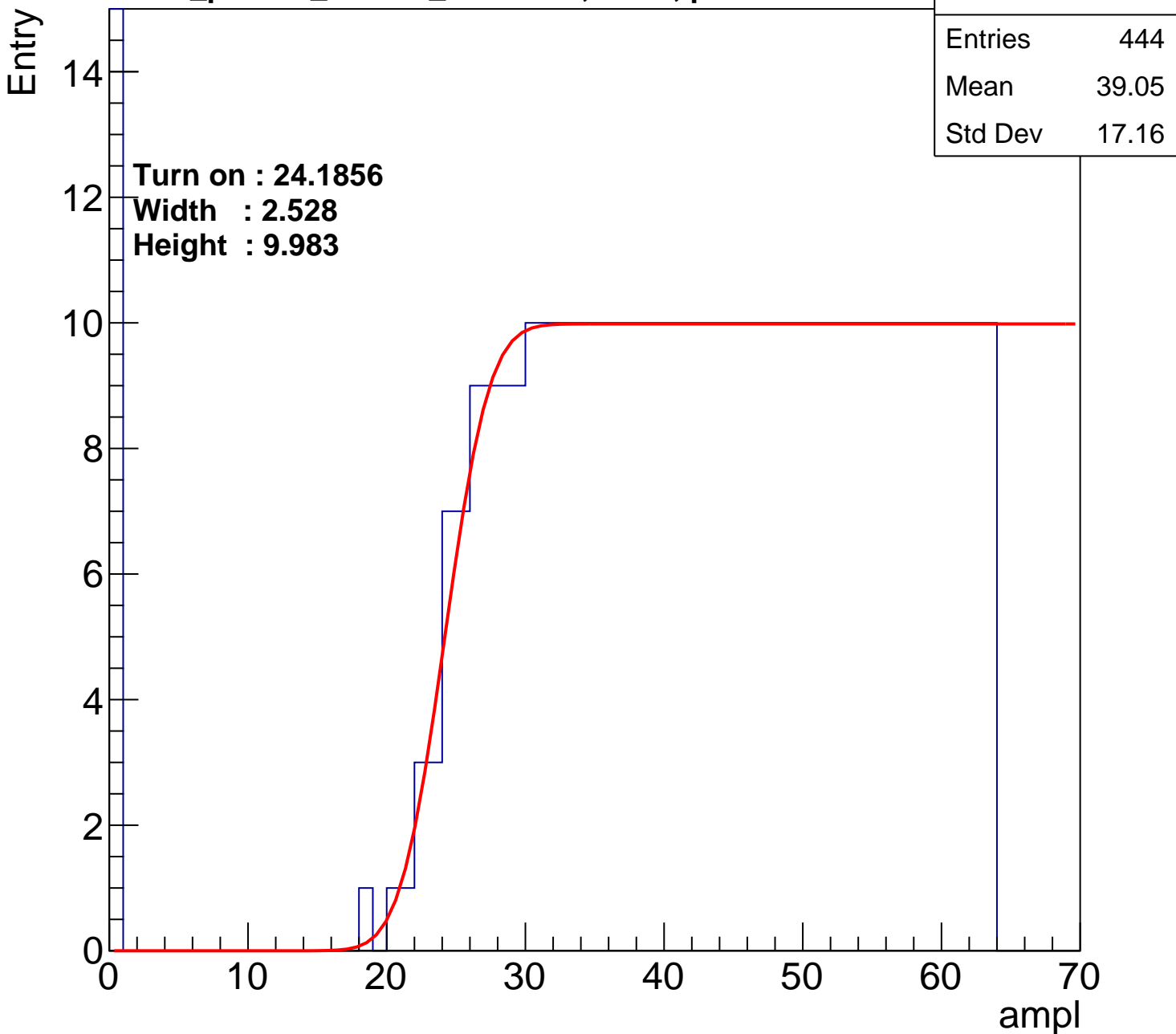
Height : 9.983

Entry

14
12
10
8
6
4
2
0

ampl

0 10 20 30 40 50 60 70



B1L103S, U11-ch39

calib_packv5_041523_1651.root, FC#0, port C2

Entries	419
Mean	39.97
Std Dev	17.19

Turn on : 26.9233

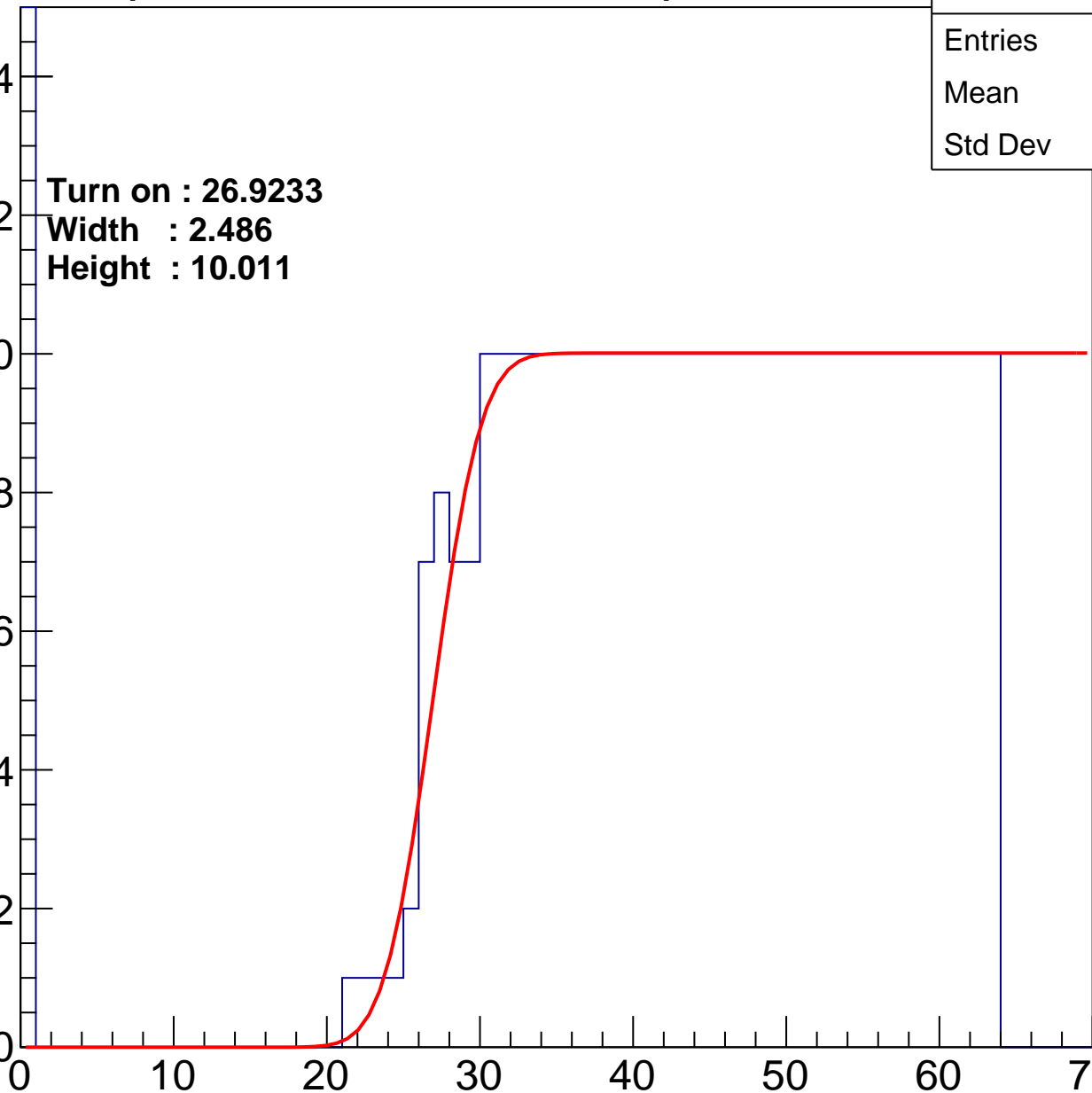
Width : 2.486

Height : 10.011

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U11-ch40

calib_packv5_041523_1651.root, FC#0, port C2

Entries	420
Mean	40.16
Std Dev	17

Turn on : 26.6064

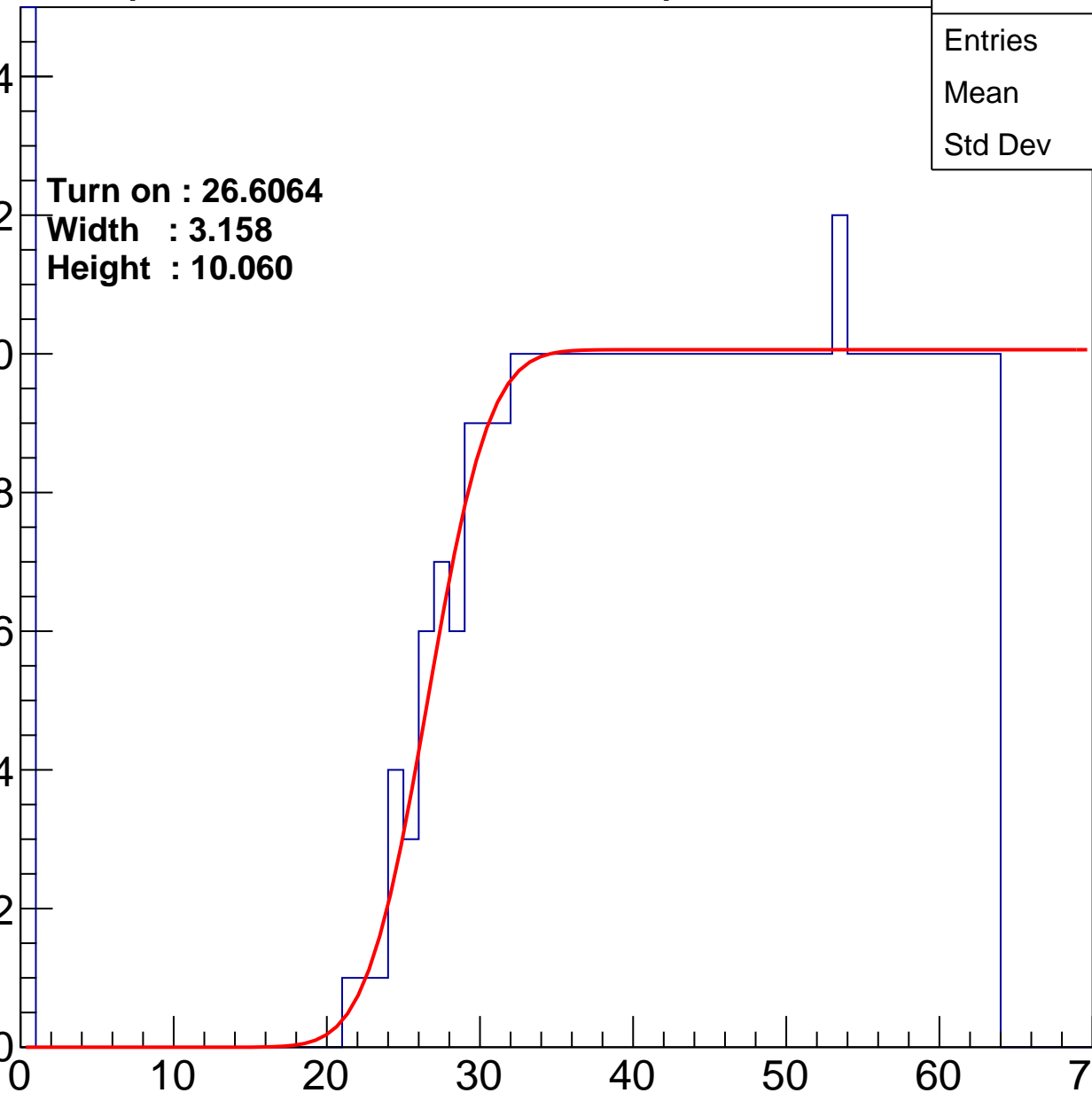
Width : 3.158

Height : 10.060

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U11-ch41

calib_packv5_041523_1651.root, FC#0, port C2

Entries	435
Mean	38.62
Std Dev	18.3

Turn on : 26.5401

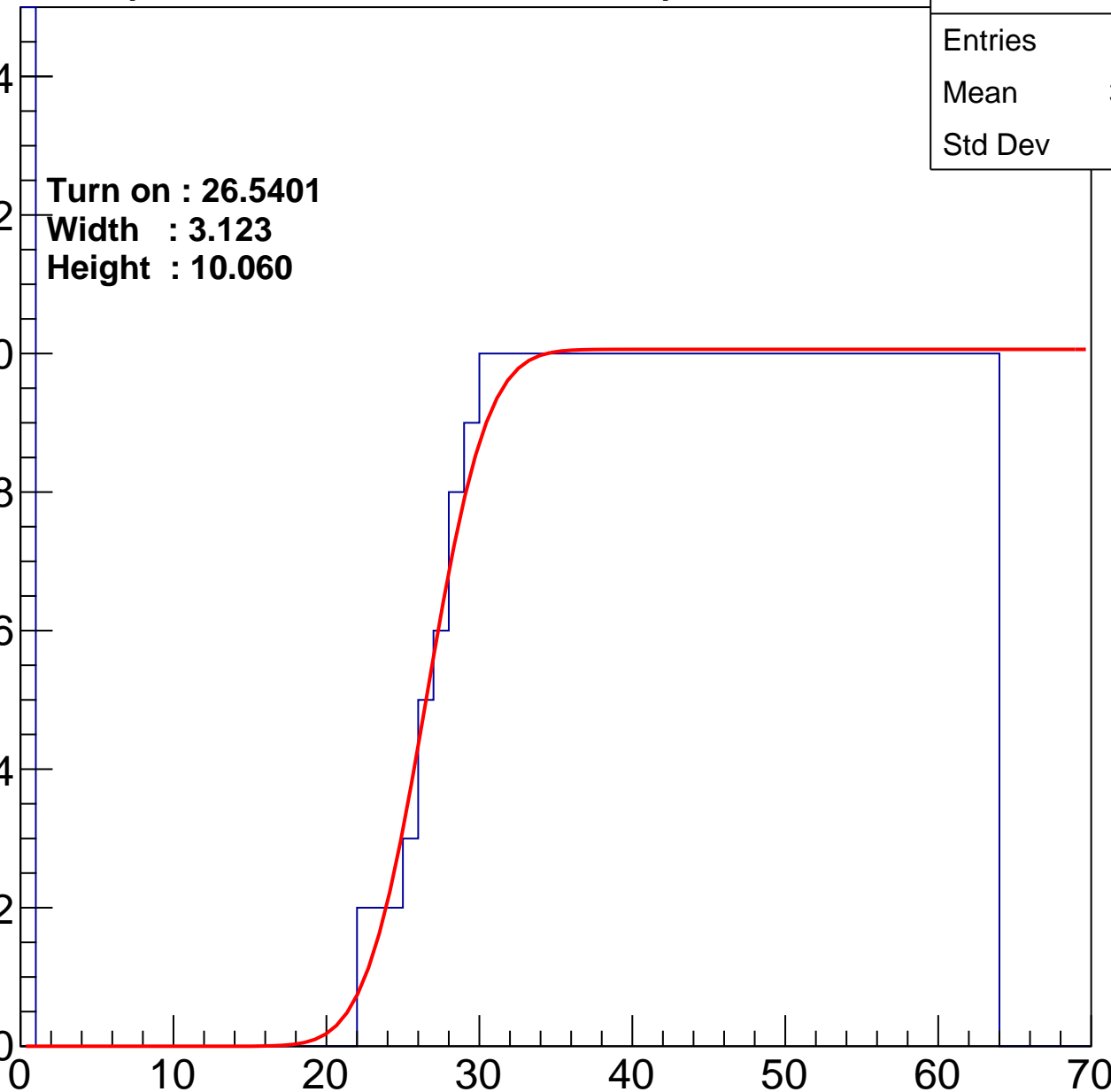
Width : 3.123

Height : 10.060

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U11-ch42

calib_packv5_041523_1651.root, FC#0, port C2

Entries	407
Mean	40.36
Std Dev	17.28

Turn on : 27.6735

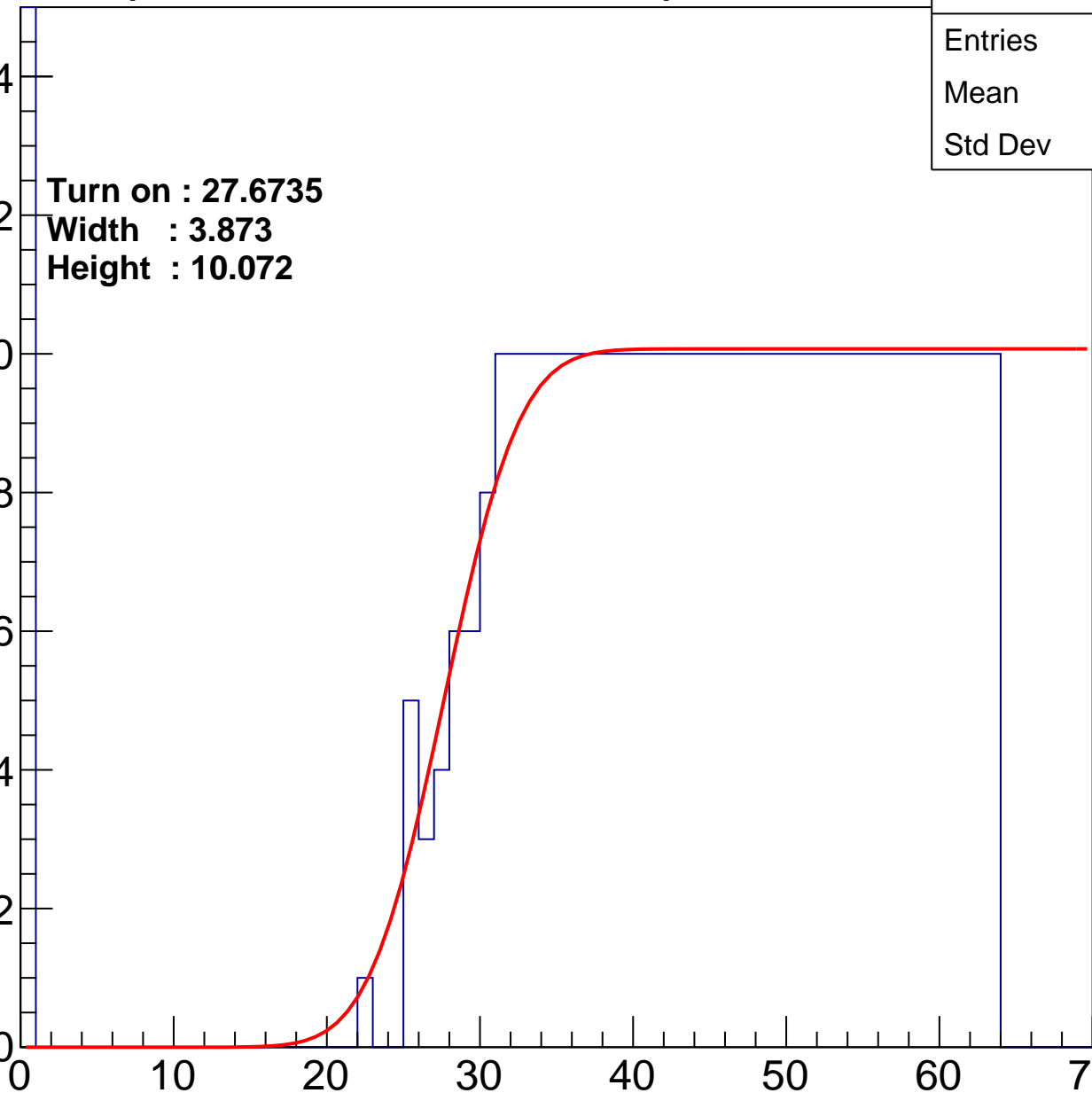
Width : 3.873

Height : 10.072

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U11-ch43

calib_packv5_041523_1651.root, FC#0, port C2

Entries	404
Mean	40.48
Std Dev	17.23

Turn on : 27.9008

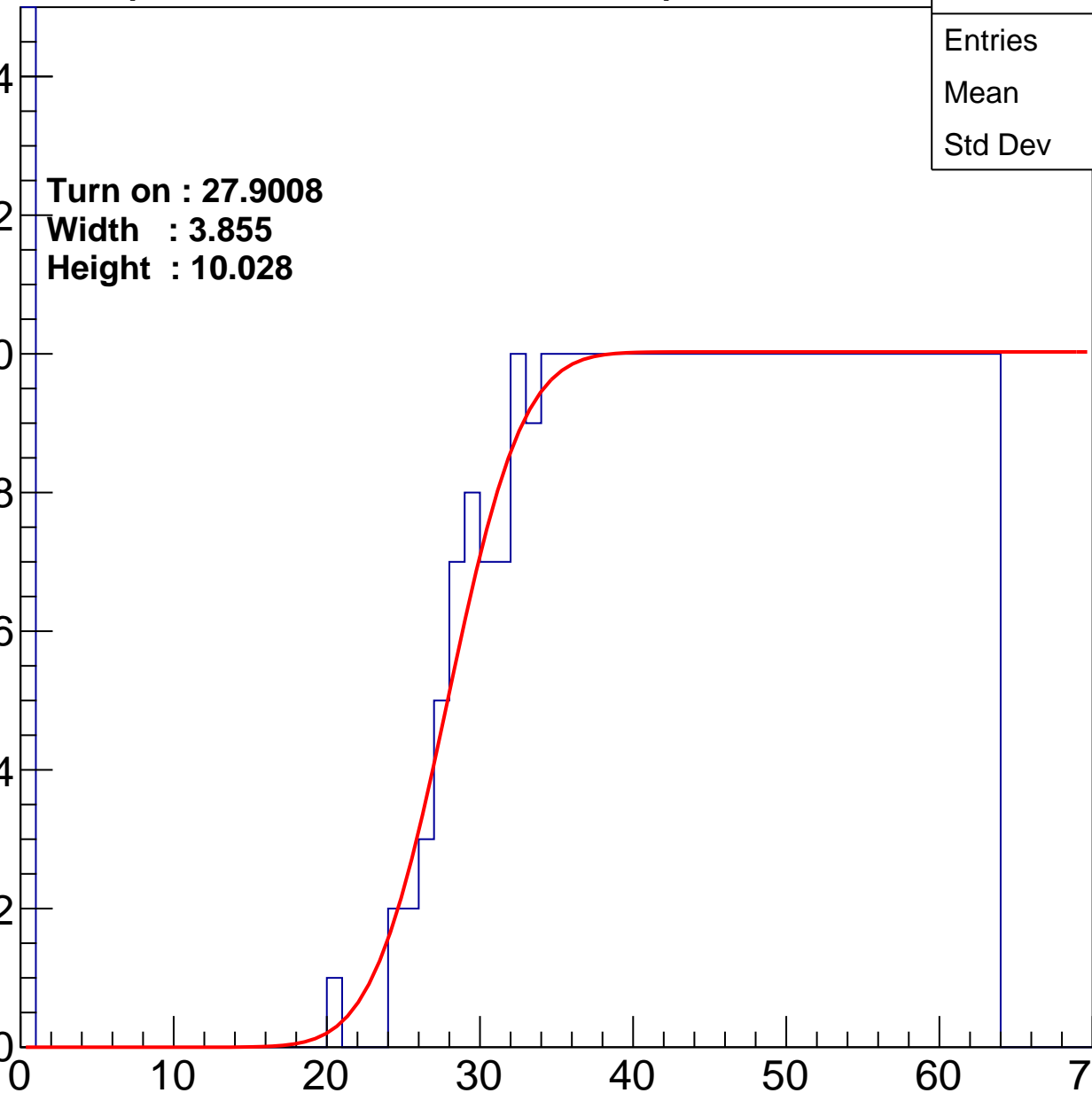
Width : 3.855

Height : 10.028

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U11-ch44

calib_packv5_041523_1651.root, FC#0, port C2

Entries	416
Mean	40.74
Std Dev	16.09

Turn on : 25.6586

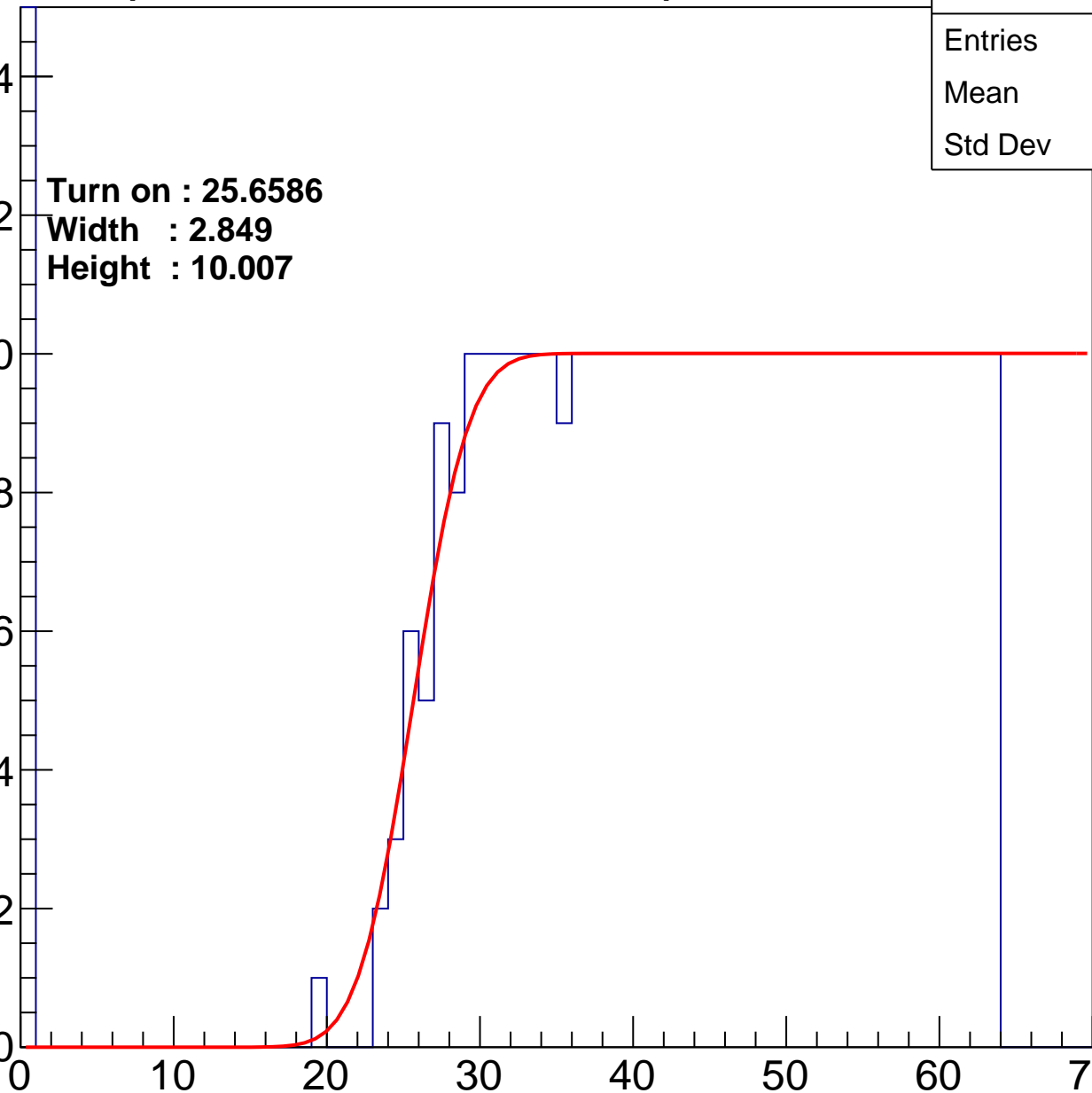
Width : 2.849

Height : 10.007

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U11-ch45

calib_packv5_041523_1651.root, FC#0, port C2

Entries	397
Mean	41.44
Std Dev	16.14

Turn on : 27.9840

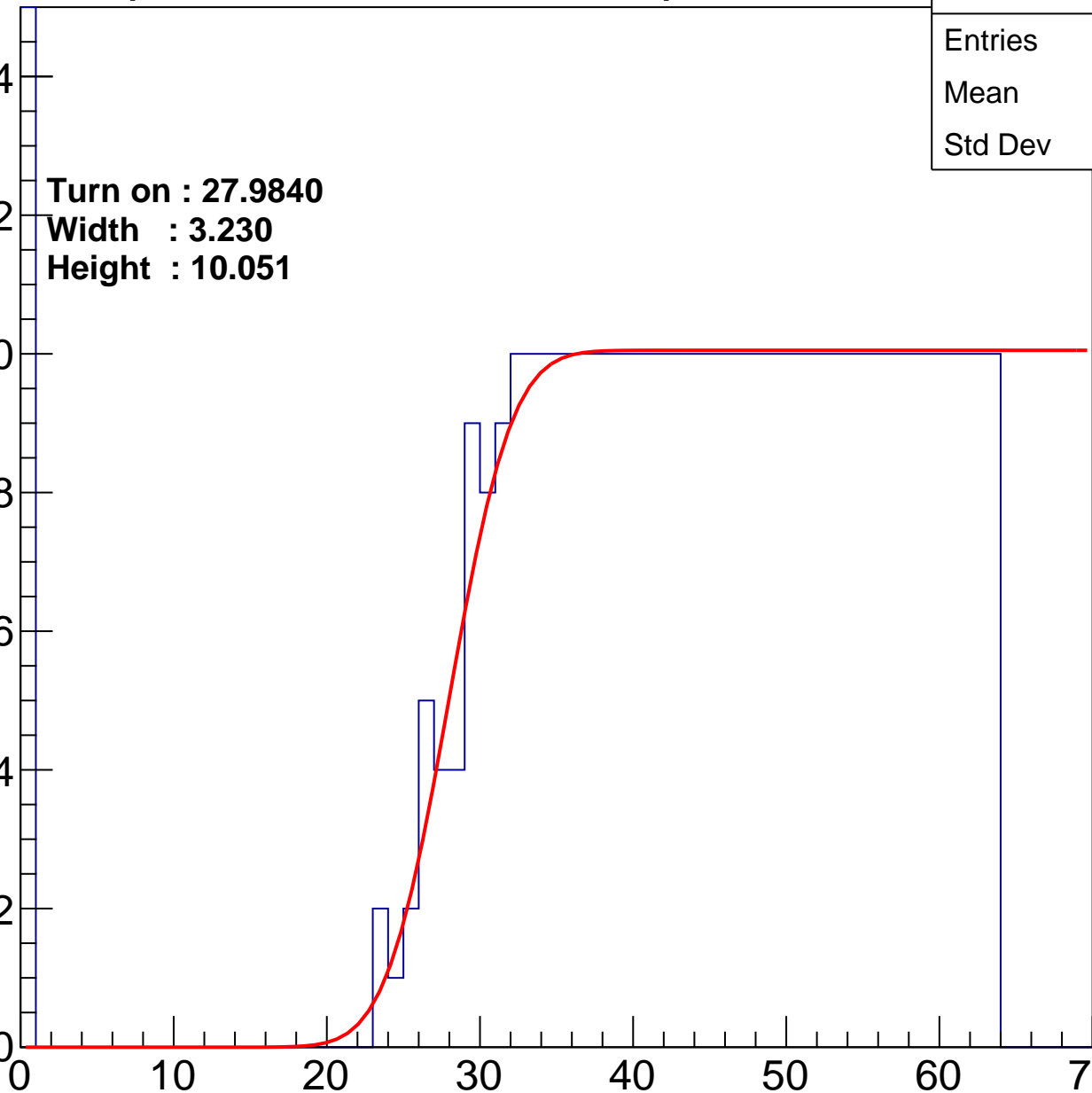
Width : 3.230

Height : 10.051

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U11-ch46

calib_packv5_041523_1651.root, FC#0, port C2

Entries	434
Mean	39.11
Std Dev	17.64

Turn on : 25.9426

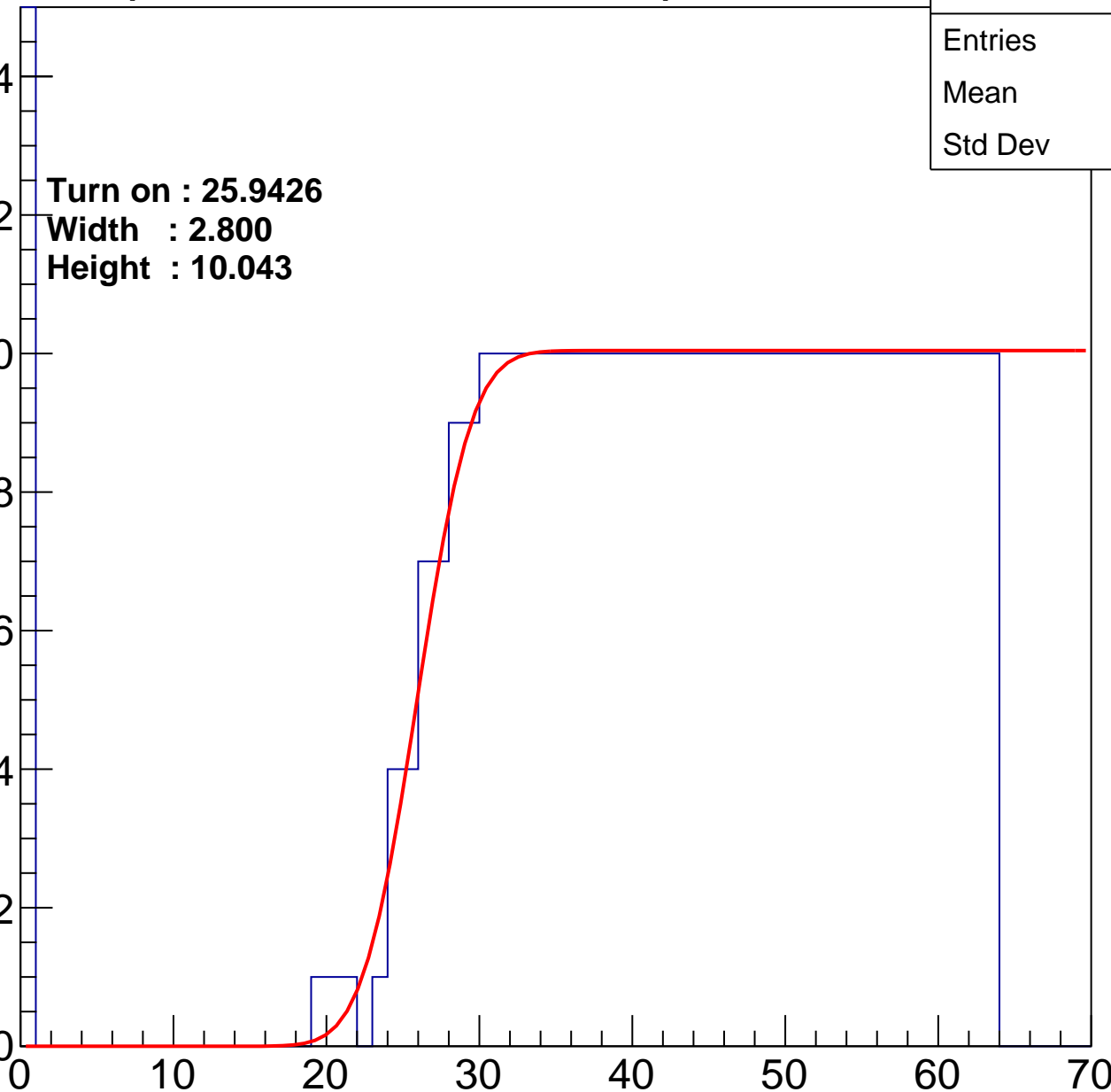
Width : 2.800

Height : 10.043

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U11-ch47

calib_packv5_041523_1651.root, FC#0, port C2

Entries	401
Mean	41.18
Std Dev	16.33

Turn on : 27.6527

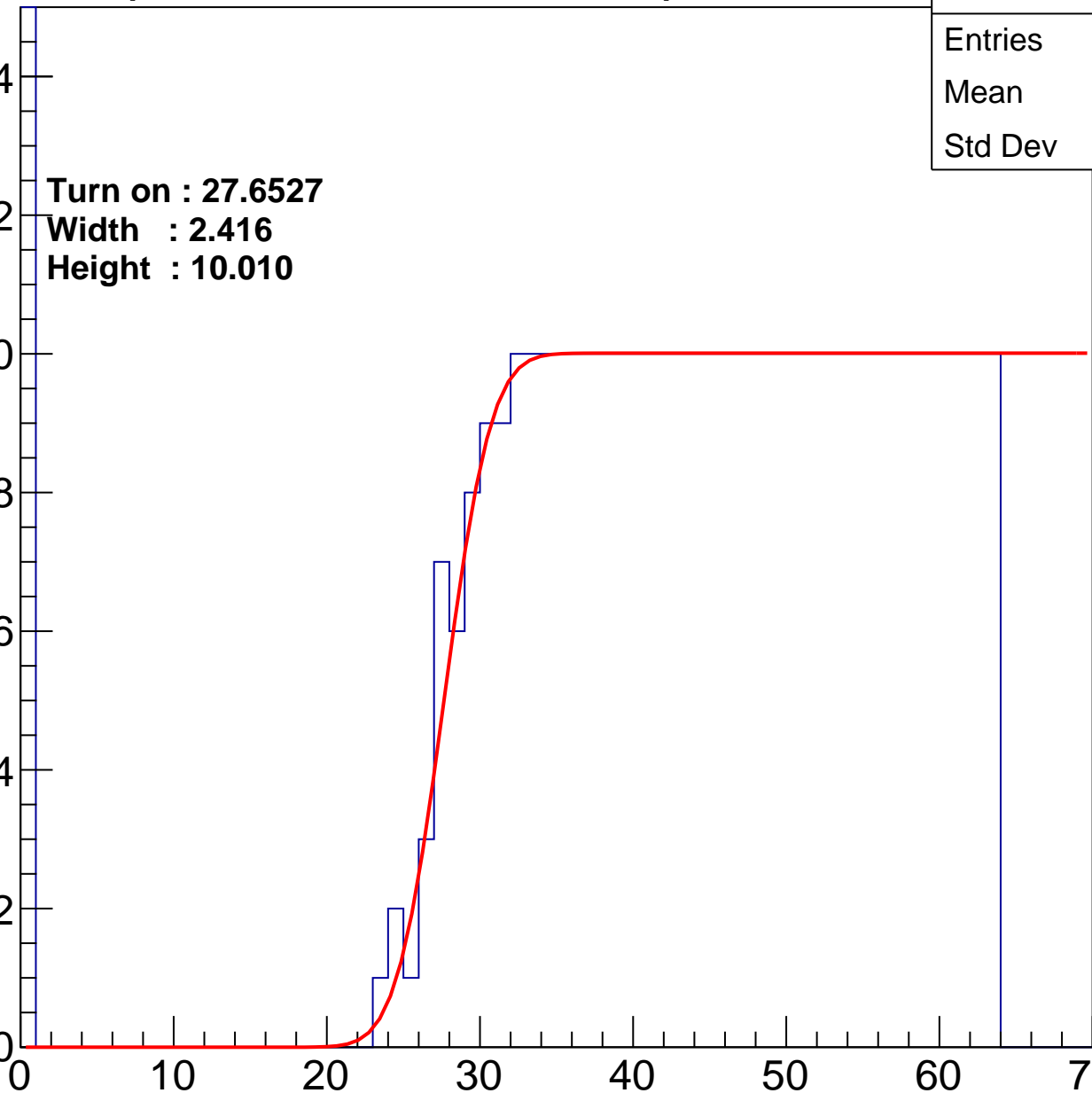
Width : 2.416

Height : 10.010

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U11-ch48

calib_packv5_041523_1651.root, FC#0, port C2

Entries	411
Mean	40.77
Std Dev	16.34

Turn on : 26.4164

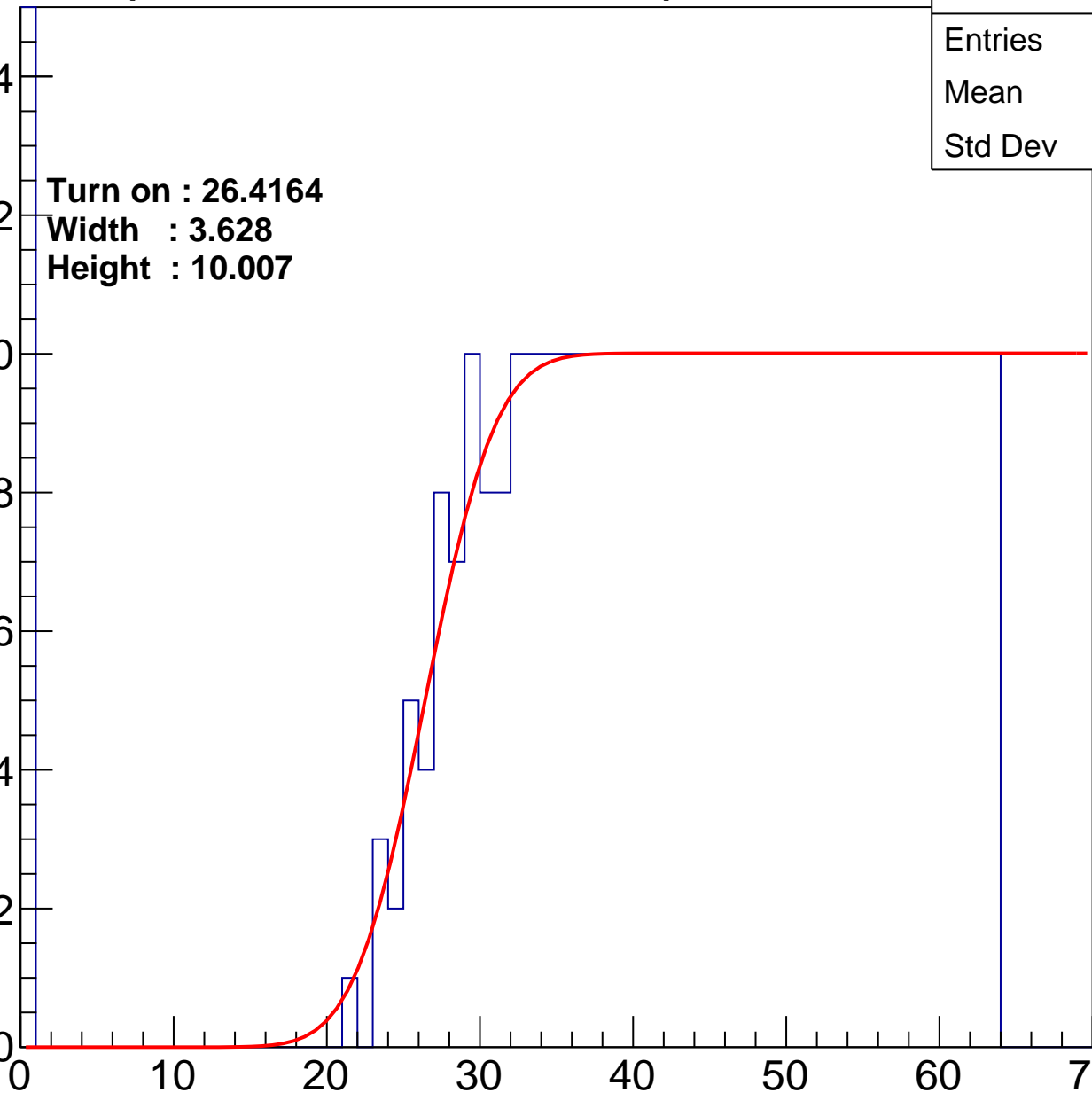
Width : 3.628

Height : 10.007

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U11-ch49

calib_packv5_041523_1651.root, FC#0, port C2

Entries	409
Mean	40.56
Std Dev	16.84

Turn on : 27.0029

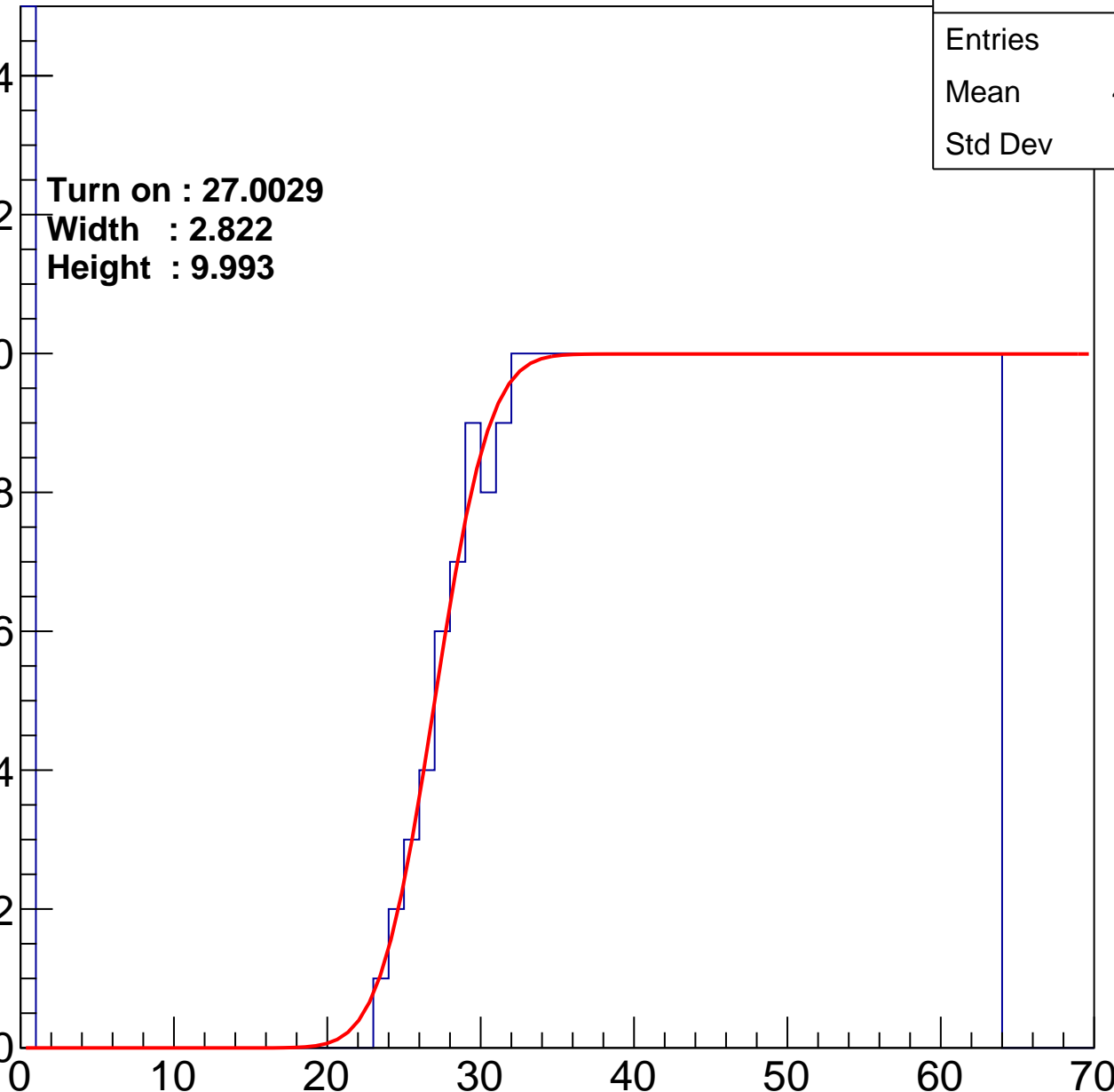
Width : 2.822

Height : 9.993

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U11-ch50

calib_packv5_041523_1651.root, FC#0, port C2

Entries	403
Mean	40.55
Std Dev	17.21

Turn on : 27.9644

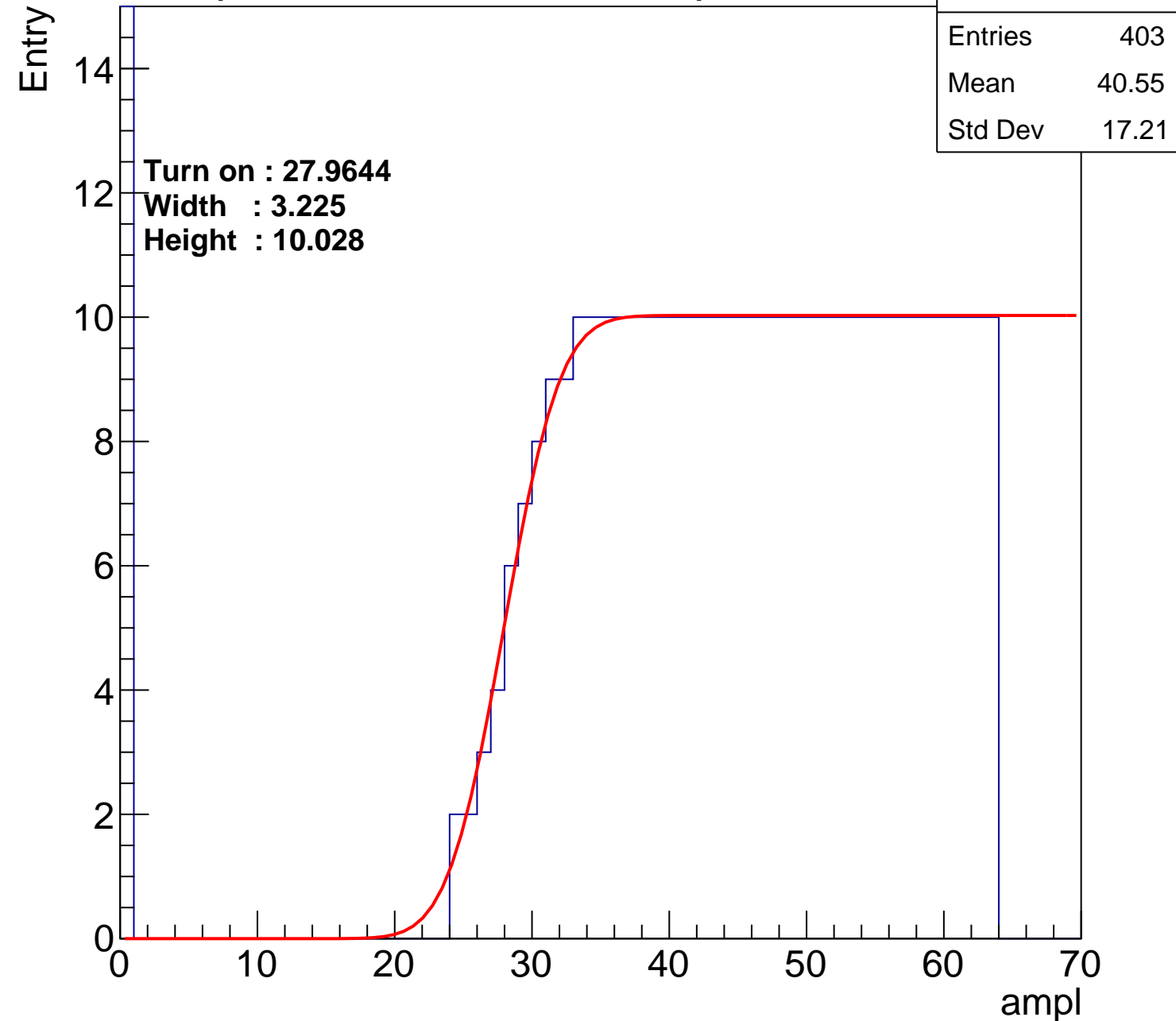
Width : 3.225

Height : 10.028

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U11-ch51

calib_packv5_041523_1651.root, FC#0, port C2

Entries	414
Mean	40.69
Std Dev	16.31

Turn on : 26.6460

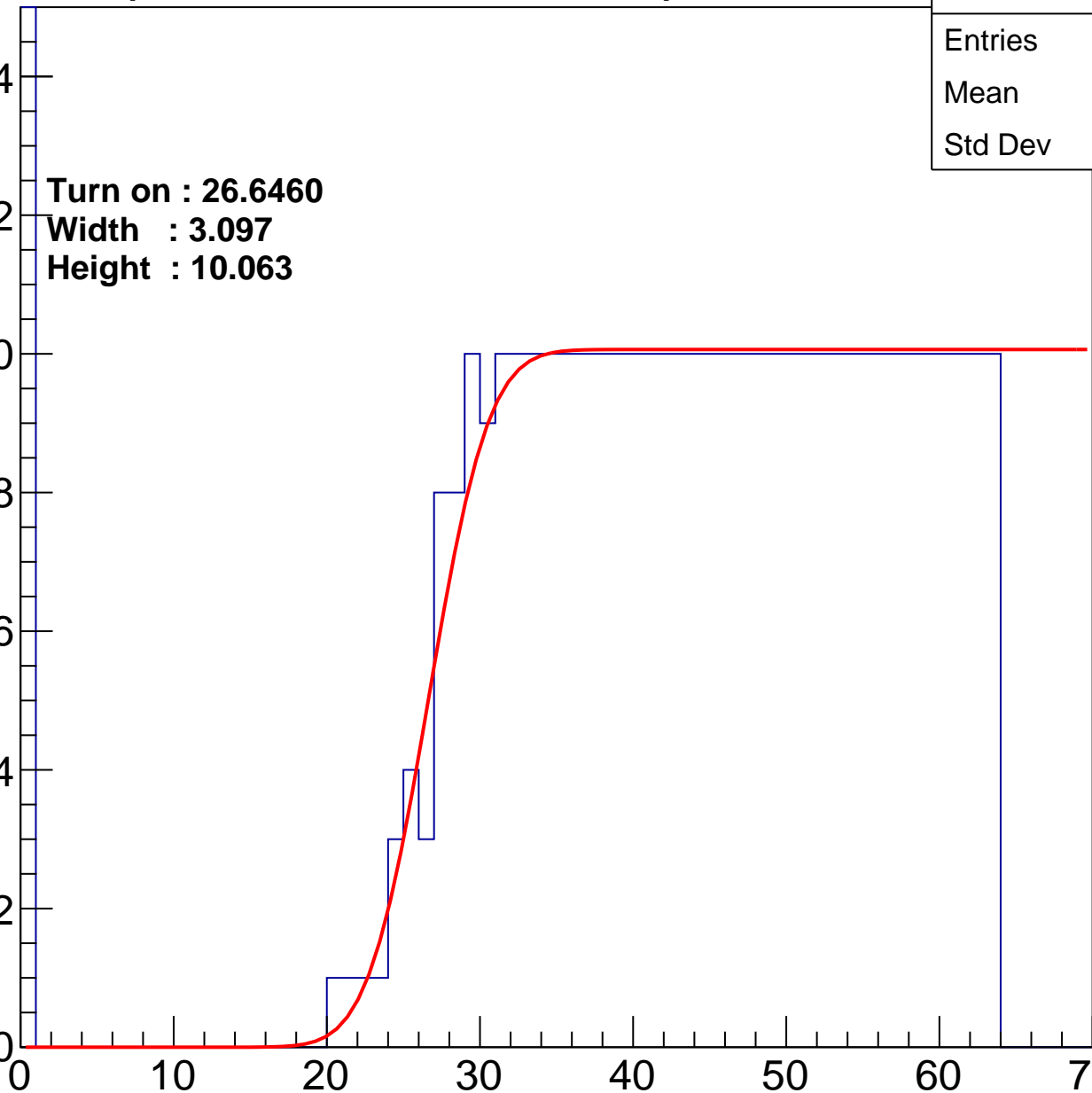
Width : 3.097

Height : 10.063

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U11-ch52

calib_packv5_041523_1651.root, FC#0, port C2

Entries	422
Mean	39.45
Std Dev	17.77

Turn on : 27.0990

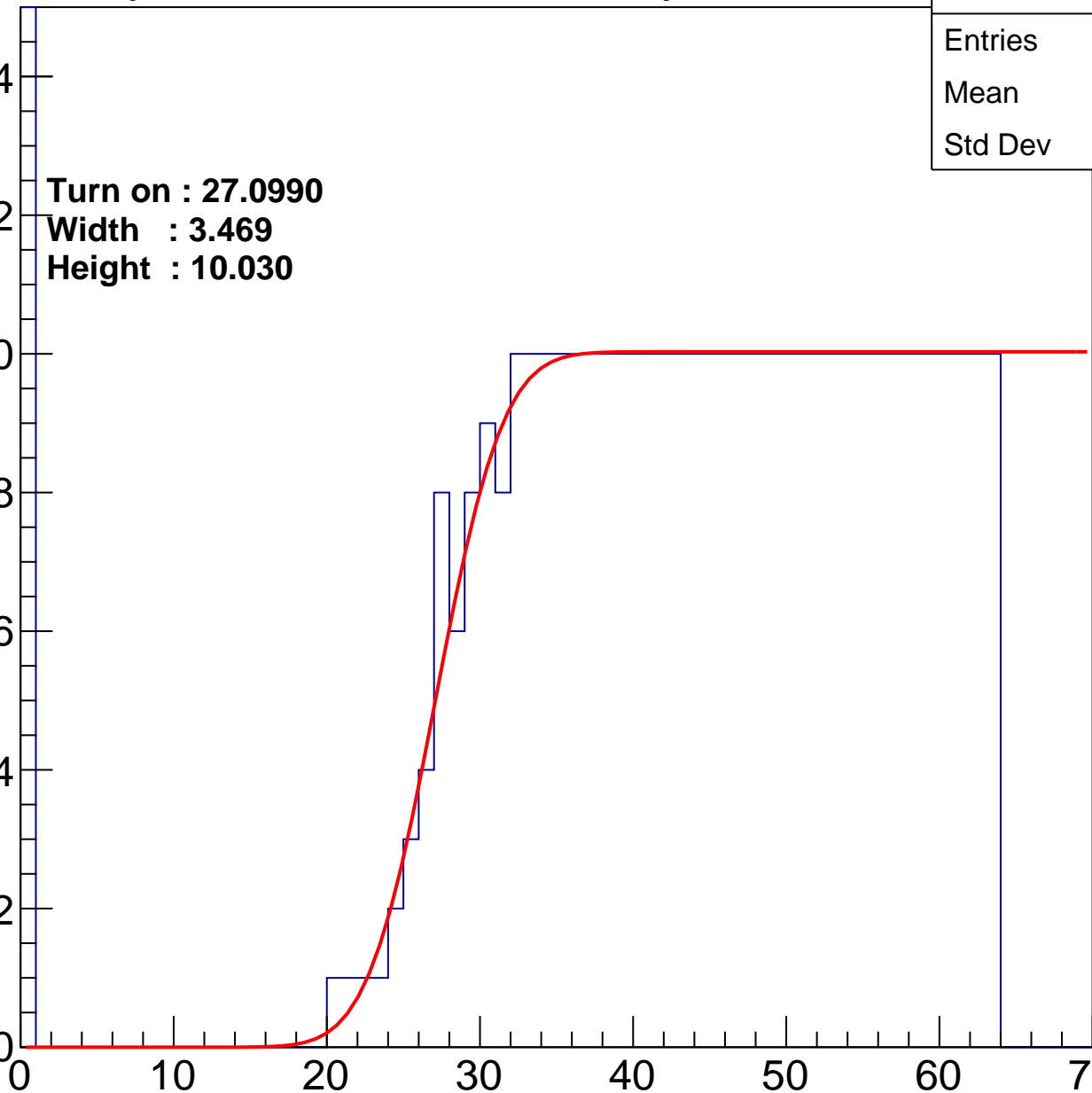
Width : 3.469

Height : 10.030

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U11-ch53

calib_packv5_041523_1651.root, FC#0, port C2

Entries	411
Mean	40.21
Std Dev	17.26

Turn on : 27.1571

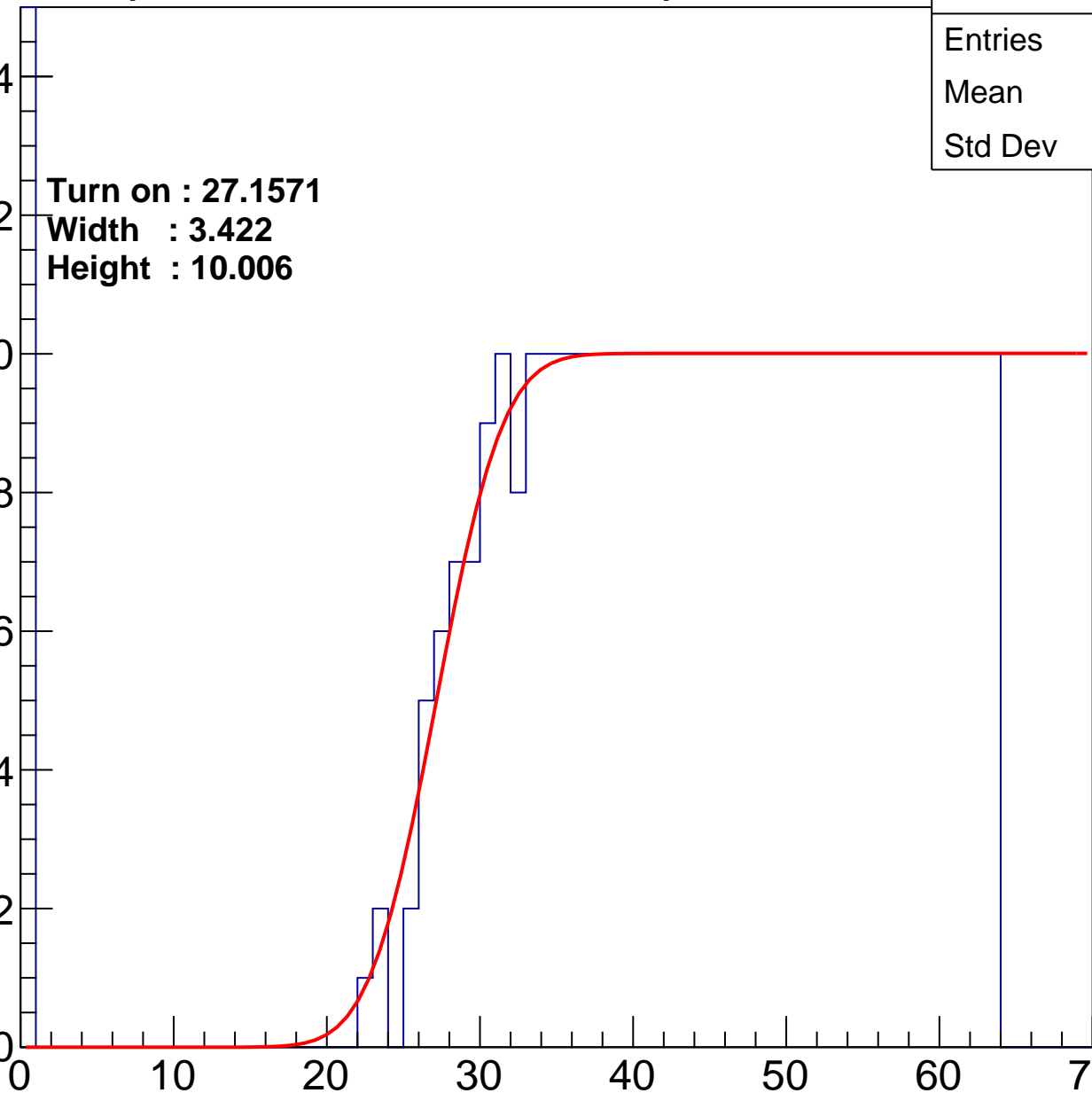
Width : 3.422

Height : 10.006

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U11-ch54

calib_packv5_041523_1651.root, FC#0, port C2

Entries	411
Mean	39.87
Std Dev	17.76

Turn on : 27.8104

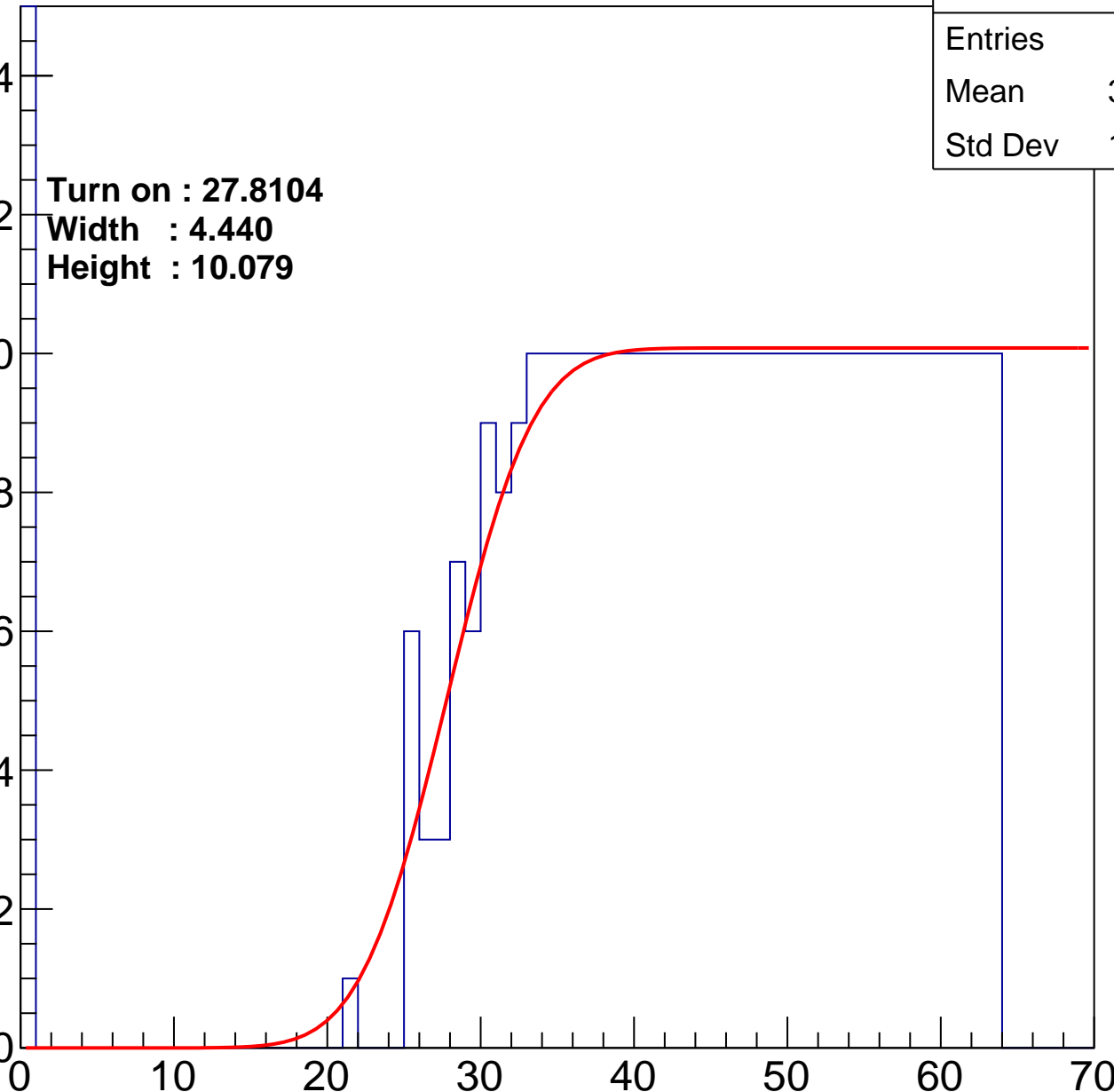
Width : 4.440

Height : 10.079

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U11-ch55

calib_packv5_041523_1651.root, FC#0, port C2

Entries	398
Mean	41.14
Std Dev	16.58

Turn on : 28.1215

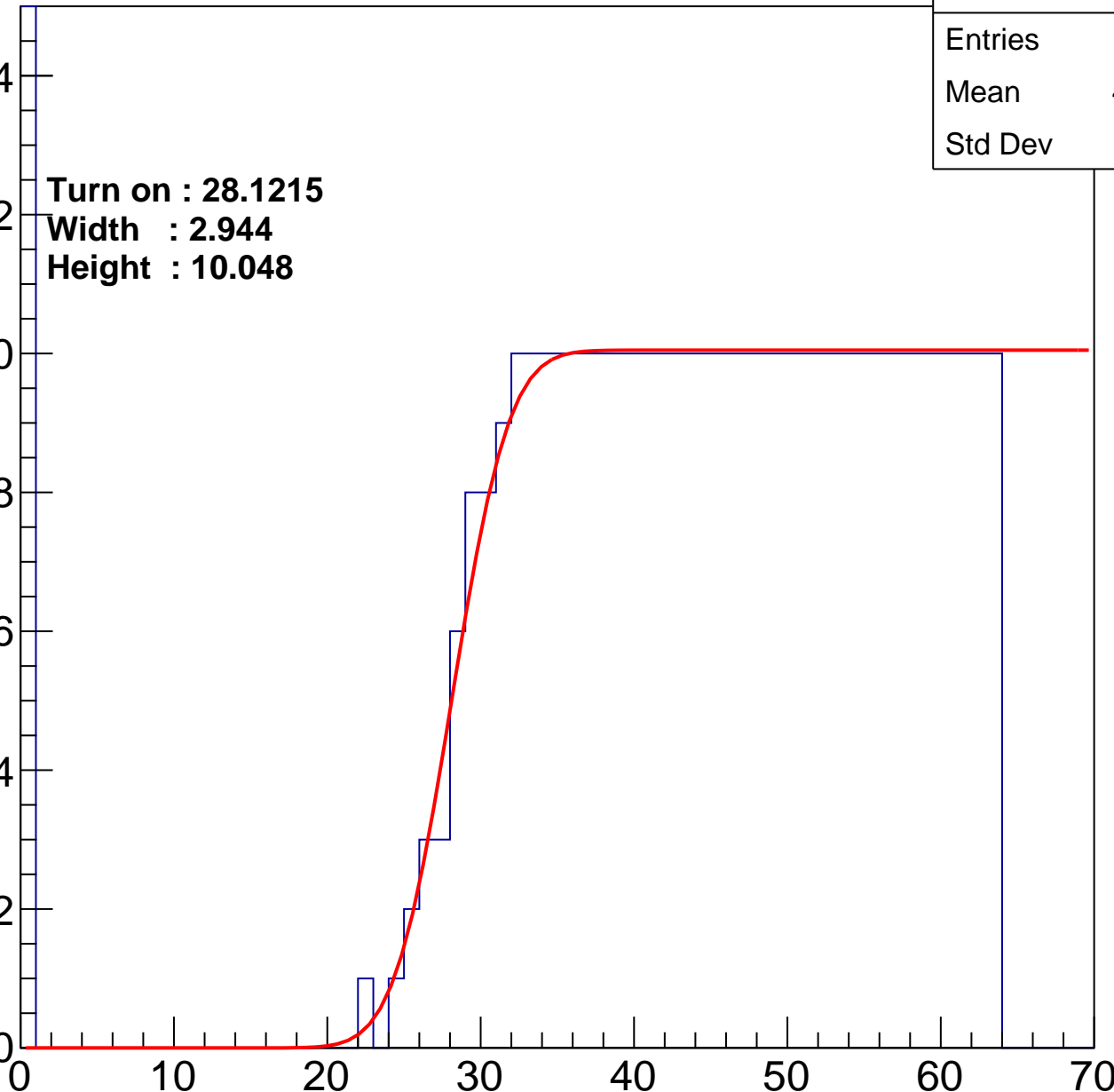
Width : 2.944

Height : 10.048

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U11-ch56

calib_packv5_041523_1651.root, FC#0, port C2

Entries	412
Mean	40.14
Std Dev	17.33

Turn on : 27.4081

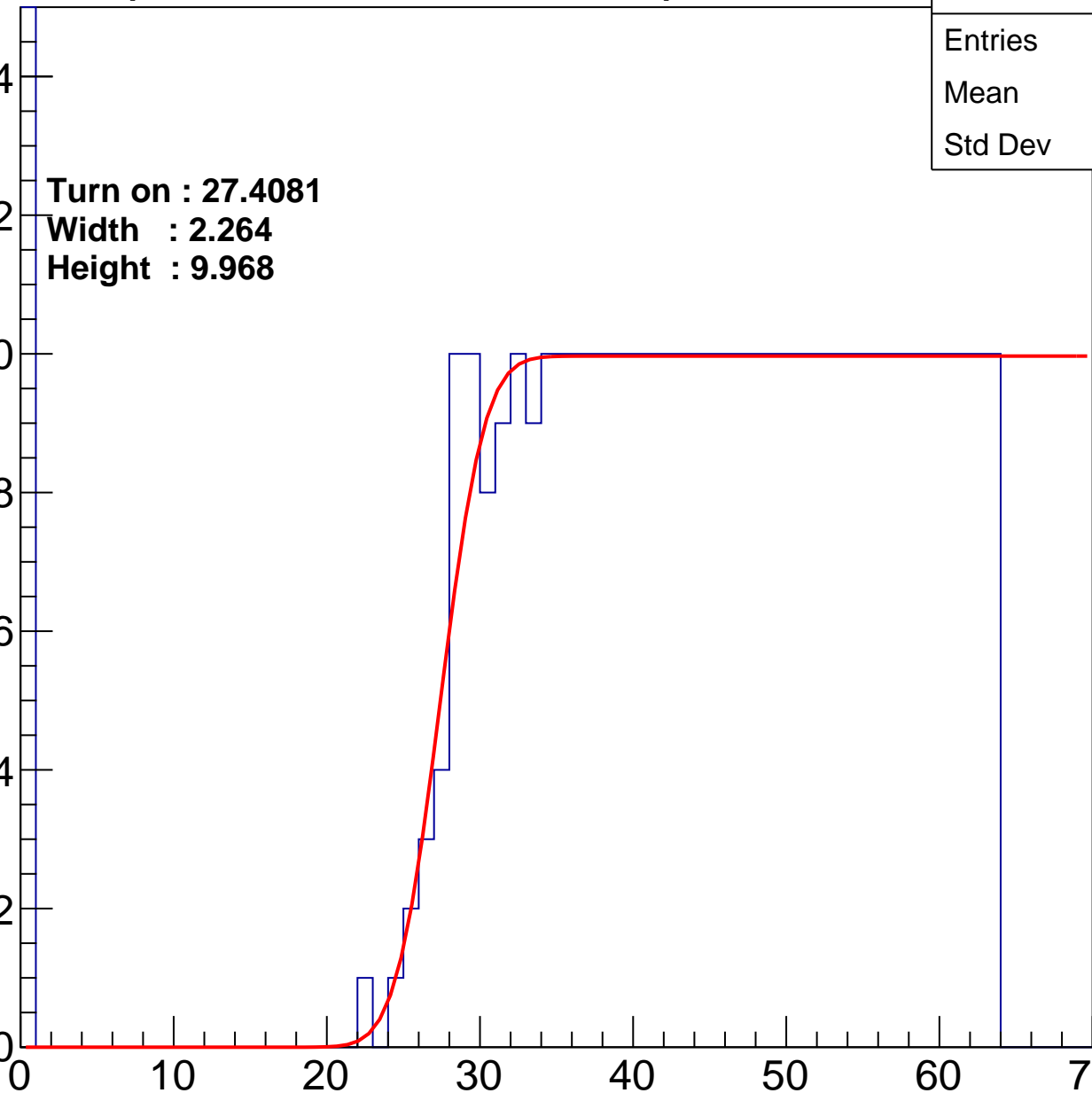
Width : 2.264

Height : 9.968

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U11-ch57

calib_packv5_041523_1651.root, FC#0, port C2

Entries	410
Mean	40.44
Std Dev	16.96

Turn on : 26.8222

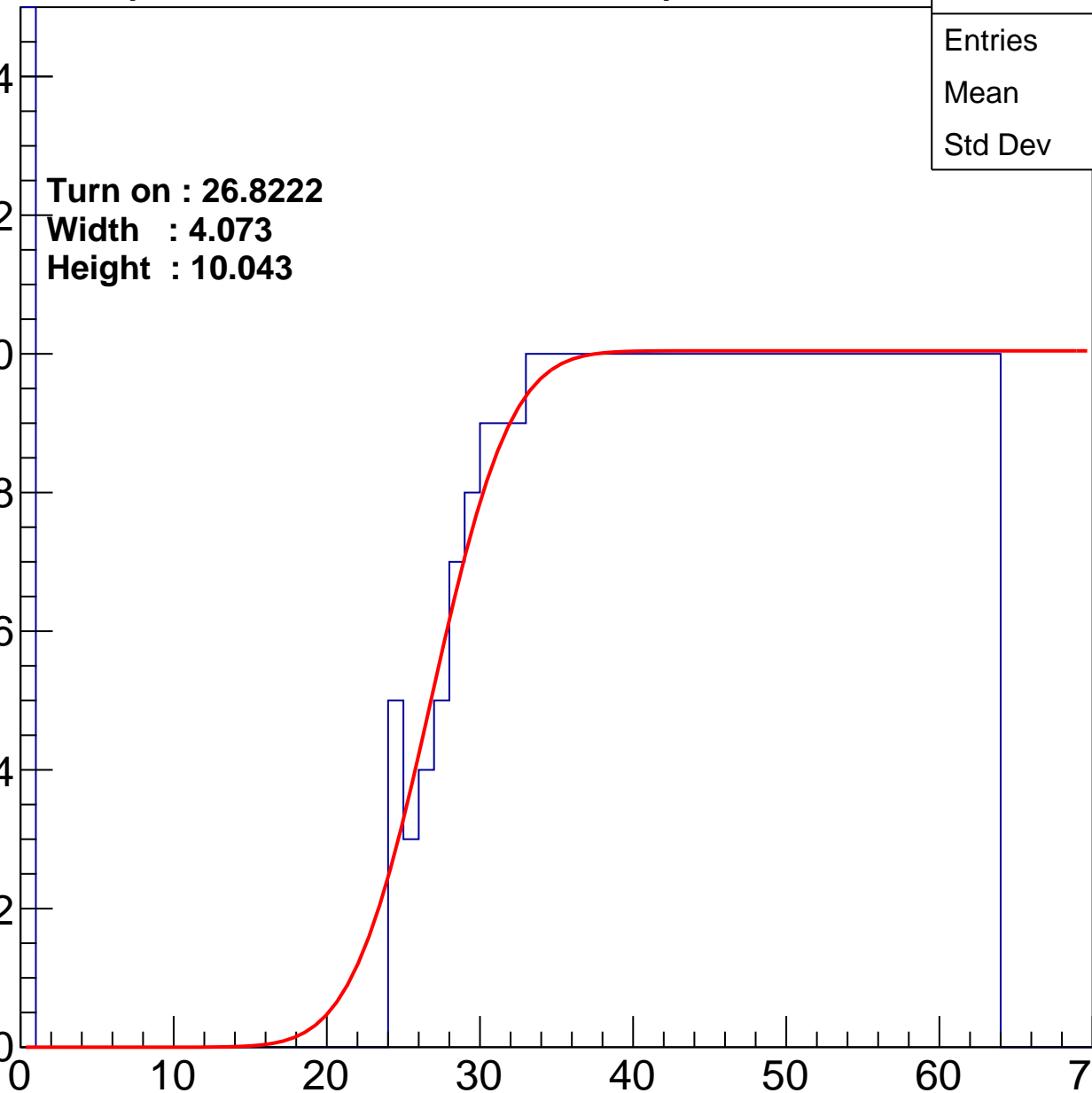
Width : 4.073

Height : 10.043

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U11-ch58

calib_packv5_041523_1651.root, FC#0, port C2

Entries	412
Mean	40.59
Std Dev	16.61

Turn on : 26.6814

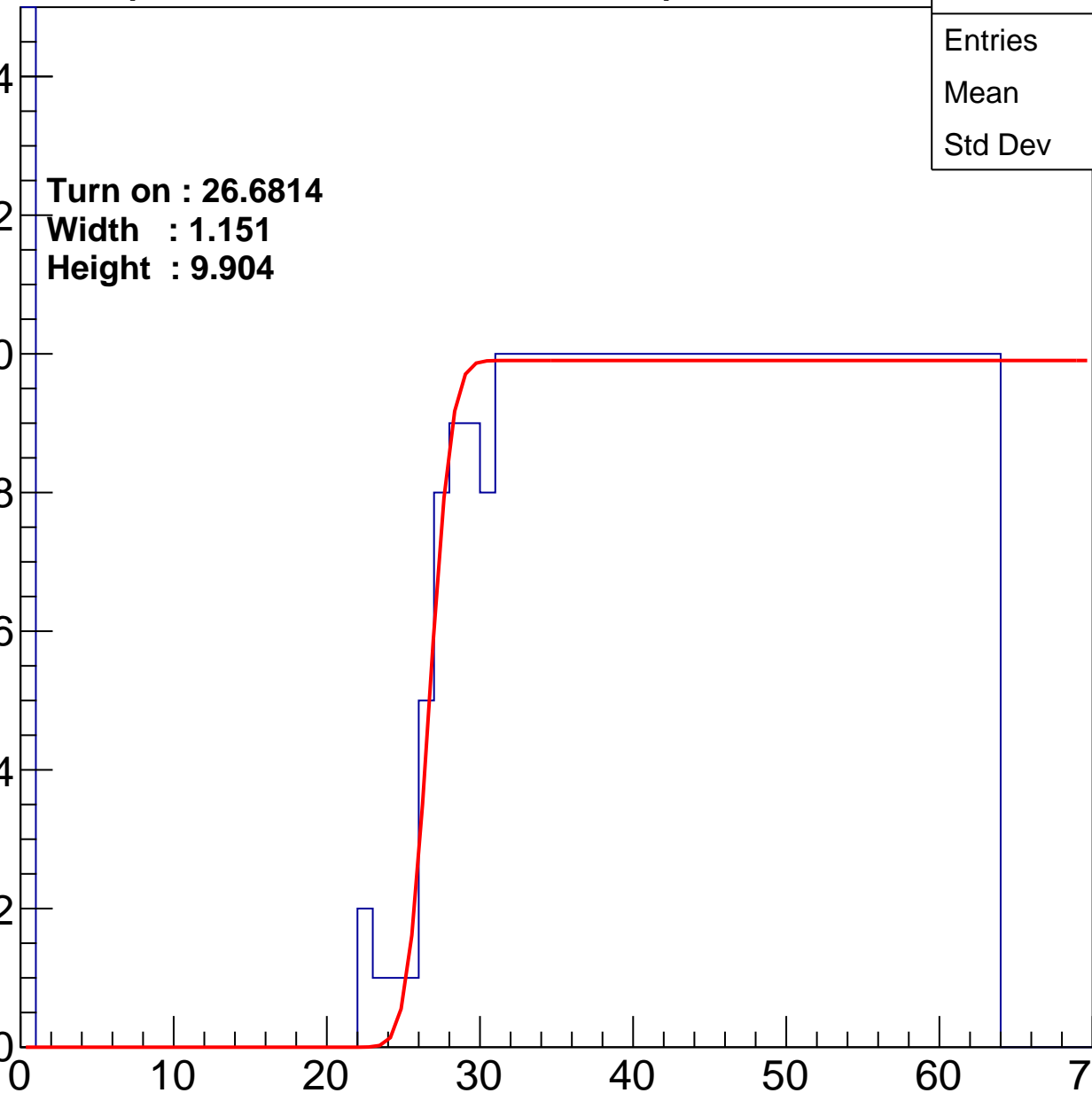
Width : 1.151

Height : 9.904

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U11-ch59

calib_packv5_041523_1651.root, FC#0, port C2

Entries	418
Mean	39.76
Std Dev	17.57

Turn on : 26.6518

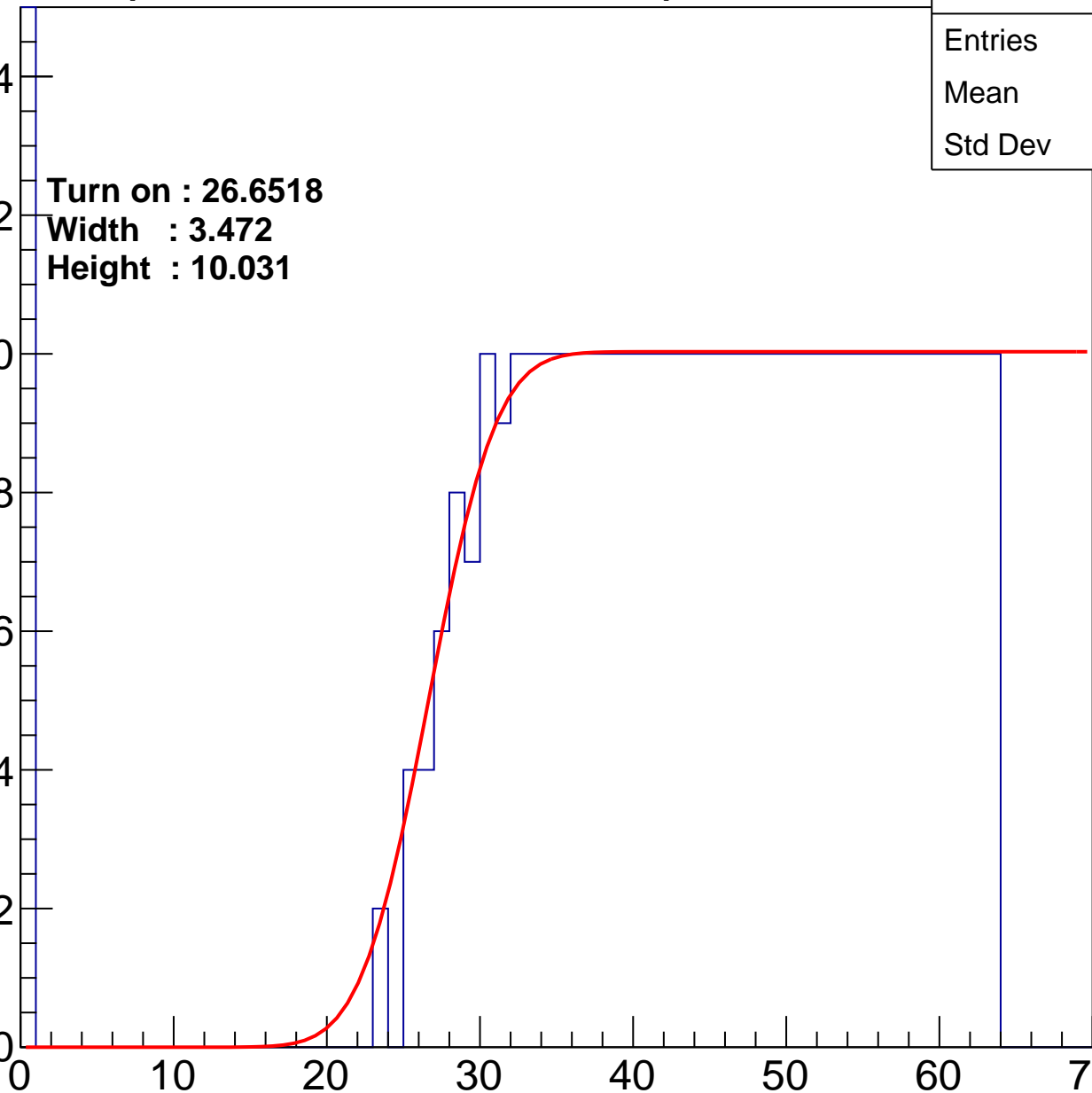
Width : 3.472

Height : 10.031

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U11-ch60

calib_packv5_041523_1651.root, FC#0, port C2

Entries	449
Mean	38.88
Std Dev	17.14

Turn on : 23.5421

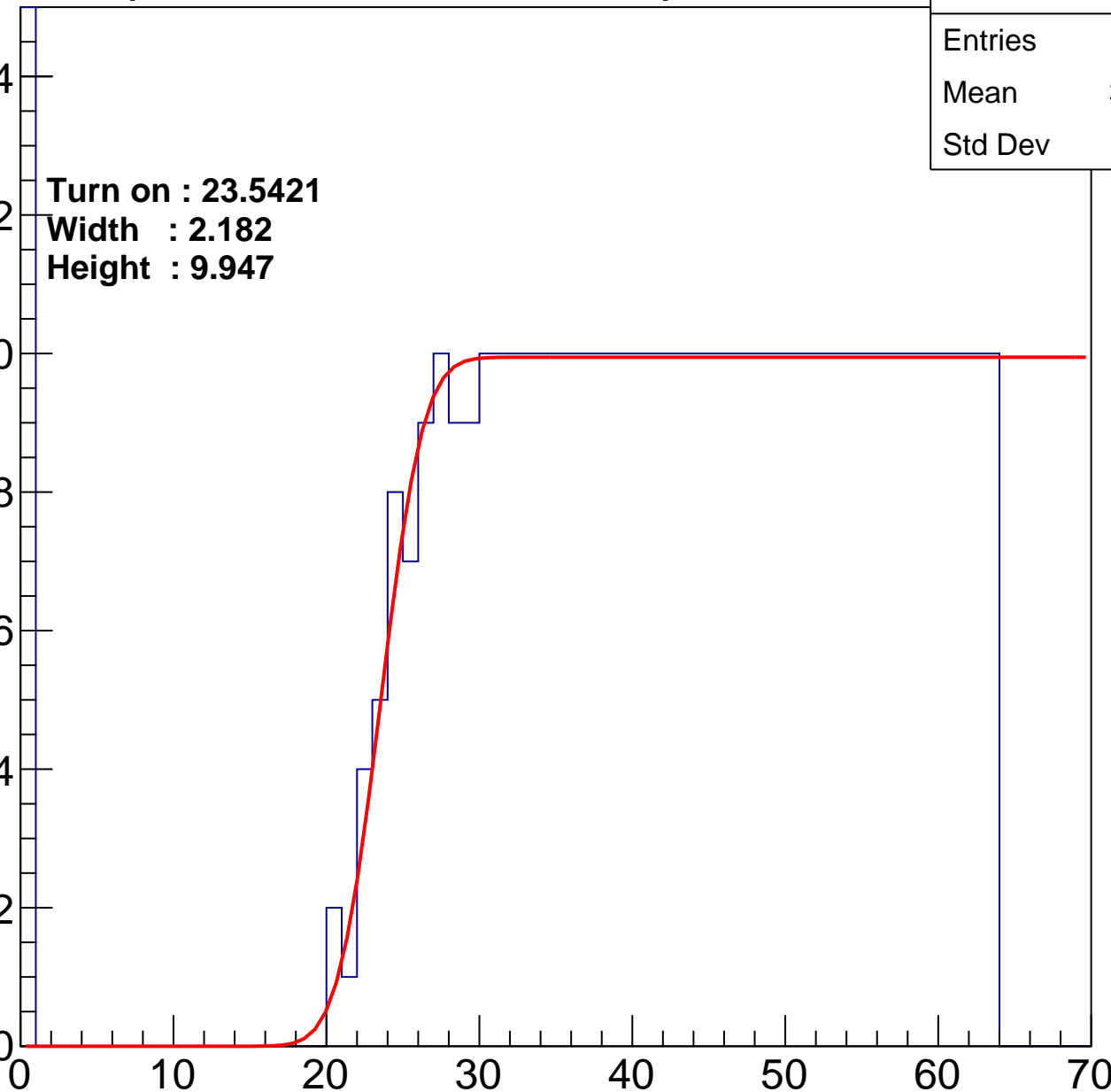
Width : 2.182

Height : 9.947

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U11-ch61

calib_packv5_041523_1651.root, FC#0, port C2

Entries	433
Mean	39.56
Std Dev	16.97

Turn on : 25.0795

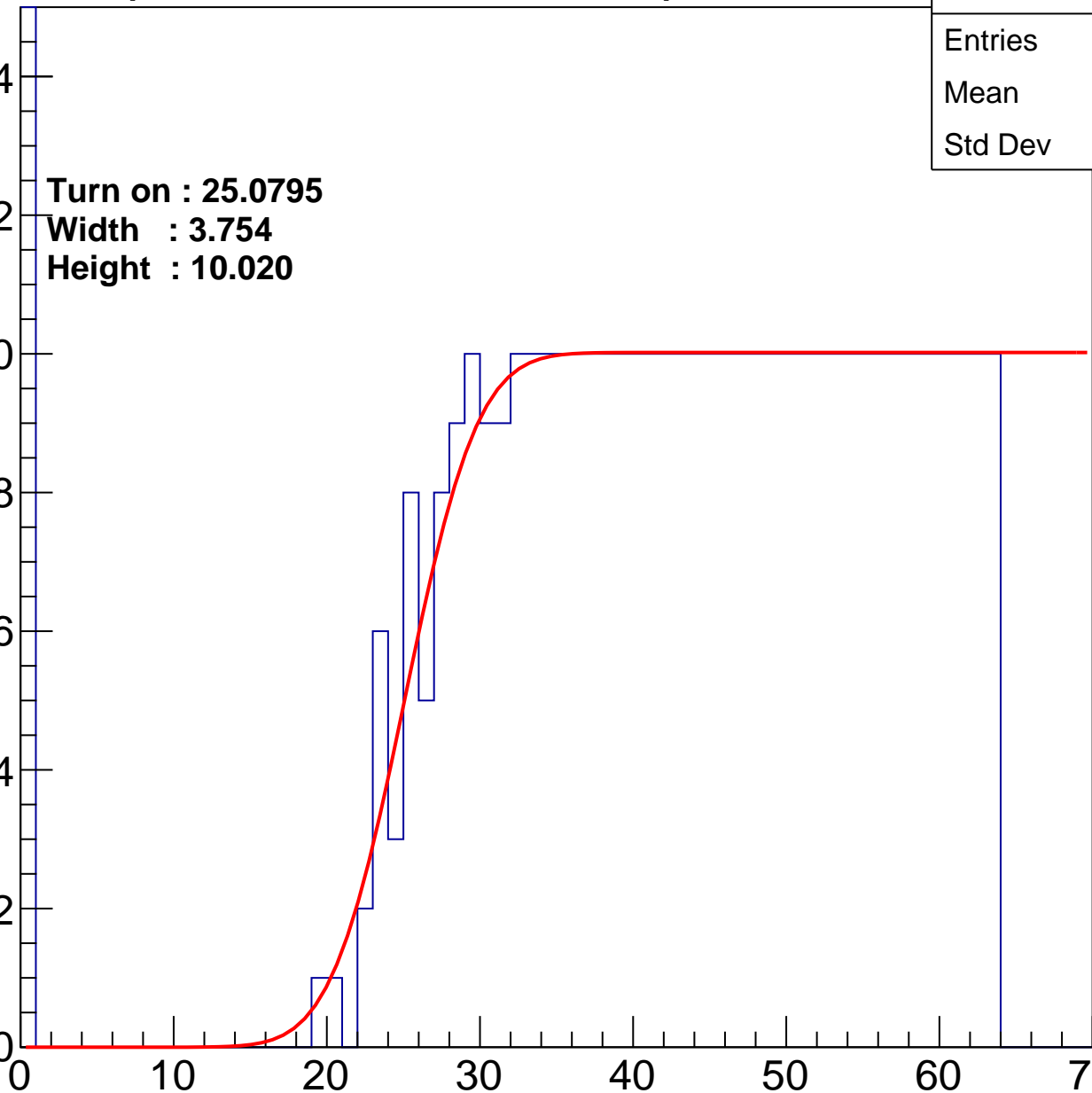
Width : 3.754

Height : 10.020

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U11-ch62

calib_packv5_041523_1651.root, FC#0, port C2

Entries	443
Mean	38.74
Std Dev	17.68

Turn on : 24.2286

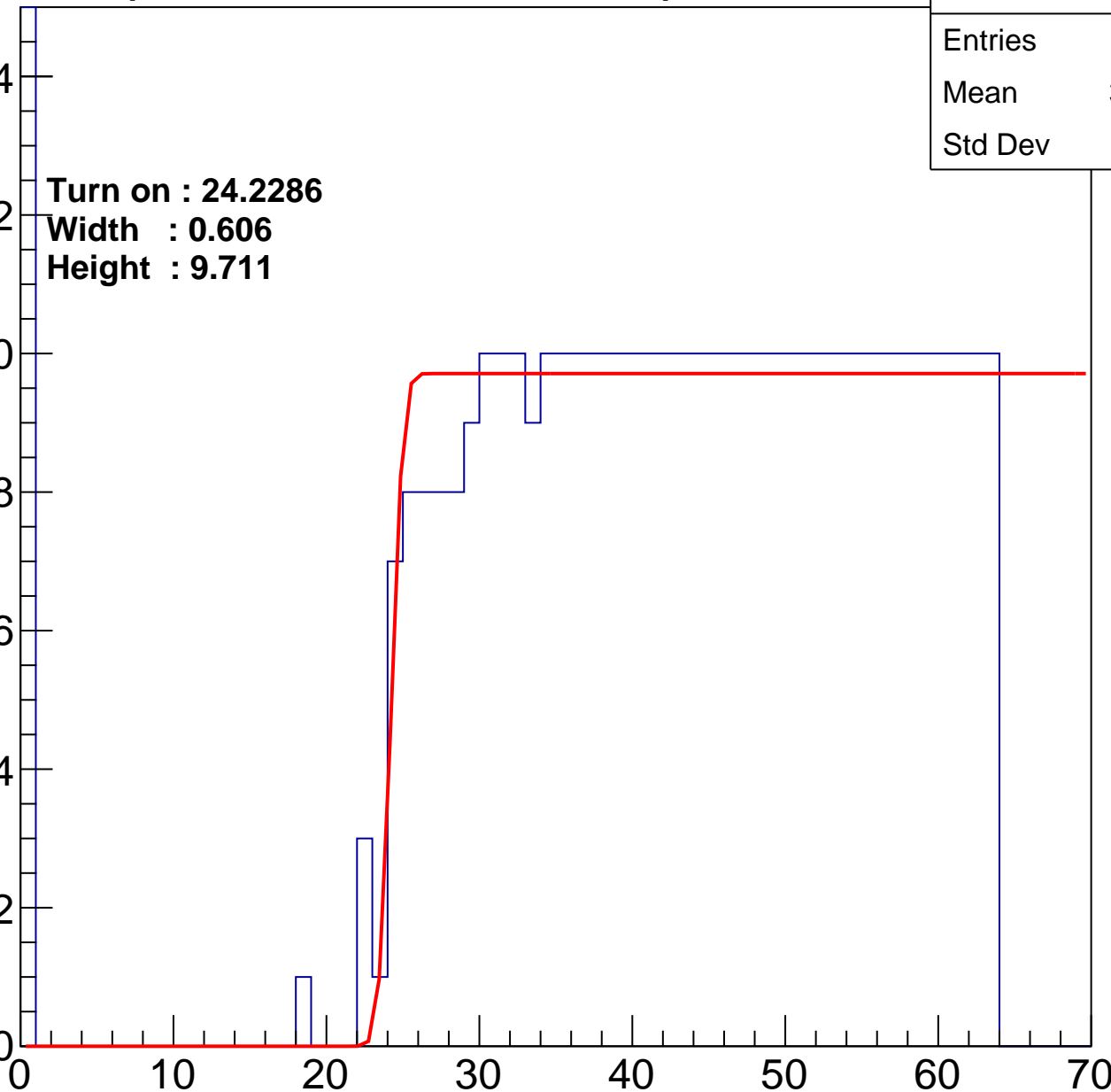
Width : 0.606

Height : 9.711

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U11-ch63

calib_packv5_041523_1651.root, FC#0, port C2

Entries	401
Mean	40.52
Std Dev	17.36

Turn on : 28.9069

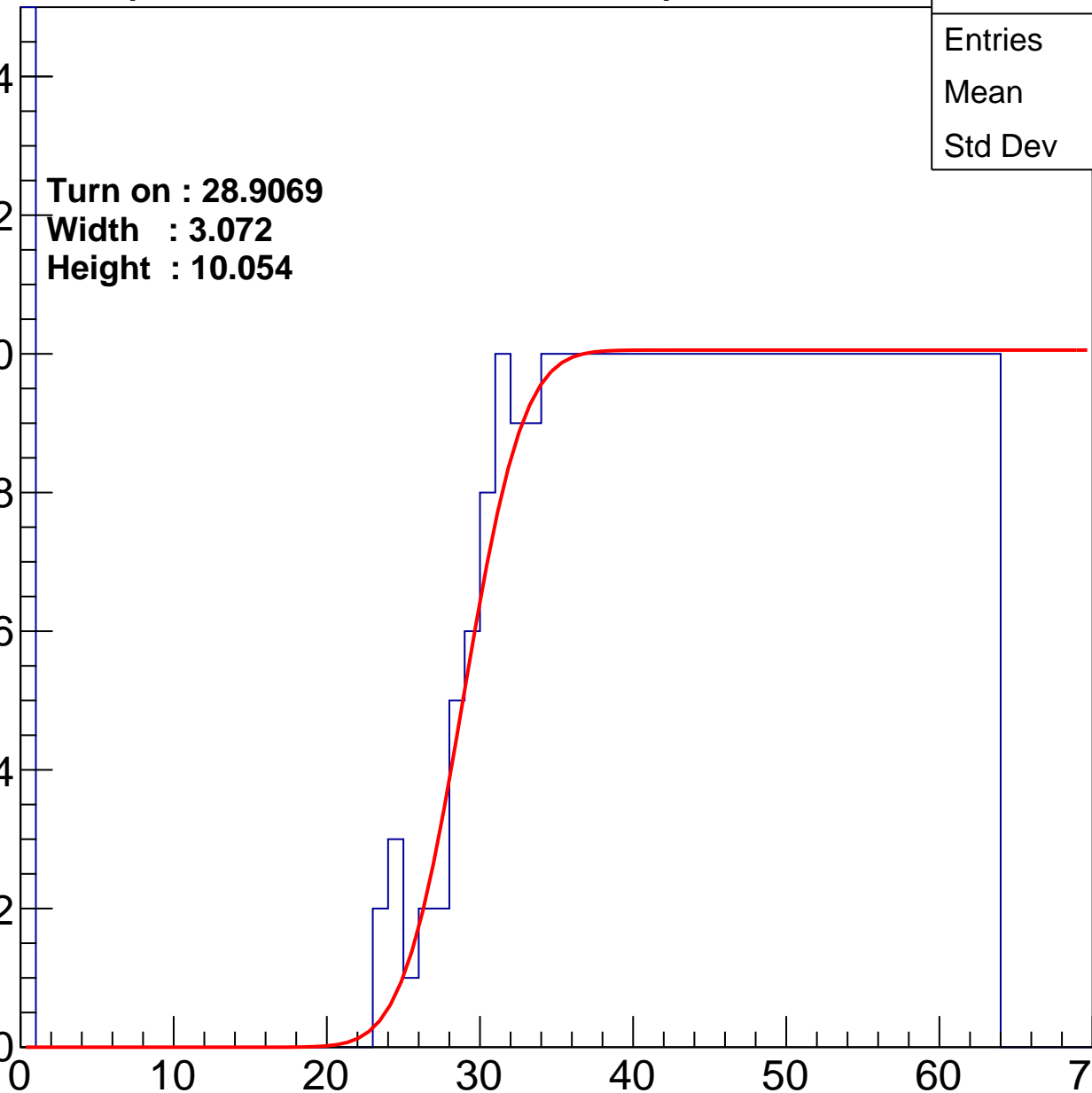
Width : 3.072

Height : 10.054

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U11-ch64

calib_packv5_041523_1651.root, FC#0, port C2

Entries	422
Mean	39.8
Std Dev	17.27

Turn on : 26.1439

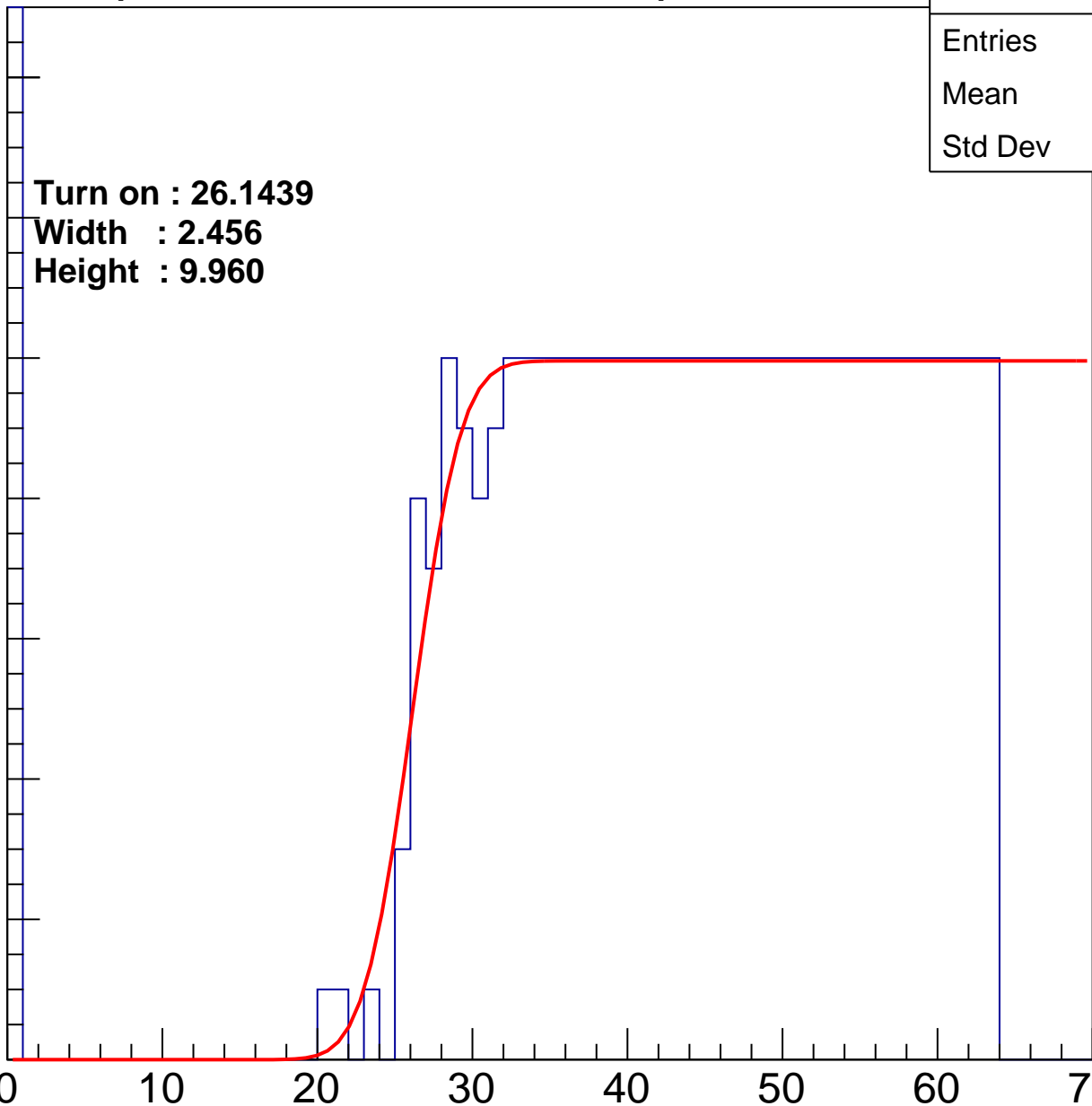
Width : 2.456

Height : 9.960

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U11-ch65

calib_packv5_041523_1651.root, FC#0, port C2

Entries	412
Mean	40.59
Std Dev	16.61

Turn on : 26.6993

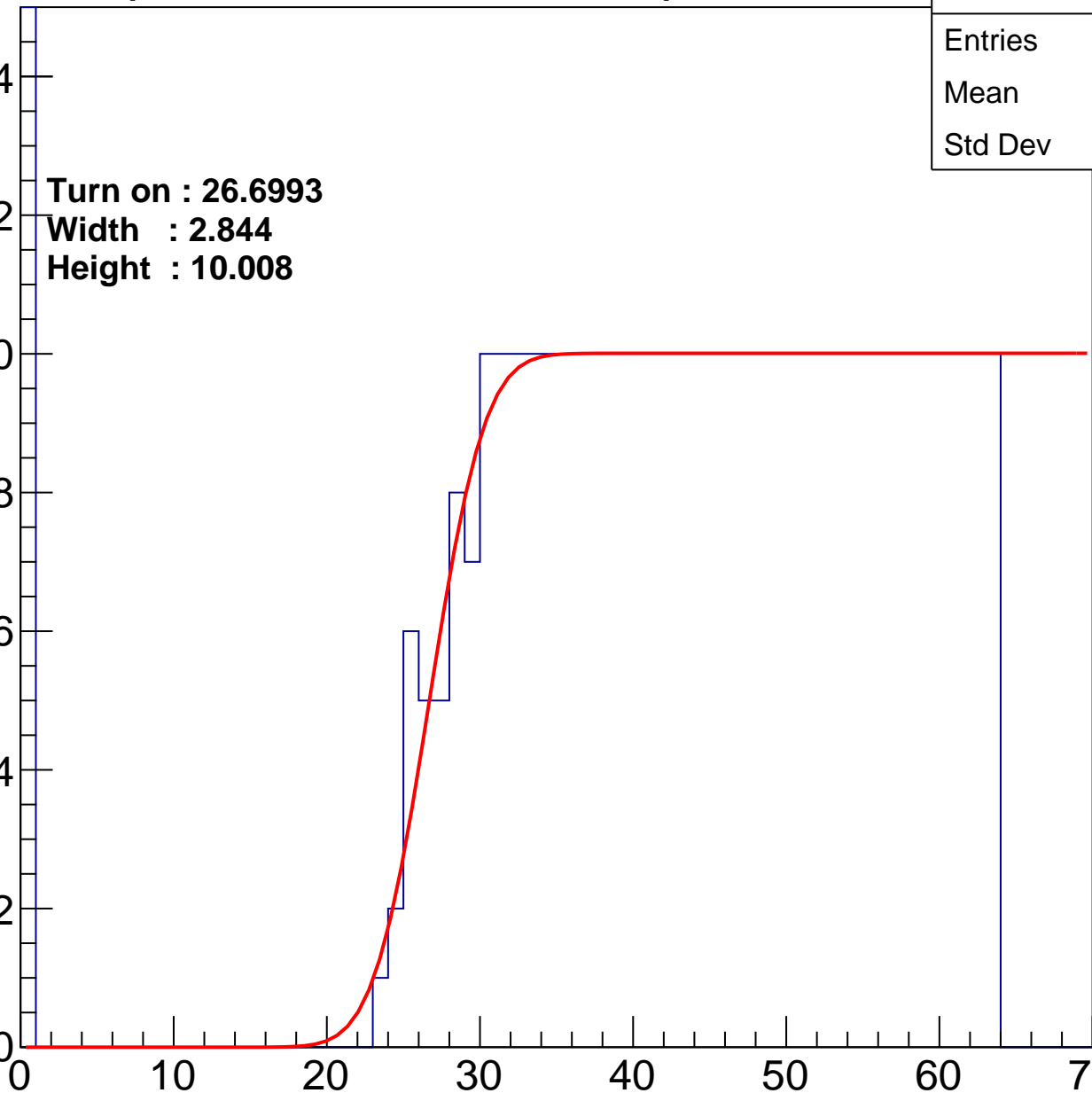
Width : 2.844

Height : 10.008

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U11-ch66

calib_packv5_041523_1651.root, FC#0, port C2

Entries	397
Mean	41.4
Std Dev	16.17

Turn on : 27.7063

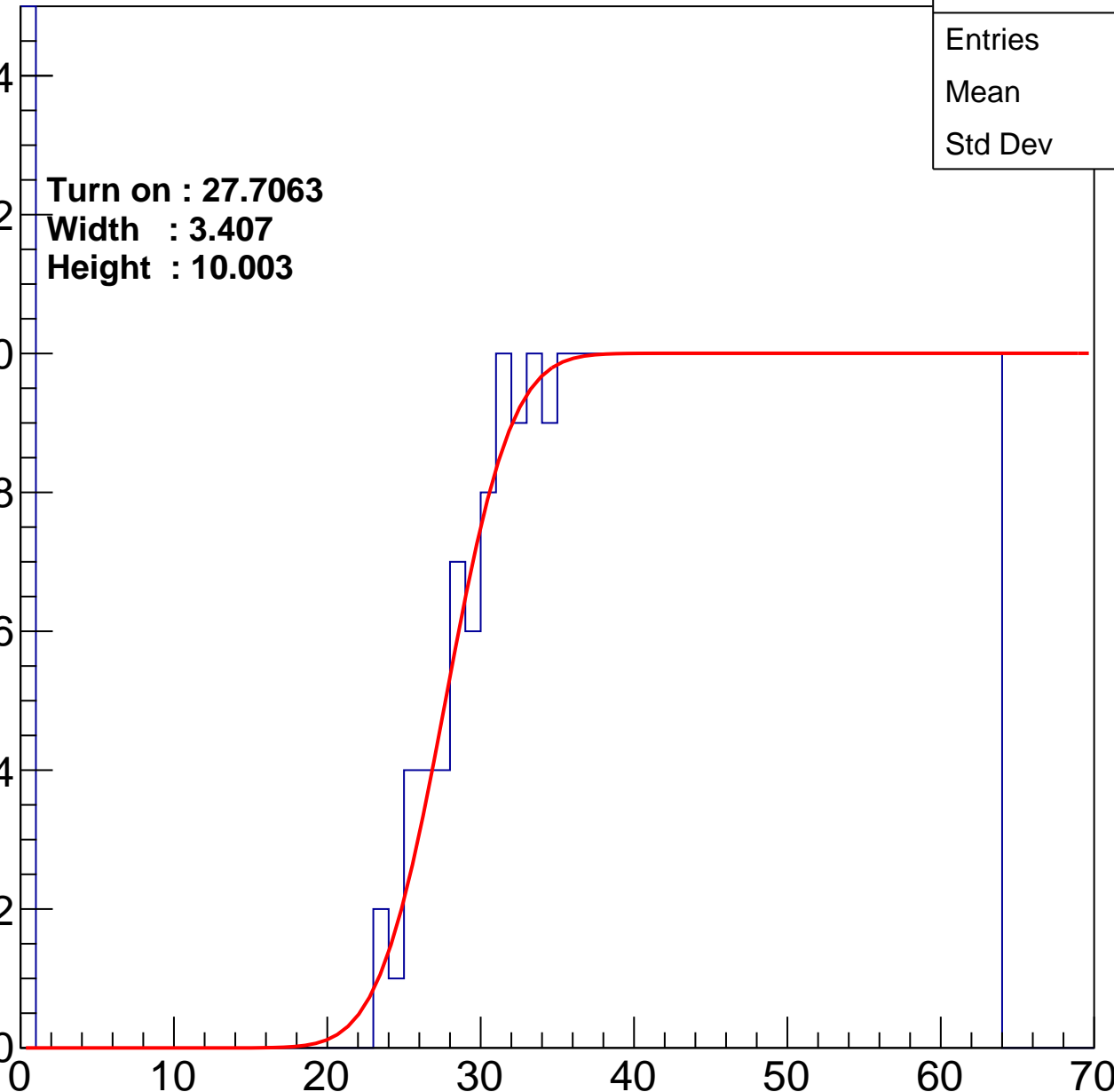
Width : 3.407

Height : 10.003

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U11-ch67

calib_packv5_041523_1651.root, FC#0, port C2

Entries	415
Mean	39.79
Std Dev	17.69

Turn on : 27.4830

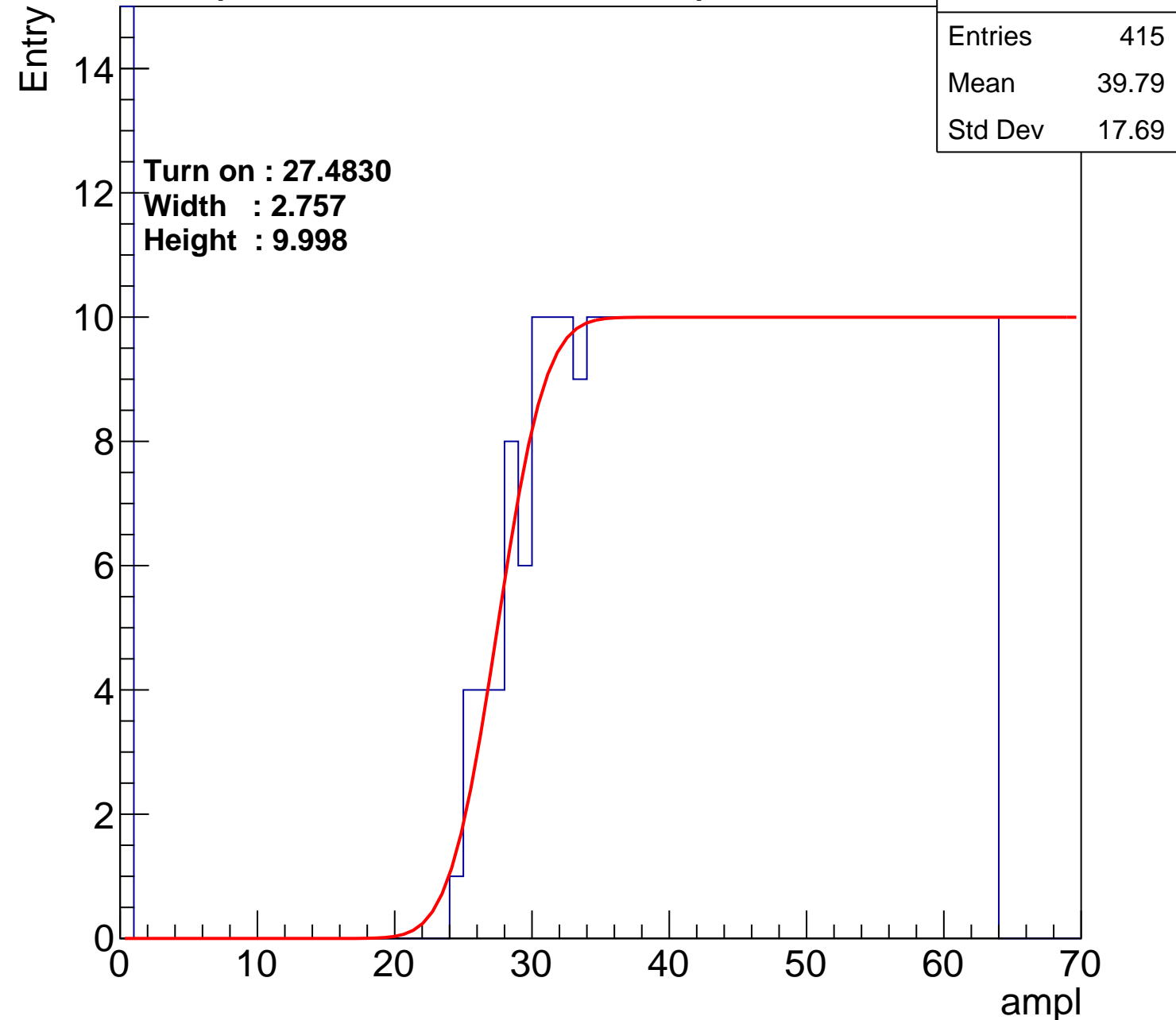
Width : 2.757

Height : 9.998

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U11-ch68

calib_packv5_041523_1651.root, FC#0, port C2

Entries	411
Mean	40.82
Std Dev	16.3

Turn on : 26.1917

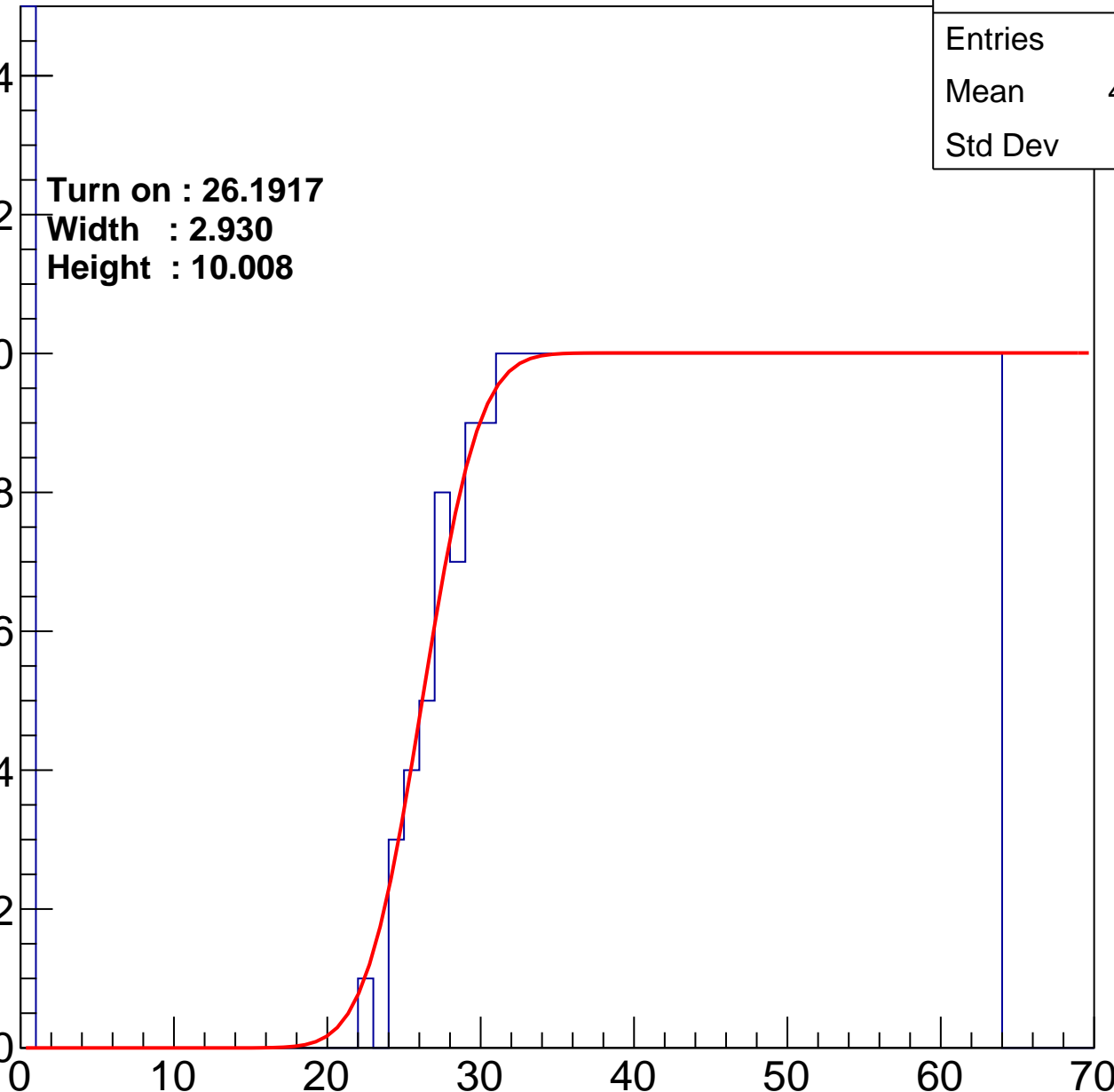
Width : 2.930

Height : 10.008

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U11-ch69

calib_packv5_041523_1651.root, FC#0, port C2

Entries	412
Mean	40.17
Std Dev	17.26

Turn on : 27.3496

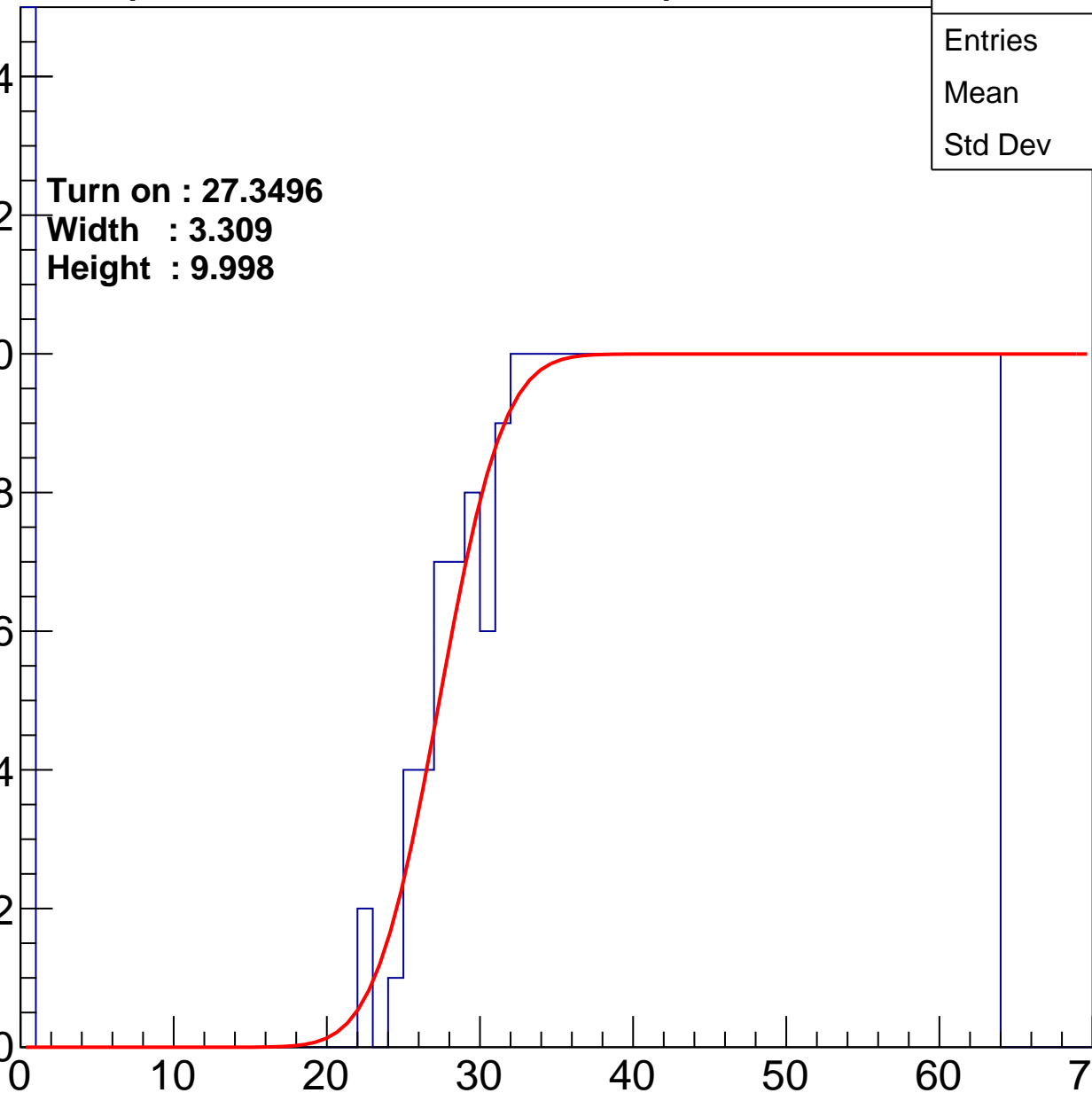
Width : 3.309

Height : 9.998

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U11-ch70

calib_packv5_041523_1651.root, FC#0, port C2

Entries	438
Mean	38.67
Std Dev	18.05

Turn on : 25.6285

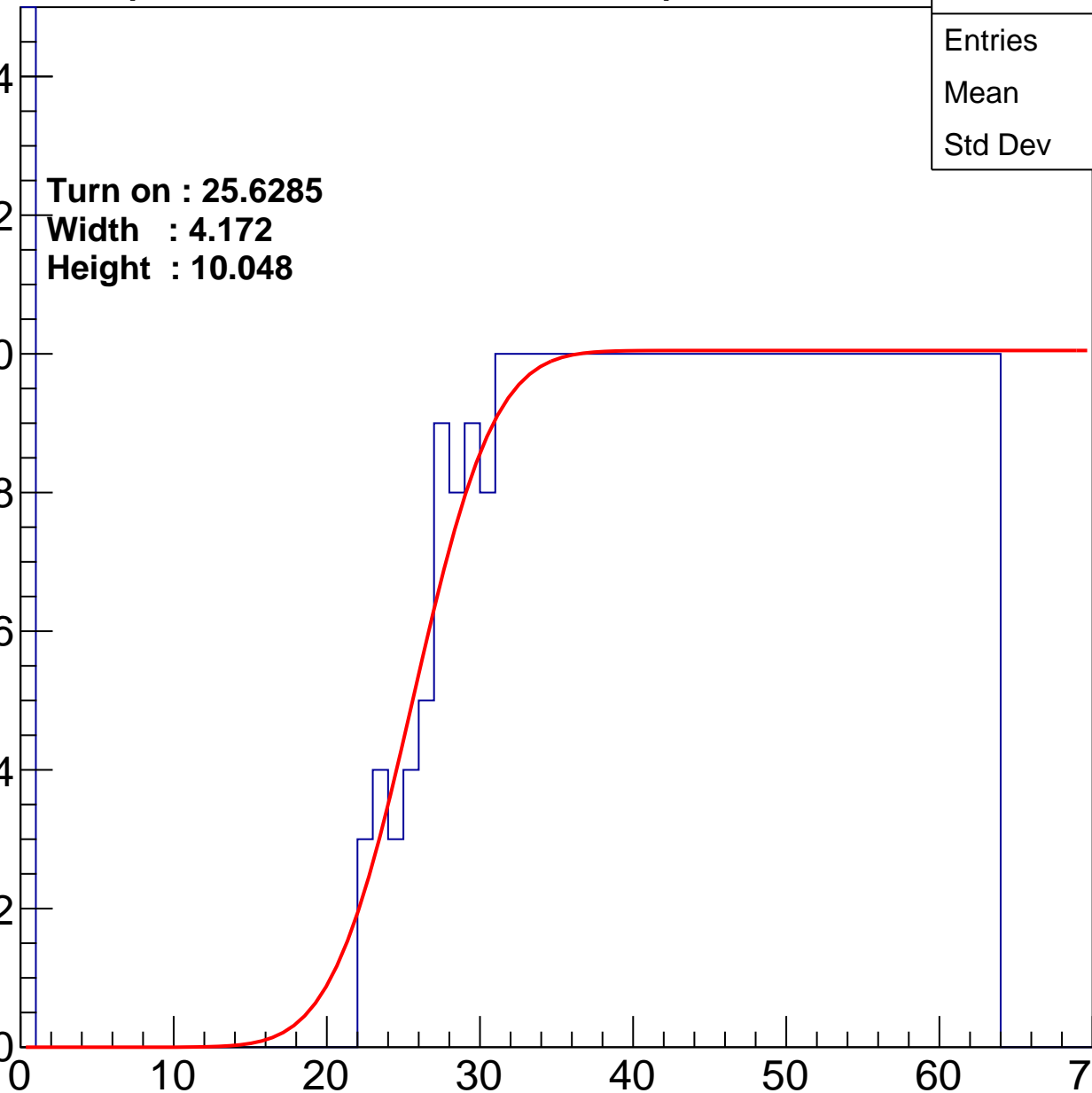
Width : 4.172

Height : 10.048

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U11-ch71

calib_packv5_041523_1651.root, FC#0, port C2

Entries	403
Mean	40.65
Std Dev	17.08

Turn on : 27.9419

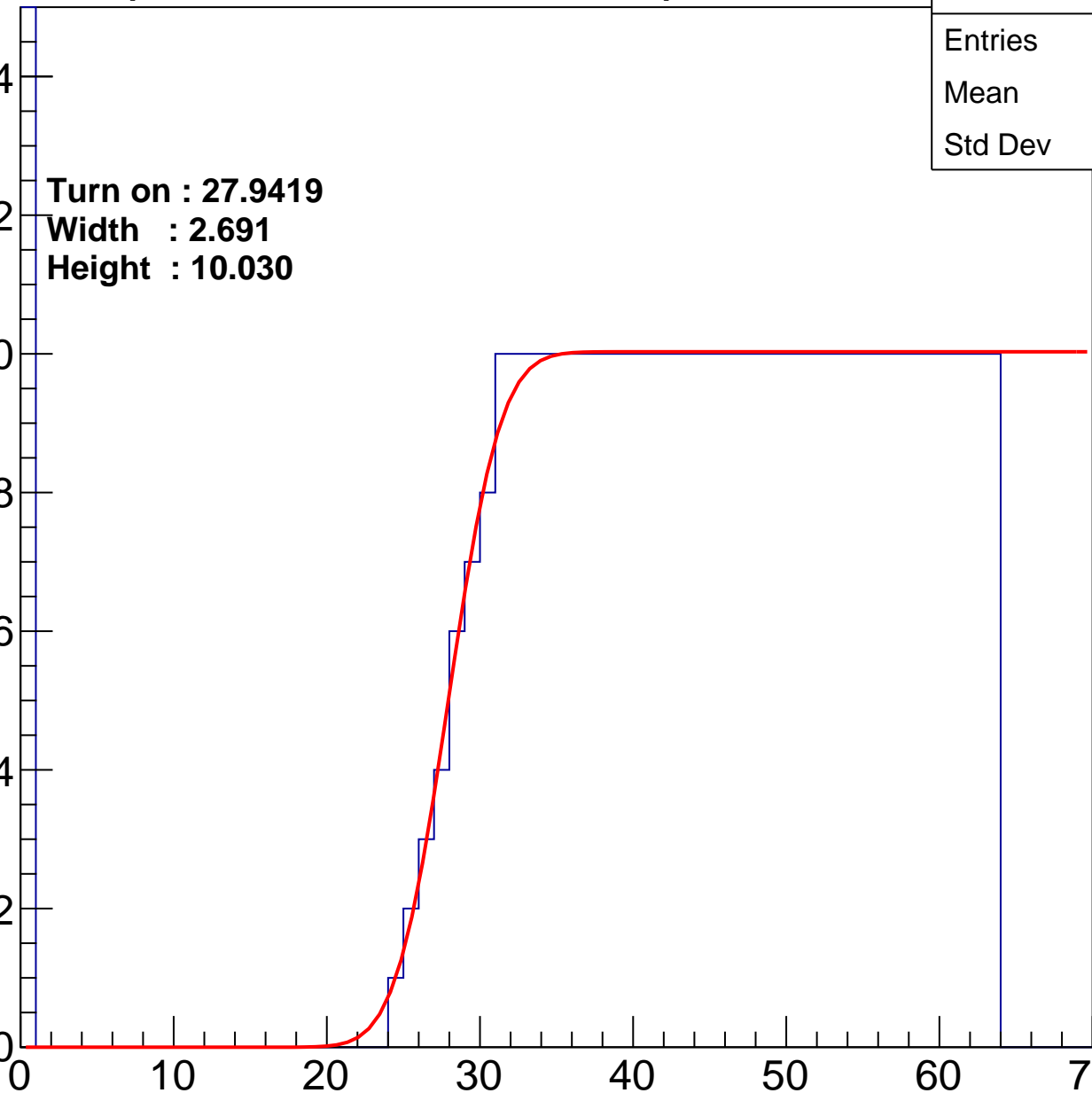
Width : 2.691

Height : 10.030

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U11-ch72

calib_packv5_041523_1651.root, FC#0, port C2

Entries	435
Mean	39.62
Std Dev	16.77

Turn on : 24.4902

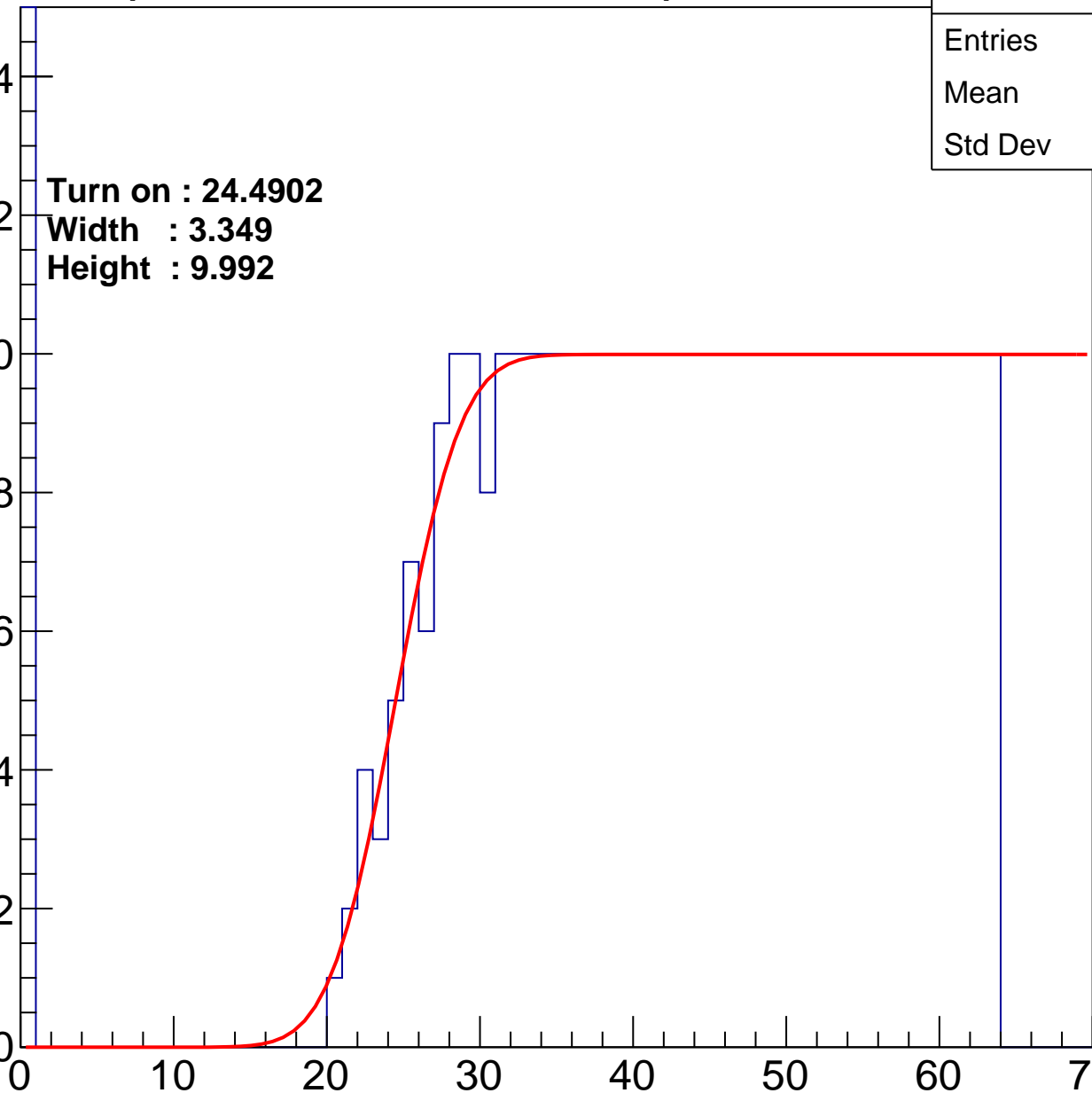
Width : 3.349

Height : 9.992

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U11-ch73

calib_packv5_041523_1651.root, FC#0, port C2

Entries	423
Mean	40.09
Std Dev	16.77

Turn on : 25.9318

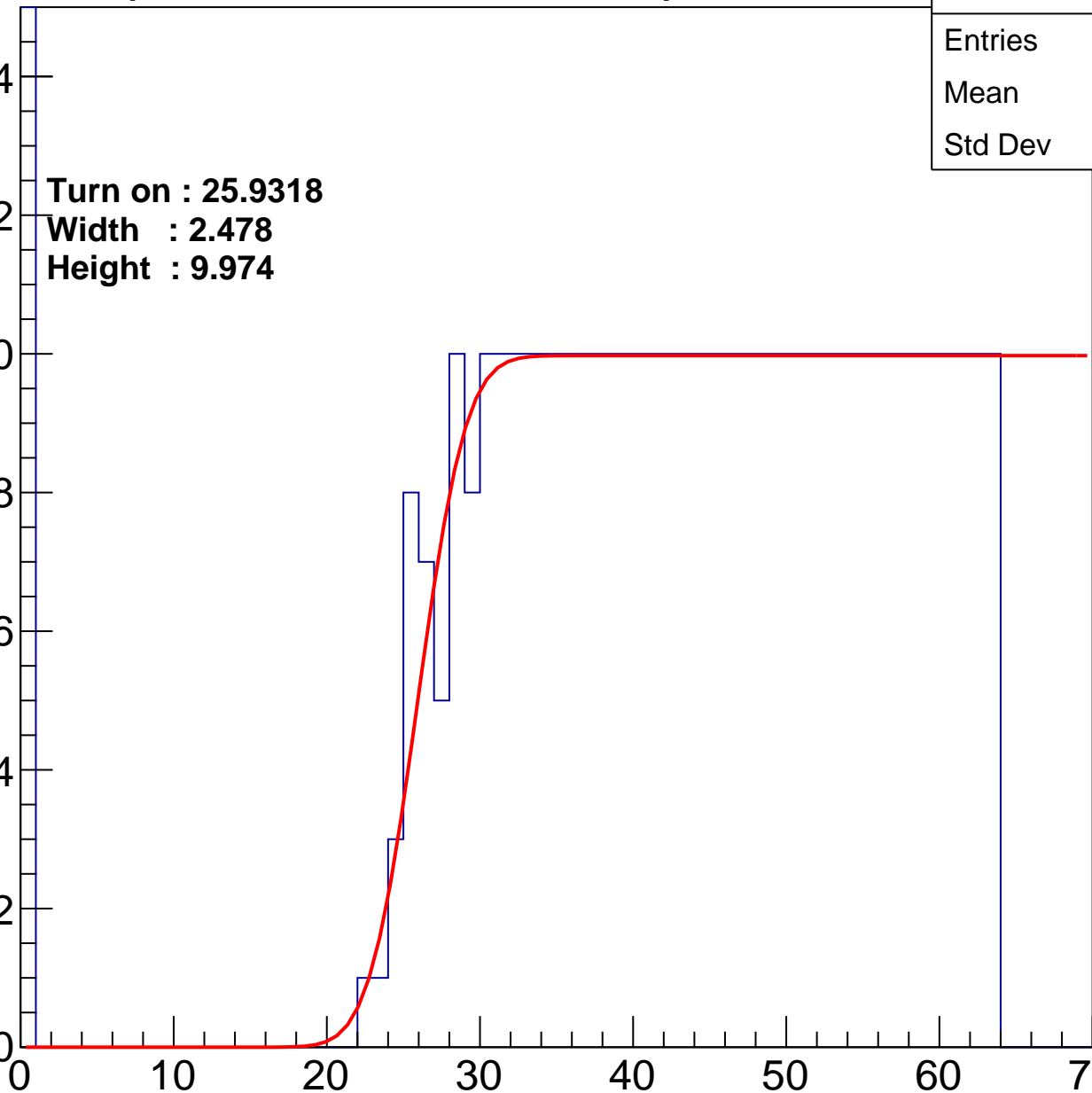
Width : 2.478

Height : 9.974

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U11-ch74

calib_packv5_041523_1651.root, FC#0, port C2

Entries	419
Mean	40.08
Std Dev	17

Turn on : 26.6065

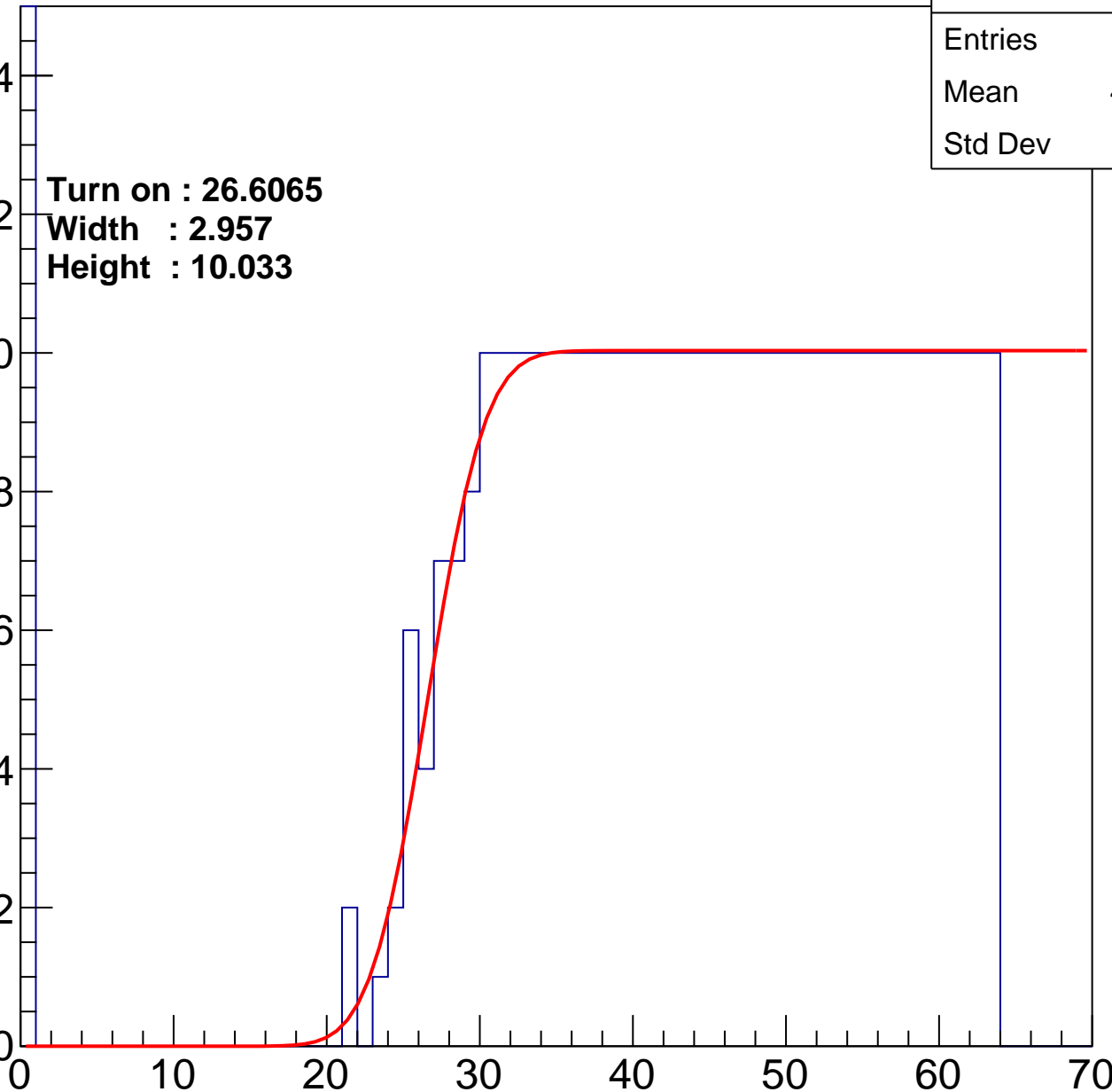
Width : 2.957

Height : 10.033

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U11-ch75

calib_packv5_041523_1651.root, FC#0, port C2

Entries	411
Mean	40.11
Std Dev	17.44

Turn on : 27.7839

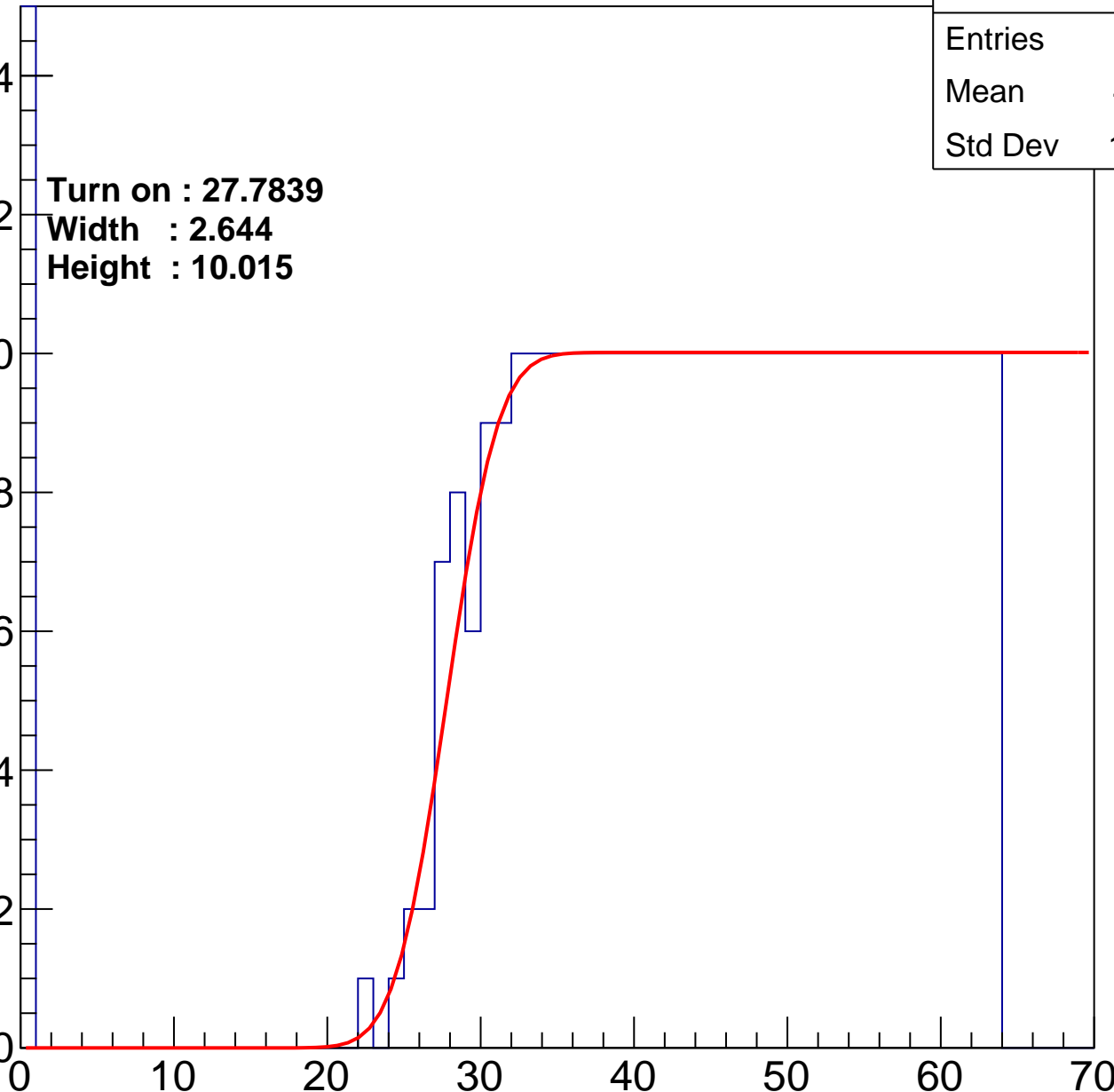
Width : 2.644

Height : 10.015

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U11-ch76

calib_packv5_041523_1651.root, FC#0, port C2

Entries	437
Mean	38.89
Std Dev	17.76

Turn on : 25.9835

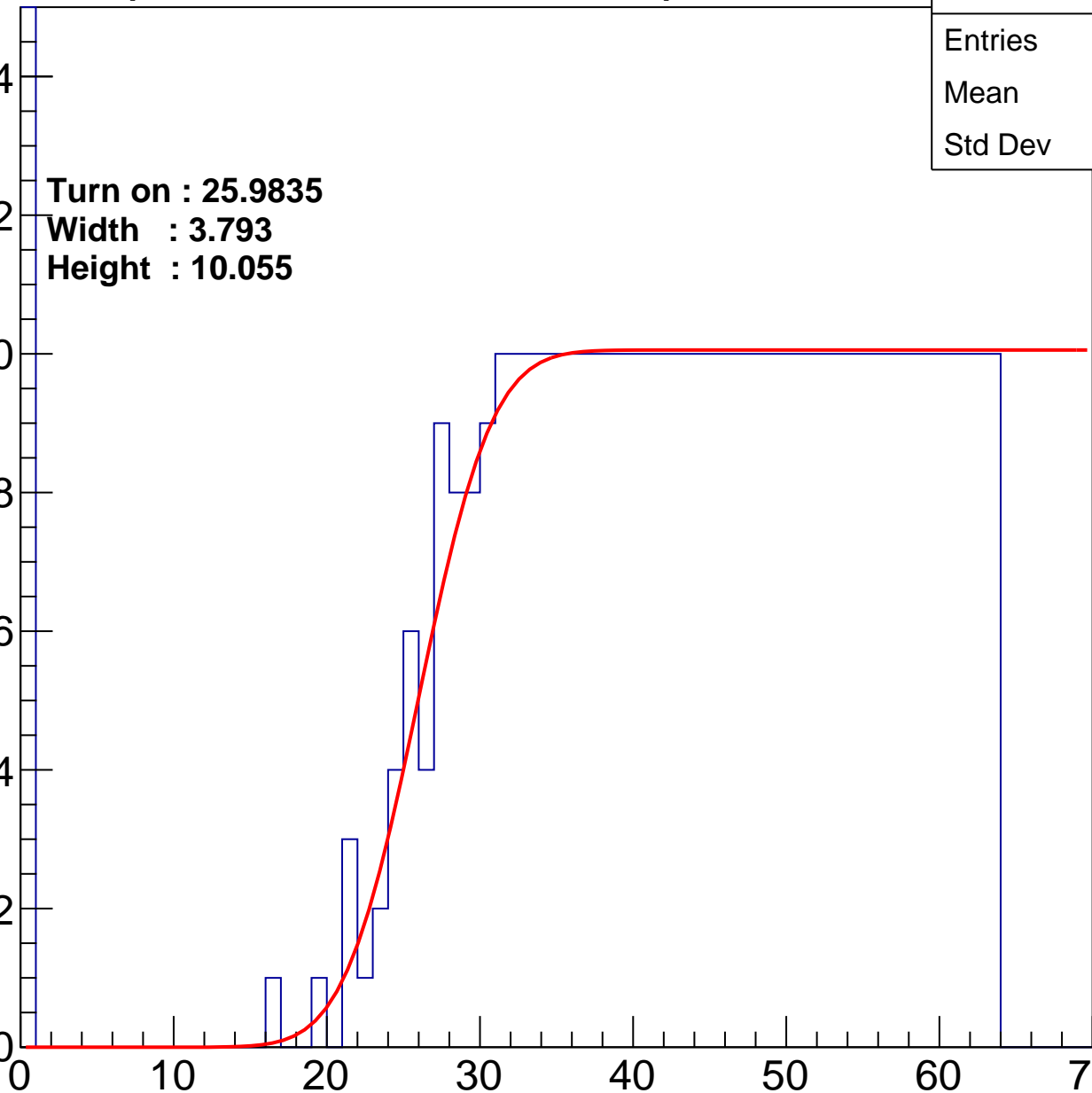
Width : 3.793

Height : 10.055

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U11-ch77

calib_packv5_041523_1651.root, FC#0, port C2

Entries	430
Mean	39.53
Std Dev	17.22

Turn on : 25.4433

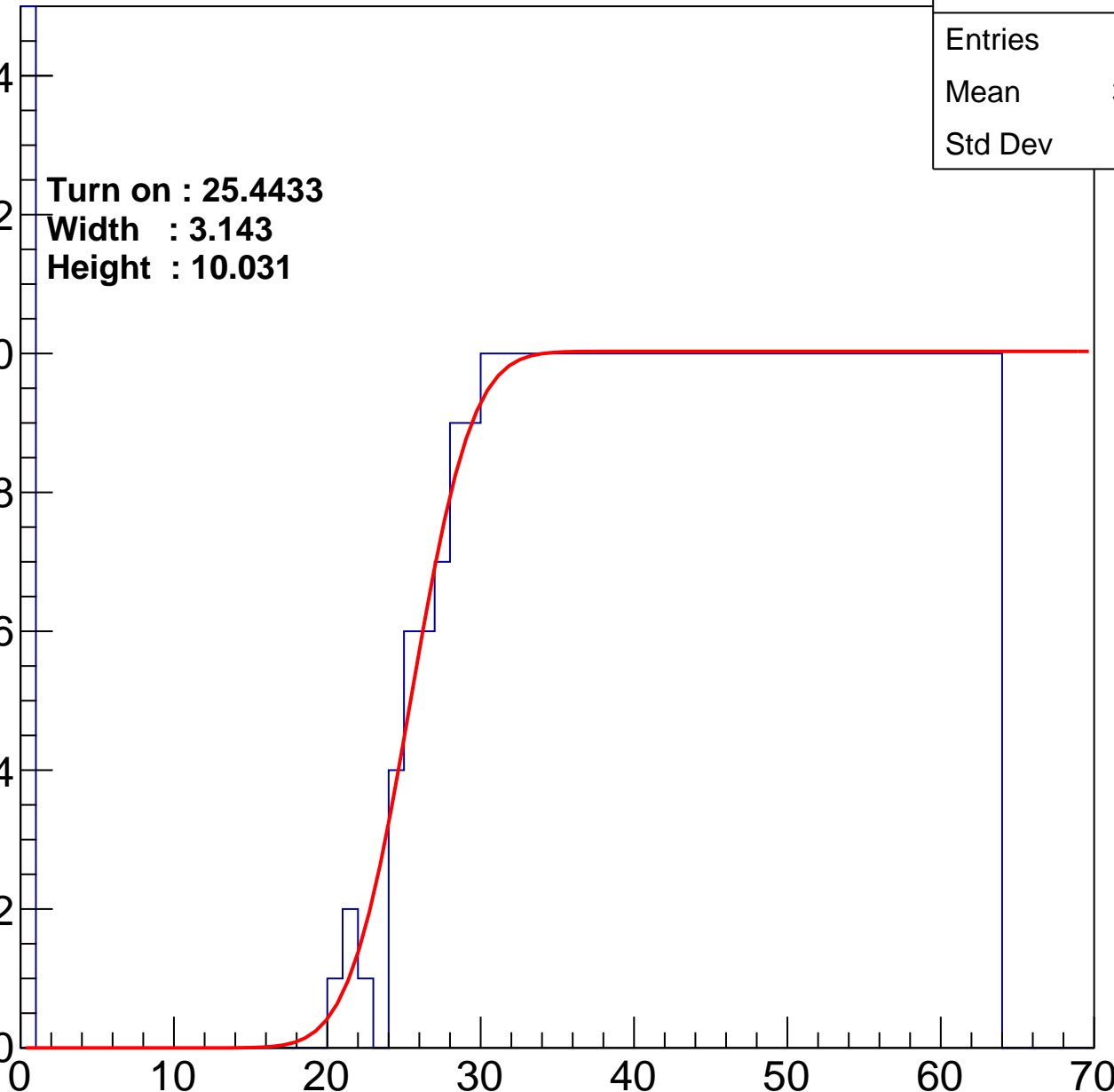
Width : 3.143

Height : 10.031

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U11-ch78

calib_packv5_041523_1651.root, FC#0, port C2

Entries	411
Mean	40.62
Std Dev	16.58

Turn on : 27.0574

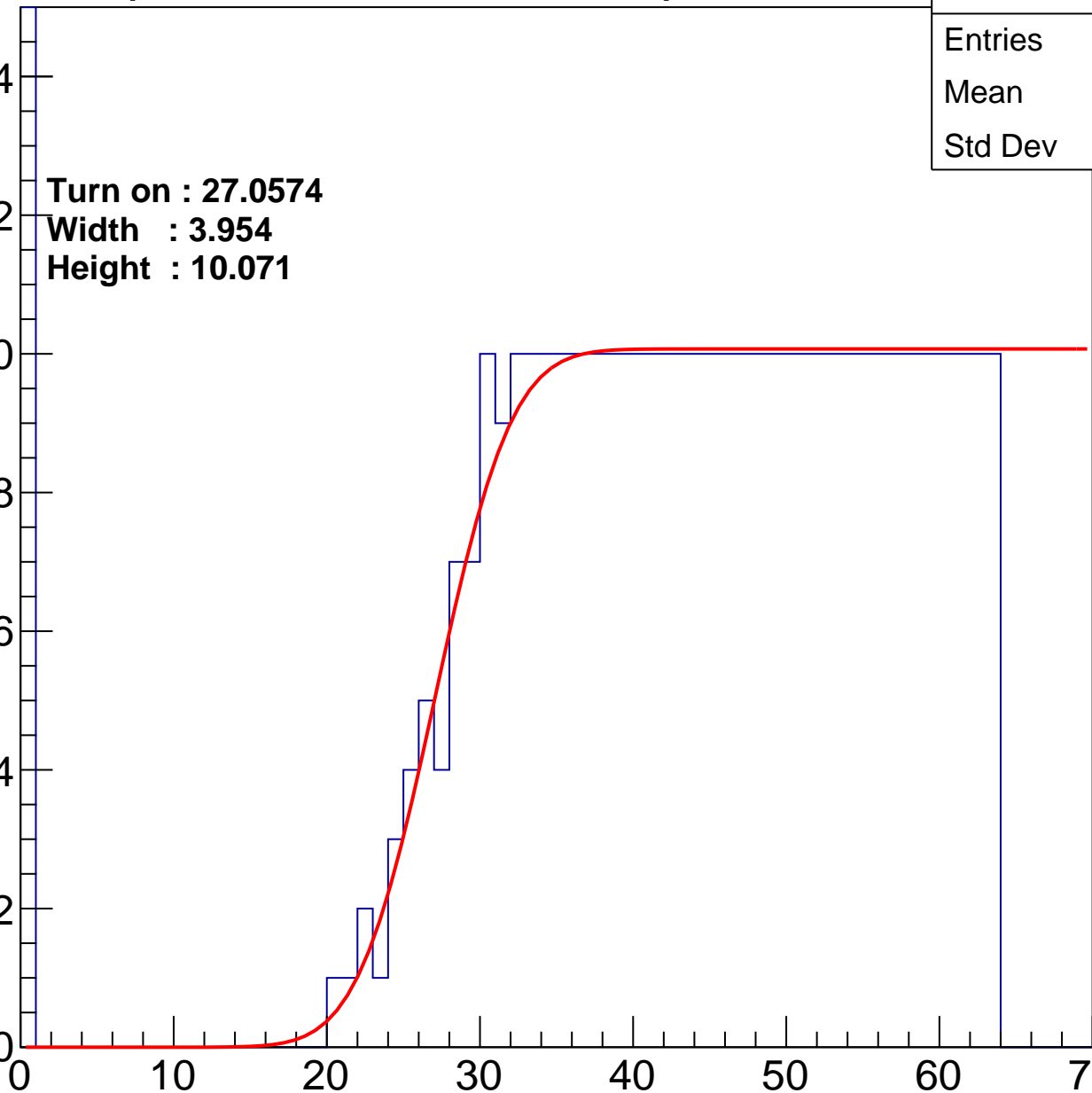
Width : 3.954

Height : 10.071

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U11-ch79

calib_packv5_041523_1651.root, FC#0, port C2

Entries	416
Mean	40.15
Std Dev	17.05

Turn on : 27.2149

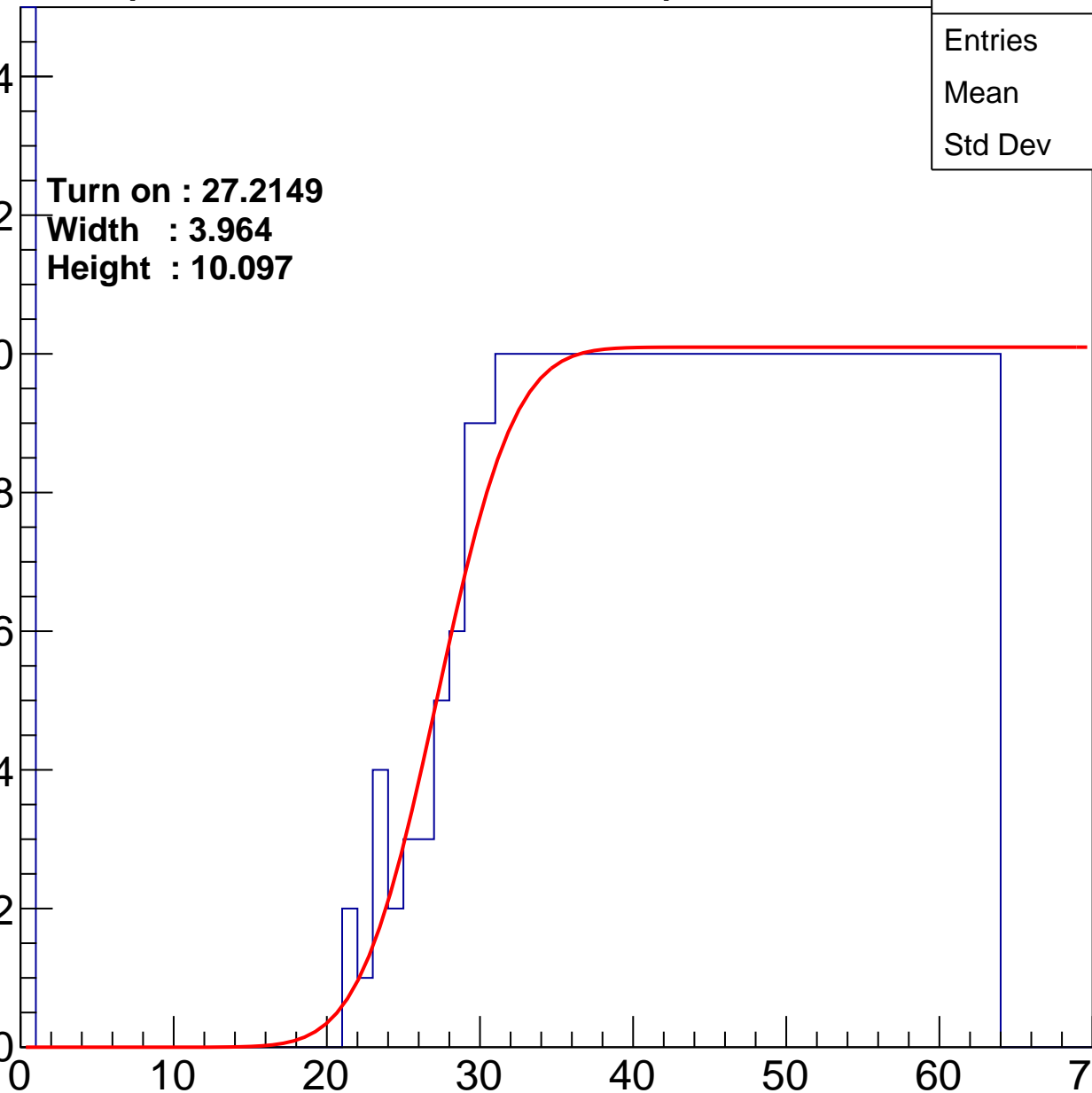
Width : 3.964

Height : 10.097

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U11-ch80

calib_packv5_041523_1651.root, FC#0, port C2

Entries	445
Mean	38.77
Std Dev	17.55

Turn on : 24.7348

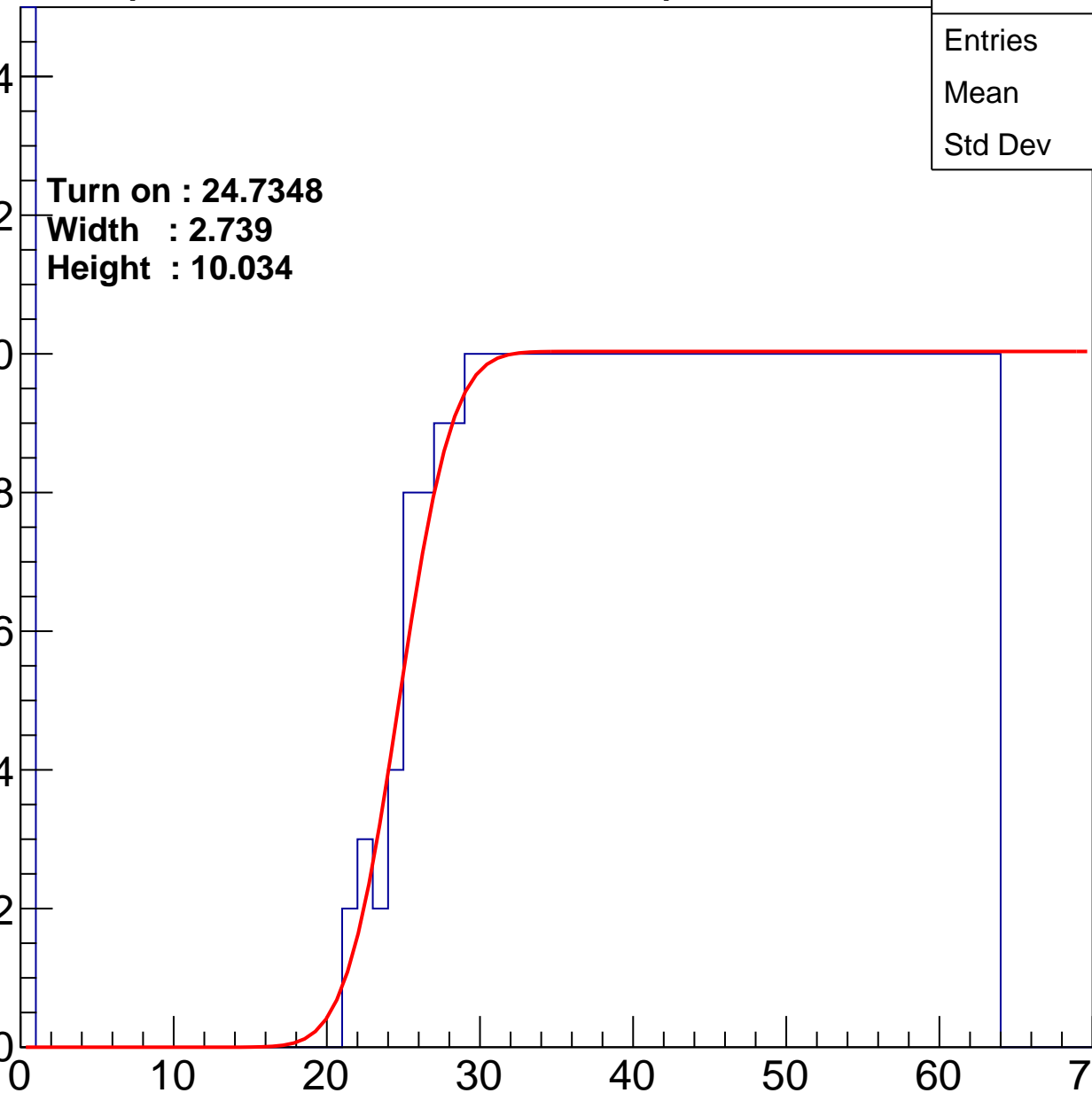
Width : 2.739

Height : 10.034

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U11-ch81

calib_packv5_041523_1651.root, FC#0, port C2

Entries	410
Mean	40.16
Std Dev	17.43

Turn on : 27.8913

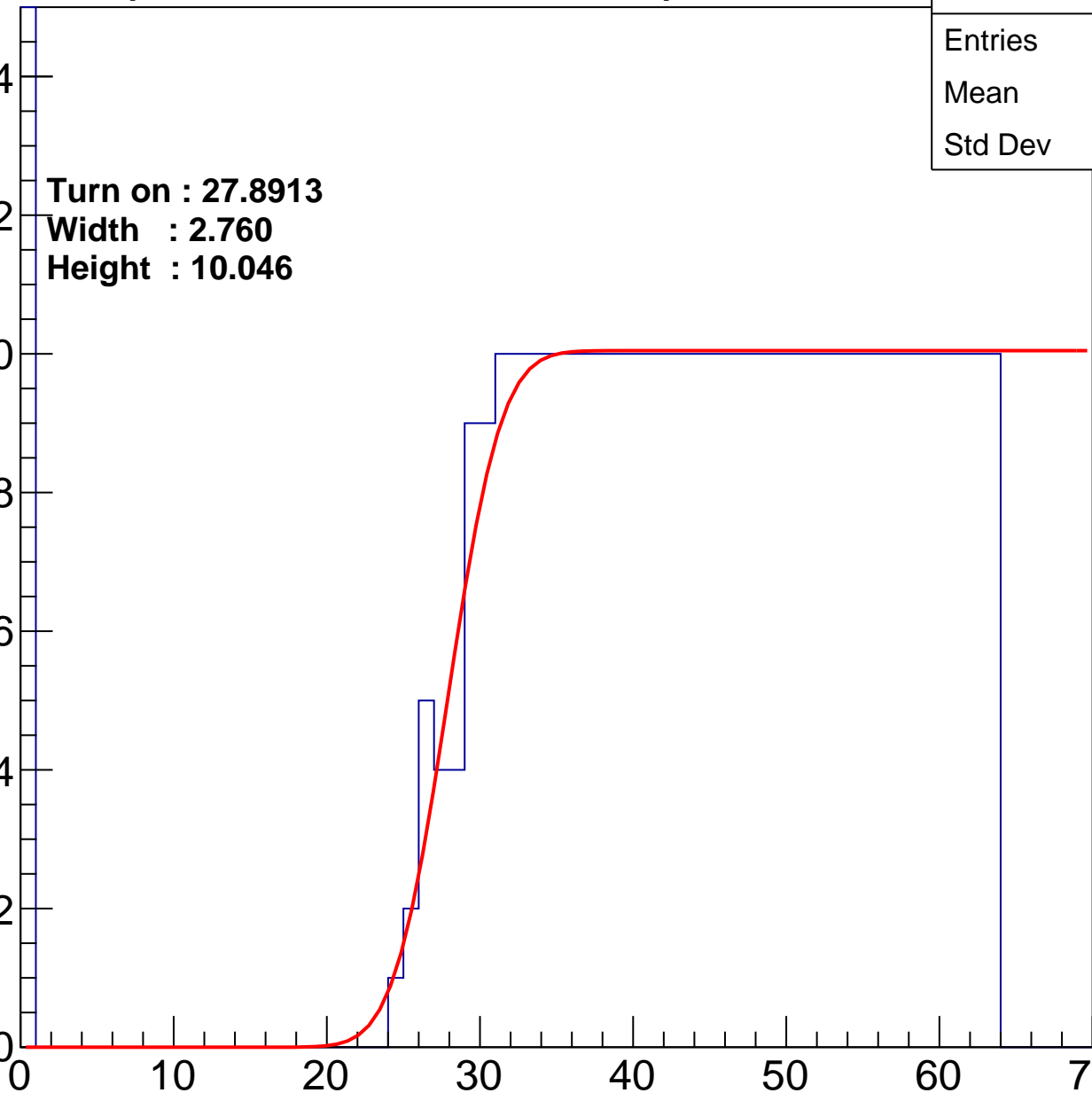
Width : 2.760

Height : 10.046

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U11-ch82

calib_packv5_041523_1651.root, FC#0, port C2

Entries	535
Mean	32.25
Std Dev	21.43

Turn on : 25.4286

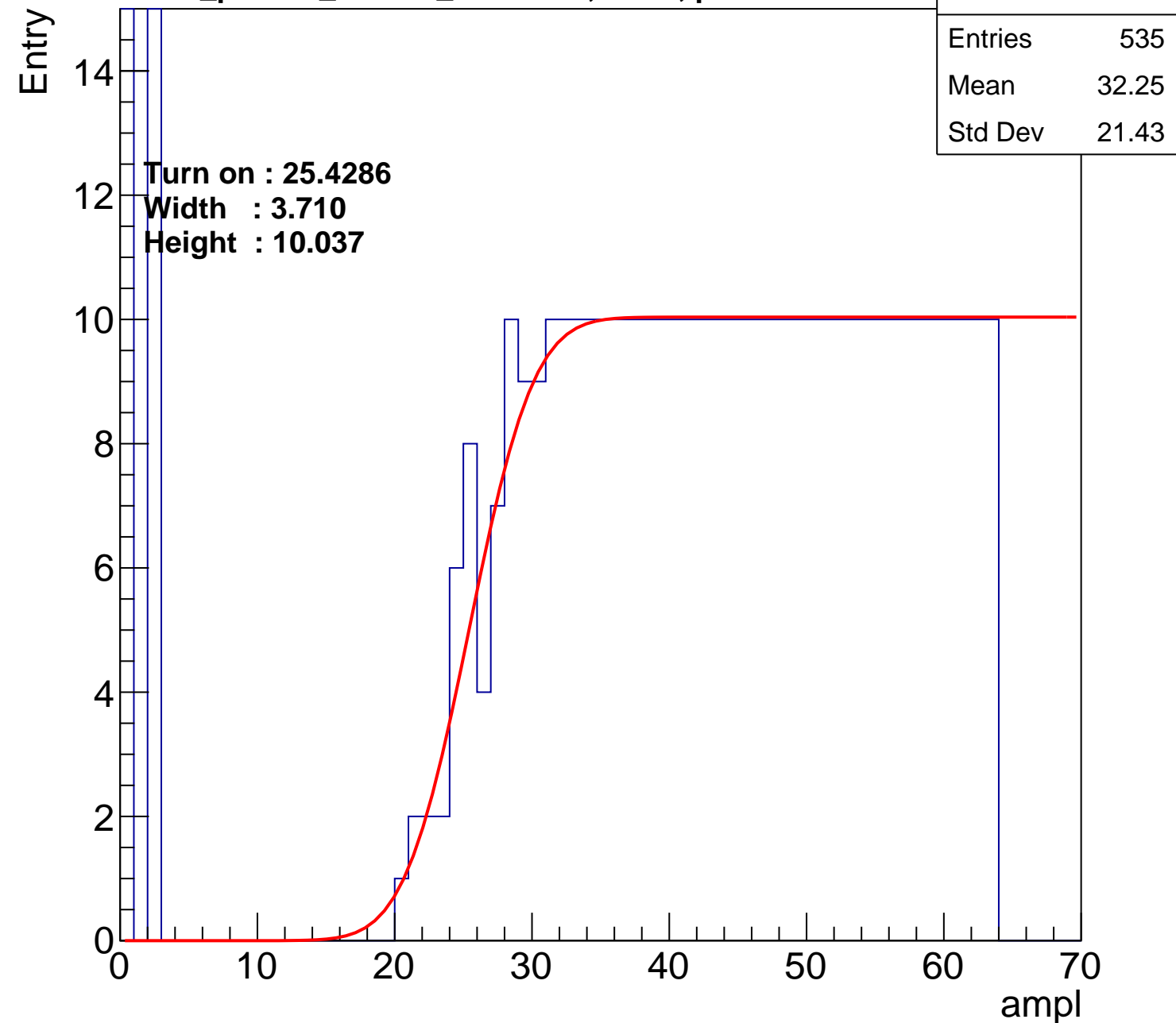
Width : 3.710

Height : 10.037

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U11-ch83

calib_packv5_041523_1651.root, FC#0, port C2

Entries	411
Mean	40.93
Std Dev	16.09

Turn on : 26.3646

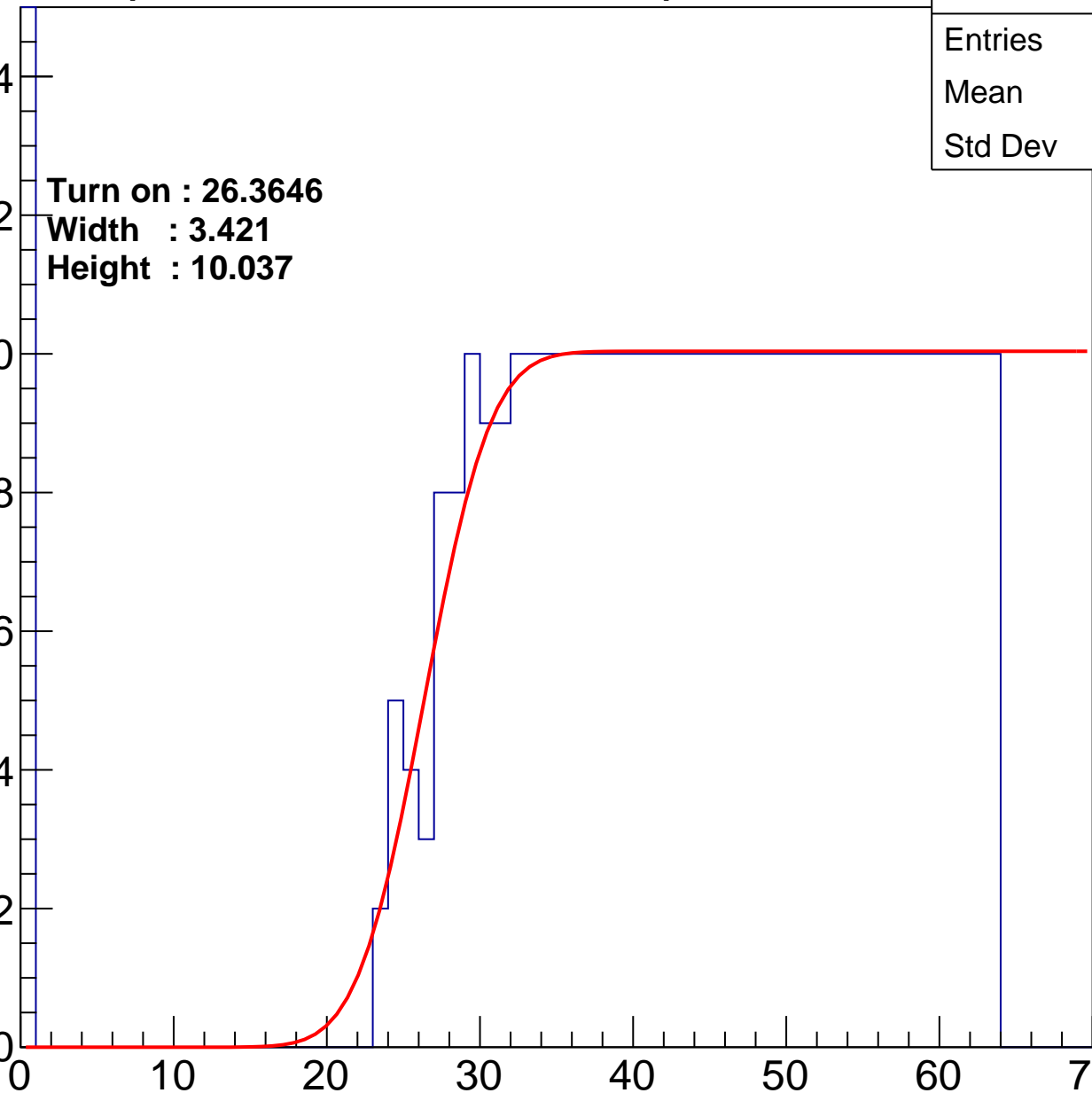
Width : 3.421

Height : 10.037

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U11-ch84

calib_packv5_041523_1651.root, FC#0, port C2

Entries	442
Mean	38.8
Std Dev	17.66

Turn on : 24.8229

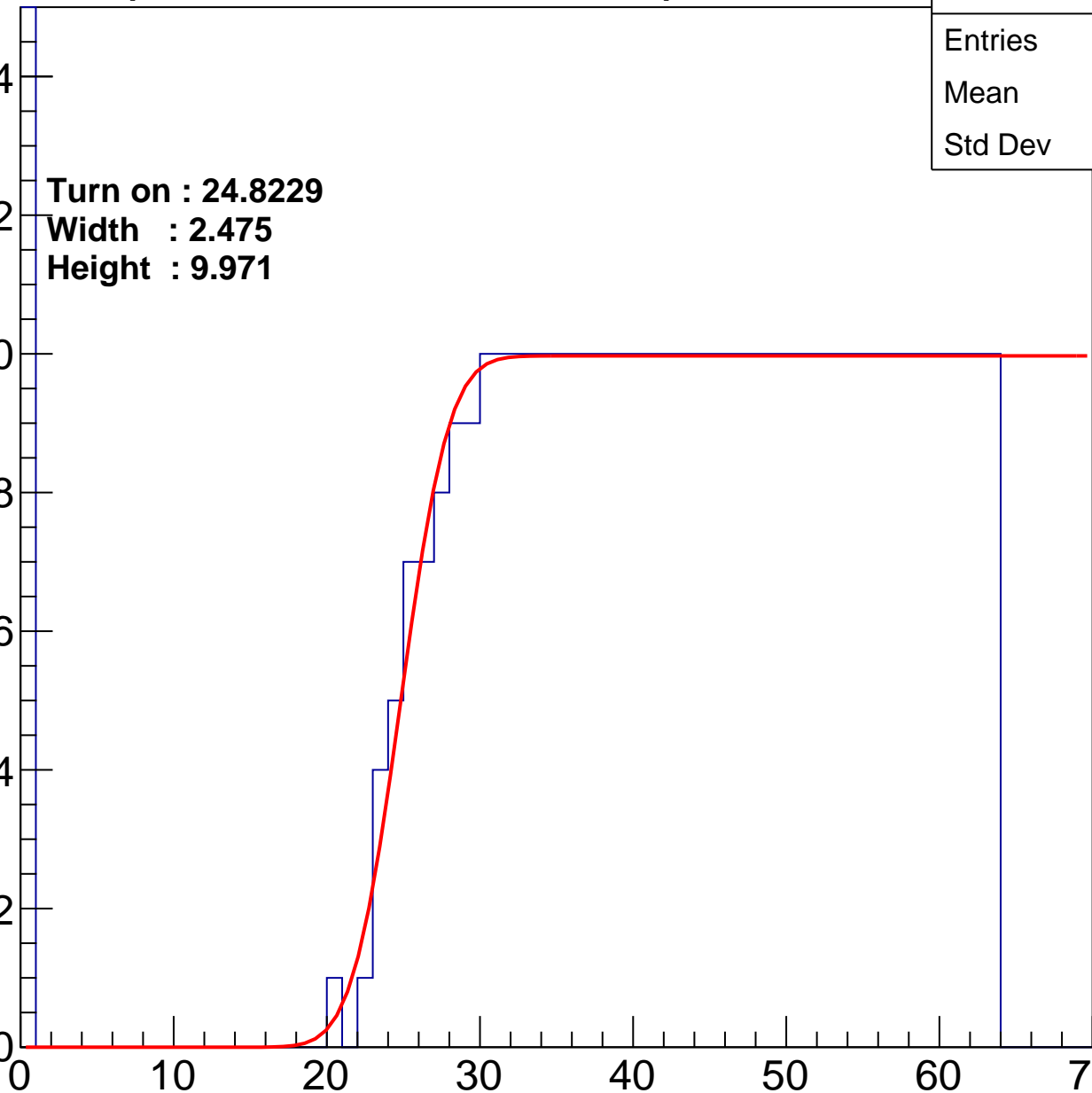
Width : 2.475

Height : 9.971

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U11-ch85

calib_packv5_041523_1651.root, FC#0, port C2

Entries	401
Mean	41.23
Std Dev	16.17

Turn on : 27.4890

Width : 3.576

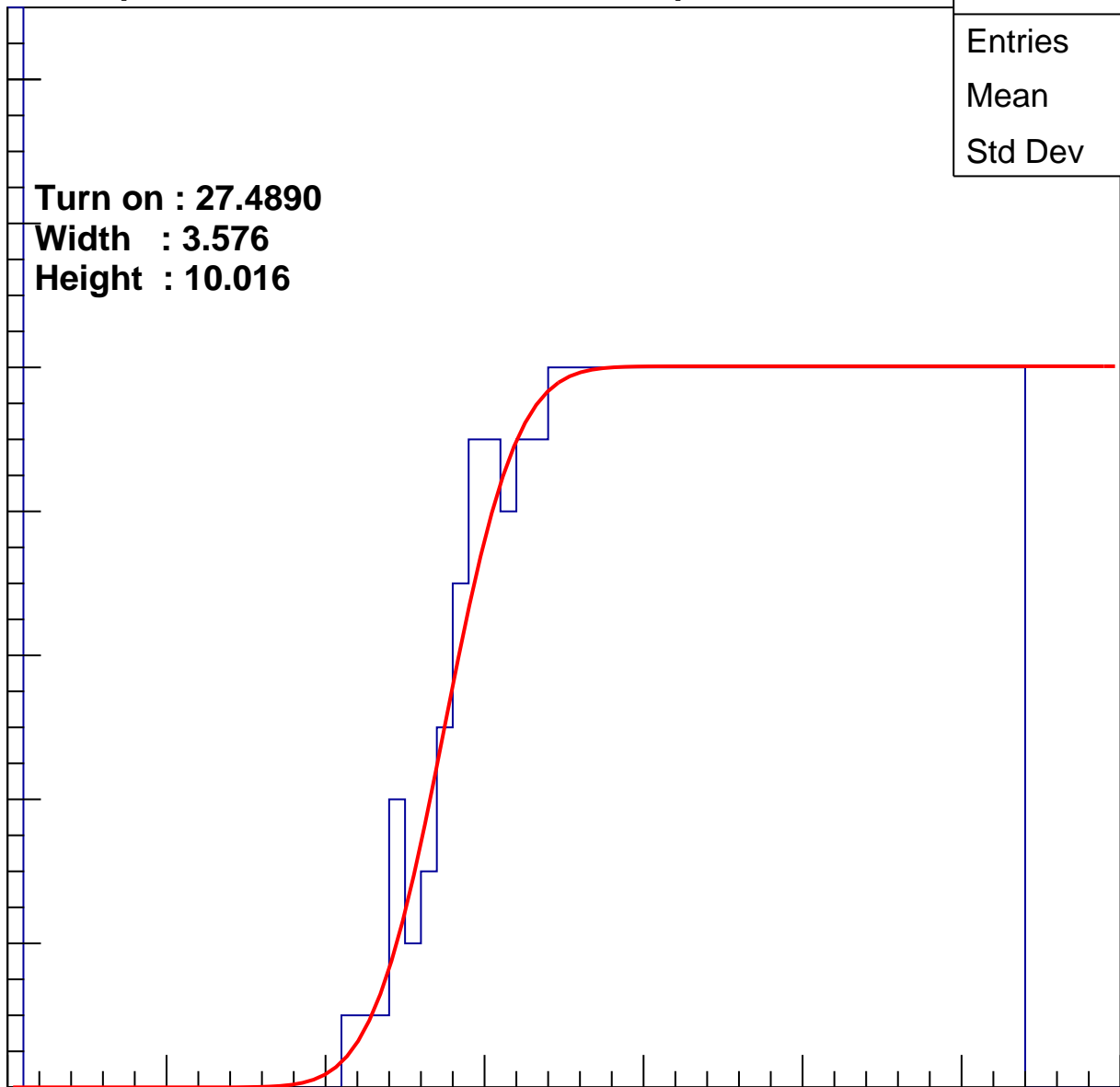
Height : 10.016

Entry

14
12
10
8
6
4
2
0

ampl

0 10 20 30 40 50 60 70



B1L103S, U11-ch86

calib_packv5_041523_1651.root, FC#0, port C2

Entries	399
Mean	40.82
Std Dev	17.03

Turn on : 28.3970

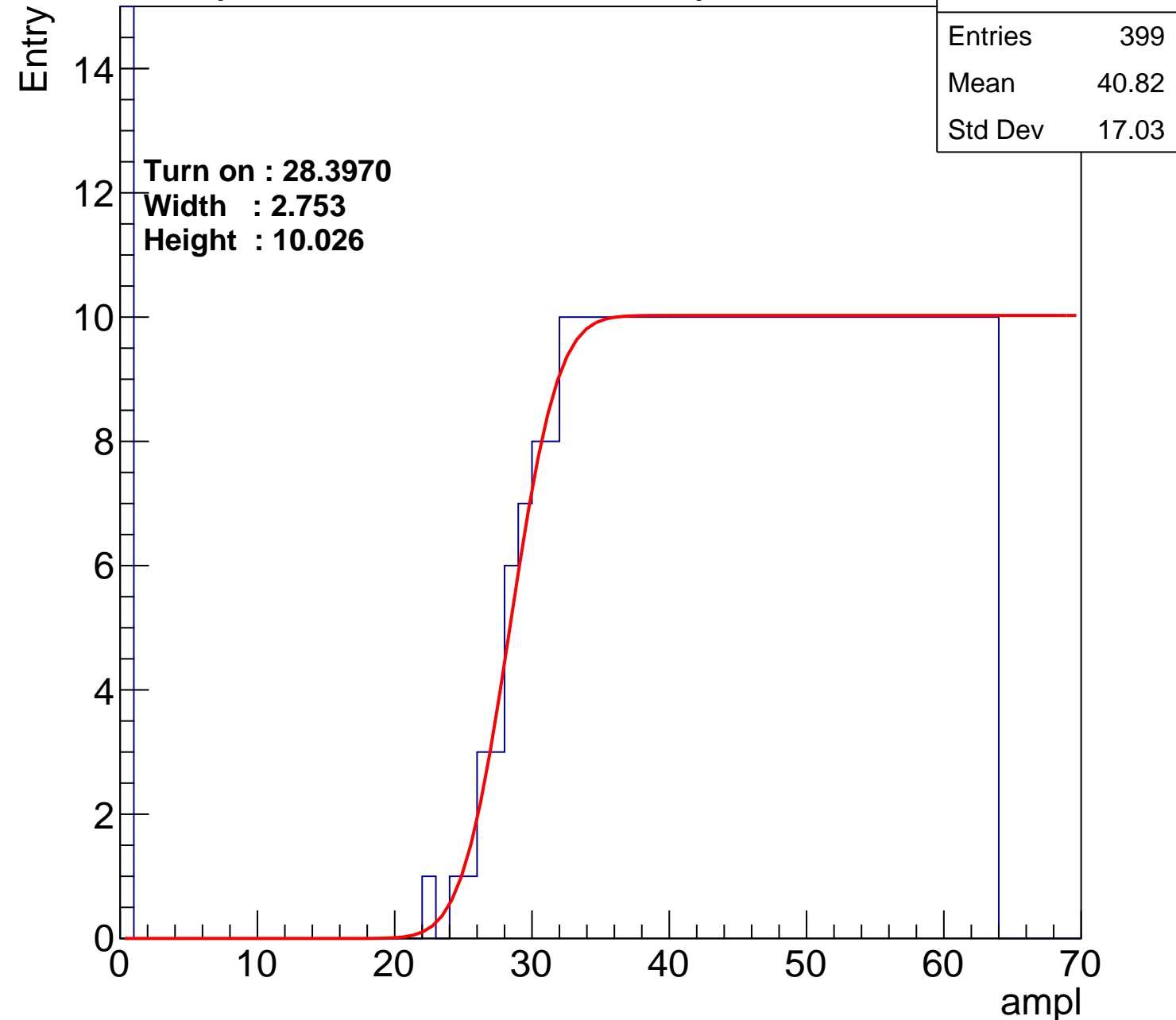
Width : 2.753

Height : 10.026

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U11-ch87

calib_packv5_041523_1651.root, FC#0, port C2

Entries	428
Mean	39.05
Std Dev	18.05

Turn on : 26.9484

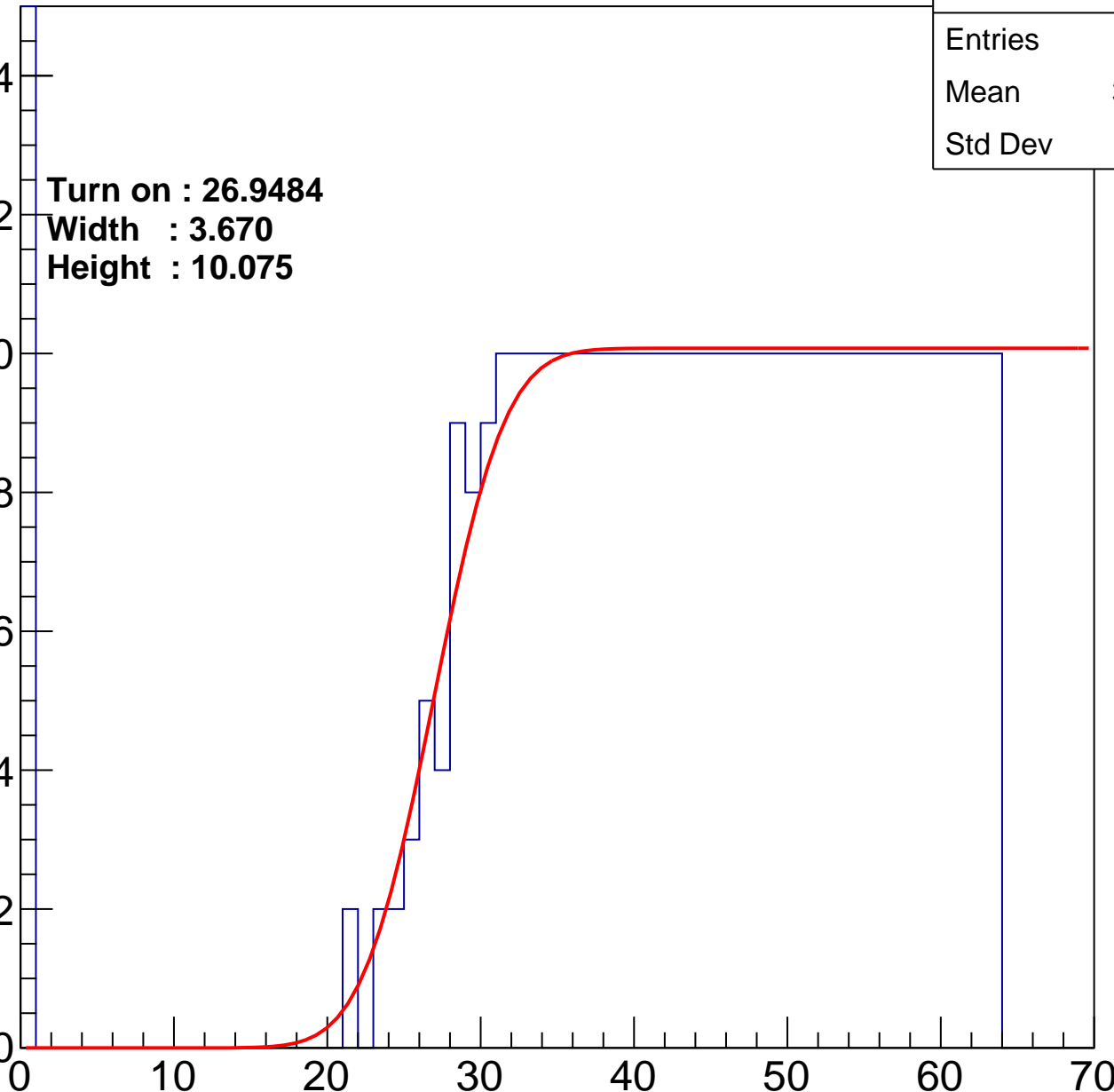
Width : 3.670

Height : 10.075

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U11-ch88

calib_packv5_041523_1651.root, FC#0, port C2

Entries	404
Mean	41.08
Std Dev	16.26

Turn on : 27.2924

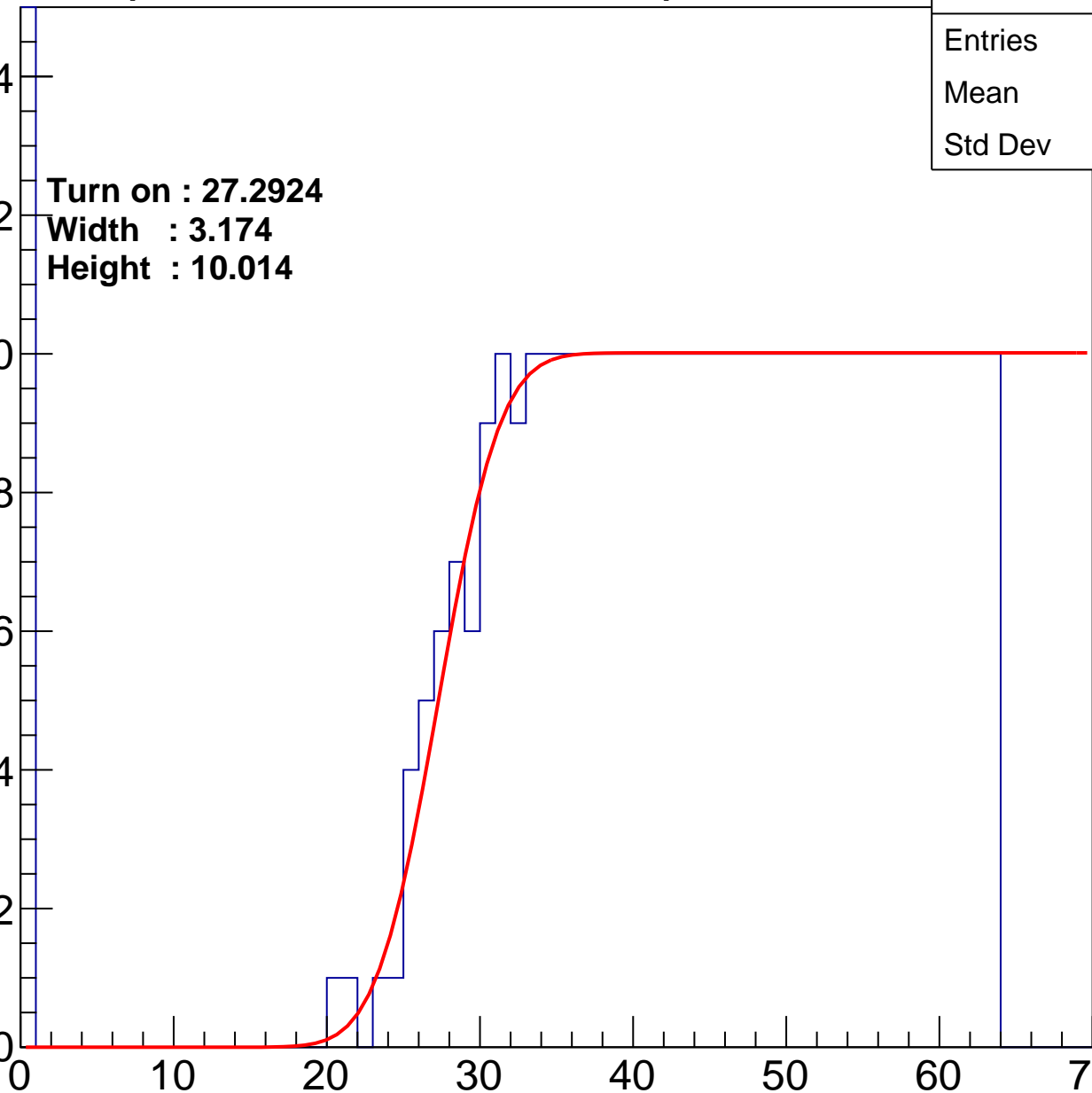
Width : 3.174

Height : 10.014

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U11-ch89

calib_packv5_041523_1651.root, FC#0, port C2

Entries	402
Mean	40.94
Std Dev	16.67

Turn on : 28.0044

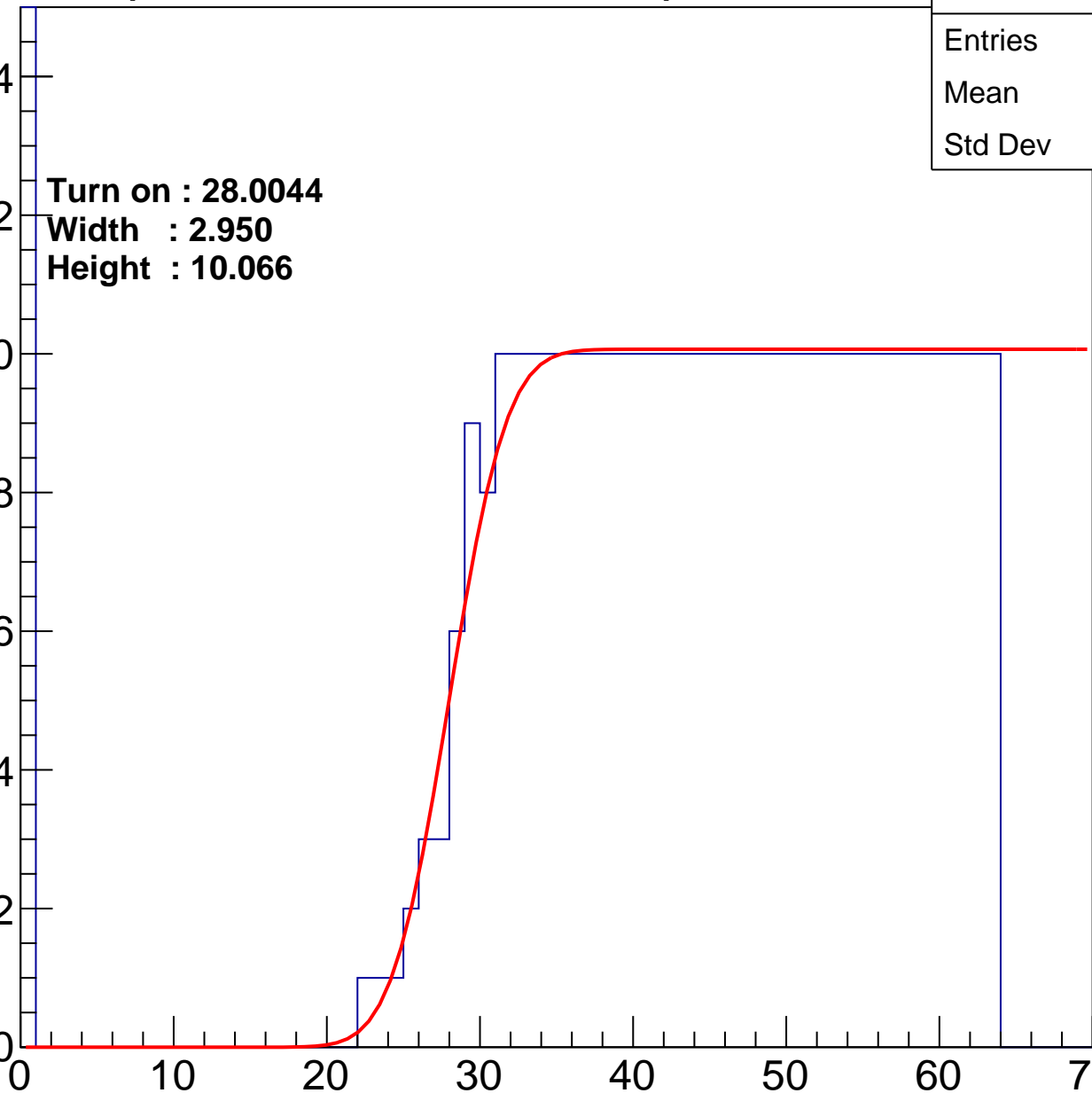
Width : 2.950

Height : 10.066

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U11-ch90

calib_packv5_041523_1651.root, FC#0, port C2

Entries	418
Mean	40.4
Std Dev	16.52

Turn on : 26.0559

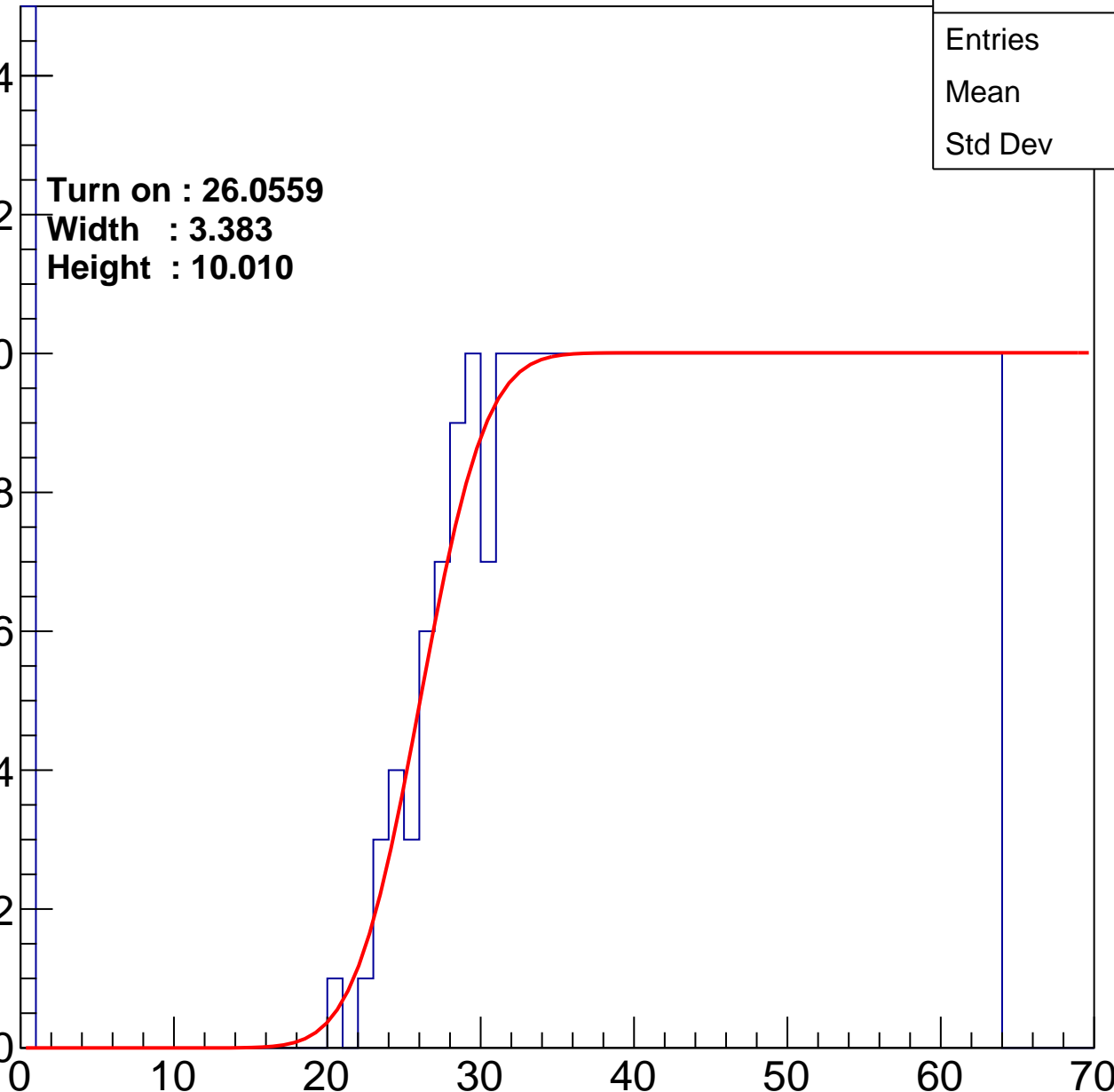
Width : 3.383

Height : 10.010

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U11-ch91

calib_packv5_041523_1651.root, FC#0, port C2

Entries	427
Mean	38.85
Std Dev	18.39

Turn on : 27.3357

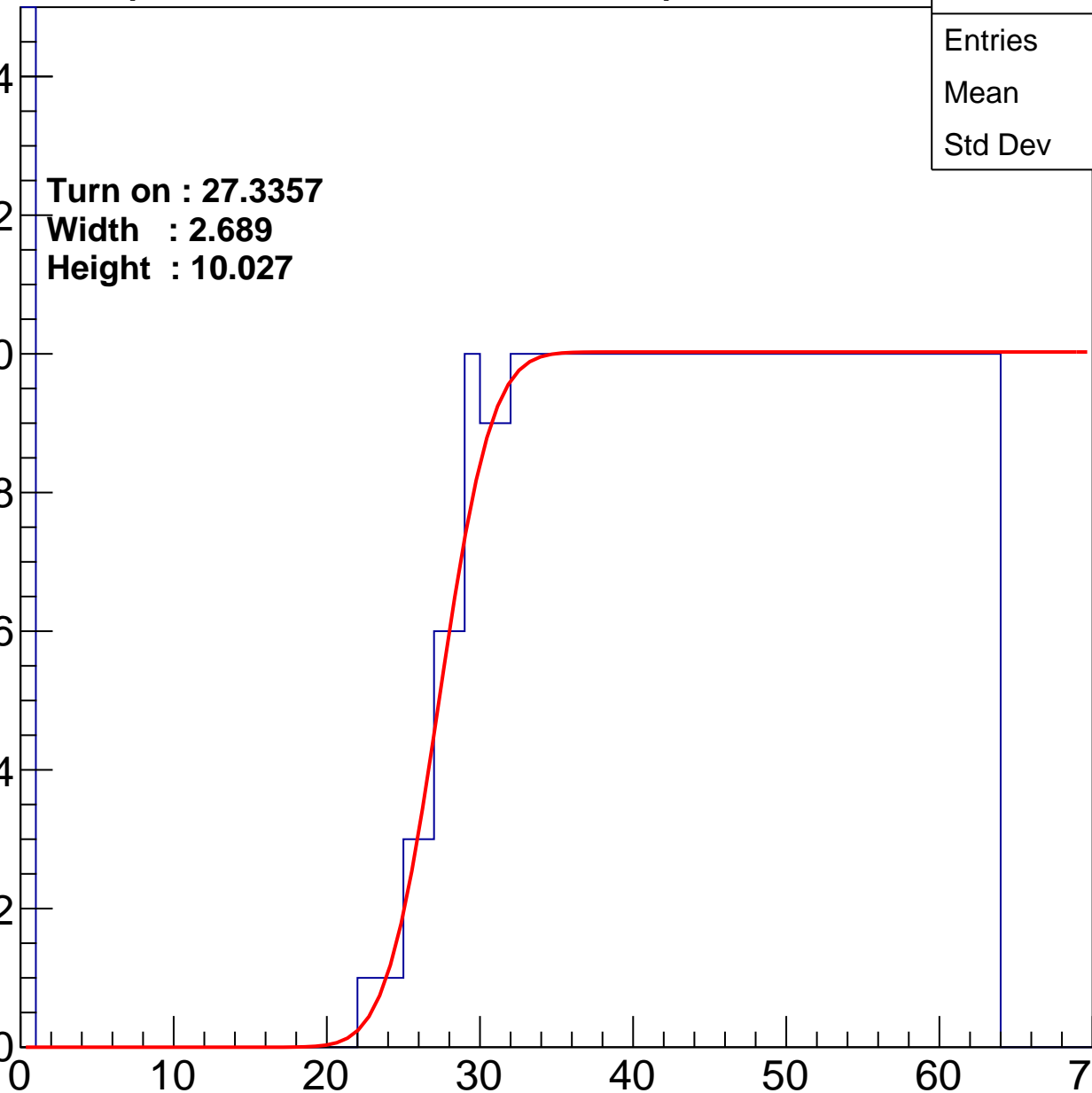
Width : 2.689

Height : 10.027

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U11-ch92

calib_packv5_041523_1651.root, FC#0, port C2

Entries	465
Mean	37.58
Std Dev	18.21

Turn on : 23.4050

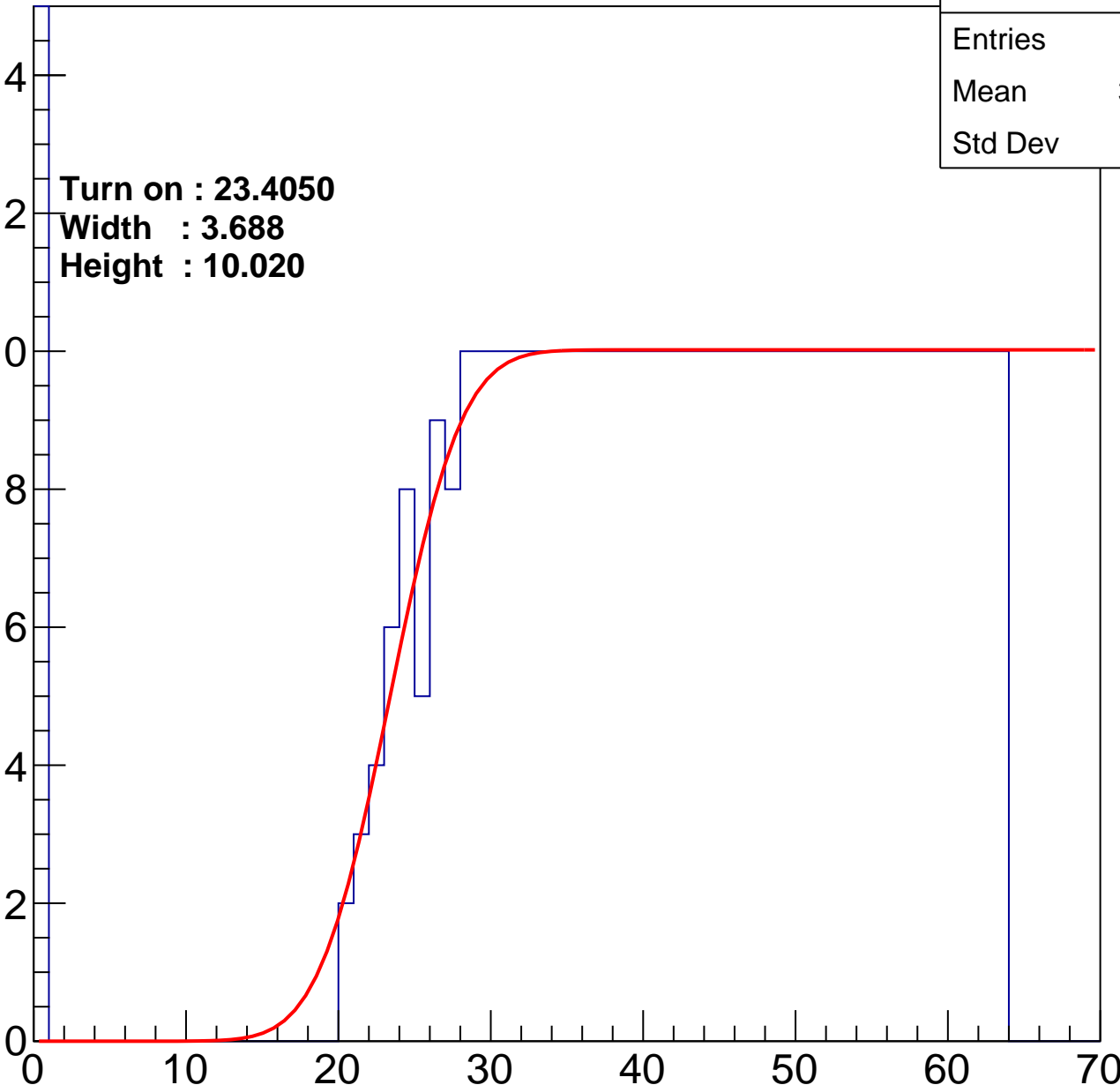
Width : 3.688

Height : 10.020

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U11-ch93

calib_packv5_041523_1651.root, FC#0, port C2

Entries	421
Mean	39.68
Std Dev	17.48

Turn on : 26.6016

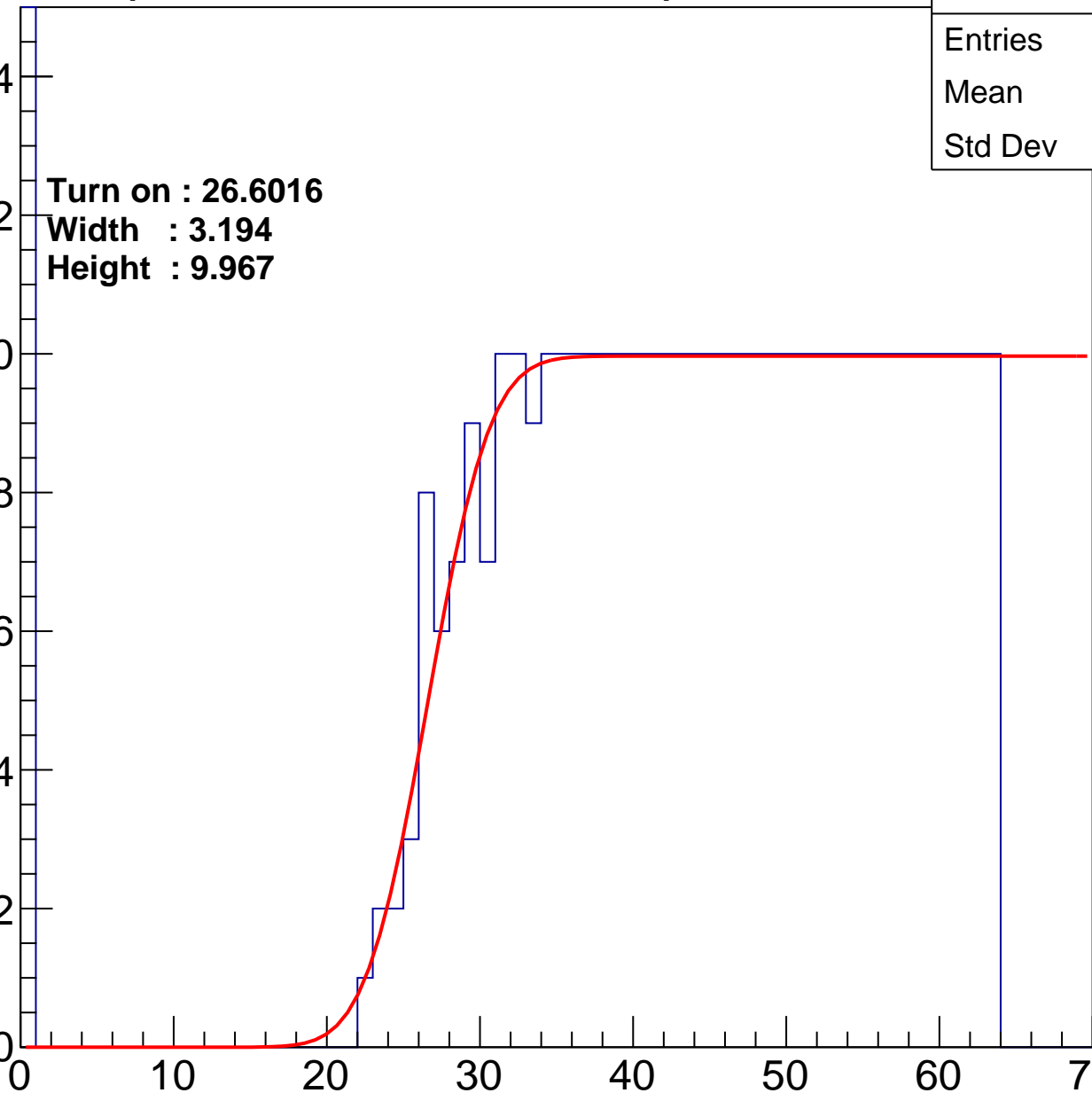
Width : 3.194

Height : 9.967

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U11-ch94

calib_packv5_041523_1651.root, FC#0, port C2

Entries	432
Mean	39.48
Std Dev	17.16

Turn on : 25.8830

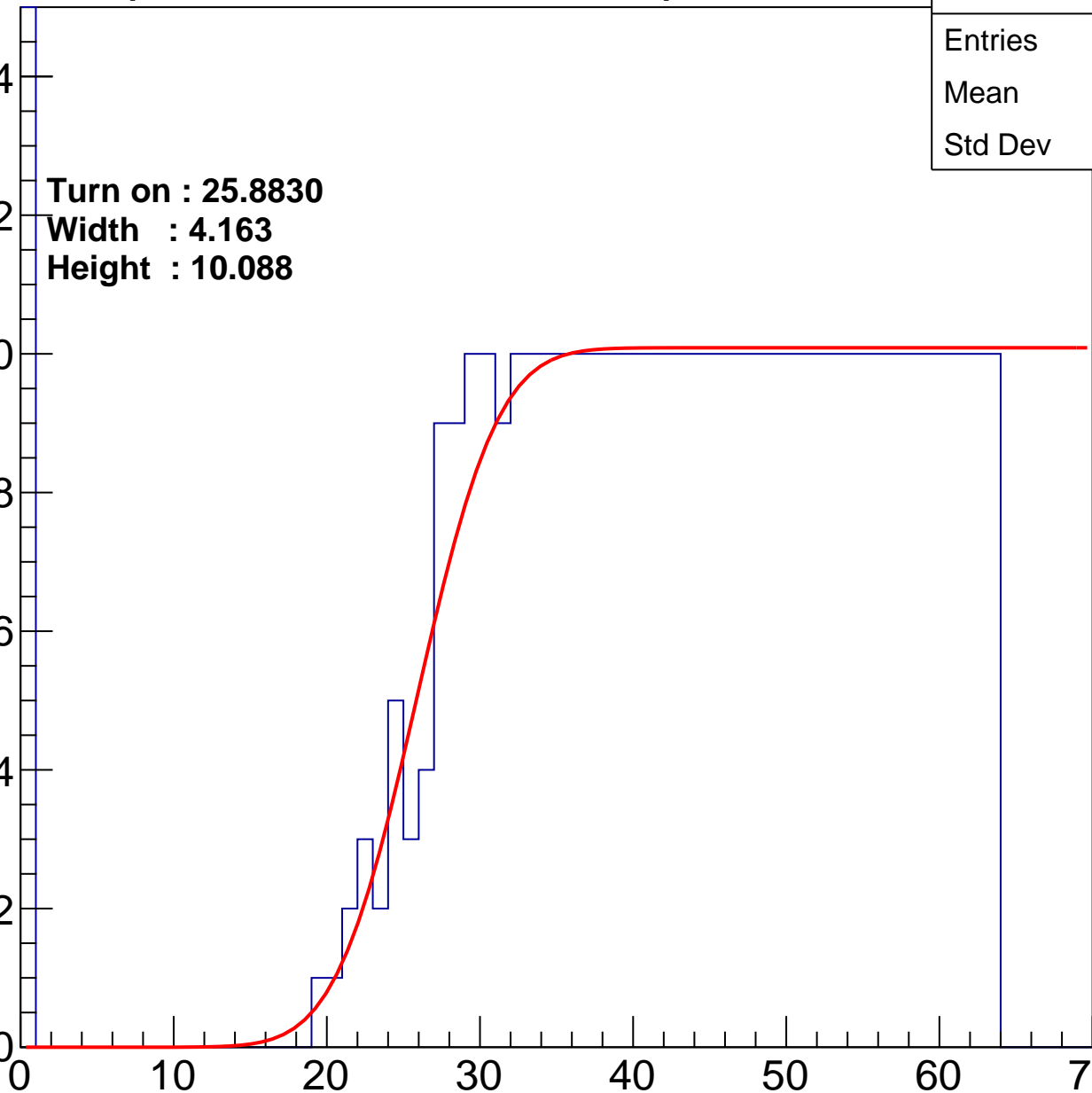
Width : 4.163

Height : 10.088

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U11-ch95

calib_packv5_041523_1651.root, FC#0, port C2

Entries	445
Mean	38.2
Std Dev	18.33

Turn on : 25.1919

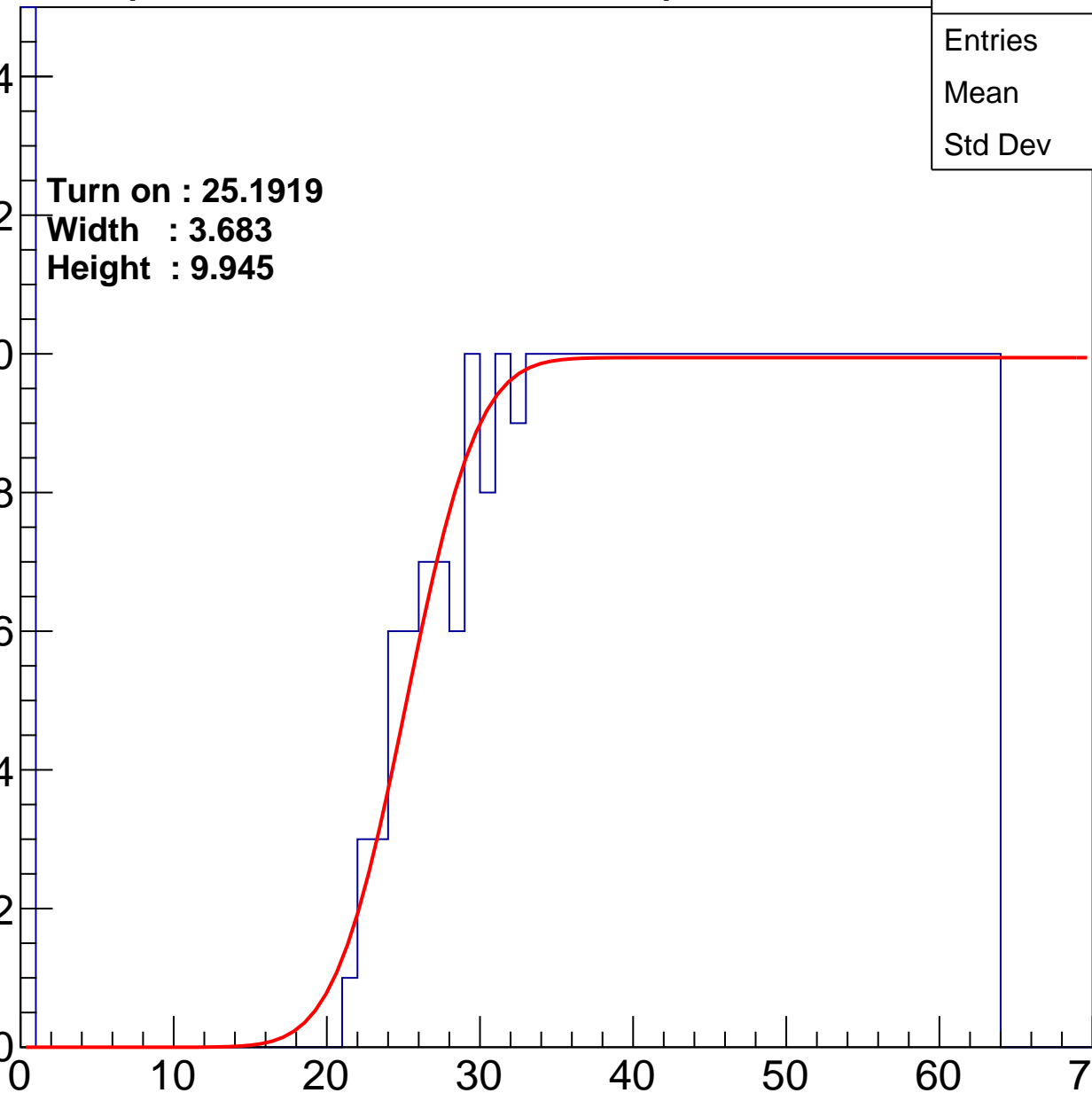
Width : 3.683

Height : 9.945

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U11-ch96

calib_packv5_041523_1651.root, FC#0, port C2

Entries	423
Mean	39.61
Std Dev	17.48

Turn on : 26.8805

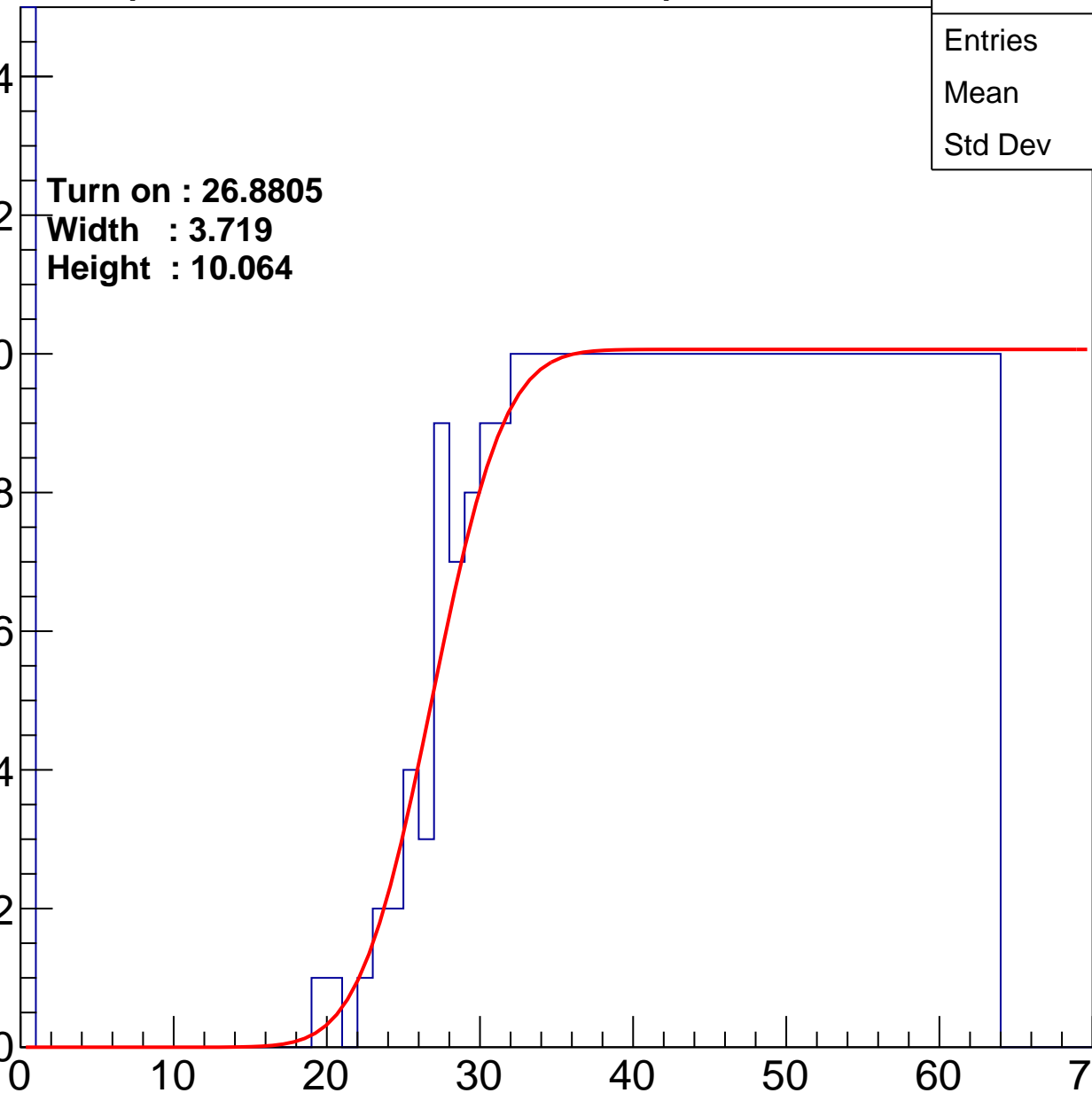
Width : 3.719

Height : 10.064

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U11-ch97

calib_packv5_041523_1651.root, FC#0, port C2

Entries	391
Mean	40.86
Std Dev	17.44

Turn on : 29.5614

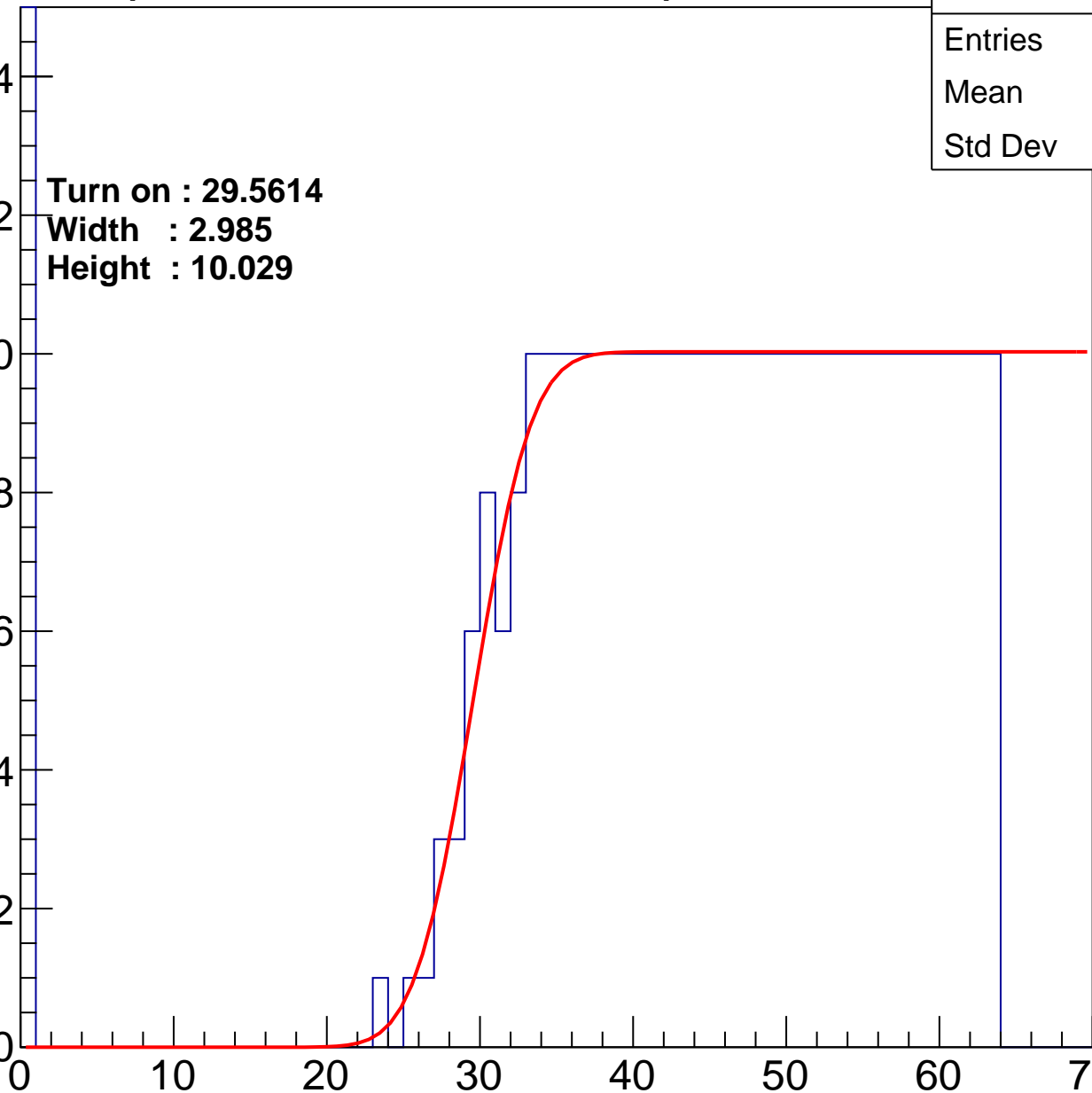
Width : 2.985

Height : 10.029

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U11-ch98

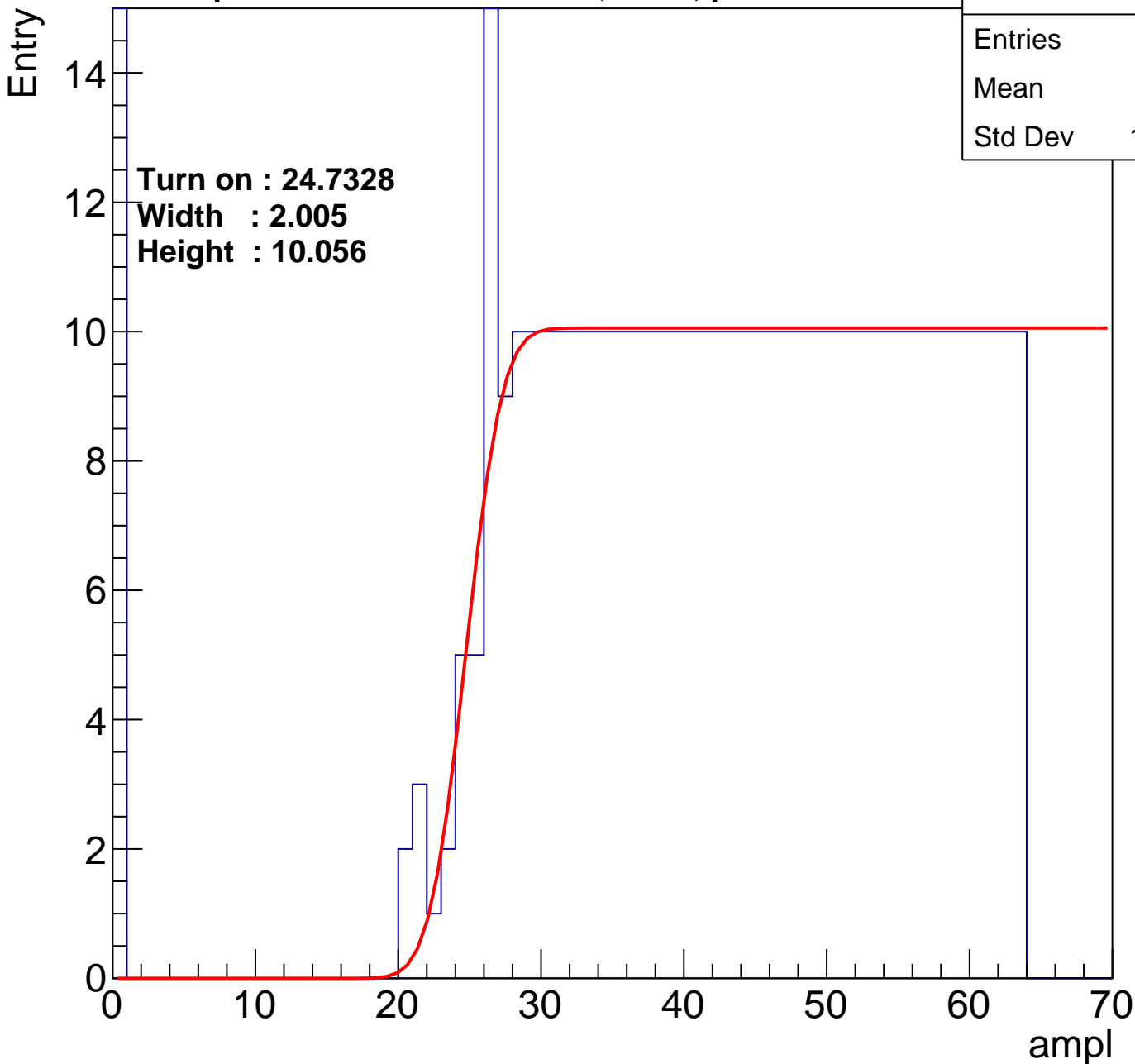
calib_packv5_041523_1651.root, FC#0, port C2

Entries	454
Mean	38.5
Std Dev	17.48

Turn on : 24.7328

Width : 2.005

Height : 10.056



B1L103S, U11-ch99

calib_packv5_041523_1651.root, FC#0, port C2

Entries	397
Mean	41.16
Std Dev	16.6

Turn on : 28.4551

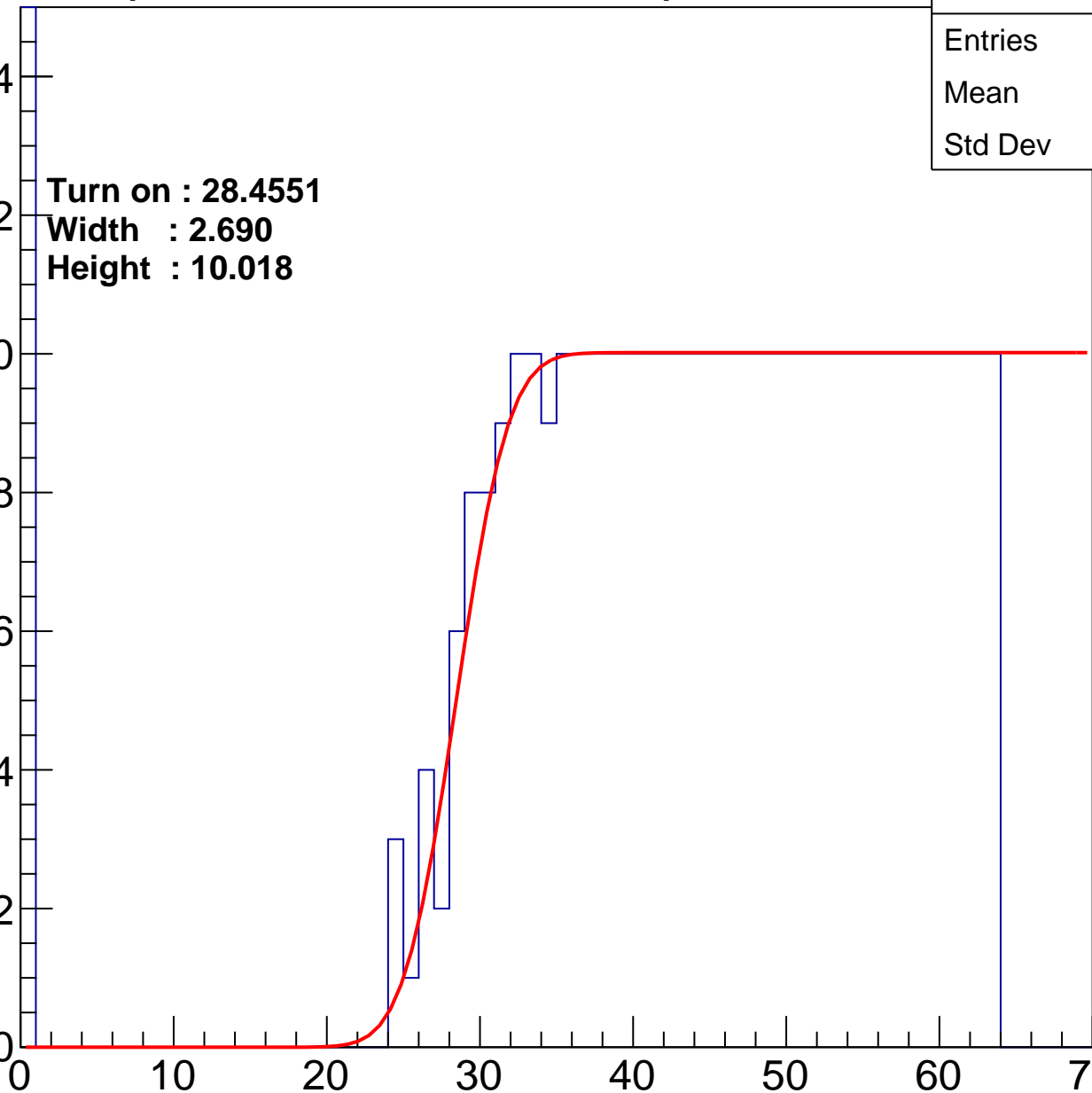
Width : 2.690

Height : 10.018

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U11-ch100

calib_packv5_041523_1651.root, FC#0, port C2

Entries	438
Mean	39.38
Std Dev	17

Turn on : 24.7719

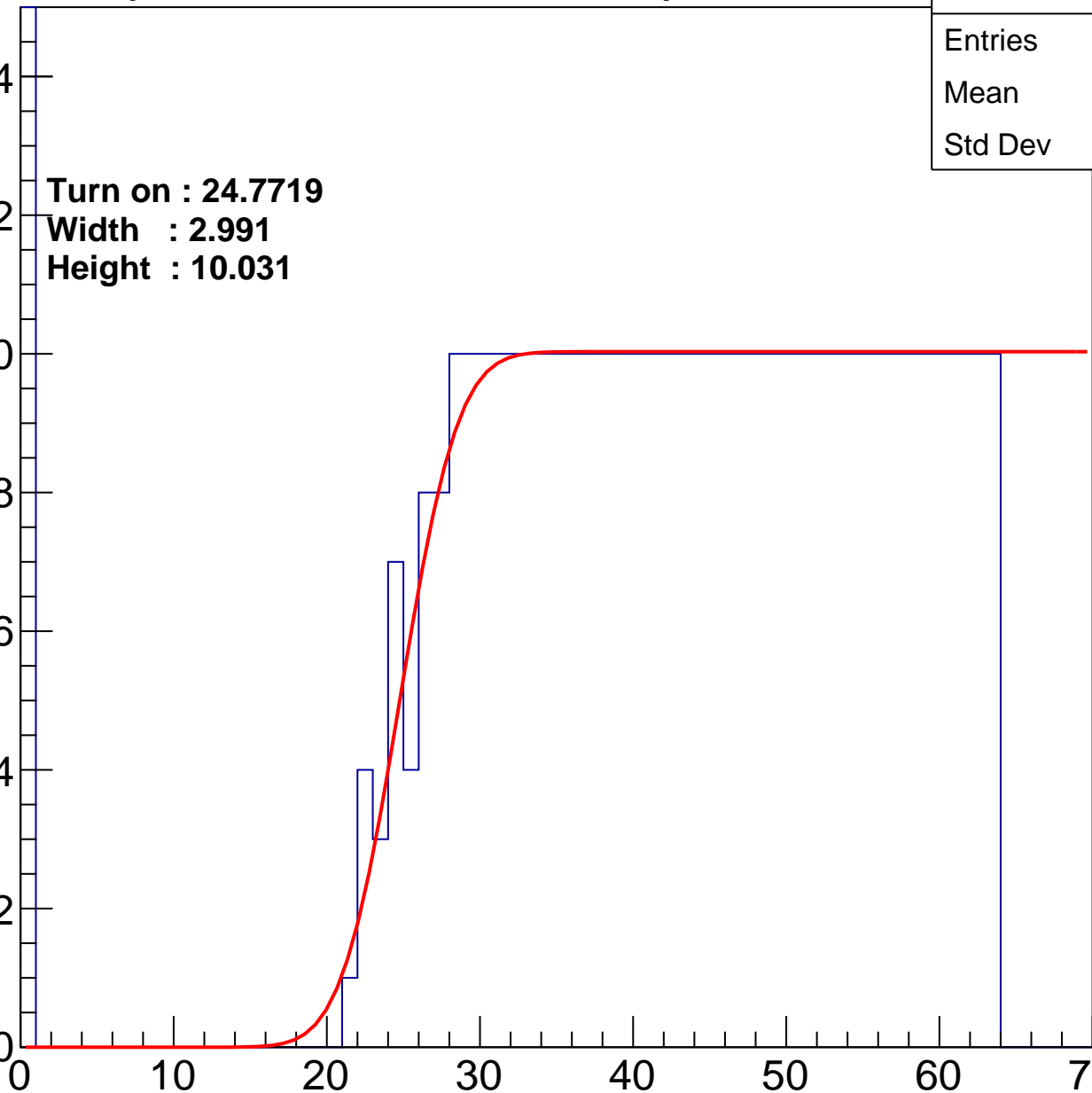
Width : 2.991

Height : 10.031

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U11-ch101

calib_packv5_041523_1651.root, FC#0, port C2

Entries	422
Mean	39.77
Std Dev	17.3

Turn on : 26.7290

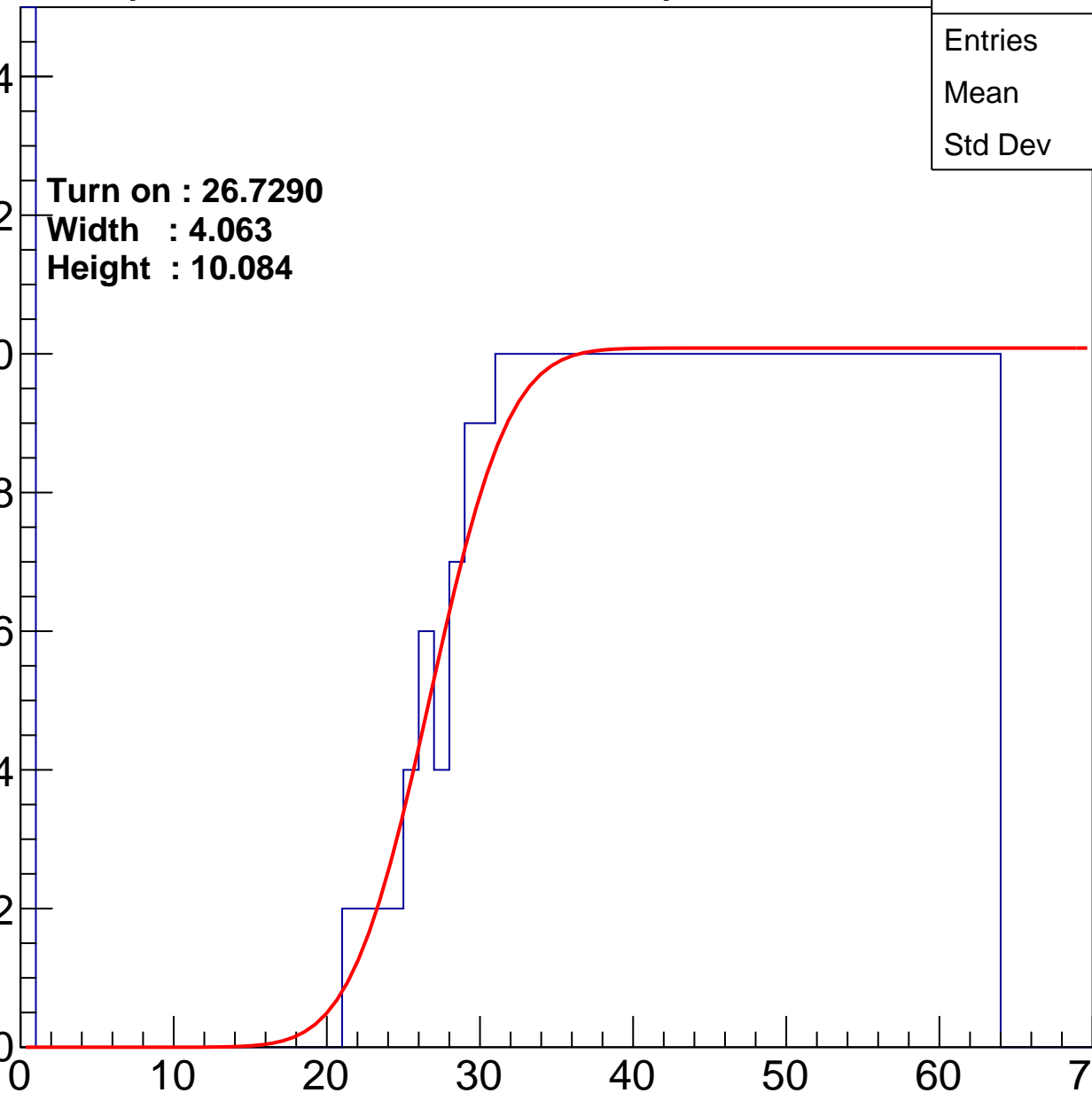
Width : 4.063

Height : 10.084

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U11-ch102

calib_packv5_041523_1651.root, FC#0, port C2

Entries	423
Mean	40.2
Std Dev	16.58

Turn on : 26.2910

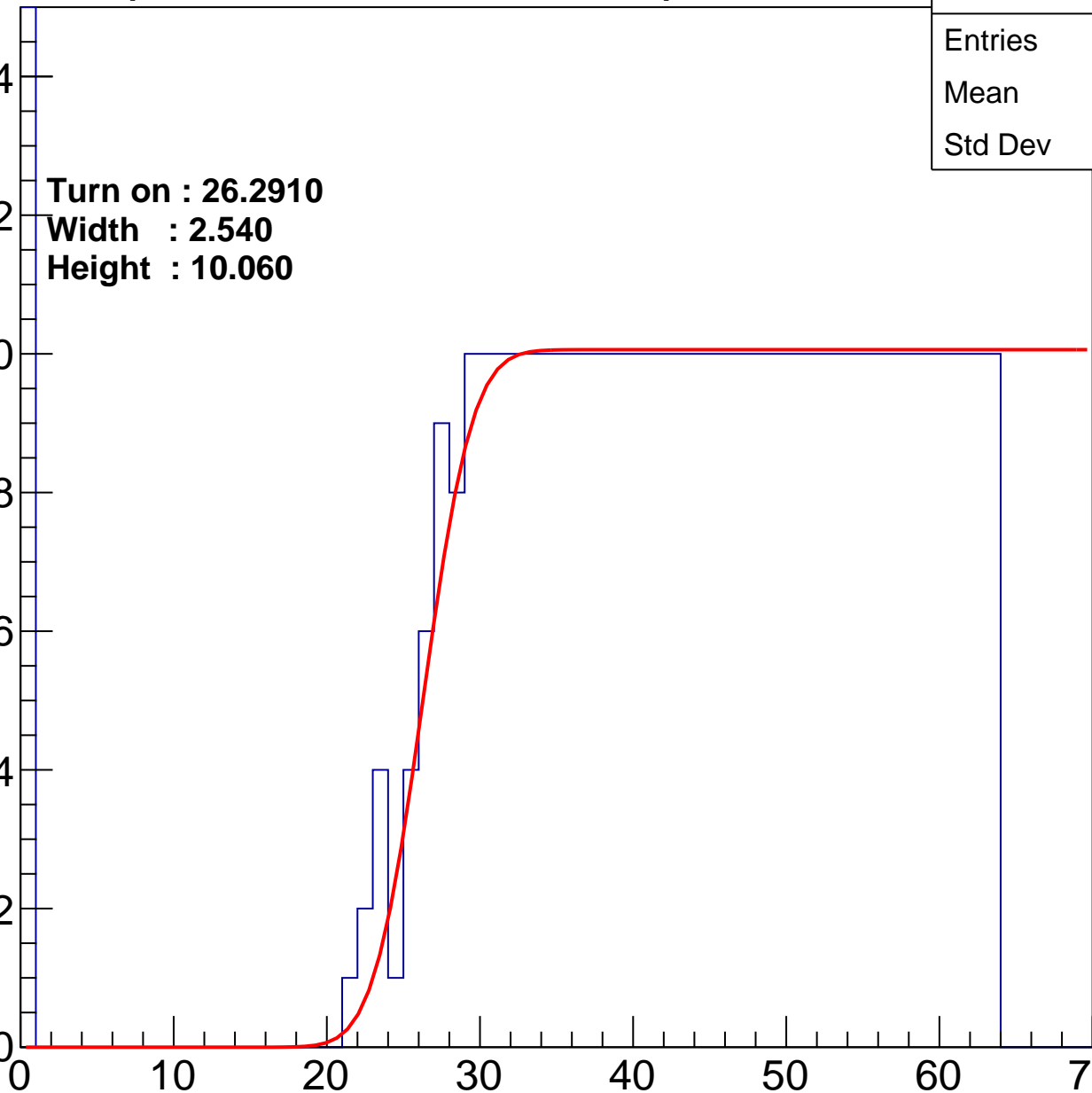
Width : 2.540

Height : 10.060

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U11-ch103

calib_packv5_041523_1651.root, FC#0, port C2

Entries	414
Mean	39.78
Std Dev	17.73

Turn on : 27.6369

Width : 3.062

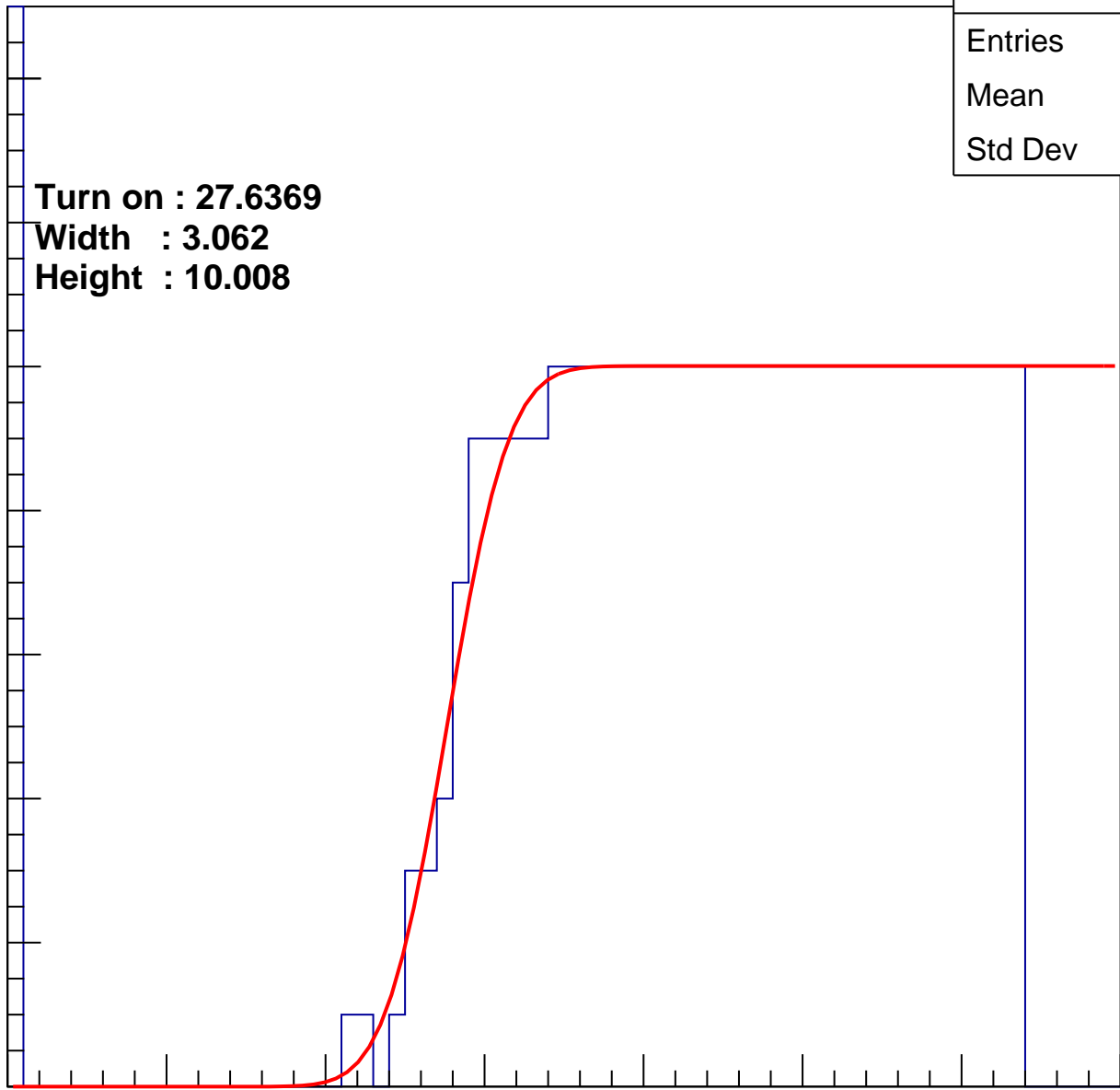
Height : 10.008

Entry

14
12
10
8
6
4
2
0

ampl

0 10 20 30 40 50 60 70



B1L103S, U11-ch104

calib_packv5_041523_1651.root, FC#0, port C2

Entries	413
Mean	40.46
Std Dev	16.74

Turn on : 26.9288

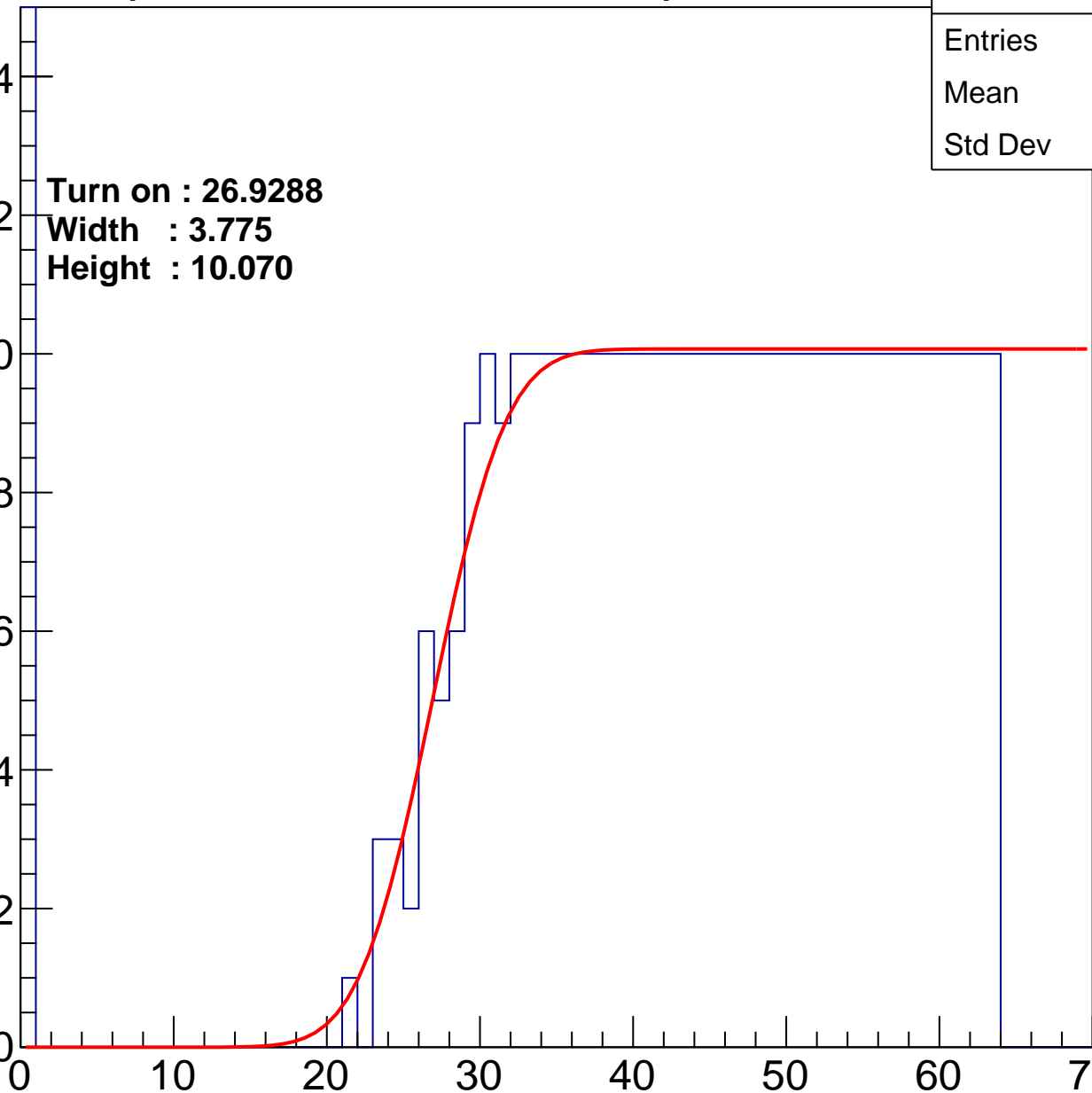
Width : 3.775

Height : 10.070

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U11-ch105

calib_packv5_041523_1651.root, FC#0, port C2

Entries	456
Mean	37.91
Std Dev	18.21

Turn on : 24.5208

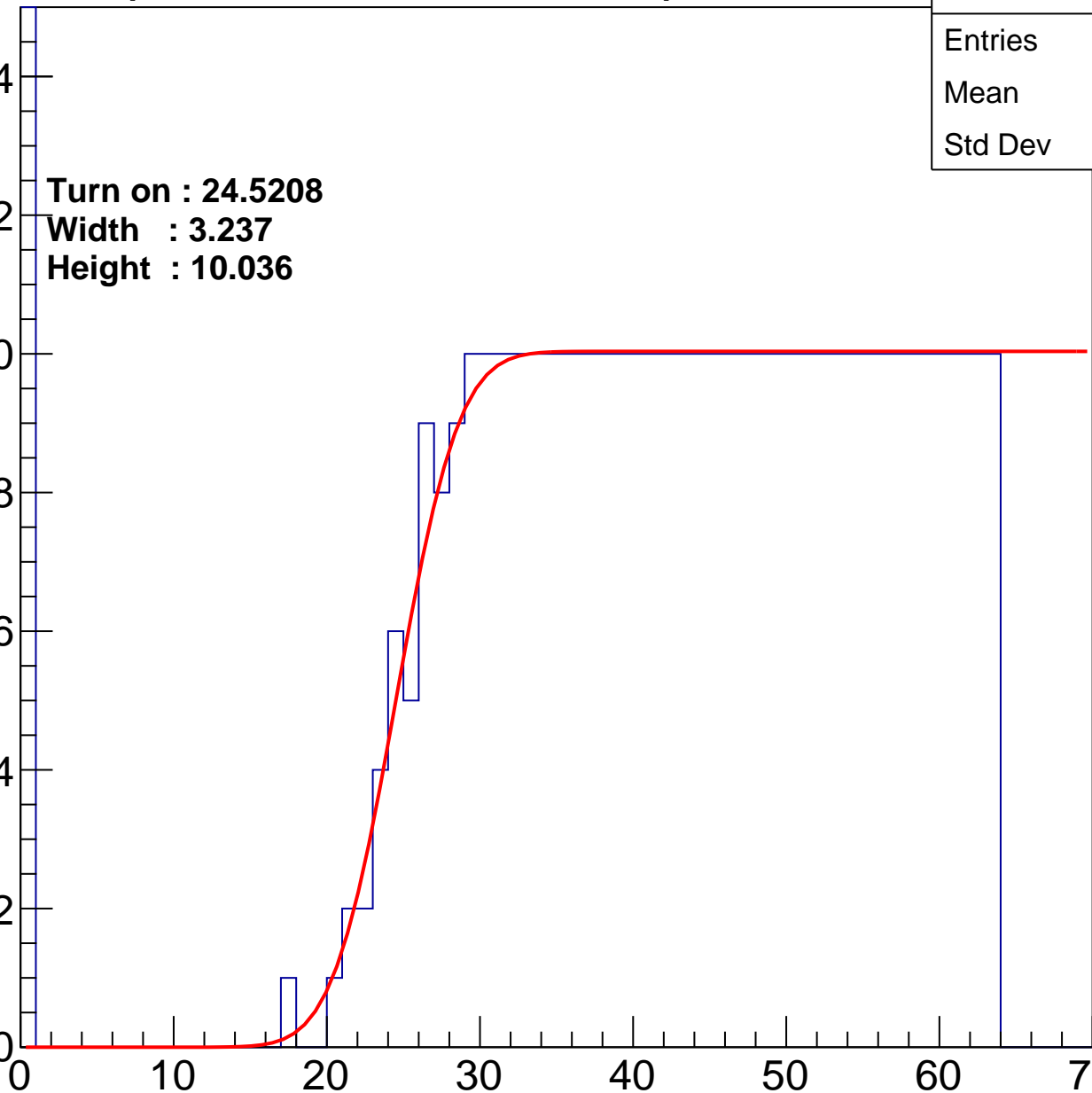
Width : 3.237

Height : 10.036

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U11-ch106

calib_packv5_041523_1651.root, FC#0, port C2

Entries	419
Mean	39.41
Std Dev	17.99

Turn on : 28.0042

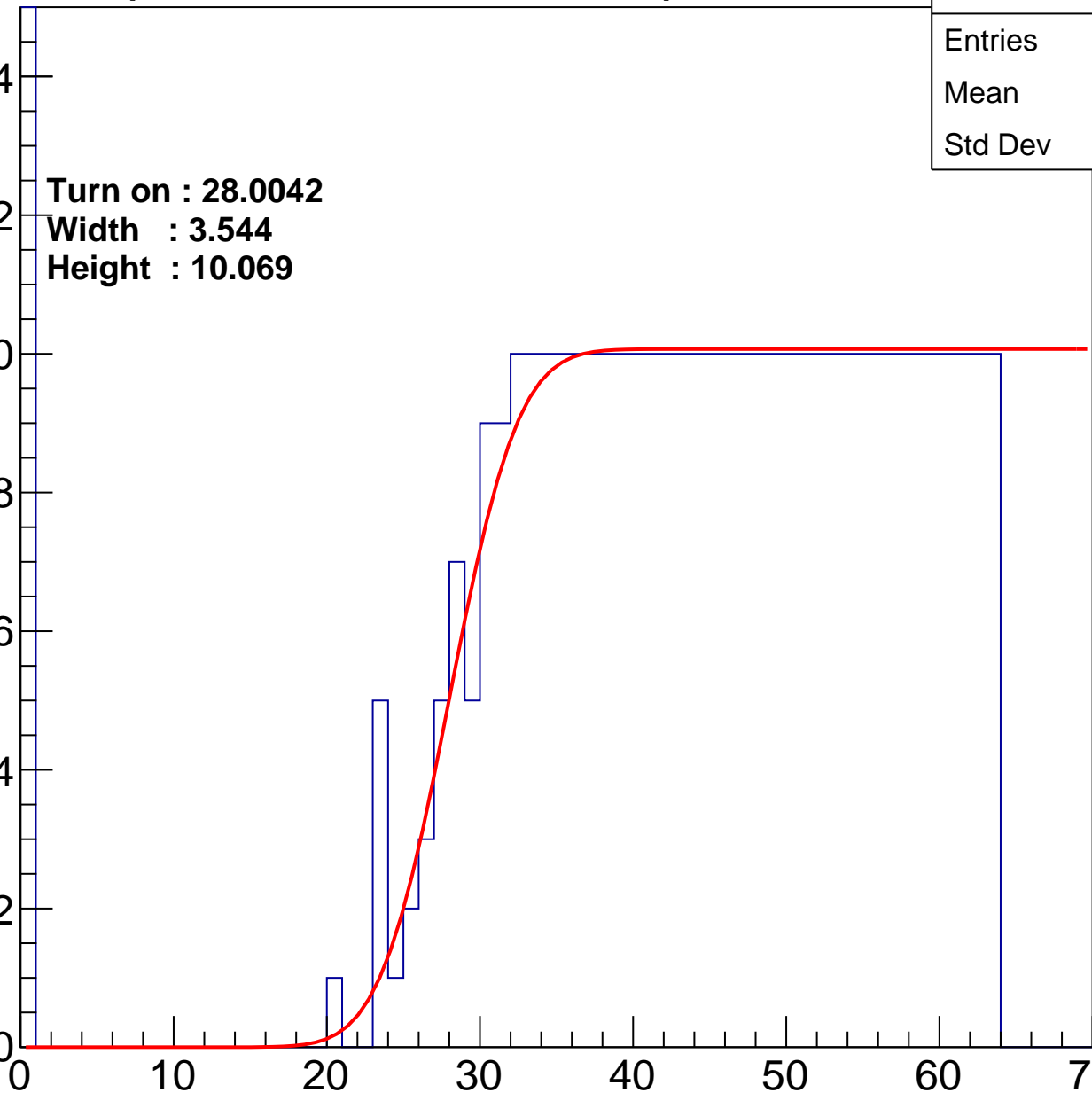
Width : 3.544

Height : 10.069

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U11-ch107

calib_packv5_041523_1651.root, FC#0, port C2

Entries	428
Mean	39.25
Std Dev	17.76

Turn on : 26.6763

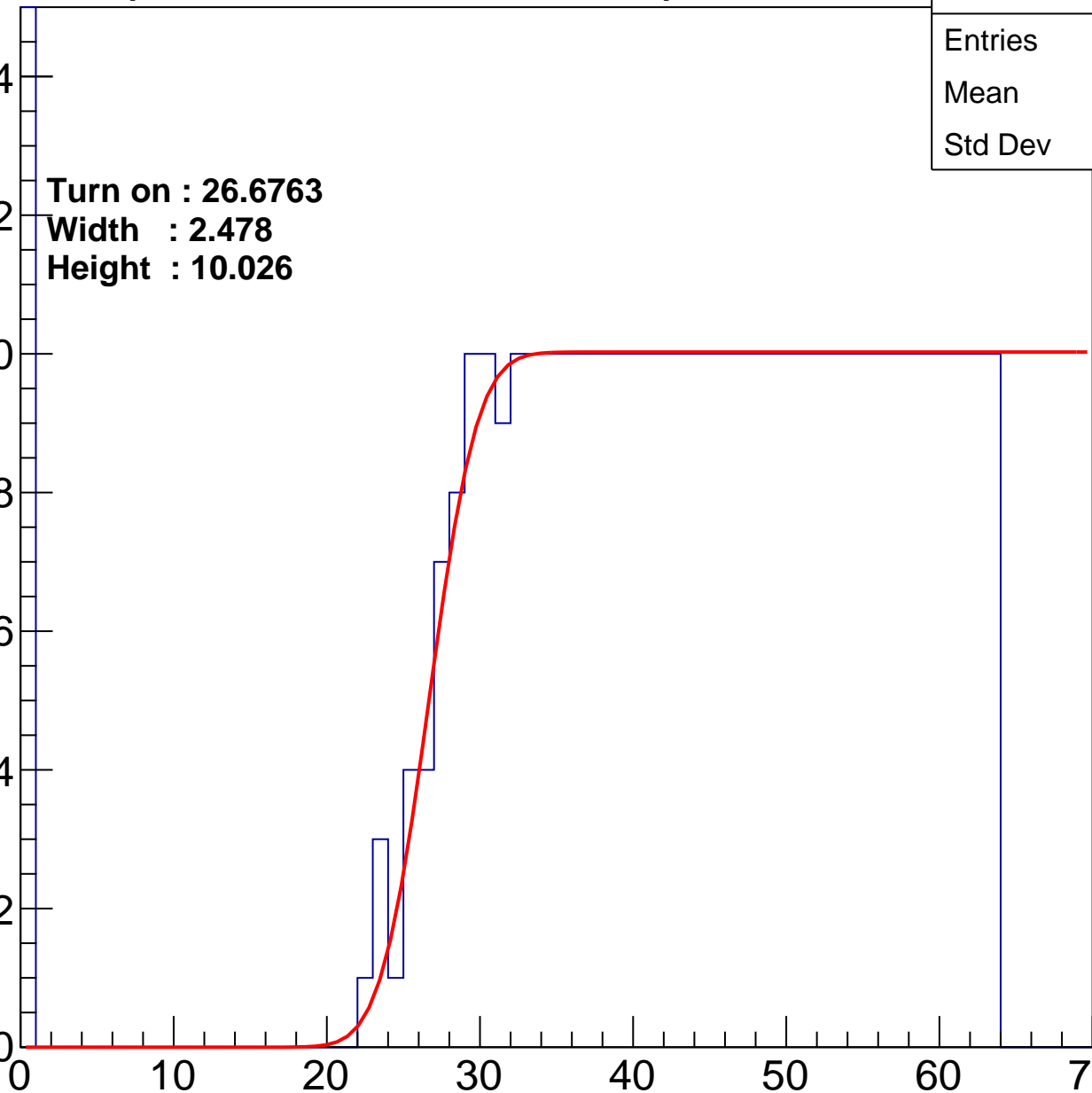
Width : 2.478

Height : 10.026

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U11-ch108

calib_packv5_041523_1651.root, FC#0, port C2

Entries	451
Mean	38.68
Std Dev	17.33

Turn on : 23.7174

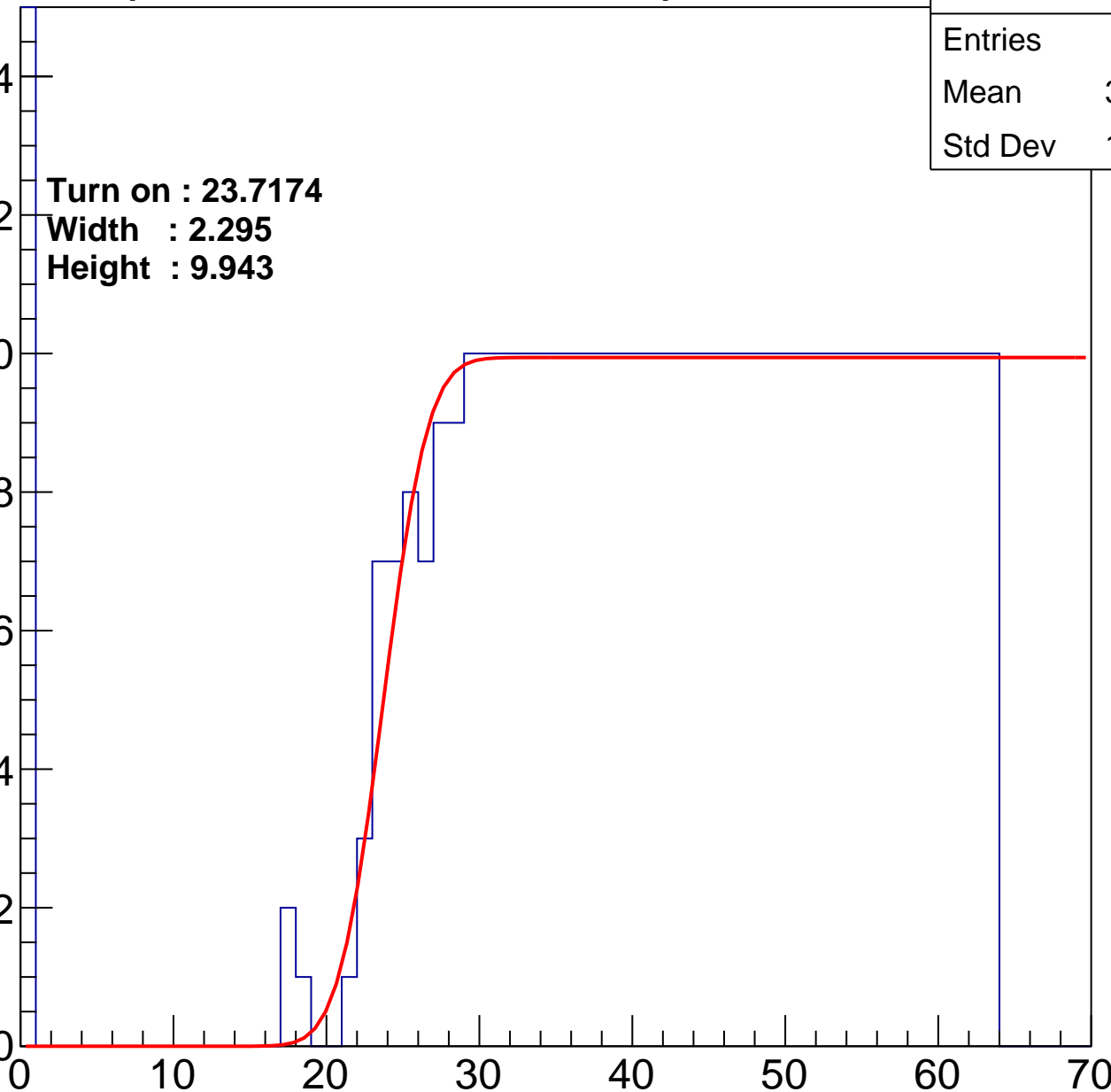
Width : 2.295

Height : 9.943

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U11-ch109

calib_packv5_041523_1651.root, FC#0, port C2

Entries	426
Mean	39.8
Std Dev	17

Turn on : 26.0915

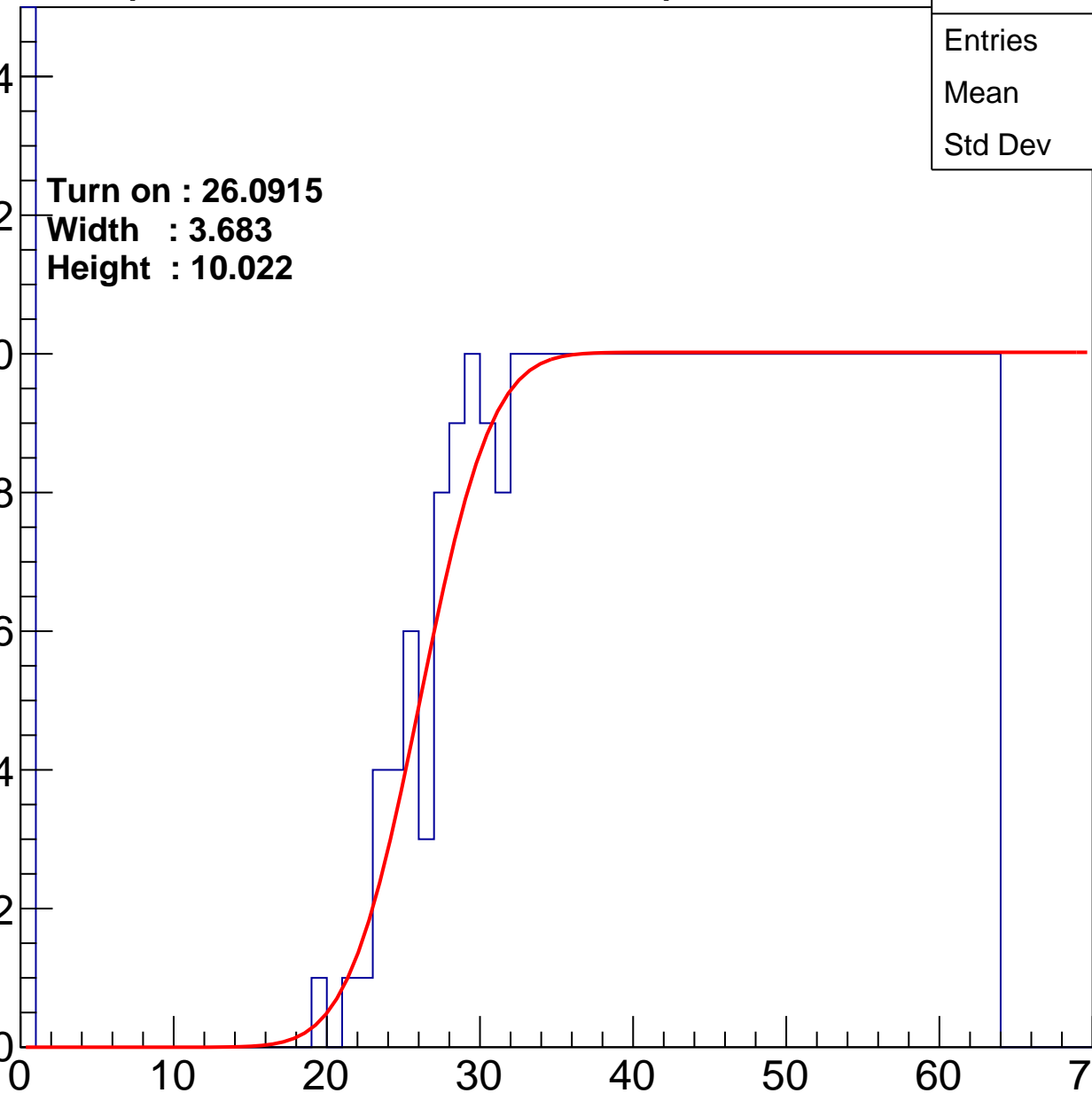
Width : 3.683

Height : 10.022

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U11-ch110

calib_packv5_041523_1651.root, FC#0, port C2

Entries	428
Mean	39.44
Std Dev	17.49

Turn on : 26.3178

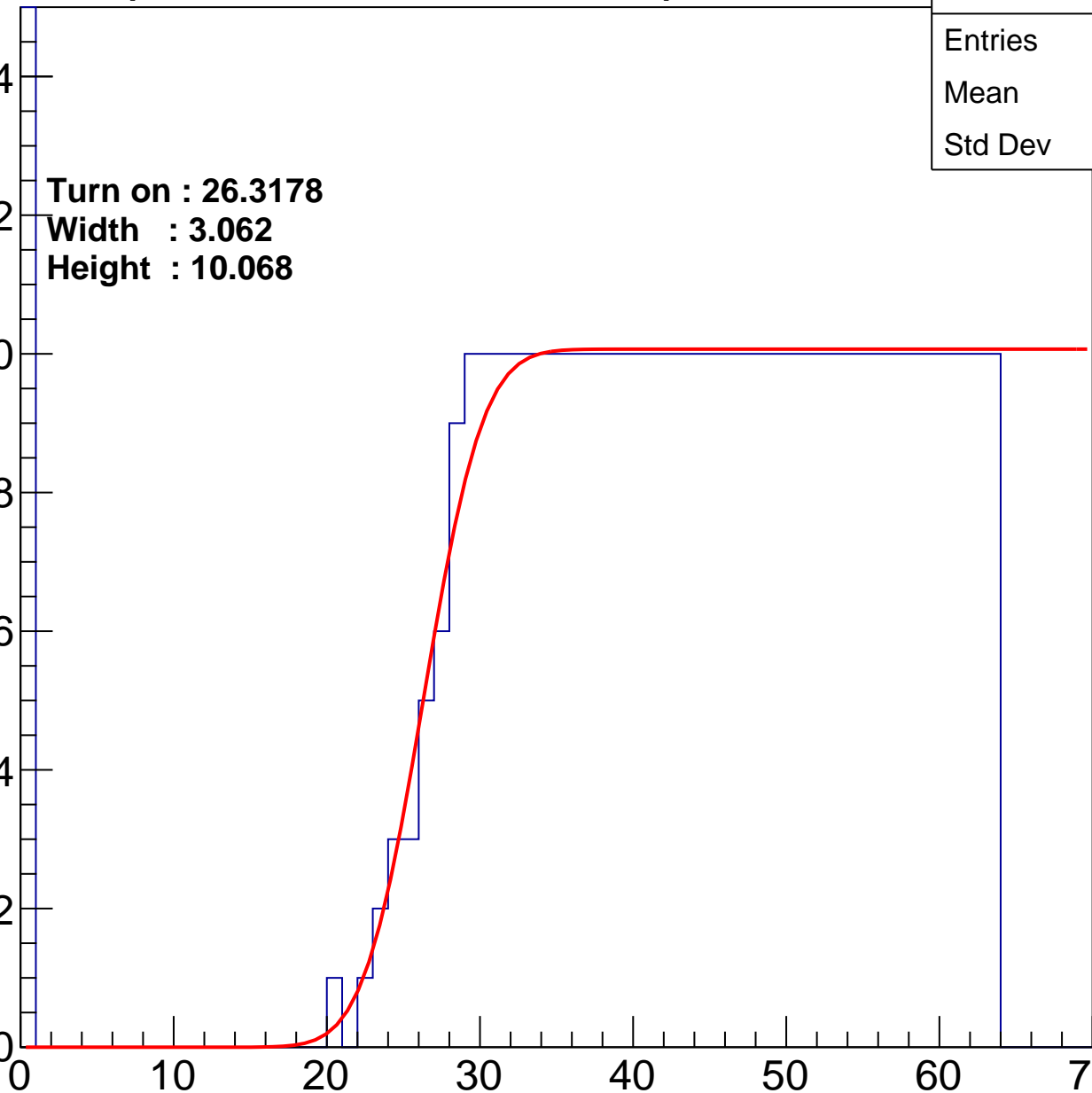
Width : 3.062

Height : 10.068

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U11-ch111

calib_packv5_041523_1651.root, FC#0, port C2

Entries	396
Mean	40.99
Std Dev	16.94

Turn on : 29.0806

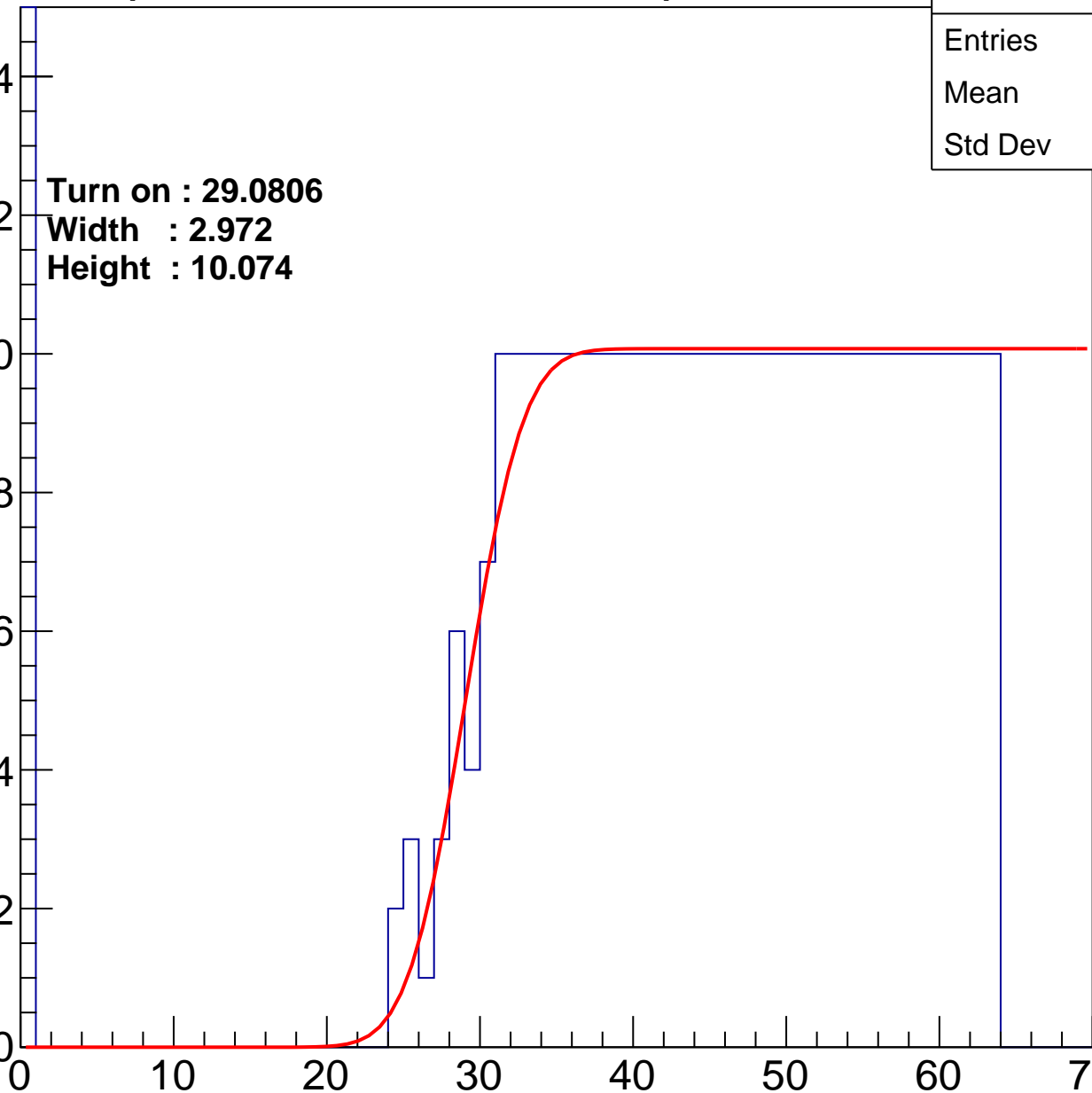
Width : 2.972

Height : 10.074

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U11-ch112

calib_packv5_041523_1651.root, FC#0, port C2

Entries	437
Mean	38.66
Std Dev	18.09

Turn on : 26.2983

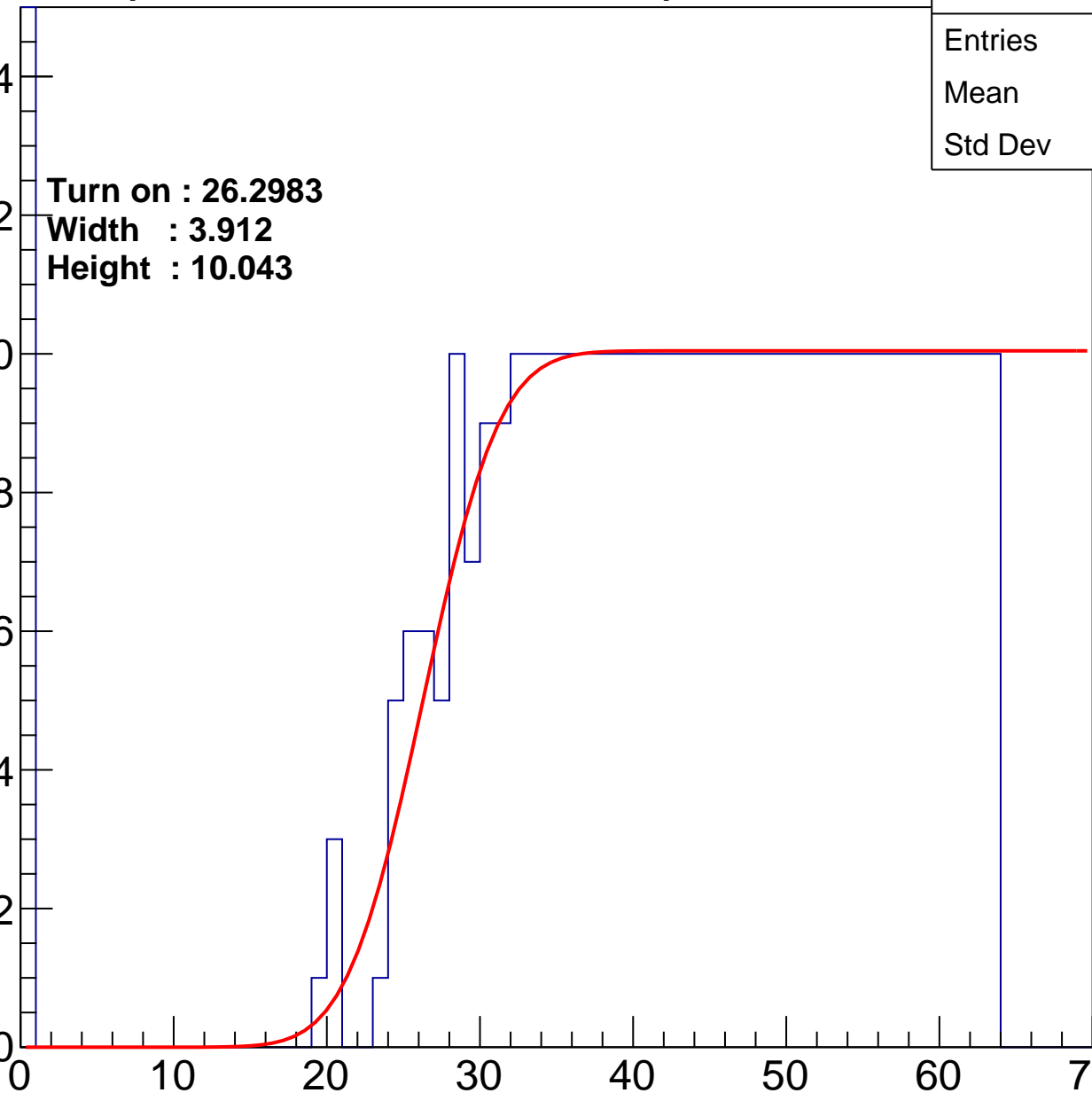
Width : 3.912

Height : 10.043

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U11-ch113

calib_packv5_041523_1651.root, FC#0, port C2

Entries	440
Mean	39.09
Std Dev	17.31

Turn on : 24.9323

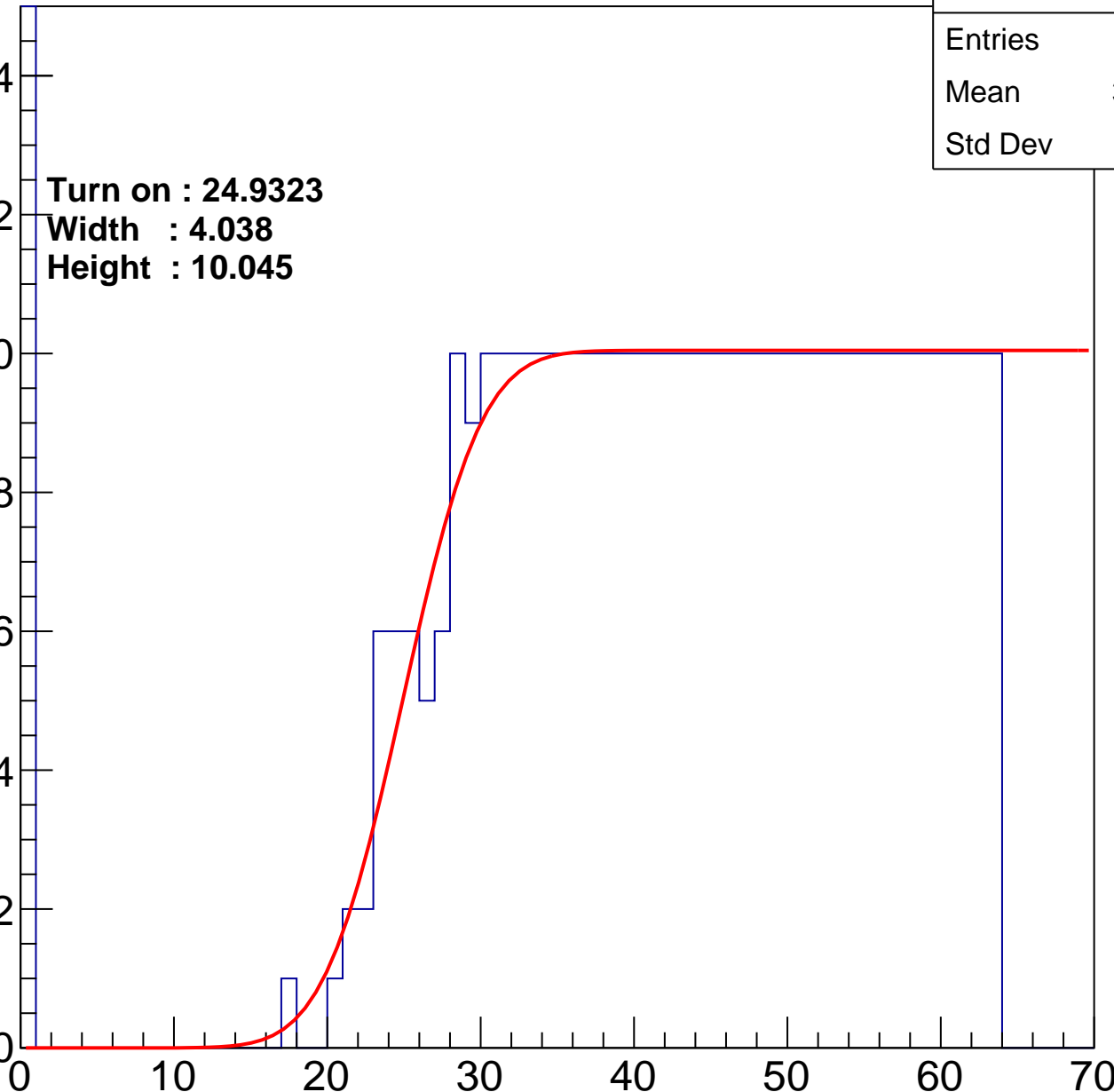
Width : 4.038

Height : 10.045

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U11-ch114

calib_packv5_041523_1651.root, FC#0, port C2

Entries	432
Mean	39.77
Std Dev	16.65

Turn on : 24.8378

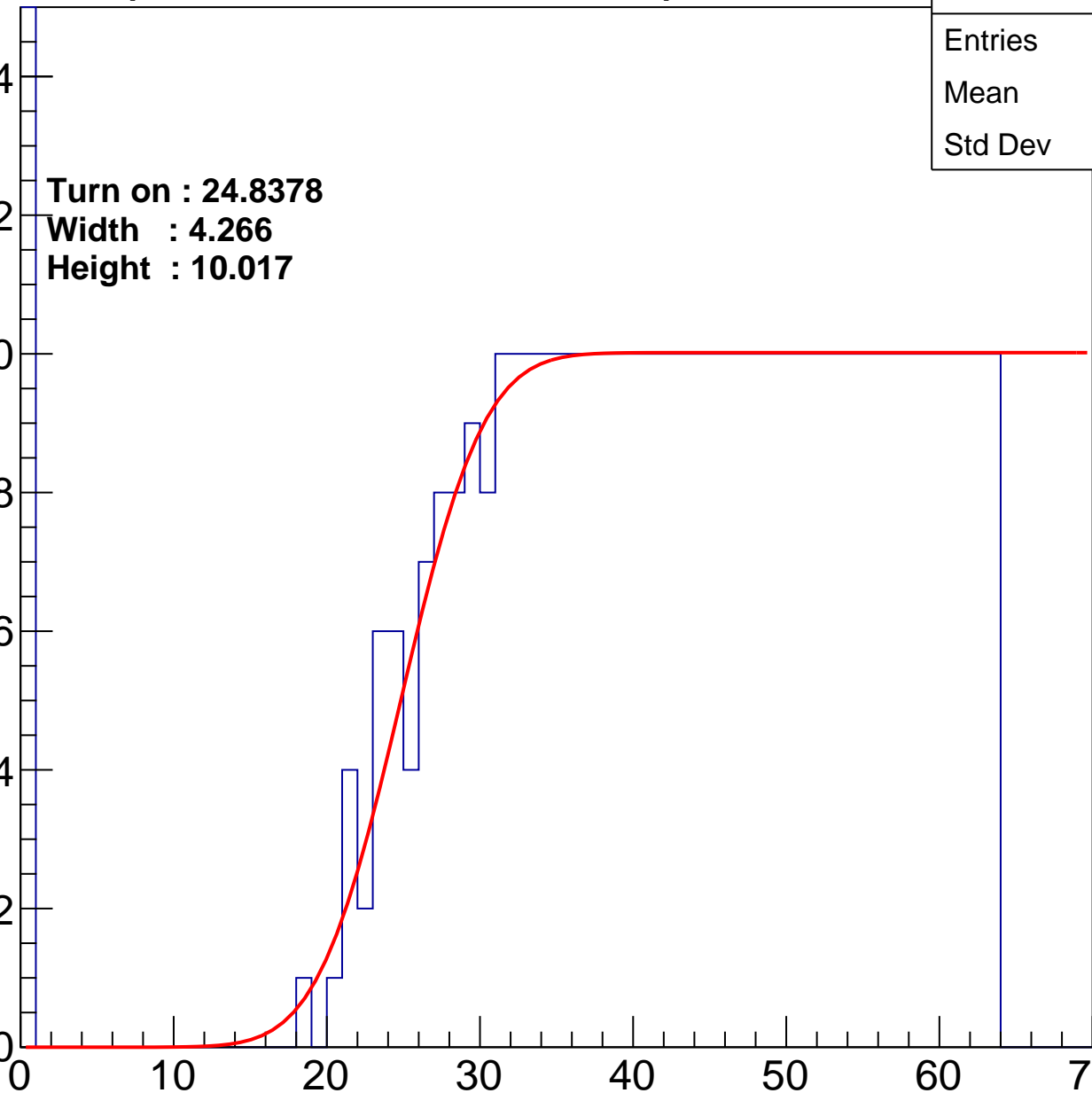
Width : 4.266

Height : 10.017

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U11-ch115

calib_packv5_041523_1651.root, FC#0, port C2

Entries	437
Mean	39.26
Std Dev	17.21

Turn on : 24.7490

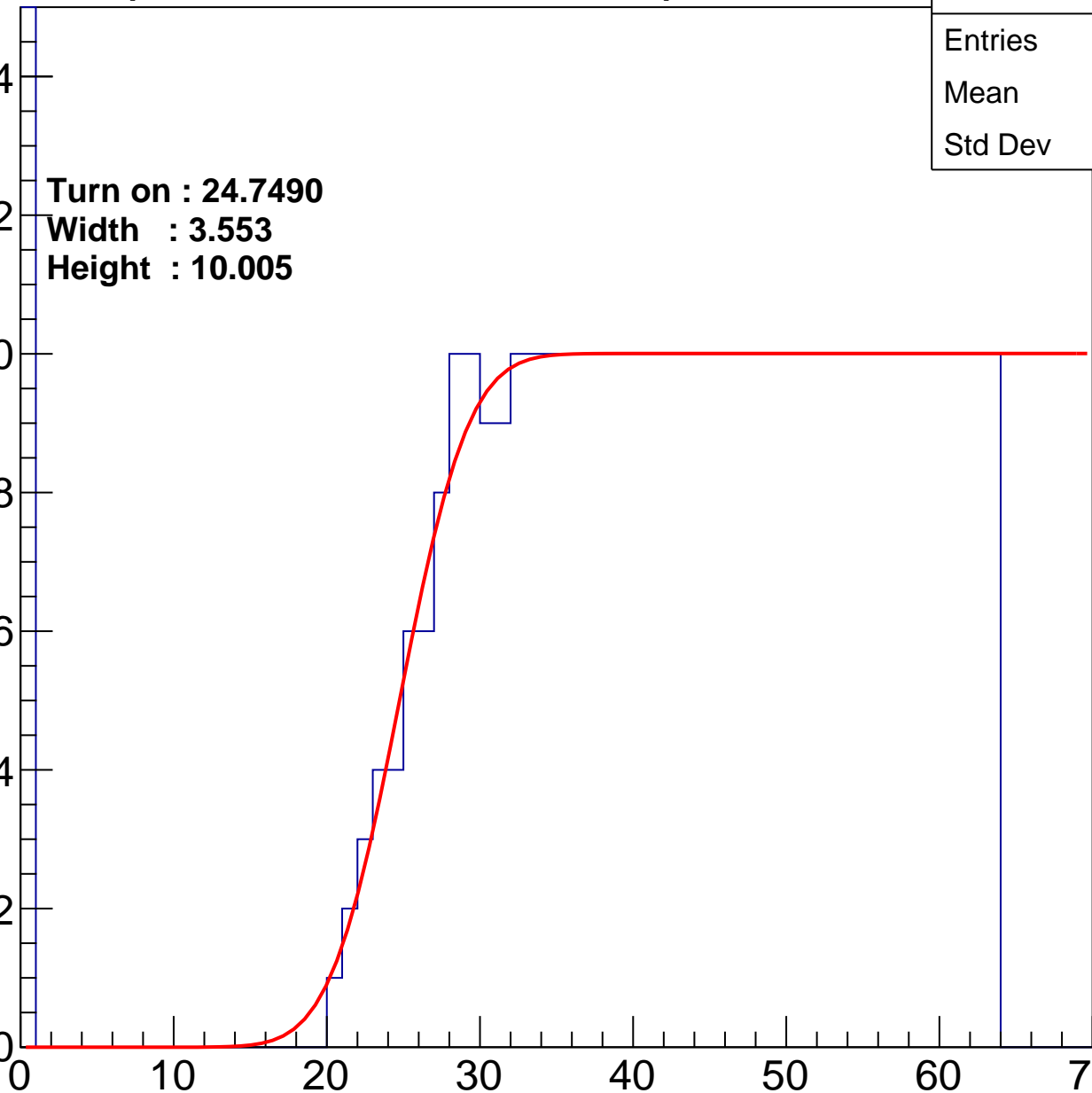
Width : 3.553

Height : 10.005

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U11-ch116

calib_packv5_041523_1651.root, FC#0, port C2

Entries	454
Mean	37.79
Std Dev	18.46

Turn on : 24.9558

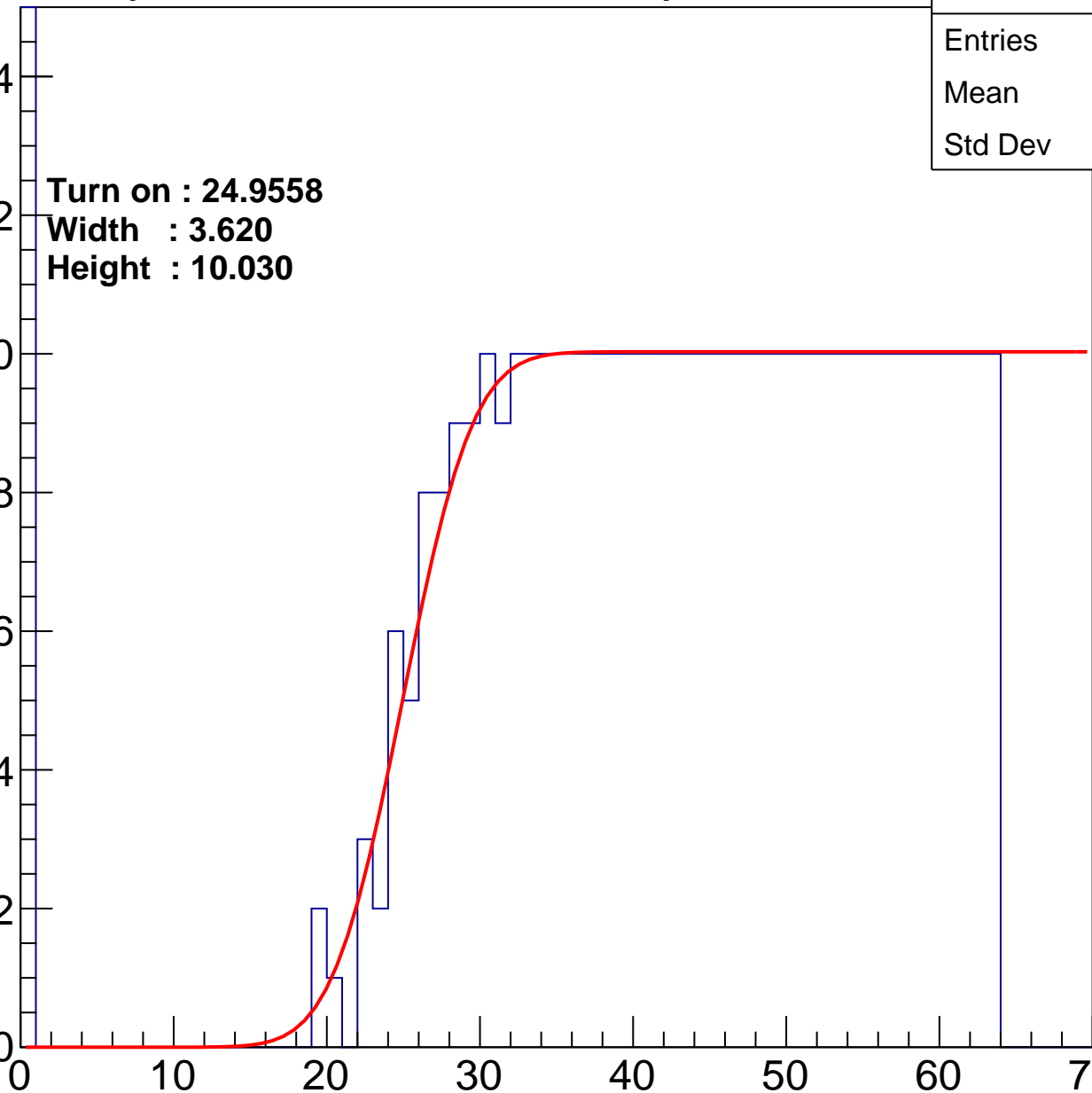
Width : 3.620

Height : 10.030

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U11-ch117

calib_packv5_041523_1651.root, FC#0, port C2

Entries	459
Mean	37.29
Std Dev	18.9

Turn on : 25.0307

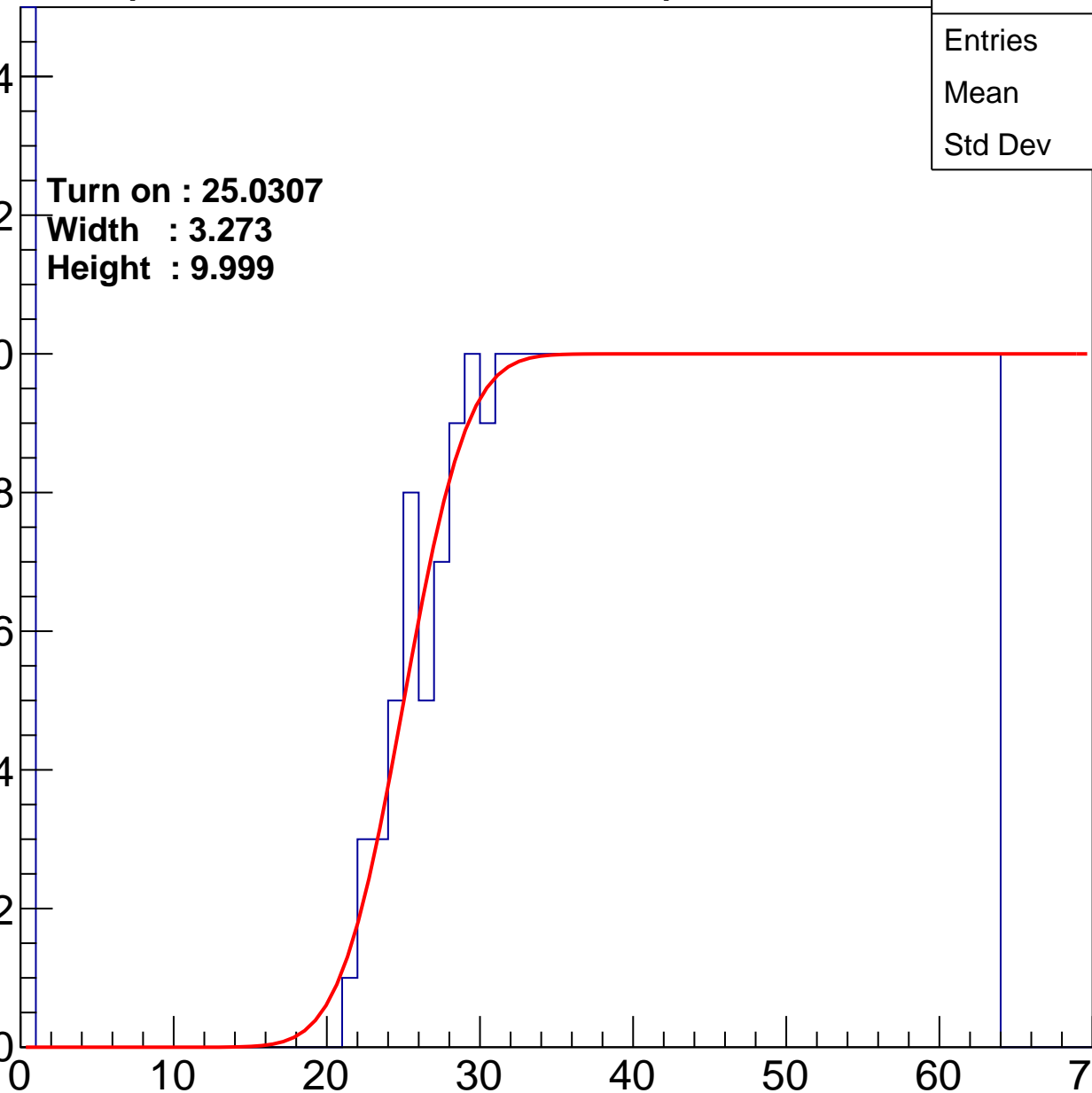
Width : 3.273

Height : 9.999

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U11-ch118

calib_packv5_041523_1651.root, FC#0, port C2

Entries	423
Mean	40.01
Std Dev	16.88

Turn on : 25.9911

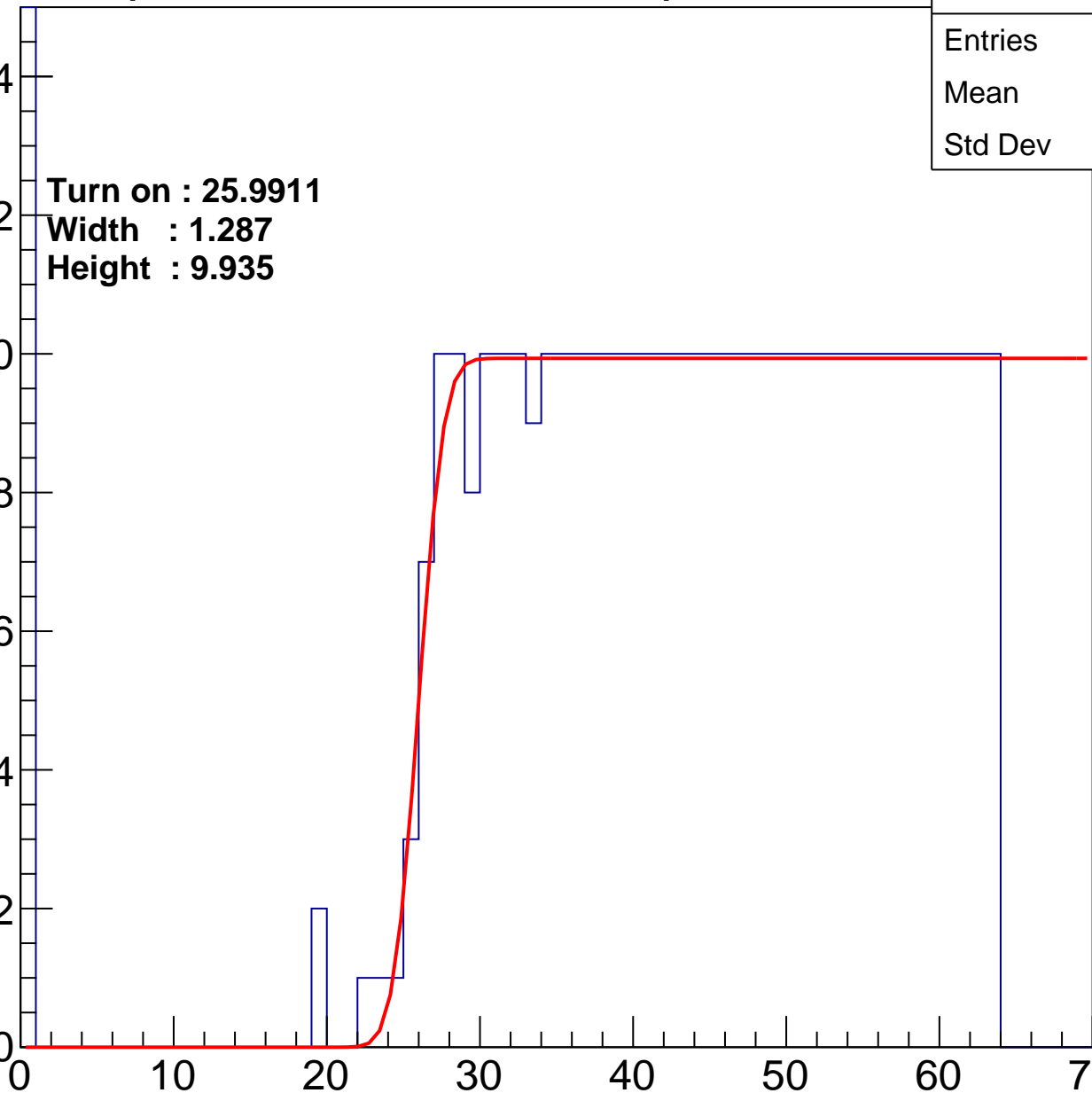
Width : 1.287

Height : 9.935

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U11-ch119

calib_packv5_041523_1651.root, FC#0, port C2

Entries	443
Mean	38.32
Std Dev	18.27

Turn on : 25.6327

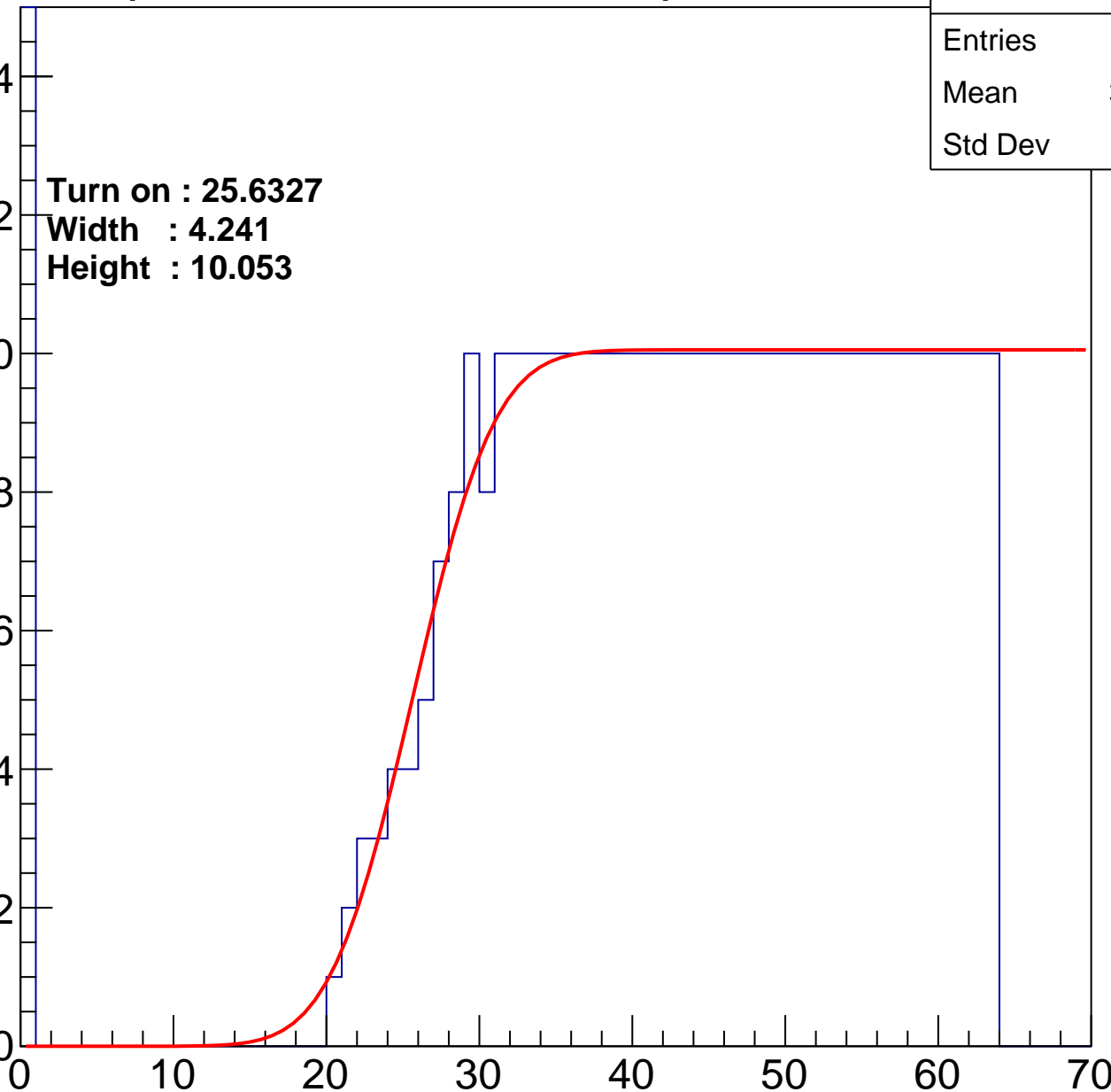
Width : 4.241

Height : 10.053

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U11-ch120

calib_packv5_041523_1651.root, FC#0, port C2

Entries	433
Mean	38.77
Std Dev	18.18

Turn on : 26.2598

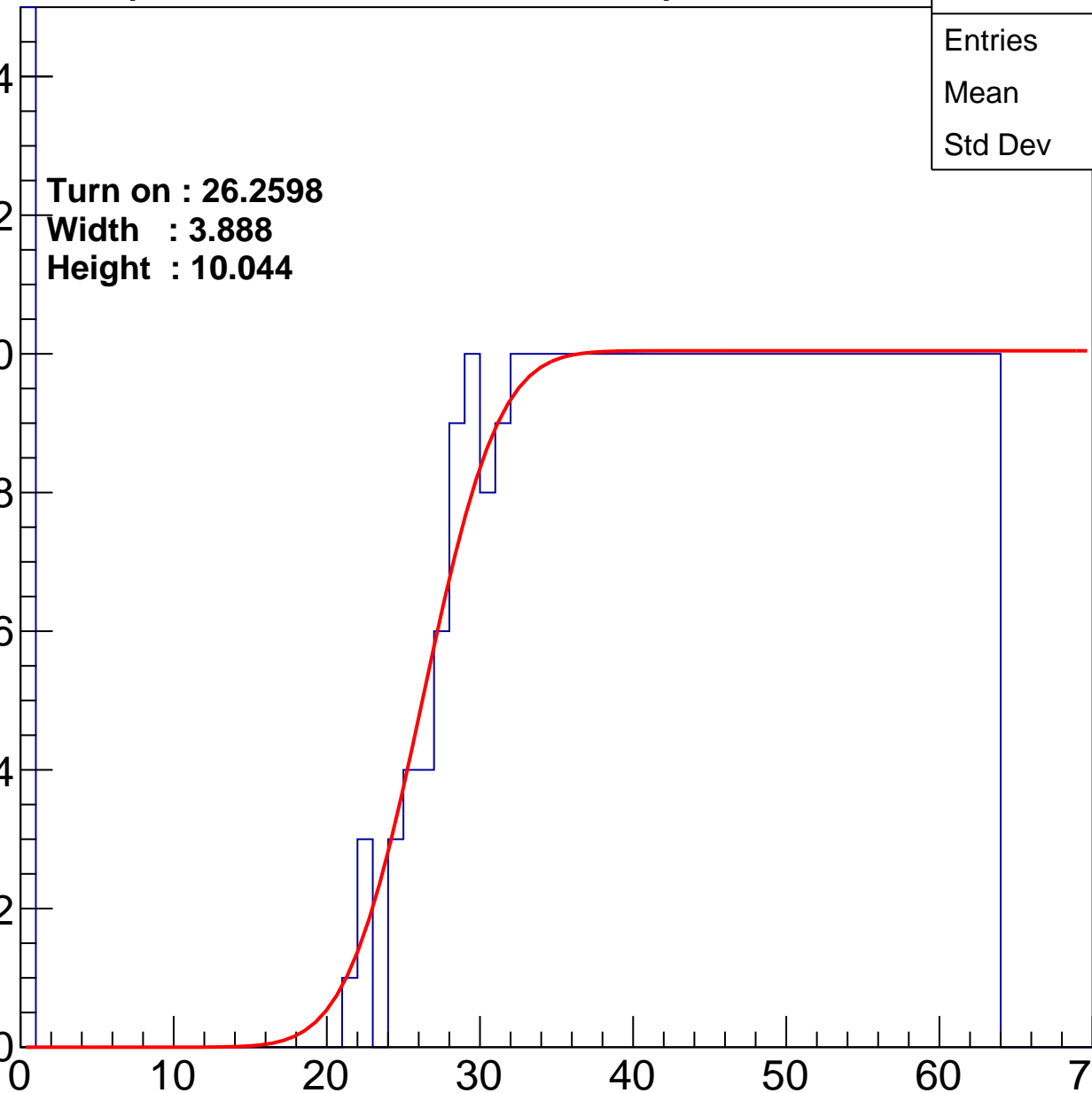
Width : 3.888

Height : 10.044

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U11-ch121

calib_packv5_041523_1651.root, FC#0, port C2

Entries	424
Mean	40.03
Std Dev	16.73

Turn on : 25.2643

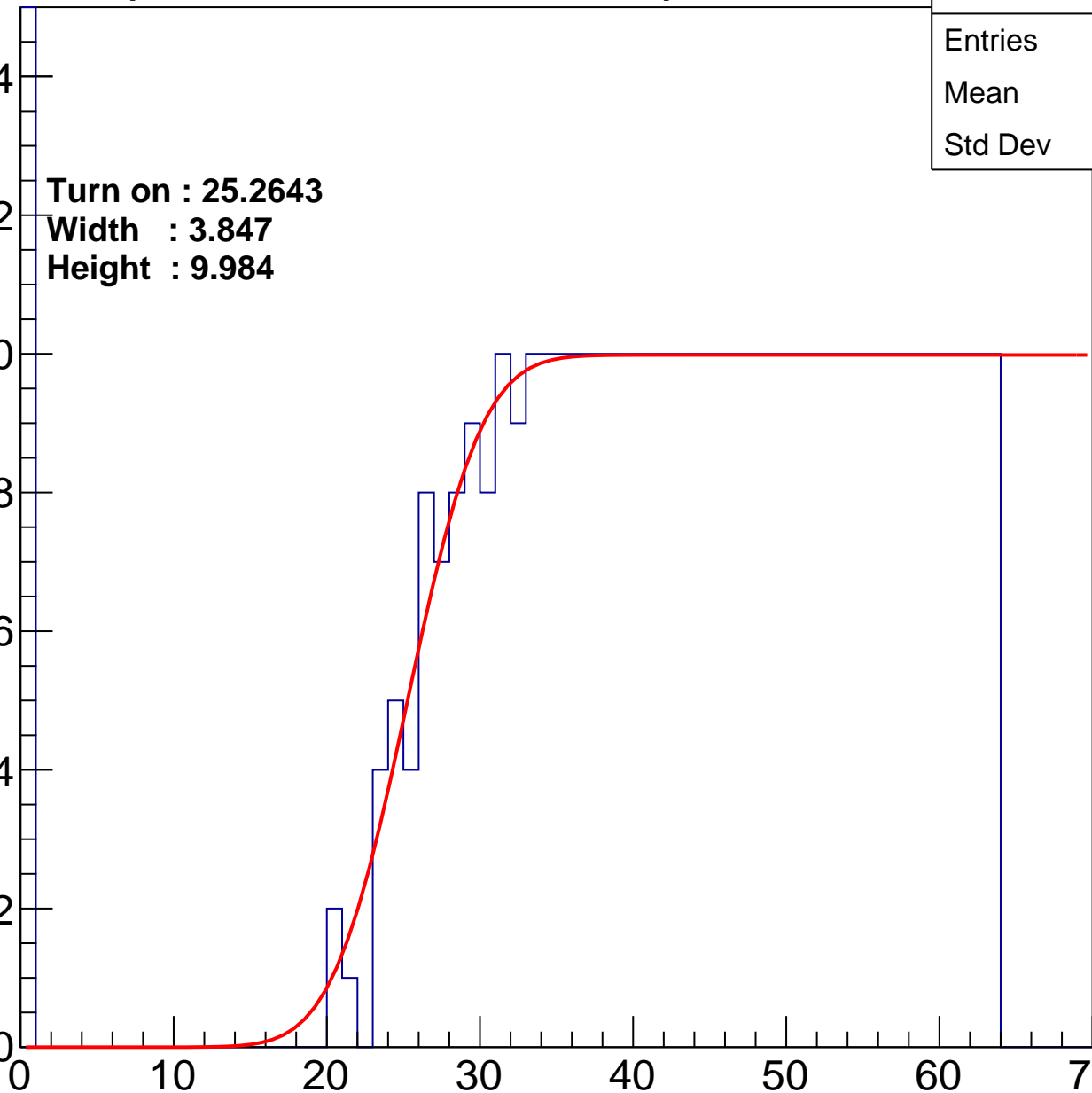
Width : 3.847

Height : 9.984

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U11-ch122

calib_packv5_041523_1651.root, FC#0, port C2

Entries	462
Mean	38.06
Std Dev	17.77

Turn on : 24.0934

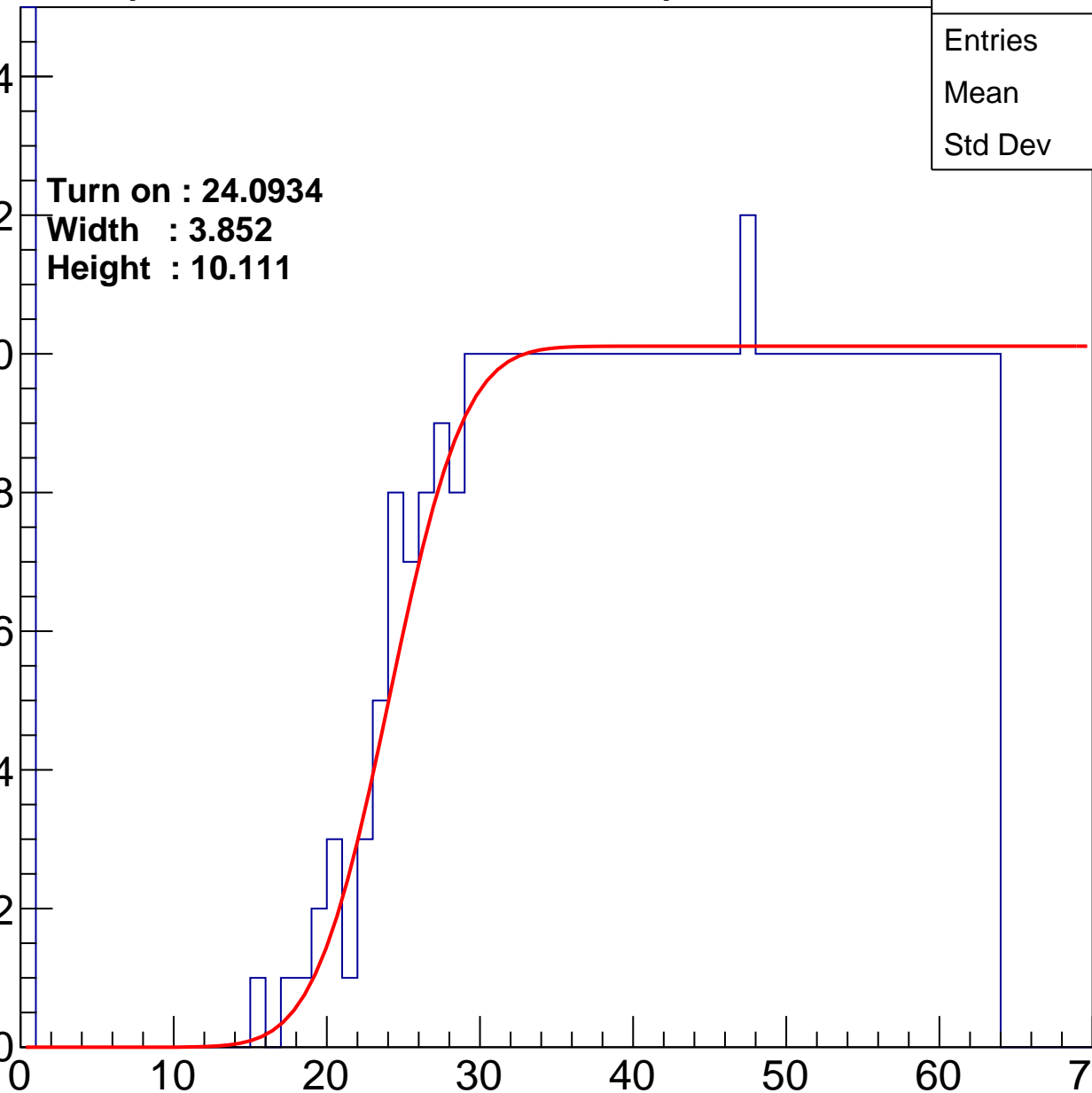
Width : 3.852

Height : 10.111

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U11-ch123

calib_packv5_041523_1651.root, FC#0, port C2

Entries	429
Mean	39.14
Std Dev	17.86

Turn on : 26.7496

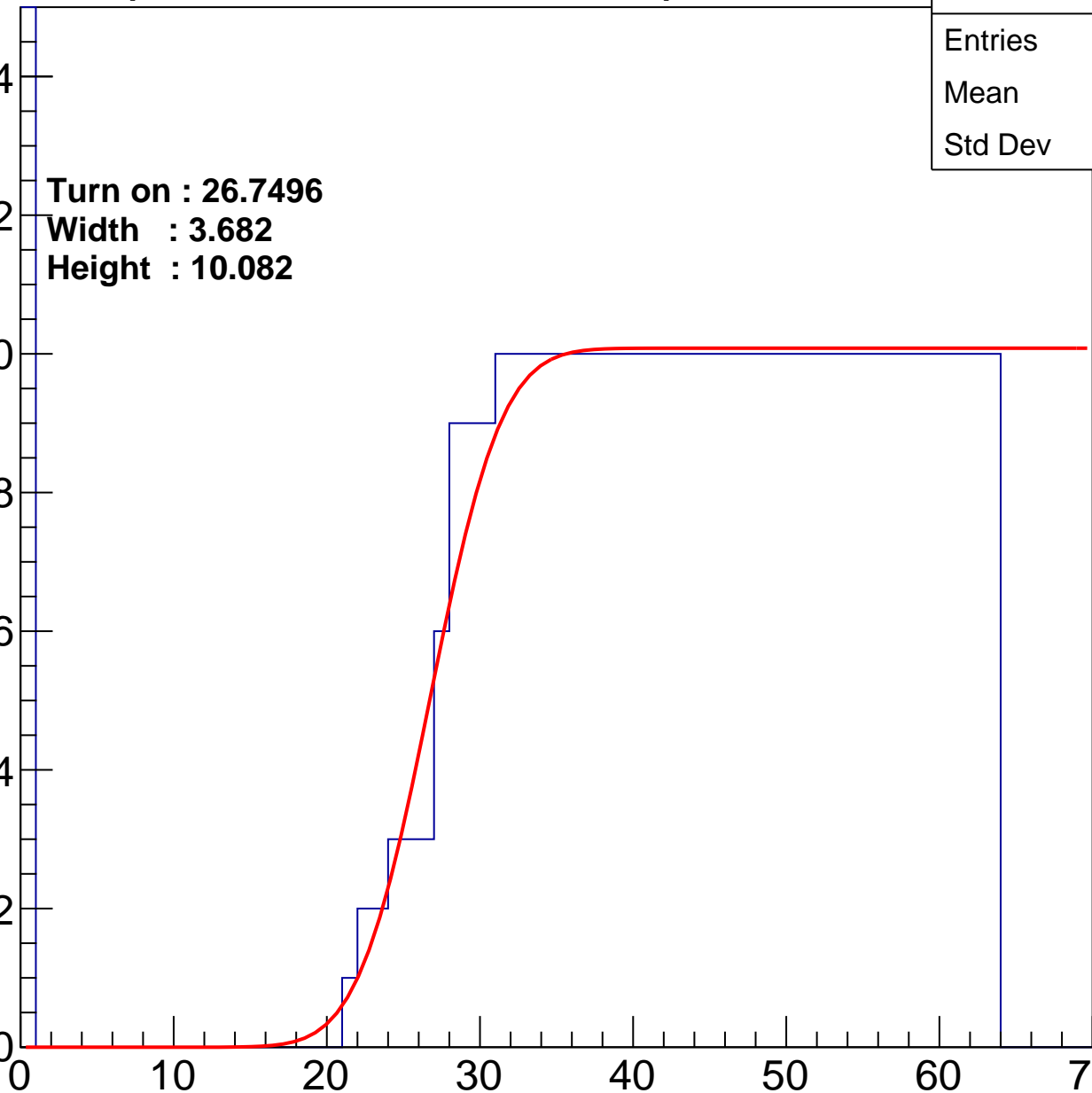
Width : 3.682

Height : 10.082

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U11-ch124

calib_packv5_041523_1651.root, FC#0, port C2

Entries	463
Mean	37.42
Std Dev	18.52

Turn on : 24.1554

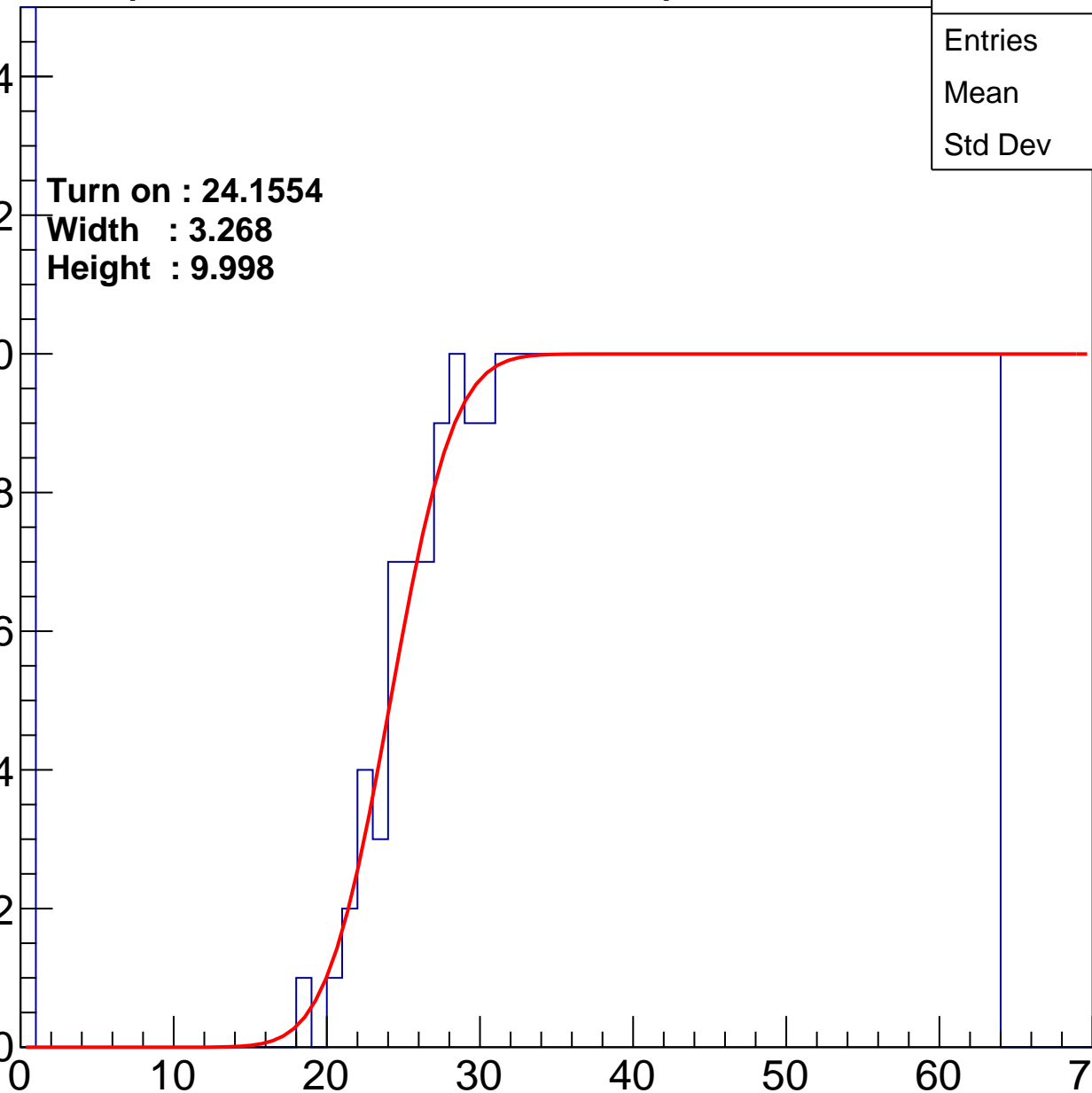
Width : 3.268

Height : 9.998

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U11-ch125

calib_packv5_041523_1651.root, FC#0, port C2

Entries	424
Mean	39.78
Std Dev	17.16

Turn on : 25.4992

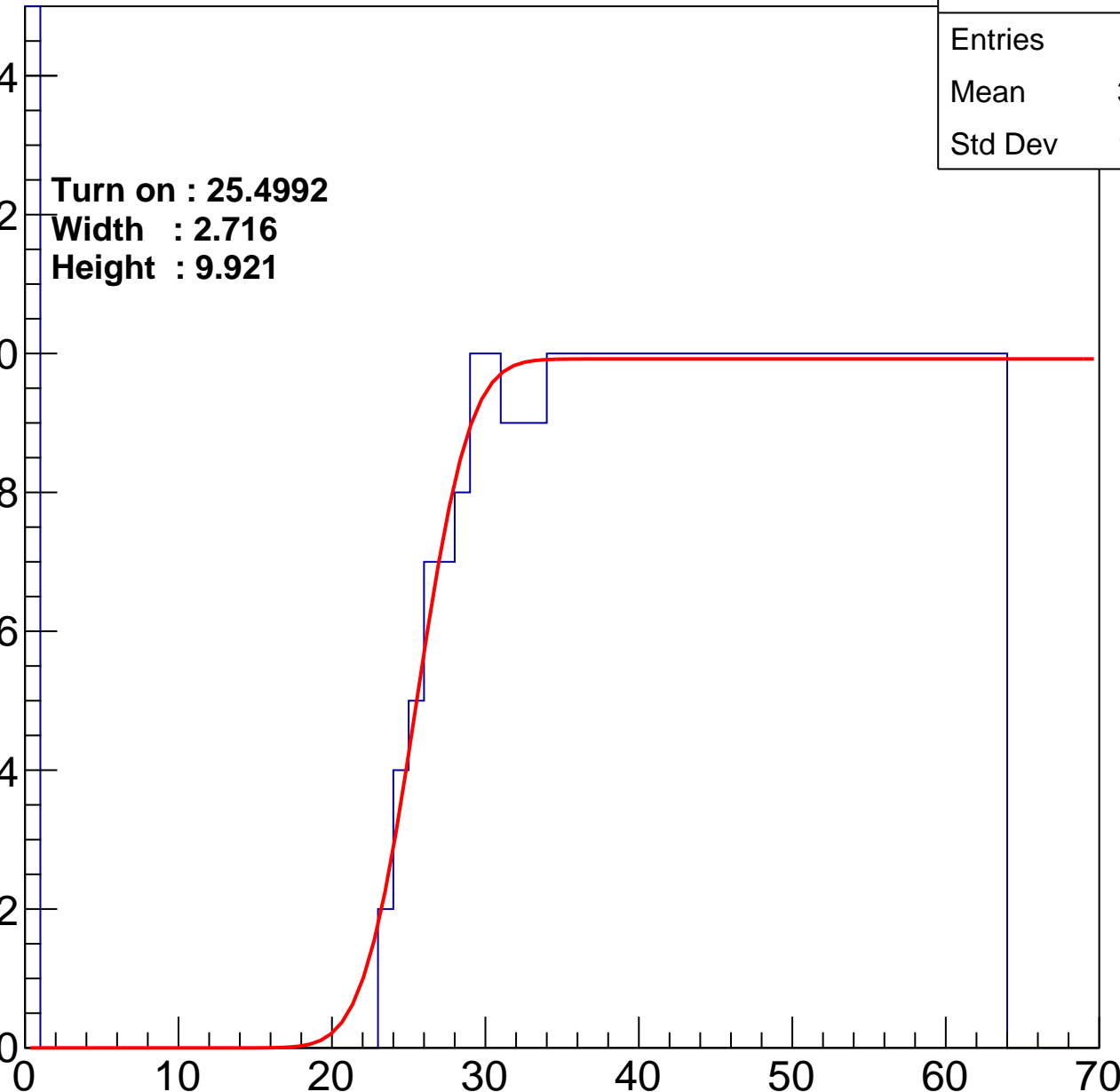
Width : 2.716

Height : 9.921

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U11-ch126

calib_packv5_041523_1651.root, FC#0, port C2

Entries	452
Mean	38.28
Std Dev	17.87

Turn on : 24.1793

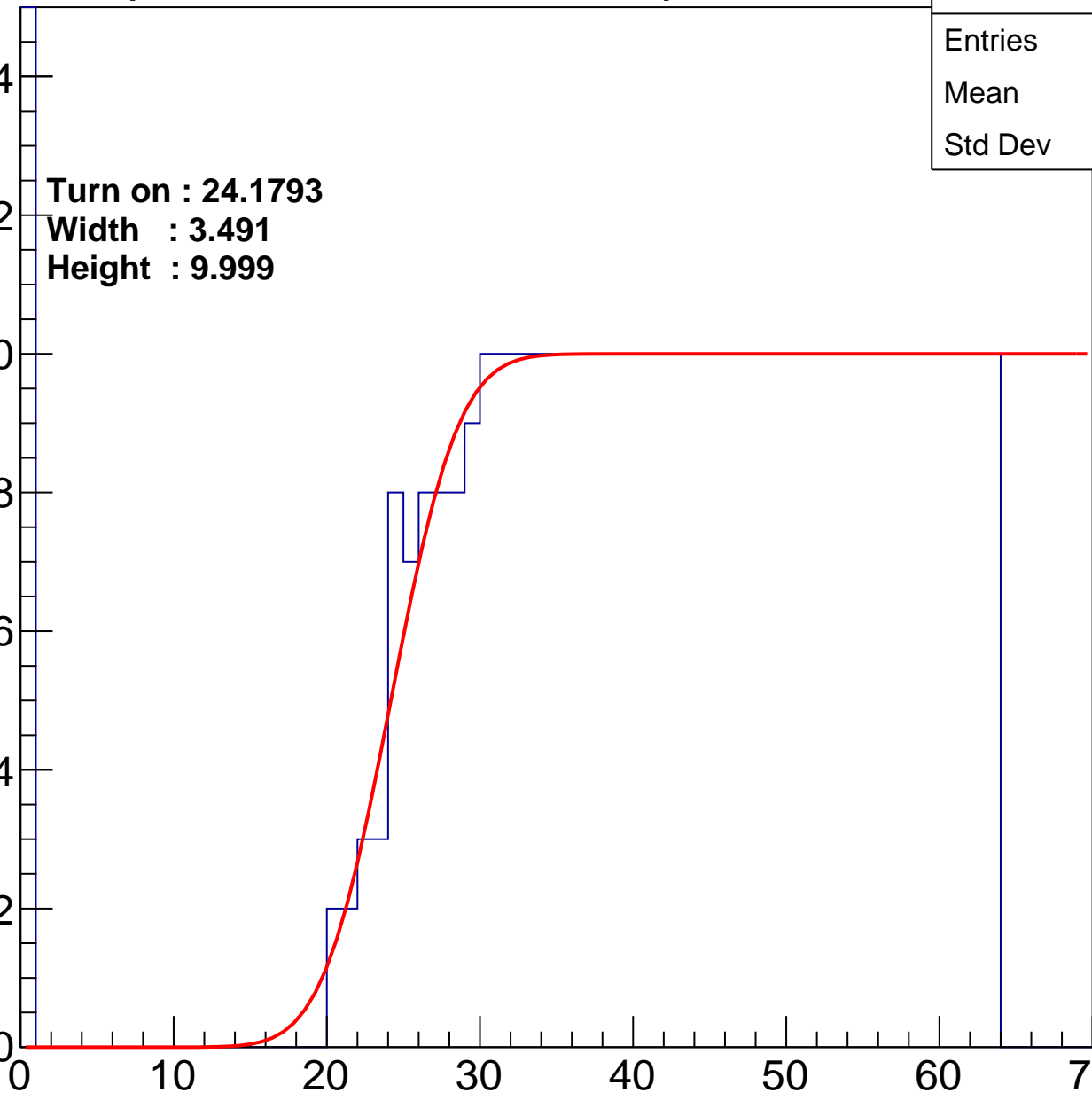
Width : 3.491

Height : 9.999

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U11-ch127

calib_packv5_041523_1651.root, FC#0, port C2

Entries	462
Mean	37.36
Std Dev	18.68

Turn on : 24.7867

Width : 3.817

Height : 10.072

Entry

14

12

10

8

6

4

2

0

0

10

20

30

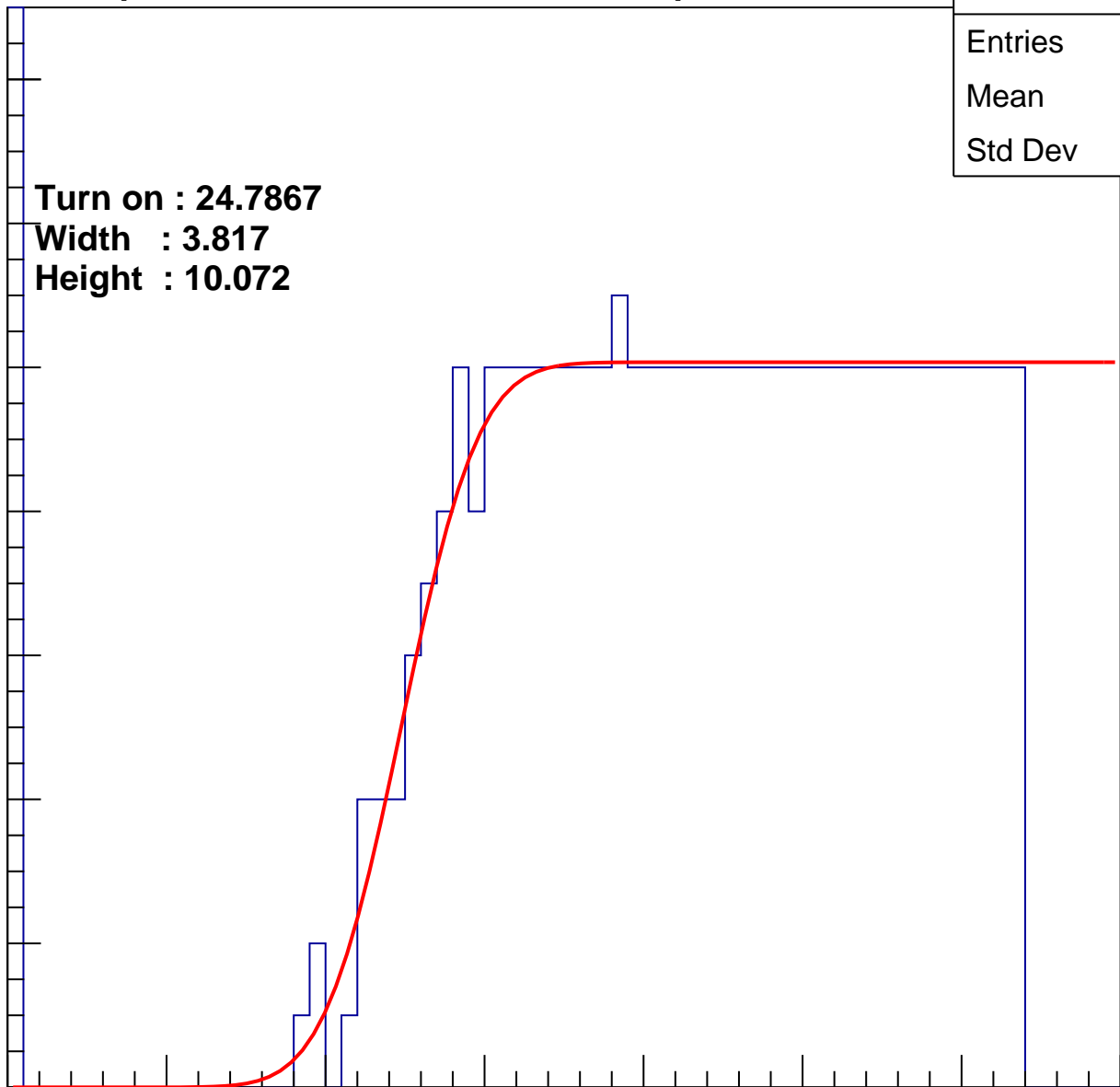
40

50

60

70

ampl



B1L103S, U11-ch127

calib_packv5_041523_1651.root, FC#0, port C2

Entries	462
Mean	37.36
Std Dev	18.68

Turn on : 24.7867

Width : 3.817

Height : 10.072

Entry

14
12
10
8
6
4
2
0

ampl

