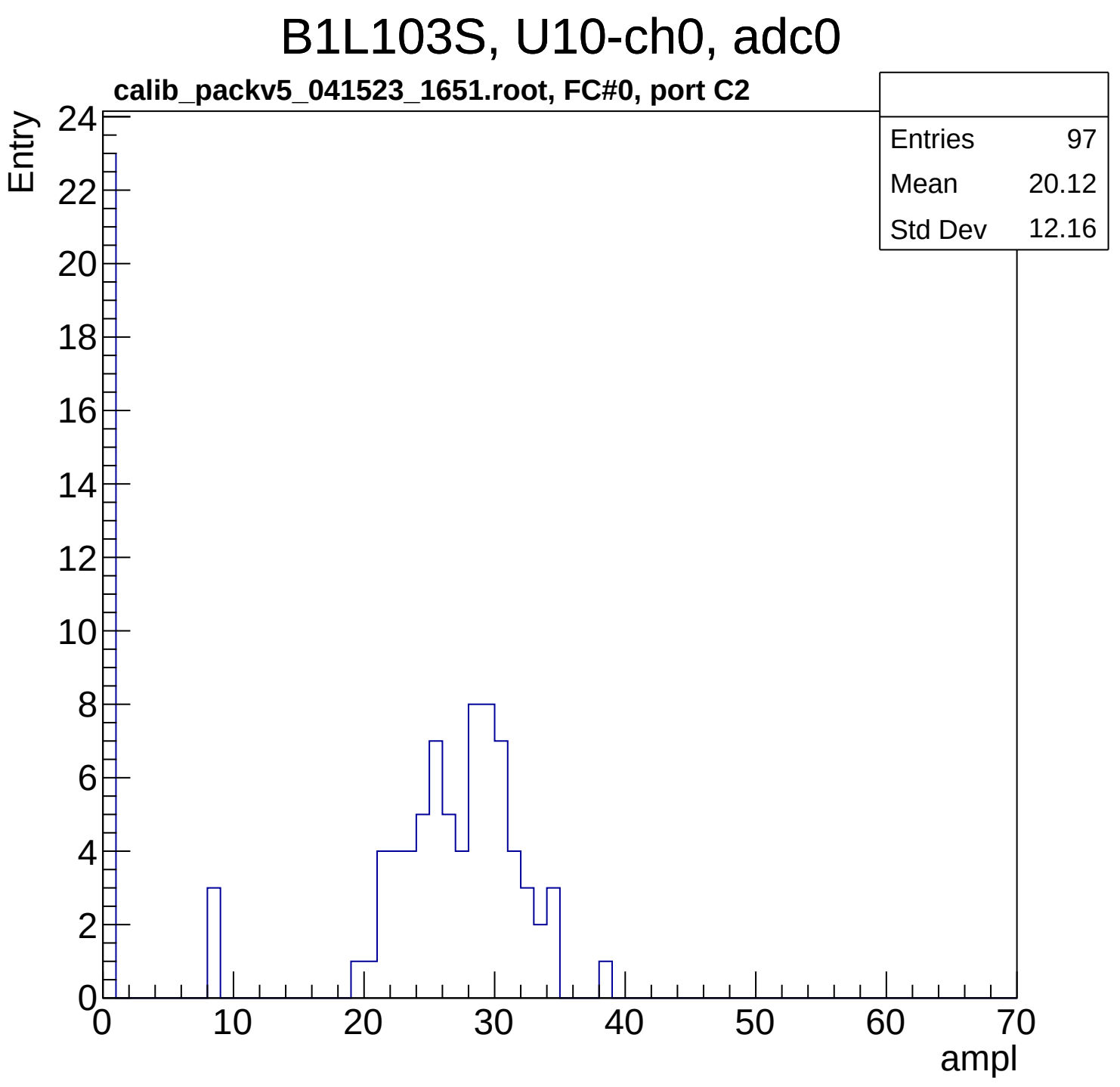
B1L103S, U10-ch0, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 97
Mean 20.12
Std Dev 12.16
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
22
24
0
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40
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60
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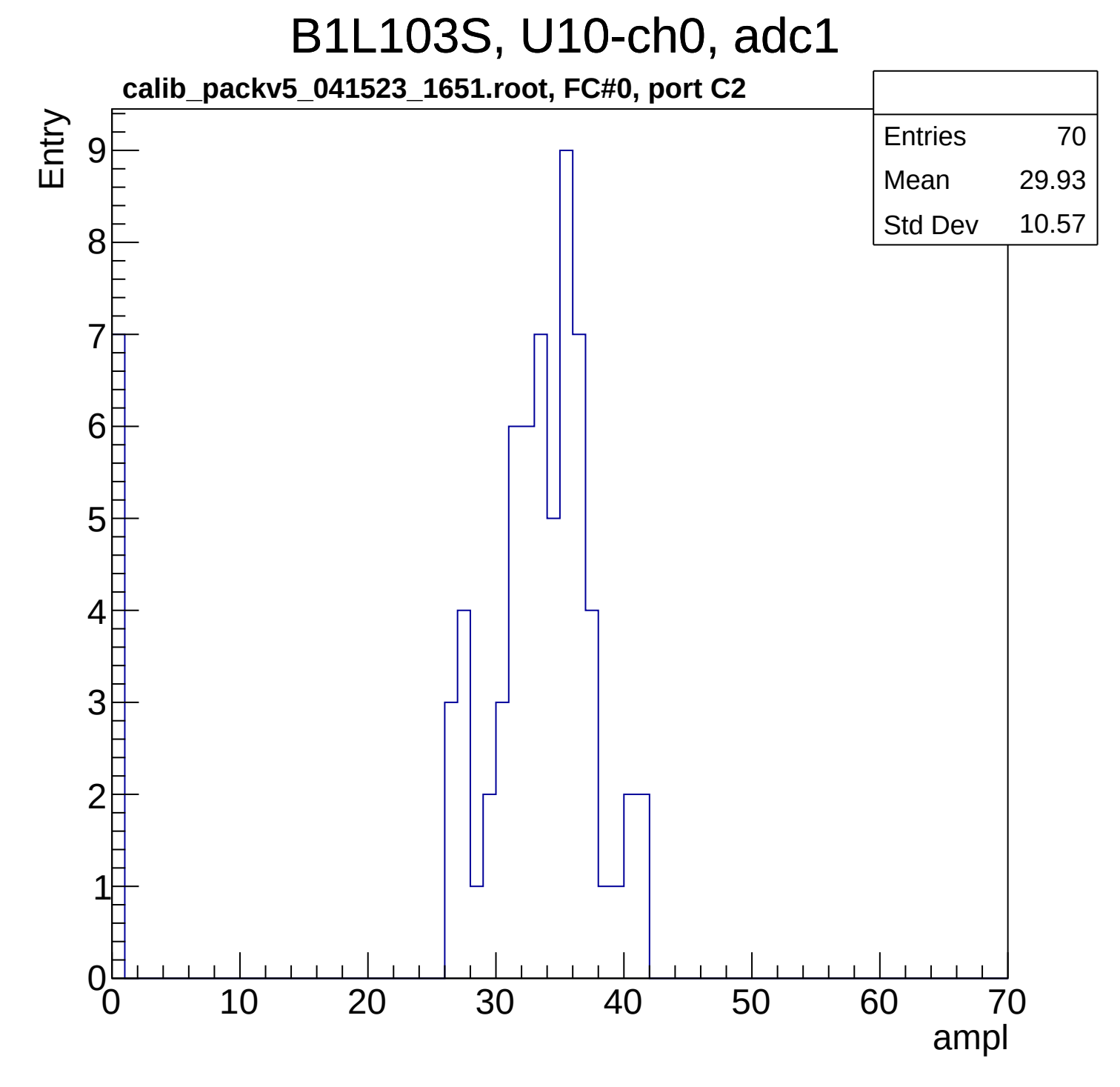
B1L103S, U10-ch0, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 29.93
Std Dev 10.57
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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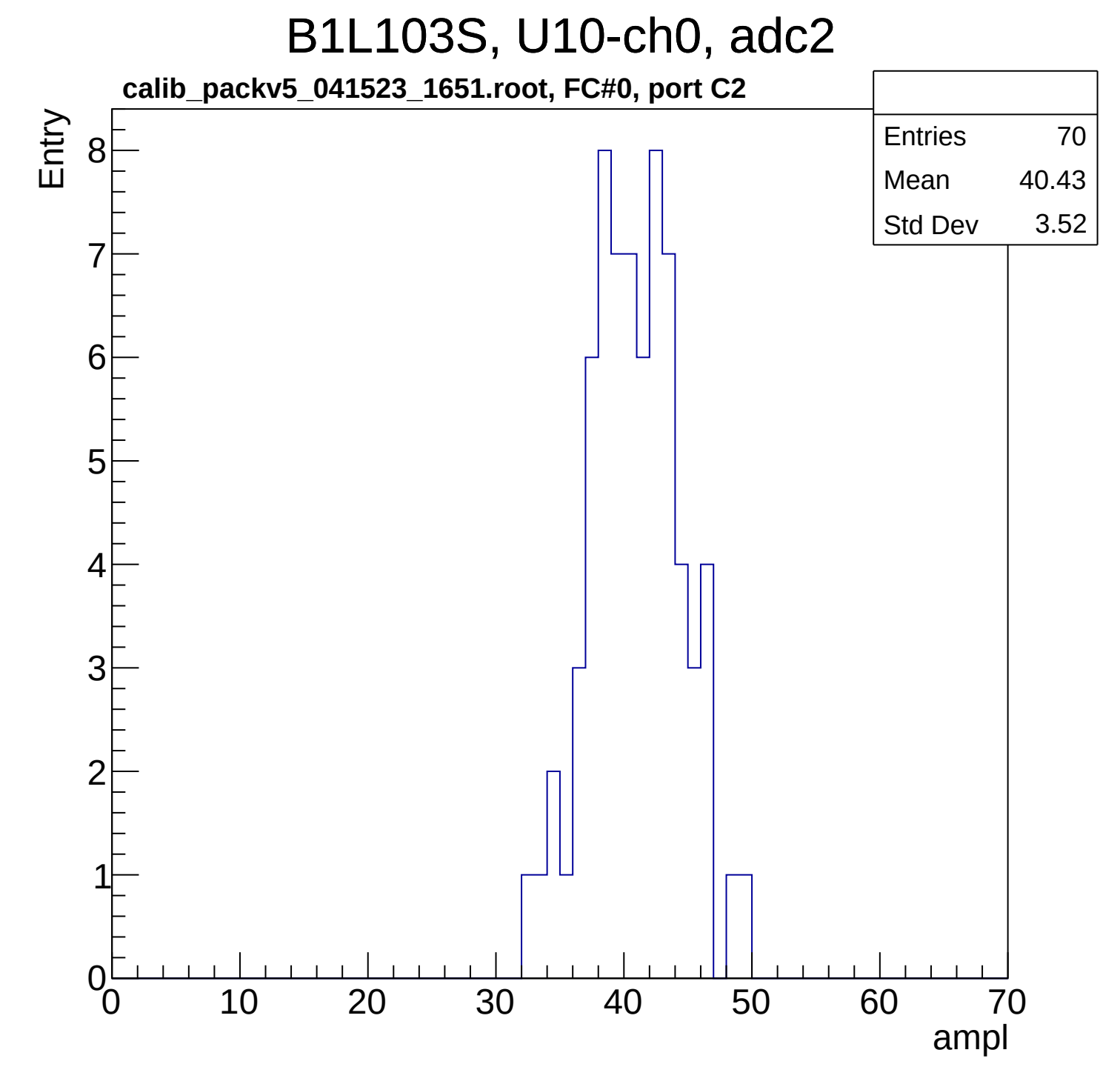
B1L103S, U10-ch0, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 40.43
Std Dev 3.52
Entry
0
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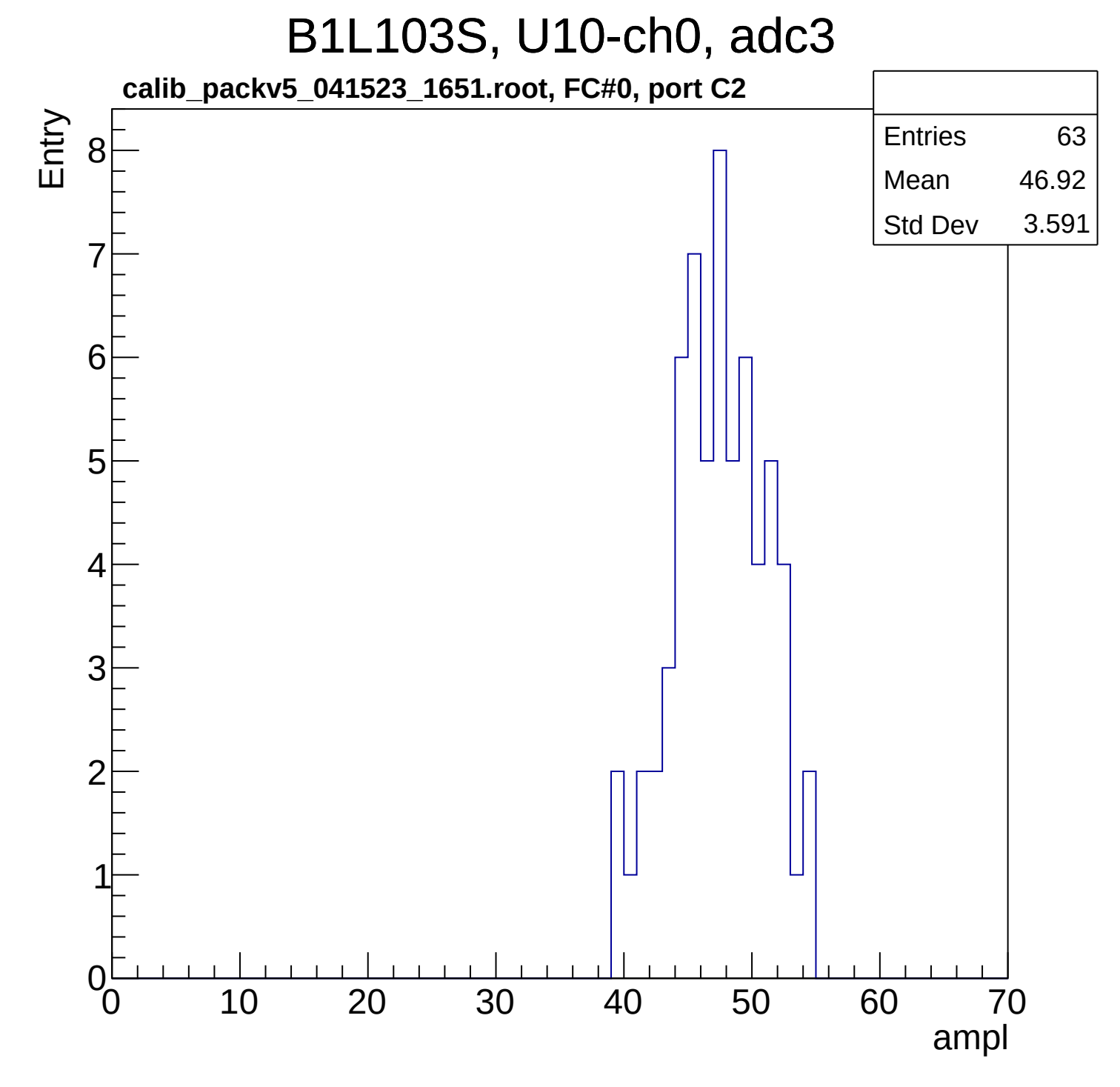
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch0, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 46.92
Std Dev 3.591
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
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60
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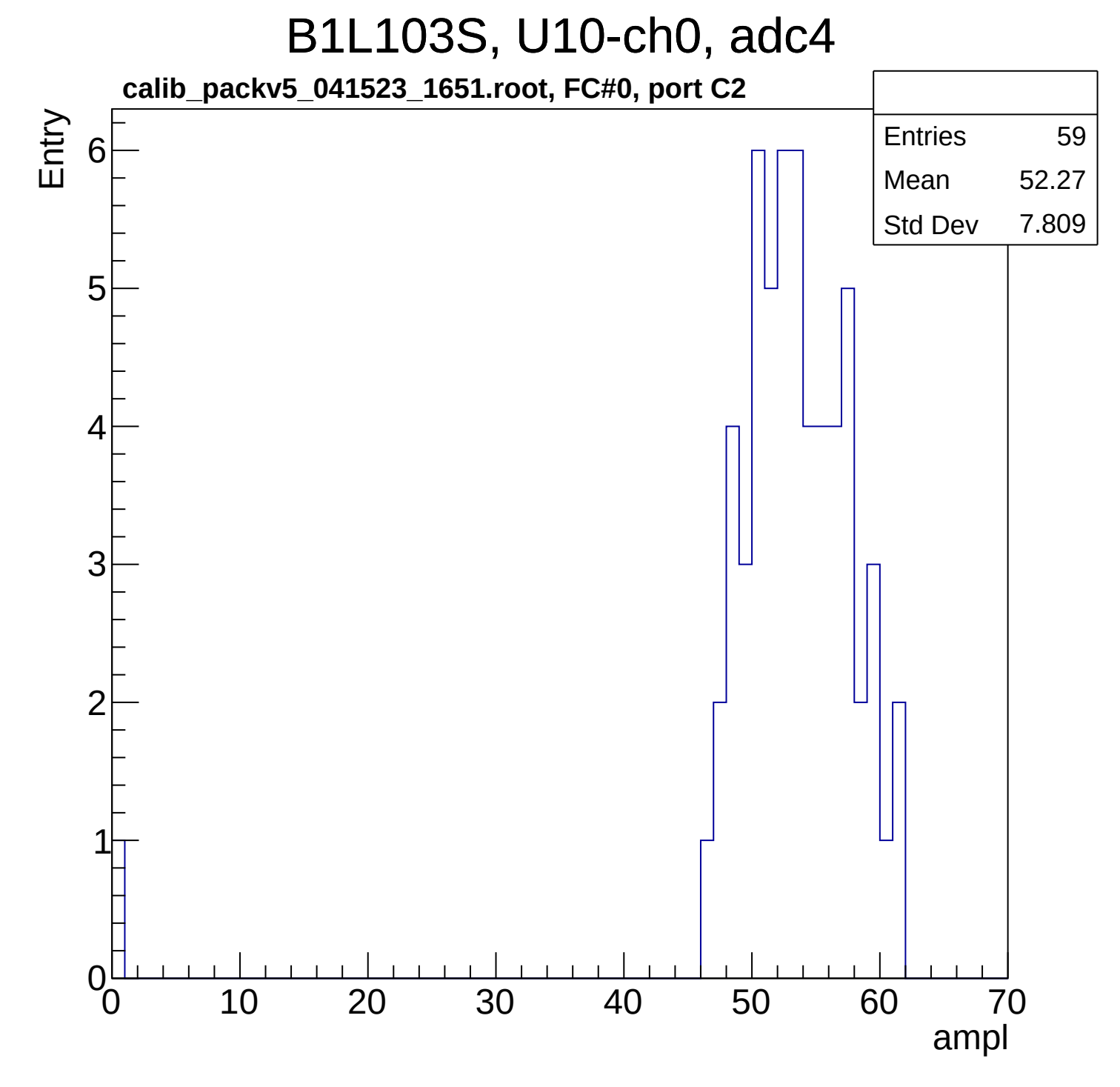
B1L103S, U10-ch0, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 52.27
Std Dev 7.809
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
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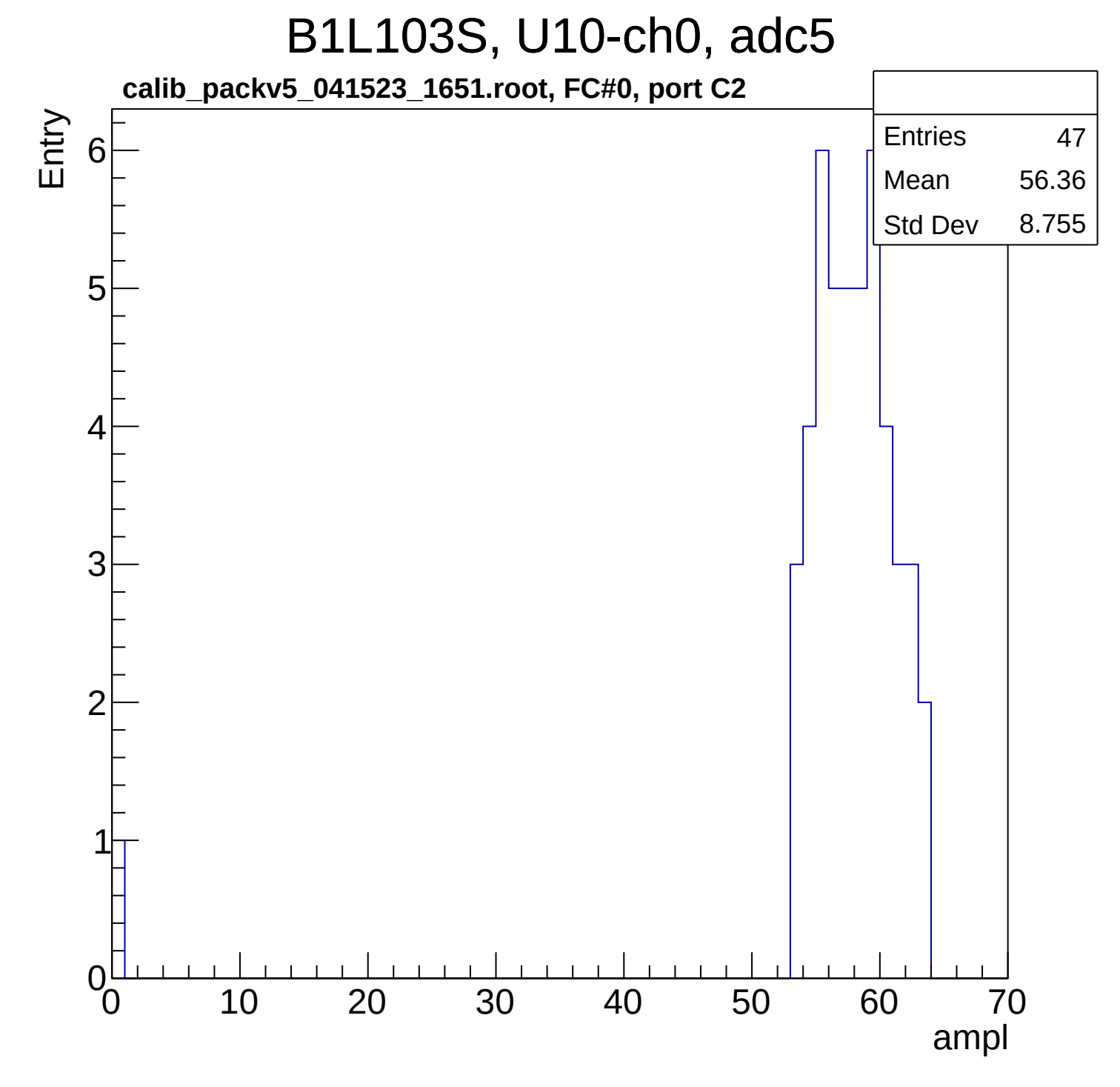
B1L103S, U10-ch0, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 56.36
Std Dev 8.755
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
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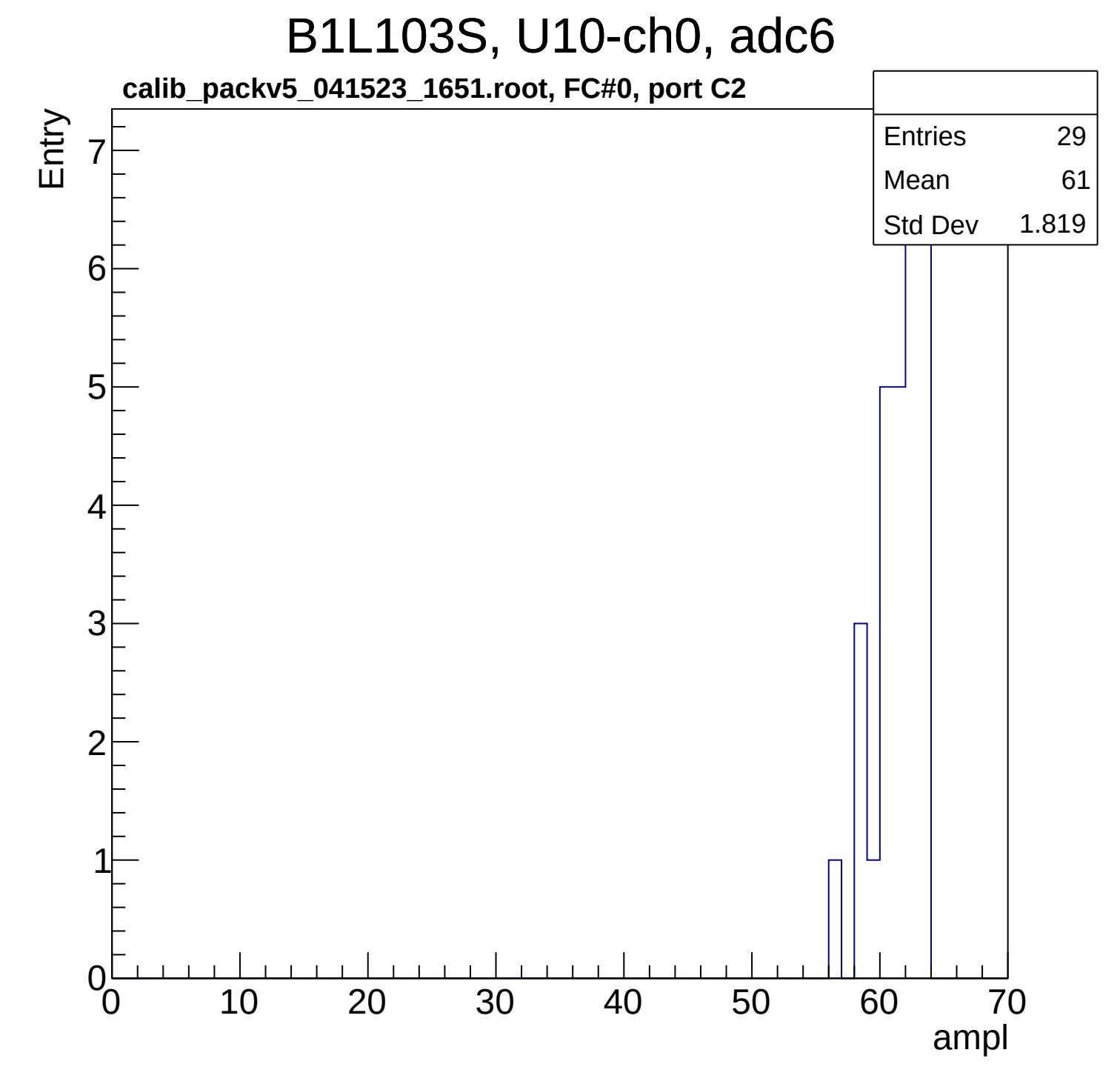
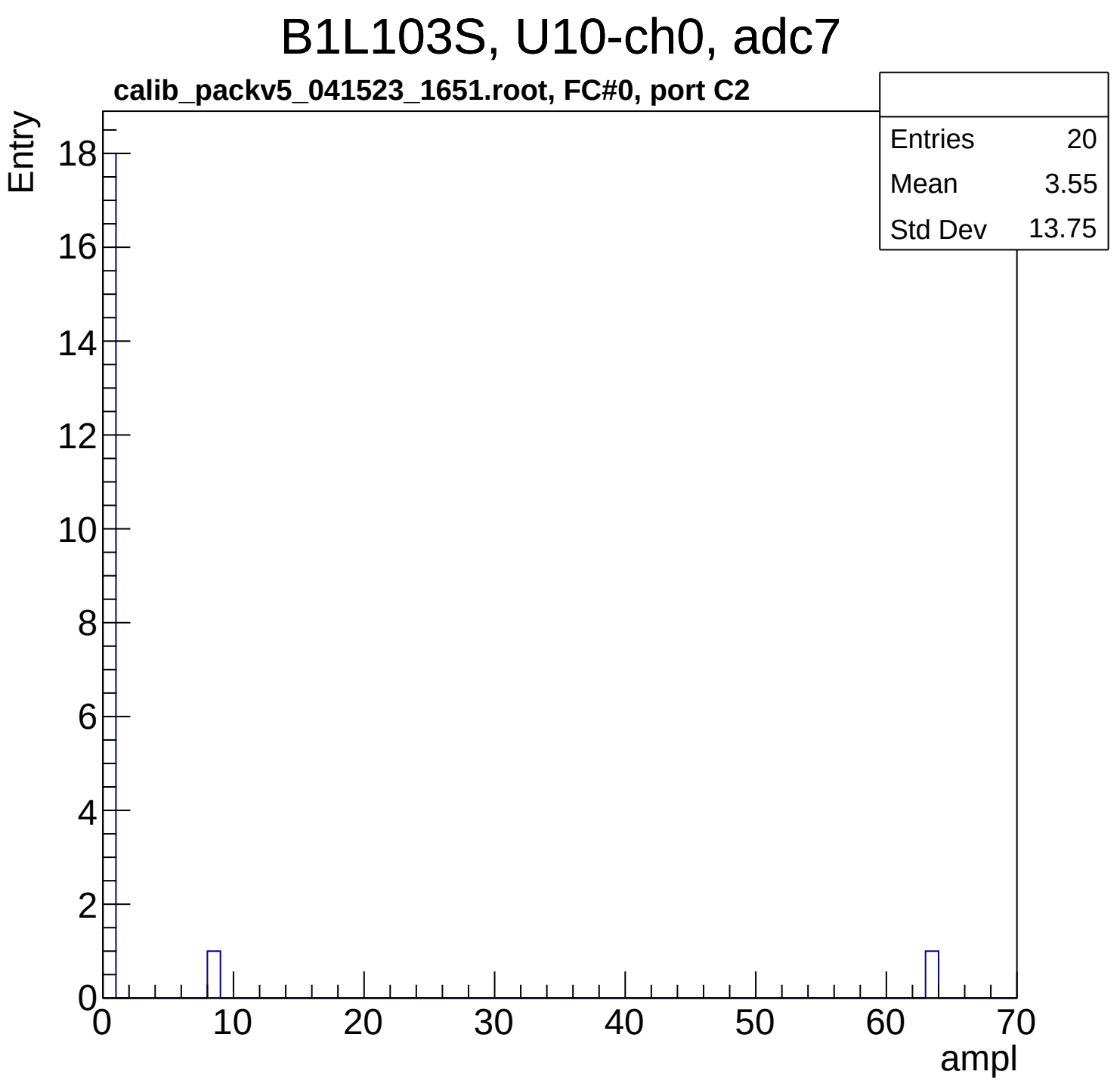
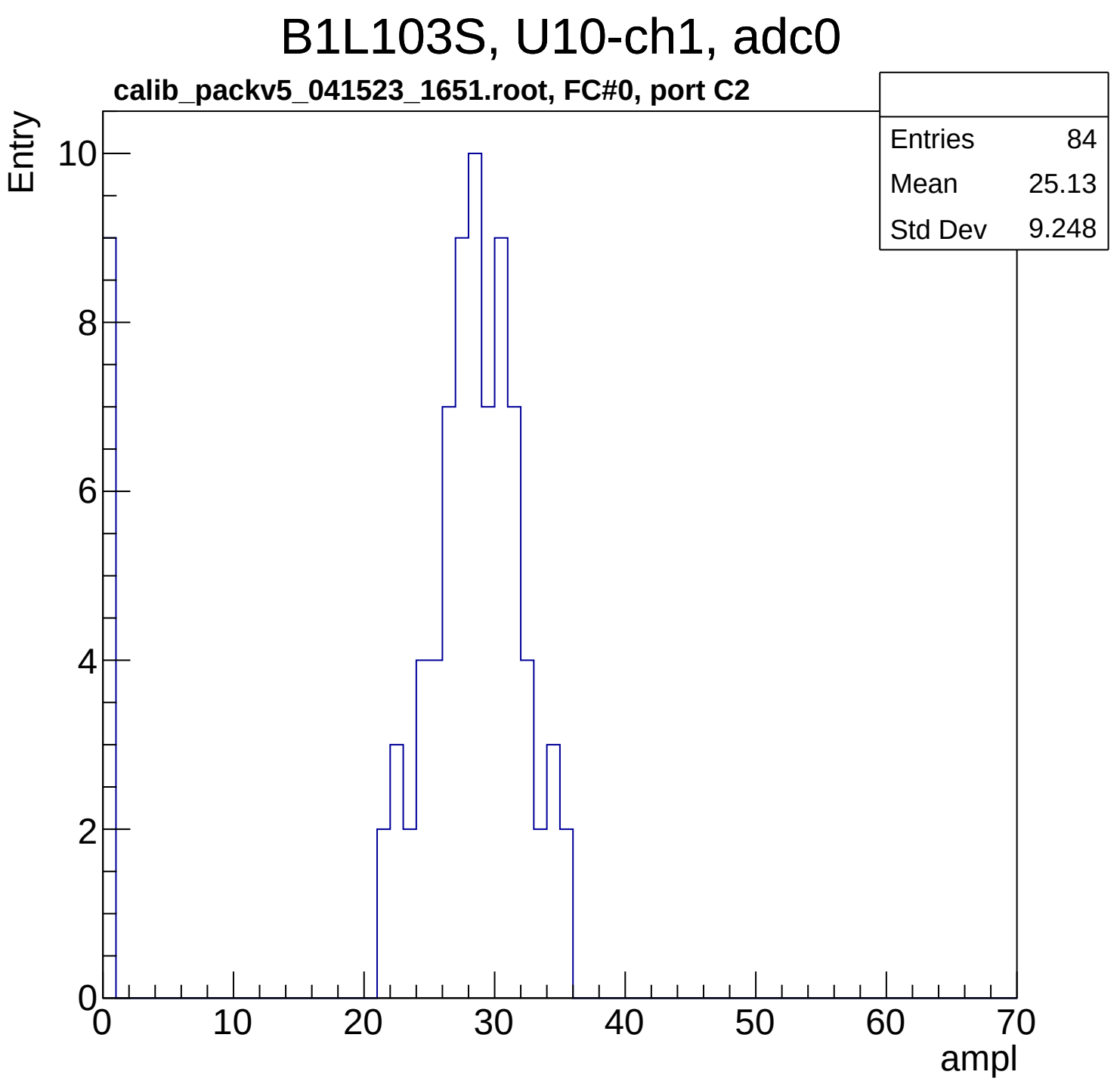
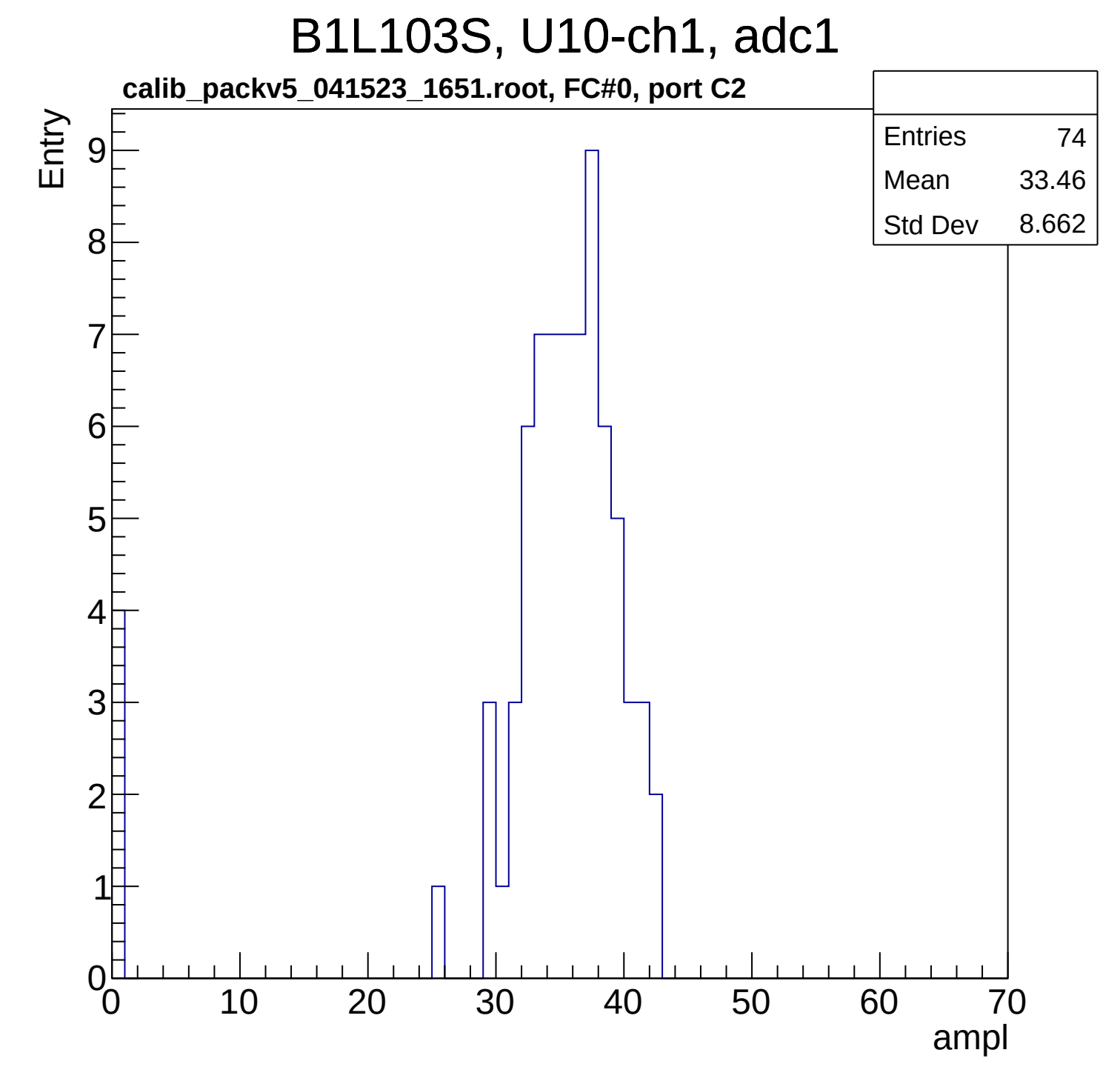
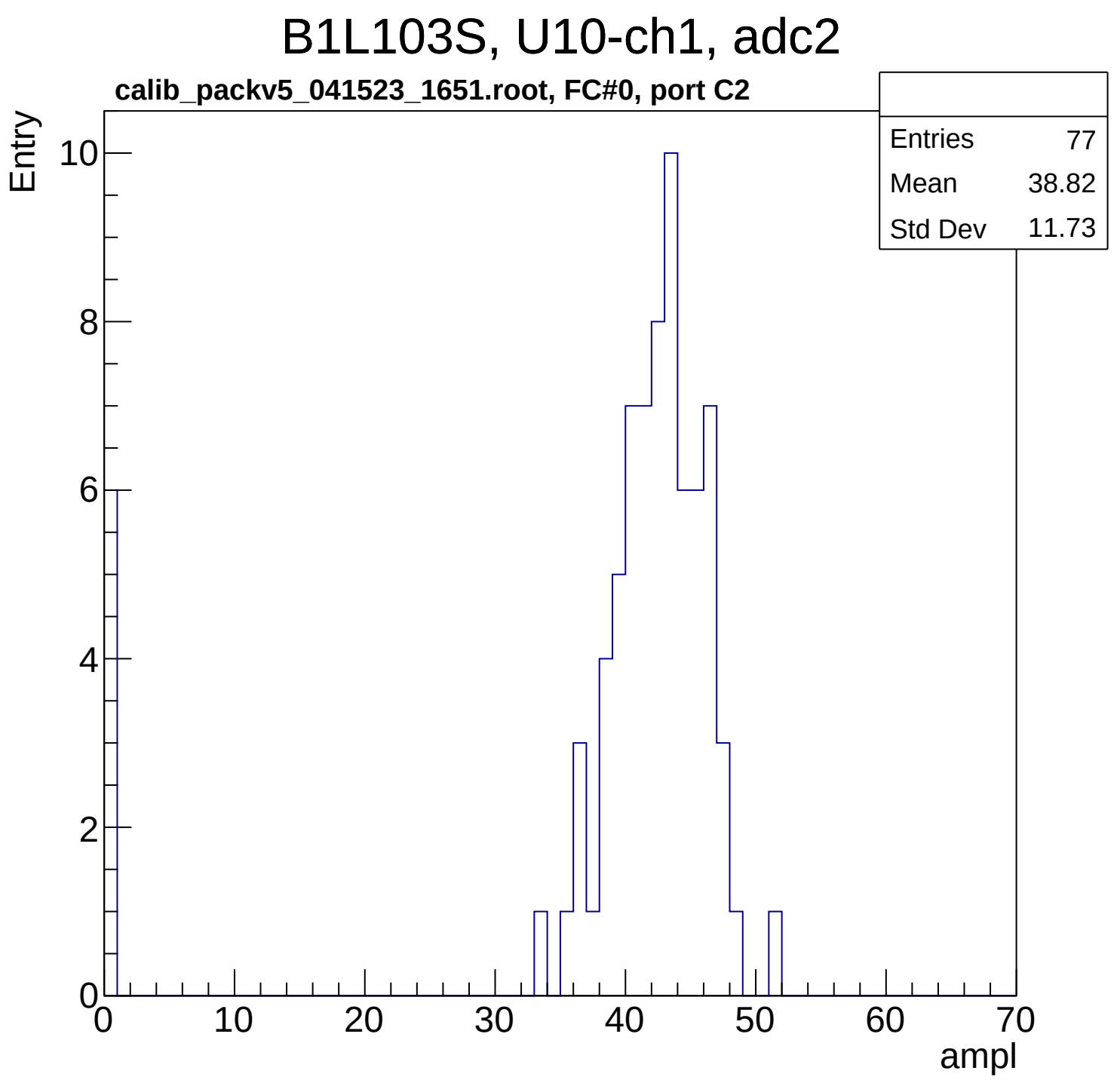
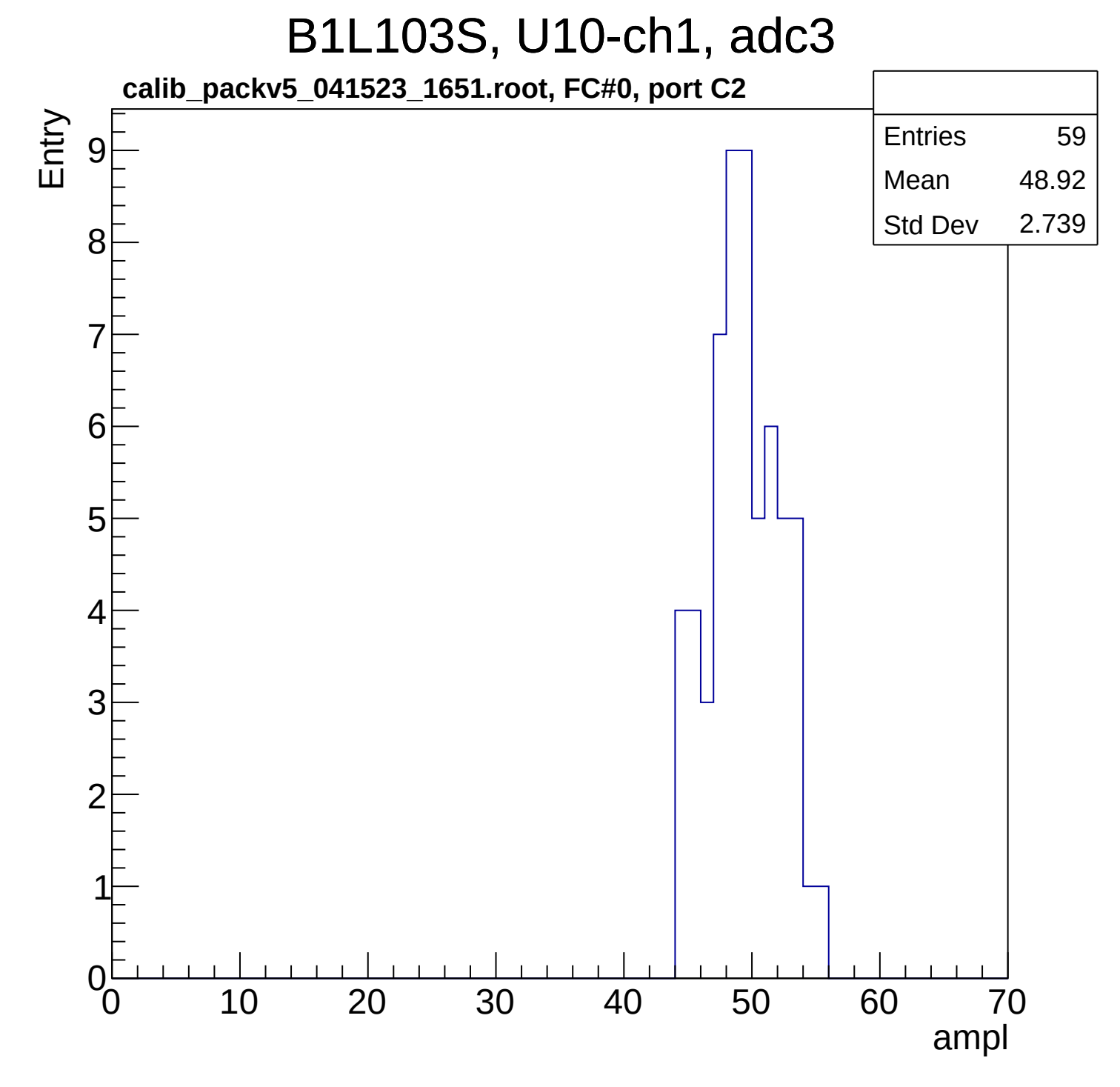

B1L103S, U10-ch0, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 29
Mean 61
Std Dev 1.819
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

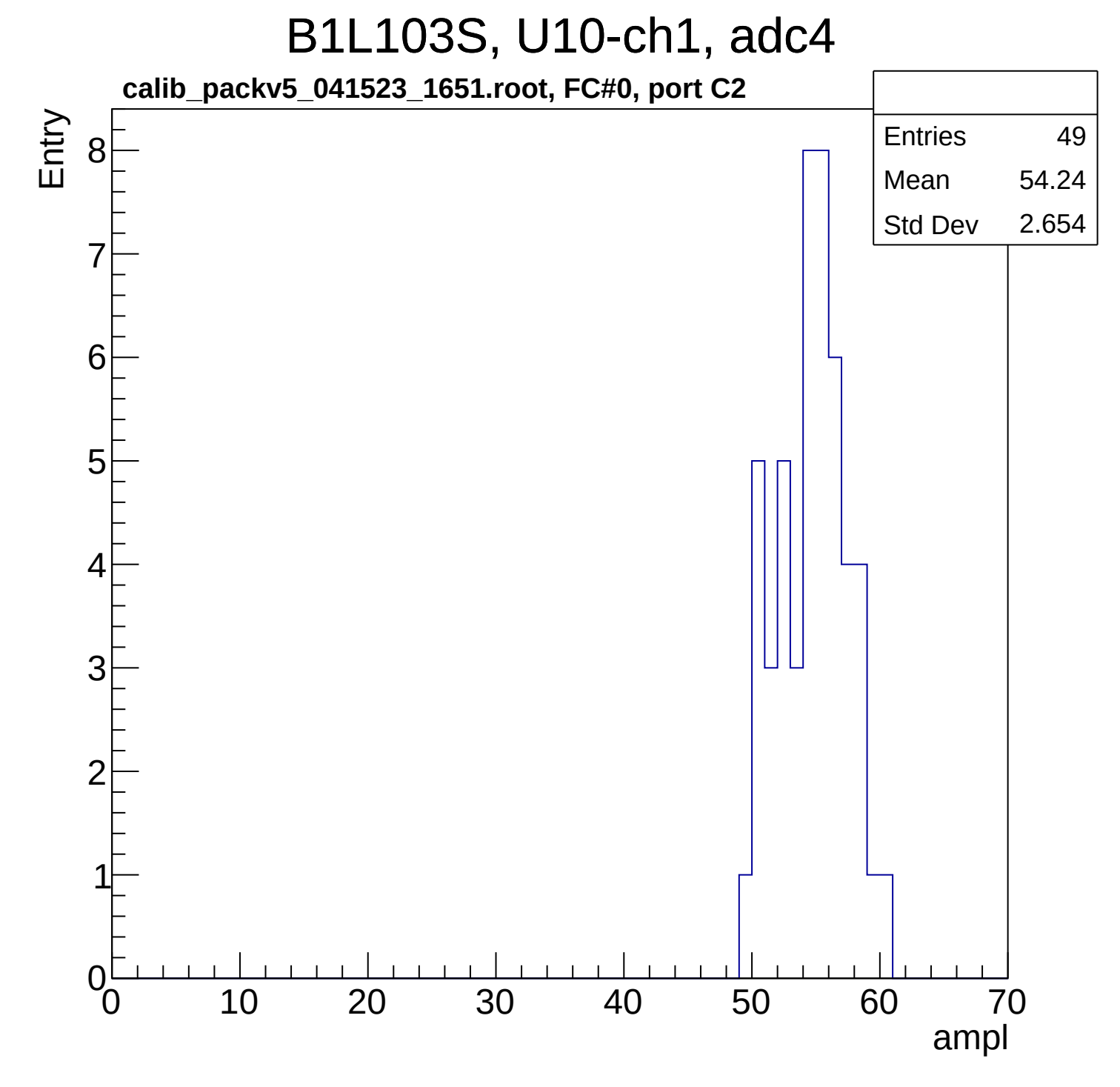

B1L103S, U10-ch0, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.55
Std Dev 13.75
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

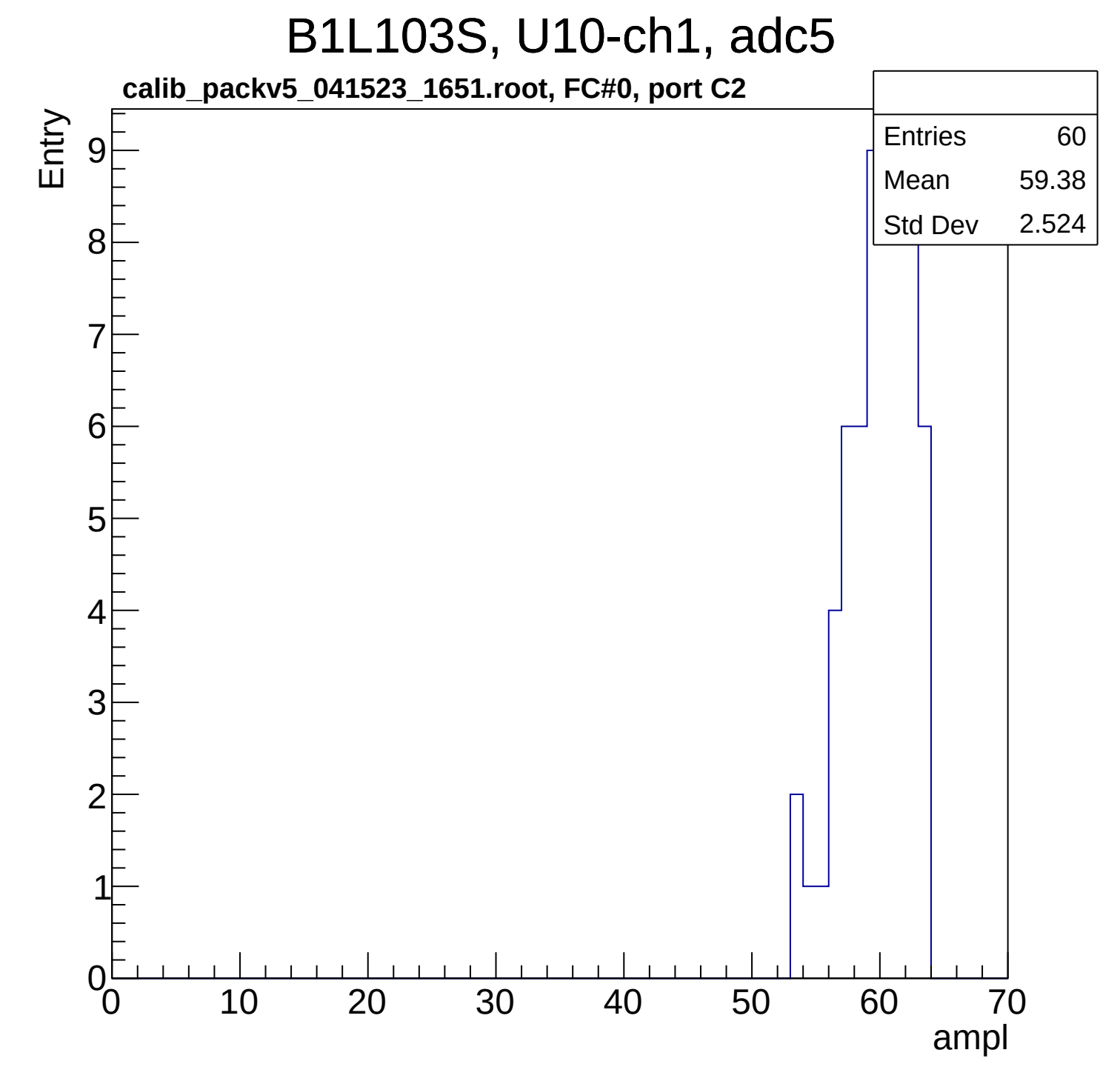

B1L103S, U10-ch1, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 25.13
Std Dev 9.248
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

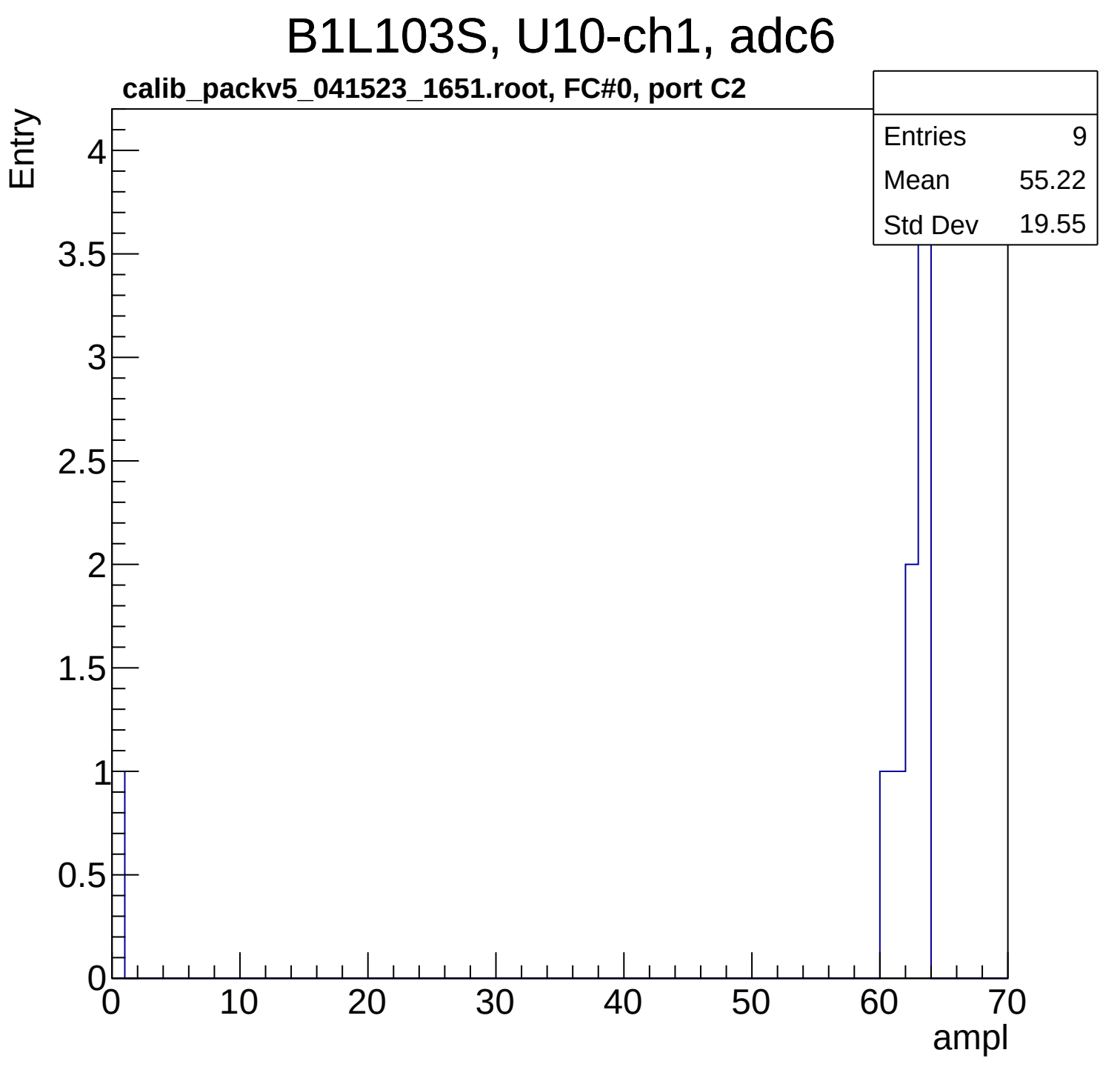

B1L103S, U10-ch1, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 33.46
Std Dev 8.662
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

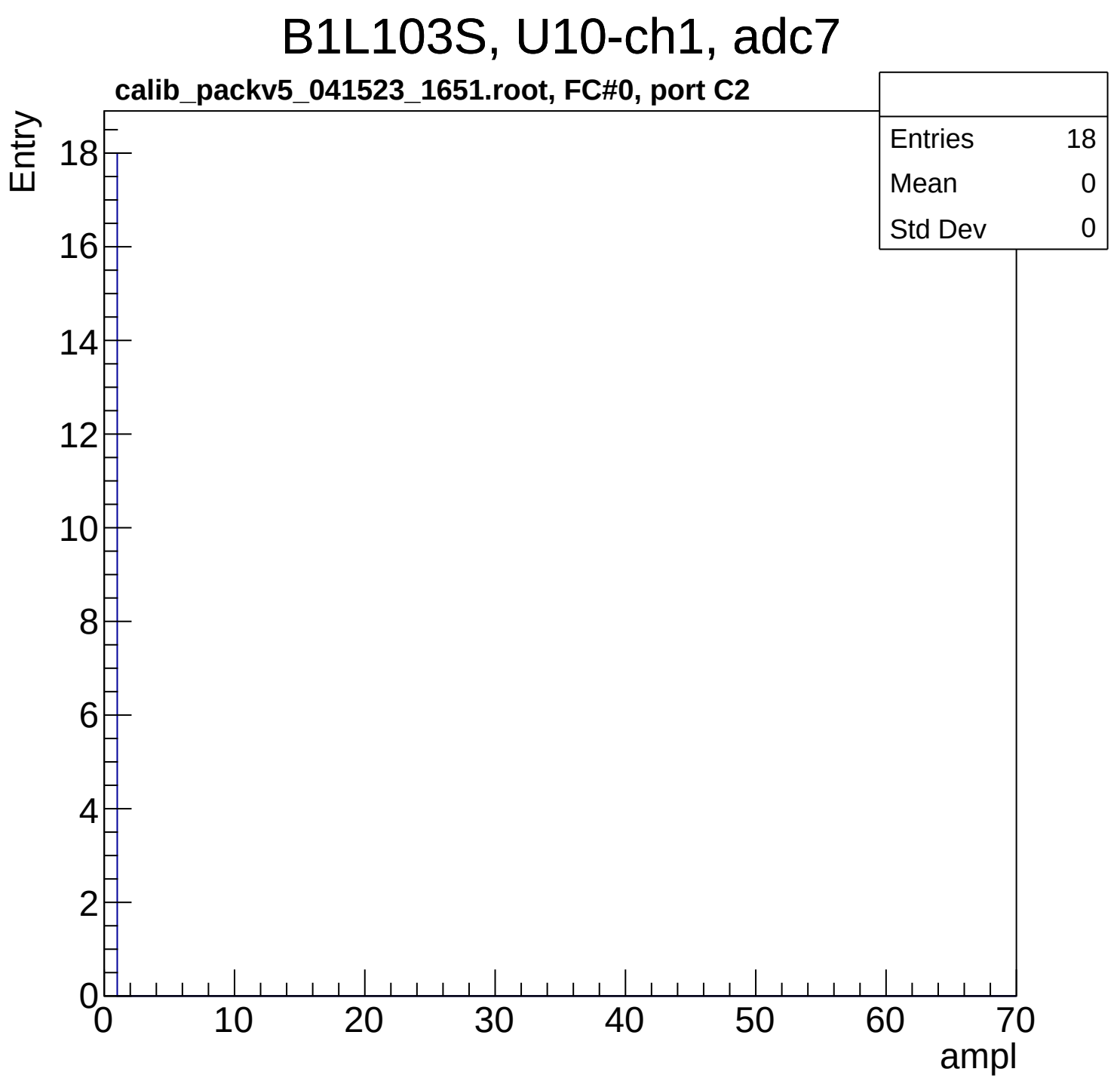

B1L103S, U10-ch1, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 38.82
Std Dev 11.73
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

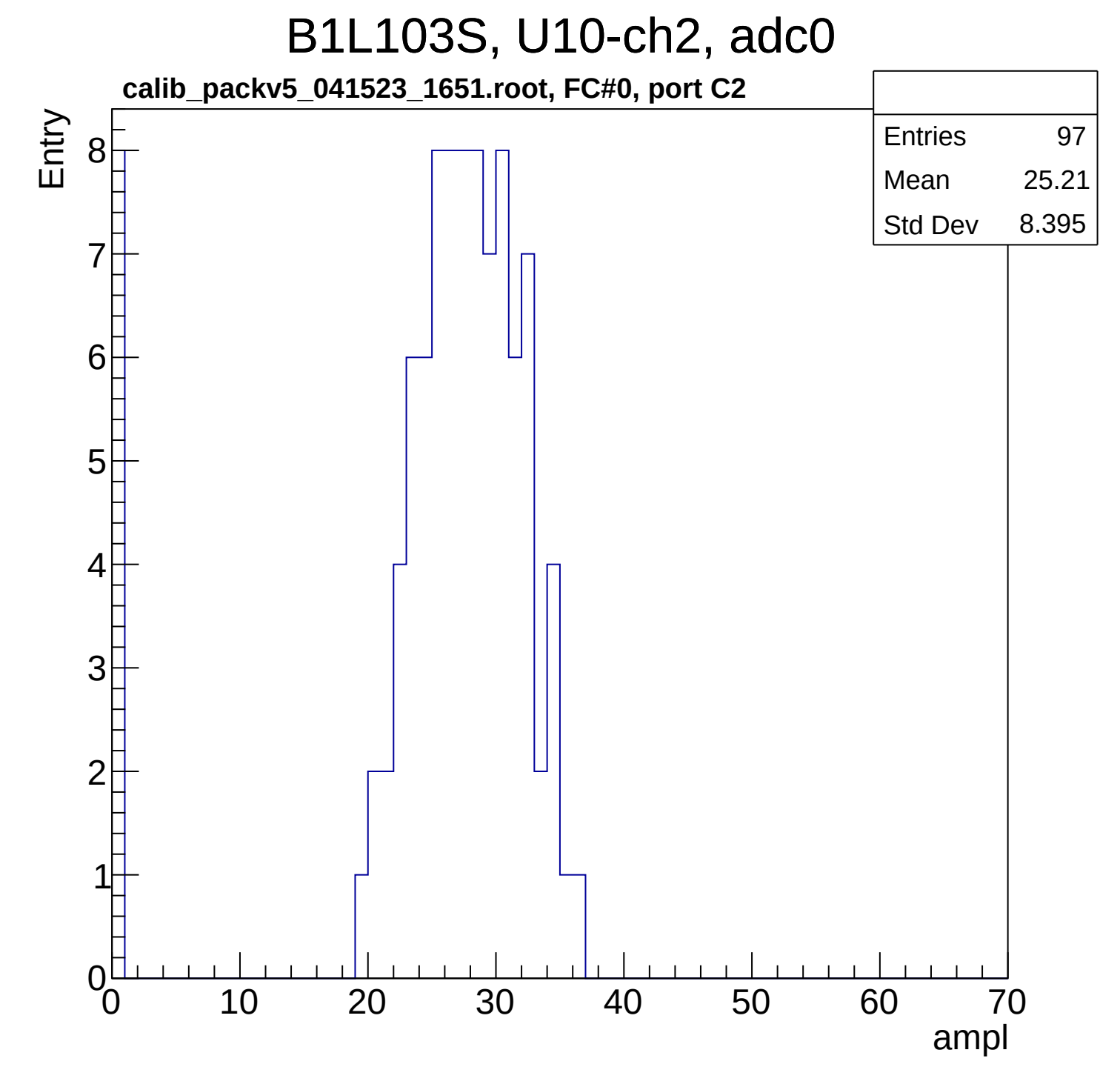

B1L103S, U10-ch1, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 48.92
Std Dev 2.739
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U10-ch1, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 54.24
Std Dev 2.654
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U10-ch1, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 59.38
Std Dev 2.524
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U10-ch1, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 9
Mean 55.22
Std Dev 19.55
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U10-ch1, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch2, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 97
Mean 25.21
Std Dev 8.395
Entry
ampl
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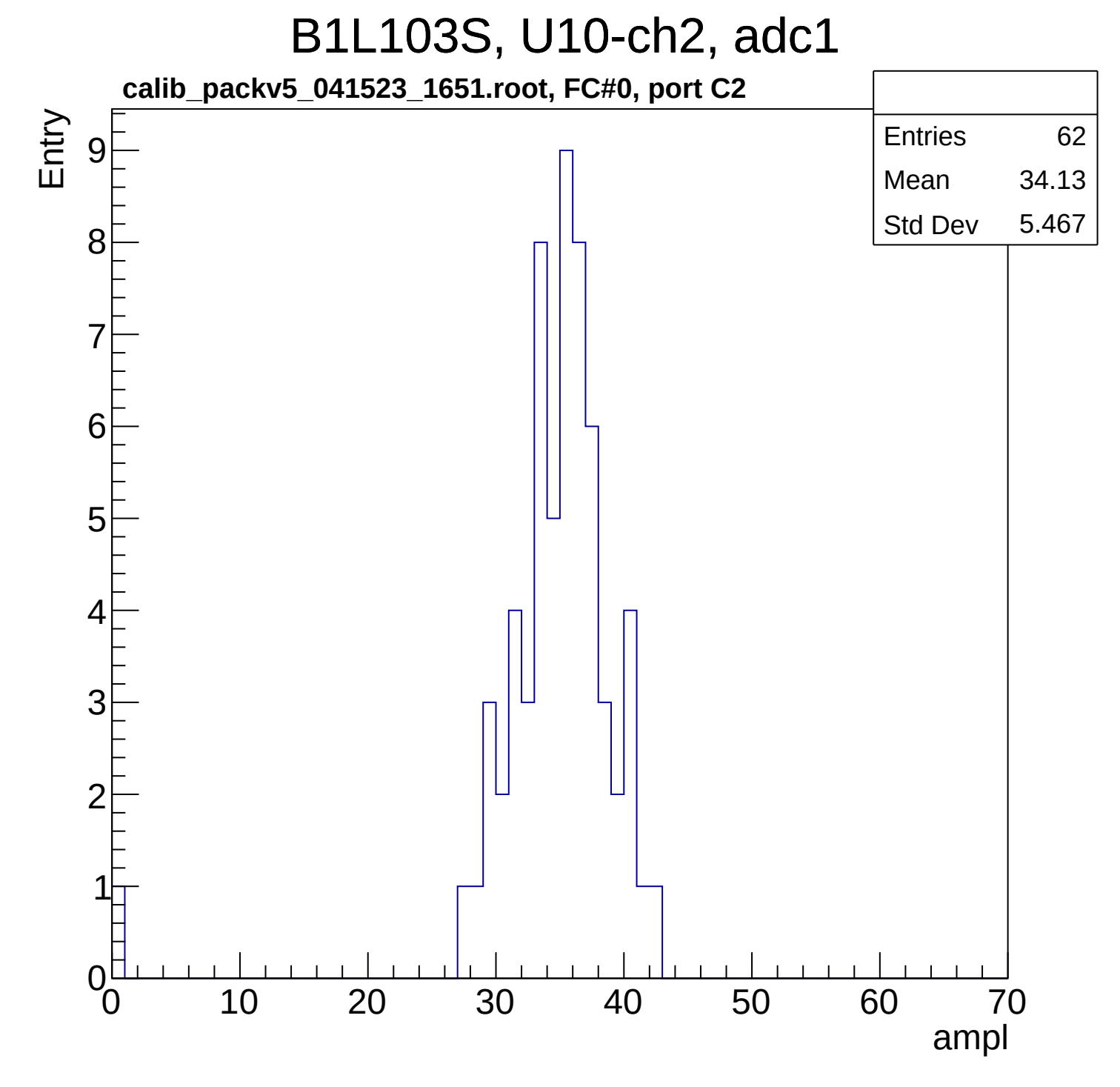
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U10-ch2, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 34.13
Std Dev 5.467
Entry
ampl
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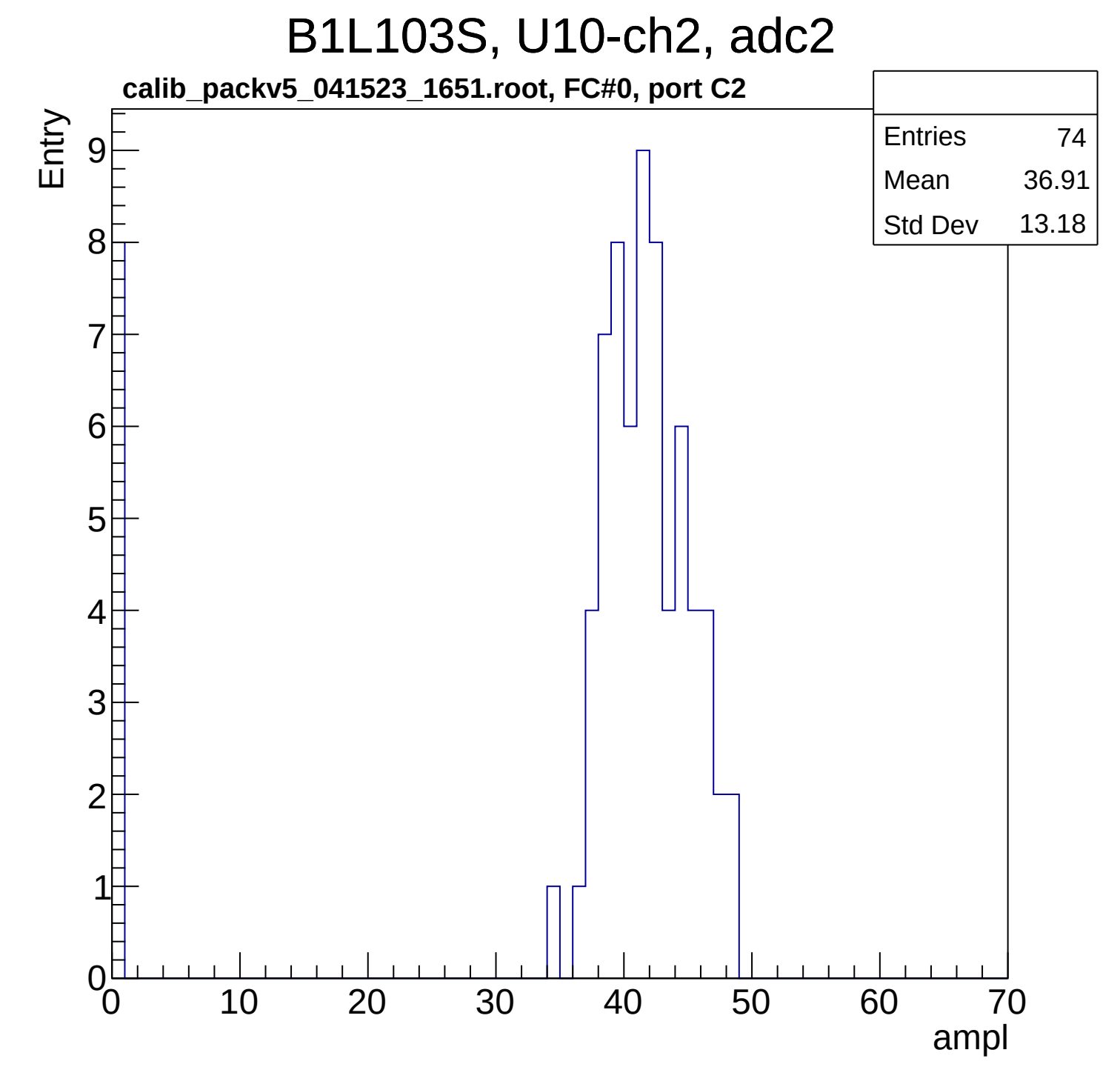
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U10-ch2, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 36.91
Std Dev 13.18
Entry
ampl
0
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2
3
4
5
6
7
8
9
0
10
20
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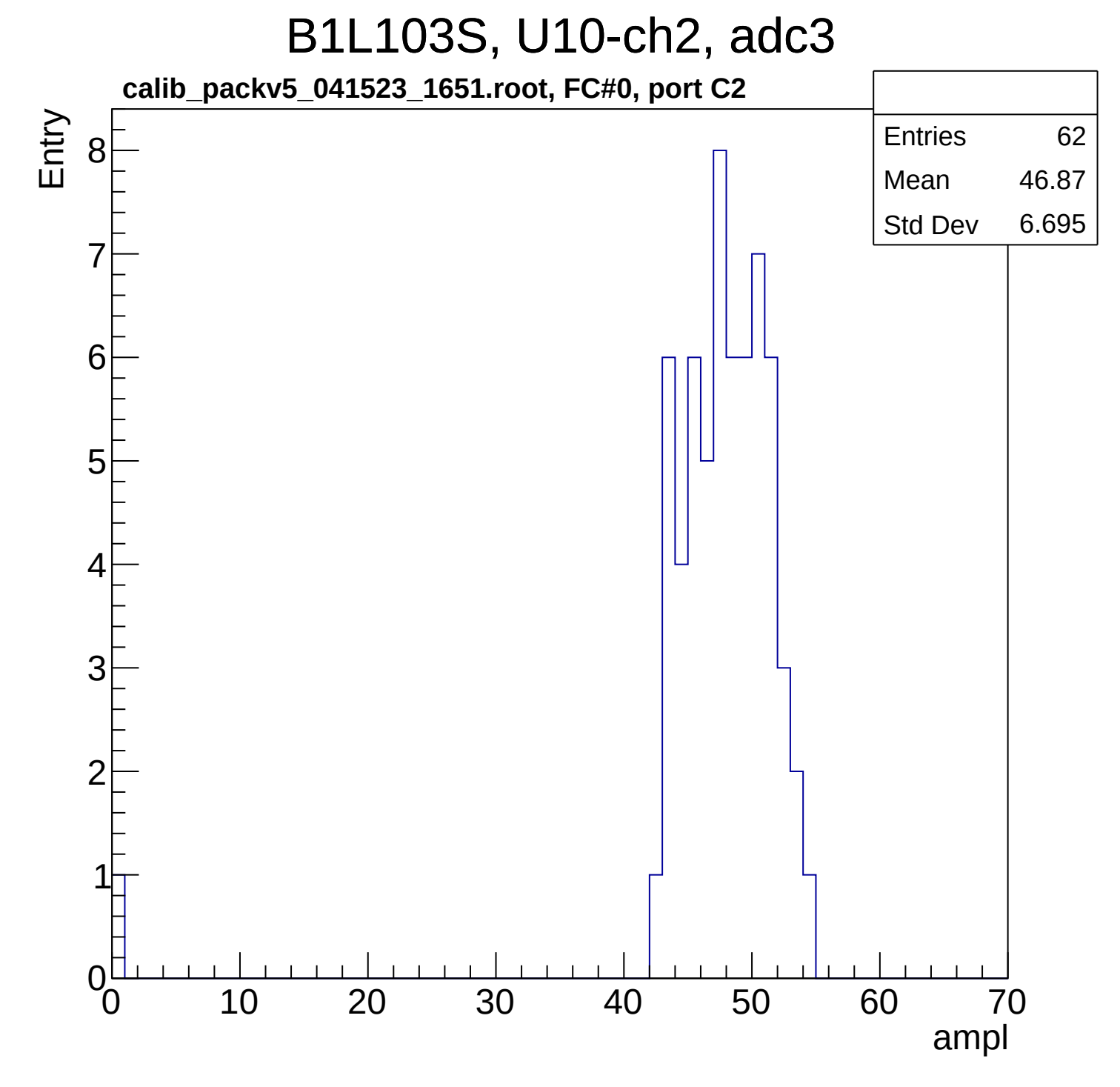
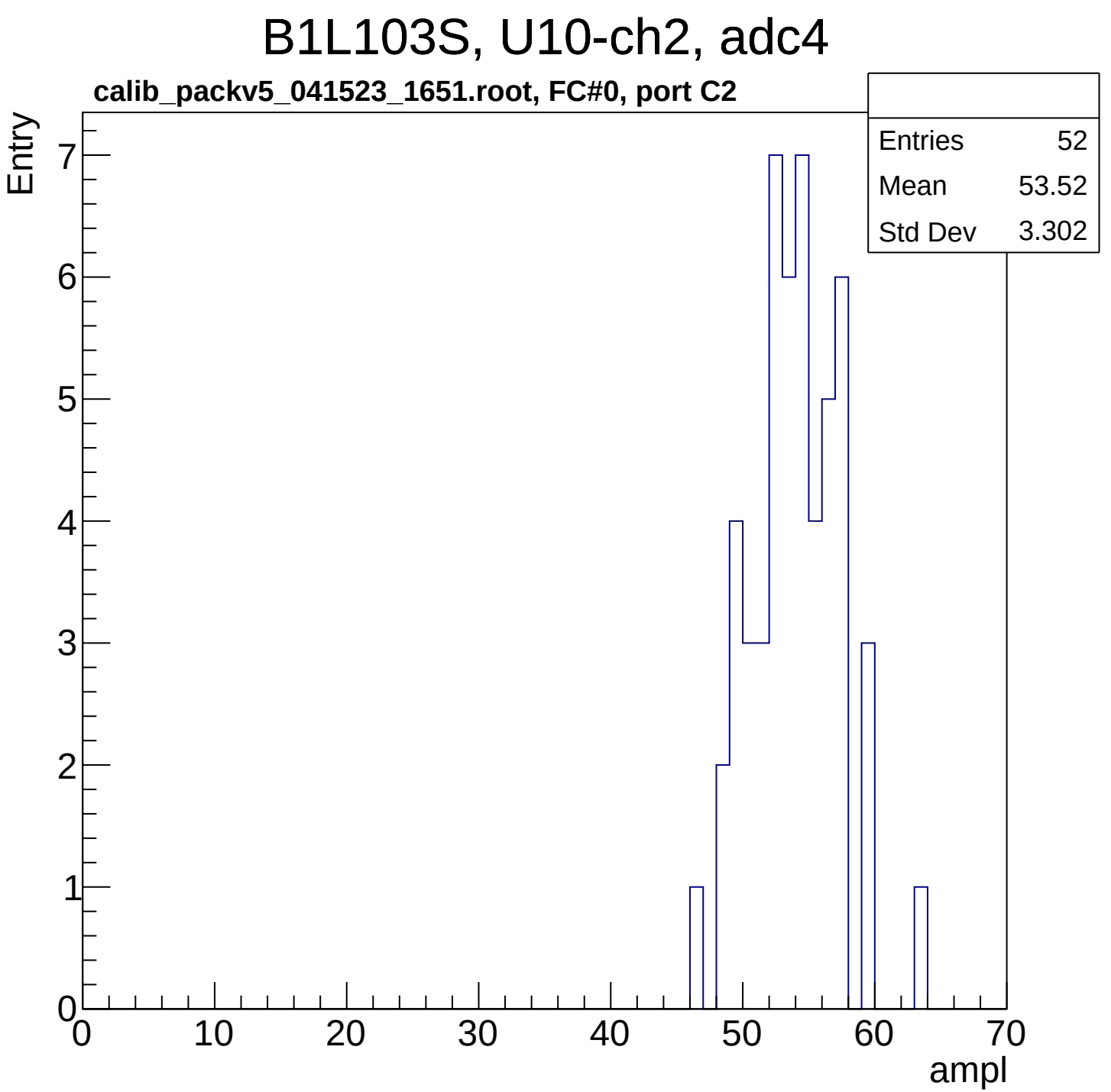
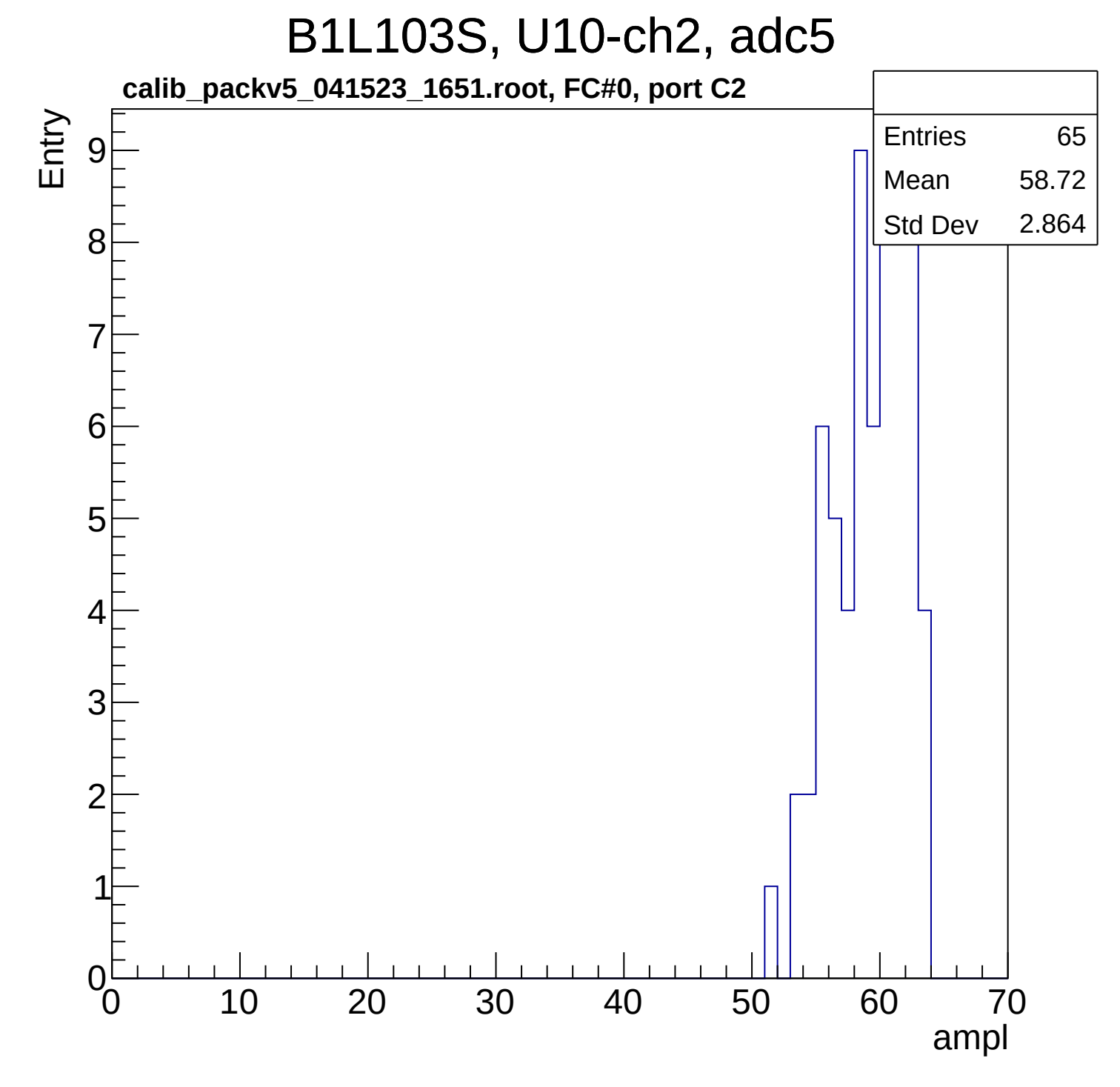
40
50
60
70


B1L103S, U10-ch2, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 46.87
Std Dev 6.695
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U10-ch2, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 53.52
Std Dev 3.302
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U10-ch2, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 58.72
Std Dev 2.864
Entry
ampl
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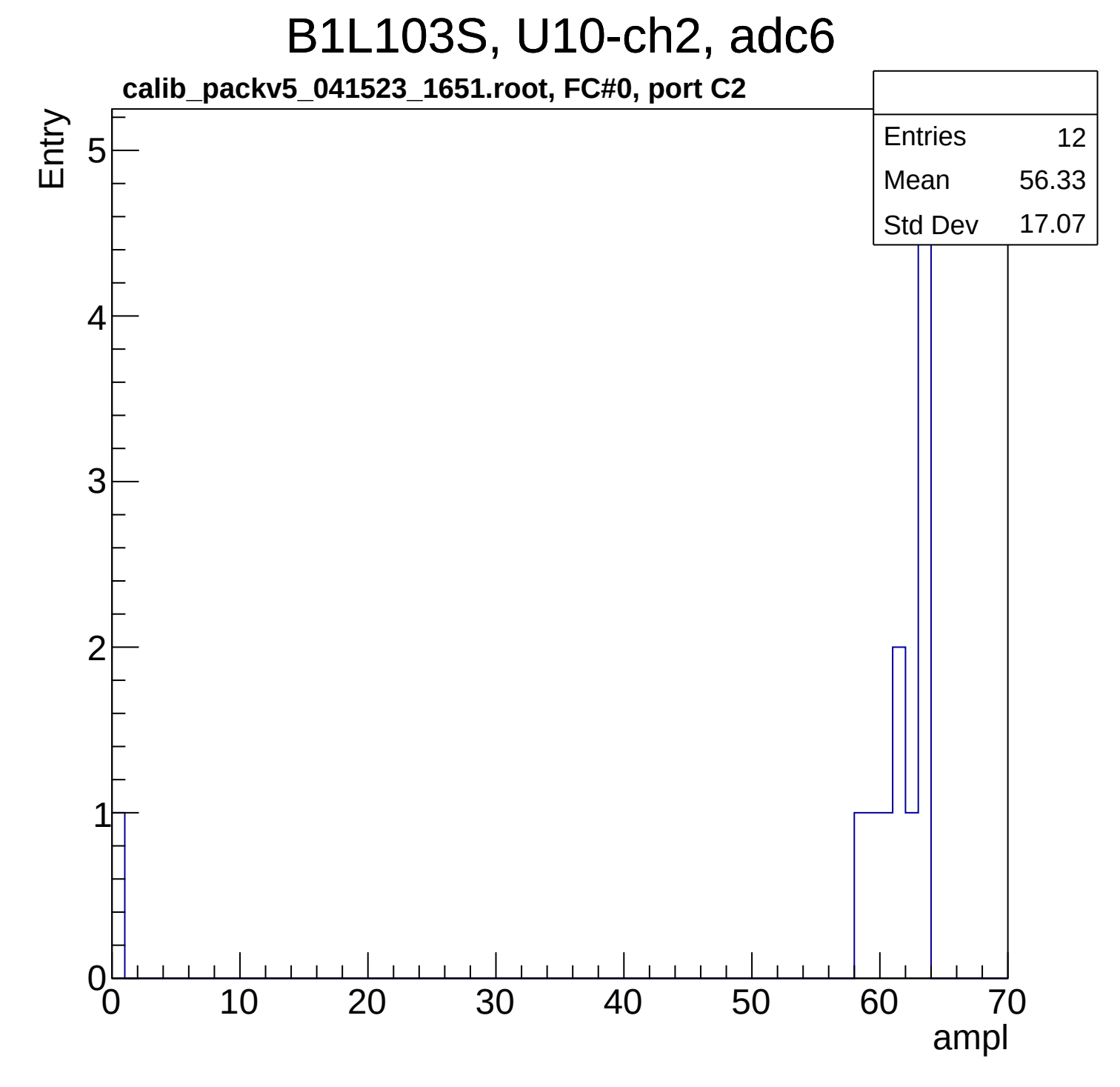
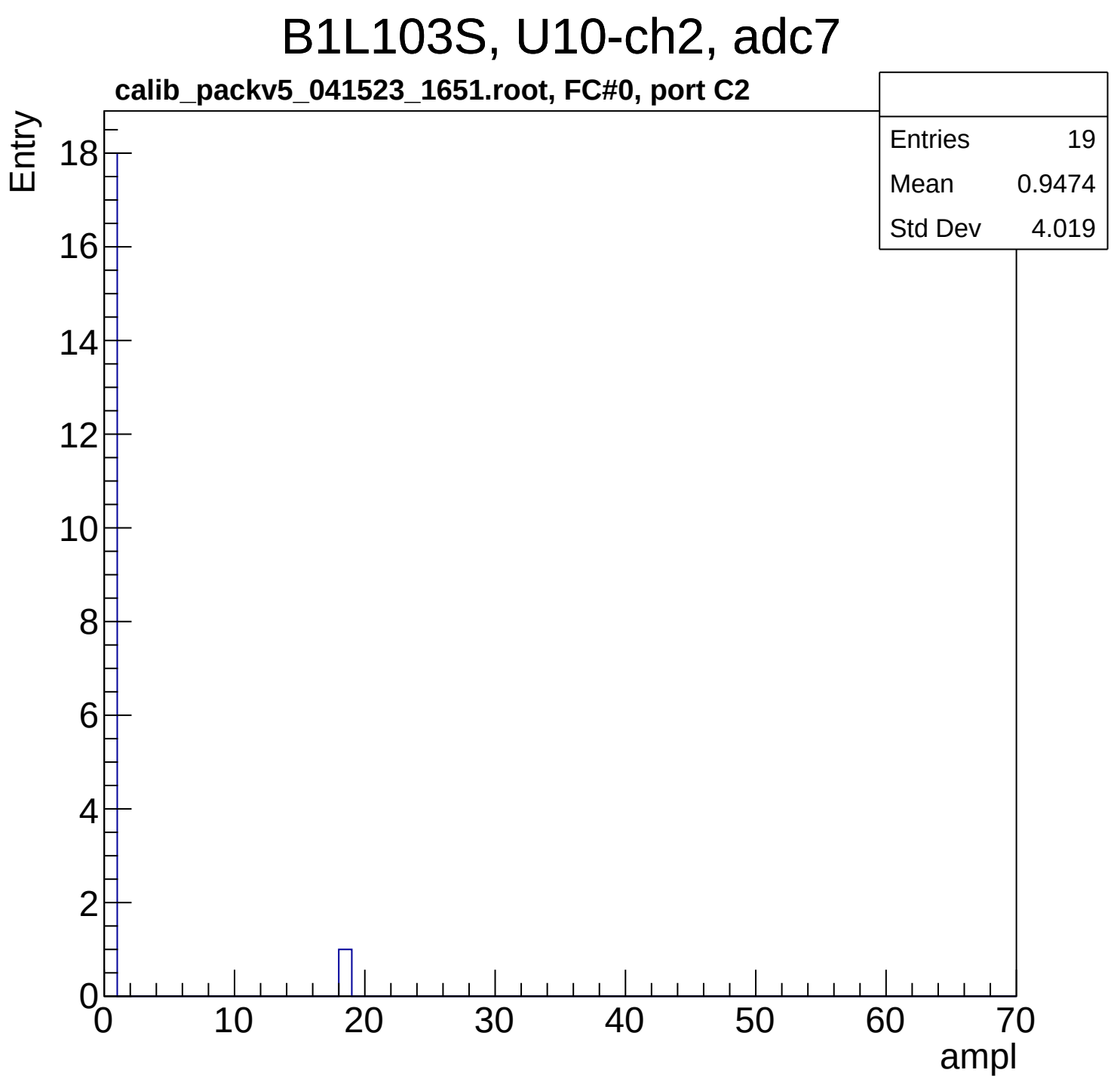
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U10-ch2, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 56.33
Std Dev 17.07
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch2, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0.9474
Std Dev 4.019
Entry
0
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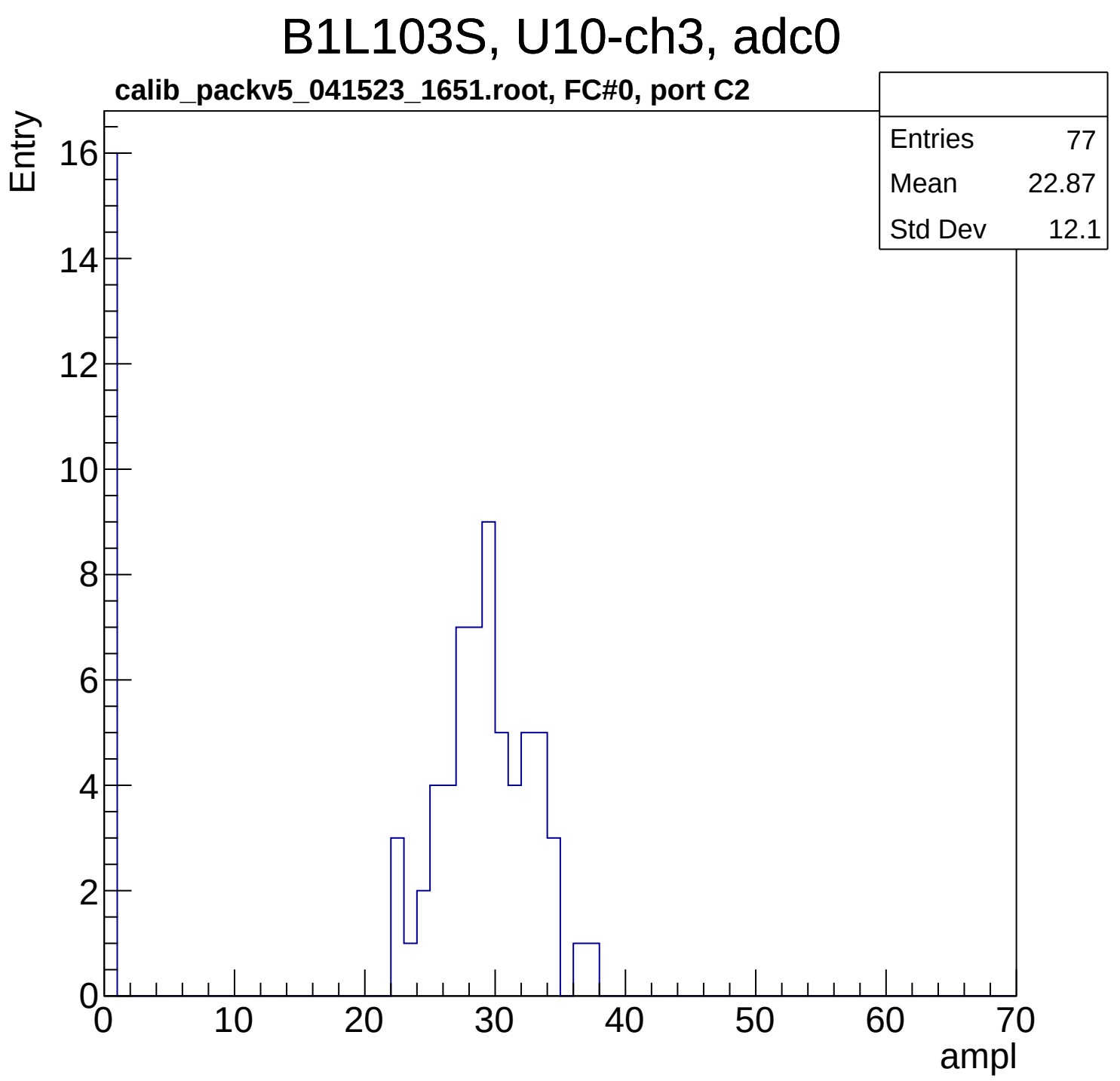
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch3, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 22.87
Std Dev 12.1
Entry
ampl
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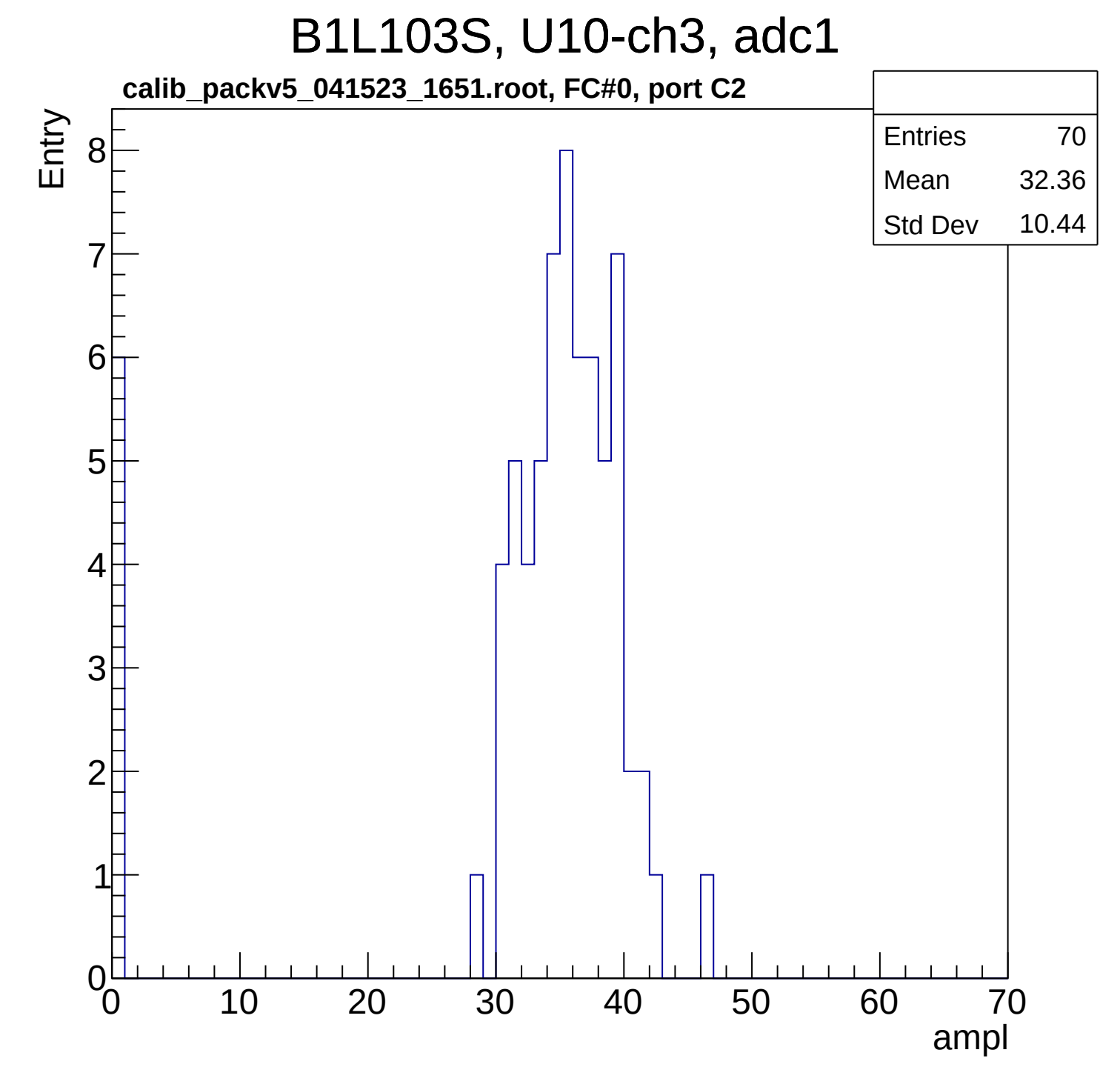
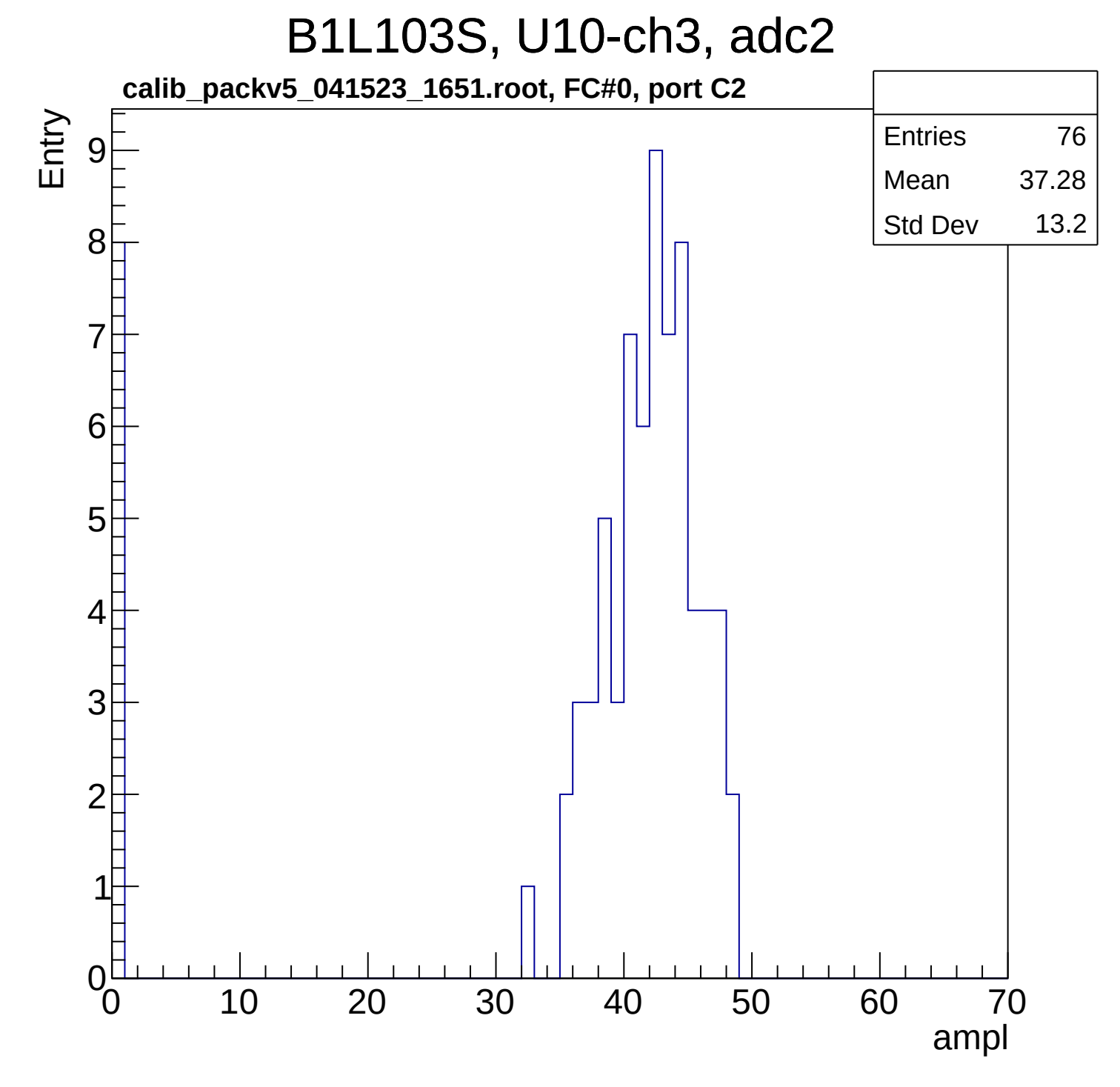
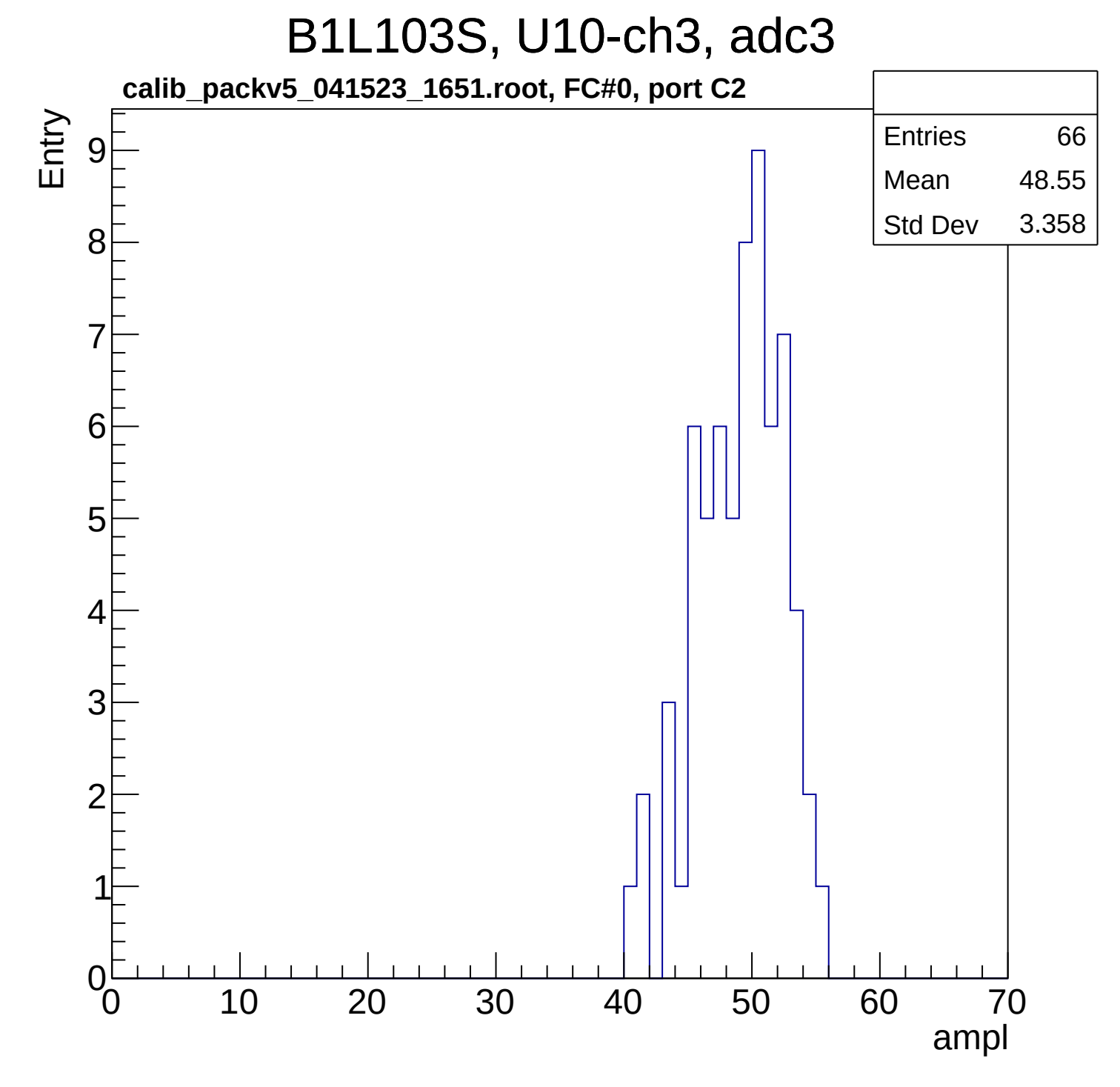
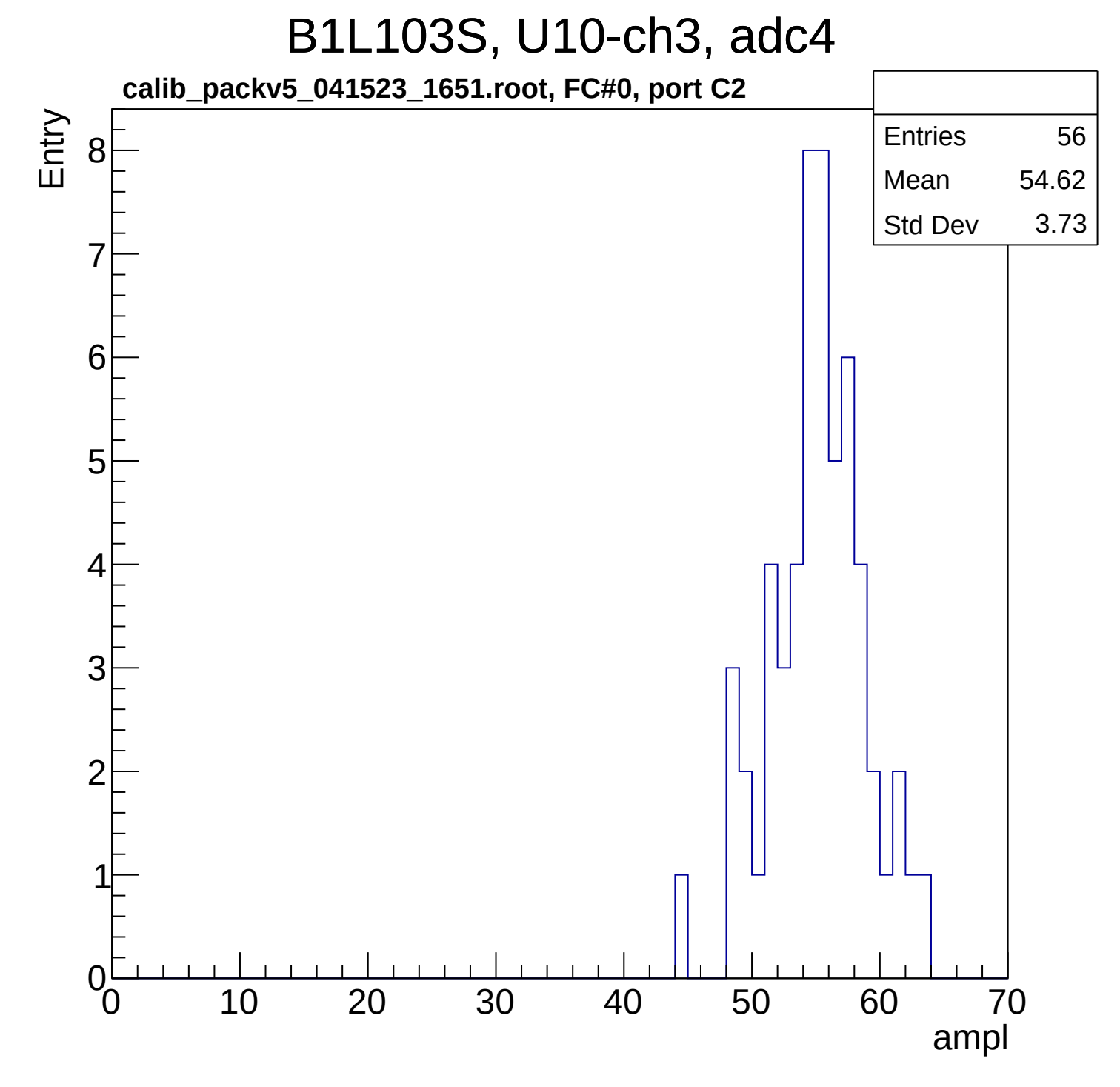
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70


B1L103S, U10-ch3, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 32.36
Std Dev 10.44
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U10-ch3, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 37.28
Std Dev 13.2
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U10-ch3, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 48.55
Std Dev 3.358
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U10-ch3, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 54.62
Std Dev 3.73
Entry
ampl
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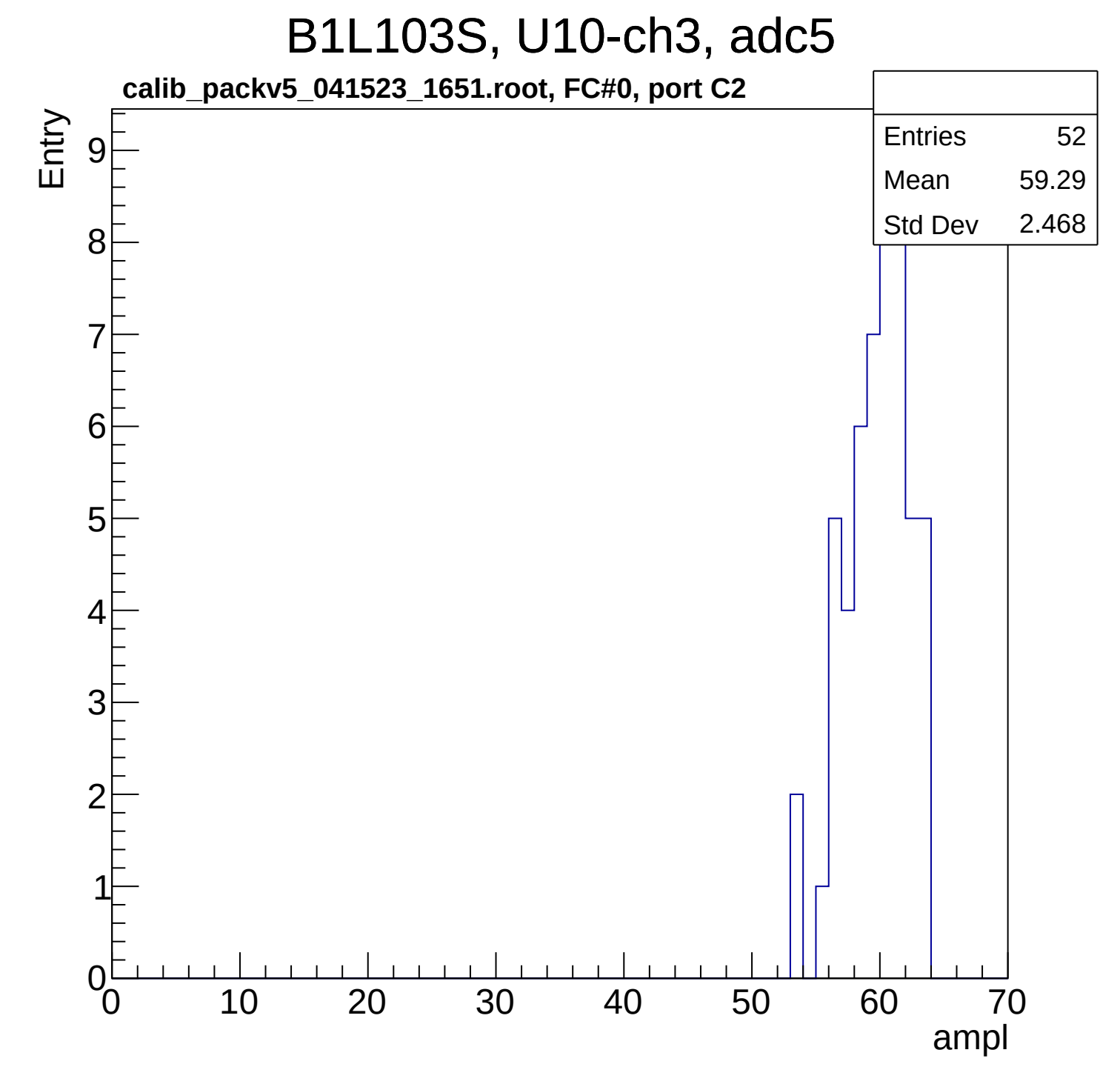
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U10-ch3, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 59.29
Std Dev 2.468
Entry
ampl
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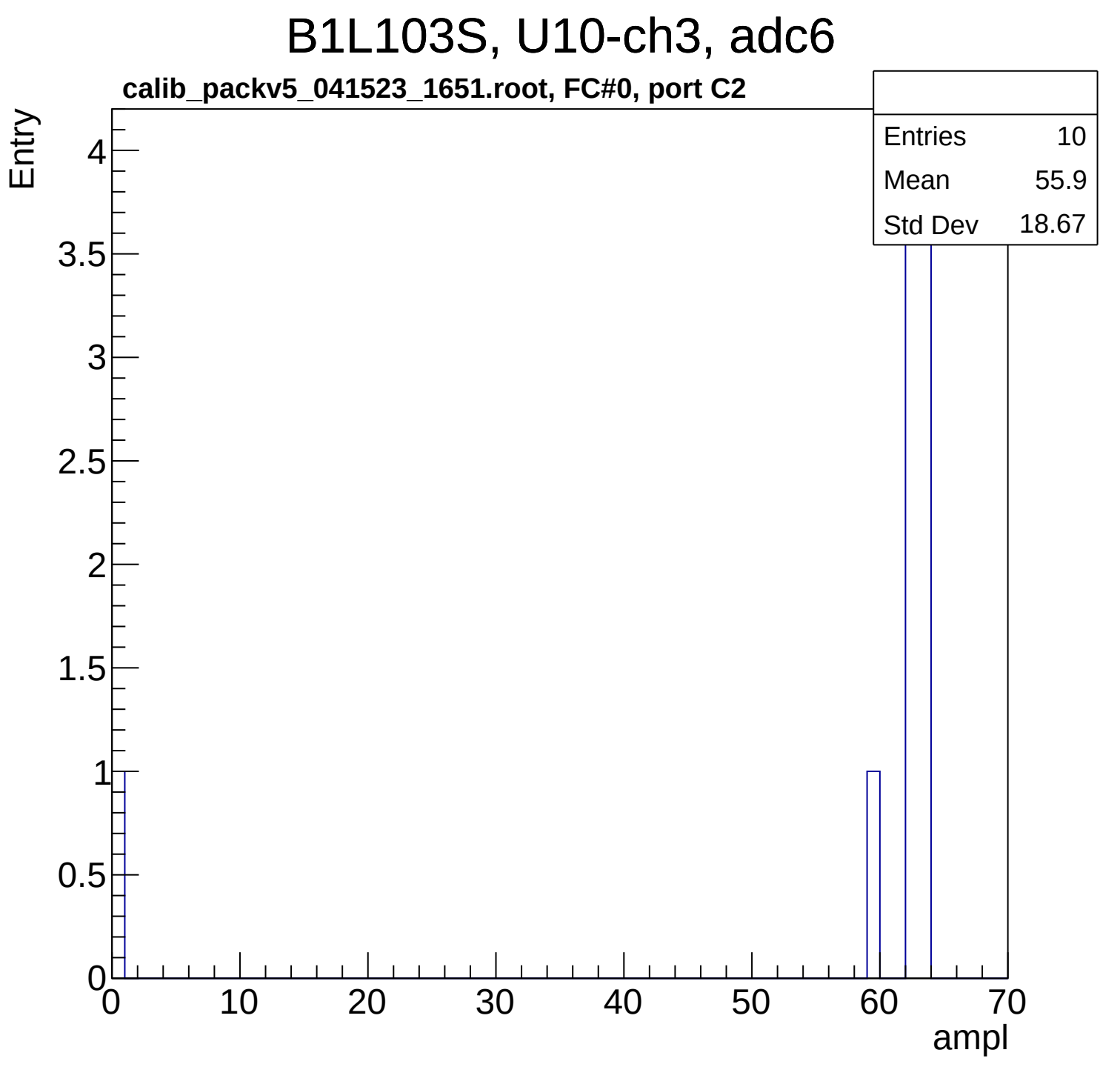
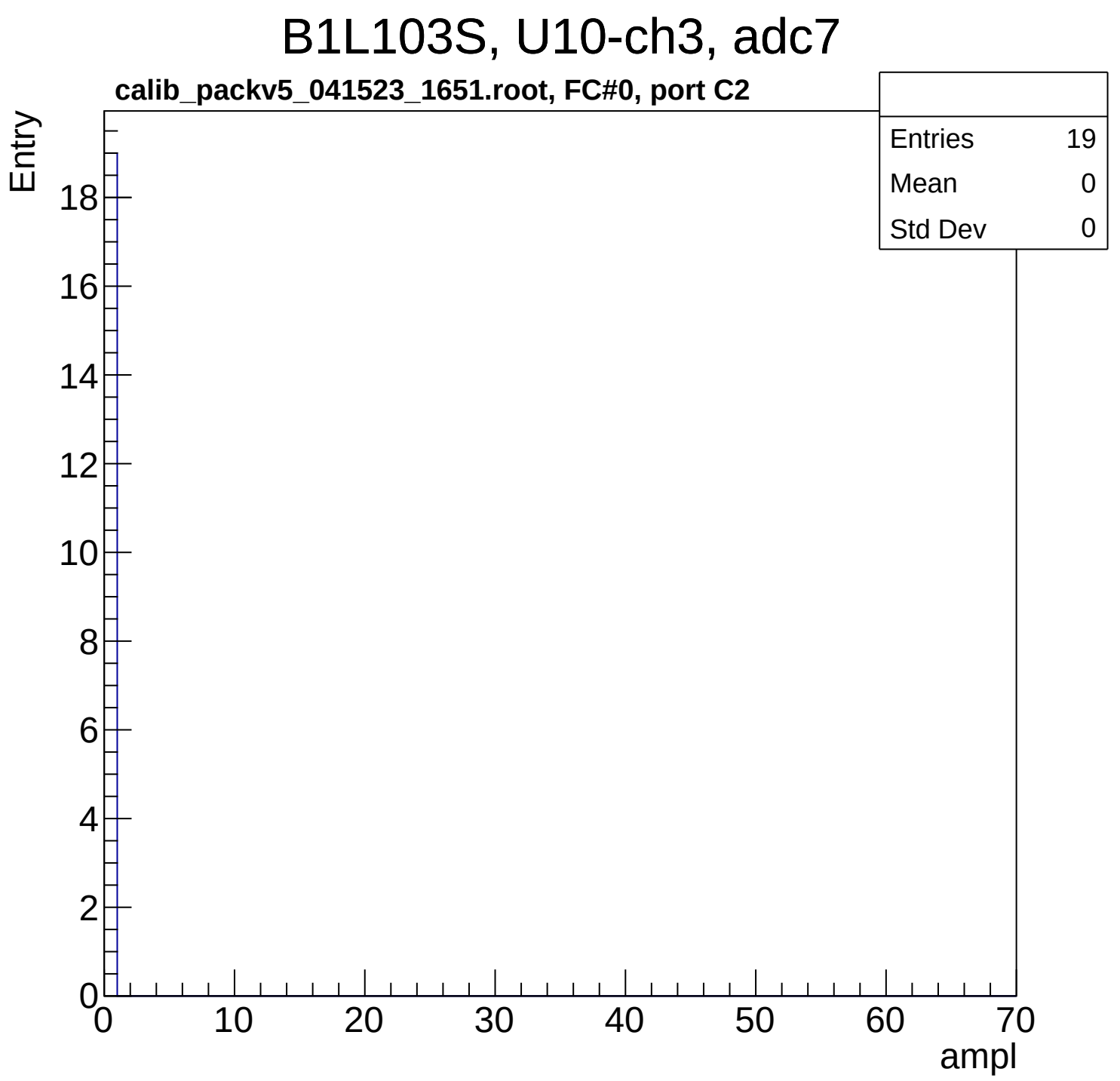
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U10-ch3, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 55.9
Std Dev 18.67
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U10-ch3, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
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10
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50
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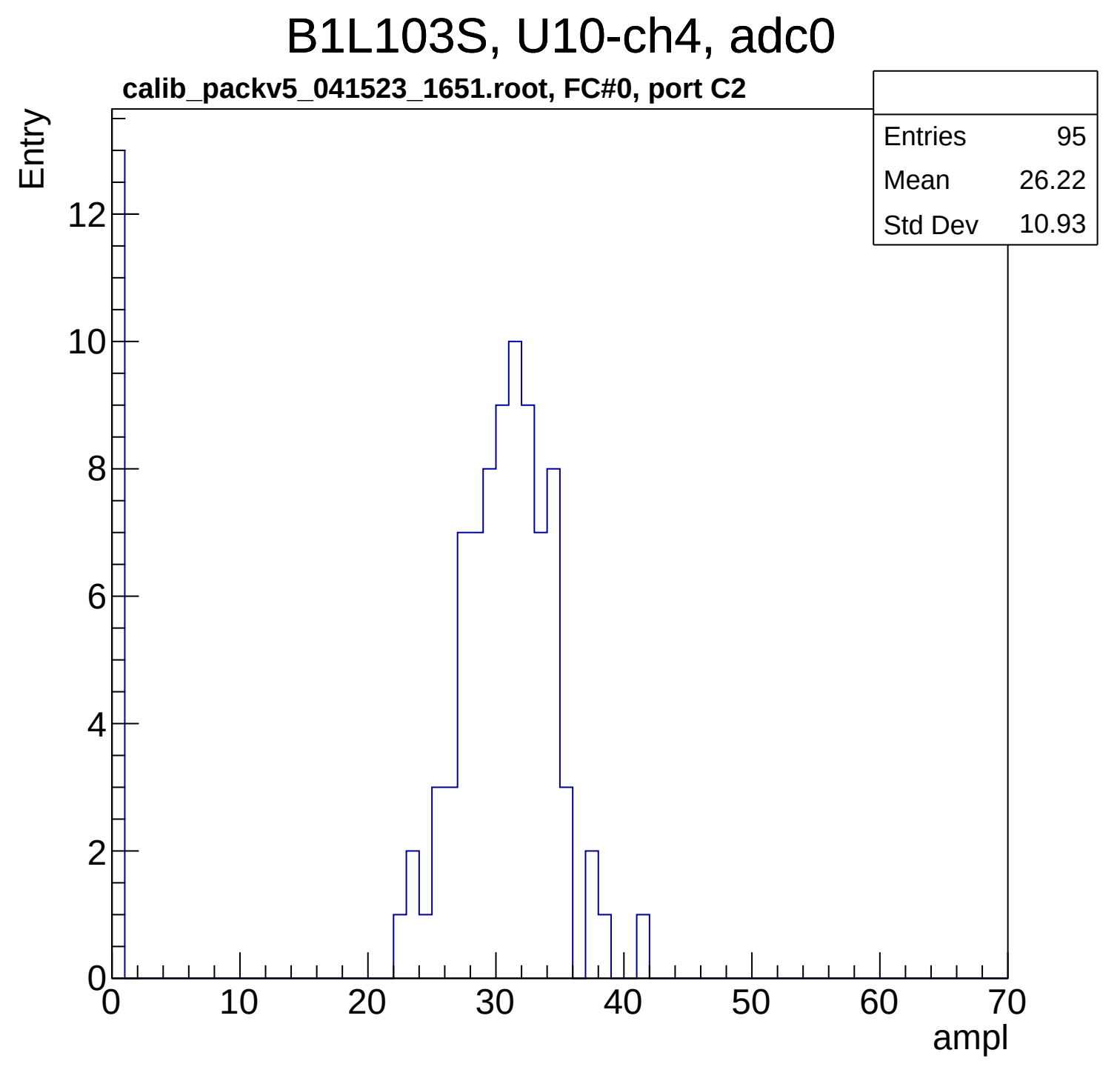
70
ampl


B1L103S, U10-ch4, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 95
Mean 26.22
Std Dev 10.93
Entry
0
2
4
6
8
10
12
0
10
20
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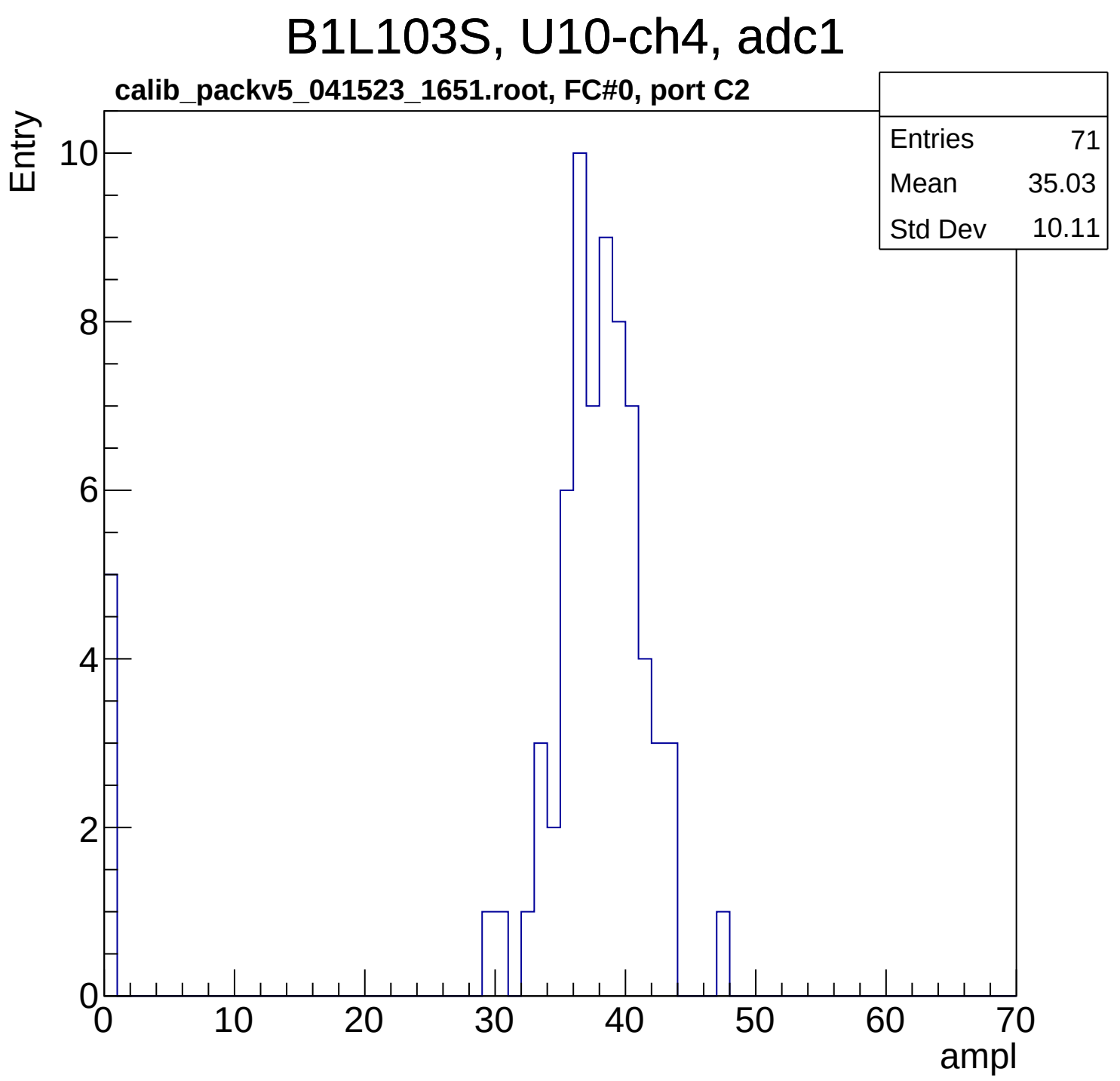
40
50
60
70
ampl


B1L103S, U10-ch4, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 35.03
Std Dev 10.11
Entry
ampl
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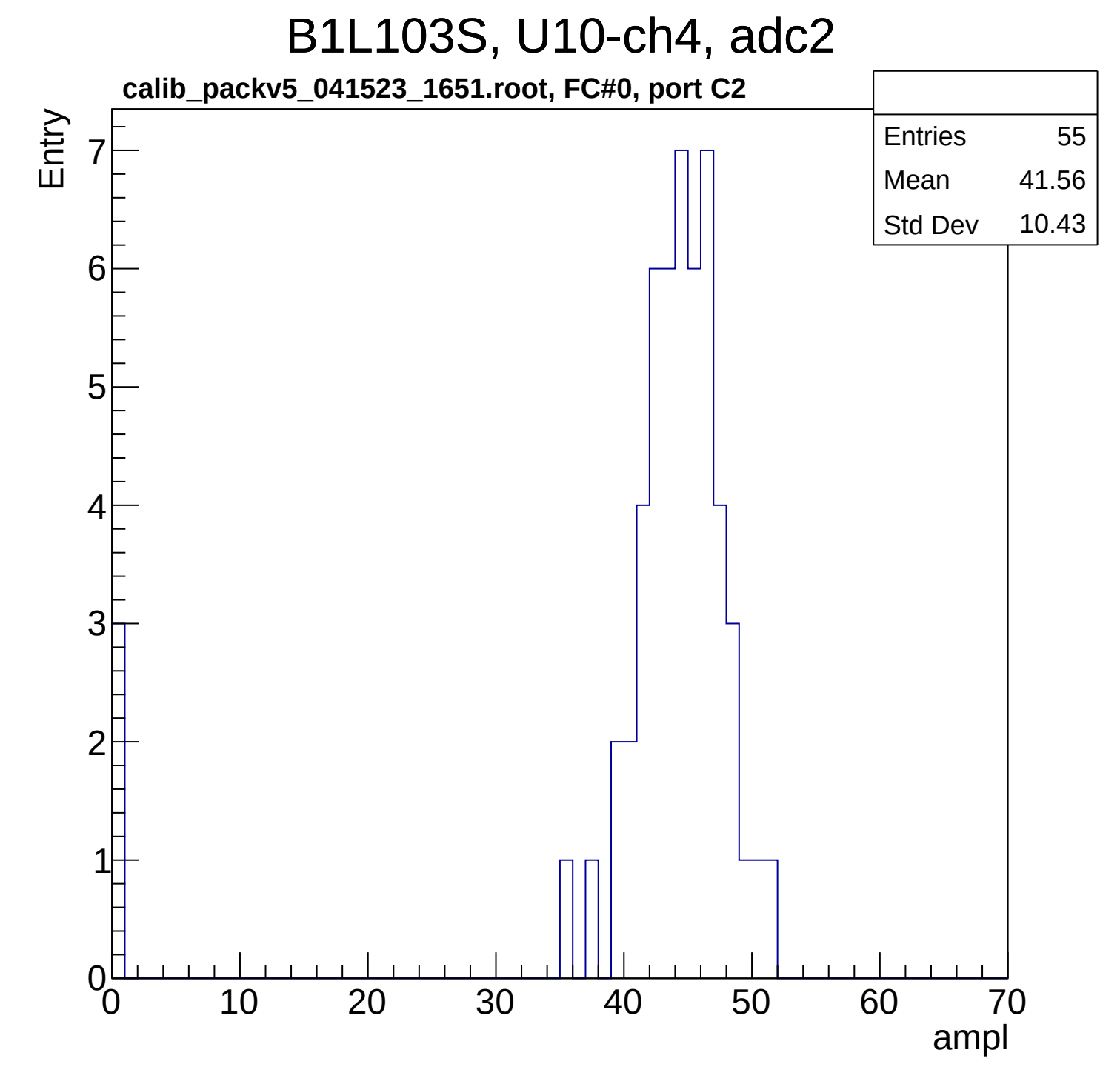
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U10-ch4, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 41.56
Std Dev 10.43
Entry
ampl
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2
3
4
5
6
7
0
10
20
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40
50
60
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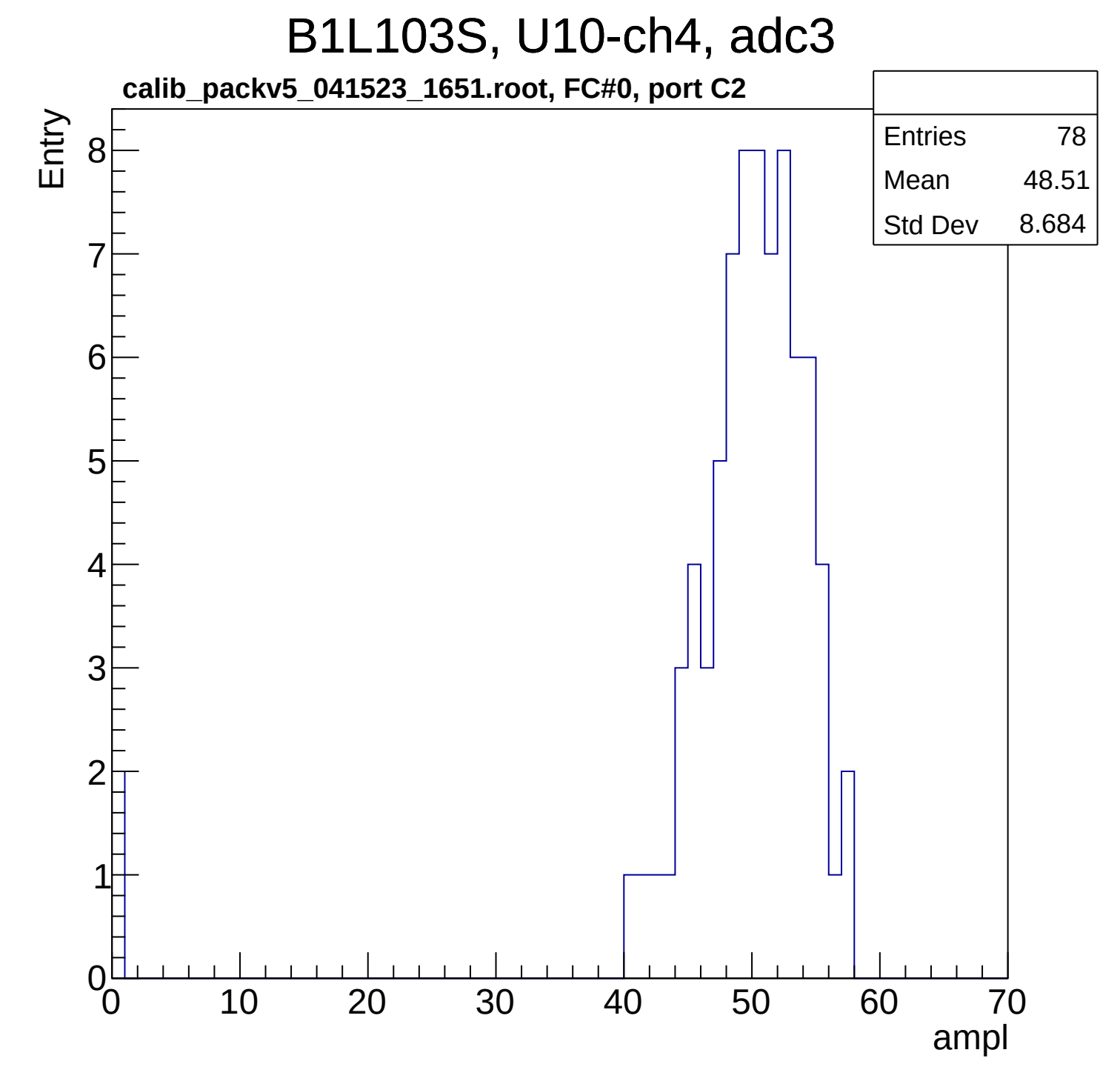
B1L103S, U10-ch4, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 48.51
Std Dev 8.684
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
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60
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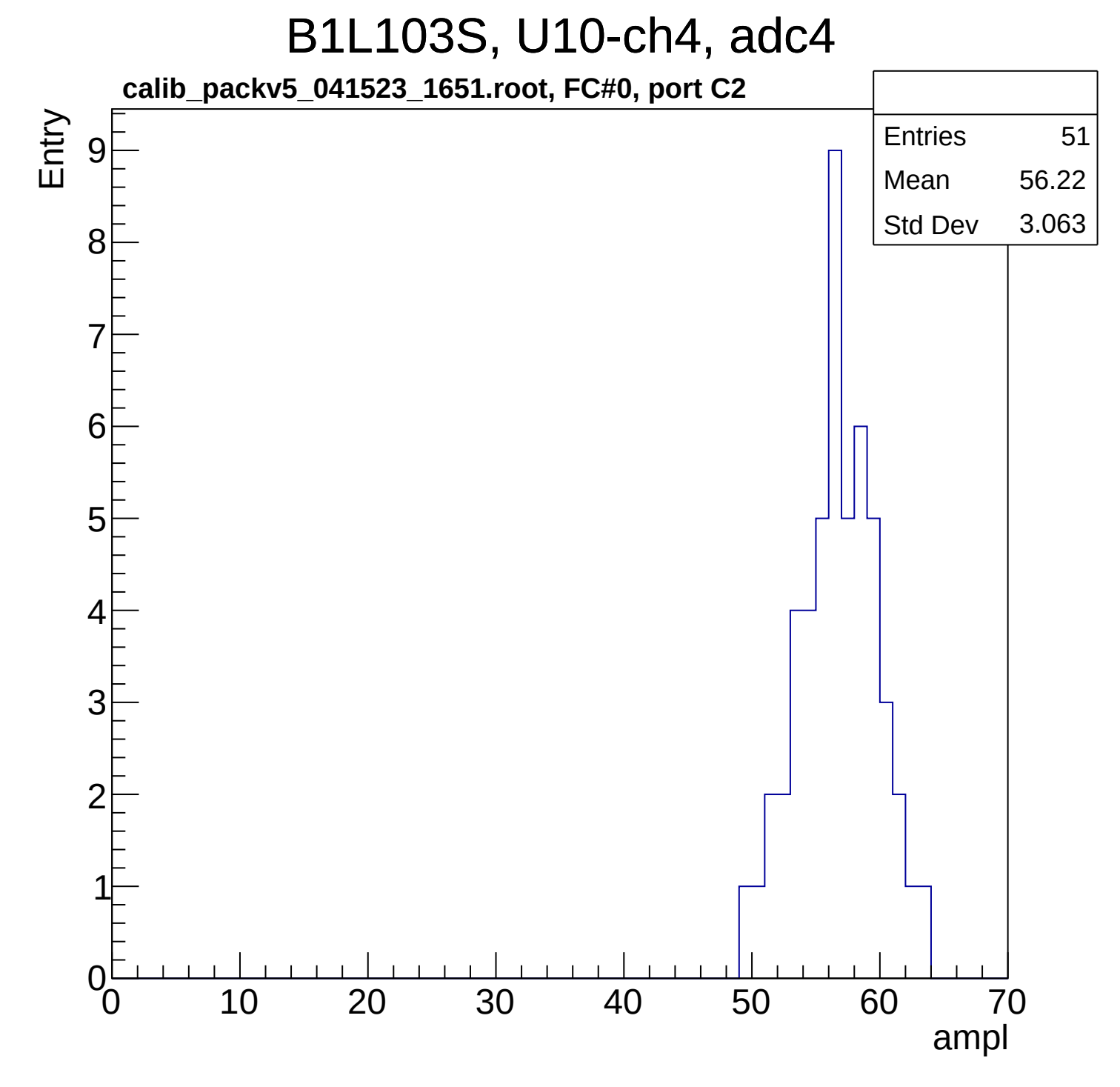
B1L103S, U10-ch4, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 56.22
Std Dev 3.063
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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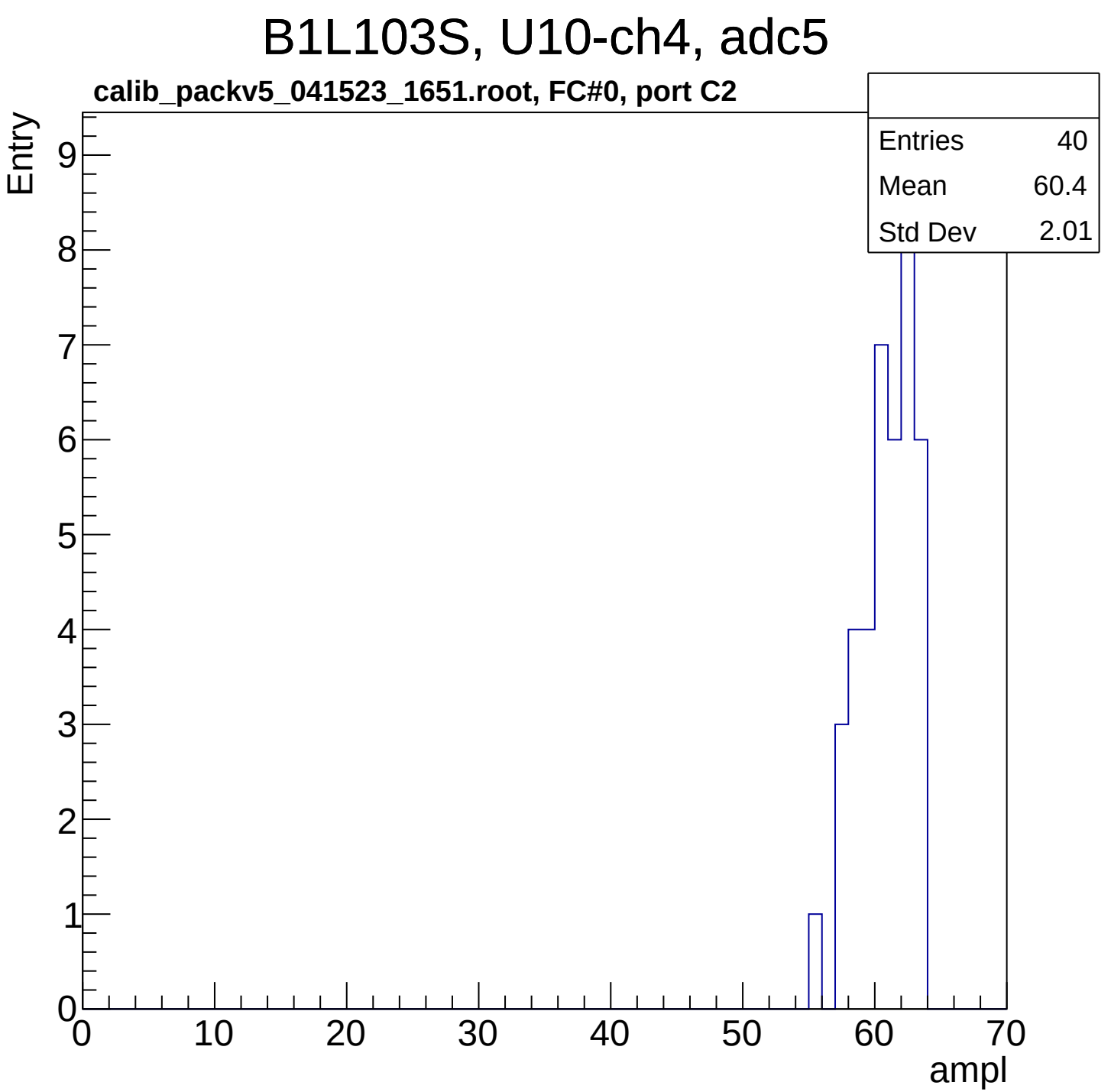
B1L103S, U10-ch4, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 40
Mean 60.4
Std Dev 2.01
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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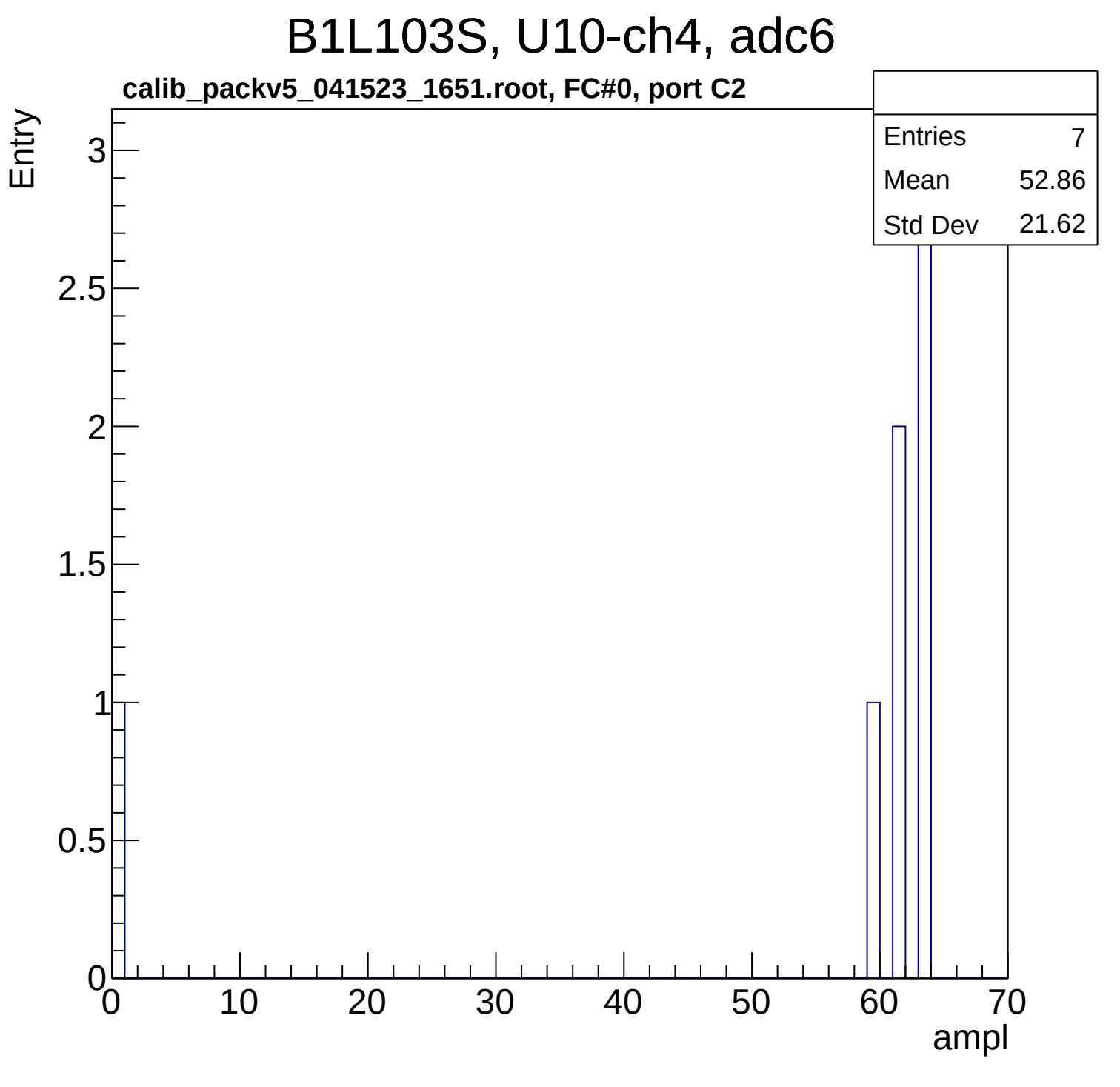
B1L103S, U10-ch4, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 52.86
Std Dev 21.62
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
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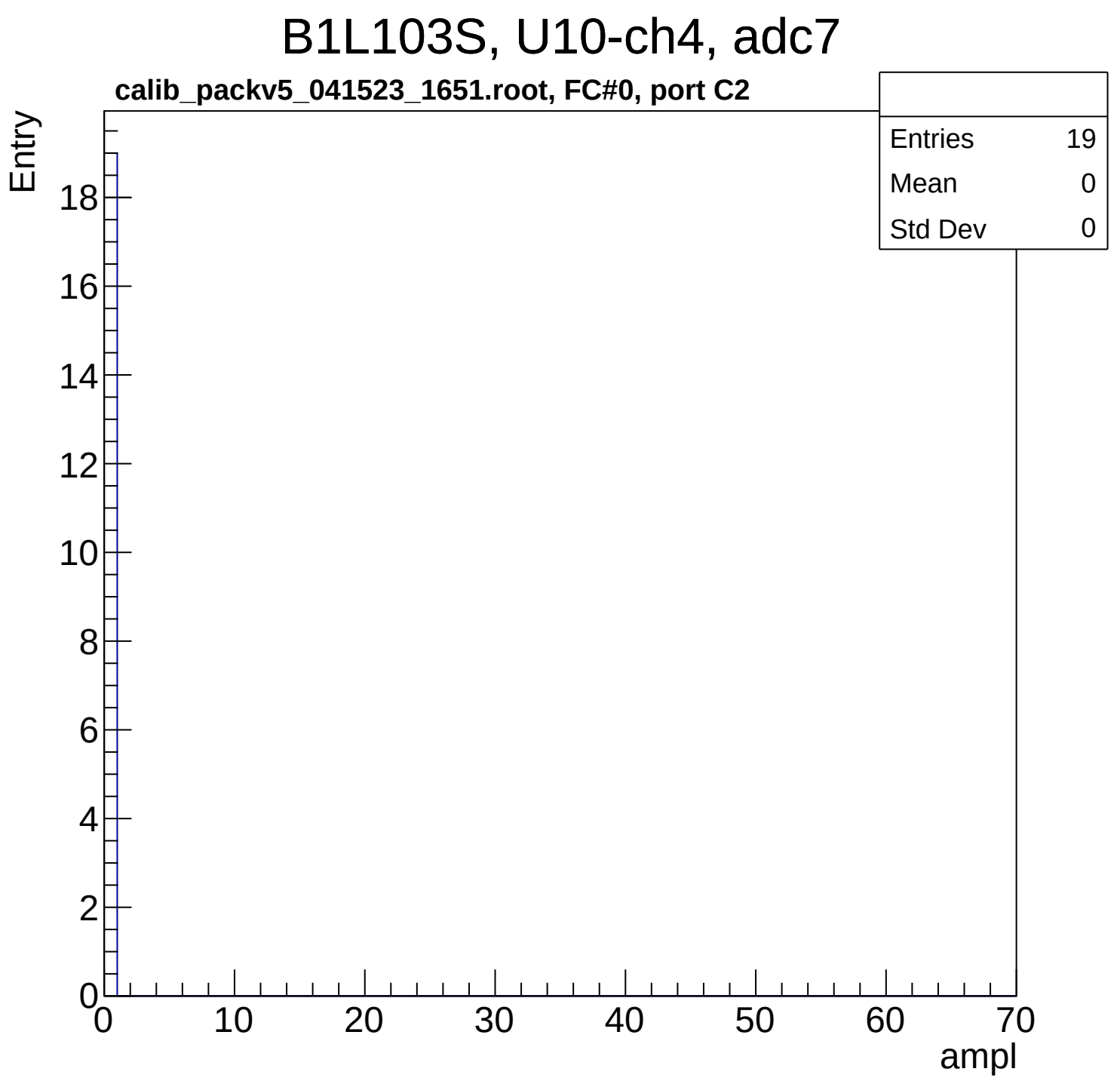
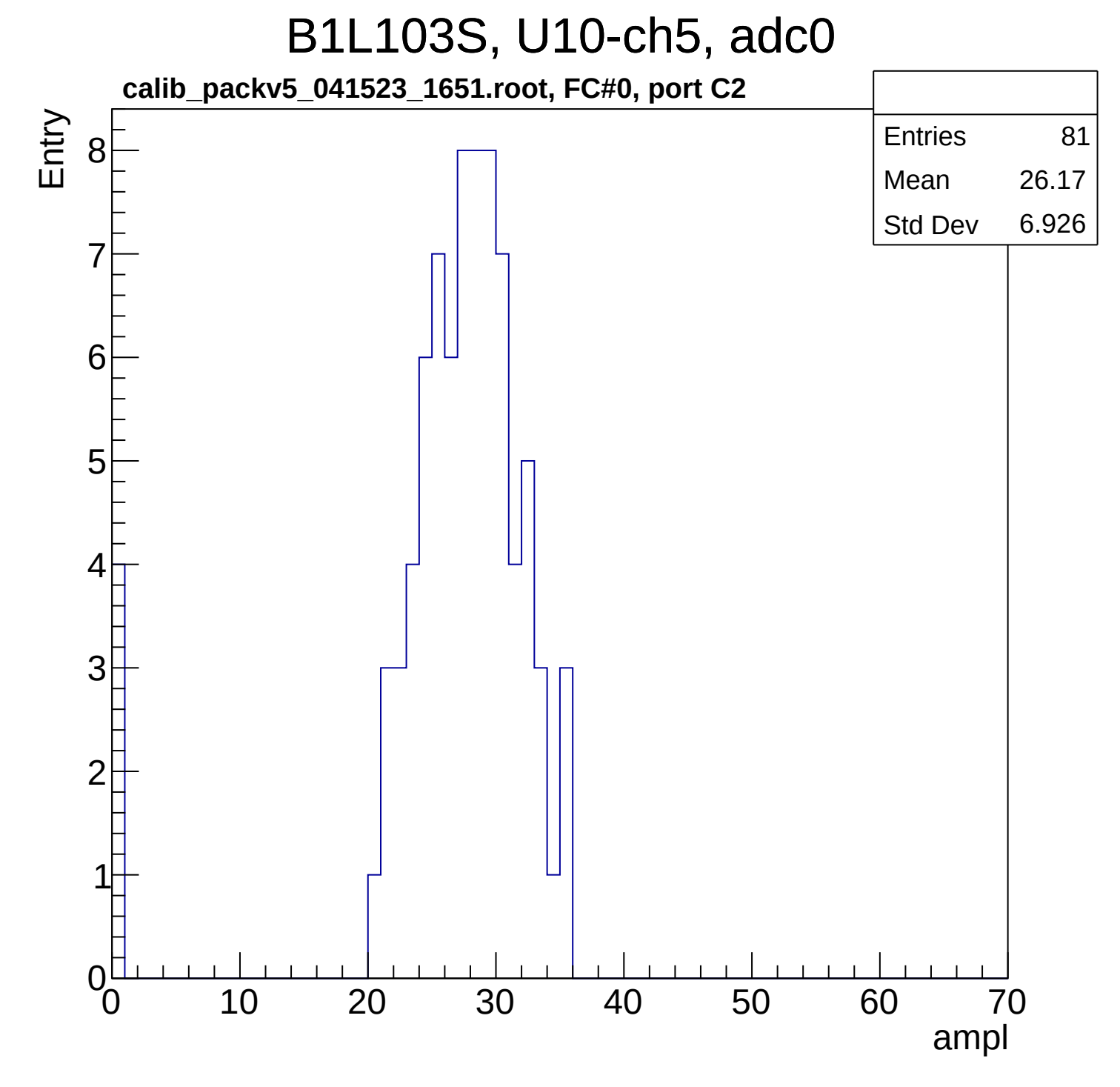

B1L103S, U10-ch4, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch5, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 26.17
Std Dev 6.926
Entry
ampl
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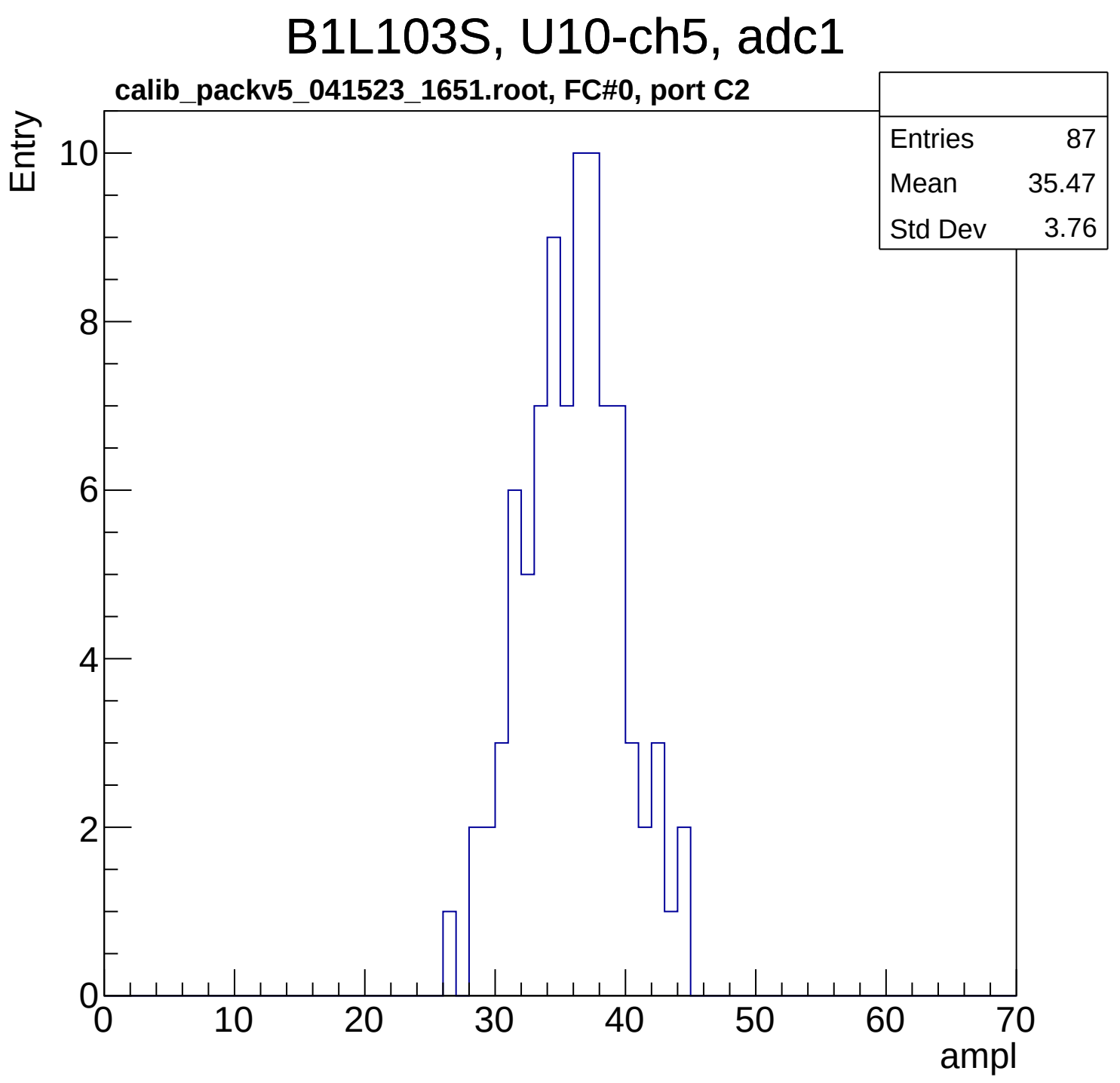
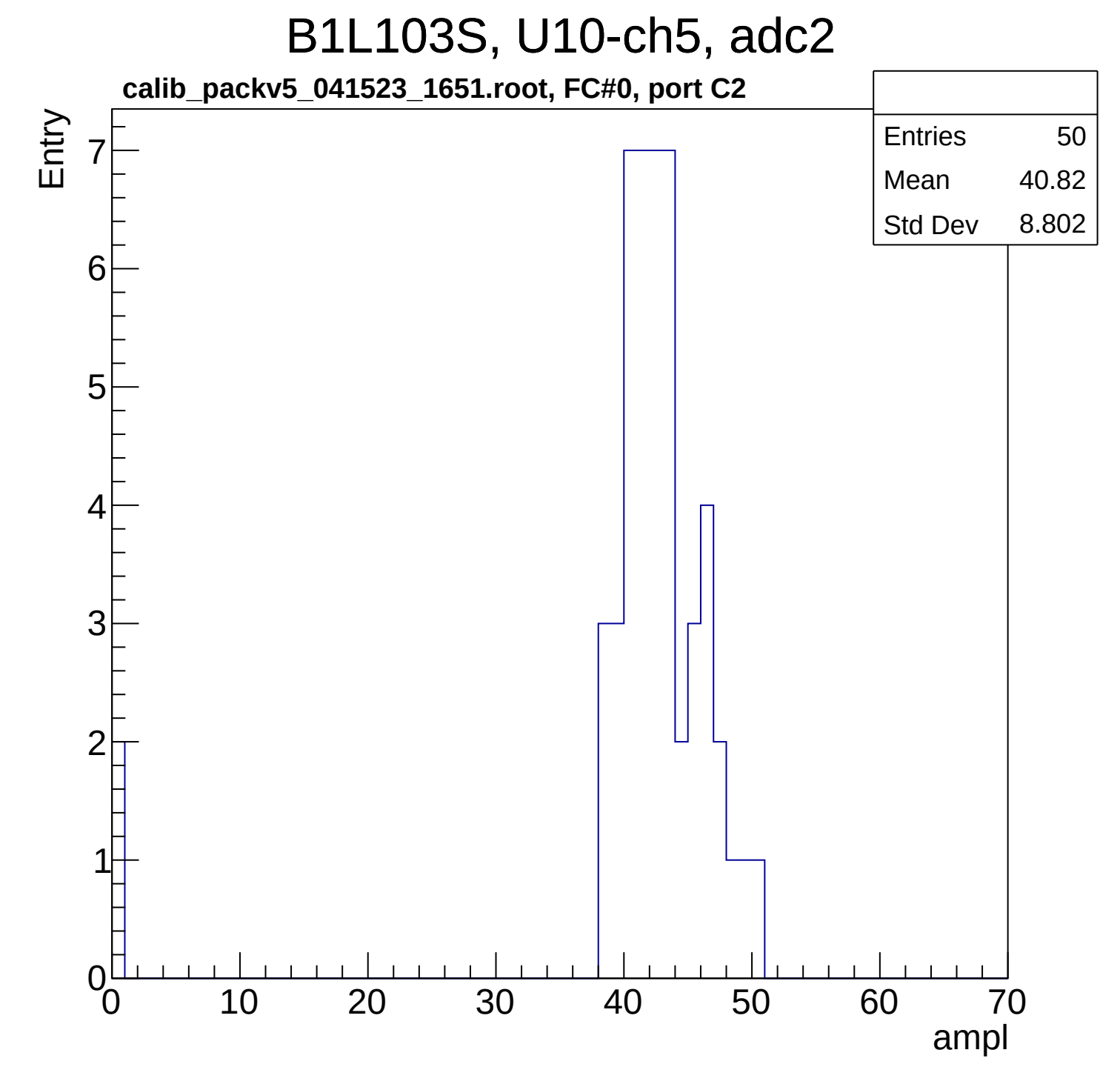
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U10-ch5, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 87
Mean 35.47
Std Dev 3.76
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U10-ch5, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 40.82
Std Dev 8.802
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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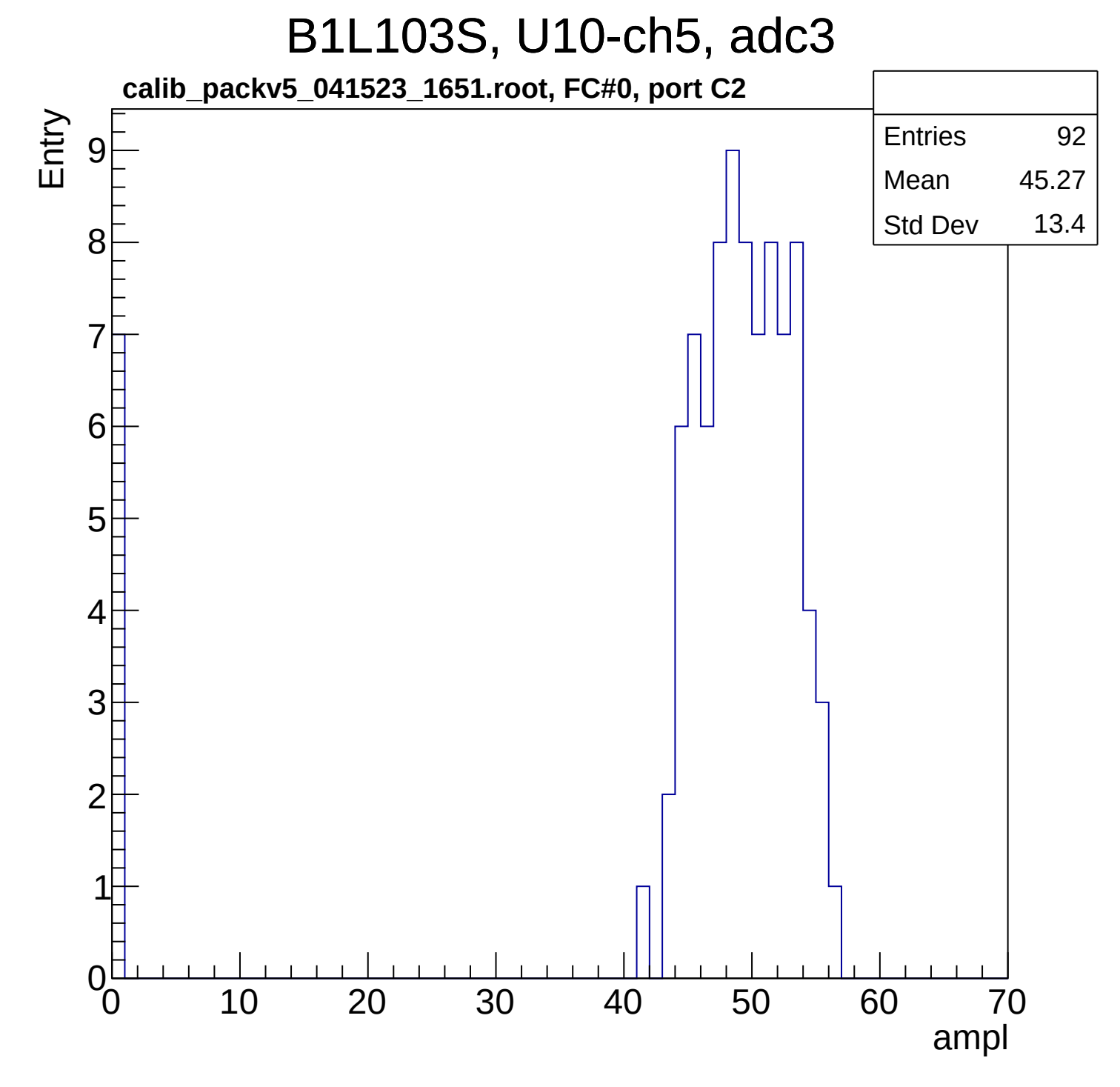
B1L103S, U10-ch5, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 92
Mean 45.27
Std Dev 13.4
Entry
ampl
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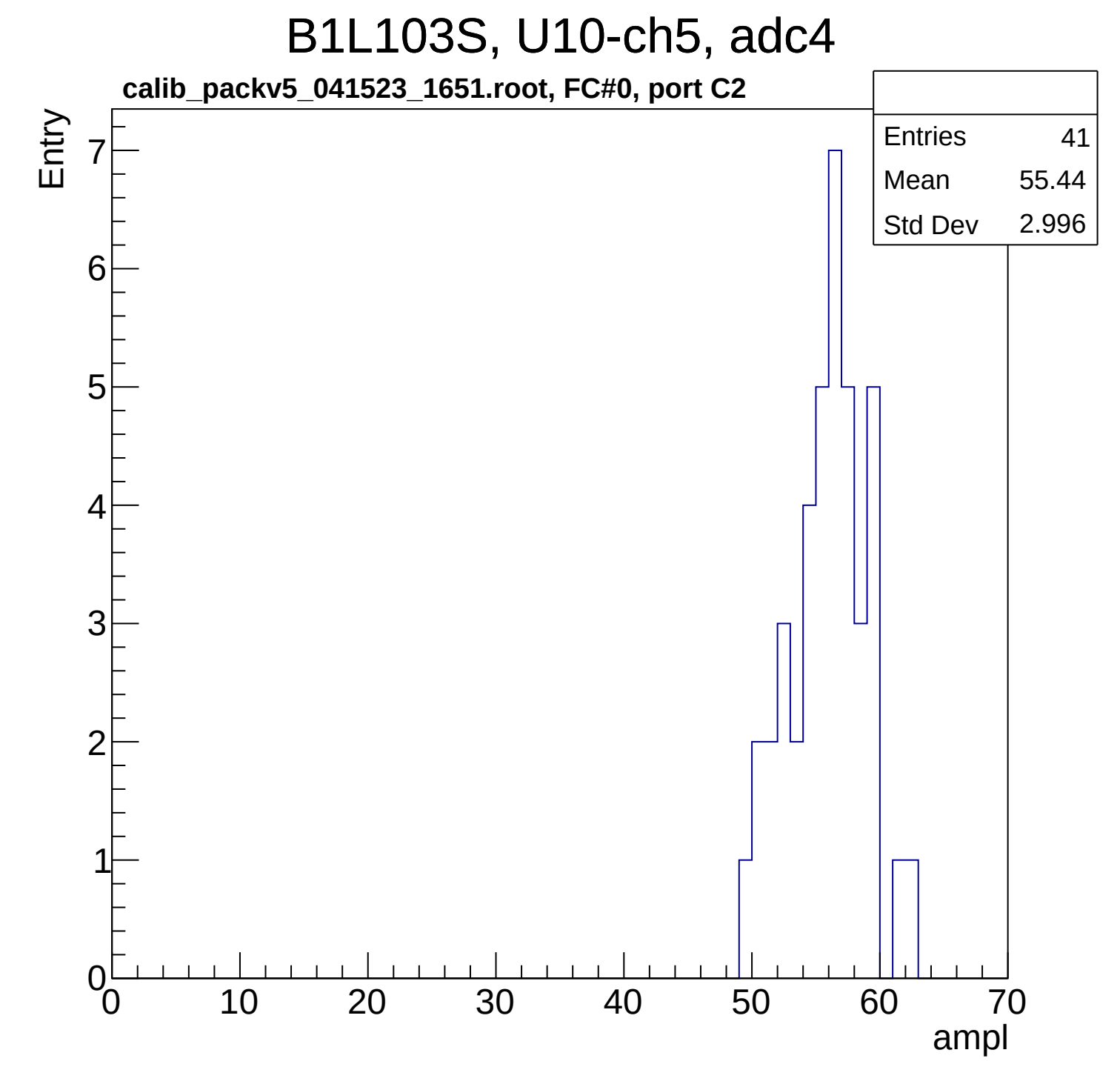
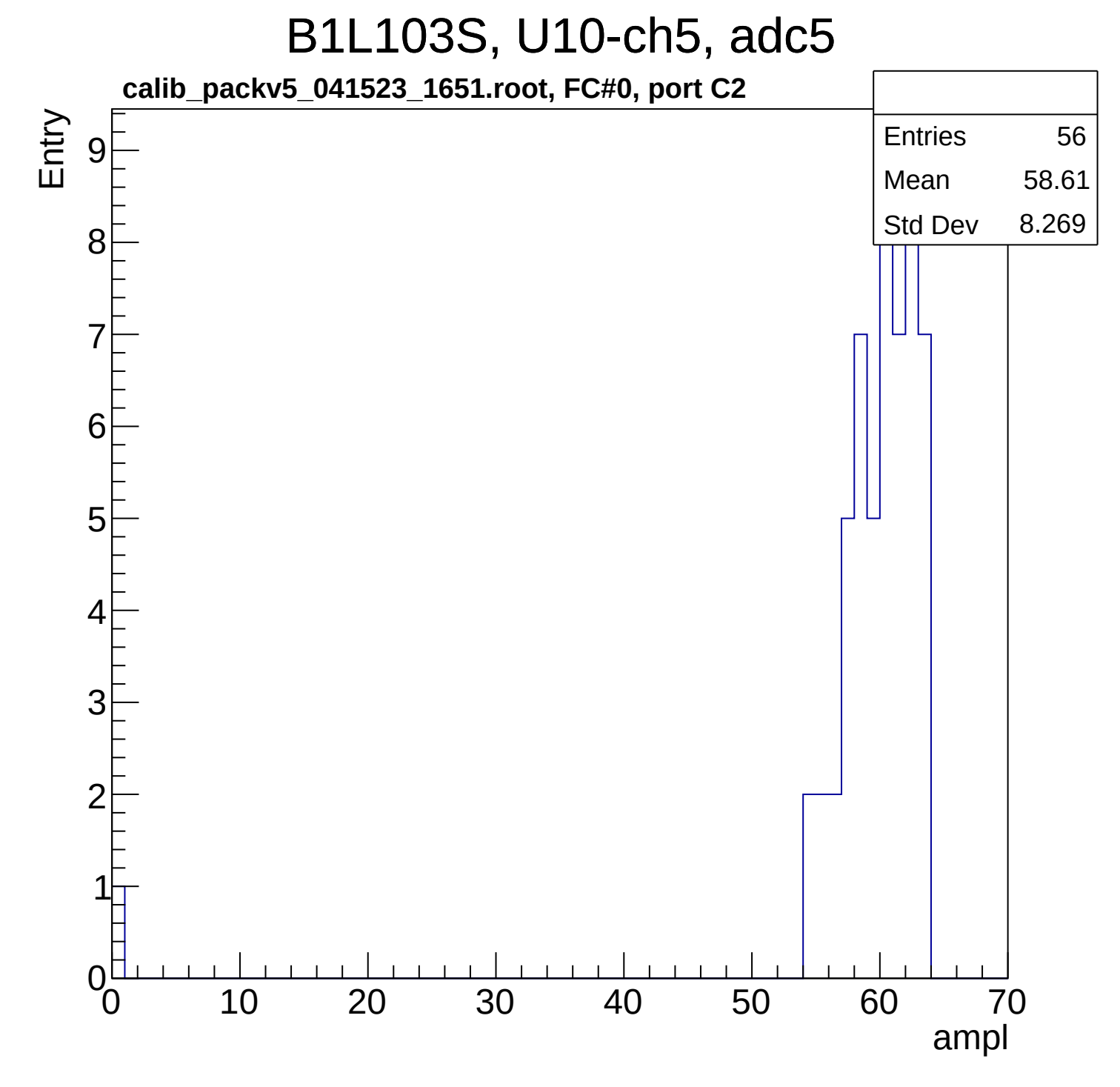
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U10-ch5, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 41
Mean 55.44
Std Dev 2.996
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U10-ch5, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 58.61
Std Dev 8.269
Entry
ampl
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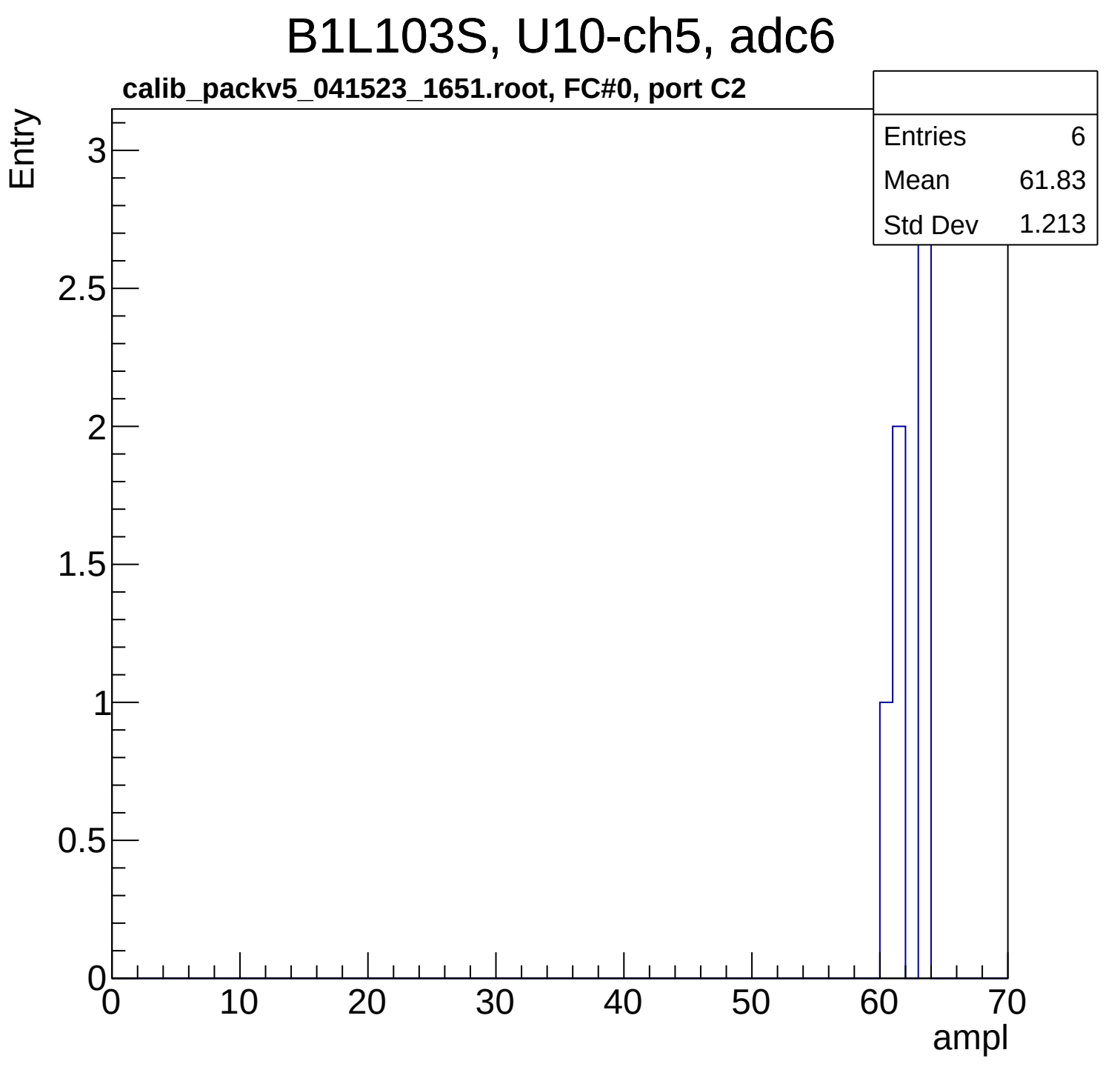
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U10-ch5, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 61.83
Std Dev 1.213
Entry
ampl
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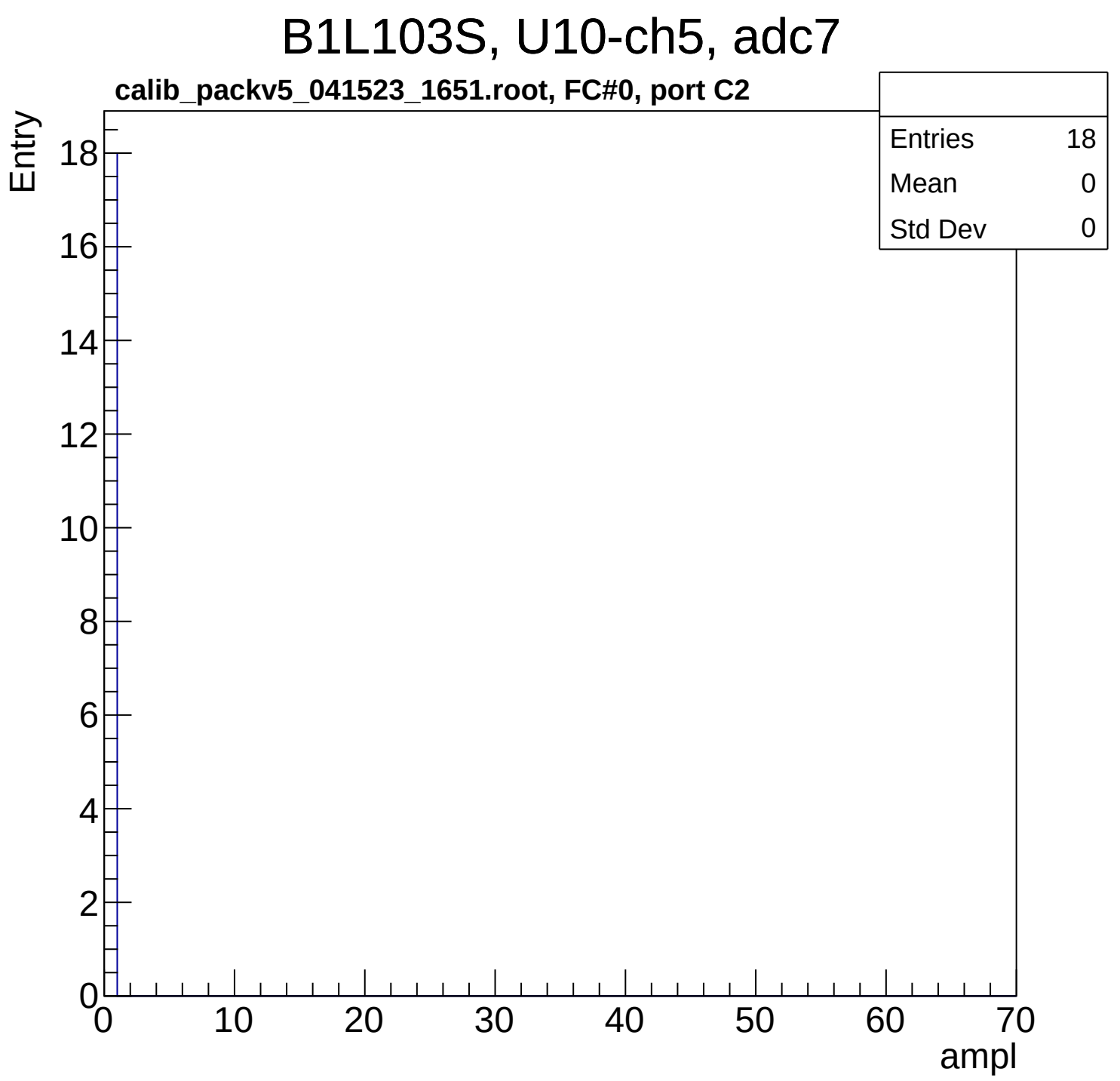
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U10-ch5, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
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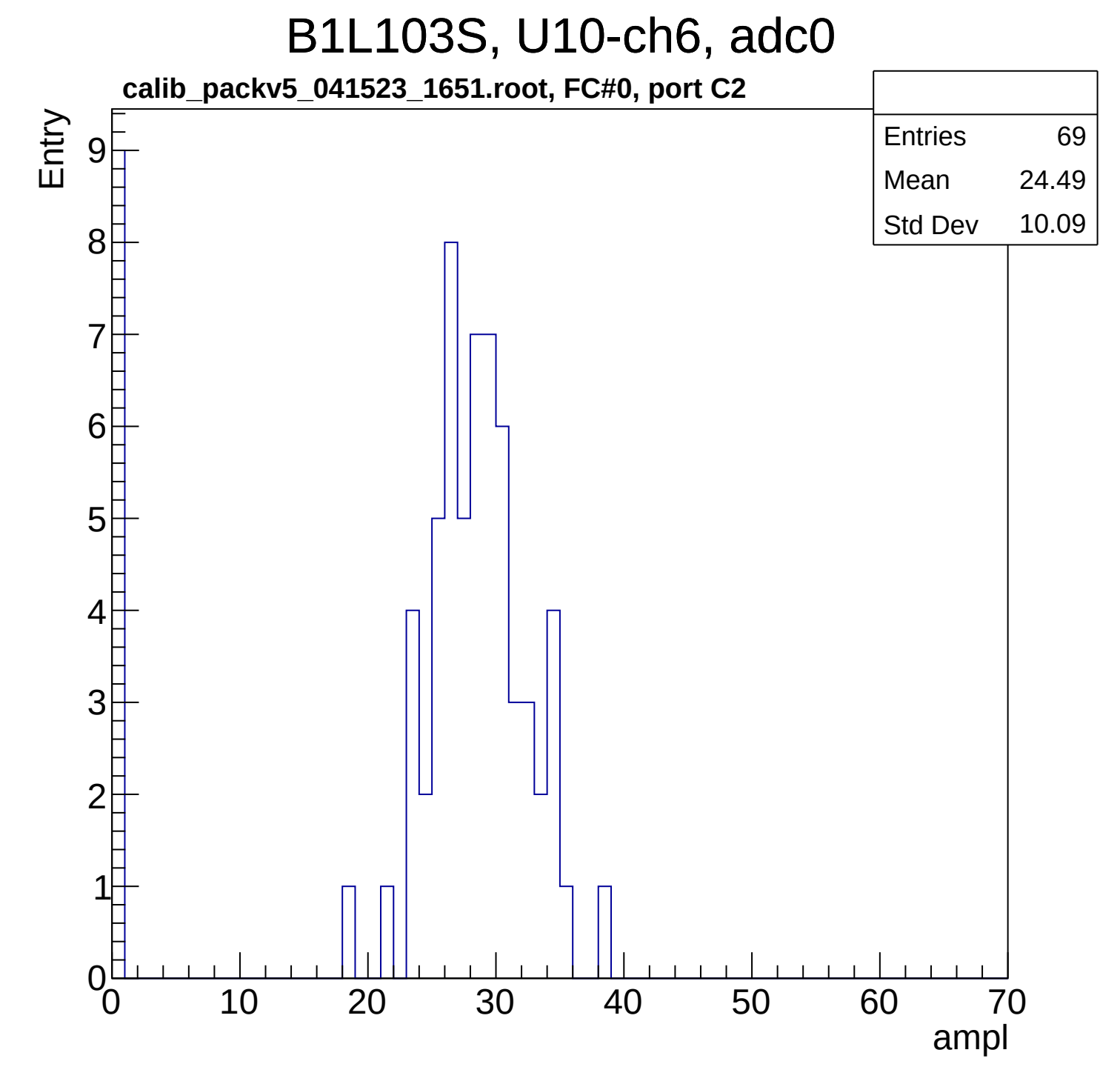
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch6, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 24.49
Std Dev 10.09
Entry
ampl
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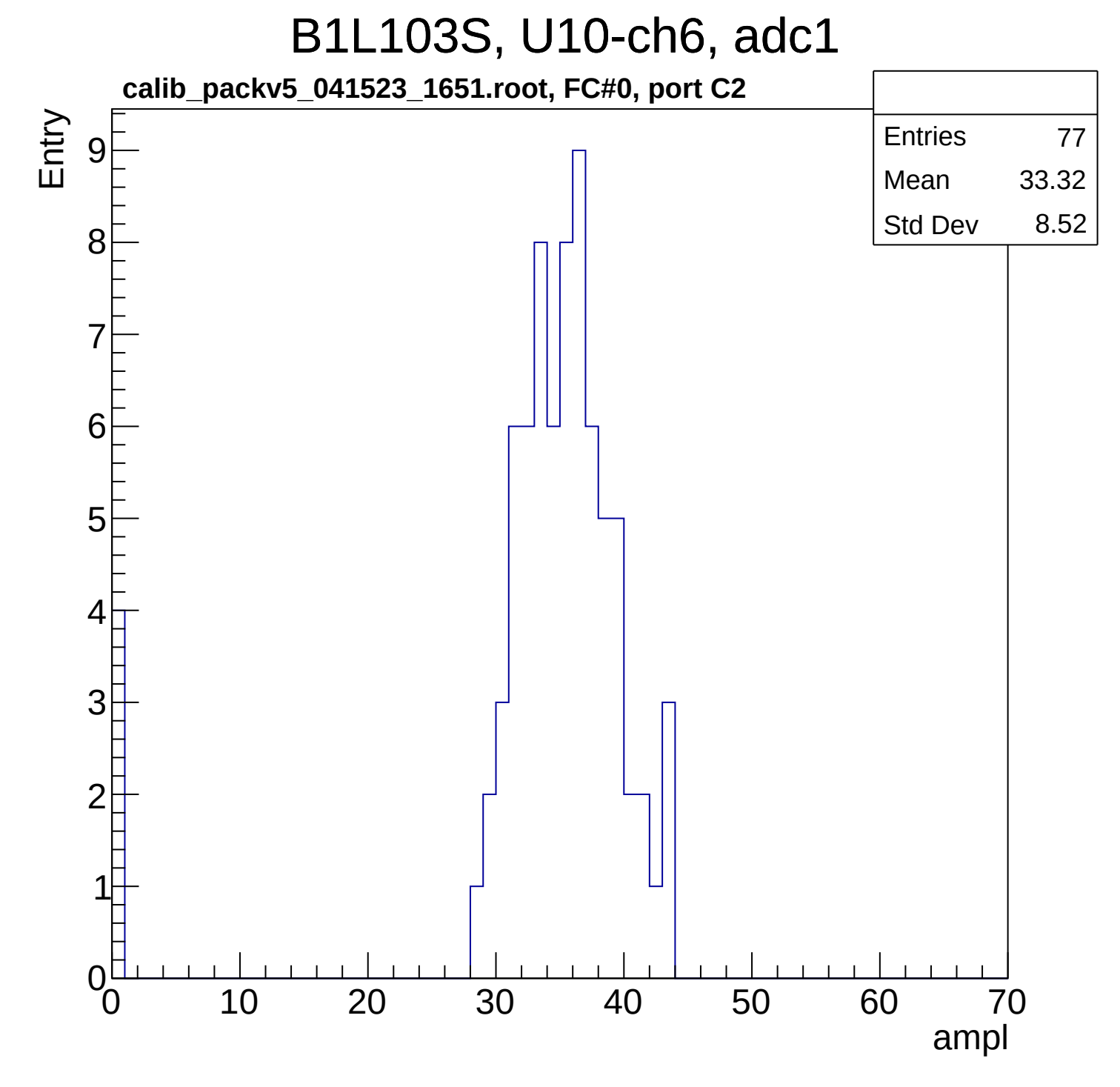
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U10-ch6, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 33.32
Std Dev 8.52
Entry
ampl
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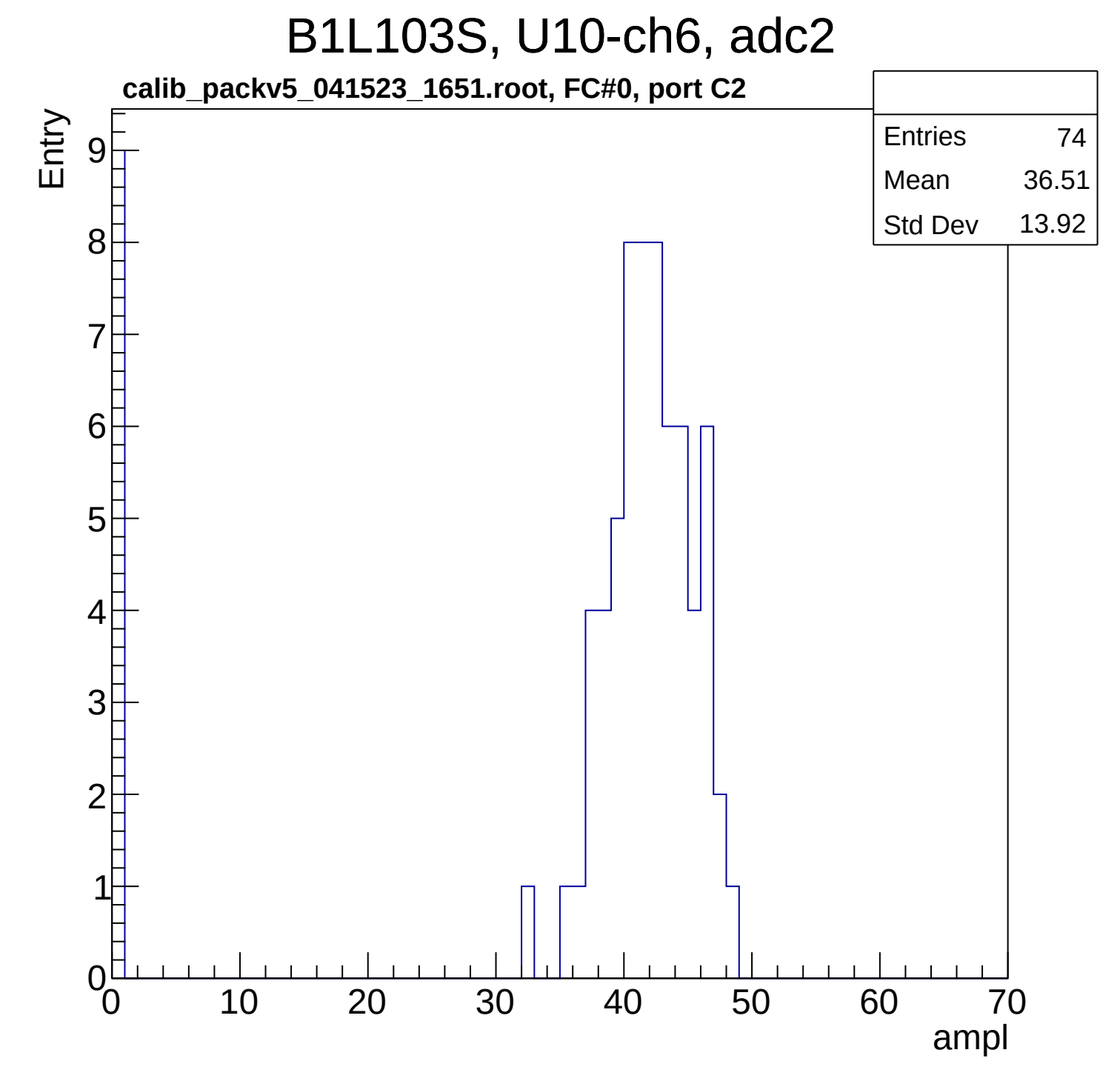
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U10-ch6, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 36.51
Std Dev 13.92
Entry
ampl
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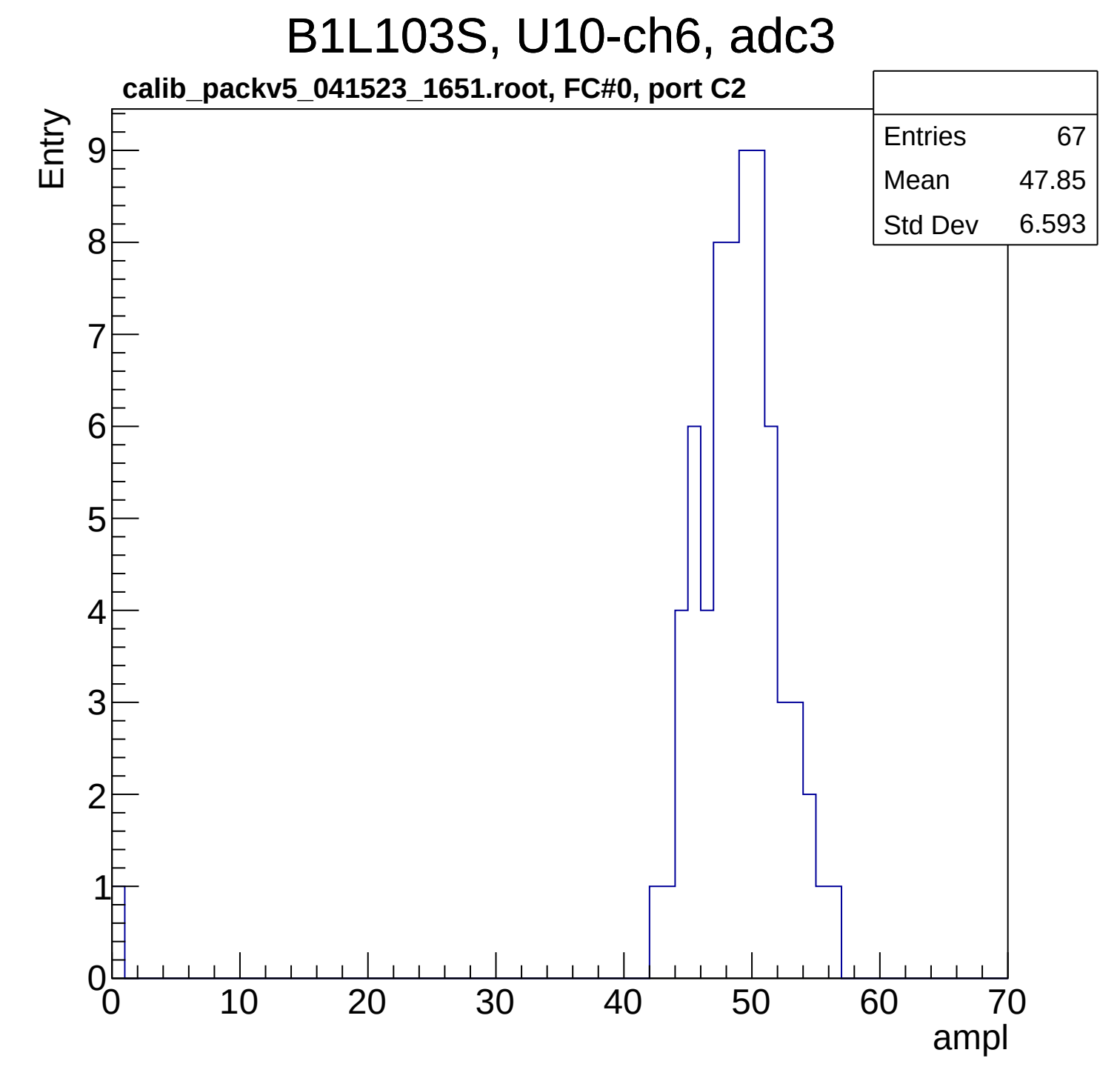
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U10-ch6, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 47.85
Std Dev 6.593
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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40
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60
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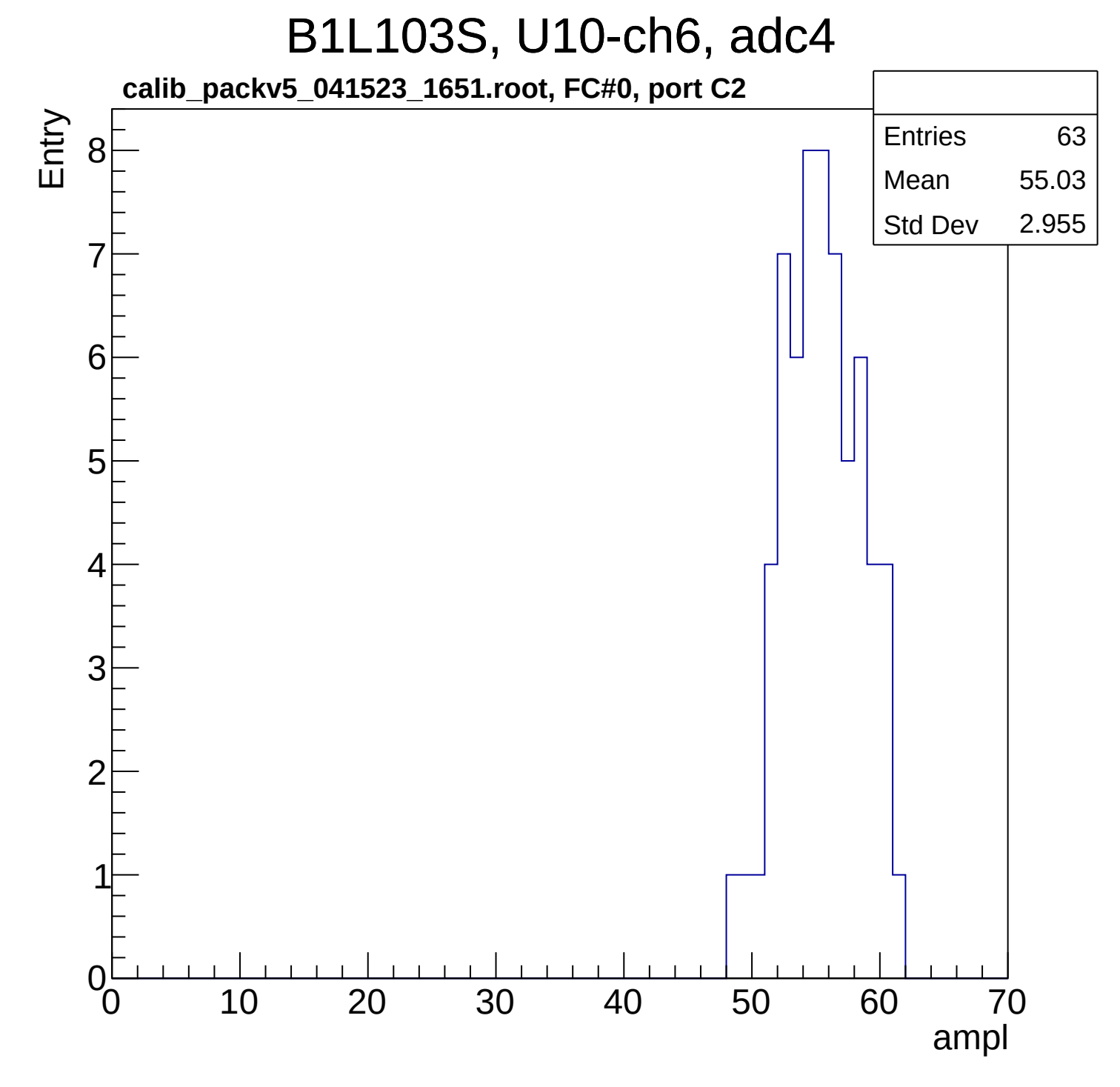
B1L103S, U10-ch6, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 55.03
Std Dev 2.955
Entry
ampl
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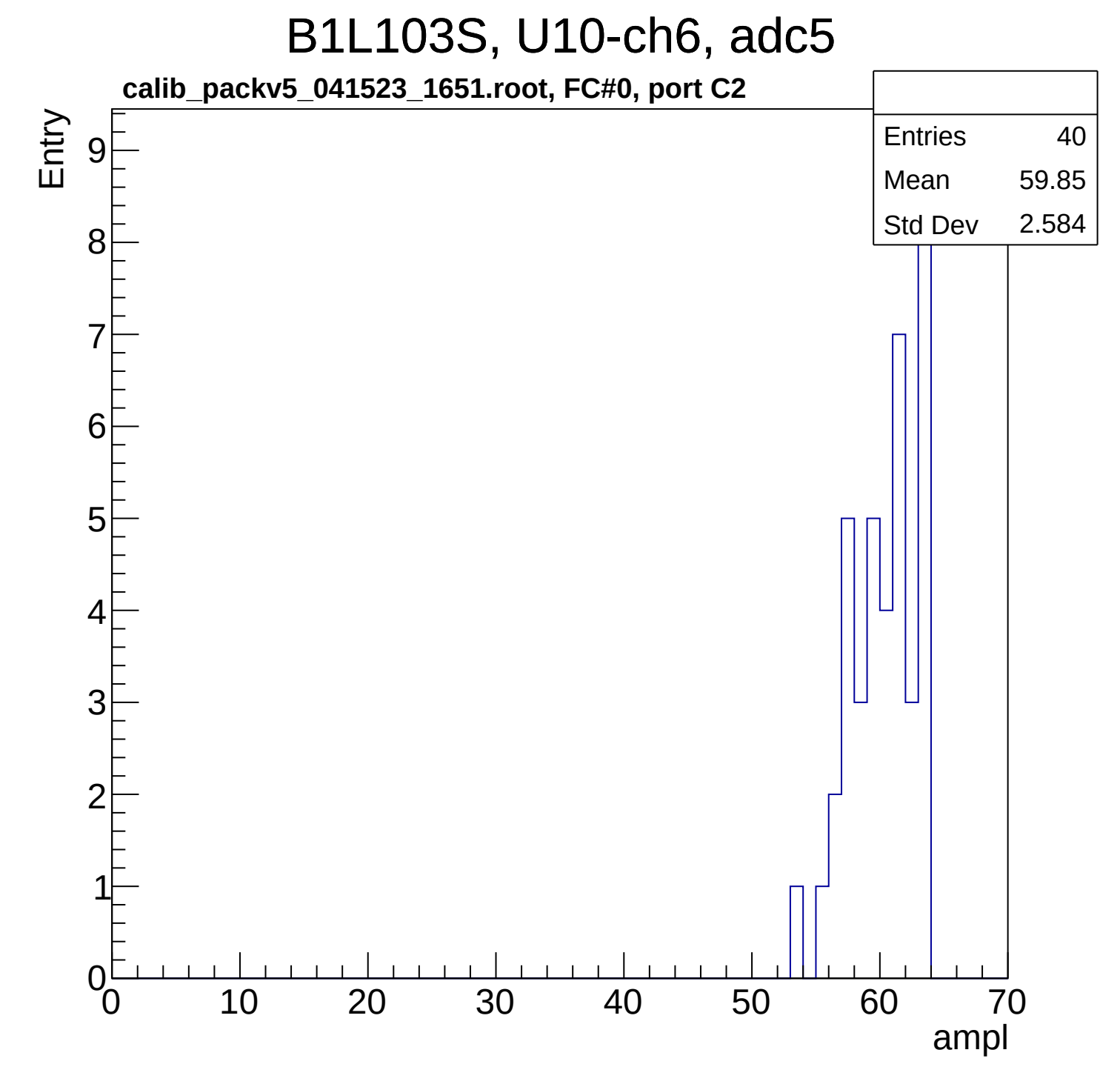
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U10-ch6, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 40
Mean 59.85
Std Dev 2.584
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
50
60
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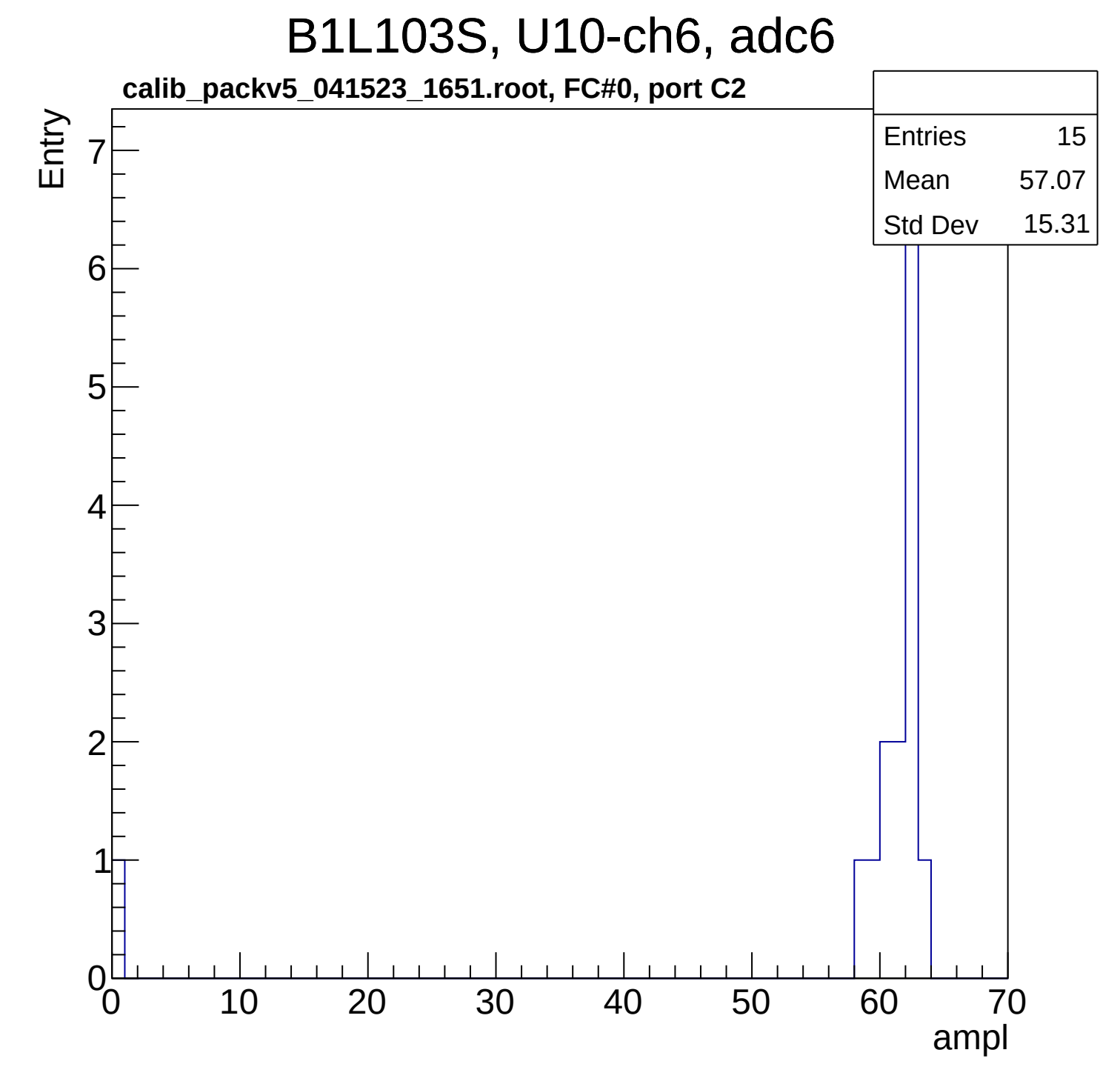
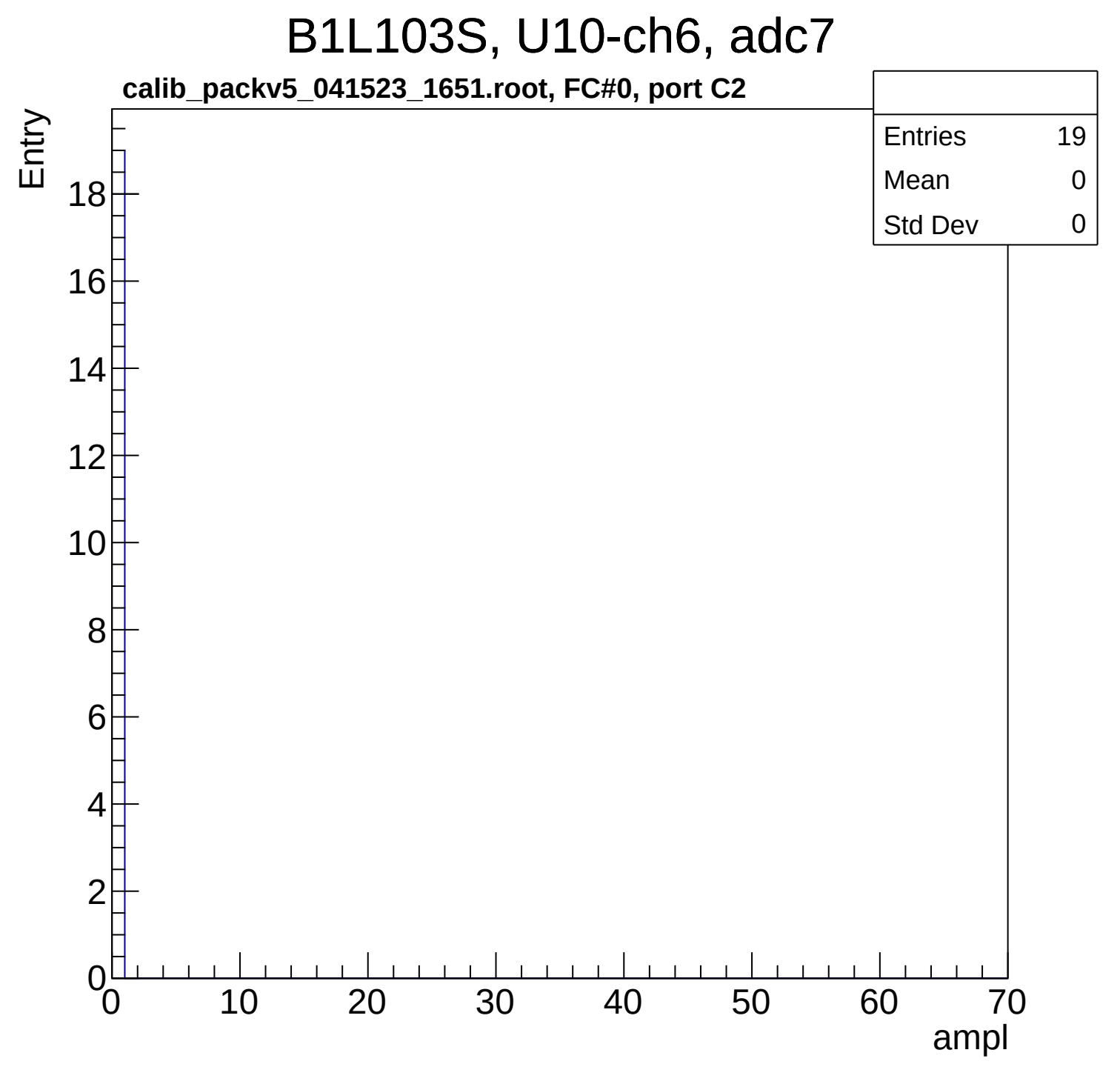

B1L103S, U10-ch6, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 15
Mean 57.07
Std Dev 15.31
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U10-ch6, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
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4
6
8
10
12
14
16
18
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10
20
30
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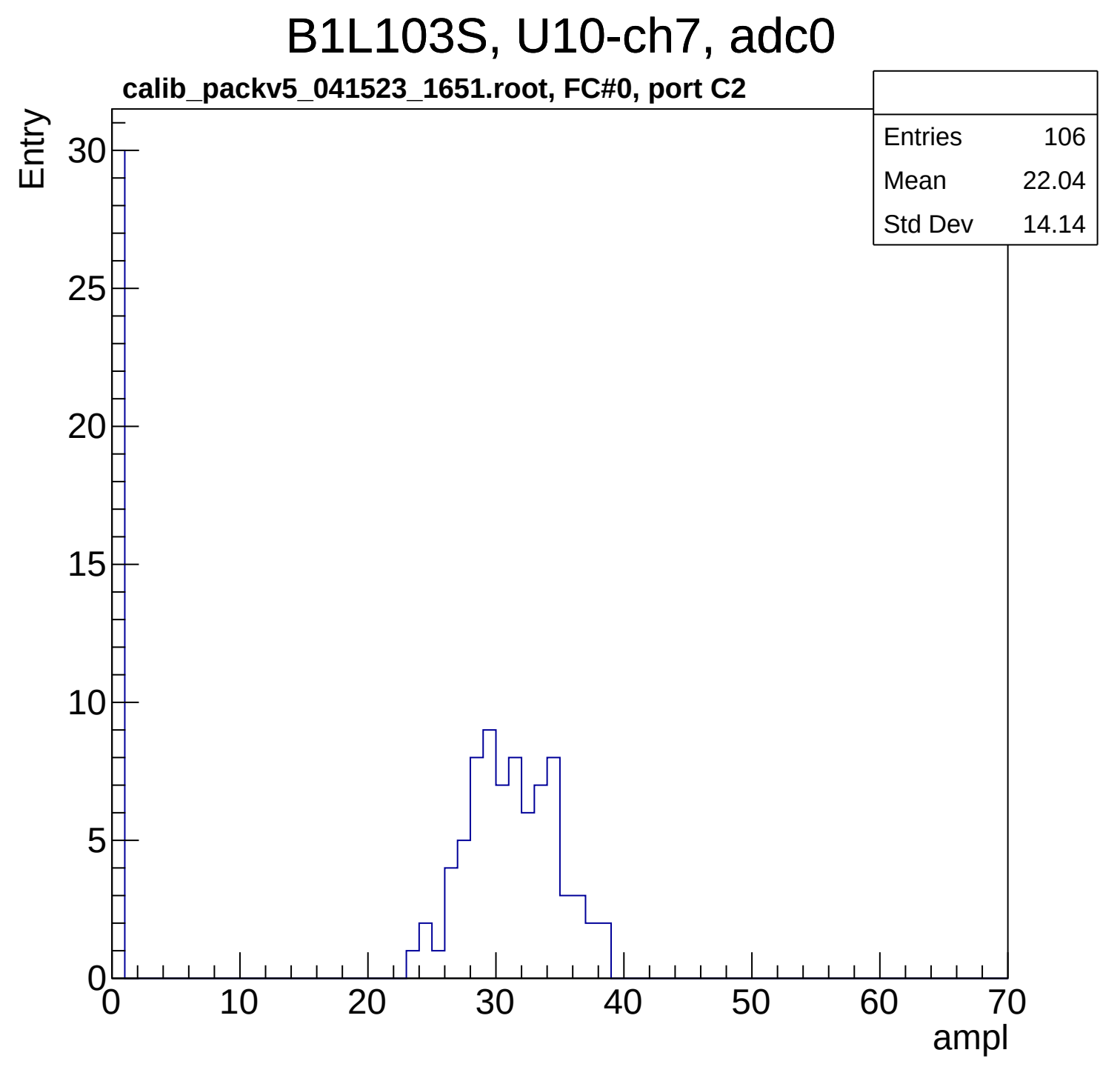
50
60
70
ampl


B1L103S, U10-ch7, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 106
Mean 22.04
Std Dev 14.14
Entry
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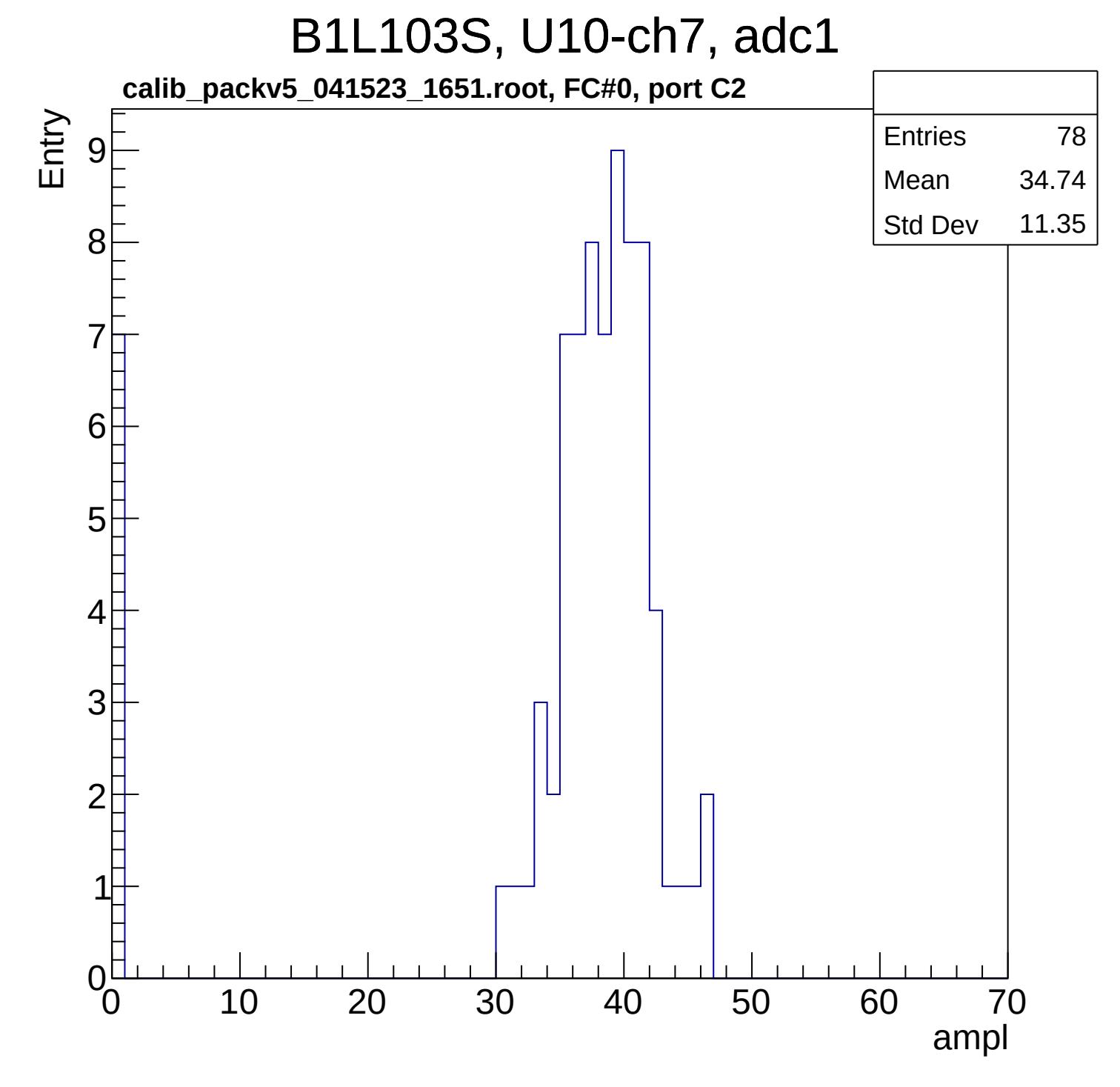
5
10
15
20
25
30
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch7, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 34.74
Std Dev 11.35
Entry
ampl
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2
3
4
5
6
7
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9
0
10
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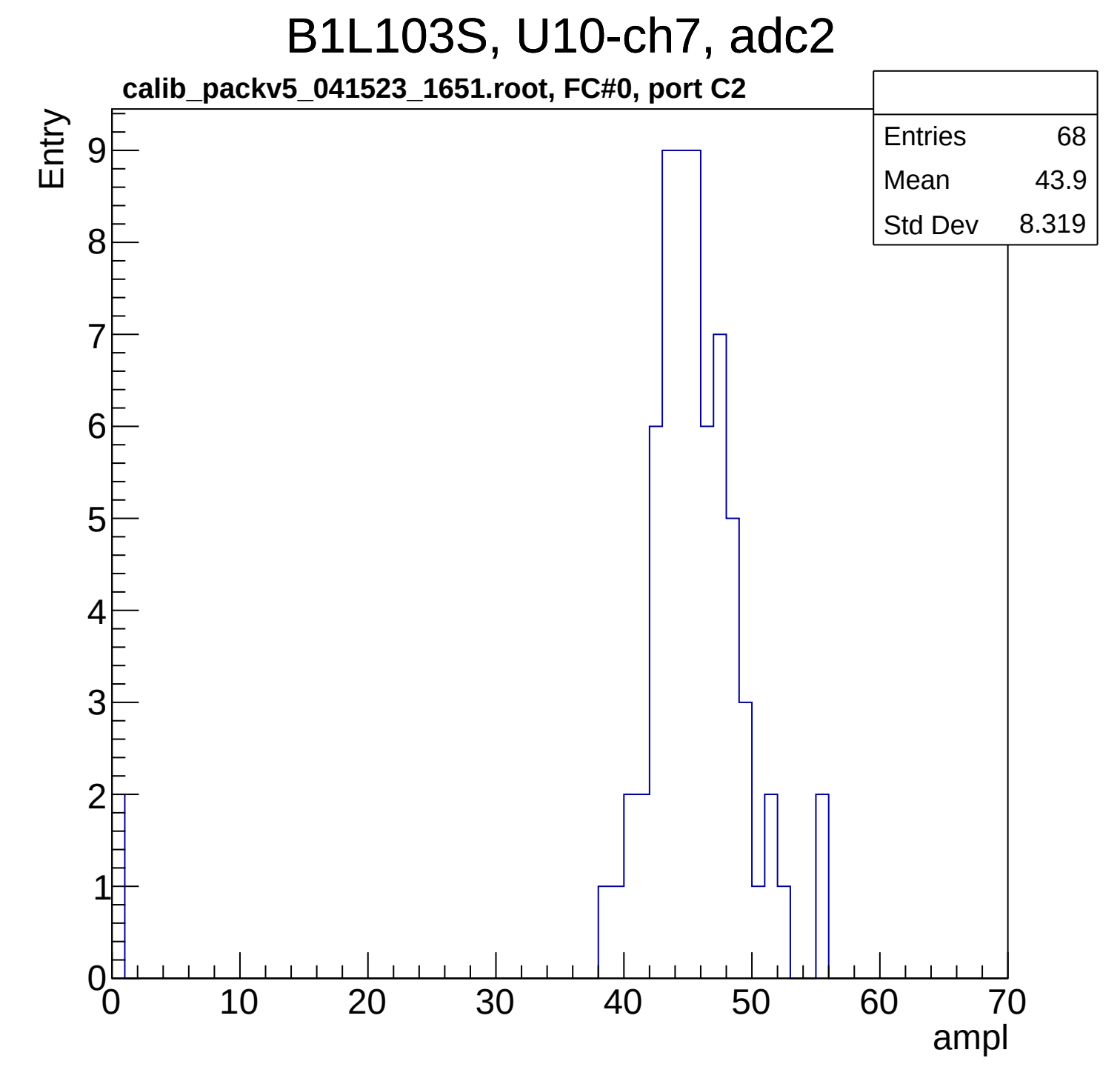
40
50
60
70


B1L103S, U10-ch7, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 43.9
Std Dev 8.319
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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40
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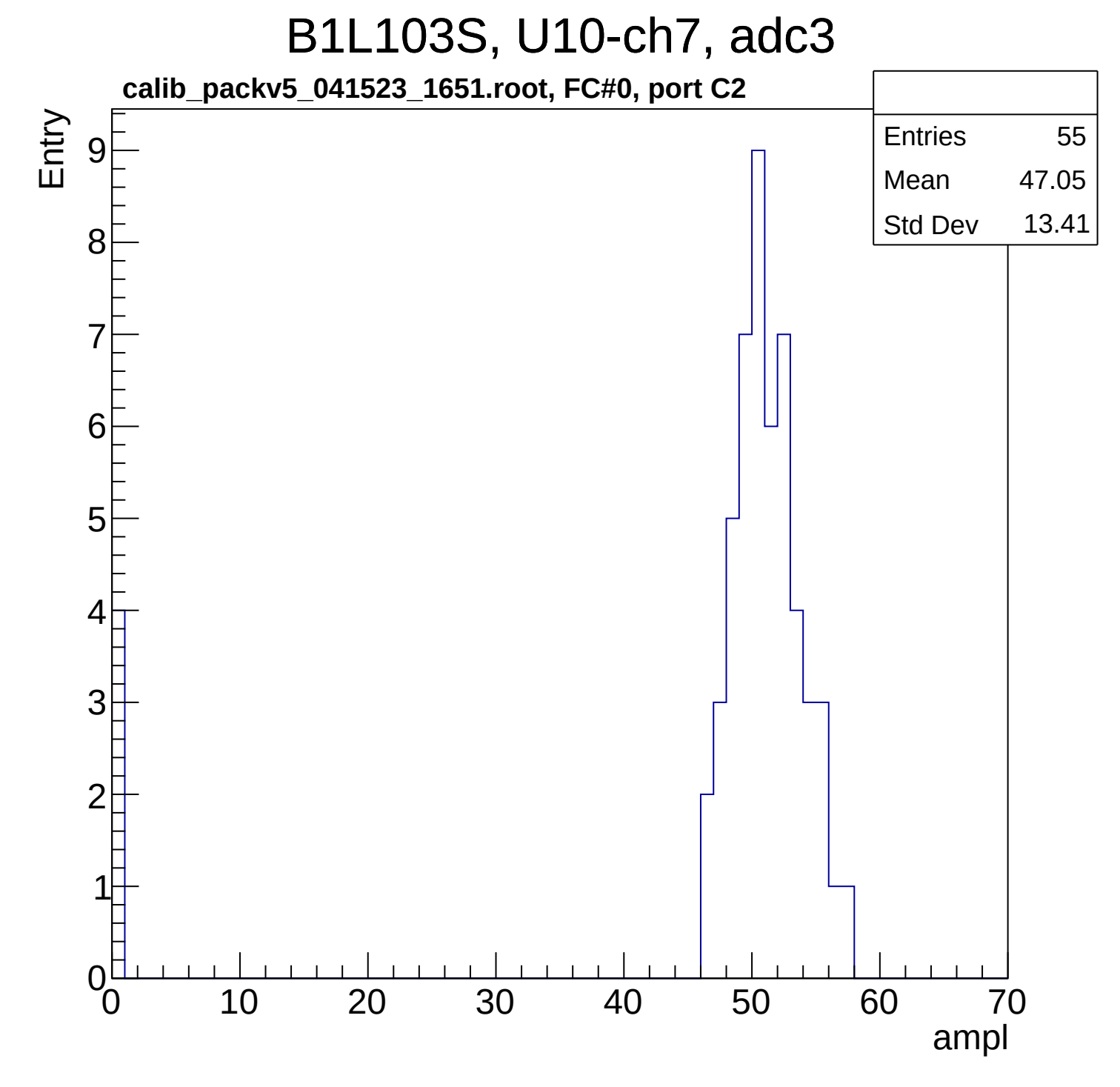
60
70


B1L103S, U10-ch7, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 47.05
Std Dev 13.41
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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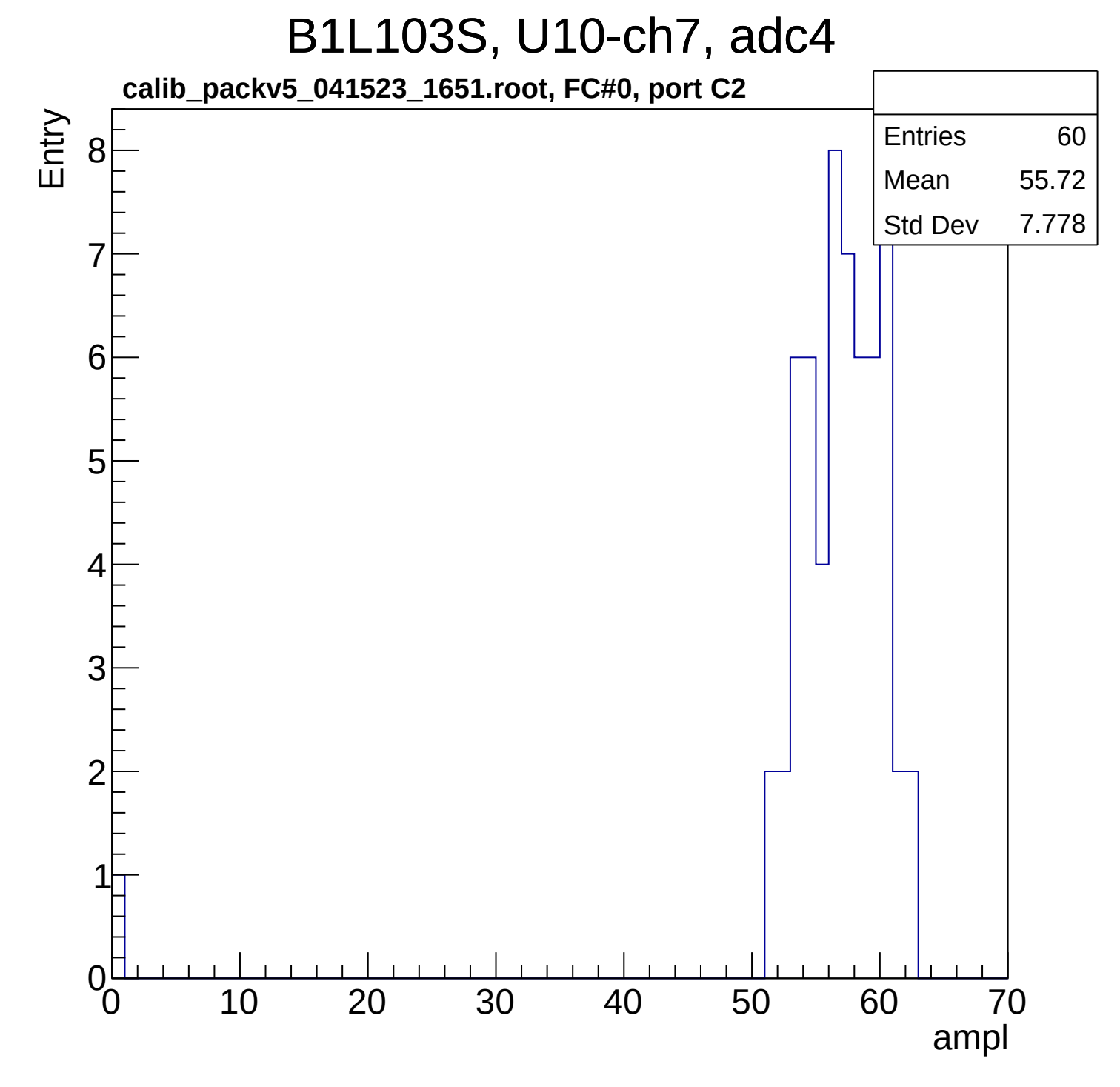
B1L103S, U10-ch7, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 55.72
Std Dev 7.778
Entry
ampl
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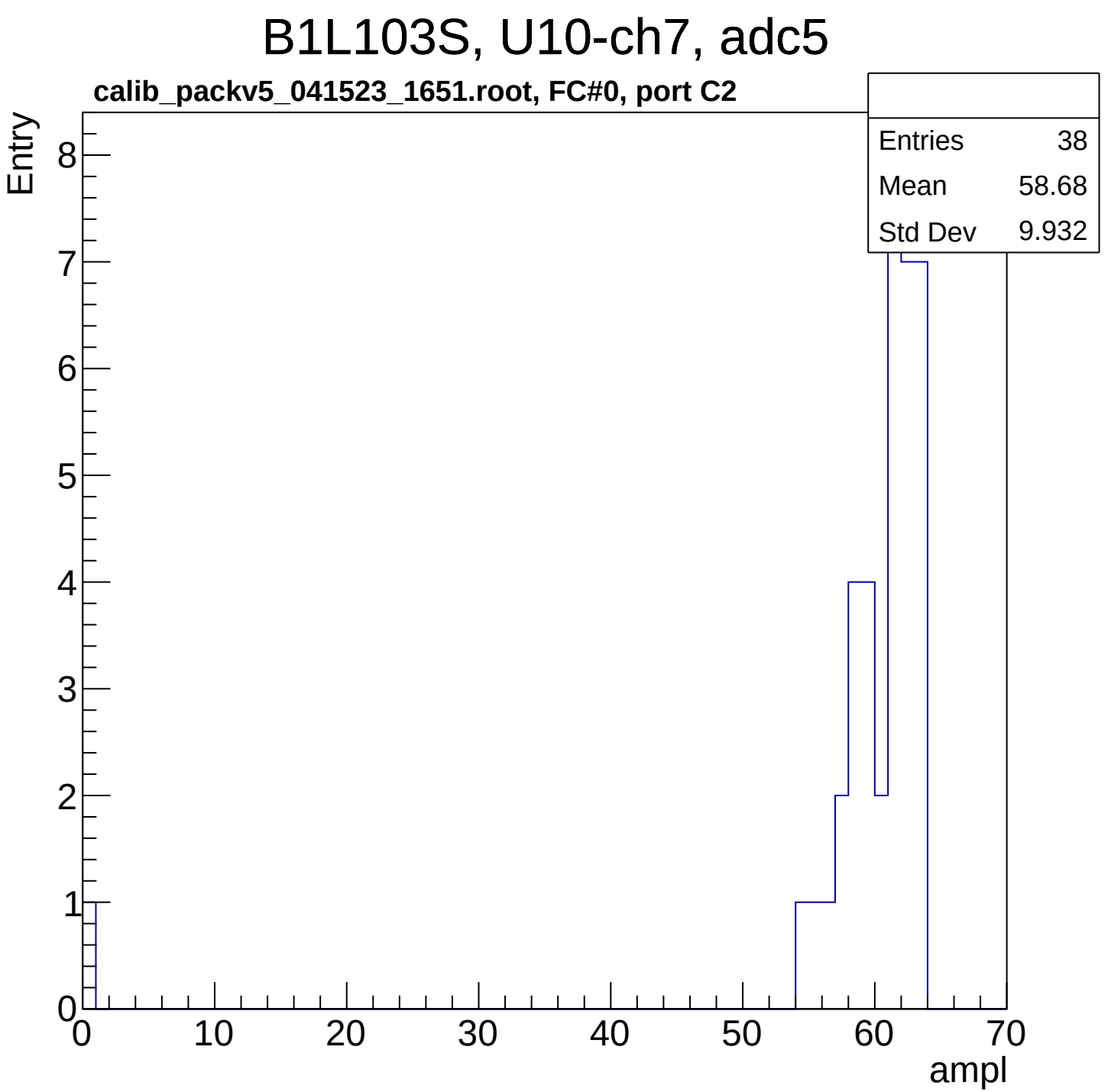
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U10-ch7, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 38
Mean 58.68
Std Dev 9.932
Entry
ampl
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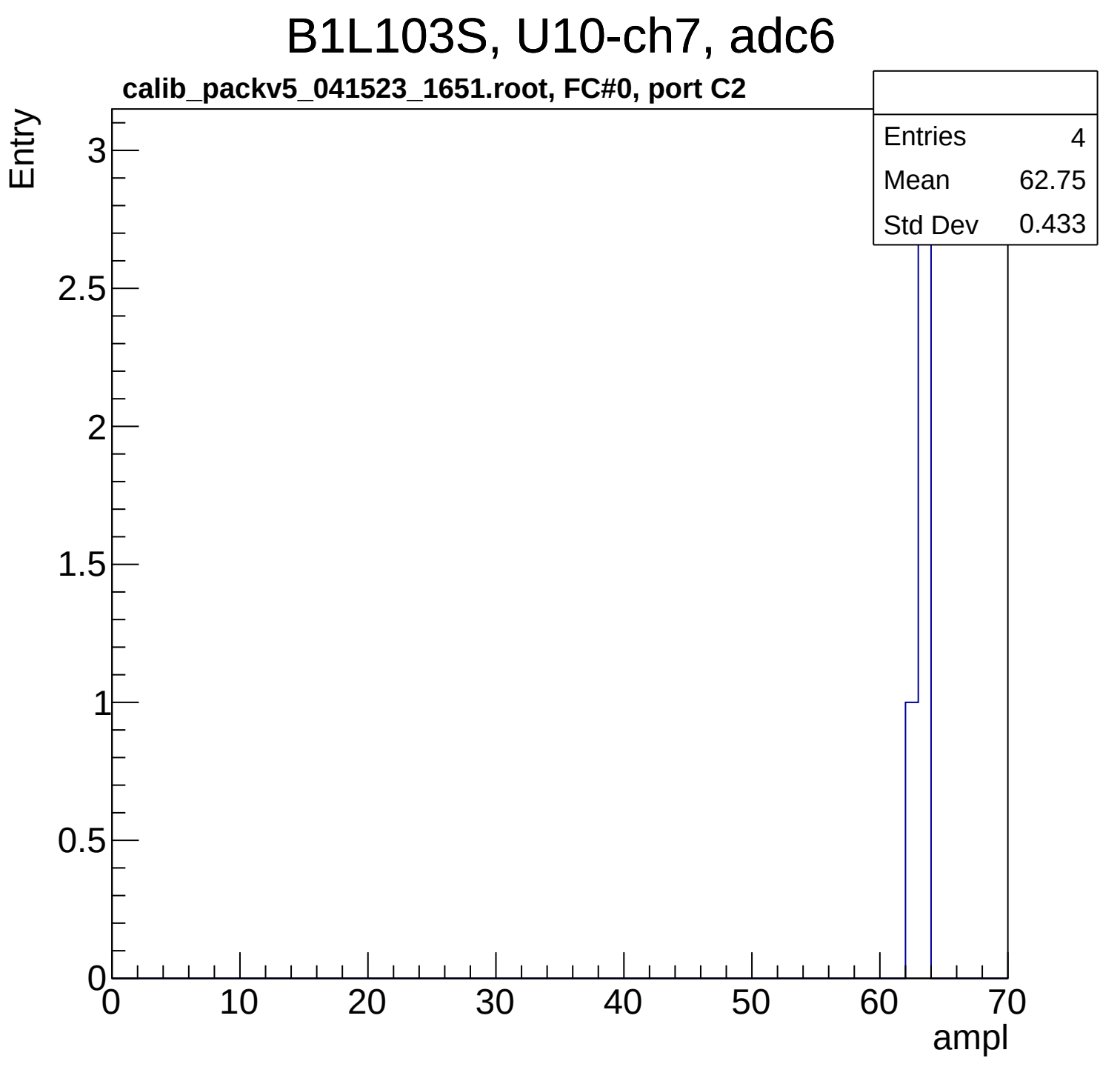
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U10-ch7, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 4
Mean 62.75
Std Dev 0.433
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
10
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40
50
60
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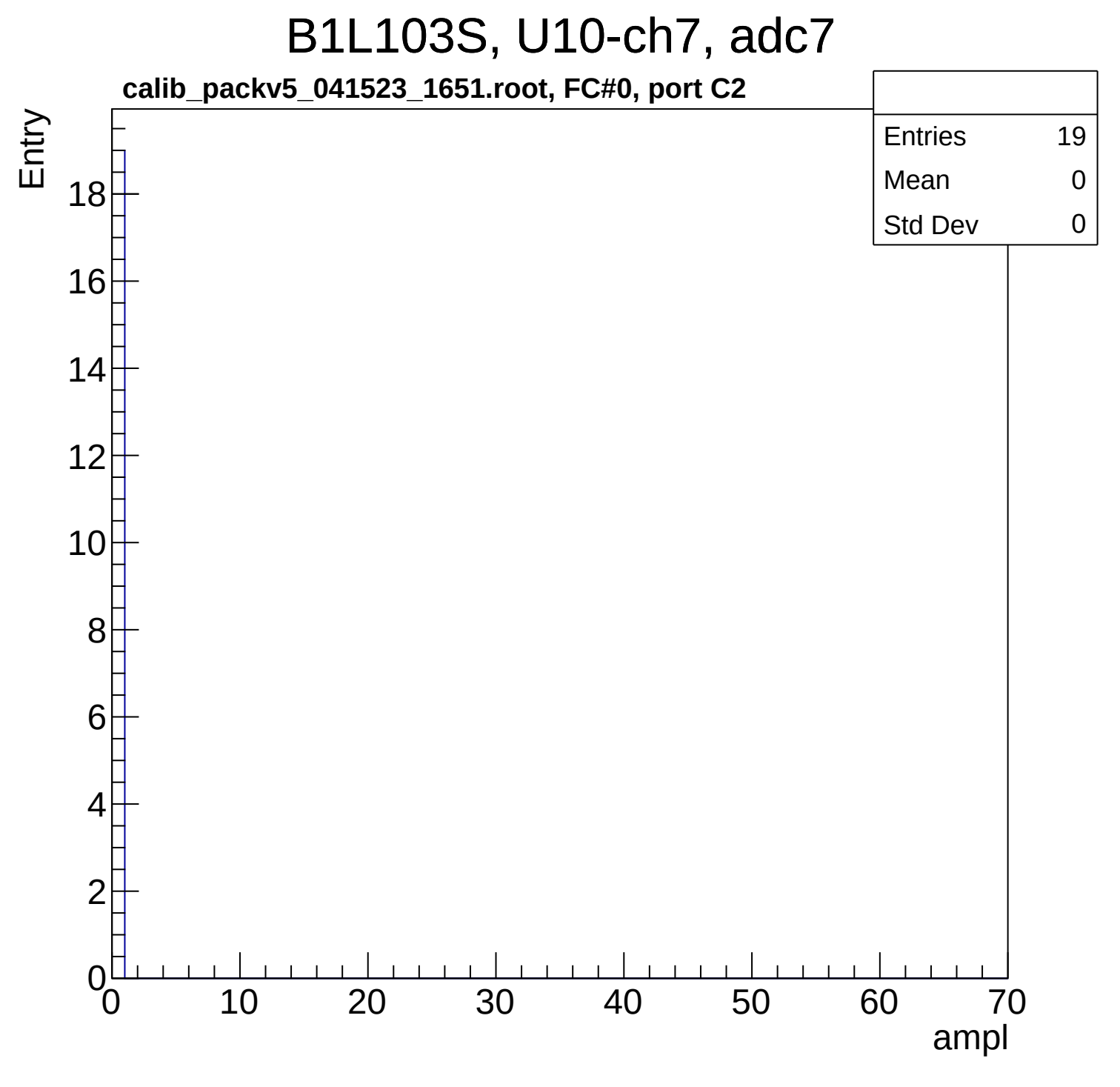
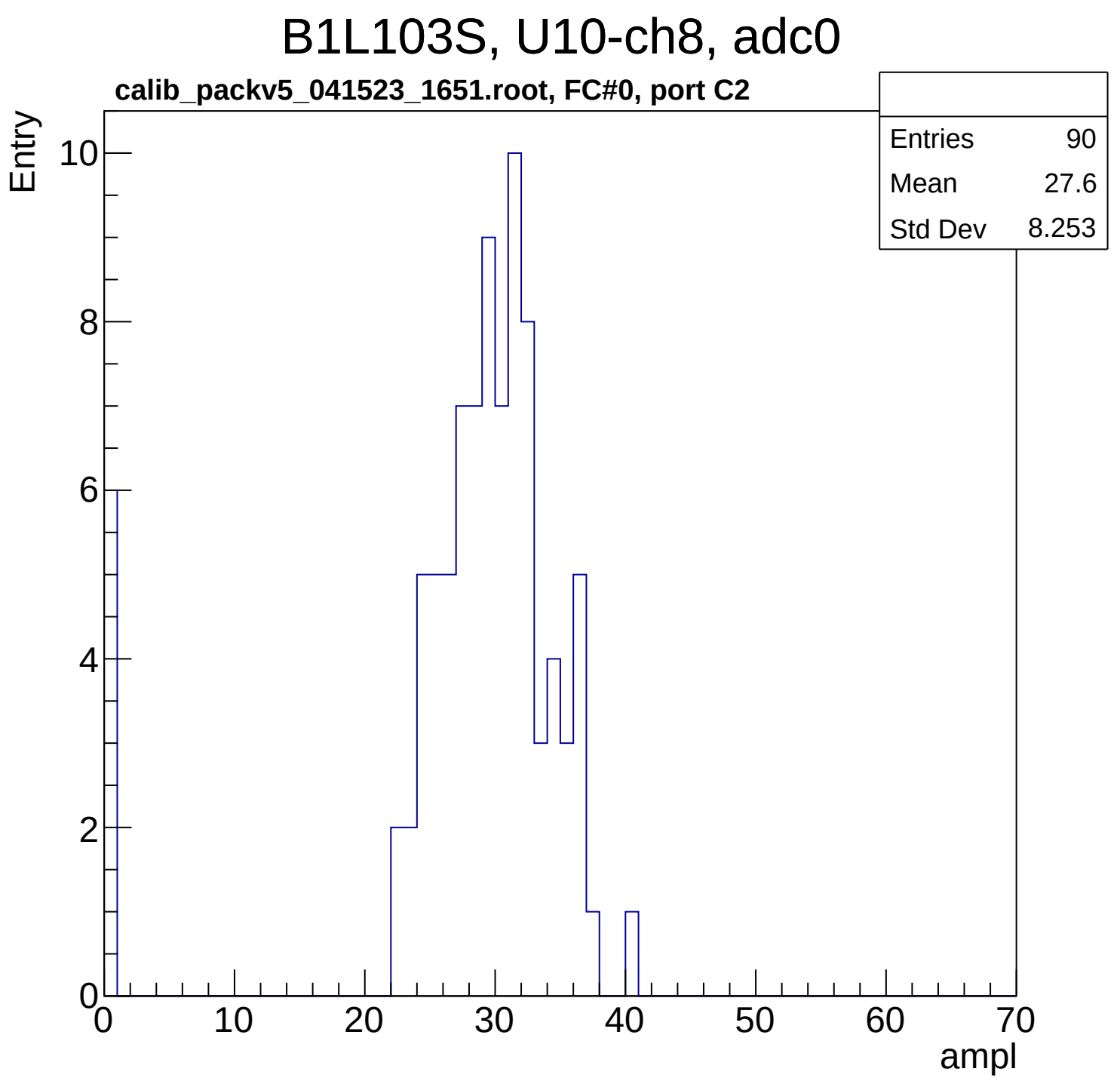

B1L103S, U10-ch7, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch8, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 90
Mean 27.6
Std Dev 8.253
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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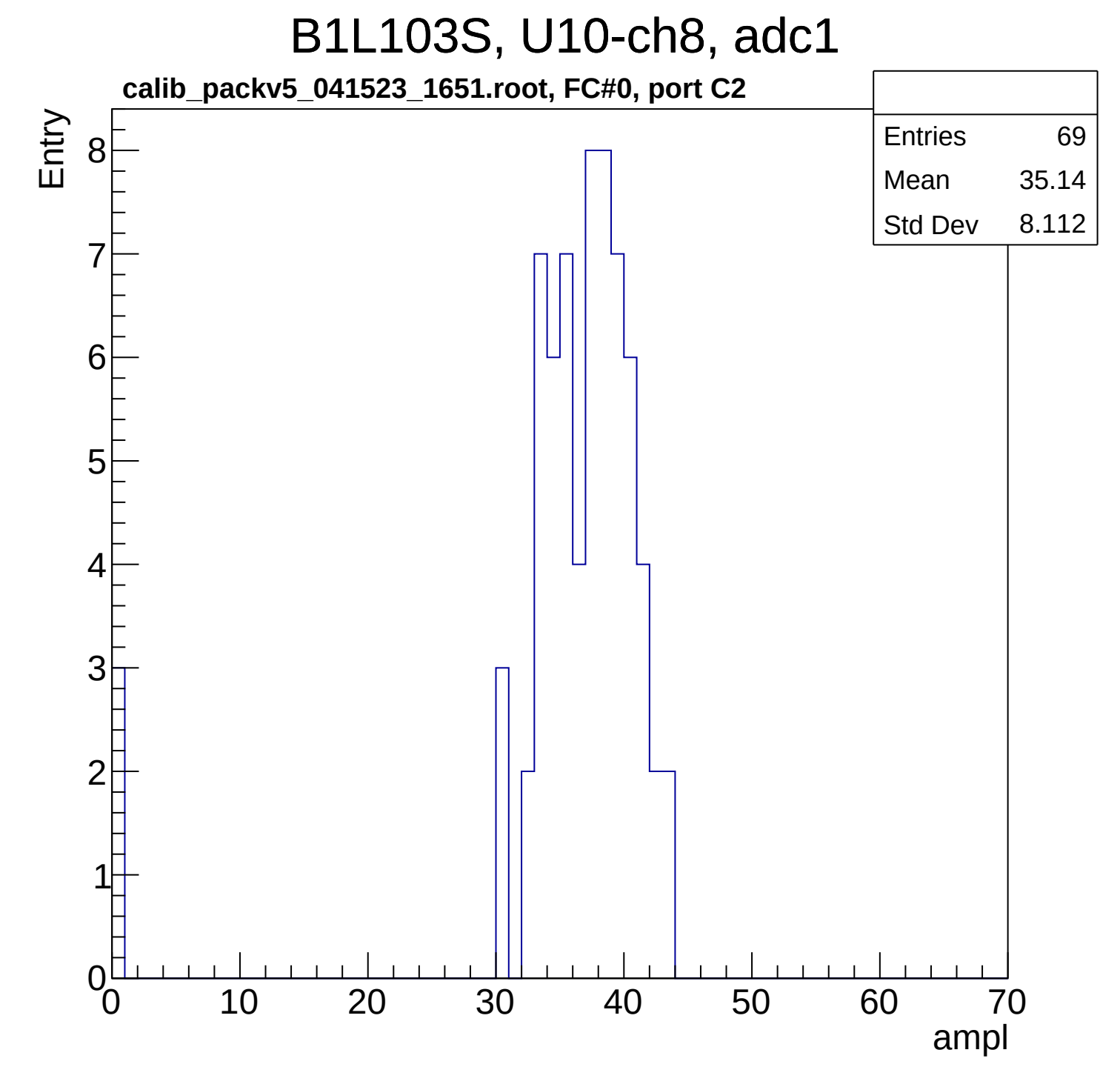
B1L103S, U10-ch8, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 35.14
Std Dev 8.112
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
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40
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60
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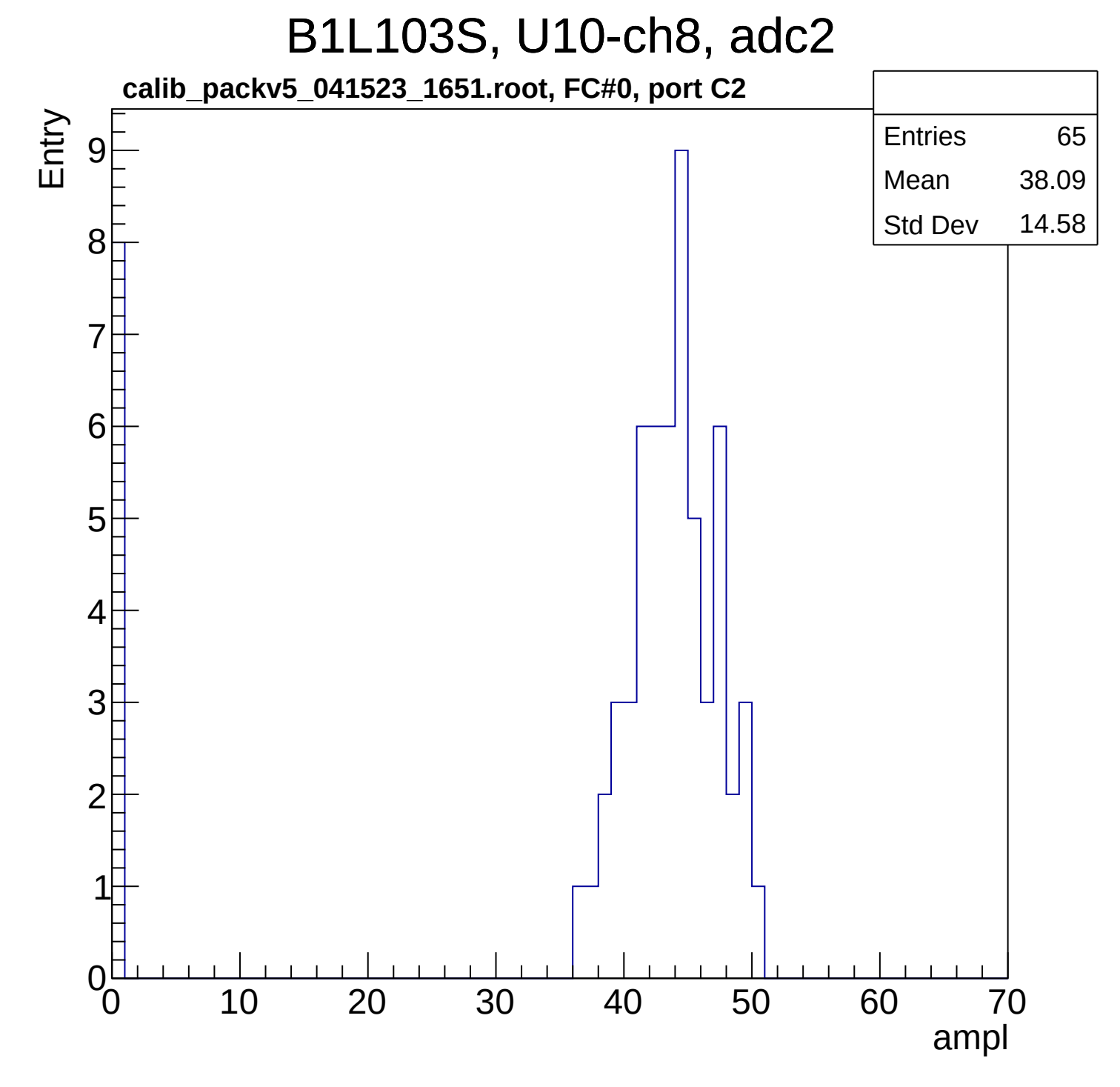
B1L103S, U10-ch8, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 38.09
Std Dev 14.58
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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60
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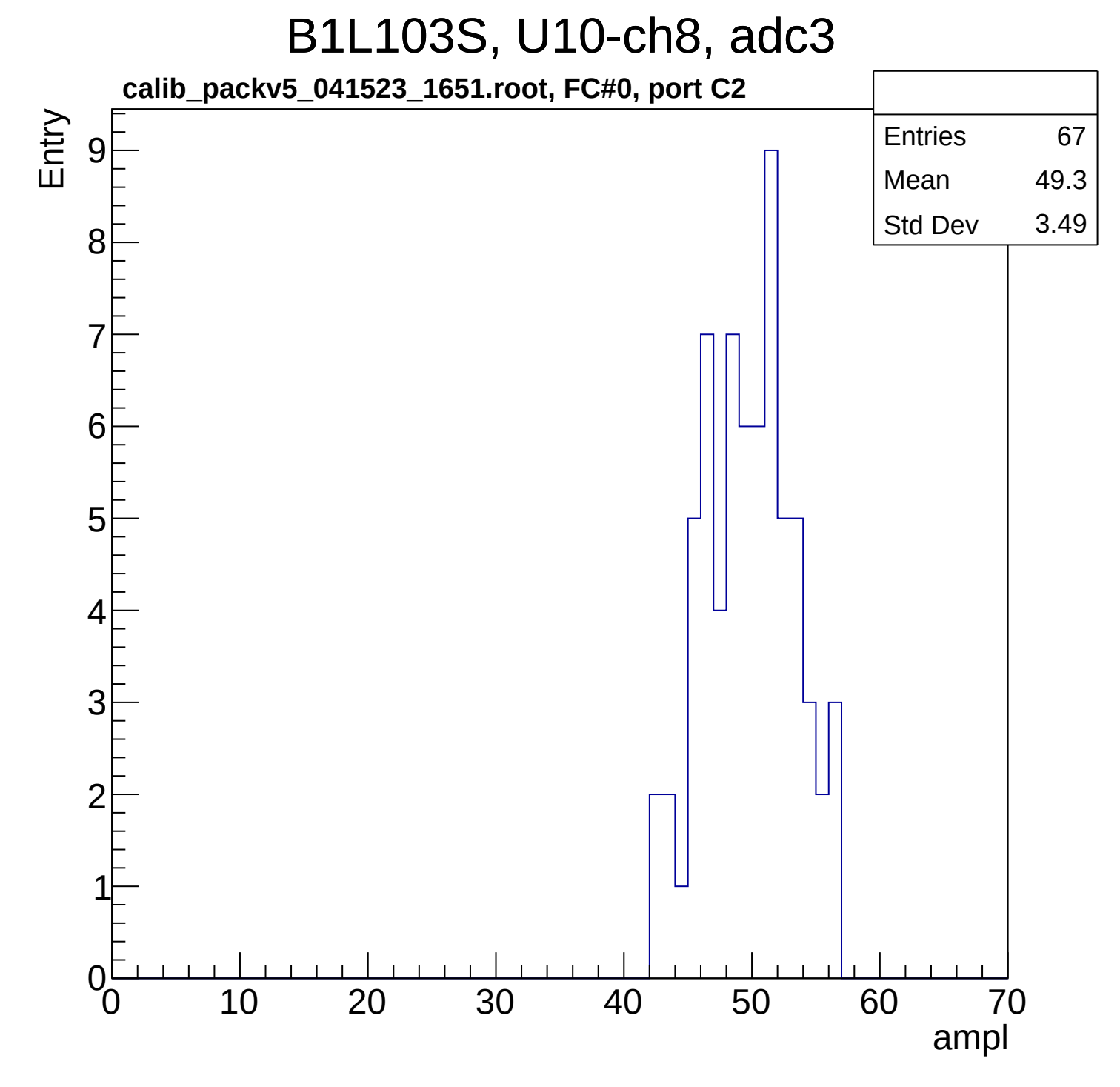
B1L103S, U10-ch8, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 49.3
Std Dev 3.49
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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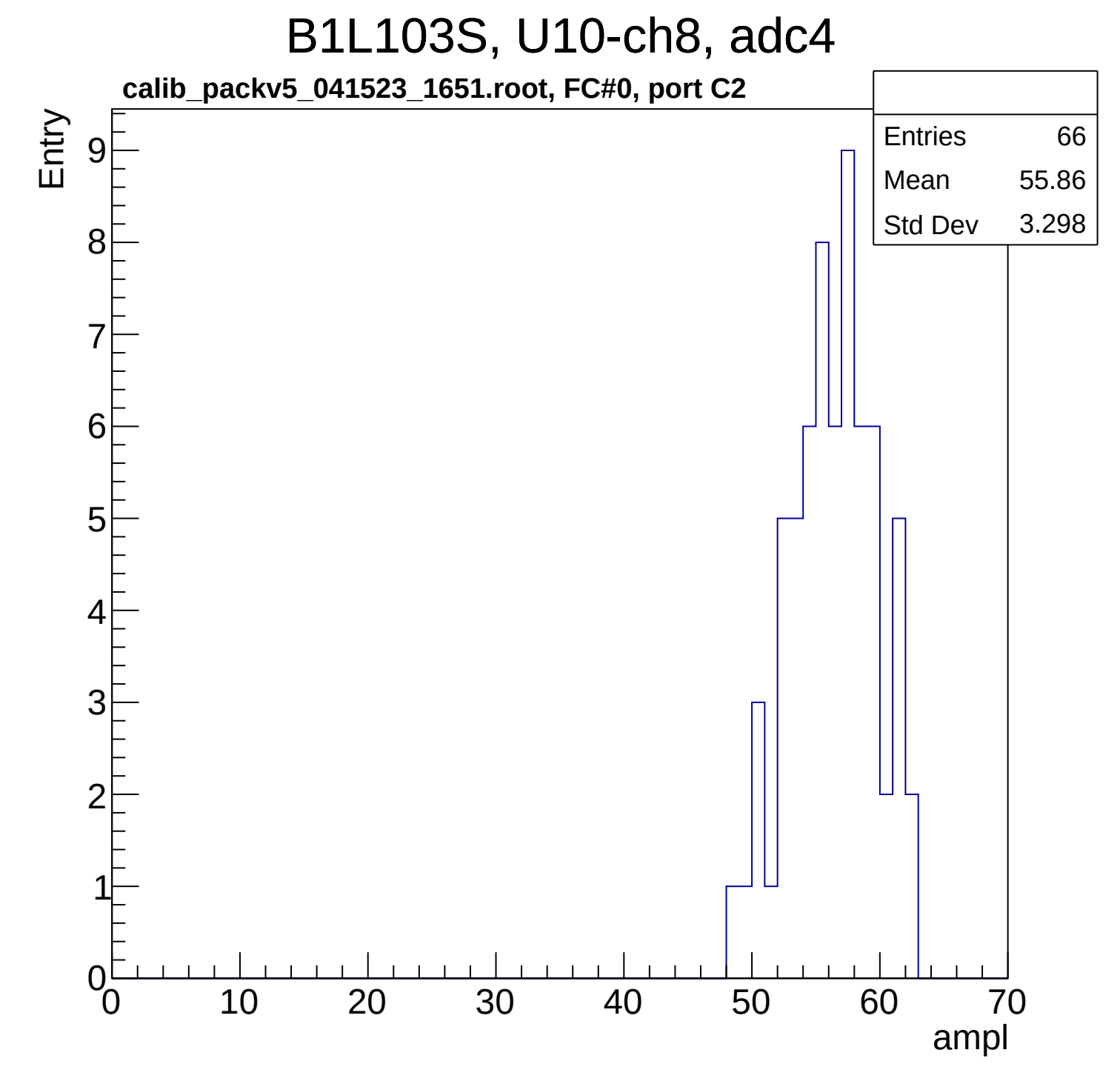
60
70


B1L103S, U10-ch8, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 55.86
Std Dev 3.298
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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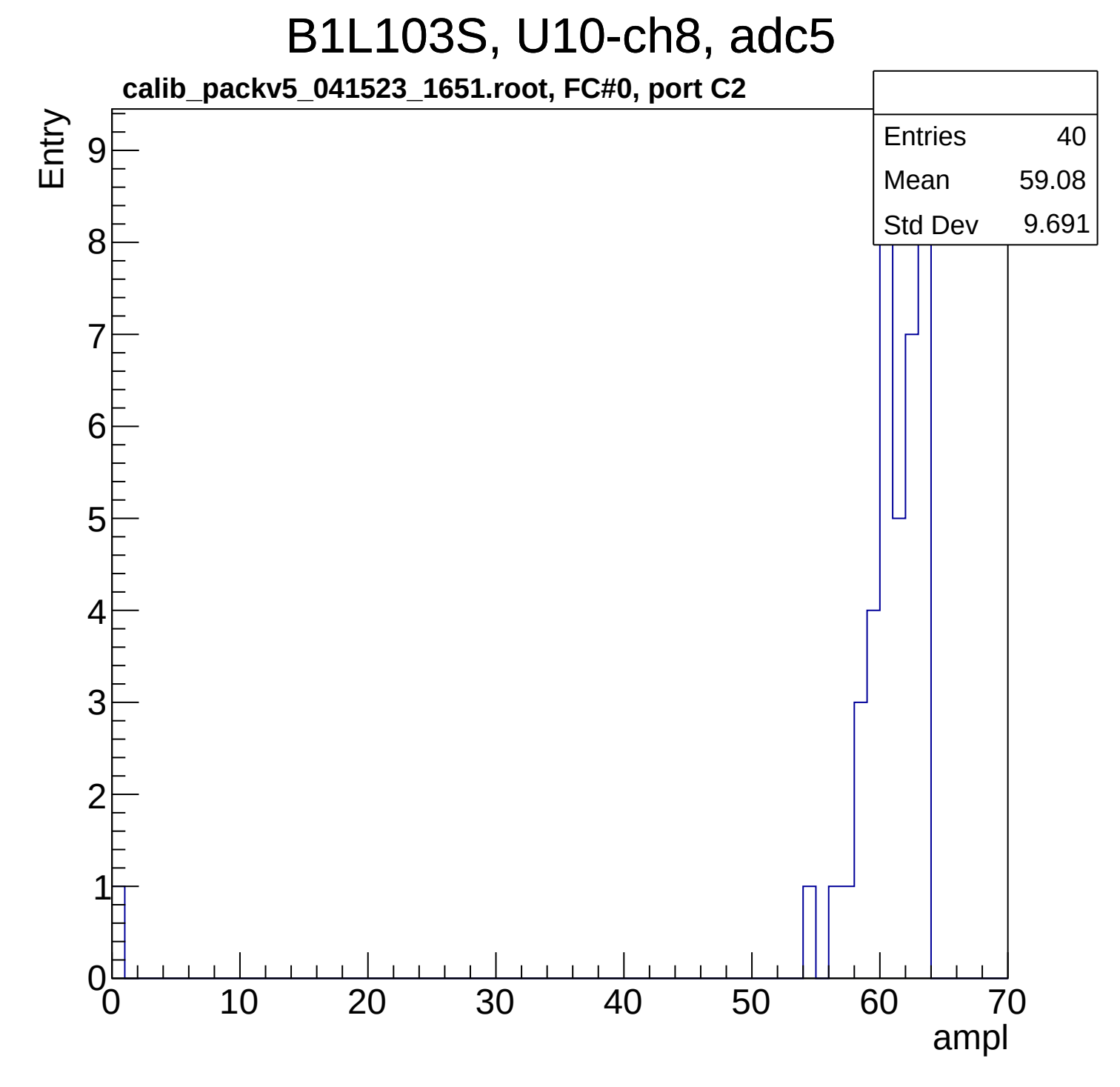
B1L103S, U10-ch8, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 40
Mean 59.08
Std Dev 9.691
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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60
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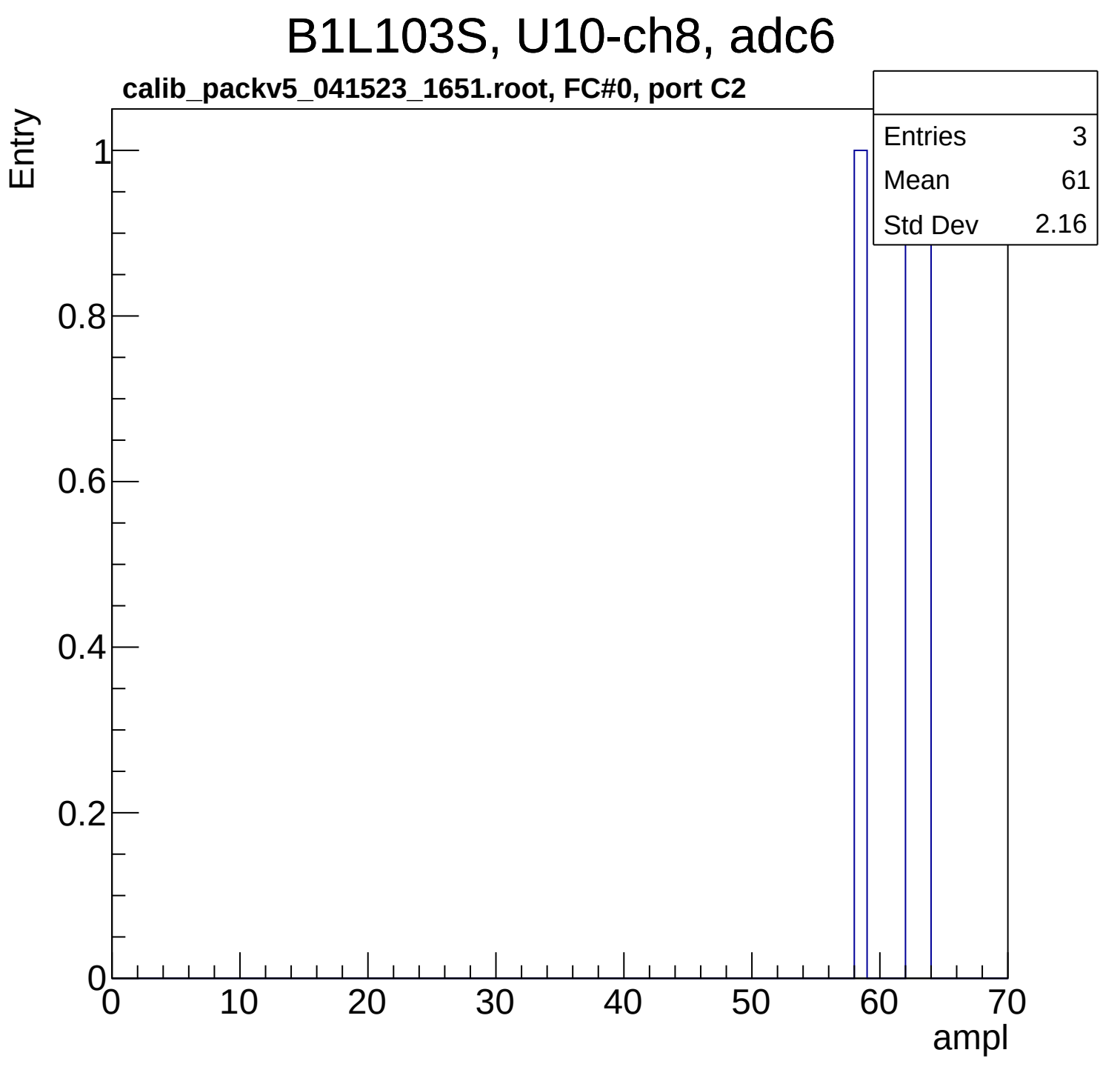
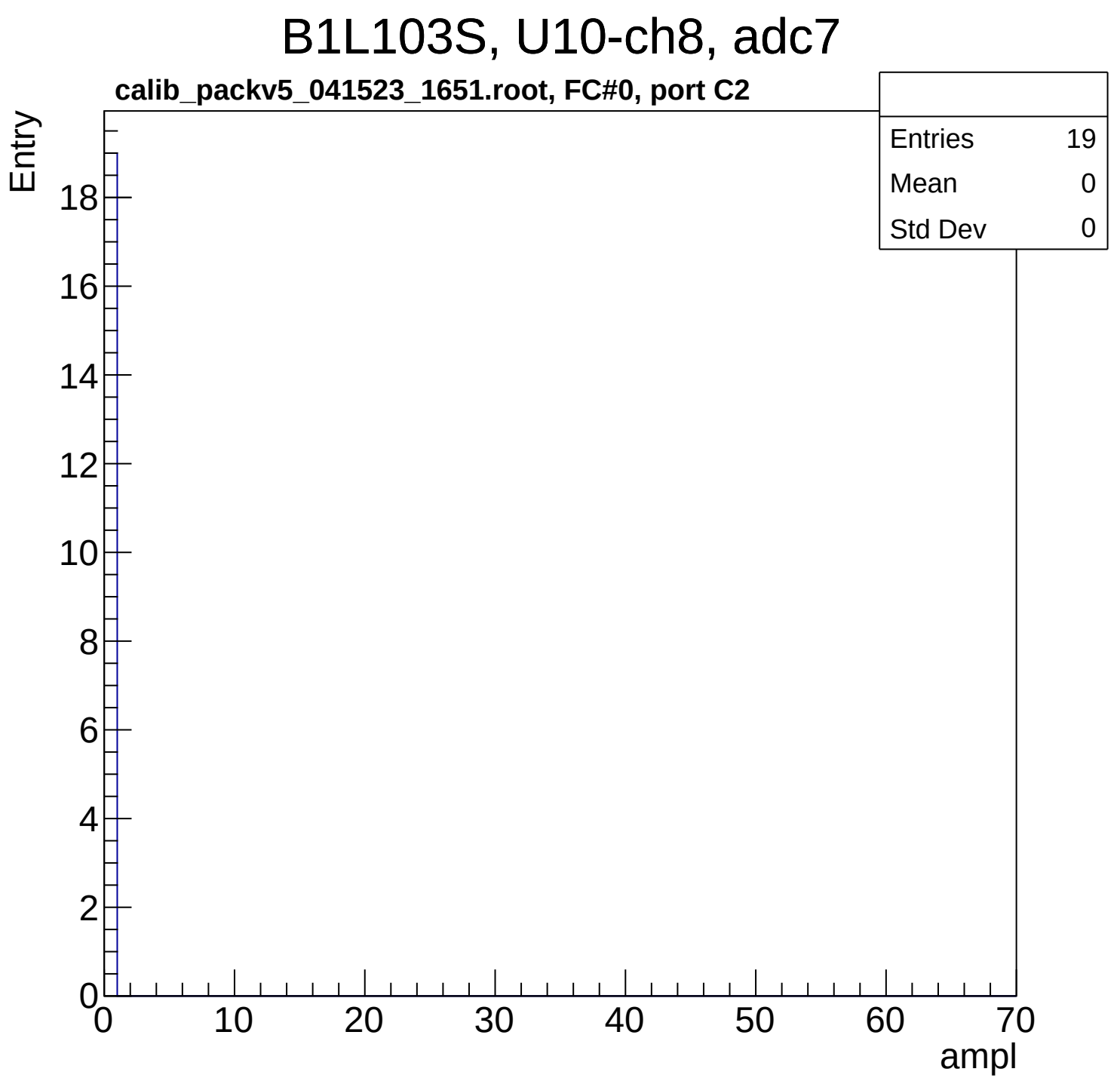
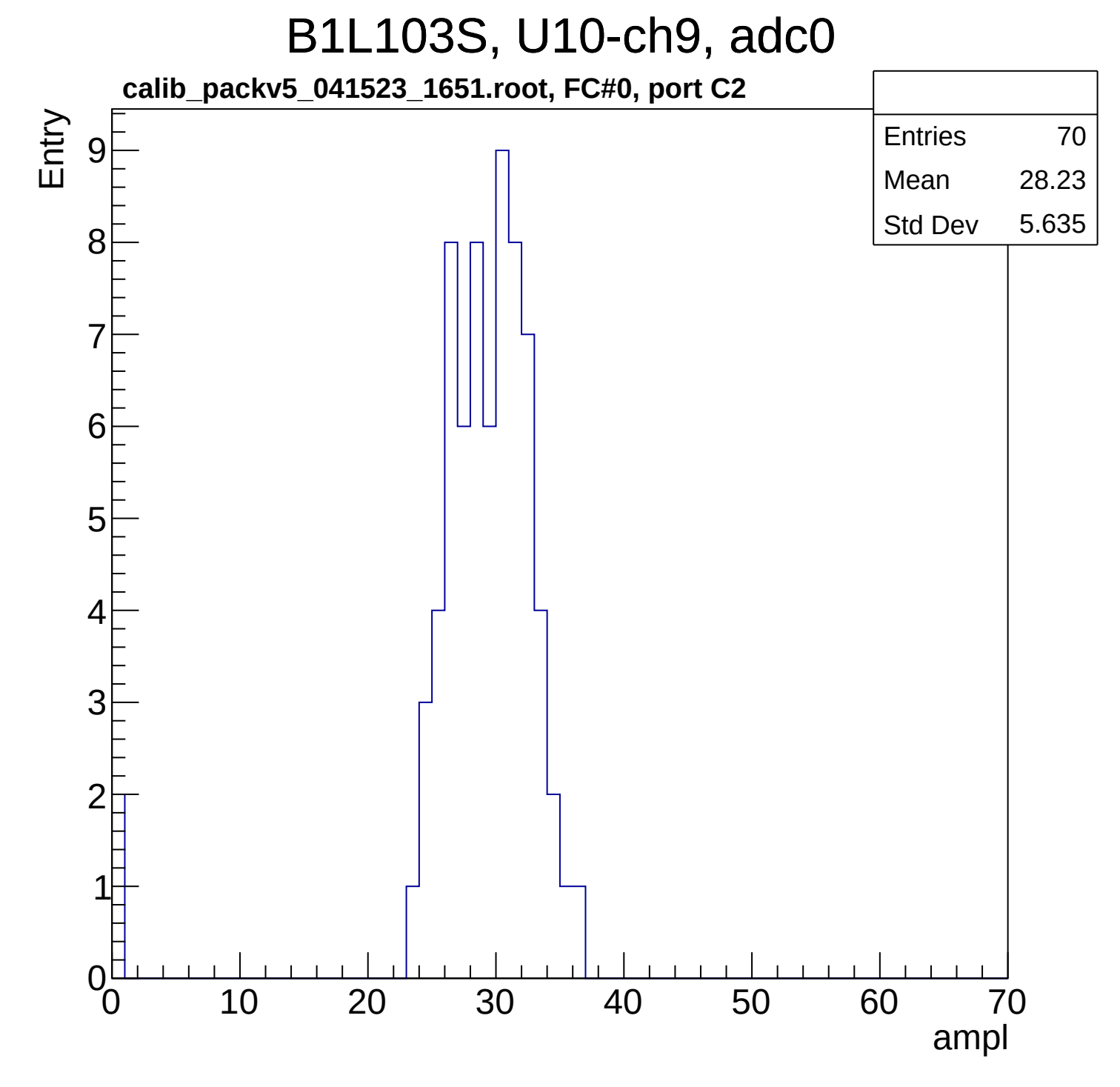

B1L103S, U10-ch8, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 3
Mean 61
Std Dev 2.16
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70


B1L103S, U10-ch8, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch9, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 28.23
Std Dev 5.635
Entry
ampl
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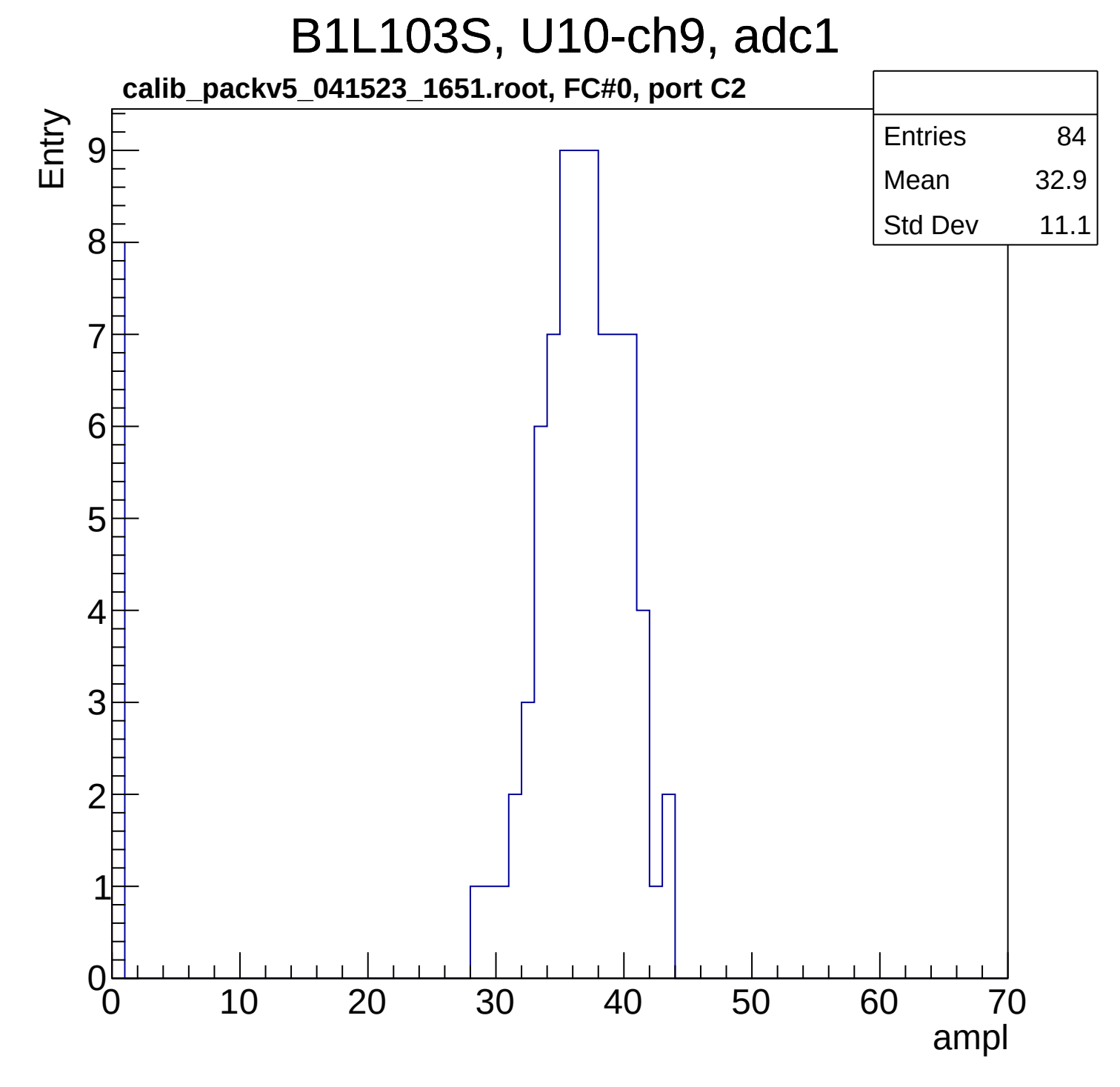
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U10-ch9, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 32.9
Std Dev 11.1
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
50
60
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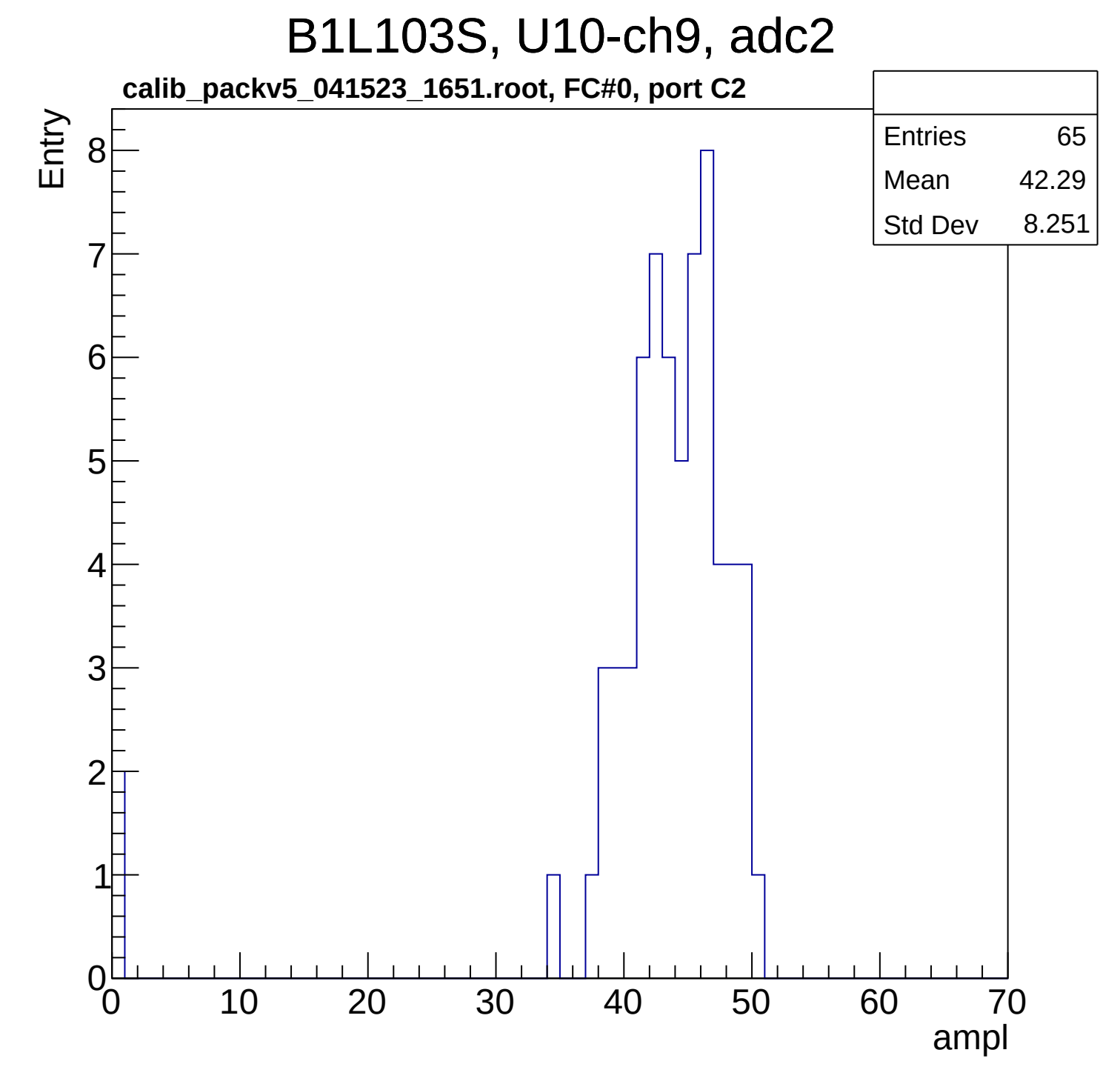
B1L103S, U10-ch9, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 42.29
Std Dev 8.251
Entry
ampl
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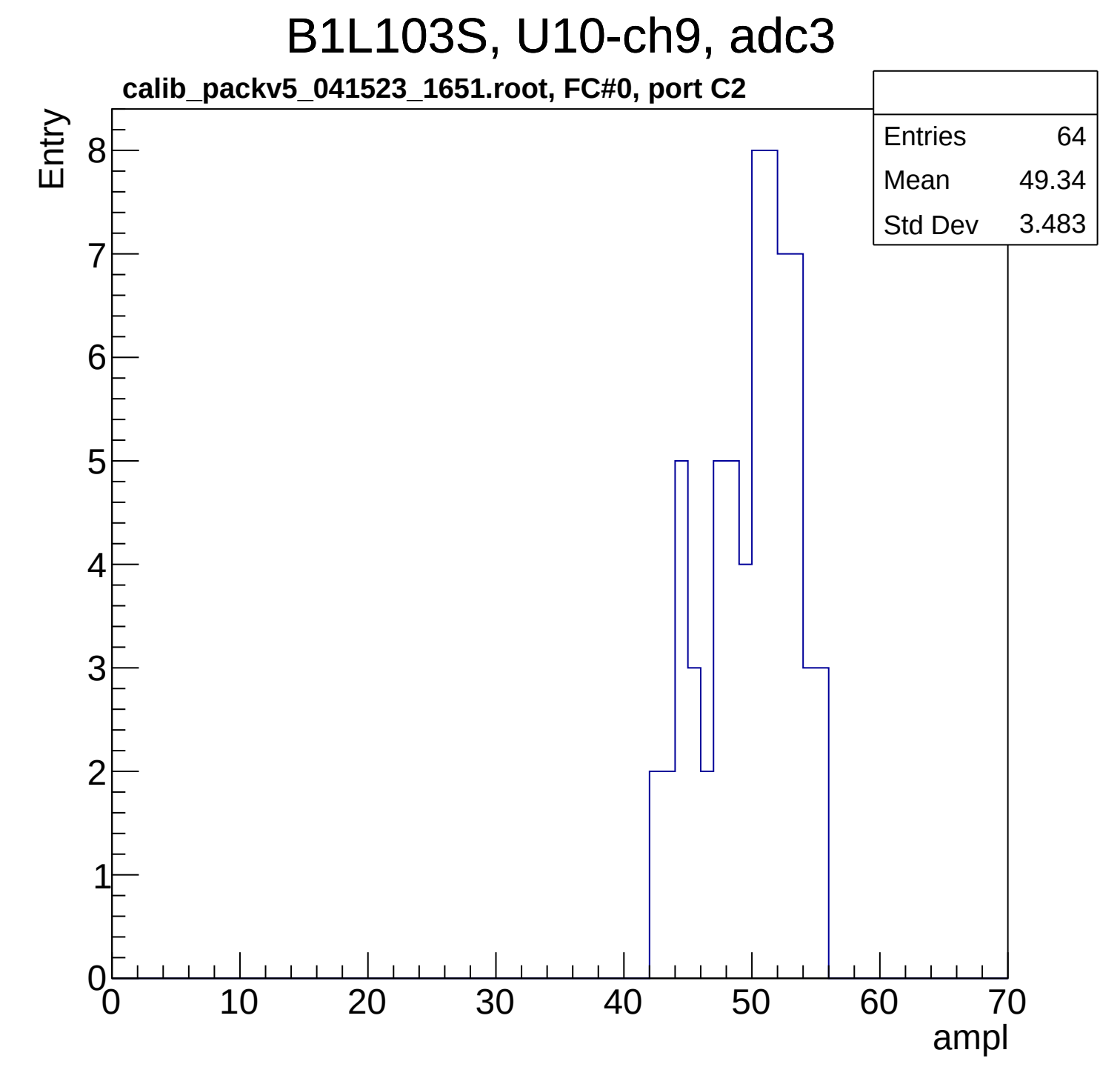
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U10-ch9, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 49.34
Std Dev 3.483
Entry
ampl
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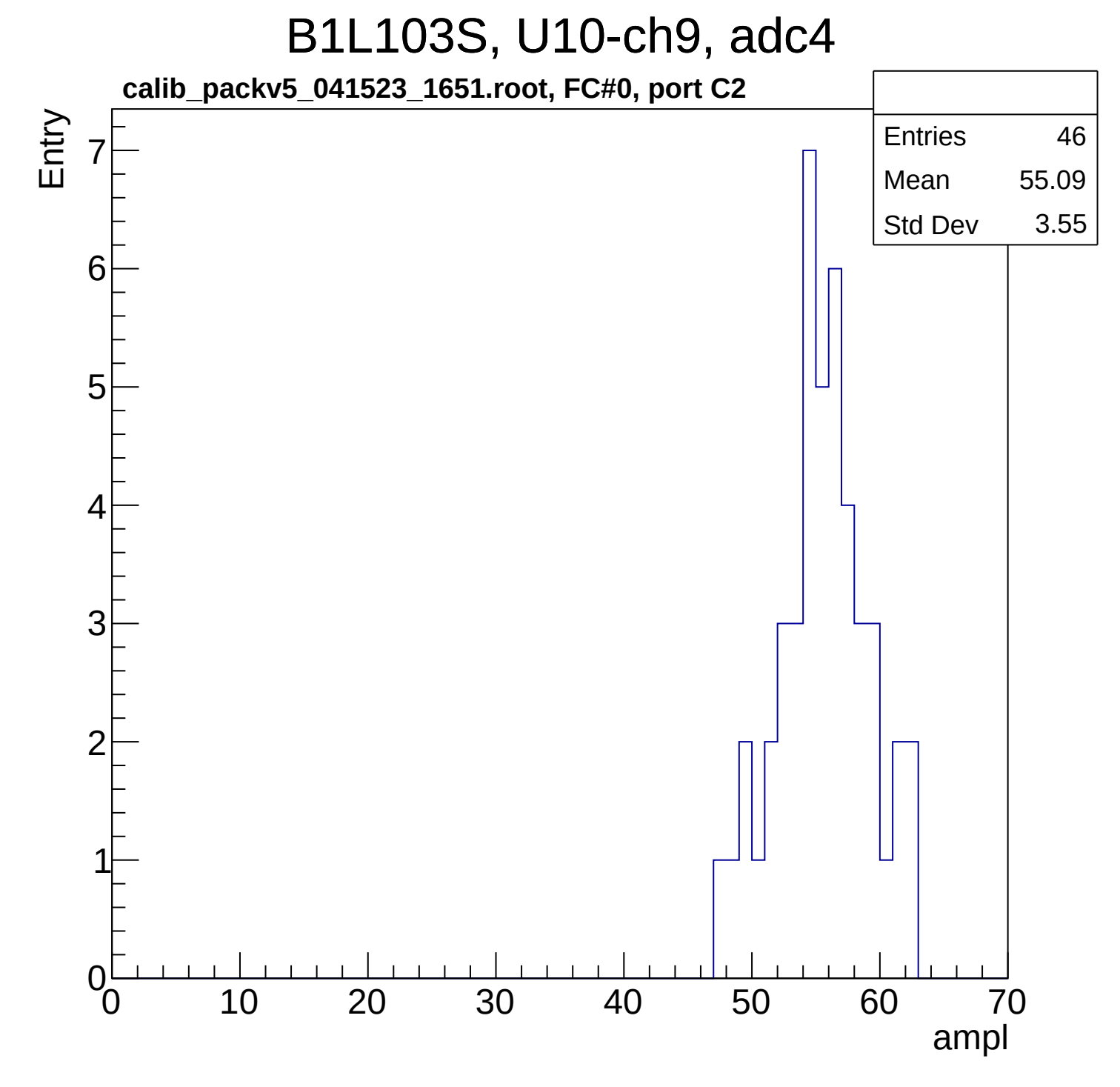
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U10-ch9, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 55.09
Std Dev 3.55
Entry
ampl
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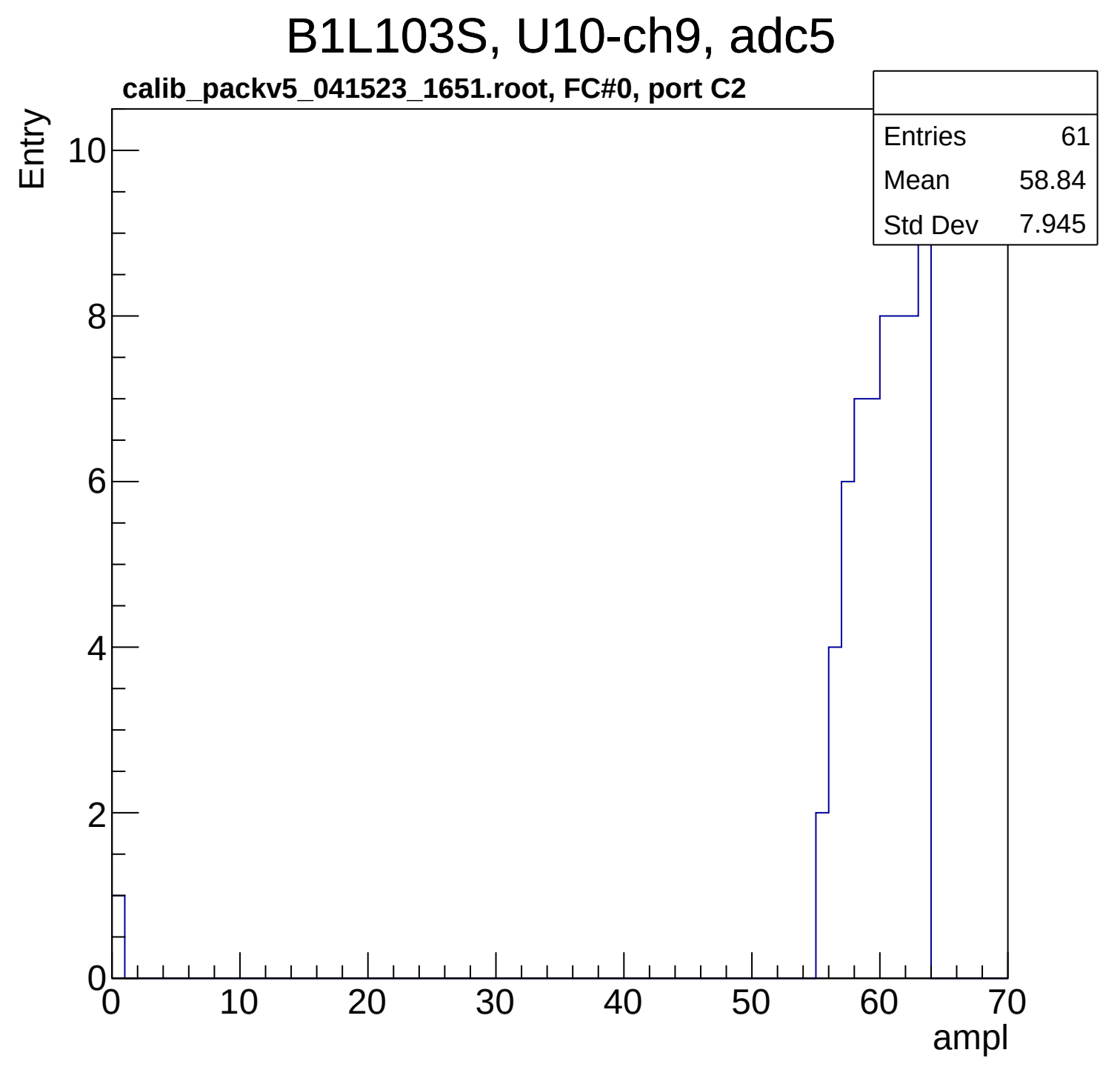
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U10-ch9, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 58.84
Std Dev 7.945
Entry
ampl
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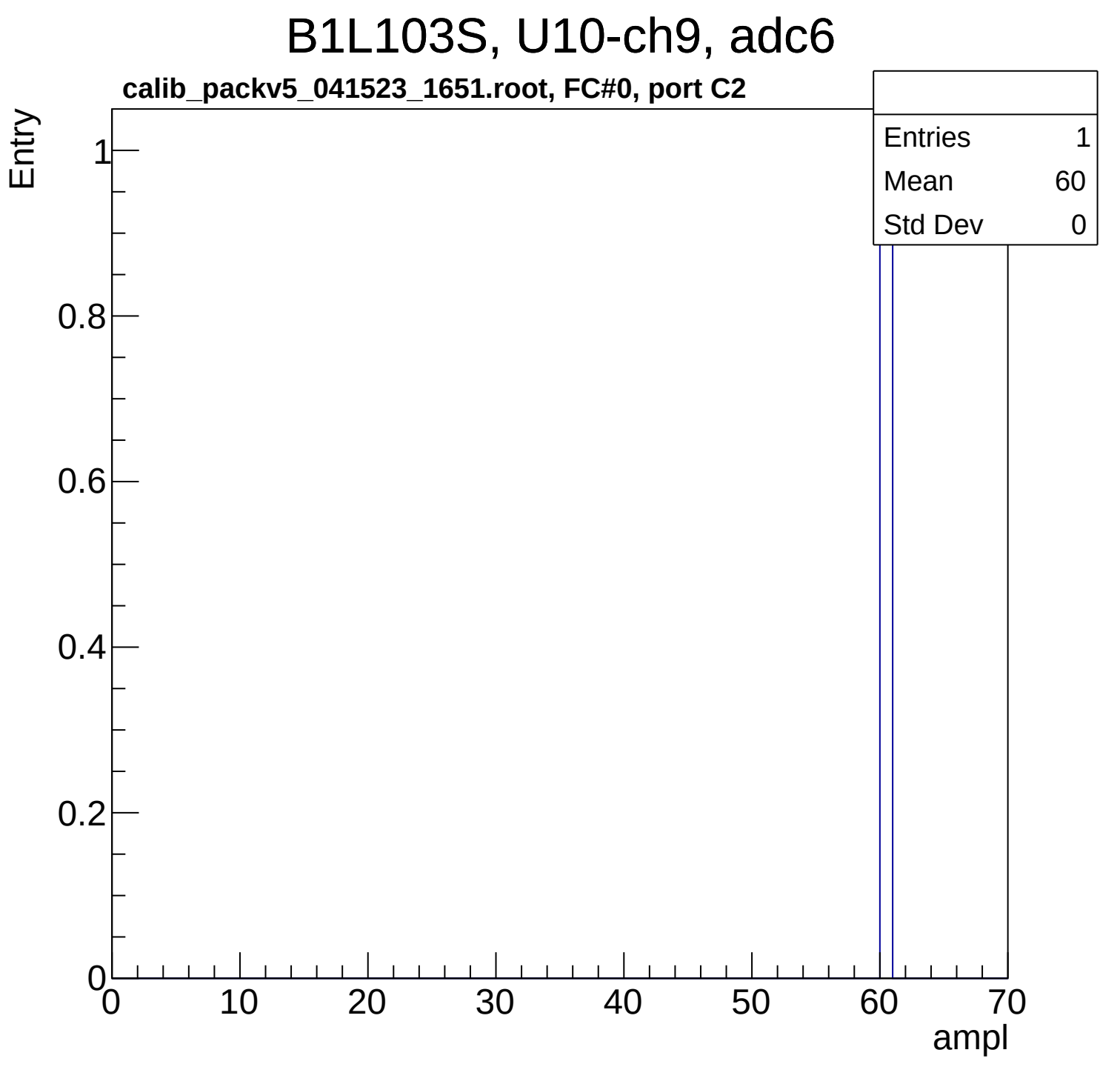
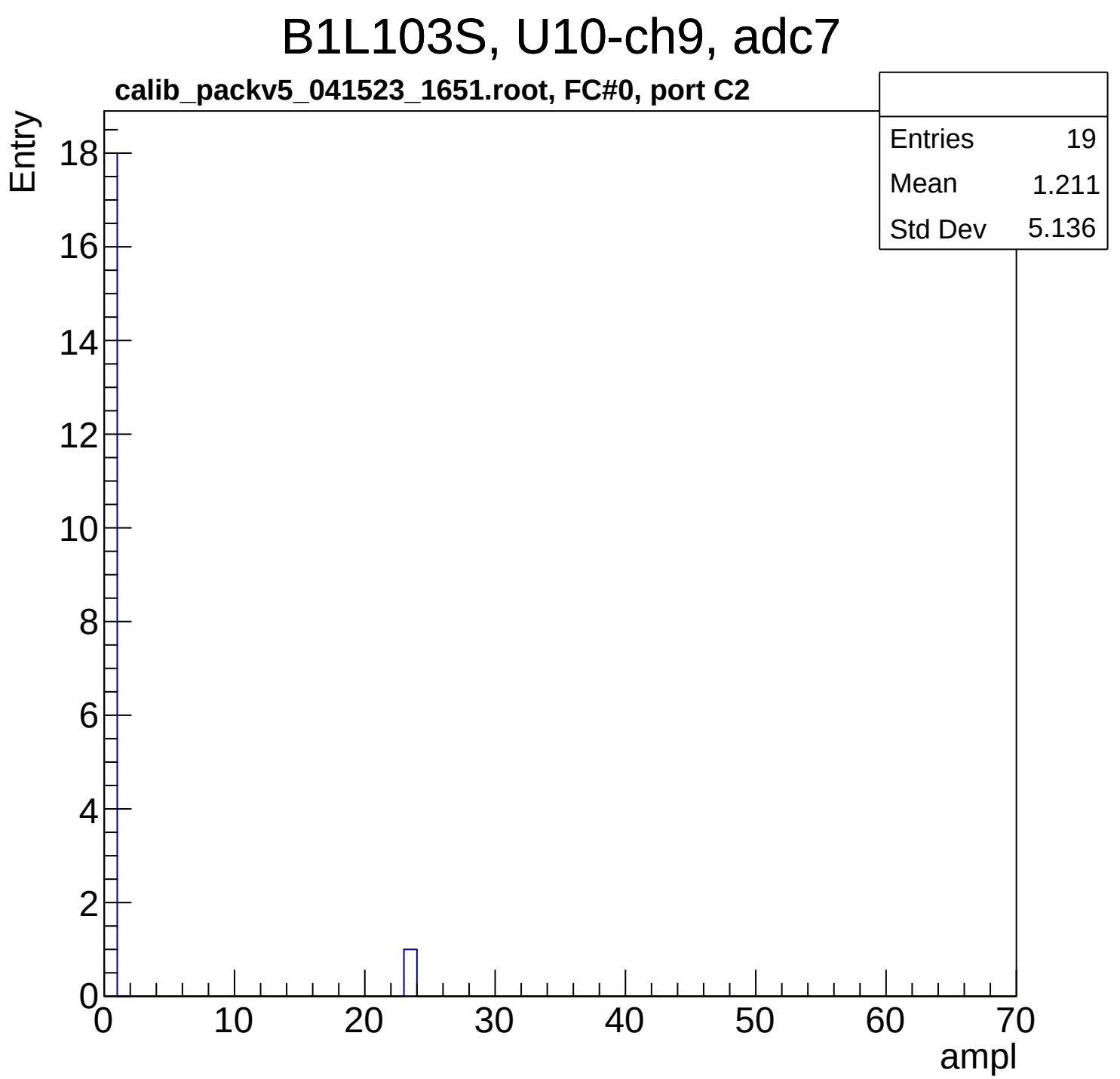
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U10-ch9, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 1
Mean 60
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch9, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.211
Std Dev 5.136
Entry
0
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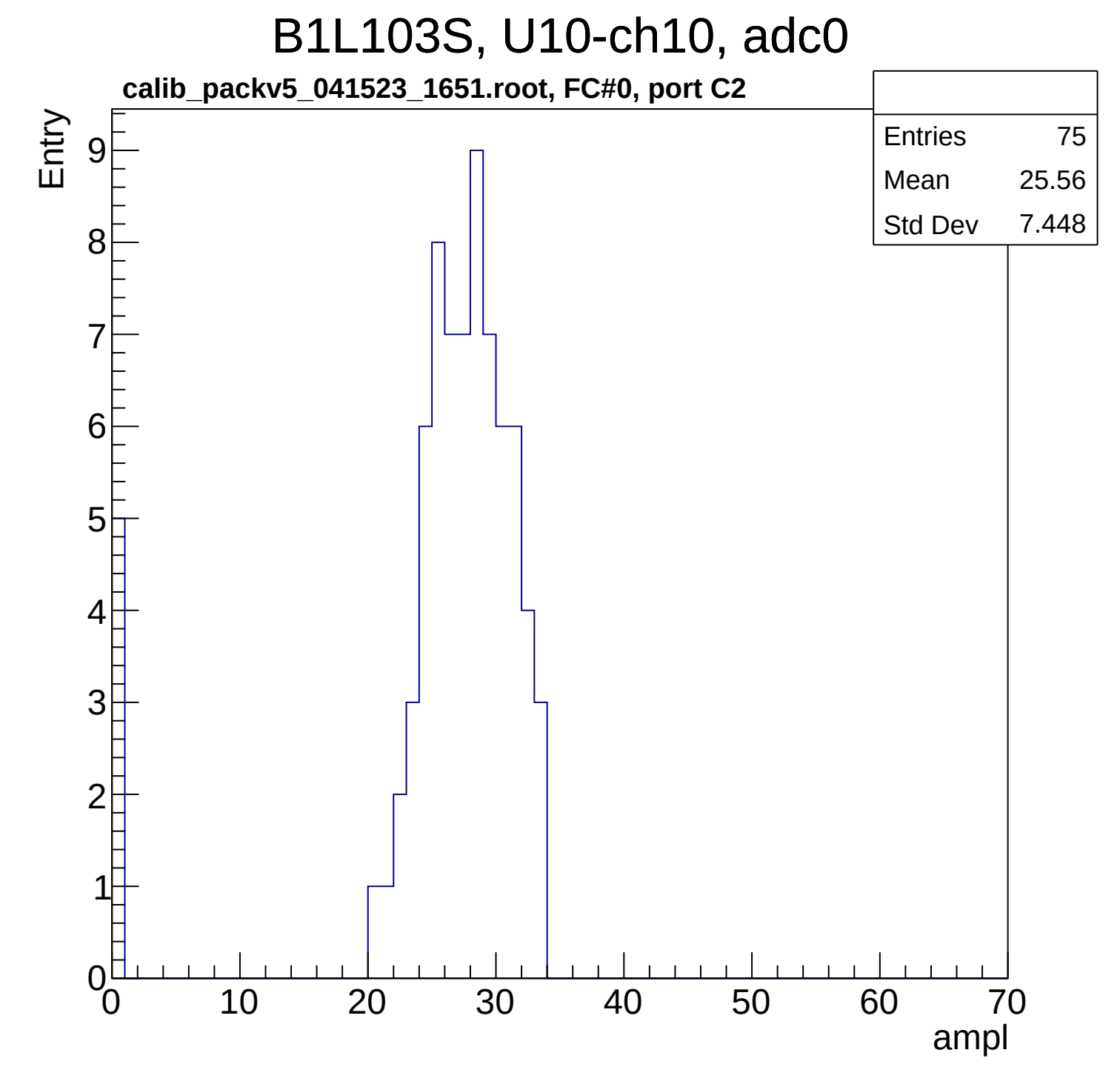
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch10, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 25.56
Std Dev 7.448
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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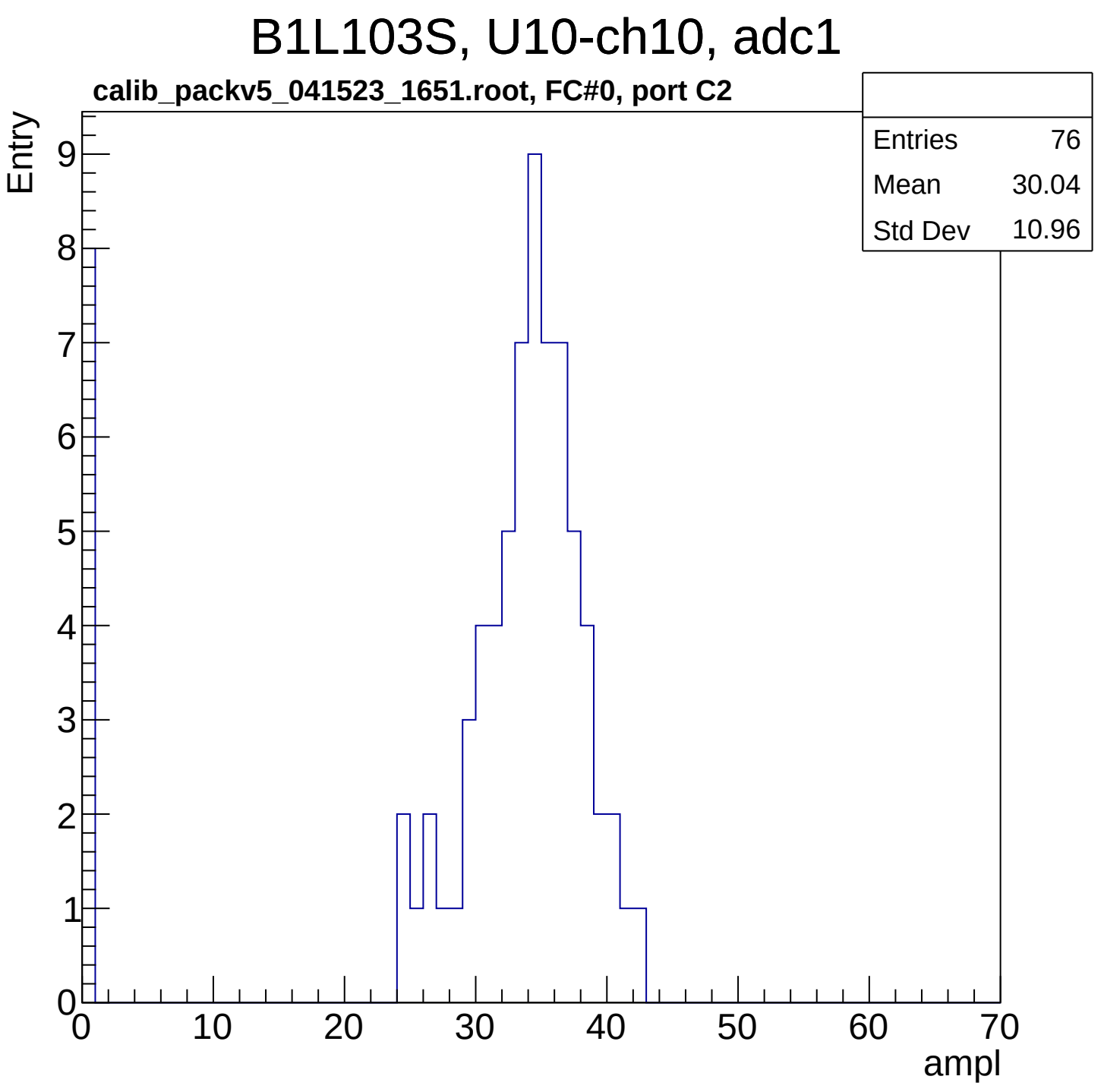
40
50
60
70


B1L103S, U10-ch10, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 30.04
Std Dev 10.96
Entry
ampl
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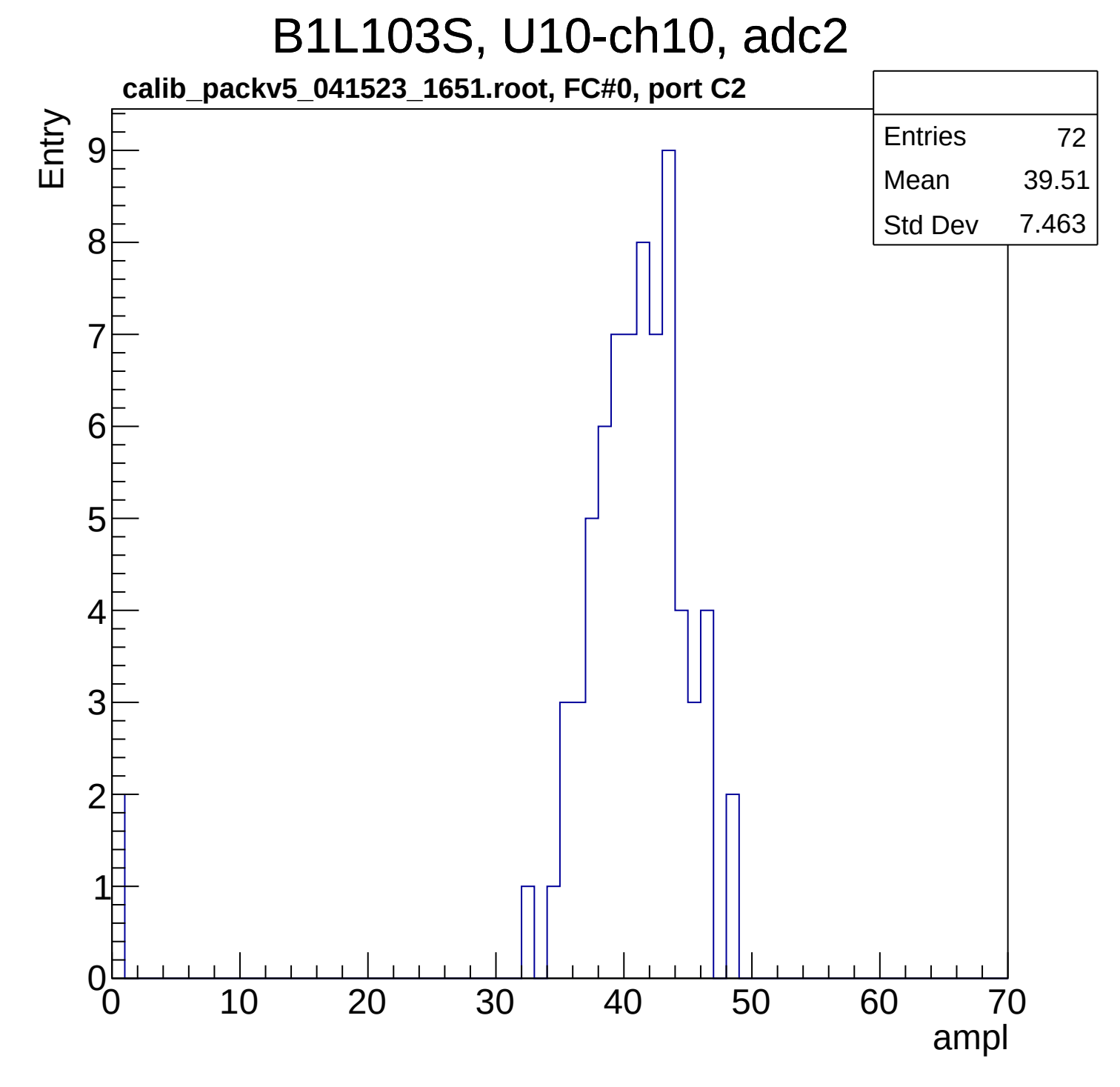
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U10-ch10, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 39.51
Std Dev 7.463
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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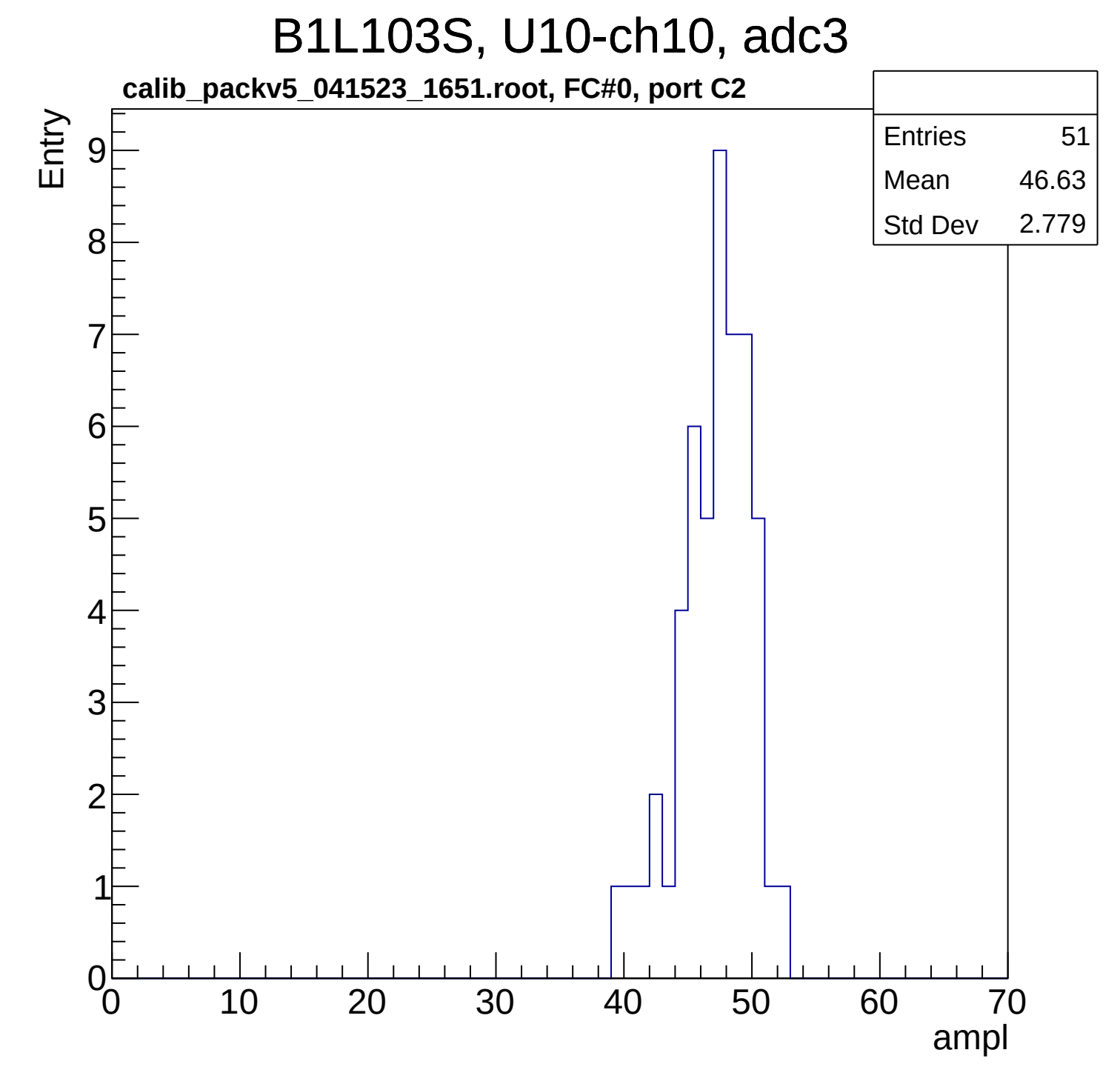
40
50
60
70


B1L103S, U10-ch10, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 46.63
Std Dev 2.779
Entry
ampl
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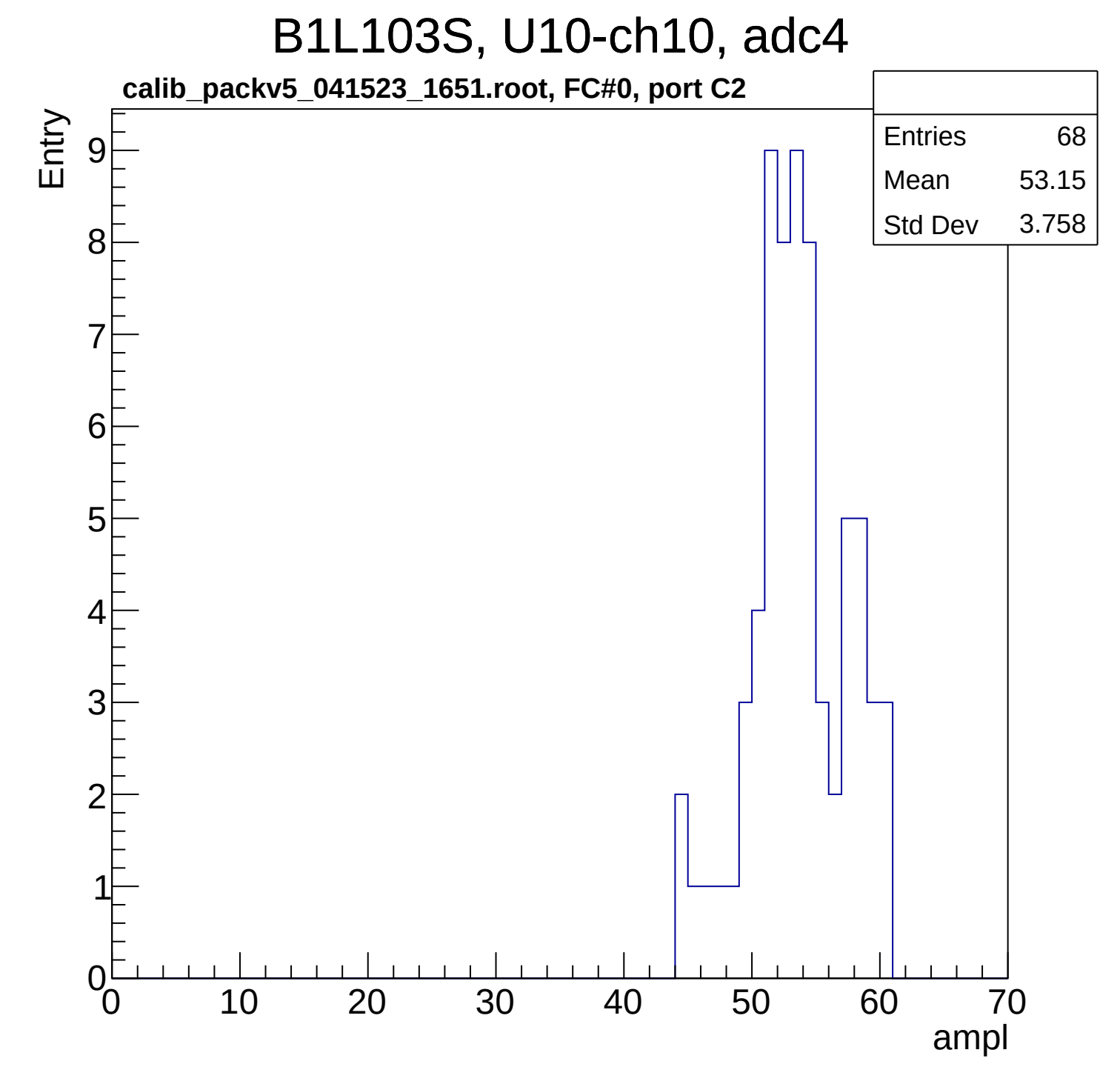
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U10-ch10, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 53.15
Std Dev 3.758
Entry
ampl
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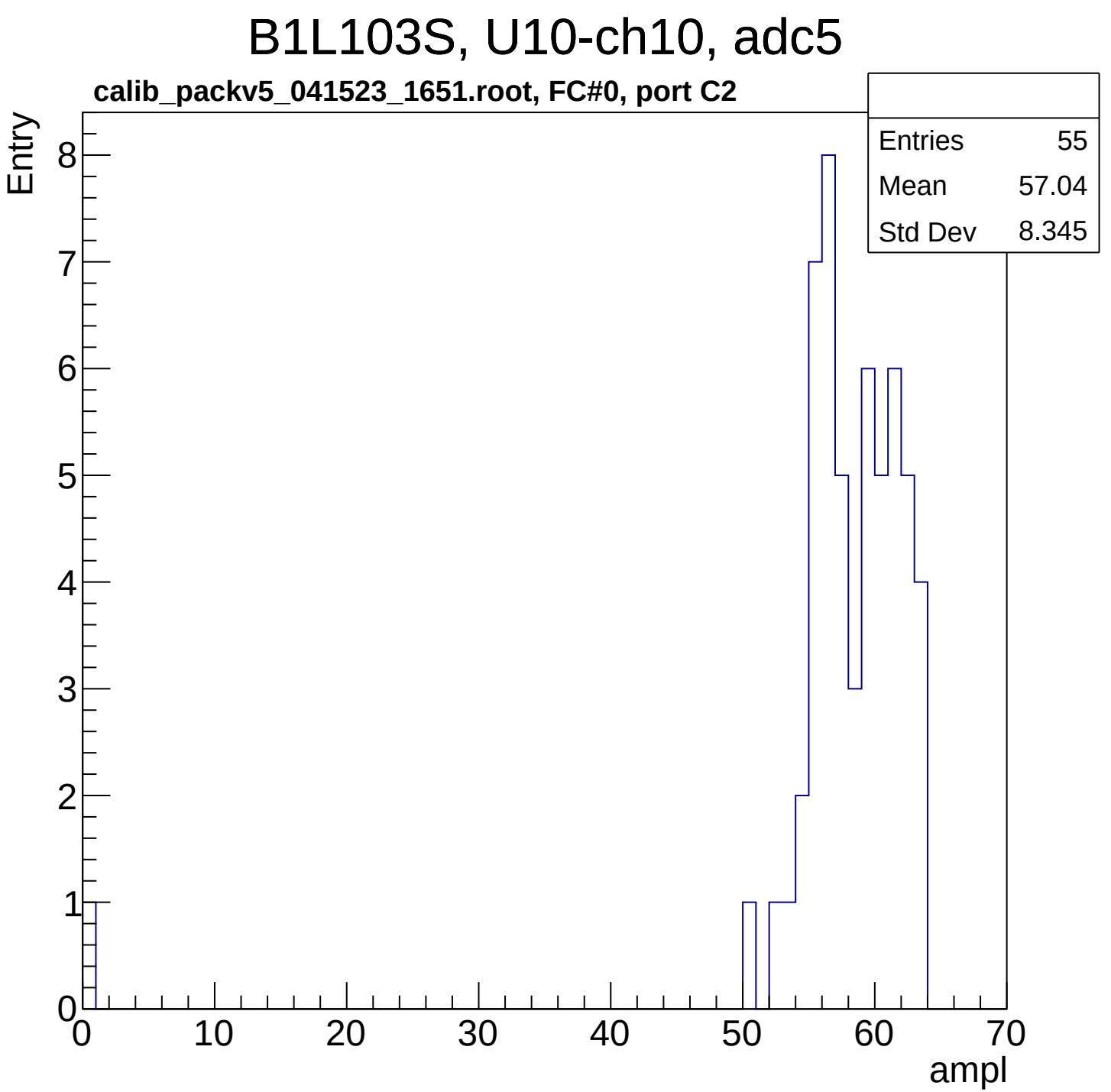
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U10-ch10, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 57.04
Std Dev 8.345
Entry
ampl
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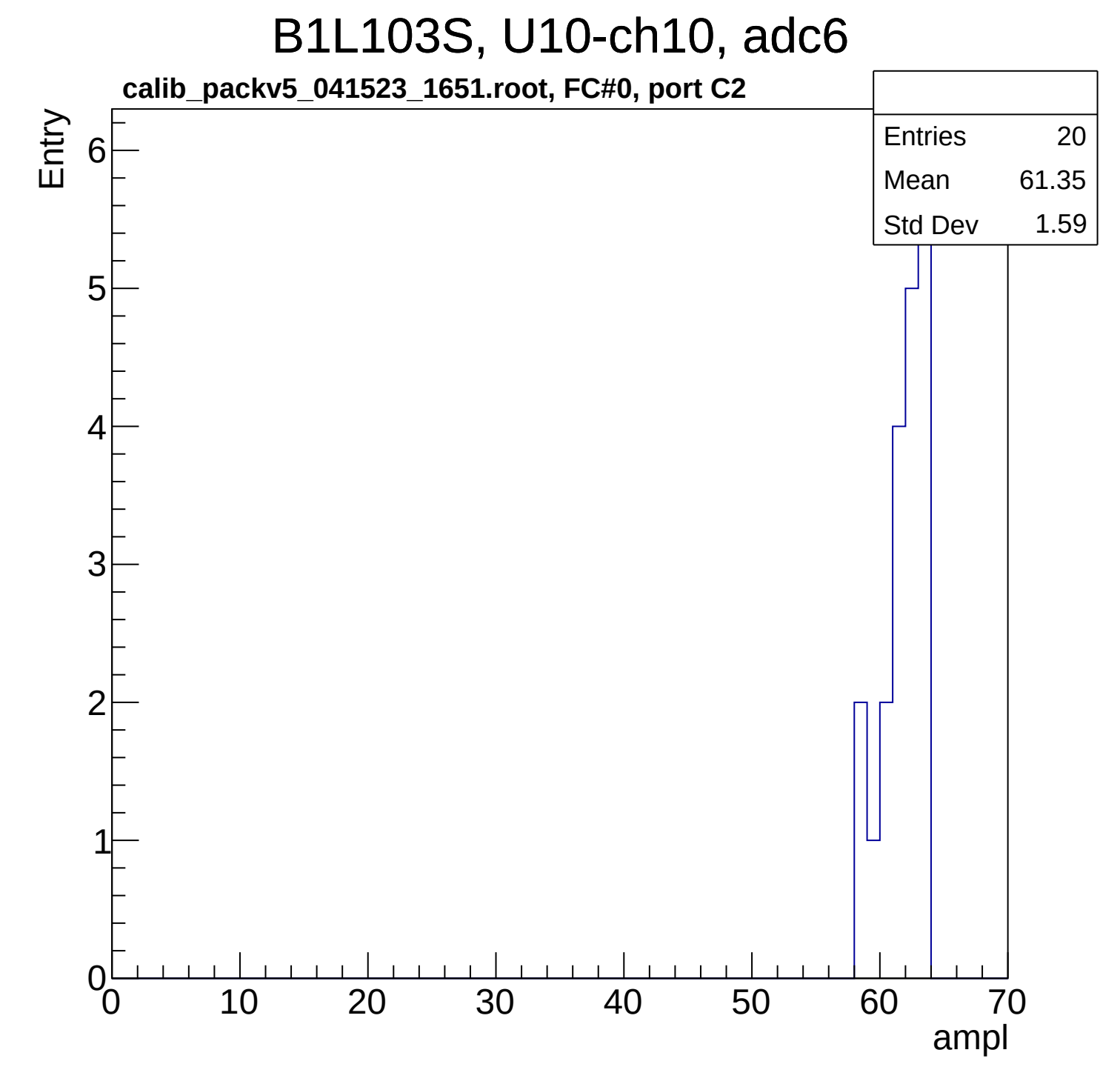
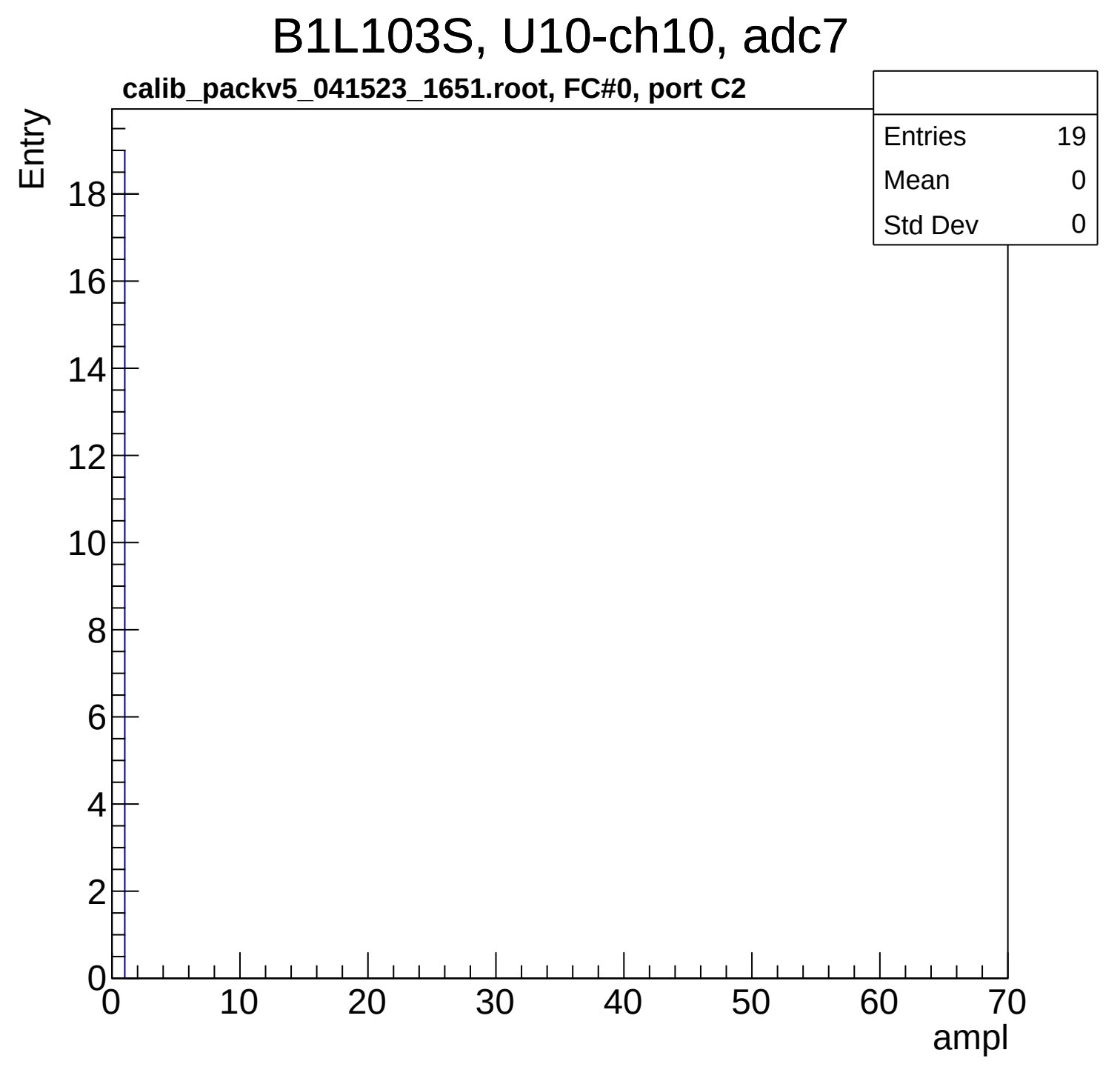
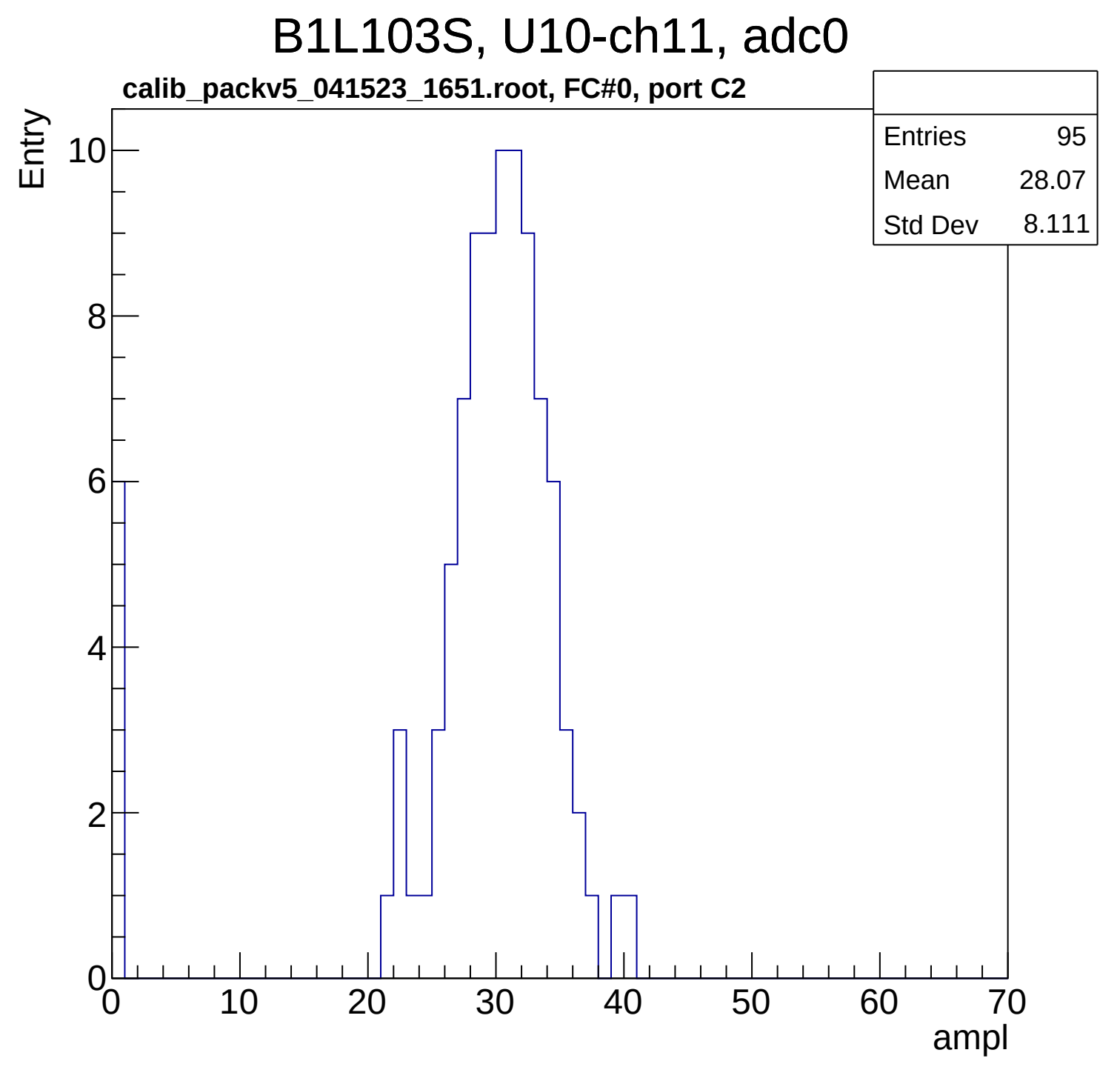
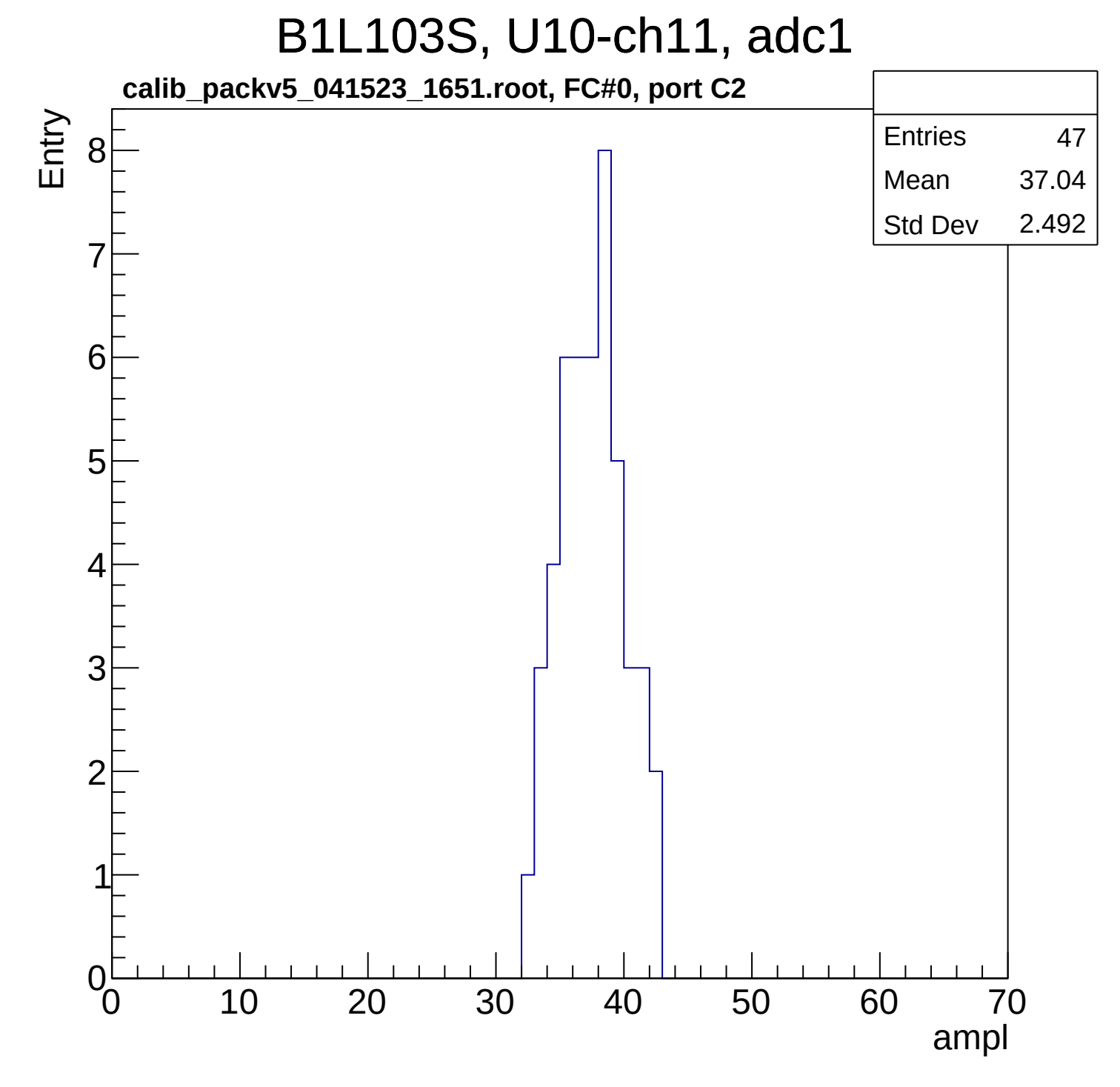
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U10-ch10, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 61.35
Std Dev 1.59
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U10-ch10, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch11, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 95
Mean 28.07
Std Dev 8.111
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U10-ch11, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 37.04
Std Dev 2.492
Entry
ampl
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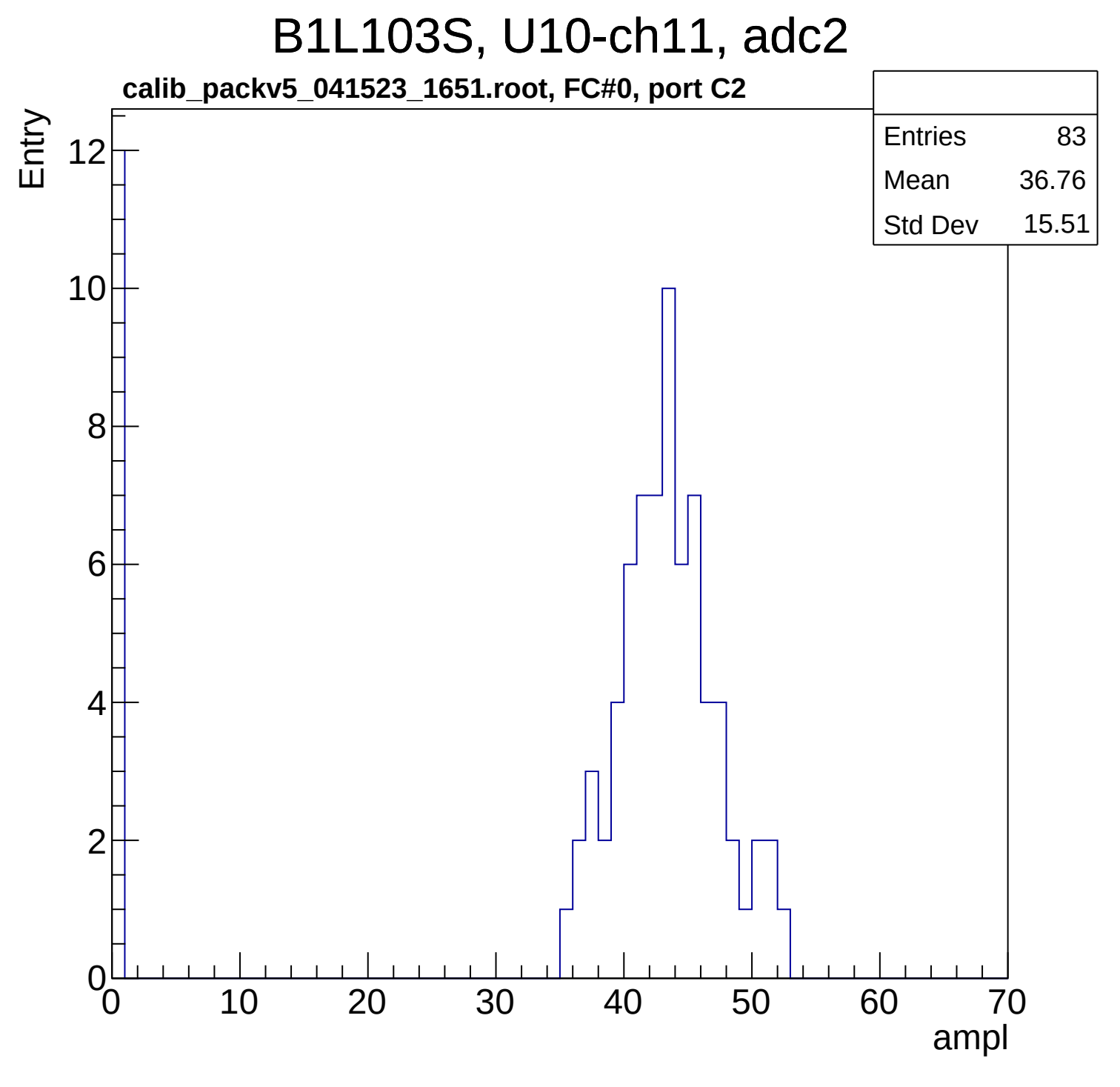
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U10-ch11, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 36.76
Std Dev 15.51
Entry
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2
4
6
8
10
12
0
10
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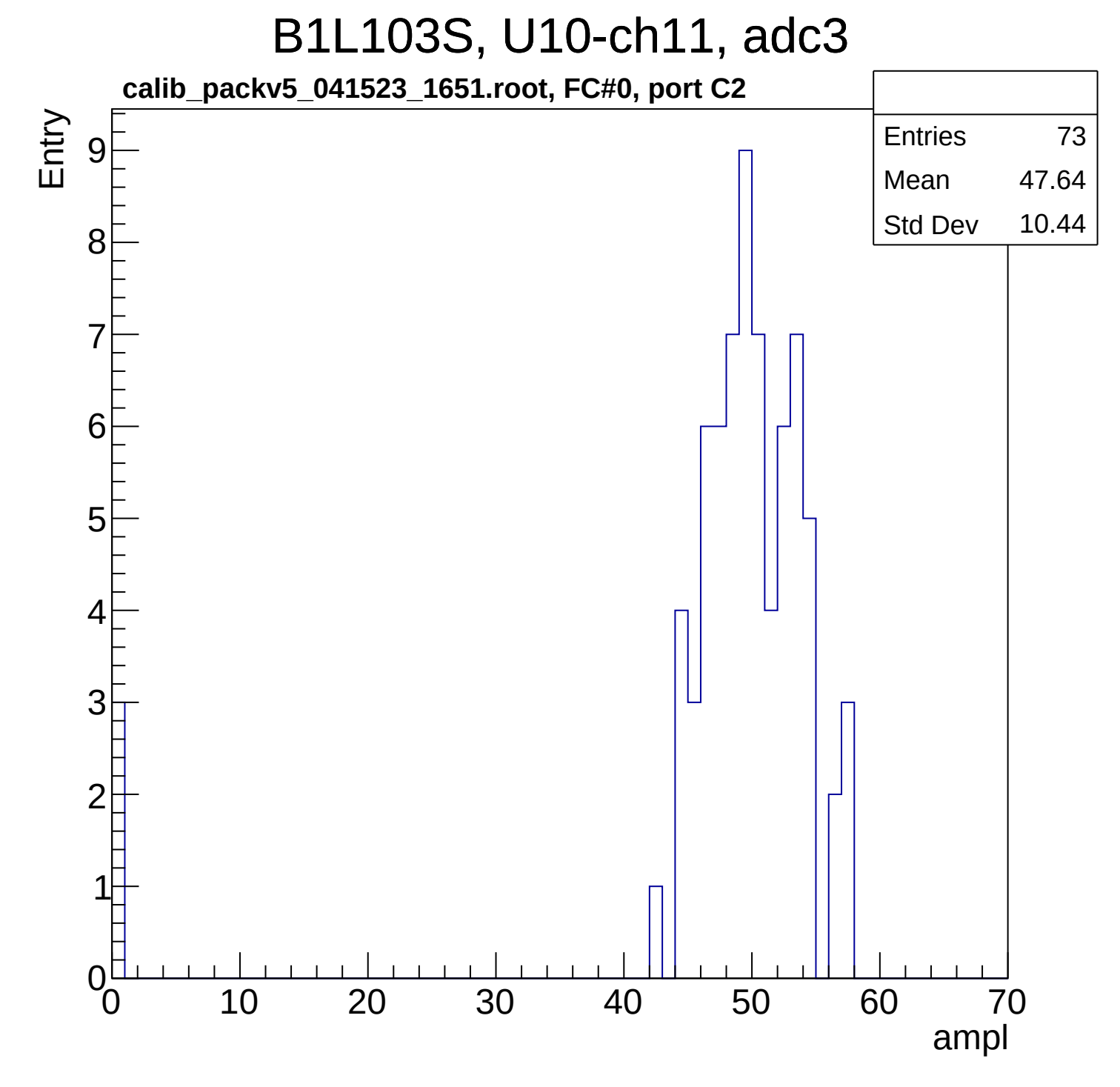
50
60
70
ampl


B1L103S, U10-ch11, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 47.64
Std Dev 10.44
Entry
ampl
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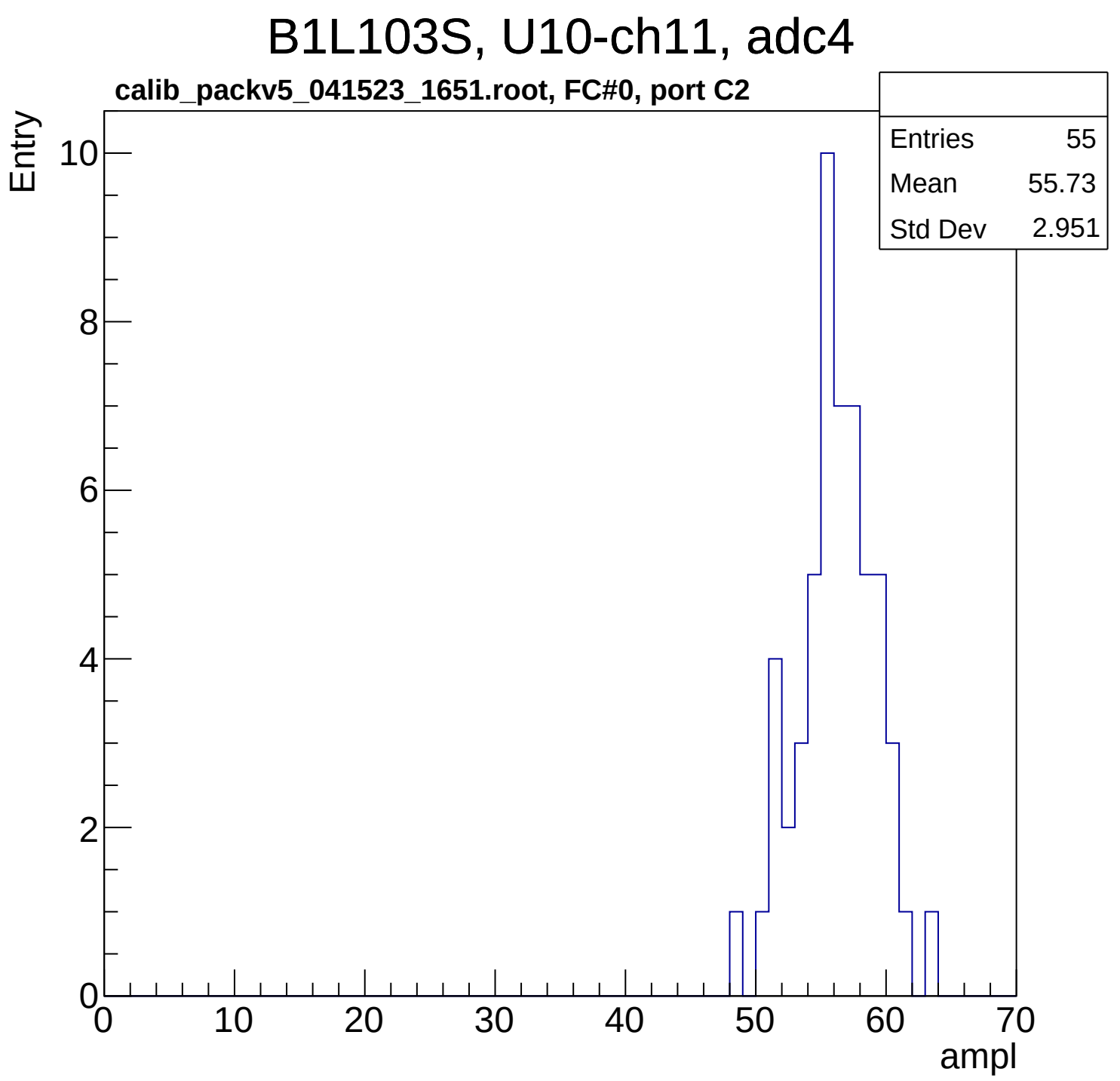
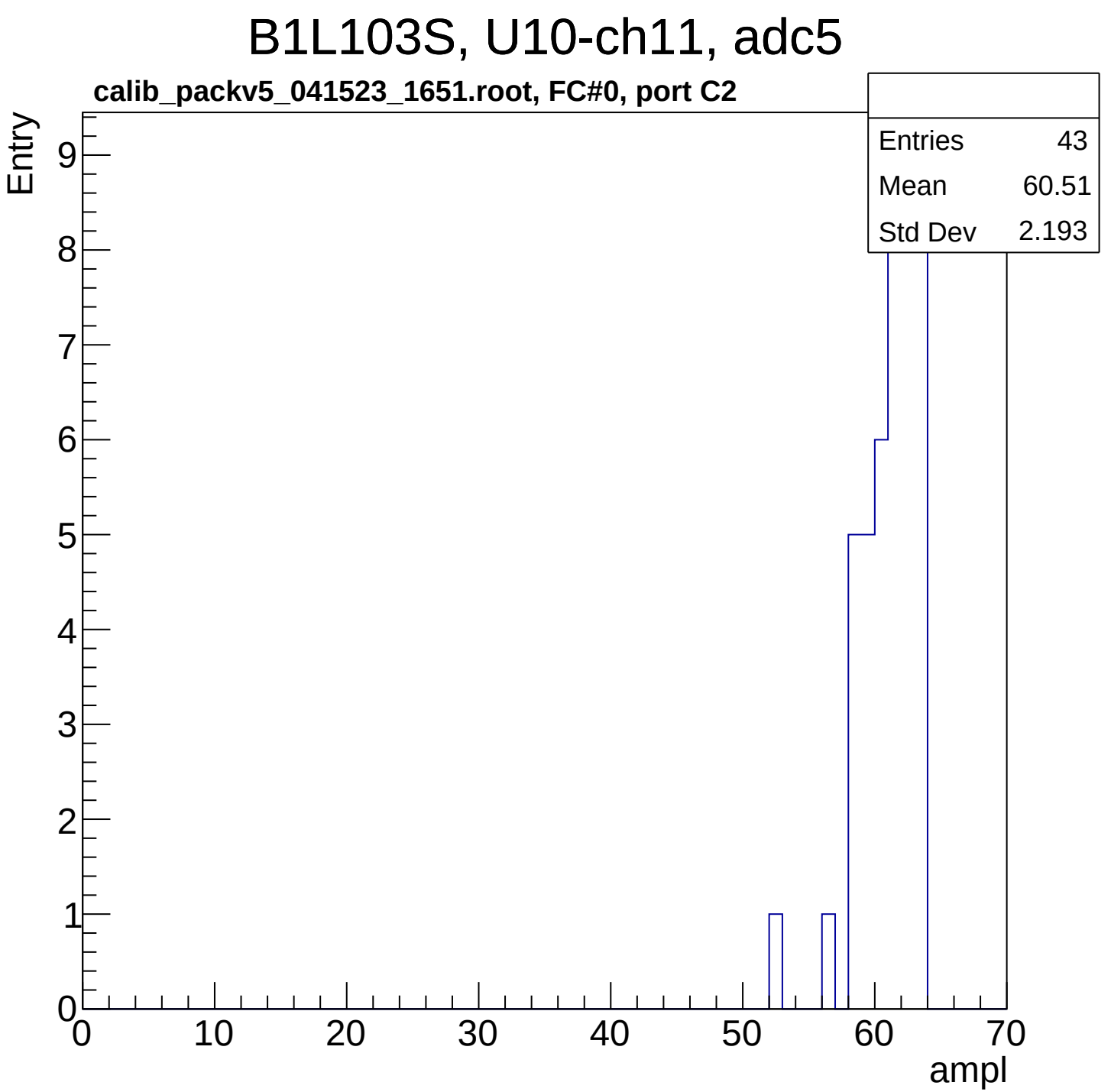
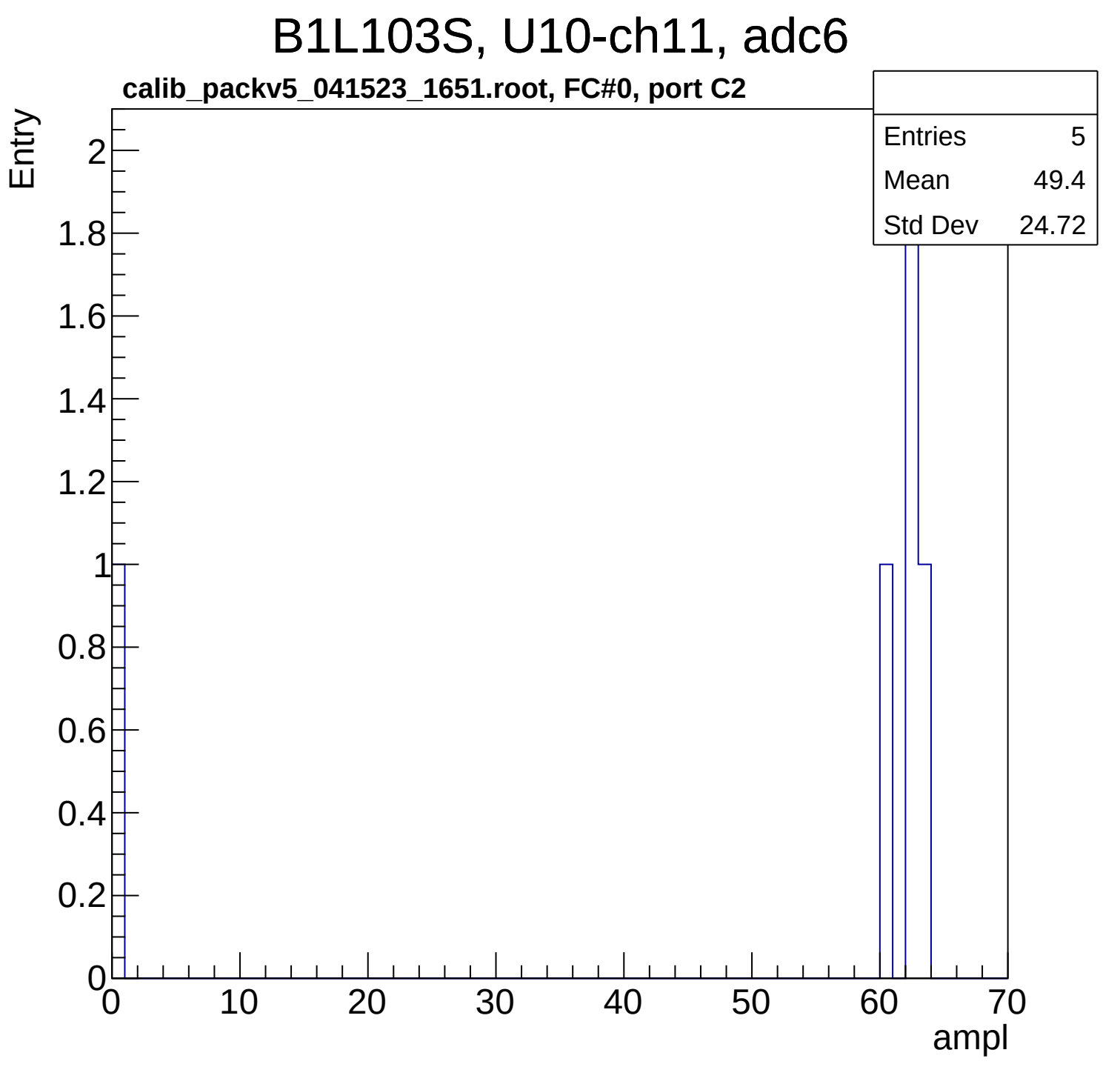
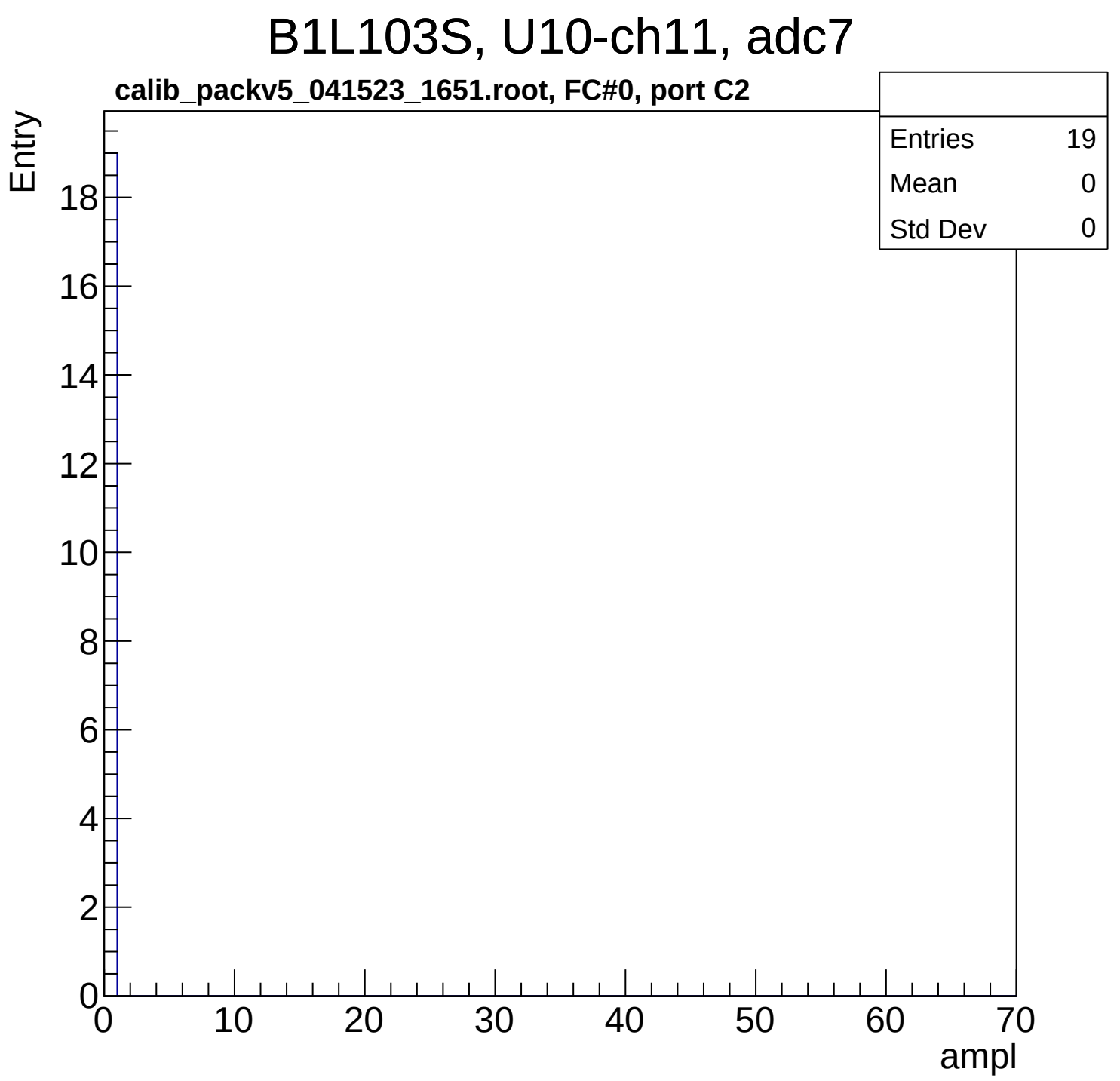
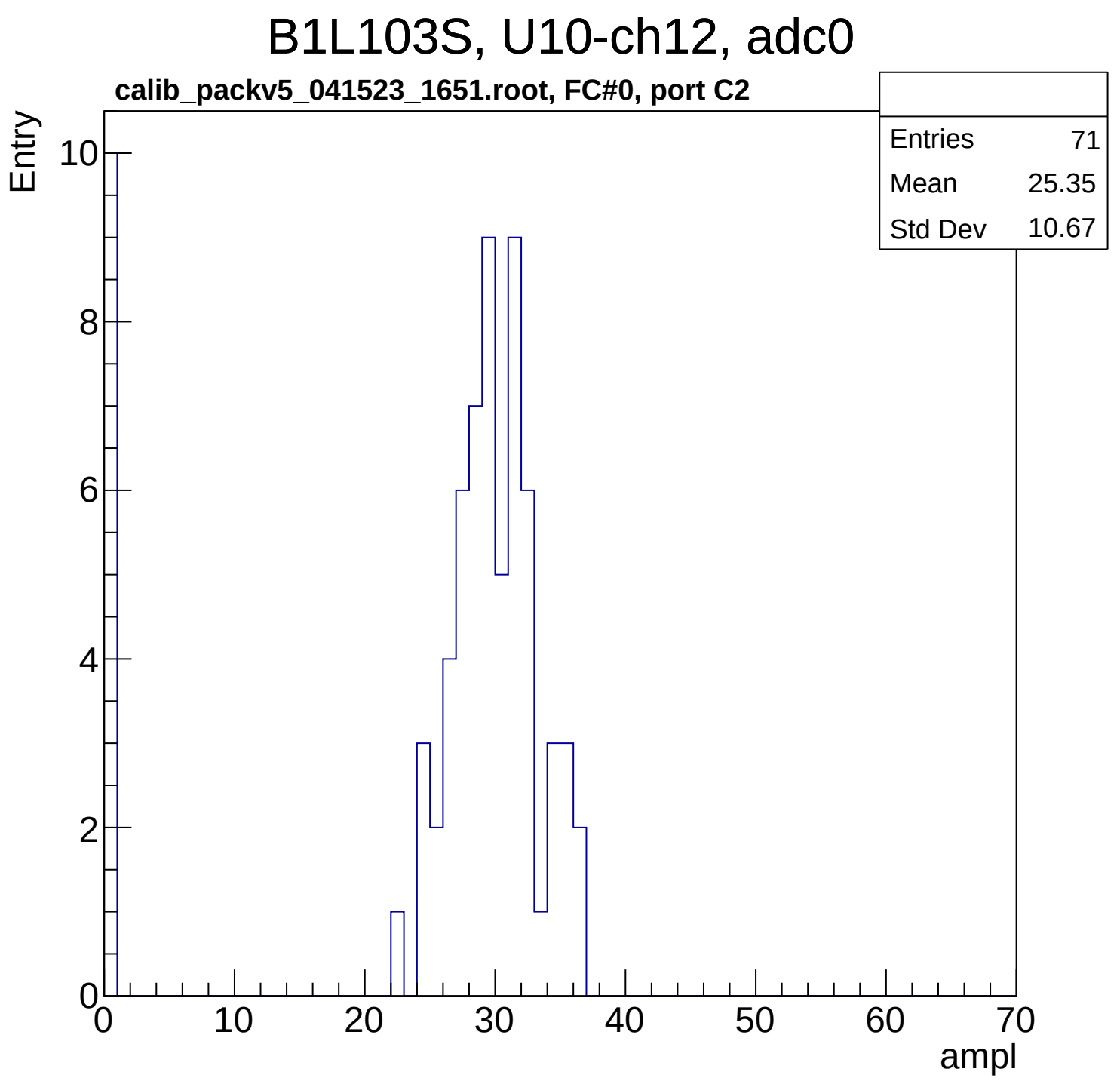
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

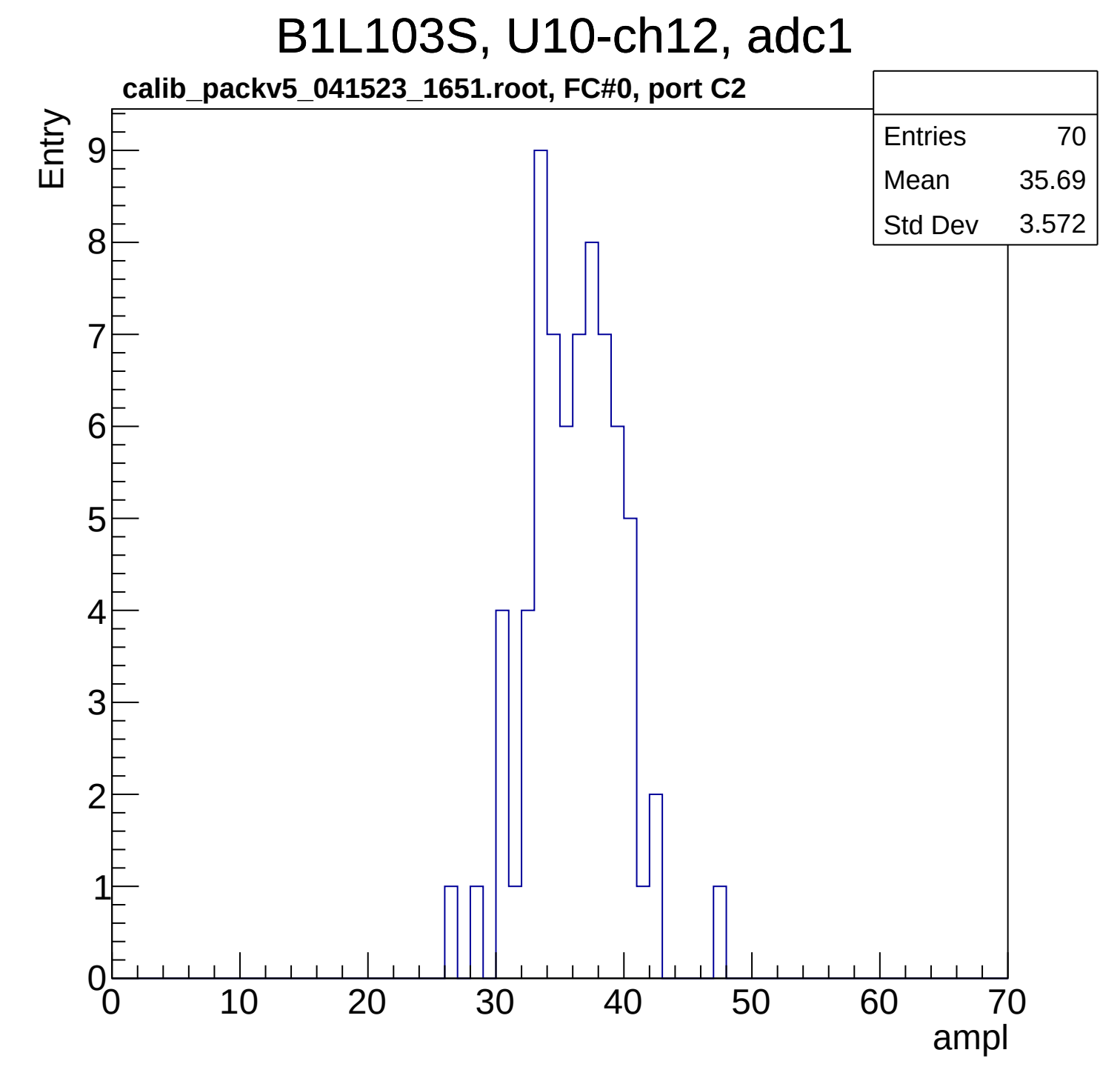

B1L103S, U10-ch11, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 55.73
Std Dev 2.951
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

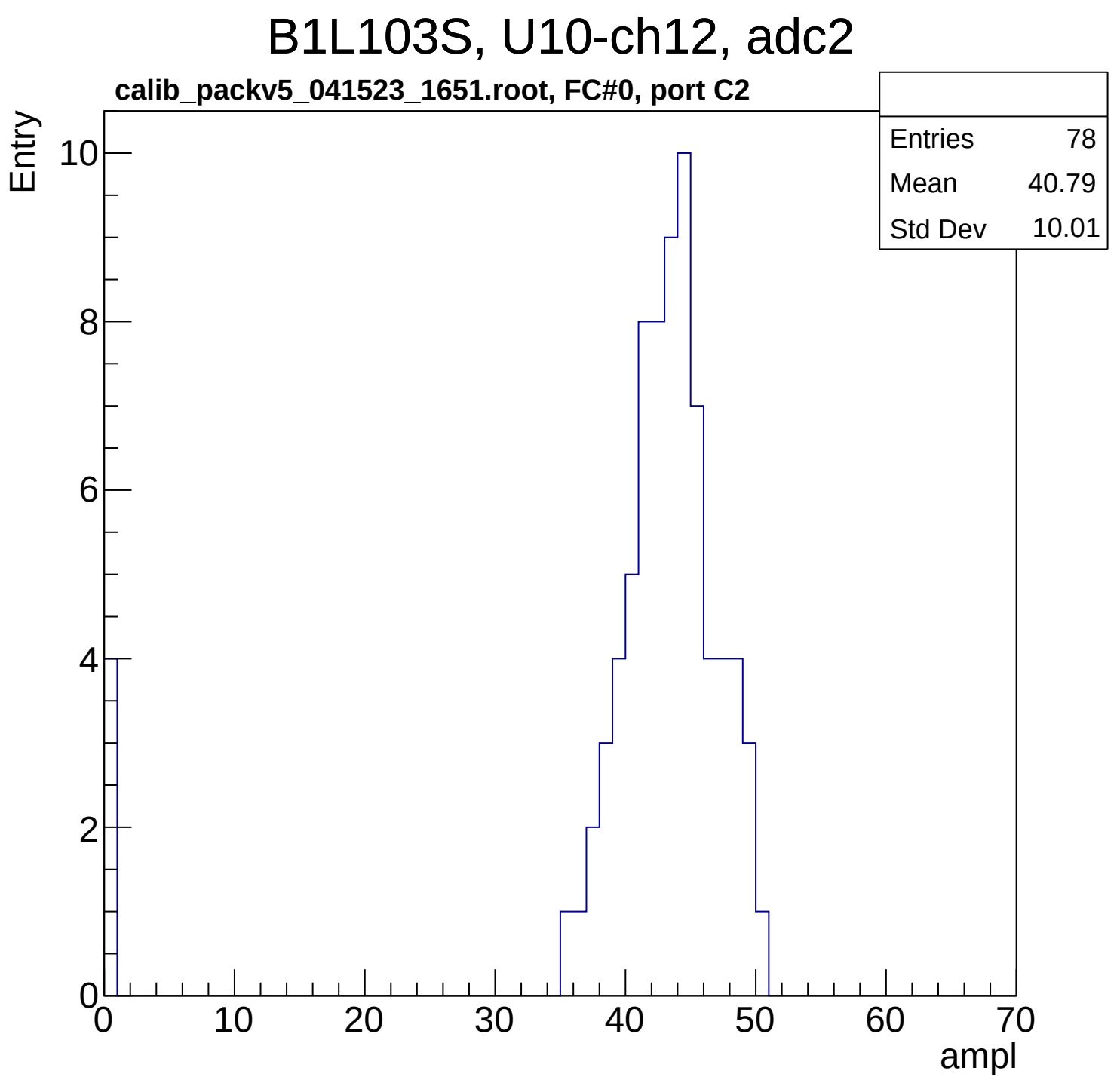

B1L103S, U10-ch11, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 43
Mean 60.51
Std Dev 2.193
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

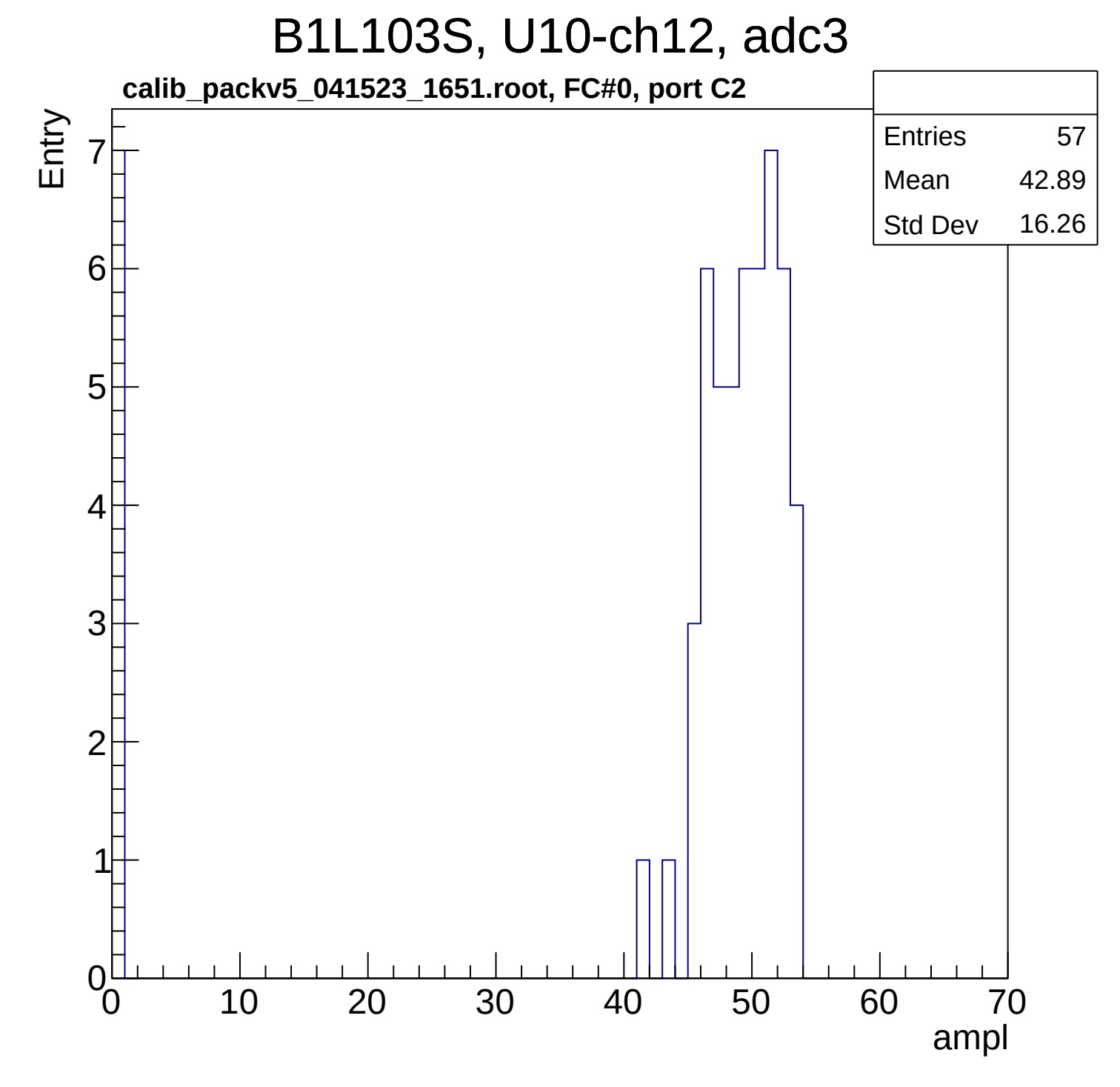

B1L103S, U10-ch11, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 5
Mean 49.4
Std Dev 24.72
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

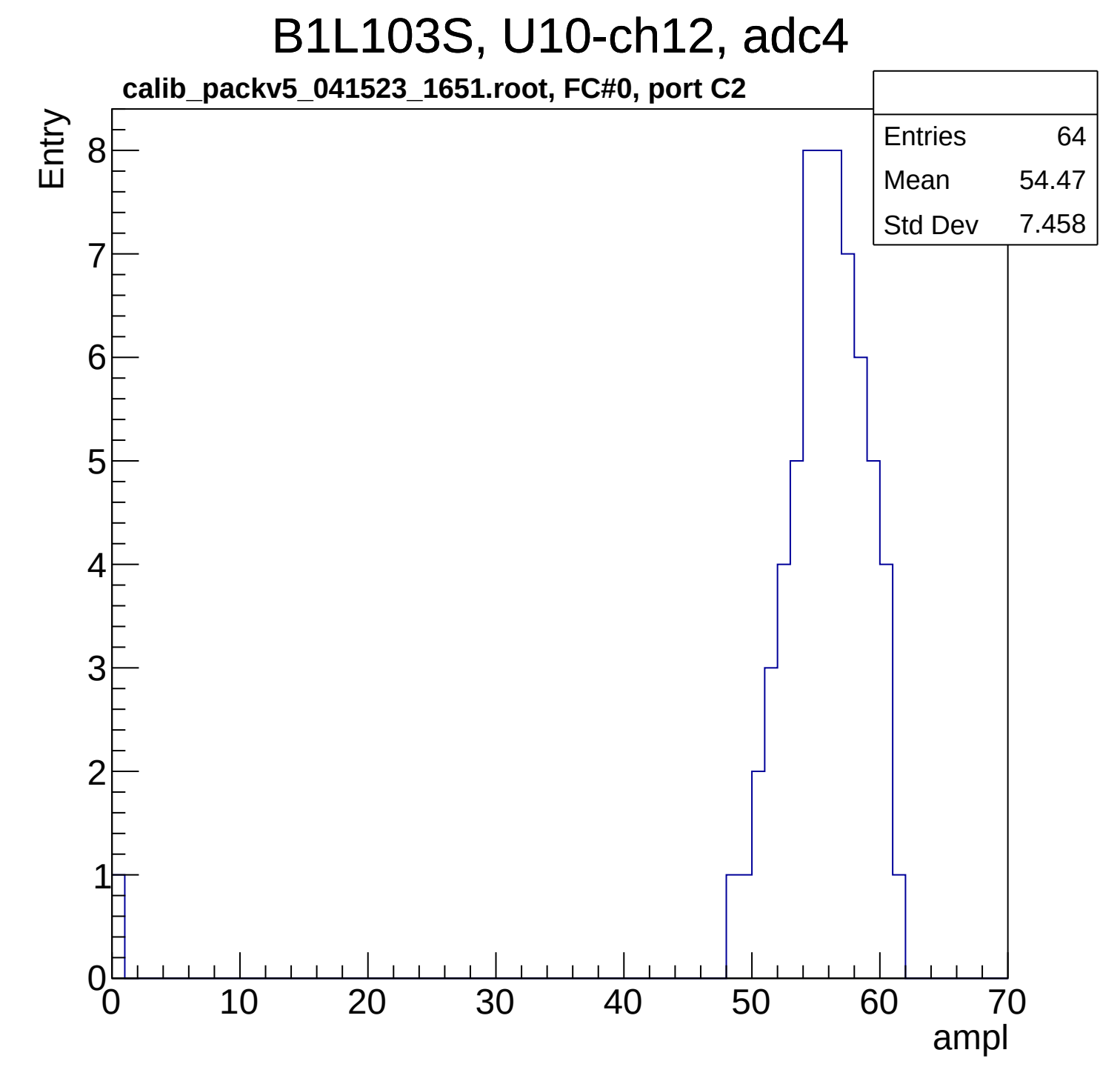

B1L103S, U10-ch11, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

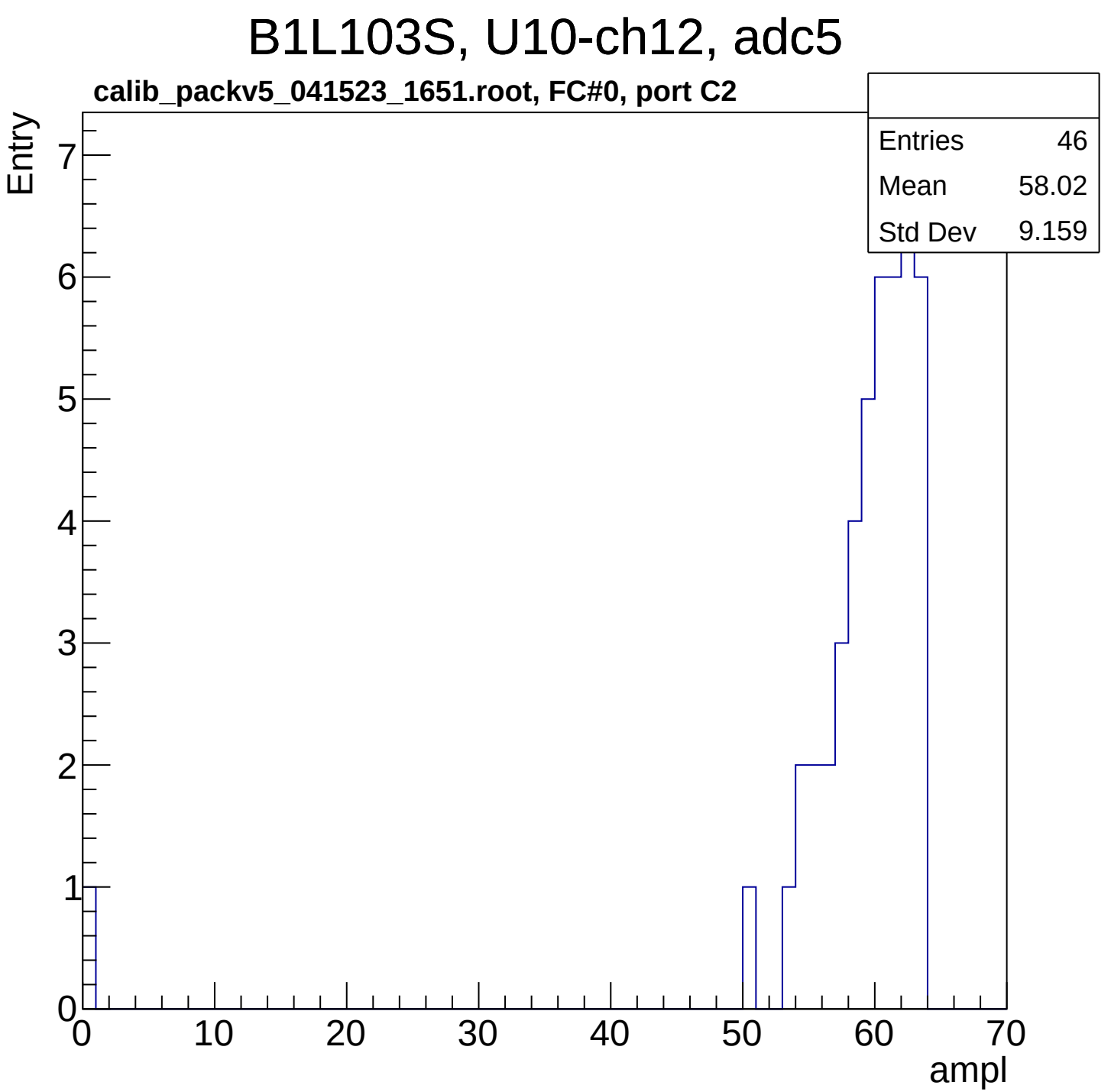

B1L103S, U10-ch12, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 25.35
Std Dev 10.67
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

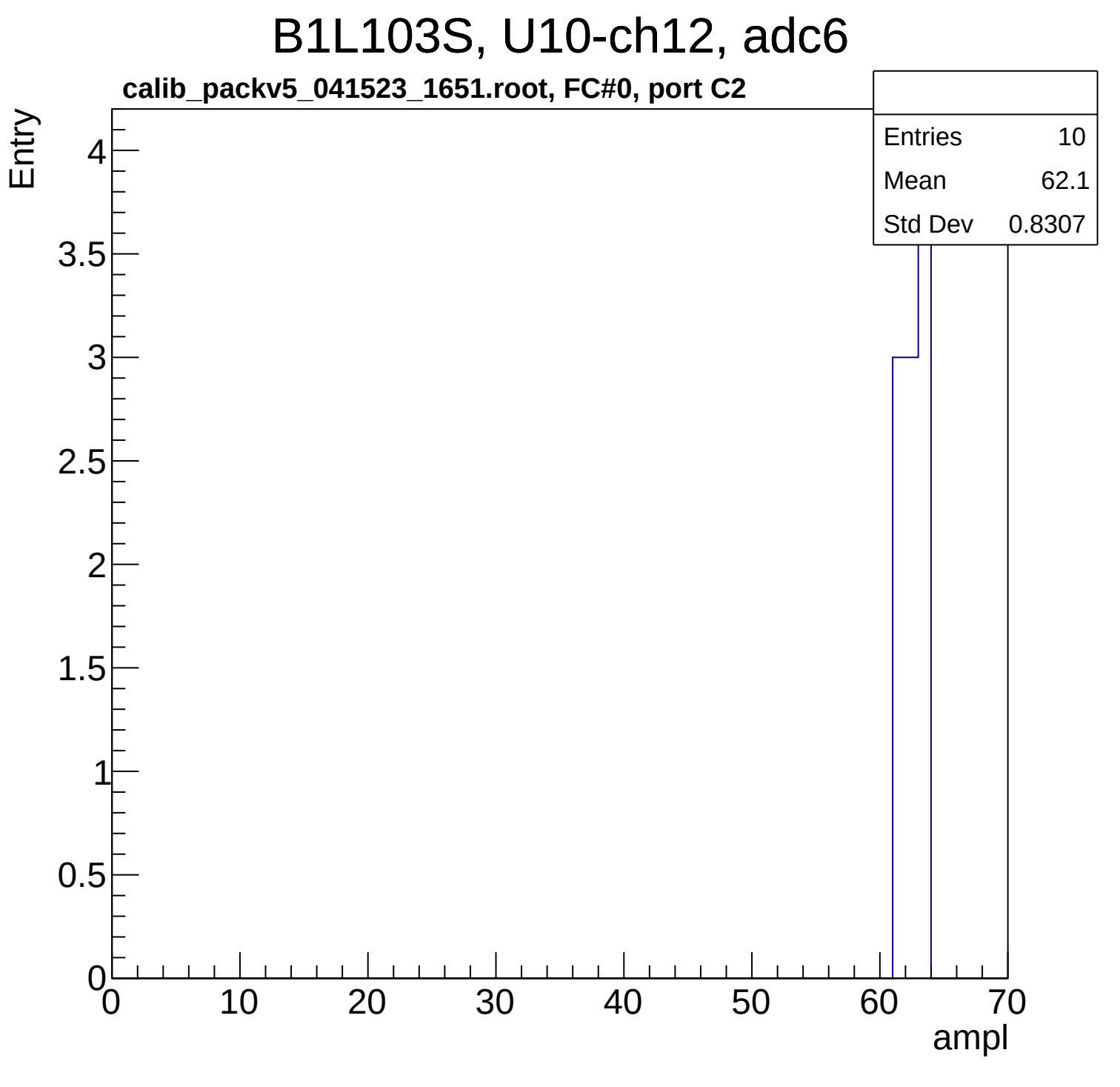

B1L103S, U10-ch12, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 35.69
Std Dev 3.572
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

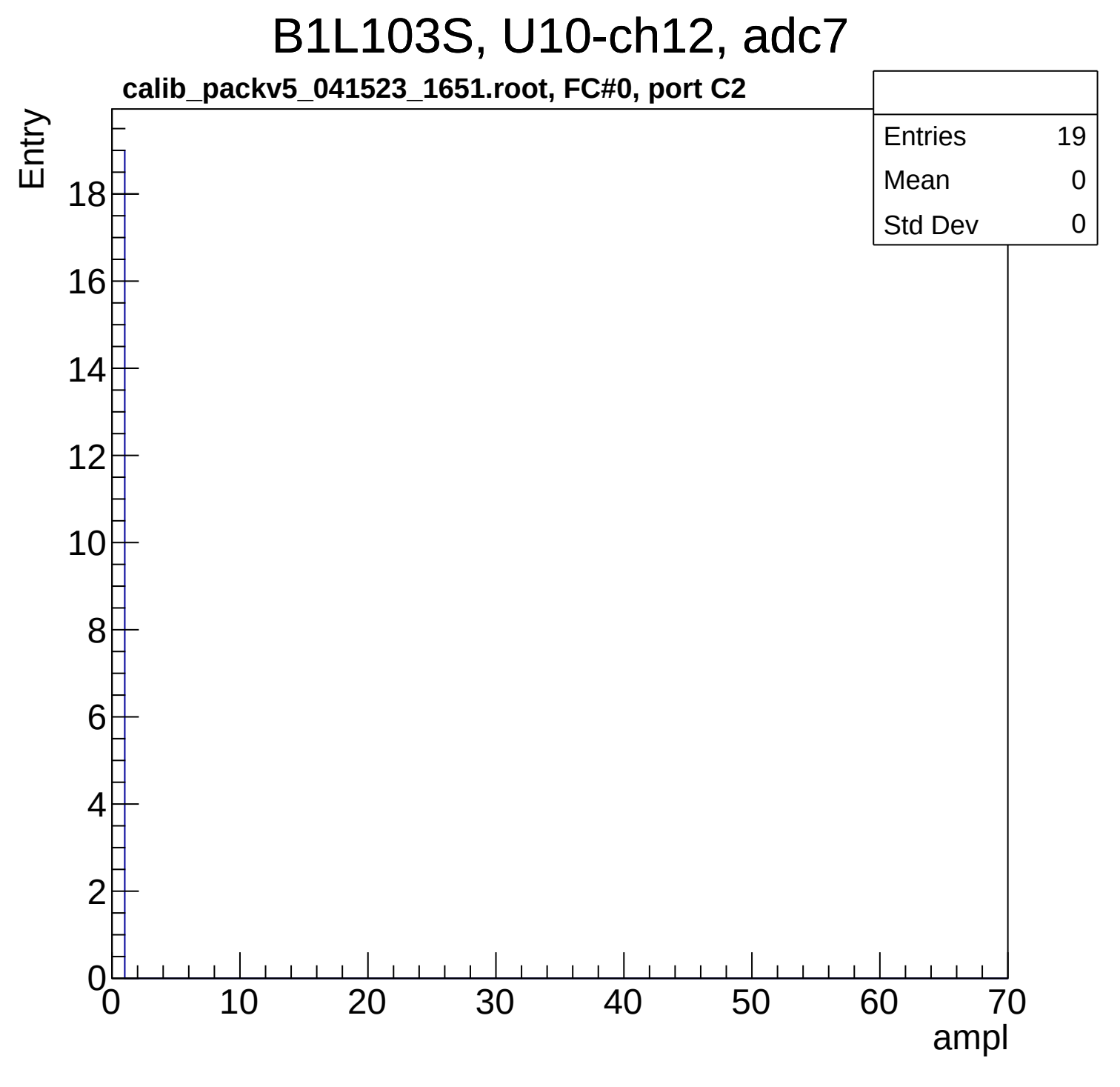

B1L103S, U10-ch12, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 40.79
Std Dev 10.01
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

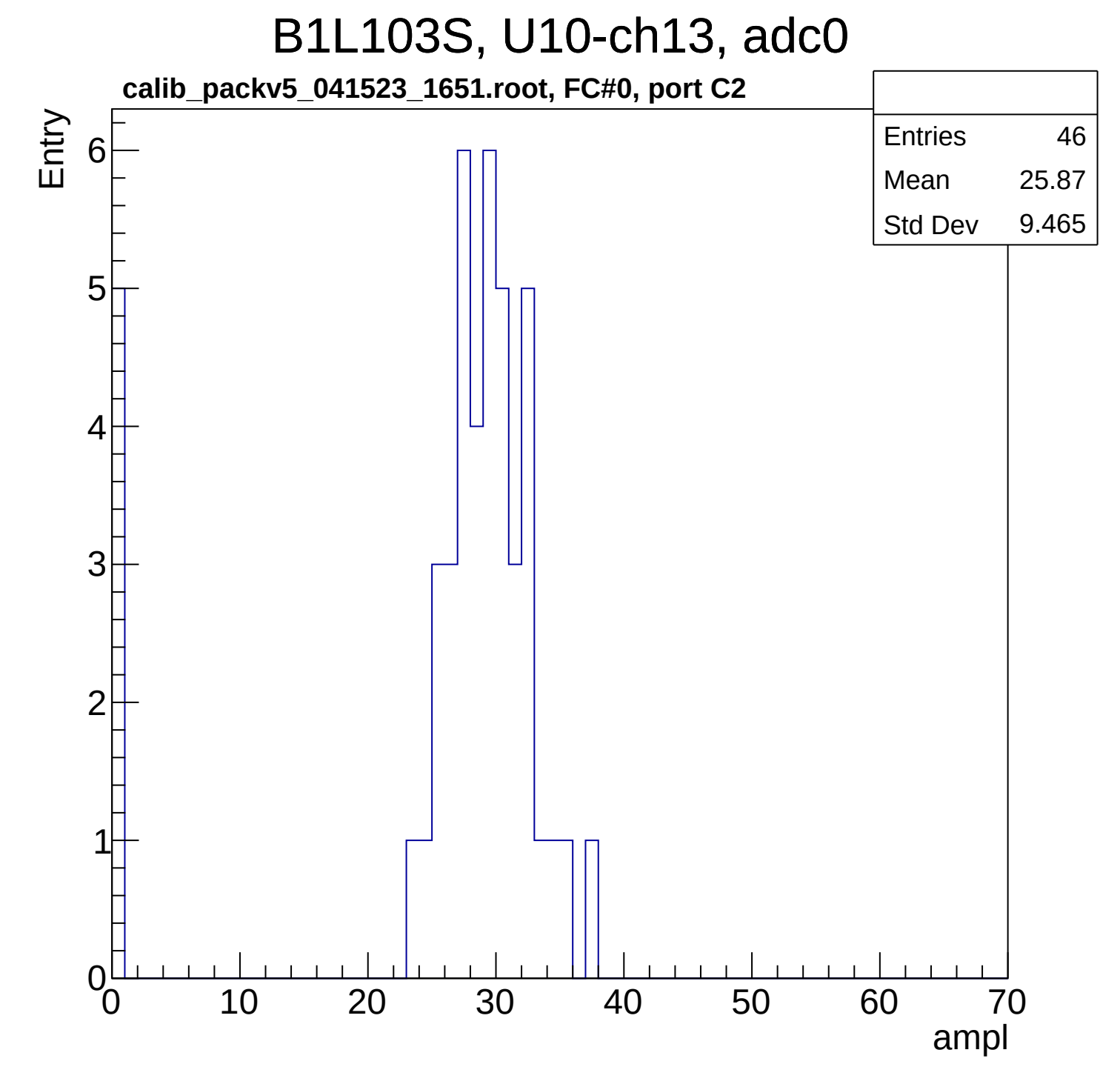

B1L103S, U10-ch12, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 42.89
Std Dev 16.26
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

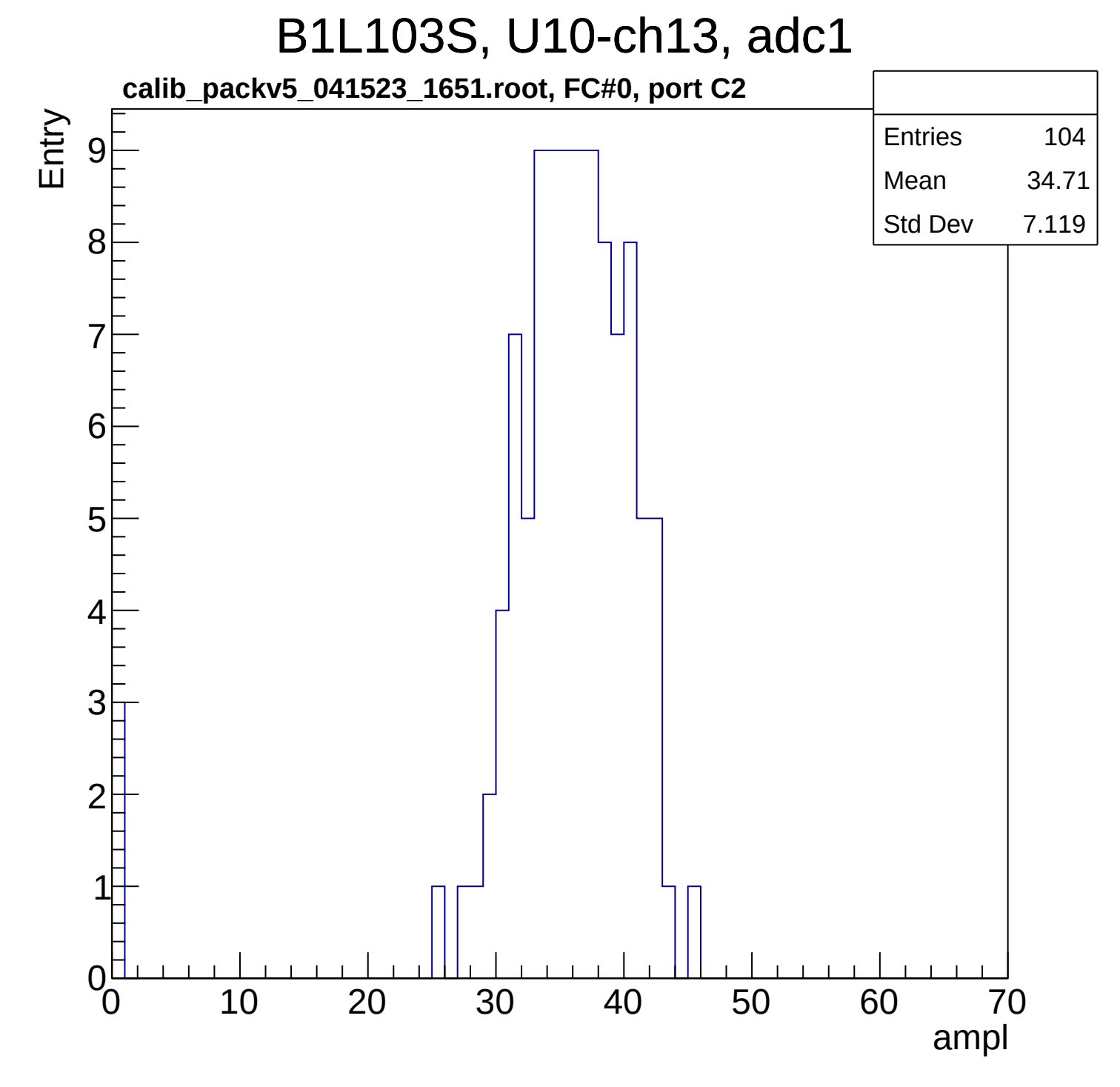

B1L103S, U10-ch12, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 54.47
Std Dev 7.458
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

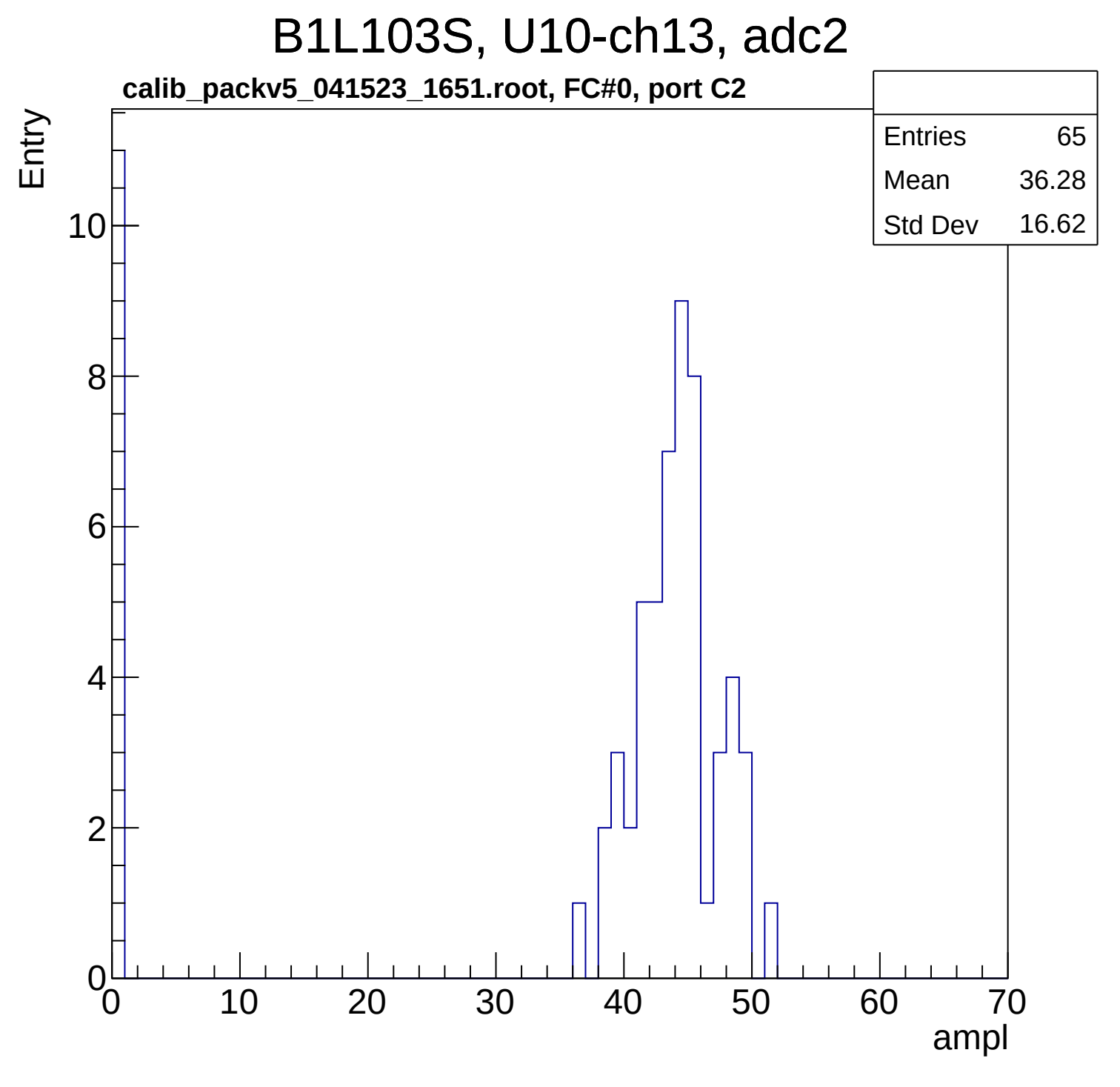

B1L103S, U10-ch12, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 58.02
Std Dev 9.159
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

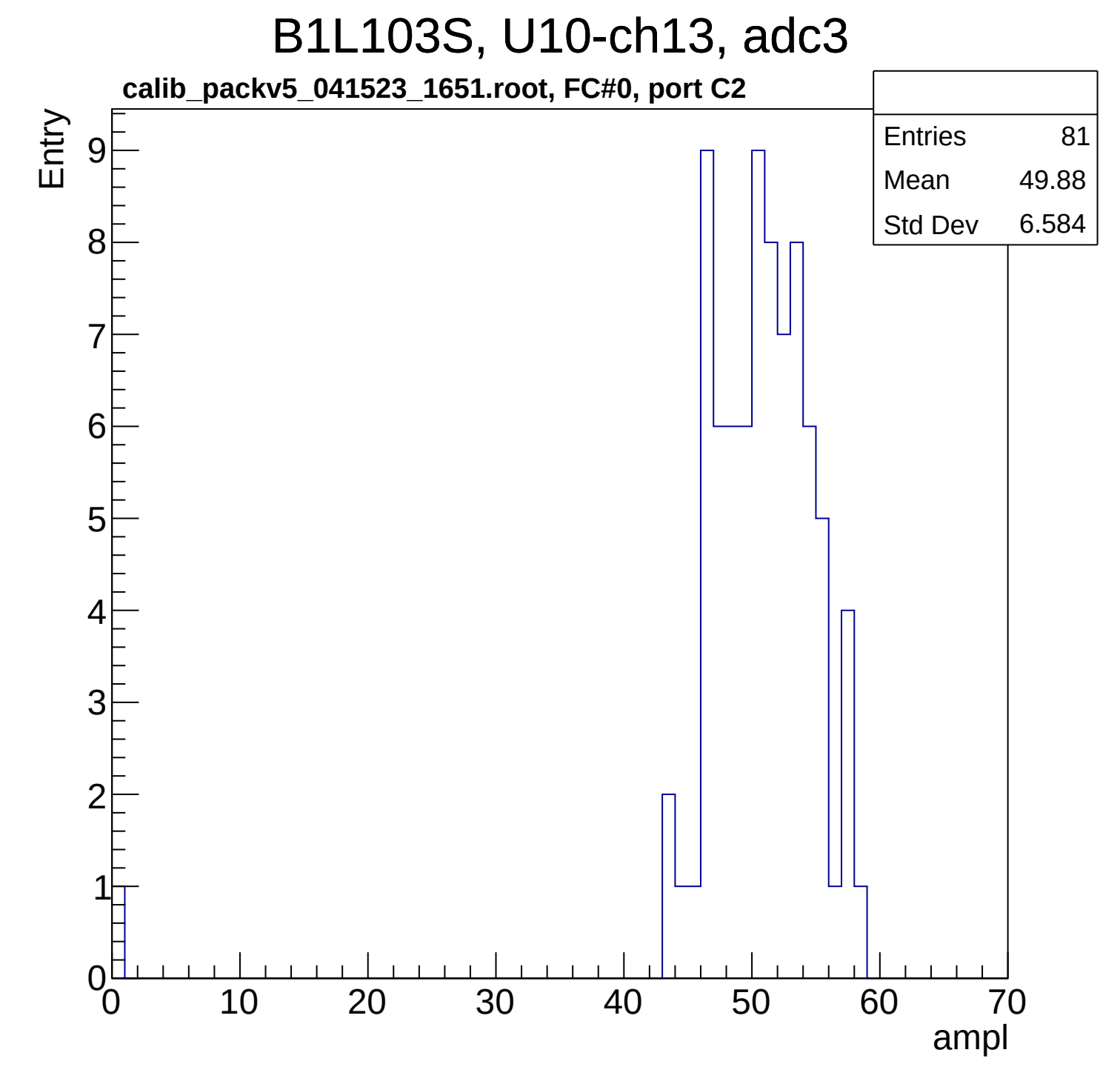

B1L103S, U10-ch12, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 62.1
Std Dev 0.8307
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

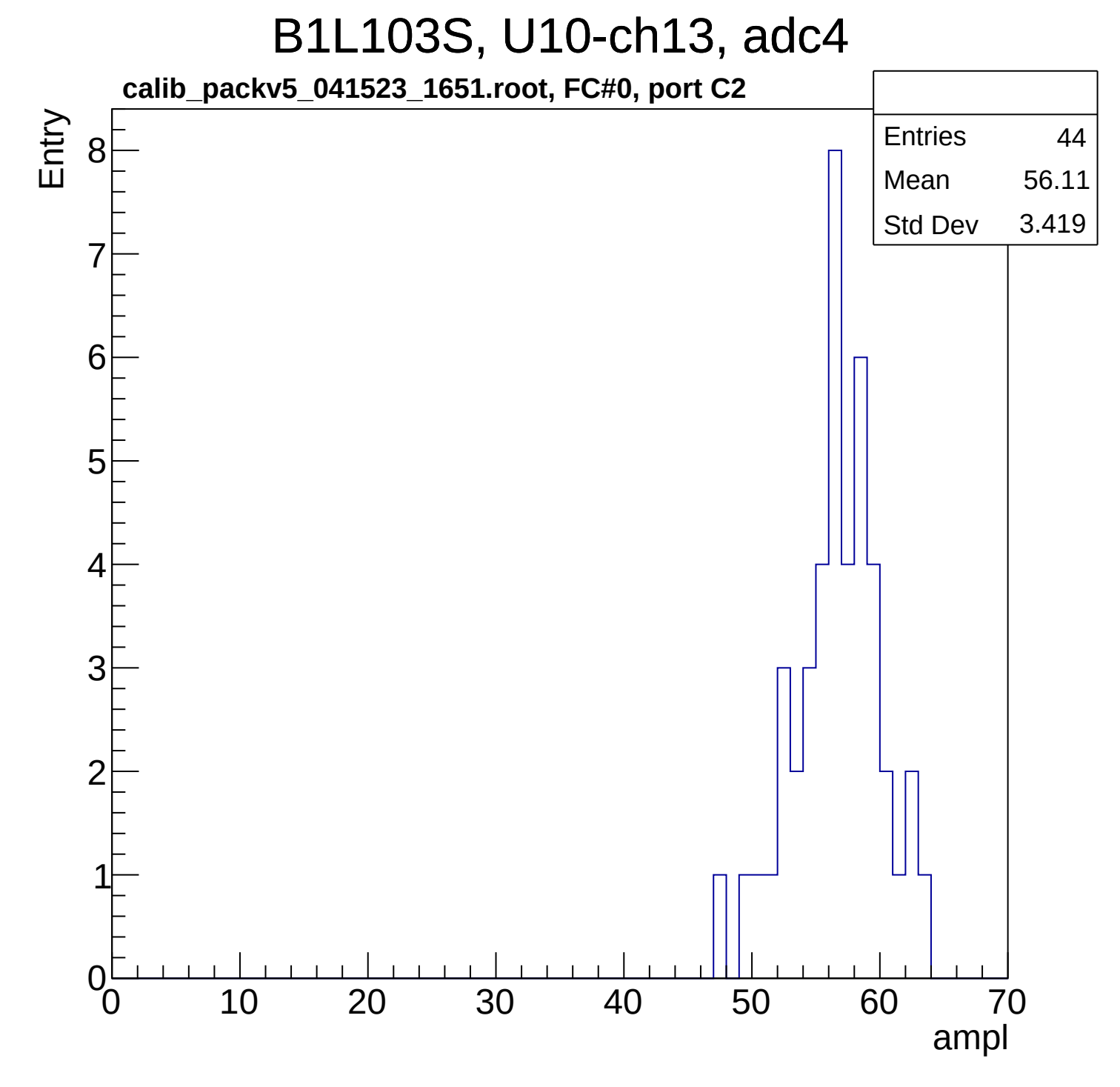

B1L103S, U10-ch12, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

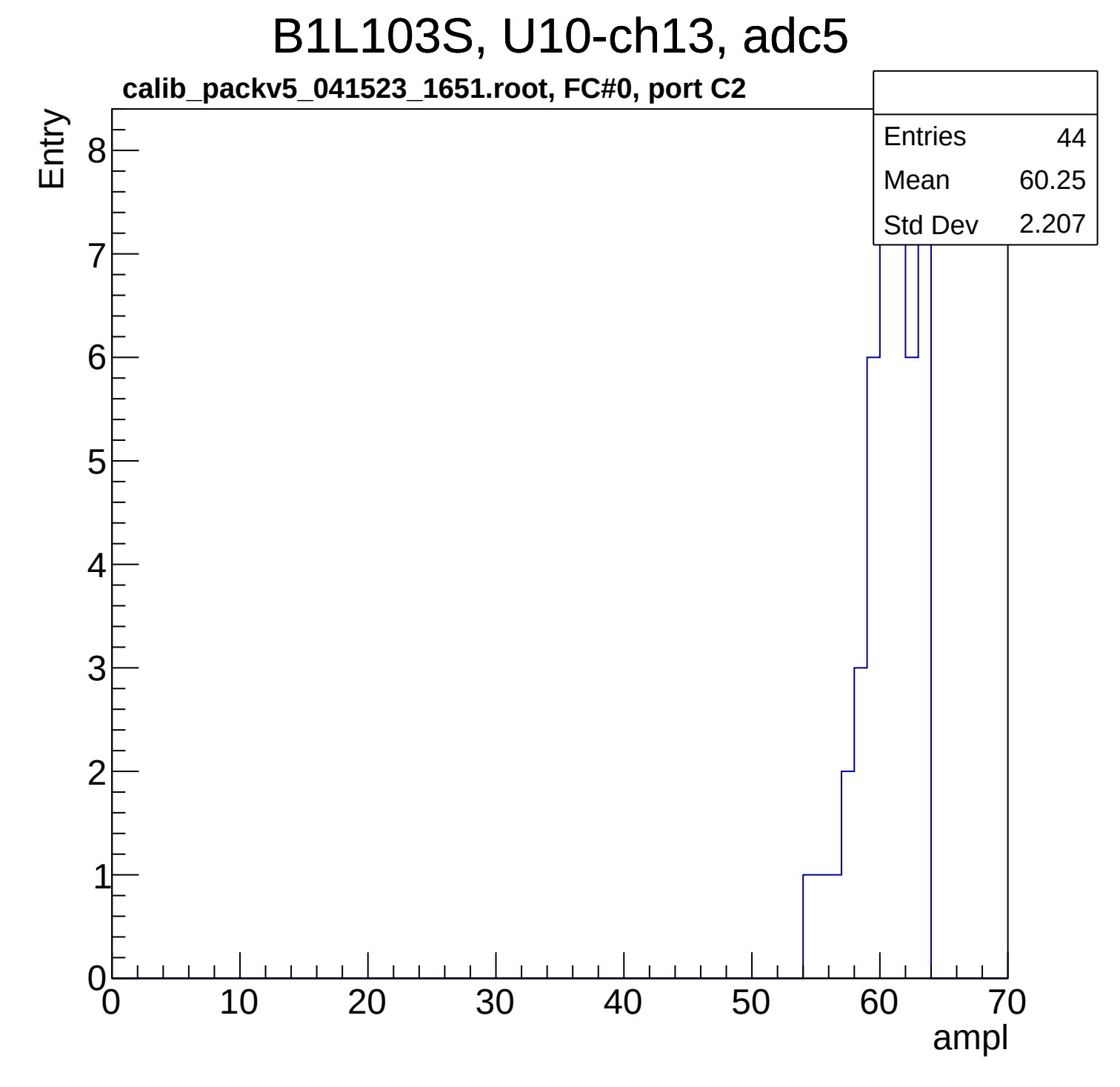

B1L103S, U10-ch13, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 25.87
Std Dev 9.465
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

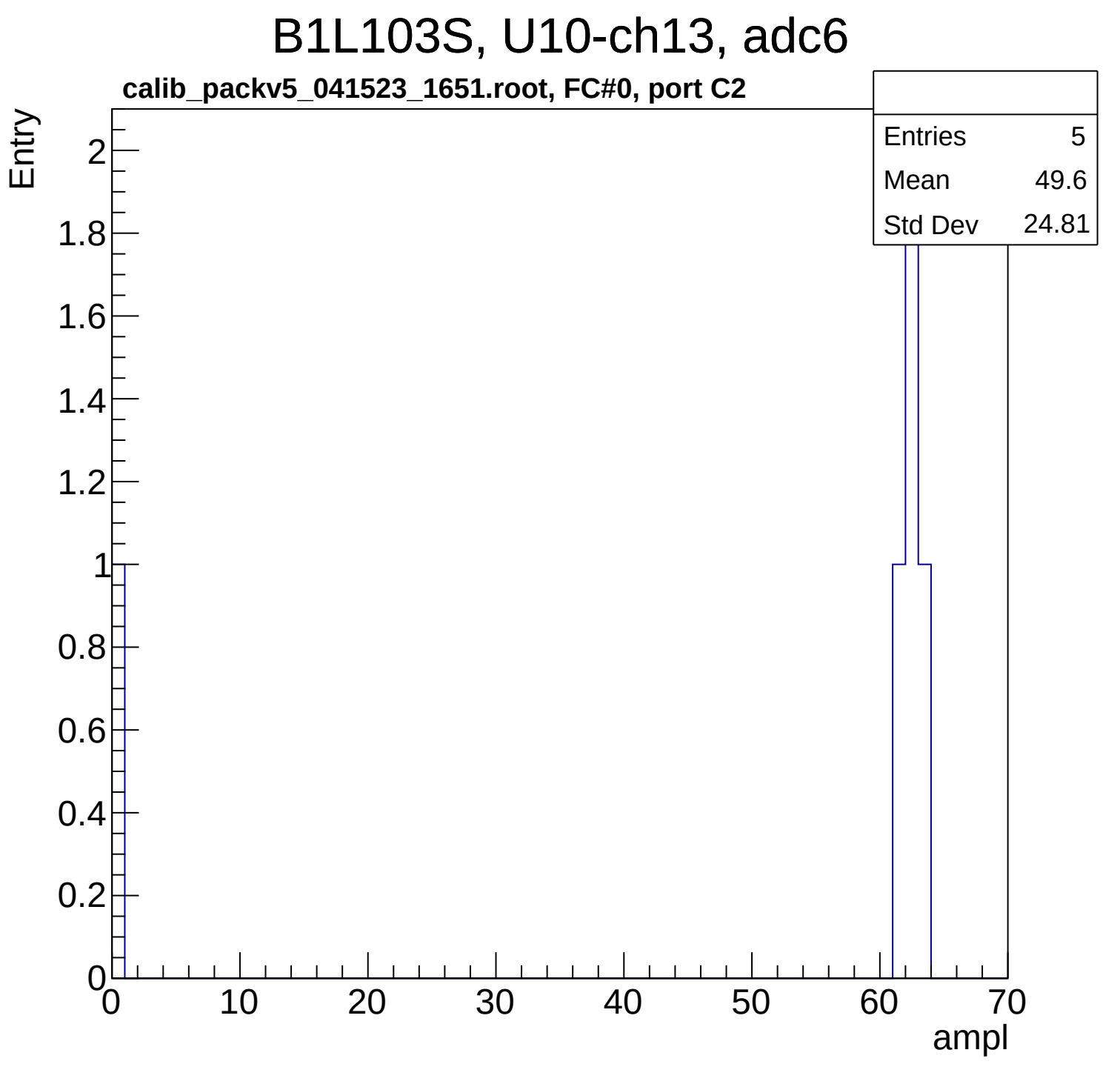

B1L103S, U10-ch13, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 104
Mean 34.71
Std Dev 7.119
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

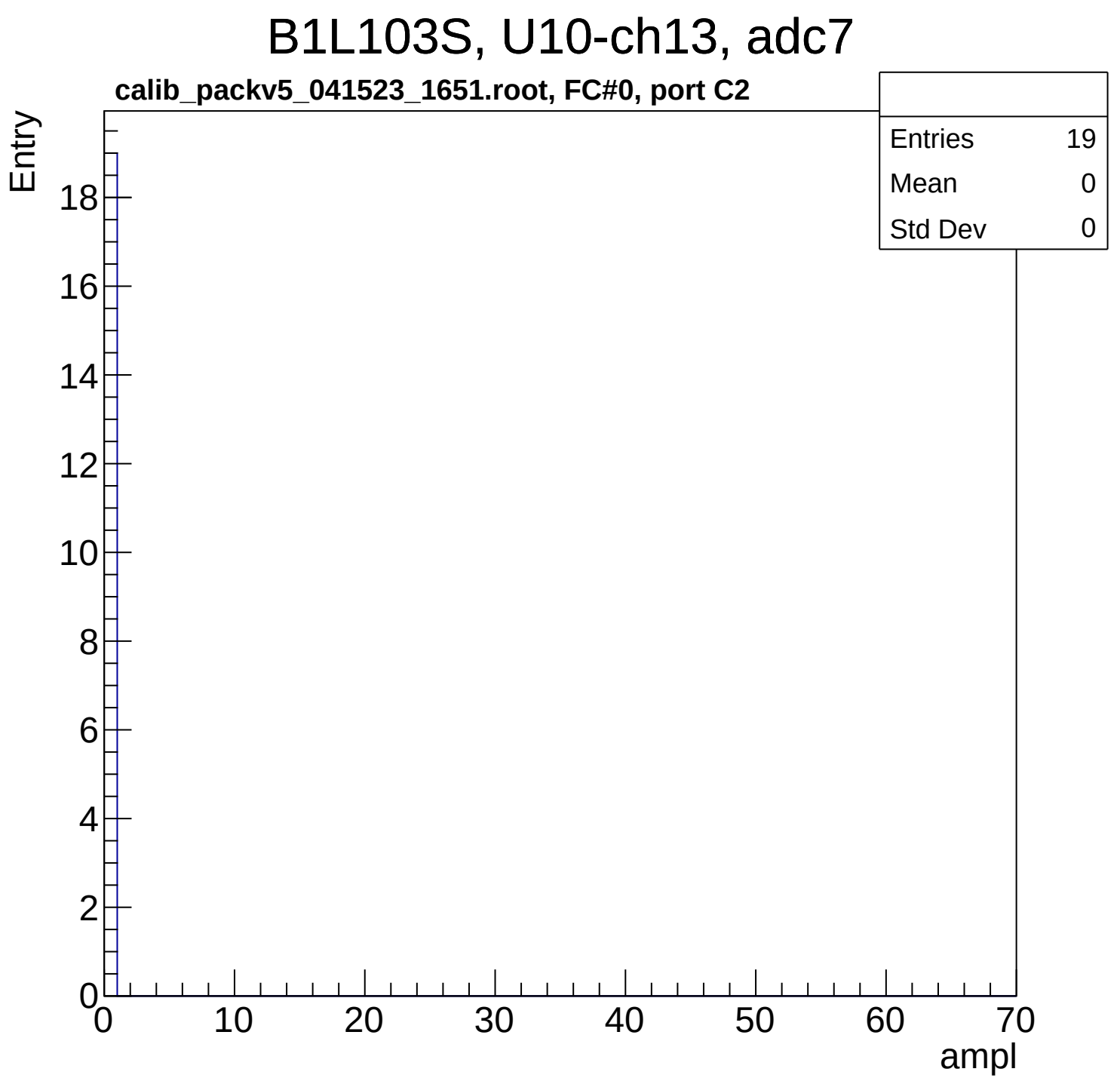

B1L103S, U10-ch13, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 36.28
Std Dev 16.62
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

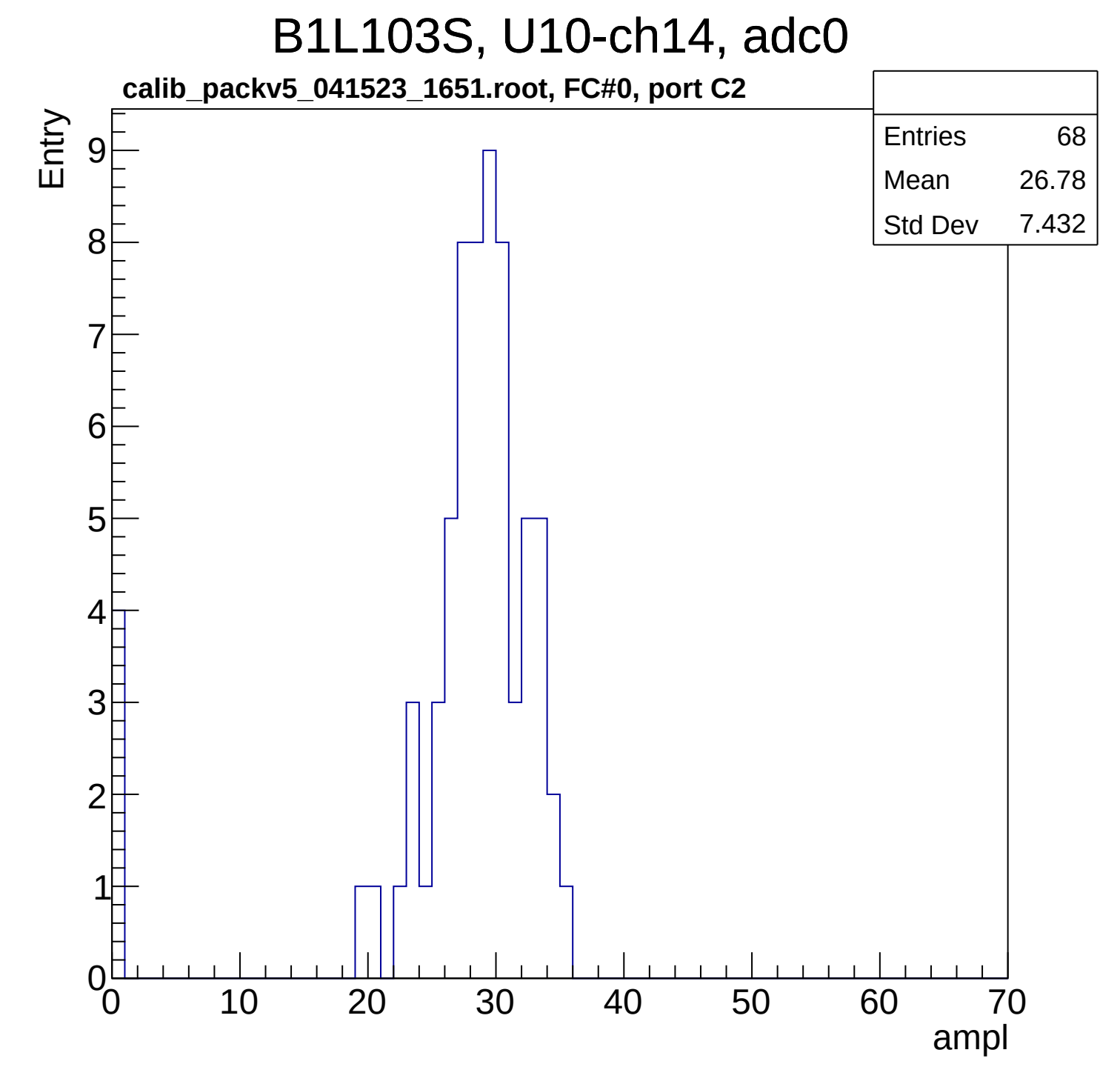

B1L103S, U10-ch13, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 49.88
Std Dev 6.584
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

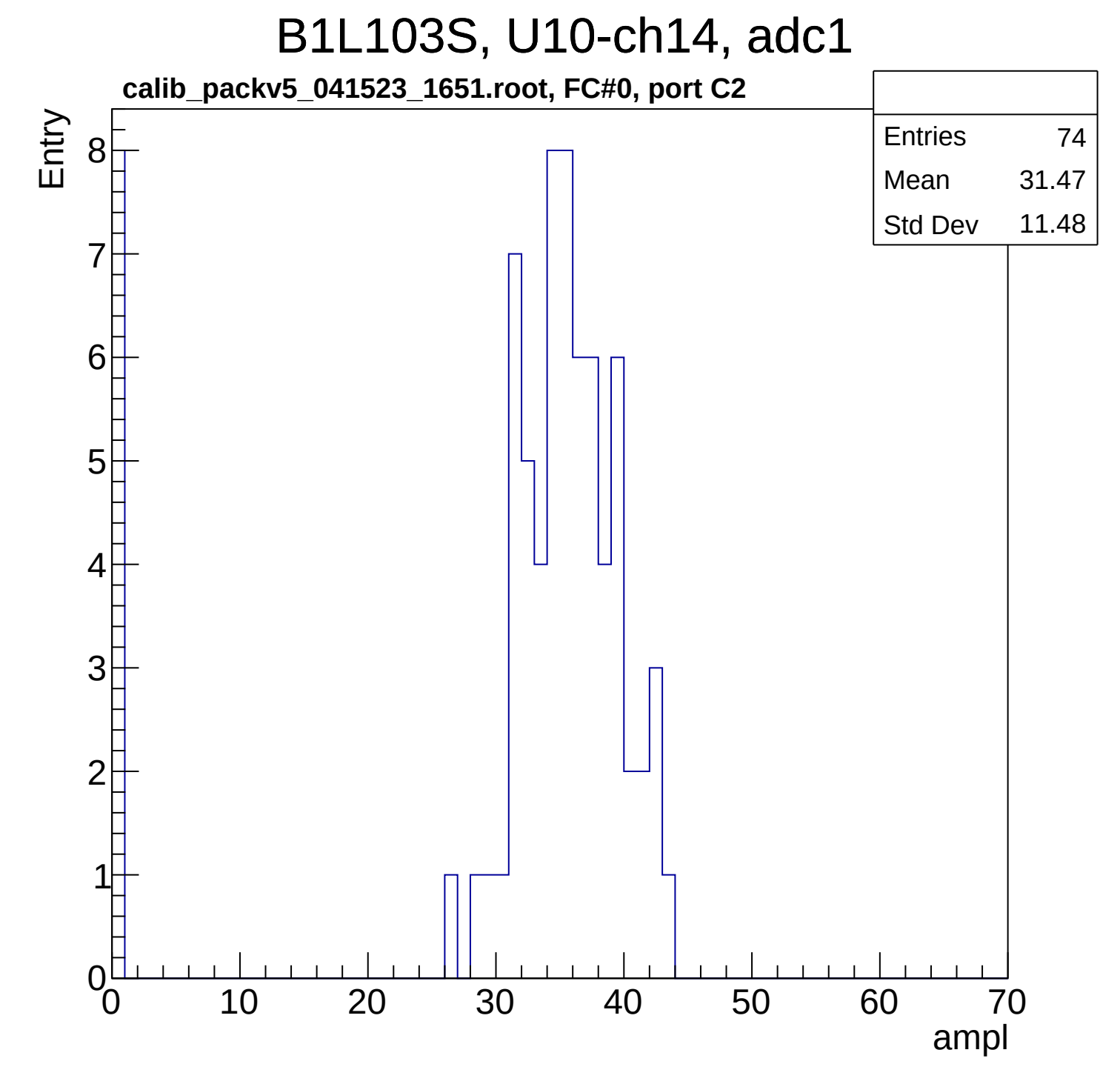

B1L103S, U10-ch13, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 56.11
Std Dev 3.419
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

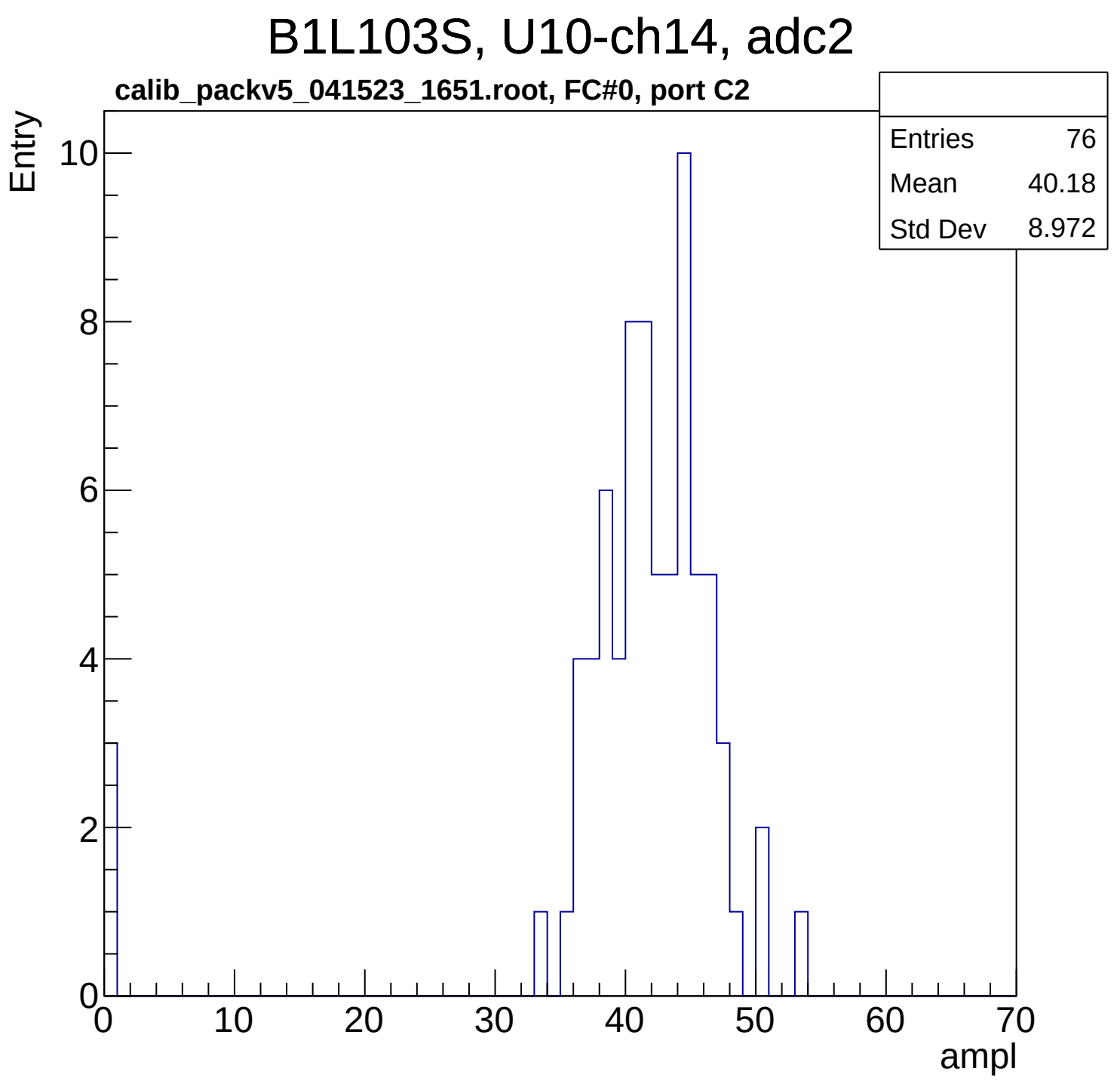

B1L103S, U10-ch13, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 60.25
Std Dev 2.207
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

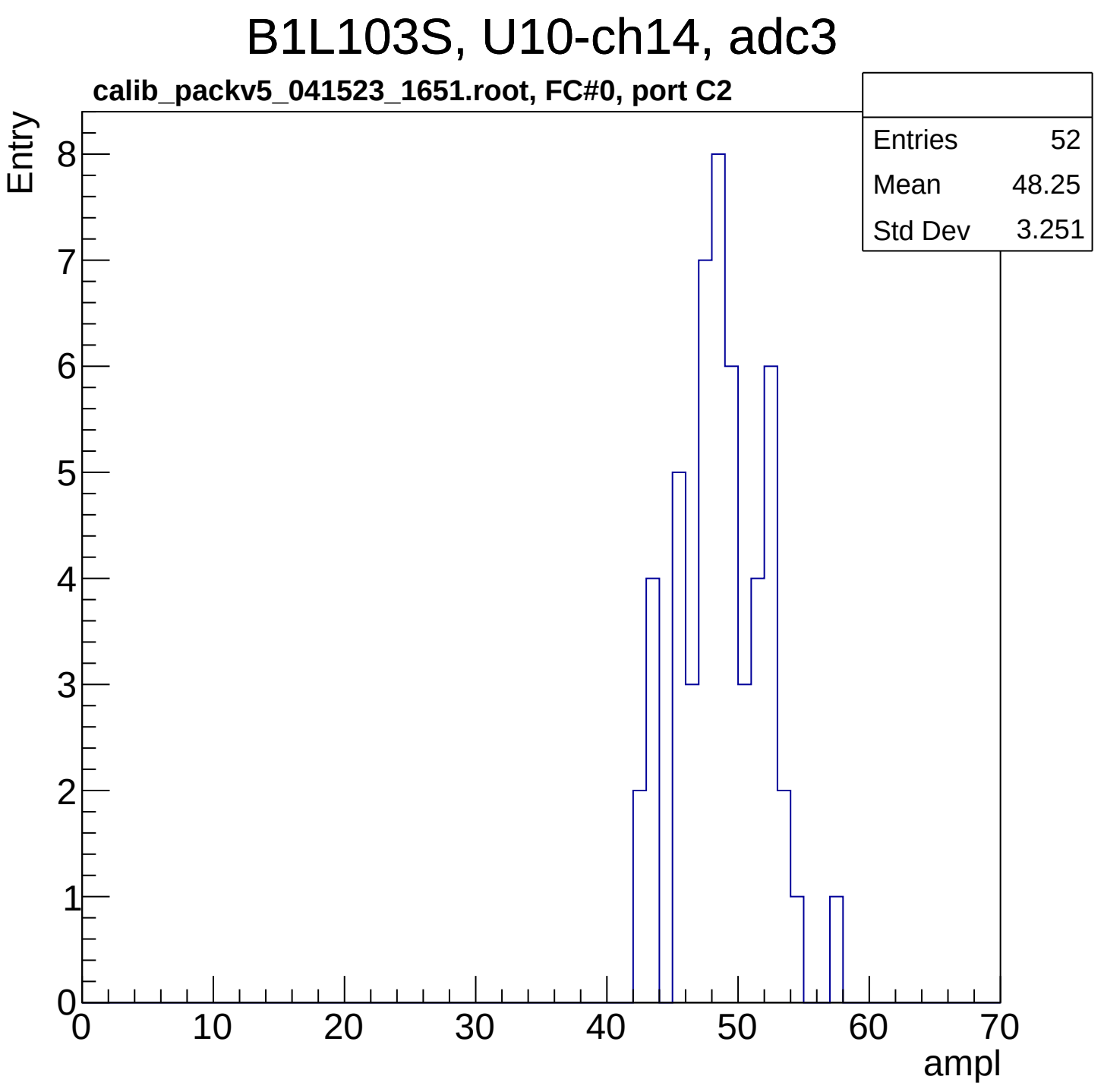

B1L103S, U10-ch13, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 5
Mean 49.6
Std Dev 24.81
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U10-ch13, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch14, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 26.78
Std Dev 7.432
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U10-ch14, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 31.47
Std Dev 11.48
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U10-ch14, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 40.18
Std Dev 8.972
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch14, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 48.25
Std Dev 3.251
Entry
ampl
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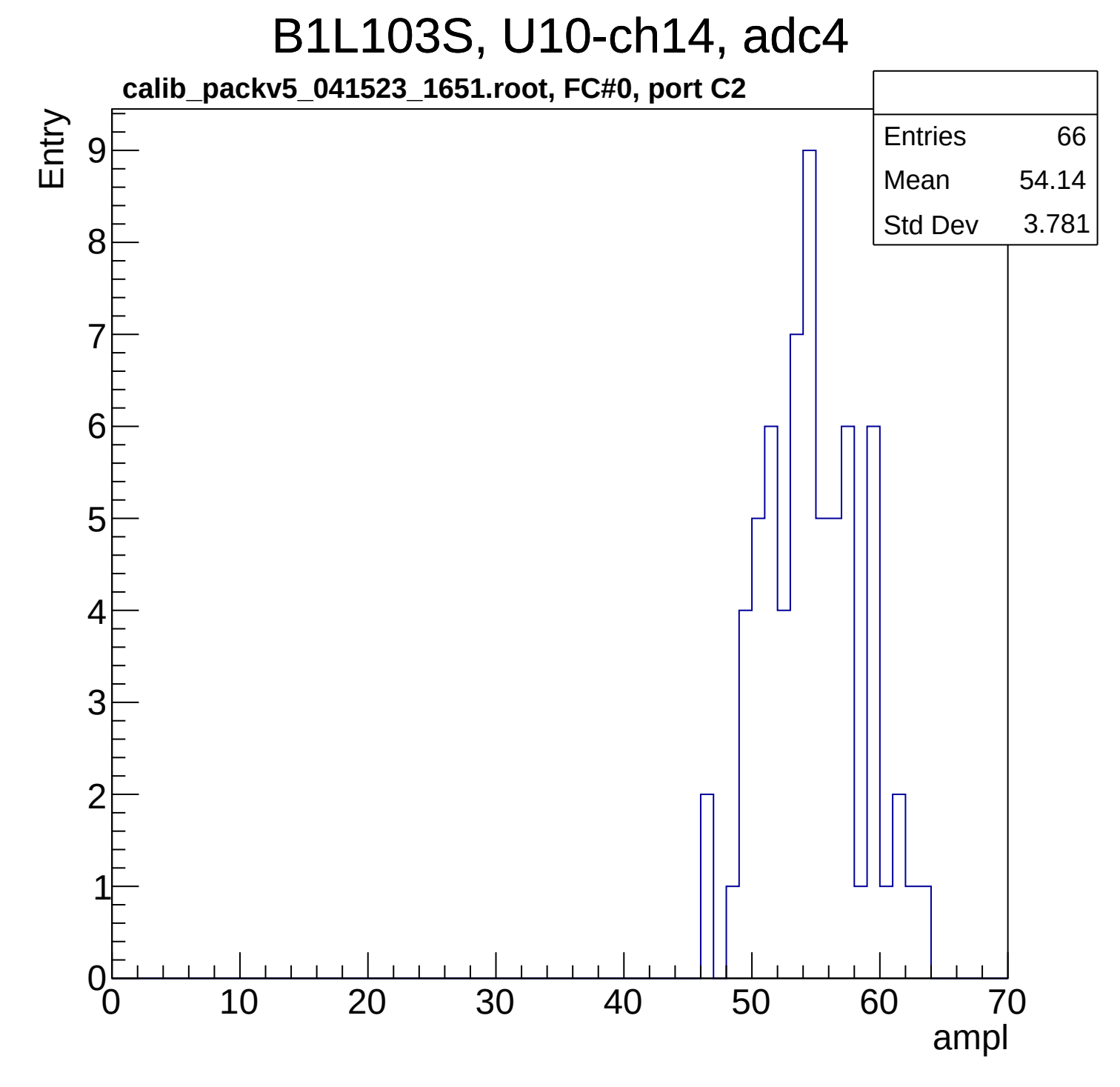
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U10-ch14, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 54.14
Std Dev 3.781
Entry
ampl
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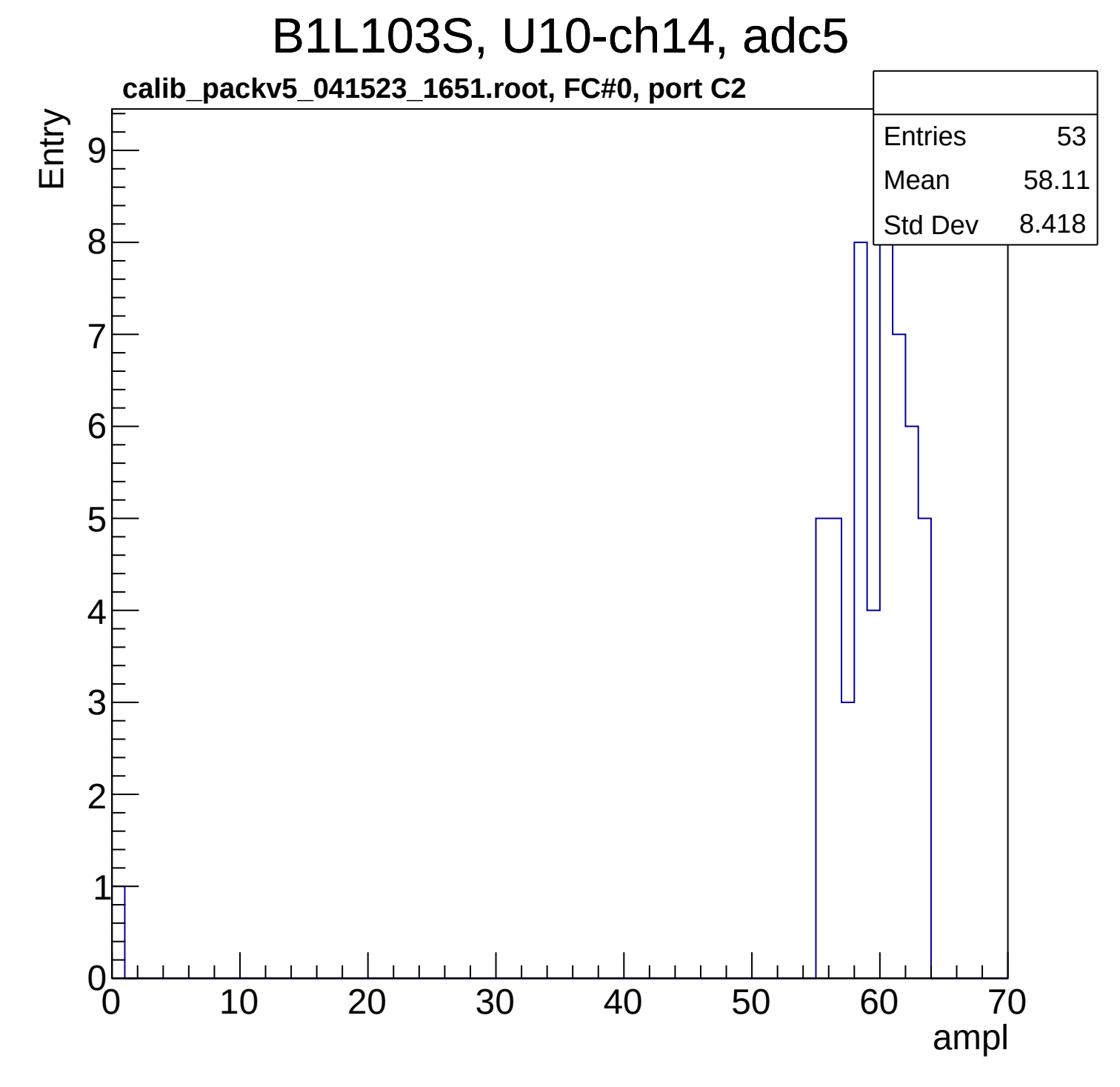
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U10-ch14, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 58.11
Std Dev 8.418
Entry
ampl
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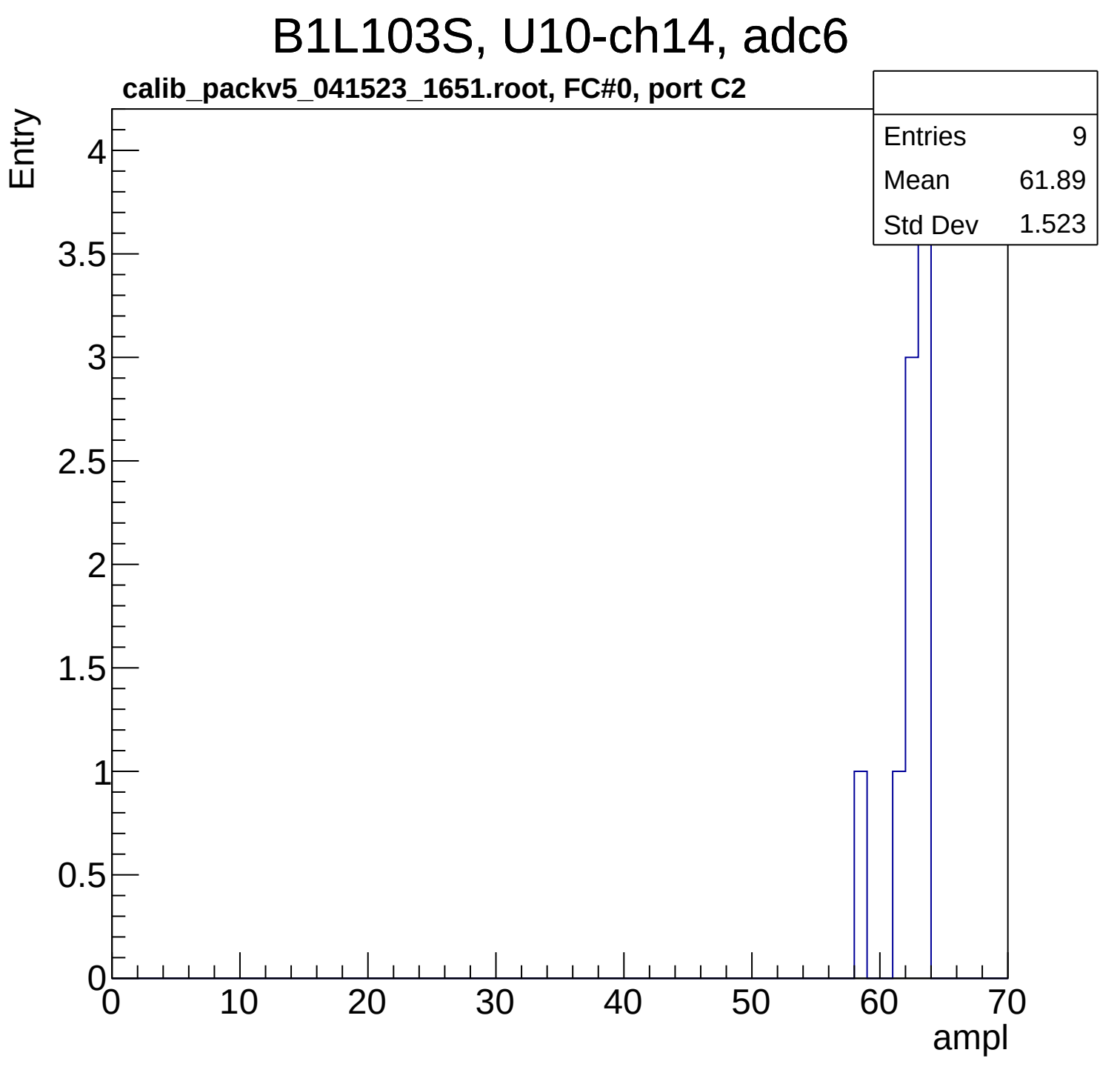
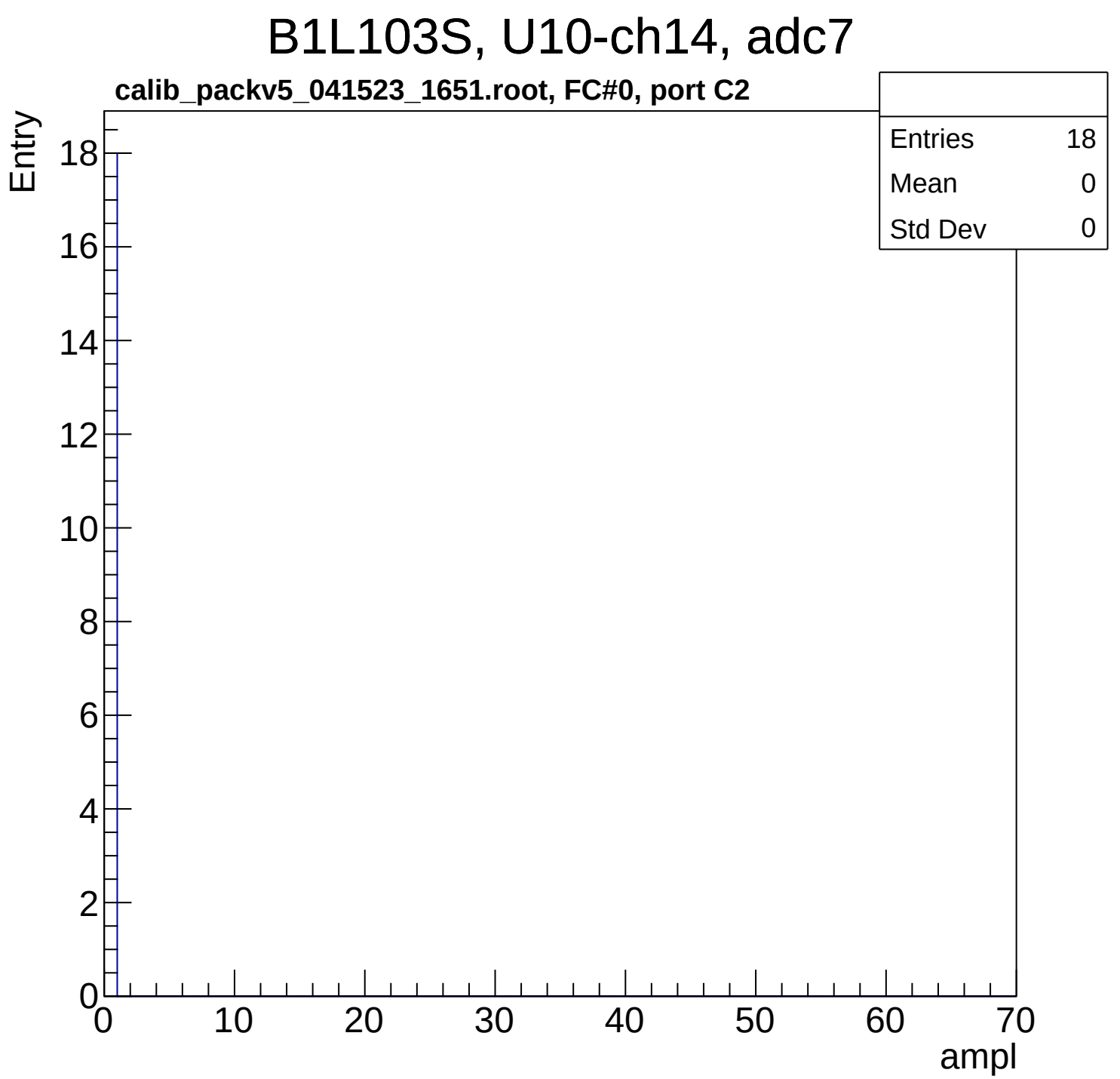
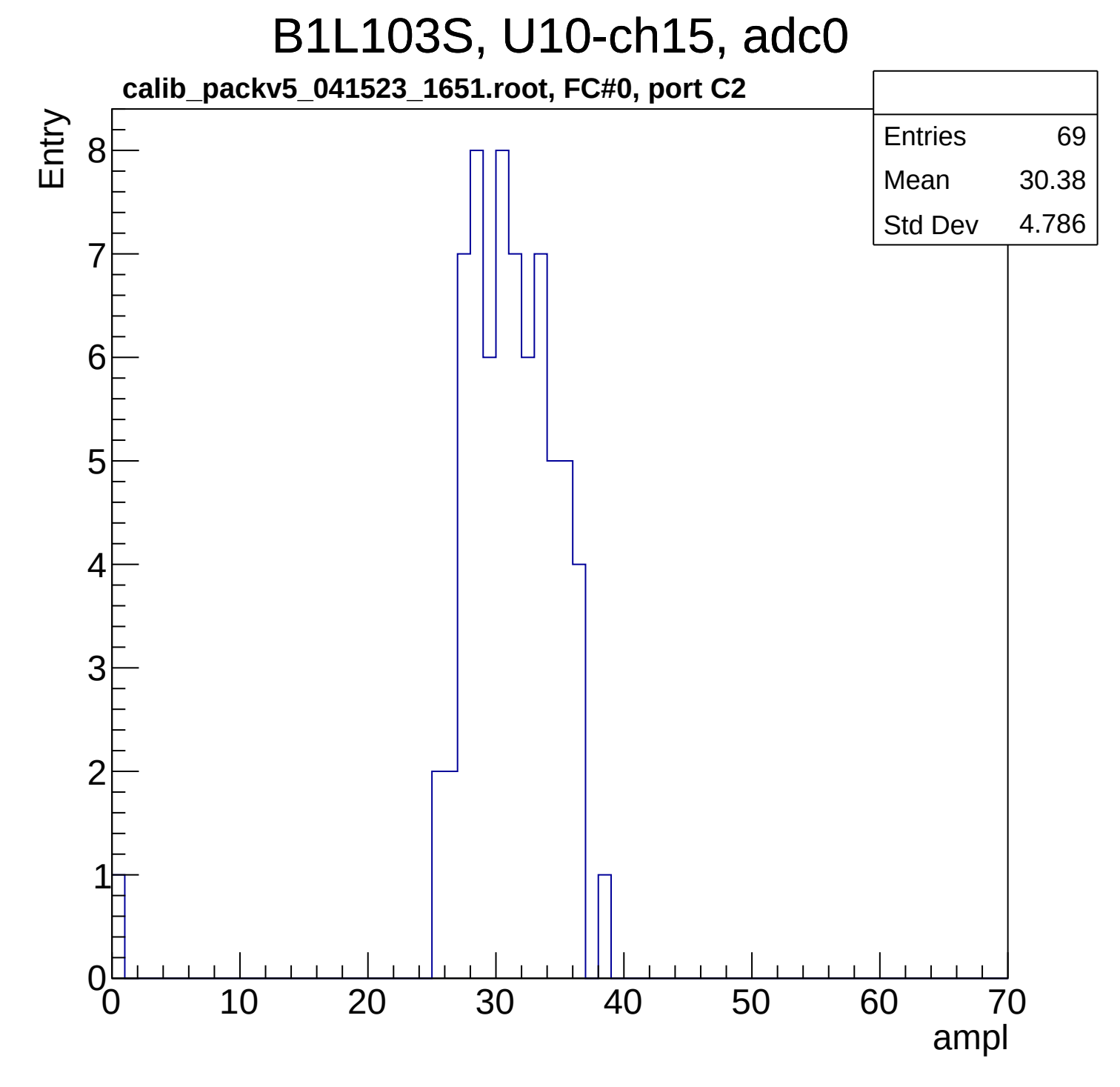
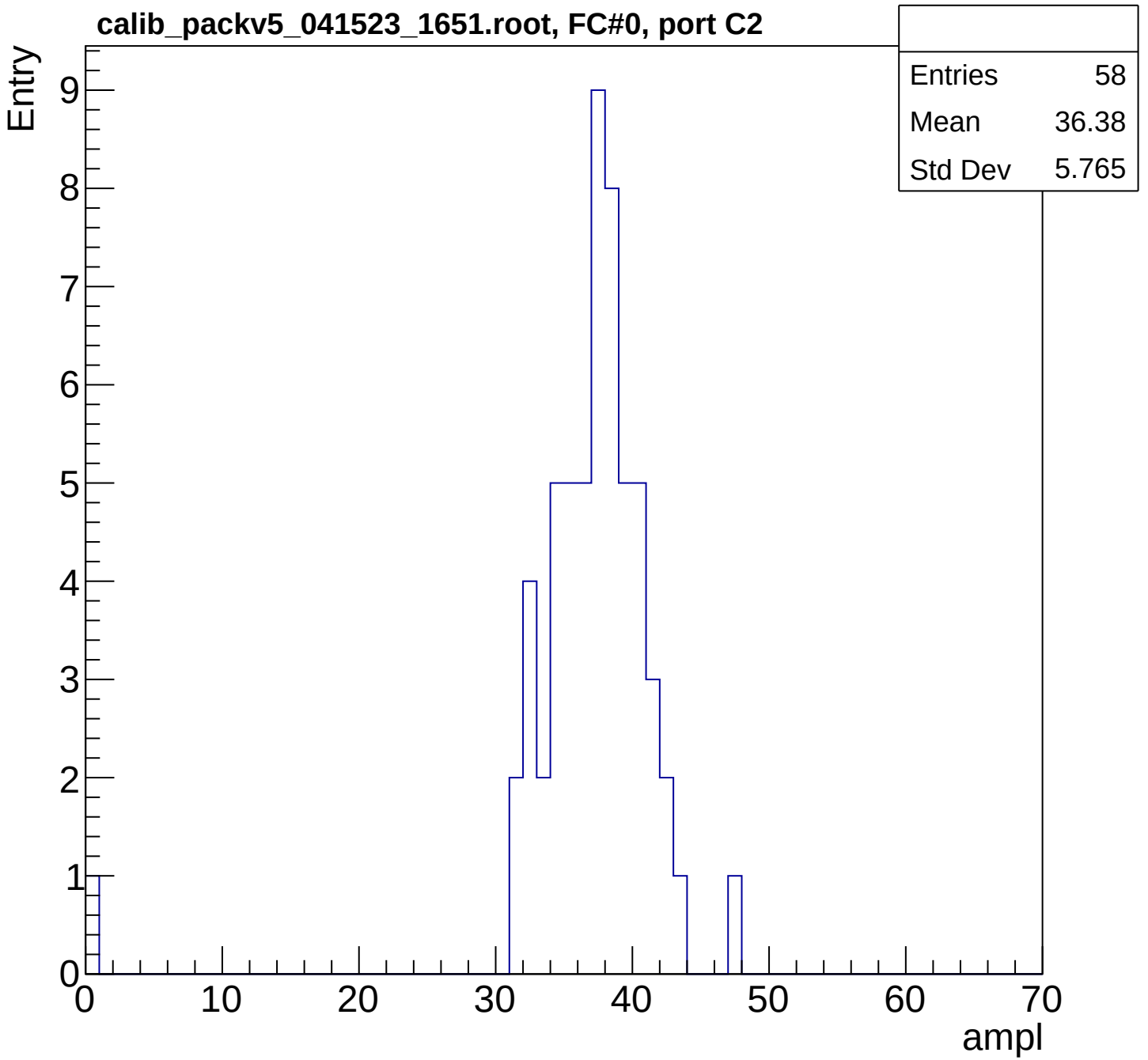
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U10-ch14, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 9
Mean 61.89
Std Dev 1.523
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U10-ch14, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch15, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 30.38
Std Dev 4.786
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U10-ch15, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 36.38
Std Dev 5.765
Entry
ampl
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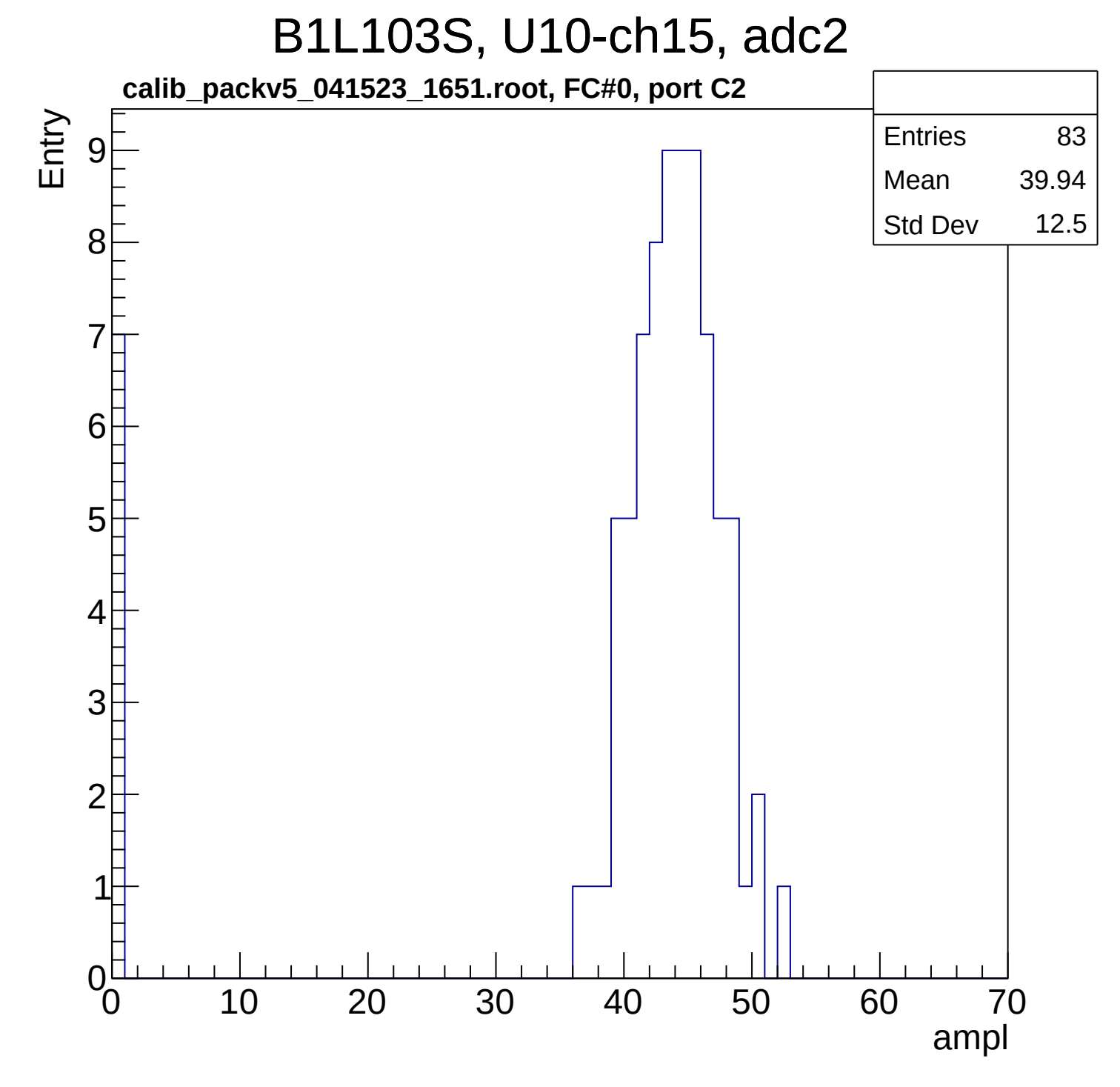
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U10-ch15, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 39.94
Std Dev 12.5
Entry
ampl
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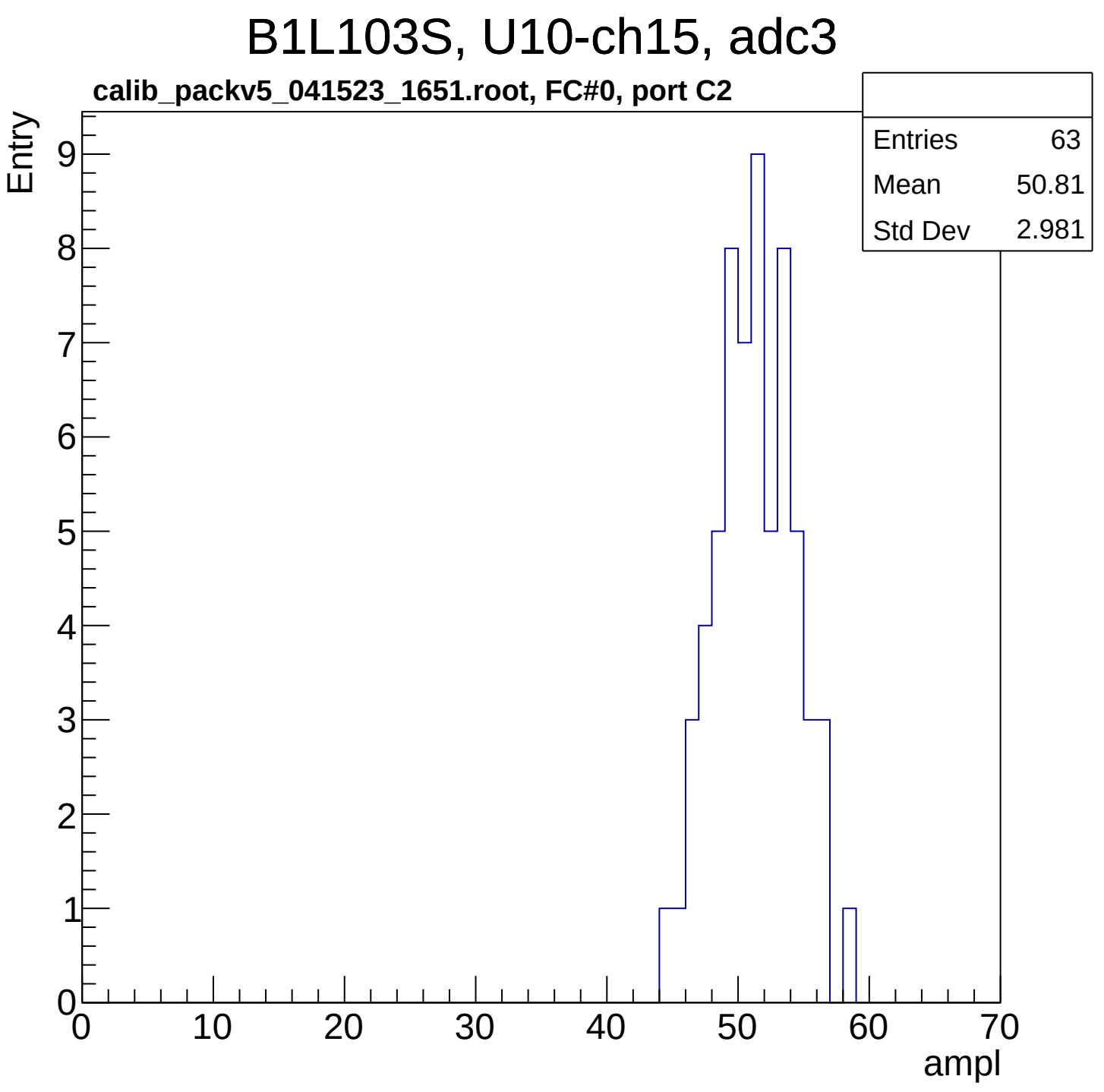
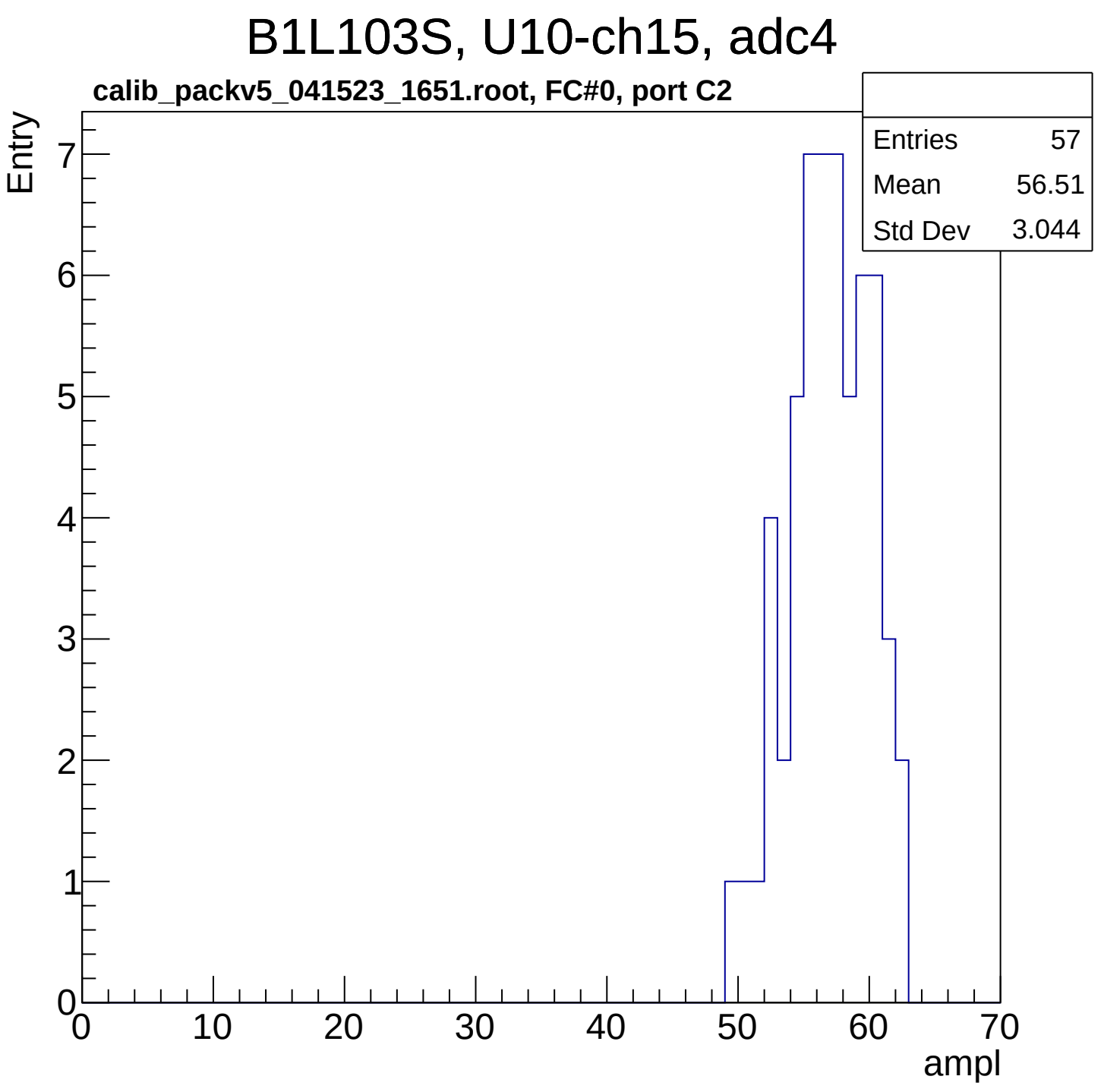
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U10-ch15, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 50.81
Std Dev 2.981
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U10-ch15, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 56.51
Std Dev 3.044
Entry
ampl
0
1
2
3
4
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6
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0
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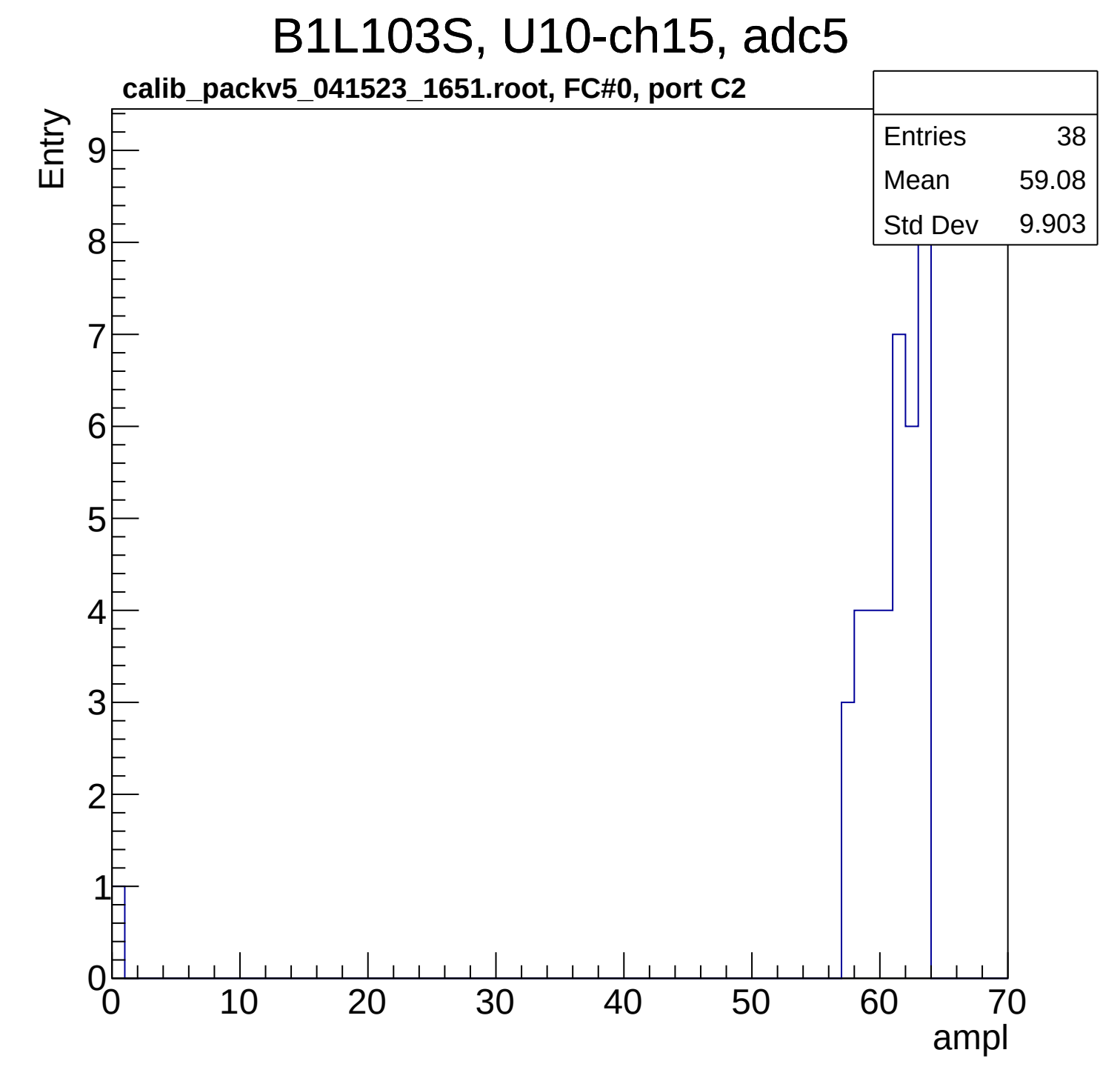
B1L103S, U10-ch15, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 38
Mean 59.08
Std Dev 9.903
Entry
ampl
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3
4
5
6
7
8
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0
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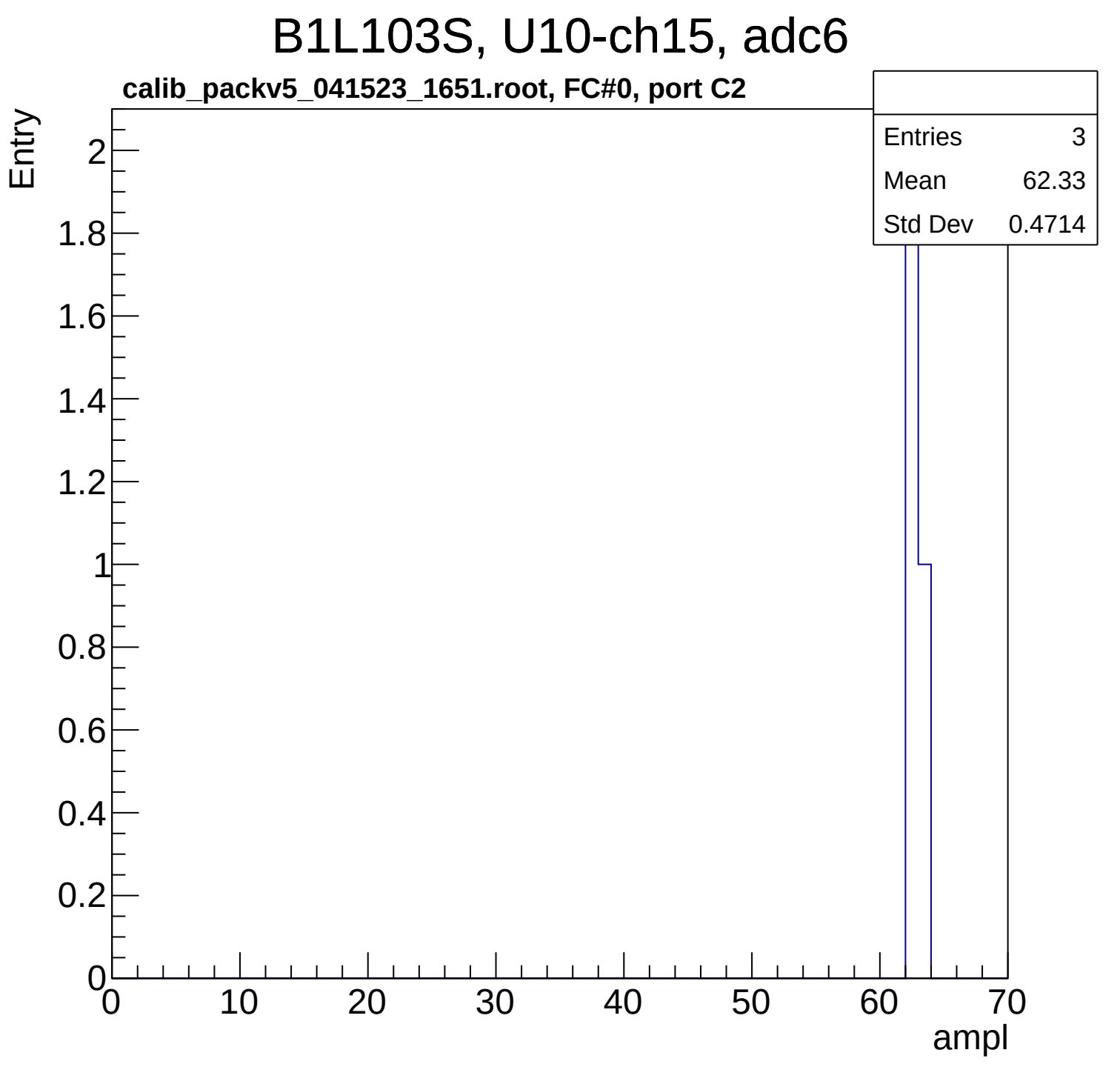
B1L103S, U10-ch15, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 3
Mean 62.33
Std Dev 0.4714
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
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40
50
60
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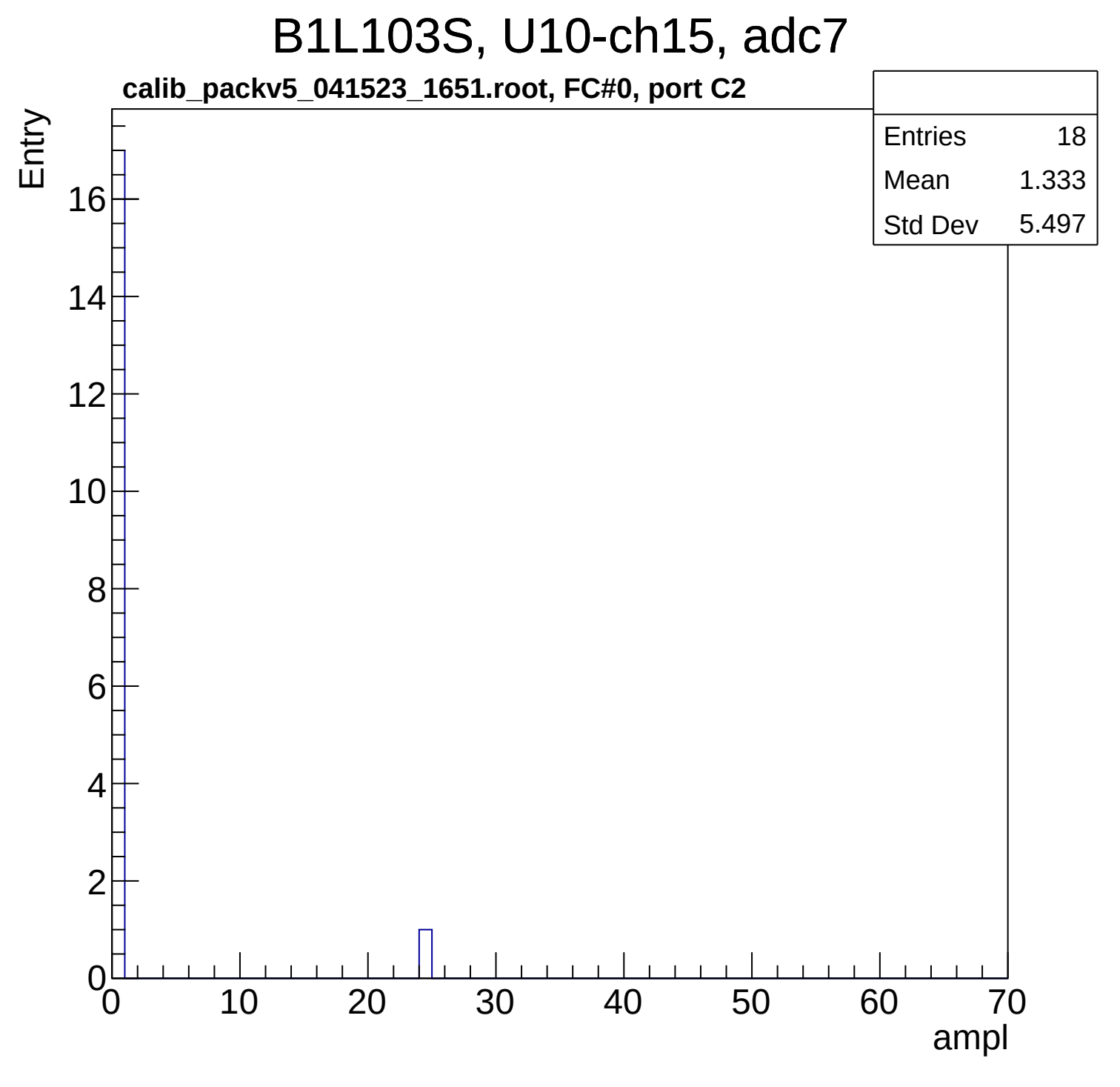
B1L103S, U10-ch15, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 1.333
Std Dev 5.497
Entry
0
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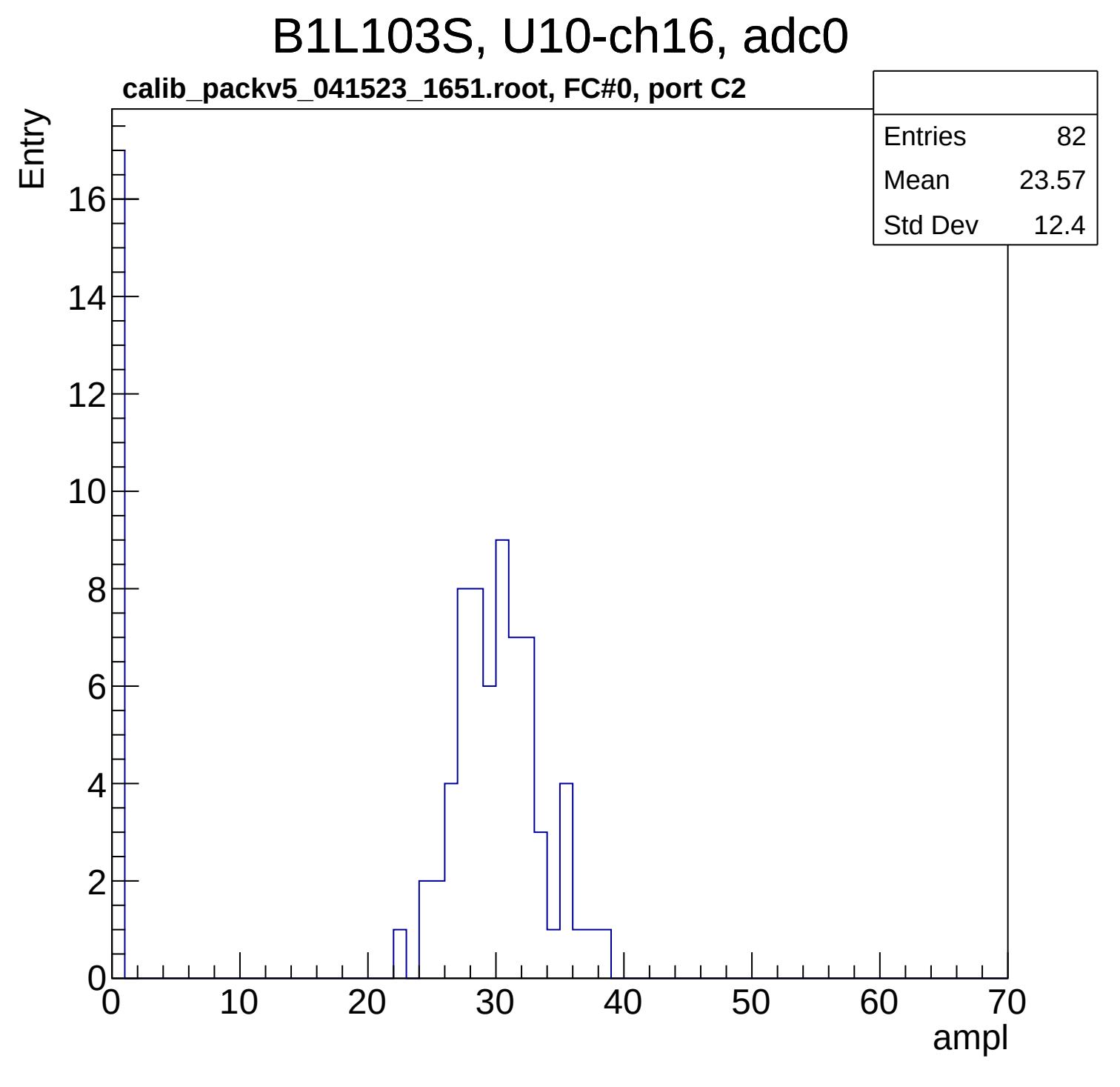
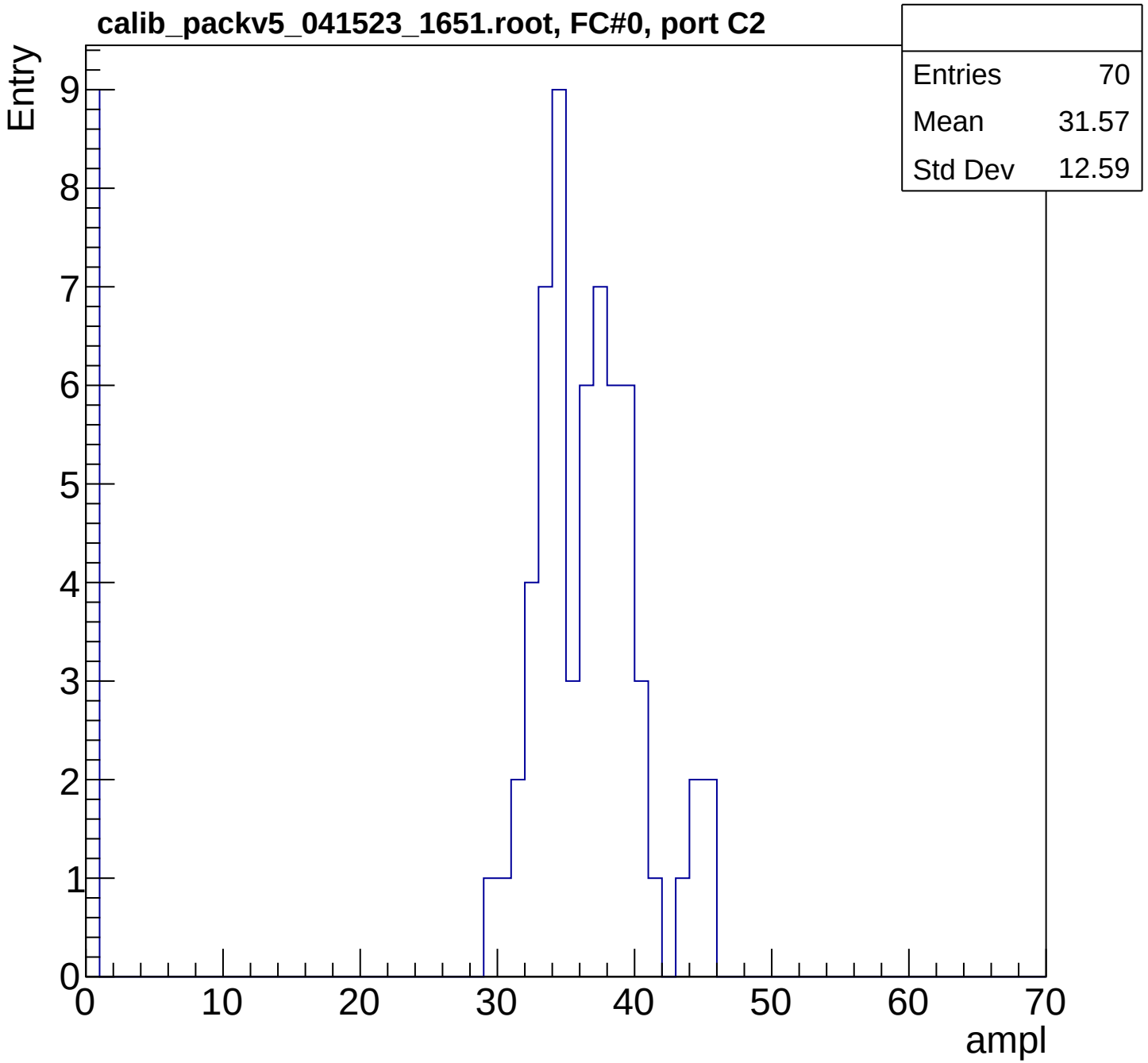
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch16, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 23.57
Std Dev 12.4
Entry
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch16, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 31.57
Std Dev 12.59
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
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30
40
50
60
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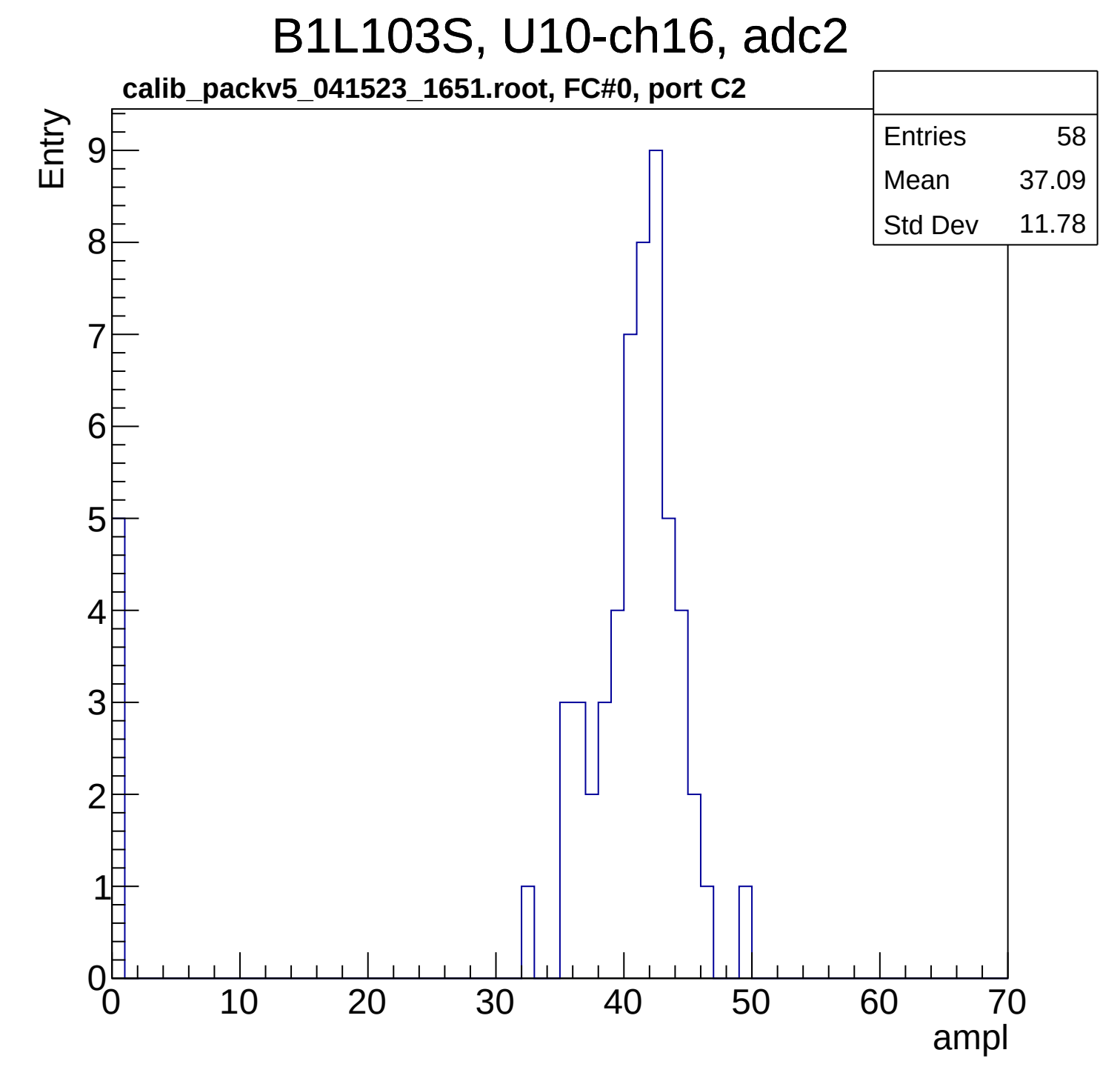
B1L103S, U10-ch16, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 37.09
Std Dev 11.78
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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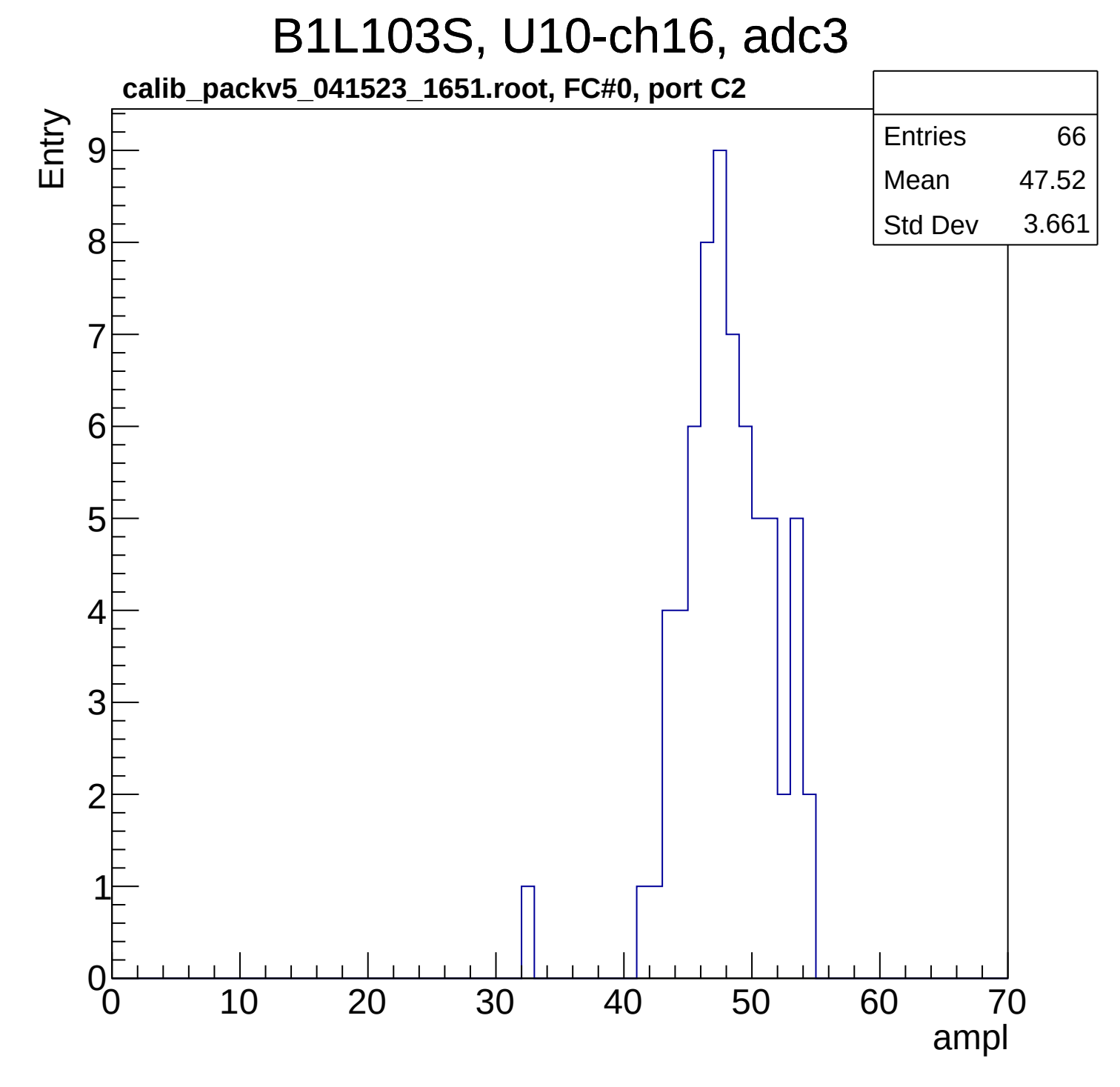
B1L103S, U10-ch16, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 47.52
Std Dev 3.661
Entry
ampl
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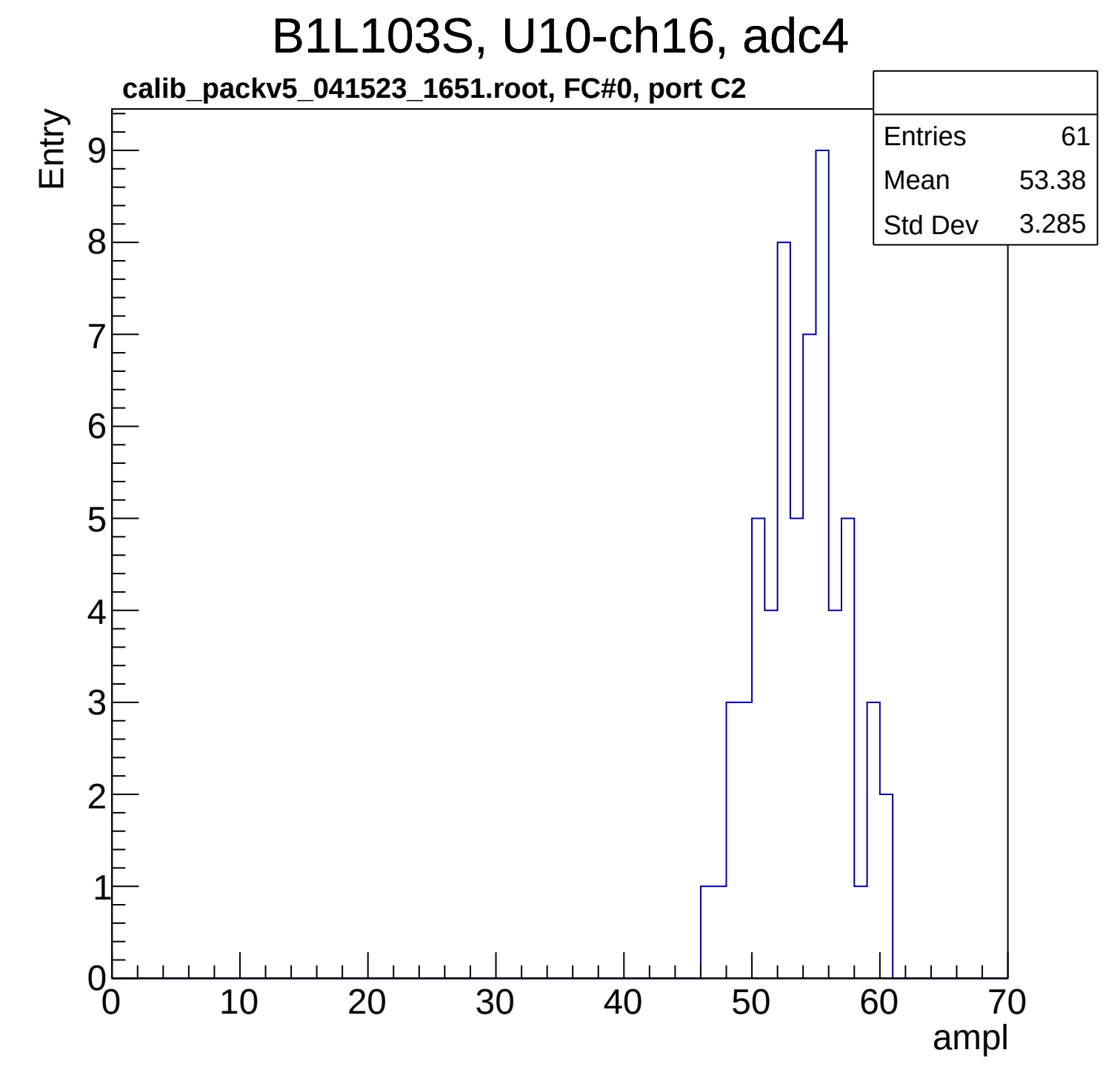
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U10-ch16, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 53.38
Std Dev 3.285
Entry
ampl
0
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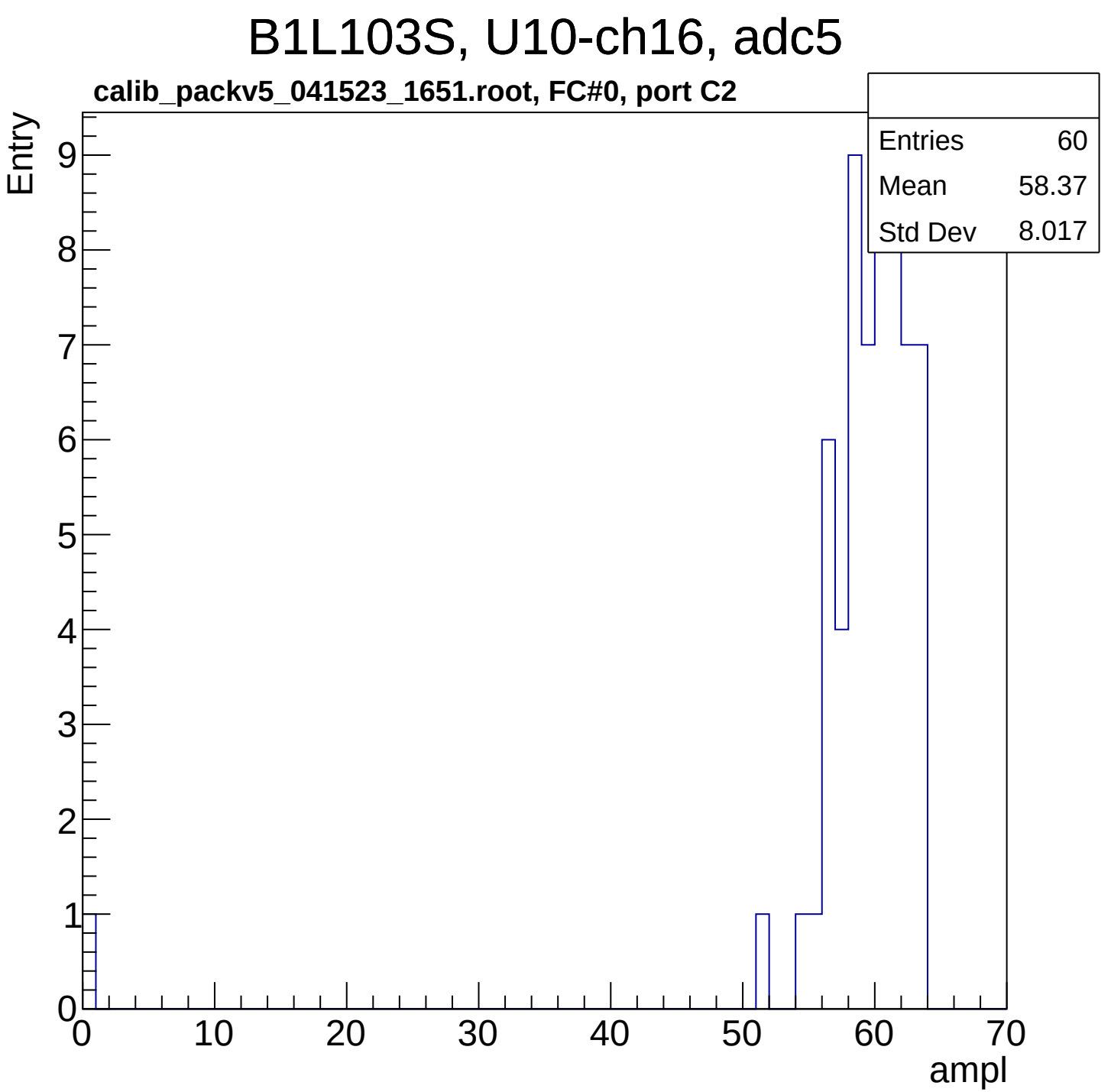
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U10-ch16, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 58.37
Std Dev 8.017
Entry
ampl
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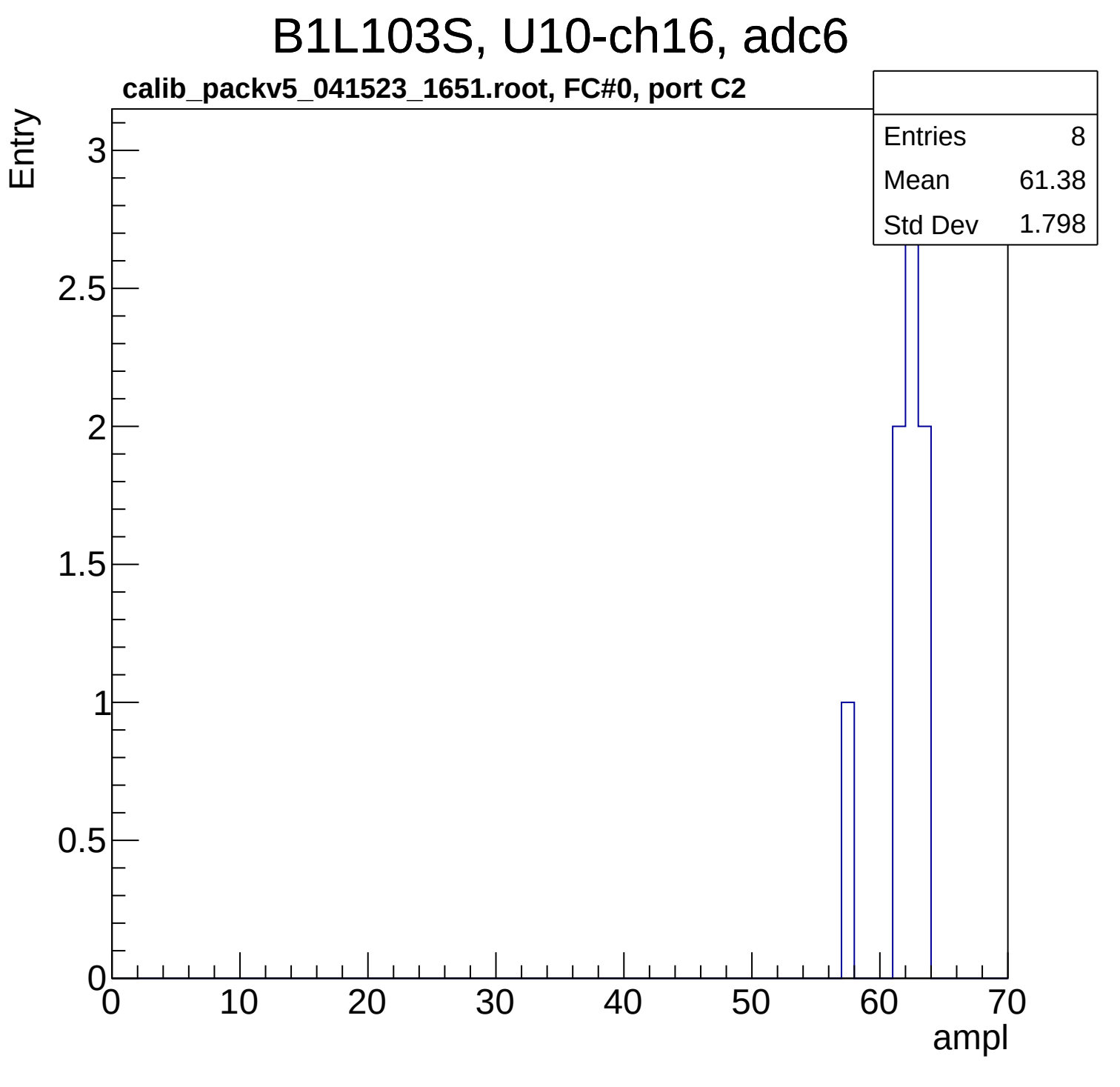
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U10-ch16, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 61.38
Std Dev 1.798
Entry
ampl
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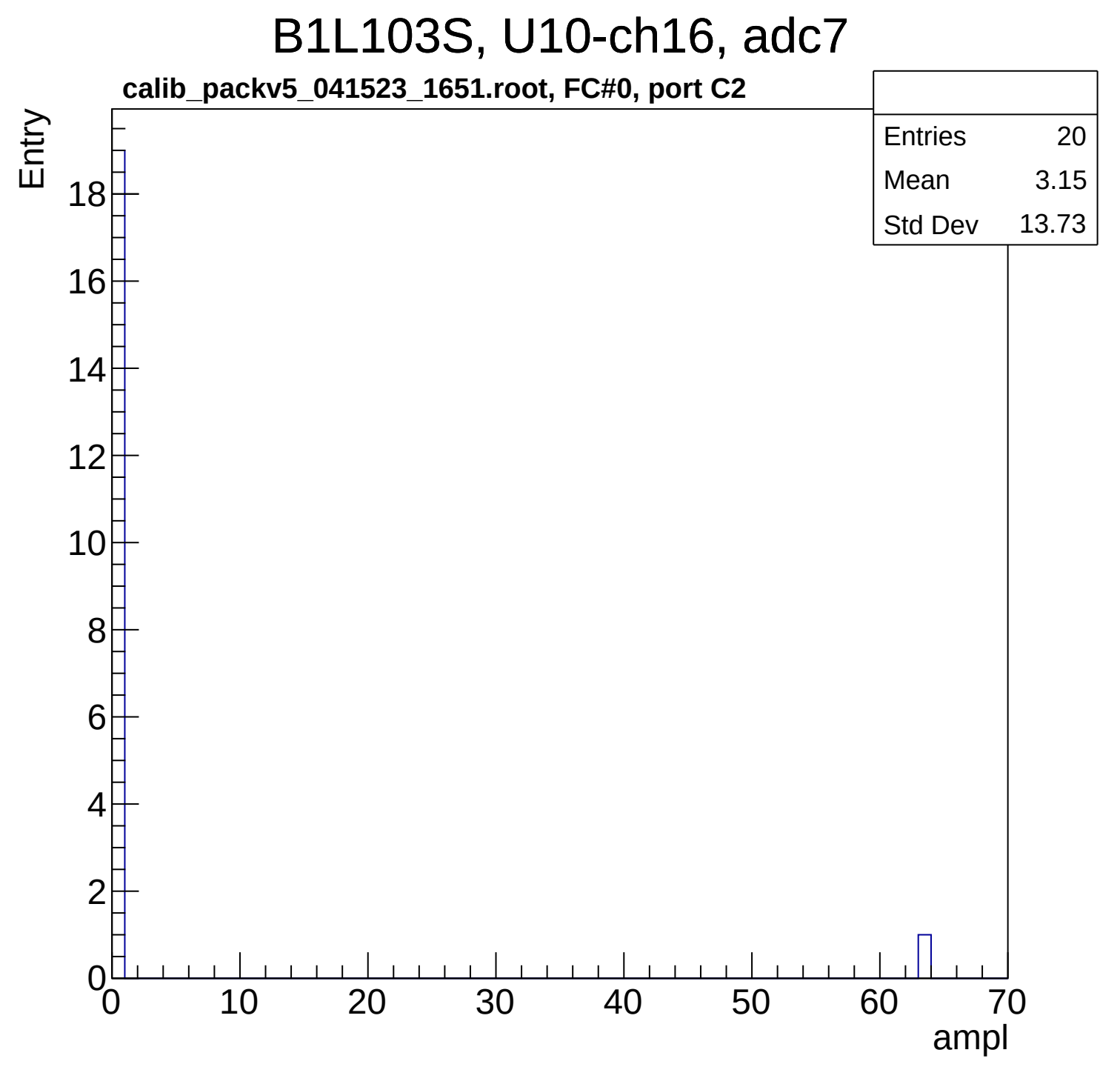
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U10-ch16, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
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2
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6
8
10
12
14
16
18
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10
20
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50
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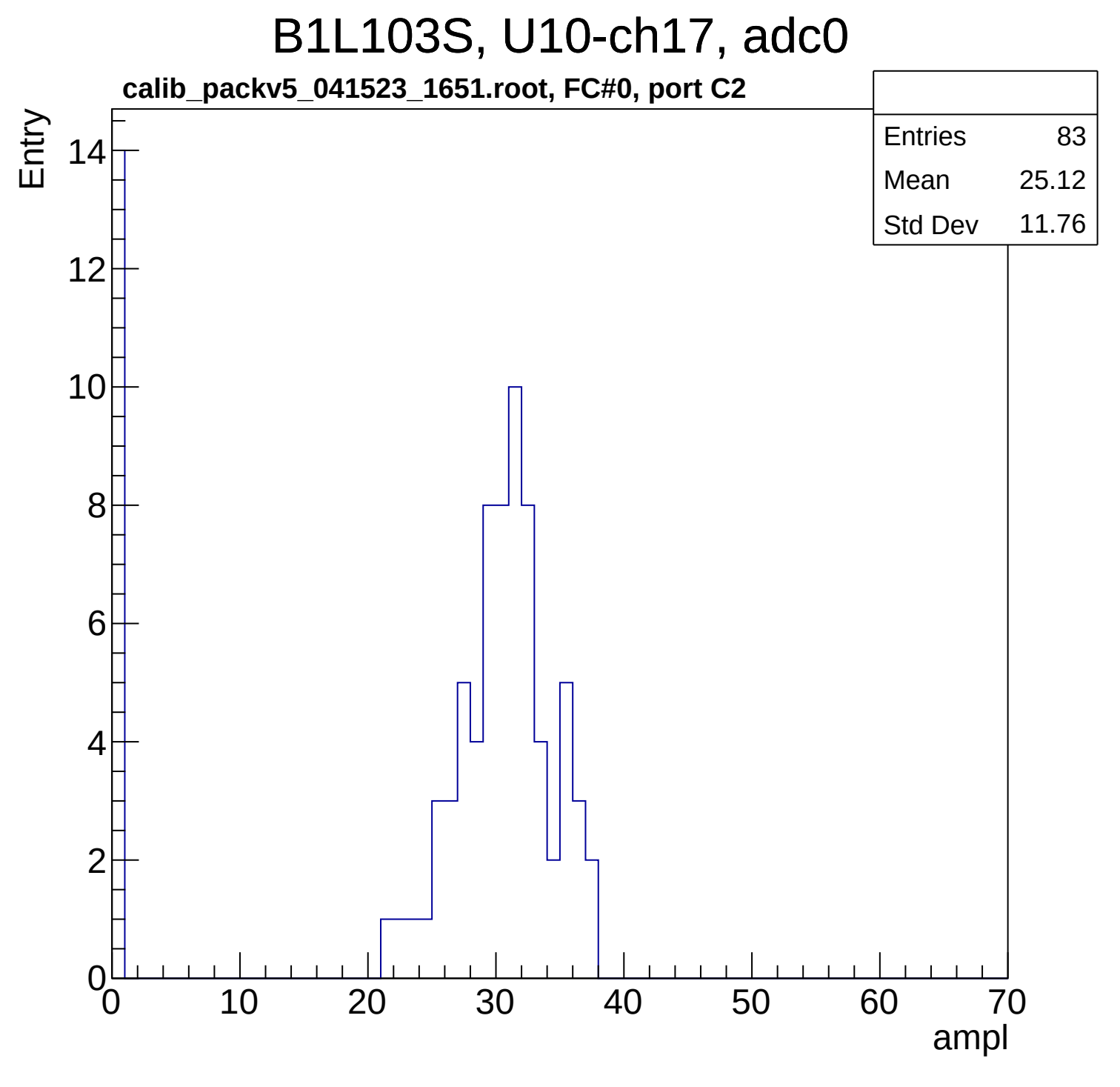
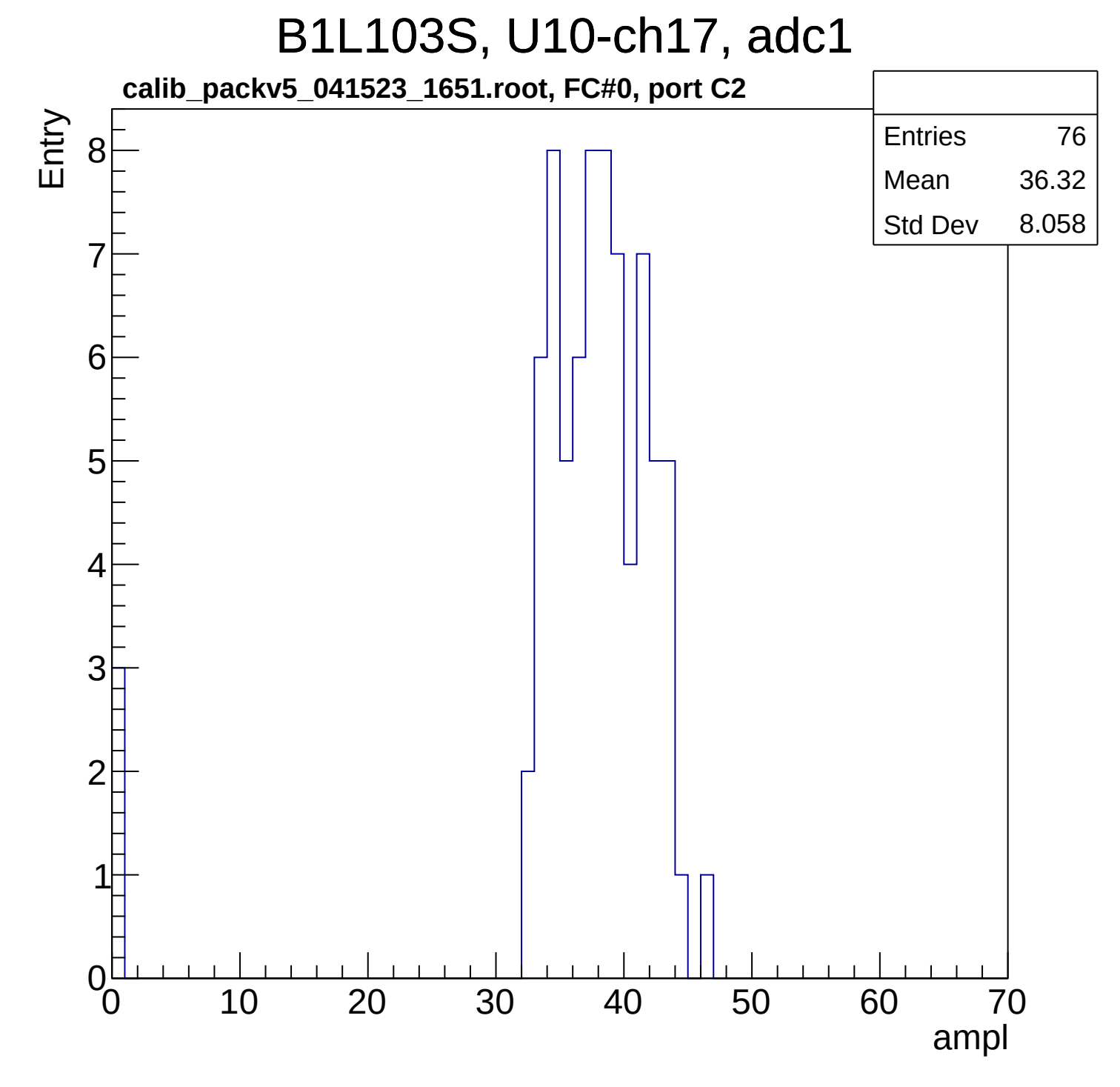
70
ampl


B1L103S, U10-ch17, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 25.12
Std Dev 11.76
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L103S, U10-ch17, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 36.32
Std Dev 8.058
Entry
ampl
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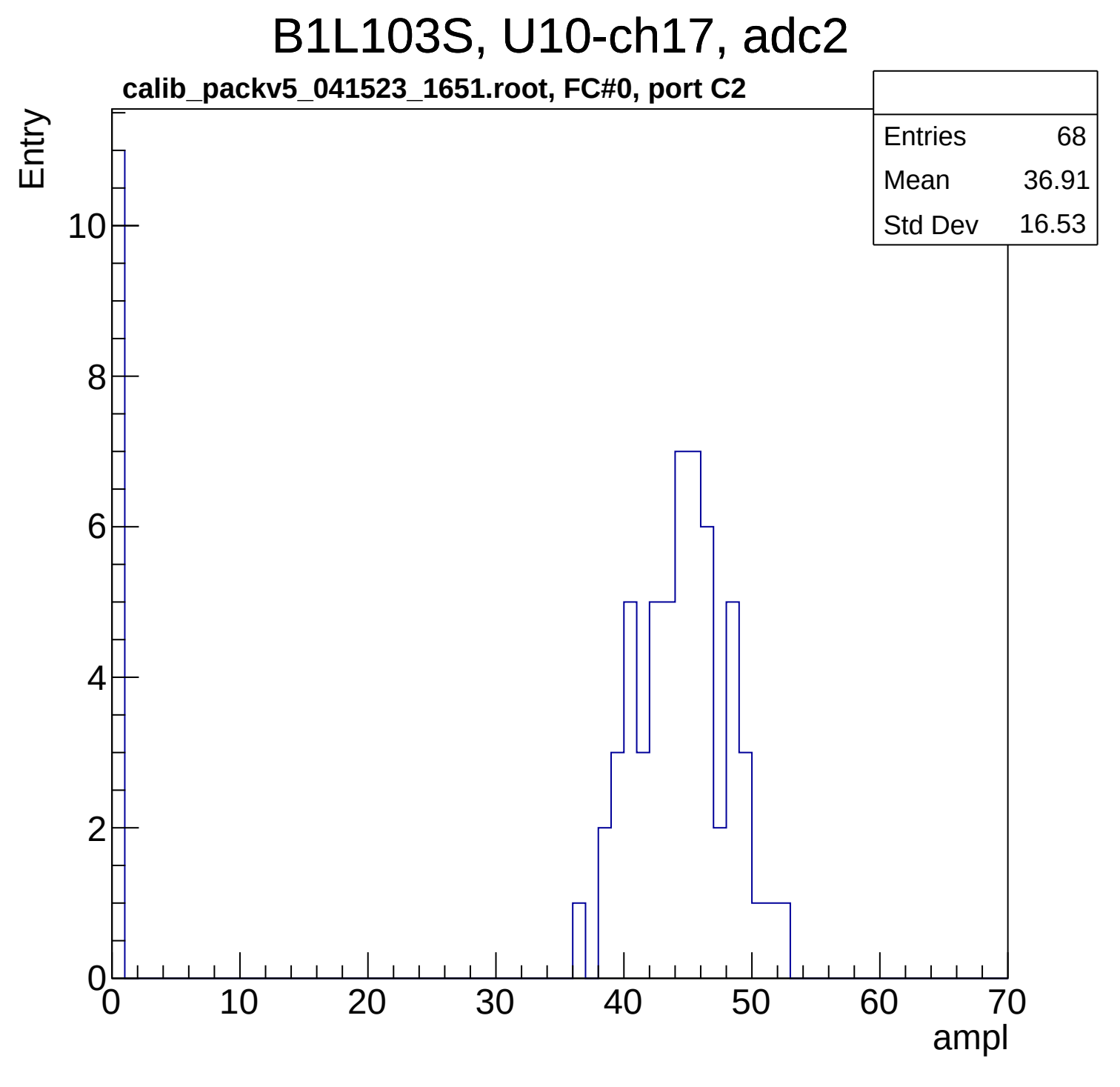
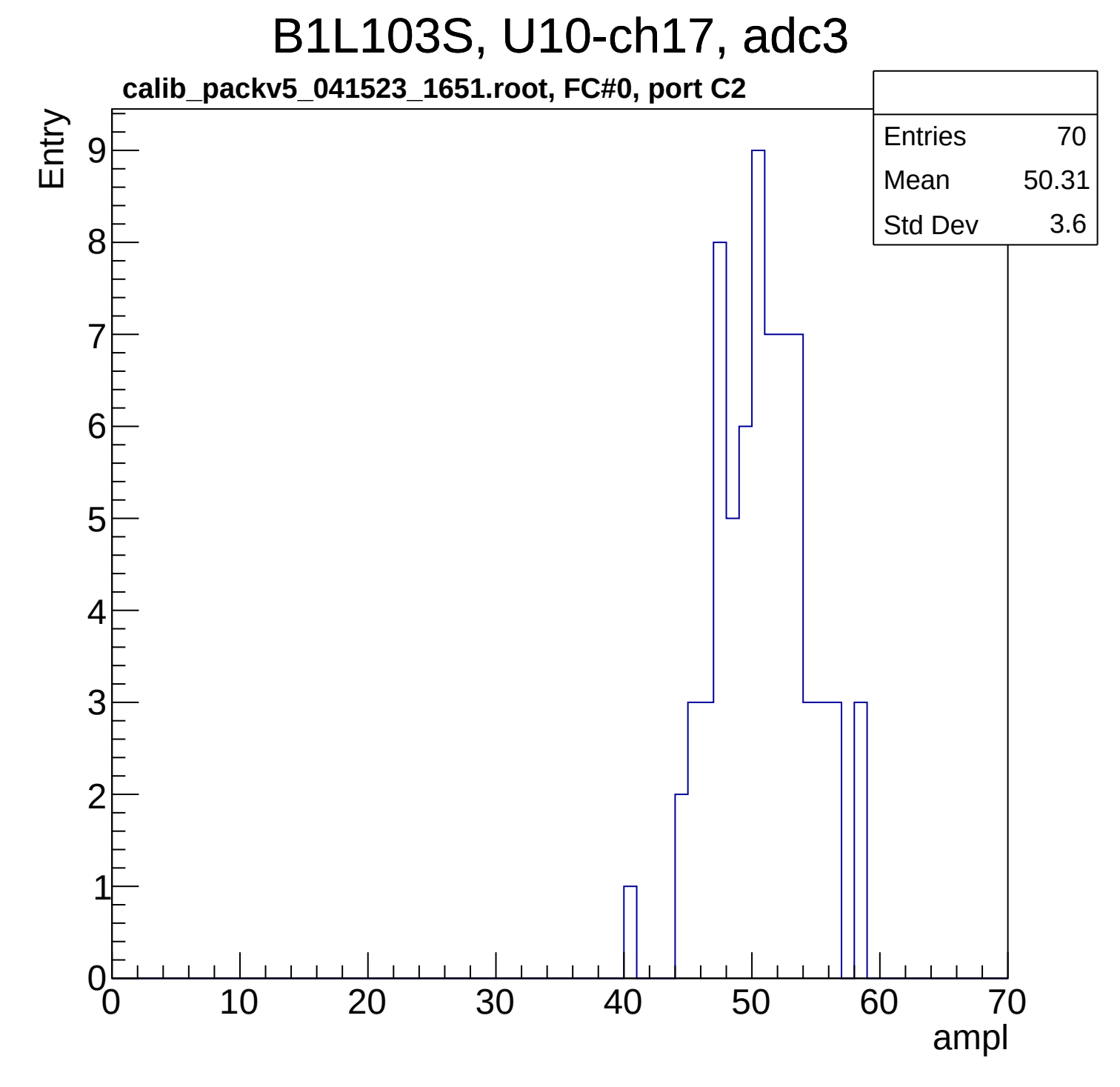
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U10-ch17, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 36.91
Std Dev 16.53
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch17, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 50.31
Std Dev 3.6
Entry
ampl
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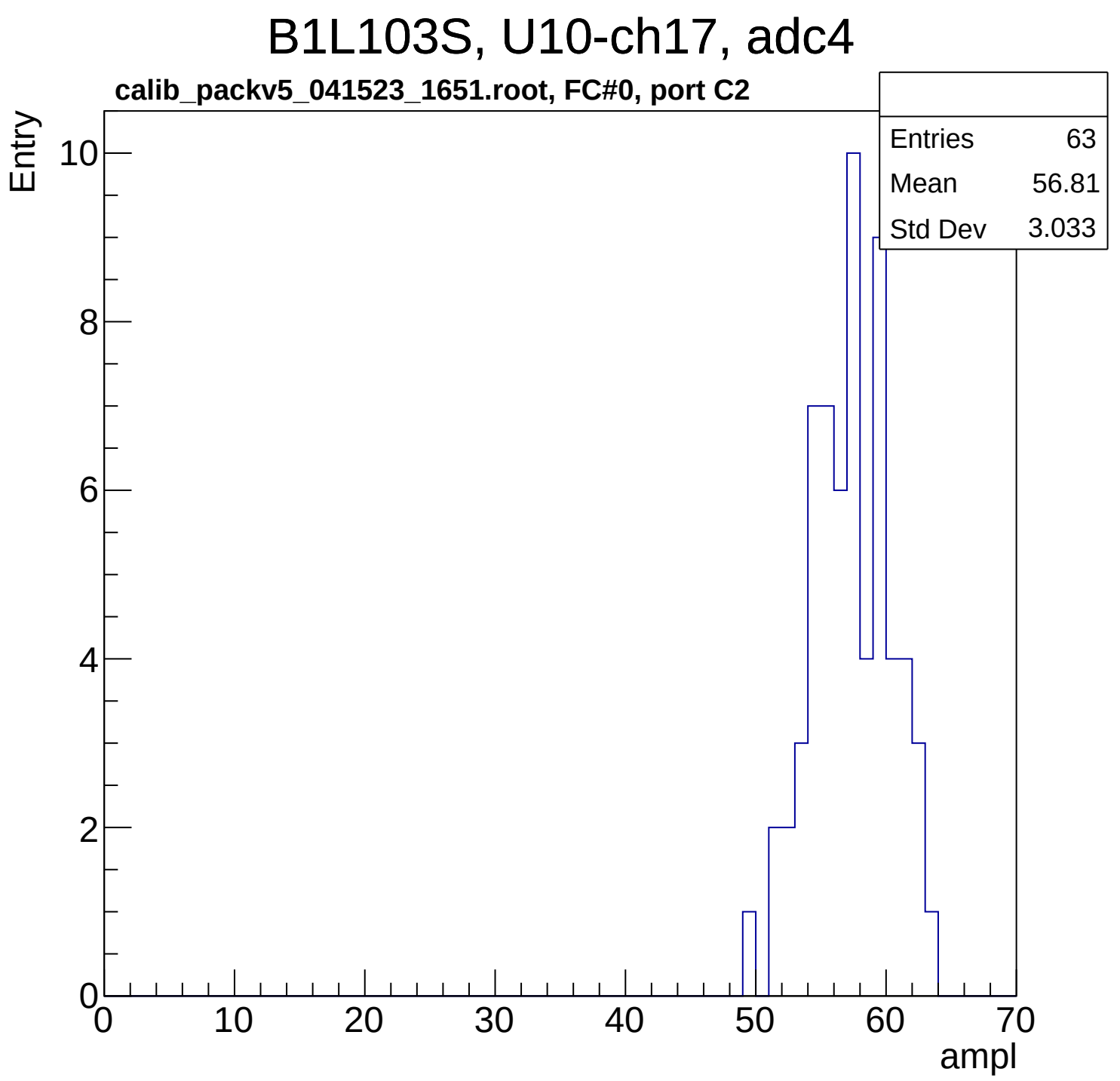
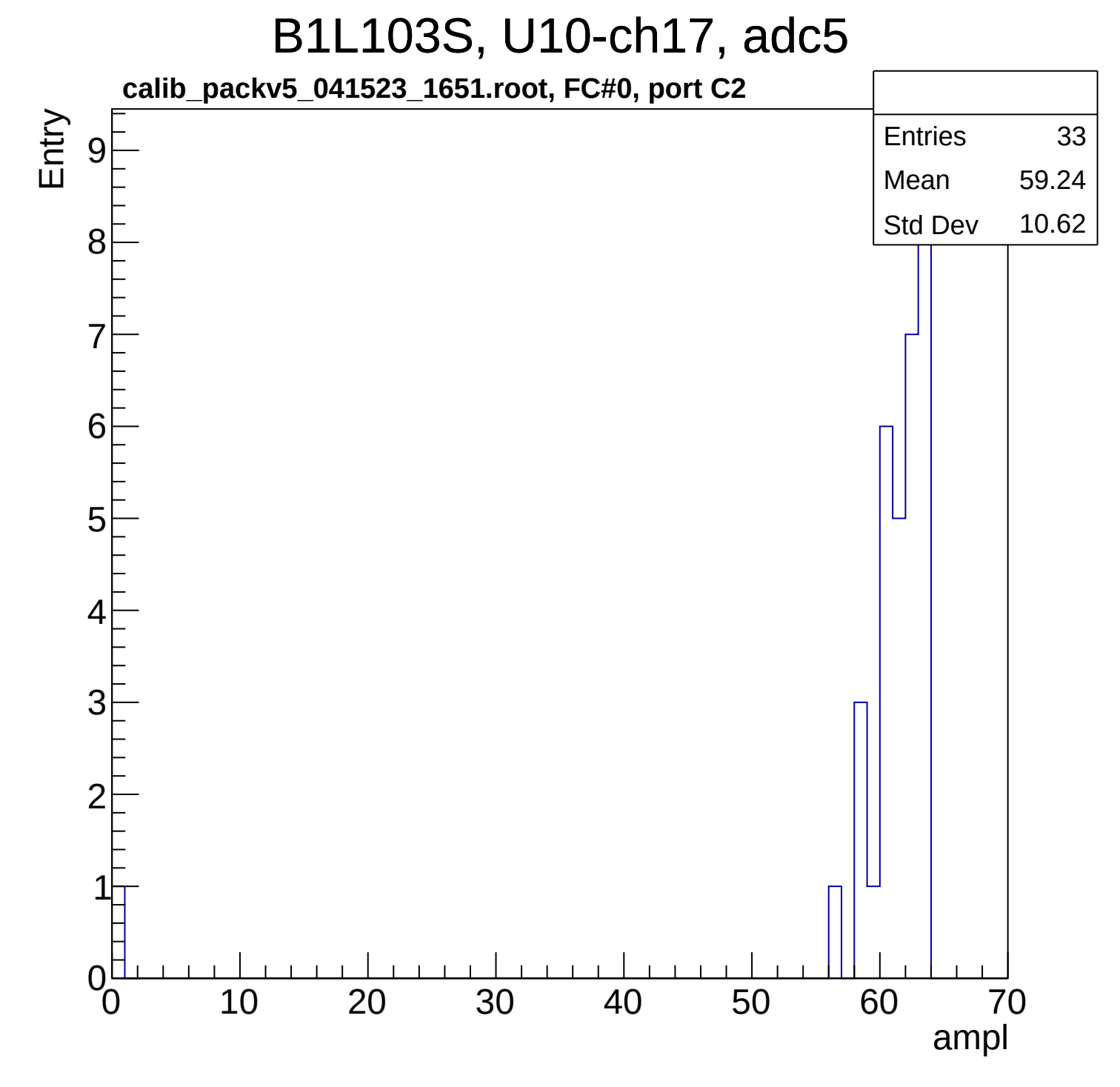
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U10-ch17, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 56.81
Std Dev 3.033
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U10-ch17, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 33
Mean 59.24
Std Dev 10.62
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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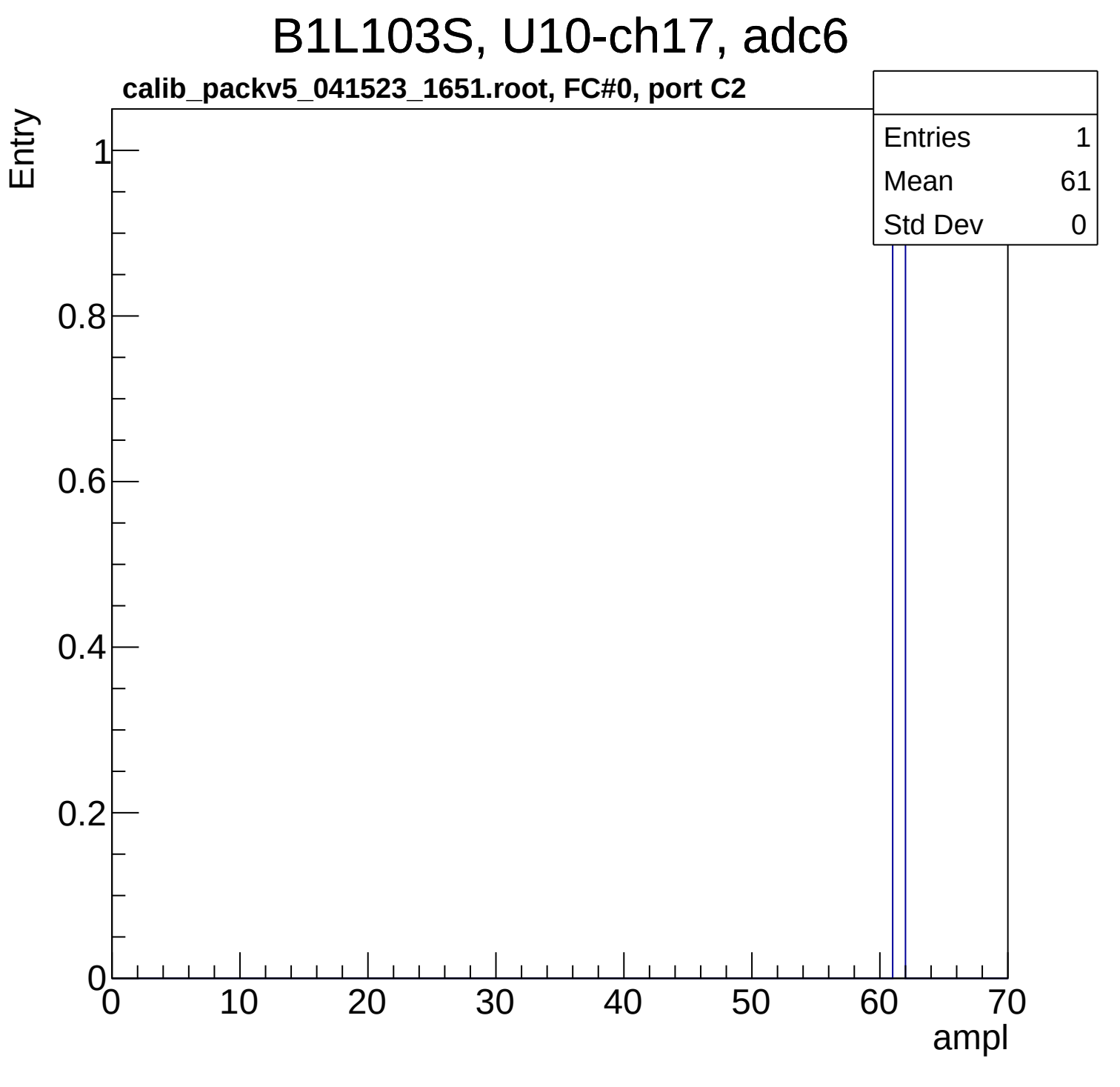
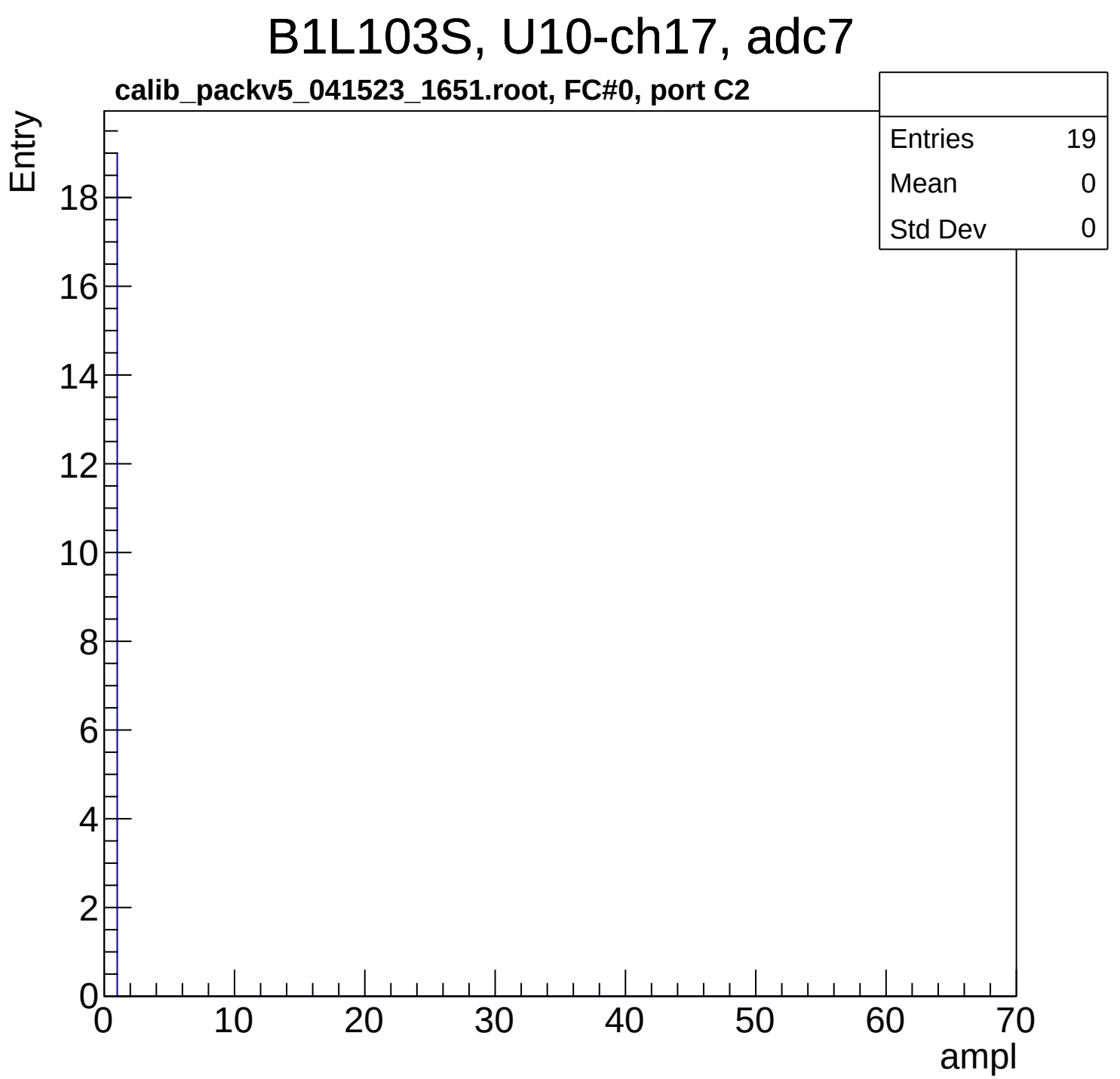
60
70


B1L103S, U10-ch17, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 1
Mean 61
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch17, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
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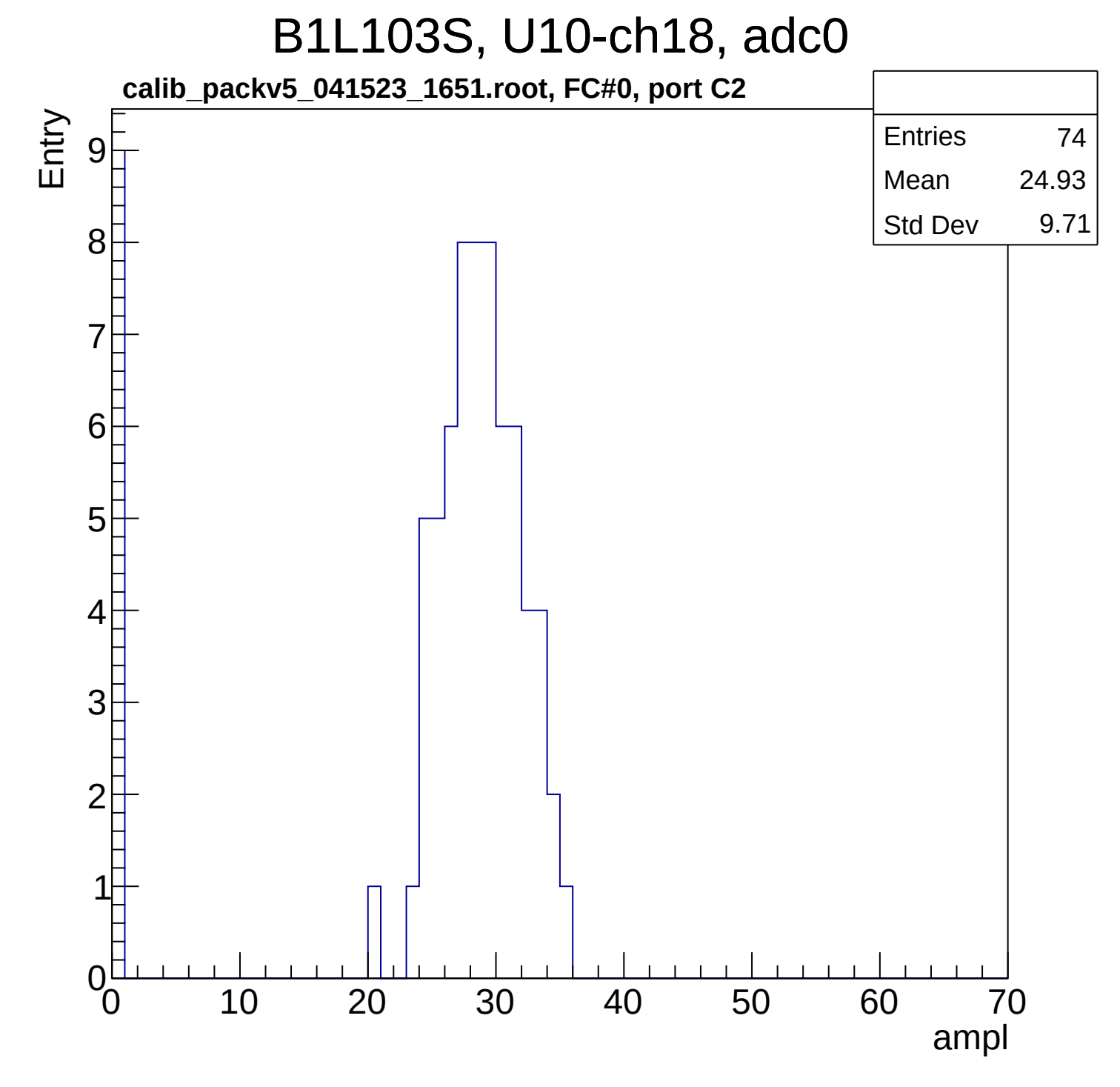
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch18, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 24.93
Std Dev 9.71
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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60
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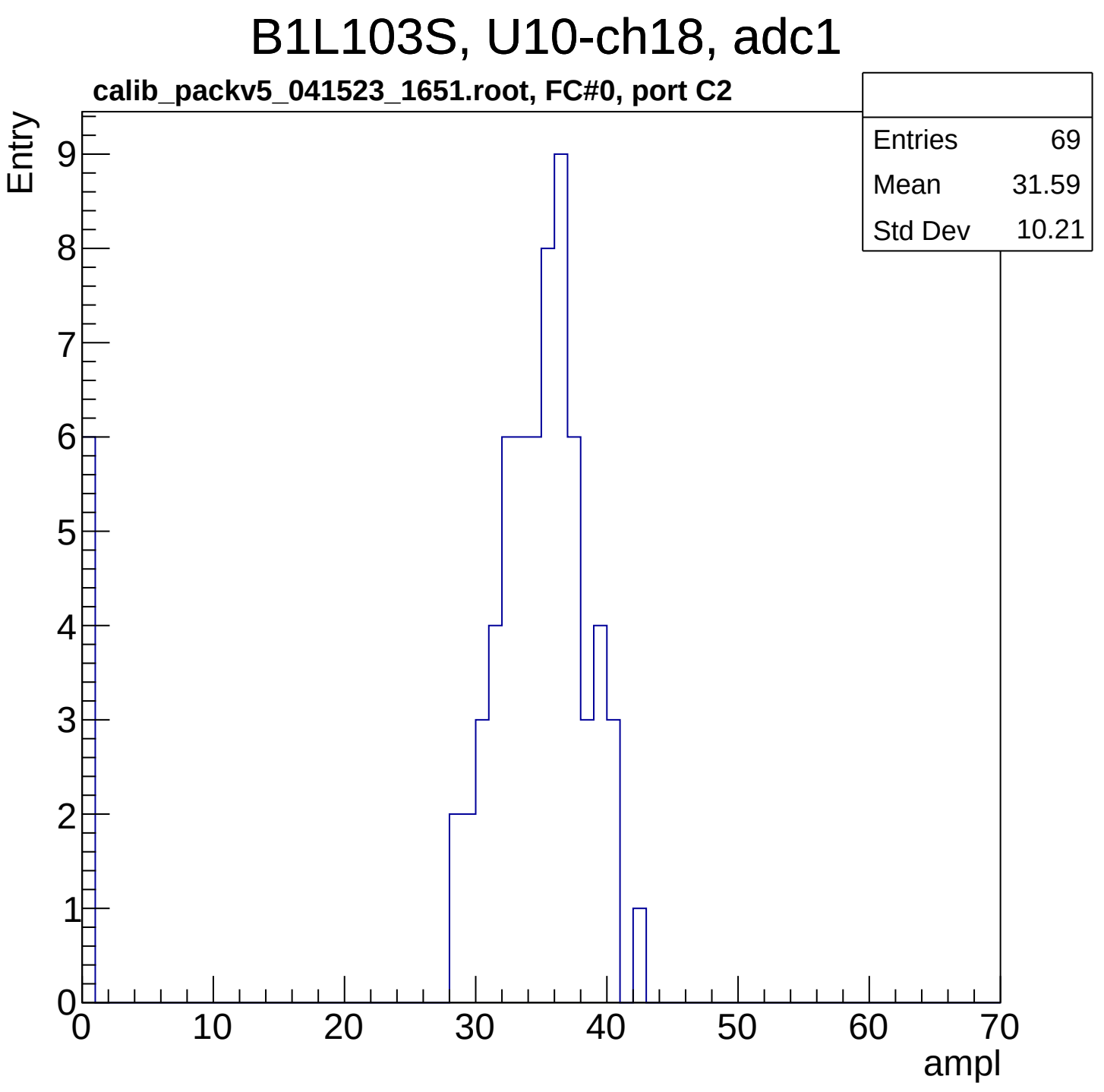
B1L103S, U10-ch18, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 31.59
Std Dev 10.21
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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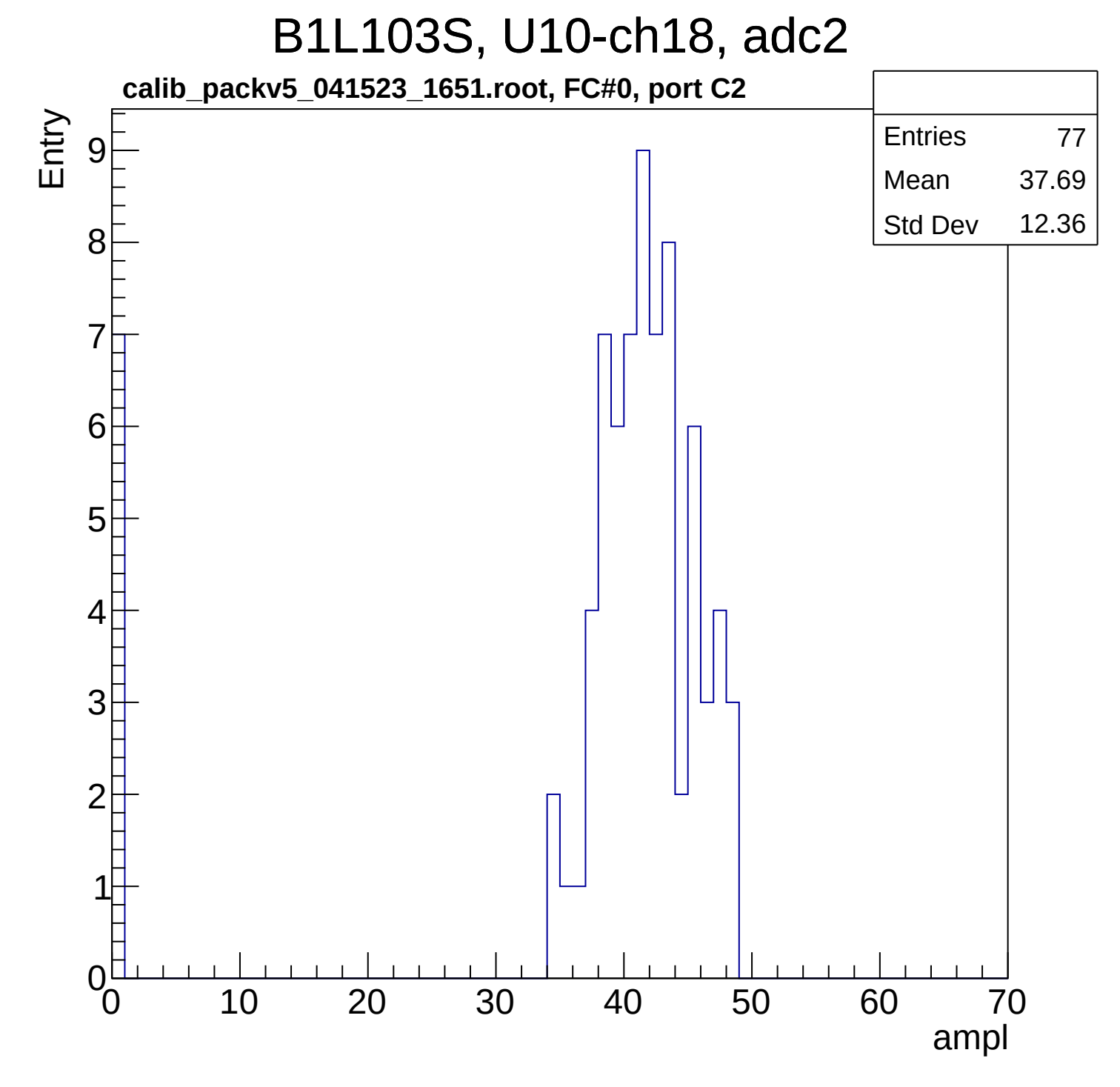
40
50
60
70


B1L103S, U10-ch18, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 37.69
Std Dev 12.36
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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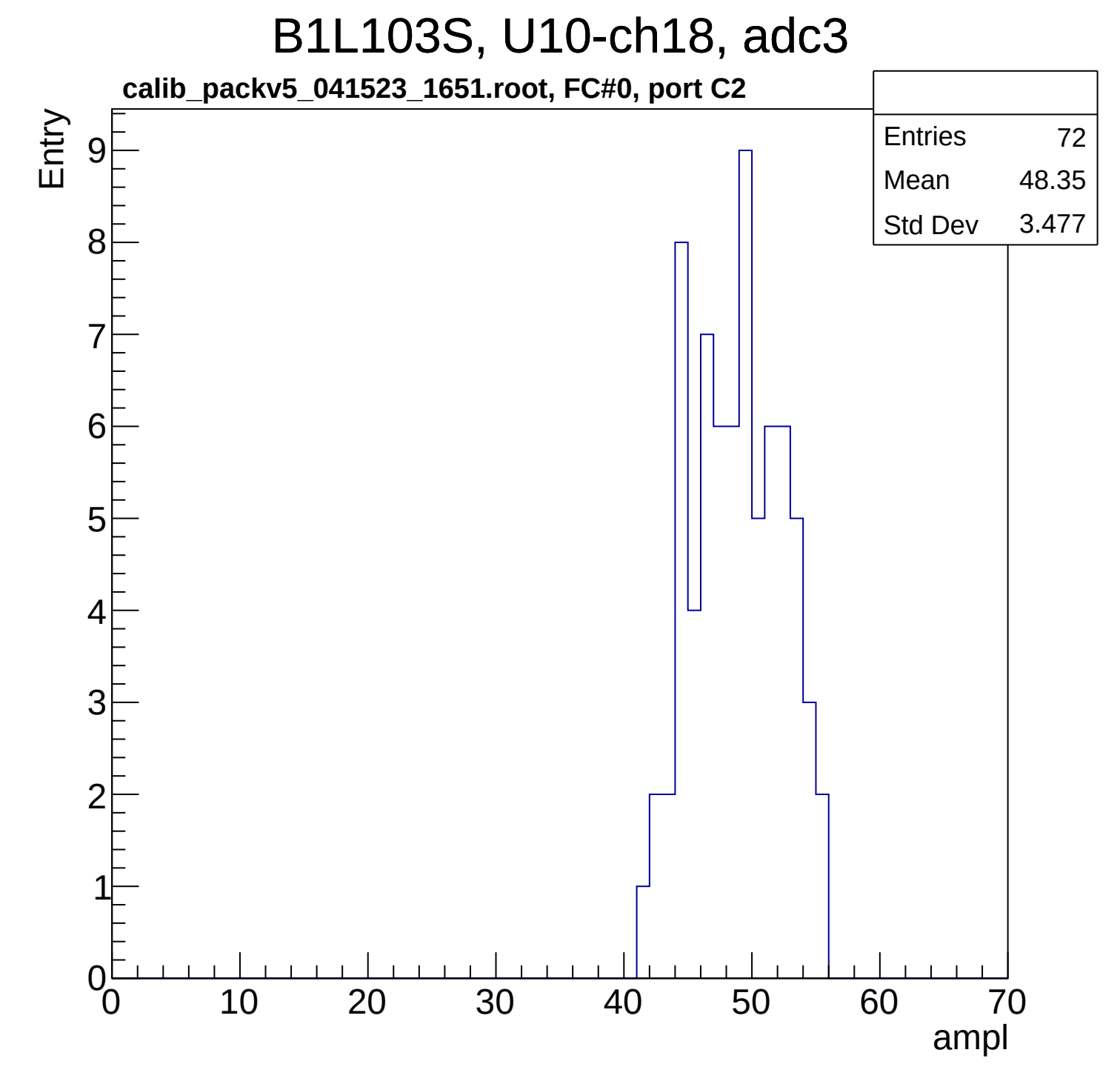
40
50
60
70


B1L103S, U10-ch18, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 48.35
Std Dev 3.477
Entry
ampl
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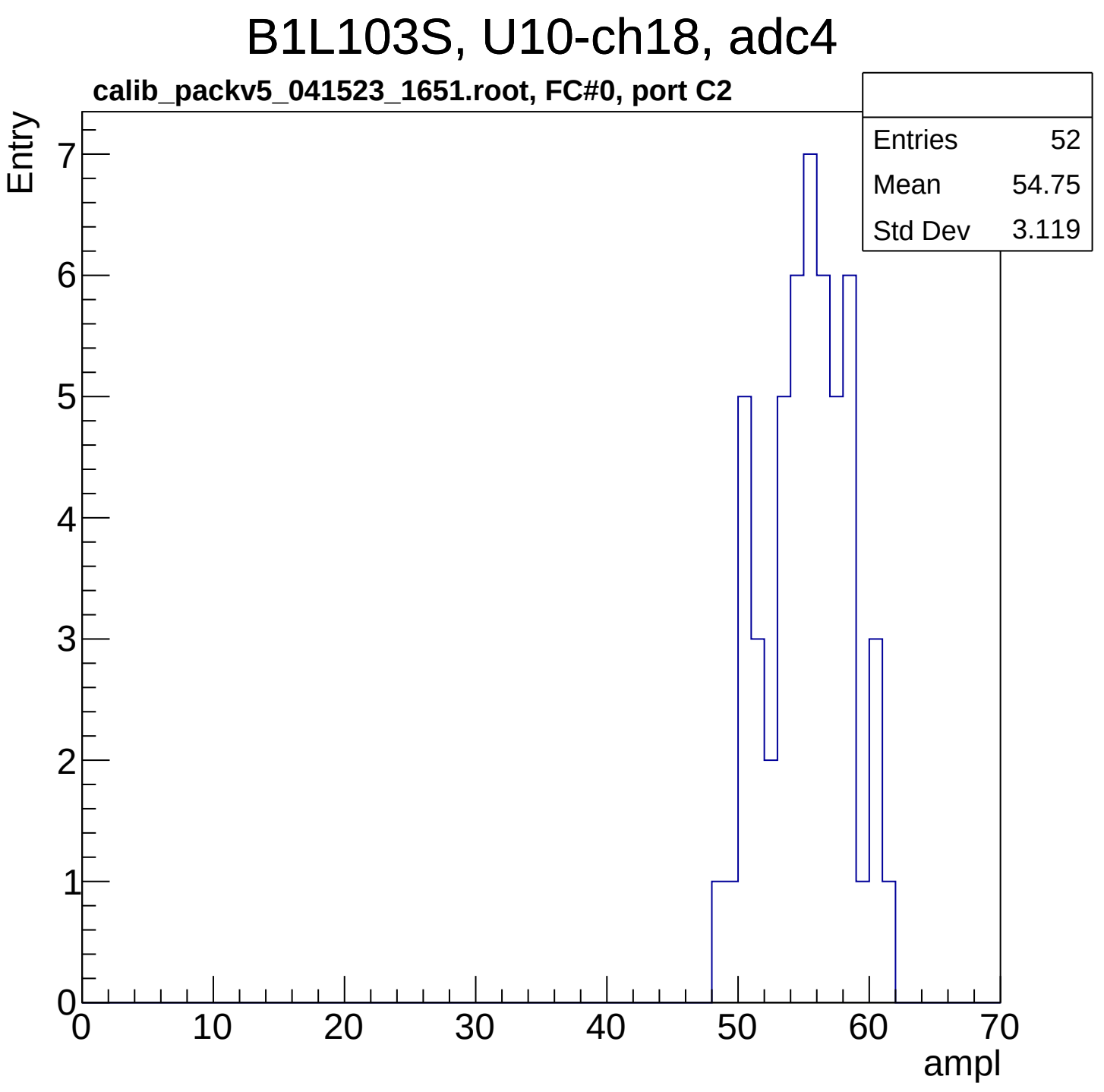
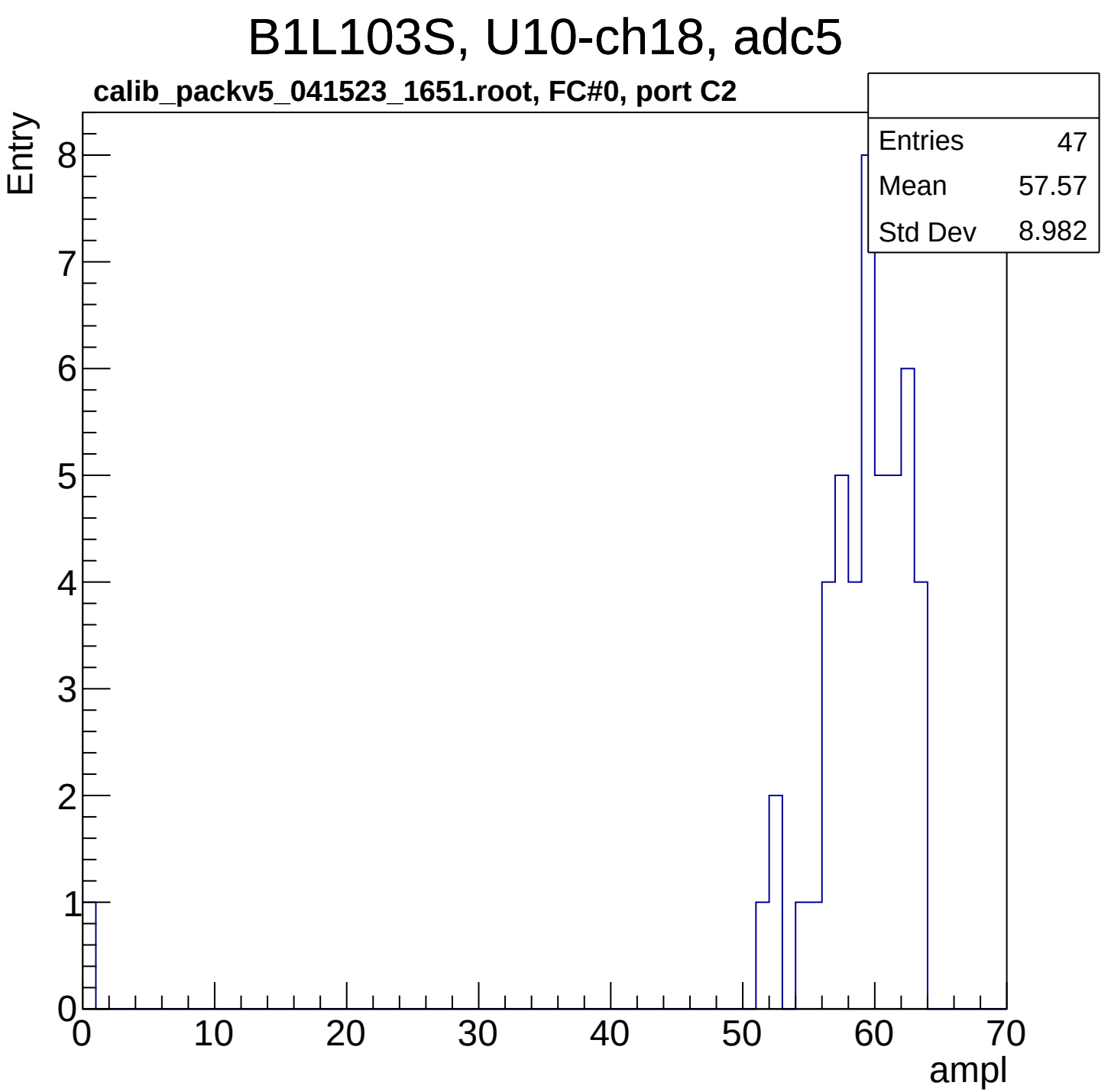
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U10-ch18, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 54.75
Std Dev 3.119
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U10-ch18, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 57.57
Std Dev 8.982
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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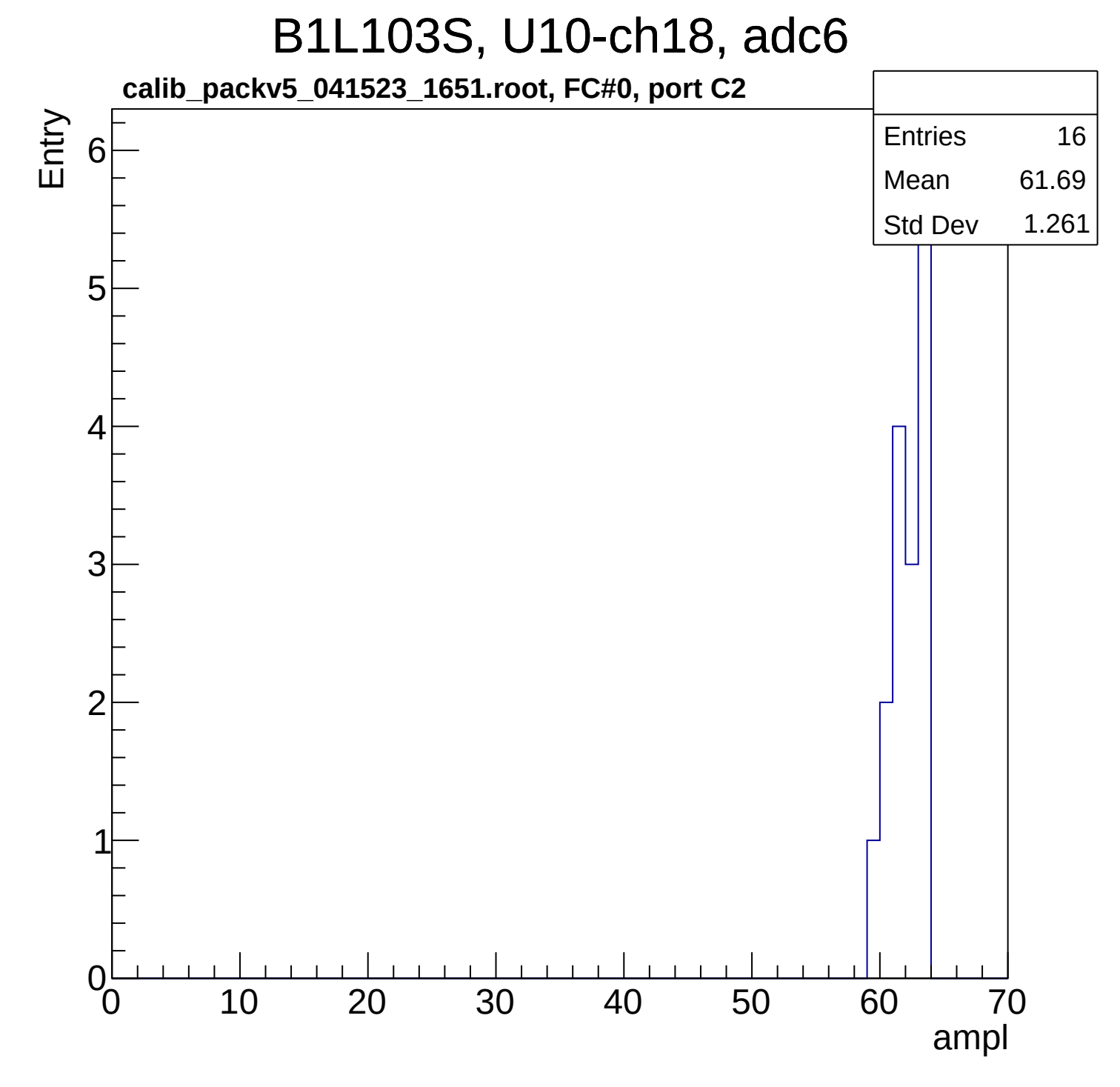
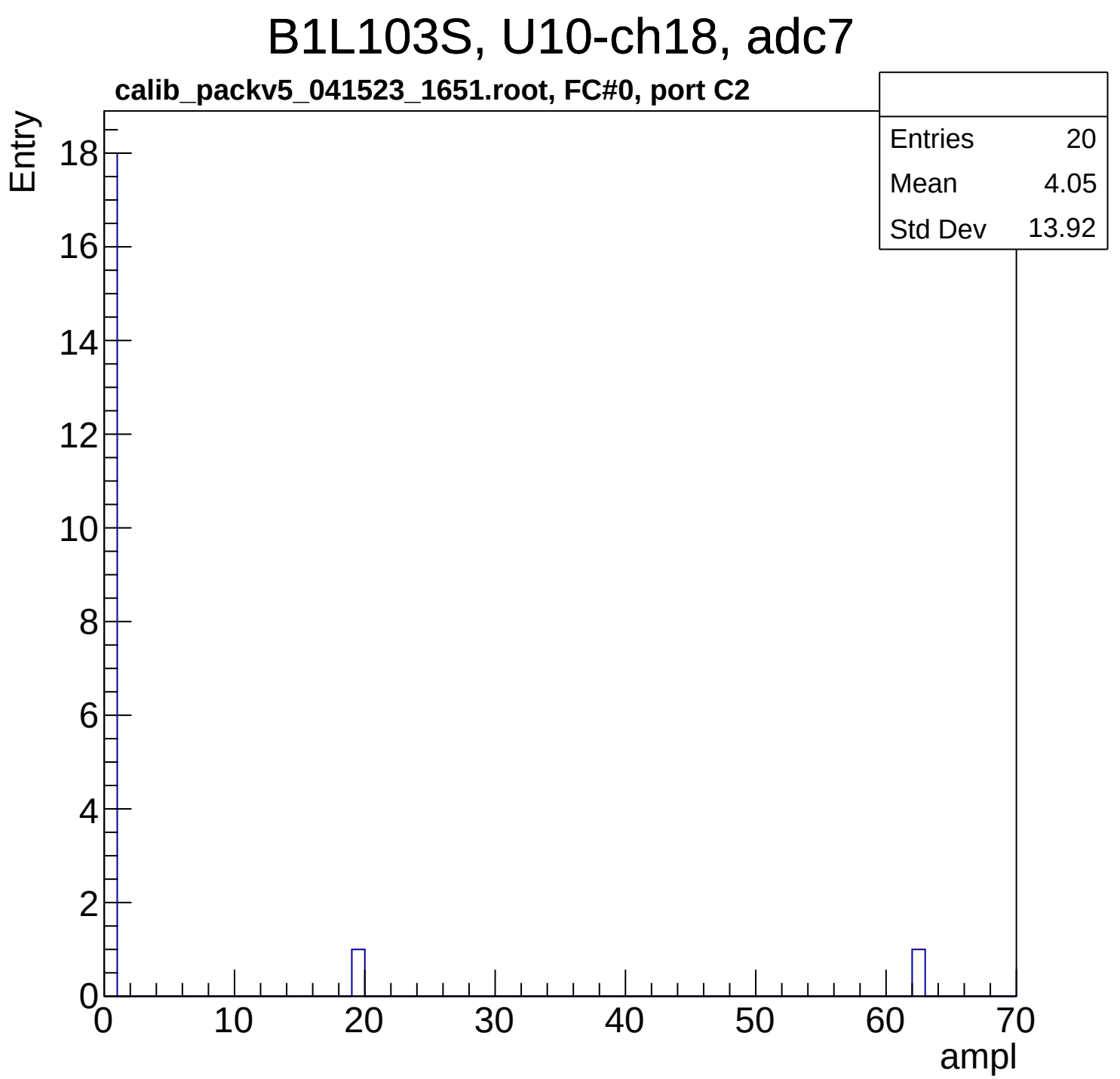
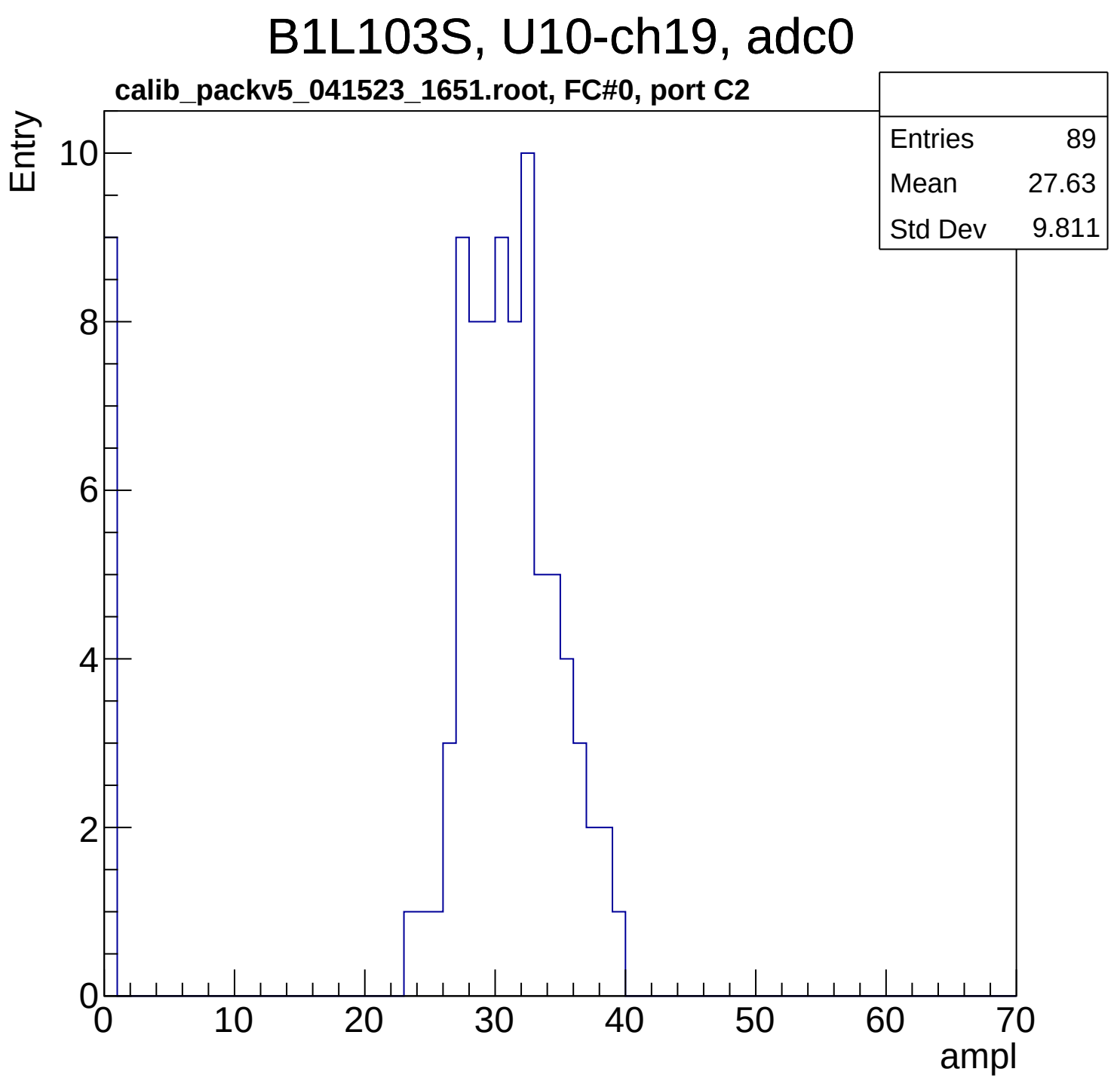
40
50
60
70


B1L103S, U10-ch18, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 16
Mean 61.69
Std Dev 1.261
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U10-ch18, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 4.05
Std Dev 13.92
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch19, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 89
Mean 27.63
Std Dev 9.811
Entry
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50
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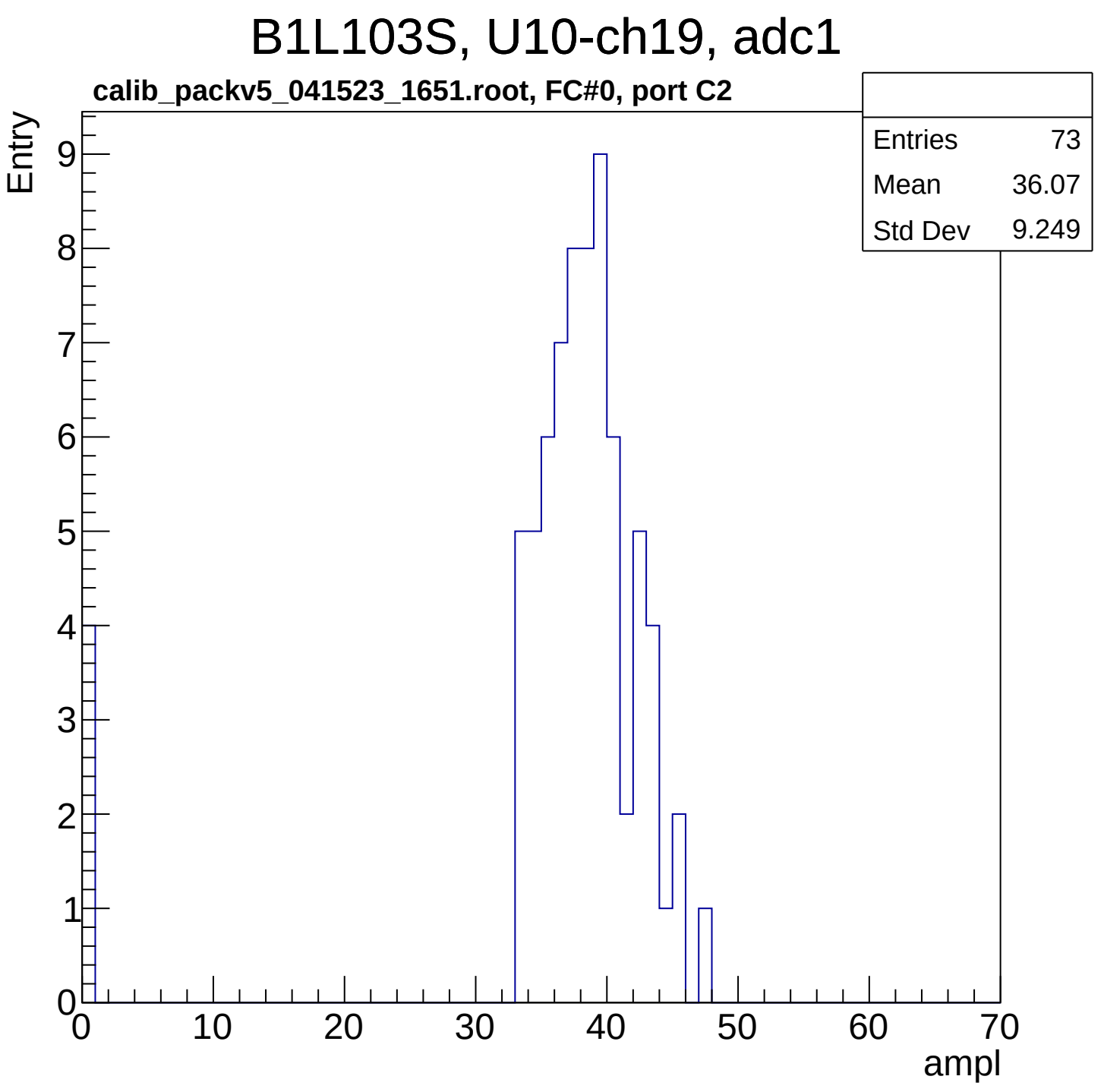
70
ampl


B1L103S, U10-ch19, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 36.07
Std Dev 9.249
Entry
ampl
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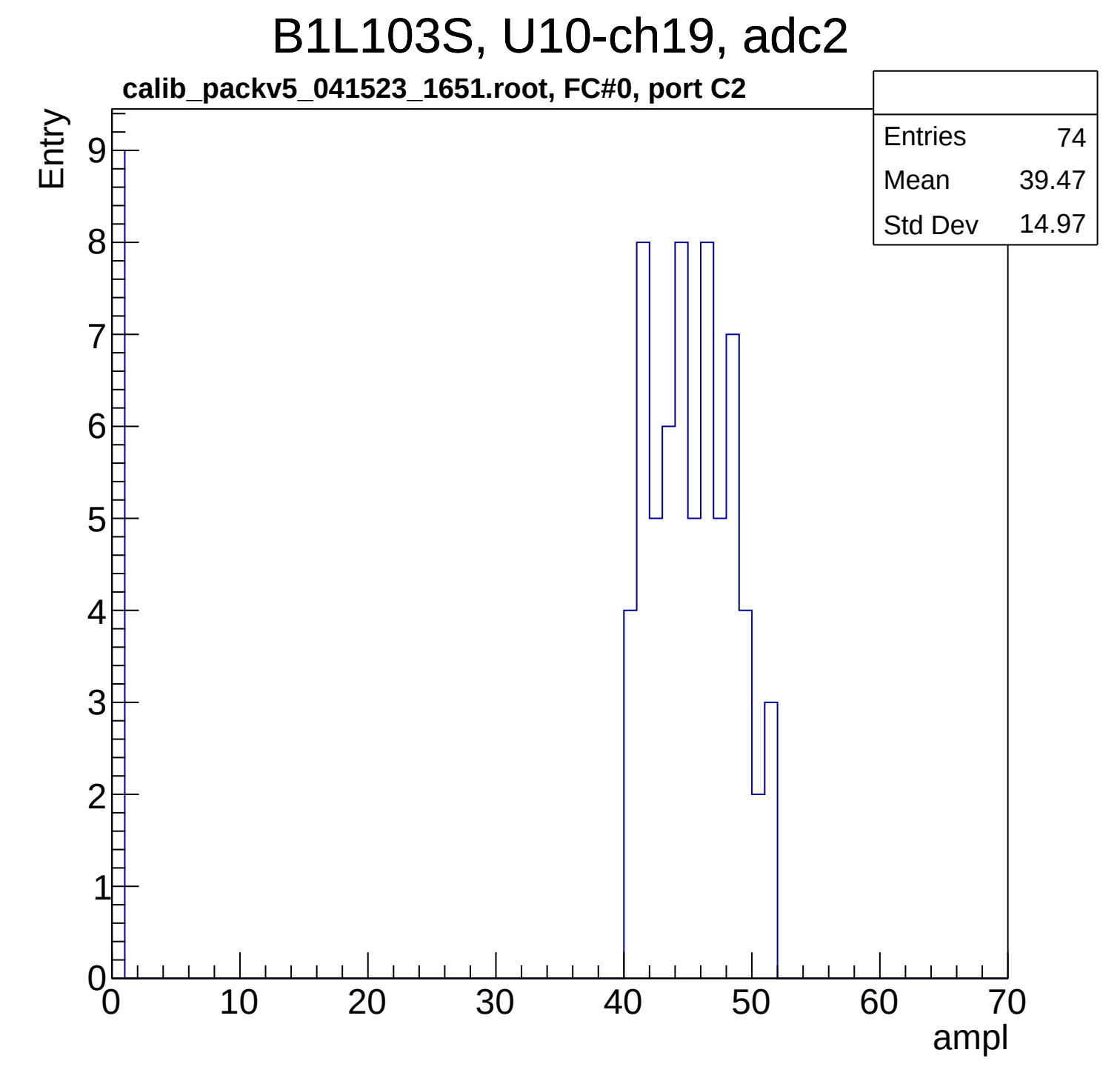
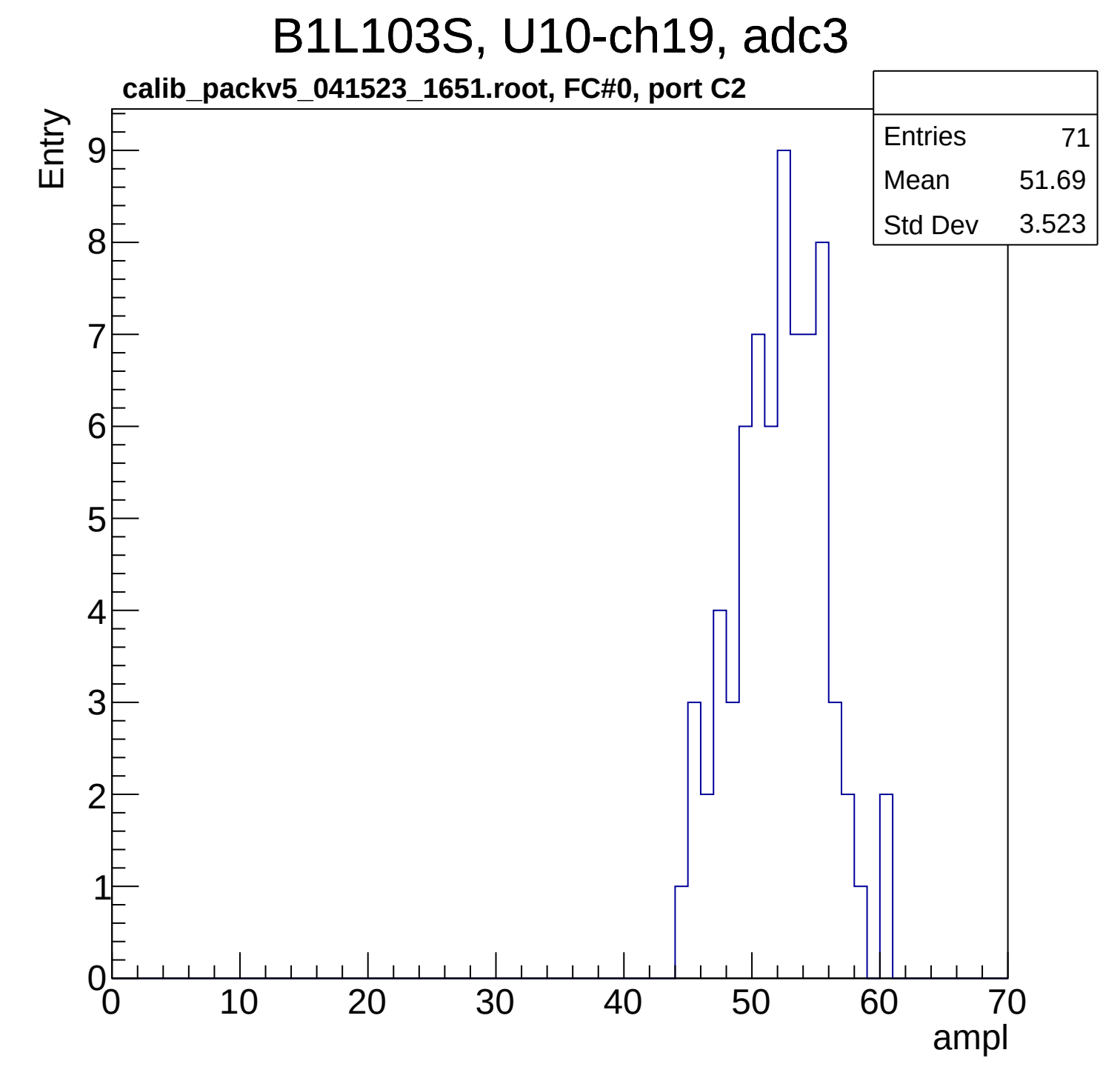
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U10-ch19, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 39.47
Std Dev 14.97
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U10-ch19, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 51.69
Std Dev 3.523
Entry
ampl
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2
3
4
5
6
7
8
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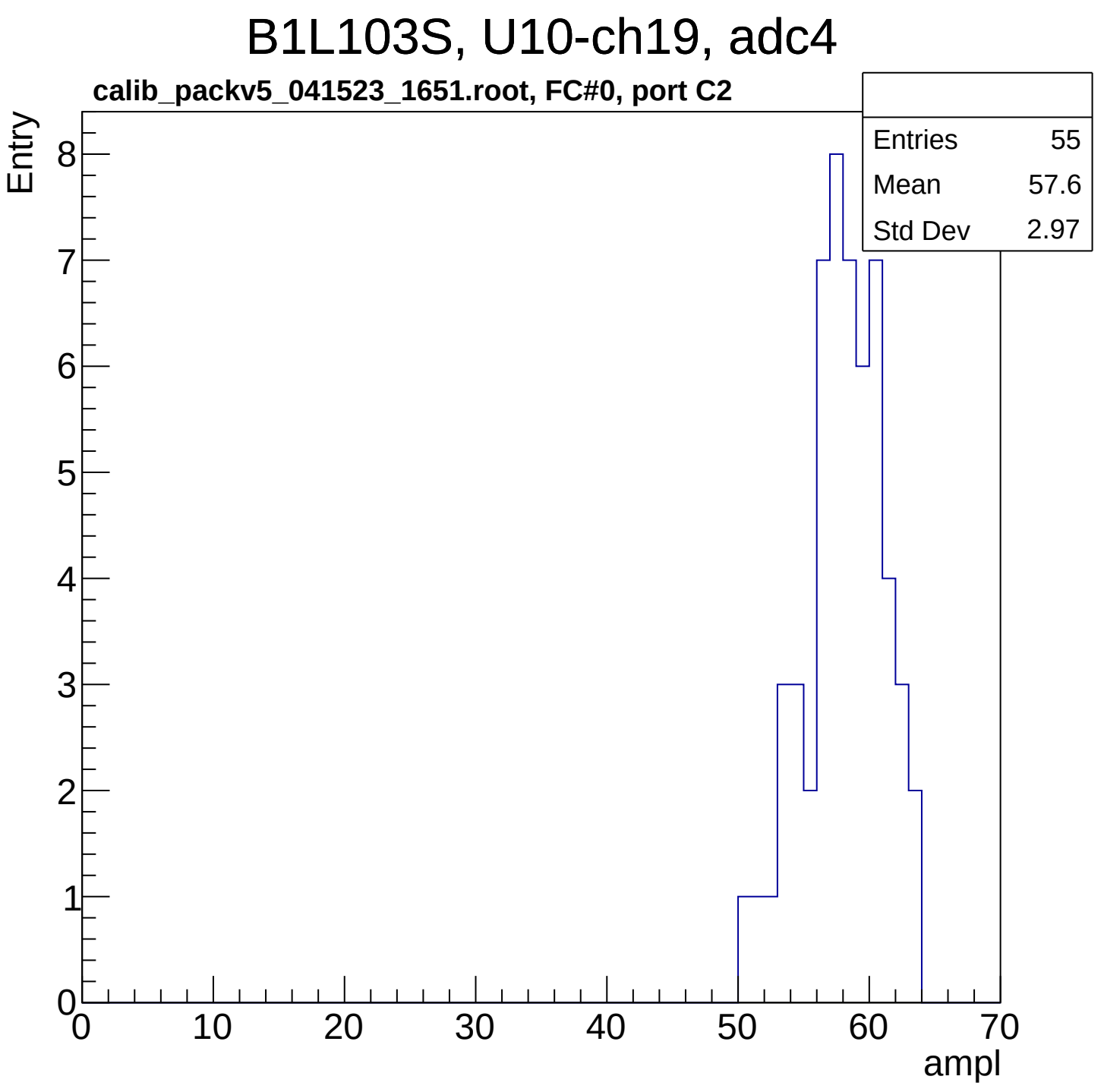
B1L103S, U10-ch19, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 57.6
Std Dev 2.97
Entry
ampl
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1
2
3
4
5
6
7
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0
10
20
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40
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60
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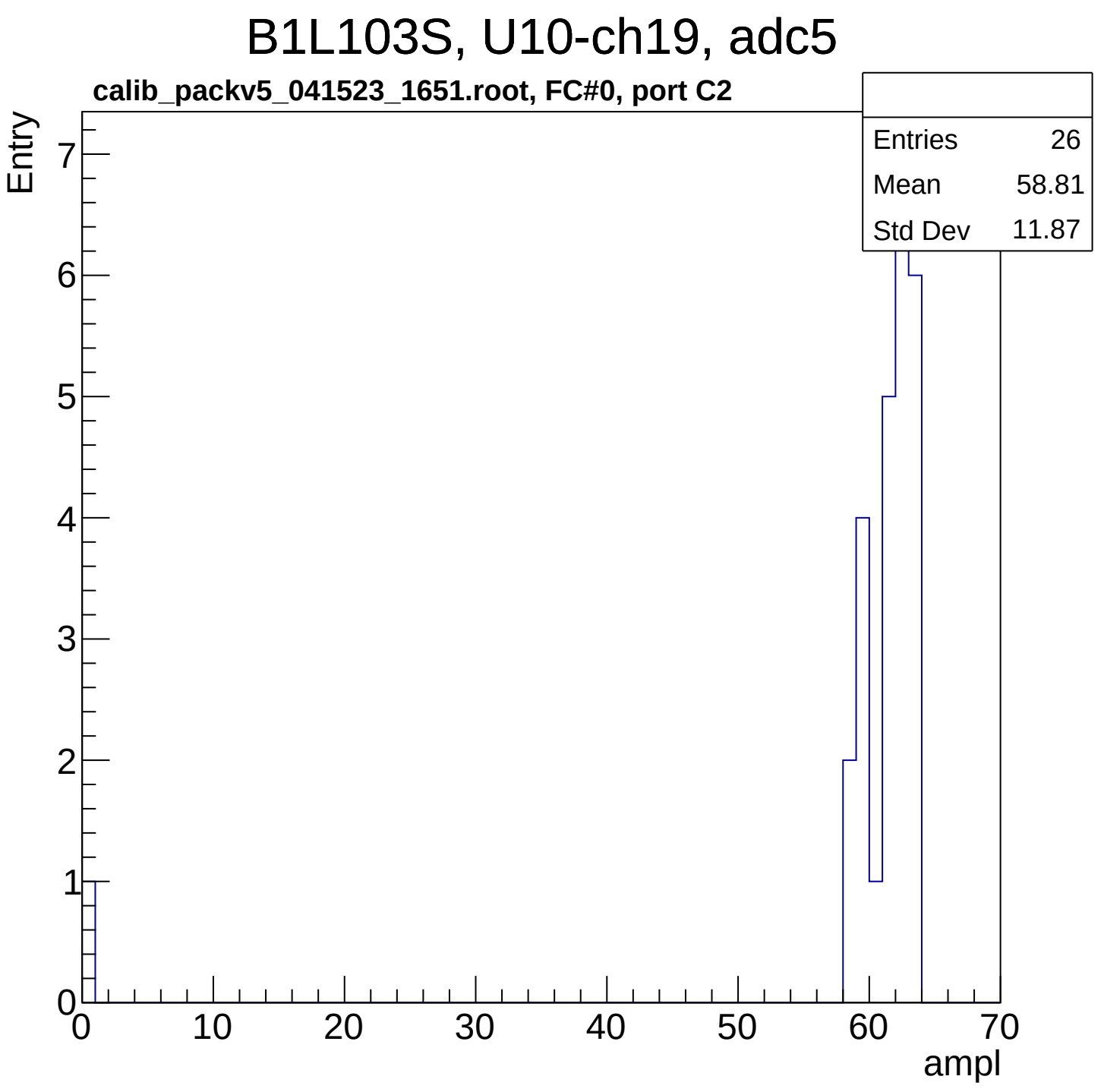
B1L103S, U10-ch19, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 26
Mean 58.81
Std Dev 11.87
Entry
ampl
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4
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6
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0
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40
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60
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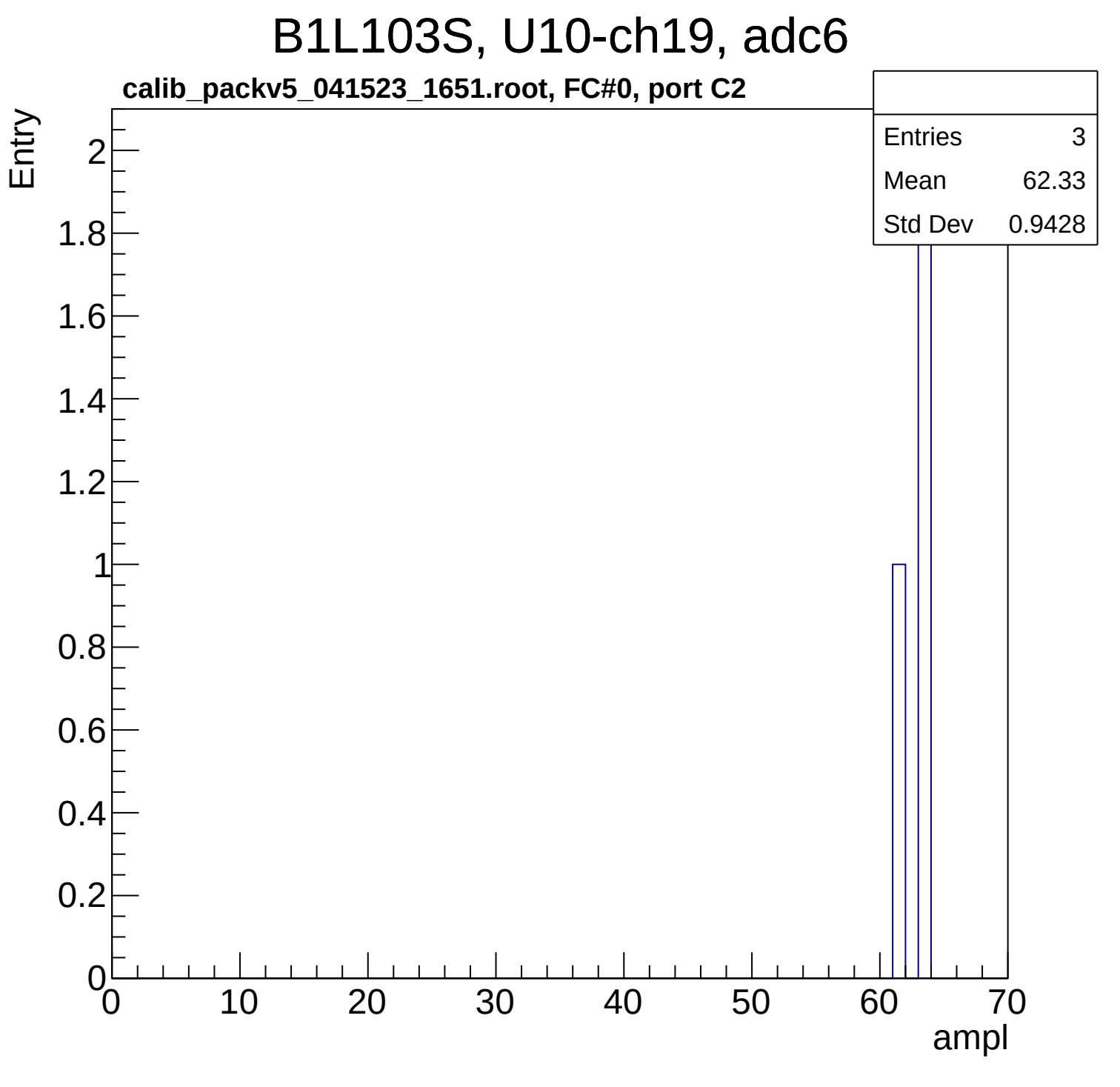
B1L103S, U10-ch19, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 3
Mean 62.33
Std Dev 0.9428
Entry
ampl
0
0.2
0.4
0.6
0.8
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1.2
1.4
1.6
1.8
2
0
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40
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60
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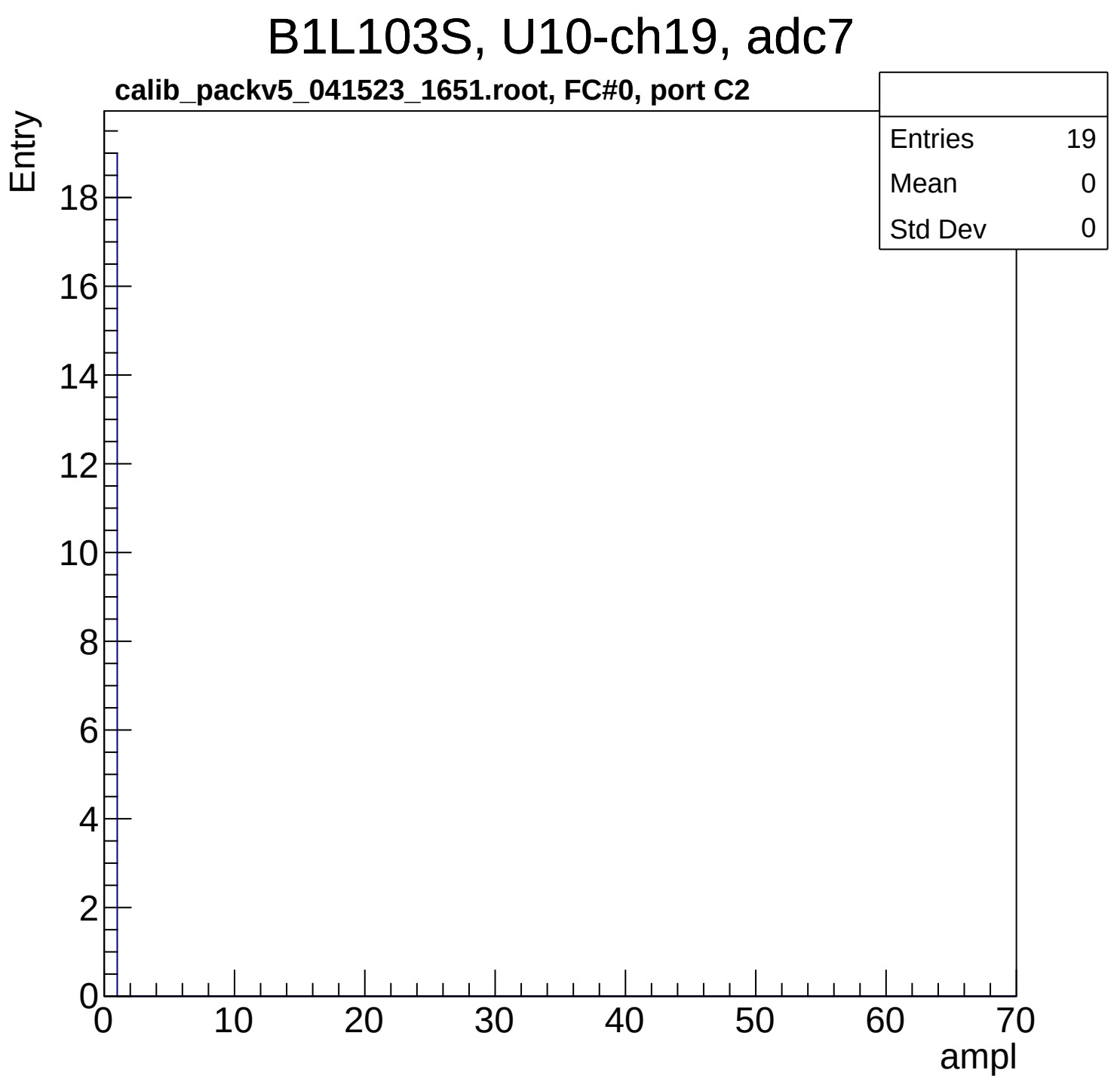
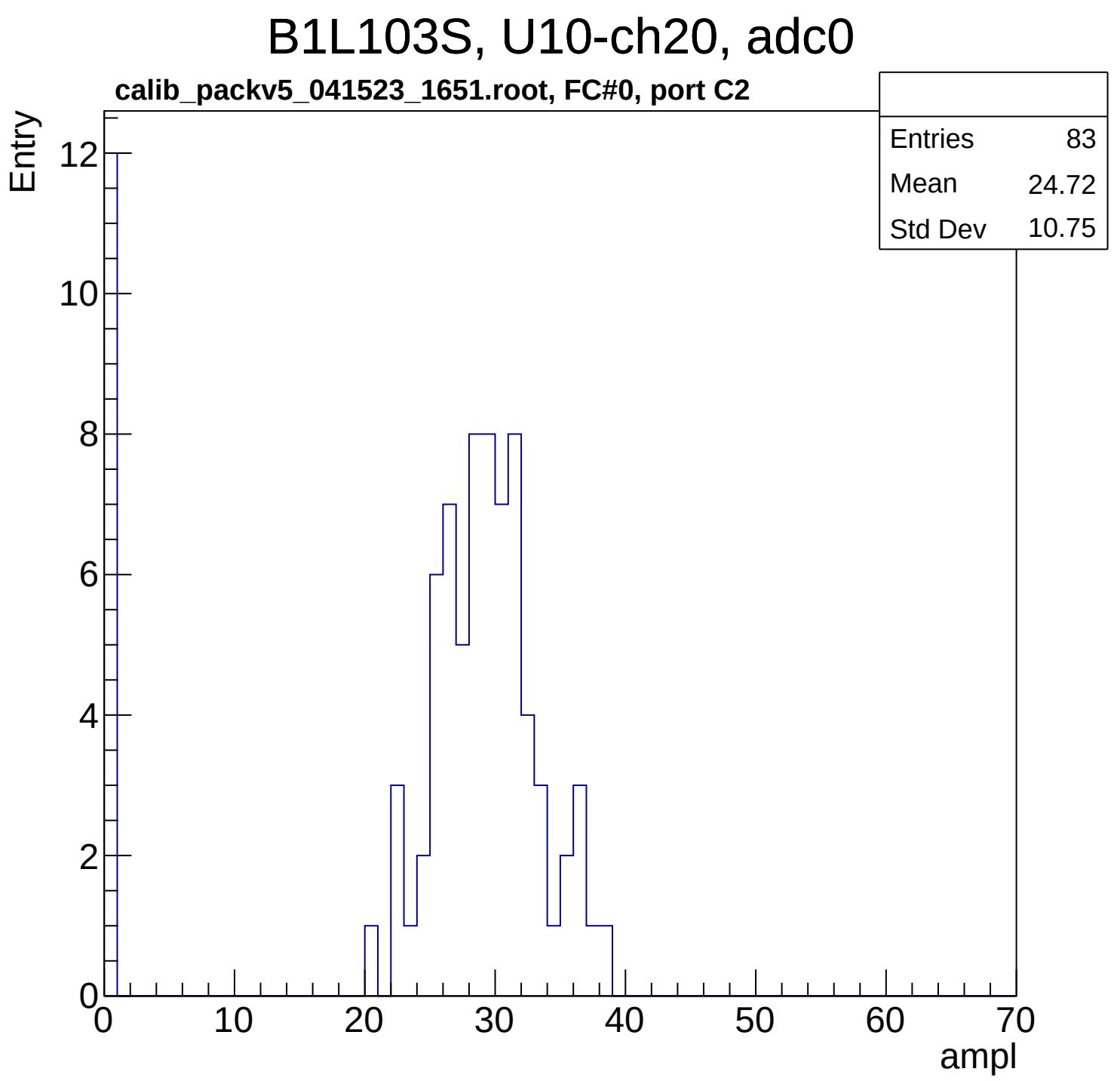
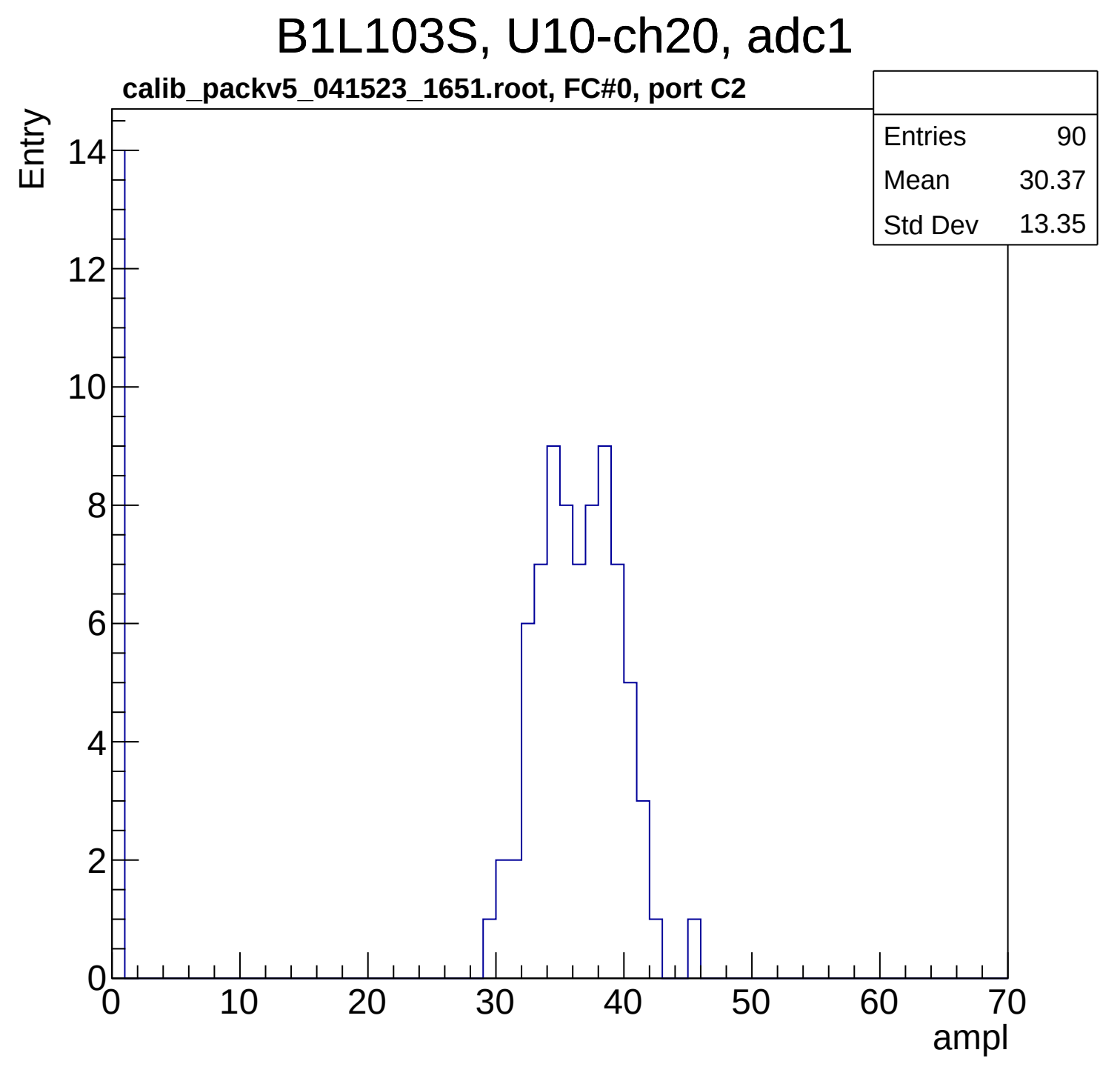

B1L103S, U10-ch19, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch20, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 24.72
Std Dev 10.75
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch20, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 90
Mean 30.37
Std Dev 13.35
Entry
ampl
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2
4
6
8
10
12
14
0
10
20
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40
50
60
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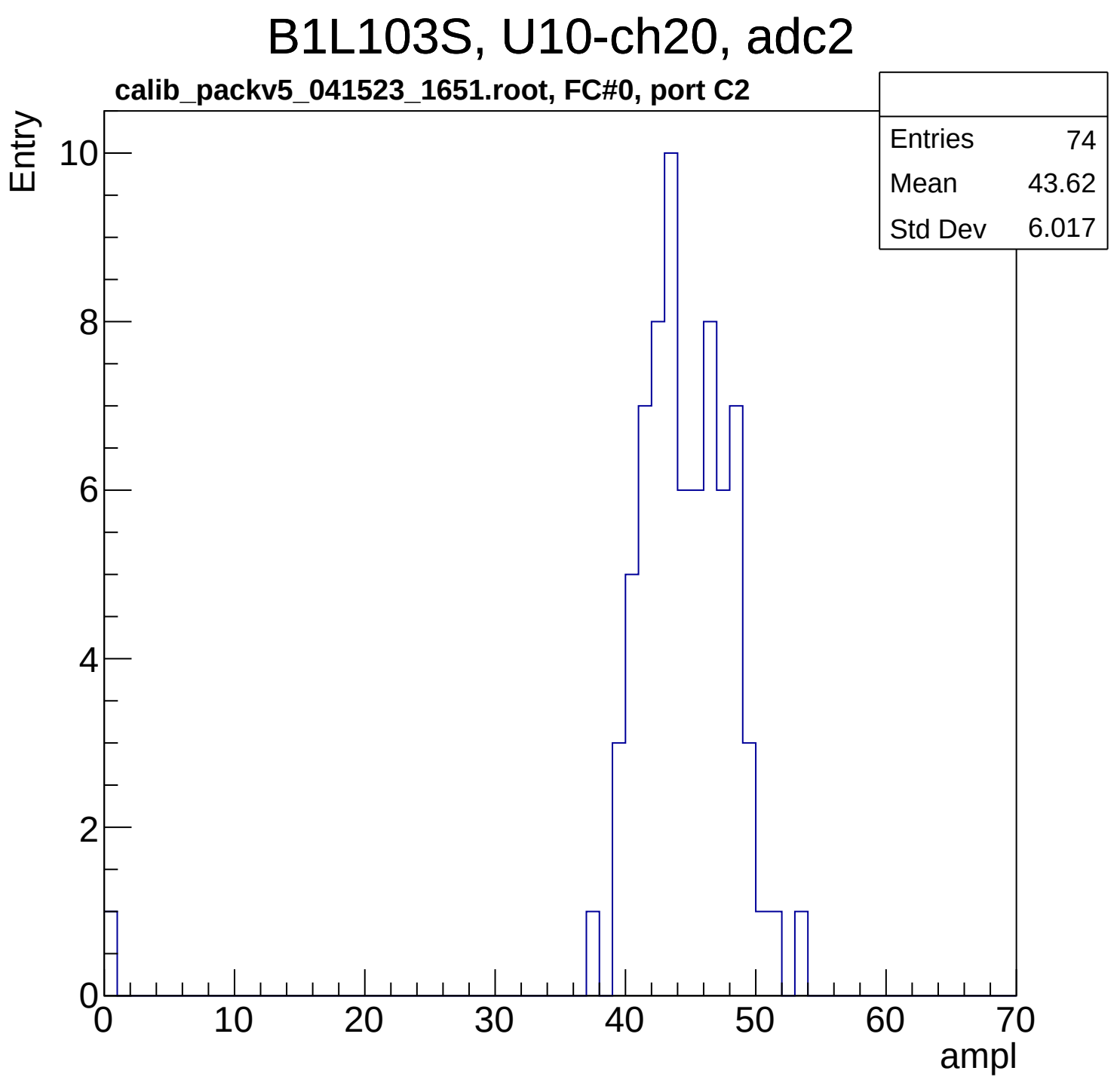
B1L103S, U10-ch20, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 43.62
Std Dev 6.017
Entry
ampl
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2
4
6
8
10
0
10
20
30
40
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60
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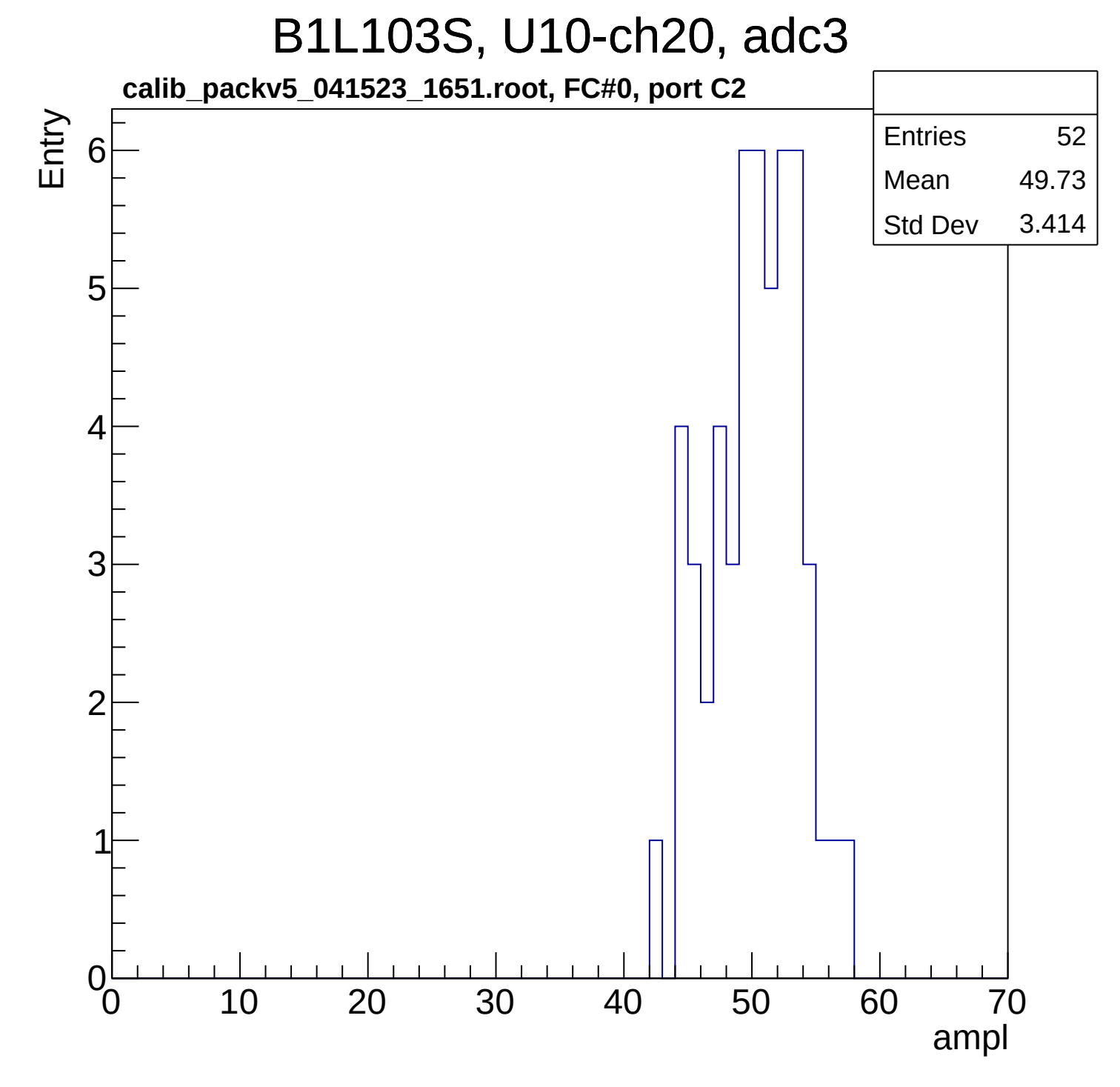
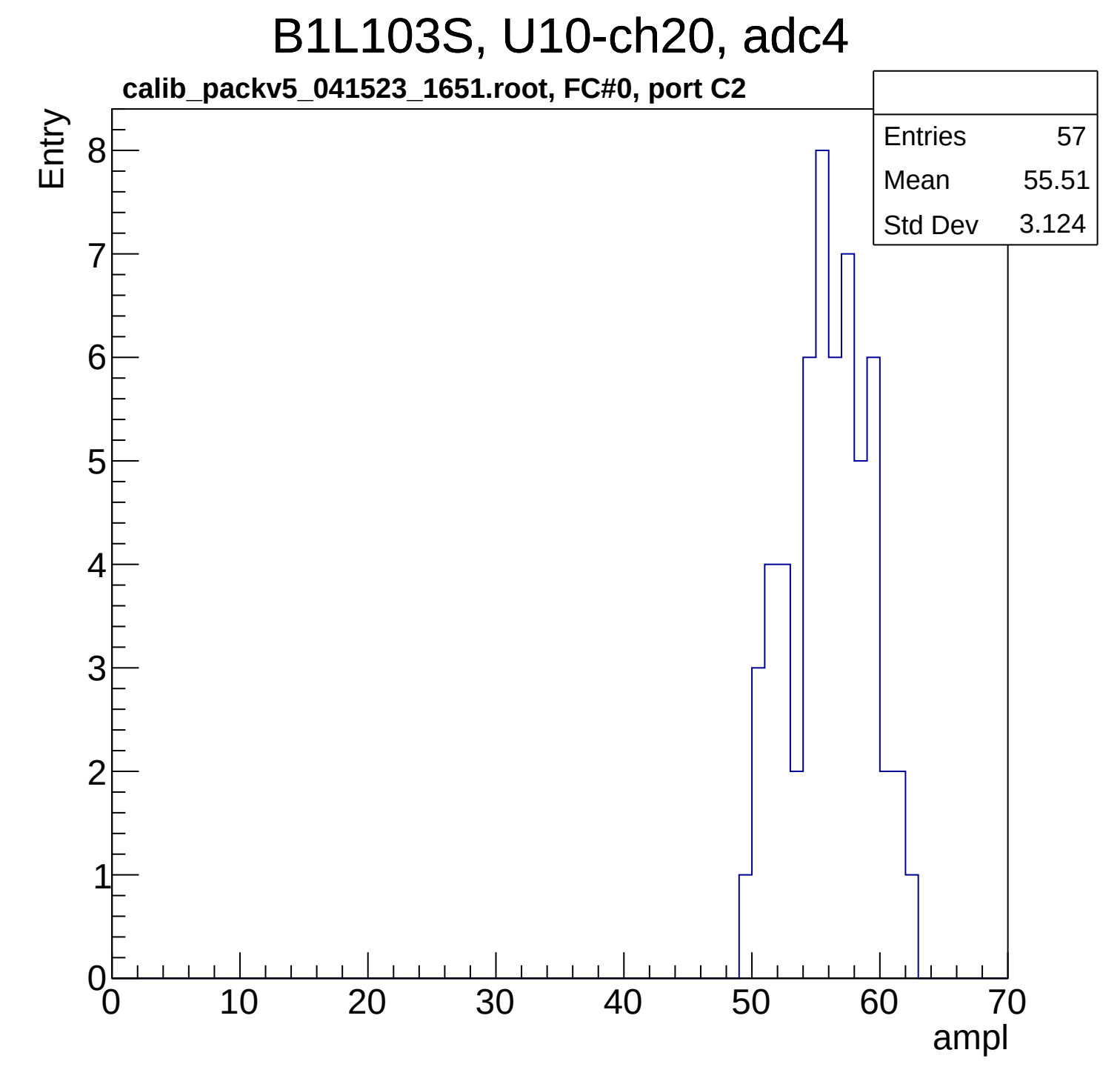
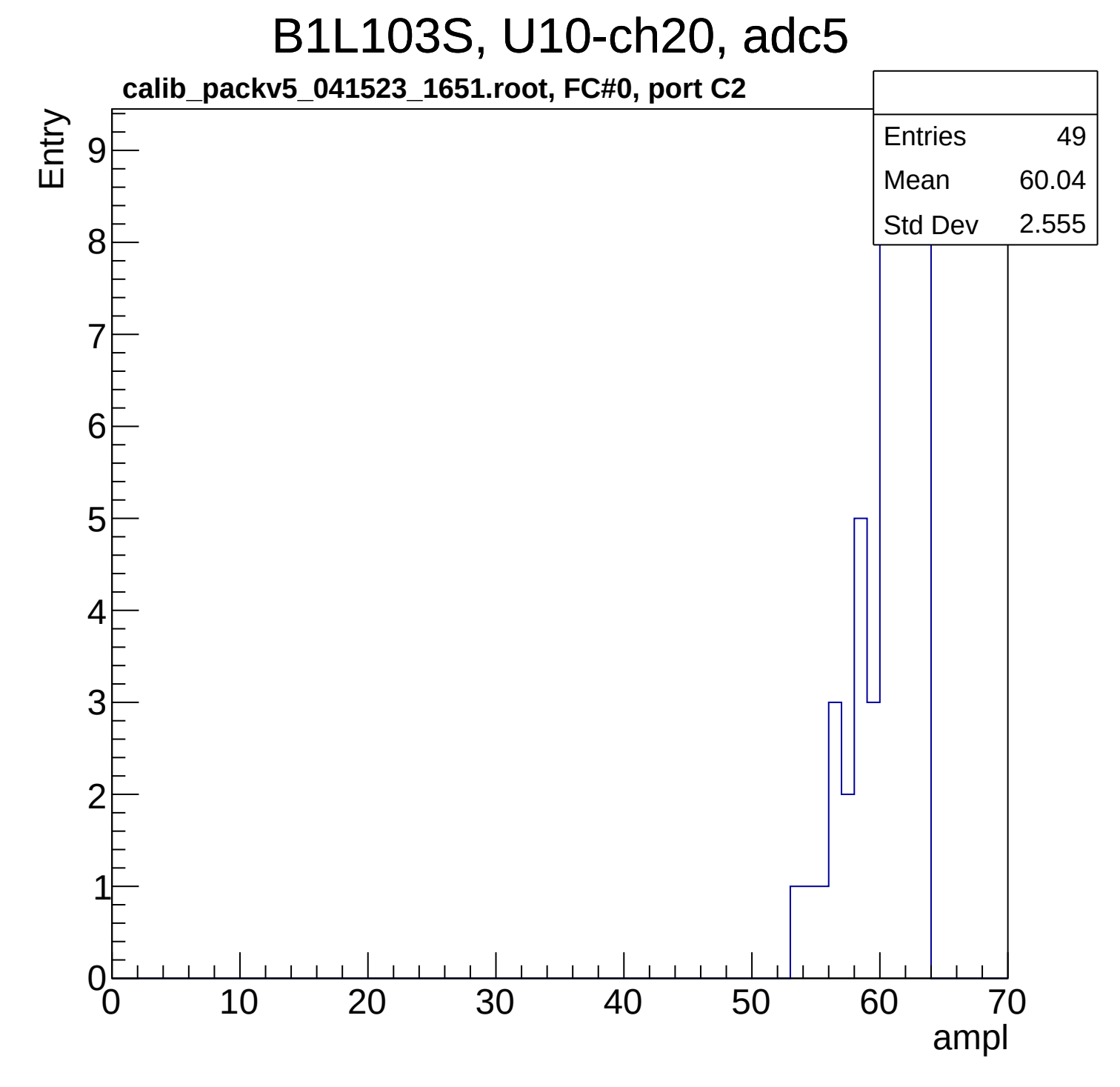

B1L103S, U10-ch20, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 49.73
Std Dev 3.414
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U10-ch20, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 55.51
Std Dev 3.124
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U10-ch20, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 60.04
Std Dev 2.555
Entry
ampl
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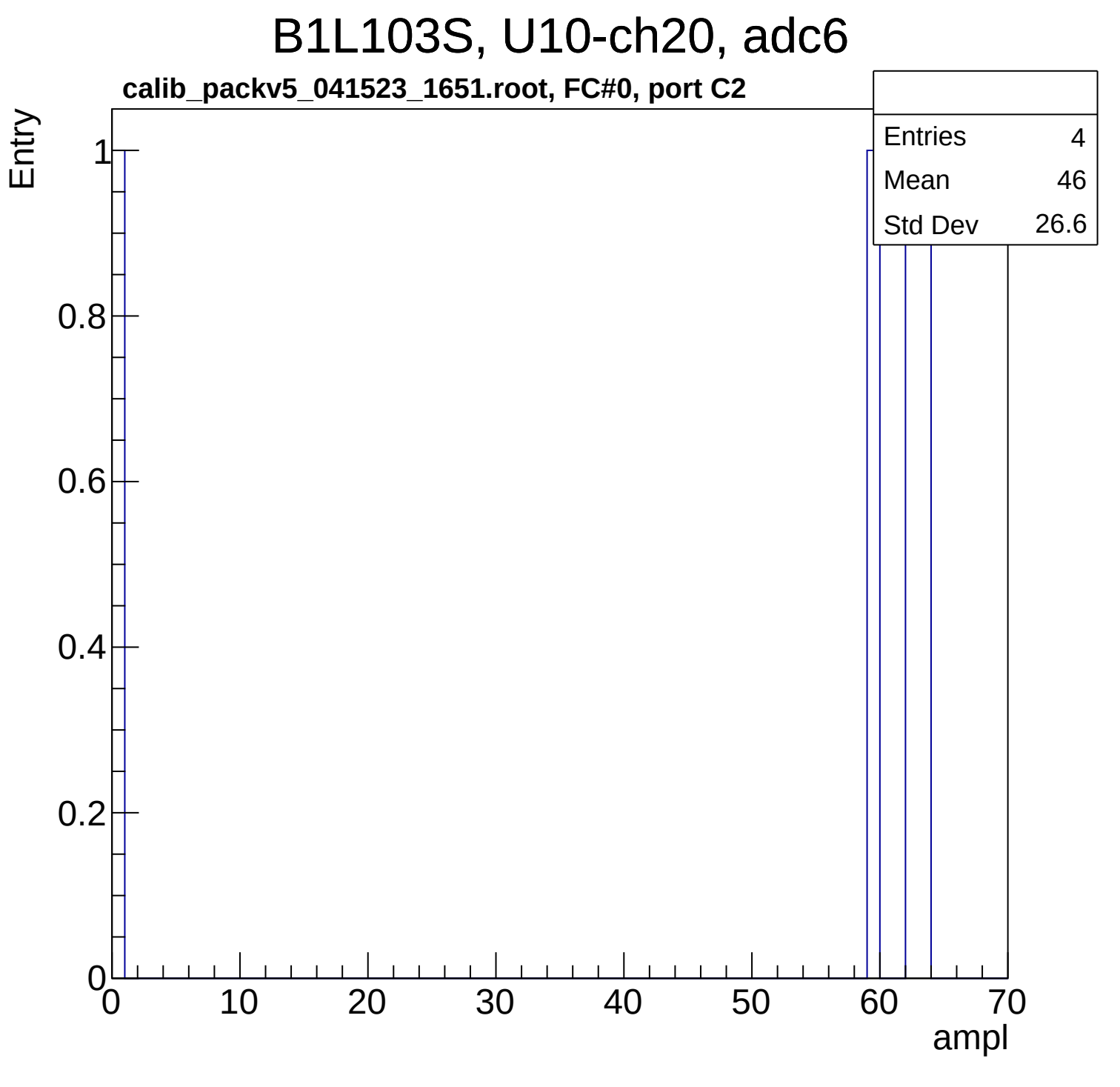
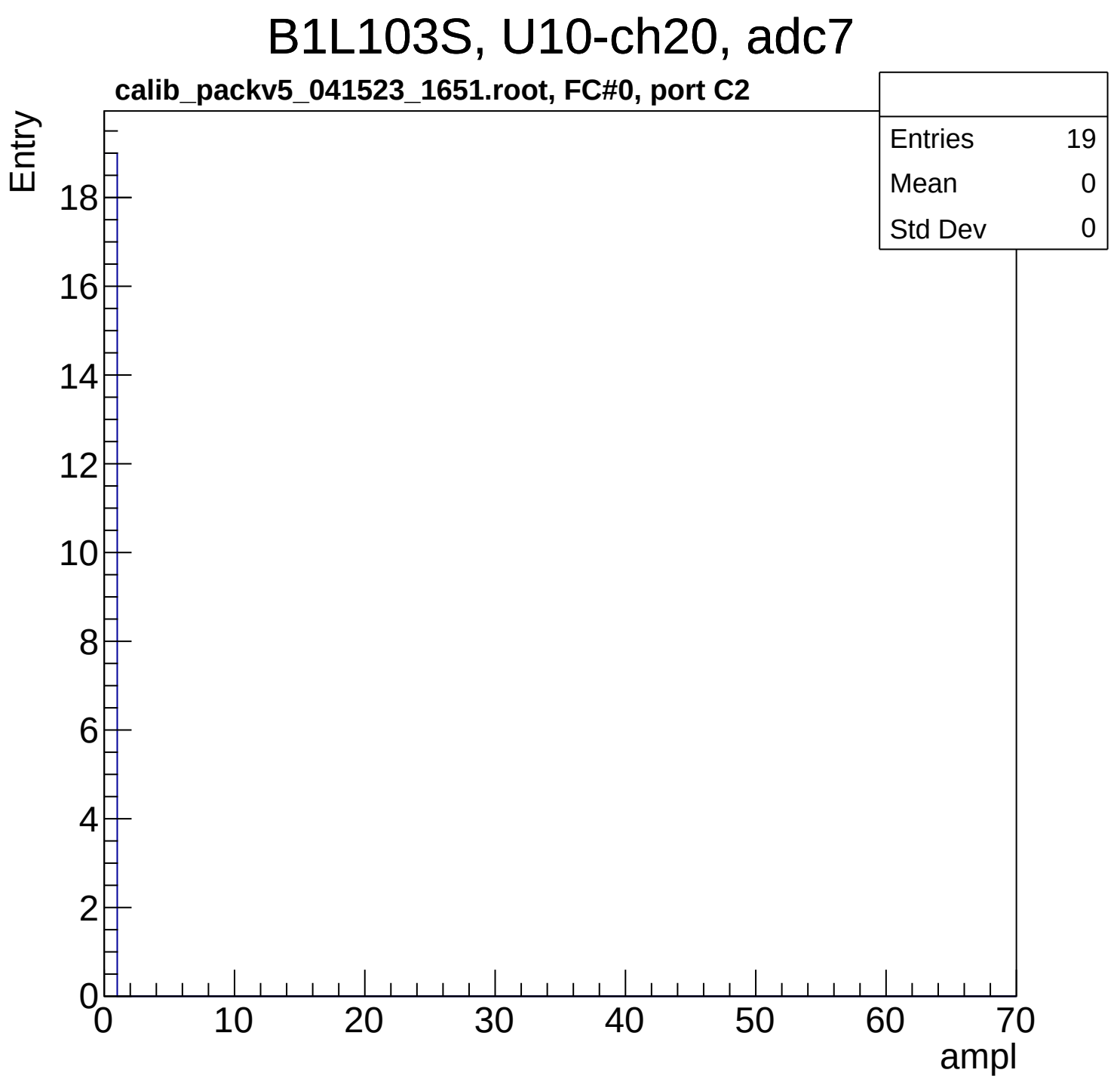
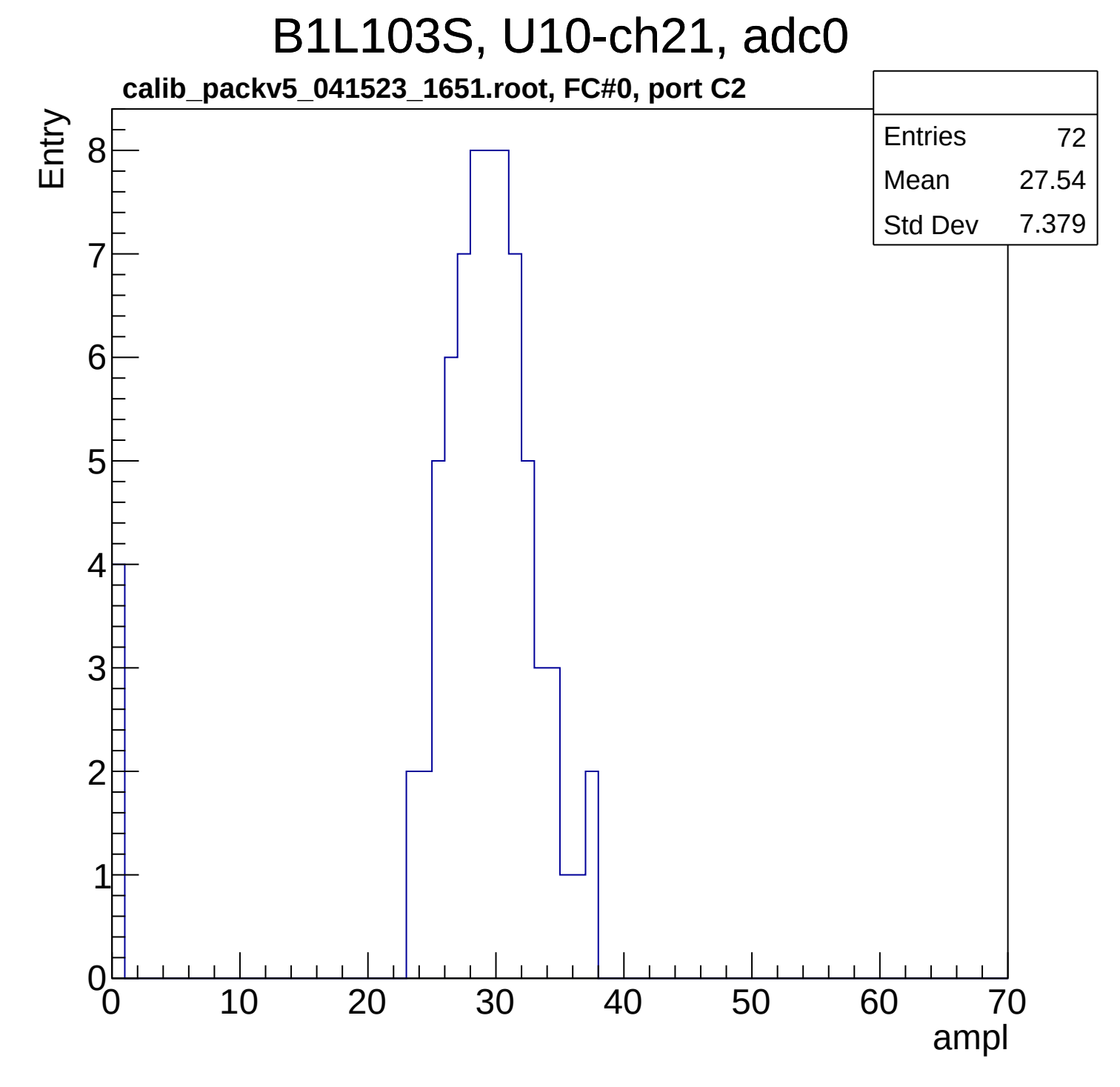
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U10-ch20, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 4
Mean 46
Std Dev 26.6
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70


B1L103S, U10-ch20, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch21, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 27.54
Std Dev 7.379
Entry
ampl
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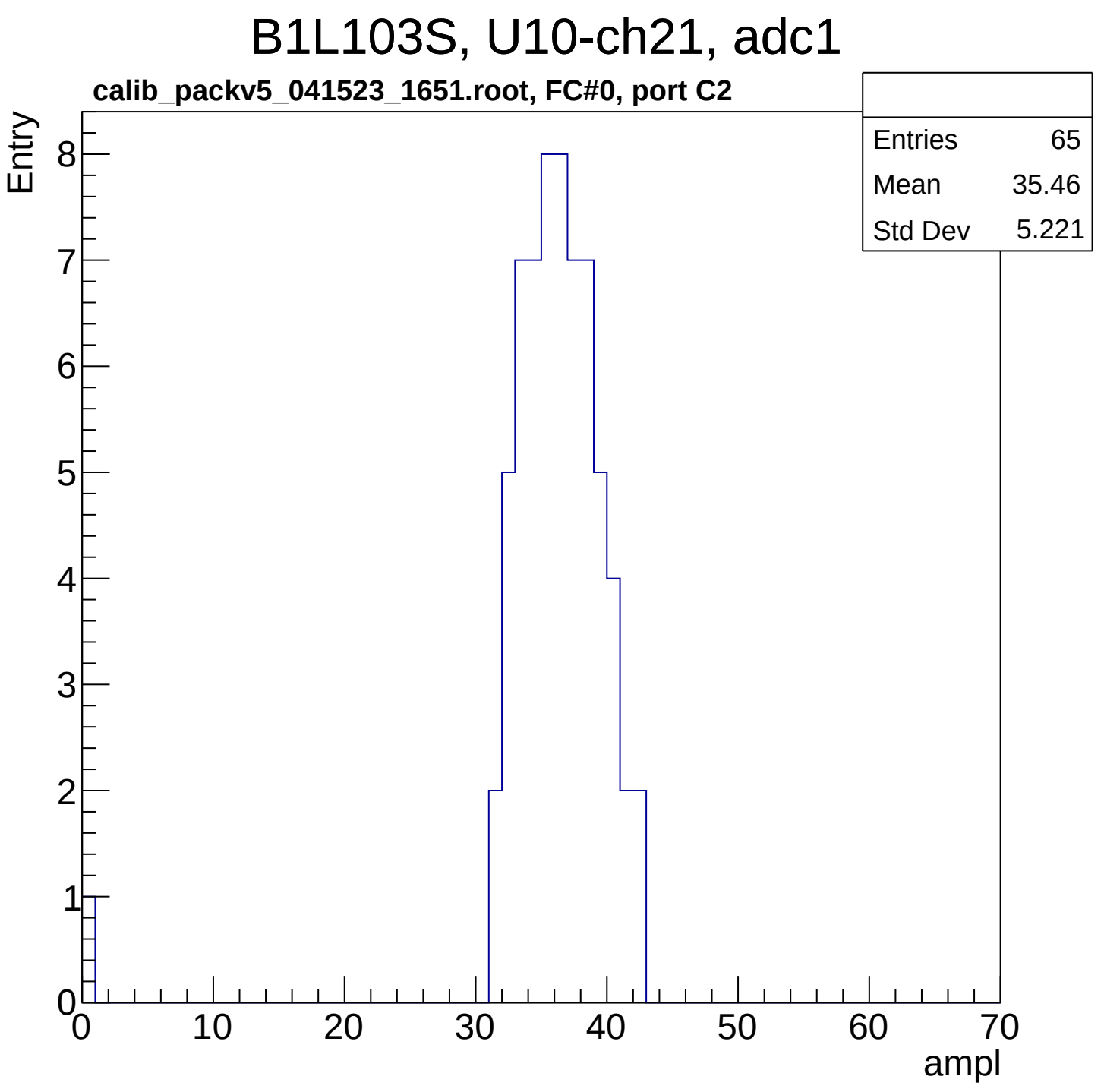
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U10-ch21, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 35.46
Std Dev 5.221
Entry
ampl
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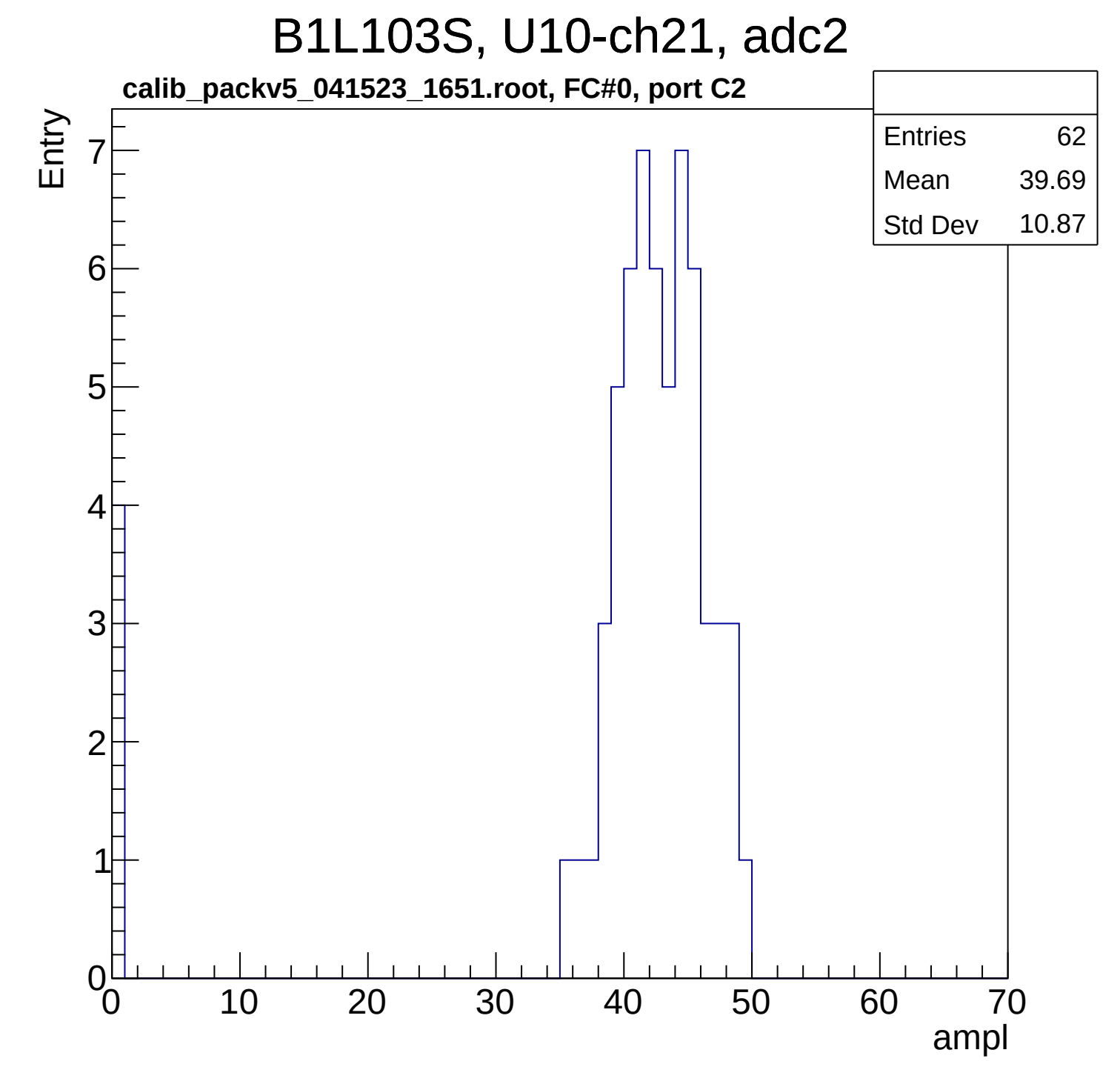
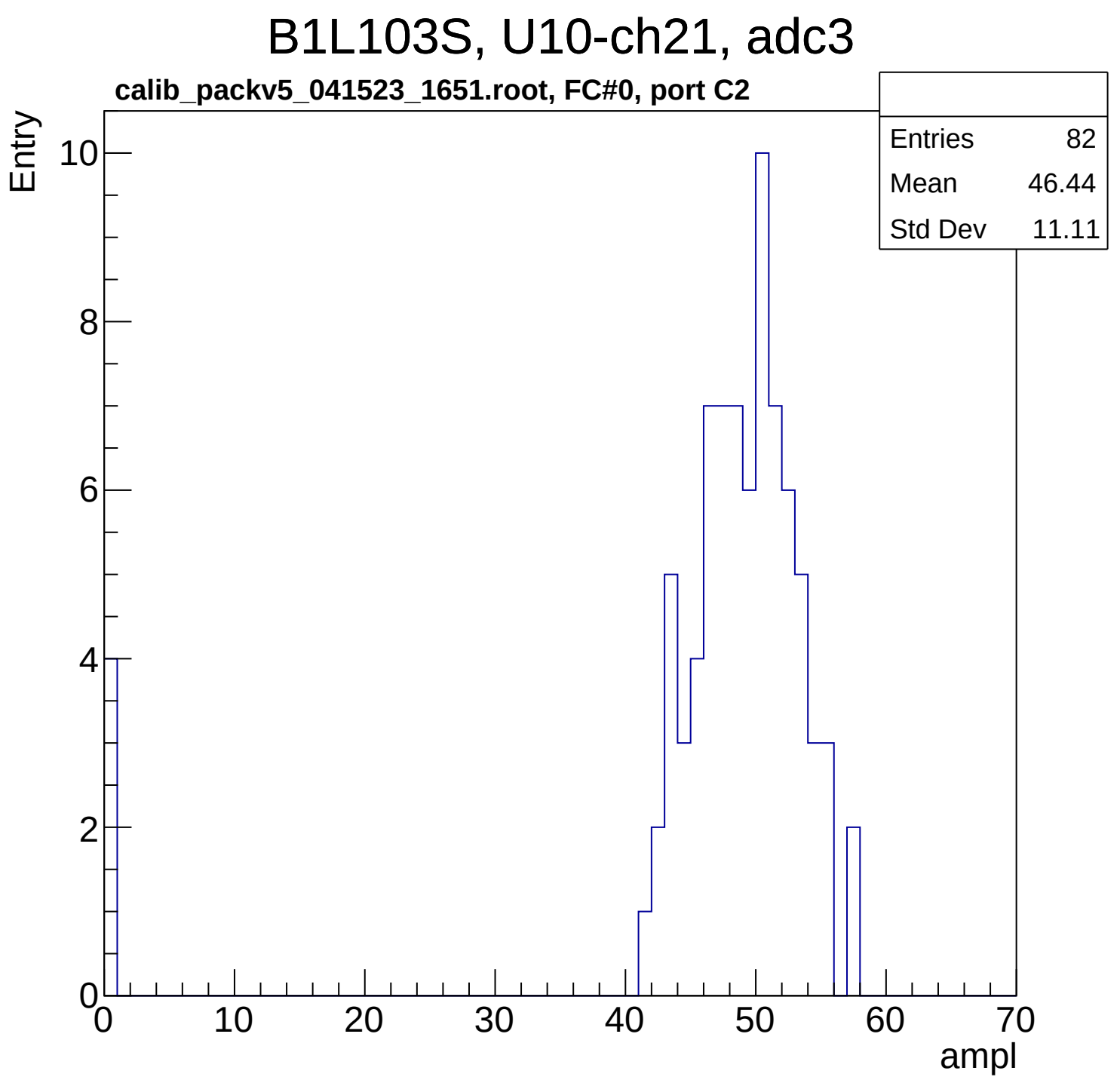
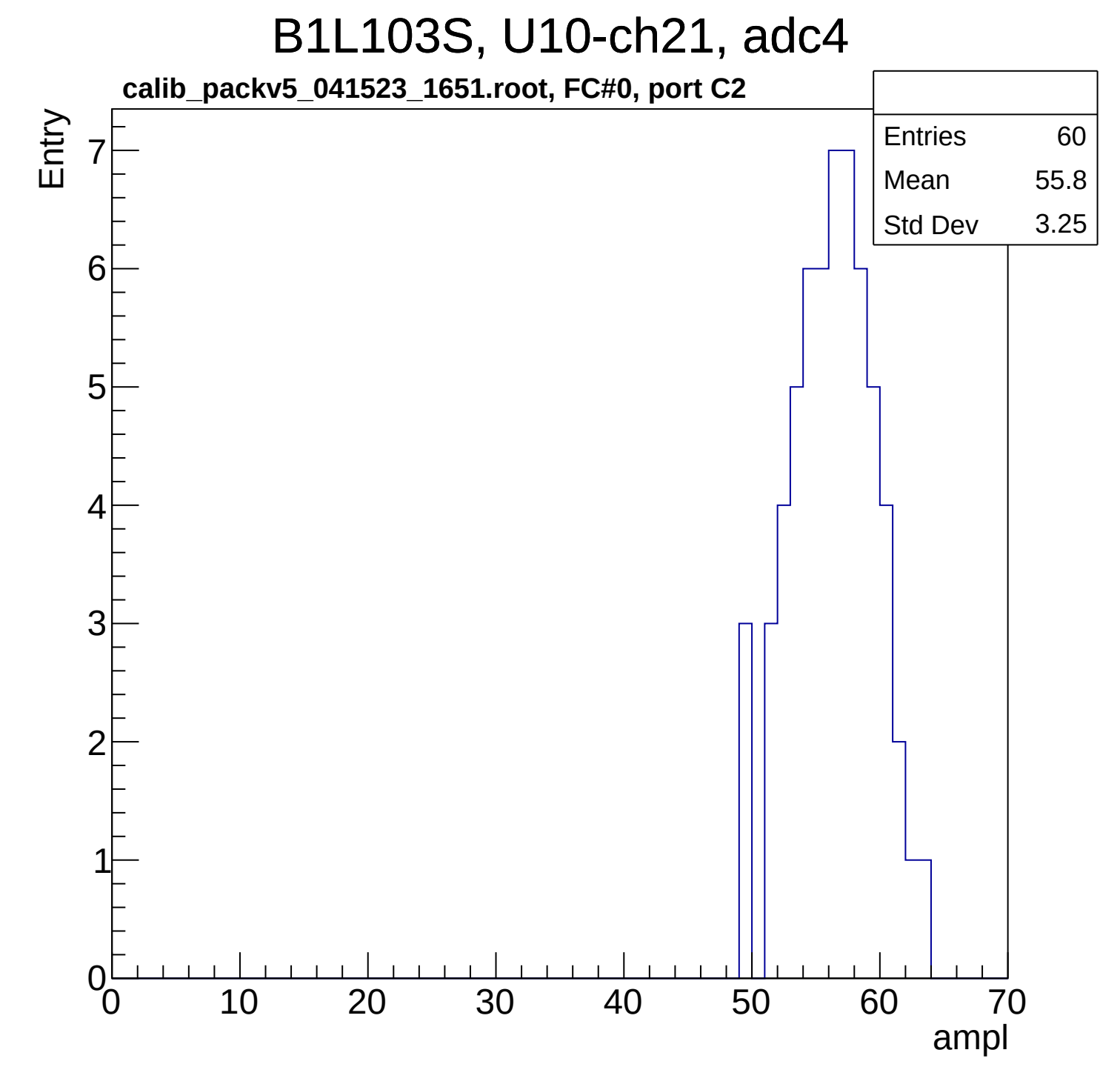
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U10-ch21, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 39.69
Std Dev 10.87
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U10-ch21, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 46.44
Std Dev 11.11
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U10-ch21, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 55.8
Std Dev 3.25
Entry
ampl
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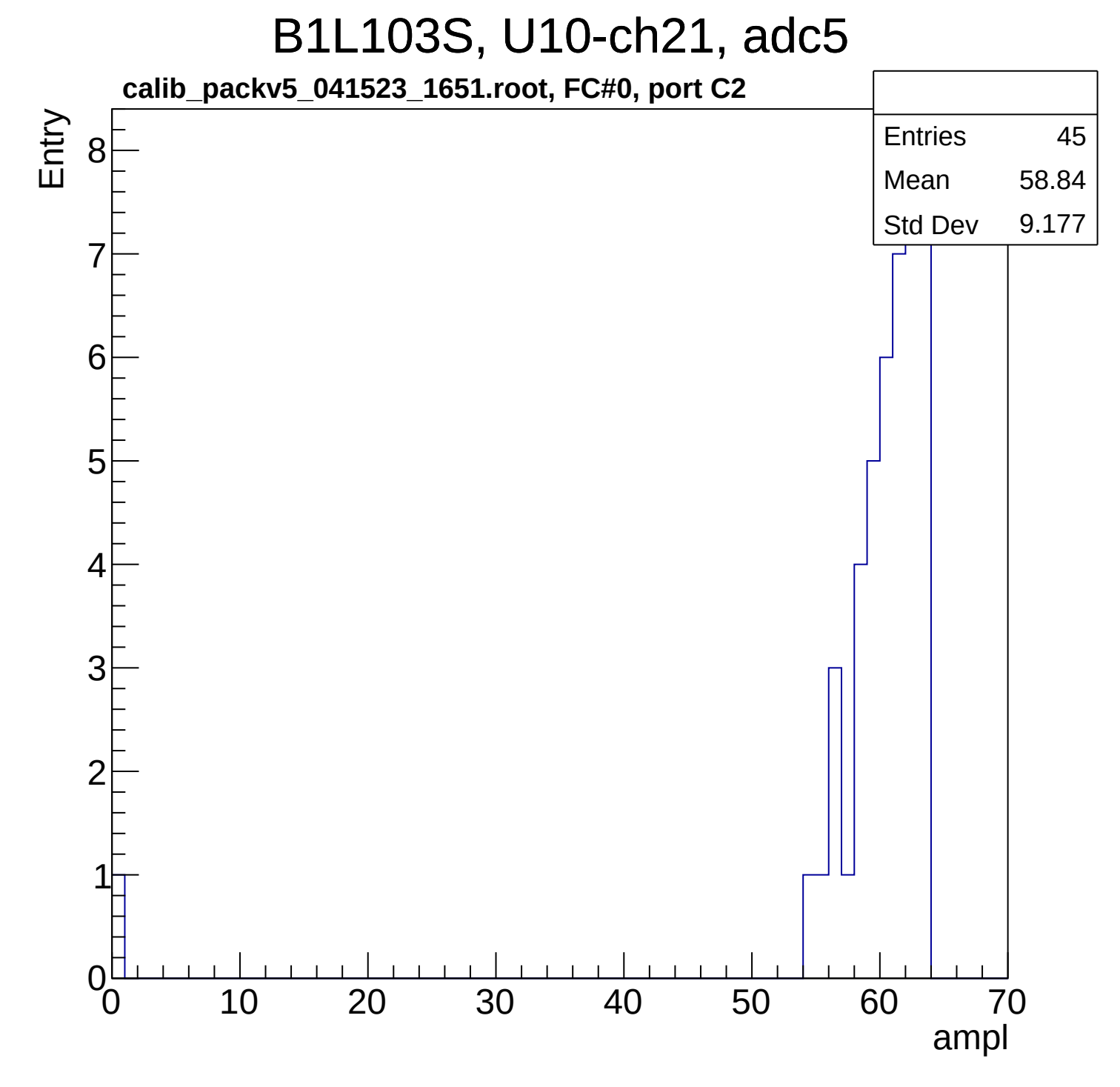
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U10-ch21, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 58.84
Std Dev 9.177
Entry
ampl
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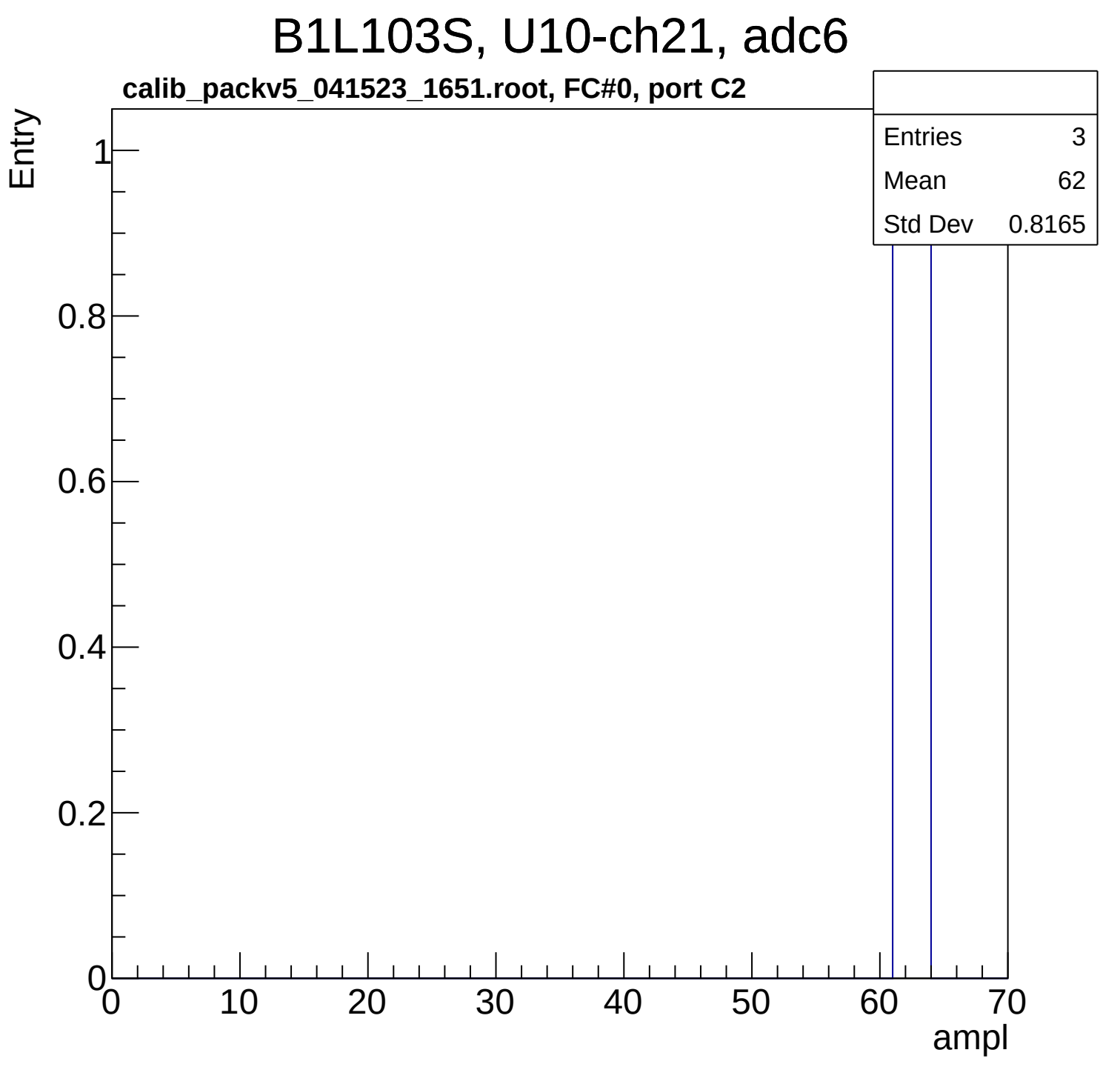
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U10-ch21, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 3
Mean 62
Std Dev 0.8165
Entry
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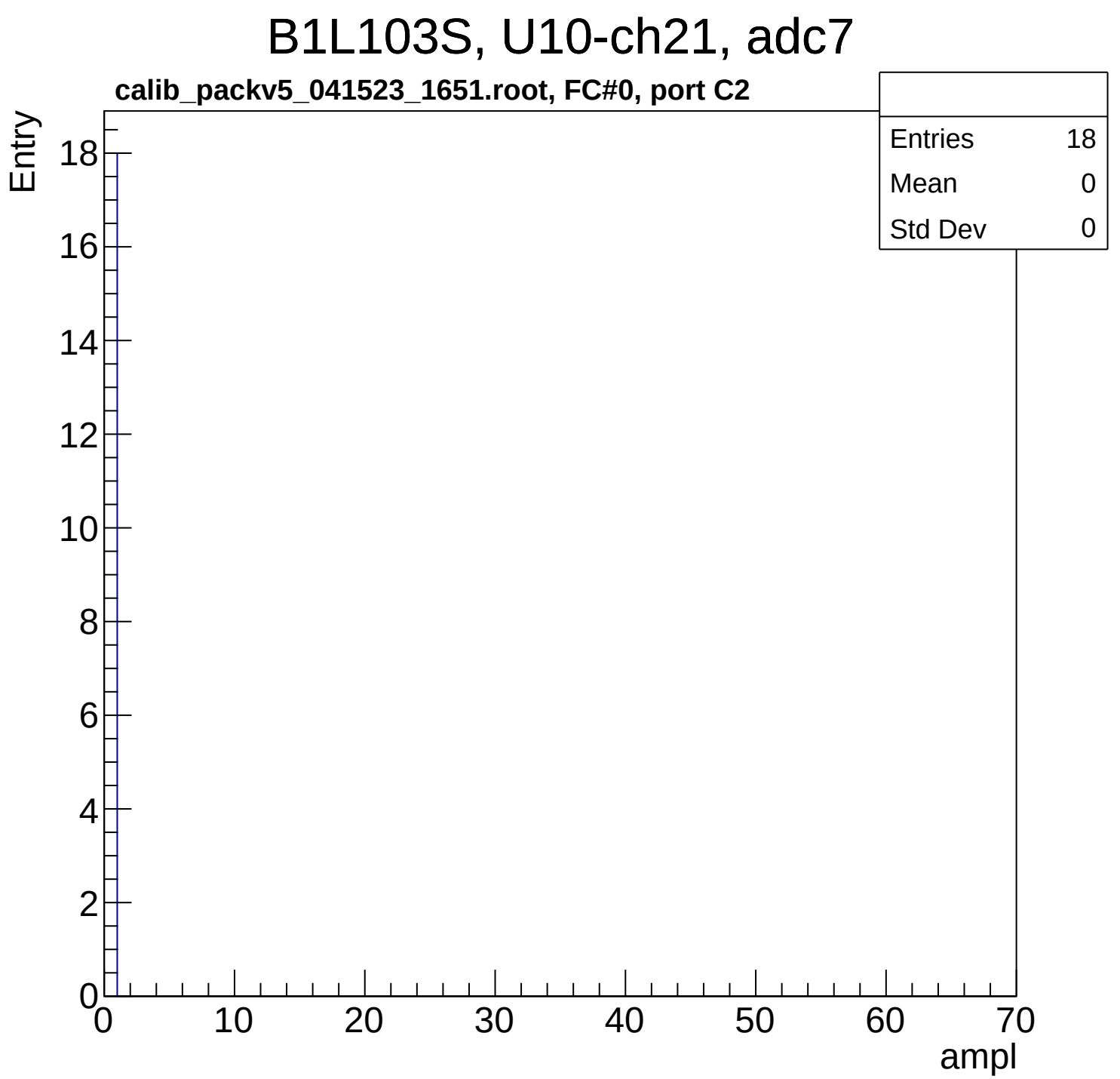
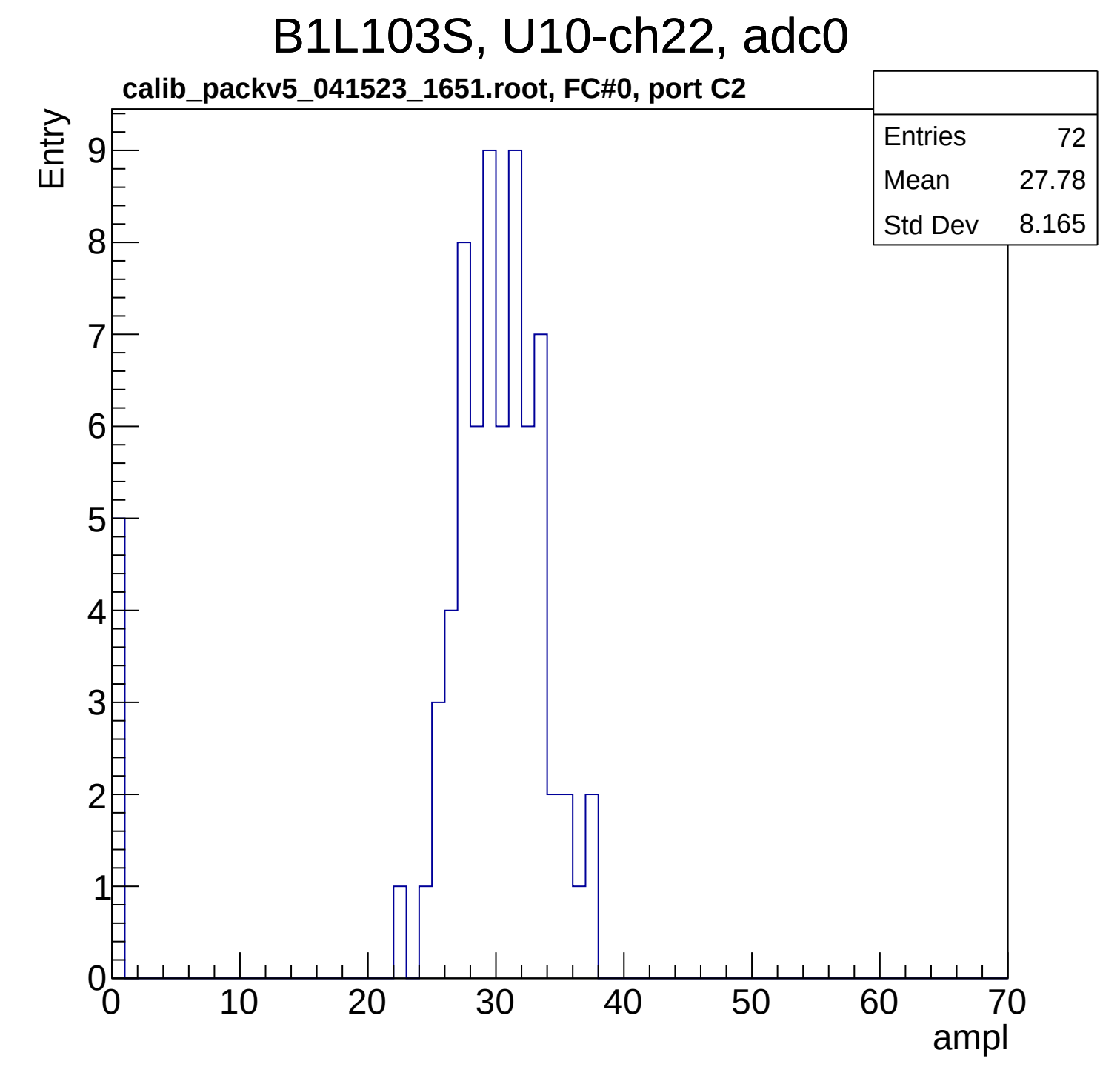
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch21, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch22, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 27.78
Std Dev 8.165
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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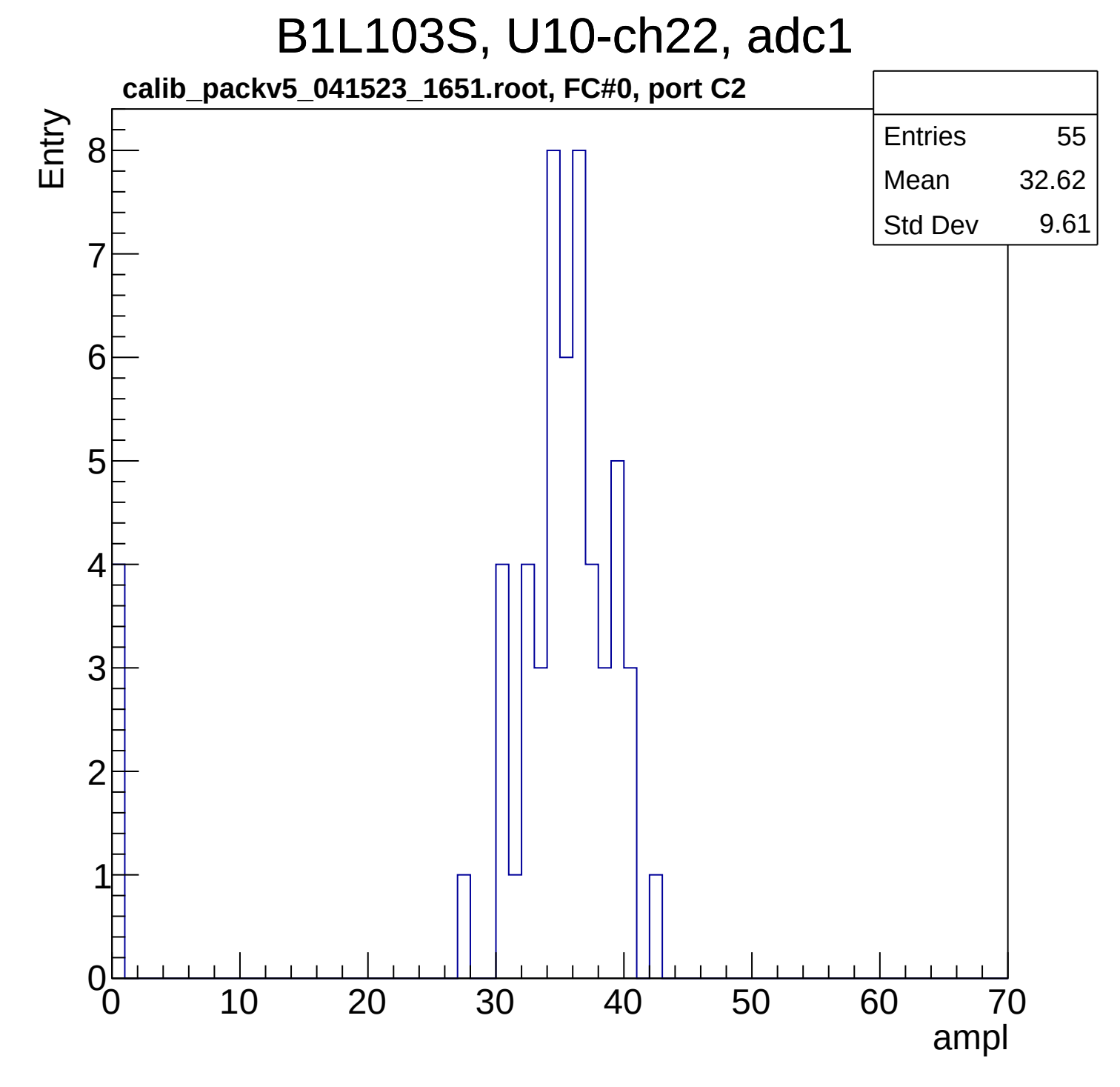
B1L103S, U10-ch22, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 32.62
Std Dev 9.61
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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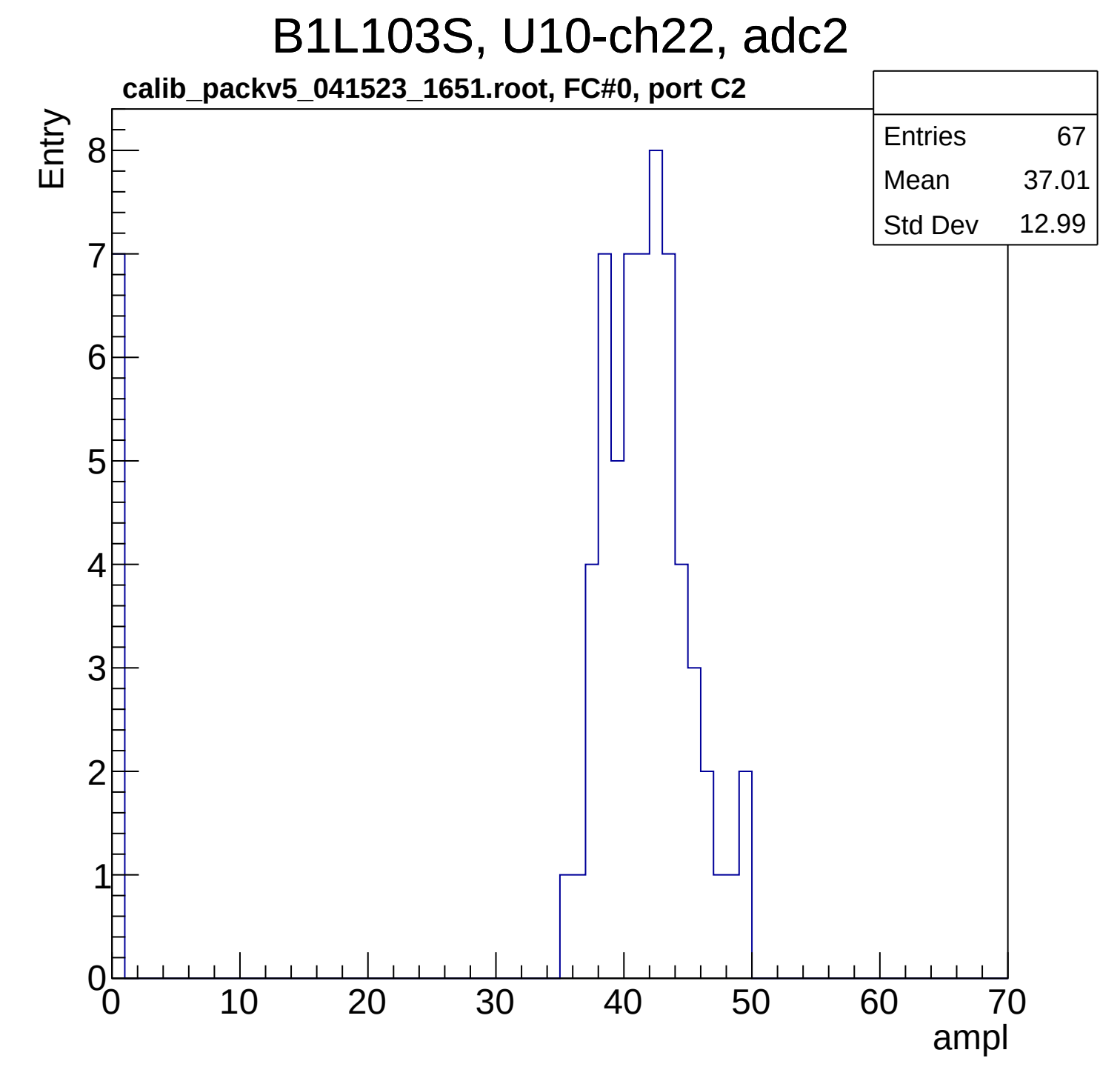
40
50
60
70


B1L103S, U10-ch22, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 37.01
Std Dev 12.99
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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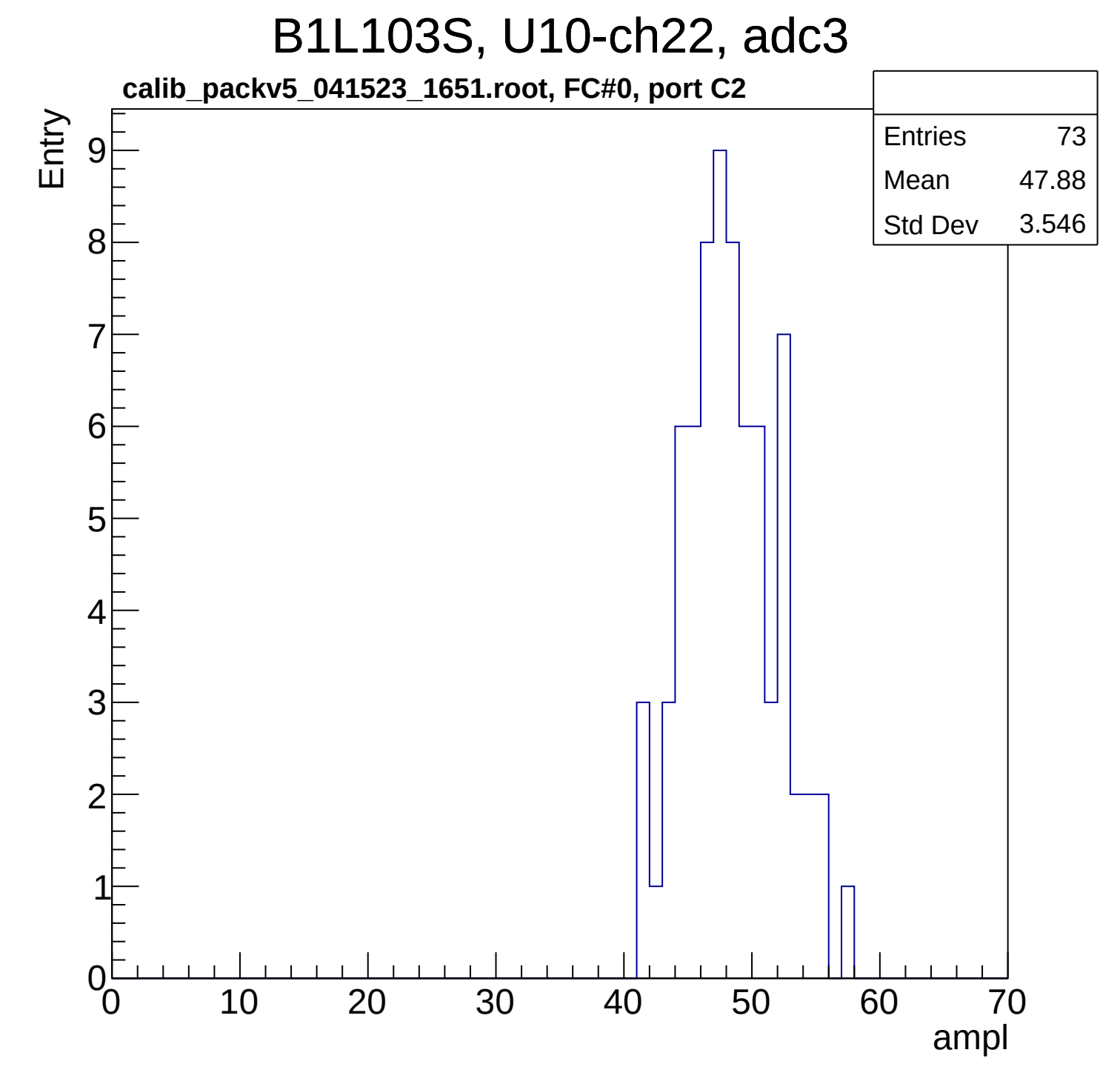
B1L103S, U10-ch22, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 47.88
Std Dev 3.546
Entry
ampl
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3
4
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7
8
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0
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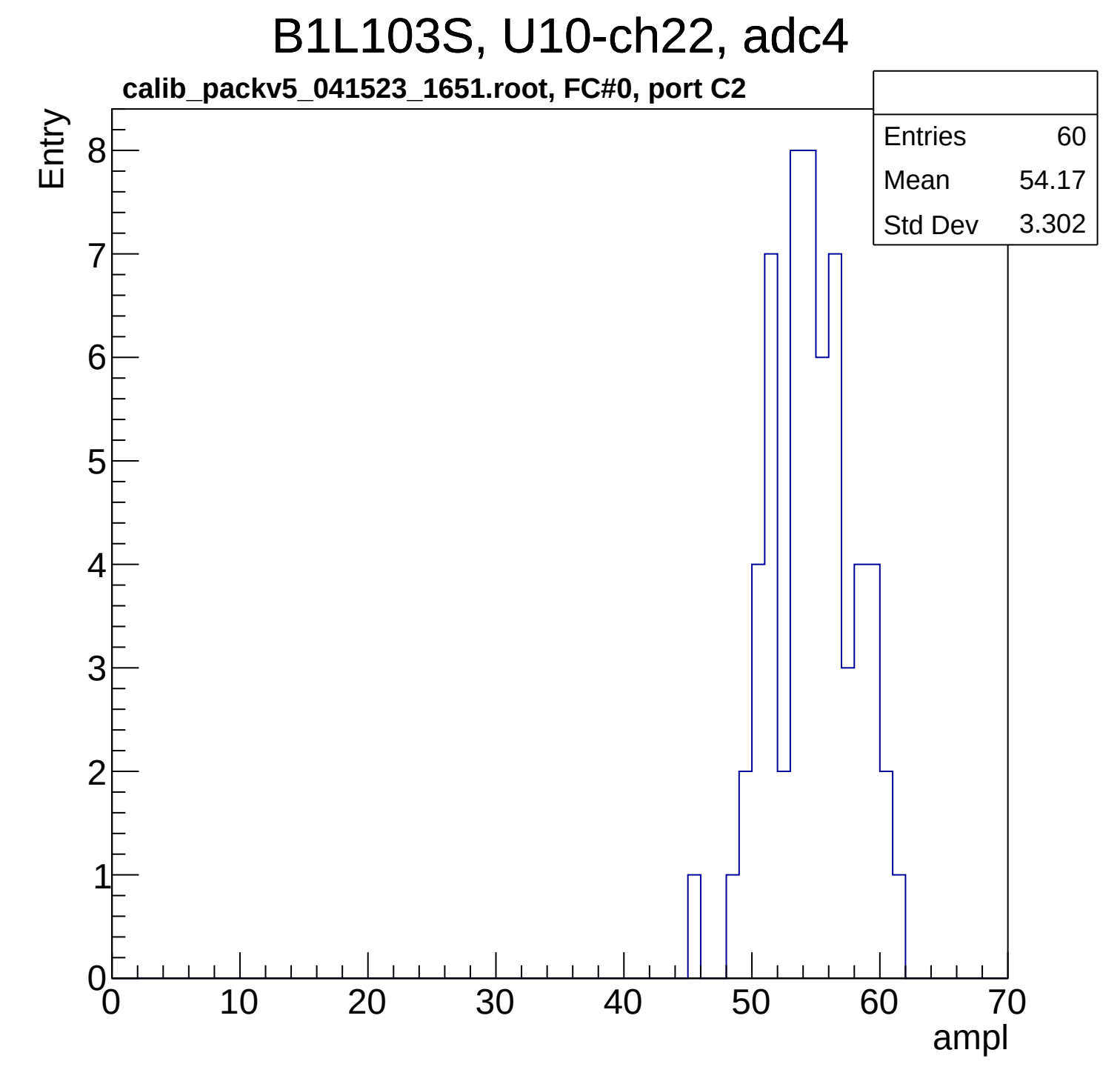
B1L103S, U10-ch22, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 54.17
Std Dev 3.302
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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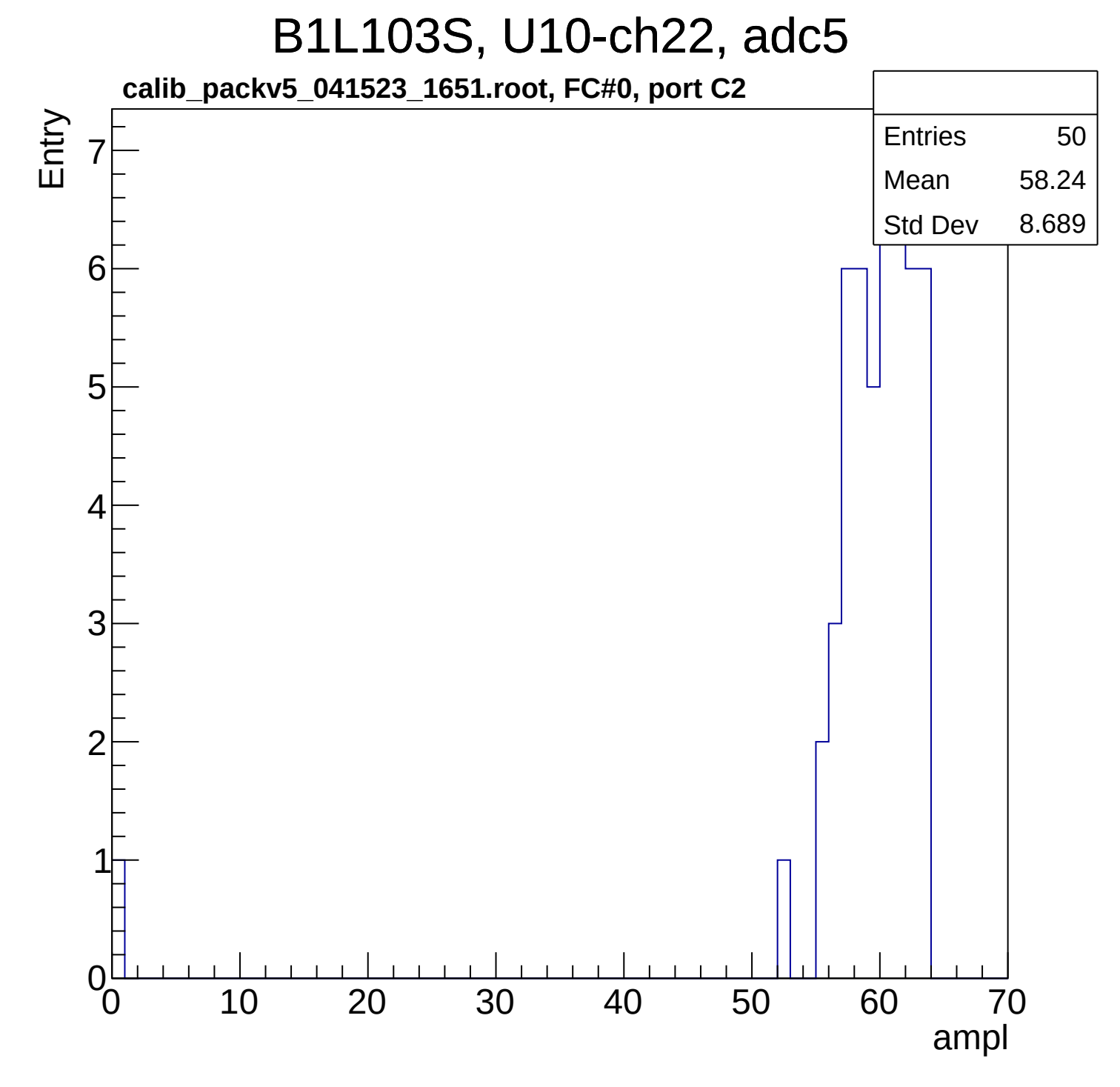
B1L103S, U10-ch22, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 58.24
Std Dev 8.689
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
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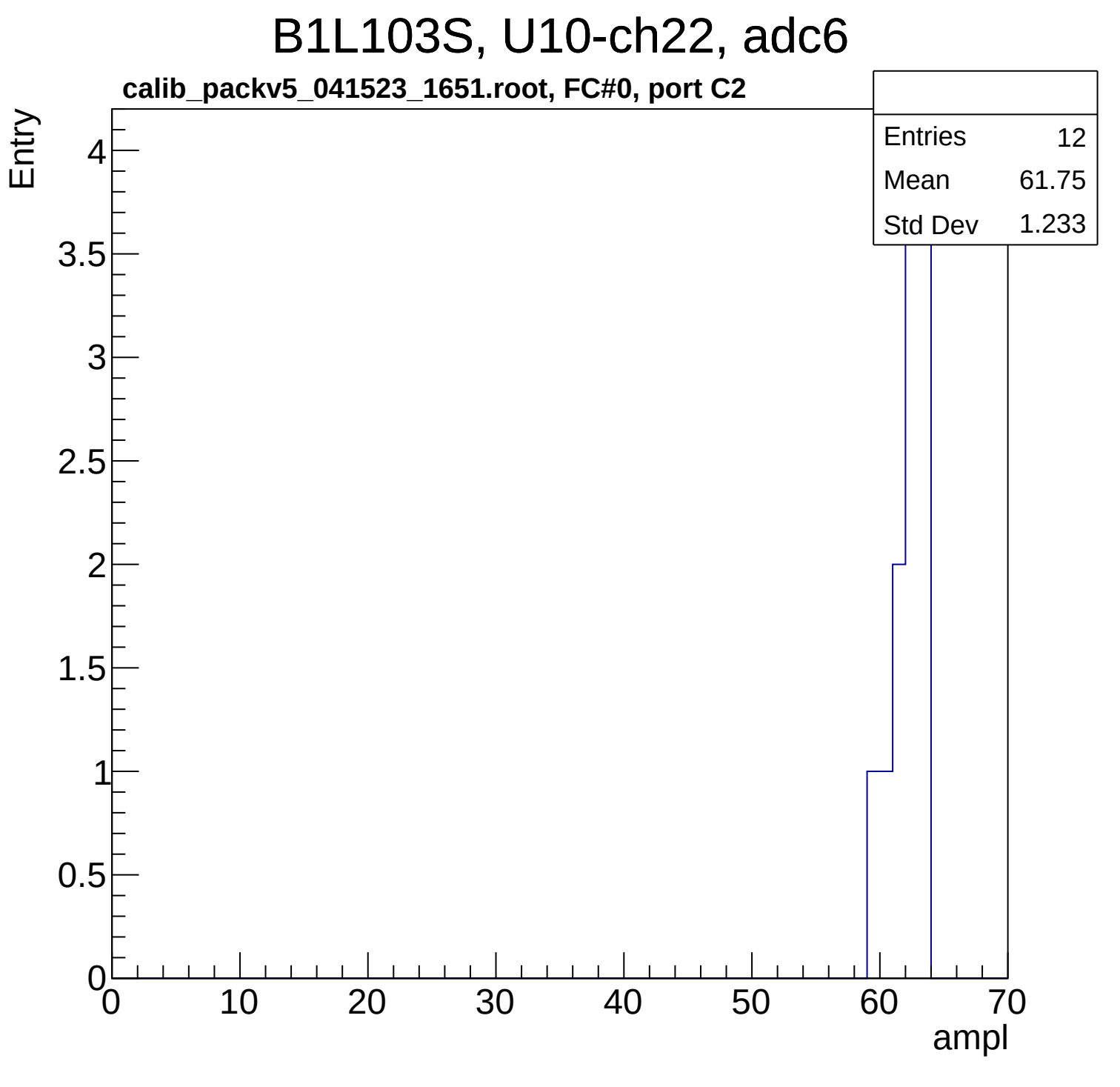
40
50
60
70


B1L103S, U10-ch22, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 61.75
Std Dev 1.233
Entry
ampl
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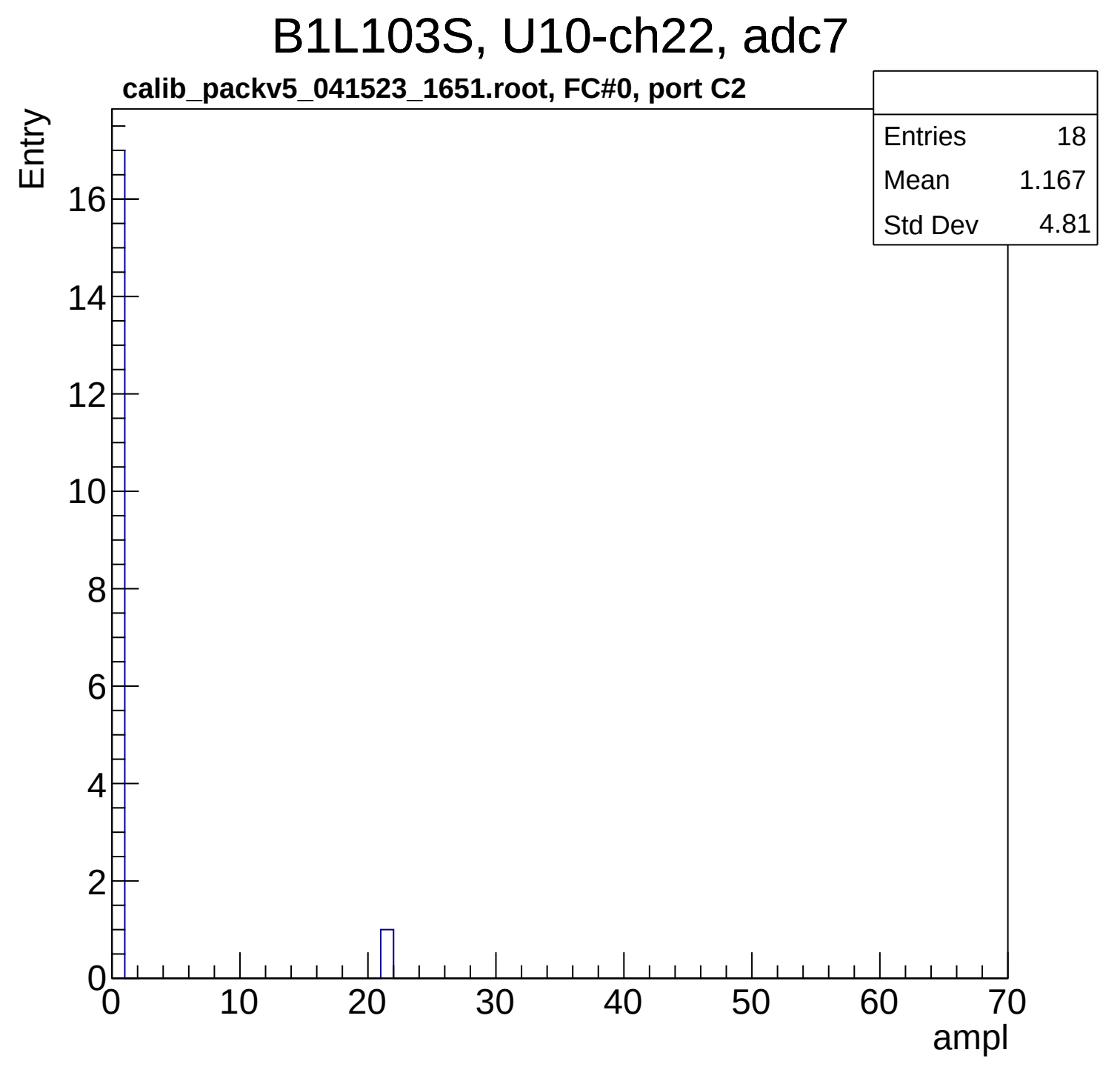
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U10-ch22, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 1.167
Std Dev 4.81
Entry
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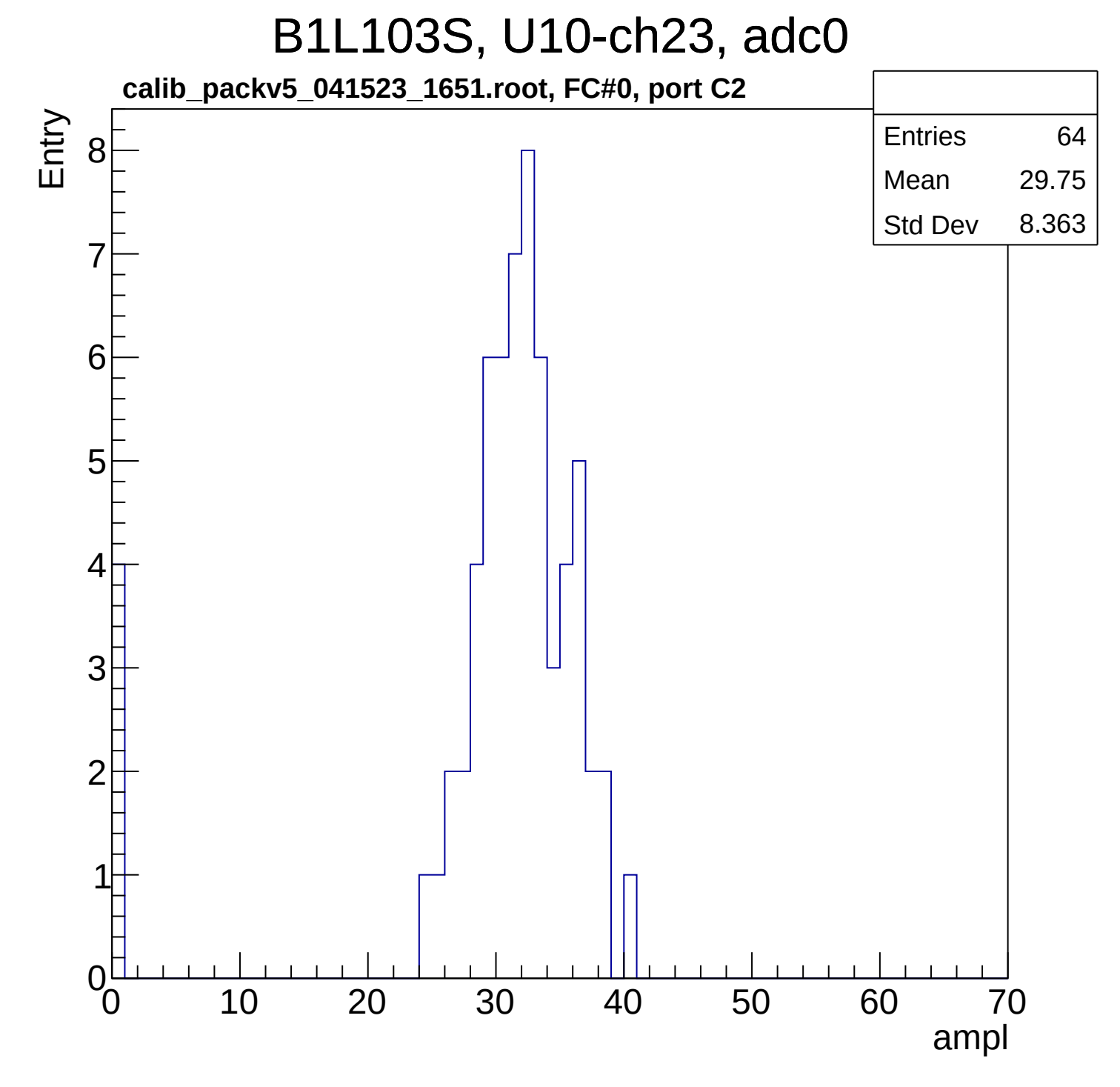
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch23, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 29.75
Std Dev 8.363
Entry
ampl
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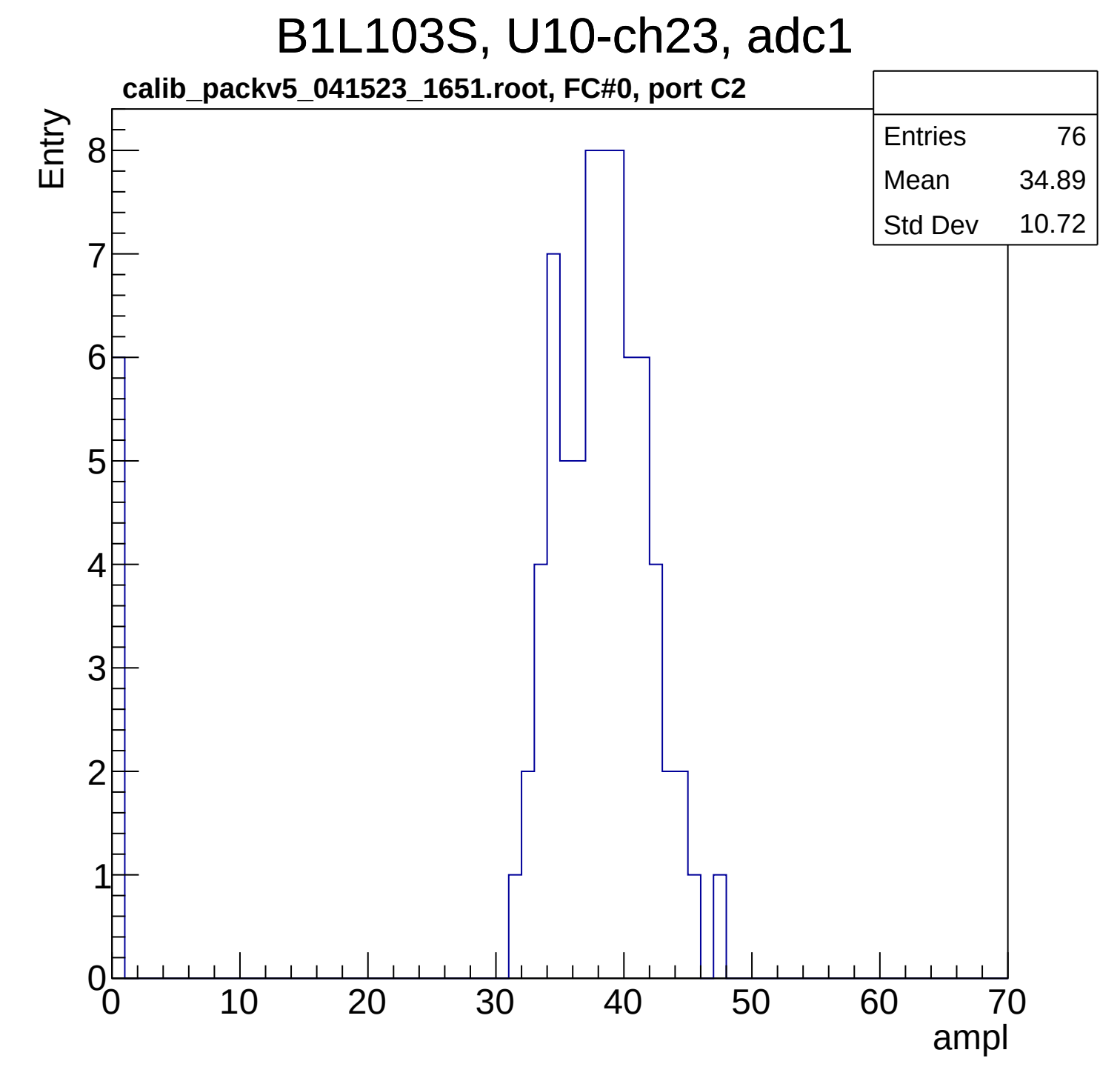
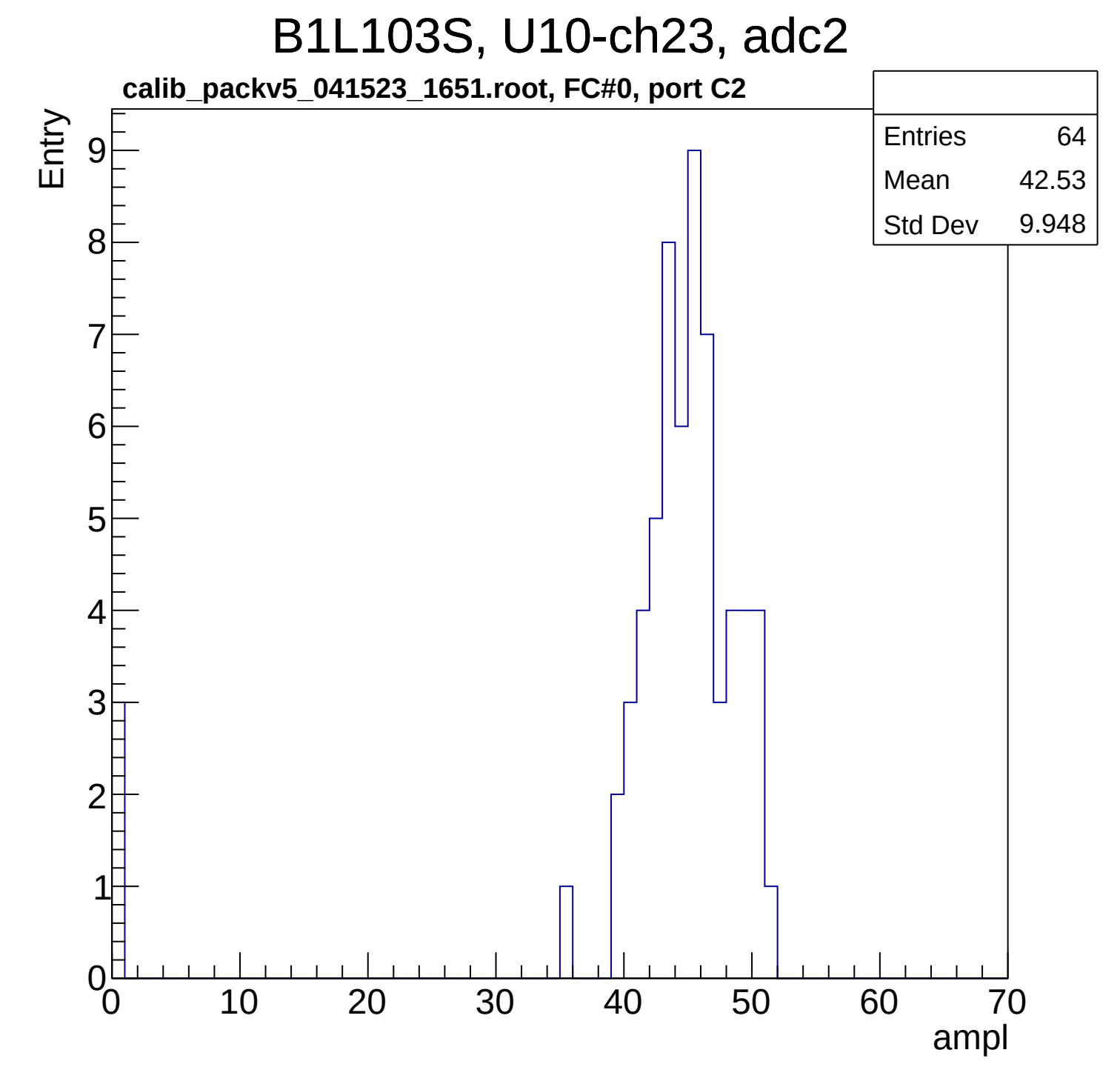
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U10-ch23, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 34.89
Std Dev 10.72
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U10-ch23, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 42.53
Std Dev 9.948
Entry
ampl
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3
4
5
6
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0
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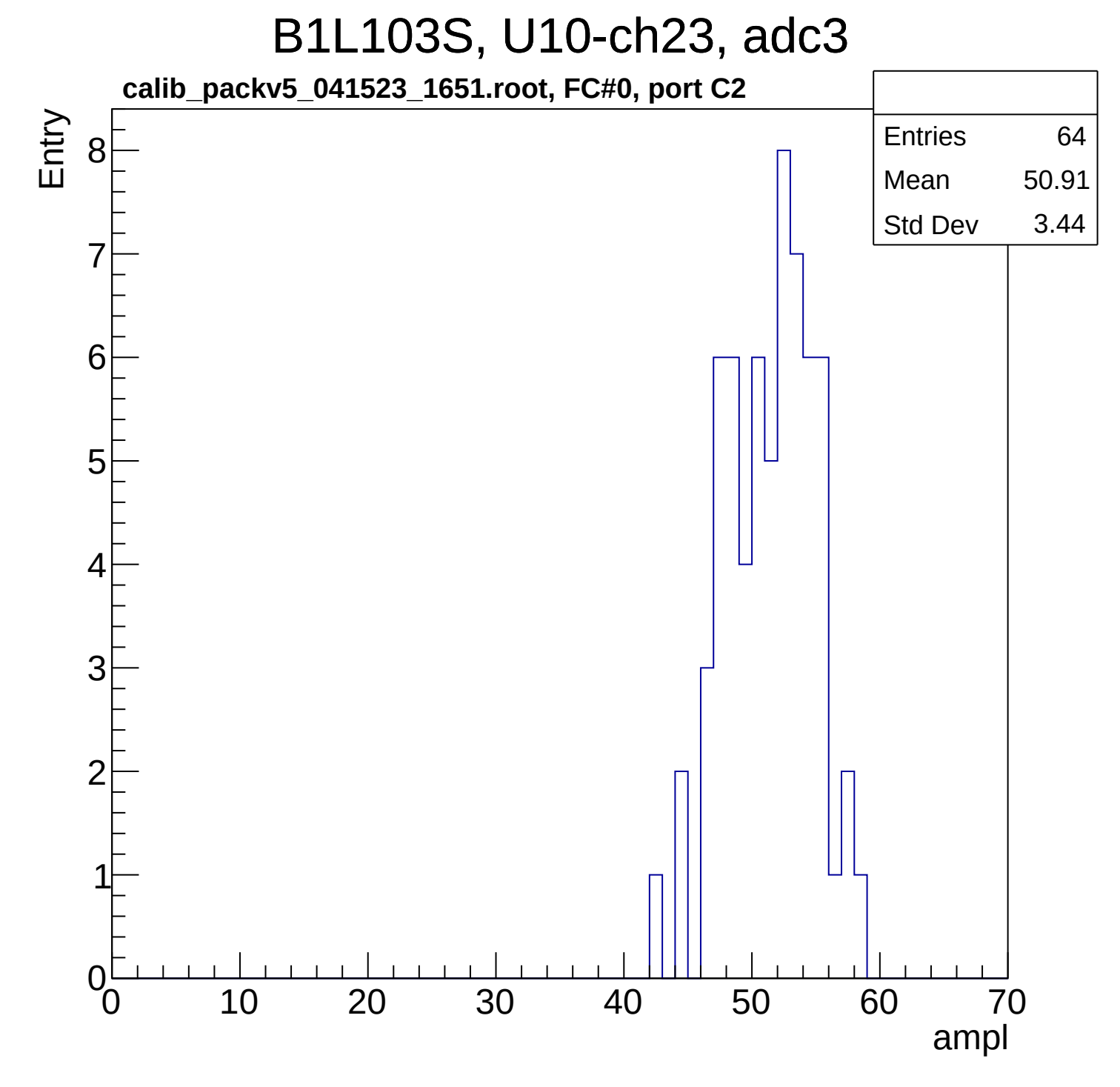
B1L103S, U10-ch23, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 50.91
Std Dev 3.44
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ampl
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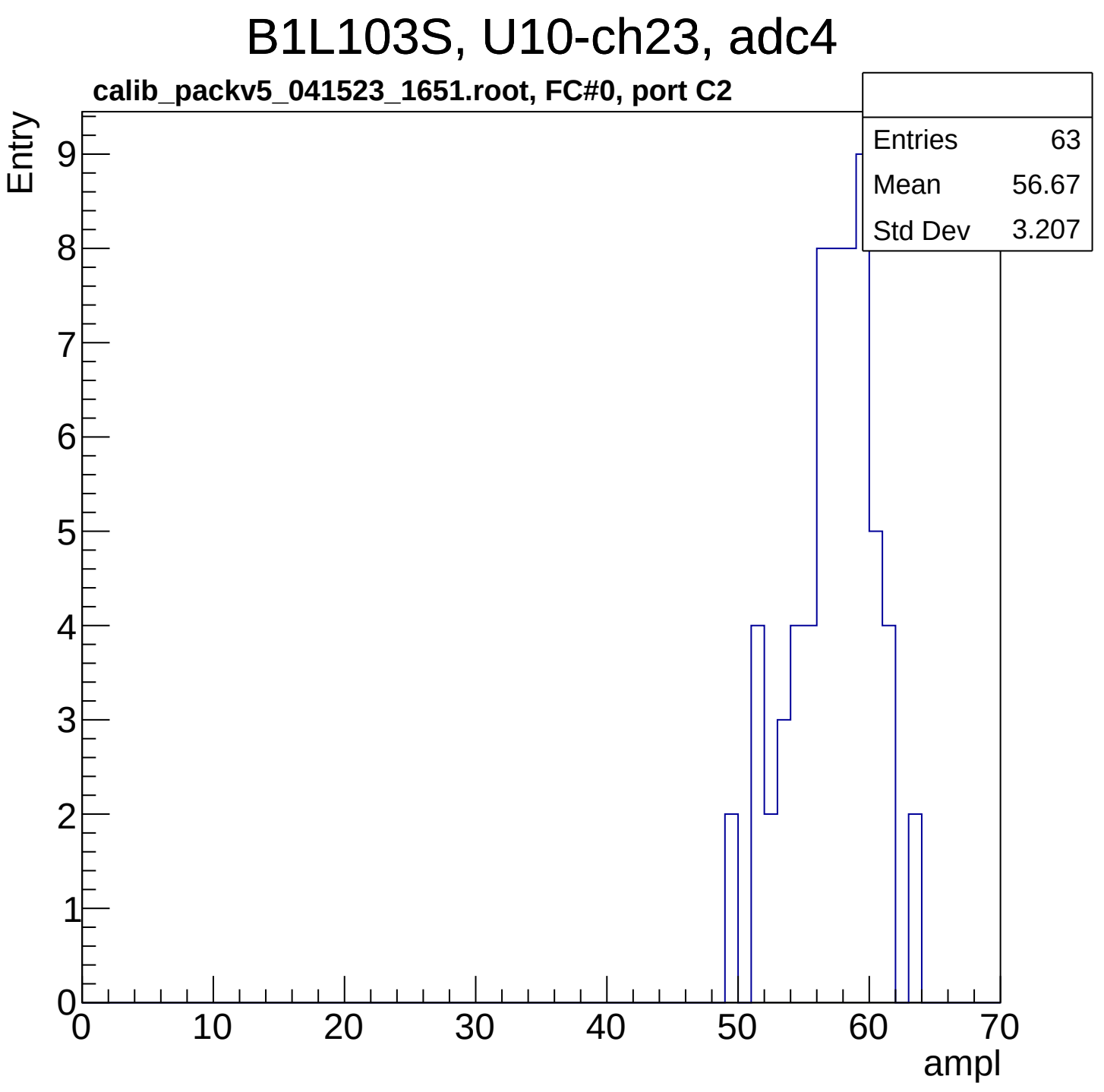
B1L103S, U10-ch23, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 56.67
Std Dev 3.207
Entry
ampl
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3
4
5
6
7
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0
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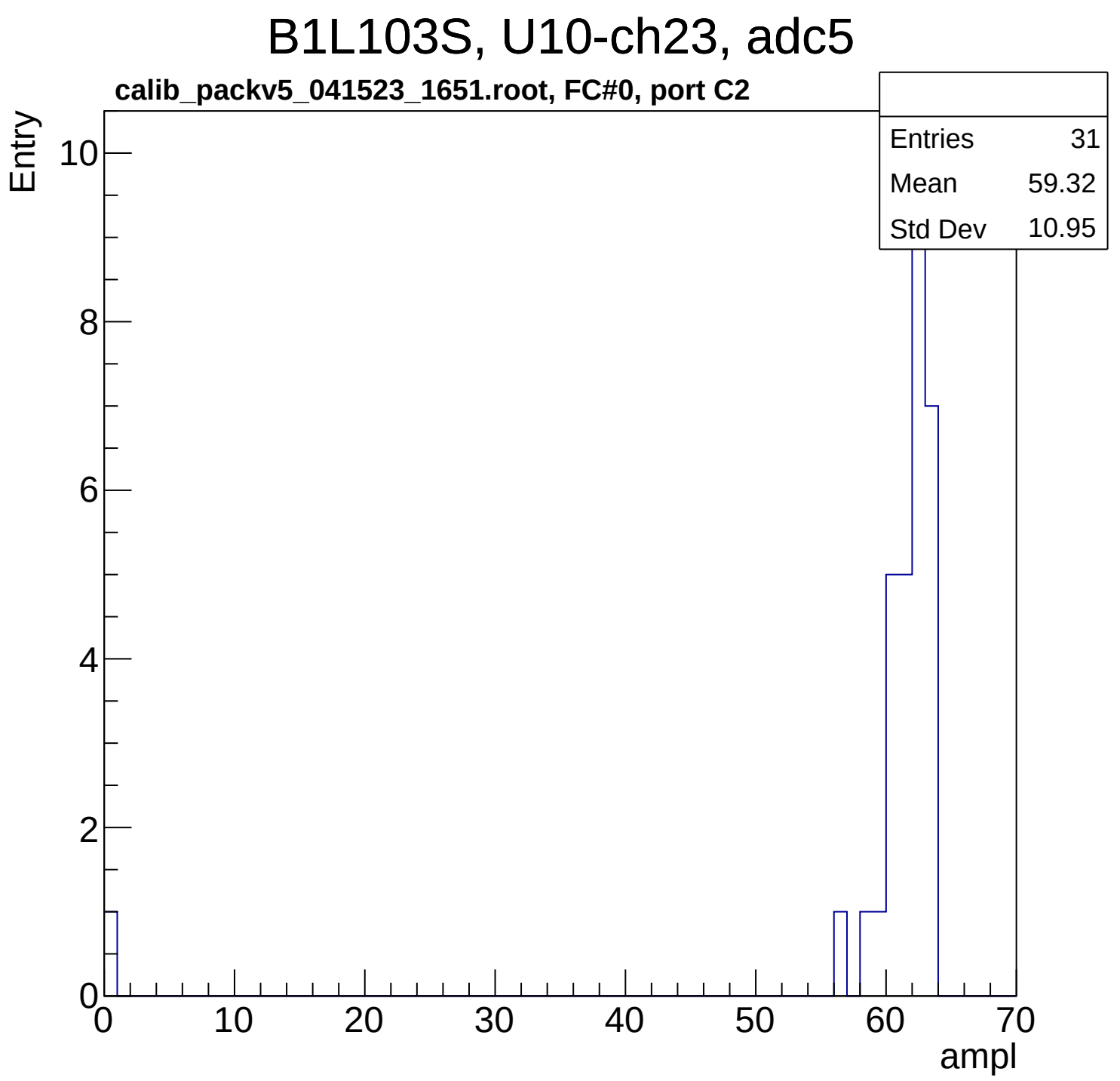
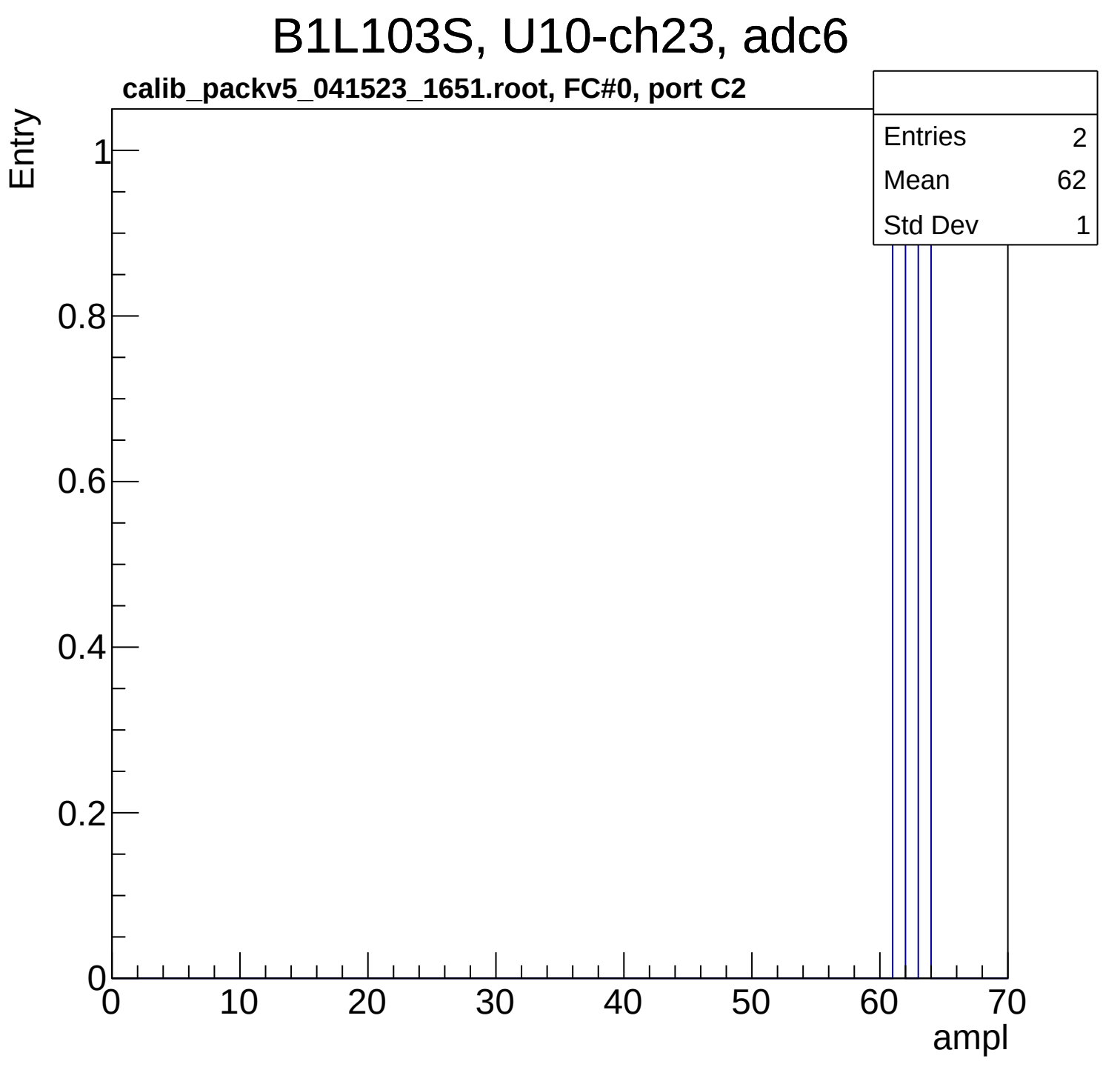

B1L103S, U10-ch23, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 31
Mean 59.32
Std Dev 10.95
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch23, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 2
Mean 62
Std Dev 1
Entry
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0.8
0.6
0.4
0.2
0
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10
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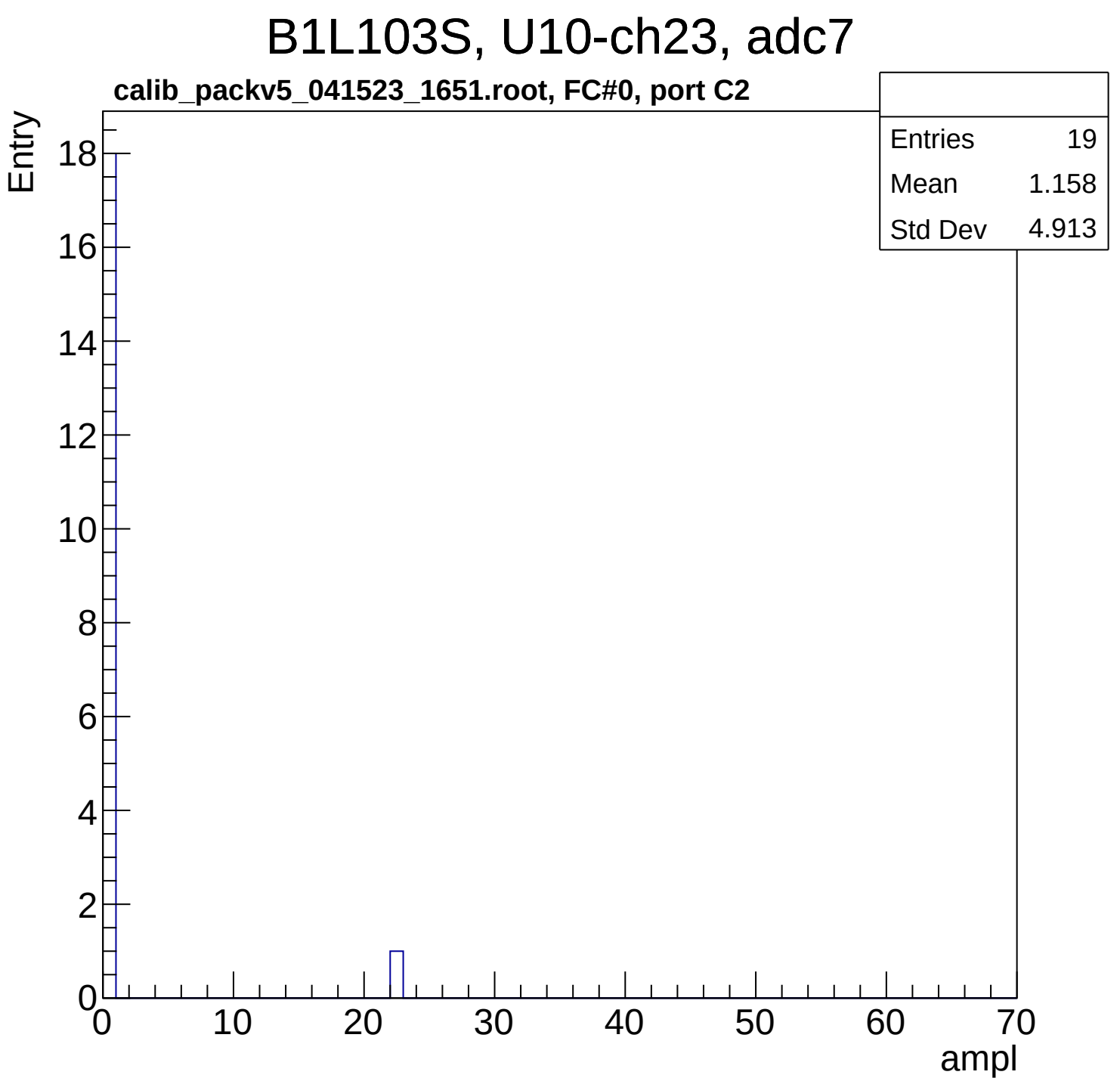
40
50
60
70
ampl


B1L103S, U10-ch23, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.158
Std Dev 4.913
Entry
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6
8
10
12
14
16
18
0
10
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30
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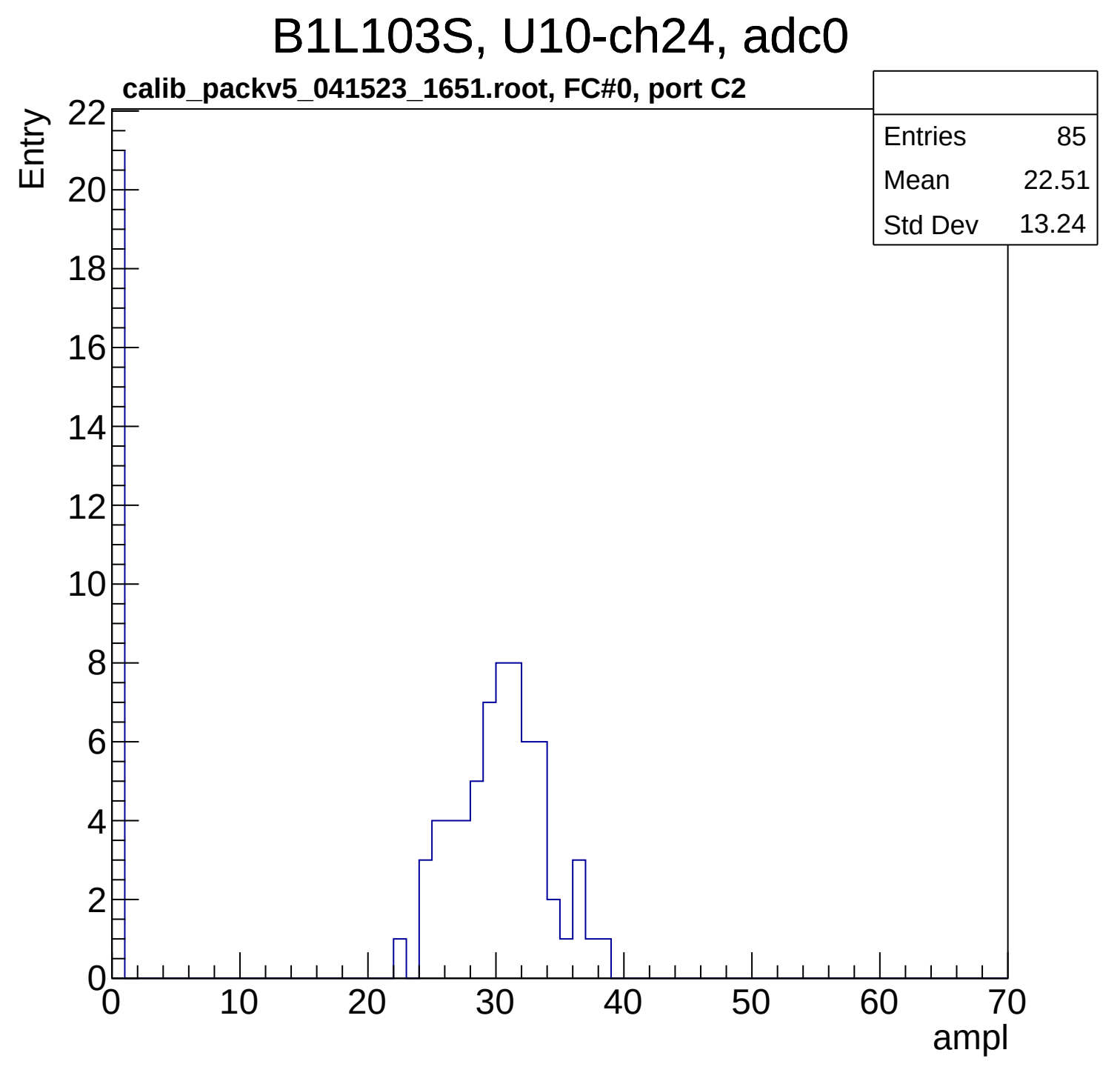
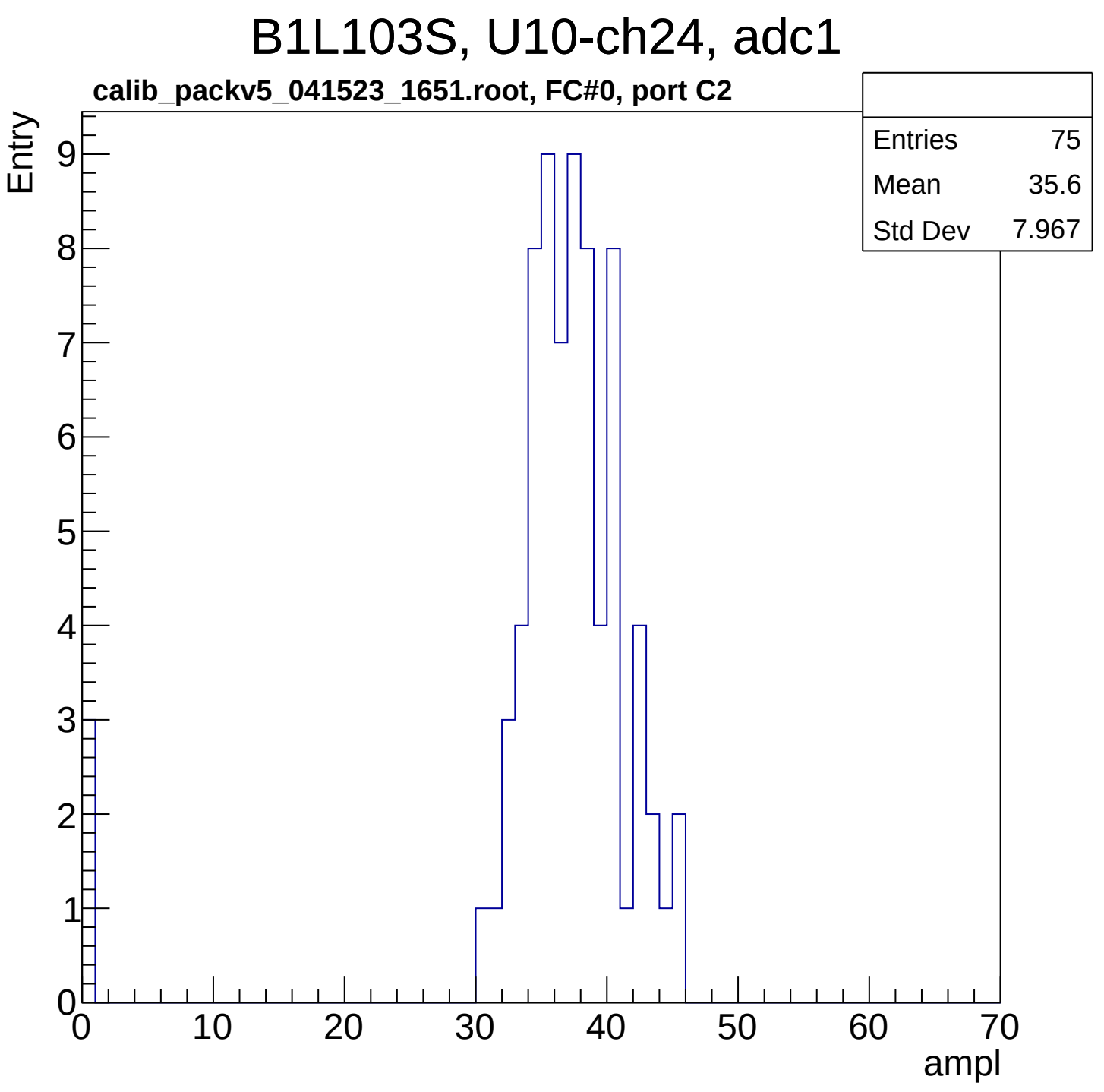
50
60
70
ampl


B1L103S, U10-ch24, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 22.51
Std Dev 13.24
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
22
0
10
20
30
40
50
60
70


B1L103S, U10-ch24, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 35.6
Std Dev 7.967
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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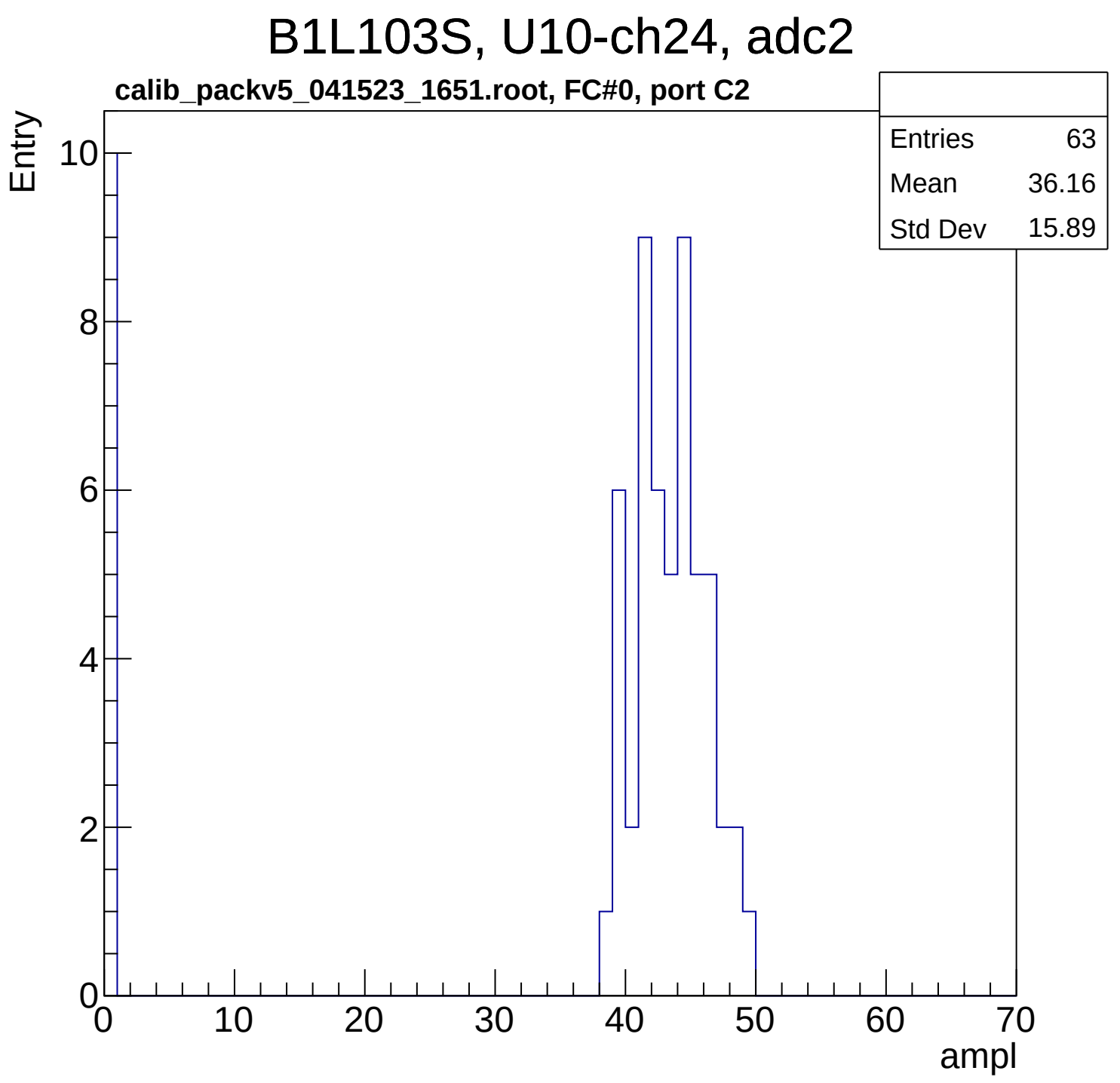
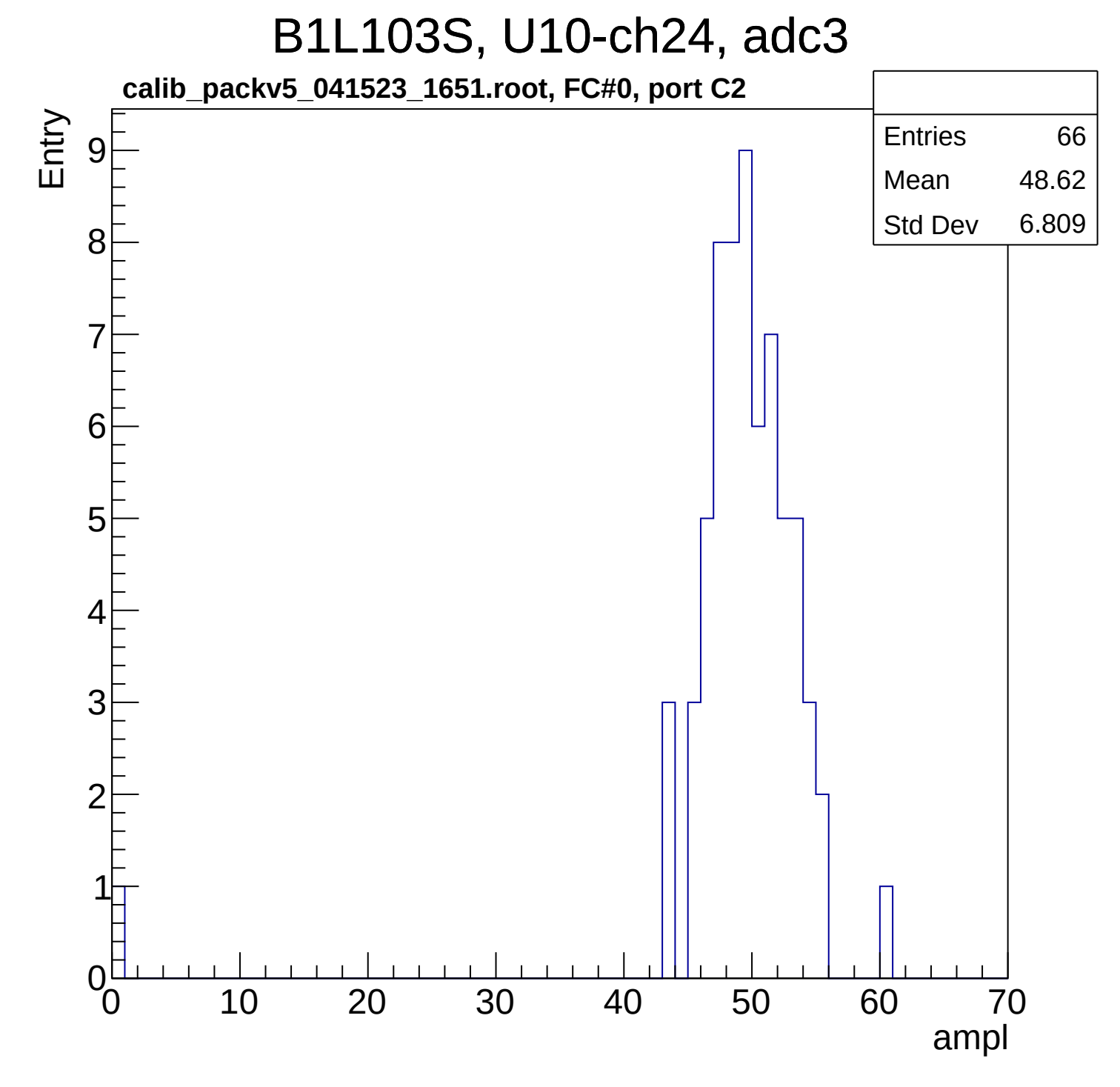
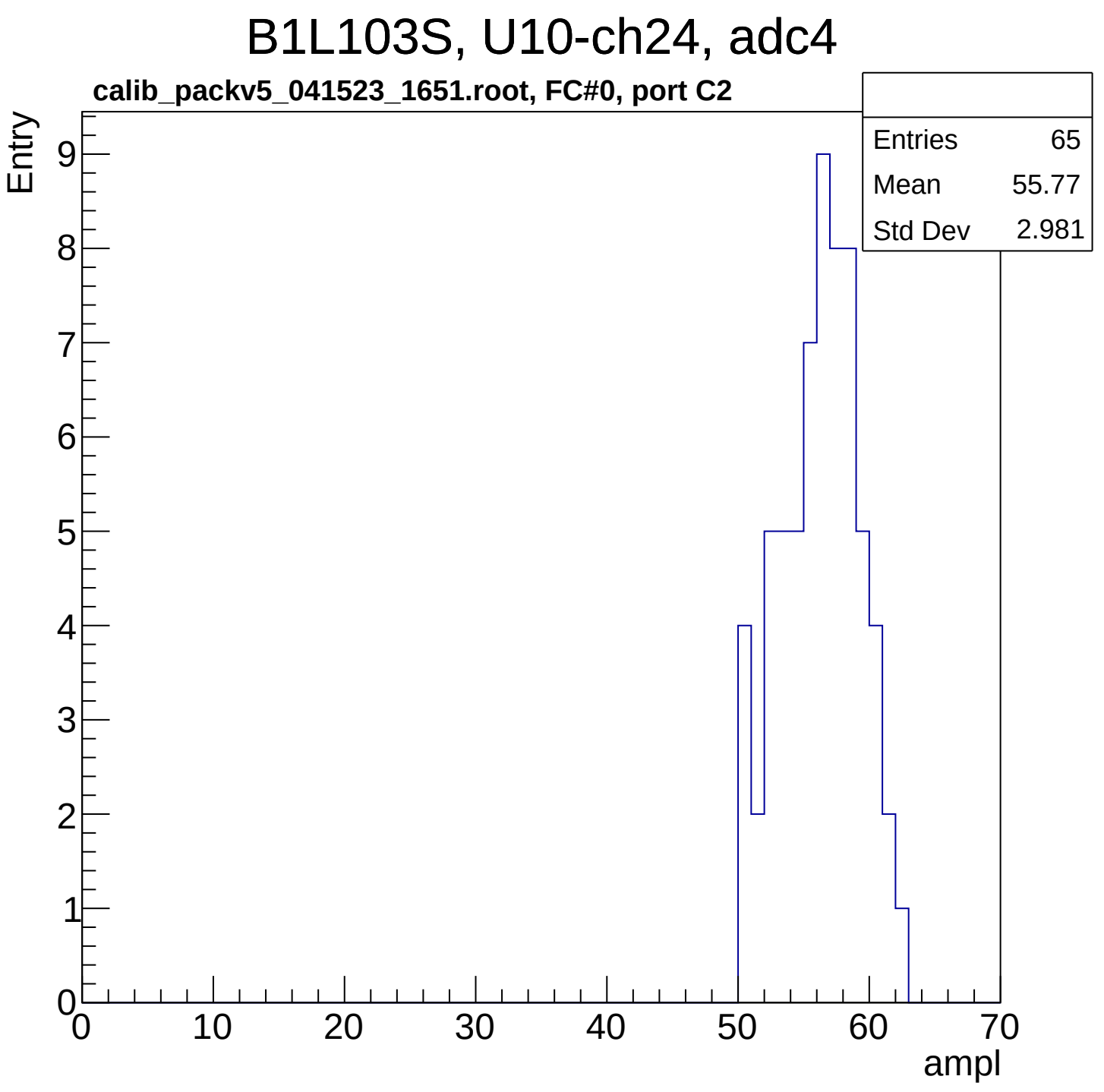

B1L103S, U10-ch24, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 36.16
Std Dev 15.89
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U10-ch24, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 48.62
Std Dev 6.809
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U10-ch24, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 55.77
Std Dev 2.981
Entry
ampl
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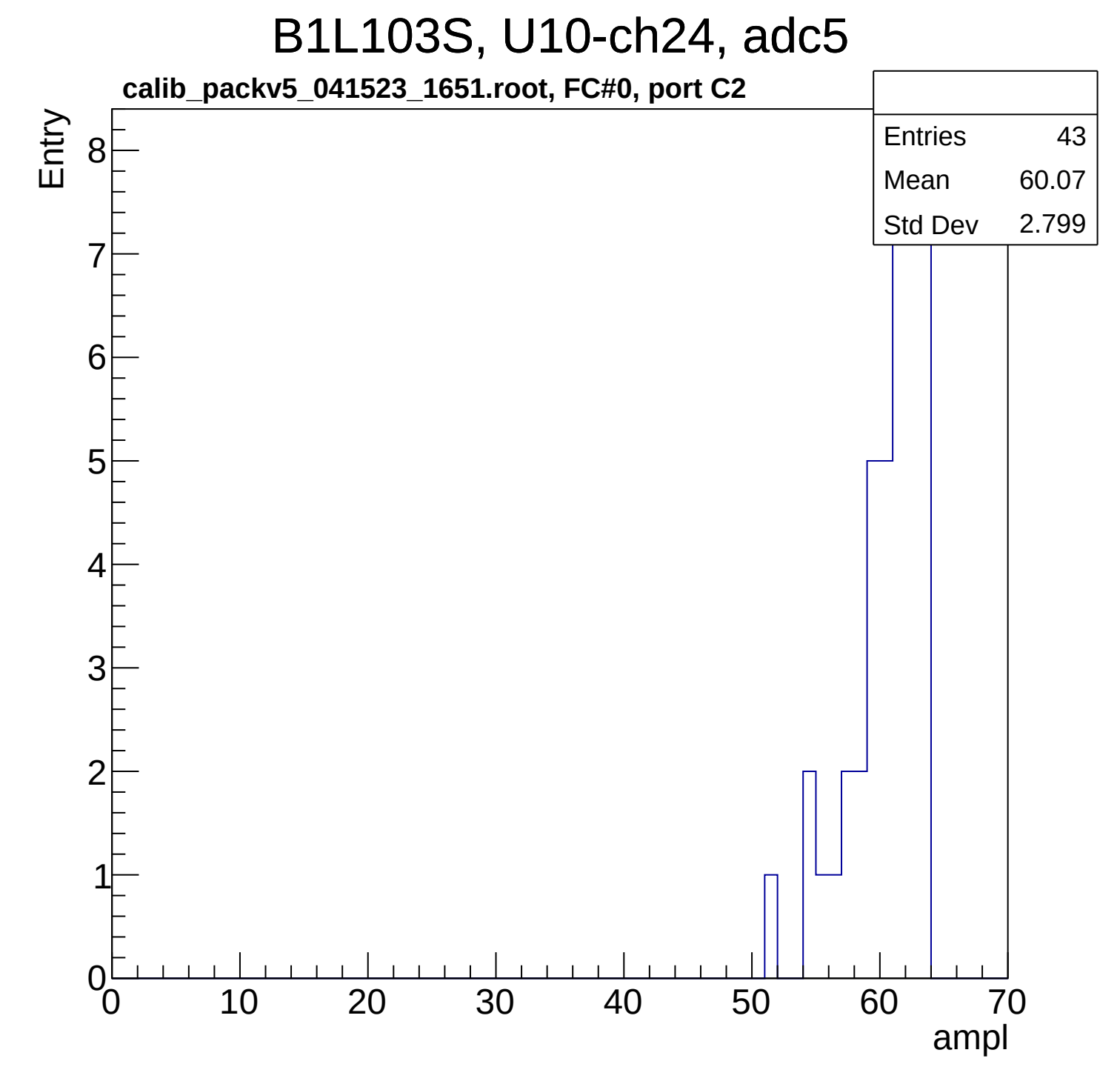
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U10-ch24, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 43
Mean 60.07
Std Dev 2.799
Entry
ampl
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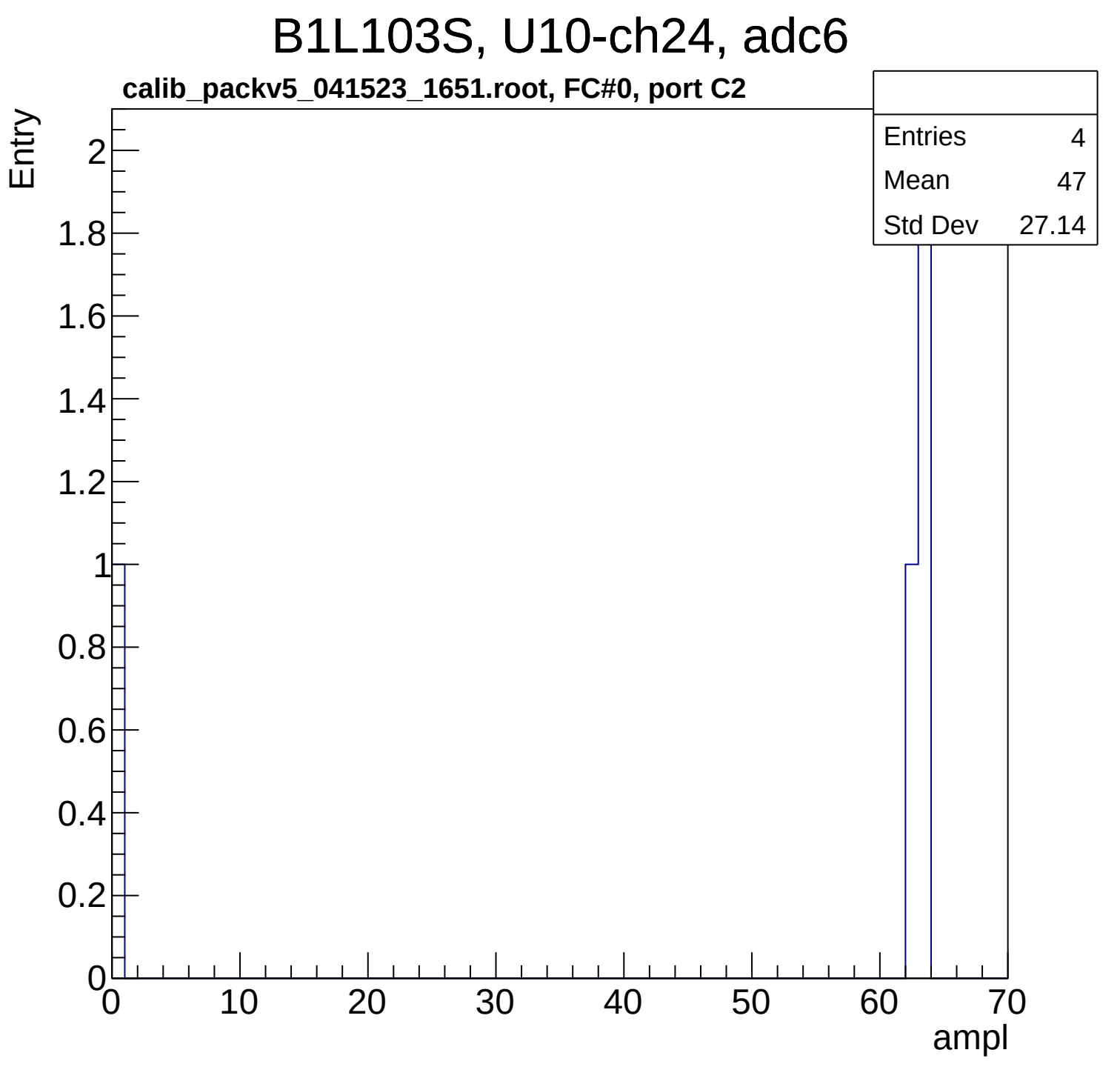
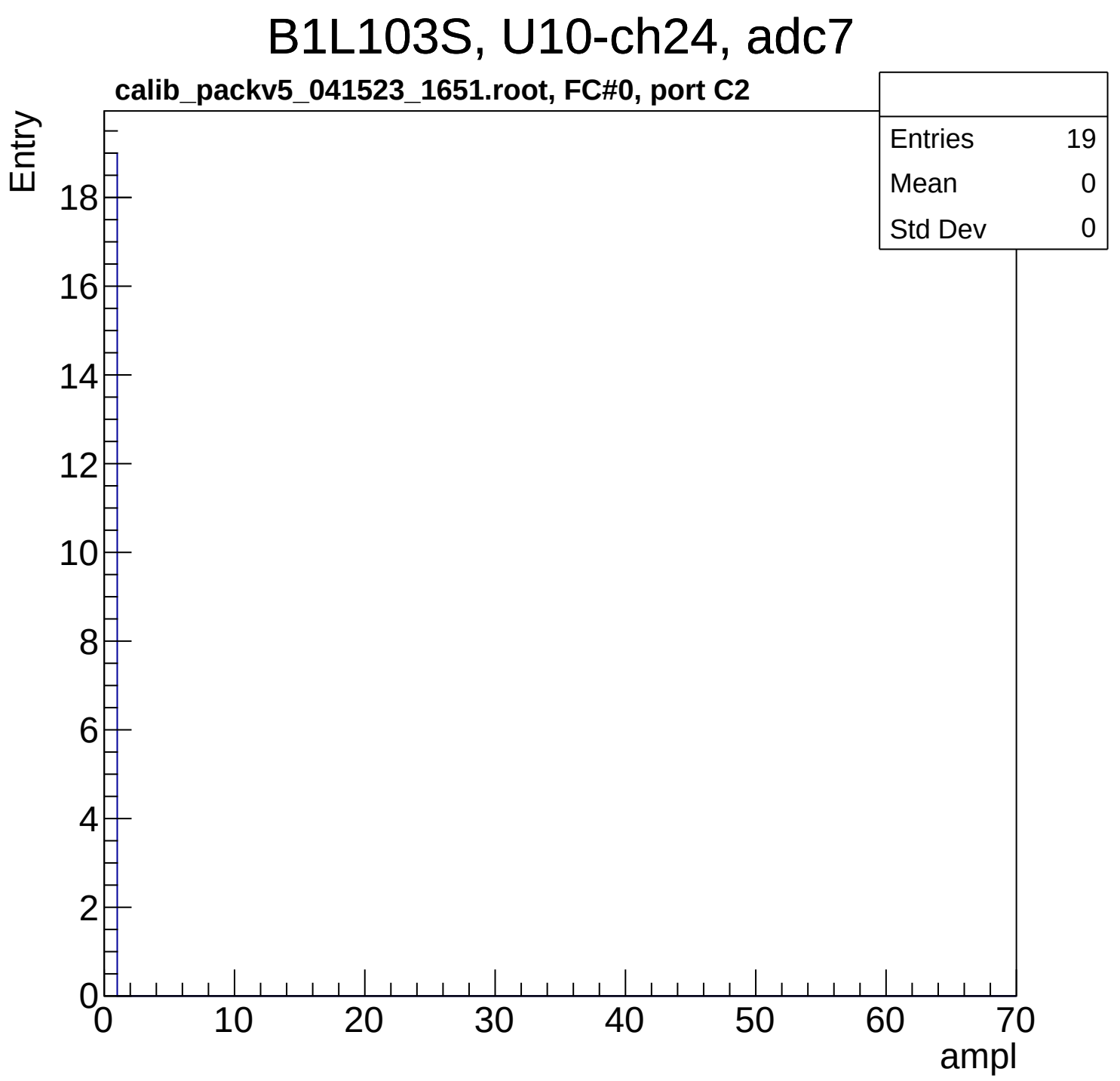
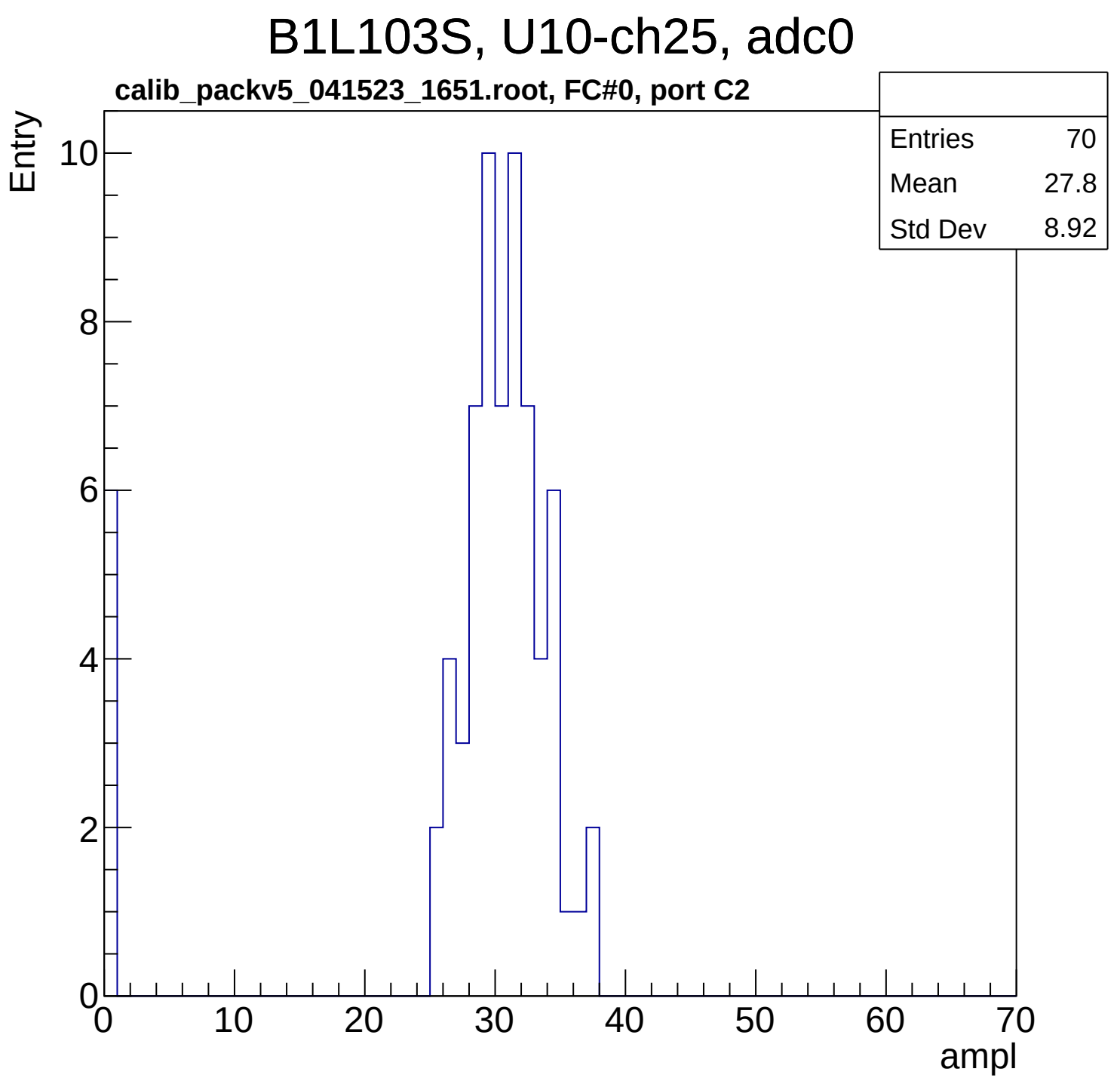
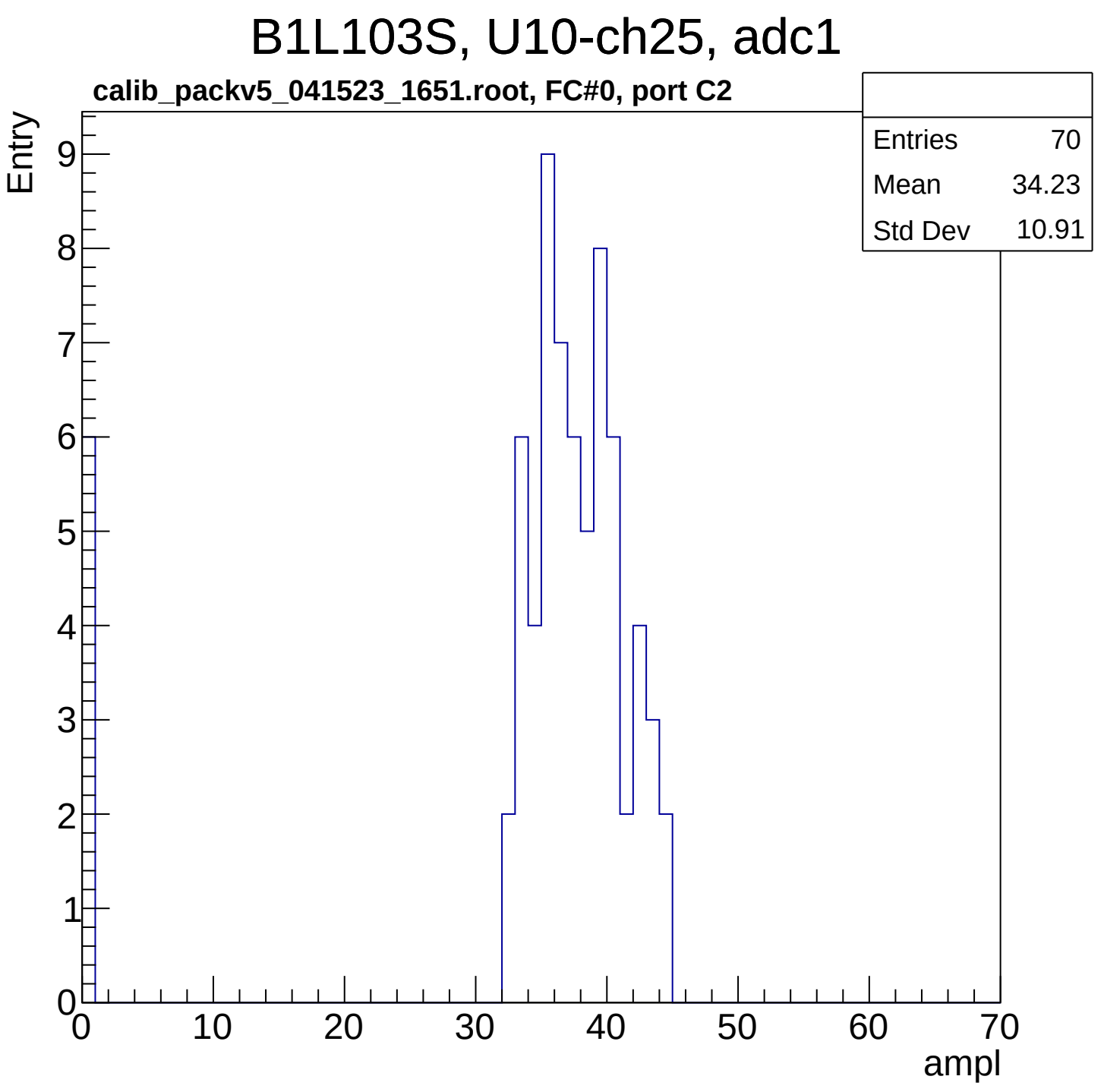
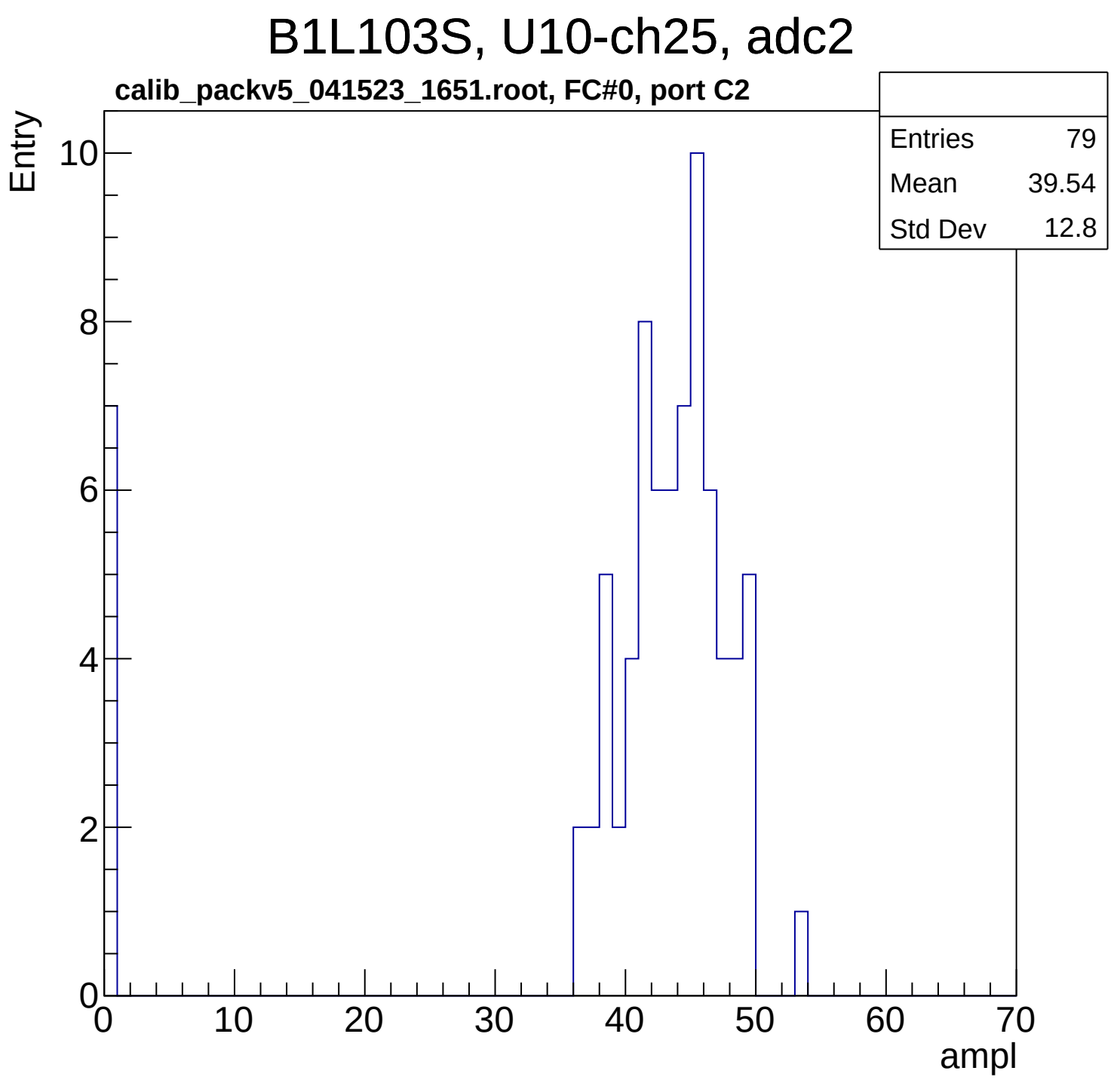
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

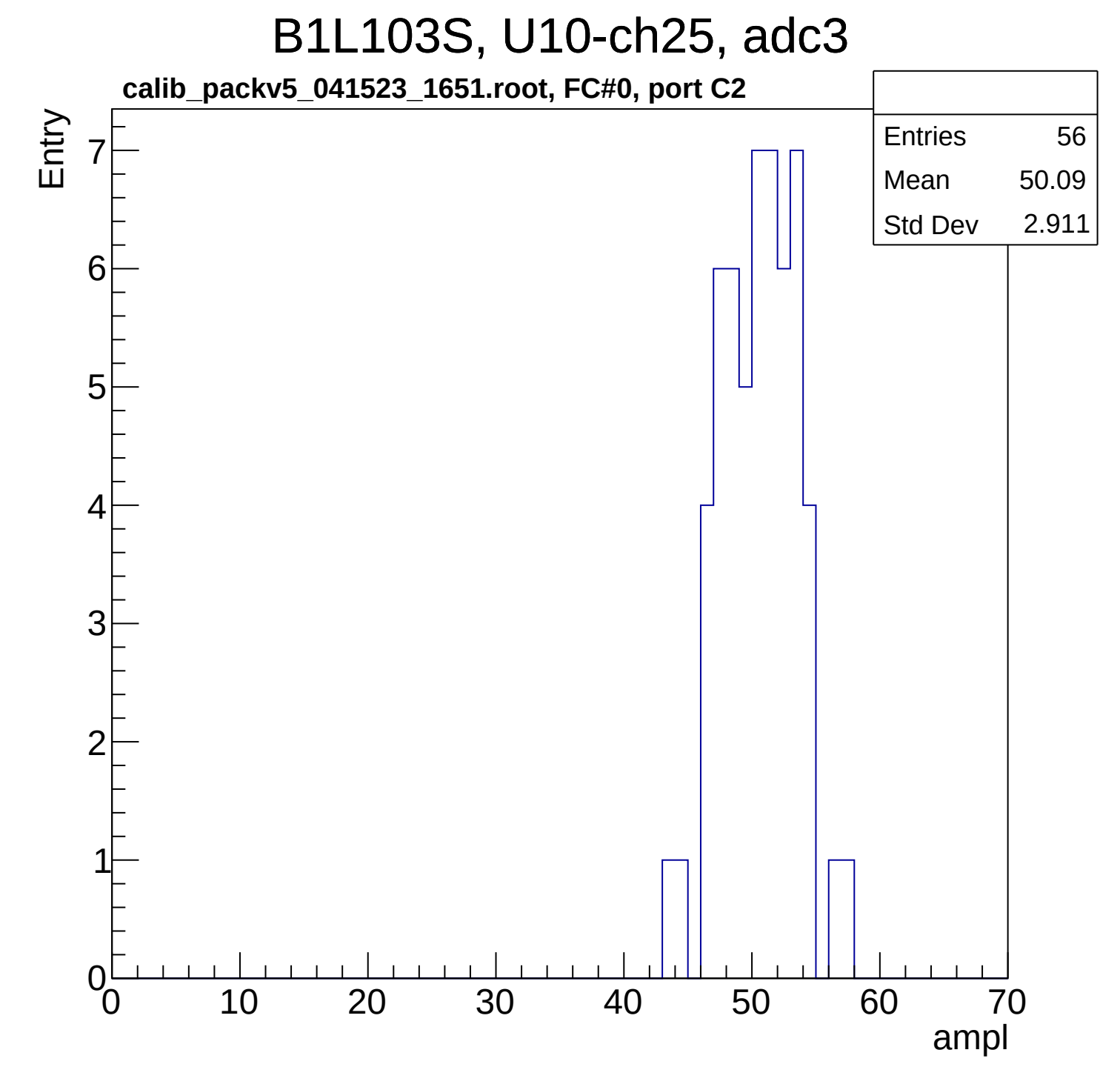

B1L103S, U10-ch24, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 4
Mean 47
Std Dev 27.14
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

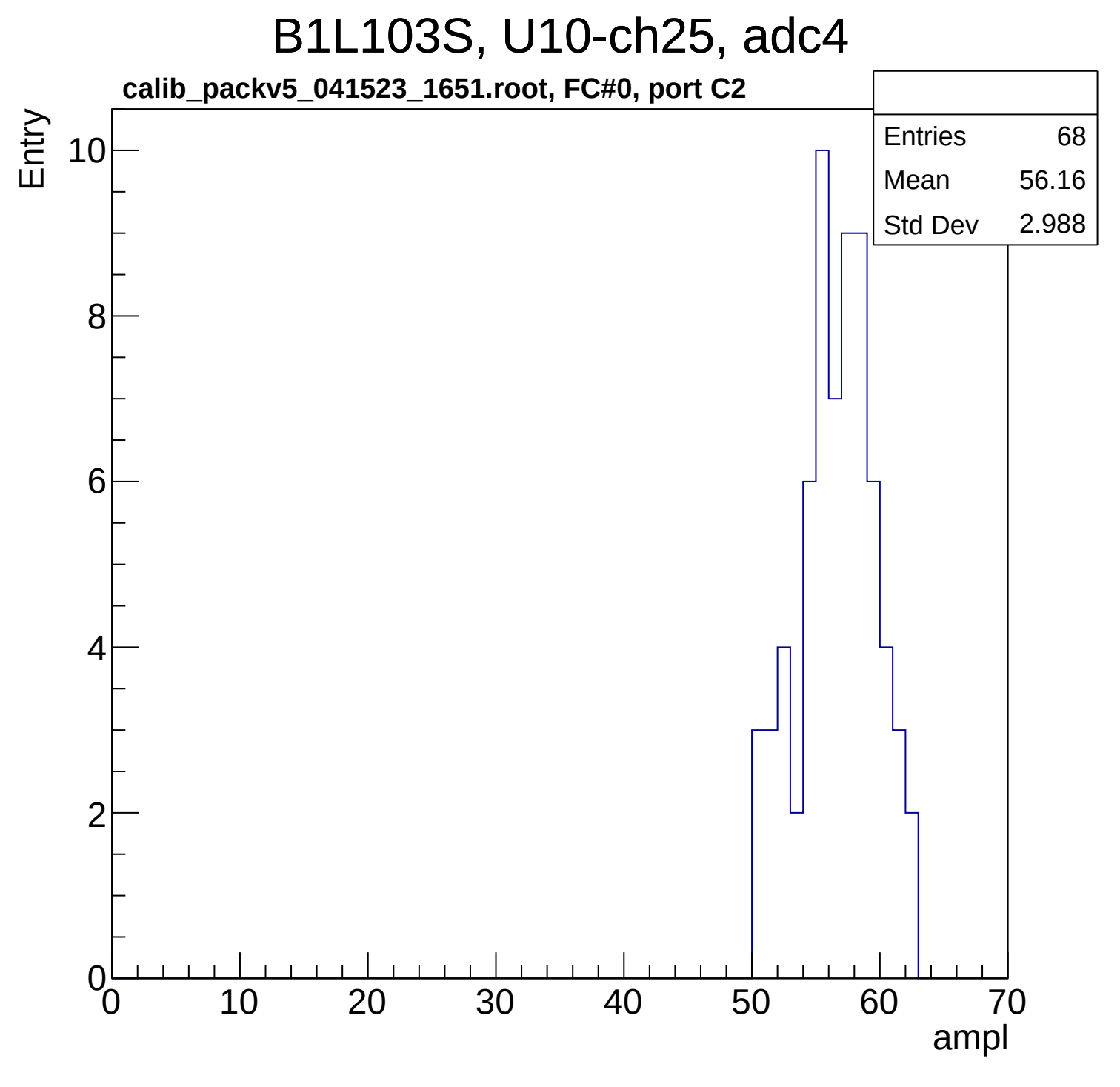

B1L103S, U10-ch24, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

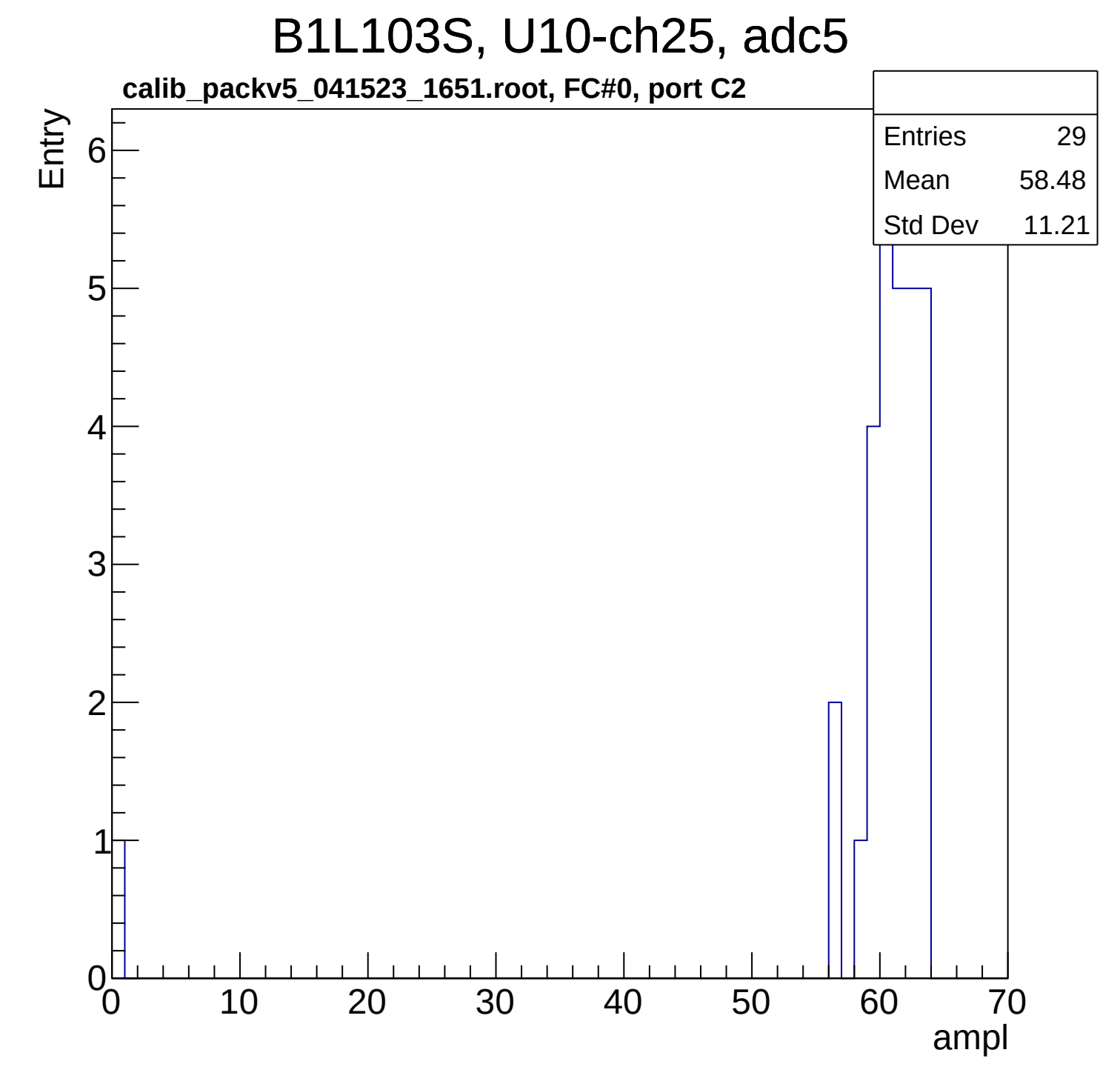

B1L103S, U10-ch25, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 27.8
Std Dev 8.92
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch25, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 34.23
Std Dev 10.91
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U10-ch25, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 39.54
Std Dev 12.8
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U10-ch25, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 50.09
Std Dev 2.911
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U10-ch25, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 56.16
Std Dev 2.988
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U10-ch25, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 29
Mean 58.48
Std Dev 11.21
Entry
ampl
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2
3
4
5
6
0
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20
30
40
50
60
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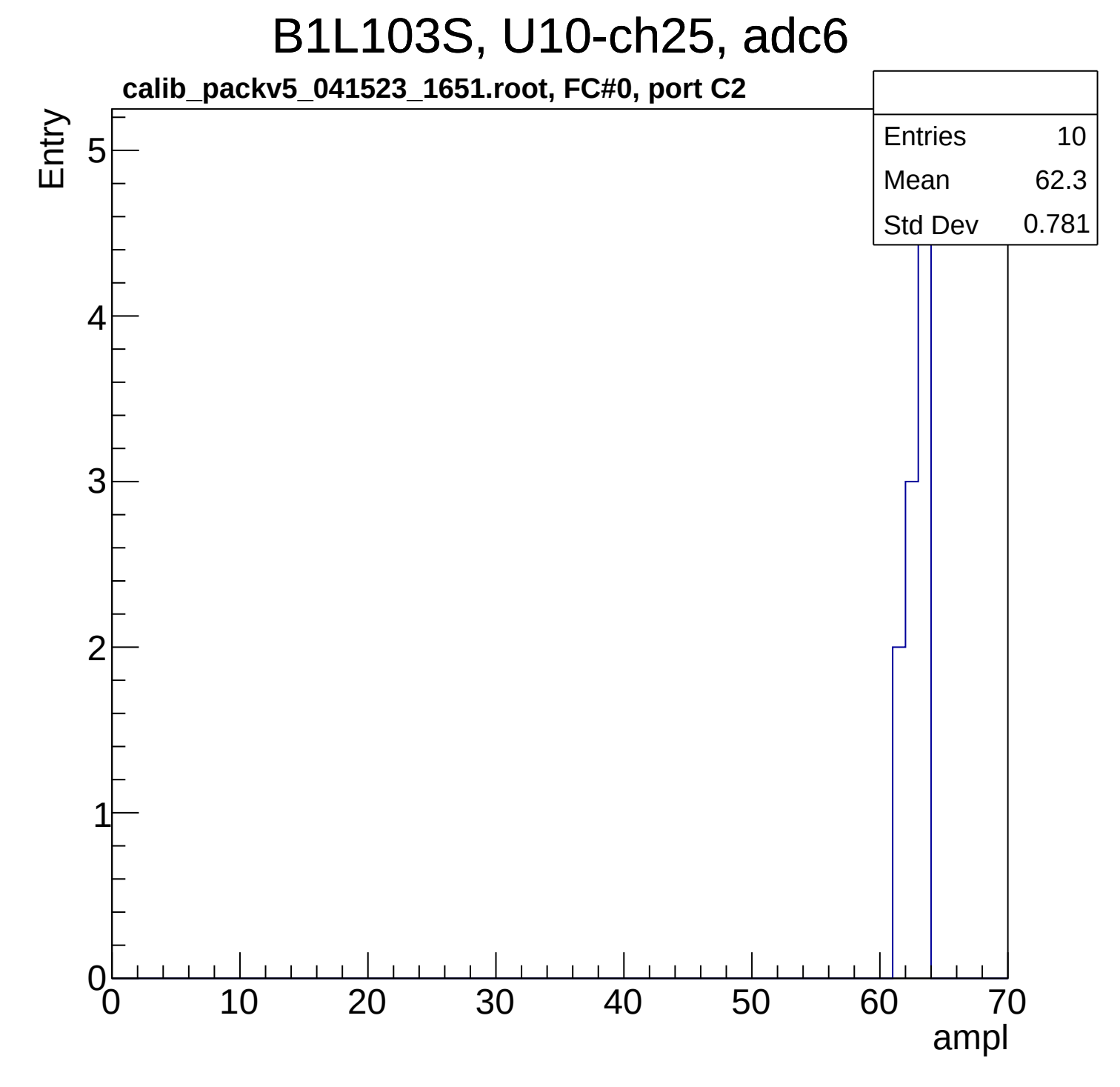
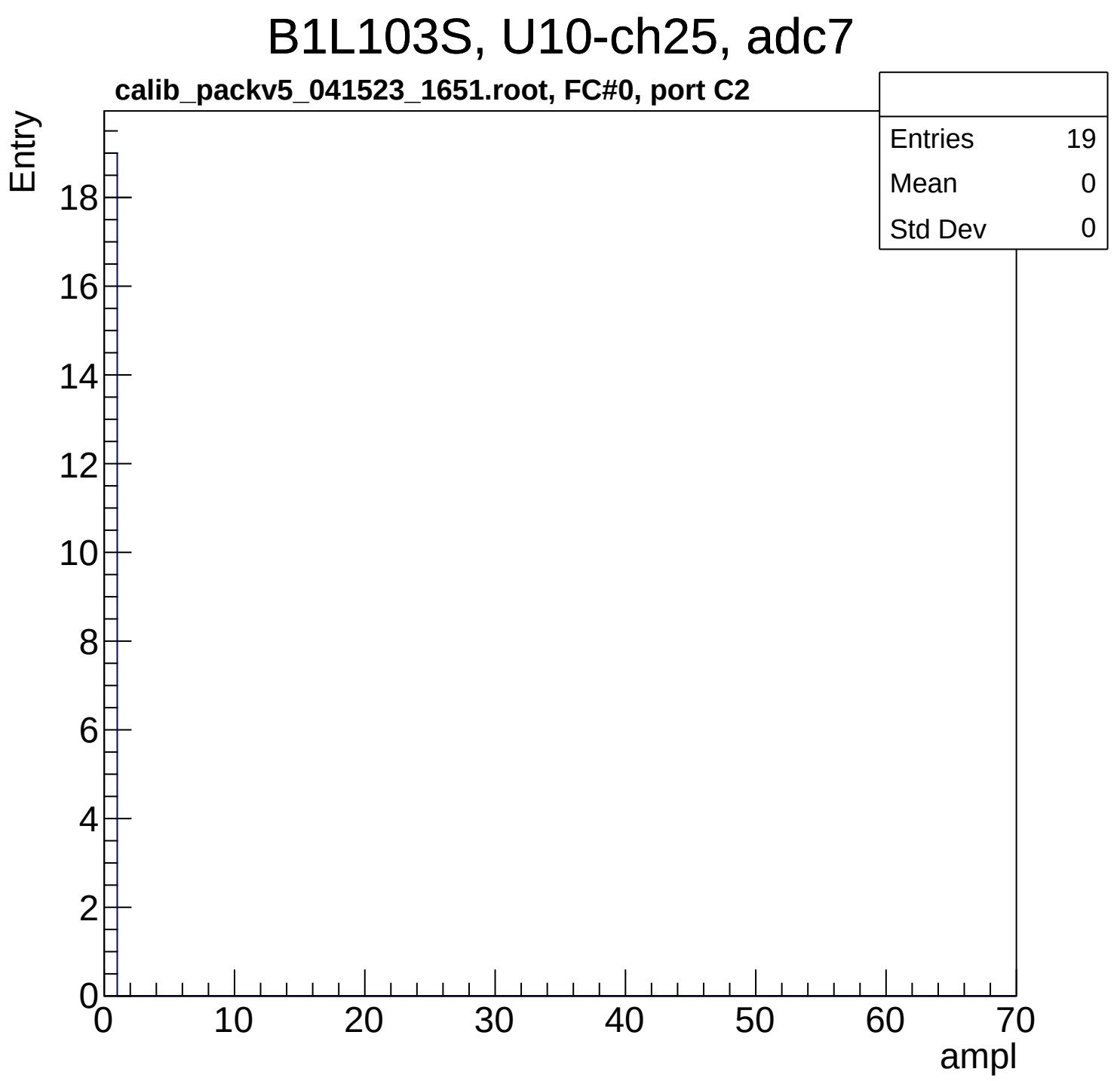
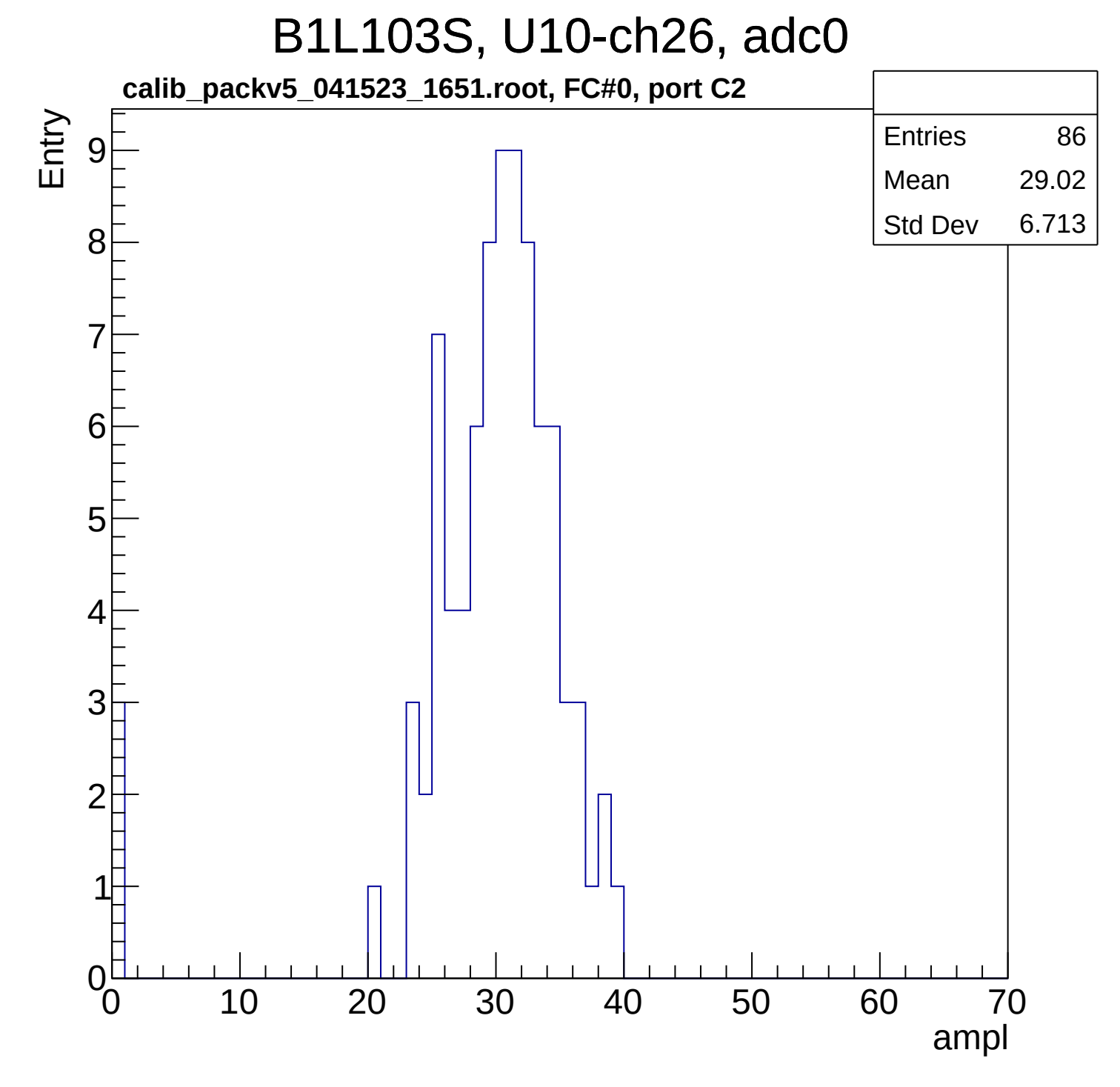

B1L103S, U10-ch25, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 62.3
Std Dev 0.781
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U10-ch25, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch26, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 29.02
Std Dev 6.713
Entry
ampl
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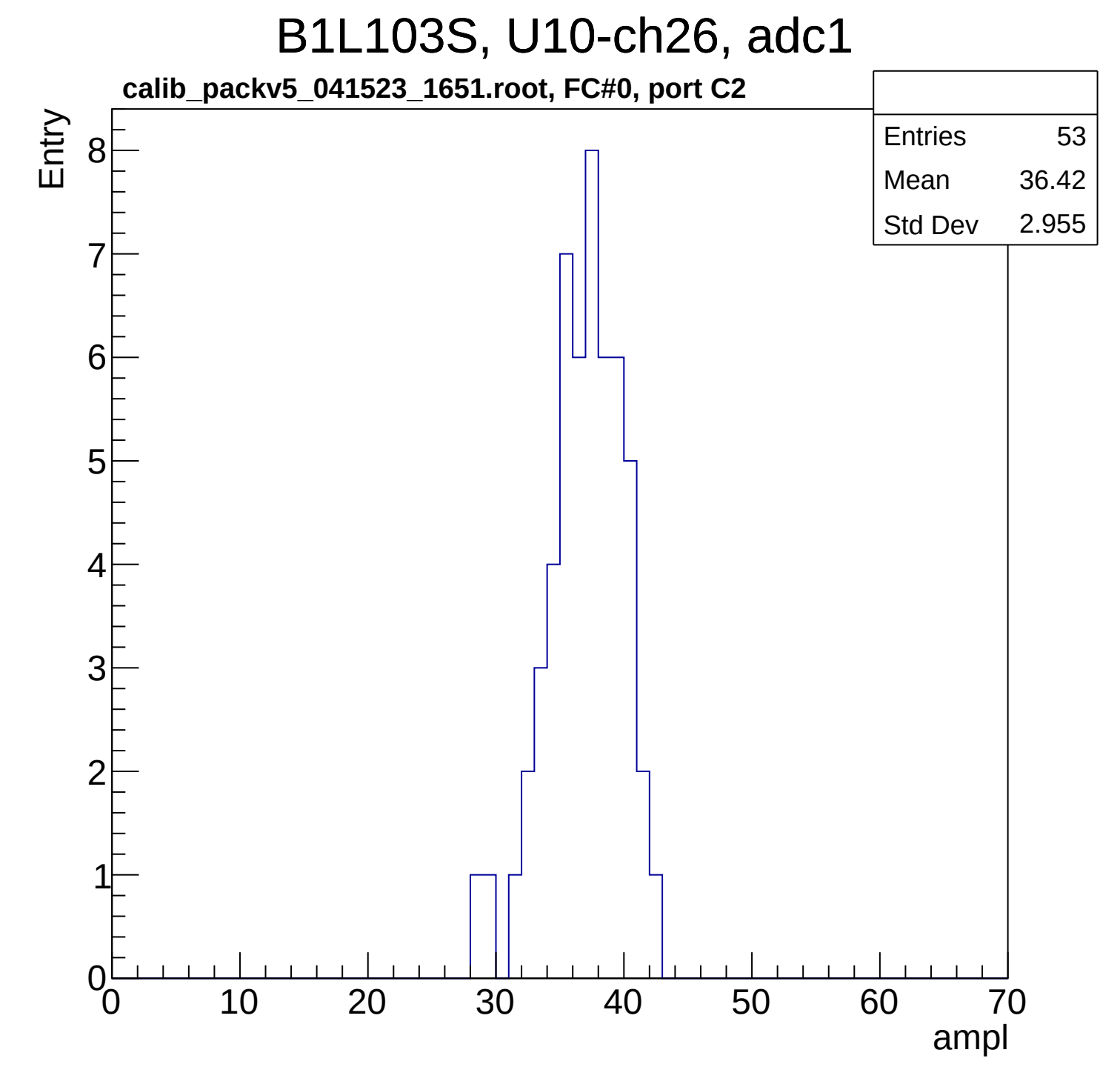
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U10-ch26, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 36.42
Std Dev 2.955
Entry
ampl
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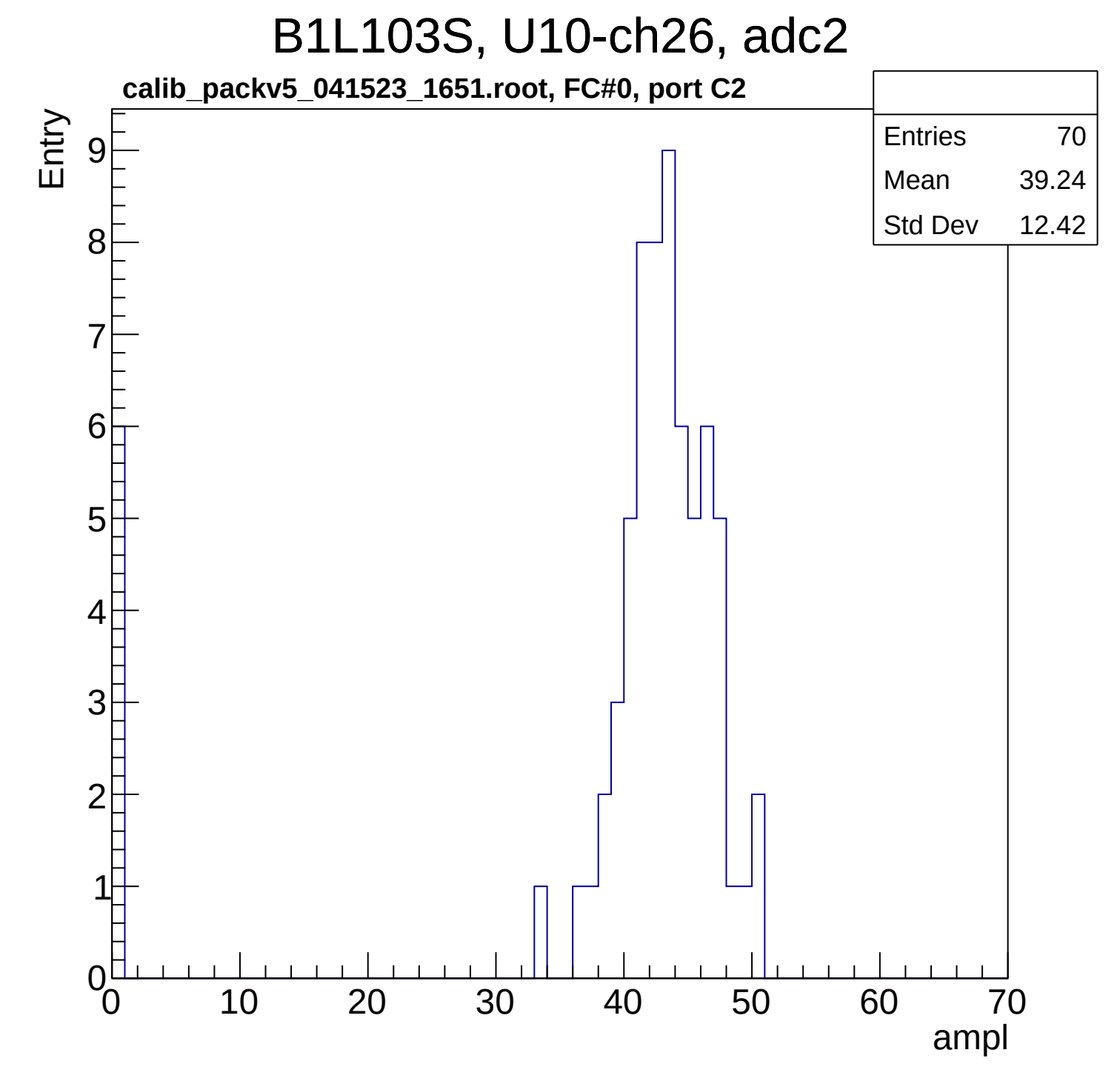
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U10-ch26, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 39.24
Std Dev 12.42
Entry
ampl
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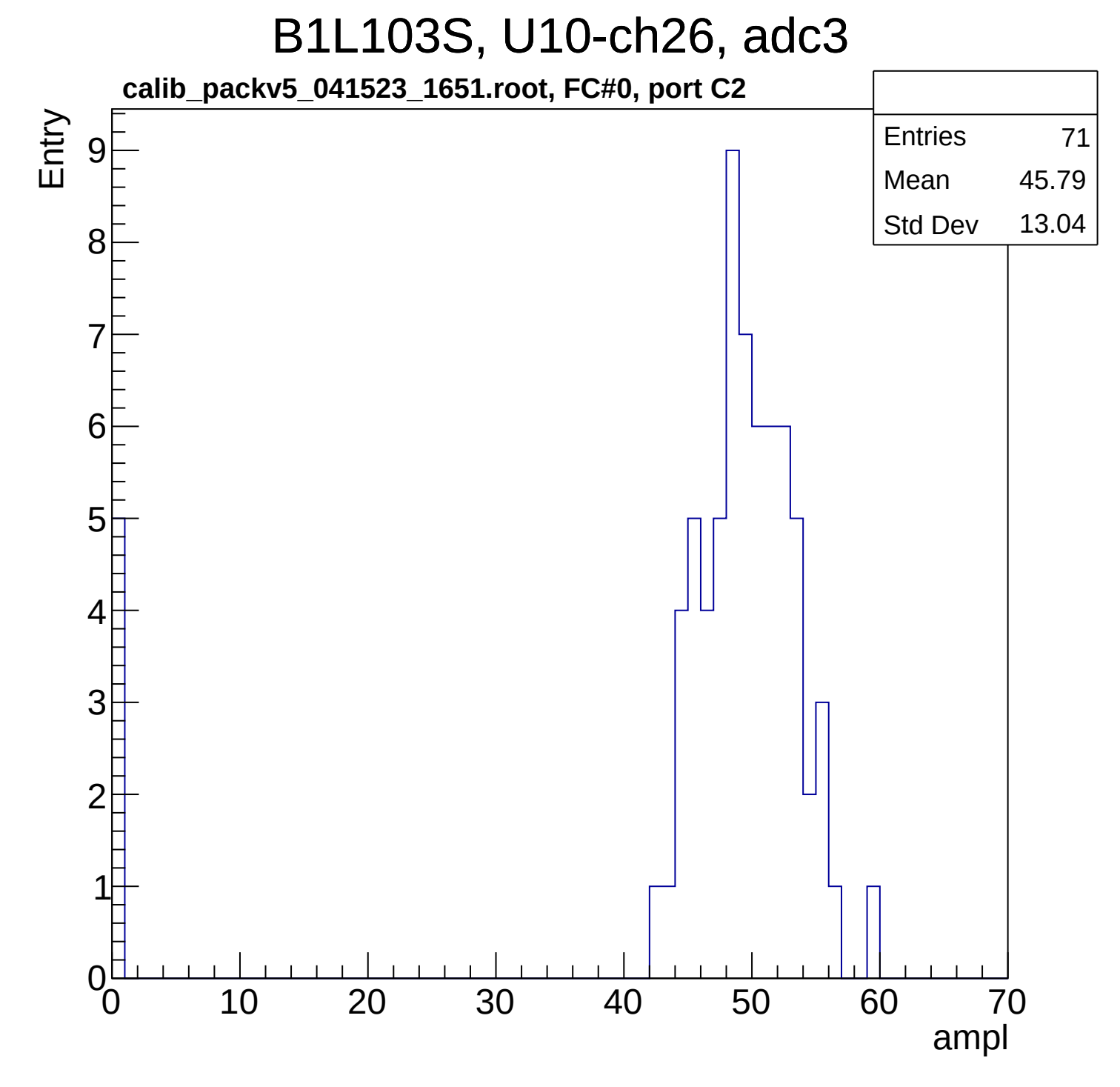
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U10-ch26, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 45.79
Std Dev 13.04
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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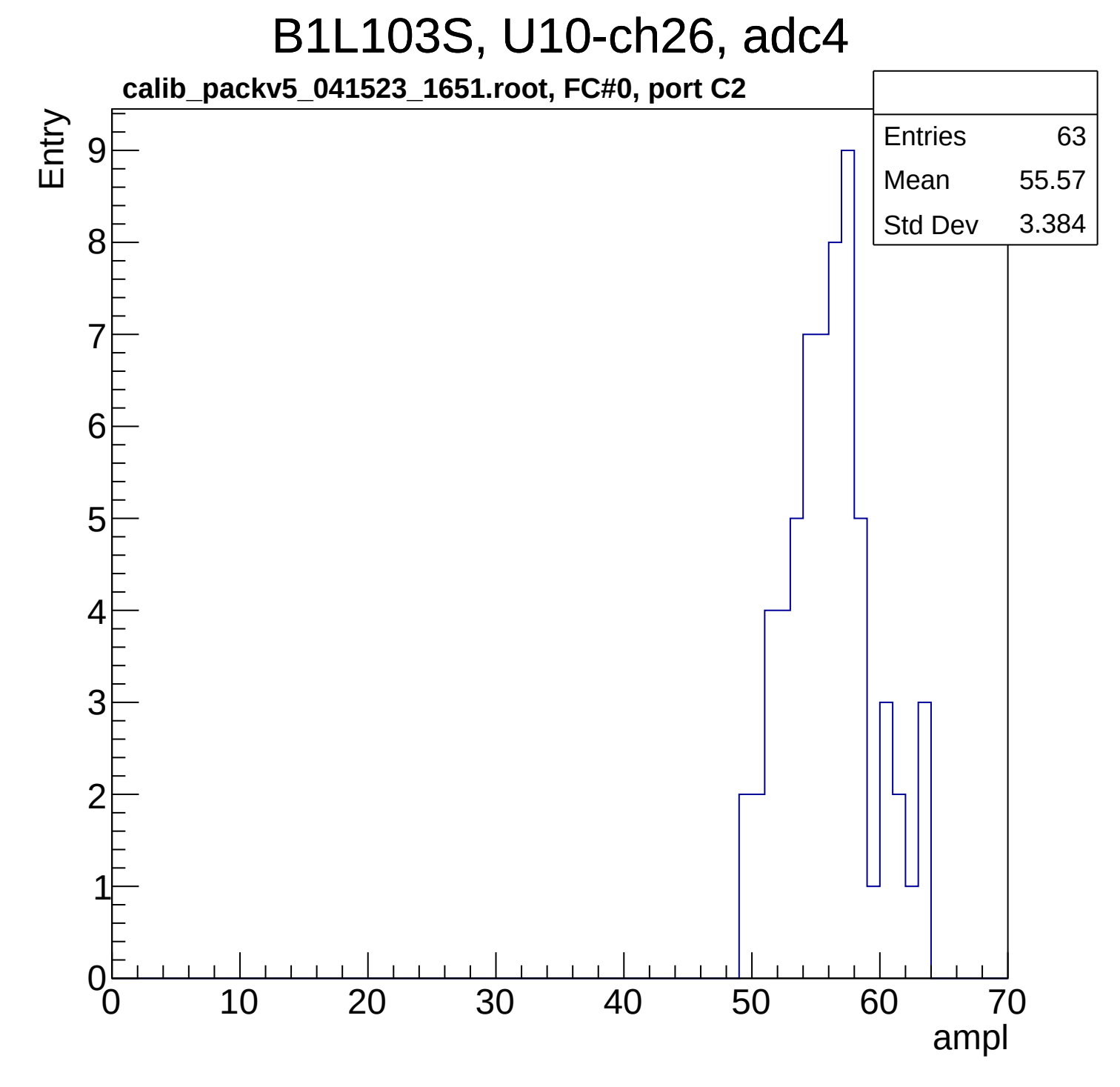
40
50
60
70


B1L103S, U10-ch26, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 55.57
Std Dev 3.384
Entry
ampl
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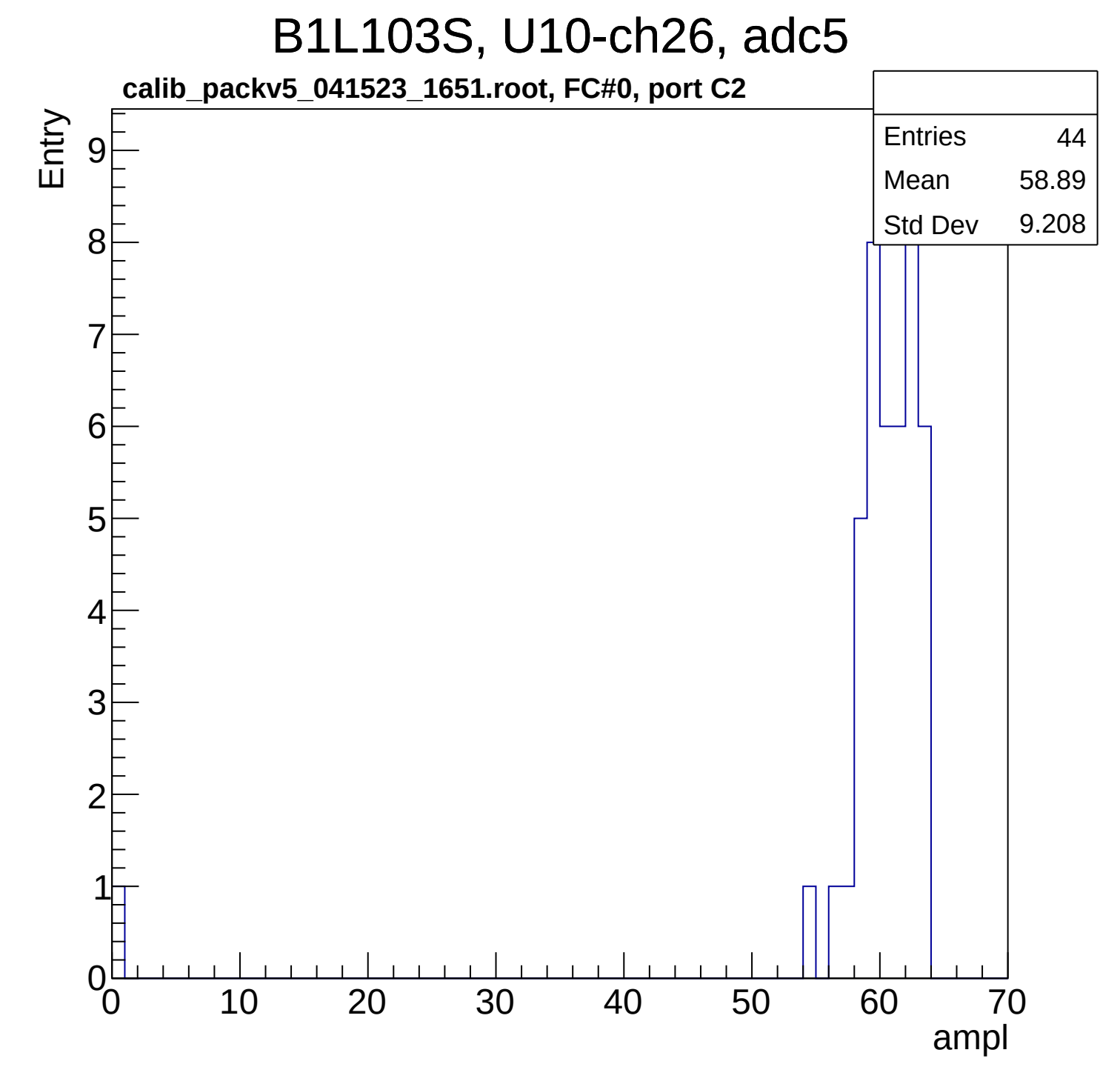
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U10-ch26, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 58.89
Std Dev 9.208
Entry
ampl
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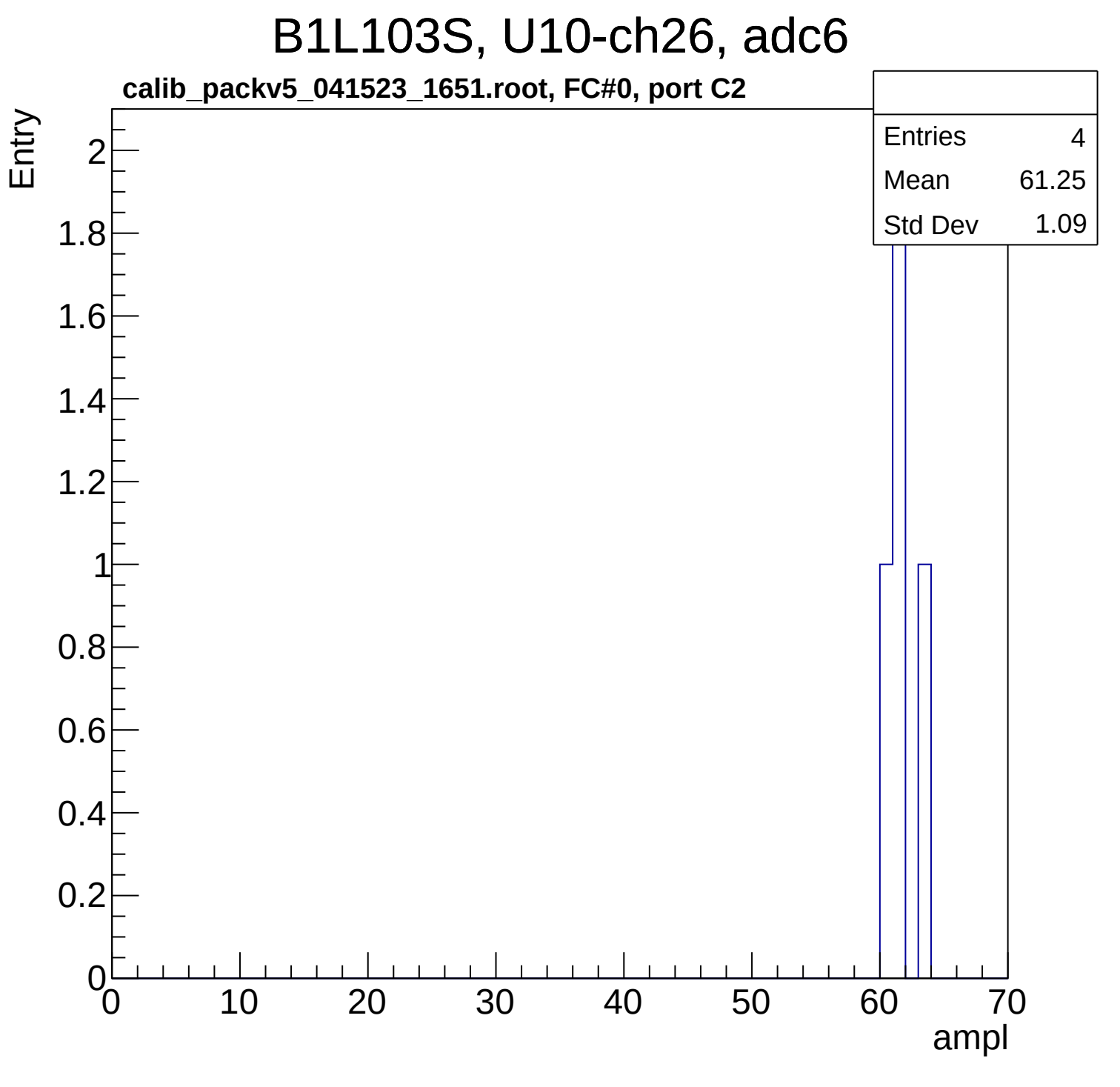
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U10-ch26, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 4
Mean 61.25
Std Dev 1.09
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
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40
50
60
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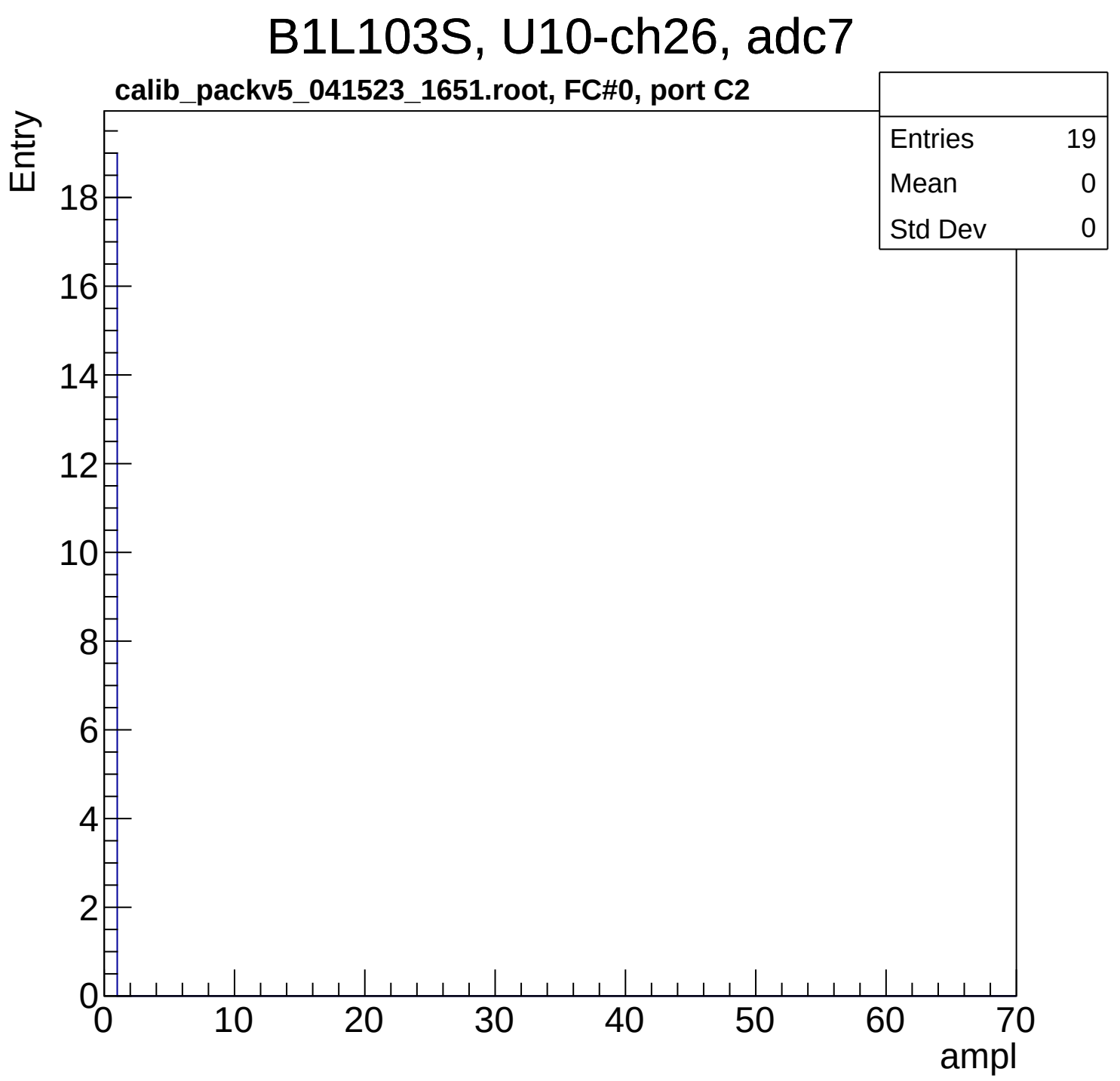
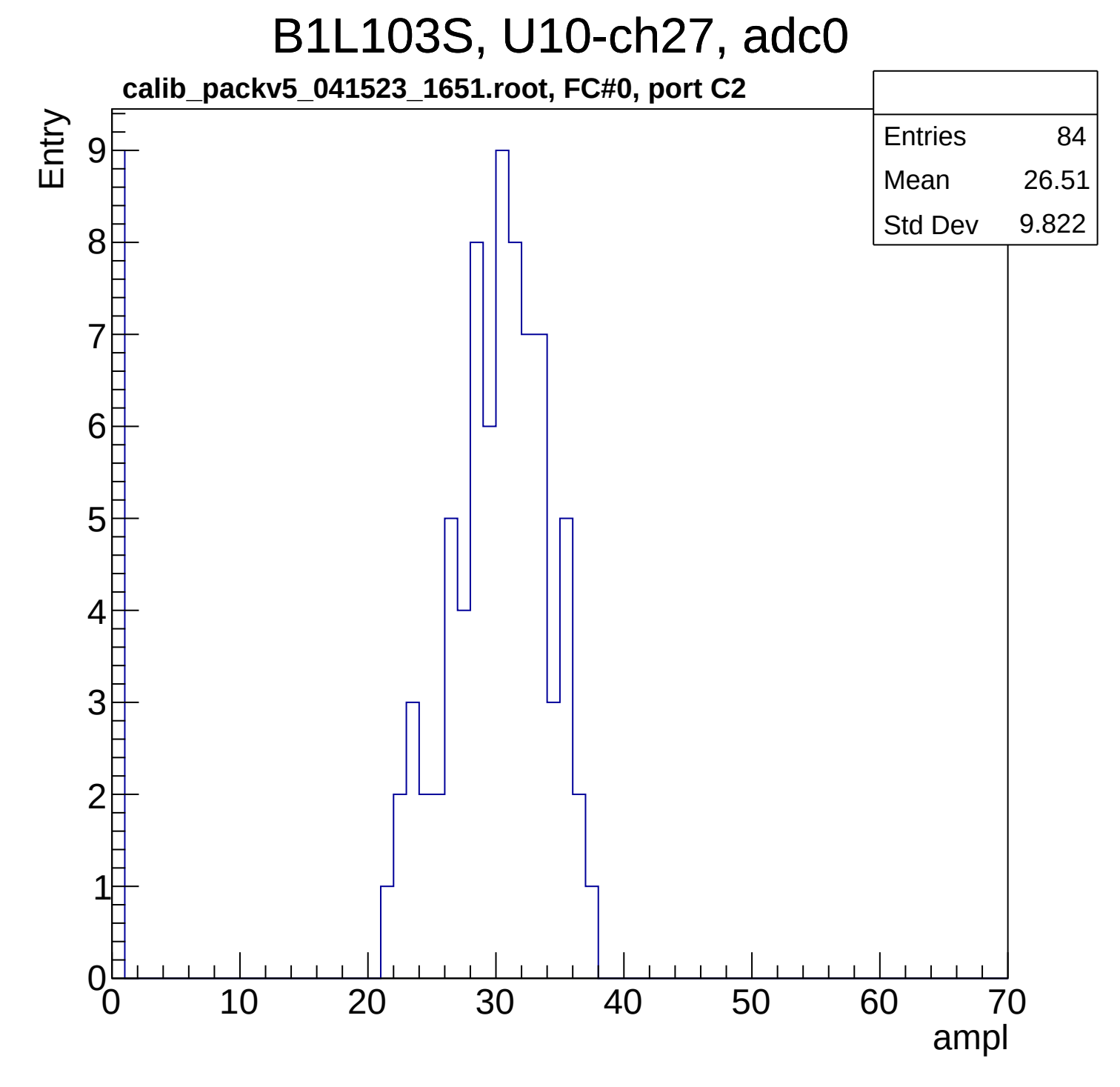
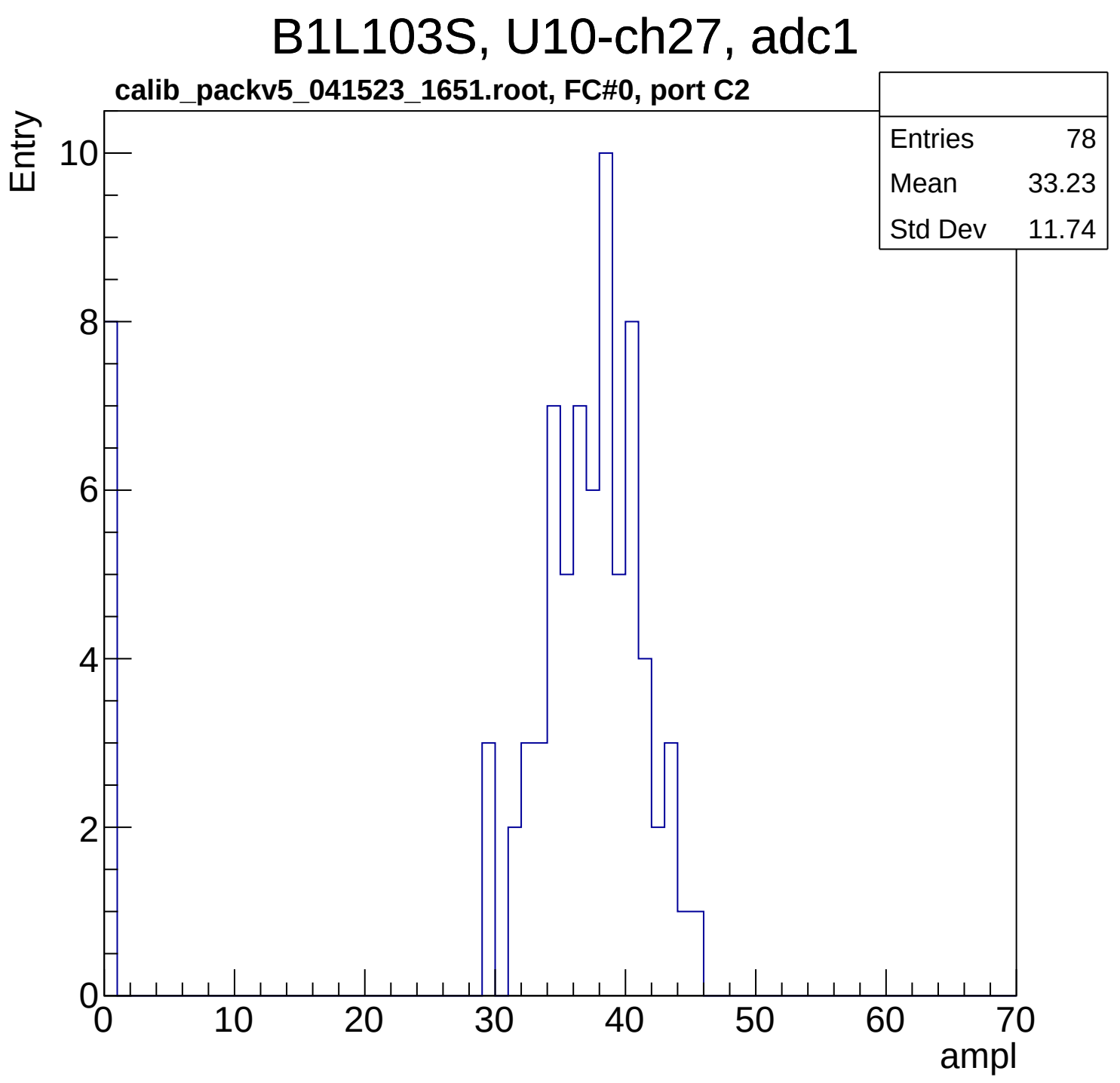

B1L103S, U10-ch26, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch27, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 26.51
Std Dev 9.822
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U10-ch27, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 33.23
Std Dev 11.74
Entry
0
2
4
6
8
10
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10
20
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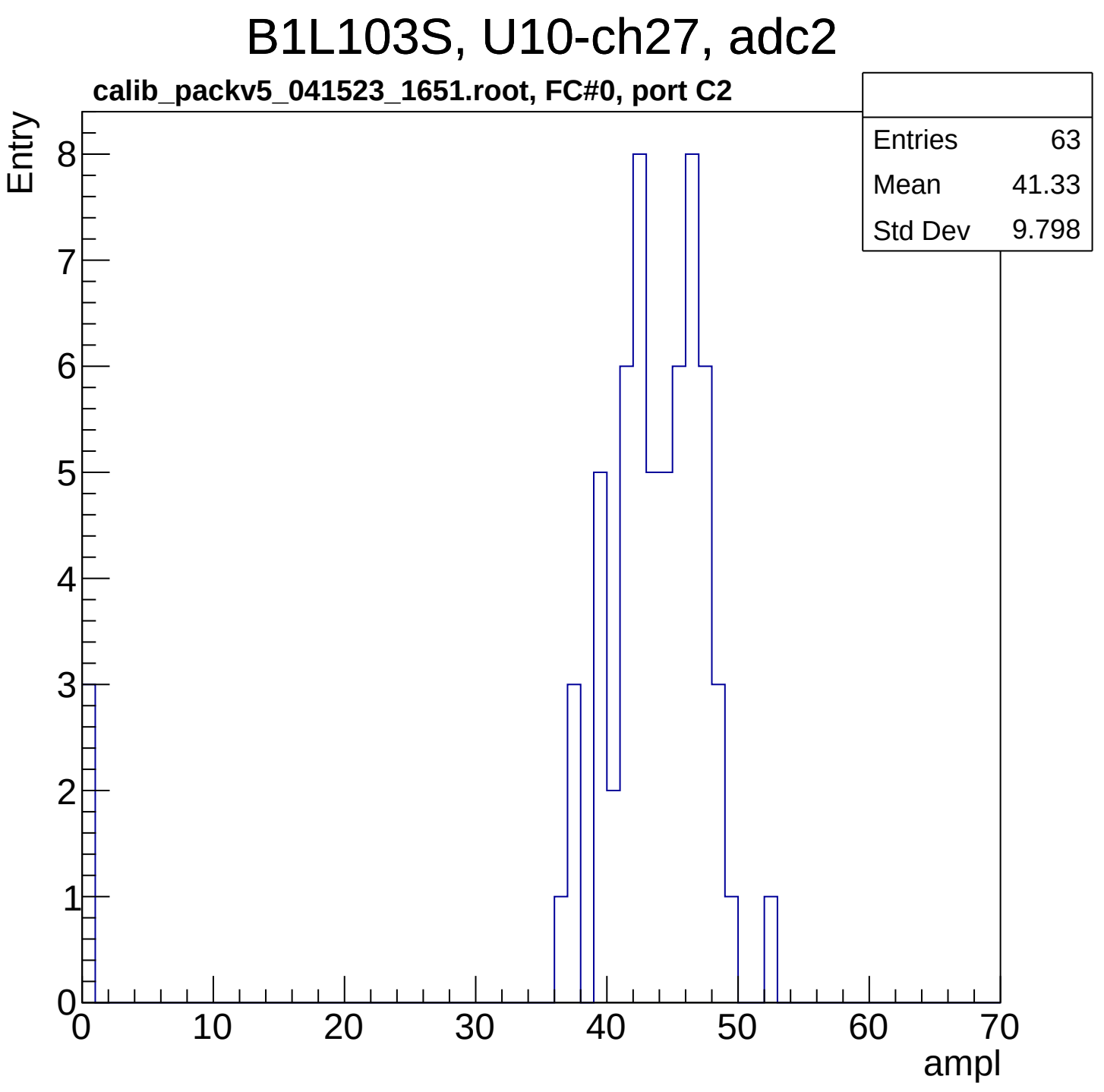
50
60
70
ampl


B1L103S, U10-ch27, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 41.33
Std Dev 9.798
Entry
ampl
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2
3
4
5
6
7
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0
10
20
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40
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60
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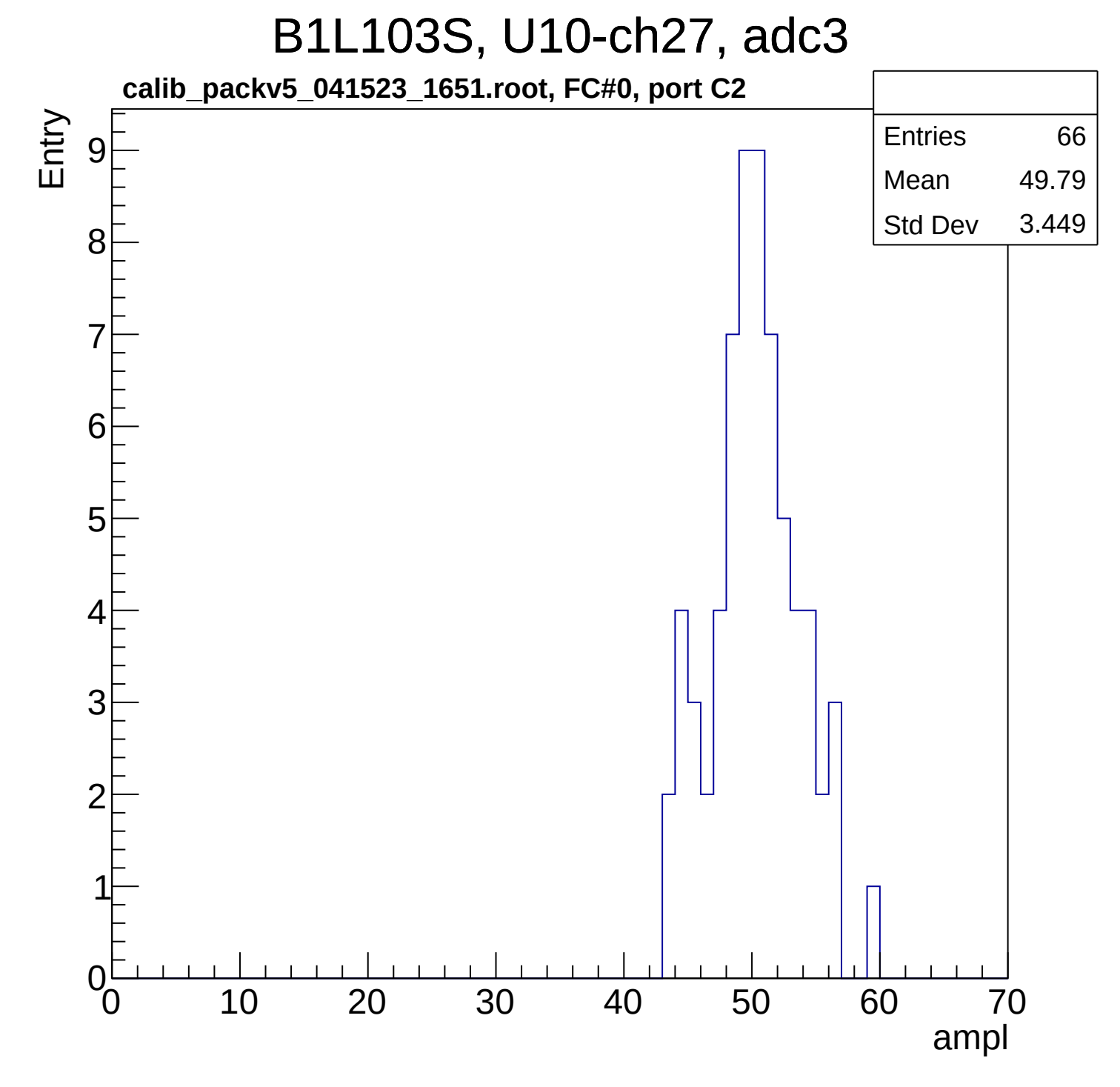
B1L103S, U10-ch27, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 49.79
Std Dev 3.449
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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60
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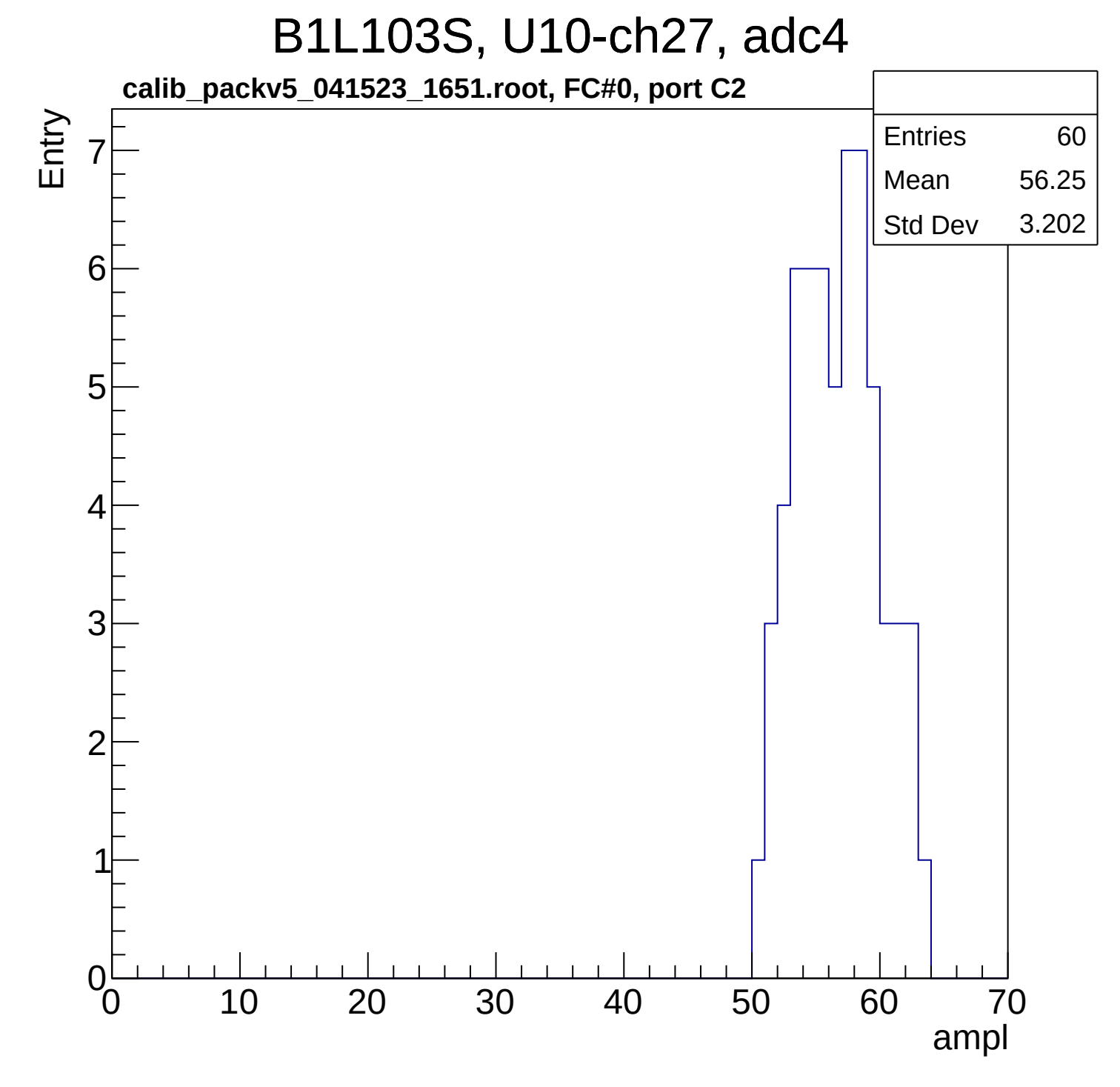
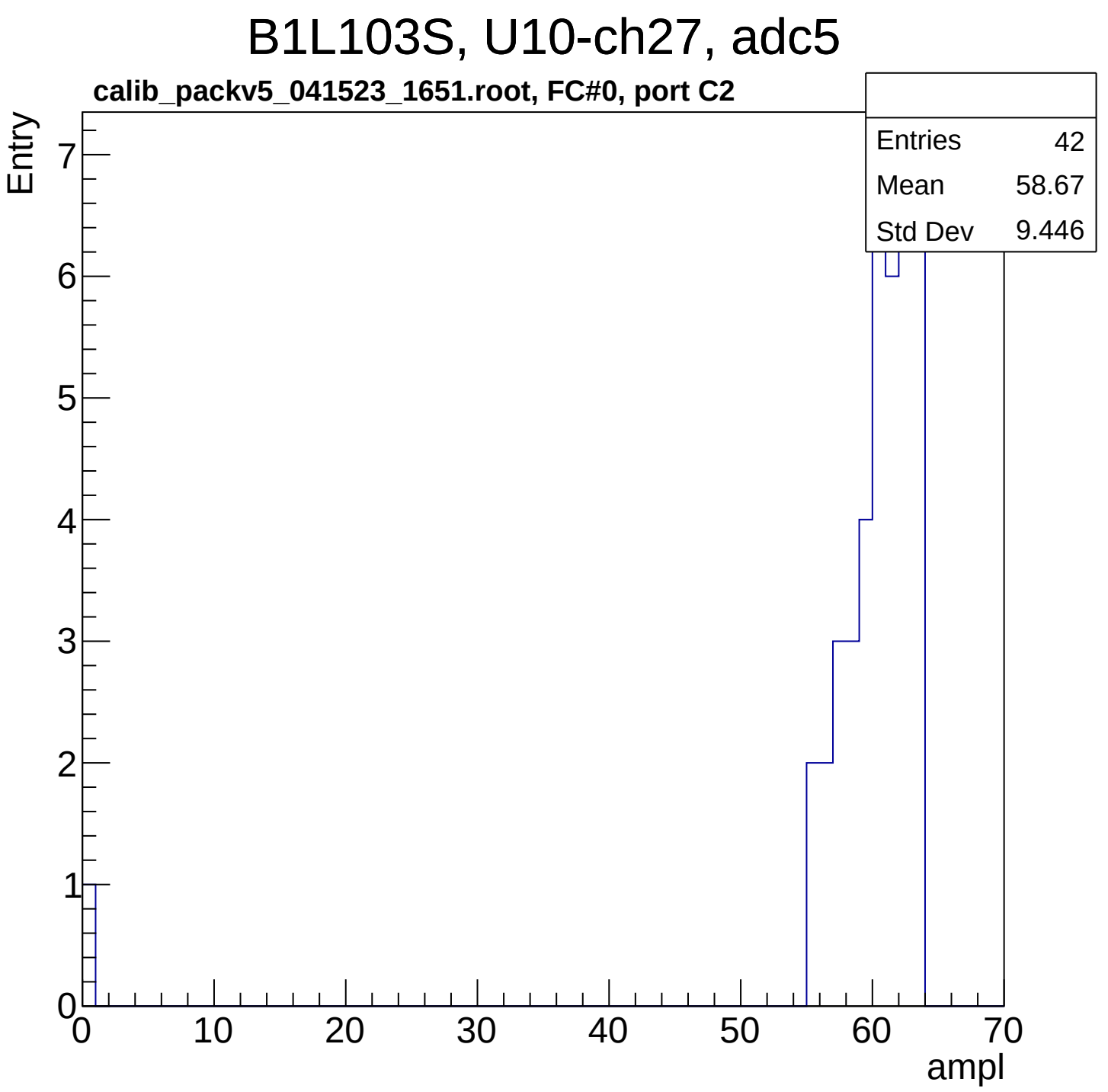
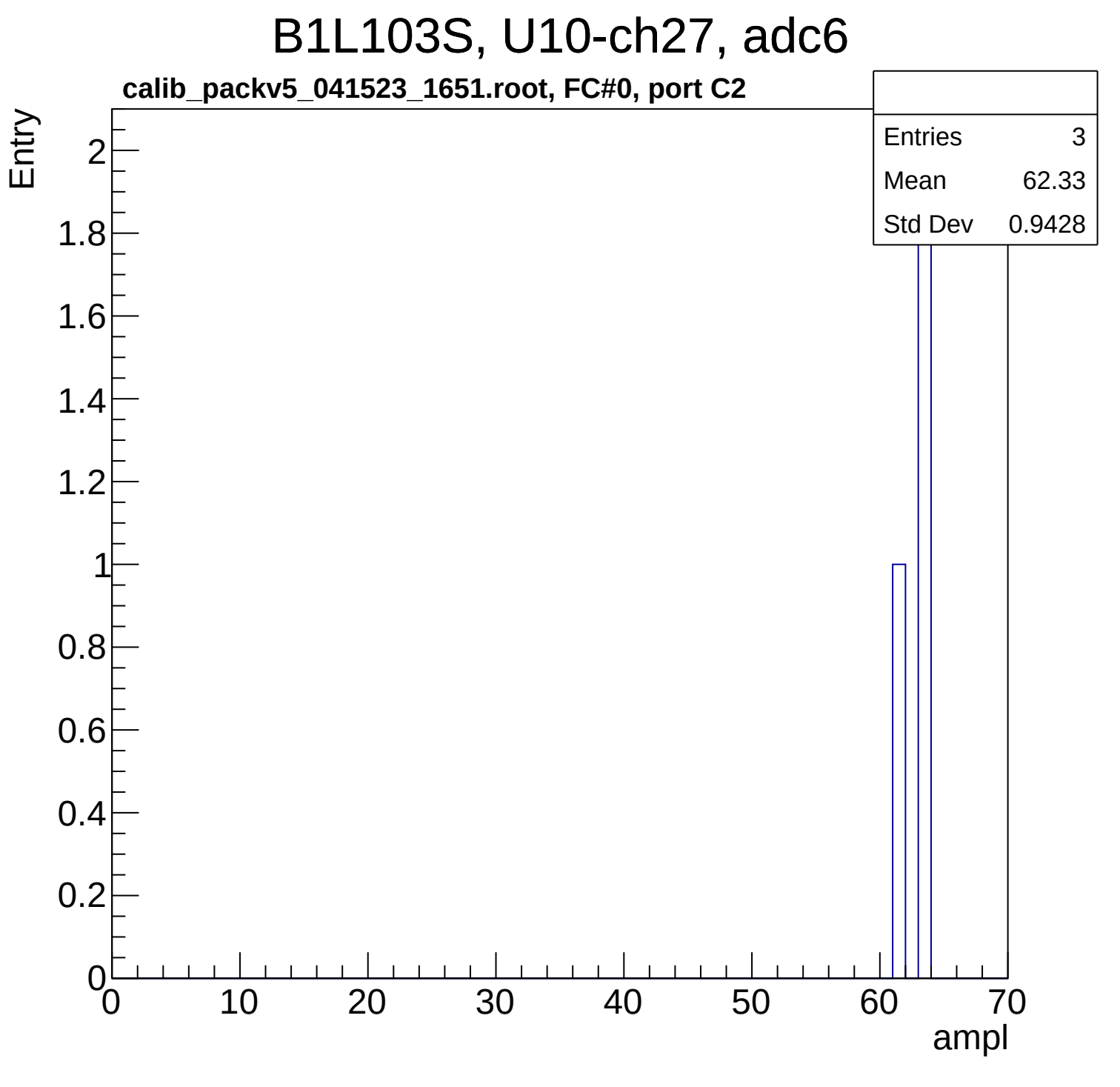

B1L103S, U10-ch27, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 56.25
Std Dev 3.202
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U10-ch27, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 42
Mean 58.67
Std Dev 9.446
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U10-ch27, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 3
Mean 62.33
Std Dev 0.9428
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
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20
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40
50
60
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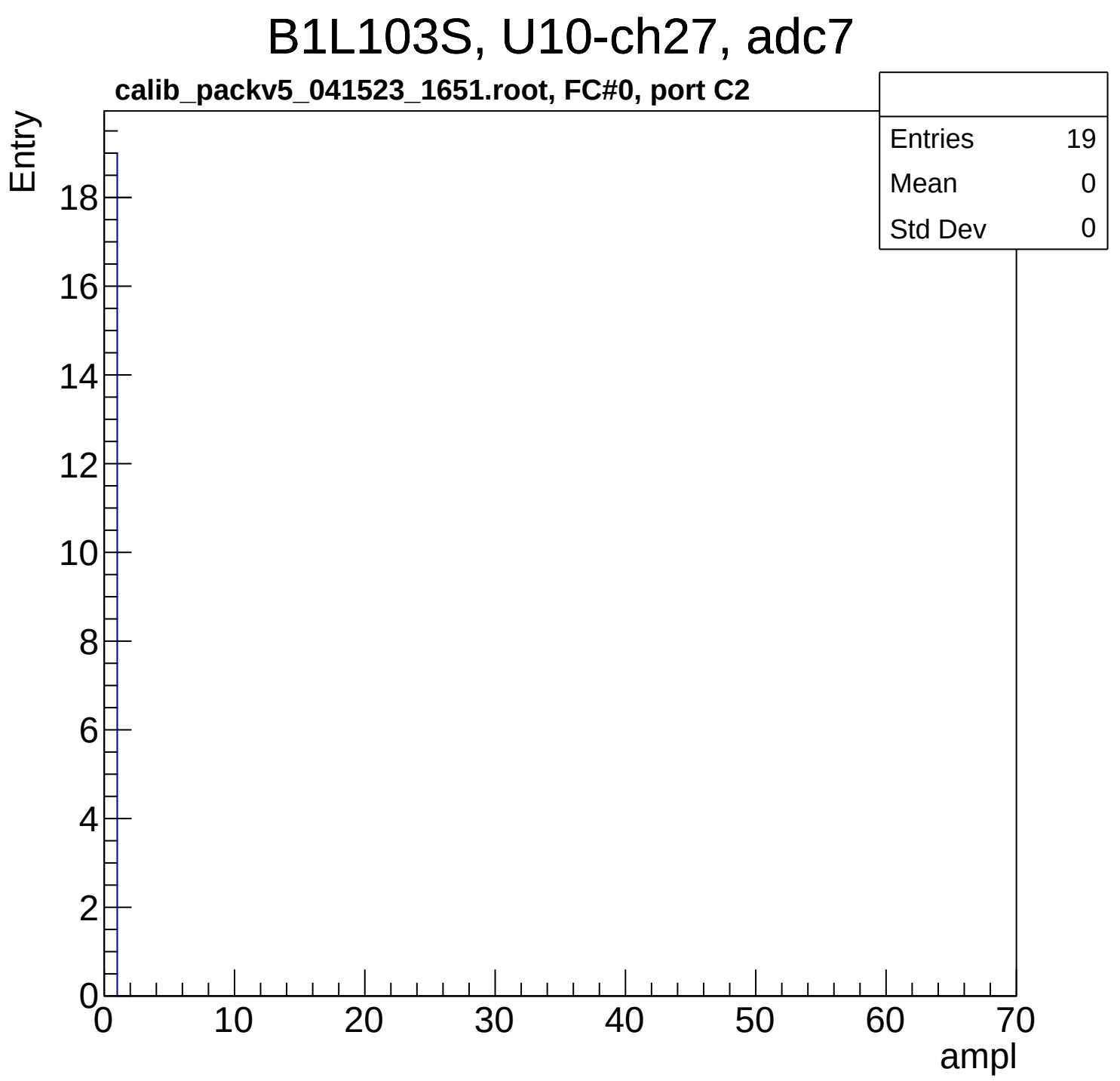
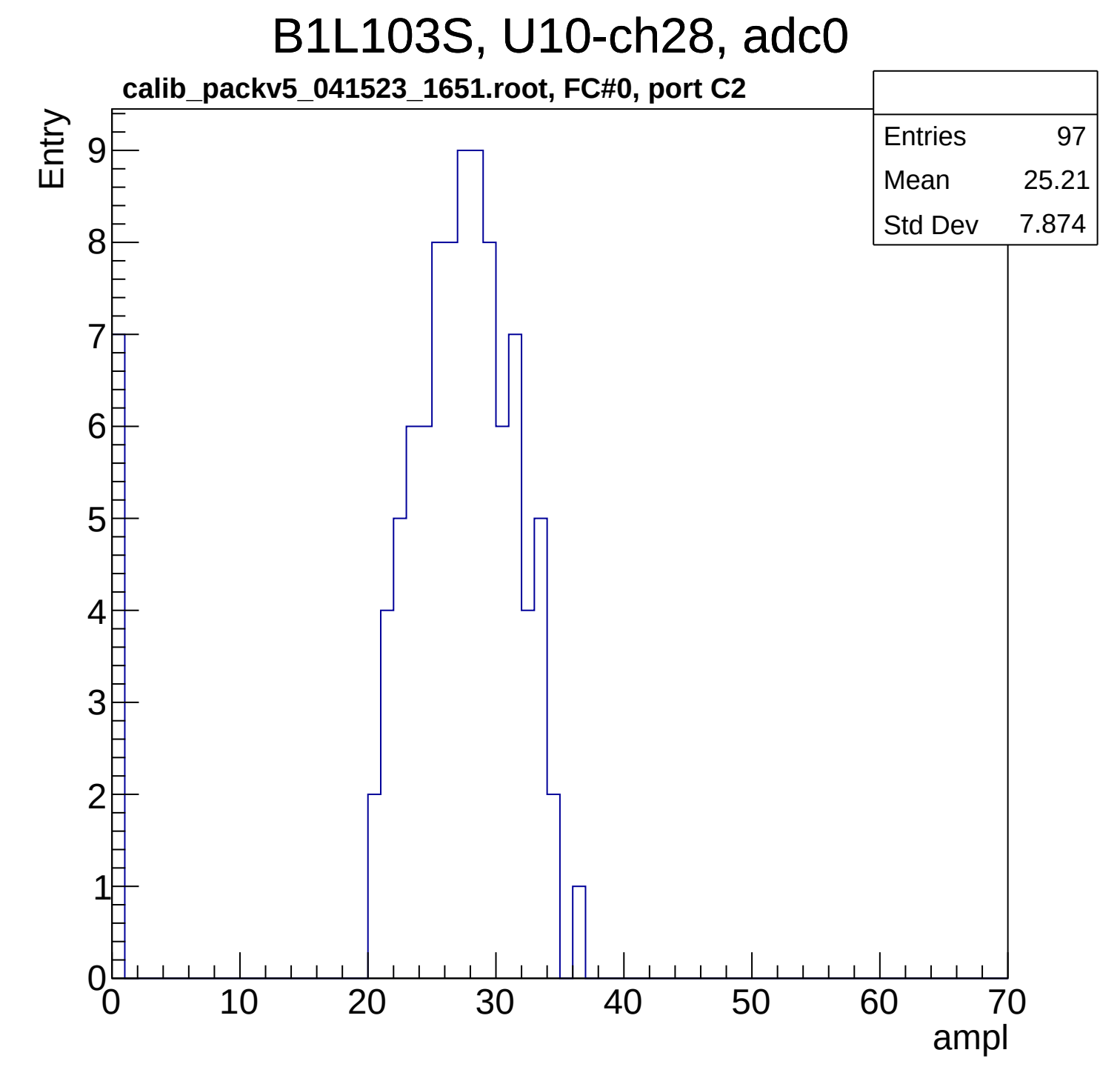

B1L103S, U10-ch27, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch28, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 97
Mean 25.21
Std Dev 7.874
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
50
60
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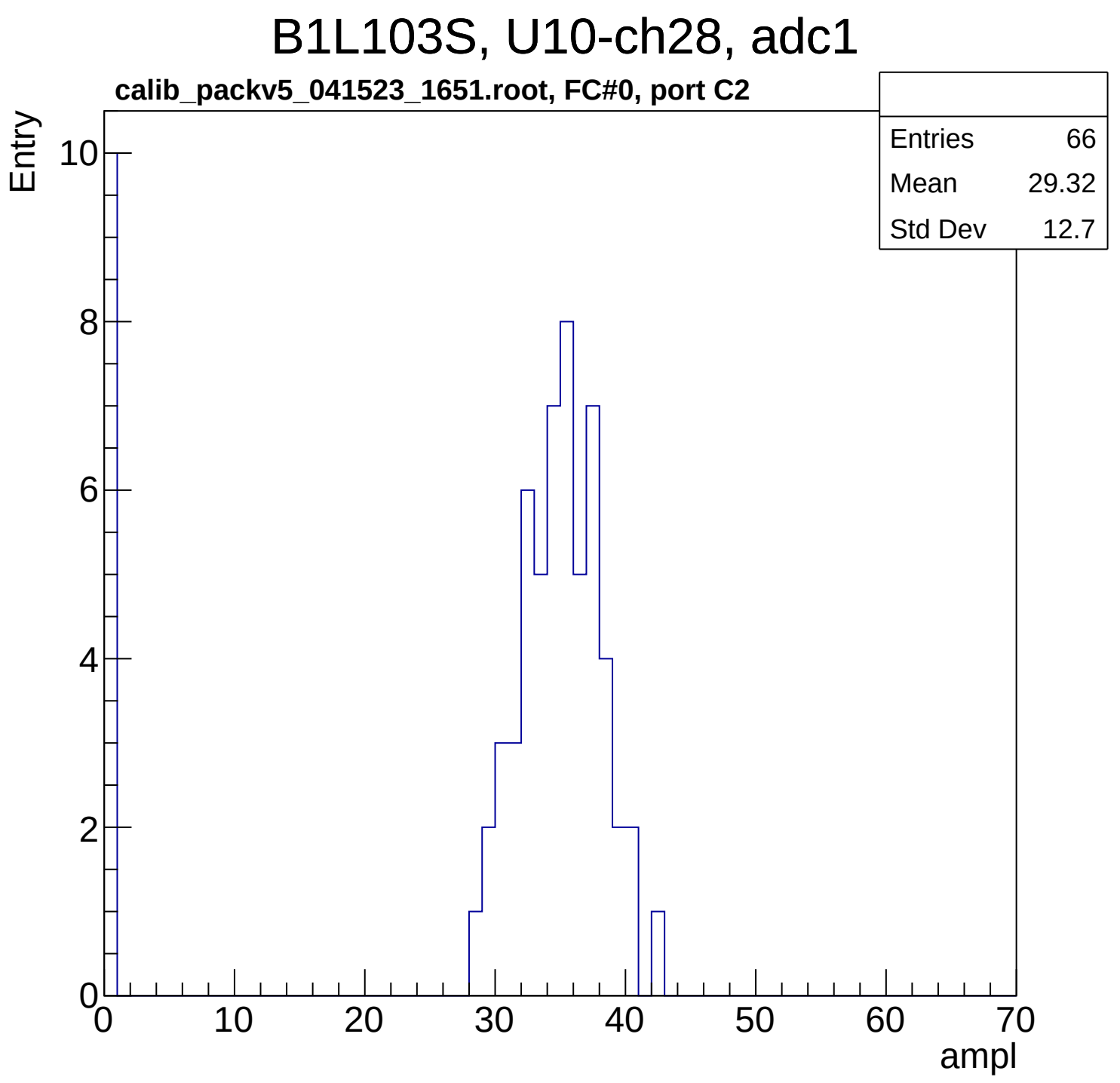
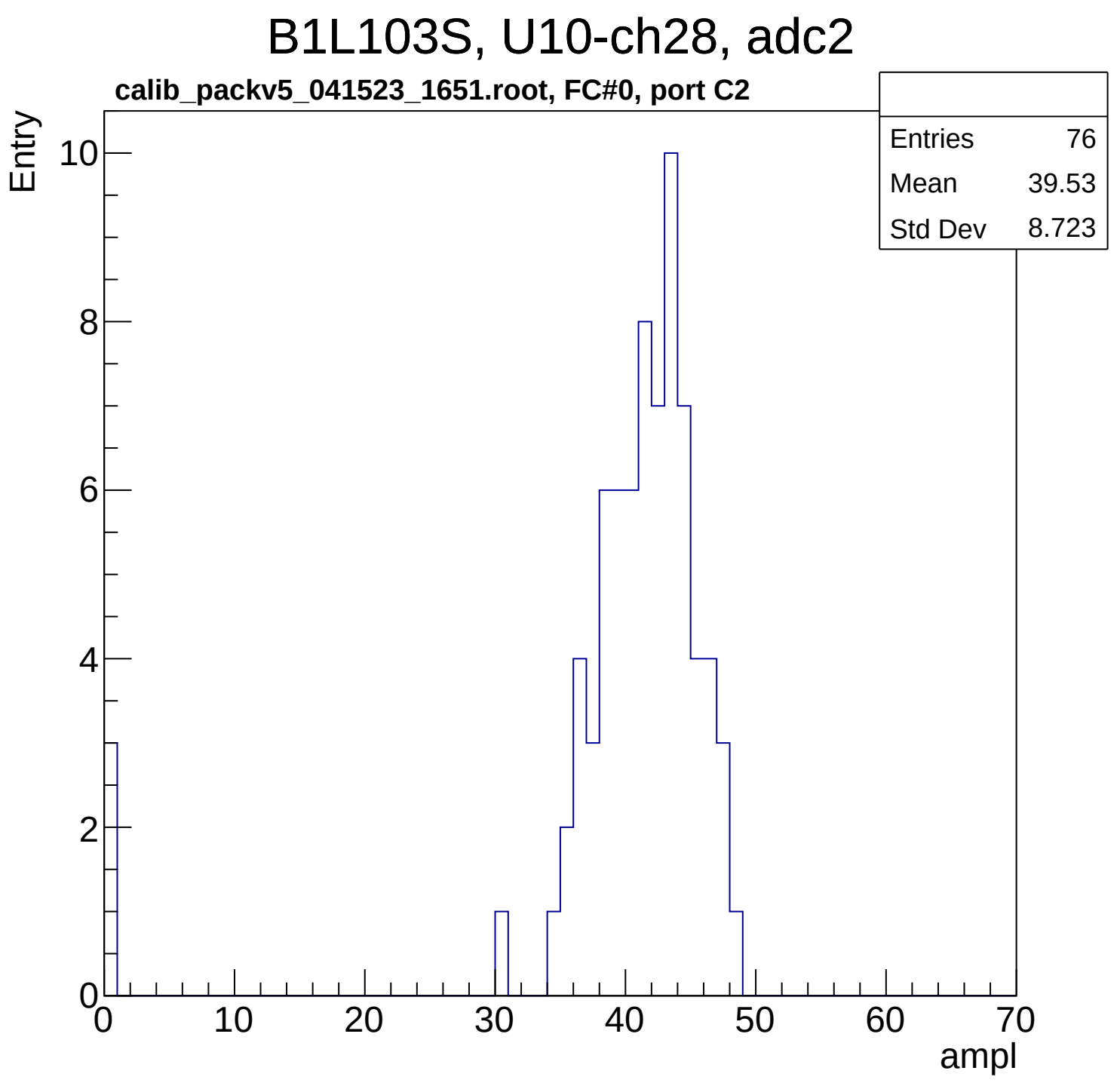
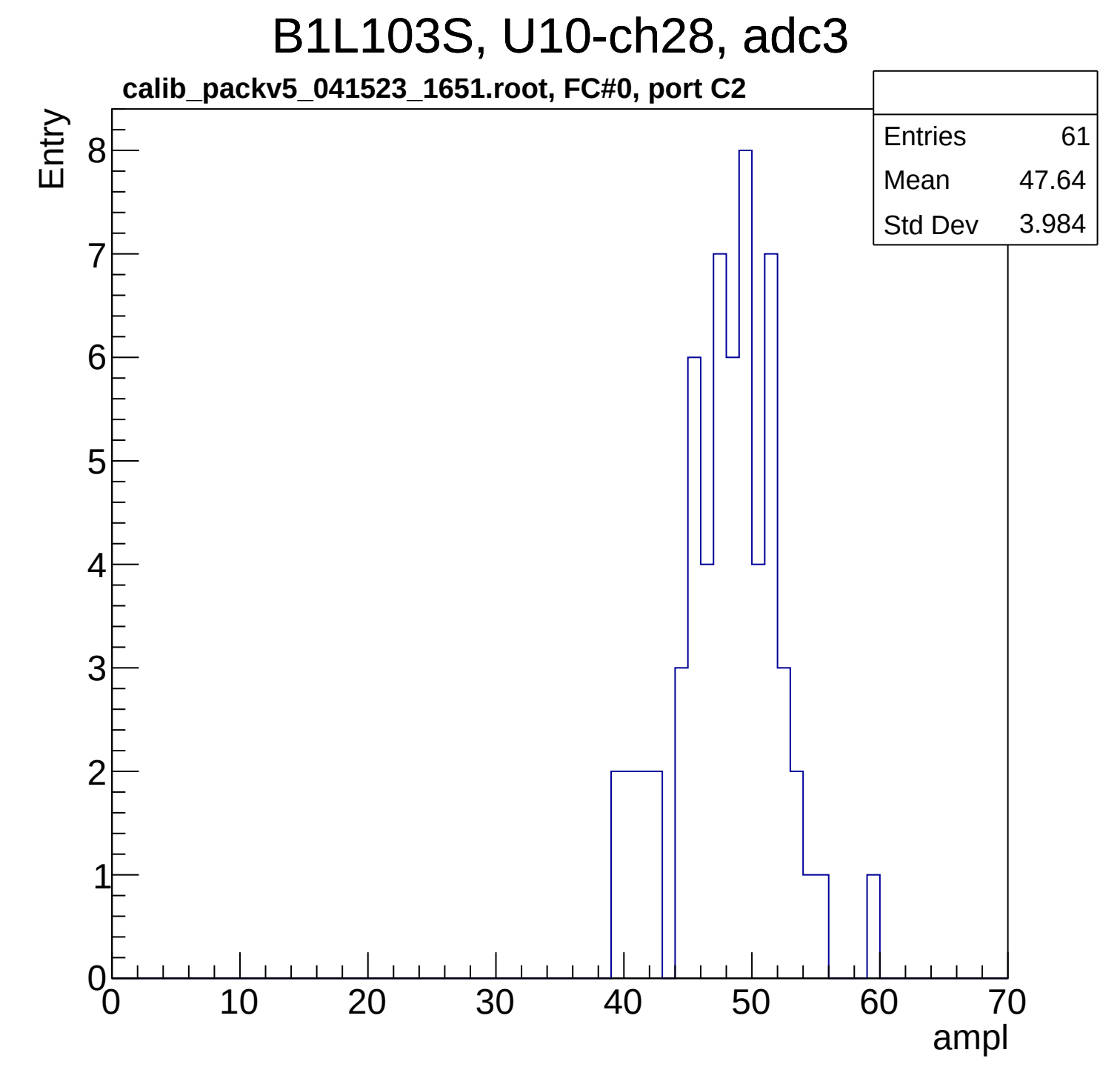
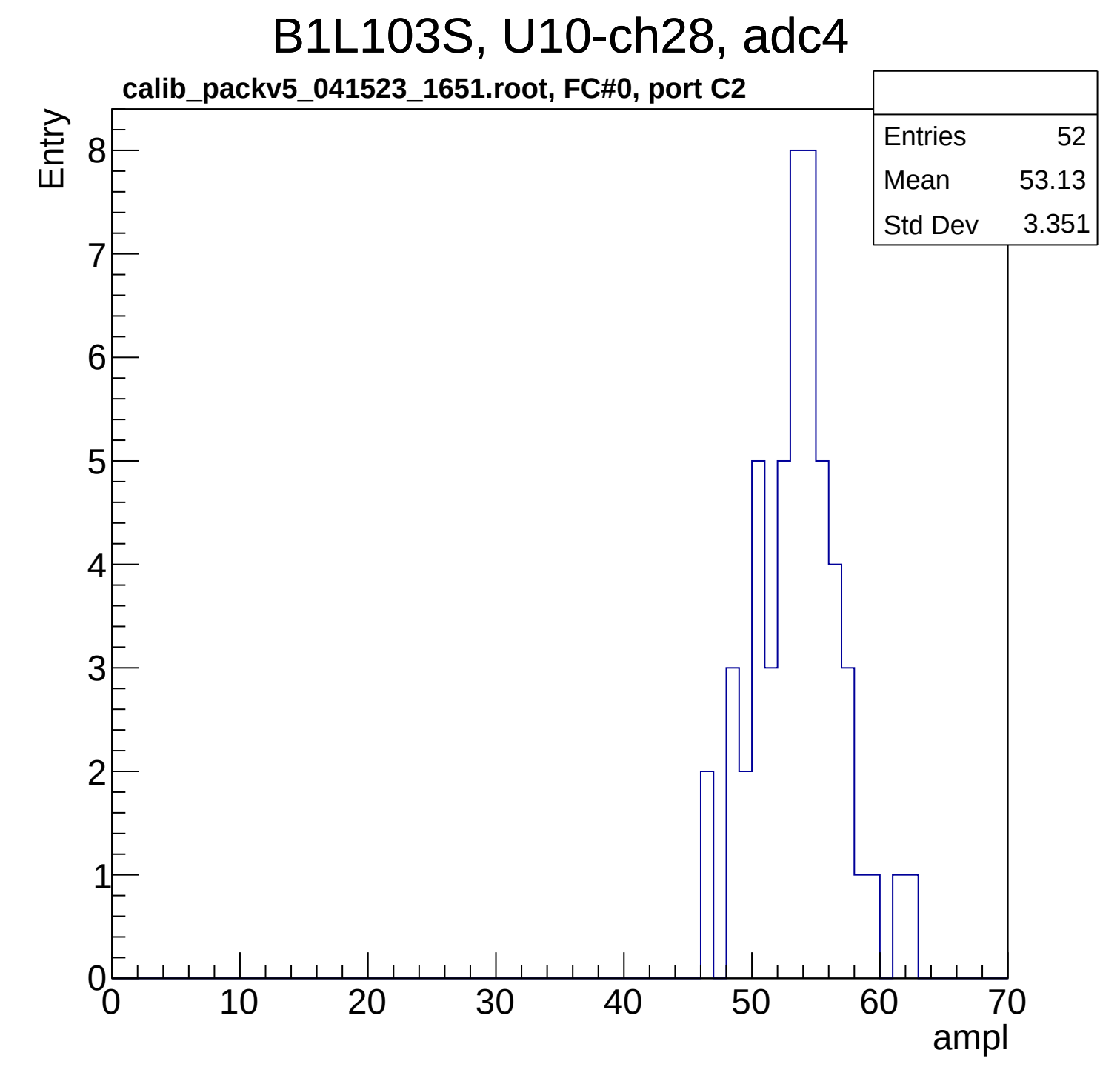
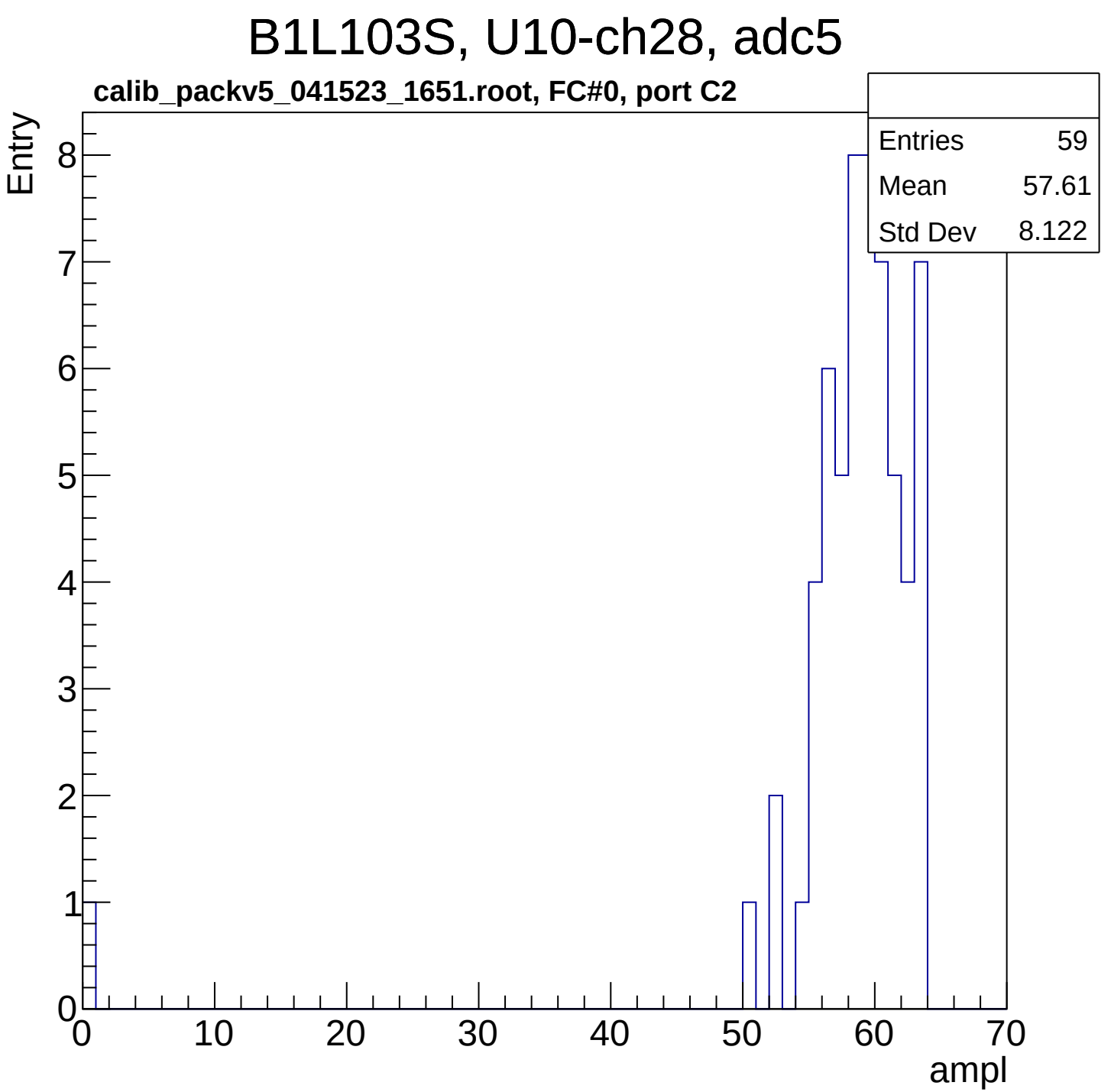
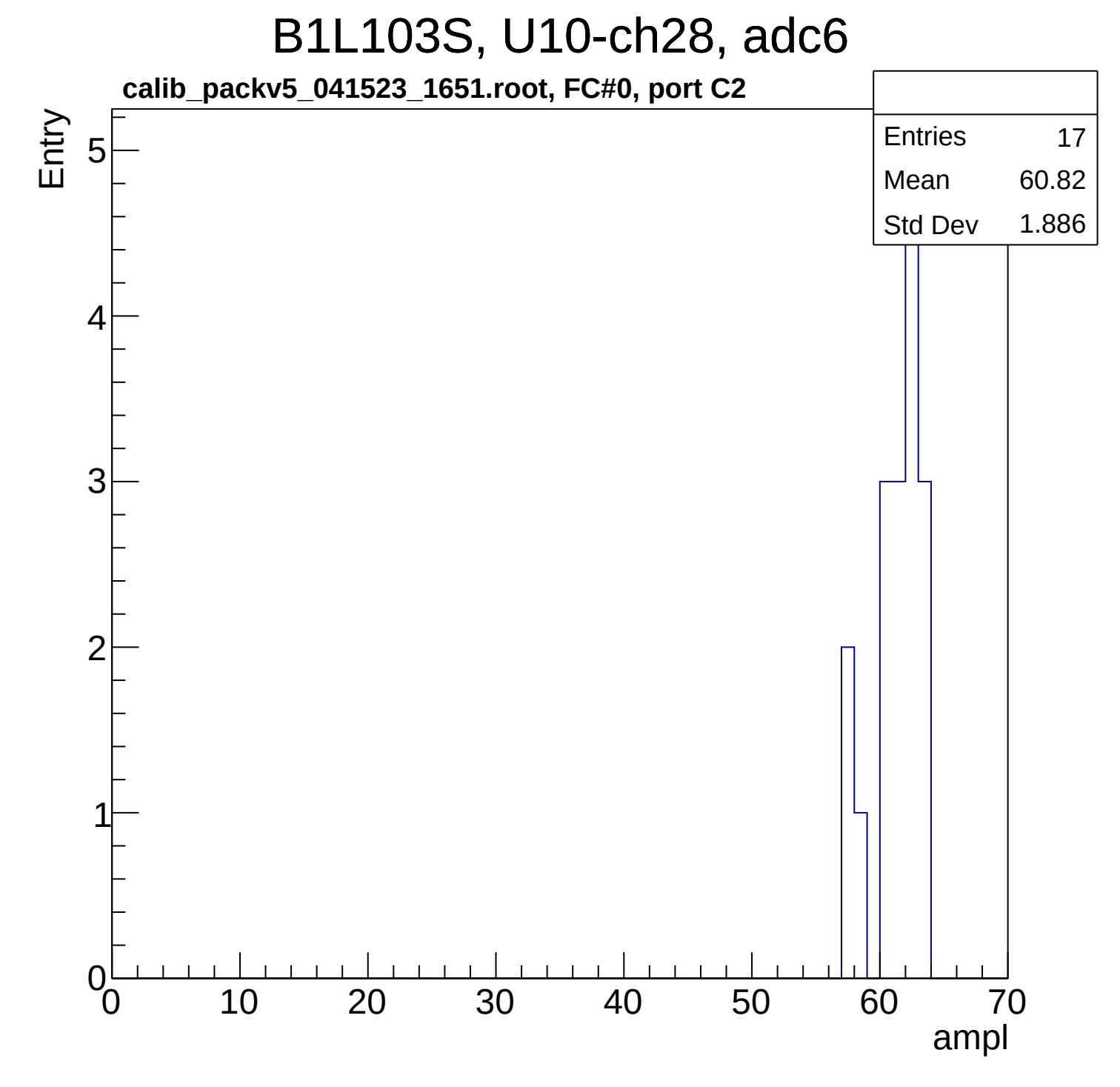

B1L103S, U10-ch28, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 29.32
Std Dev 12.7
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

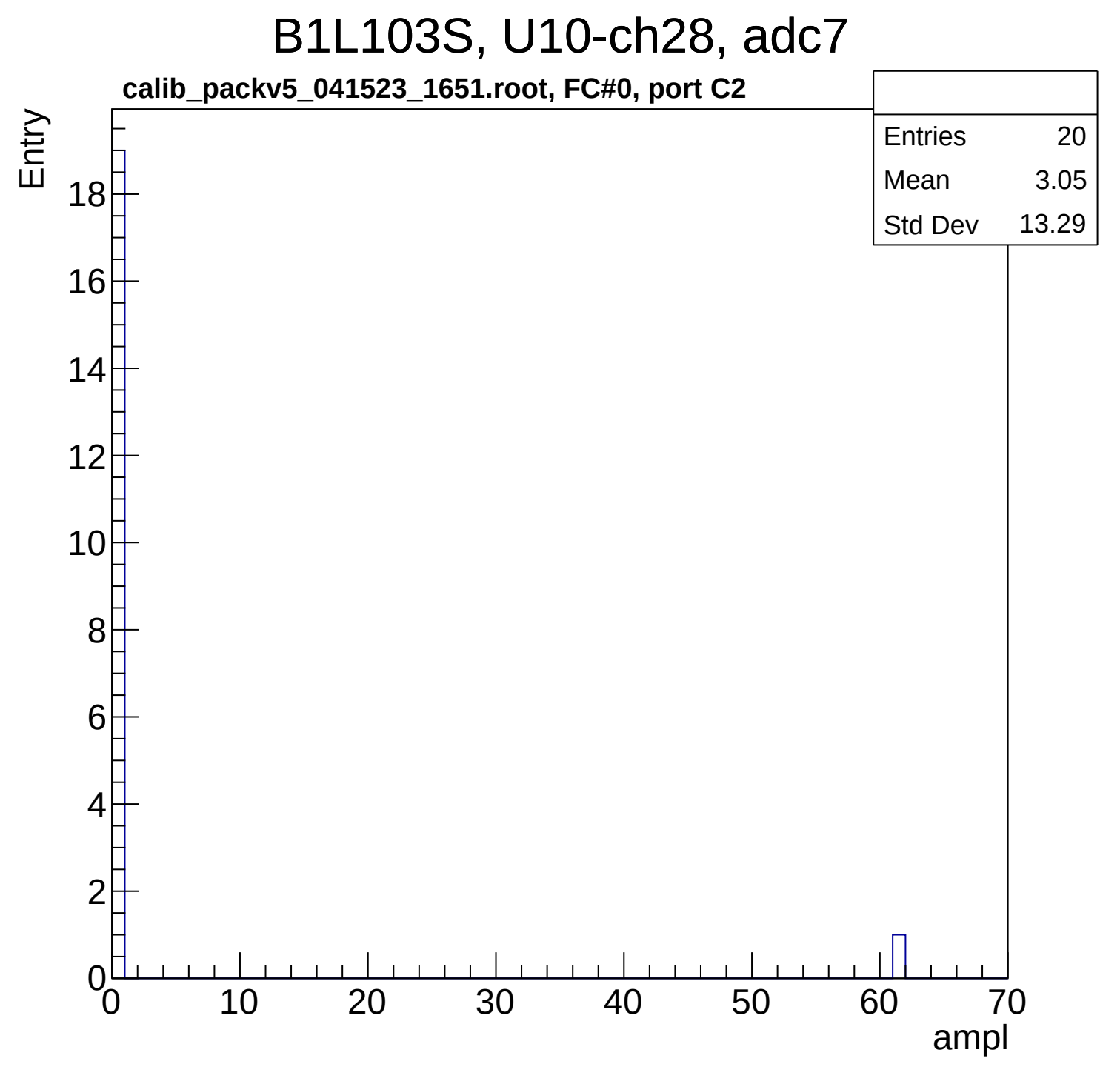

B1L103S, U10-ch28, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 39.53
Std Dev 8.723
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

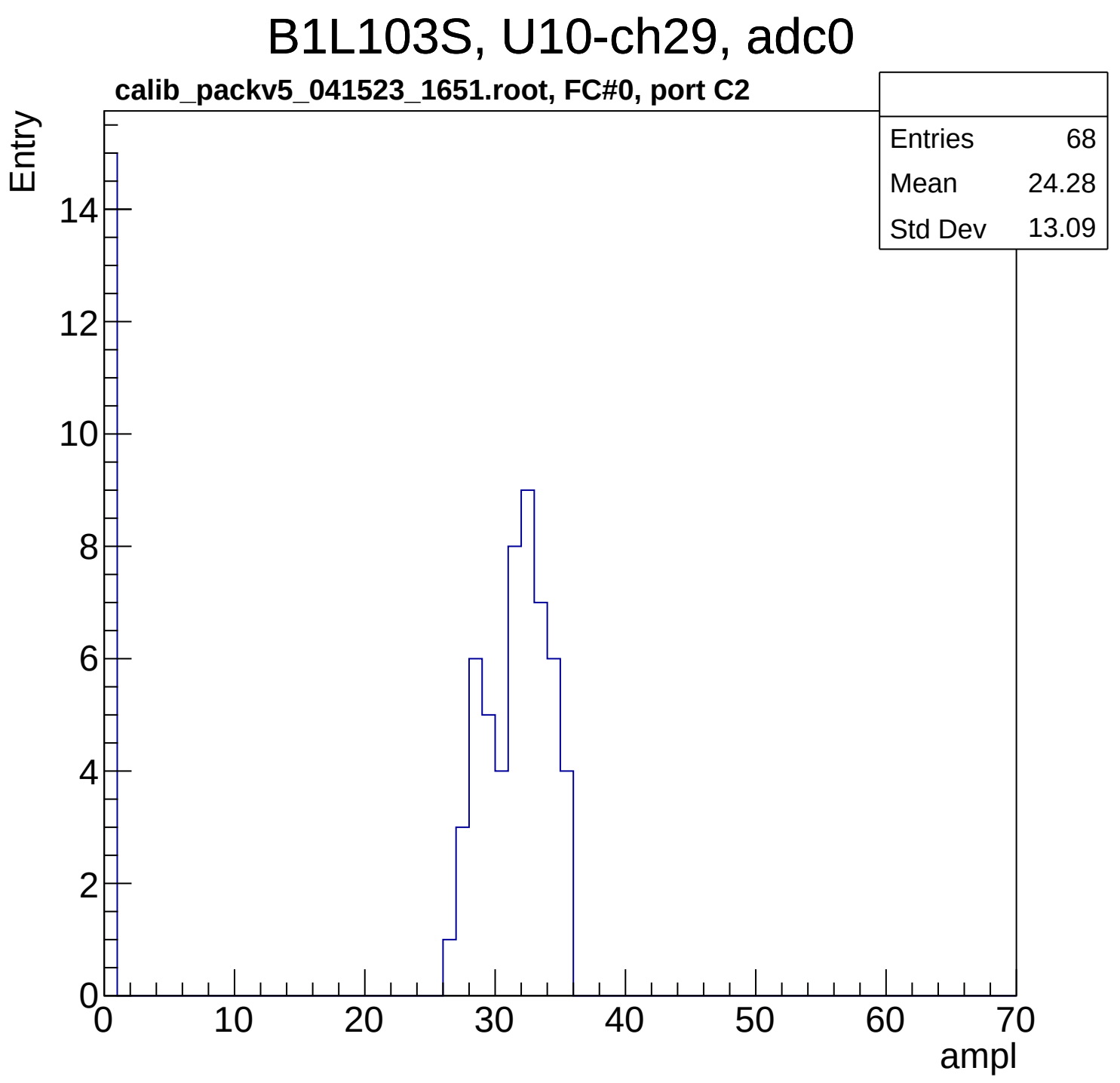

B1L103S, U10-ch28, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 47.64
Std Dev 3.984
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U10-ch28, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 53.13
Std Dev 3.351
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U10-ch28, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 57.61
Std Dev 8.122
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U10-ch28, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 17
Mean 60.82
Std Dev 1.886
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U10-ch28, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.05
Std Dev 13.29
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch29, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 24.28
Std Dev 13.09
Entry
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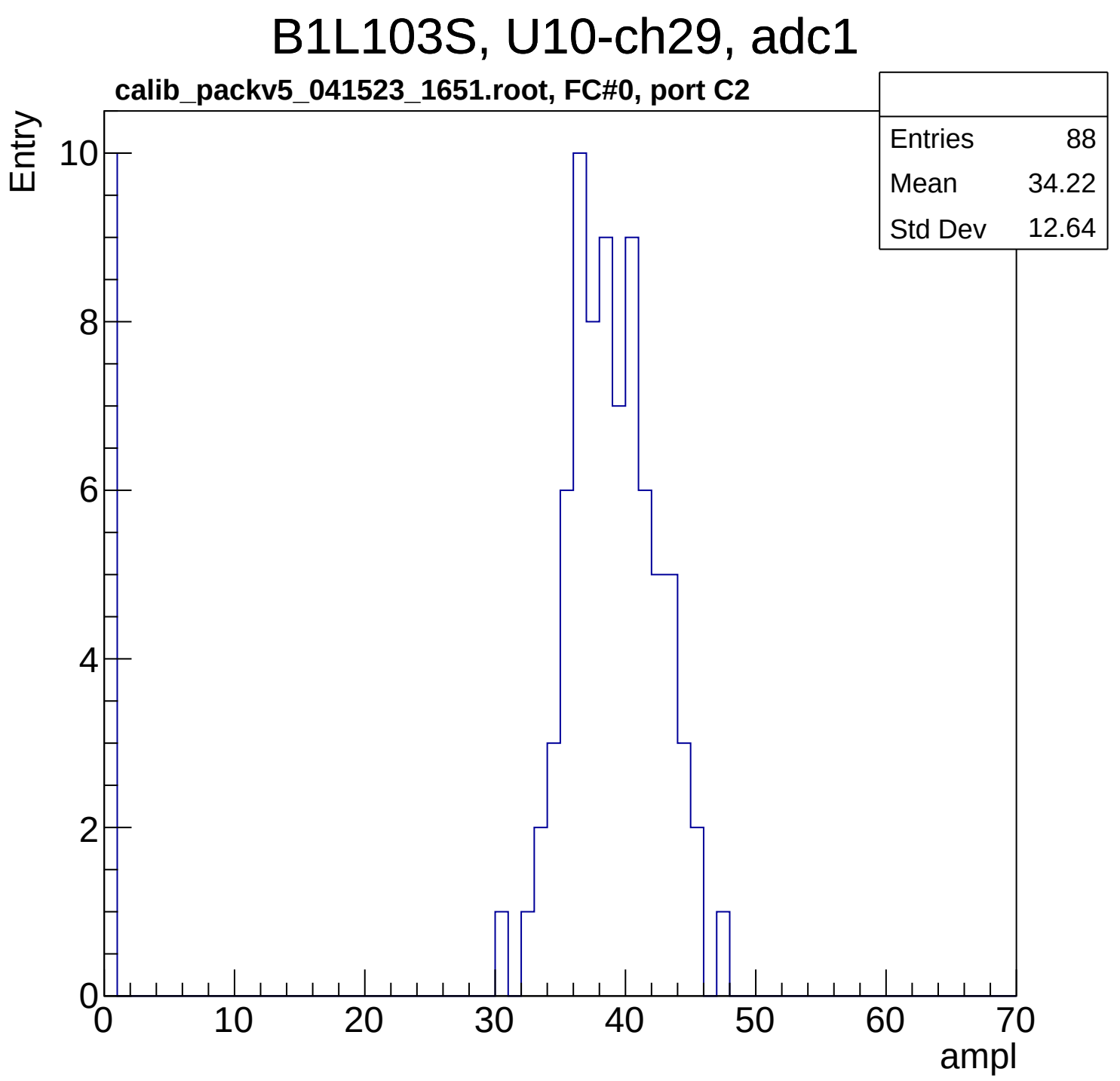
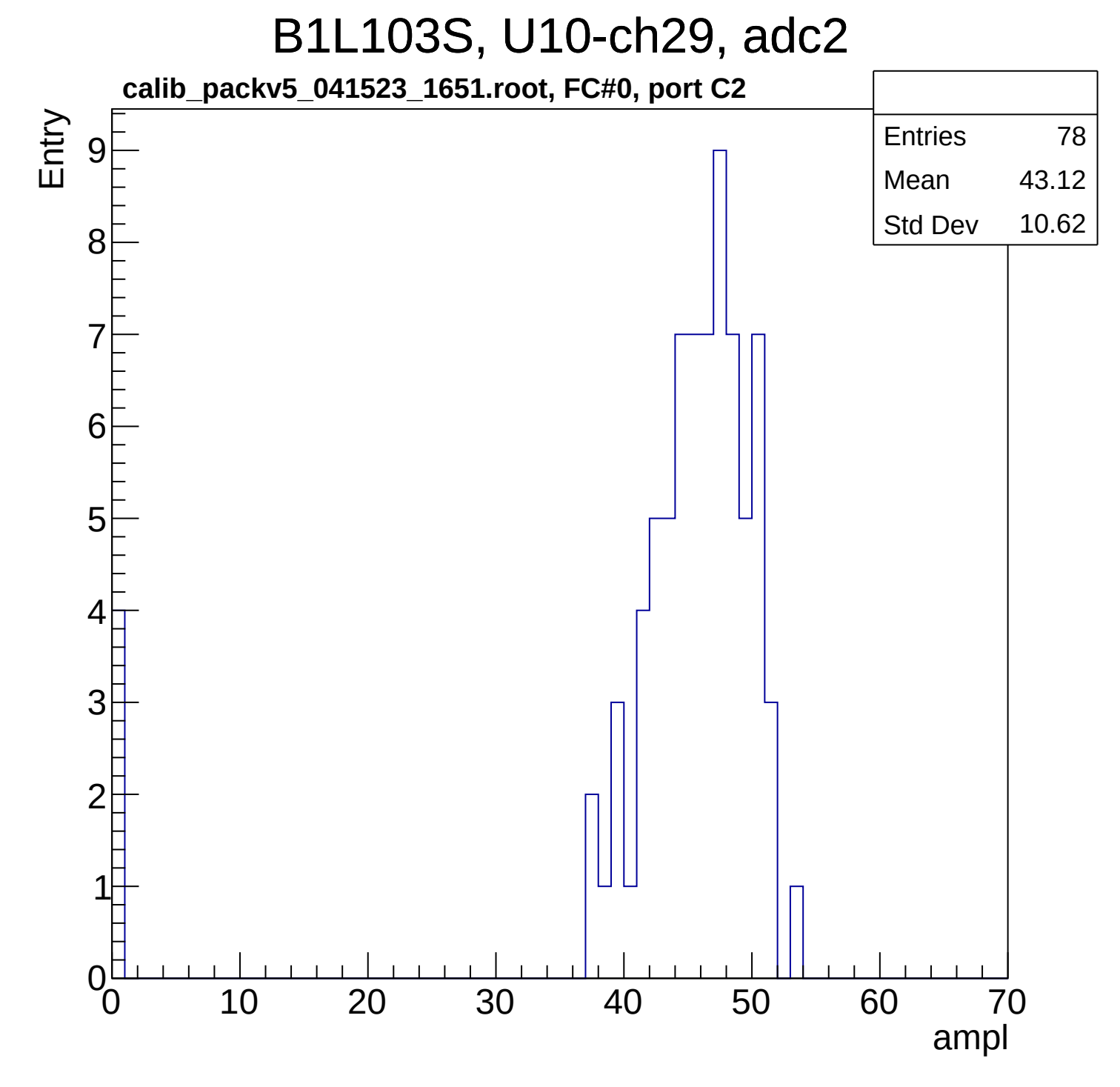
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch29, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 88
Mean 34.22
Std Dev 12.64
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch29, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 43.12
Std Dev 10.62
Entry
ampl
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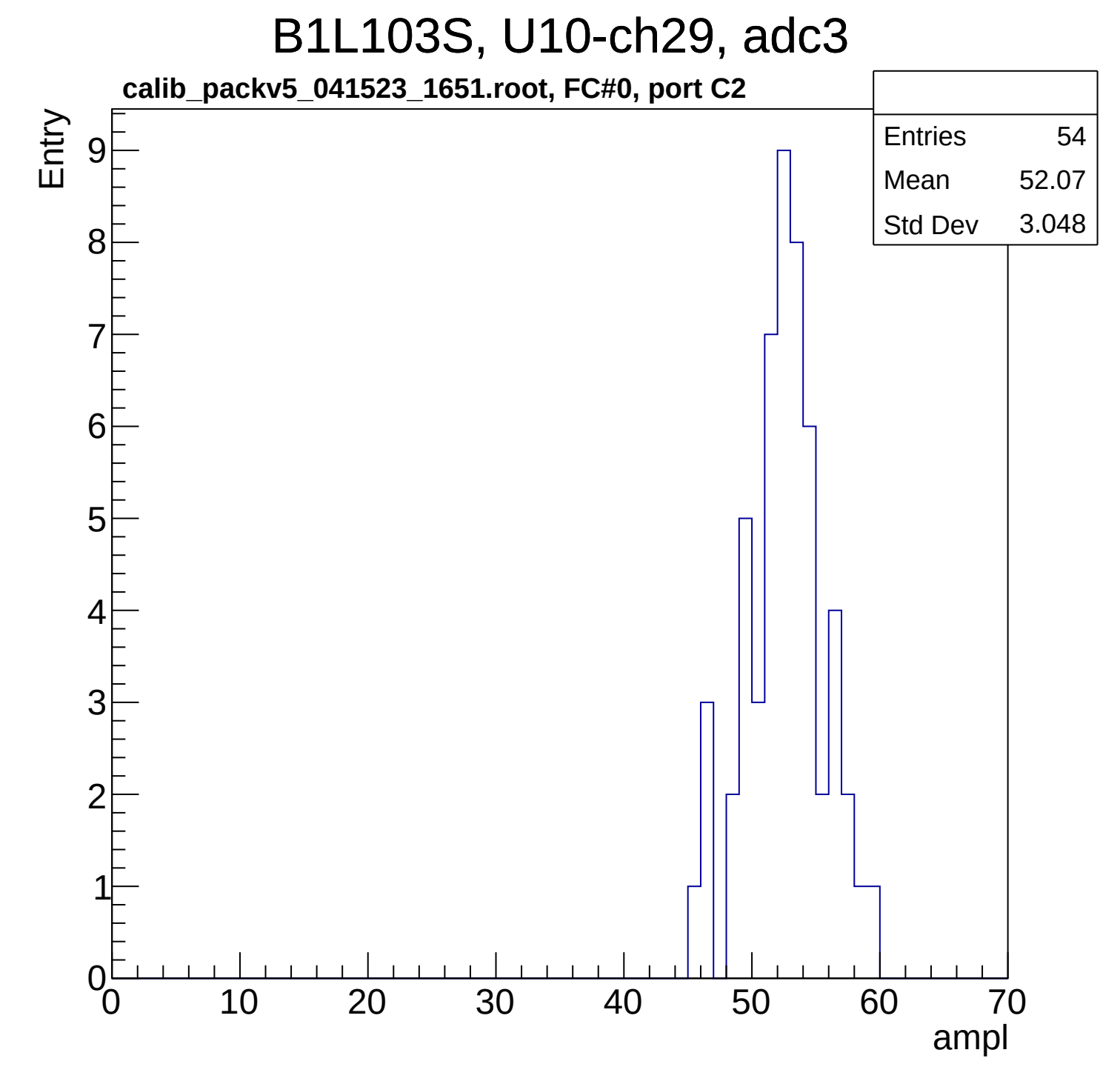
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U10-ch29, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 52.07
Std Dev 3.048
Entry
ampl
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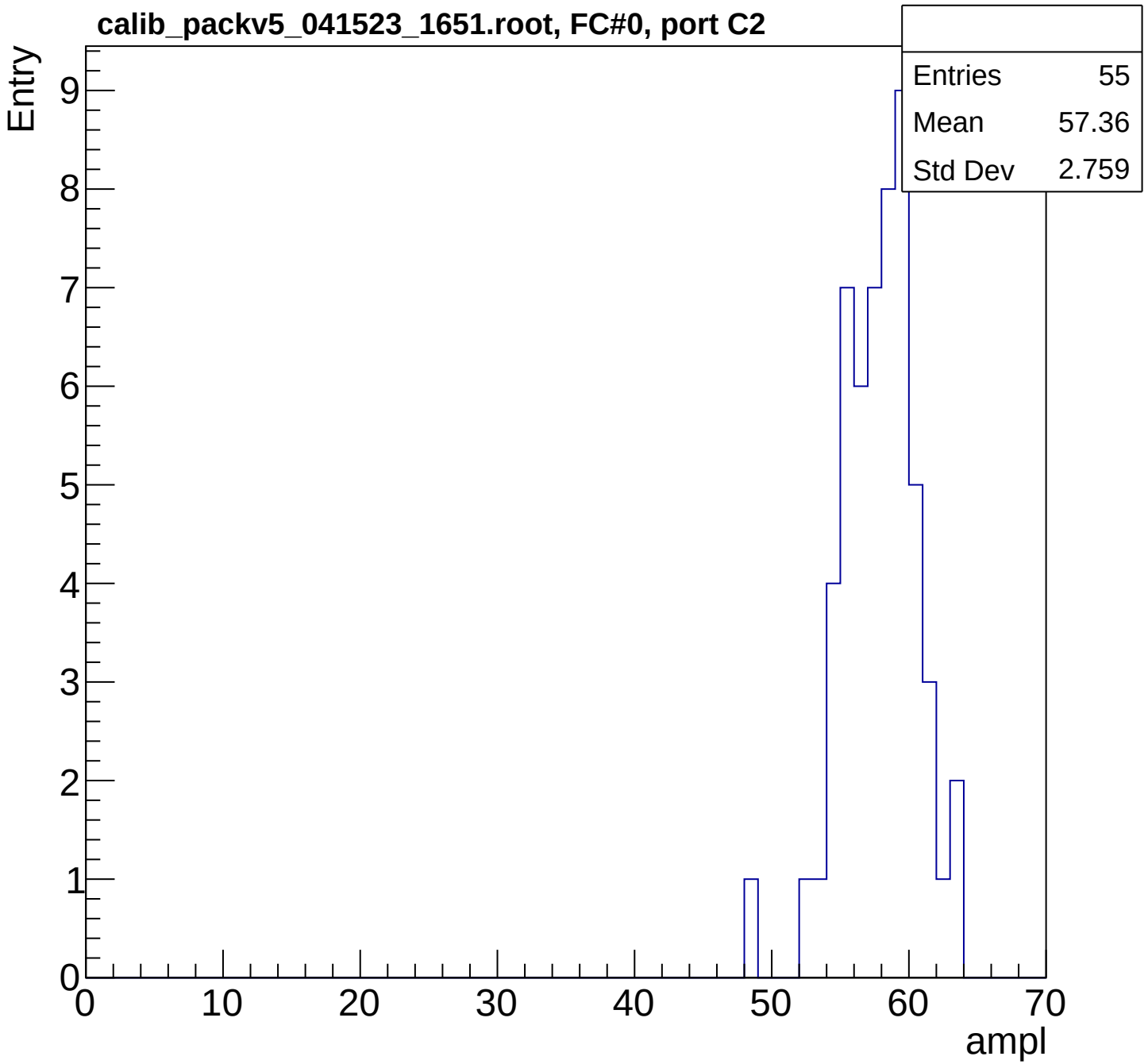
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U10-ch29, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 57.36
Std Dev 2.759
Entry
ampl
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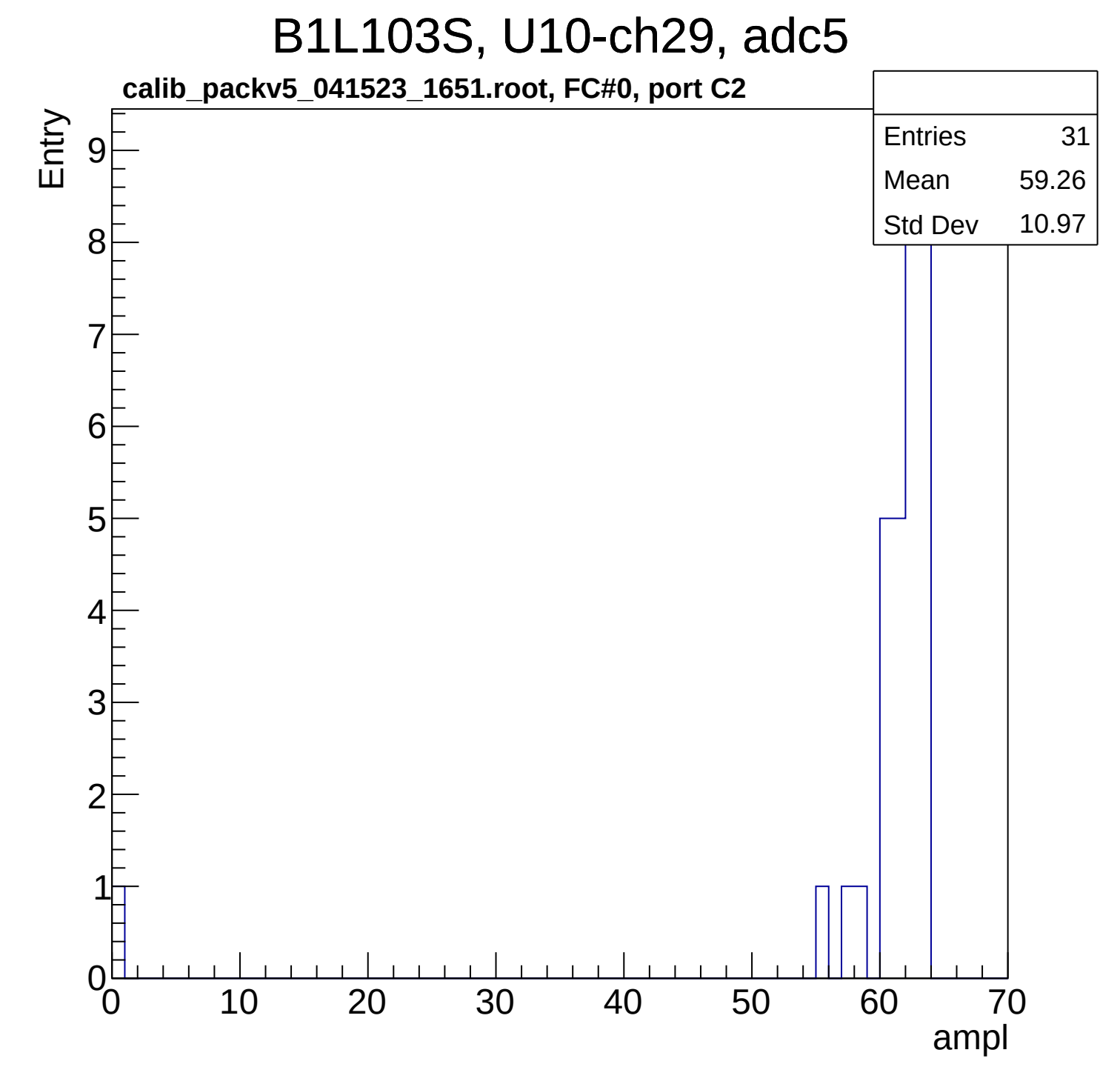
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U10-ch29, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 31
Mean 59.26
Std Dev 10.97
Entry
ampl
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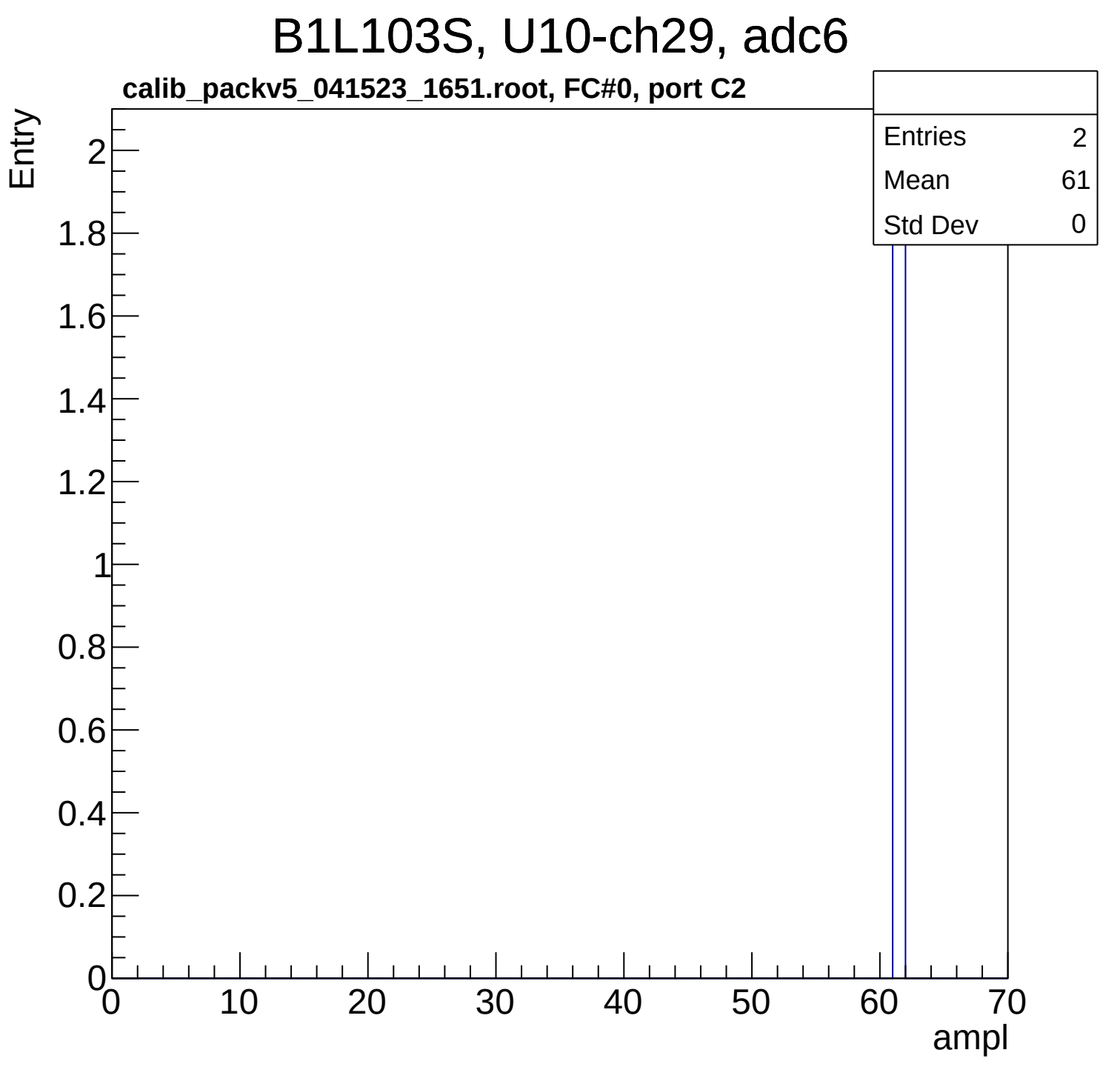
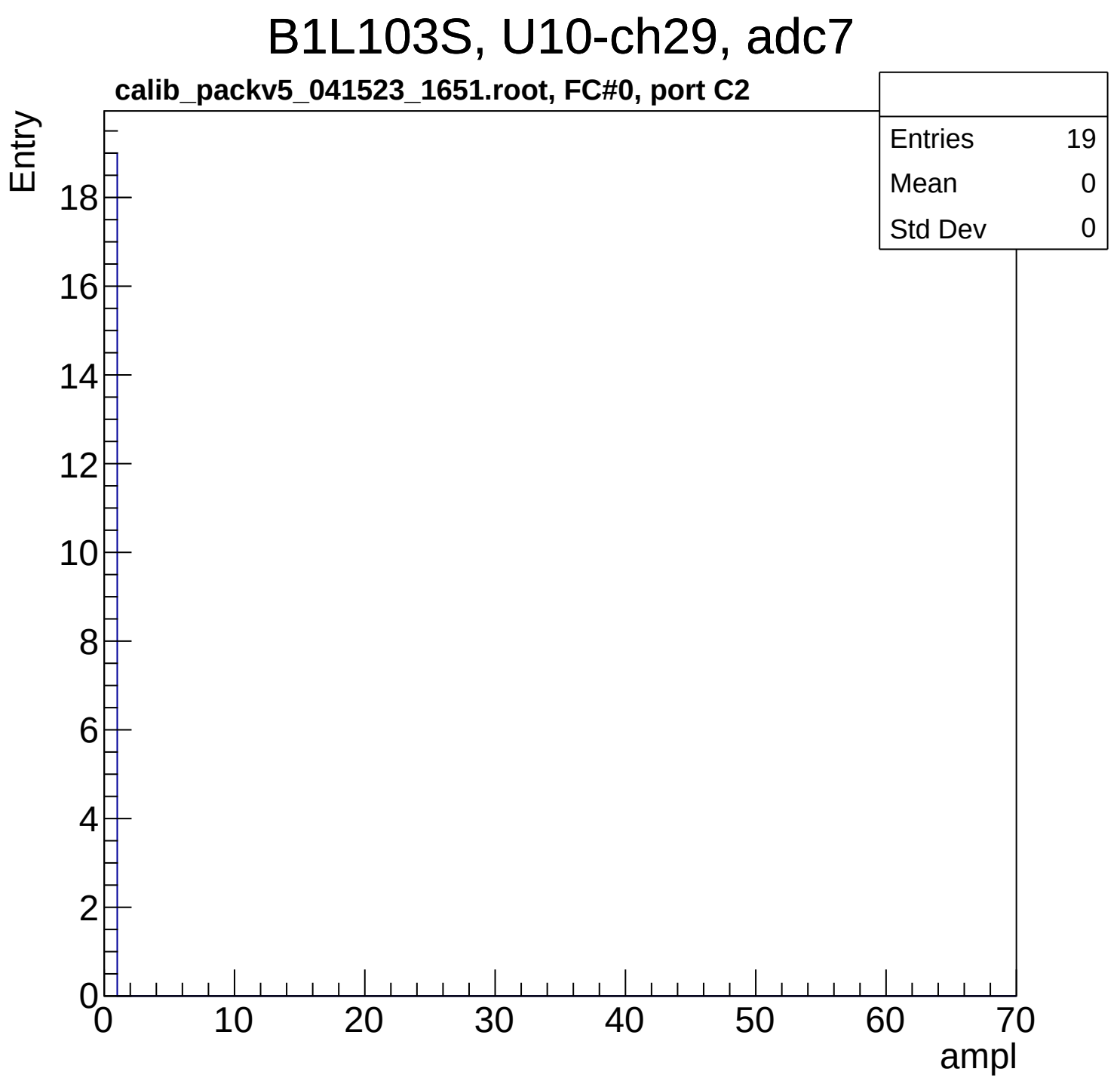
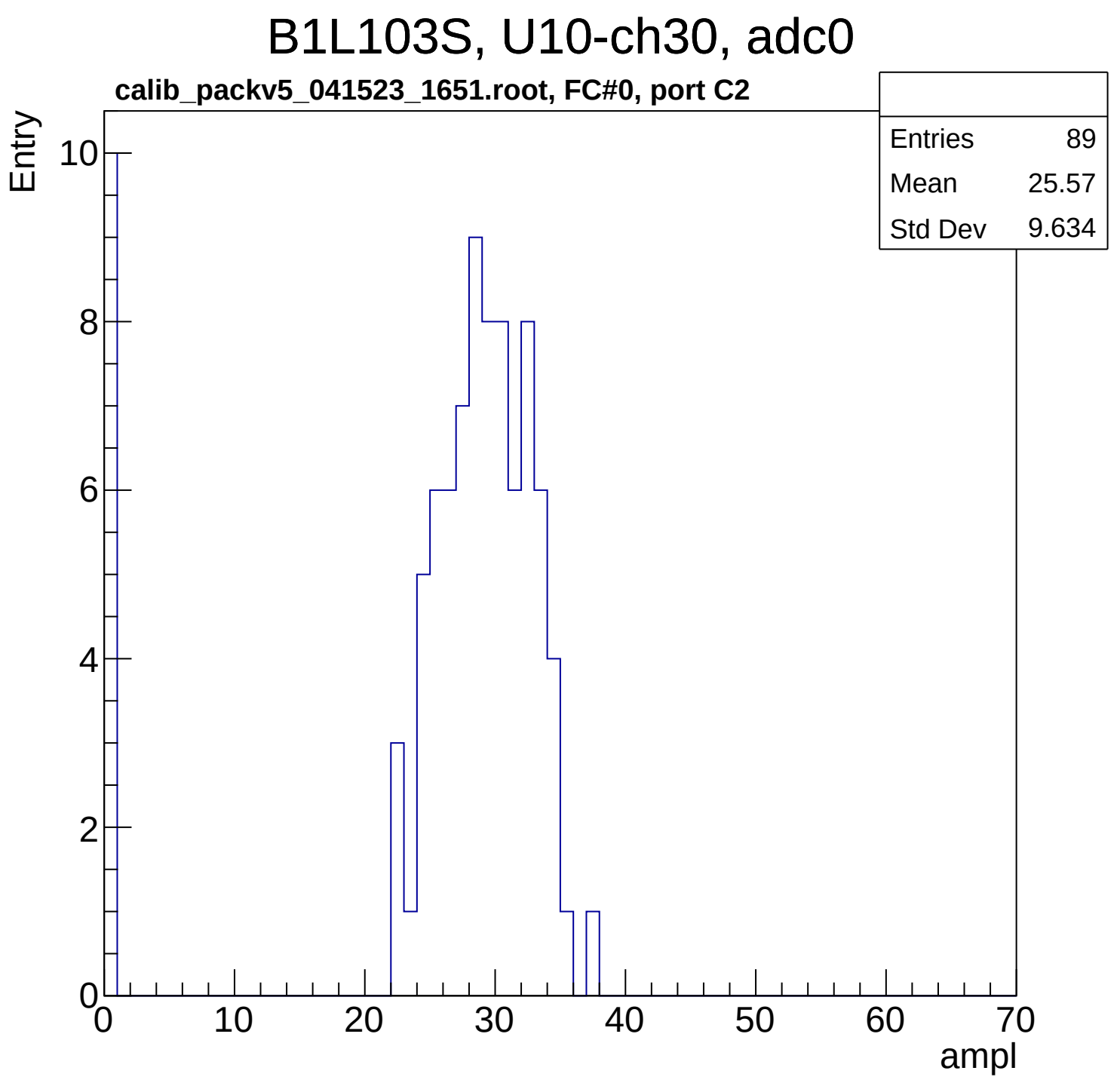
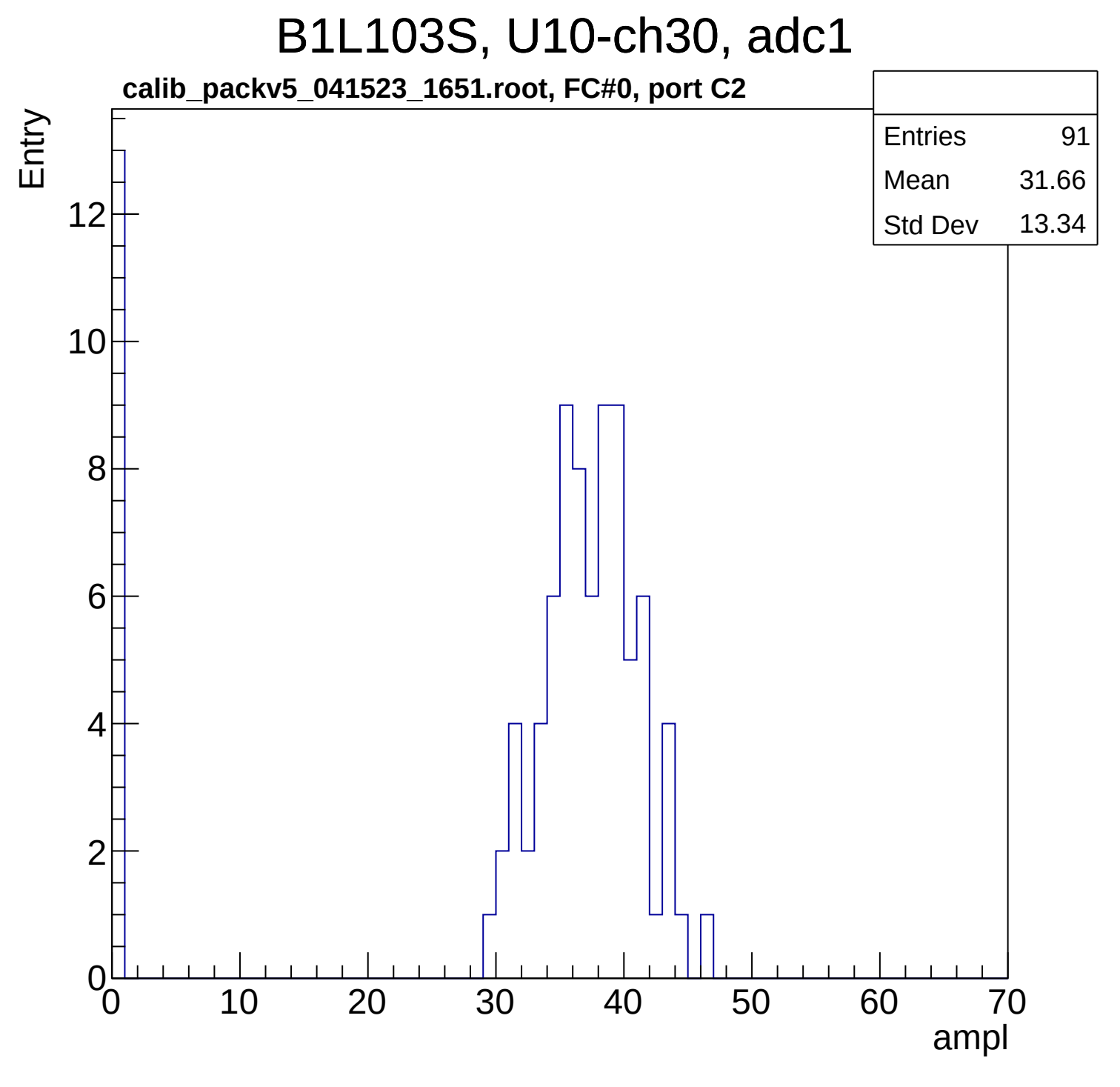
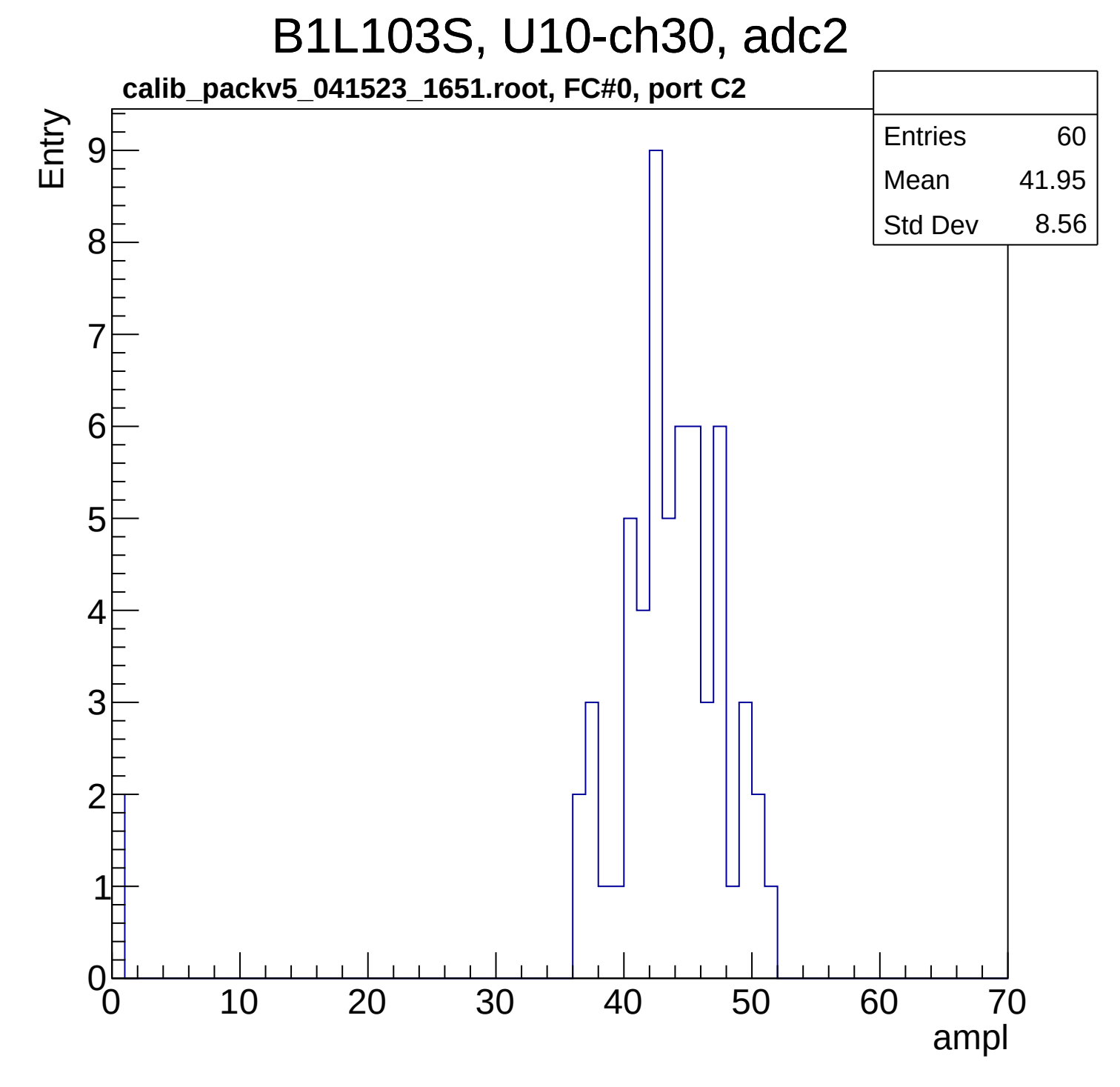
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U10-ch29, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 2
Mean 61
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U10-ch29, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch30, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 89
Mean 25.57
Std Dev 9.634
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U10-ch30, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 91
Mean 31.66
Std Dev 13.34
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch30, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 41.95
Std Dev 8.56
Entry
ampl
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10
20
30
40
50
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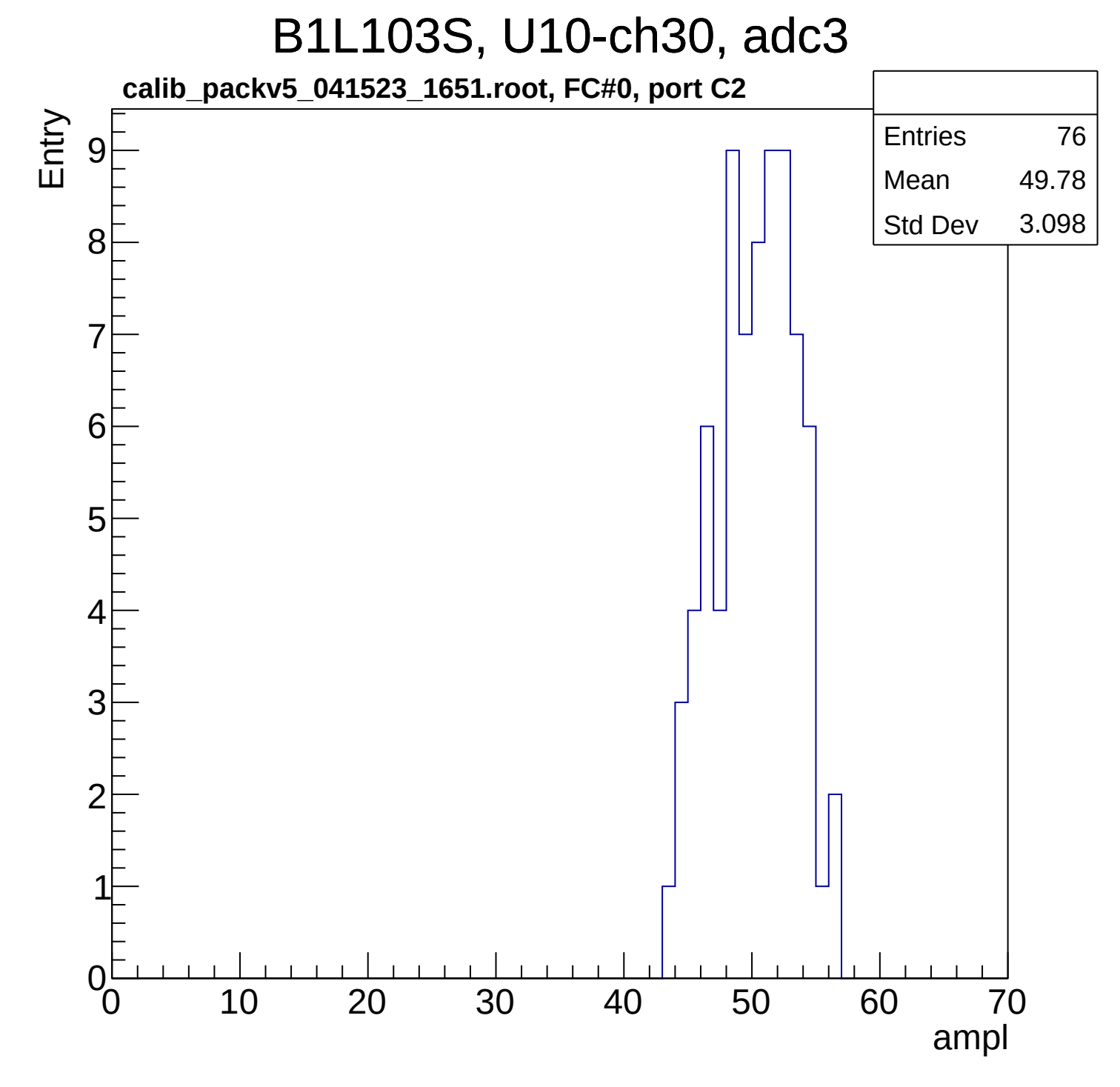
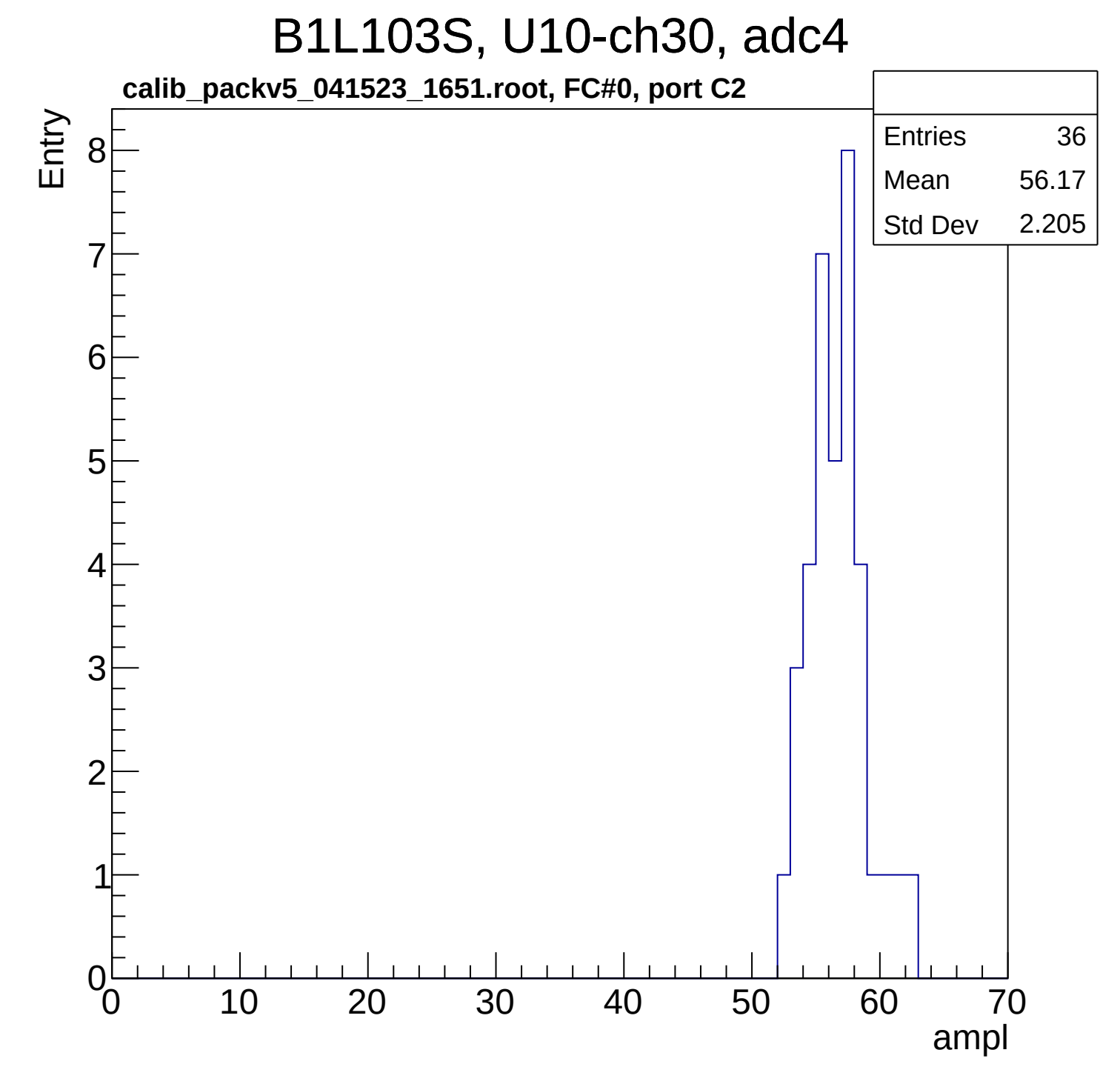
70
1
2
3
4
5
6
7
8
9


B1L103S, U10-ch30, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 49.78
Std Dev 3.098
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U10-ch30, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 36
Mean 56.17
Std Dev 2.205
Entry
ampl
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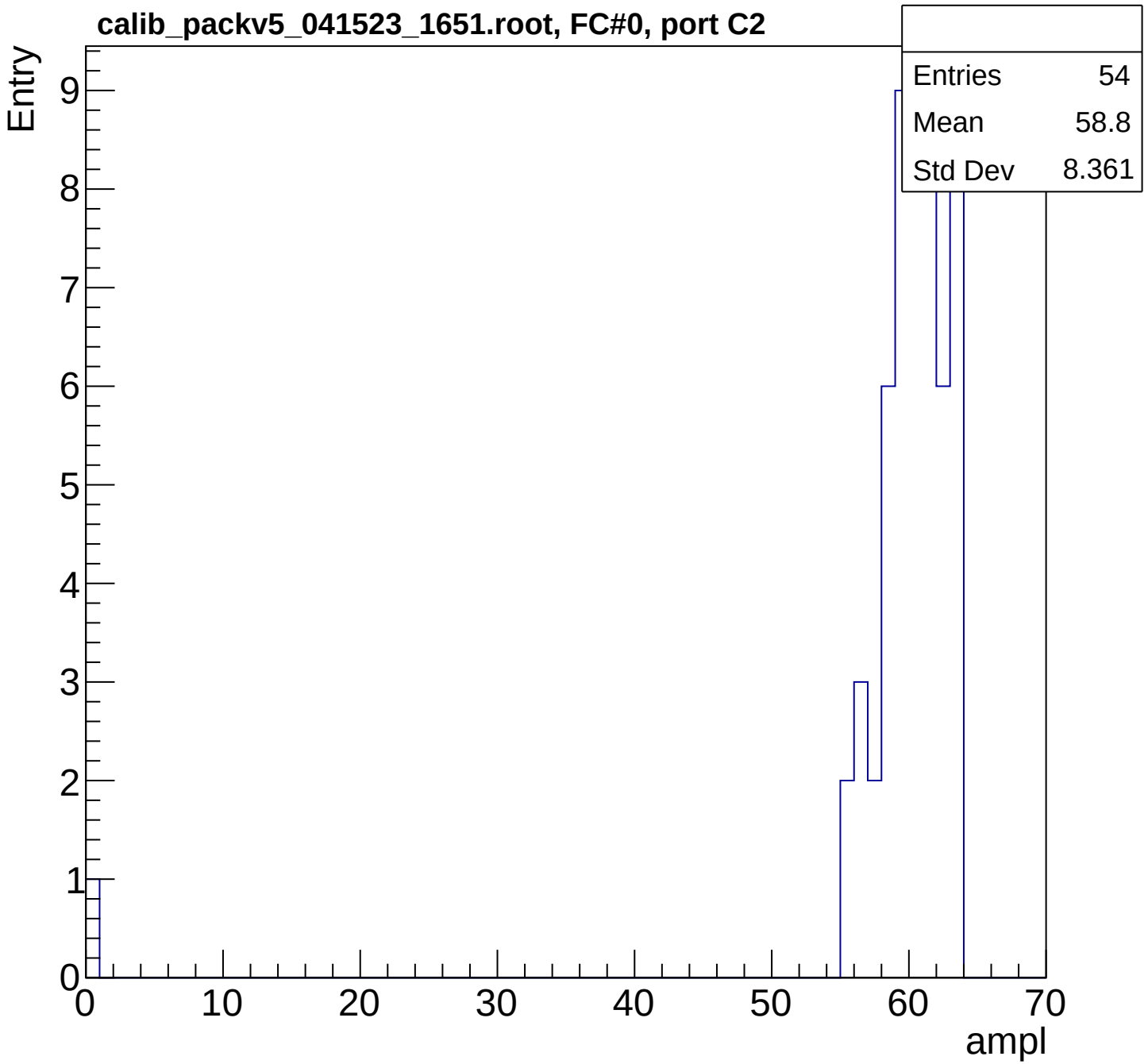
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U10-ch30, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 58.8
Std Dev 8.361
Entry
ampl
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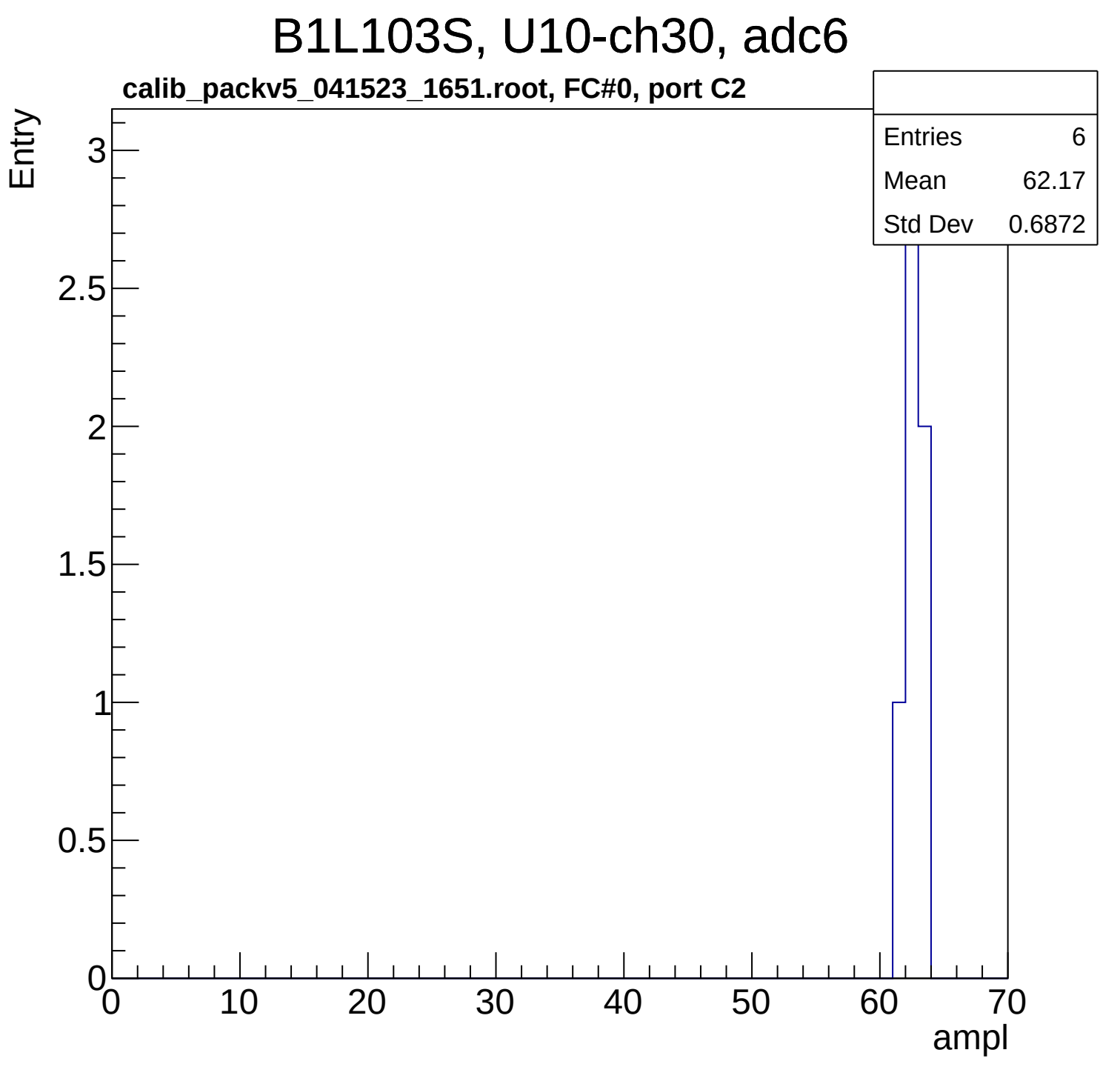
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U10-ch30, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 62.17
Std Dev 0.6872
Entry
ampl
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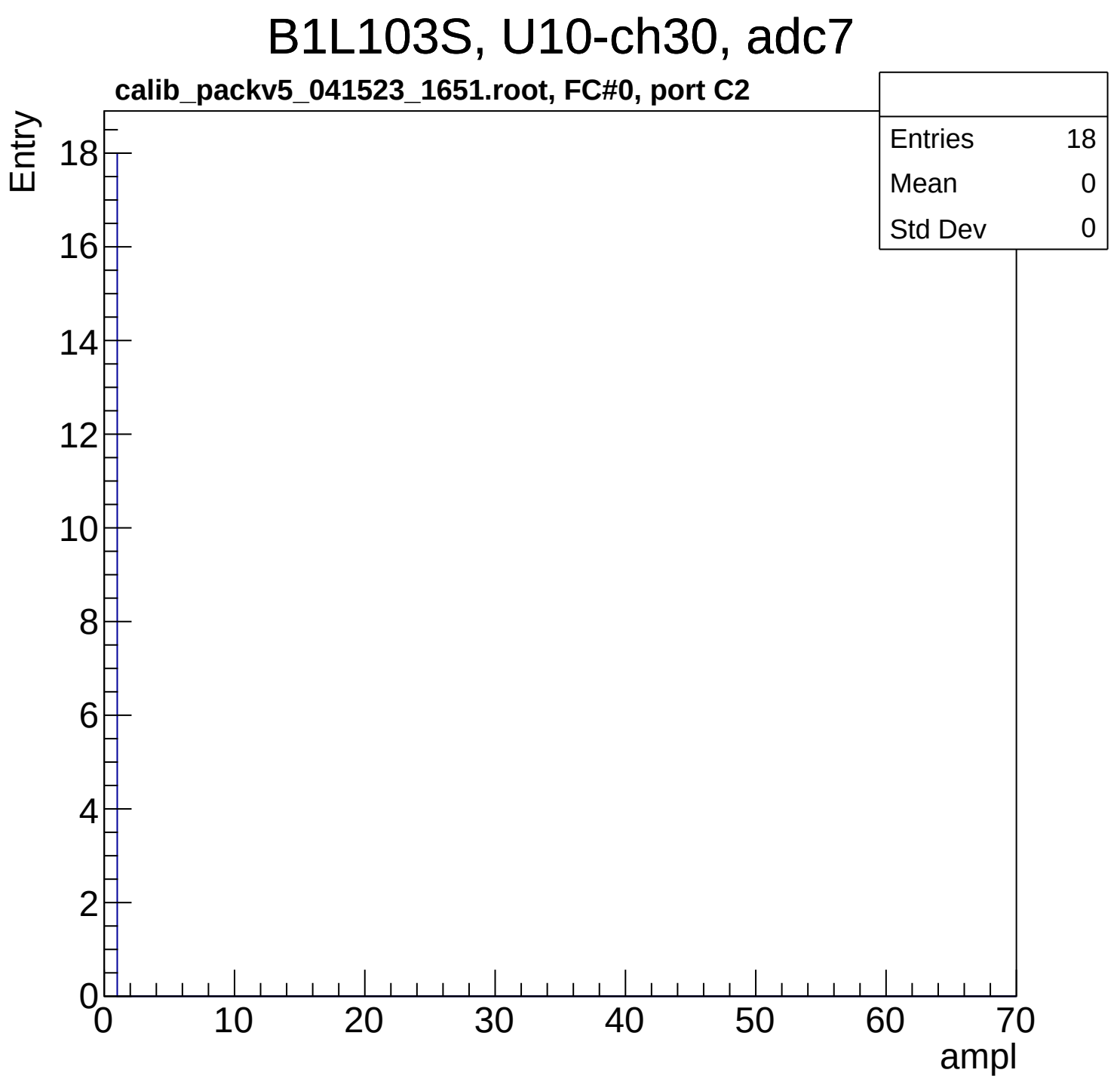
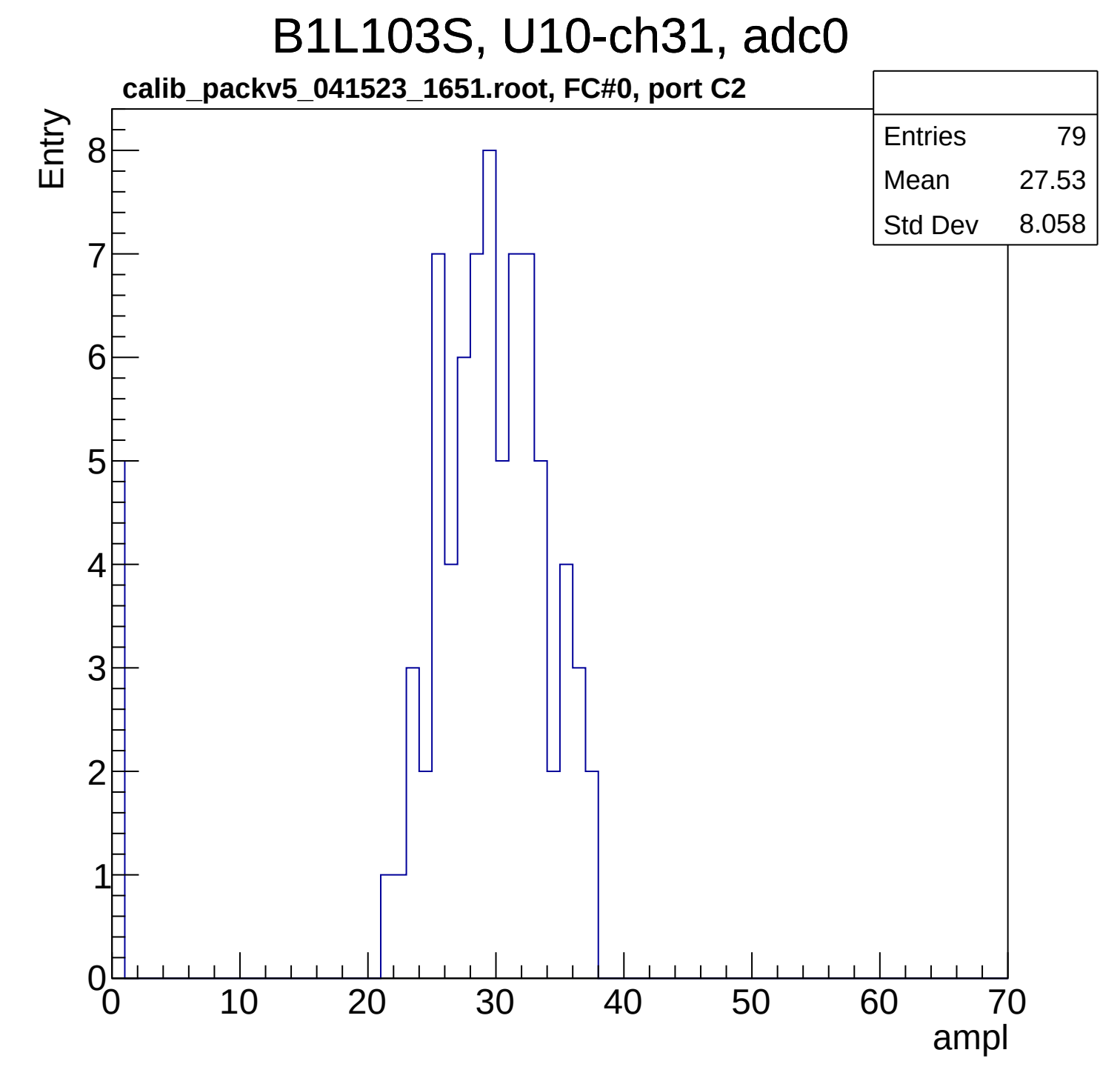
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U10-ch30, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch31, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 27.53
Std Dev 8.058
Entry
ampl
0
1
2
3
4
5
6
7
8
0
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20
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40
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60
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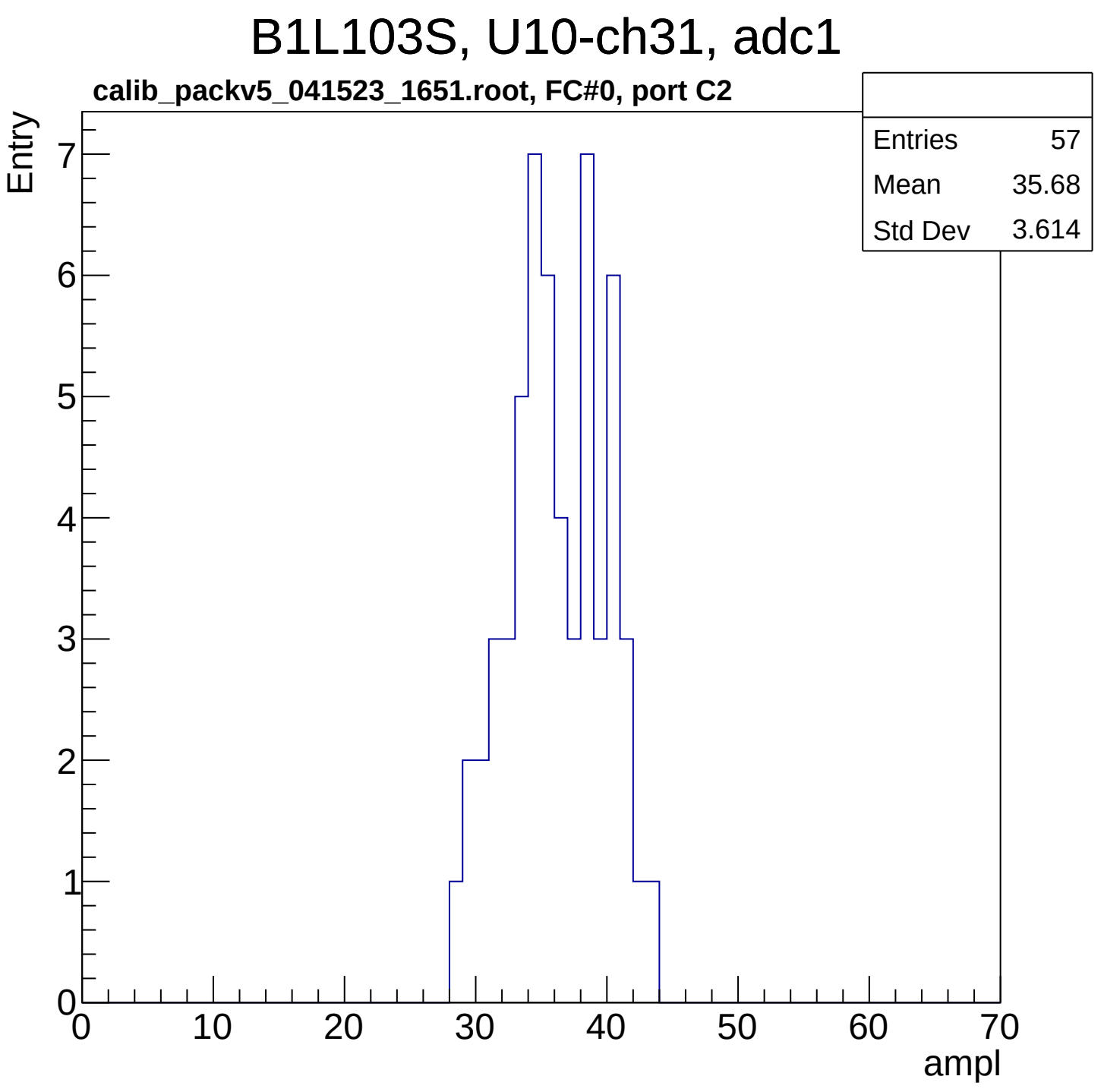
B1L103S, U10-ch31, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 35.68
Std Dev 3.614
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
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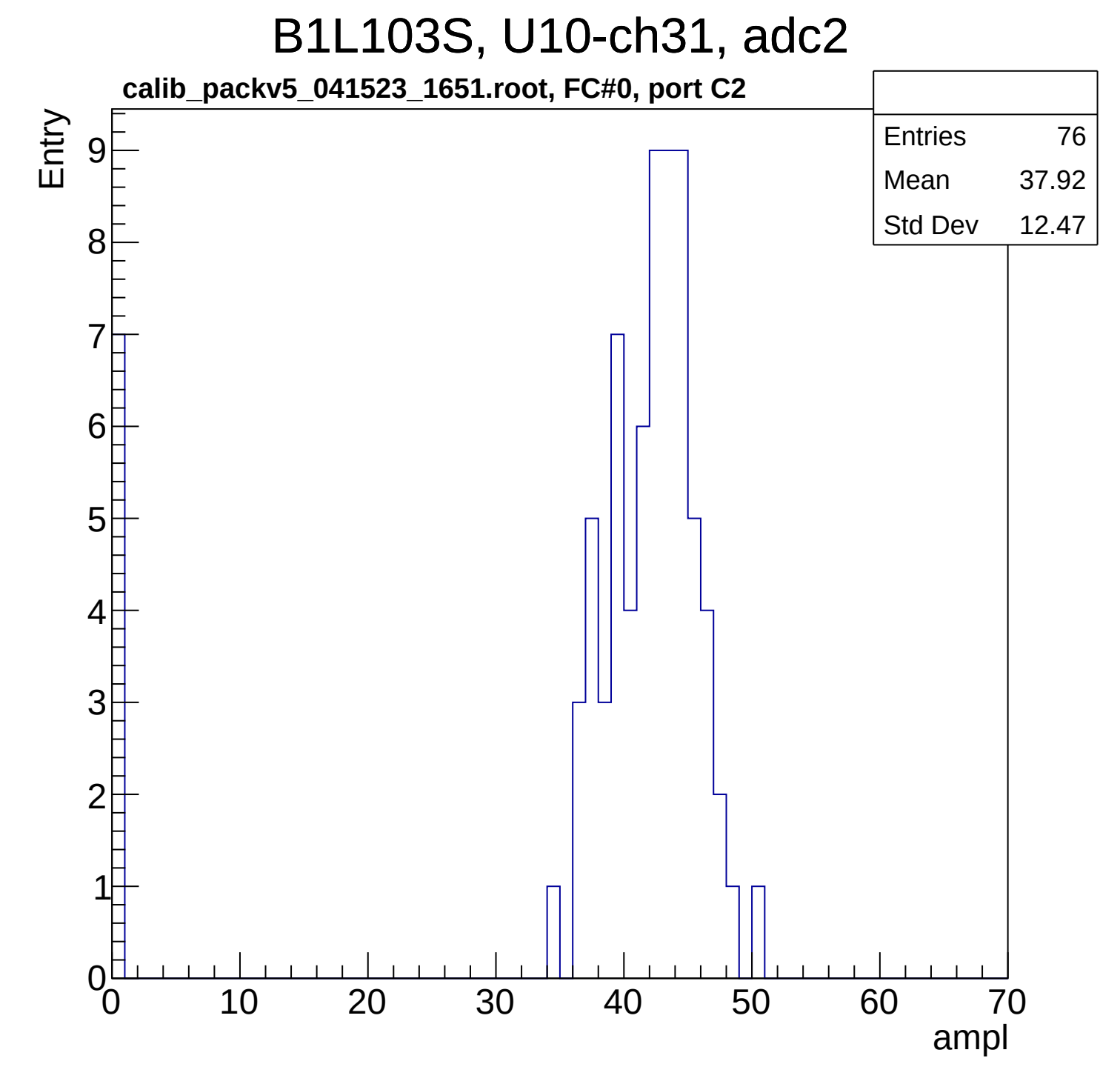
40
50
60
70


B1L103S, U10-ch31, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 37.92
Std Dev 12.47
Entry
ampl
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2
3
4
5
6
7
8
9
0
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40
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60
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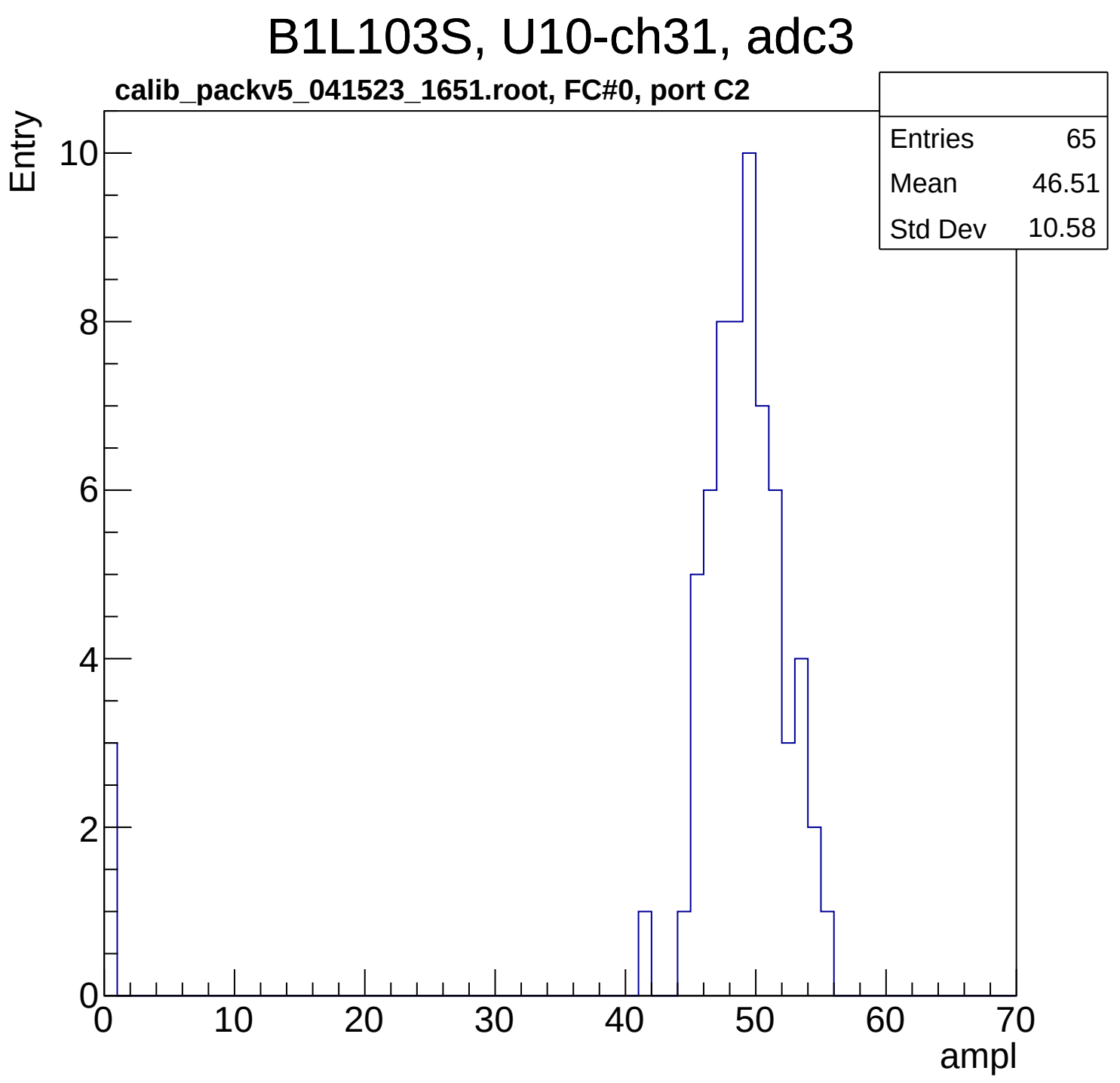
B1L103S, U10-ch31, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 46.51
Std Dev 10.58
Entry
ampl
0
2
4
6
8
10
0
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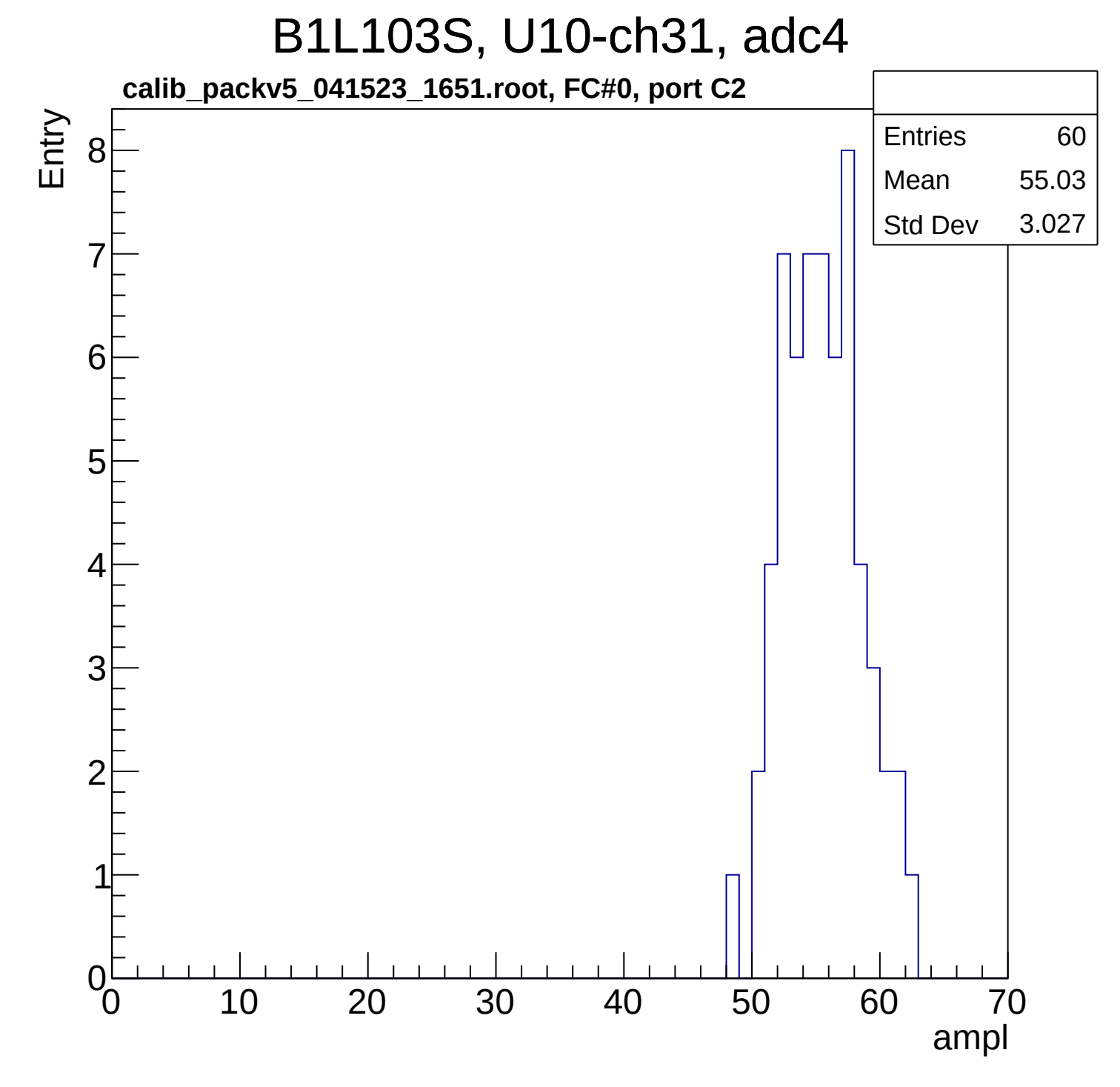
20
30
40
50
60
70


B1L103S, U10-ch31, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 55.03
Std Dev 3.027
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
30
40
50
60
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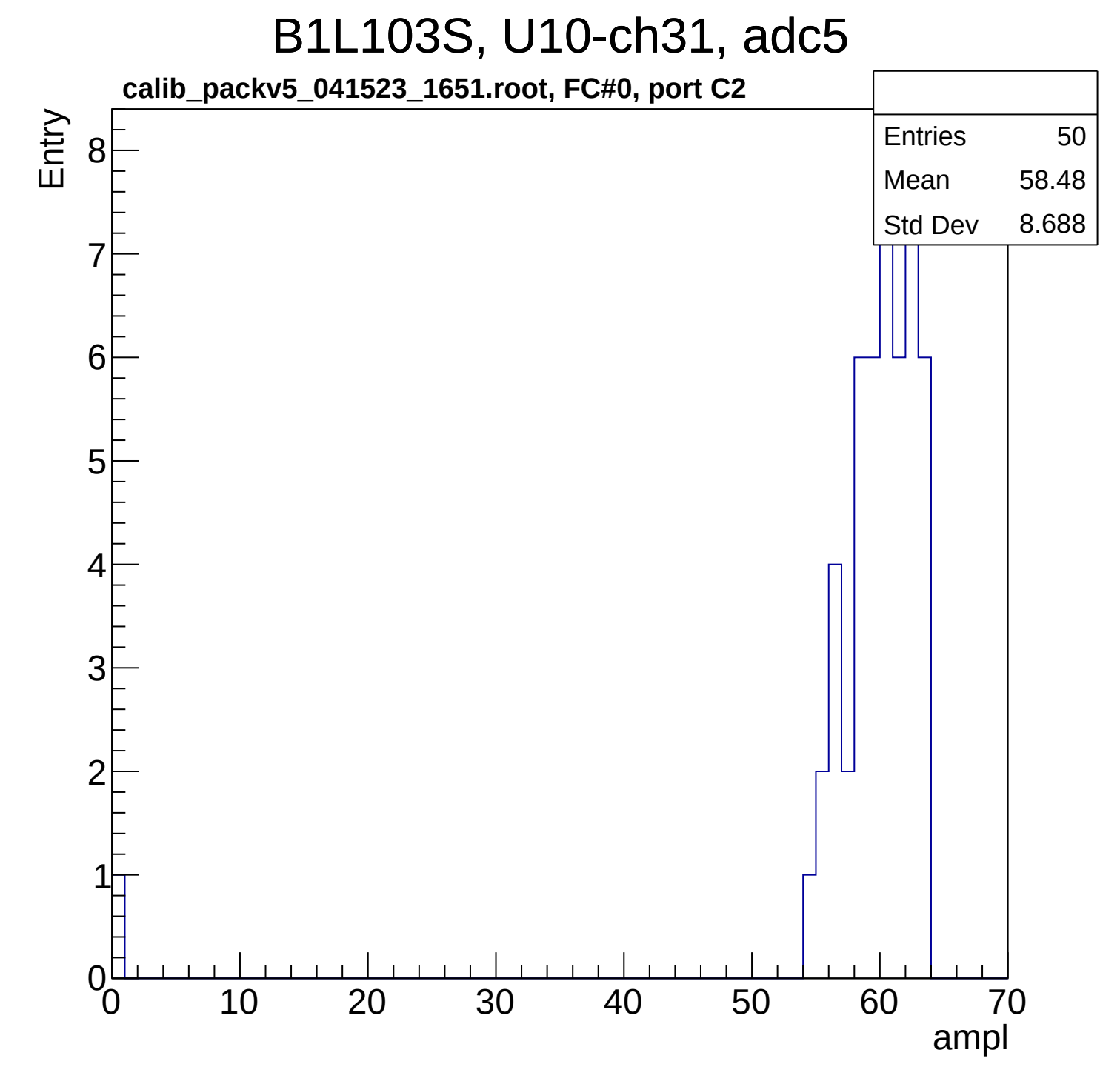
B1L103S, U10-ch31, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 58.48
Std Dev 8.688
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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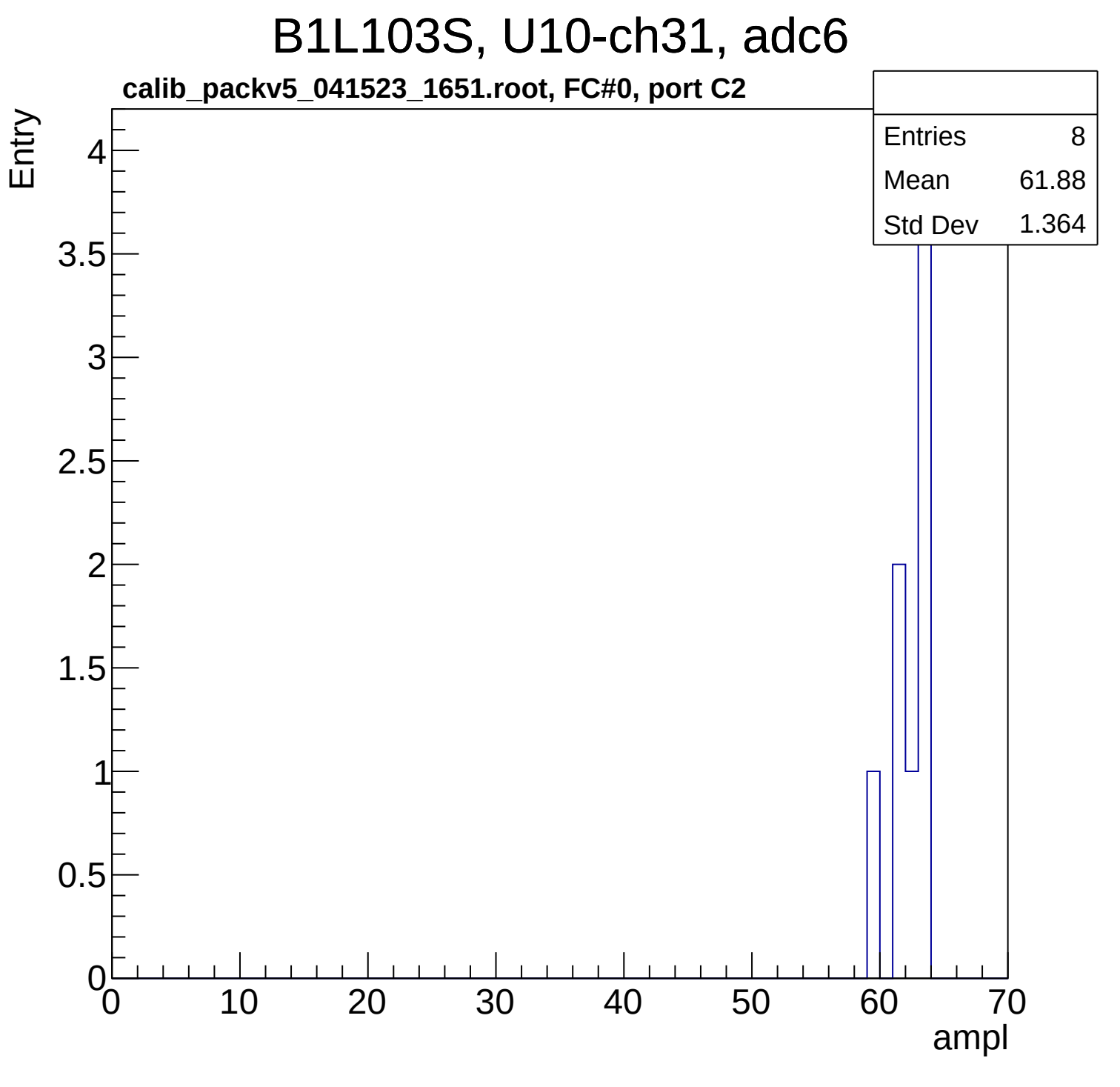
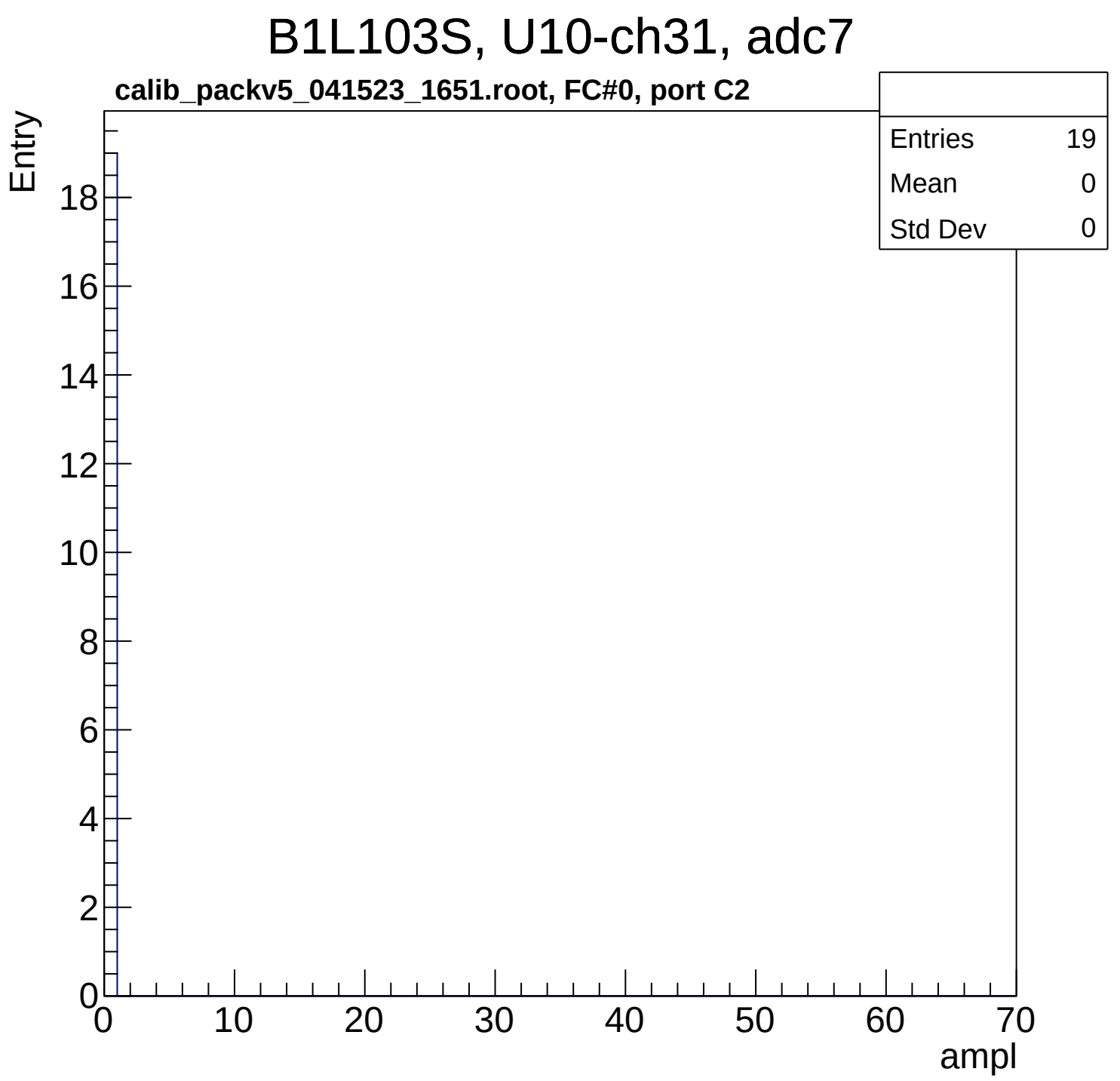
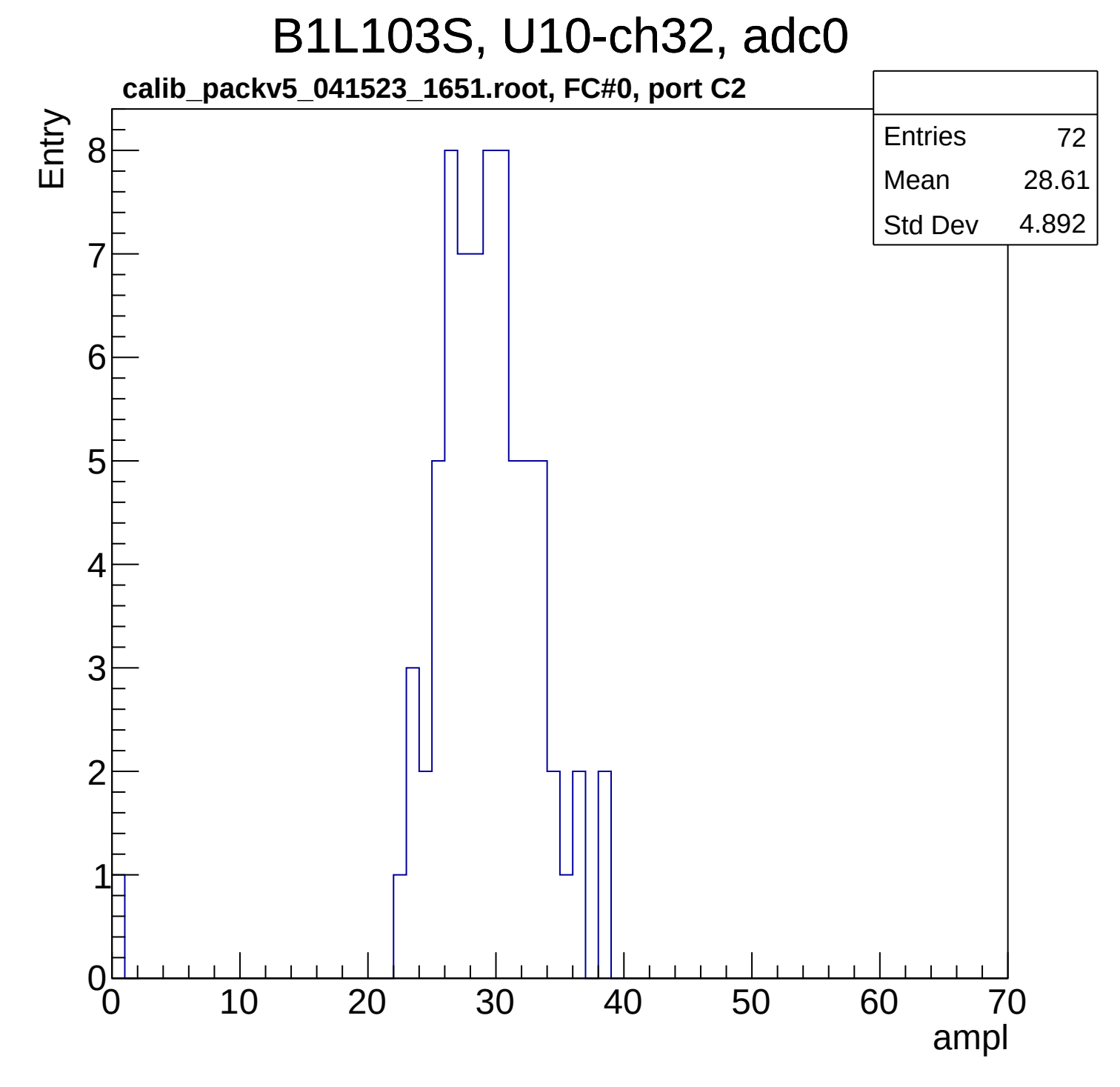
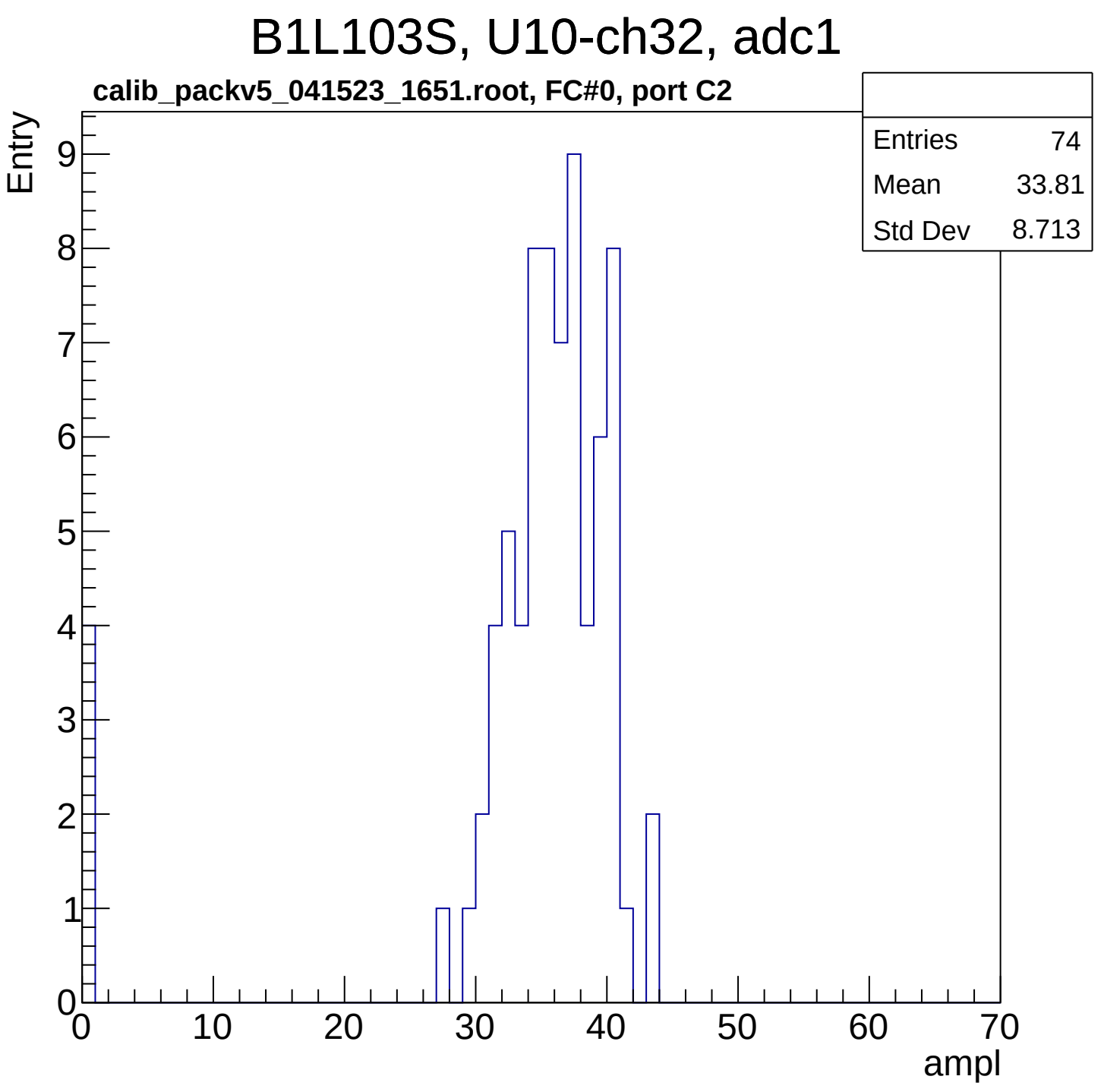
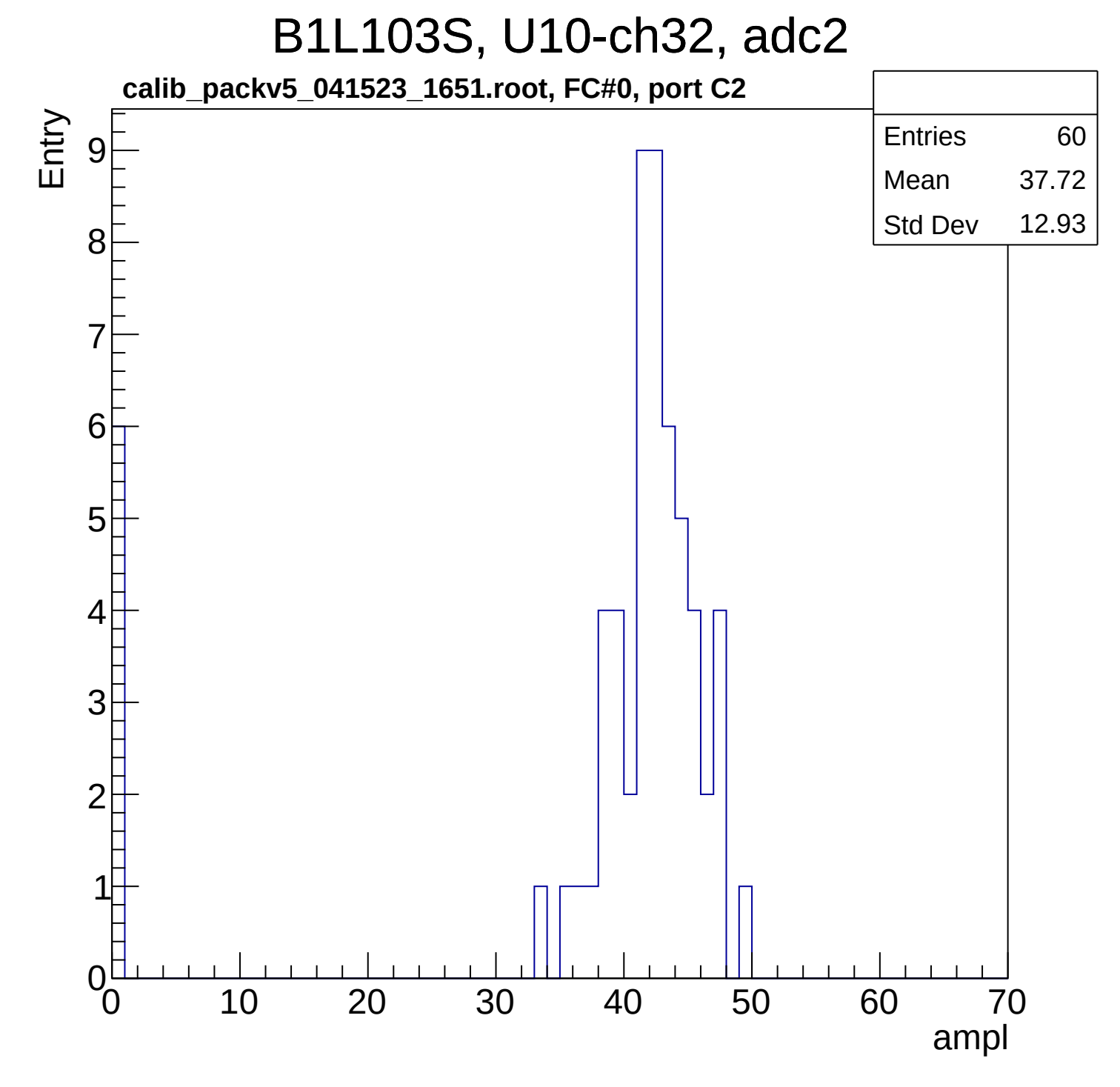
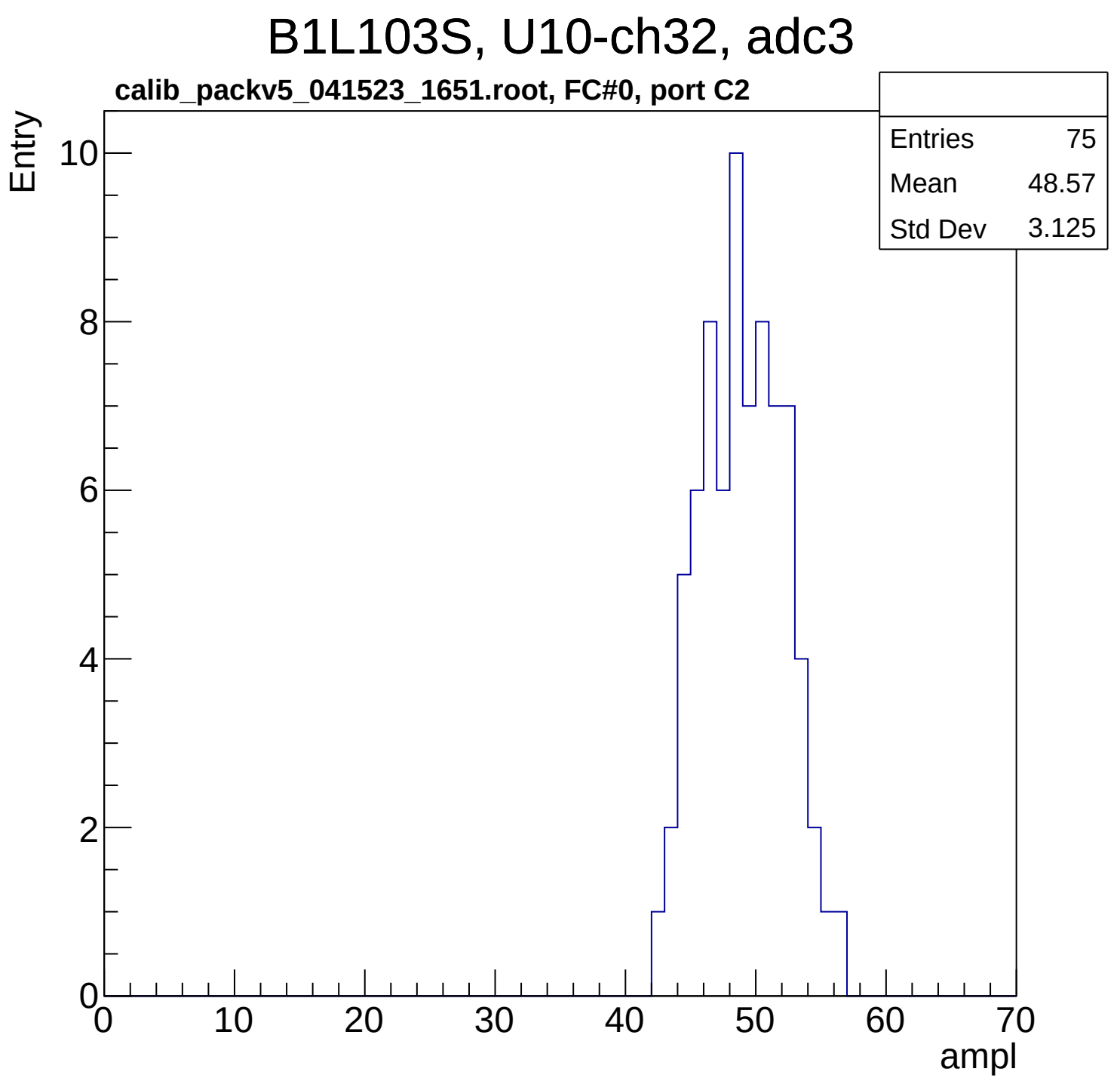

B1L103S, U10-ch31, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 61.88
Std Dev 1.364
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

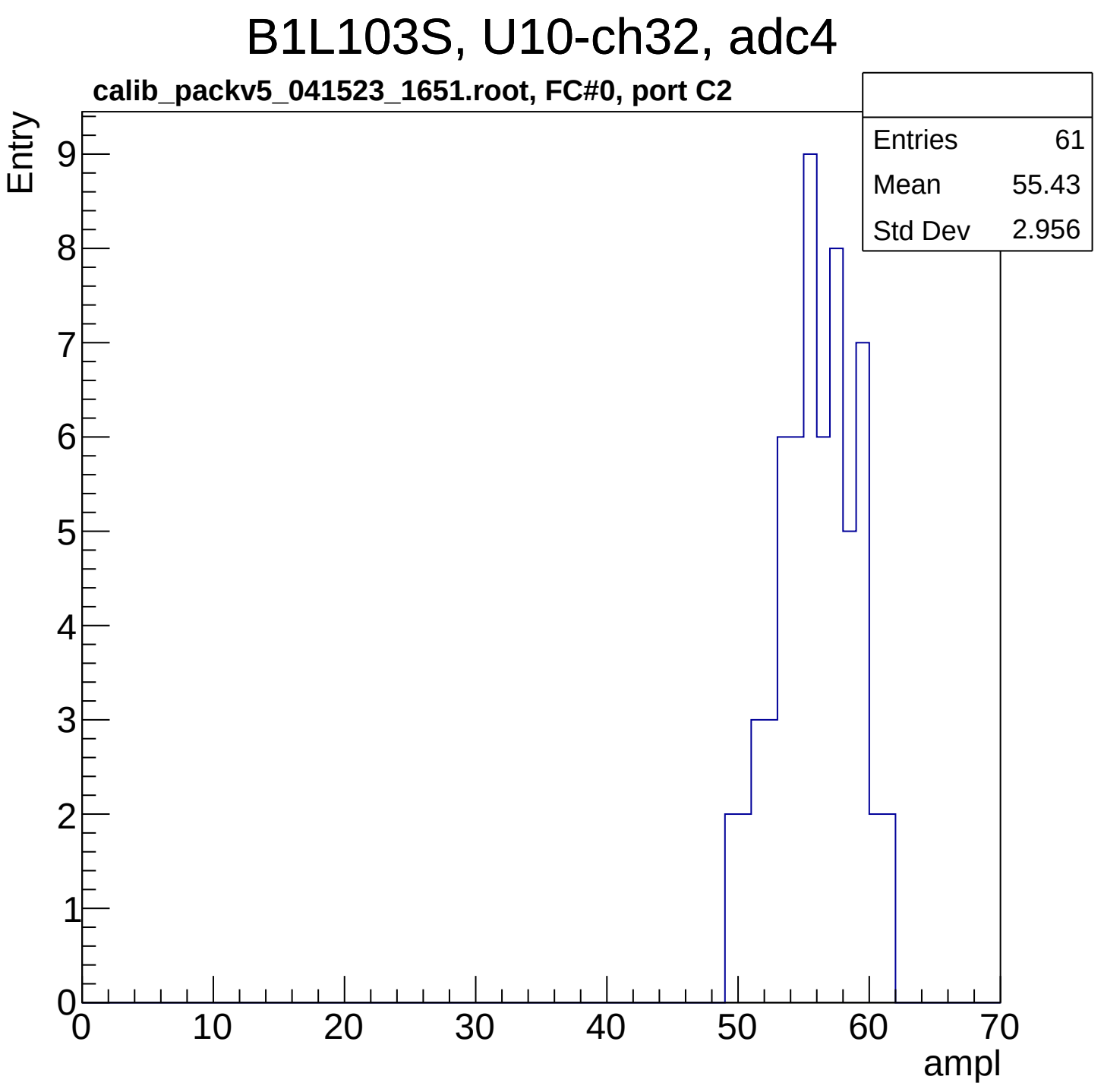

B1L103S, U10-ch31, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

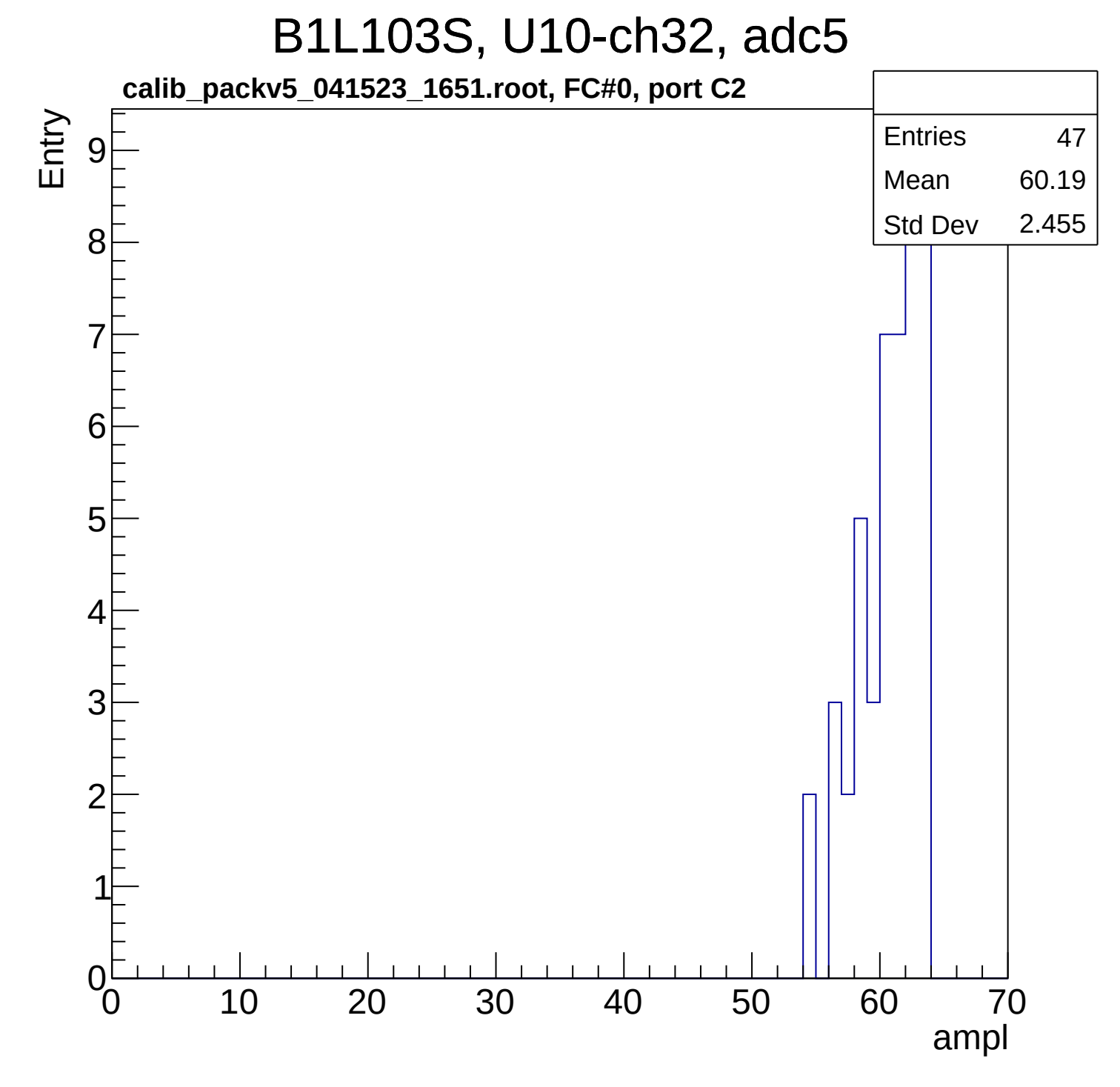

B1L103S, U10-ch32, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 28.61
Std Dev 4.892
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

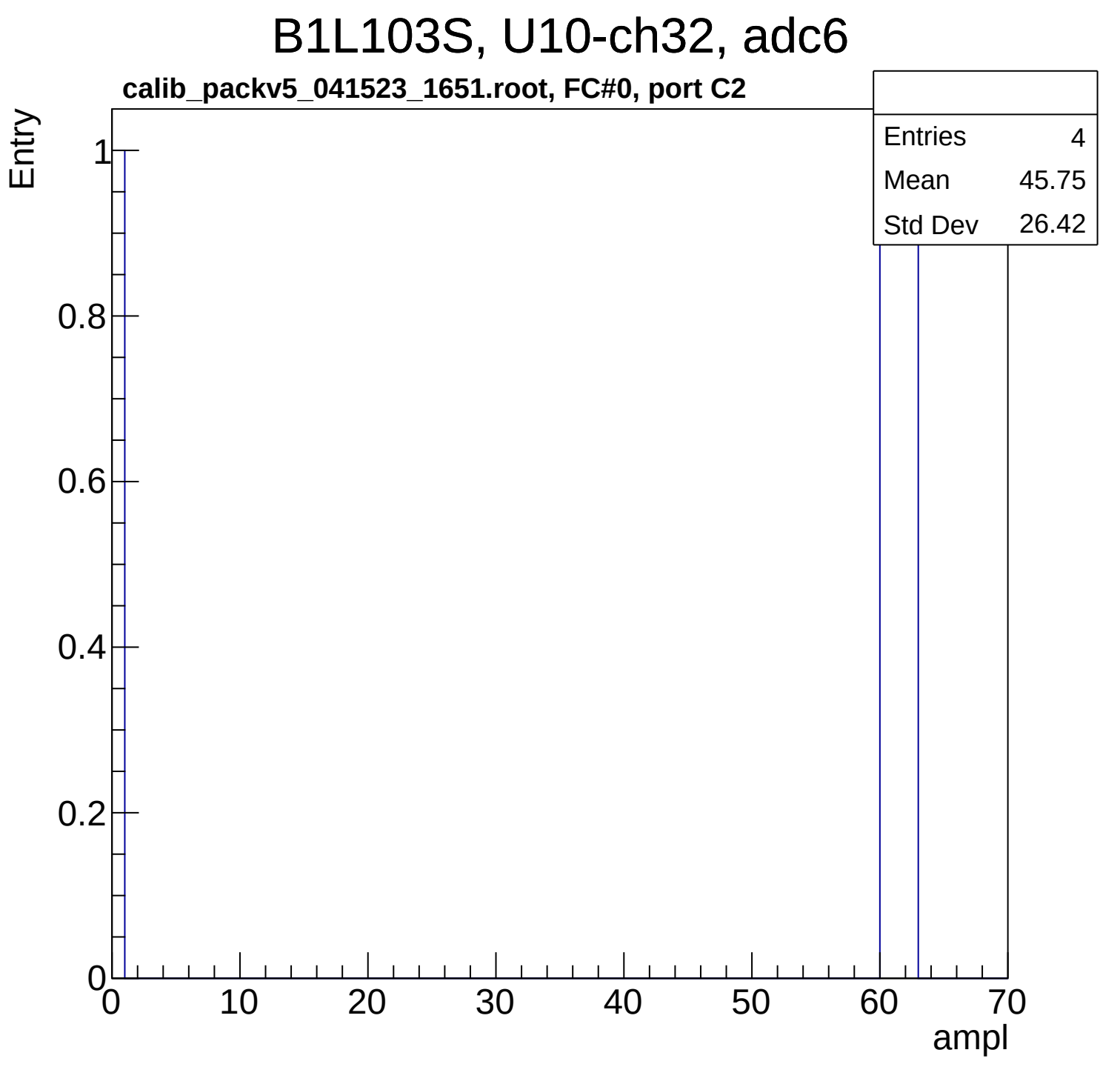

B1L103S, U10-ch32, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 33.81
Std Dev 8.713
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

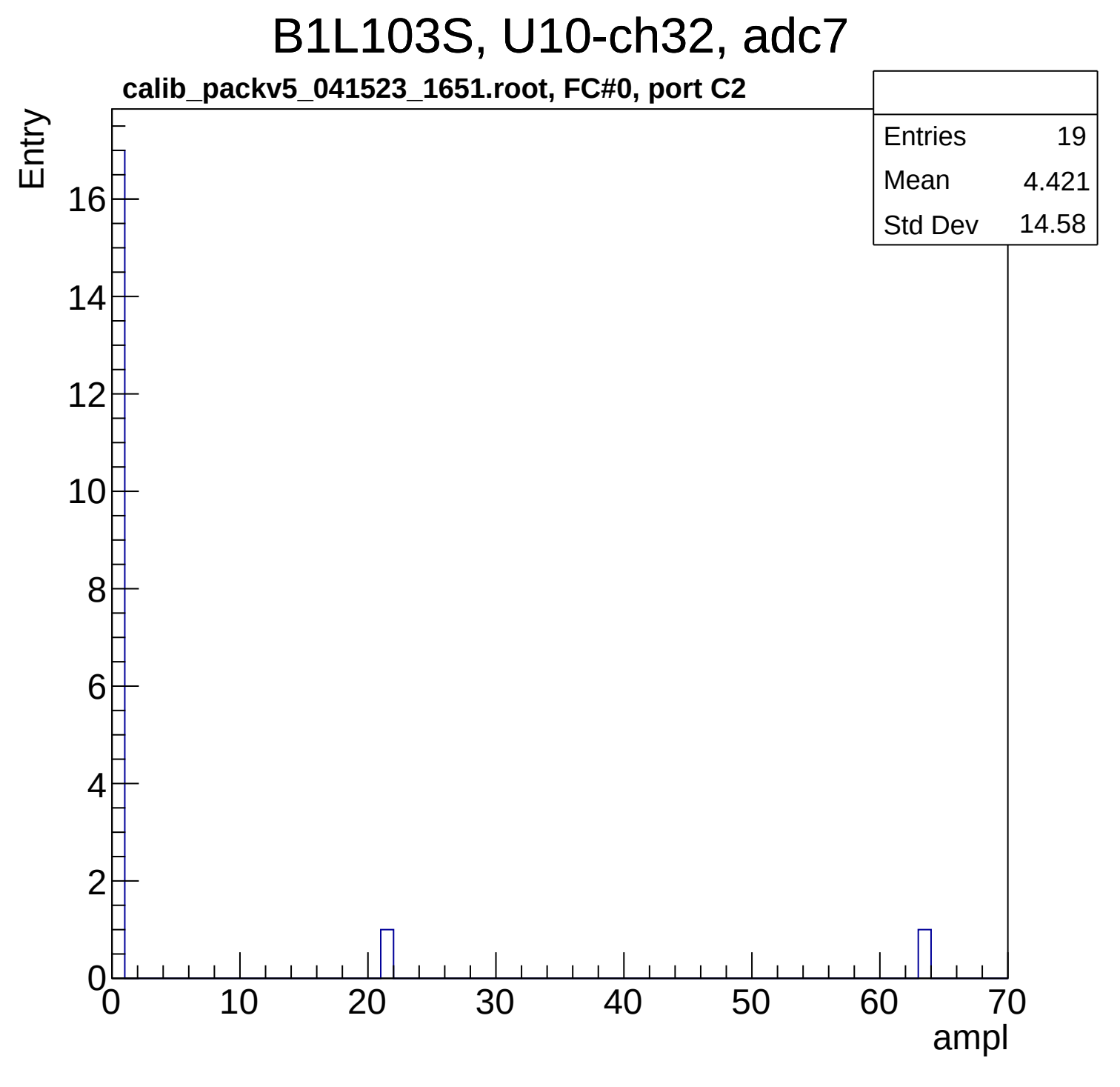

B1L103S, U10-ch32, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 37.72
Std Dev 12.93
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

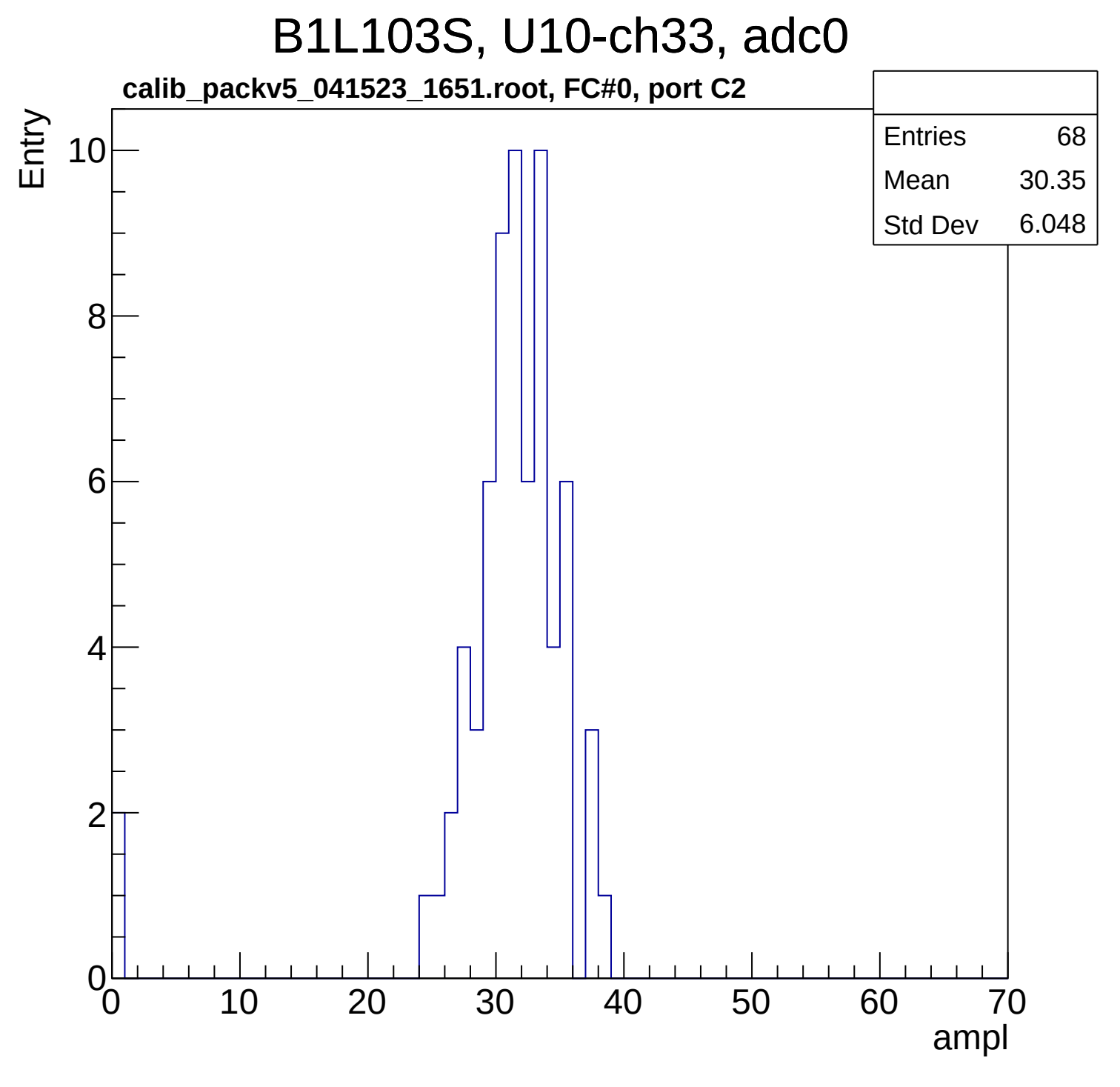

B1L103S, U10-ch32, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 48.57
Std Dev 3.125
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

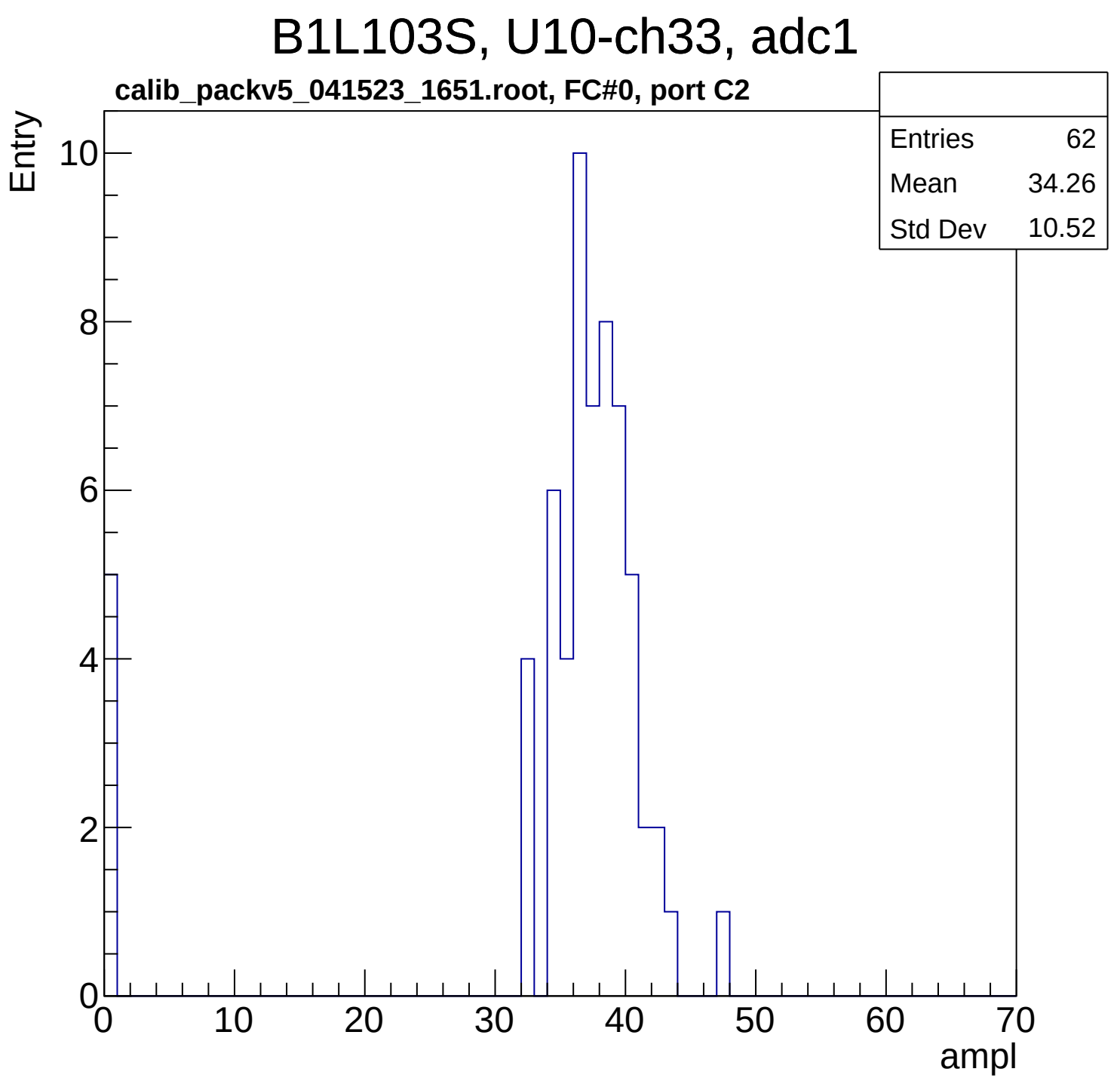

B1L103S, U10-ch32, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 55.43
Std Dev 2.956
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

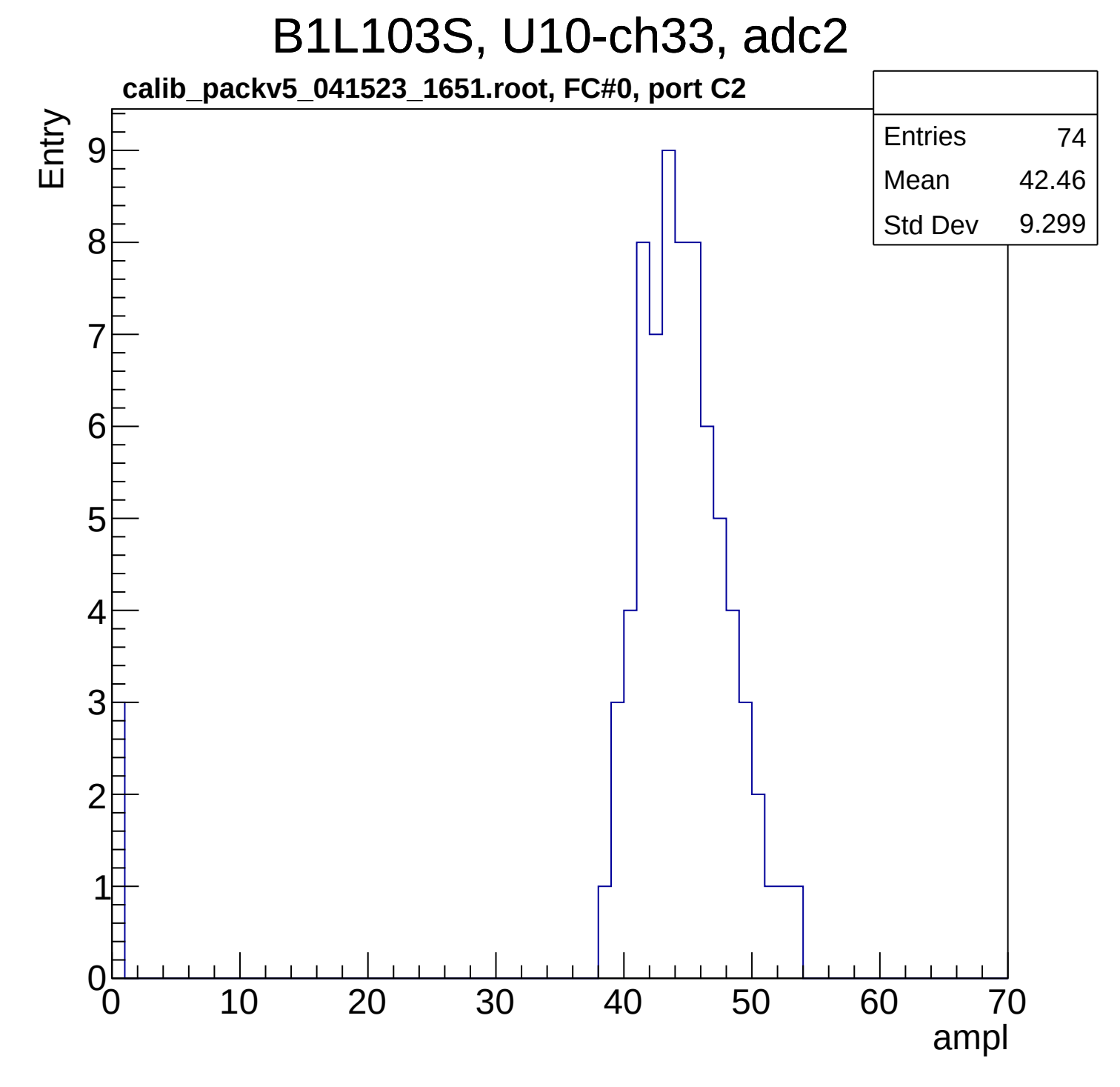

B1L103S, U10-ch32, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 60.19
Std Dev 2.455
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U10-ch32, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 4
Mean 45.75
Std Dev 26.42
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch32, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 4.421
Std Dev 14.58
Entry
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch33, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 30.35
Std Dev 6.048
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U10-ch33, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 34.26
Std Dev 10.52
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch33, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 42.46
Std Dev 9.299
Entry
ampl
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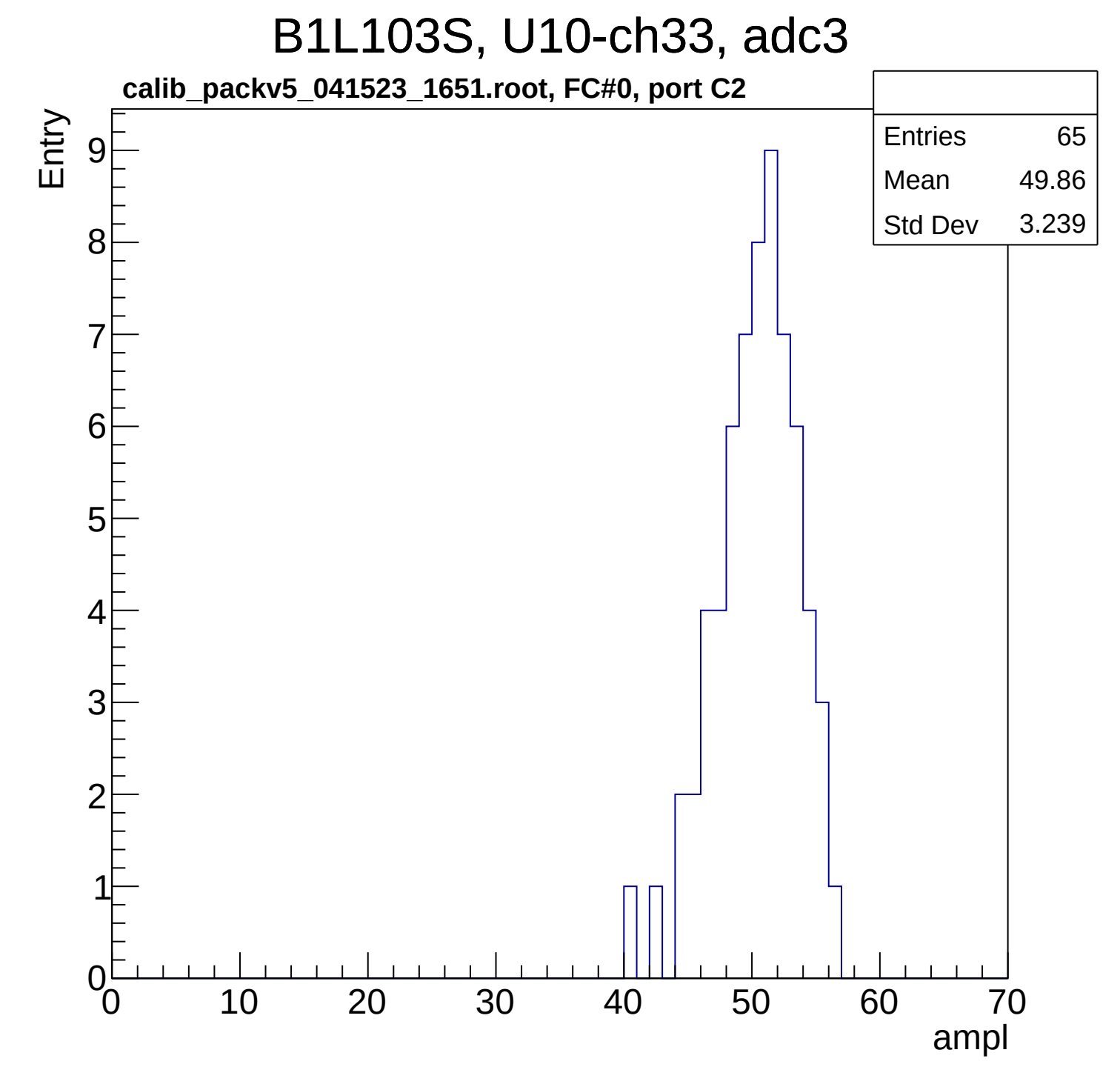
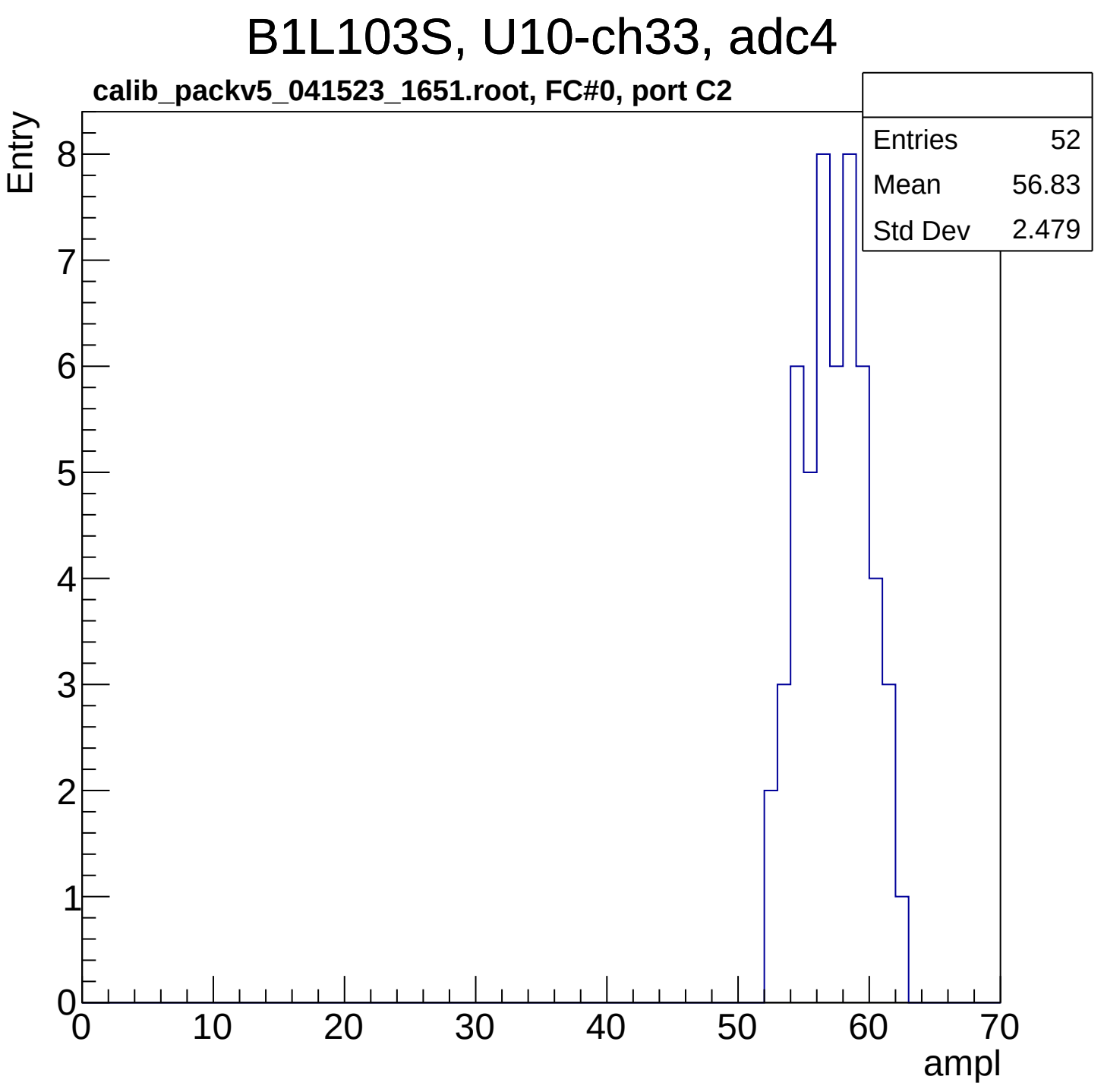
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U10-ch33, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 49.86
Std Dev 3.239
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U10-ch33, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 56.83
Std Dev 2.479
Entry
ampl
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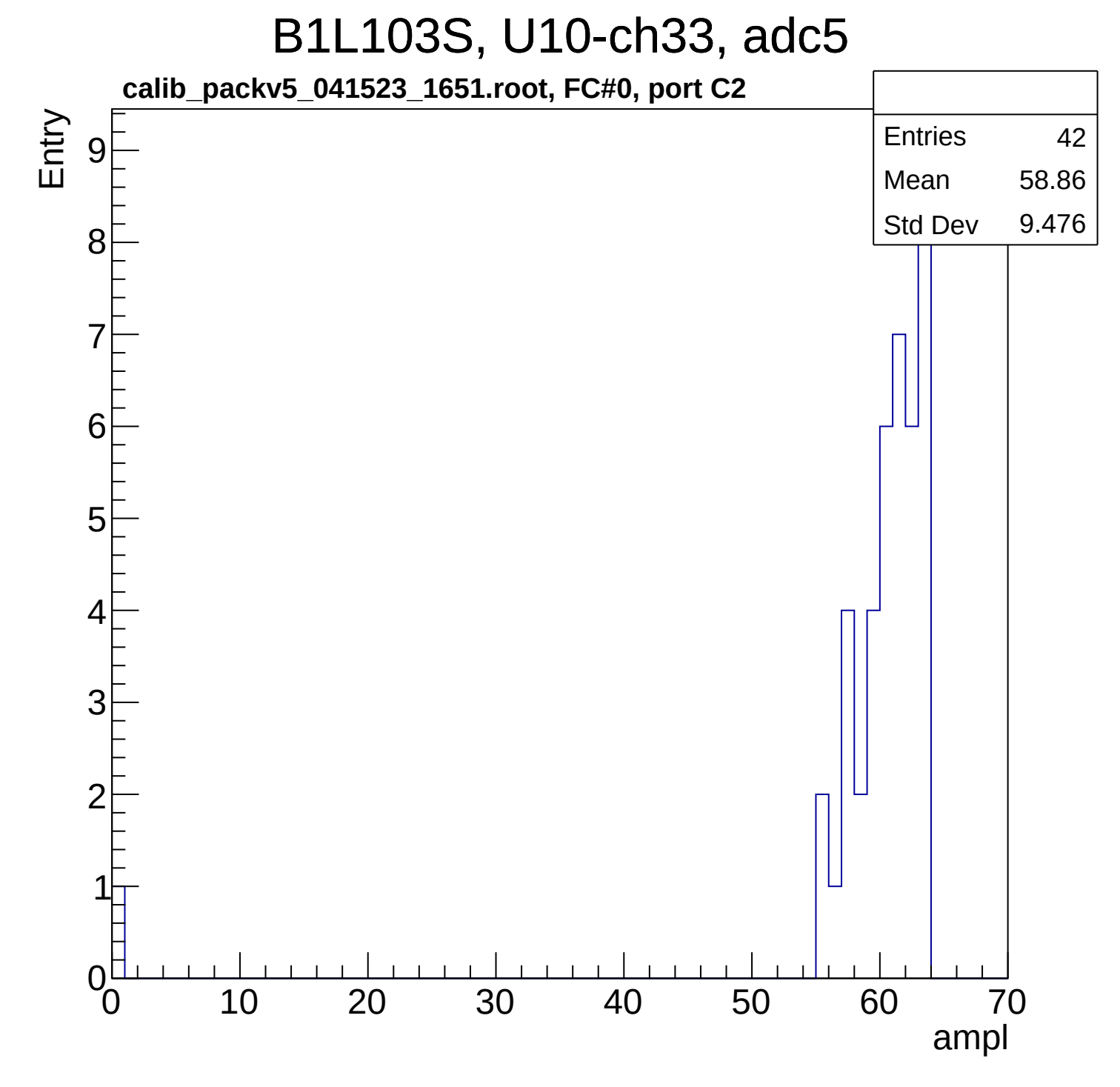
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U10-ch33, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 42
Mean 58.86
Std Dev 9.476
Entry
ampl
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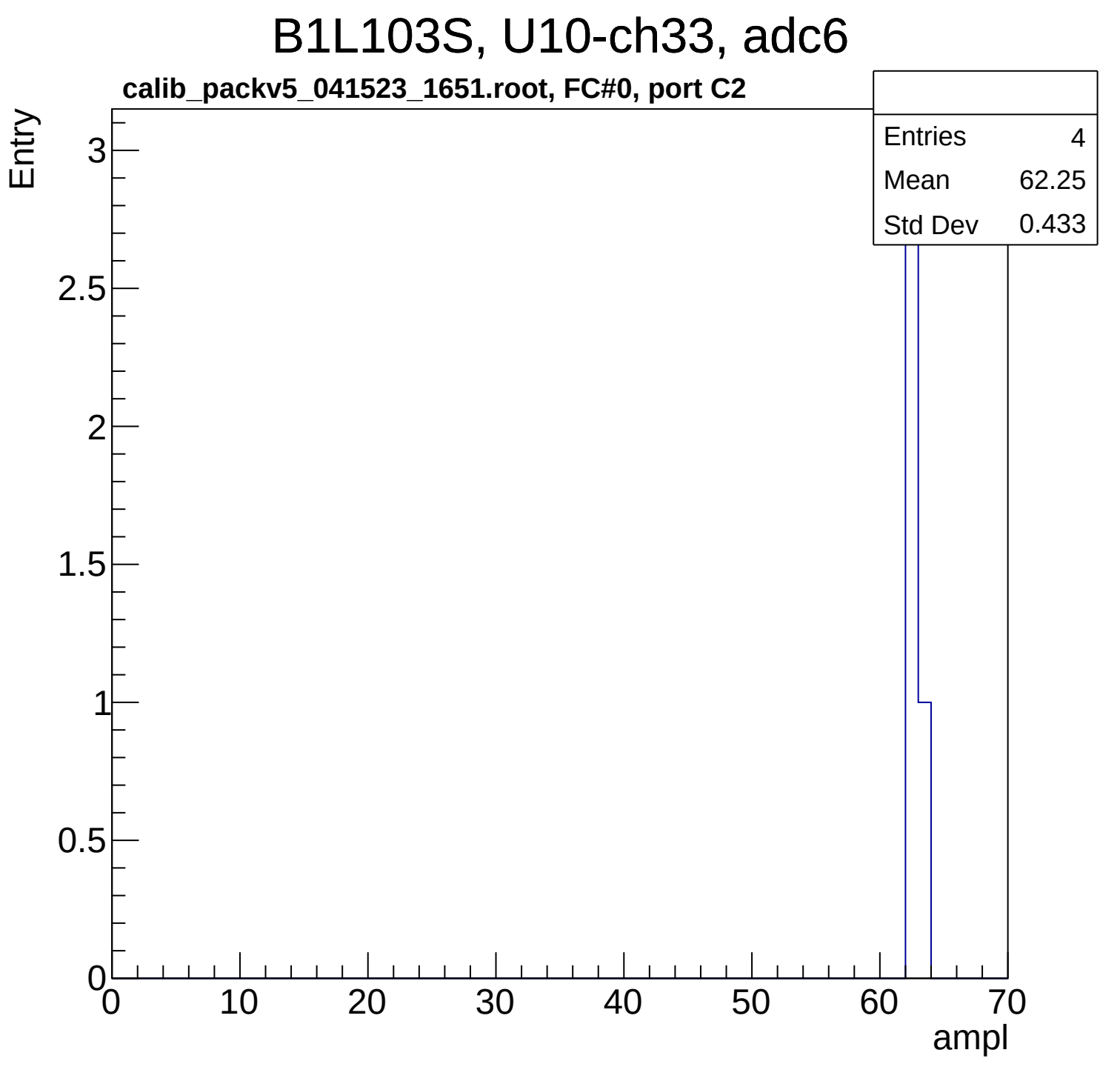
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U10-ch33, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 4
Mean 62.25
Std Dev 0.433
Entry
ampl
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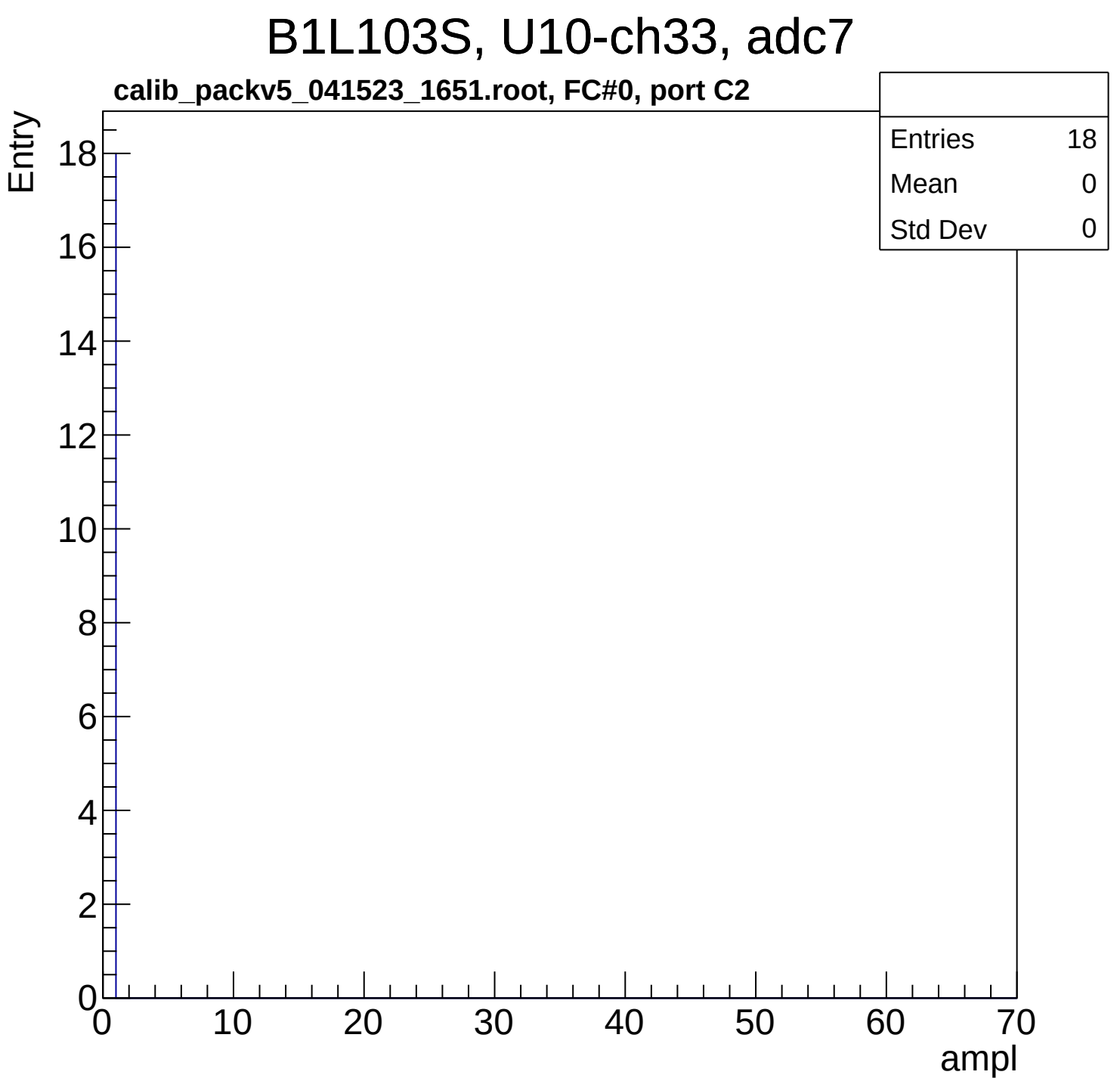
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U10-ch33, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
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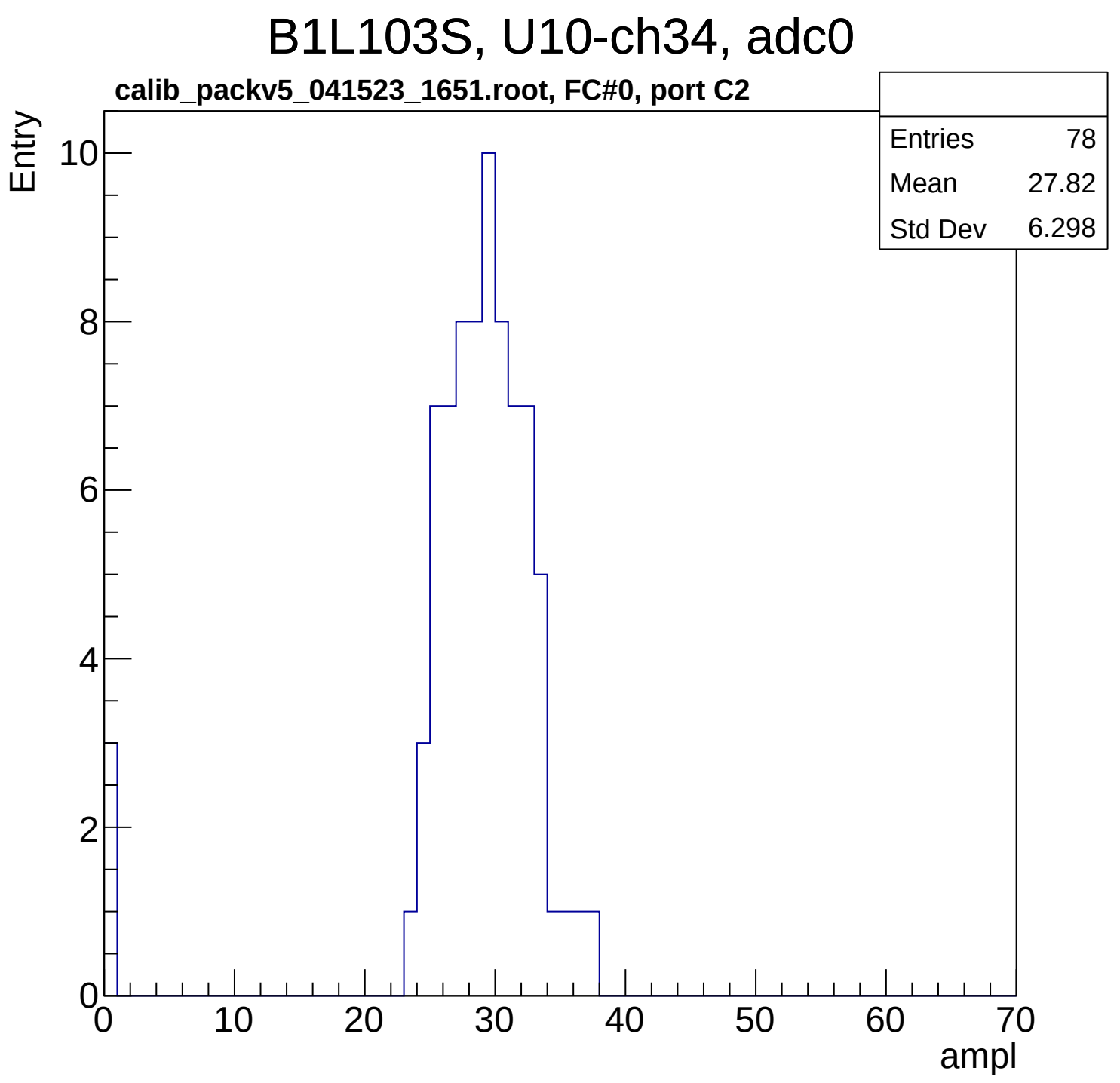
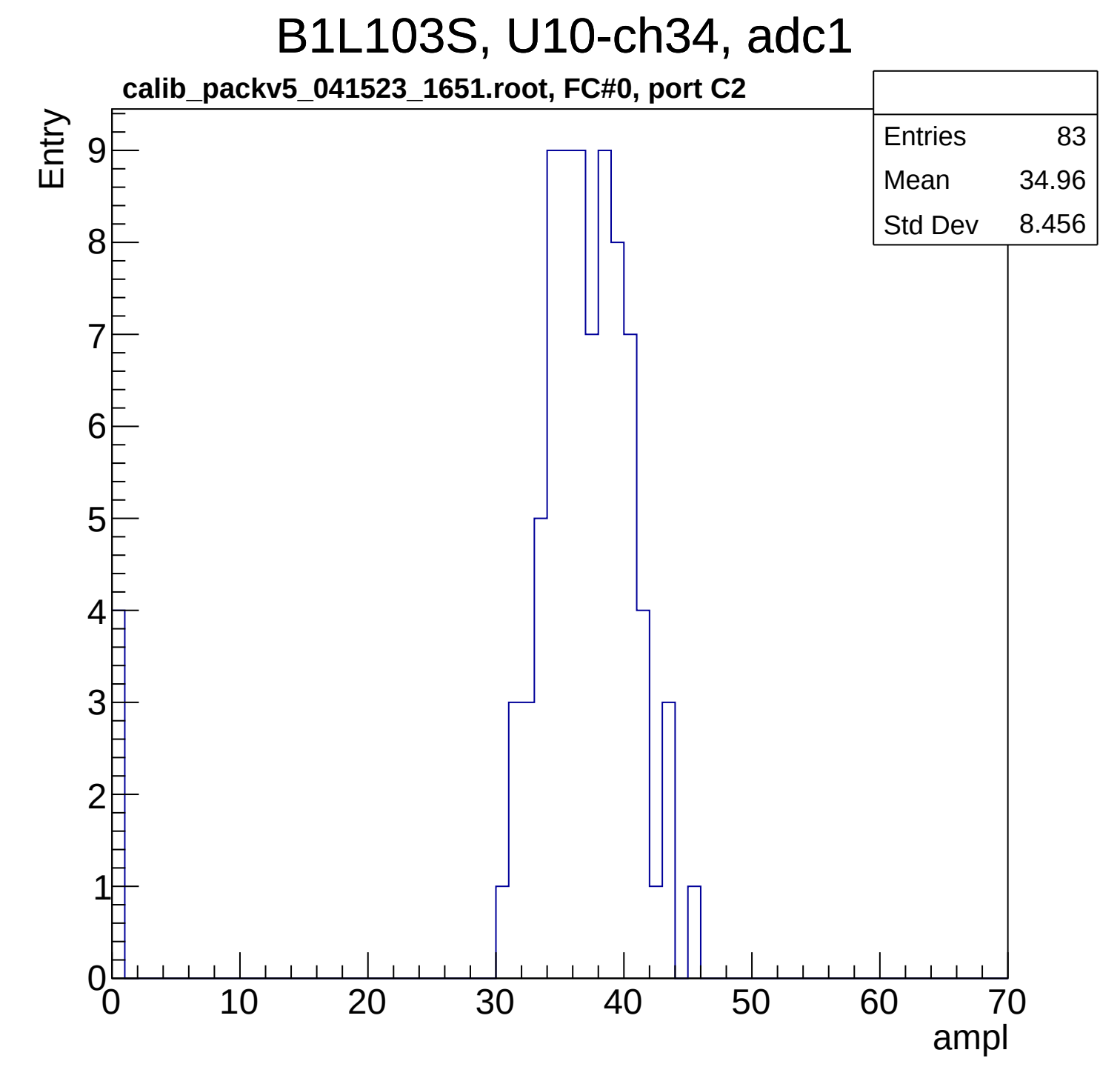
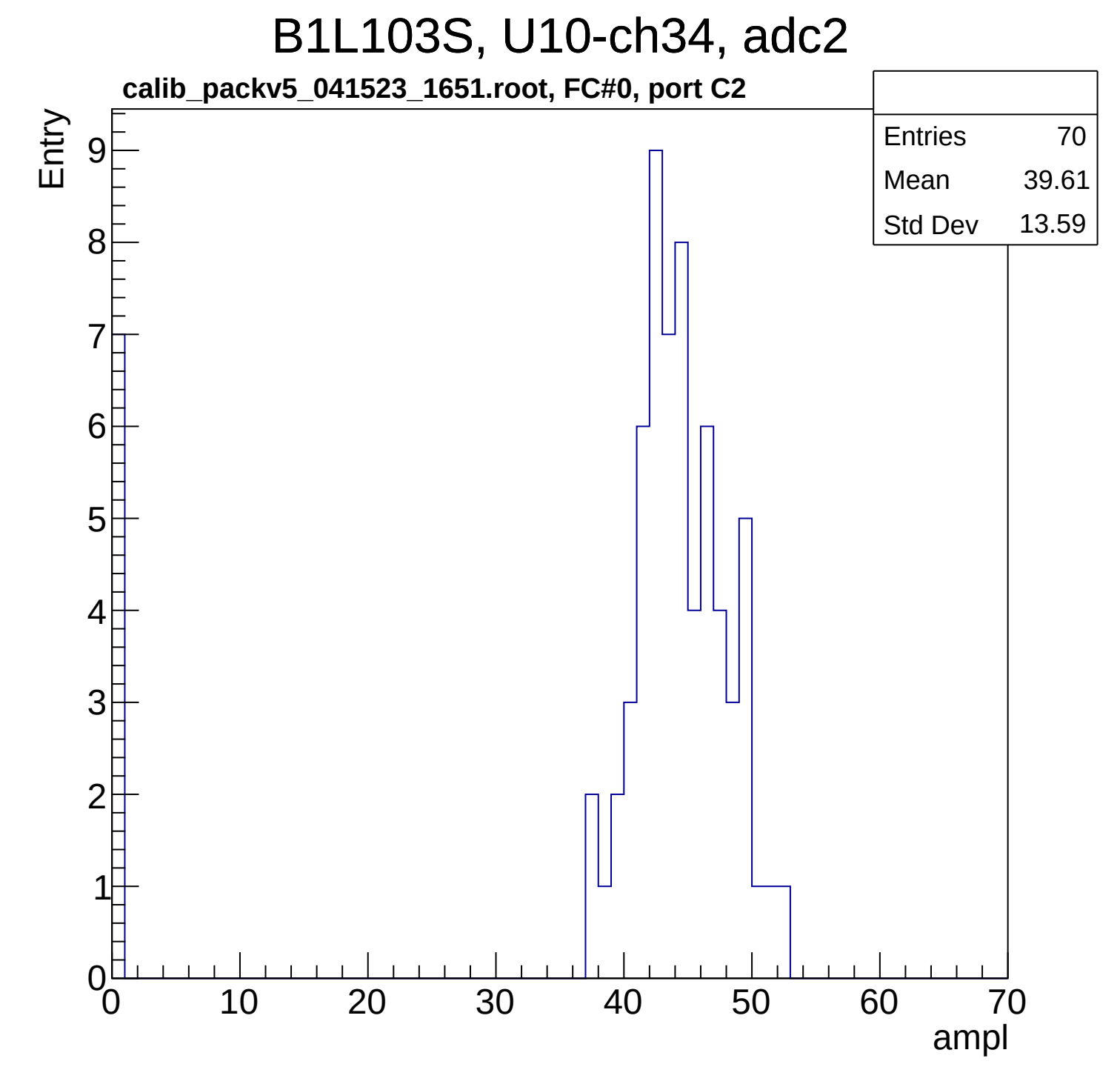
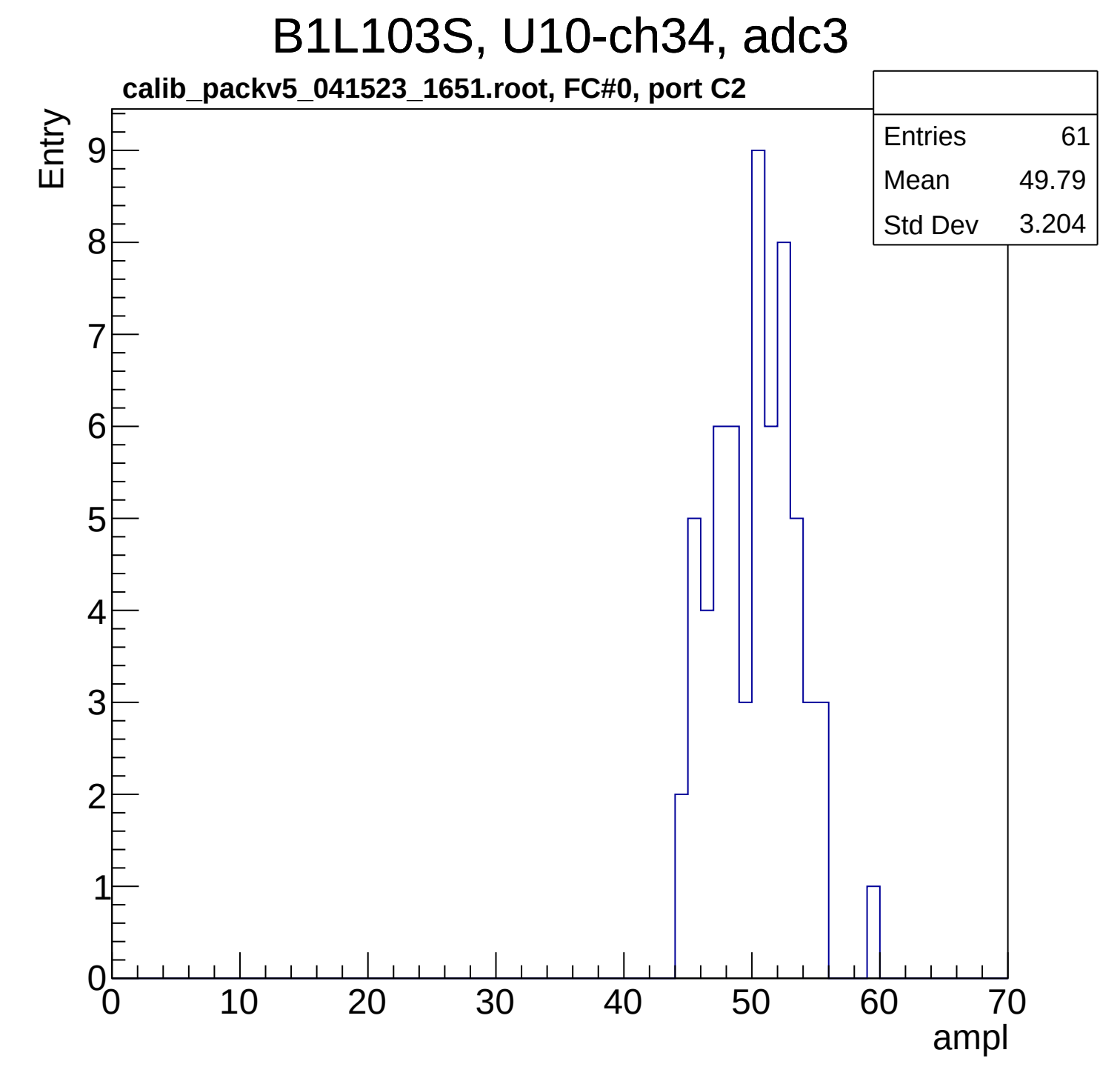
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch34, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 27.82
Std Dev 6.298
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U10-ch34, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 34.96
Std Dev 8.456
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U10-ch34, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 39.61
Std Dev 13.59
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U10-ch34, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 49.79
Std Dev 3.204
Entry
ampl
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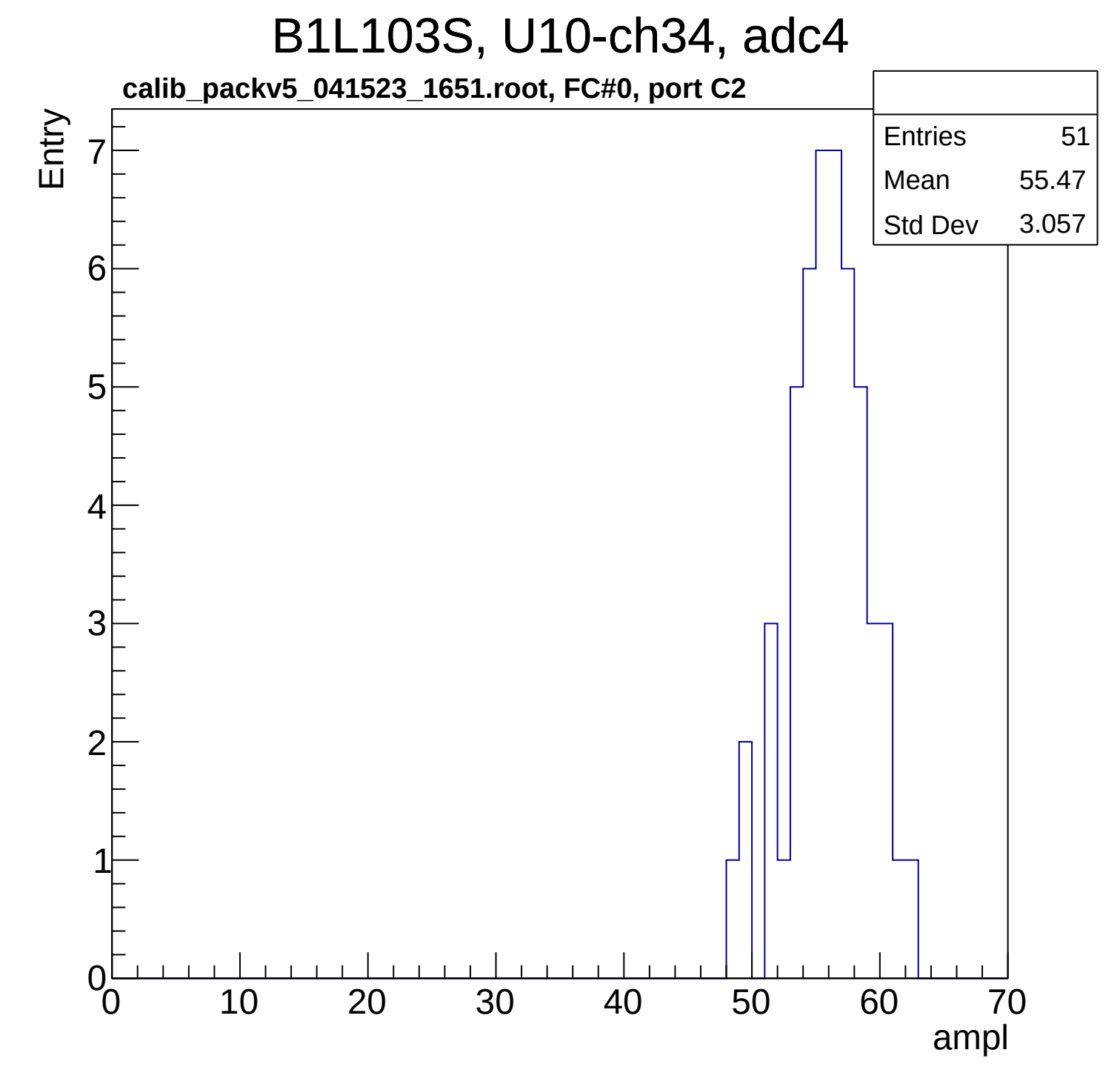
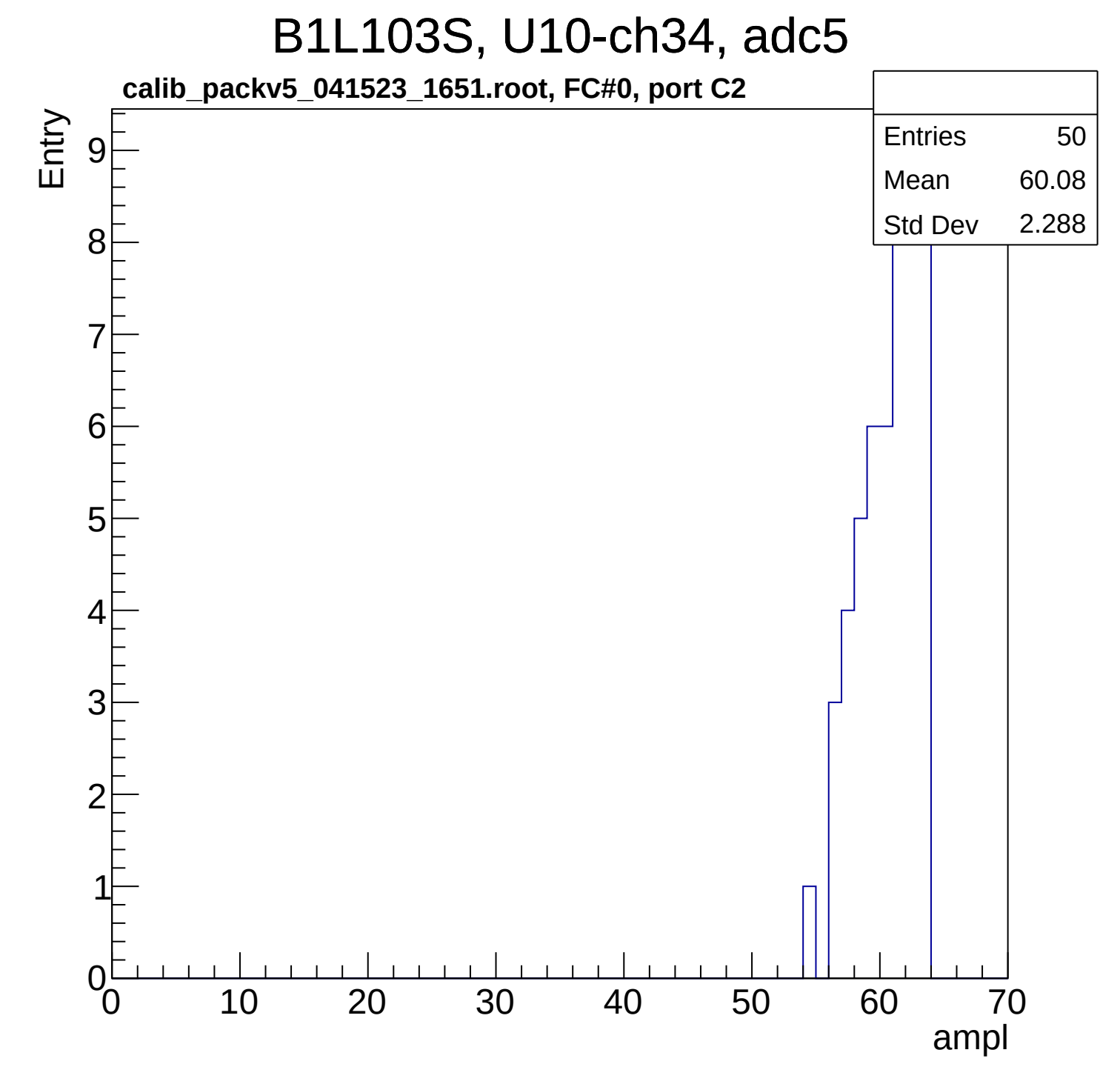
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U10-ch34, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 55.47
Std Dev 3.057
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U10-ch34, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 60.08
Std Dev 2.288
Entry
ampl
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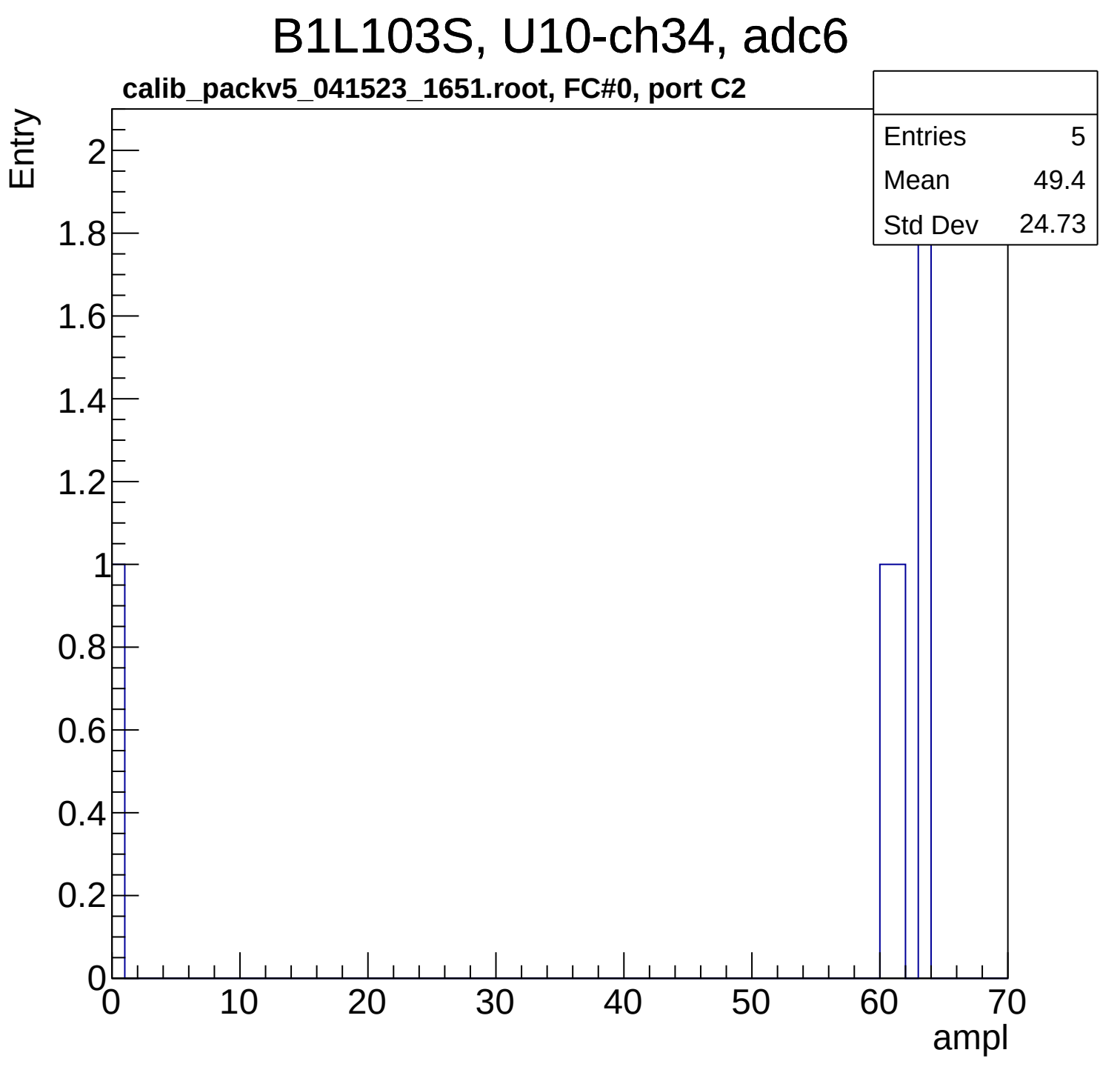
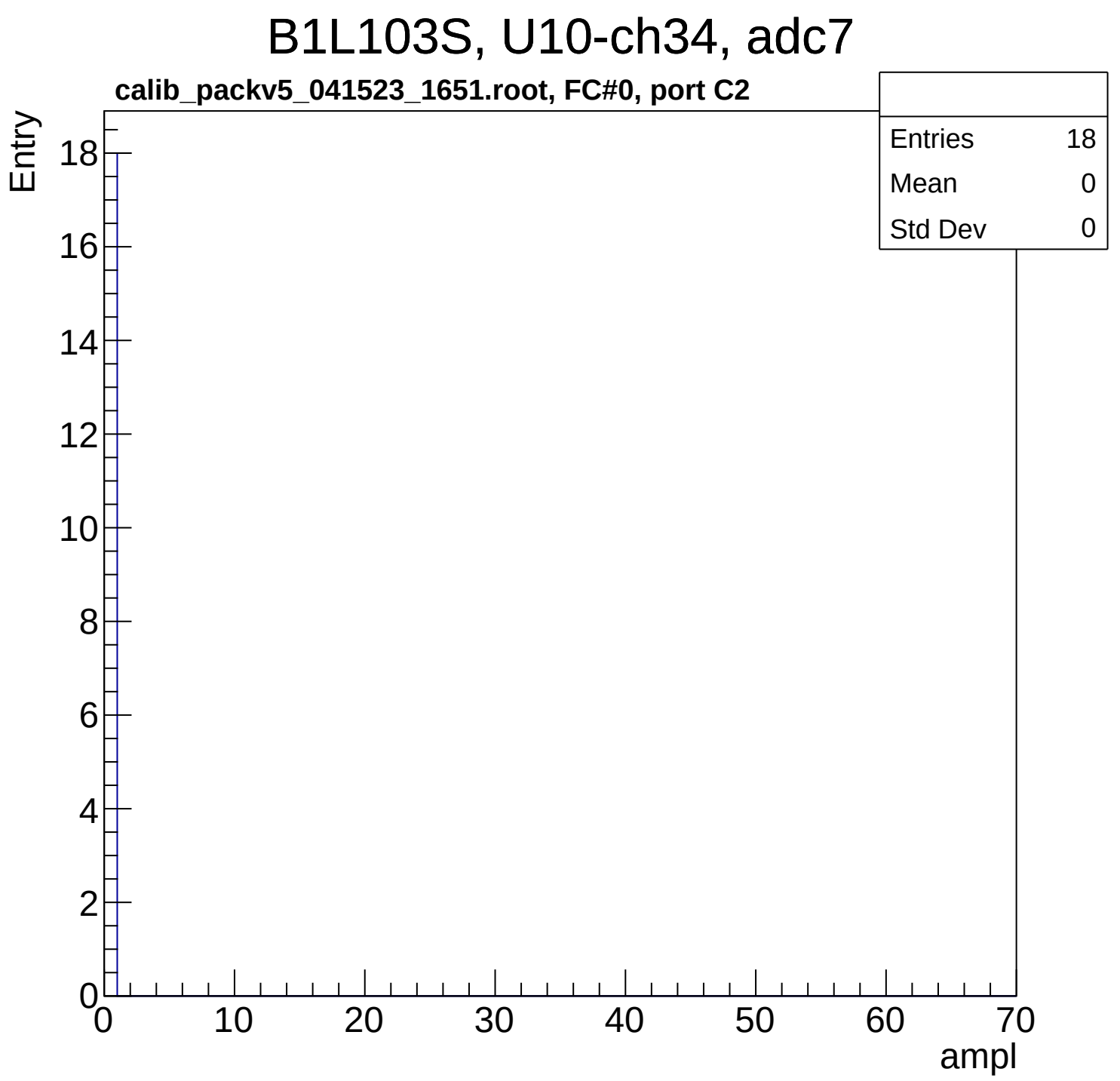
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U10-ch34, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 5
Mean 49.4
Std Dev 24.73
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U10-ch34, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
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2
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6
8
10
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14
16
18
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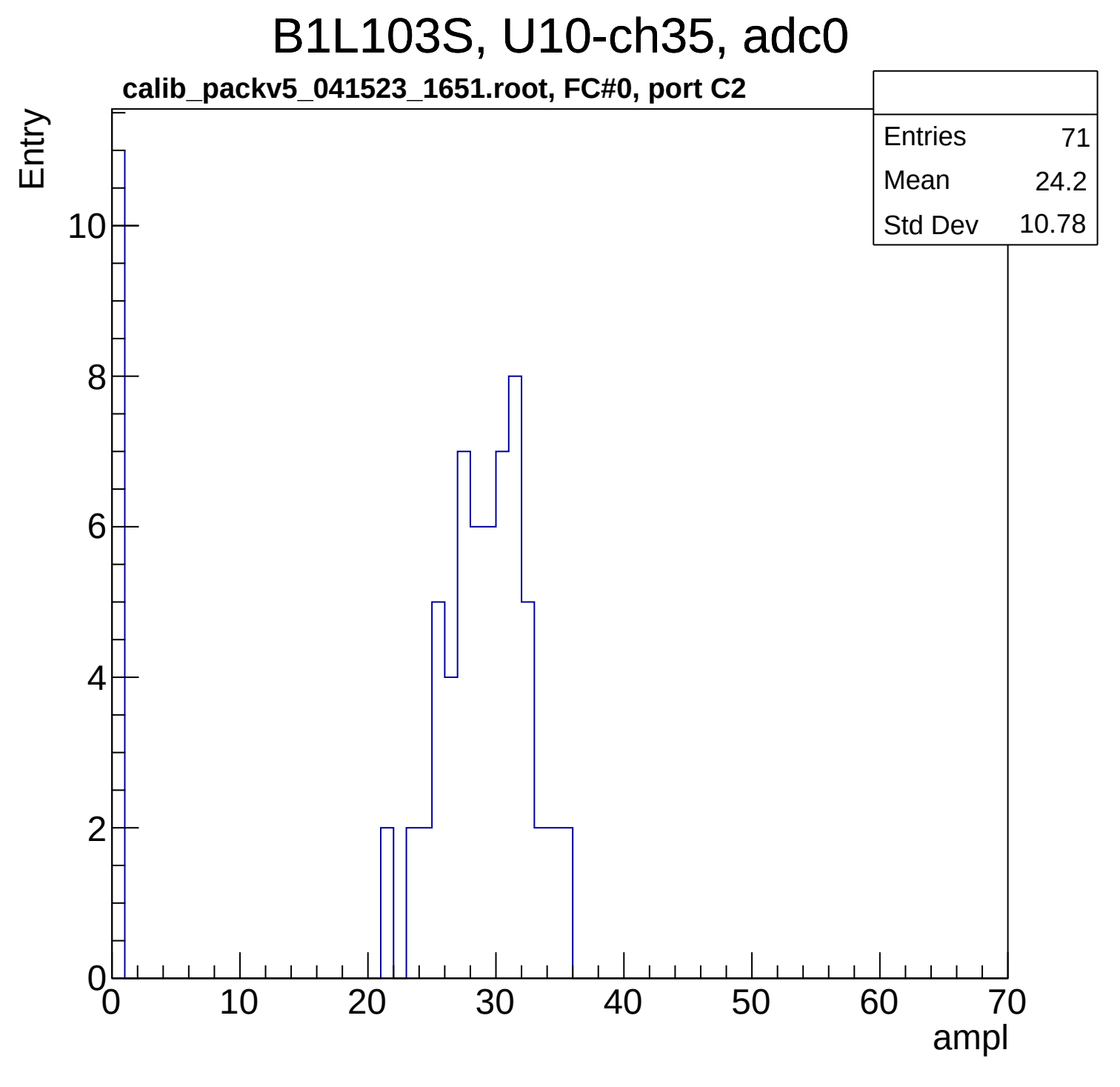
70
ampl


B1L103S, U10-ch35, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 24.2
Std Dev 10.78
Entry
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6
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10
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20
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50
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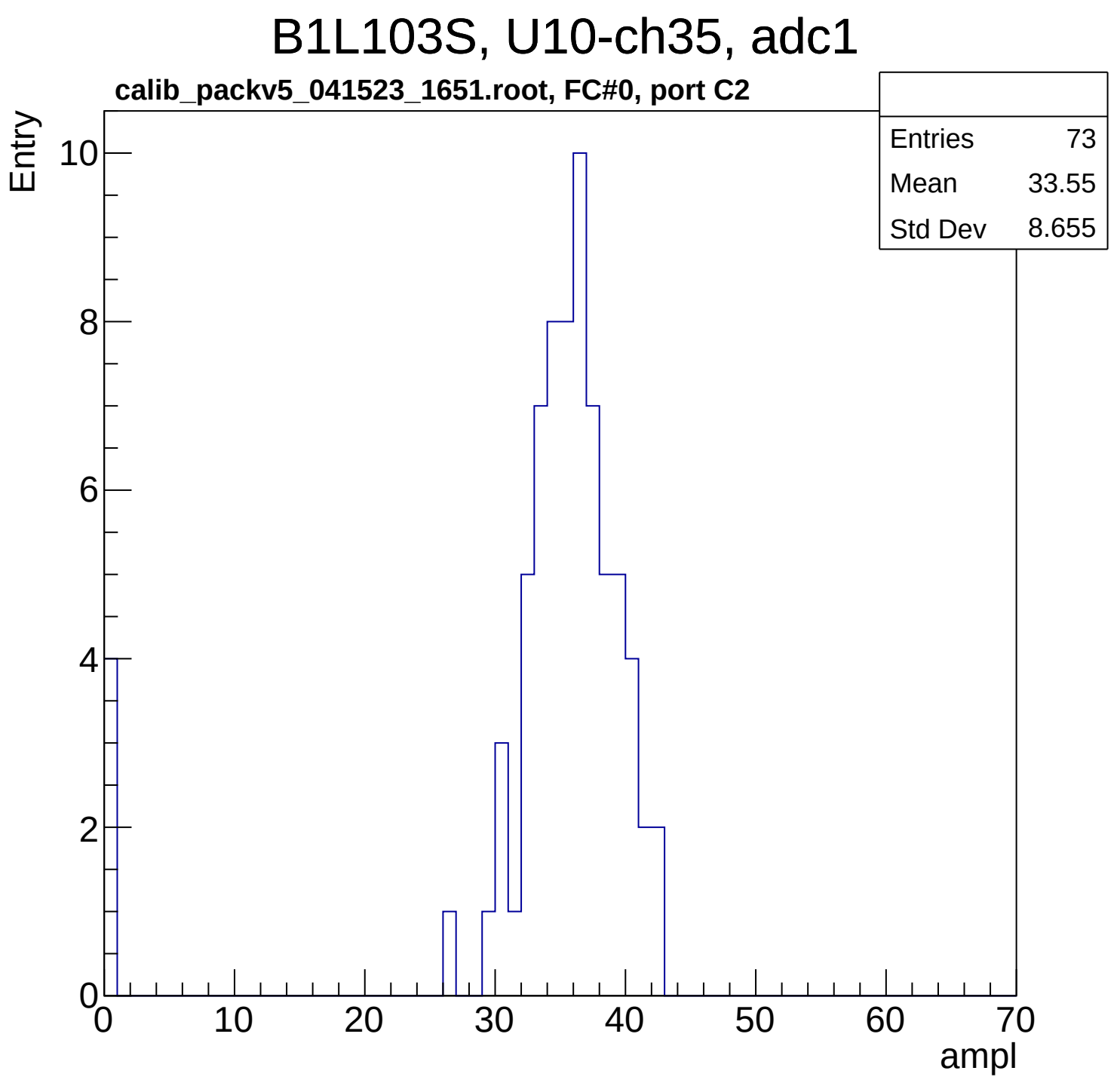
70
ampl


B1L103S, U10-ch35, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 33.55
Std Dev 8.655
Entry
ampl
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40
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60
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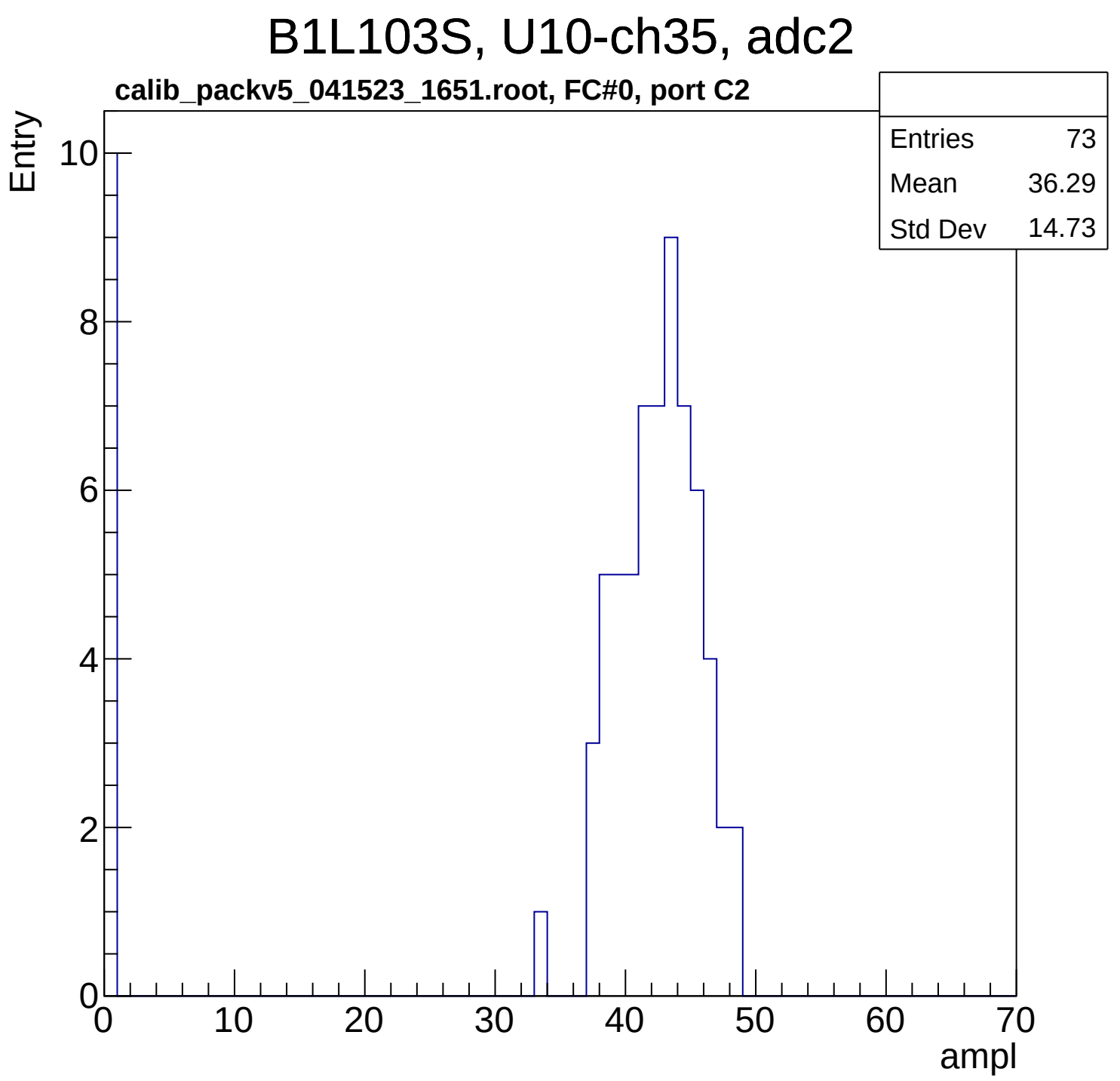
B1L103S, U10-ch35, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 36.29
Std Dev 14.73
Entry
ampl
0
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0
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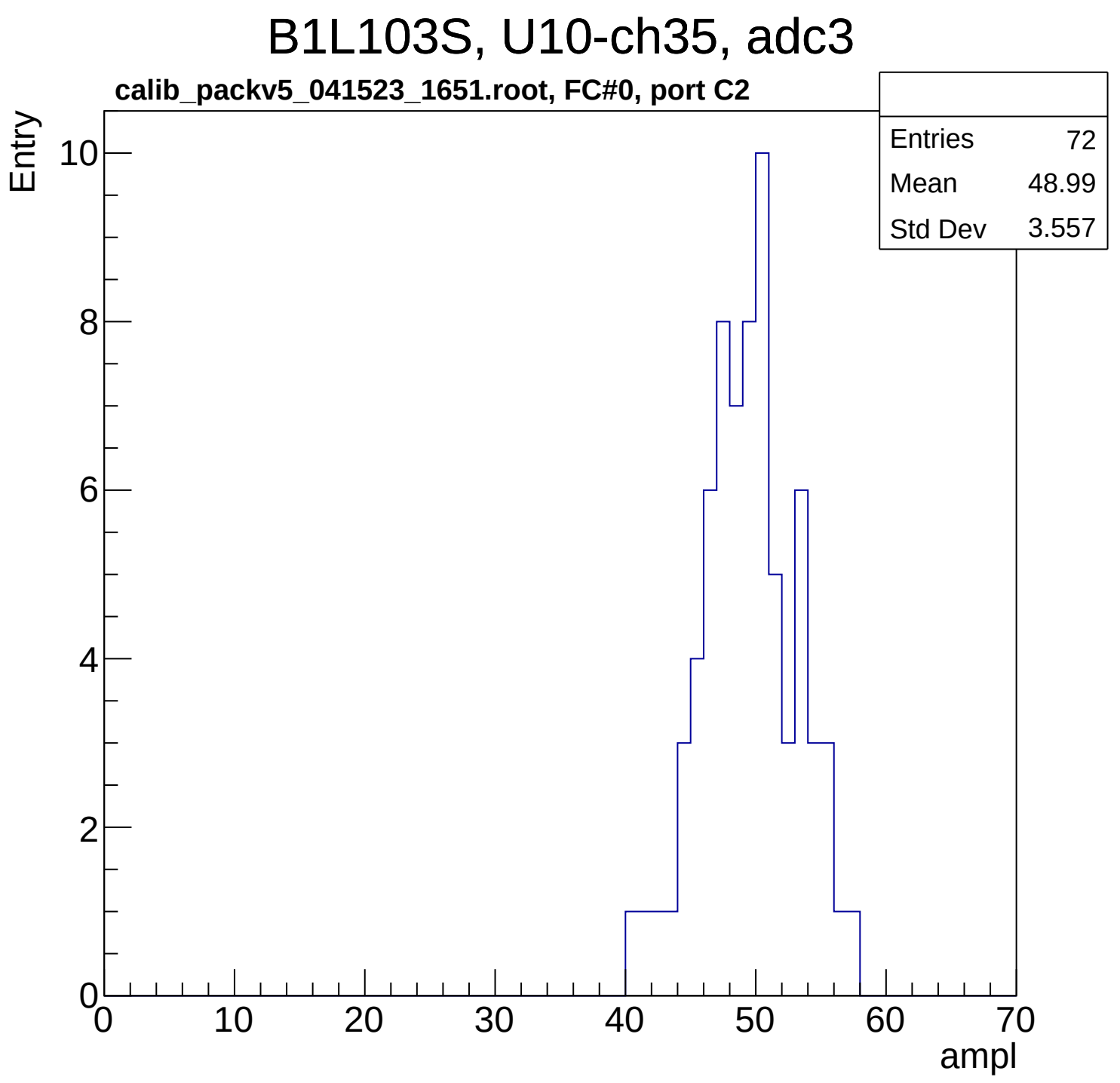
B1L103S, U10-ch35, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 48.99
Std Dev 3.557
Entry
ampl
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0
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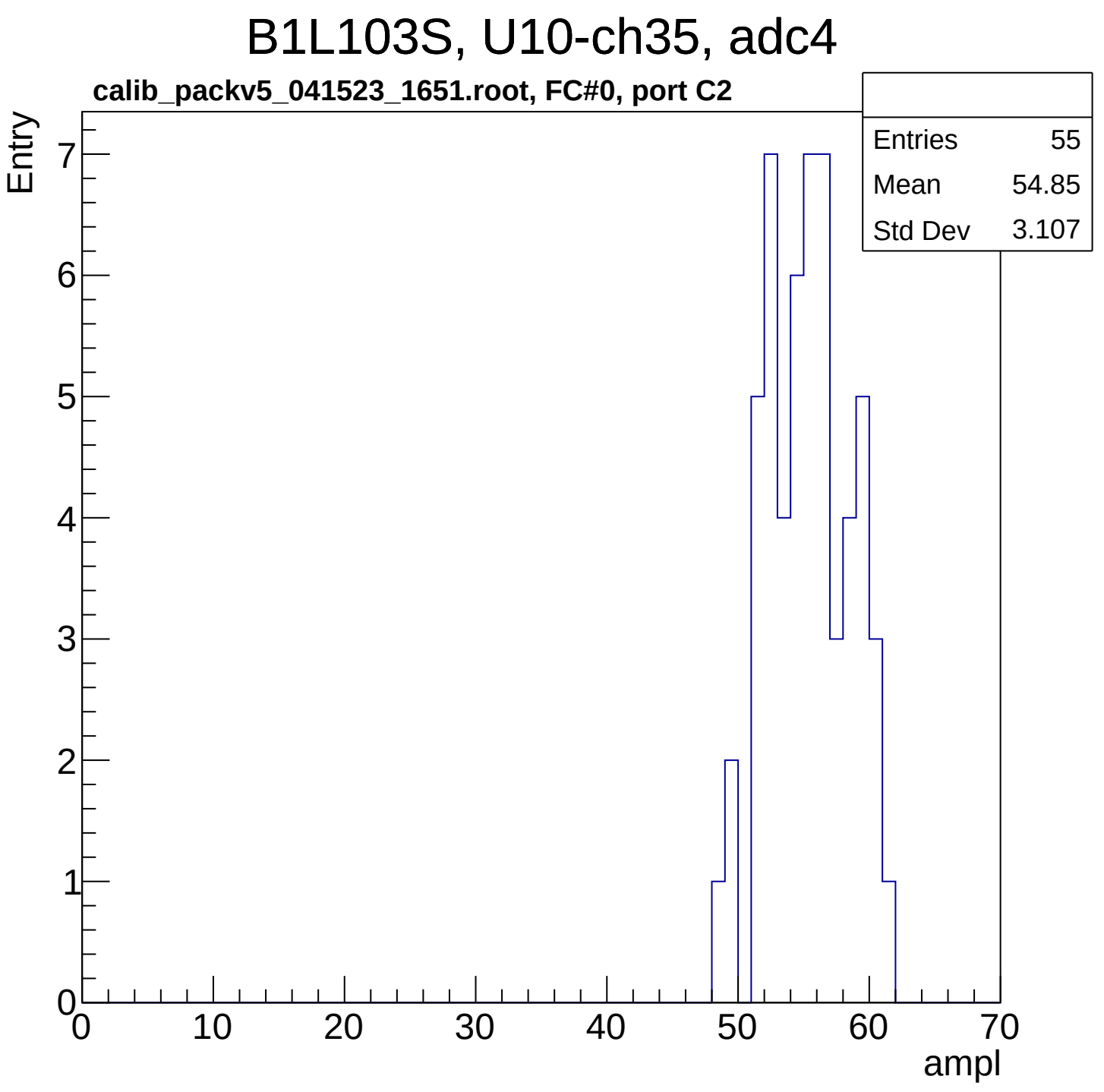
B1L103S, U10-ch35, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 54.85
Std Dev 3.107
Entry
ampl
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2
3
4
5
6
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0
10
20
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40
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60
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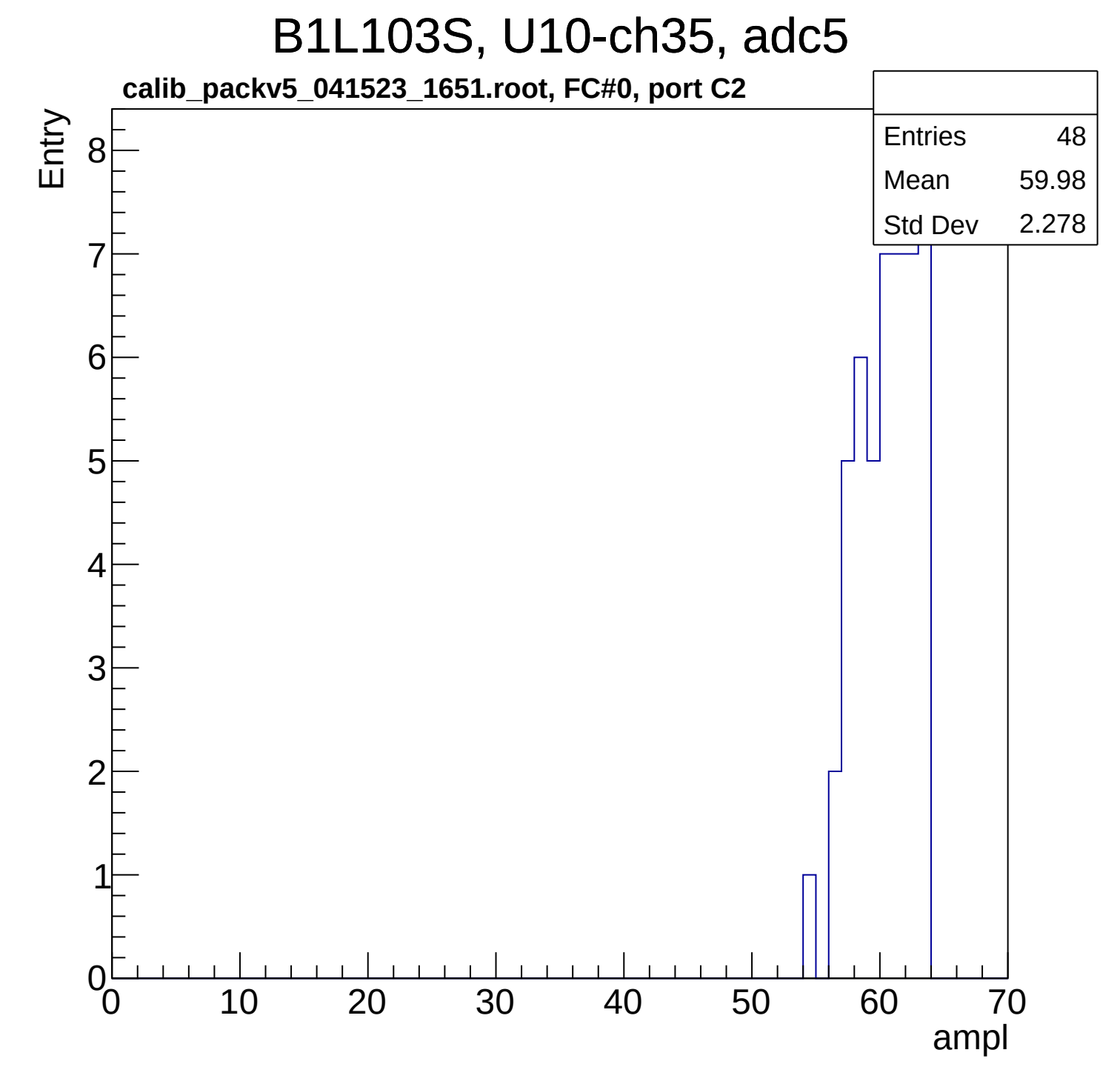
B1L103S, U10-ch35, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 59.98
Std Dev 2.278
Entry
ampl
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4
5
6
7
8
0
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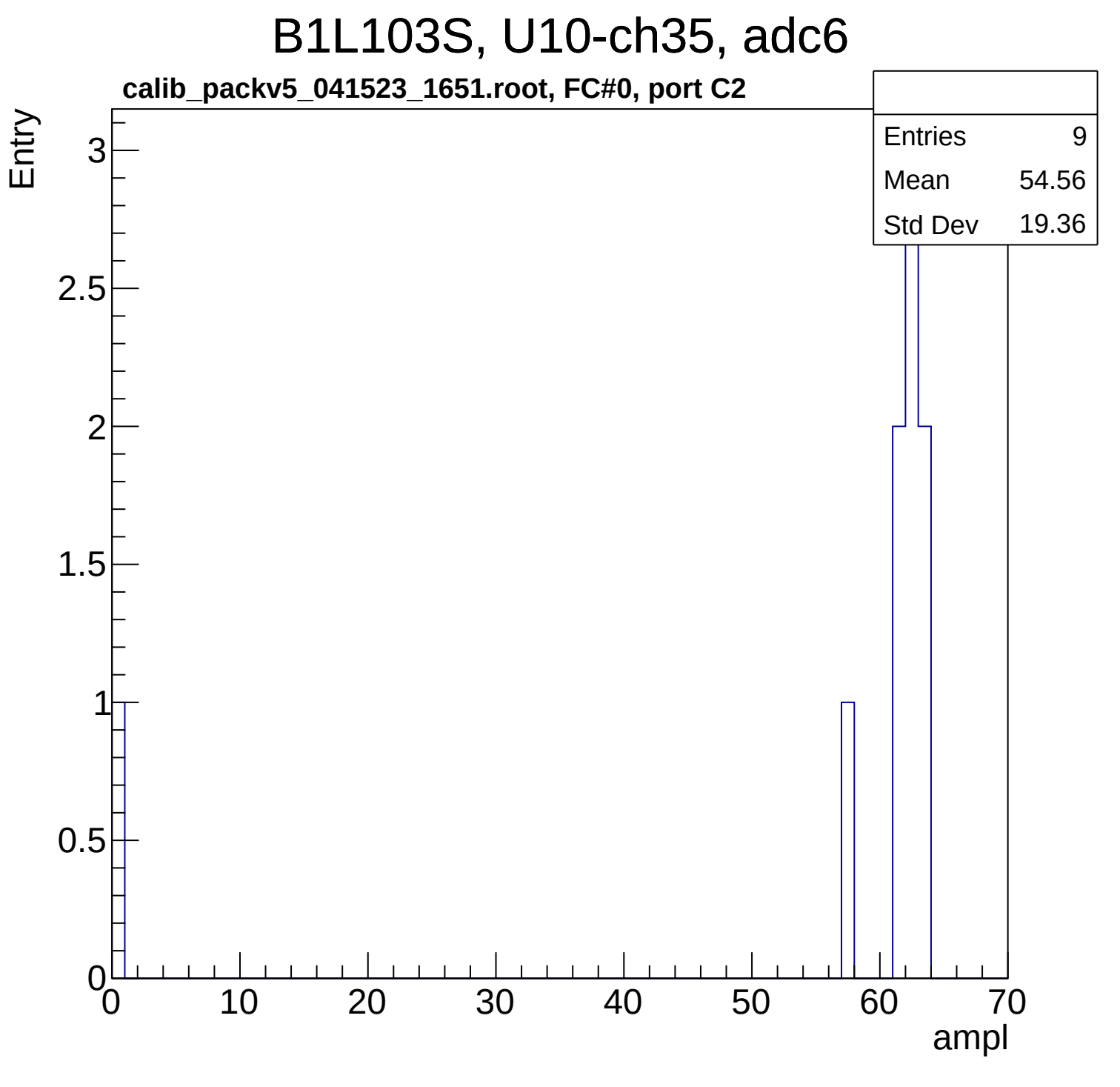
B1L103S, U10-ch35, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 9
Mean 54.56
Std Dev 19.36
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
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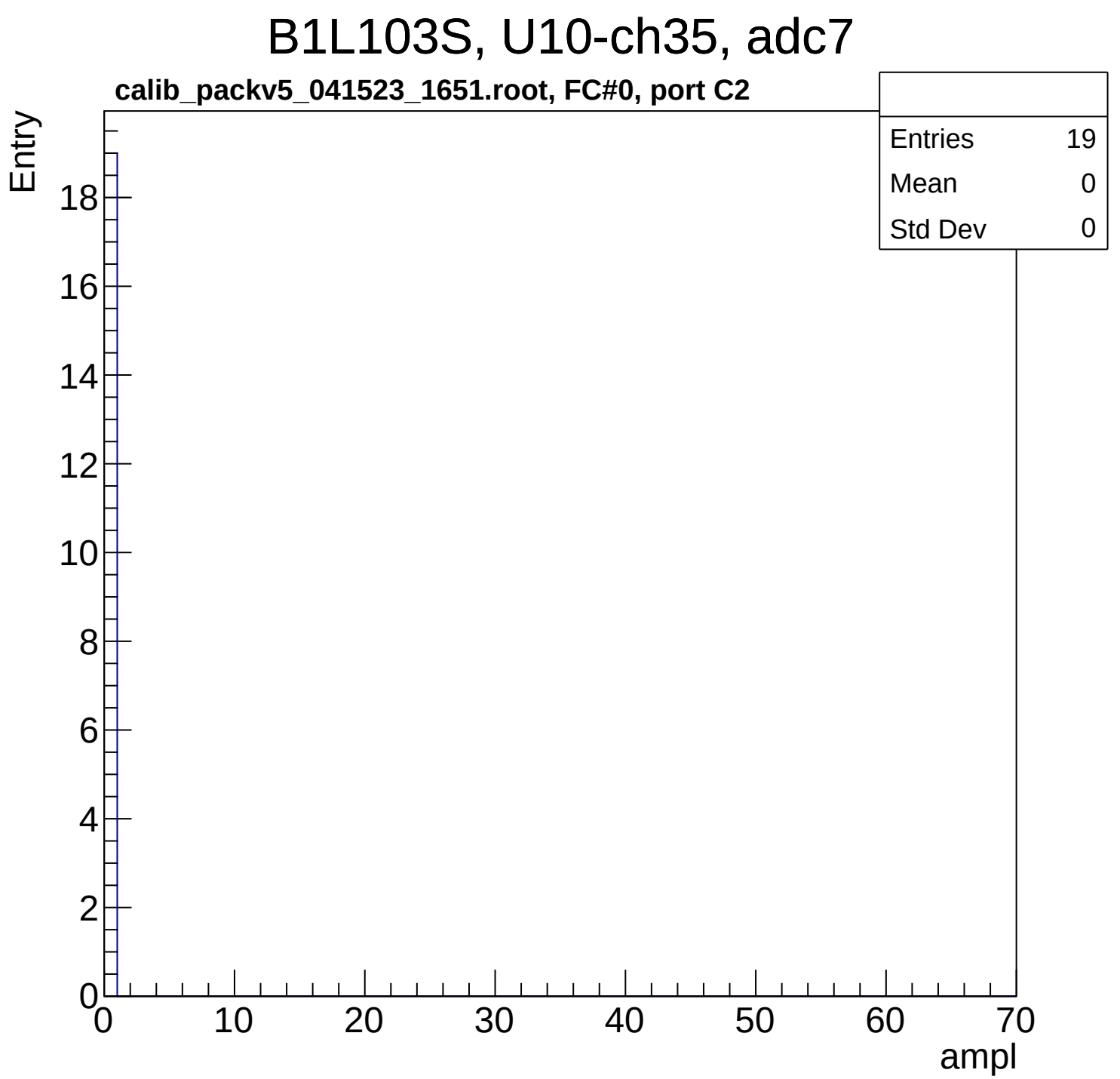
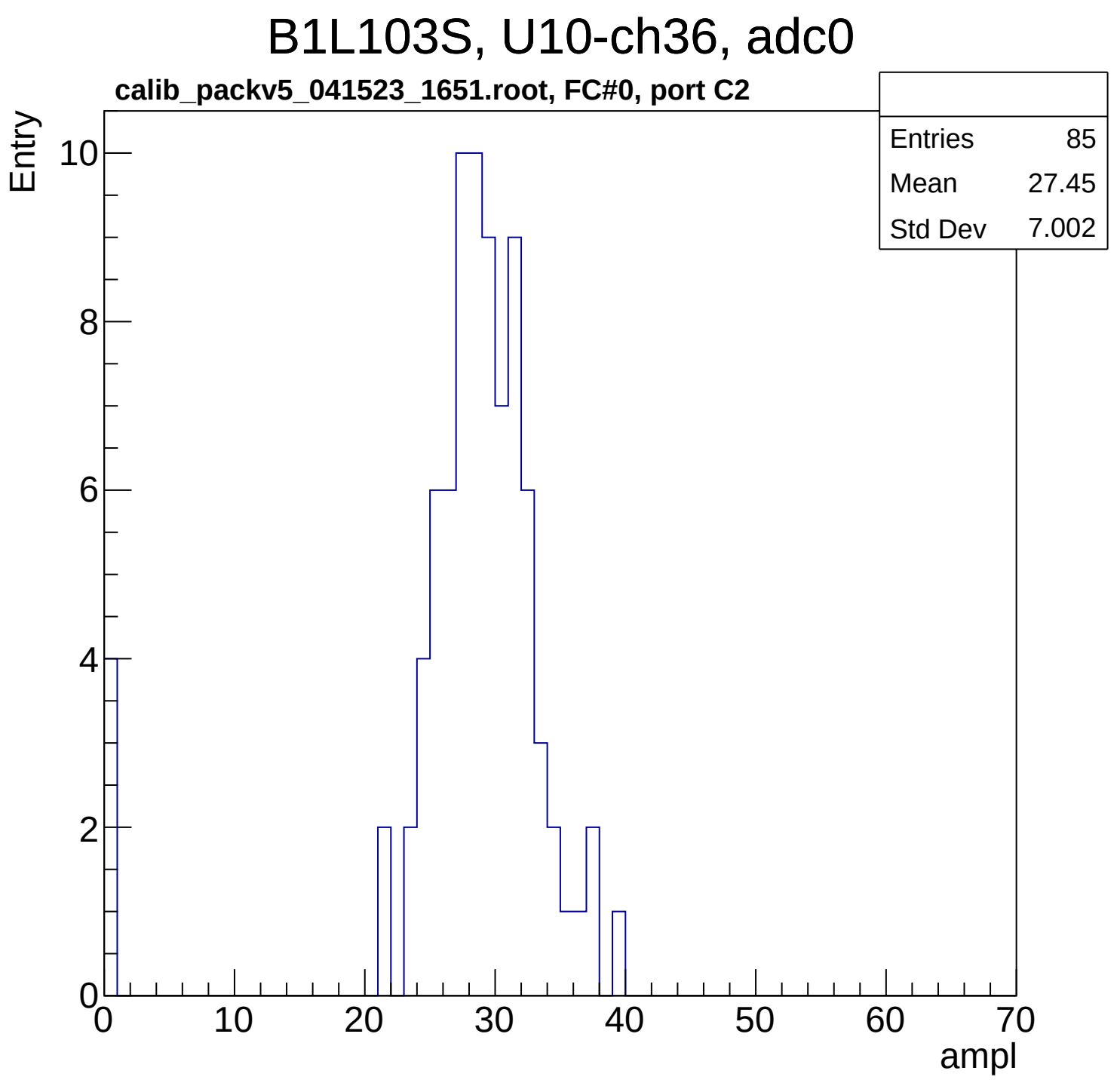
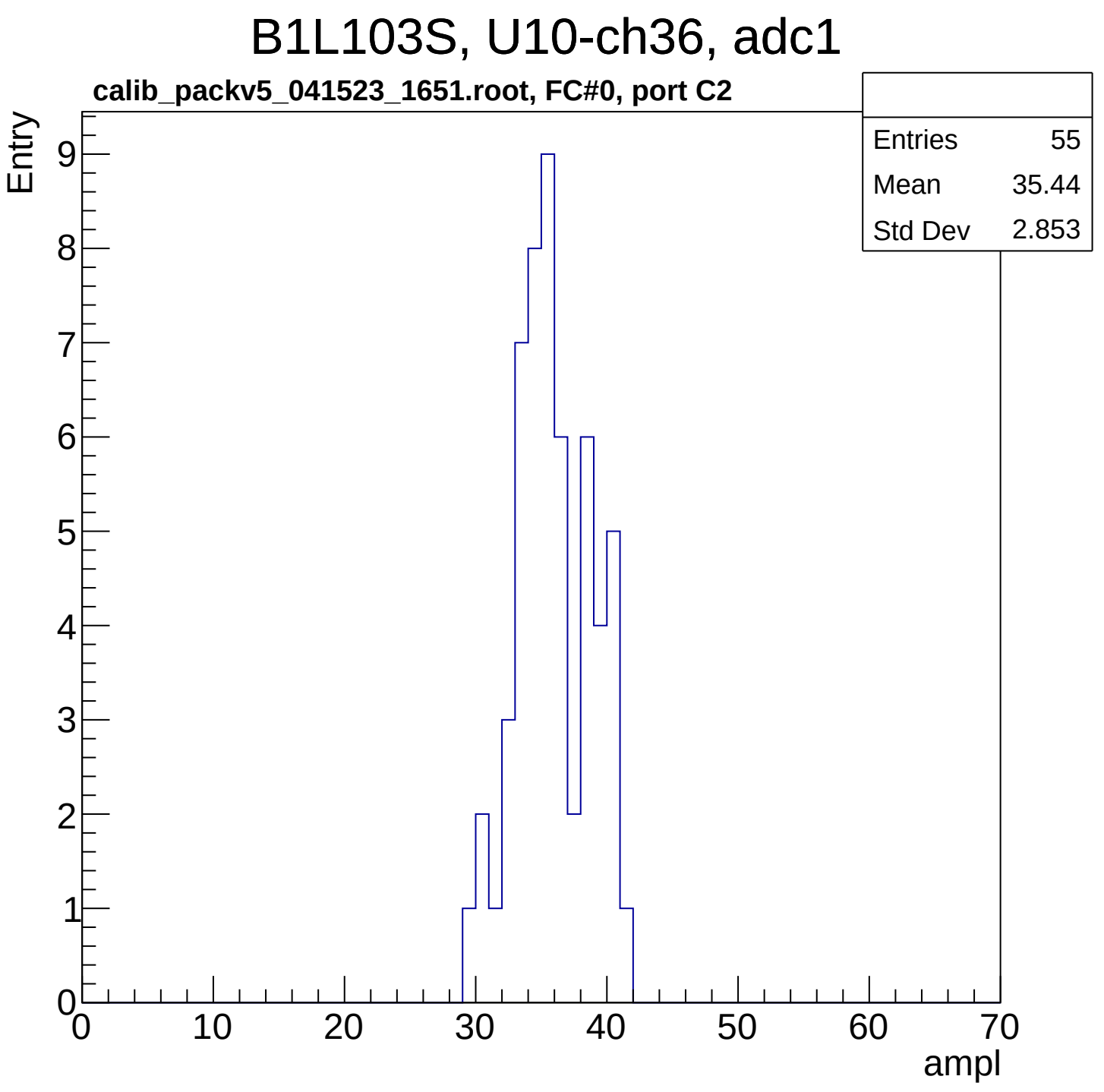

B1L103S, U10-ch35, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch36, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 27.45
Std Dev 7.002
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U10-ch36, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 35.44
Std Dev 2.853
Entry
ampl
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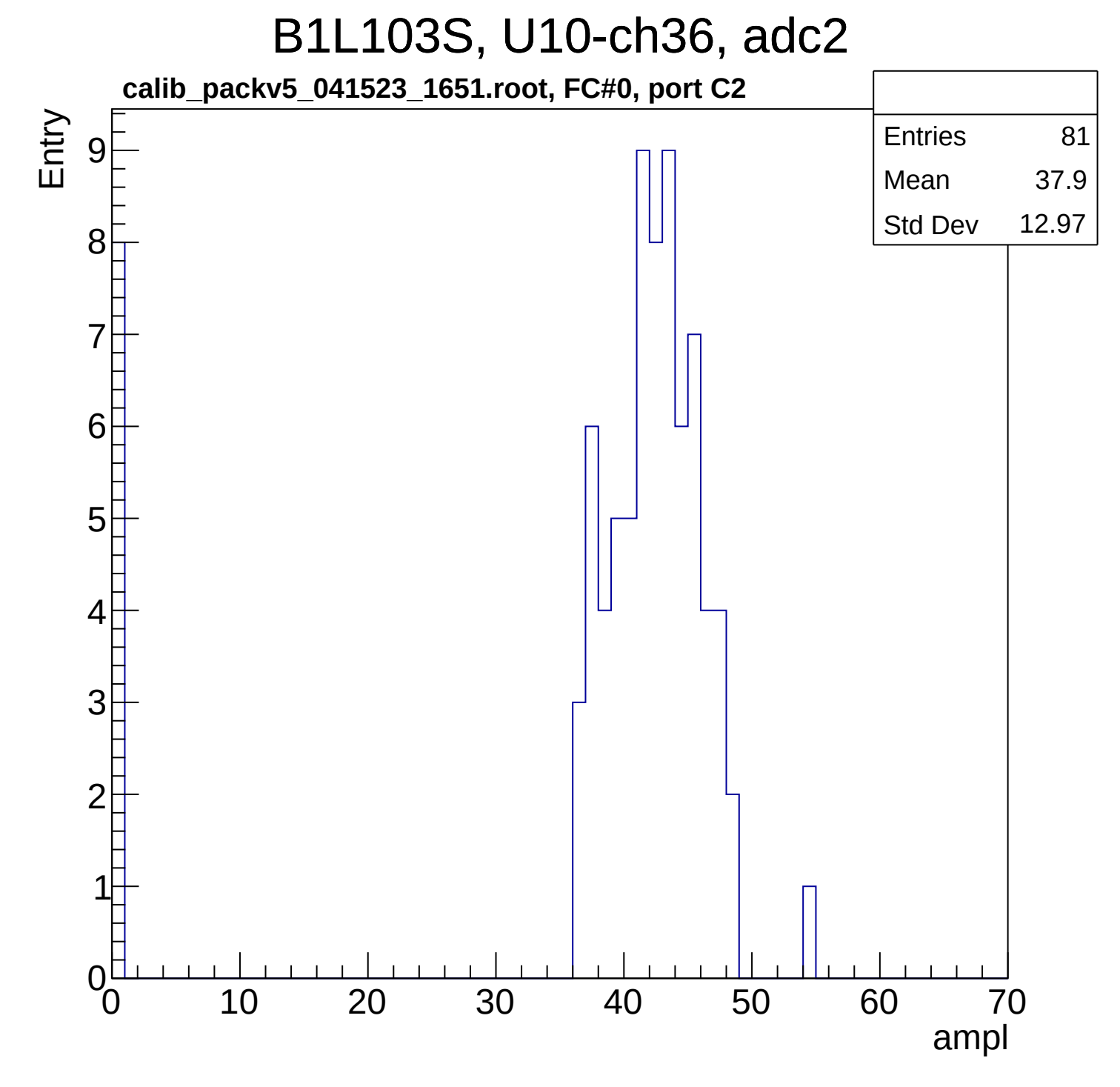
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U10-ch36, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 37.9
Std Dev 12.97
Entry
ampl
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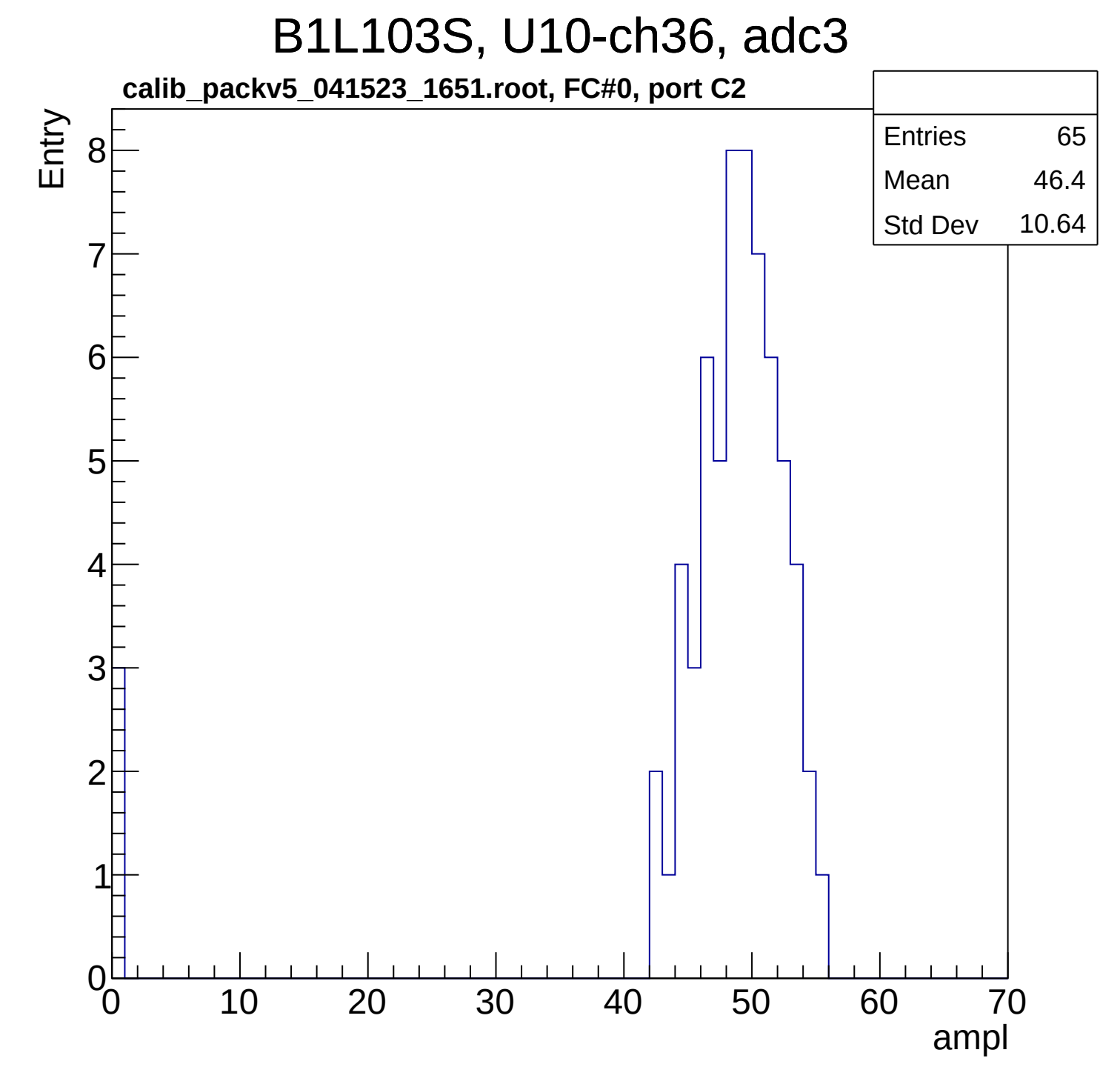
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U10-ch36, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 46.4
Std Dev 10.64
Entry
ampl
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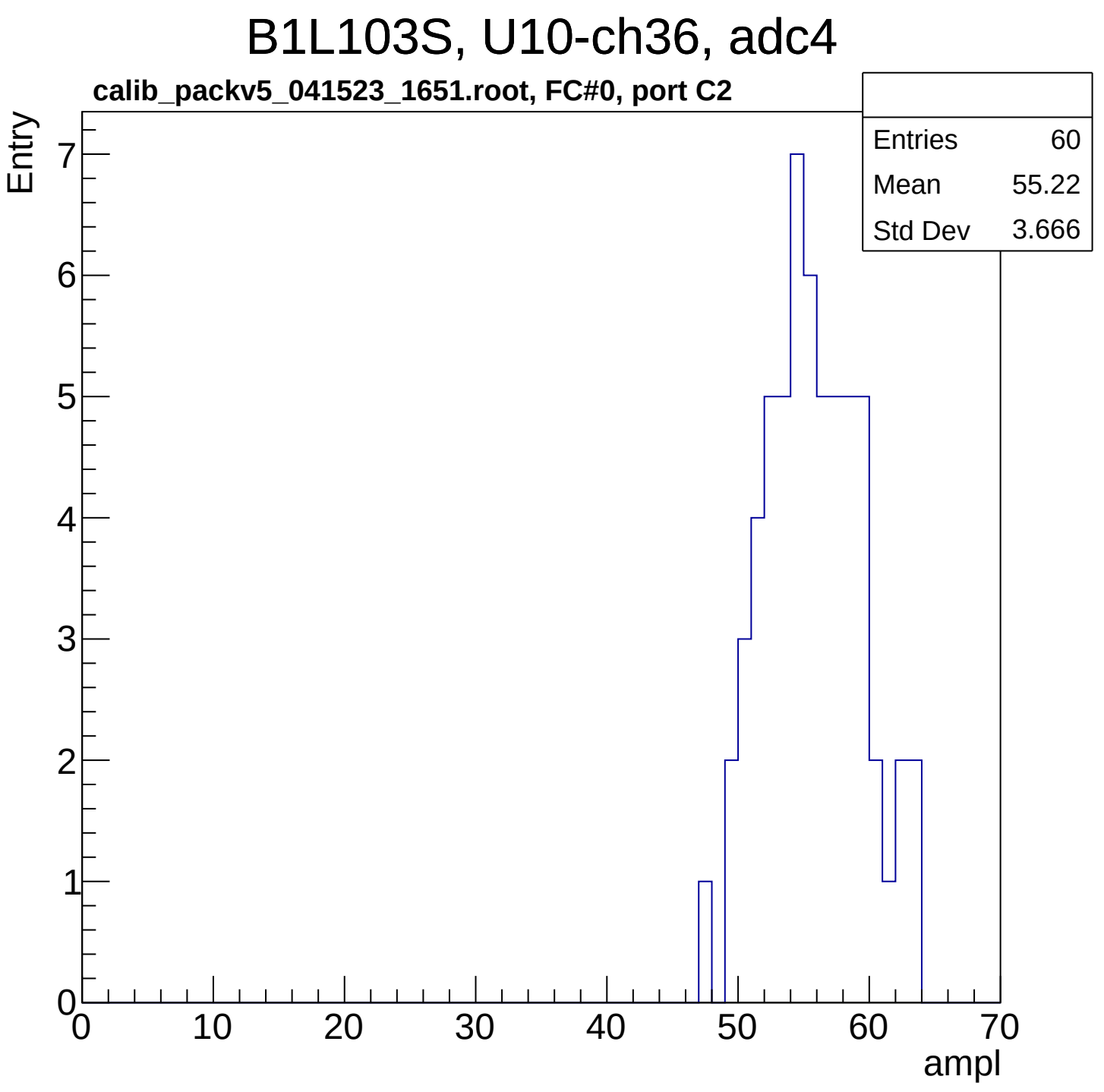
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U10-ch36, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 55.22
Std Dev 3.666
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
30
40
50
60
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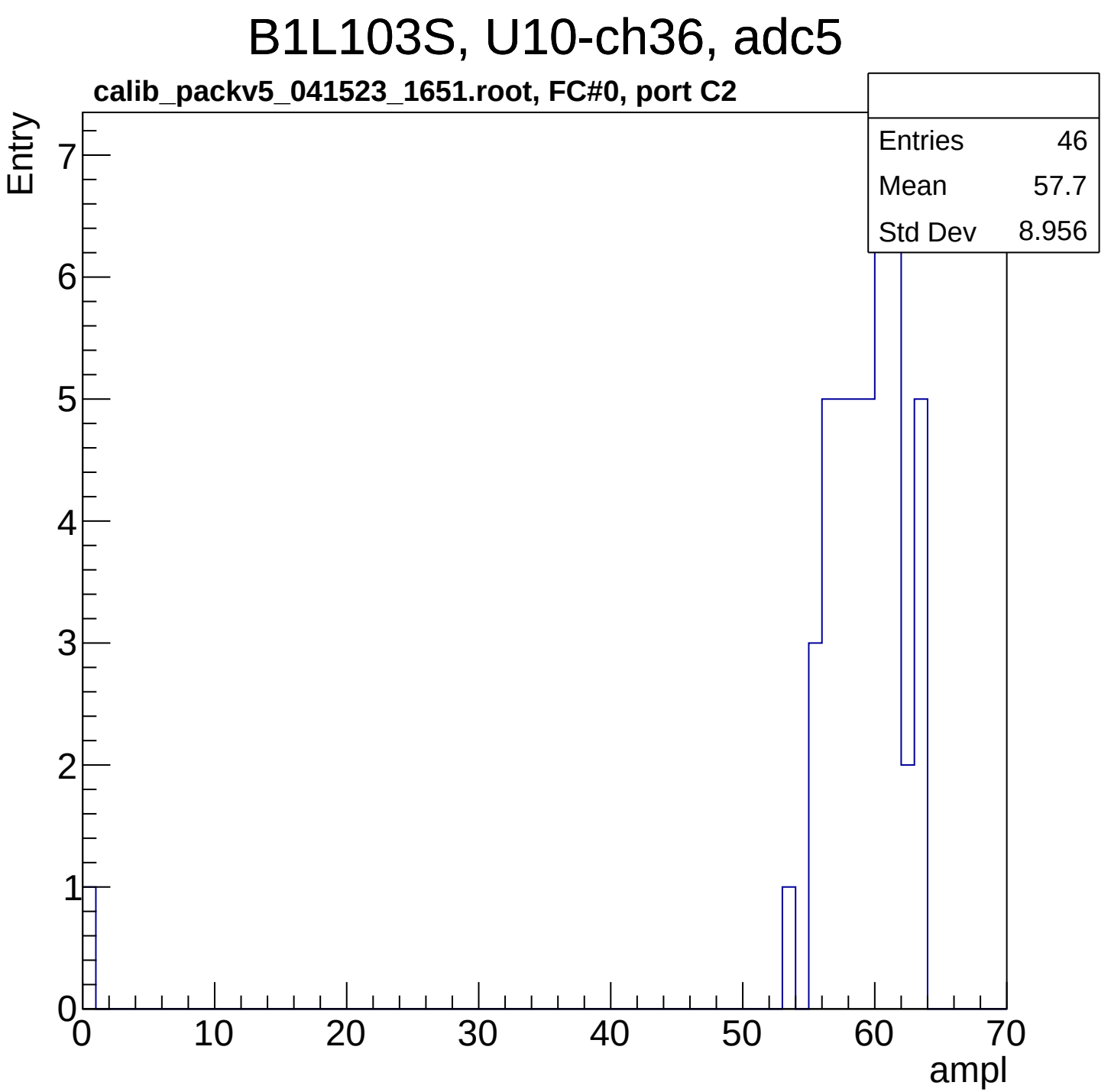
B1L103S, U10-ch36, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 57.7
Std Dev 8.956
Entry
ampl
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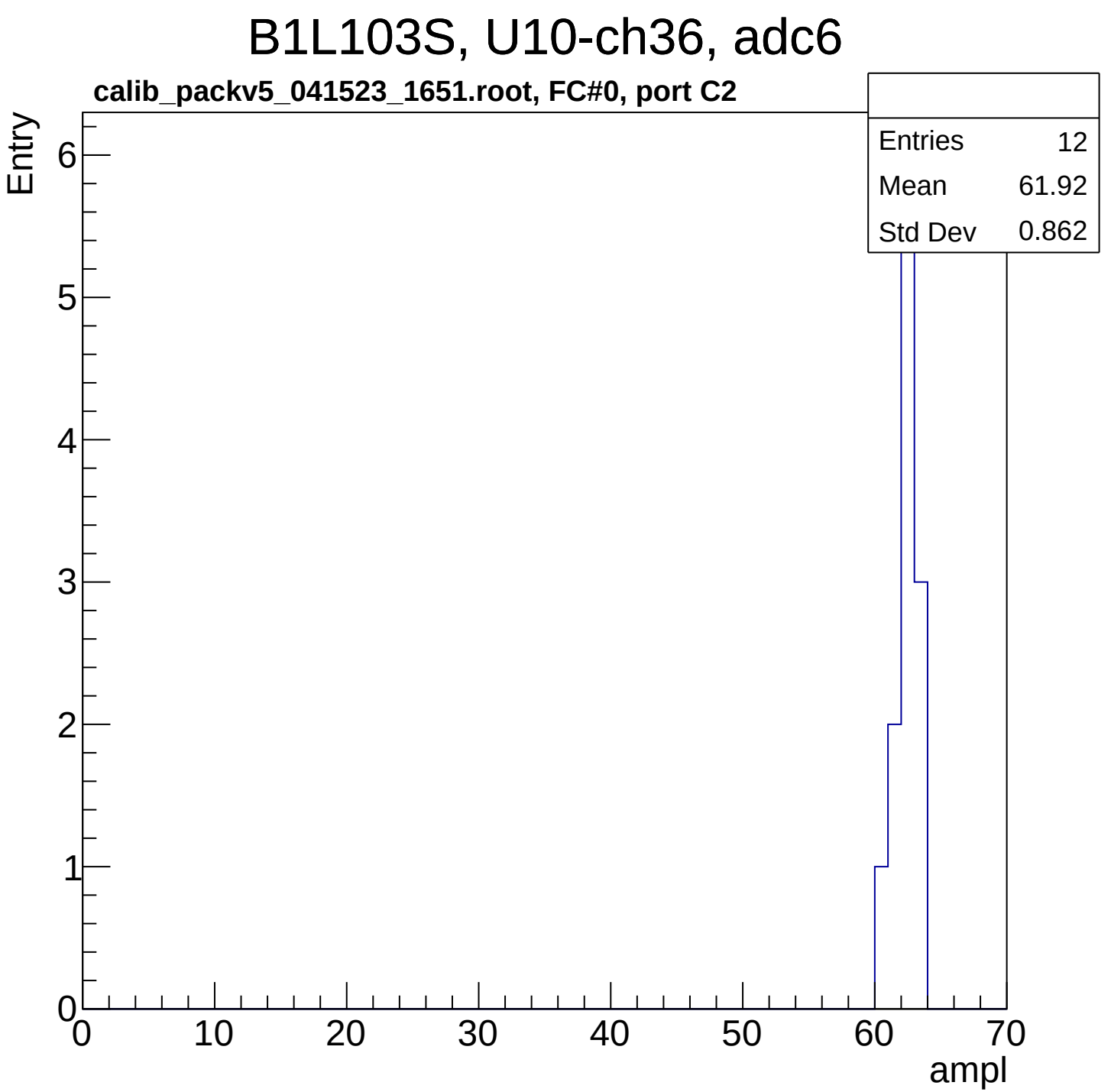
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U10-ch36, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 61.92
Std Dev 0.862
Entry
ampl
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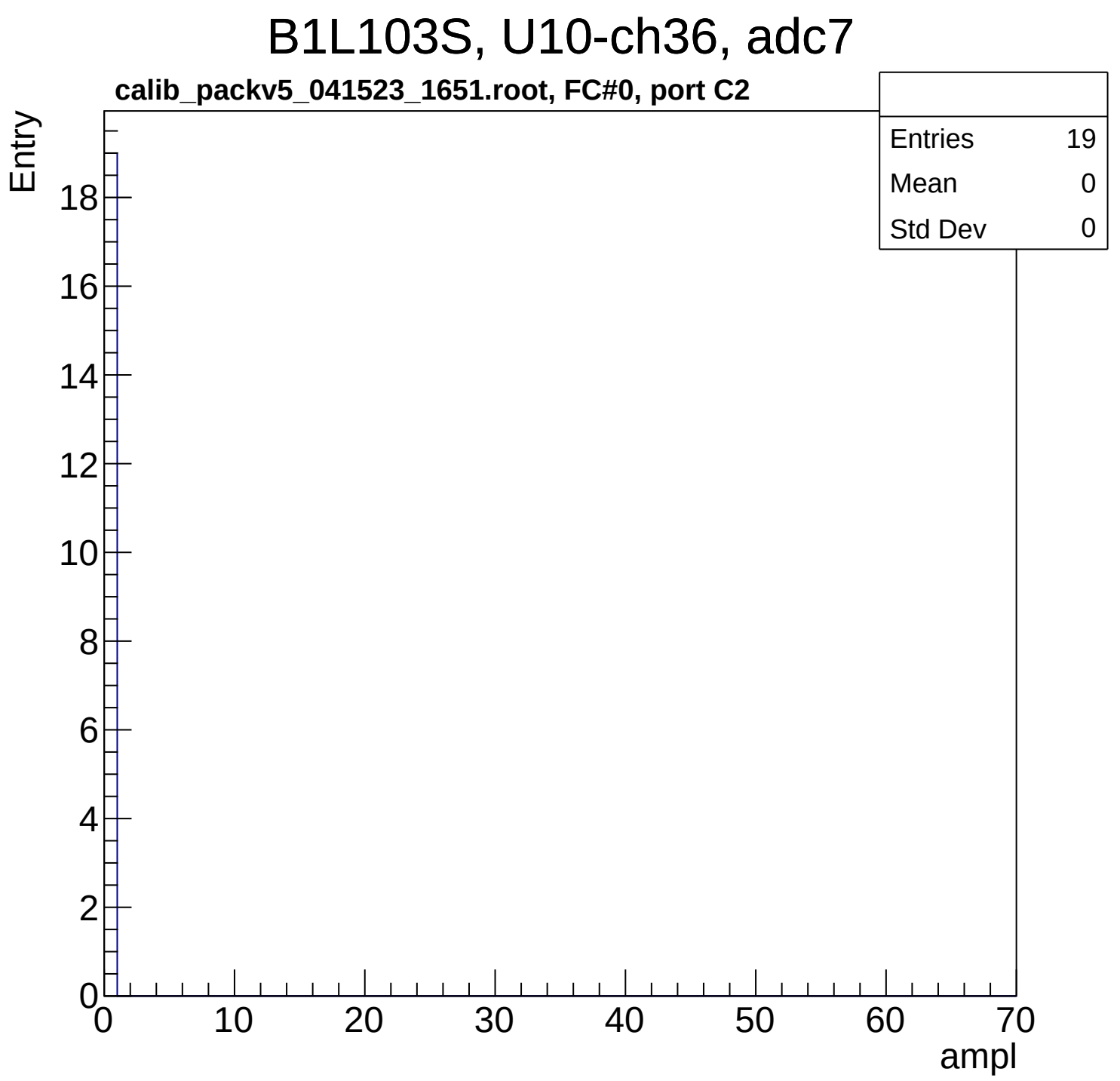
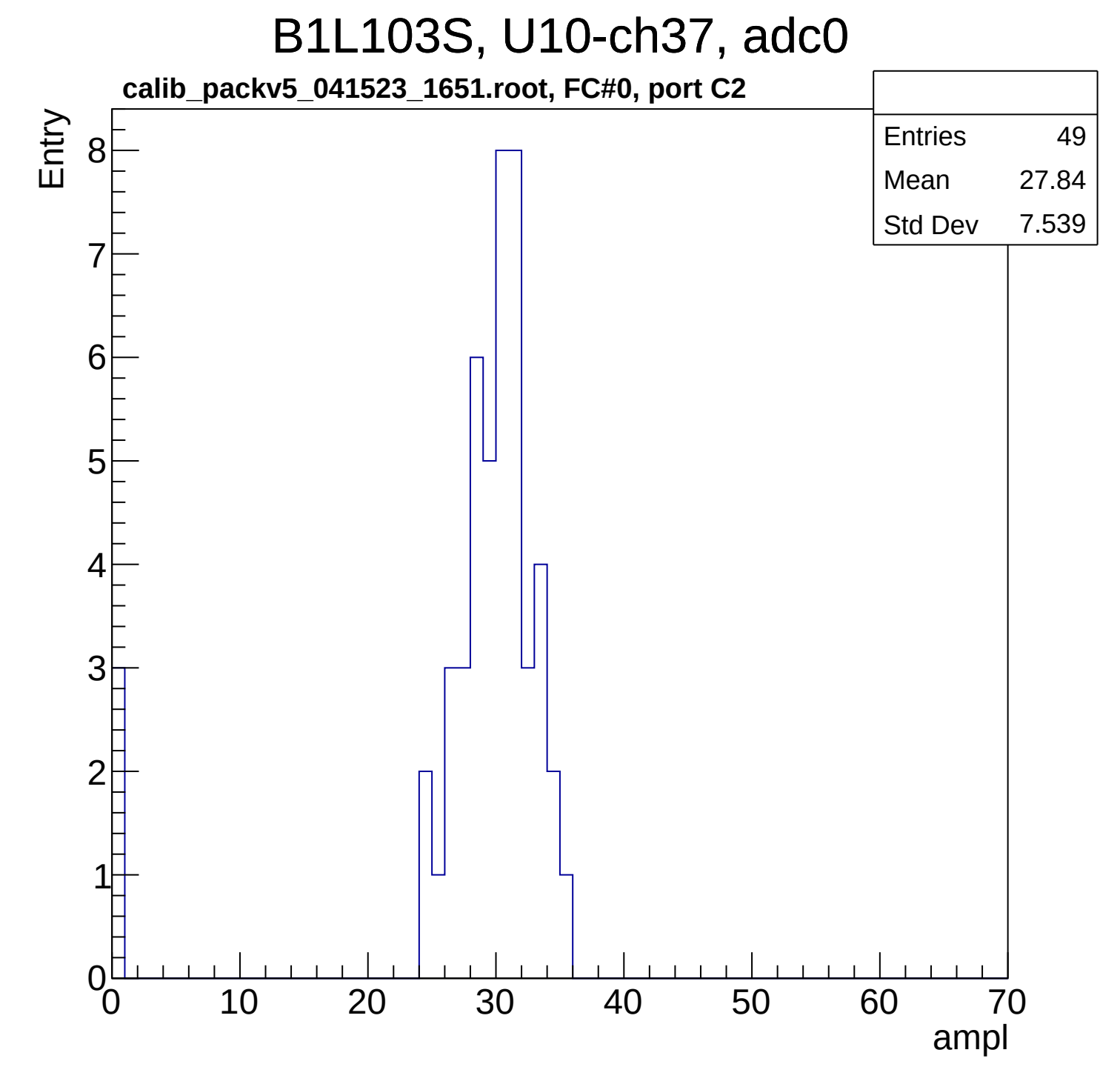
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U10-ch36, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch37, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 27.84
Std Dev 7.539
Entry
ampl
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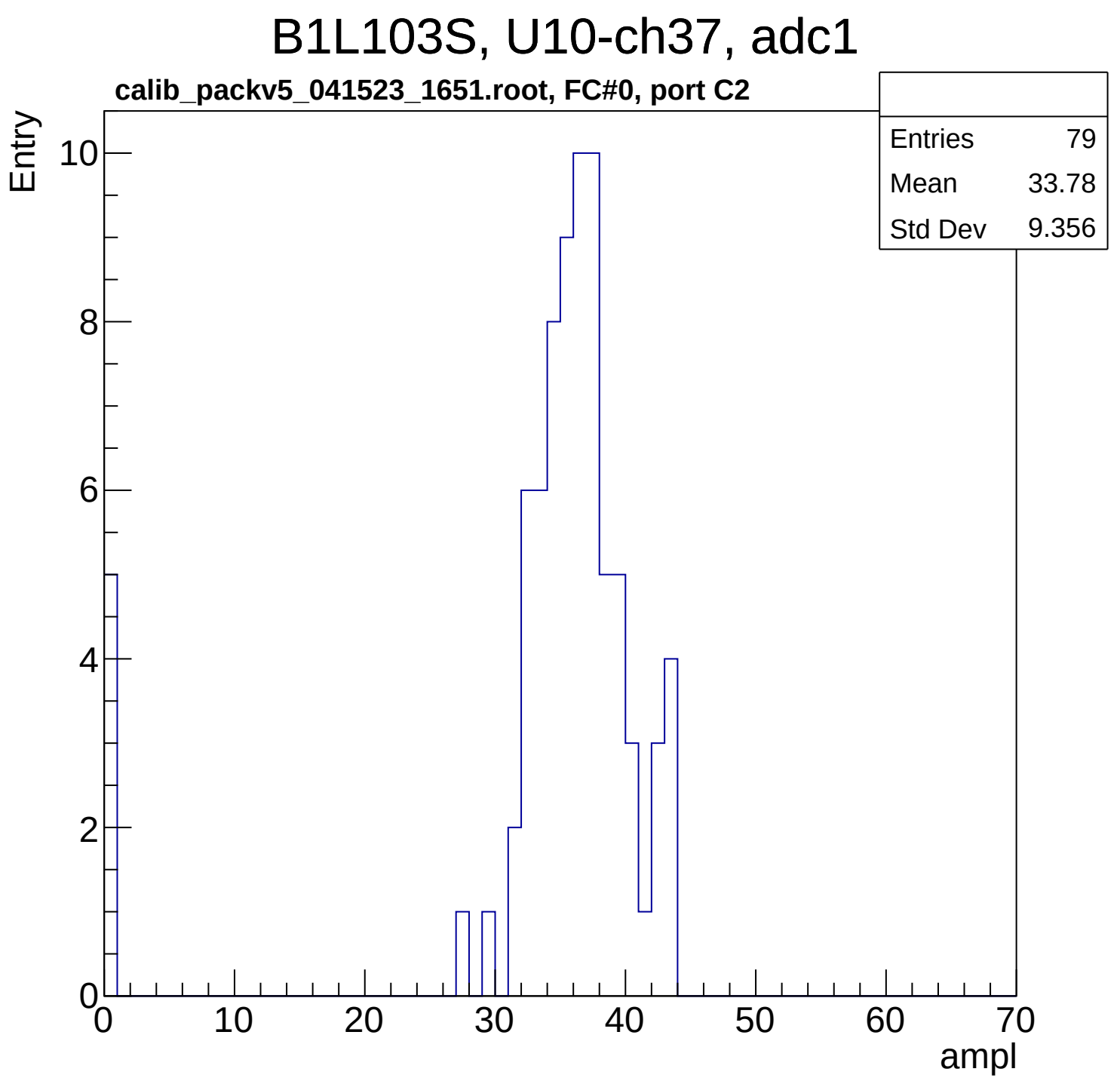
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U10-ch37, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 33.78
Std Dev 9.356
Entry
ampl
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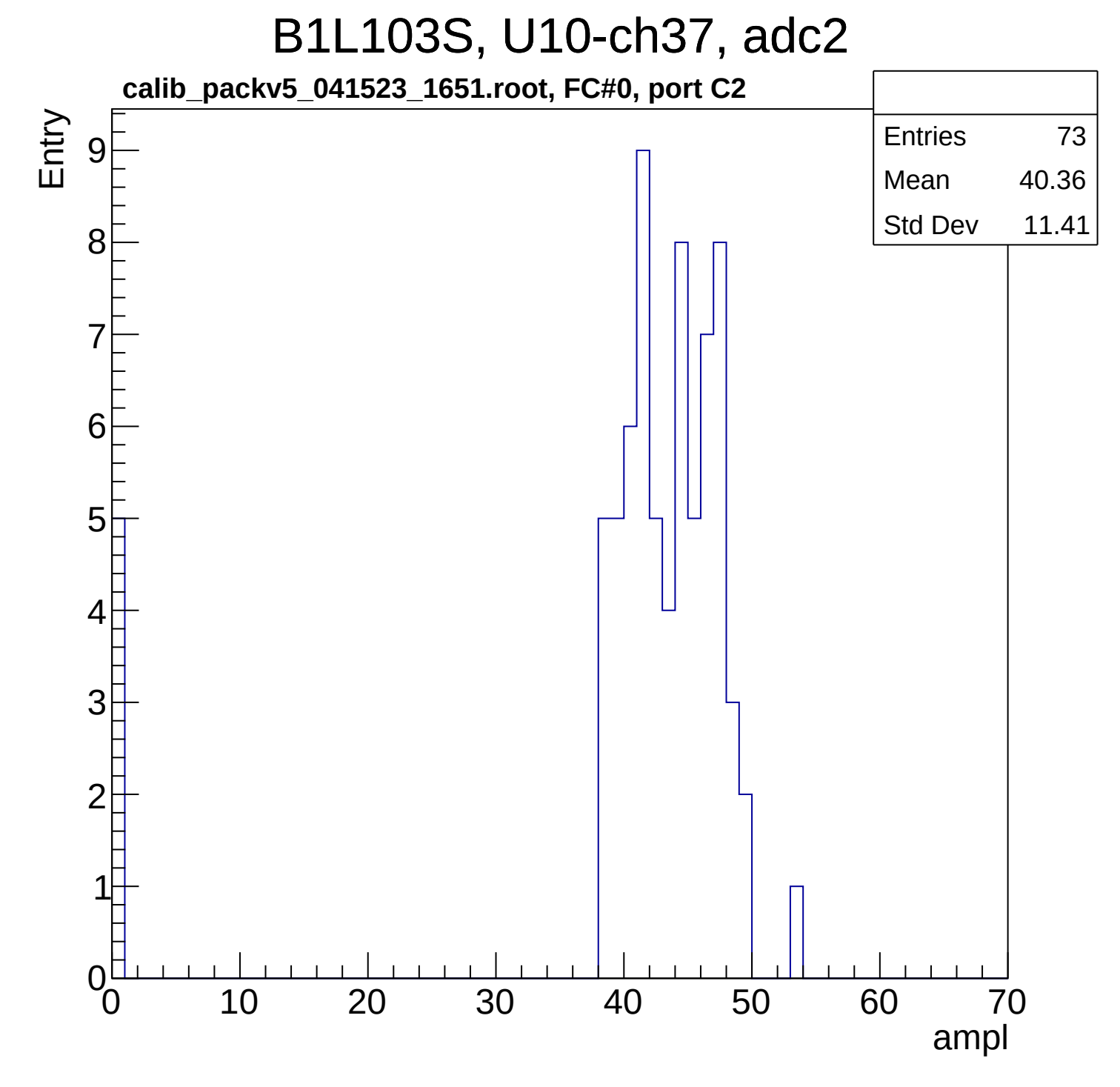
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U10-ch37, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 40.36
Std Dev 11.41
Entry
ampl
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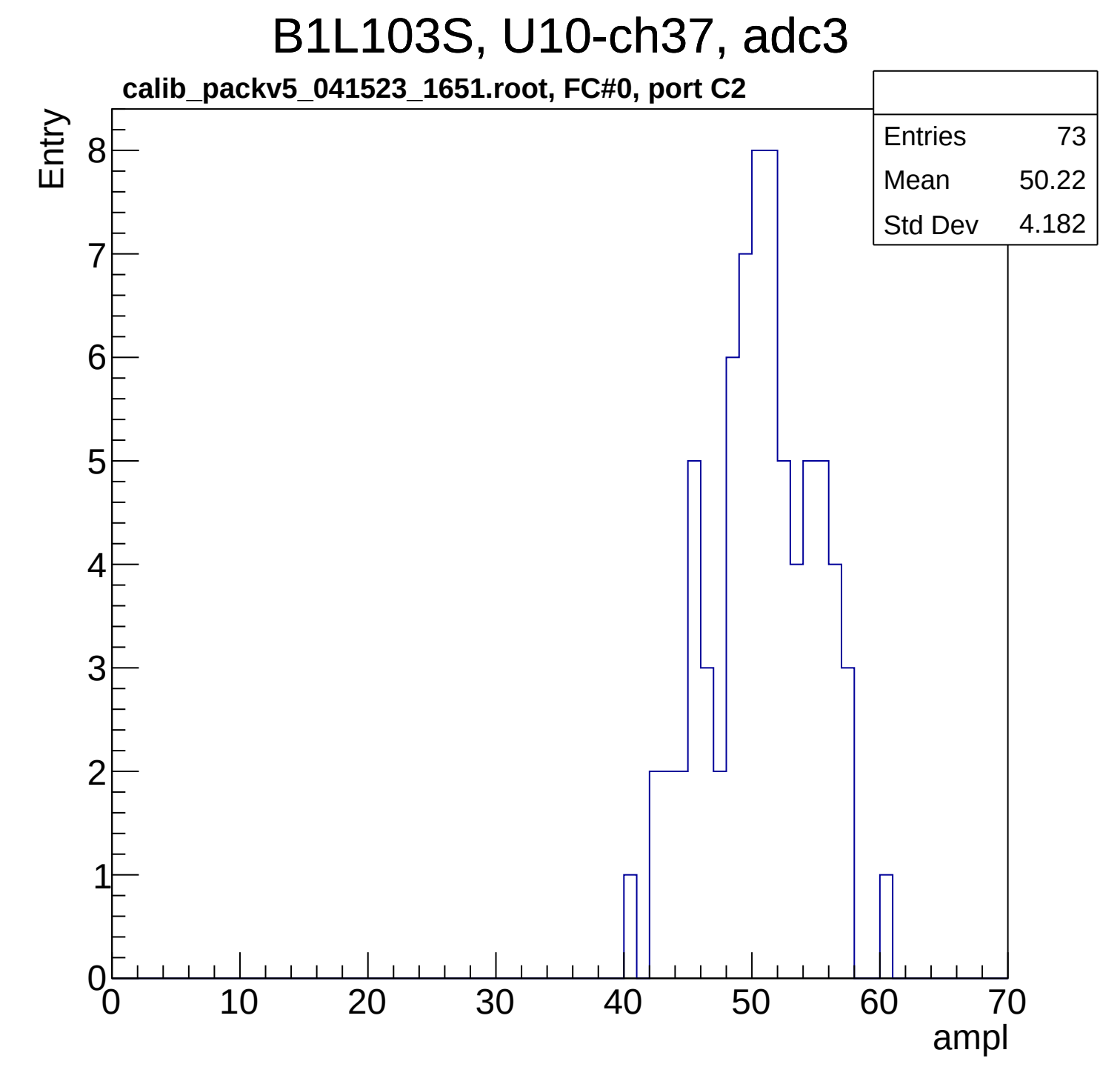
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U10-ch37, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 50.22
Std Dev 4.182
Entry
ampl
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2
3
4
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6
7
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0
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60
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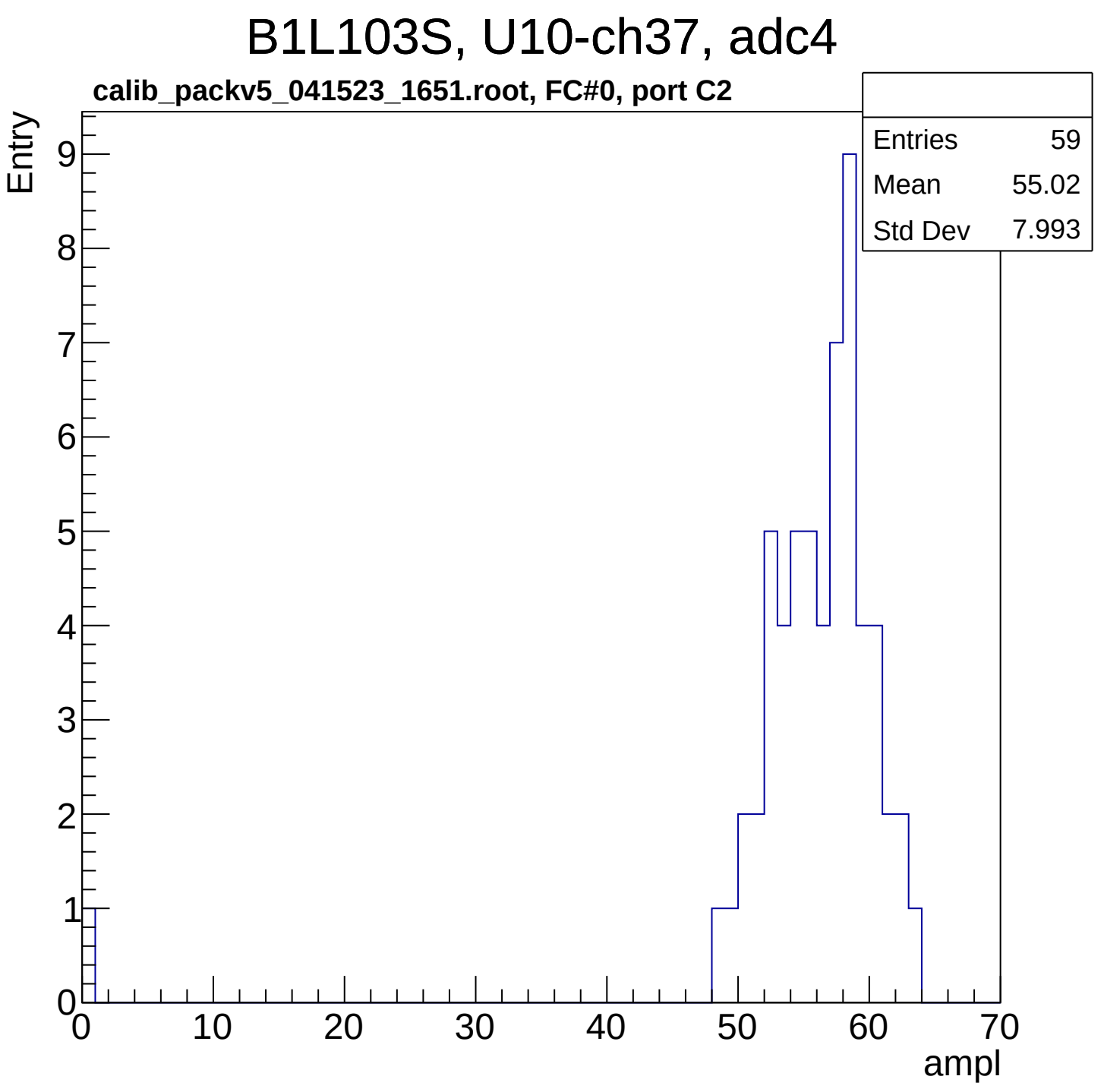
B1L103S, U10-ch37, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 55.02
Std Dev 7.993
Entry
ampl
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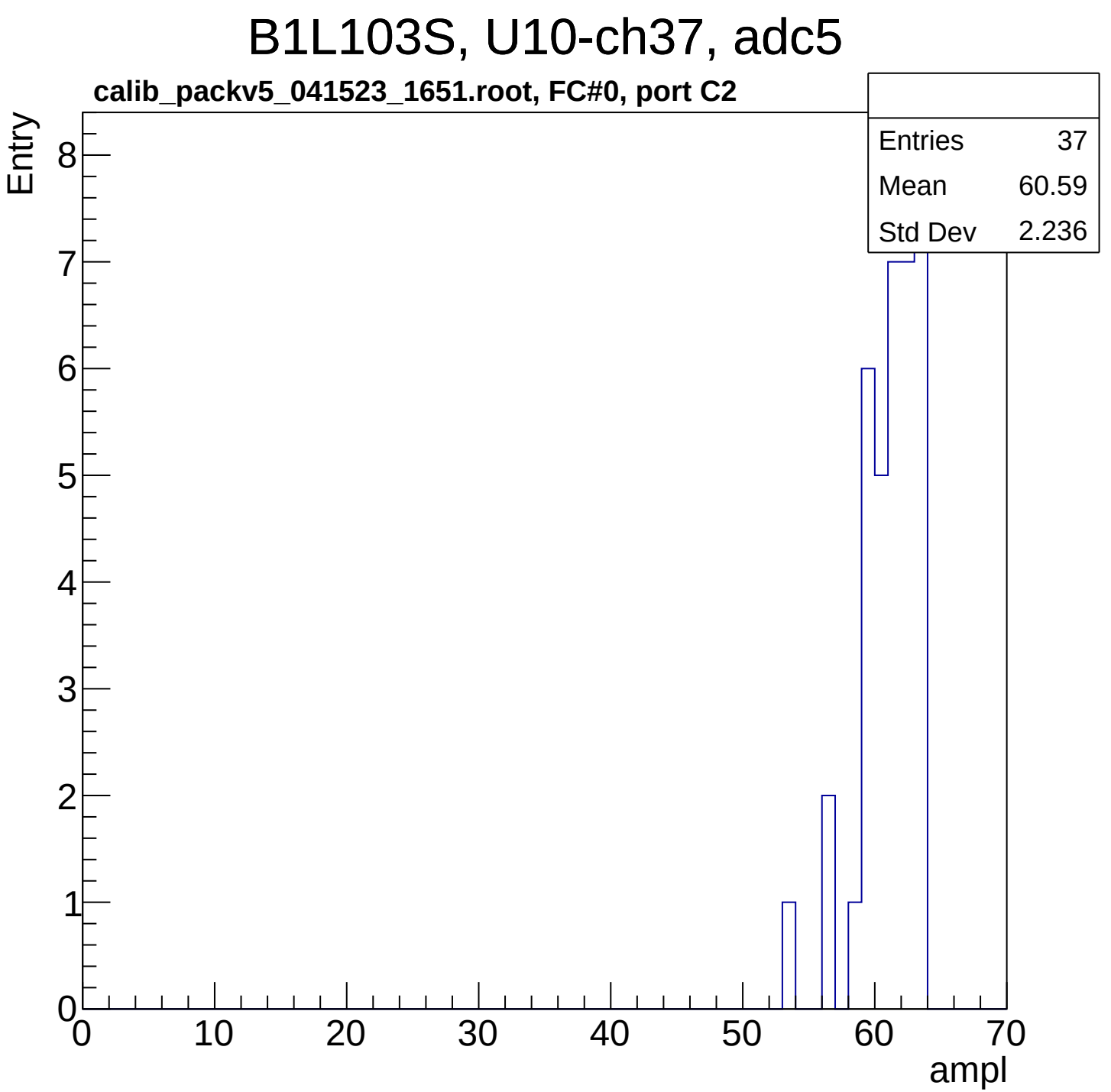
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U10-ch37, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 37
Mean 60.59
Std Dev 2.236
Entry
ampl
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1
2
3
4
5
6
7
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0
10
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40
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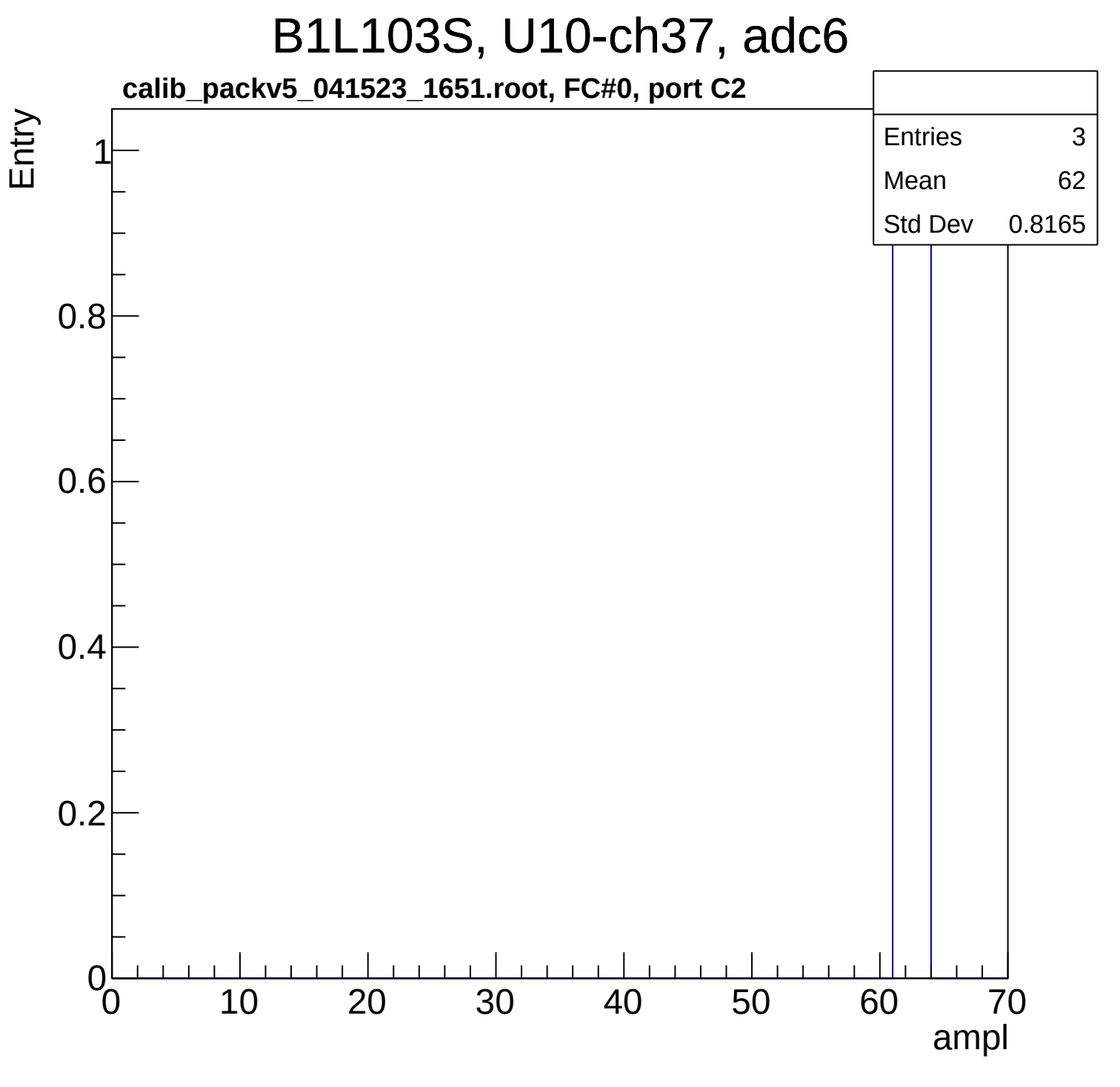
60
70


B1L103S, U10-ch37, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 3
Mean 62
Std Dev 0.8165
Entry
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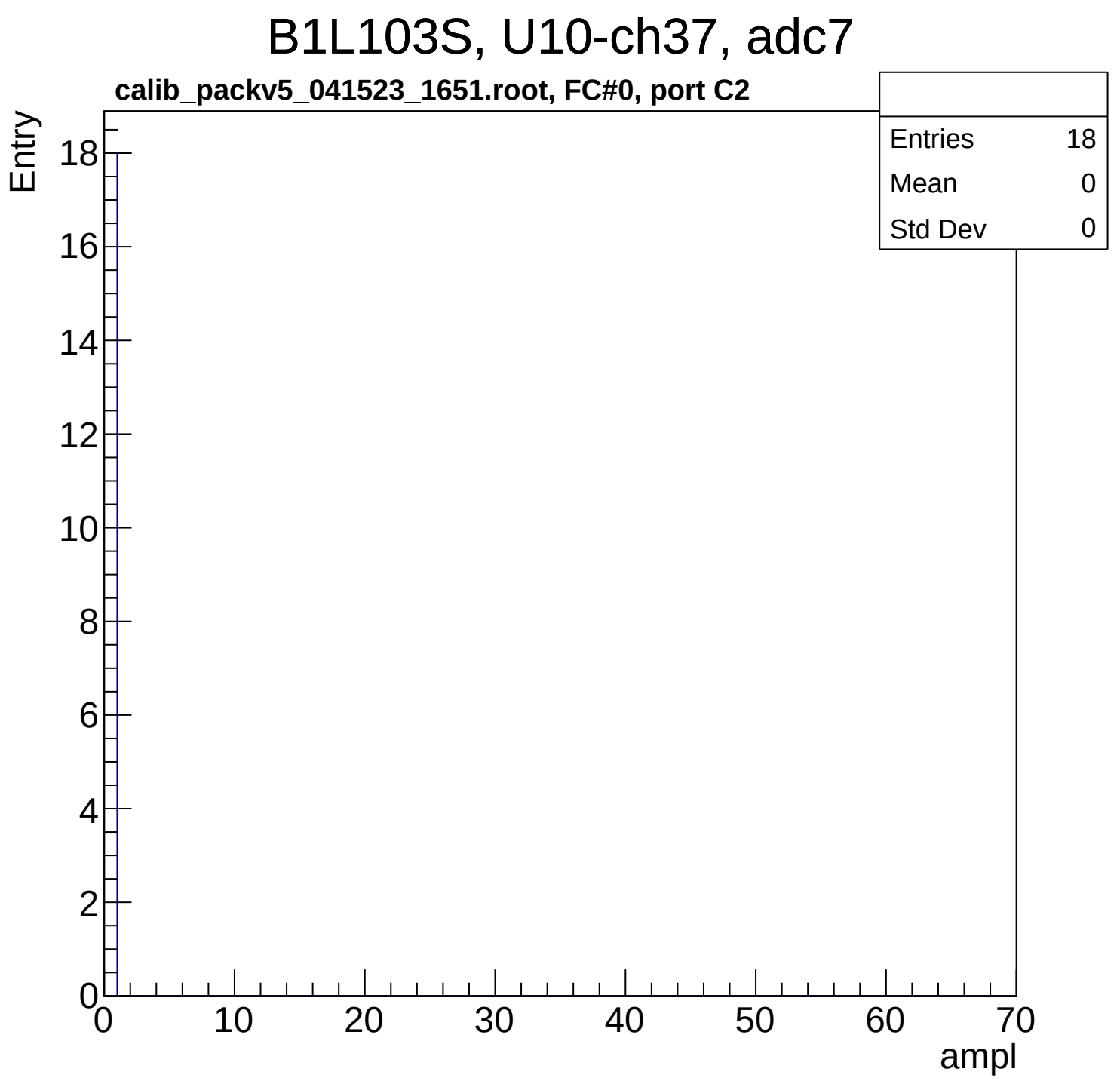
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch37, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
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10
20
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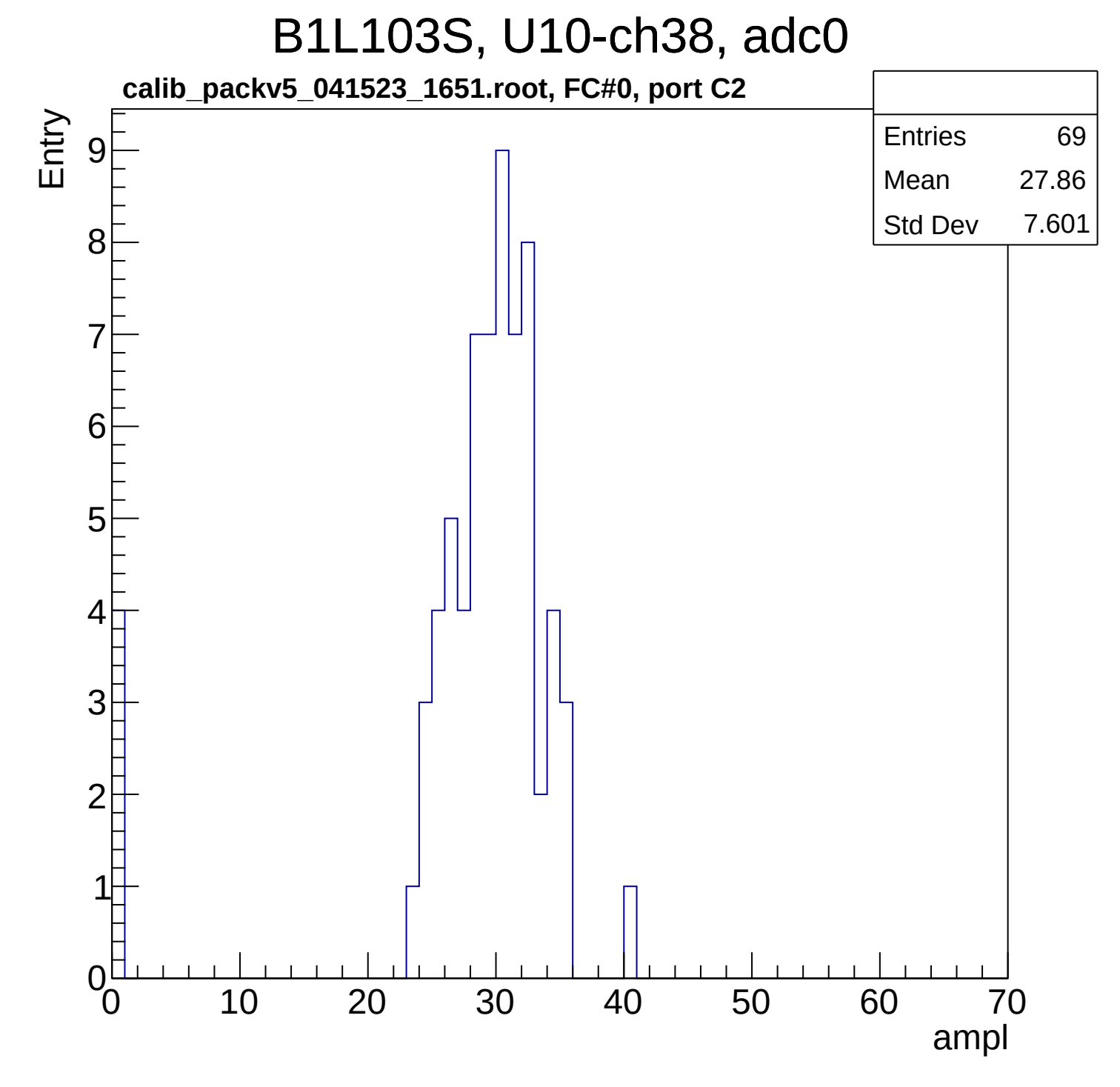
50
60
70
ampl


B1L103S, U10-ch38, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 27.86
Std Dev 7.601
Entry
ampl
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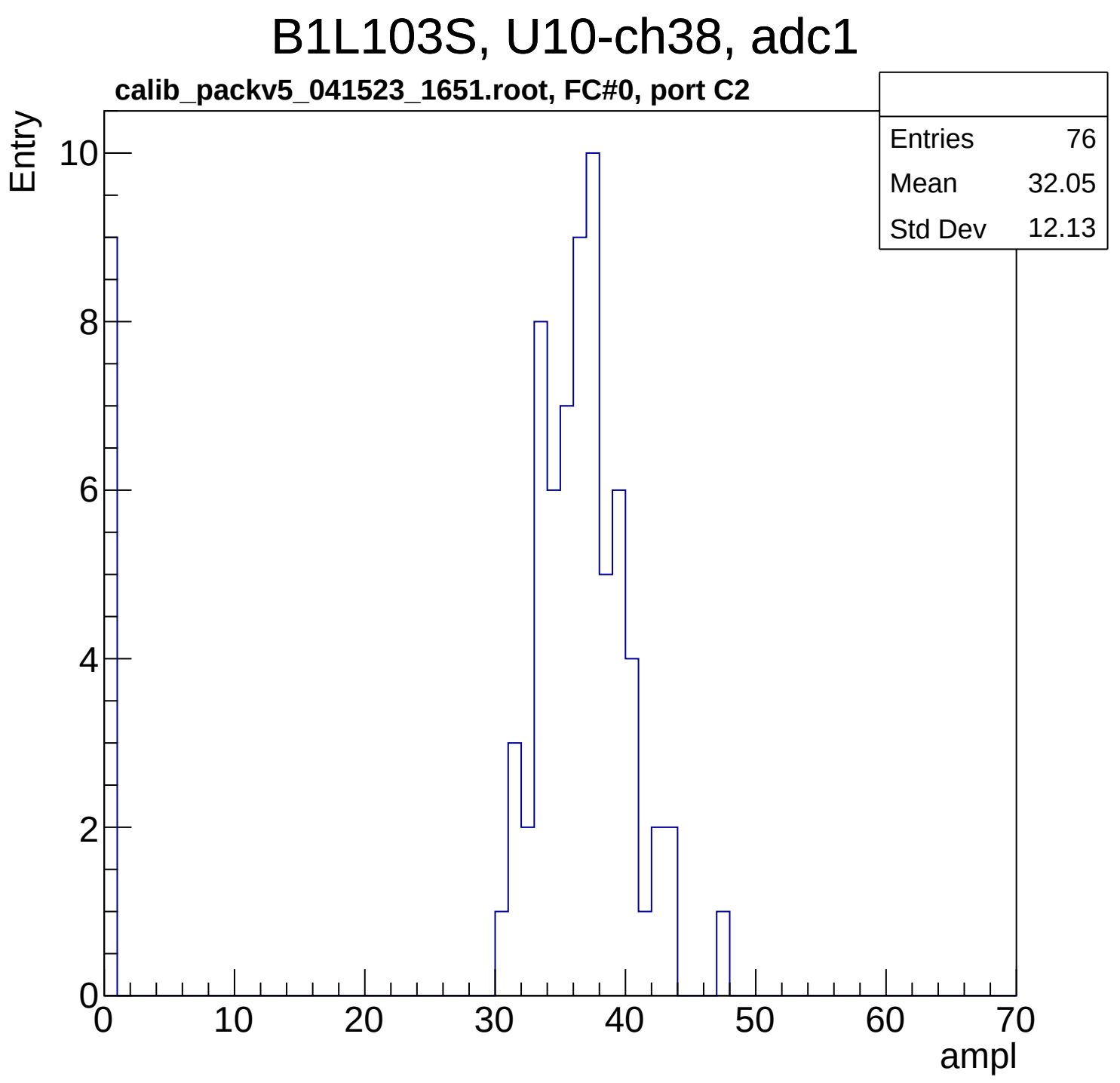
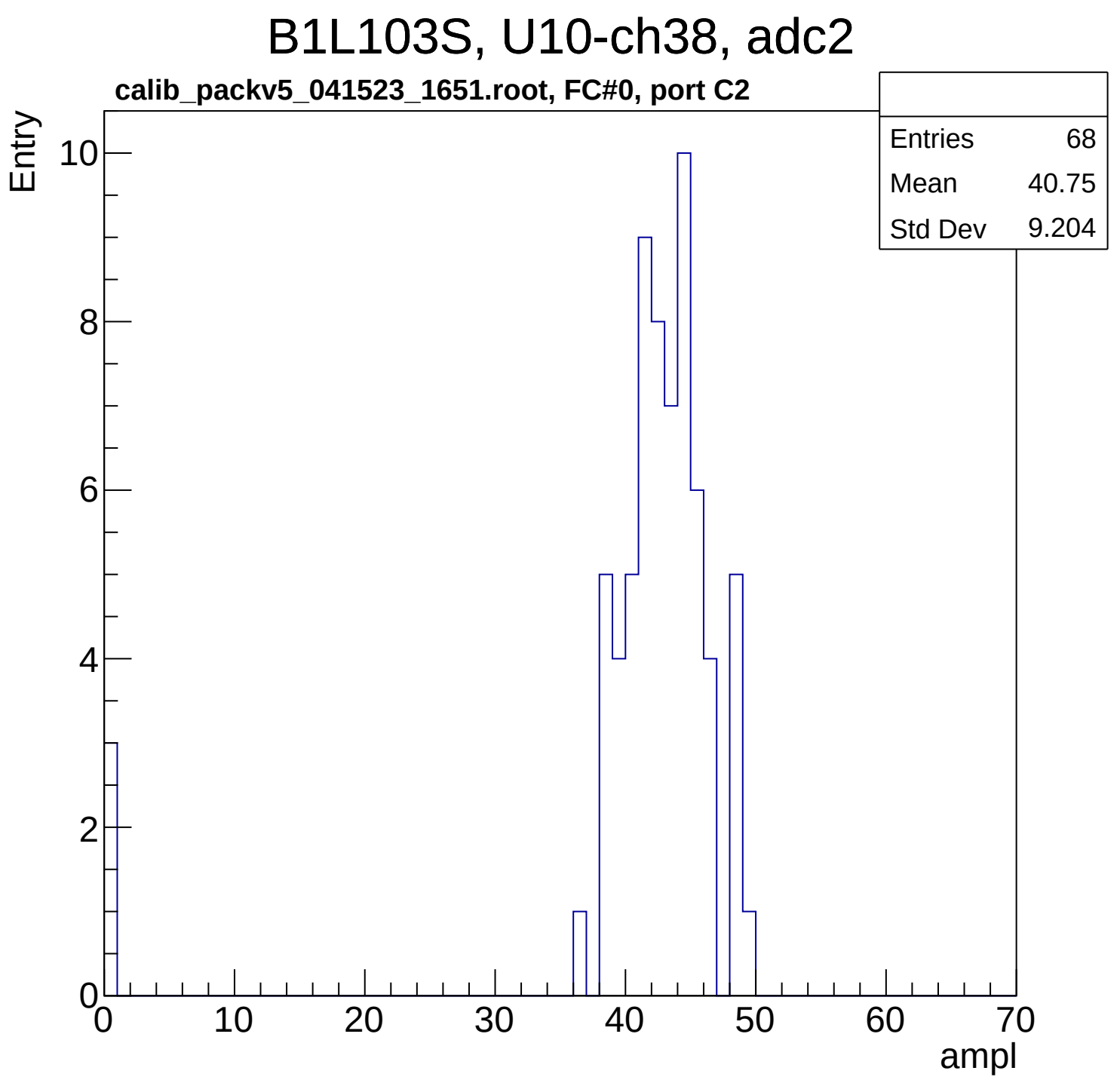
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U10-ch38, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 32.05
Std Dev 12.13
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U10-ch38, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 40.75
Std Dev 9.204
Entry
ampl
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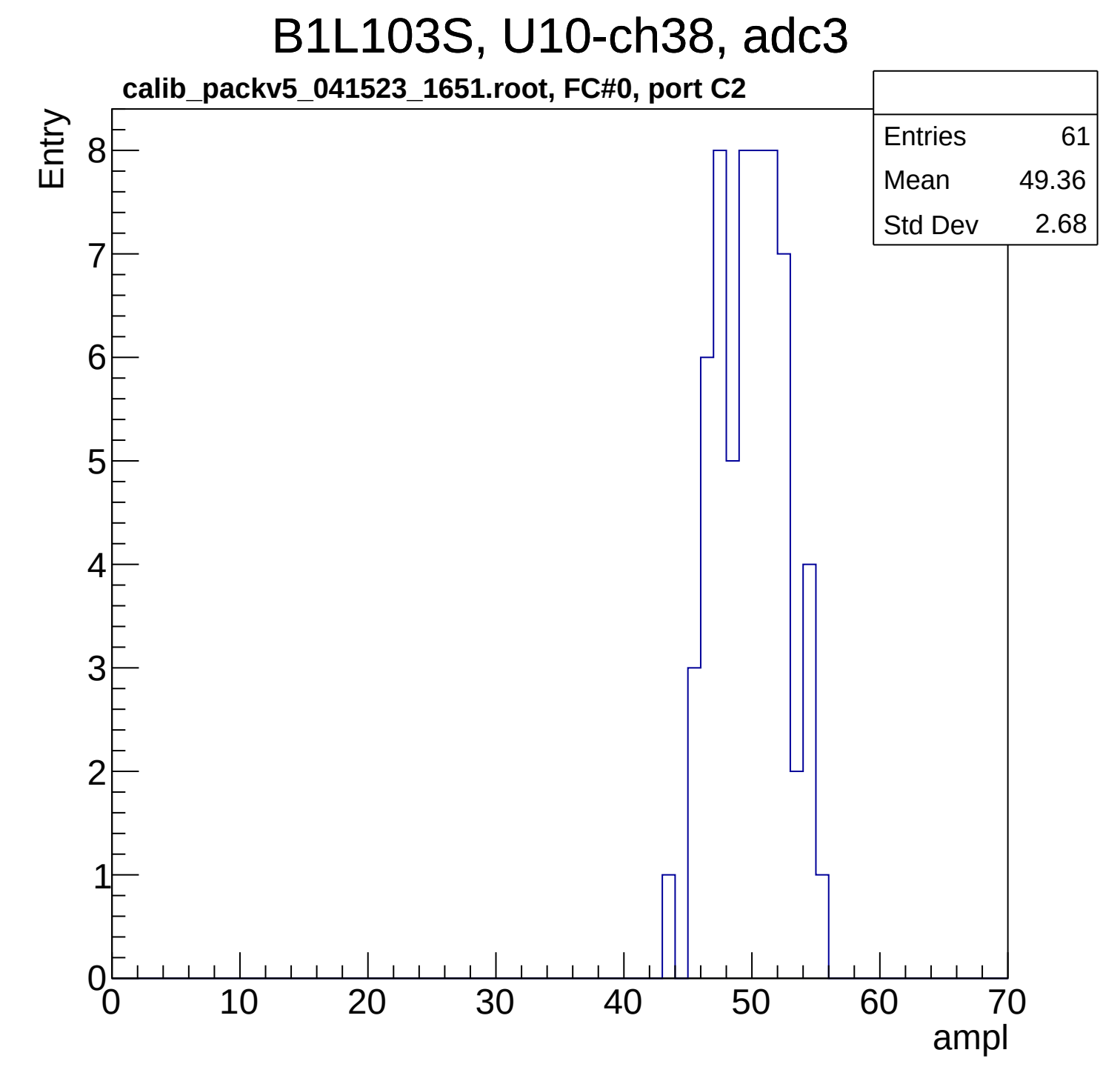
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U10-ch38, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 49.36
Std Dev 2.68
Entry
ampl
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2
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4
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6
7
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10
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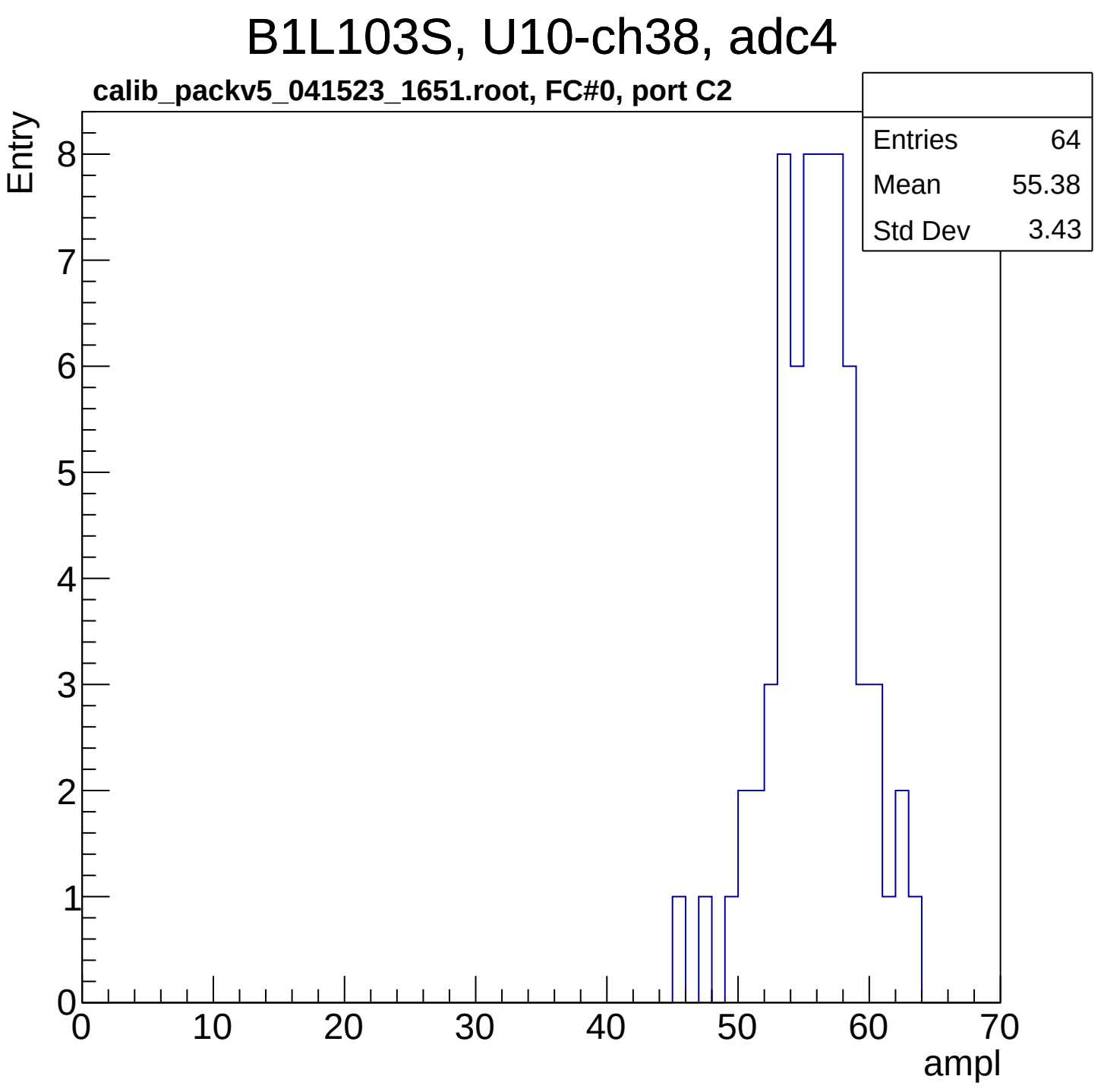
B1L103S, U10-ch38, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 55.38
Std Dev 3.43
Entry
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2
3
4
5
6
7
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10
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30
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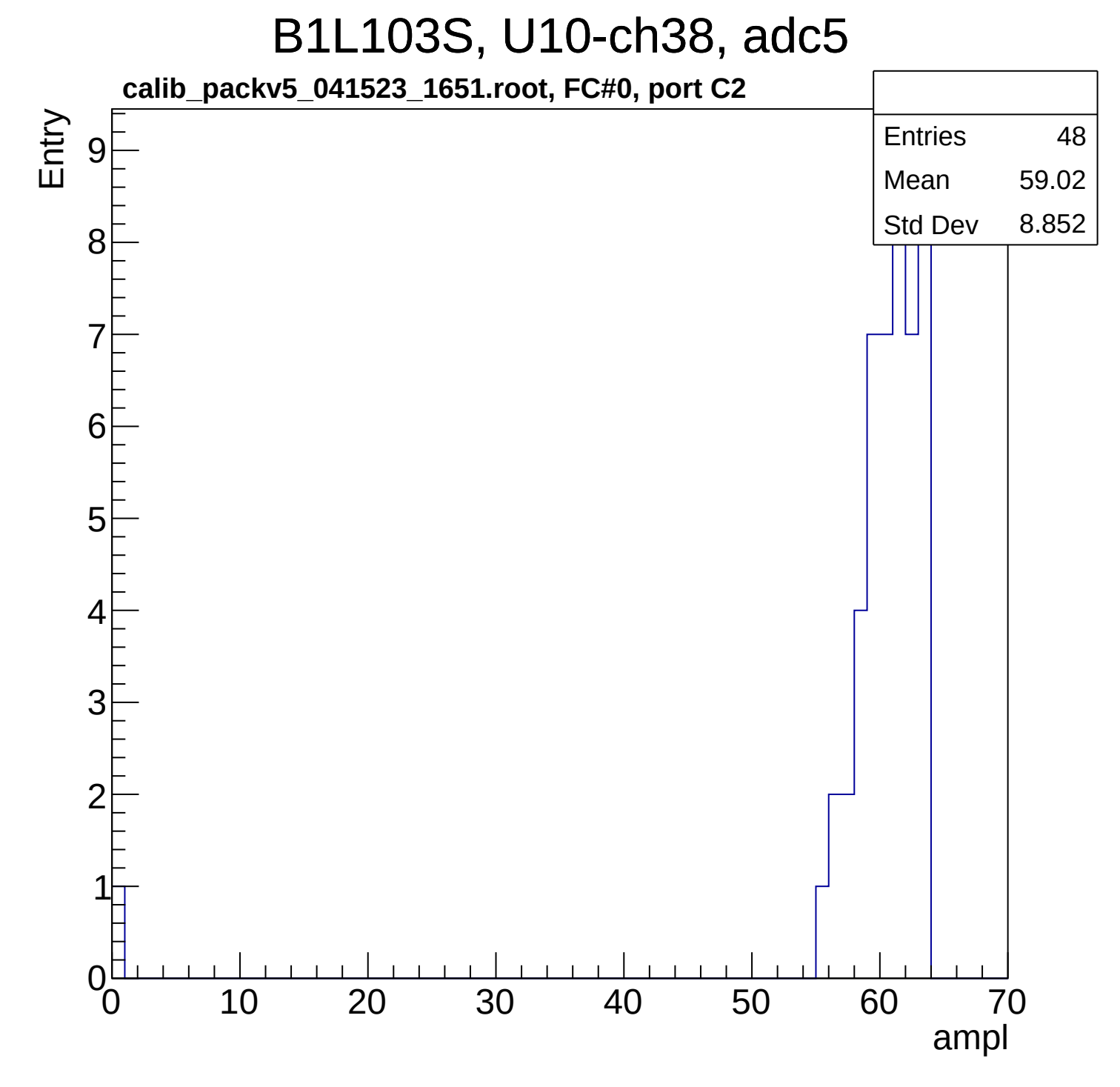
50
60
70


B1L103S, U10-ch38, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 59.02
Std Dev 8.852
Entry
ampl
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2
3
4
5
6
7
8
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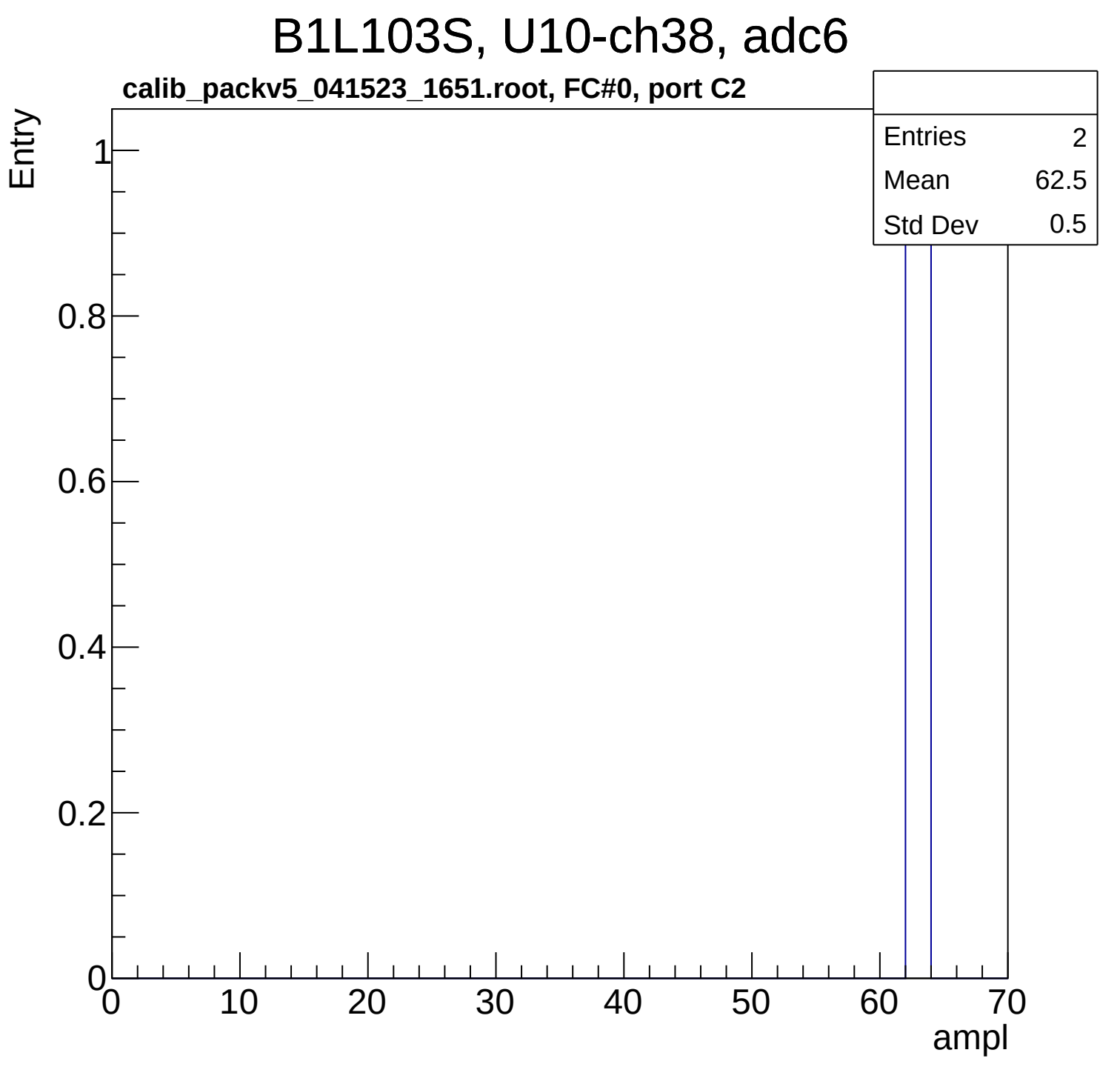
0
10
20
30
40
50
60
70


B1L103S, U10-ch38, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 2
Mean 62.5
Std Dev 0.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
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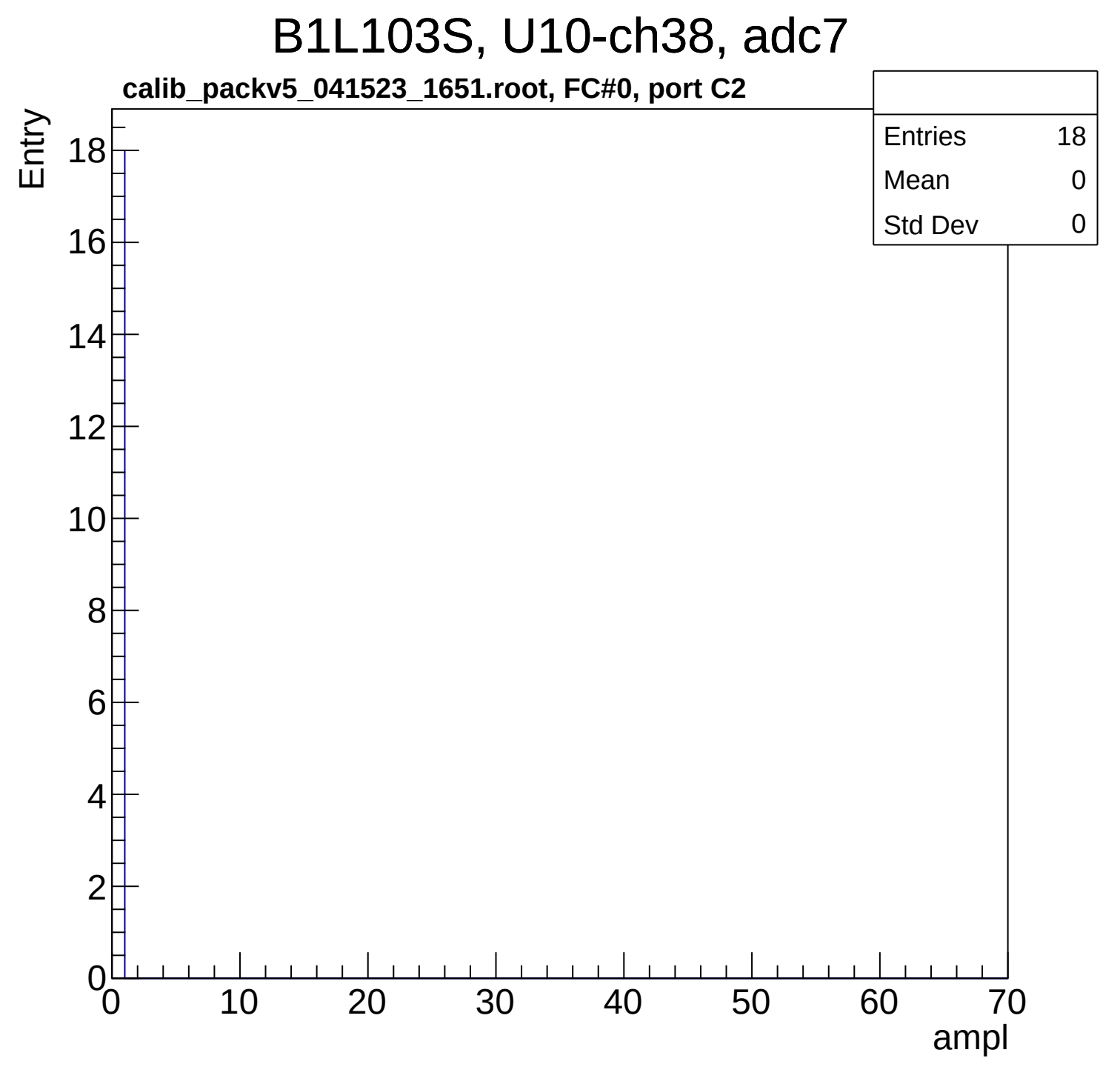
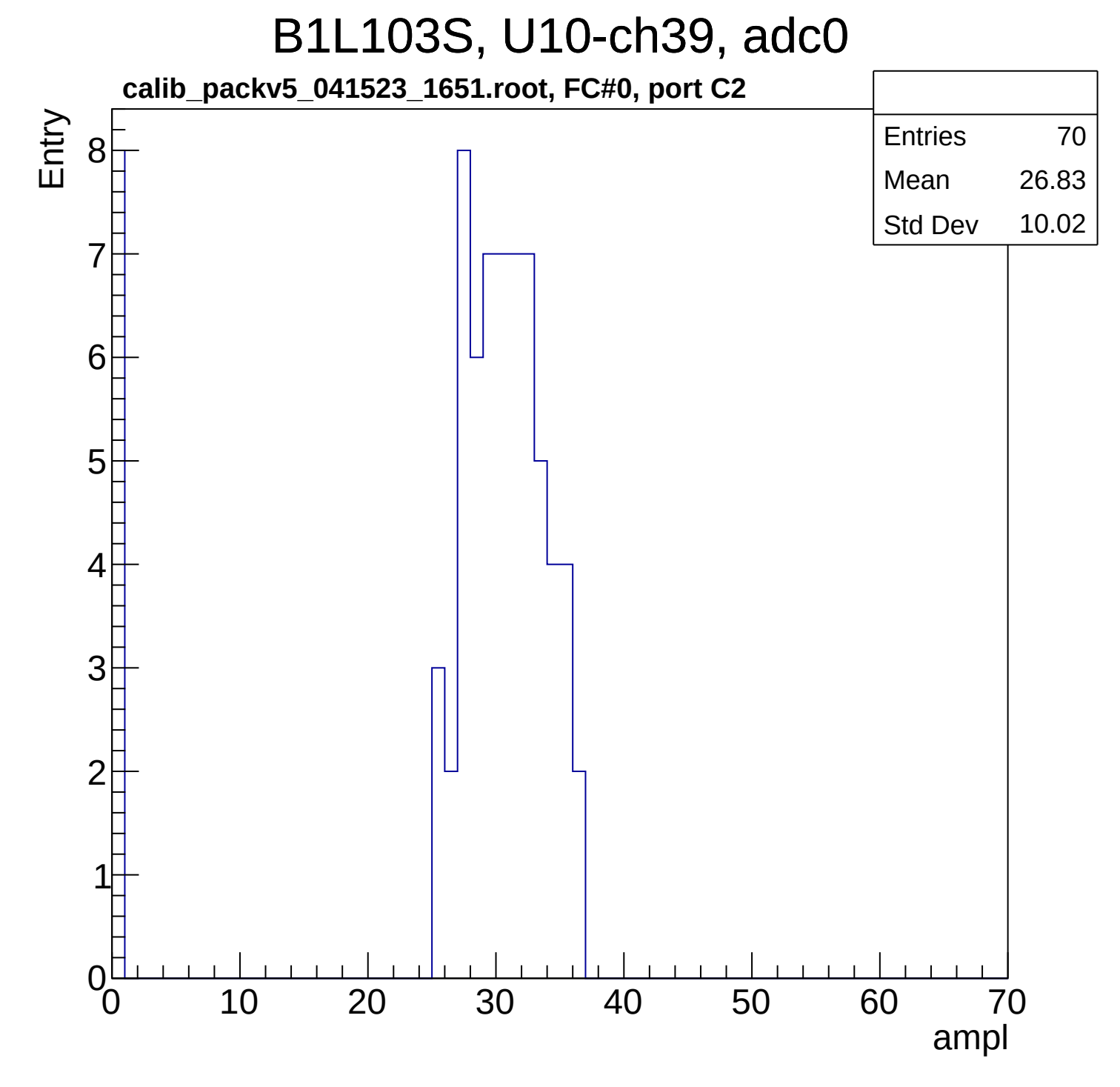
40
50
60
70
ampl


B1L103S, U10-ch38, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch39, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 26.83
Std Dev 10.02
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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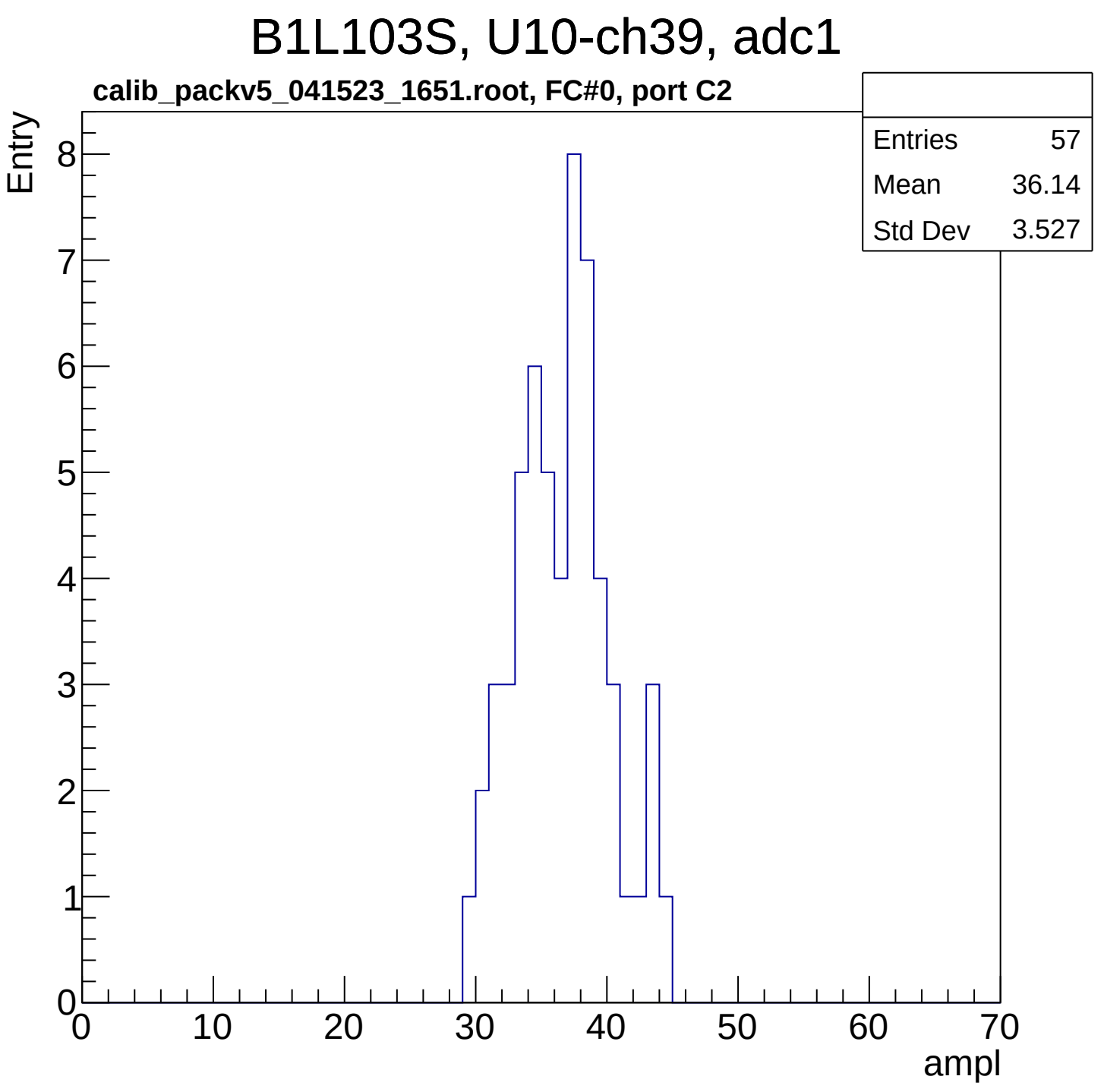
B1L103S, U10-ch39, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 36.14
Std Dev 3.527
Entry
ampl
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1
2
3
4
5
6
7
8
0
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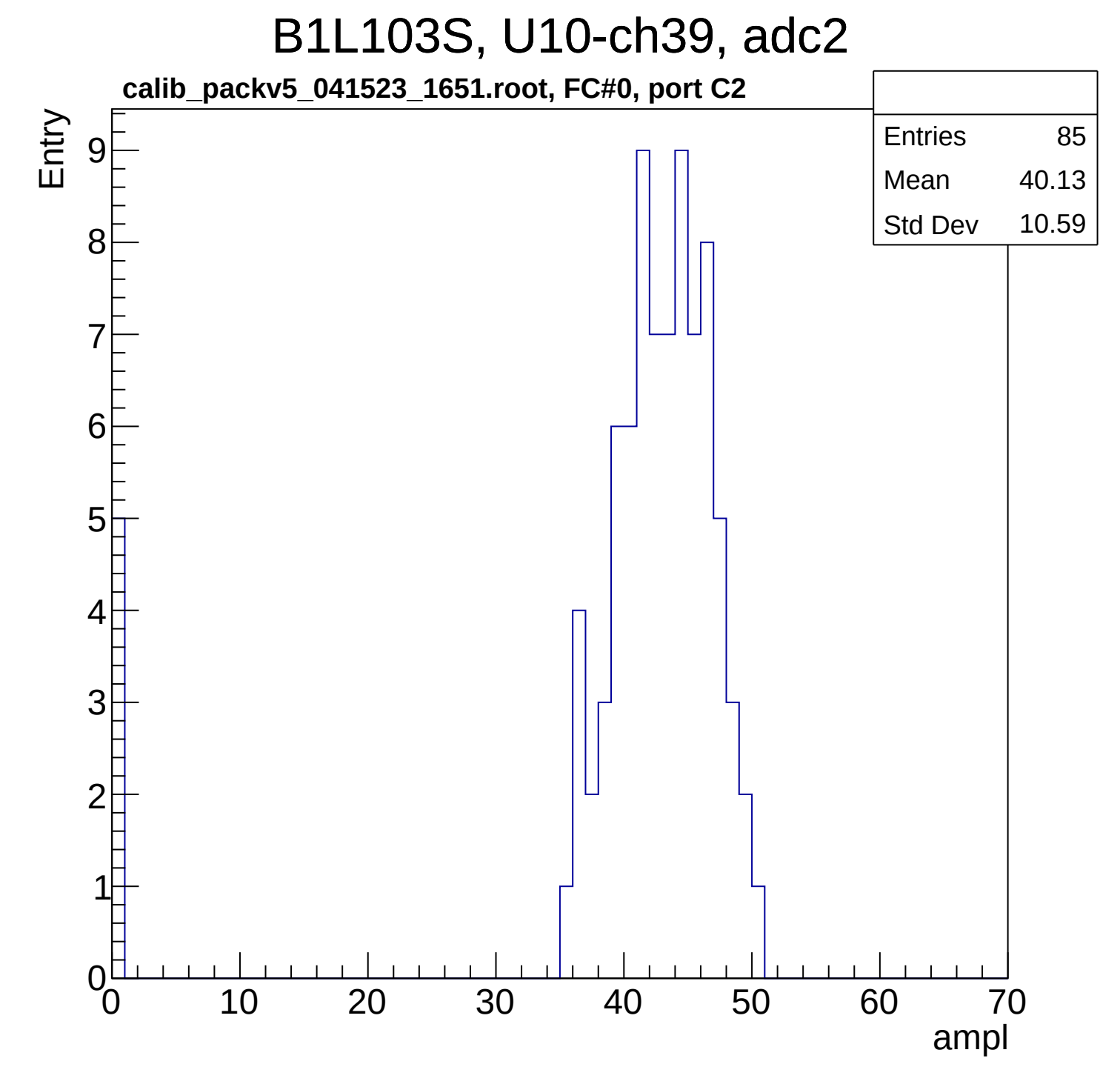
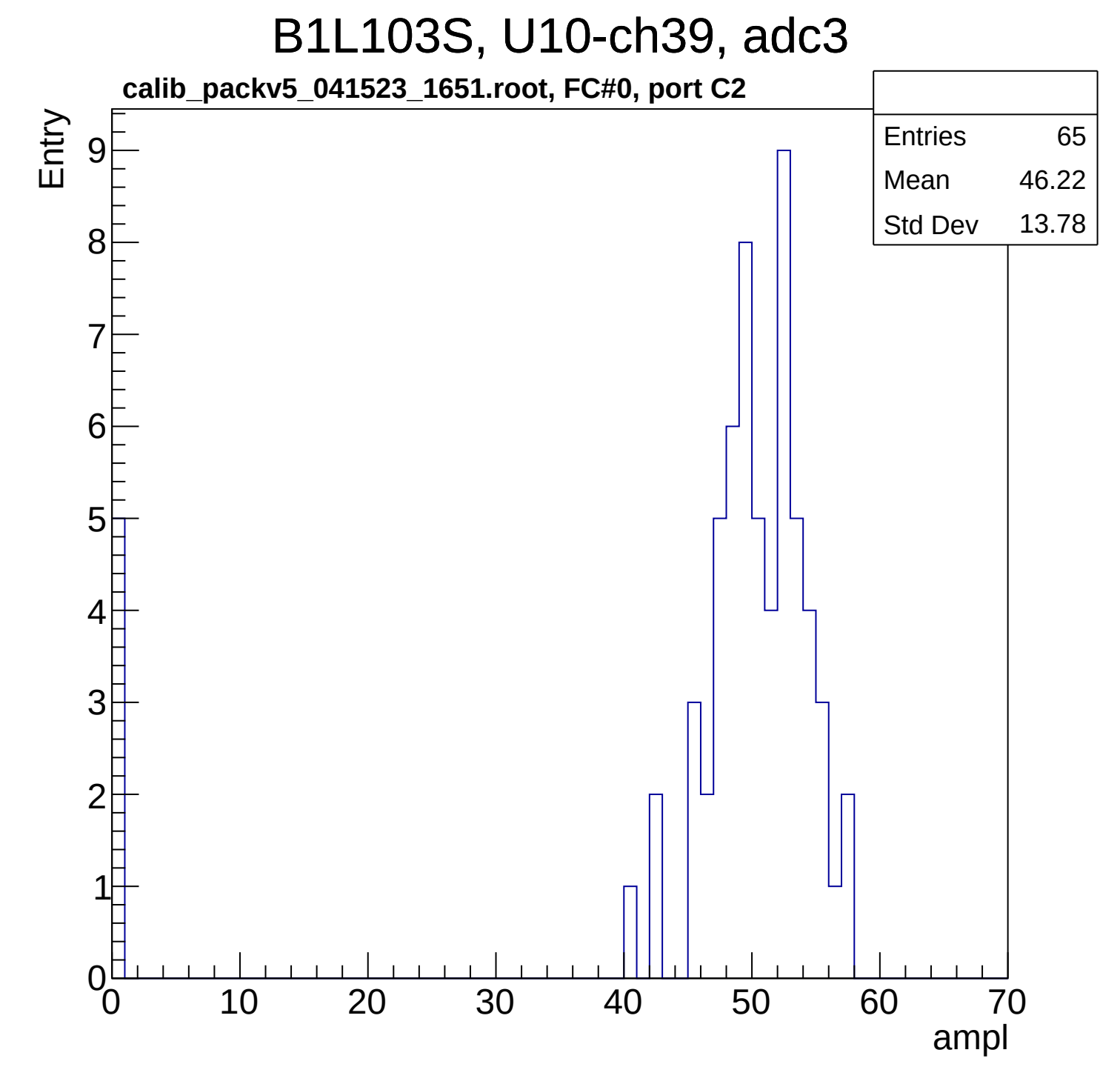
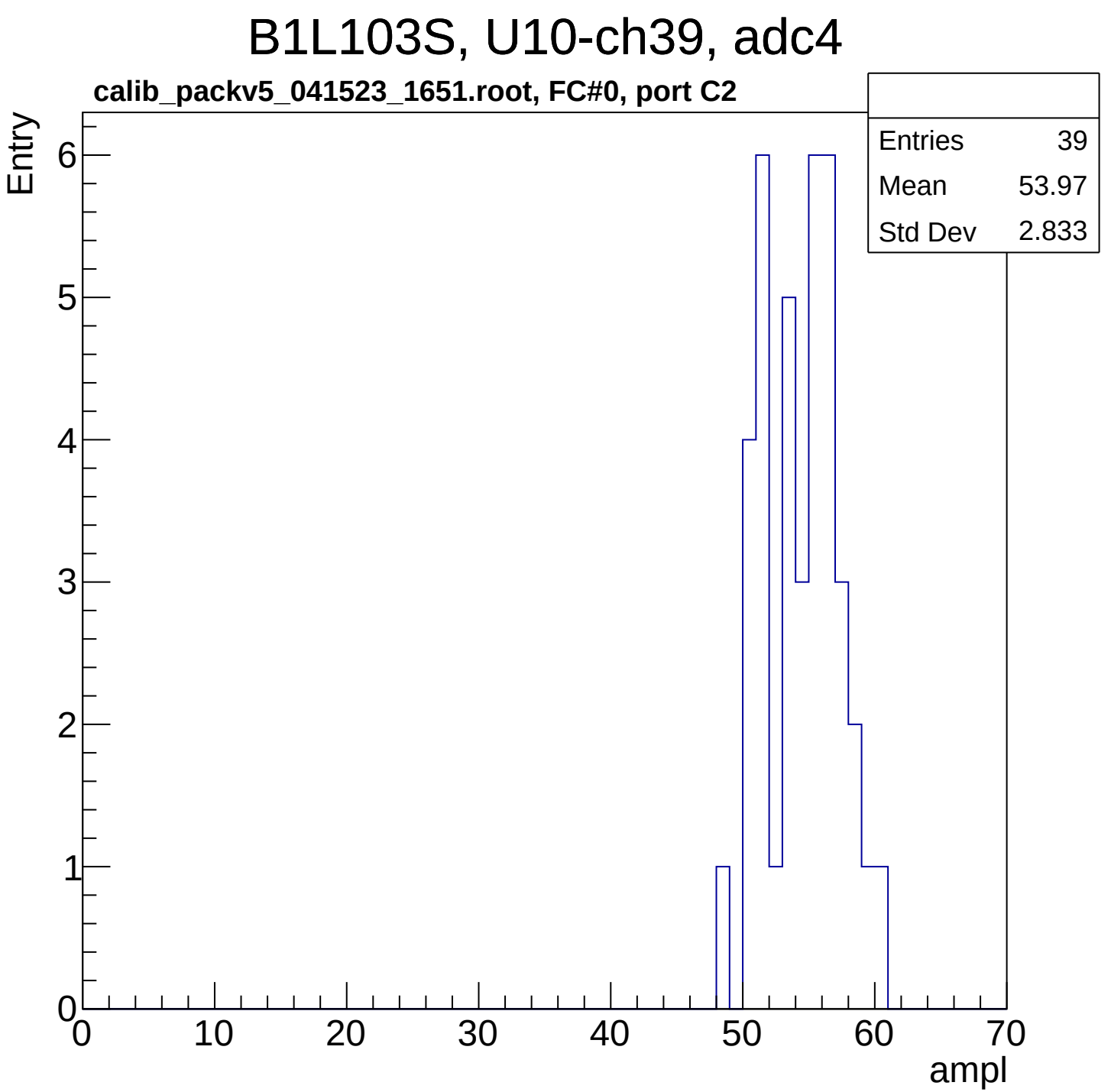
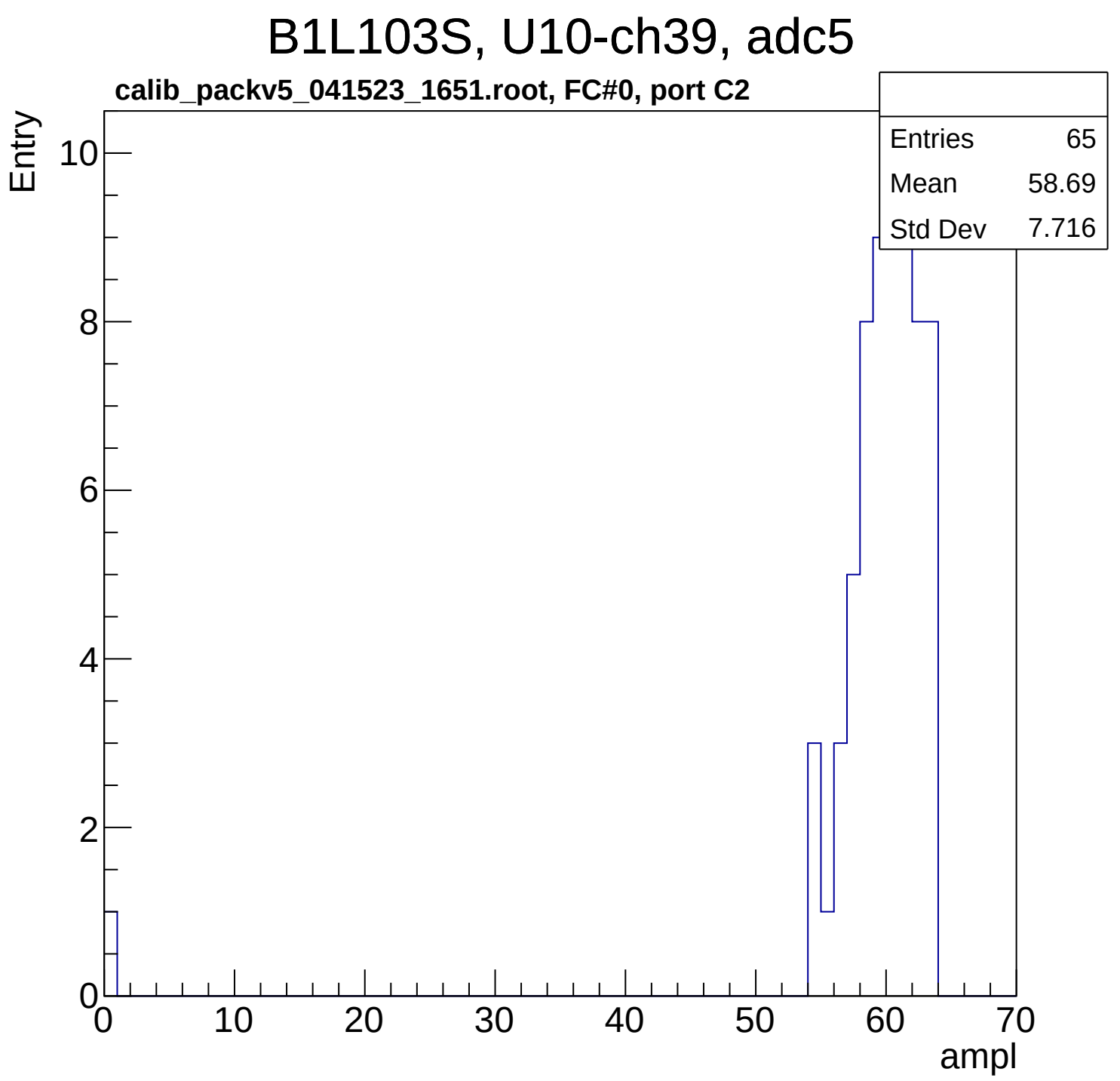
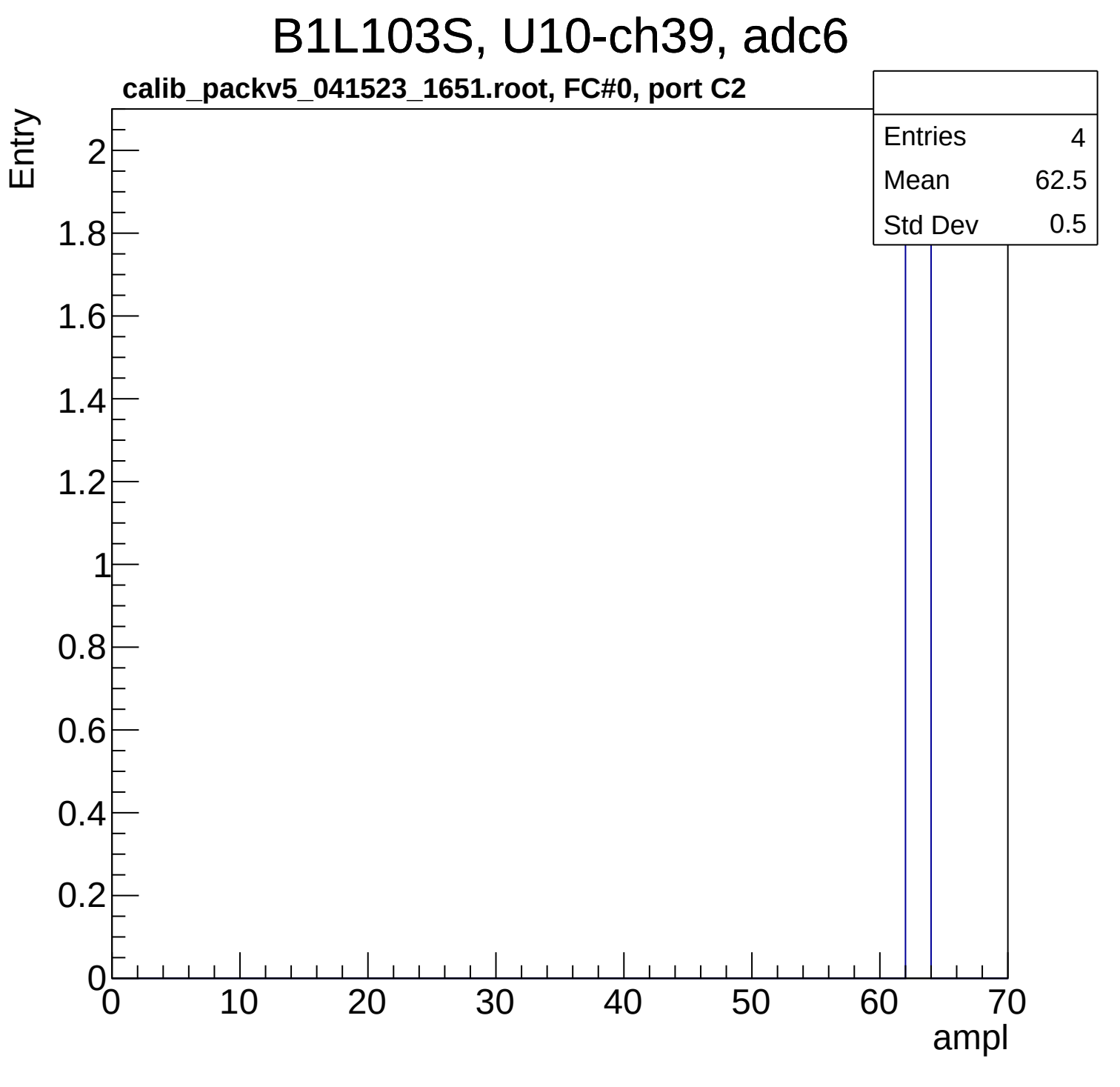
40
50
60
70

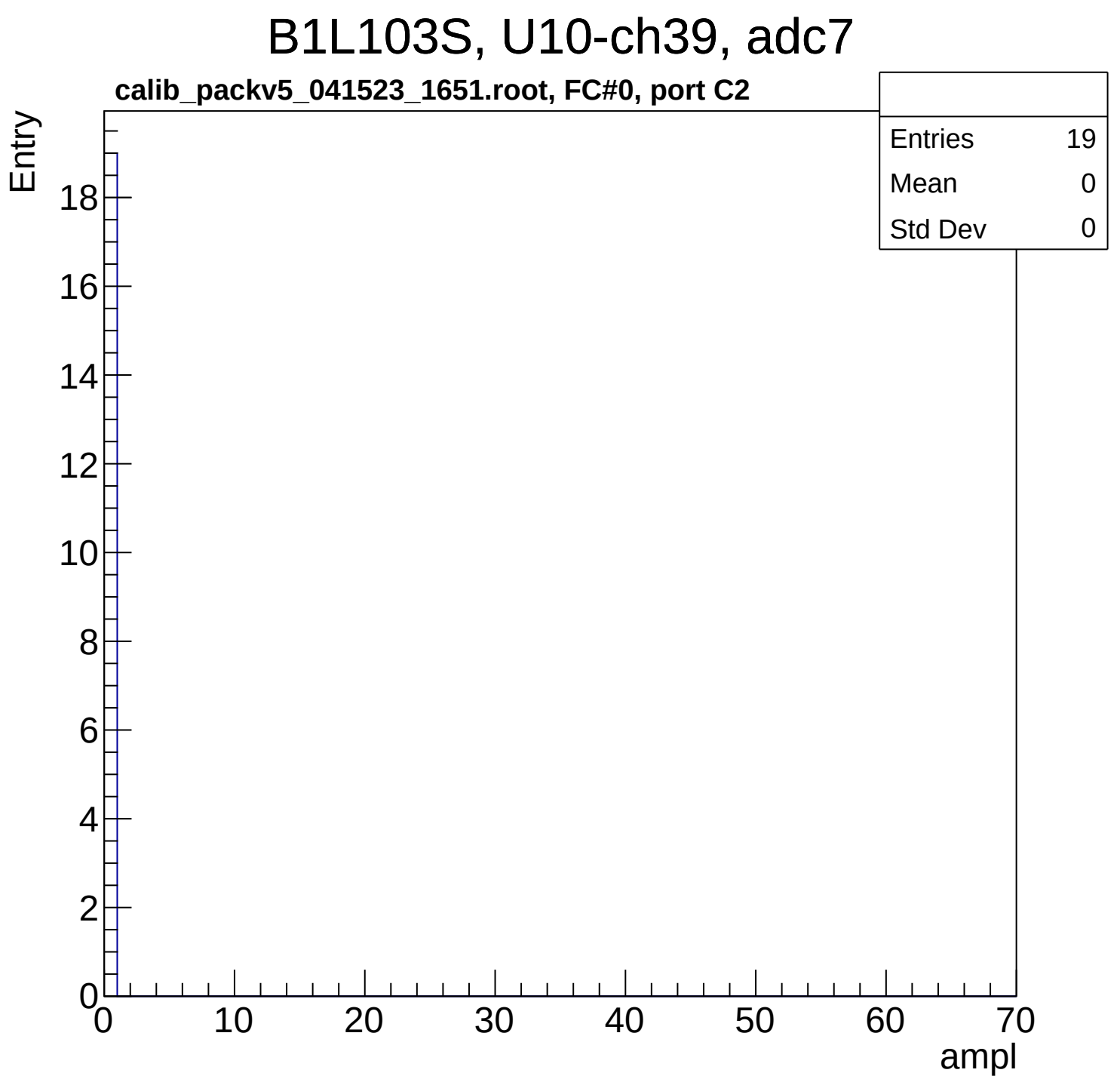

B1L103S, U10-ch39, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 40.13
Std Dev 10.59
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

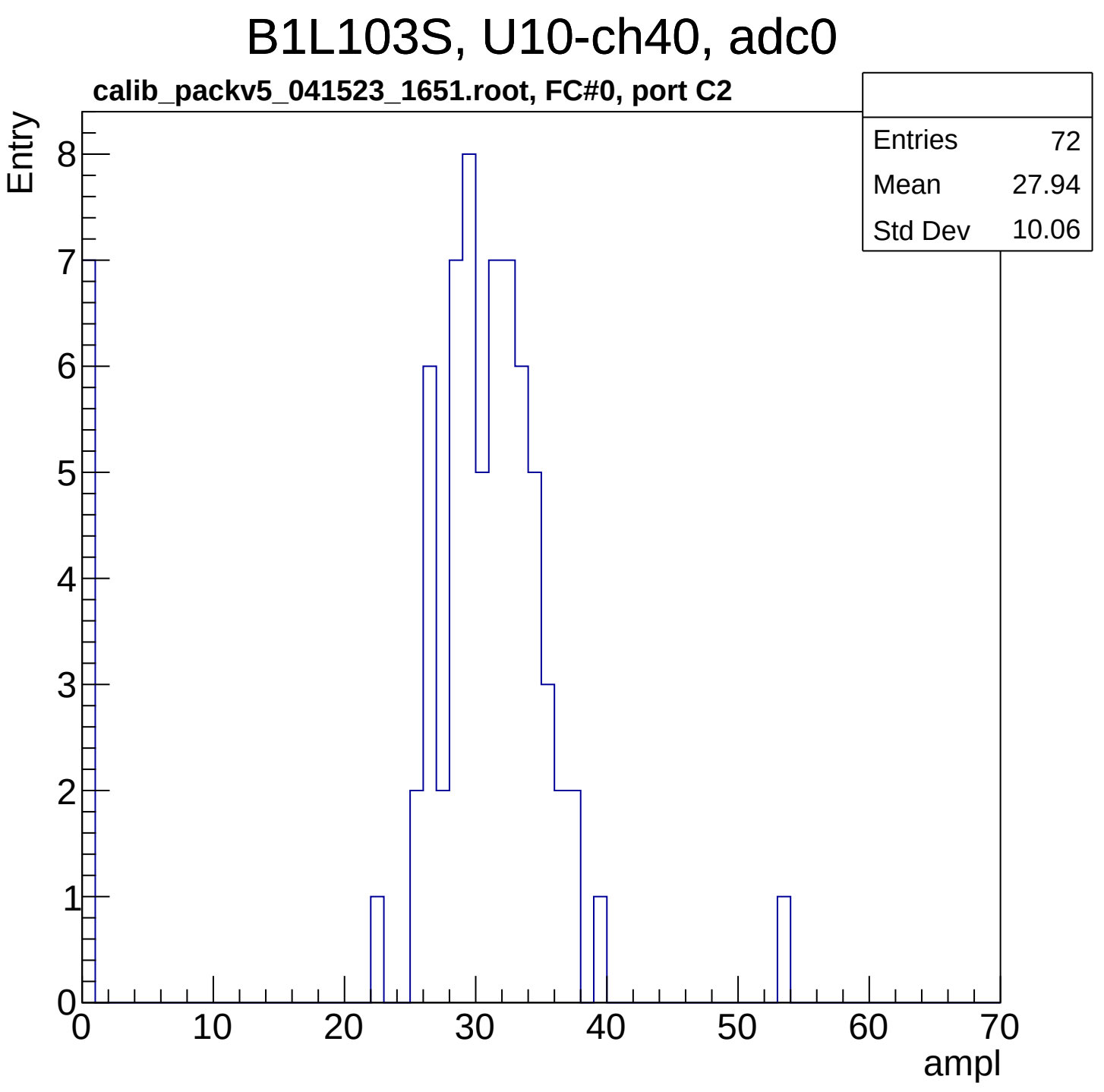

B1L103S, U10-ch39, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 46.22
Std Dev 13.78
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

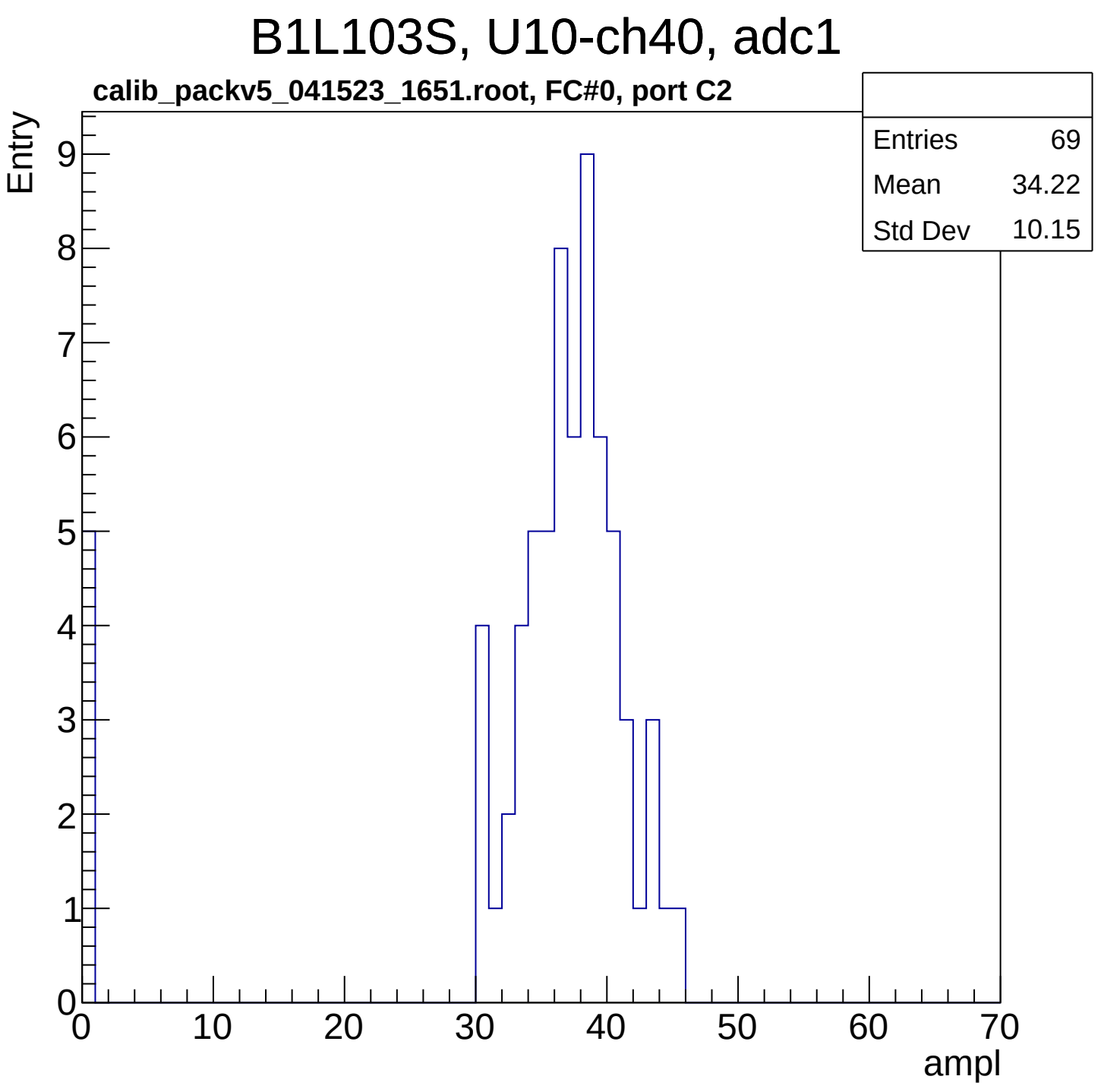

B1L103S, U10-ch39, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 39
Mean 53.97
Std Dev 2.833
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl

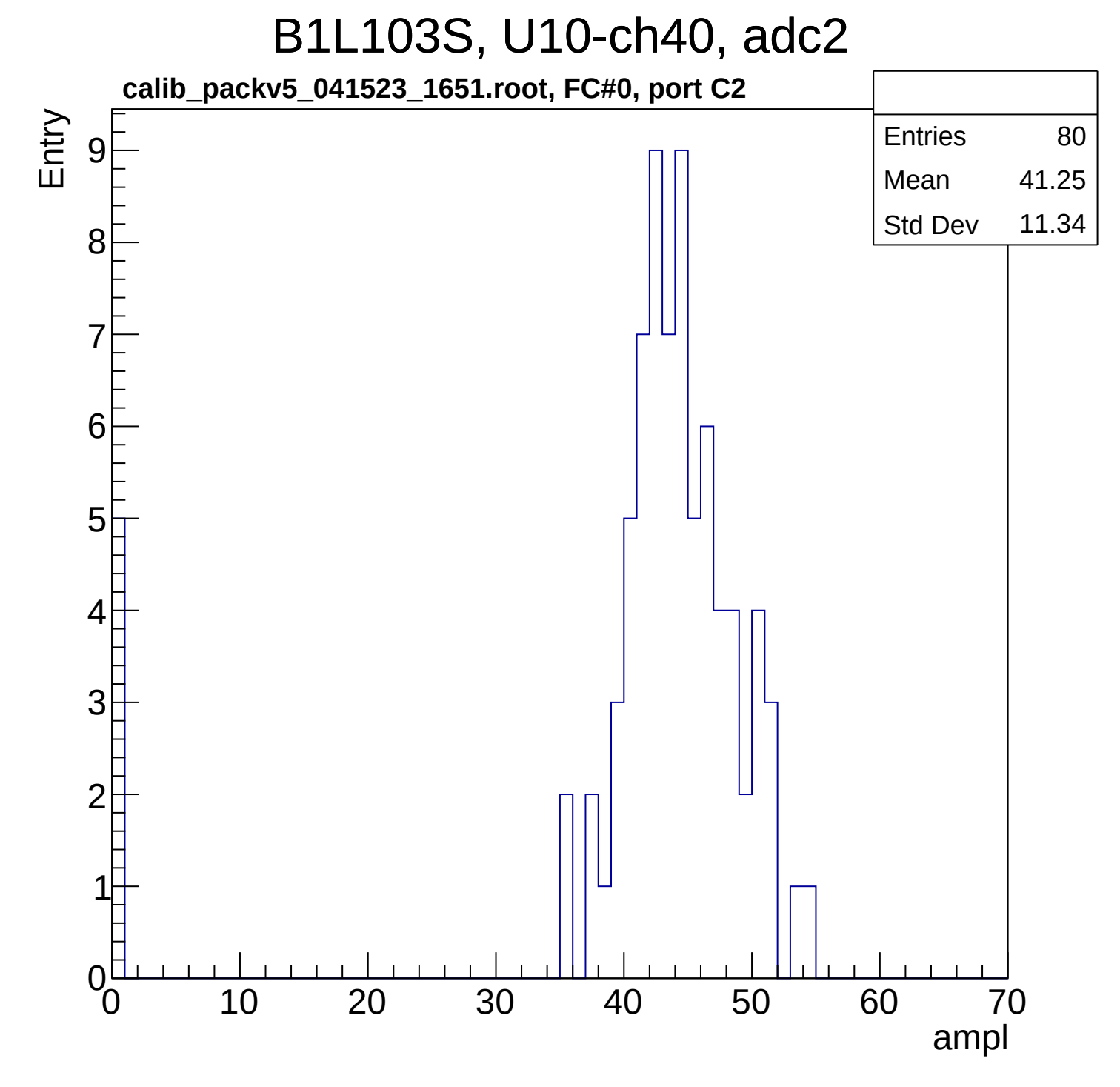

B1L103S, U10-ch39, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 58.69
Std Dev 7.716
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

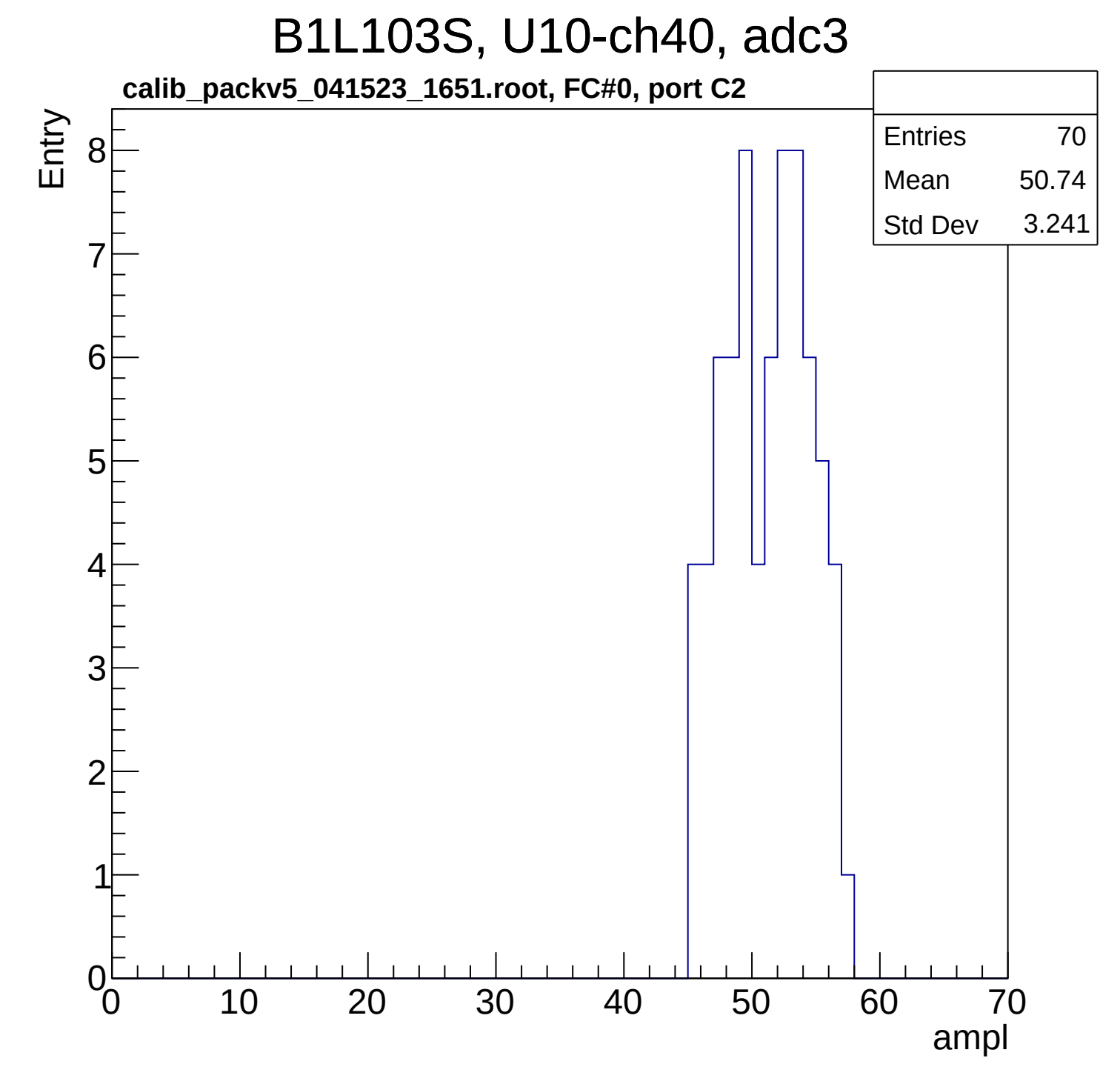

B1L103S, U10-ch39, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 4
Mean 62.5
Std Dev 0.5
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

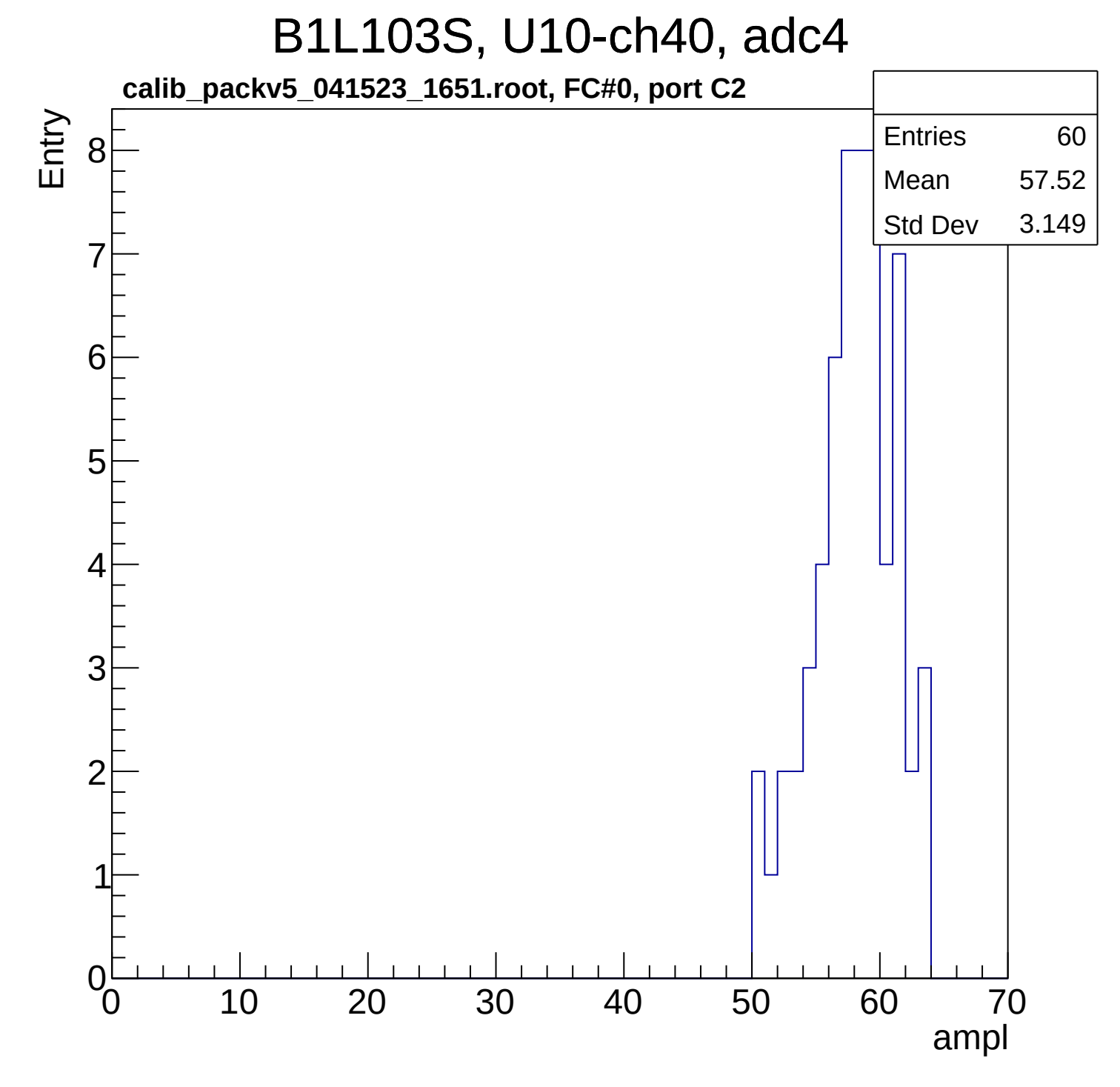

B1L103S, U10-ch39, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

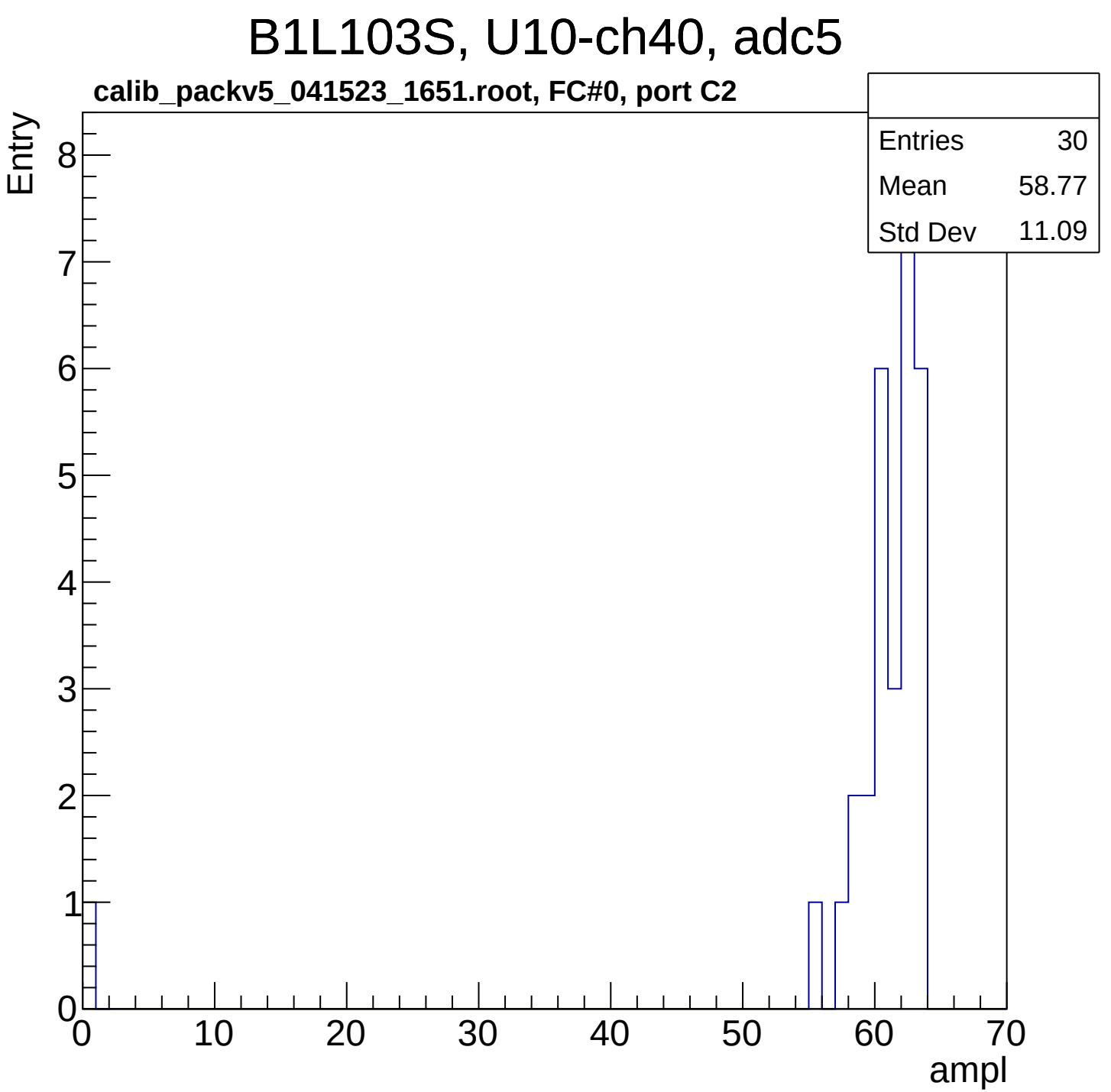

B1L103S, U10-ch40, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 27.94
Std Dev 10.06
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

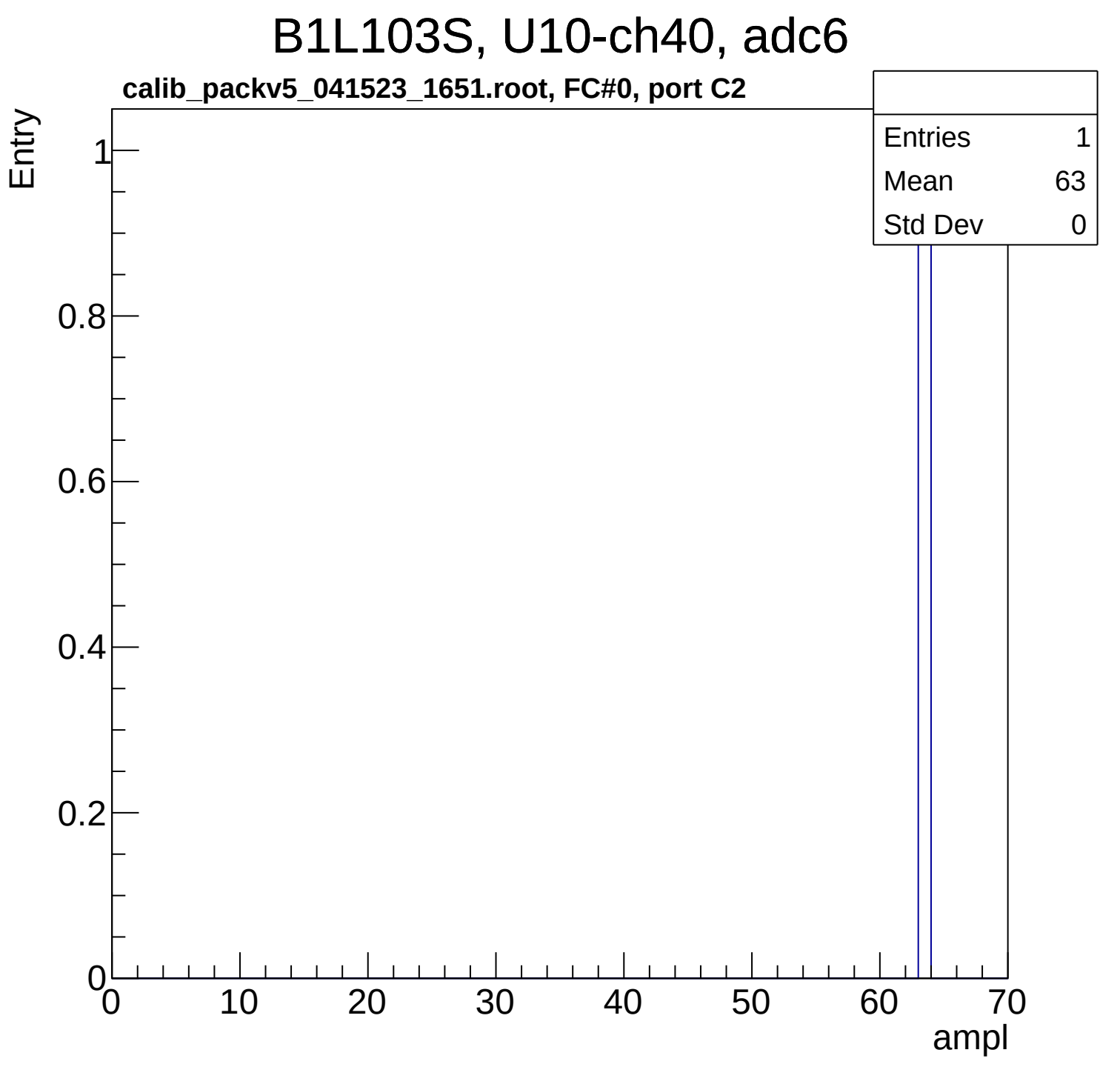

B1L103S, U10-ch40, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 34.22
Std Dev 10.15
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

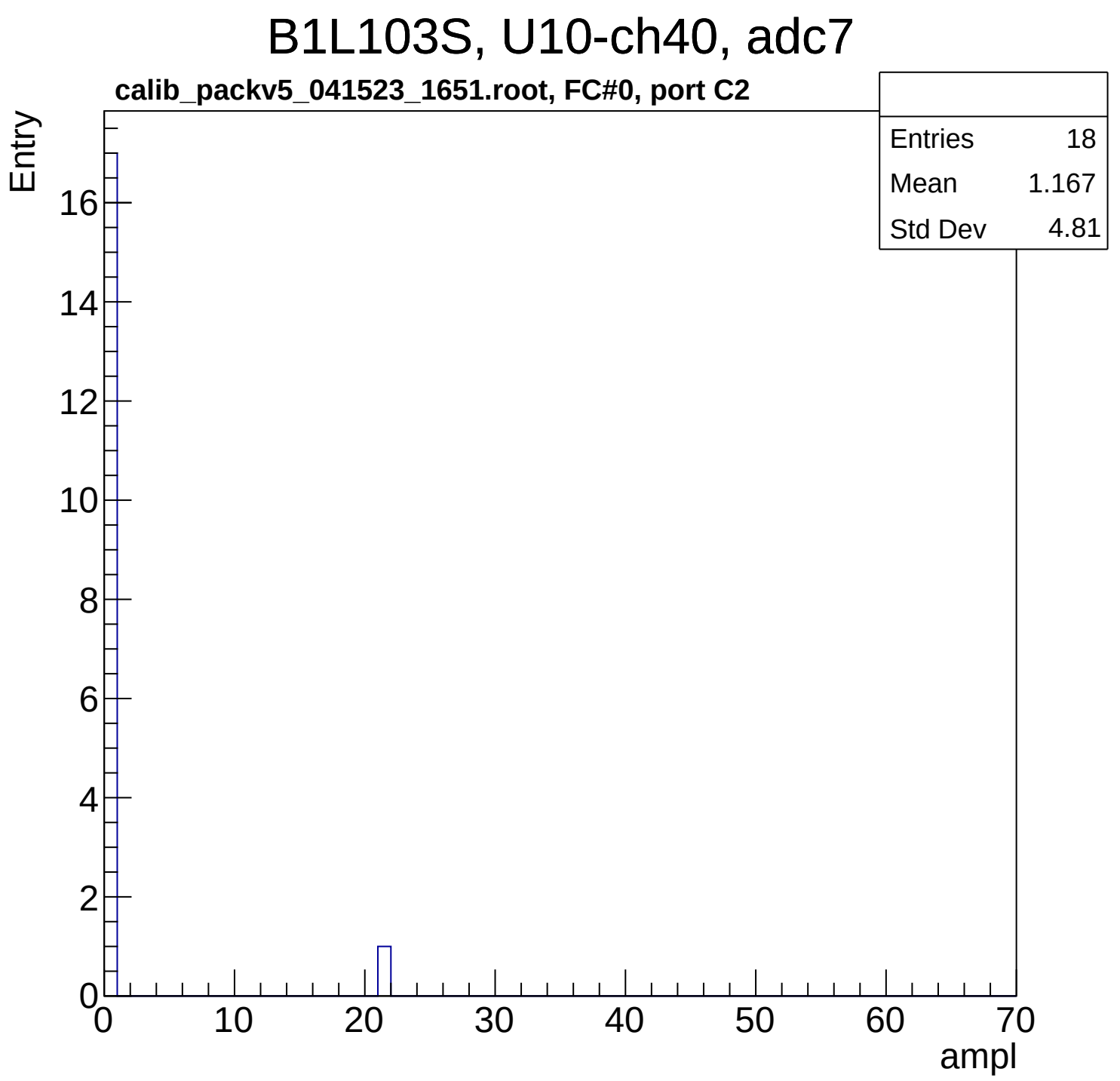

B1L103S, U10-ch40, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 41.25
Std Dev 11.34
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

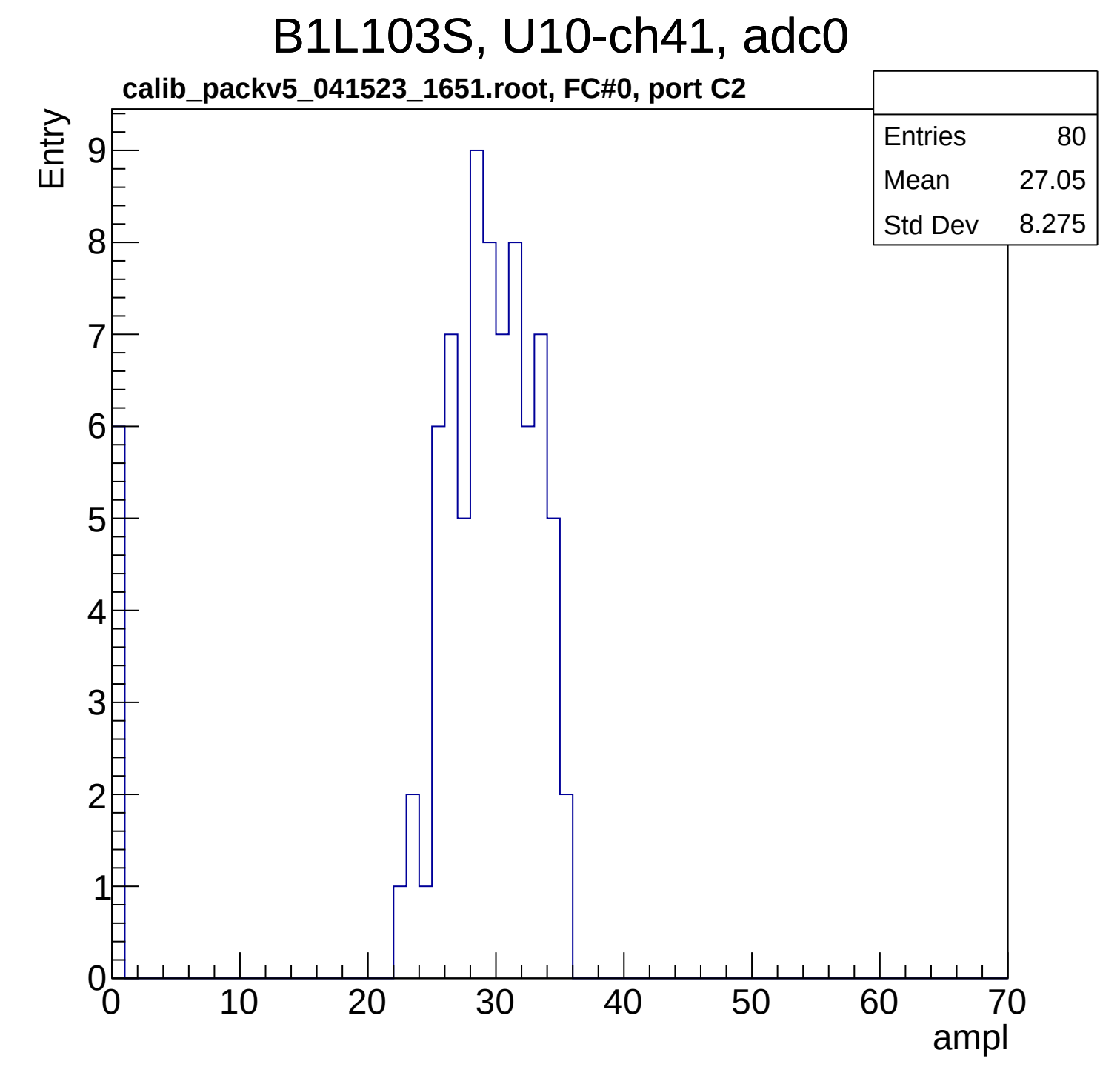

B1L103S, U10-ch40, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 50.74
Std Dev 3.241
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

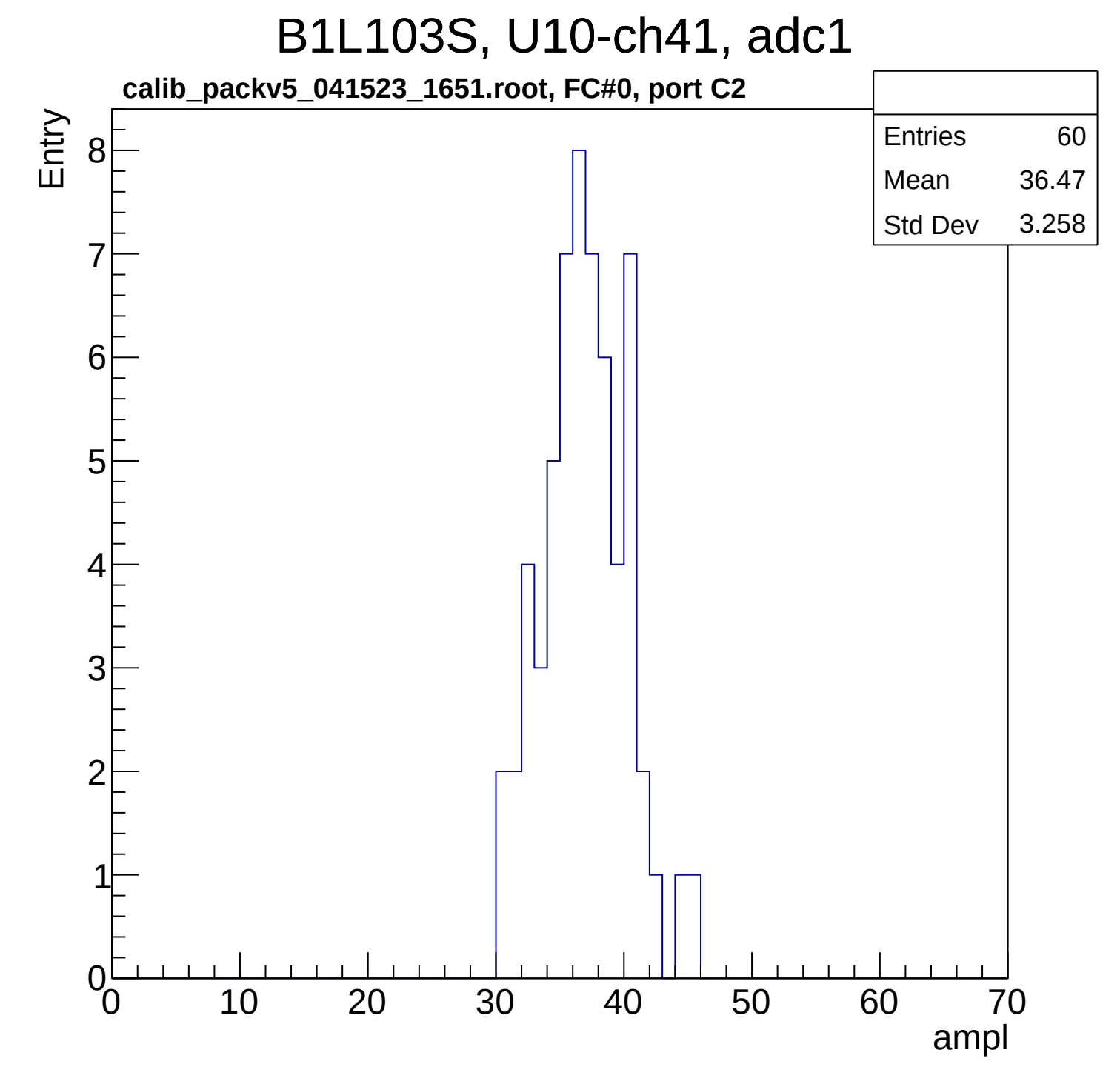

B1L103S, U10-ch40, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 57.52
Std Dev 3.149
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U10-ch40, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 30
Mean 58.77
Std Dev 11.09
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U10-ch40, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 1
Mean 63
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch40, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 1.167
Std Dev 4.81
Entry
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch41, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 27.05
Std Dev 8.275
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U10-ch41, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 36.47
Std Dev 3.258
Entry
ampl
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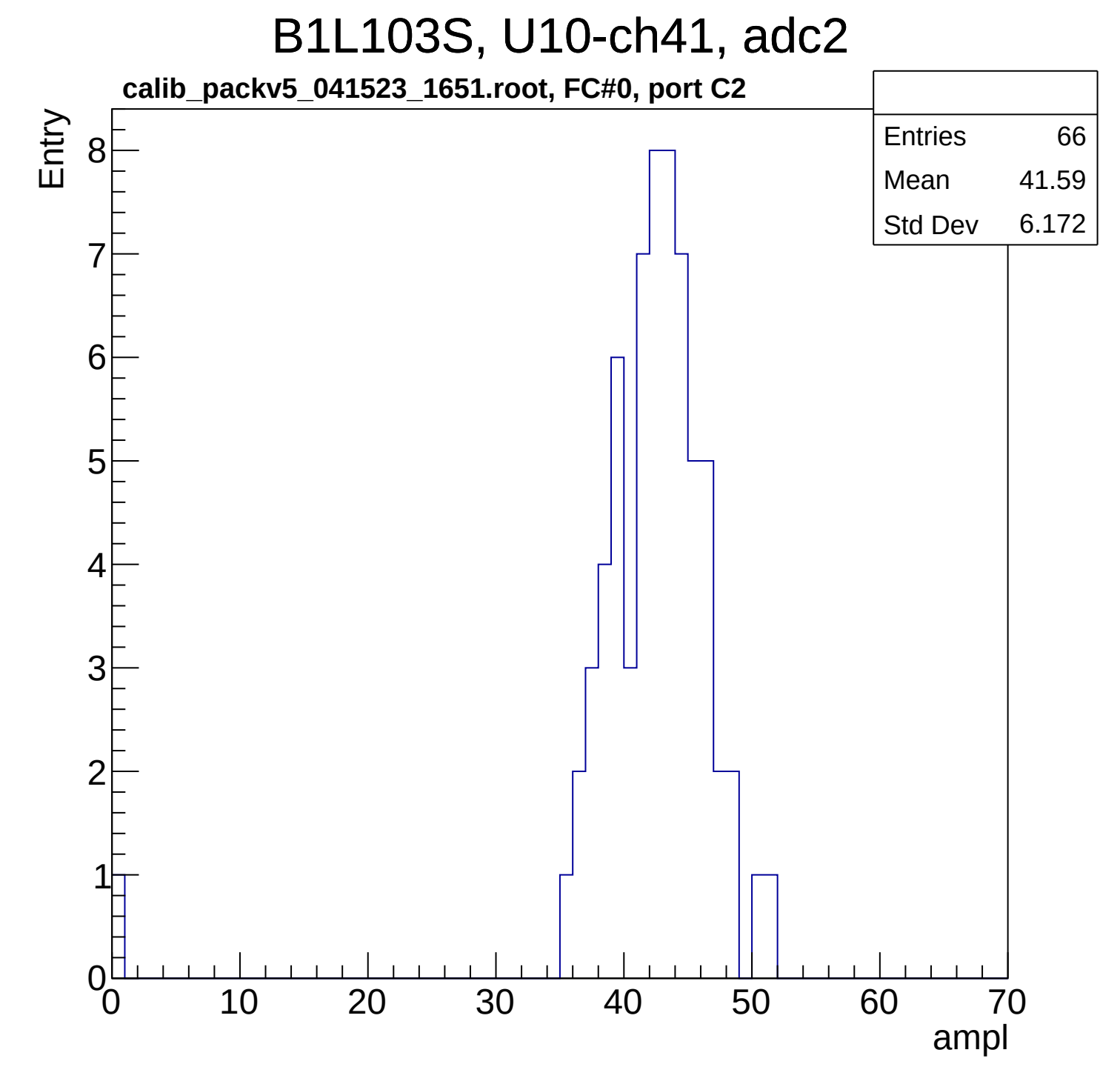
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U10-ch41, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 41.59
Std Dev 6.172
Entry
ampl
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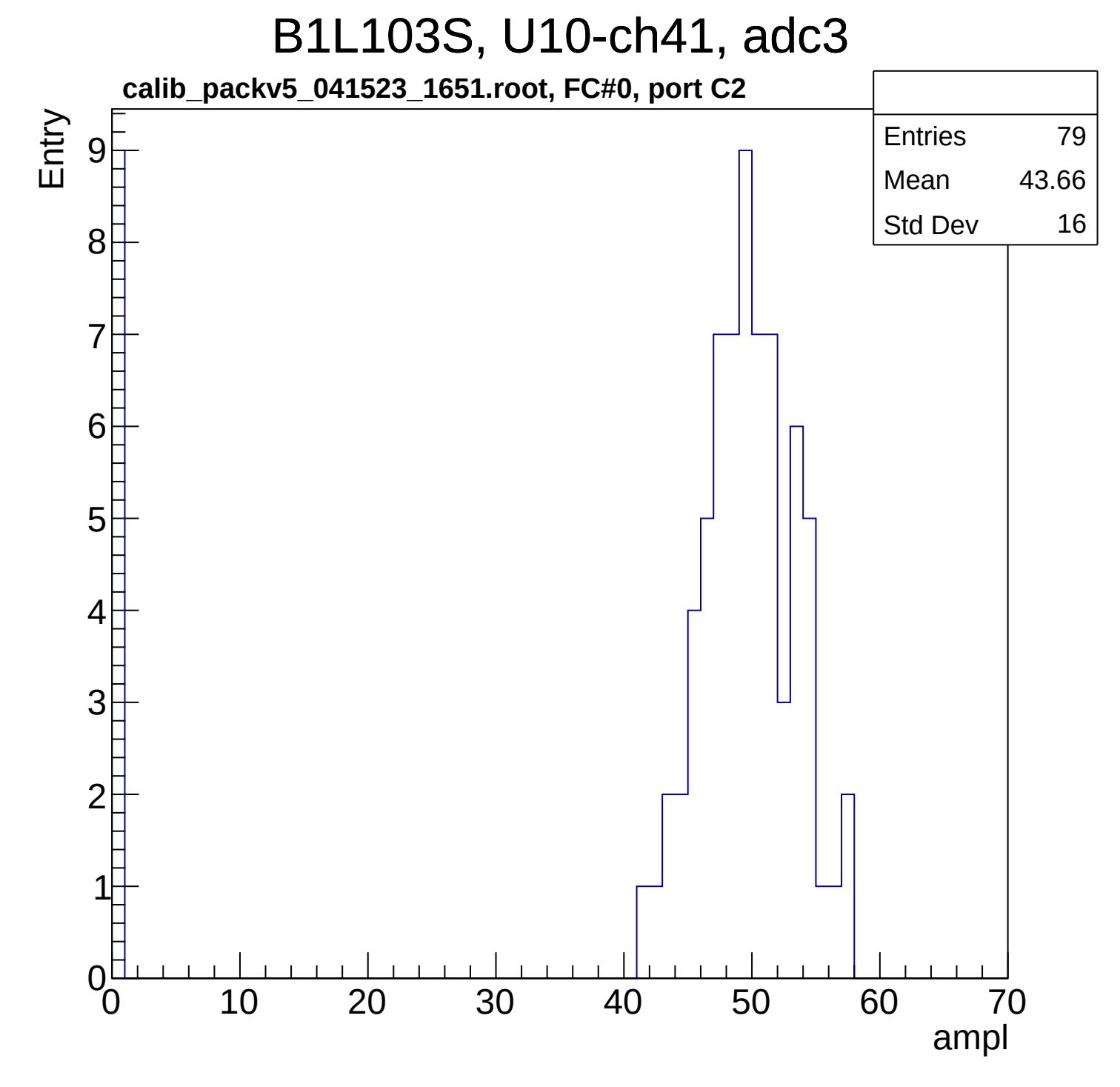
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U10-ch41, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 43.66
Std Dev 16
Entry
ampl
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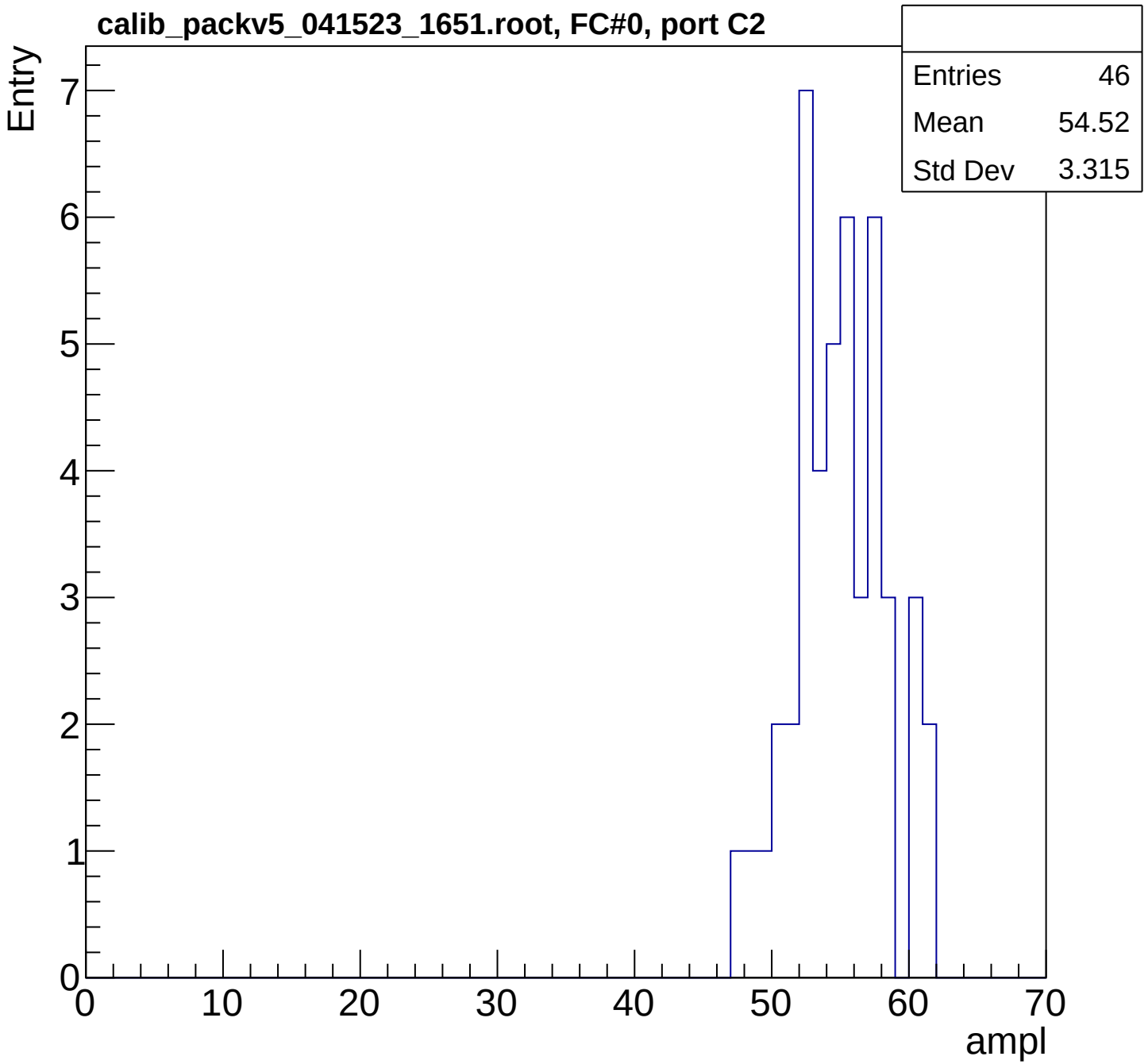
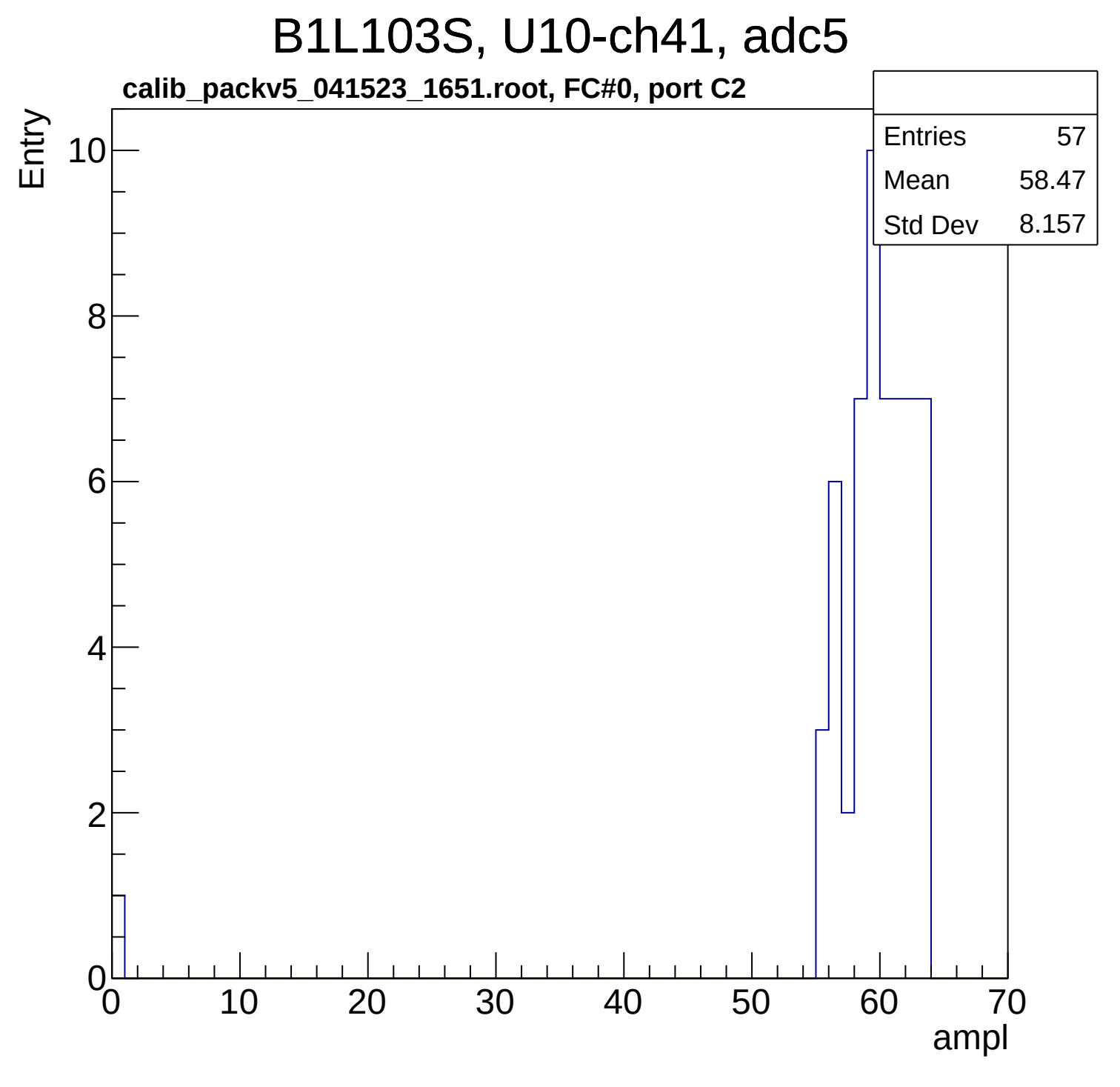
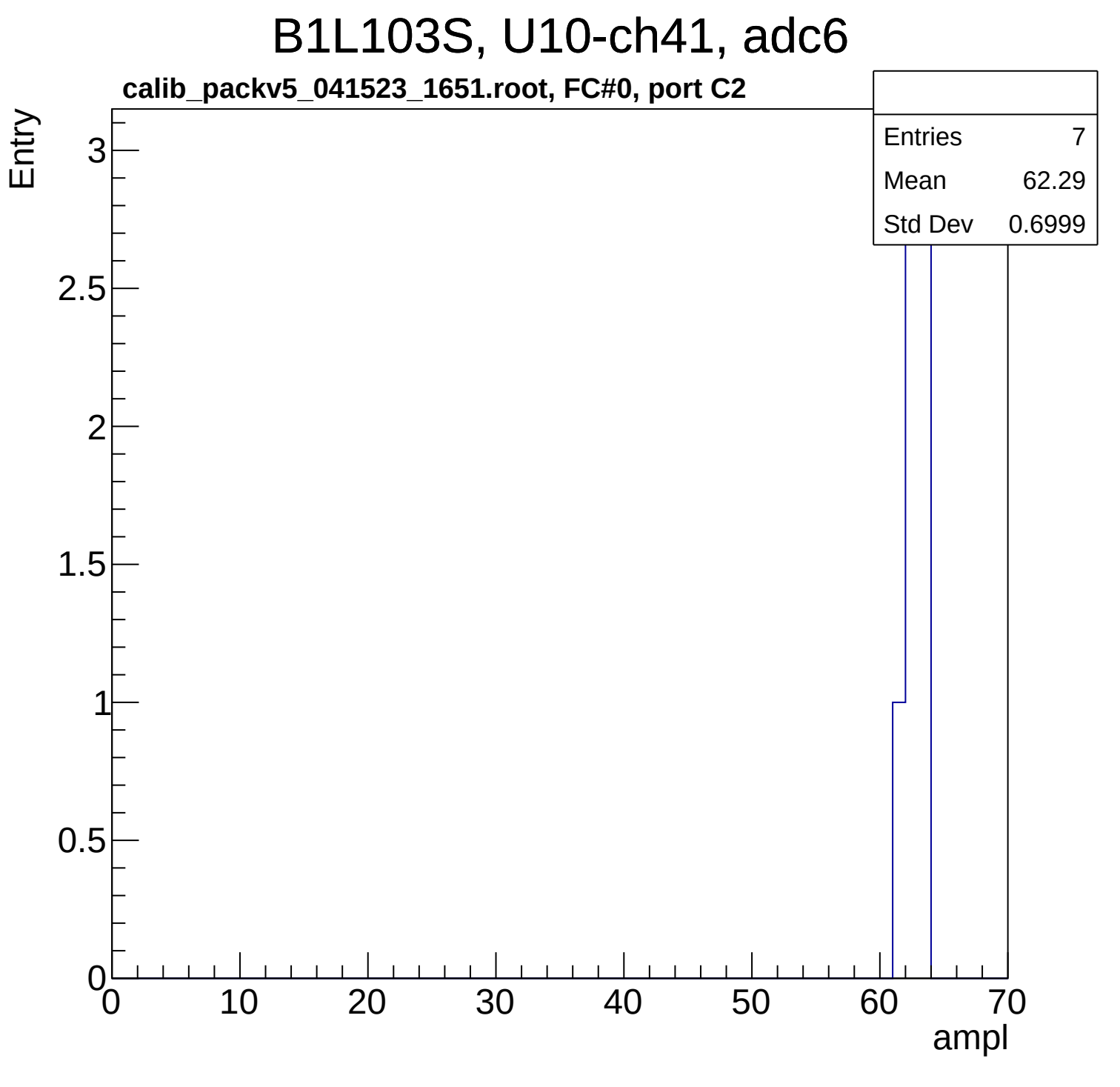
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U10-ch41, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 54.52
Std Dev 3.315
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U10-ch41, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 58.47
Std Dev 8.157
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U10-ch41, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 62.29
Std Dev 0.6999
Entry
ampl
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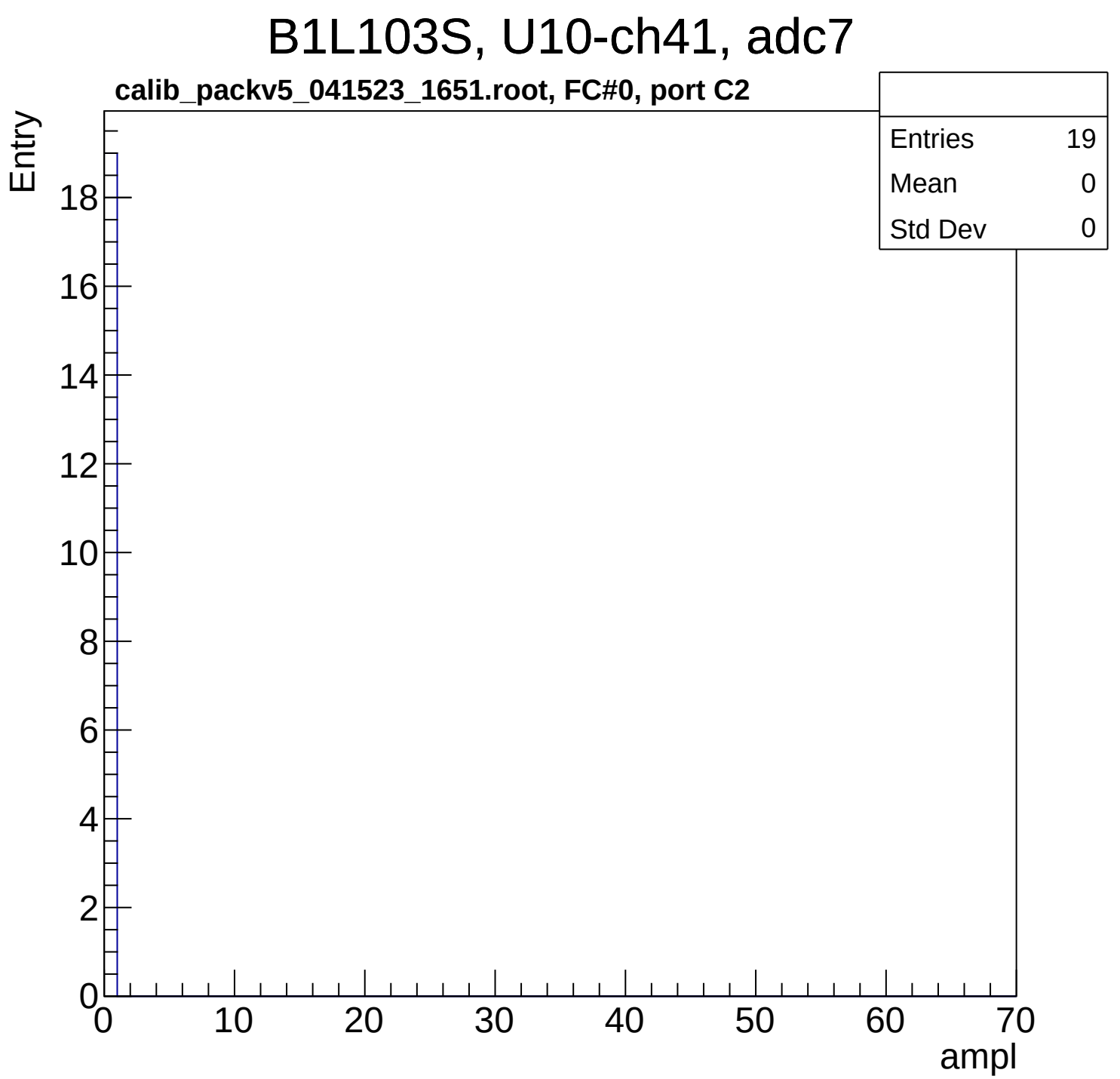
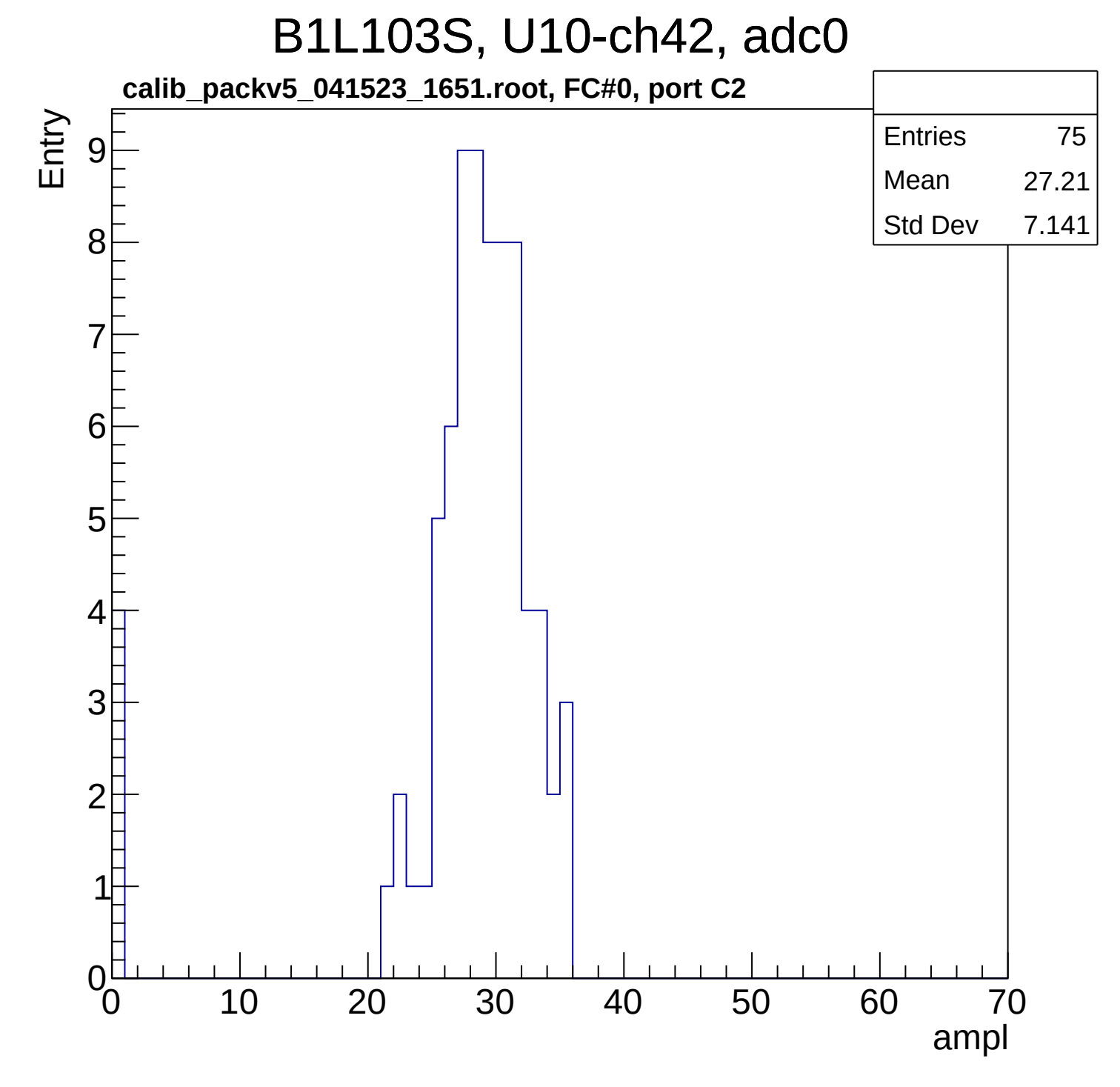
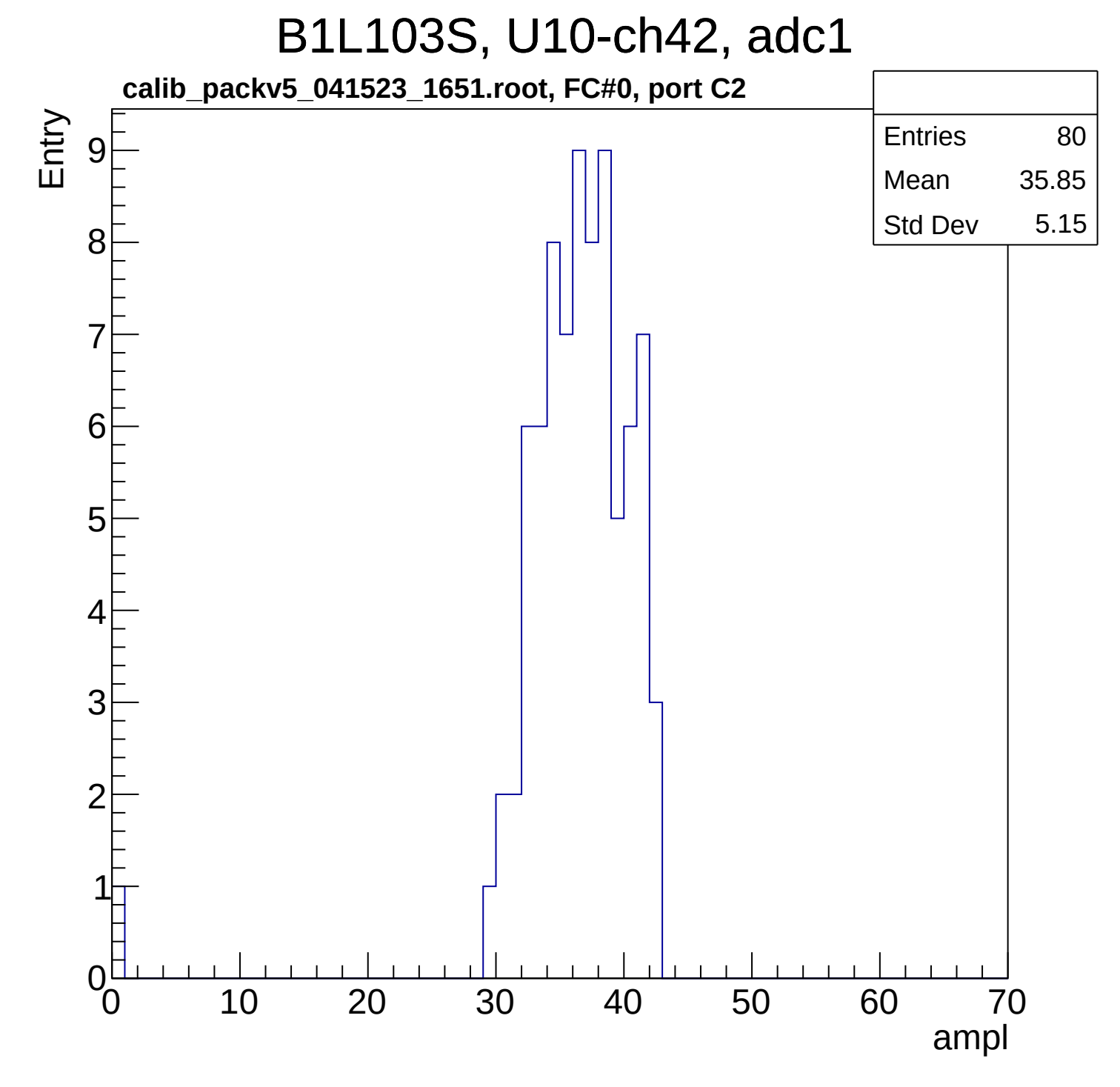
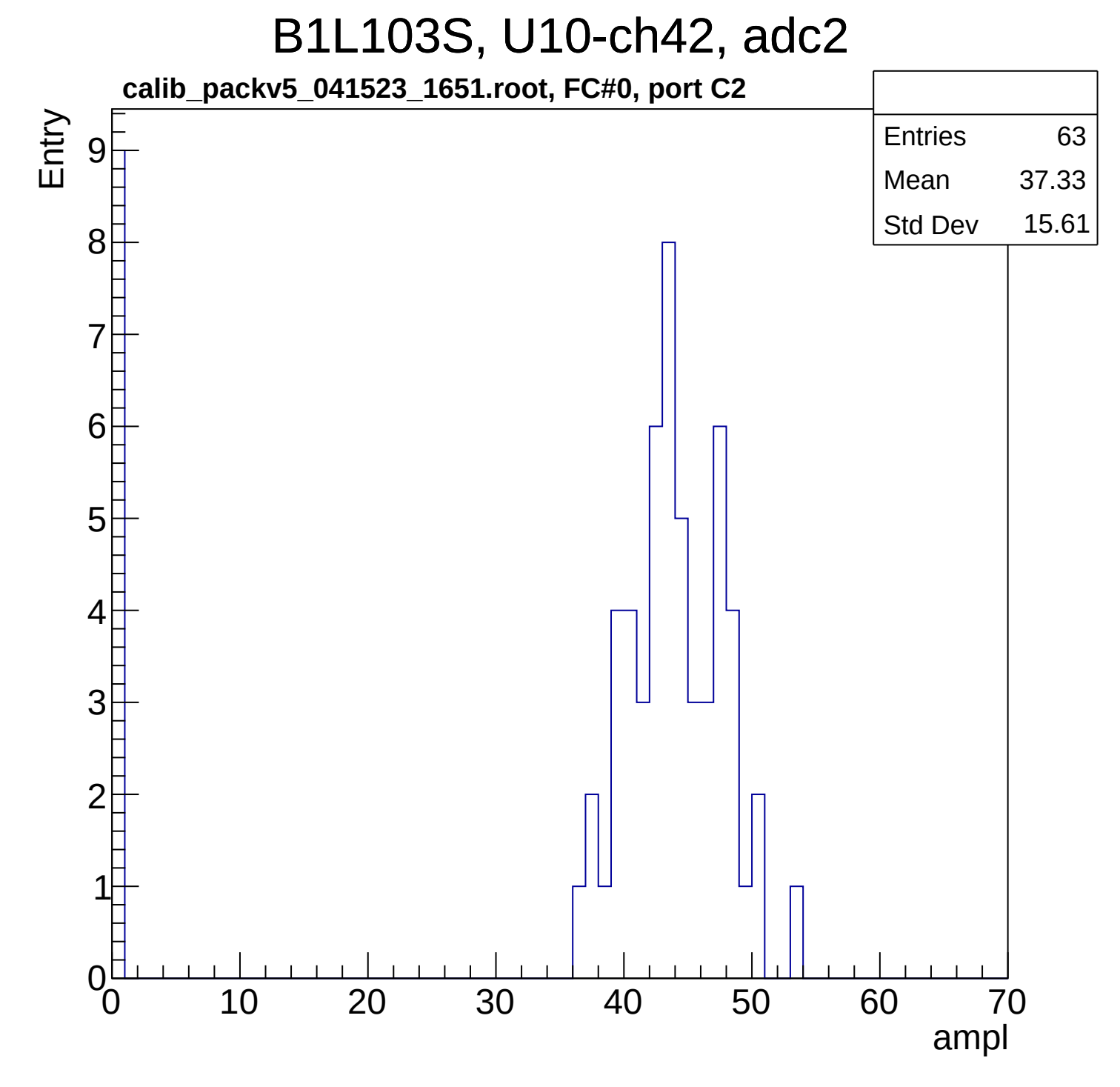
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U10-ch41, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch42, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 27.21
Std Dev 7.141
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U10-ch42, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 35.85
Std Dev 5.15
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U10-ch42, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 37.33
Std Dev 15.61
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
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60
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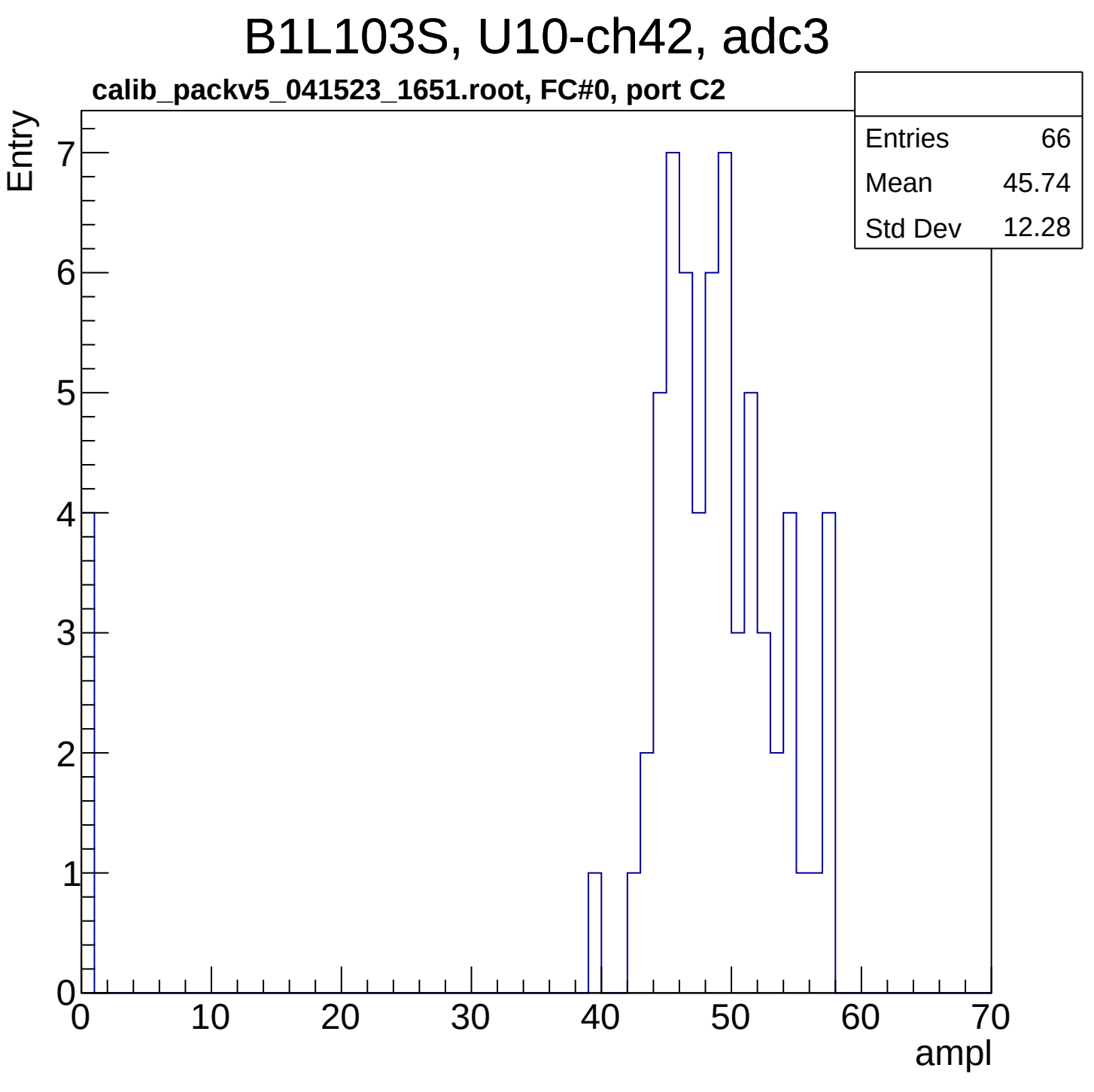
B1L103S, U10-ch42, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 45.74
Std Dev 12.28
Entry
ampl
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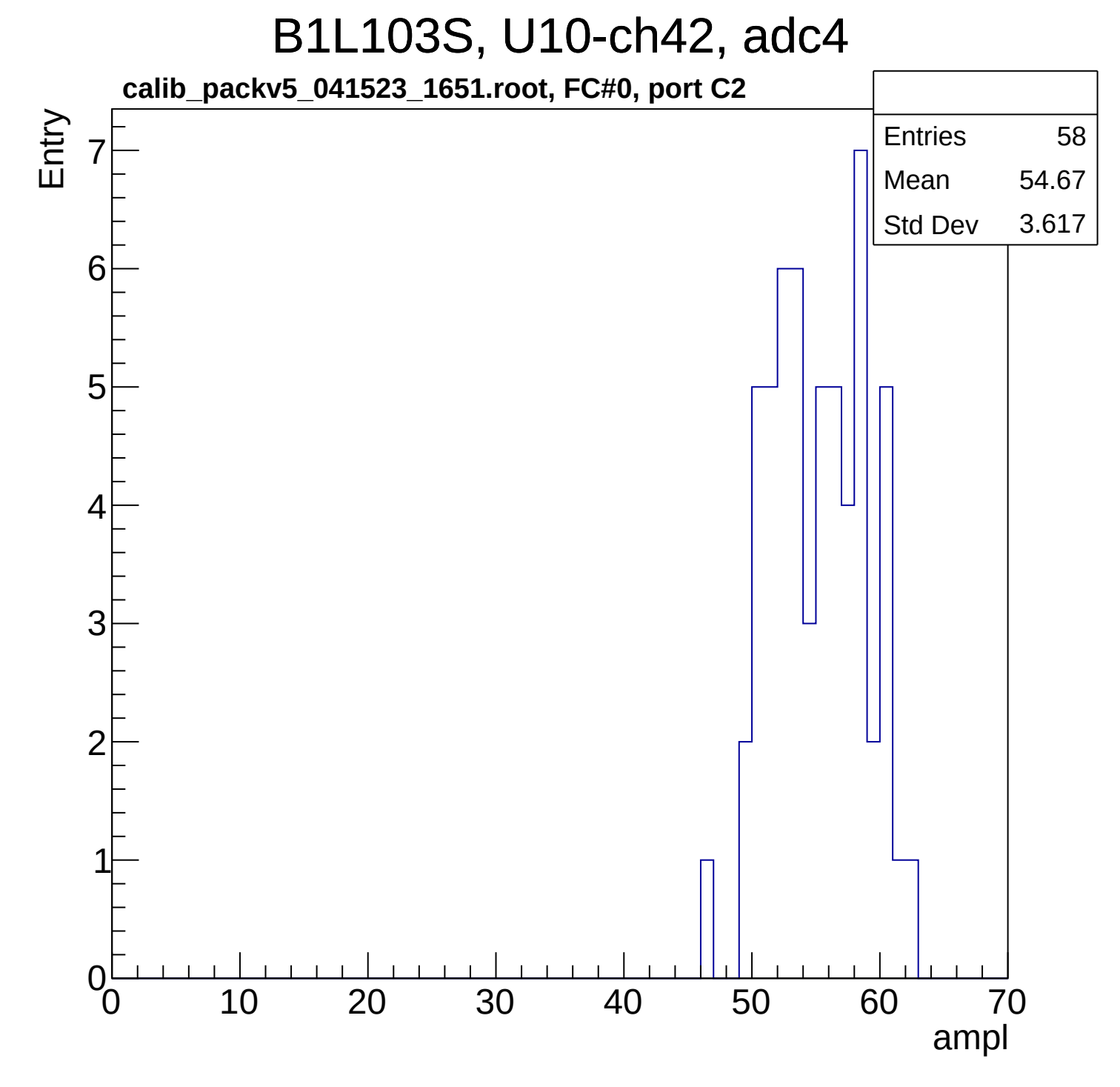
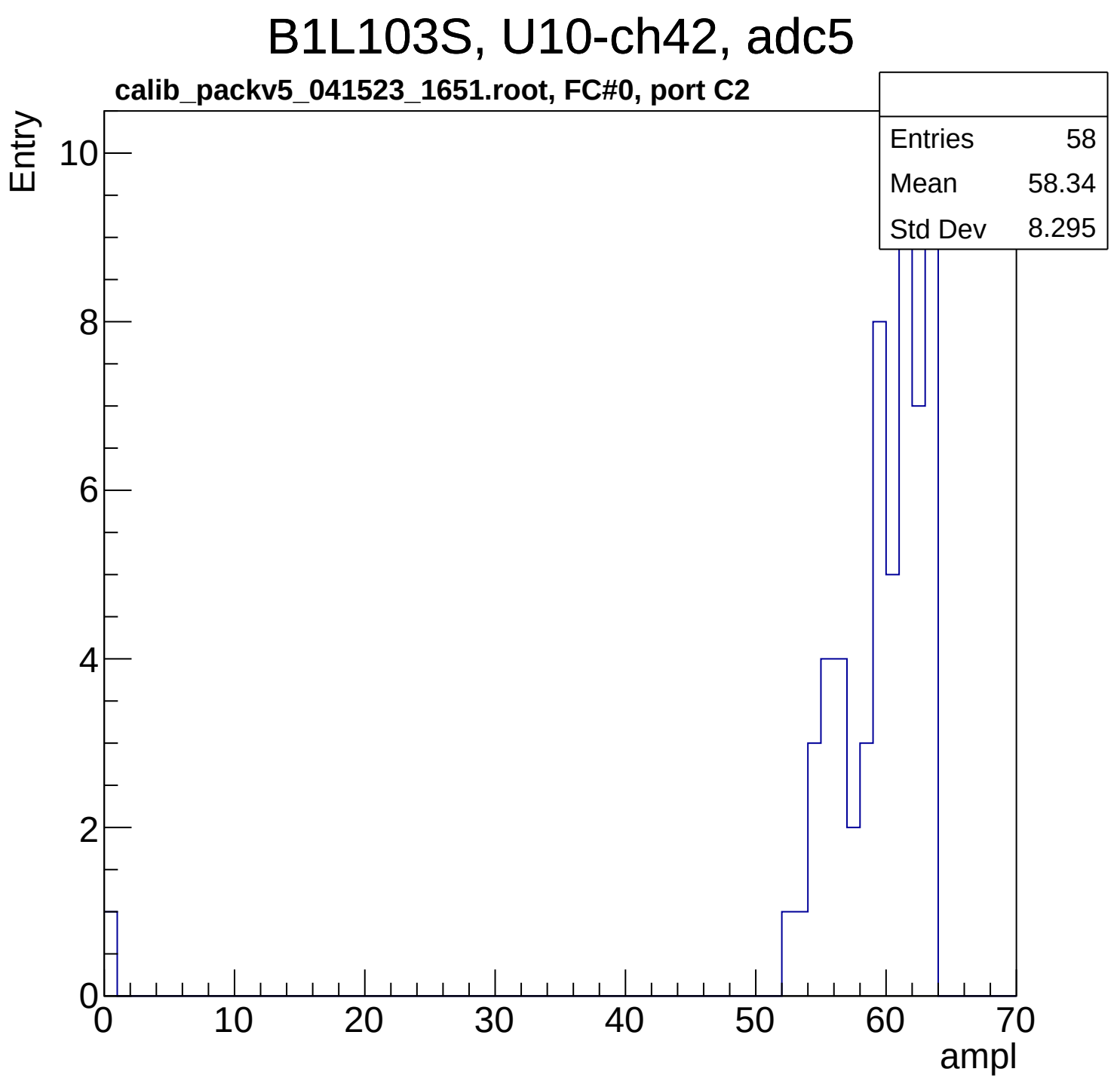
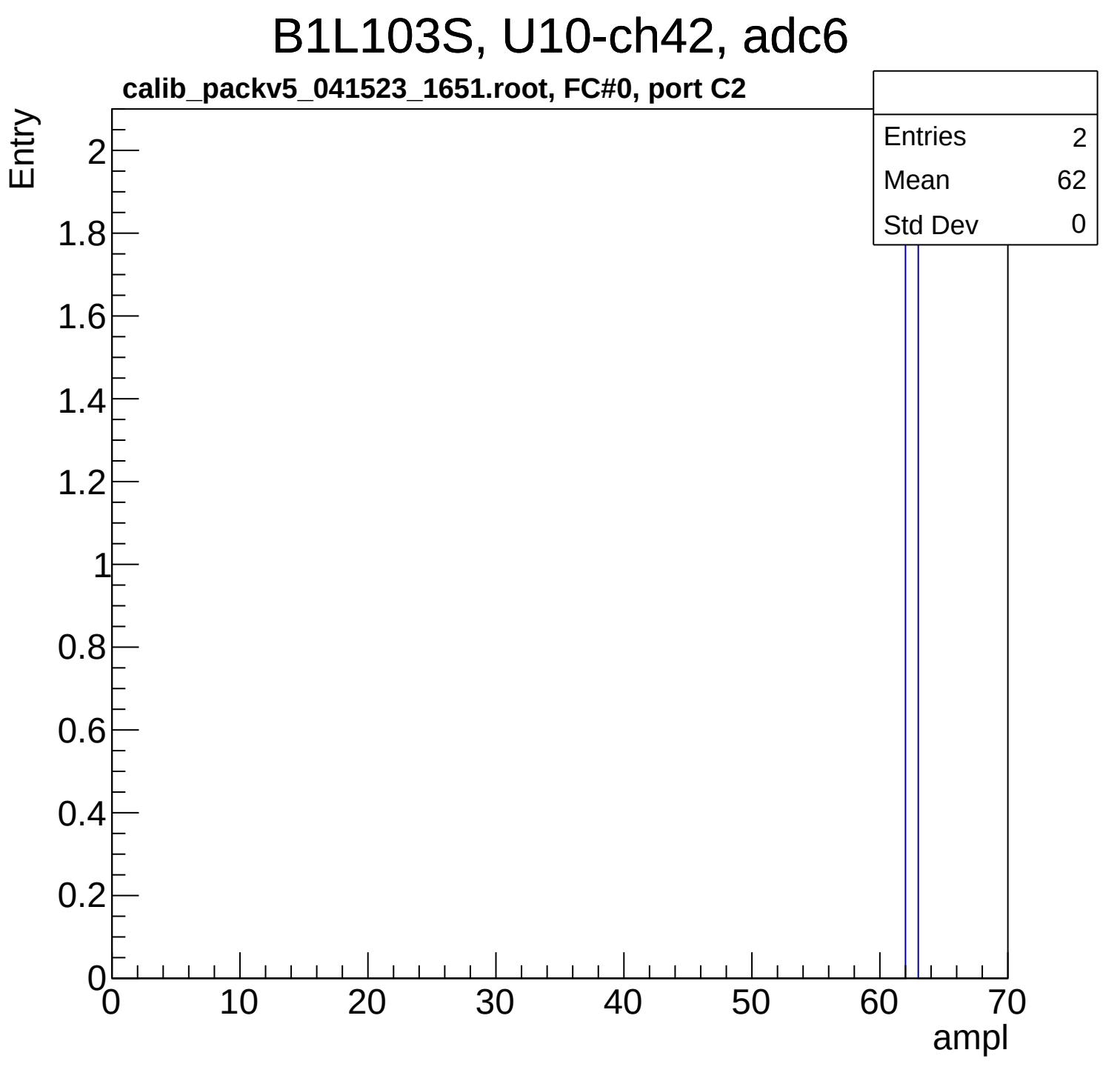
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U10-ch42, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 54.67
Std Dev 3.617
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U10-ch42, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 58.34
Std Dev 8.295
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch42, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 2
Mean 62
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
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40
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60
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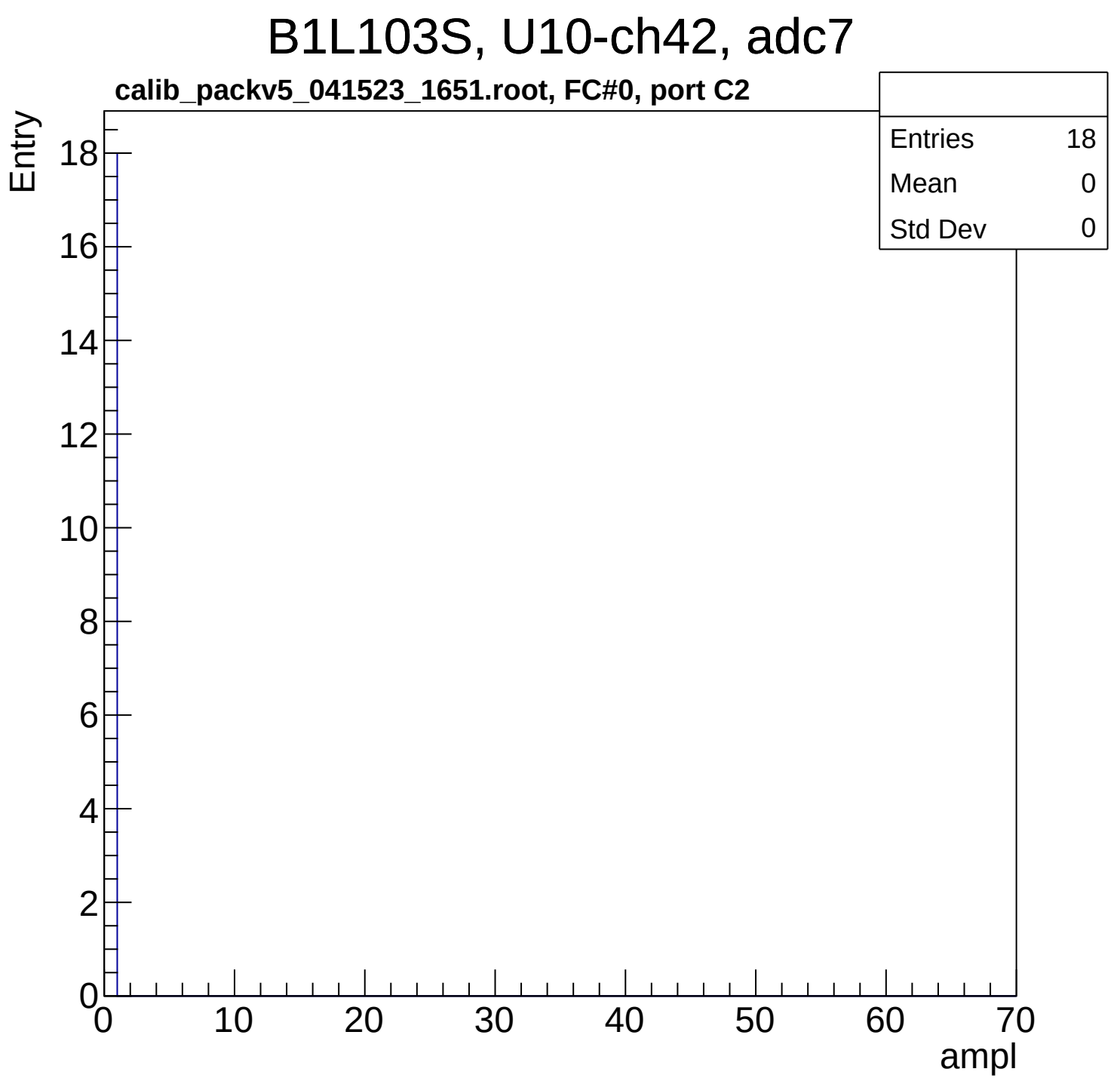
B1L103S, U10-ch42, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
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10
20
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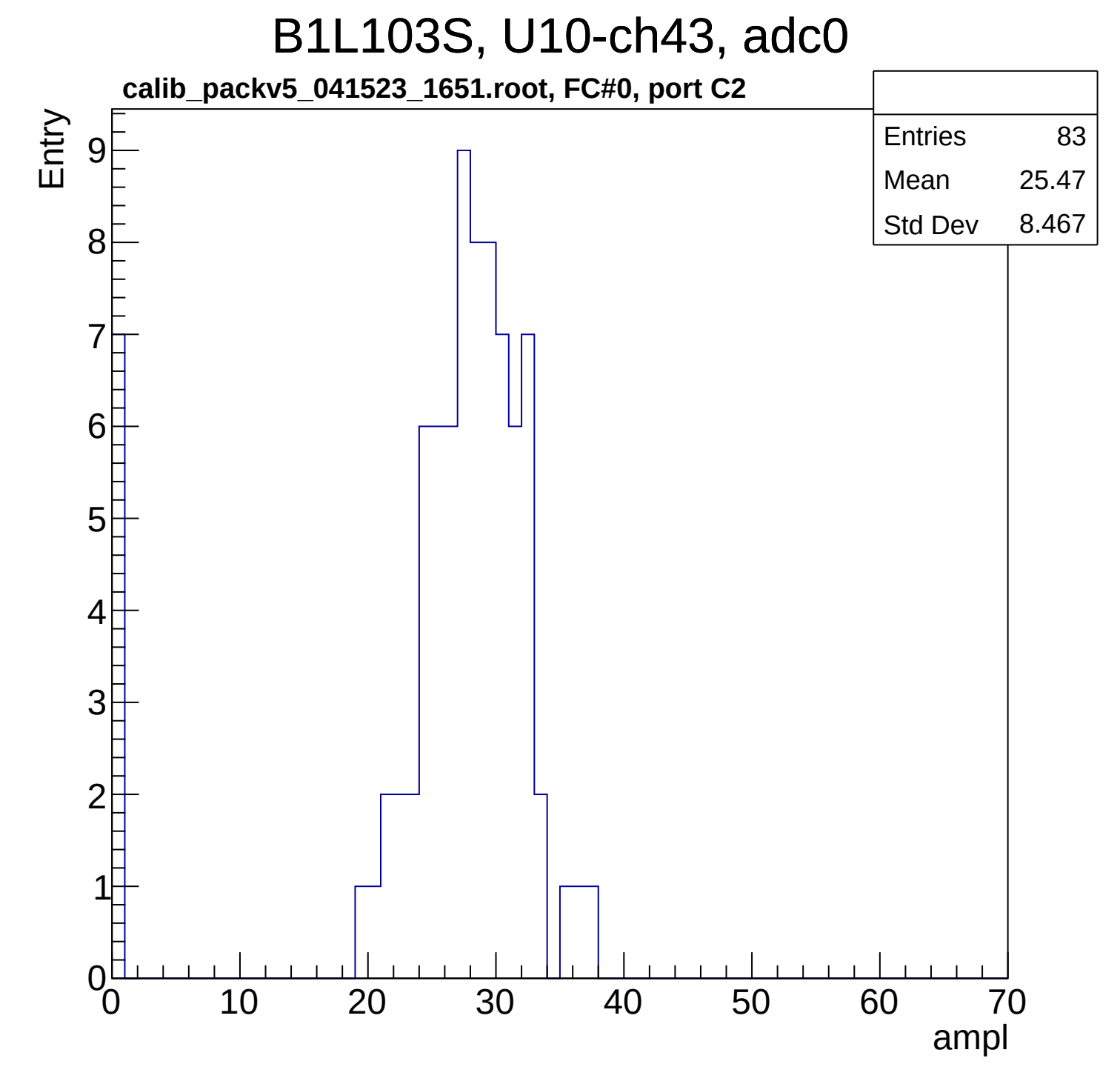
50
60
70
ampl


B1L103S, U10-ch43, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 25.47
Std Dev 8.467
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
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40
50
60
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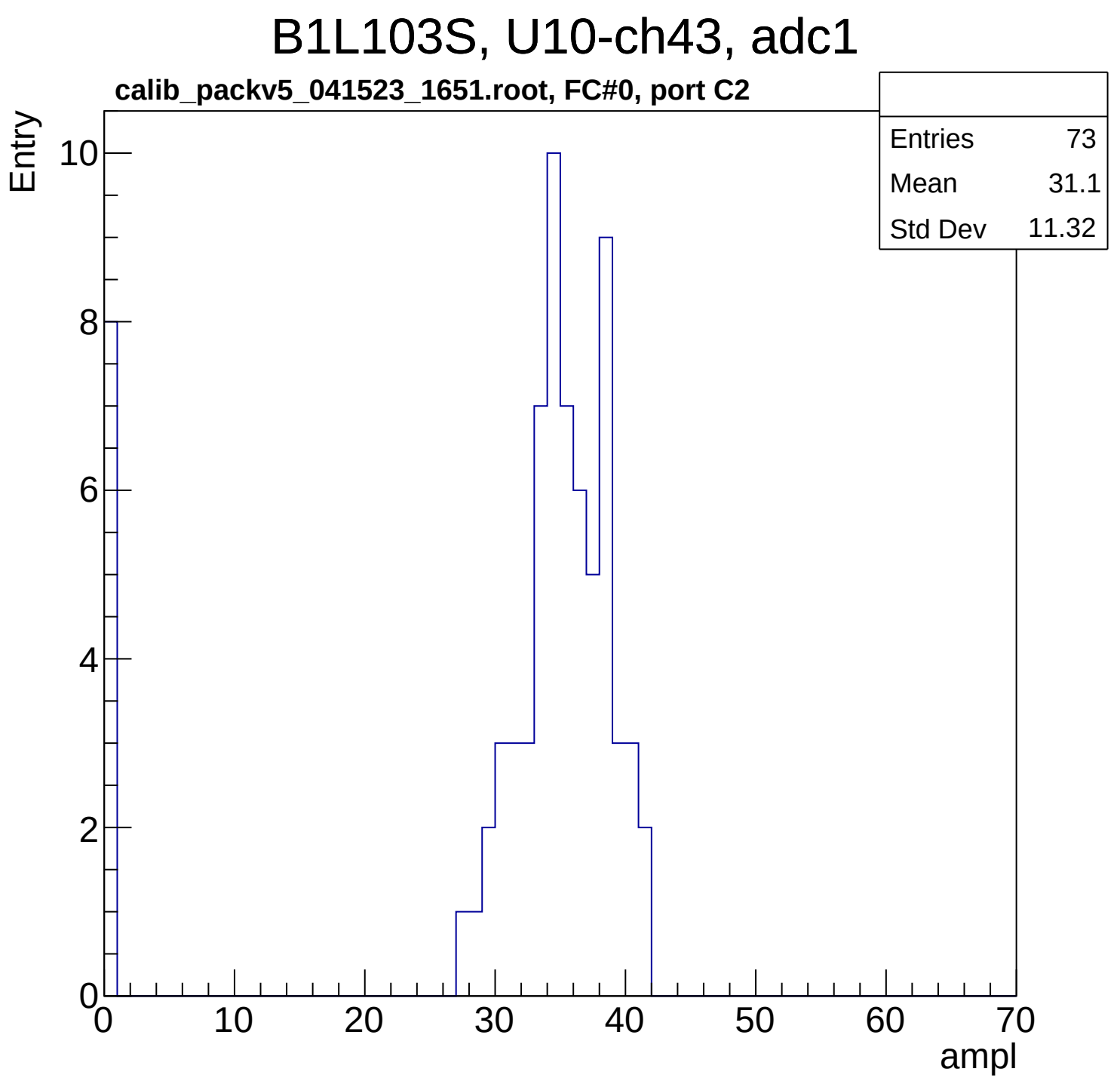
B1L103S, U10-ch43, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 31.1
Std Dev 11.32
Entry
ampl
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4
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8
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0
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40
50
60
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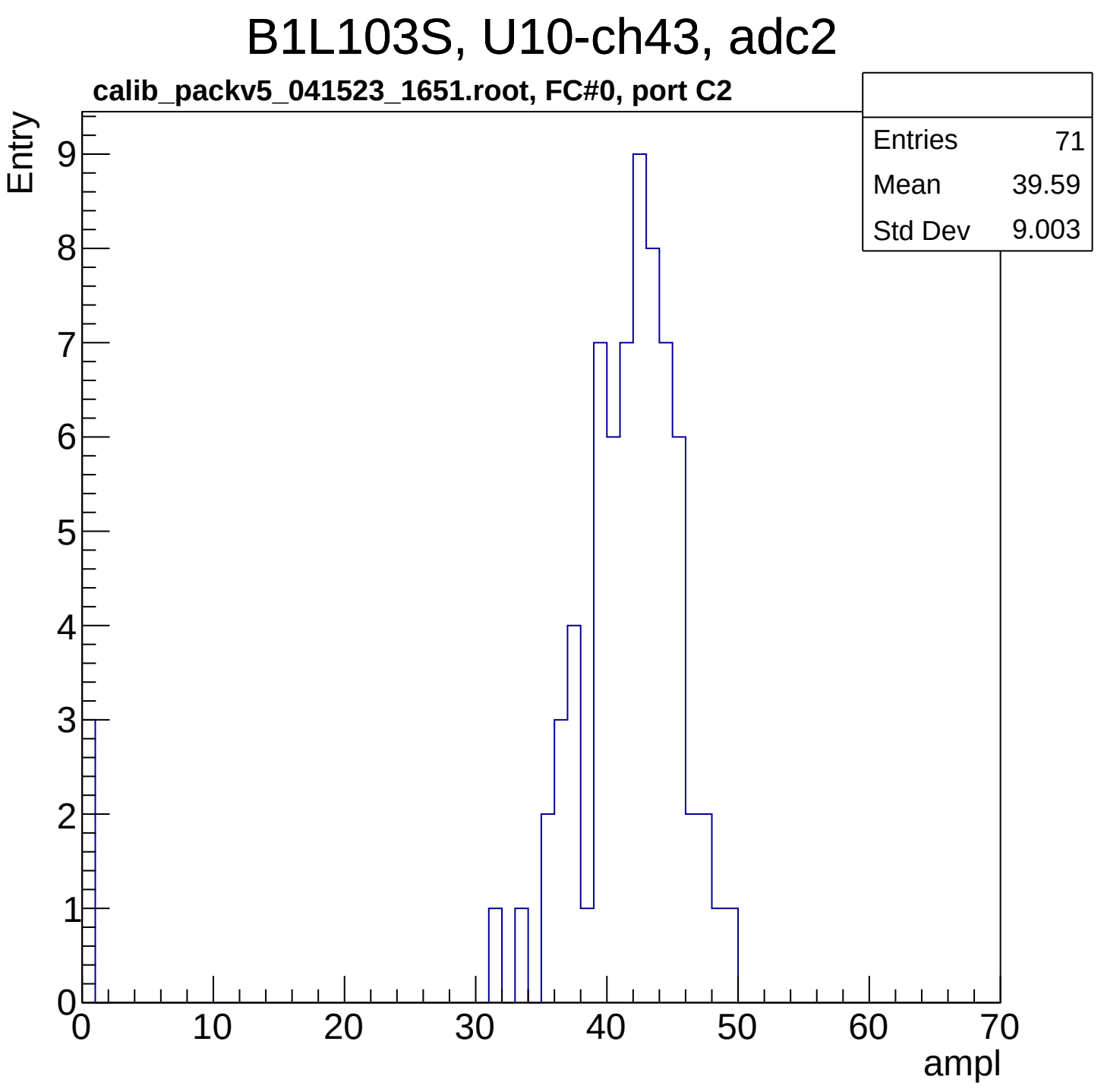
B1L103S, U10-ch43, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 39.59
Std Dev 9.003
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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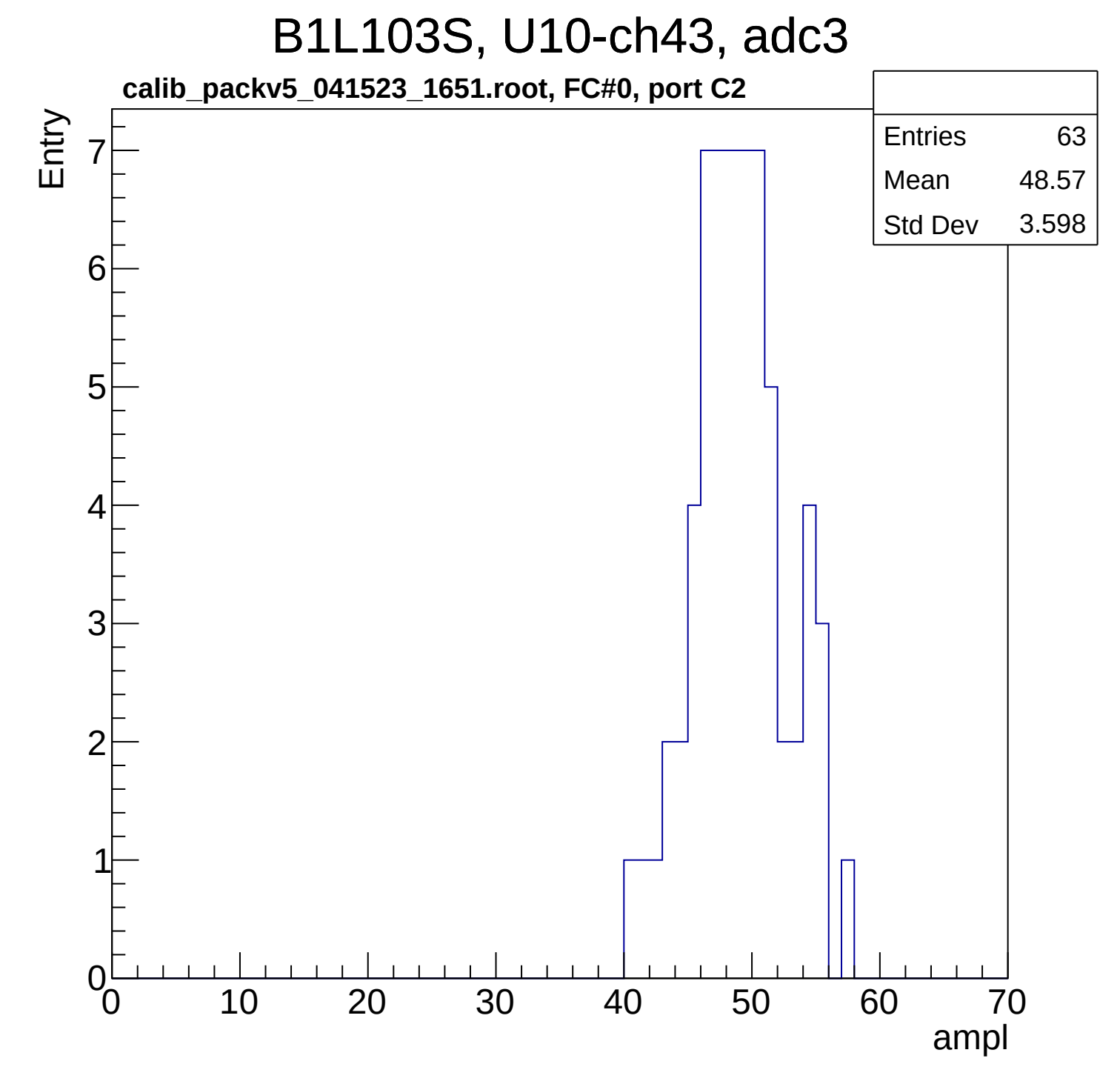
B1L103S, U10-ch43, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 48.57
Std Dev 3.598
Entry
ampl
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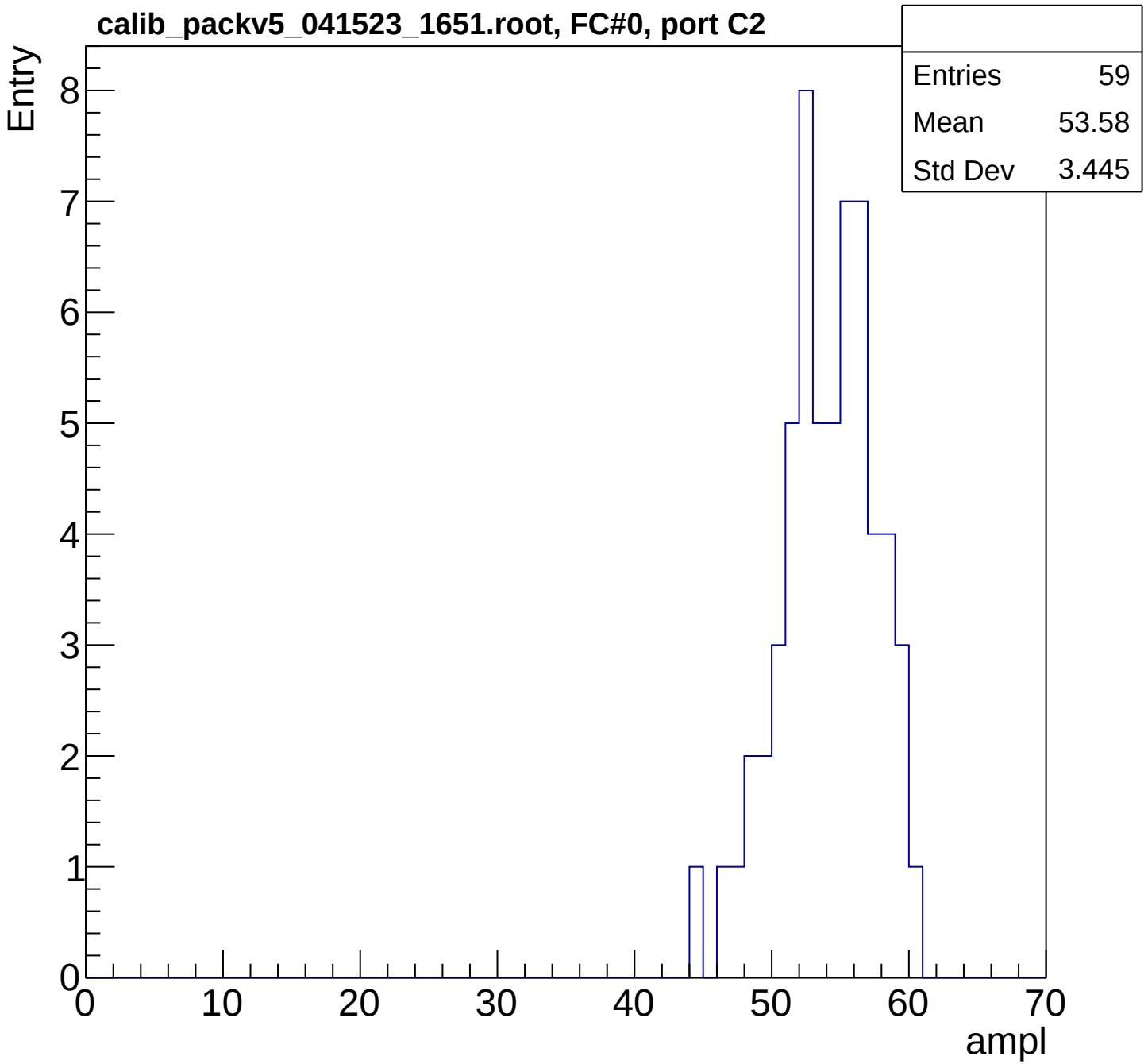
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U10-ch43, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 53.58
Std Dev 3.445
Entry
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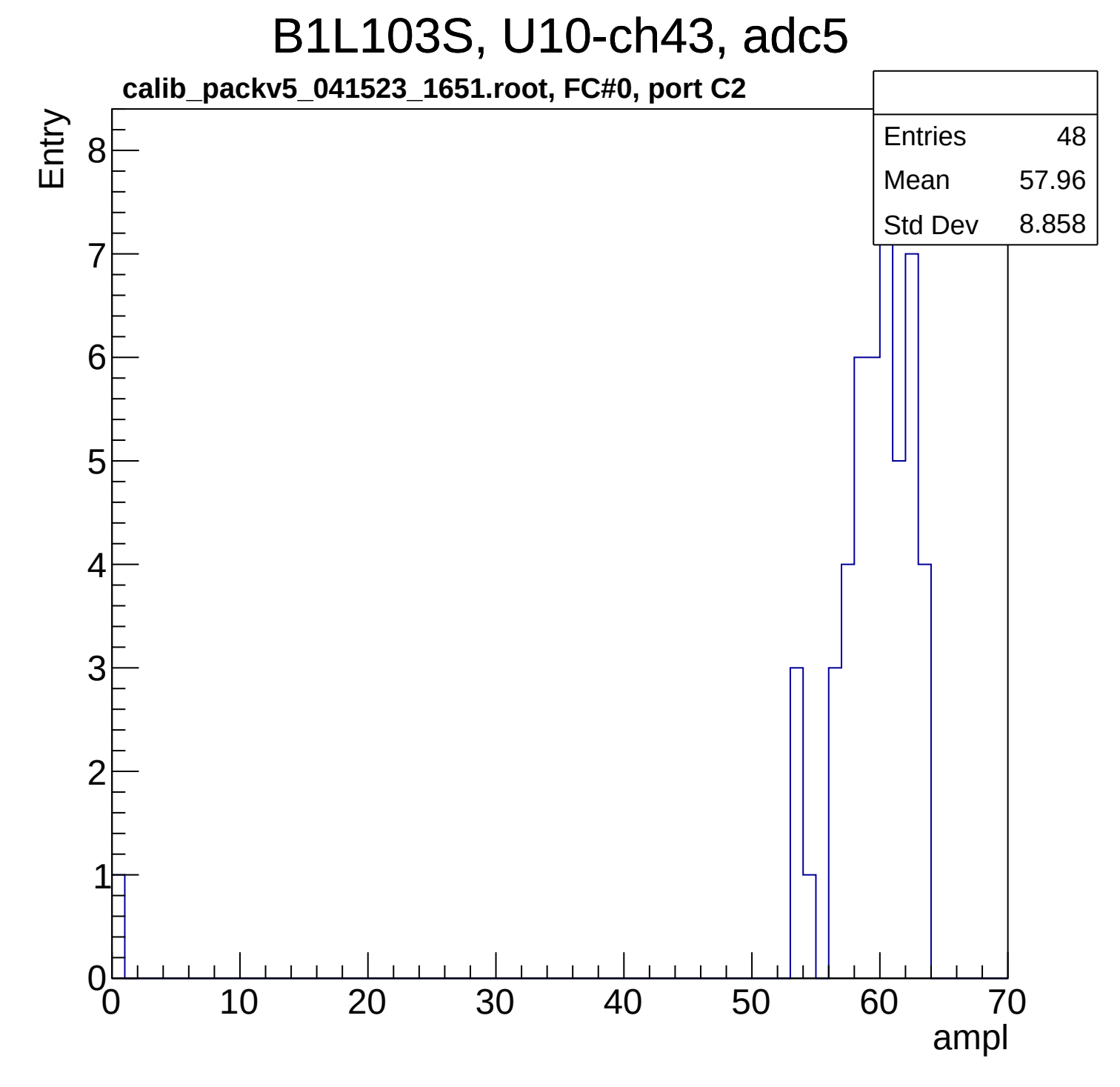
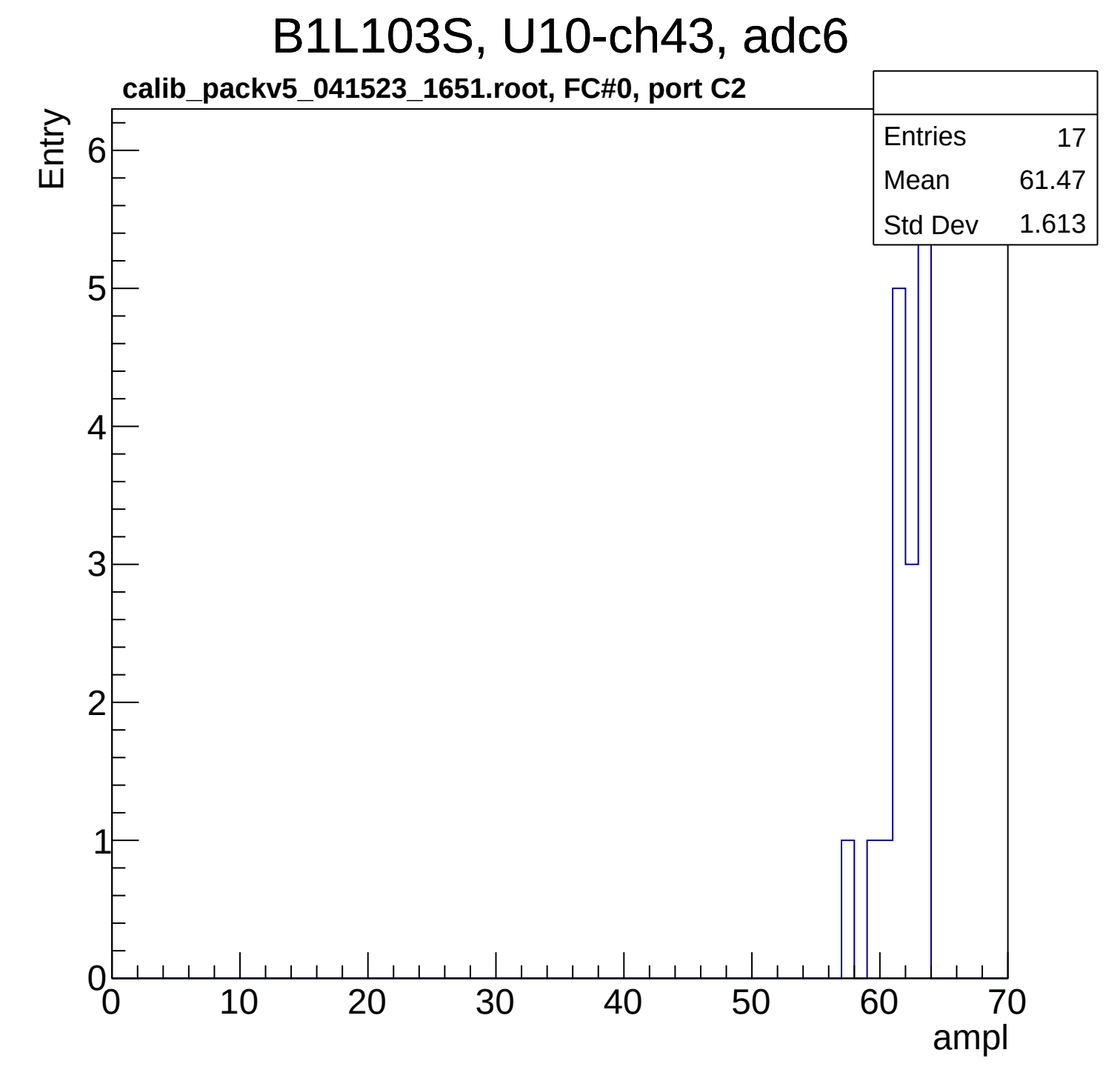
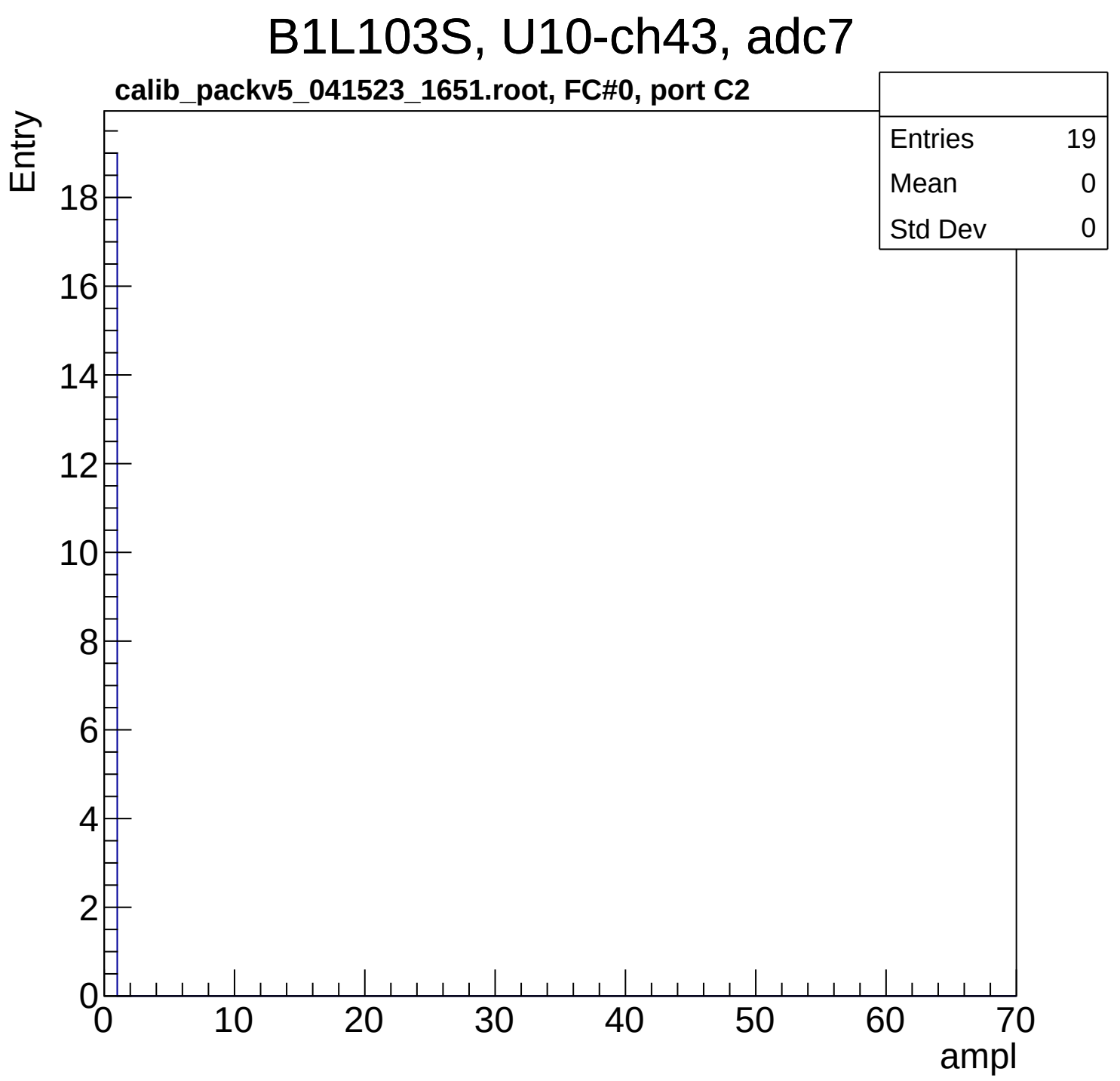
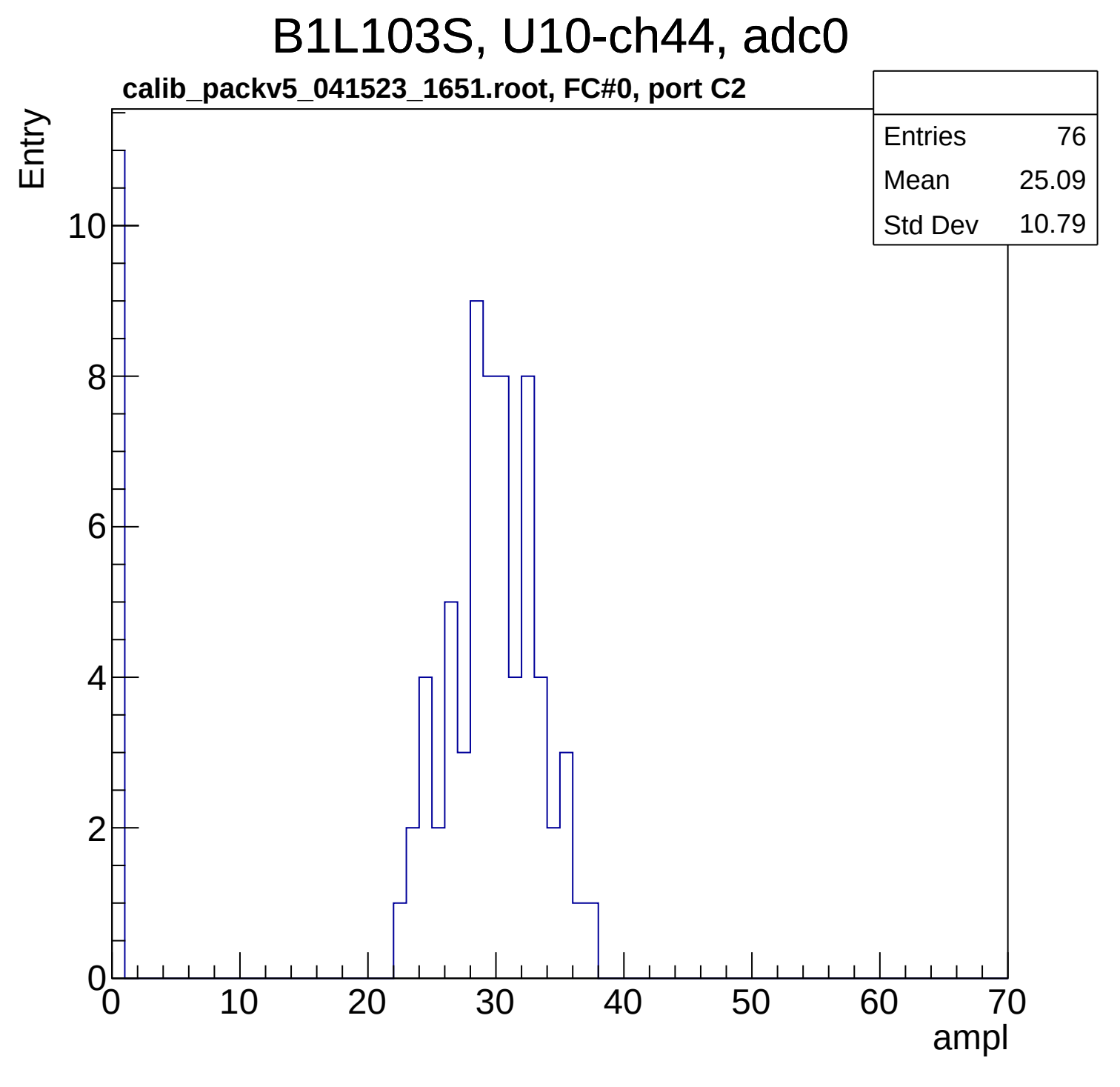
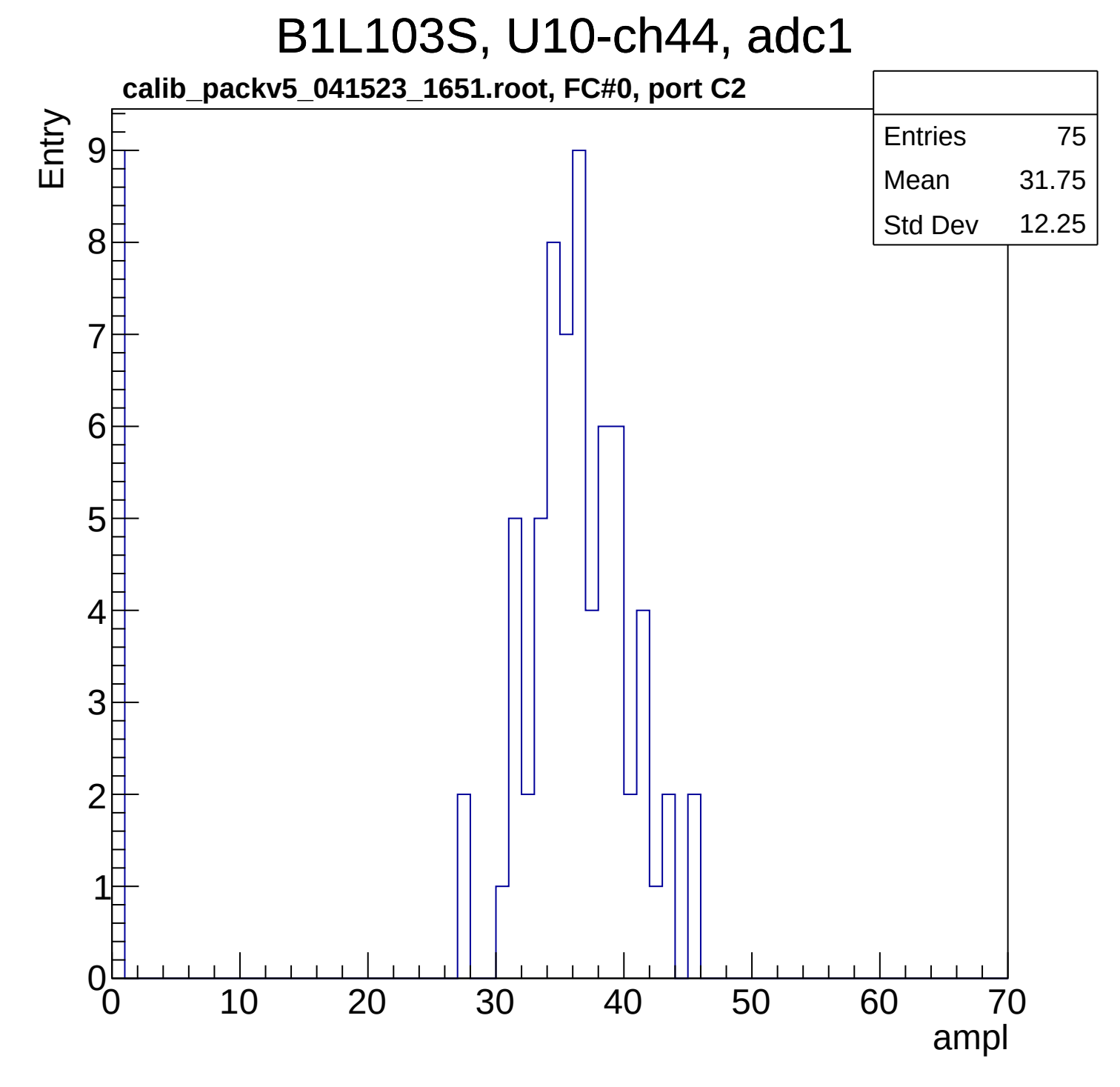
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch43, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 57.96
Std Dev 8.858
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U10-ch43, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 17
Mean 61.47
Std Dev 1.613
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U10-ch43, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch44, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 25.09
Std Dev 10.79
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch44, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 31.75
Std Dev 12.25
Entry
ampl
0
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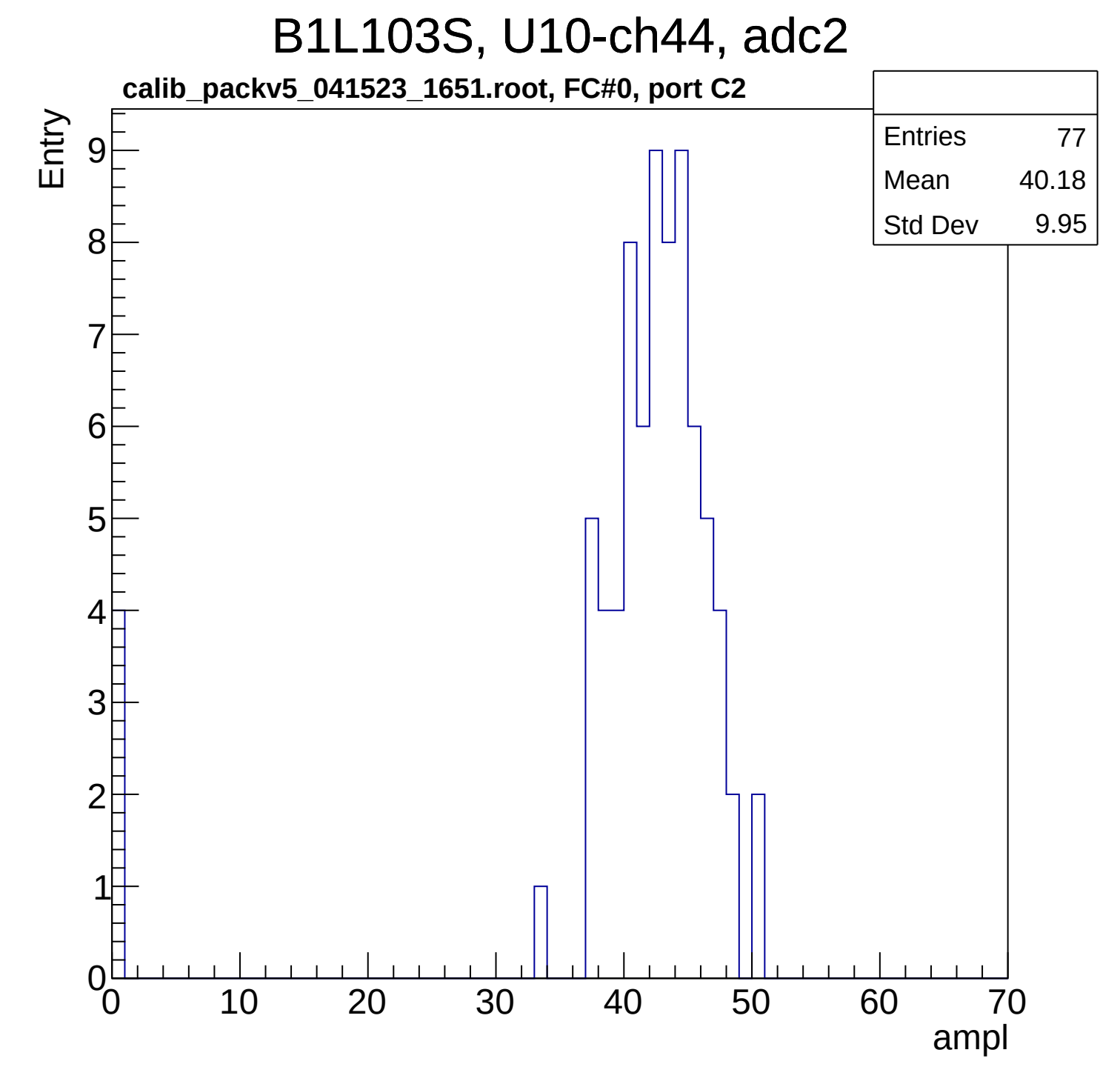
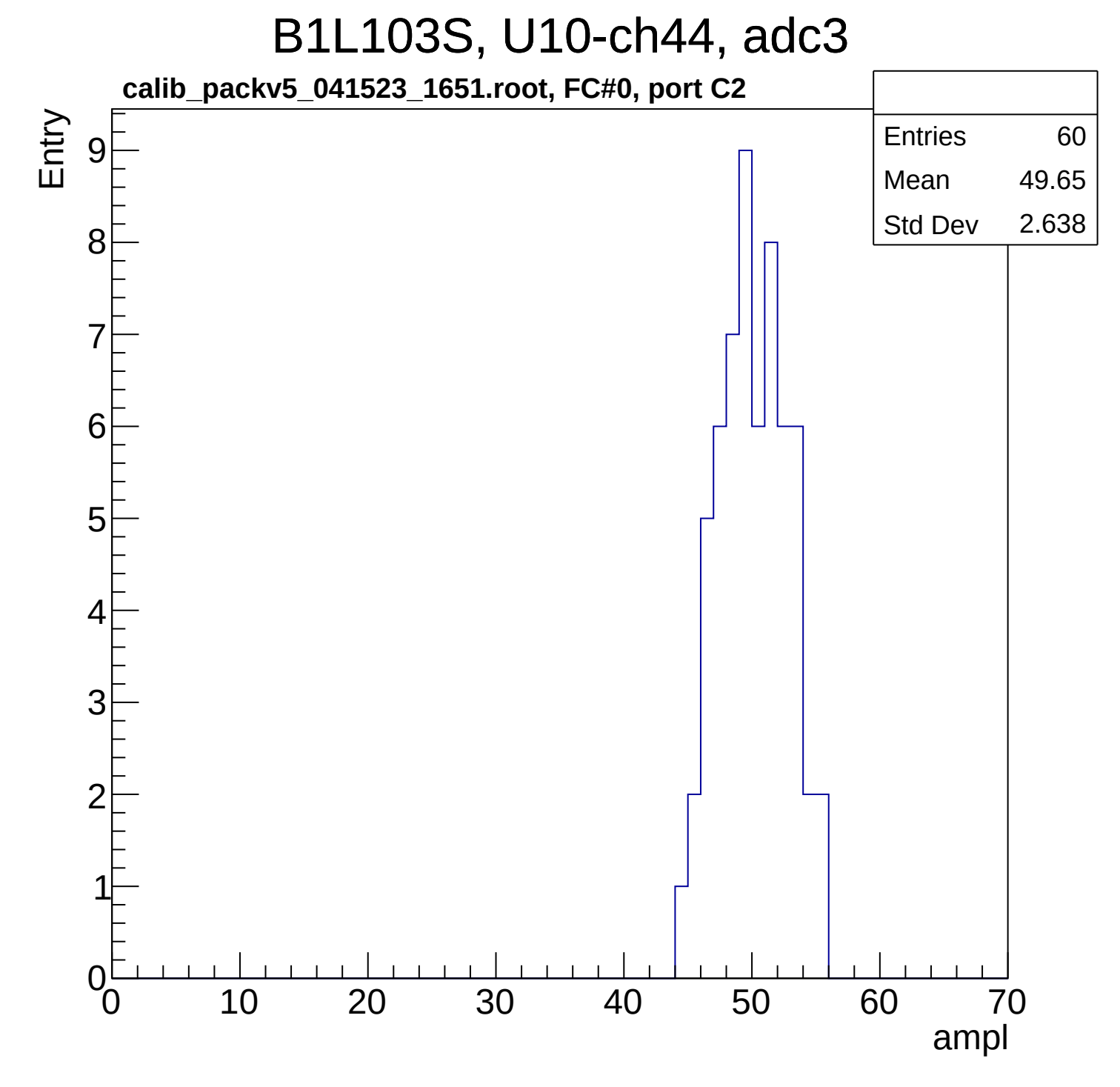
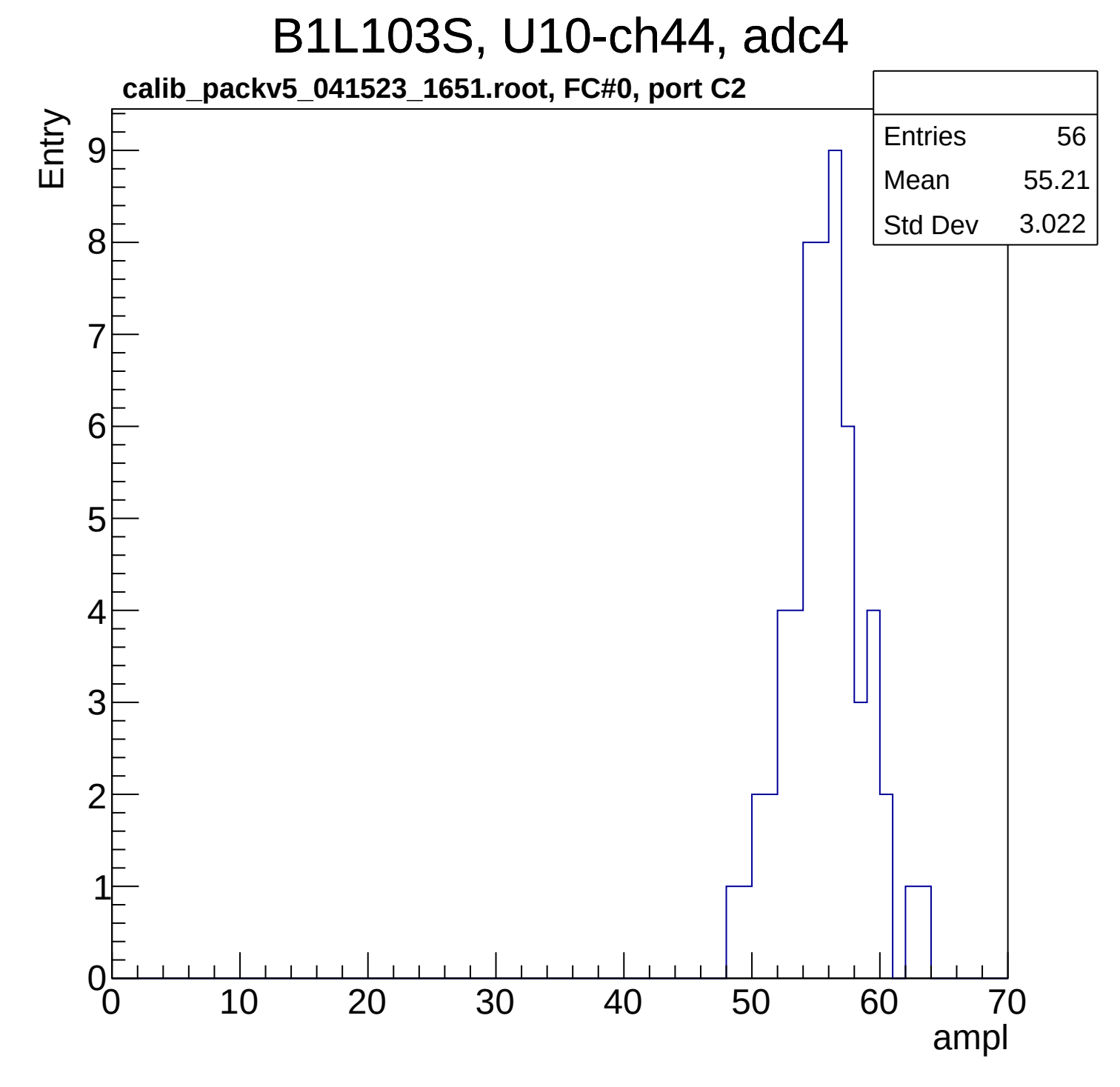
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U10-ch44, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 40.18
Std Dev 9.95
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U10-ch44, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 49.65
Std Dev 2.638
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U10-ch44, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 55.21
Std Dev 3.022
Entry
ampl
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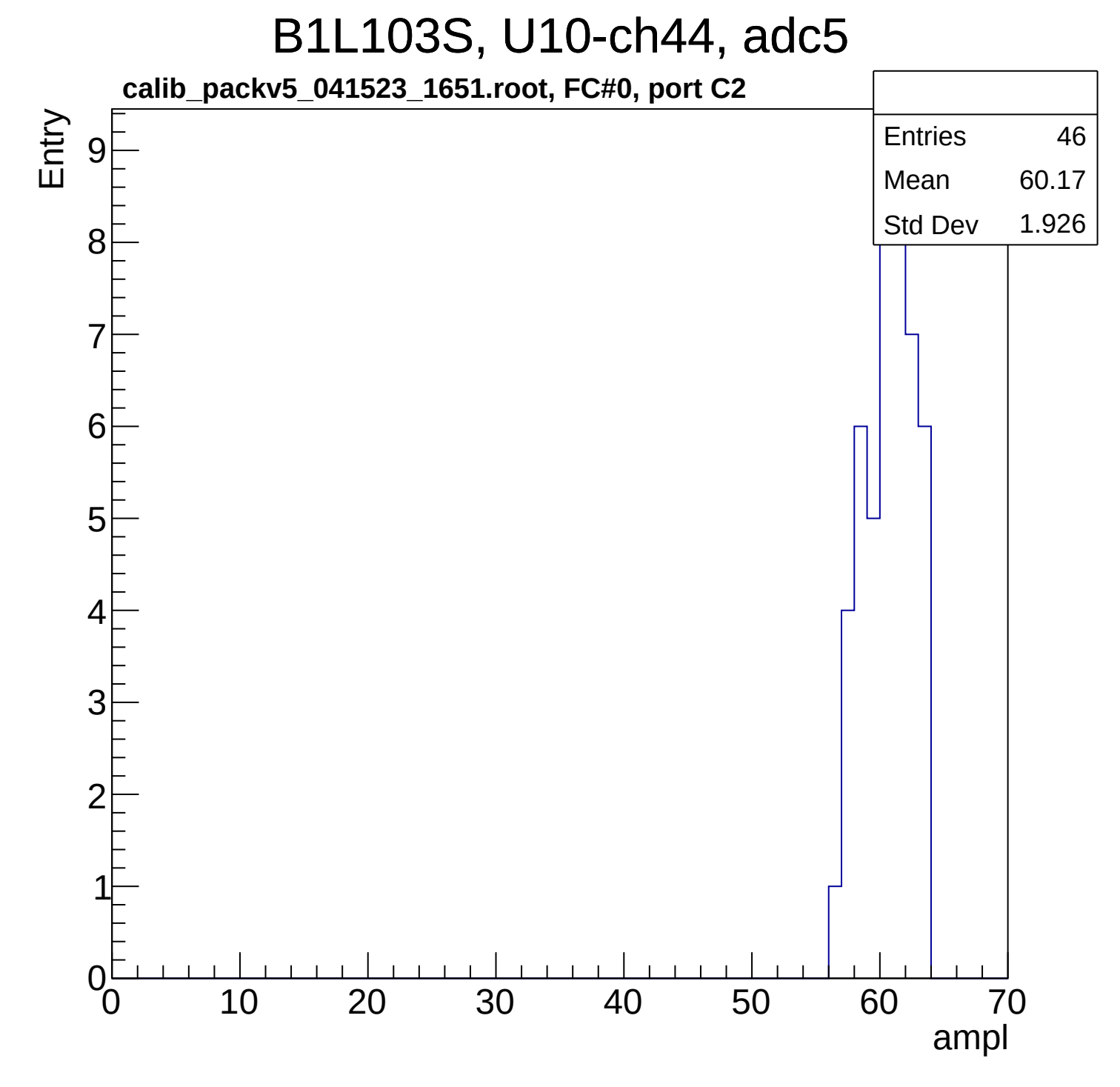
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U10-ch44, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 60.17
Std Dev 1.926
Entry
ampl
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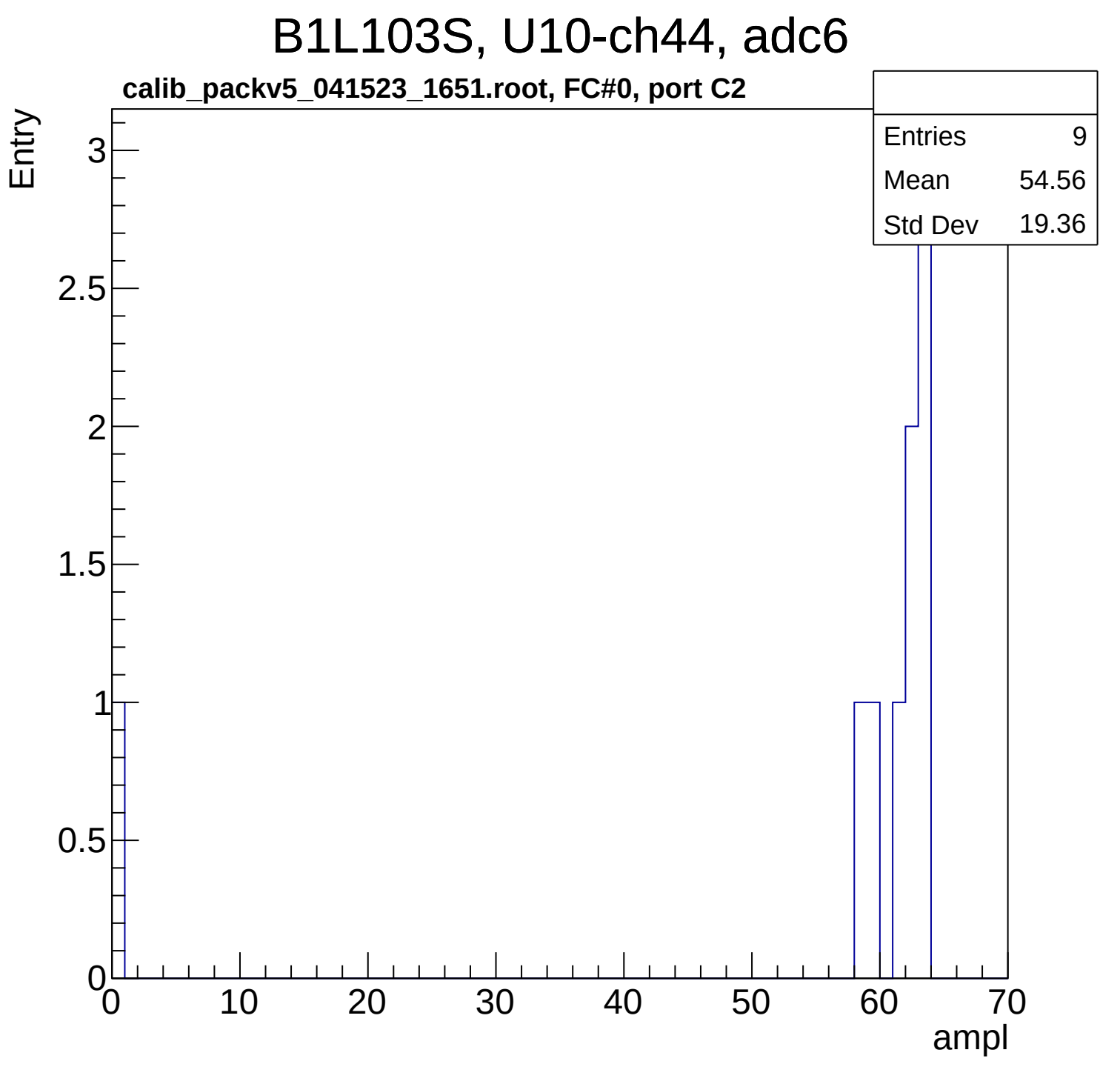
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U10-ch44, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 9
Mean 54.56
Std Dev 19.36
Entry
ampl
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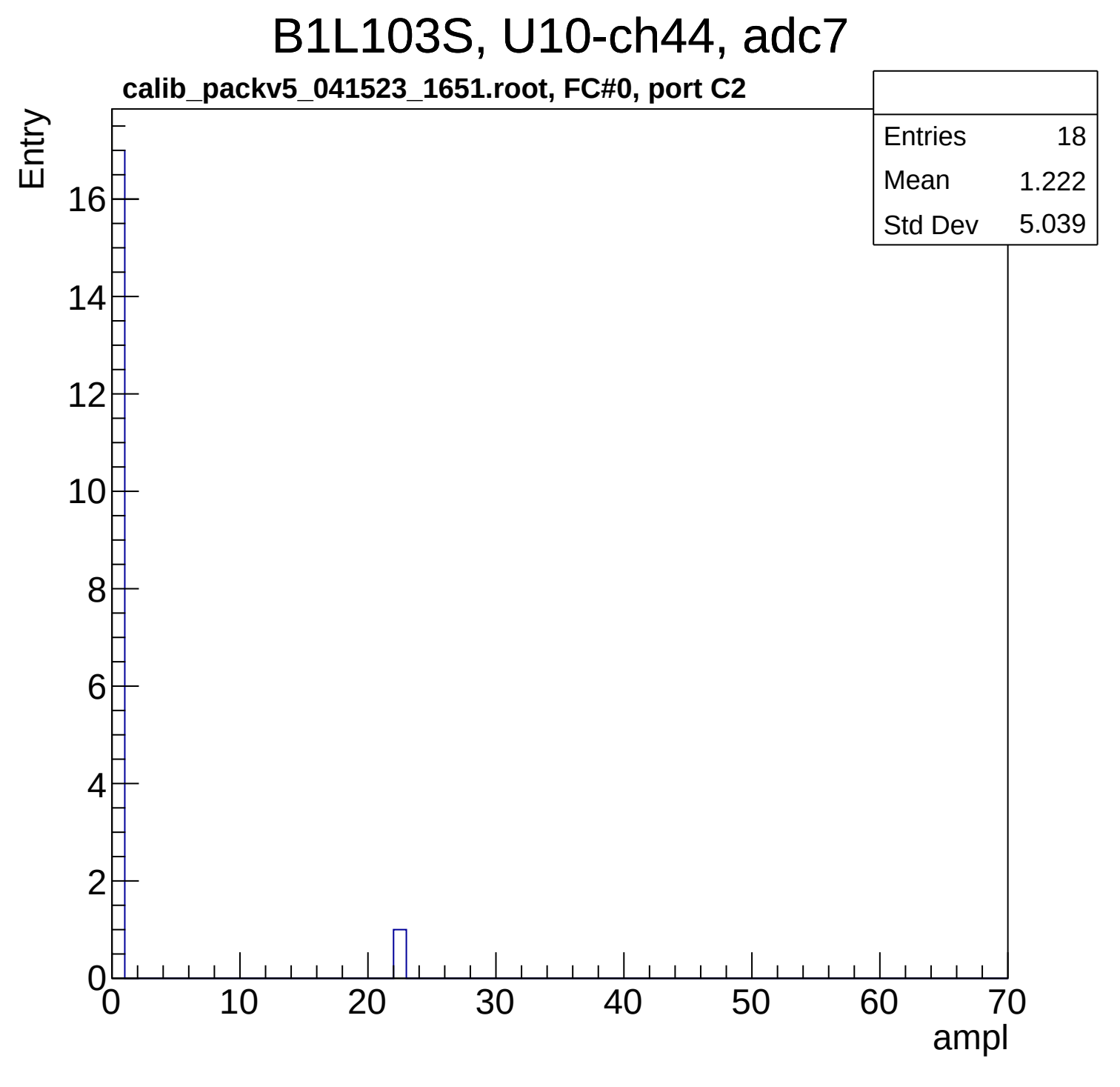
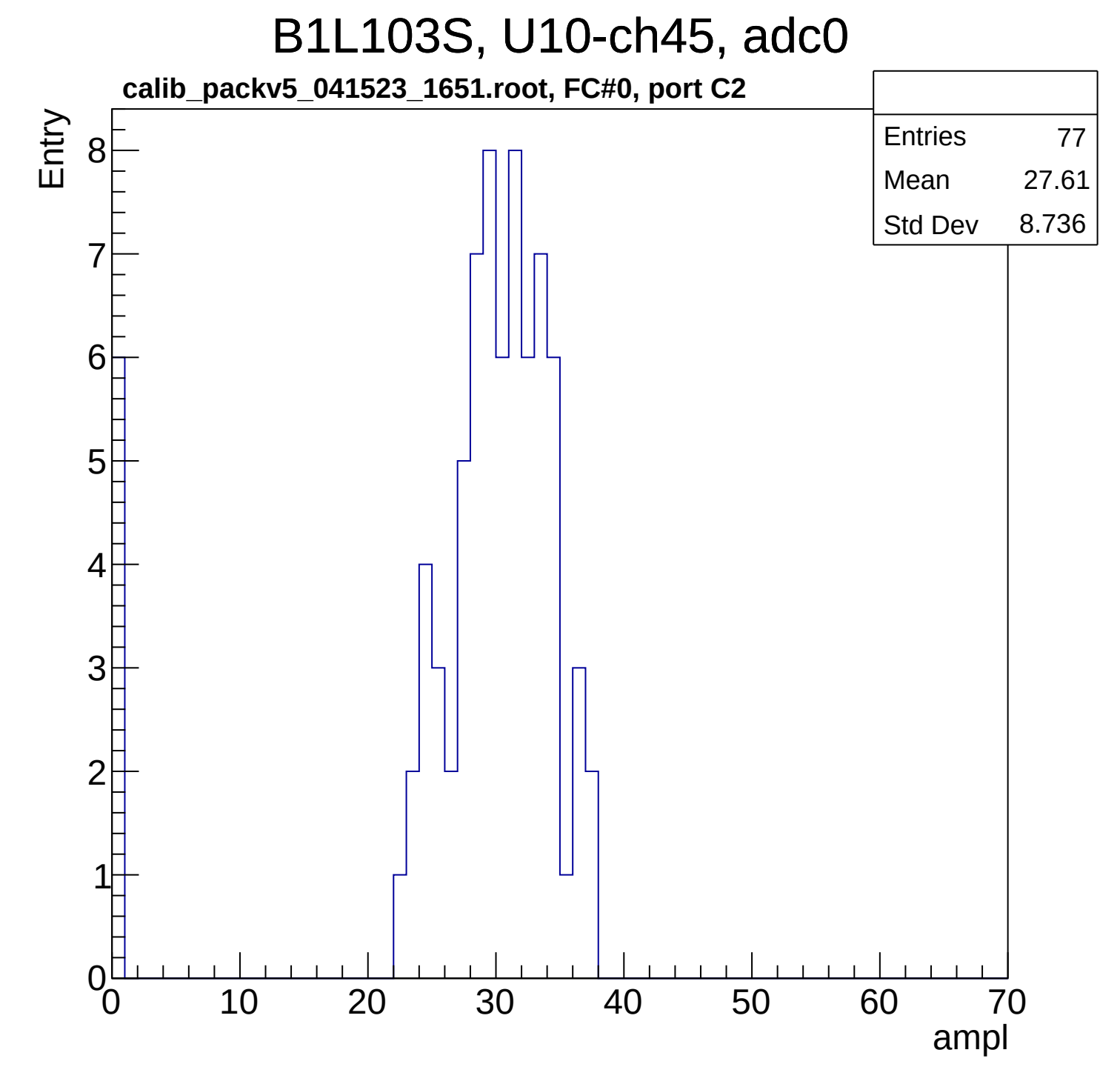
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U10-ch44, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 1.222
Std Dev 5.039
Entry
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch45, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 27.61
Std Dev 8.736
Entry
ampl
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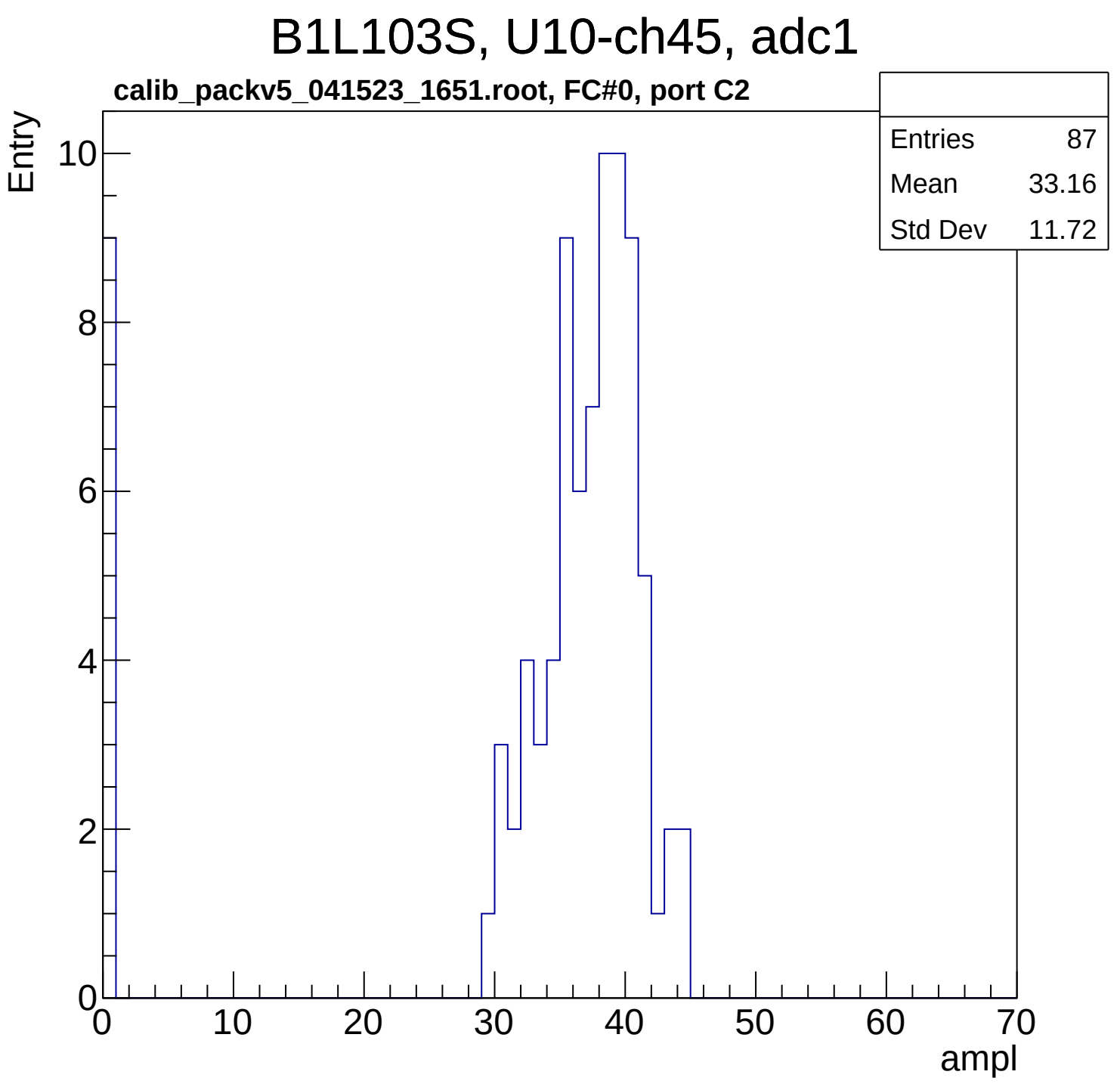
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U10-ch45, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 87
Mean 33.16
Std Dev 11.72
Entry
ampl
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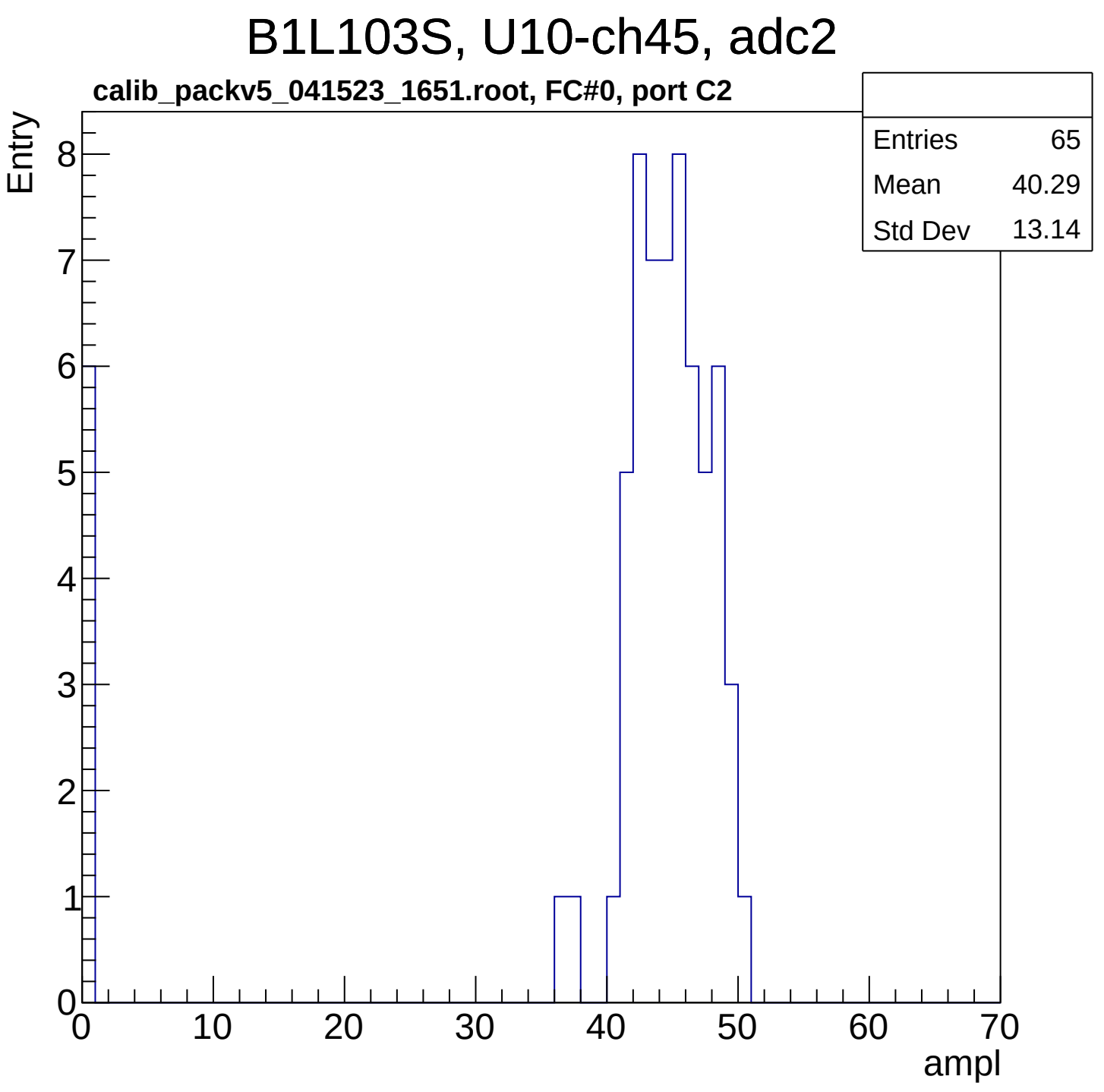
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U10-ch45, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 40.29
Std Dev 13.14
Entry
ampl
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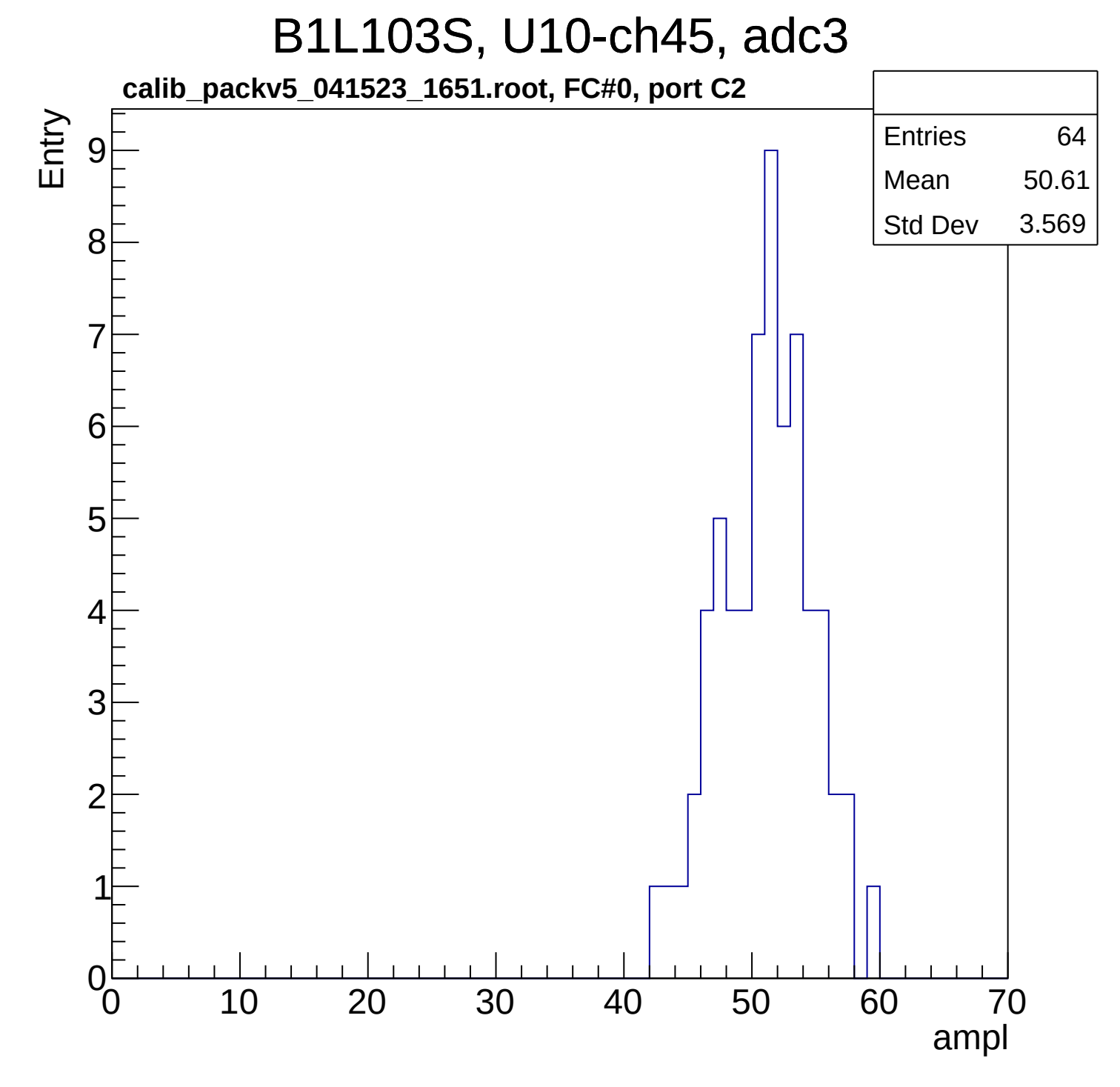
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U10-ch45, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 50.61
Std Dev 3.569
Entry
ampl
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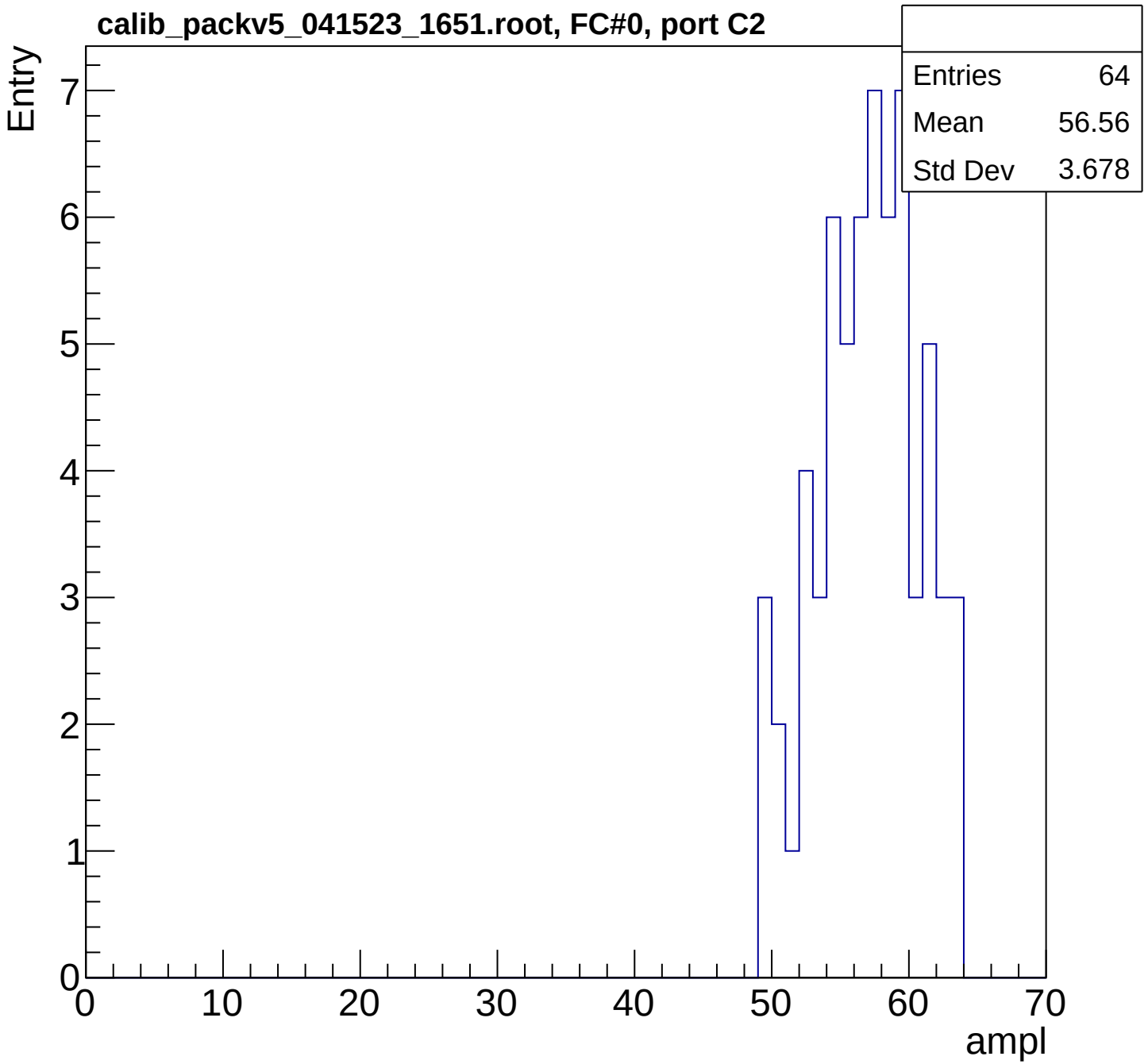
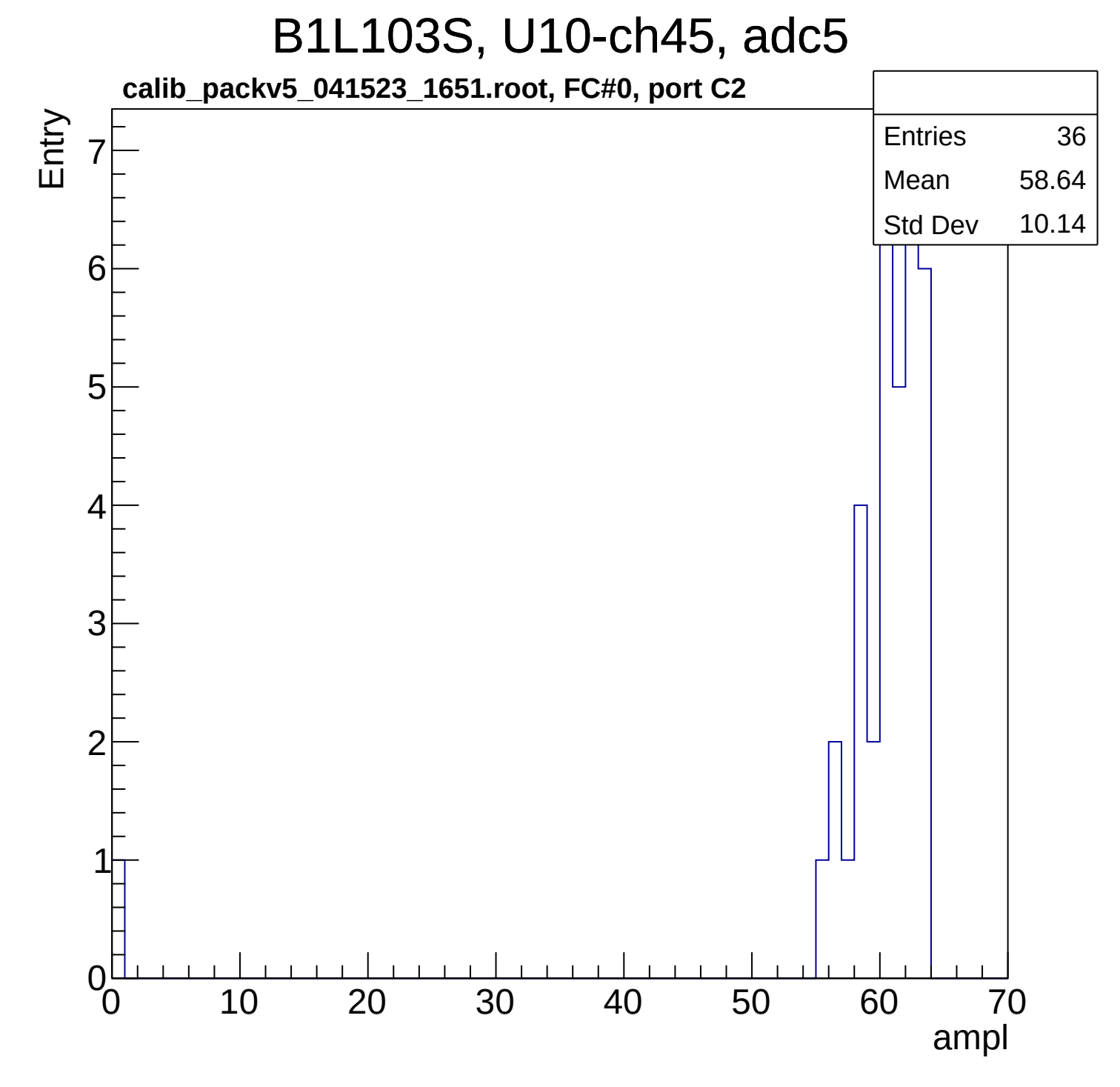
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U10-ch45, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 56.56
Std Dev 3.678
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U10-ch45, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 36
Mean 58.64
Std Dev 10.14
Entry
ampl
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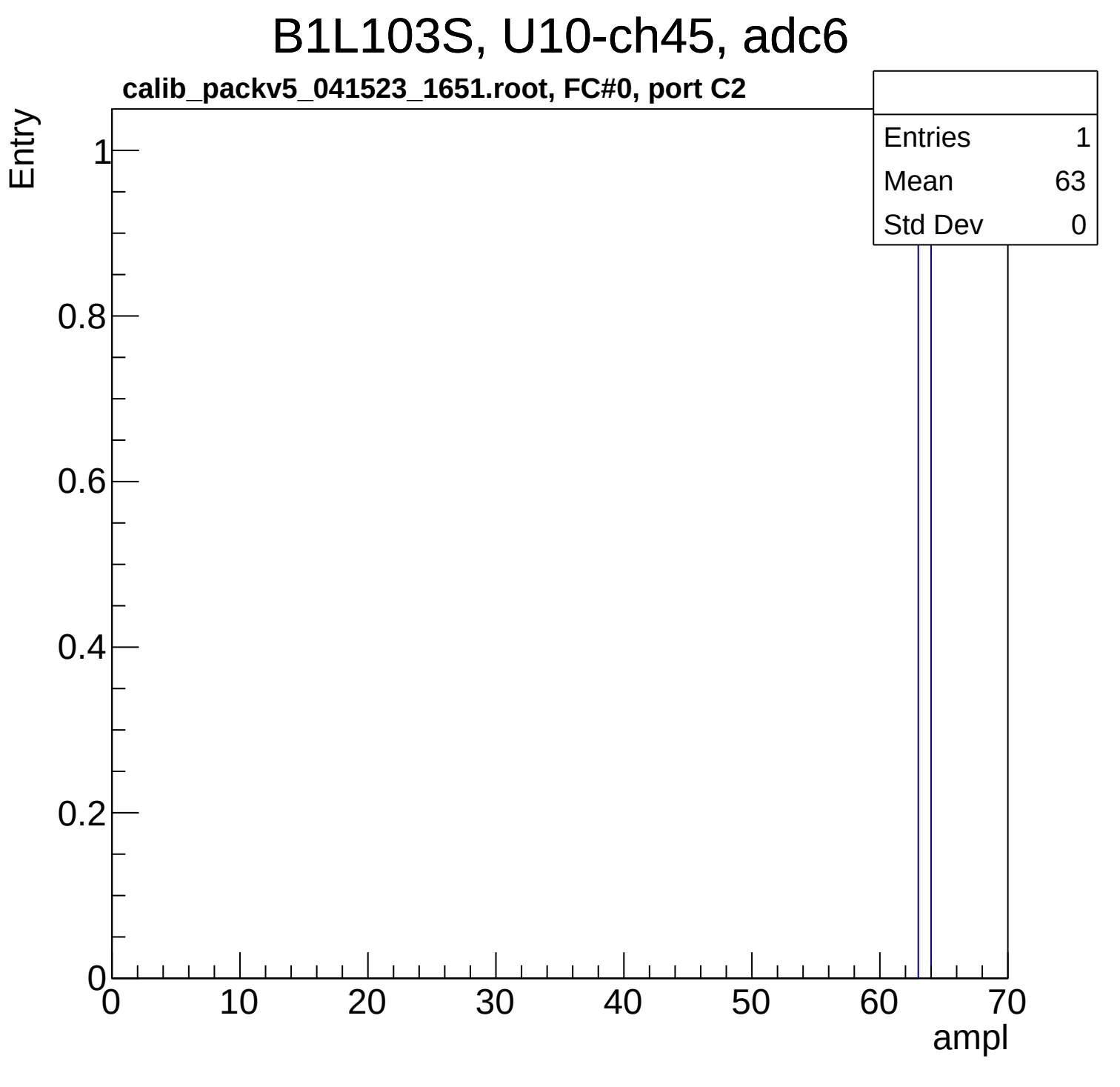
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U10-ch45, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 1
Mean 63
Std Dev 0
Entry
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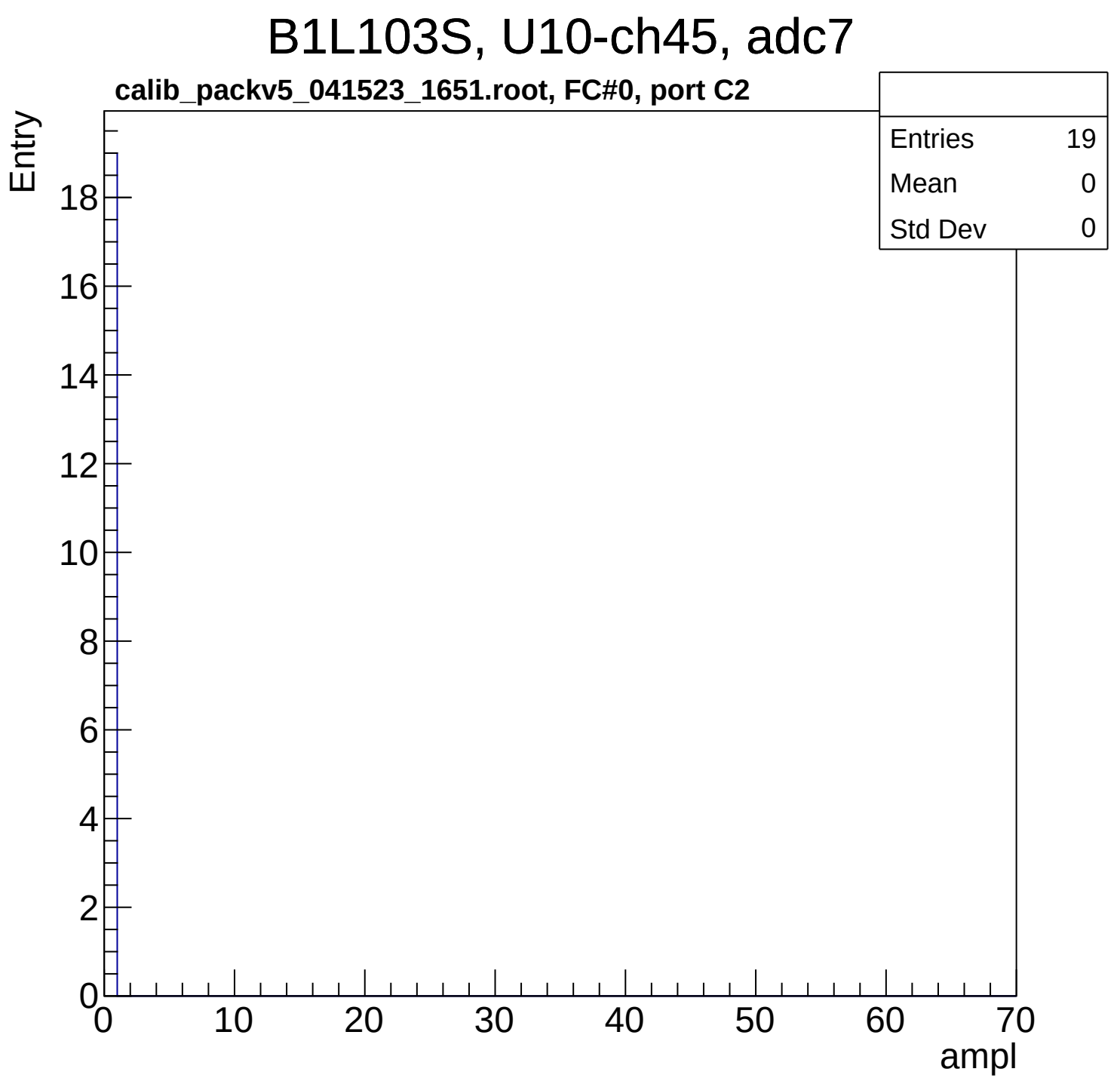
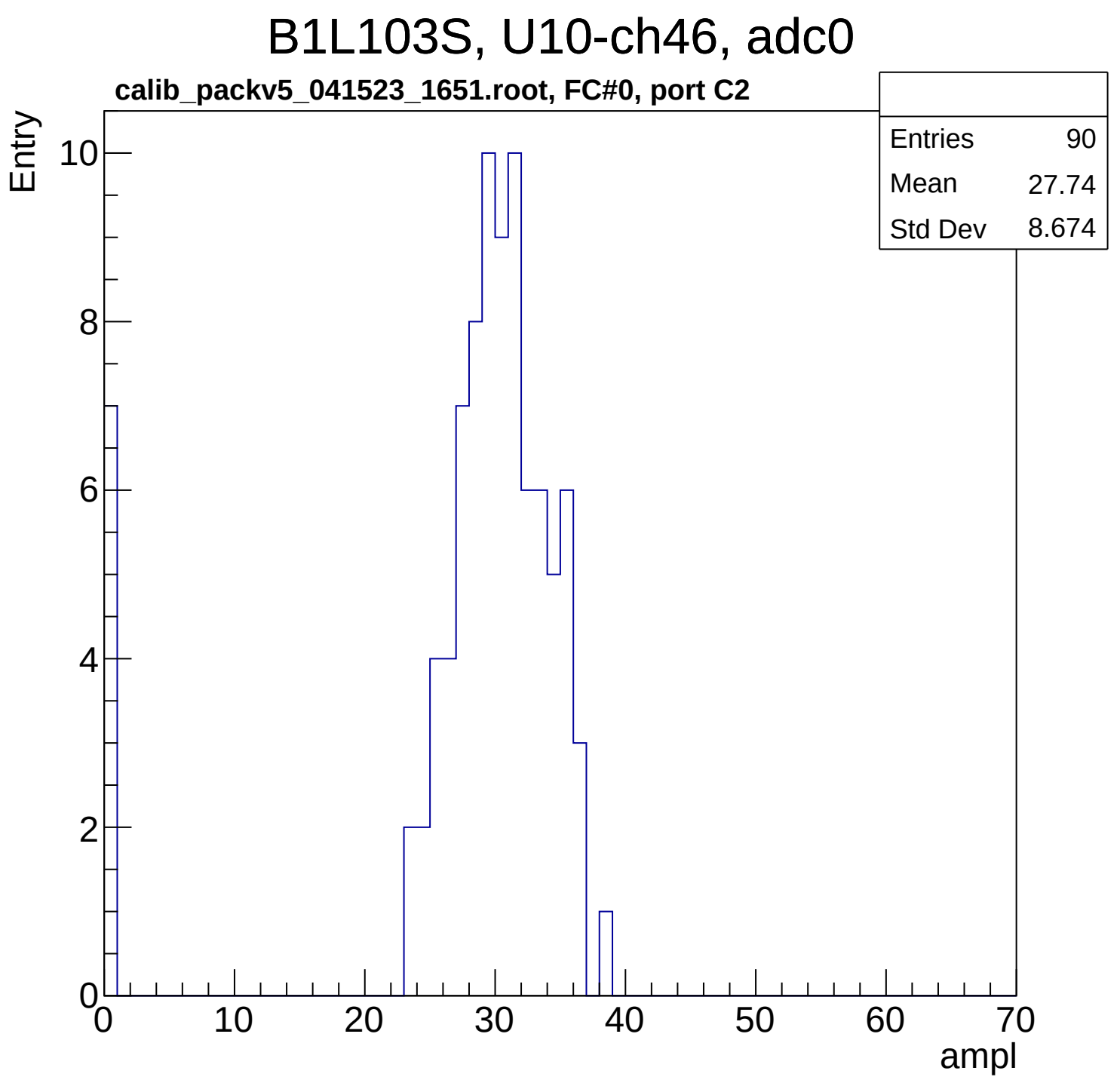
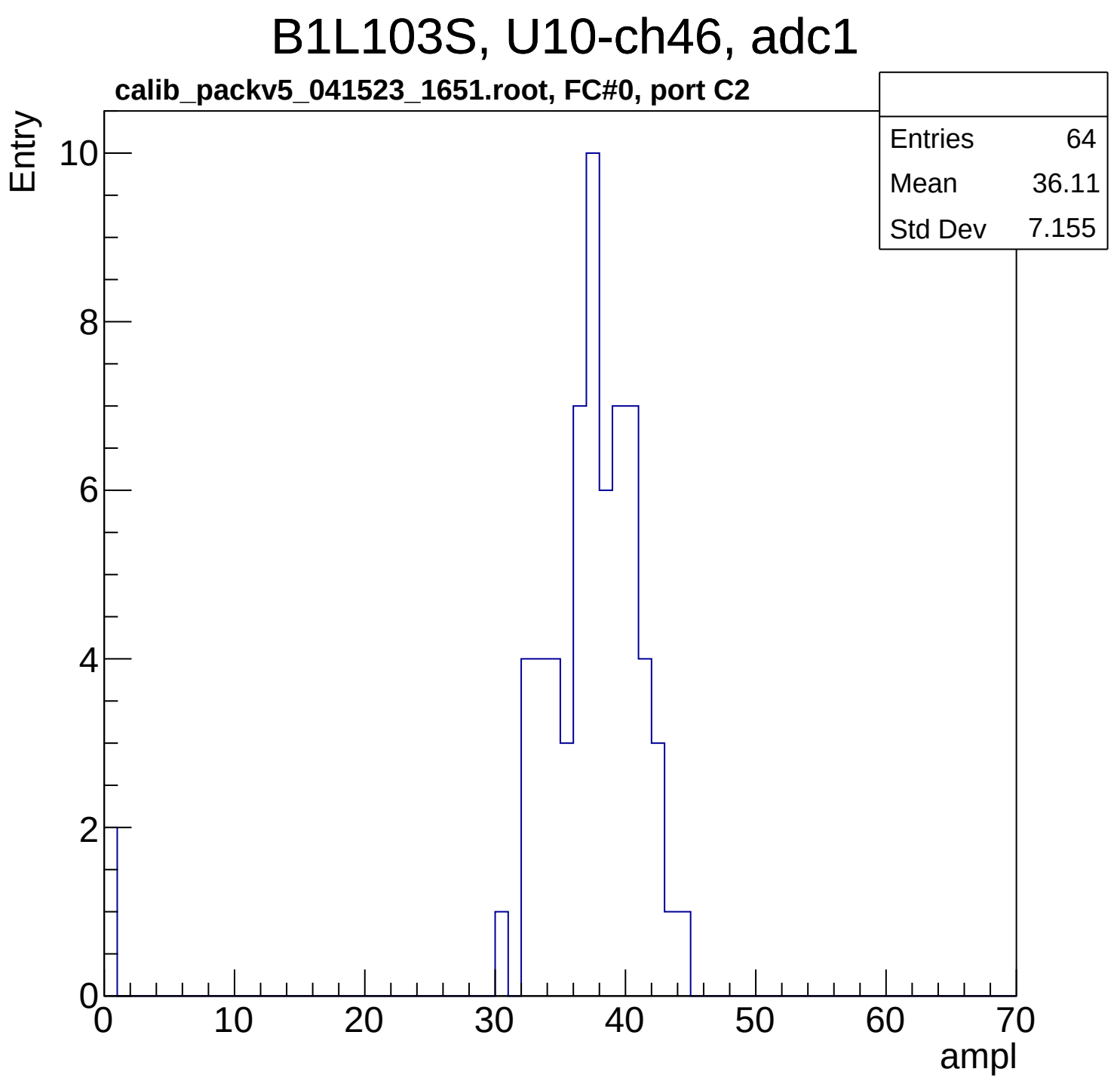
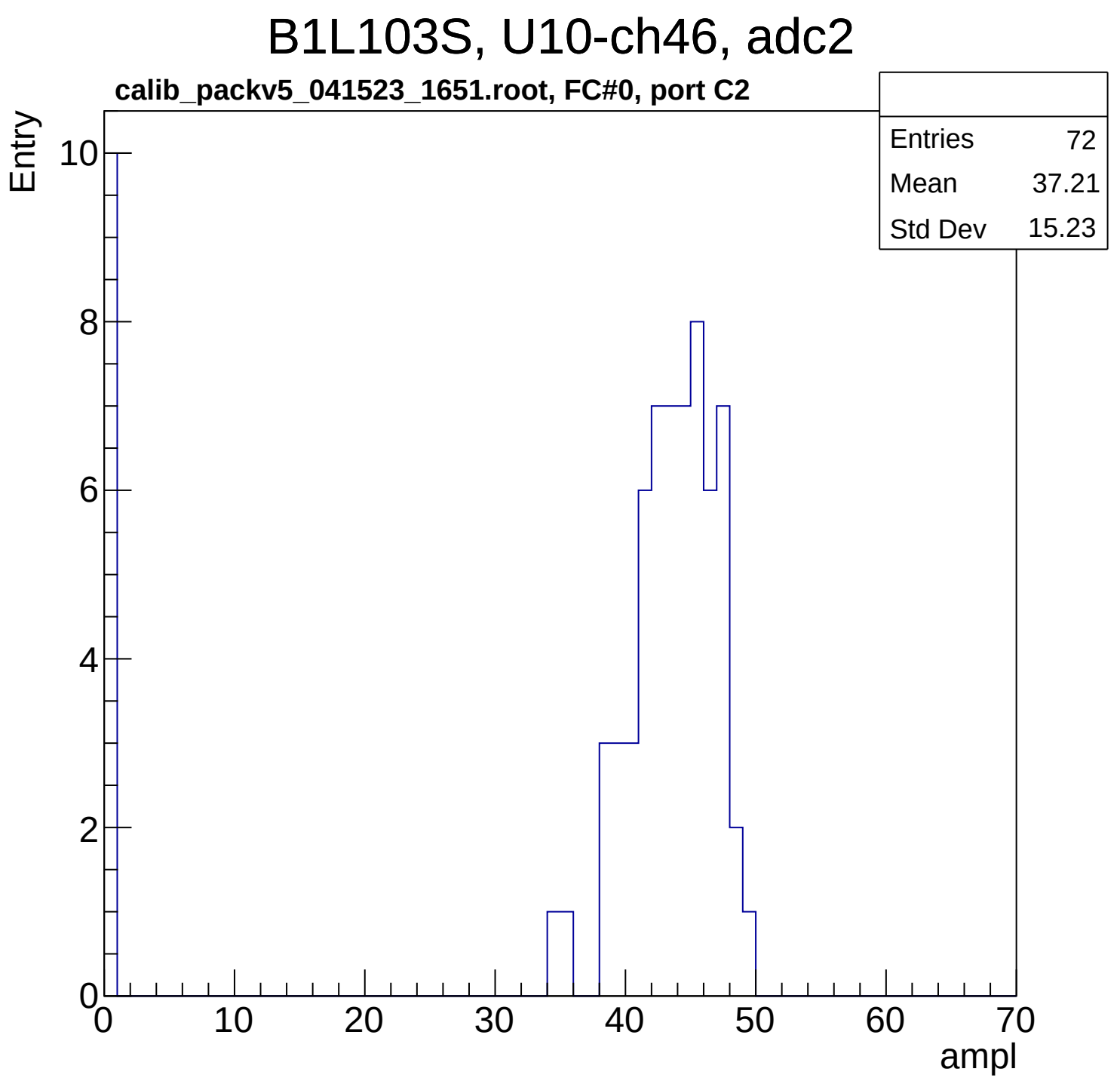
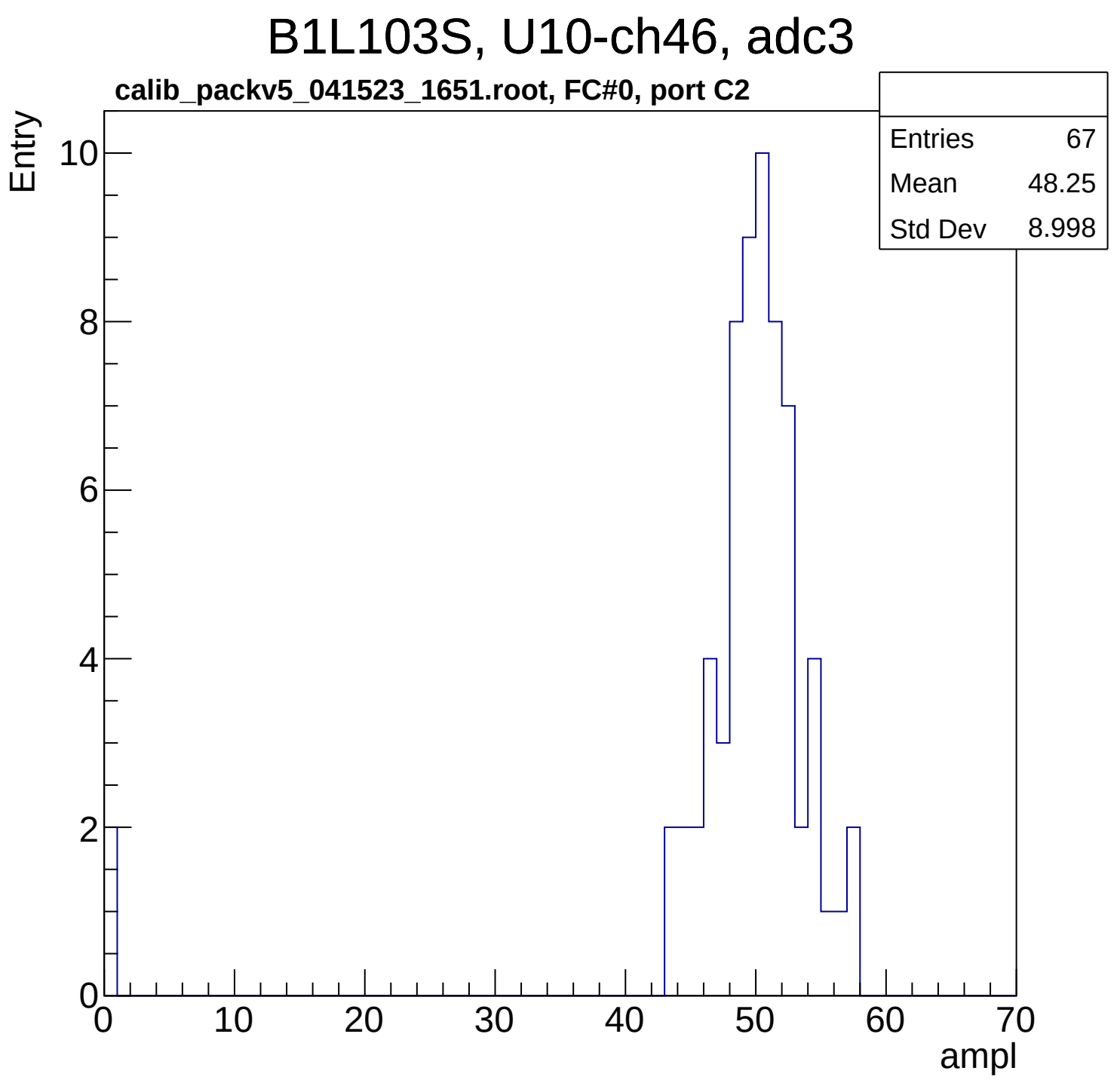
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

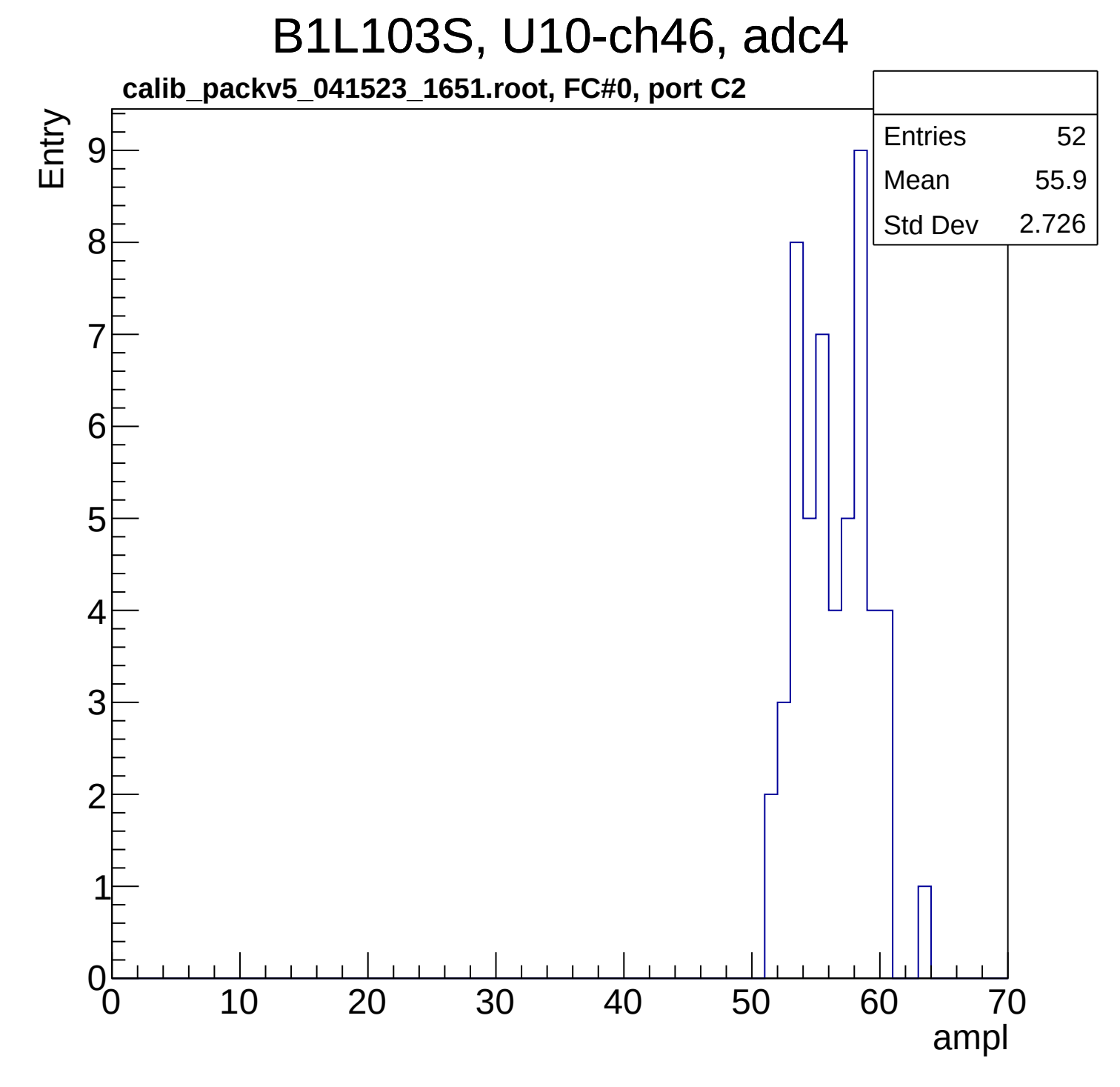

B1L103S, U10-ch45, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch46, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 90
Mean 27.74
Std Dev 8.674
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U10-ch46, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 36.11
Std Dev 7.155
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U10-ch46, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 37.21
Std Dev 15.23
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch46, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 48.25
Std Dev 8.998
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U10-ch46, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 55.9
Std Dev 2.726
Entry
ampl
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2
3
4
5
6
7
8
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0
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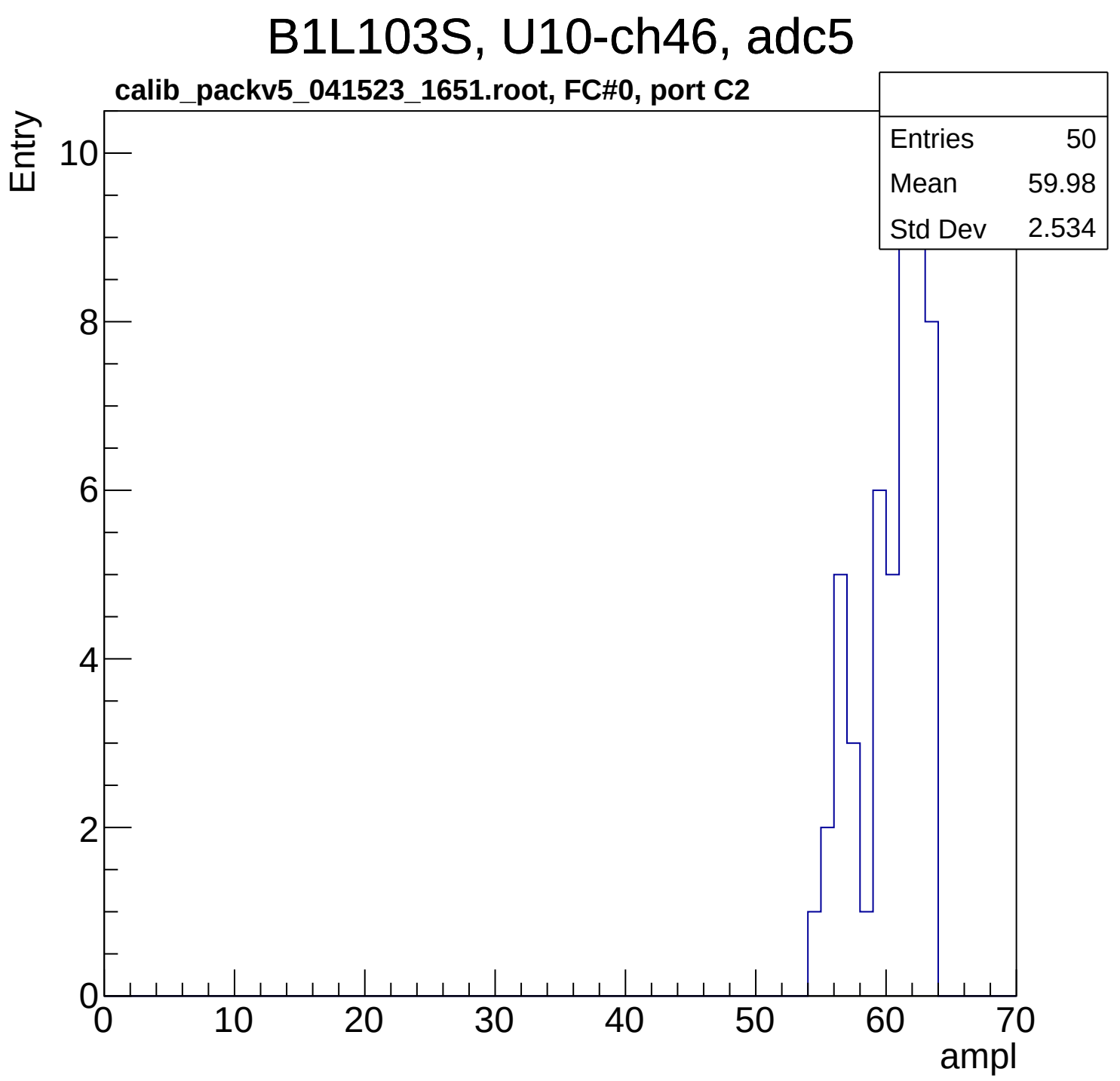
B1L103S, U10-ch46, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 59.98
Std Dev 2.534
Entry
ampl
0
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8
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0
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20
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40
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60
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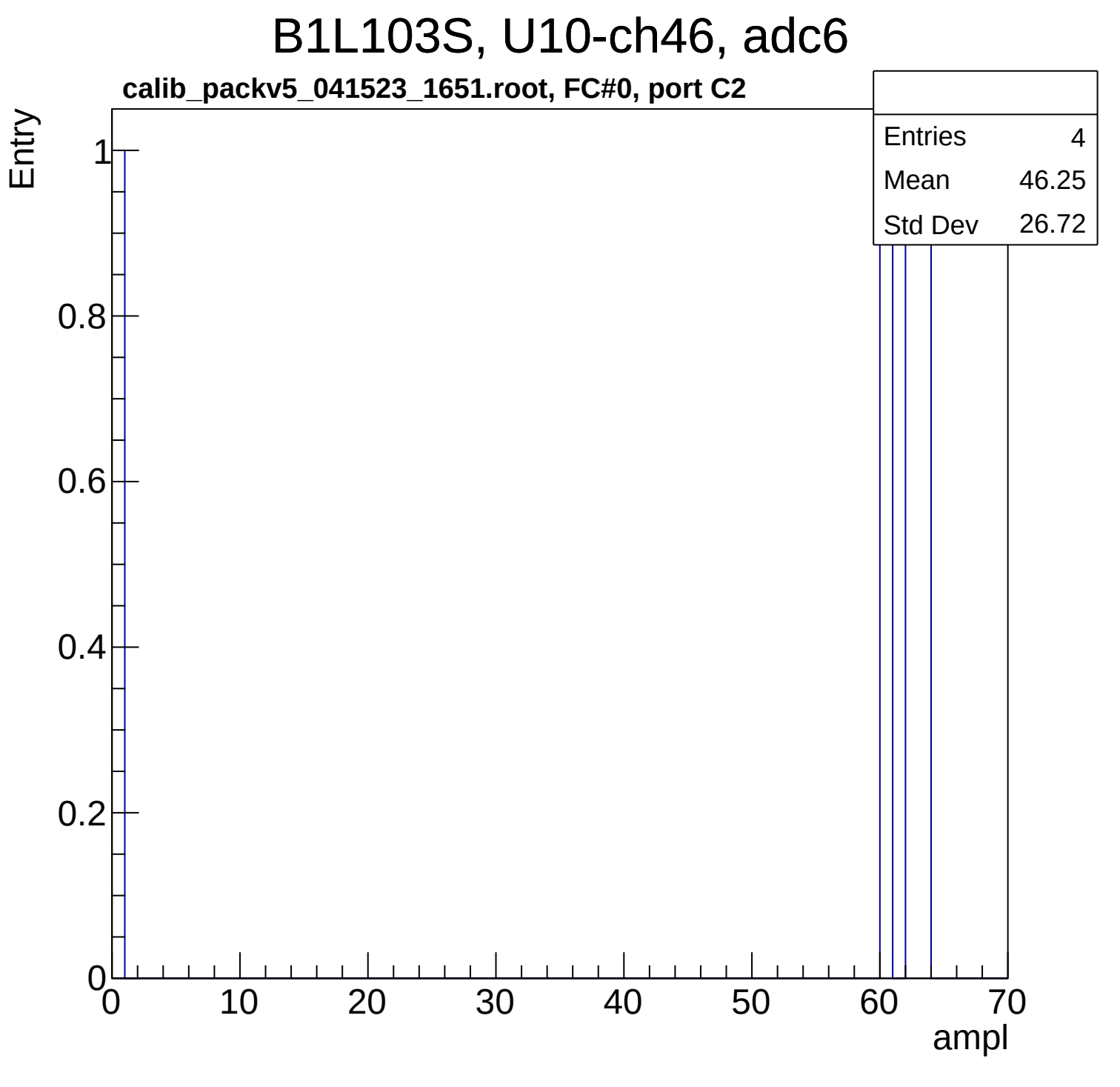
B1L103S, U10-ch46, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 4
Mean 46.25
Std Dev 26.72
Entry
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0.6
0.4
0.2
0
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10
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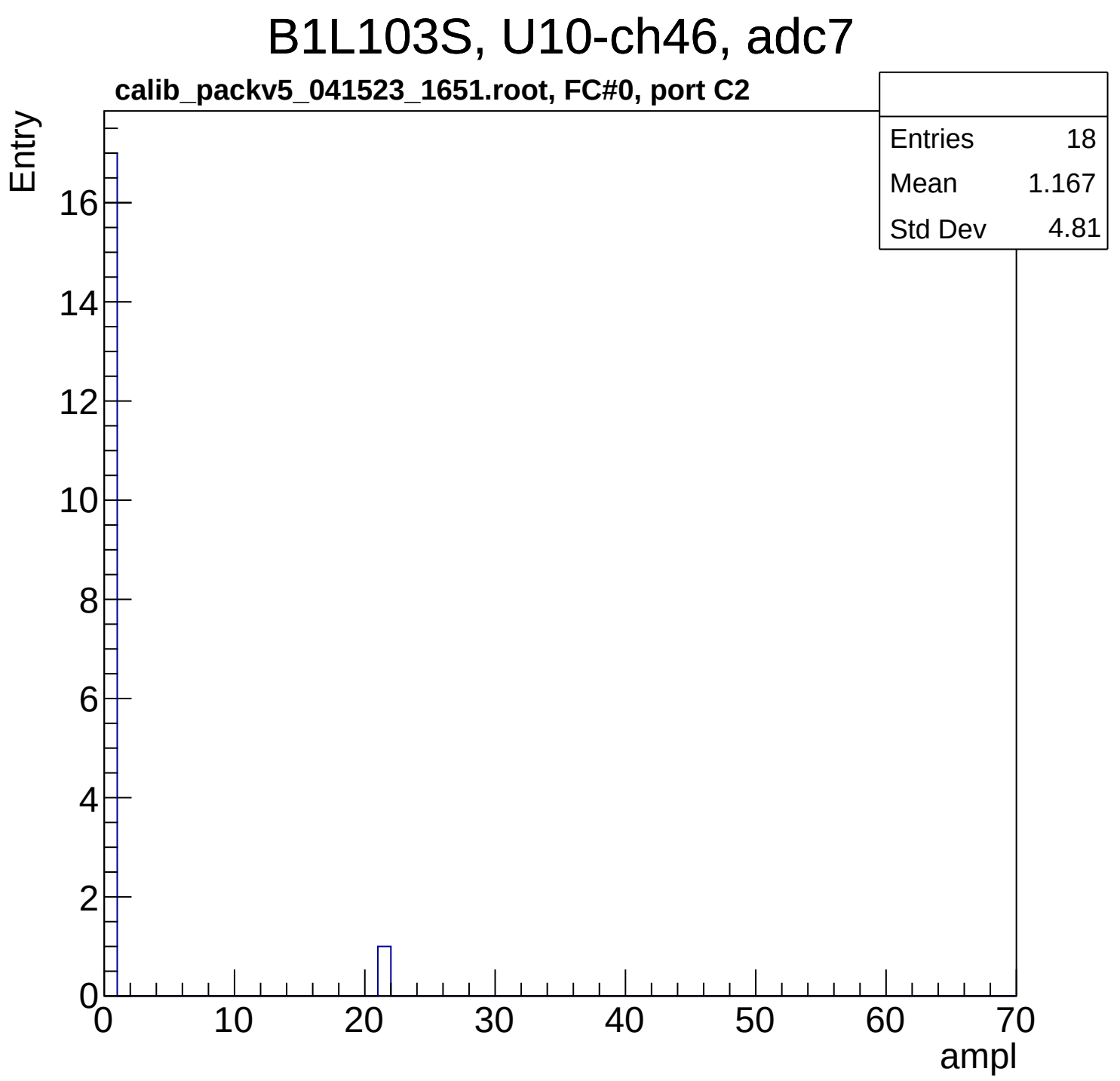
40
50
60
70
ampl


B1L103S, U10-ch46, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 1.167
Std Dev 4.81
Entry
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4
6
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10
12
14
16
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10
20
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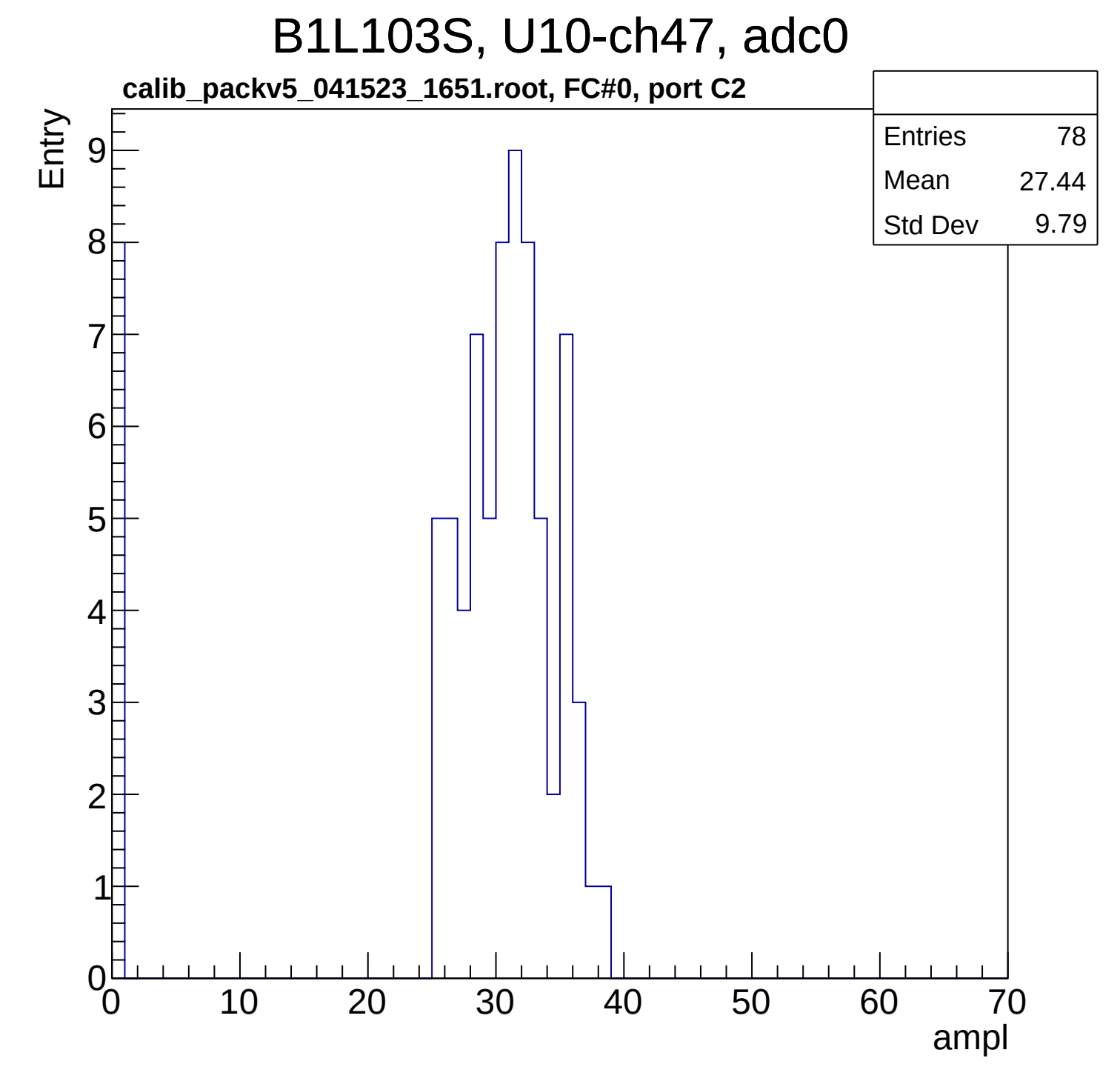
50
60
70
ampl


B1L103S, U10-ch47, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 27.44
Std Dev 9.79
Entry
ampl
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2
3
4
5
6
7
8
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0
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60
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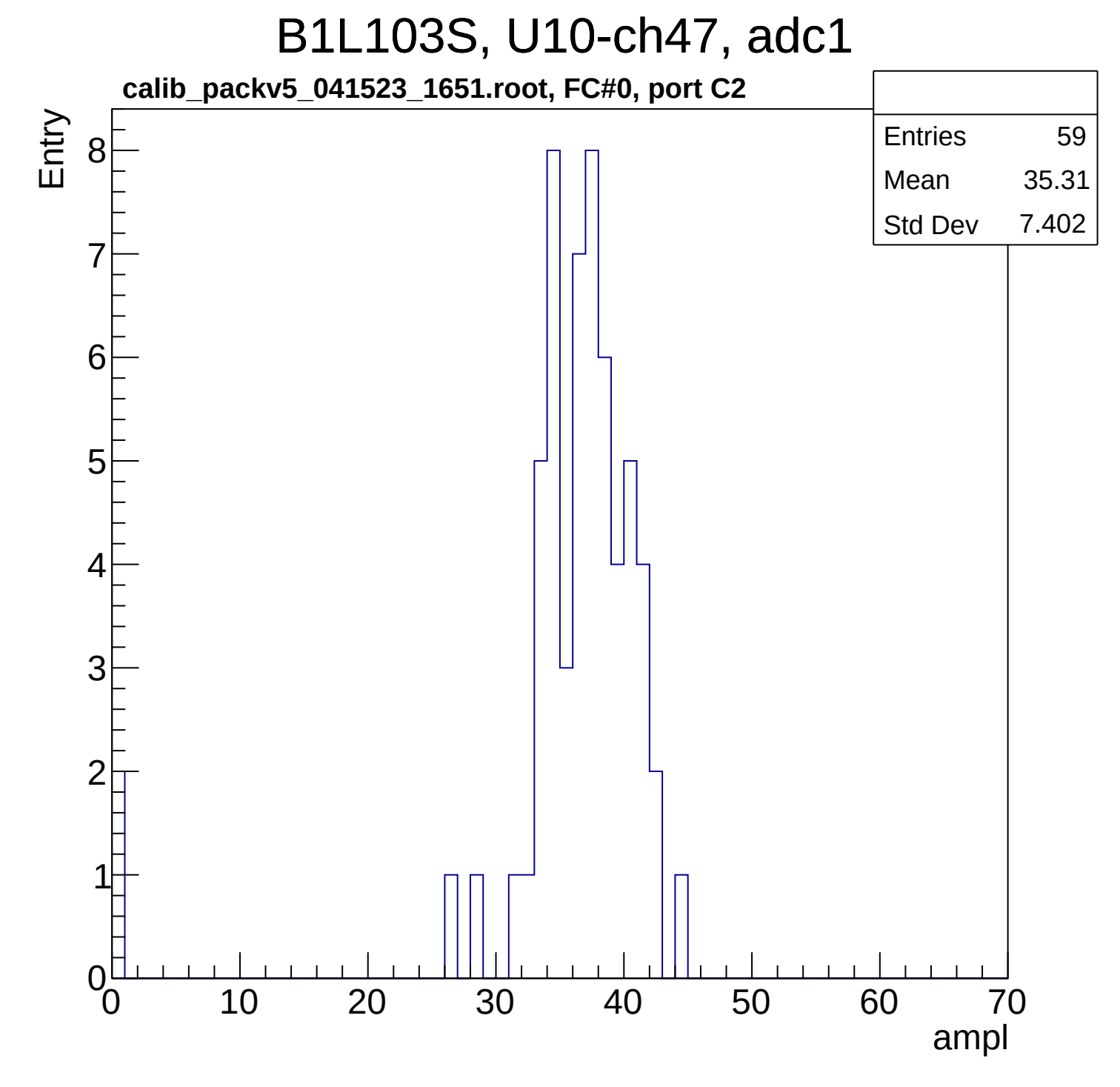
B1L103S, U10-ch47, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 35.31
Std Dev 7.402
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
30
40
50
60
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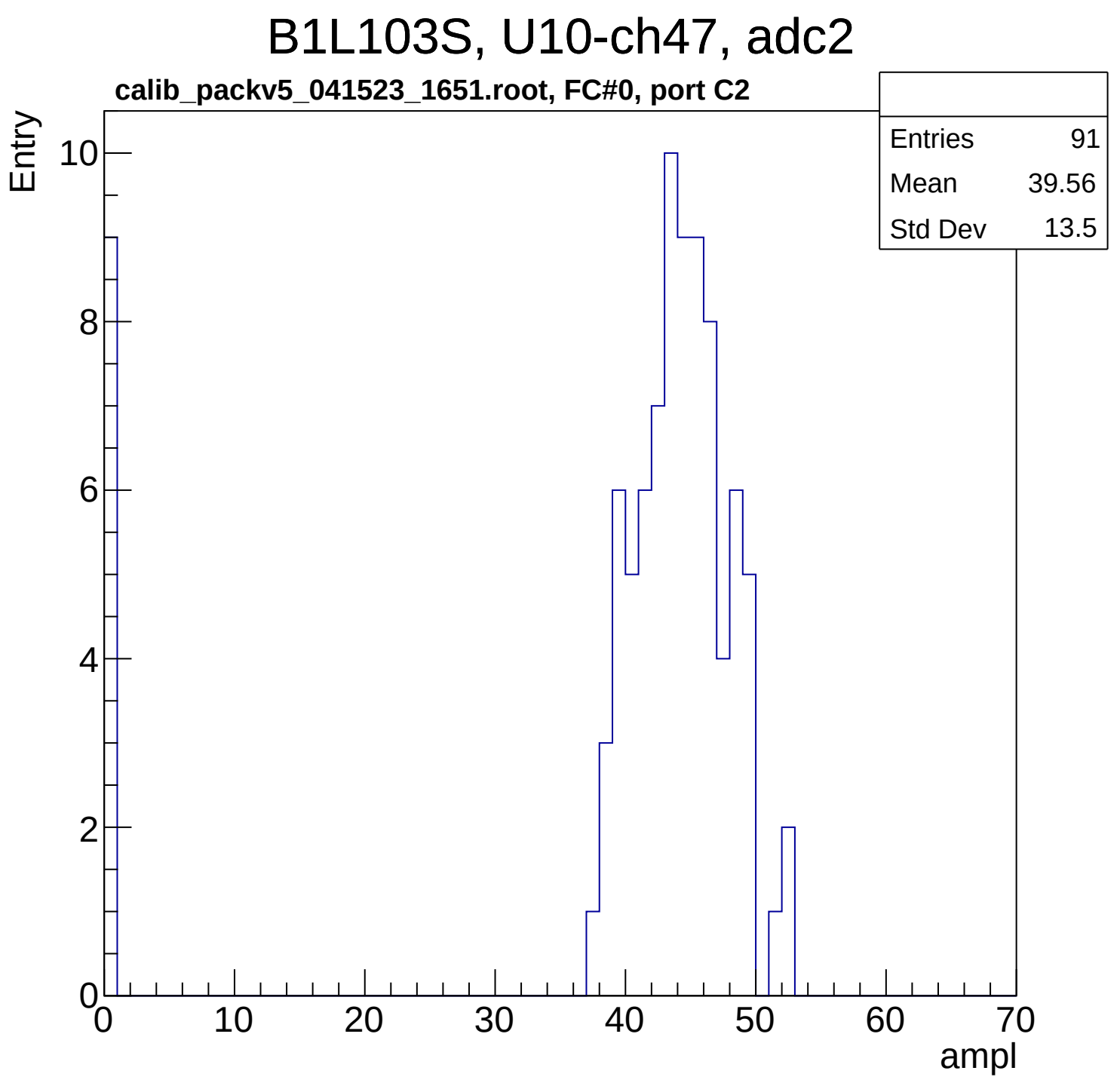
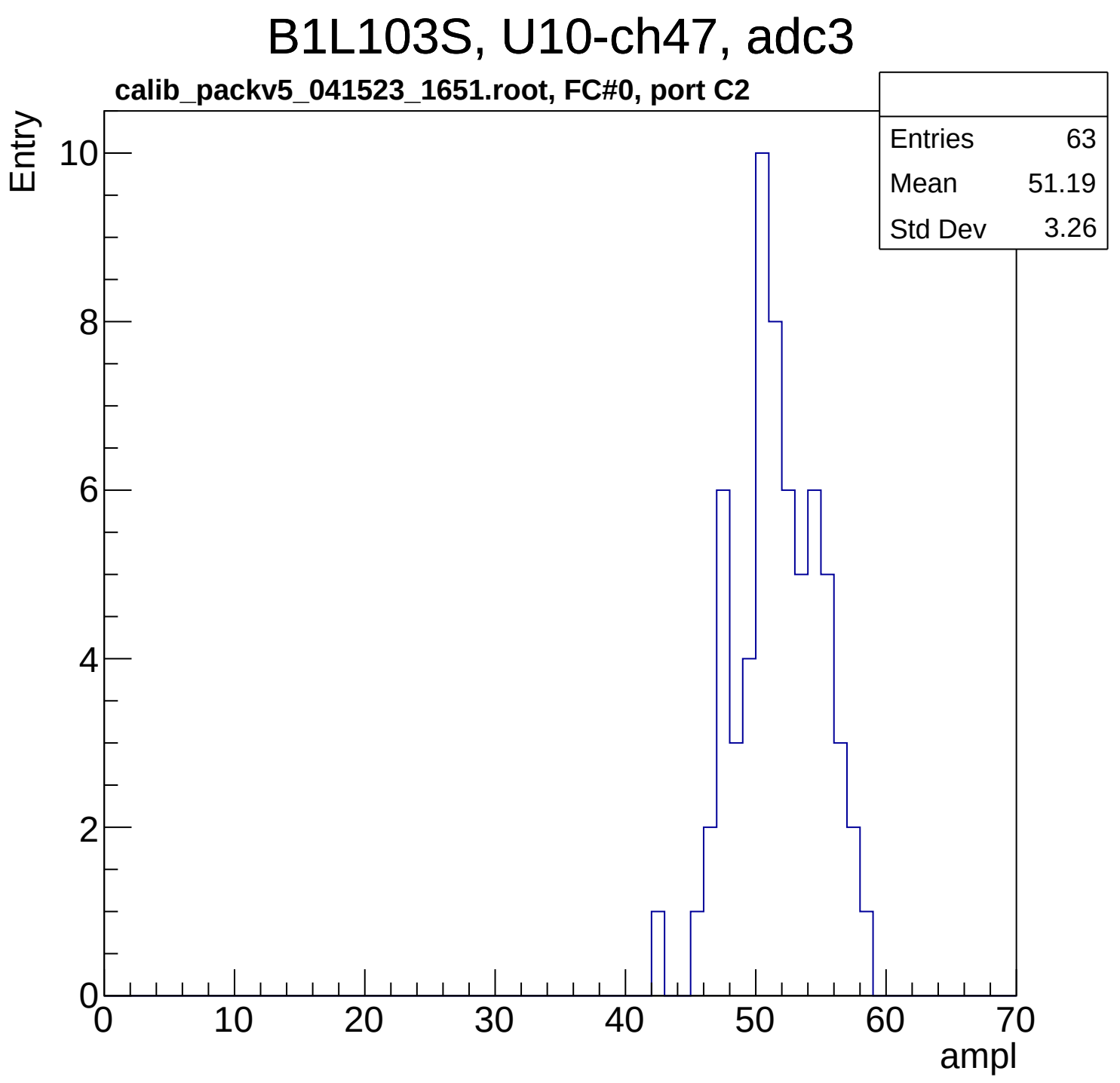
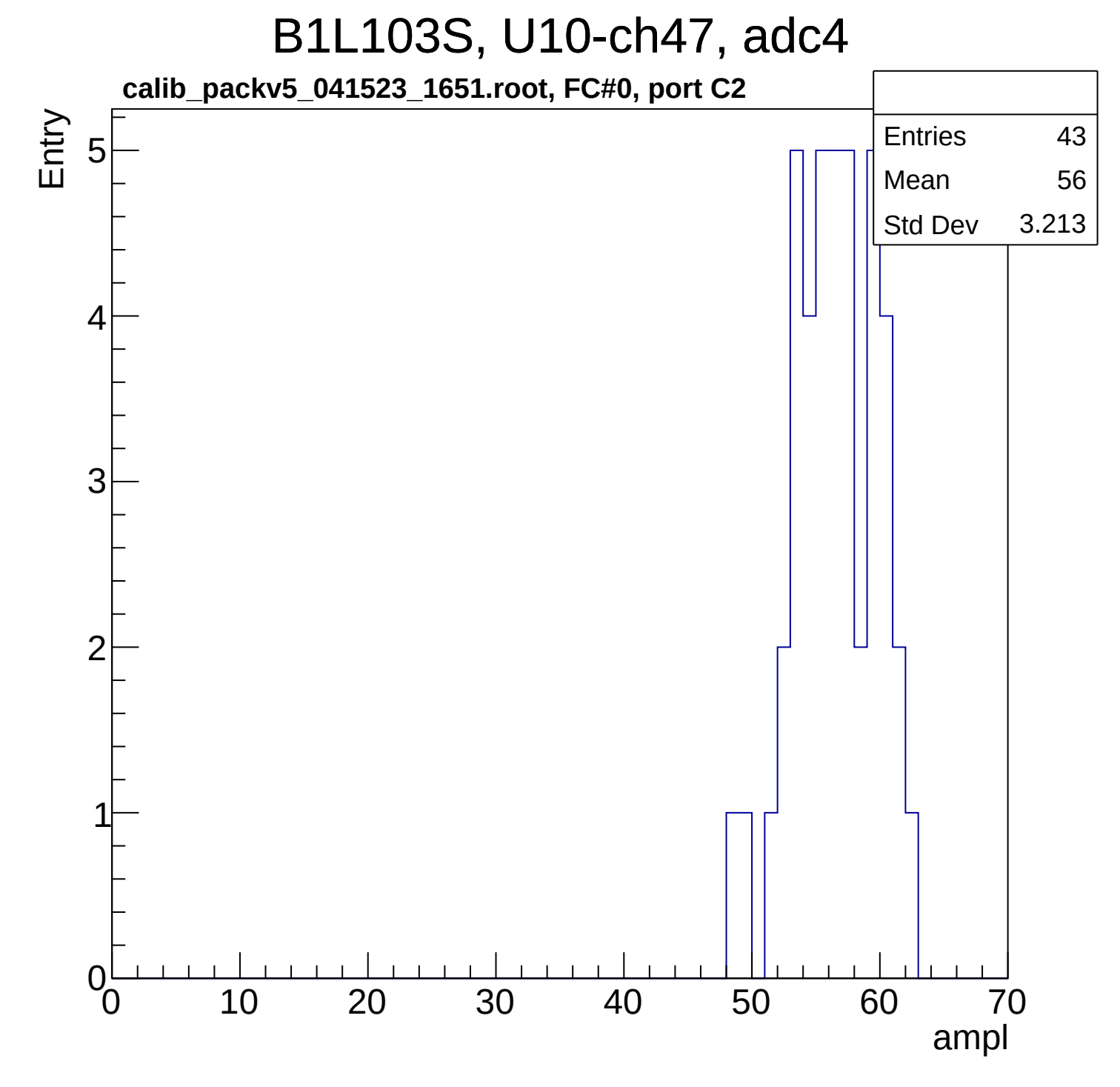
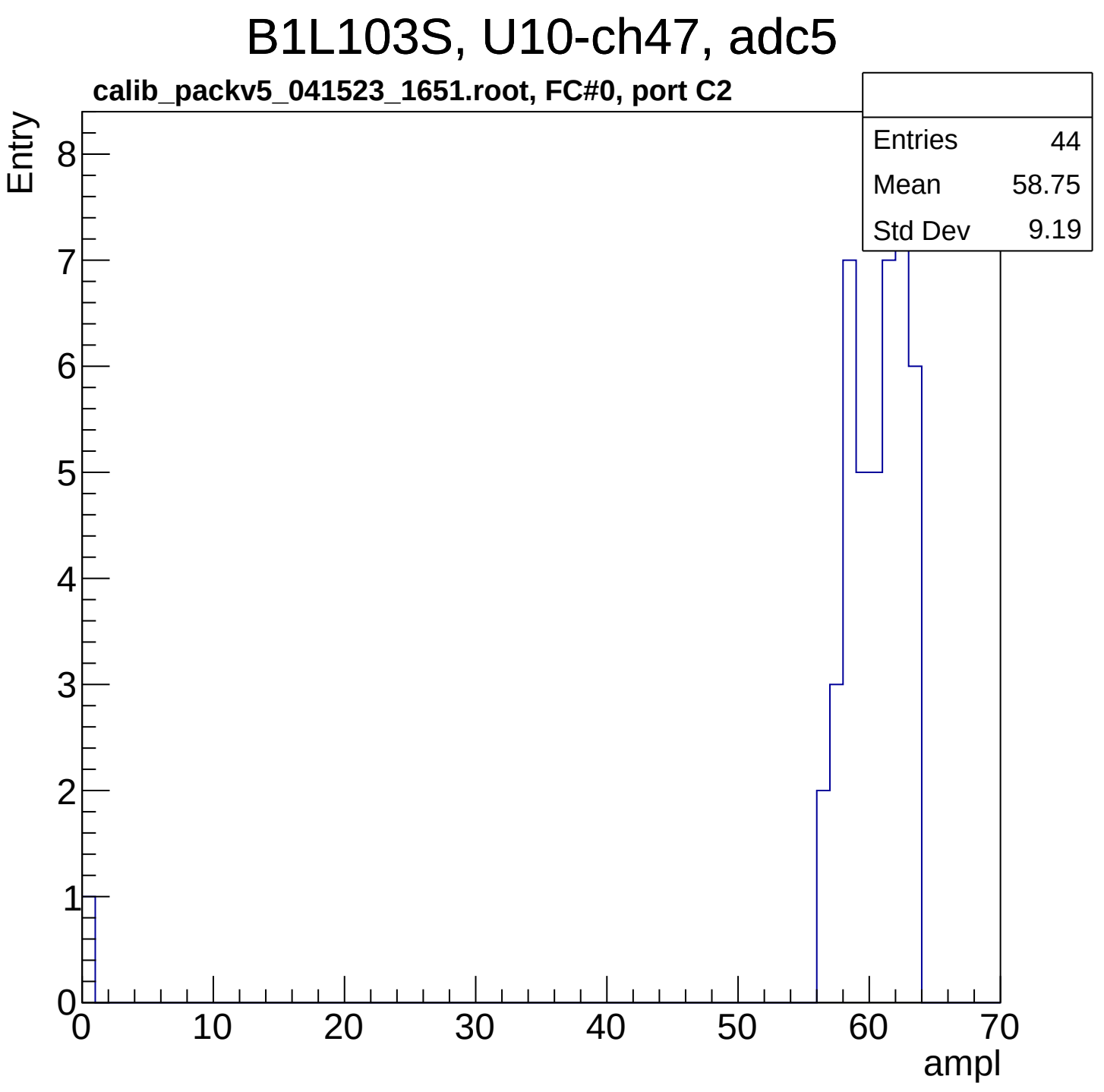

B1L103S, U10-ch47, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 91
Mean 39.56
Std Dev 13.5
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch47, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 51.19
Std Dev 3.26
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U10-ch47, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 43
Mean 56
Std Dev 3.213
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U10-ch47, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 58.75
Std Dev 9.19
Entry
ampl
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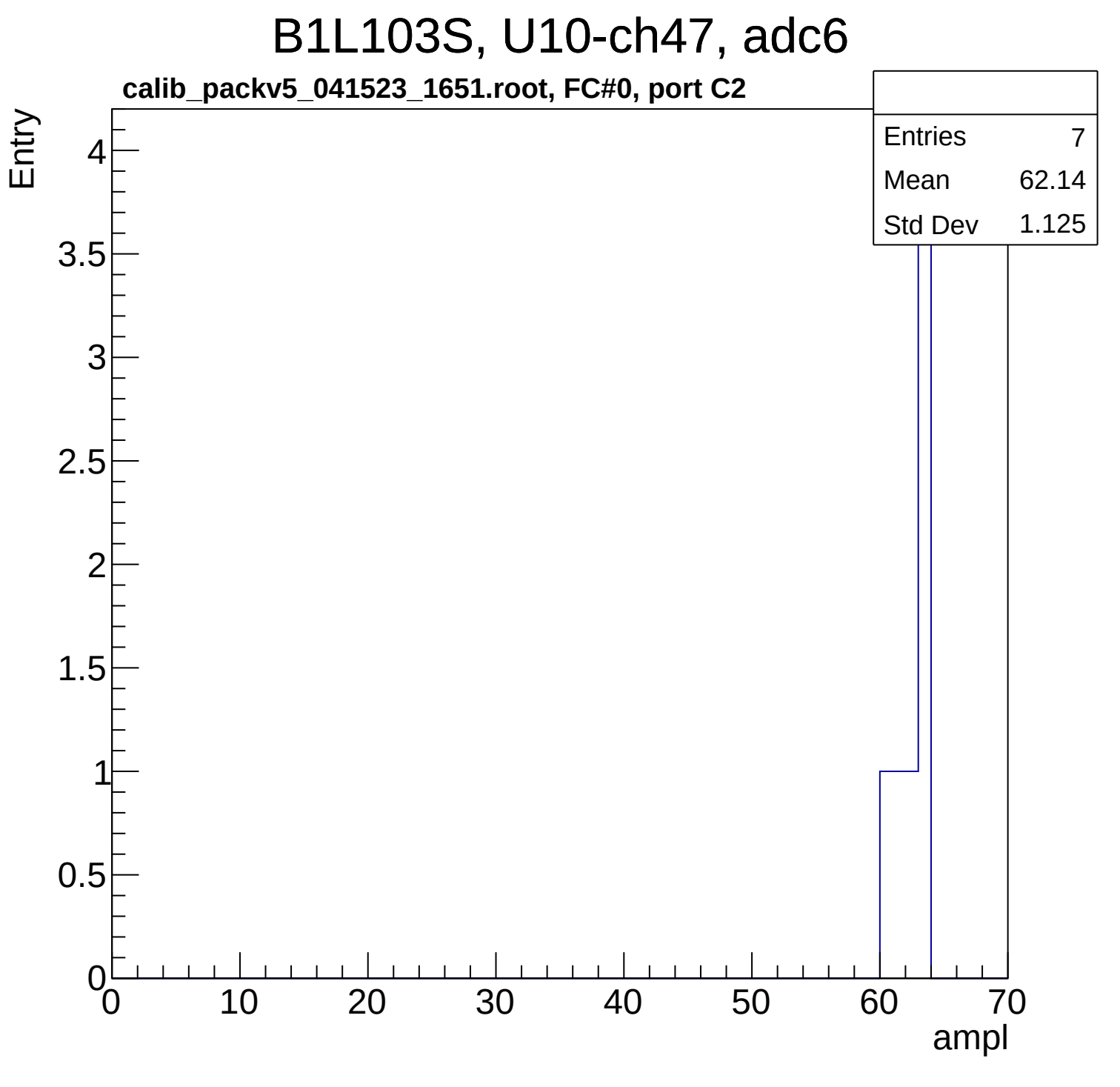
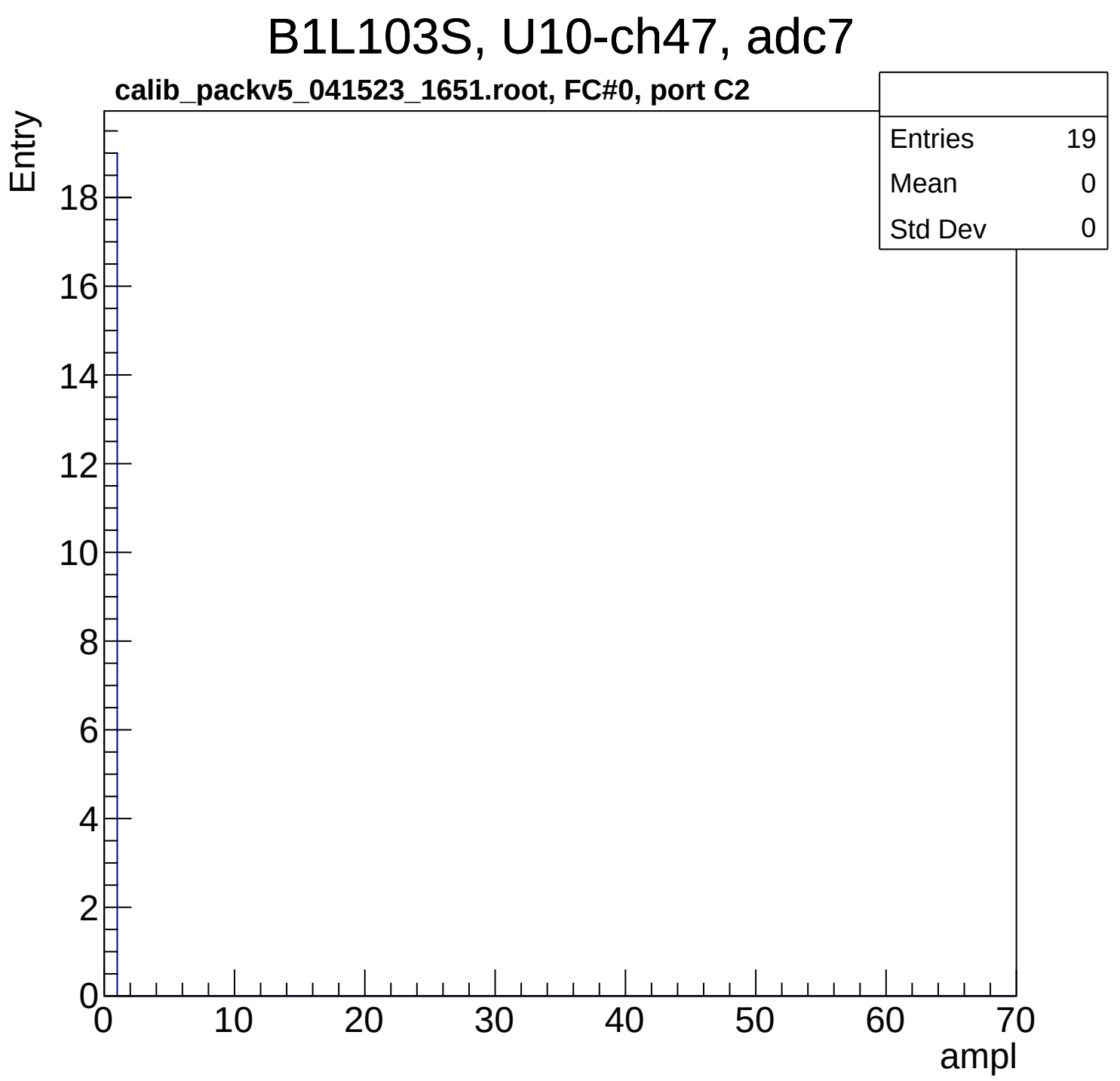
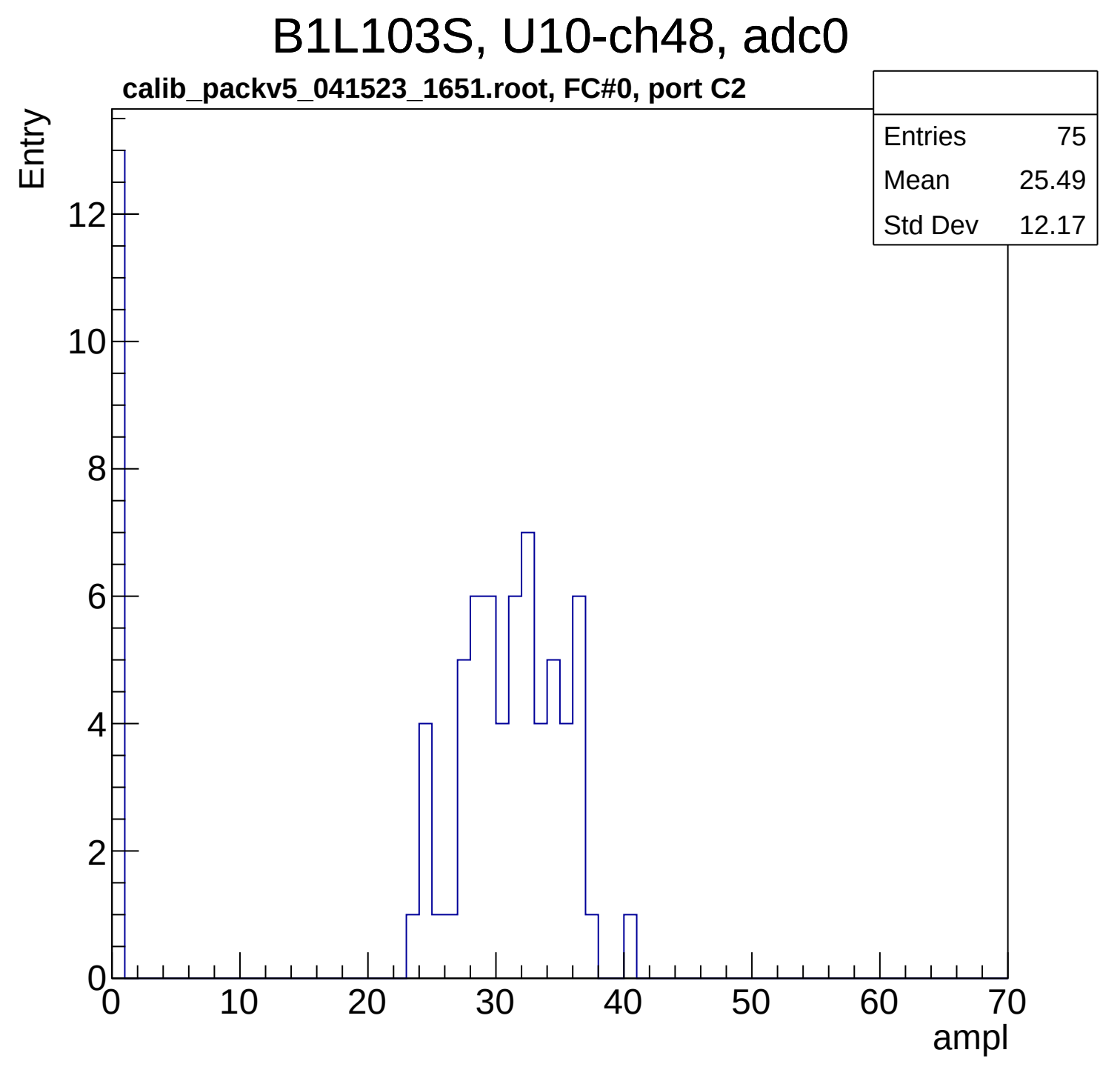
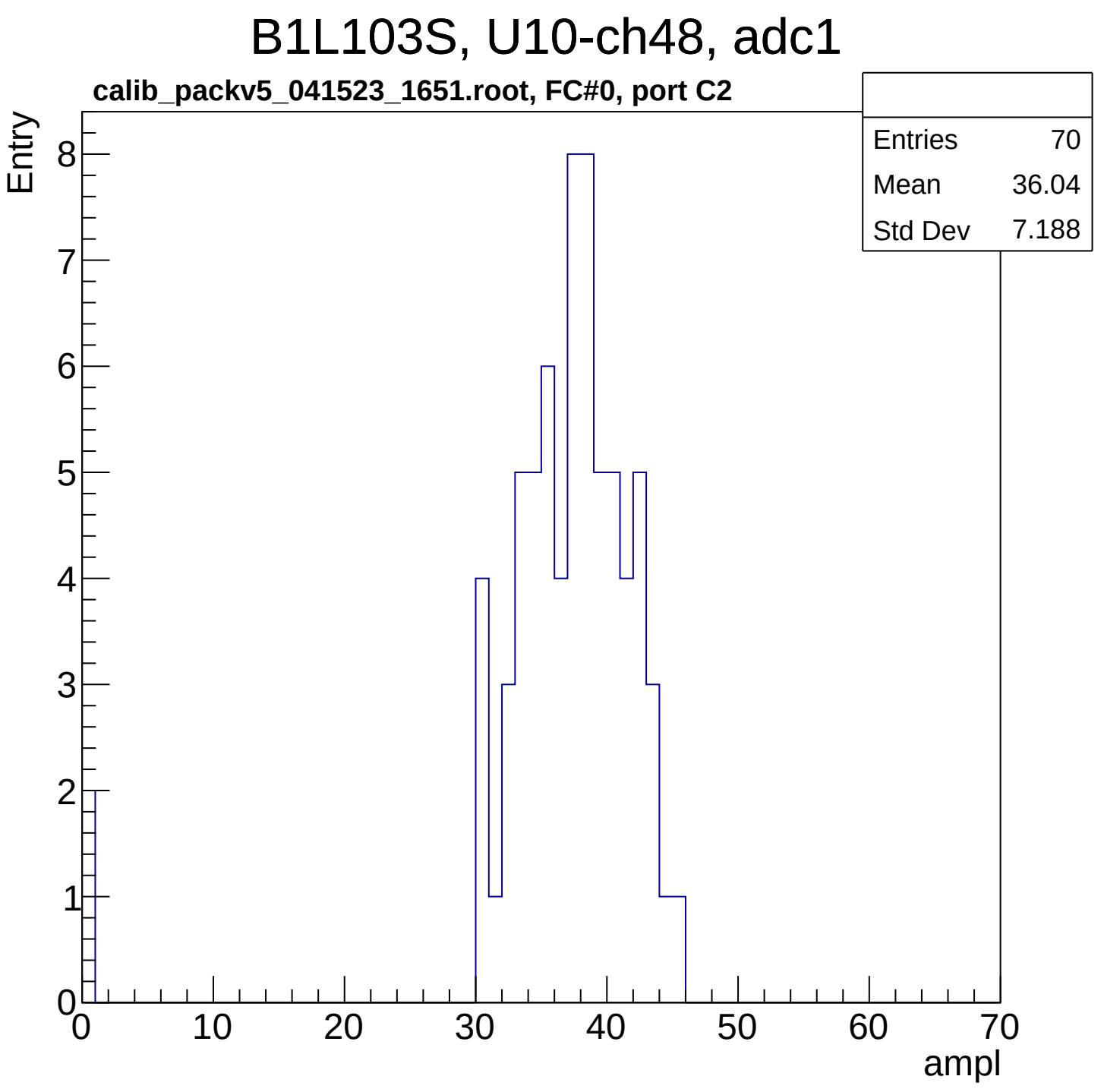
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U10-ch47, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 62.14
Std Dev 1.125
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U10-ch47, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch48, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 25.49
Std Dev 12.17
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch48, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 36.04
Std Dev 7.188
Entry
ampl
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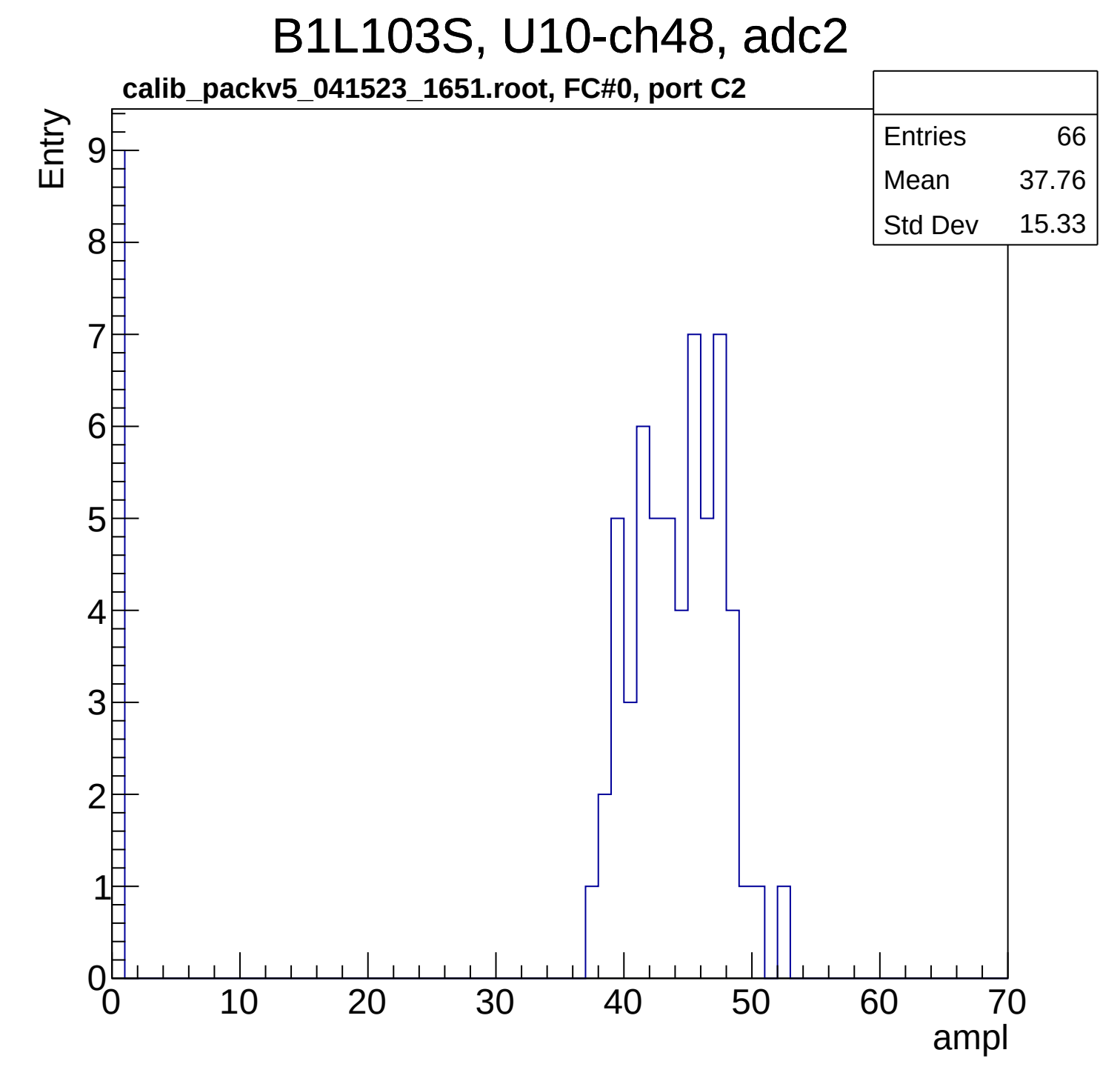
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U10-ch48, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 37.76
Std Dev 15.33
Entry
ampl
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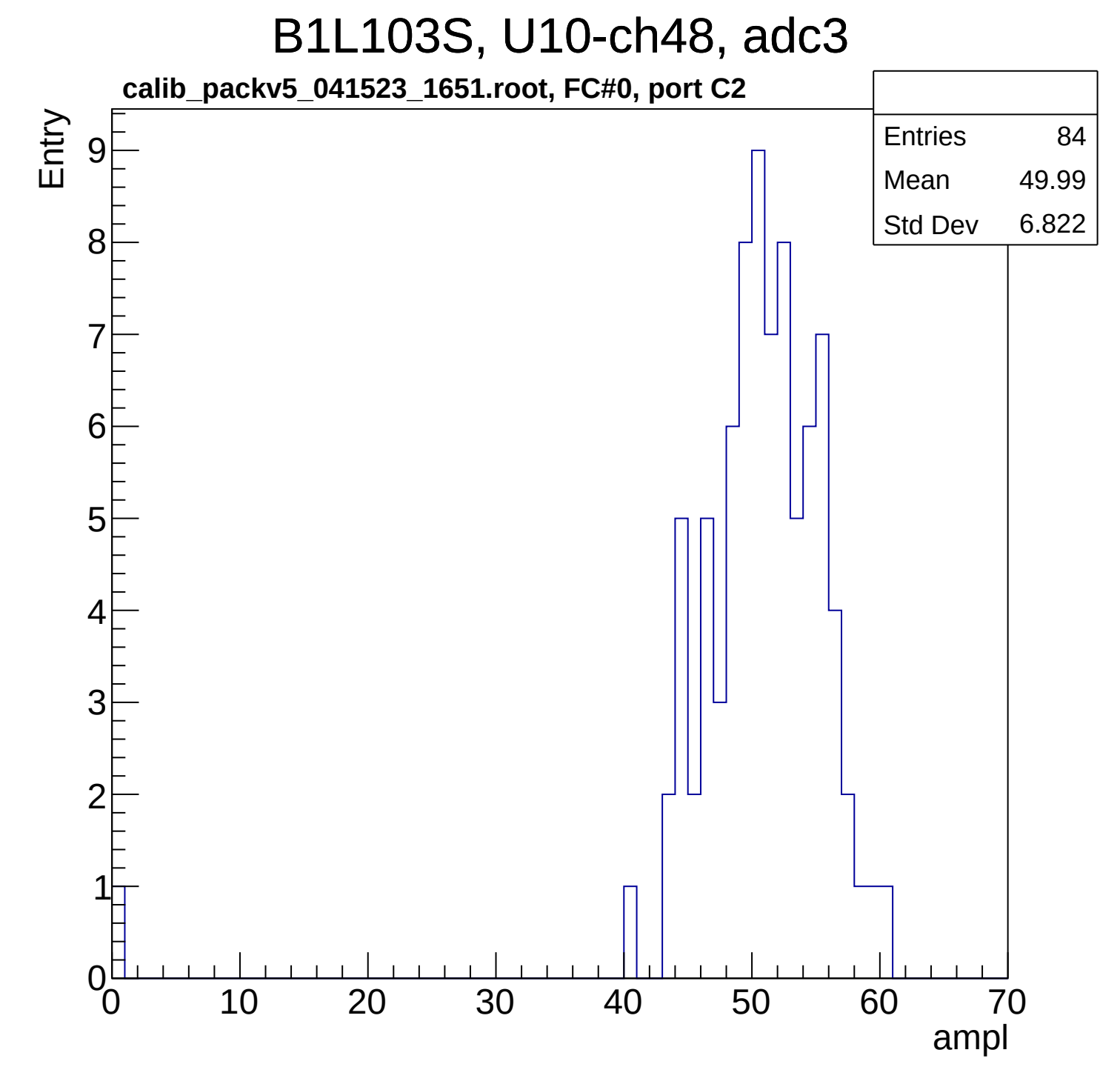
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U10-ch48, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 49.99
Std Dev 6.822
Entry
ampl
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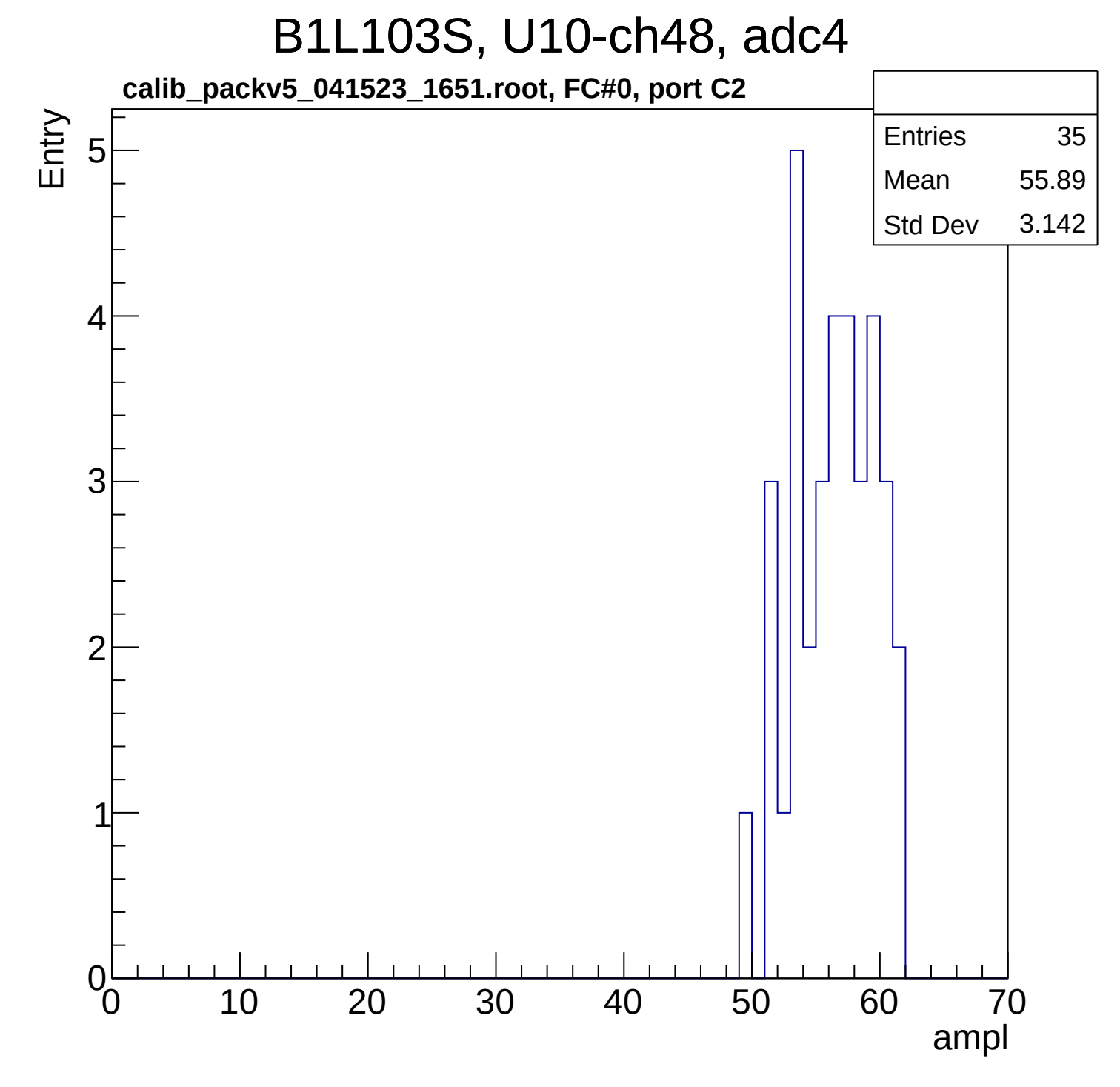
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9


B1L103S, U10-ch48, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 35
Mean 55.89
Std Dev 3.142
Entry
ampl
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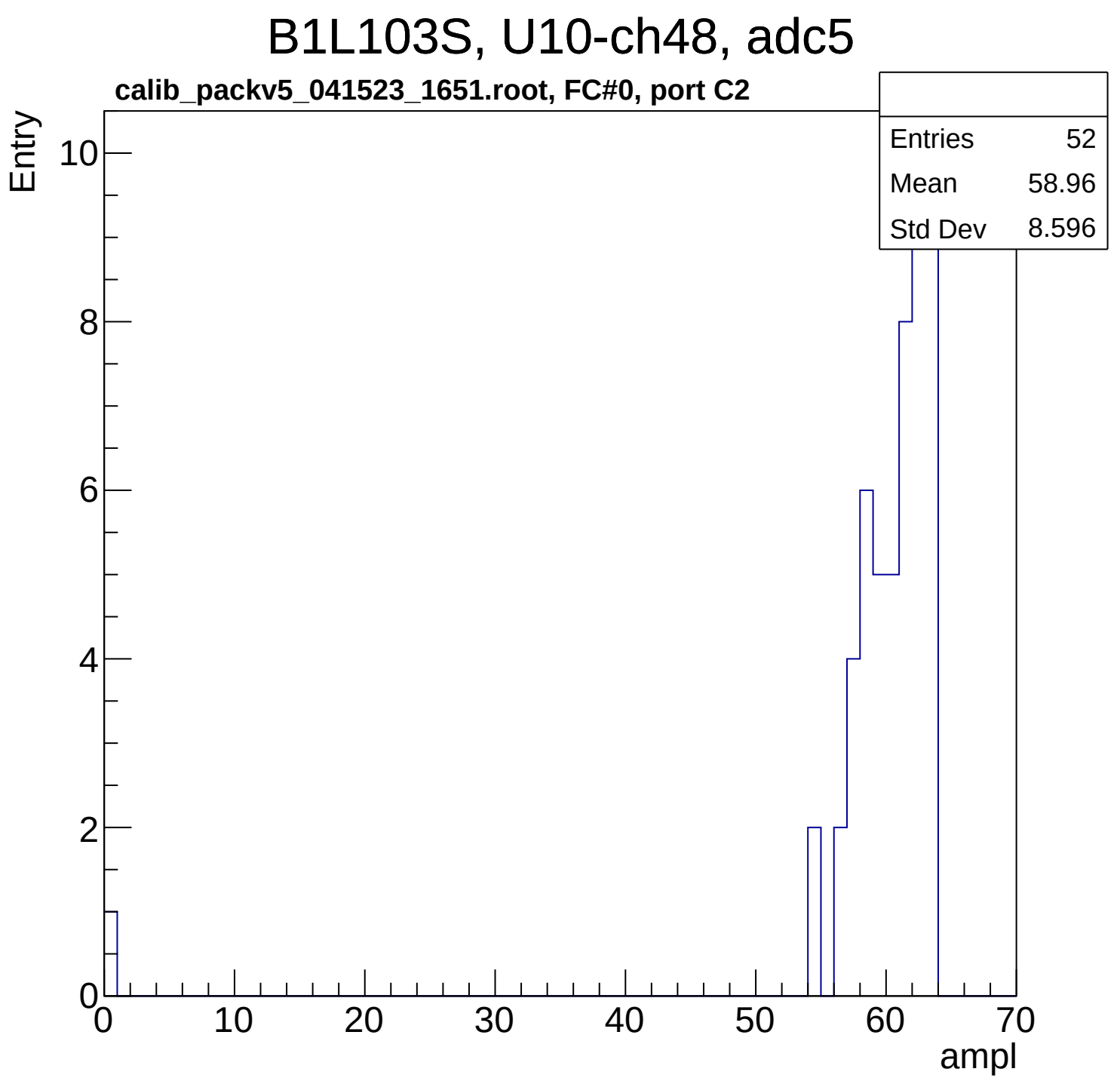
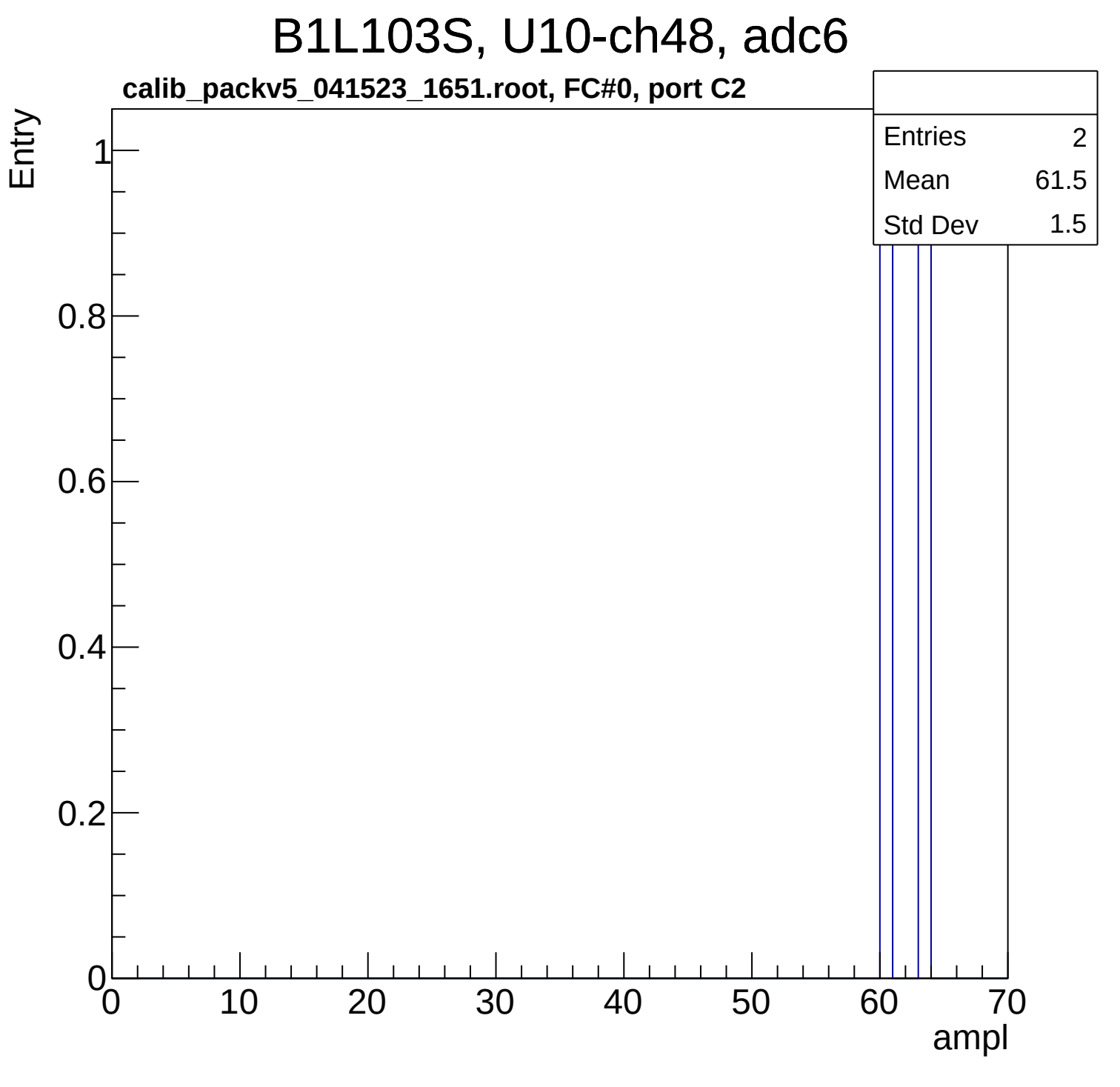
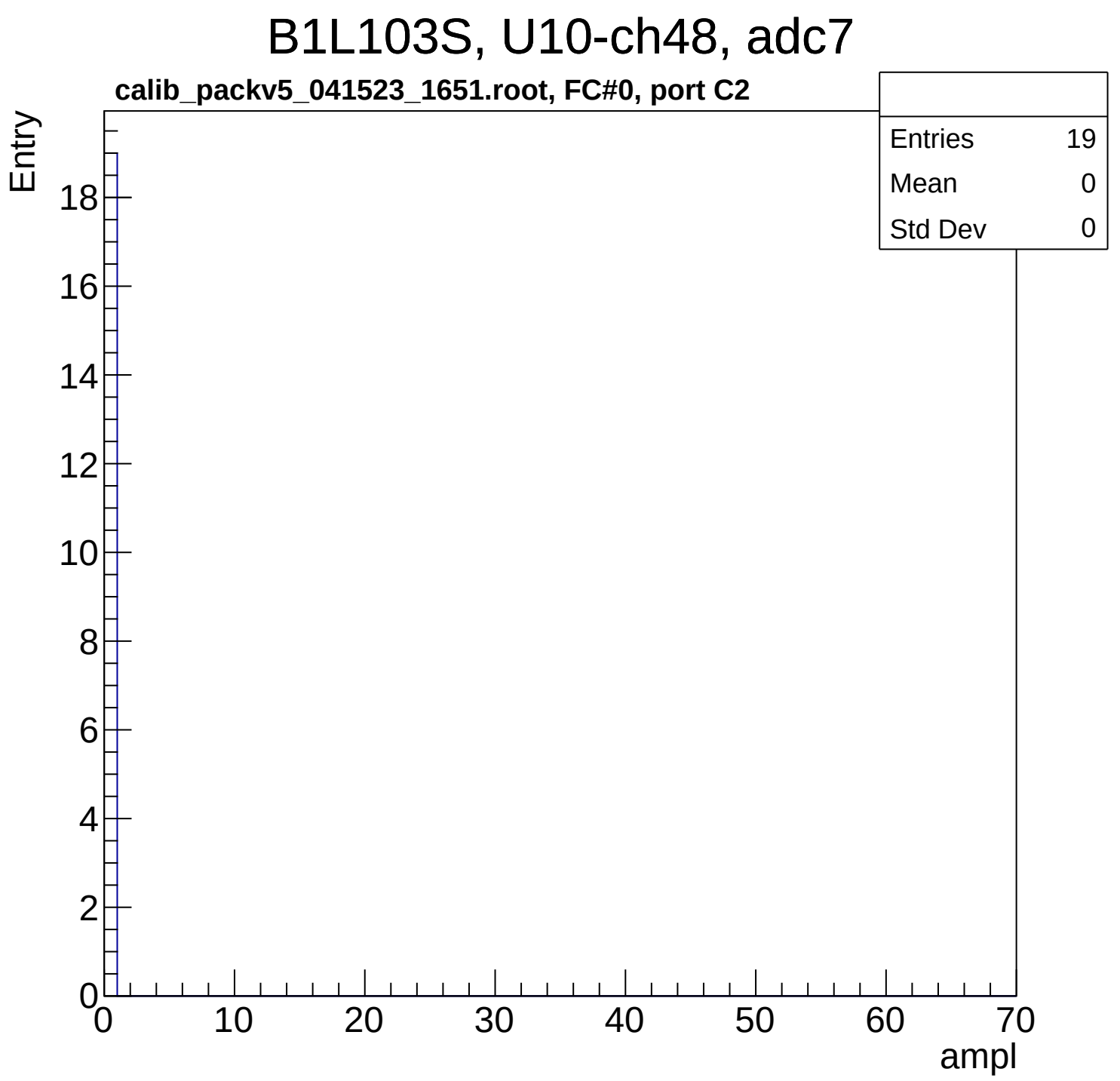
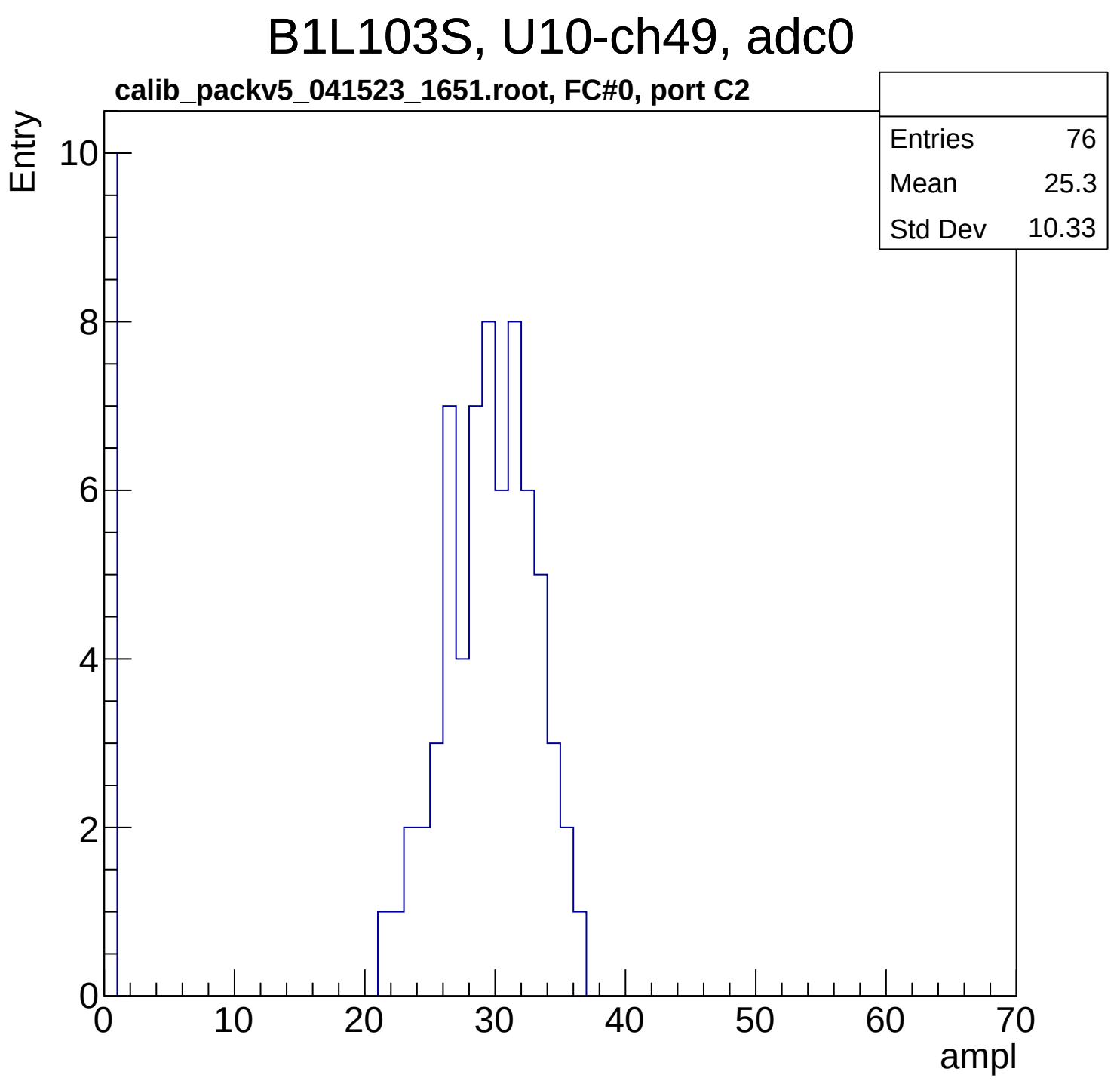
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U10-ch48, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 58.96
Std Dev 8.596
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U10-ch48, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 2
Mean 61.5
Std Dev 1.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch48, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch49, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 25.3
Std Dev 10.33
Entry
ampl
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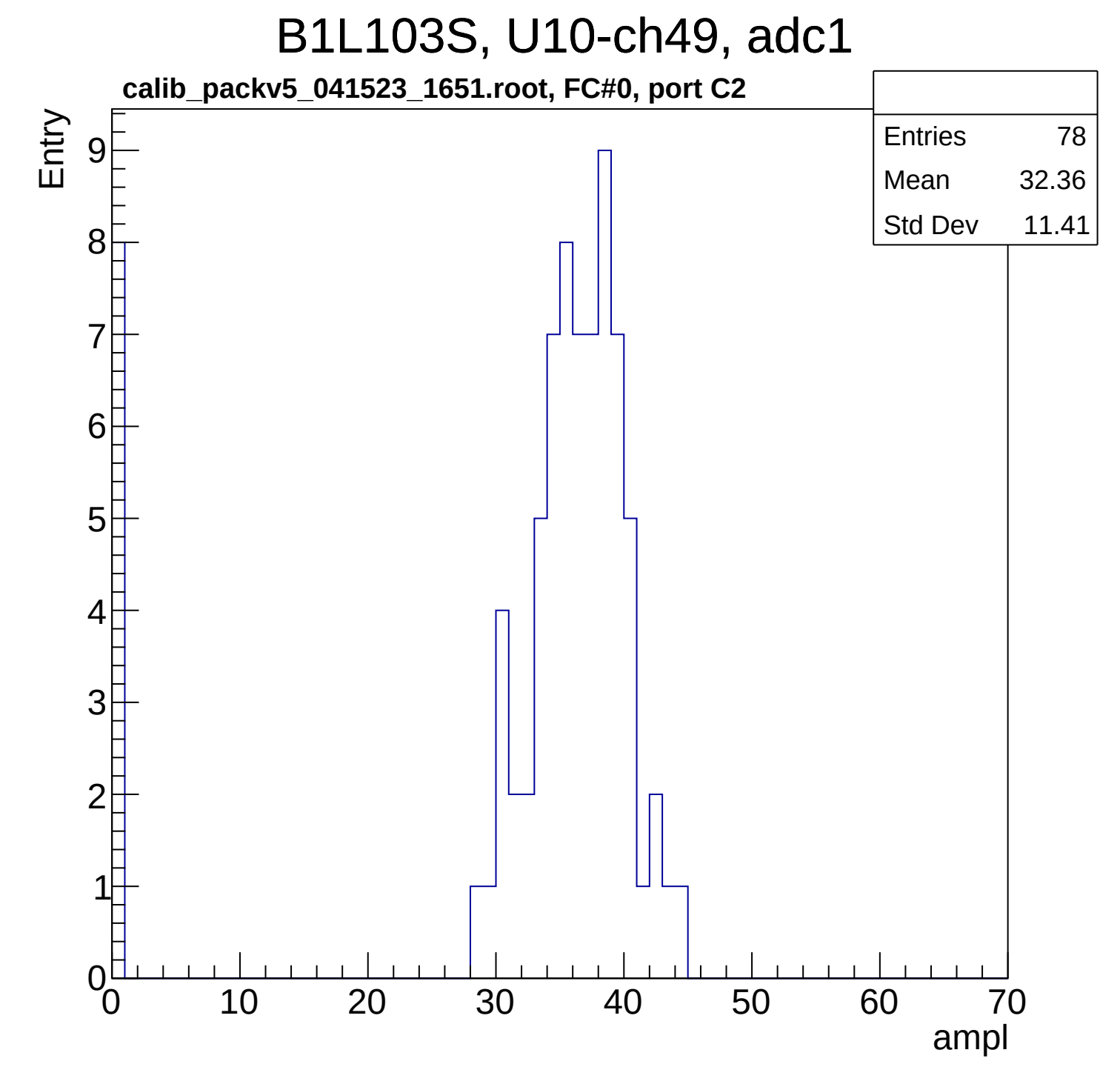
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U10-ch49, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 32.36
Std Dev 11.41
Entry
ampl
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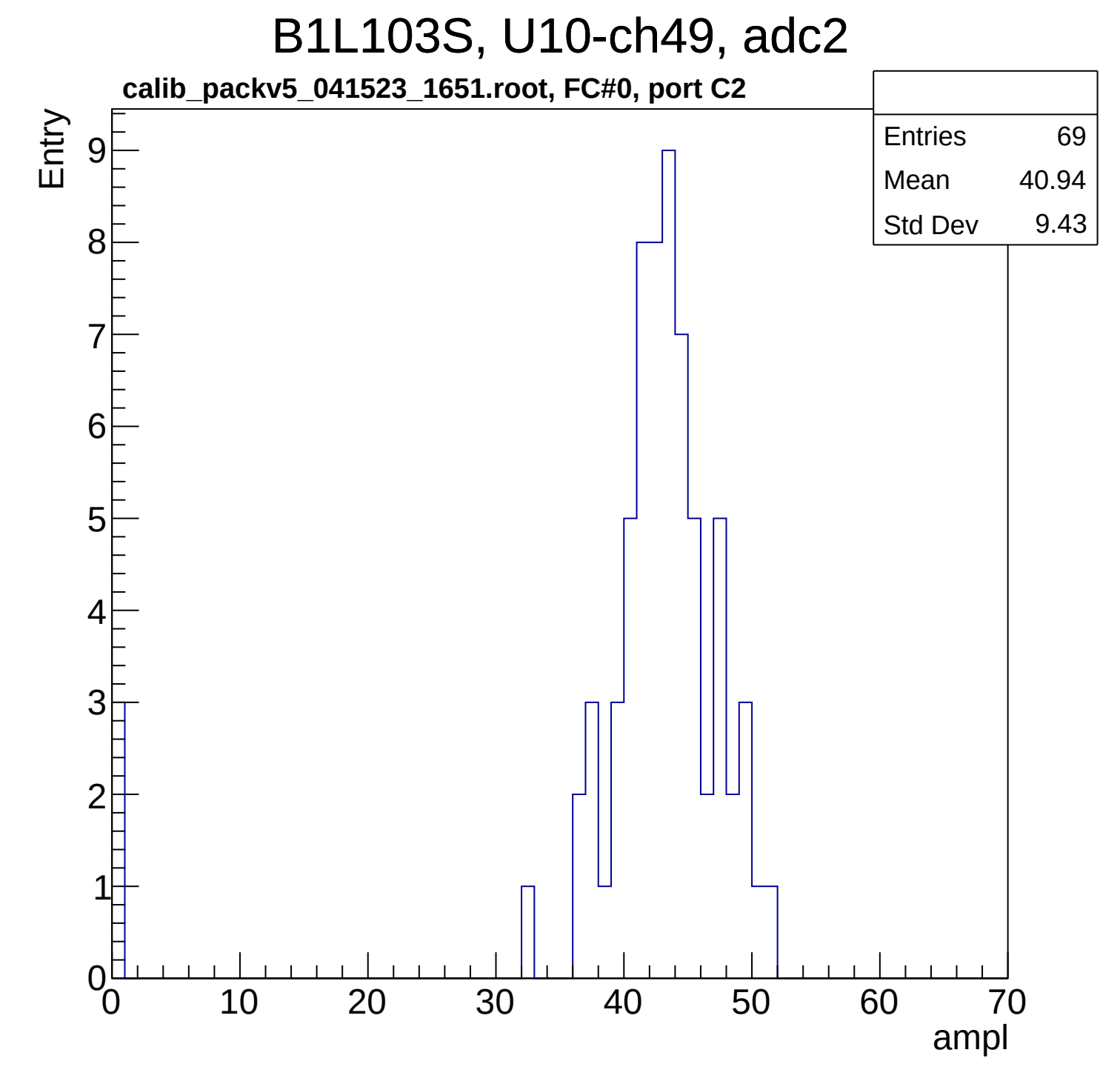
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U10-ch49, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 40.94
Std Dev 9.43
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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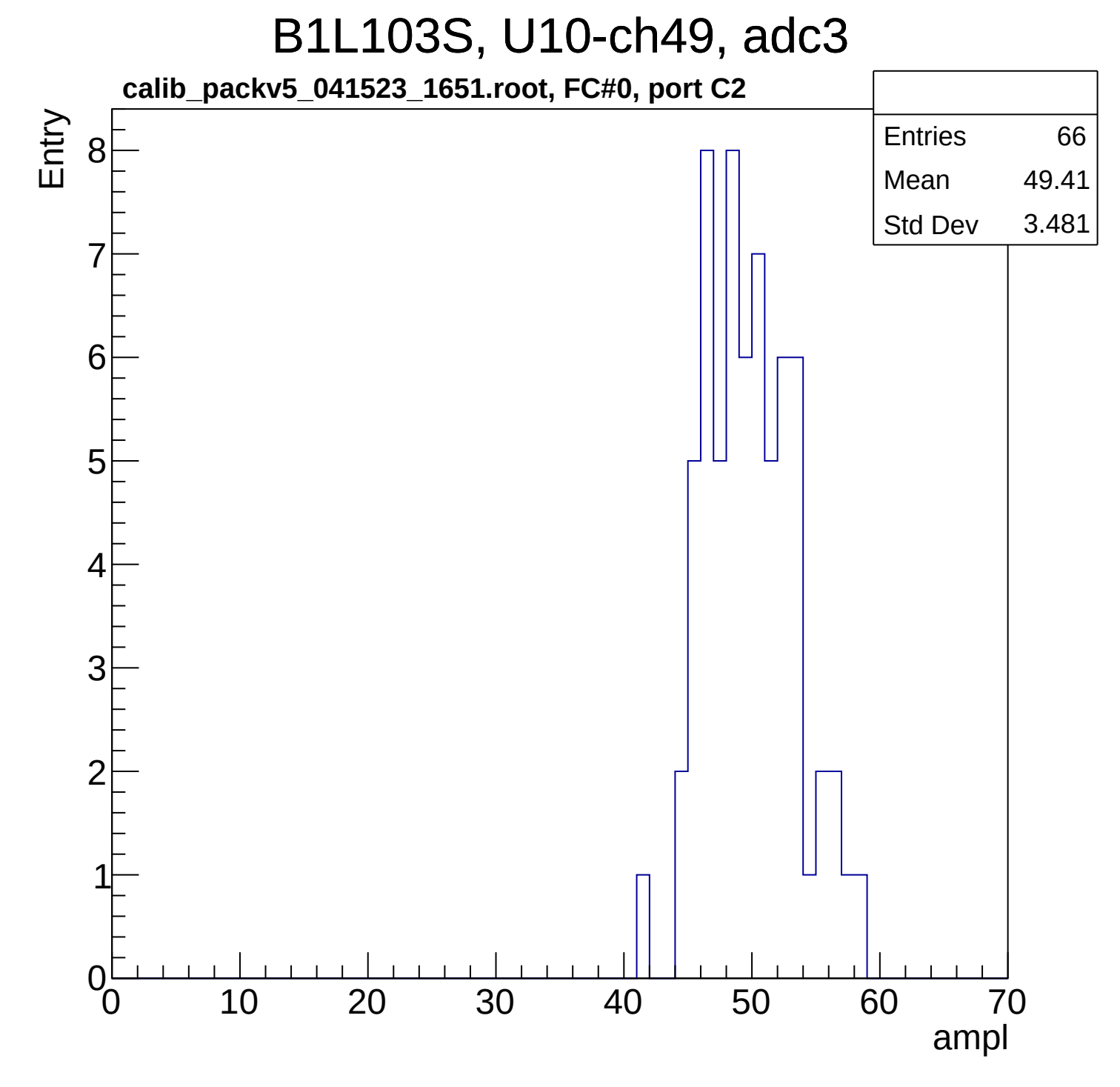
40
50
60
70


B1L103S, U10-ch49, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 49.41
Std Dev 3.481
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
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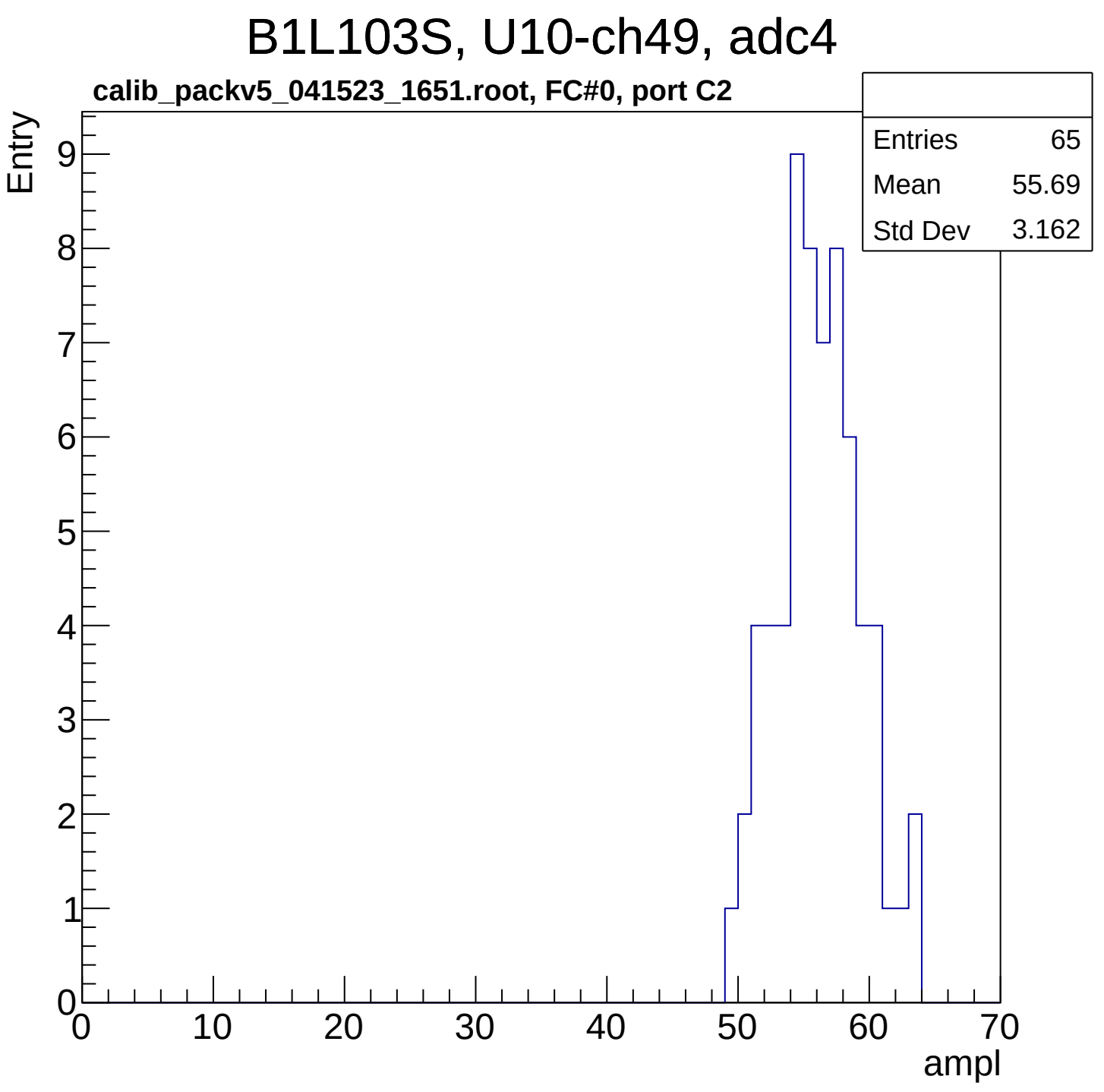
60
70


B1L103S, U10-ch49, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 55.69
Std Dev 3.162
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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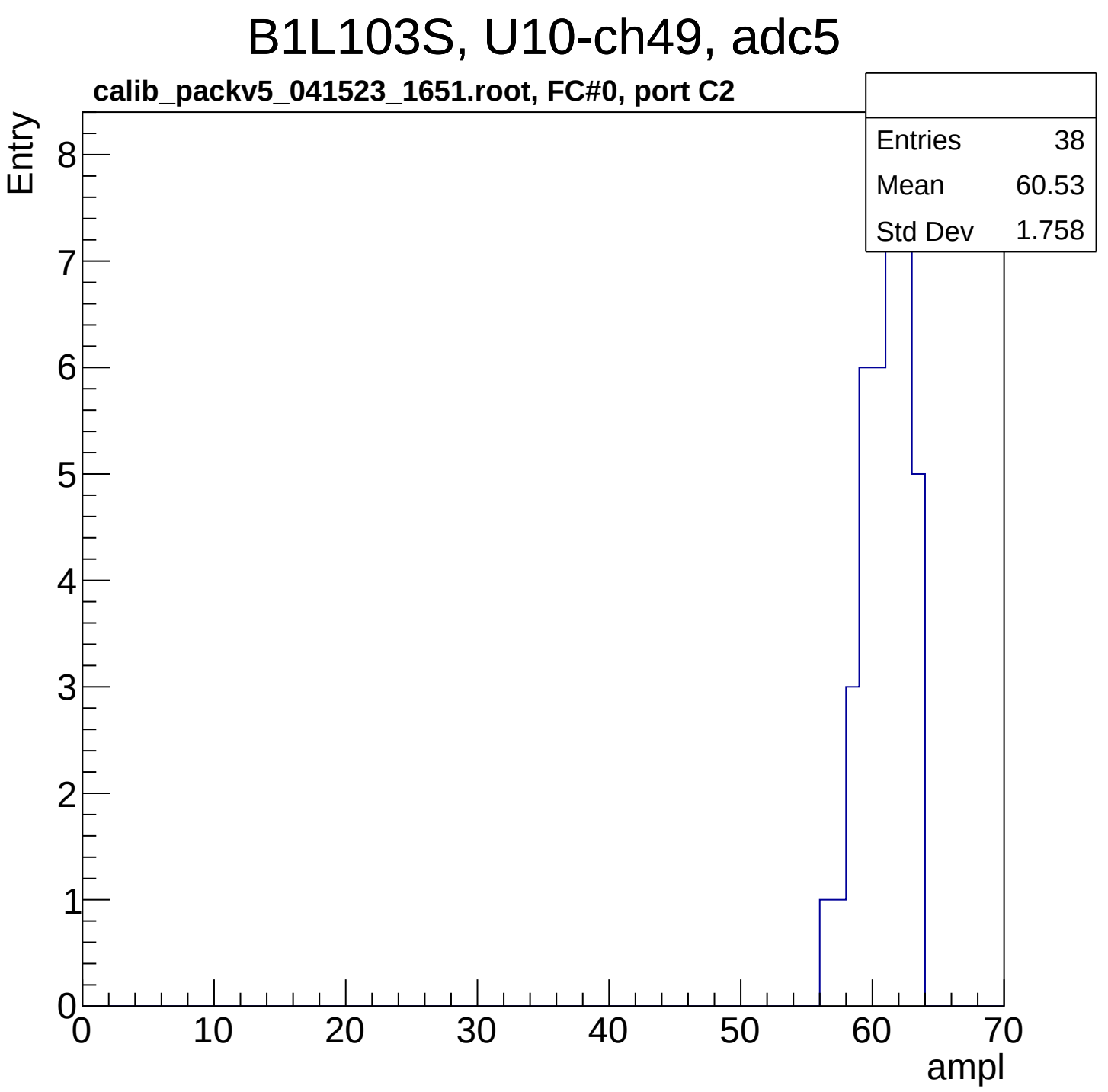
50
60
70


B1L103S, U10-ch49, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 38
Mean 60.53
Std Dev 1.758
Entry
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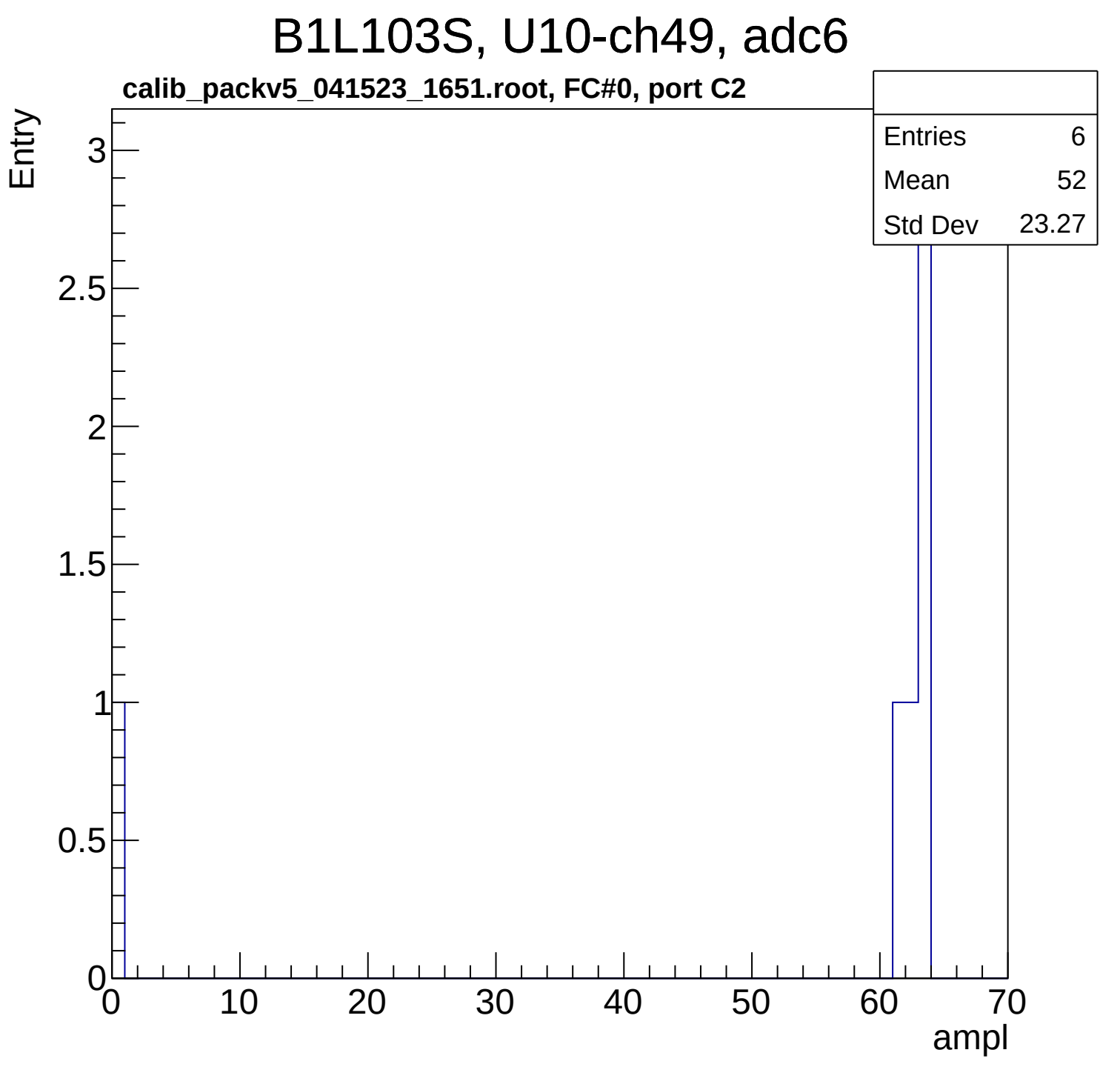
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch49, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 52
Std Dev 23.27
Entry
ampl
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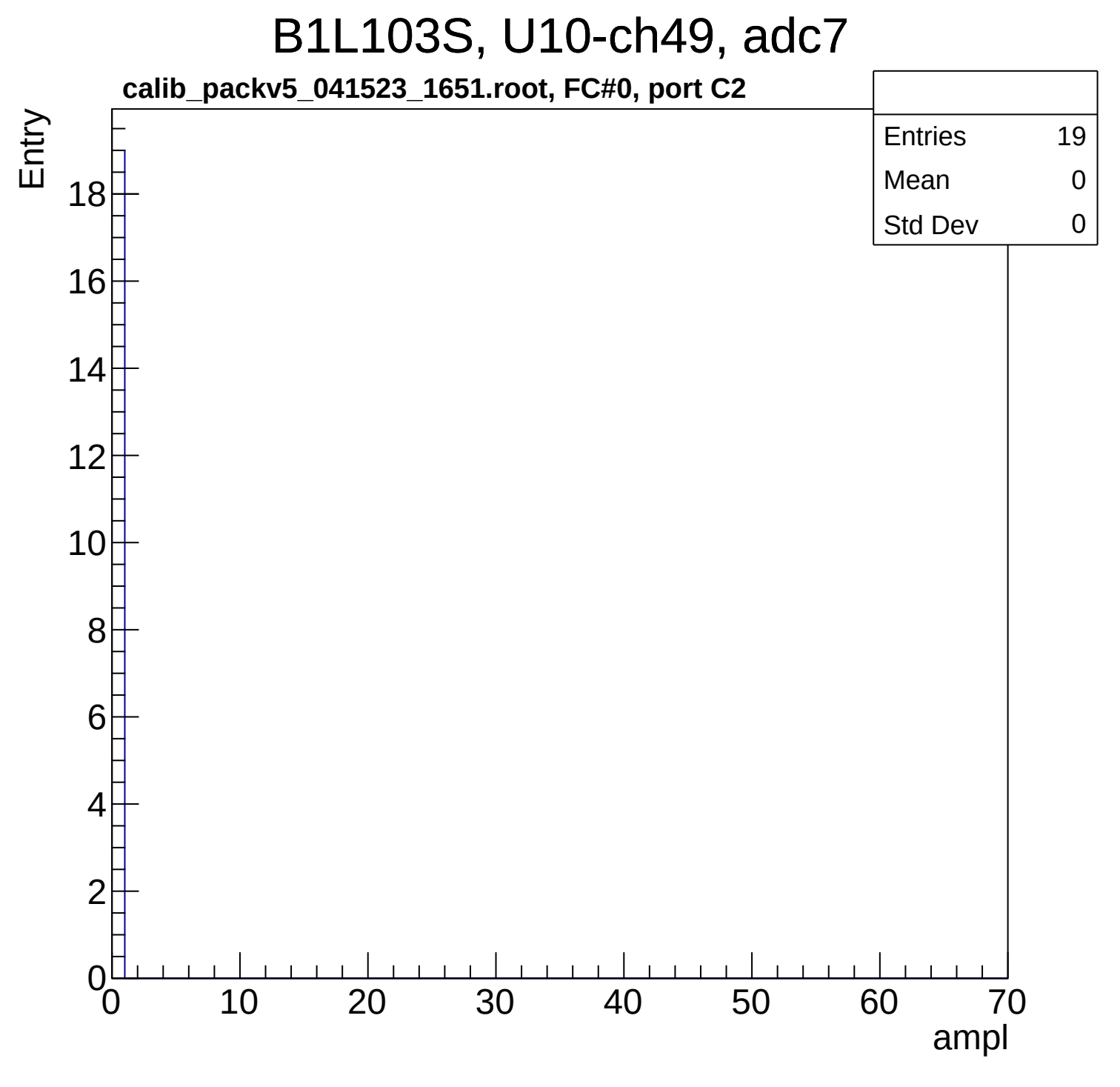
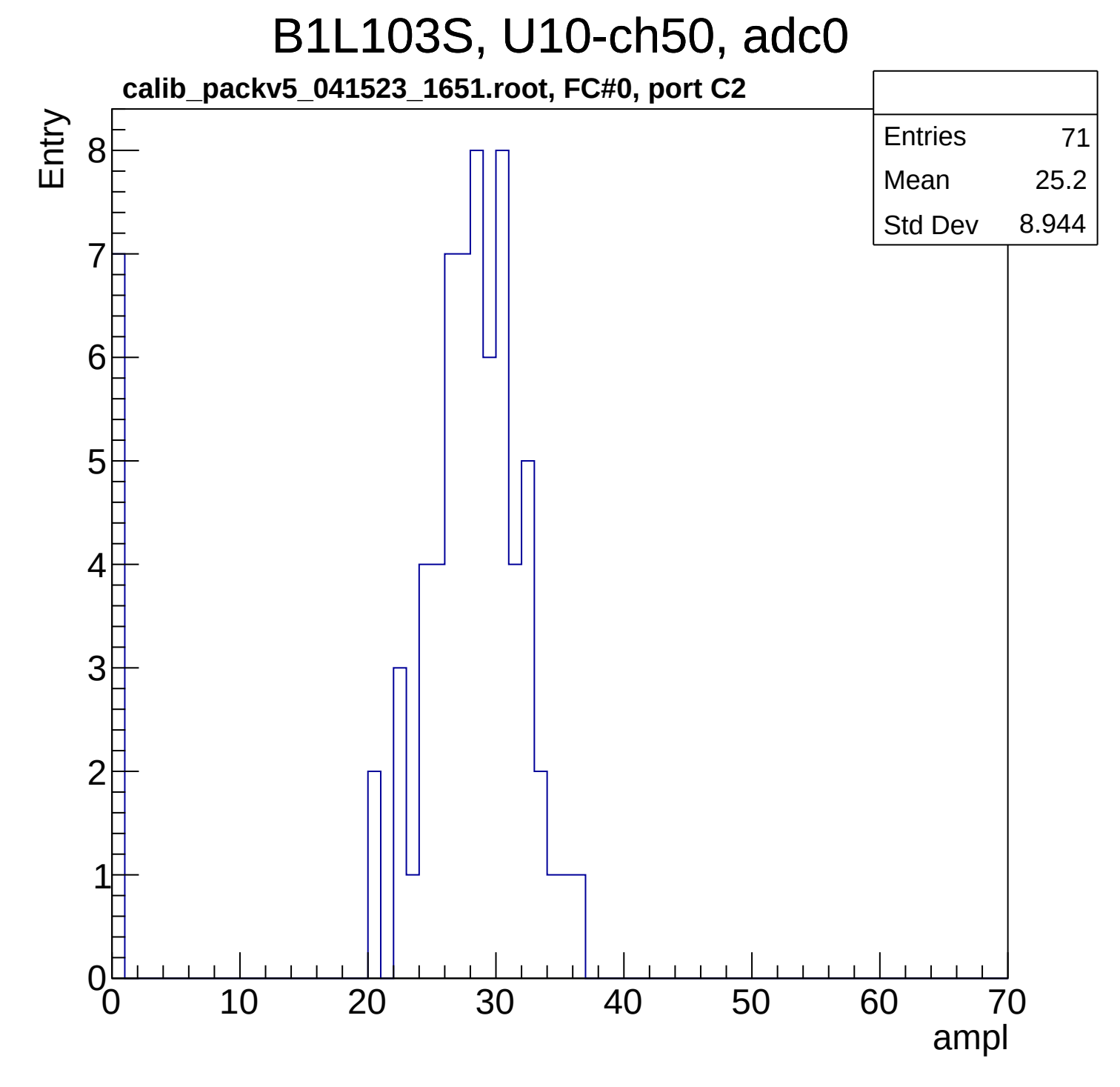
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U10-ch49, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch50, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 25.2
Std Dev 8.944
Entry
ampl
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2
3
4
5
6
7
8
0
10
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60
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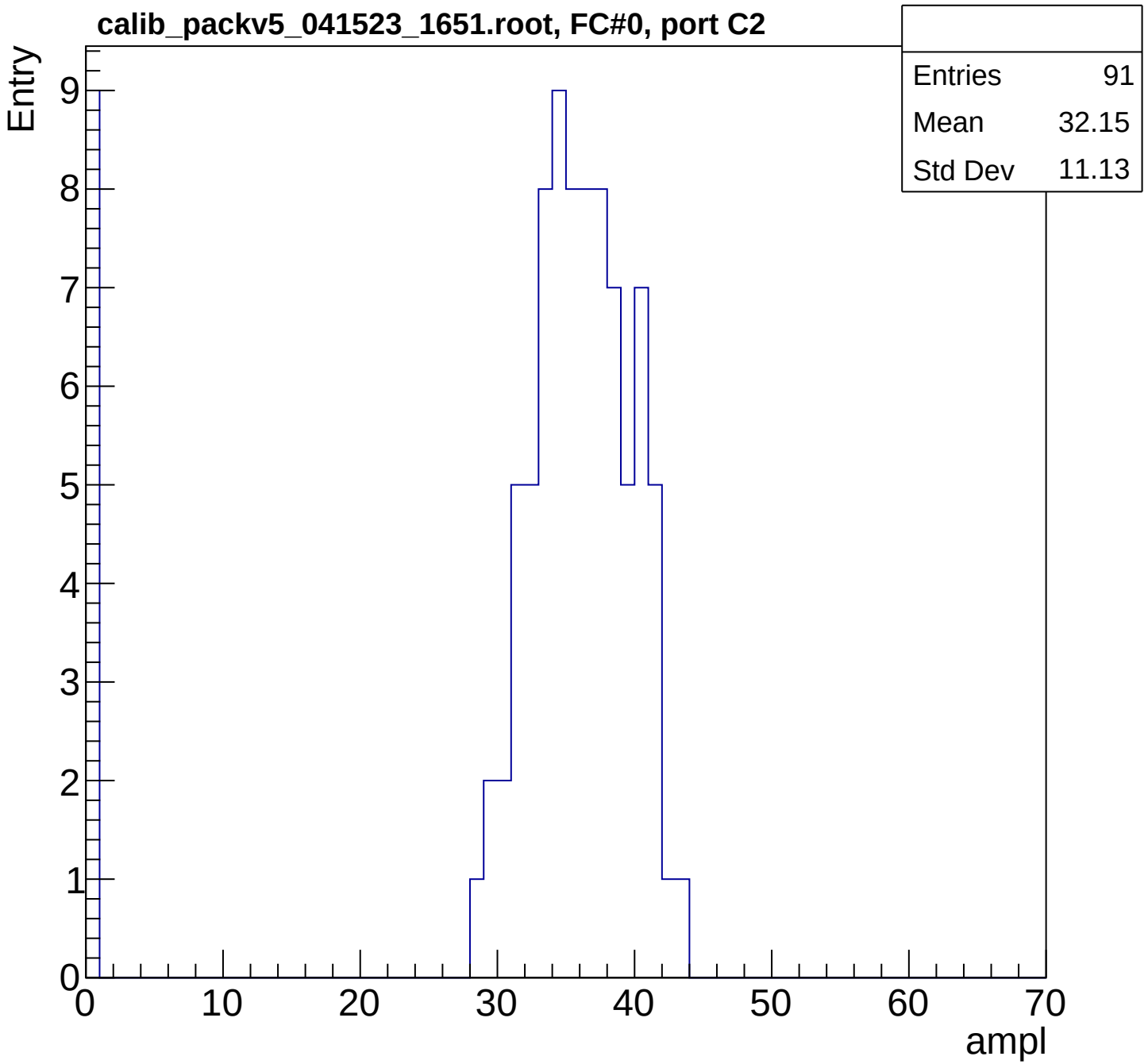
B1L103S, U10-ch50, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 91
Mean 32.15
Std Dev 11.13
Entry
ampl
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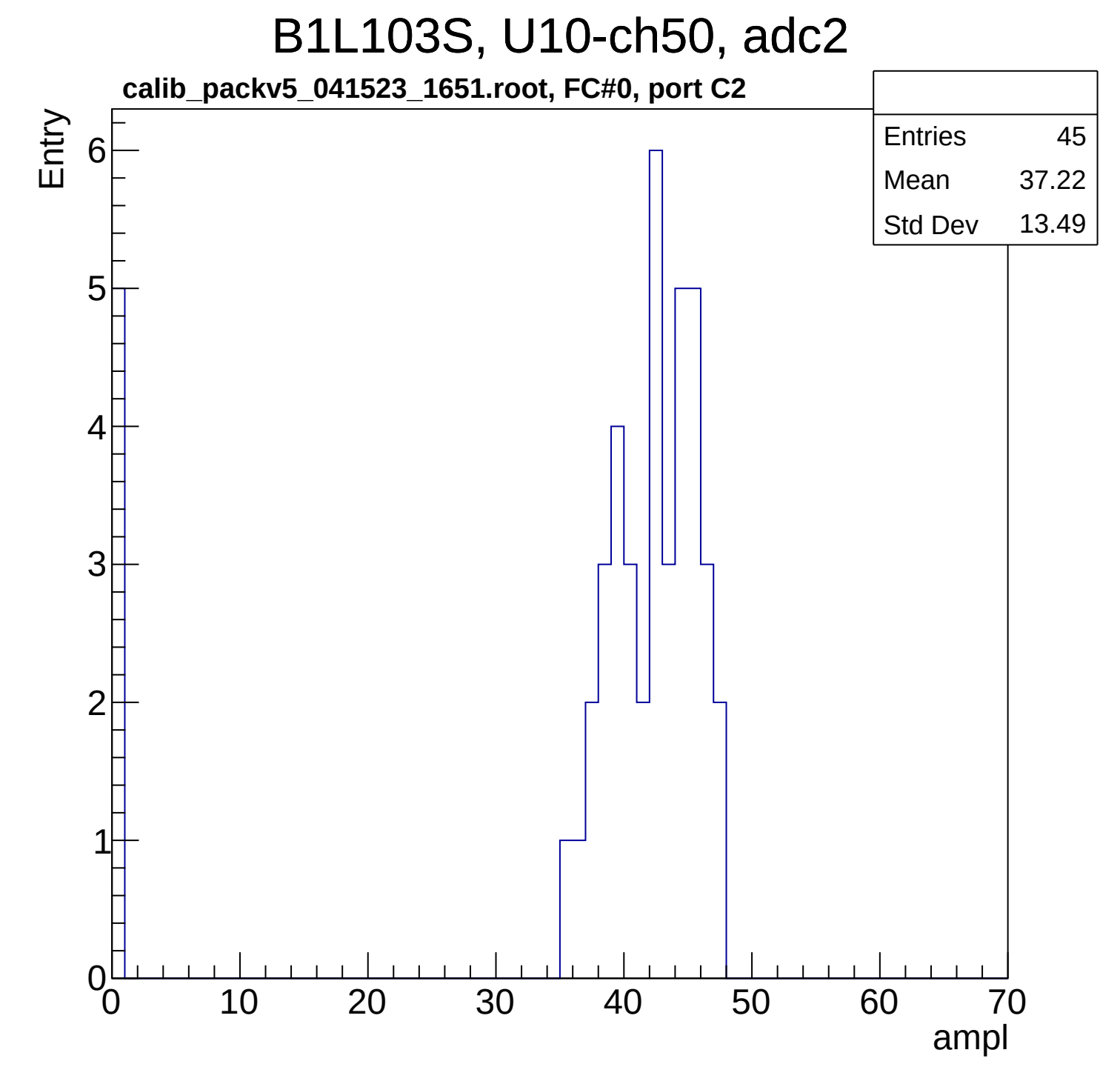
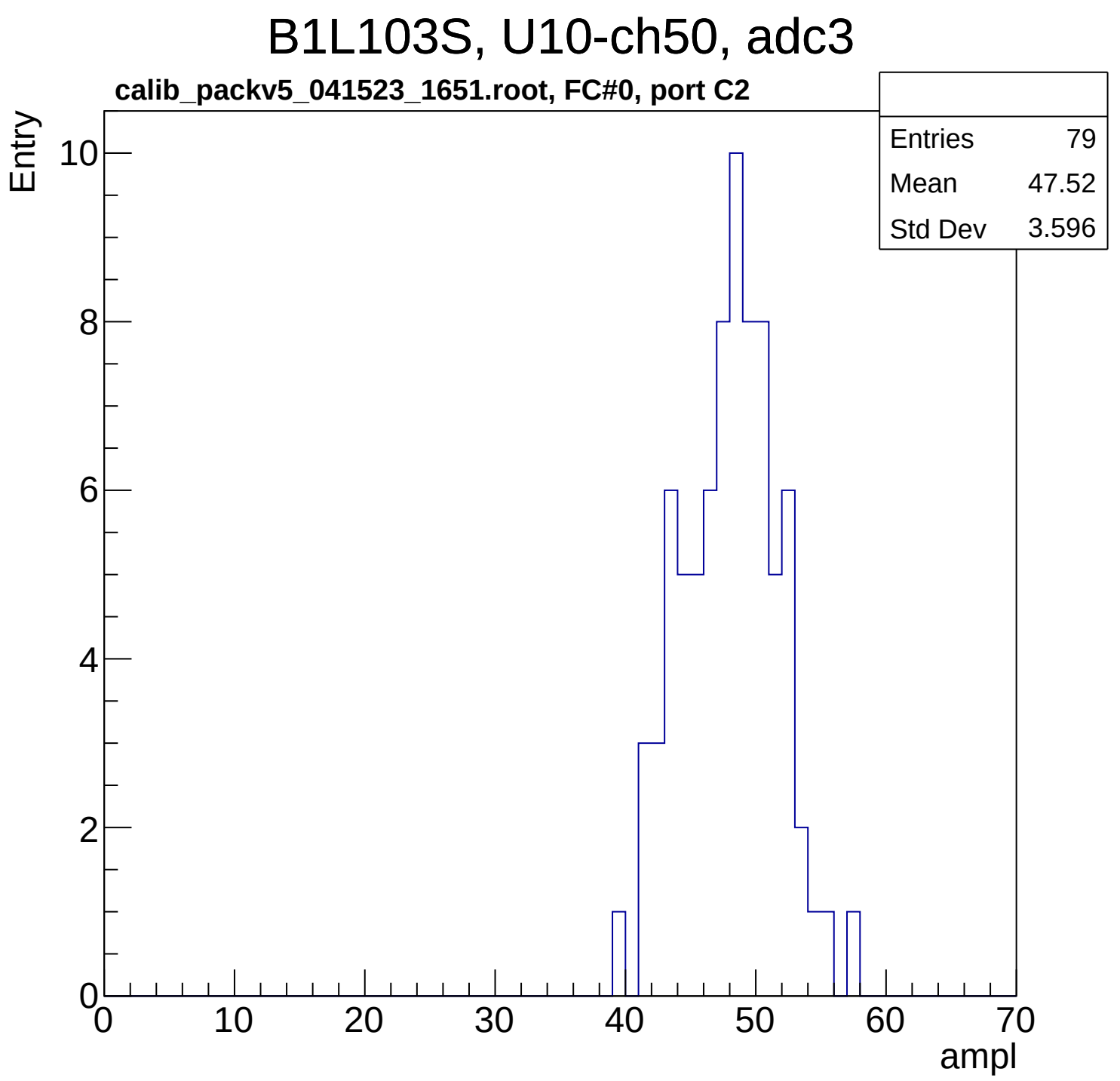
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U10-ch50, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 37.22
Std Dev 13.49
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch50, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 47.52
Std Dev 3.596
Entry
ampl
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4
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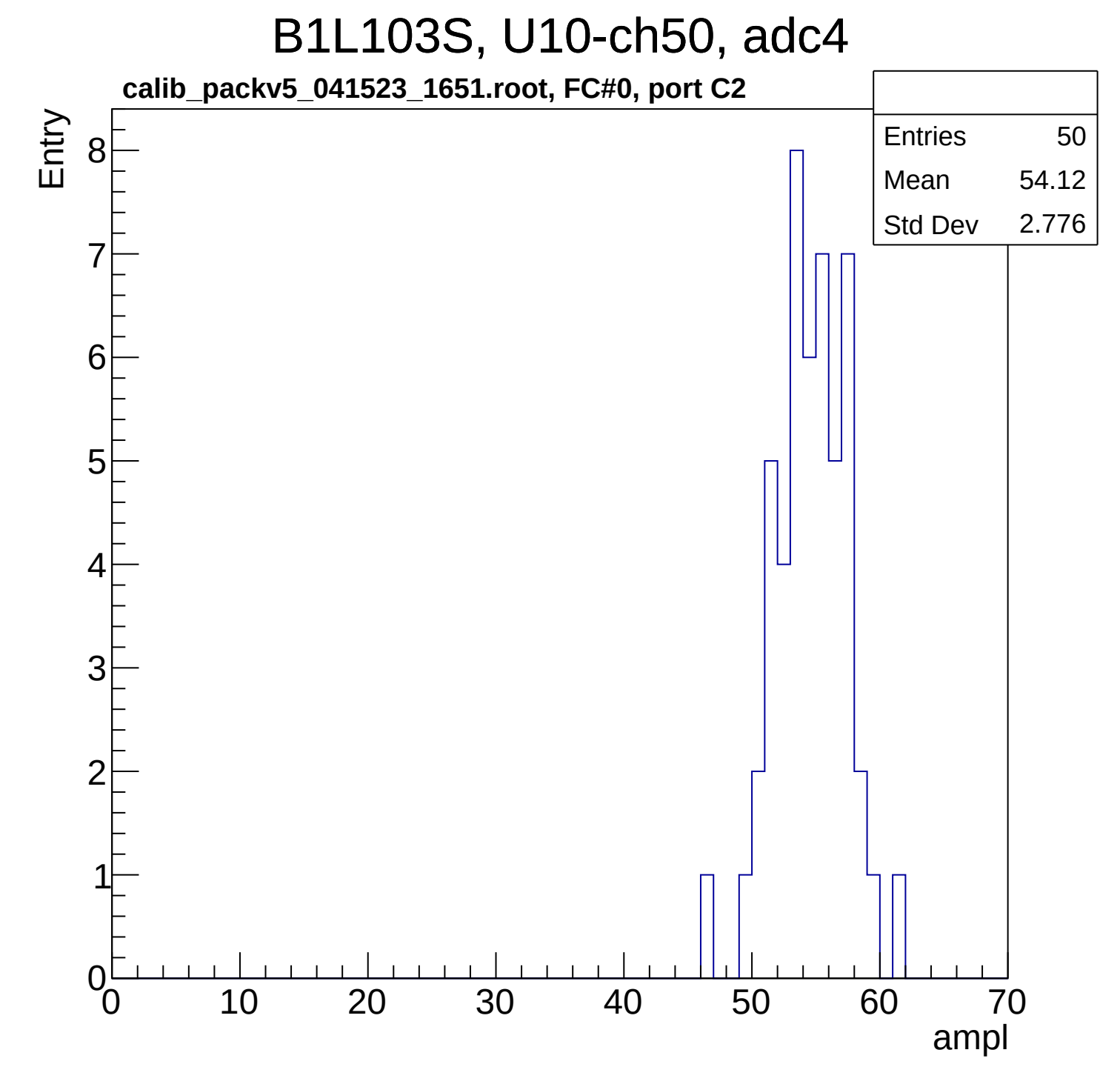
B1L103S, U10-ch50, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 54.12
Std Dev 2.776
Entry
ampl
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5
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7
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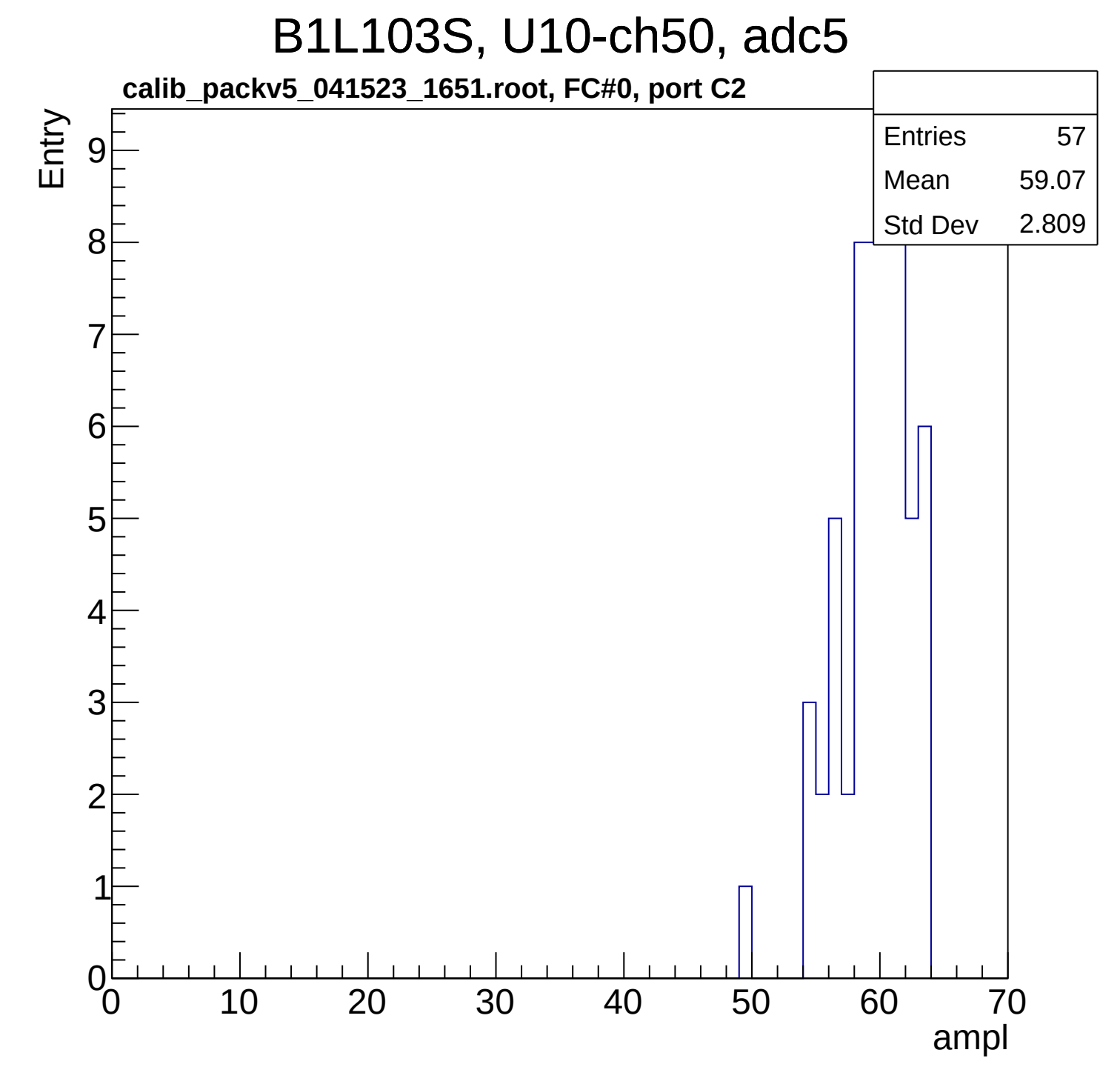
B1L103S, U10-ch50, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 59.07
Std Dev 2.809
Entry
ampl
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8
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0
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60
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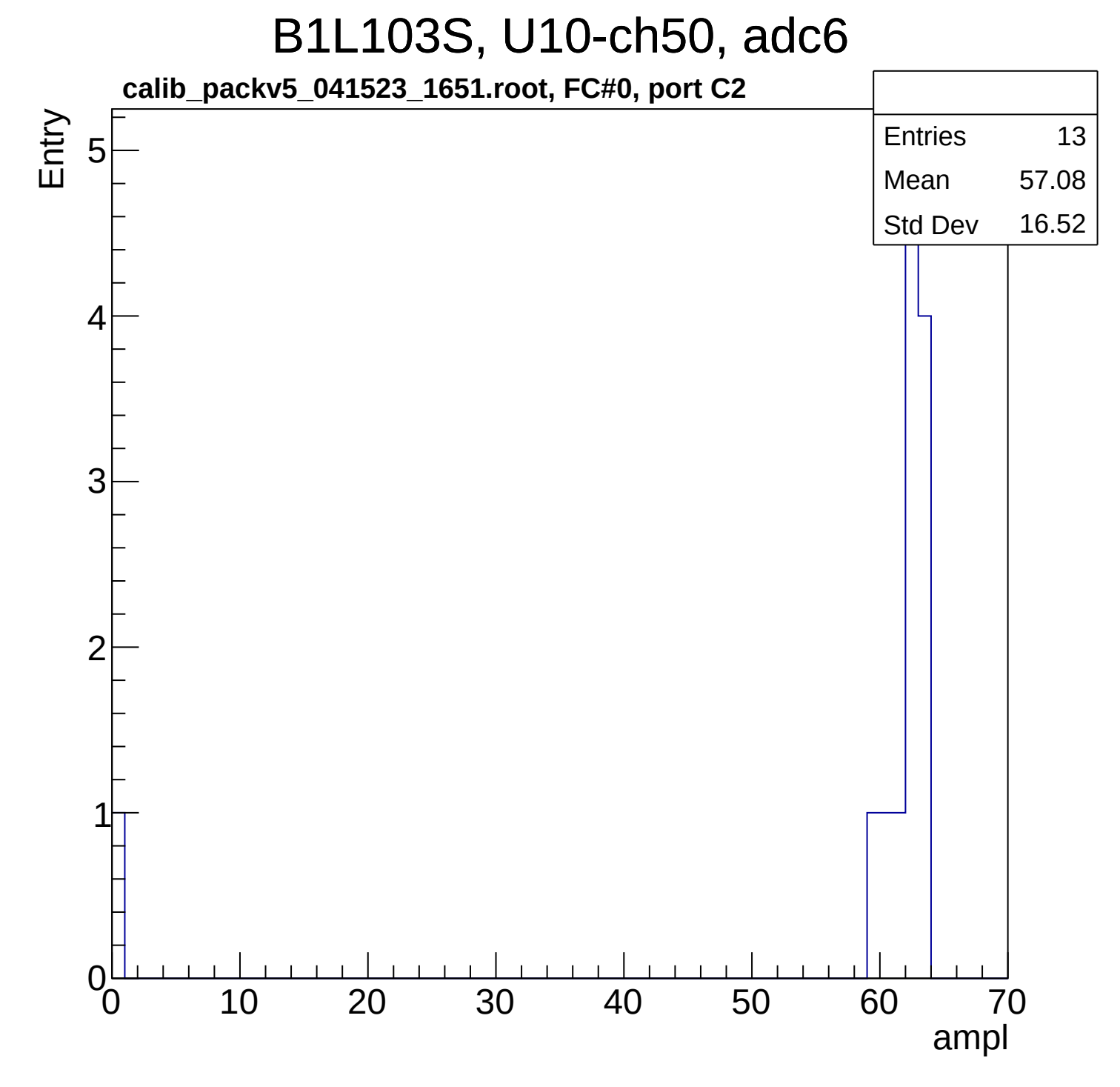
B1L103S, U10-ch50, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 13
Mean 57.08
Std Dev 16.52
Entry
ampl
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2
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4
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0
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40
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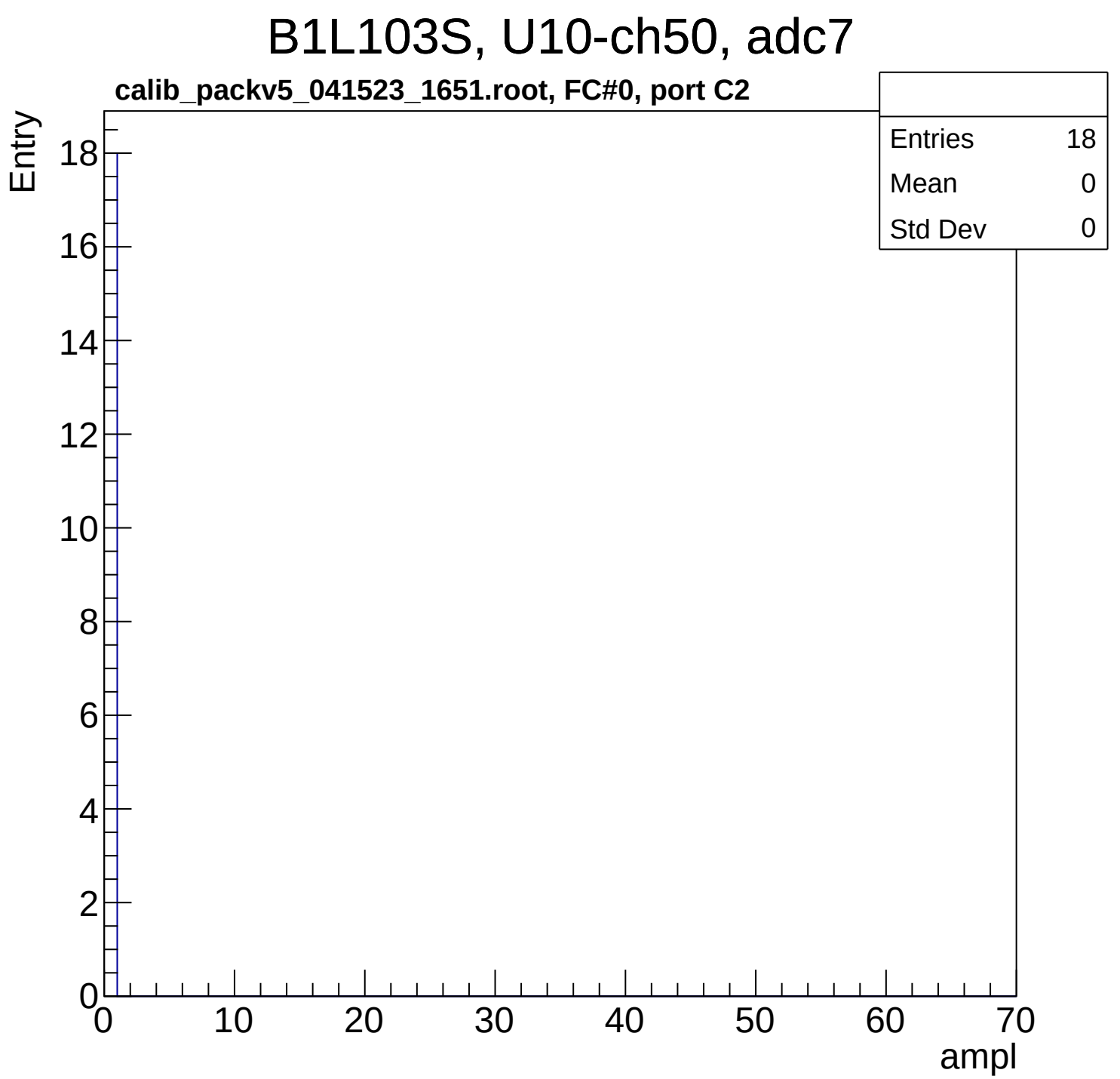
B1L103S, U10-ch50, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
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6
8
10
12
14
16
18
0
10
20
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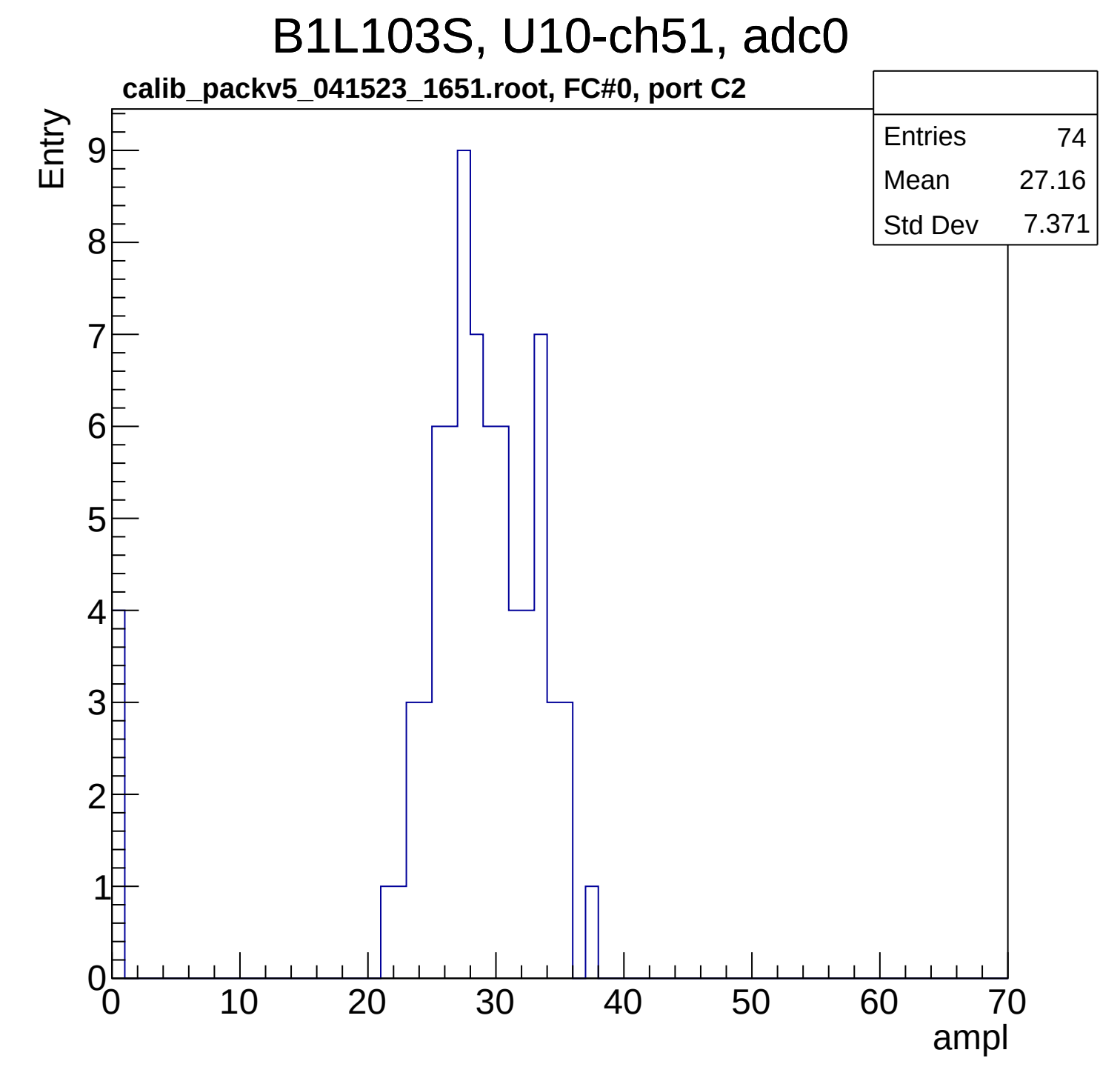
50
60
70
ampl


B1L103S, U10-ch51, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 27.16
Std Dev 7.371
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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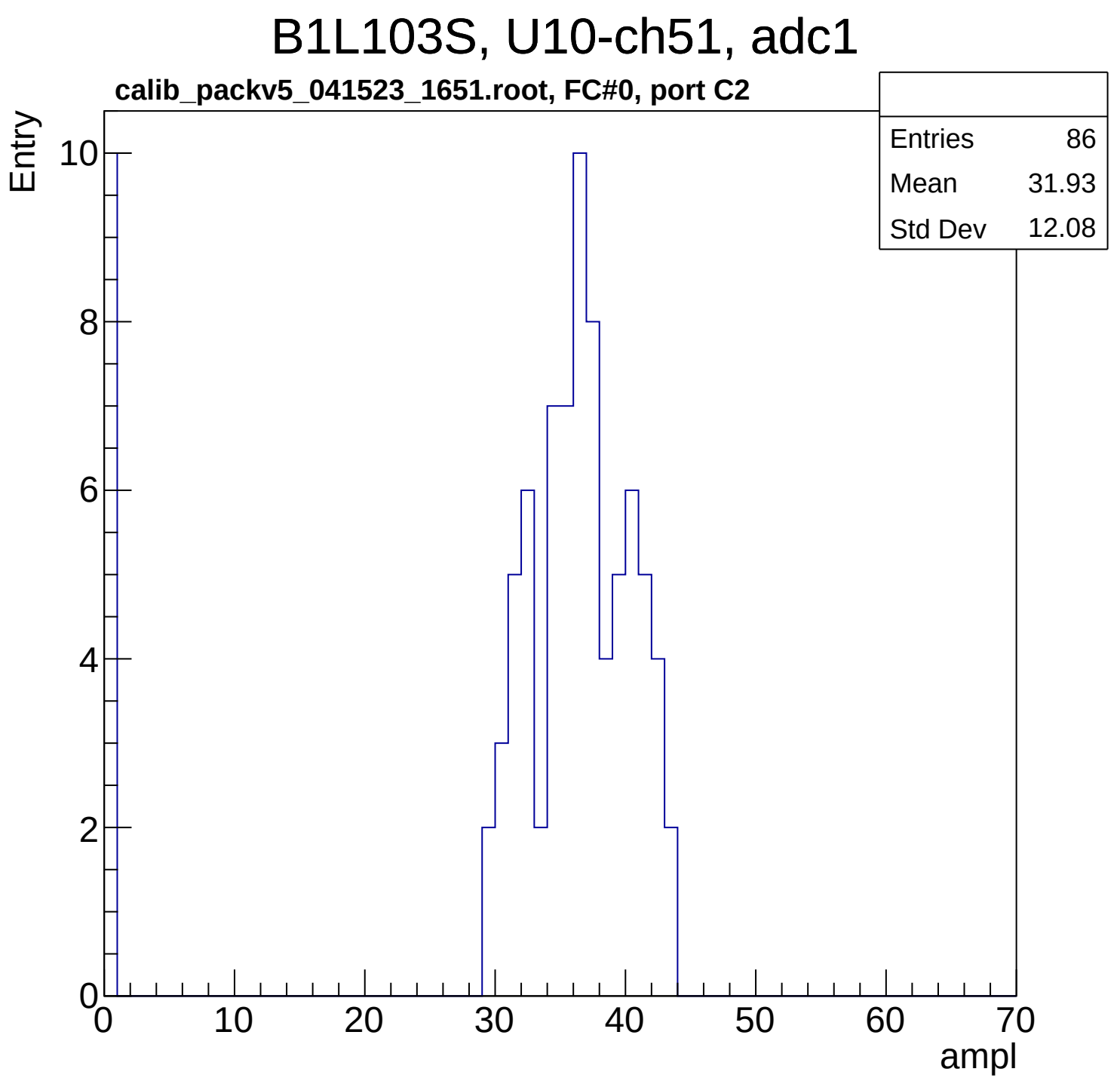
B1L103S, U10-ch51, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 31.93
Std Dev 12.08
Entry
ampl
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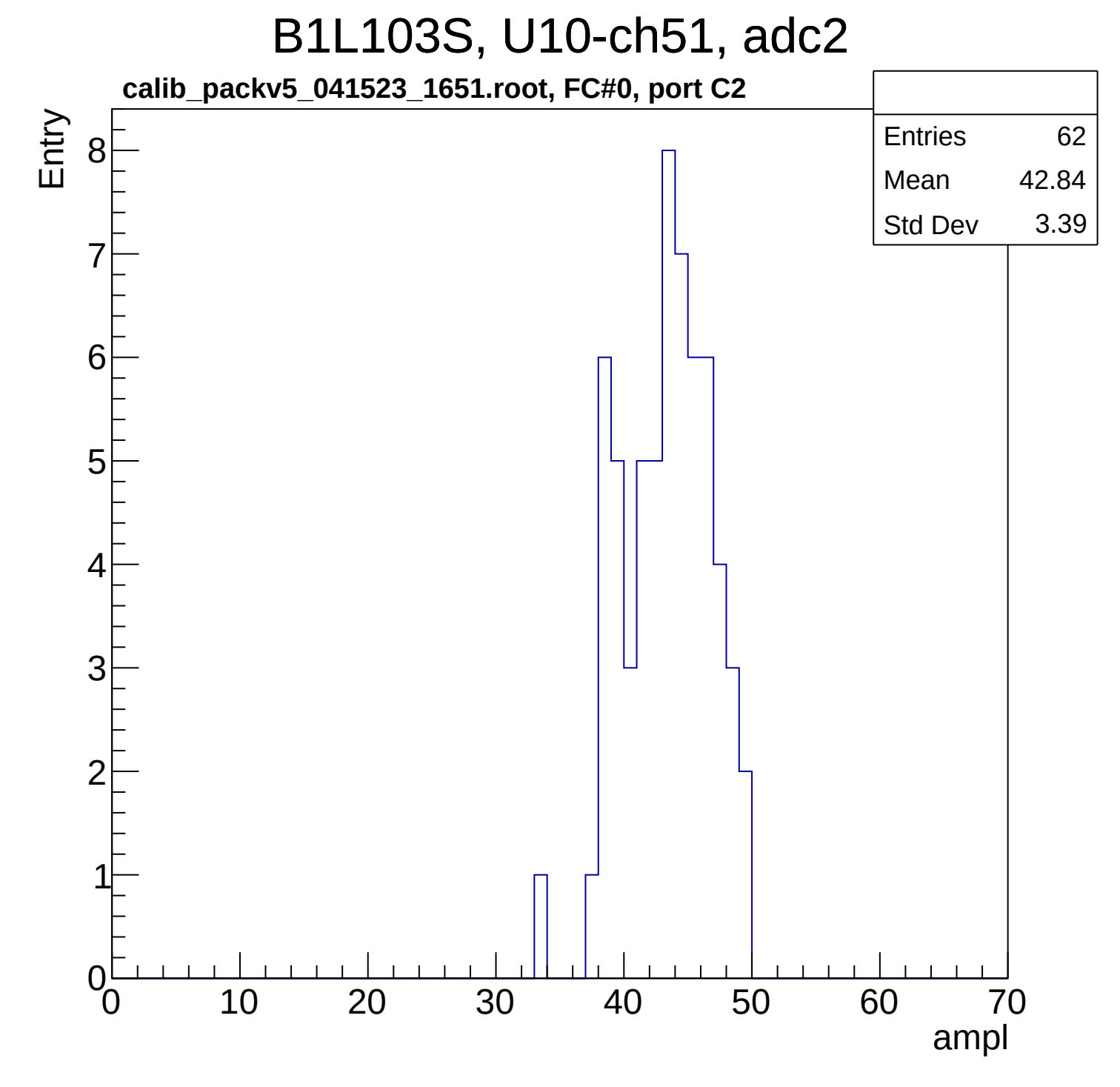
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U10-ch51, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 42.84
Std Dev 3.39
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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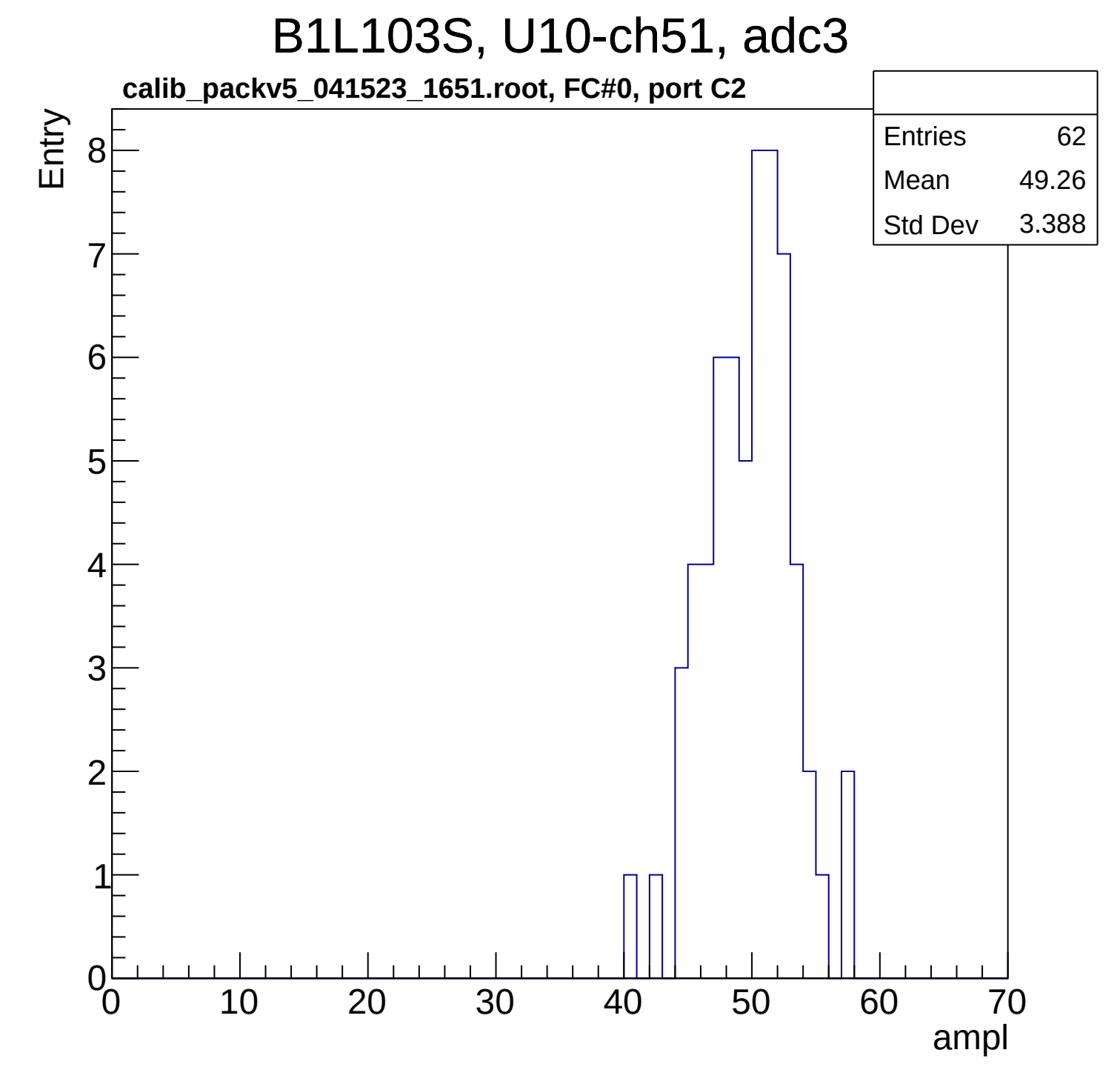
40
50
60
70


B1L103S, U10-ch51, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 49.26
Std Dev 3.388
Entry
ampl
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1
2
3
4
5
6
7
8
0
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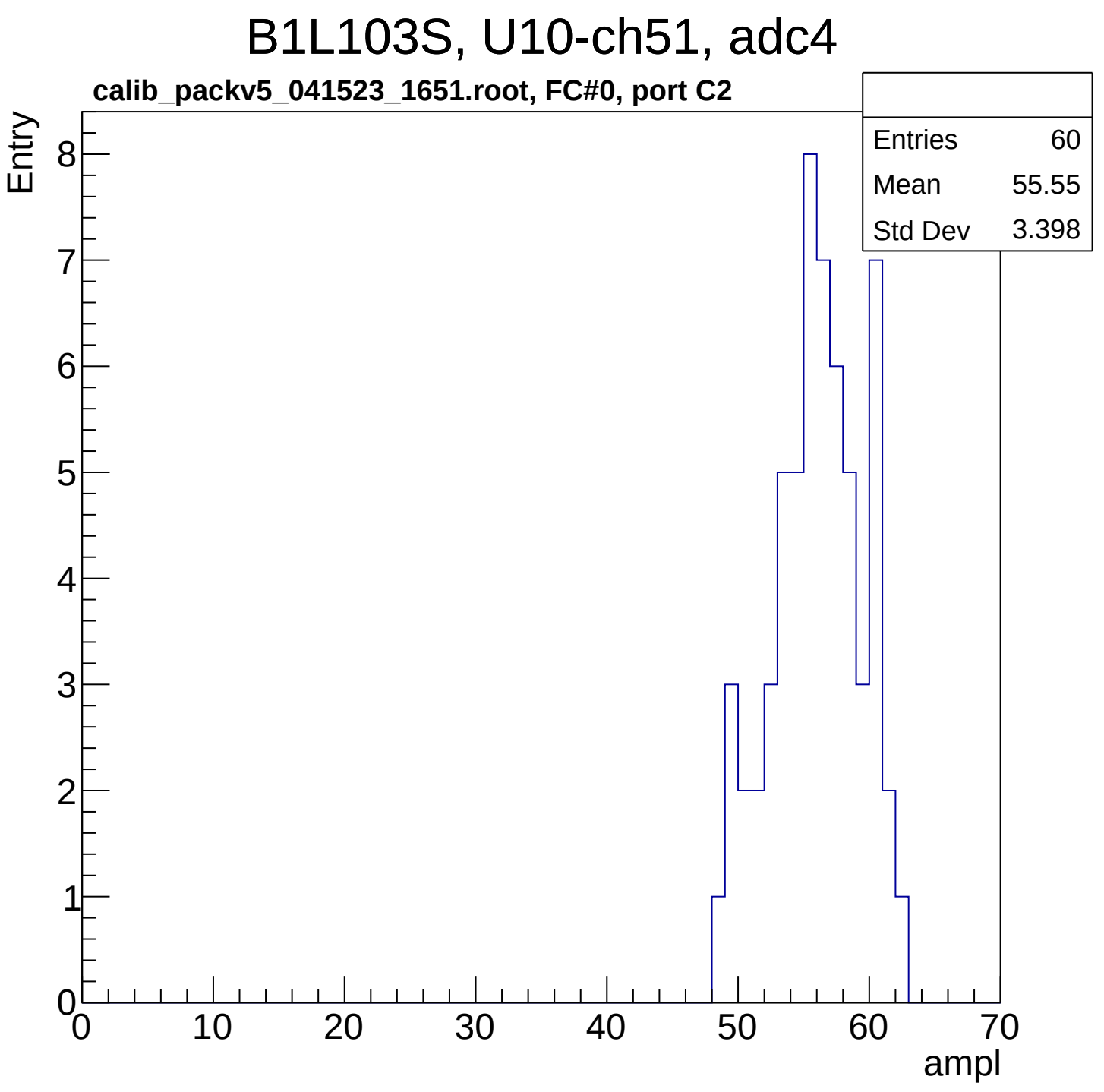
20
30
40
50
60
70


B1L103S, U10-ch51, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 55.55
Std Dev 3.398
Entry
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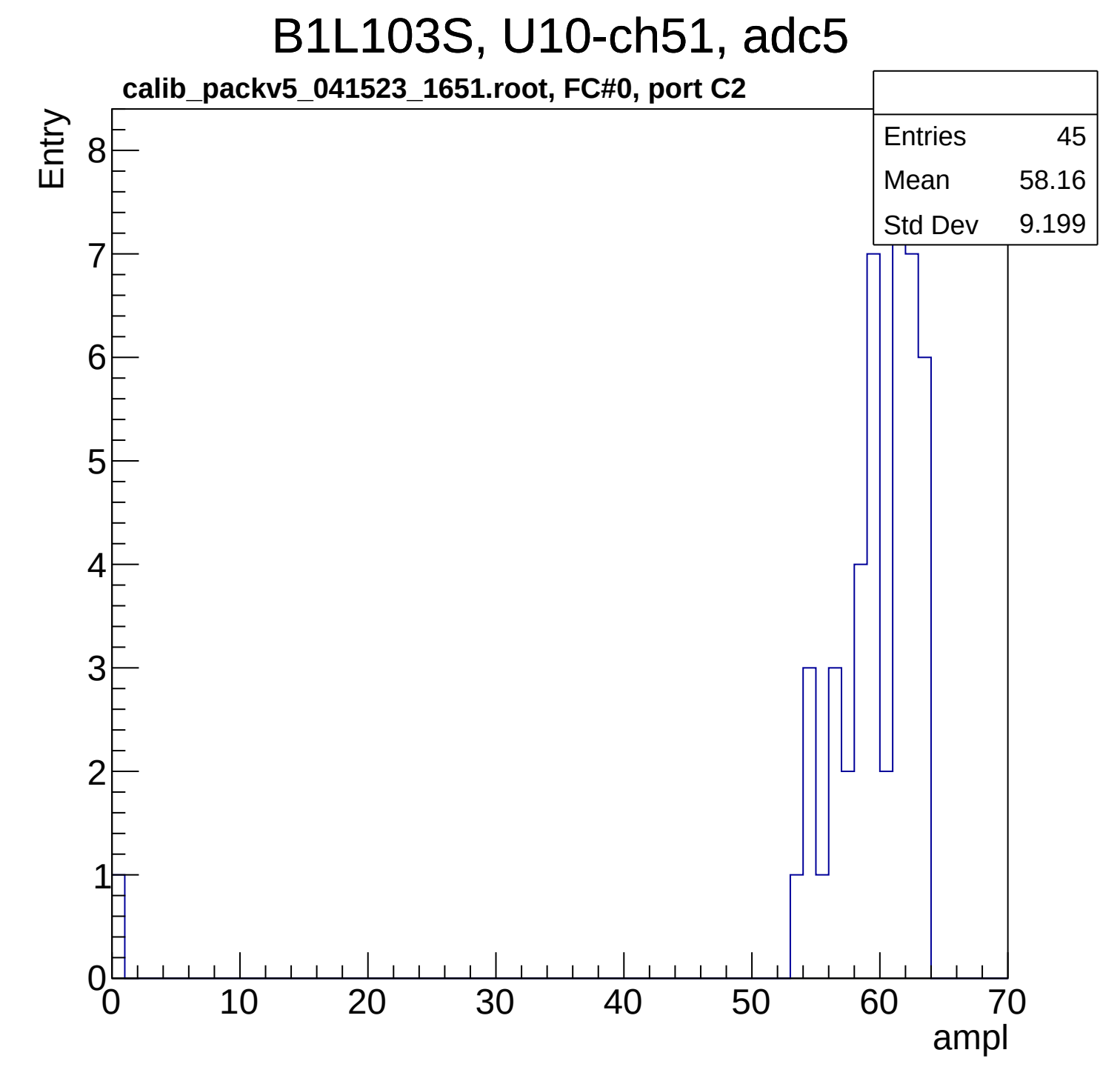
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch51, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 58.16
Std Dev 9.199
Entry
ampl
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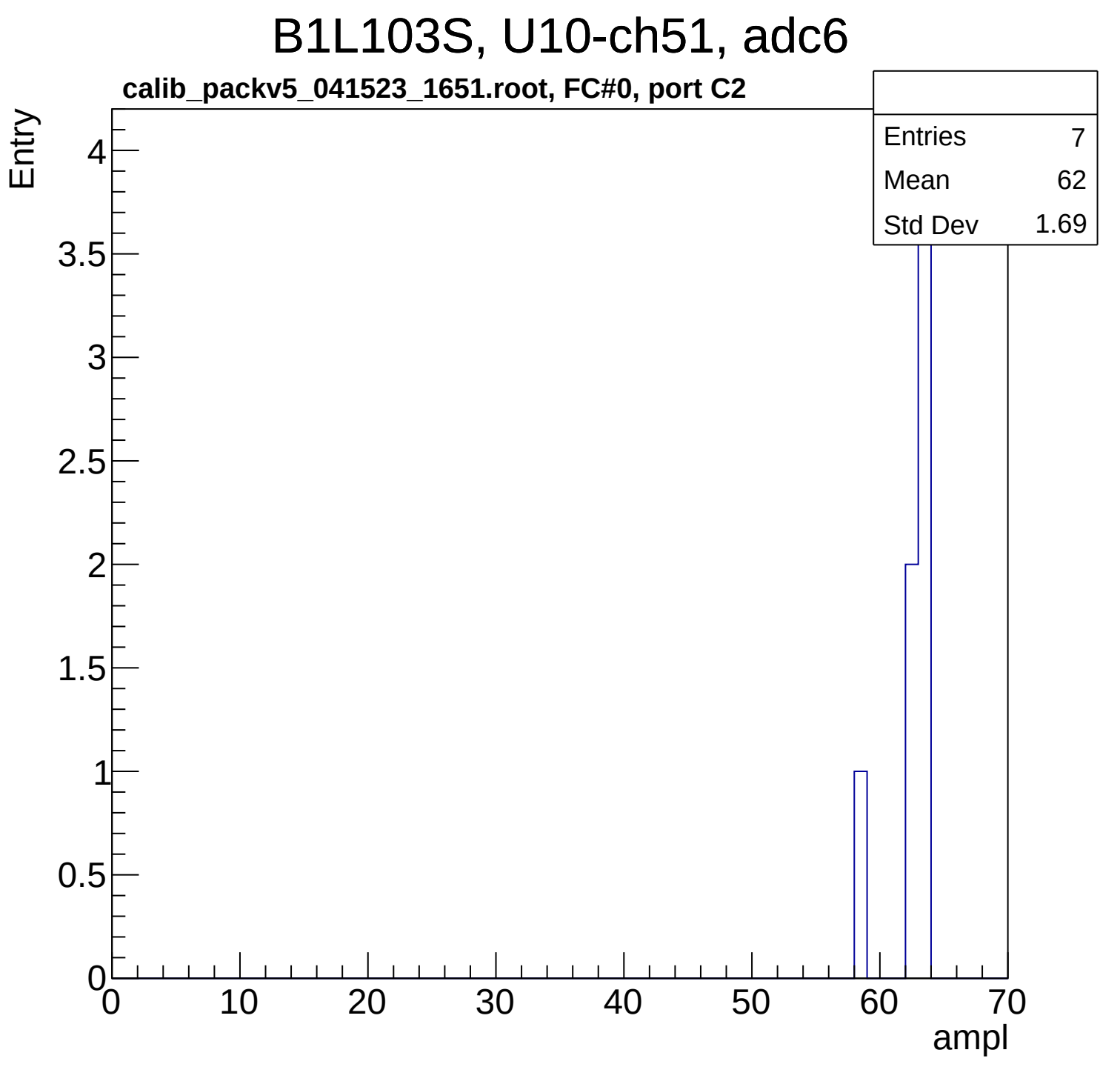
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U10-ch51, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 62
Std Dev 1.69
Entry
ampl
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1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
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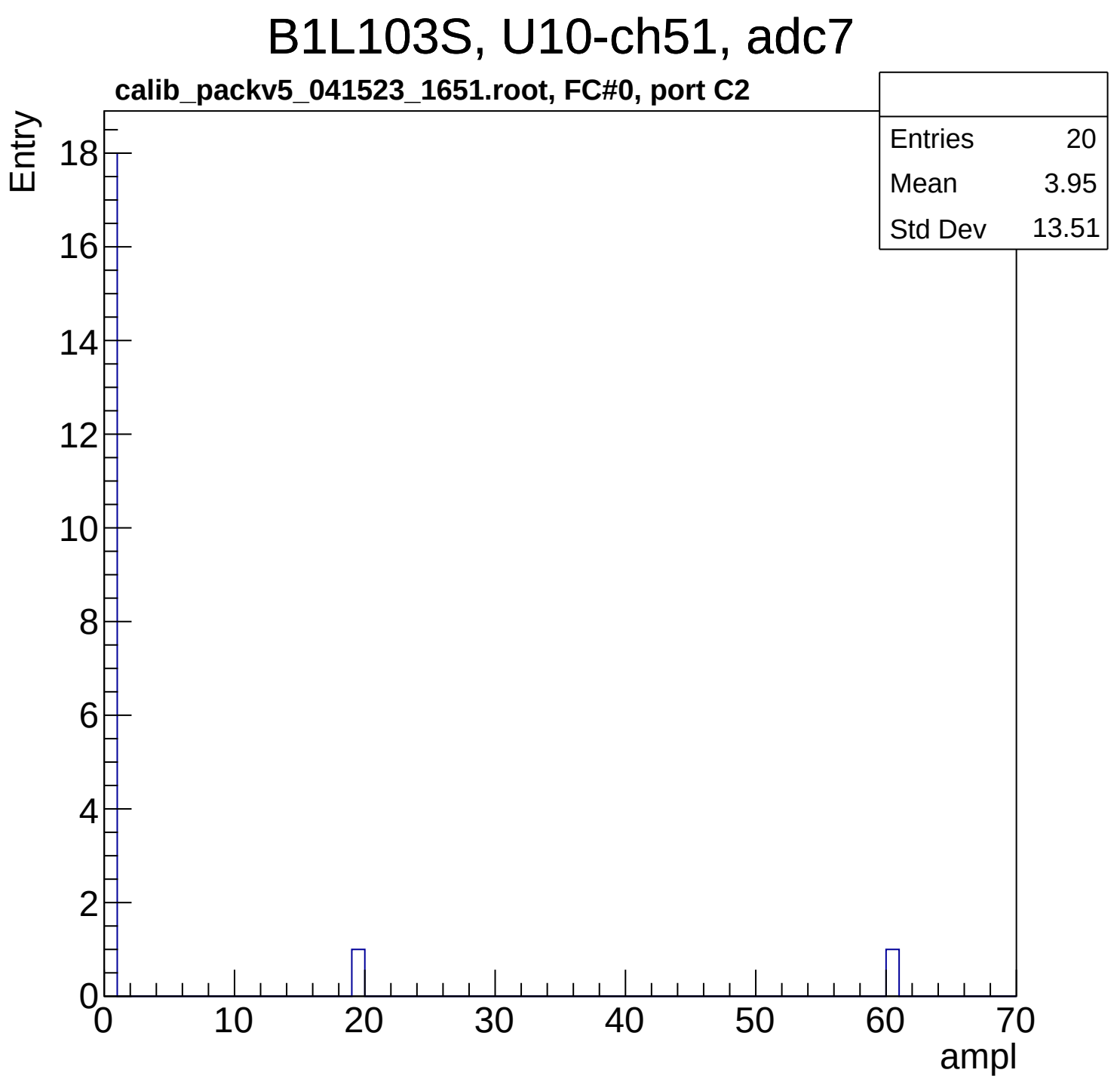
B1L103S, U10-ch51, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.95
Std Dev 13.51
Entry
0
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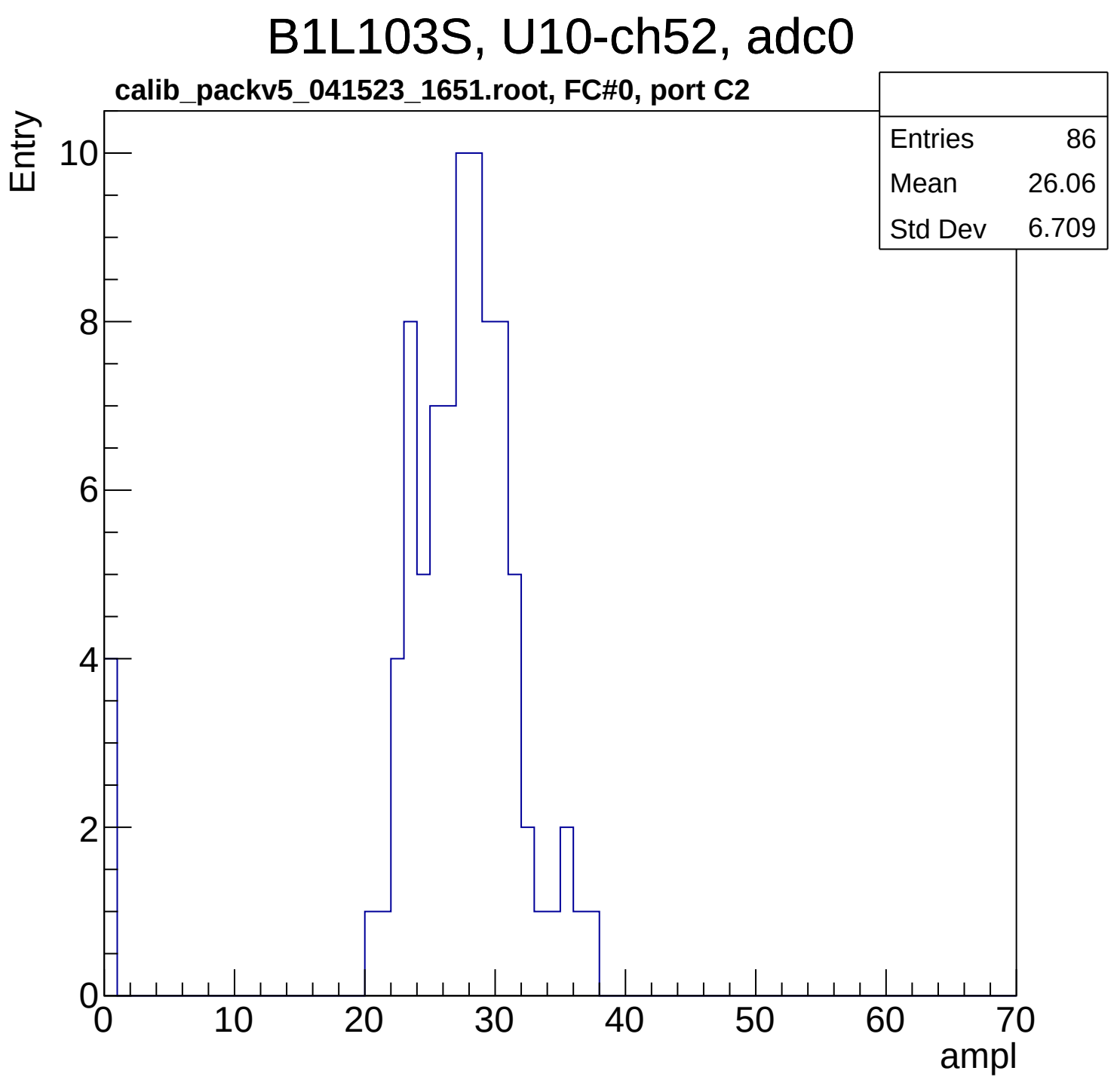
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch52, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 26.06
Std Dev 6.709
Entry
ampl
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4
6
8
10
0
10
20
30
40
50
60
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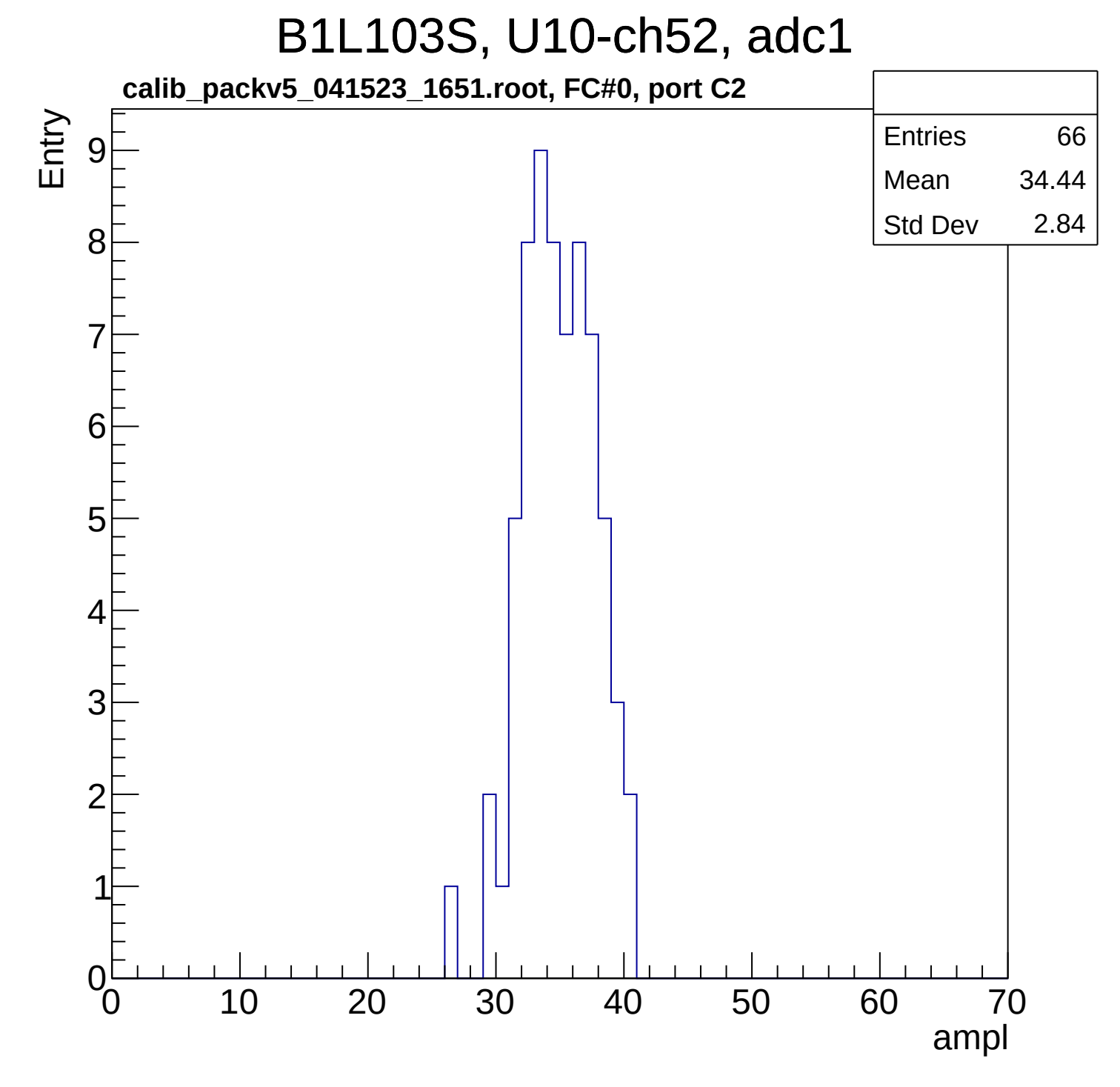
B1L103S, U10-ch52, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 34.44
Std Dev 2.84
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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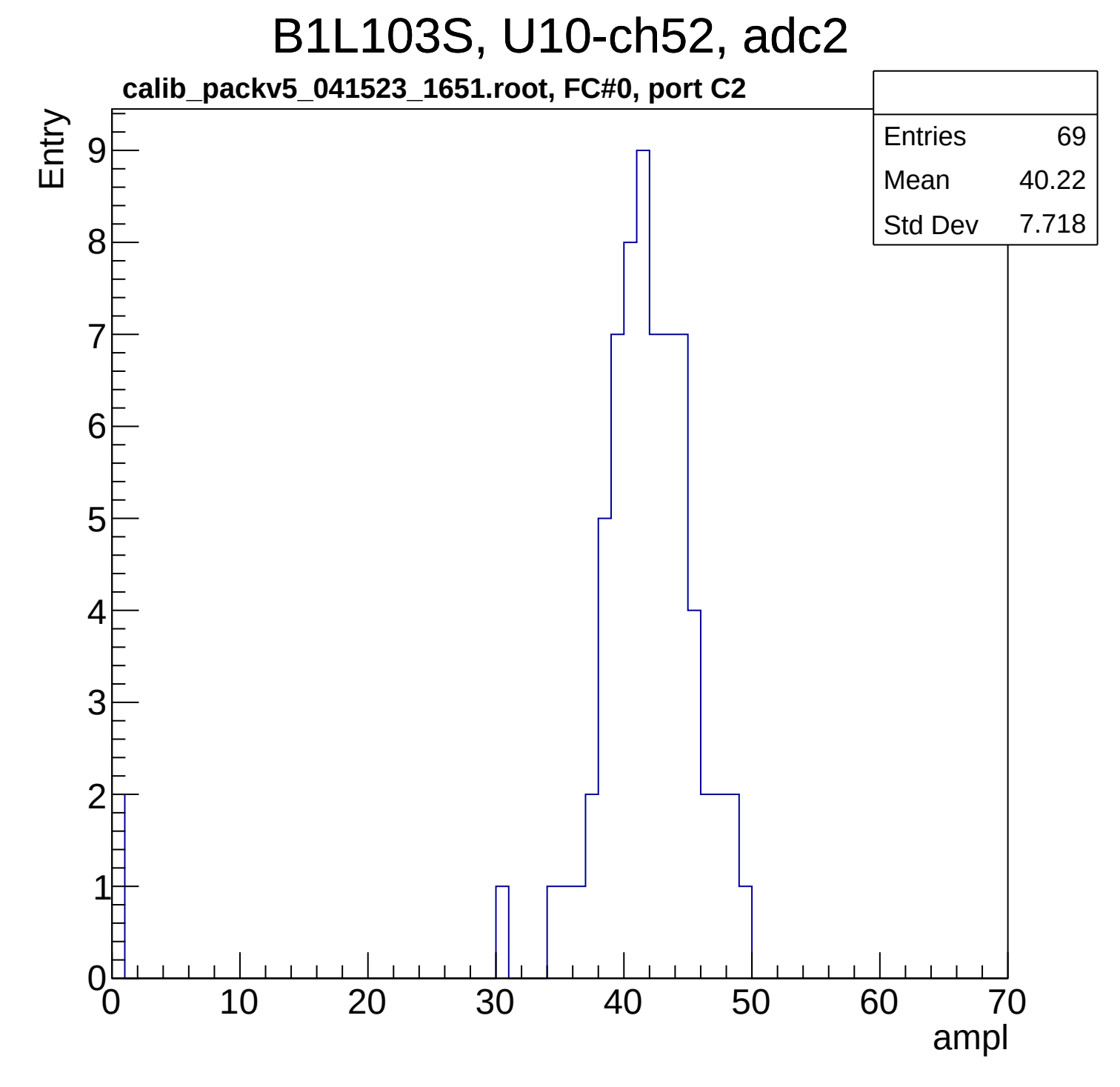
B1L103S, U10-ch52, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 40.22
Std Dev 7.718
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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60
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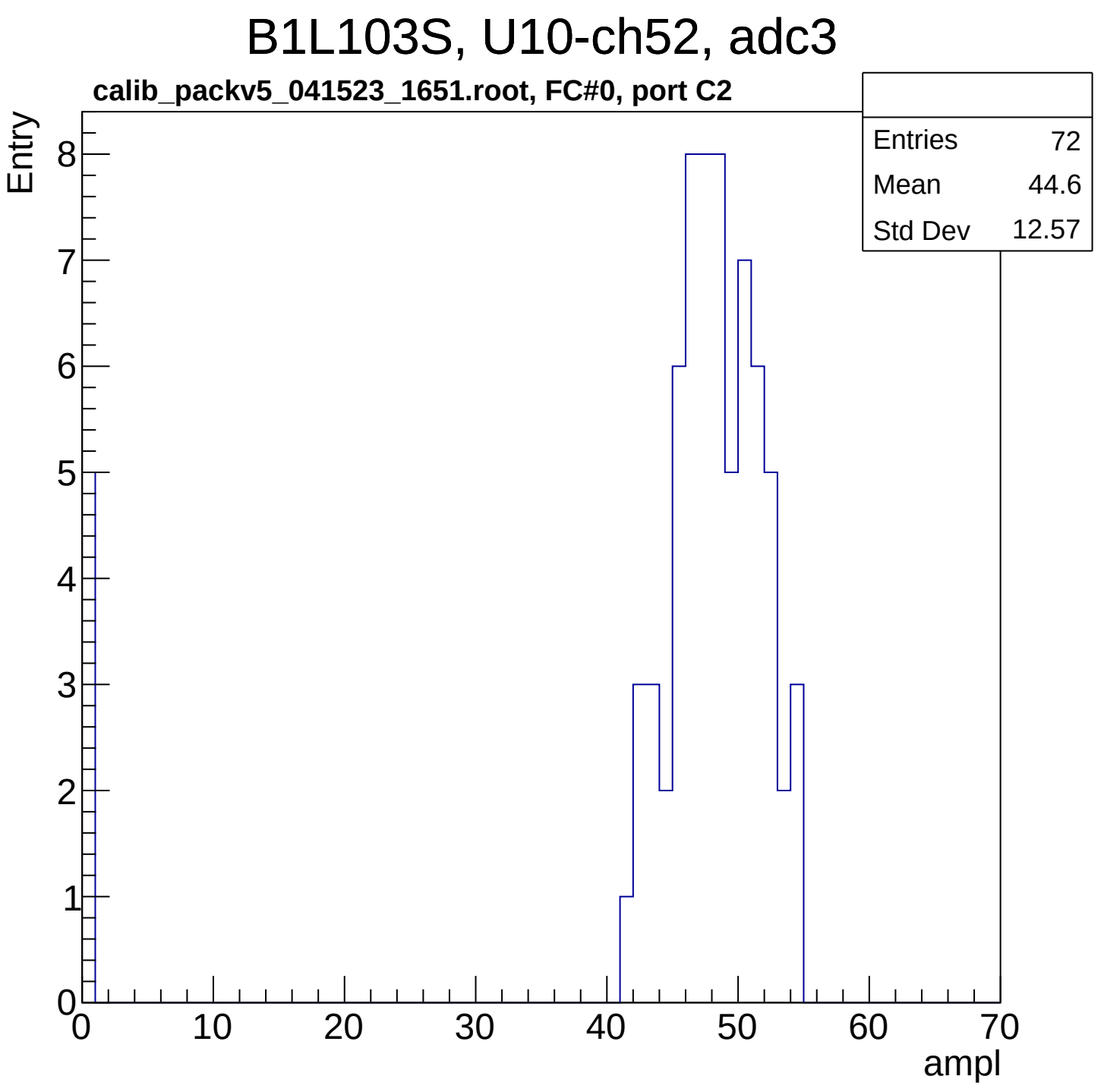
B1L103S, U10-ch52, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 44.6
Std Dev 12.57
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
30
40
50
60
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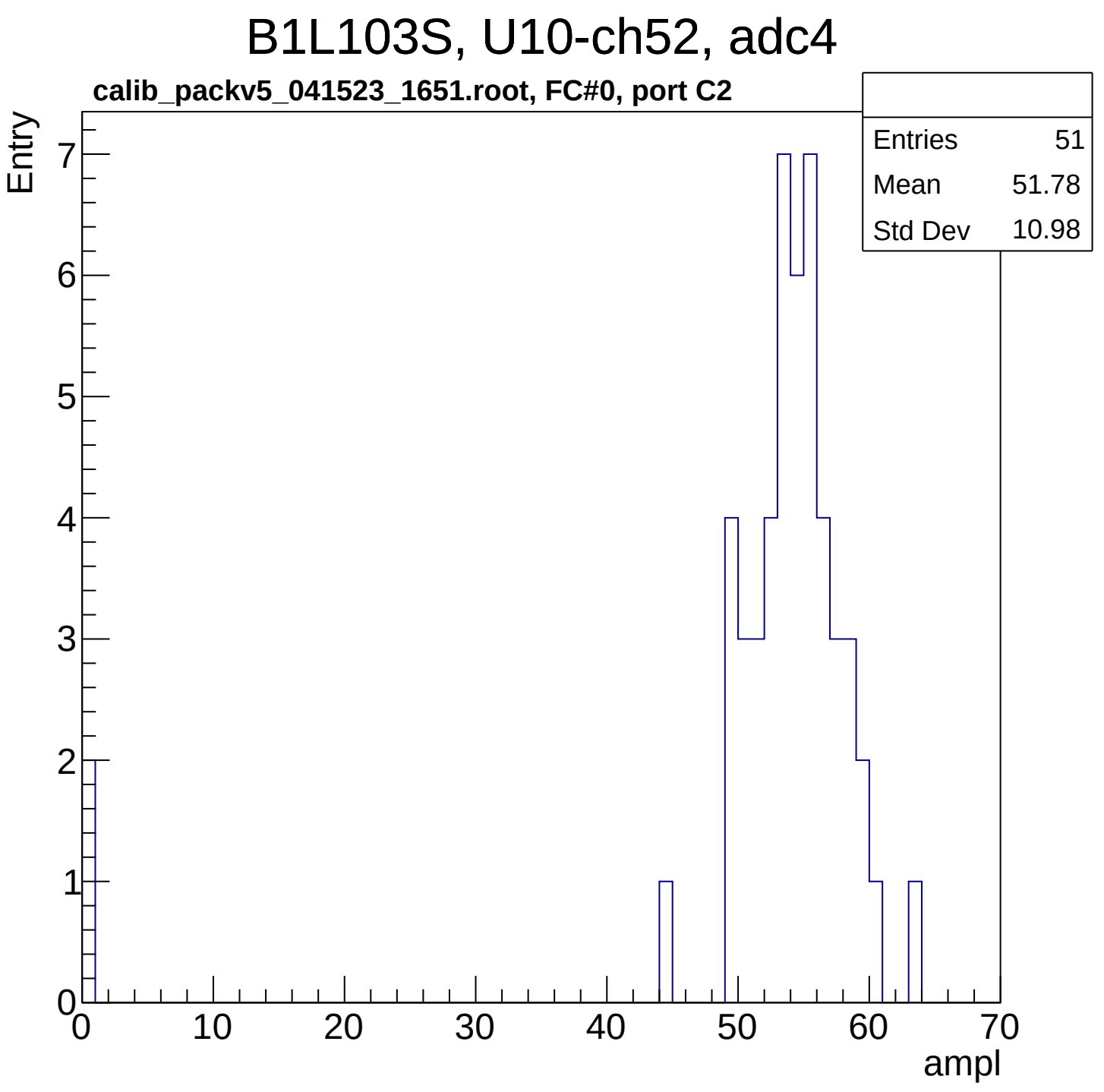
B1L103S, U10-ch52, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 51.78
Std Dev 10.98
Entry
ampl
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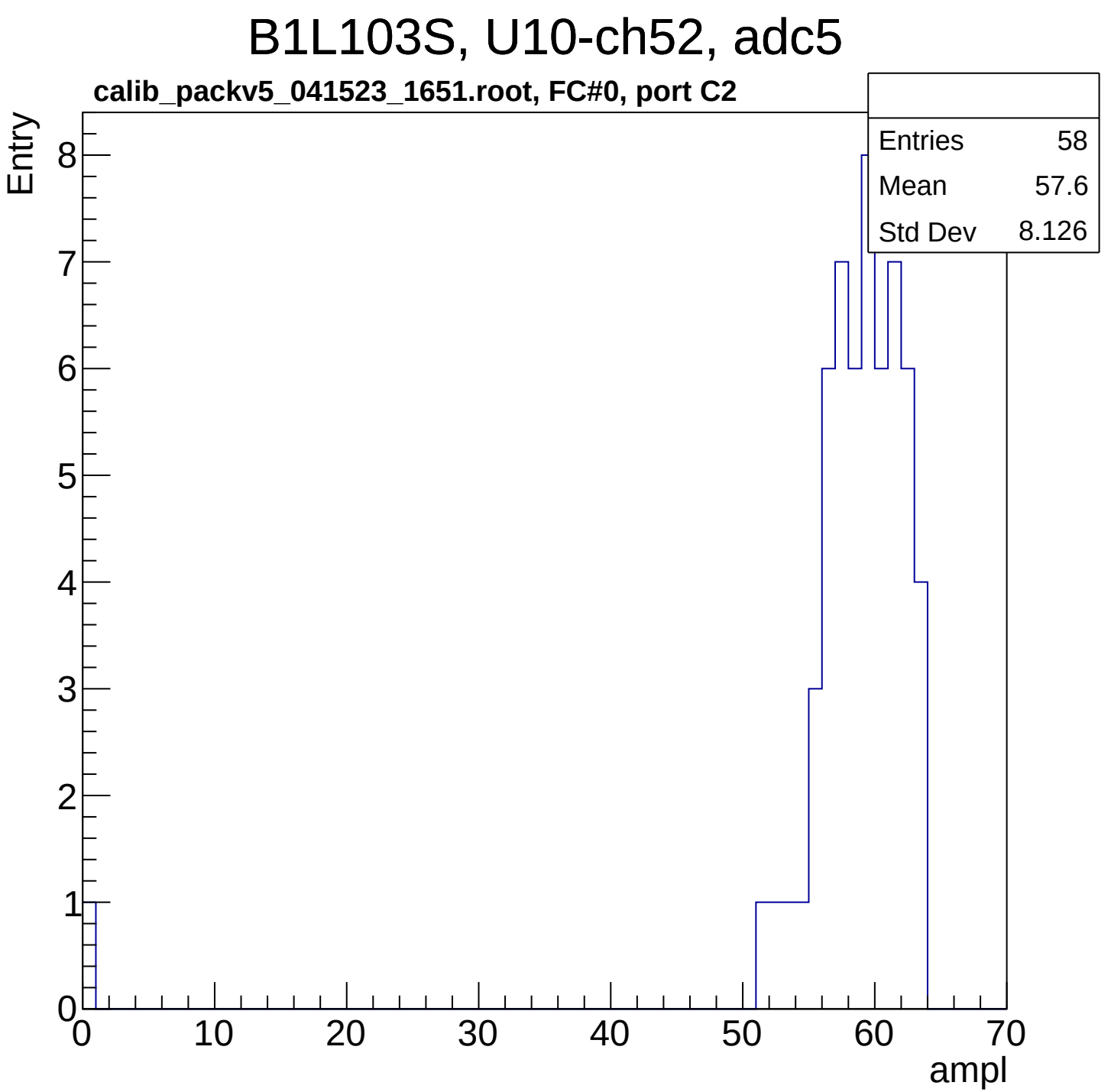
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U10-ch52, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 57.6
Std Dev 8.126
Entry
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3
4
5
6
7
8
0
10
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50
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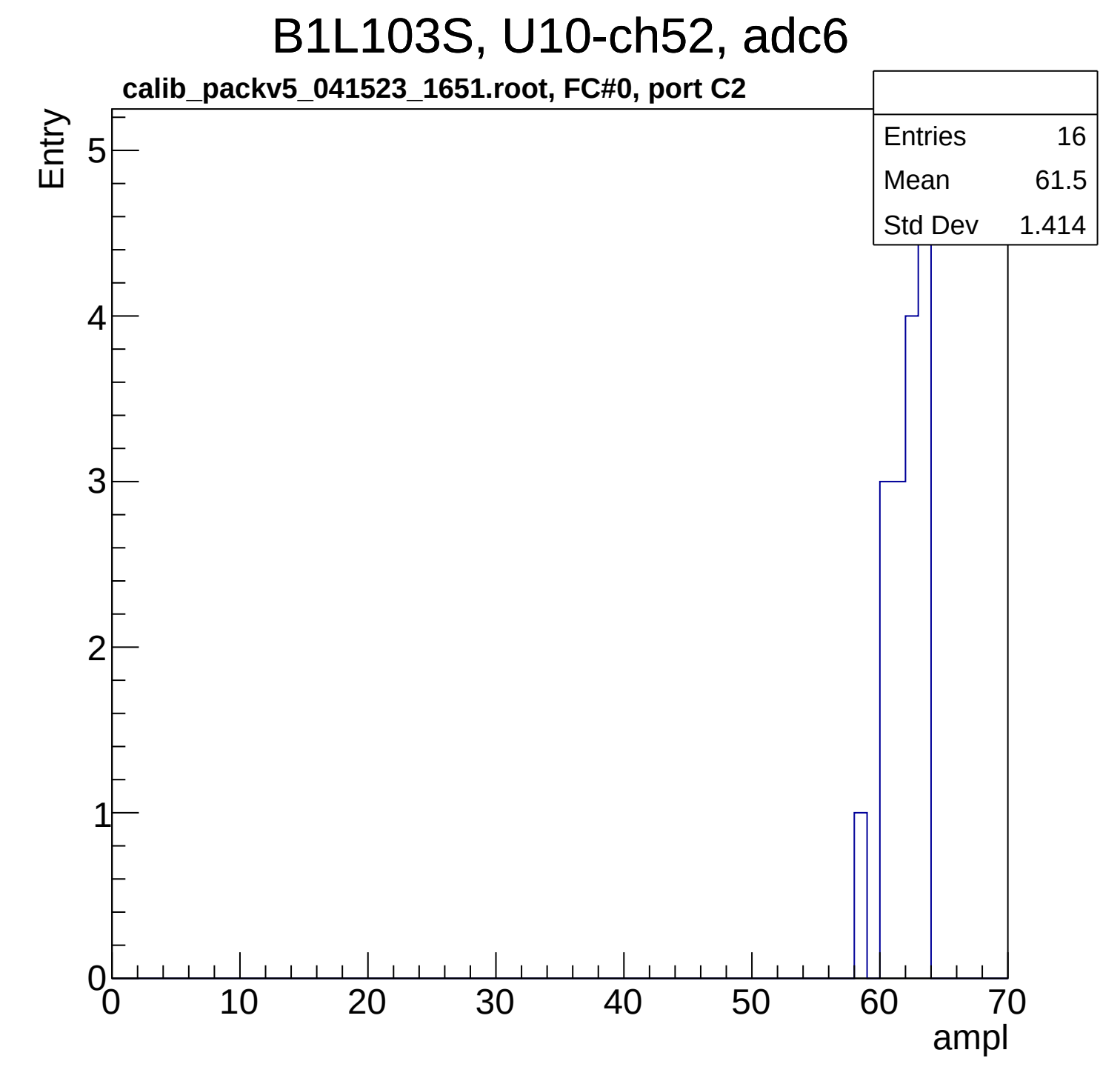
70
ampl


B1L103S, U10-ch52, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 16
Mean 61.5
Std Dev 1.414
Entry
ampl
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0
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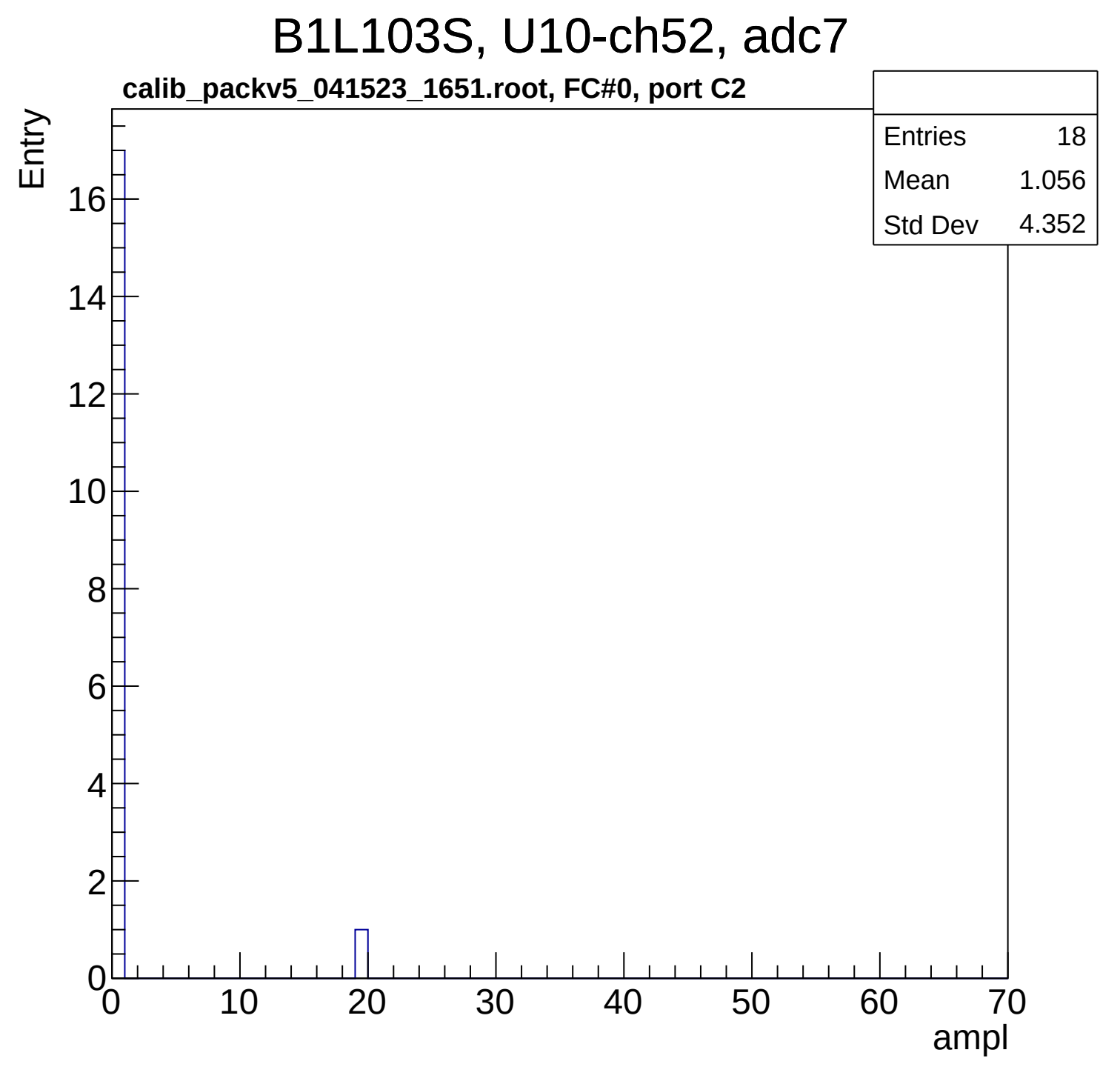
B1L103S, U10-ch52, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 1.056
Std Dev 4.352
Entry
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4
6
8
10
12
14
16
0
10
20
30
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50
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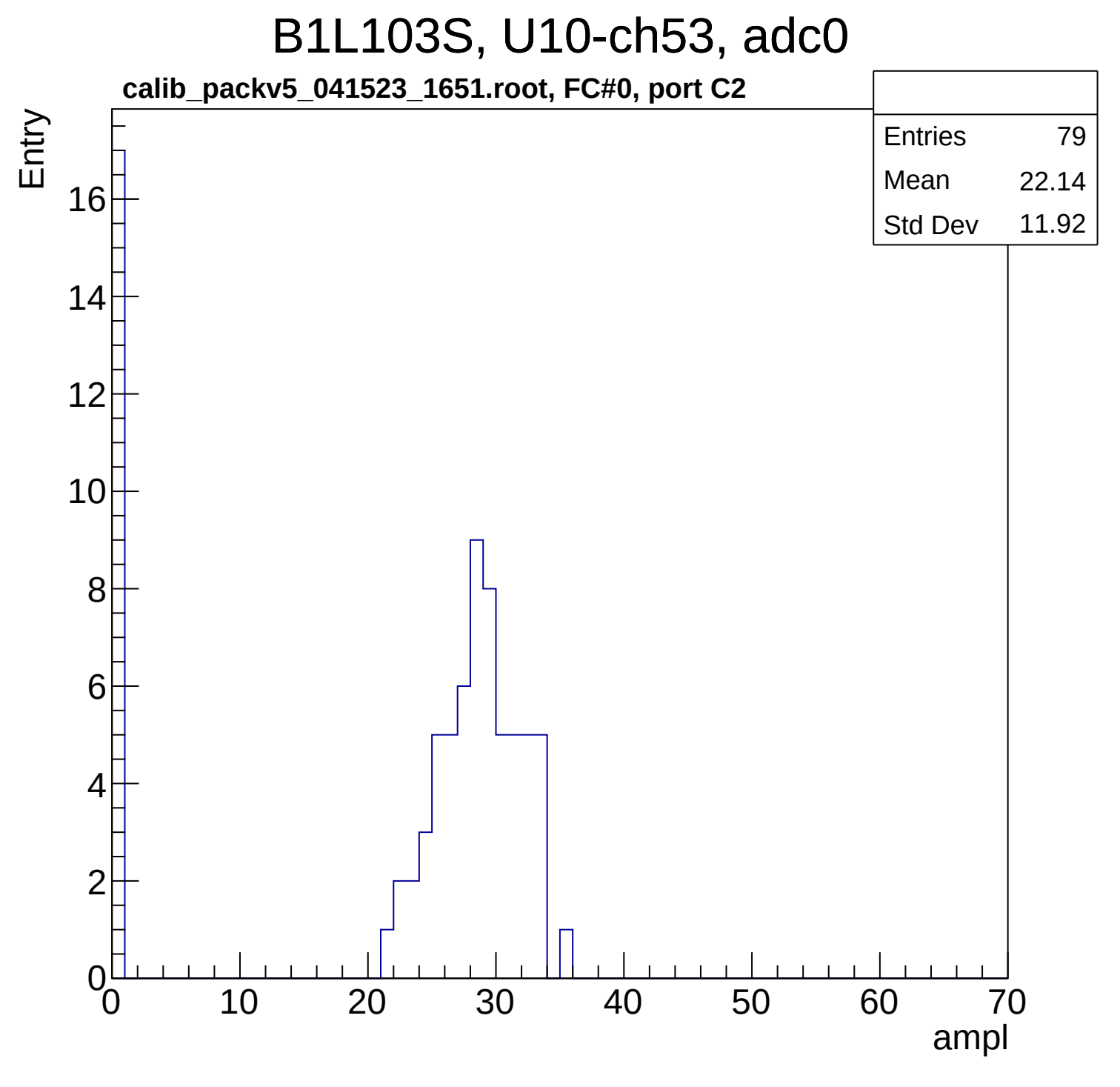
70
ampl


B1L103S, U10-ch53, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 22.14
Std Dev 11.92
Entry
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4
6
8
10
12
14
16
0
10
20
30
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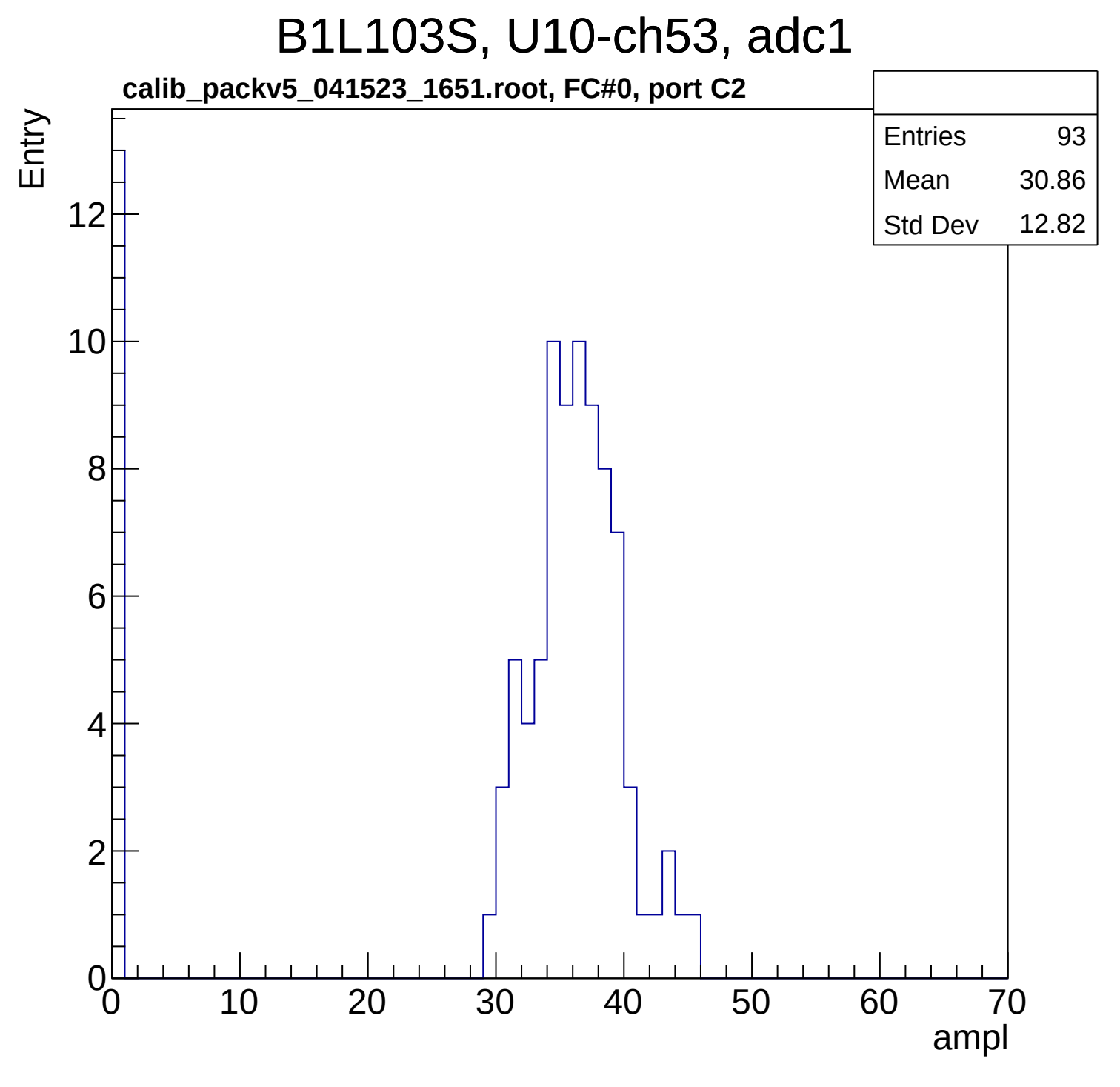
50
60
70
ampl


B1L103S, U10-ch53, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 93
Mean 30.86
Std Dev 12.82
Entry
ampl
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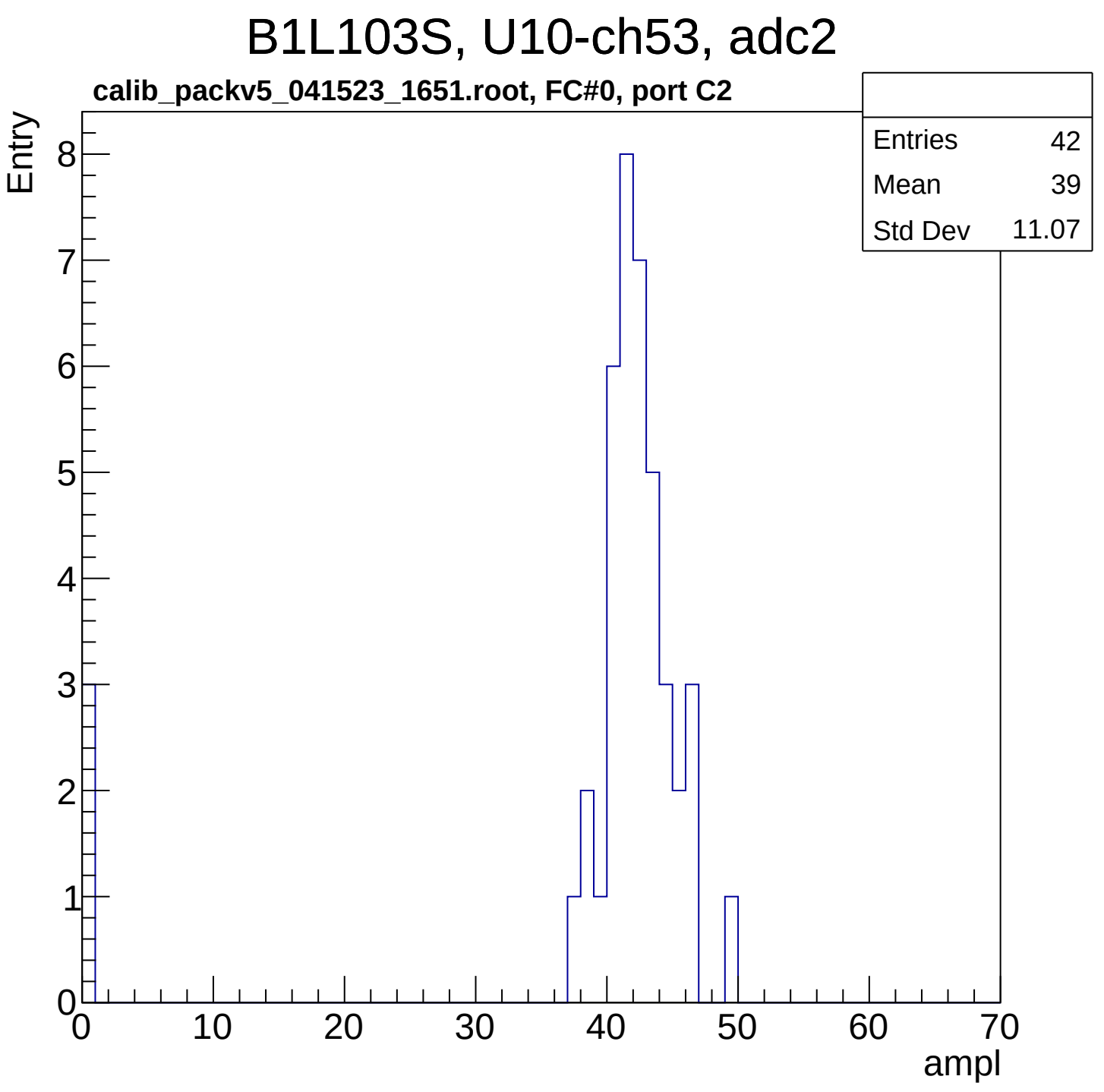
6
8
10
12
0
10
20
30
40
50
60
70


B1L103S, U10-ch53, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 42
Mean 39
Std Dev 11.07
Entry
ampl
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2
3
4
5
6
7
8
0
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20
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40
50
60
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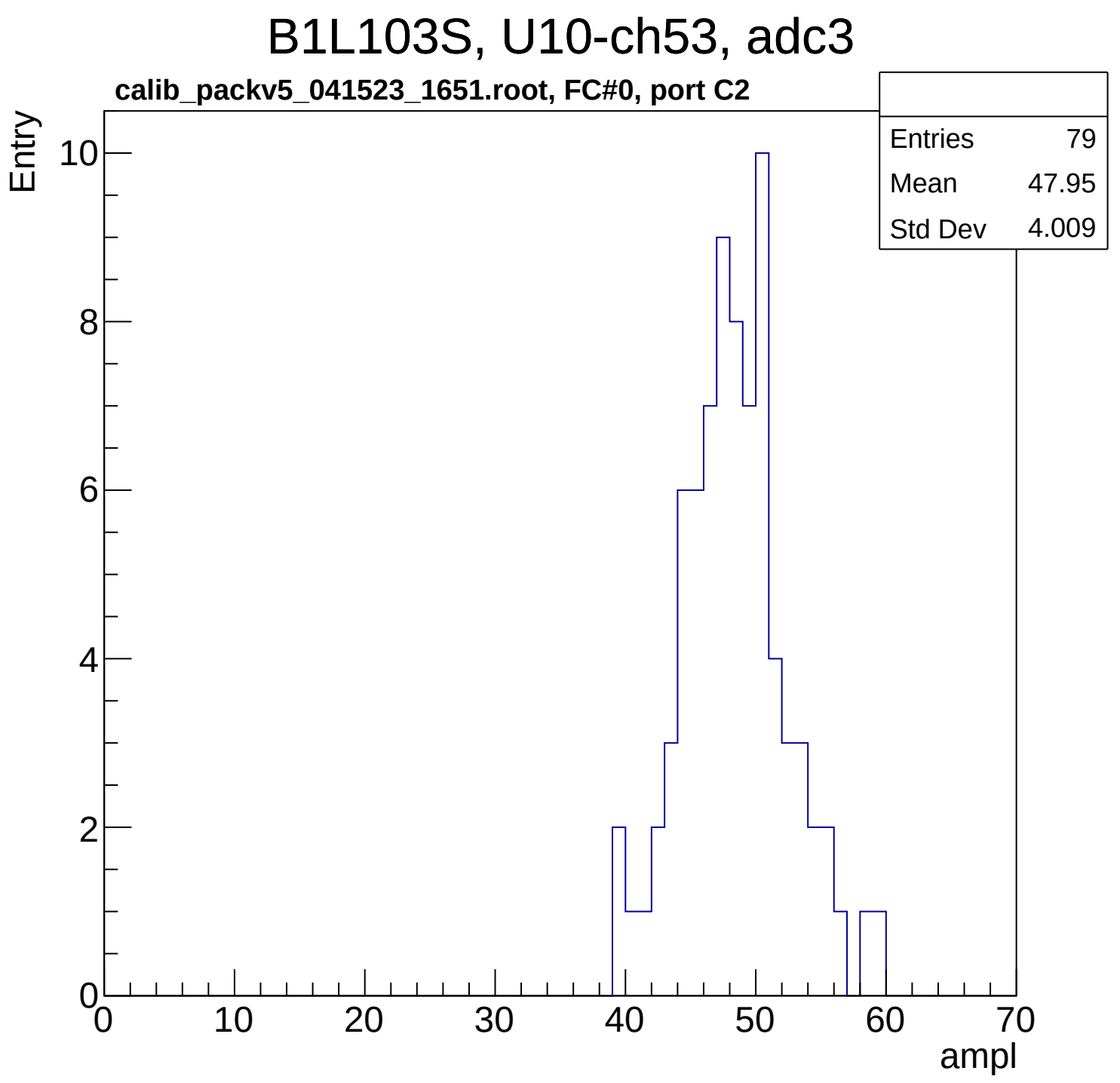
B1L103S, U10-ch53, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 47.95
Std Dev 4.009
Entry
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2
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6
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10
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10
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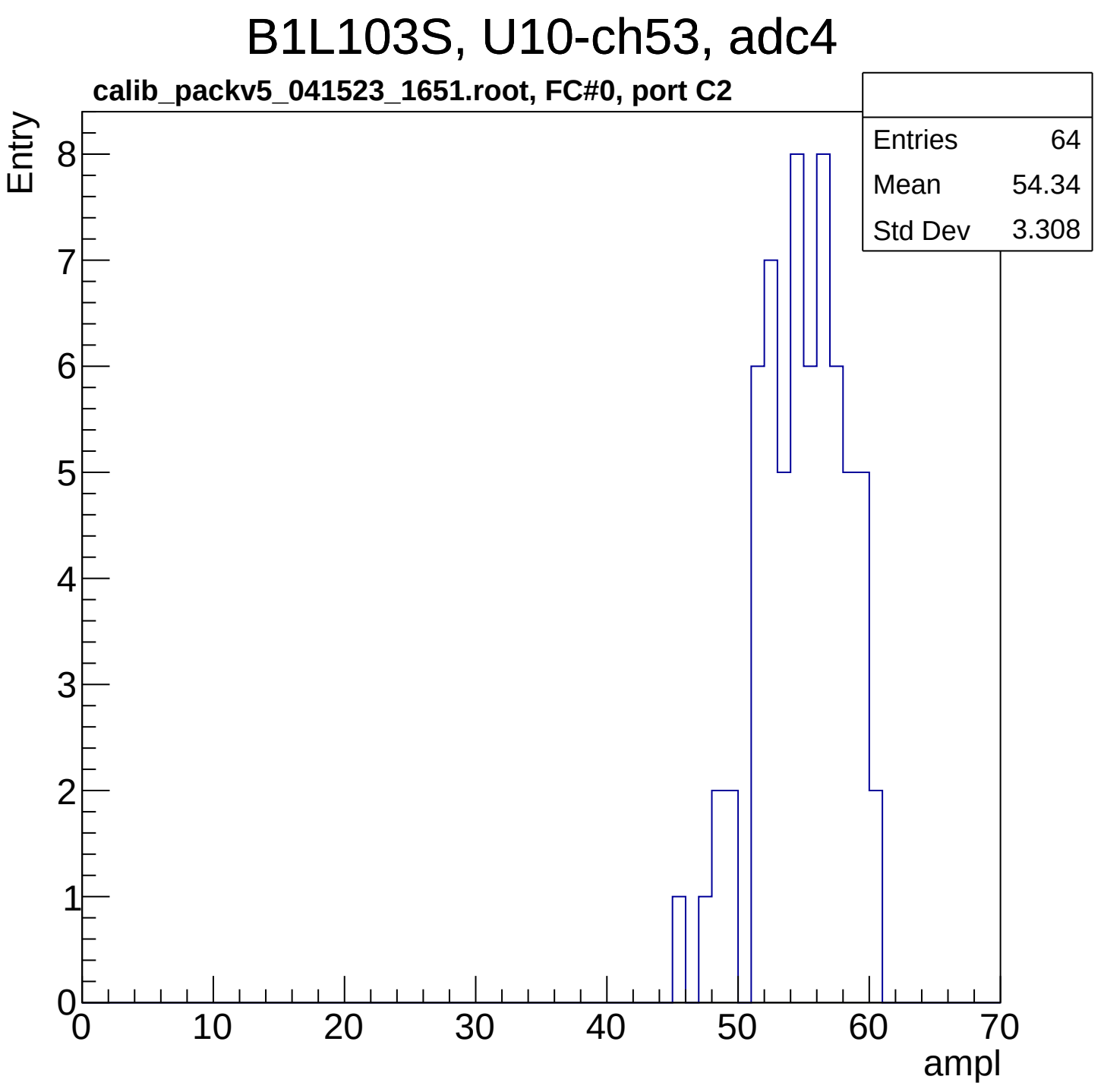
50
60
70
ampl


B1L103S, U10-ch53, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 54.34
Std Dev 3.308
Entry
ampl
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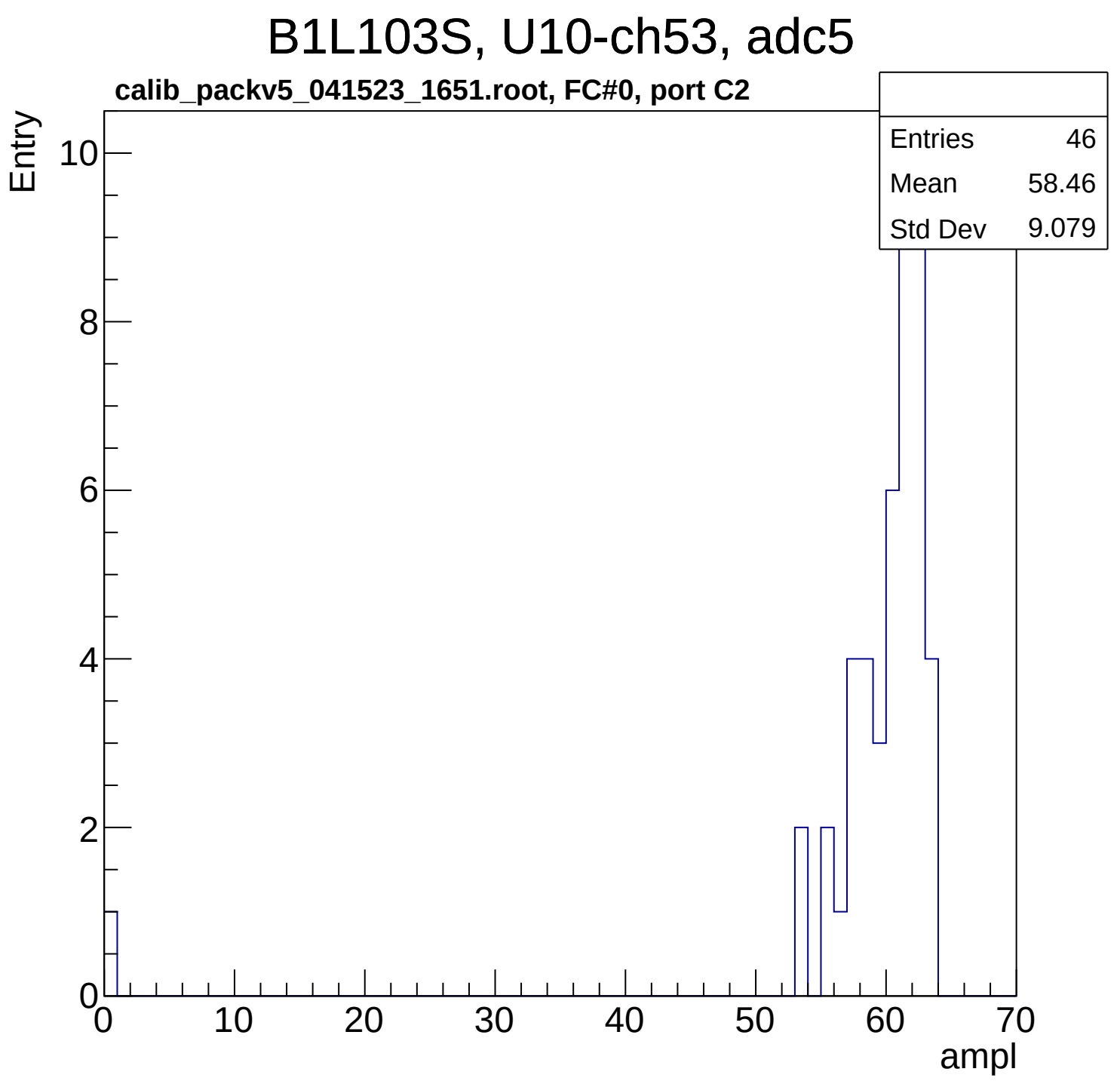
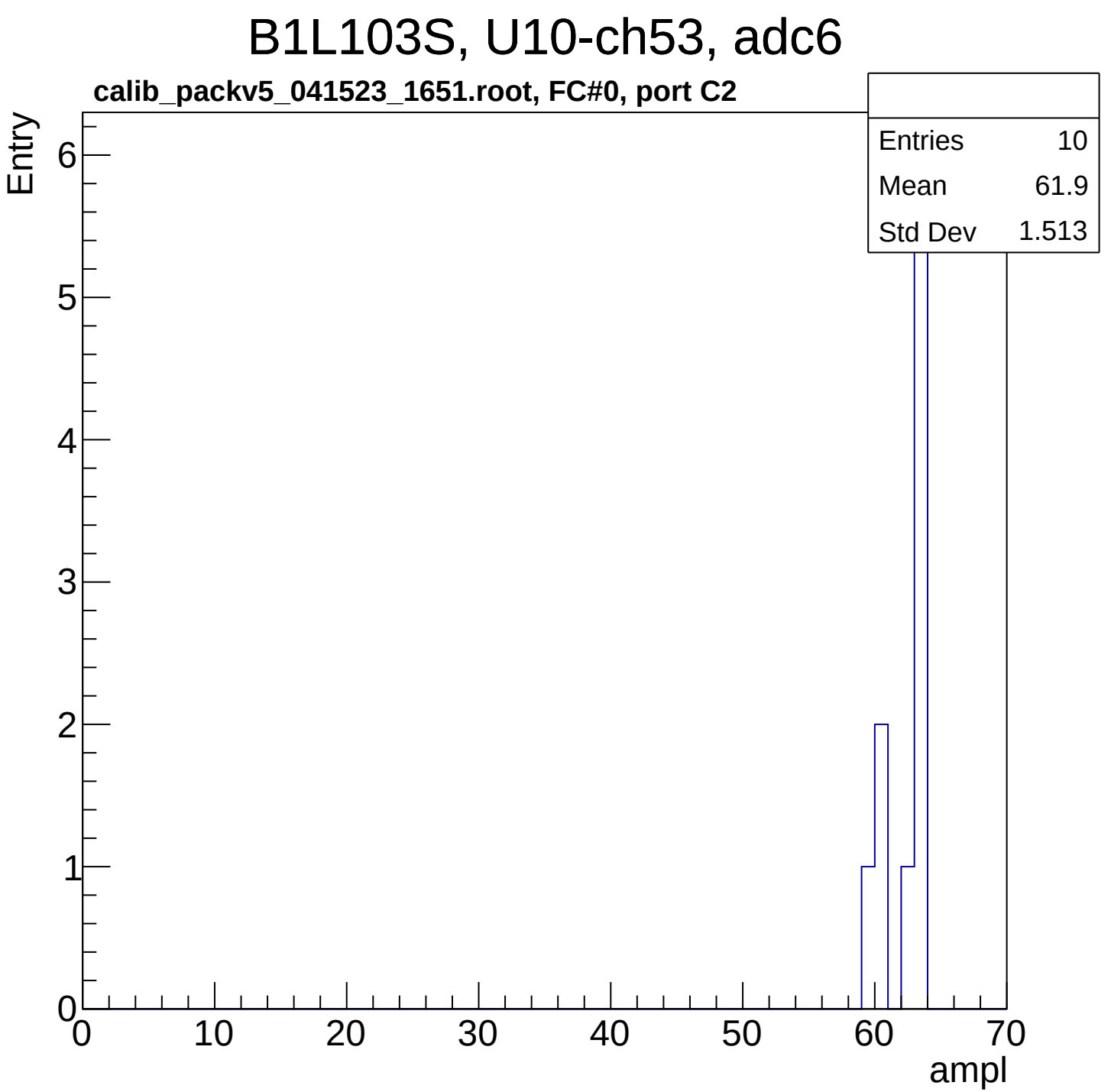
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U10-ch53, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 58.46
Std Dev 9.079
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch53, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 61.9
Std Dev 1.513
Entry
0
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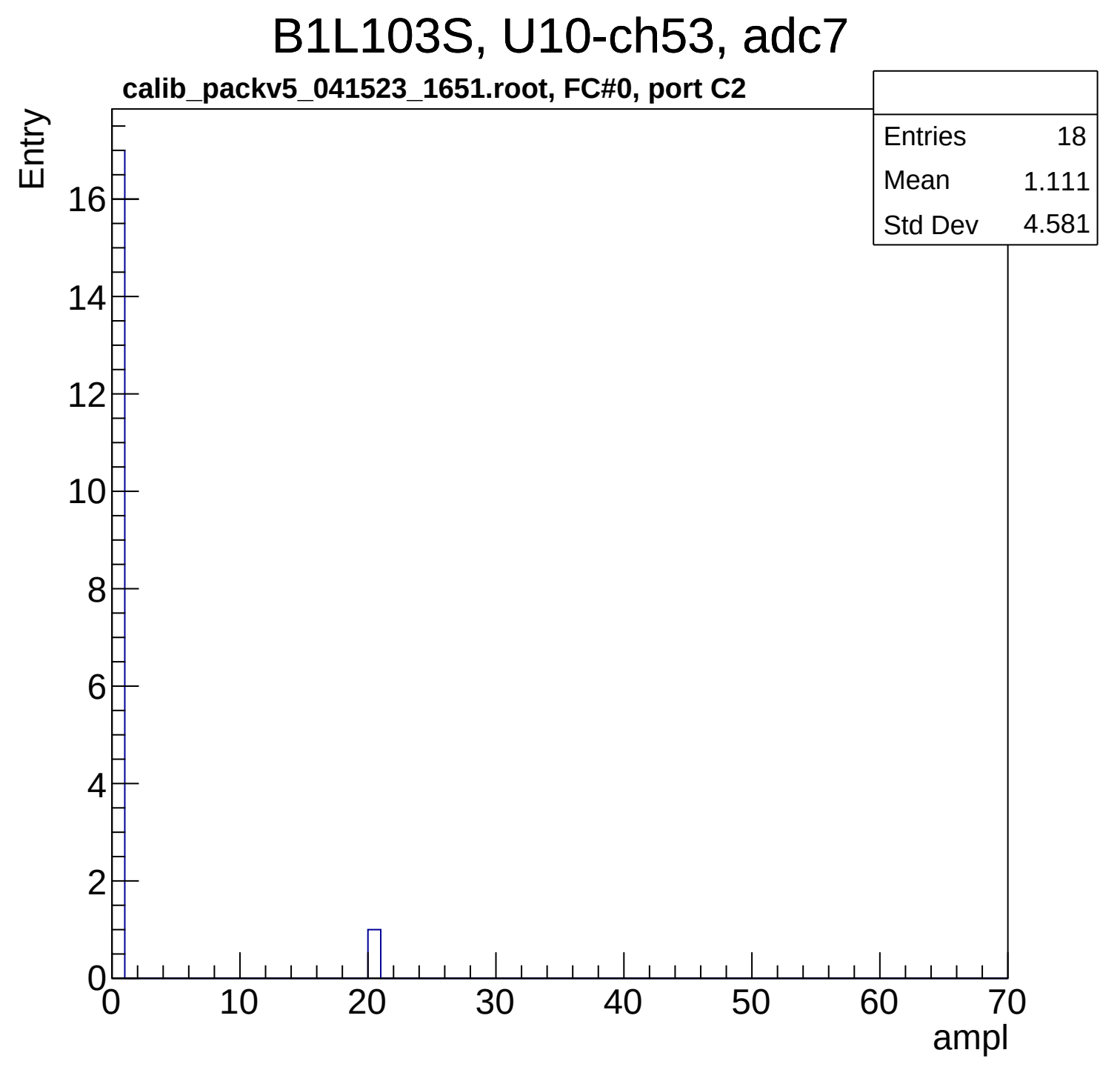
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch53, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 1.111
Std Dev 4.581
Entry
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4
6
8
10
12
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16
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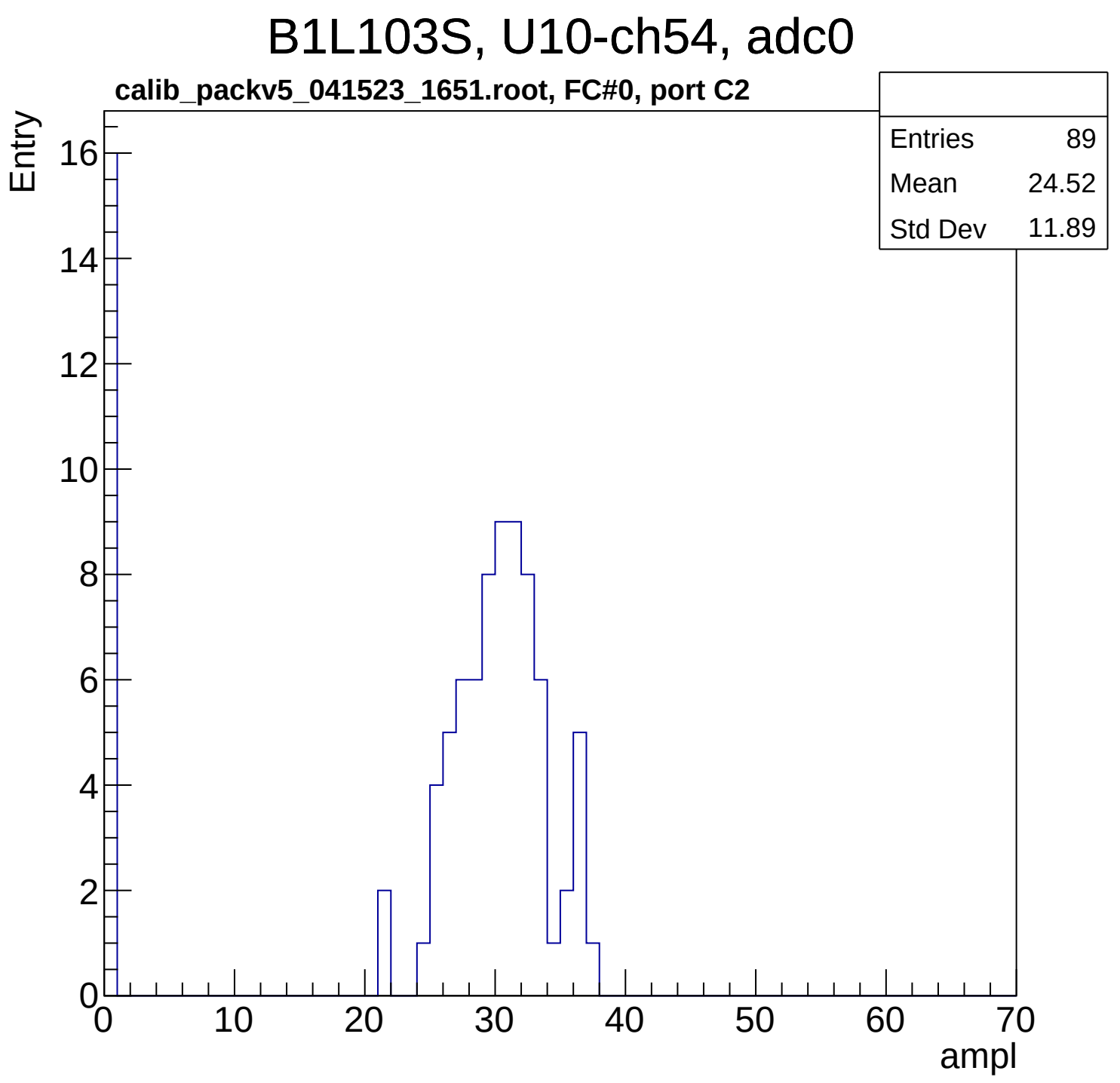
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch54, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 89
Mean 24.52
Std Dev 11.89
Entry
ampl
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2
4
6
8
10
12
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16
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10
20
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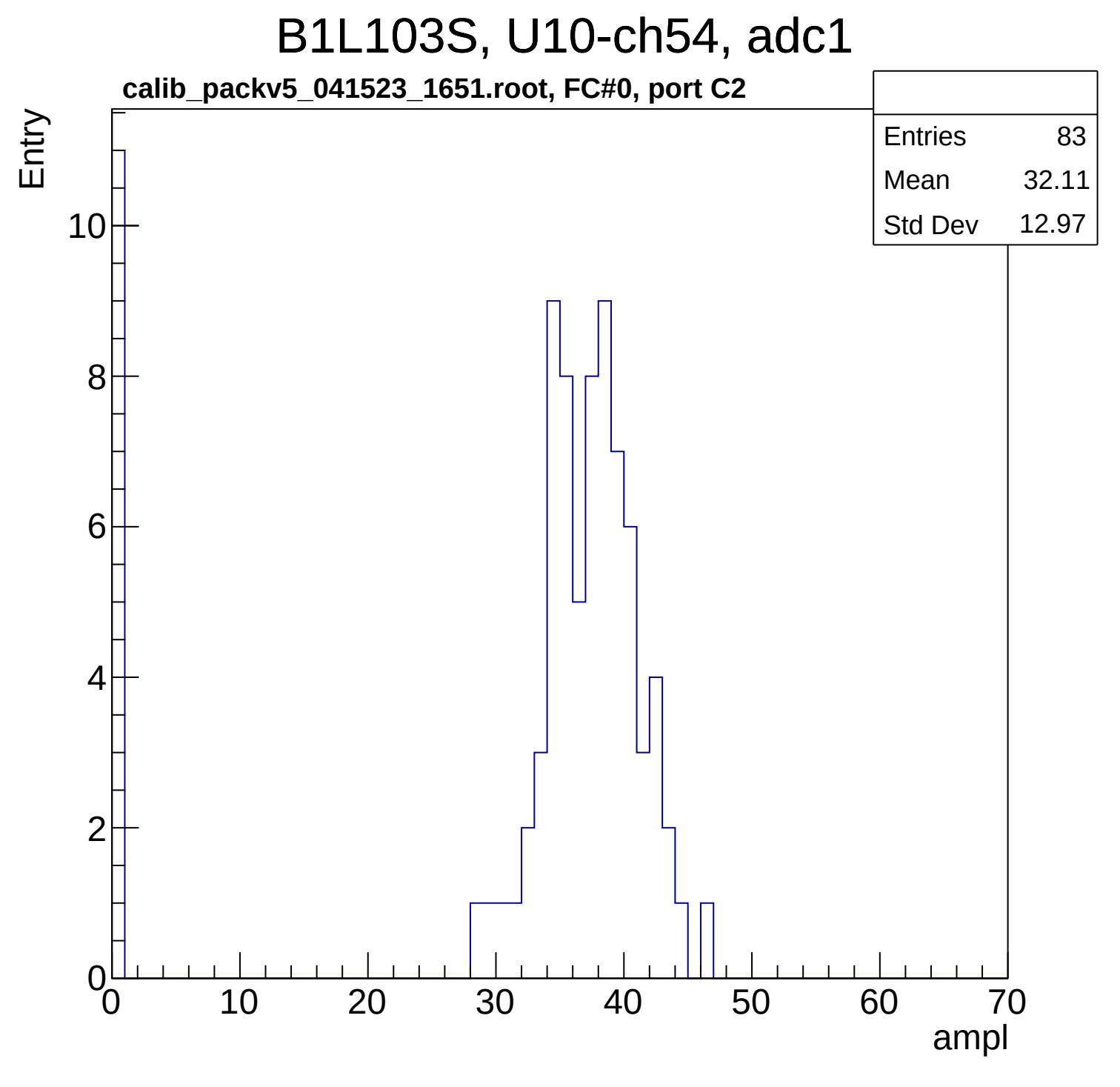
40
50
60
70


B1L103S, U10-ch54, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 32.11
Std Dev 12.97
Entry
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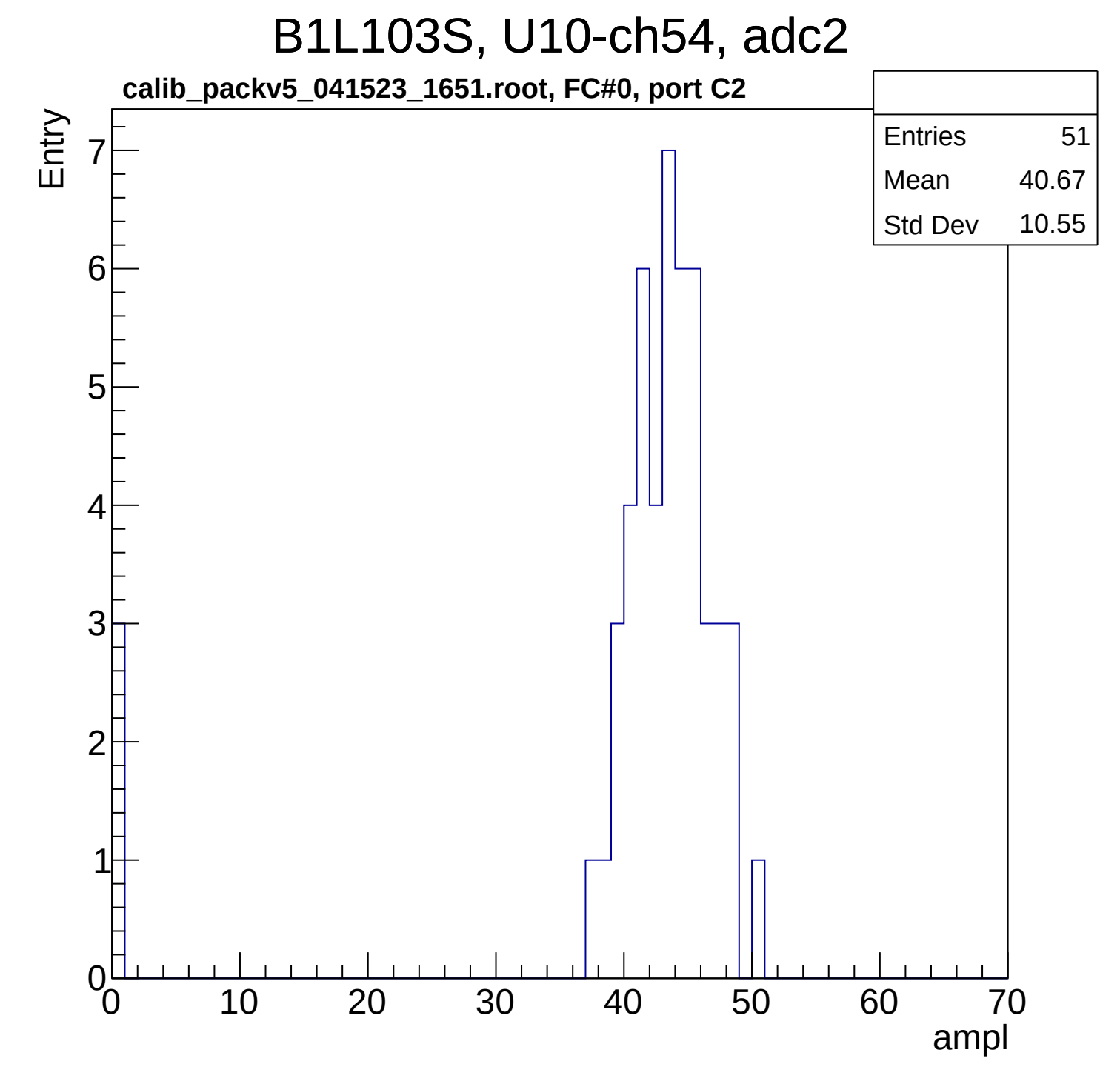
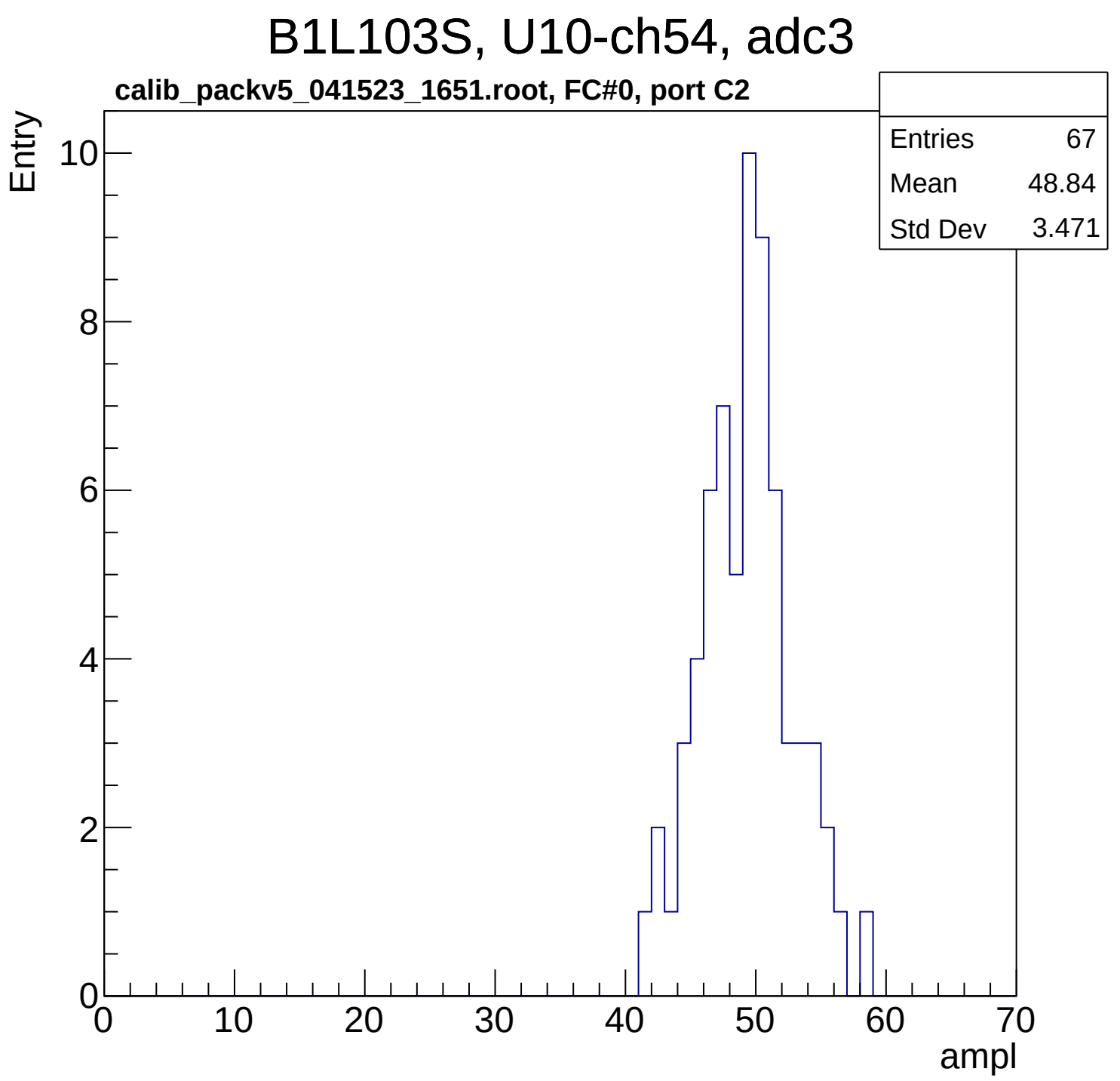
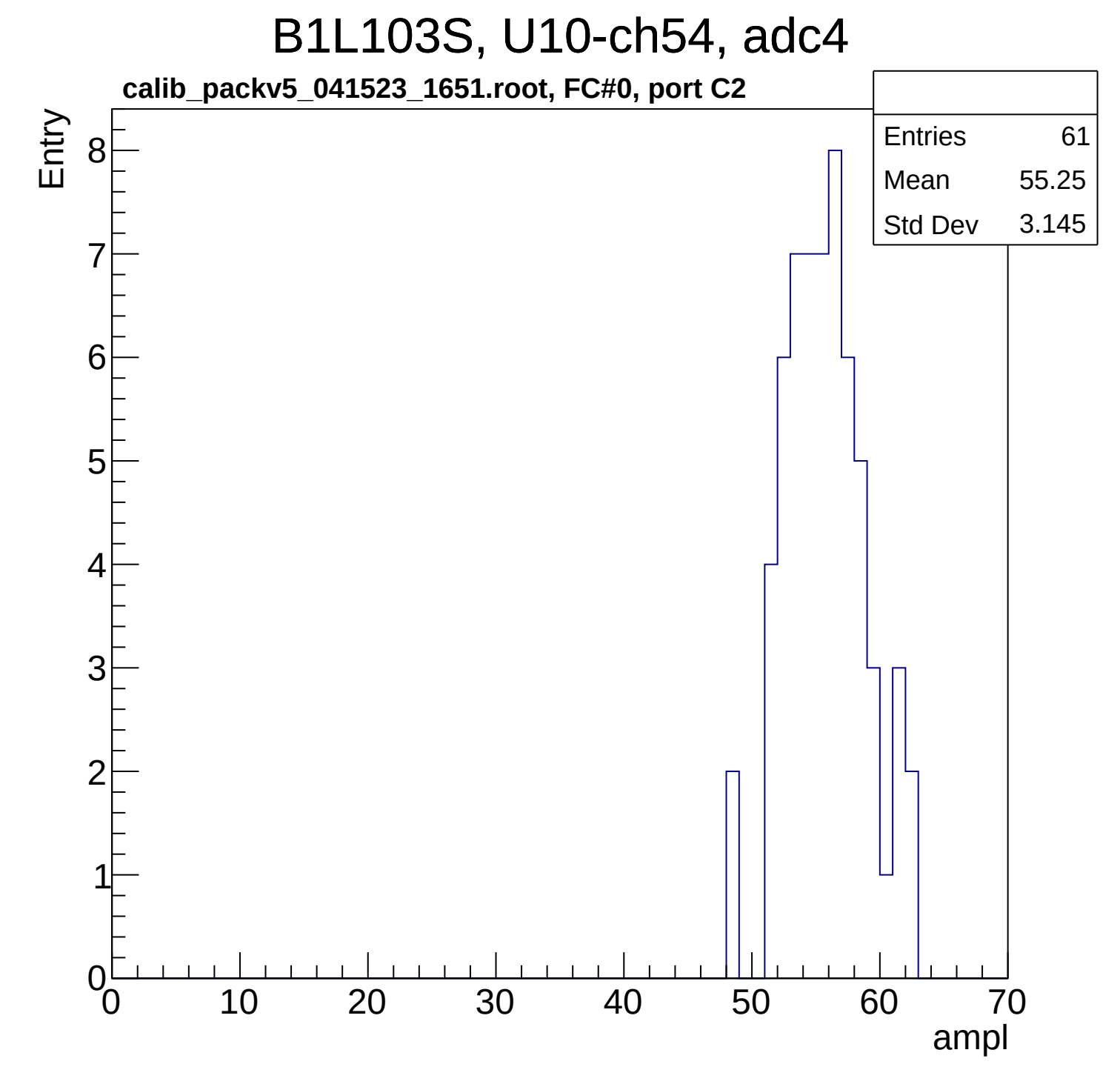
60
70
ampl


B1L103S, U10-ch54, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 40.67
Std Dev 10.55
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U10-ch54, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 48.84
Std Dev 3.471
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U10-ch54, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 55.25
Std Dev 3.145
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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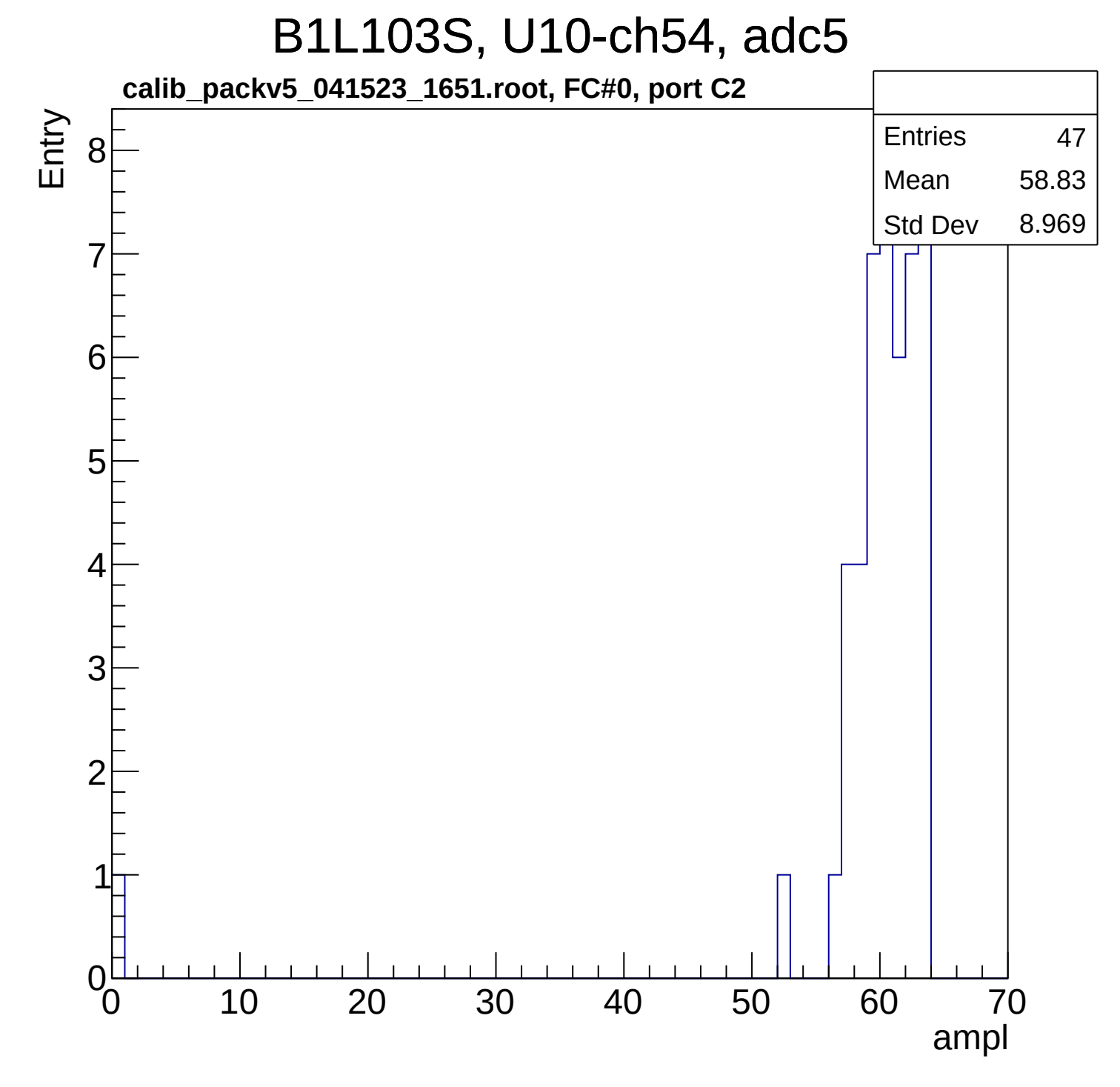
B1L103S, U10-ch54, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 58.83
Std Dev 8.969
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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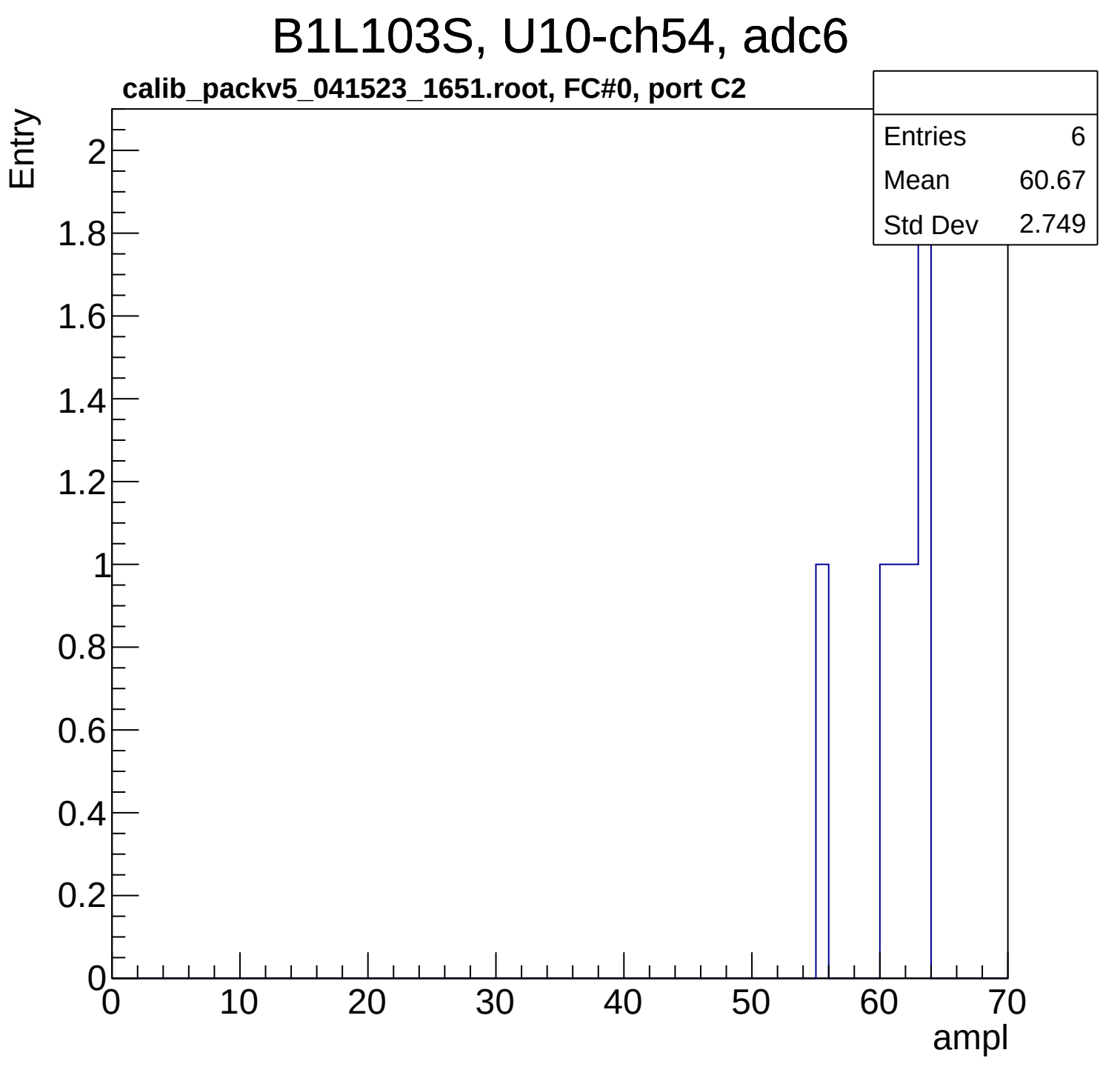
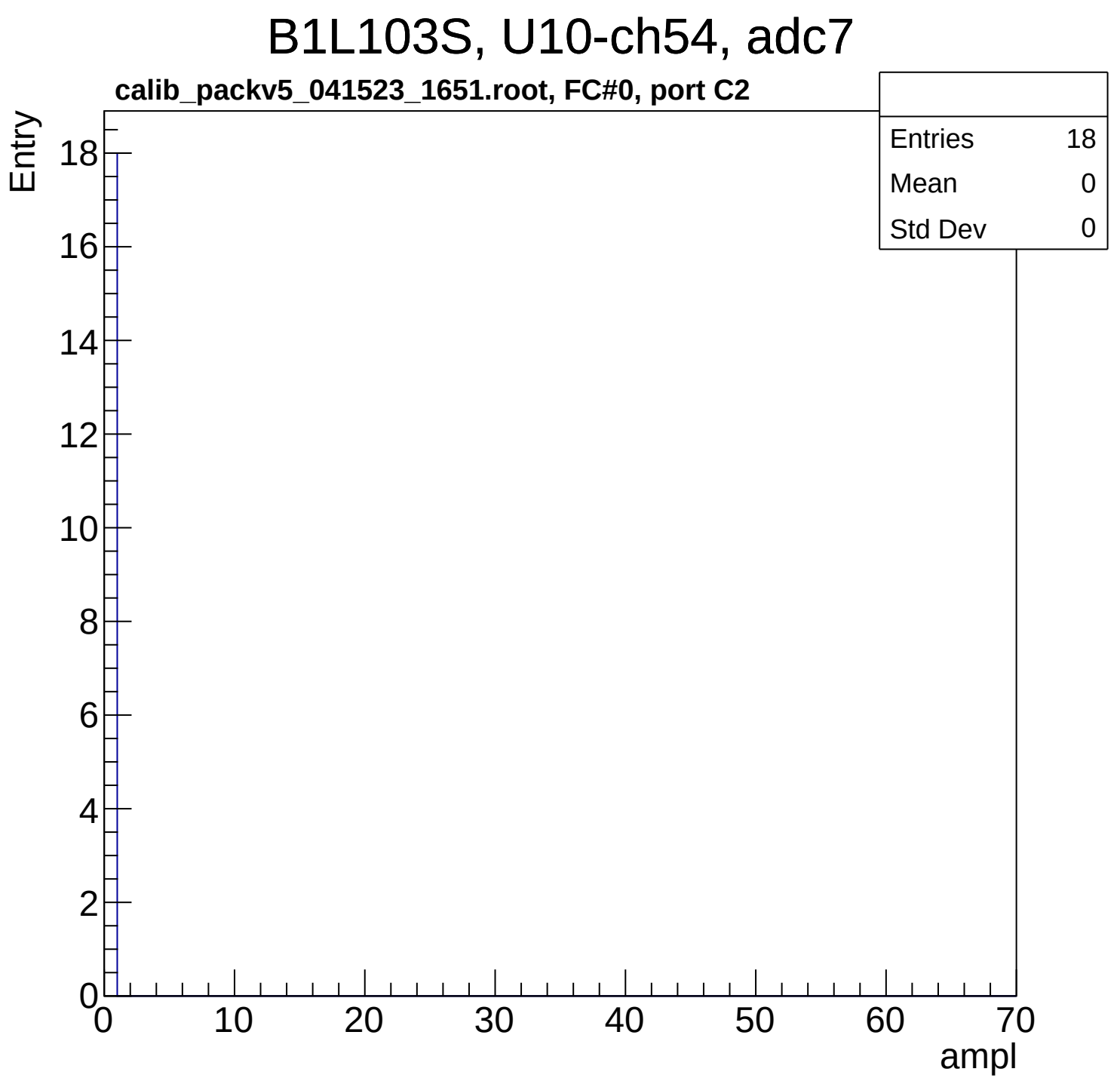
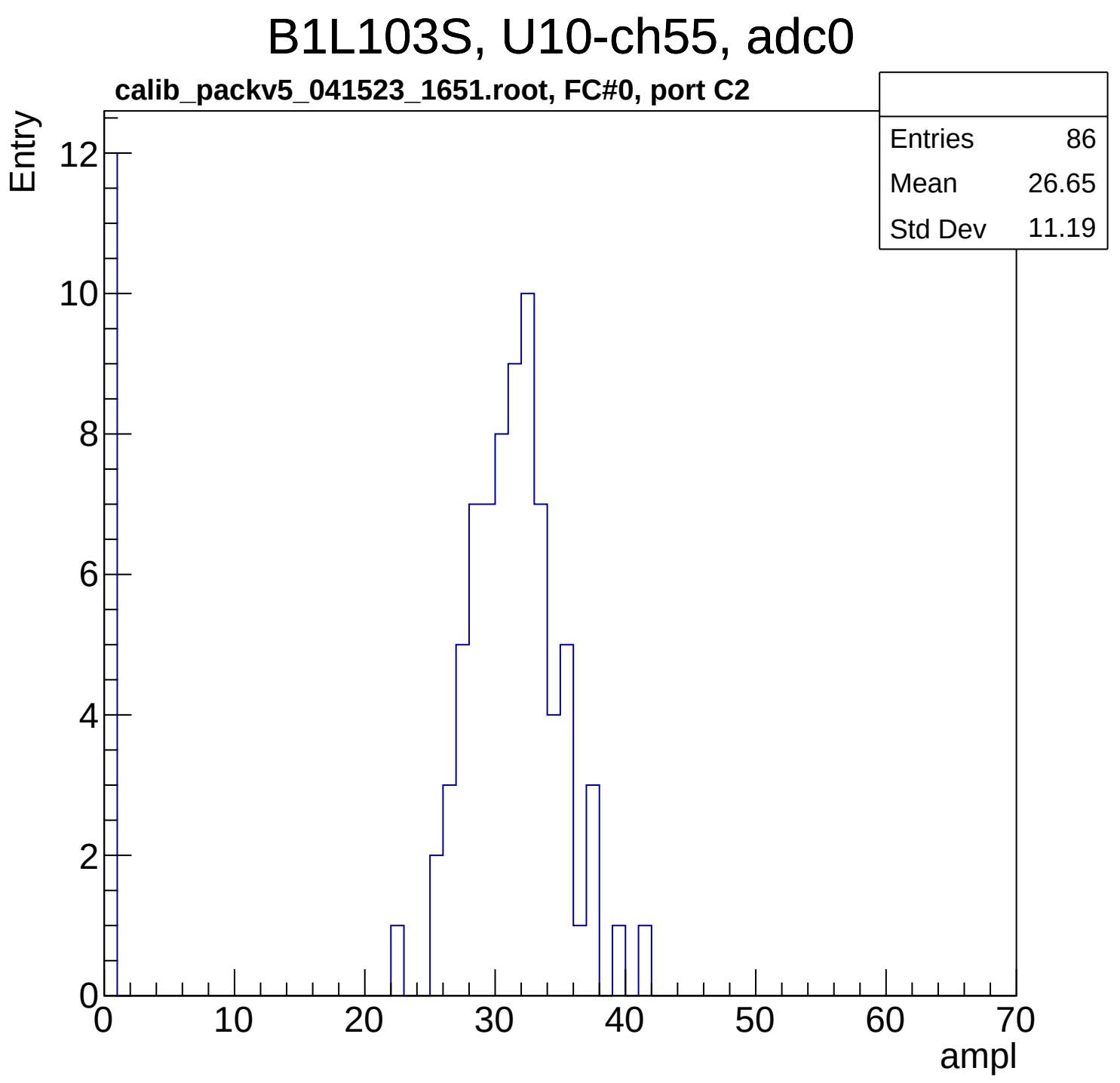
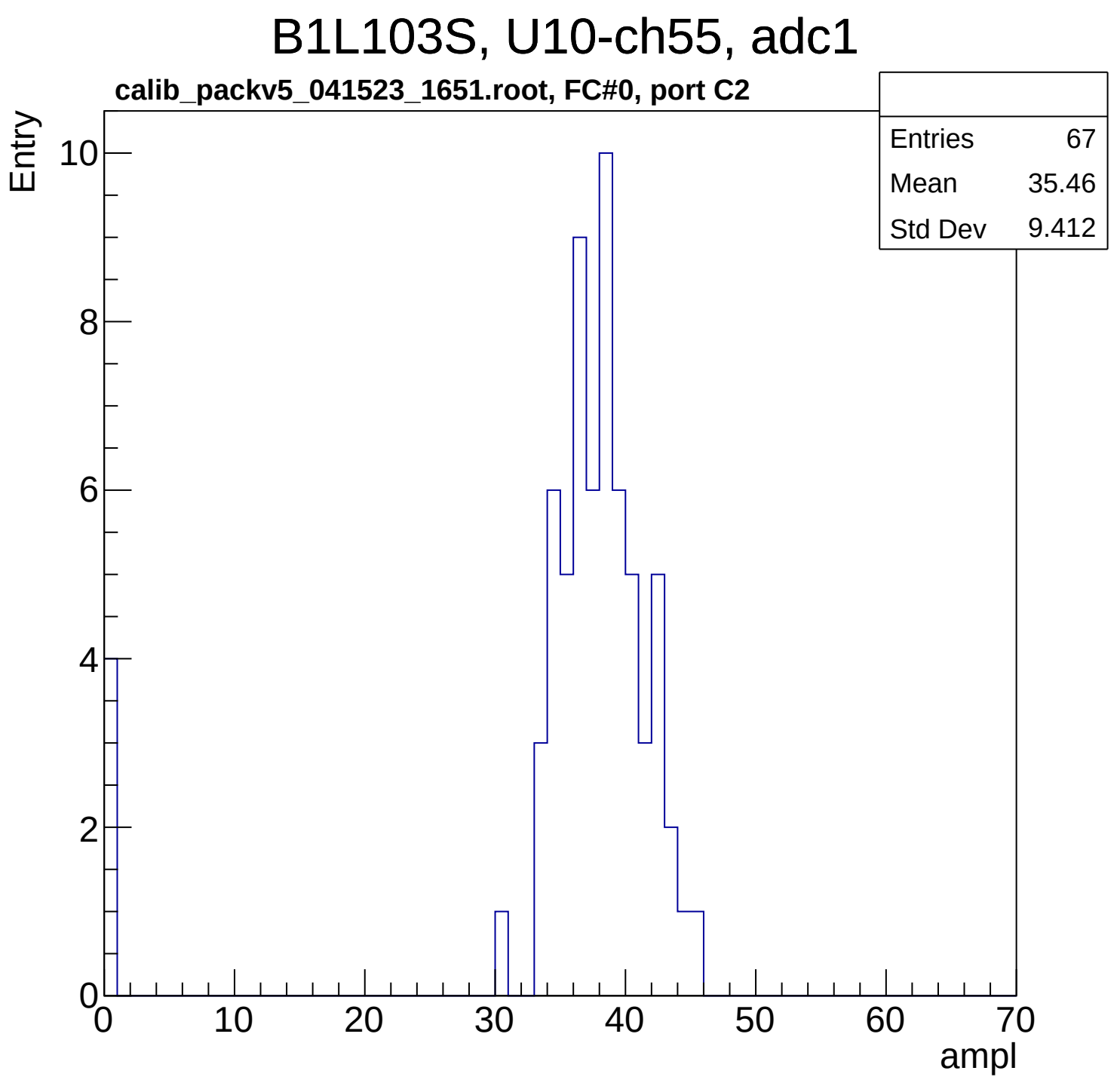

B1L103S, U10-ch54, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 60.67
Std Dev 2.749
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U10-ch54, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch55, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 26.65
Std Dev 11.19
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch55, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 35.46
Std Dev 9.412
Entry
ampl
0
2
4
6
8
10
0
10
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40
50
60
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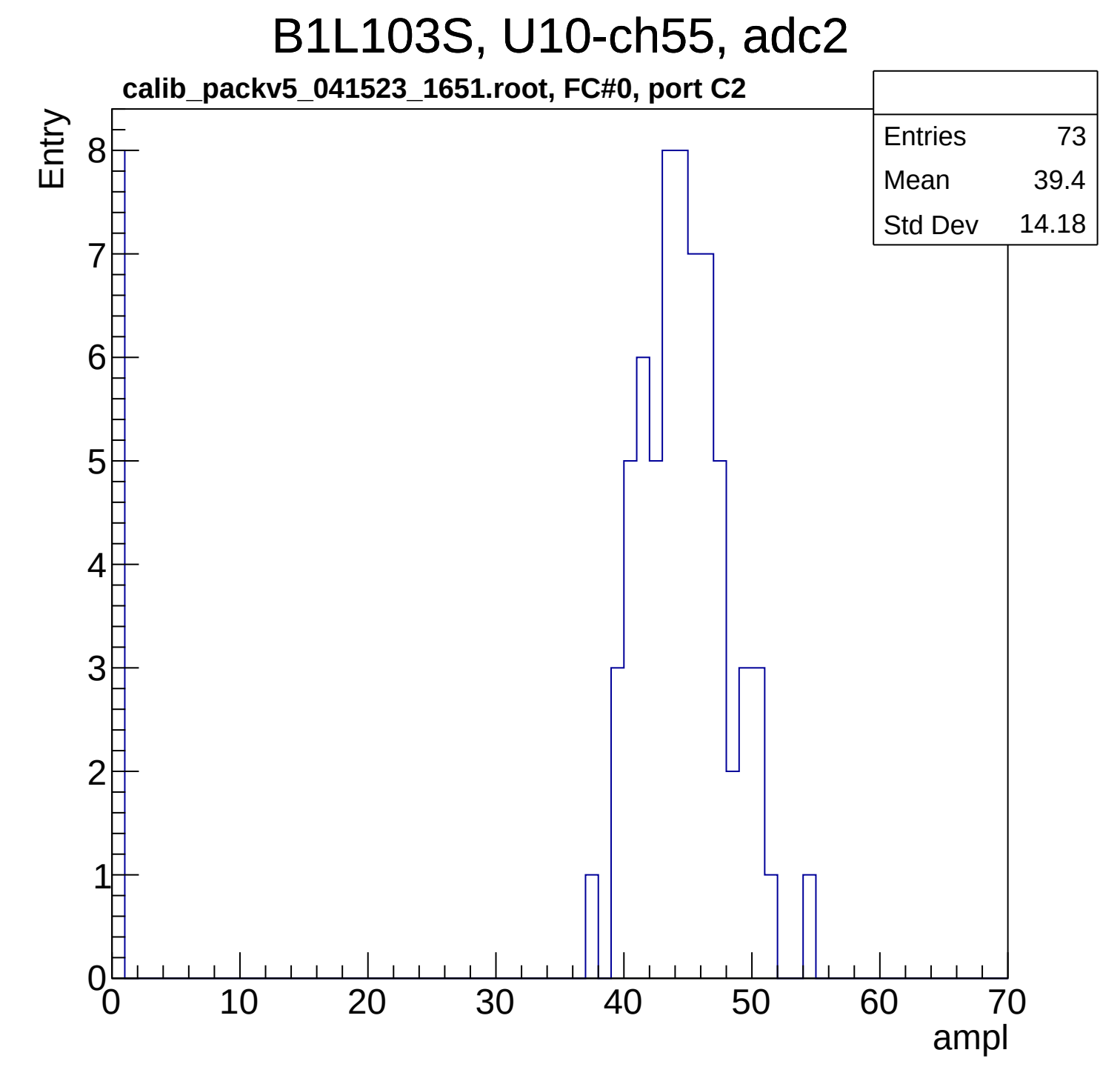
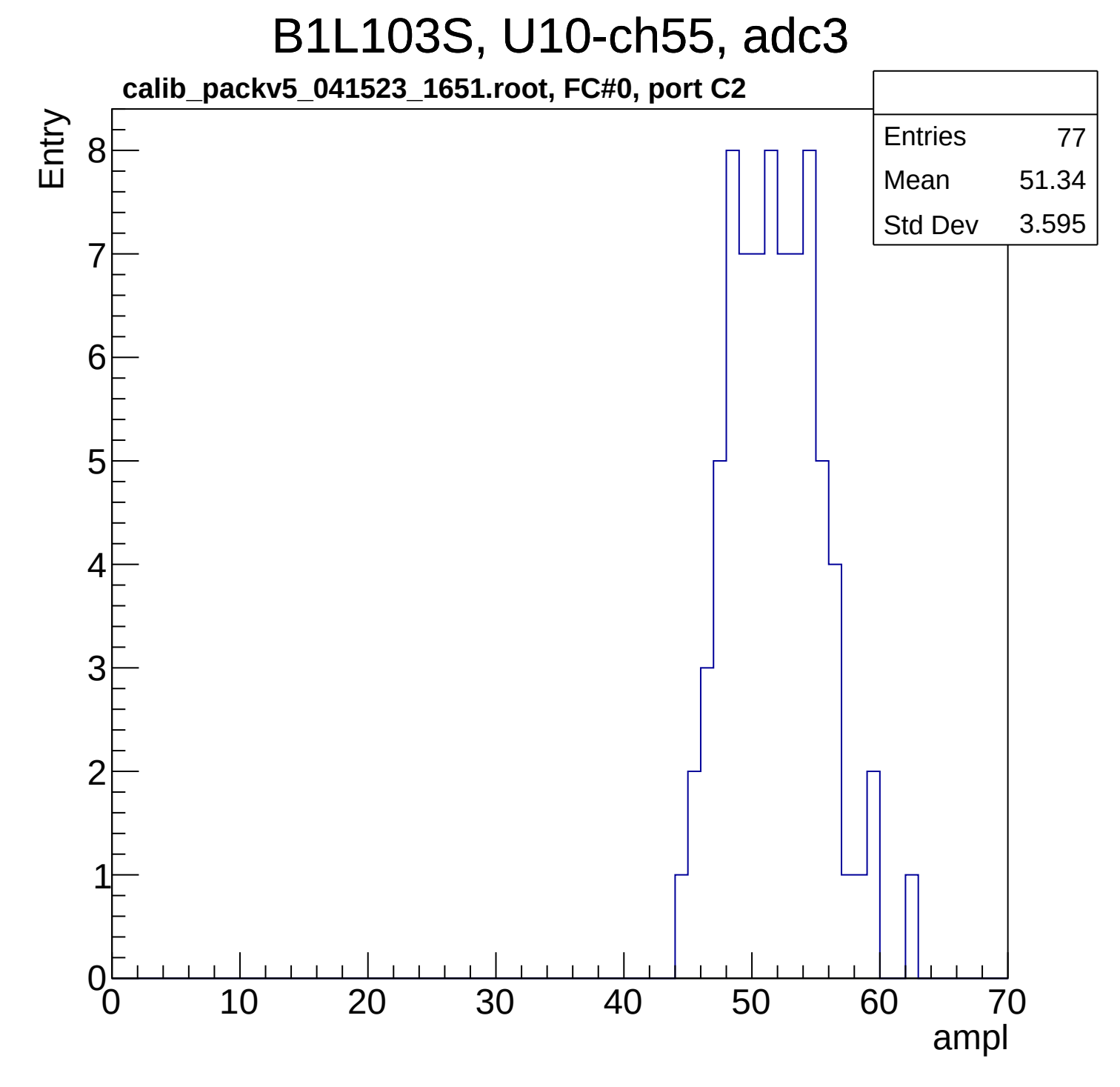
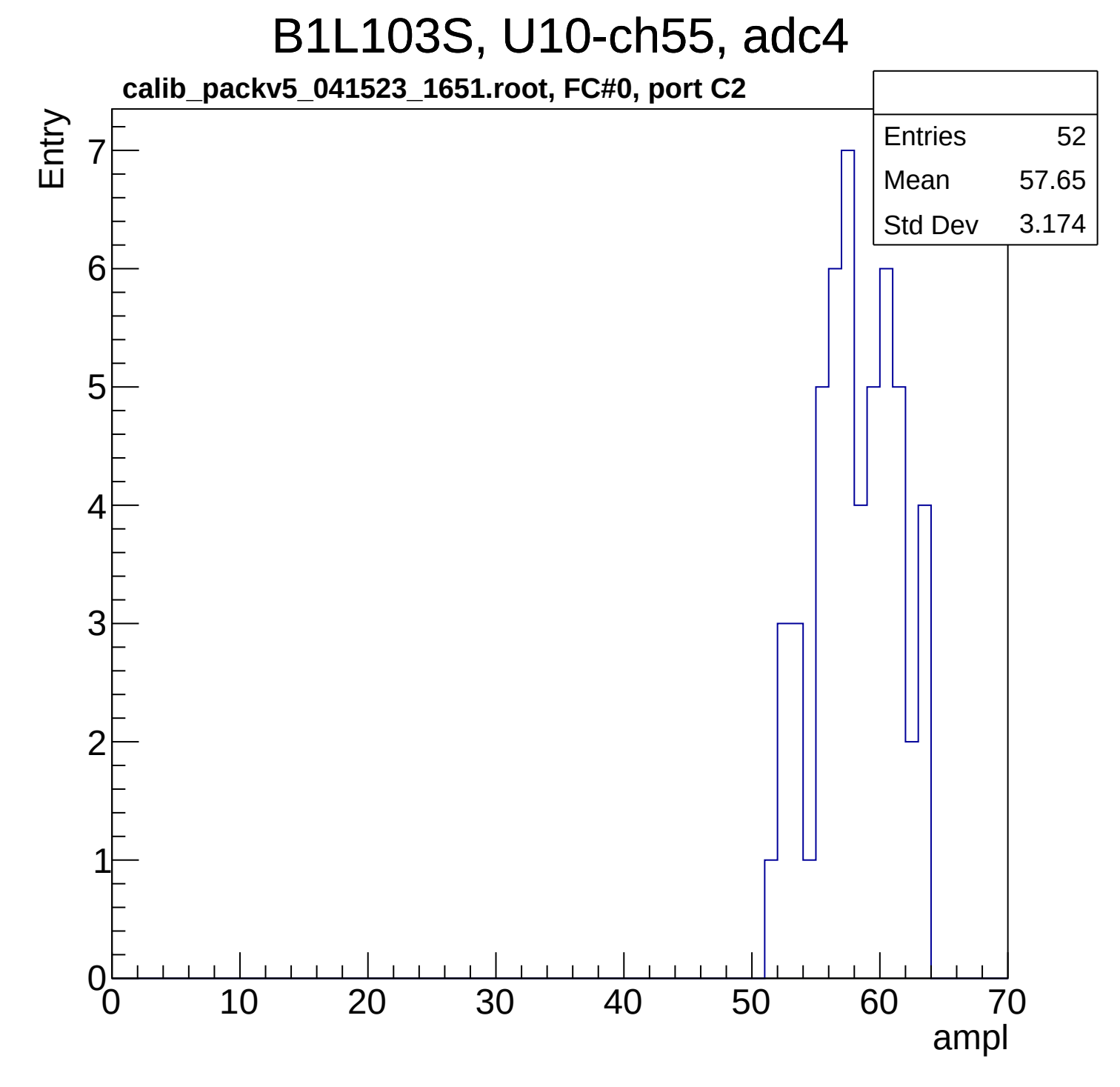
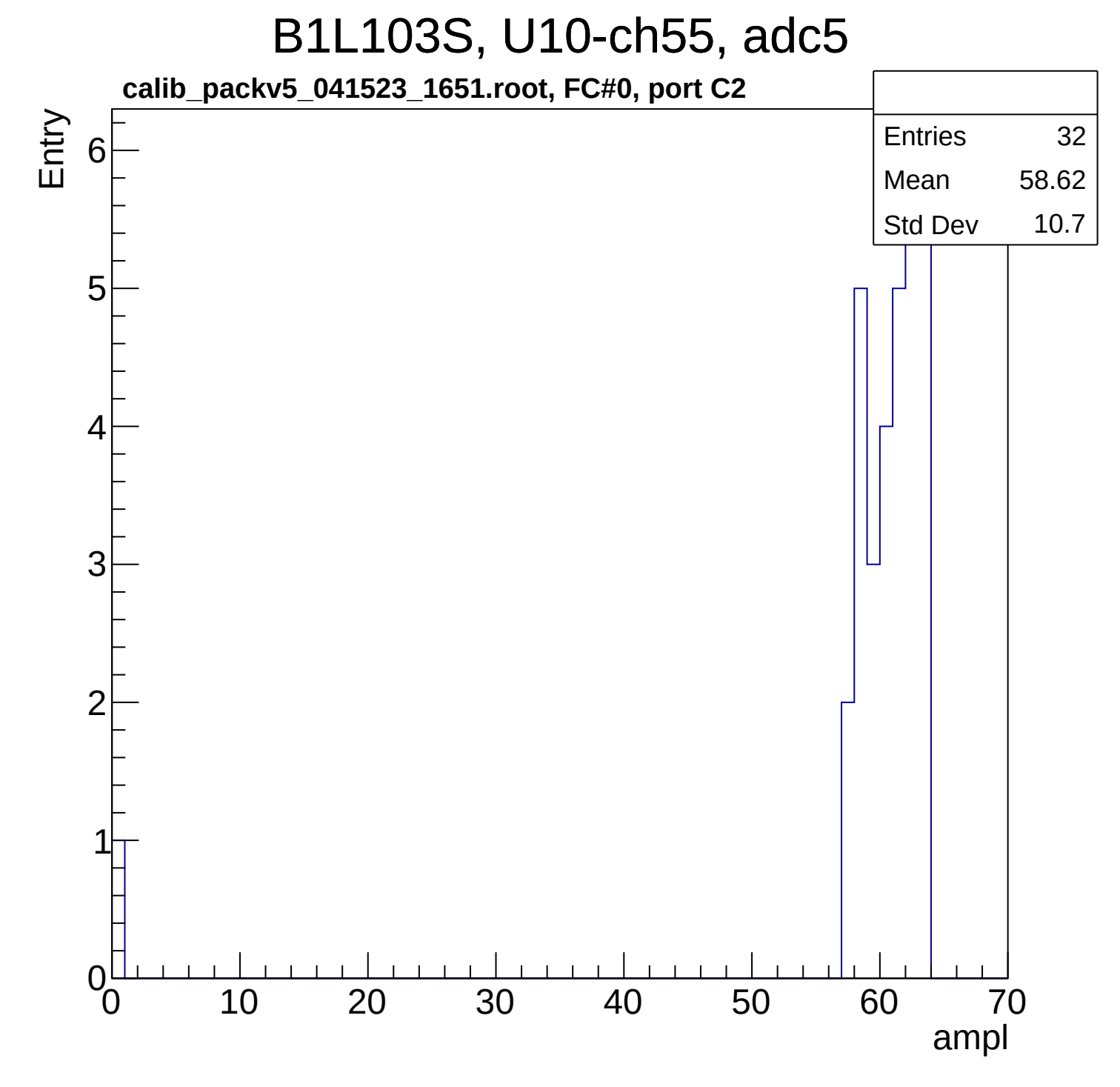
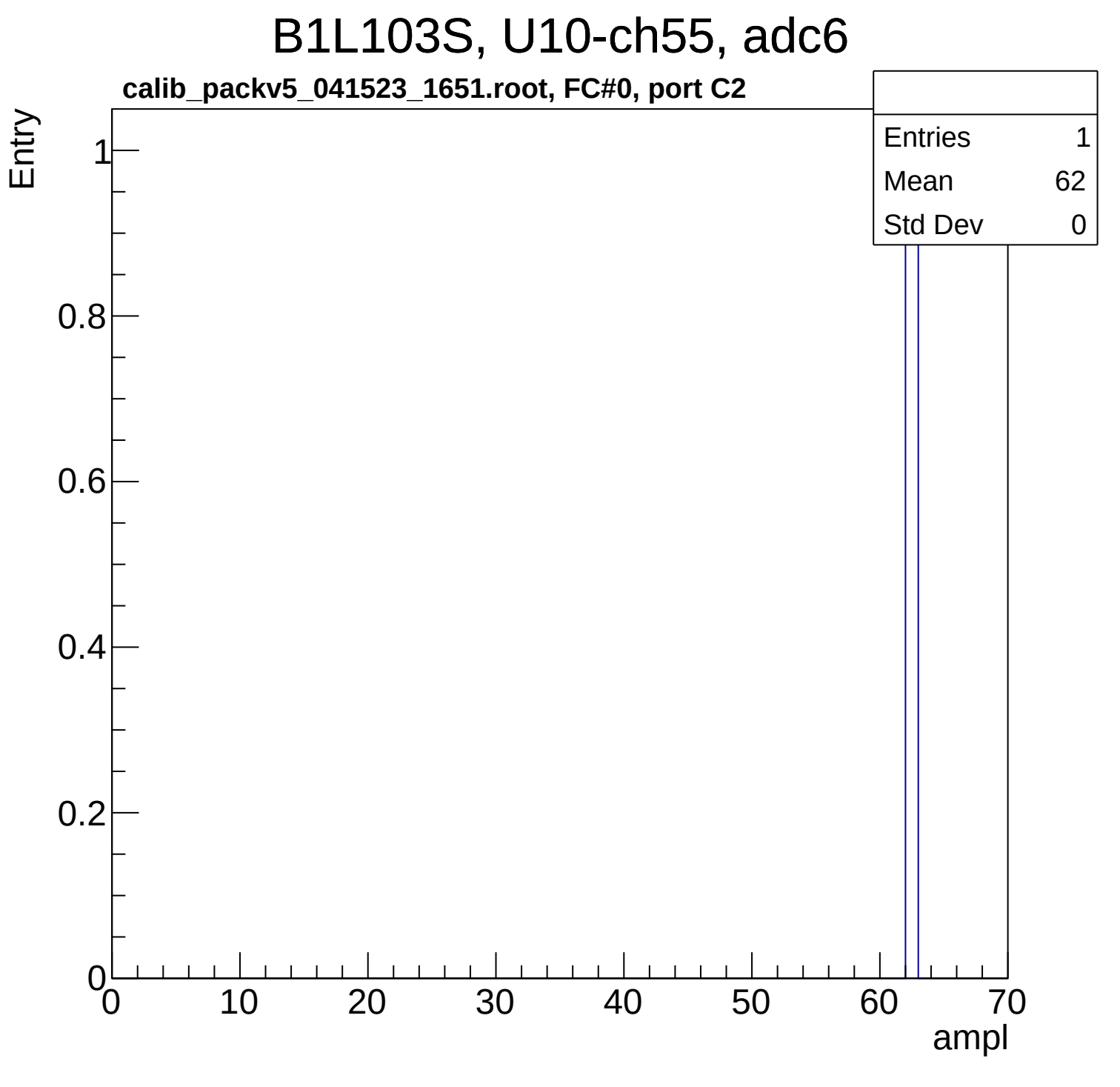
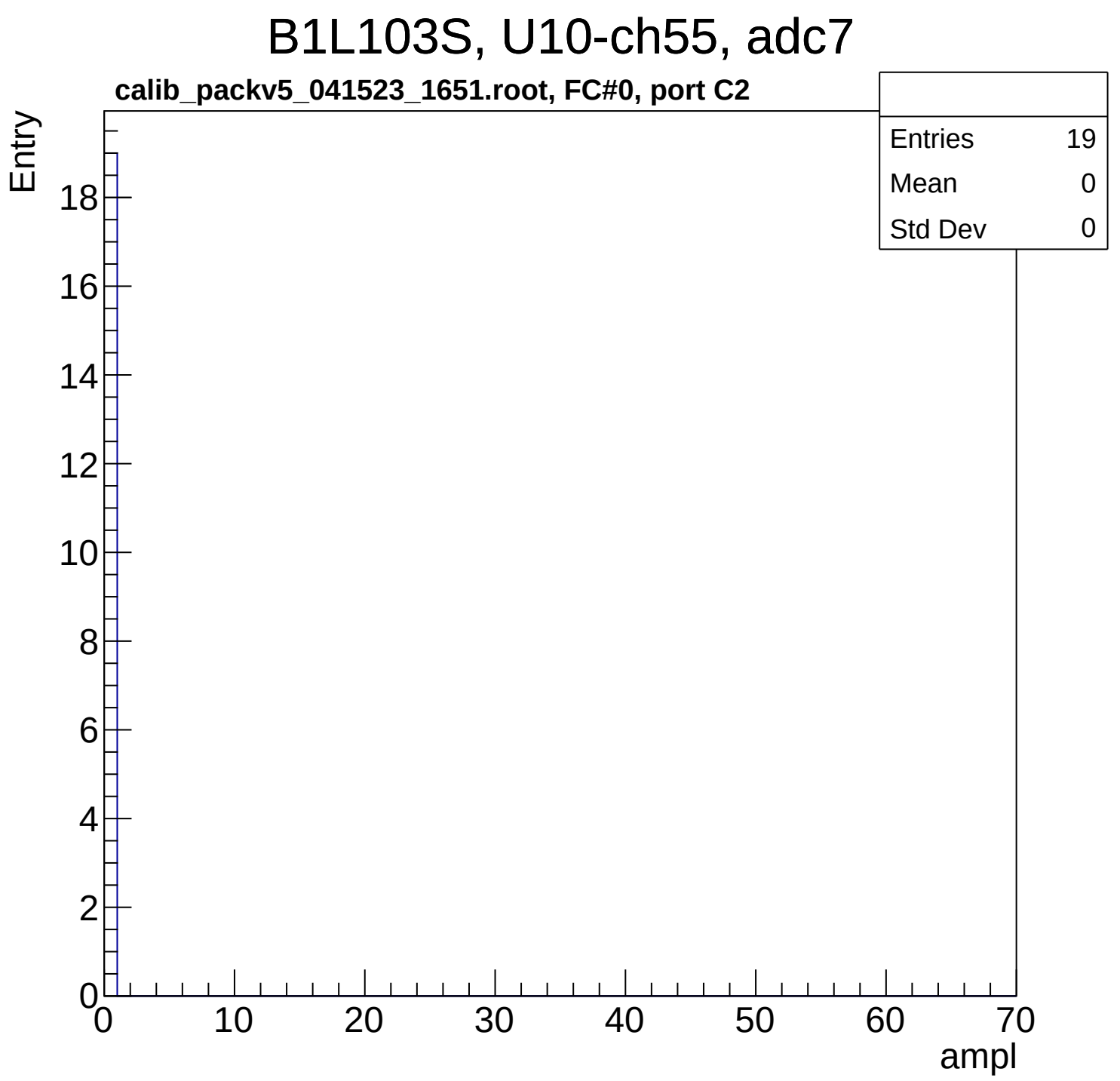

B1L103S, U10-ch55, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 39.4
Std Dev 14.18
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

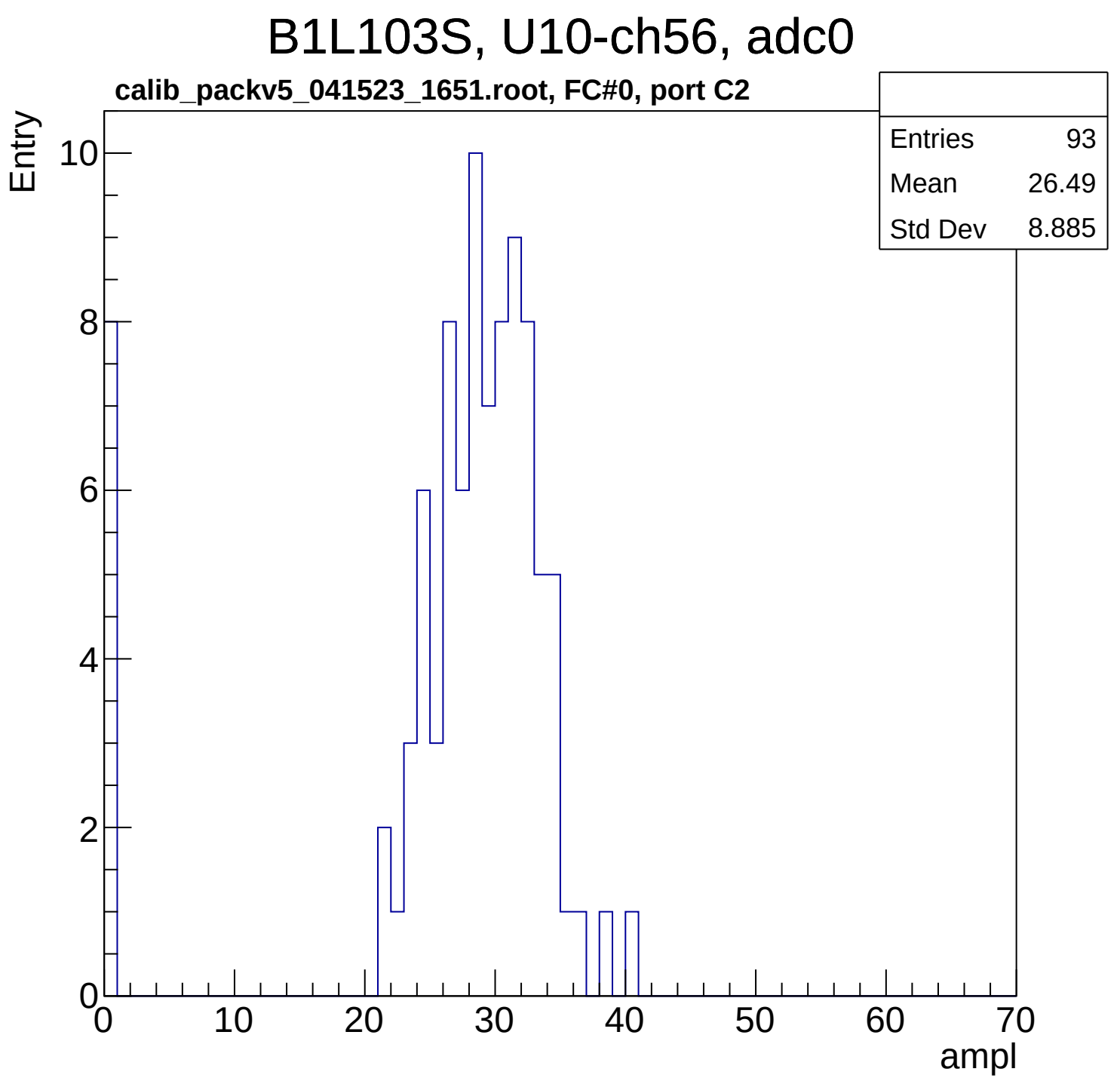

B1L103S, U10-ch55, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 51.34
Std Dev 3.595
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

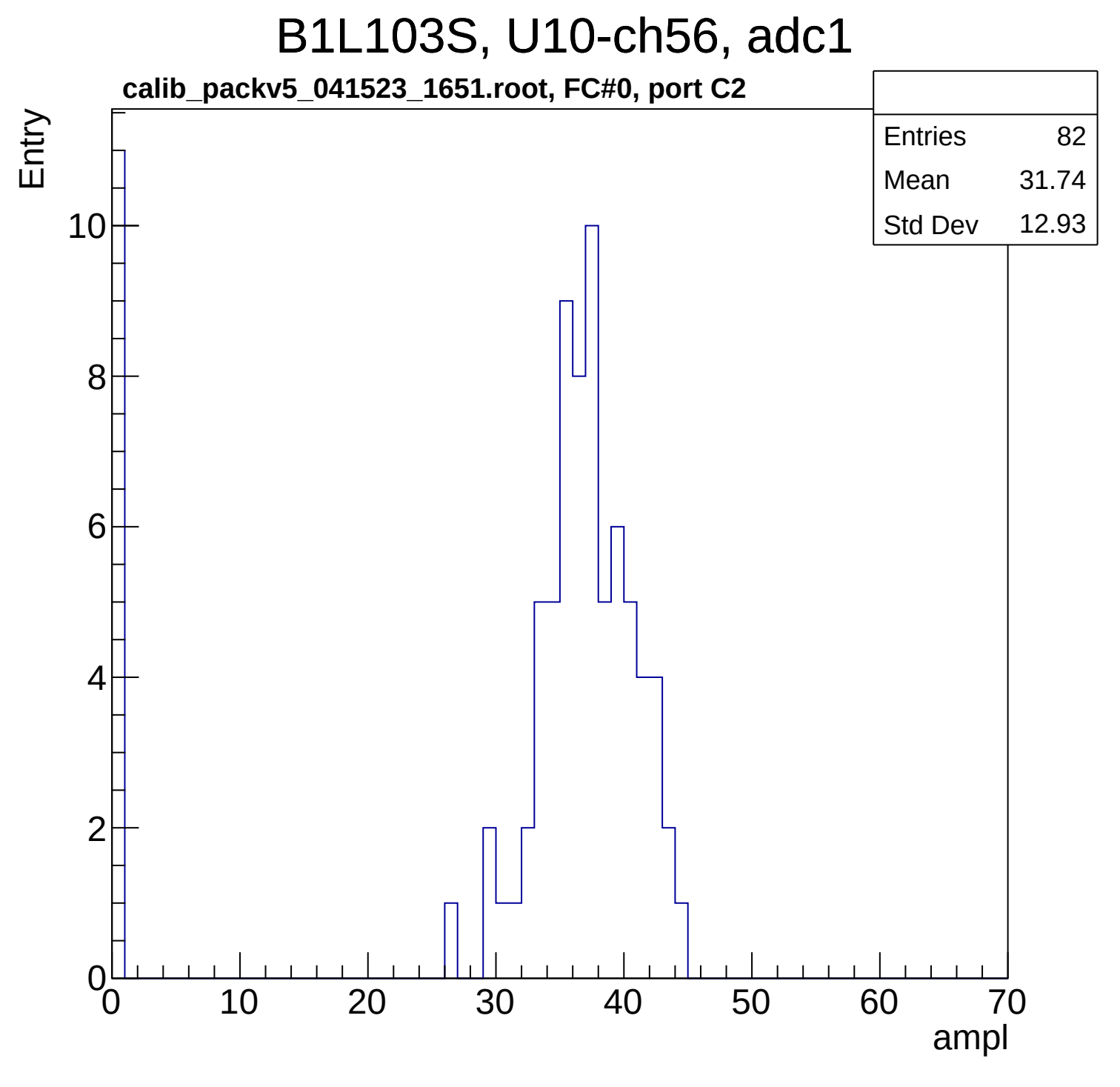

B1L103S, U10-ch55, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 57.65
Std Dev 3.174
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

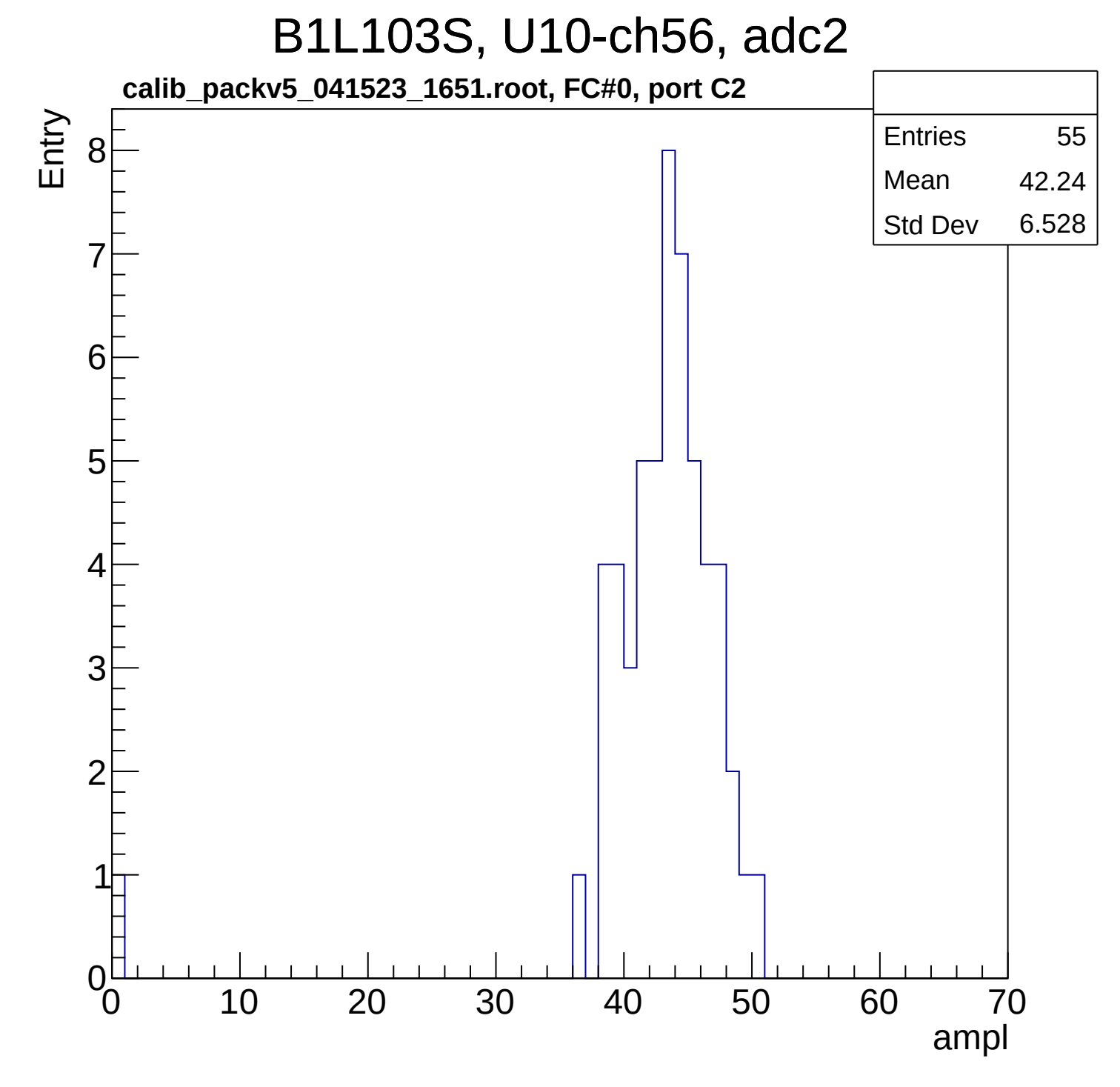

B1L103S, U10-ch55, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 32
Mean 58.62
Std Dev 10.7
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

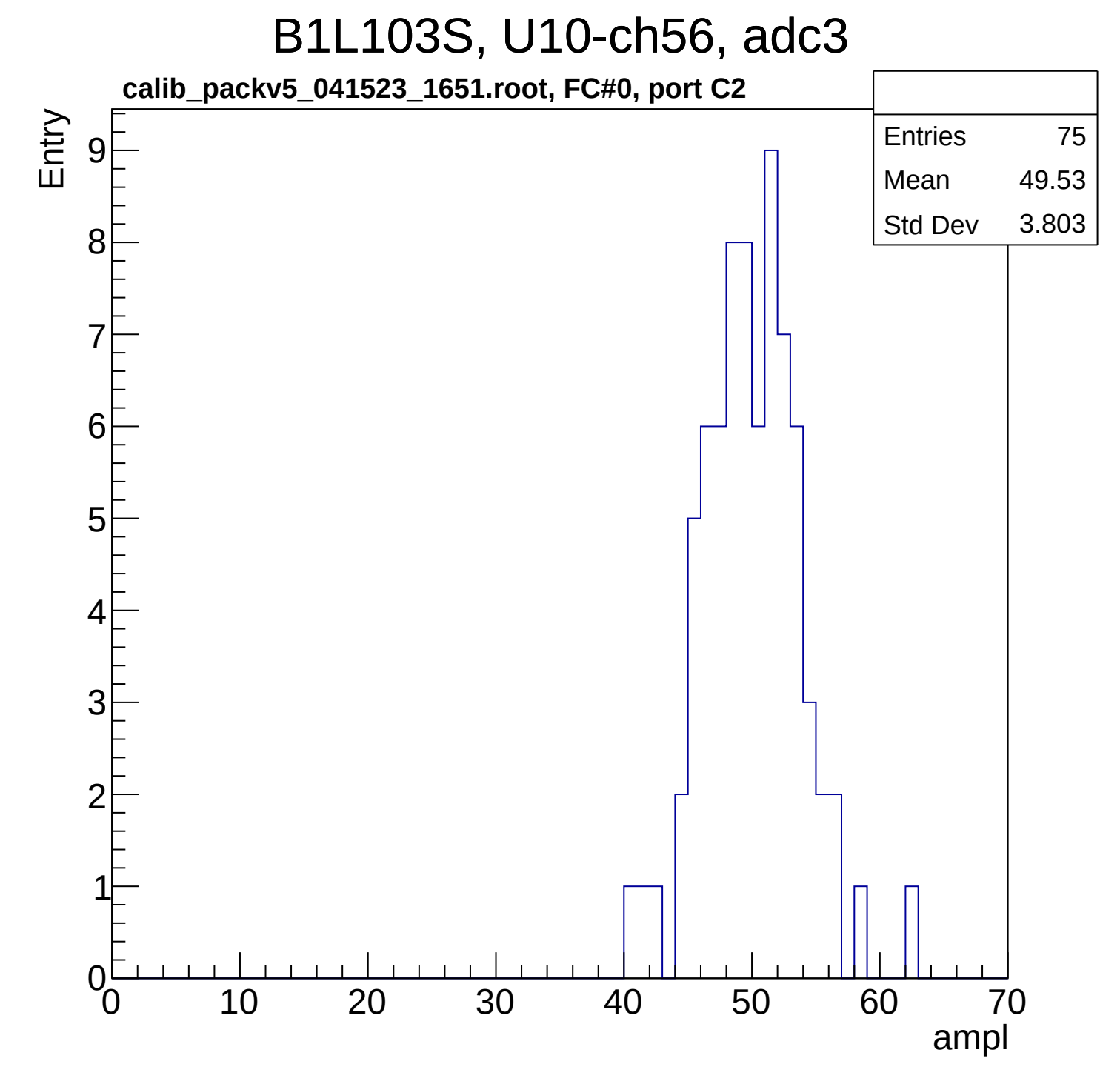

B1L103S, U10-ch55, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 1
Mean 62
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

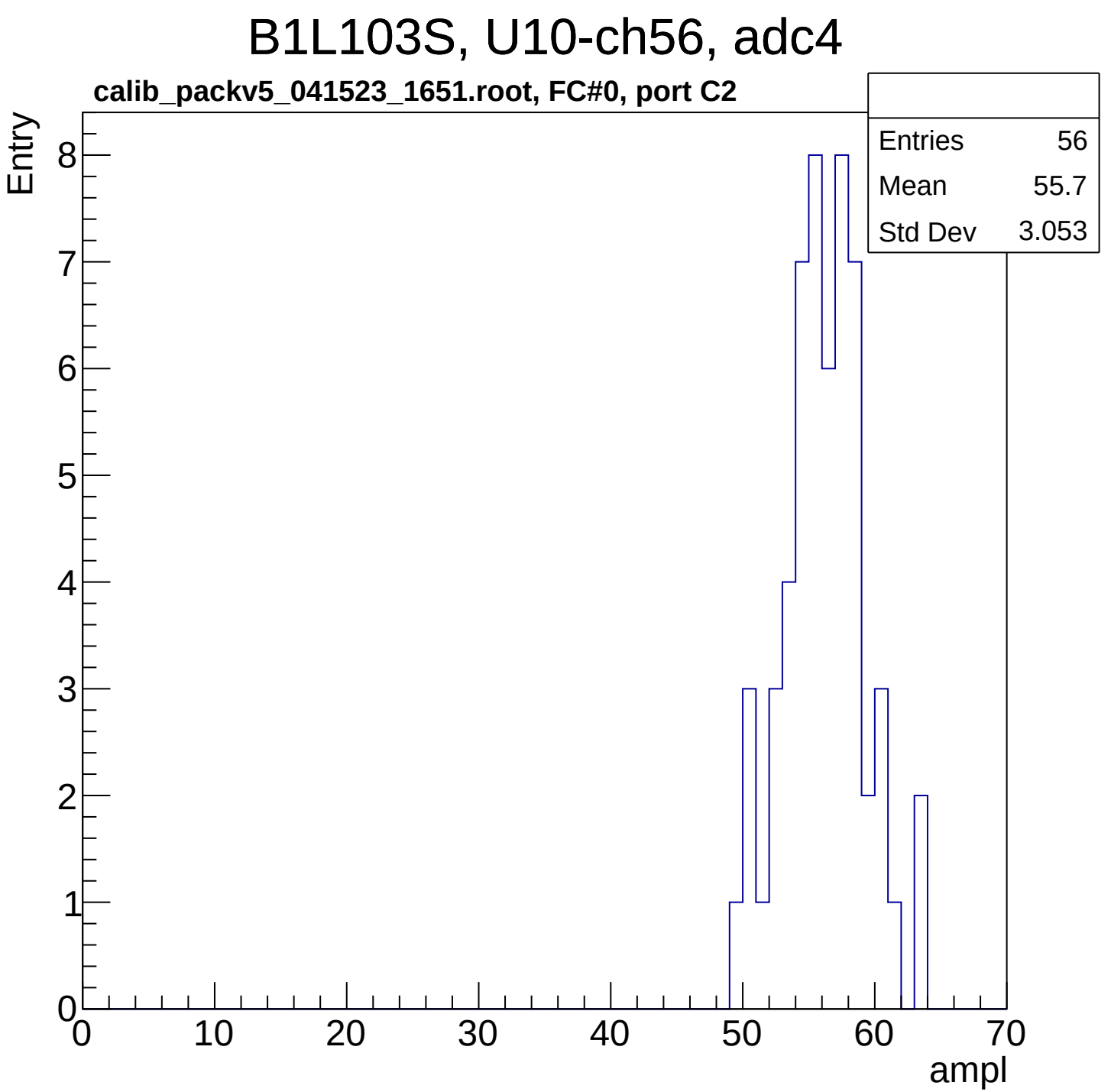

B1L103S, U10-ch55, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch56, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 93
Mean 26.49
Std Dev 8.885
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U10-ch56, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 31.74
Std Dev 12.93
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch56, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 42.24
Std Dev 6.528
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U10-ch56, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 49.53
Std Dev 3.803
Entry
ampl
0
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9


B1L103S, U10-ch56, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 55.7
Std Dev 3.053
Entry
ampl
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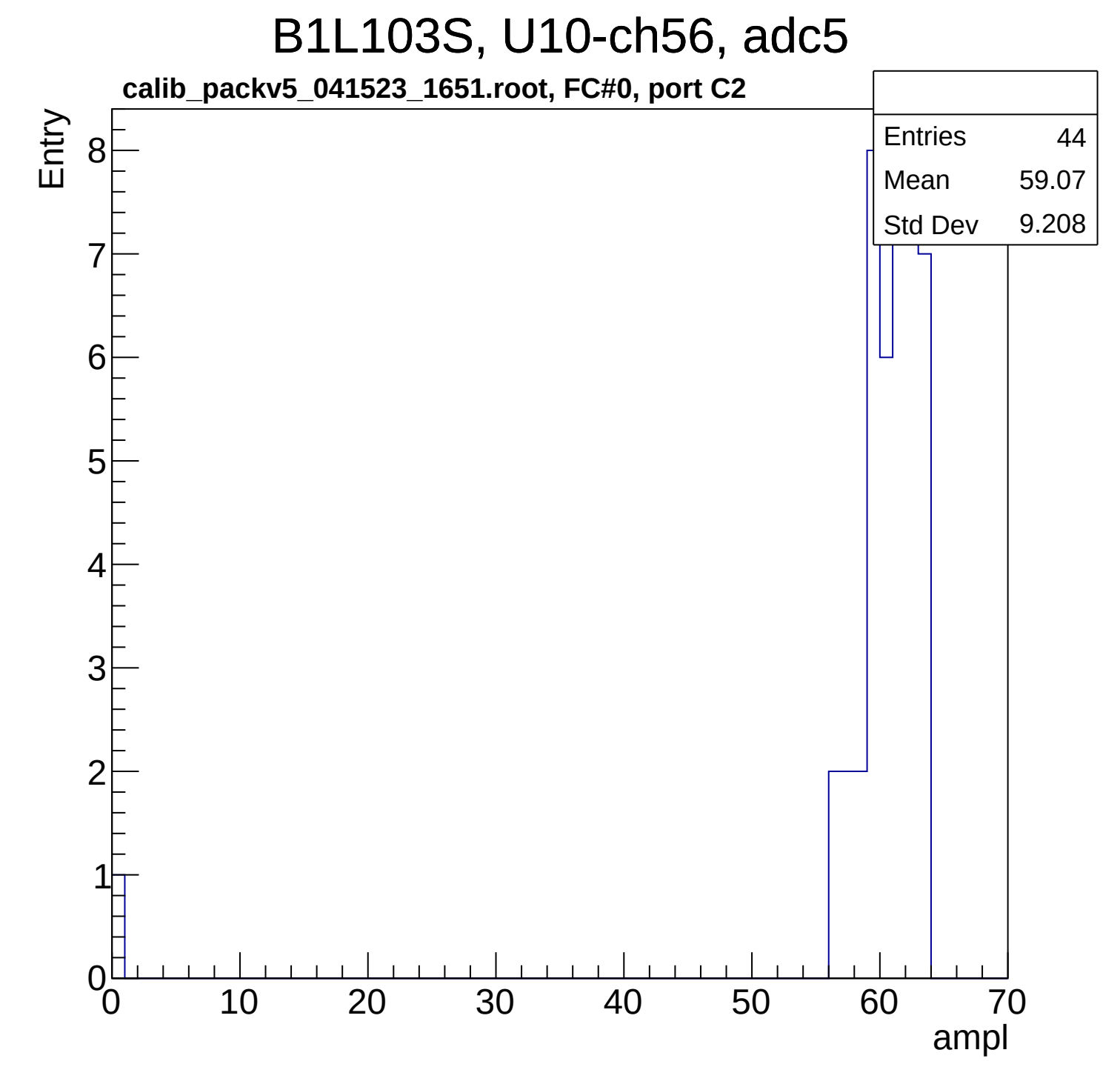
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U10-ch56, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 59.07
Std Dev 9.208
Entry
ampl
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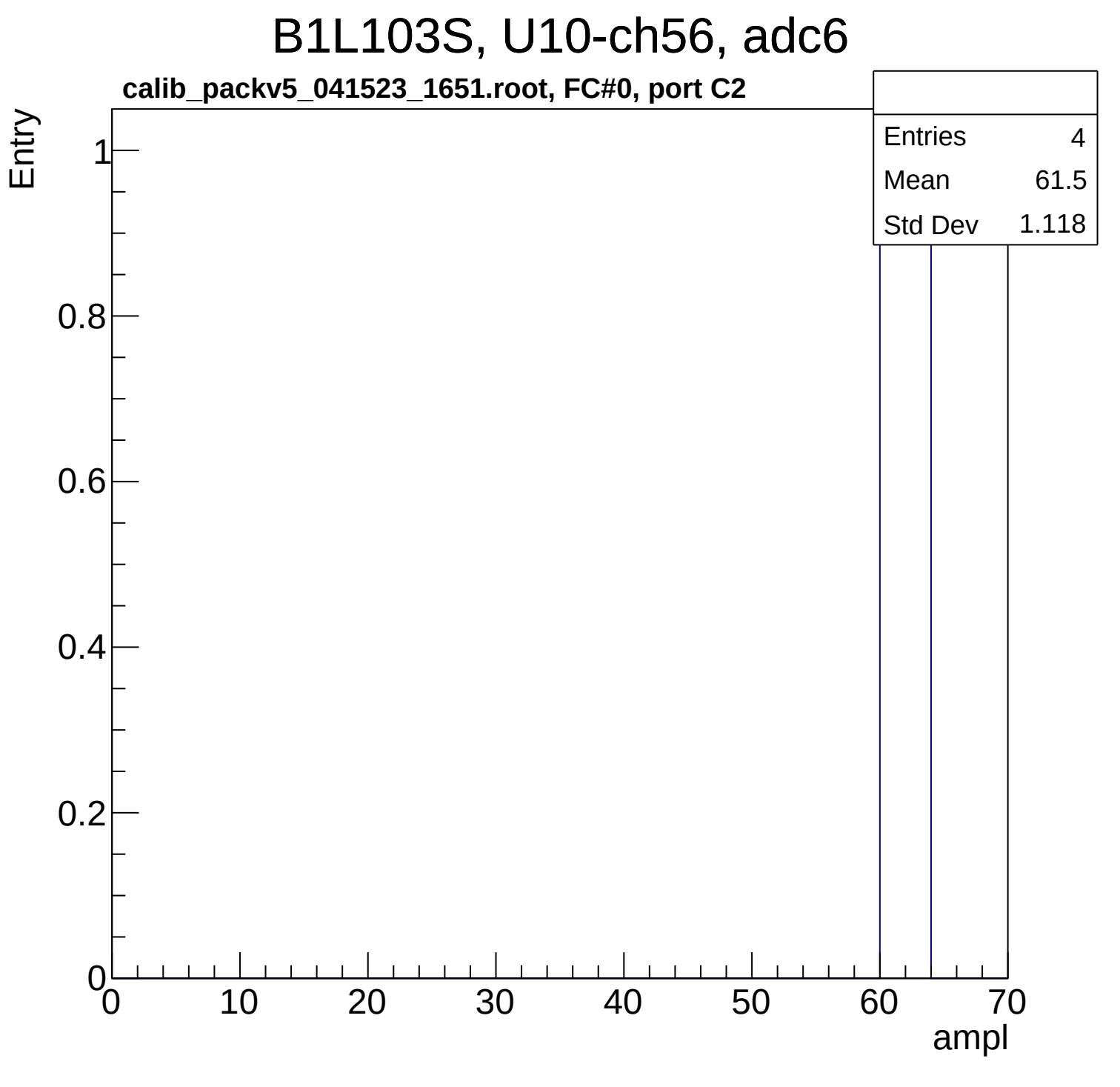
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U10-ch56, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 4
Mean 61.5
Std Dev 1.118
Entry
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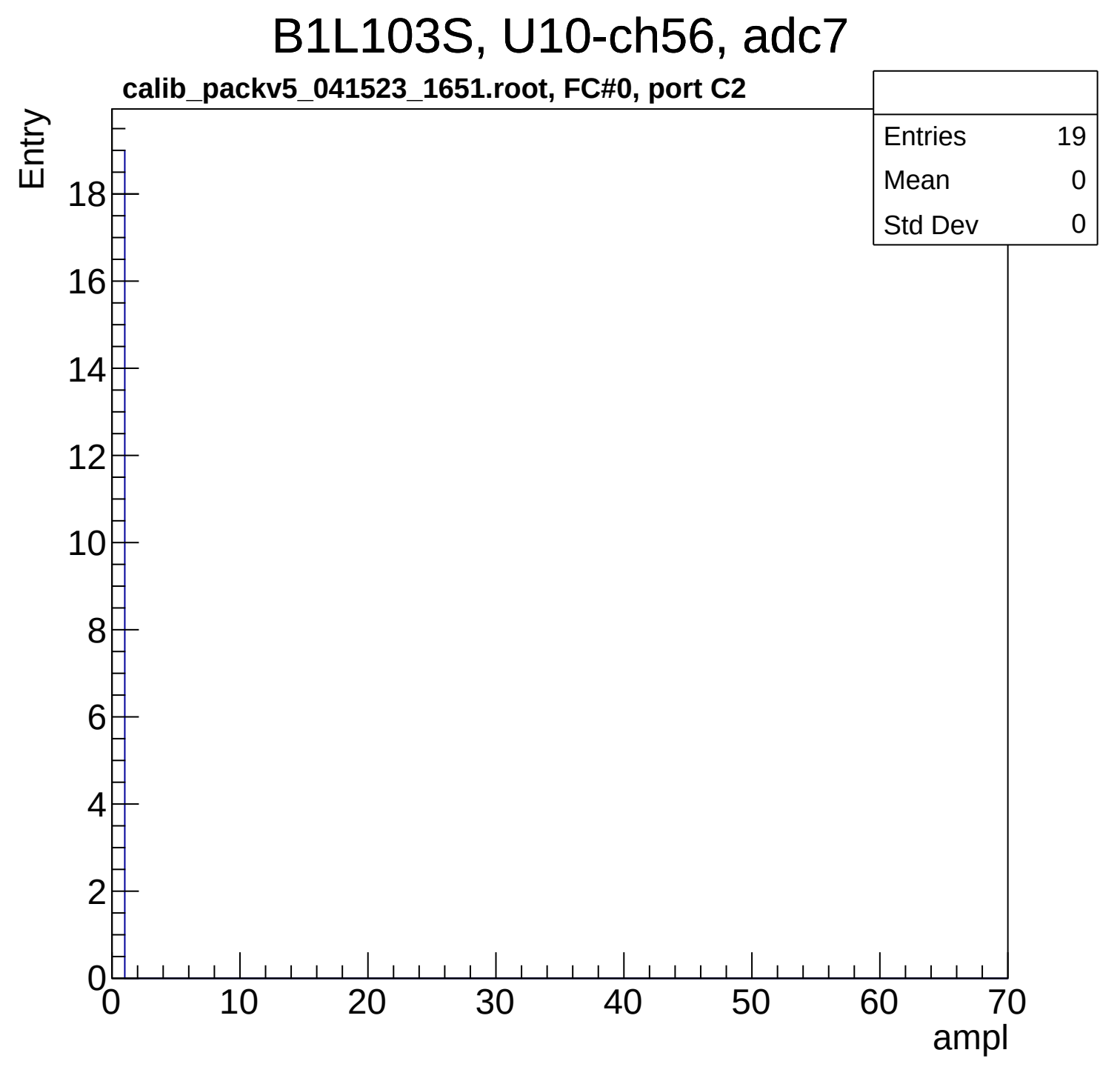
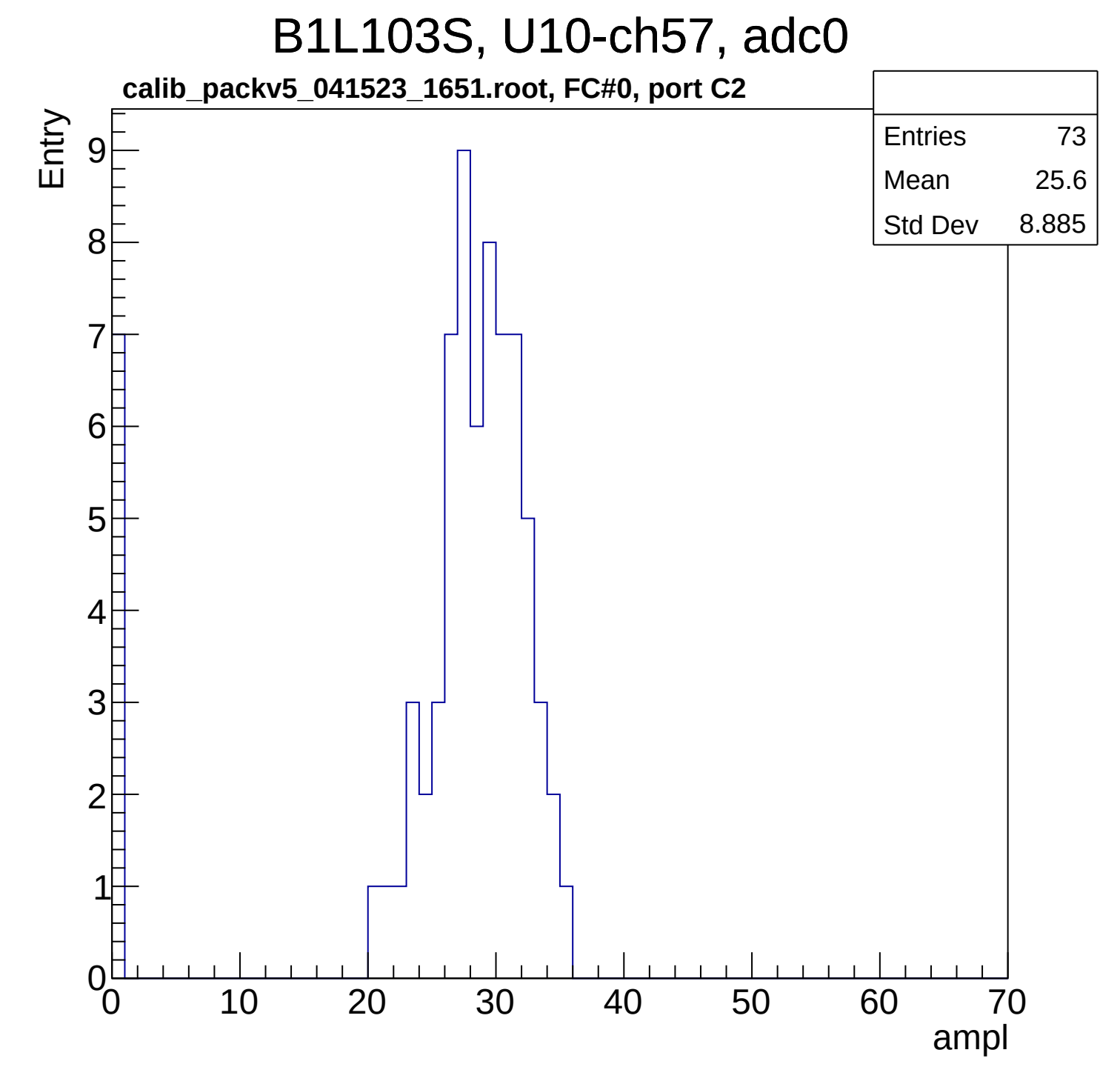
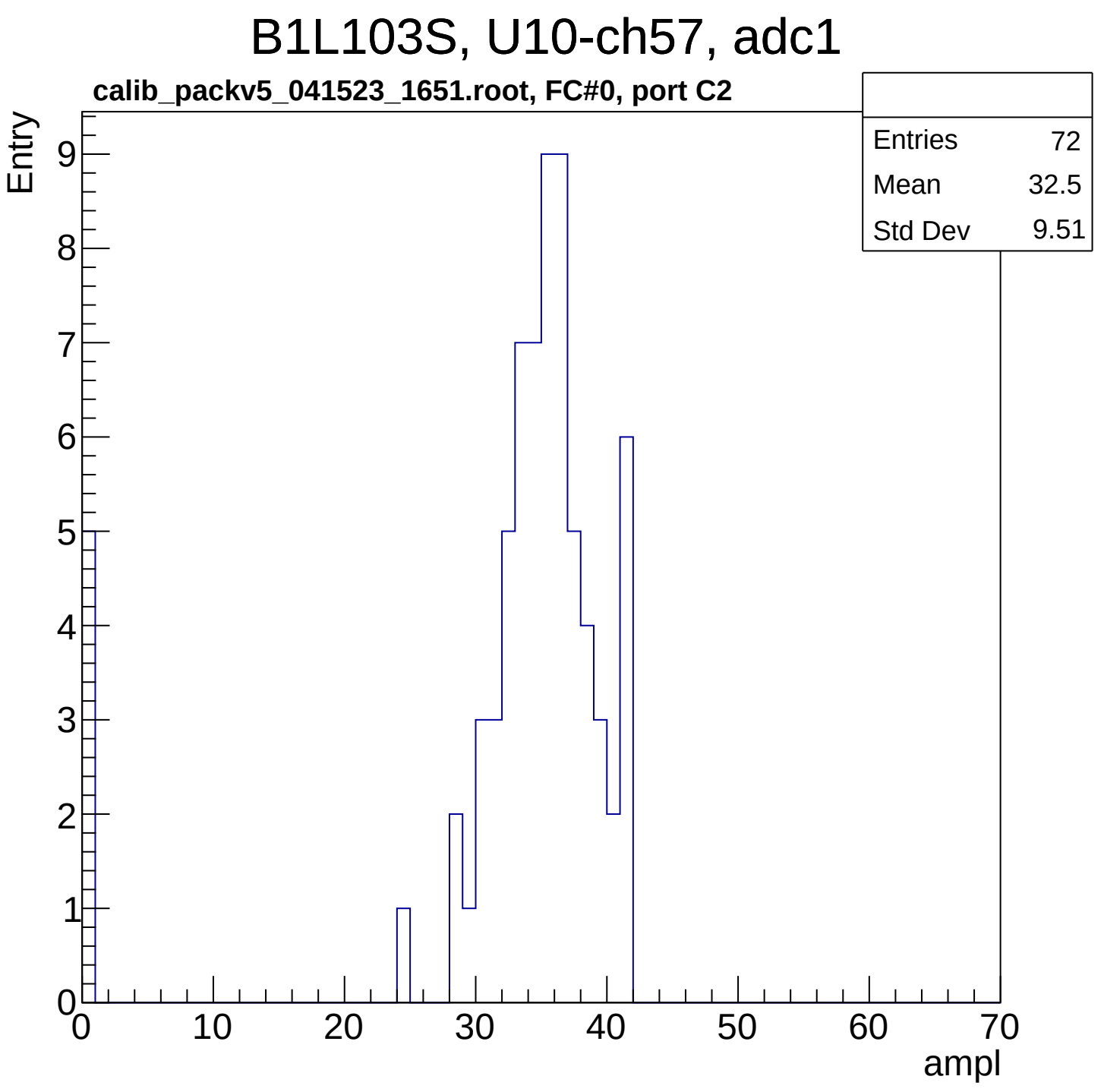
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch56, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch57, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 25.6
Std Dev 8.885
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U10-ch57, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 32.5
Std Dev 9.51
Entry
ampl
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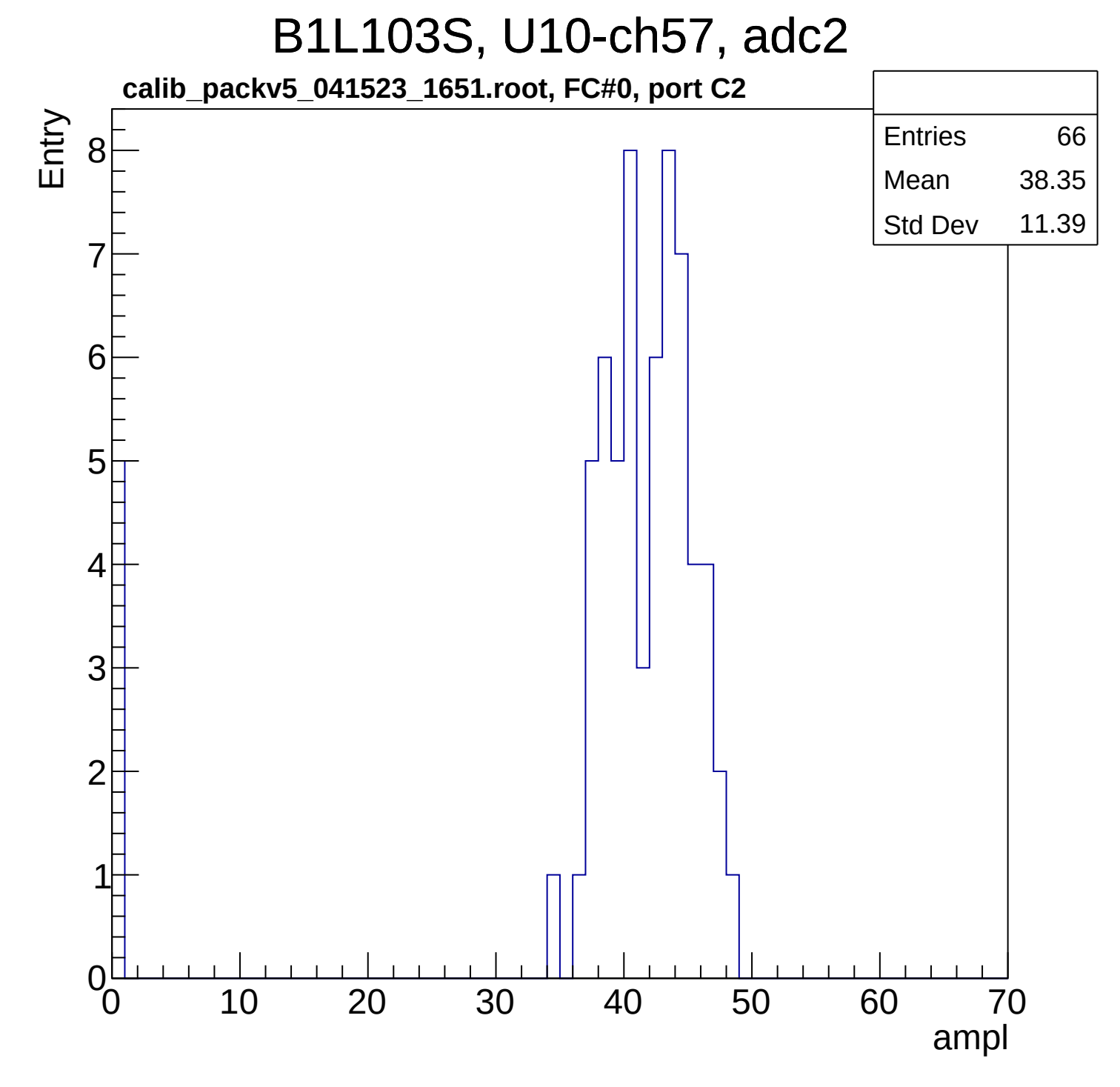
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U10-ch57, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 38.35
Std Dev 11.39
Entry
ampl
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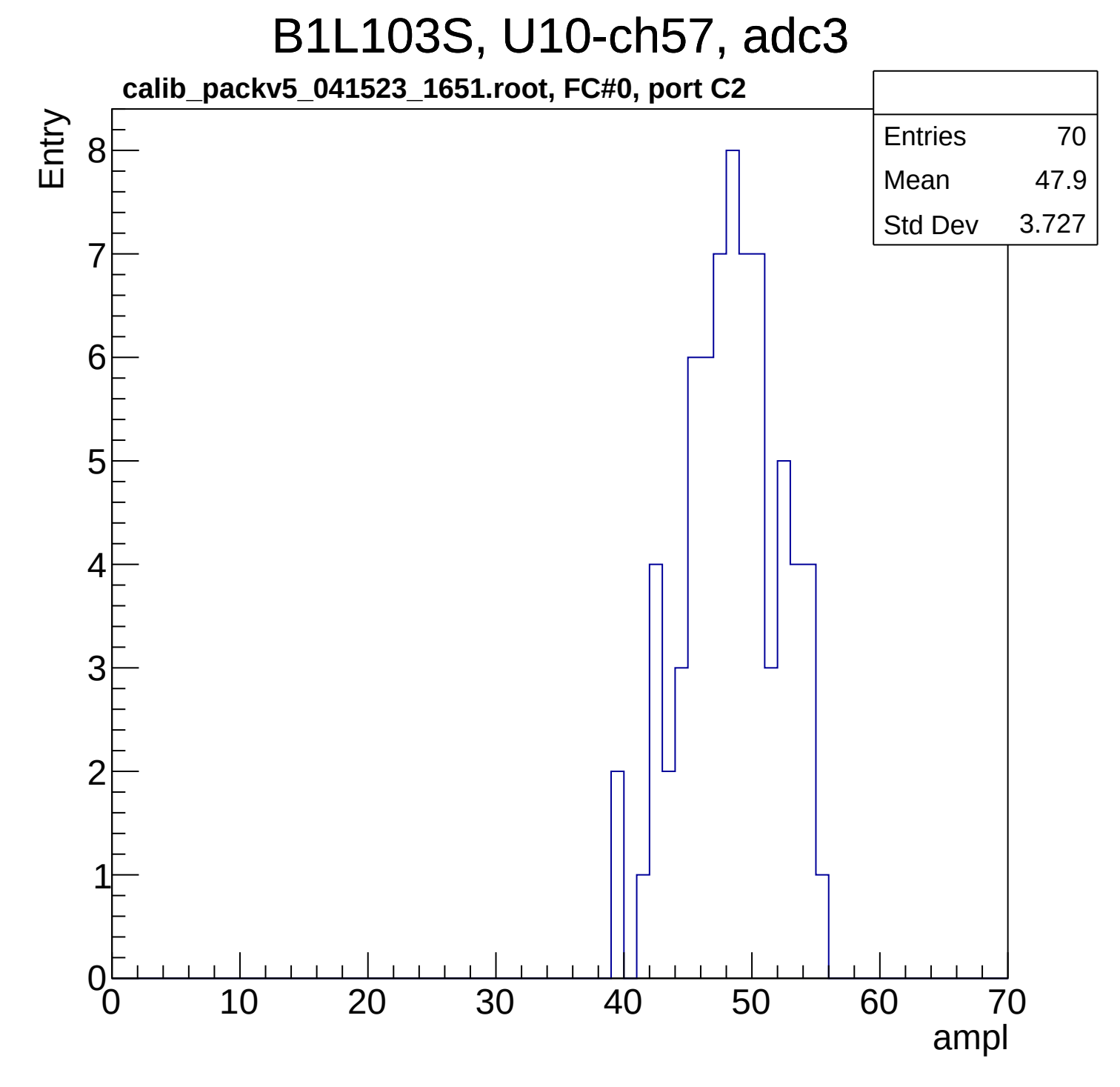
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U10-ch57, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 47.9
Std Dev 3.727
Entry
ampl
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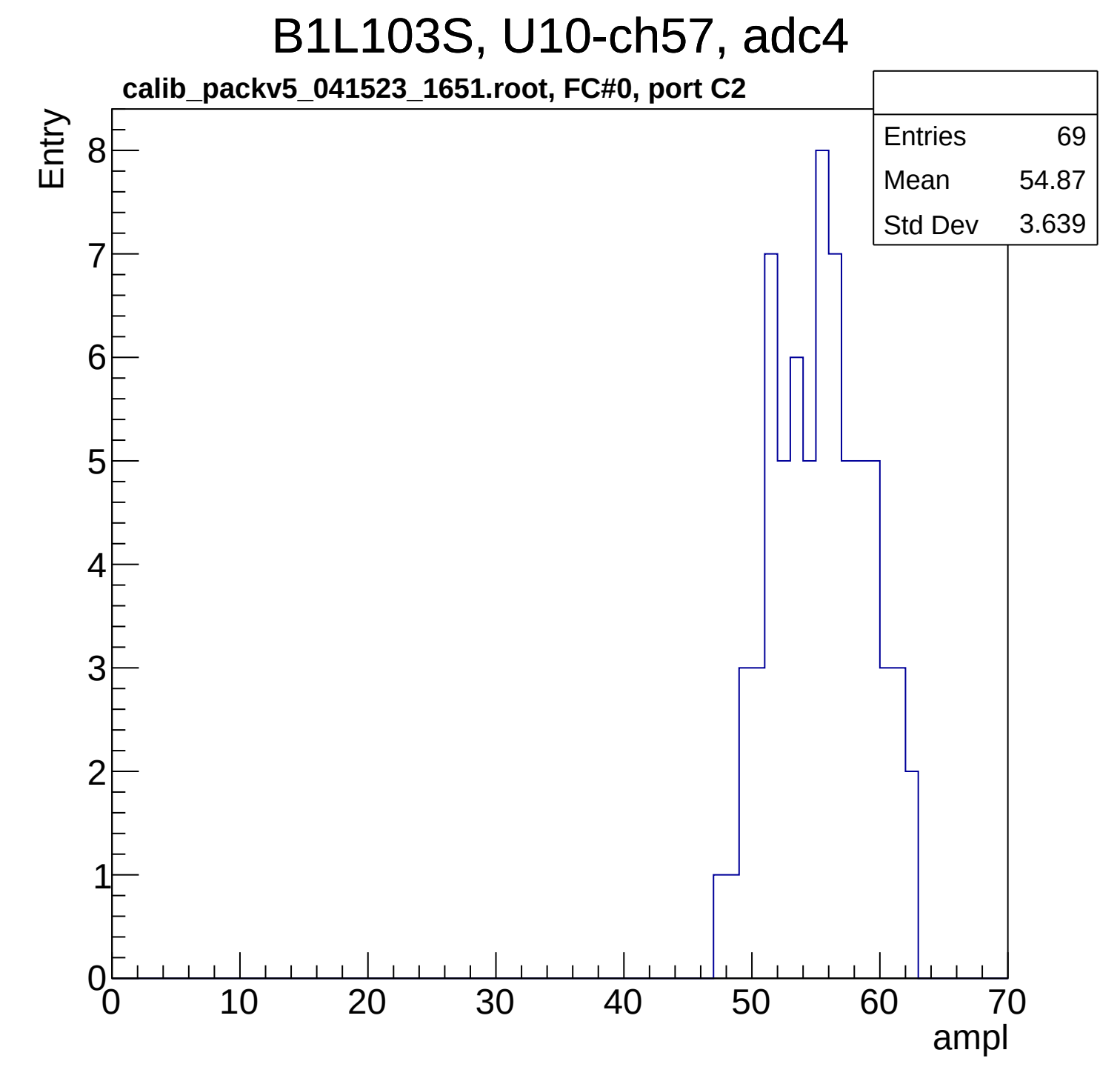
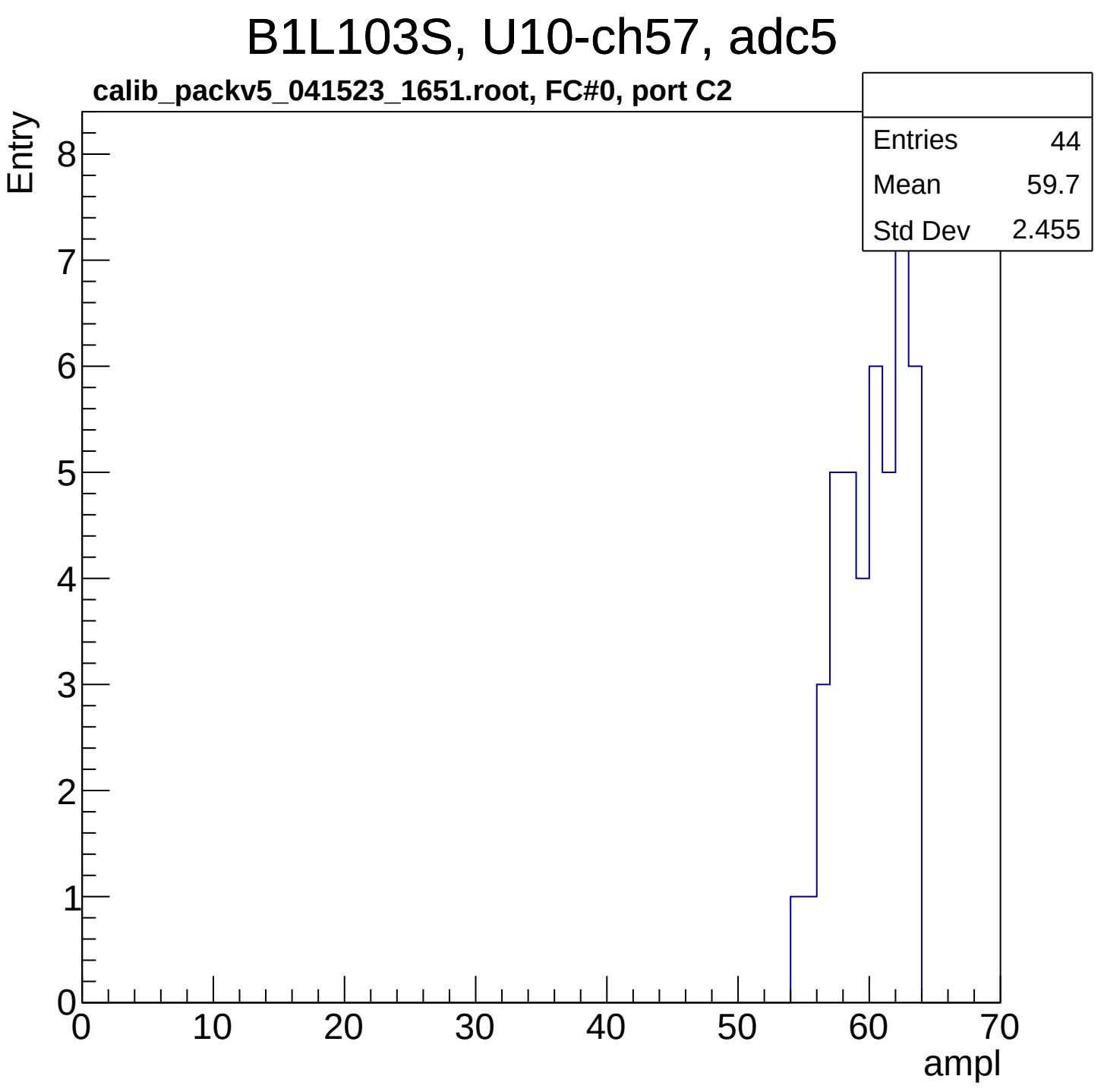
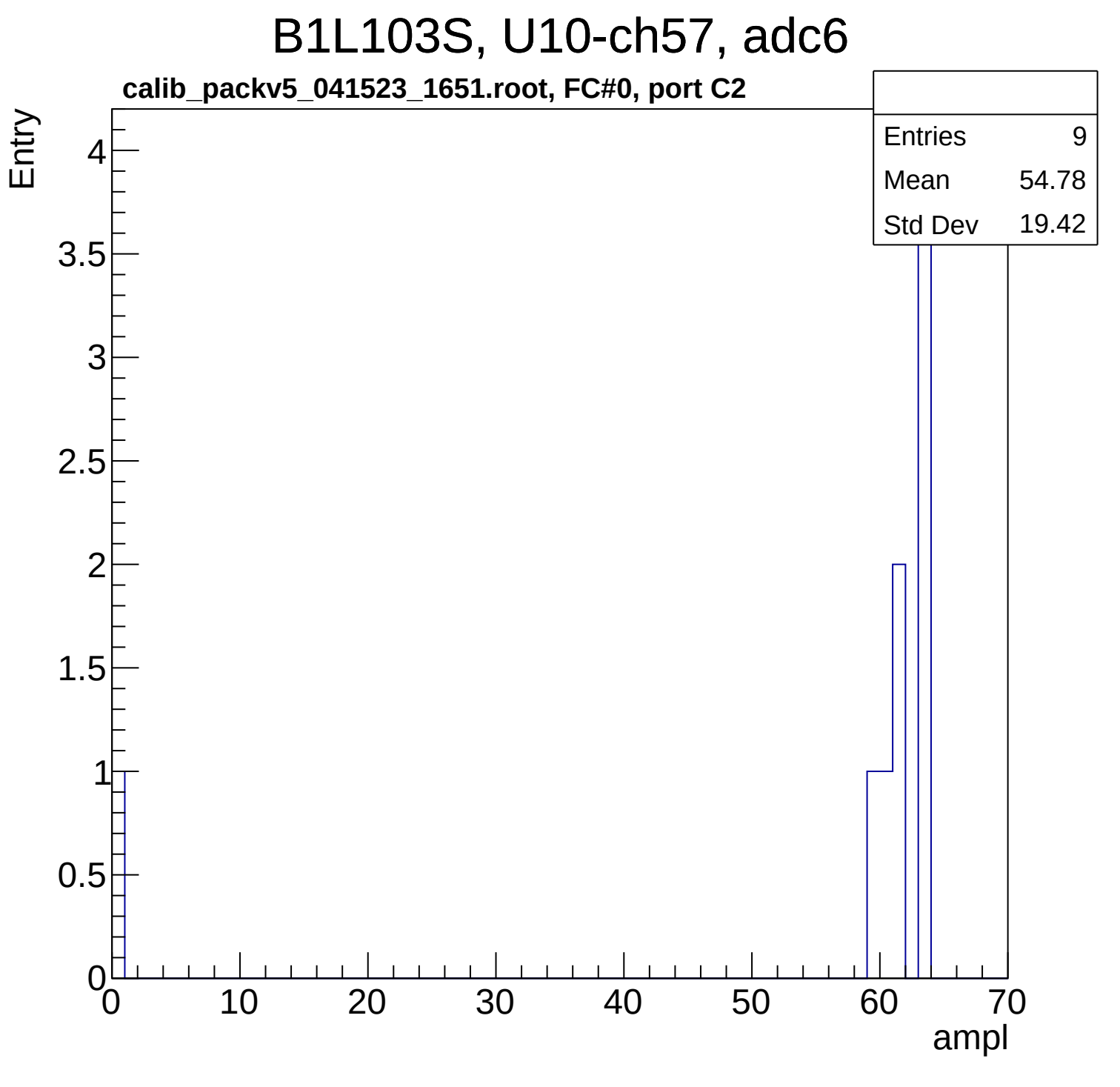
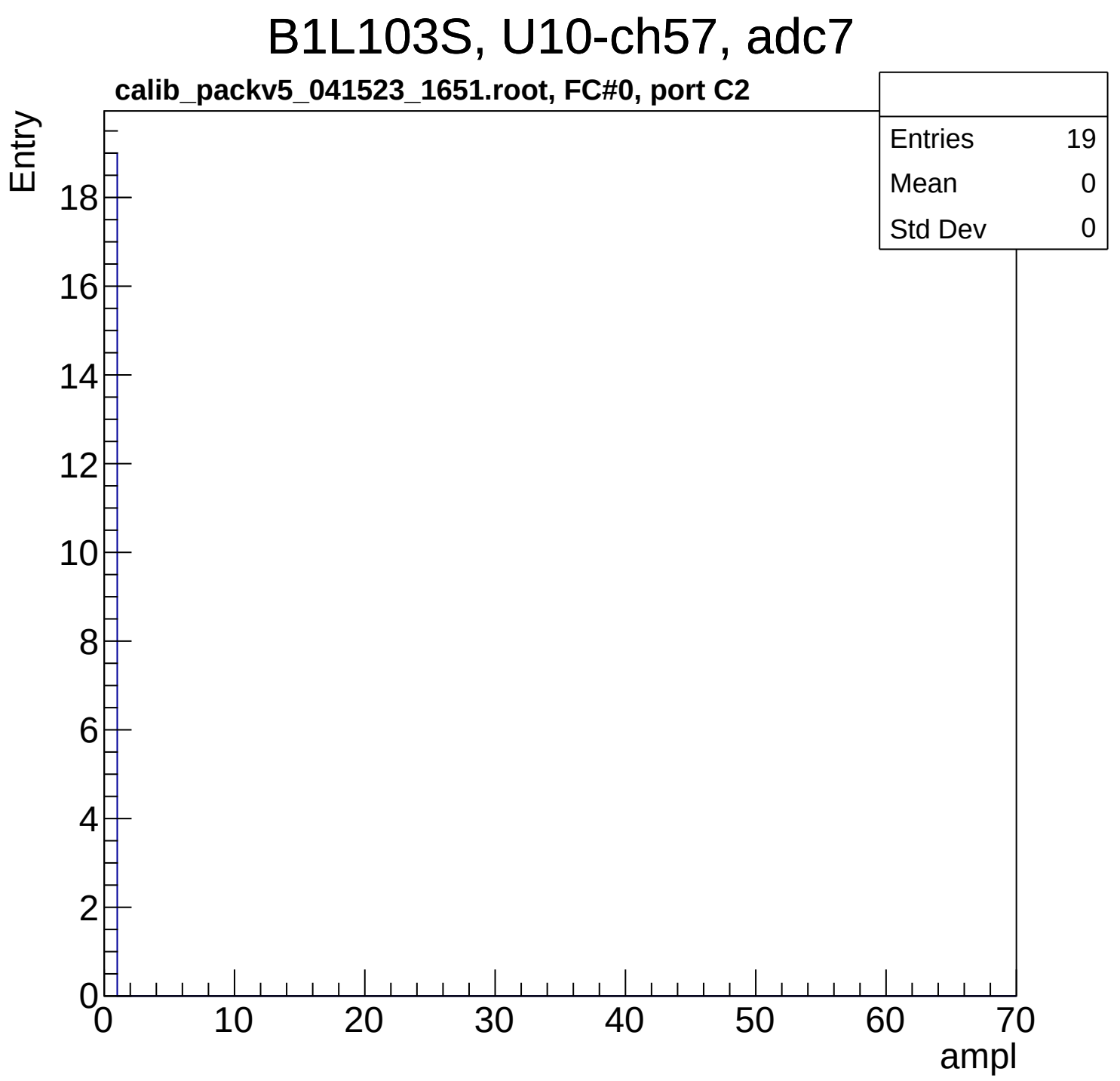
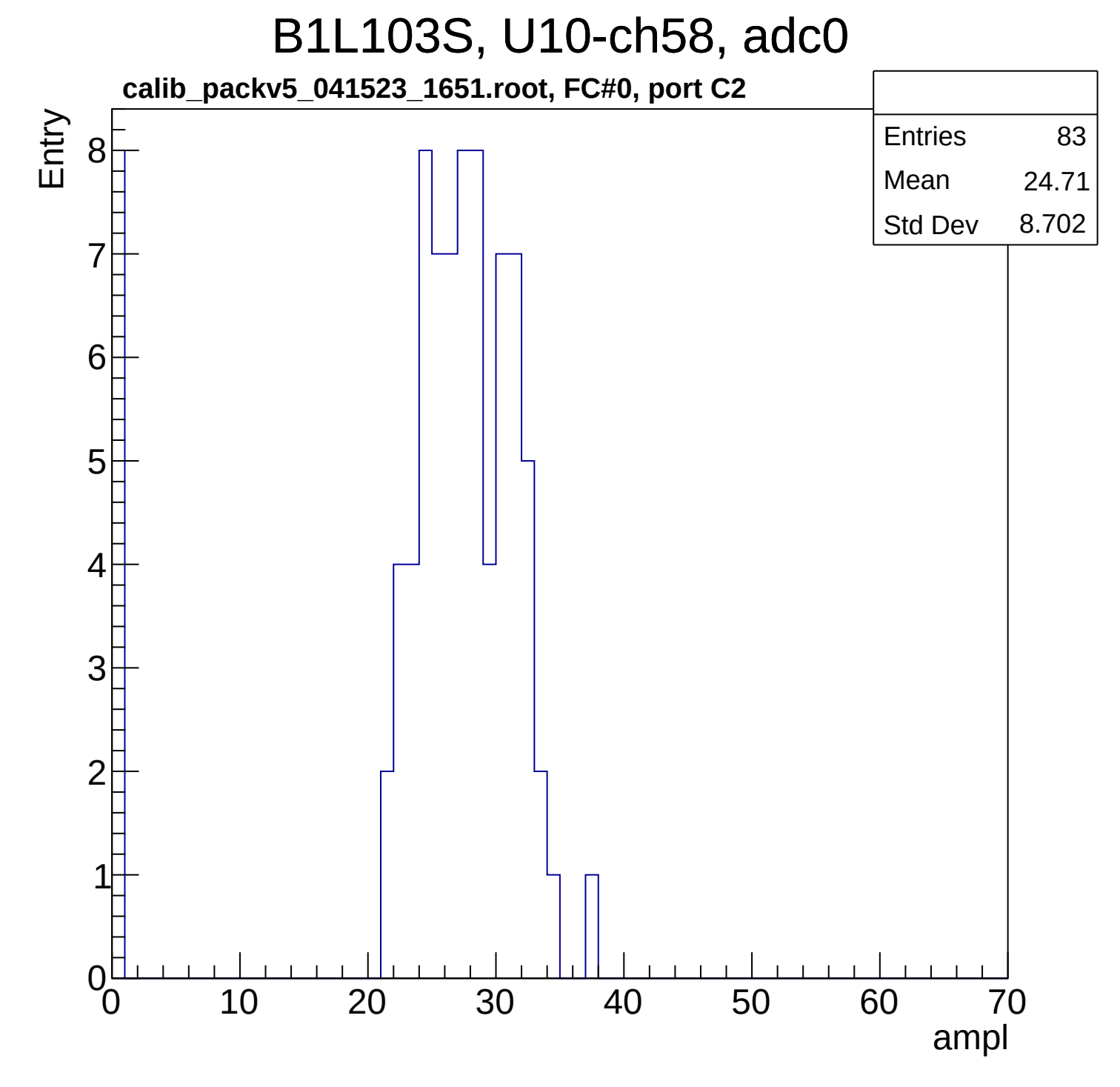
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

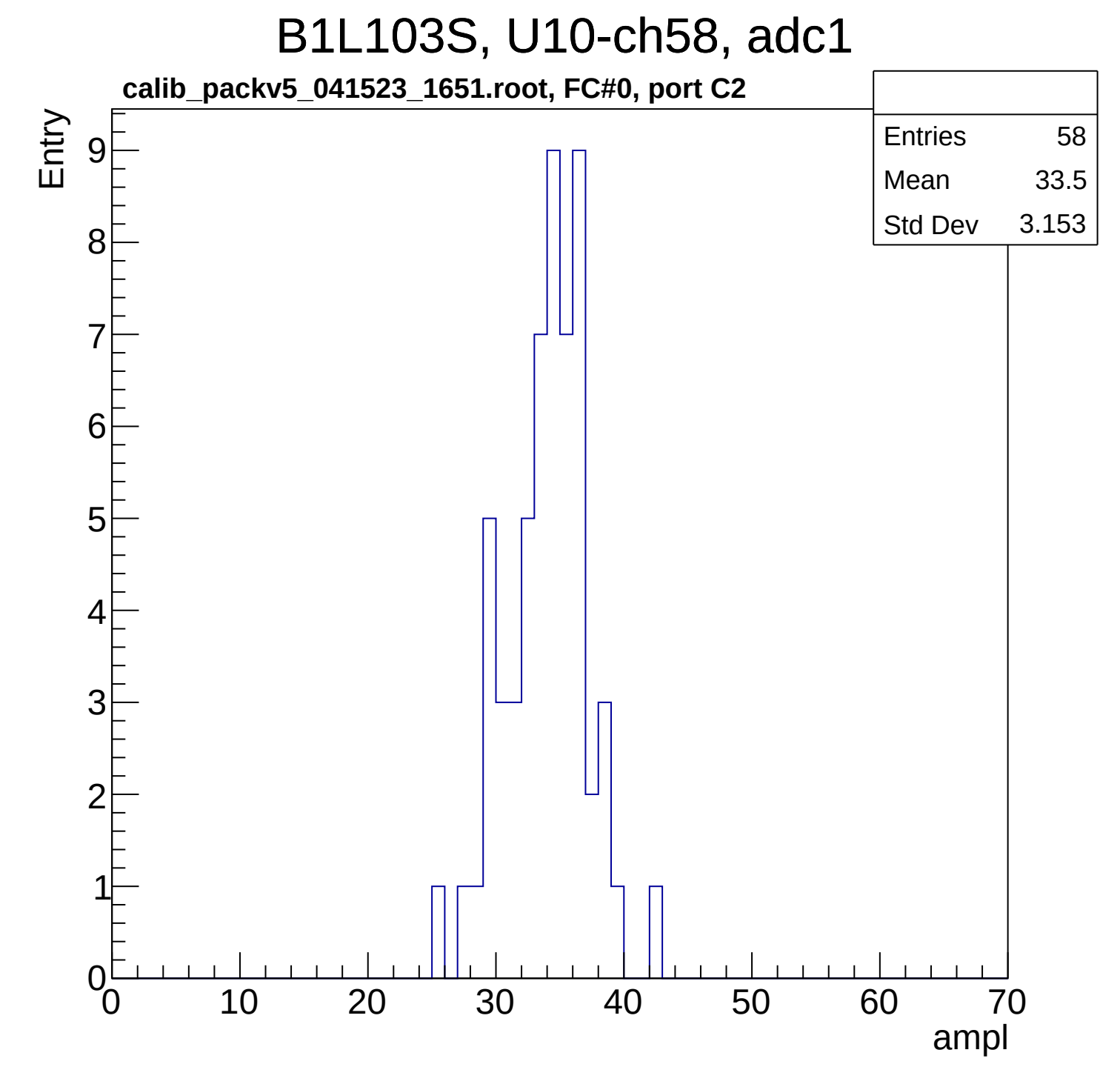

B1L103S, U10-ch57, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 54.87
Std Dev 3.639
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U10-ch57, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 59.7
Std Dev 2.455
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U10-ch57, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 9
Mean 54.78
Std Dev 19.42
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U10-ch57, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch58, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 24.71
Std Dev 8.702
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U10-ch58, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 33.5
Std Dev 3.153
Entry
ampl
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2
3
4
5
6
7
8
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0
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40
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60
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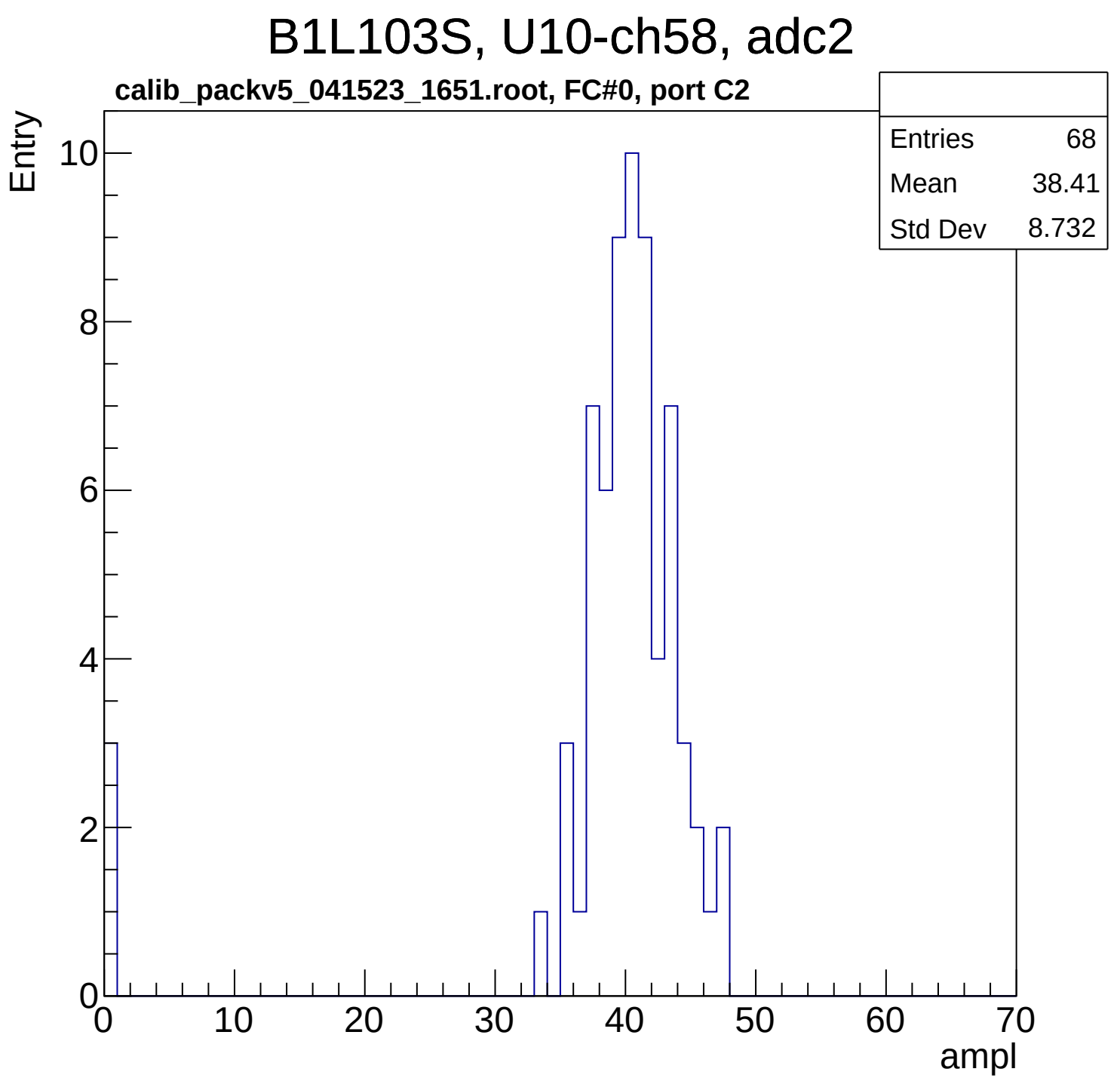
B1L103S, U10-ch58, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 38.41
Std Dev 8.732
Entry
ampl
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2
4
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8
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0
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40
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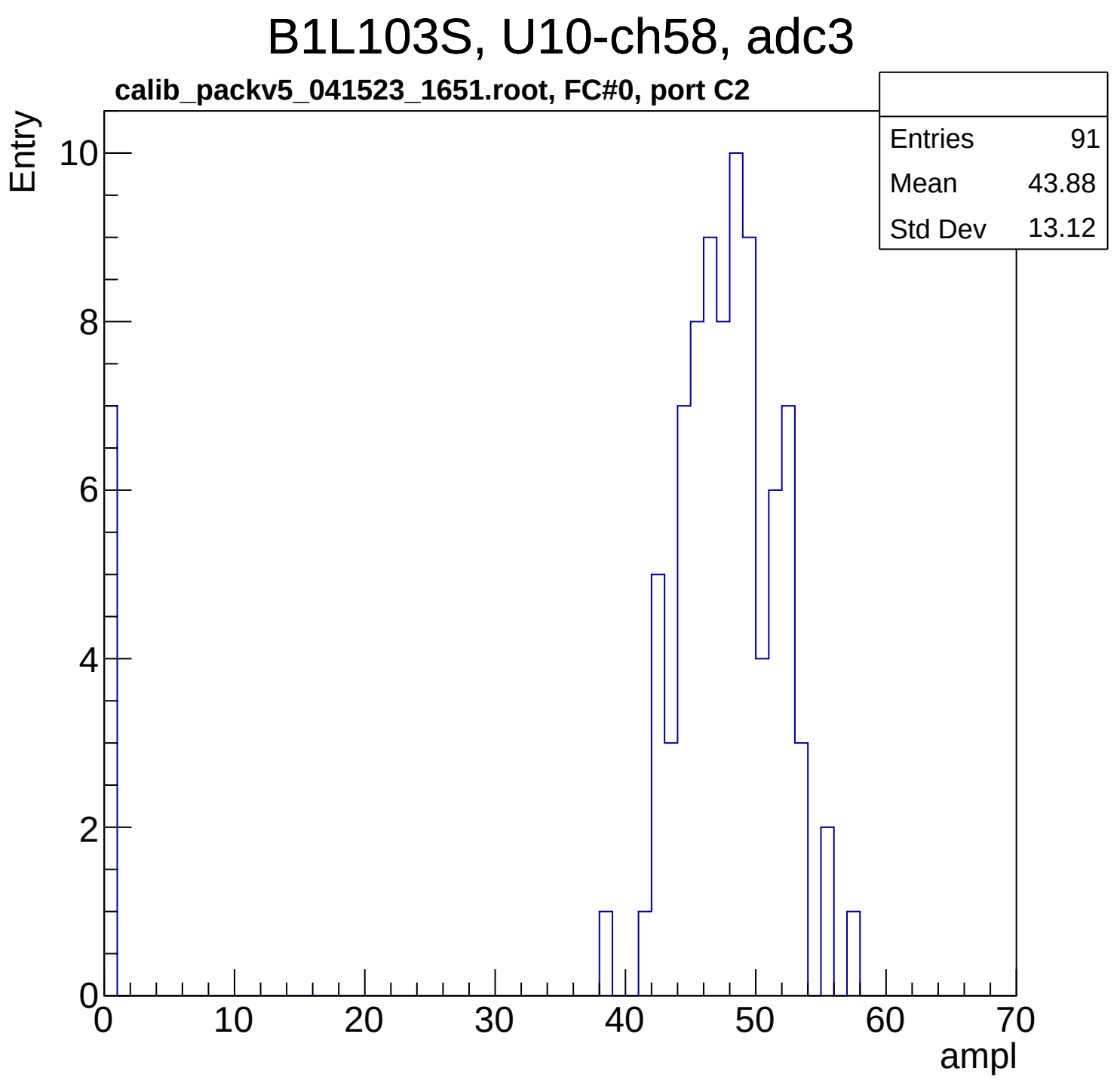
B1L103S, U10-ch58, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 91
Mean 43.88
Std Dev 13.12
Entry
ampl
0
2
4
6
8
10
0
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40
50
60
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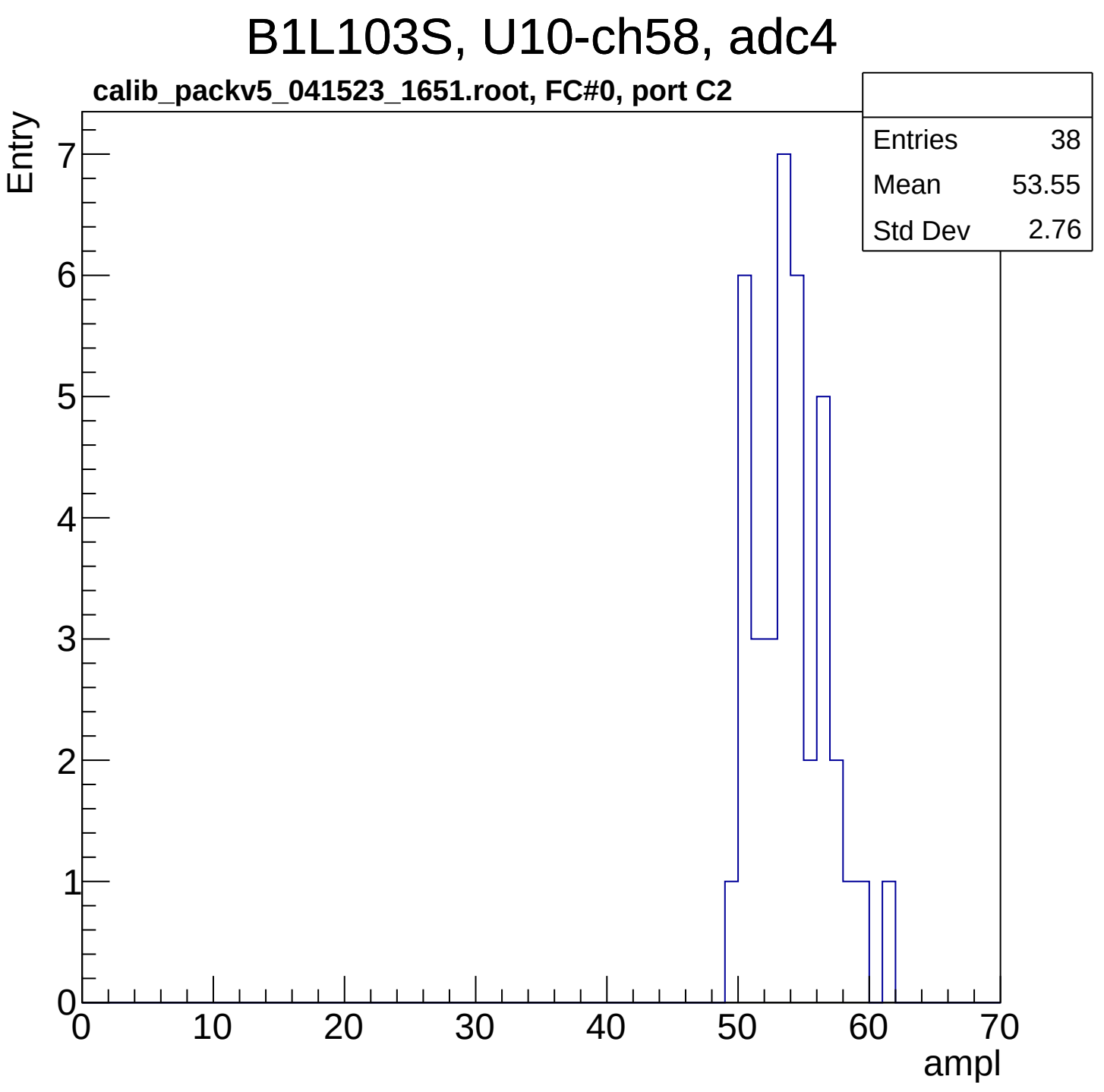
B1L103S, U10-ch58, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 38
Mean 53.55
Std Dev 2.76
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
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40
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60
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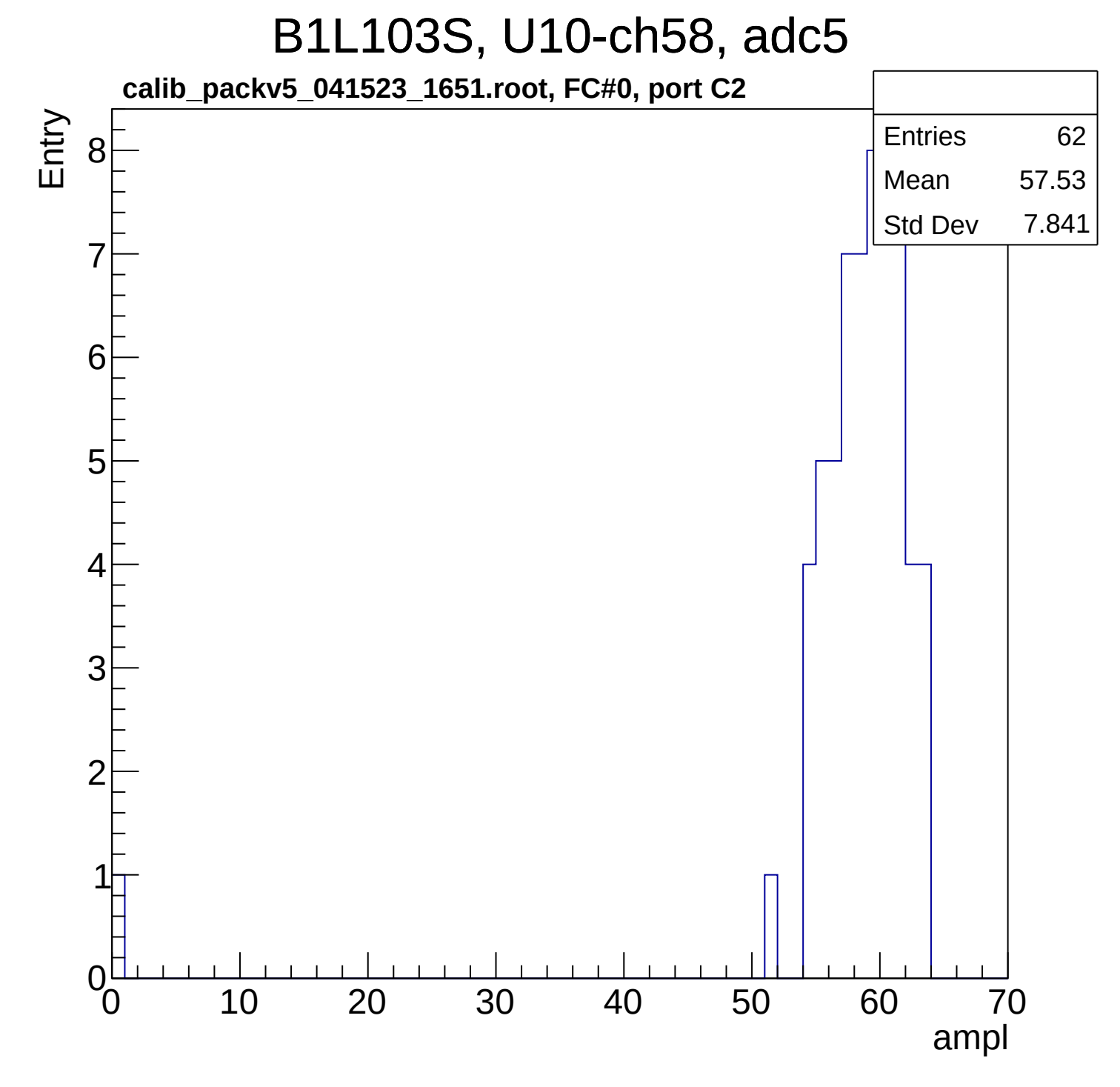
B1L103S, U10-ch58, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 57.53
Std Dev 7.841
Entry
ampl
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4
5
6
7
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0
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60
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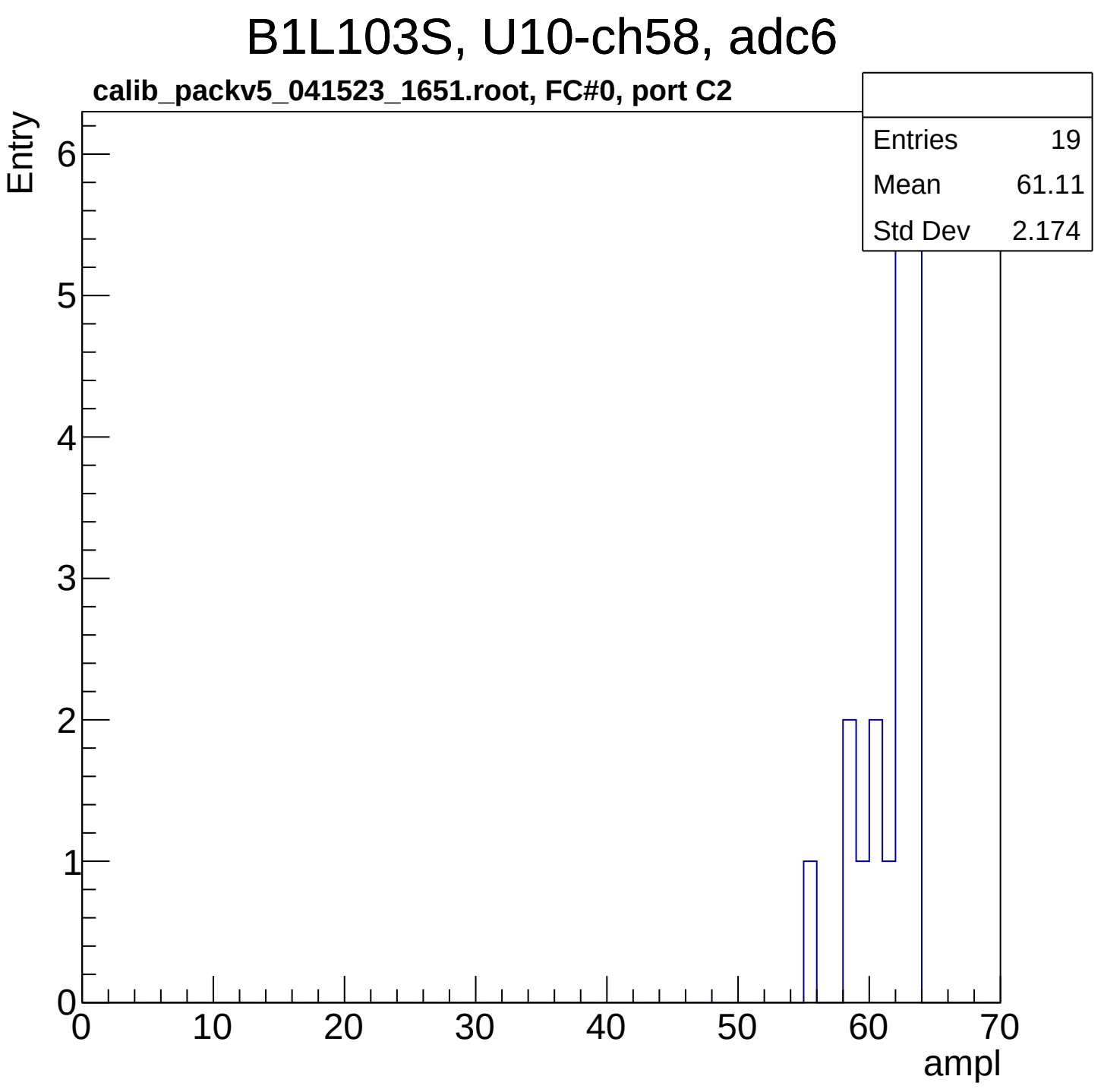
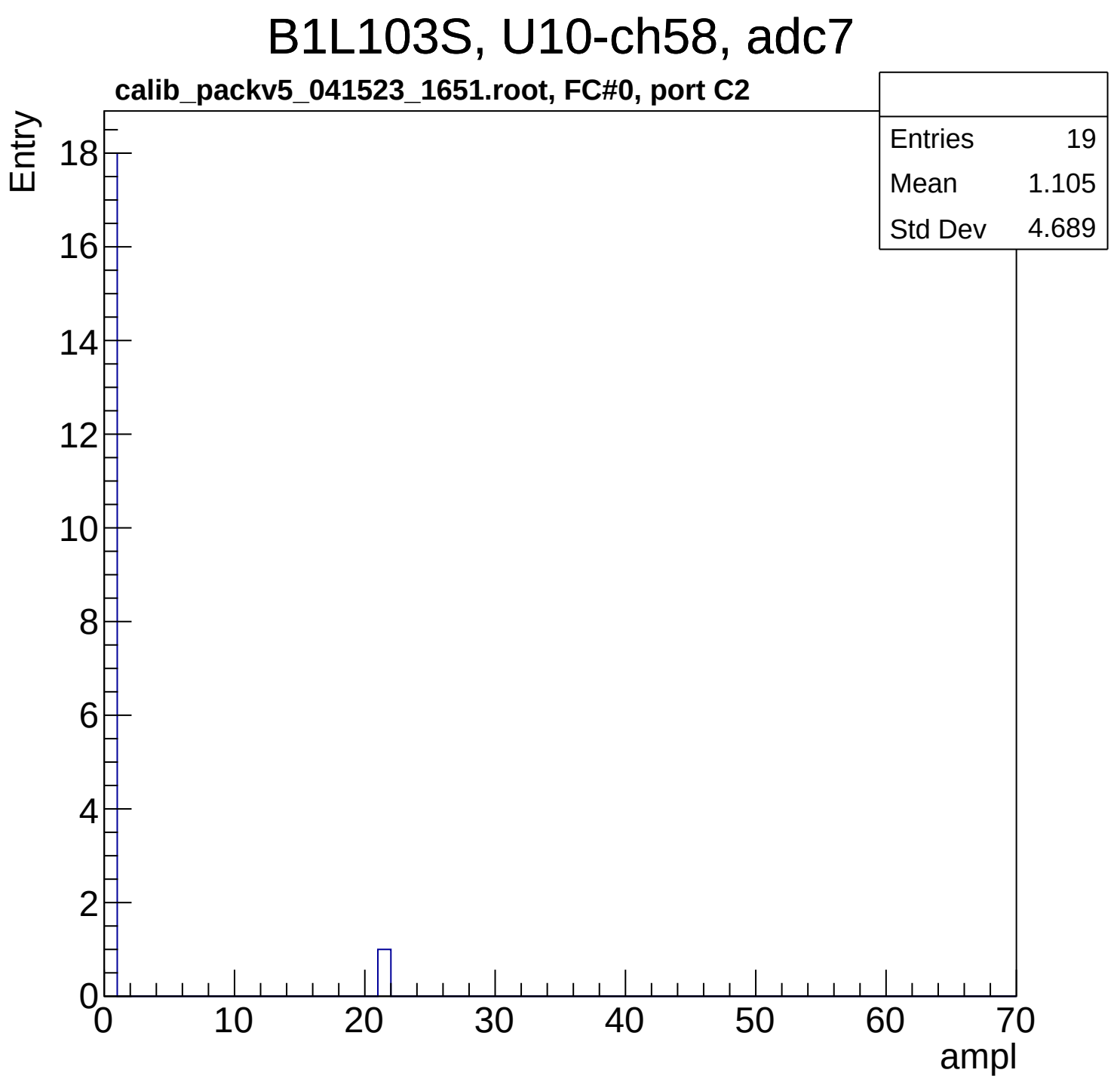

B1L103S, U10-ch58, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 61.11
Std Dev 2.174
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch58, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.105
Std Dev 4.689
Entry
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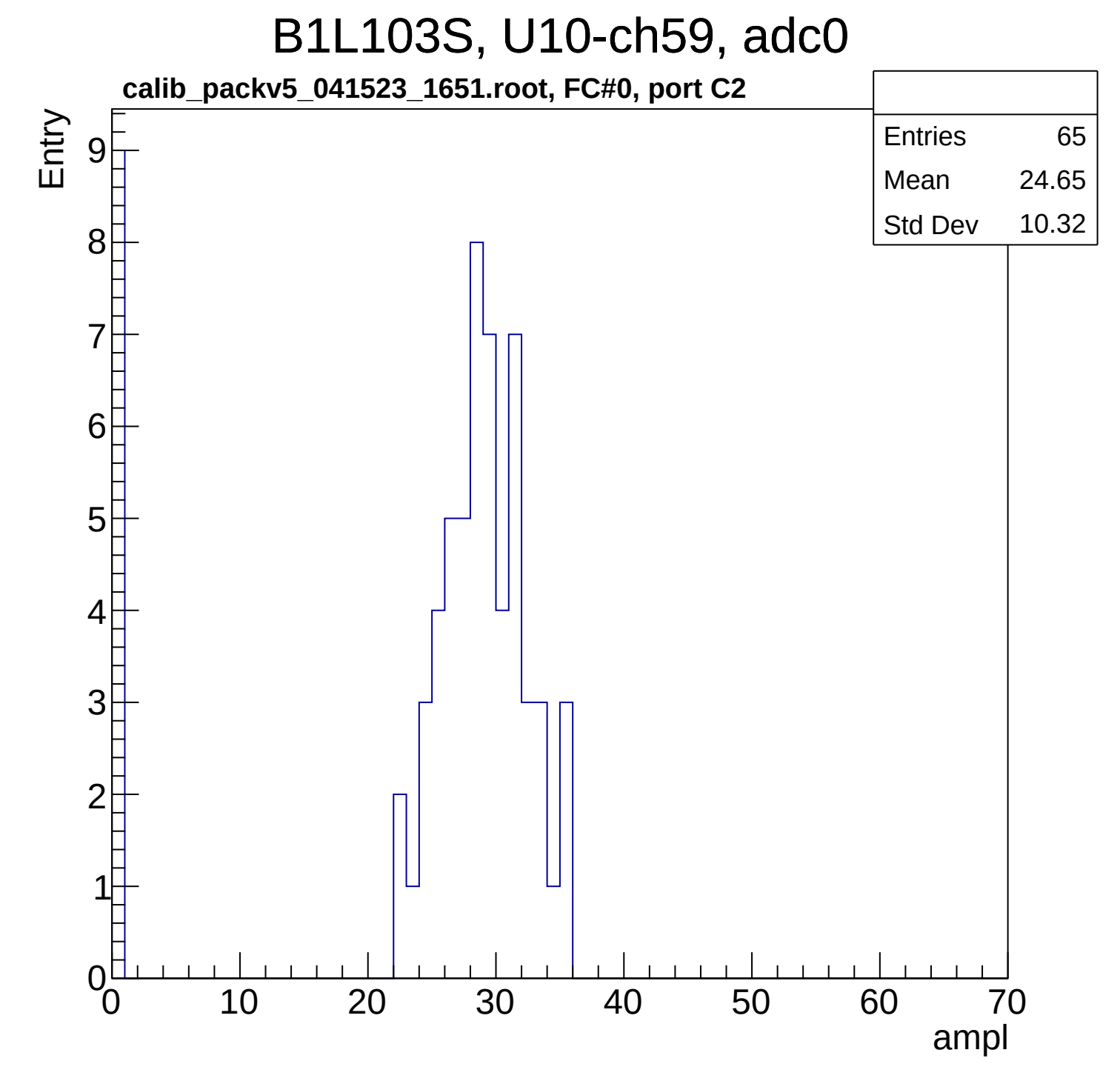
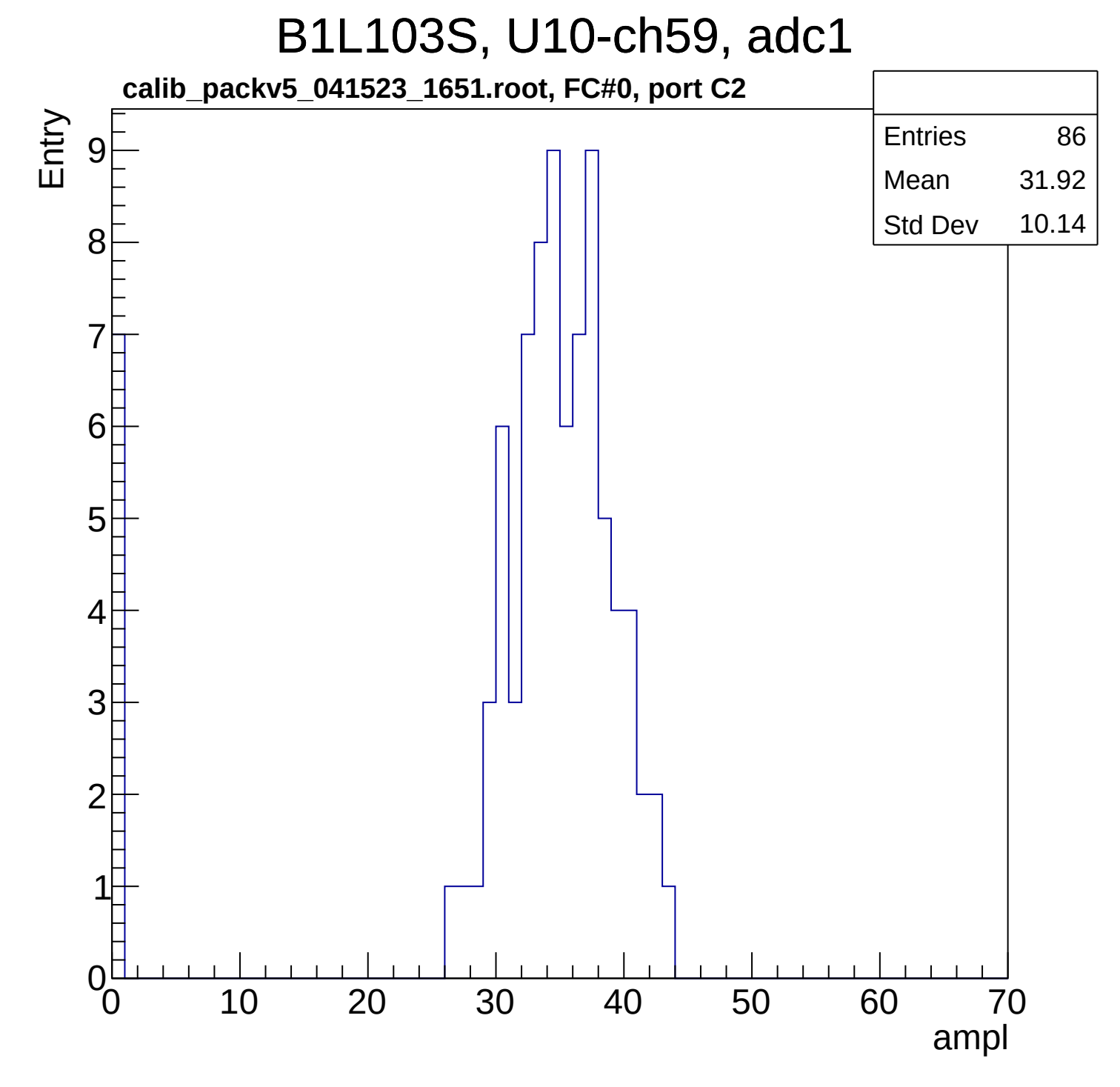
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch59, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 24.65
Std Dev 10.32
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U10-ch59, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 31.92
Std Dev 10.14
Entry
ampl
0
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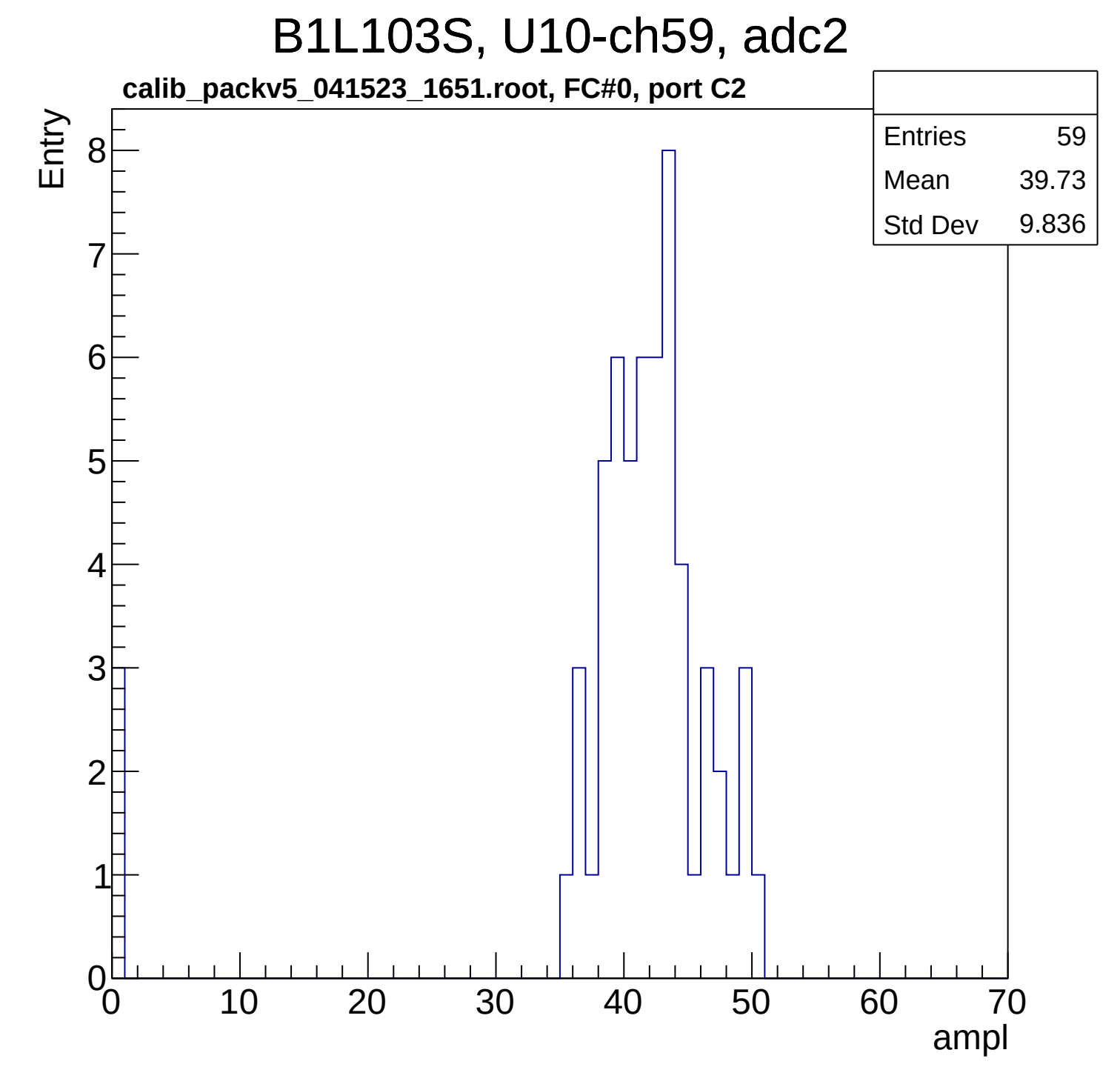
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U10-ch59, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 39.73
Std Dev 9.836
Entry
ampl
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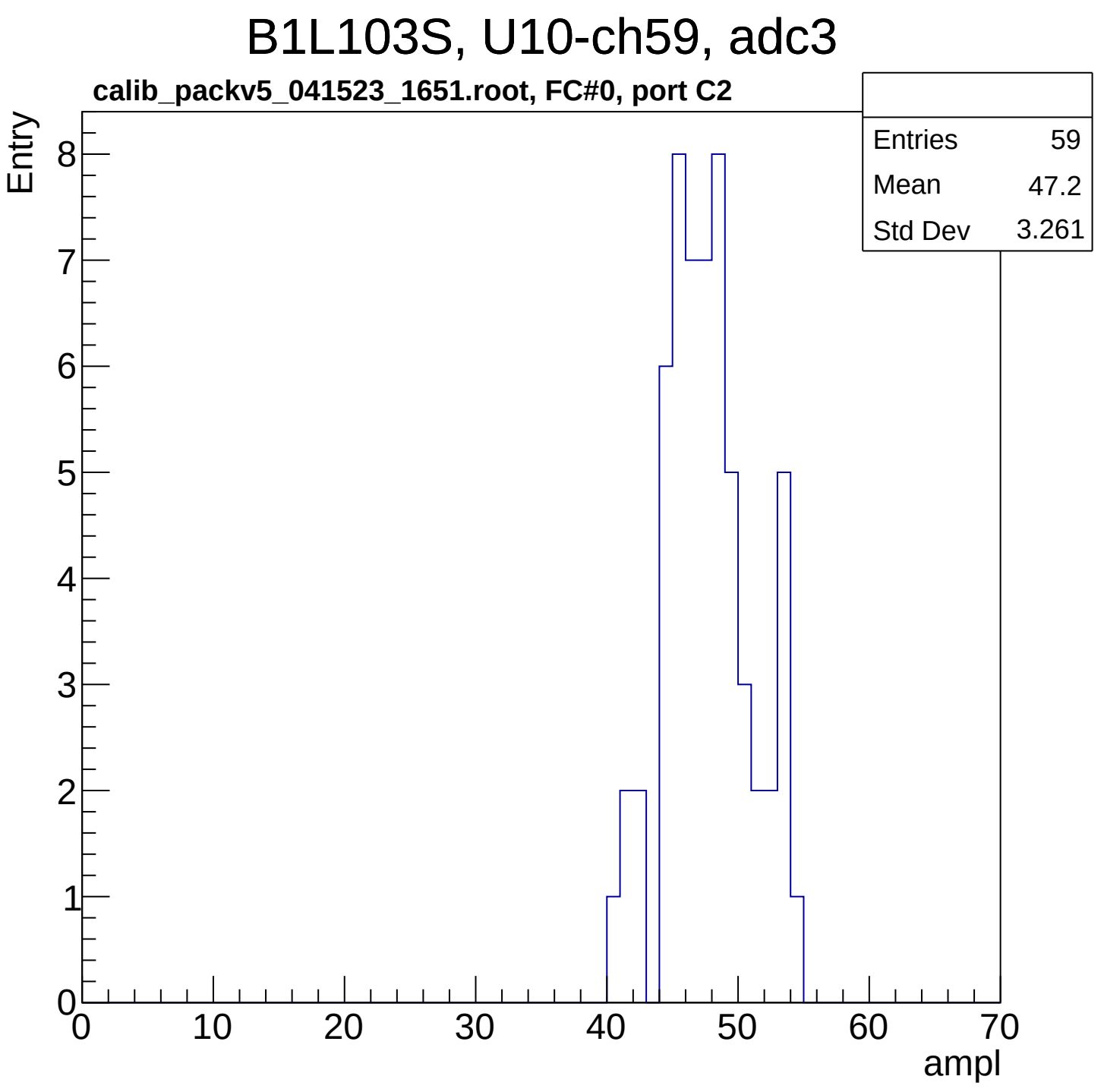
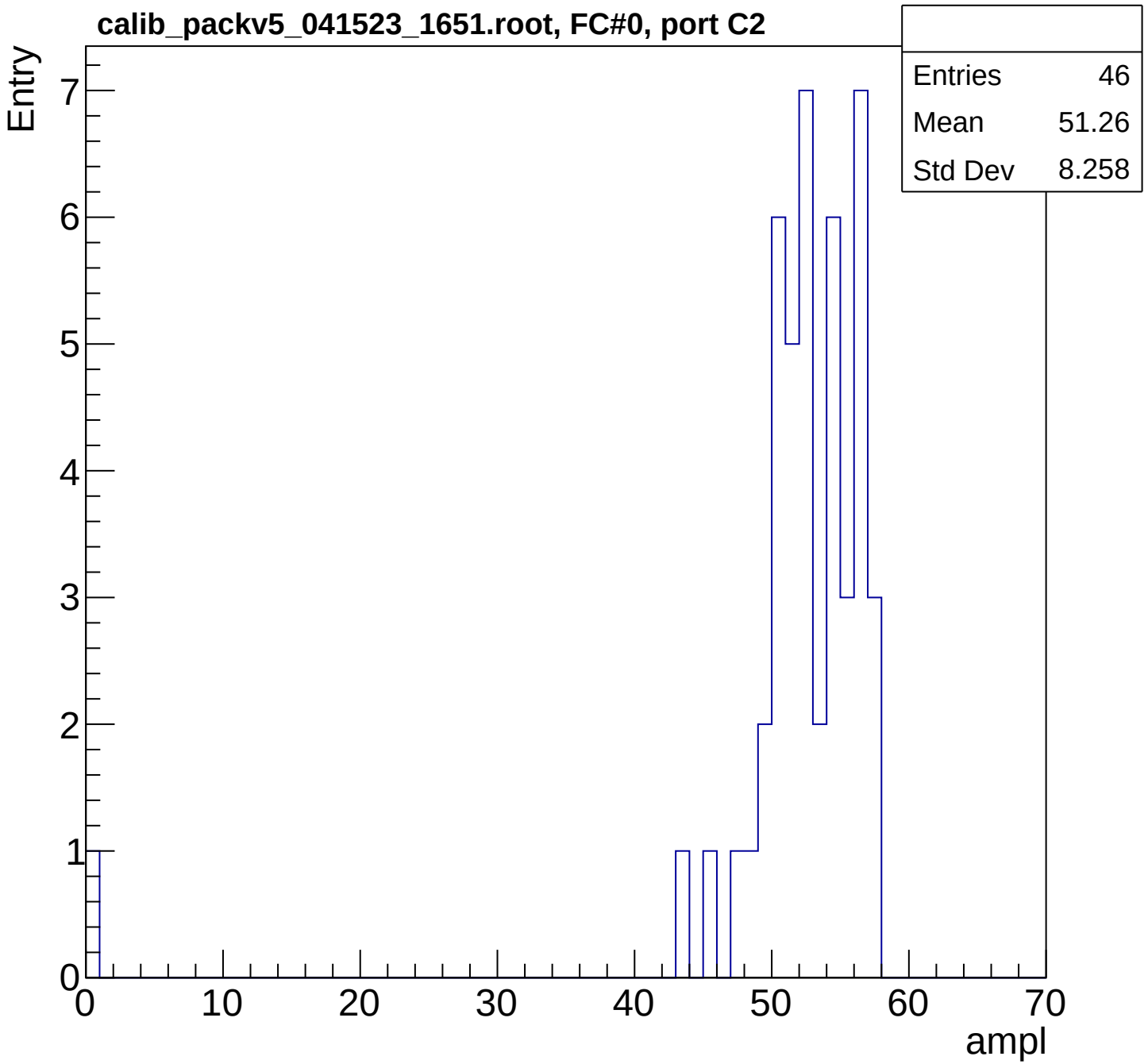
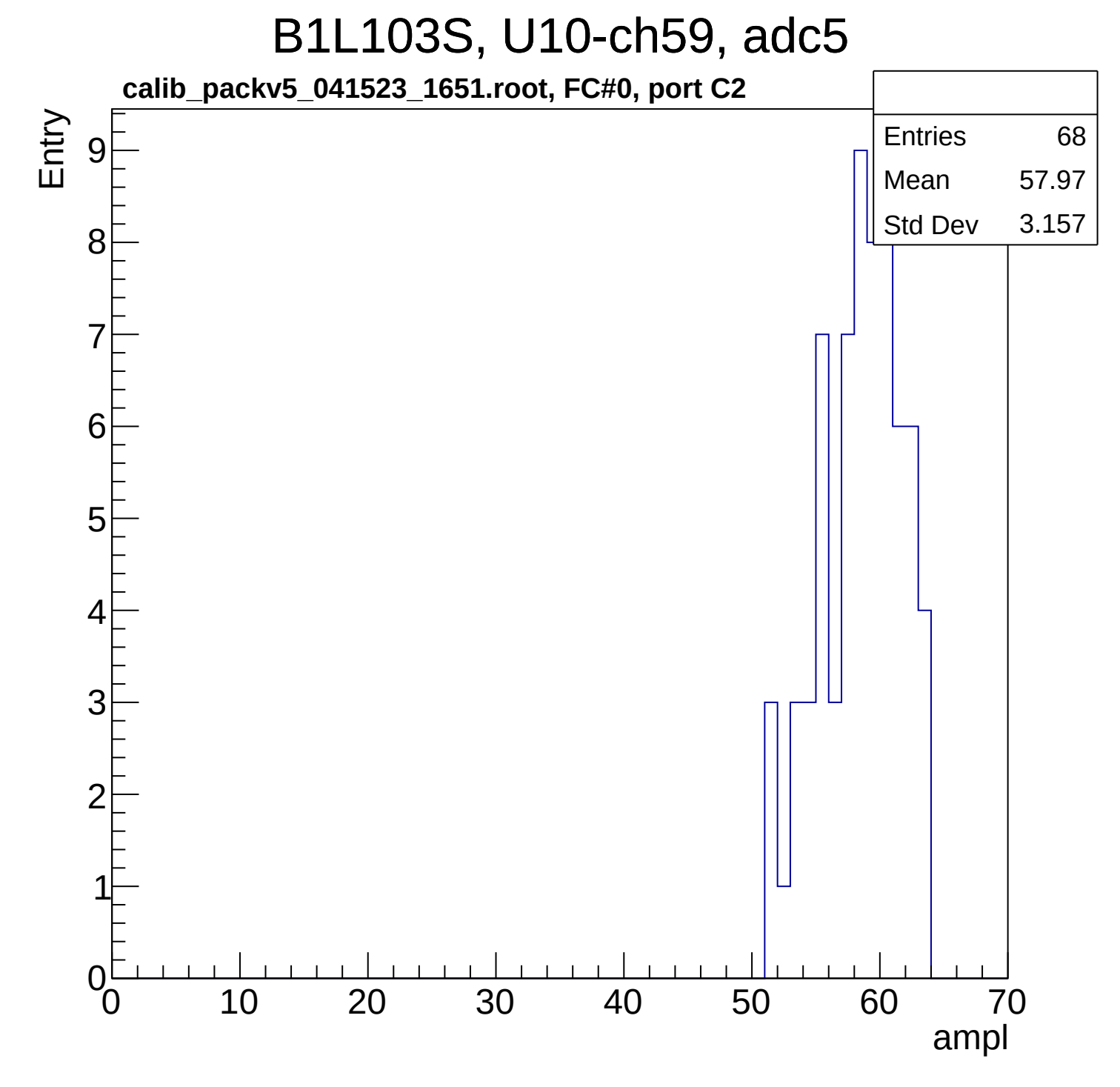
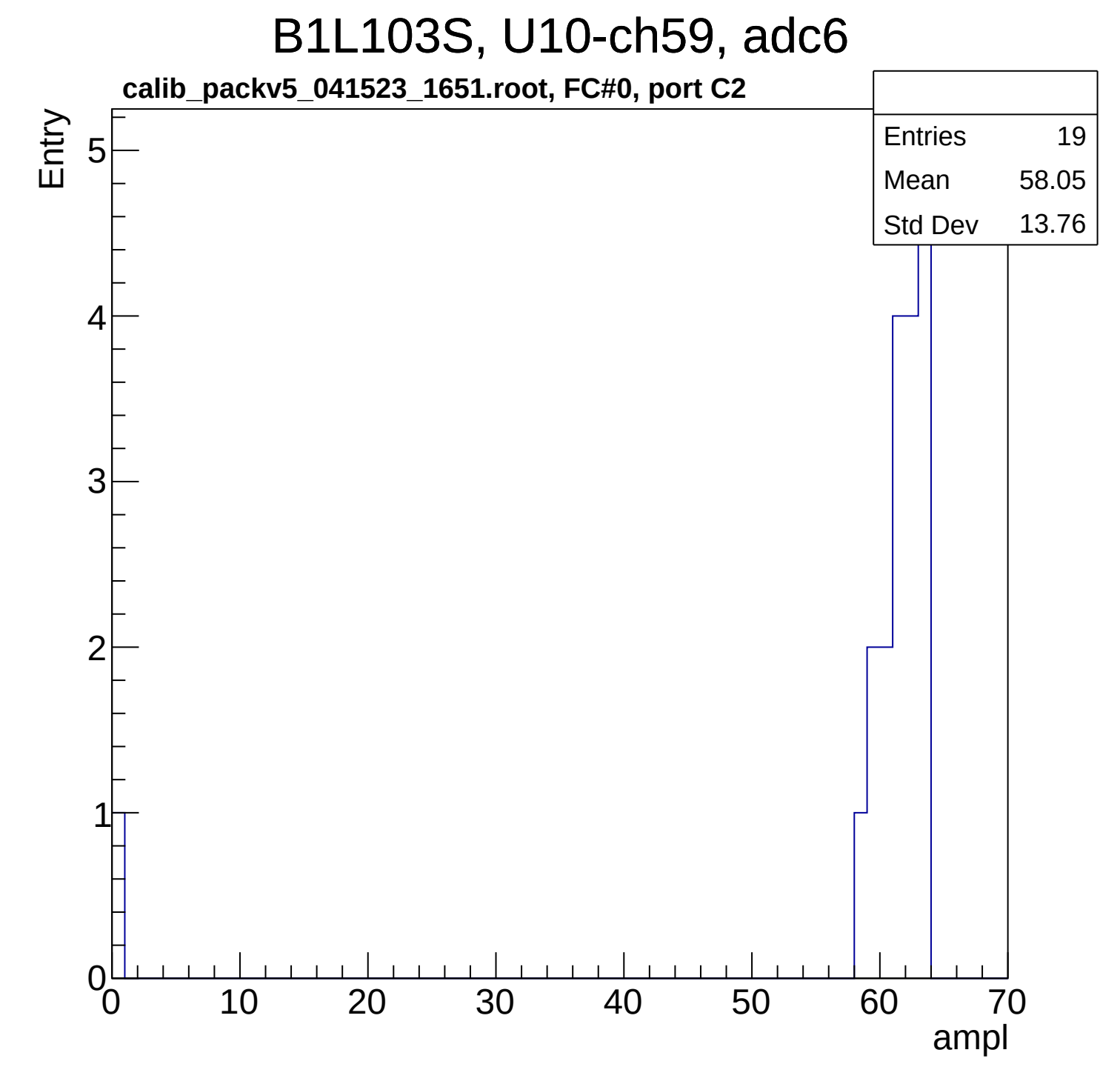
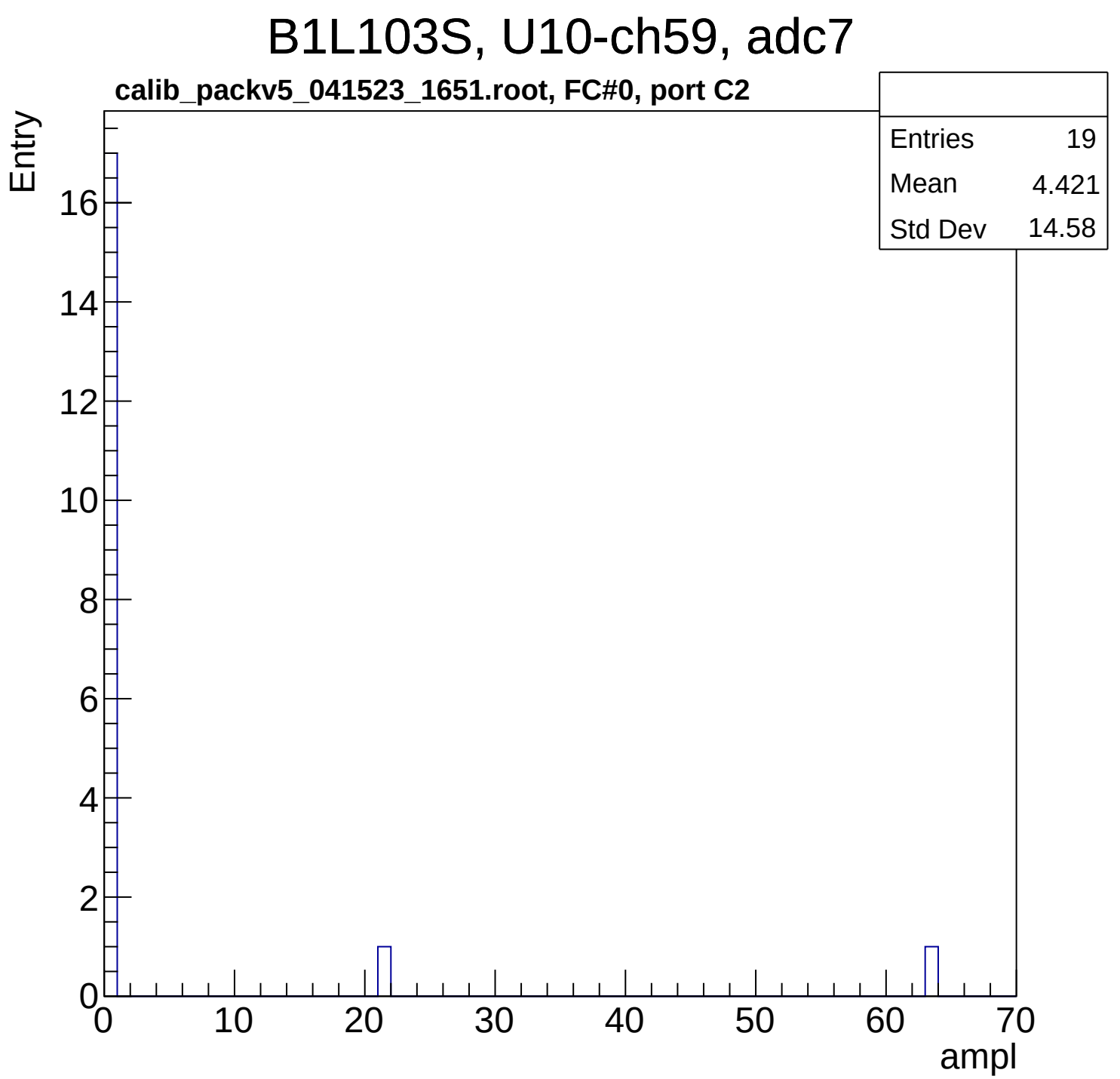
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U10-ch59, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 47.2
Std Dev 3.261
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U10-ch59, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 51.26
Std Dev 8.258
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U10-ch59, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 57.97
Std Dev 3.157
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U10-ch59, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 58.05
Std Dev 13.76
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U10-ch59, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 4.421
Std Dev 14.58
Entry
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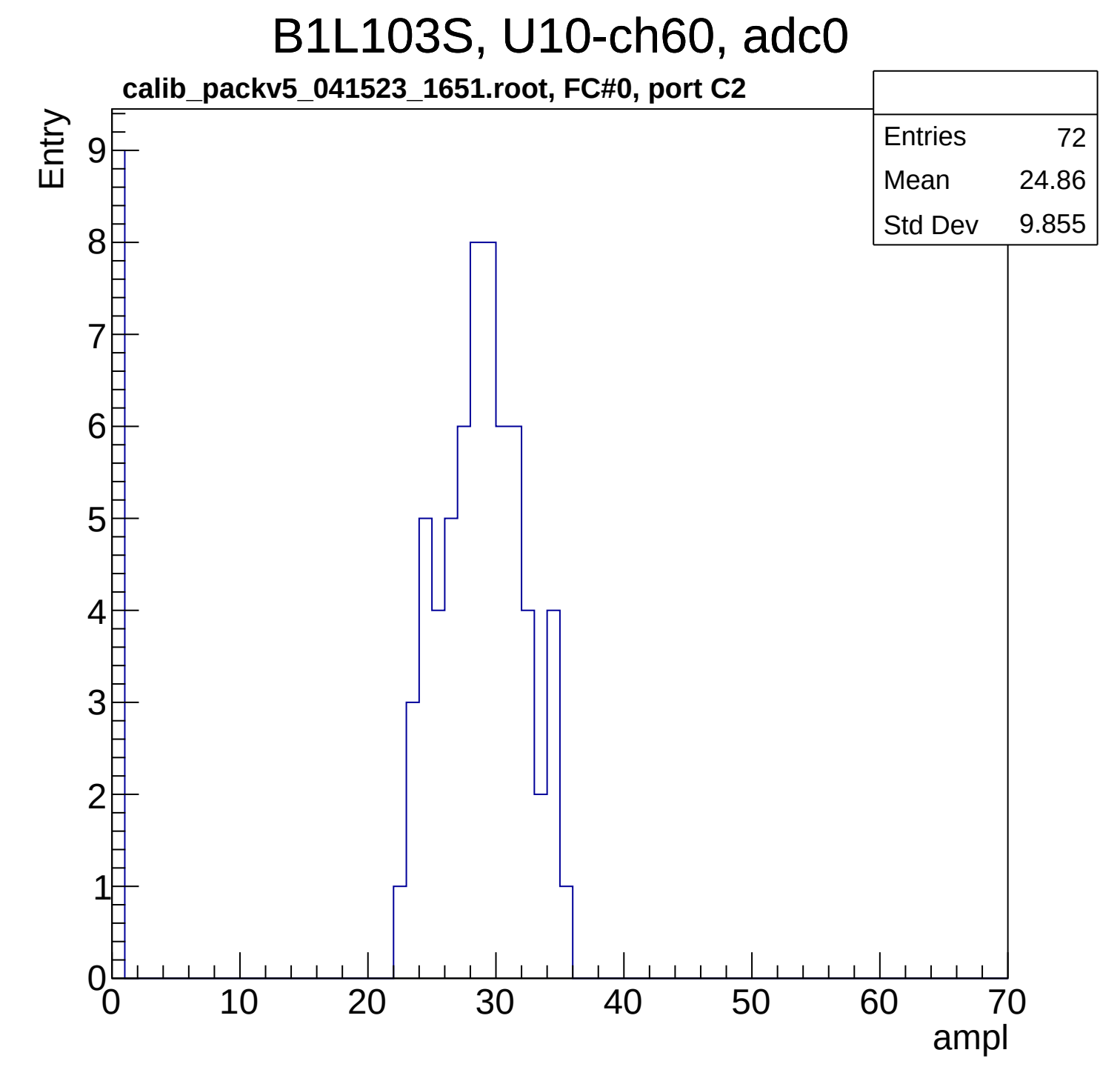
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch60, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 24.86
Std Dev 9.855
Entry
ampl
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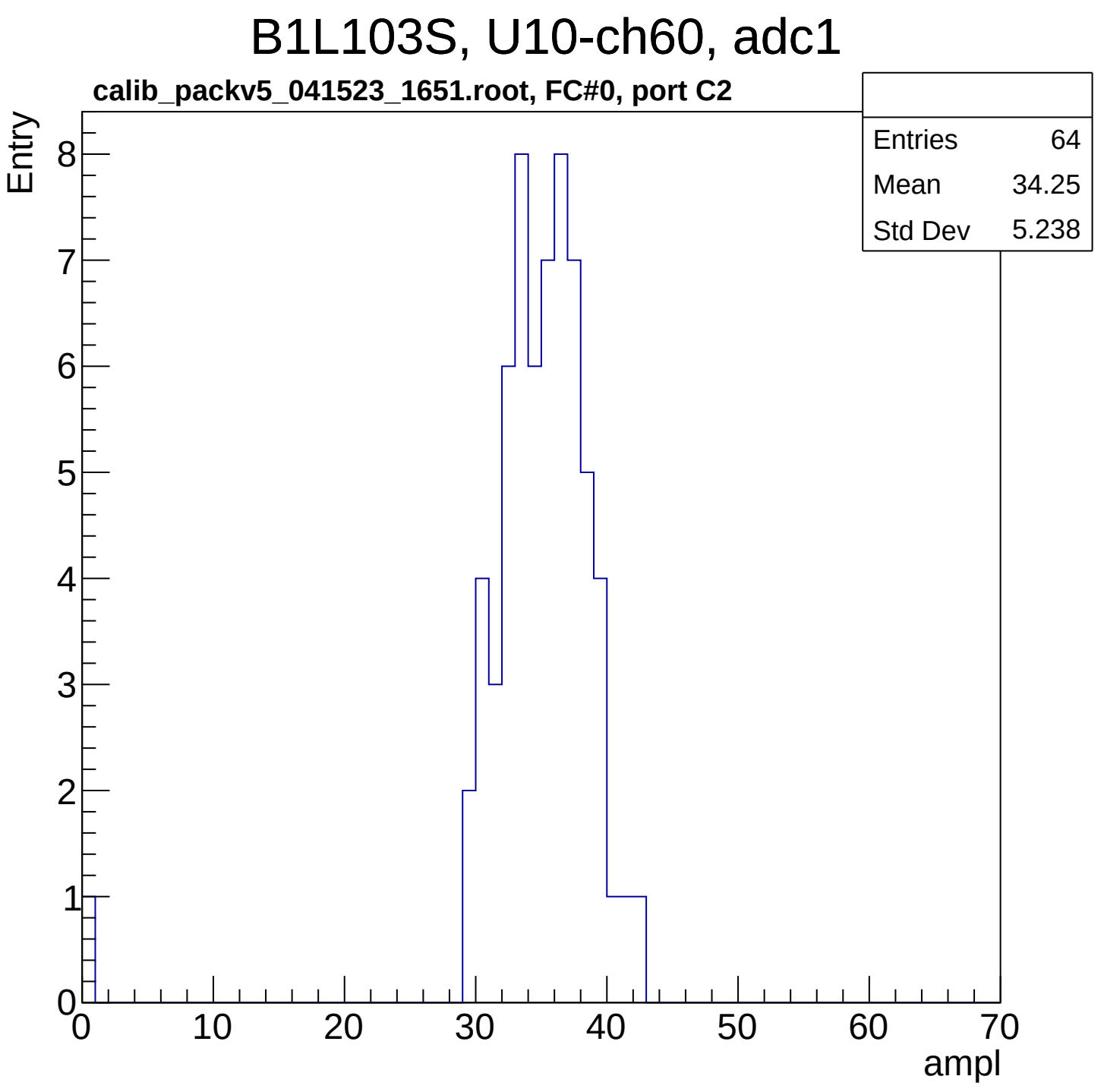
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U10-ch60, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 34.25
Std Dev 5.238
Entry
ampl
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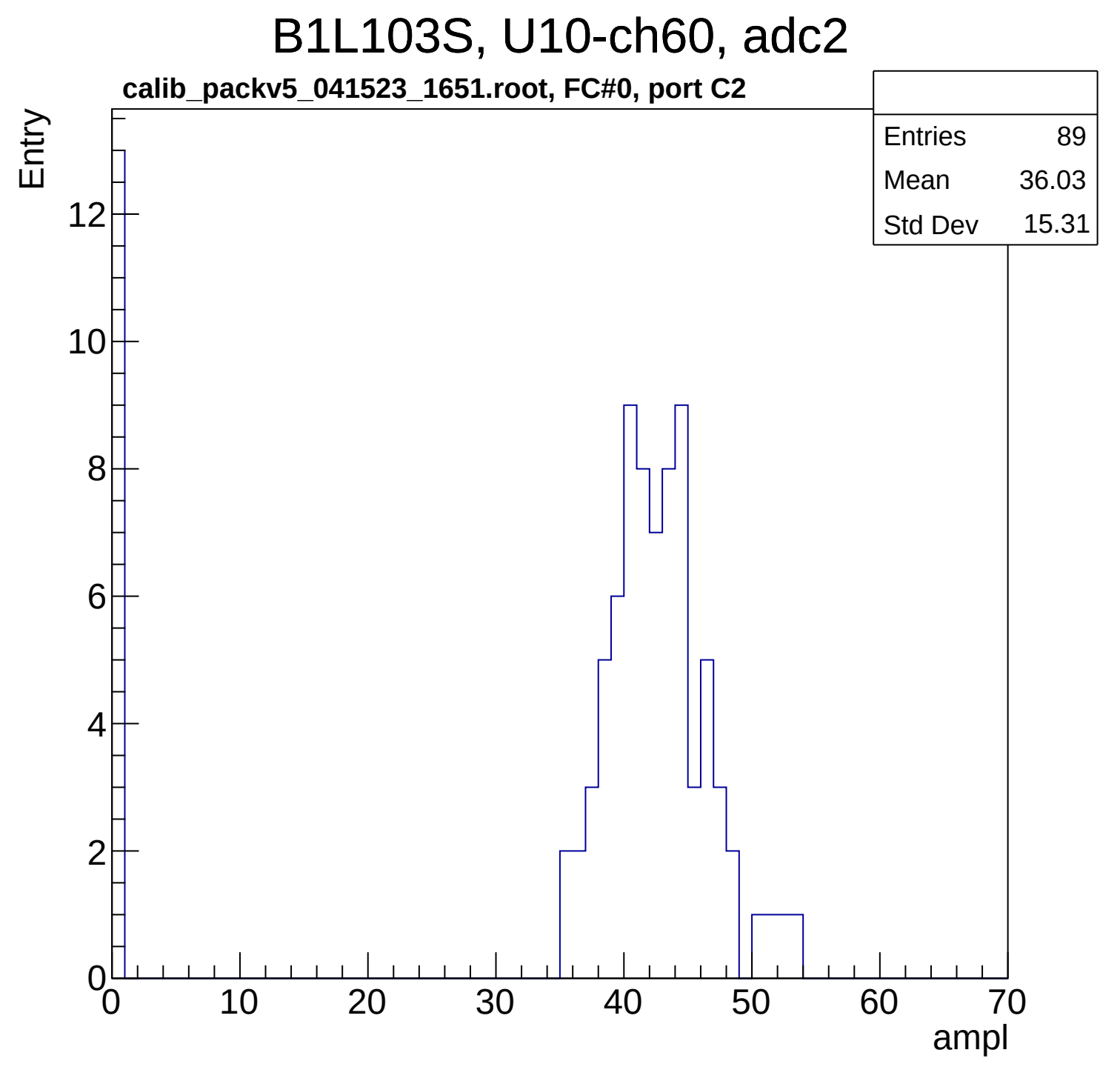
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U10-ch60, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 89
Mean 36.03
Std Dev 15.31
Entry
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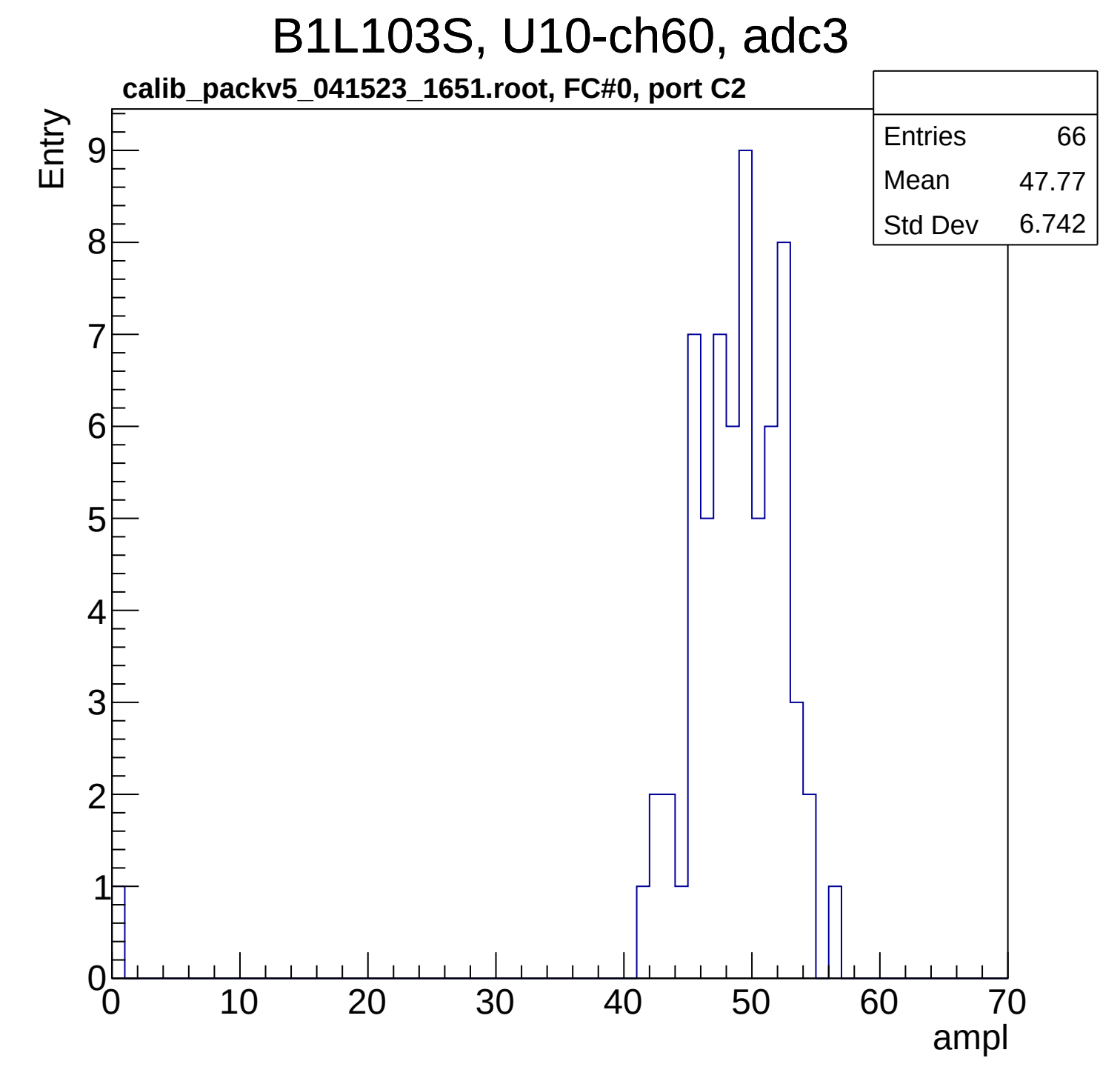
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch60, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 47.77
Std Dev 6.742
Entry
ampl
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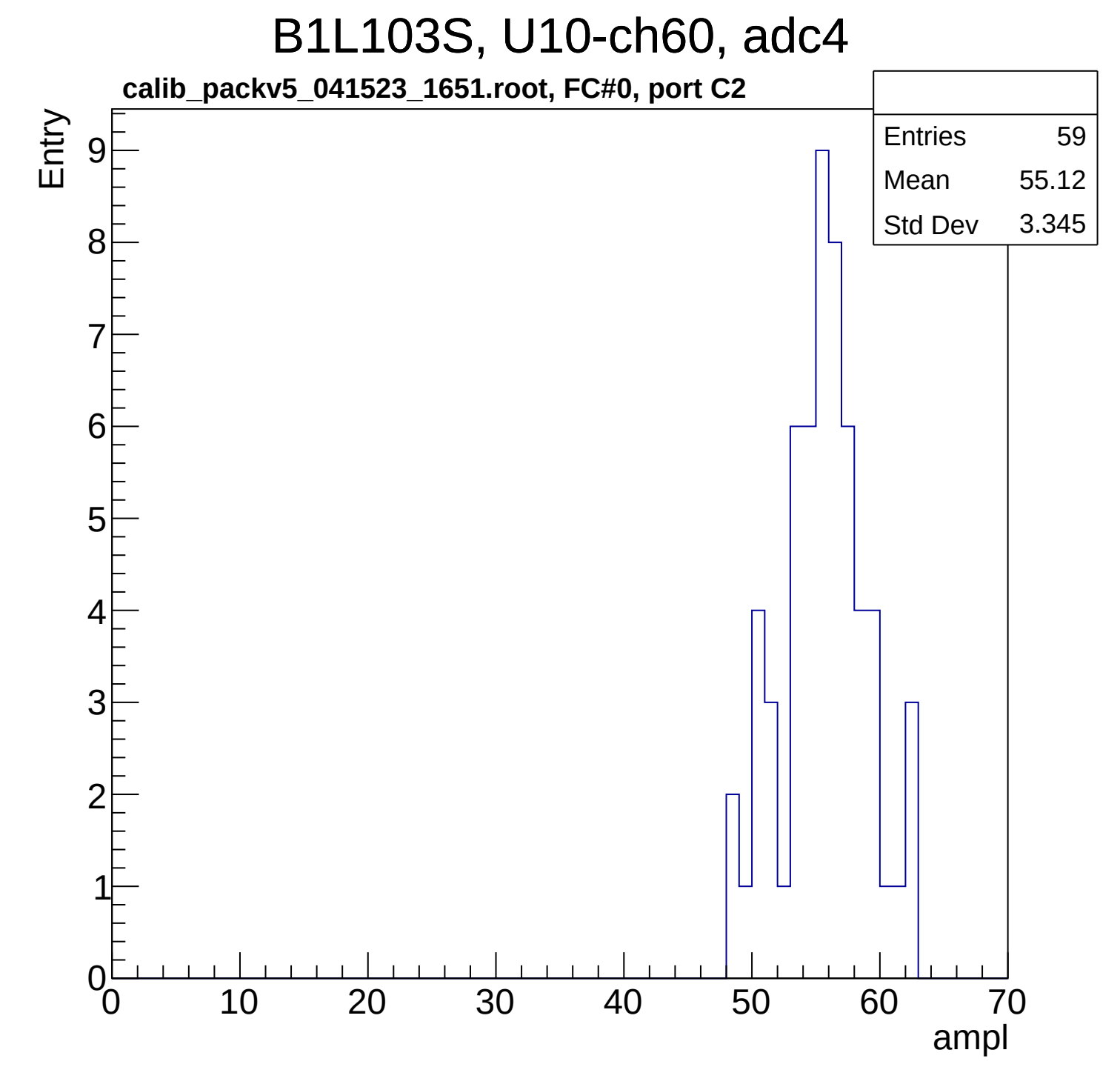
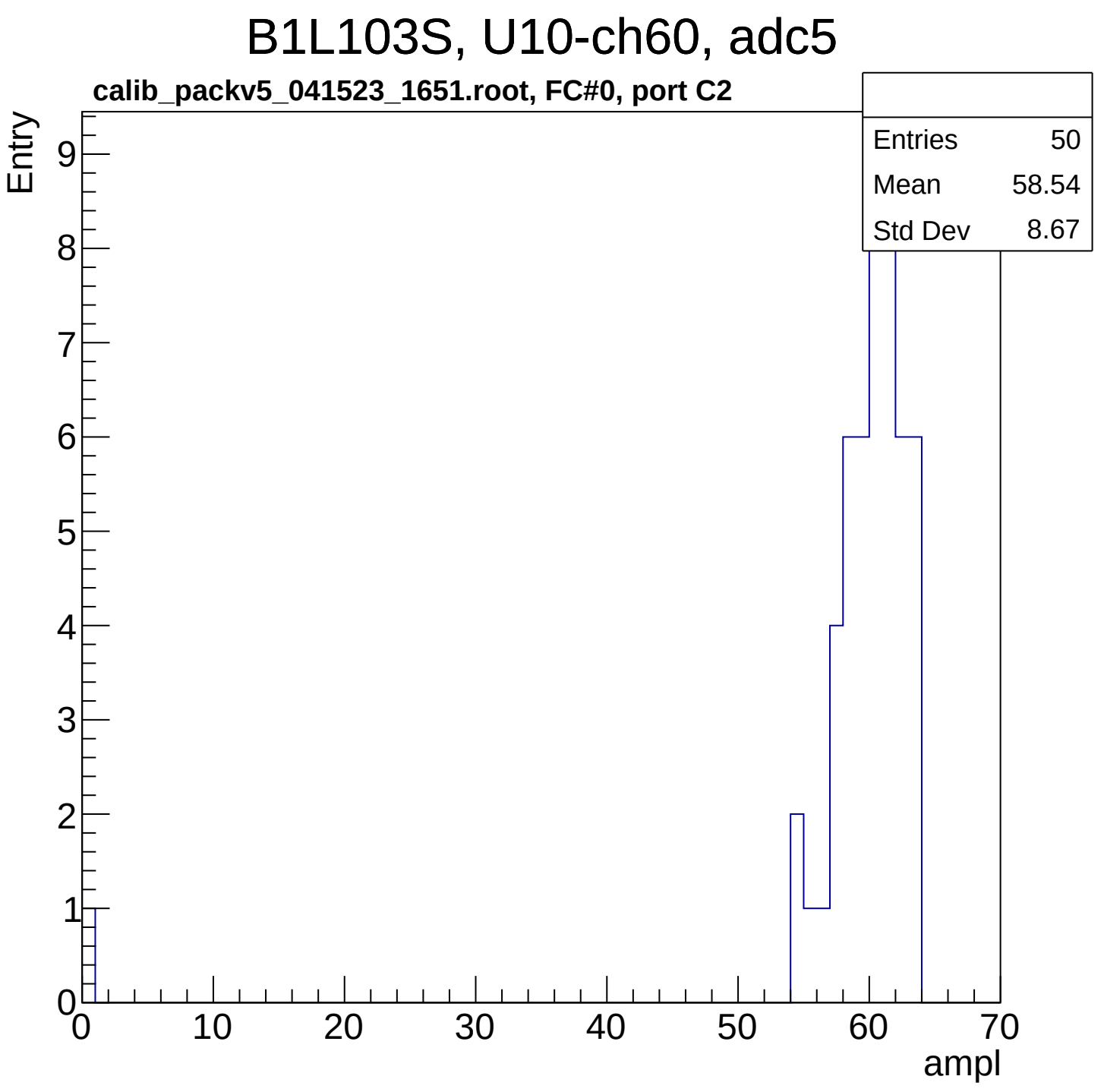
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U10-ch60, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 55.12
Std Dev 3.345
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U10-ch60, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 58.54
Std Dev 8.67
Entry
ampl
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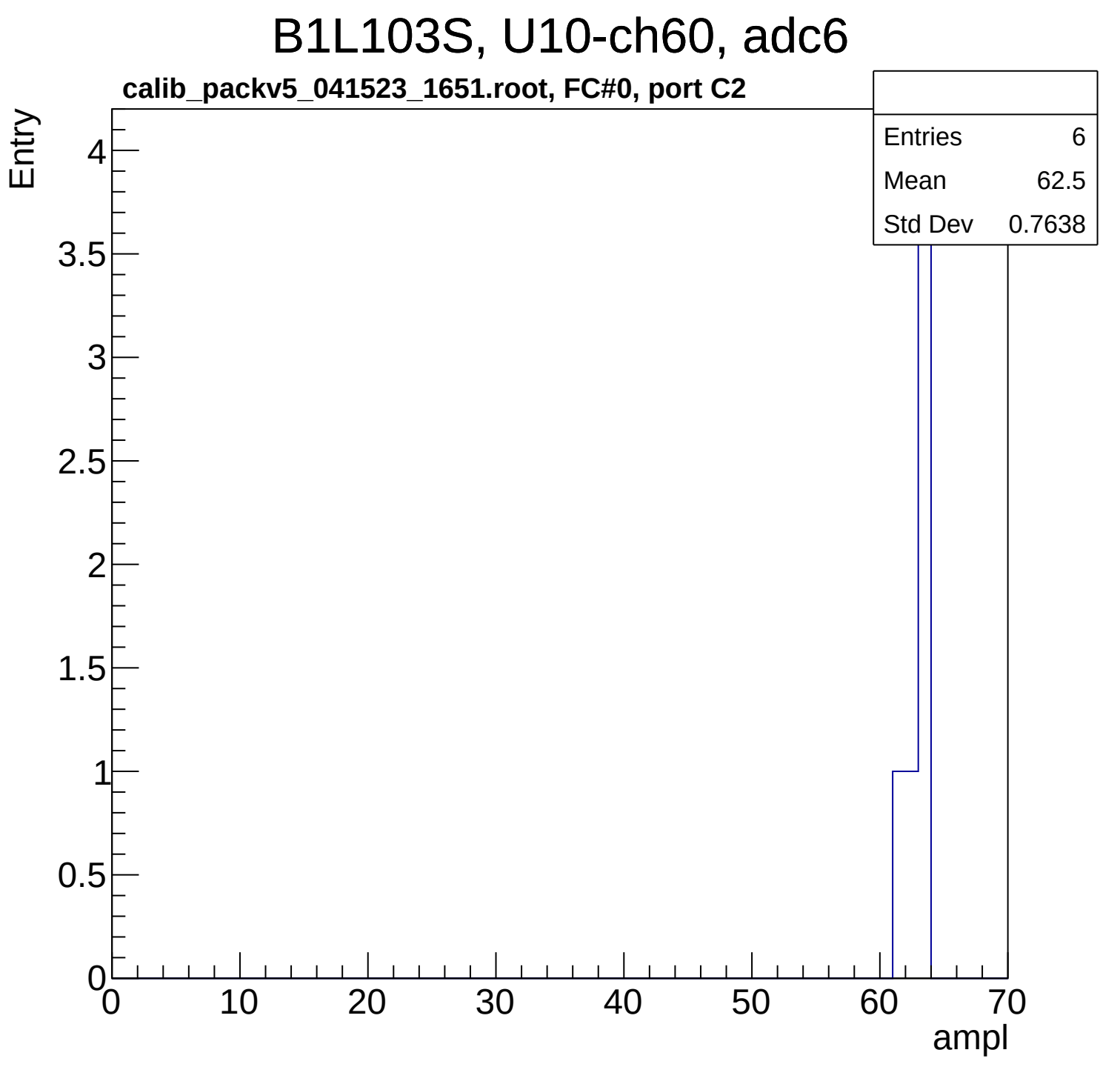
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U10-ch60, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 62.5
Std Dev 0.7638
Entry
ampl
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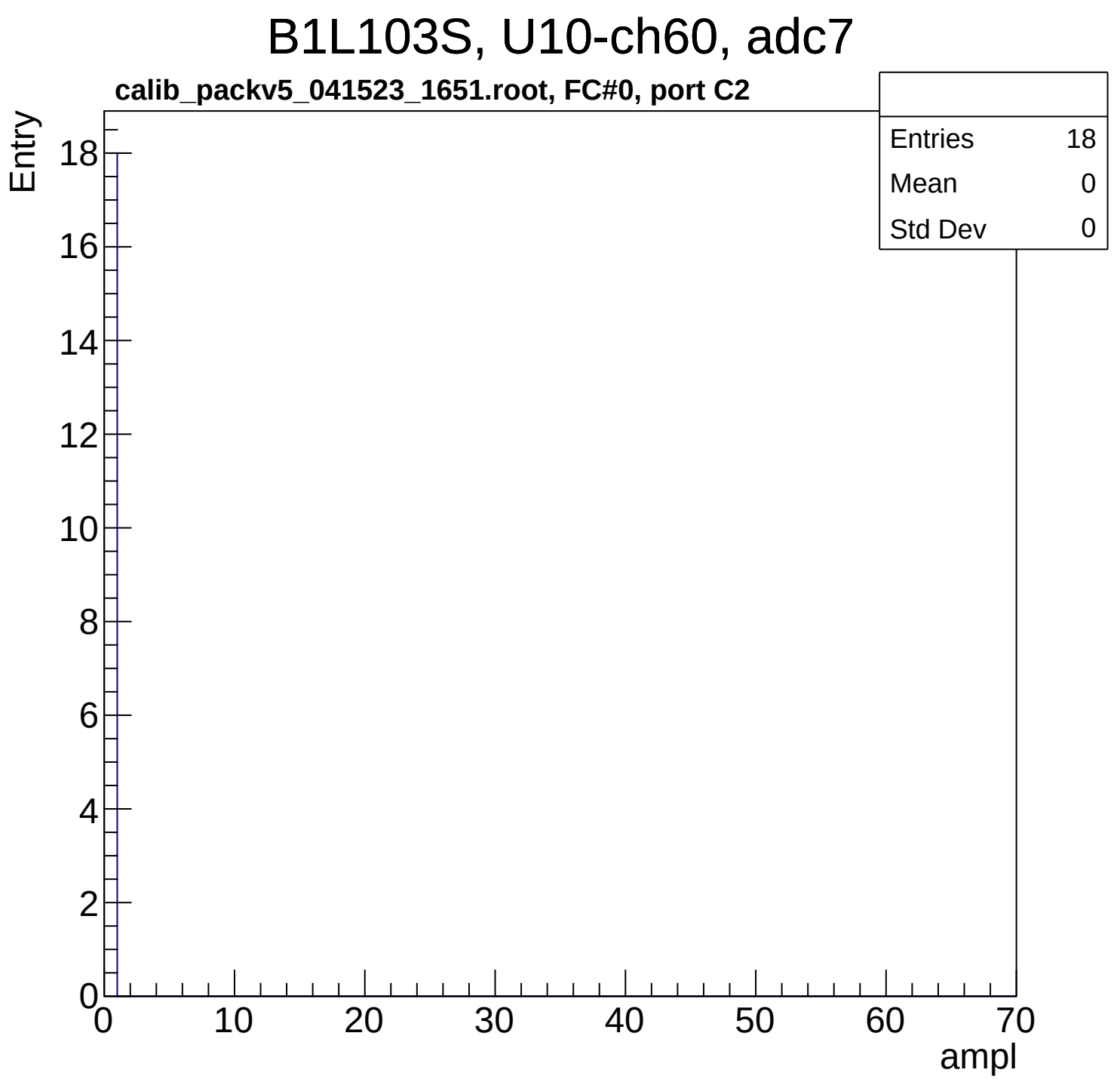
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U10-ch60, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
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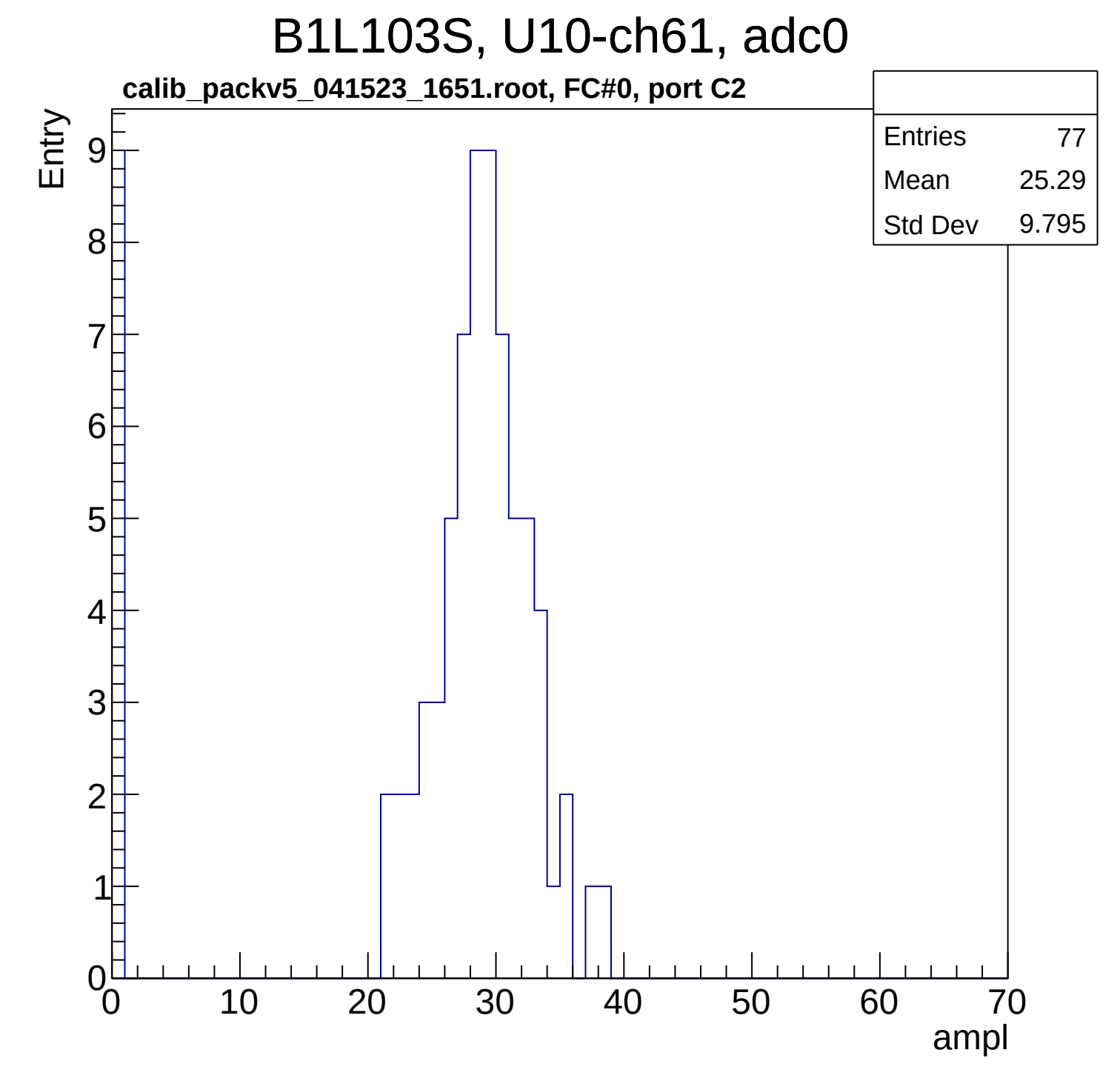
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch61, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 25.29
Std Dev 9.795
Entry
ampl
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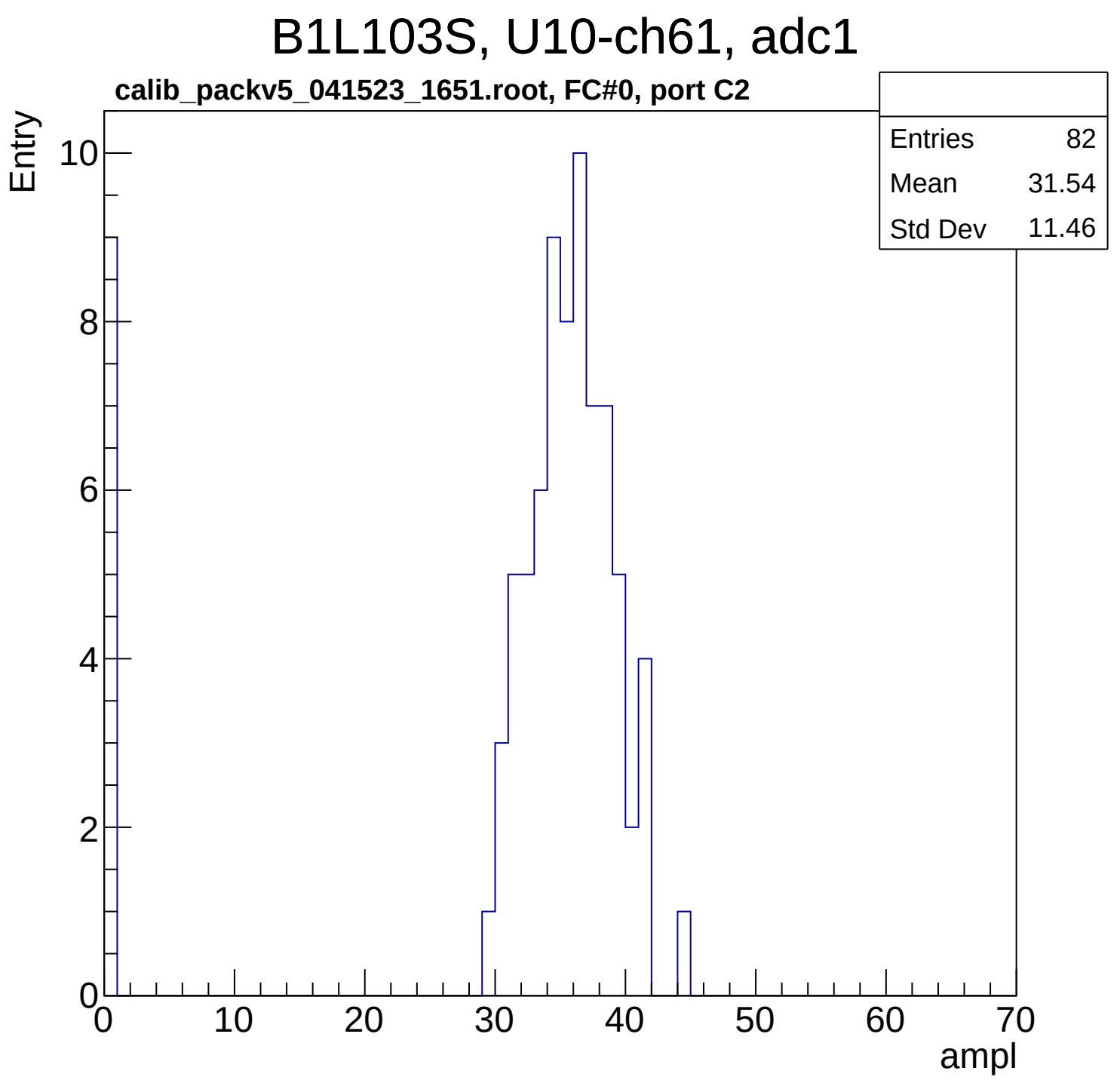
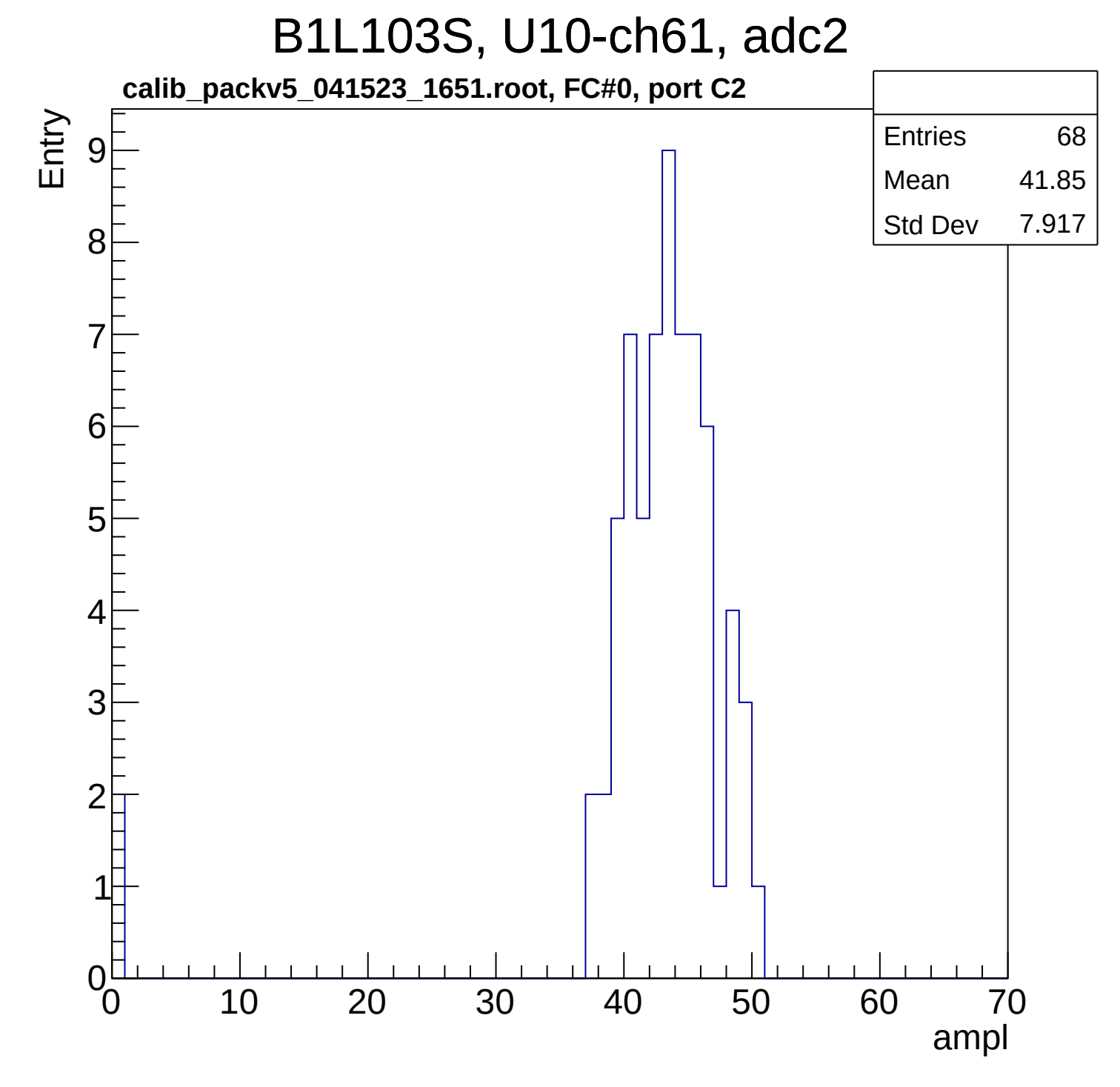
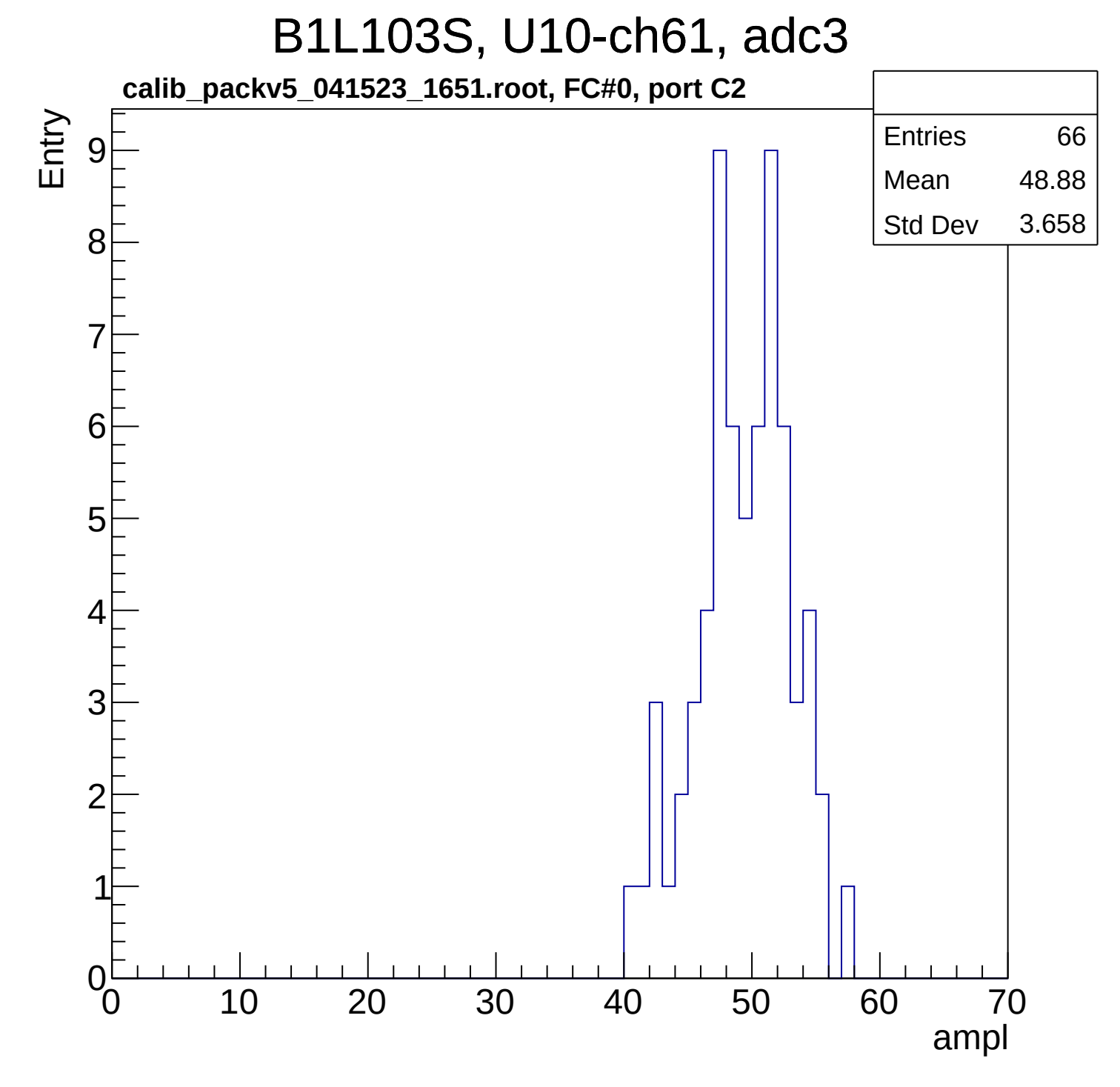
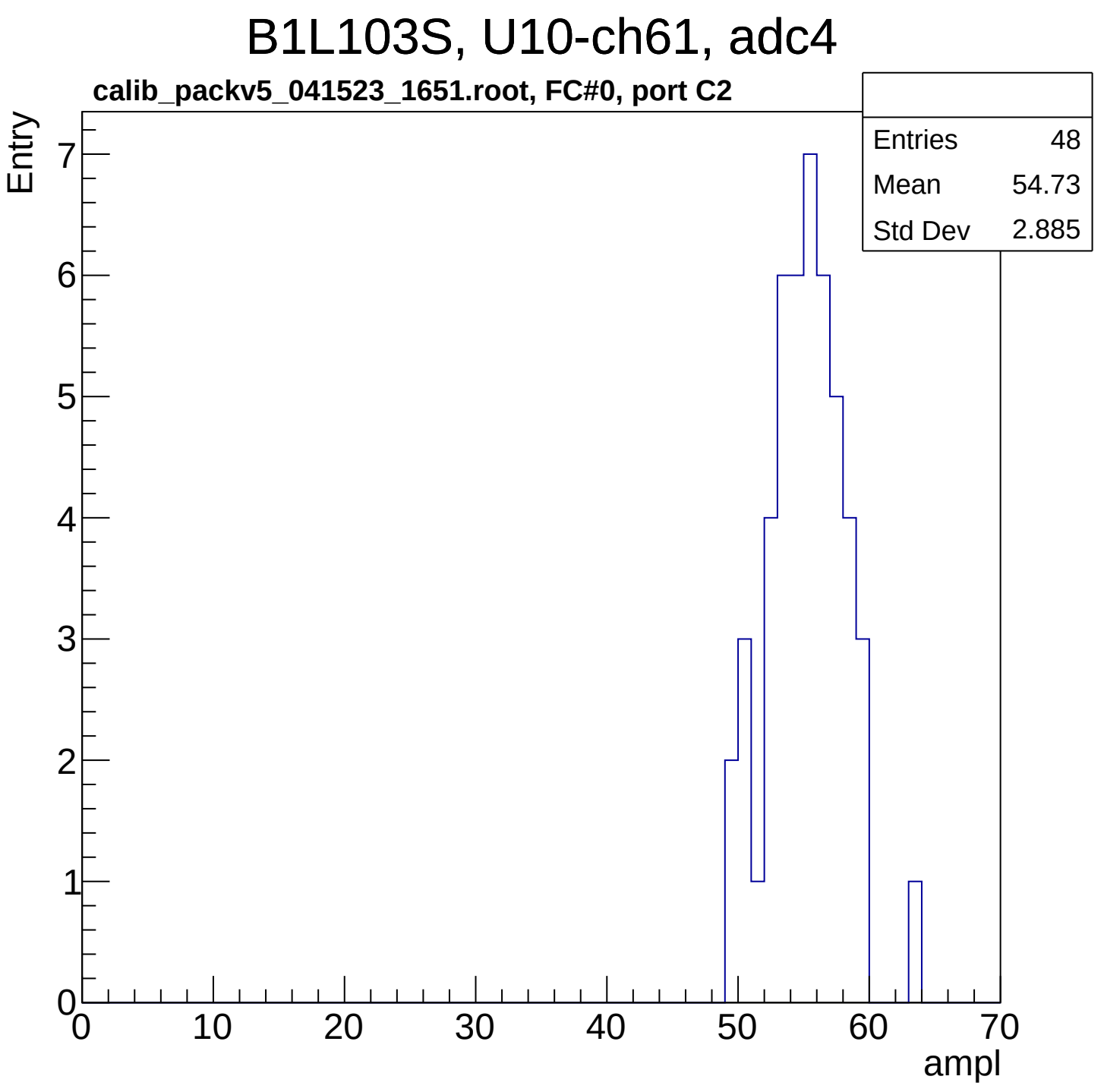
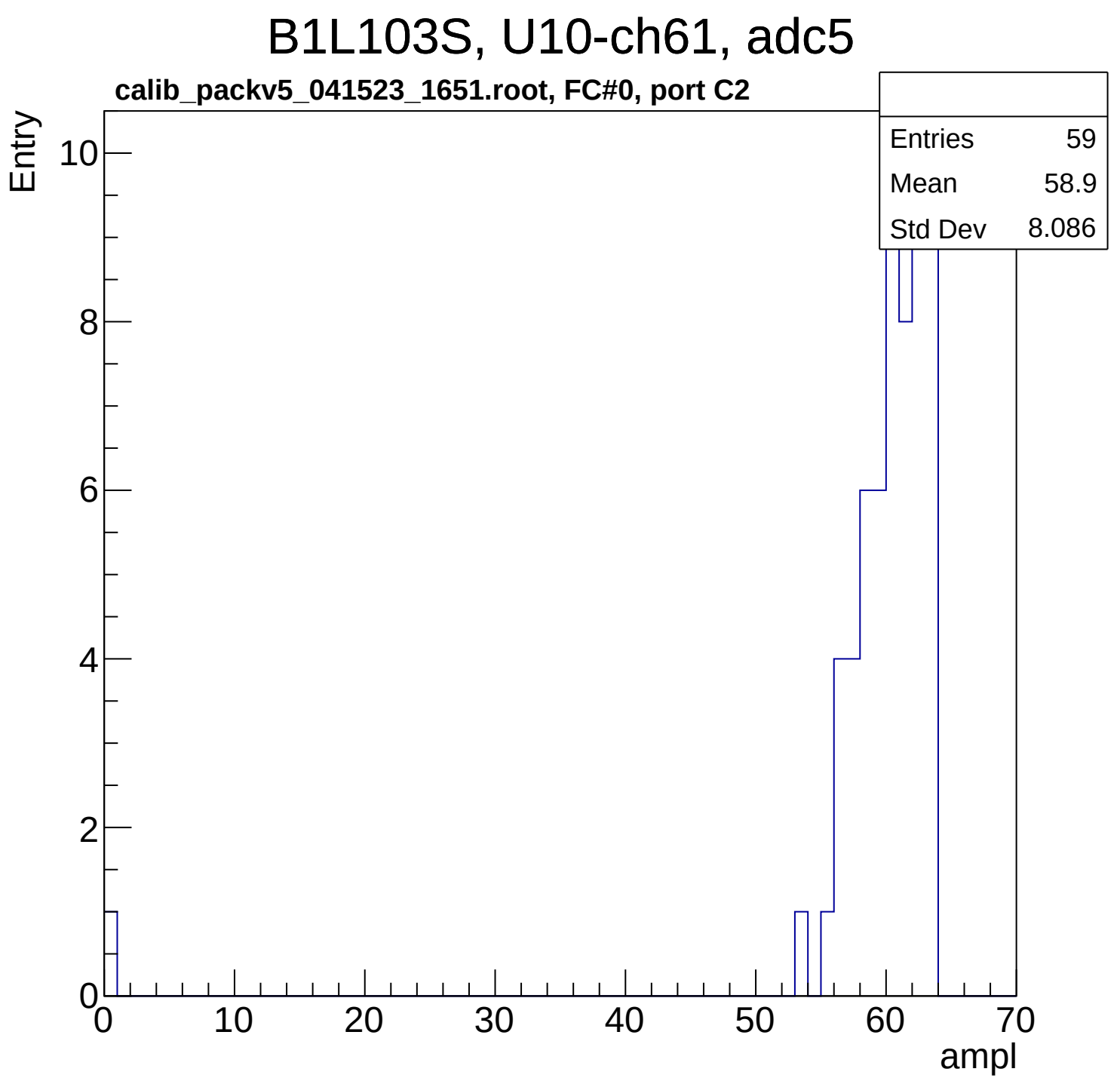
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

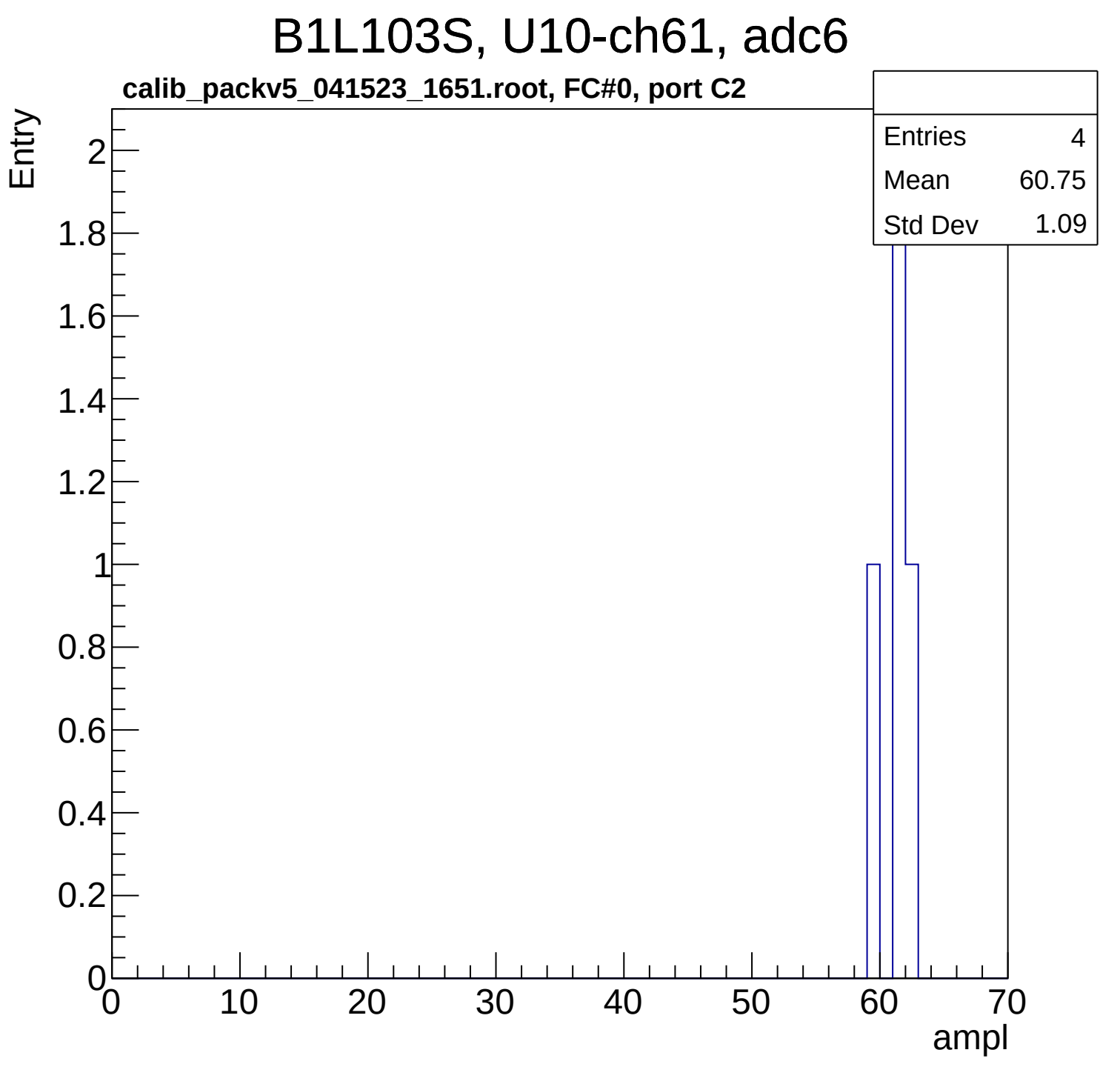

B1L103S, U10-ch61, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 31.54
Std Dev 11.46
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

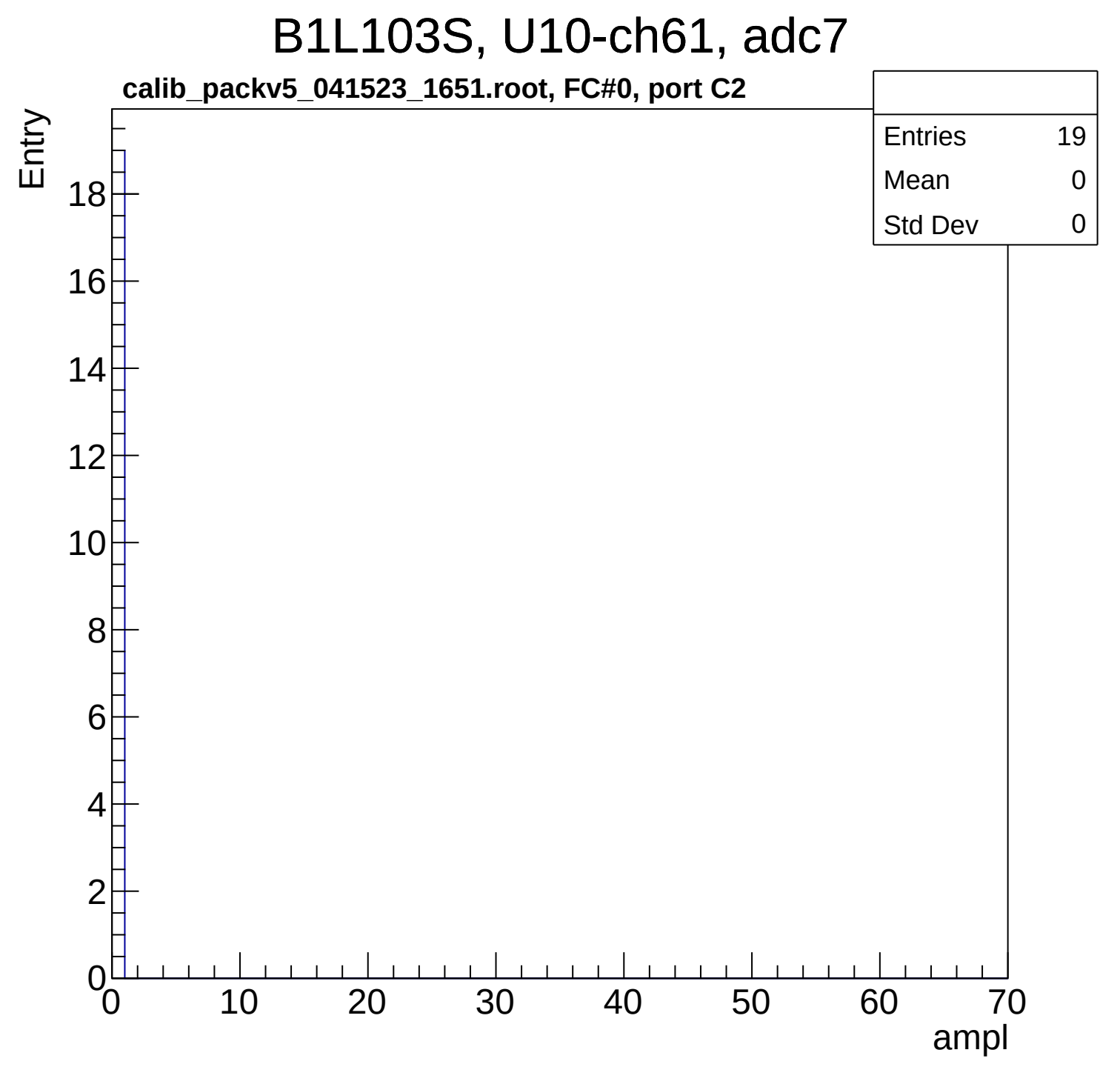

B1L103S, U10-ch61, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 41.85
Std Dev 7.917
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

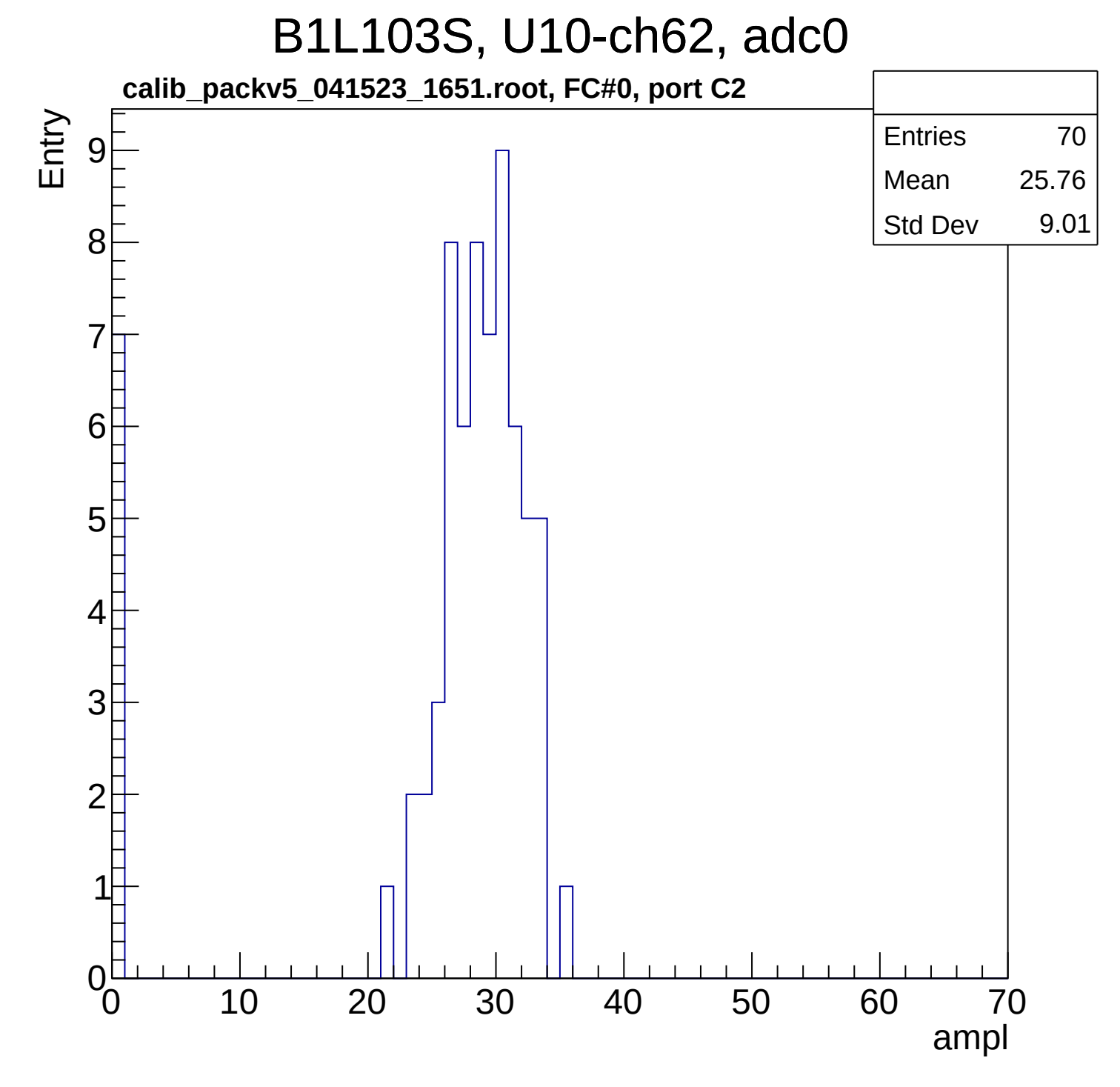

B1L103S, U10-ch61, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 48.88
Std Dev 3.658
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U10-ch61, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 54.73
Std Dev 2.885
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U10-ch61, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 58.9
Std Dev 8.086
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U10-ch61, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 4
Mean 60.75
Std Dev 1.09
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U10-ch61, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch62, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 25.76
Std Dev 9.01
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
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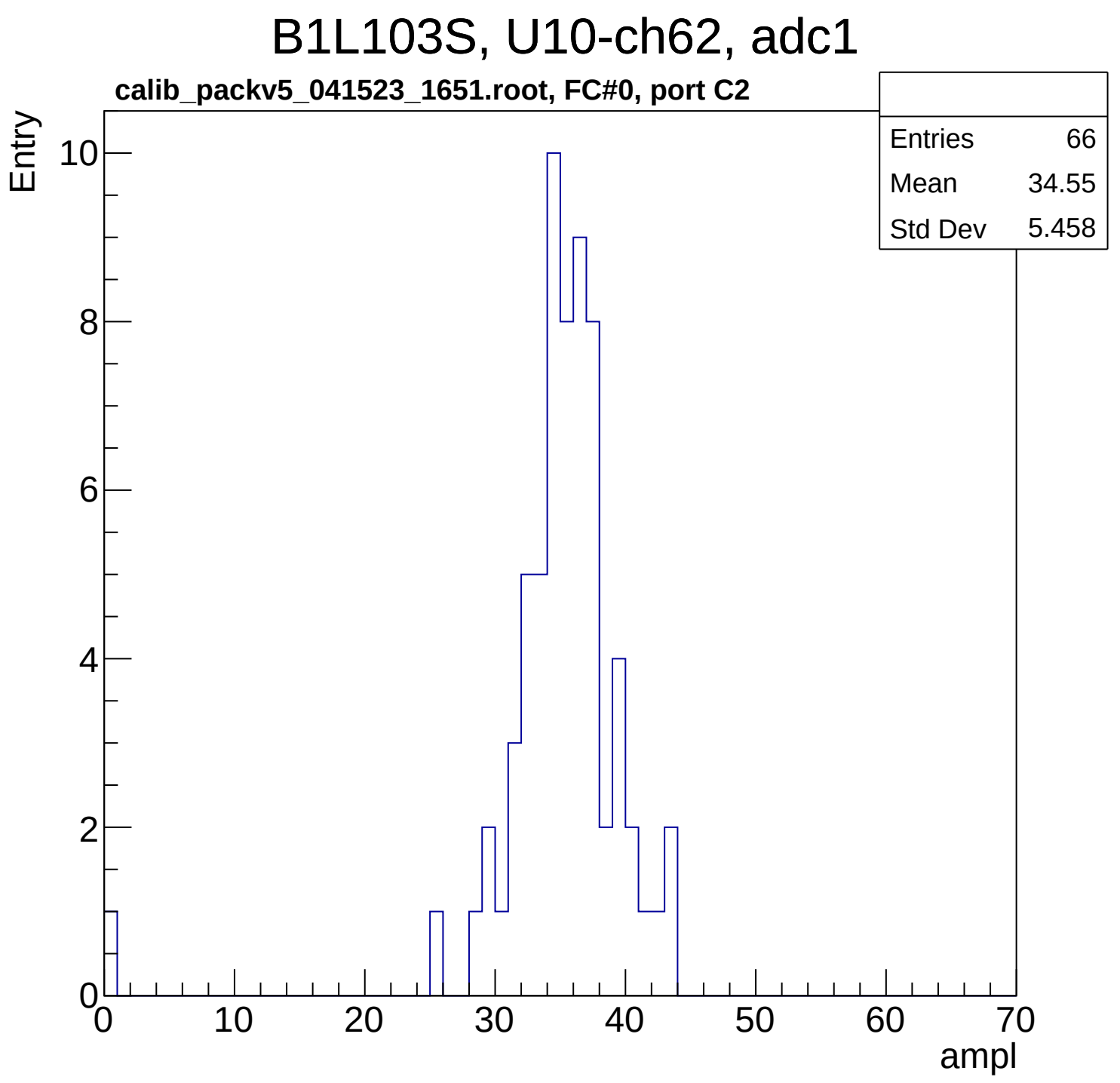
40
50
60
70


B1L103S, U10-ch62, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 34.55
Std Dev 5.458
Entry
ampl
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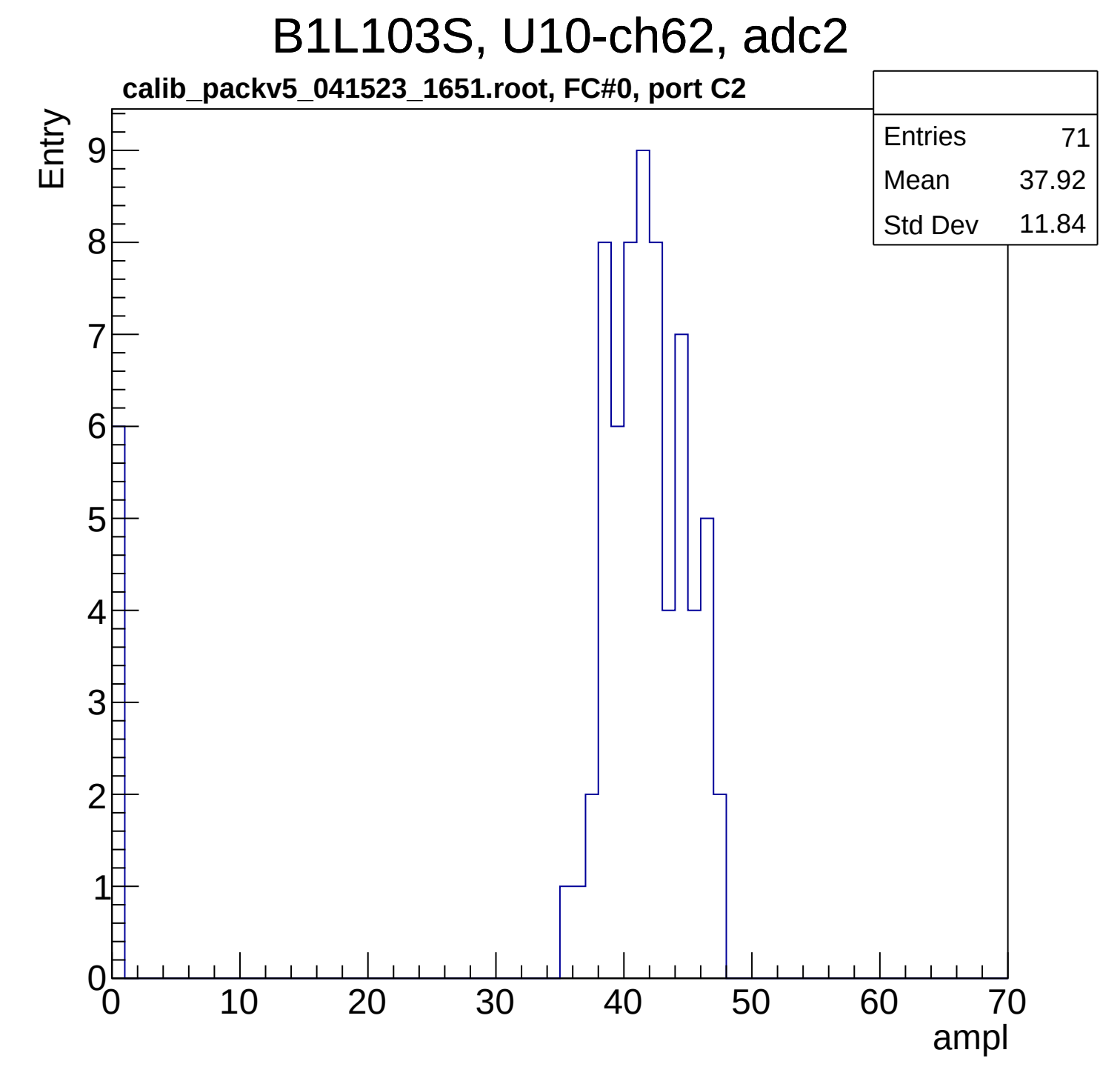
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U10-ch62, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 37.92
Std Dev 11.84
Entry
ampl
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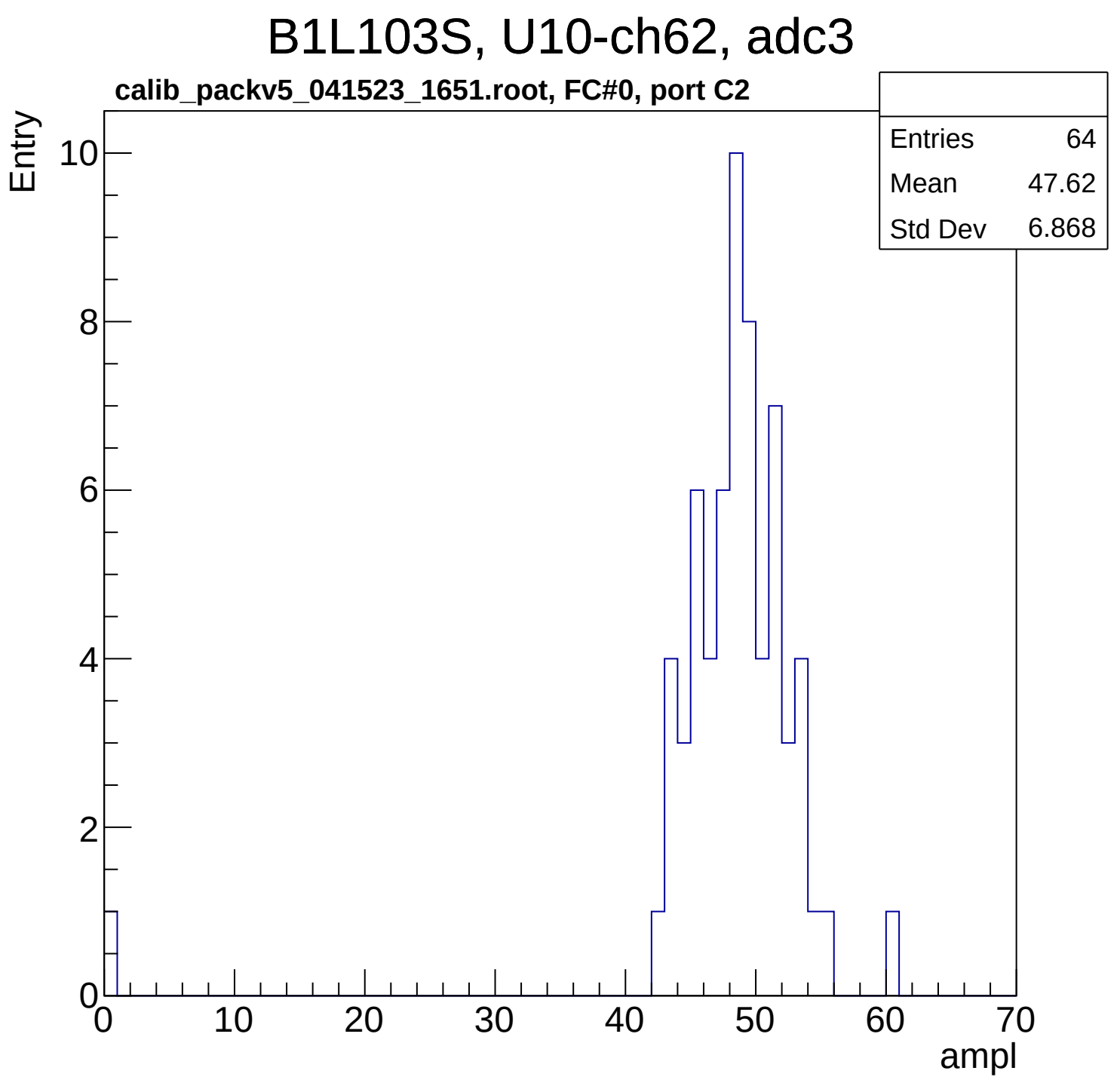
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U10-ch62, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 47.62
Std Dev 6.868
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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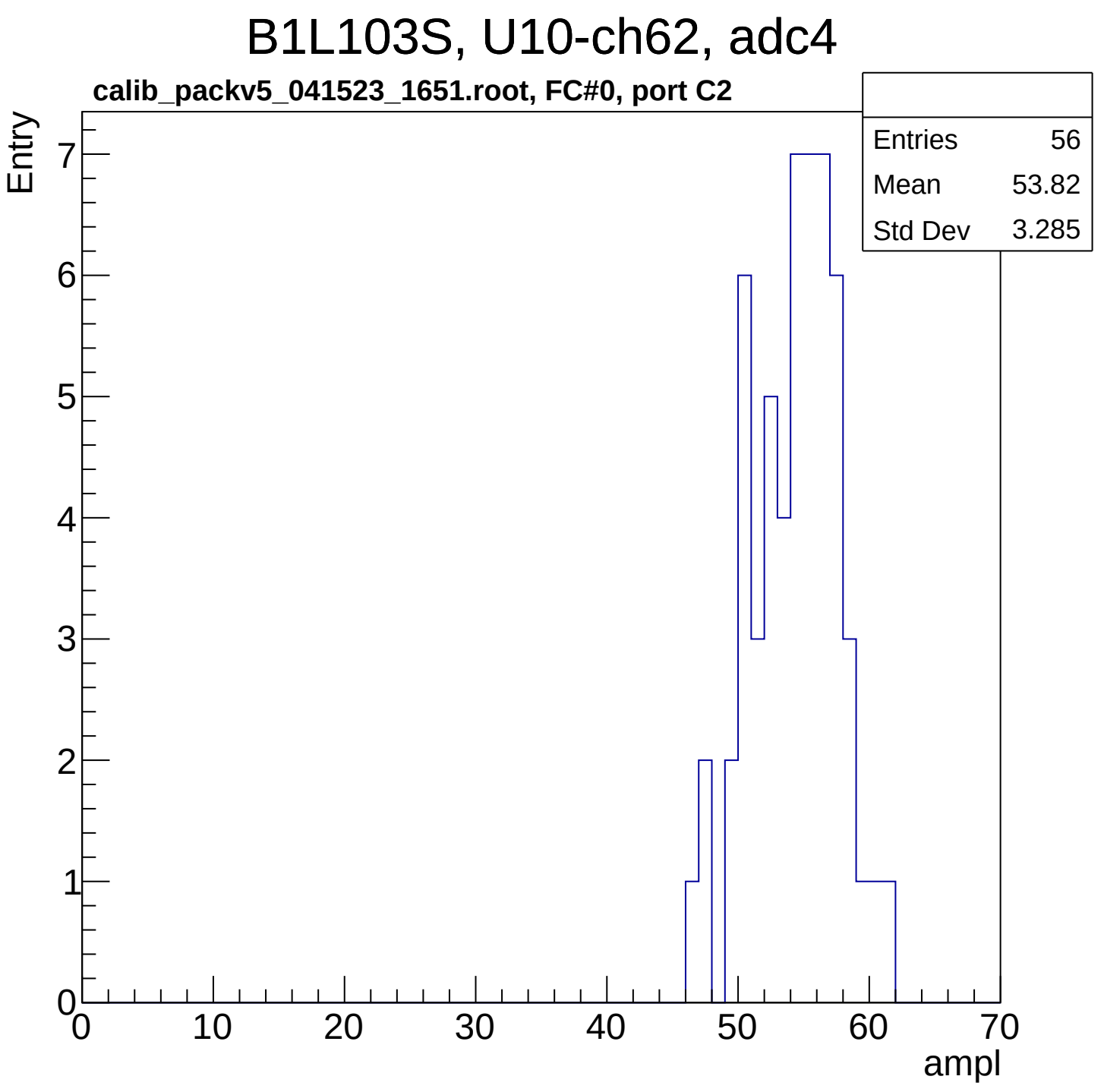
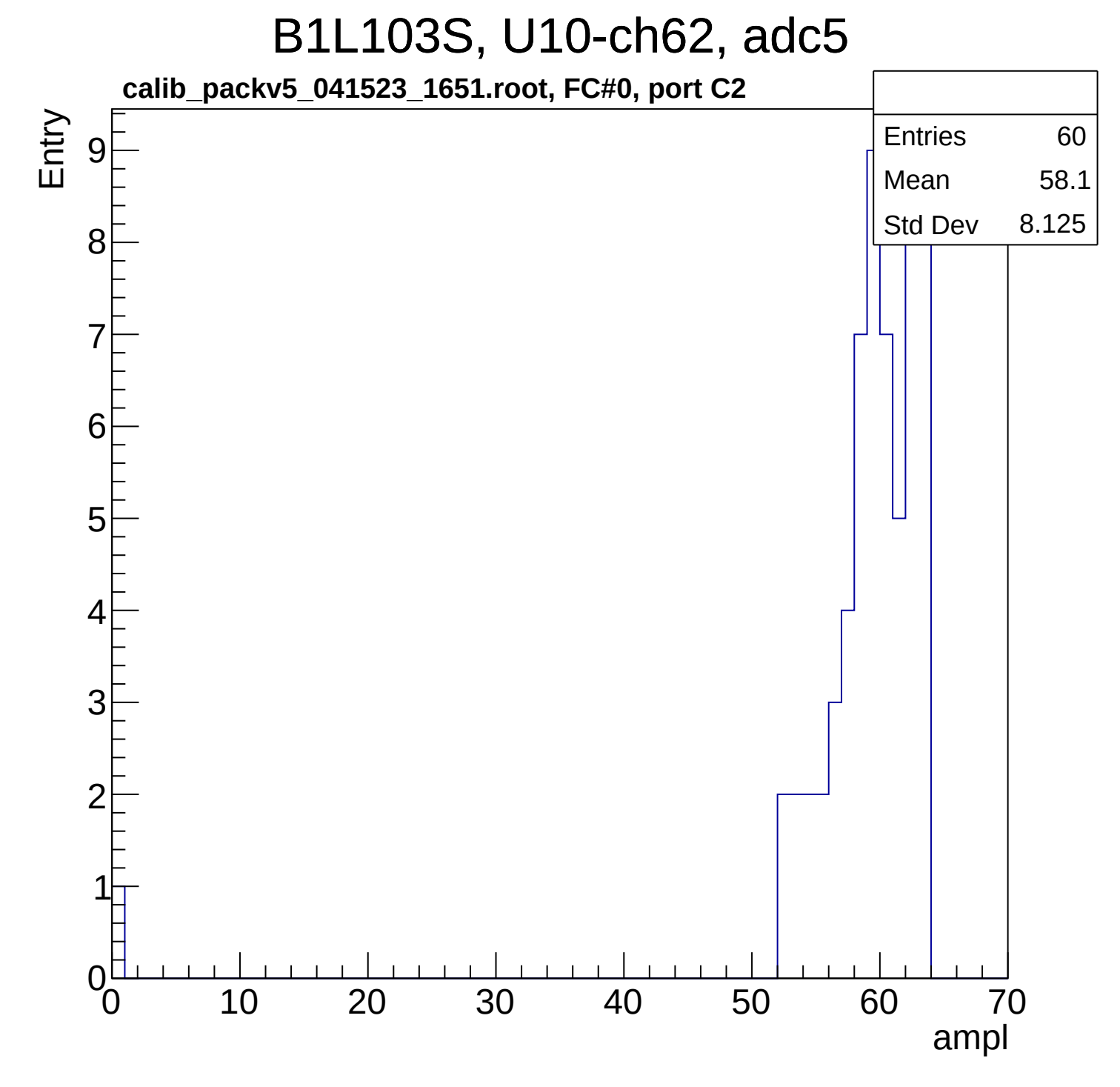
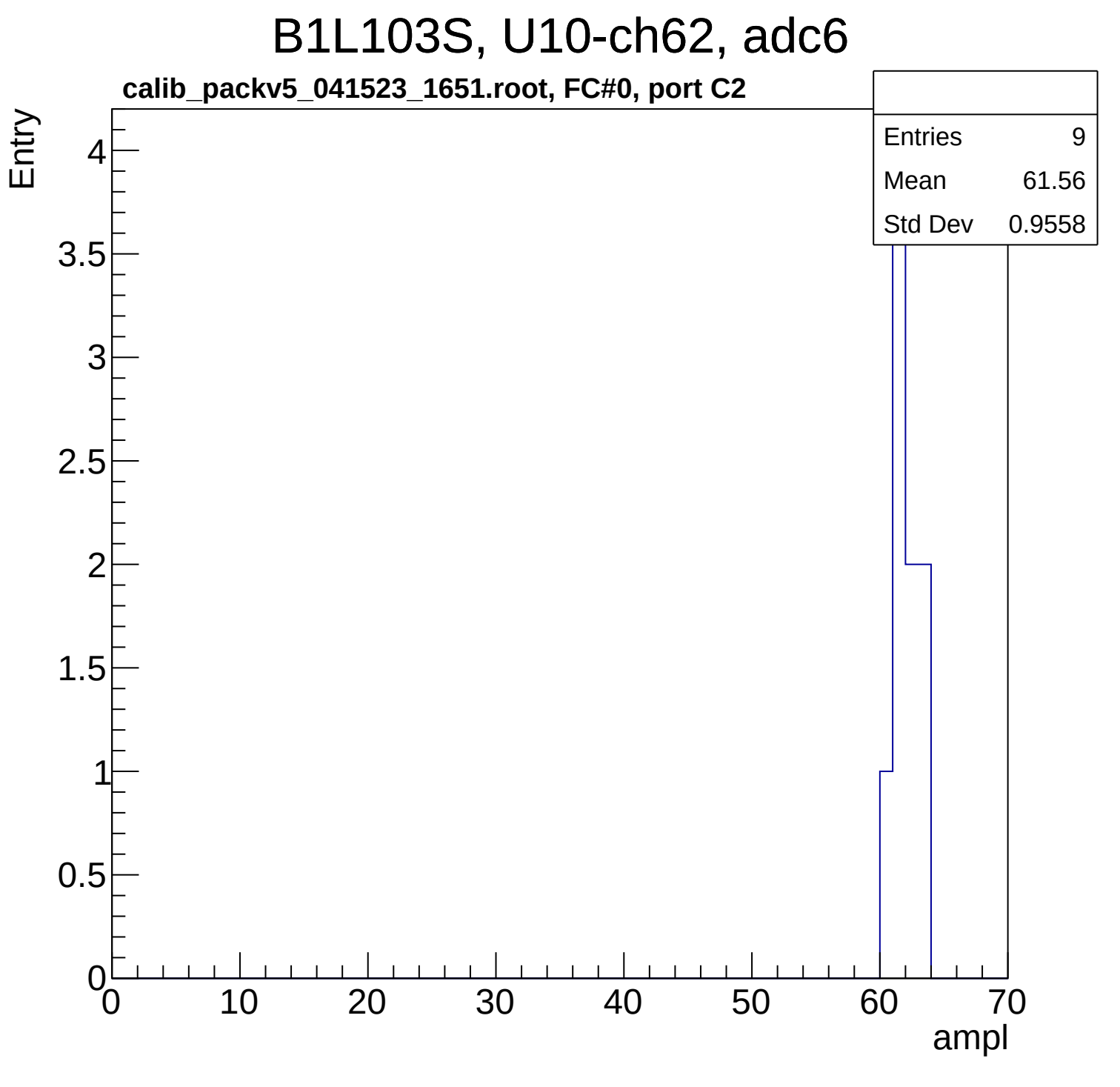
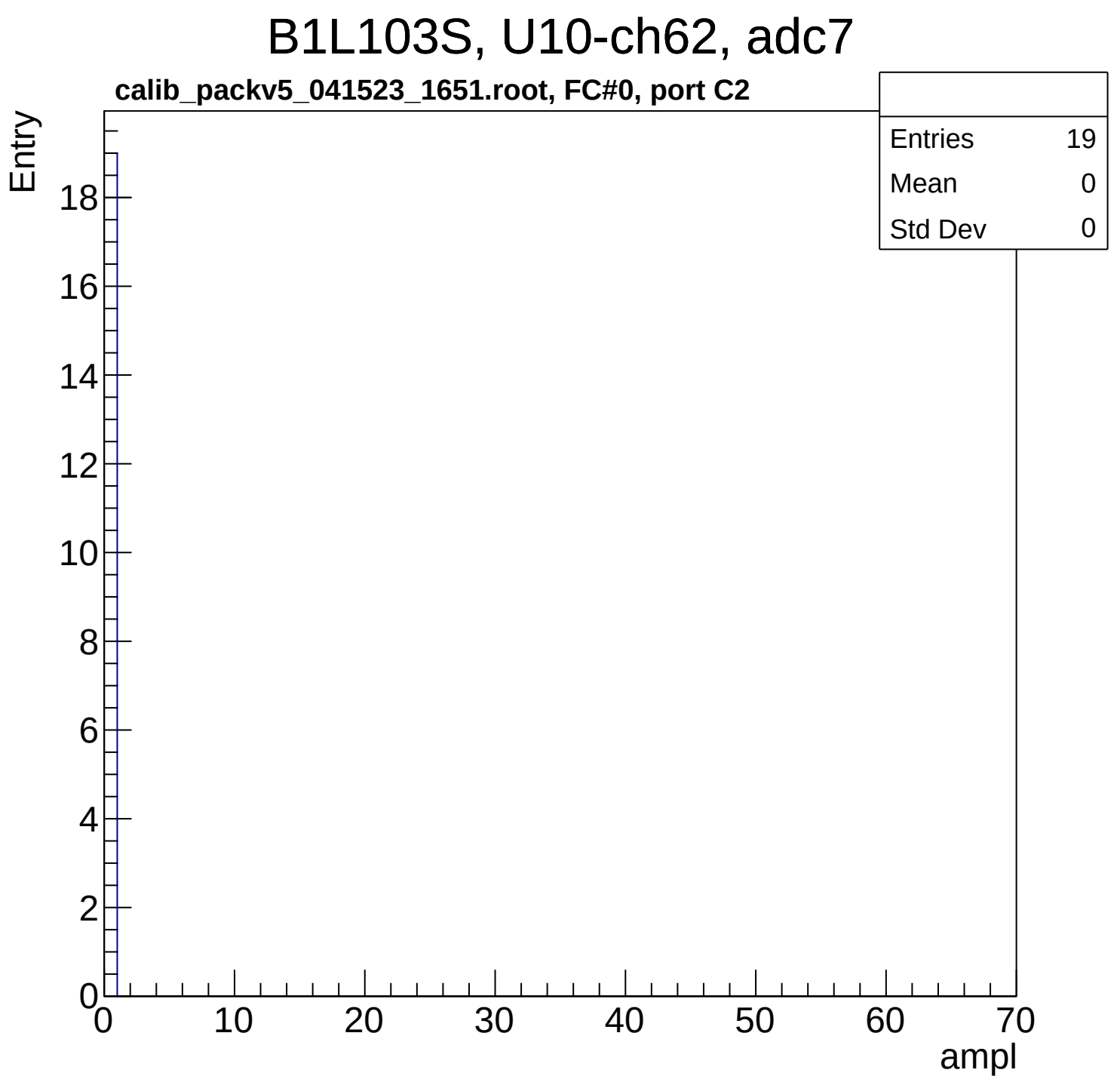
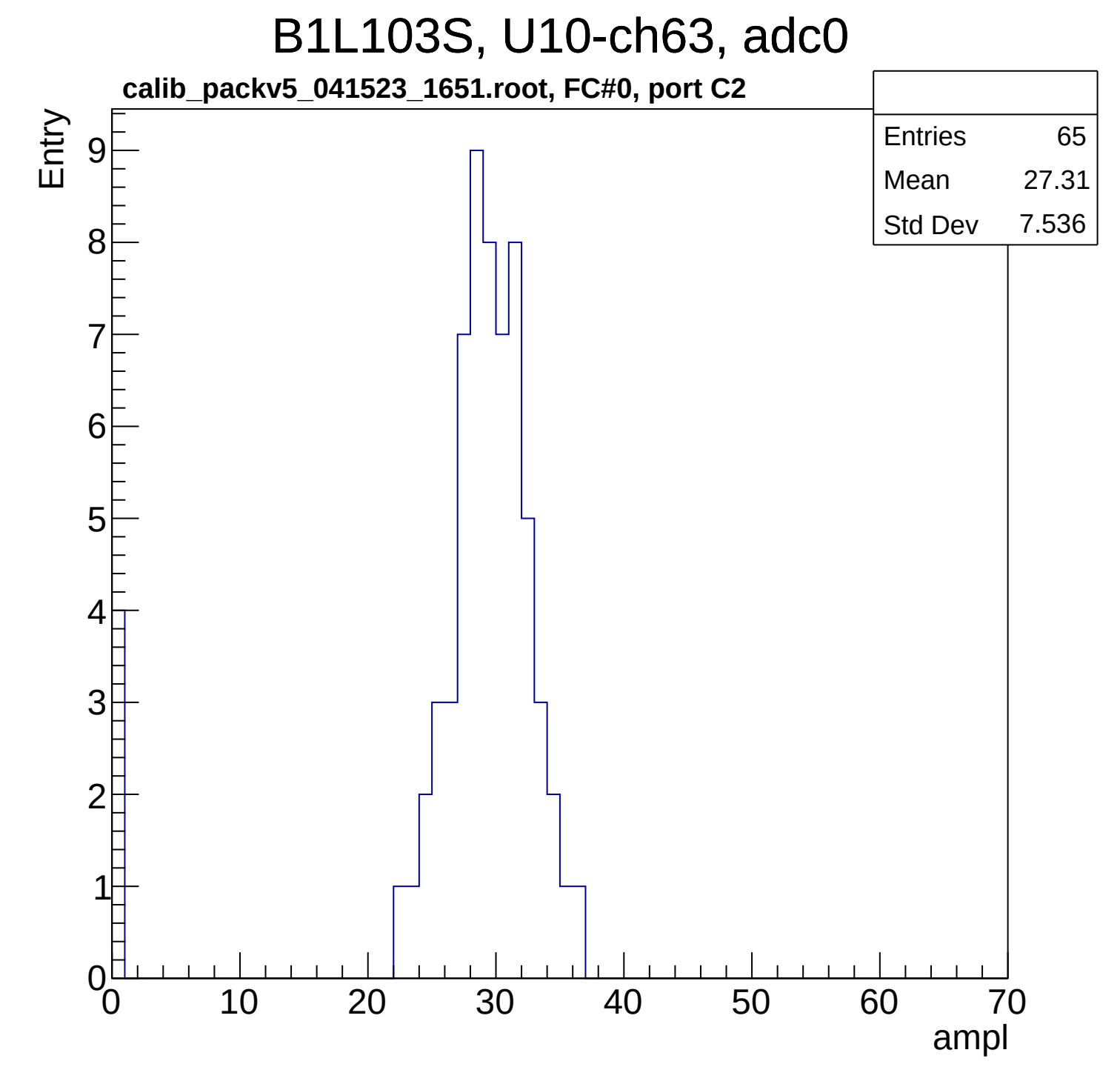
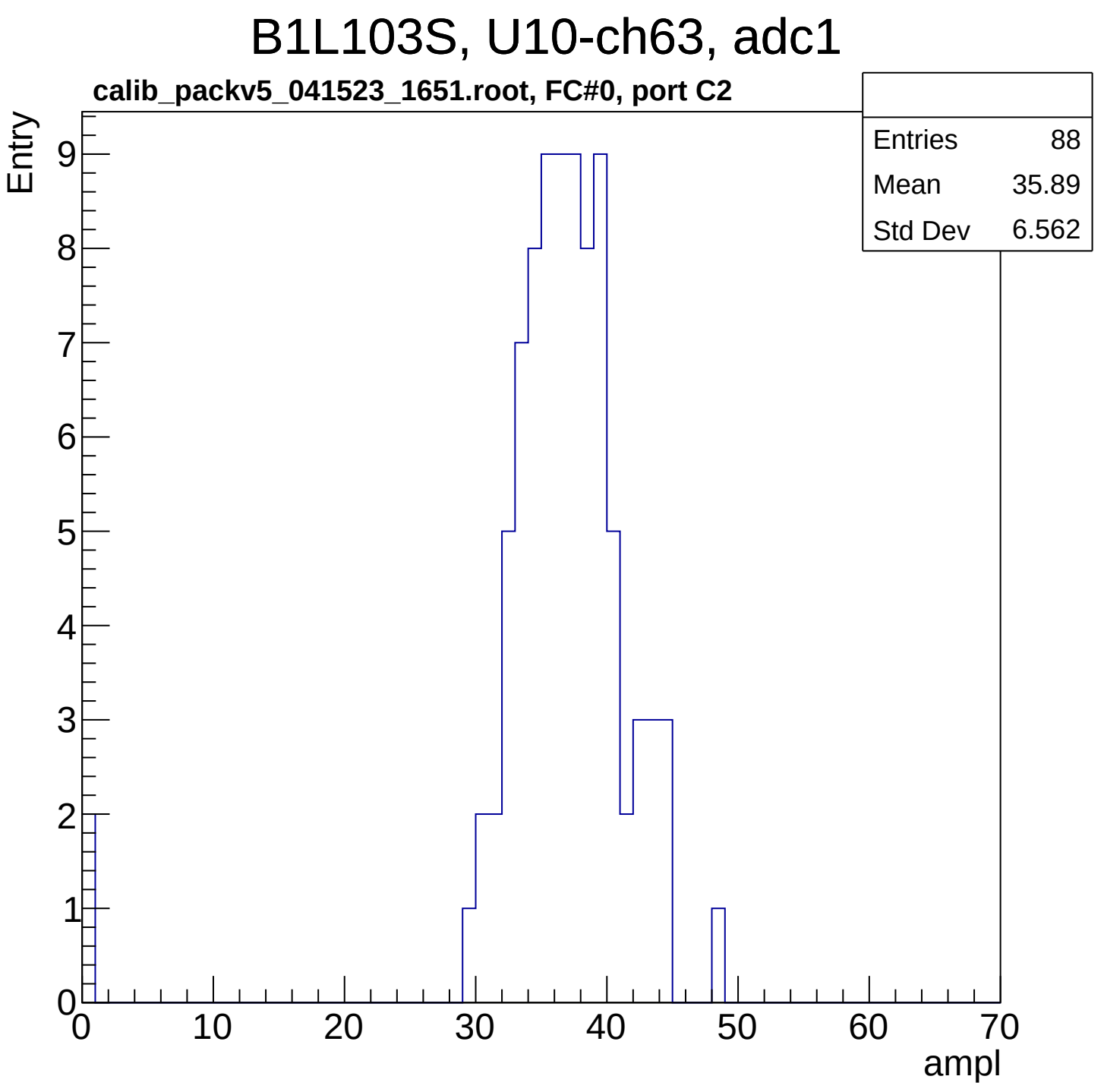

B1L103S, U10-ch62, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 53.82
Std Dev 3.285
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

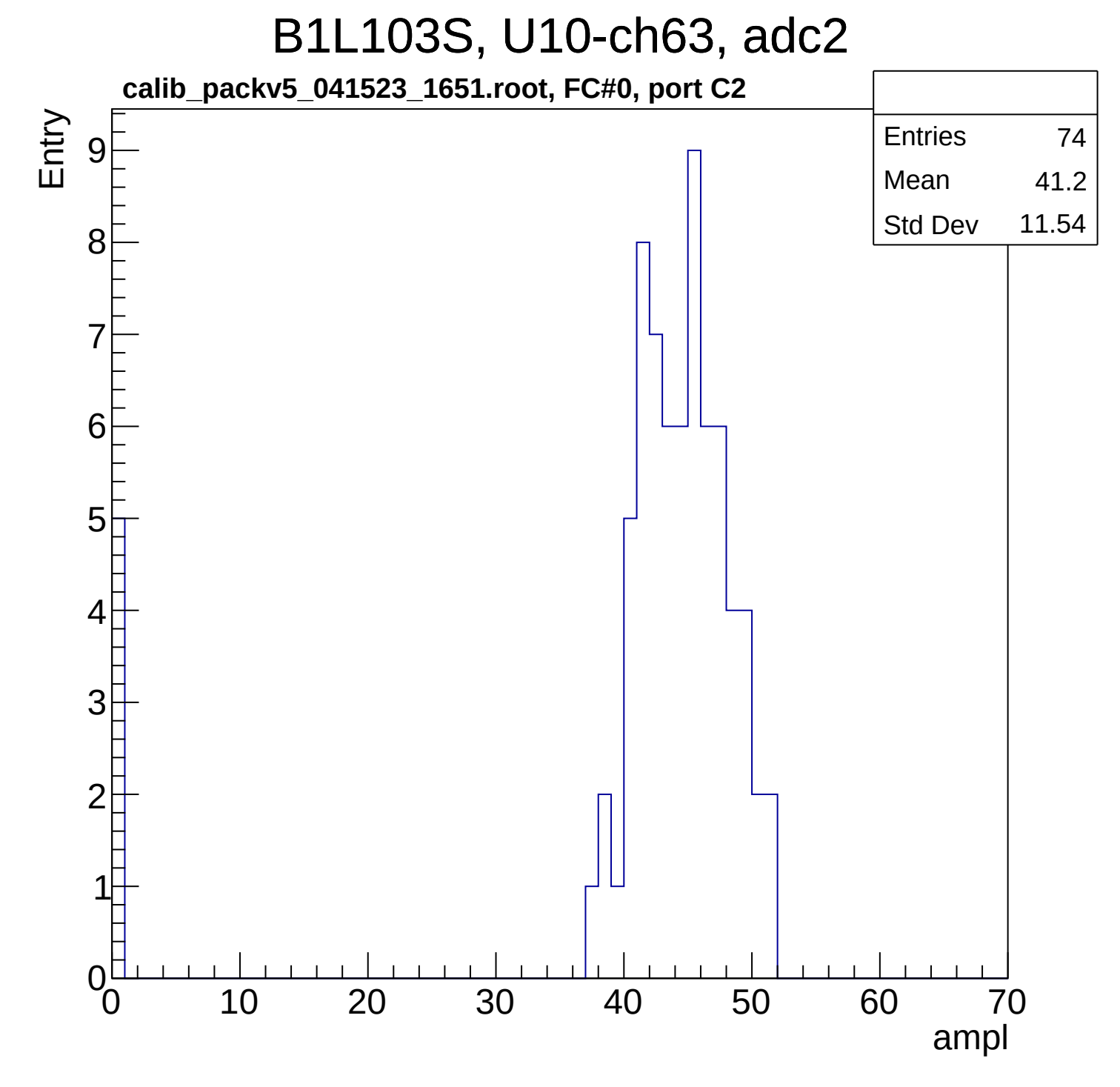

B1L103S, U10-ch62, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 58.1
Std Dev 8.125
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

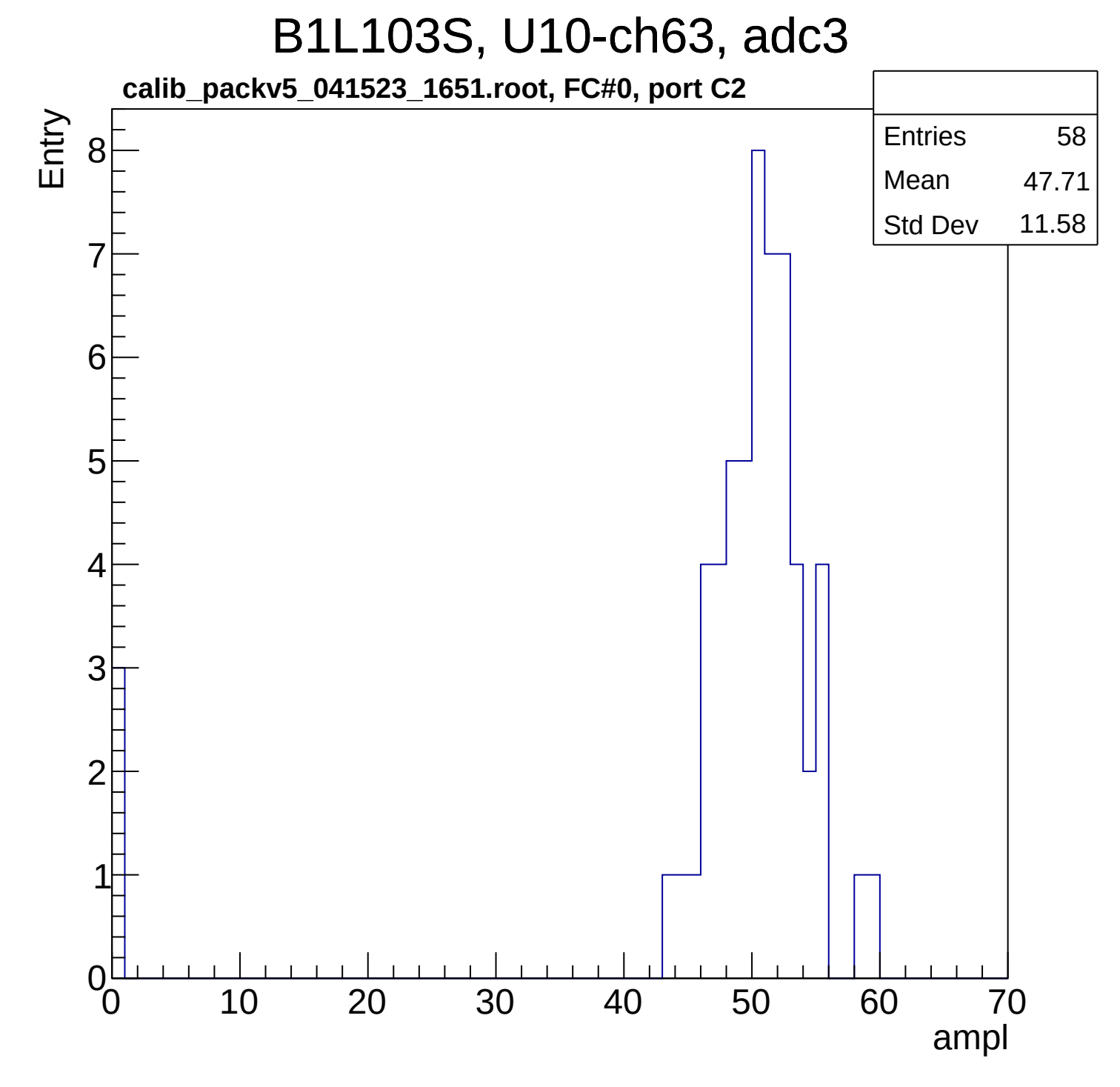

B1L103S, U10-ch62, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 9
Mean 61.56
Std Dev 0.9558
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U10-ch62, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch63, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 27.31
Std Dev 7.536
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U10-ch63, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 88
Mean 35.89
Std Dev 6.562
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U10-ch63, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 41.2
Std Dev 11.54
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U10-ch63, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 47.71
Std Dev 11.58
Entry
ampl
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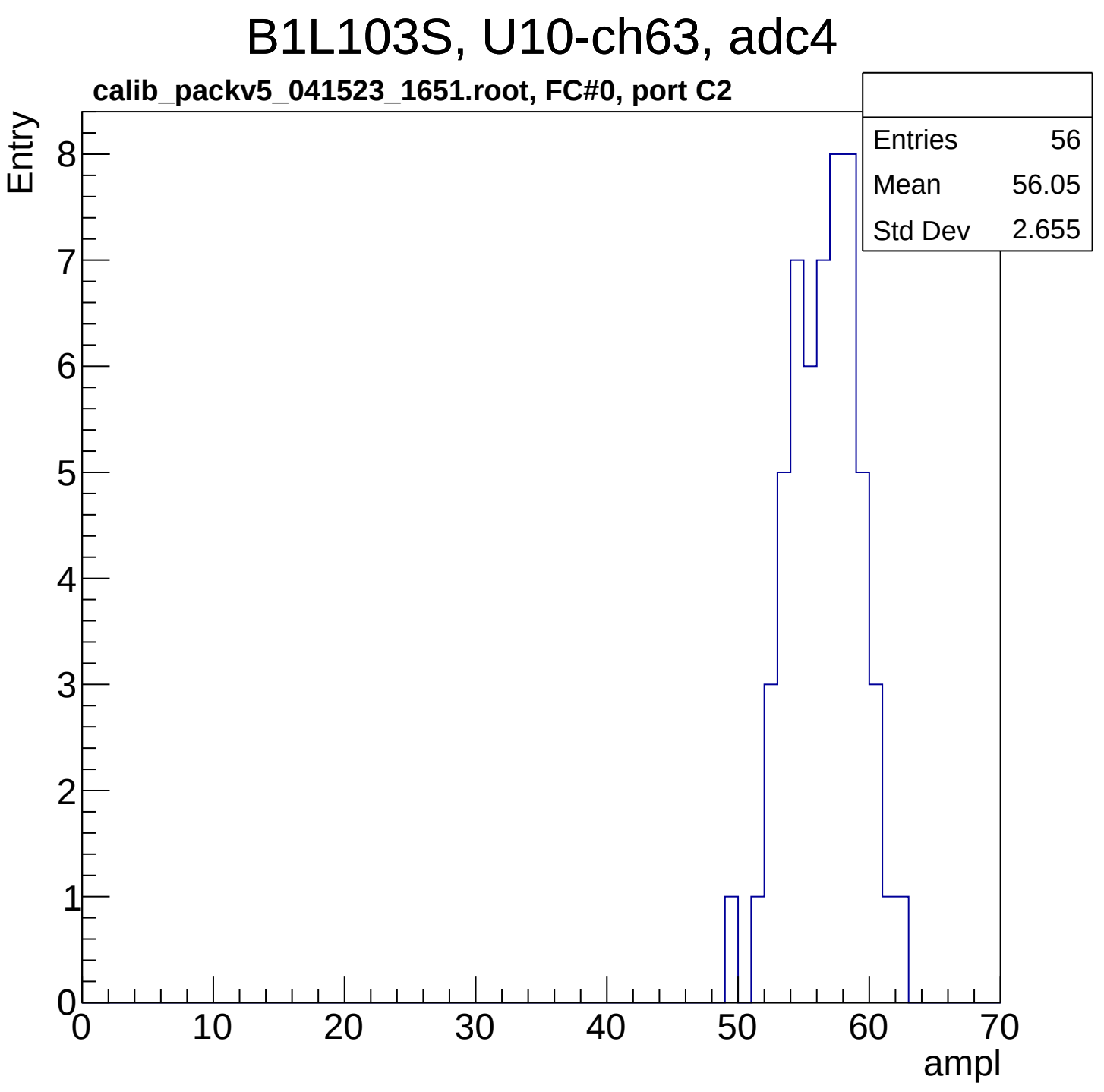
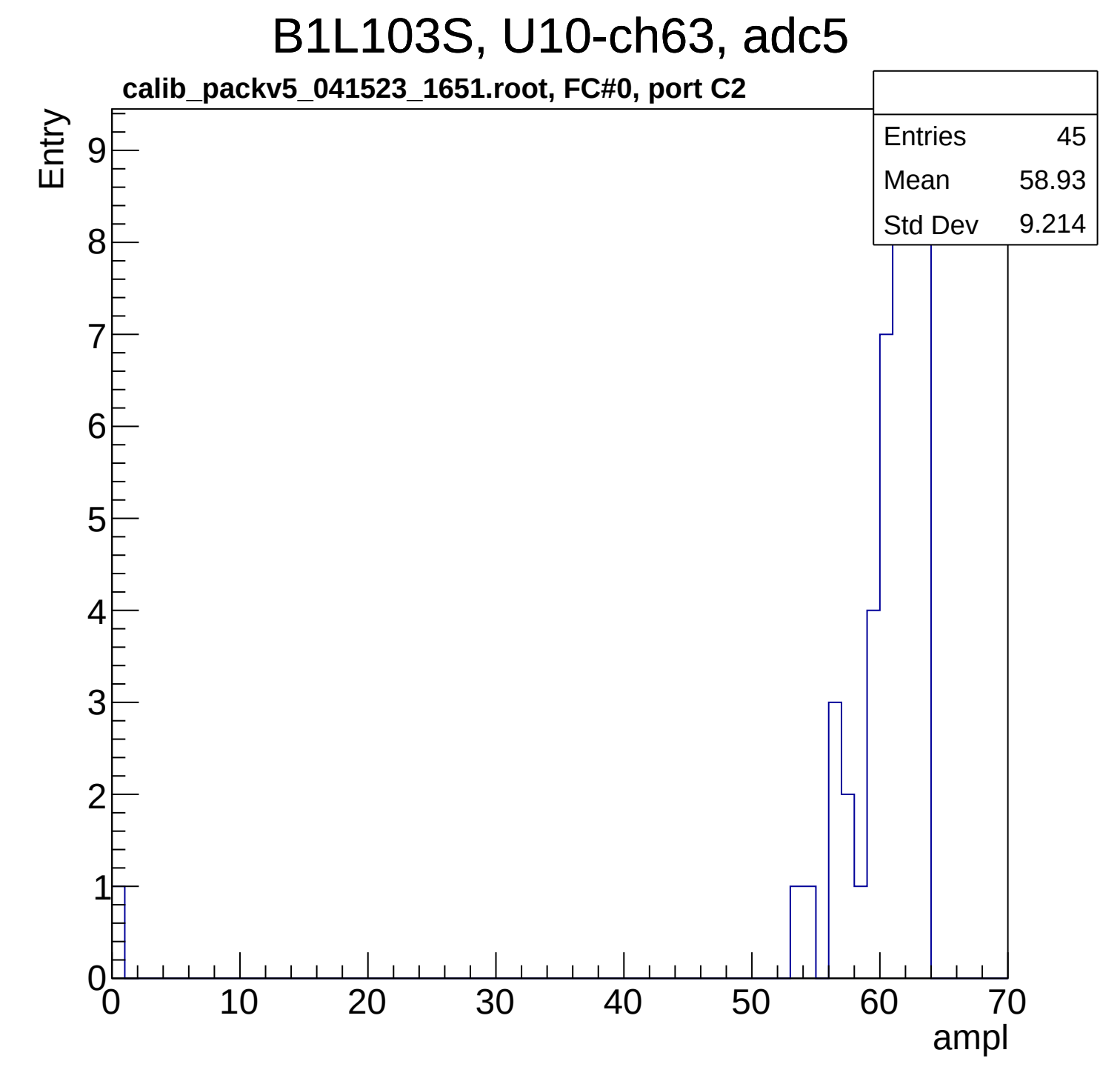
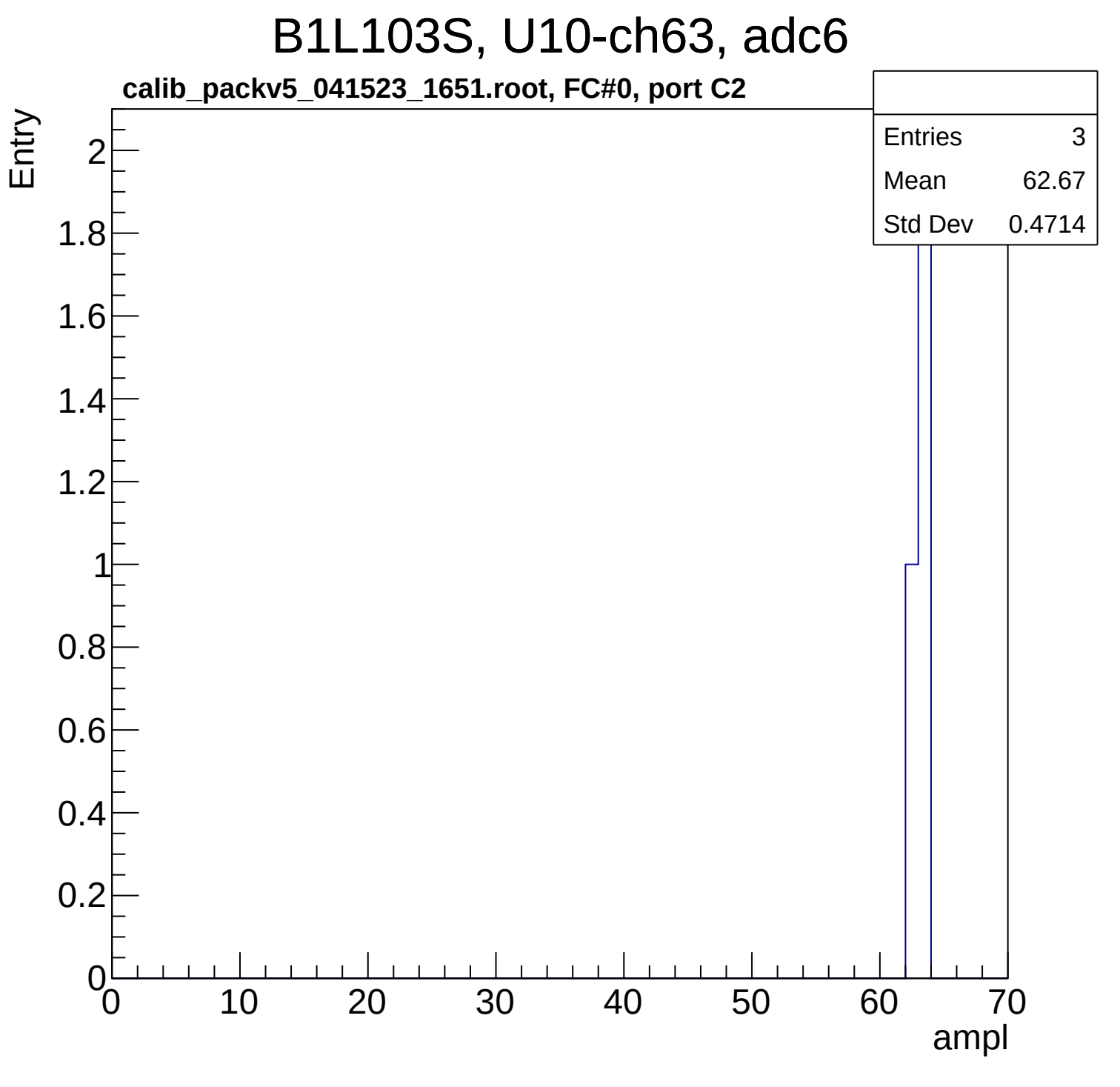
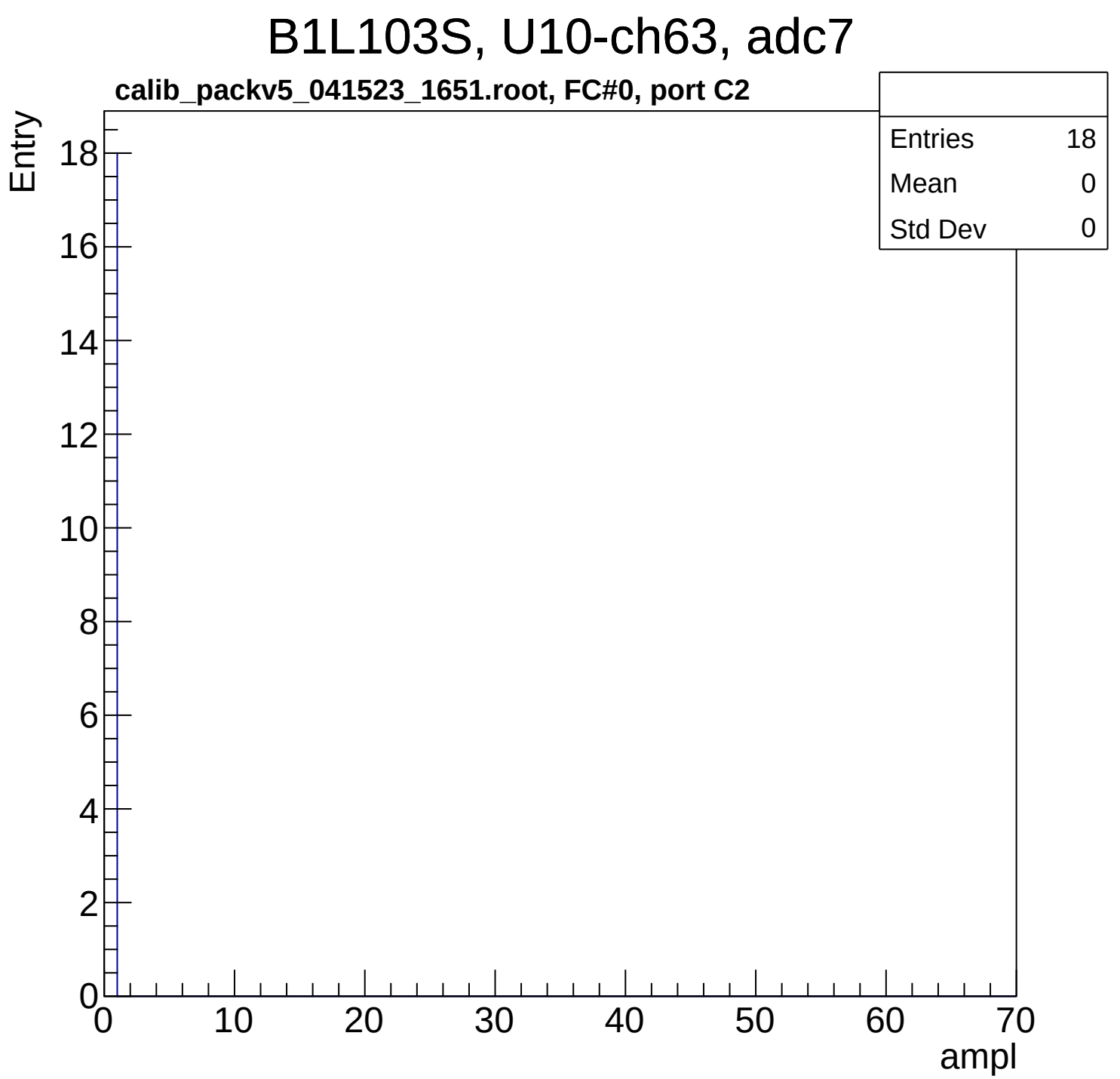
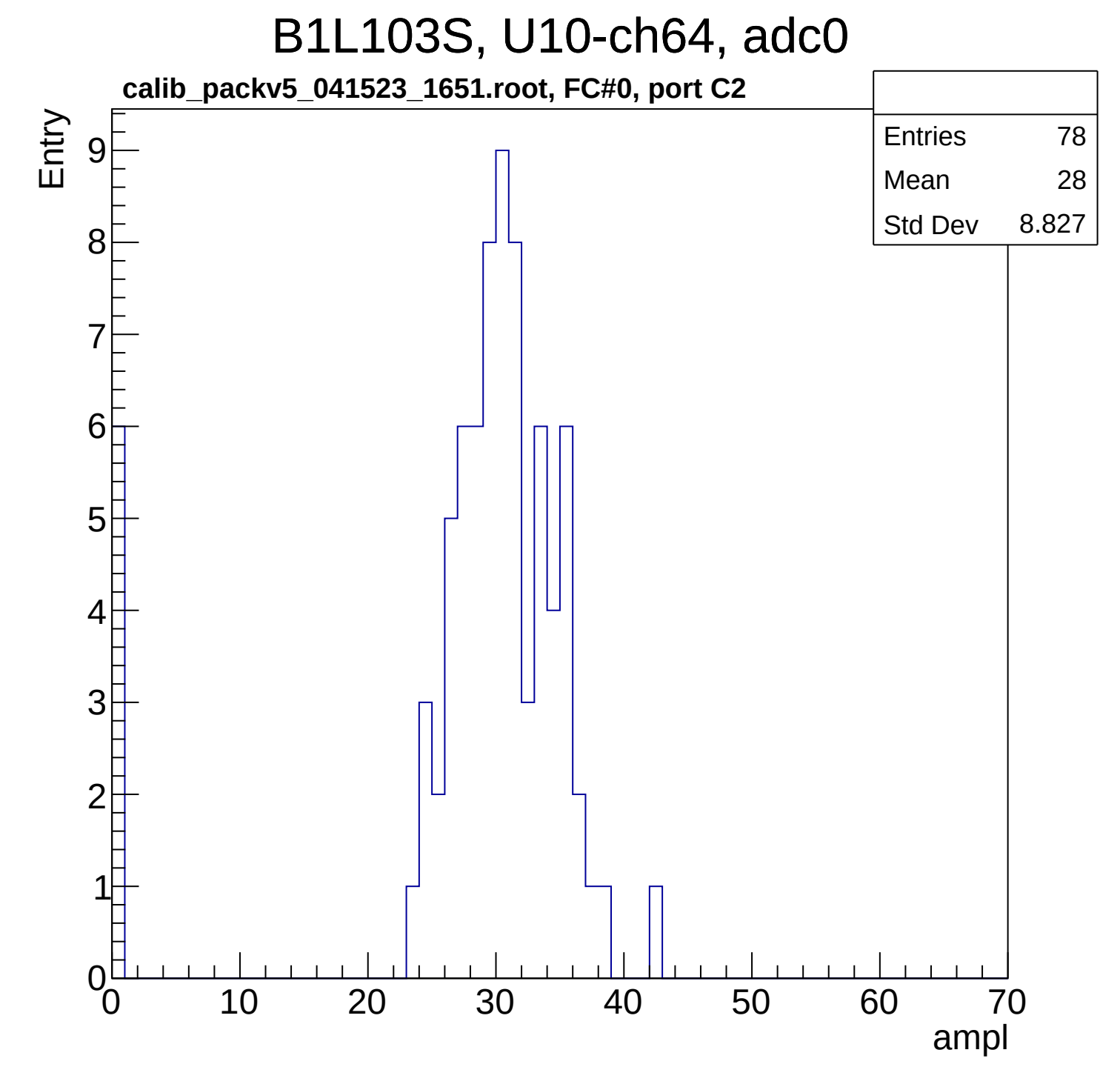
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

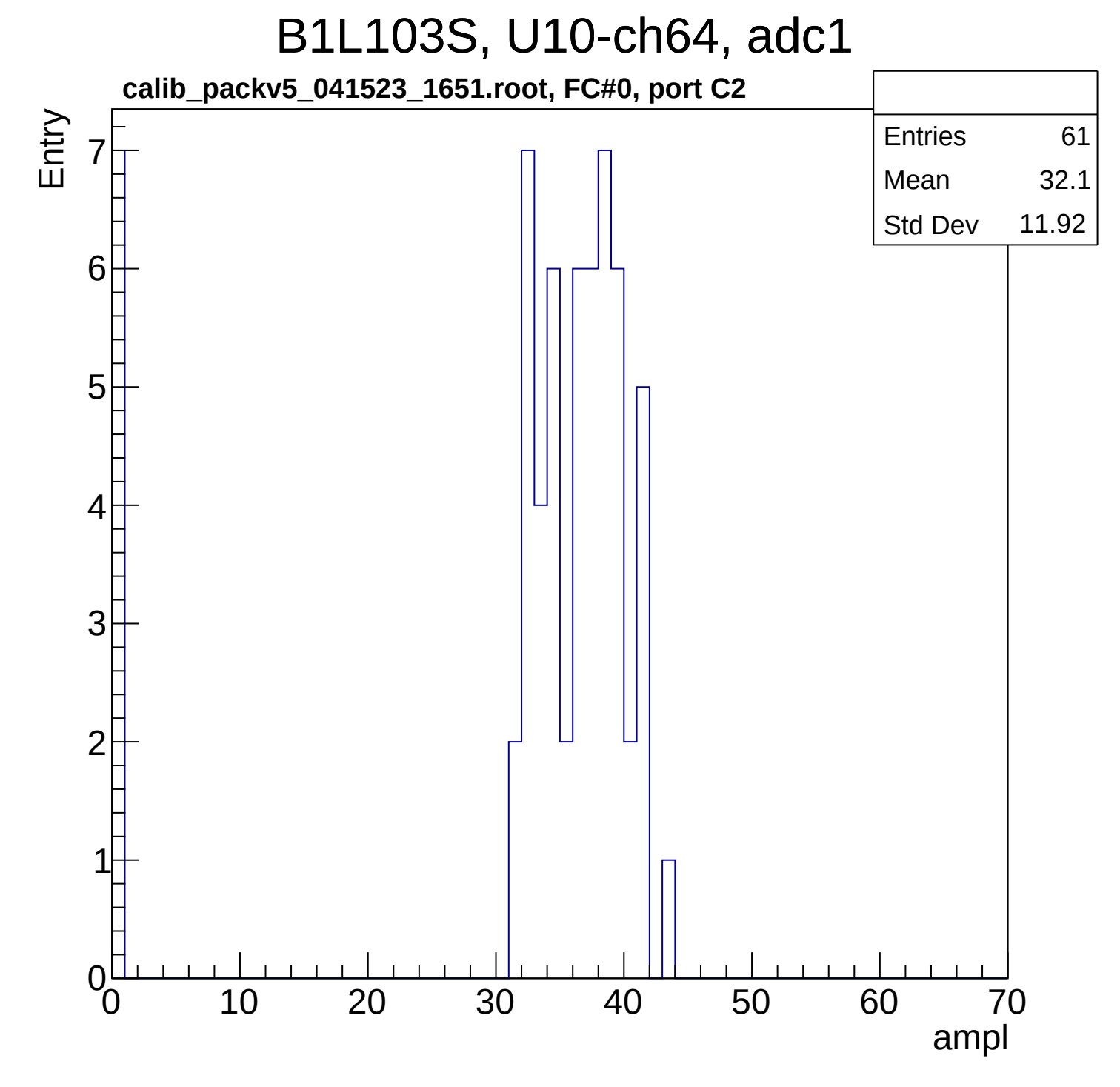

B1L103S, U10-ch63, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 56.05
Std Dev 2.655
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

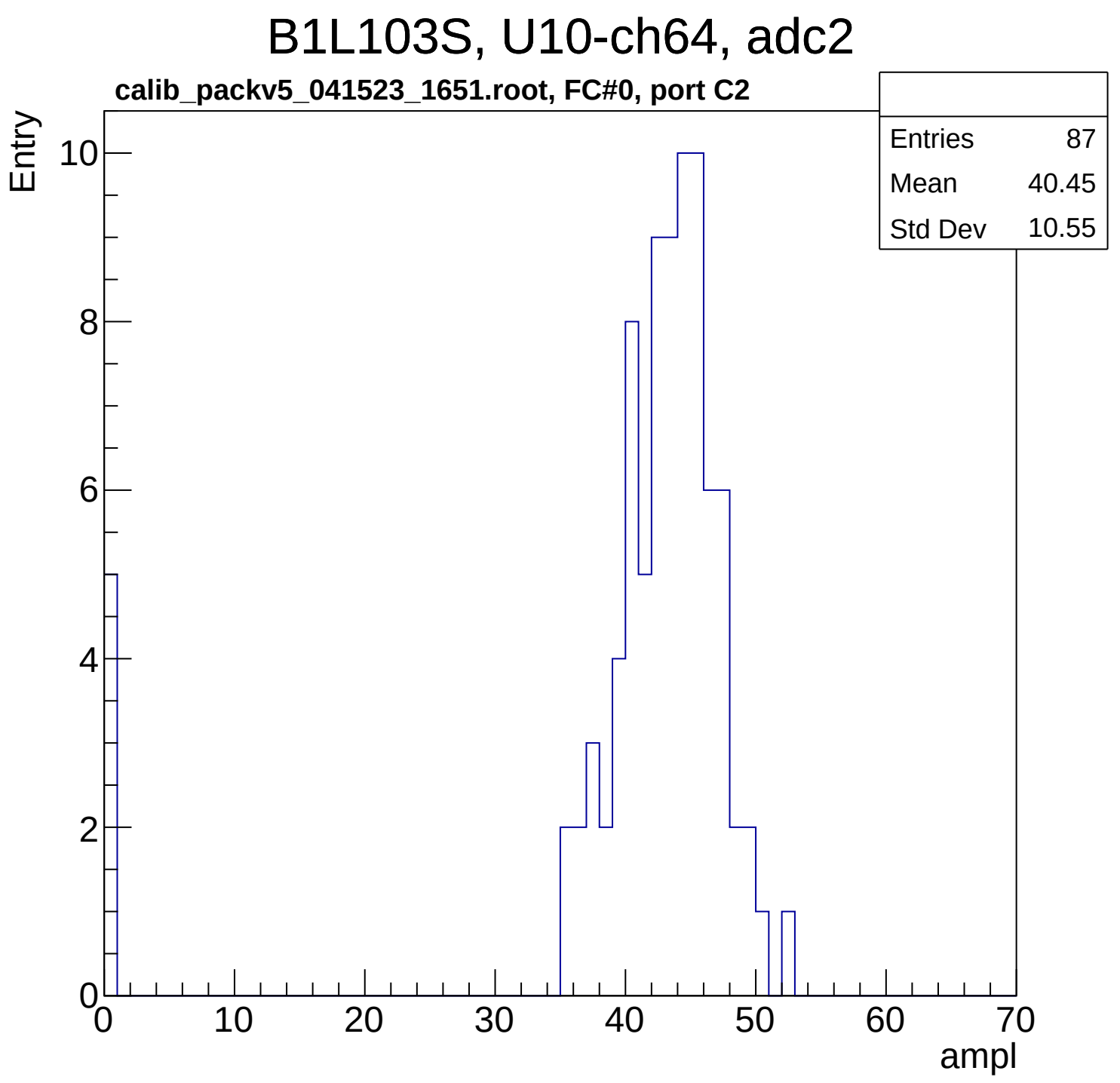

B1L103S, U10-ch63, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 58.93
Std Dev 9.214
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

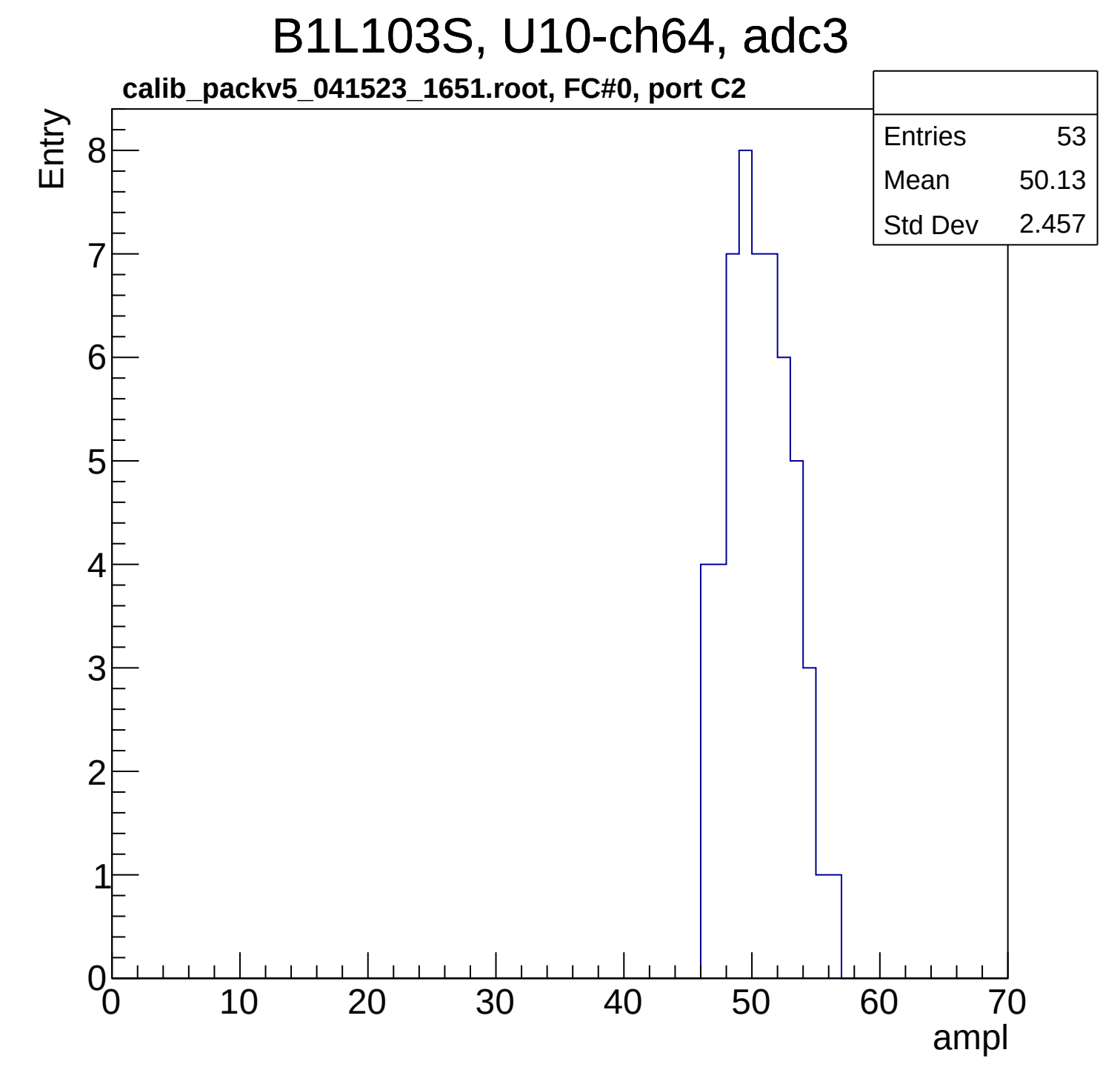

B1L103S, U10-ch63, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 3
Mean 62.67
Std Dev 0.4714
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U10-ch63, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch64, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 28
Std Dev 8.827
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U10-ch64, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 32.1
Std Dev 11.92
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U10-ch64, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 87
Mean 40.45
Std Dev 10.55
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U10-ch64, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 50.13
Std Dev 2.457
Entry
ampl
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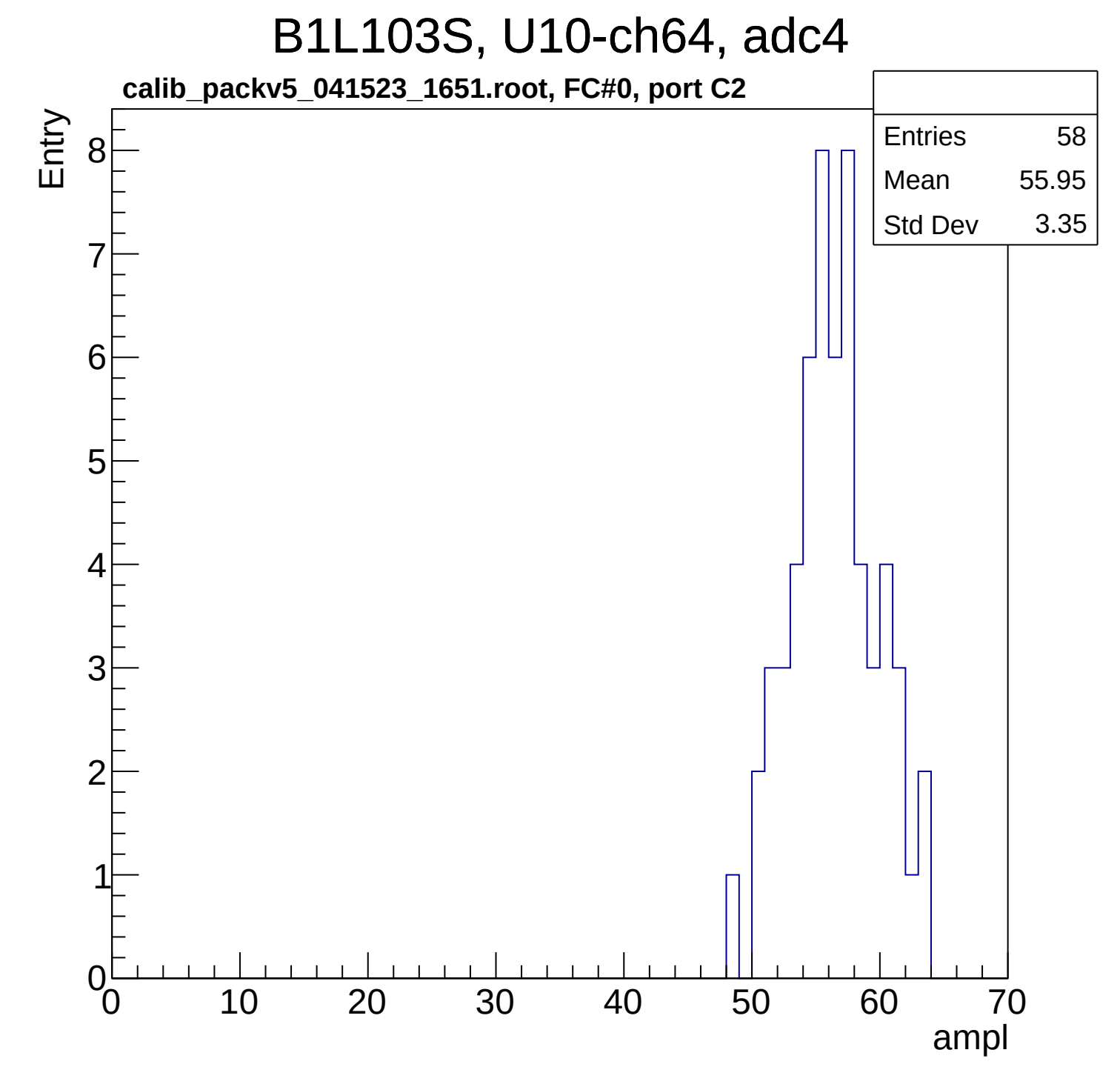
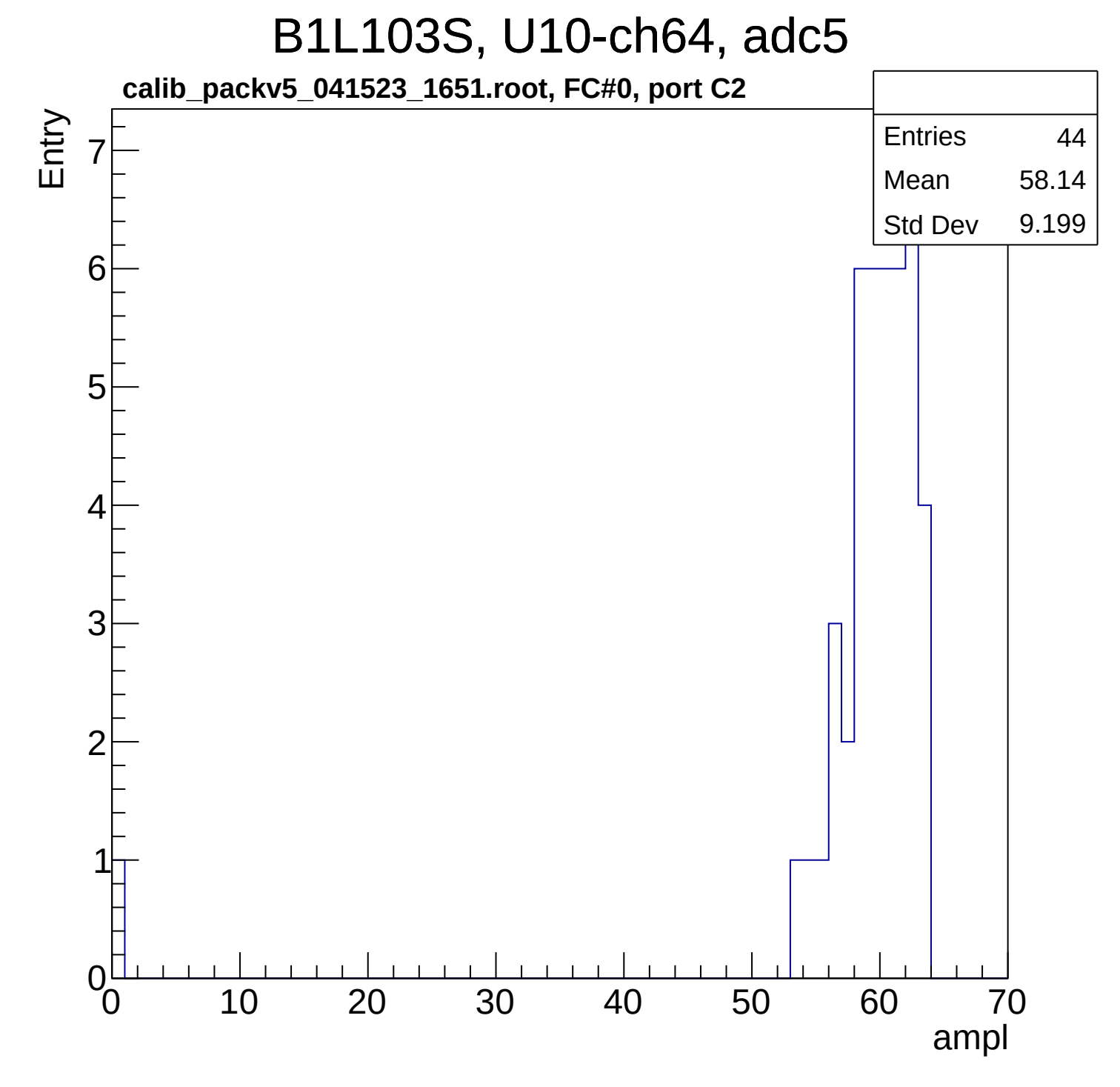
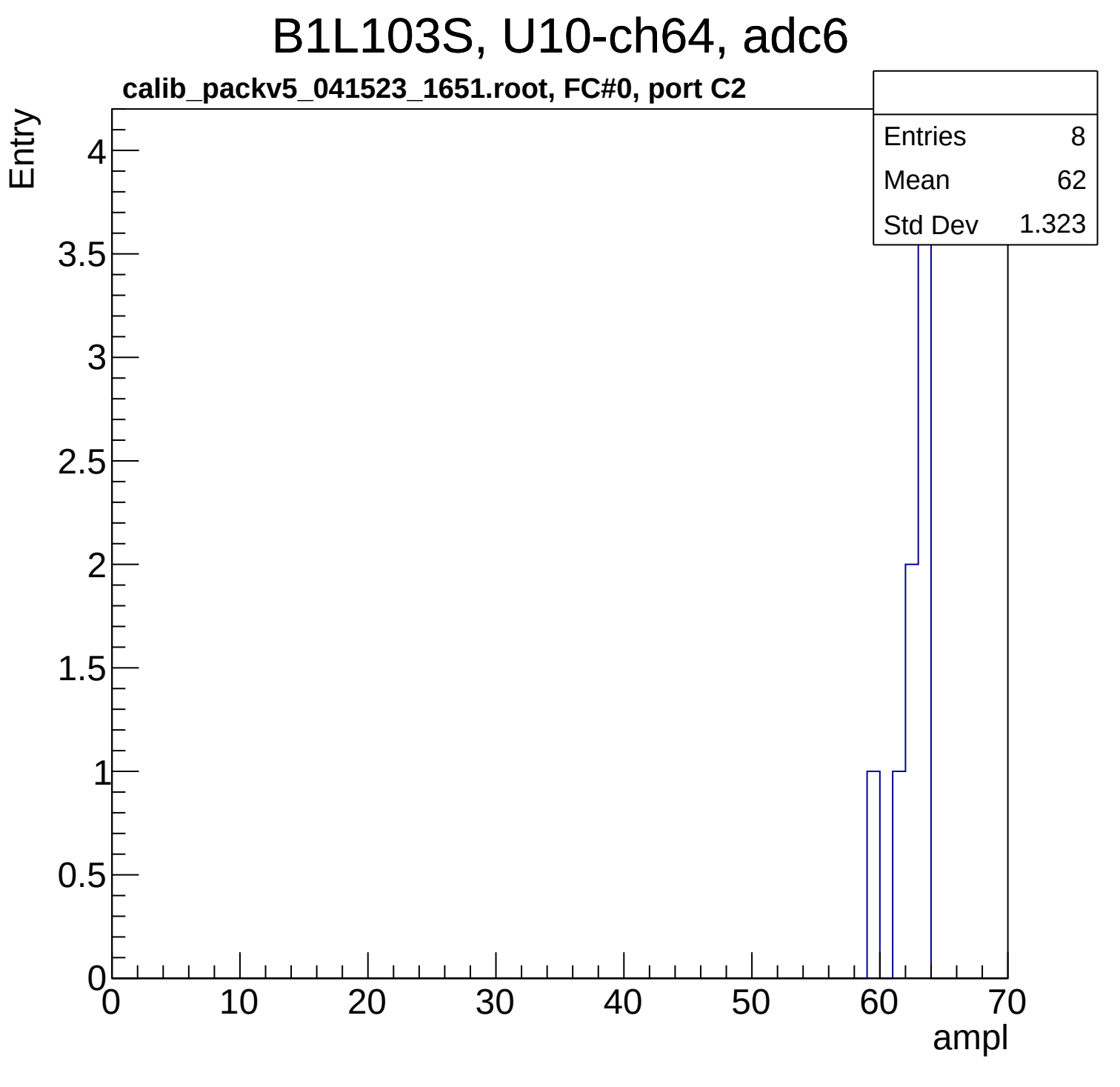
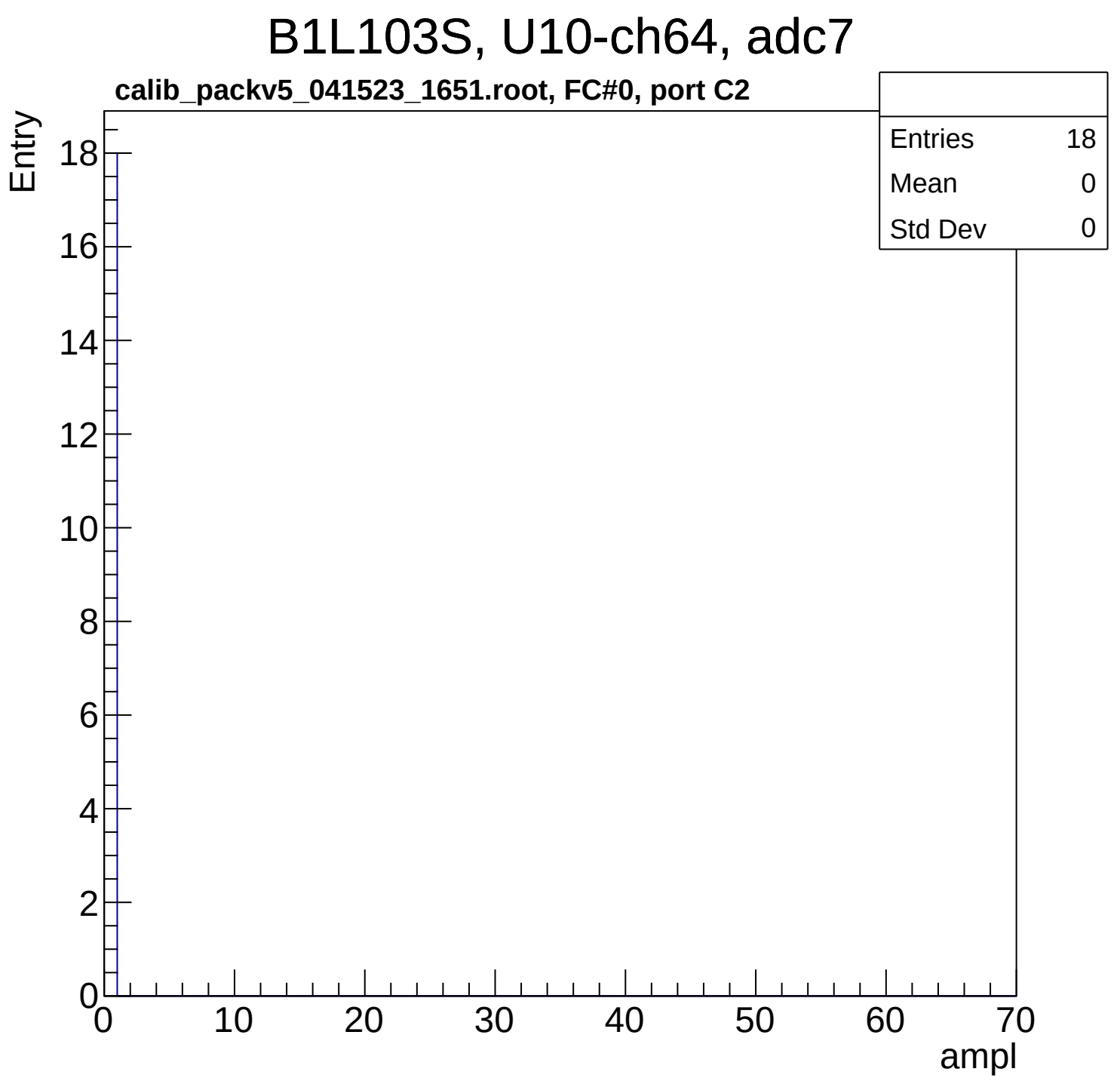
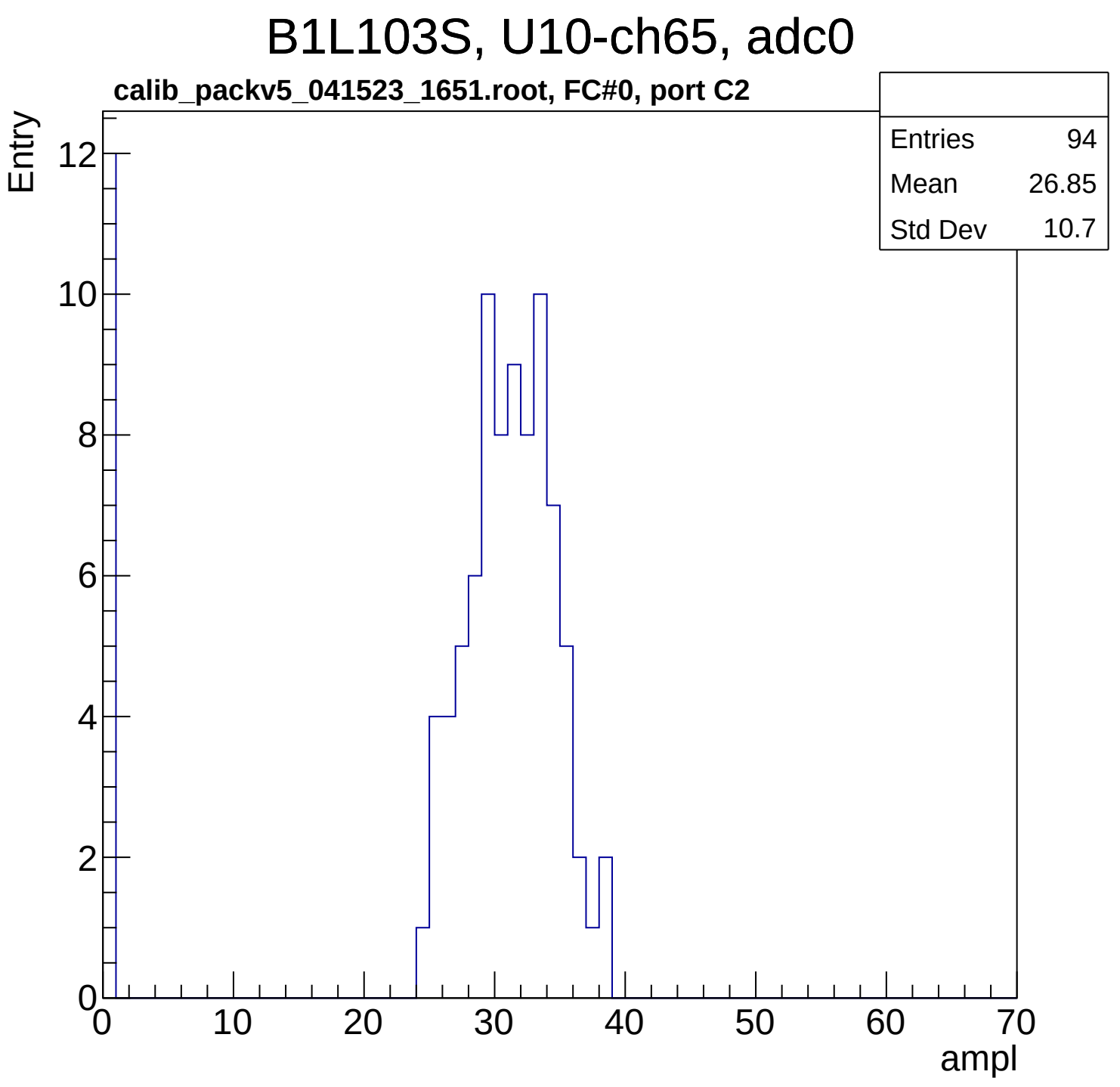
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

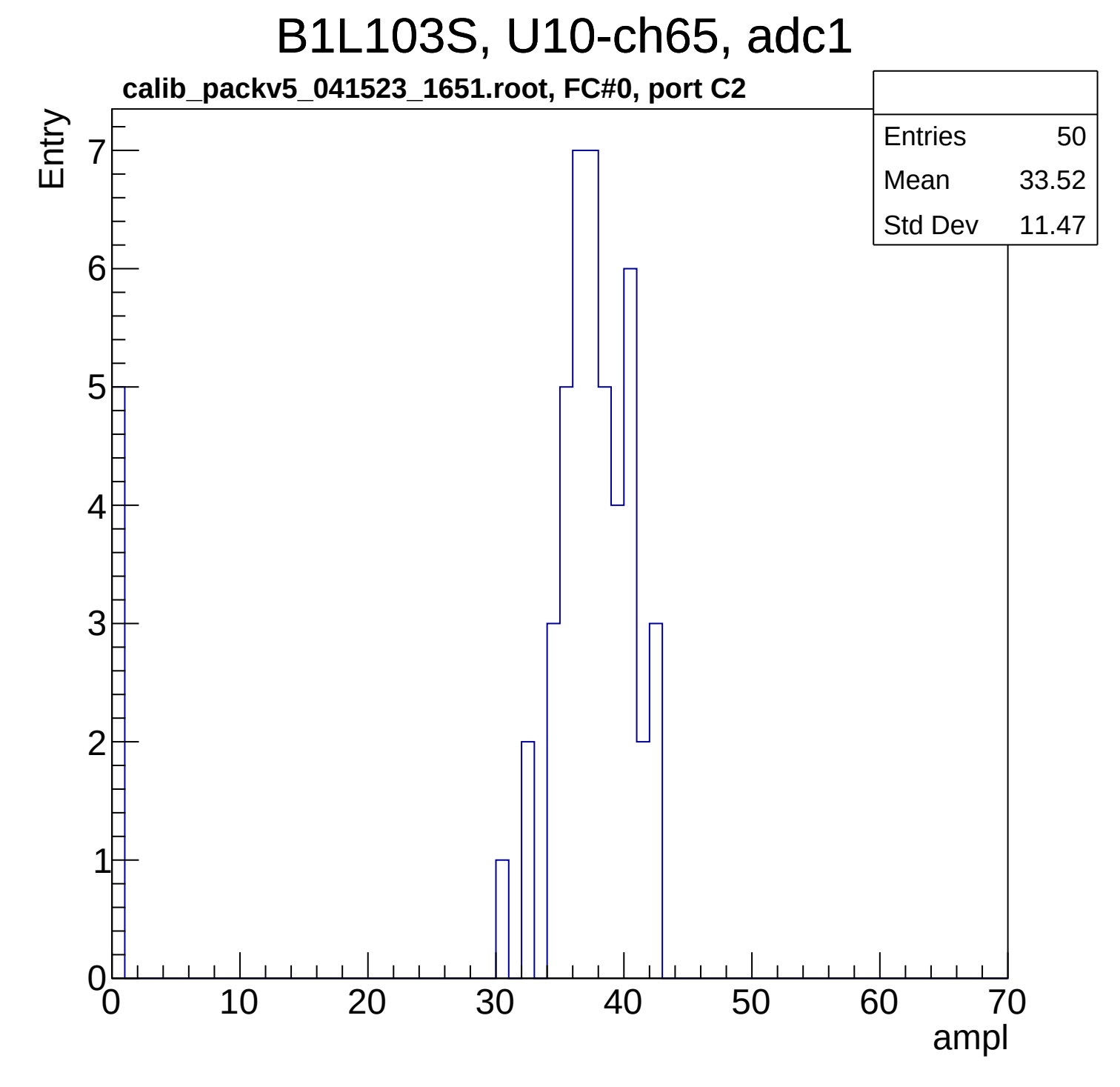

B1L103S, U10-ch64, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 55.95
Std Dev 3.35
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

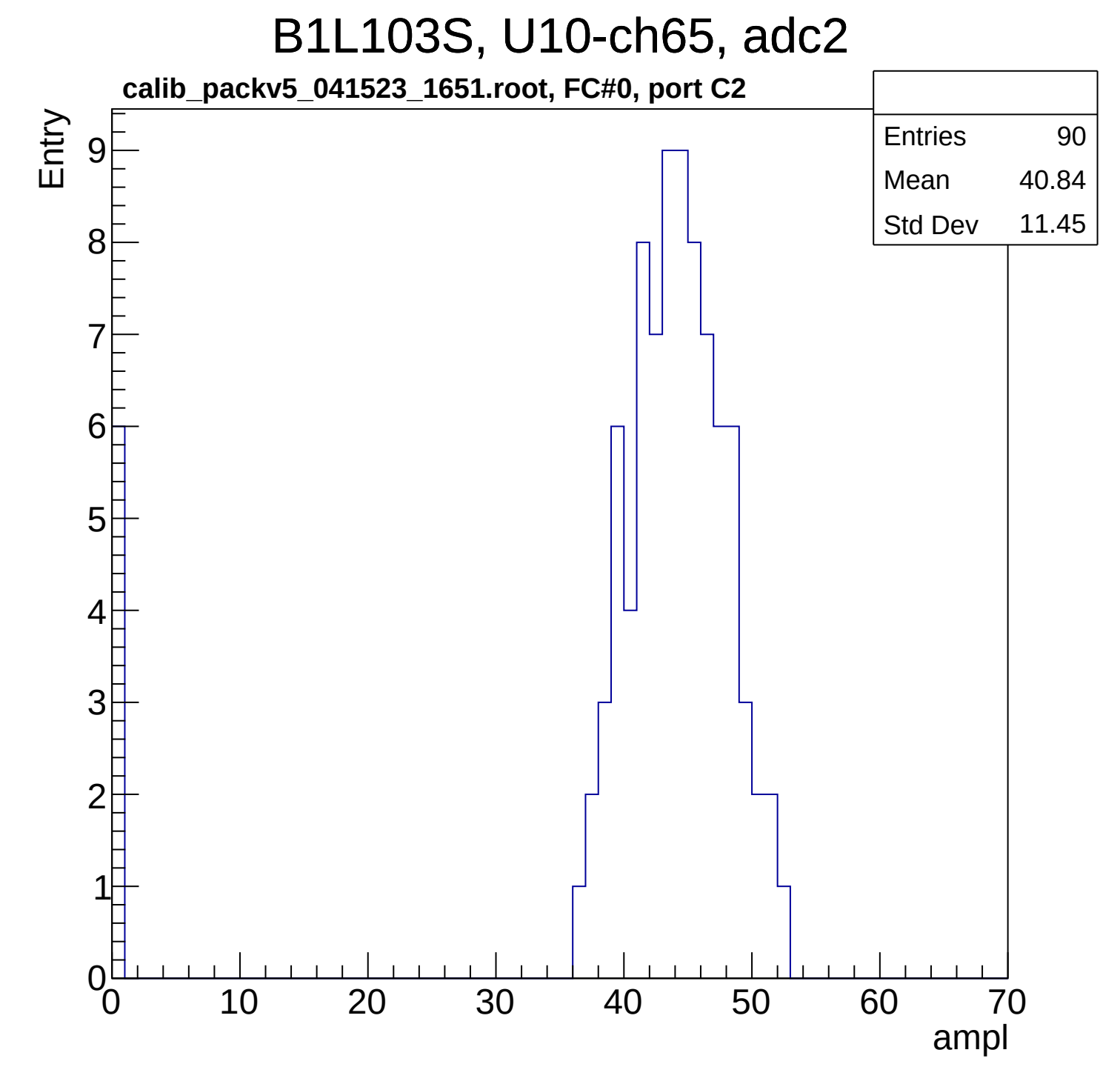

B1L103S, U10-ch64, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 58.14
Std Dev 9.199
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

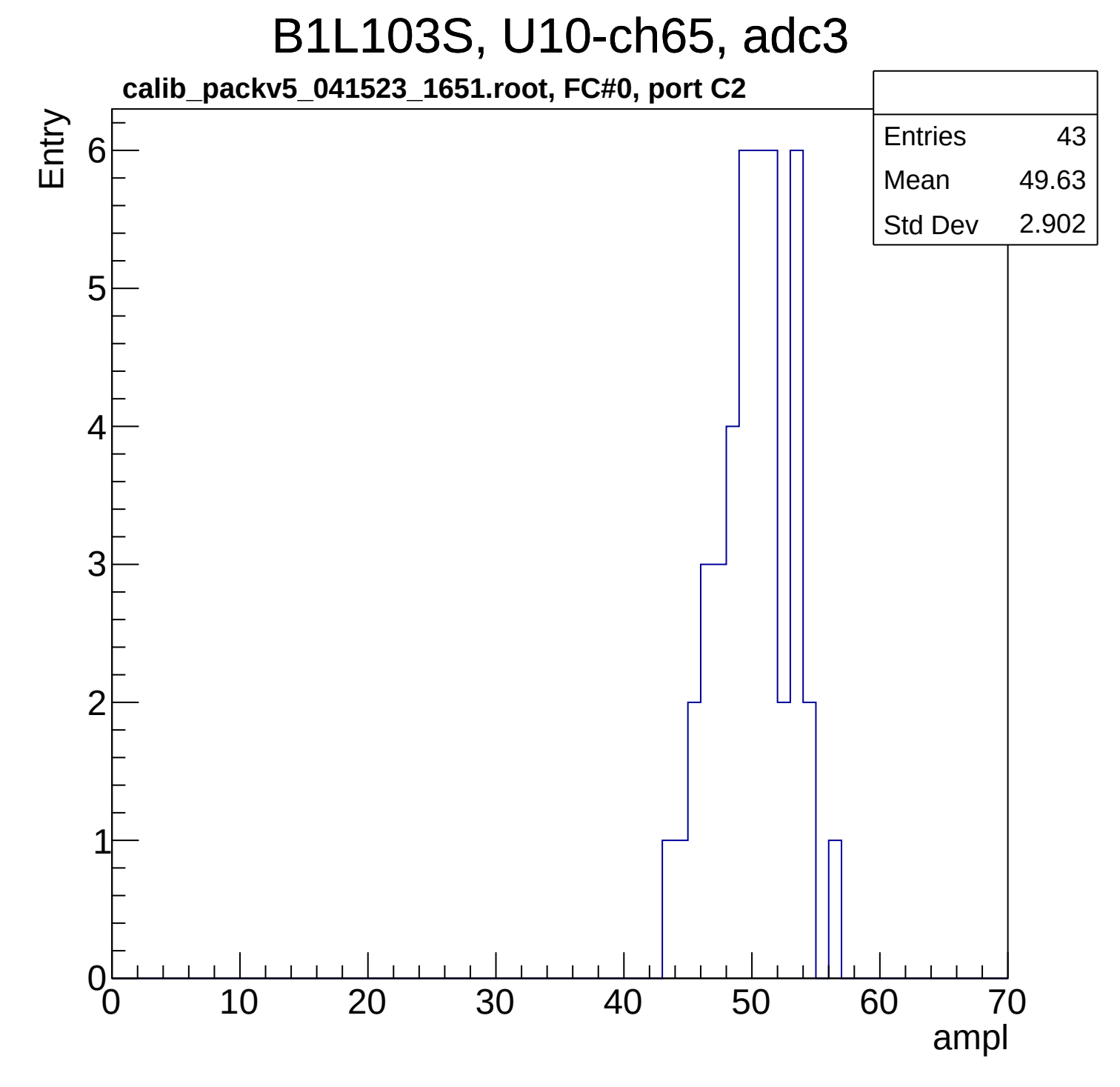

B1L103S, U10-ch64, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 62
Std Dev 1.323
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

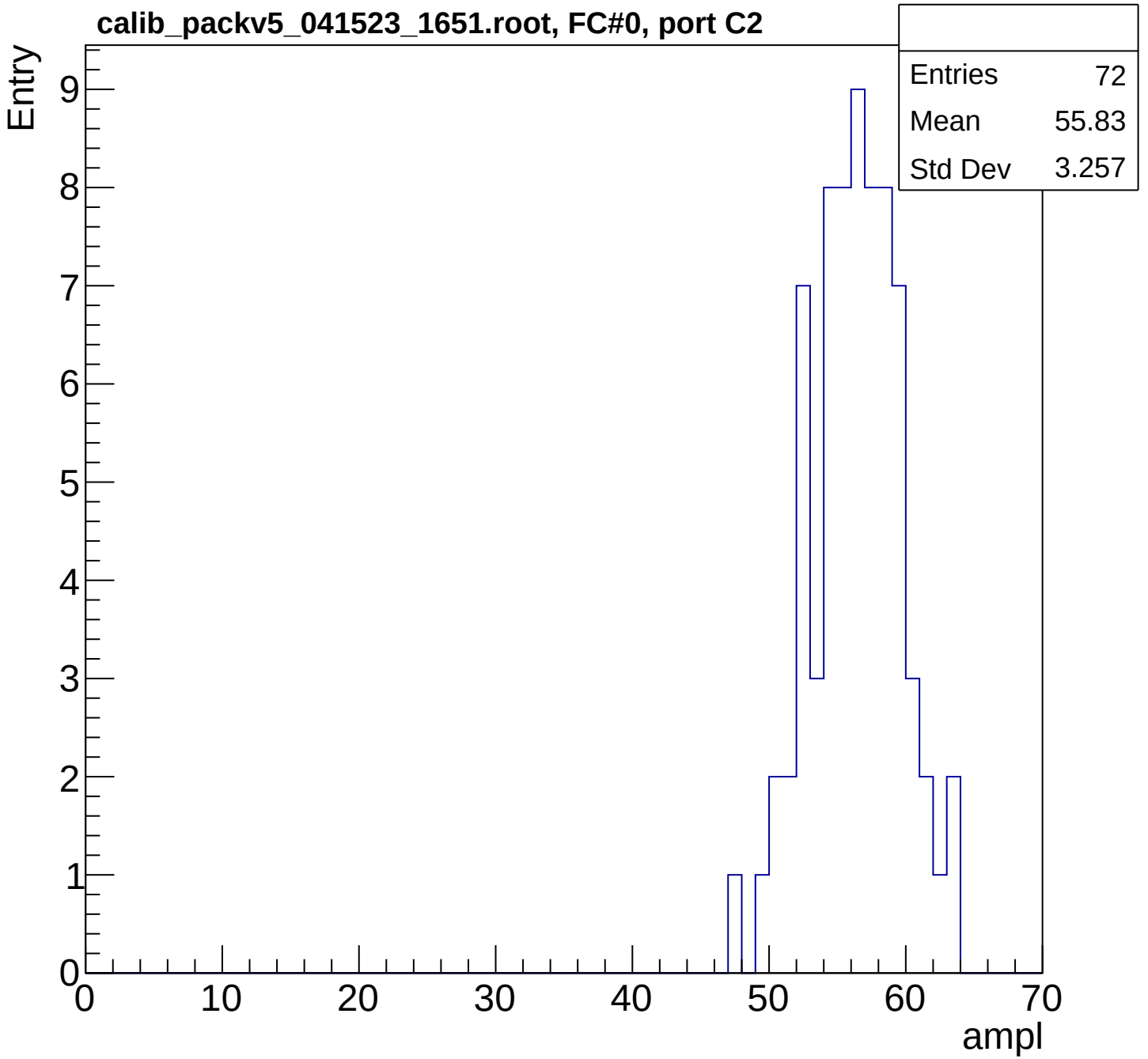

B1L103S, U10-ch64, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

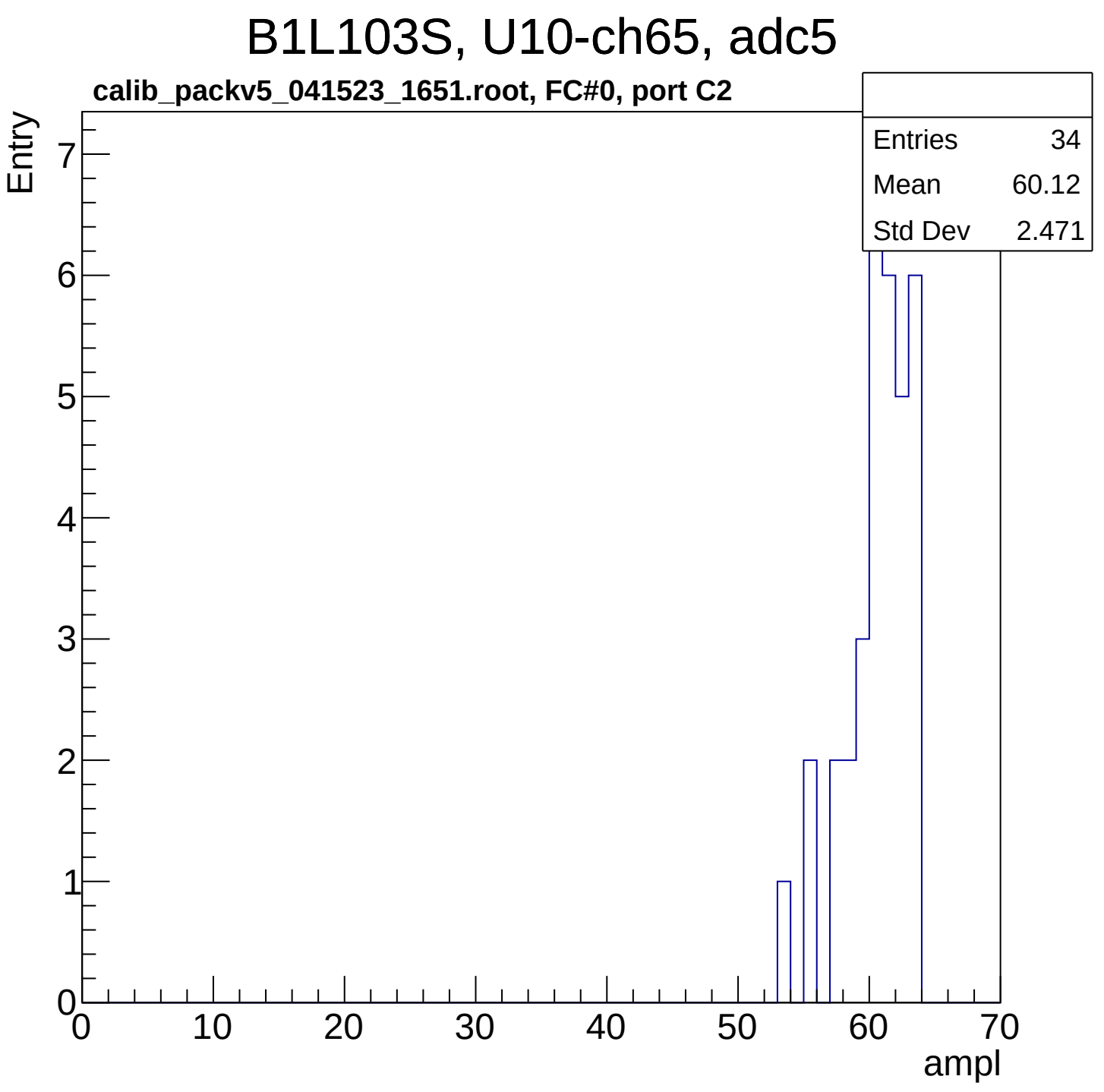

B1L103S, U10-ch65, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 94
Mean 26.85
Std Dev 10.7
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl

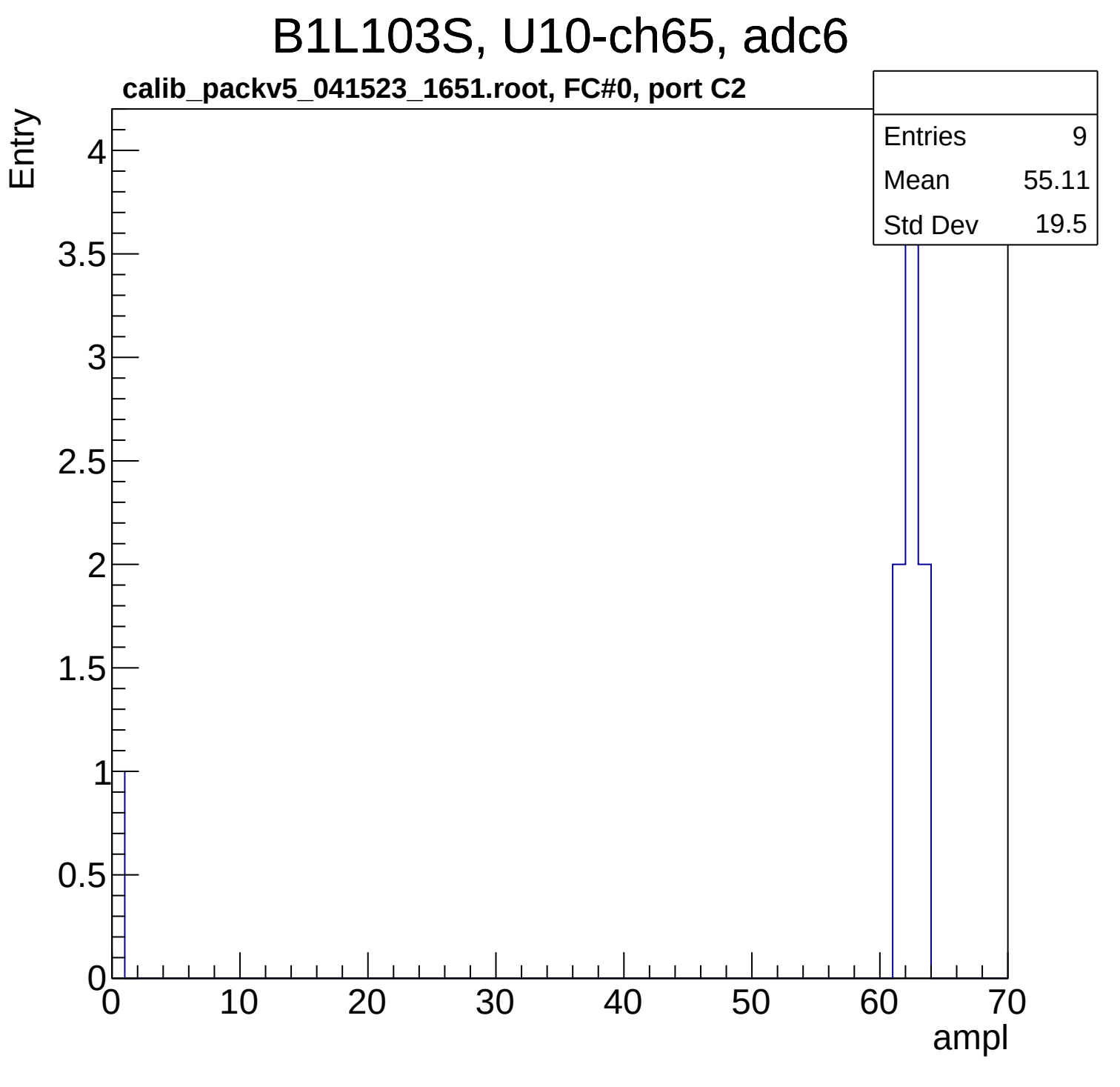

B1L103S, U10-ch65, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 33.52
Std Dev 11.47
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

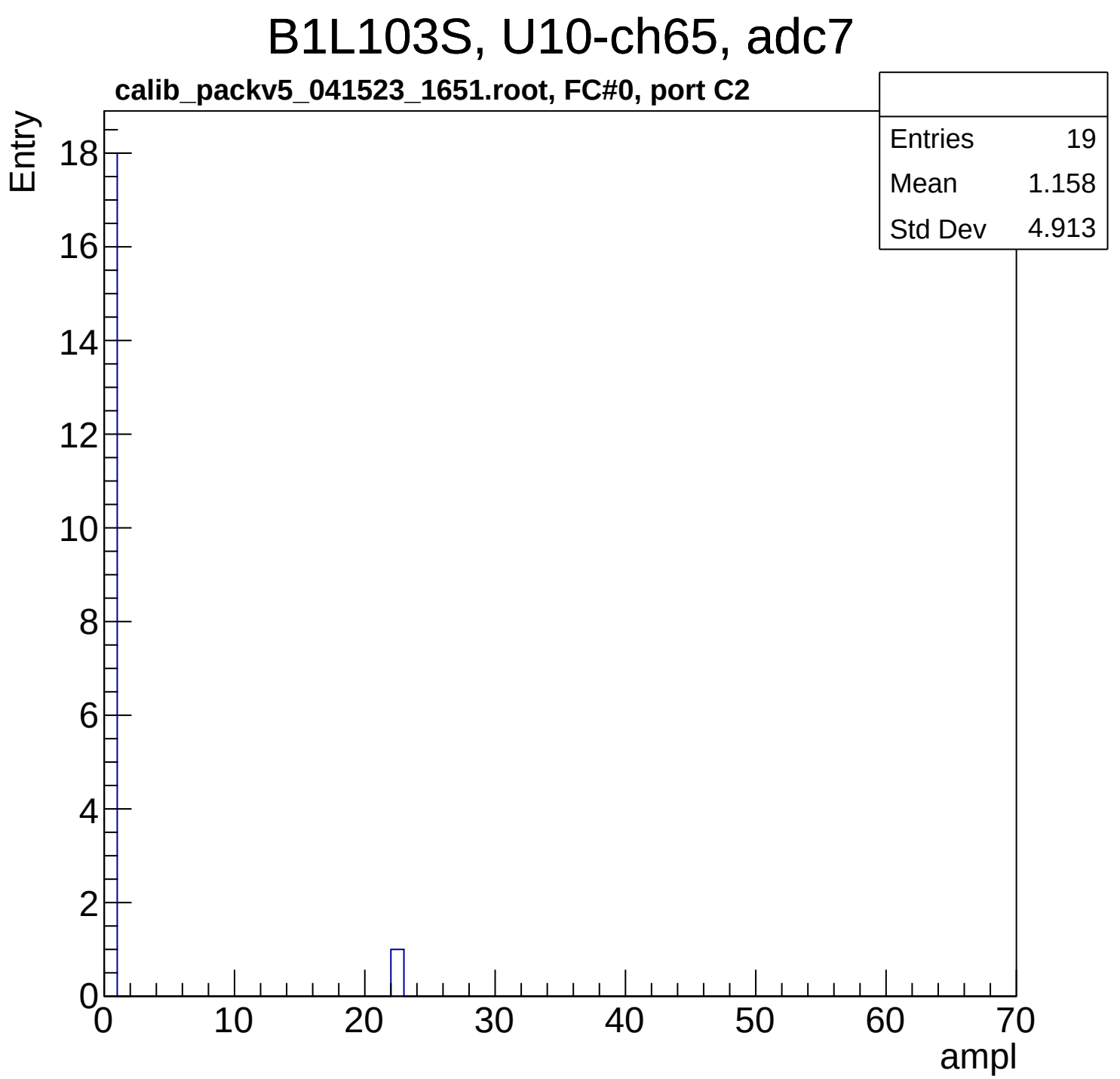

B1L103S, U10-ch65, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 90
Mean 40.84
Std Dev 11.45
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U10-ch65, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 43
Mean 49.63
Std Dev 2.902
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch65, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 55.83
Std Dev 3.257
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U10-ch65, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 34
Mean 60.12
Std Dev 2.471
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U10-ch65, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 9
Mean 55.11
Std Dev 19.5
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U10-ch65, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.158
Std Dev 4.913
Entry
0
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4
6
8
10
12
14
16
18
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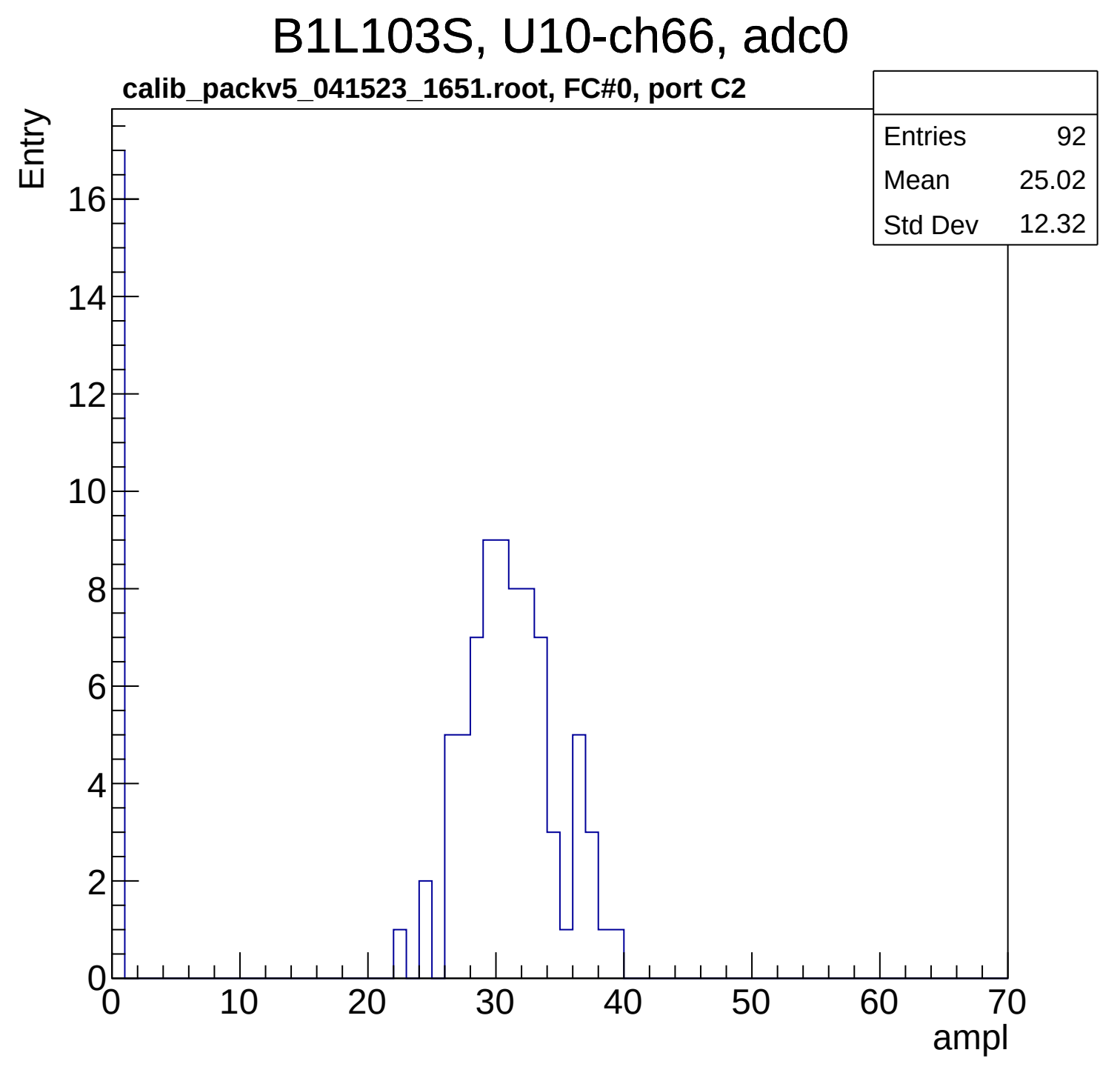
70
ampl


B1L103S, U10-ch66, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 92
Mean 25.02
Std Dev 12.32
Entry
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4
6
8
10
12
14
16
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10
20
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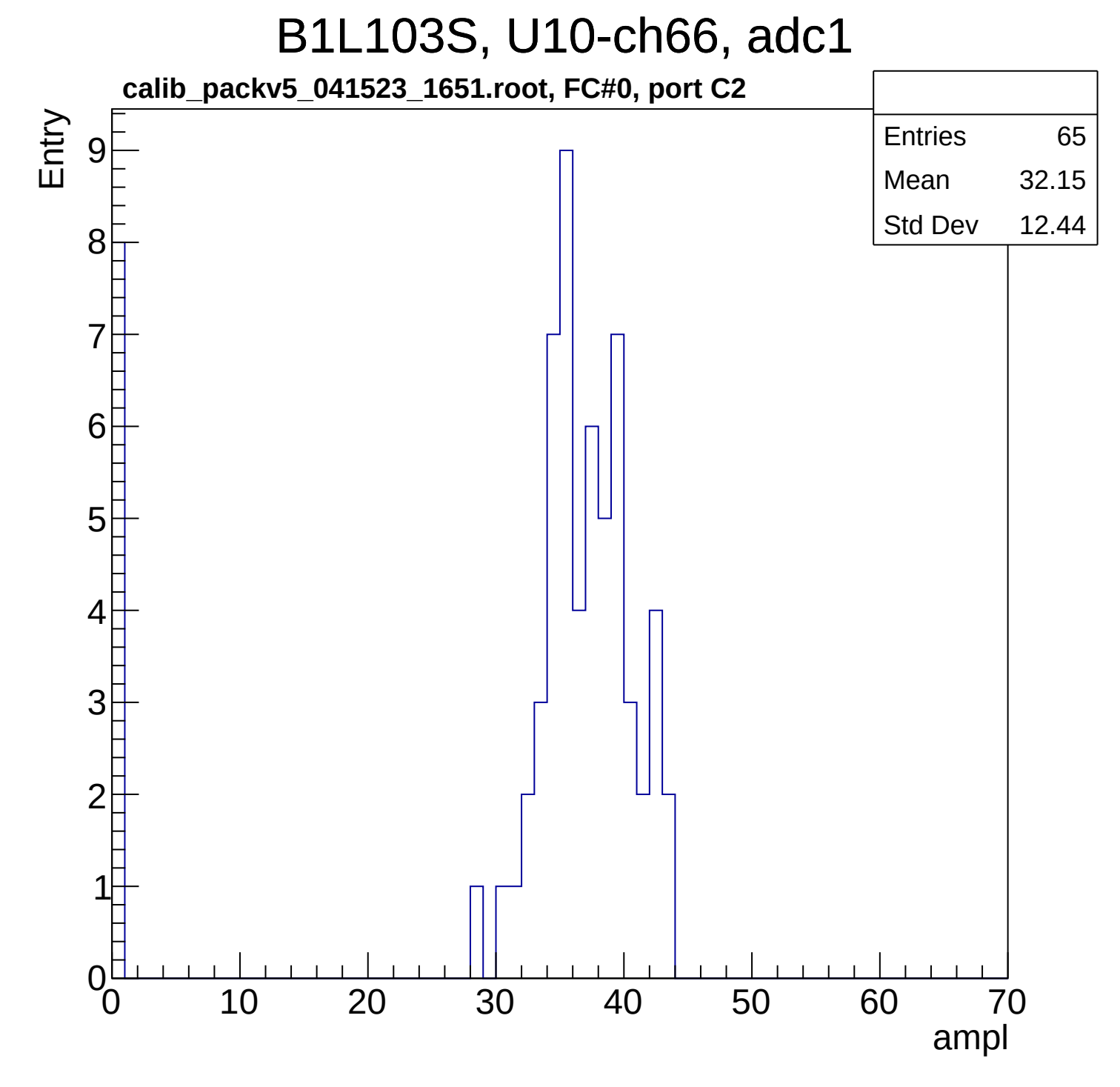
50
60
70
ampl


B1L103S, U10-ch66, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 32.15
Std Dev 12.44
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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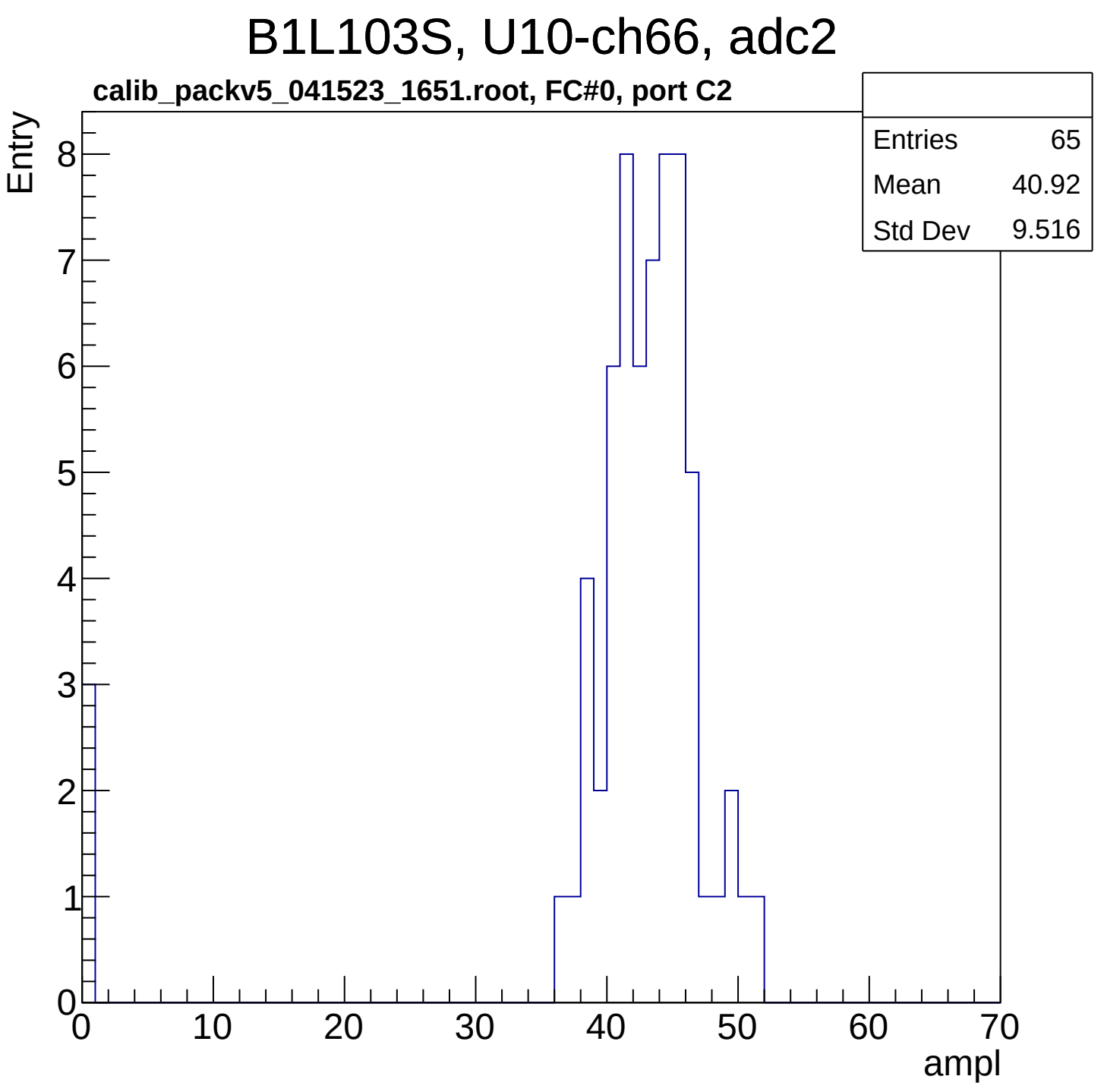
40
50
60
70


B1L103S, U10-ch66, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 40.92
Std Dev 9.516
Entry
ampl
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1
2
3
4
5
6
7
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0
10
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40
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60
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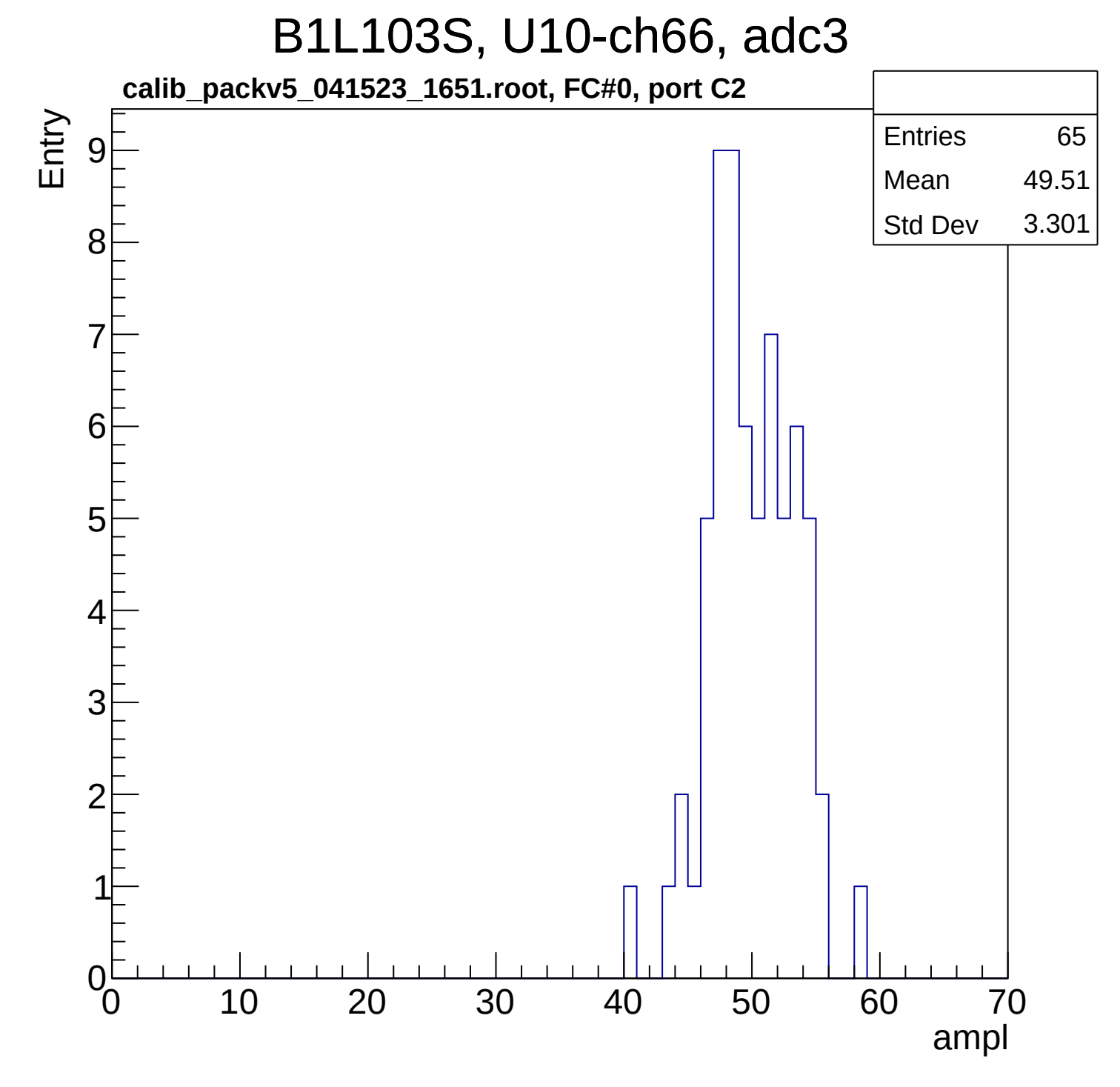
B1L103S, U10-ch66, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 49.51
Std Dev 3.301
Entry
ampl
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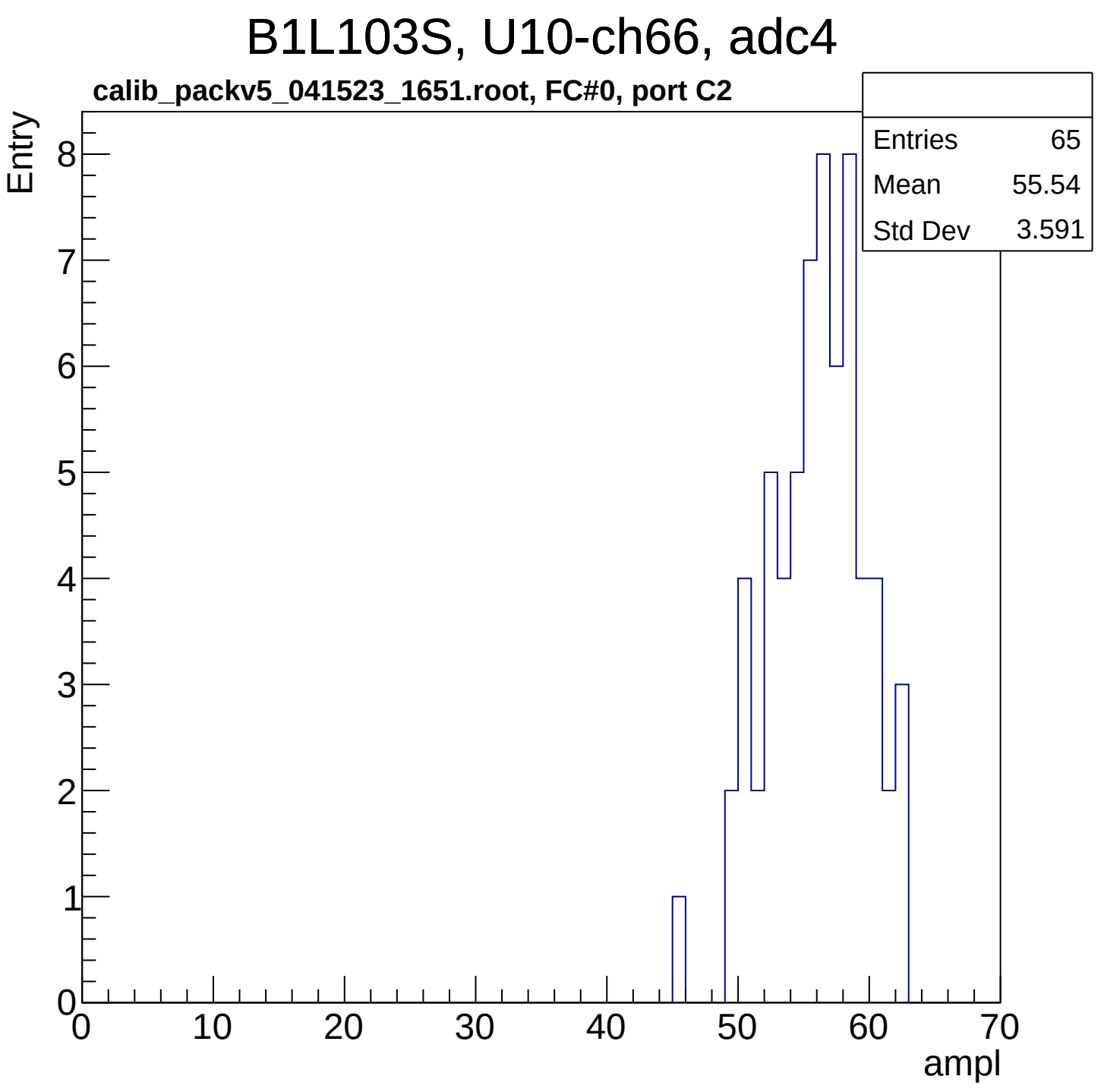
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U10-ch66, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 55.54
Std Dev 3.591
Entry
ampl
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1
2
3
4
5
6
7
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0
10
20
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40
50
60
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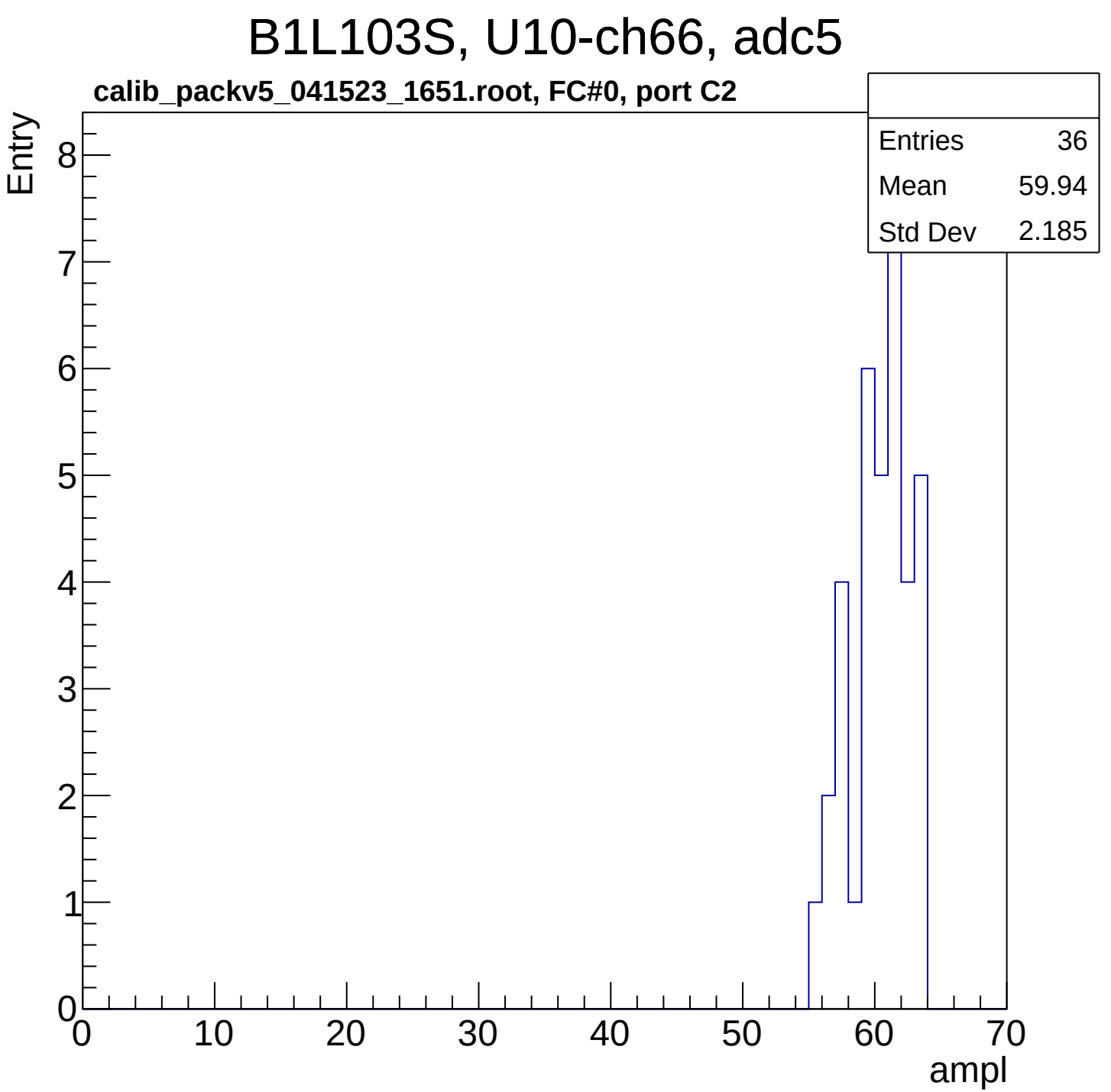
B1L103S, U10-ch66, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 36
Mean 59.94
Std Dev 2.185
Entry
ampl
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1
2
3
4
5
6
7
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0
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40
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60
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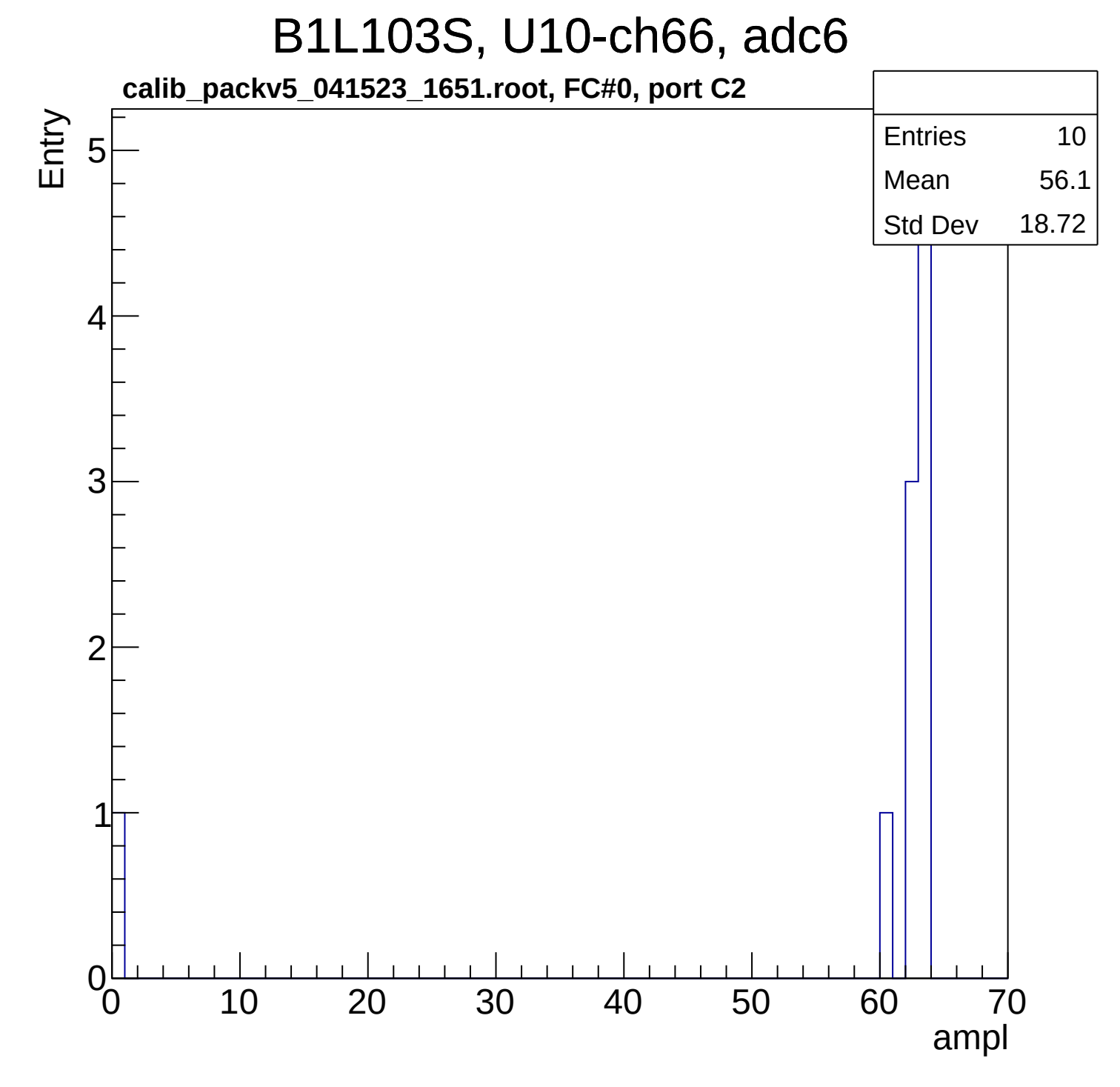
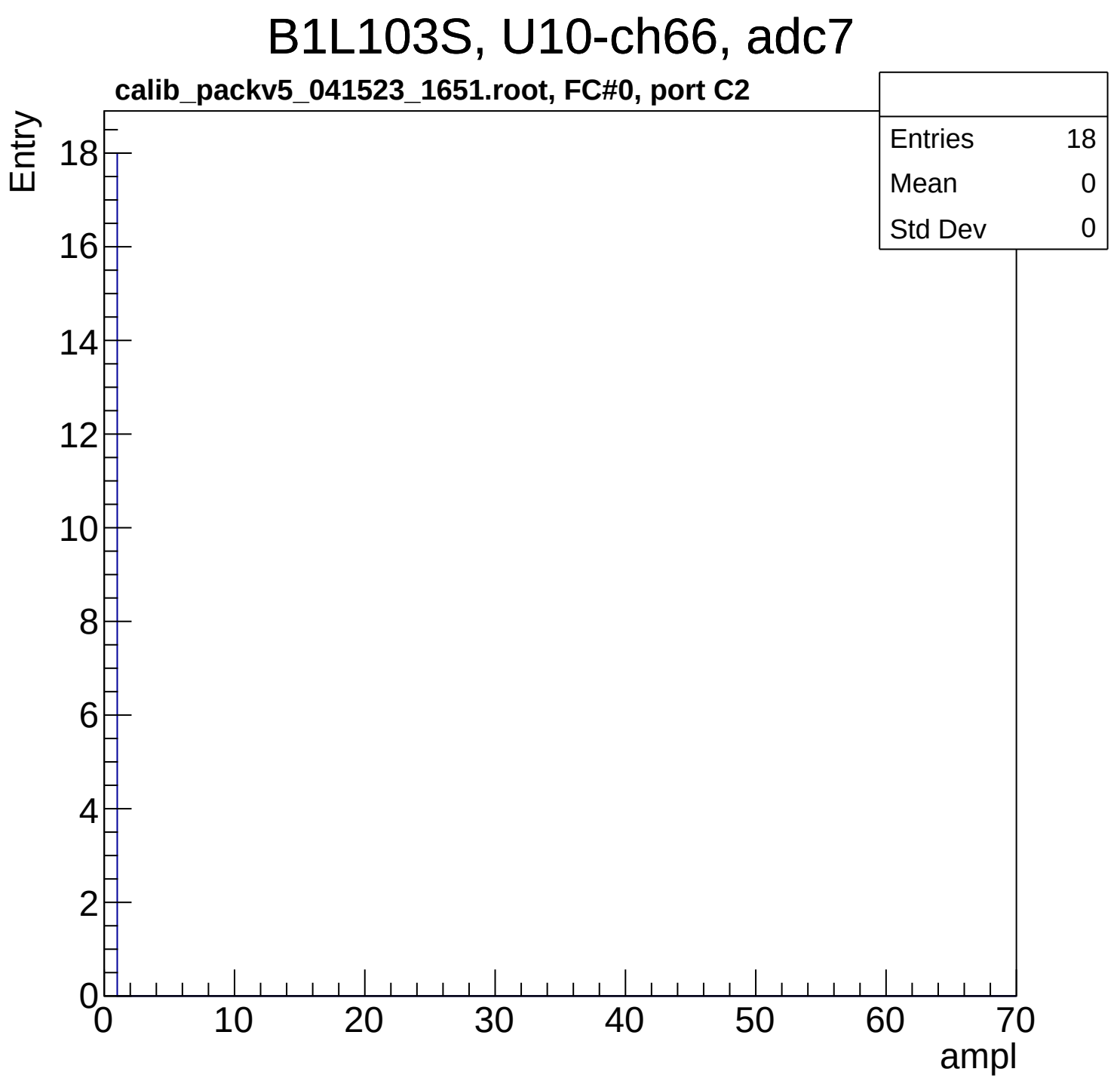
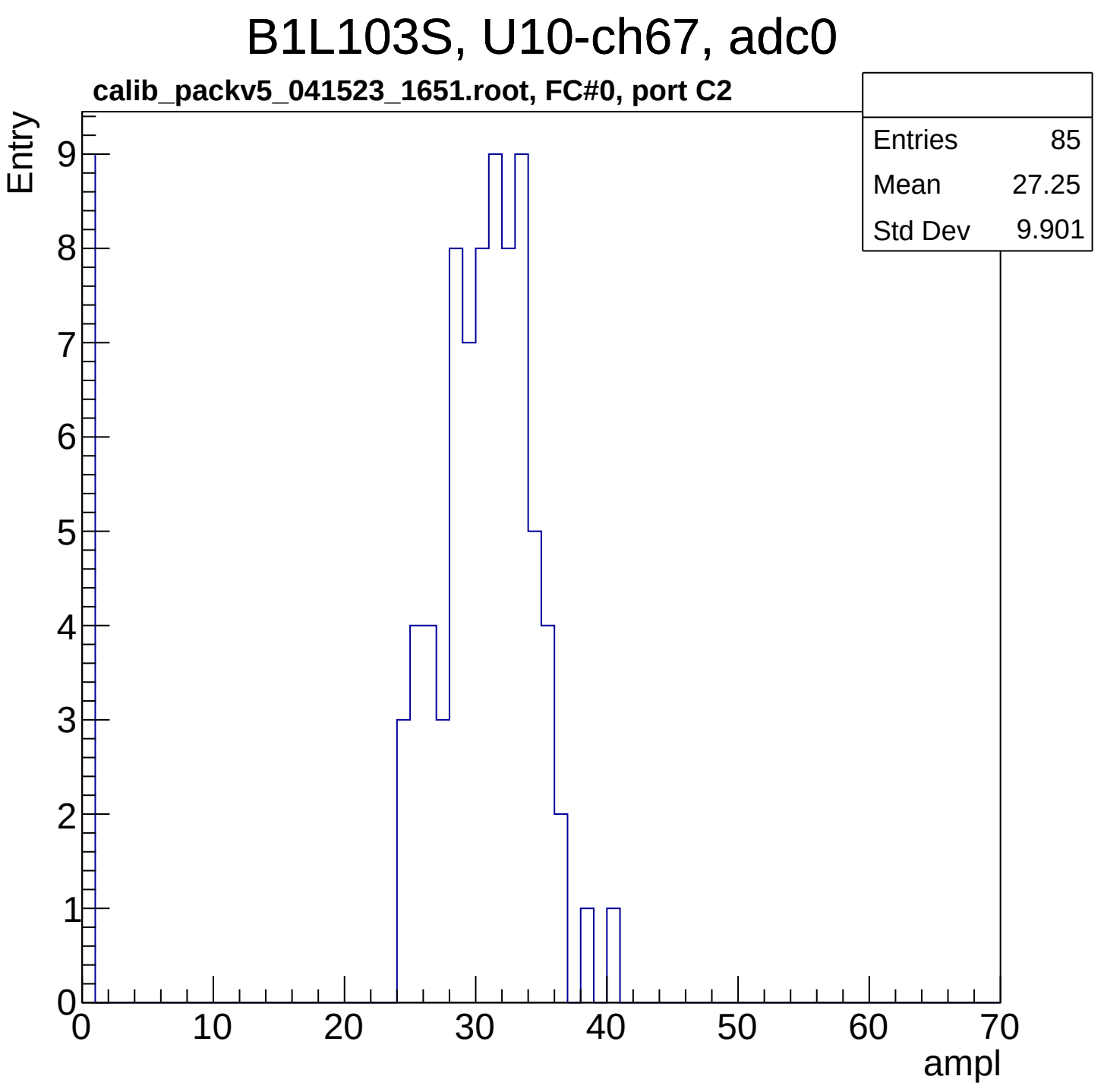

B1L103S, U10-ch66, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 56.1
Std Dev 18.72
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U10-ch66, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch67, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 27.25
Std Dev 9.901
Entry
ampl
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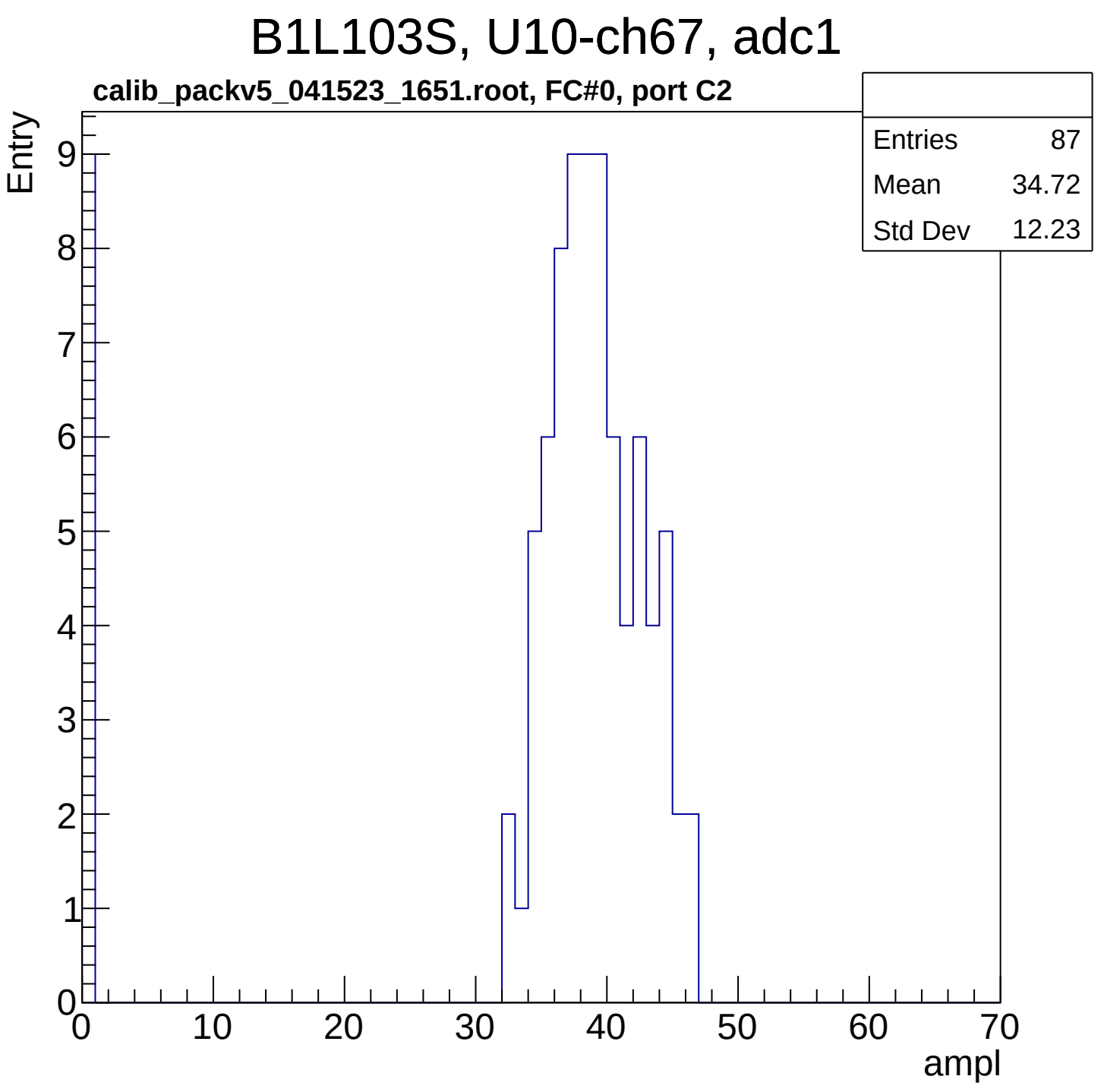
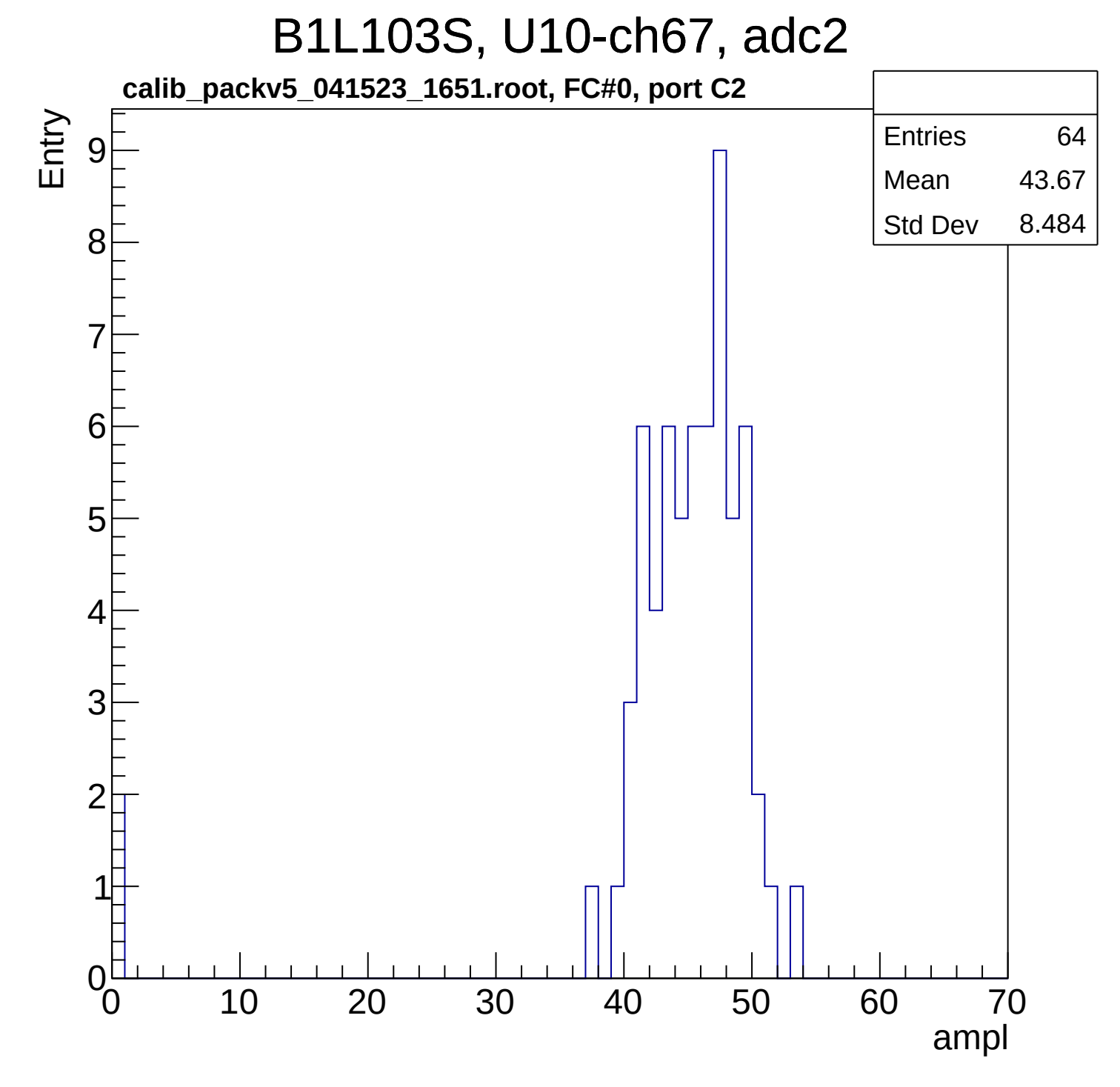
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U10-ch67, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 87
Mean 34.72
Std Dev 12.23
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U10-ch67, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 43.67
Std Dev 8.484
Entry
ampl
0
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2
3
4
5
6
7
8
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0
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20
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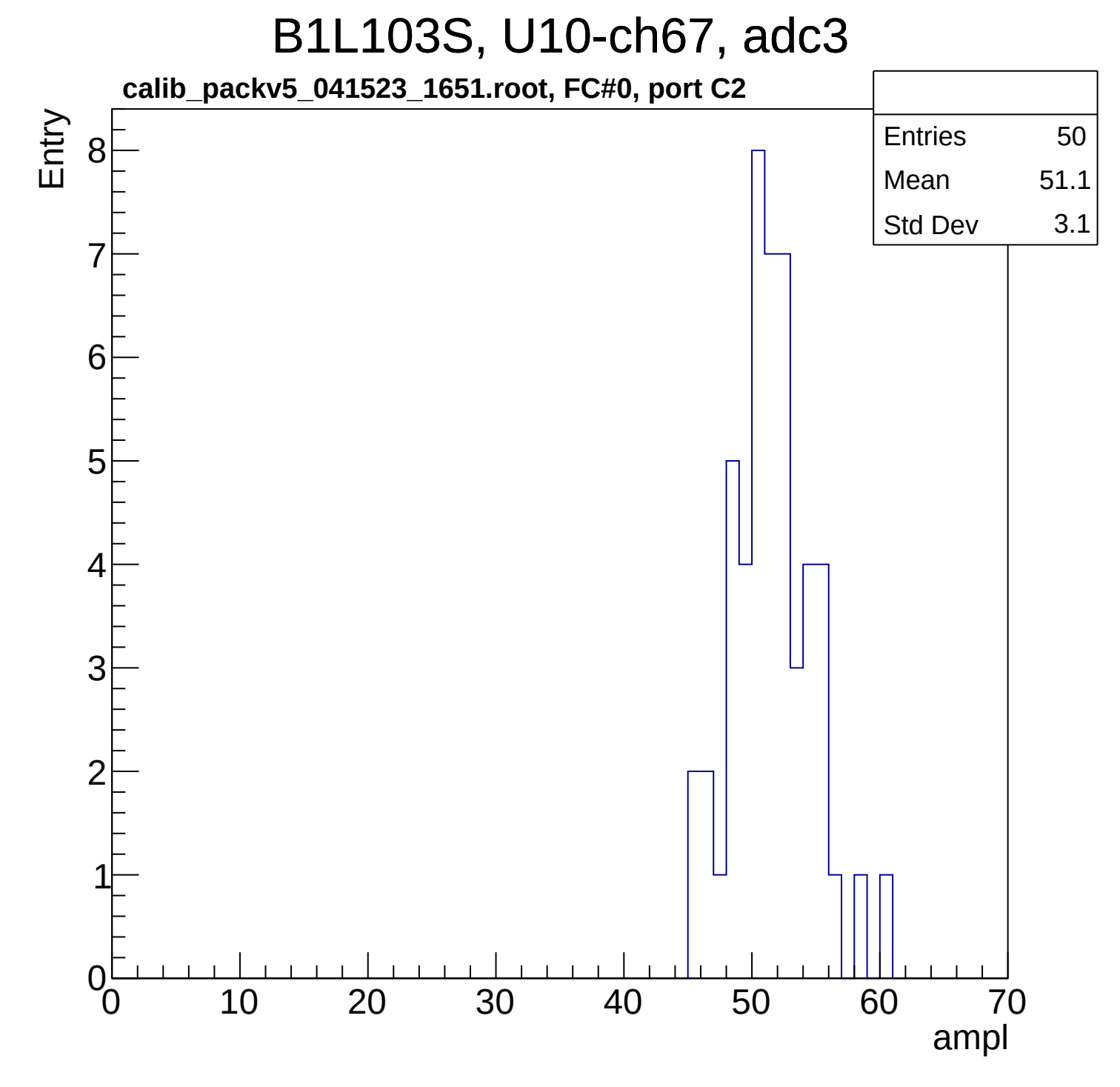
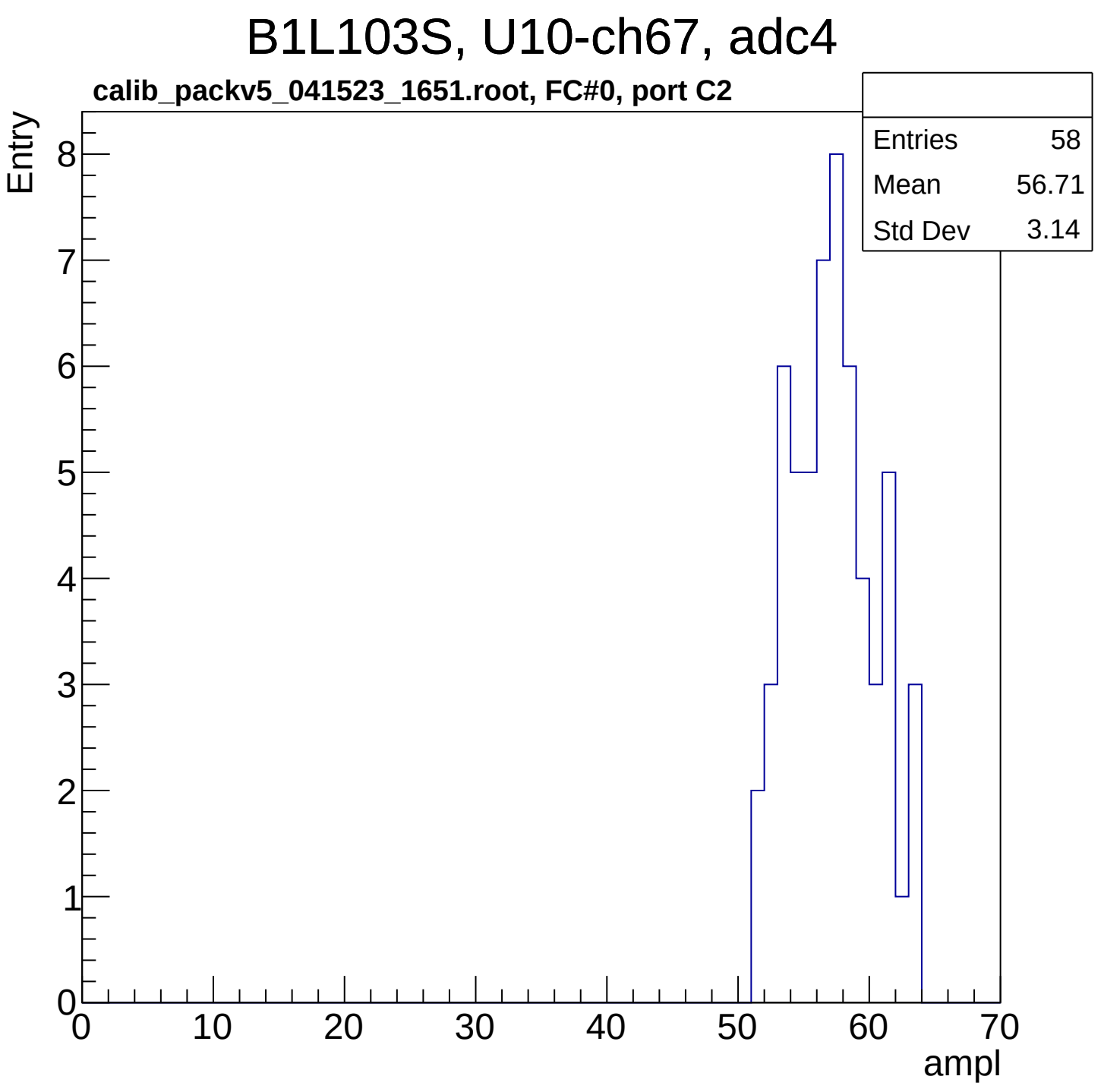
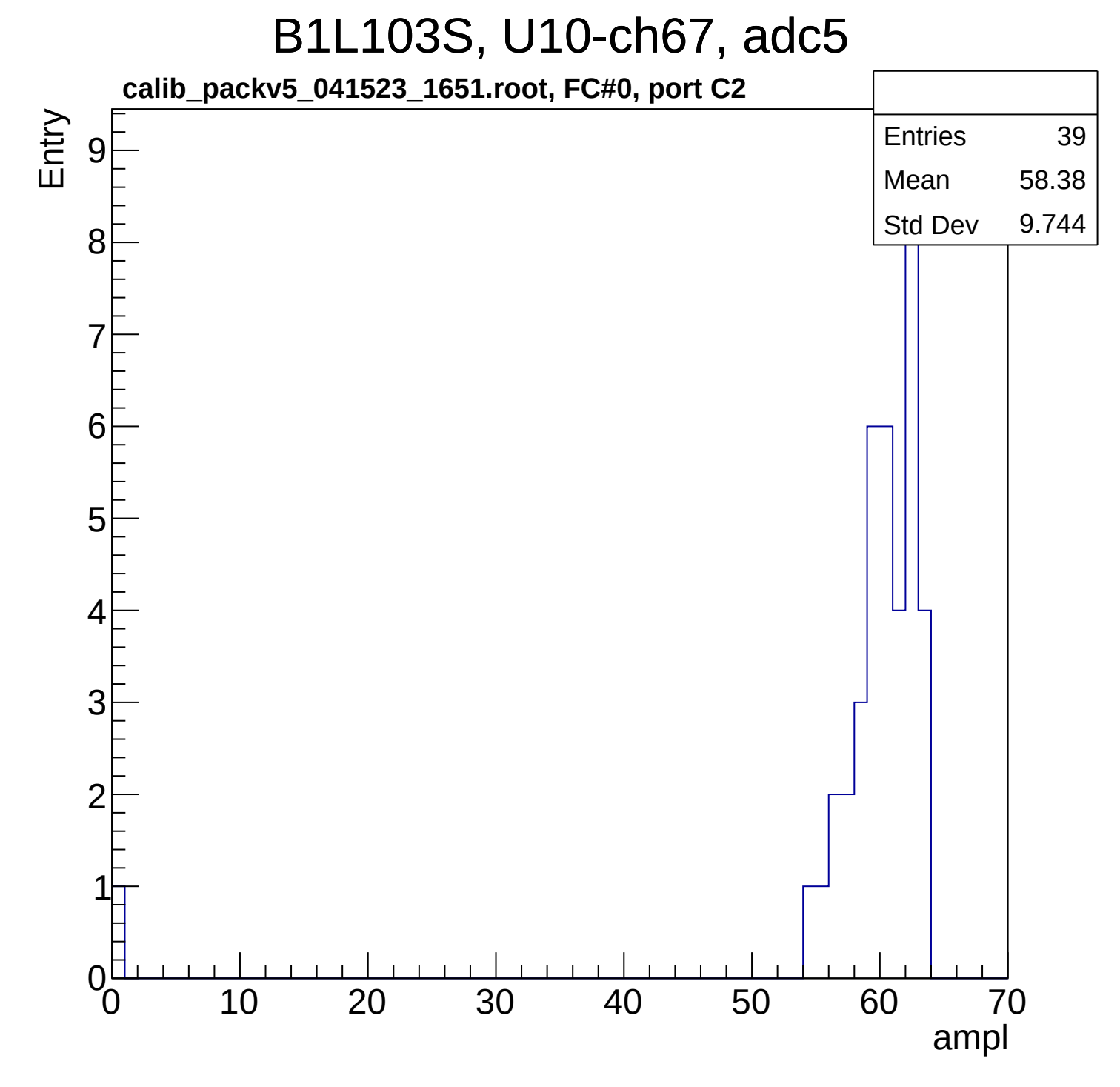
40
50
60
70


B1L103S, U10-ch67, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 51.1
Std Dev 3.1
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U10-ch67, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 56.71
Std Dev 3.14
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U10-ch67, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 39
Mean 58.38
Std Dev 9.744
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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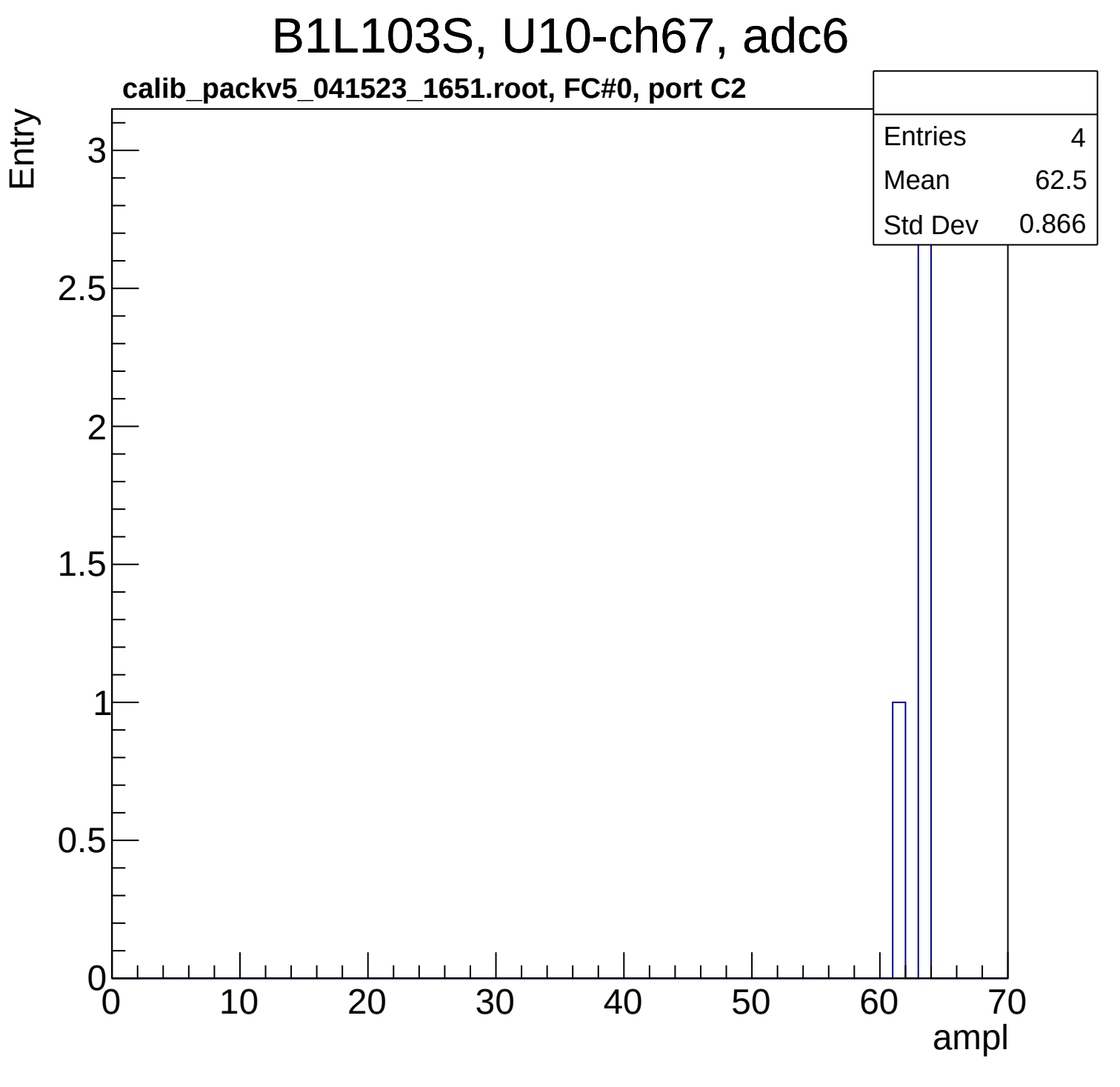
40
50
60
70


B1L103S, U10-ch67, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 4
Mean 62.5
Std Dev 0.866
Entry
ampl
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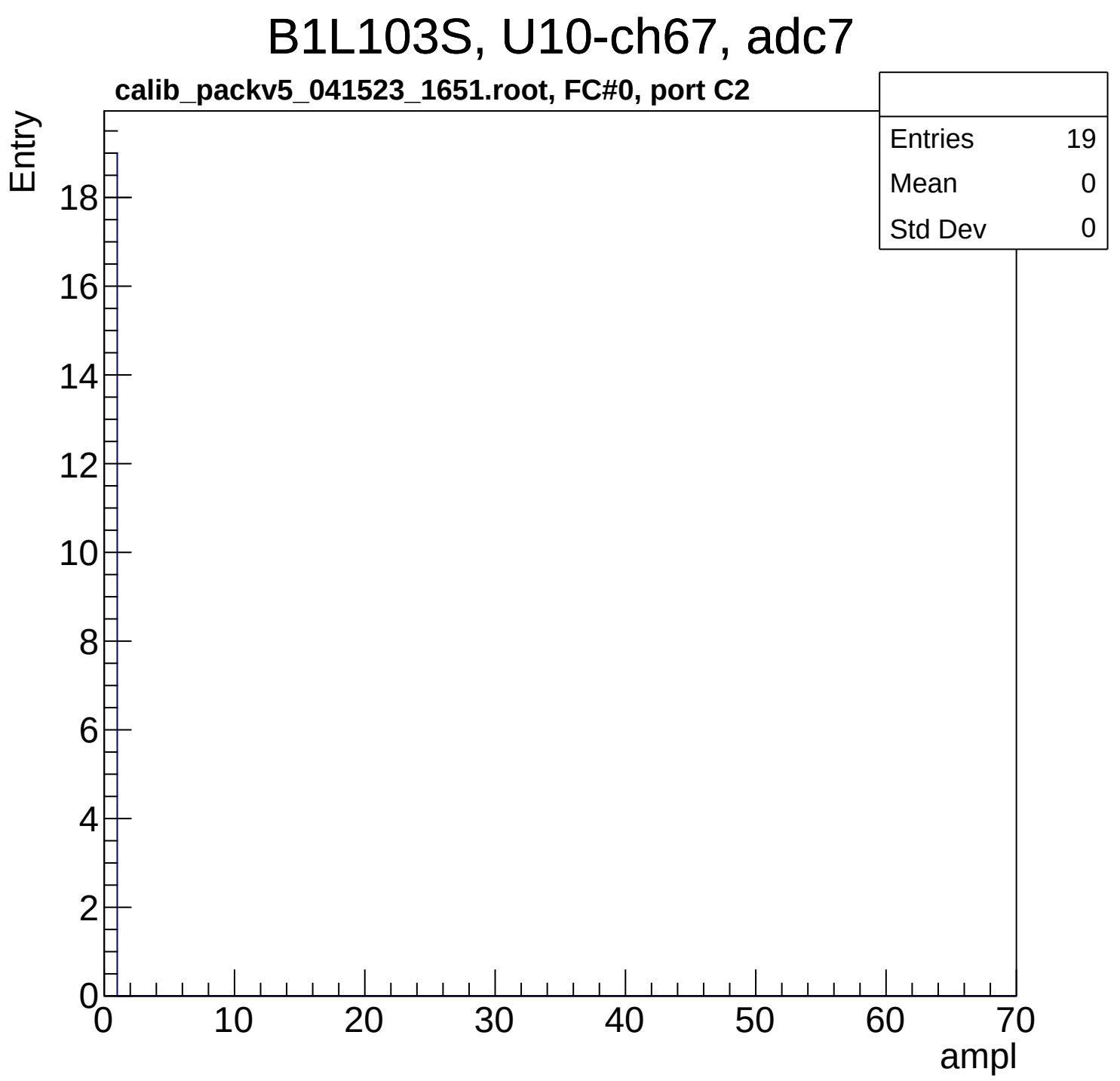
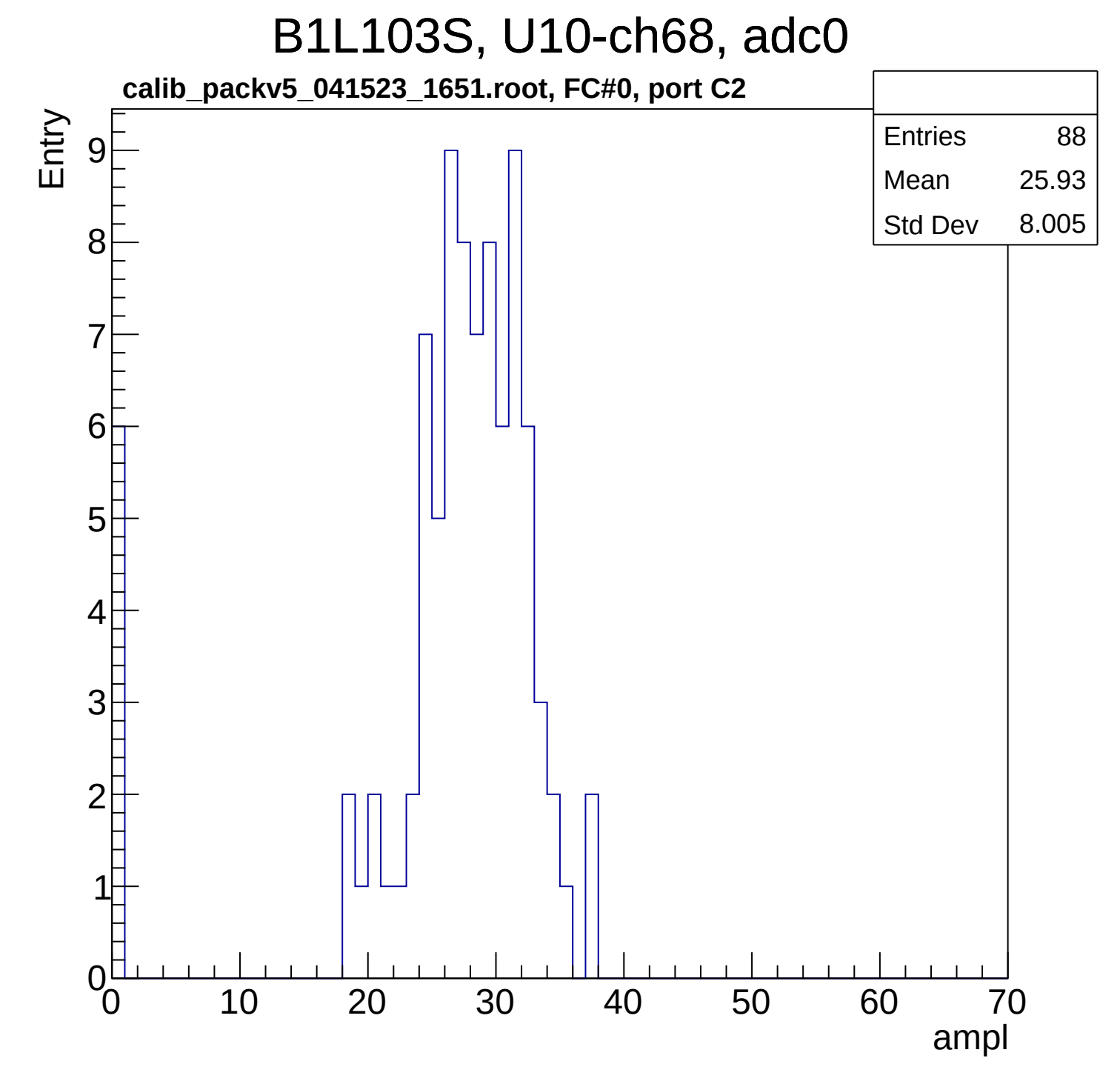
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U10-ch67, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch68, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 88
Mean 25.93
Std Dev 8.005
Entry
ampl
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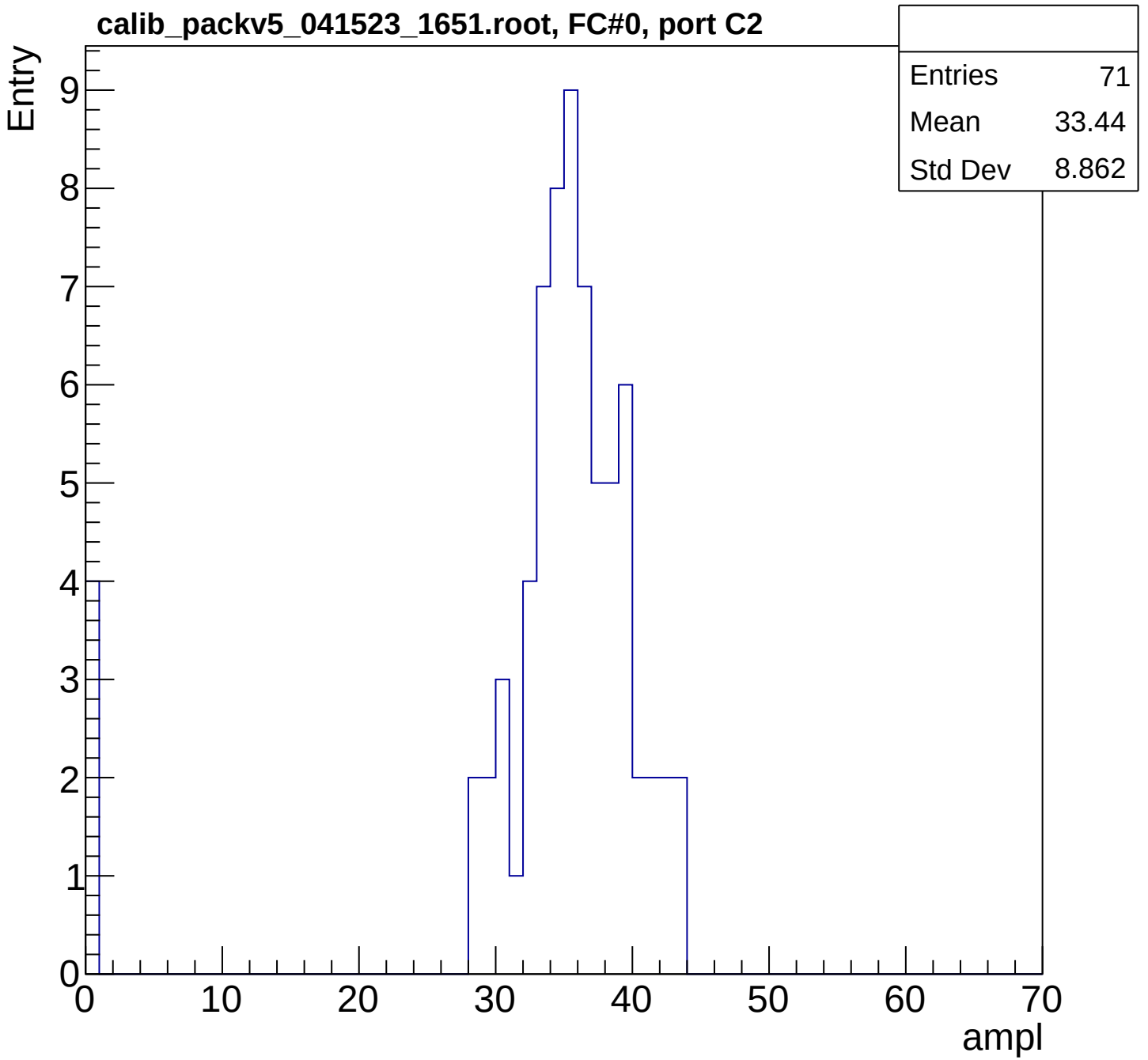
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U10-ch68, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 33.44
Std Dev 8.862
Entry
ampl
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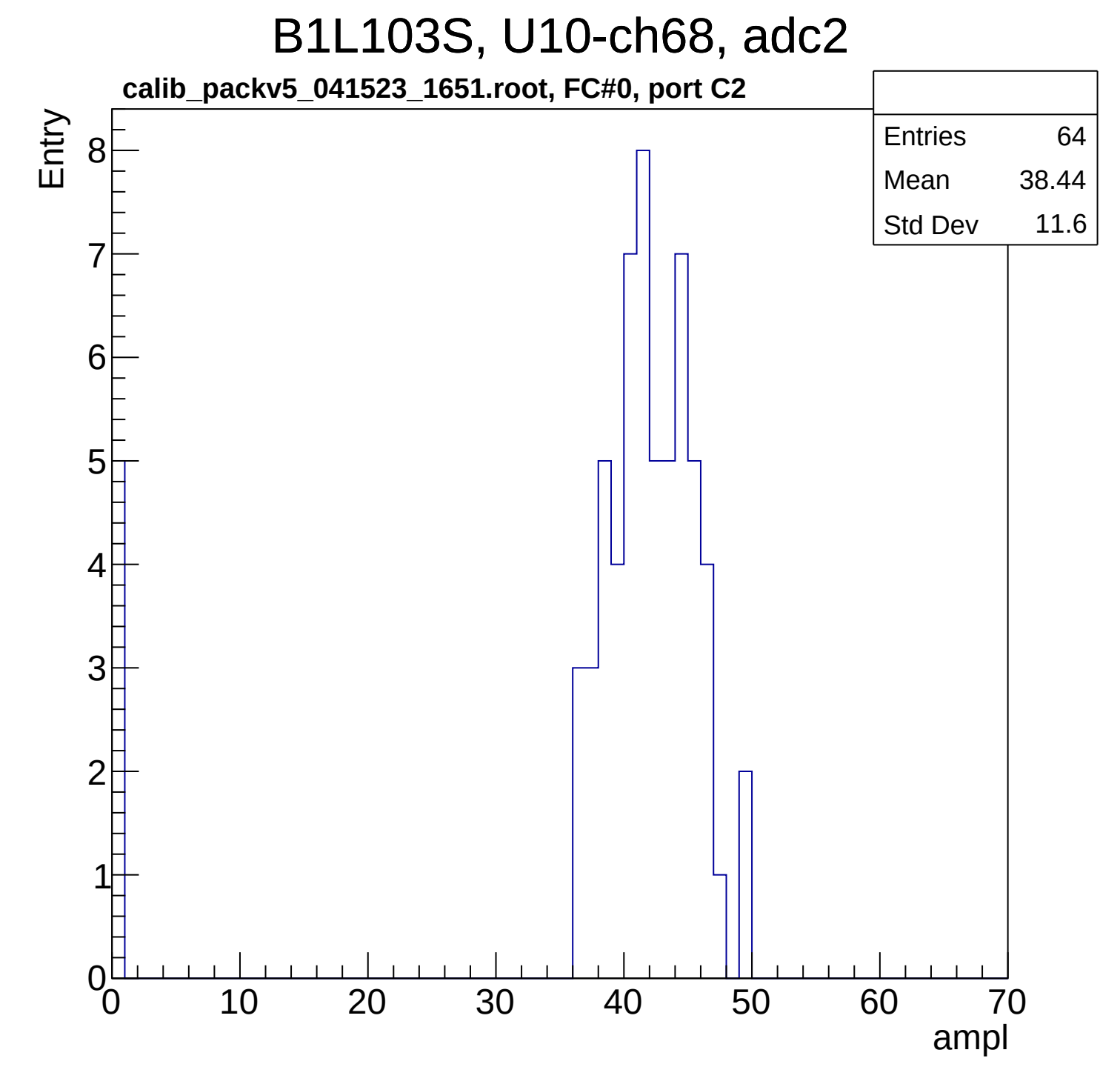
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U10-ch68, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 38.44
Std Dev 11.6
Entry
ampl
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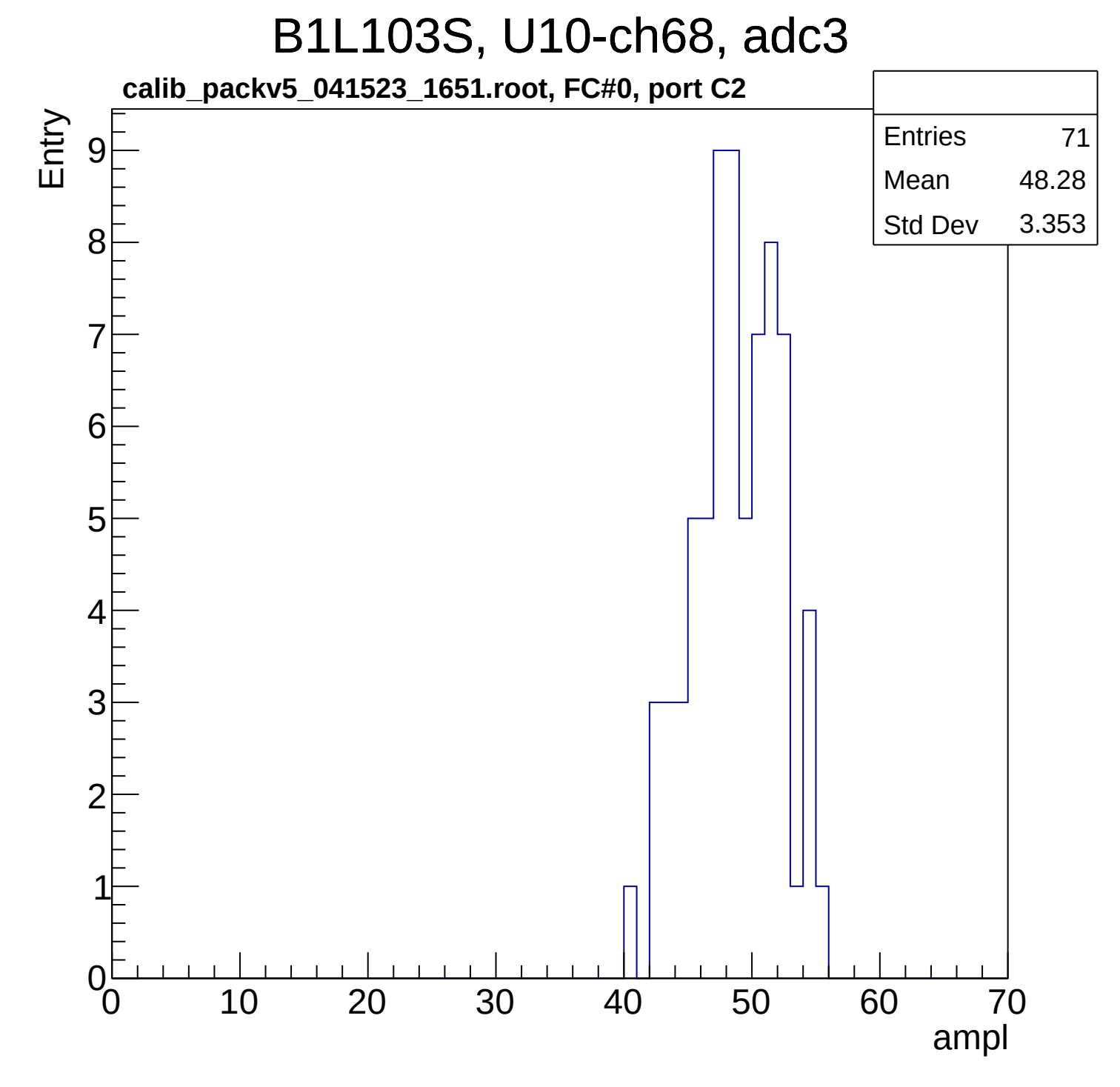
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U10-ch68, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 48.28
Std Dev 3.353
Entry
ampl
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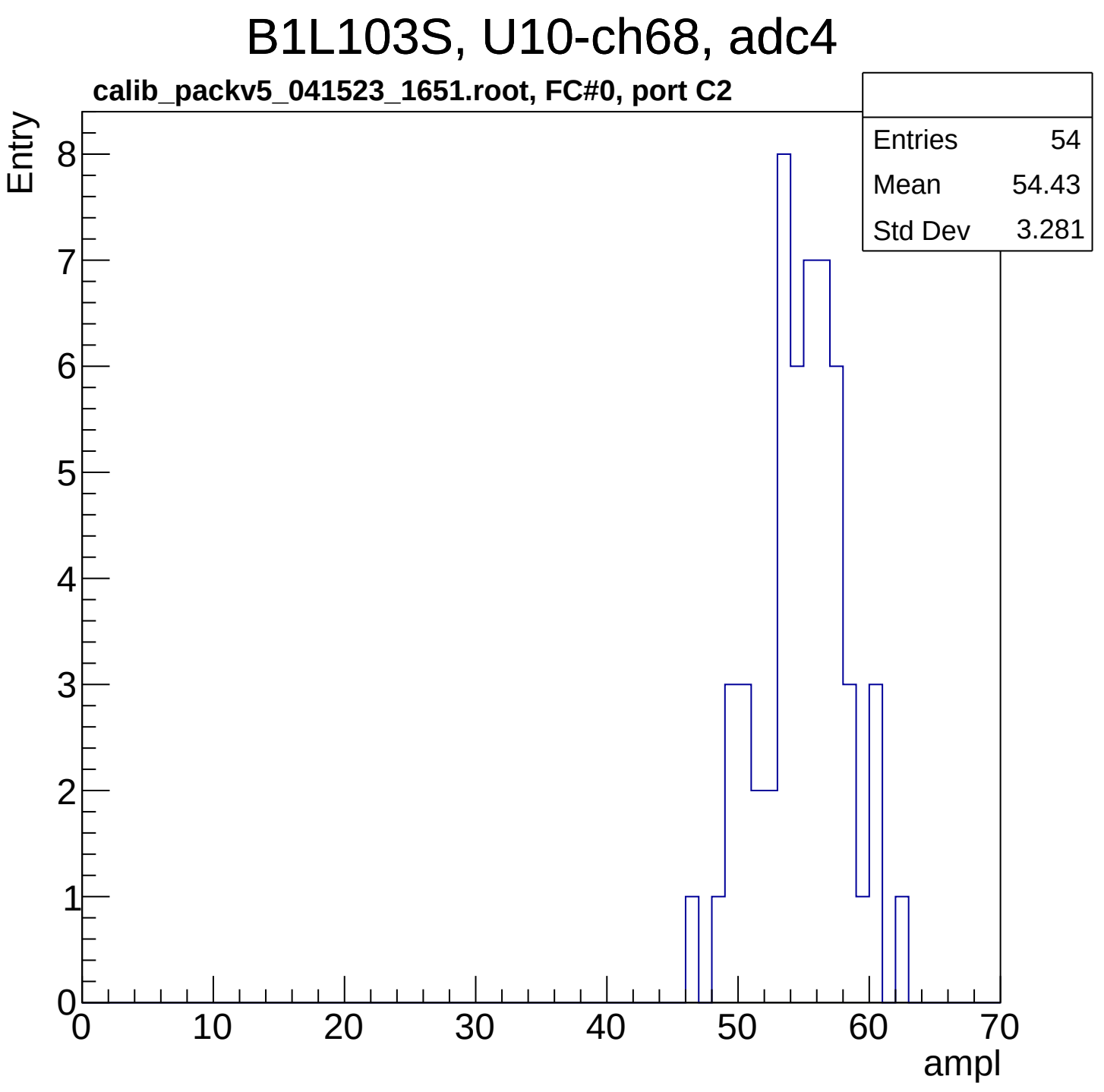
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U10-ch68, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 54.43
Std Dev 3.281
Entry
ampl
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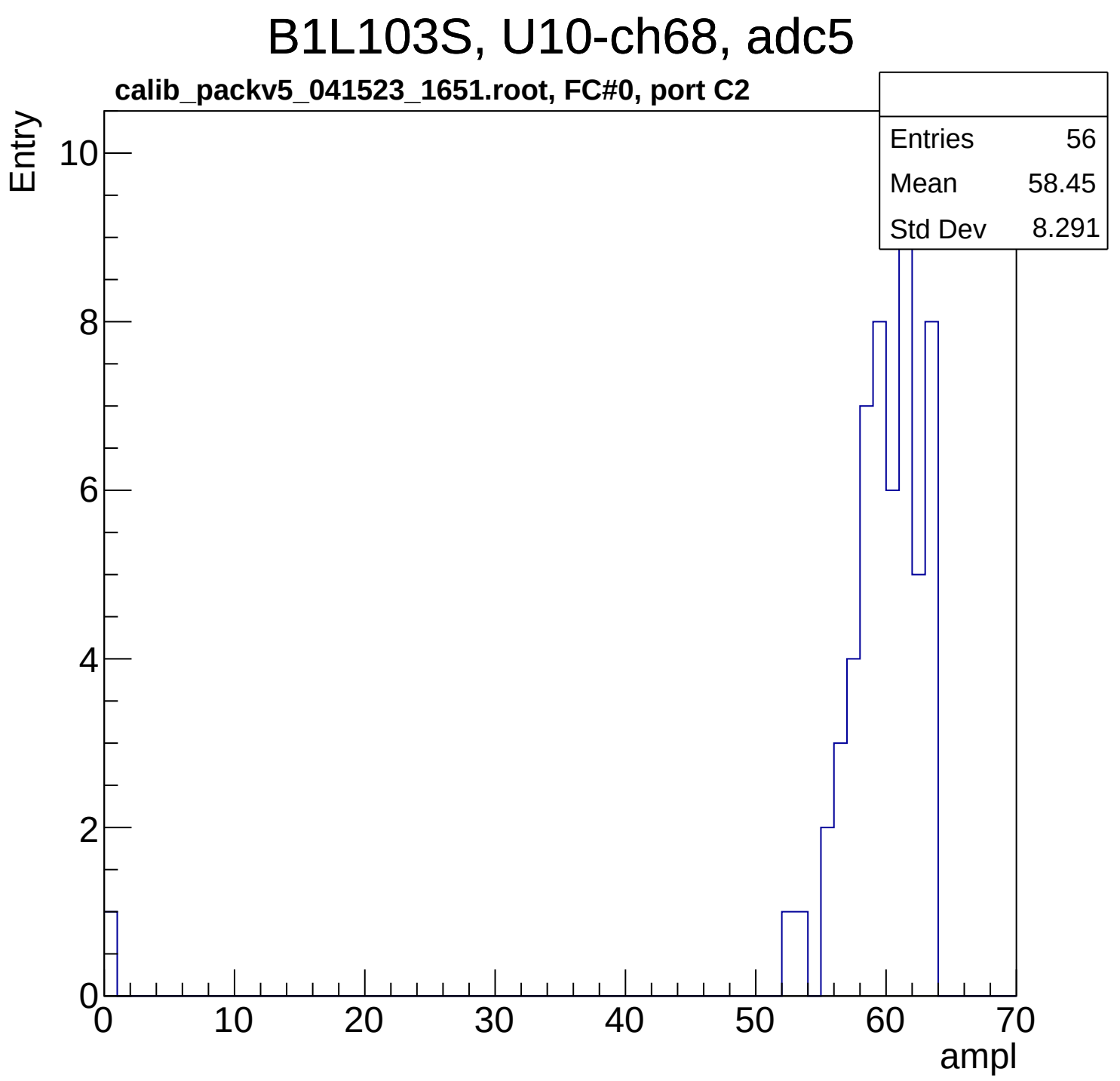
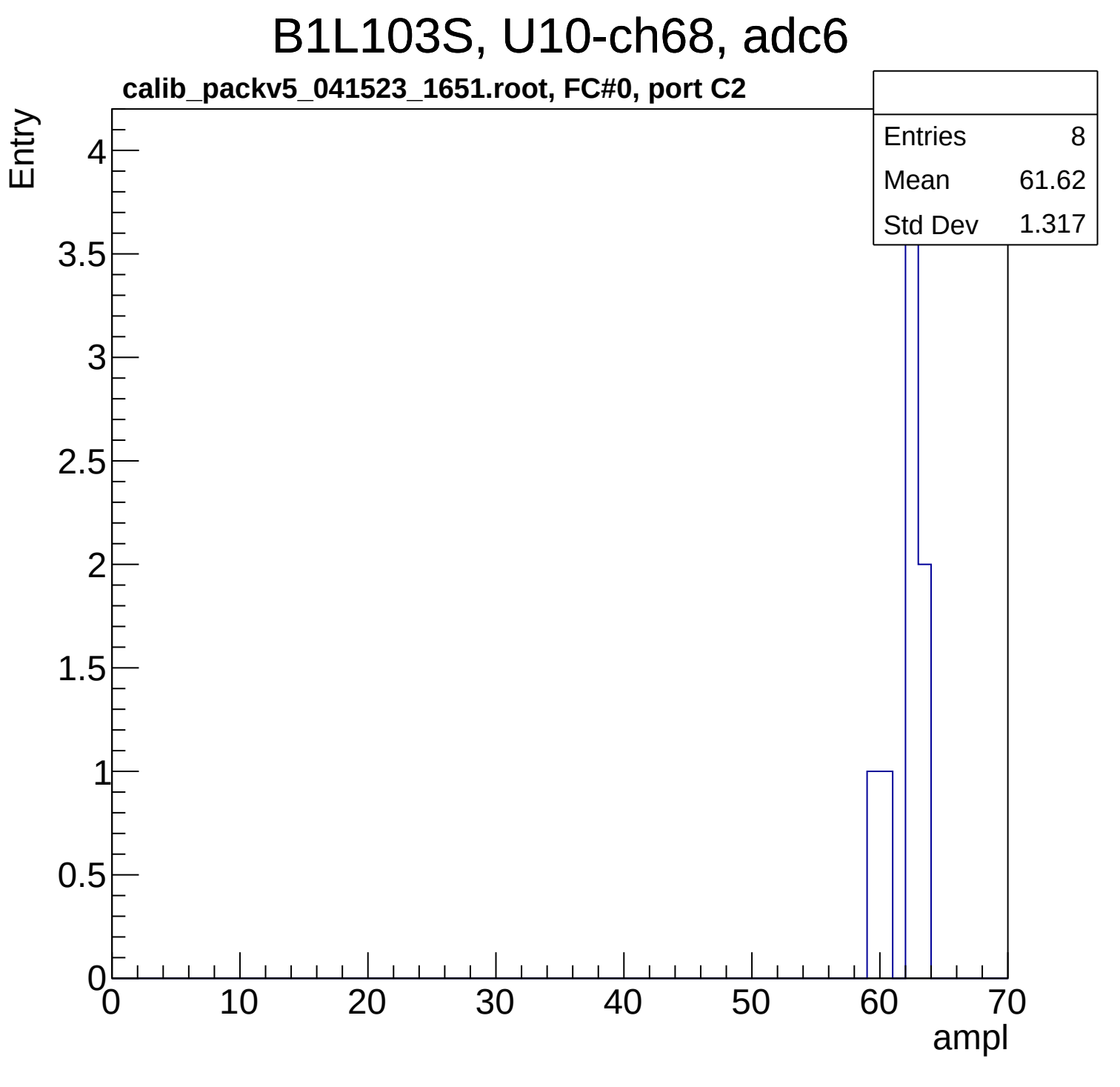
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U10-ch68, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 58.45
Std Dev 8.291
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch68, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 61.62
Std Dev 1.317
Entry
ampl
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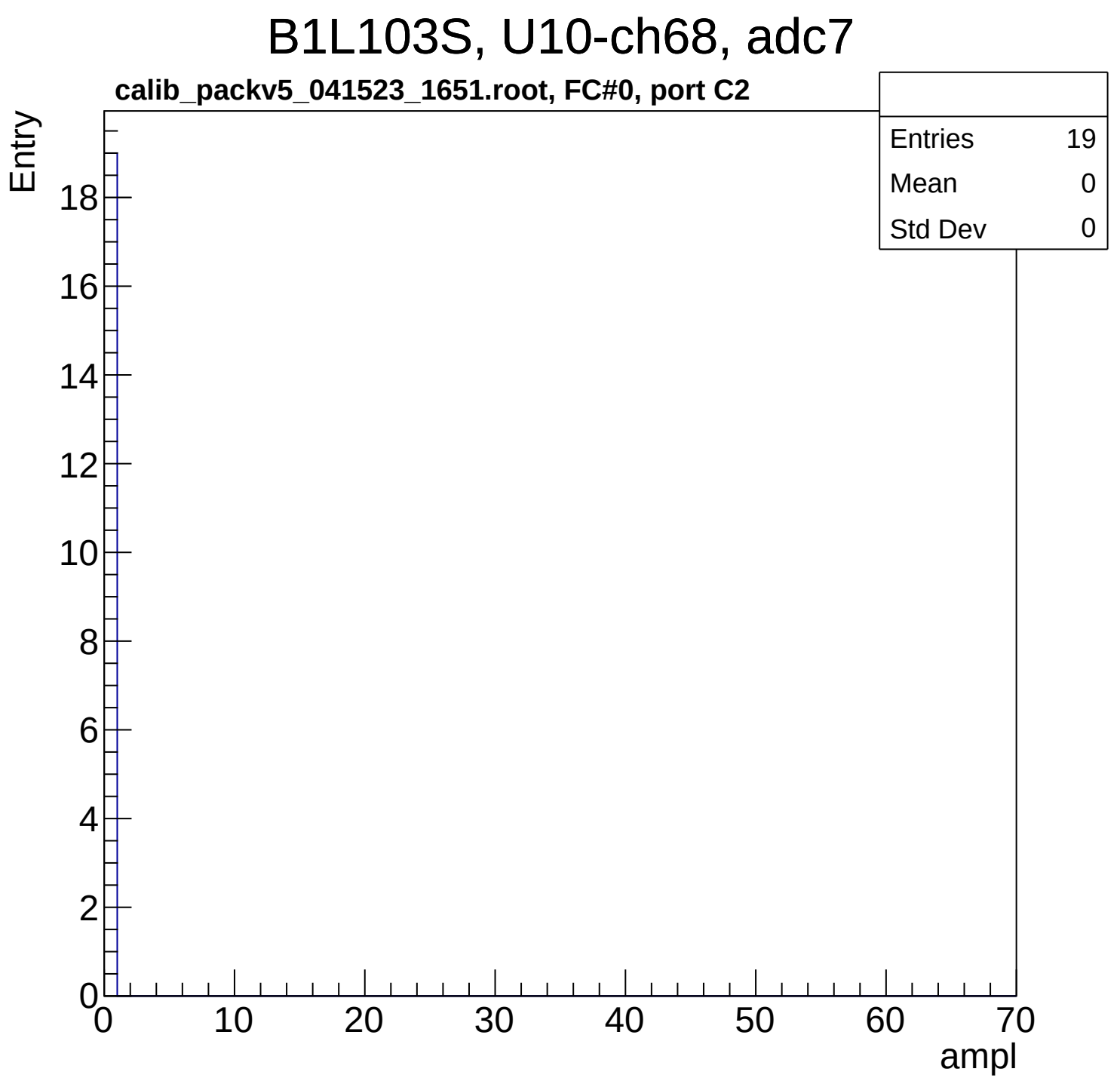
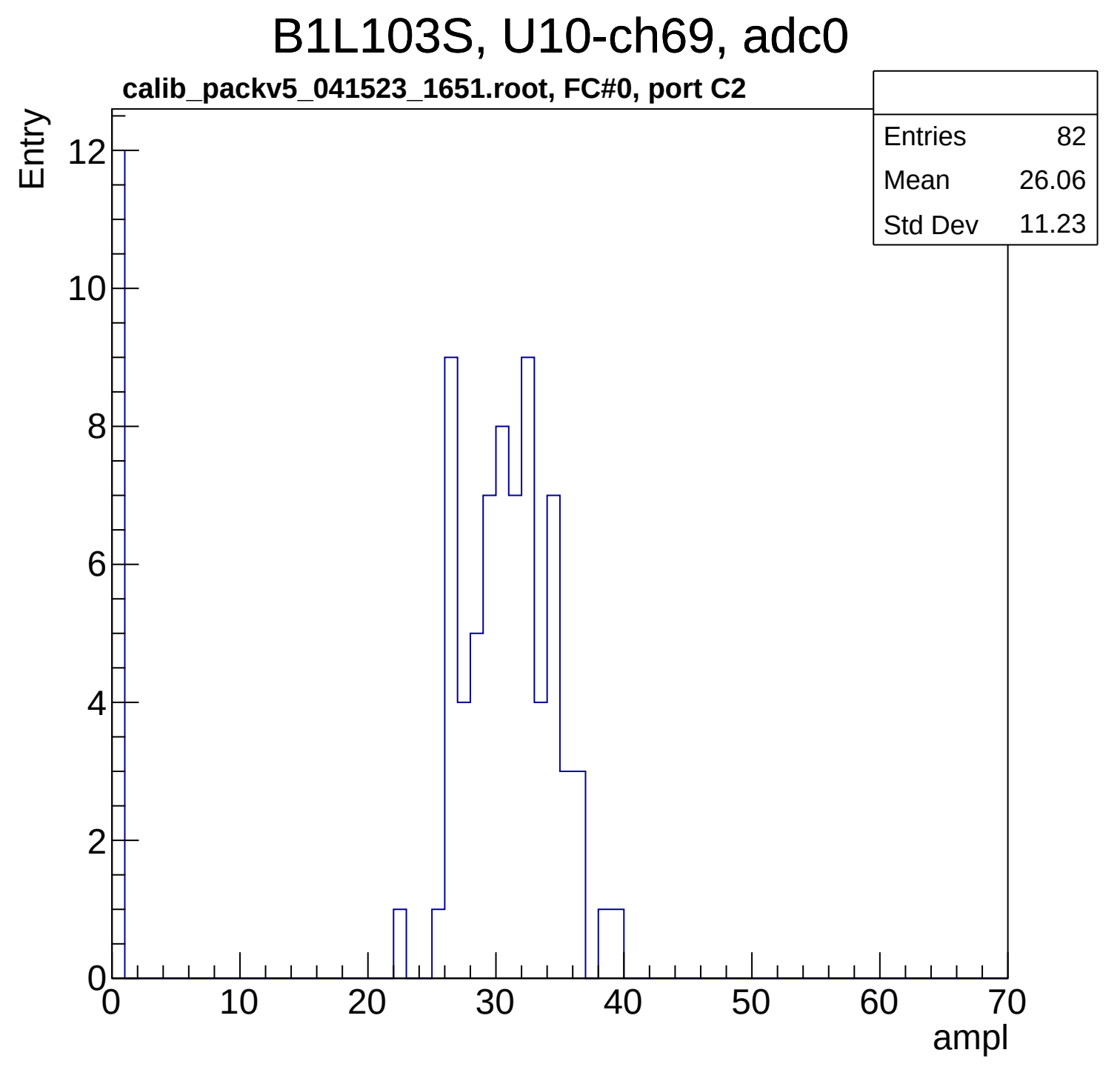
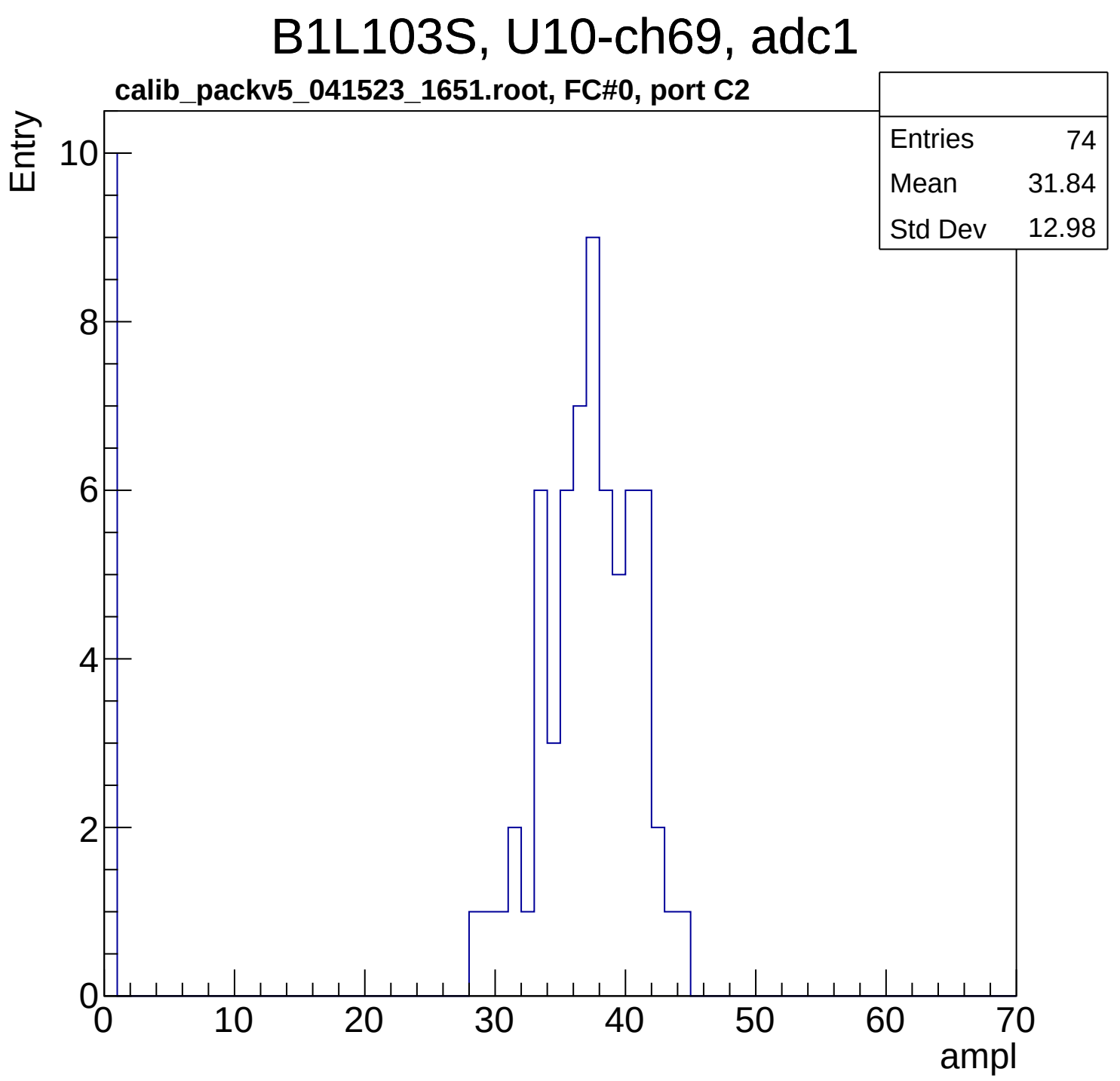
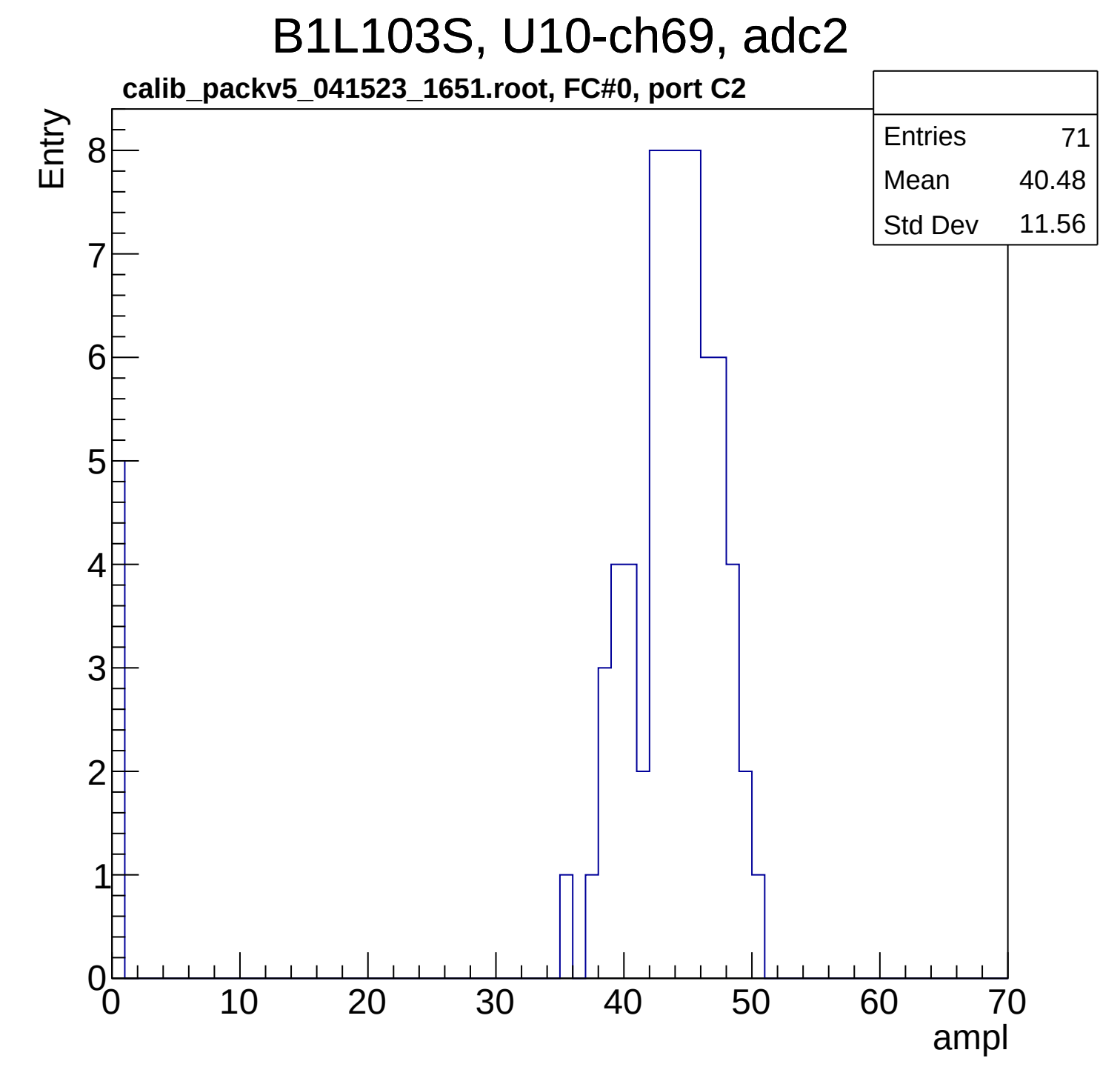
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U10-ch68, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch69, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 26.06
Std Dev 11.23
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch69, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 31.84
Std Dev 12.98
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch69, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 40.48
Std Dev 11.56
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
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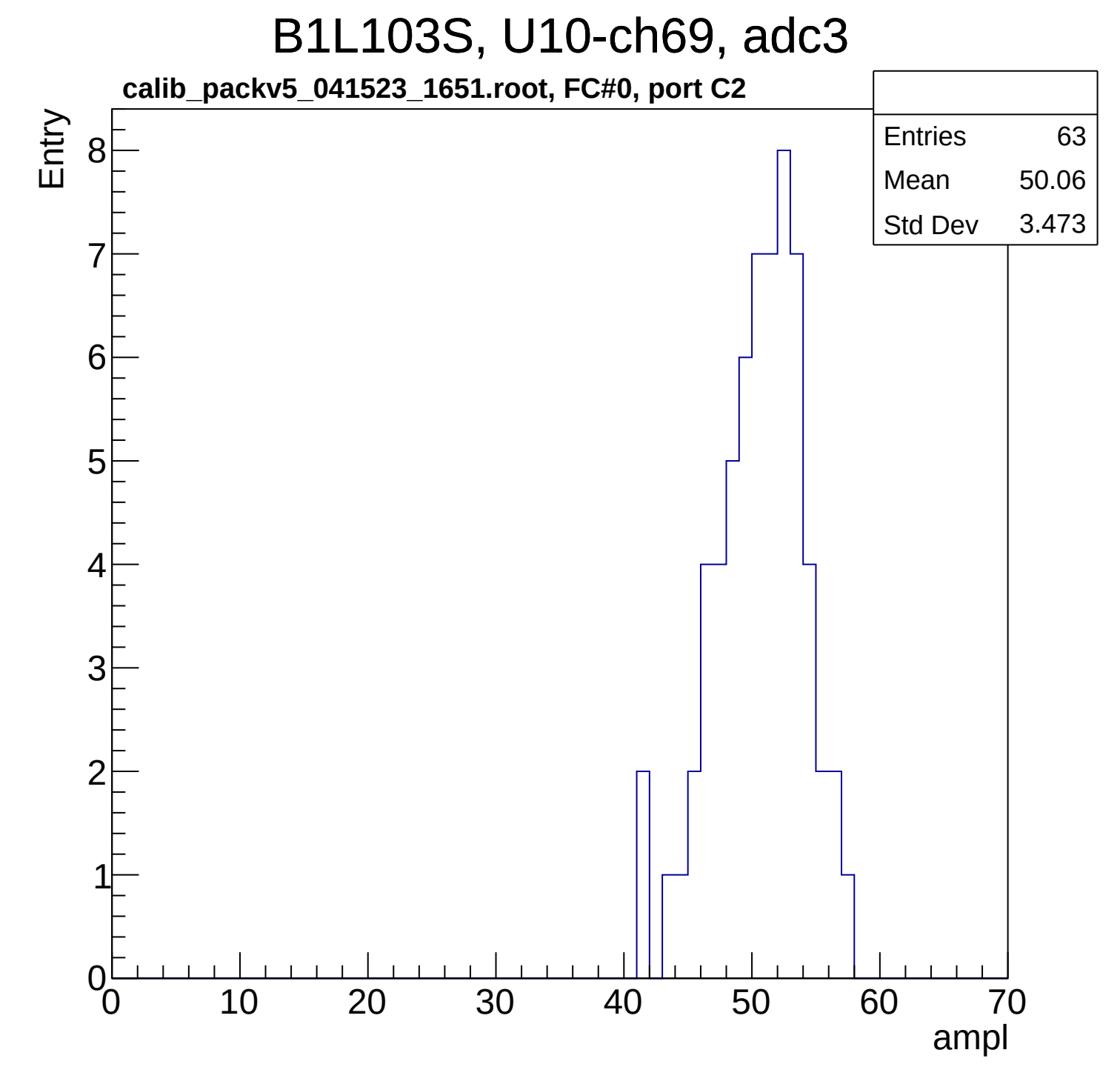
40
50
60
70


B1L103S, U10-ch69, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 50.06
Std Dev 3.473
Entry
ampl
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1
2
3
4
5
6
7
8
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10
20
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40
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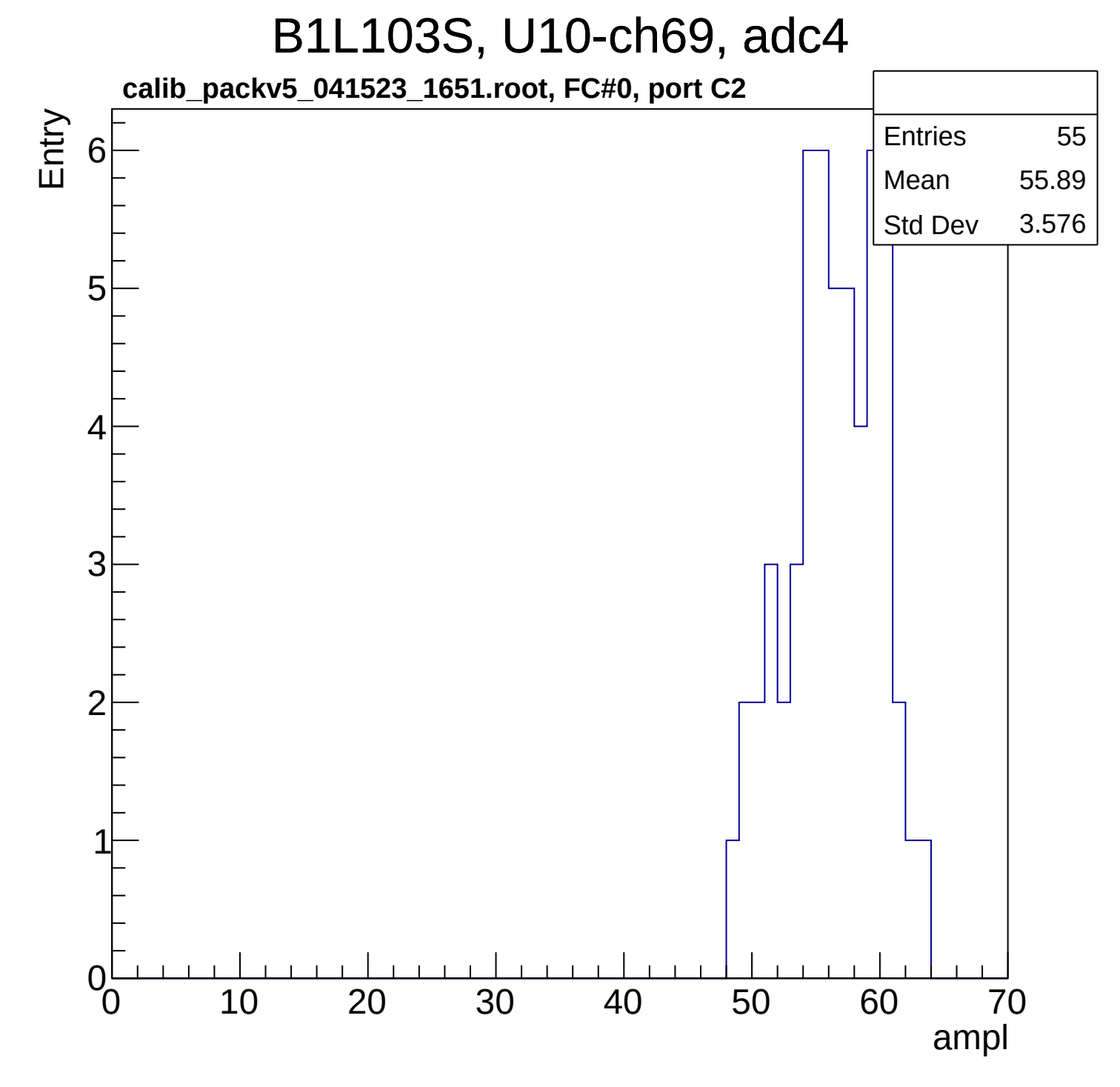
60
70


B1L103S, U10-ch69, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 55.89
Std Dev 3.576
Entry
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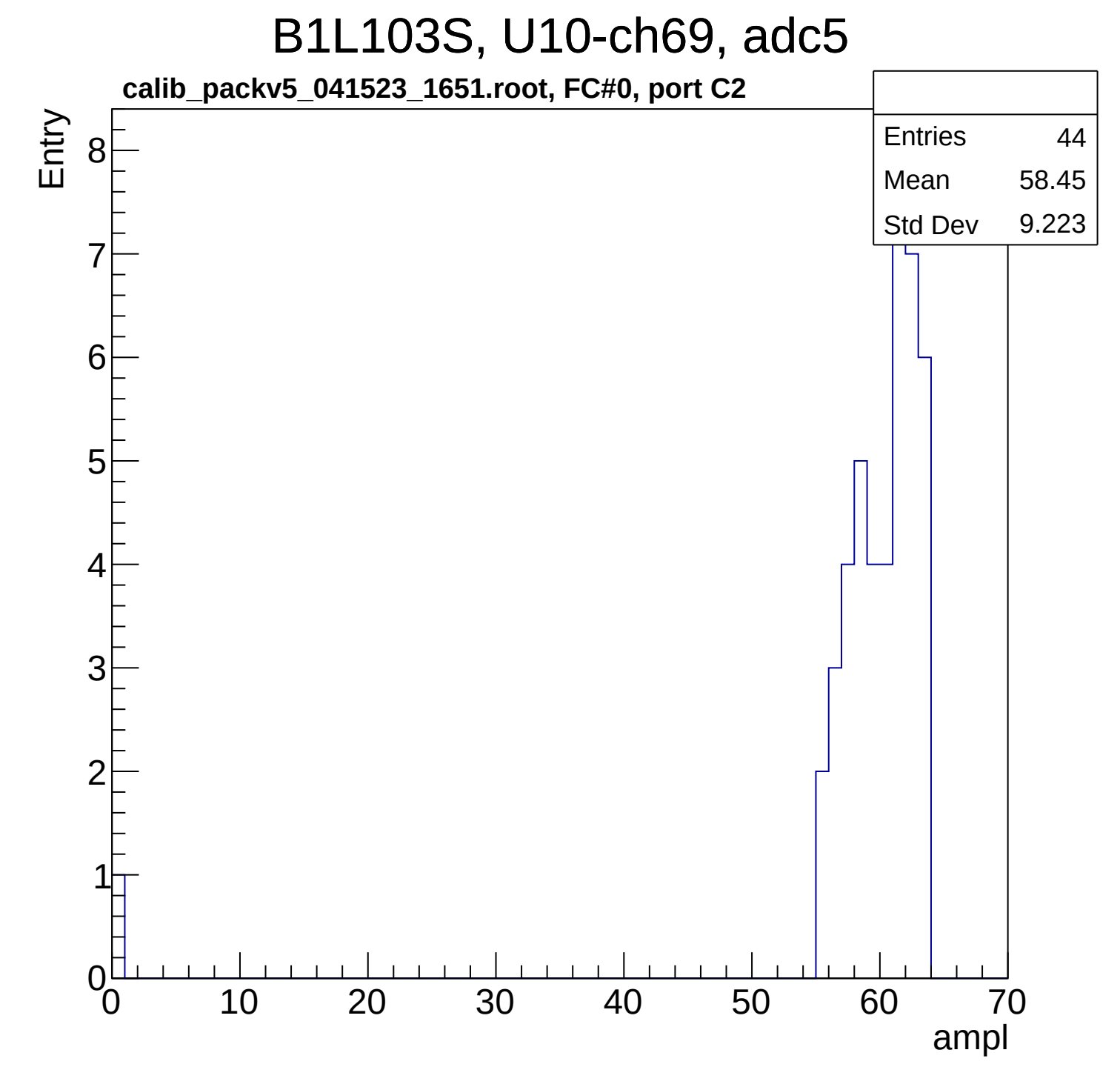
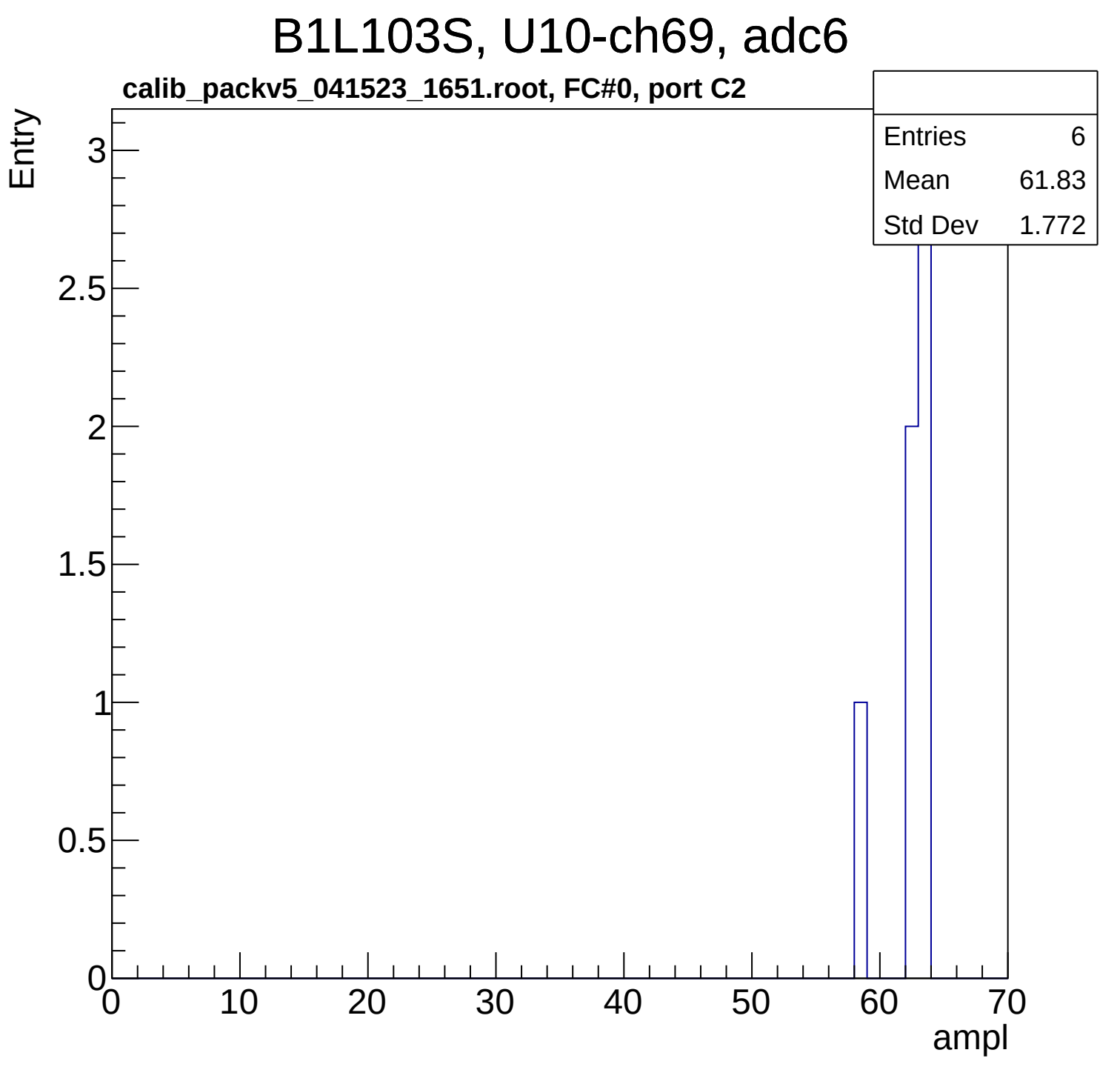
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch69, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 58.45
Std Dev 9.223
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U10-ch69, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 61.83
Std Dev 1.772
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
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40
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60
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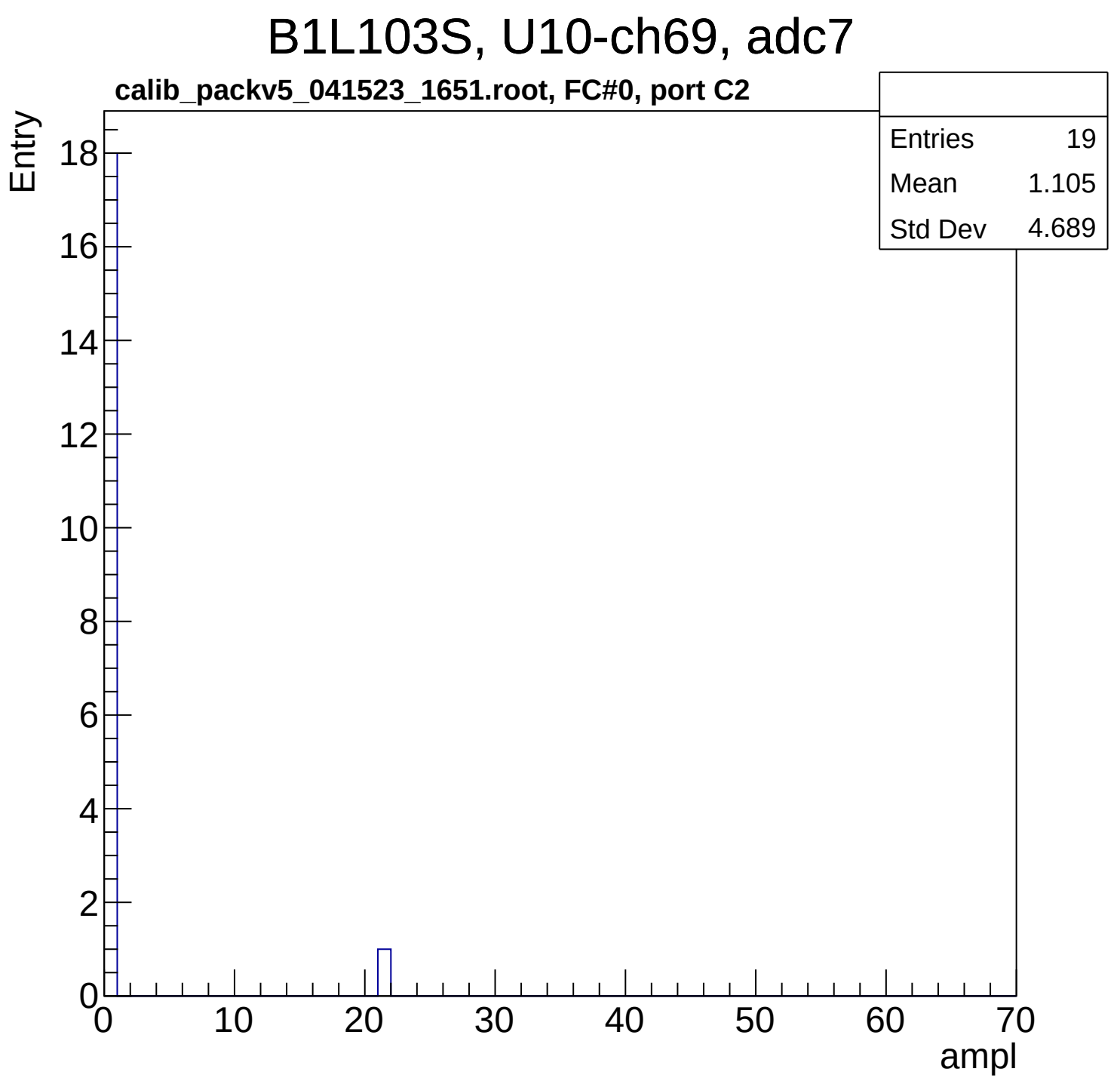
B1L103S, U10-ch69, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.105
Std Dev 4.689
Entry
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6
8
10
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14
16
18
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10
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30
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50
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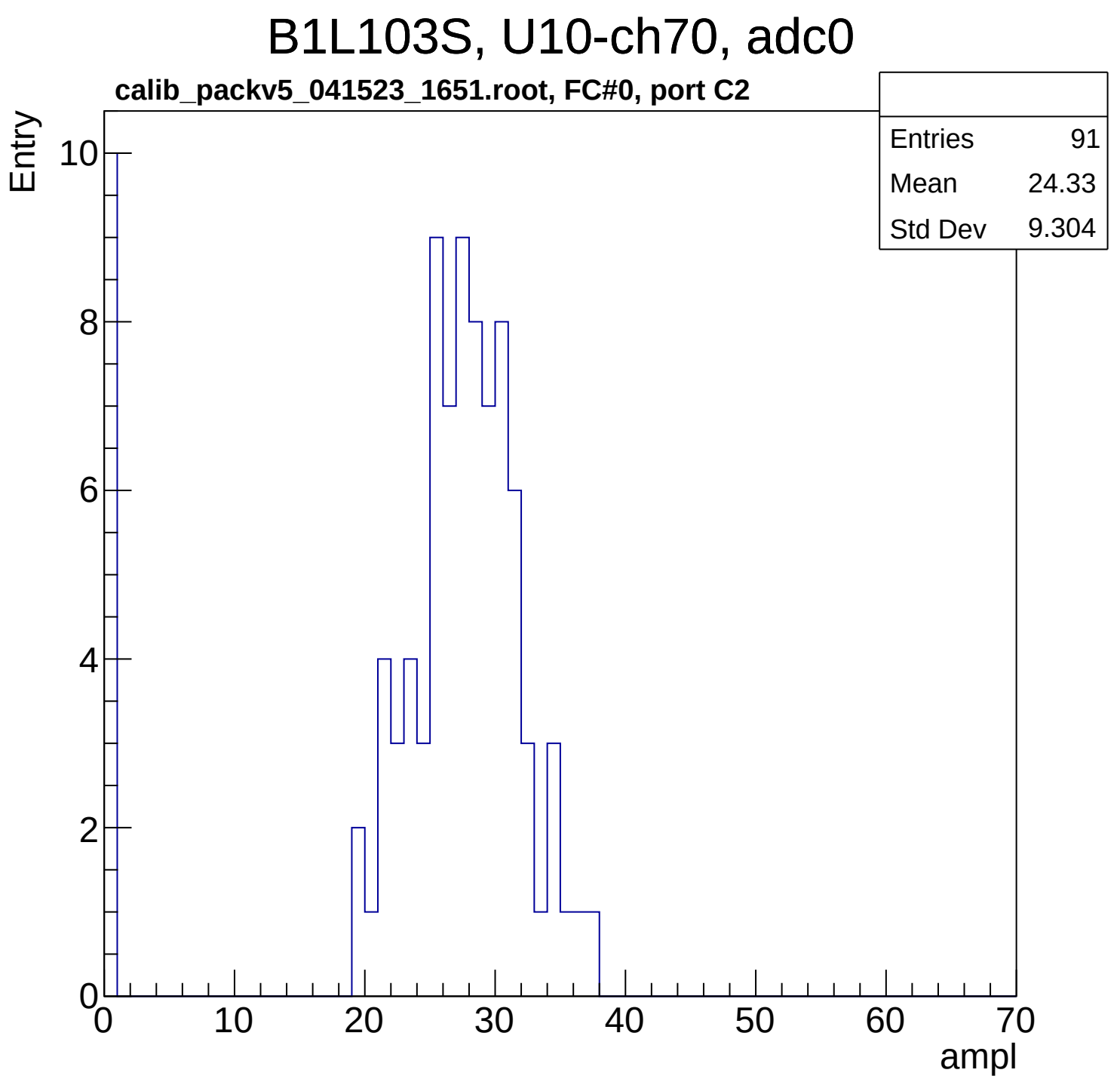
70
ampl


B1L103S, U10-ch70, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 91
Mean 24.33
Std Dev 9.304
Entry
ampl
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2
4
6
8
10
0
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40
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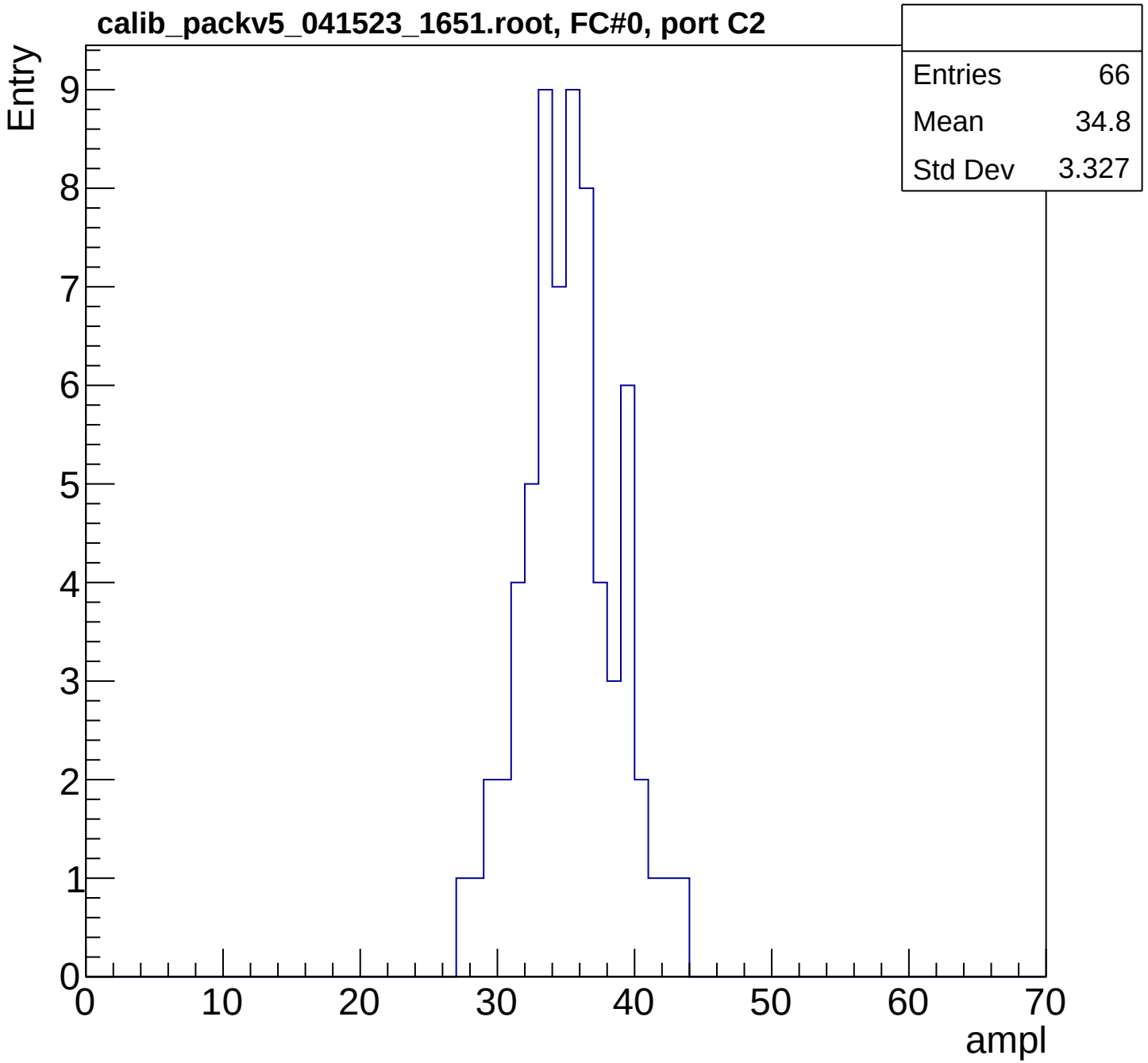
B1L103S, U10-ch70, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 34.8
Std Dev 3.327
Entry
ampl
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3
4
5
6
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0
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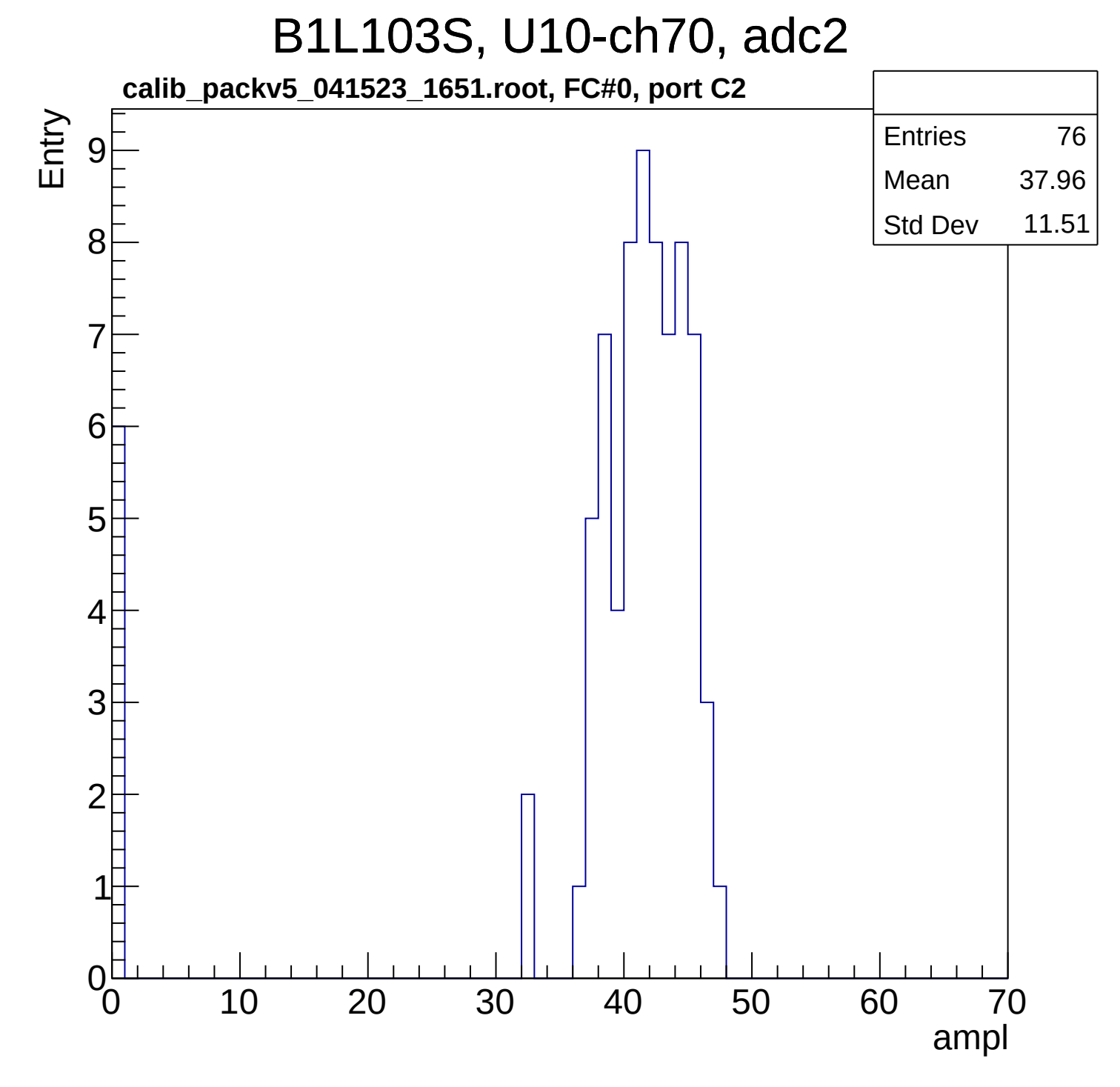
B1L103S, U10-ch70, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 37.96
Std Dev 11.51
Entry
ampl
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2
3
4
5
6
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8
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0
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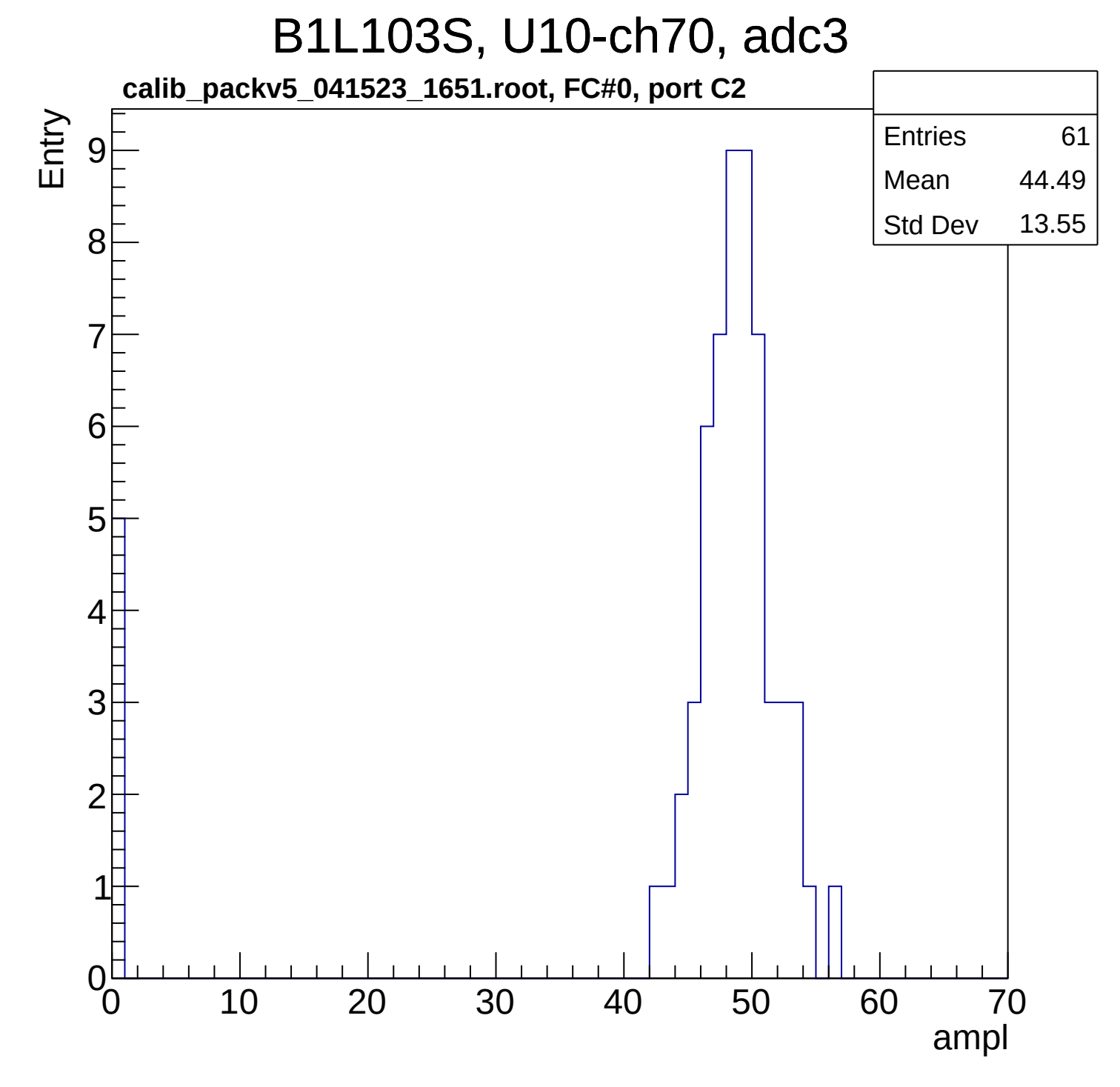
B1L103S, U10-ch70, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 44.49
Std Dev 13.55
Entry
ampl
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2
3
4
5
6
7
8
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0
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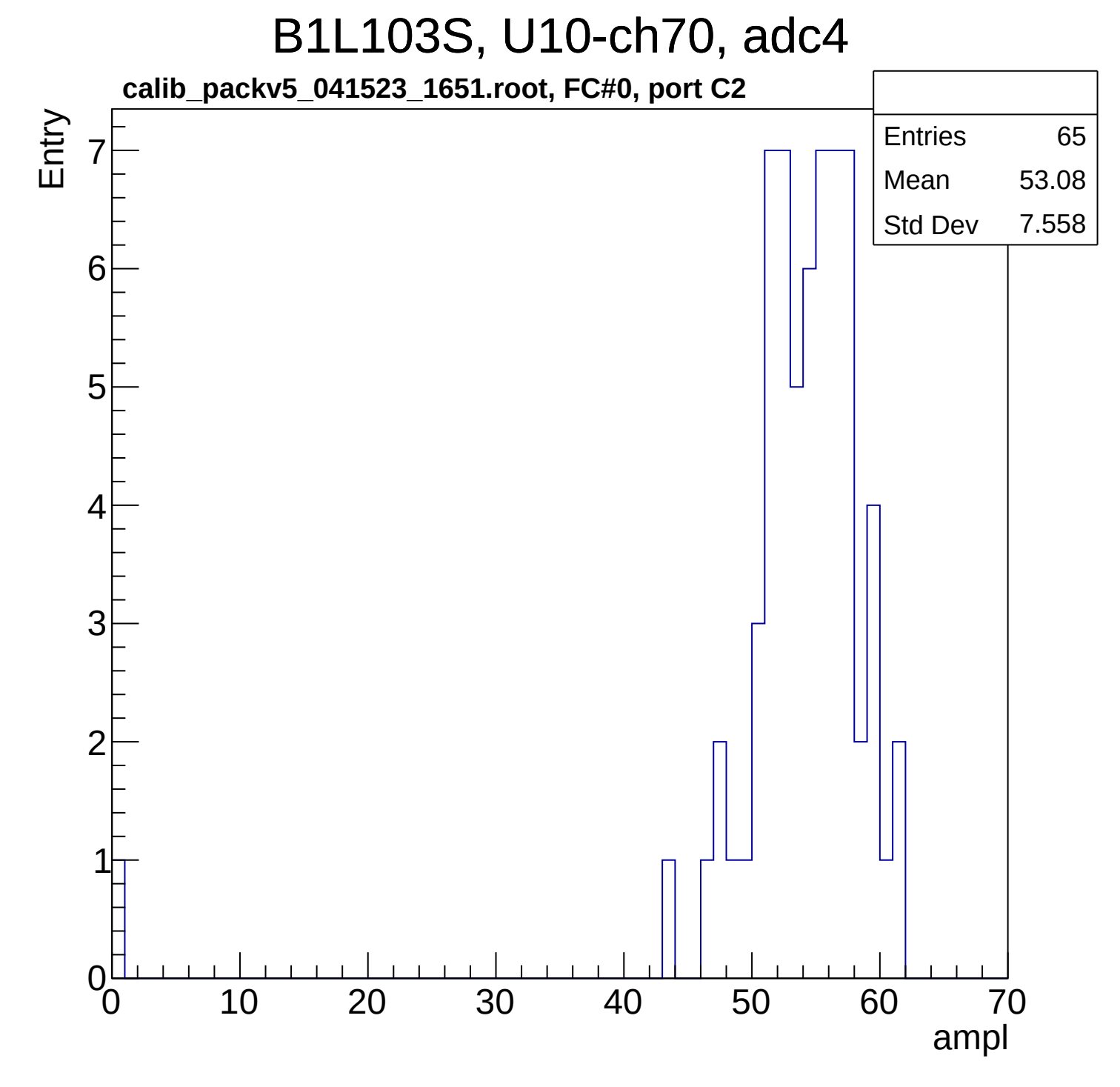
B1L103S, U10-ch70, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 53.08
Std Dev 7.558
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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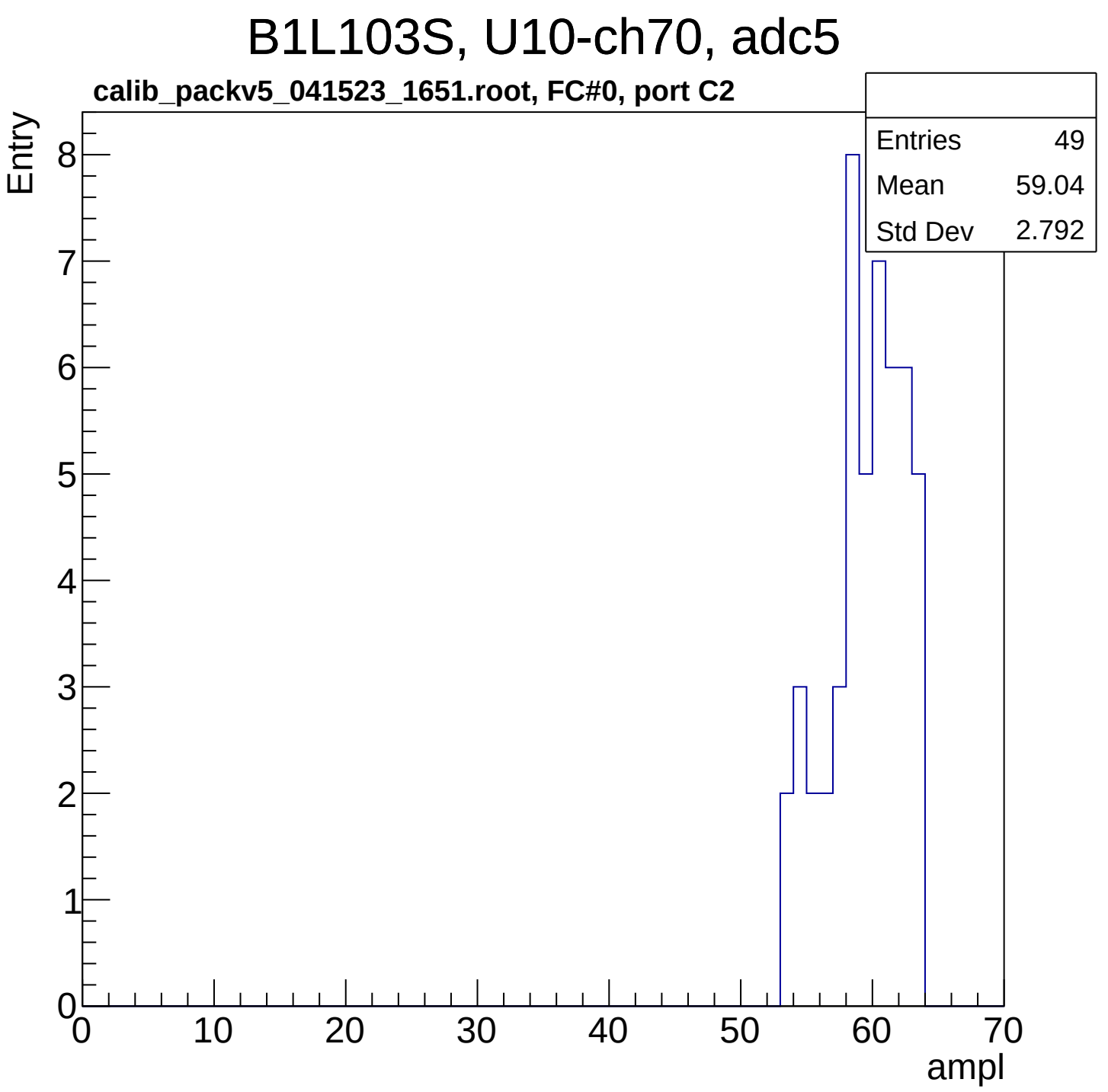
B1L103S, U10-ch70, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 59.04
Std Dev 2.792
Entry
ampl
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2
3
4
5
6
7
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0
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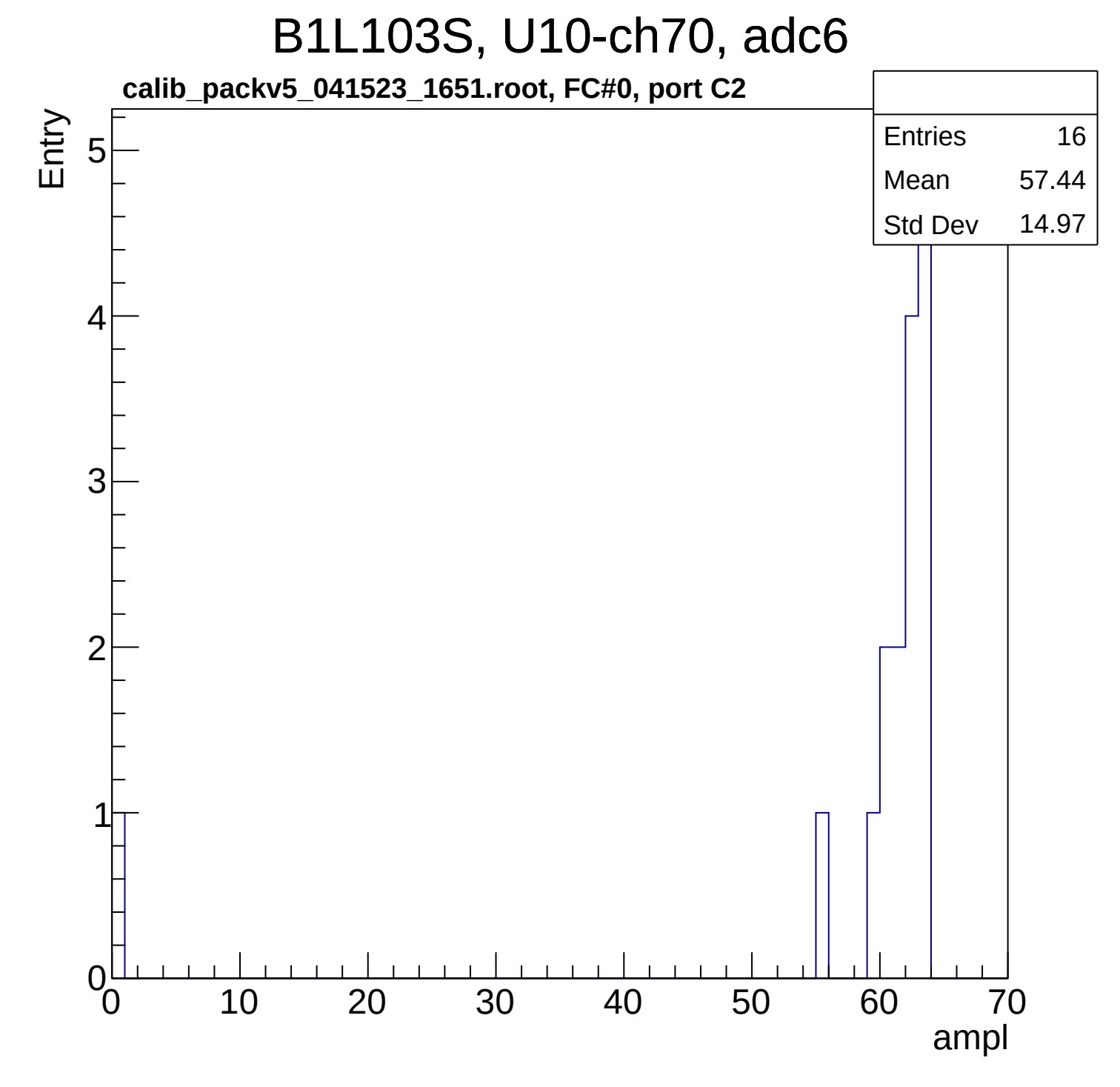
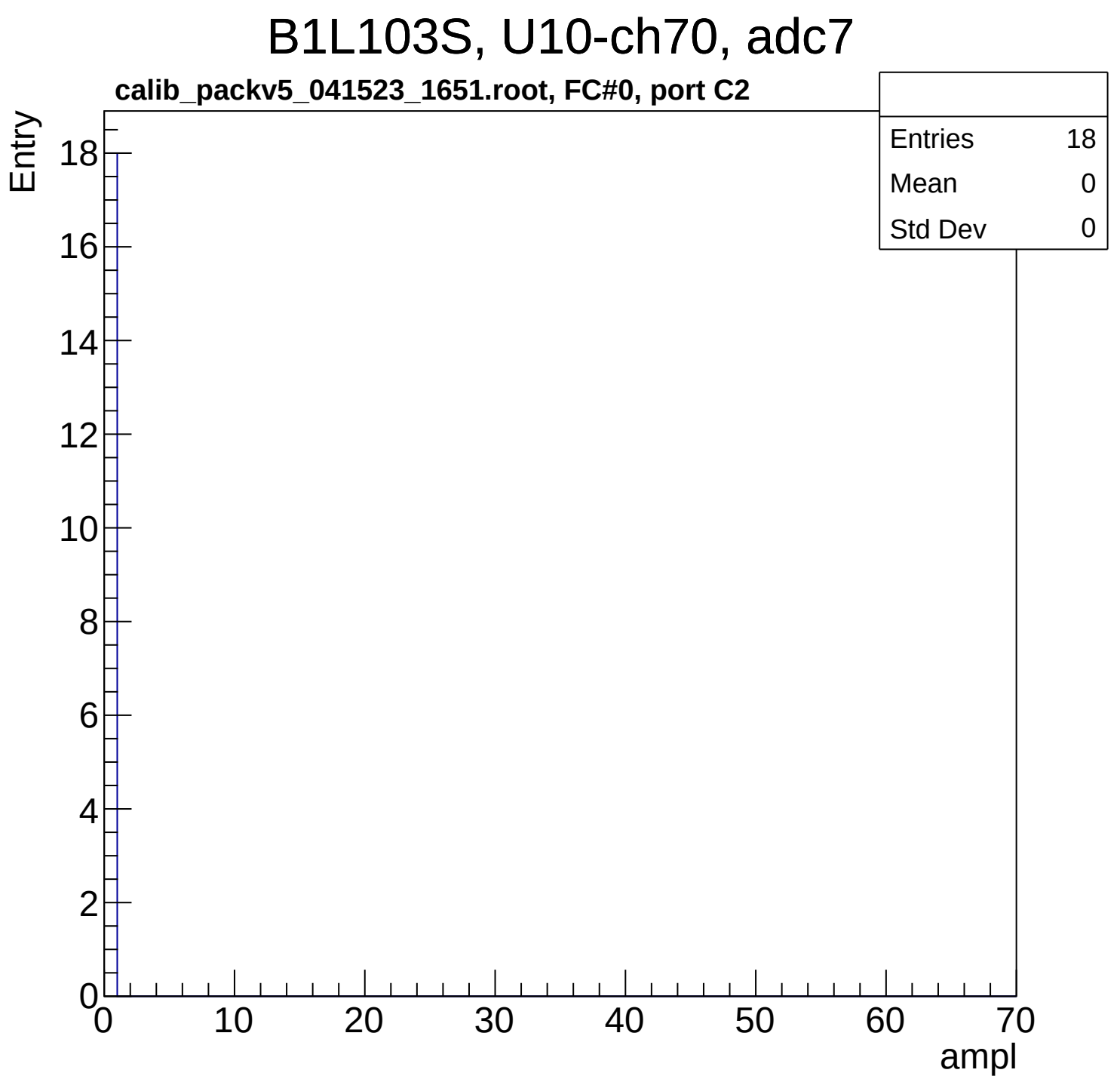
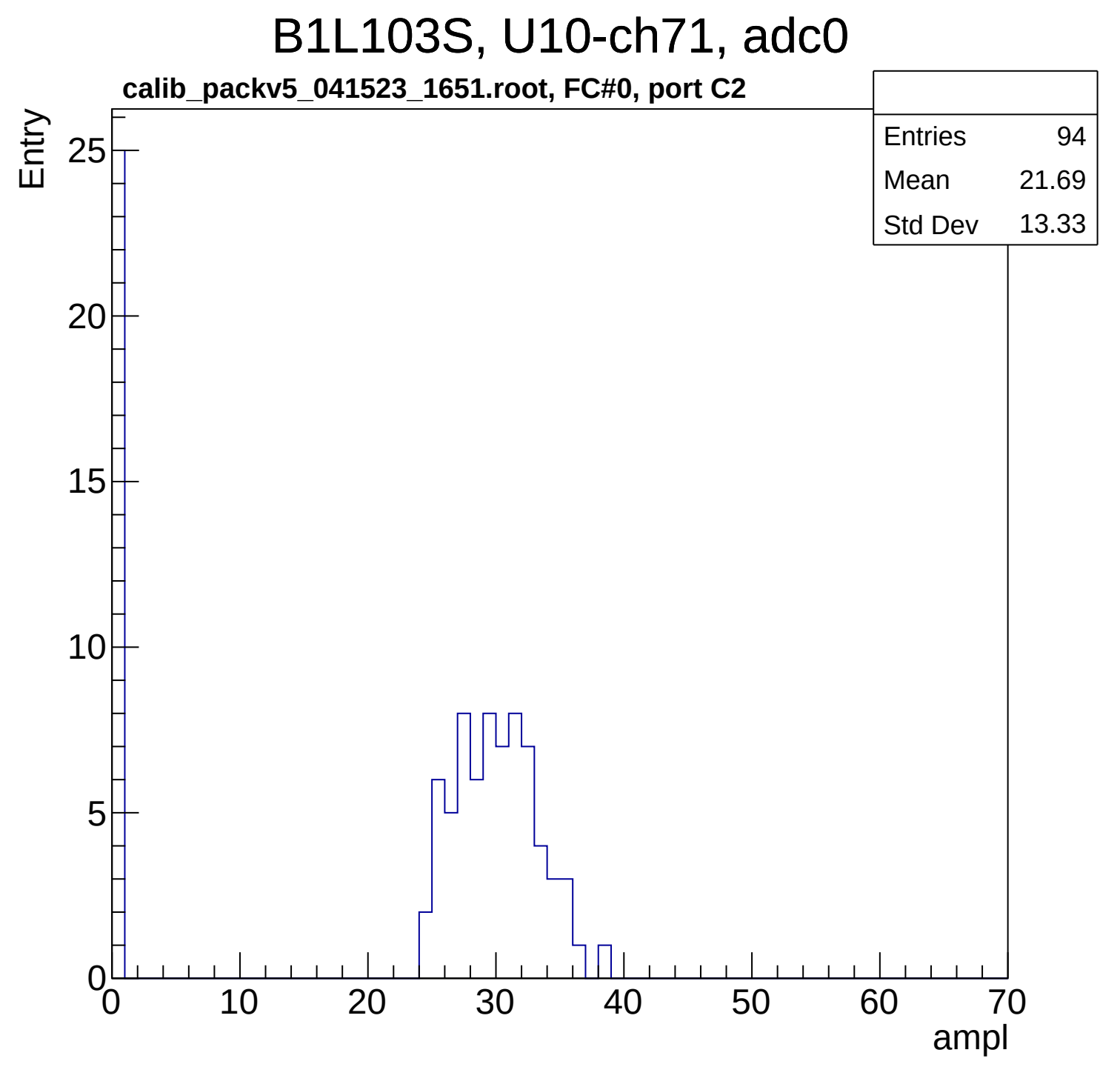
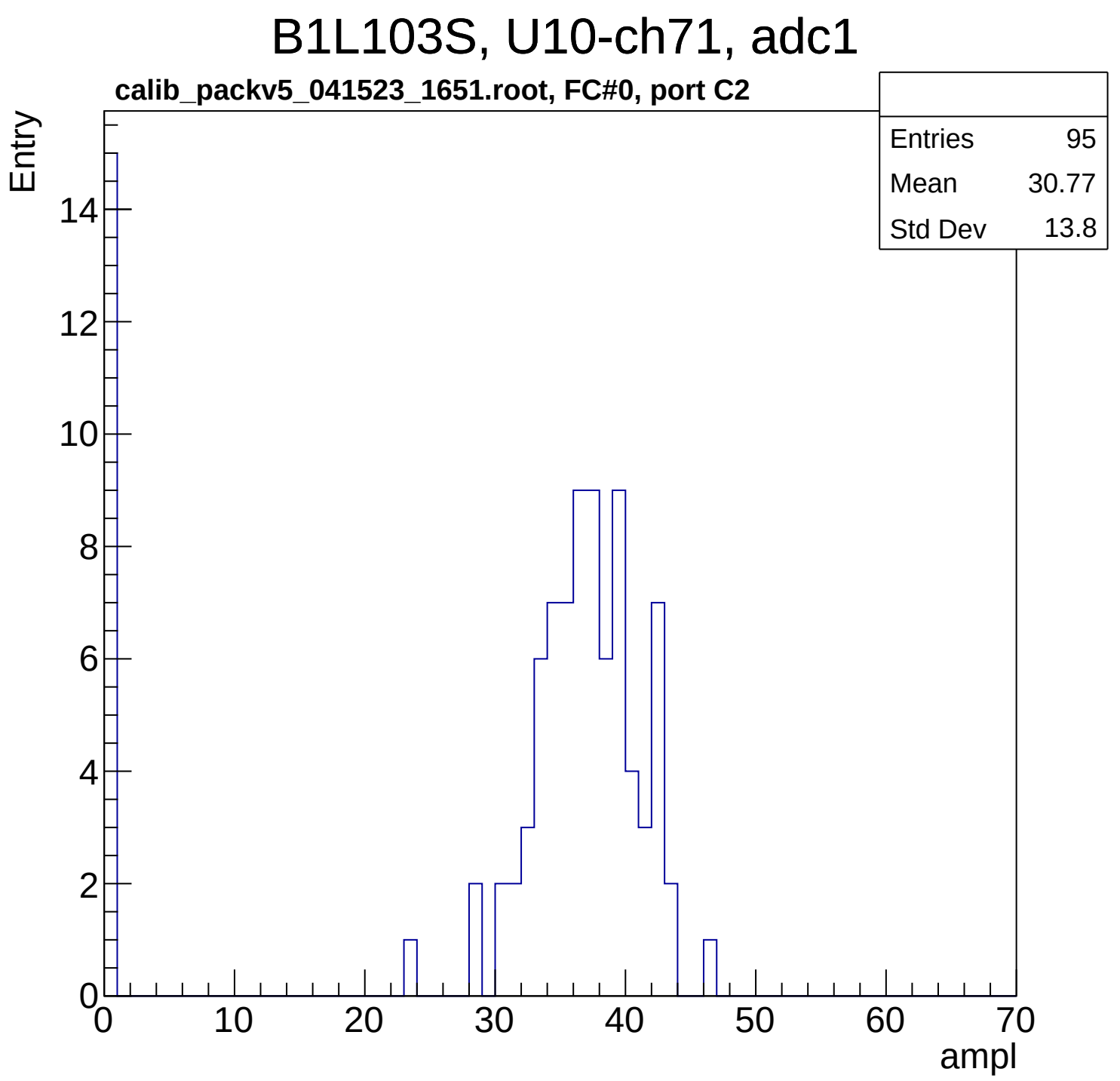

B1L103S, U10-ch70, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 16
Mean 57.44
Std Dev 14.97
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U10-ch70, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch71, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 94
Mean 21.69
Std Dev 13.33
Entry
0
5
10
15
20
25
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch71, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 95
Mean 30.77
Std Dev 13.8
Entry
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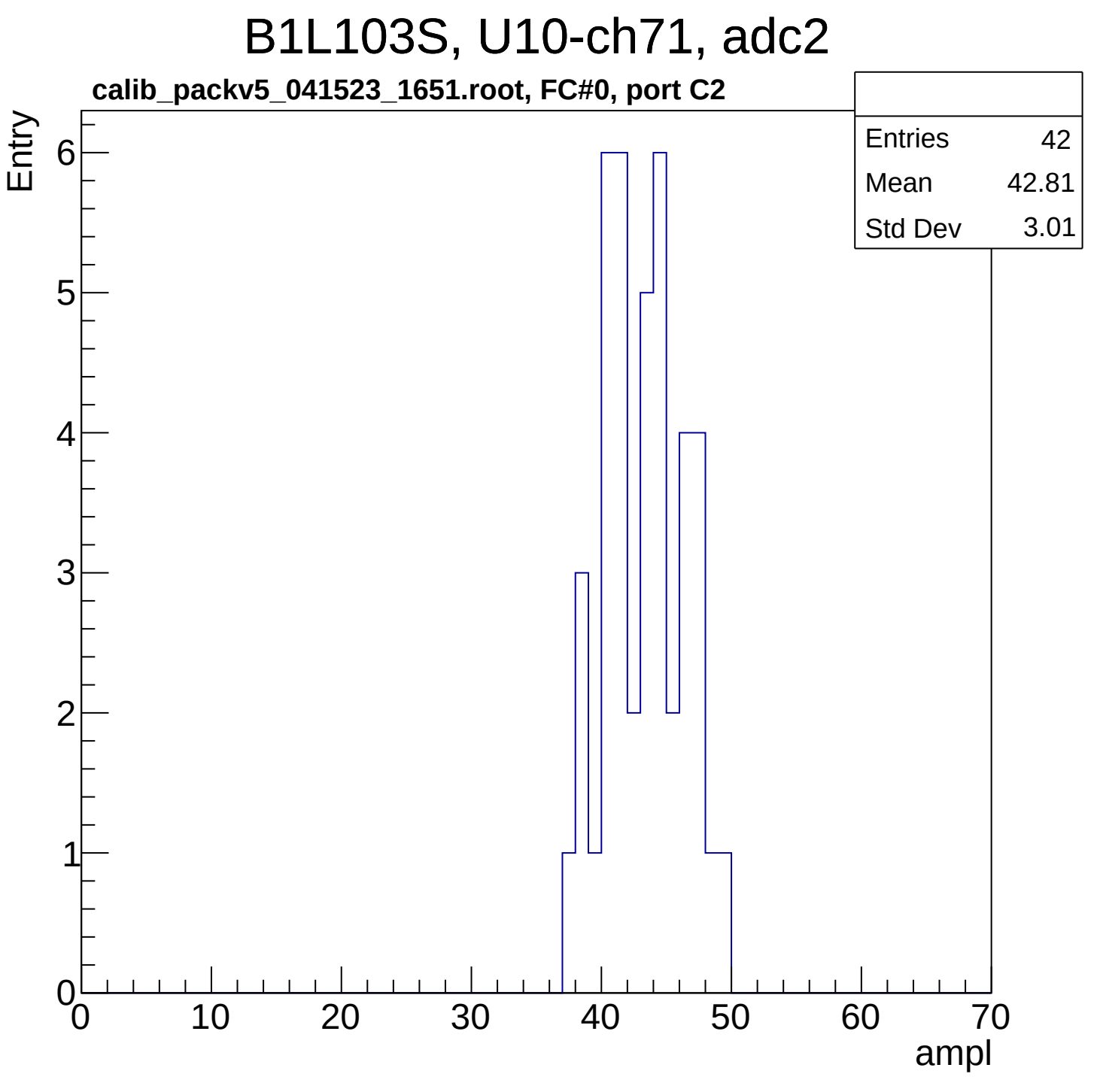
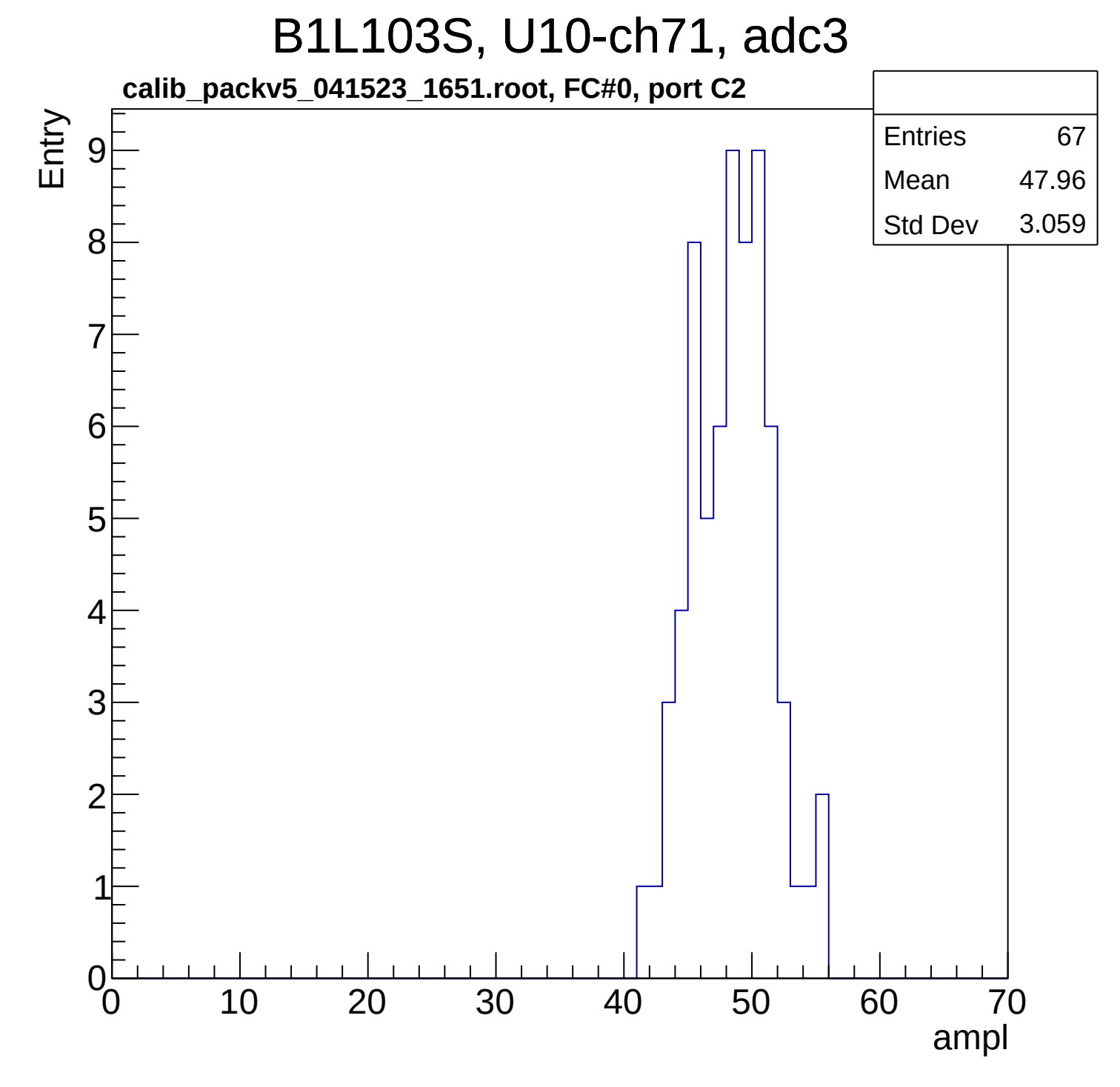
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch71, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 42
Mean 42.81
Std Dev 3.01
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch71, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 47.96
Std Dev 3.059
Entry
ampl
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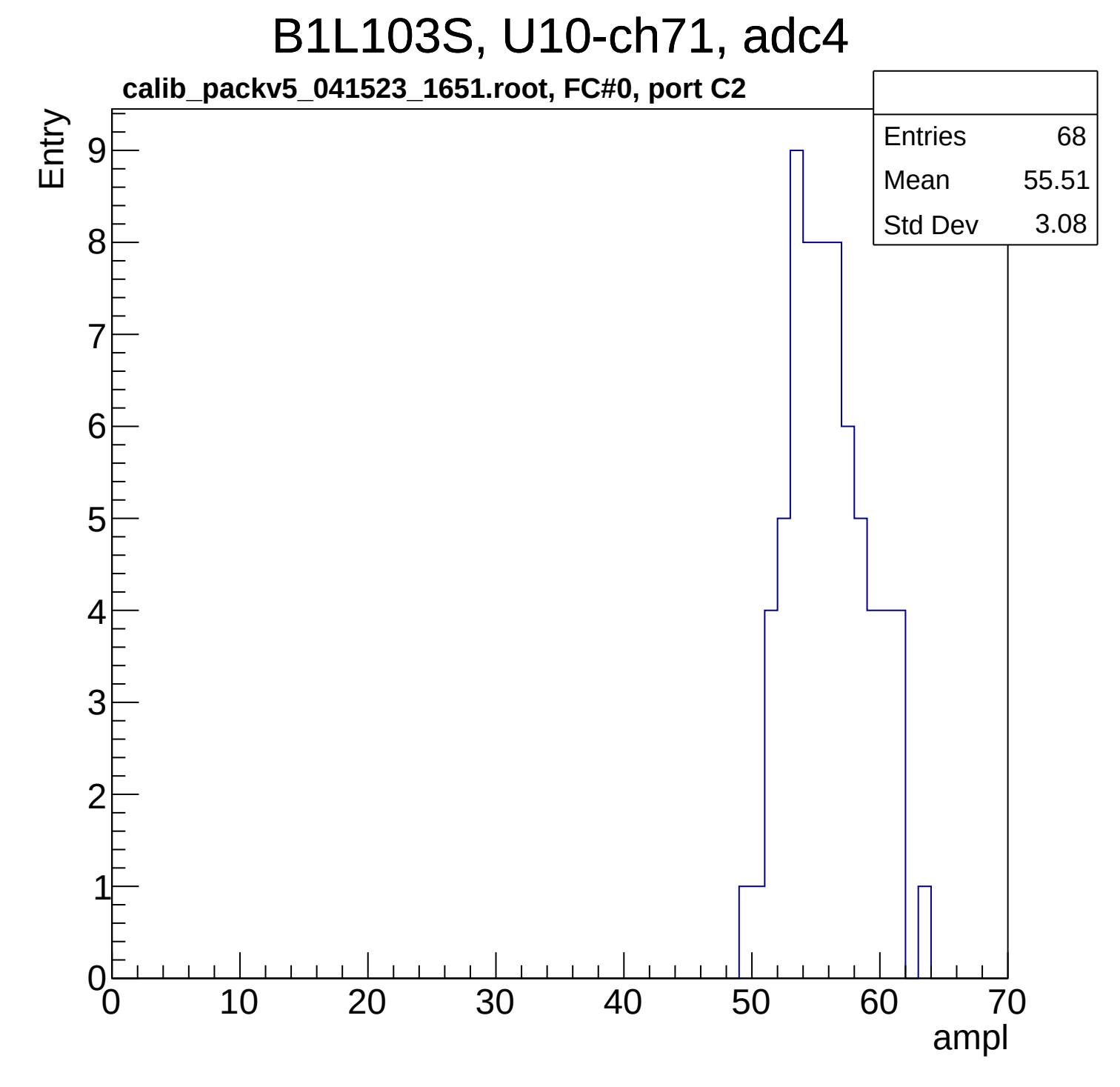
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U10-ch71, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 55.51
Std Dev 3.08
Entry
ampl
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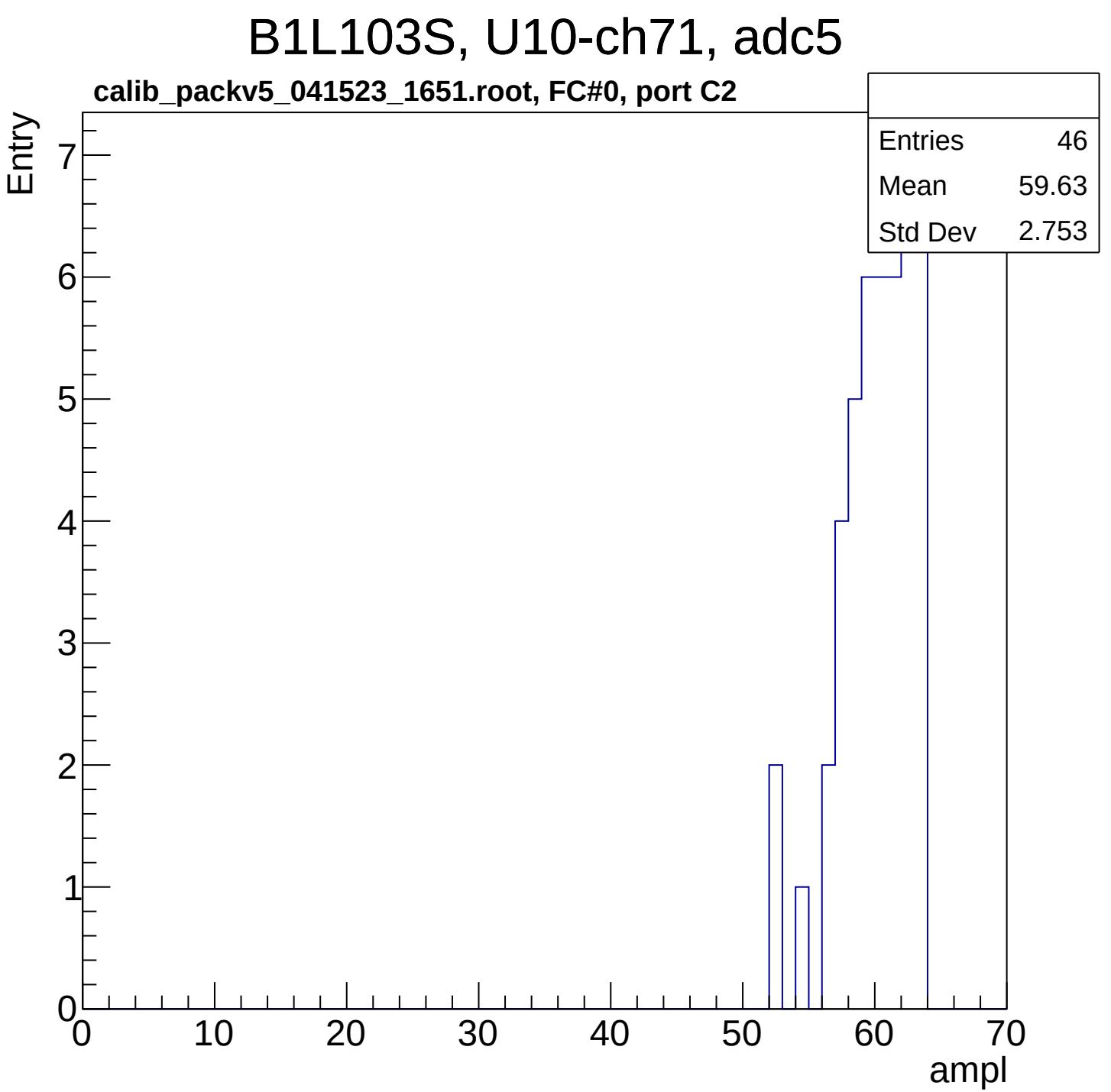
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U10-ch71, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 59.63
Std Dev 2.753
Entry
ampl
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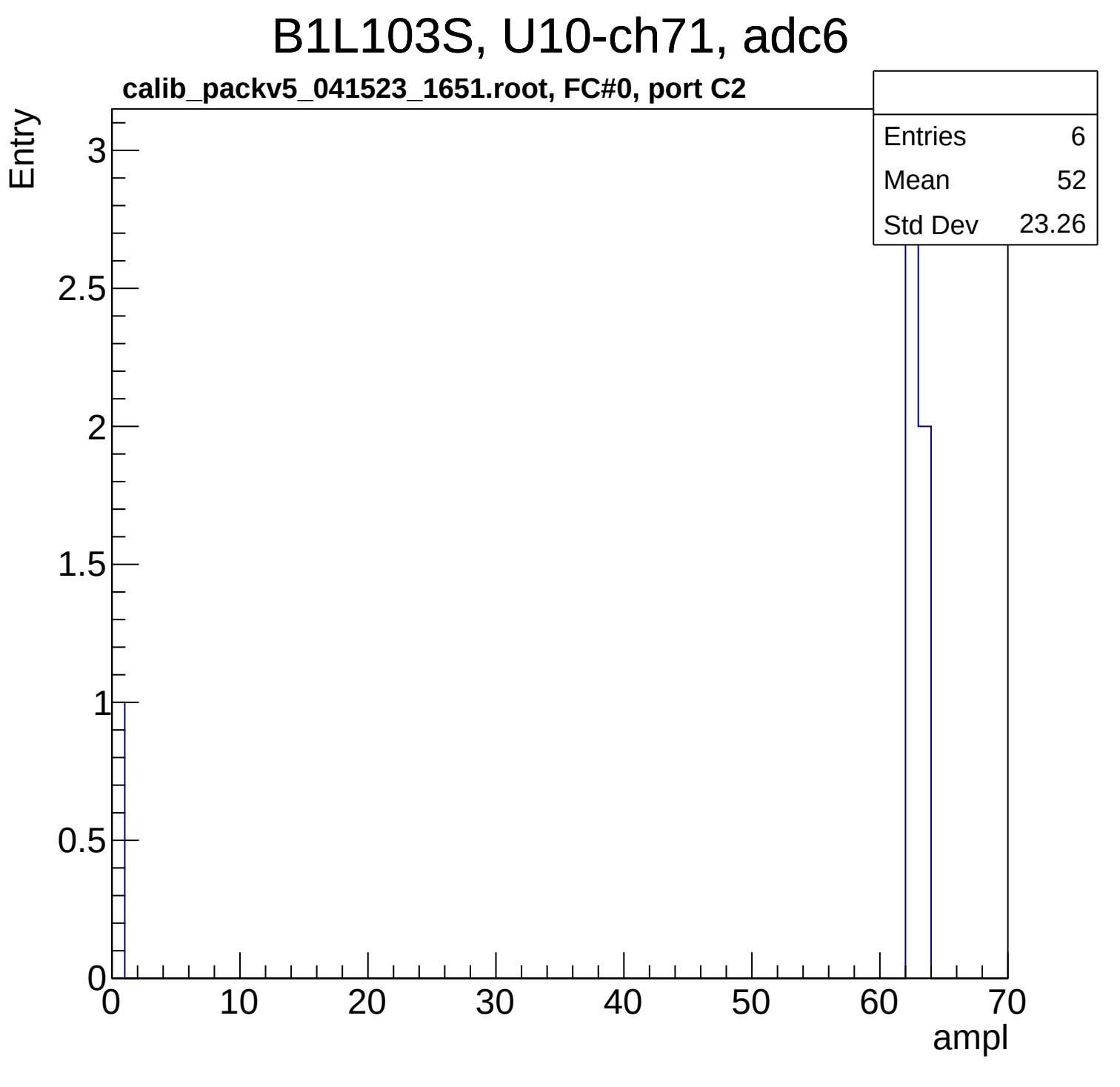
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U10-ch71, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 52
Std Dev 23.26
Entry
ampl
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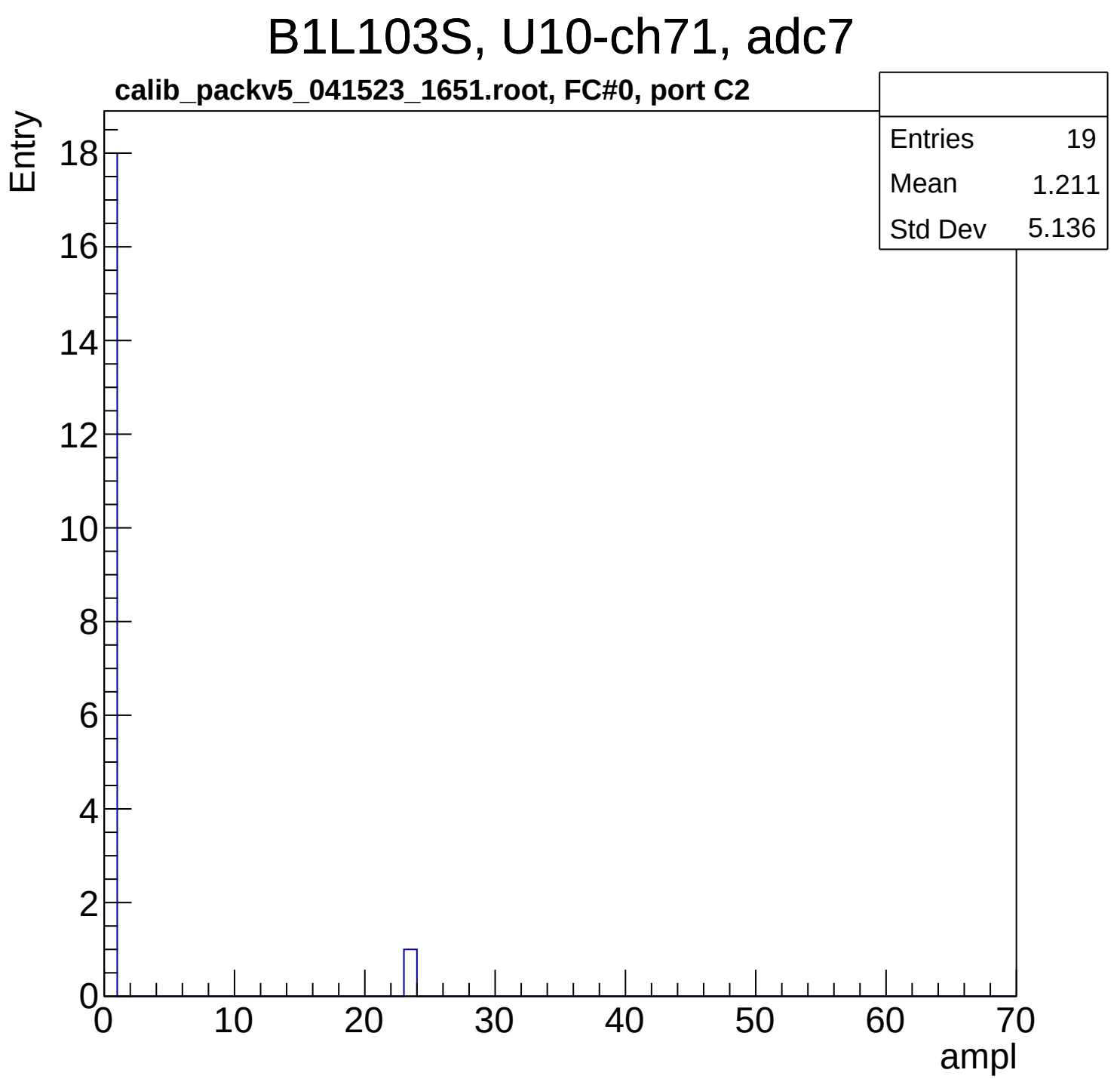
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U10-ch71, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.211
Std Dev 5.136
Entry
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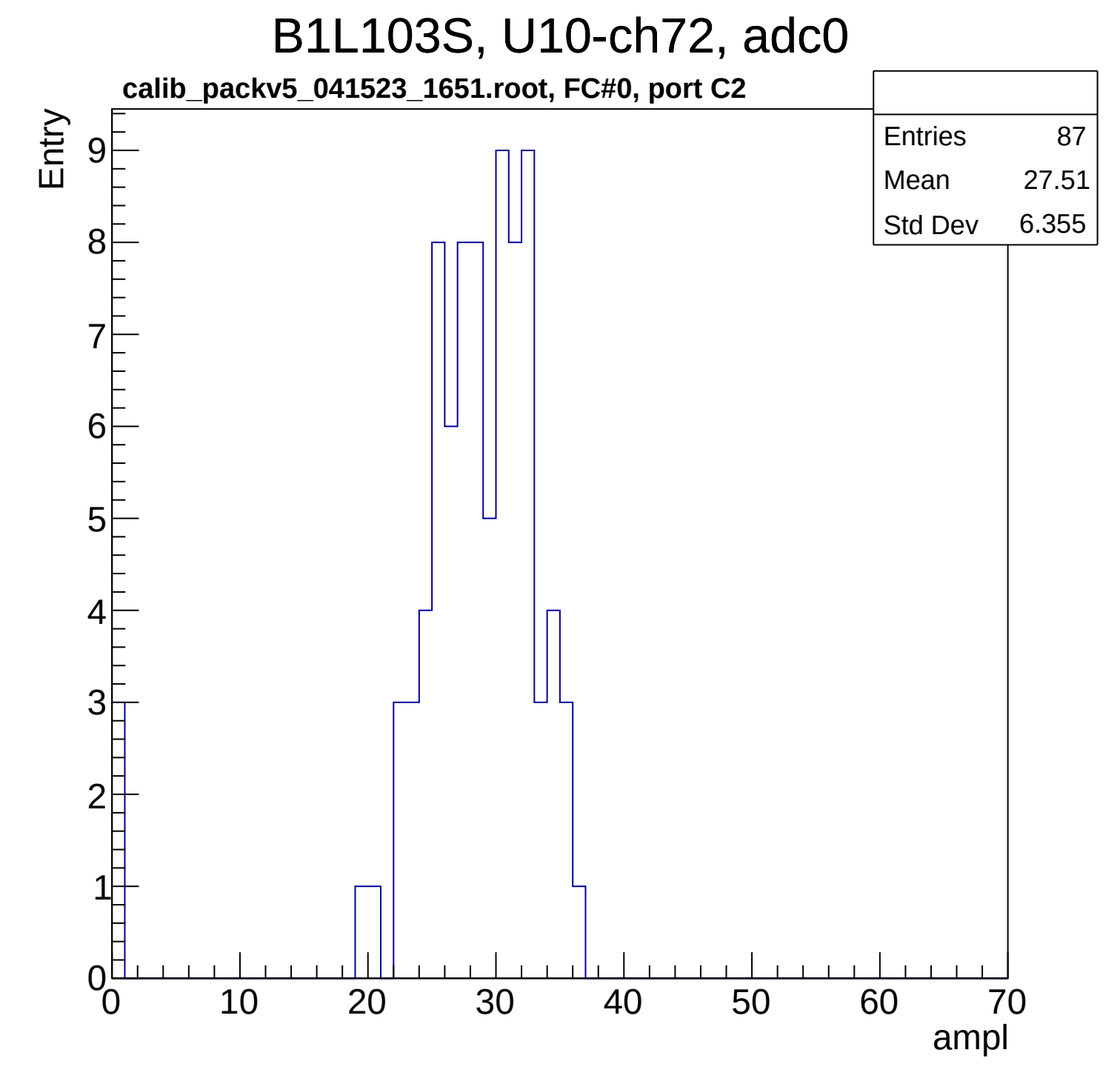
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch72, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 87
Mean 27.51
Std Dev 6.355
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
50
60
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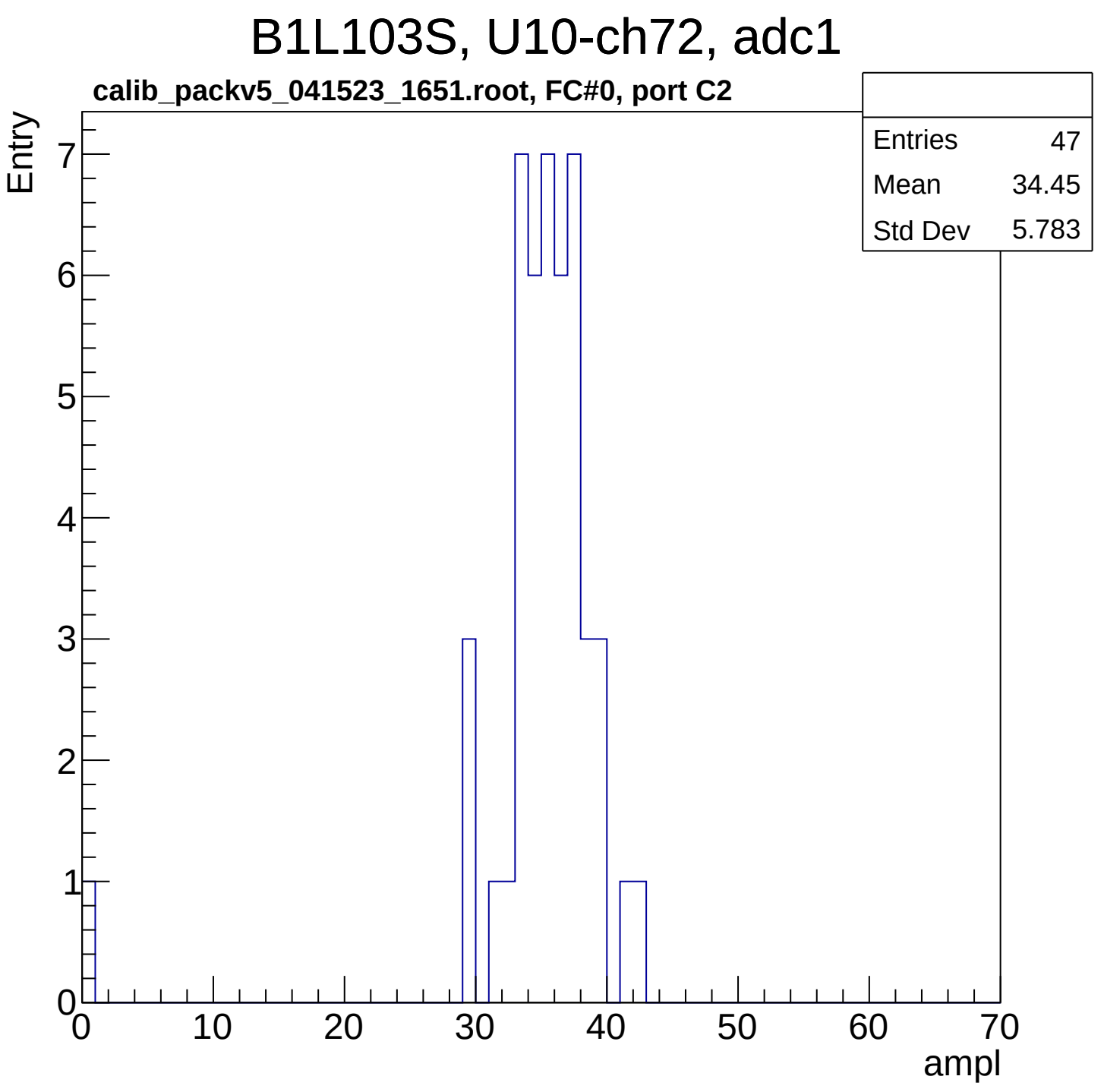
B1L103S, U10-ch72, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 34.45
Std Dev 5.783
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
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40
50
60
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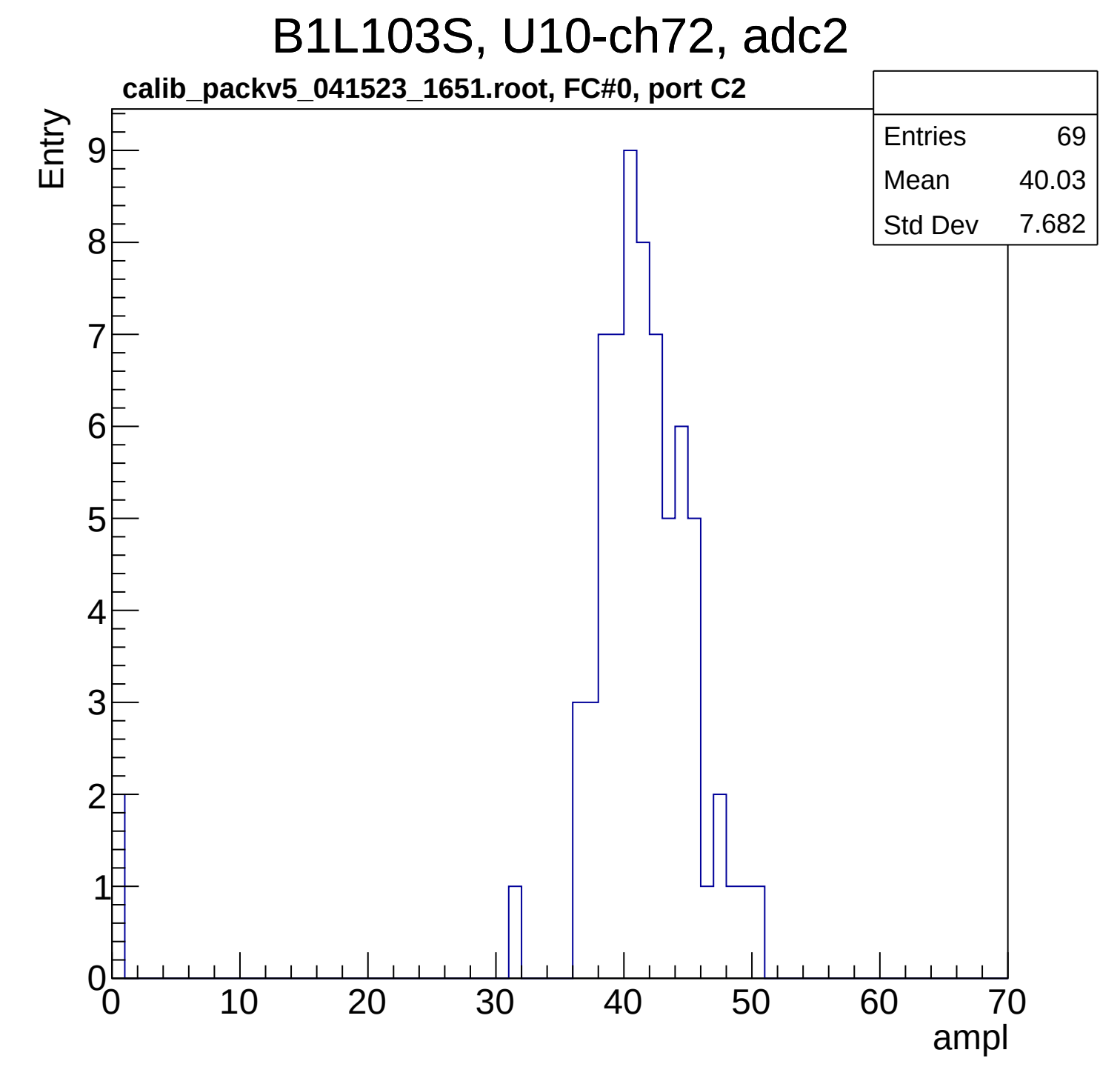
B1L103S, U10-ch72, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 40.03
Std Dev 7.682
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
50
60
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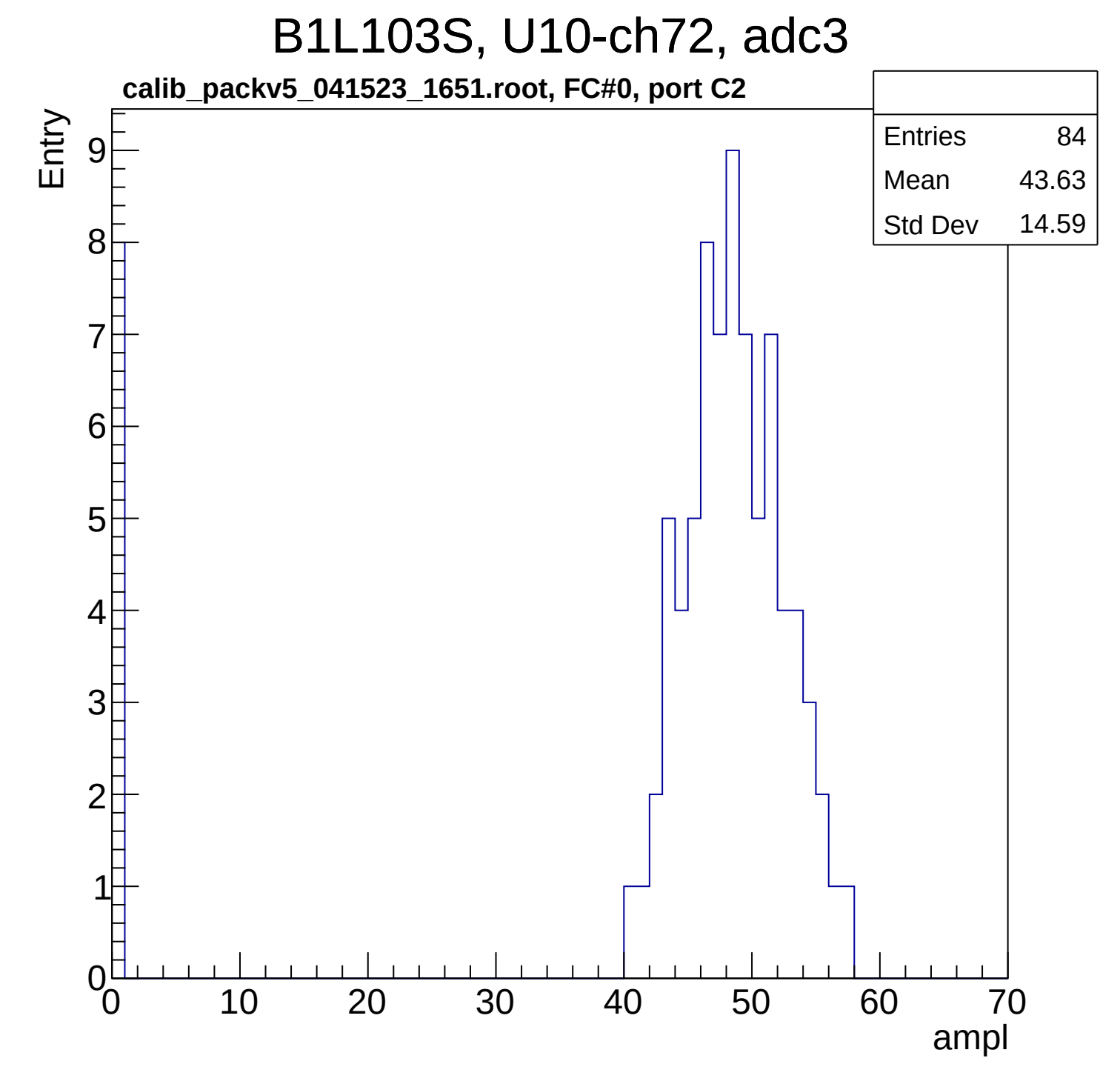
B1L103S, U10-ch72, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 43.63
Std Dev 14.59
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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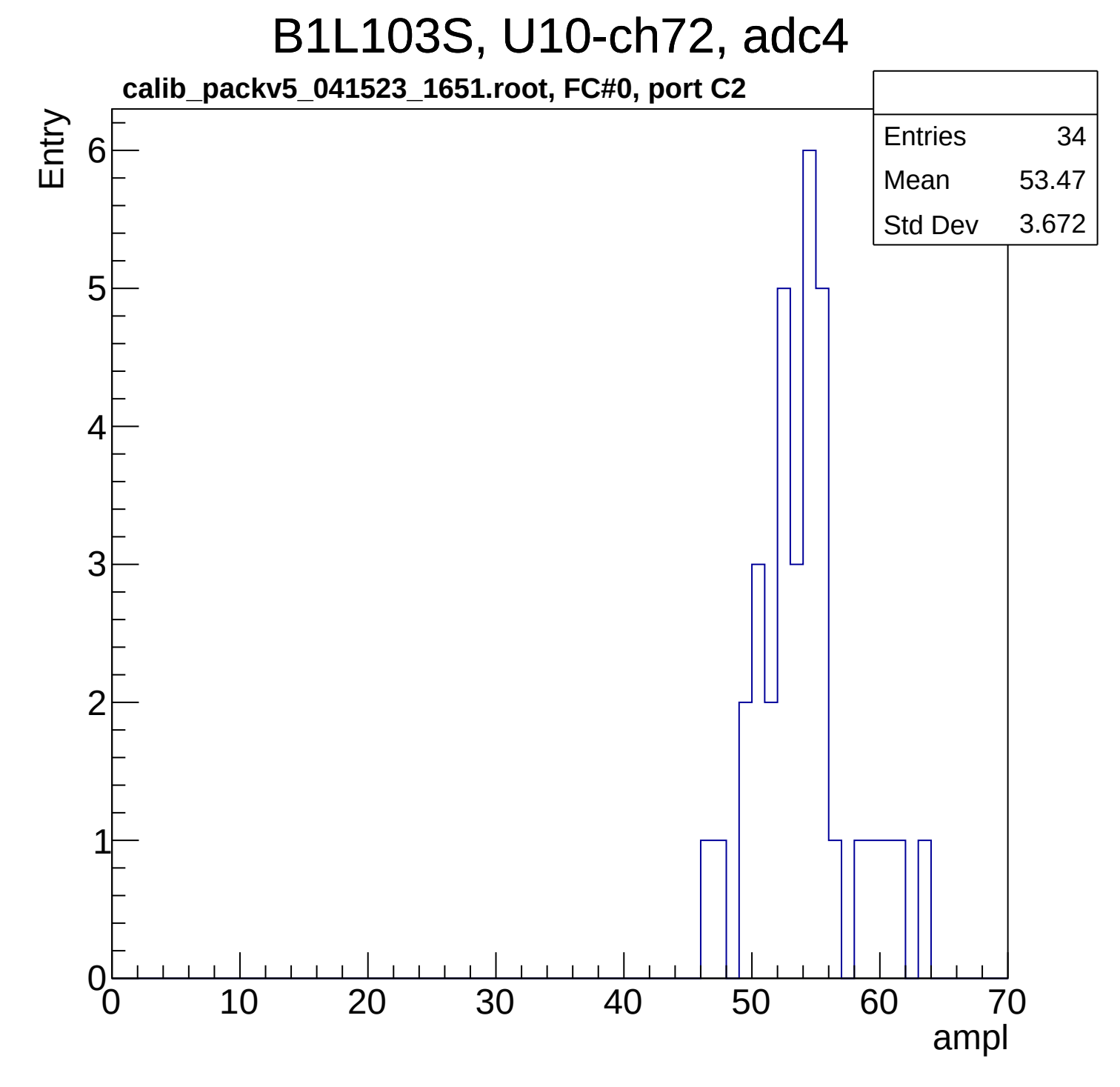
40
50
60
70


B1L103S, U10-ch72, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 34
Mean 53.47
Std Dev 3.672
Entry
ampl
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1
2
3
4
5
6
0
10
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40
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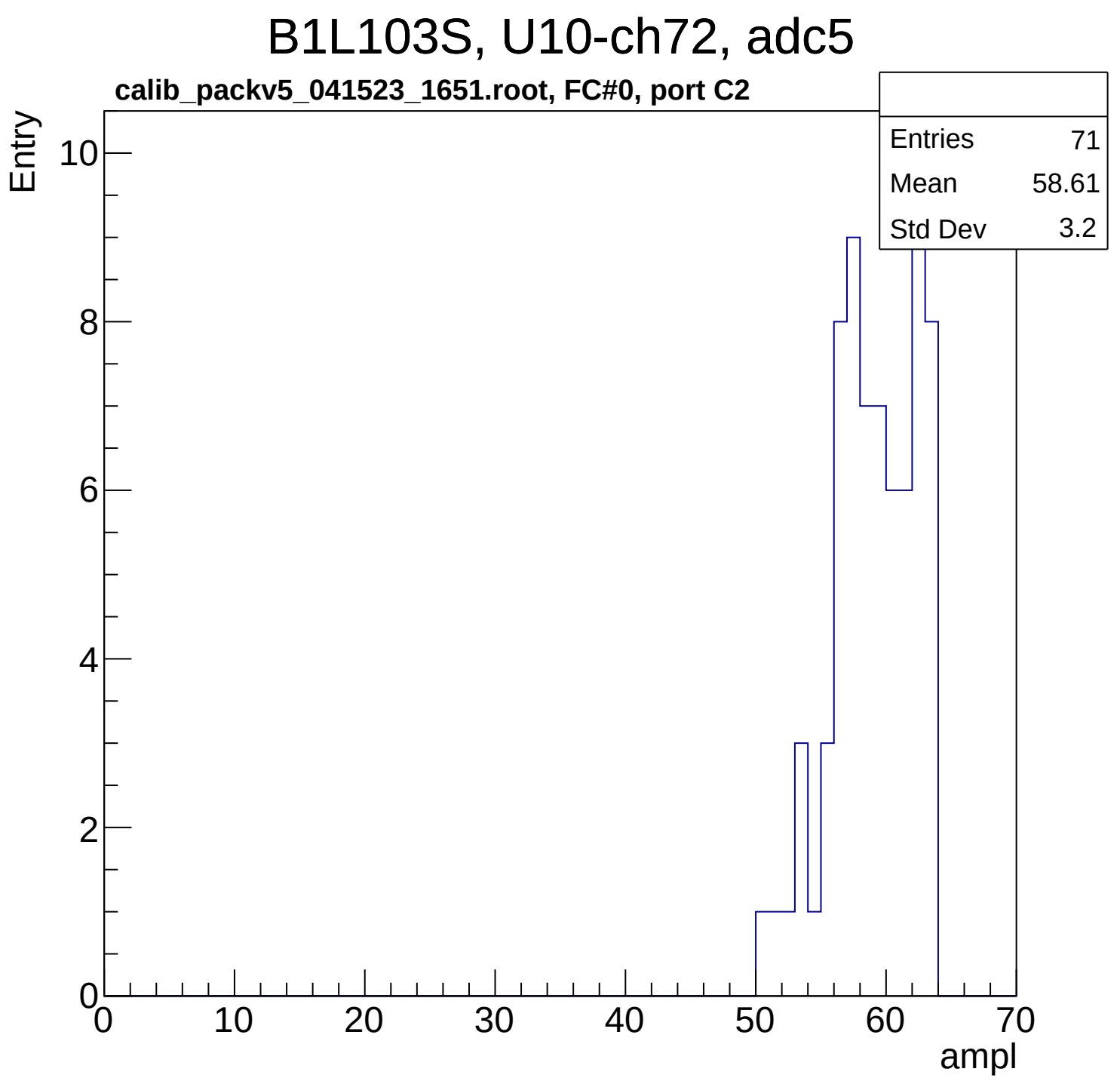
60
70


B1L103S, U10-ch72, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 58.61
Std Dev 3.2
Entry
ampl
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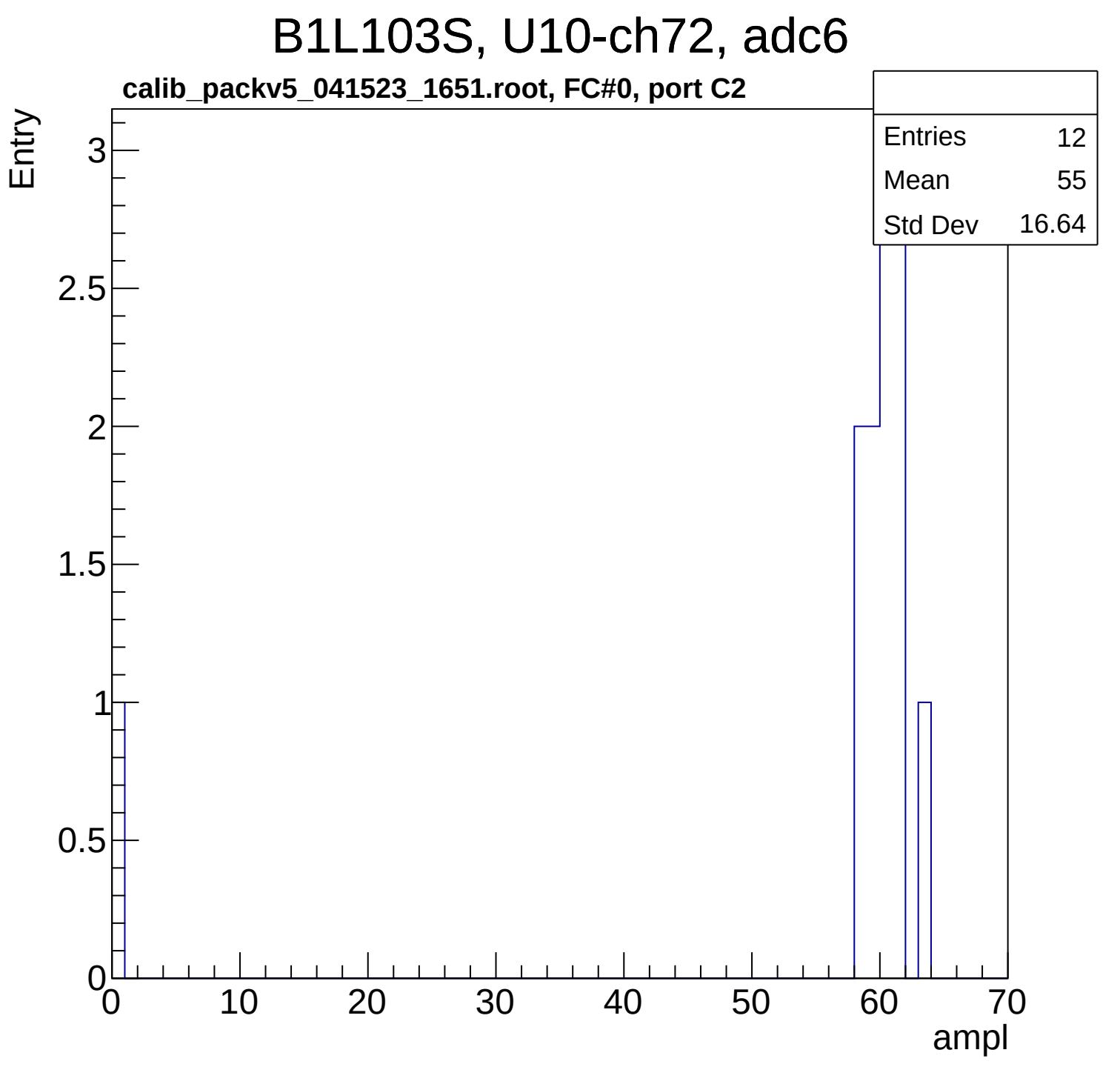
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U10-ch72, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 55
Std Dev 16.64
Entry
ampl
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1.5
2
2.5
3
0
10
20
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40
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60
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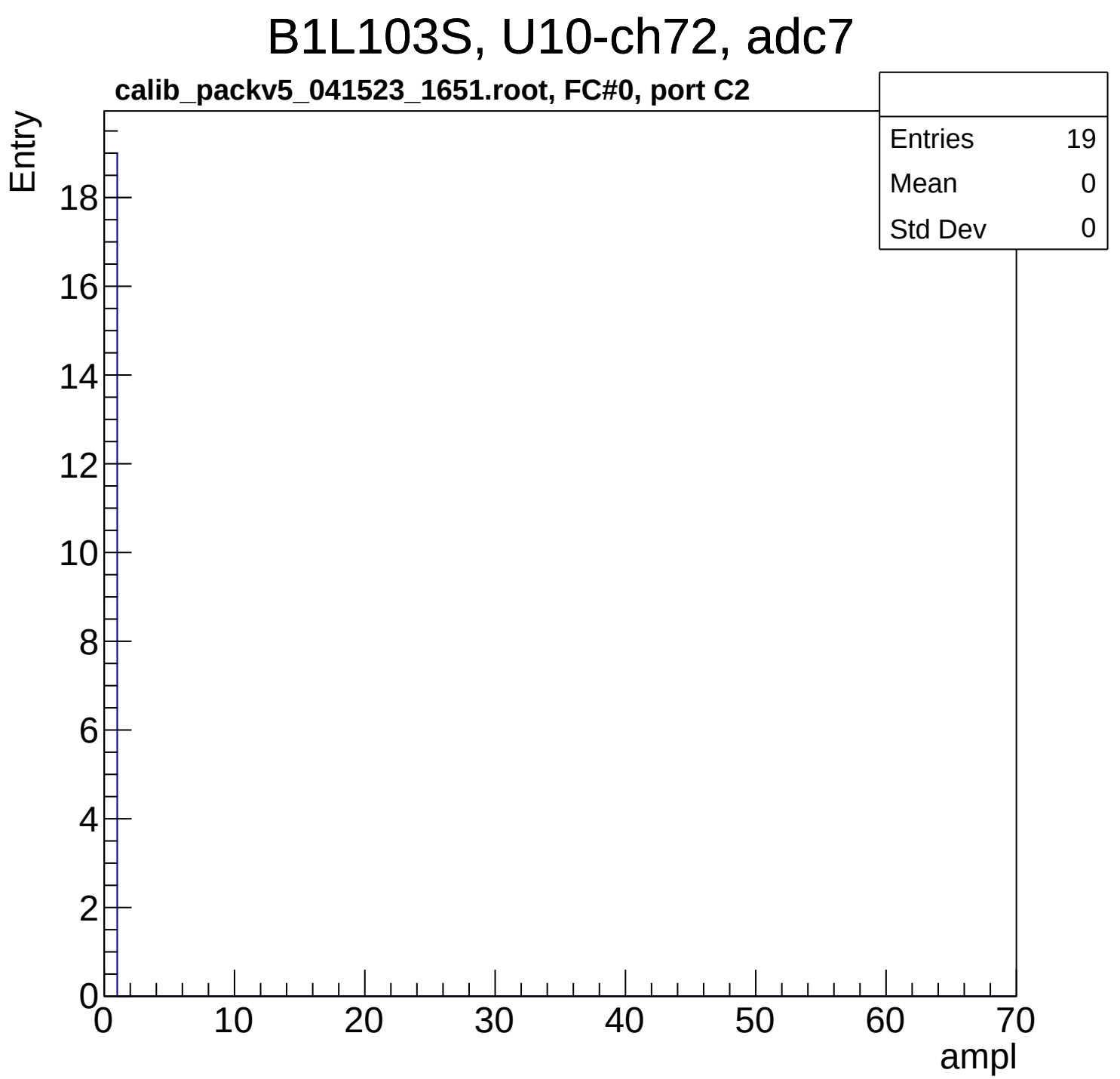
B1L103S, U10-ch72, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
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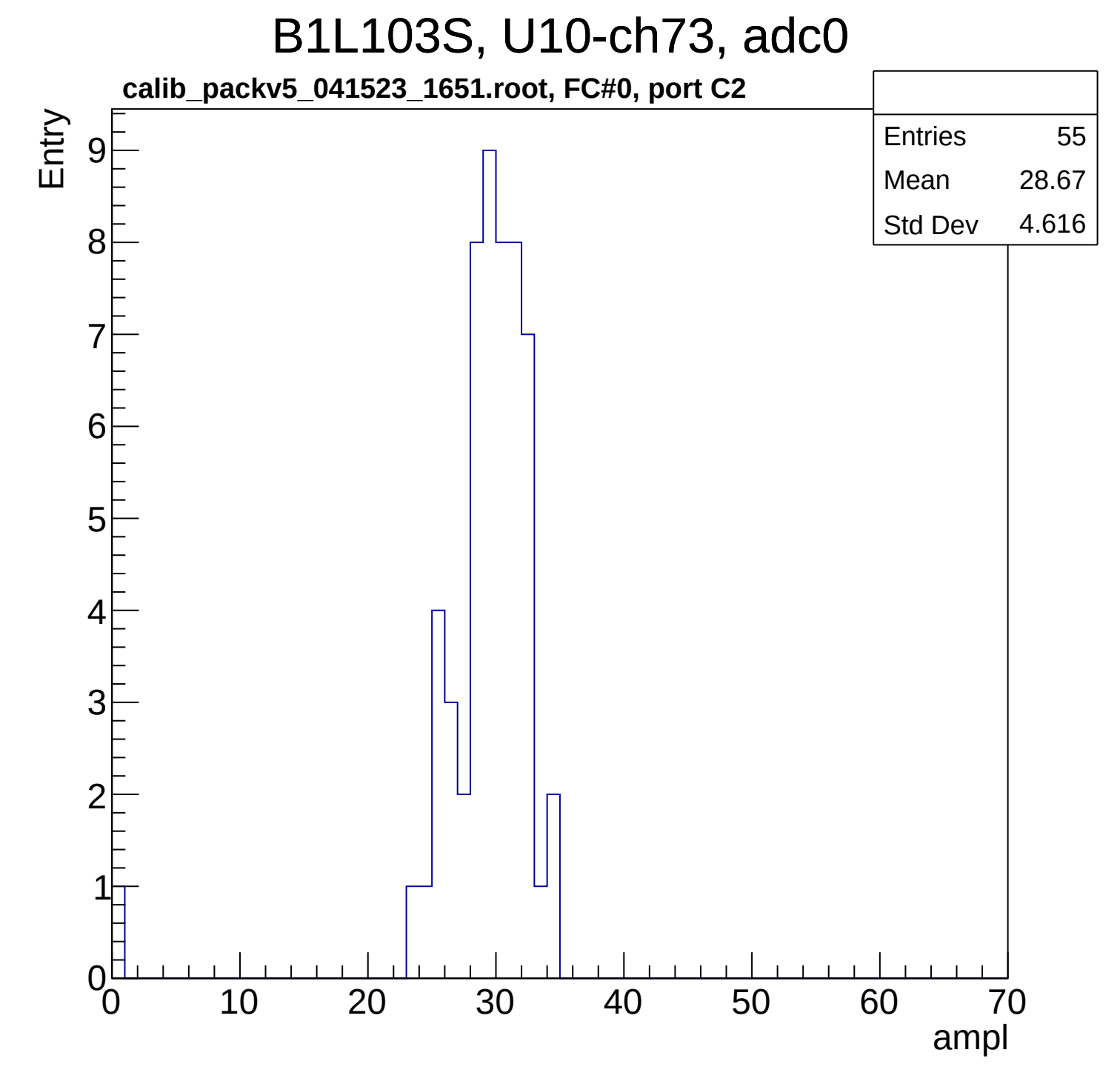
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch73, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 28.67
Std Dev 4.616
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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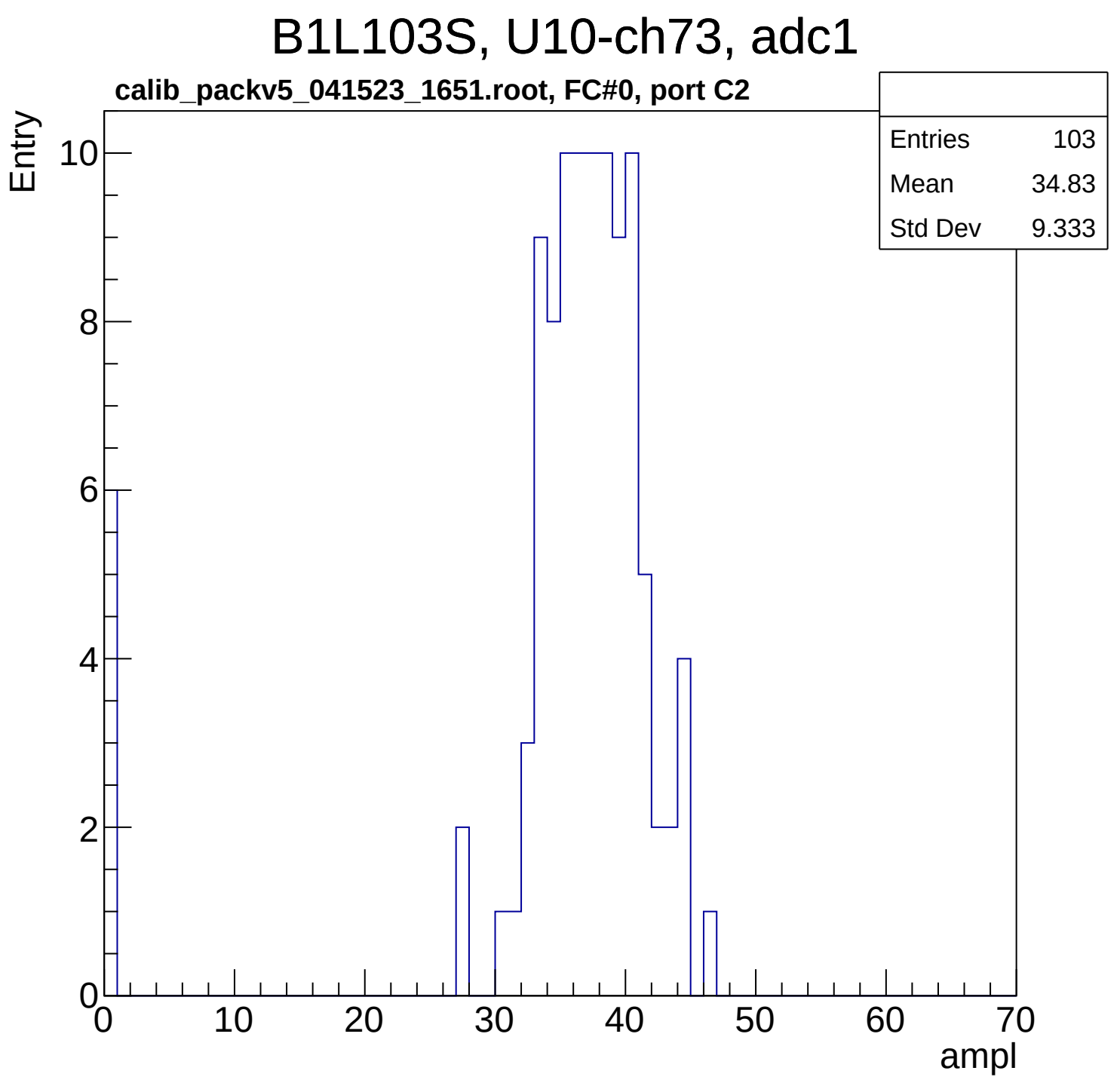
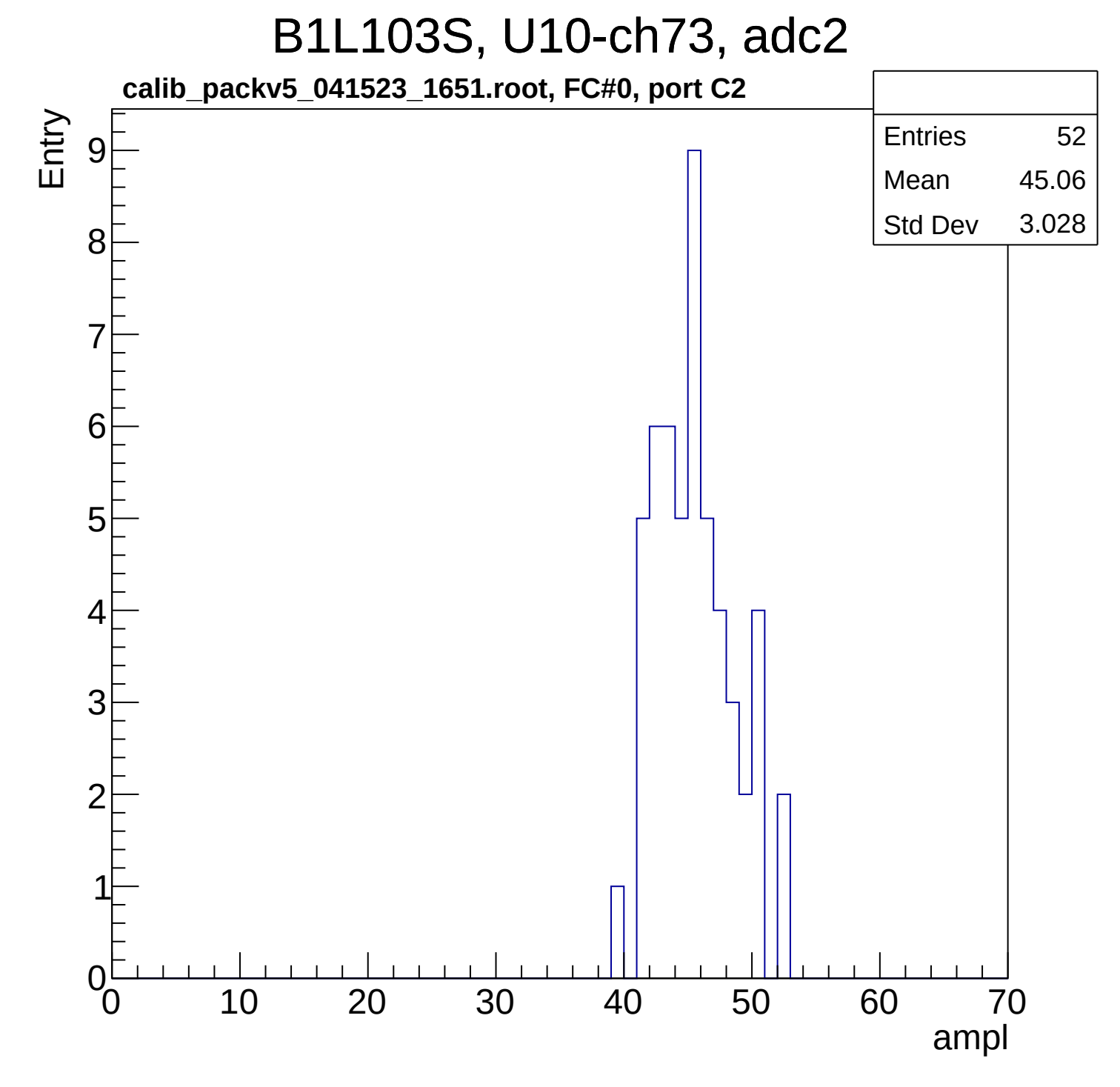
50
60
70


B1L103S, U10-ch73, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 103
Mean 34.83
Std Dev 9.333
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U10-ch73, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 45.06
Std Dev 3.028
Entry
ampl
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2
3
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5
6
7
8
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0
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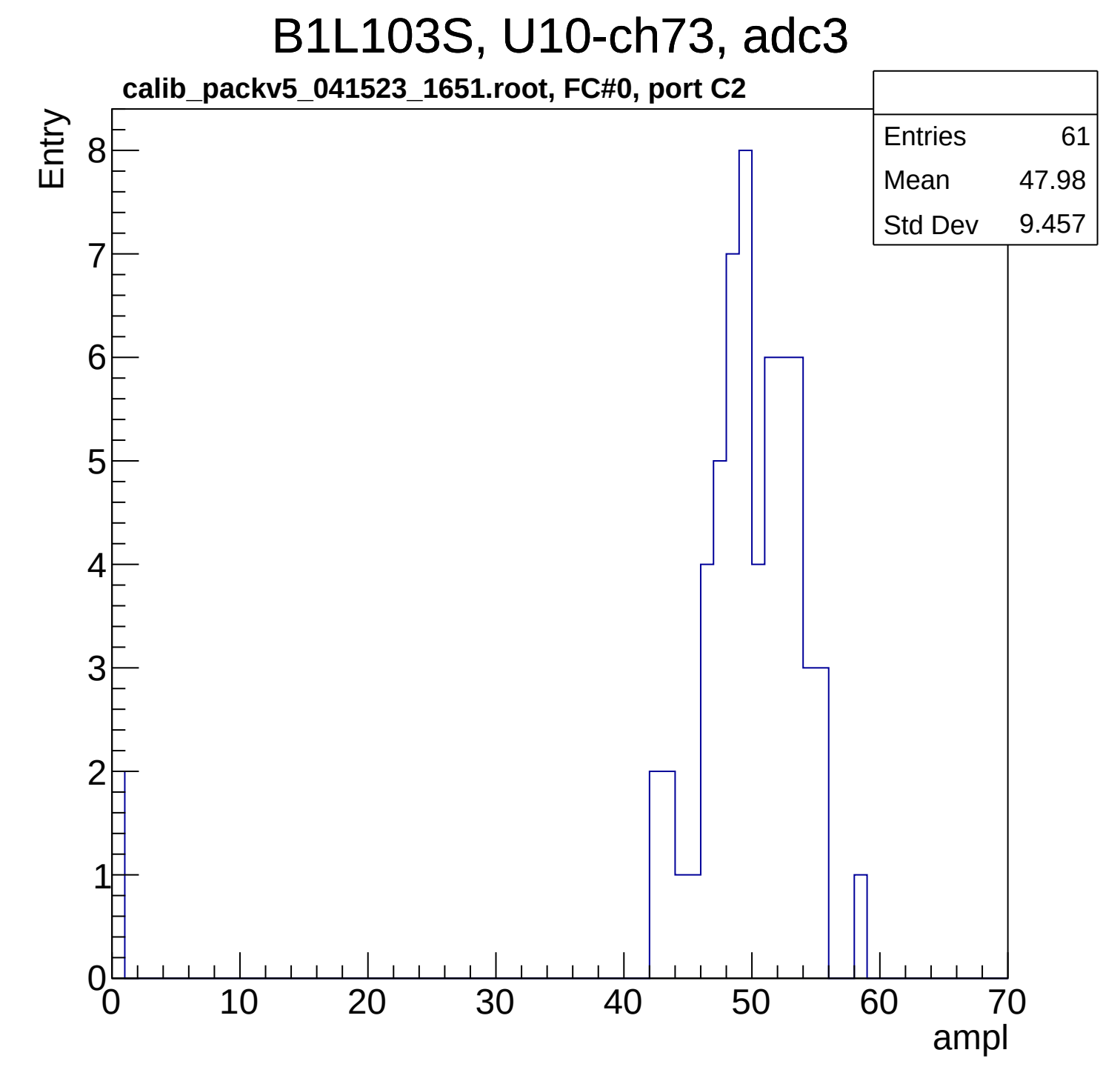
B1L103S, U10-ch73, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 47.98
Std Dev 9.457
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
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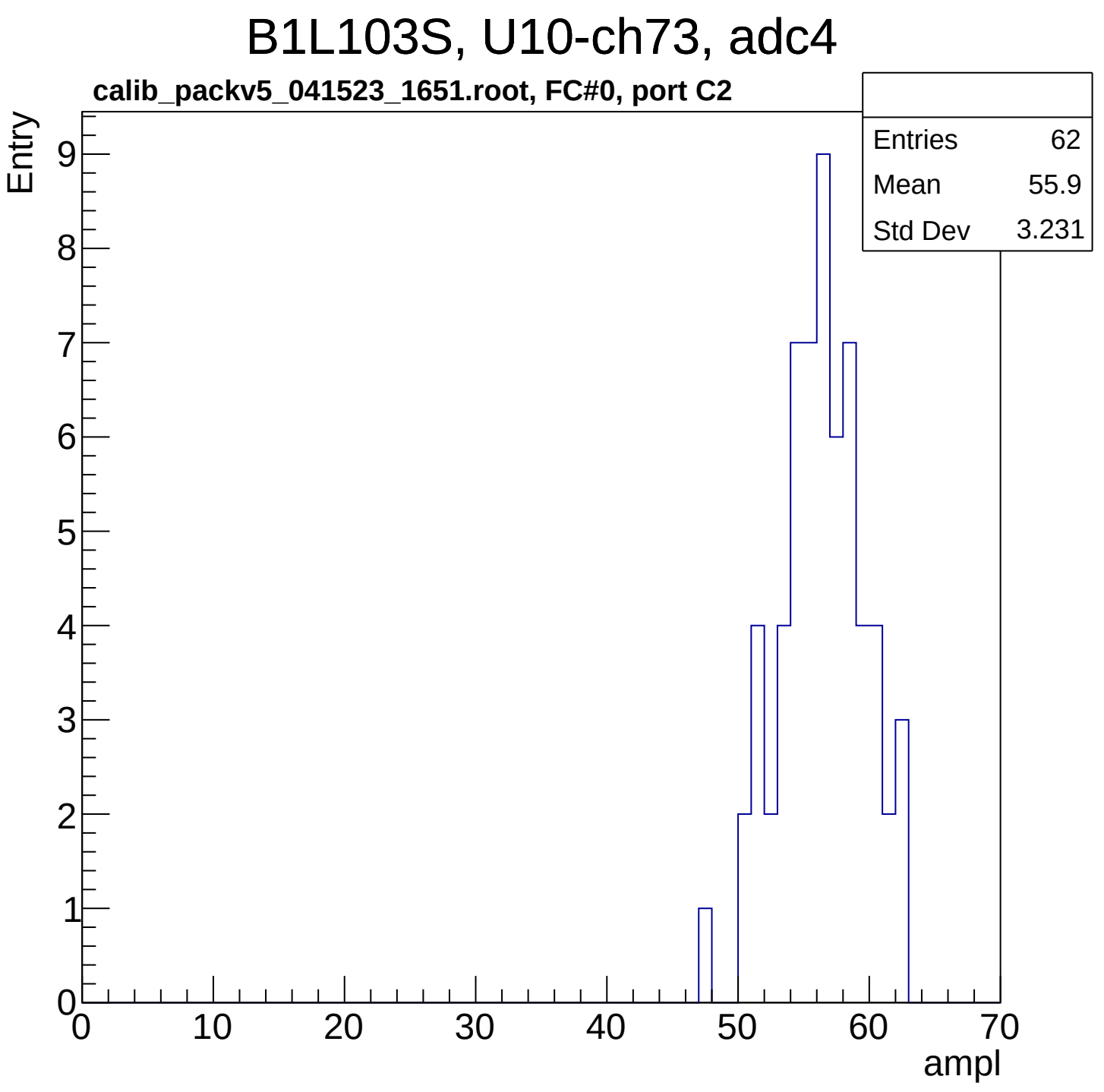
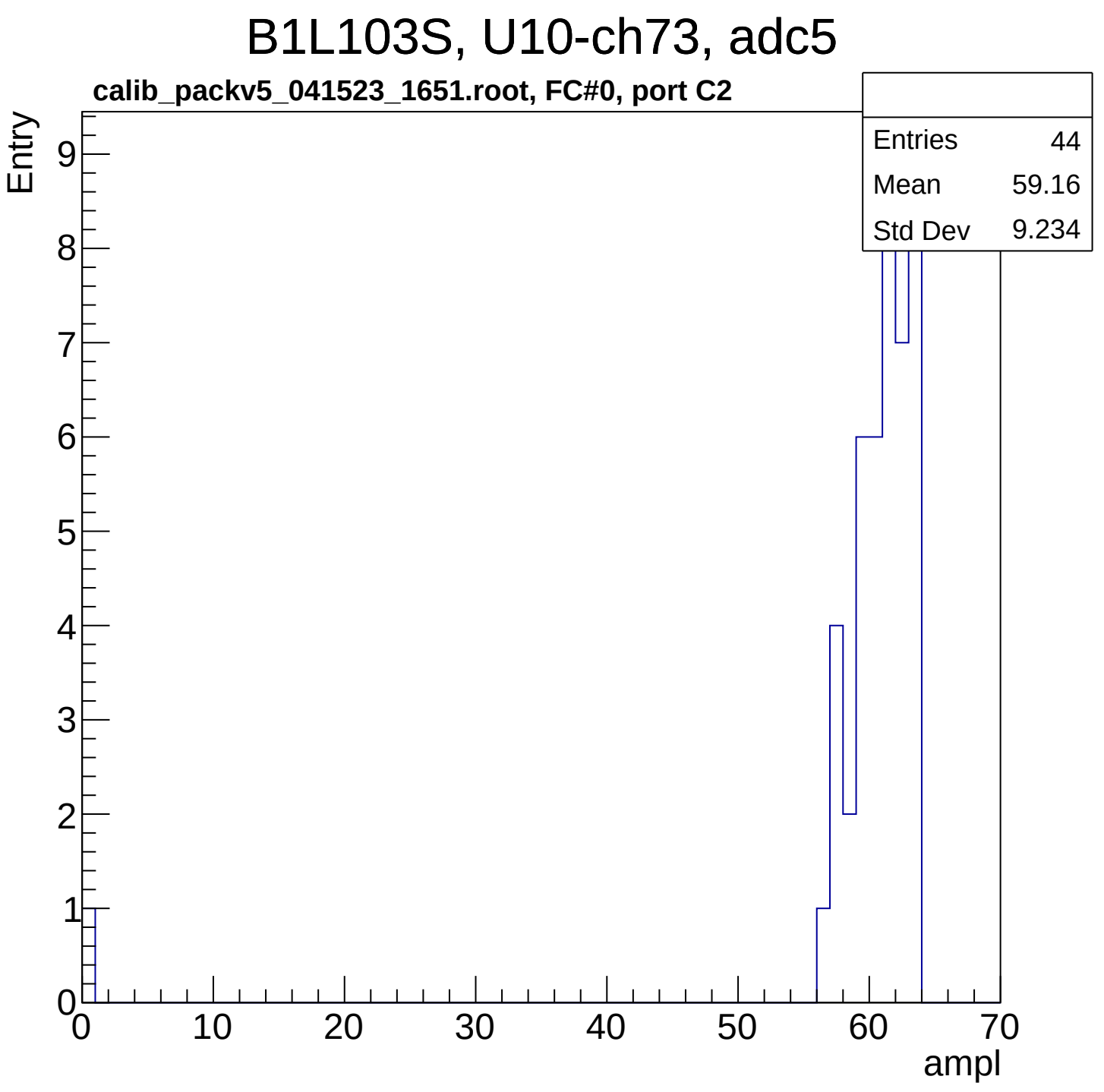
40
50
60
70


B1L103S, U10-ch73, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 55.9
Std Dev 3.231
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U10-ch73, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 59.16
Std Dev 9.234
Entry
ampl
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2
3
4
5
6
7
8
9
0
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40
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60
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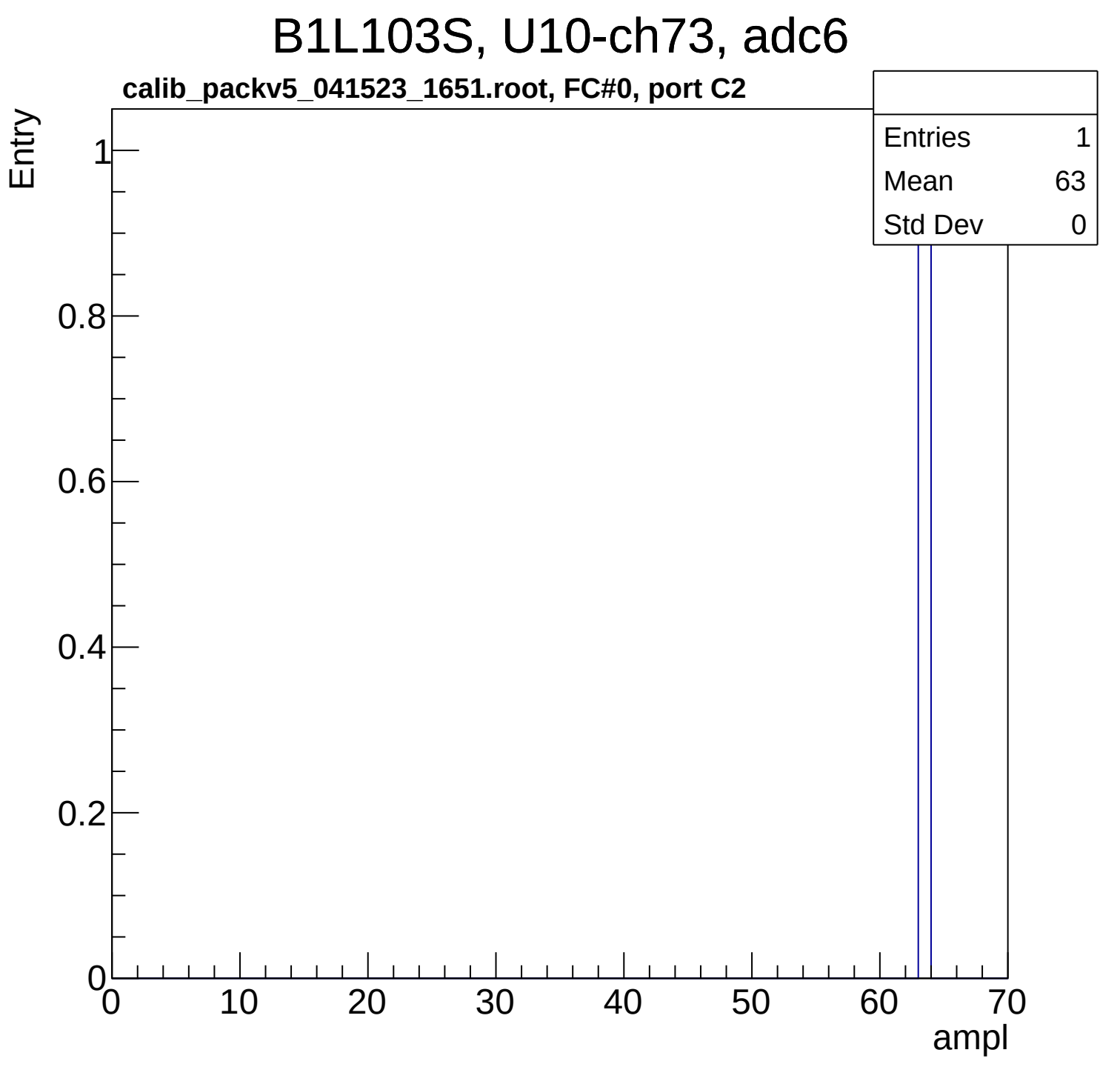
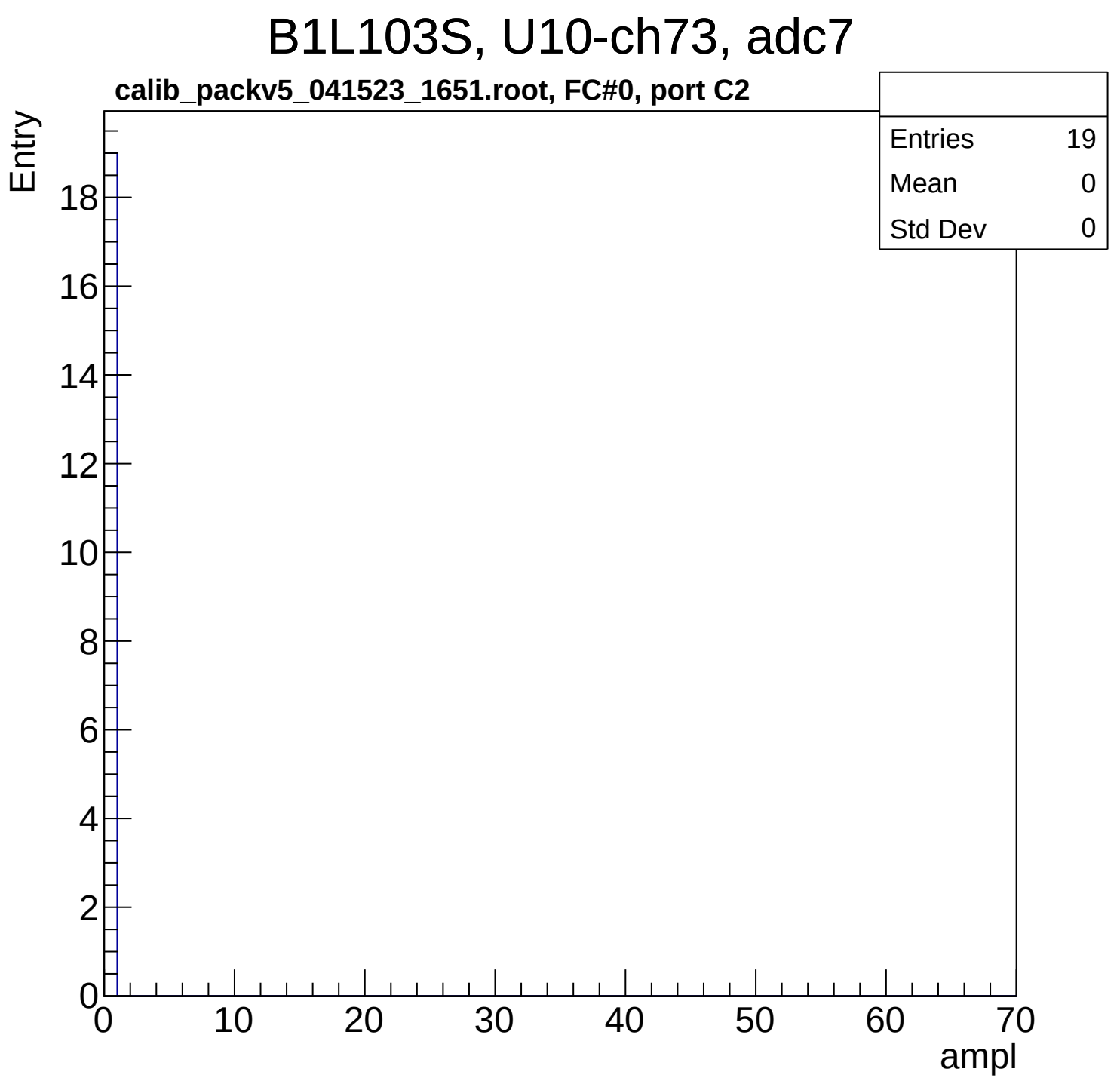

B1L103S, U10-ch73, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 1
Mean 63
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch73, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
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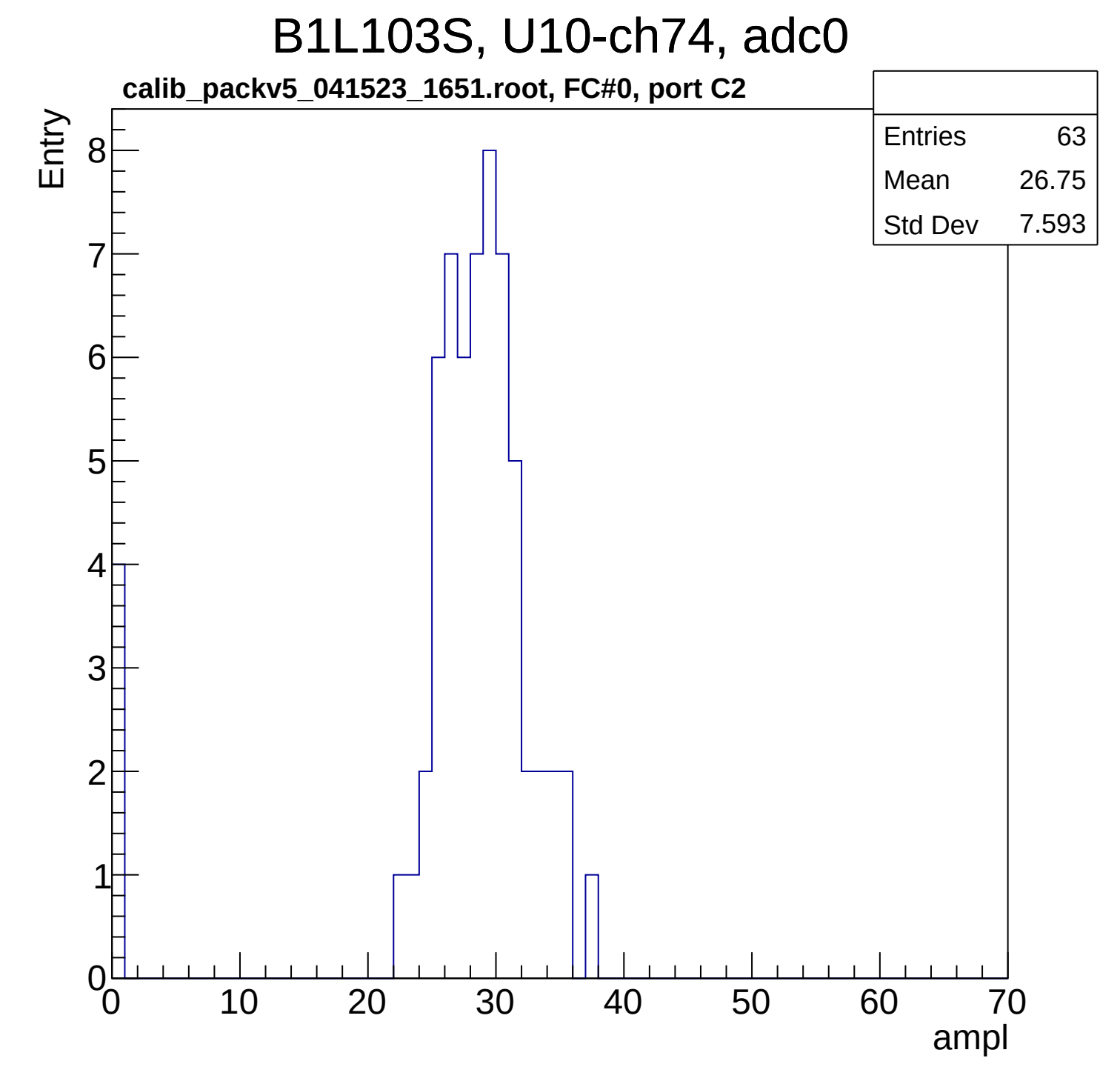
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch74, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 26.75
Std Dev 7.593
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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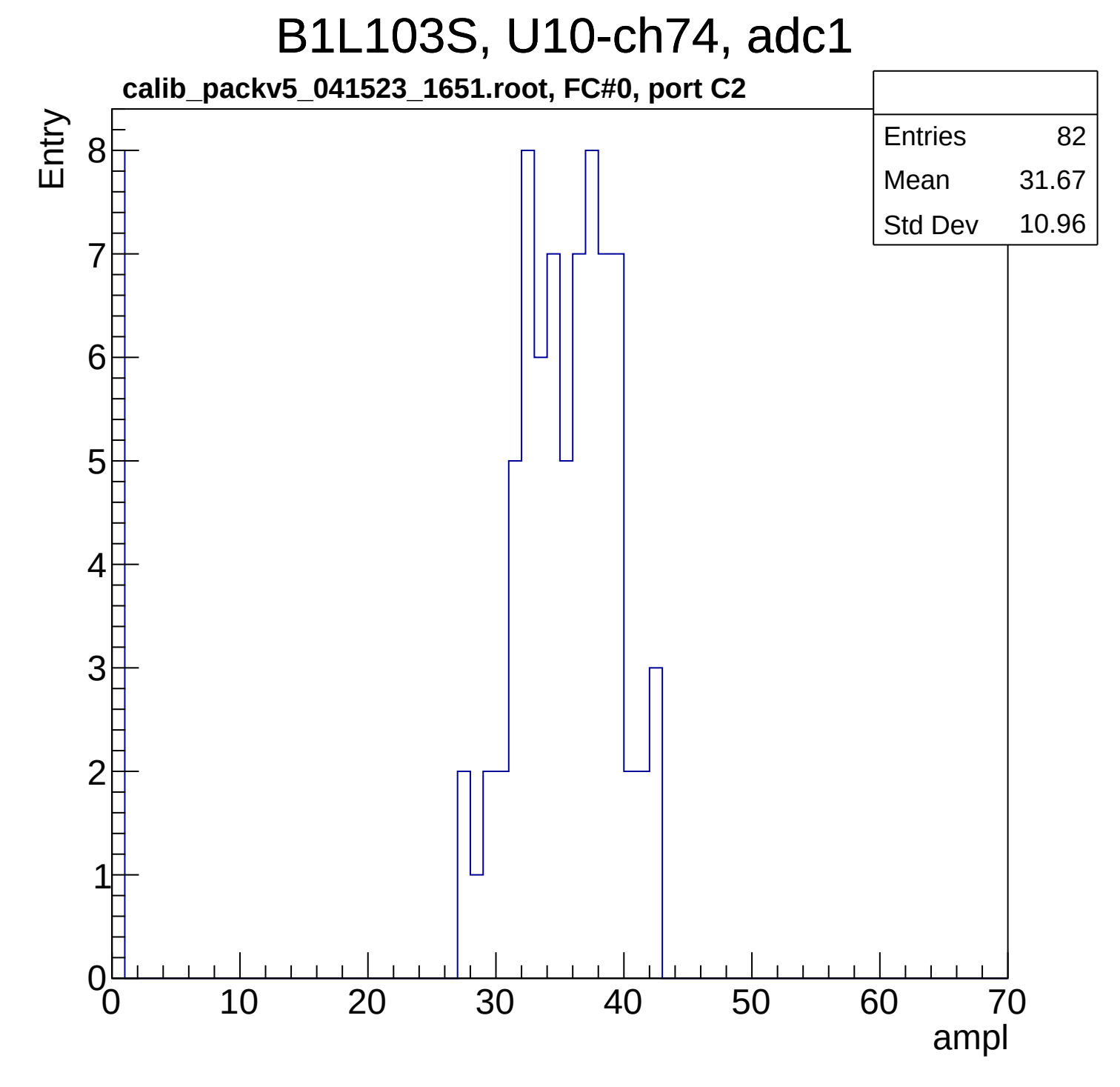
40
50
60
70


B1L103S, U10-ch74, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 31.67
Std Dev 10.96
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
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60
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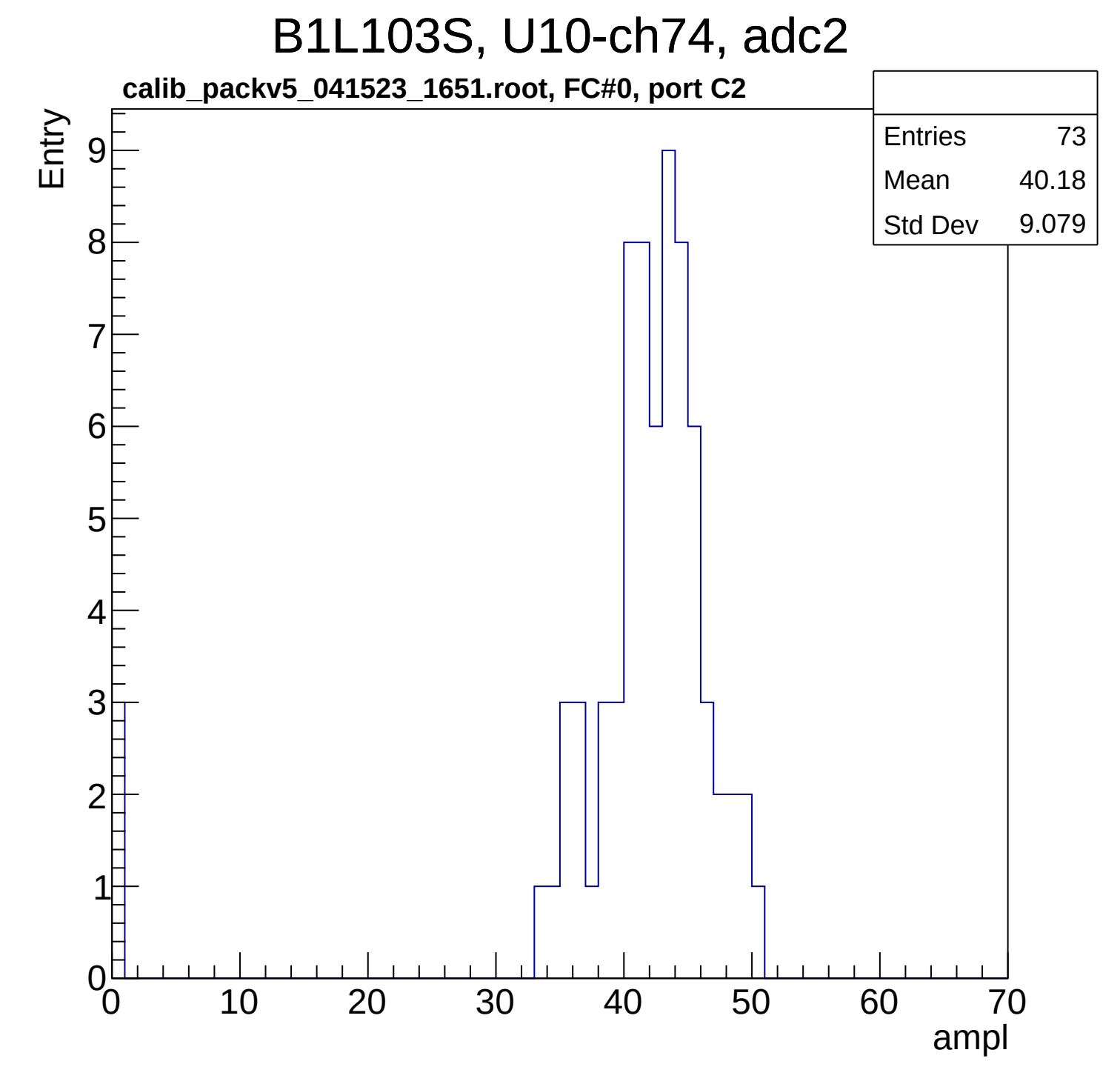
B1L103S, U10-ch74, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 40.18
Std Dev 9.079
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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40
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60
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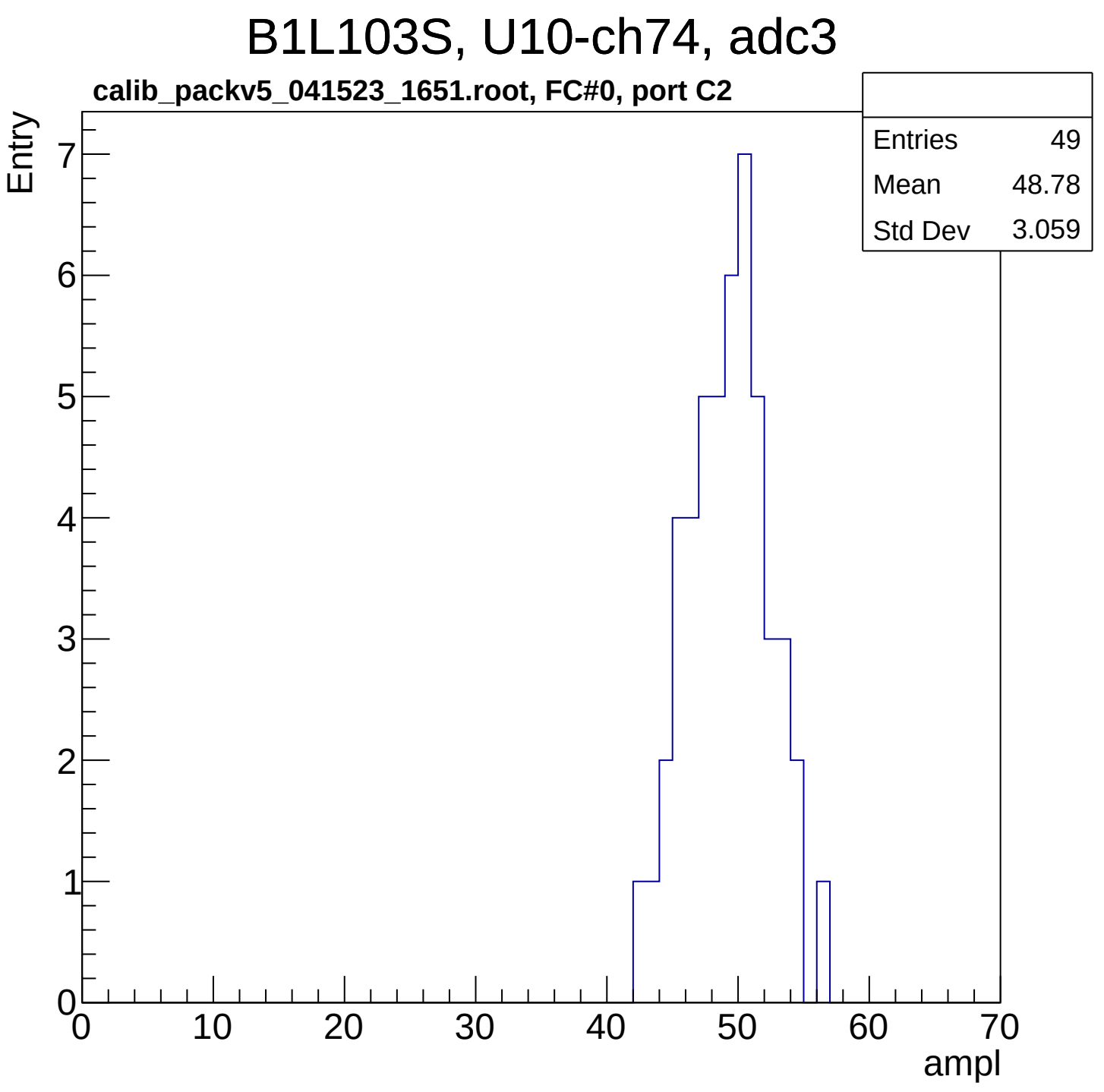
B1L103S, U10-ch74, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 48.78
Std Dev 3.059
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
30
40
50
60
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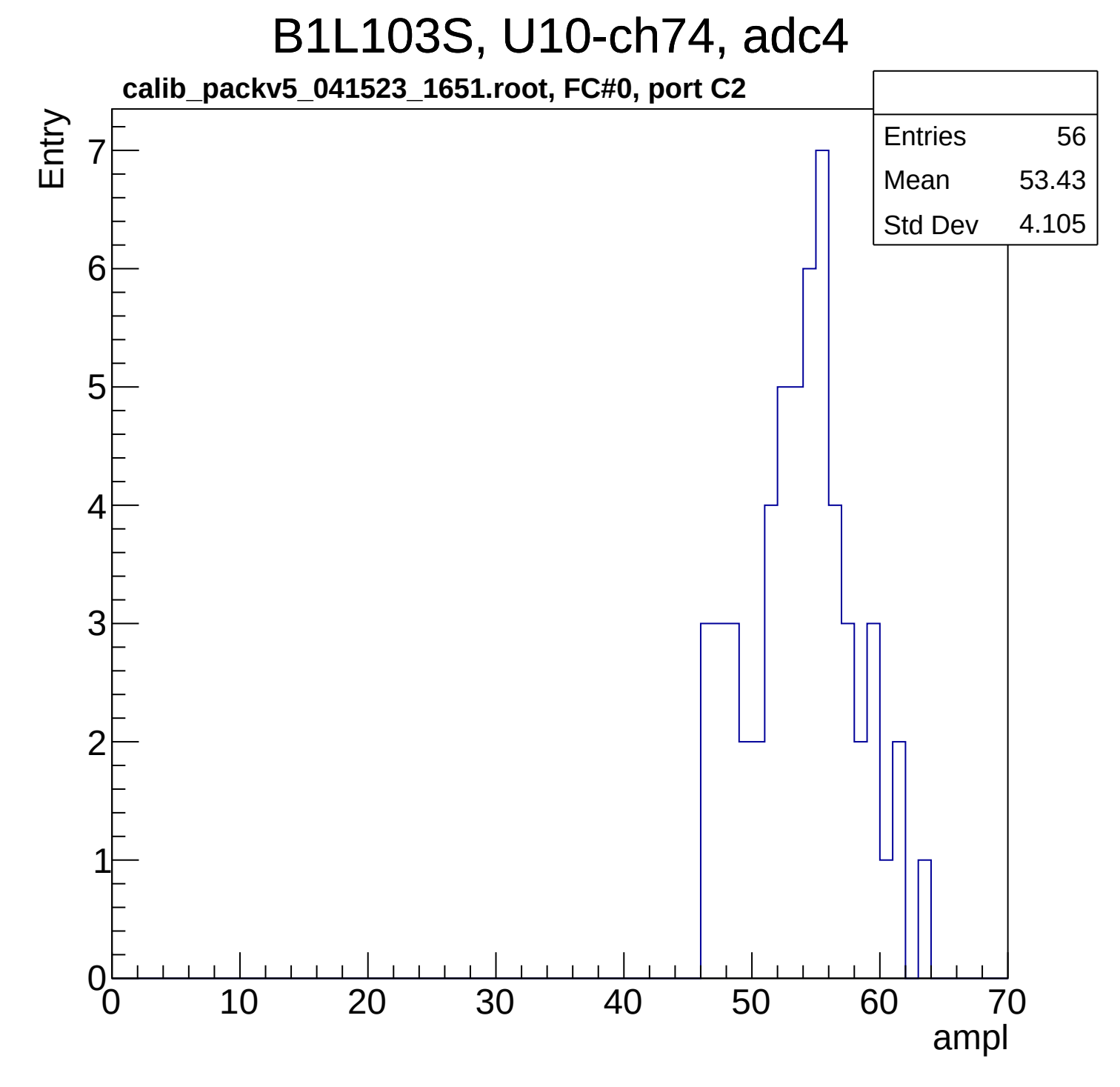
B1L103S, U10-ch74, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 53.43
Std Dev 4.105
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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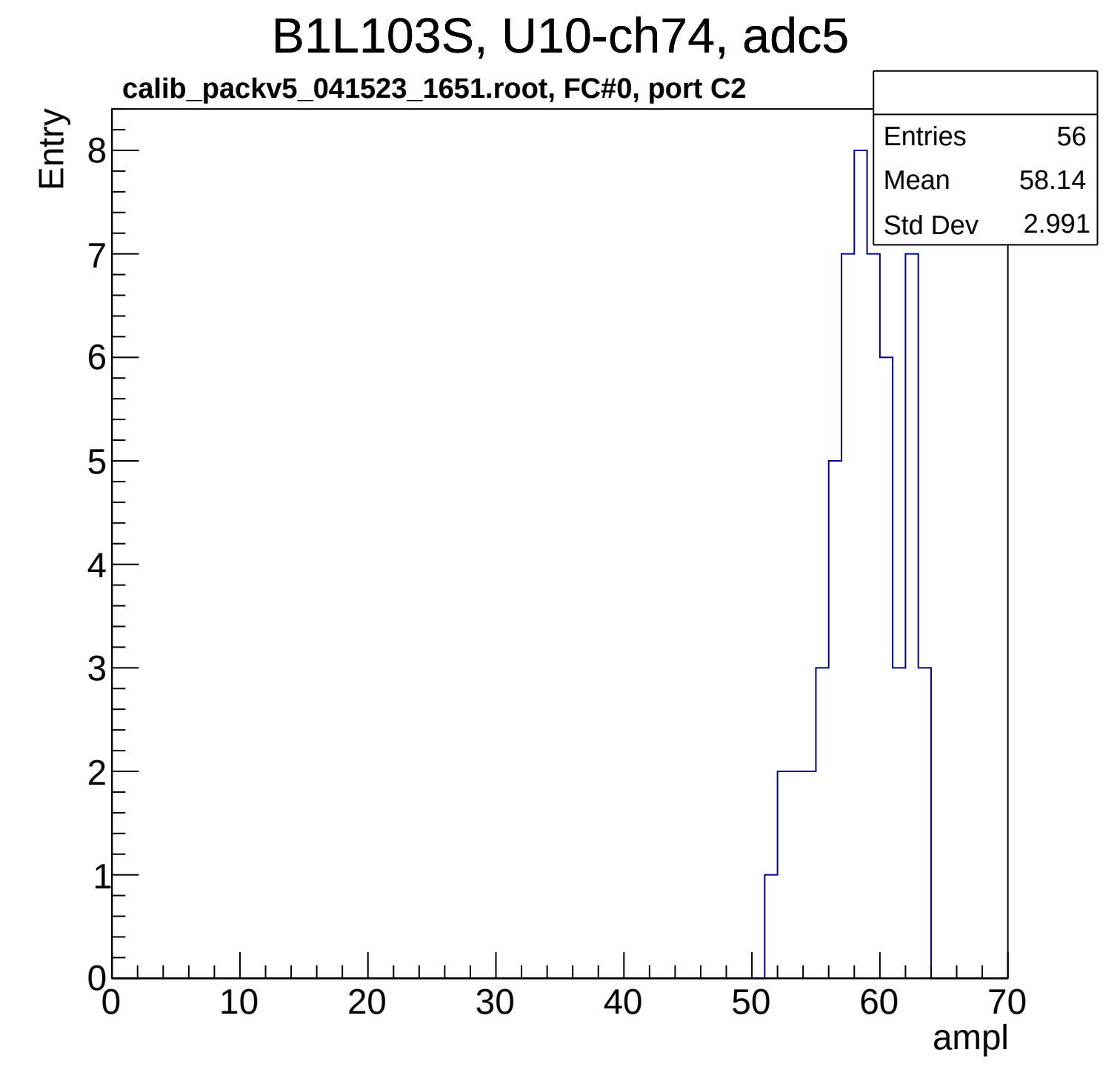
B1L103S, U10-ch74, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 58.14
Std Dev 2.991
Entry
ampl
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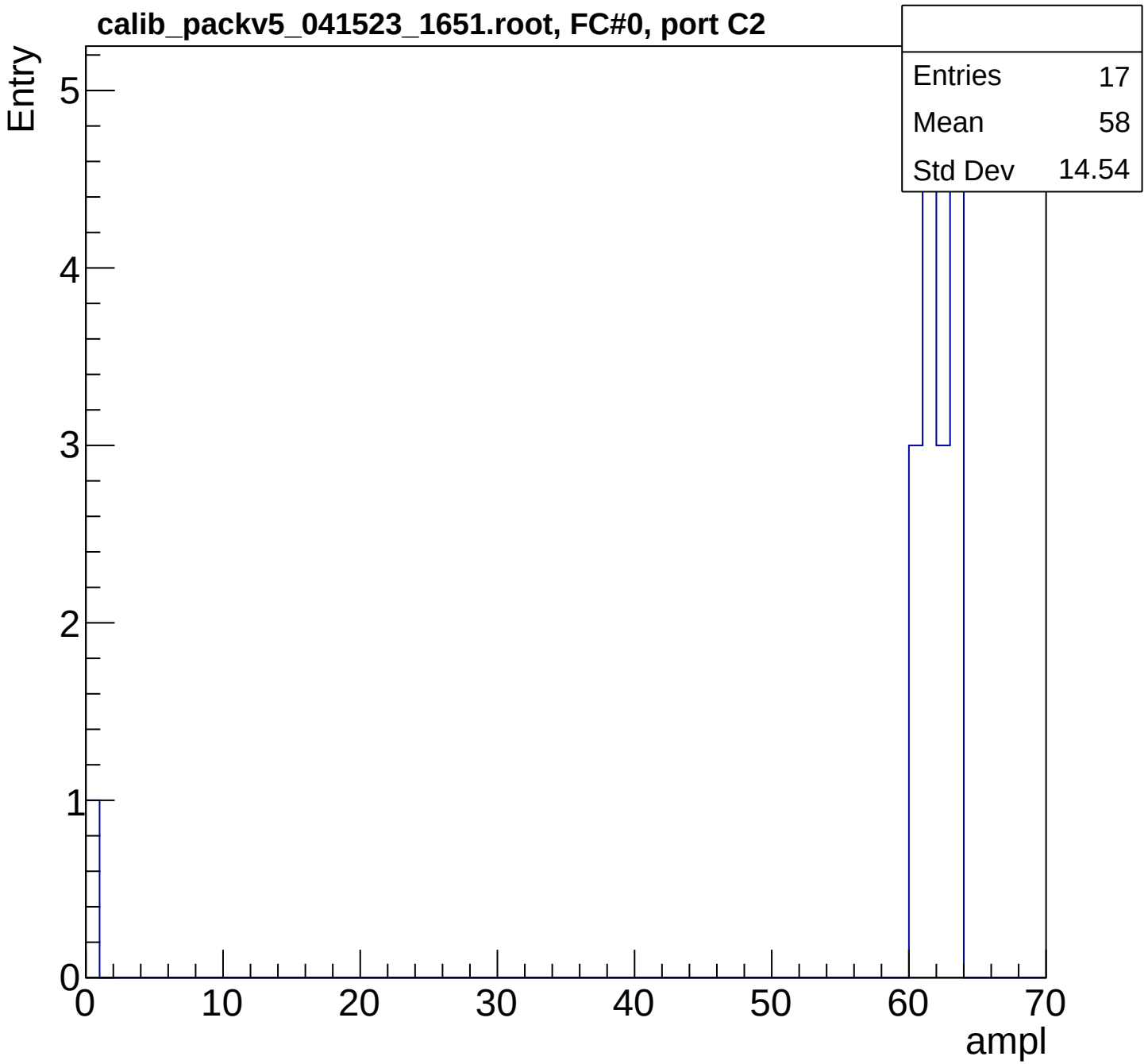
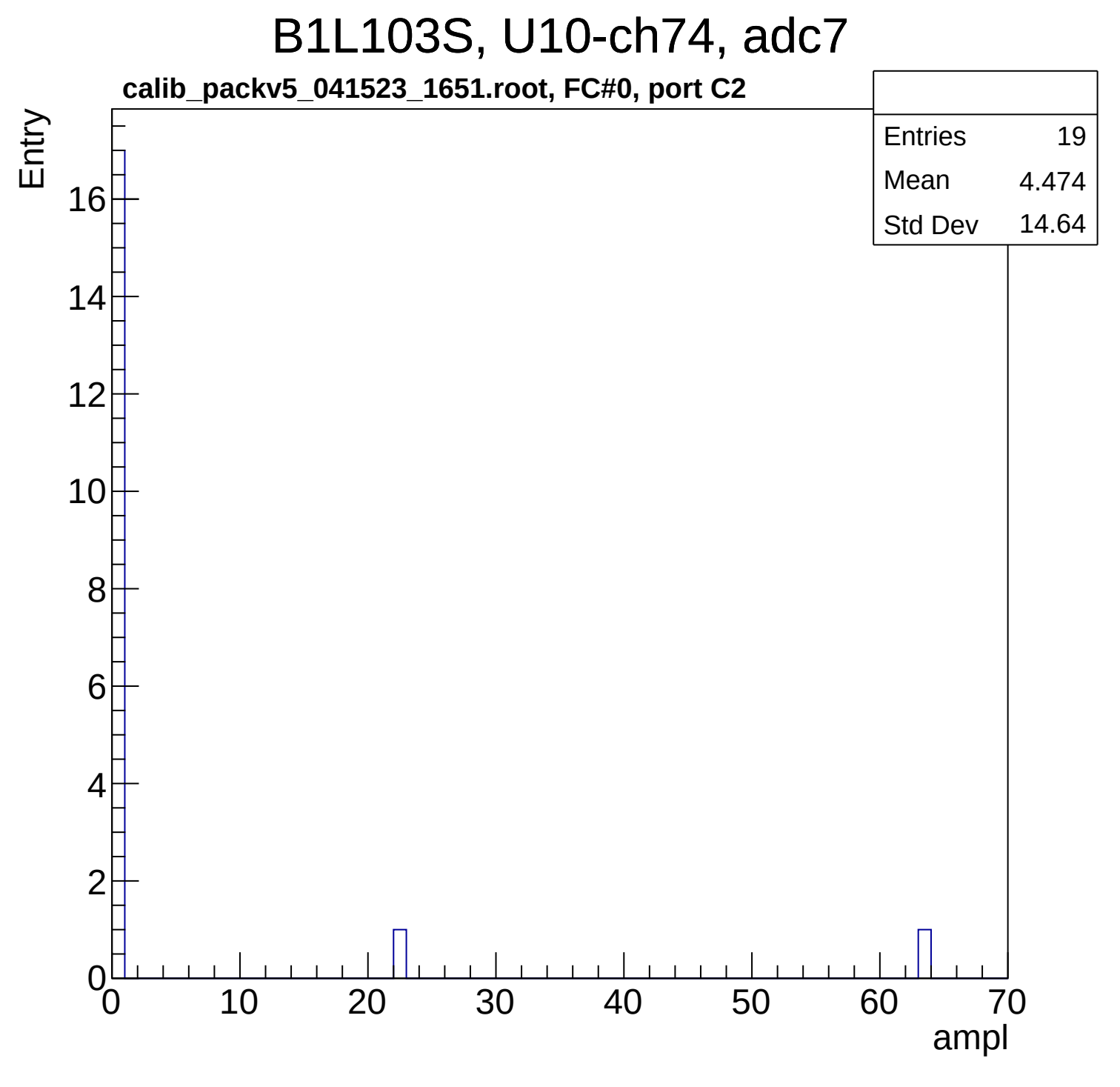
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U10-ch74, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 17
Mean 58
Std Dev 14.54
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch74, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 4.474
Std Dev 14.64
Entry
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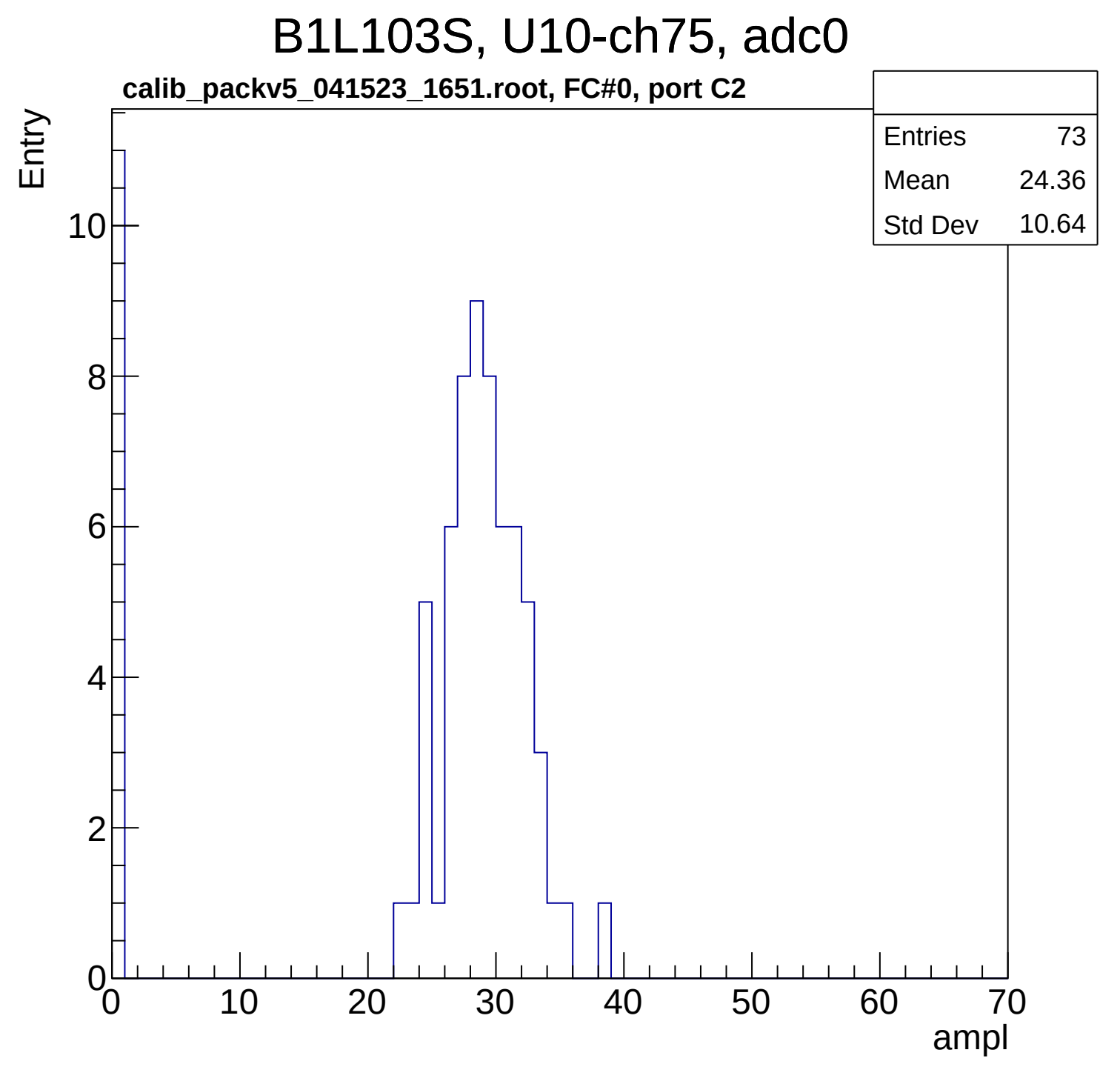
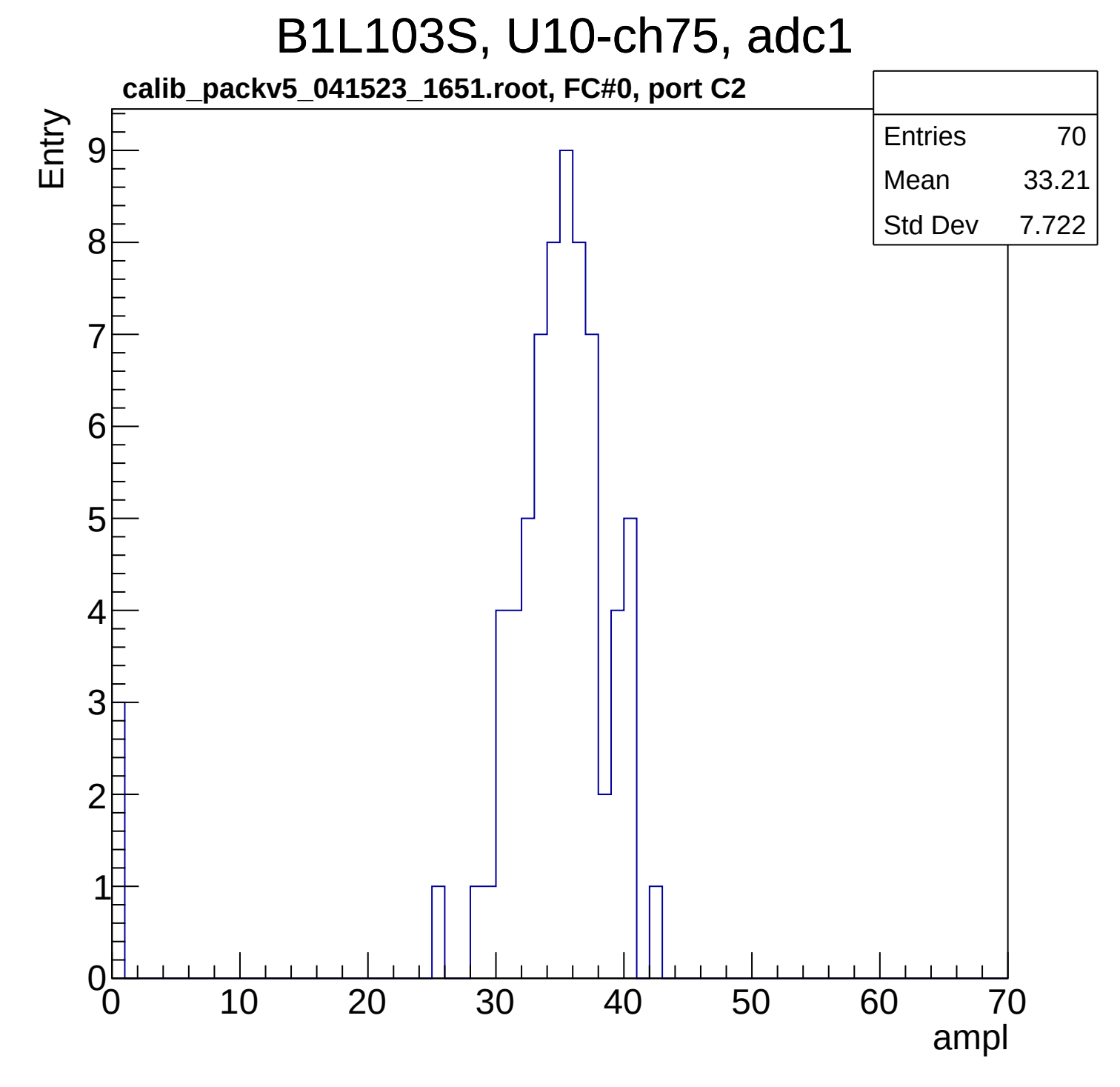
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch75, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 24.36
Std Dev 10.64
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch75, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 33.21
Std Dev 7.722
Entry
ampl
0
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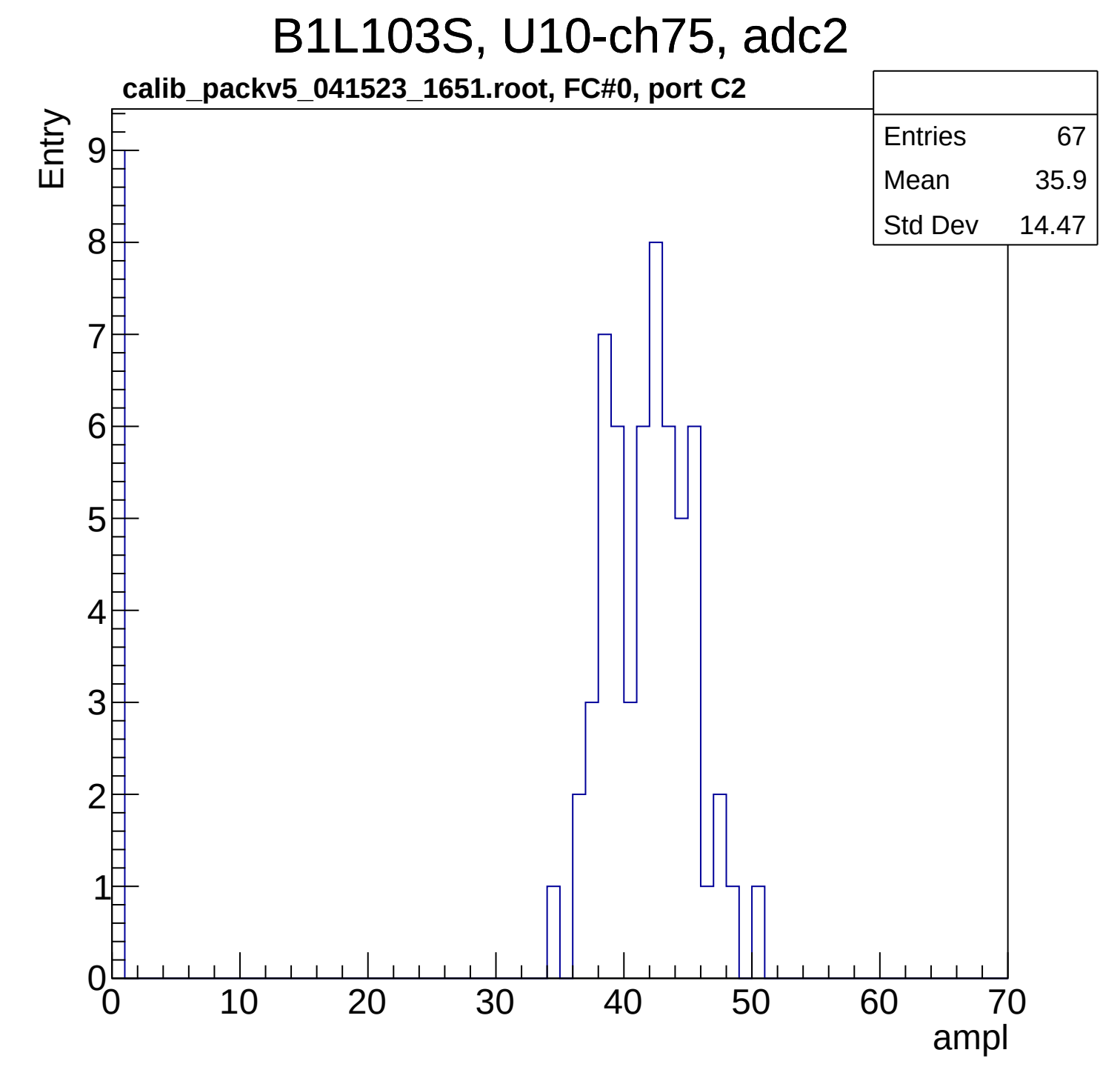
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U10-ch75, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 35.9
Std Dev 14.47
Entry
ampl
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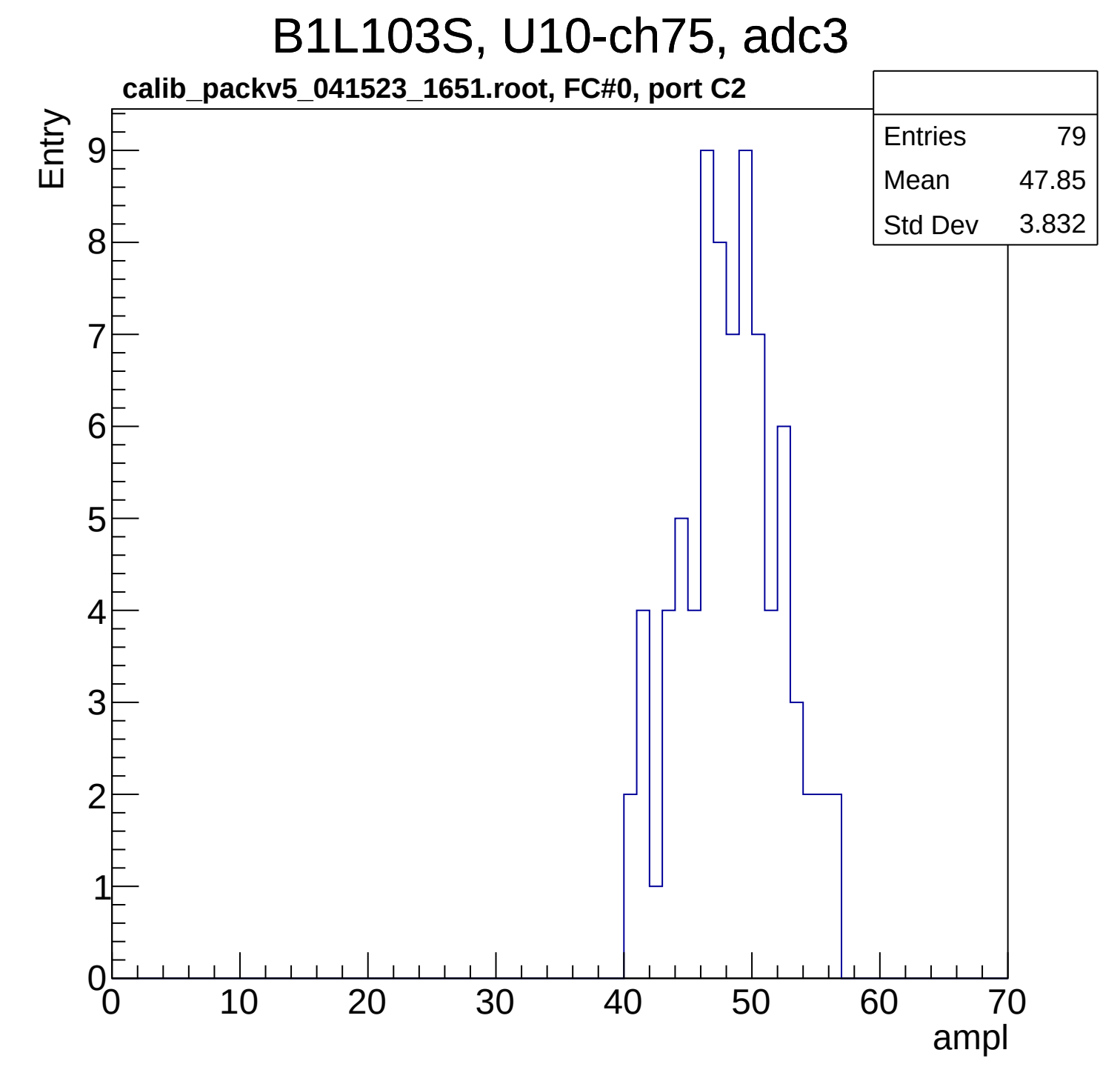
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U10-ch75, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 47.85
Std Dev 3.832
Entry
ampl
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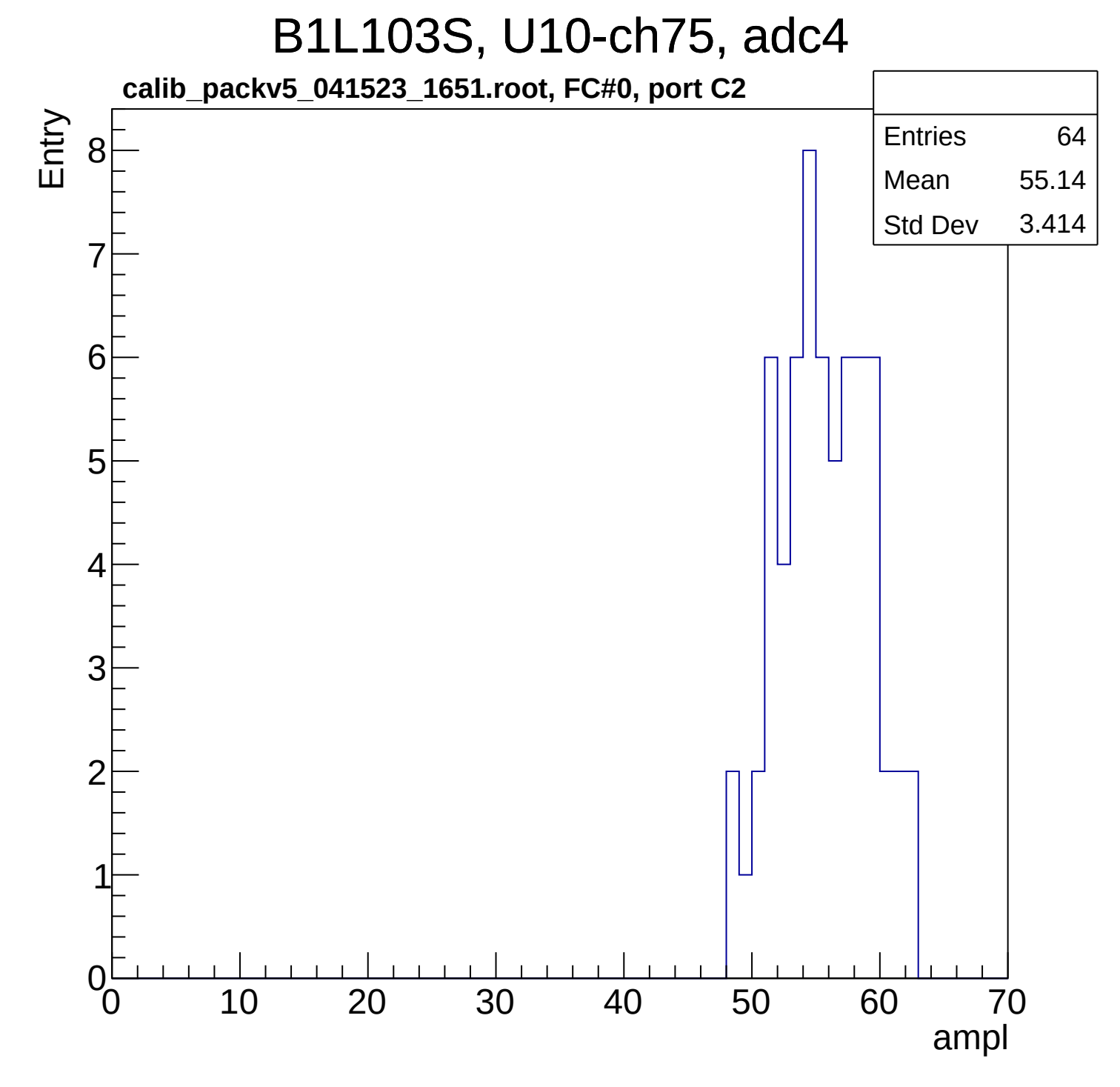
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U10-ch75, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 55.14
Std Dev 3.414
Entry
ampl
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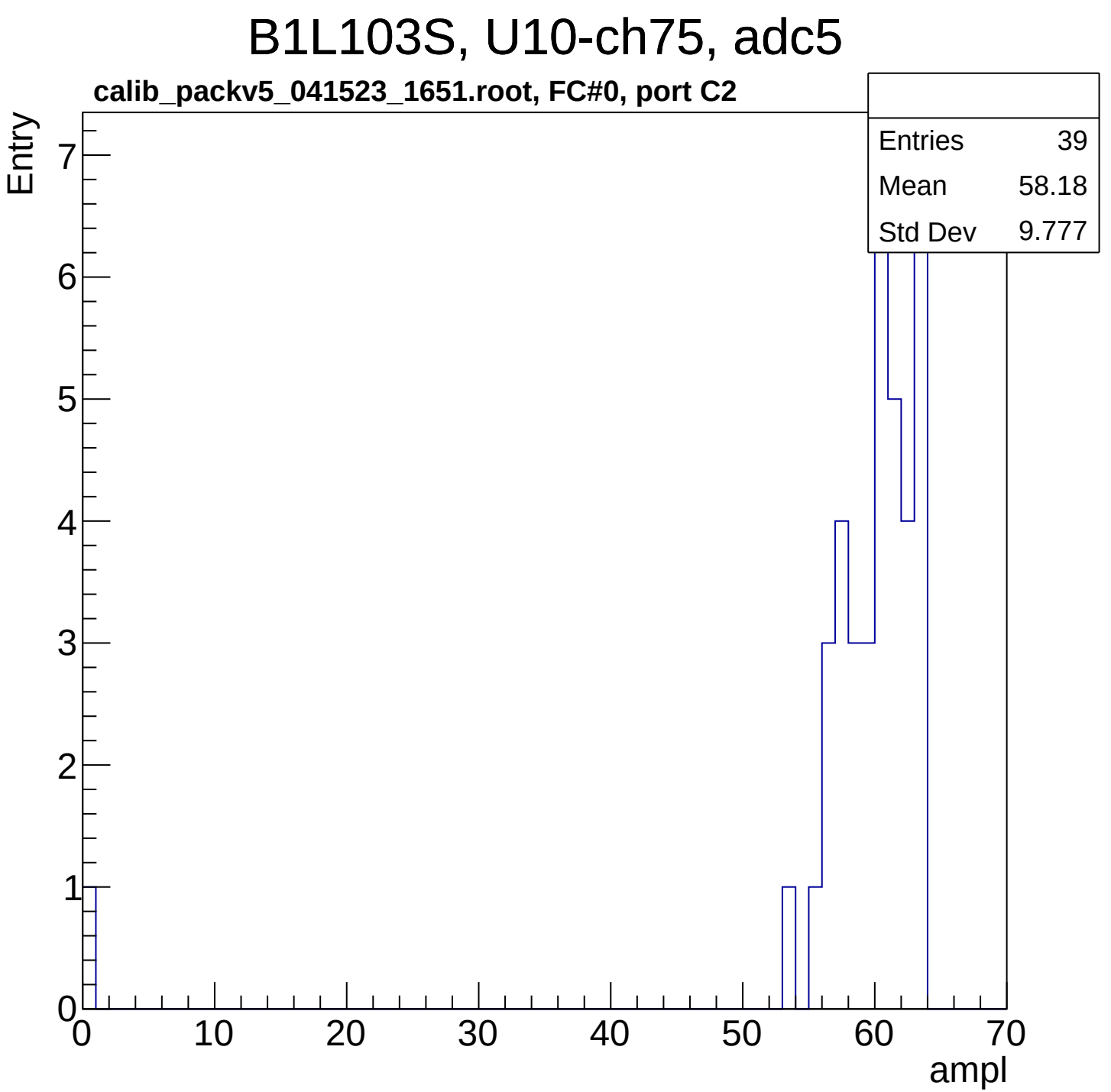
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U10-ch75, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 39
Mean 58.18
Std Dev 9.777
Entry
ampl
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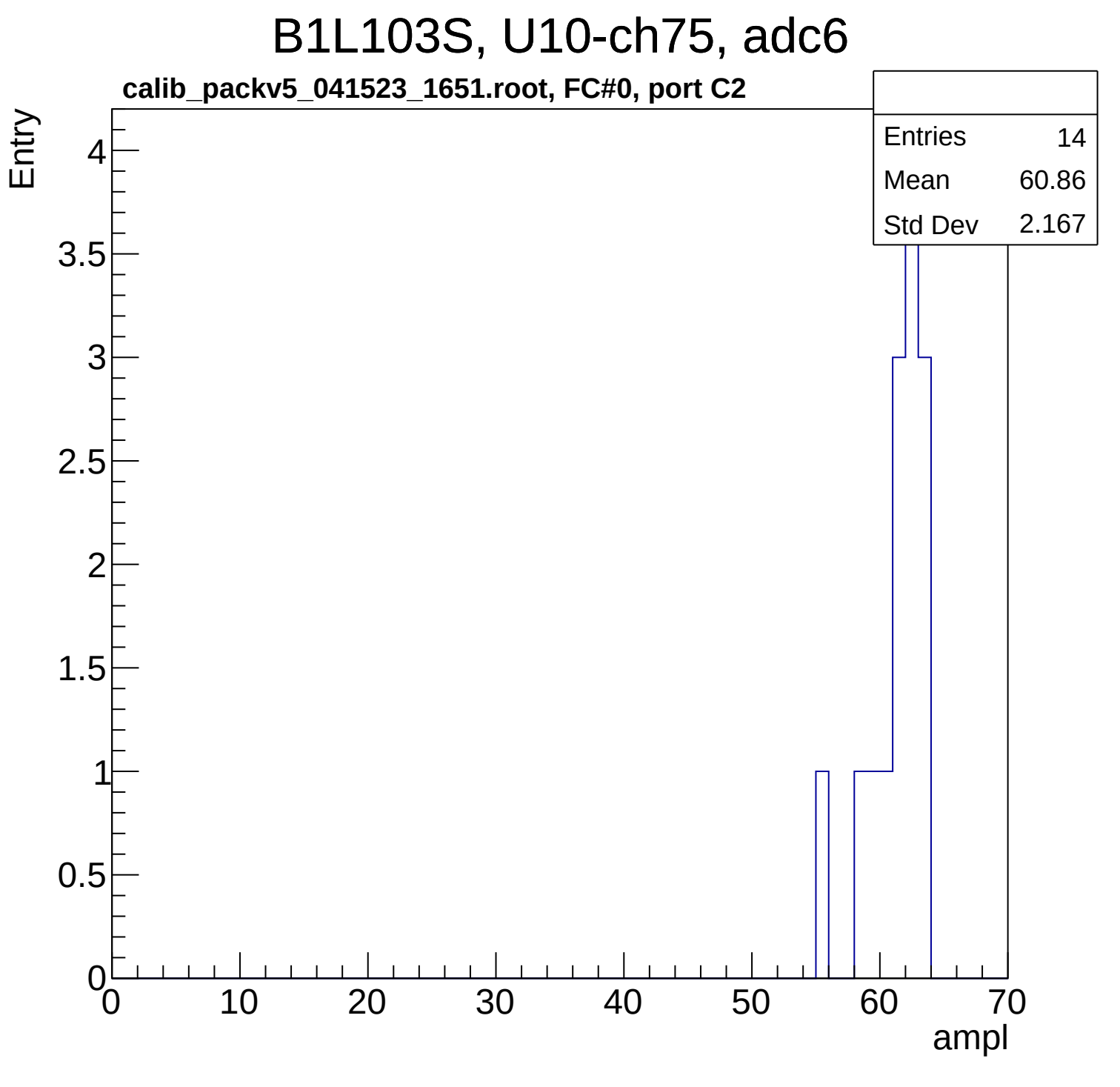
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U10-ch75, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 14
Mean 60.86
Std Dev 2.167
Entry
ampl
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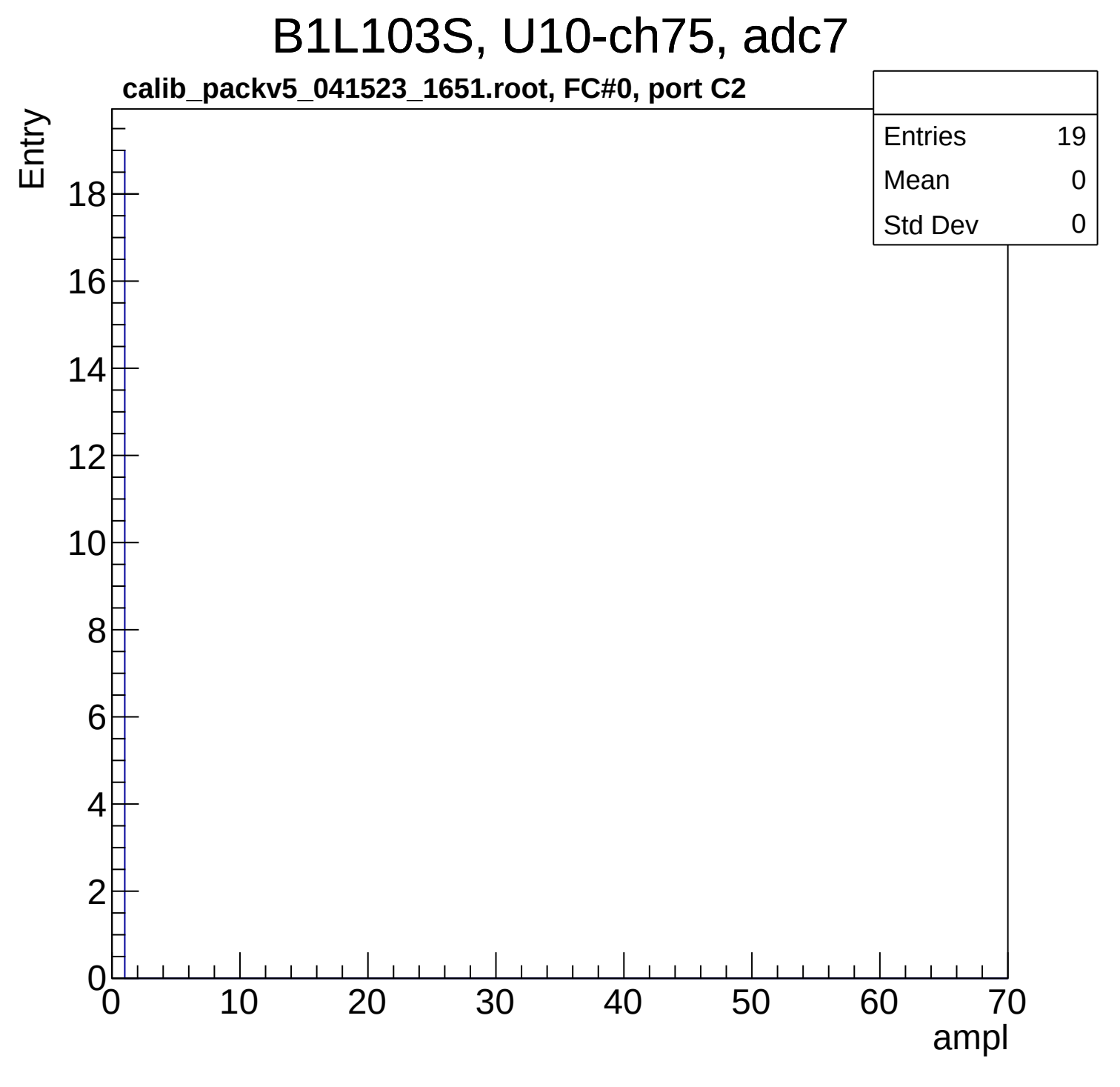
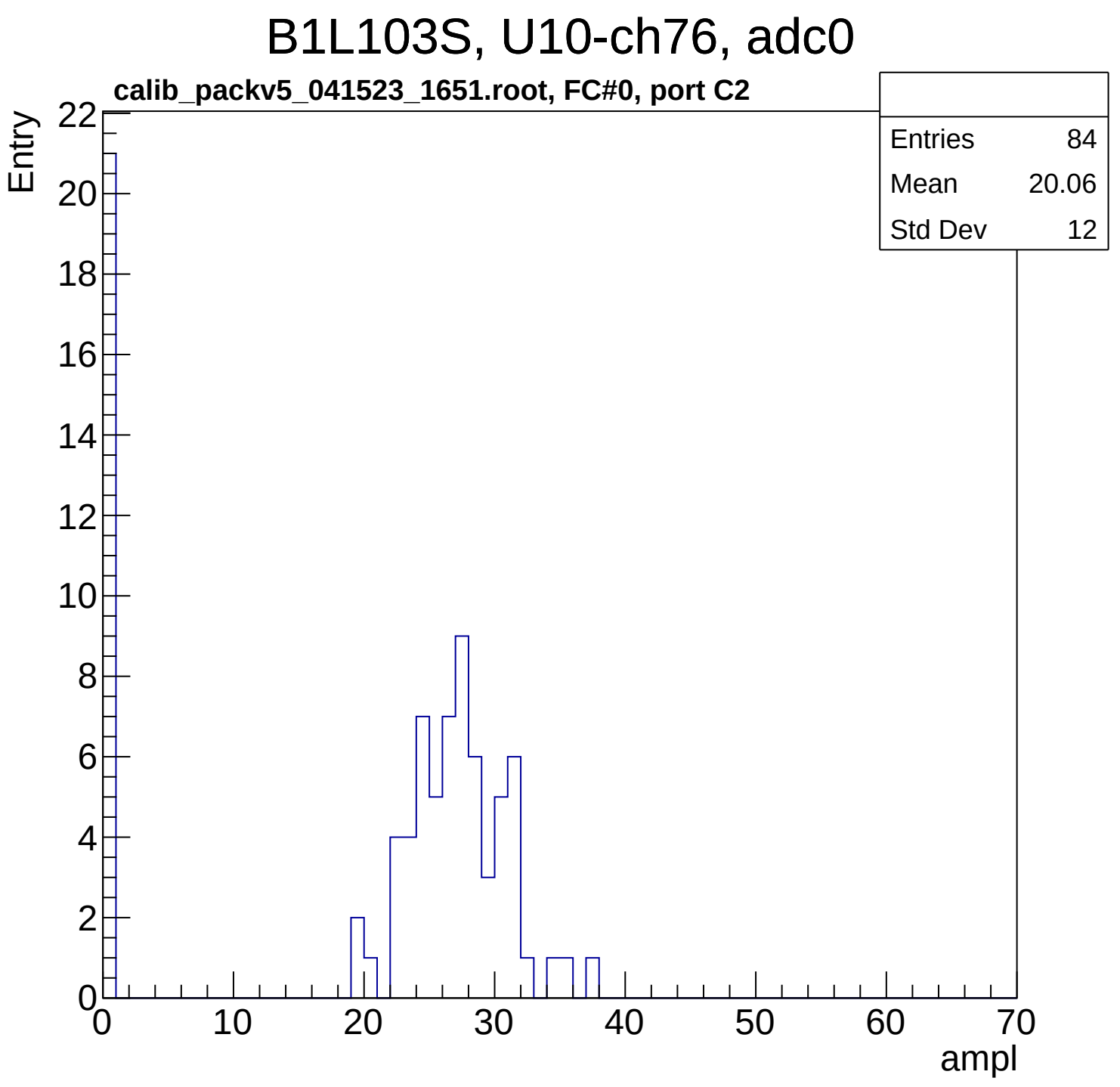
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U10-ch75, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch76, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 20.06
Std Dev 12
Entry
ampl
0
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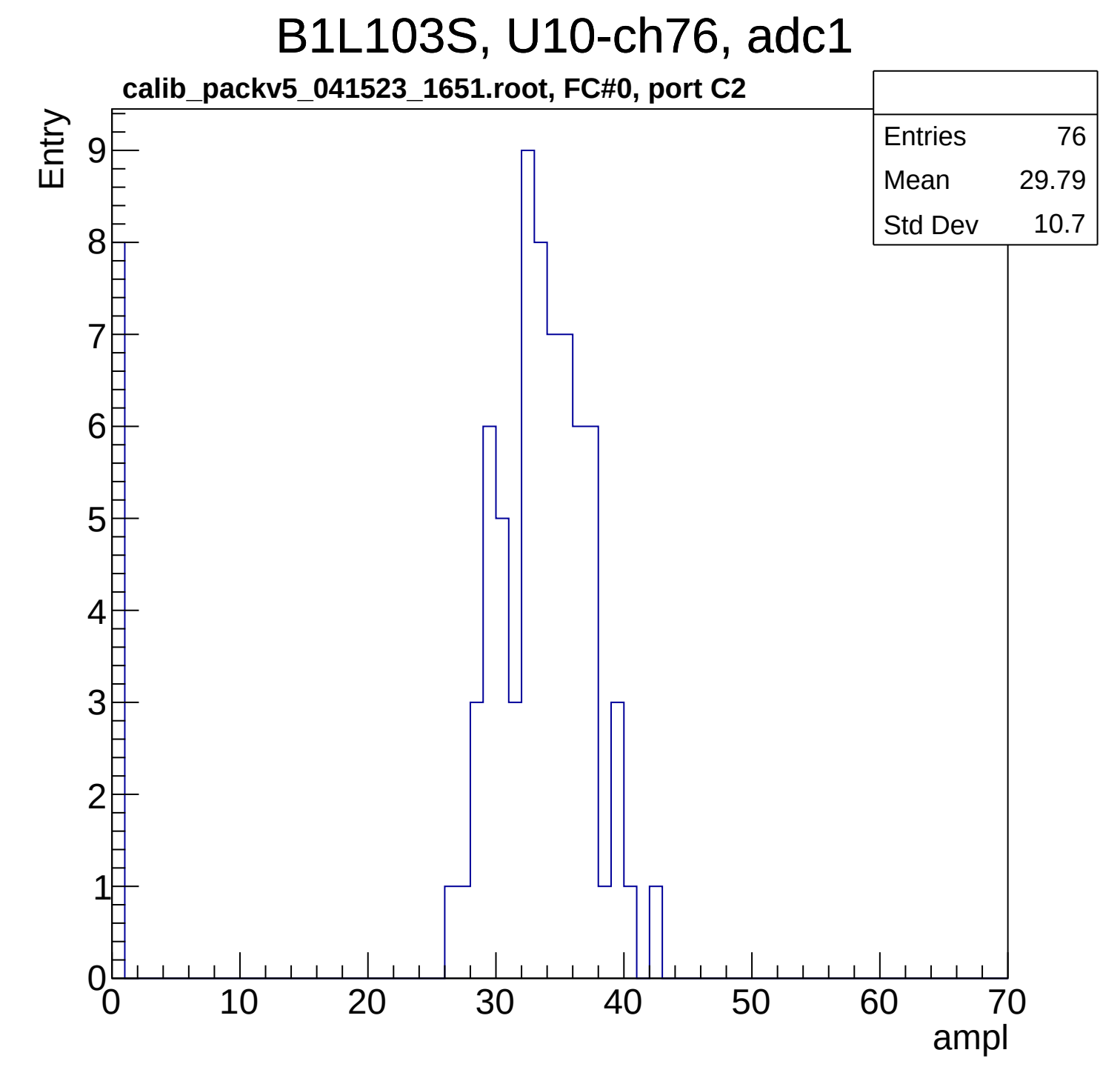
6
8
10
12
14
16
18
20
22
0
10
20
30
40
50
60
70


B1L103S, U10-ch76, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 29.79
Std Dev 10.7
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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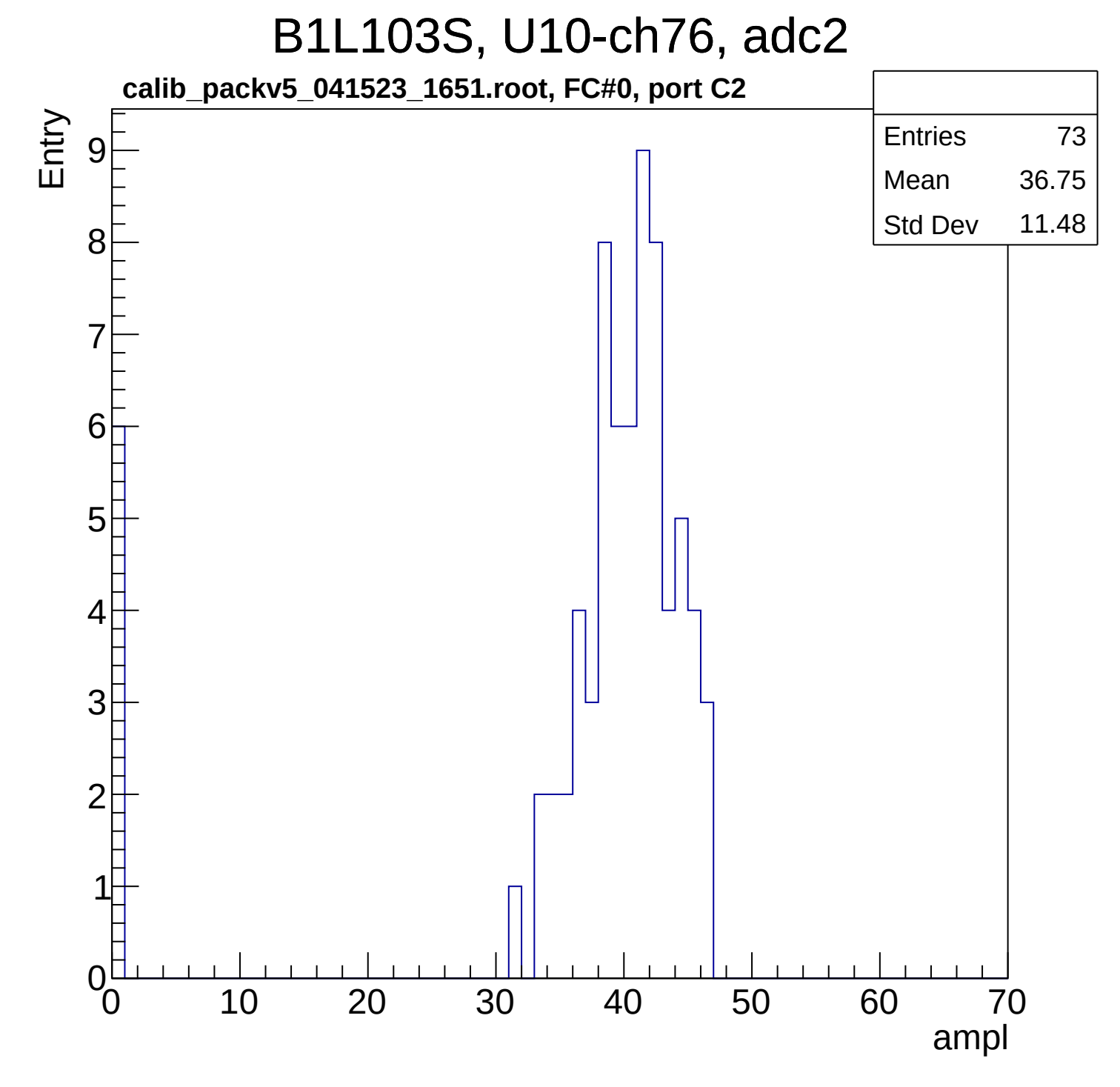
40
50
60
70


B1L103S, U10-ch76, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 36.75
Std Dev 11.48
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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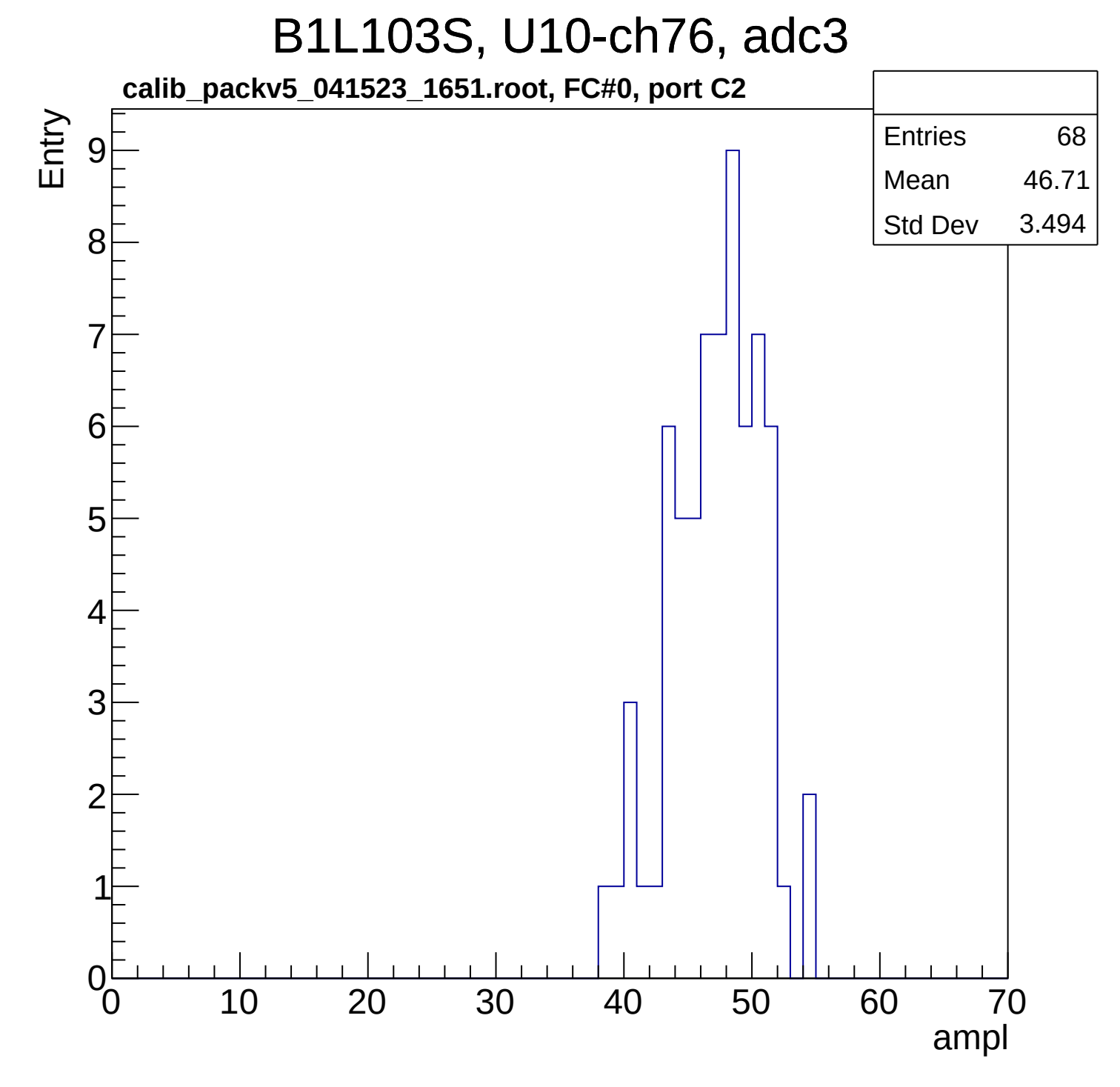
40
50
60
70


B1L103S, U10-ch76, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 46.71
Std Dev 3.494
Entry
ampl
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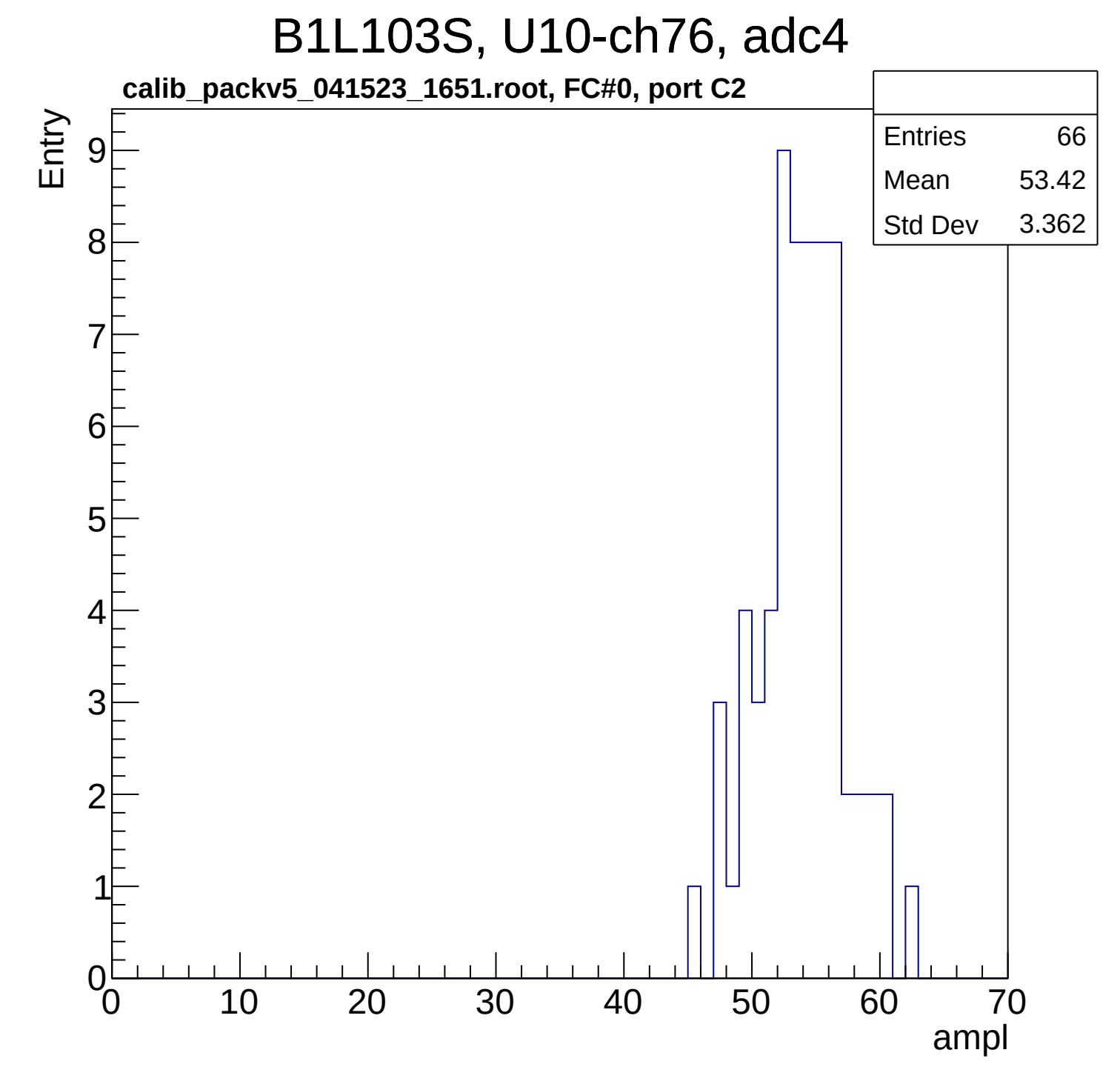
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U10-ch76, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 53.42
Std Dev 3.362
Entry
ampl
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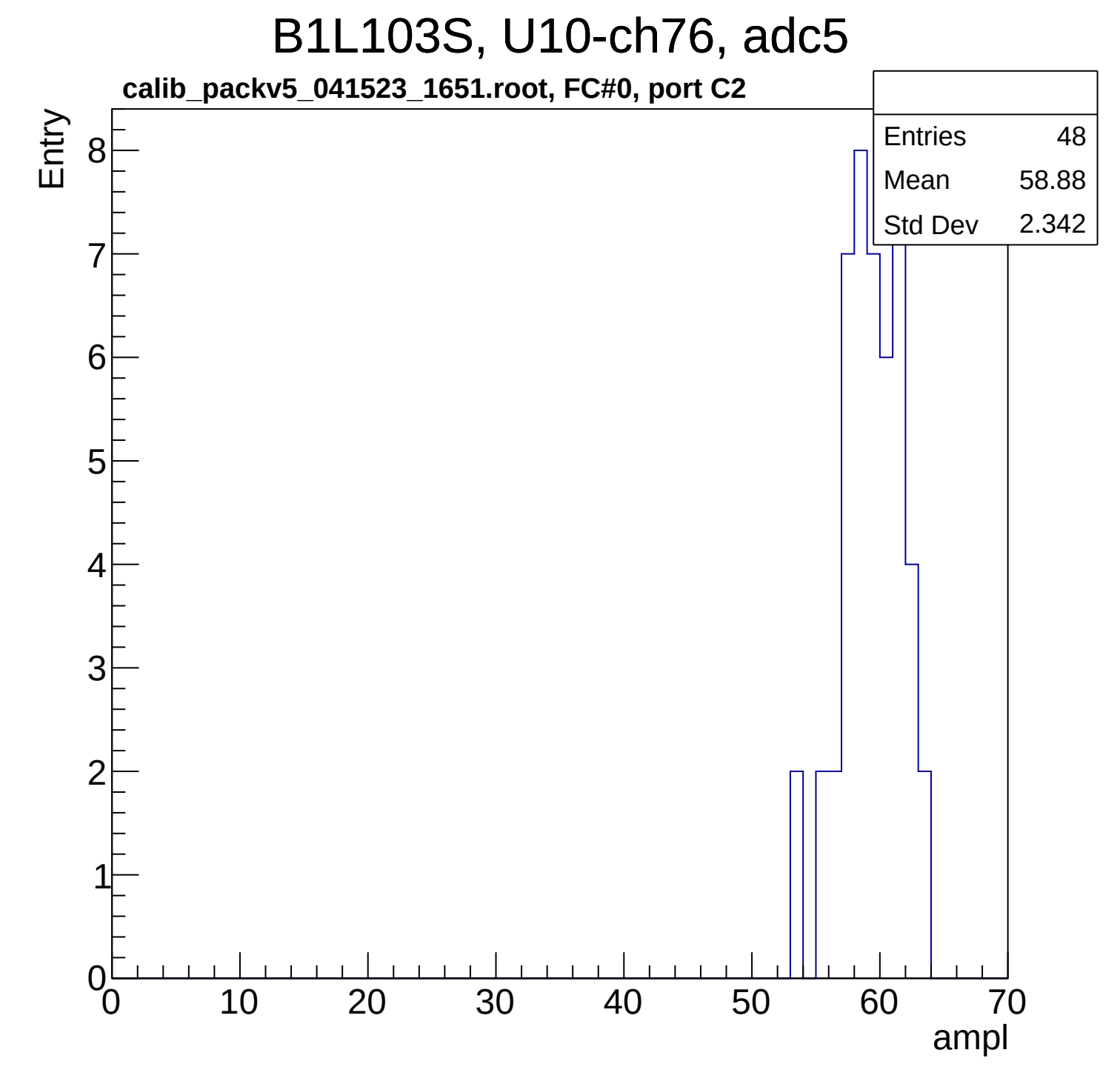
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U10-ch76, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 58.88
Std Dev 2.342
Entry
ampl
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1
2
3
4
5
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7
8
0
10
20
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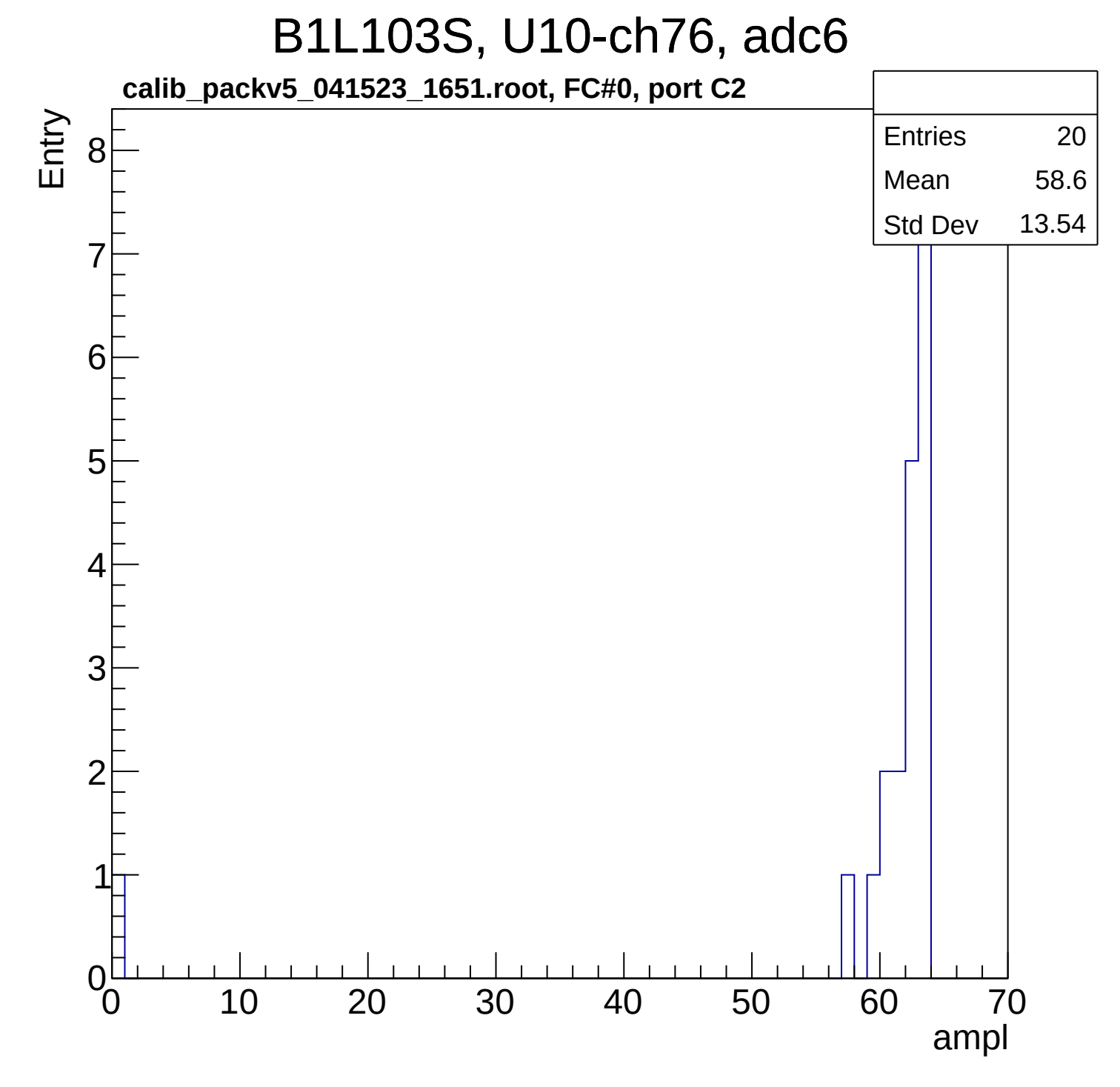
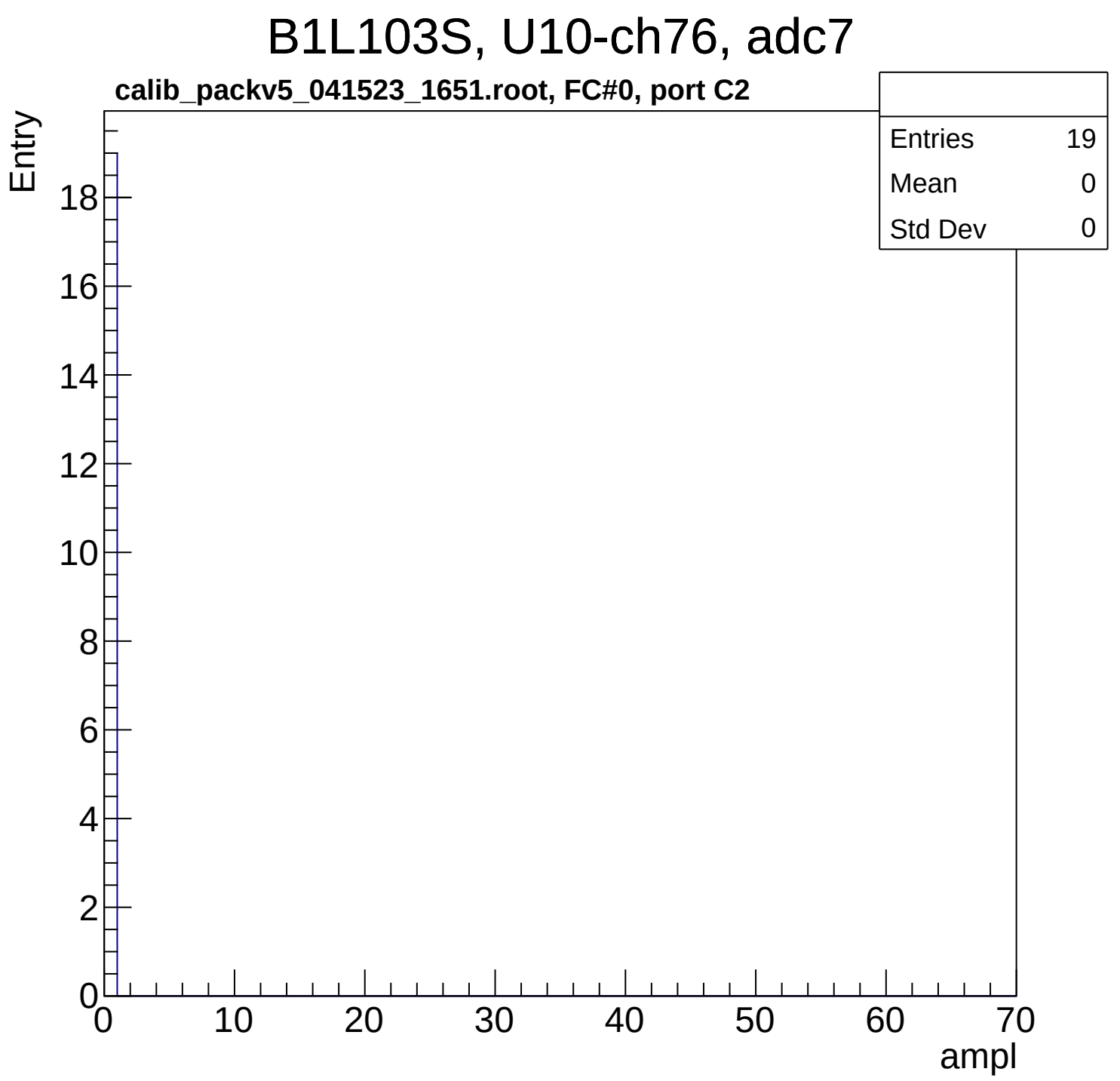
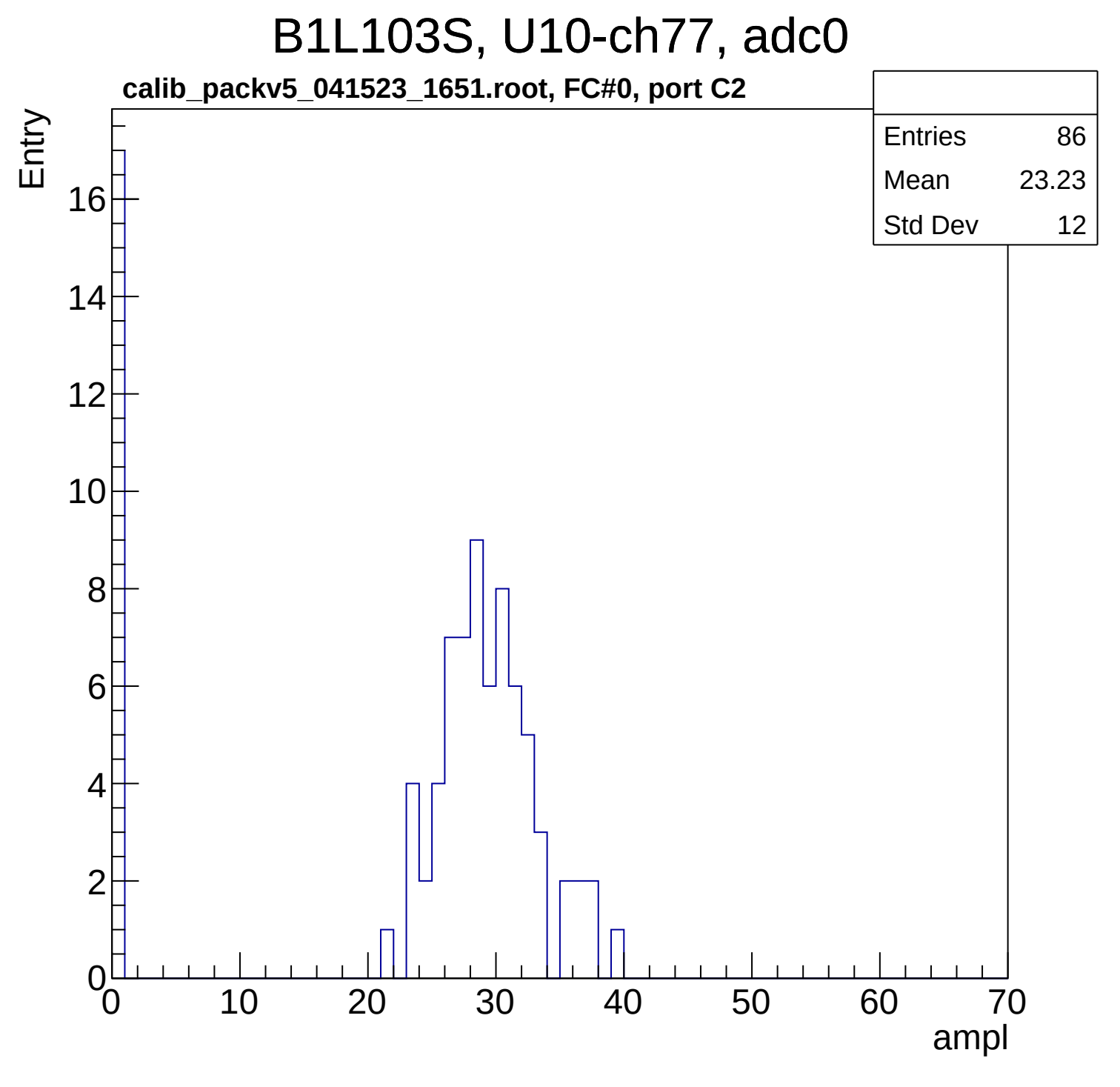
40
50
60
70


B1L103S, U10-ch76, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 58.6
Std Dev 13.54
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U10-ch76, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch77, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 23.23
Std Dev 12
Entry
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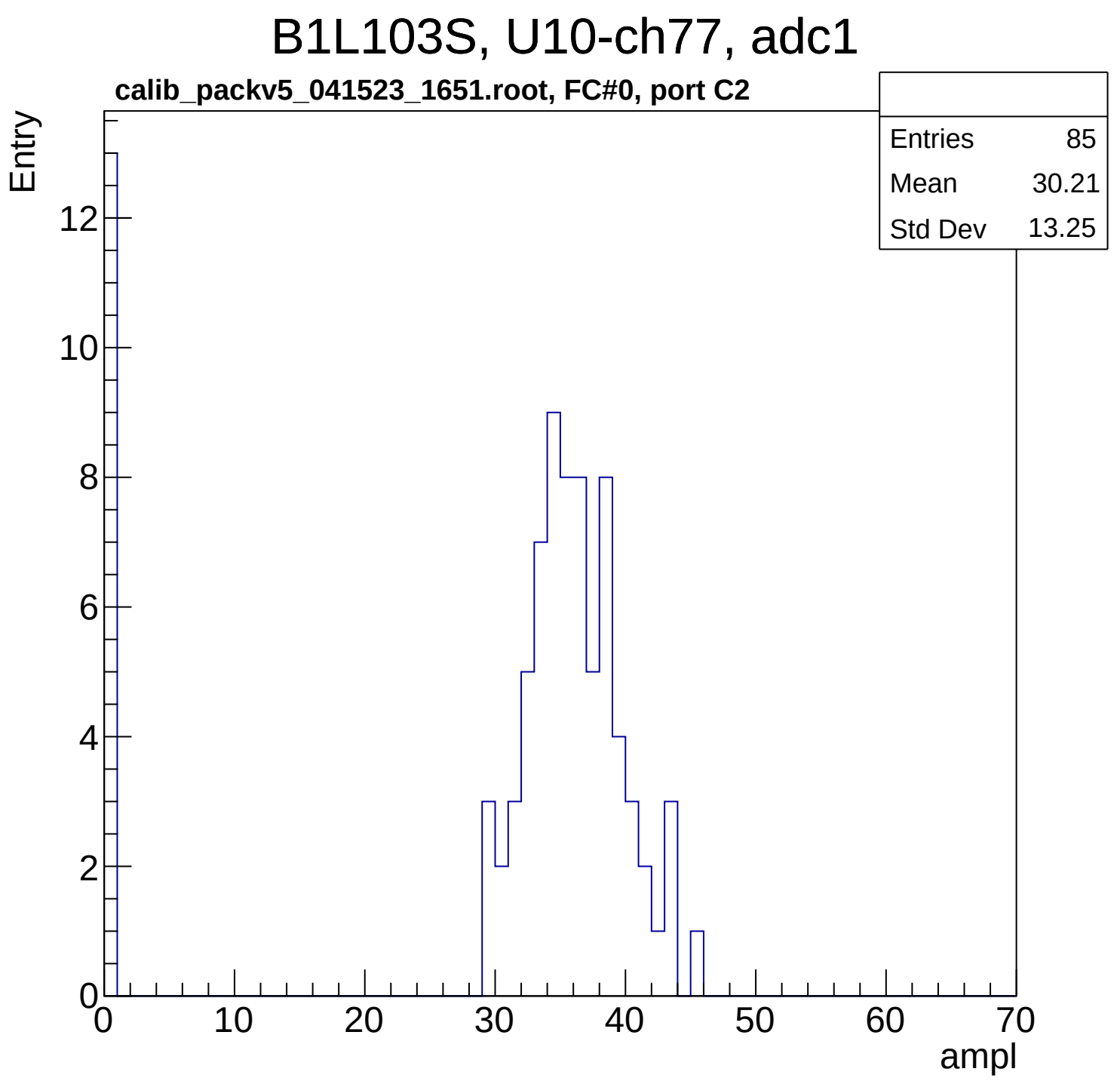
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch77, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 30.21
Std Dev 13.25
Entry
0
2
4
6
8
10
12
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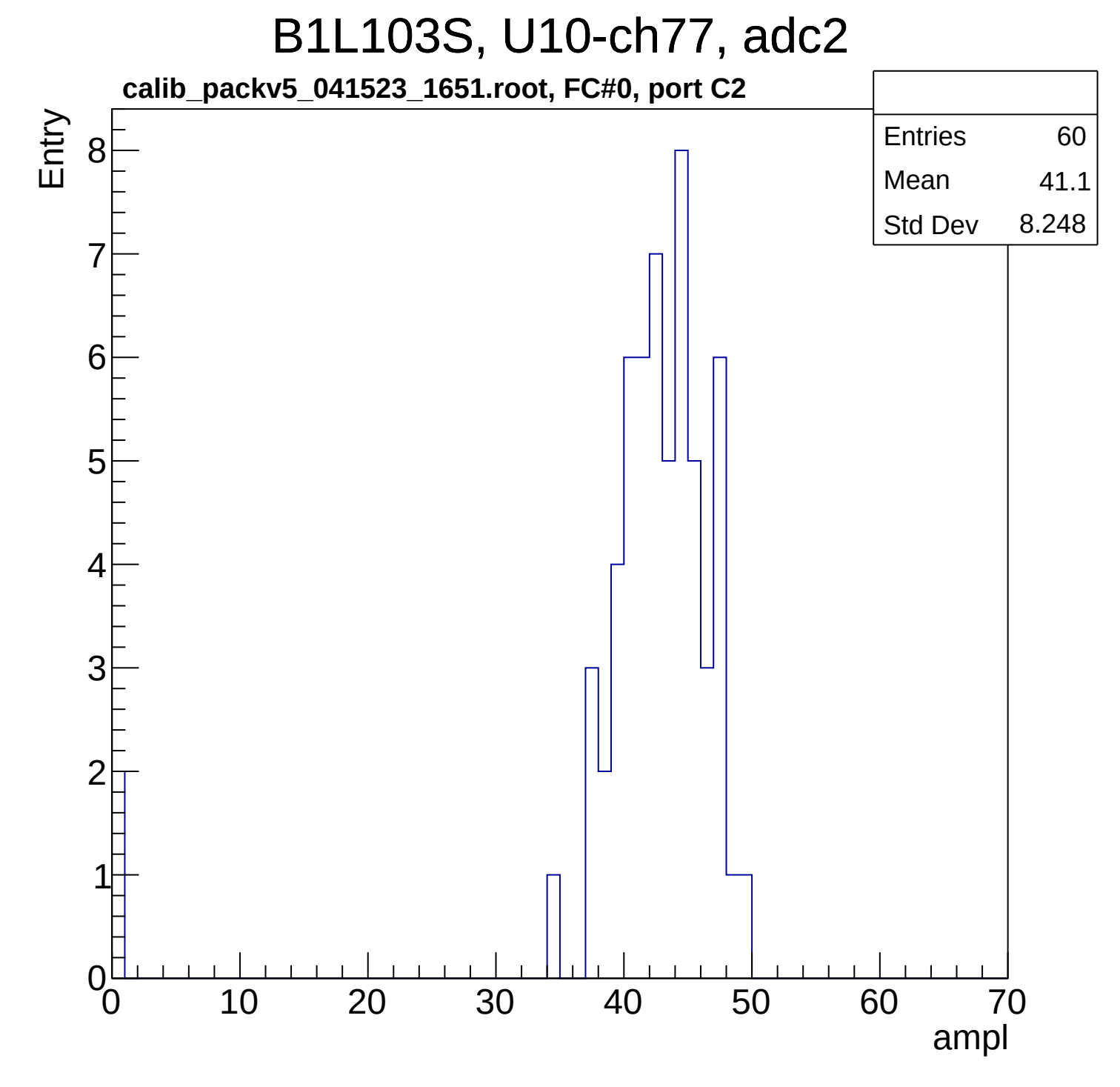
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch77, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 41.1
Std Dev 8.248
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
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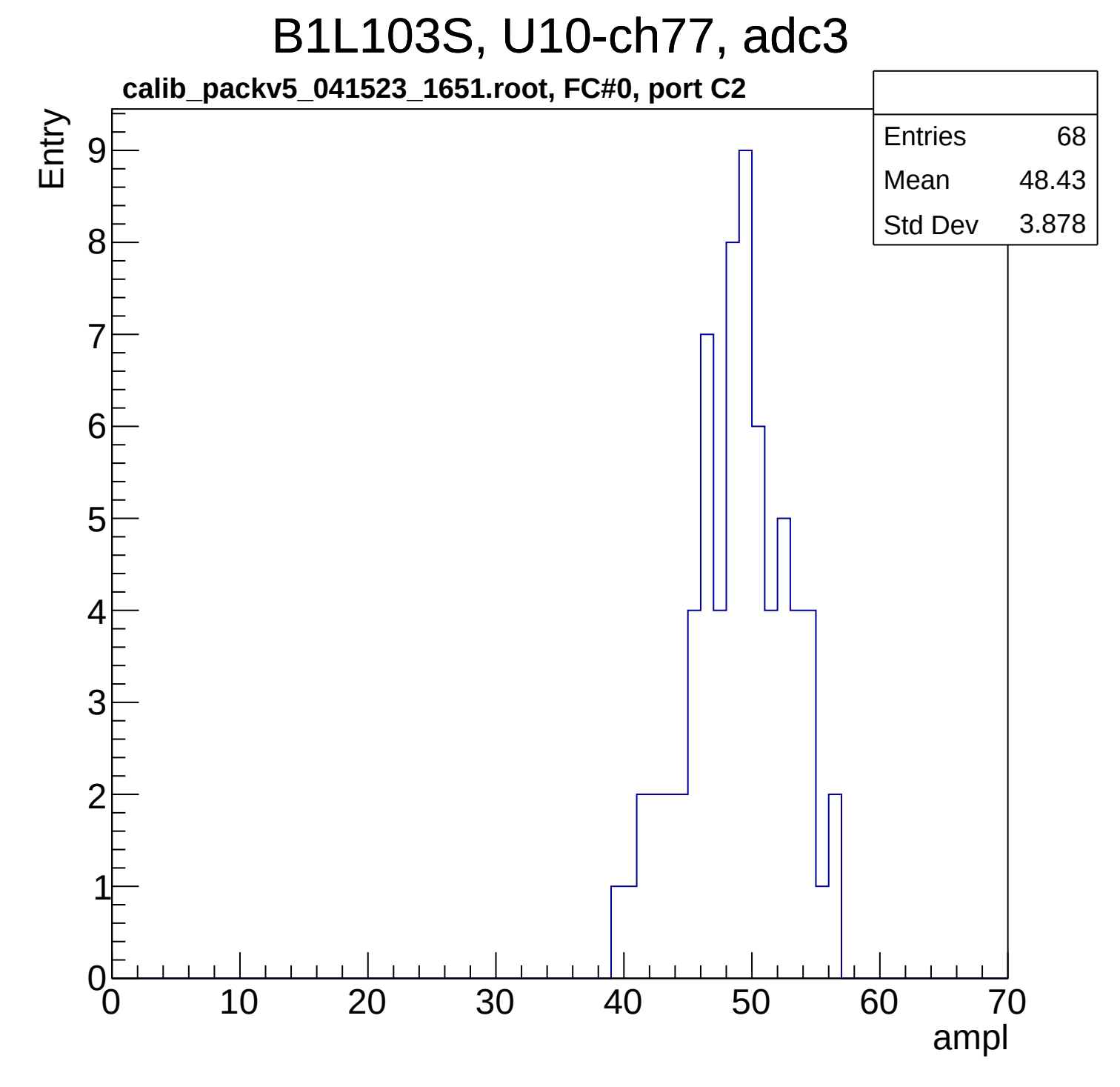
40
50
60
70


B1L103S, U10-ch77, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 48.43
Std Dev 3.878
Entry
ampl
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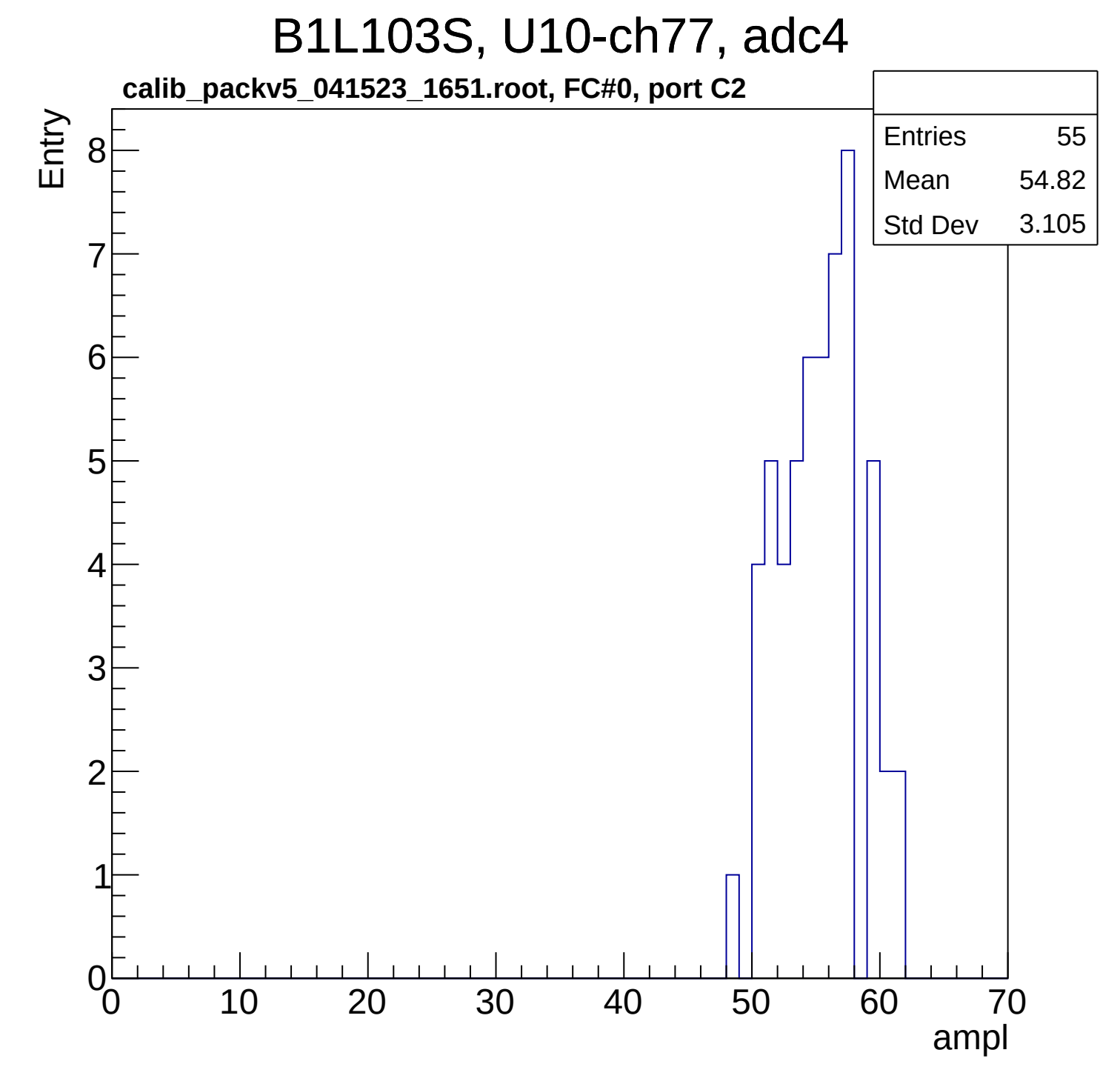
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U10-ch77, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 54.82
Std Dev 3.105
Entry
ampl
0
1
2
3
4
5
6
7
8
0
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40
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60
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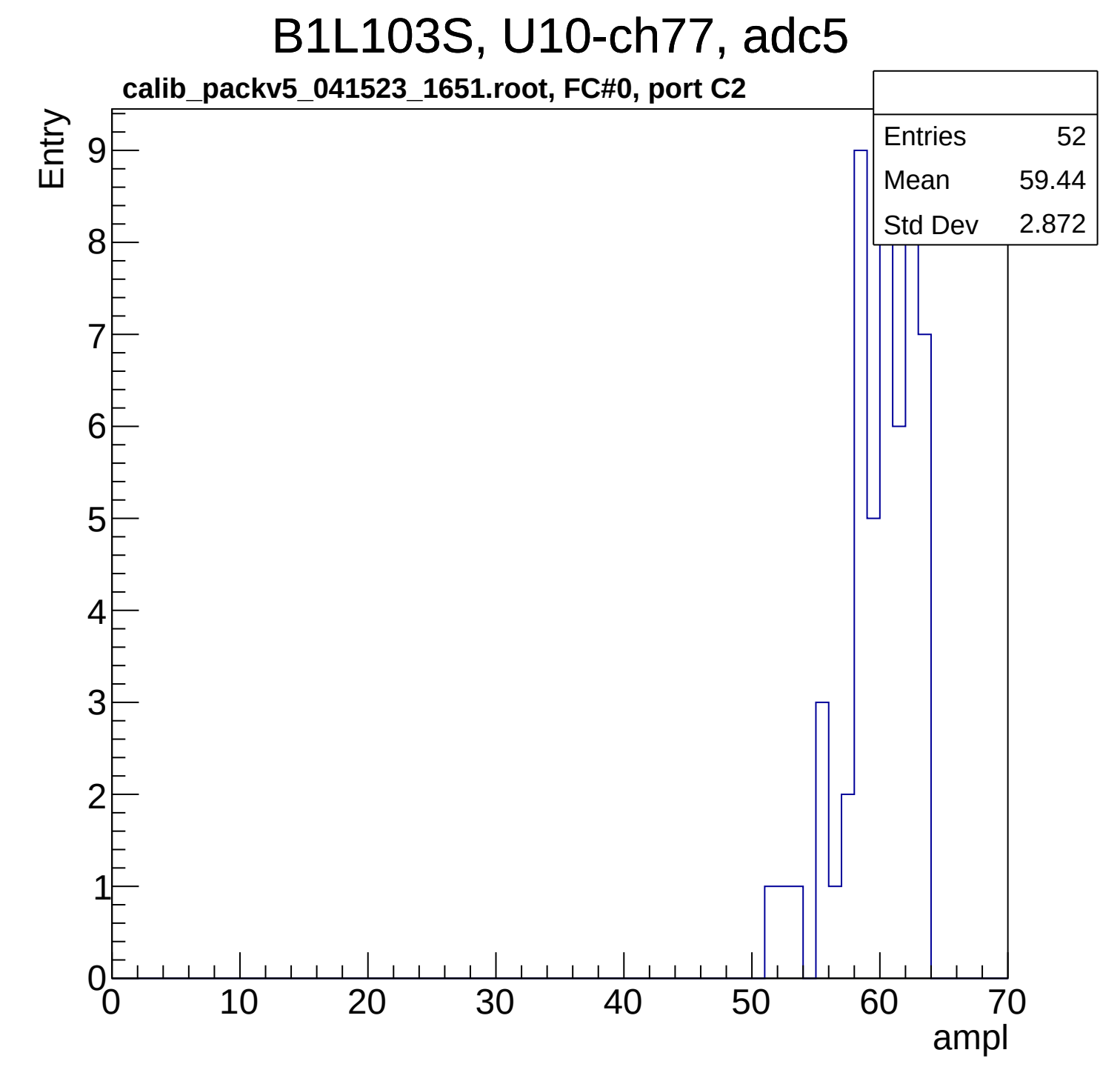
B1L103S, U10-ch77, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 59.44
Std Dev 2.872
Entry
ampl
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2
3
4
5
6
7
8
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0
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60
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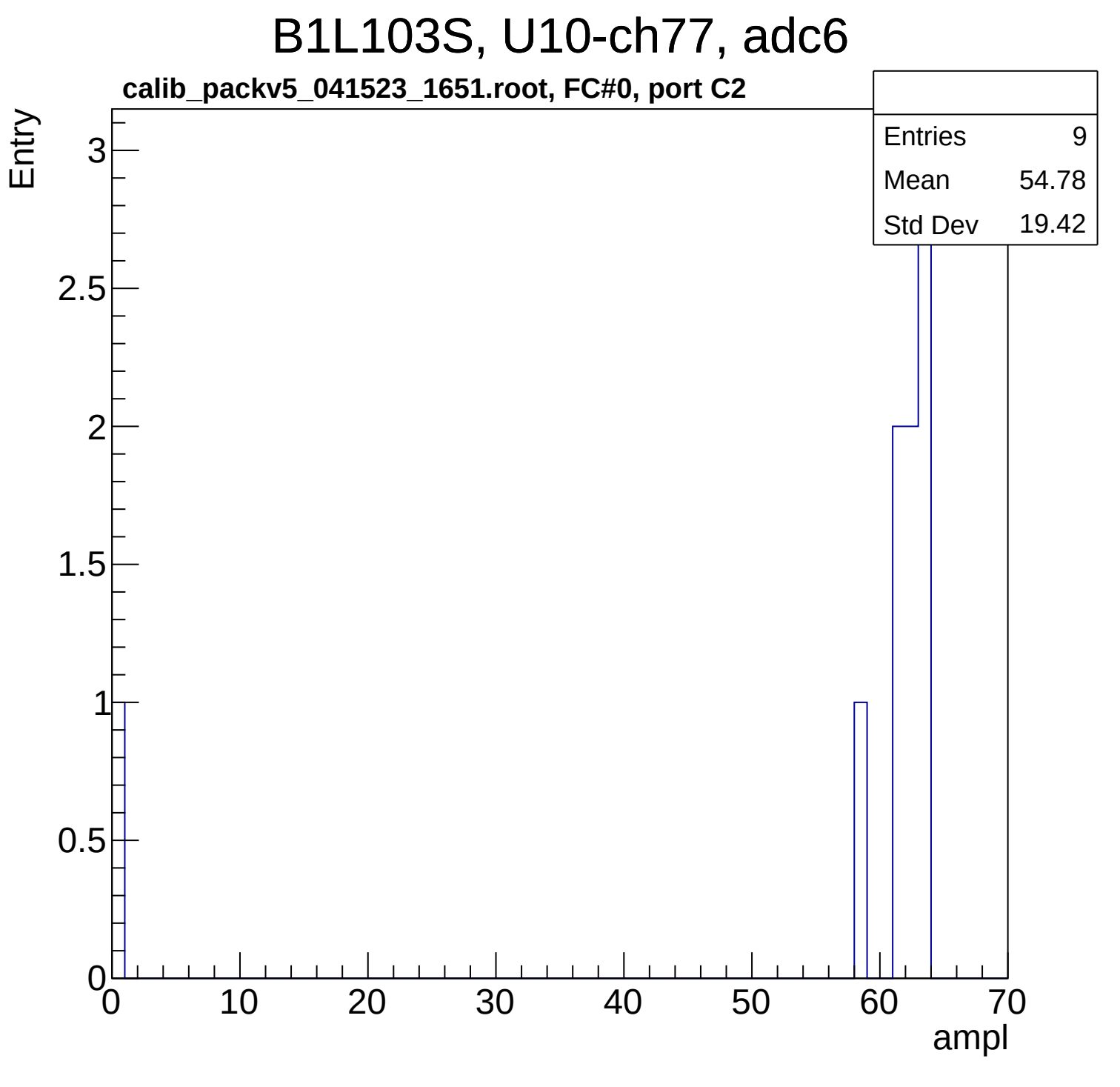
B1L103S, U10-ch77, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 9
Mean 54.78
Std Dev 19.42
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
10
20
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40
50
60
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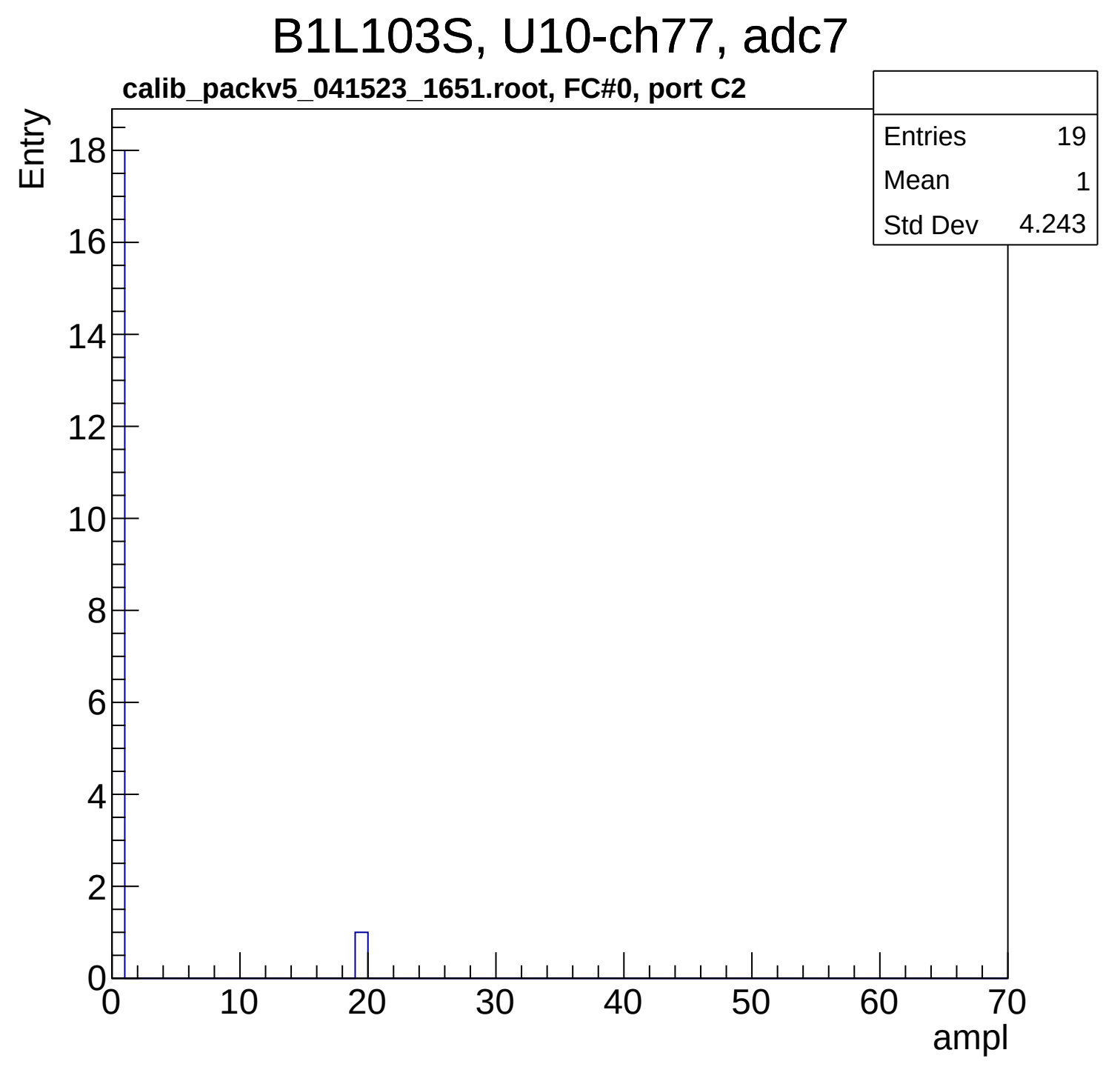
B1L103S, U10-ch77, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1
Std Dev 4.243
Entry
0
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6
8
10
12
14
16
18
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10
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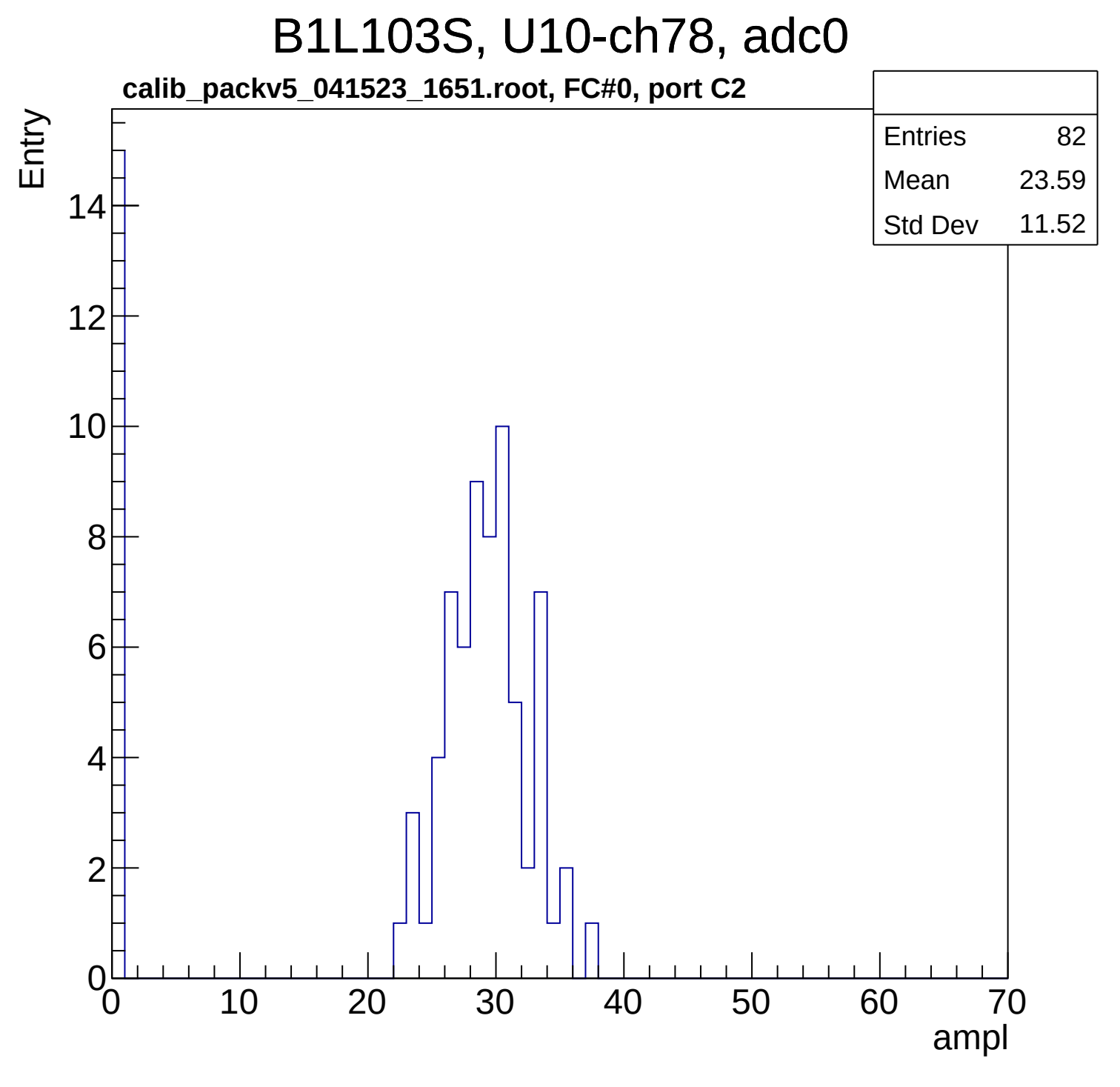
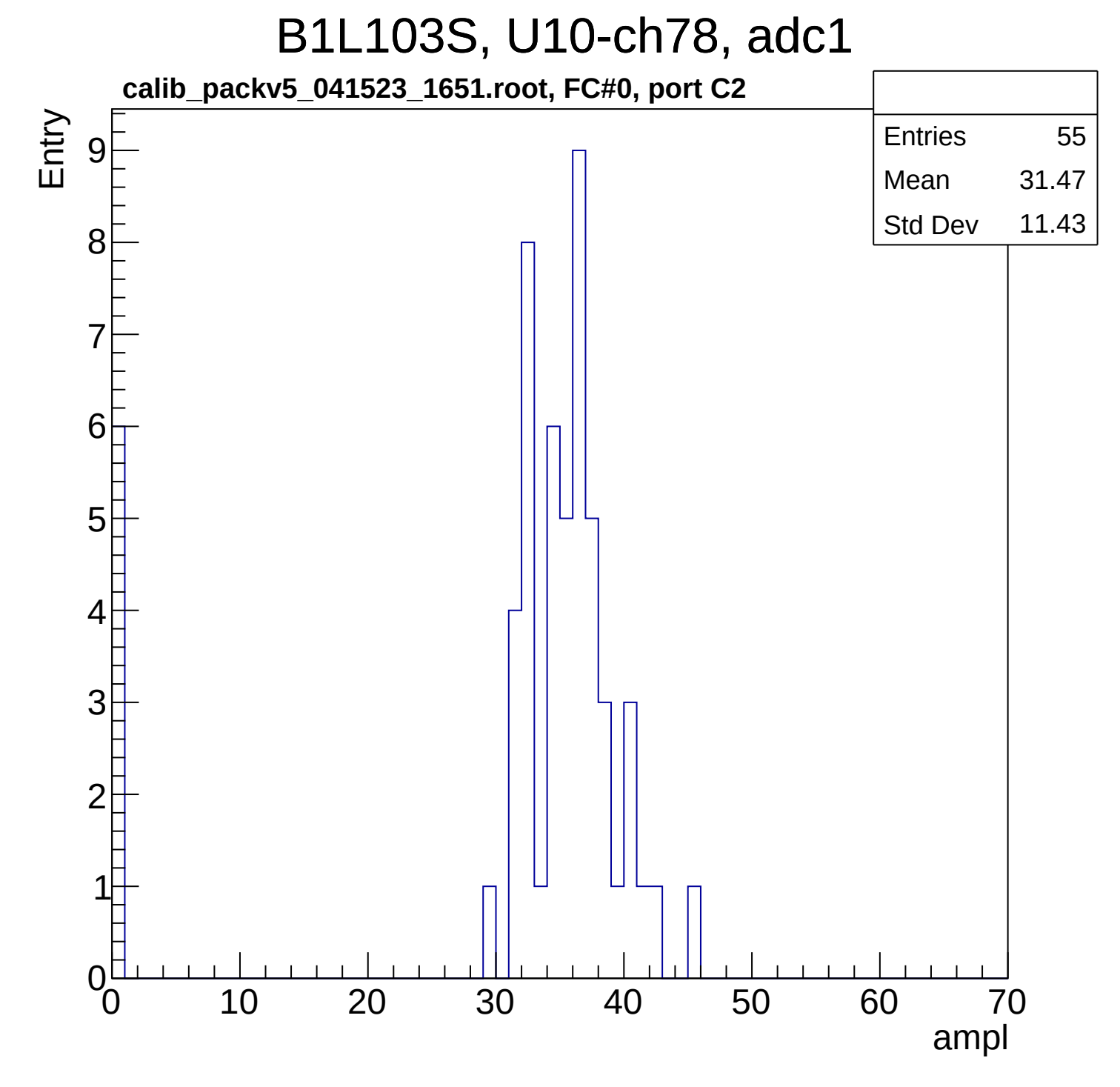
50
60
70
ampl


B1L103S, U10-ch78, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 23.59
Std Dev 11.52
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch78, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 31.47
Std Dev 11.43
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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40
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60
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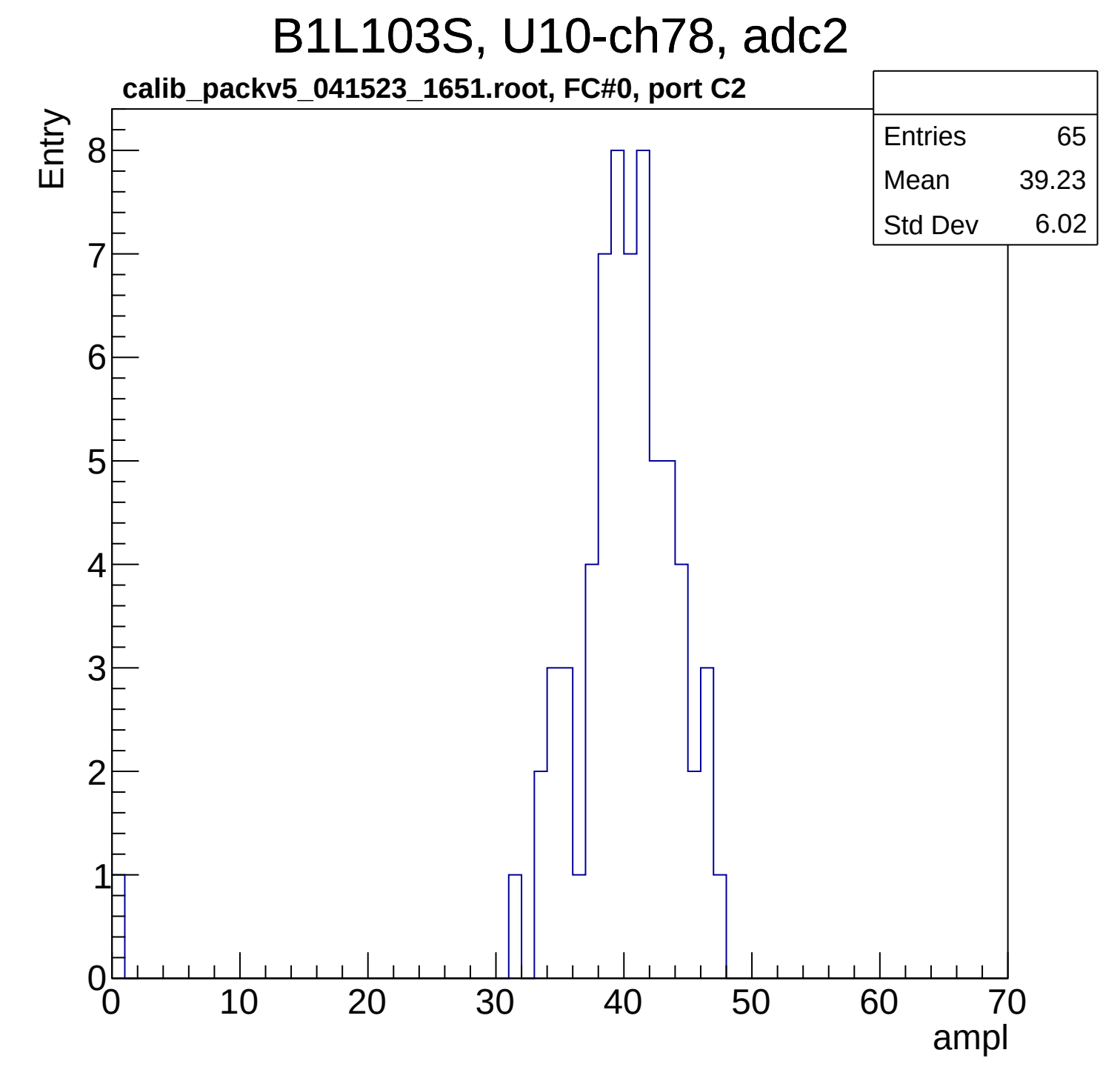
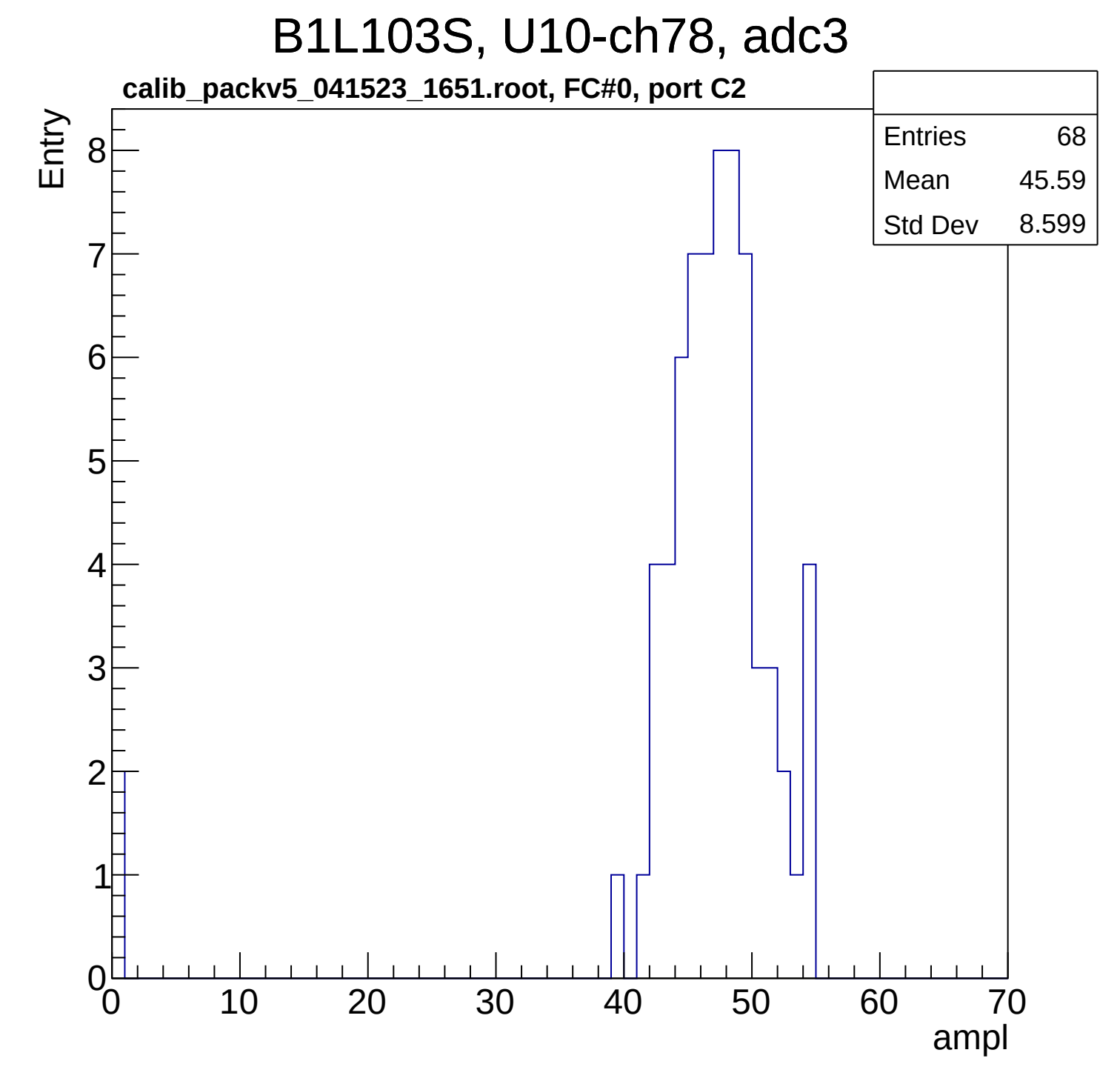

B1L103S, U10-ch78, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 39.23
Std Dev 6.02
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U10-ch78, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 45.59
Std Dev 8.599
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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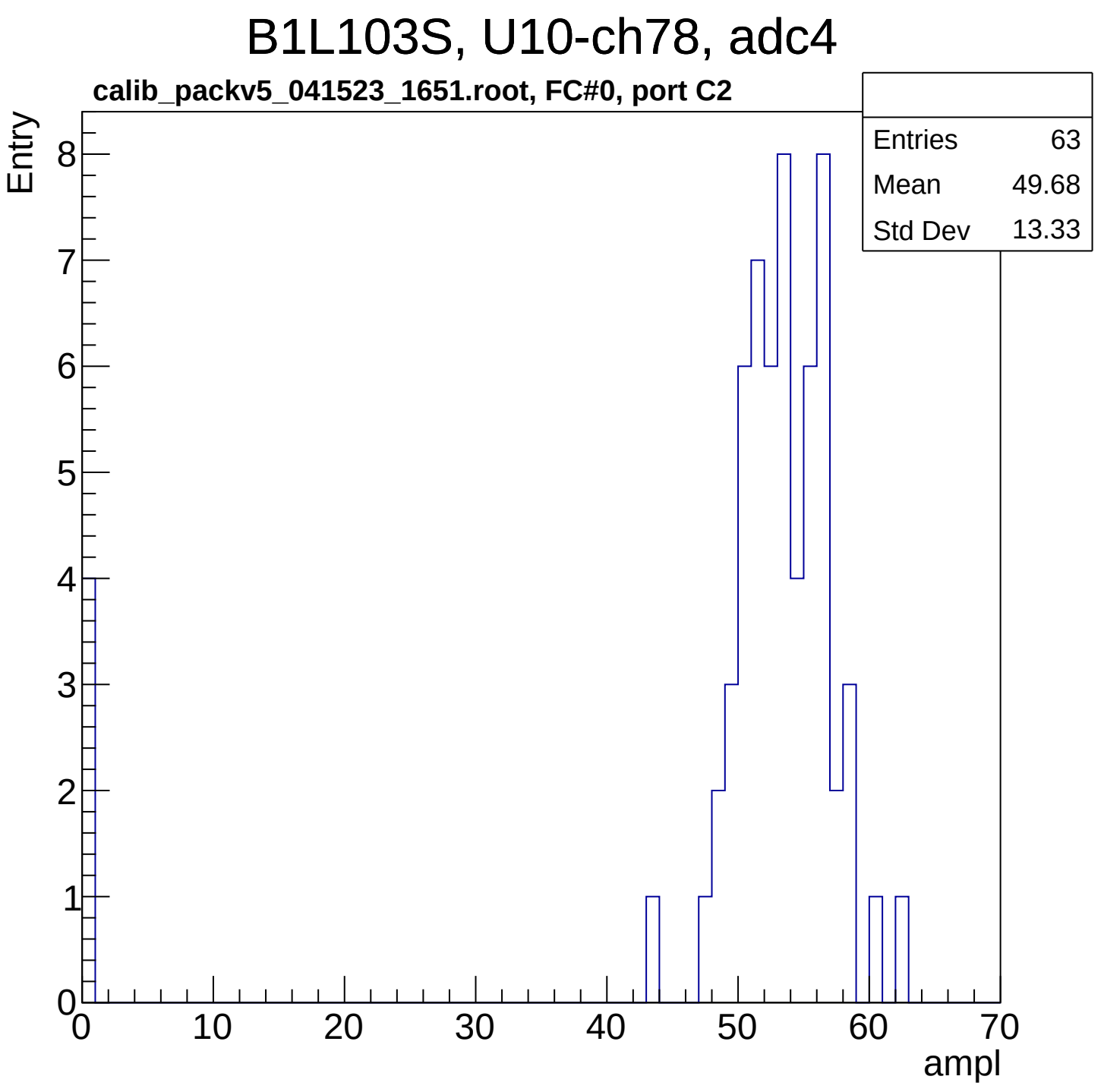
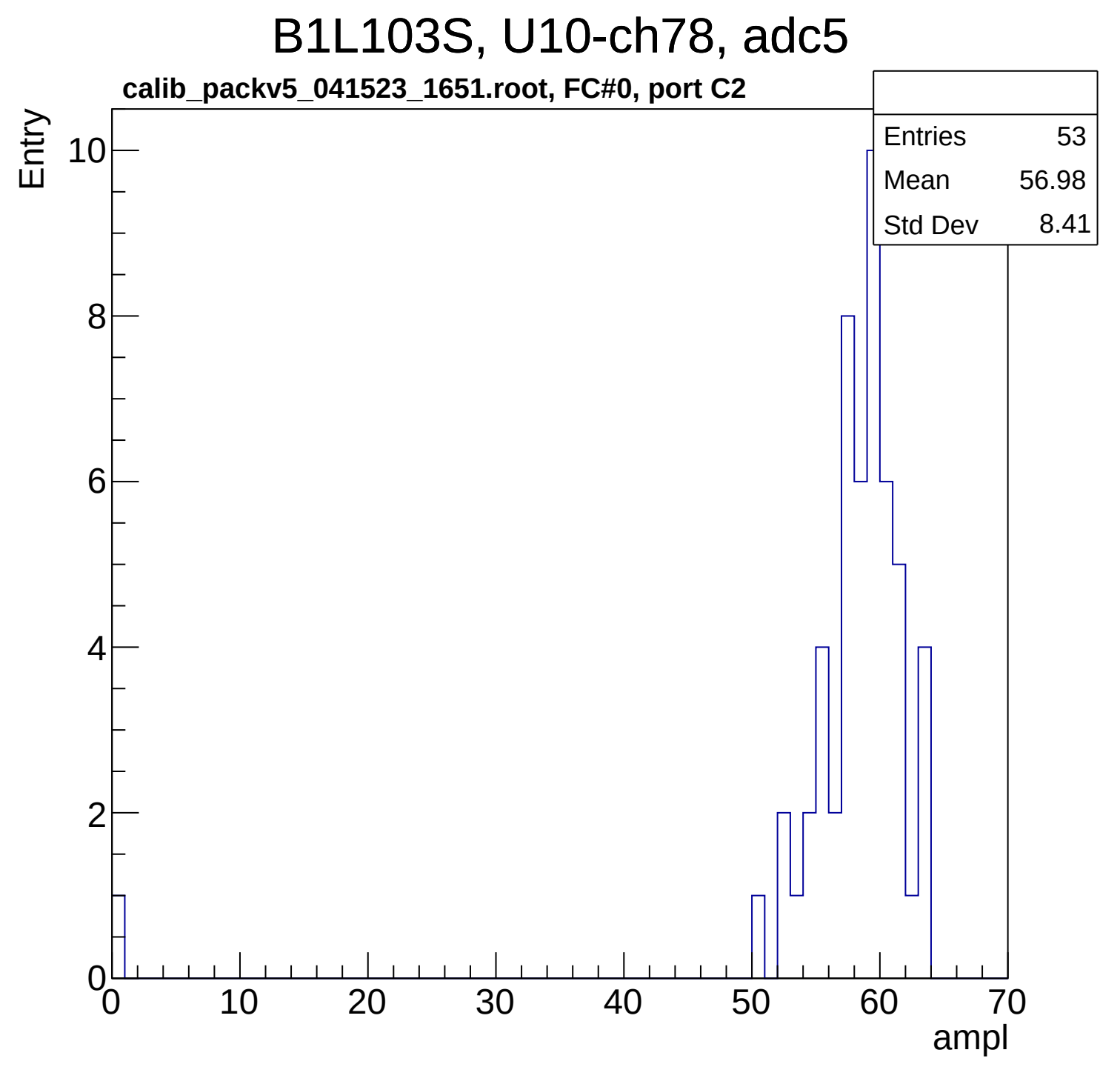
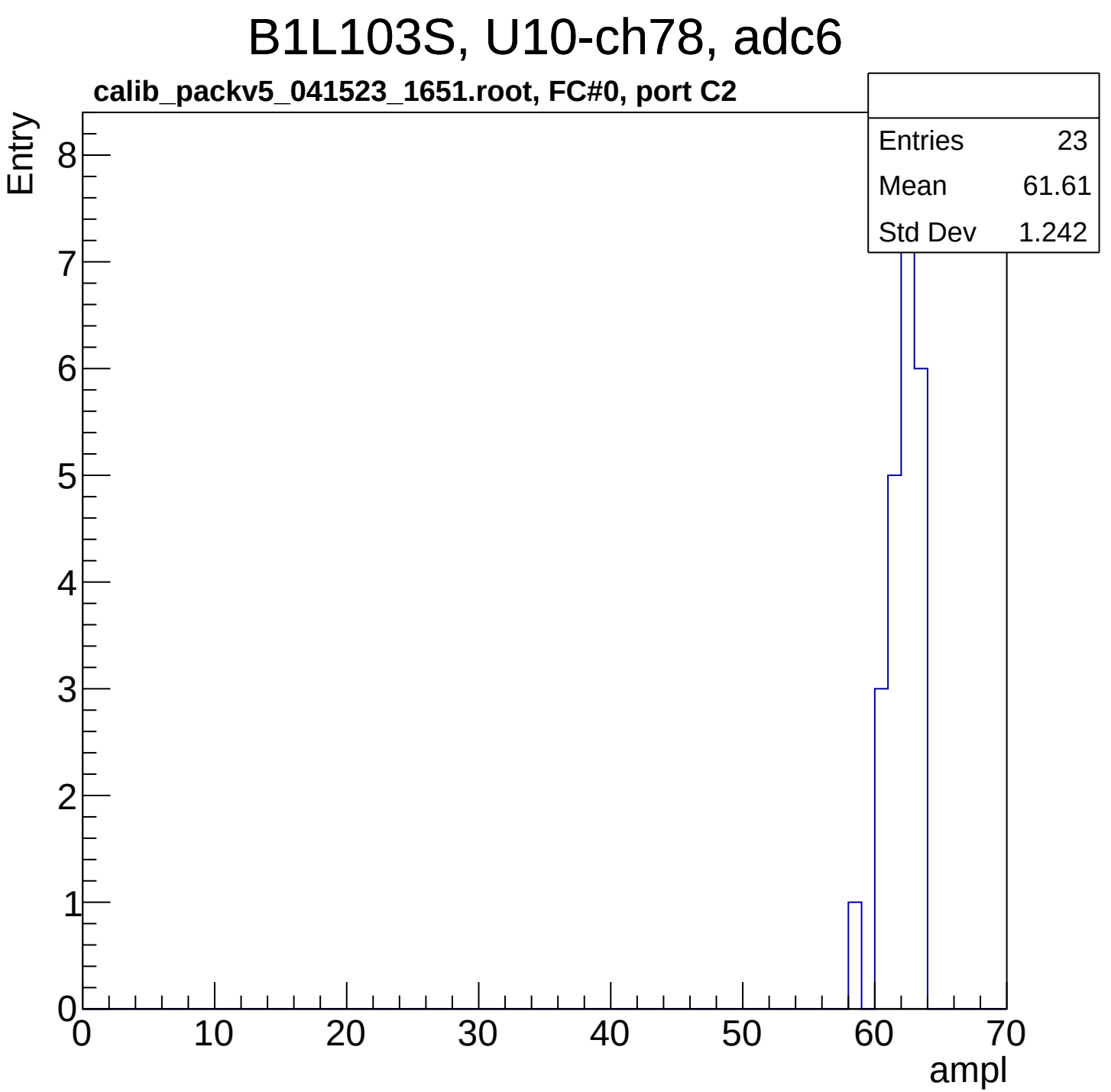
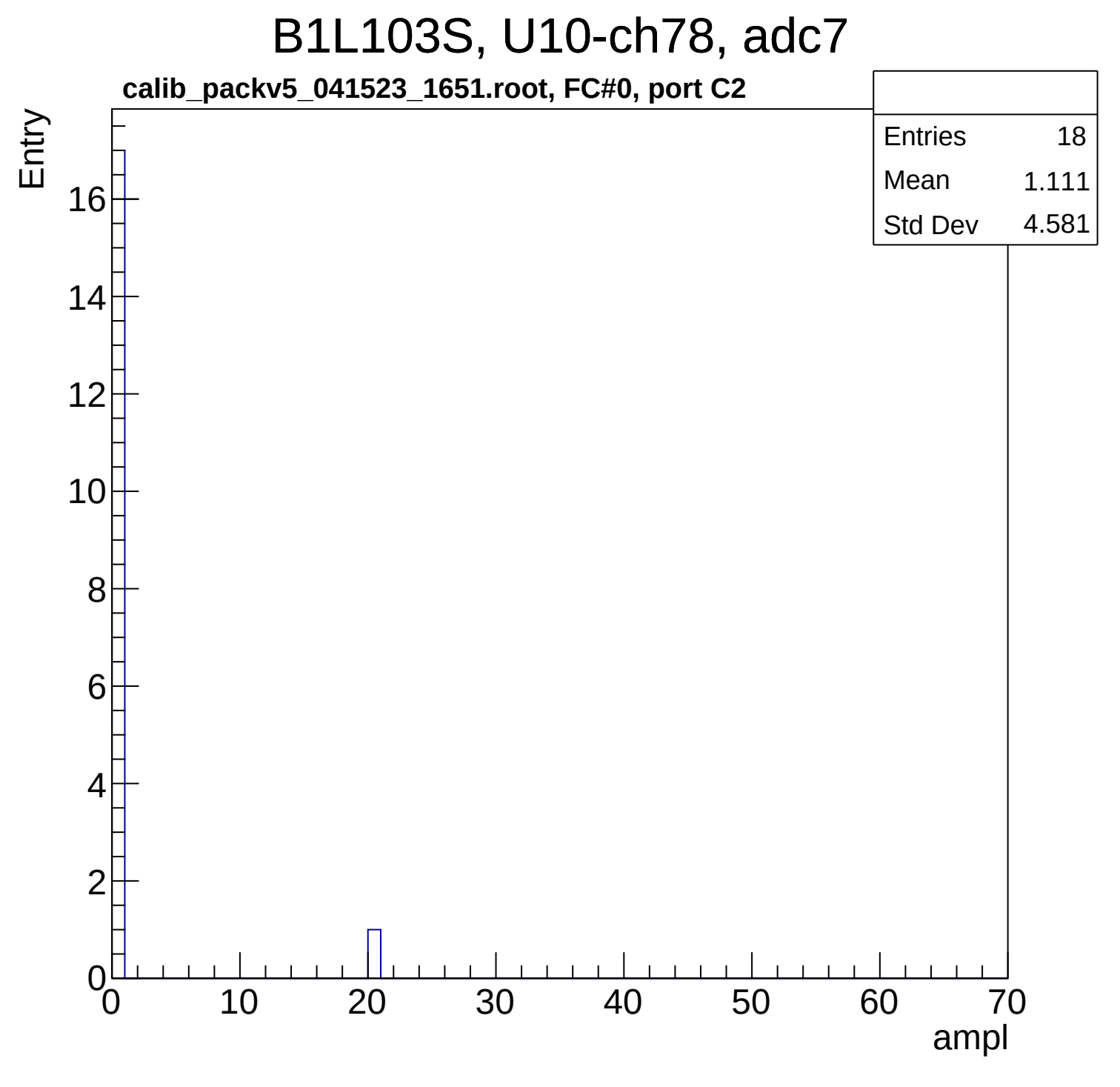
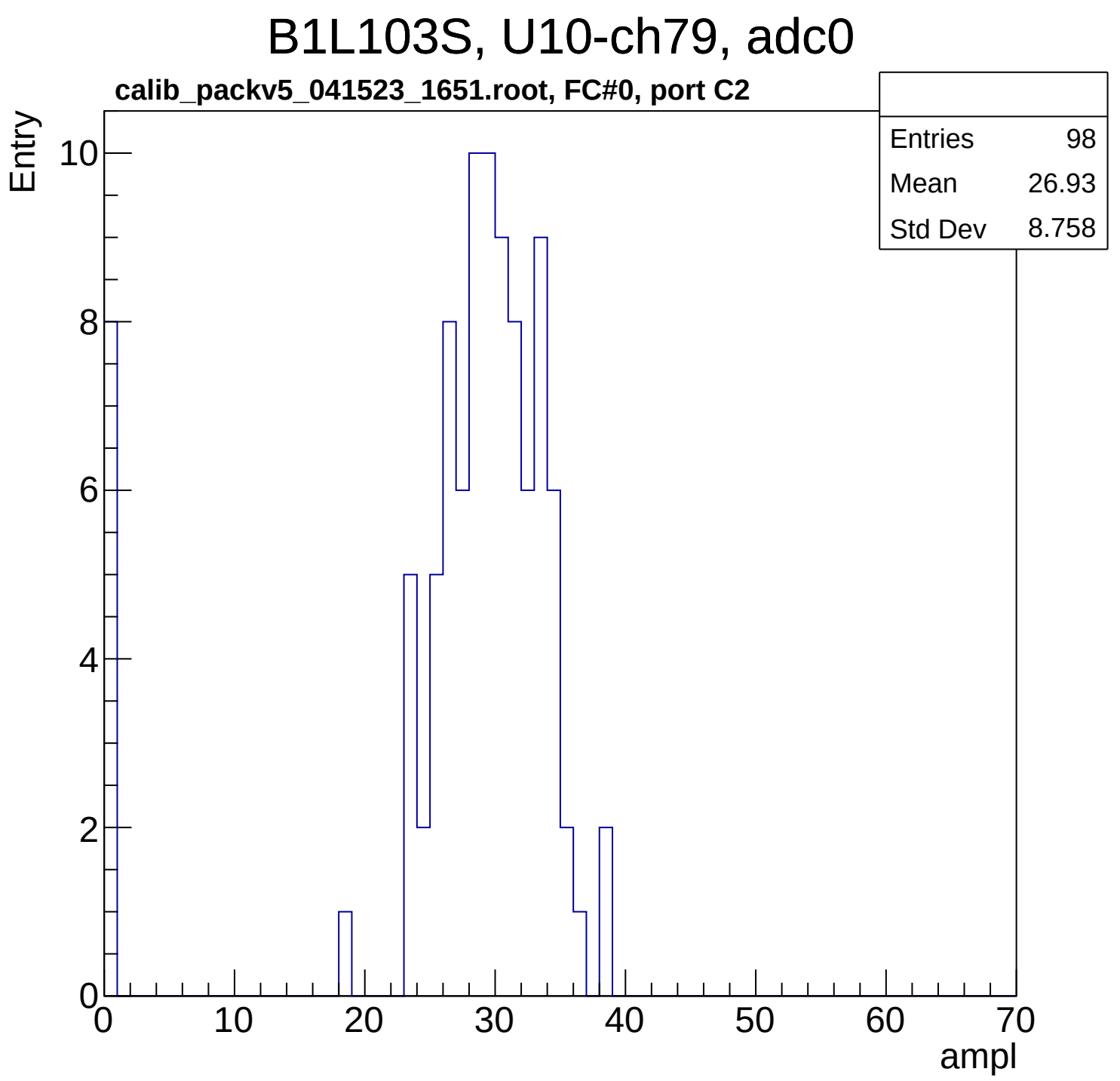
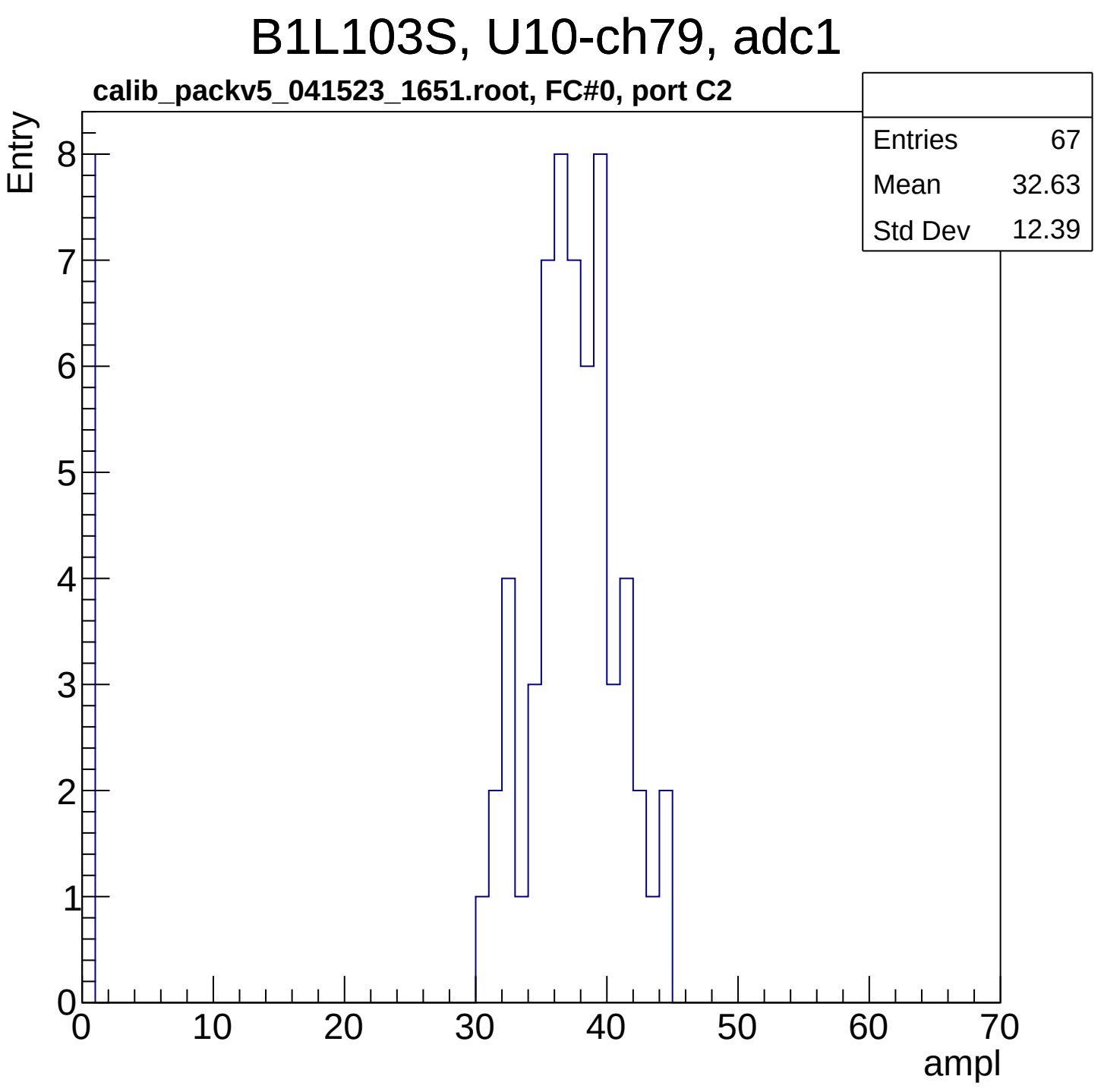

B1L103S, U10-ch78, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 49.68
Std Dev 13.33
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

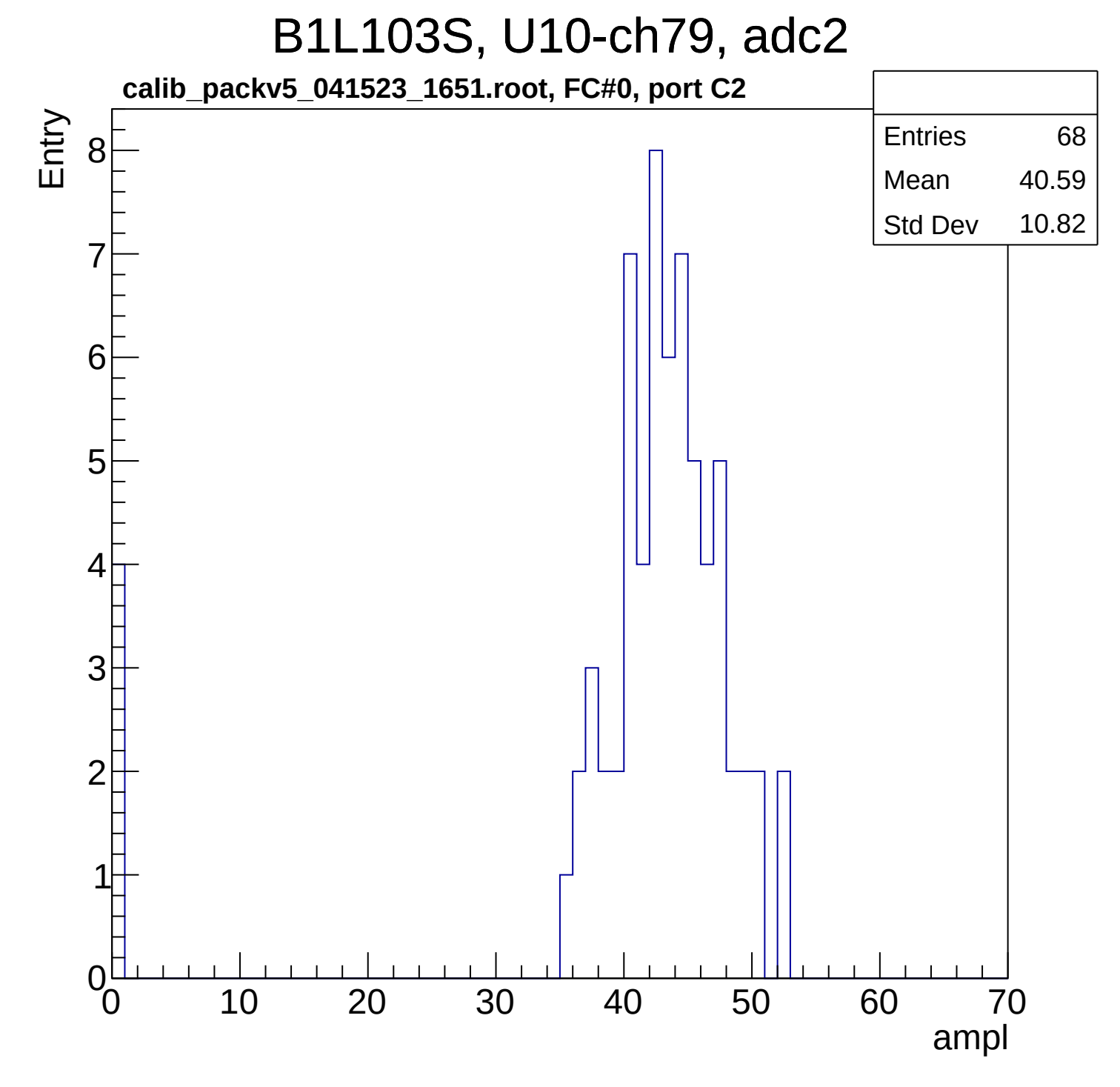

B1L103S, U10-ch78, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 56.98
Std Dev 8.41
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

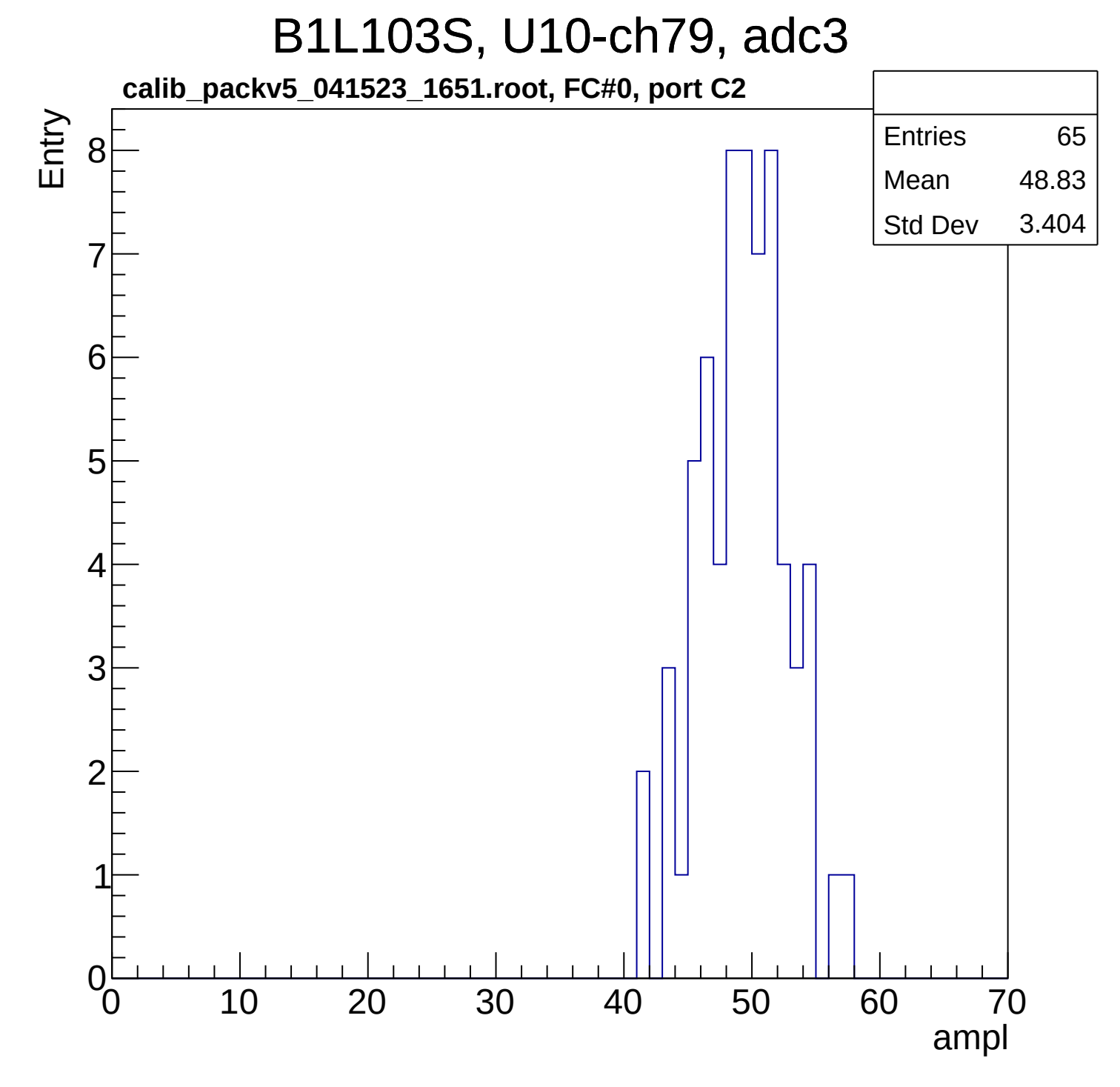

B1L103S, U10-ch78, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 23
Mean 61.61
Std Dev 1.242
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

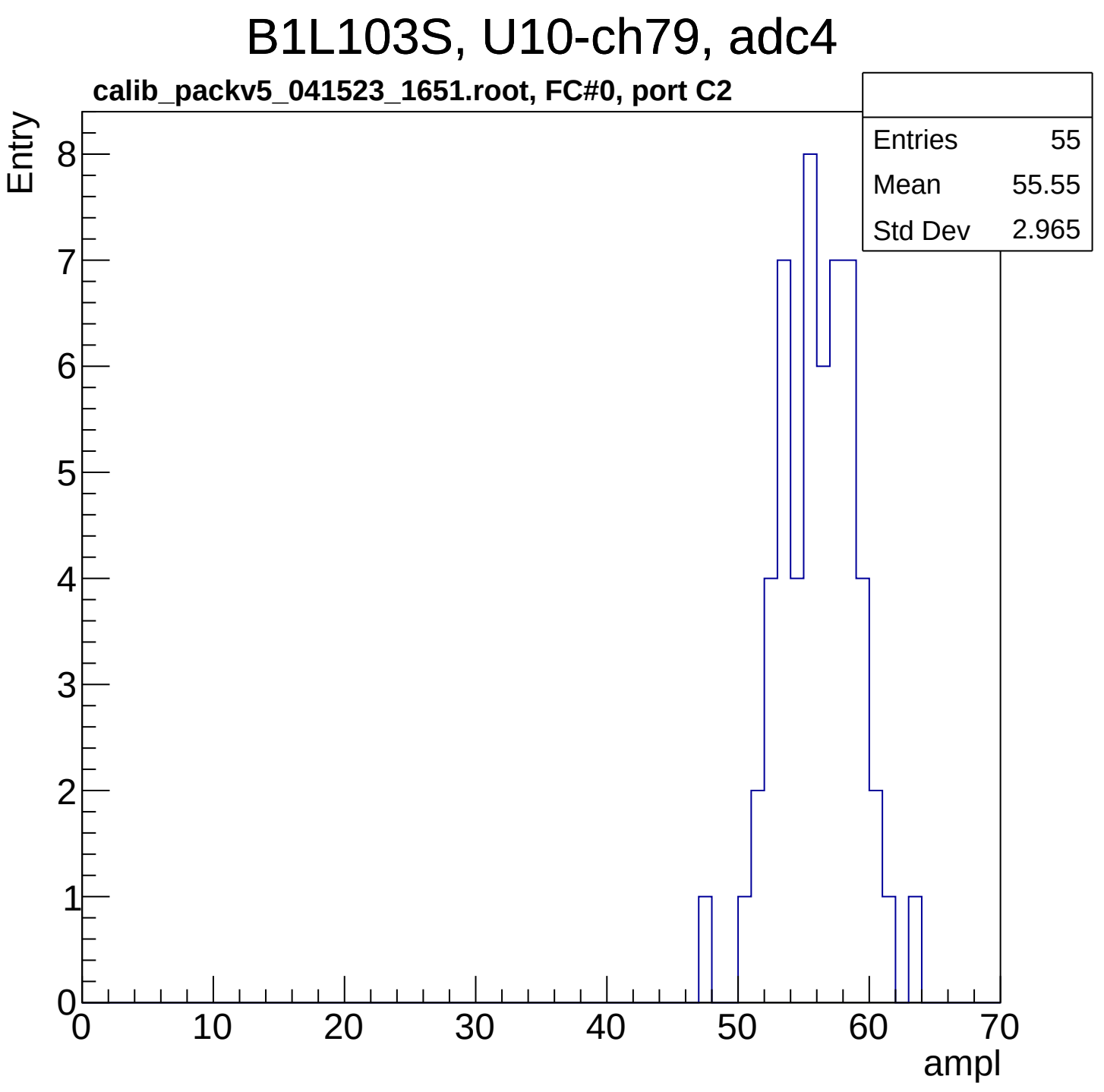

B1L103S, U10-ch78, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 1.111
Std Dev 4.581
Entry
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch79, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 98
Mean 26.93
Std Dev 8.758
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U10-ch79, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 32.63
Std Dev 12.39
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U10-ch79, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 40.59
Std Dev 10.82
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U10-ch79, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 48.83
Std Dev 3.404
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U10-ch79, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 55.55
Std Dev 2.965
Entry
ampl
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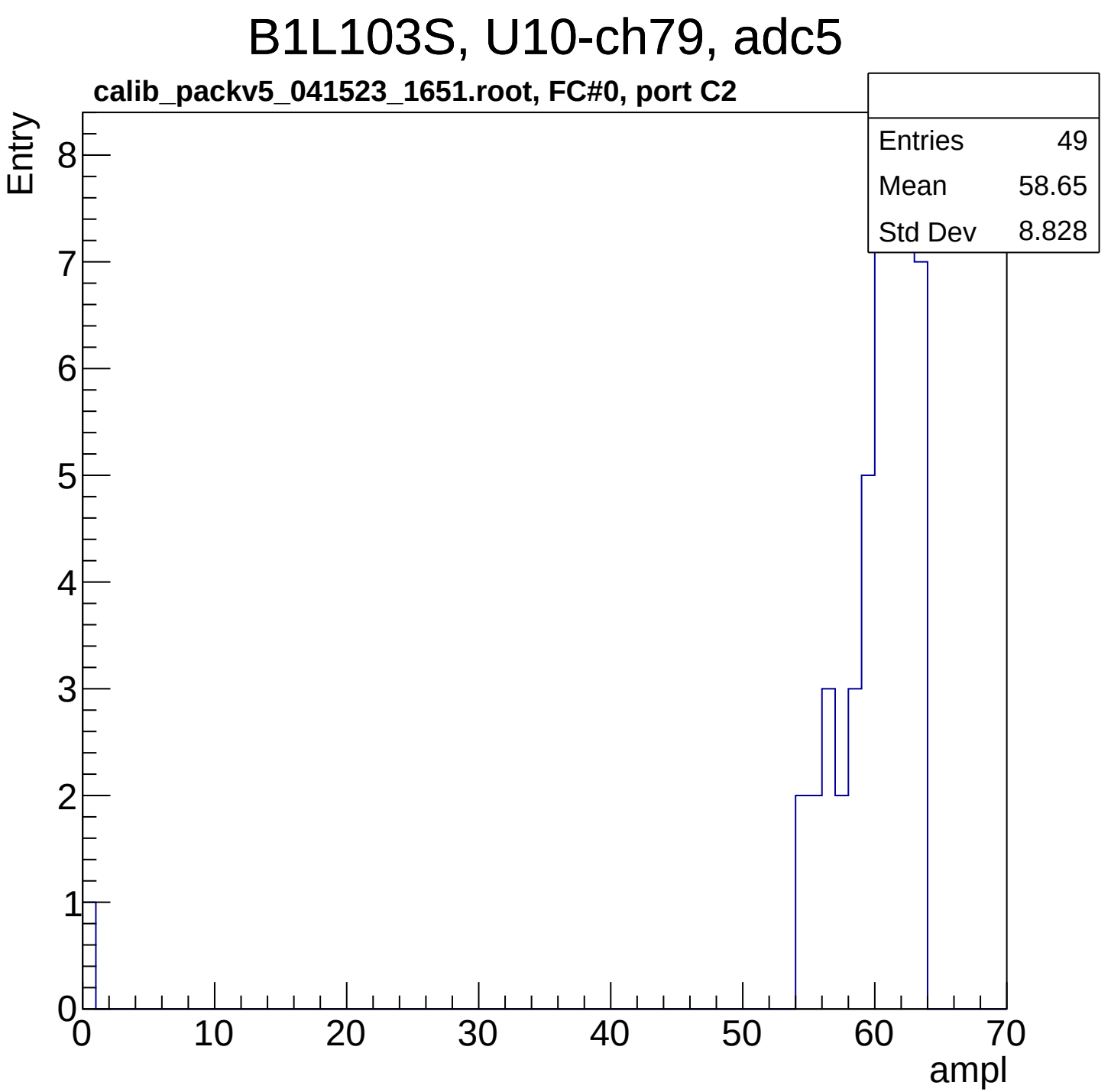
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U10-ch79, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 58.65
Std Dev 8.828
Entry
ampl
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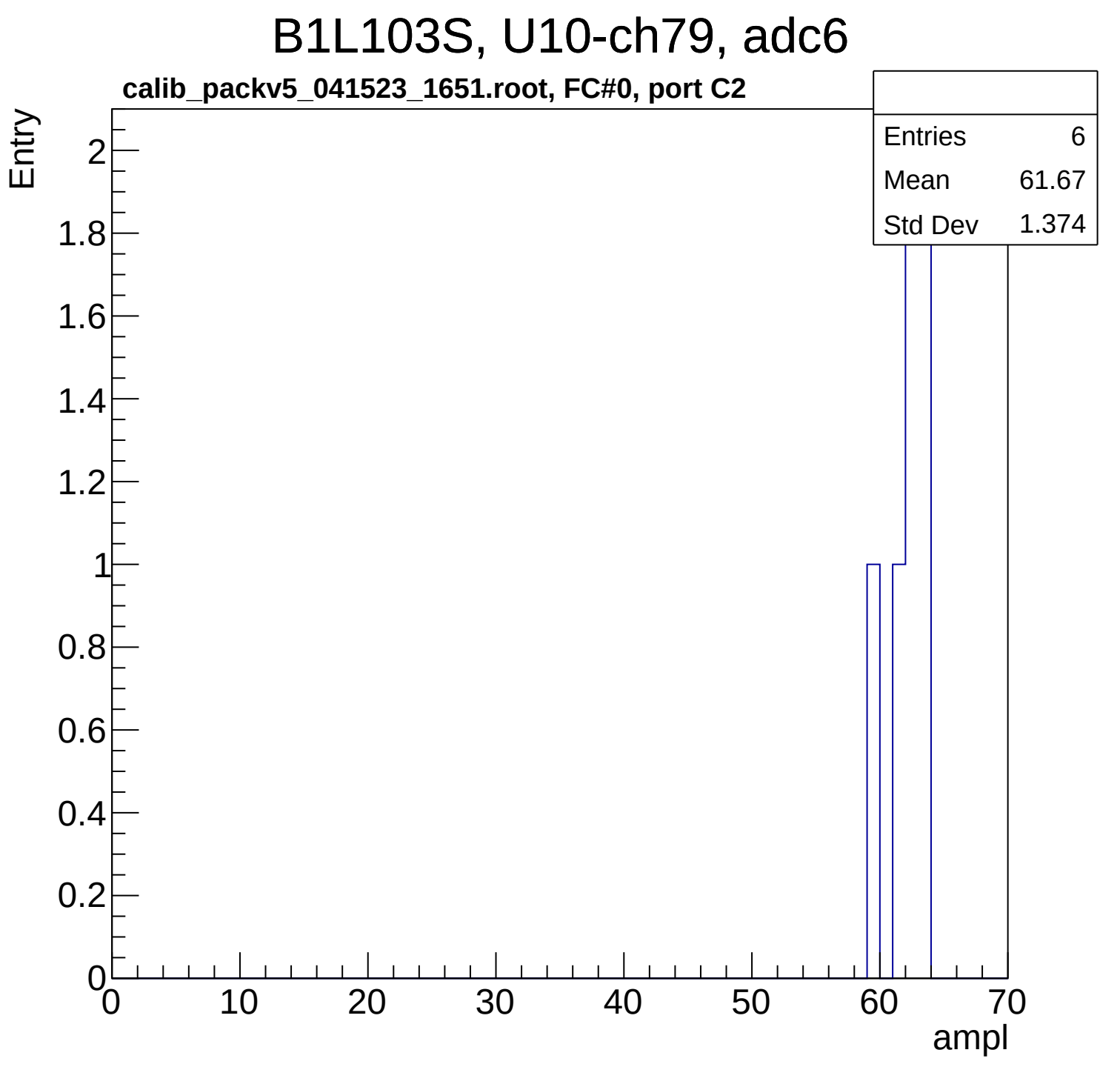
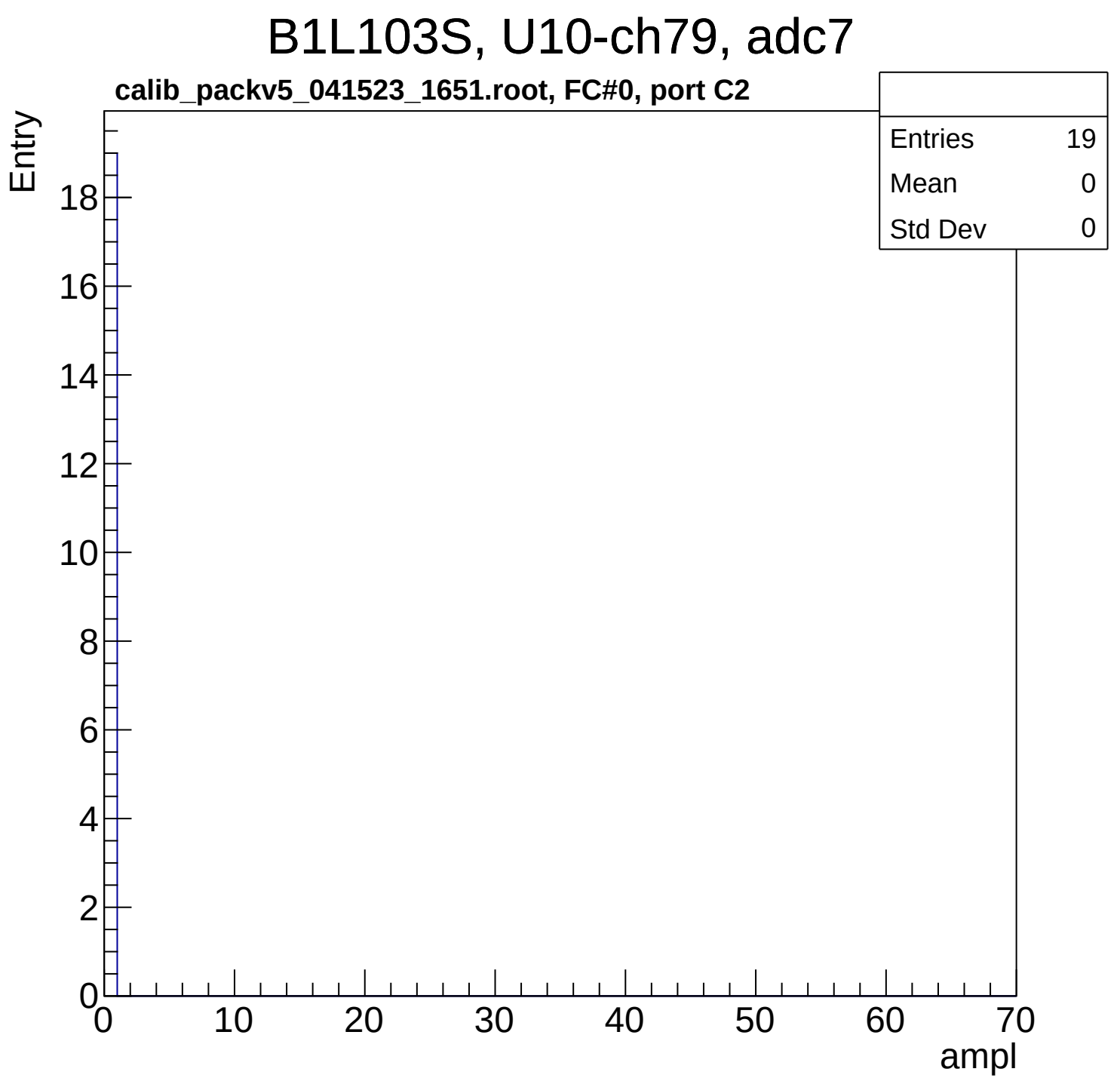
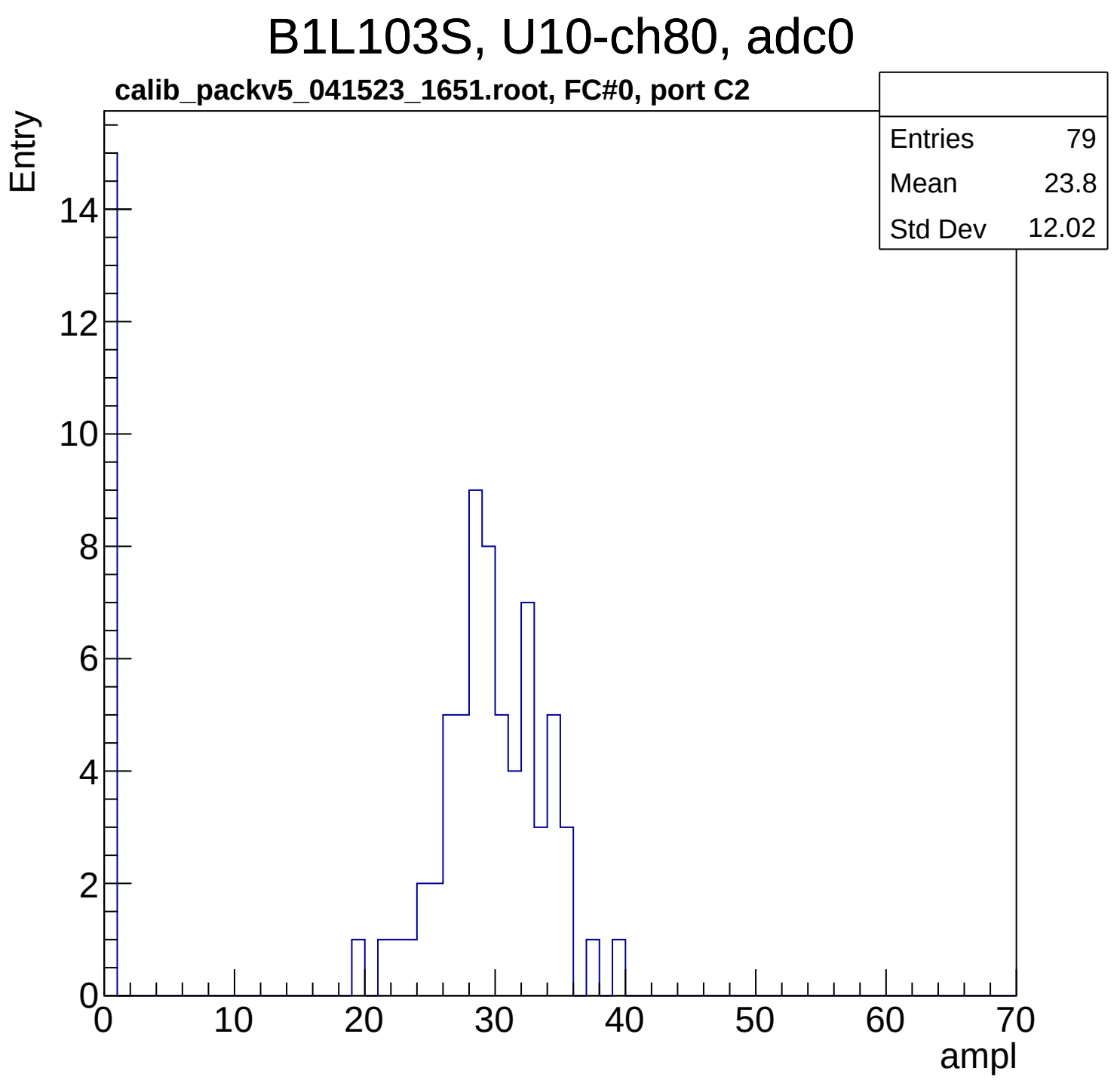
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U10-ch79, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 61.67
Std Dev 1.374
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U10-ch79, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch80, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 23.8
Std Dev 12.02
Entry
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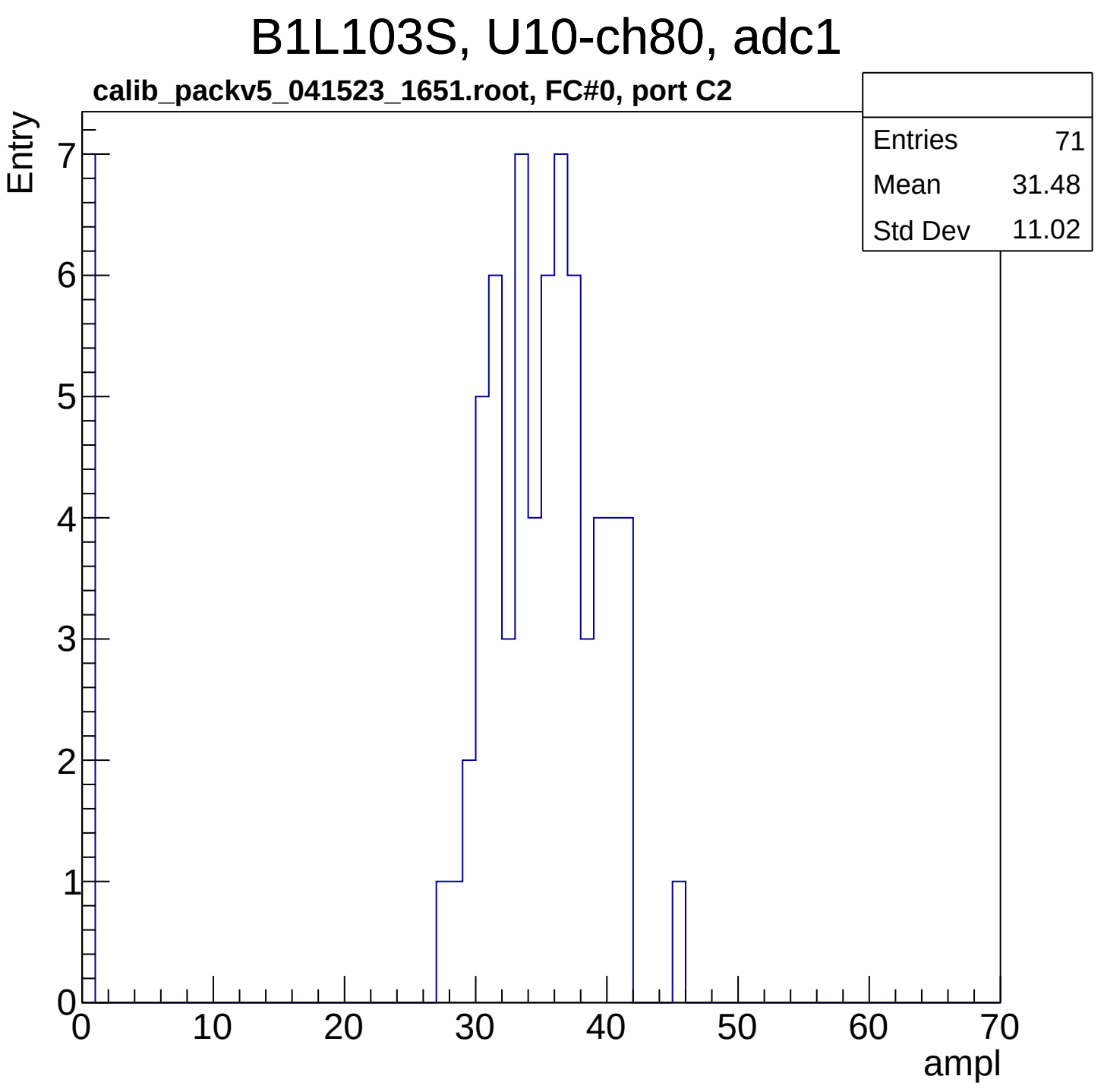
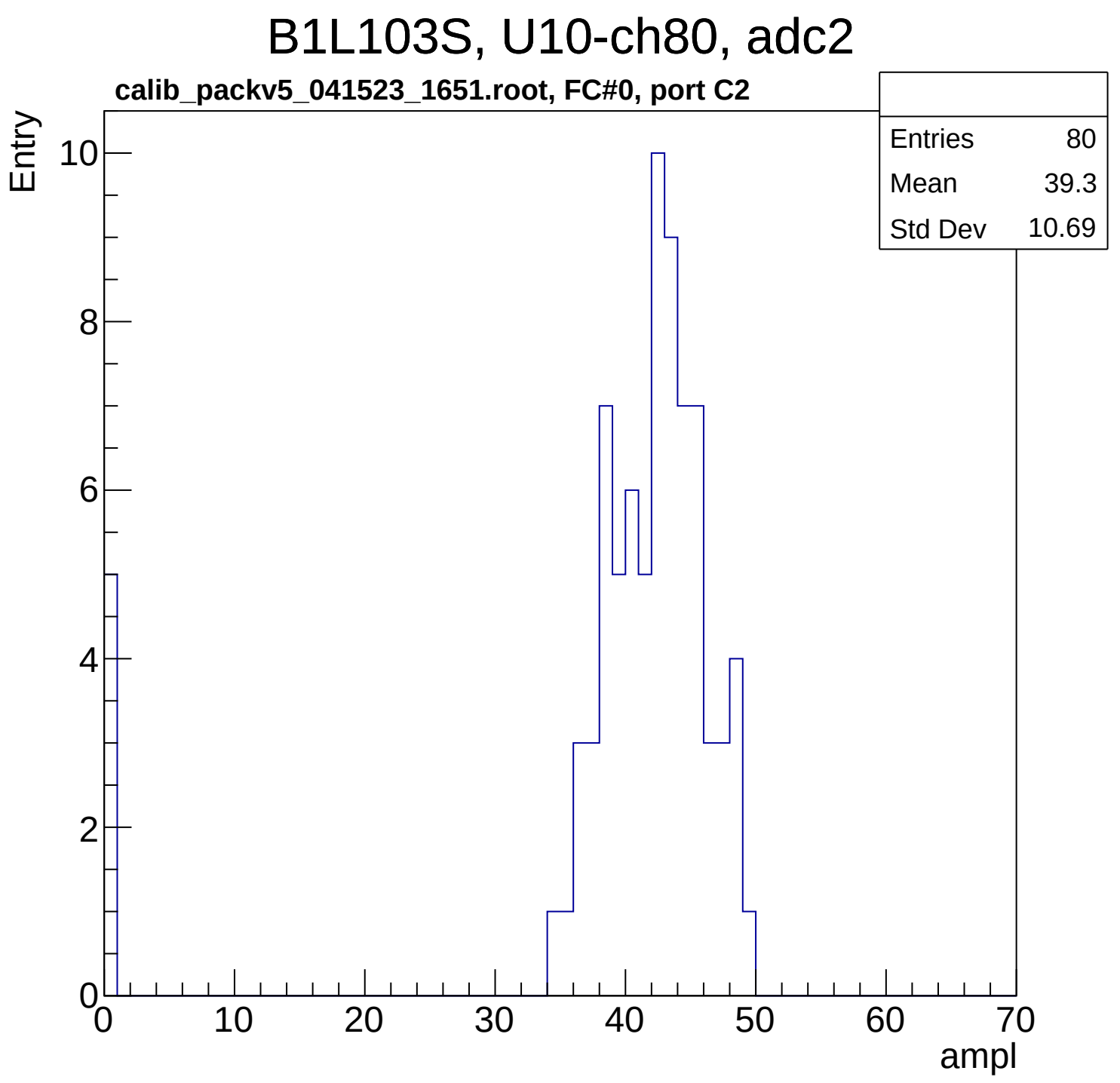
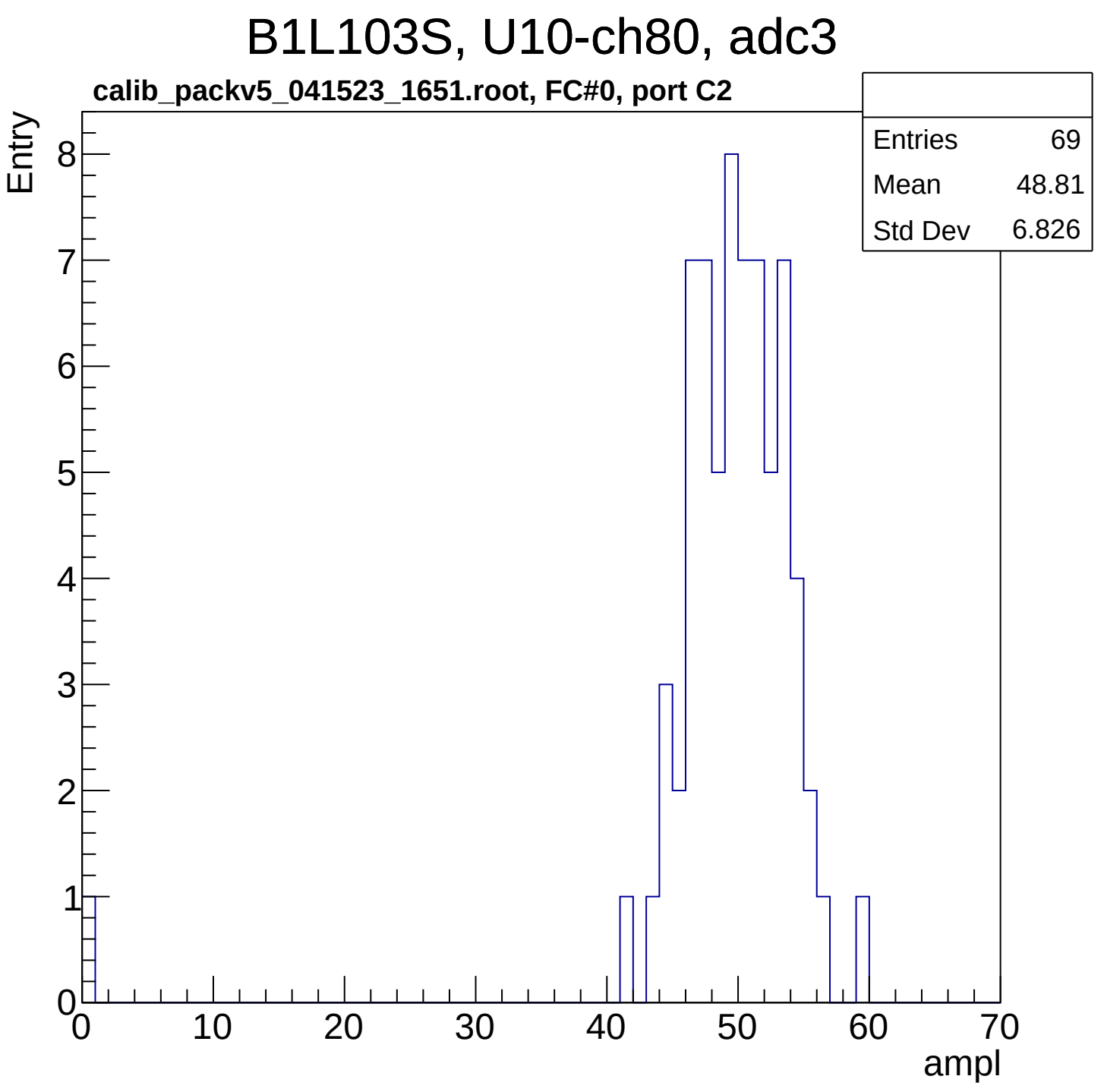
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch80, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 31.48
Std Dev 11.02
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U10-ch80, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 39.3
Std Dev 10.69
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U10-ch80, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 48.81
Std Dev 6.826
Entry
ampl
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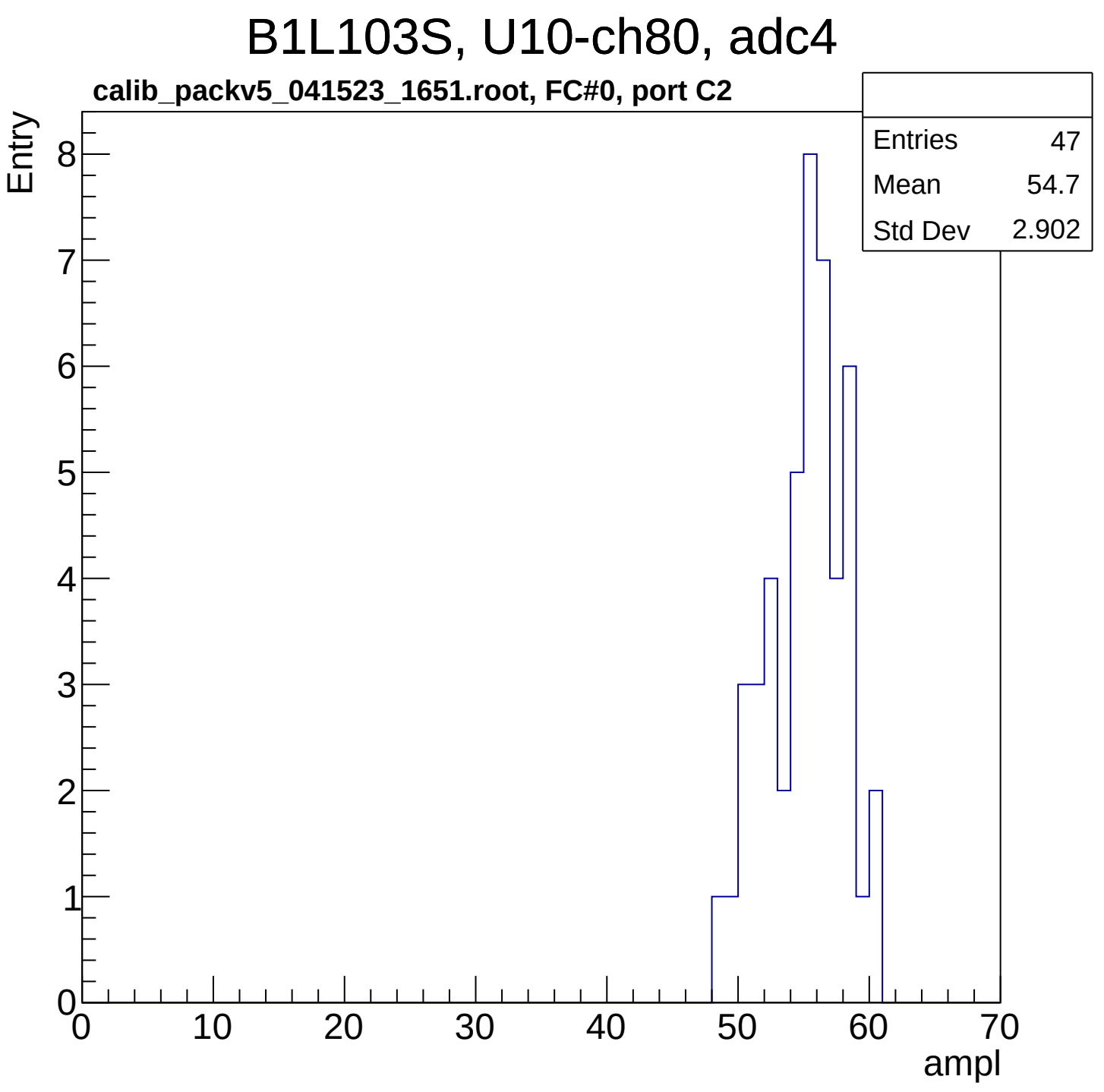
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U10-ch80, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 54.7
Std Dev 2.902
Entry
ampl
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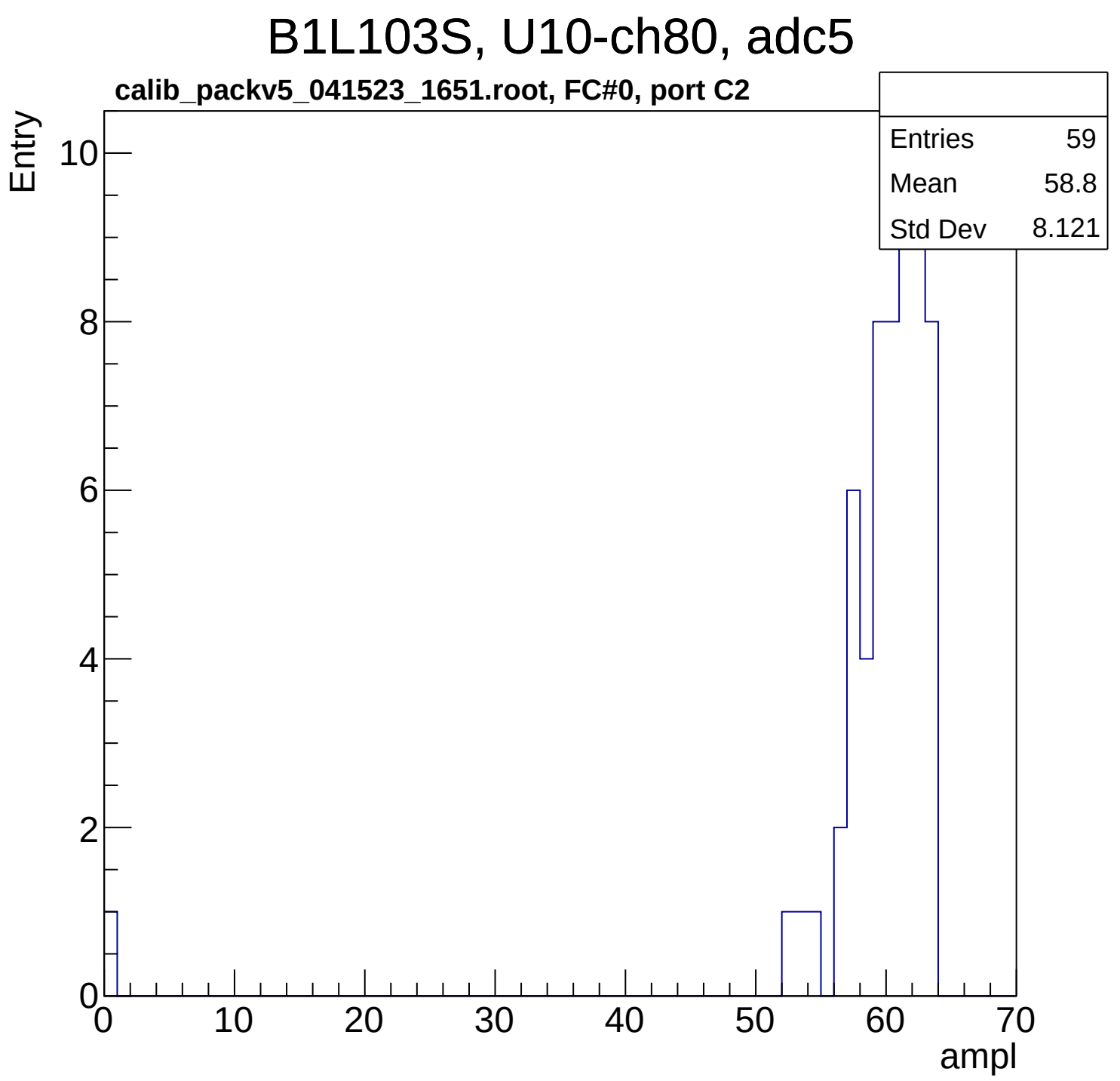
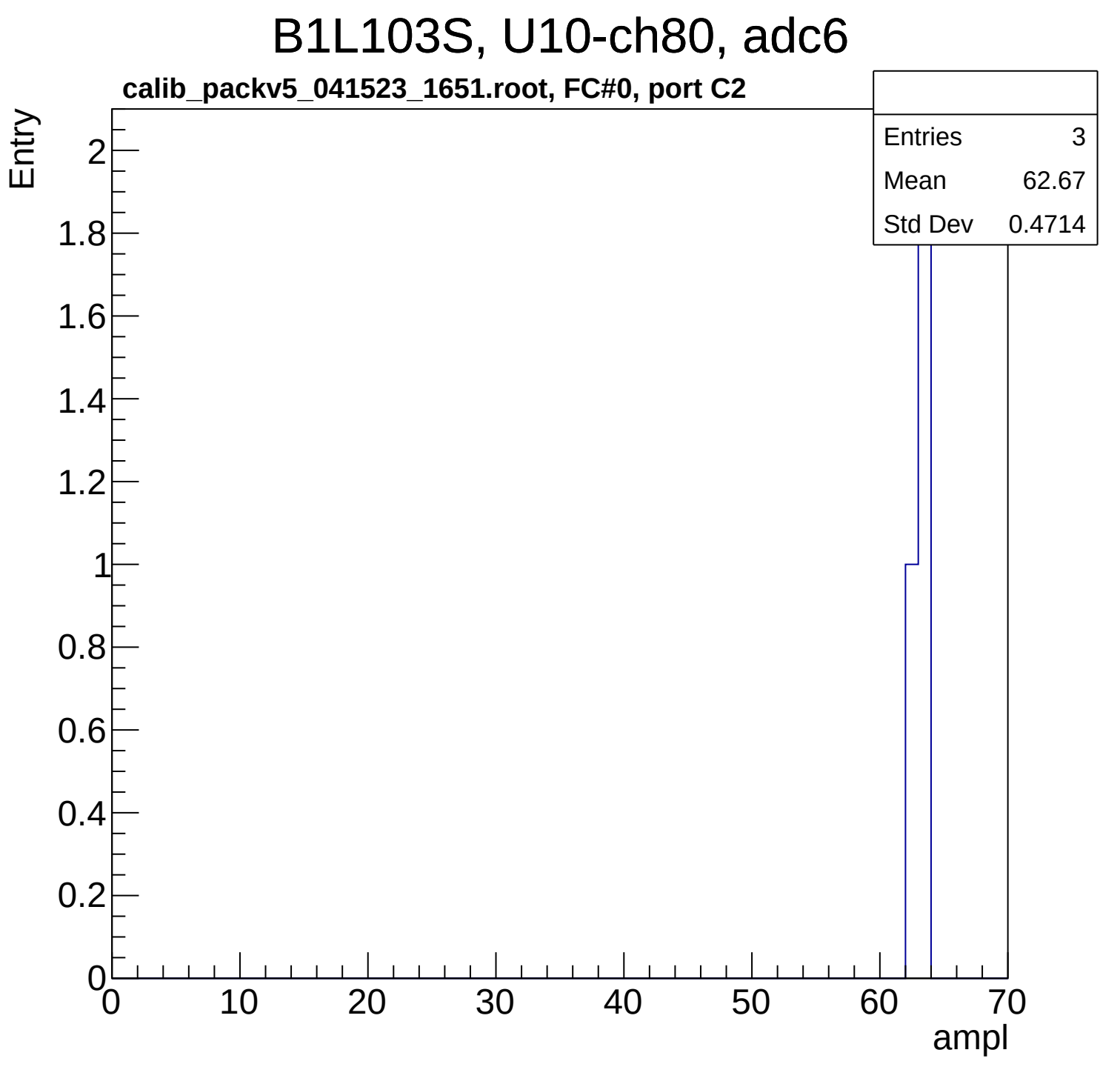
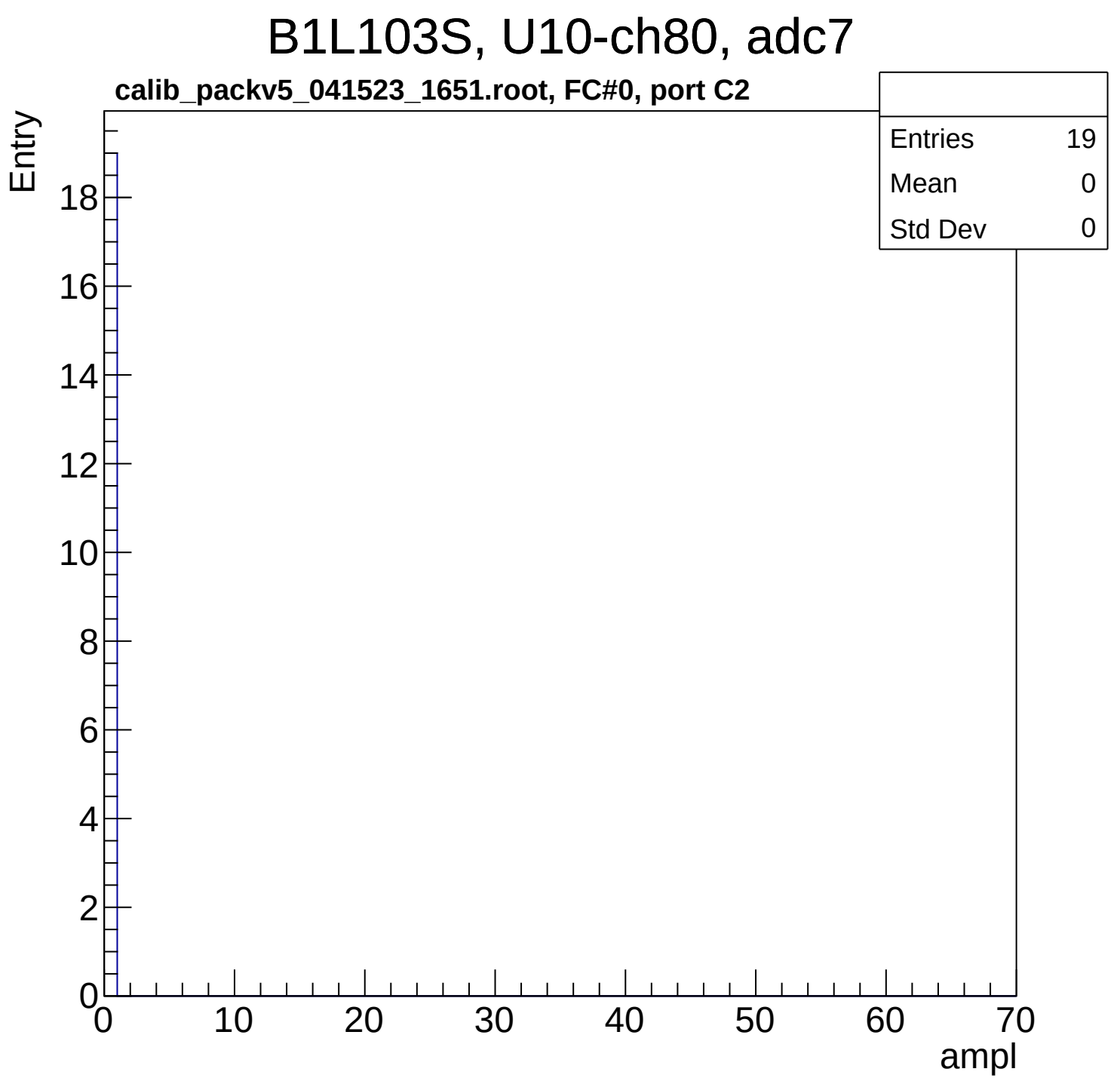
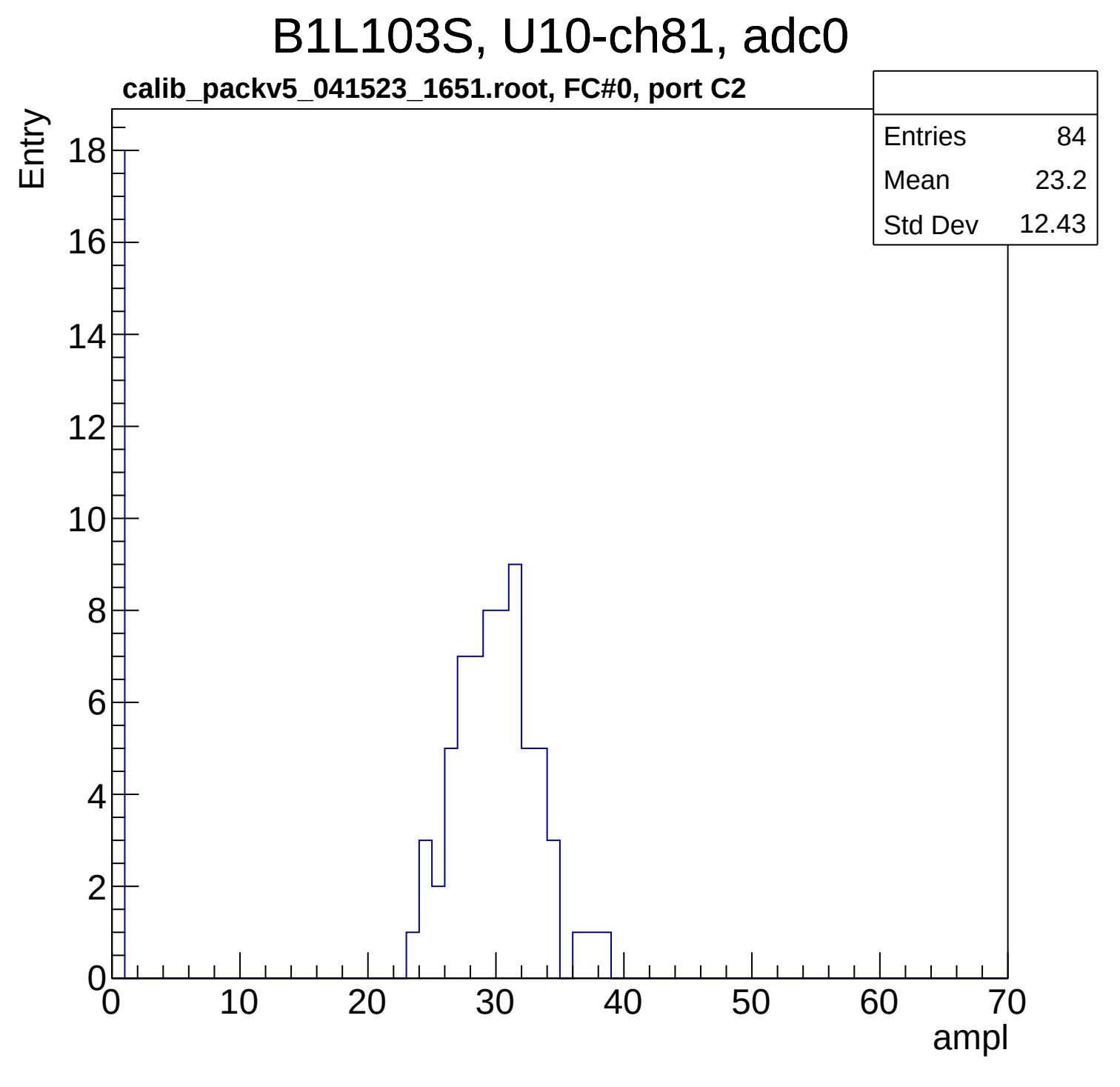
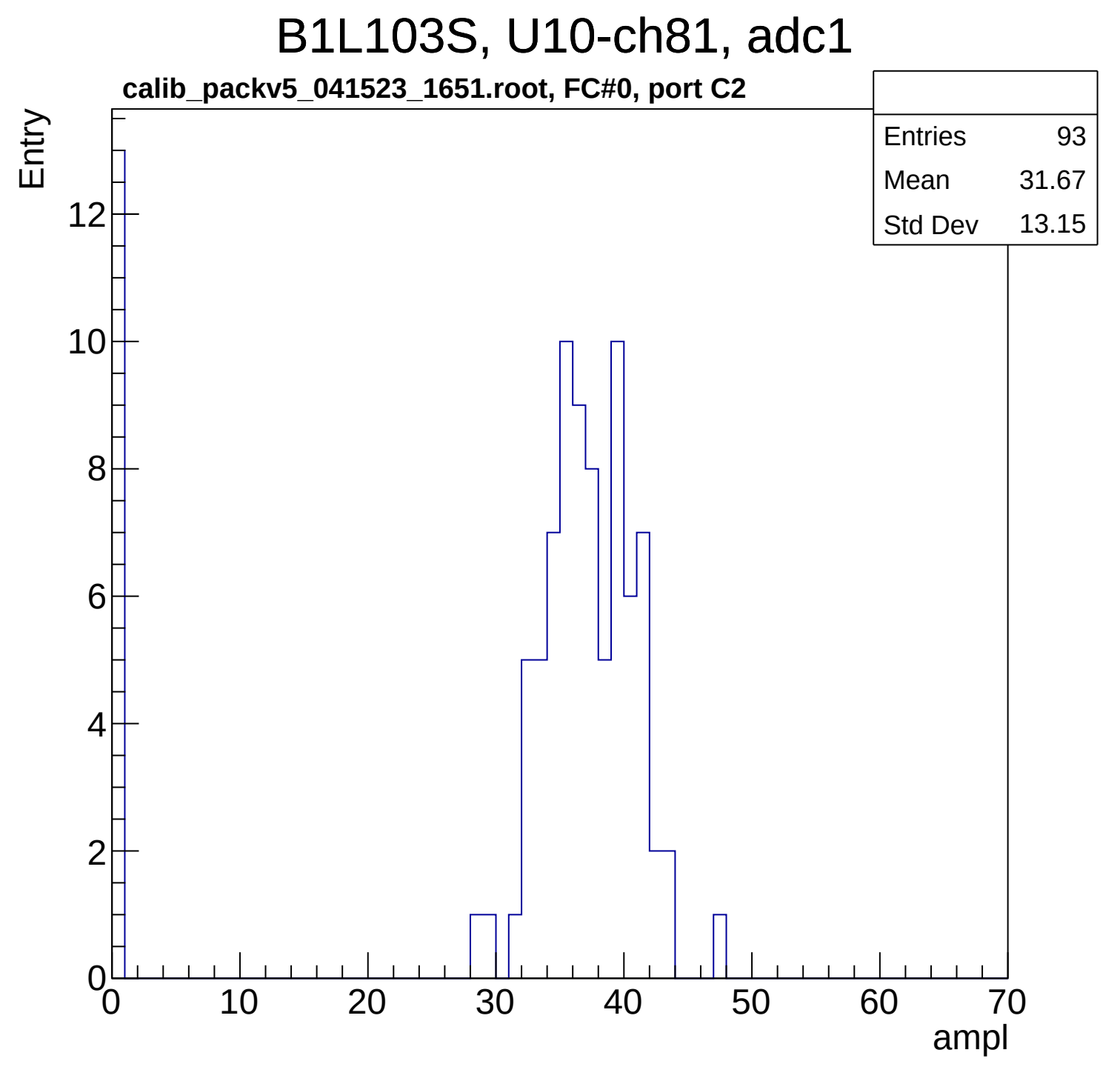
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

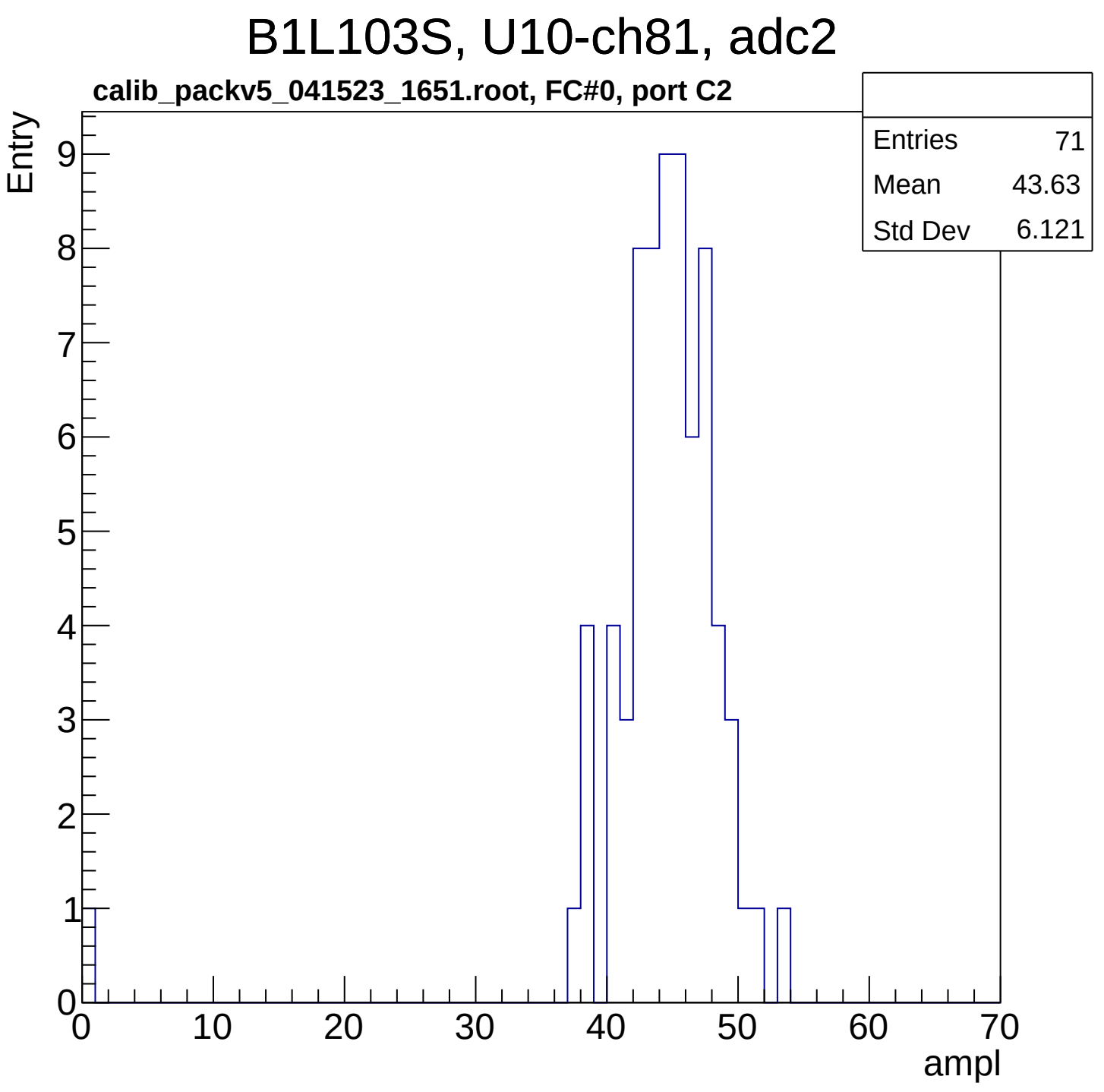

B1L103S, U10-ch80, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 58.8
Std Dev 8.121
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

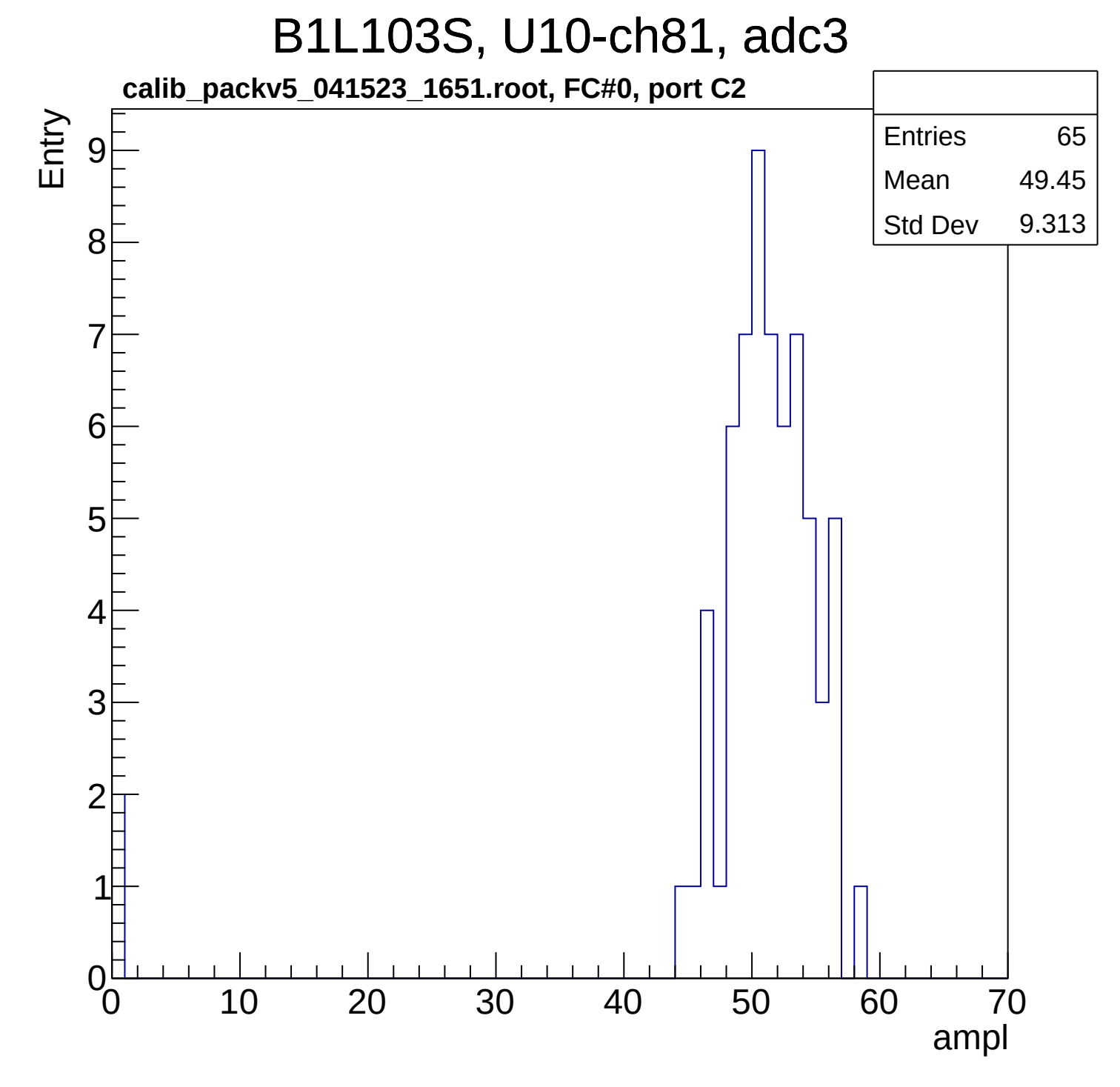

B1L103S, U10-ch80, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 3
Mean 62.67
Std Dev 0.4714
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U10-ch80, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch81, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 23.2
Std Dev 12.43
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70


B1L103S, U10-ch81, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 93
Mean 31.67
Std Dev 13.15
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch81, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 43.63
Std Dev 6.121
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U10-ch81, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 49.45
Std Dev 9.313
Entry
ampl
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2
3
4
5
6
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8
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0
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60
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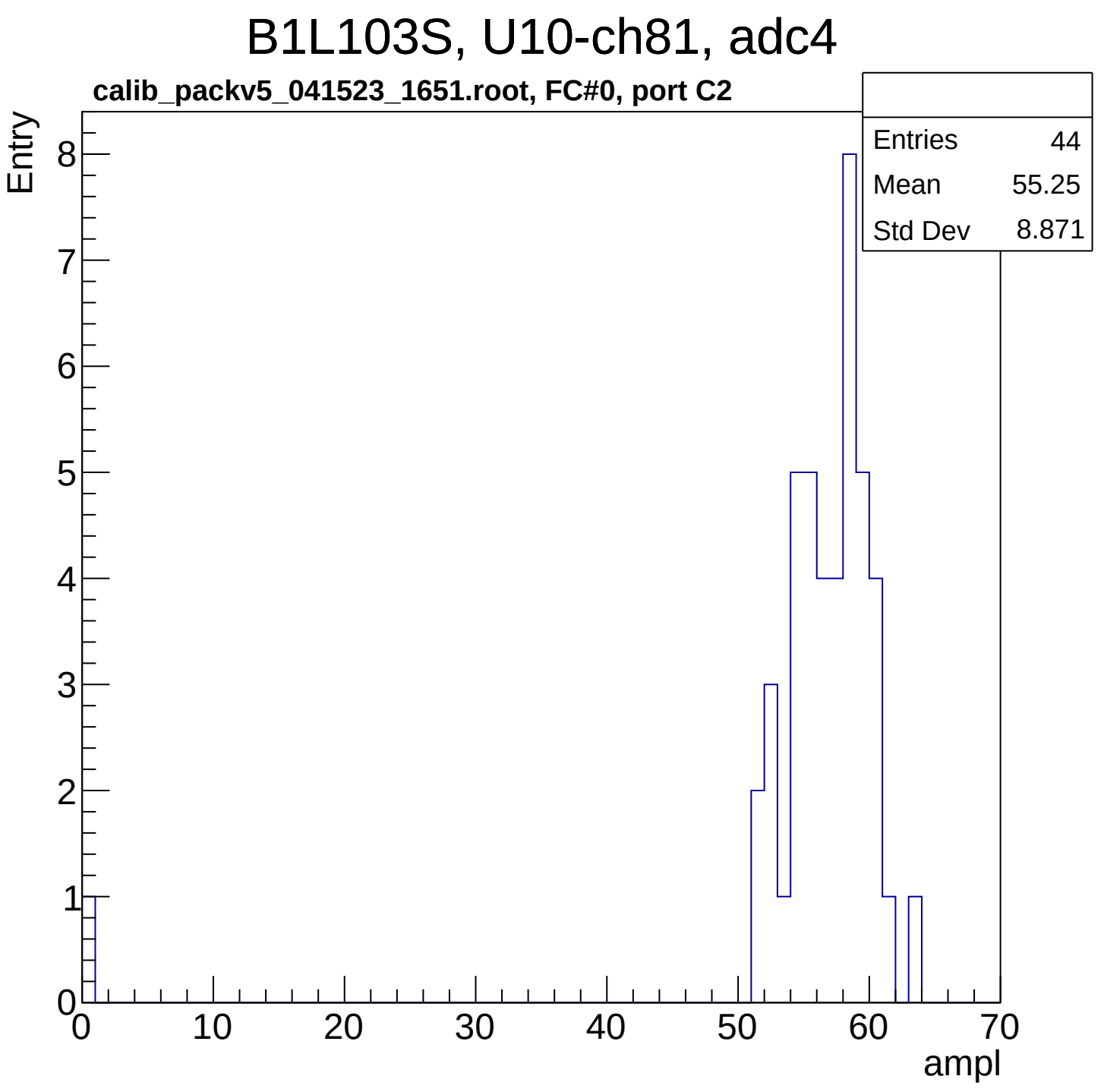
B1L103S, U10-ch81, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 55.25
Std Dev 8.871
Entry
ampl
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3
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7
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0
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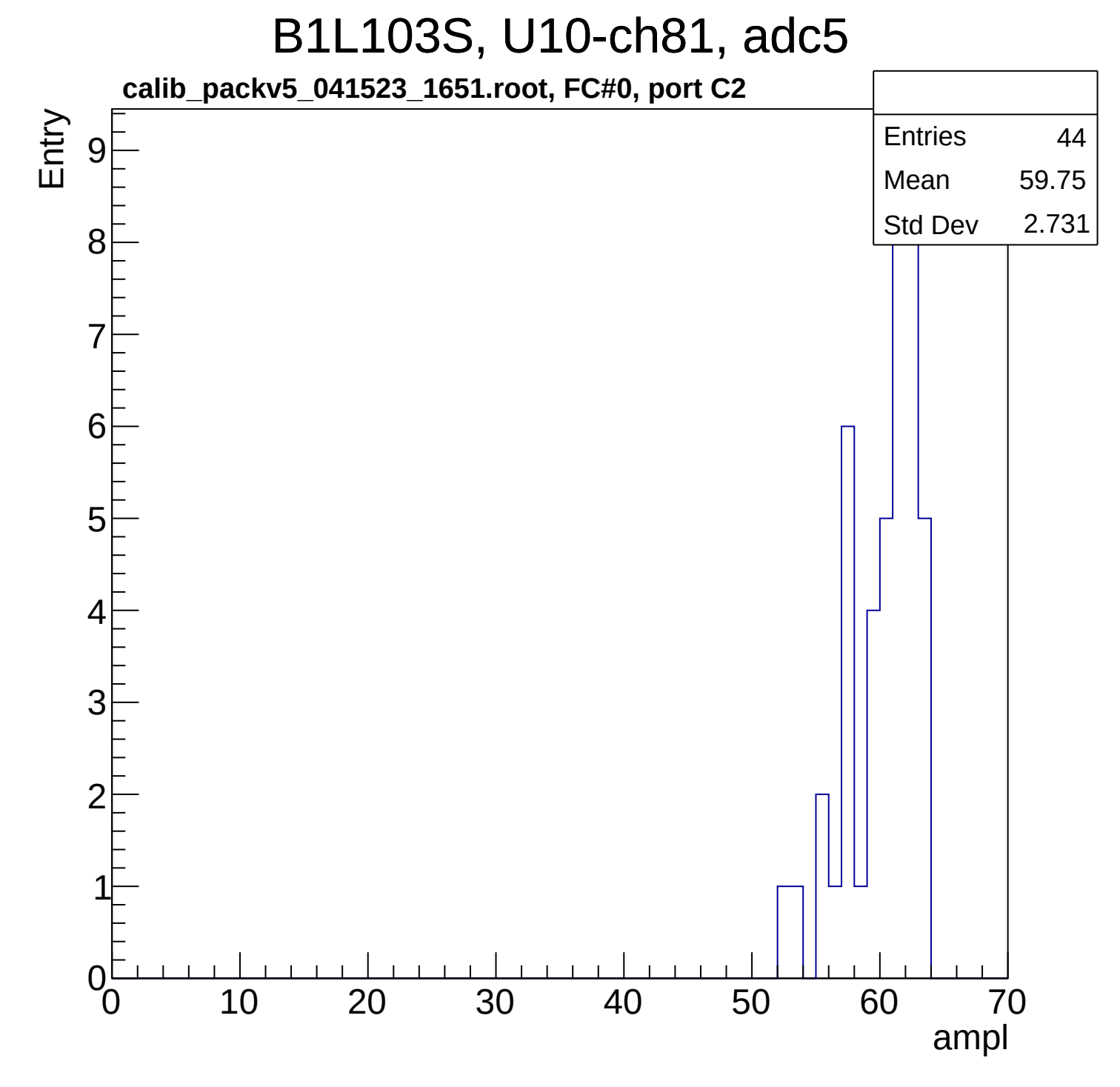
B1L103S, U10-ch81, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 59.75
Std Dev 2.731
Entry
ampl
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0
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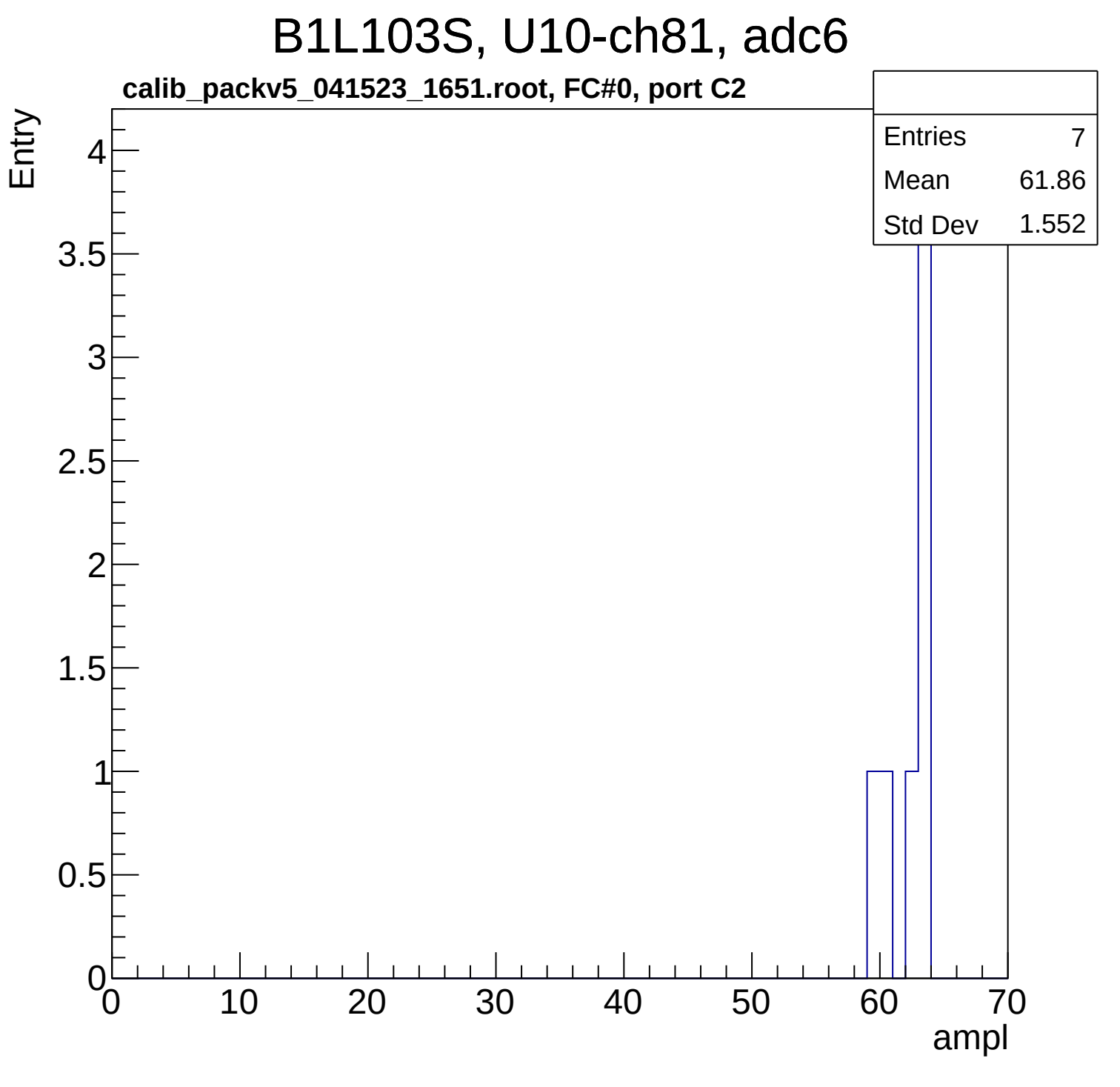
B1L103S, U10-ch81, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 61.86
Std Dev 1.552
Entry
ampl
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0.5
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1.5
2
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3
3.5
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0
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40
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60
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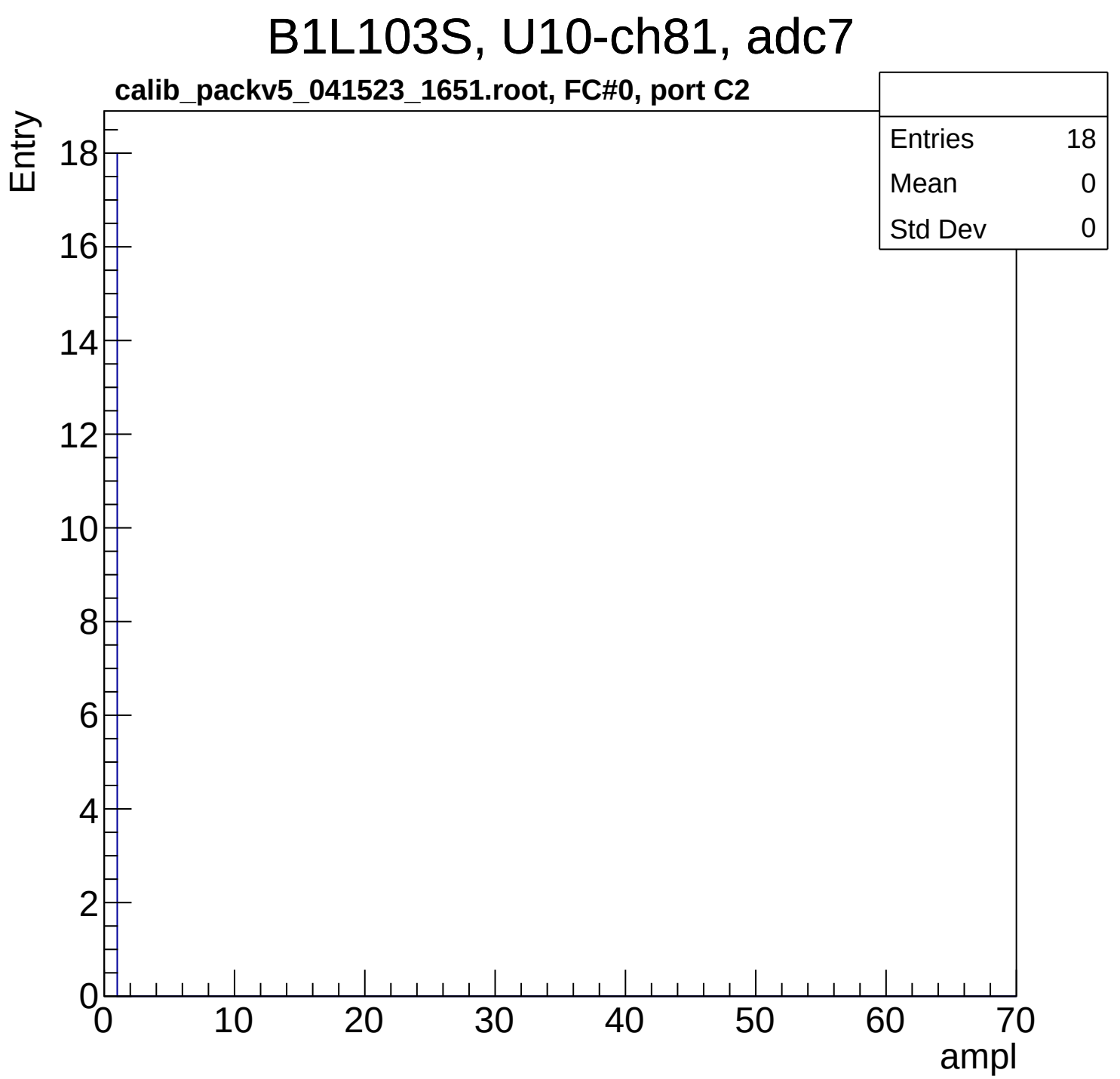
B1L103S, U10-ch81, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
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4
6
8
10
12
14
16
18
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10
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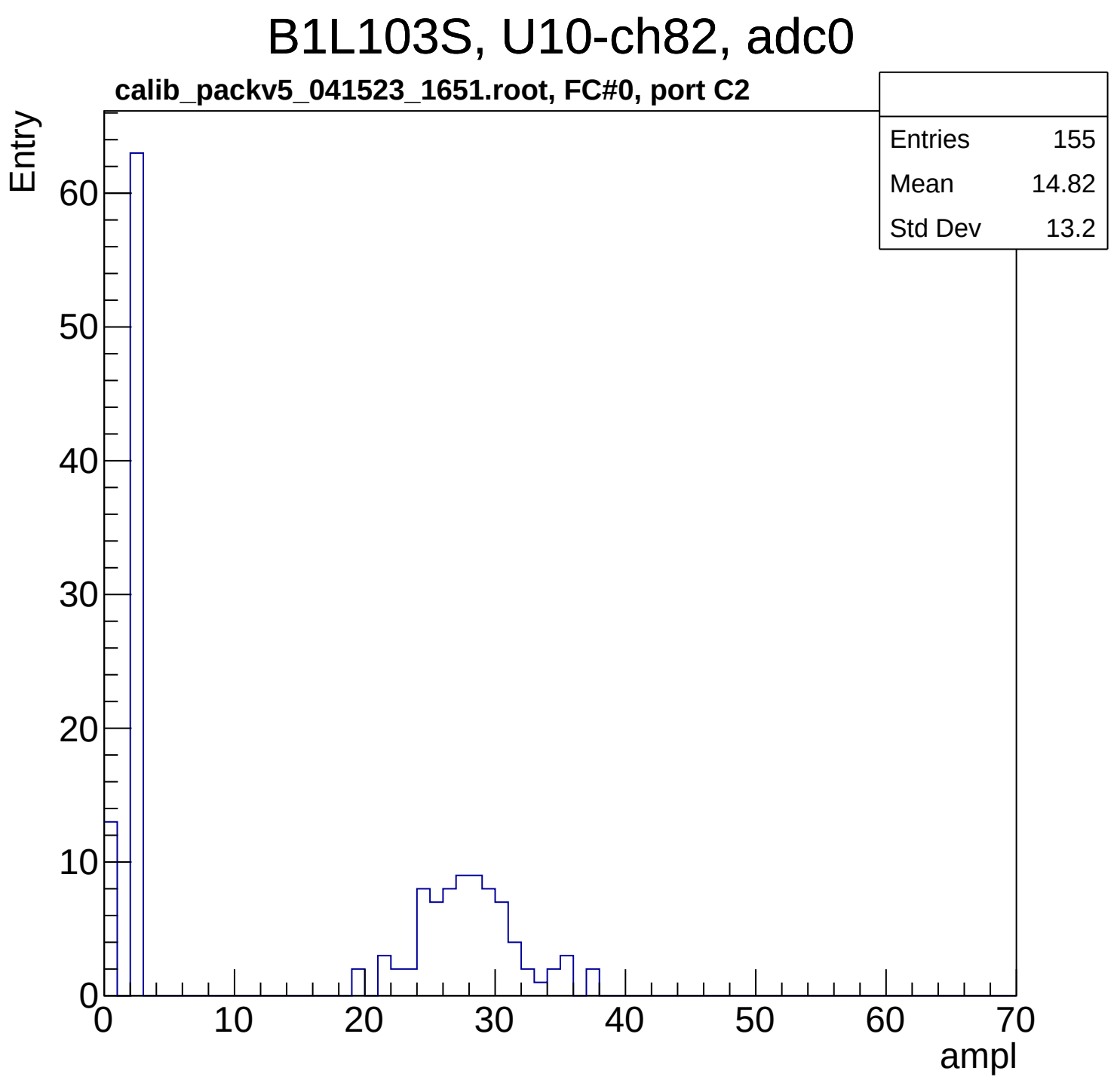
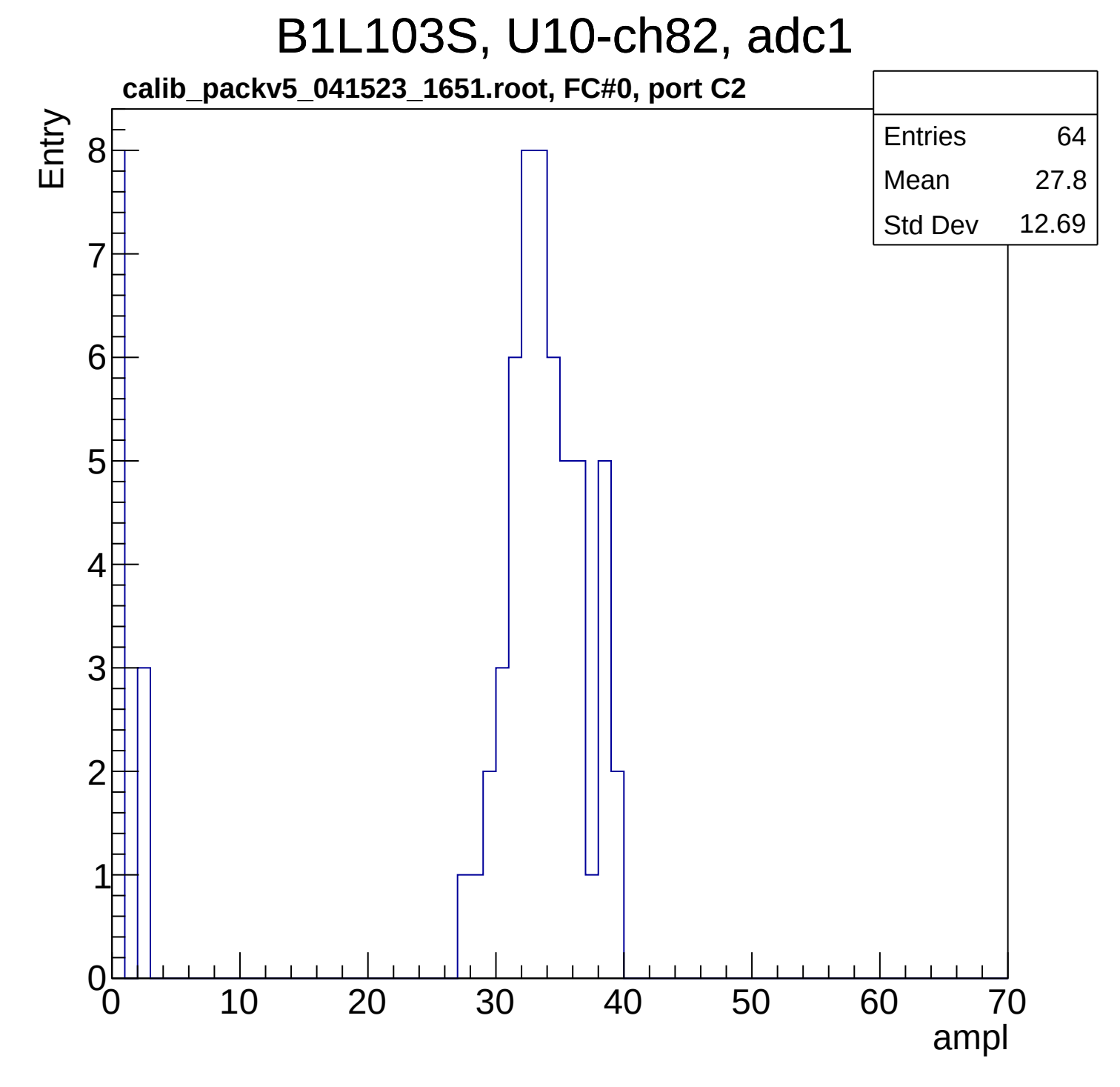
50
60
70
ampl


B1L103S, U10-ch82, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 155
Mean 14.82
Std Dev 13.2
Entry
0
10
20
30
40
50
60
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch82, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 27.8
Std Dev 12.69
Entry
ampl
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2
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5
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7
8
0
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40
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60
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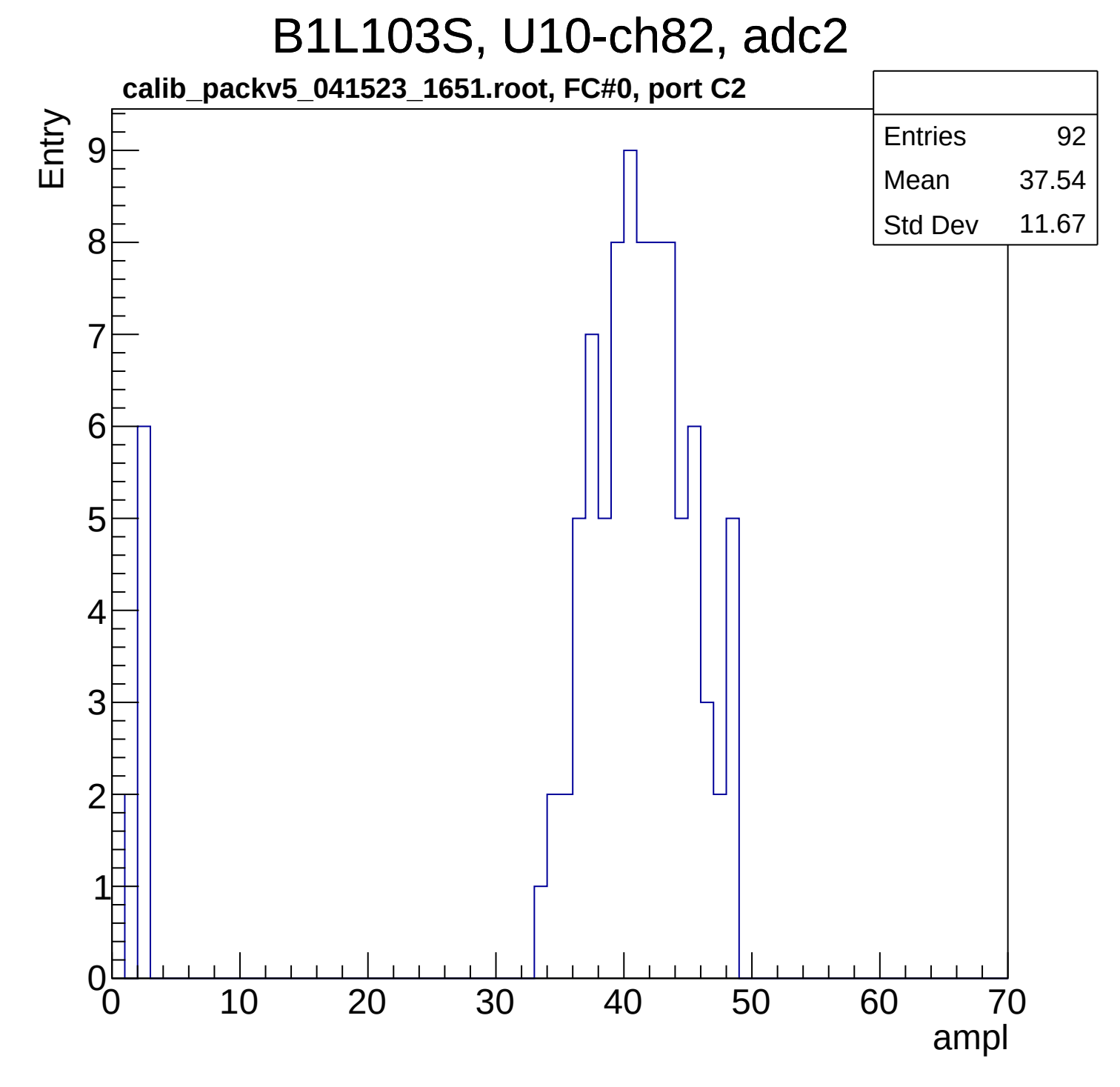
B1L103S, U10-ch82, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 92
Mean 37.54
Std Dev 11.67
Entry
ampl
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3
4
5
6
7
8
9
0
10
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40
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60
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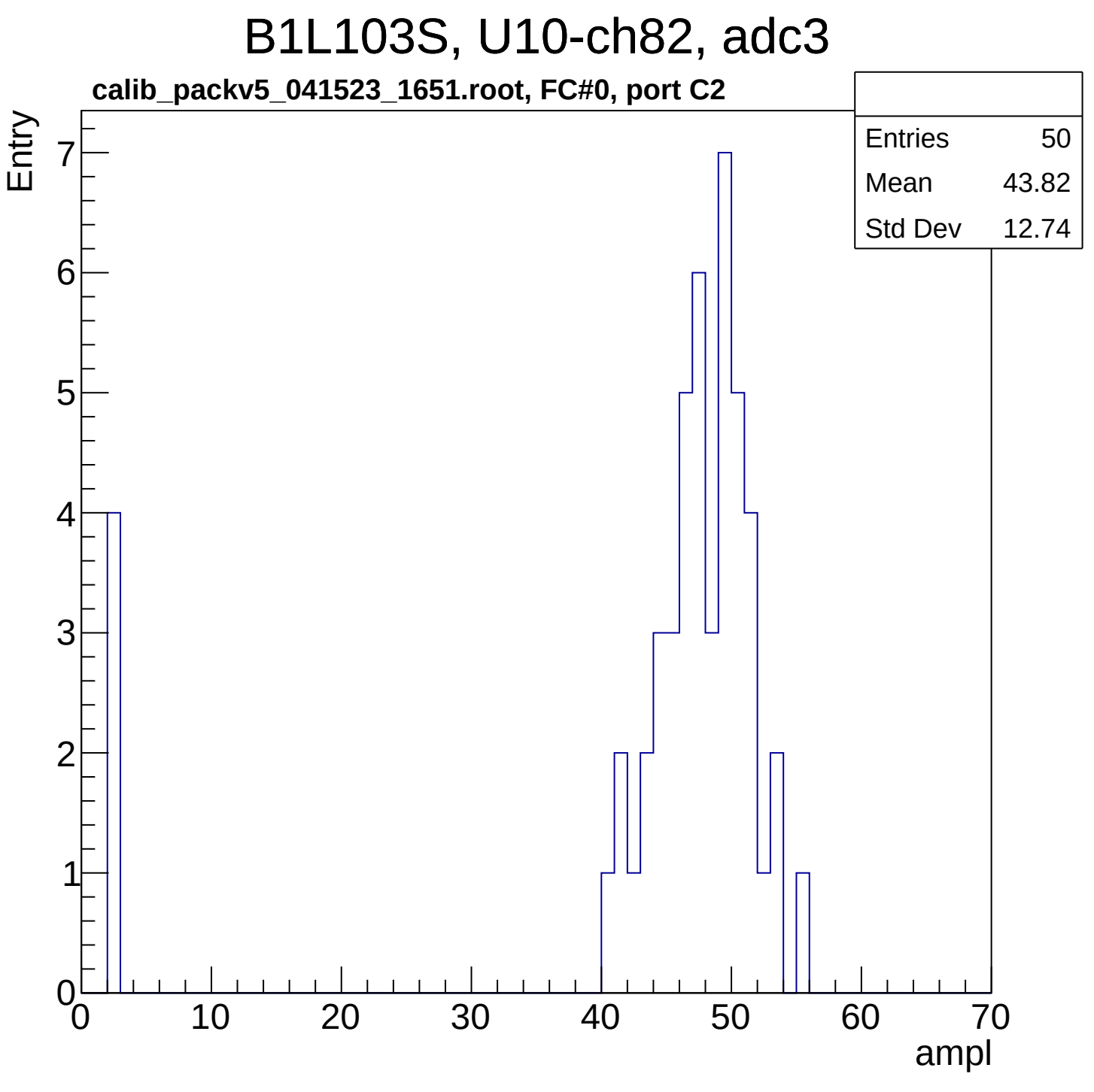
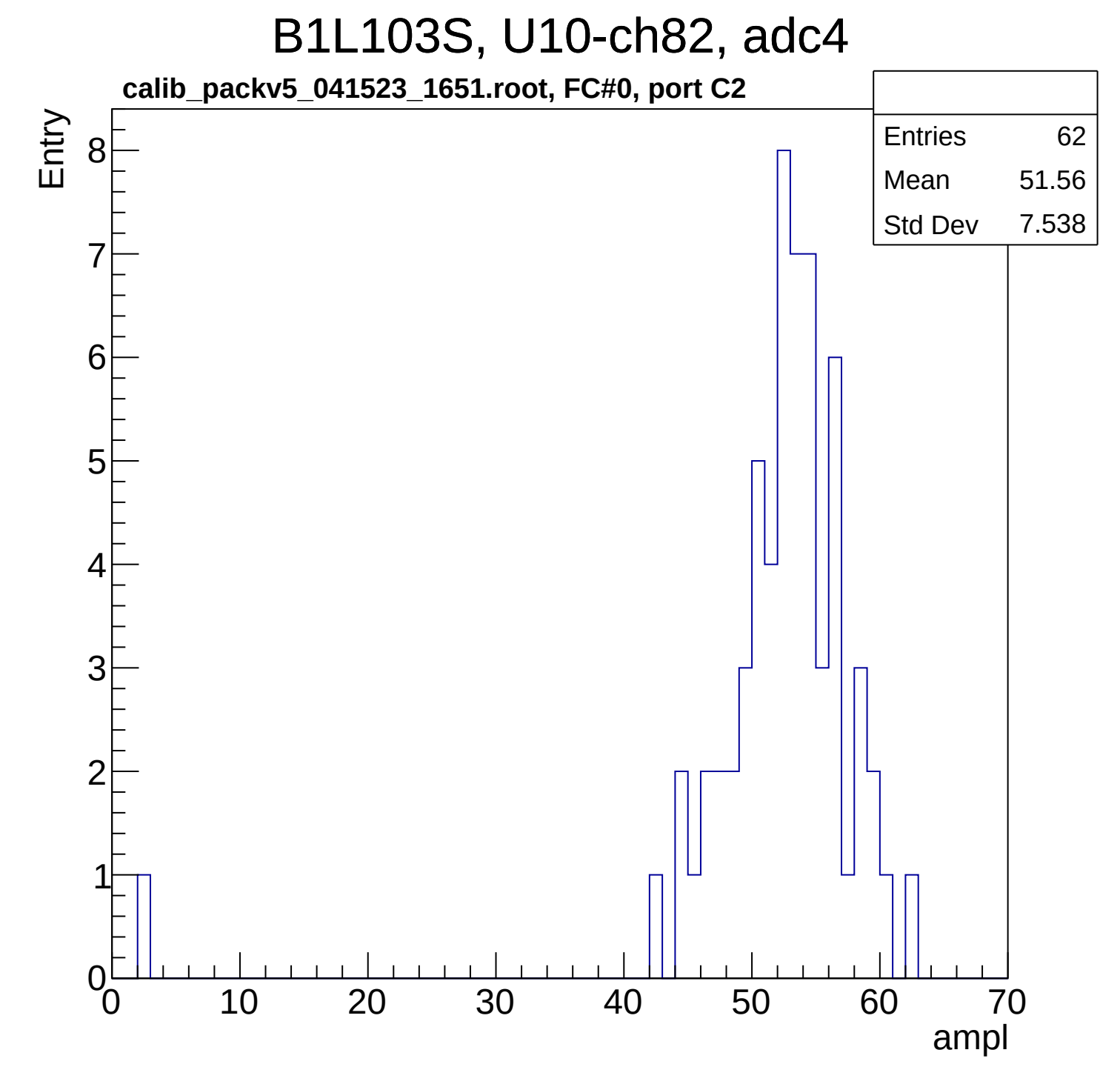

B1L103S, U10-ch82, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 43.82
Std Dev 12.74
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U10-ch82, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 51.56
Std Dev 7.538
Entry
ampl
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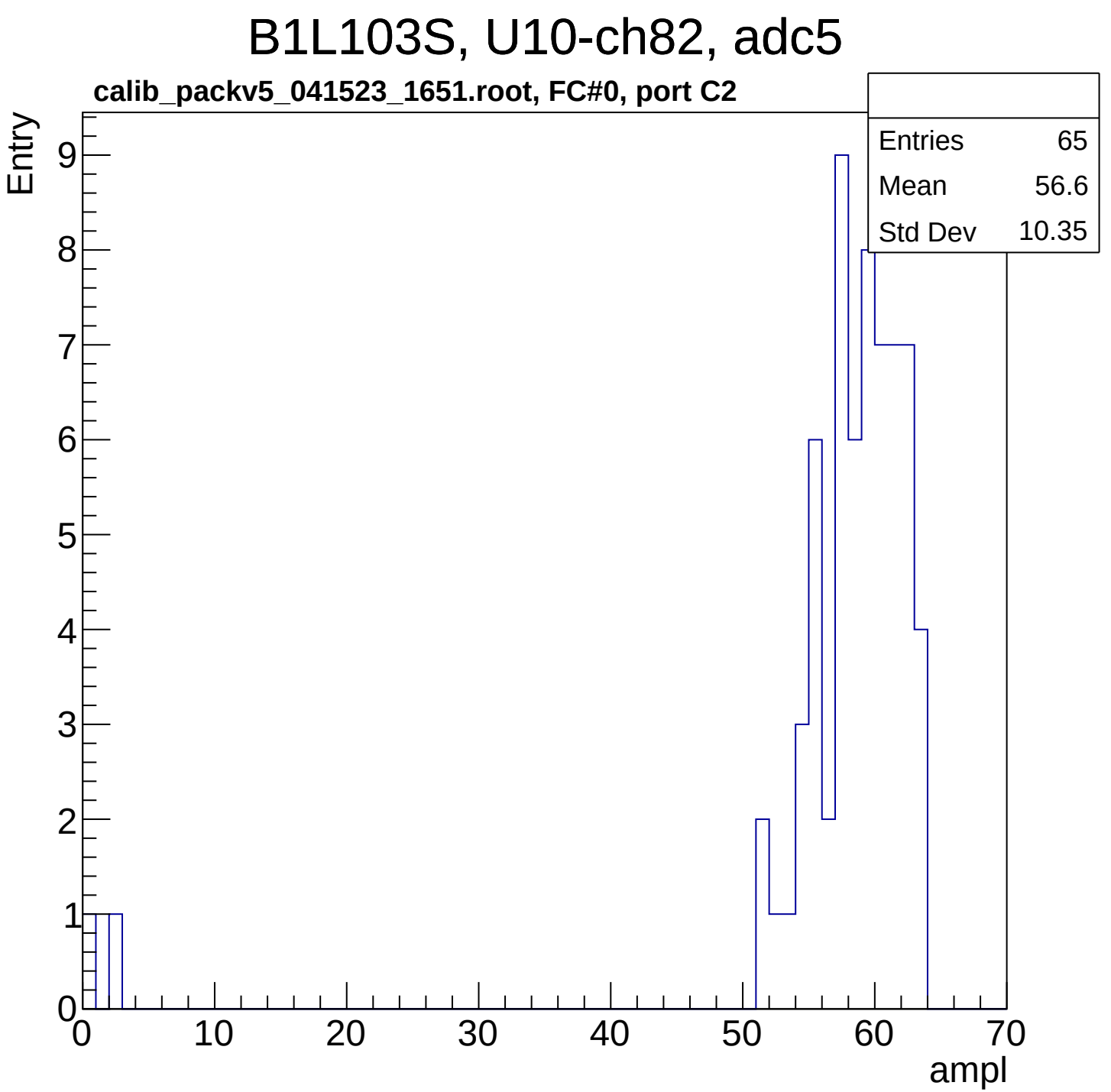
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U10-ch82, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 56.6
Std Dev 10.35
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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40
50
60
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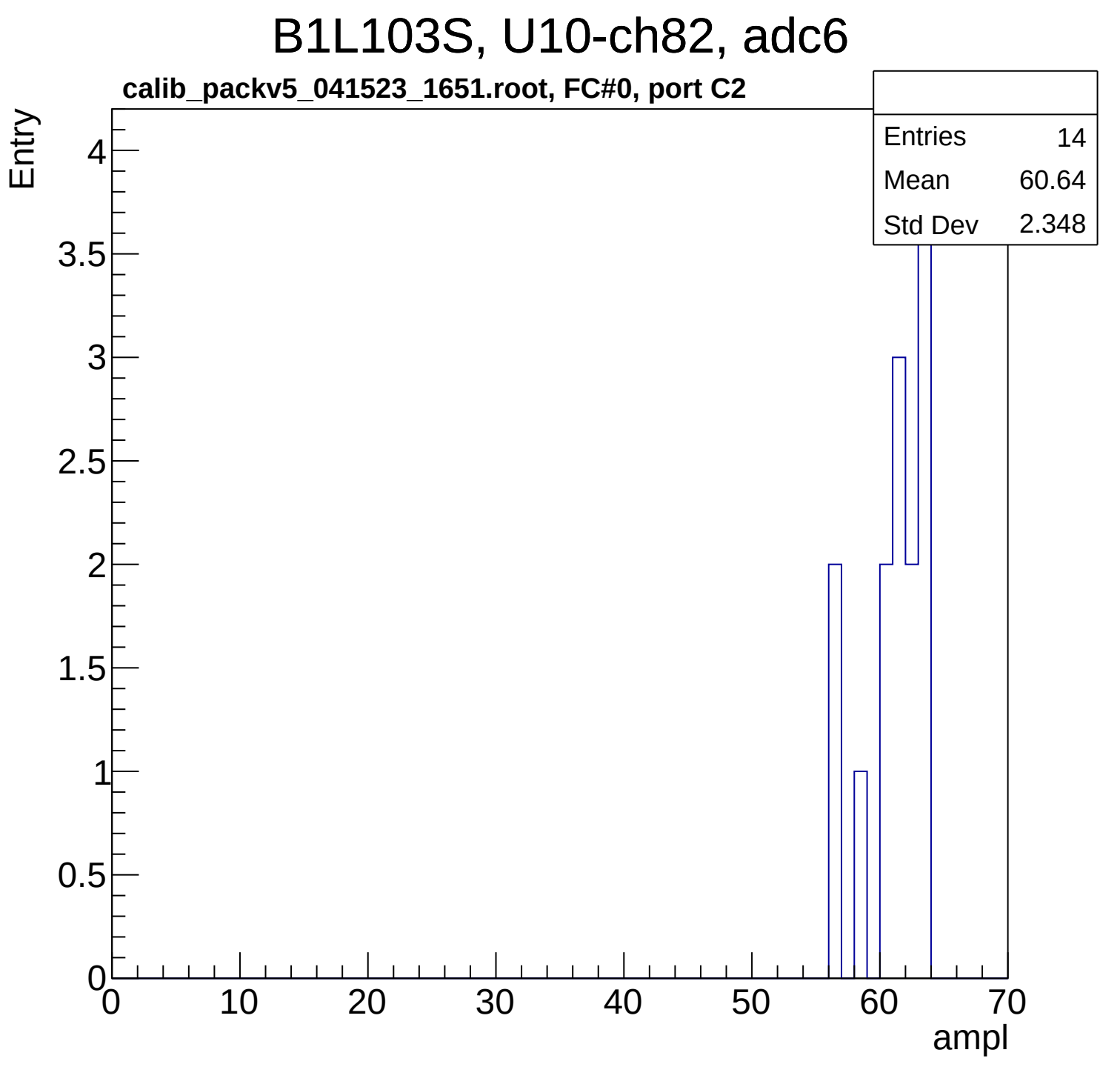
B1L103S, U10-ch82, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 14
Mean 60.64
Std Dev 2.348
Entry
ampl
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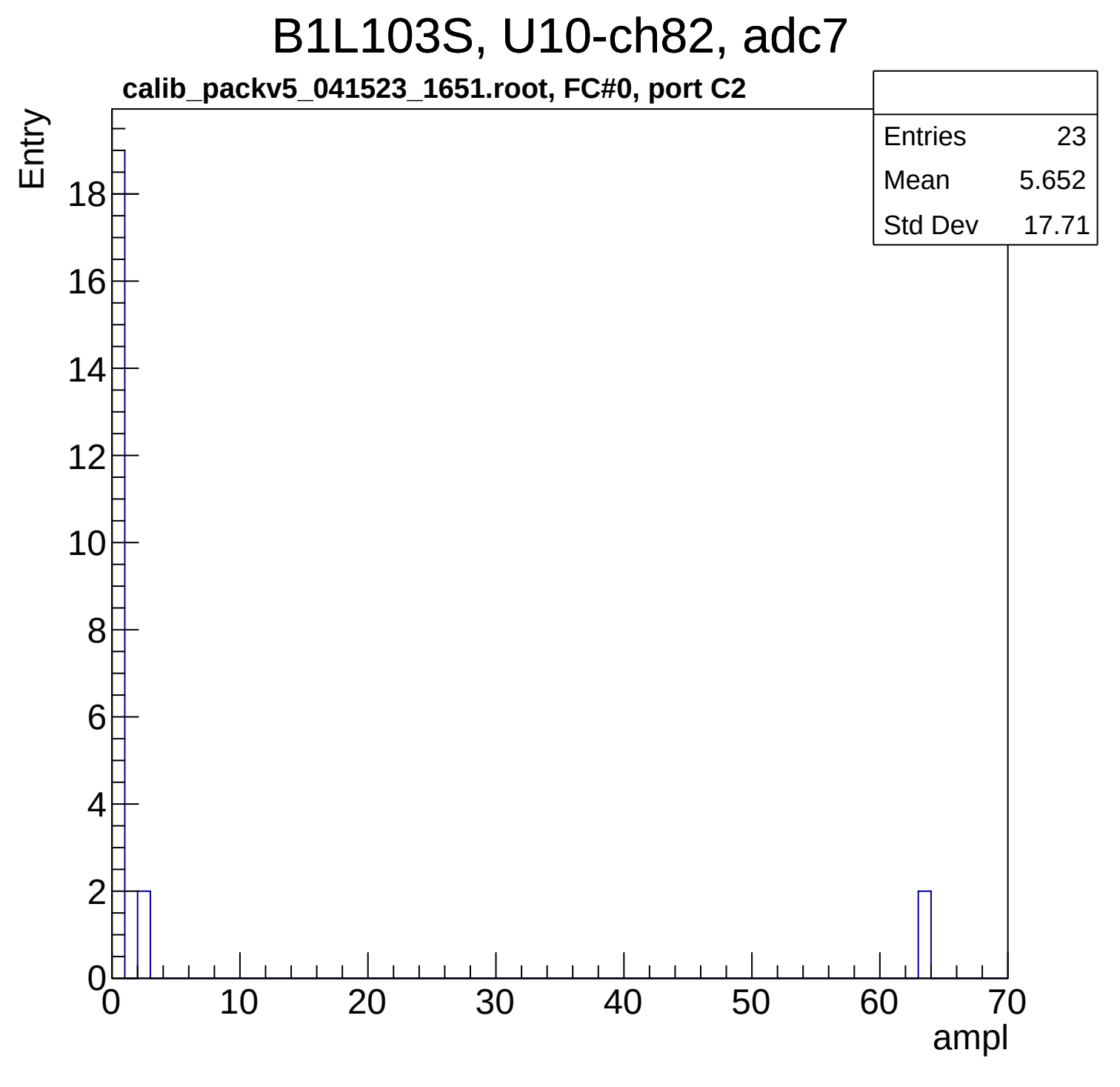
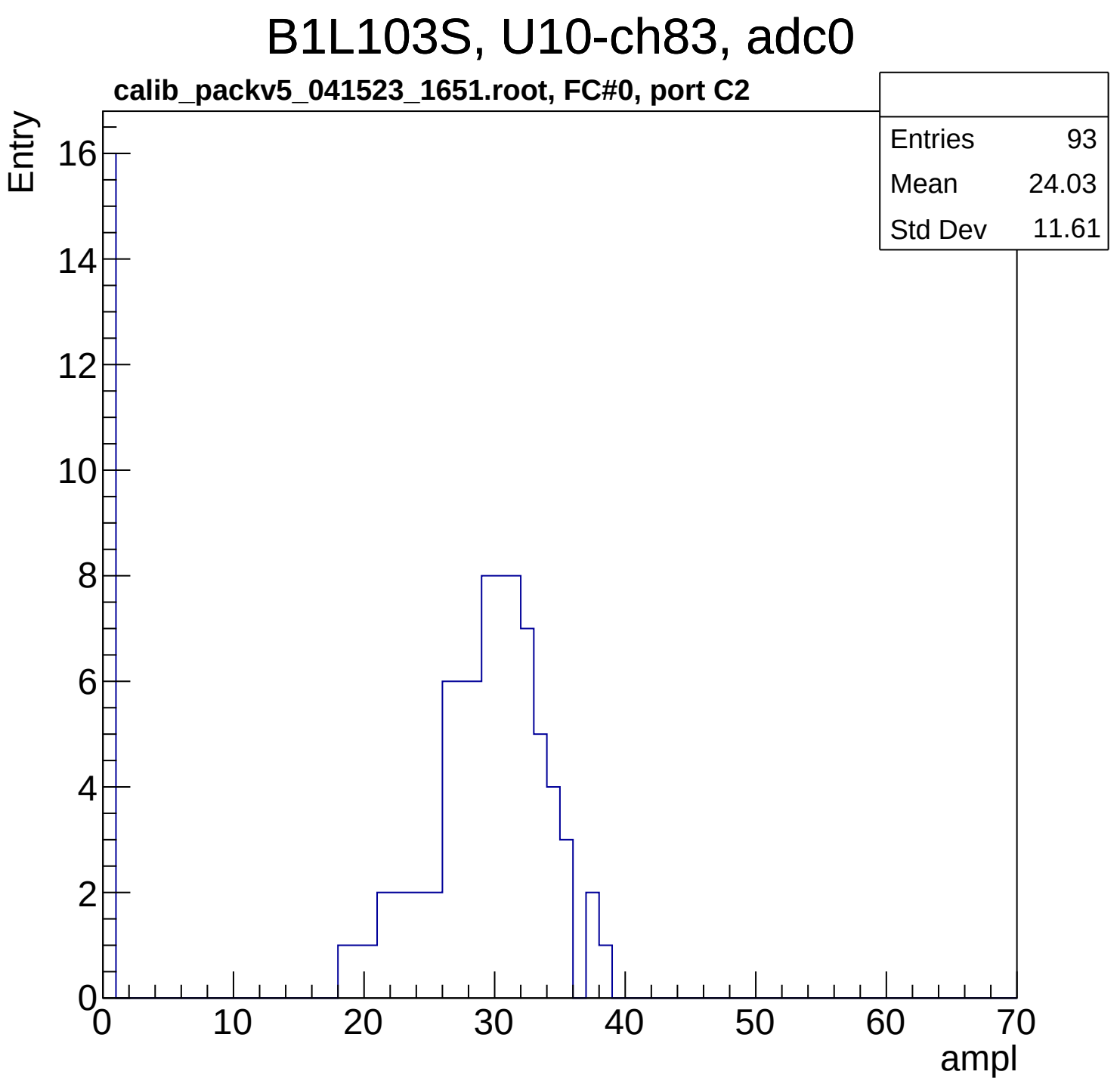
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U10-ch82, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 23
Mean 5.652
Std Dev 17.71
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70


B1L103S, U10-ch83, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 93
Mean 24.03
Std Dev 11.61
Entry
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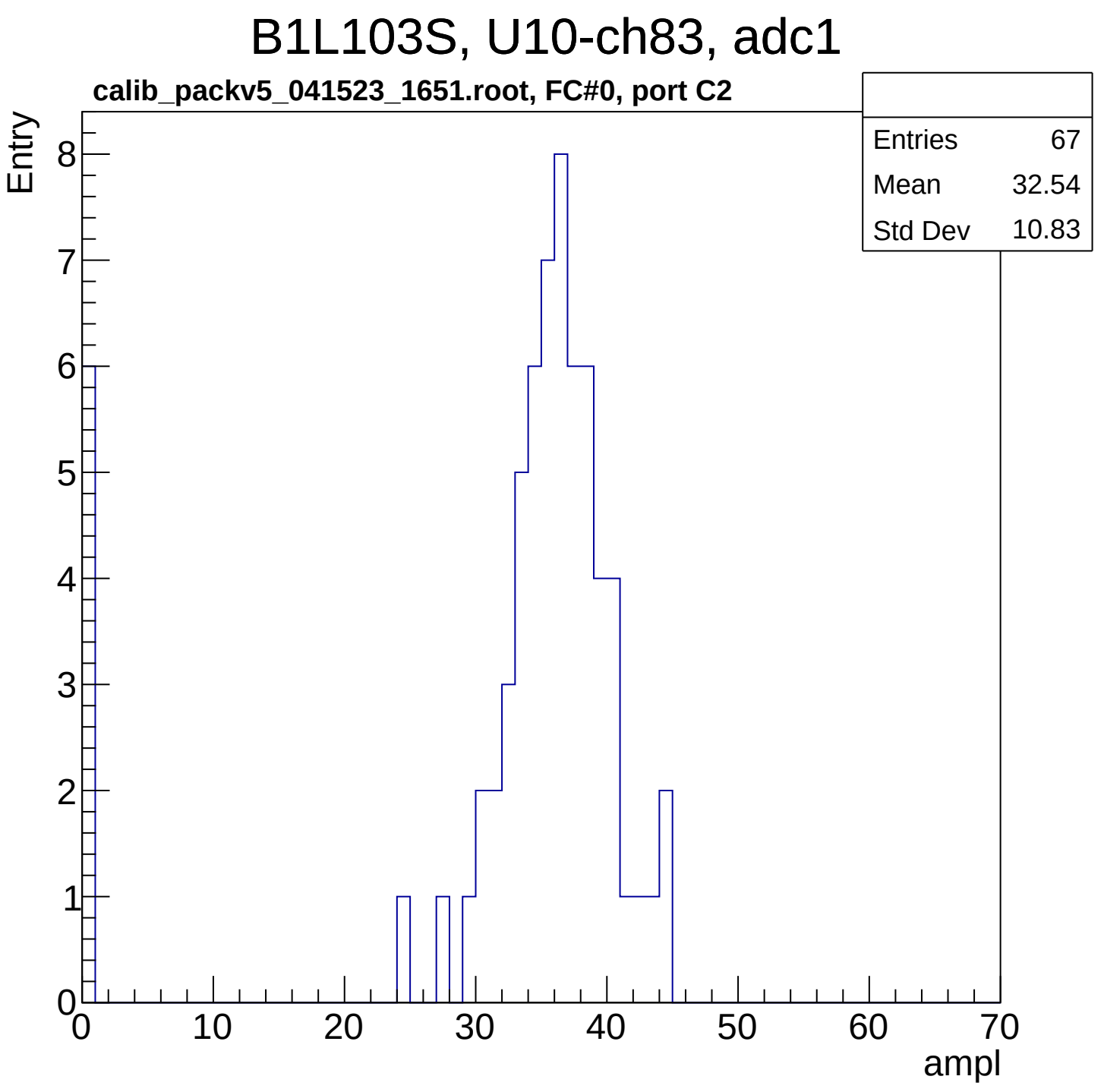
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch83, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 32.54
Std Dev 10.83
Entry
ampl
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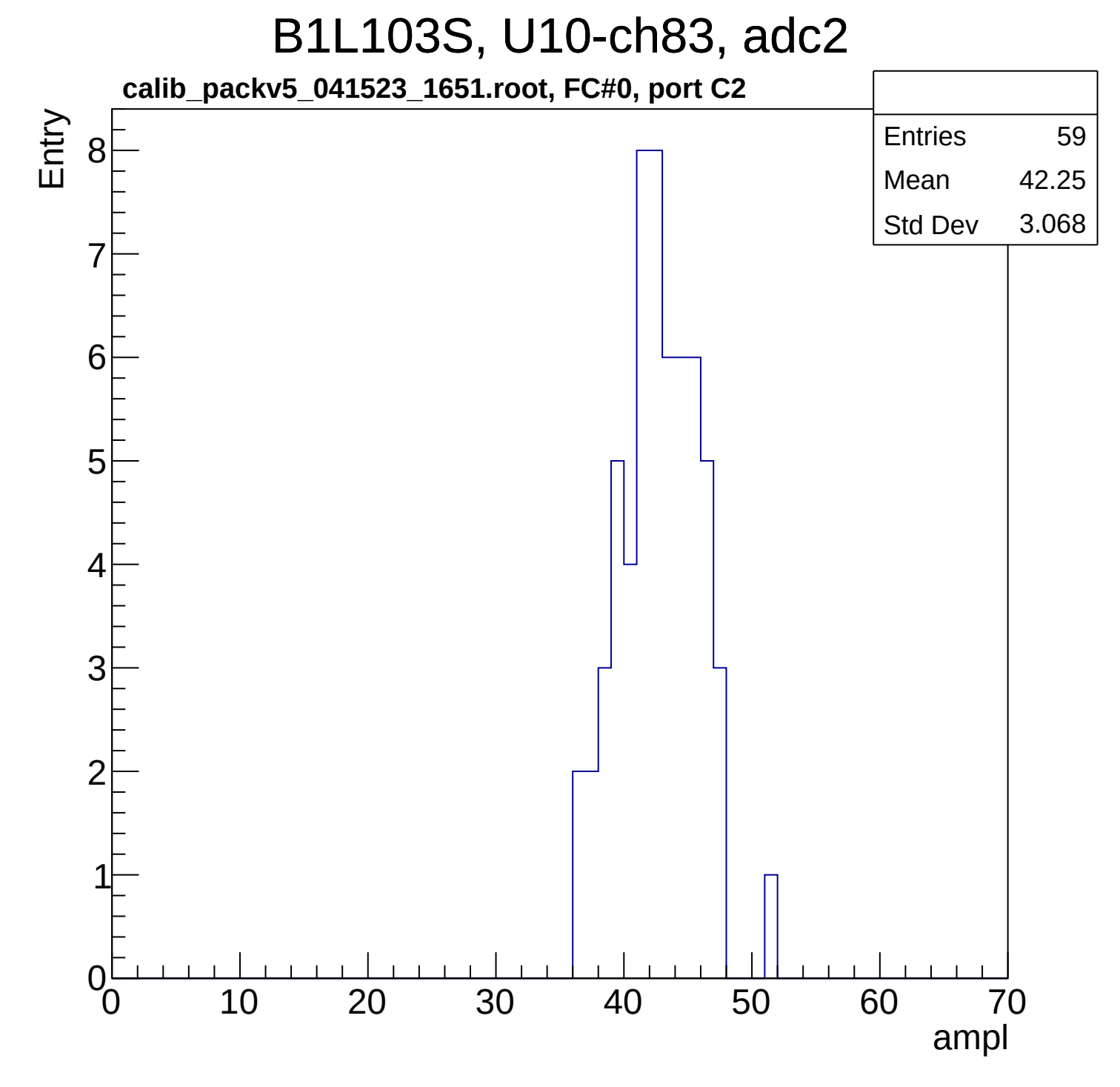
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U10-ch83, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 42.25
Std Dev 3.068
Entry
ampl
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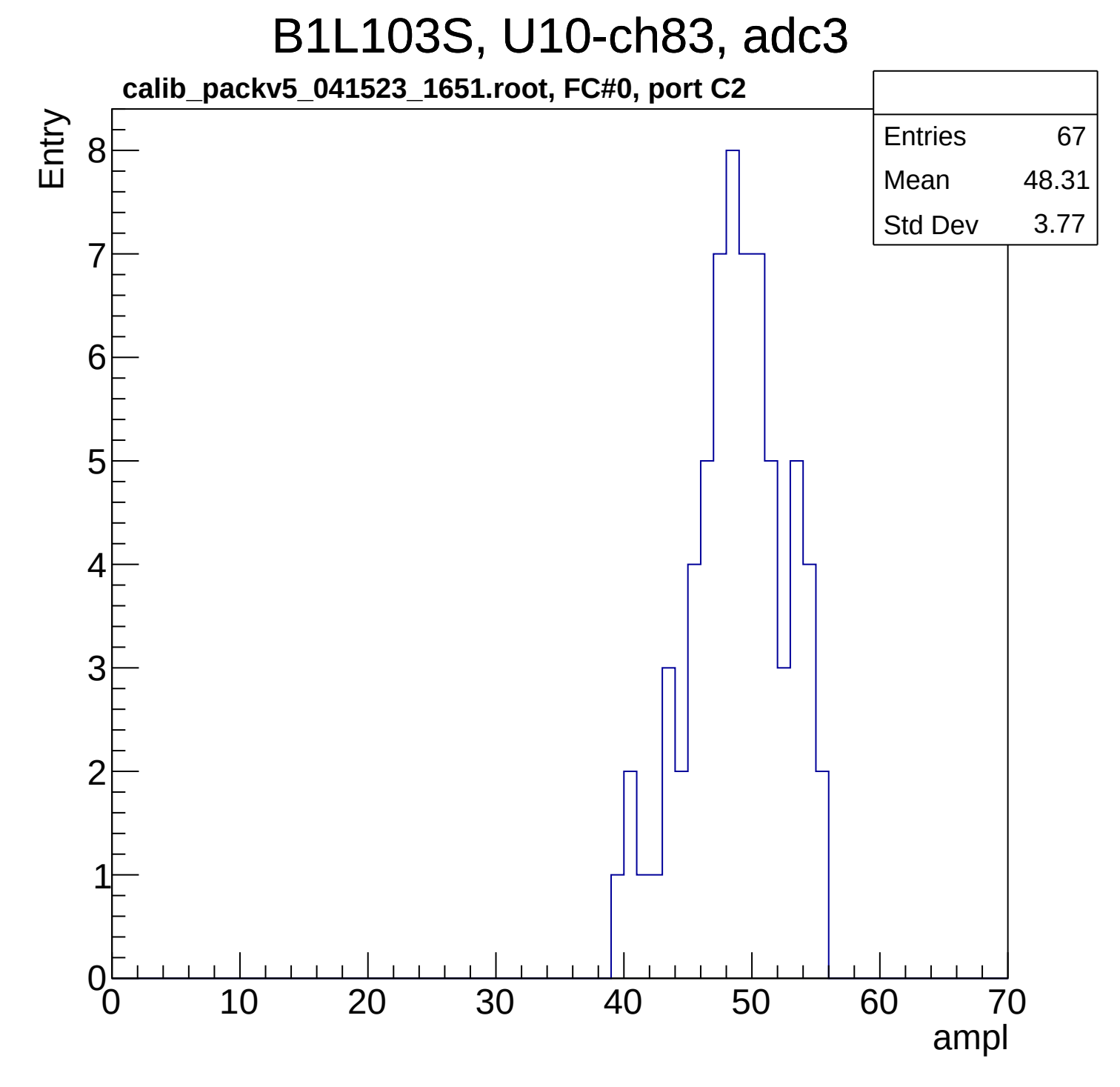
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U10-ch83, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 48.31
Std Dev 3.77
Entry
ampl
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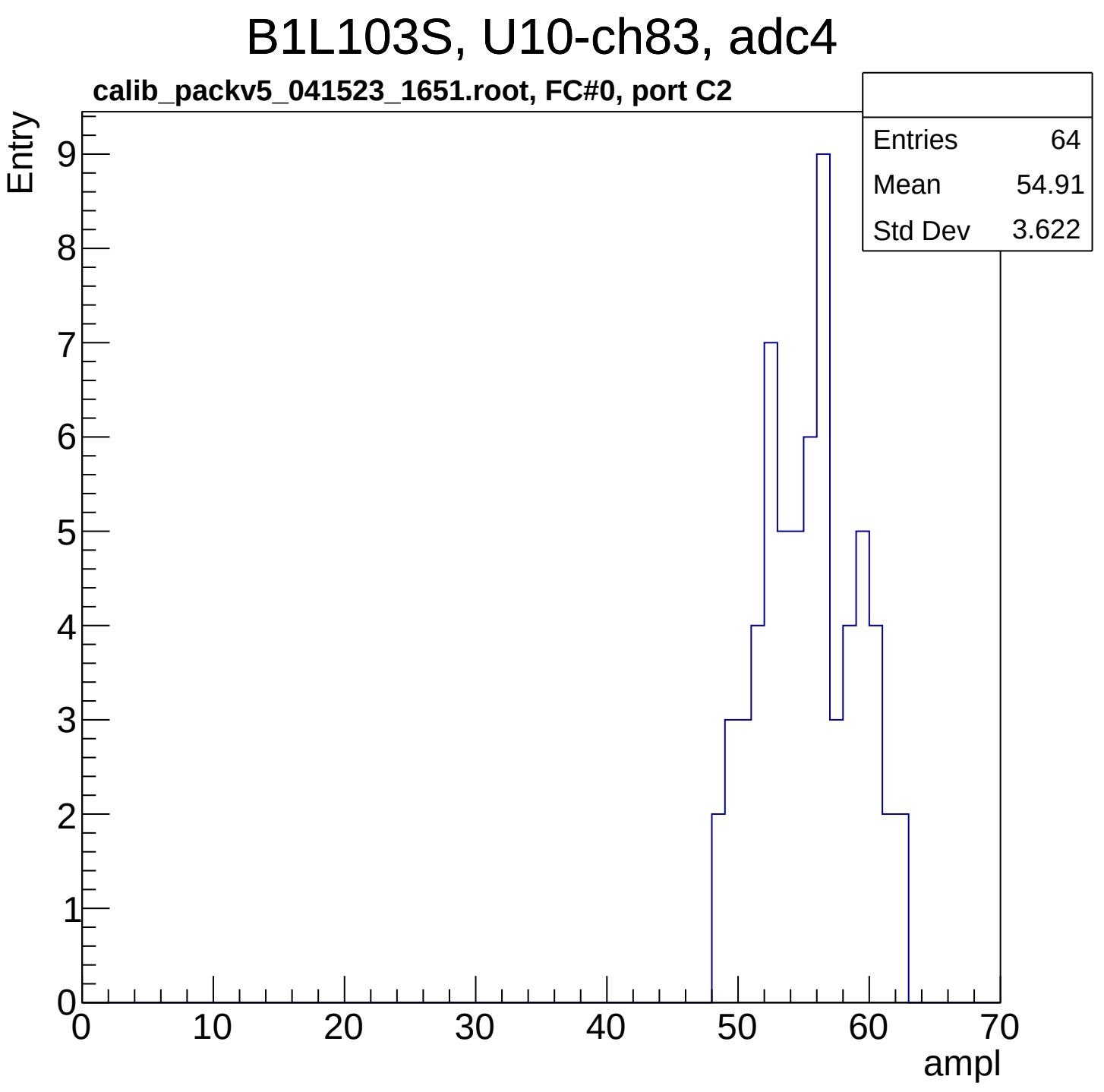
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U10-ch83, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 54.91
Std Dev 3.622
Entry
ampl
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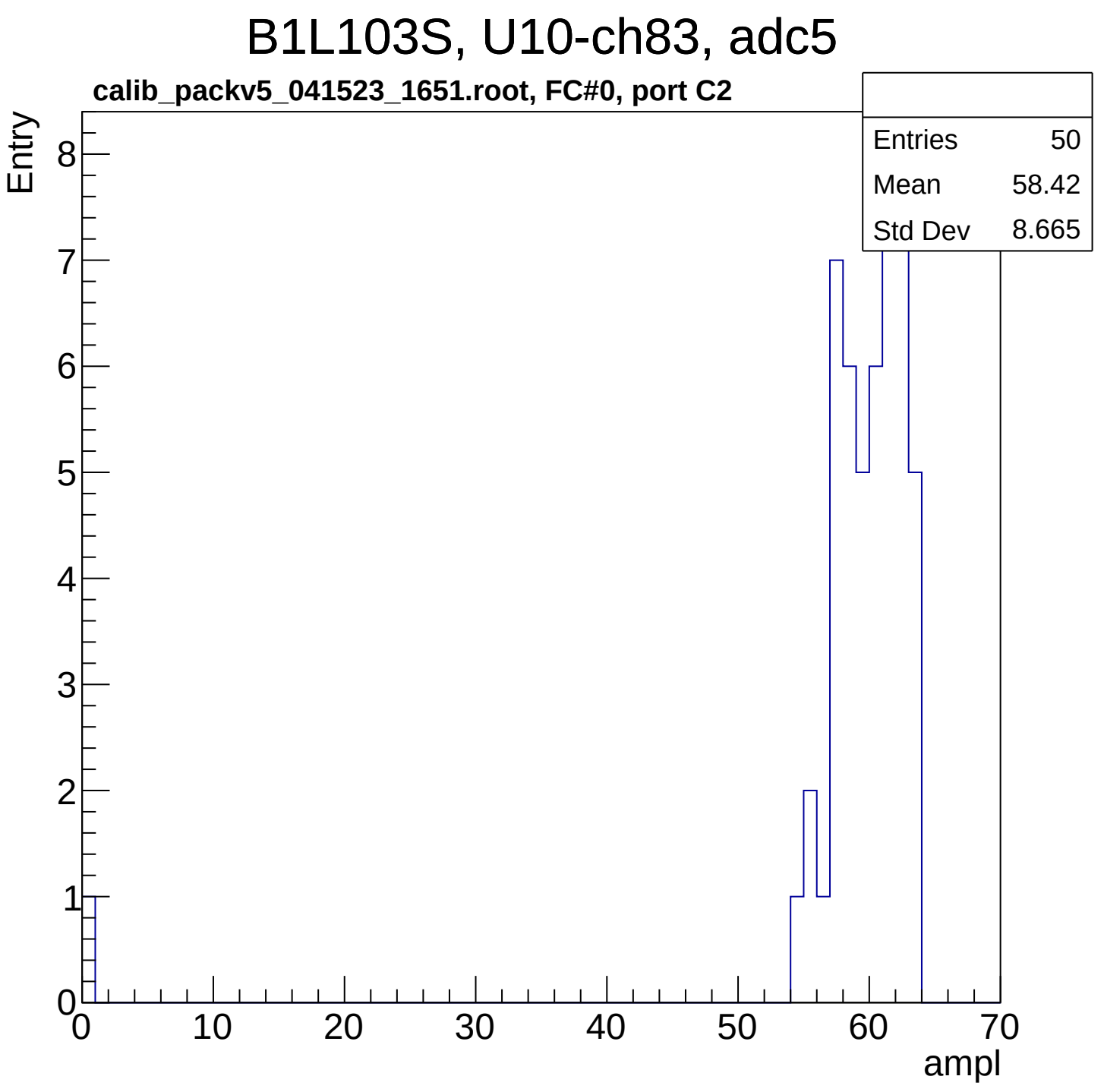
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U10-ch83, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 58.42
Std Dev 8.665
Entry
ampl
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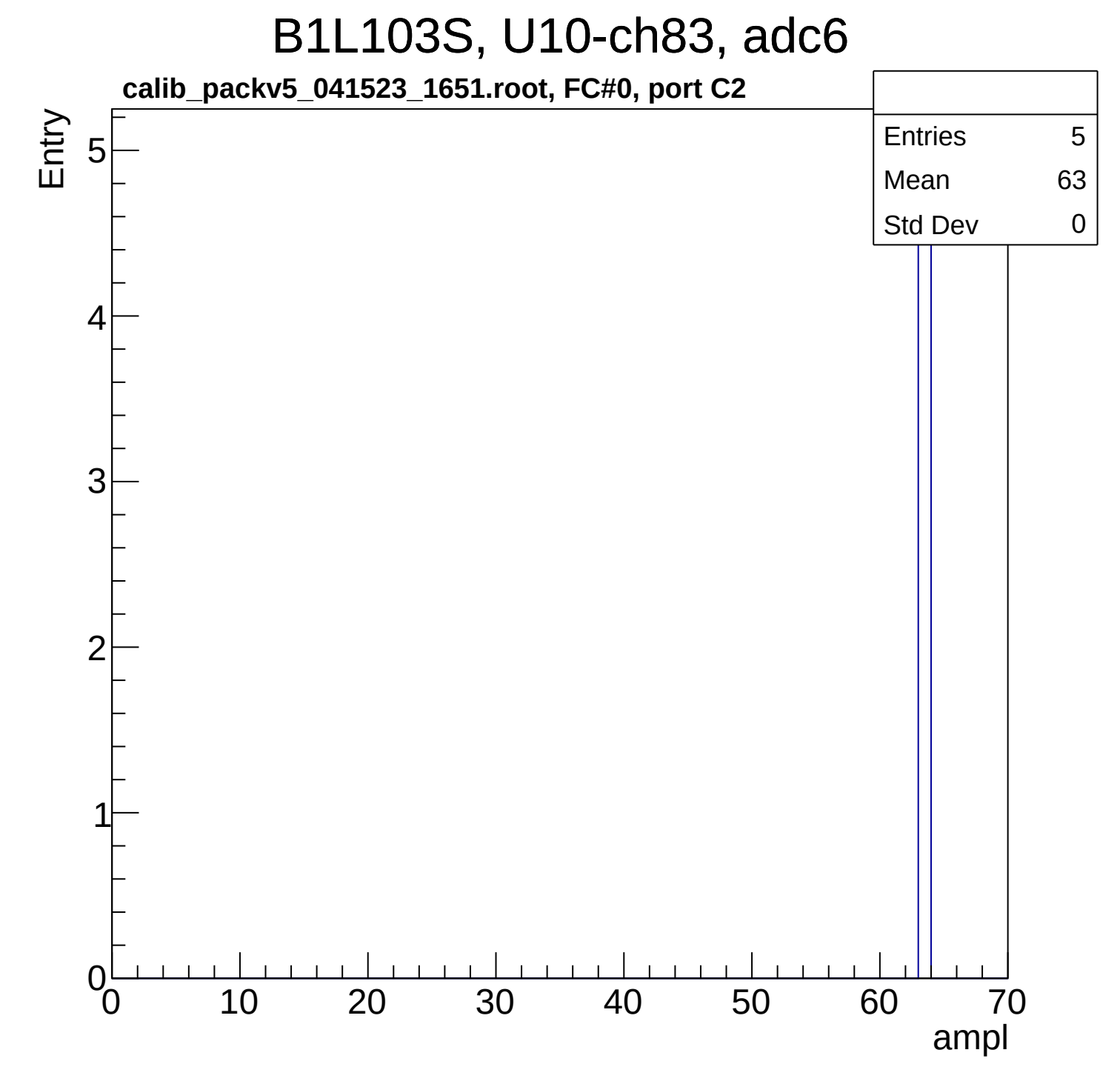
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U10-ch83, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 5
Mean 63
Std Dev 0
Entry
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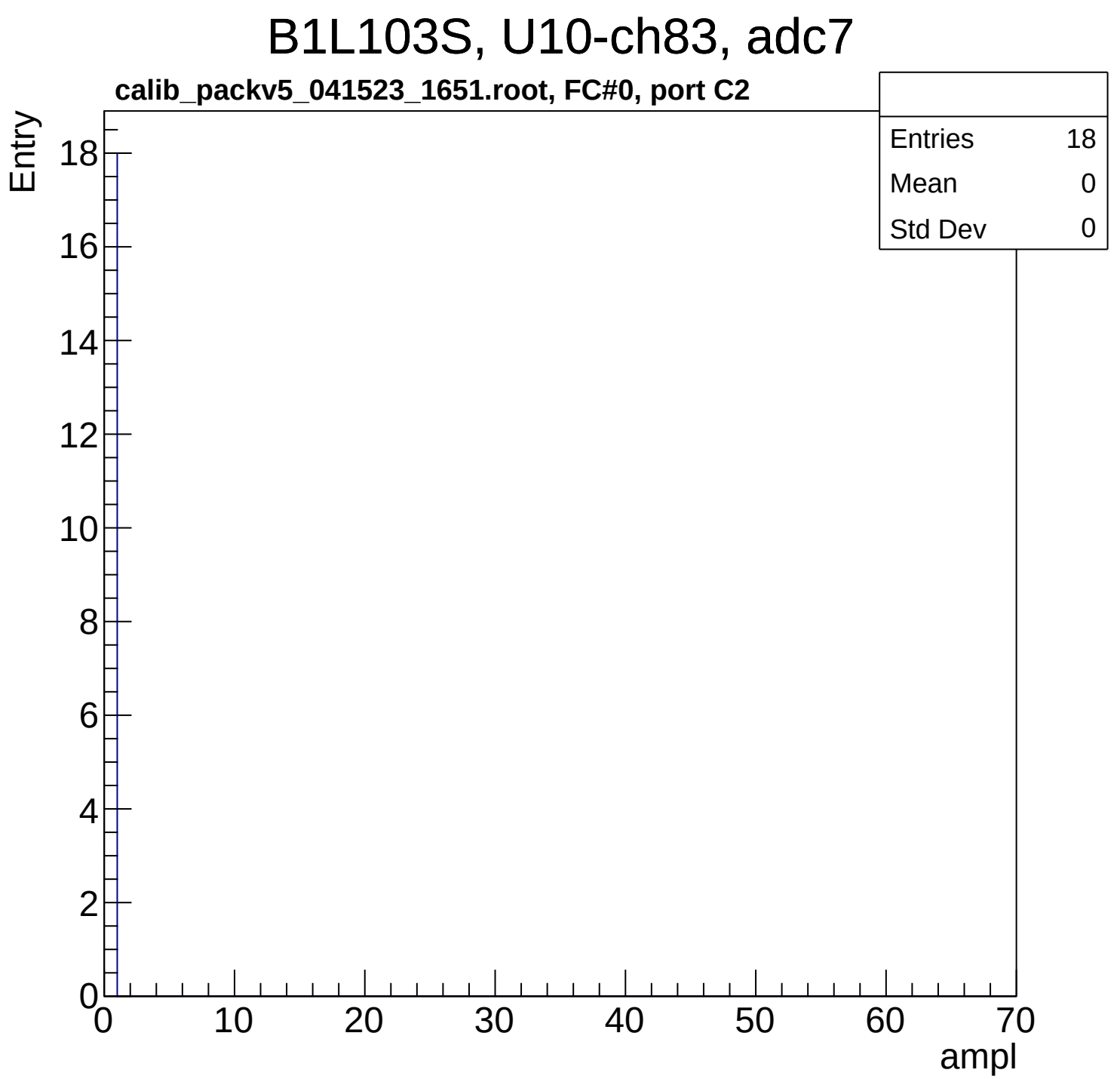
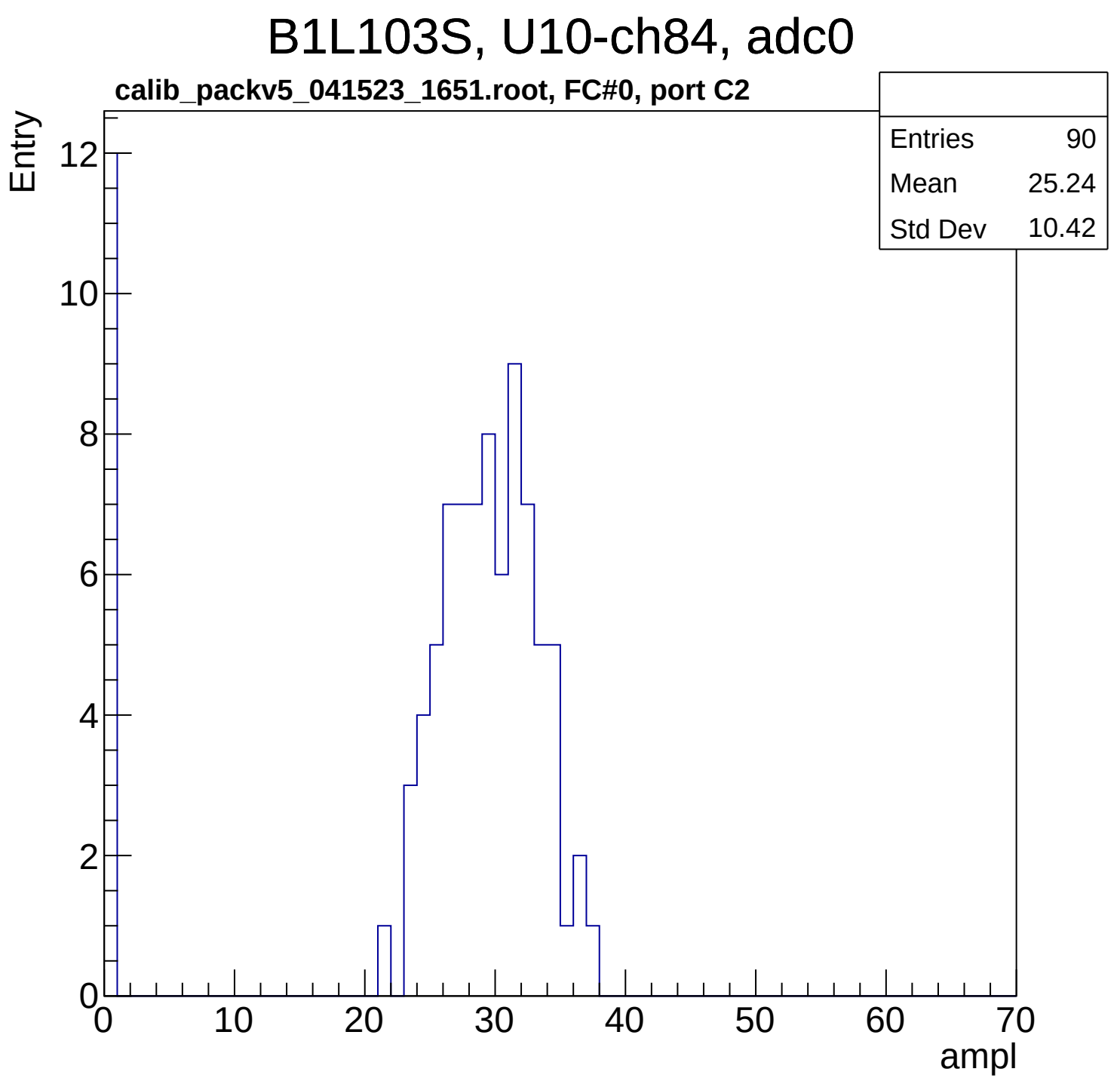
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch83, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch84, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 90
Mean 25.24
Std Dev 10.42
Entry
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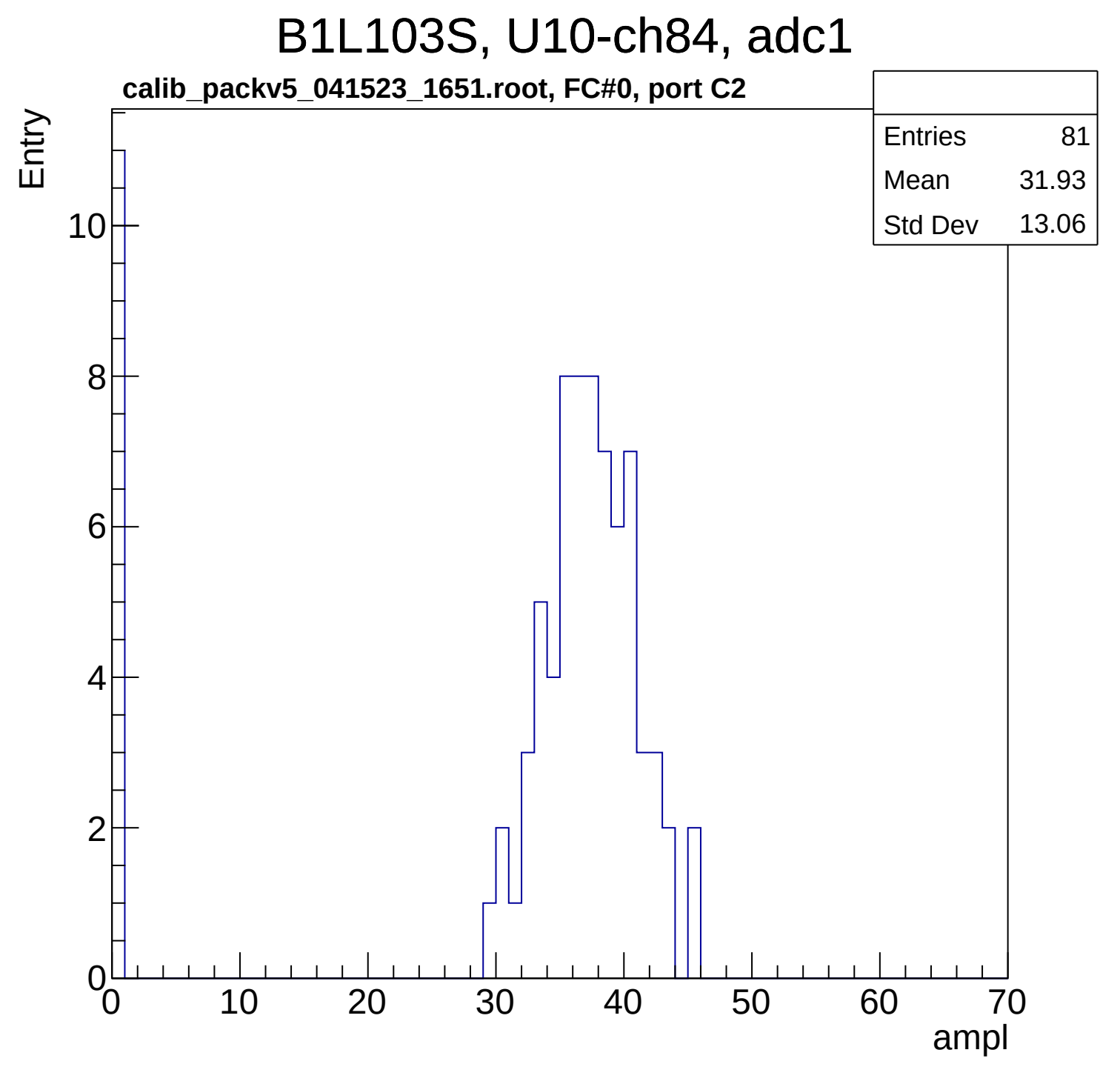
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch84, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 31.93
Std Dev 13.06
Entry
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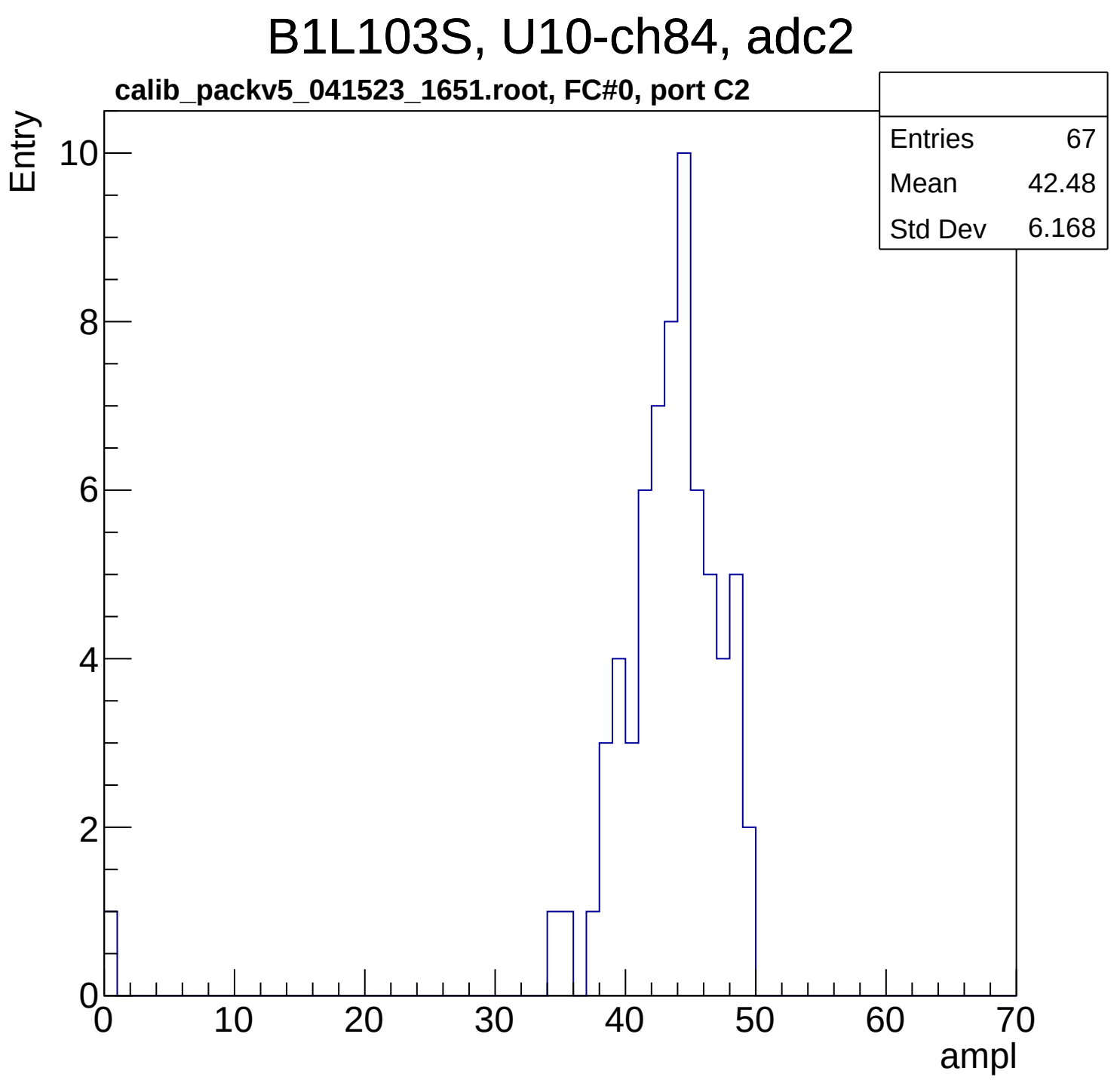
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch84, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 42.48
Std Dev 6.168
Entry
ampl
0
2
4
6
8
10
0
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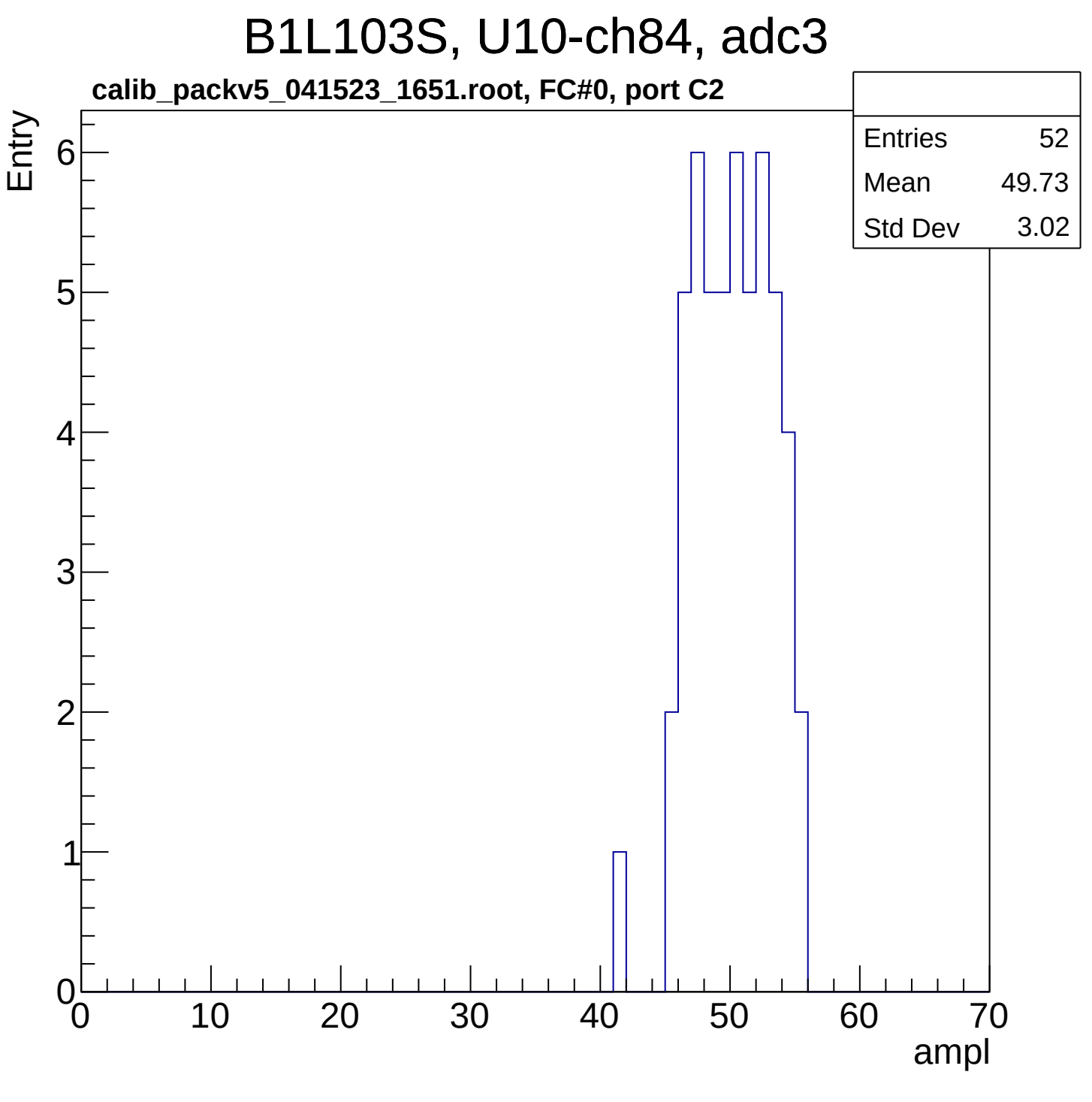
20
30
40
50
60
70


B1L103S, U10-ch84, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 49.73
Std Dev 3.02
Entry
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2
3
4
5
6
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10
20
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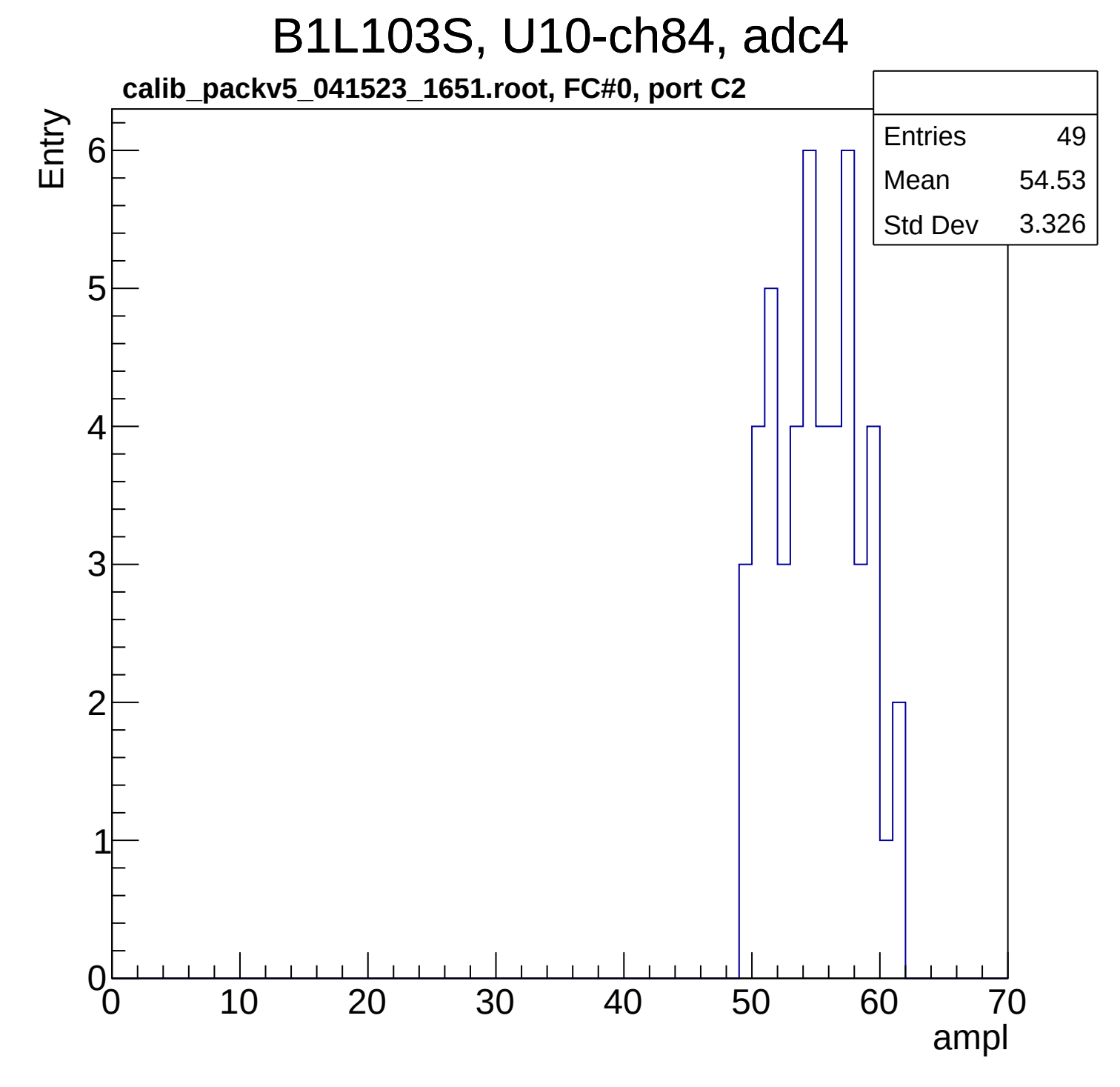
60
70
ampl


B1L103S, U10-ch84, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 54.53
Std Dev 3.326
Entry
ampl
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1
2
3
4
5
6
0
10
20
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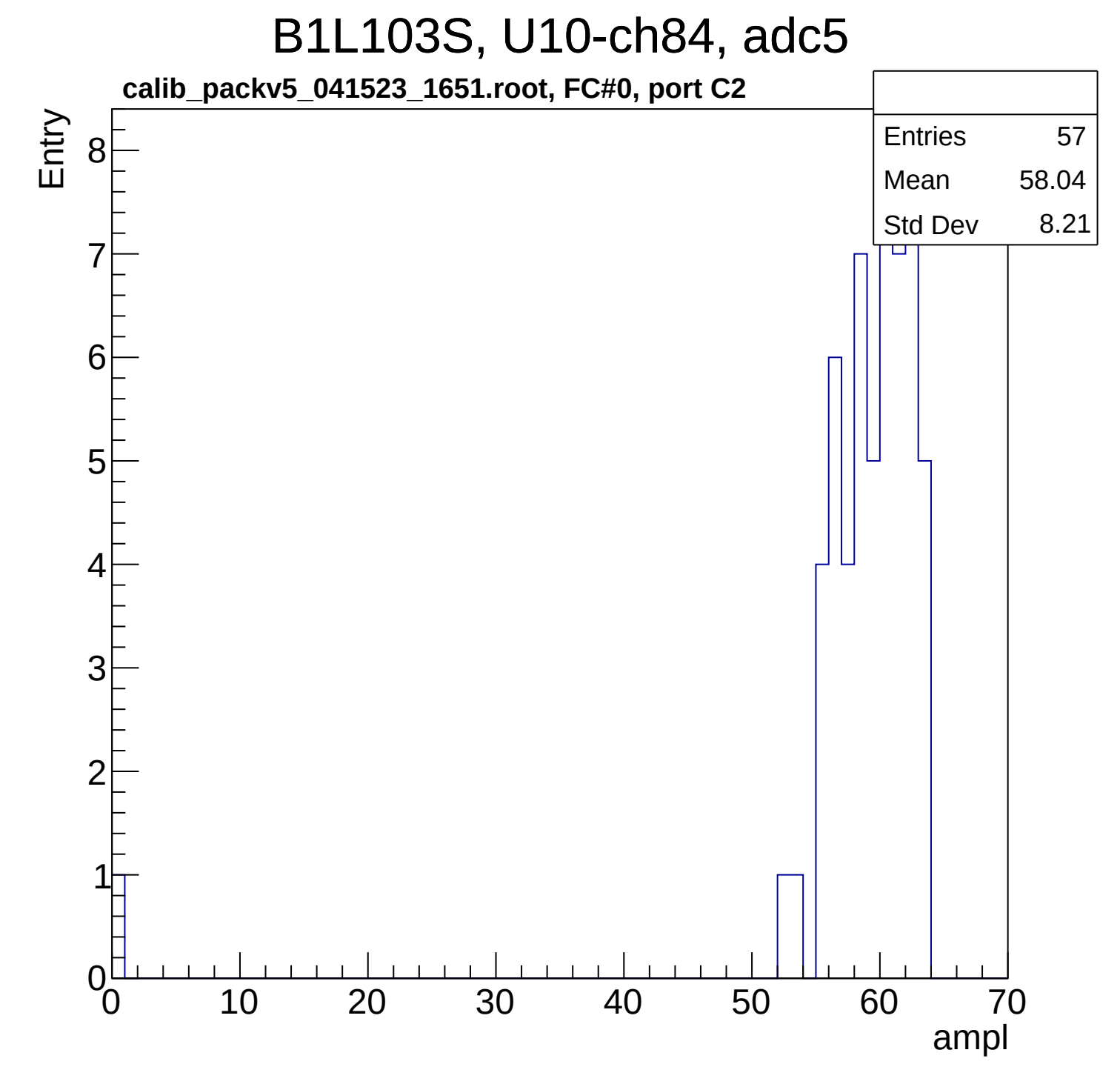
40
50
60
70


B1L103S, U10-ch84, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 58.04
Std Dev 8.21
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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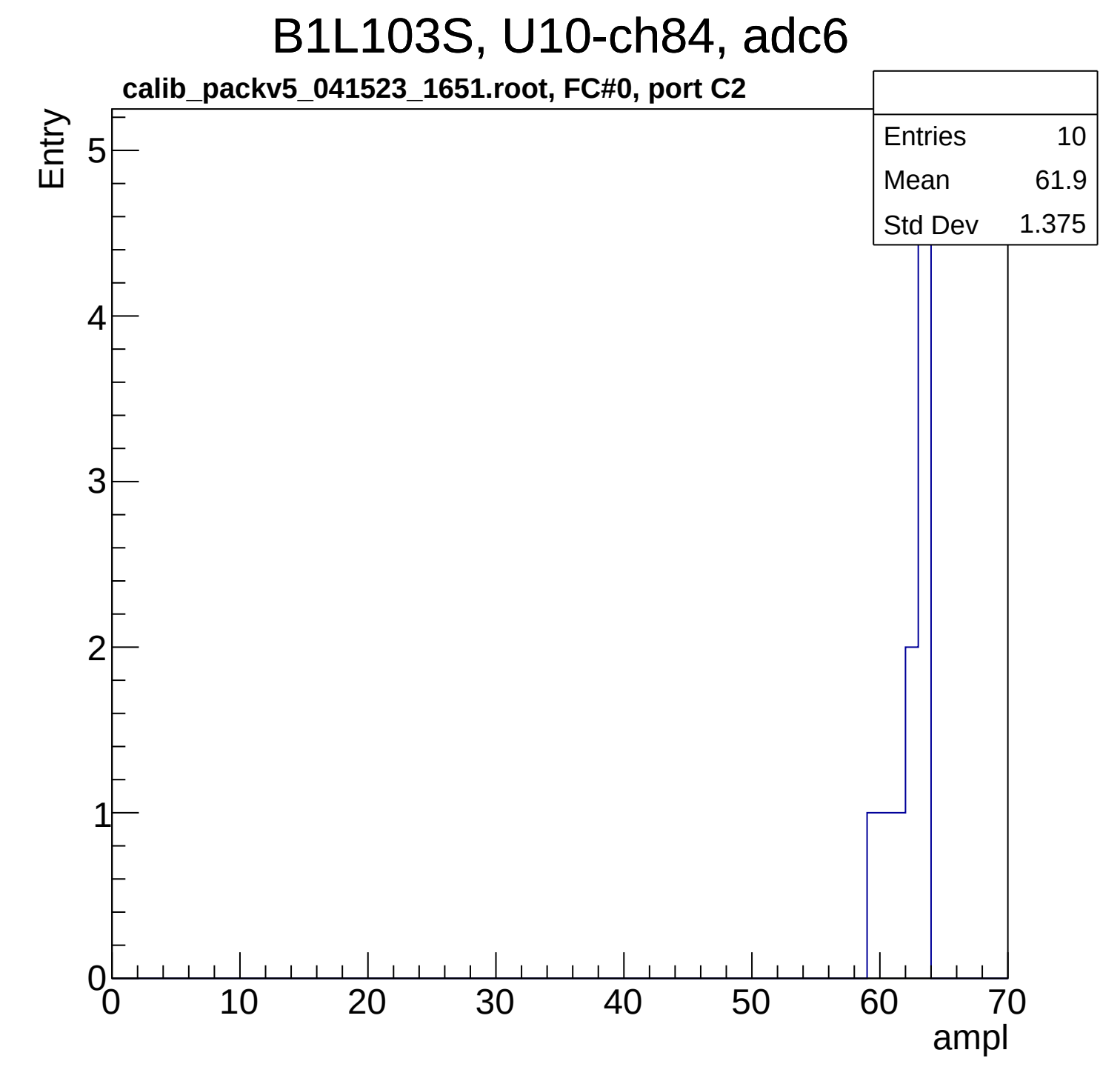
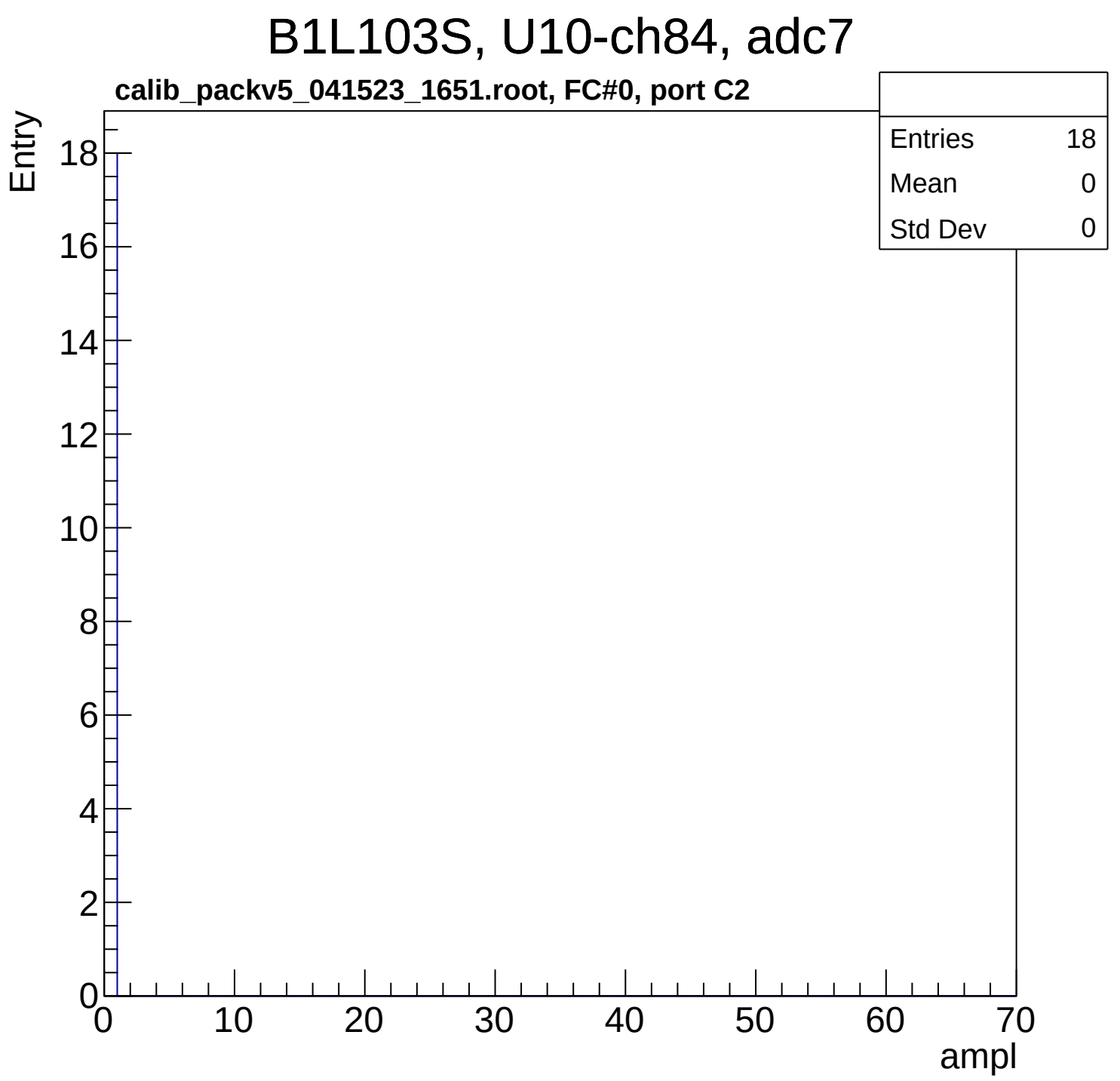
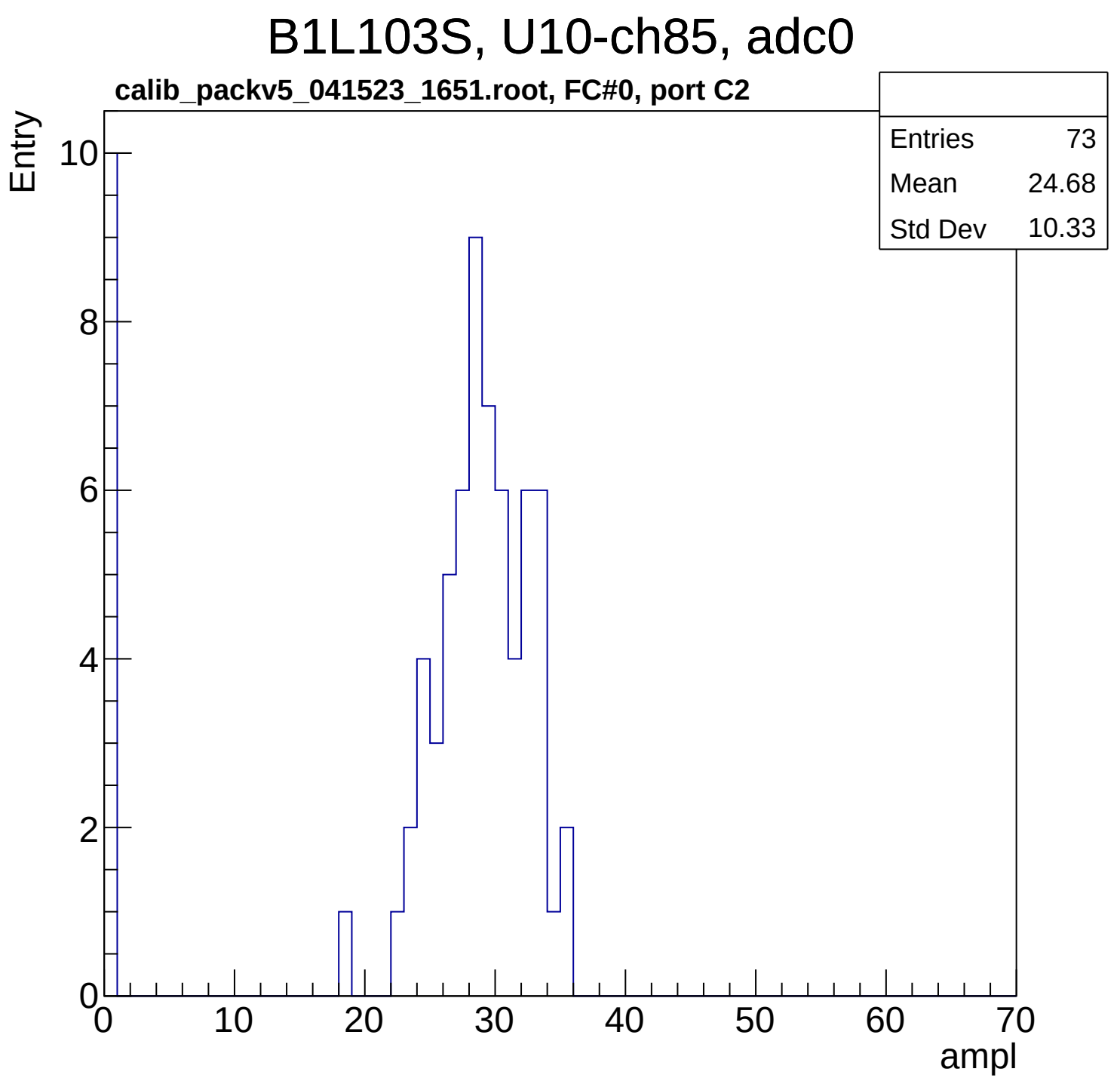
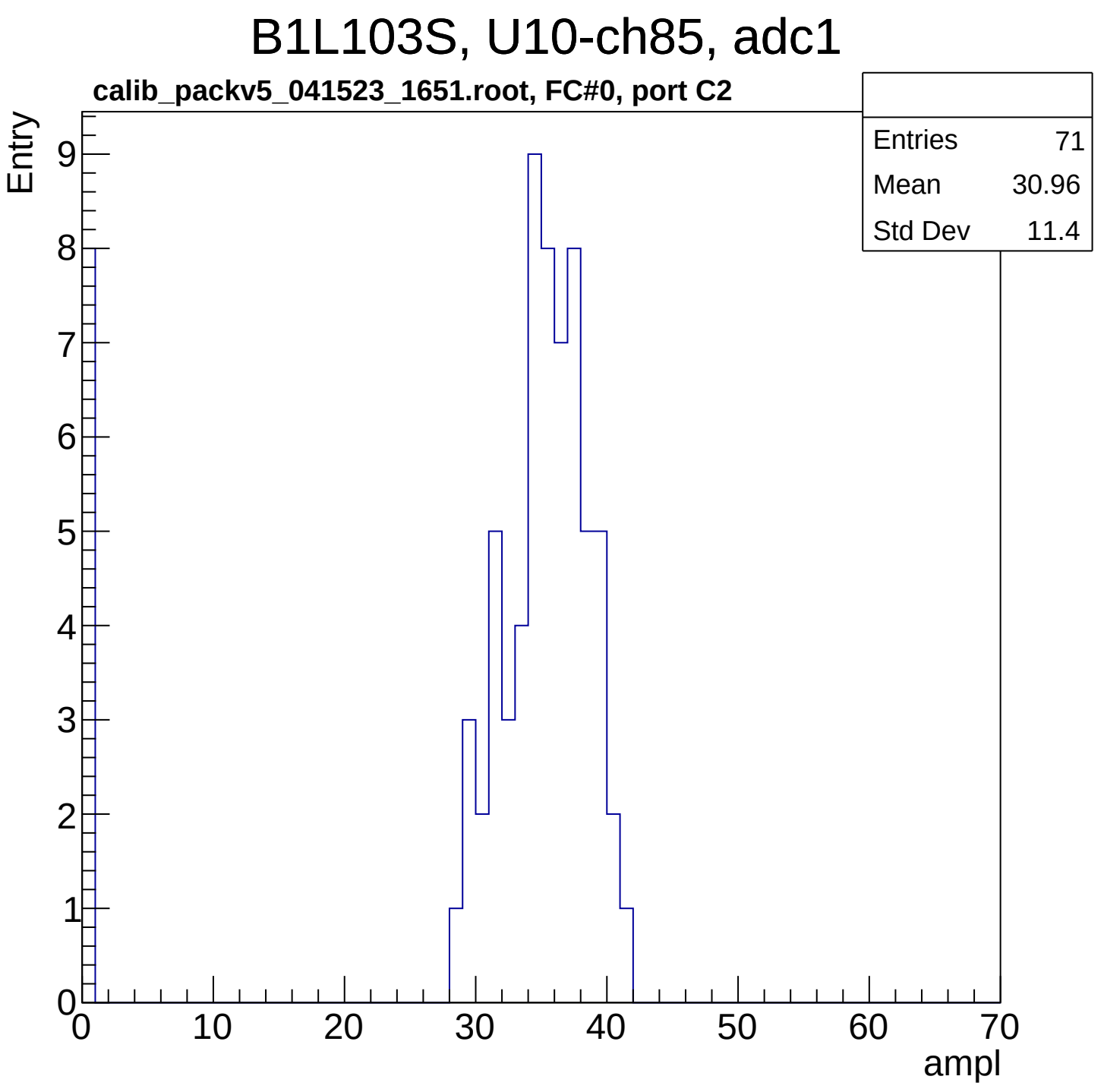
40
50
60
70


B1L103S, U10-ch84, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 61.9
Std Dev 1.375
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U10-ch84, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch85, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 24.68
Std Dev 10.33
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch85, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 30.96
Std Dev 11.4
Entry
ampl
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2
3
4
5
6
7
8
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0
10
20
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40
50
60
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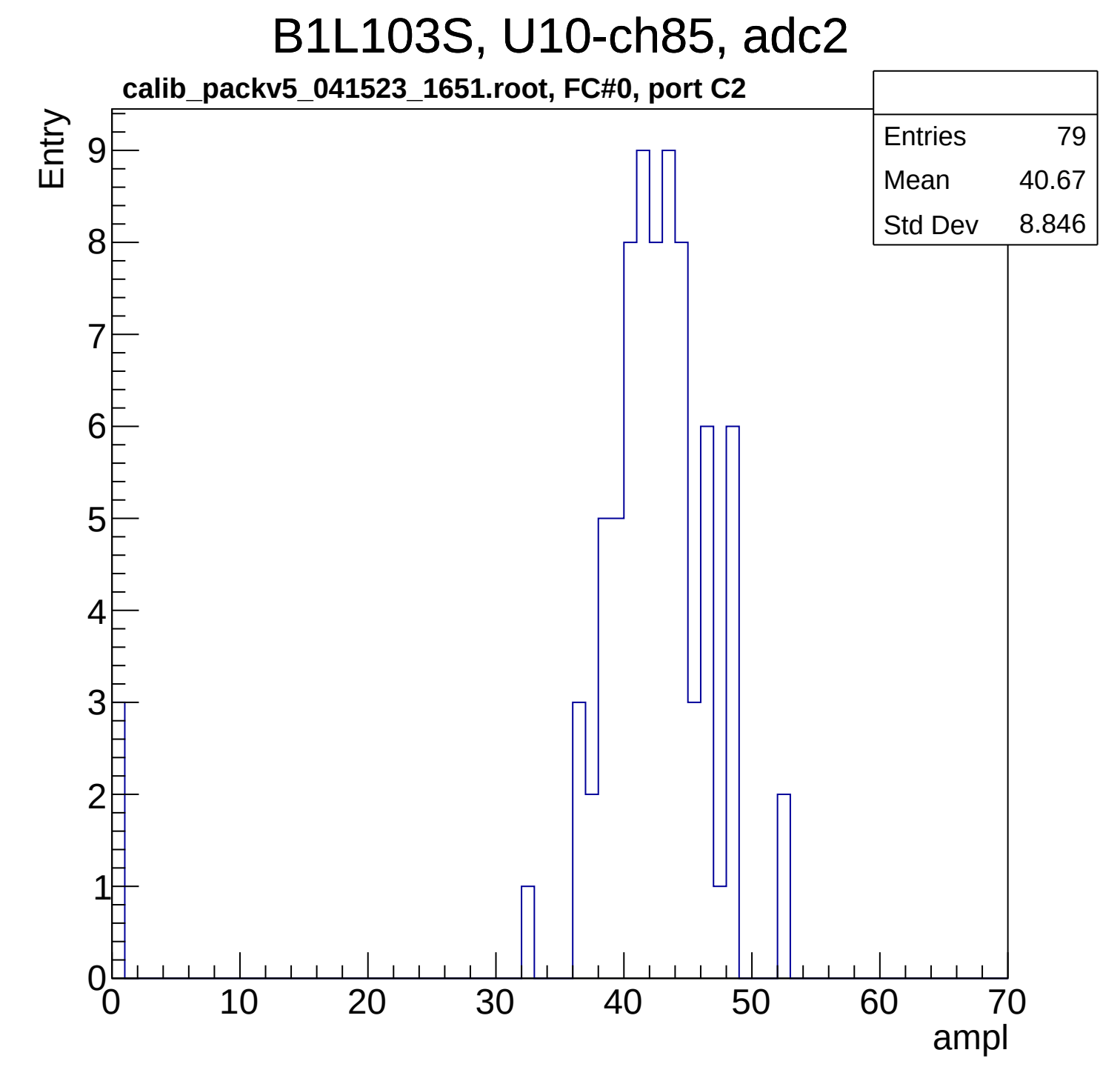
B1L103S, U10-ch85, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 40.67
Std Dev 8.846
Entry
ampl
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2
3
4
5
6
7
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0
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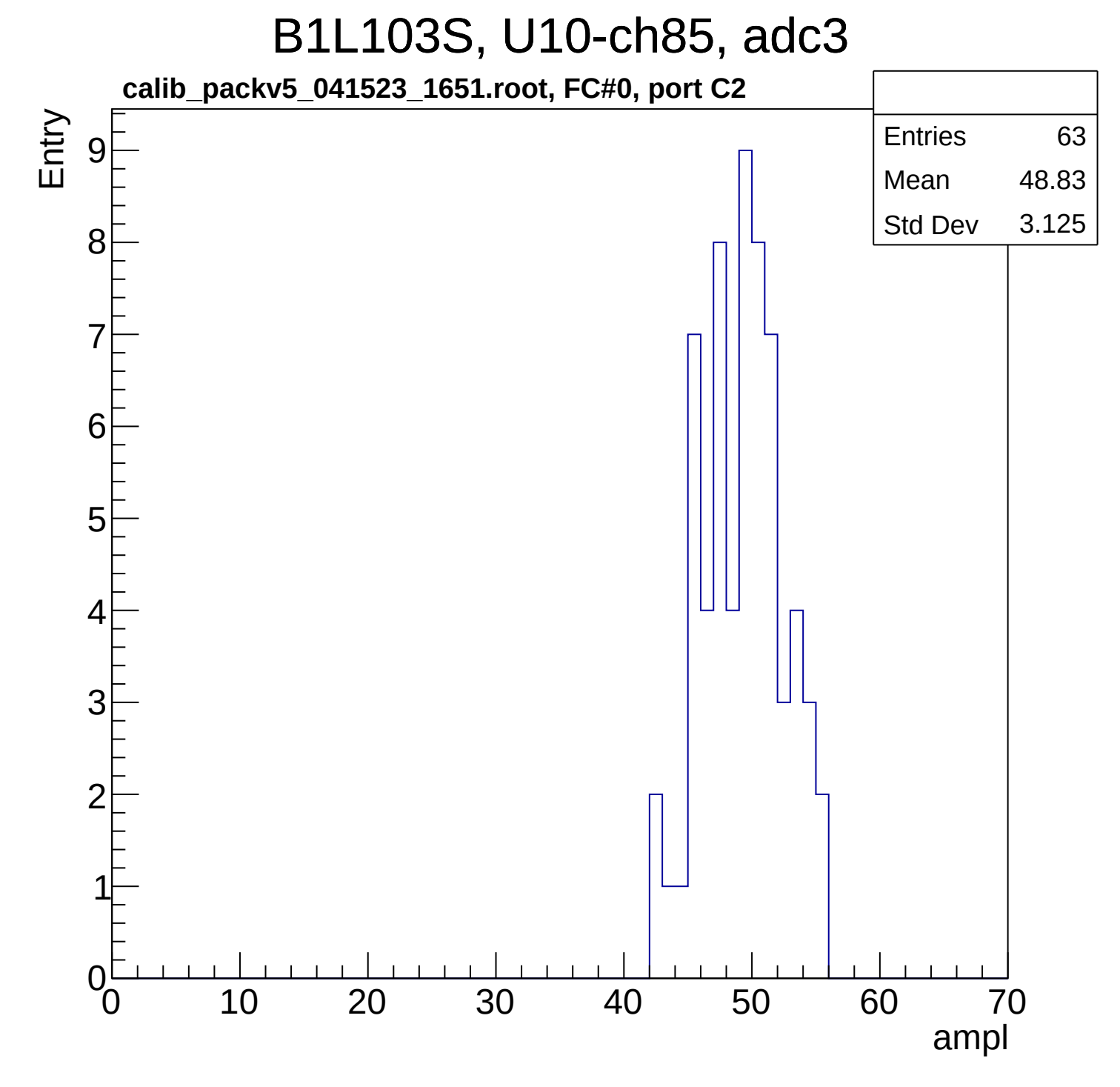
B1L103S, U10-ch85, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 48.83
Std Dev 3.125
Entry
ampl
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3
4
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6
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8
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0
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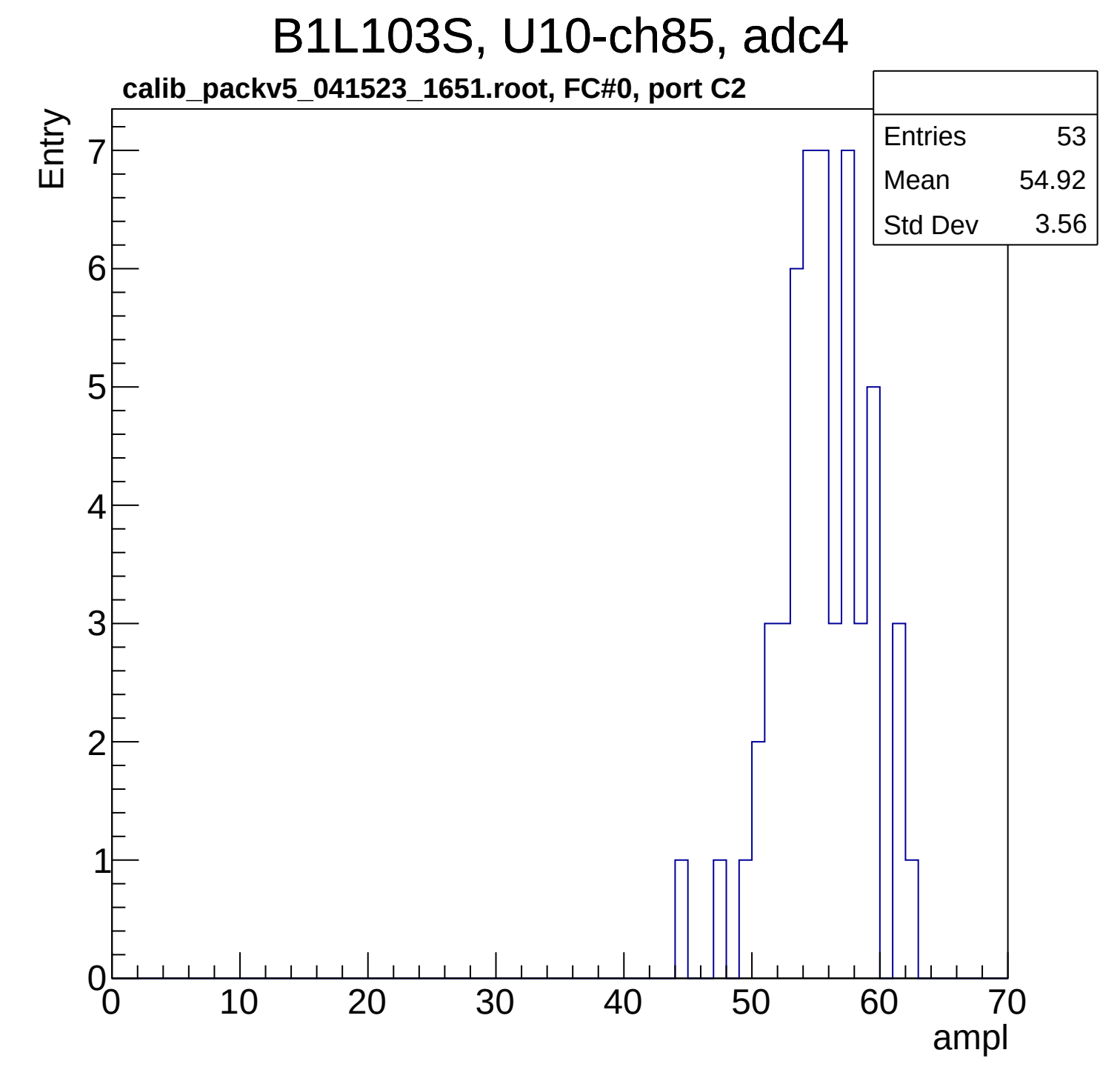
B1L103S, U10-ch85, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 54.92
Std Dev 3.56
Entry
ampl
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4
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0
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40
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60
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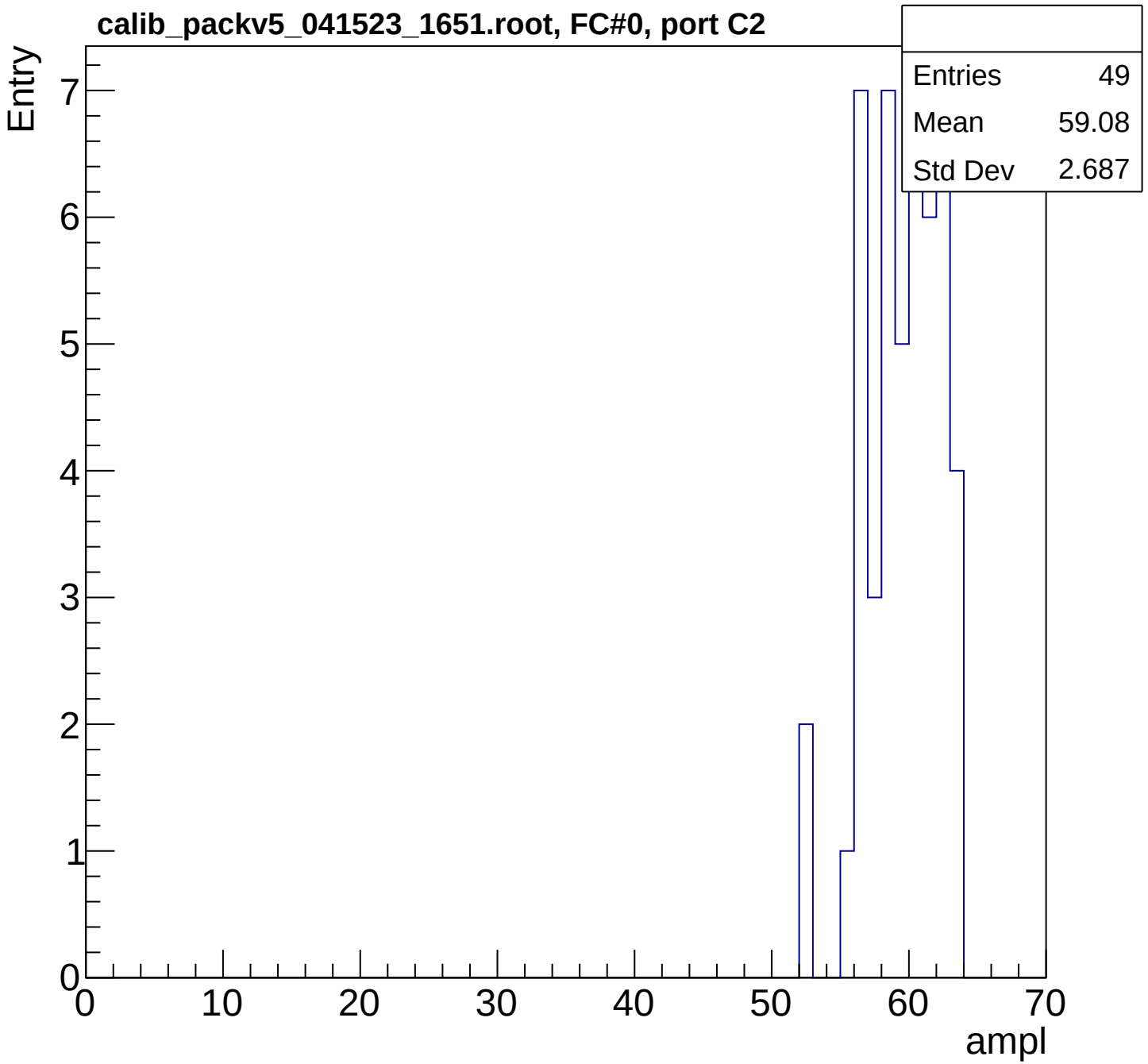
B1L103S, U10-ch85, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 59.08
Std Dev 2.687
Entry
ampl
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6
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0
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40
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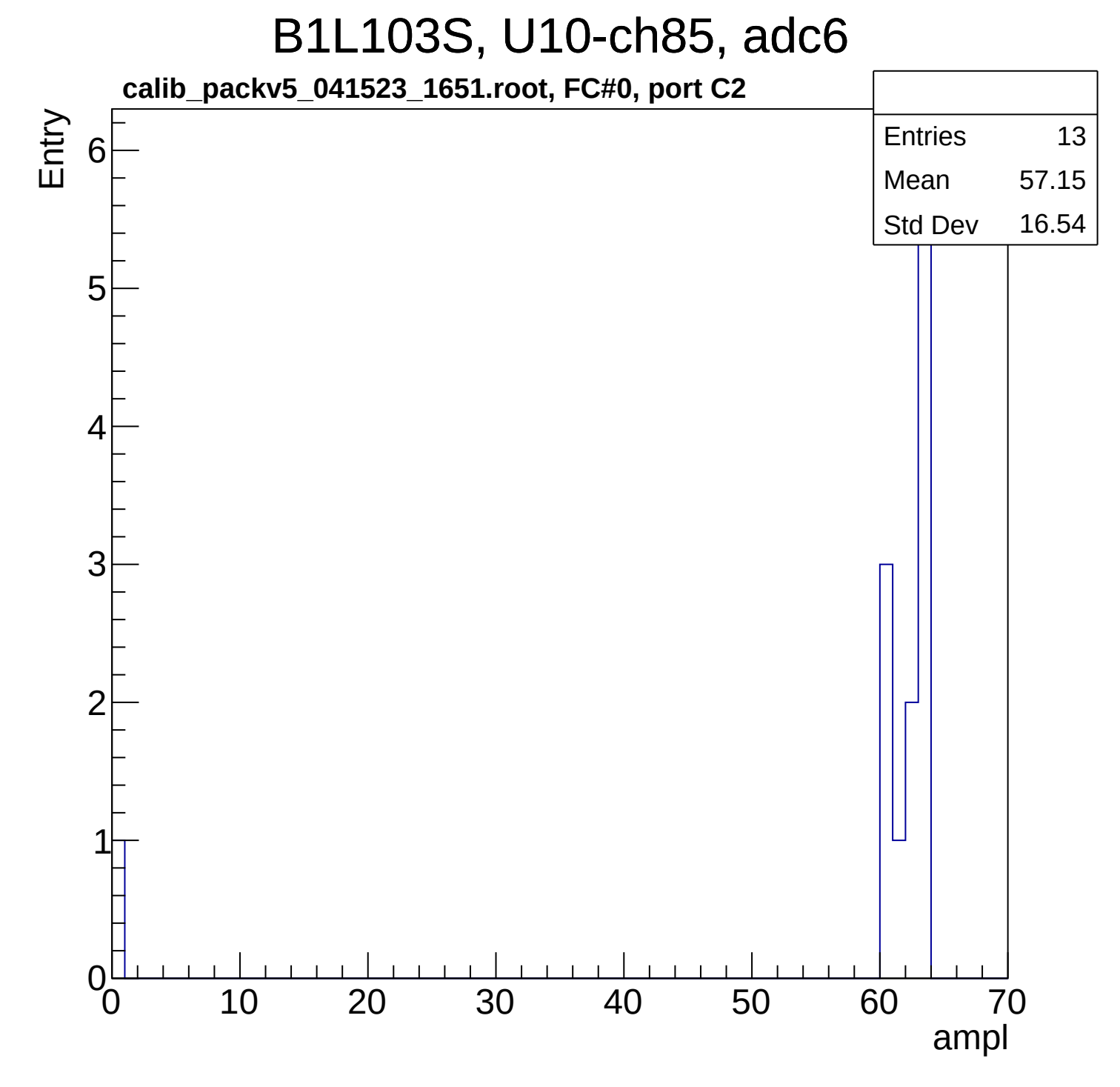
B1L103S, U10-ch85, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 13
Mean 57.15
Std Dev 16.54
Entry
ampl
0
1
2
3
4
5
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0
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40
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60
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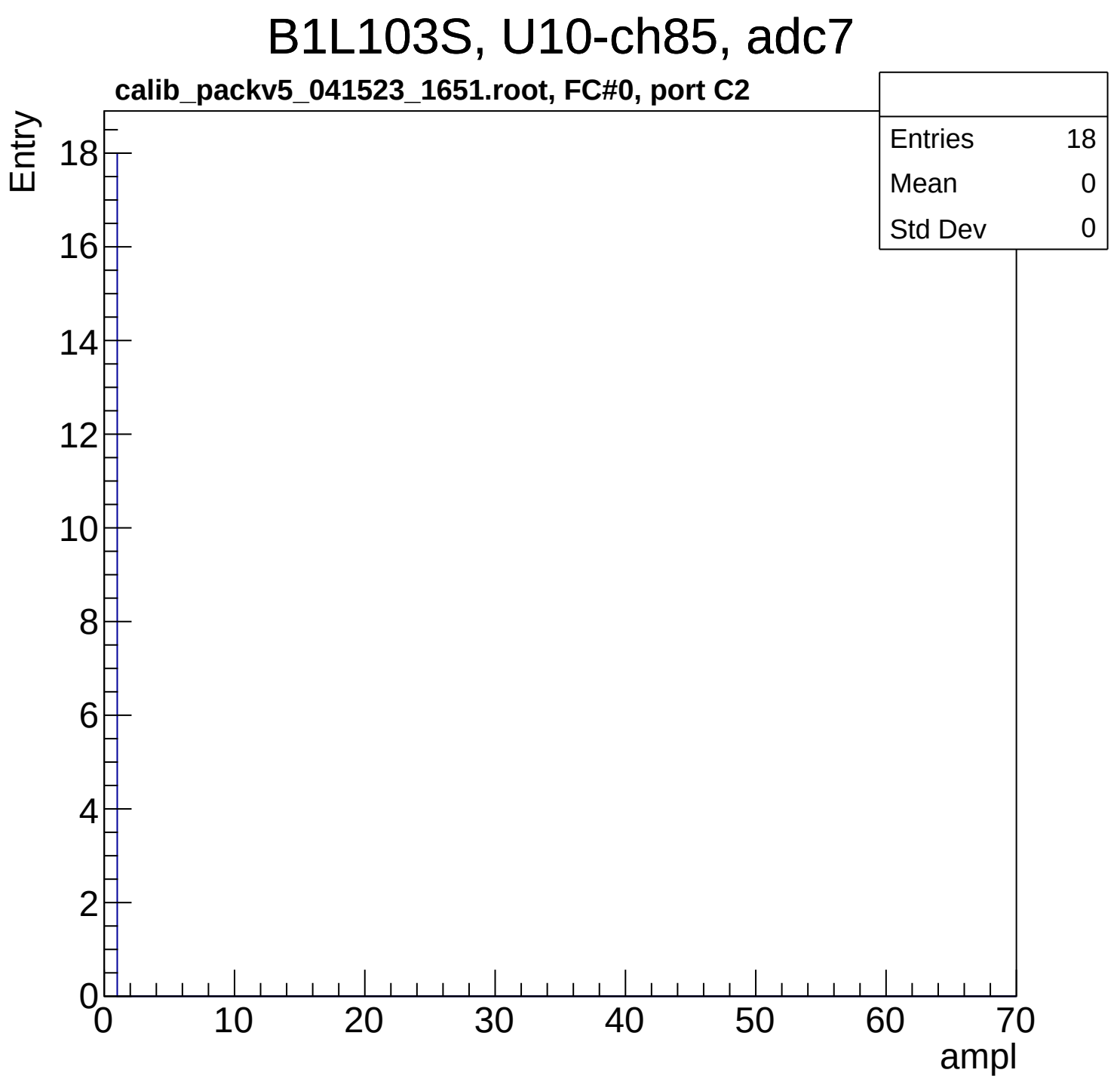
B1L103S, U10-ch85, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
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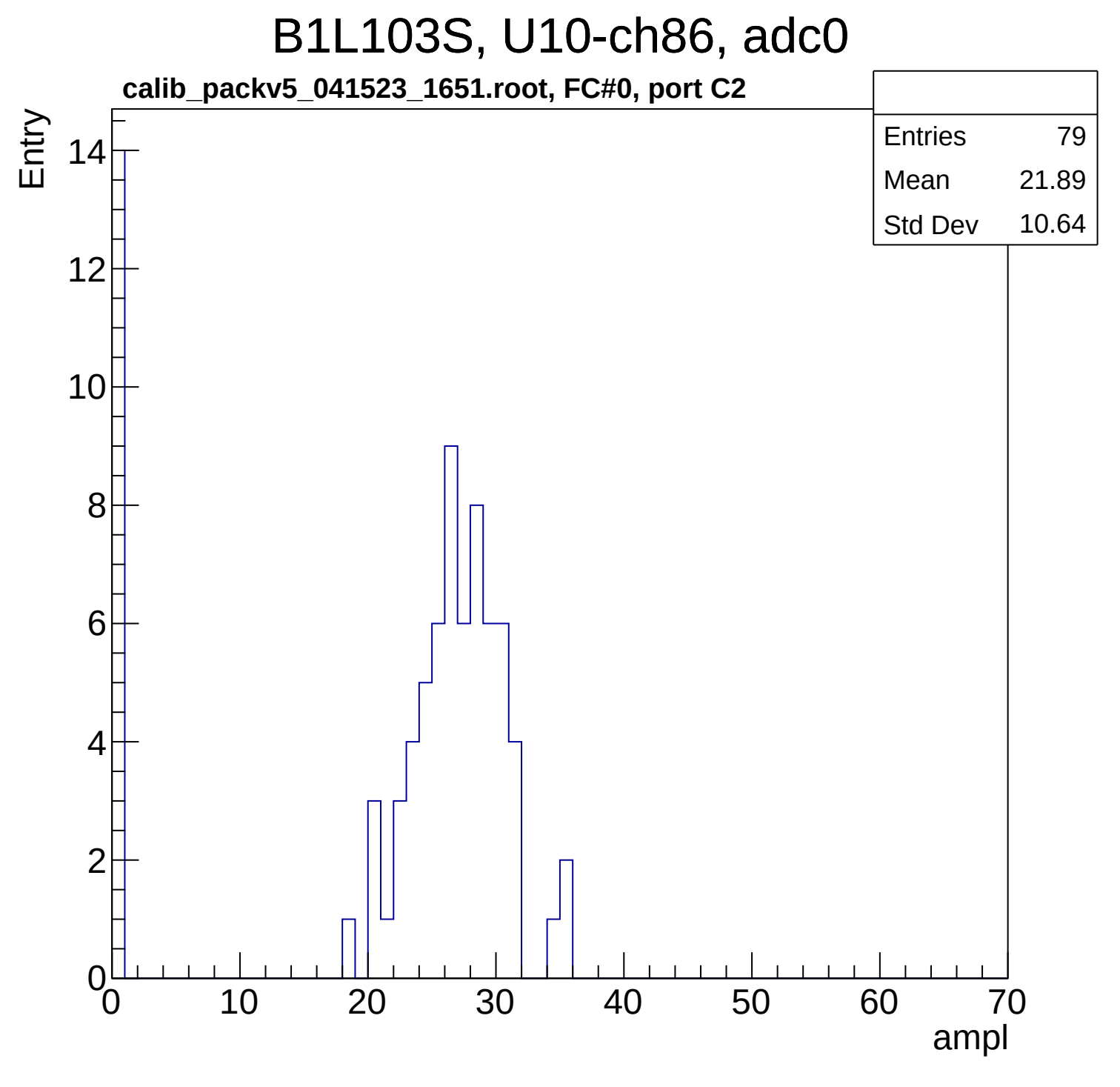
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch86, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 21.89
Std Dev 10.64
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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40
50
60
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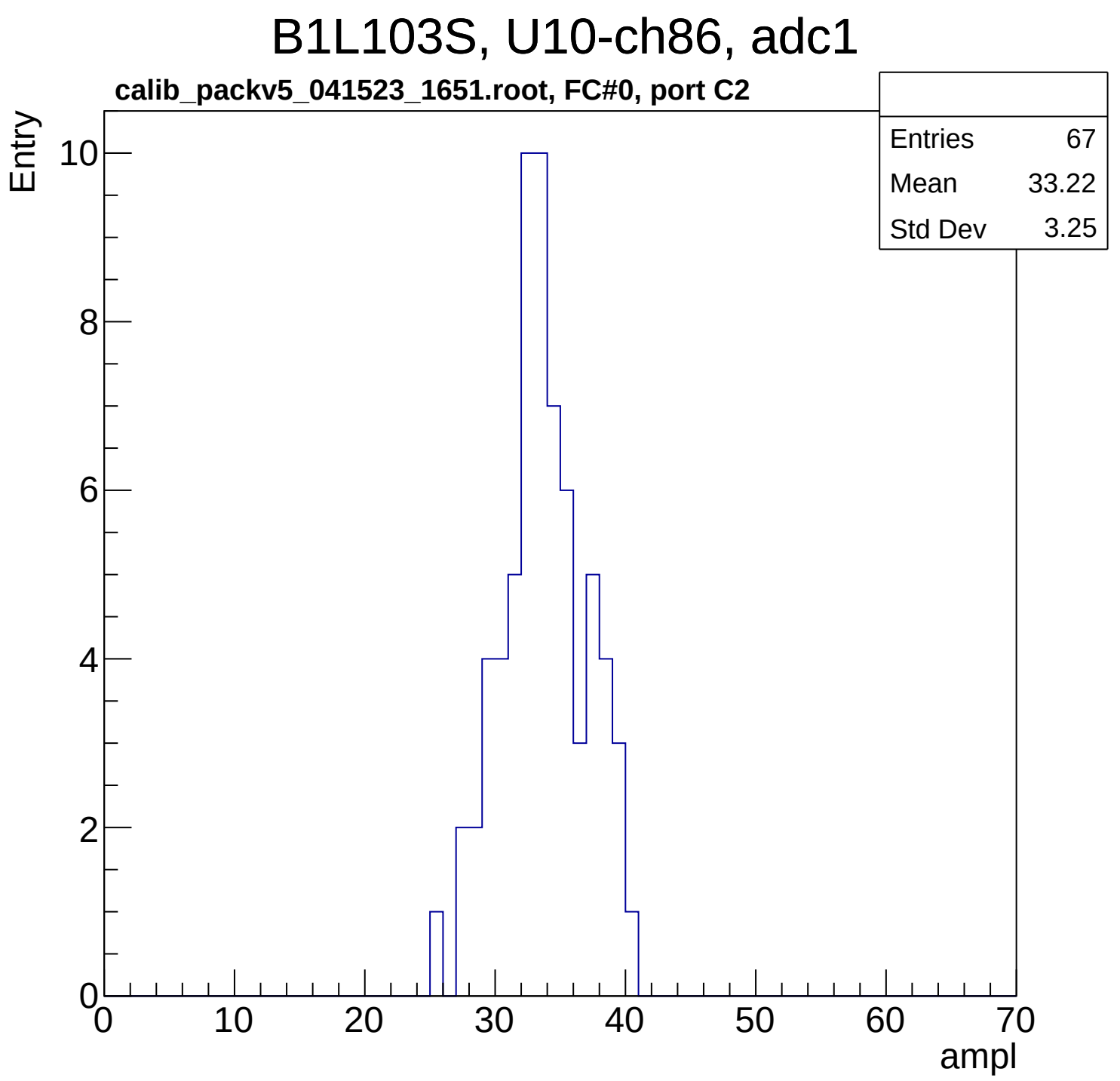
B1L103S, U10-ch86, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 33.22
Std Dev 3.25
Entry
0
2
4
6
8
10
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10
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30
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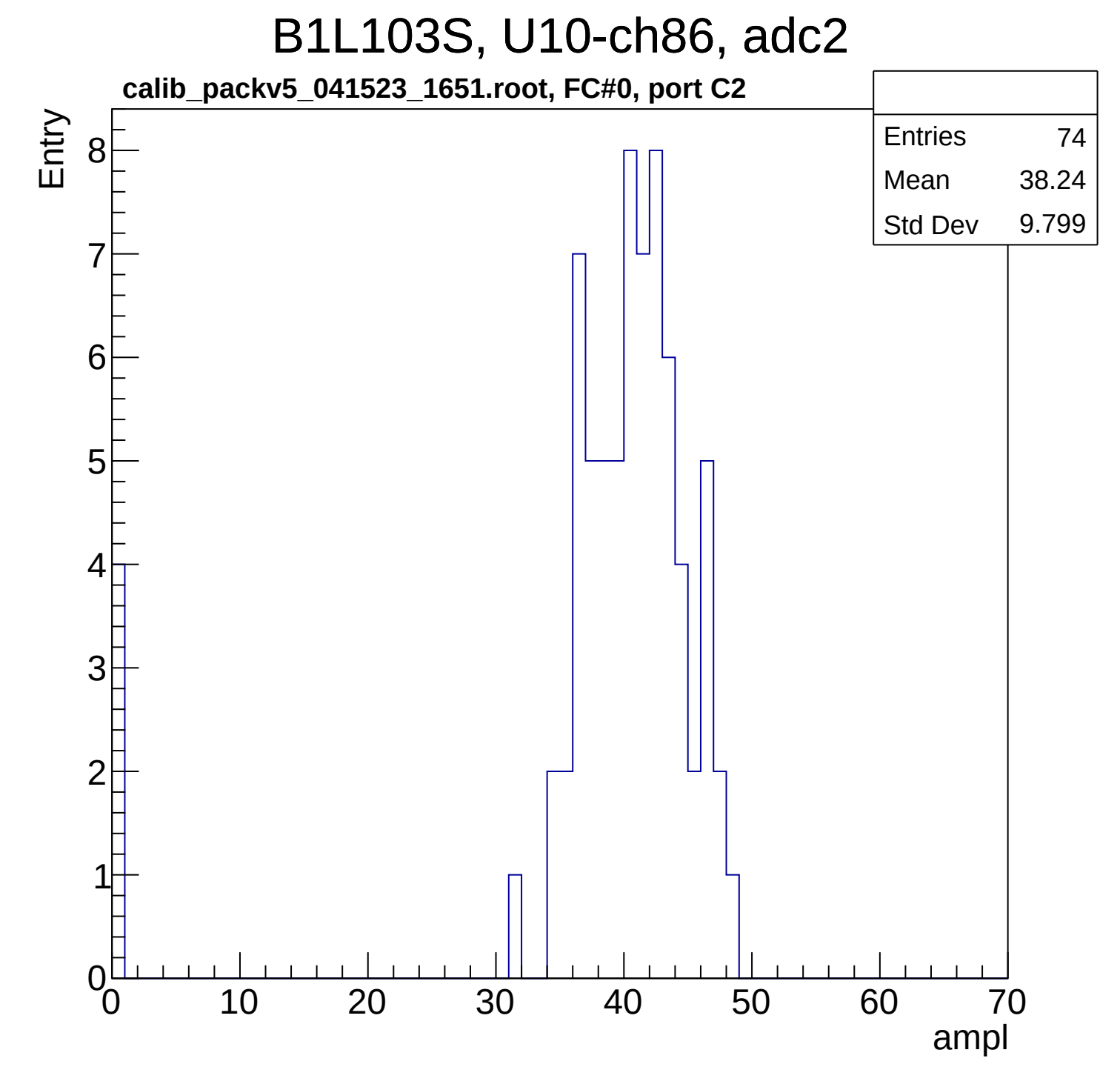
50
60
70
ampl


B1L103S, U10-ch86, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 38.24
Std Dev 9.799
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
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60
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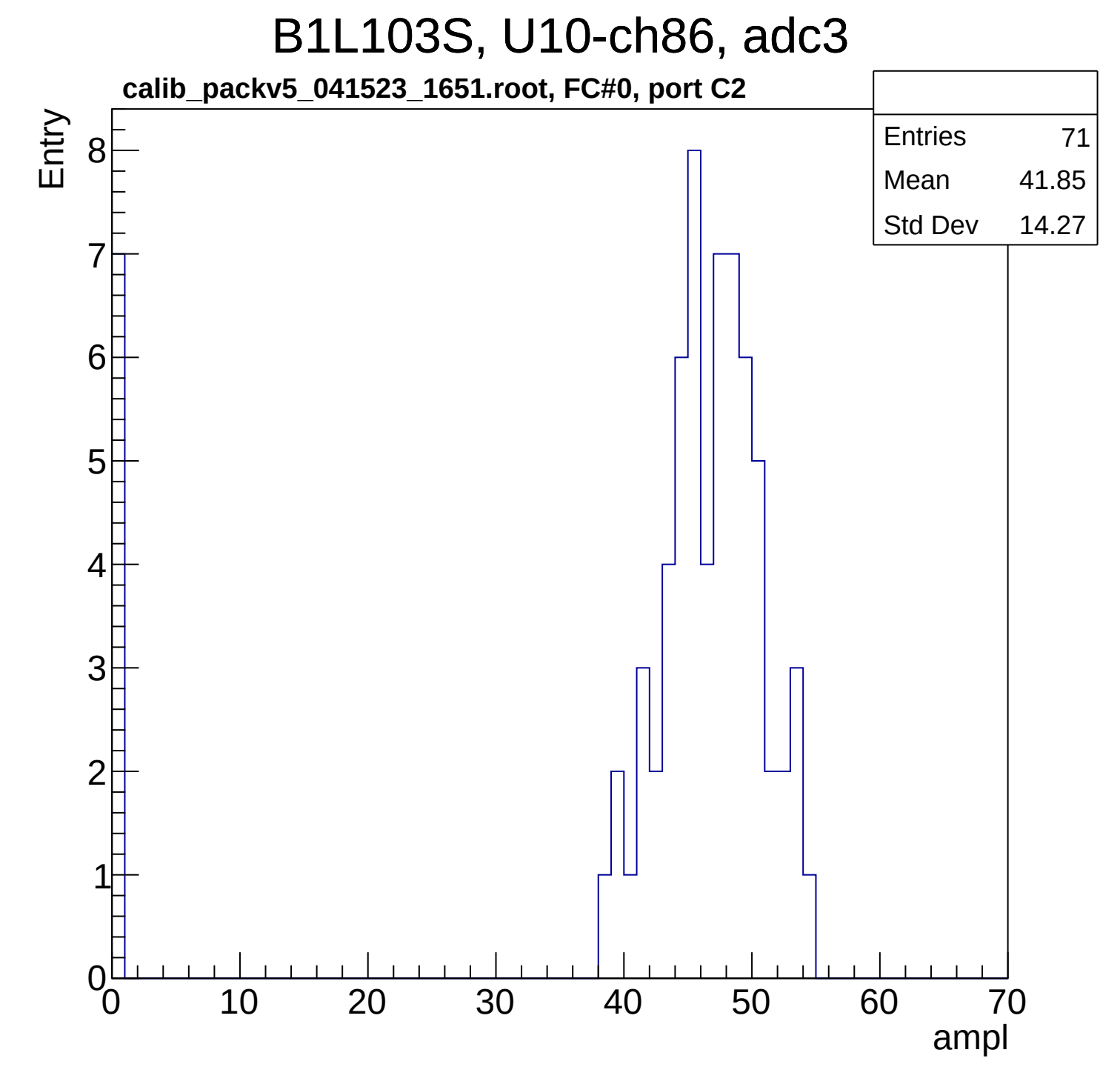
B1L103S, U10-ch86, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 41.85
Std Dev 14.27
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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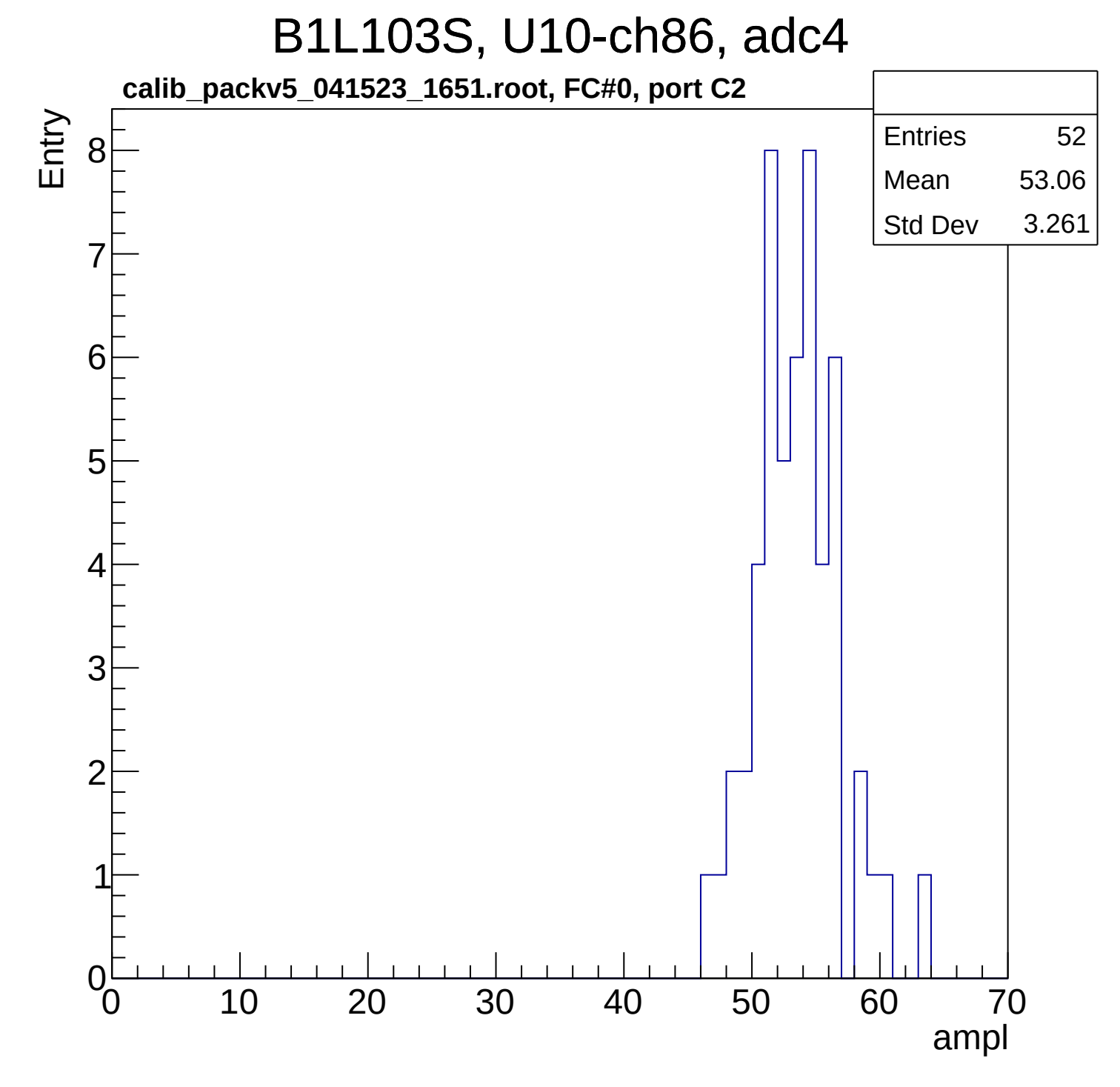
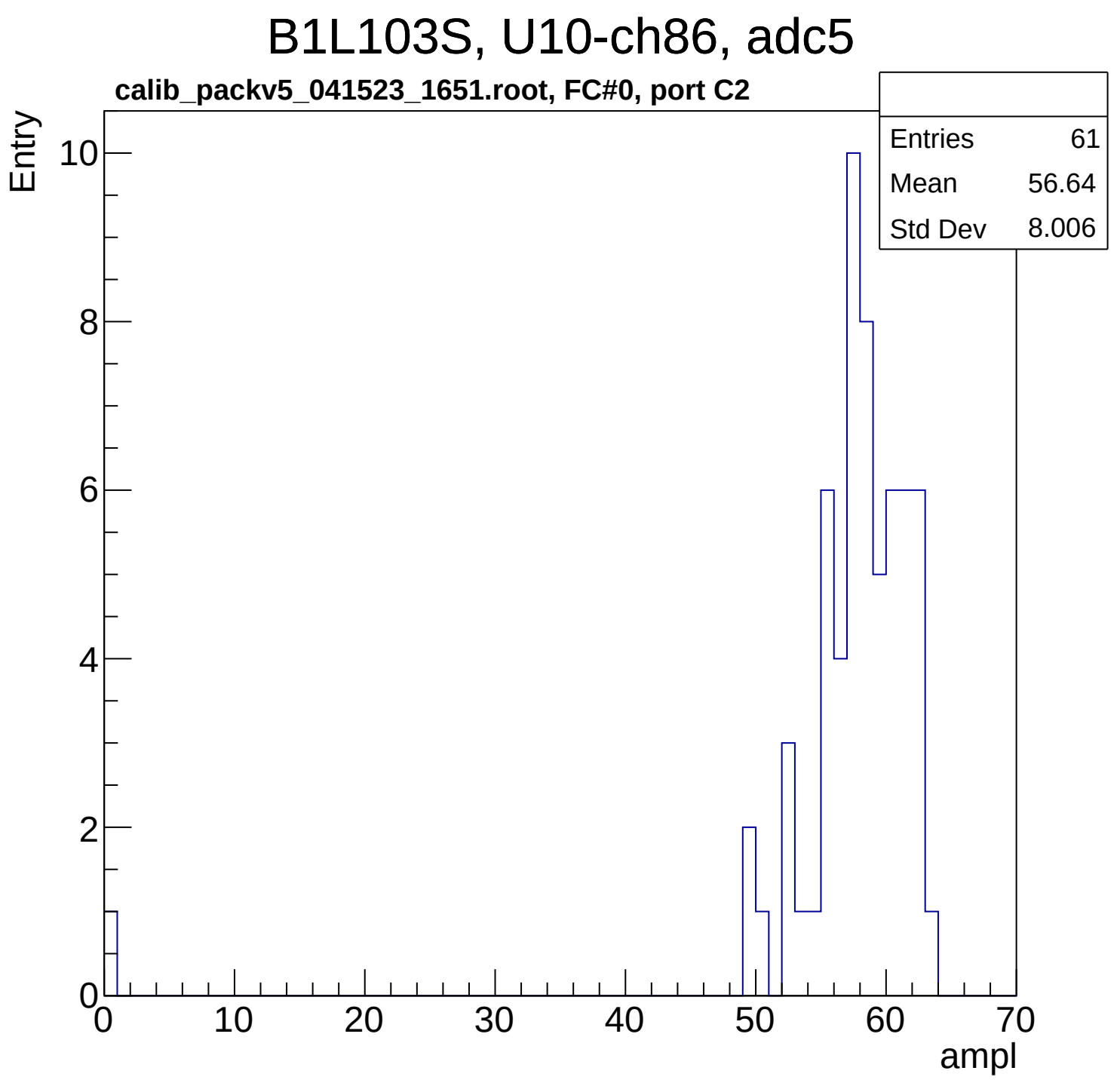
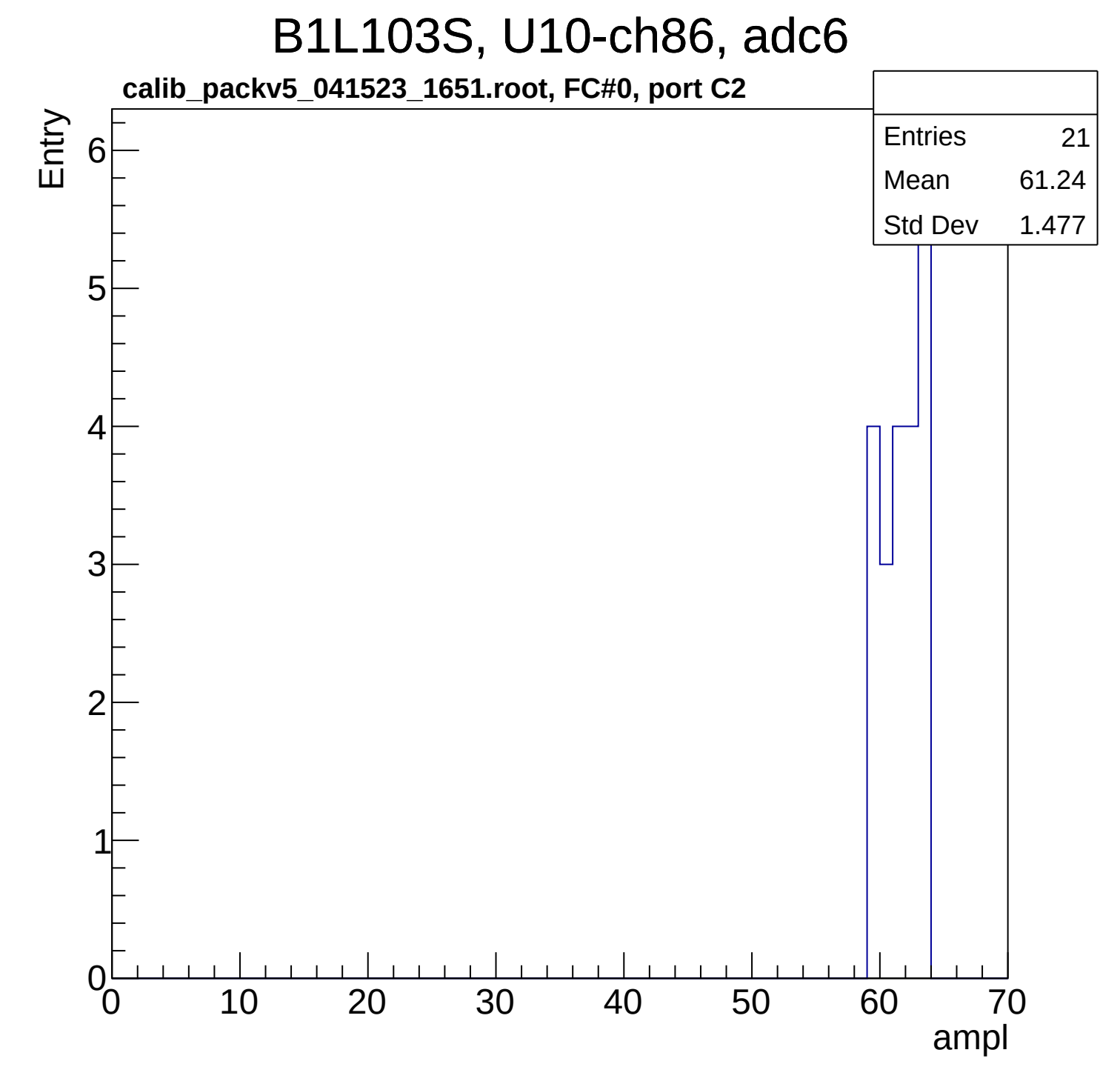
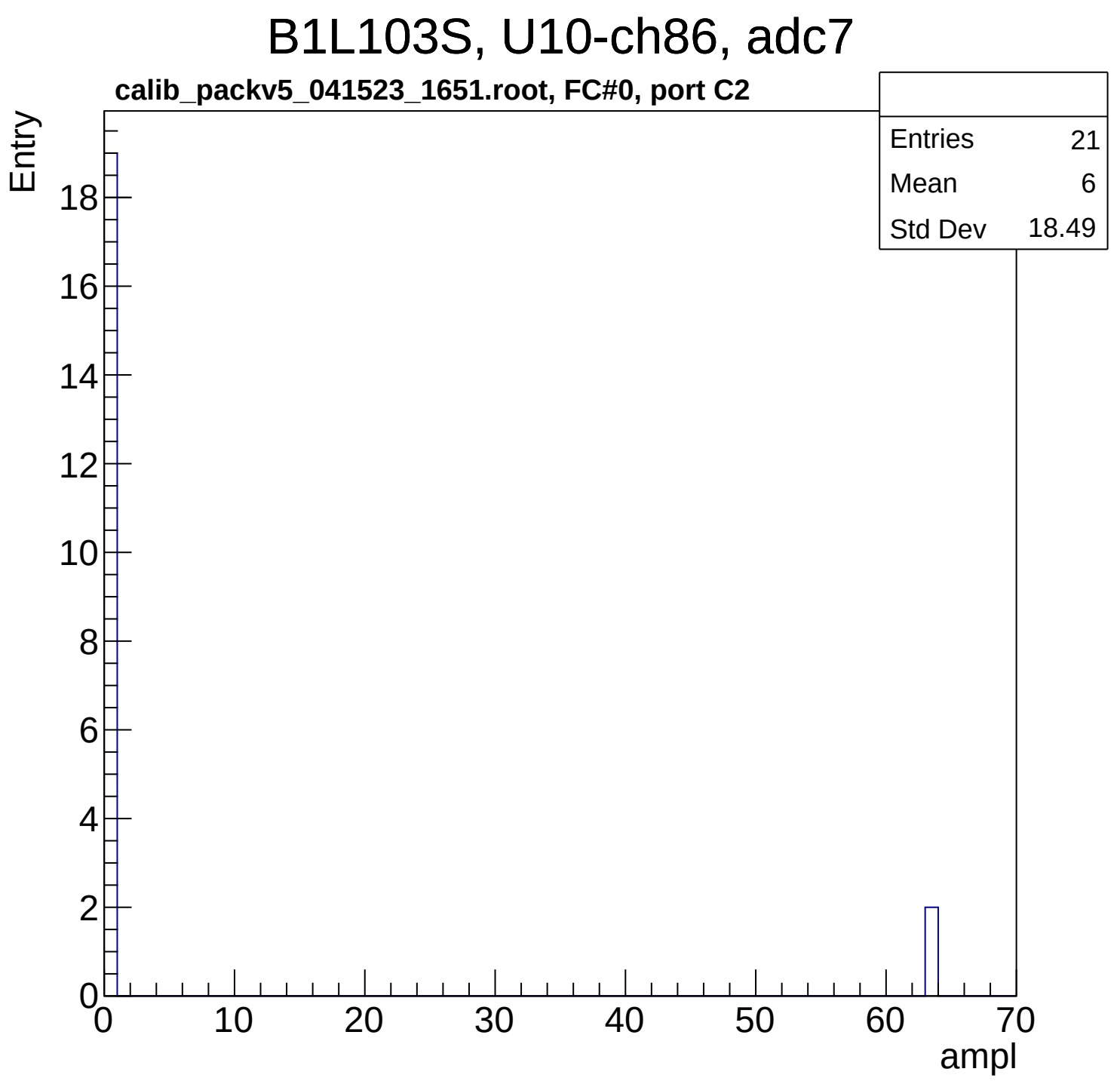

B1L103S, U10-ch86, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 53.06
Std Dev 3.261
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U10-ch86, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 56.64
Std Dev 8.006
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch86, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 61.24
Std Dev 1.477
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch86, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 6
Std Dev 18.49
Entry
0
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4
6
8
10
12
14
16
18
0
10
20
30
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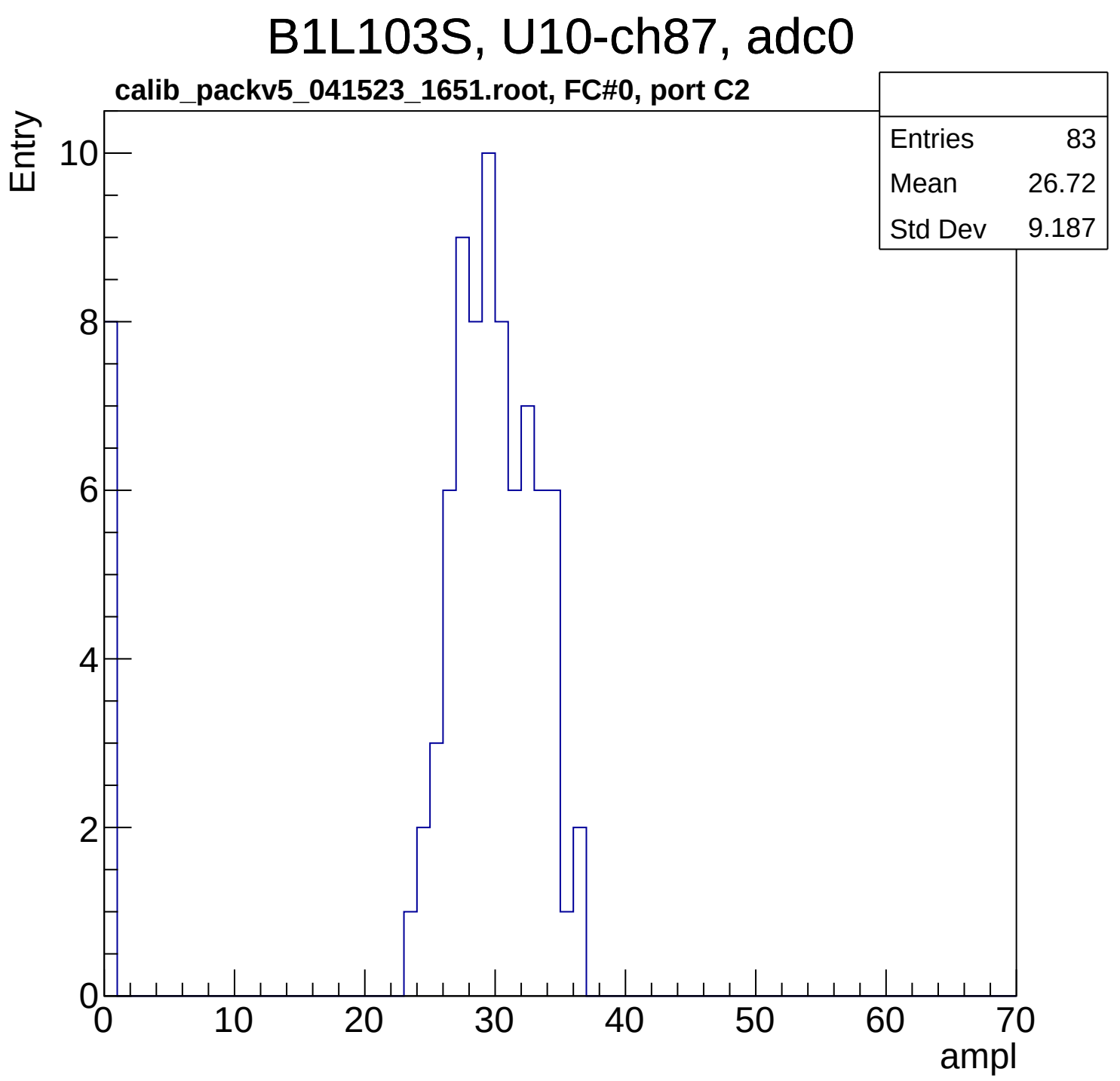
50
60
70
ampl


B1L103S, U10-ch87, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 26.72
Std Dev 9.187
Entry
ampl
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8
10
0
10
20
30
40
50
60
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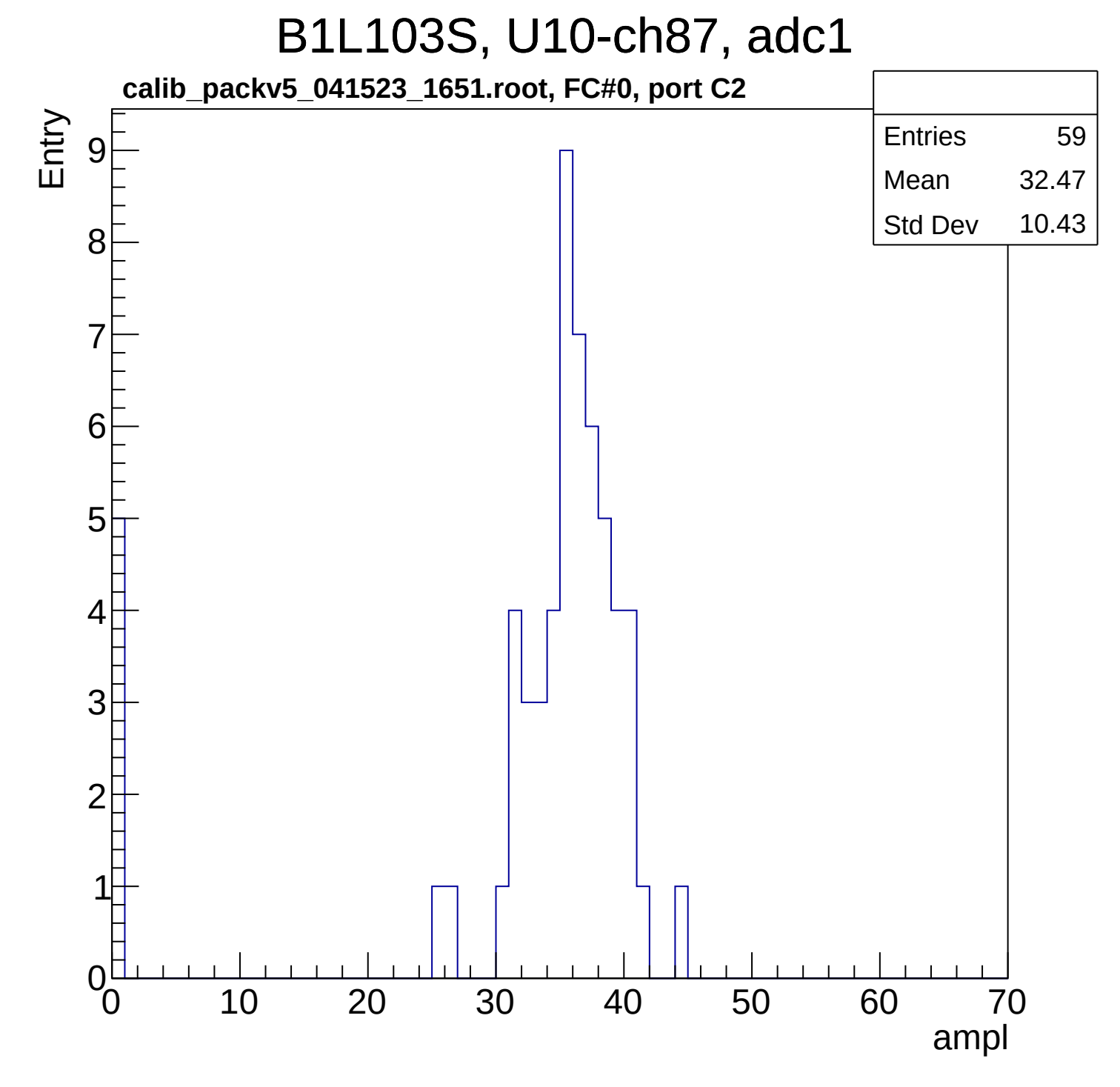
B1L103S, U10-ch87, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 32.47
Std Dev 10.43
Entry
ampl
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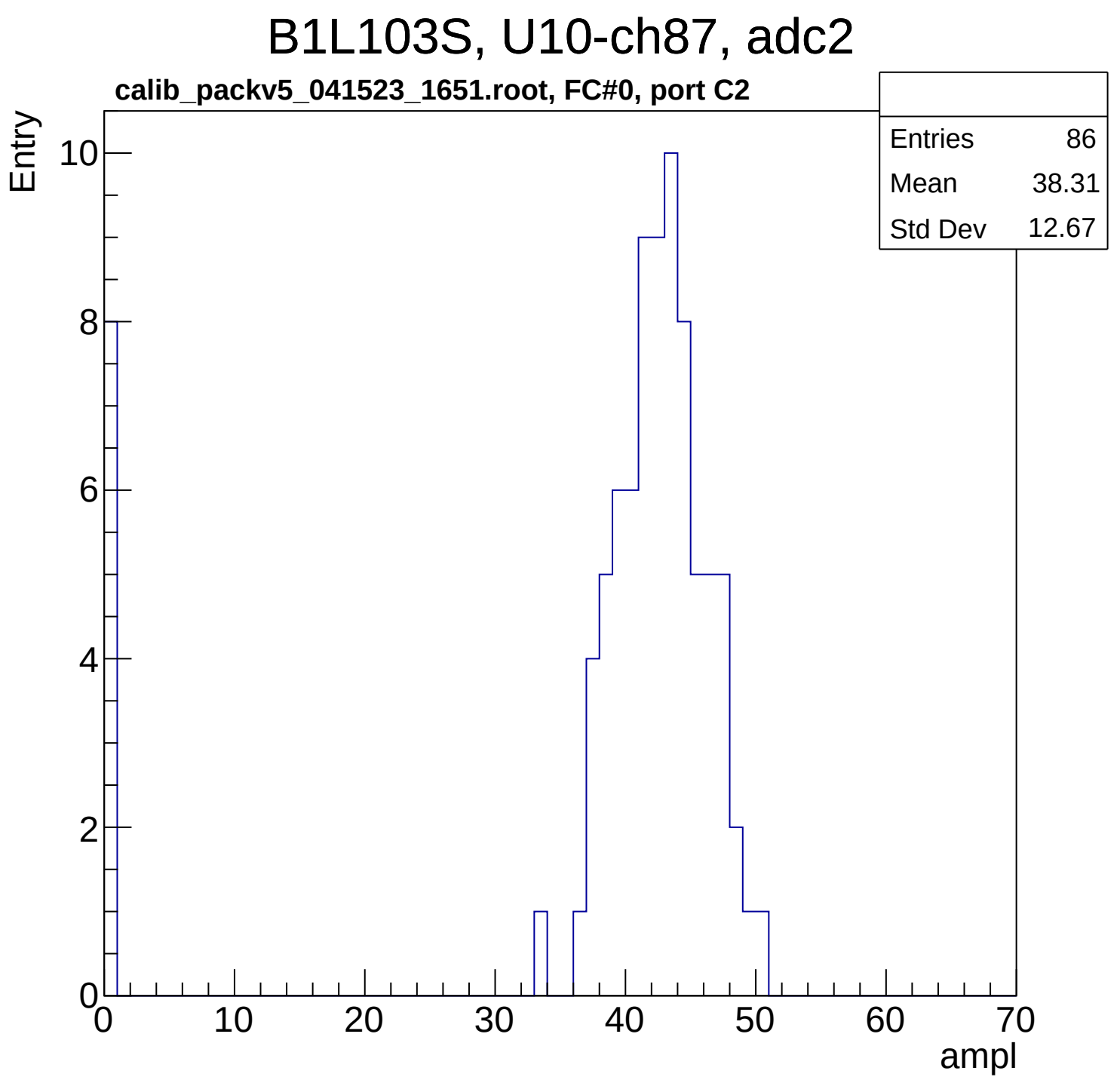
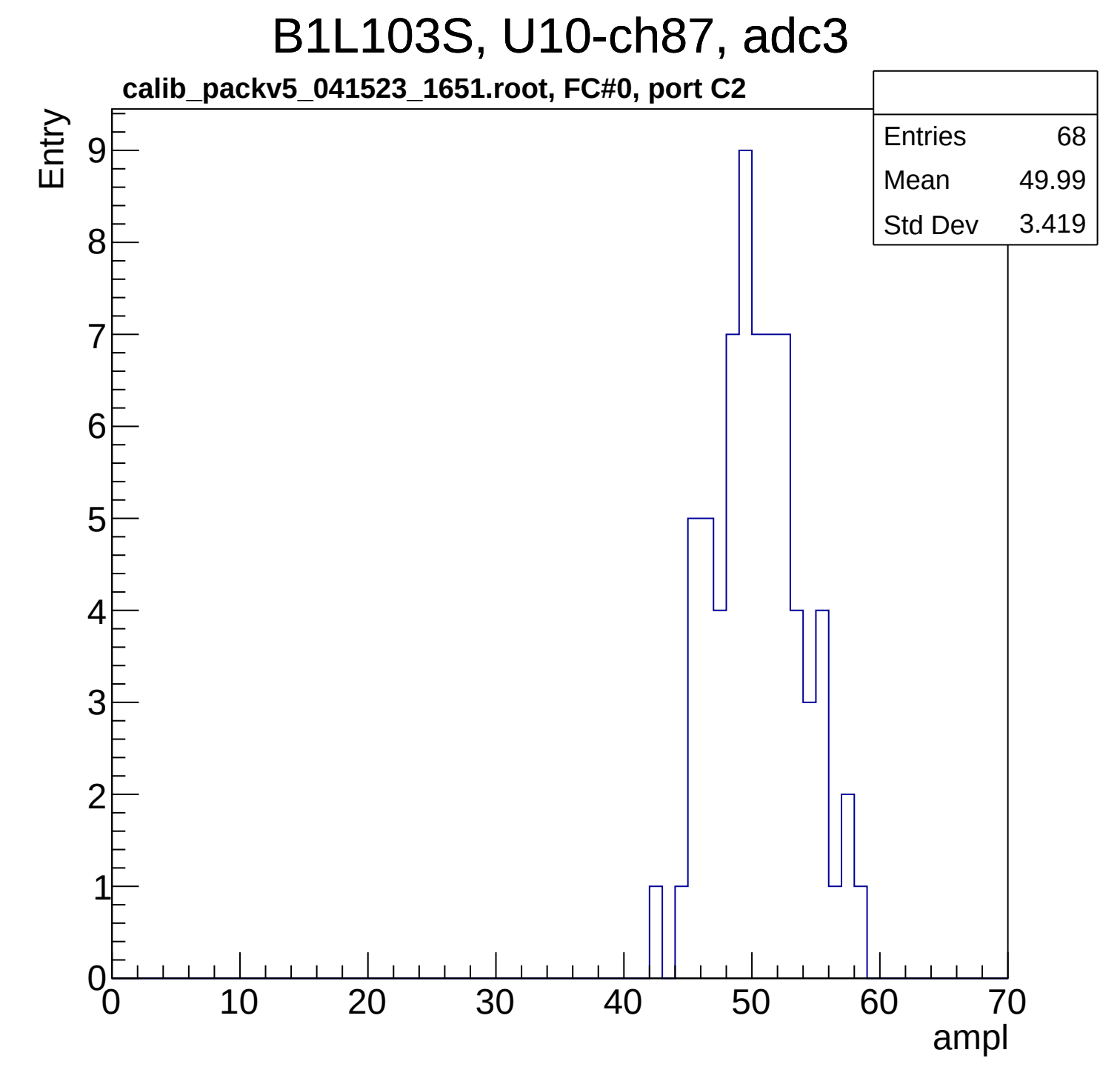
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U10-ch87, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 38.31
Std Dev 12.67
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U10-ch87, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 49.99
Std Dev 3.419
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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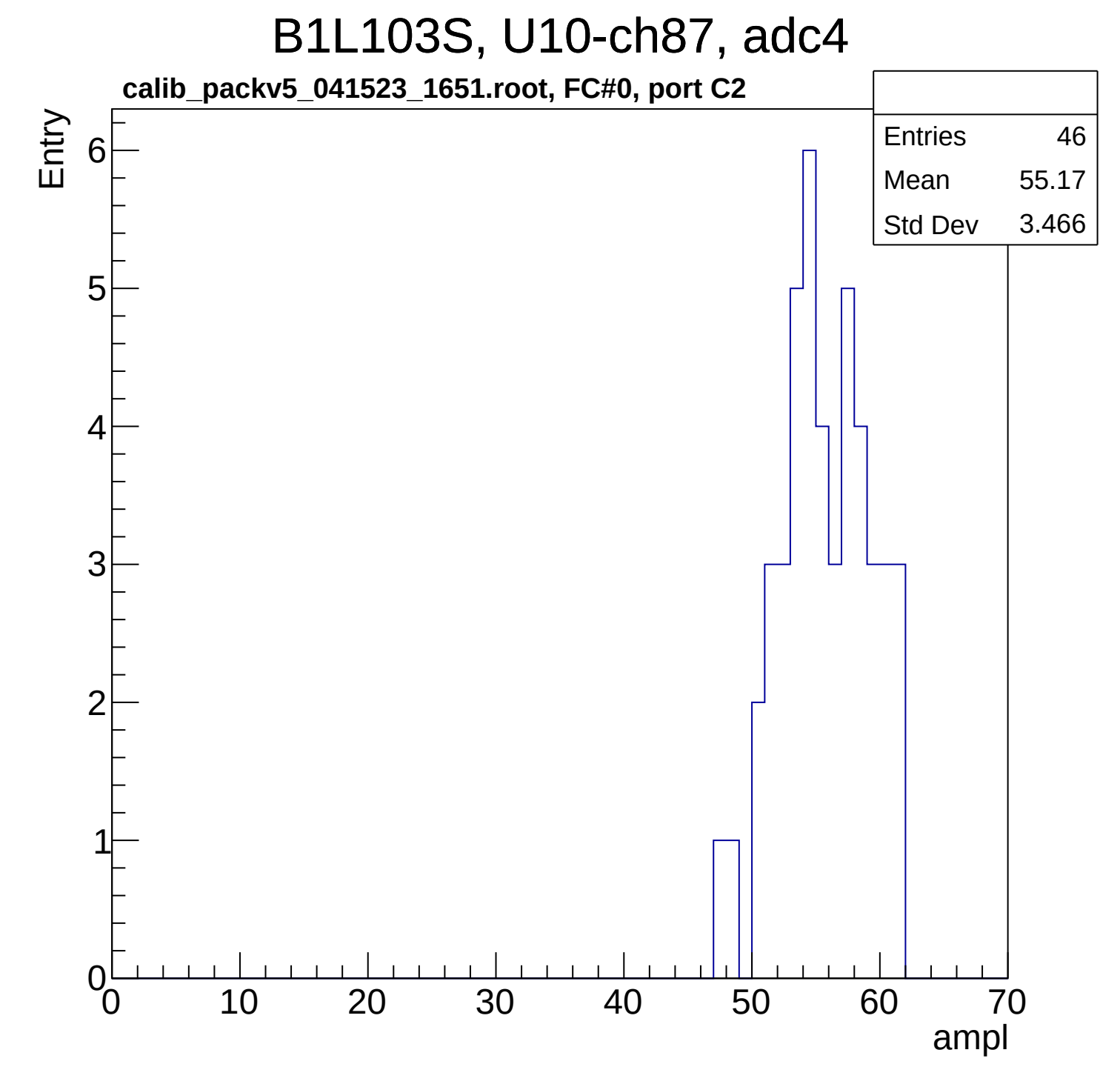
40
50
60
70


B1L103S, U10-ch87, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 55.17
Std Dev 3.466
Entry
ampl
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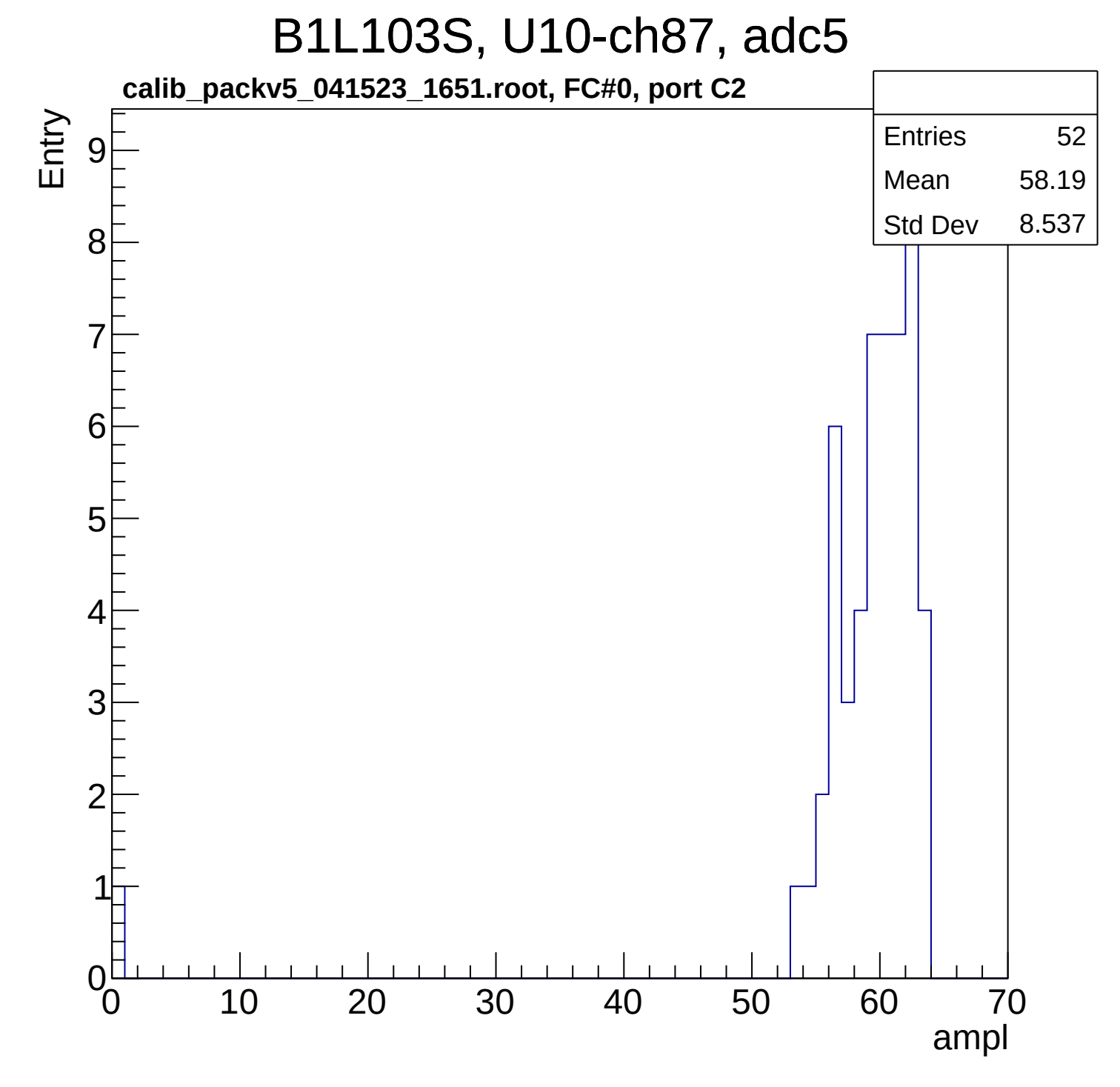
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U10-ch87, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 58.19
Std Dev 8.537
Entry
ampl
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2
3
4
5
6
7
8
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0
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60
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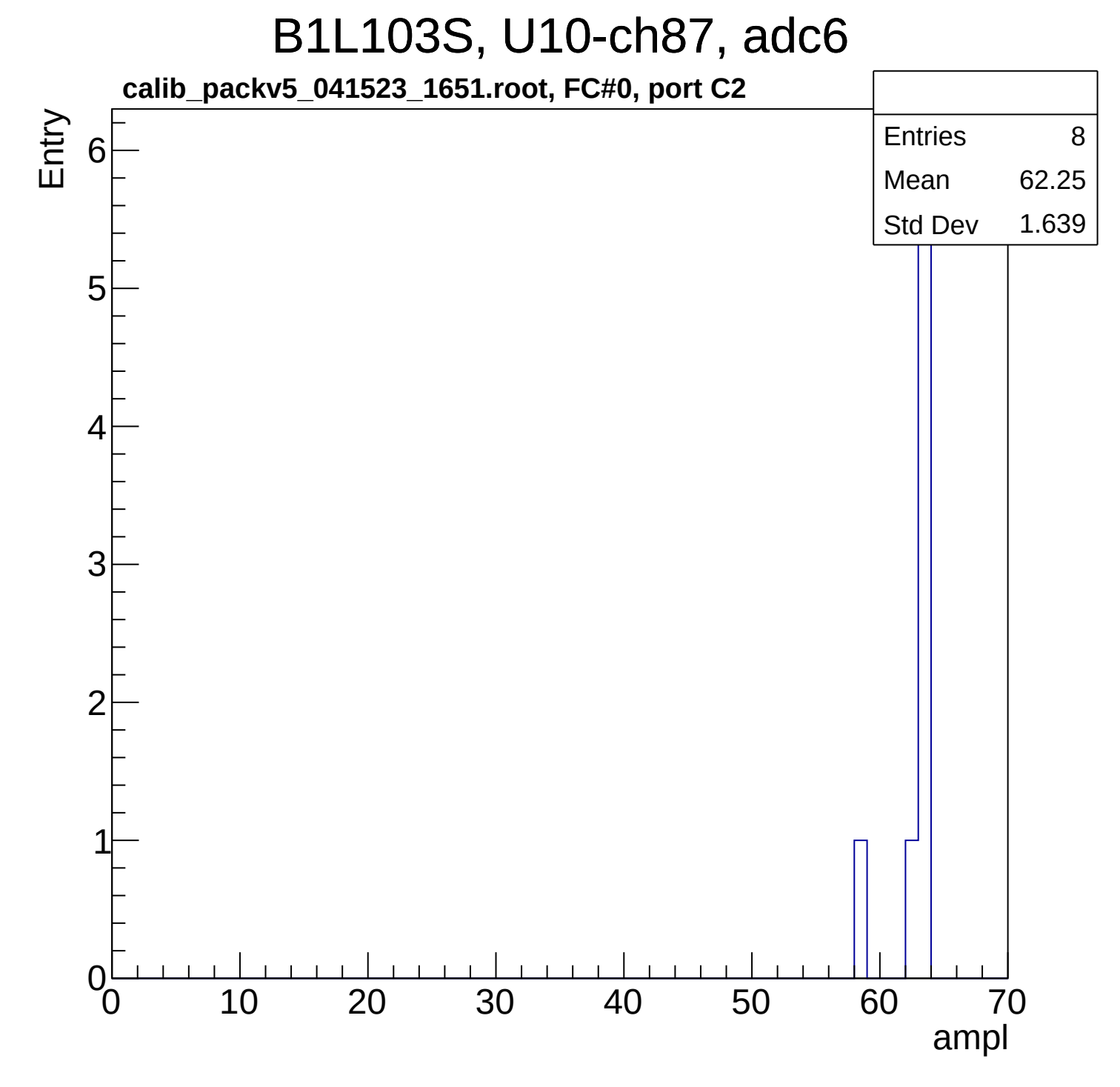
B1L103S, U10-ch87, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 62.25
Std Dev 1.639
Entry
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2
3
4
5
6
0
10
20
30
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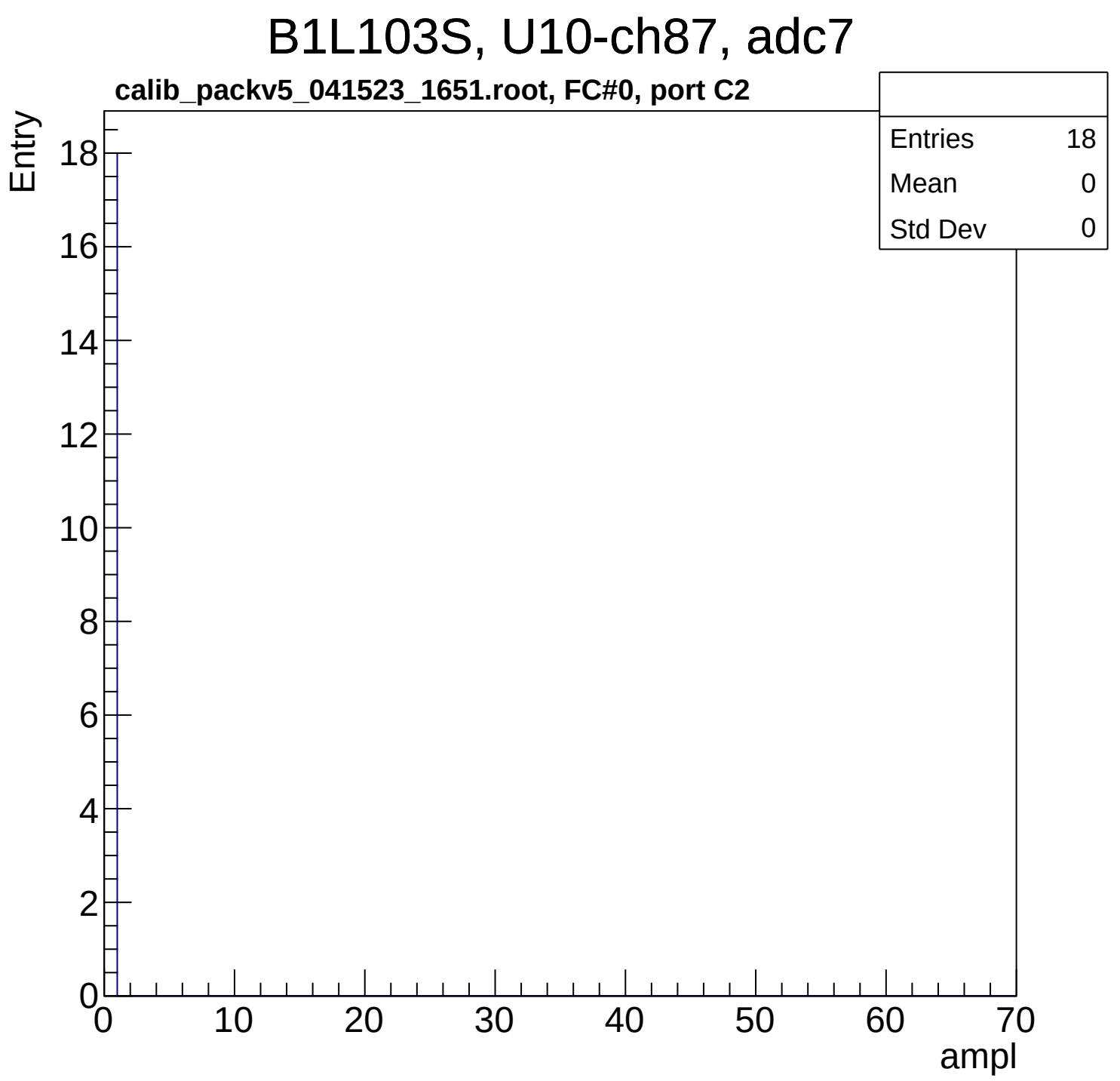
50
60
70
ampl


B1L103S, U10-ch87, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
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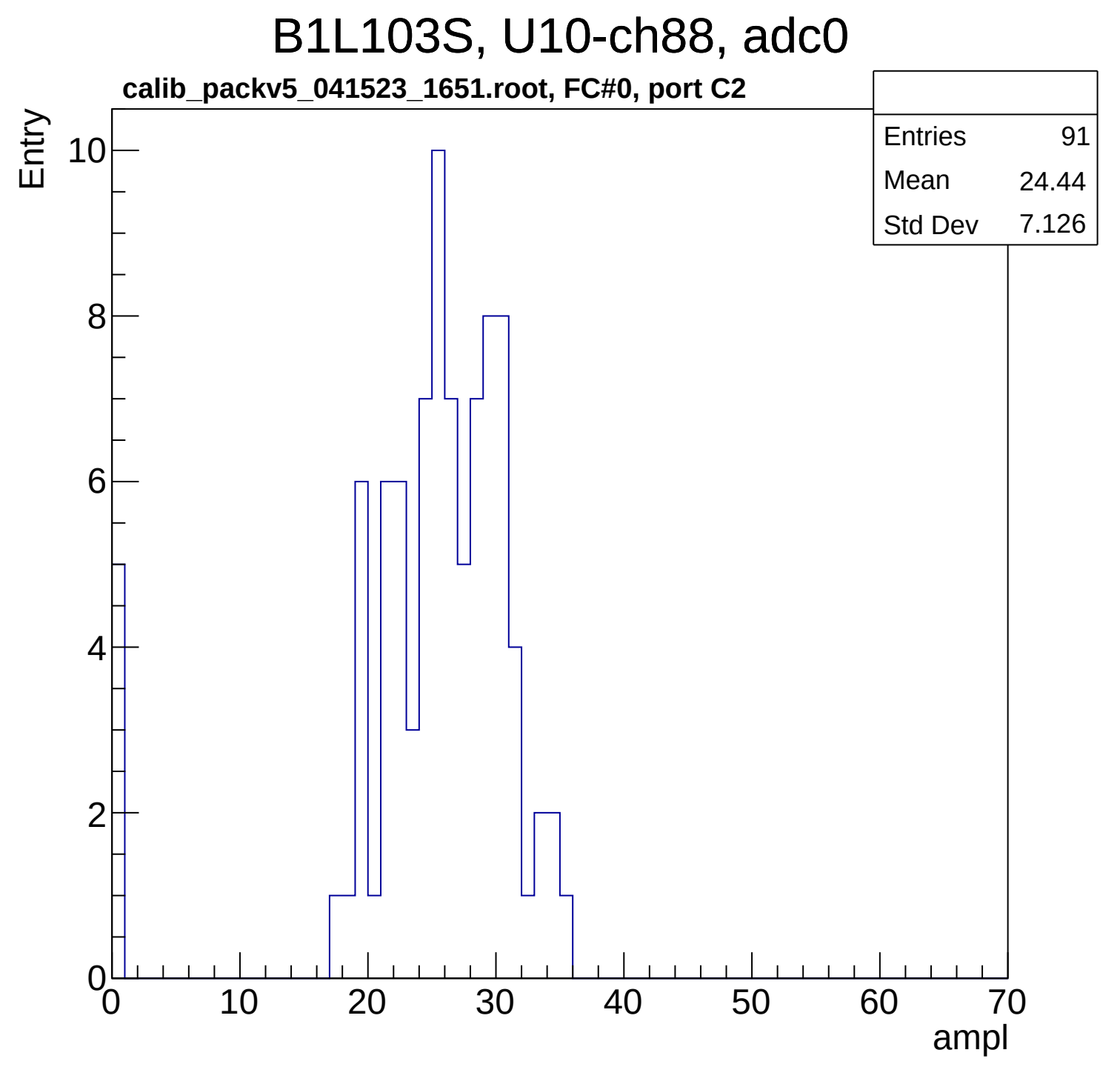
50
60
70
ampl


B1L103S, U10-ch88, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 91
Mean 24.44
Std Dev 7.126
Entry
ampl
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2
4
6
8
10
0
10
20
30
40
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60
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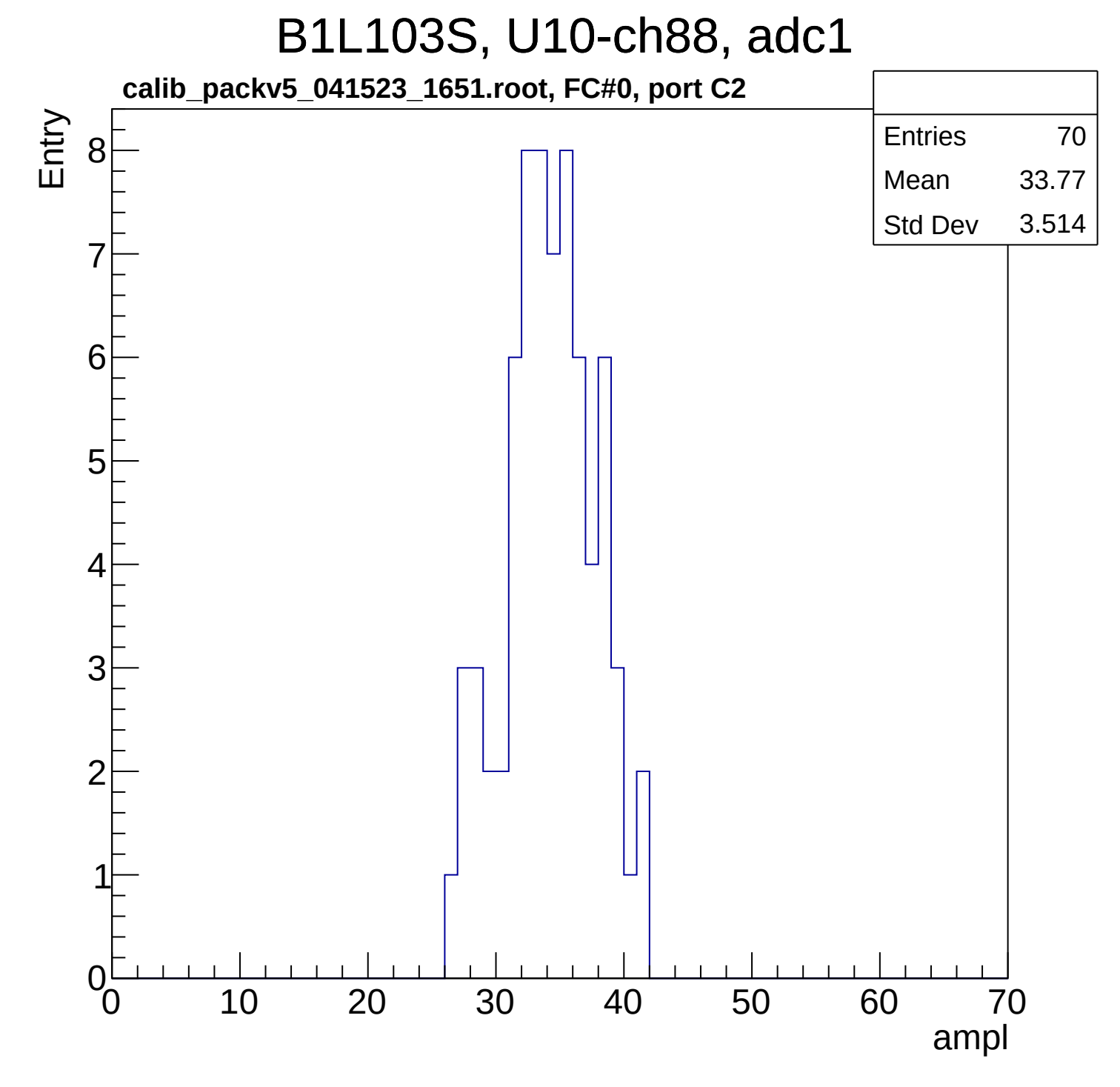
B1L103S, U10-ch88, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 33.77
Std Dev 3.514
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
30
40
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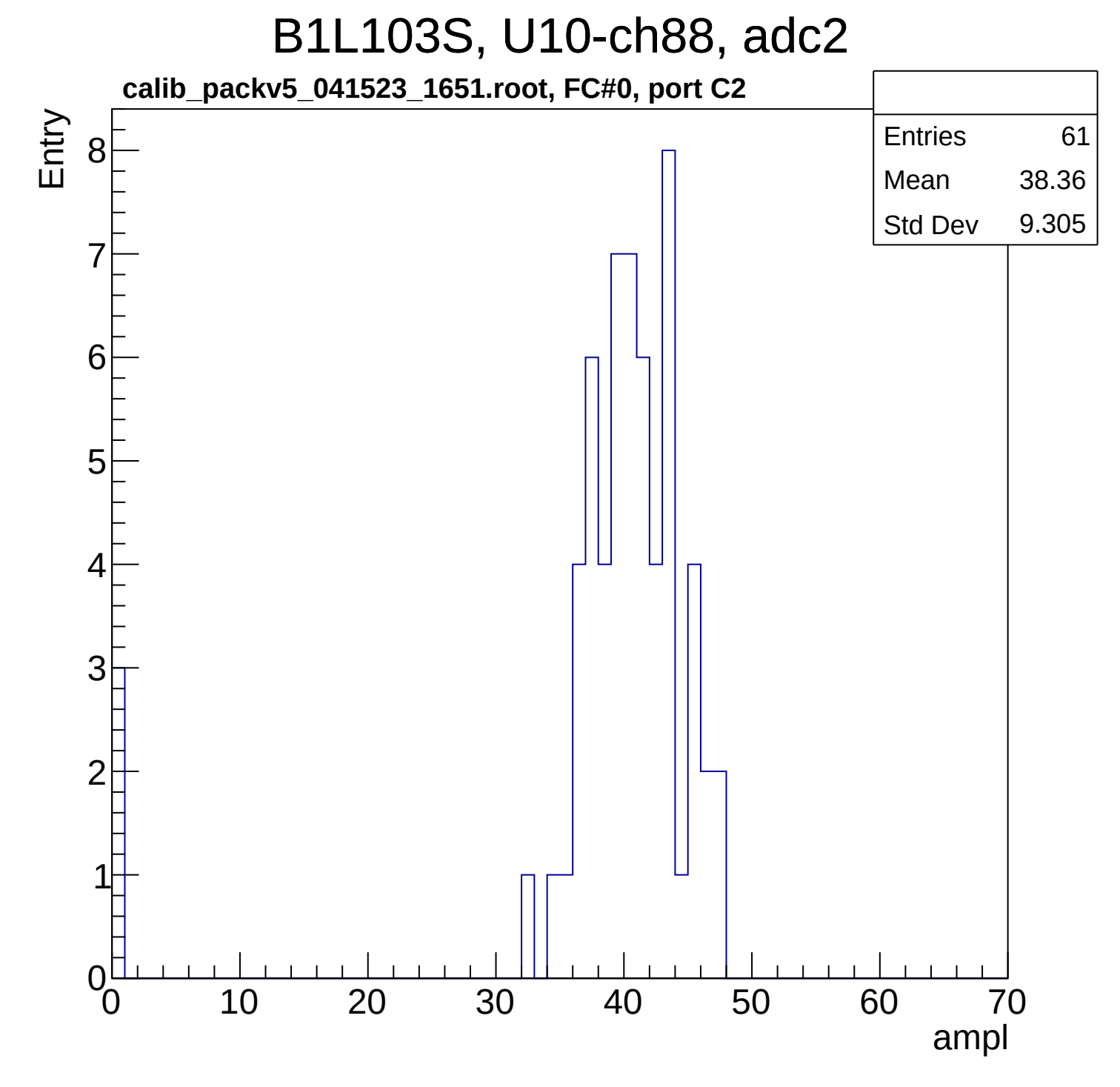
60
70


B1L103S, U10-ch88, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 38.36
Std Dev 9.305
Entry
ampl
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1
2
3
4
5
6
7
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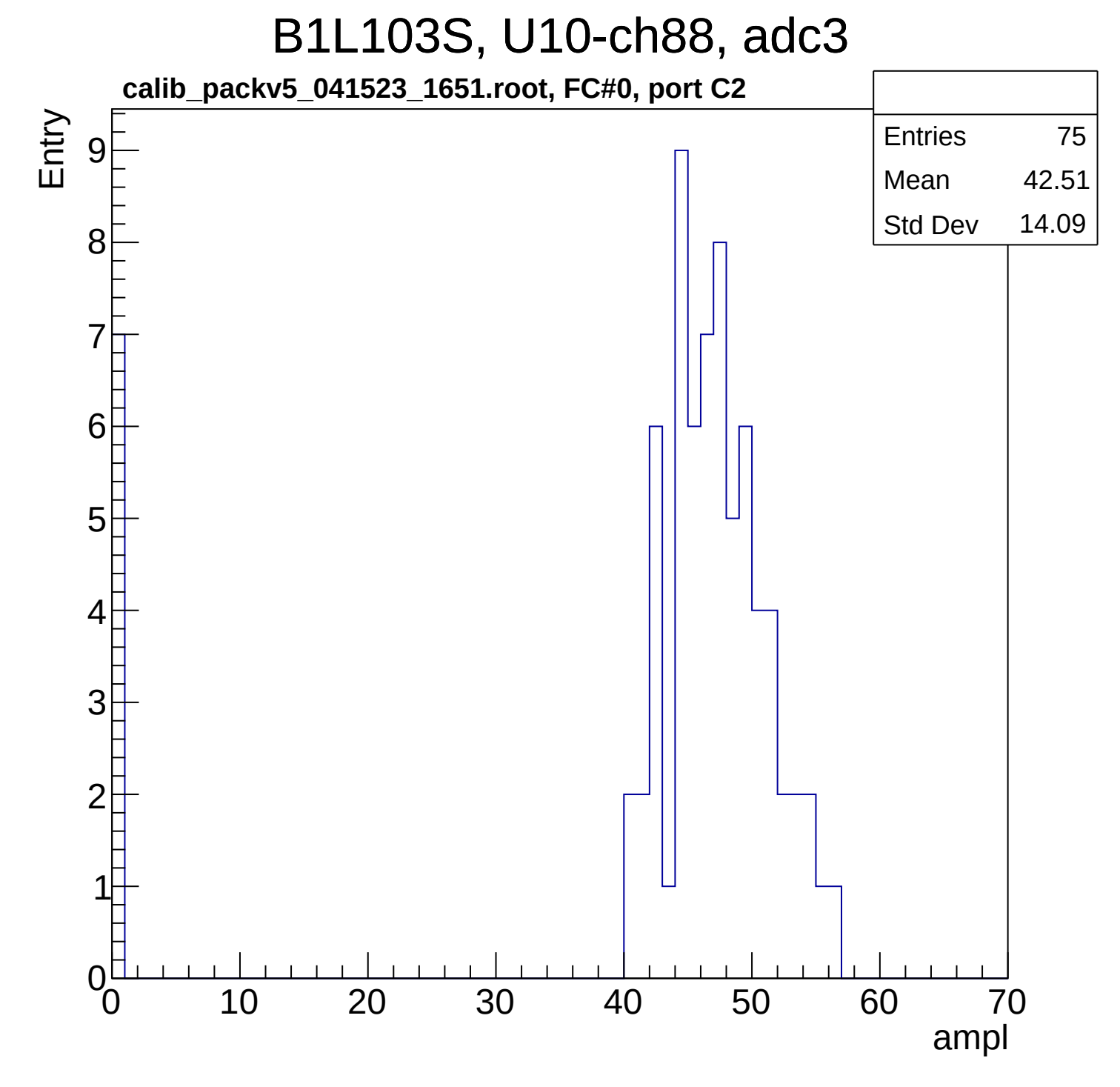
B1L103S, U10-ch88, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 42.51
Std Dev 14.09
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
50
60
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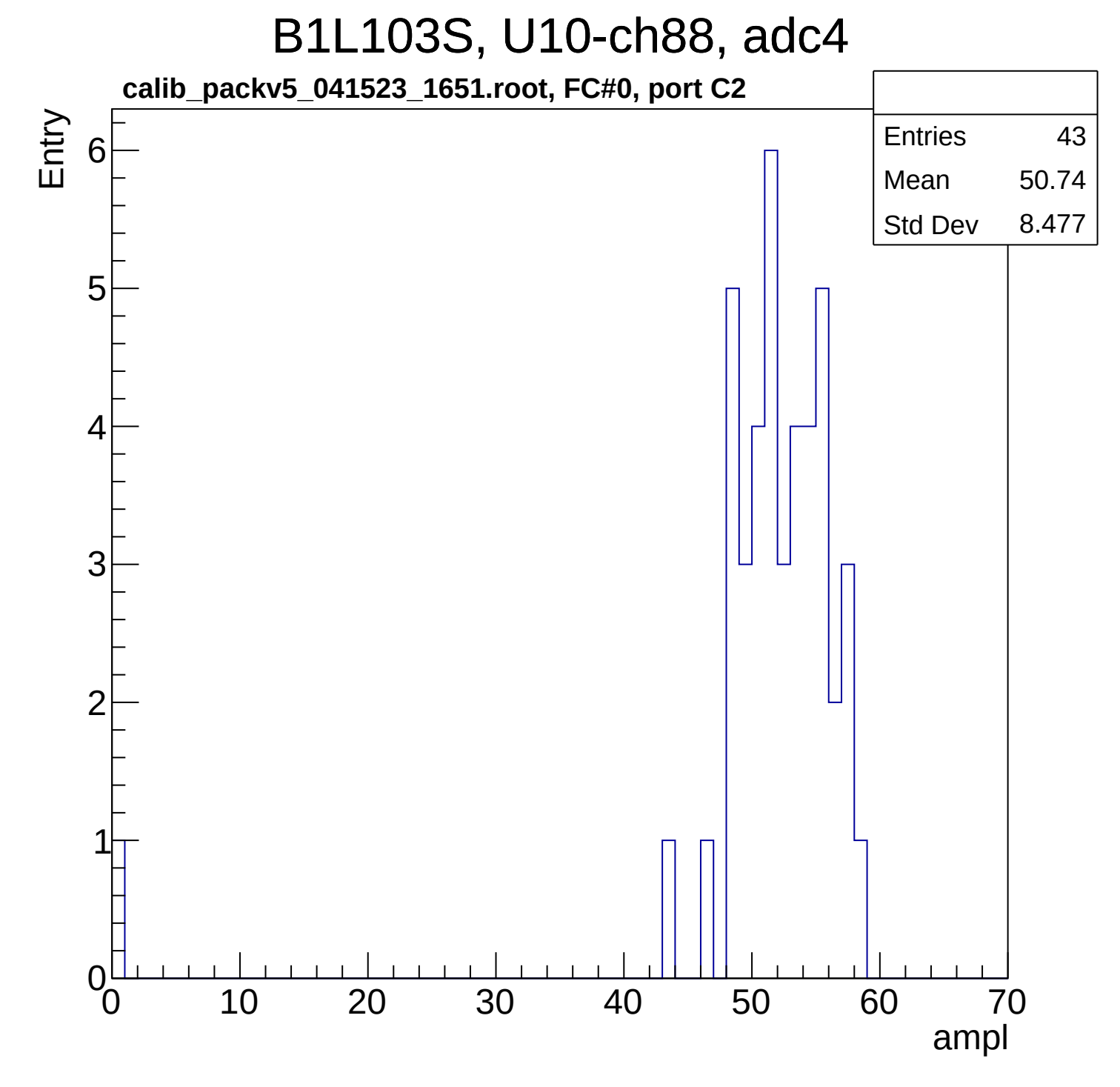
B1L103S, U10-ch88, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 43
Mean 50.74
Std Dev 8.477
Entry
ampl
0
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2
3
4
5
6
0
10
20
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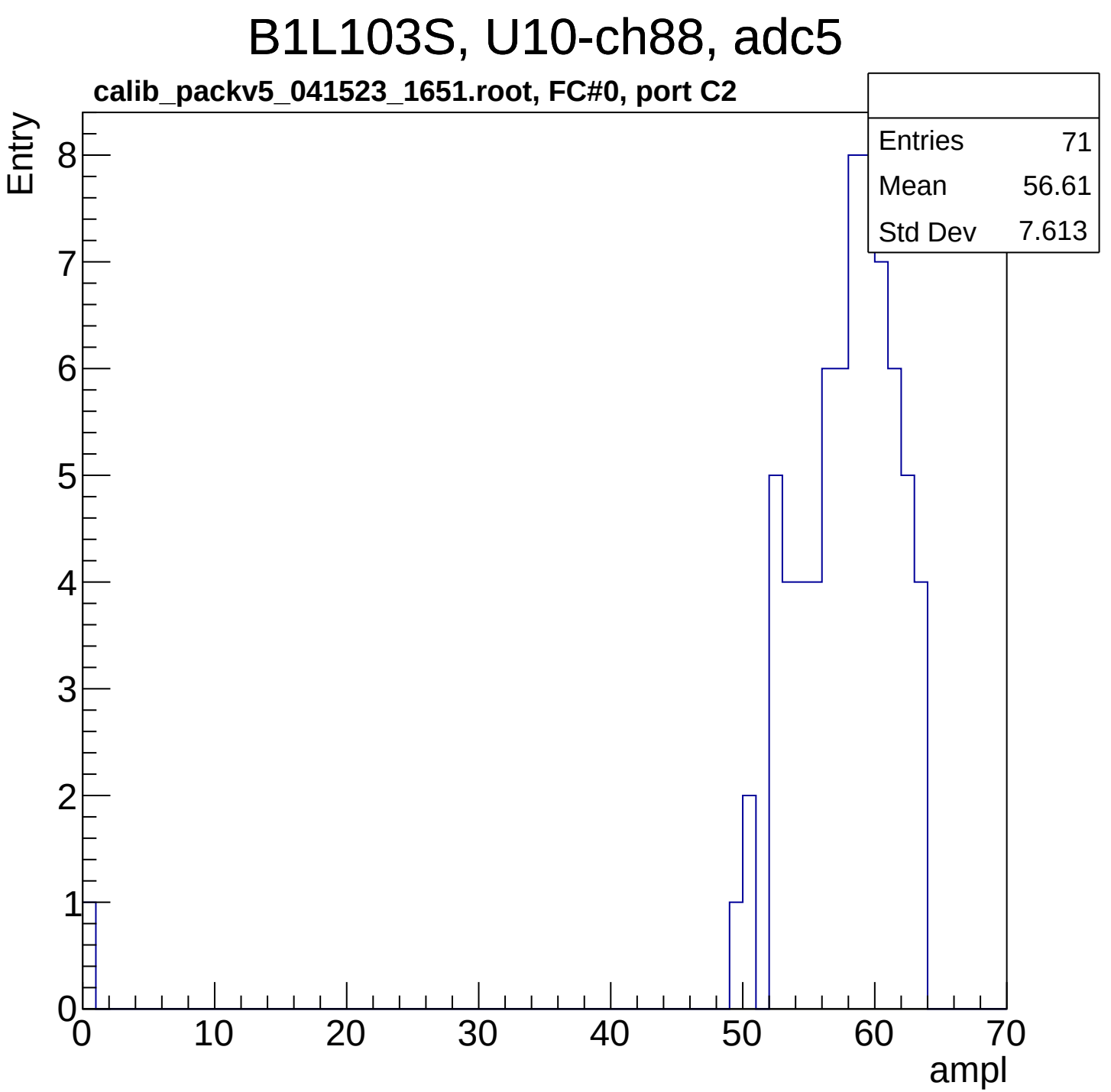
40
50
60
70


B1L103S, U10-ch88, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 56.61
Std Dev 7.613
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
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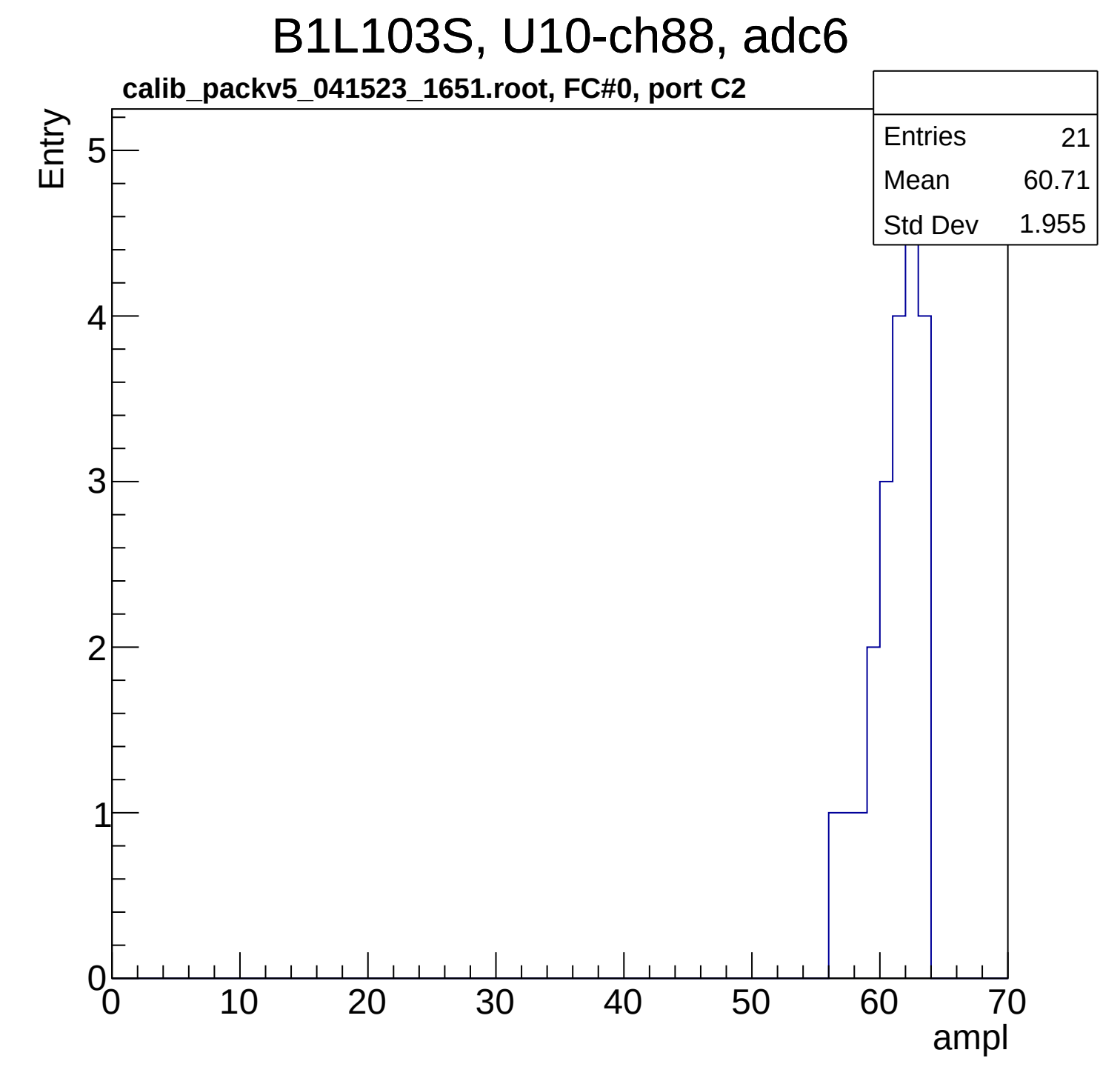
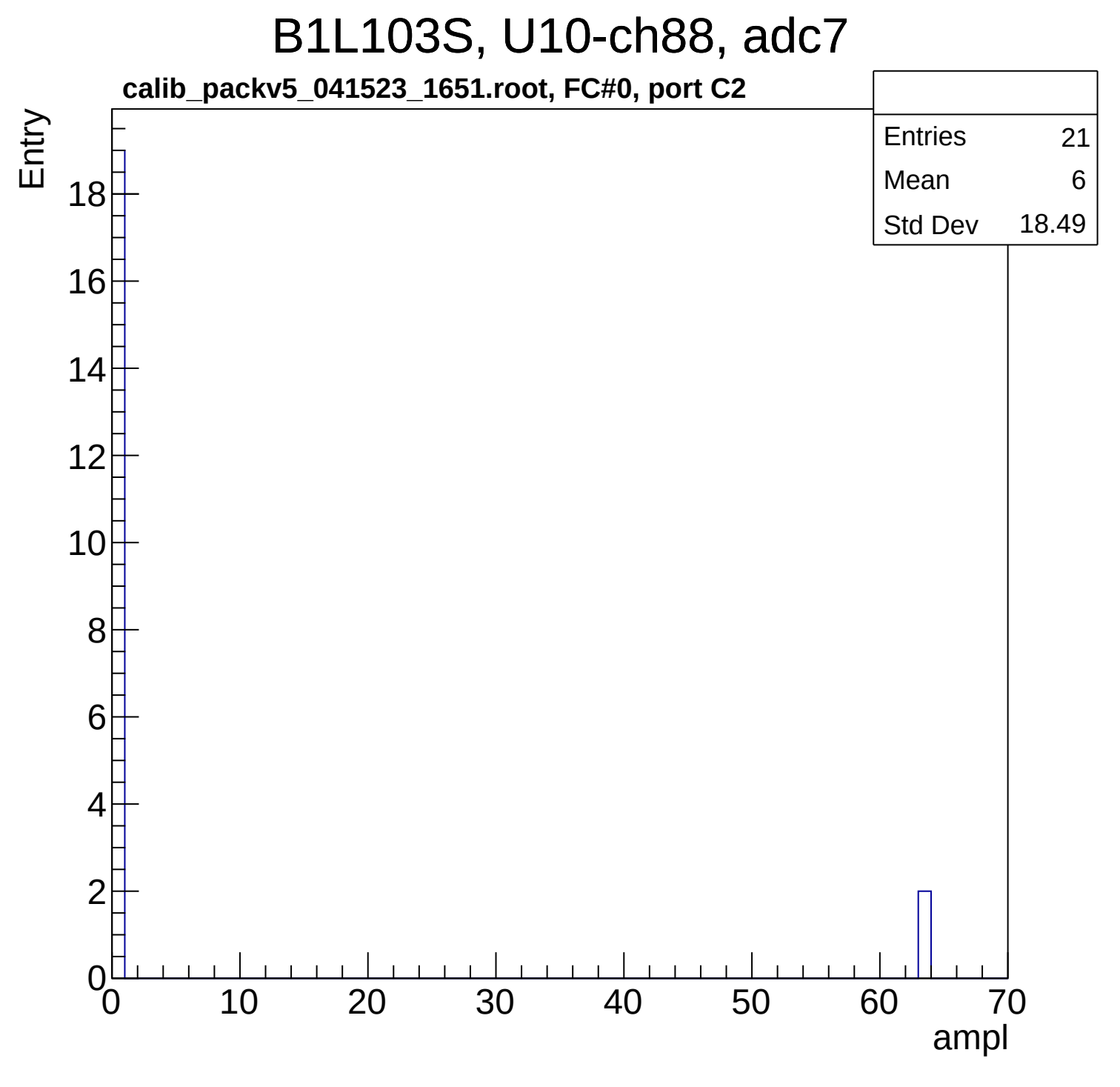
40
50
60
70


B1L103S, U10-ch88, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 60.71
Std Dev 1.955
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch88, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 6
Std Dev 18.49
Entry
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6
8
10
12
14
16
18
0
10
20
30
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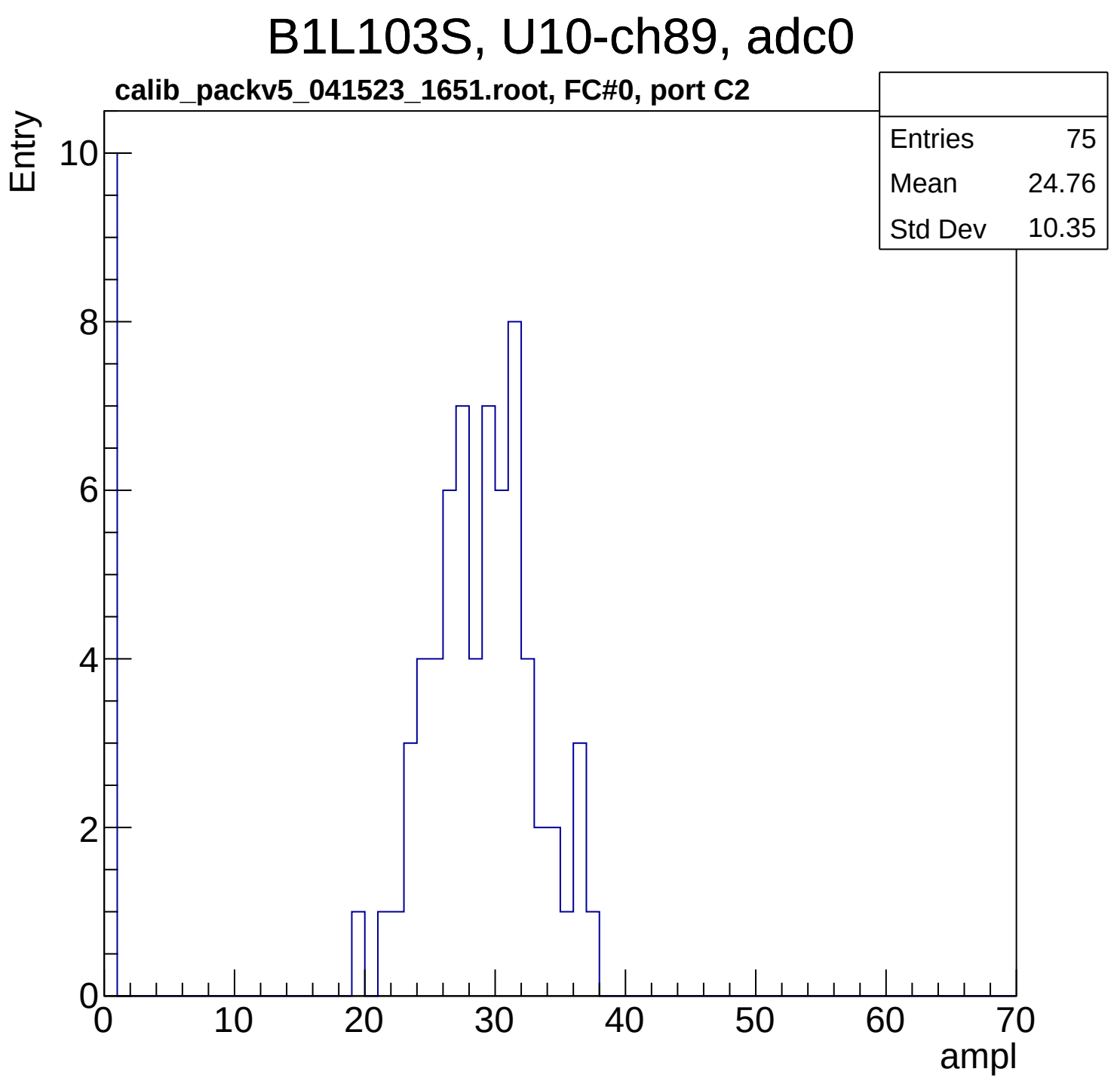
50
60
70
ampl


B1L103S, U10-ch89, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 24.76
Std Dev 10.35
Entry
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10
20
30
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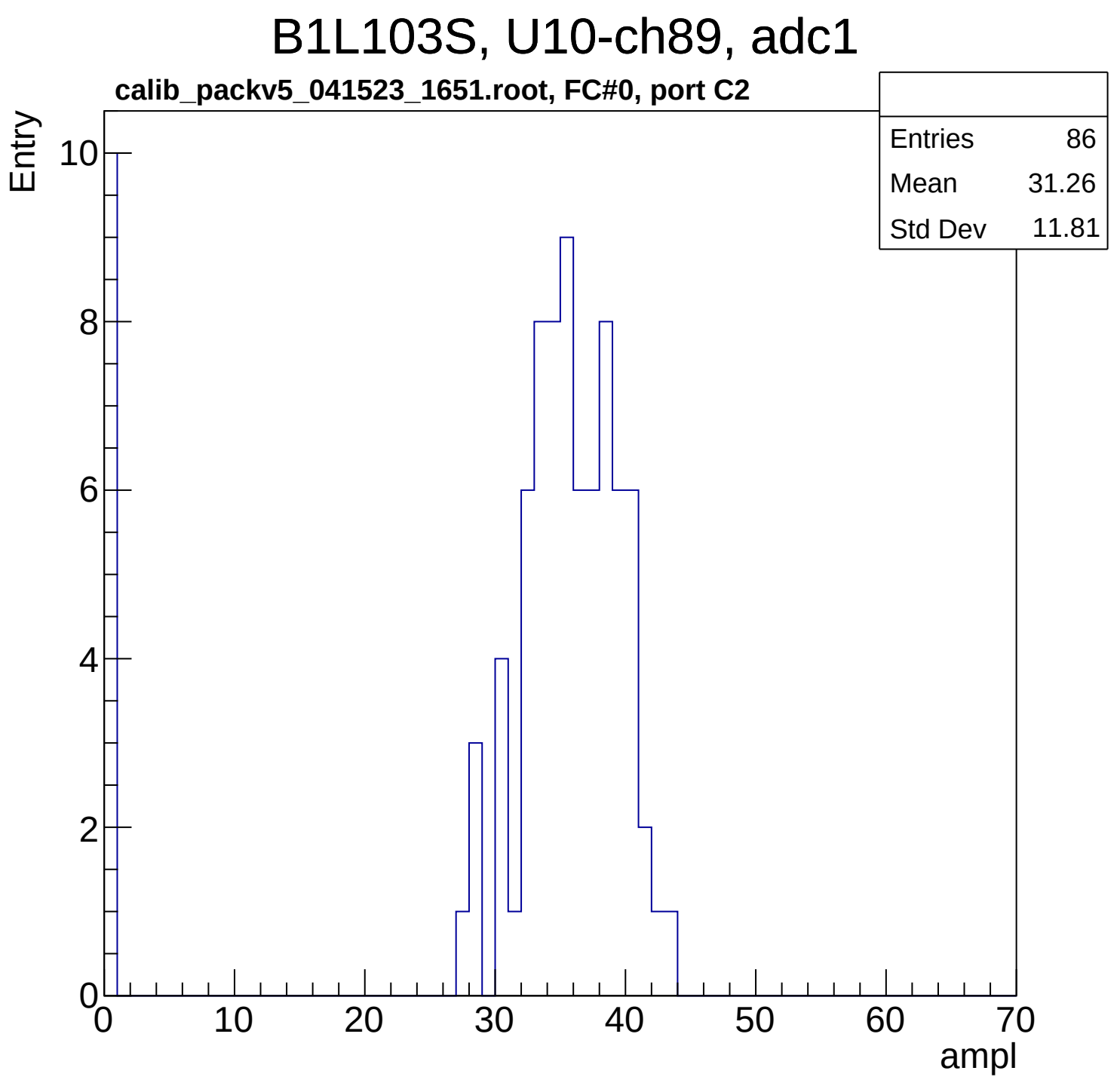
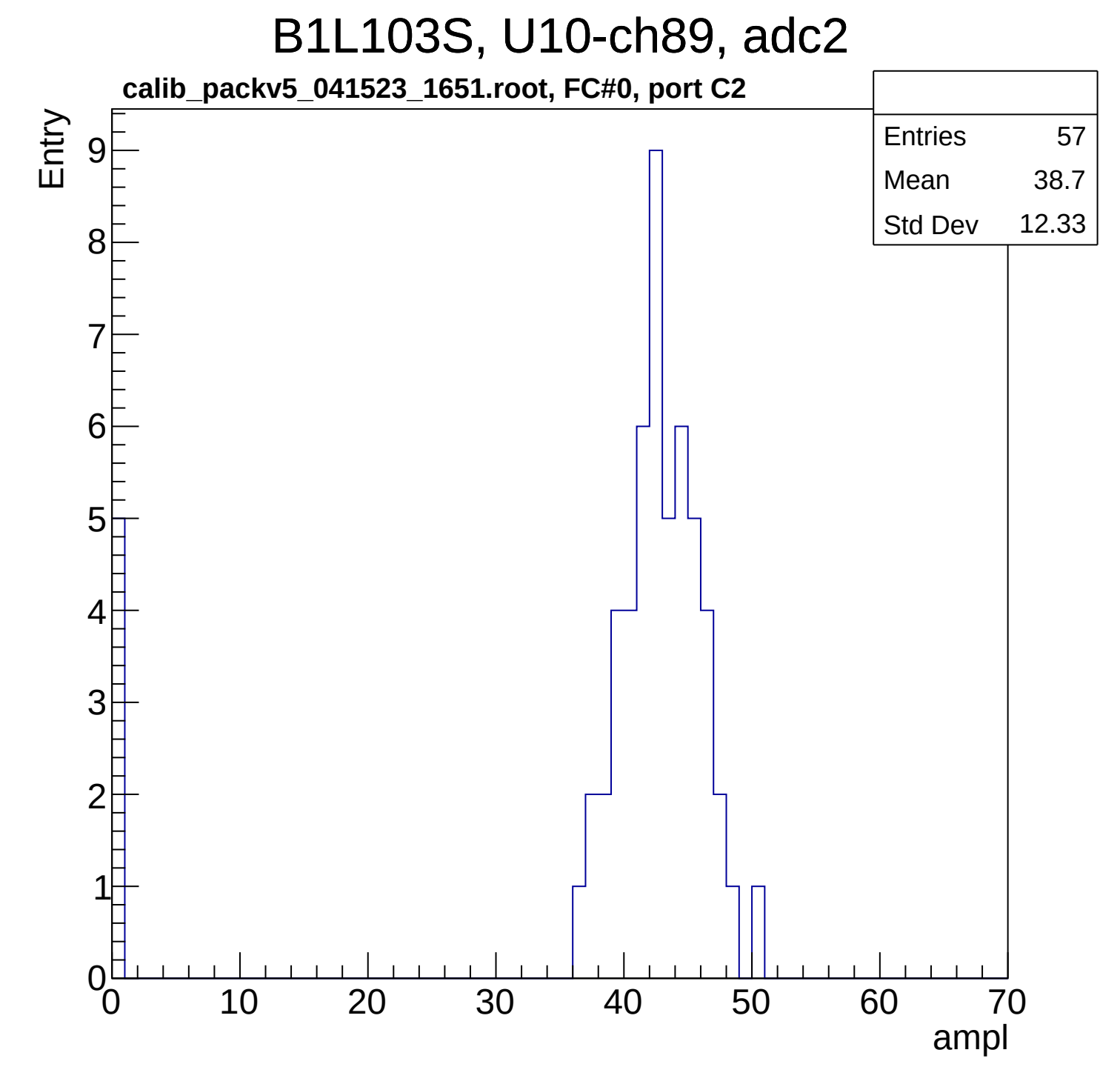
50
60
70
ampl


B1L103S, U10-ch89, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 31.26
Std Dev 11.81
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch89, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 38.7
Std Dev 12.33
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
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40
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60
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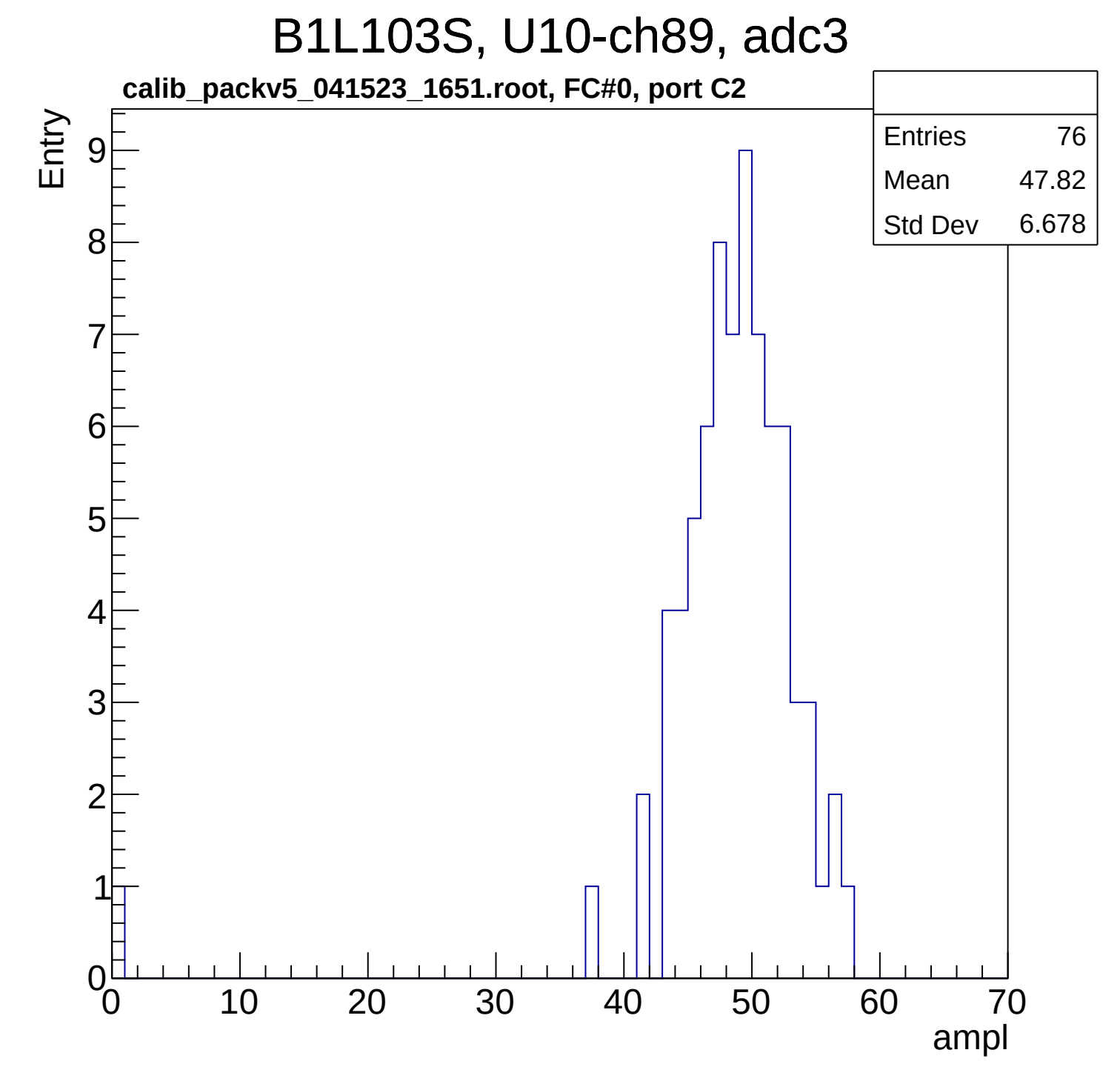
B1L103S, U10-ch89, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 47.82
Std Dev 6.678
Entry
ampl
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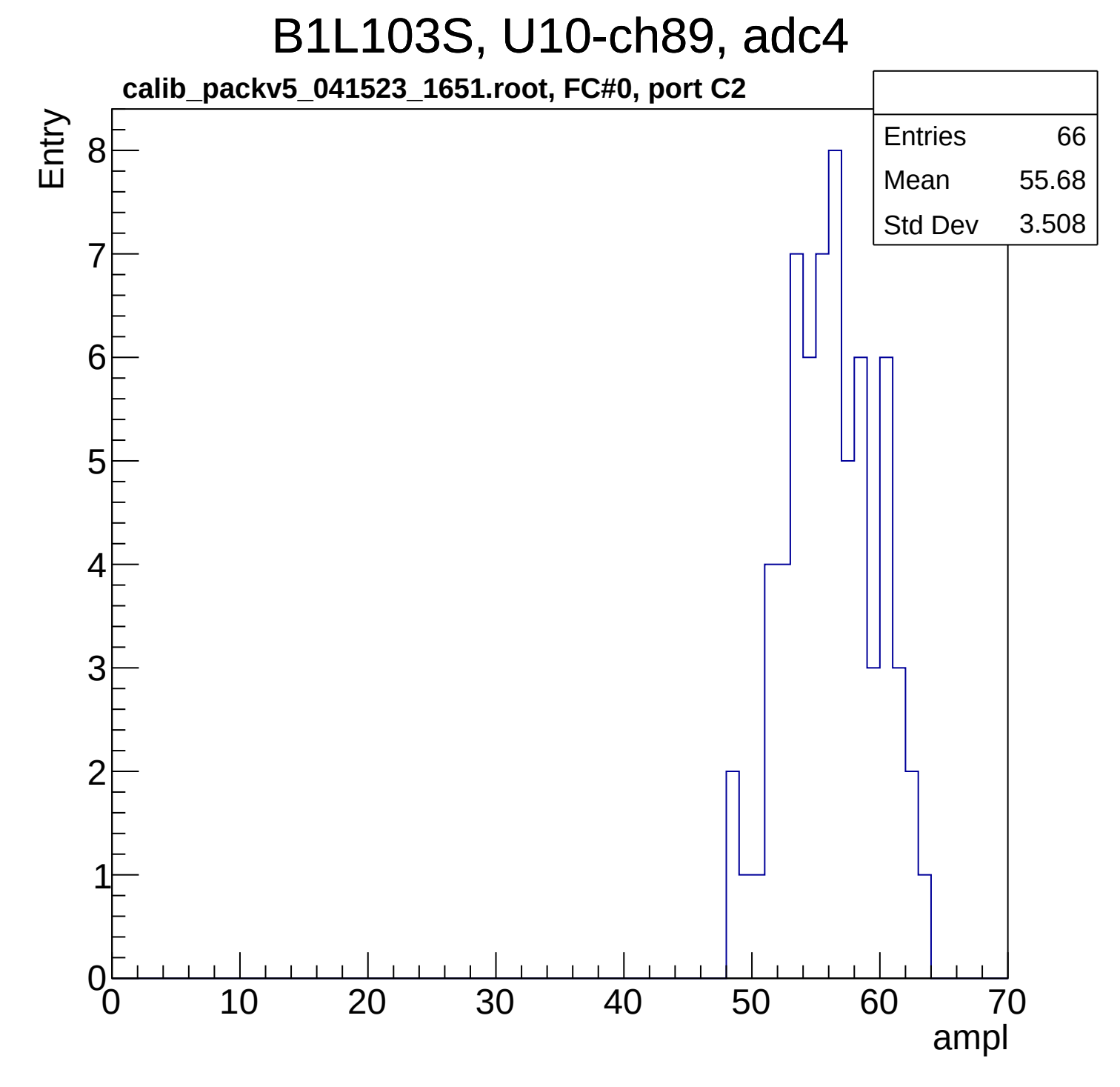
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U10-ch89, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 55.68
Std Dev 3.508
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
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60
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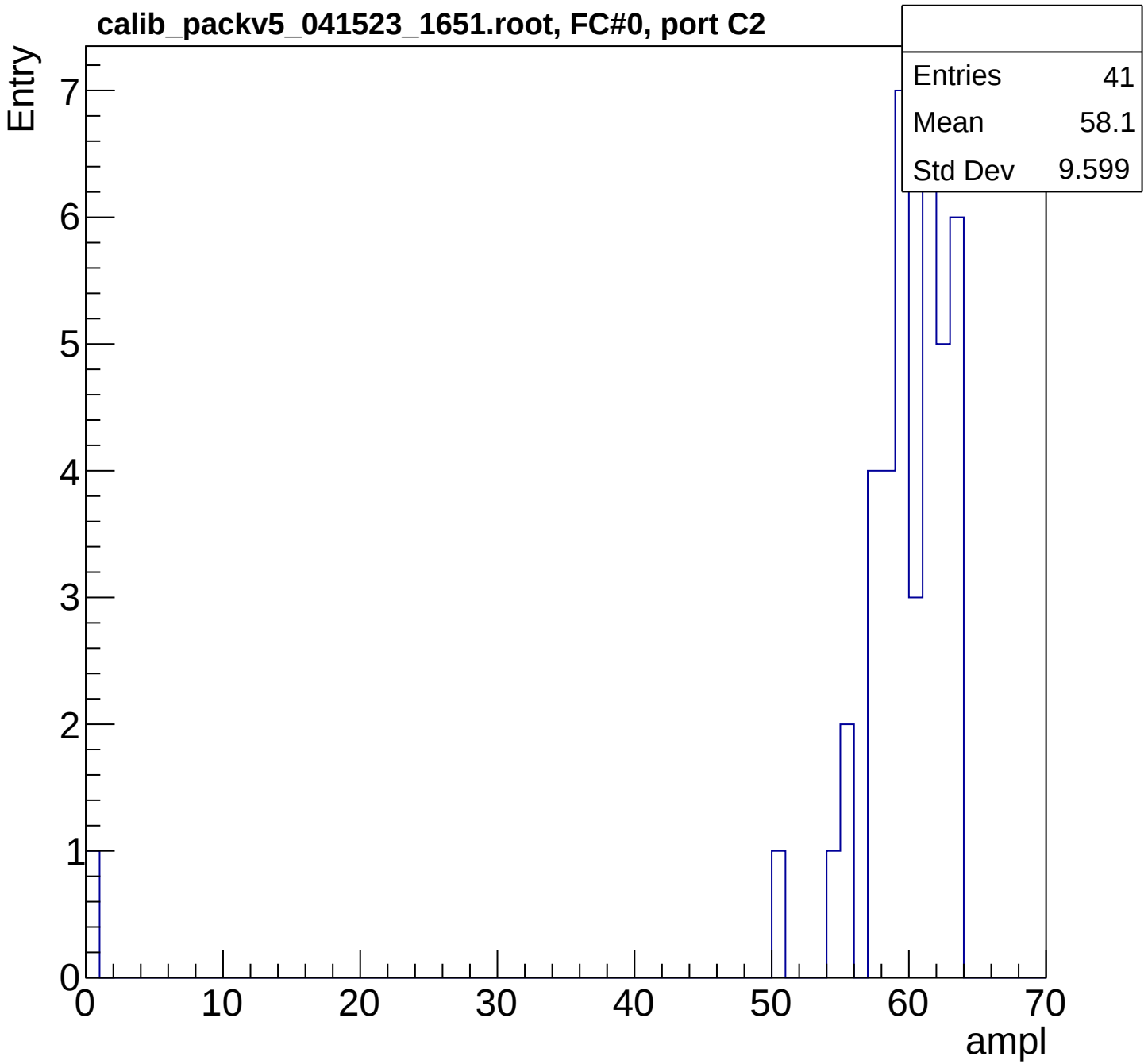
B1L103S, U10-ch89, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 41
Mean 58.1
Std Dev 9.599
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
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40
50
60
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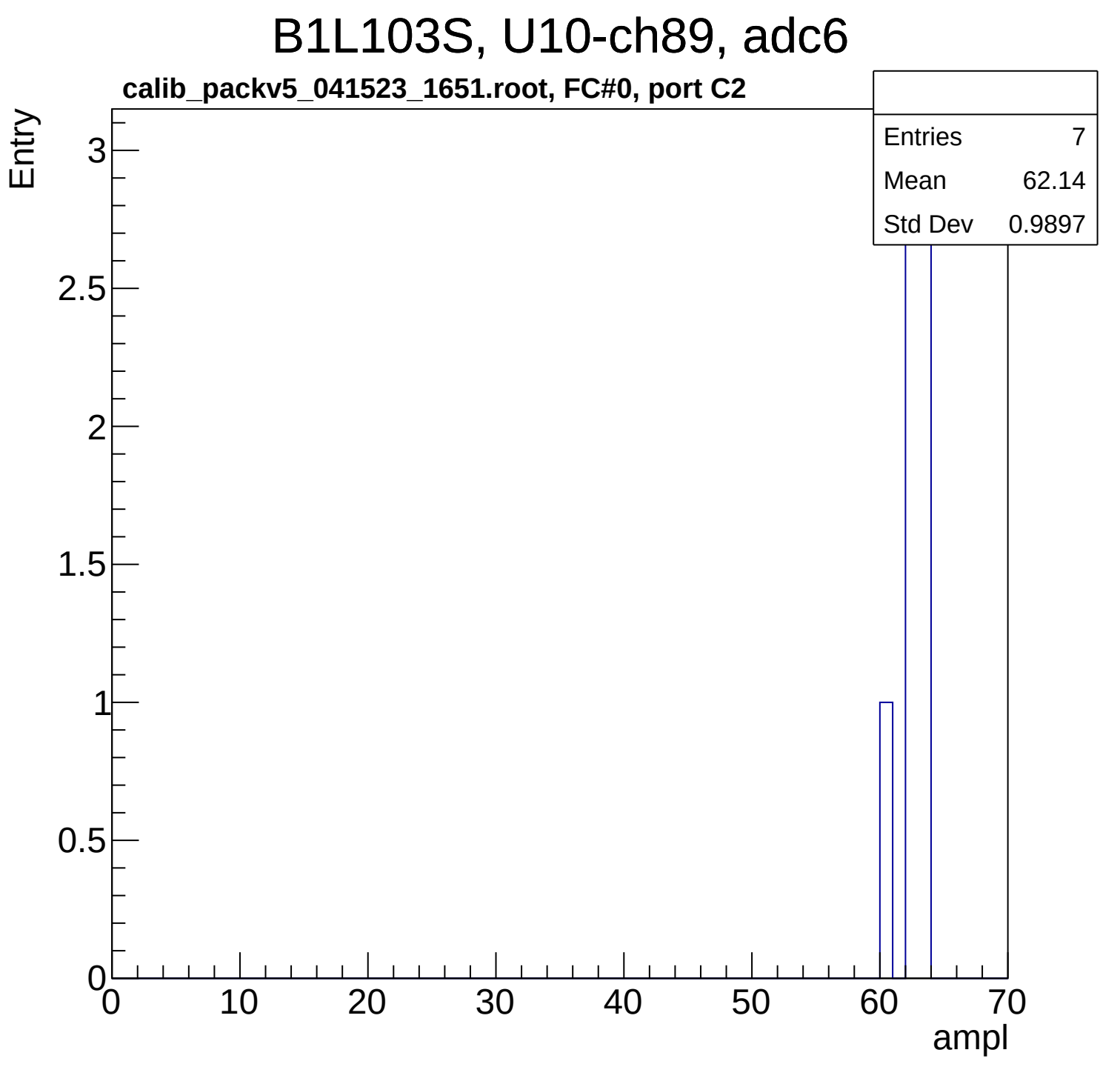
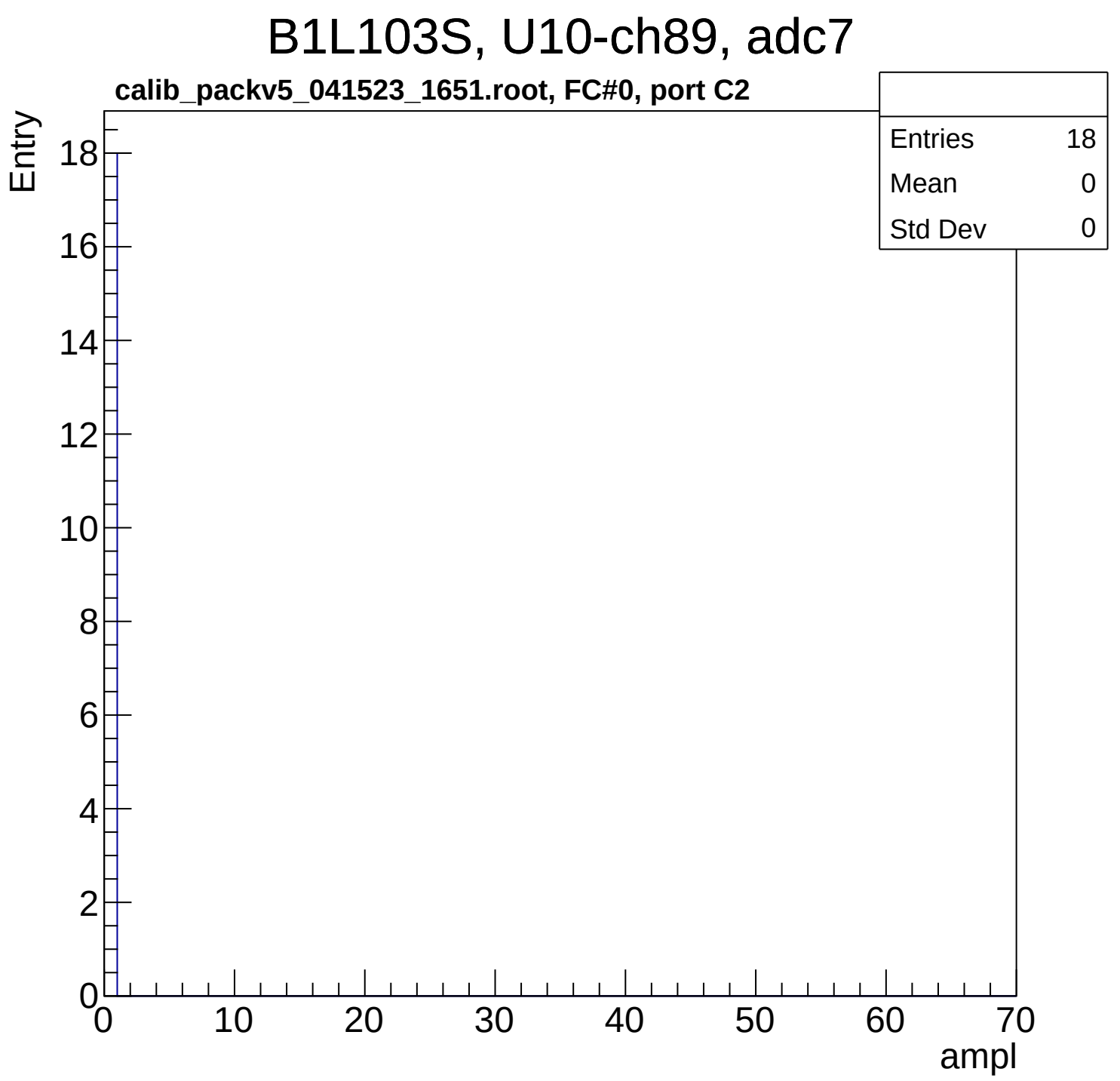
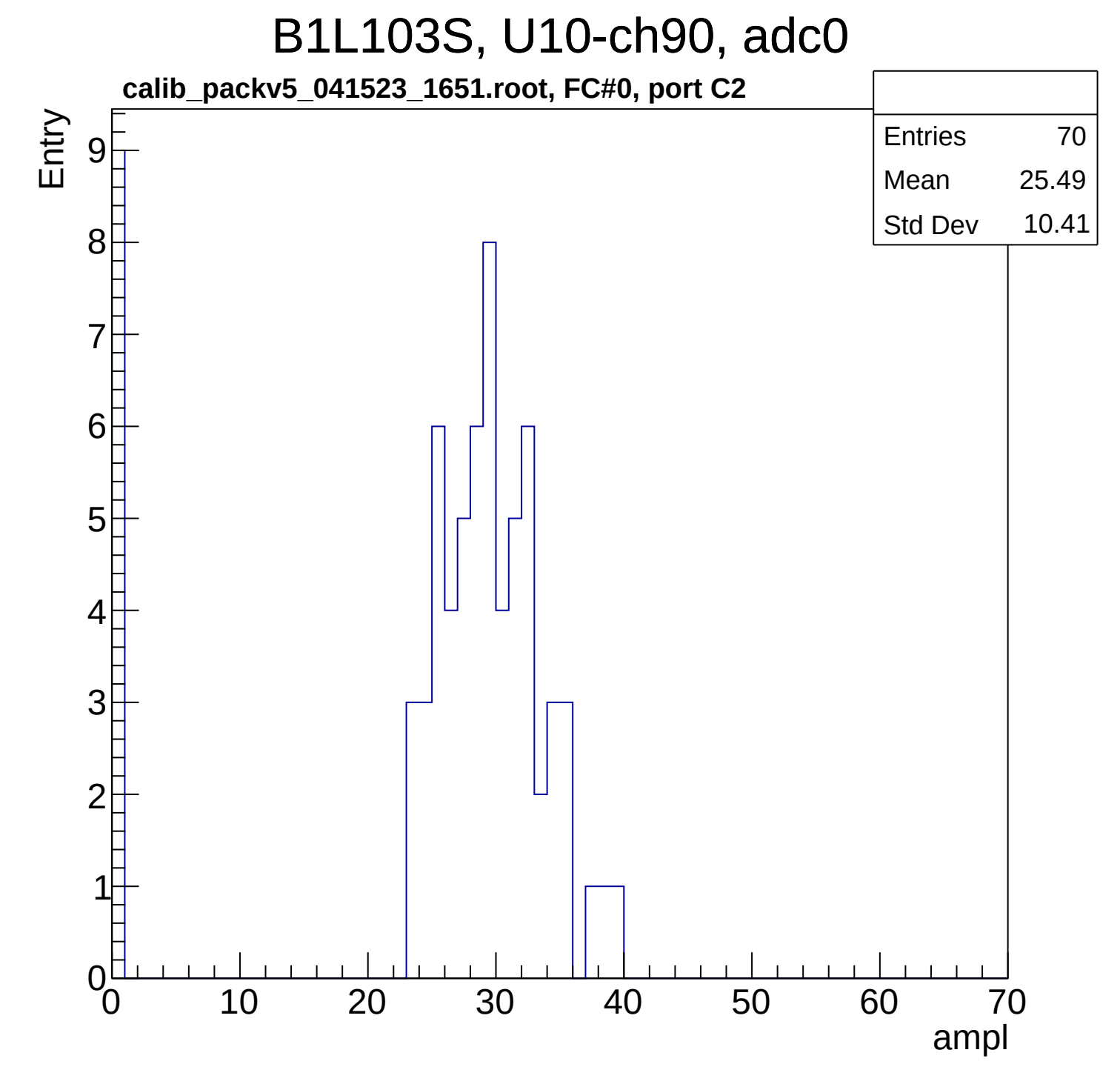

B1L103S, U10-ch89, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 62.14
Std Dev 0.9897
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U10-ch89, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch90, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 25.49
Std Dev 10.41
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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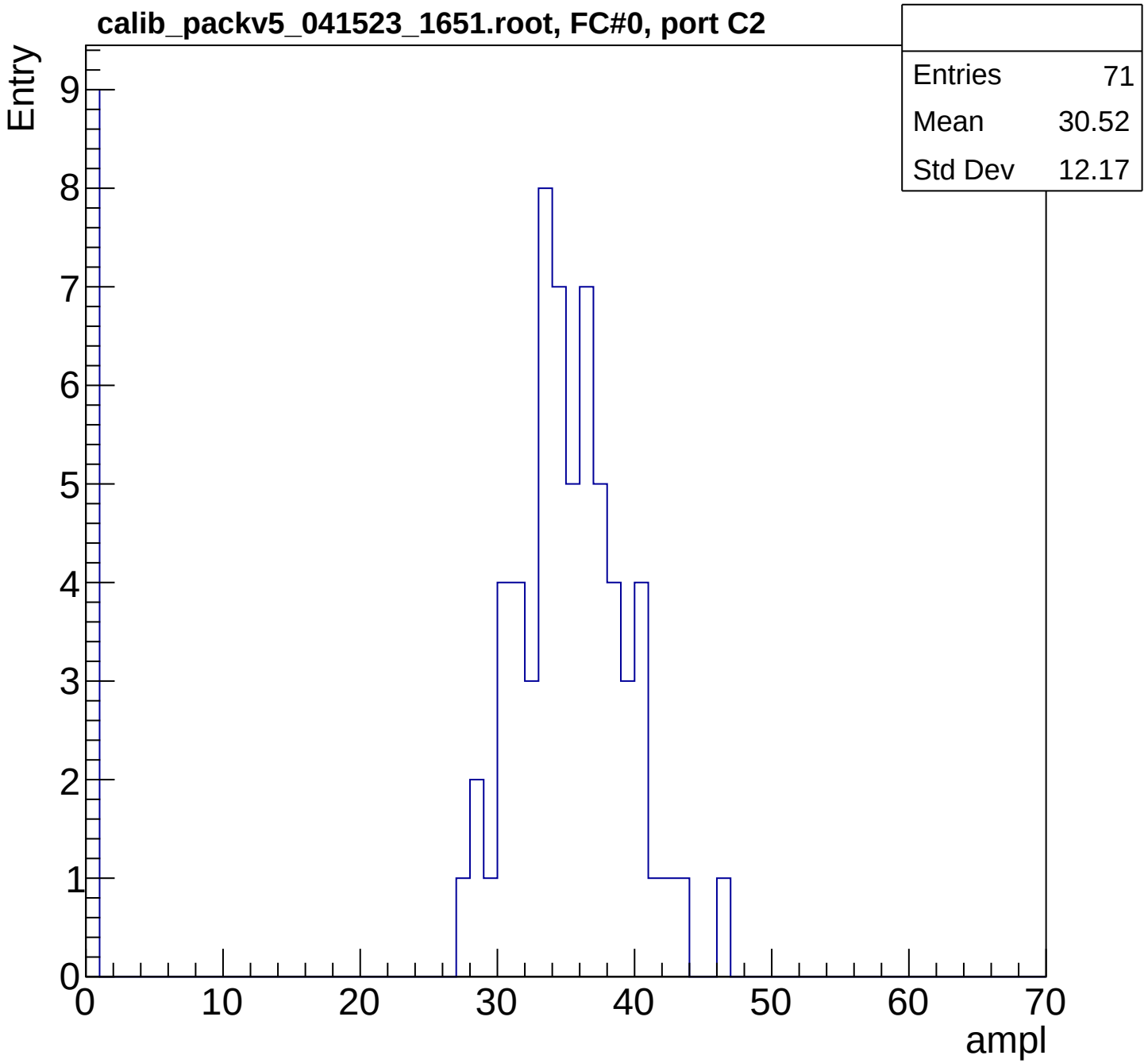
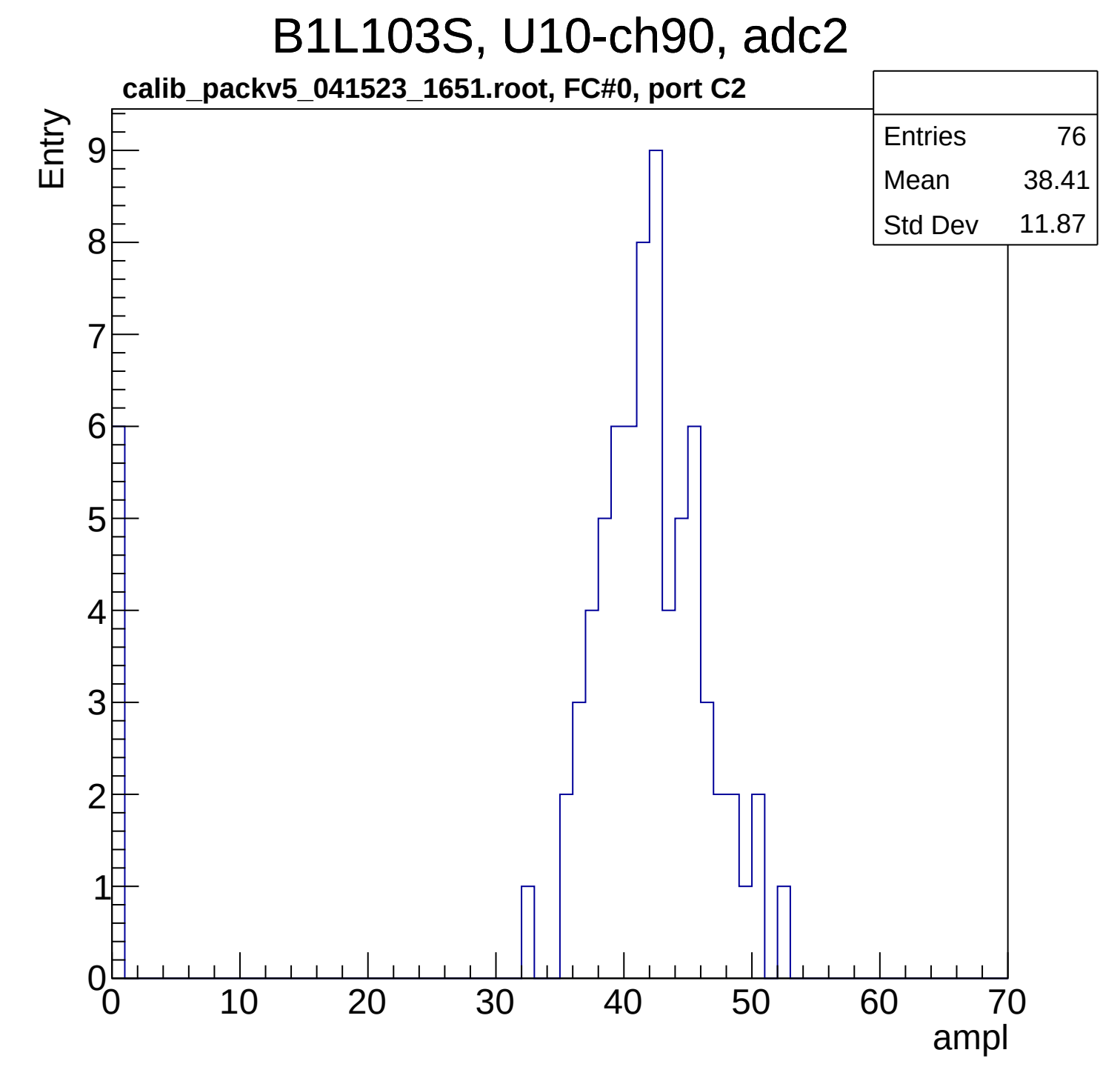
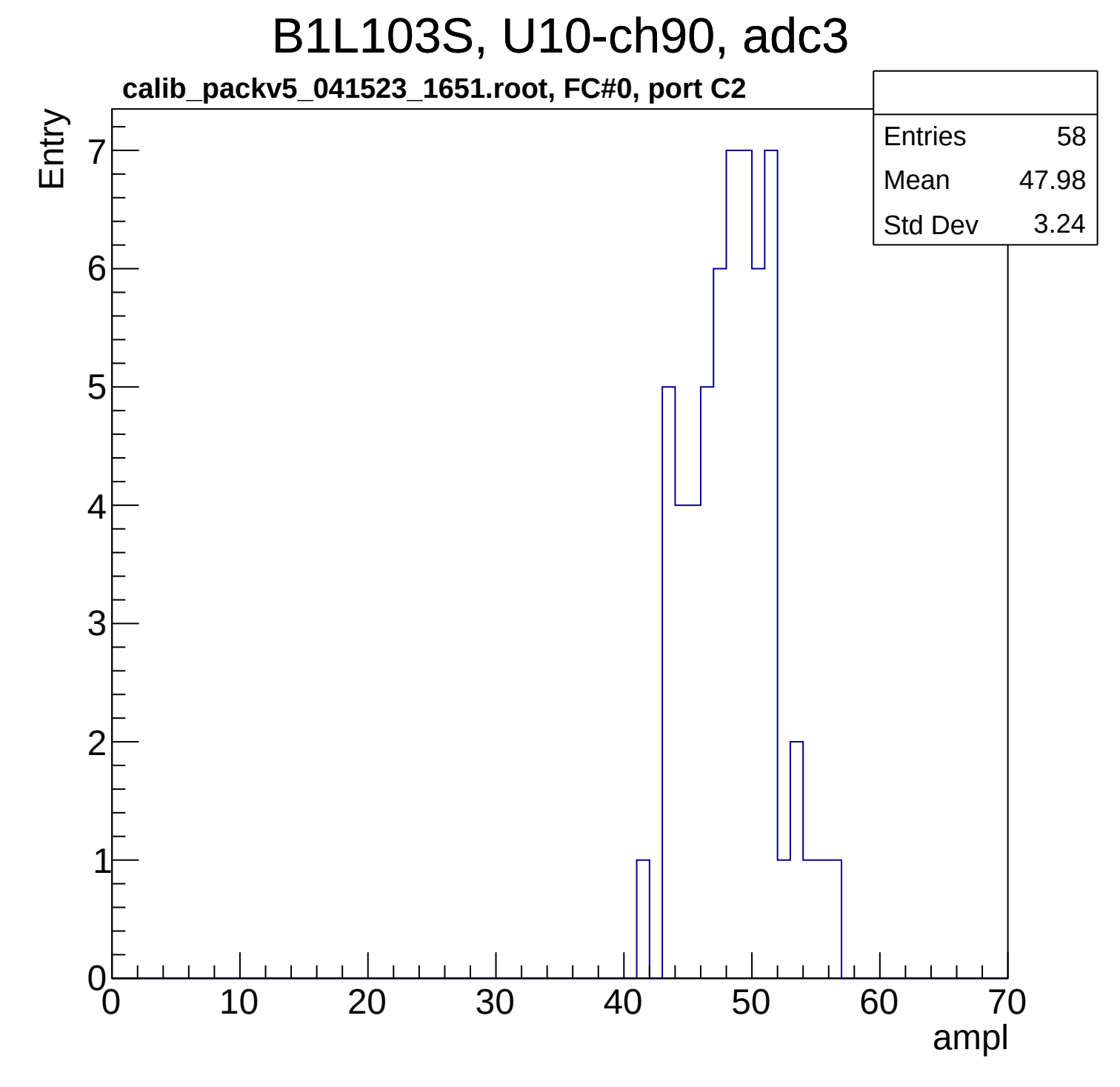
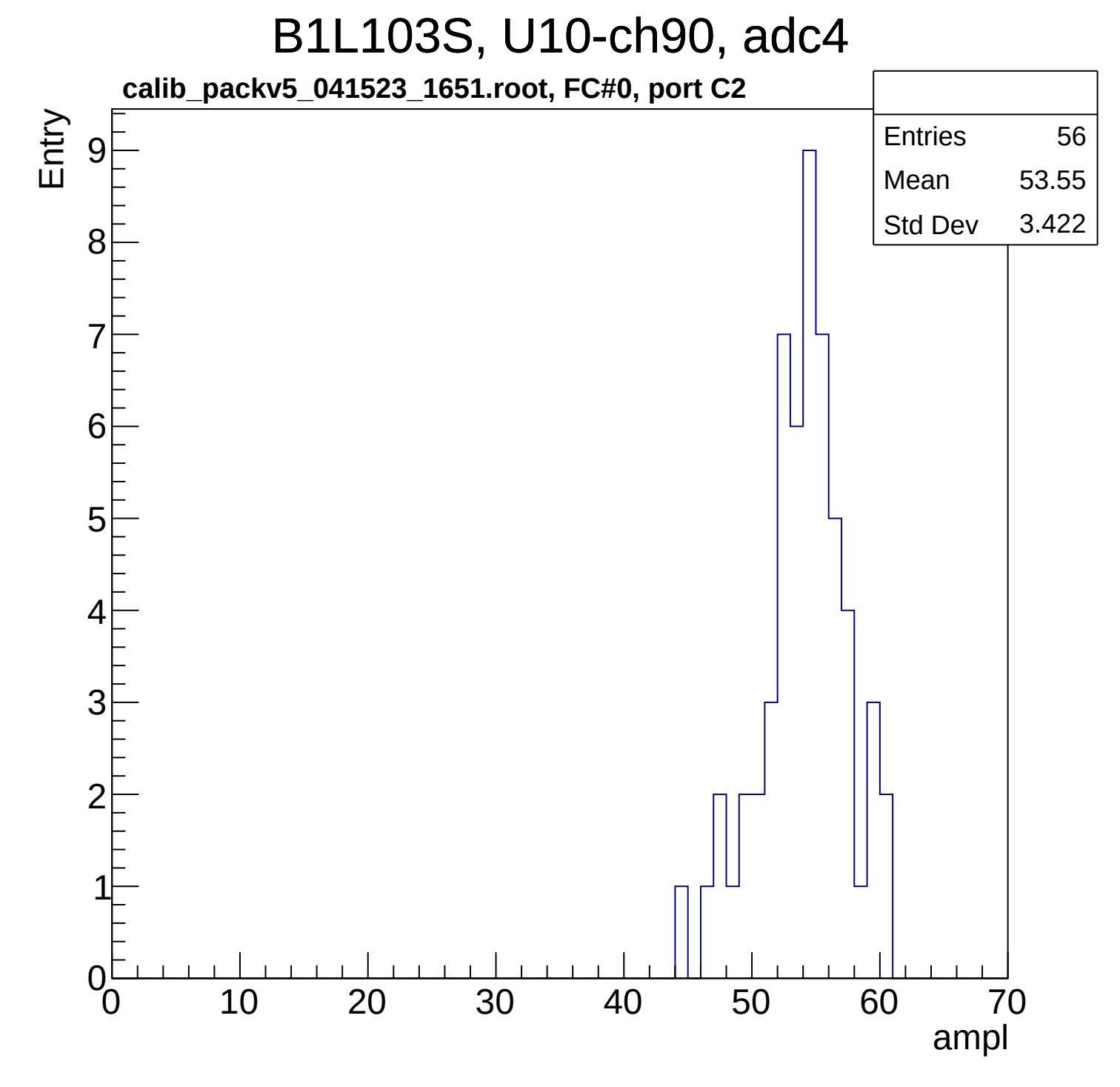
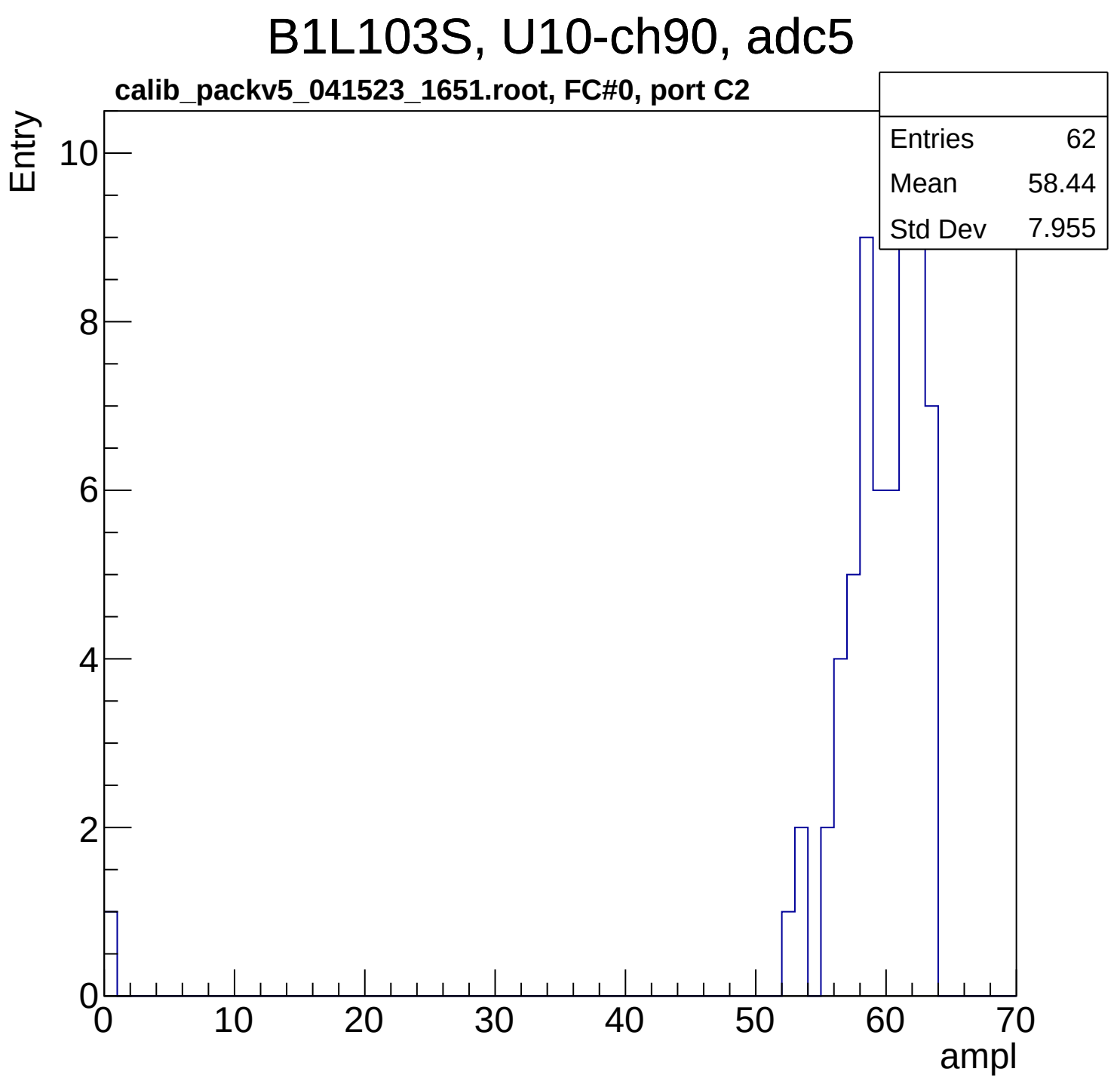
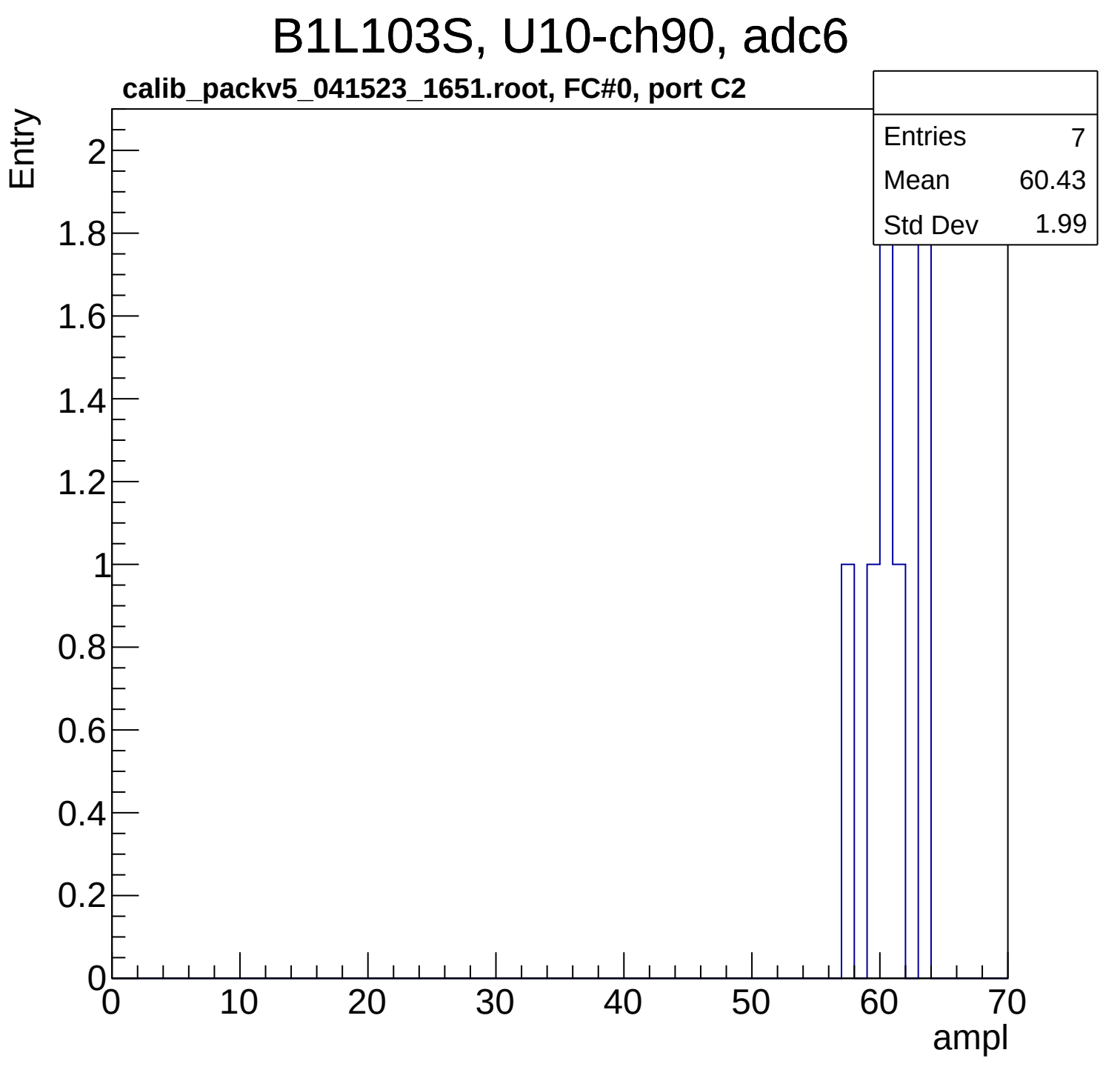

B1L103S, U10-ch90, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 30.52
Std Dev 12.17
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

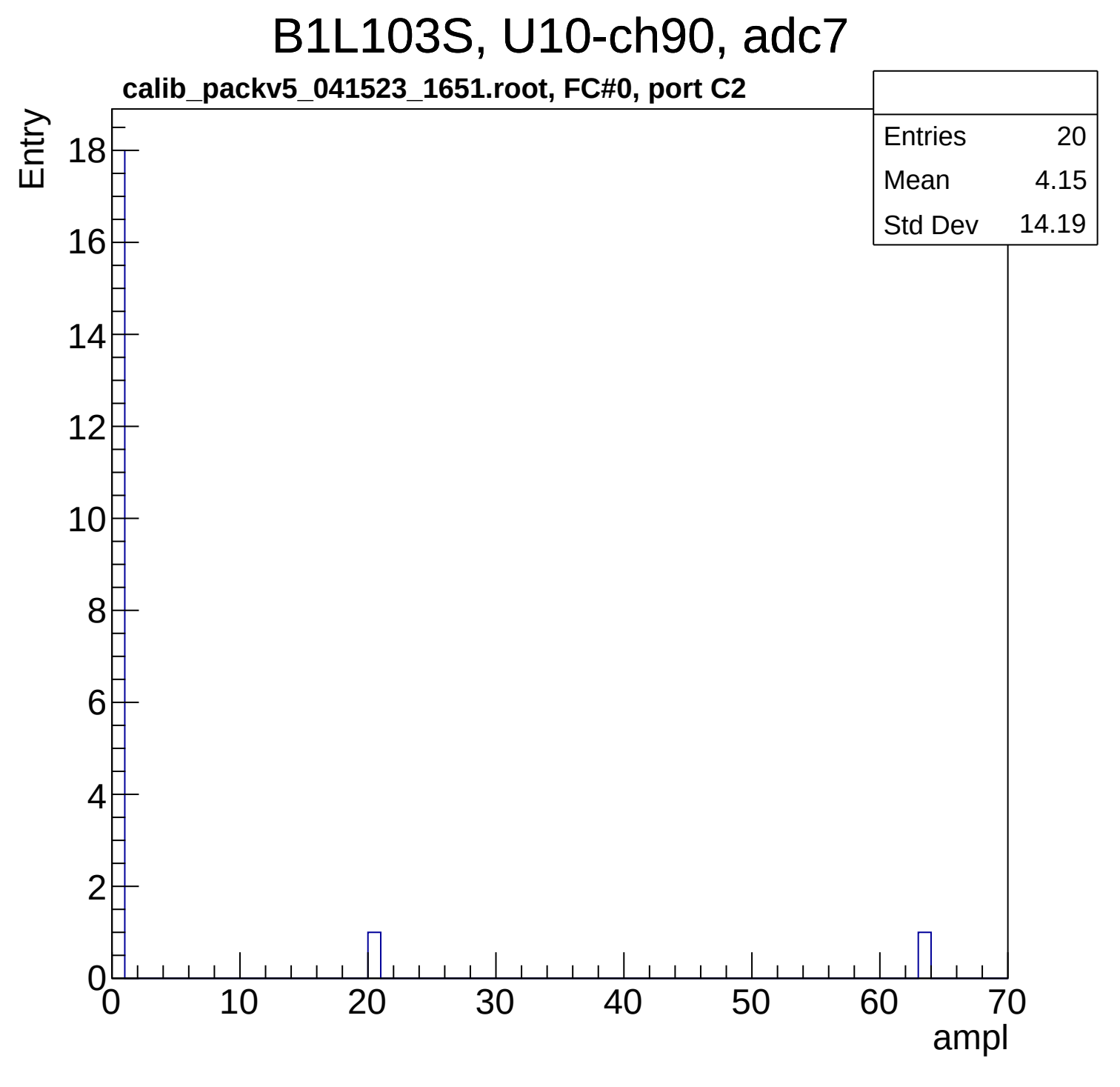

B1L103S, U10-ch90, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 38.41
Std Dev 11.87
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

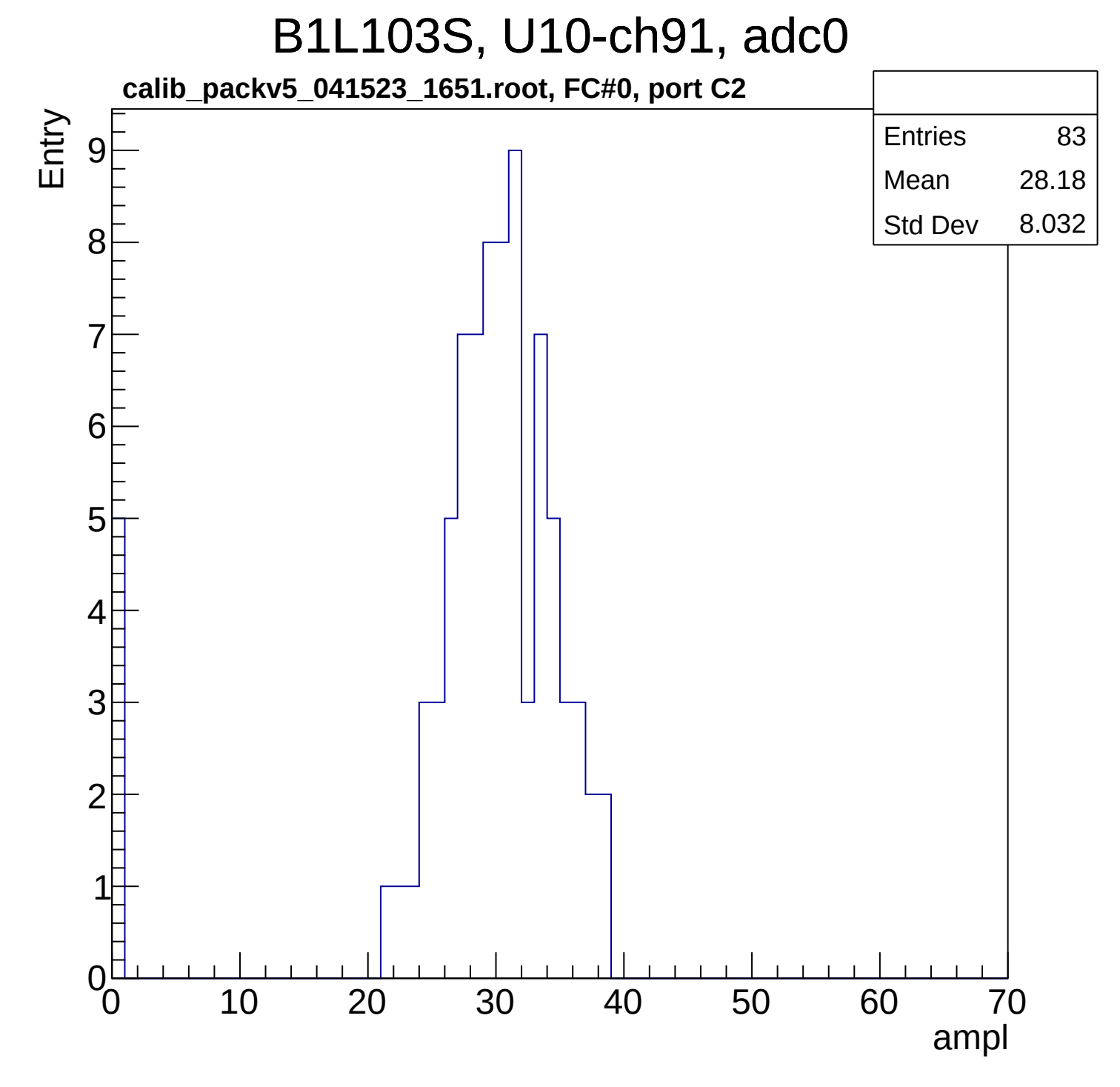

B1L103S, U10-ch90, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 47.98
Std Dev 3.24
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U10-ch90, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 53.55
Std Dev 3.422
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U10-ch90, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 58.44
Std Dev 7.955
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U10-ch90, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 60.43
Std Dev 1.99
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U10-ch90, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 4.15
Std Dev 14.19
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch91, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 28.18
Std Dev 8.032
Entry
ampl
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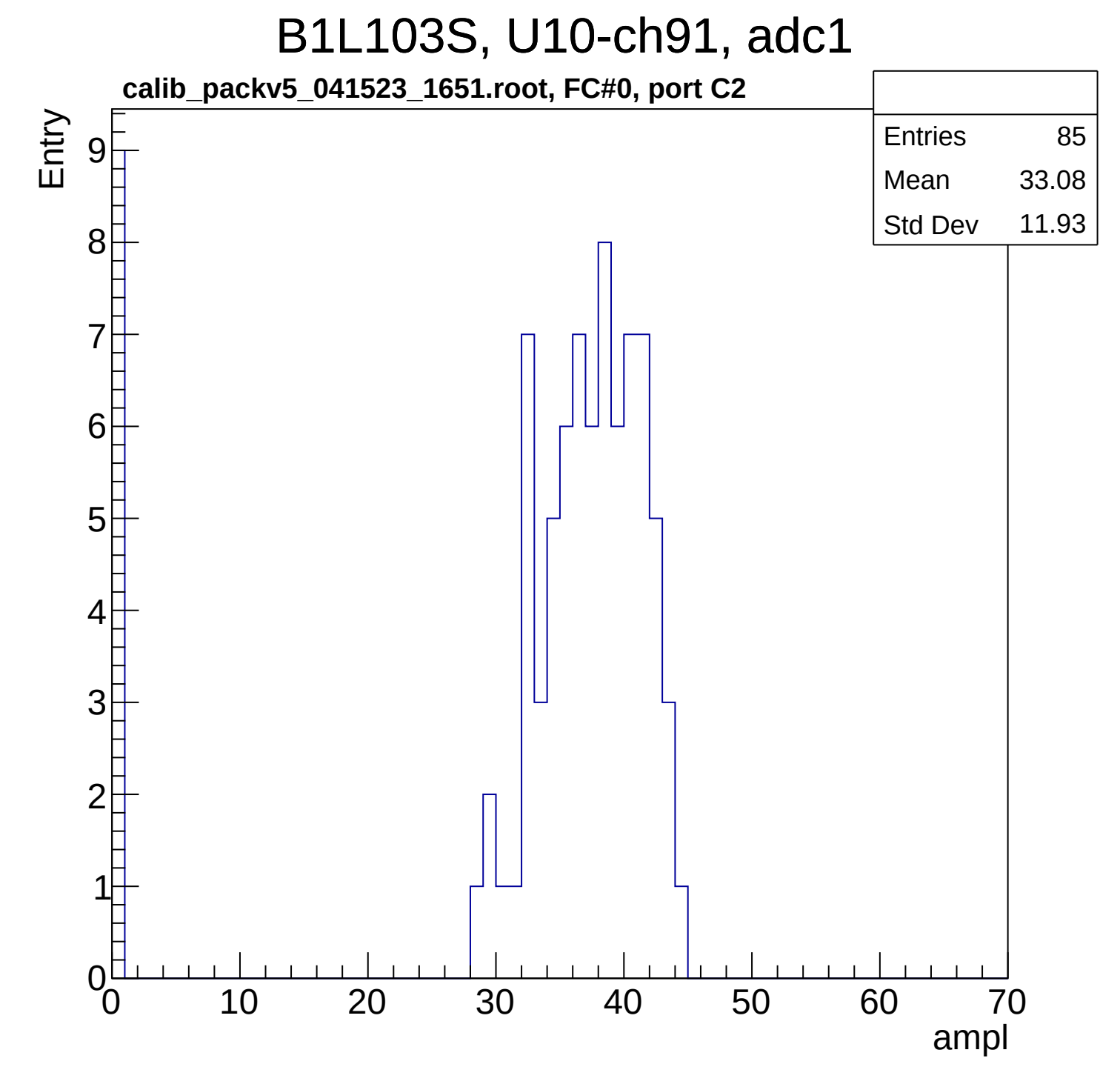
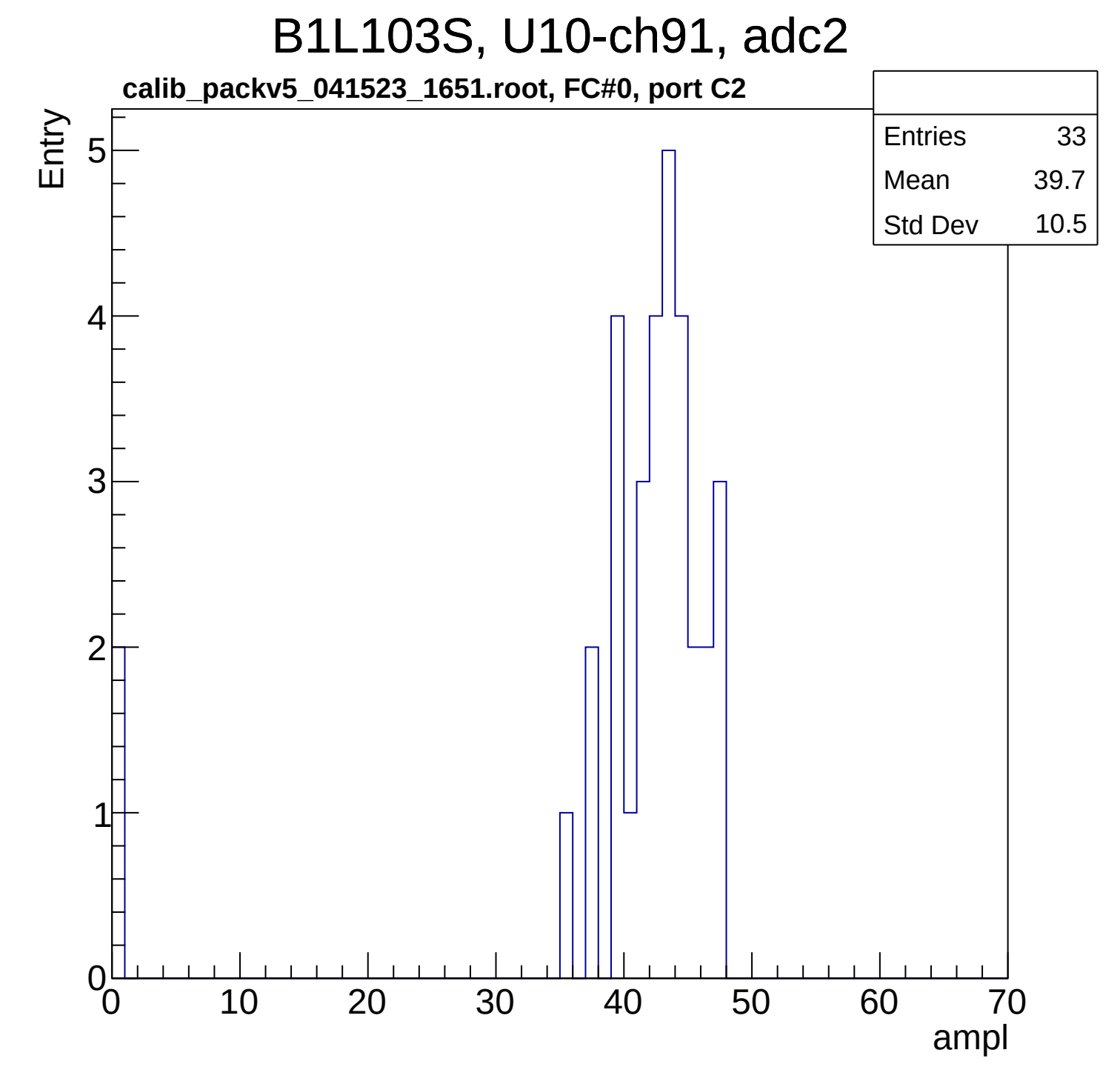
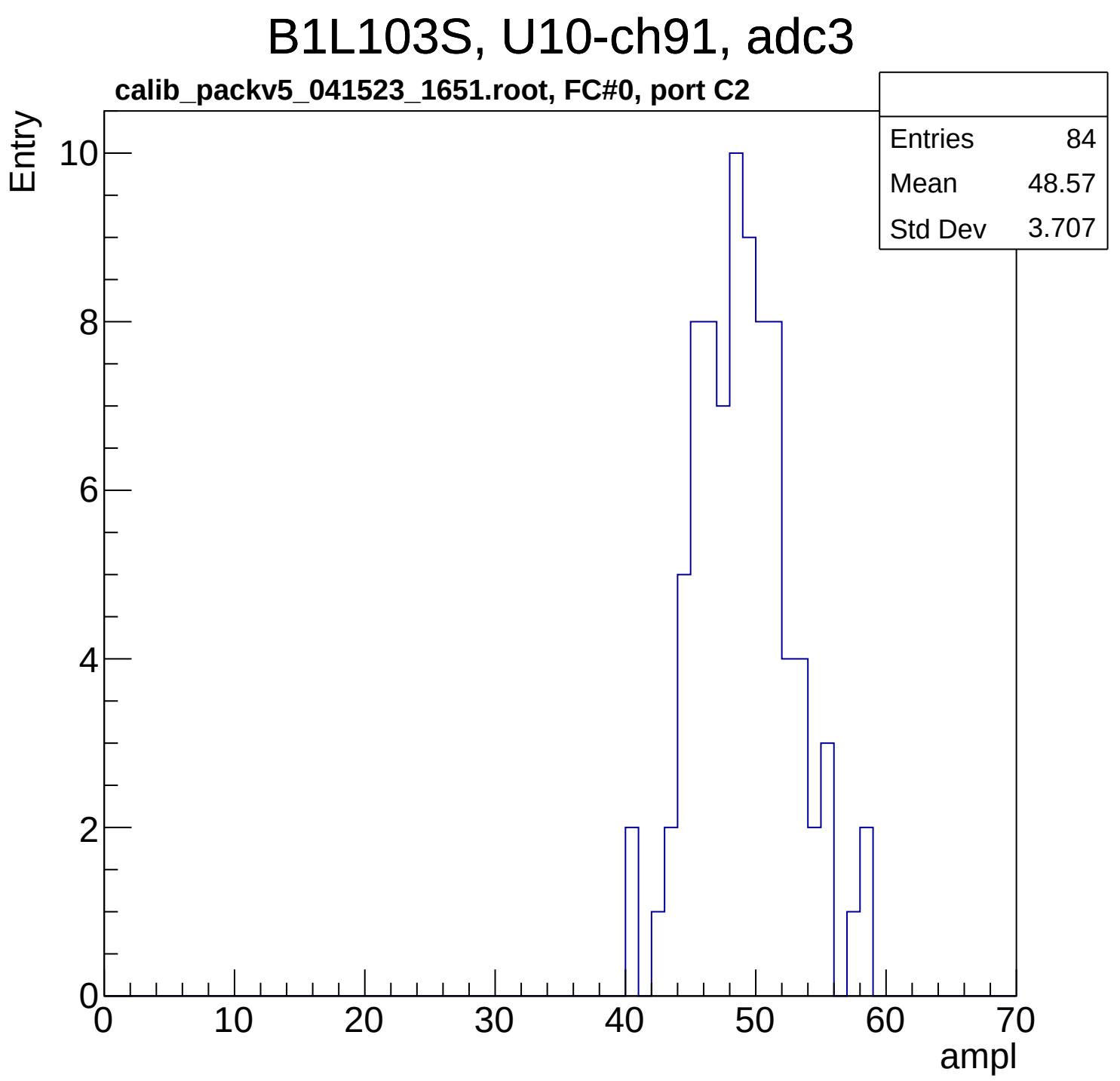
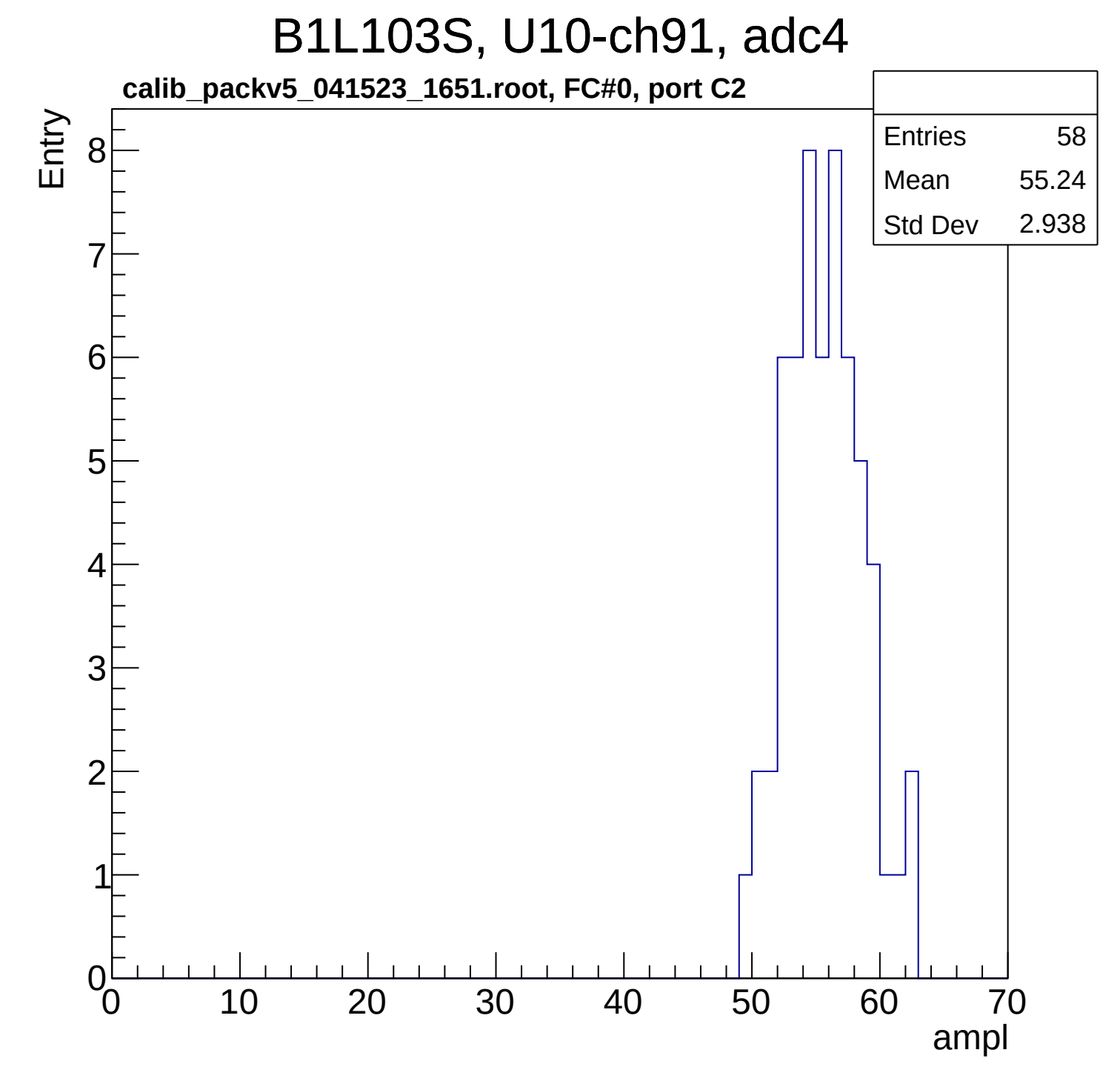
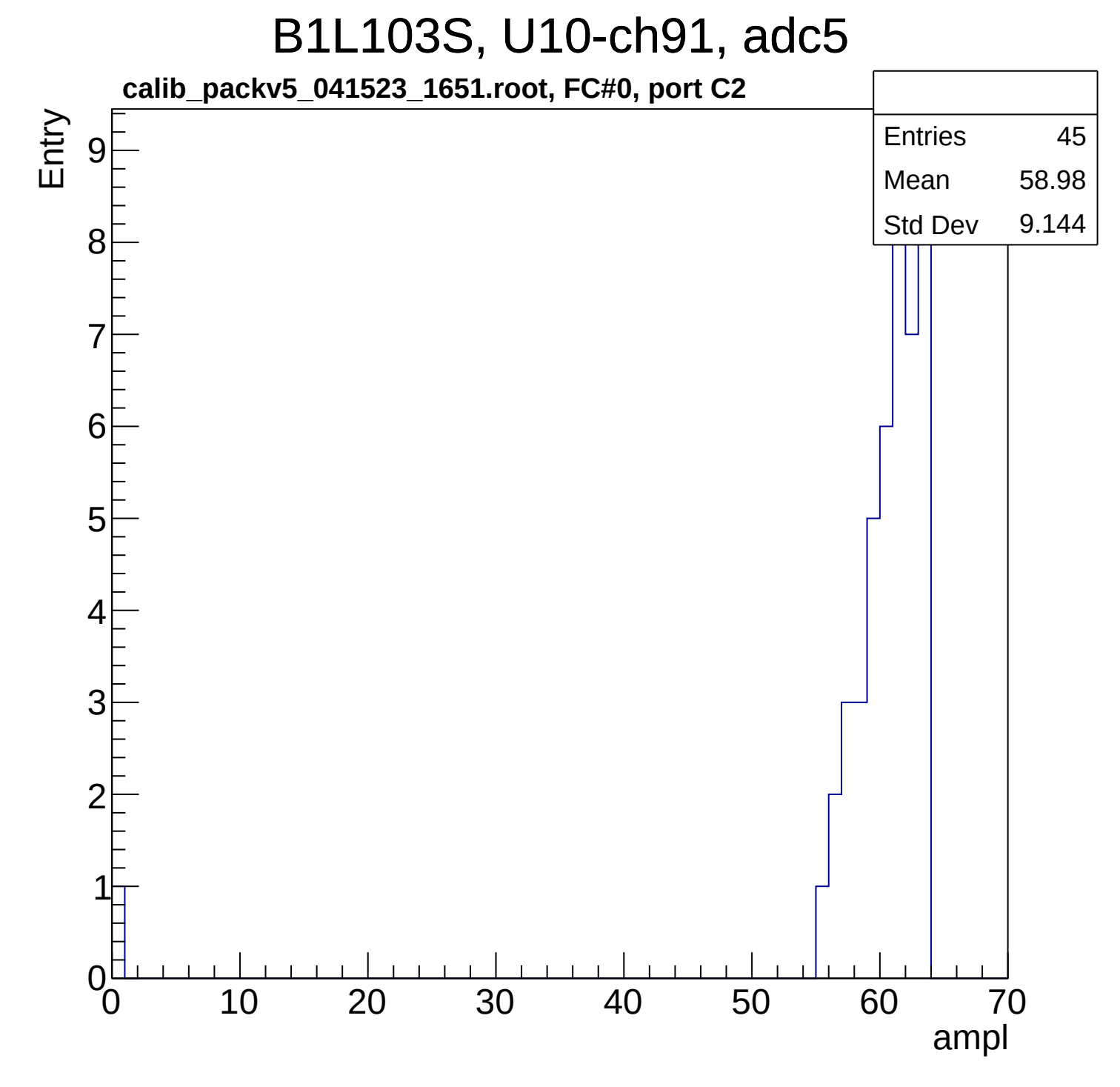
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U10-ch91, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 33.08
Std Dev 11.93
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U10-ch91, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 33
Mean 39.7
Std Dev 10.5
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch91, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 48.57
Std Dev 3.707
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U10-ch91, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 55.24
Std Dev 2.938
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U10-ch91, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 58.98
Std Dev 9.144
Entry
ampl
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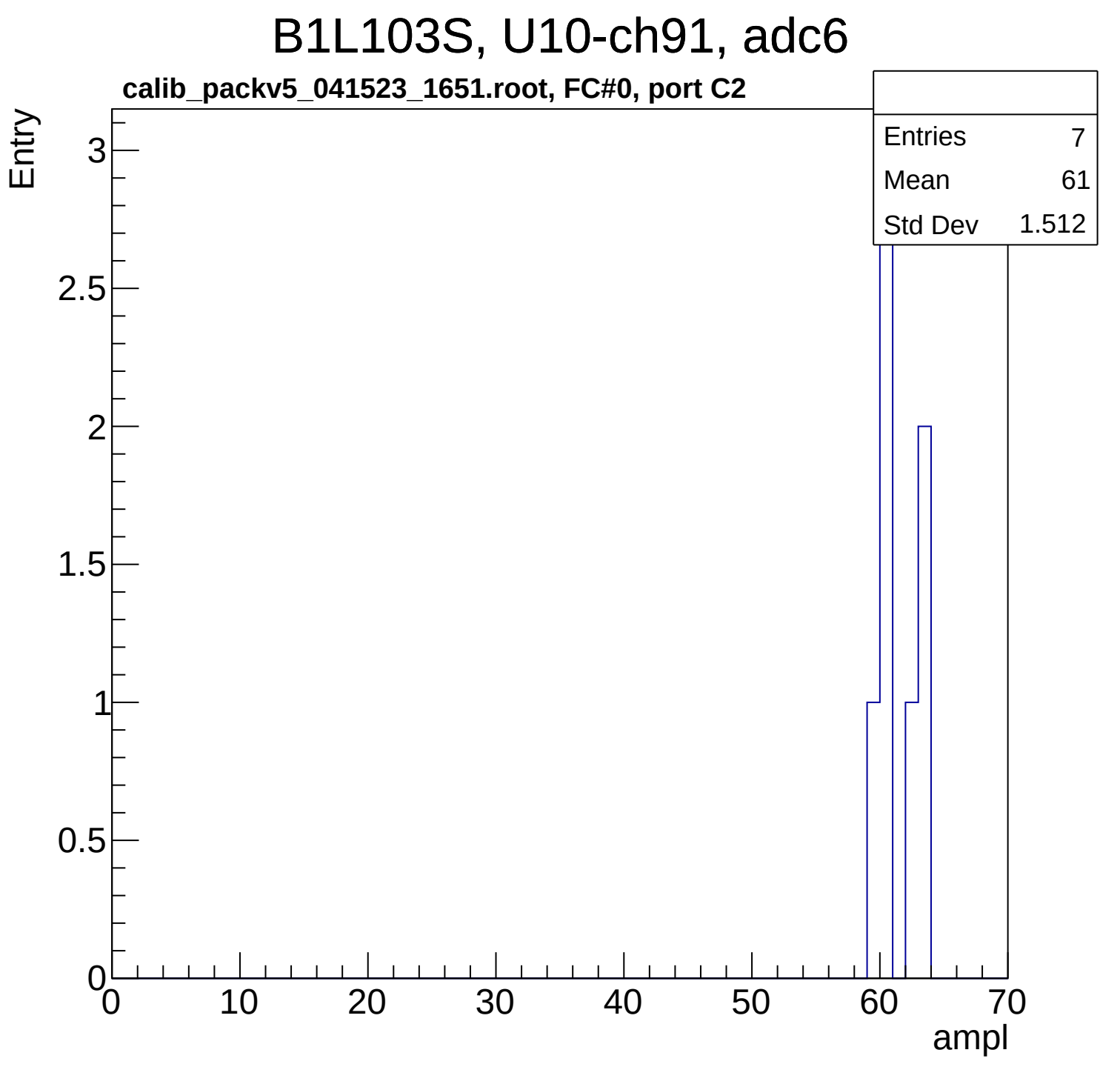
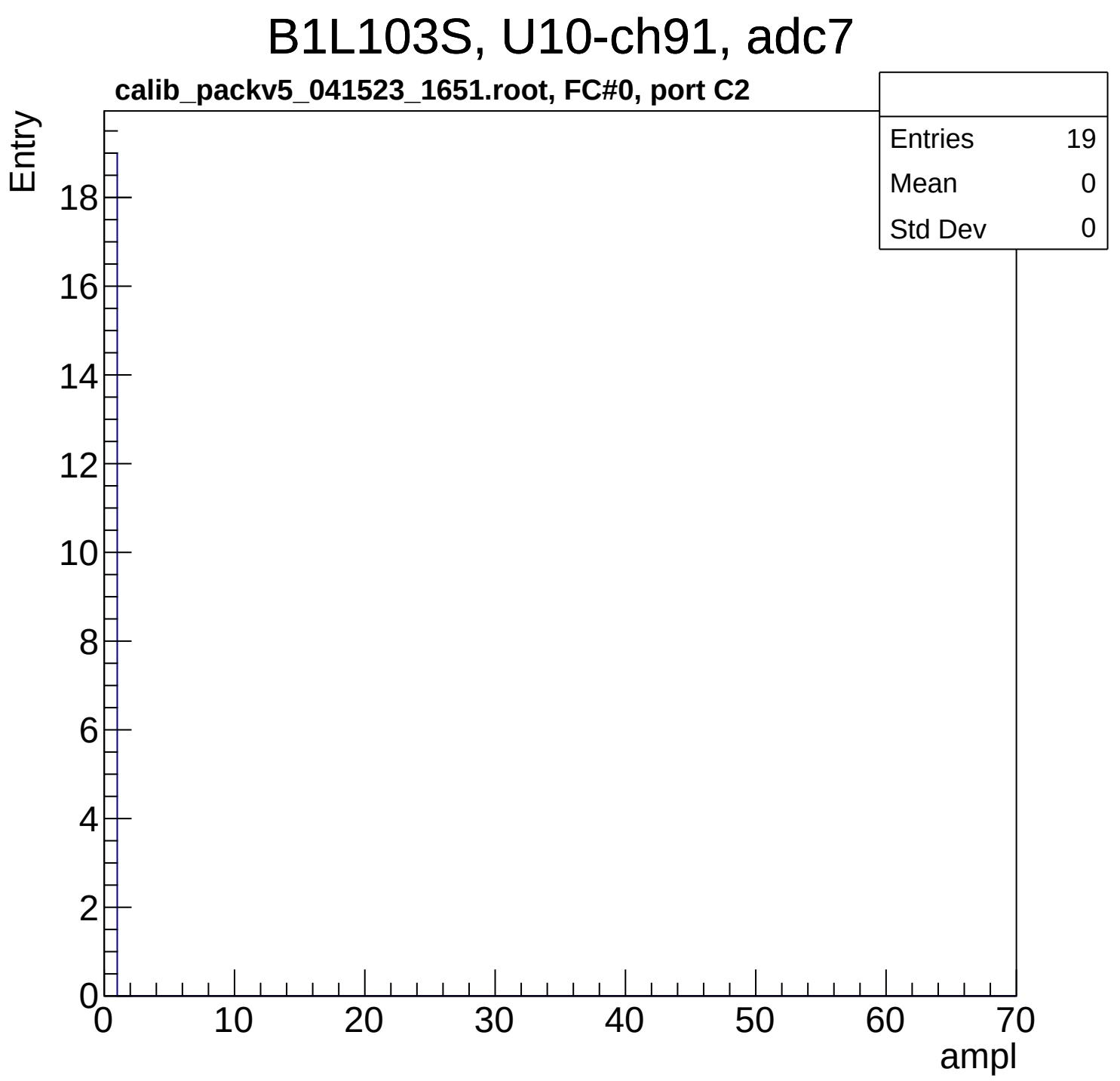
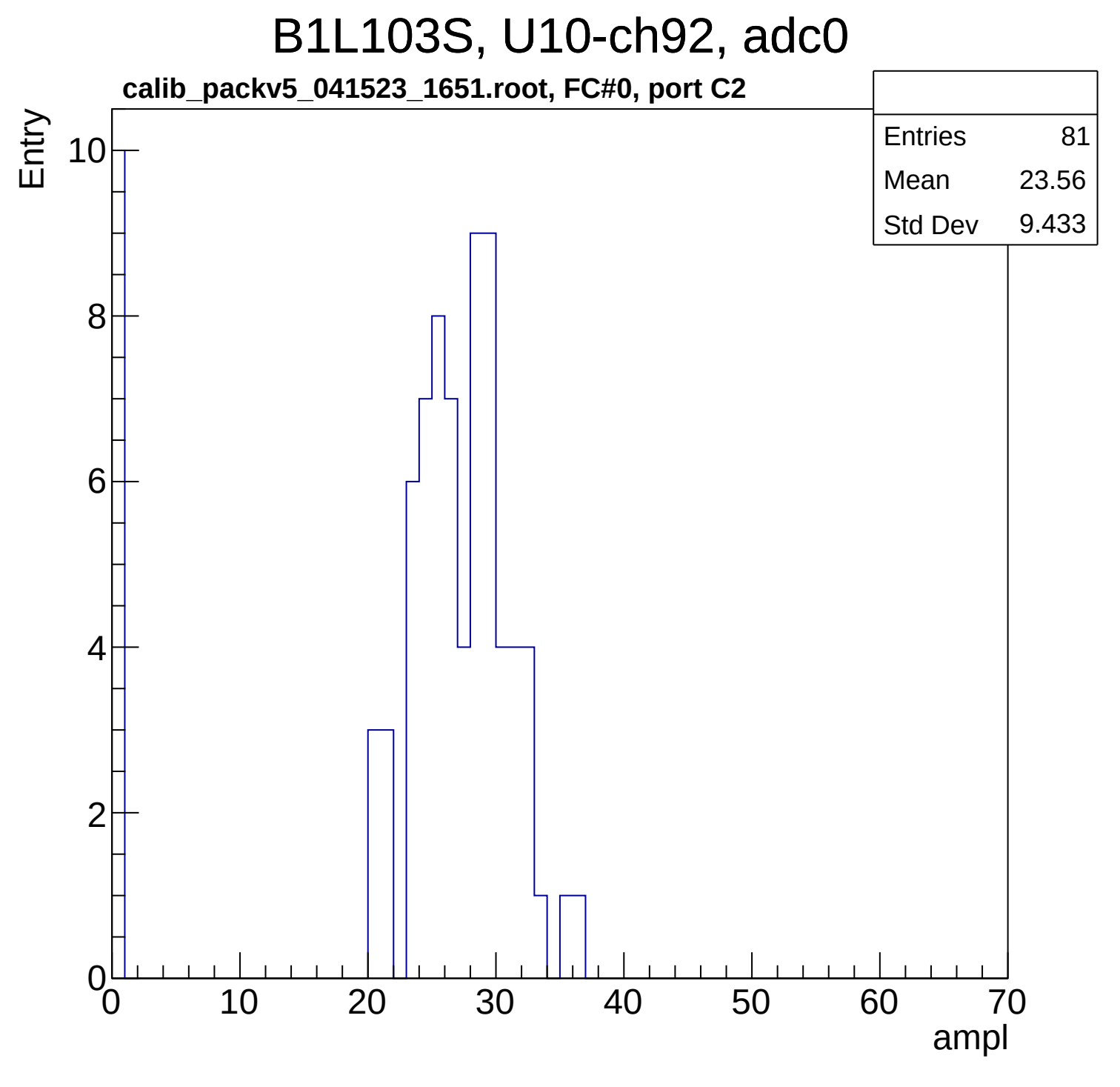
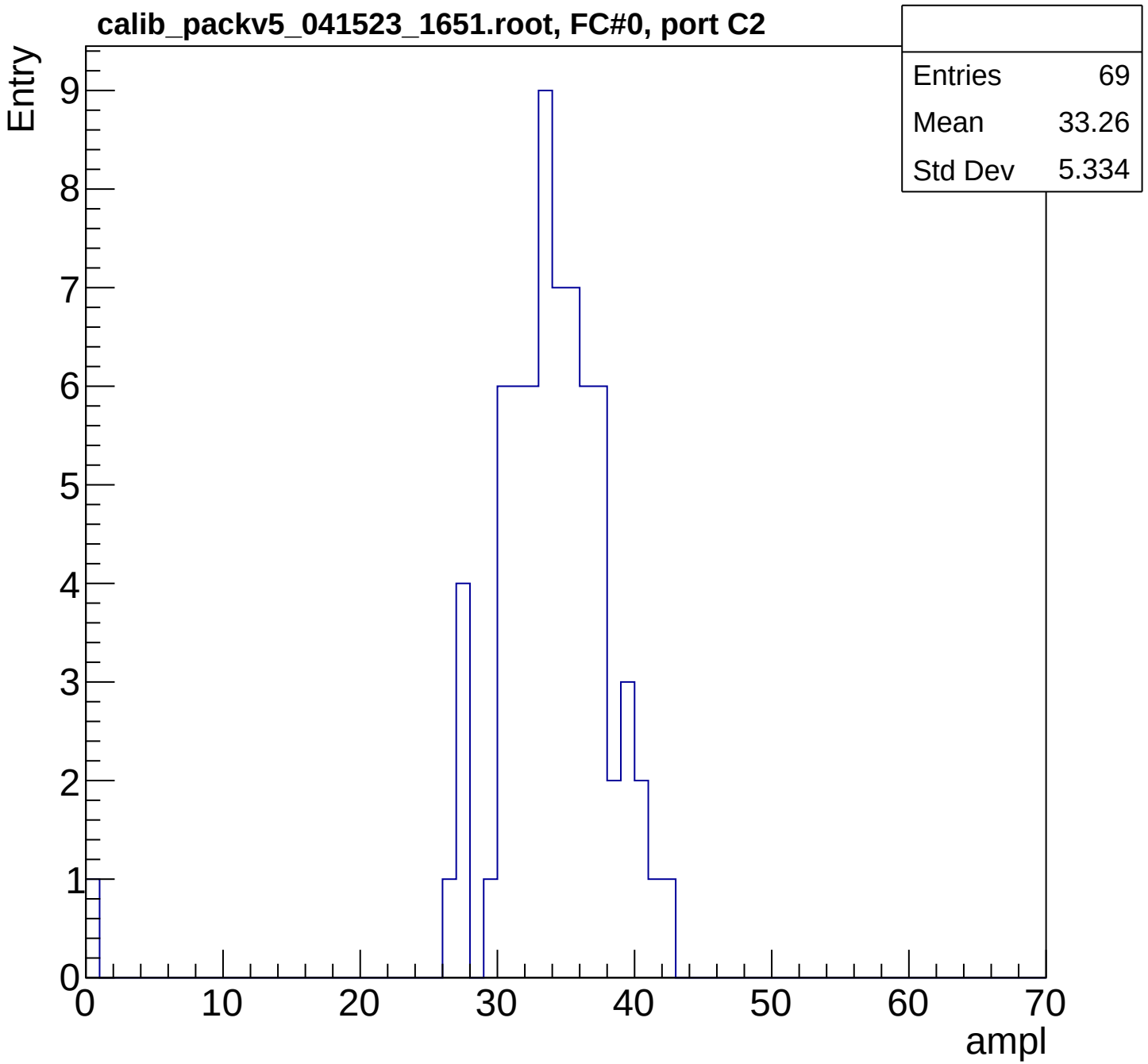
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U10-ch91, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 61
Std Dev 1.512
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U10-ch91, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch92, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 23.56
Std Dev 9.433
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U10-ch92, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 33.26
Std Dev 5.334
Entry
ampl
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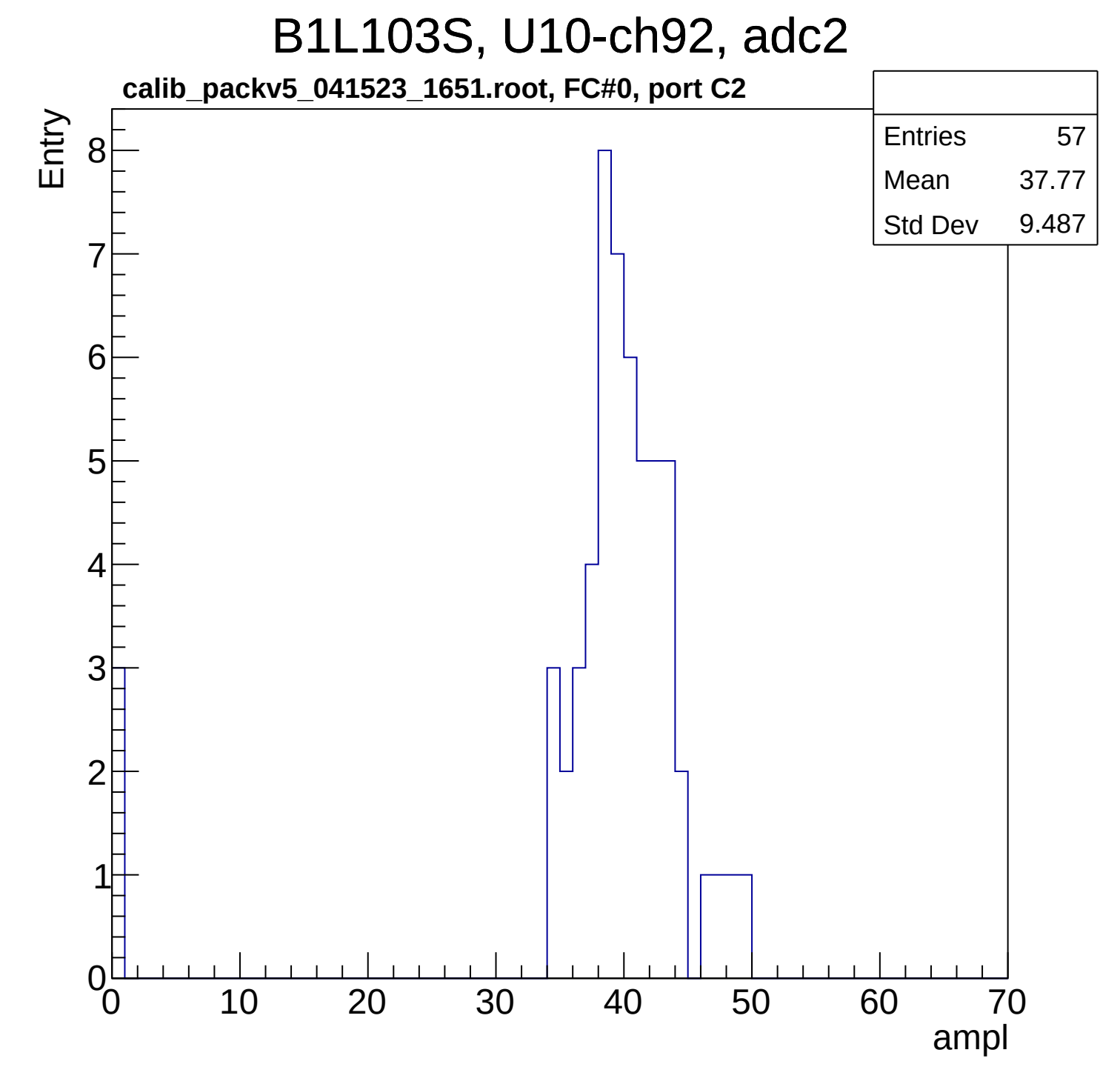
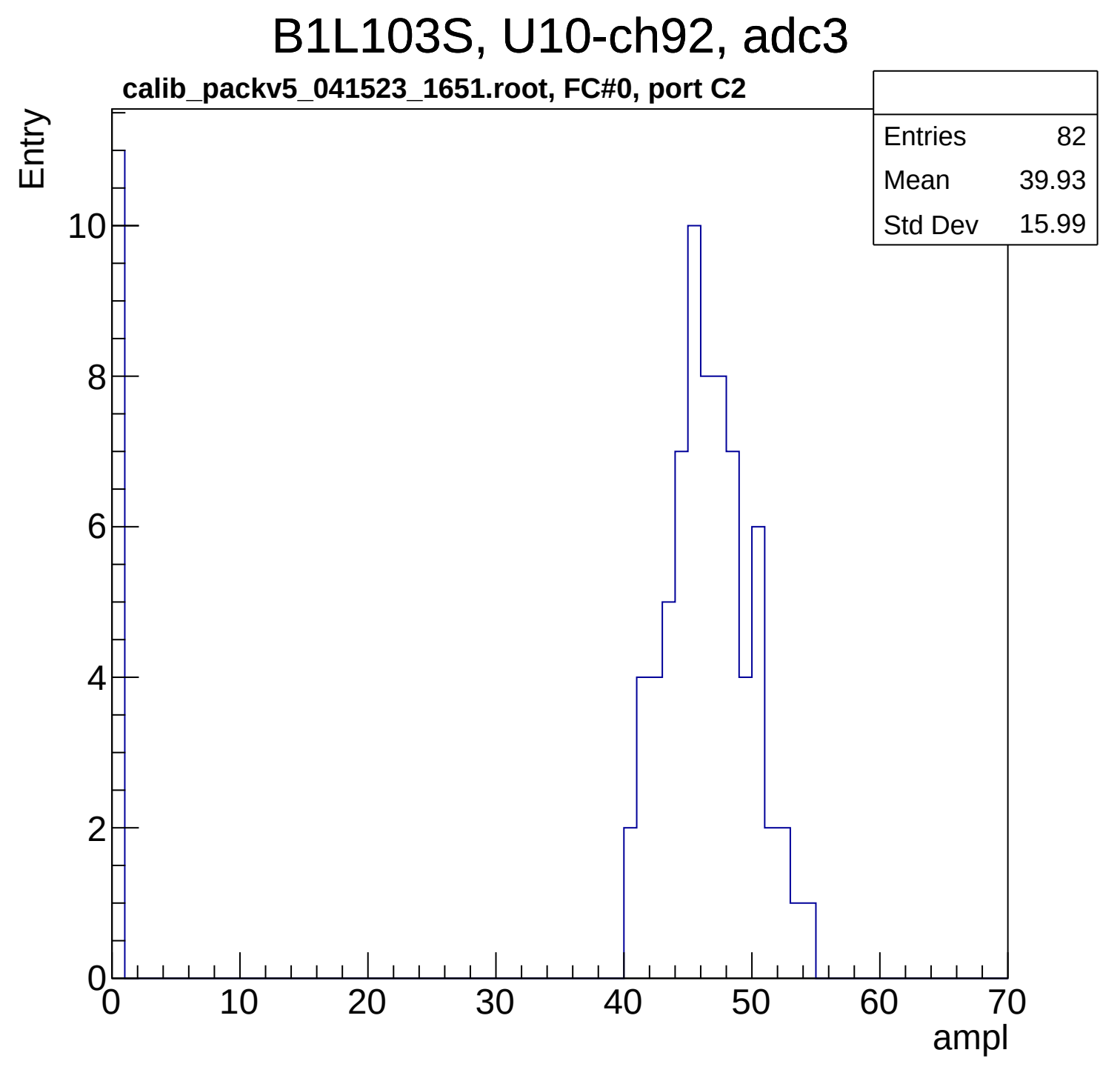
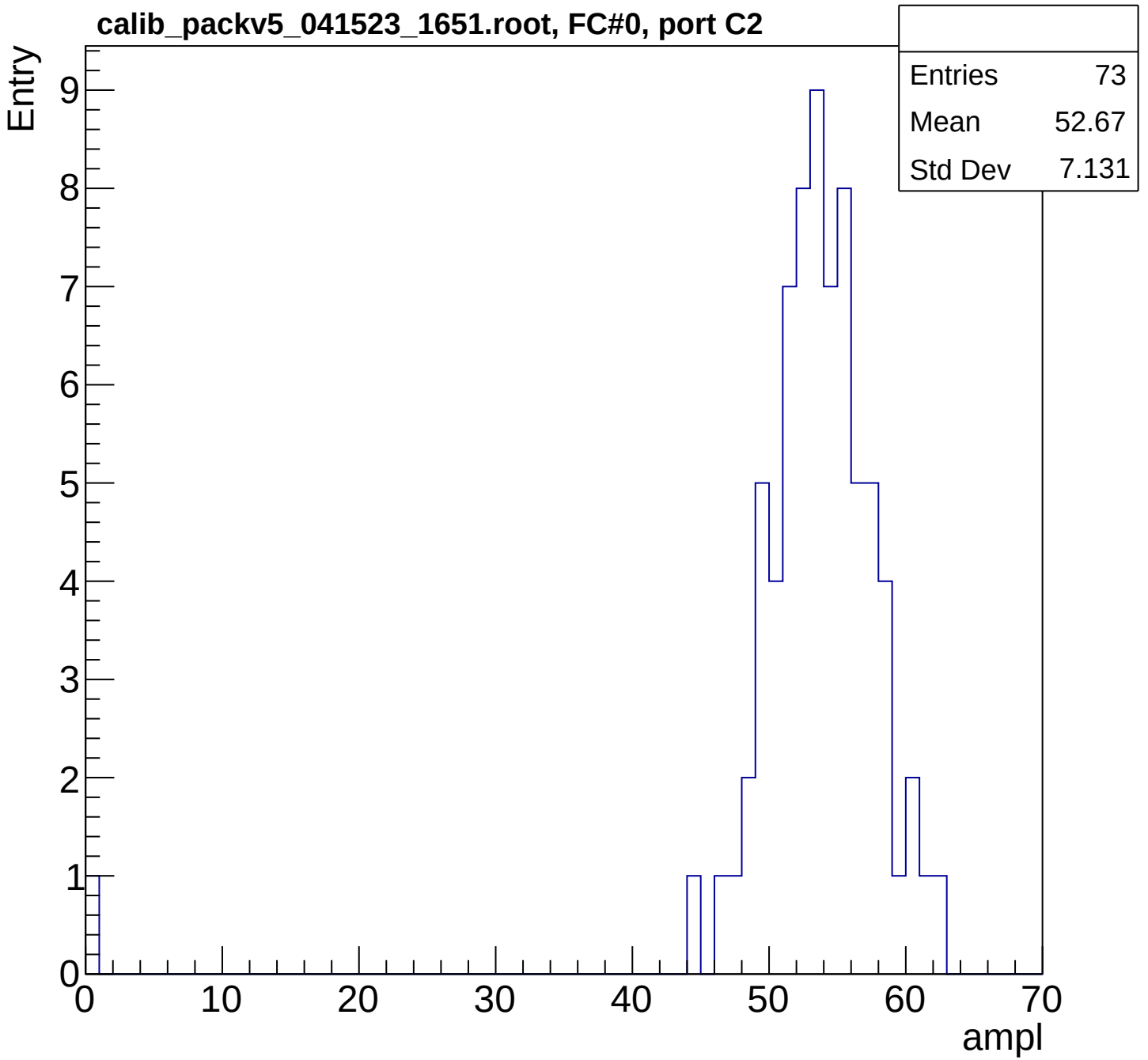
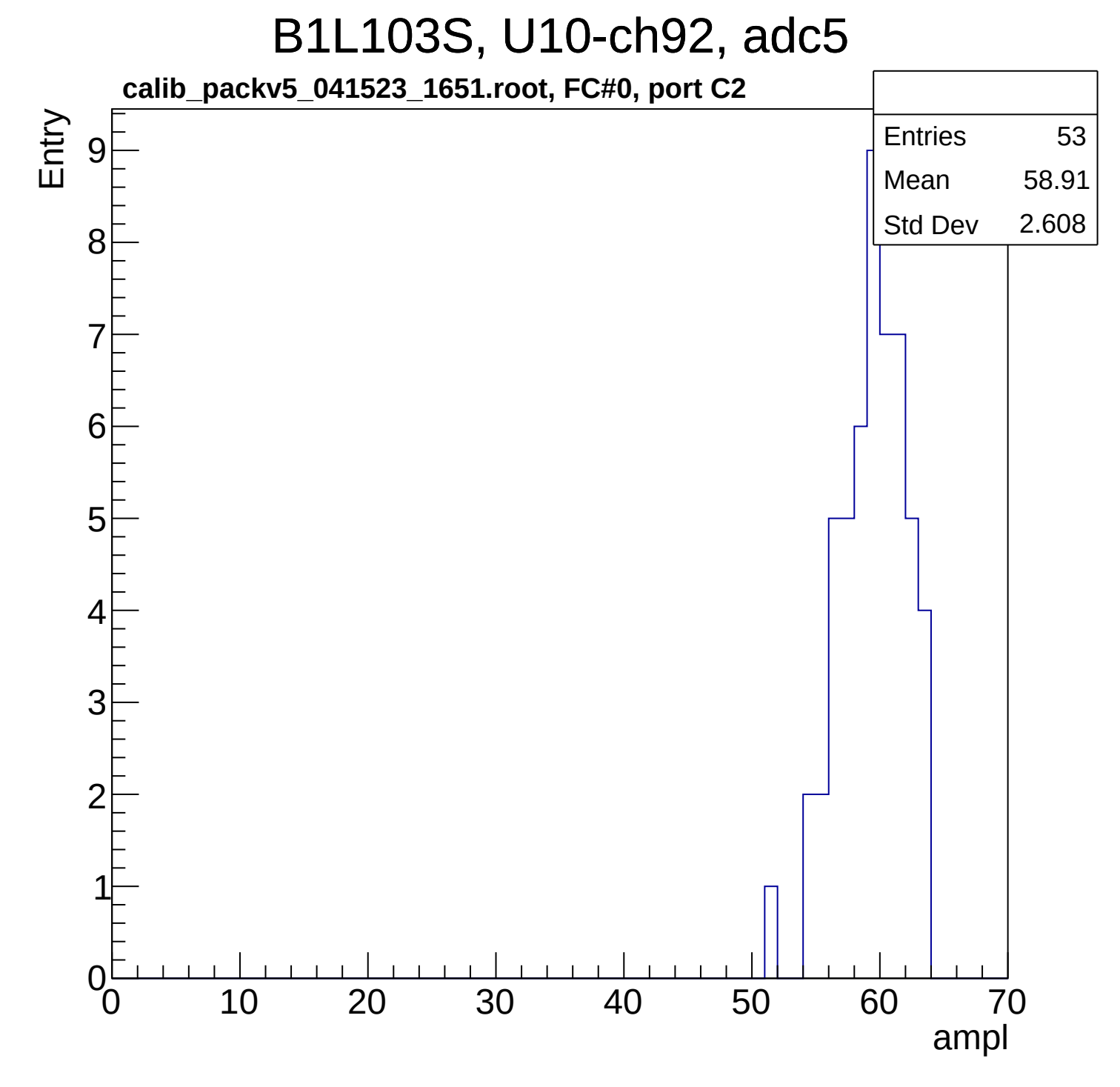
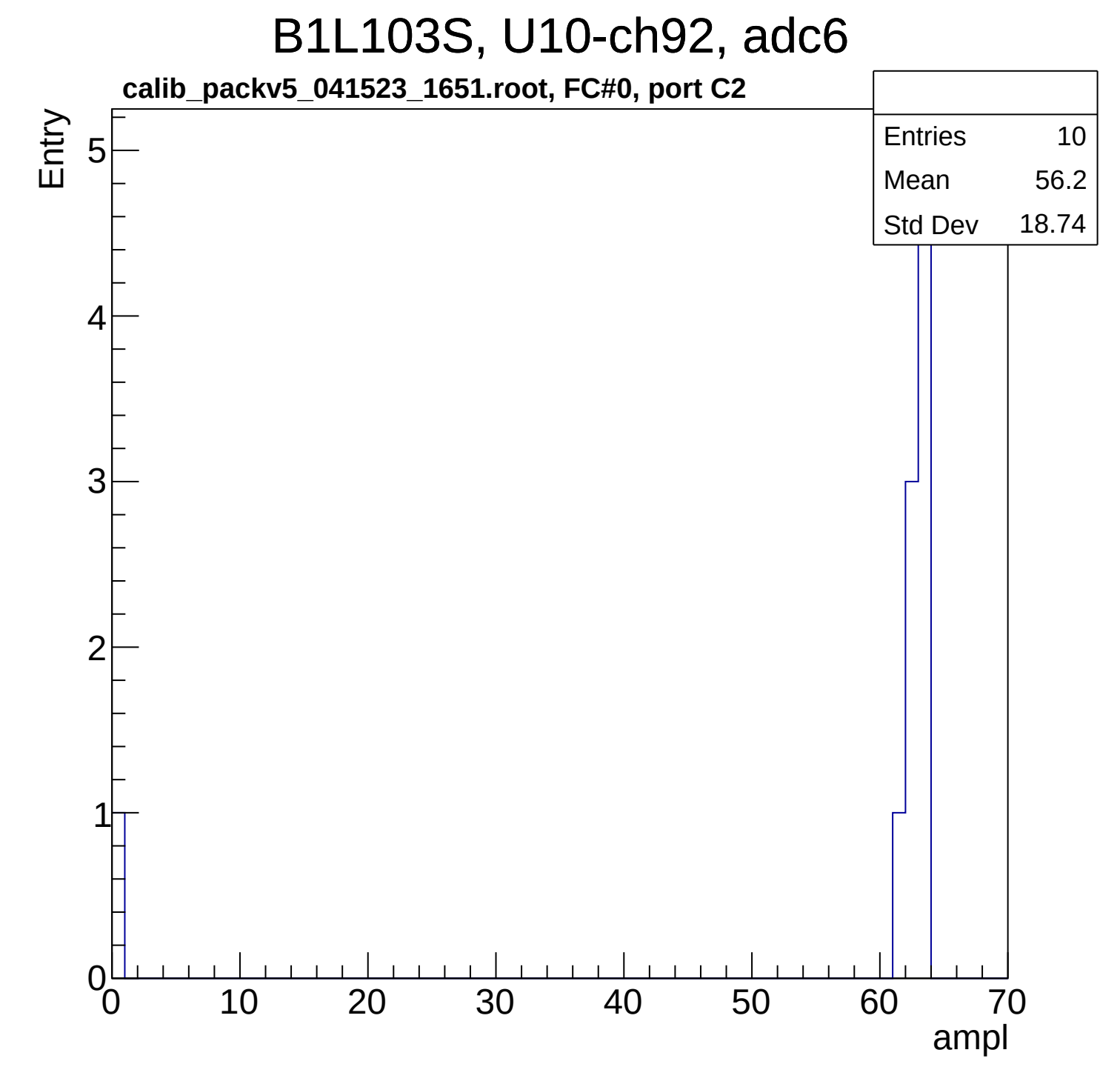
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

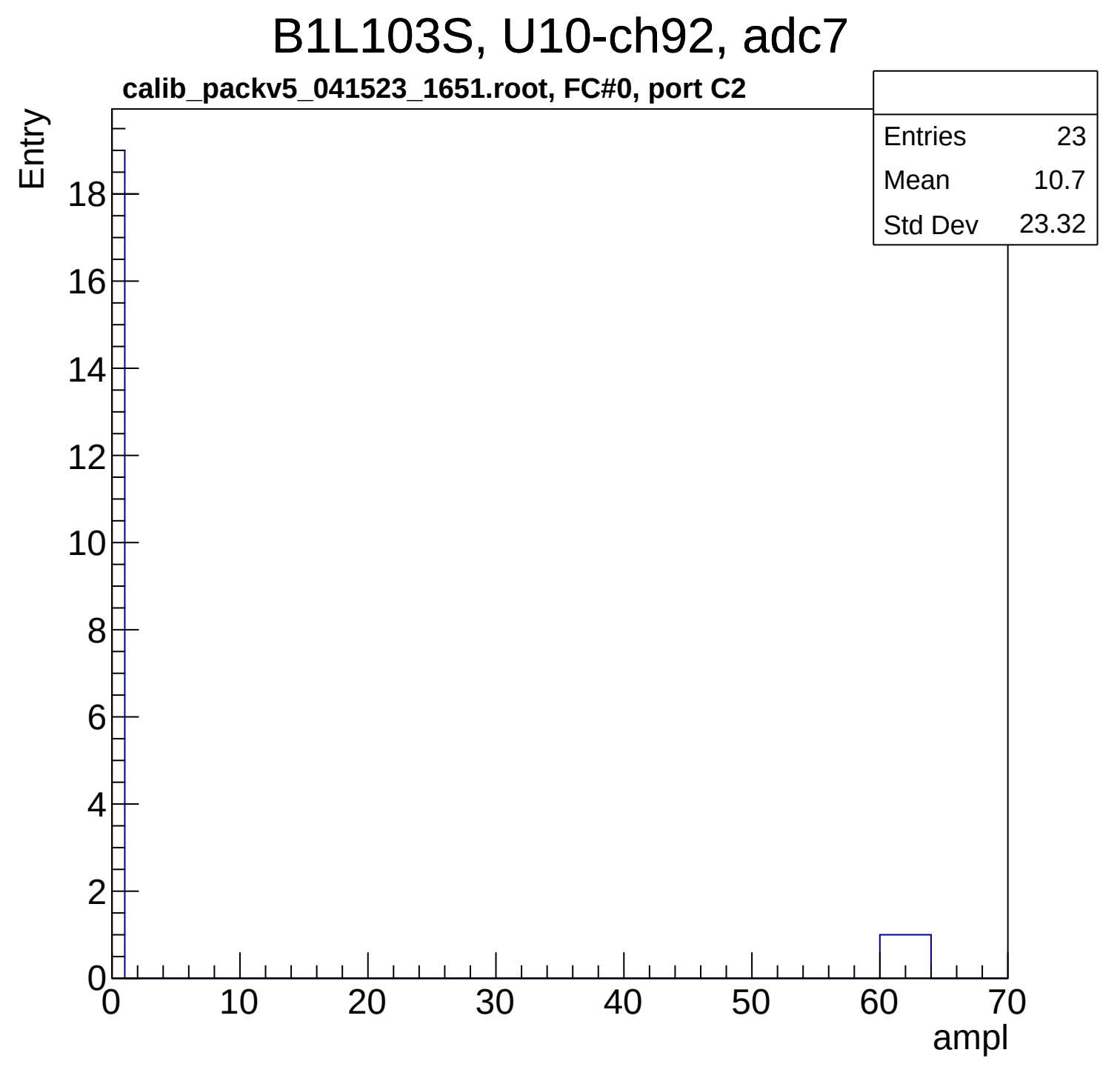

B1L103S, U10-ch92, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 37.77
Std Dev 9.487
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

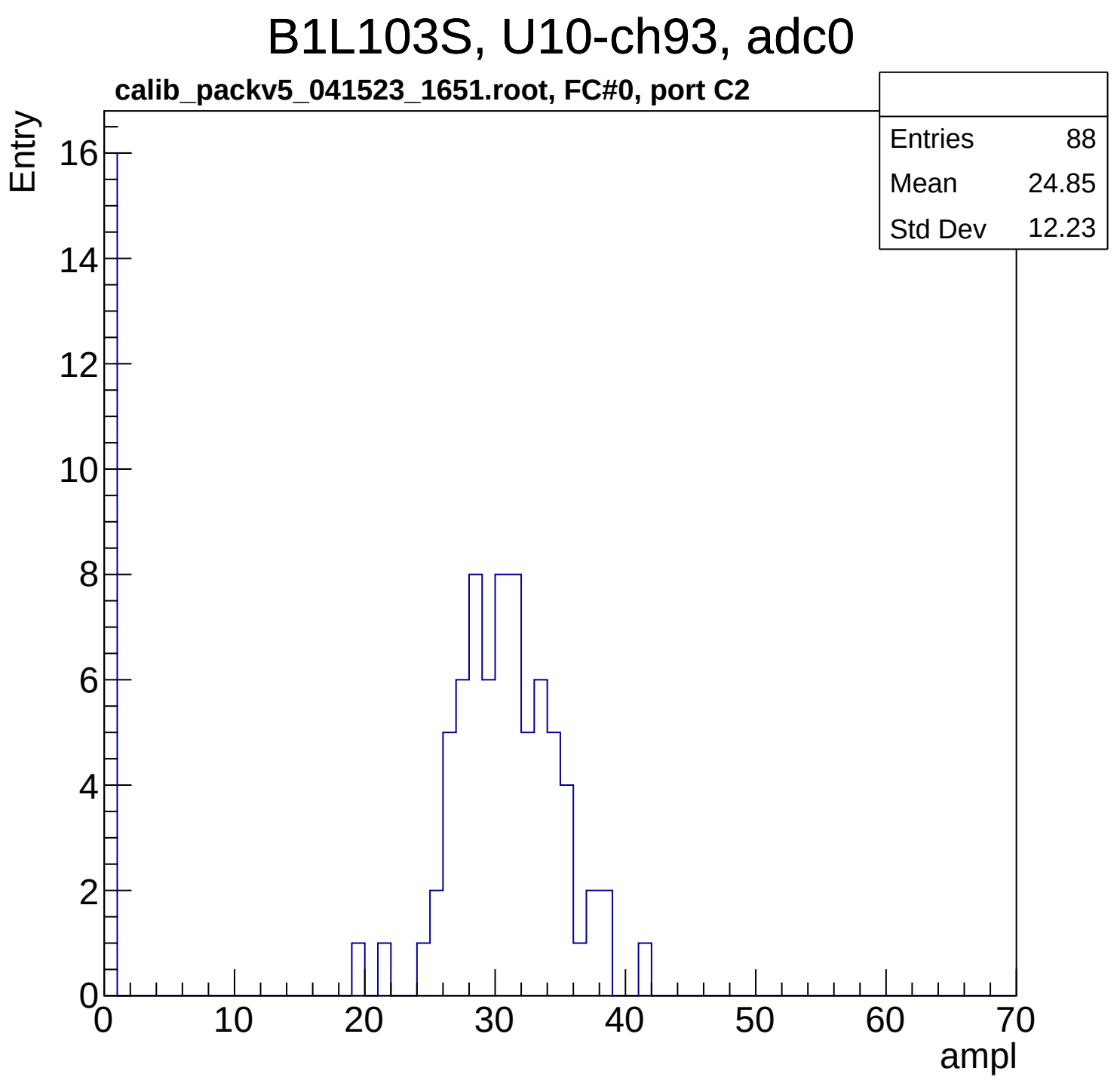

B1L103S, U10-ch92, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 39.93
Std Dev 15.99
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch92, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 52.67
Std Dev 7.131
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U10-ch92, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 58.91
Std Dev 2.608
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U10-ch92, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 56.2
Std Dev 18.74
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch92, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 23
Mean 10.7
Std Dev 23.32
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch93, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 88
Mean 24.85
Std Dev 12.23
Entry
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2
4
6
8
10
12
14
16
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10
20
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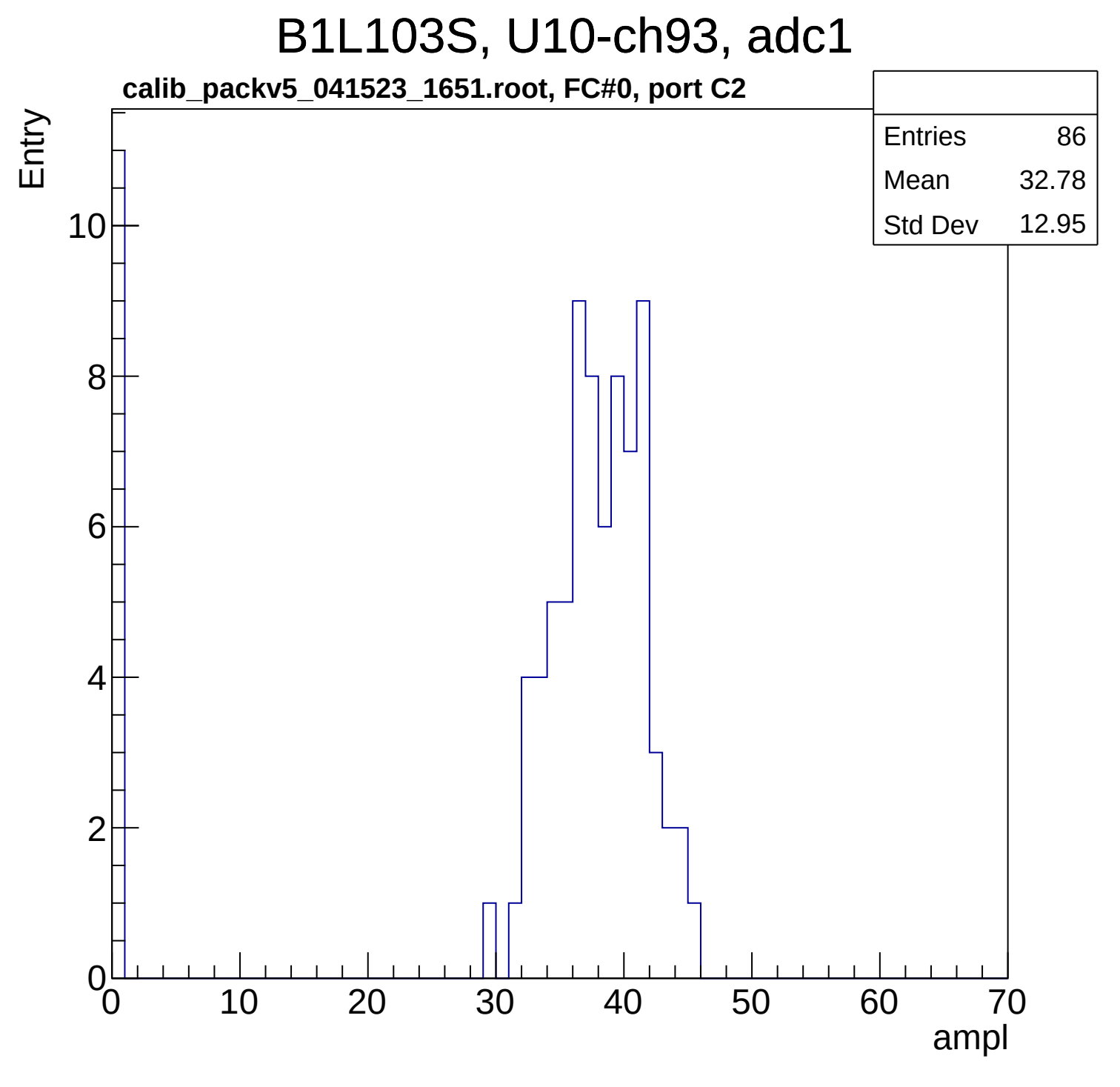
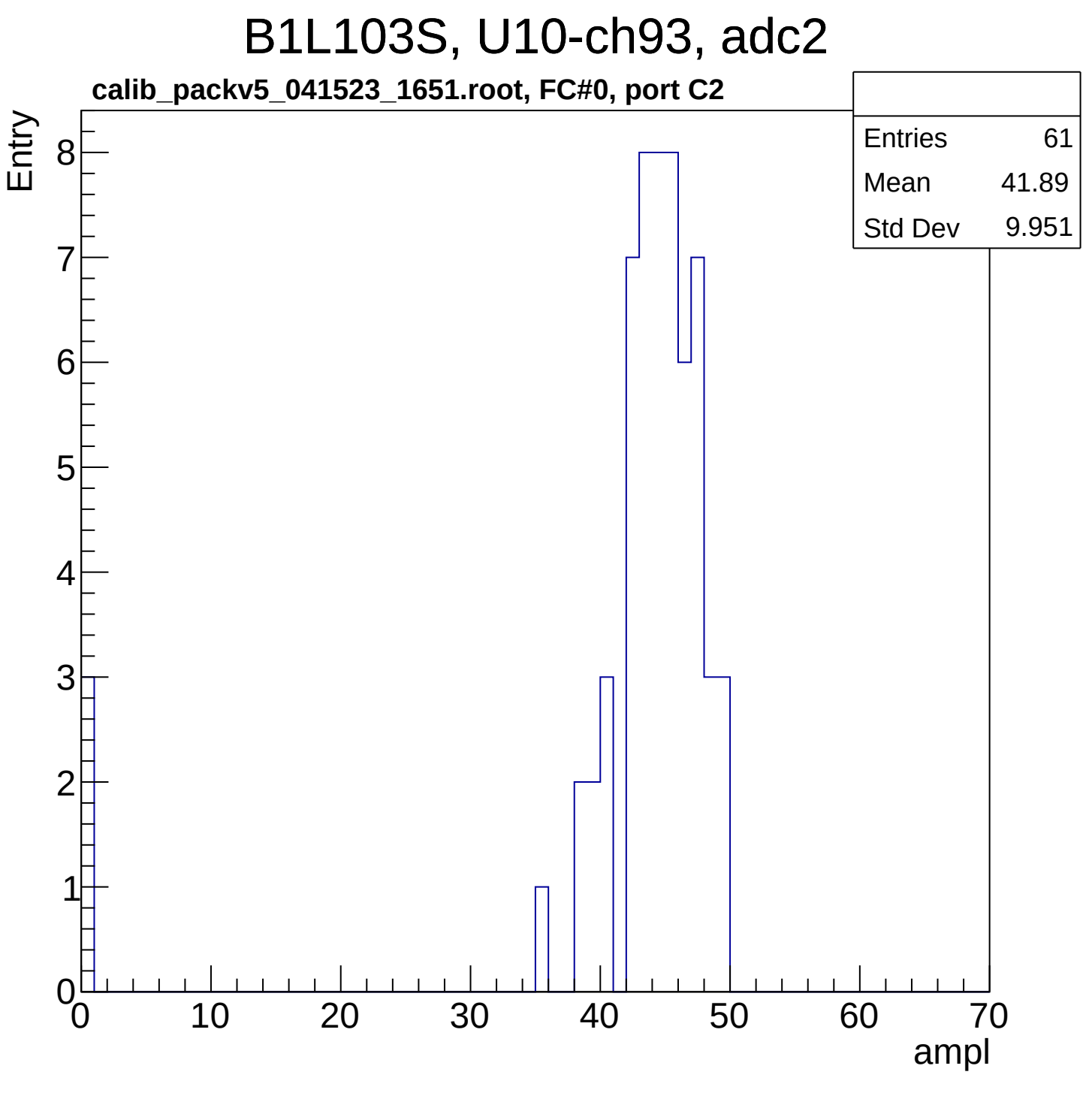
50
60
70
ampl


B1L103S, U10-ch93, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 32.78
Std Dev 12.95
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U10-ch93, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 41.89
Std Dev 9.951
Entry
ampl
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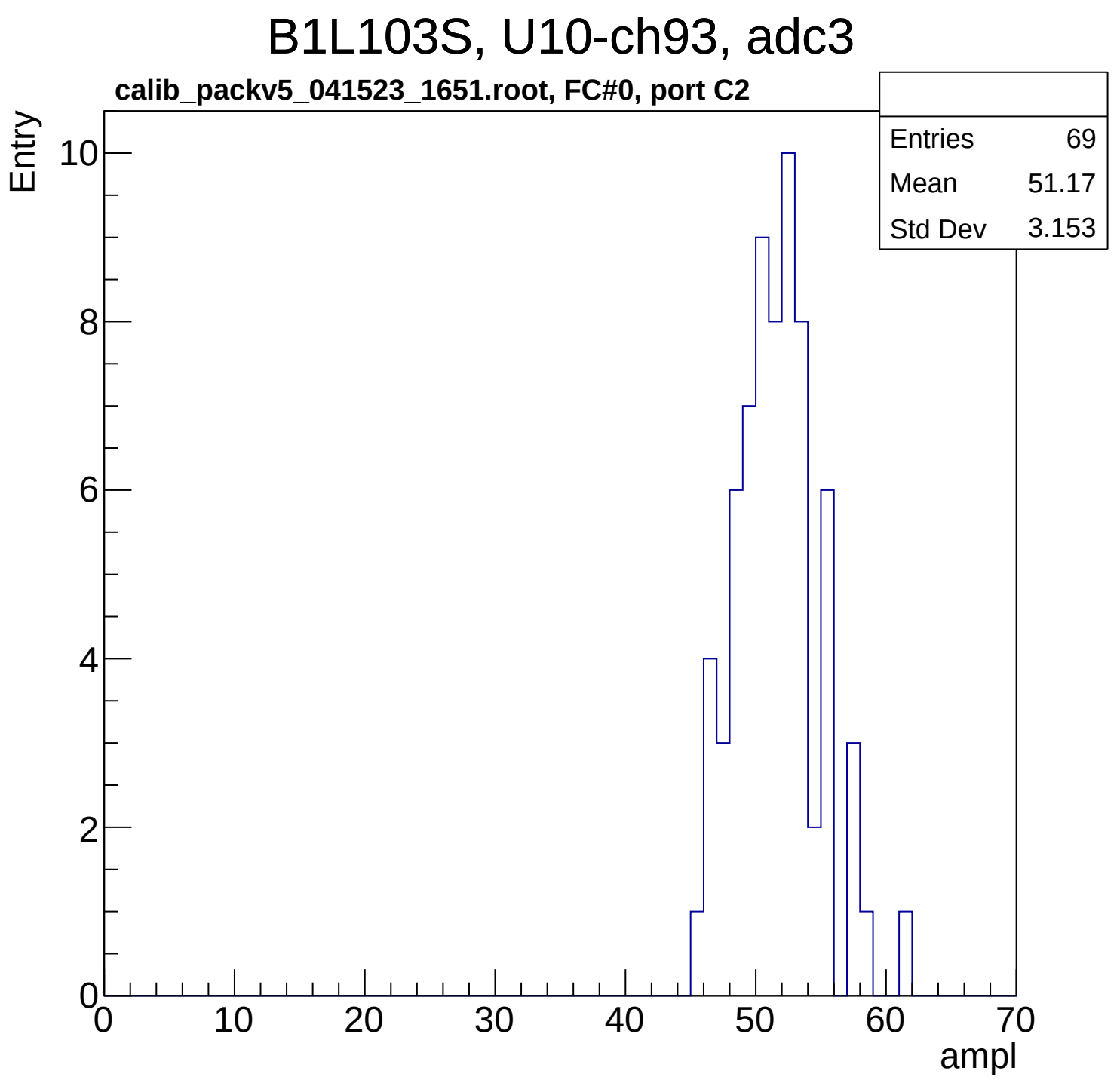
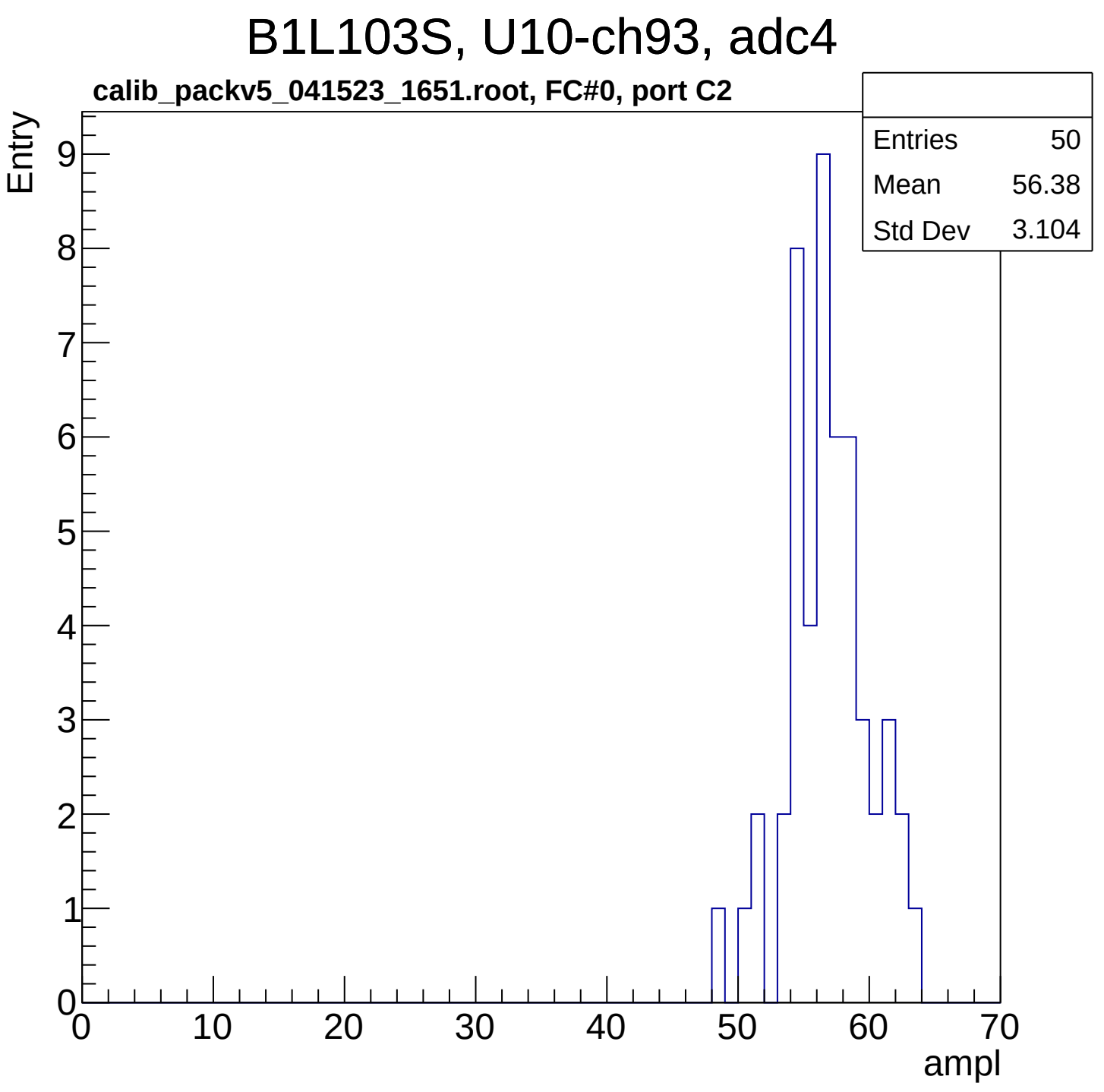
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U10-ch93, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 51.17
Std Dev 3.153
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U10-ch93, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 56.38
Std Dev 3.104
Entry
ampl
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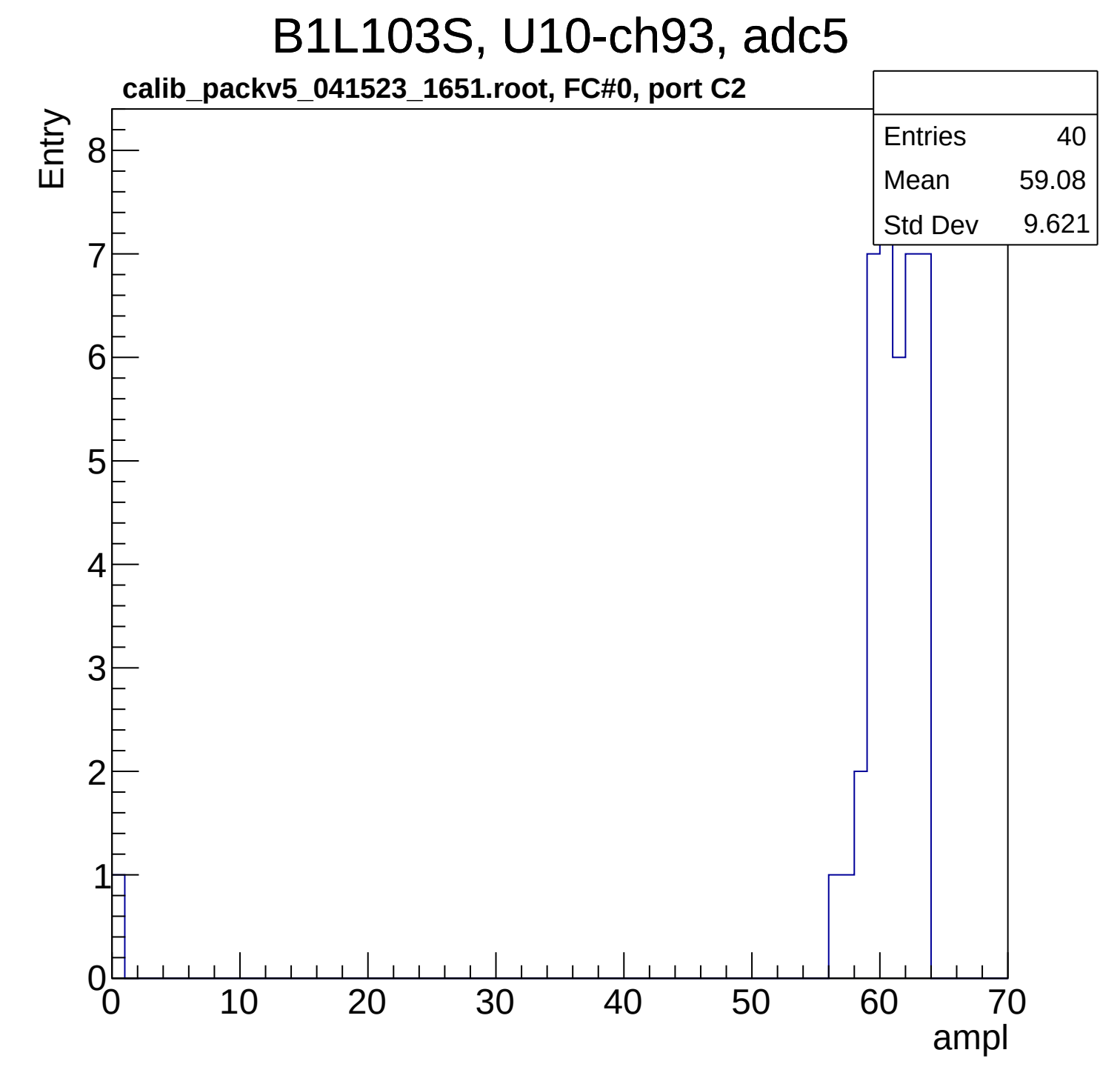
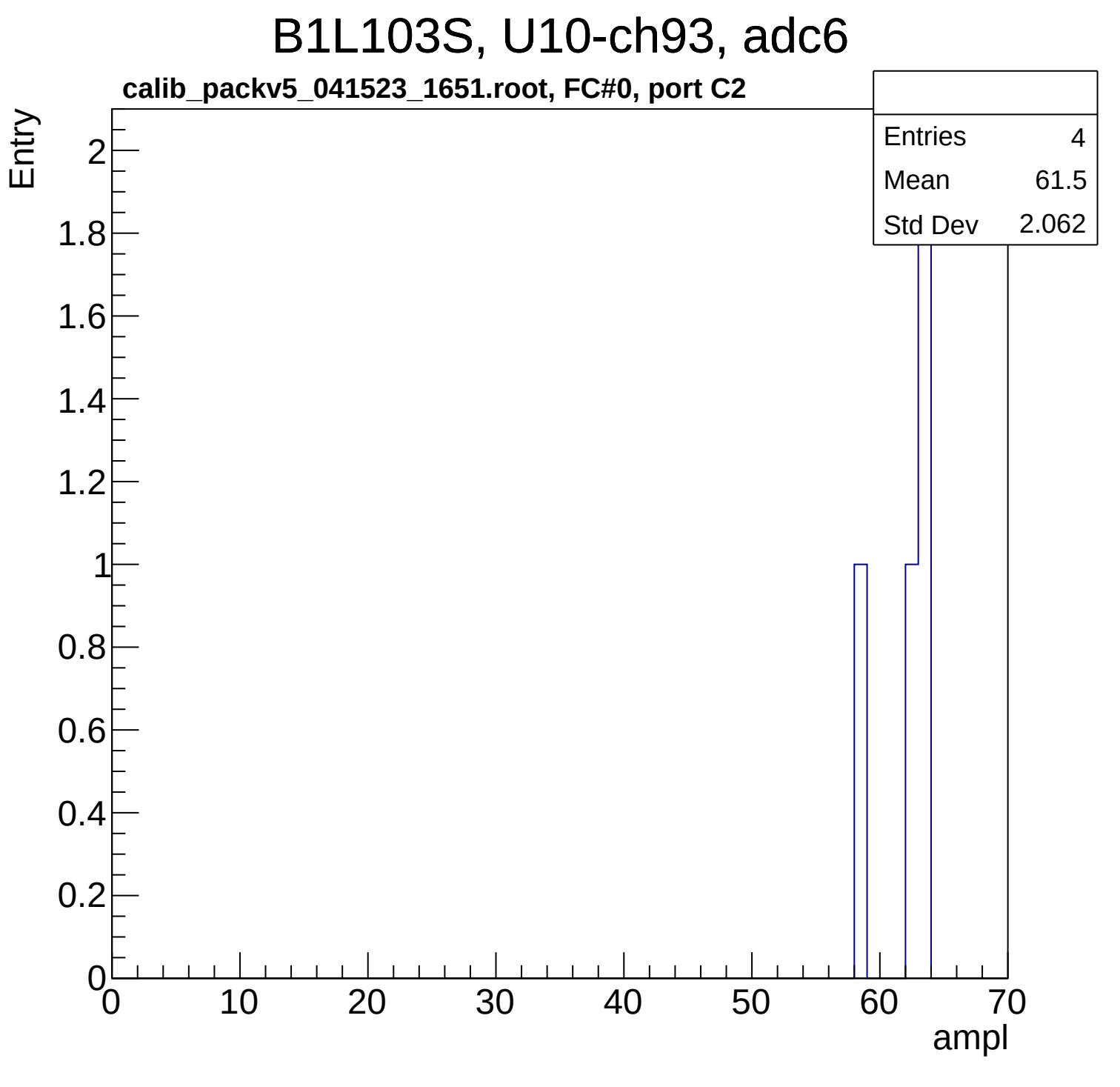
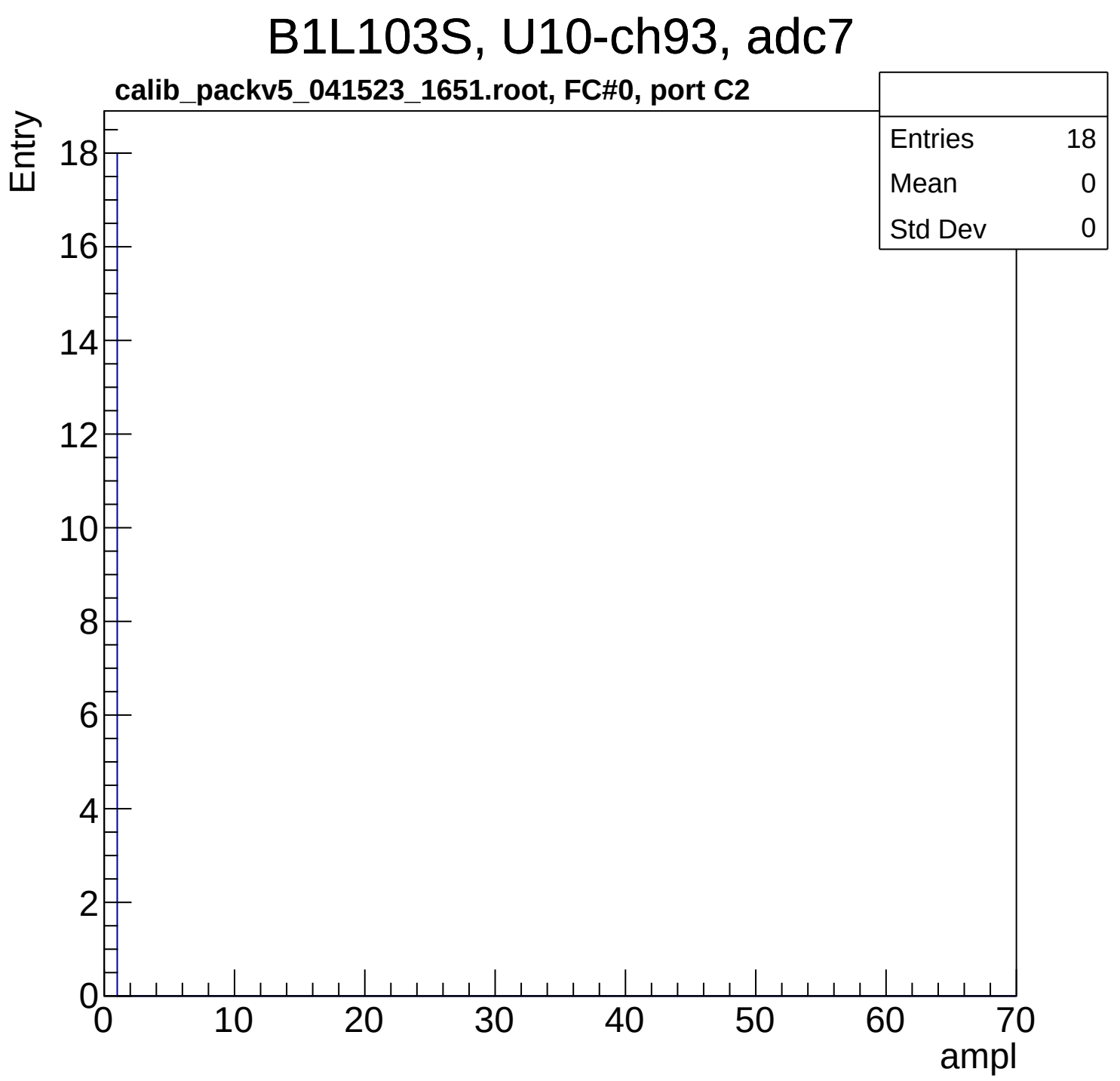
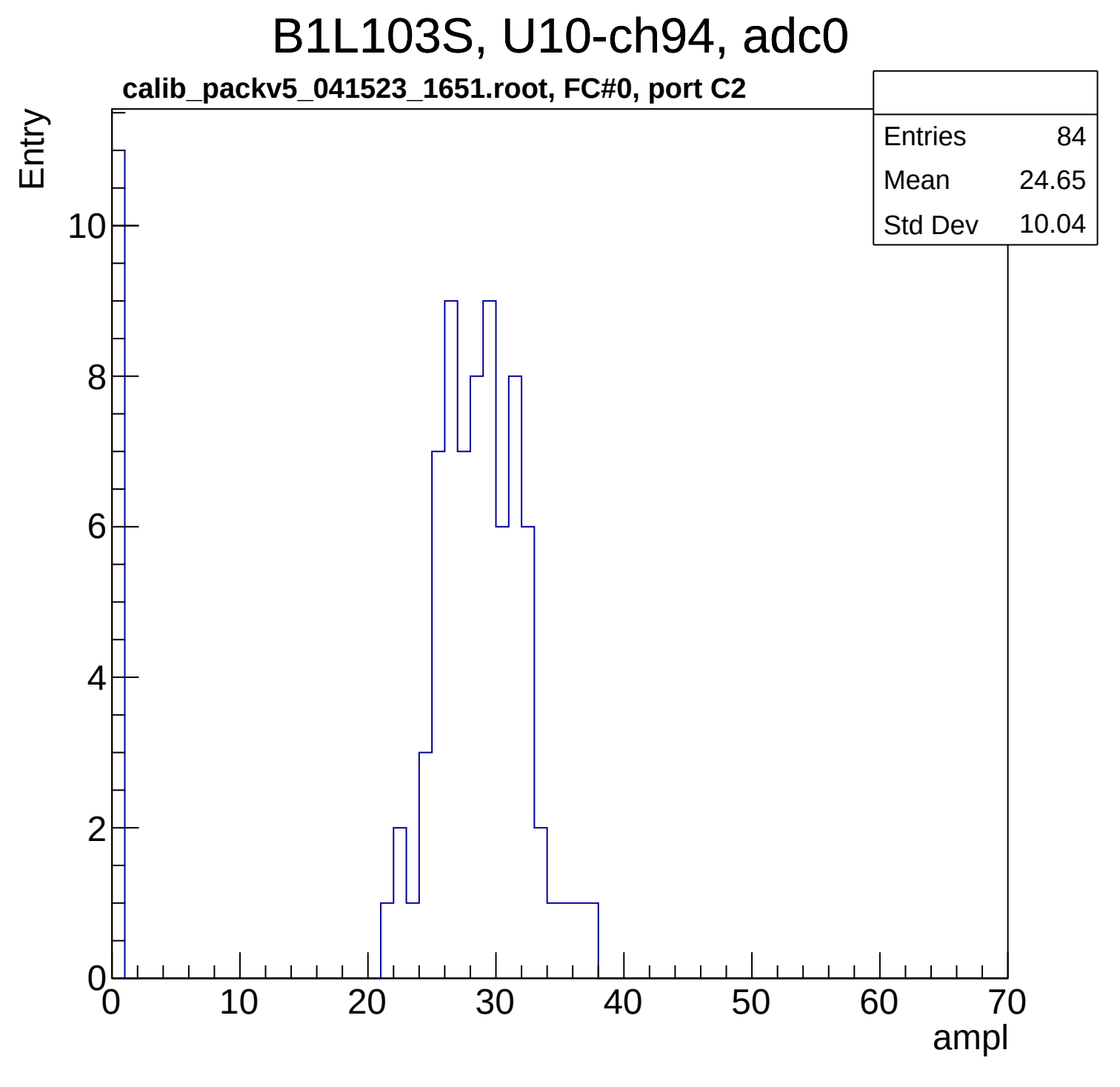
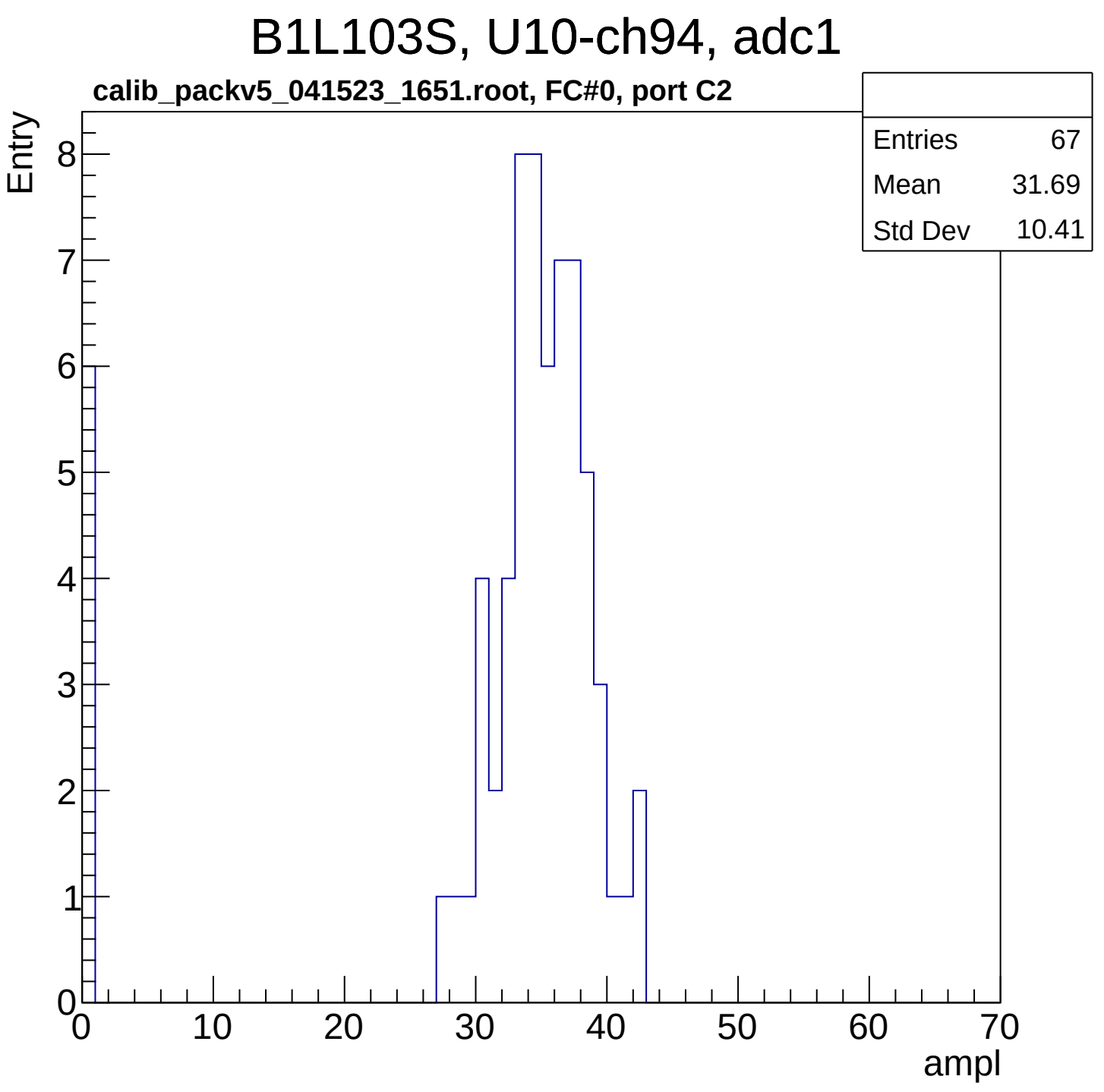
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

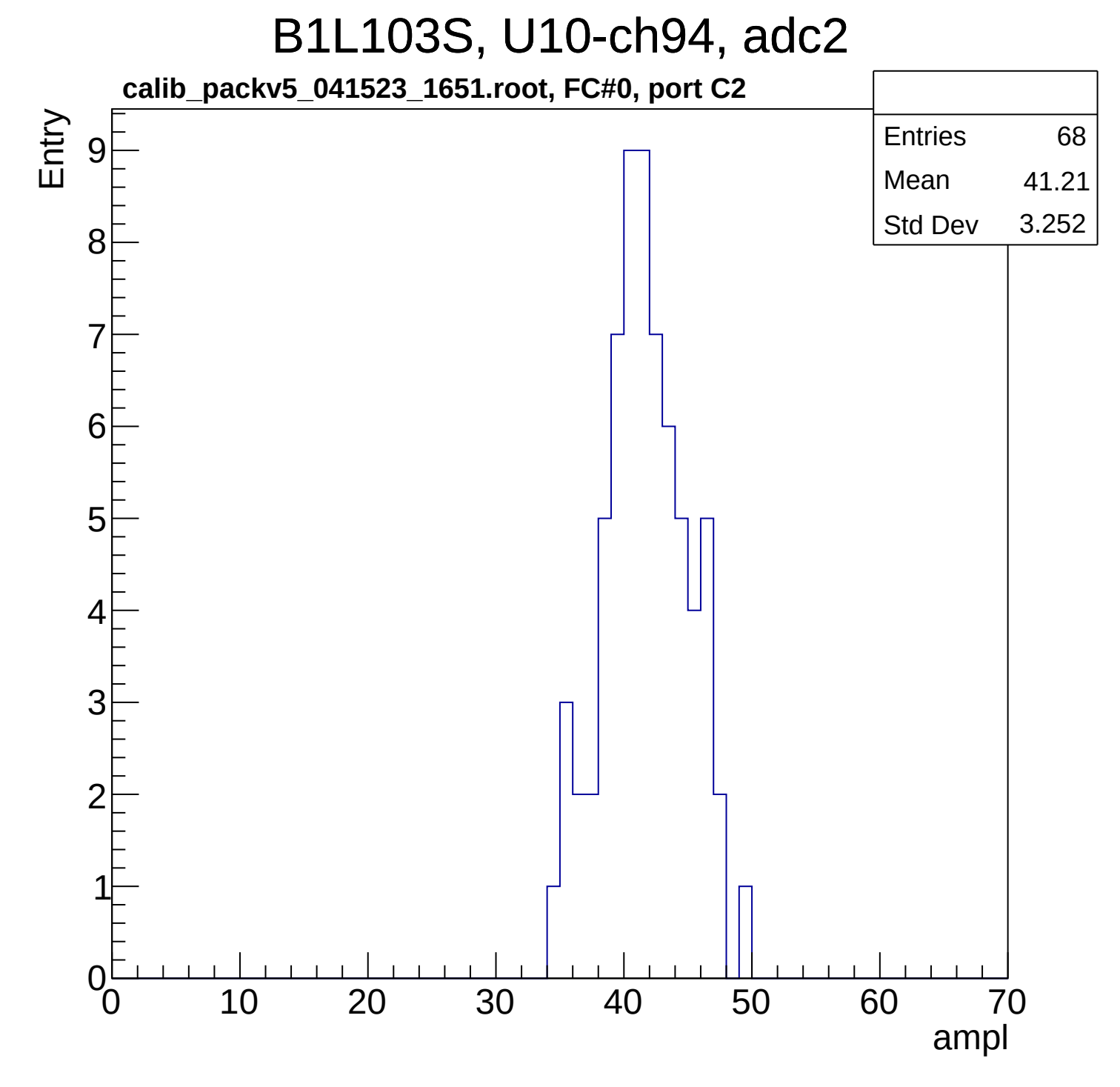

B1L103S, U10-ch93, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 40
Mean 59.08
Std Dev 9.621
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

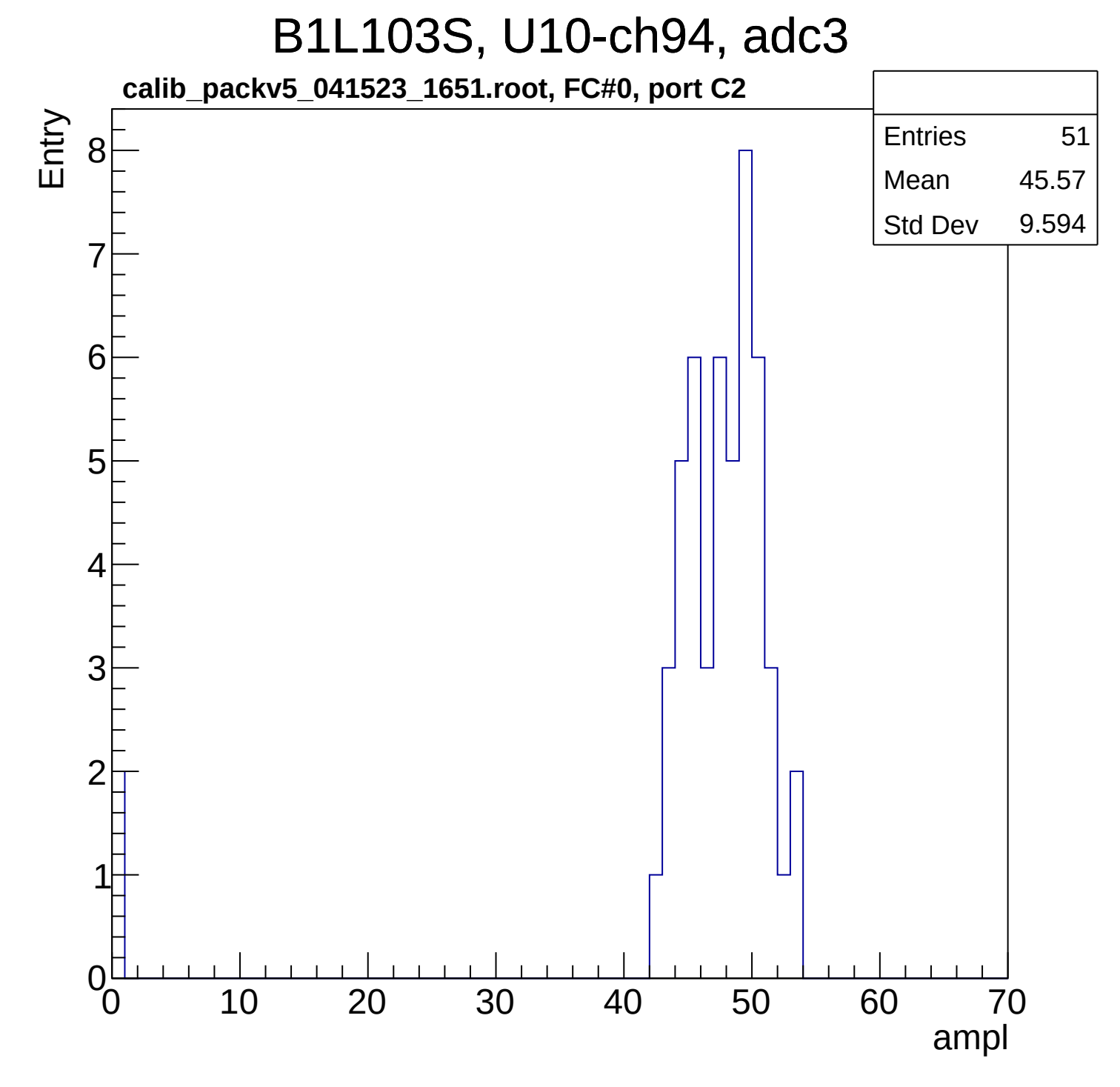

B1L103S, U10-ch93, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 4
Mean 61.5
Std Dev 2.062
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U10-ch93, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch94, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 24.65
Std Dev 10.04
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch94, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 31.69
Std Dev 10.41
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U10-ch94, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 41.21
Std Dev 3.252
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U10-ch94, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 45.57
Std Dev 9.594
Entry
ampl
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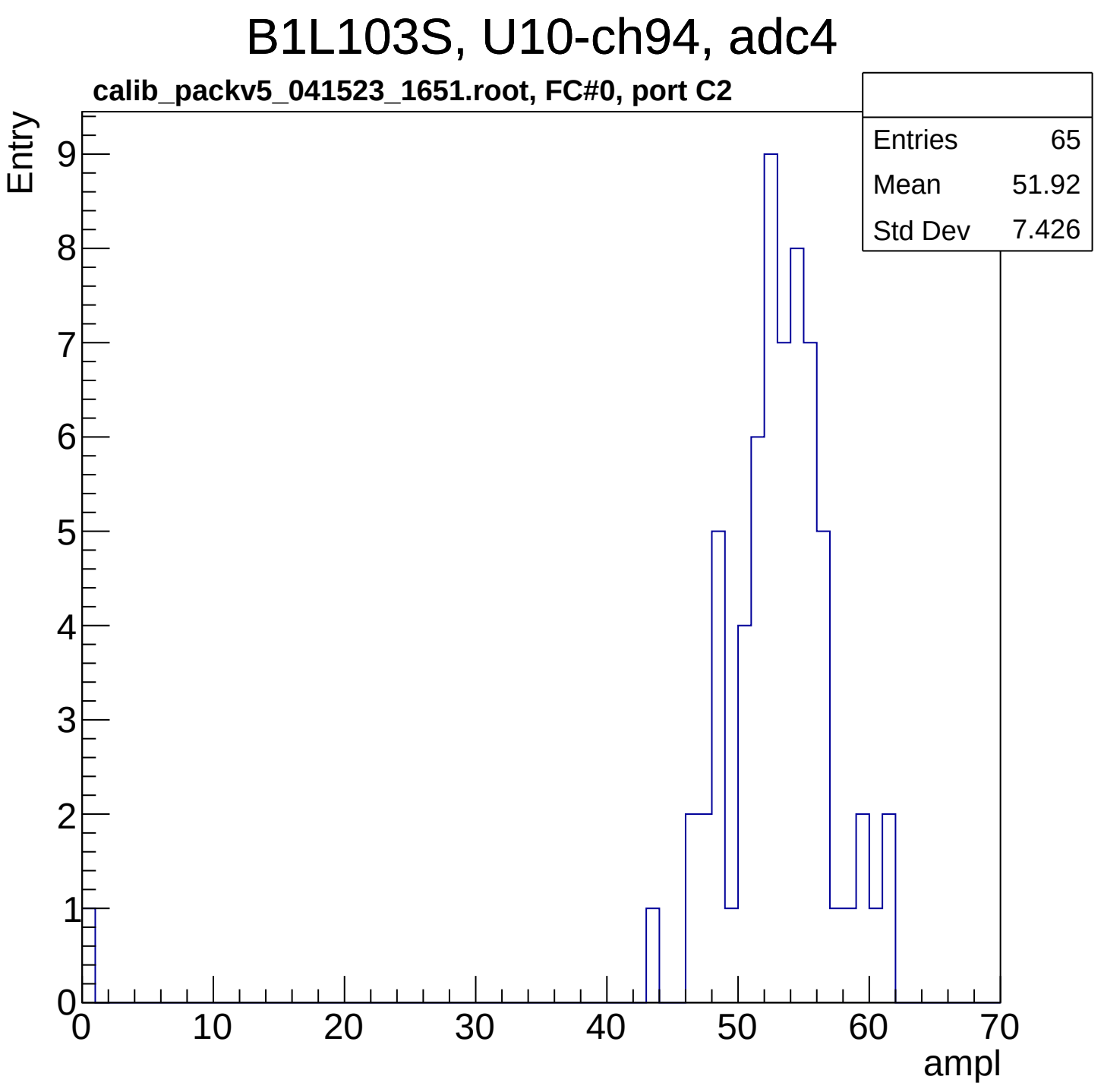
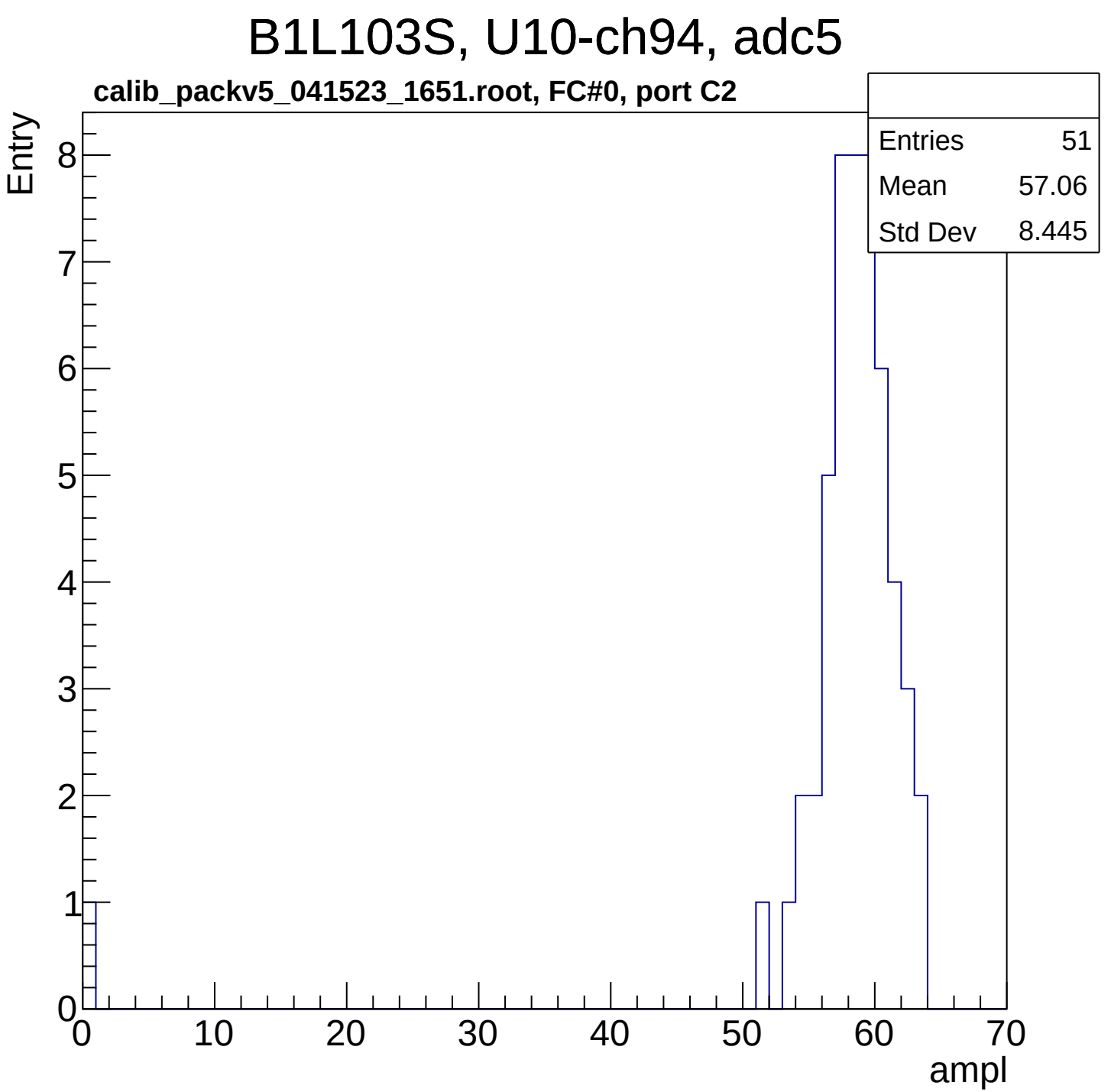
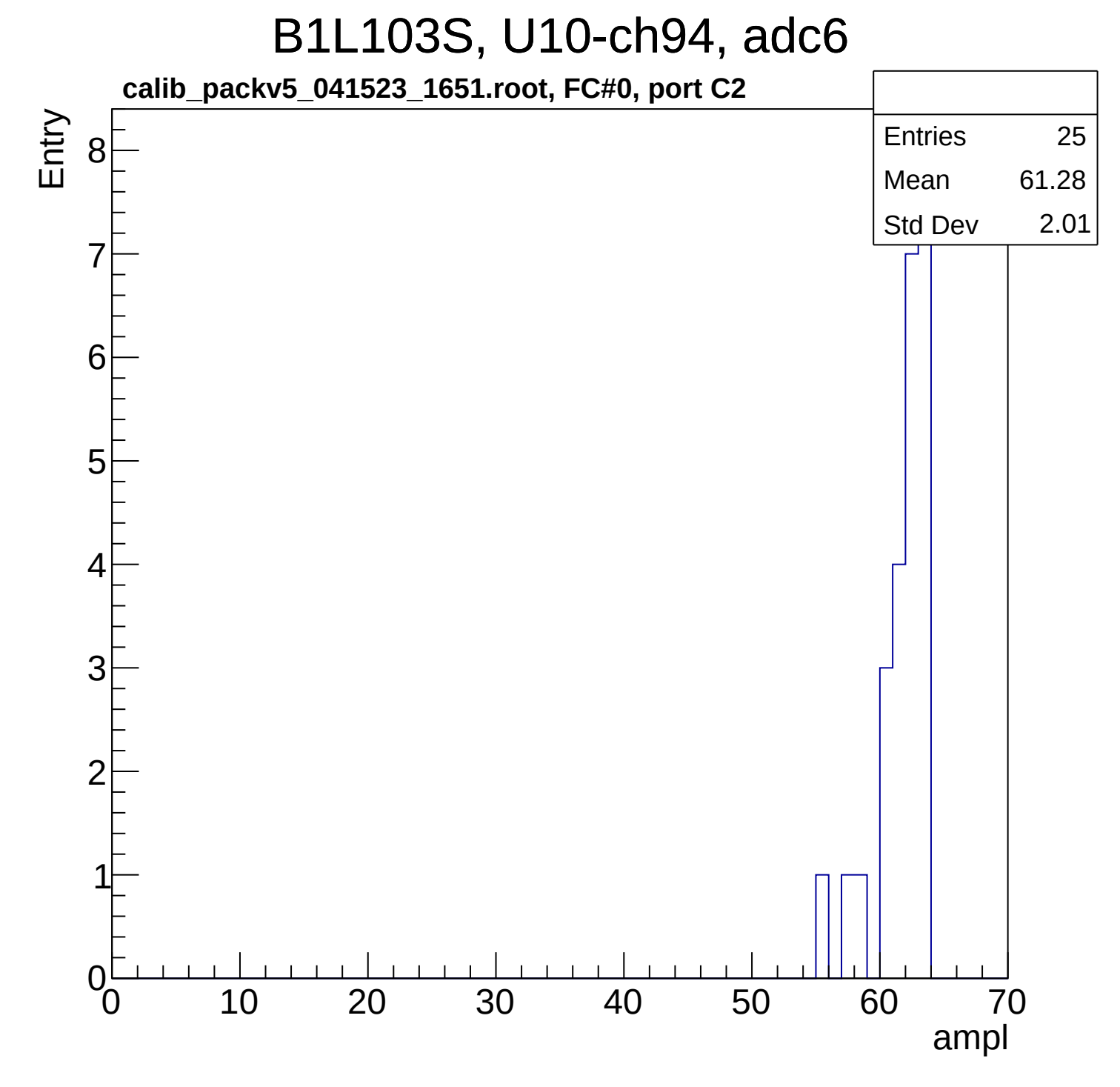
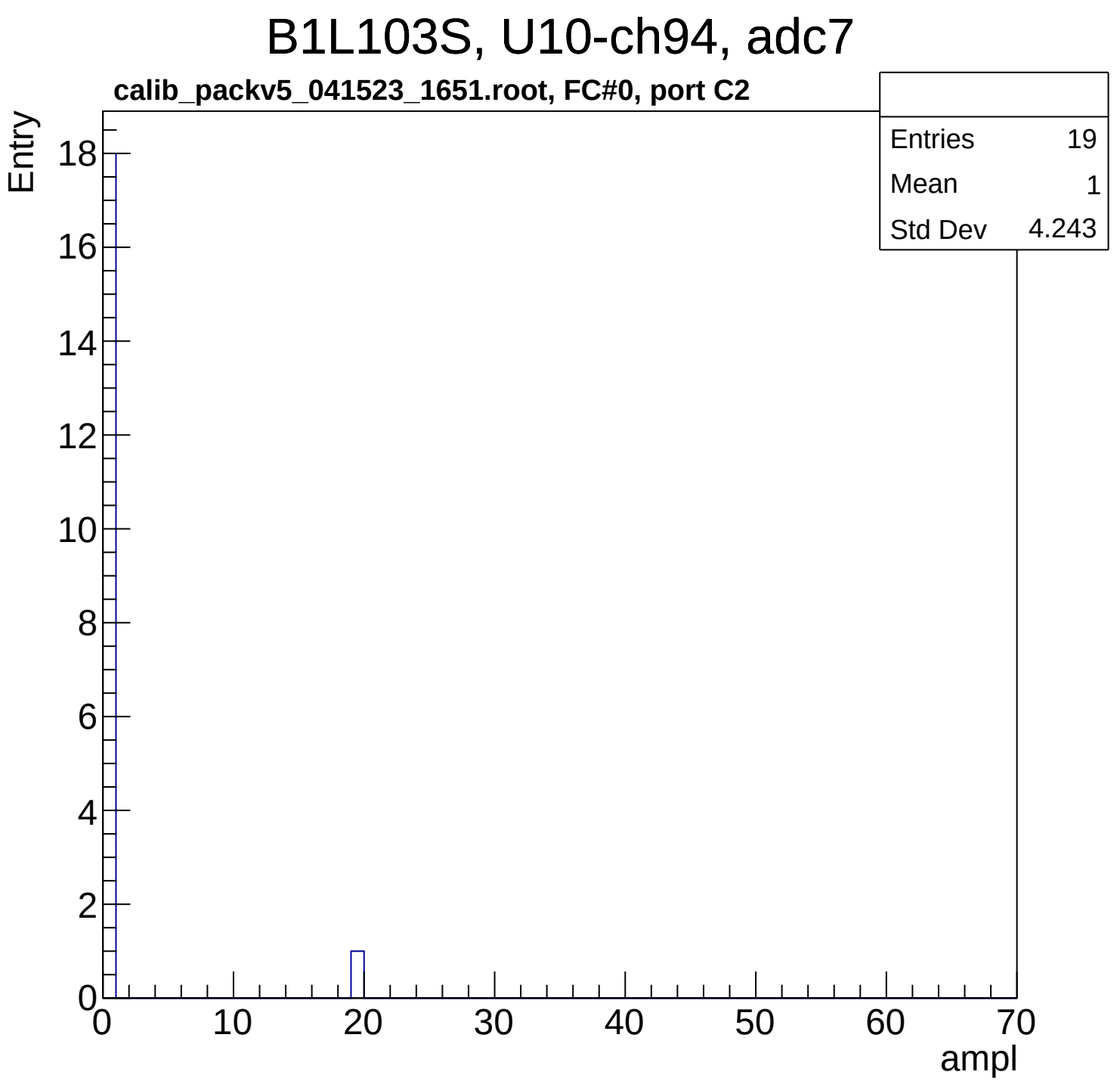
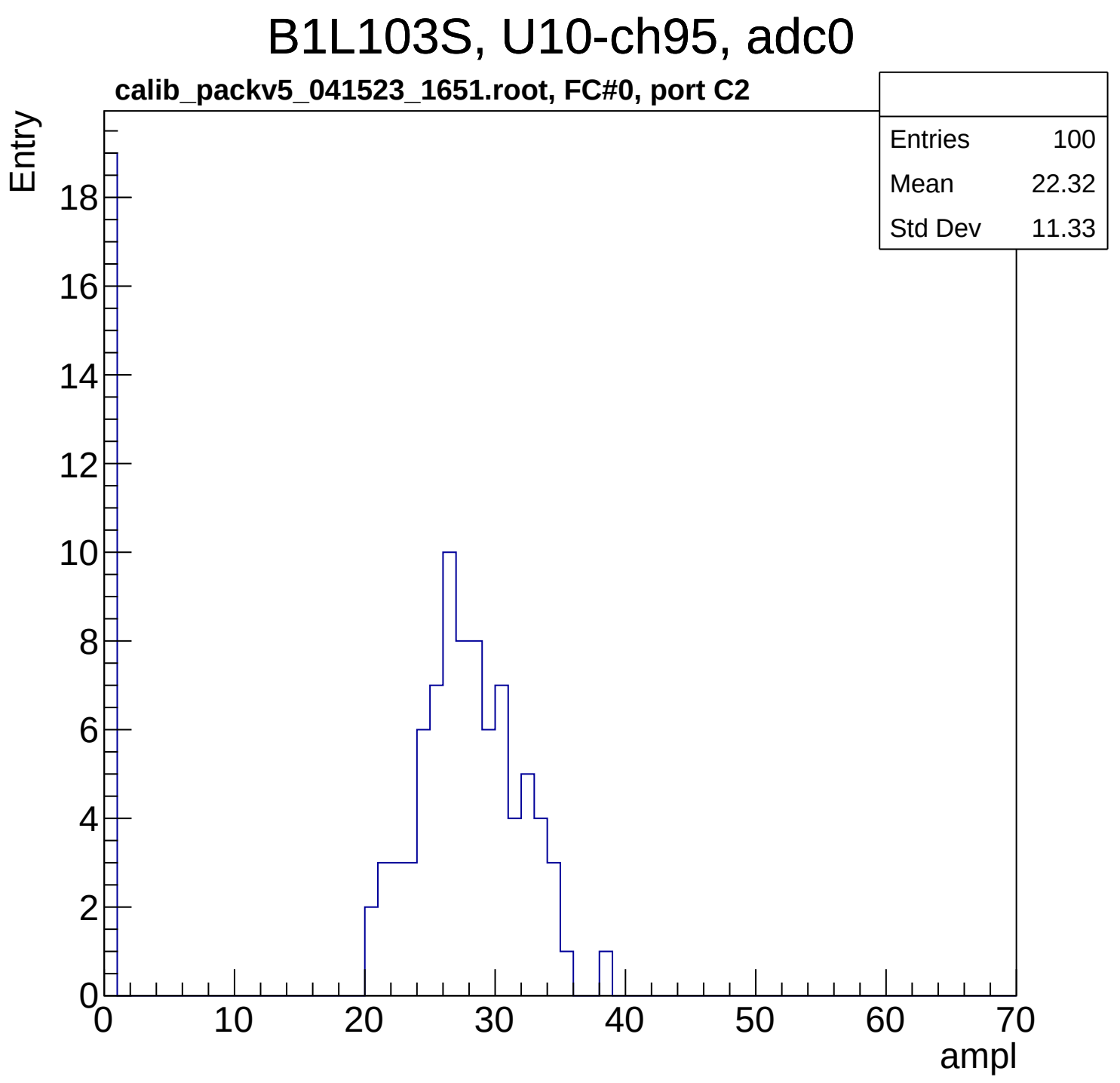
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

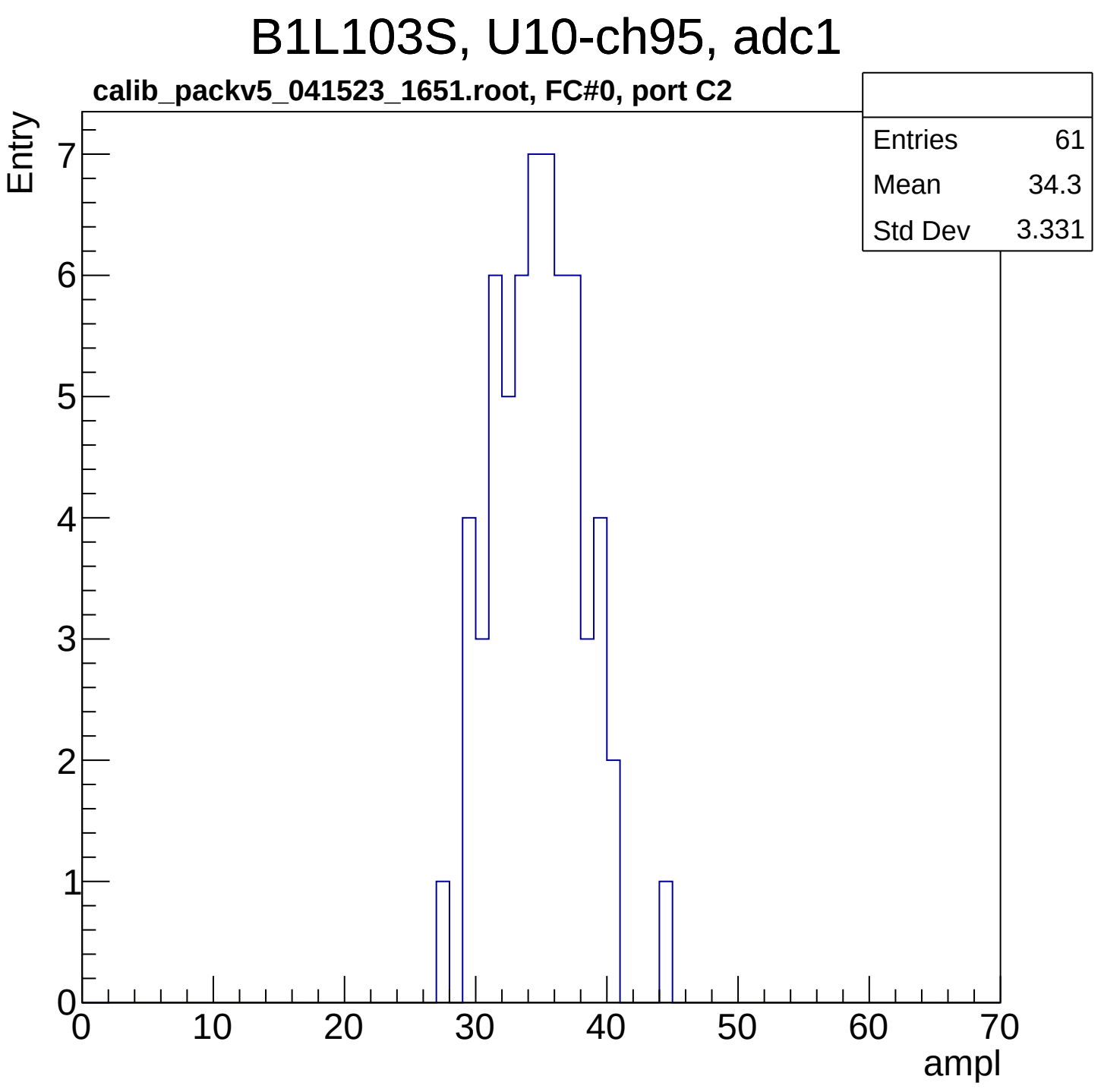

B1L103S, U10-ch94, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 51.92
Std Dev 7.426
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

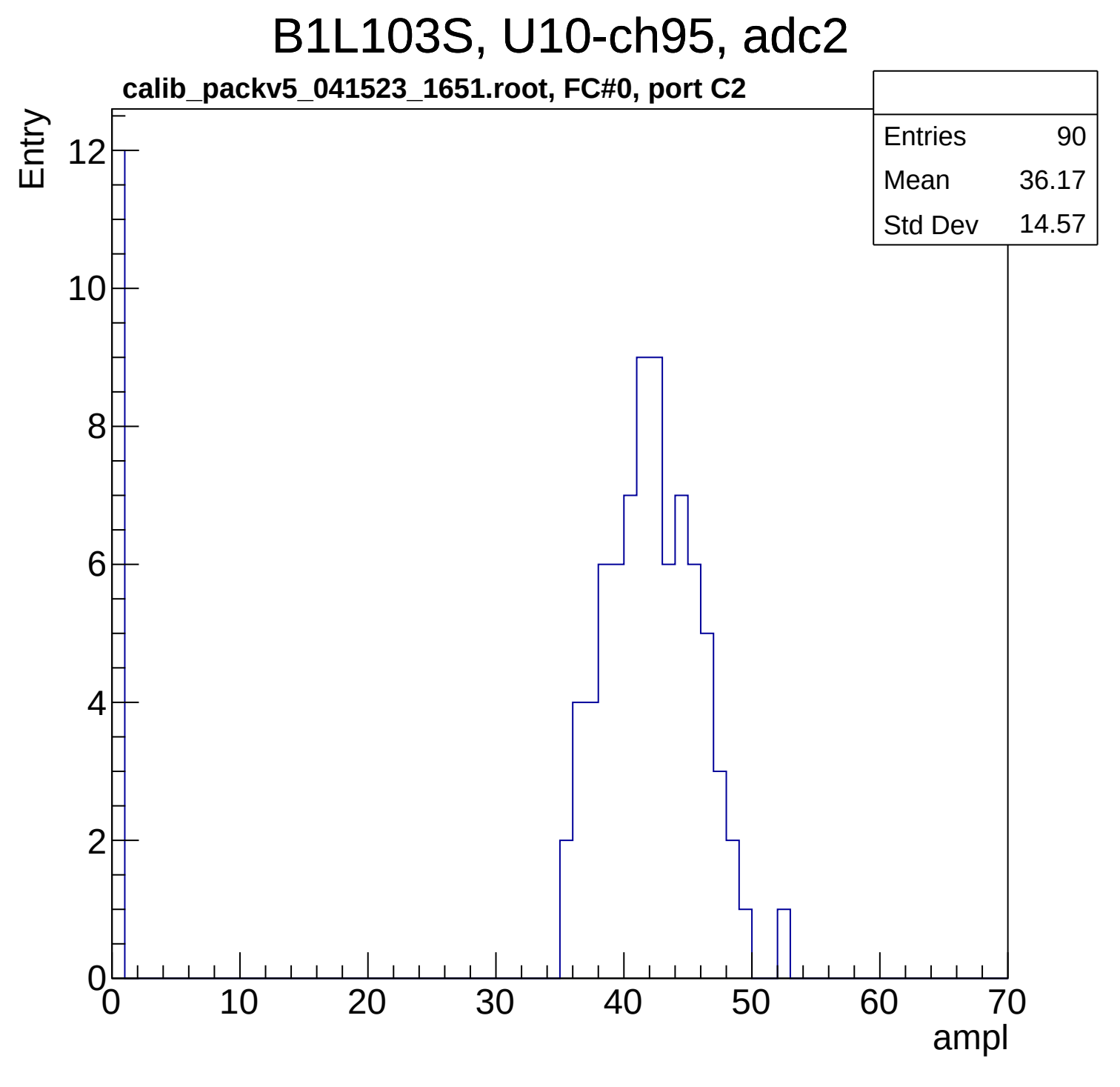

B1L103S, U10-ch94, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 57.06
Std Dev 8.445
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

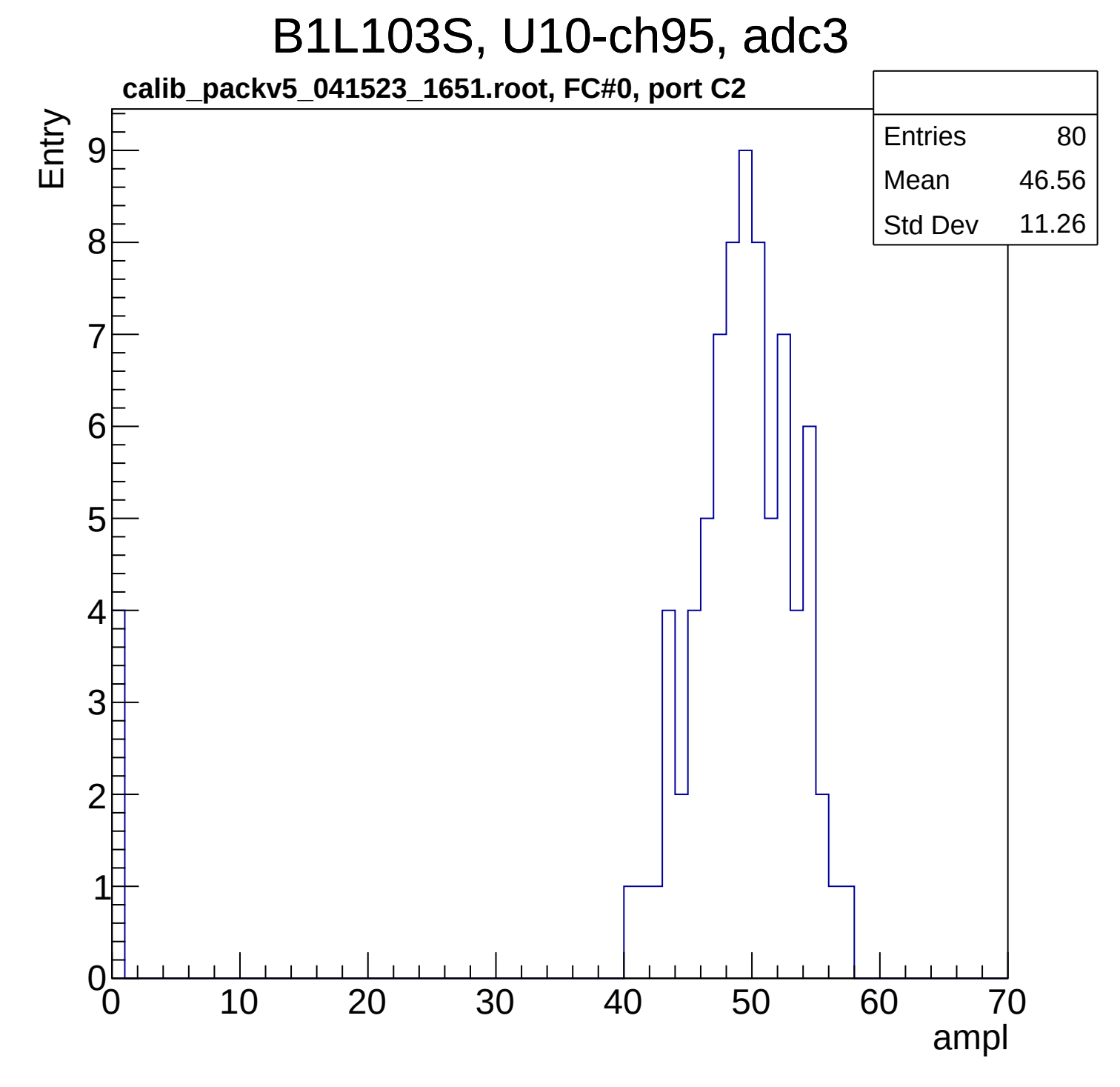

B1L103S, U10-ch94, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 25
Mean 61.28
Std Dev 2.01
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U10-ch94, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1
Std Dev 4.243
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch95, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 100
Mean 22.32
Std Dev 11.33
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch95, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 34.3
Std Dev 3.331
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U10-ch95, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 90
Mean 36.17
Std Dev 14.57
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch95, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 46.56
Std Dev 11.26
Entry
ampl
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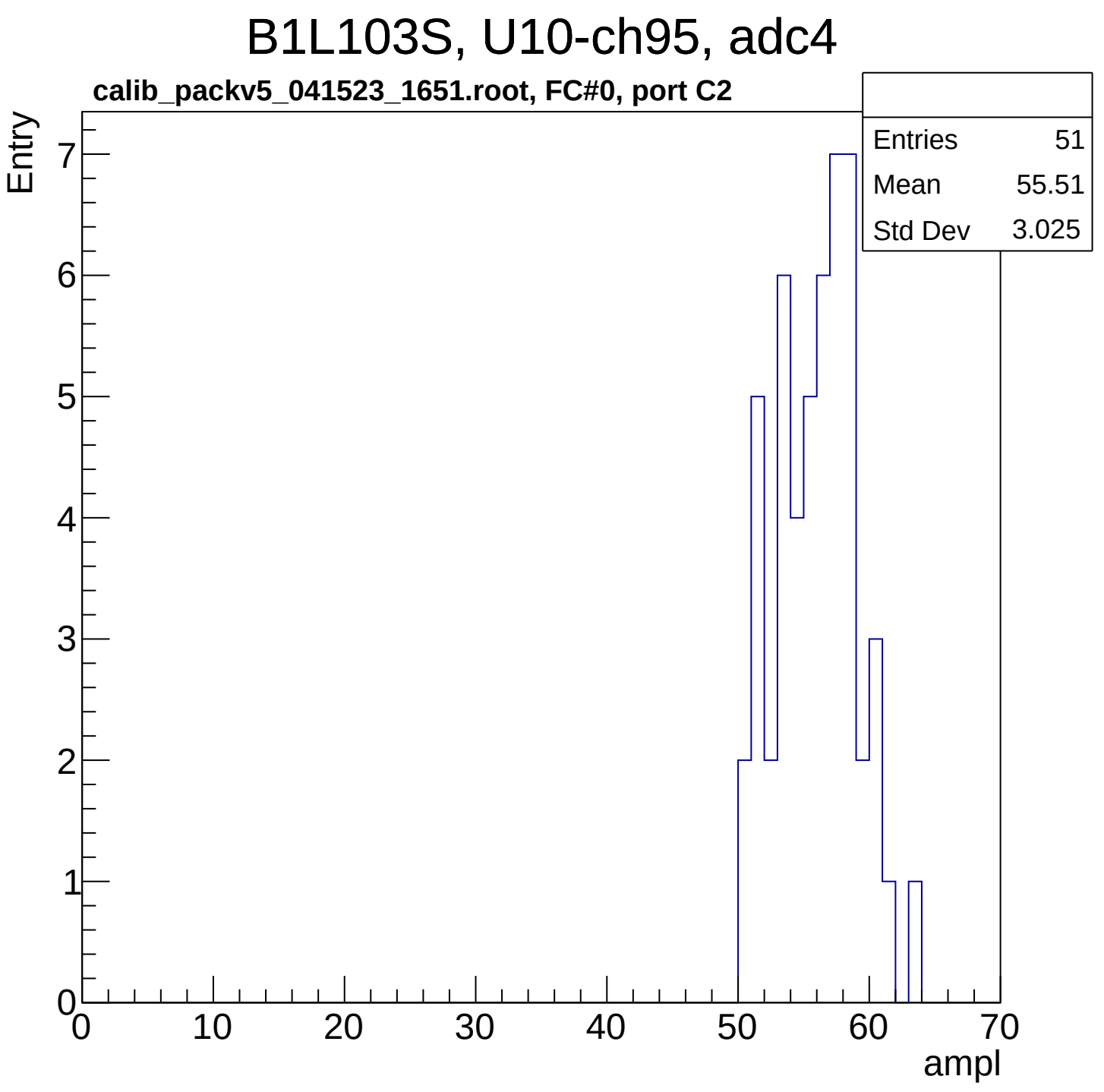
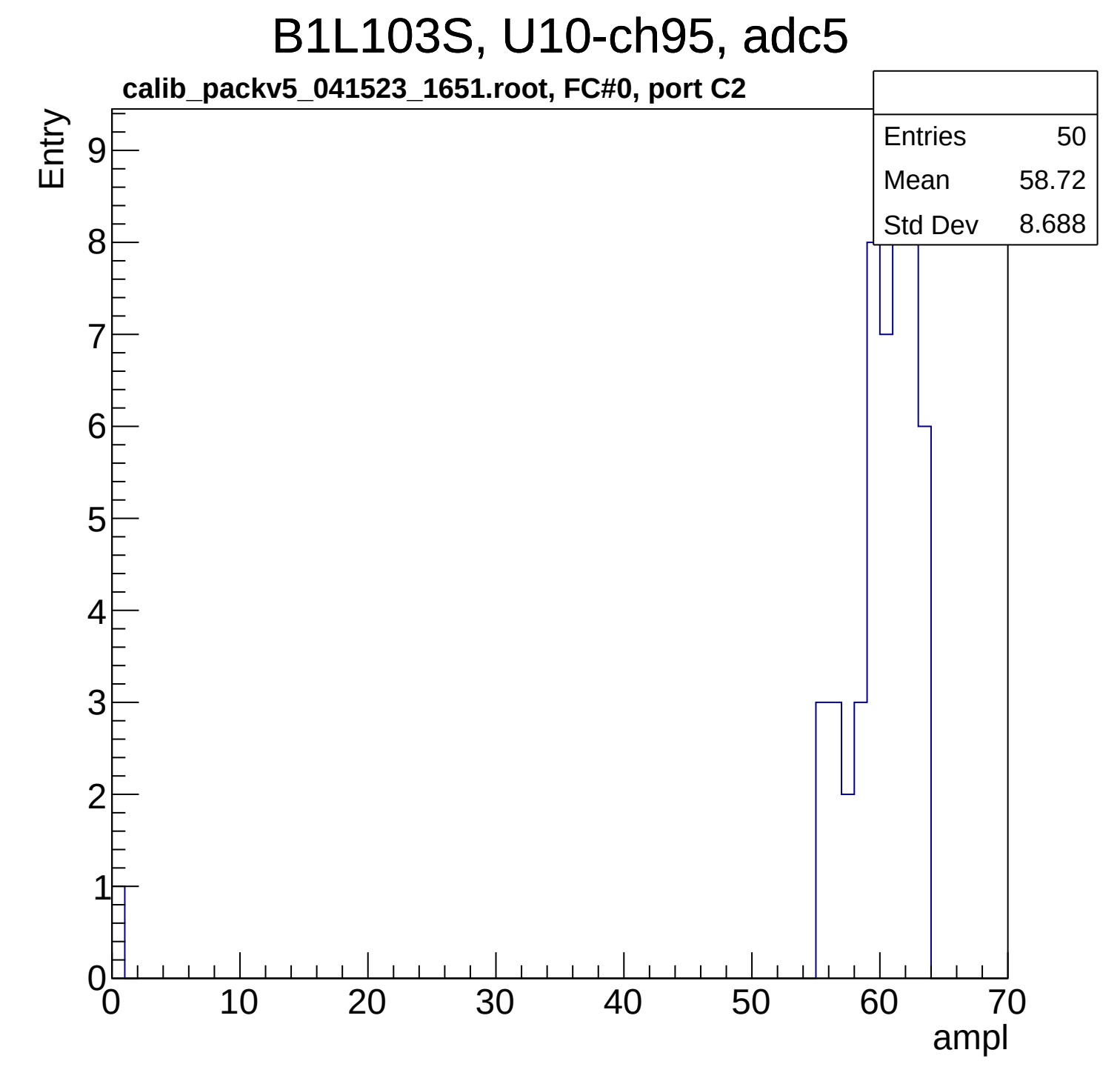
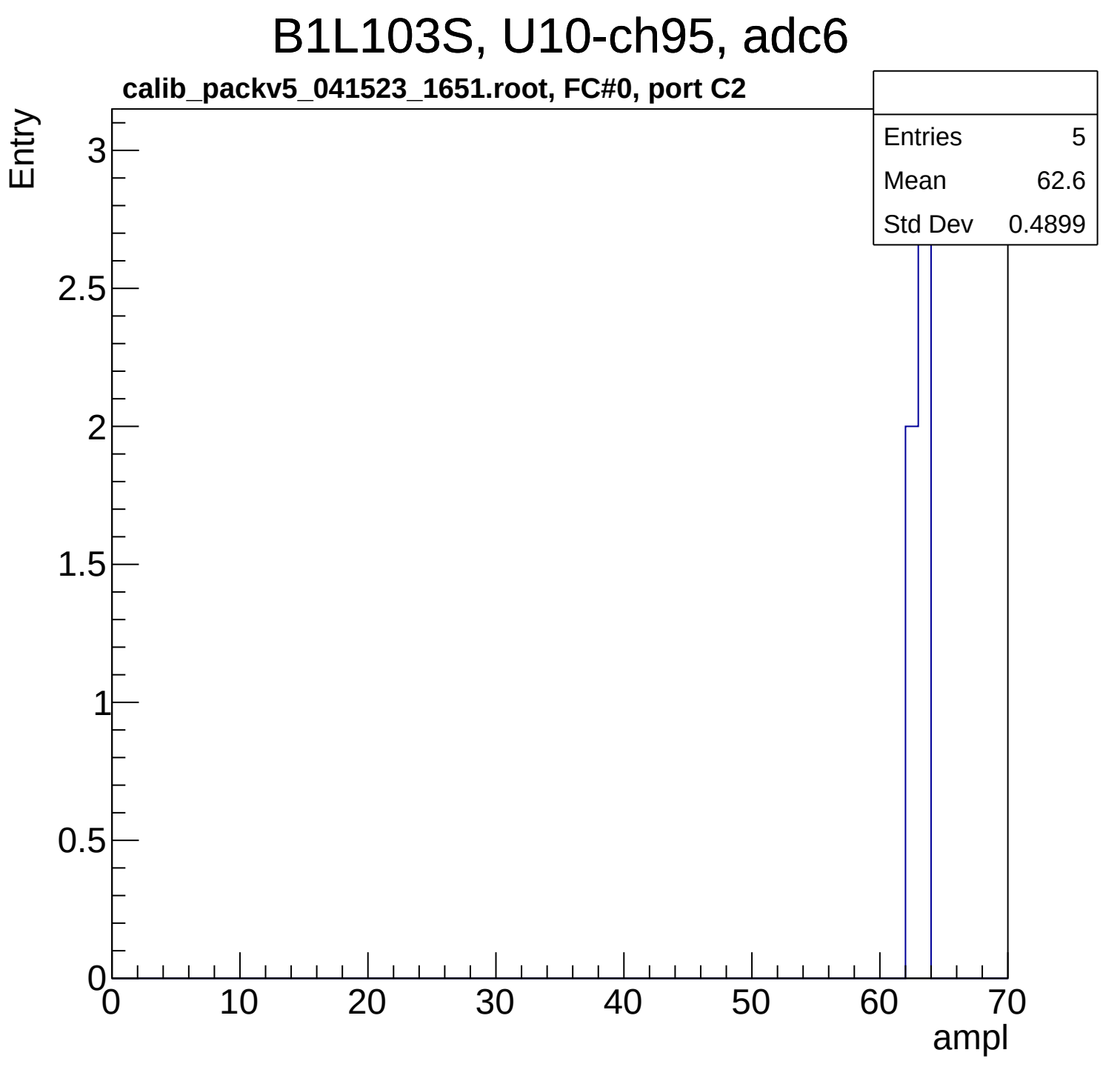
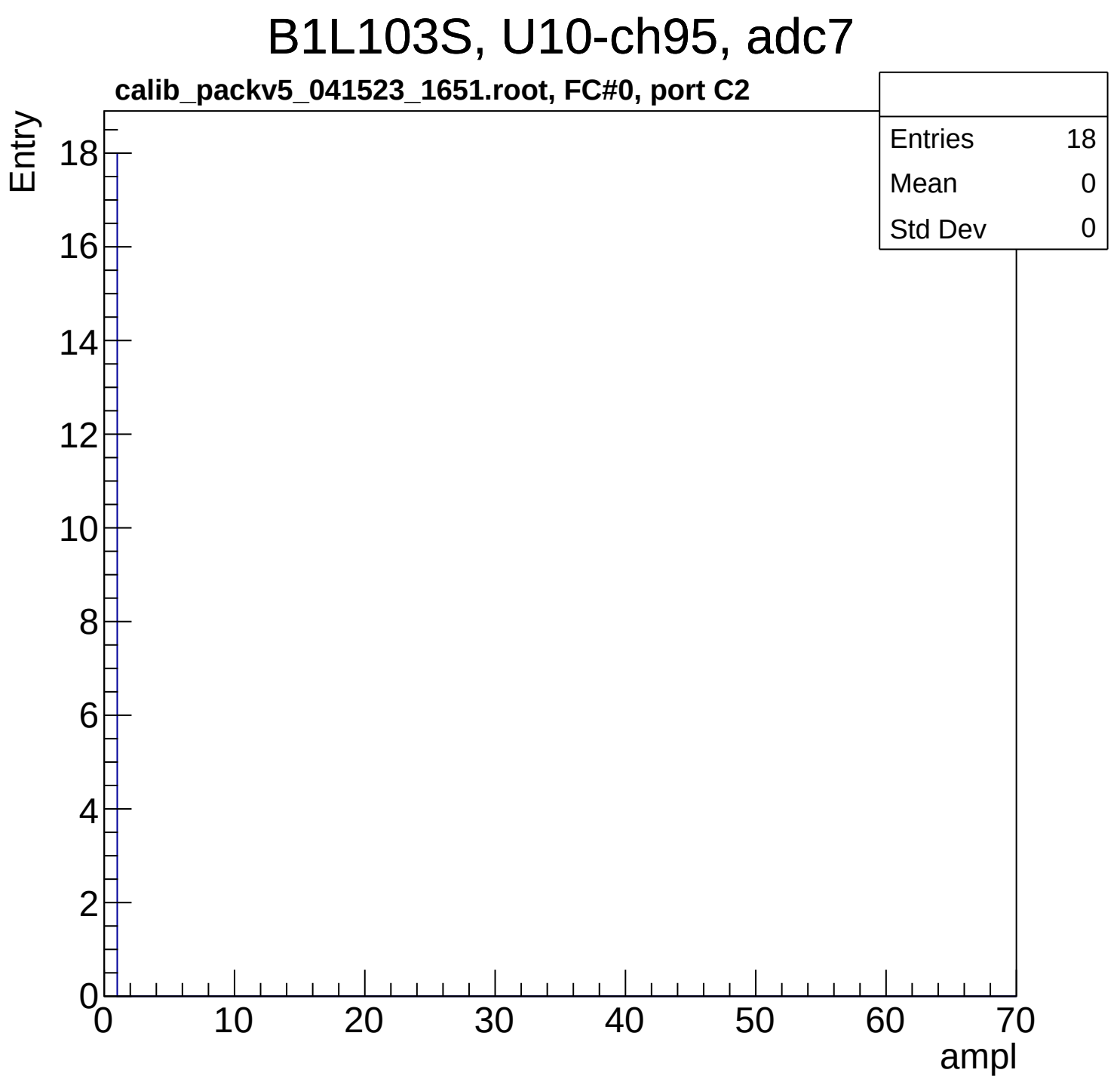
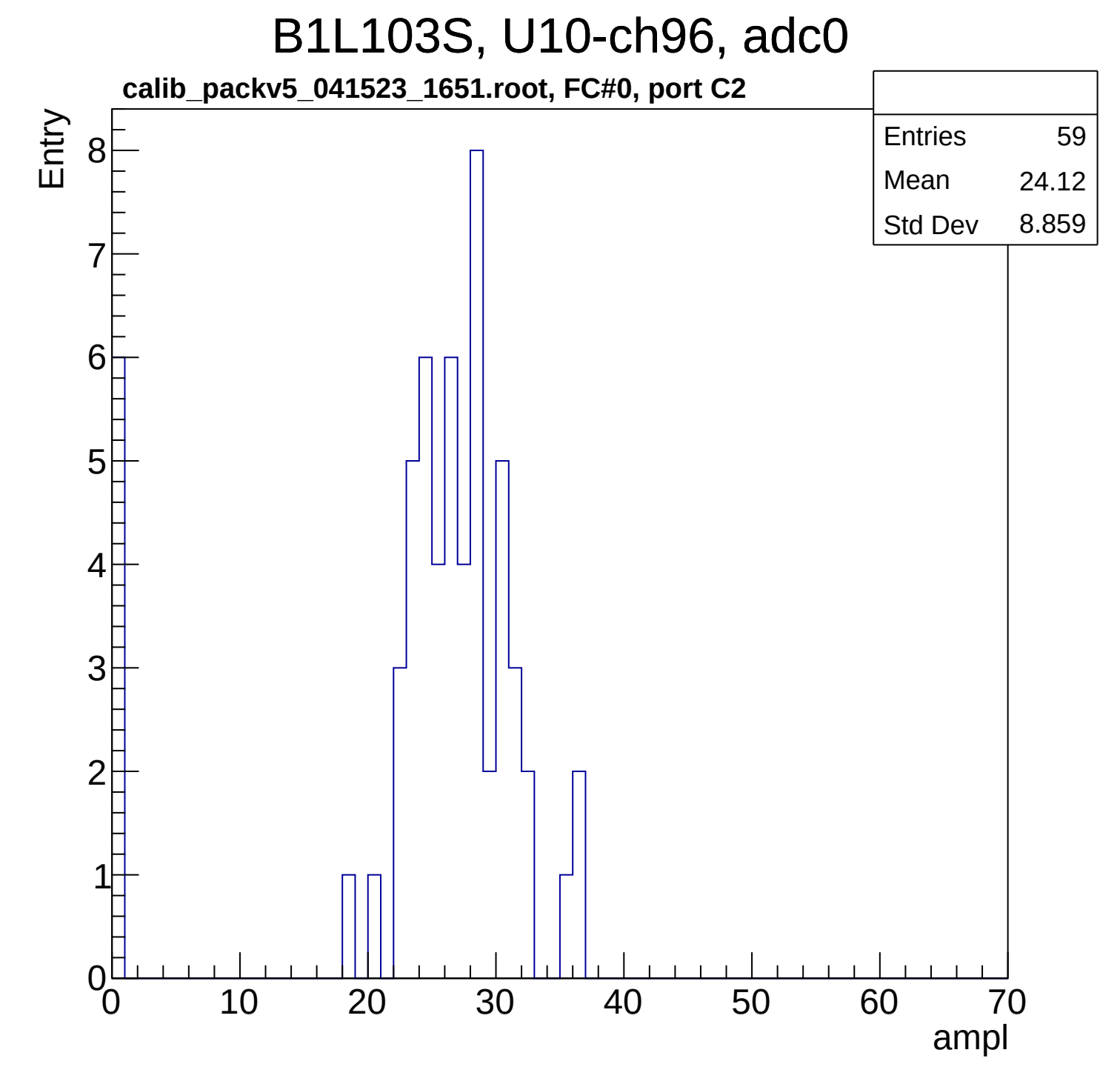
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9


B1L103S, U10-ch95, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 55.51
Std Dev 3.025
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U10-ch95, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 58.72
Std Dev 8.688
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U10-ch95, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 5
Mean 62.6
Std Dev 0.4899
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U10-ch95, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch96, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 24.12
Std Dev 8.859
Entry
ampl
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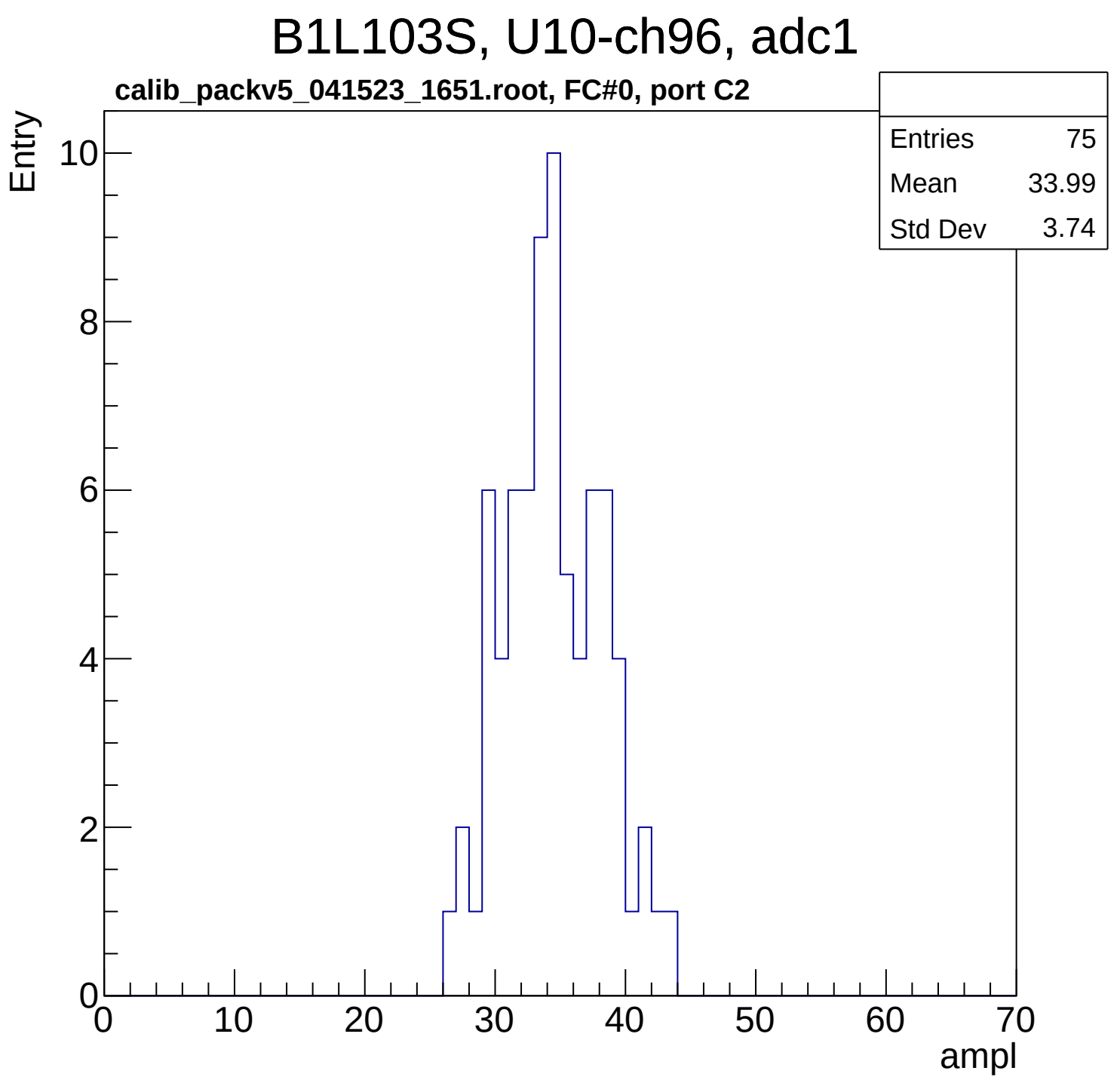
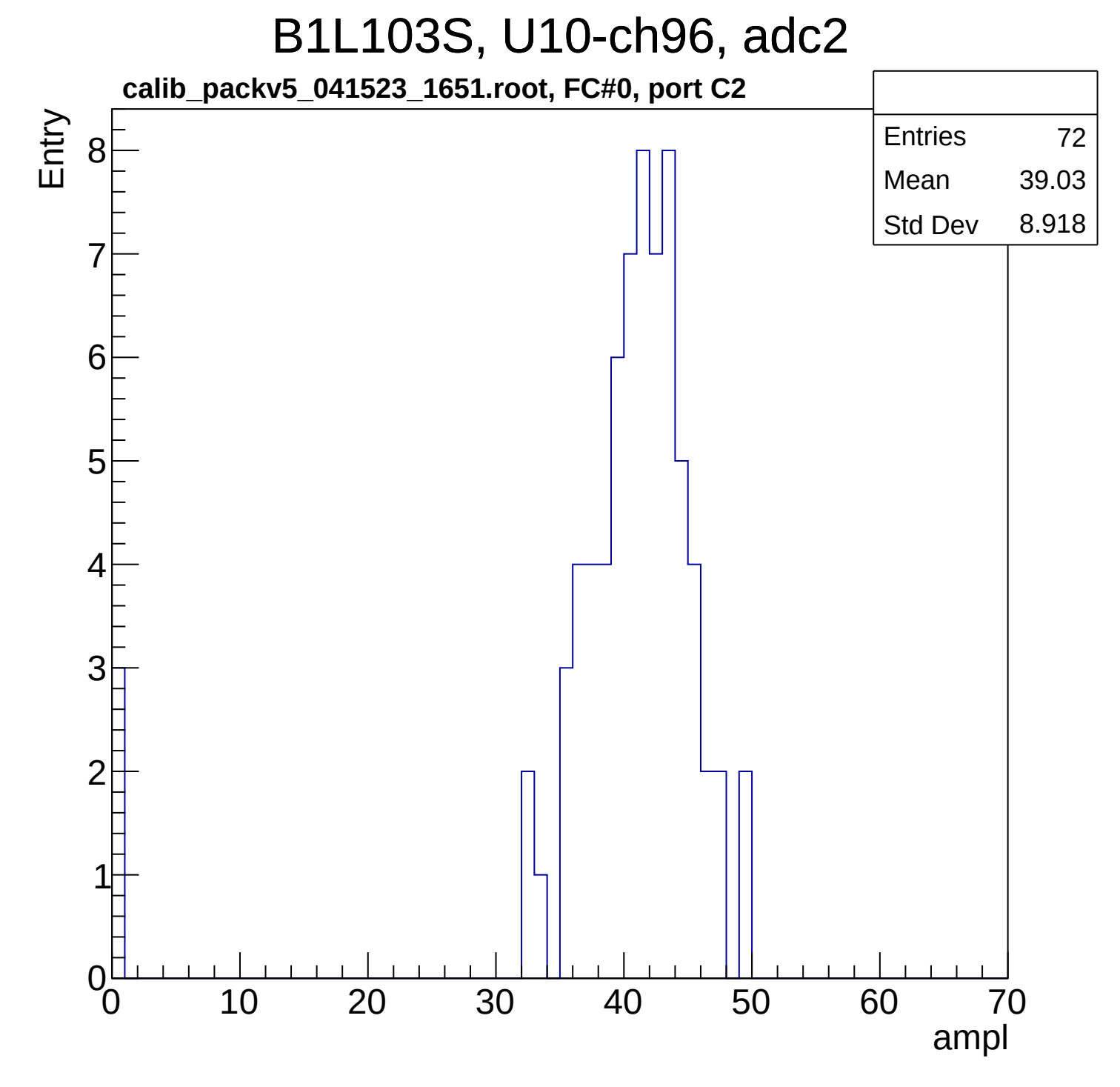
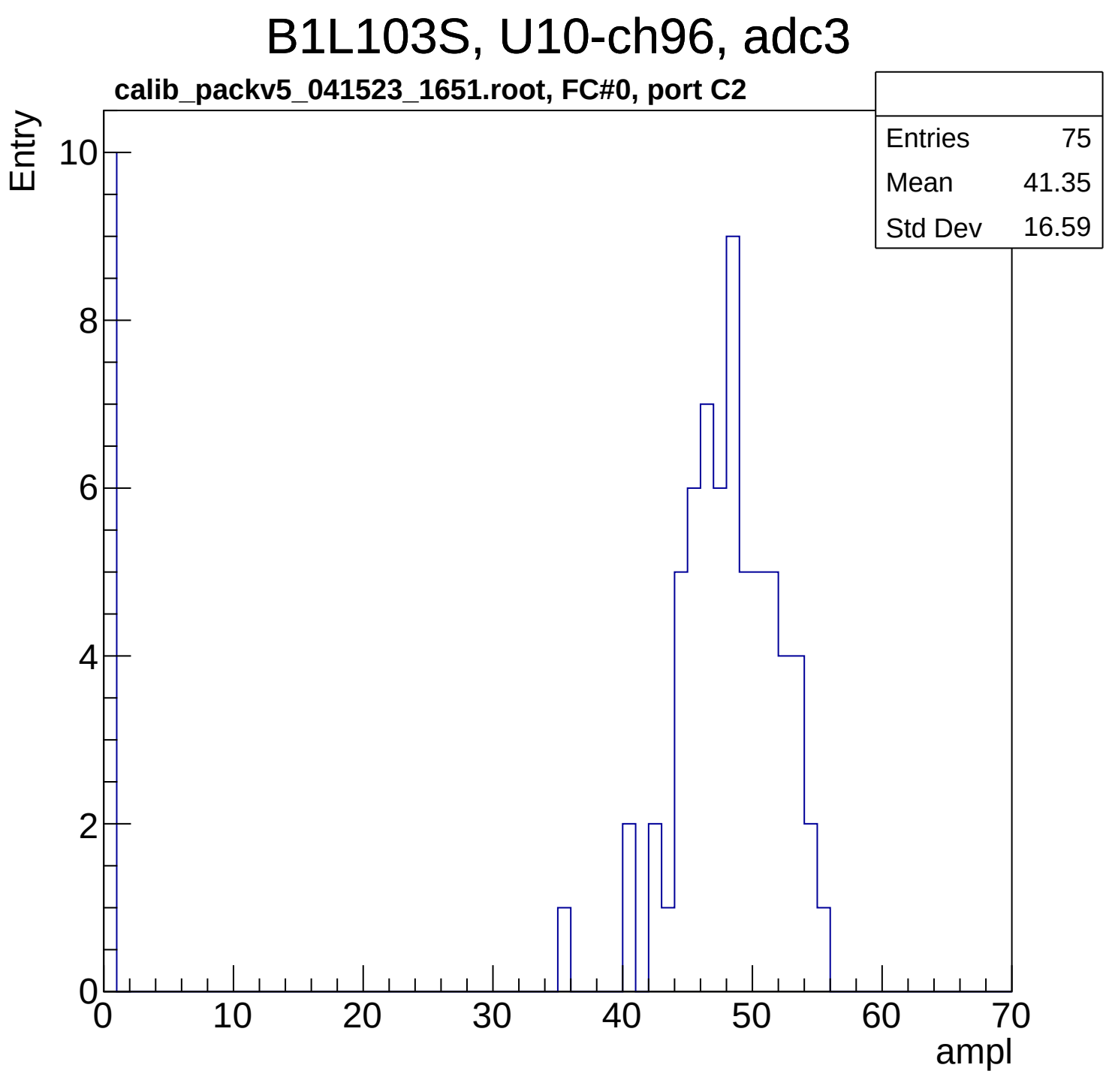
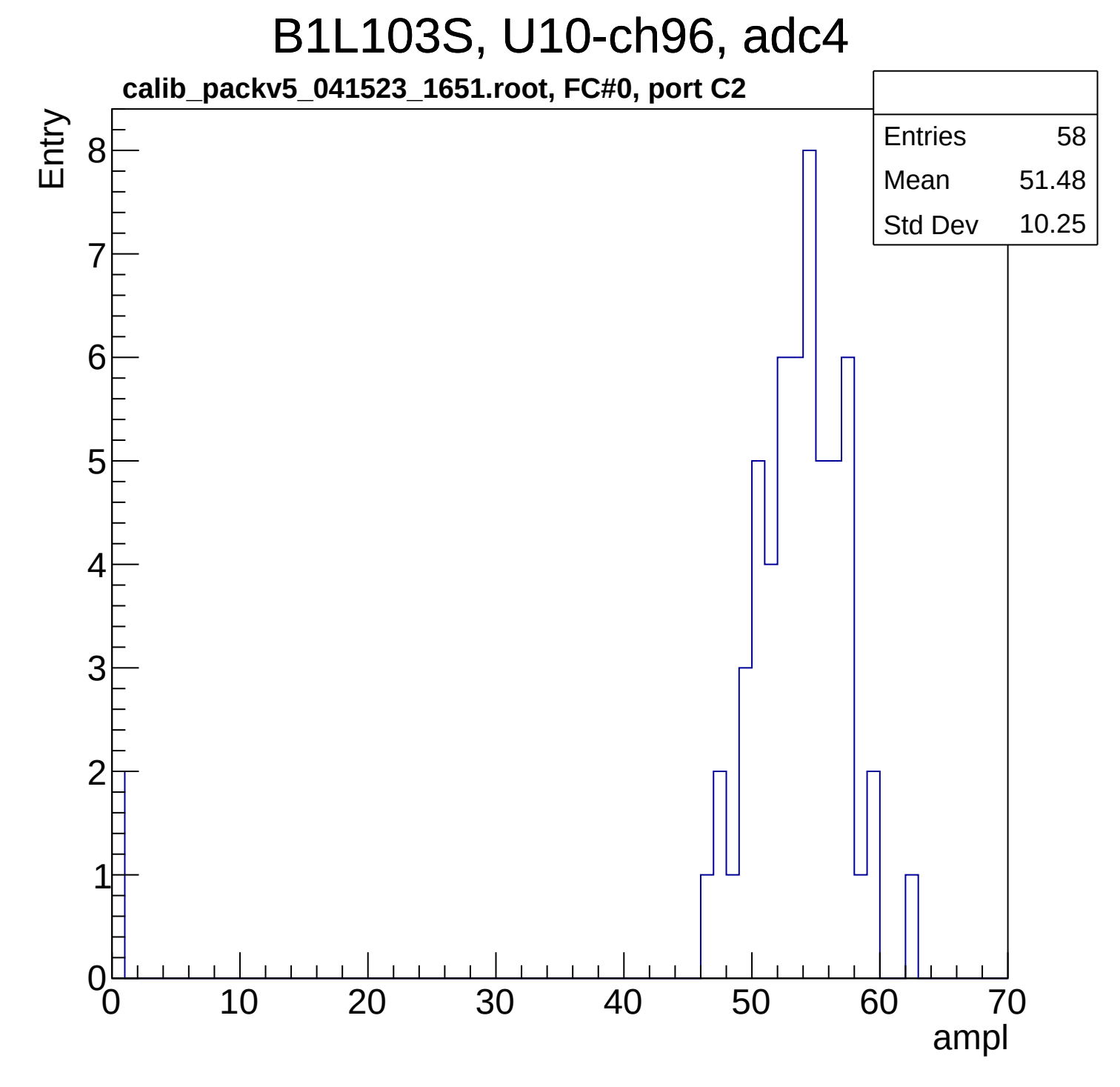
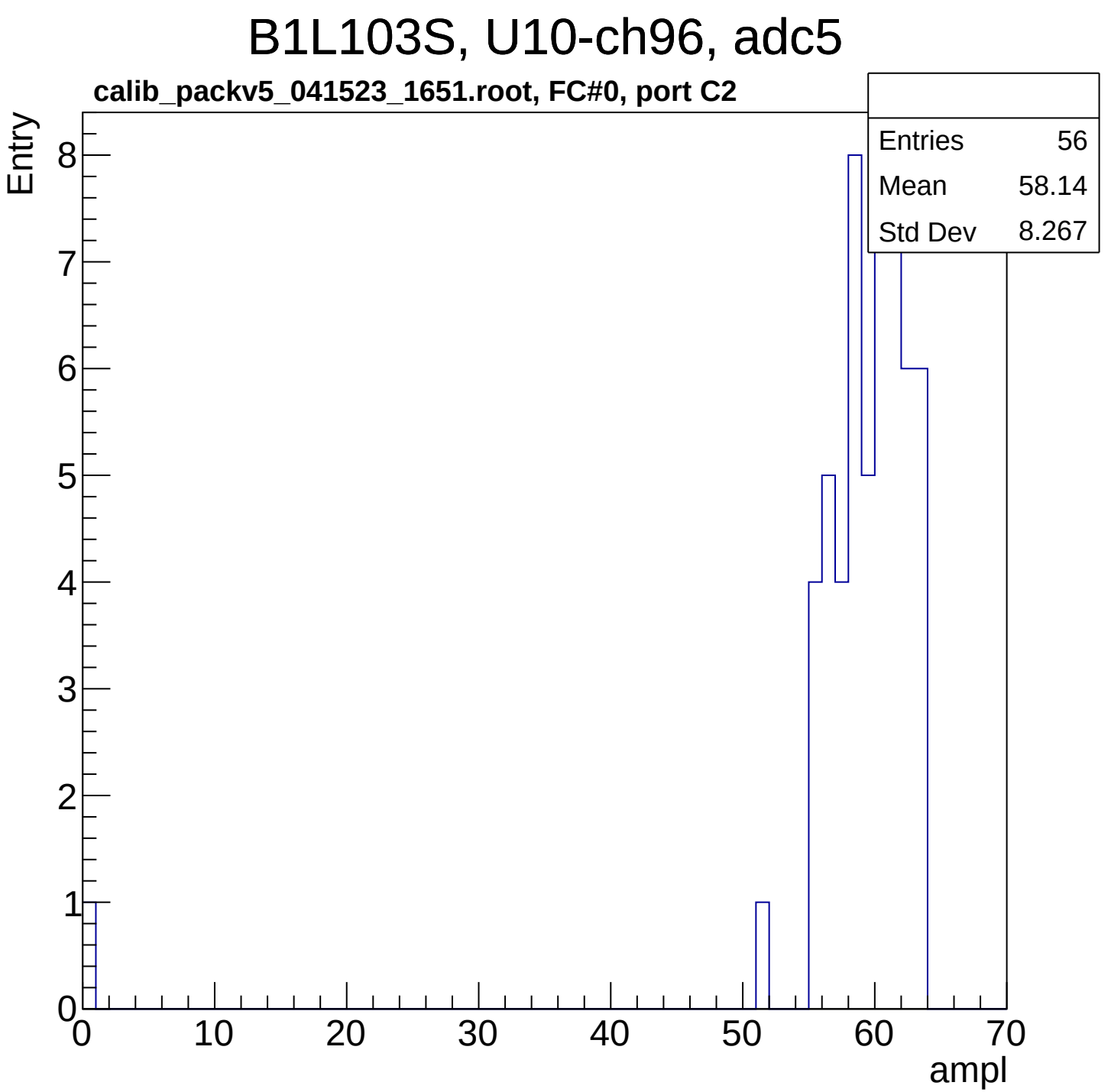
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U10-ch96, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 33.99
Std Dev 3.74
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch96, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 39.03
Std Dev 8.918
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U10-ch96, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 41.35
Std Dev 16.59
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U10-ch96, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 51.48
Std Dev 10.25
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U10-ch96, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 58.14
Std Dev 8.267
Entry
ampl
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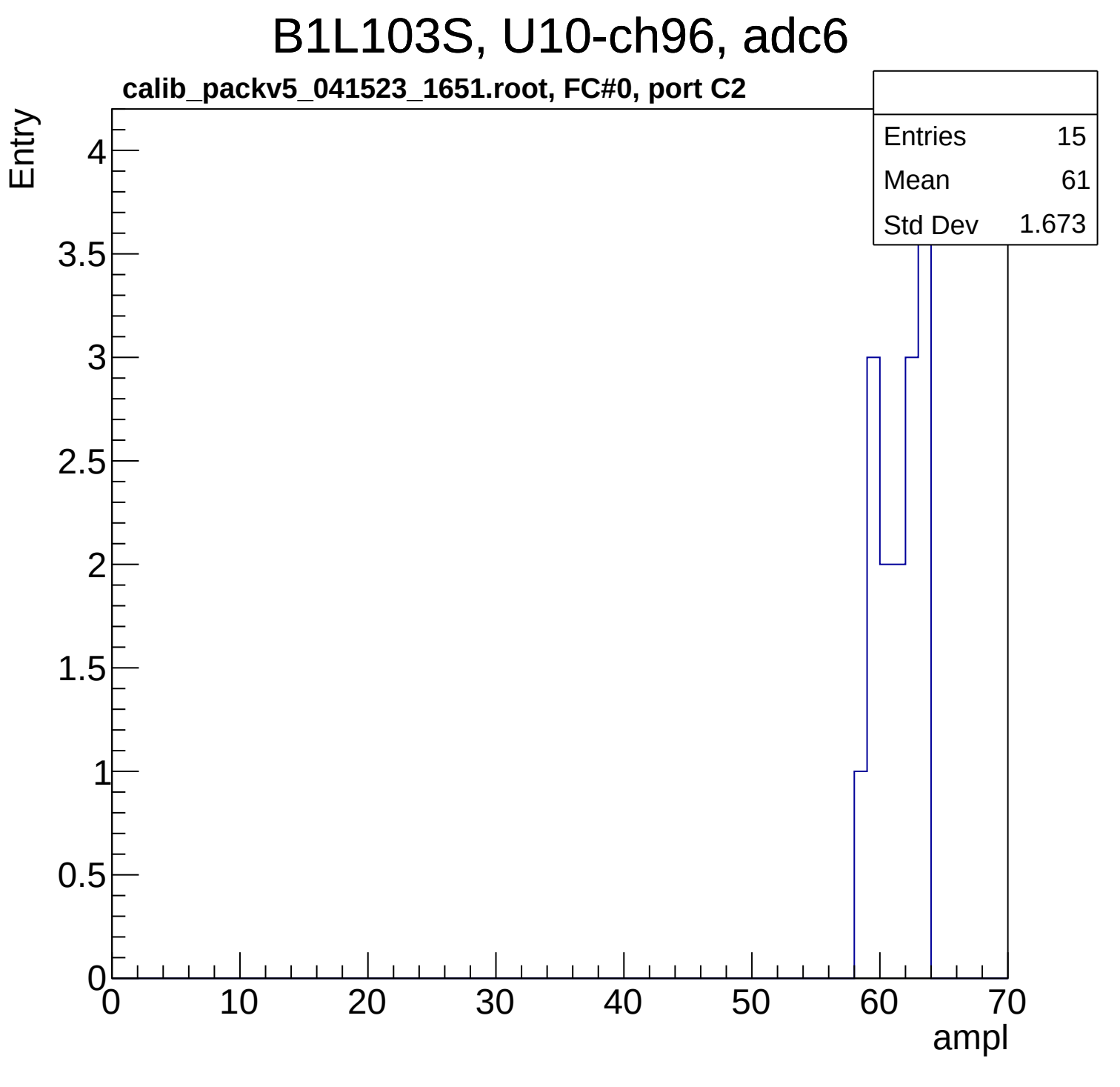
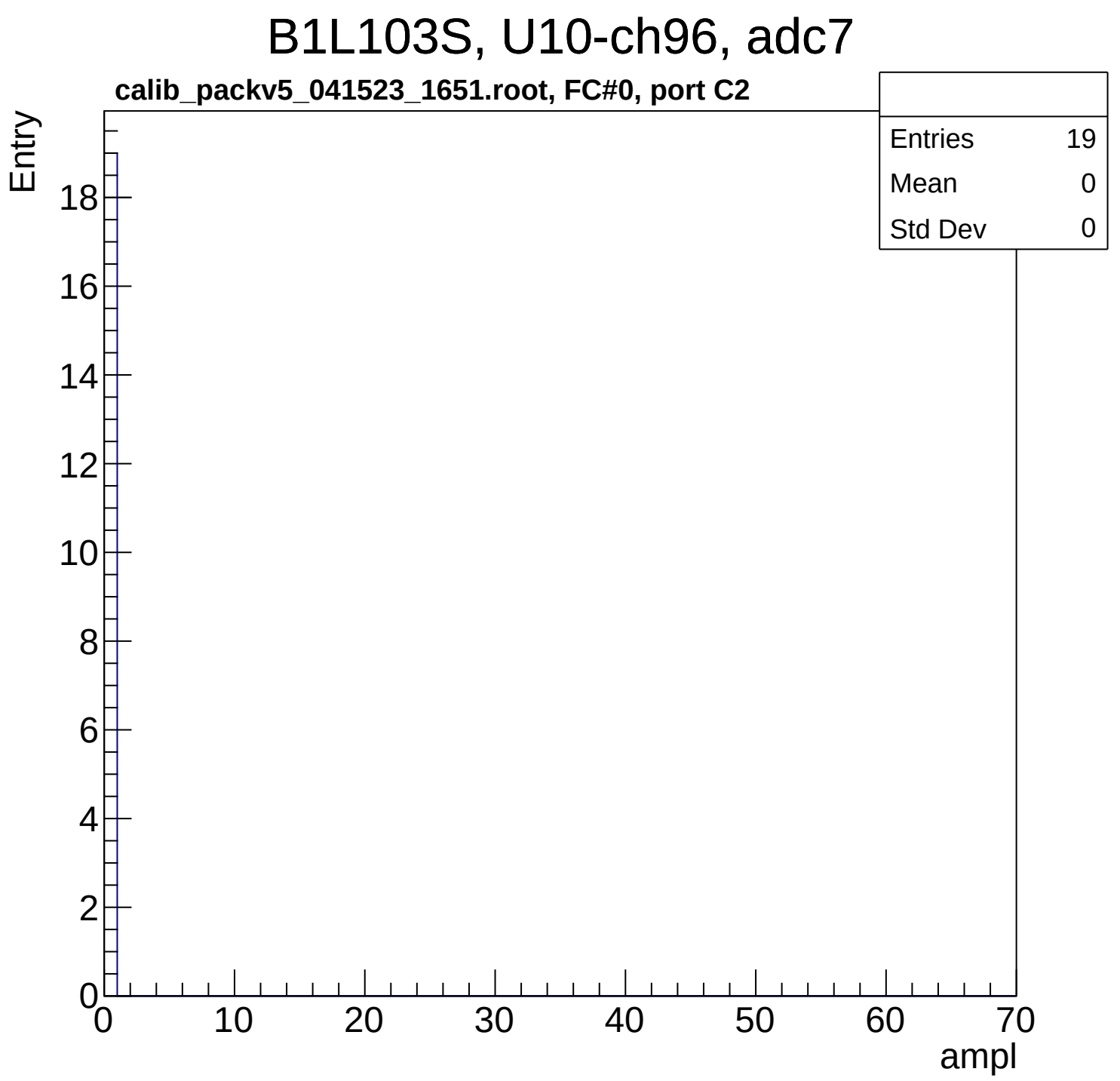
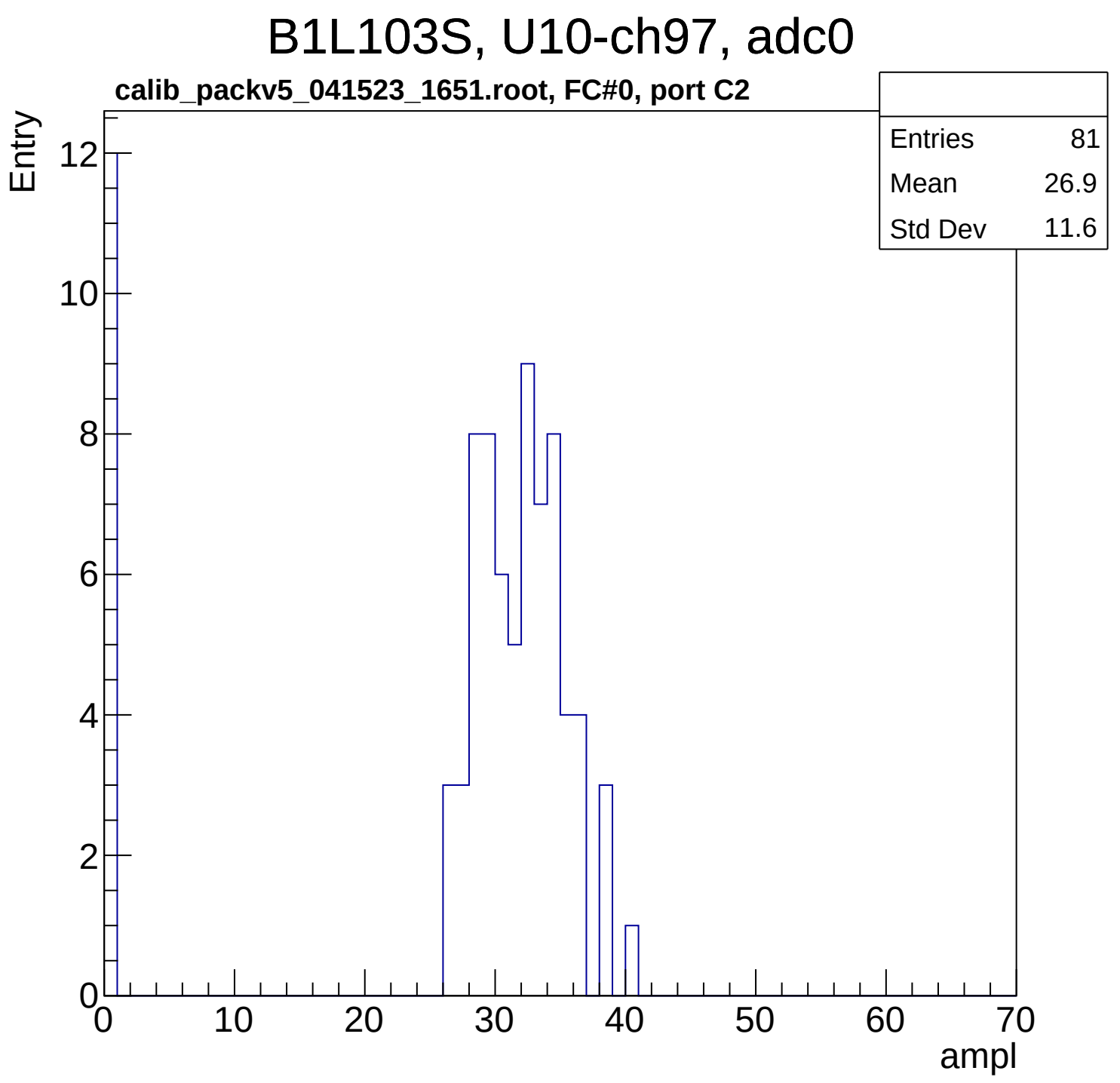
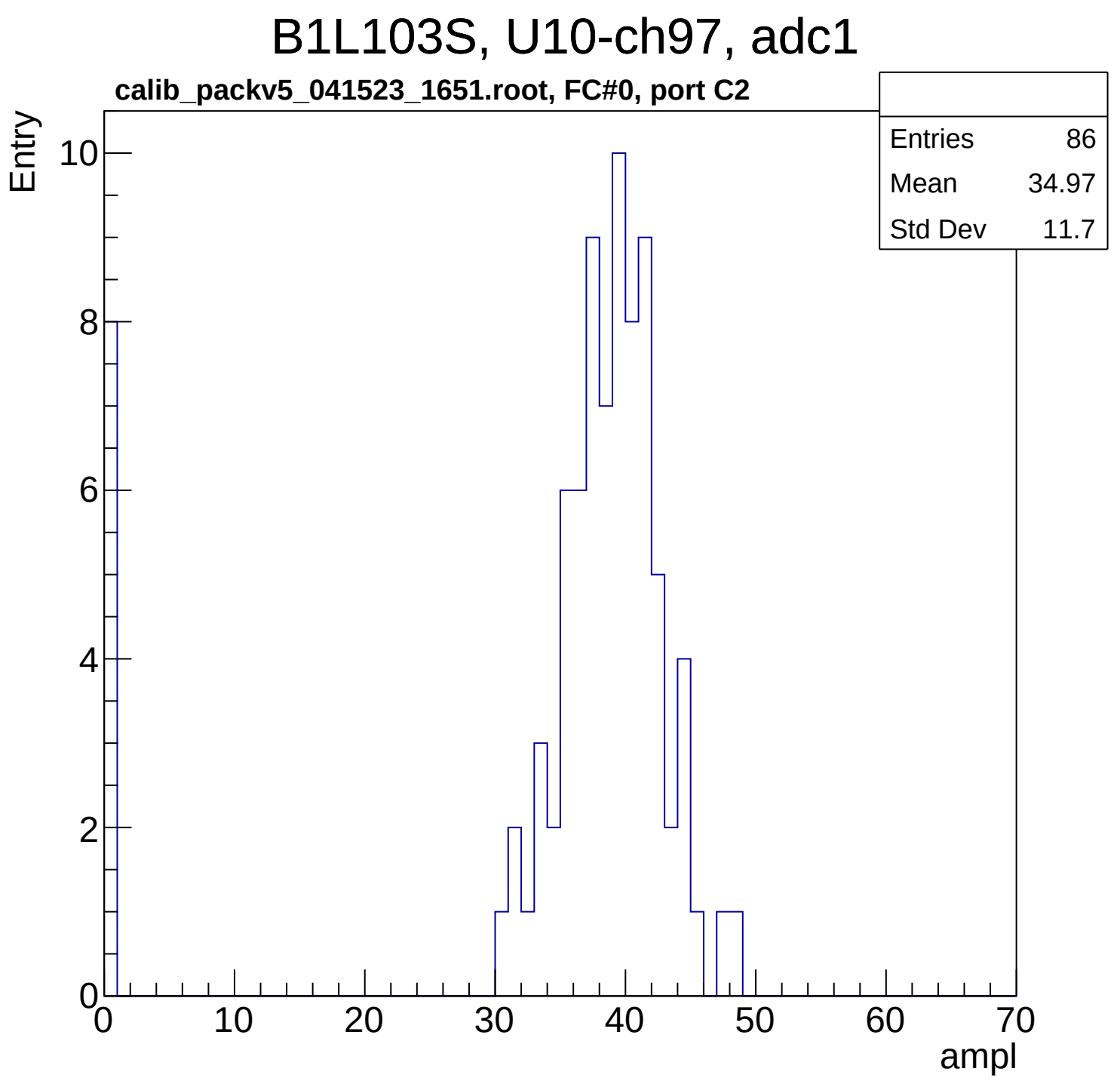
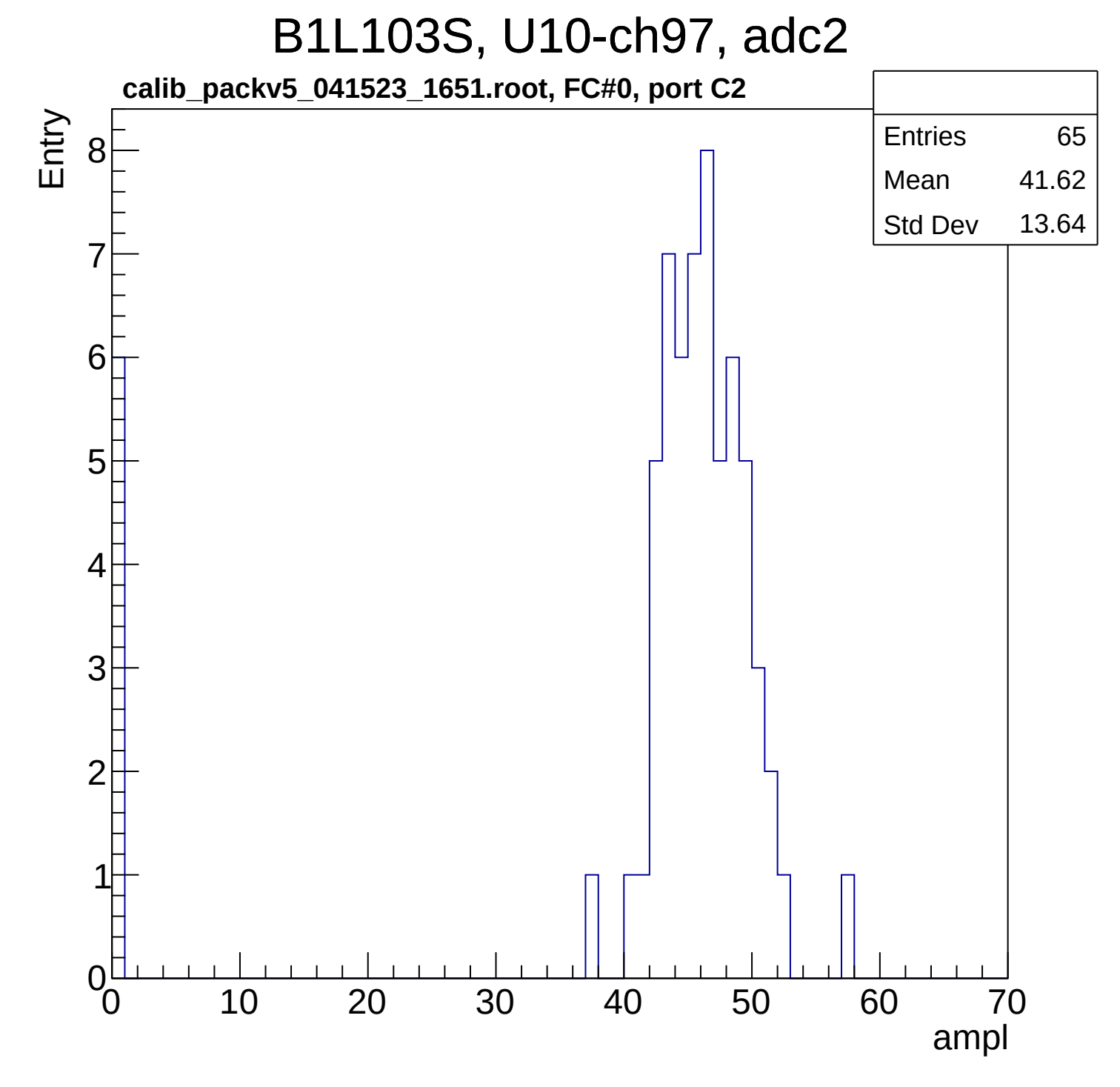
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U10-ch96, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 15
Mean 61
Std Dev 1.673
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U10-ch96, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch97, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 26.9
Std Dev 11.6
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch97, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 34.97
Std Dev 11.7
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch97, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 41.62
Std Dev 13.64
Entry
ampl
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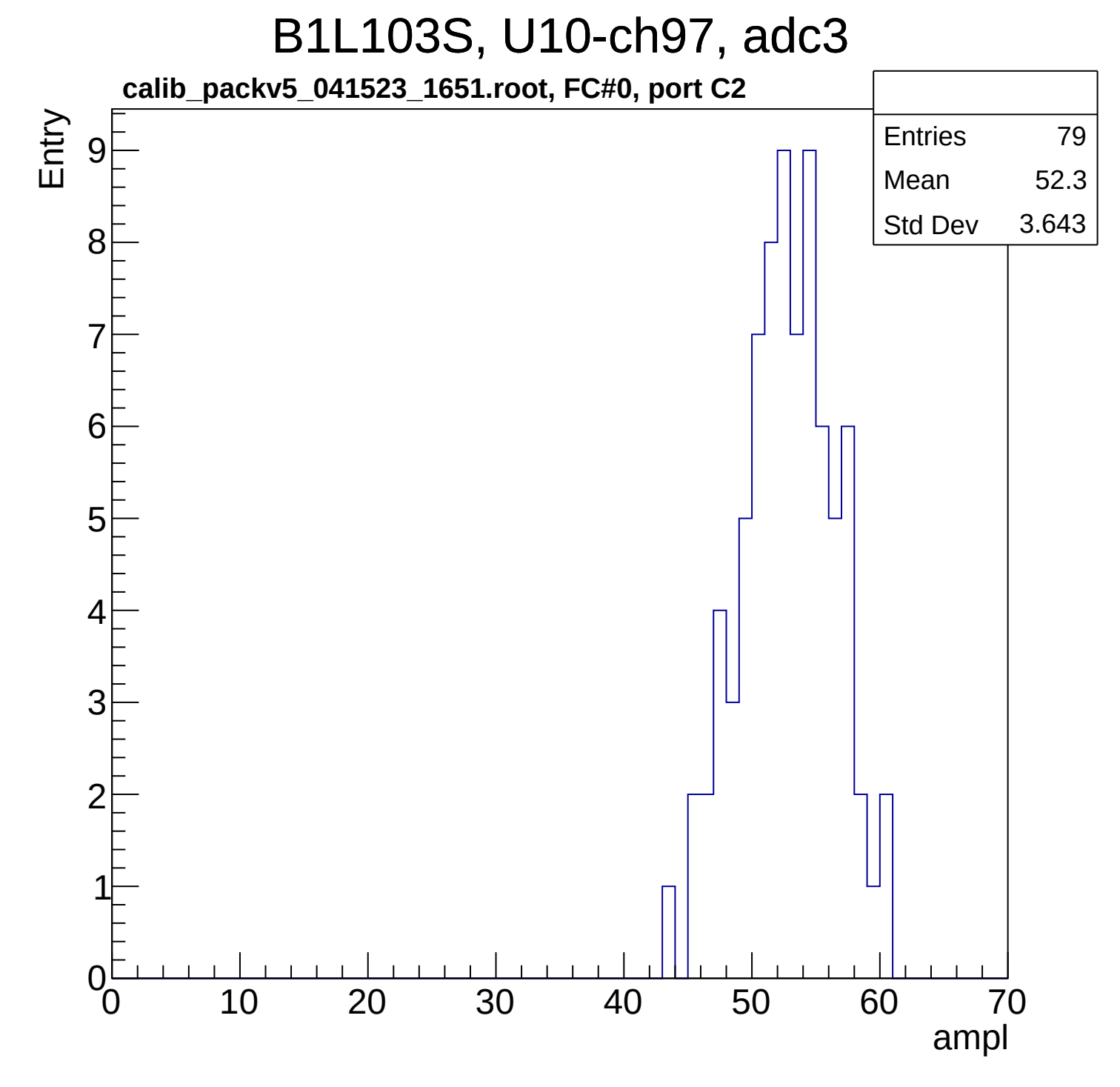
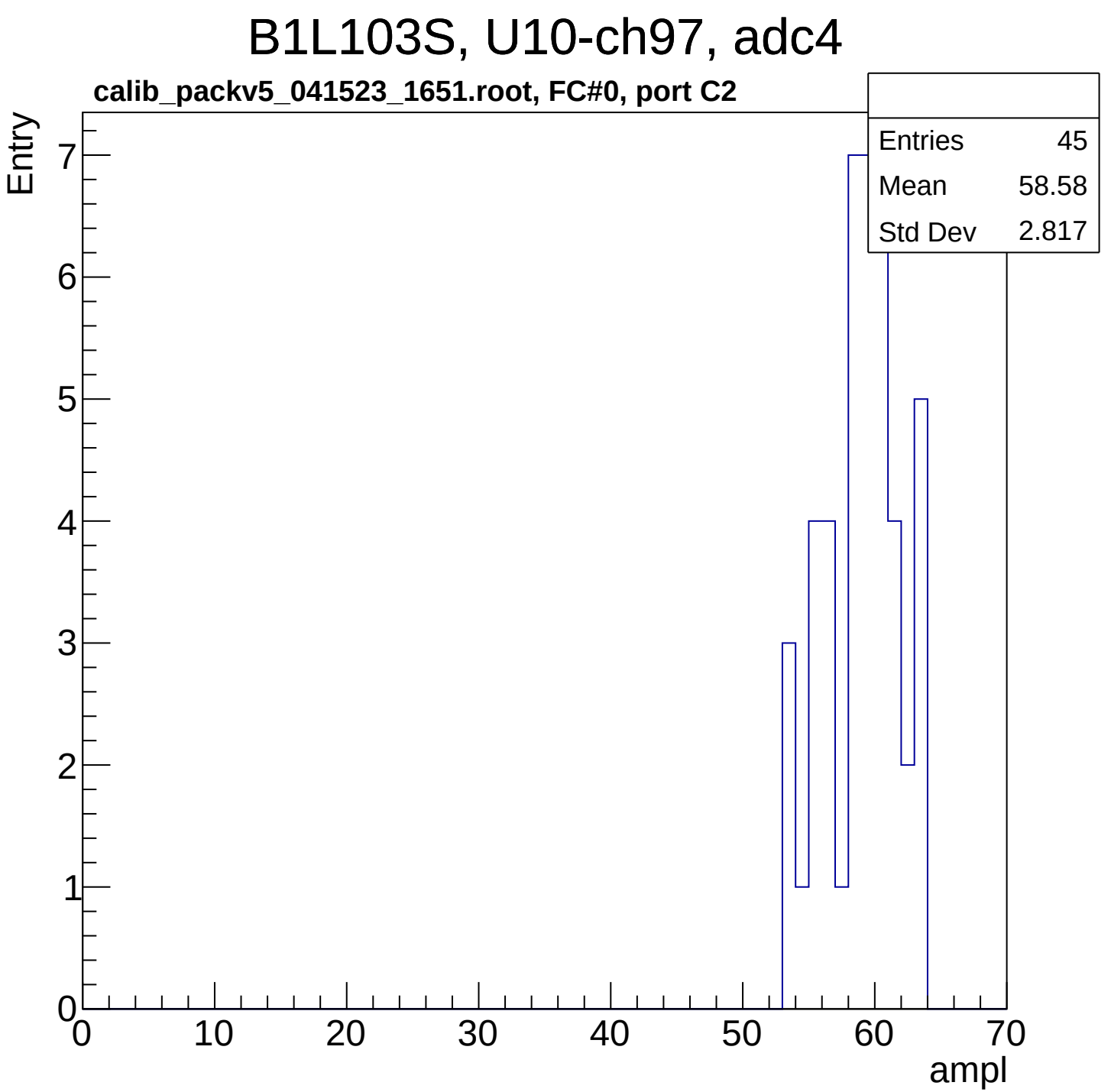
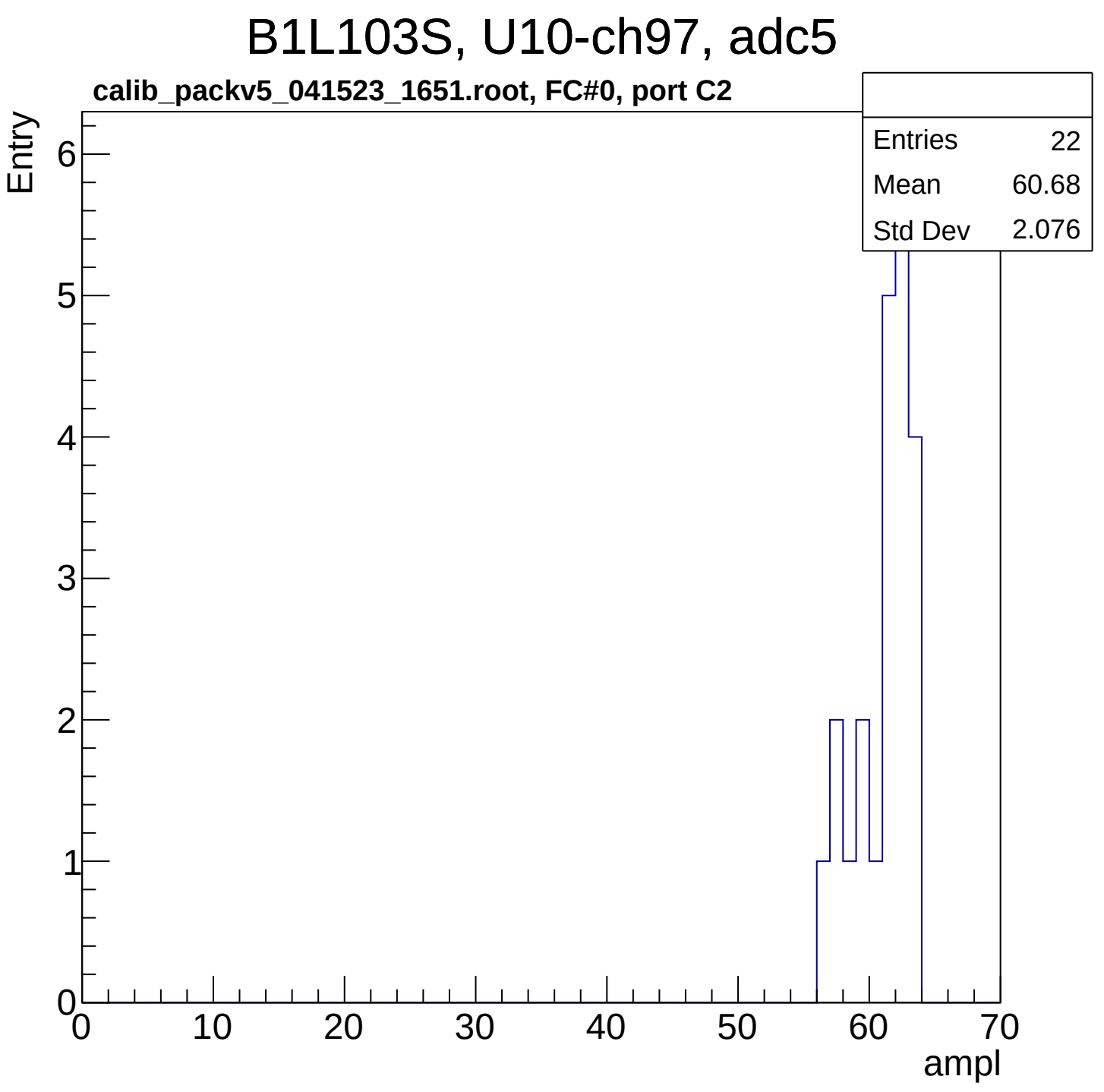
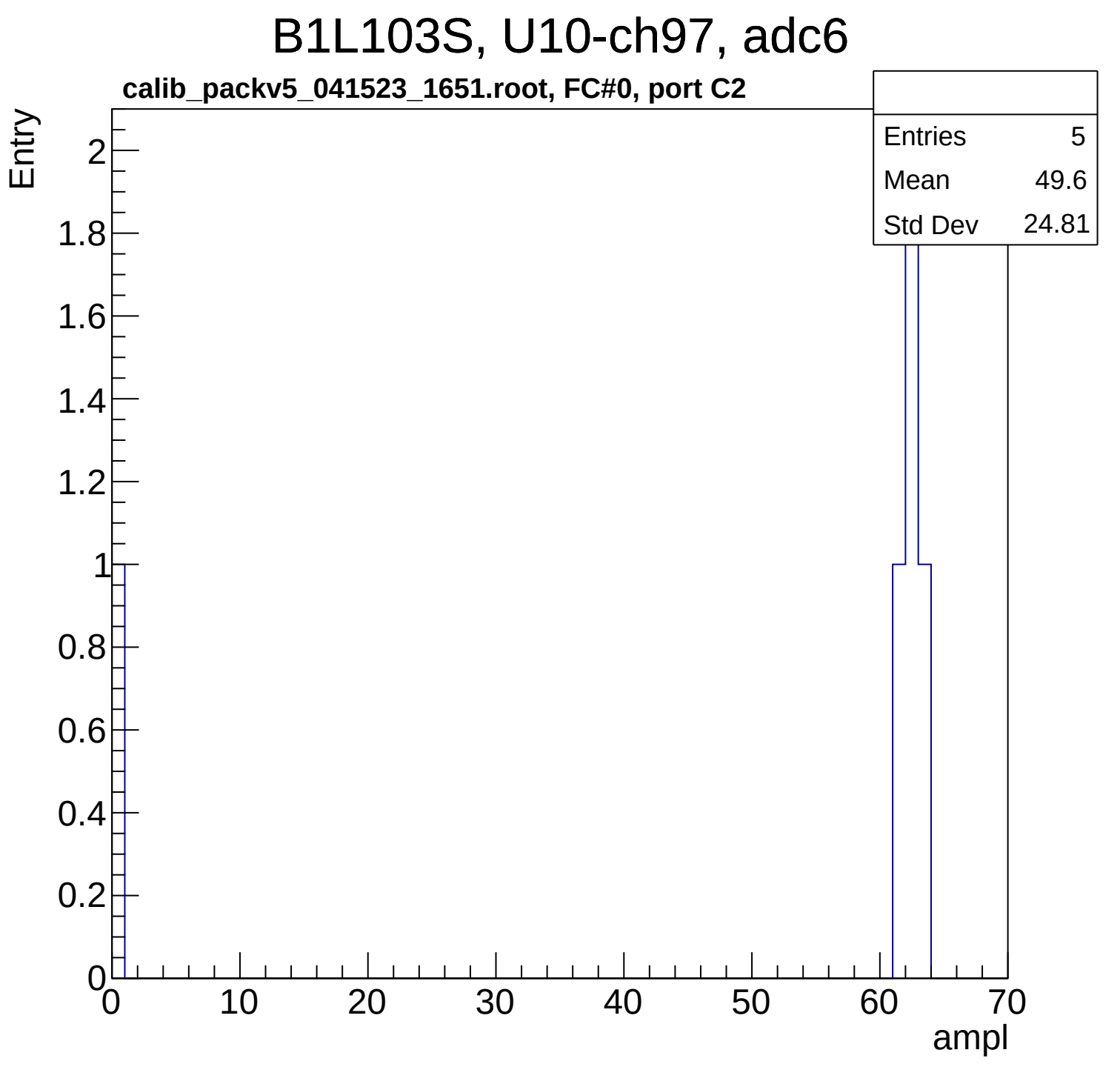
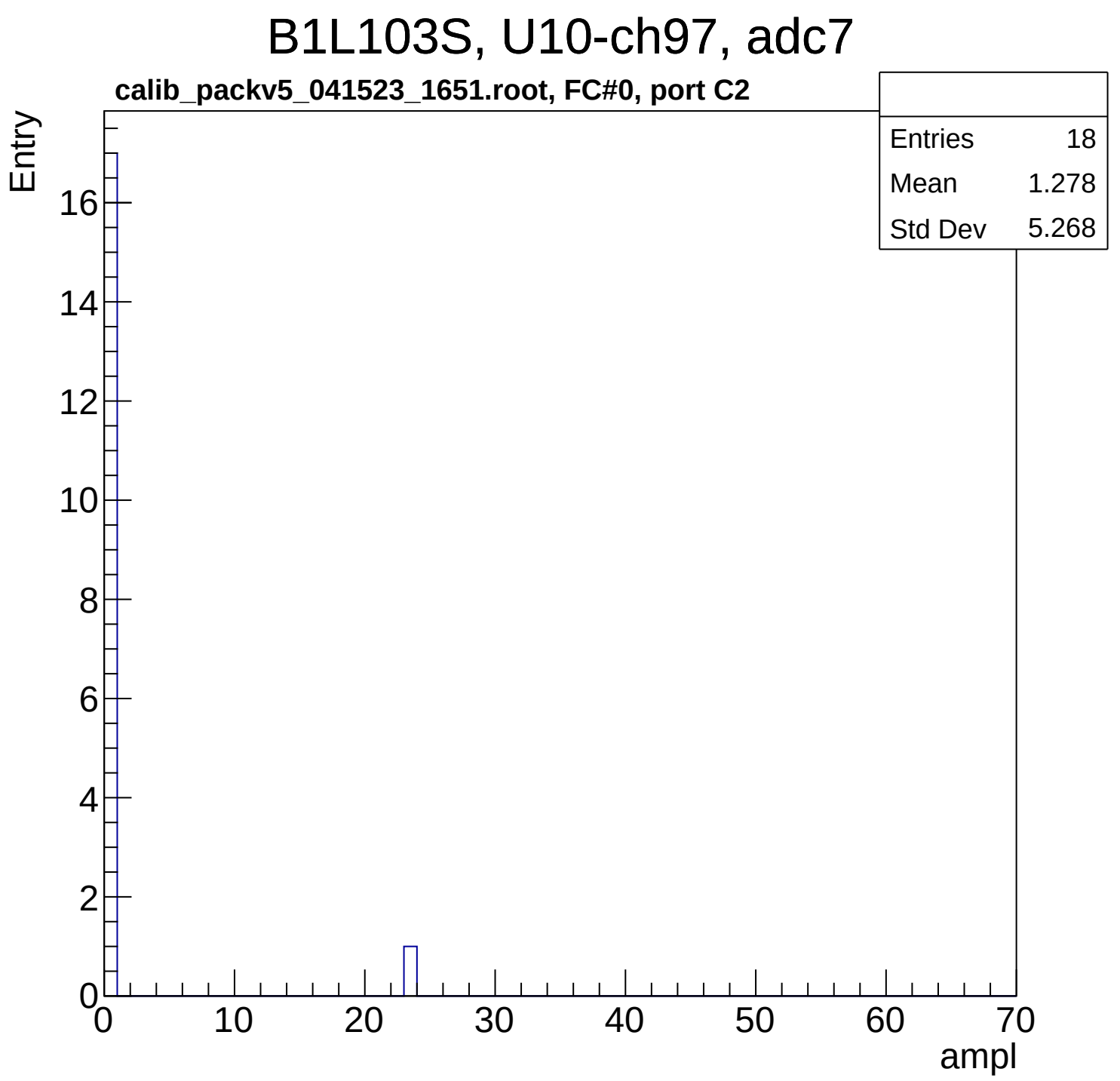
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

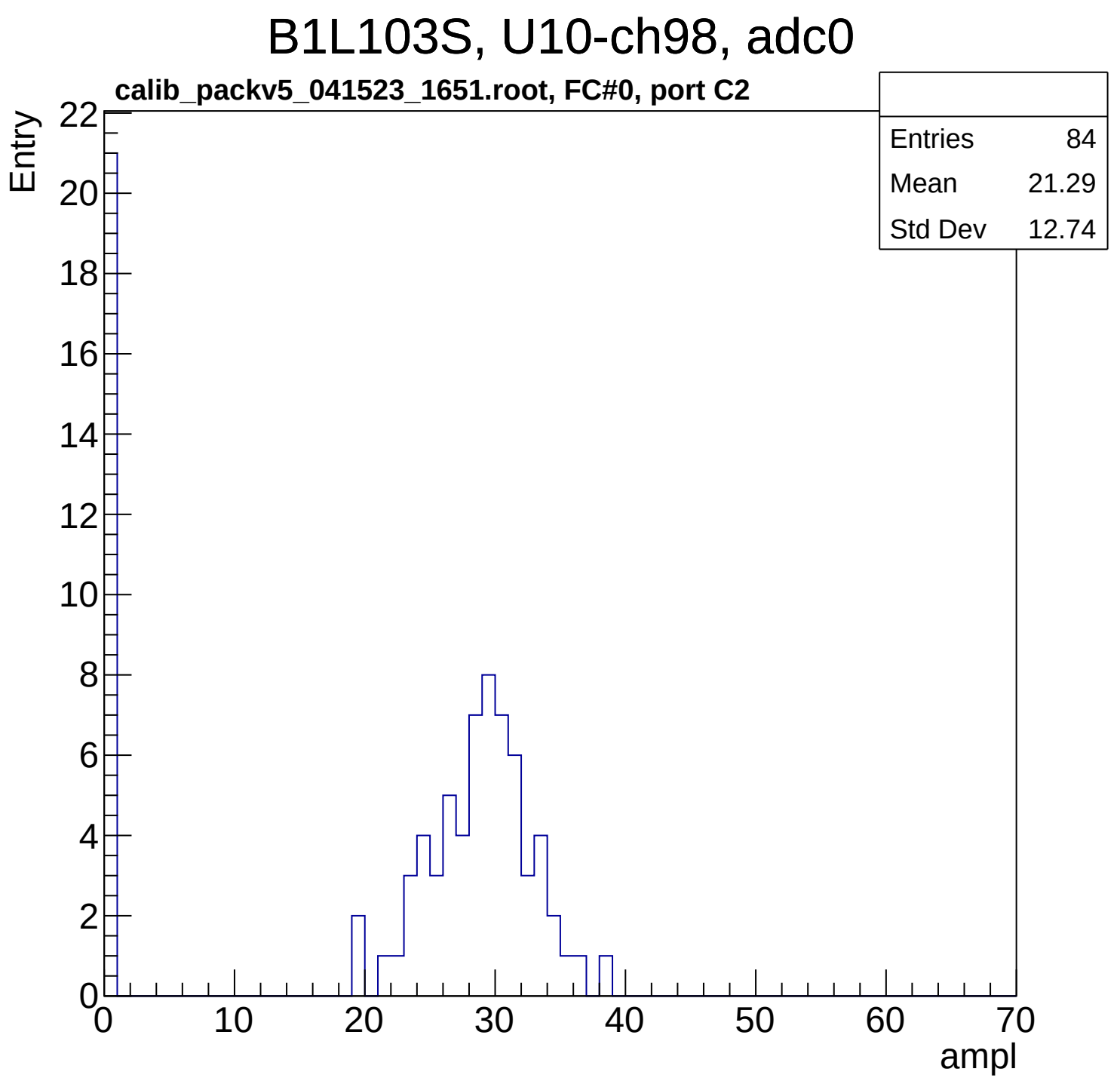

B1L103S, U10-ch97, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 52.3
Std Dev 3.643
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

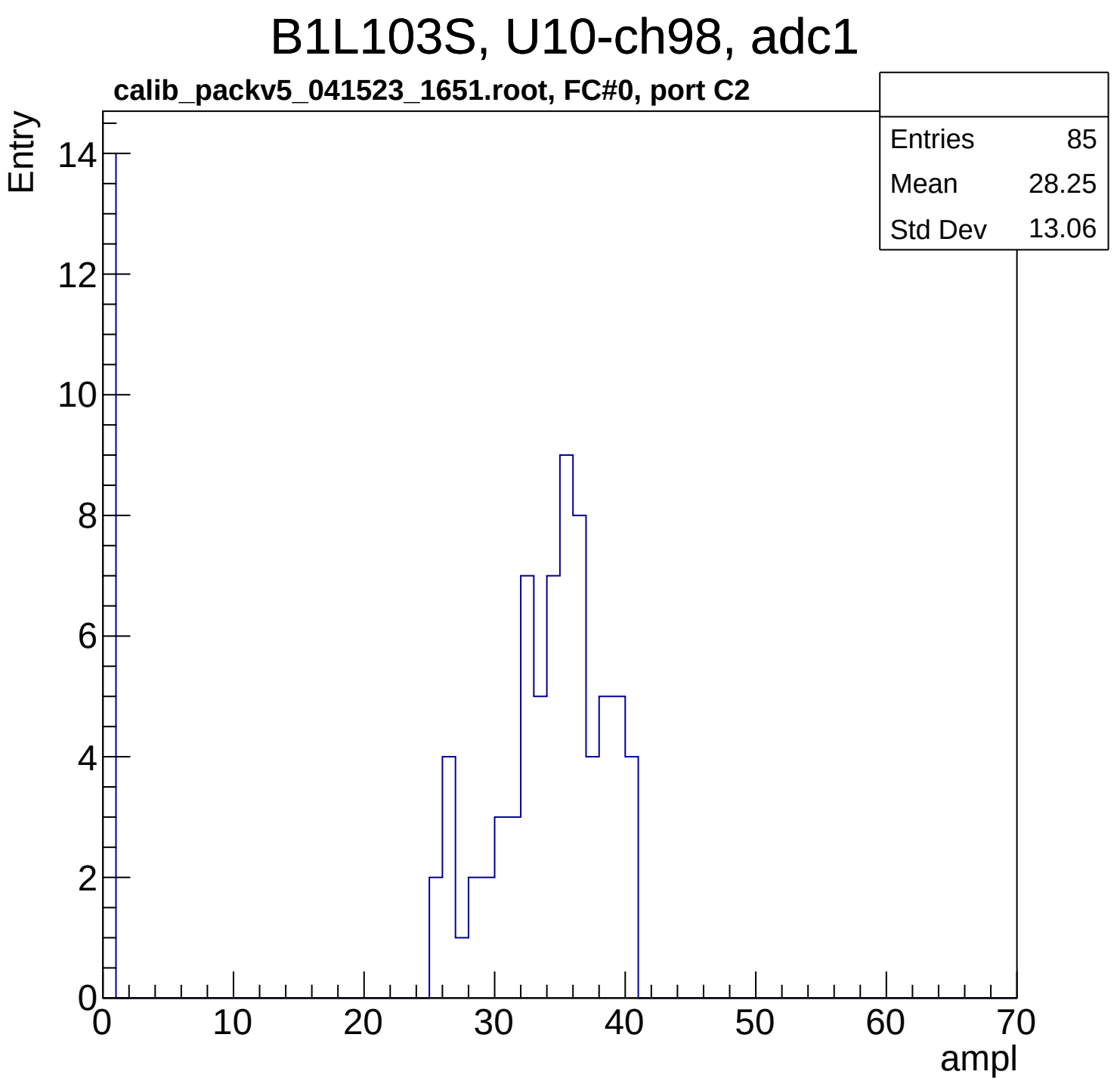

B1L103S, U10-ch97, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 58.58
Std Dev 2.817
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

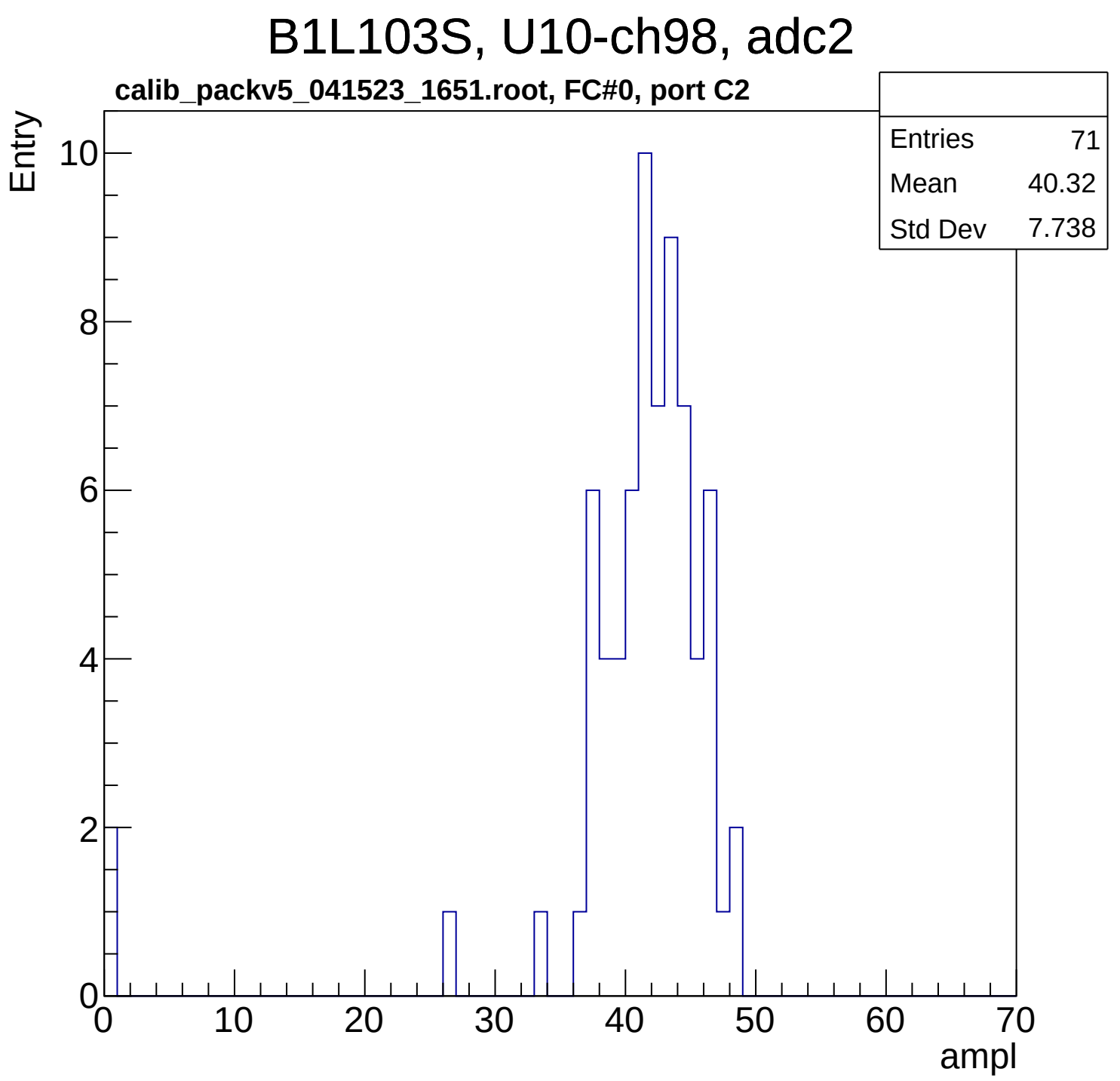

B1L103S, U10-ch97, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 60.68
Std Dev 2.076
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl

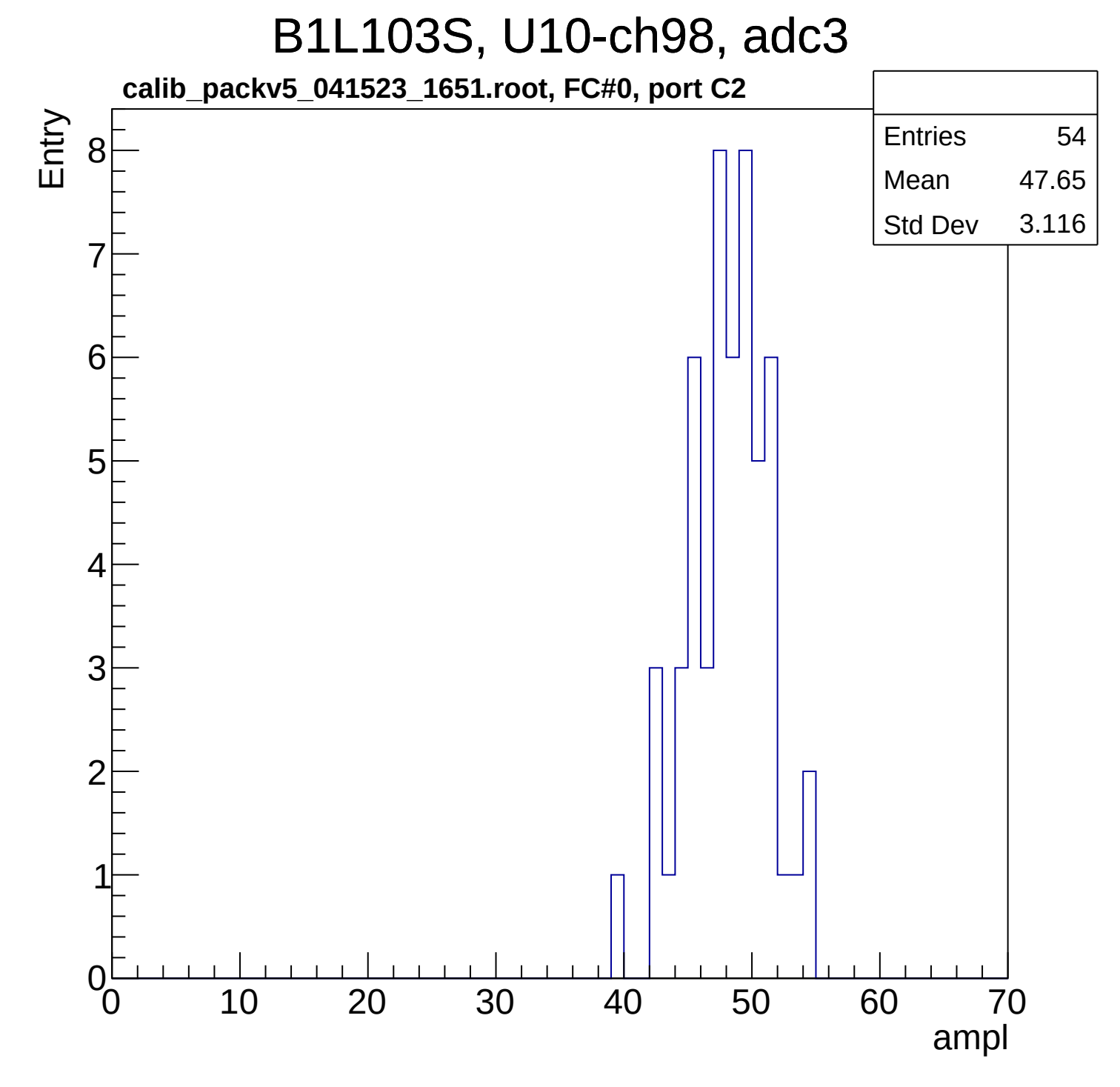

B1L103S, U10-ch97, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 5
Mean 49.6
Std Dev 24.81
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

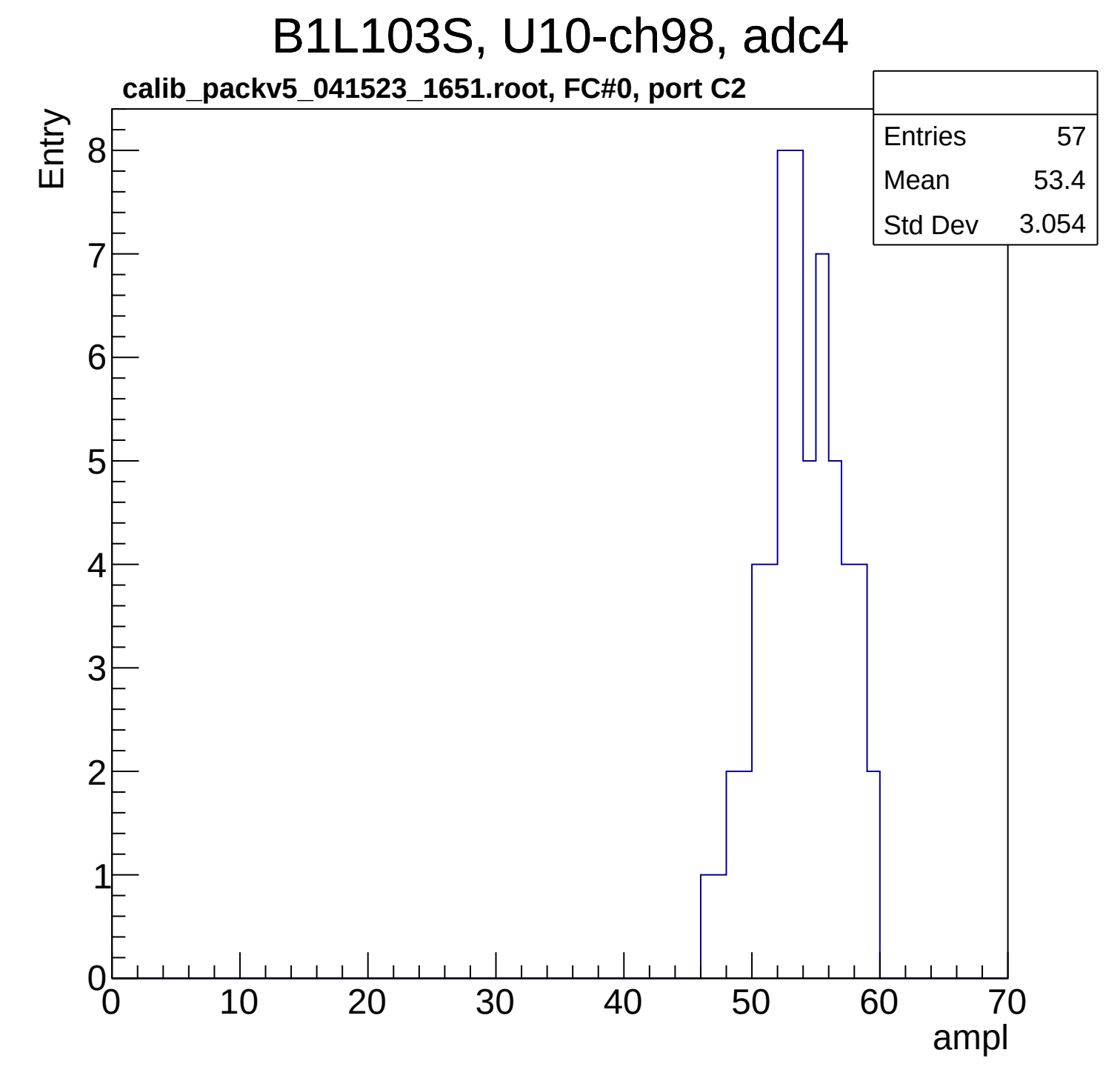

B1L103S, U10-ch97, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 1.278
Std Dev 5.268
Entry
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl

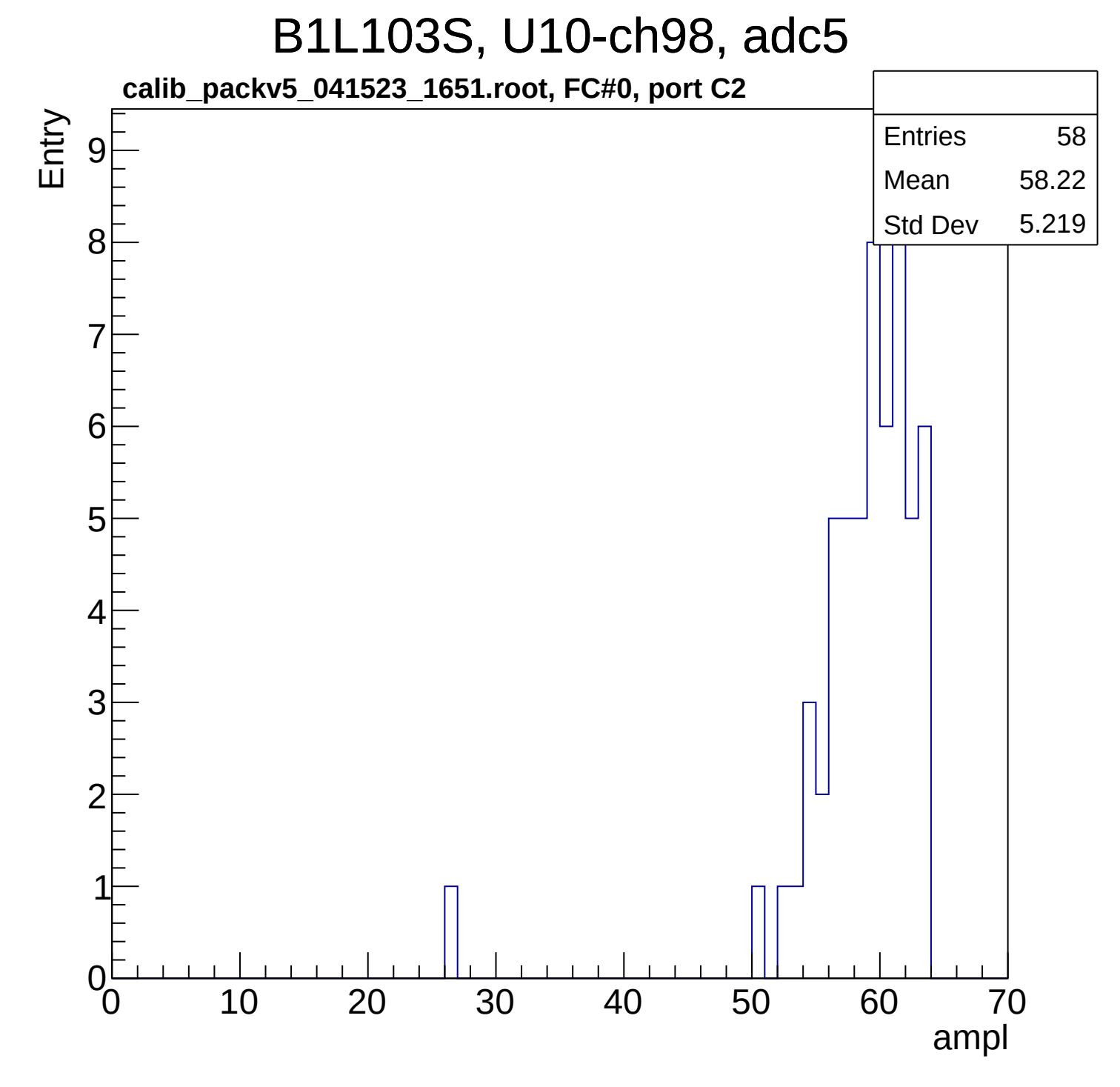

B1L103S, U10-ch98, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 21.29
Std Dev 12.74
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
22
0
10
20
30
40
50
60
70


B1L103S, U10-ch98, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 28.25
Std Dev 13.06
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch98, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 40.32
Std Dev 7.738
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U10-ch98, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 47.65
Std Dev 3.116
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U10-ch98, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 53.4
Std Dev 3.054
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U10-ch98, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 58.22
Std Dev 5.219
Entry
ampl
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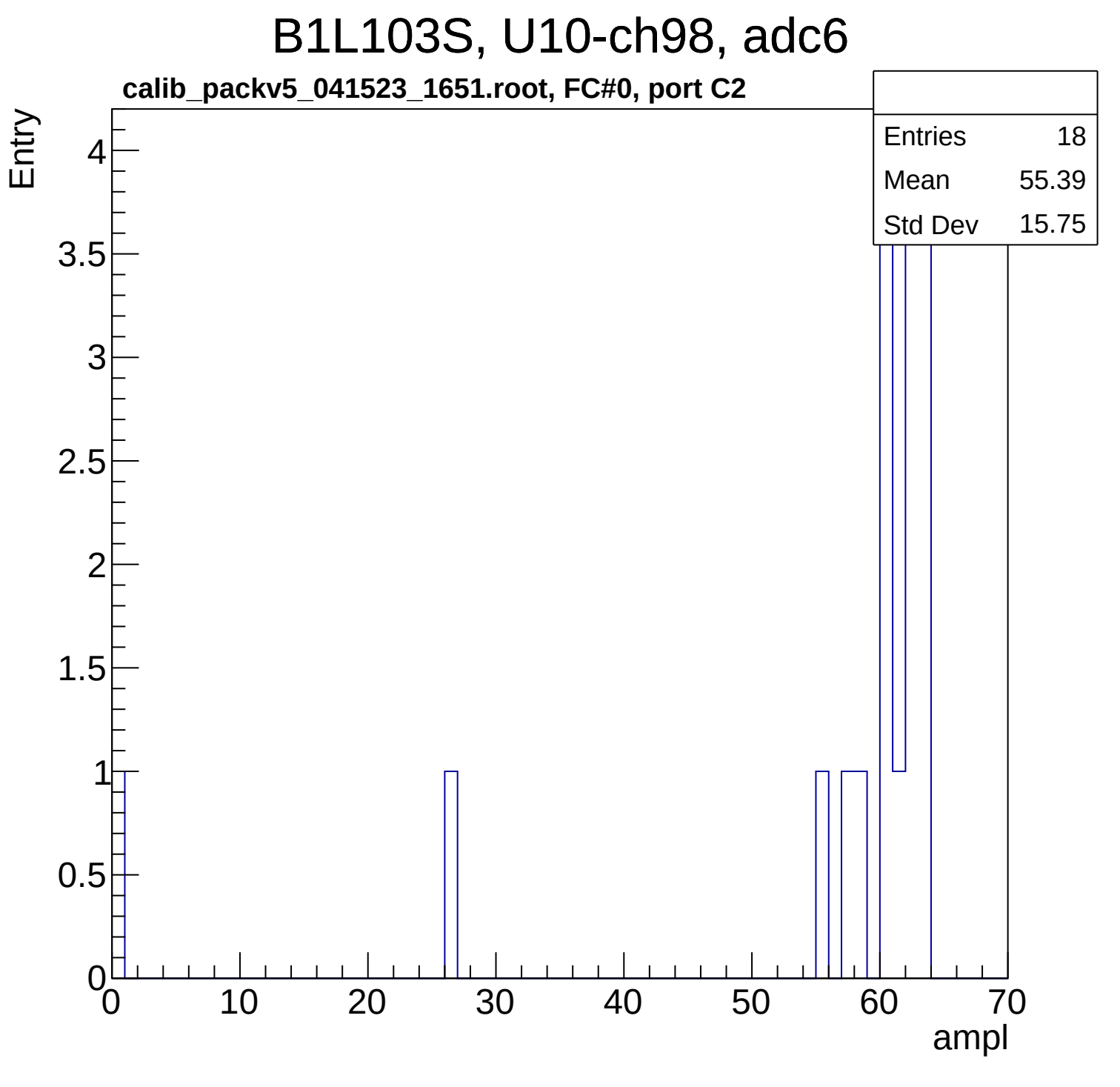
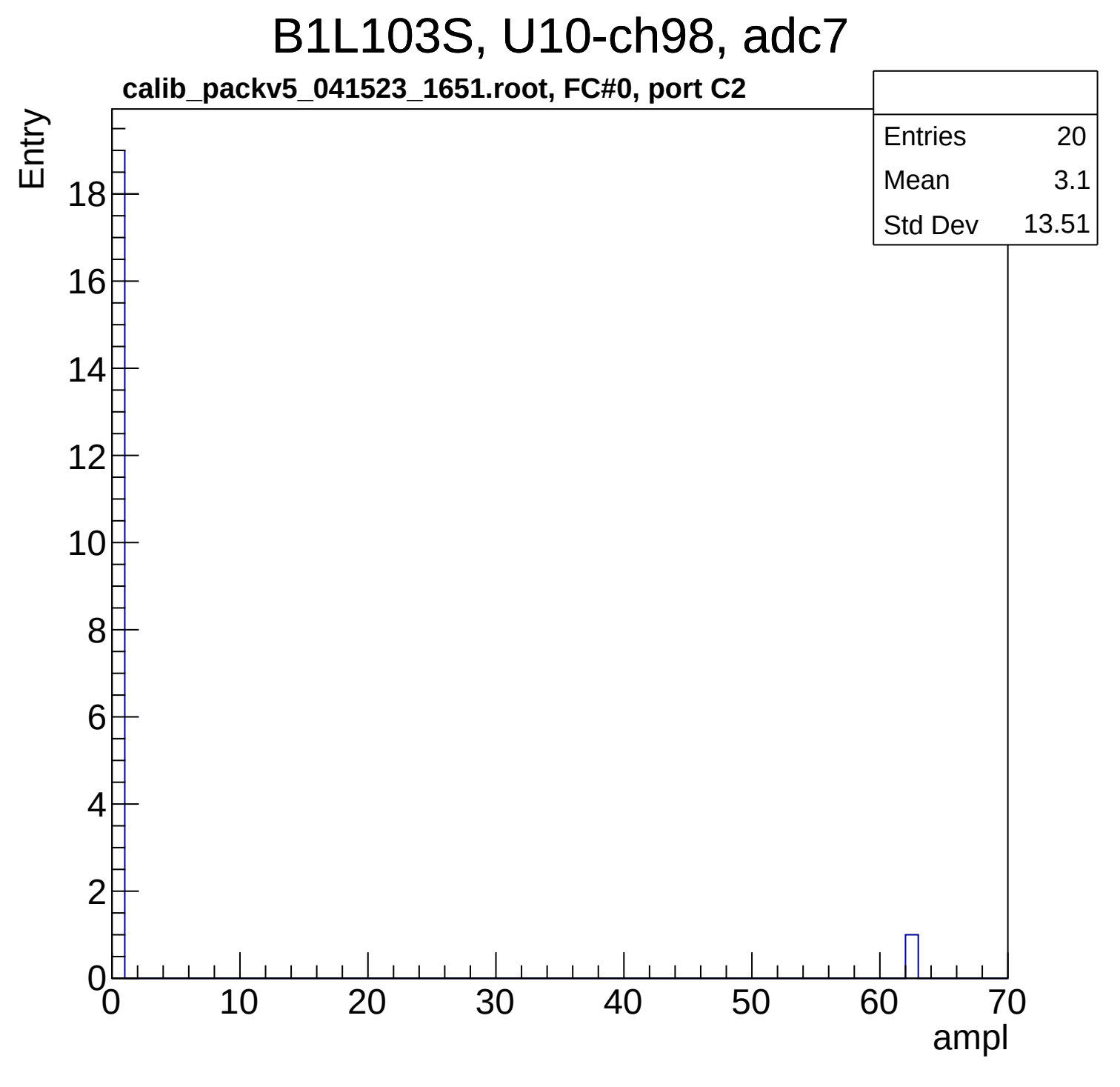
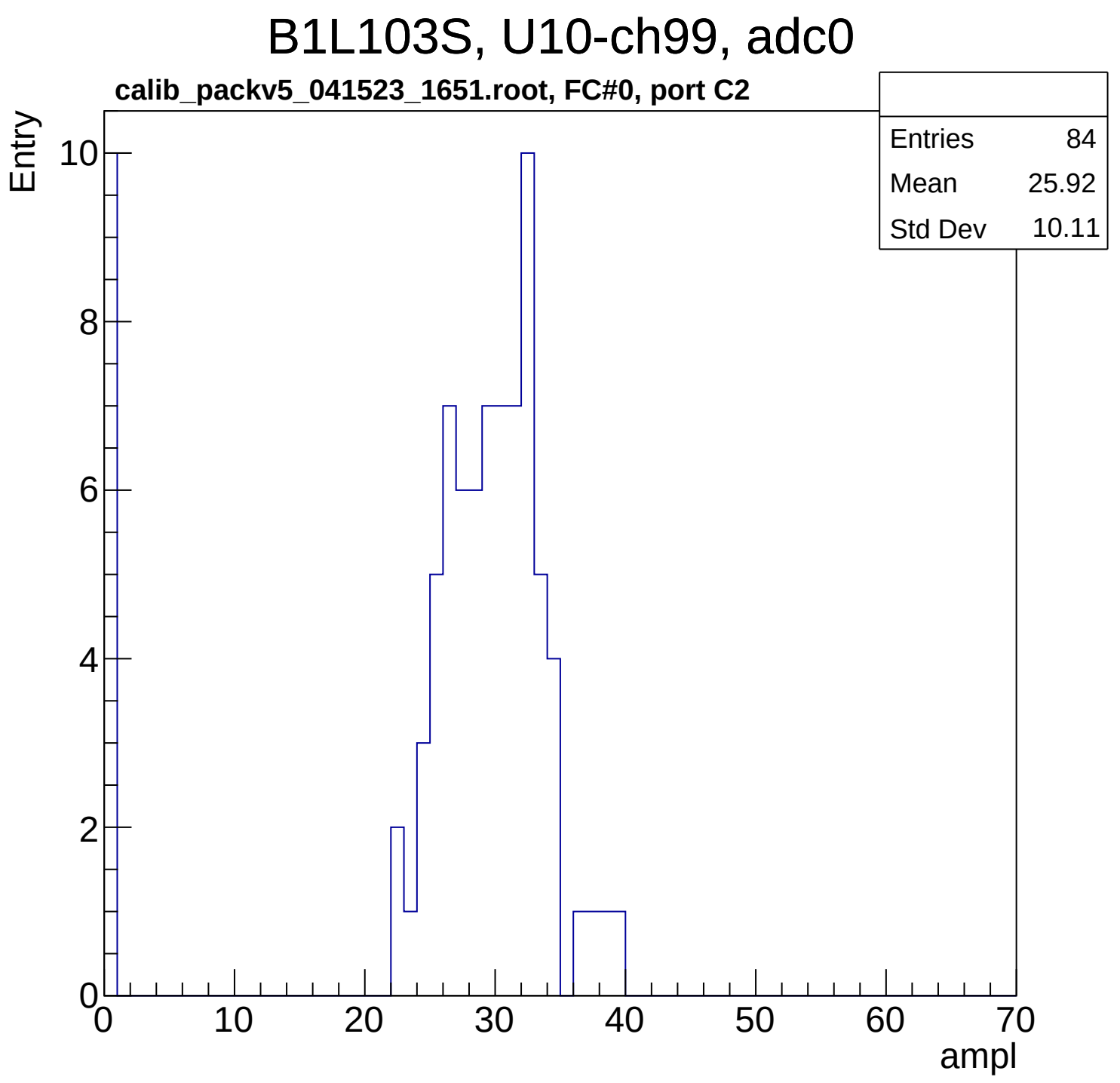
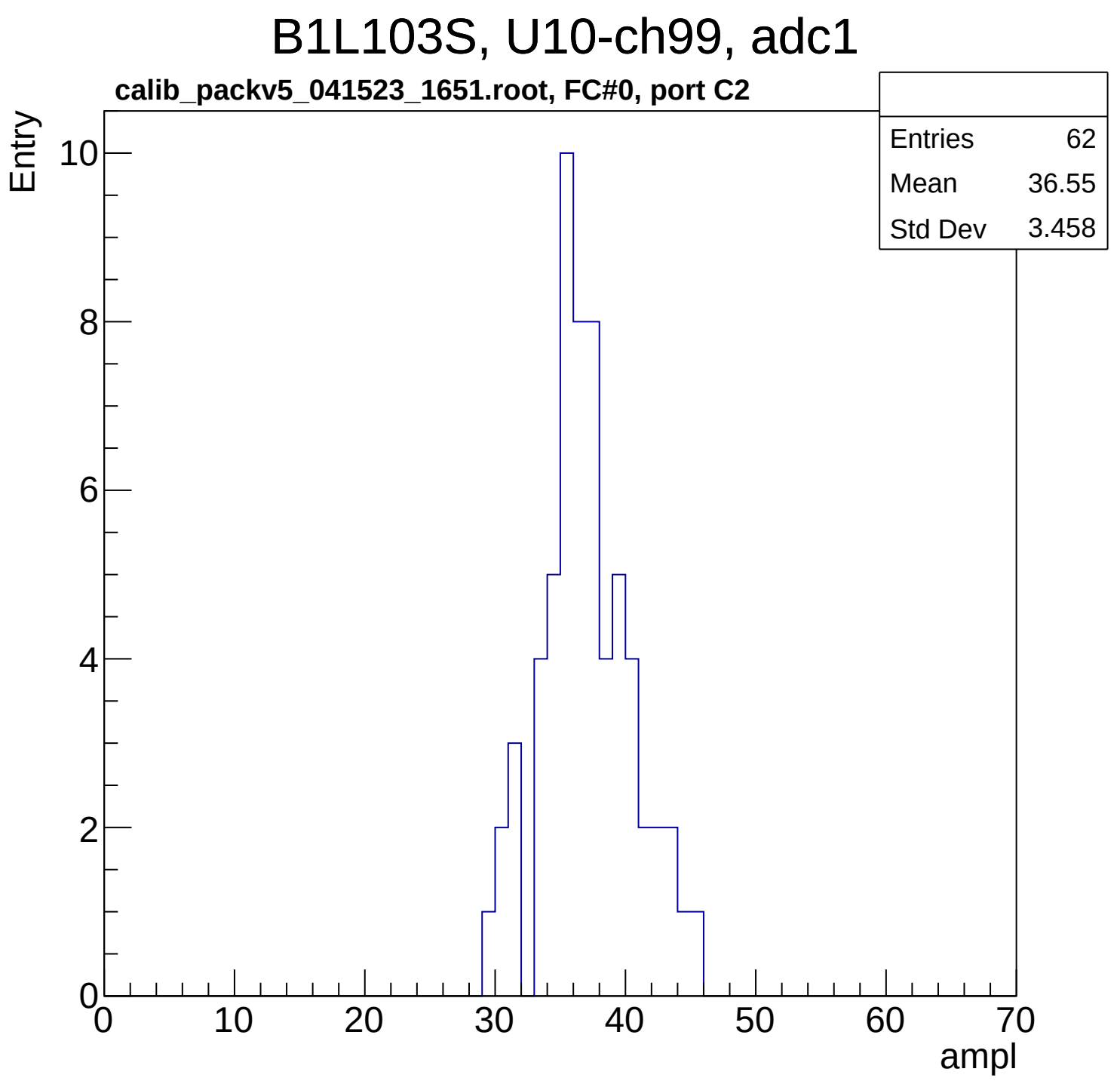
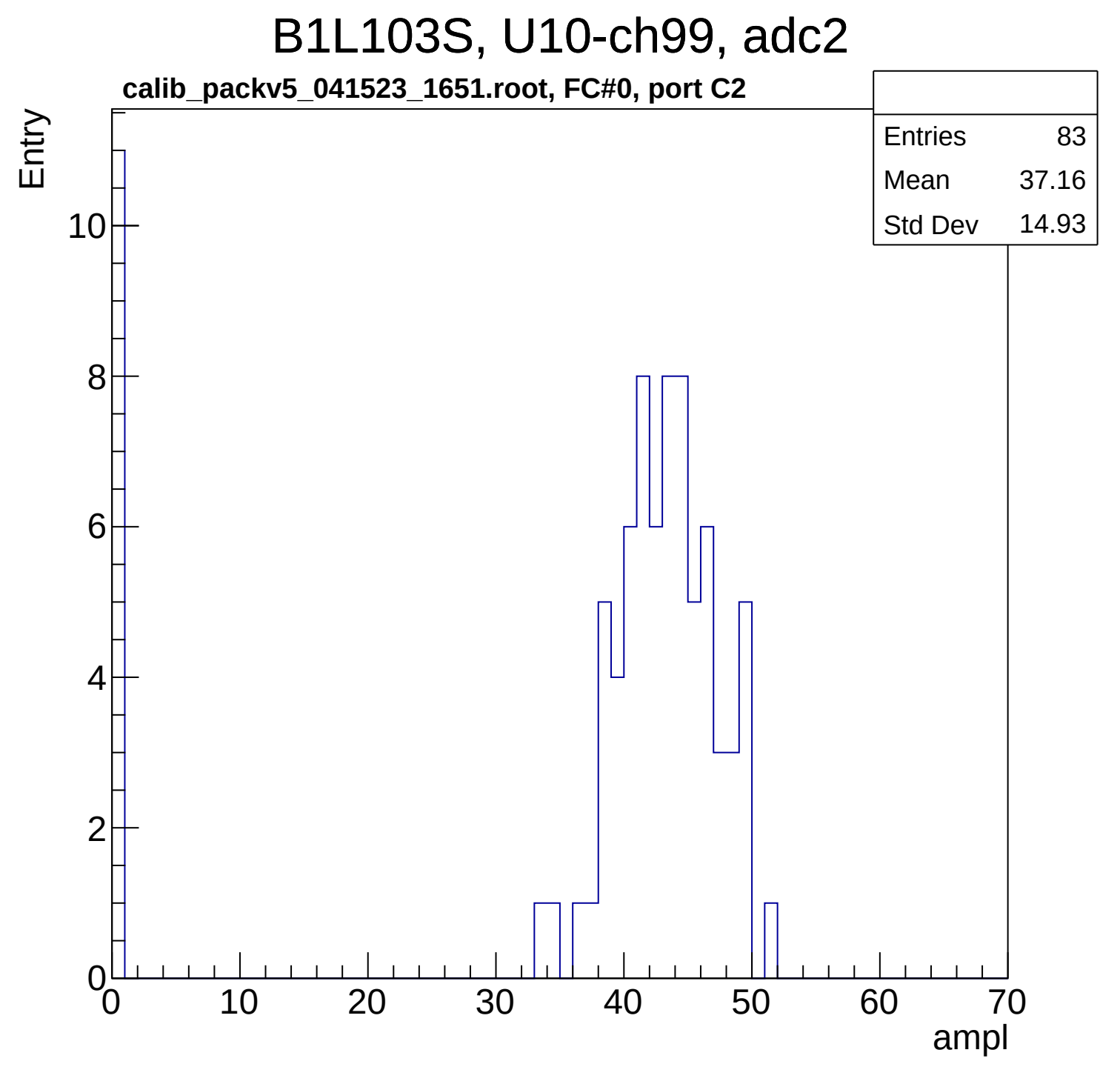
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

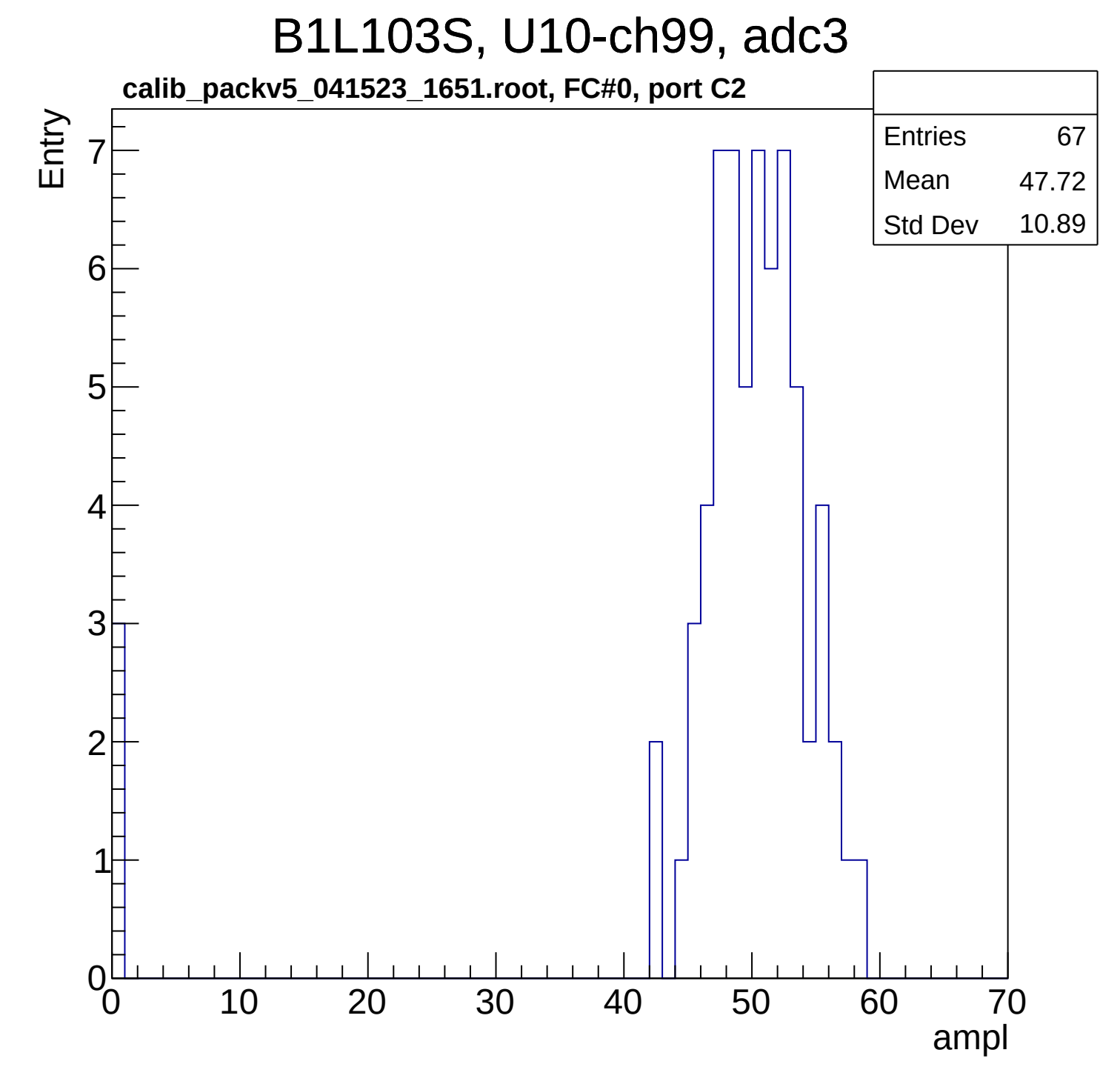

B1L103S, U10-ch98, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 55.39
Std Dev 15.75
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

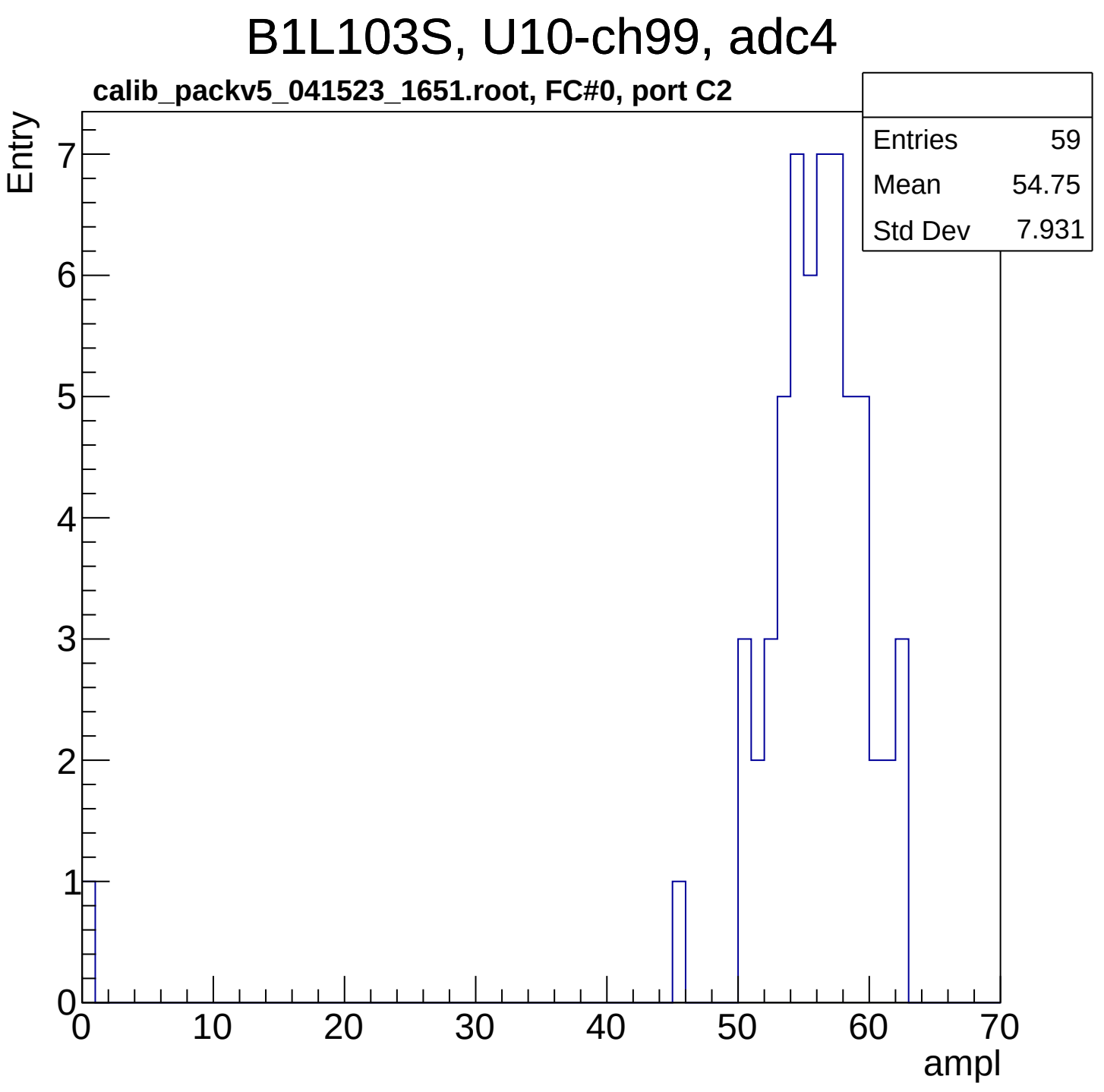

B1L103S, U10-ch98, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.1
Std Dev 13.51
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

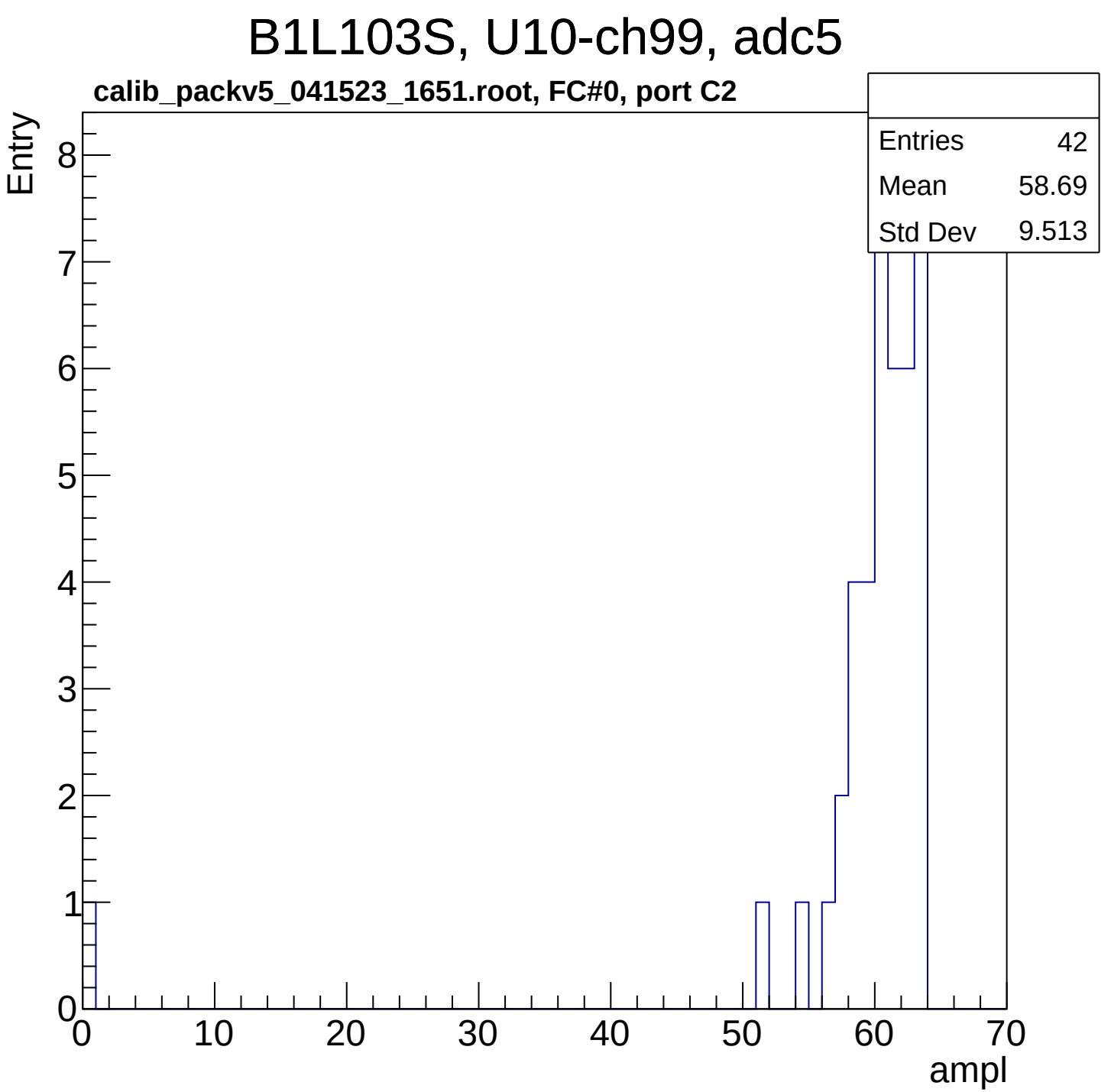

B1L103S, U10-ch99, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 25.92
Std Dev 10.11
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U10-ch99, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 36.55
Std Dev 3.458
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U10-ch99, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 37.16
Std Dev 14.93
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch99, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 47.72
Std Dev 10.89
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U10-ch99, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 54.75
Std Dev 7.931
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U10-ch99, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 42
Mean 58.69
Std Dev 9.513
Entry
ampl
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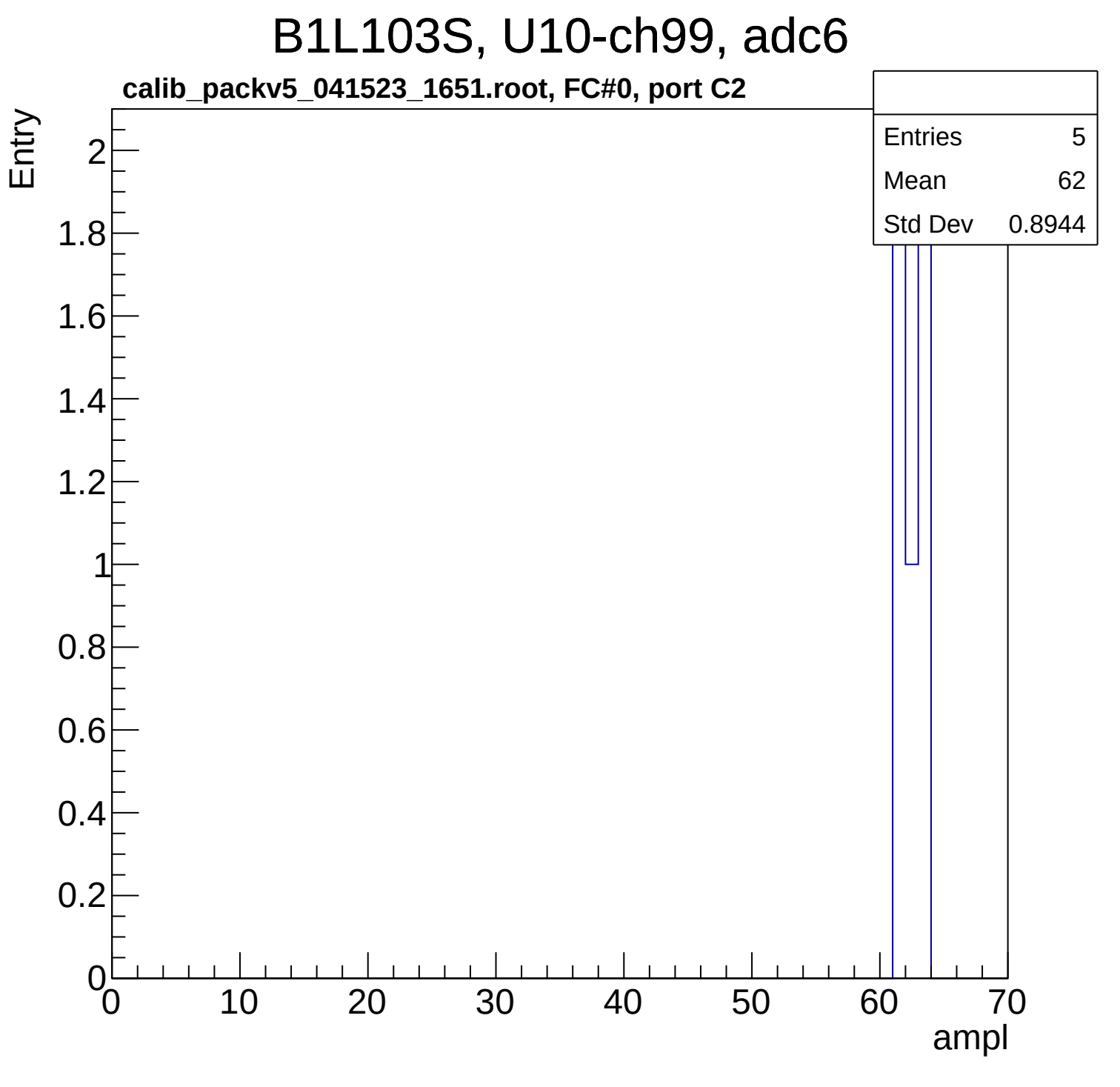
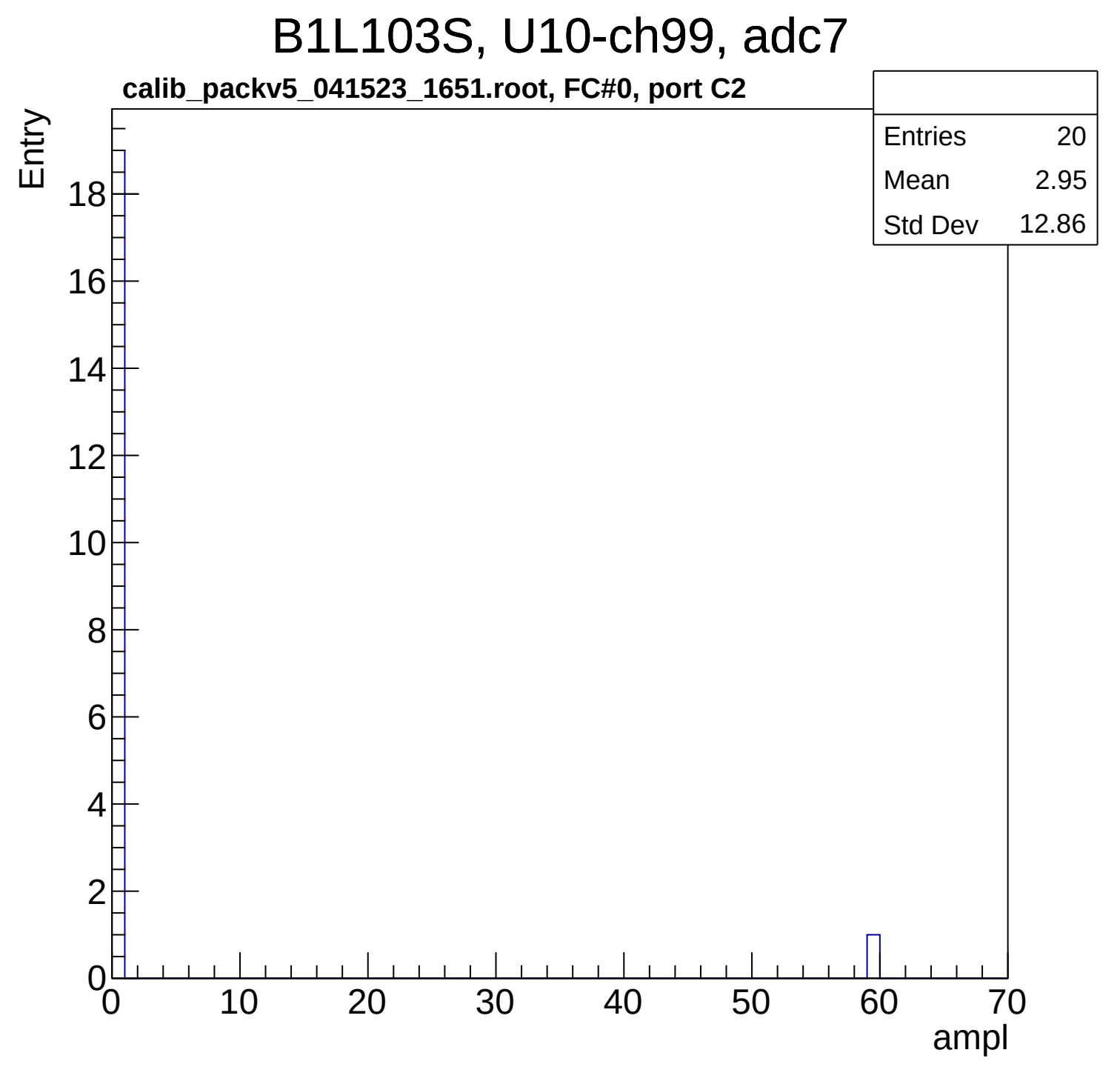
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U10-ch99, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 5
Mean 62
Std Dev 0.8944
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U10-ch99, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 2.95
Std Dev 12.86
Entry
0
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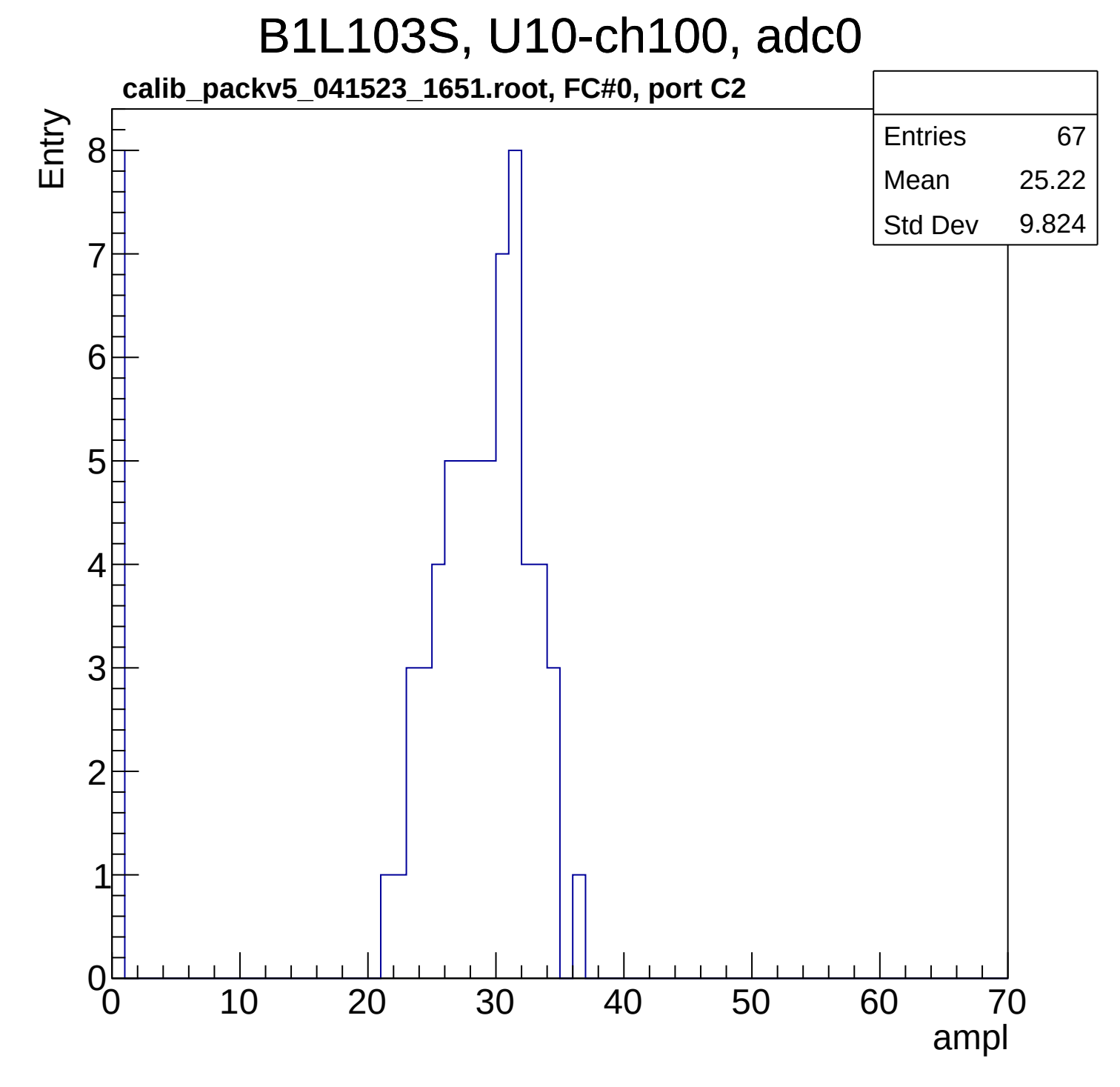
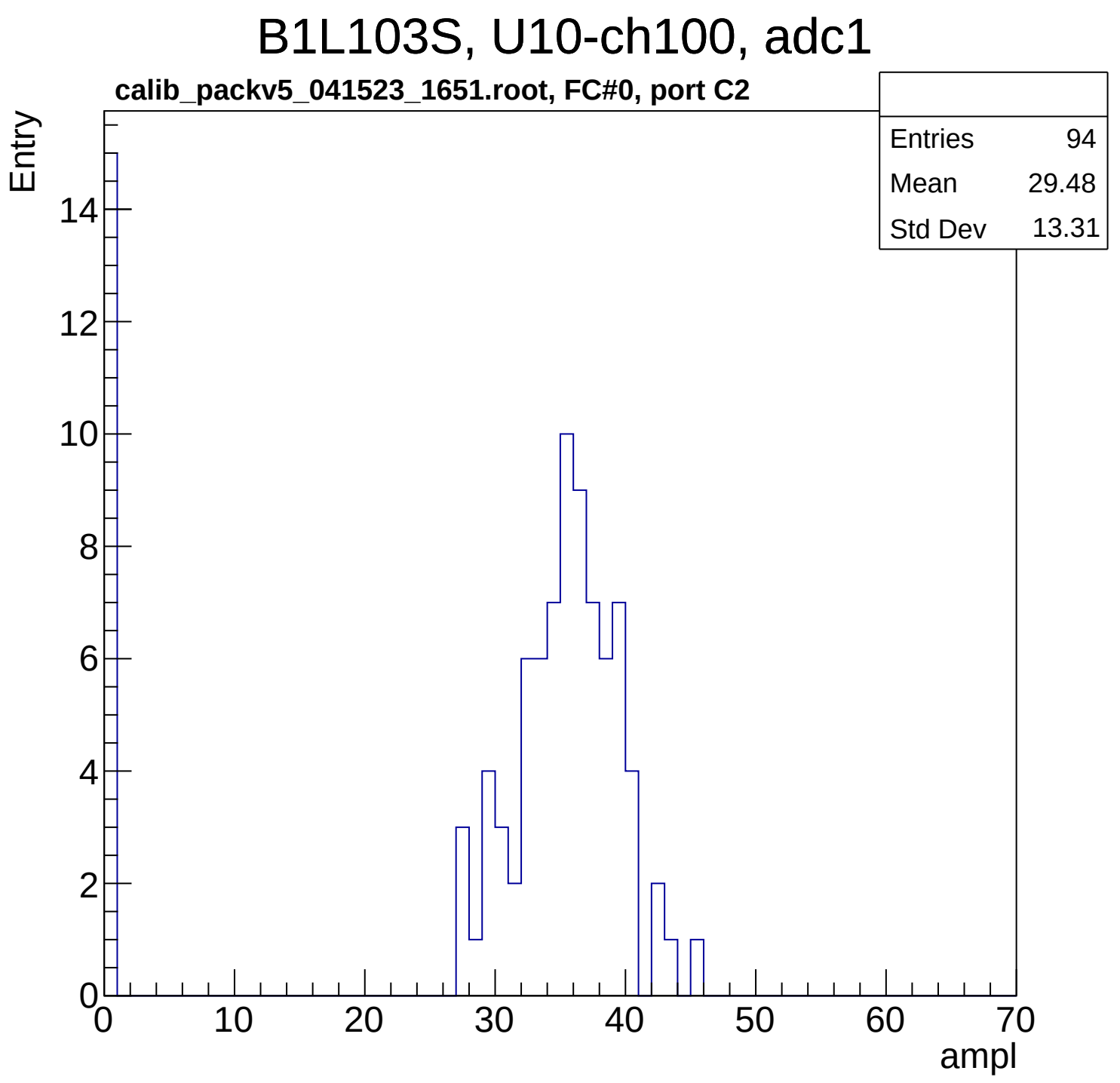
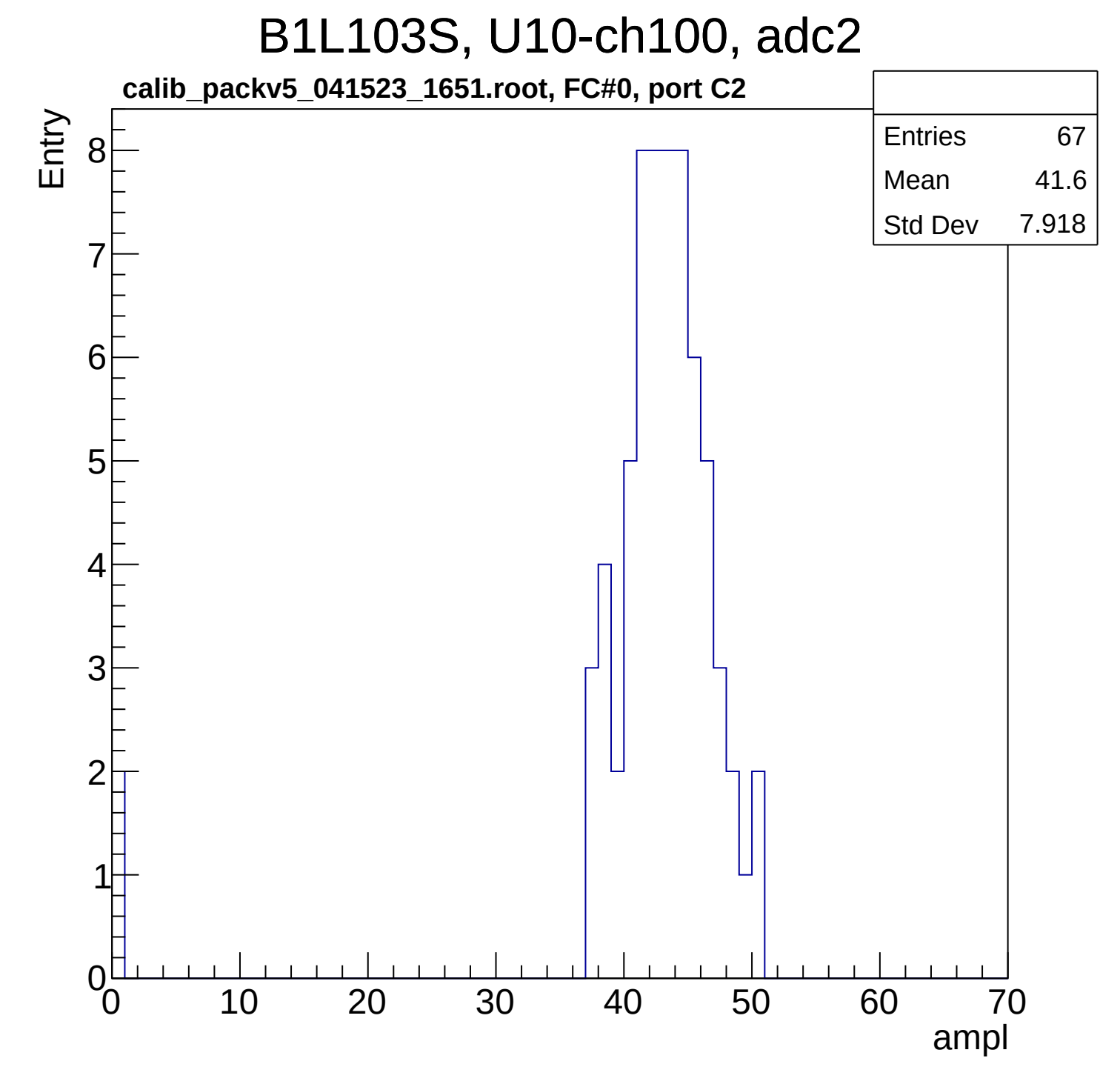
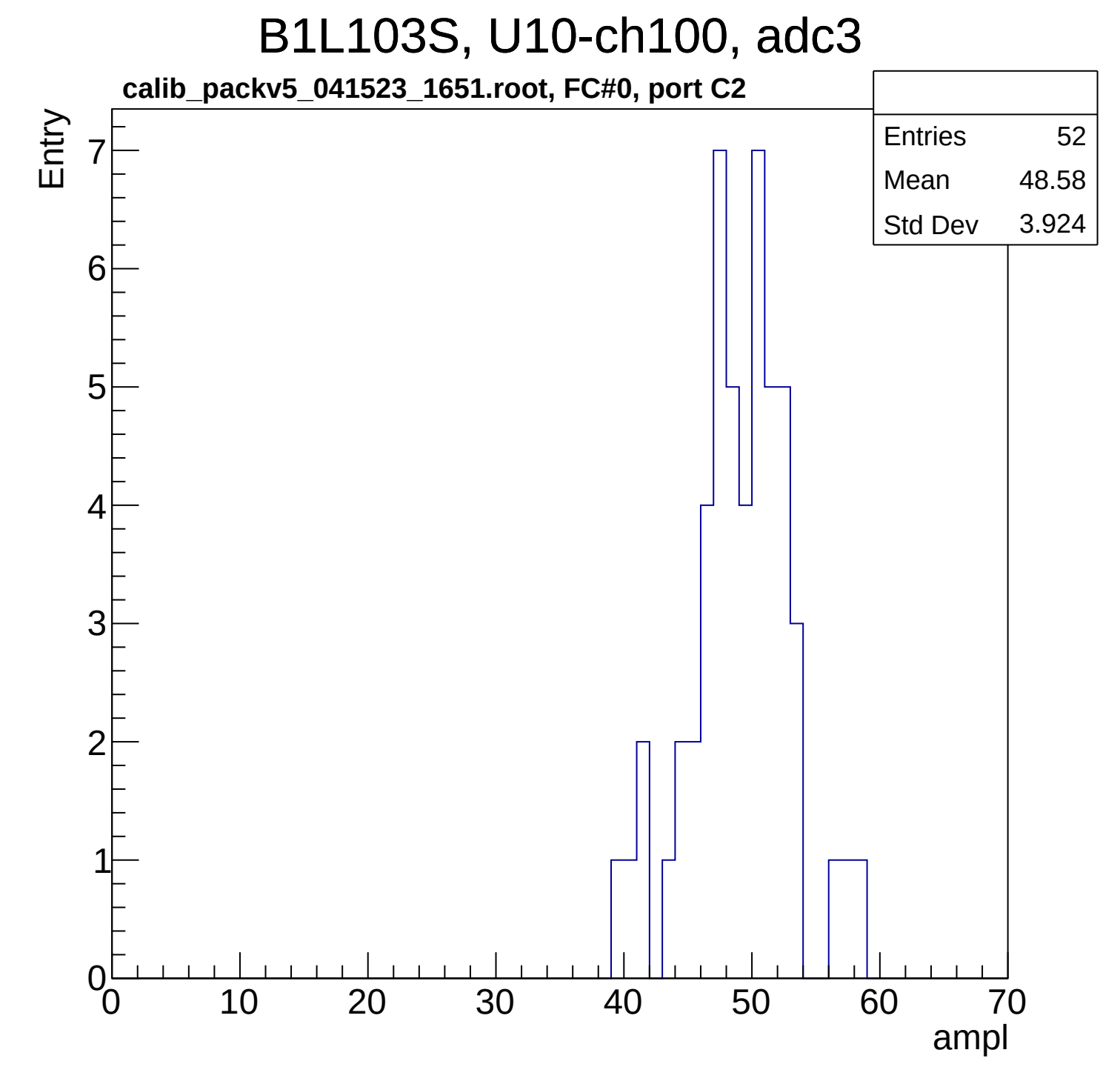
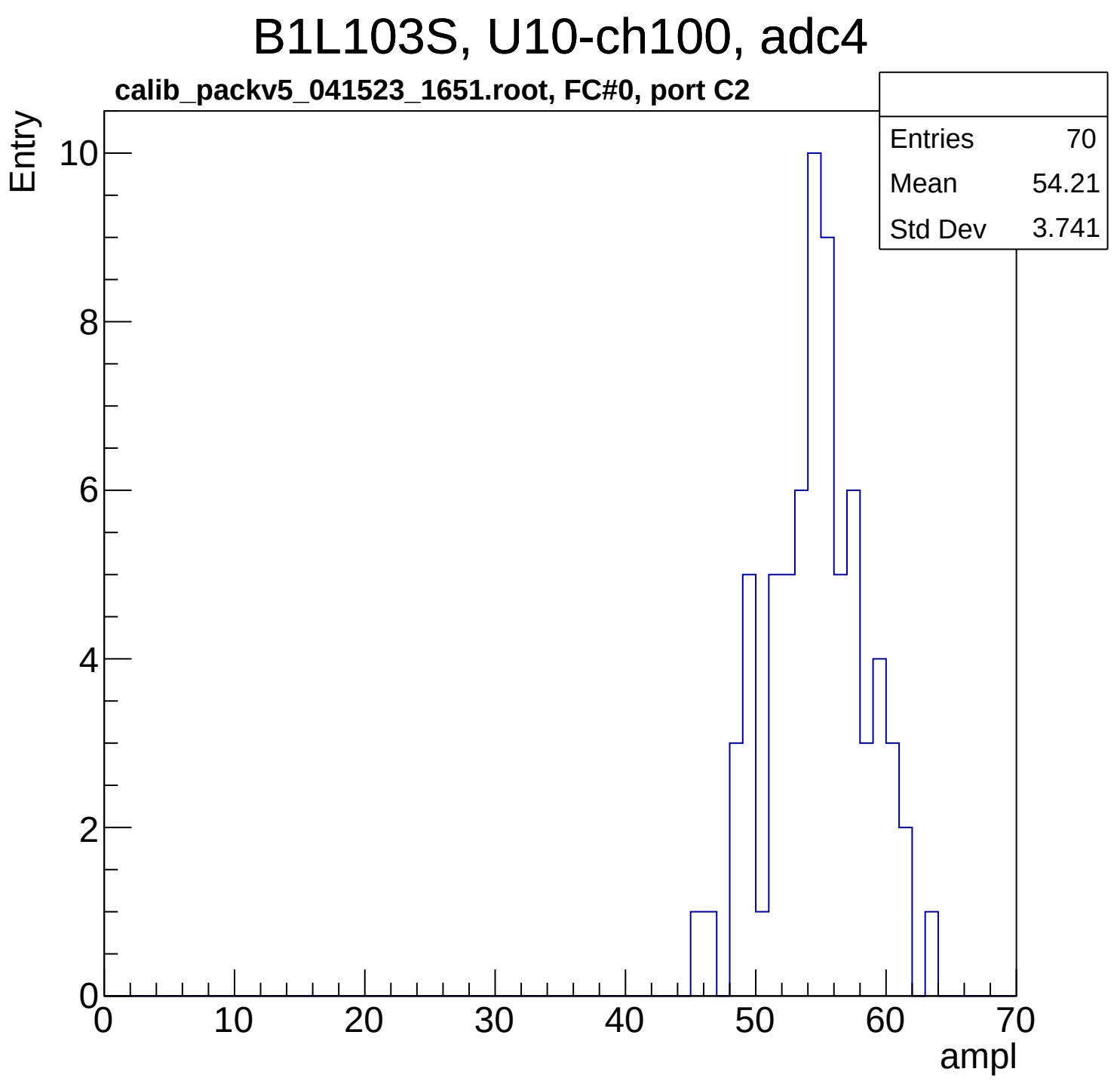
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

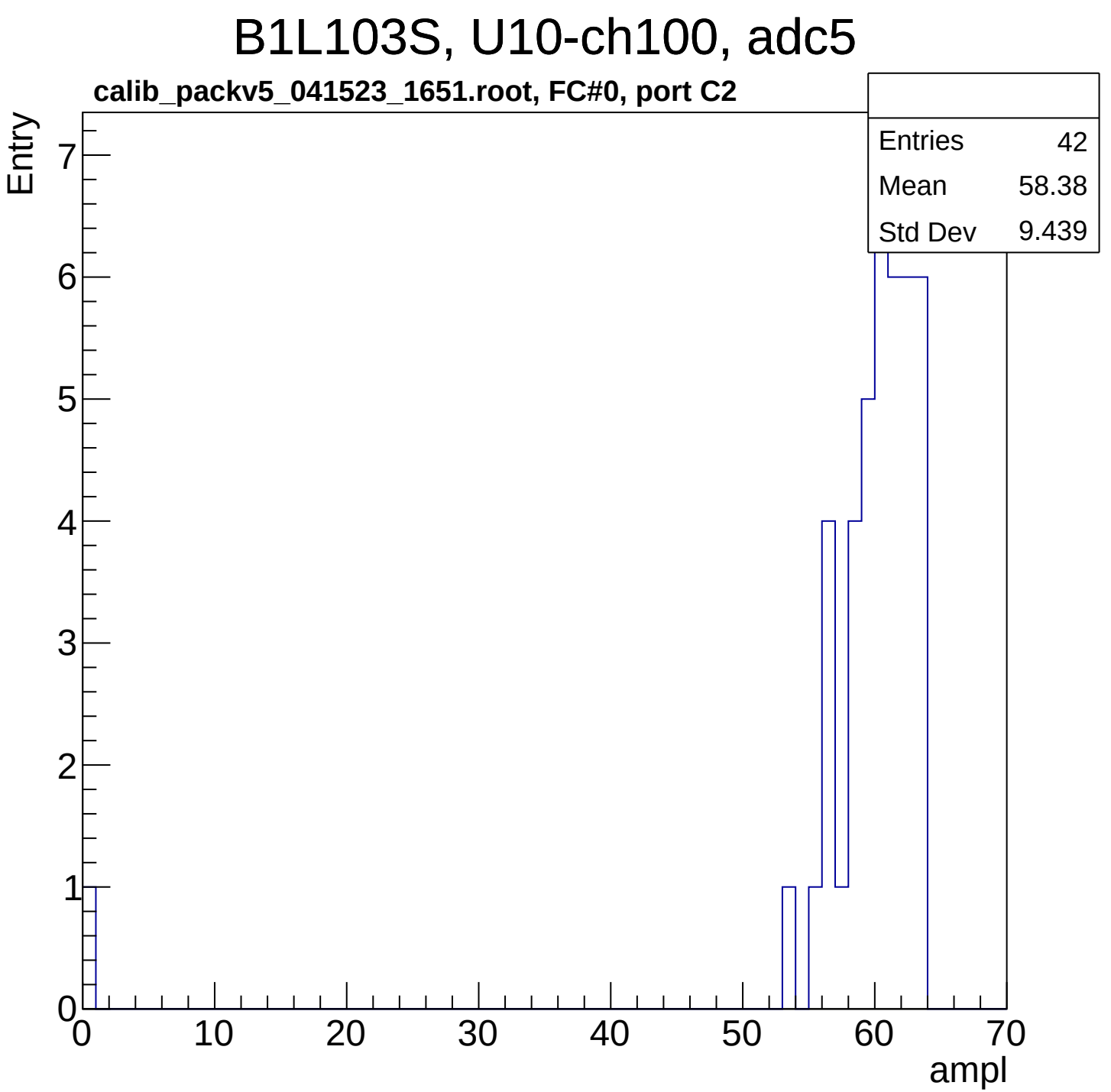

B1L103S, U10-ch100, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 25.22
Std Dev 9.824
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

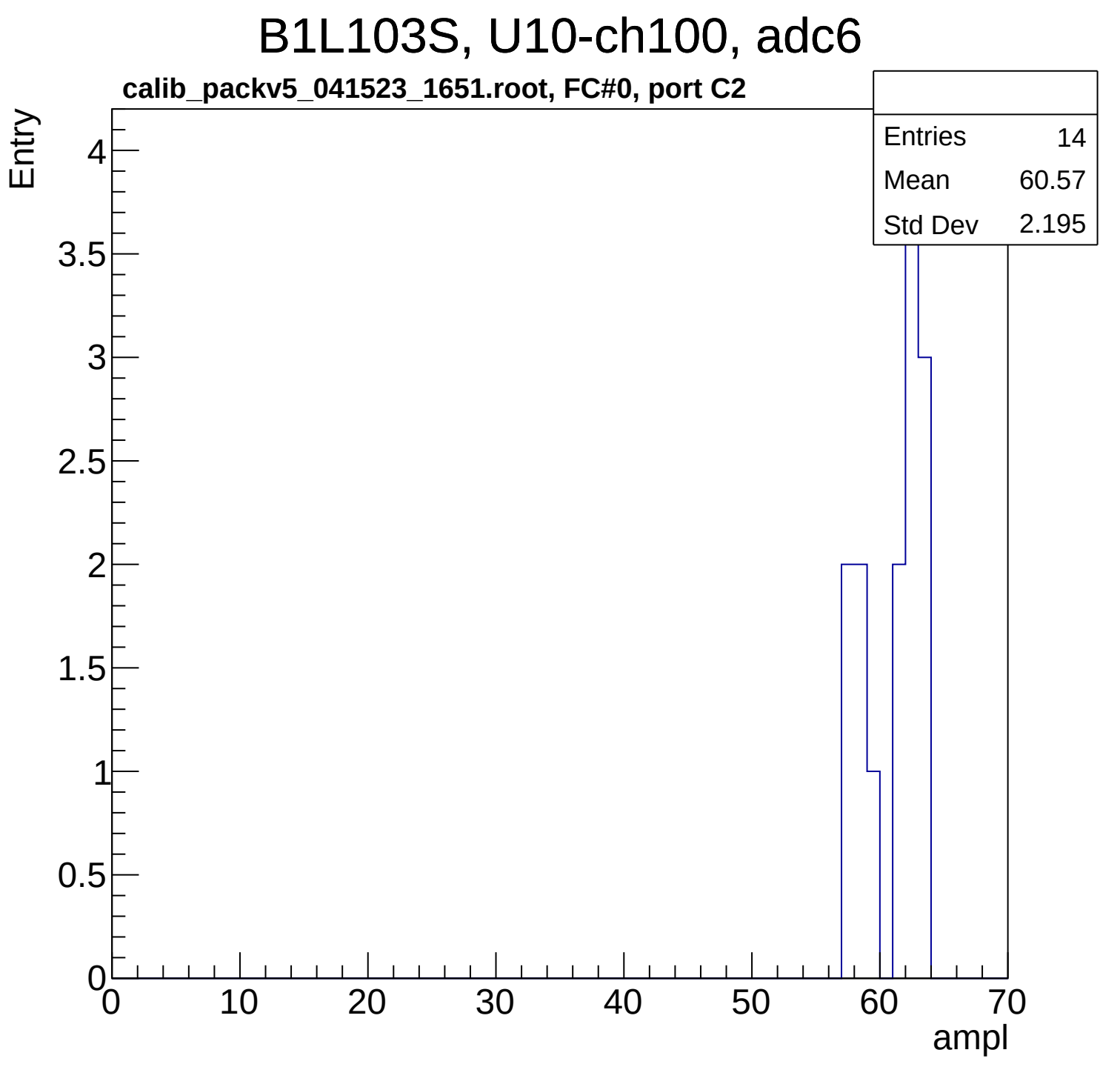

B1L103S, U10-ch100, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 94
Mean 29.48
Std Dev 13.31
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch100, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 41.6
Std Dev 7.918
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U10-ch100, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 48.58
Std Dev 3.924
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U10-ch100, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 54.21
Std Dev 3.741
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U10-ch100, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 42
Mean 58.38
Std Dev 9.439
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U10-ch100, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 14
Mean 60.57
Std Dev 2.195
Entry
ampl
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1.5
2
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3
3.5
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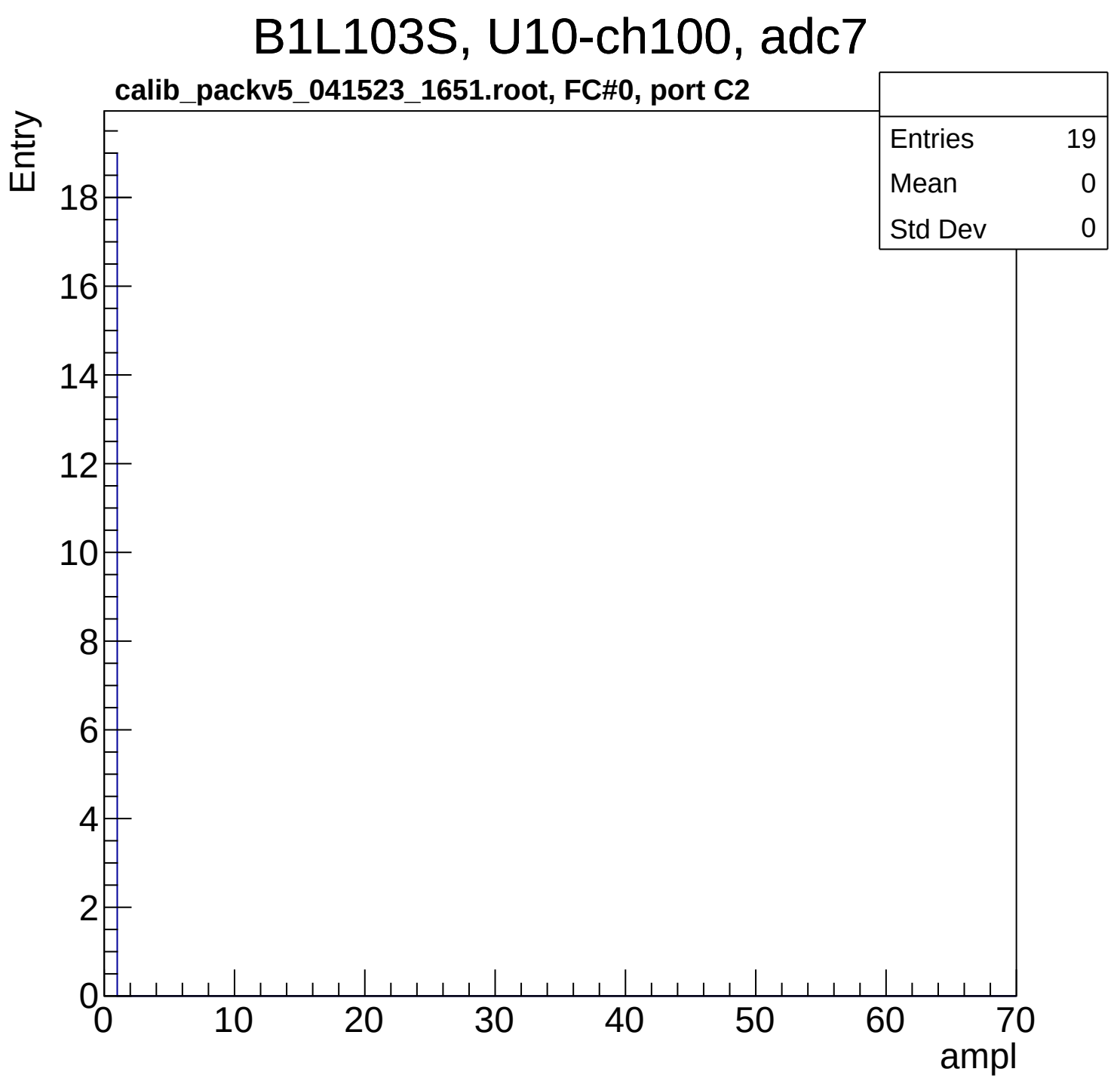
B1L103S, U10-ch100, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
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6
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10
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14
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50
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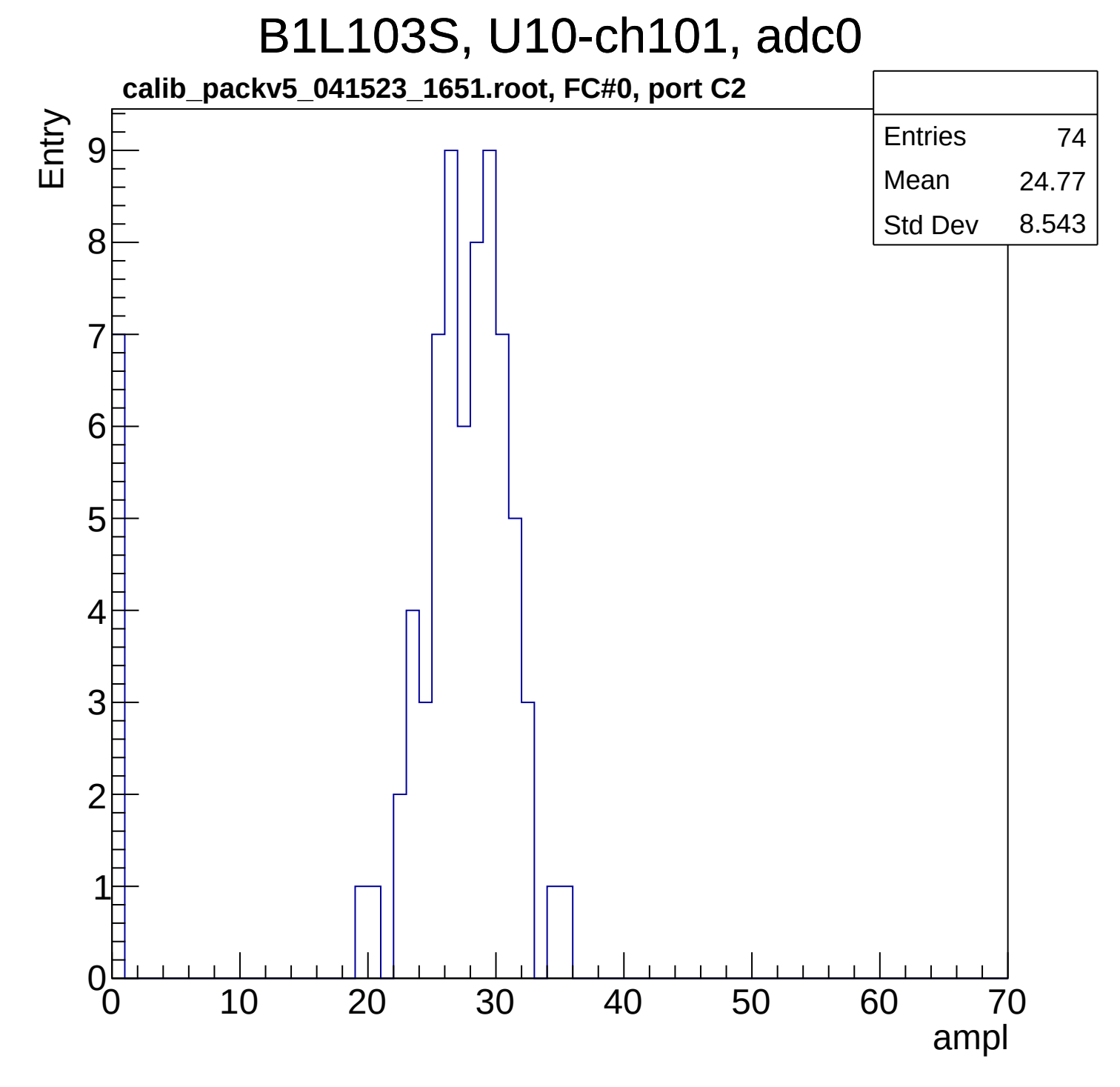
70
ampl


B1L103S, U10-ch101, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 24.77
Std Dev 8.543
Entry
ampl
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0
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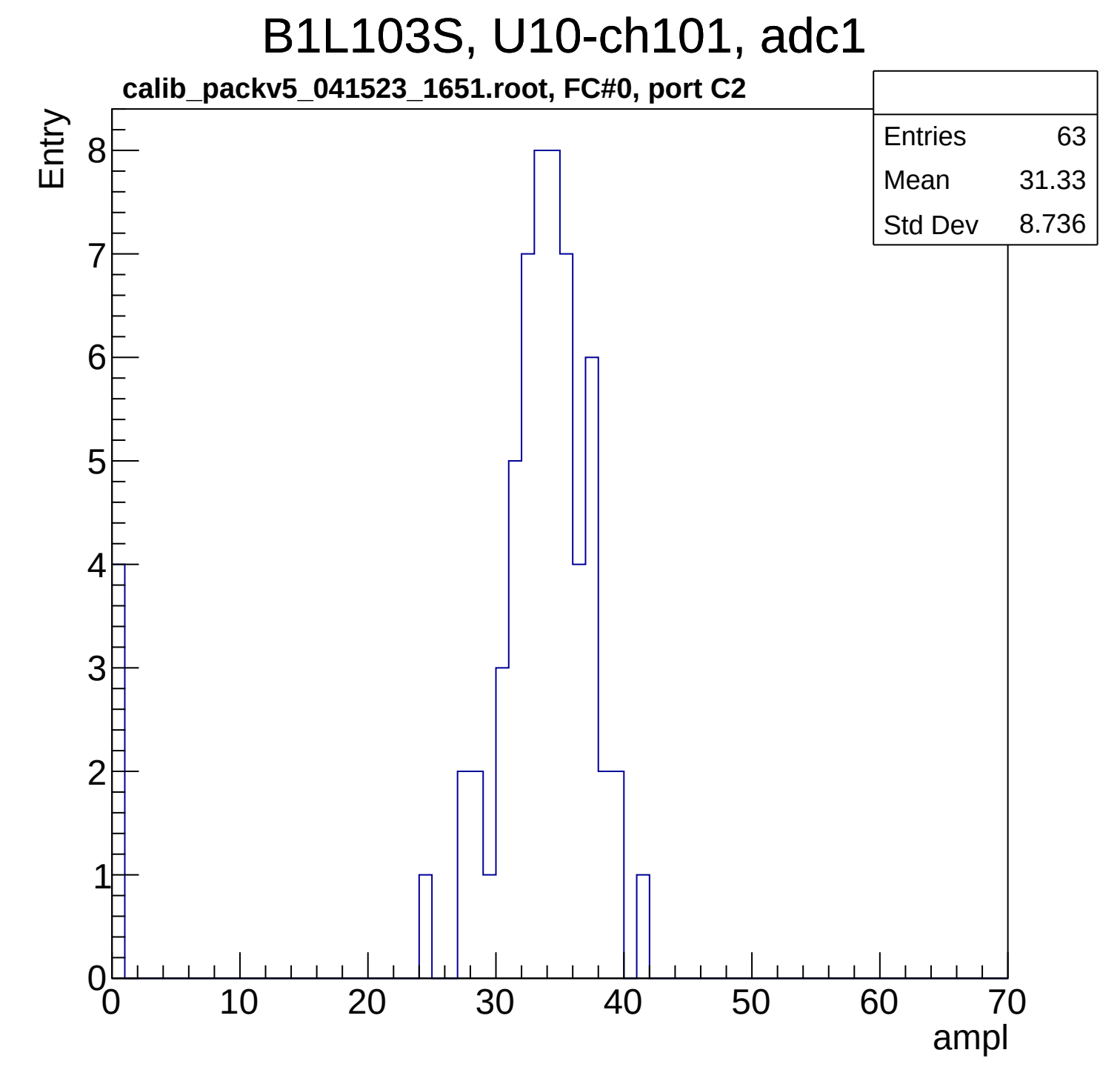
B1L103S, U10-ch101, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 31.33
Std Dev 8.736
Entry
ampl
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1
2
3
4
5
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7
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0
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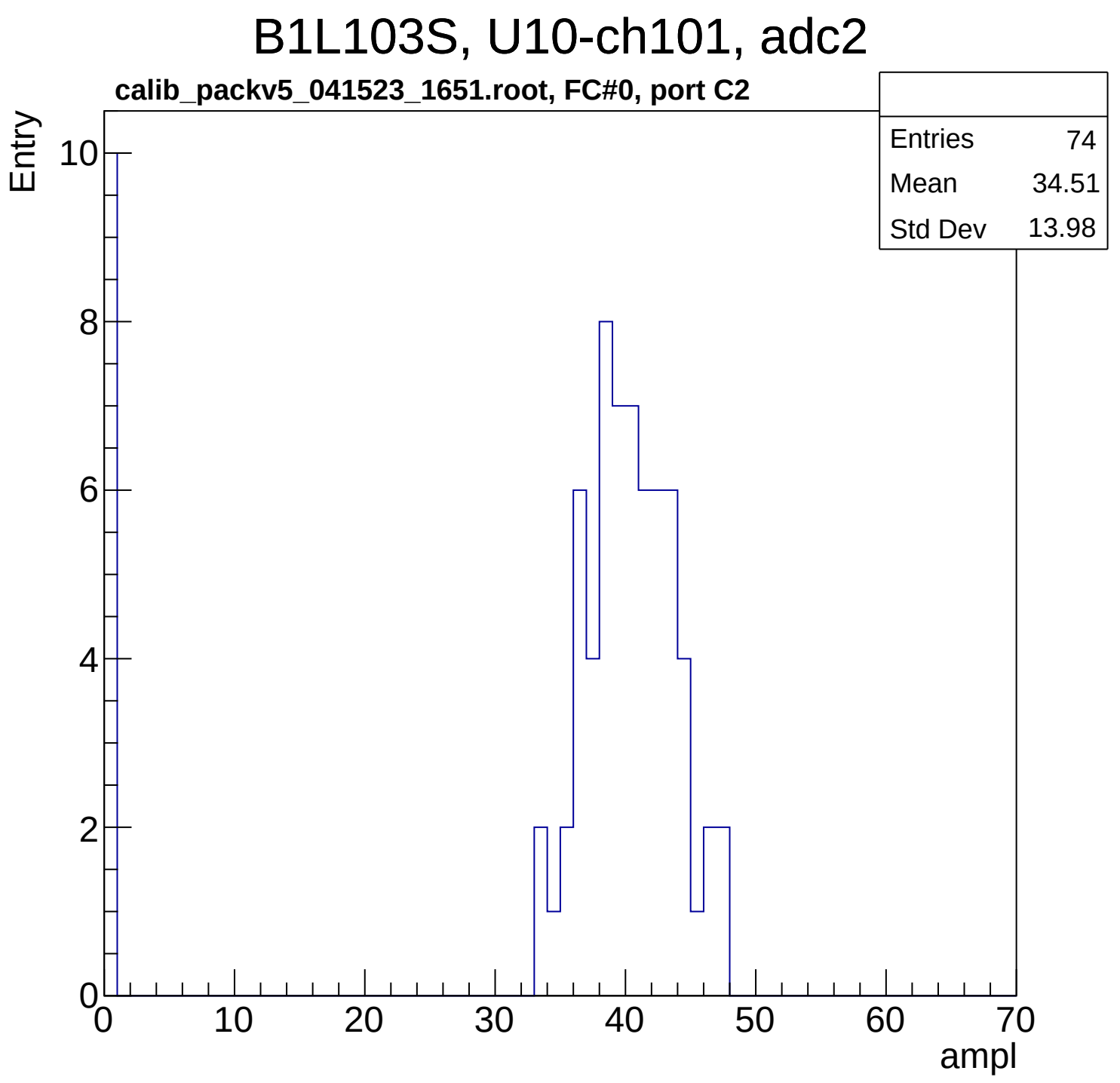
B1L103S, U10-ch101, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 34.51
Std Dev 13.98
Entry
0
2
4
6
8
10
0
10
20
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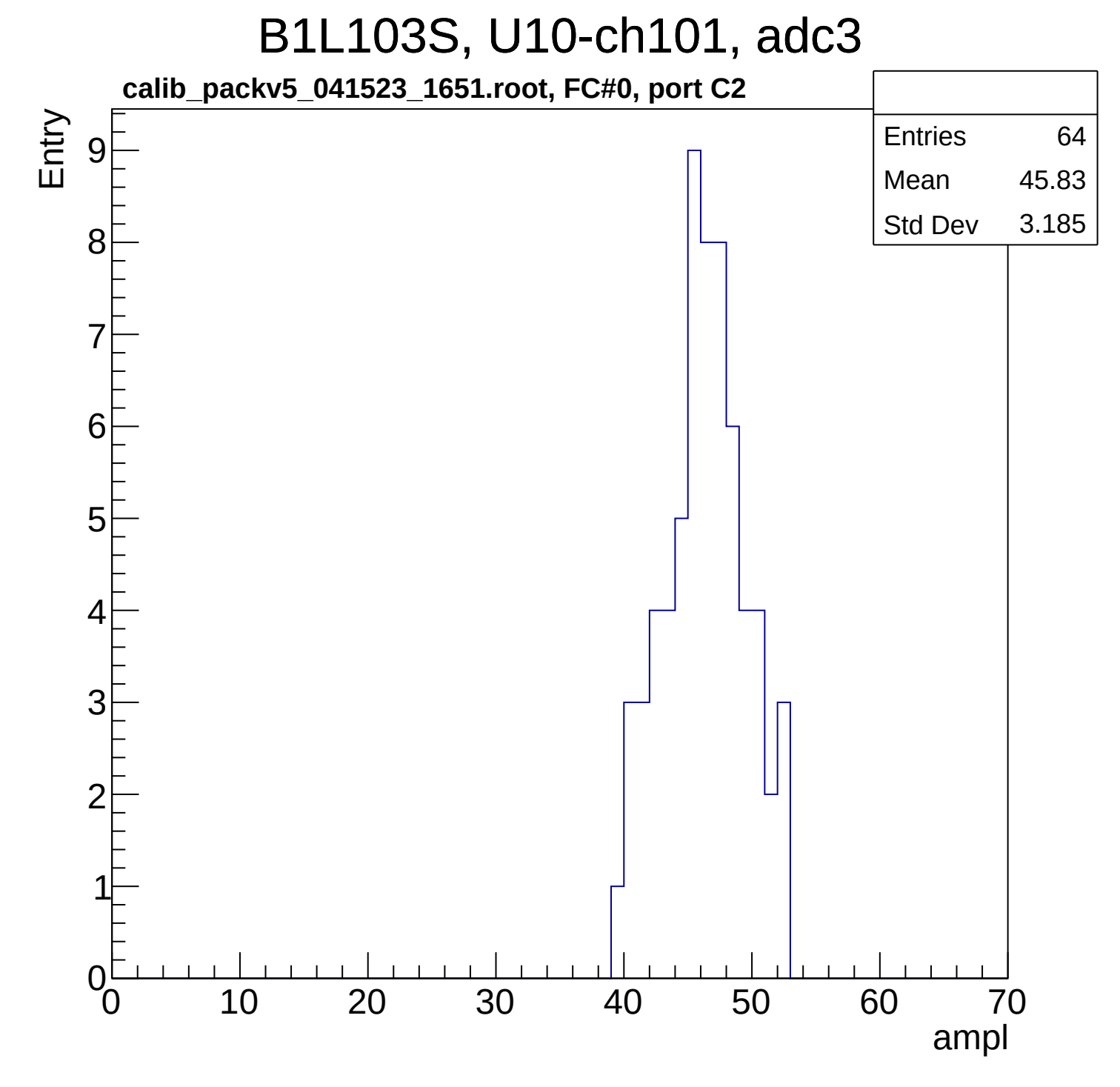
40
50
60
70
ampl


B1L103S, U10-ch101, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 45.83
Std Dev 3.185
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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30
40
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60
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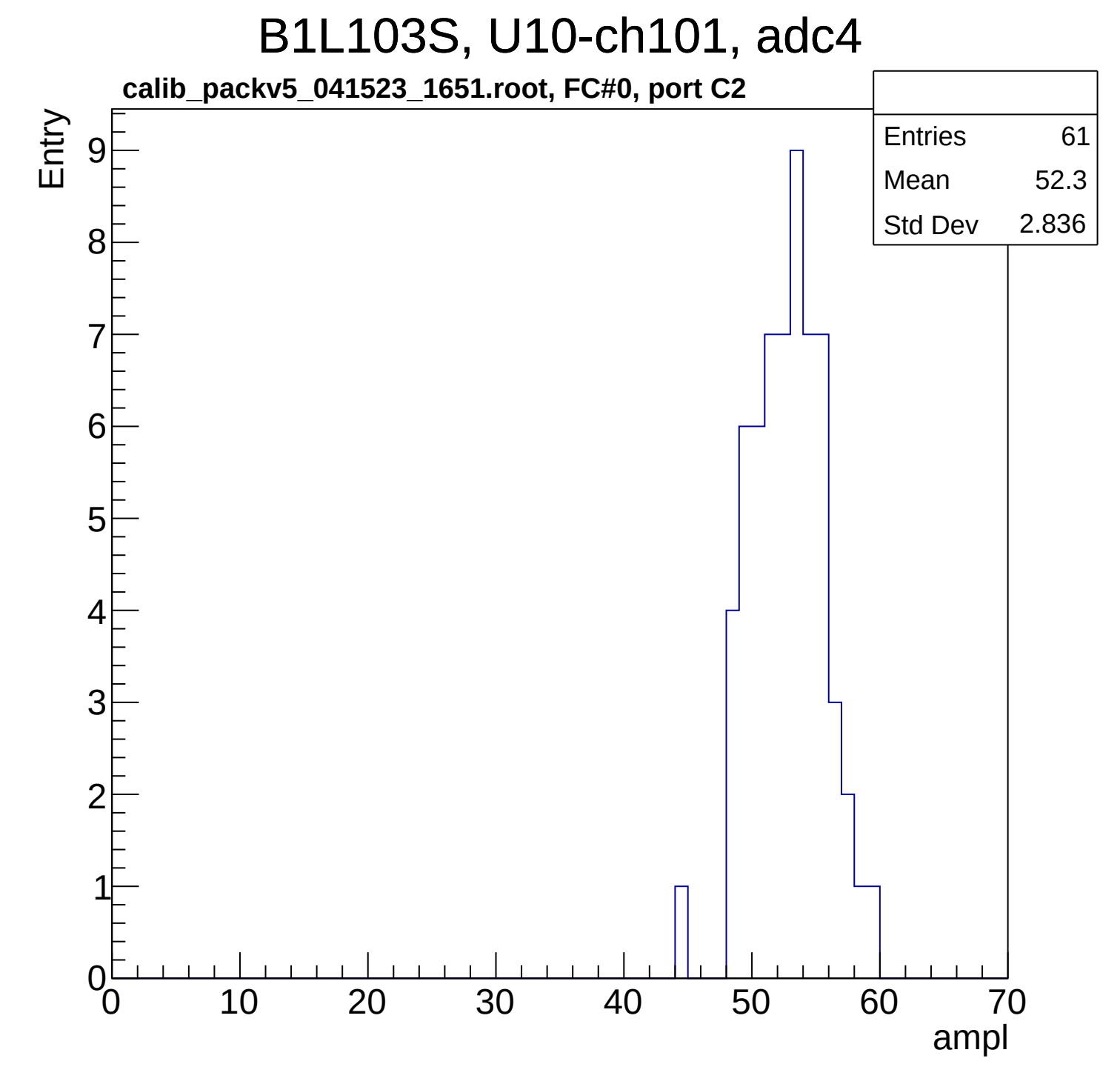
B1L103S, U10-ch101, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 52.3
Std Dev 2.836
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
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40
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60
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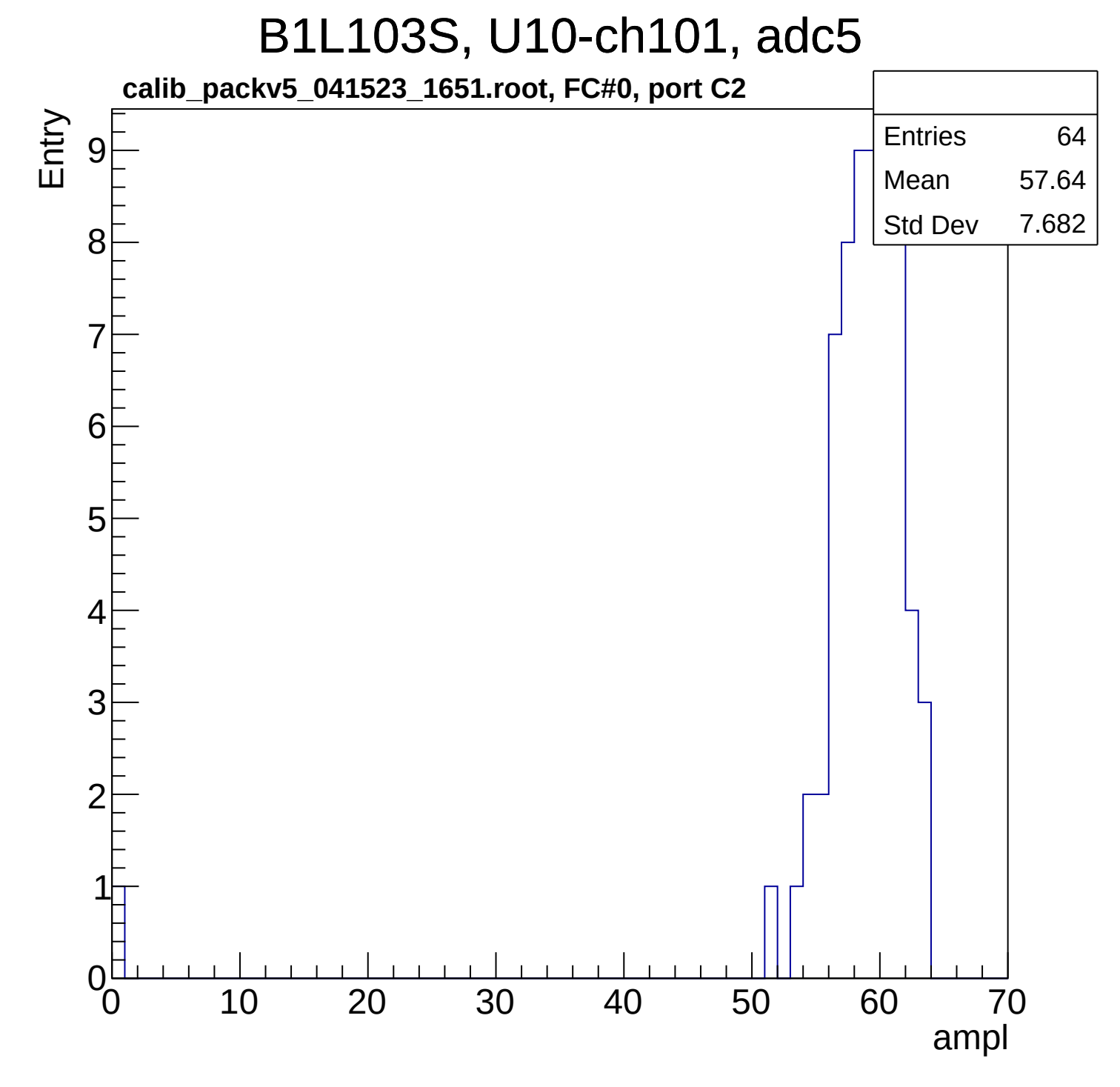
B1L103S, U10-ch101, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 57.64
Std Dev 7.682
Entry
ampl
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2
3
4
5
6
7
8
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0
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40
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60
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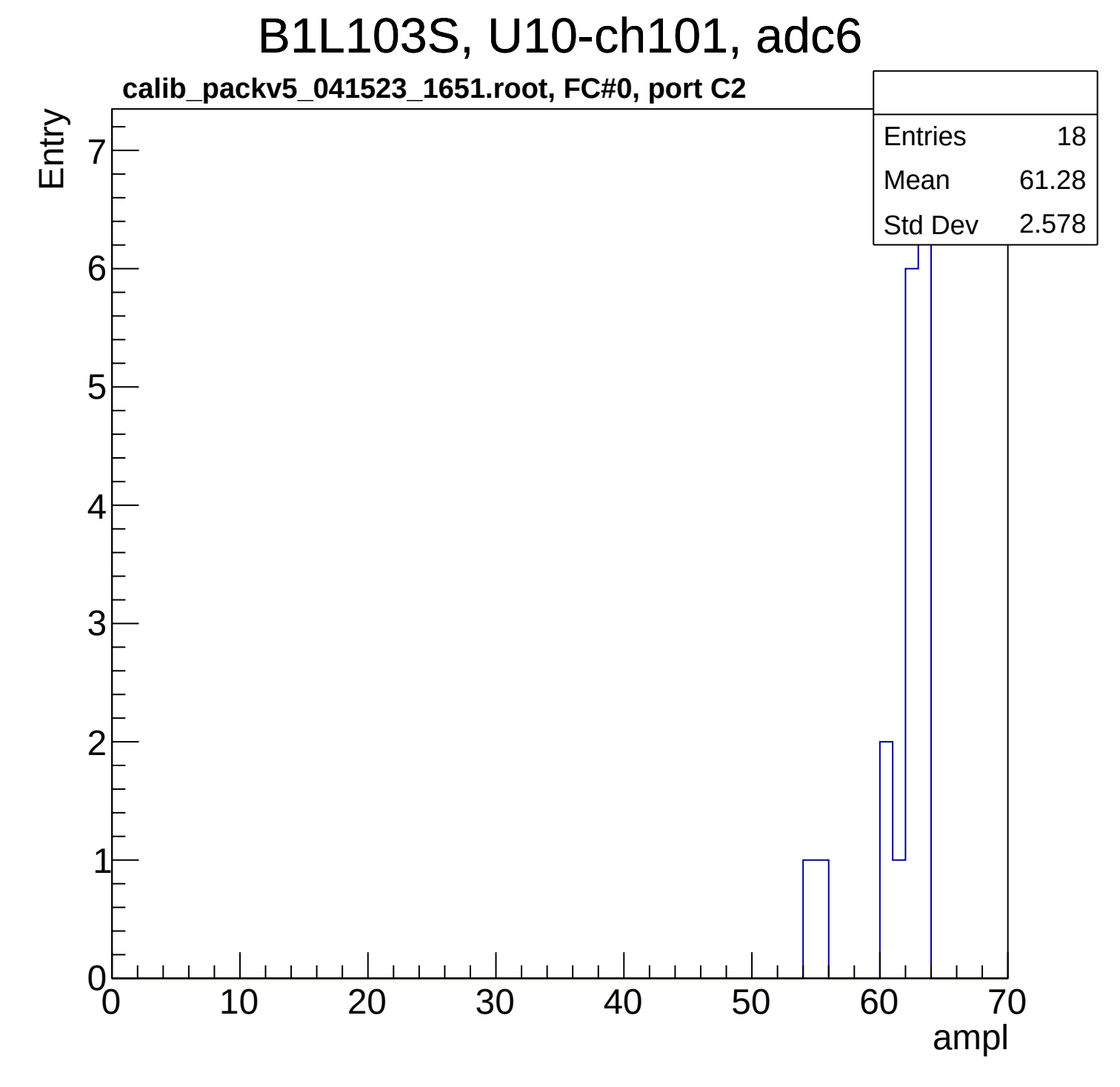
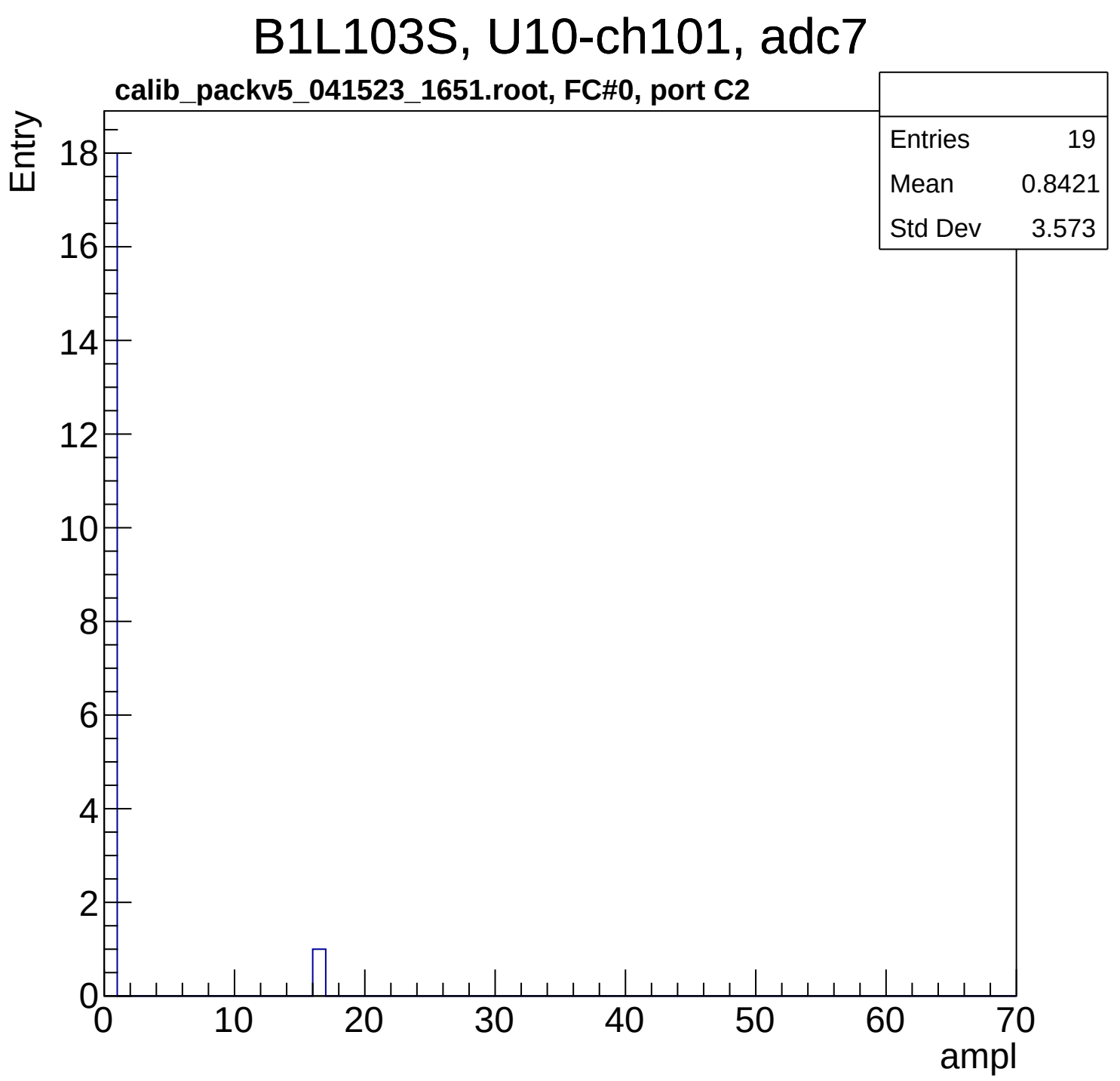
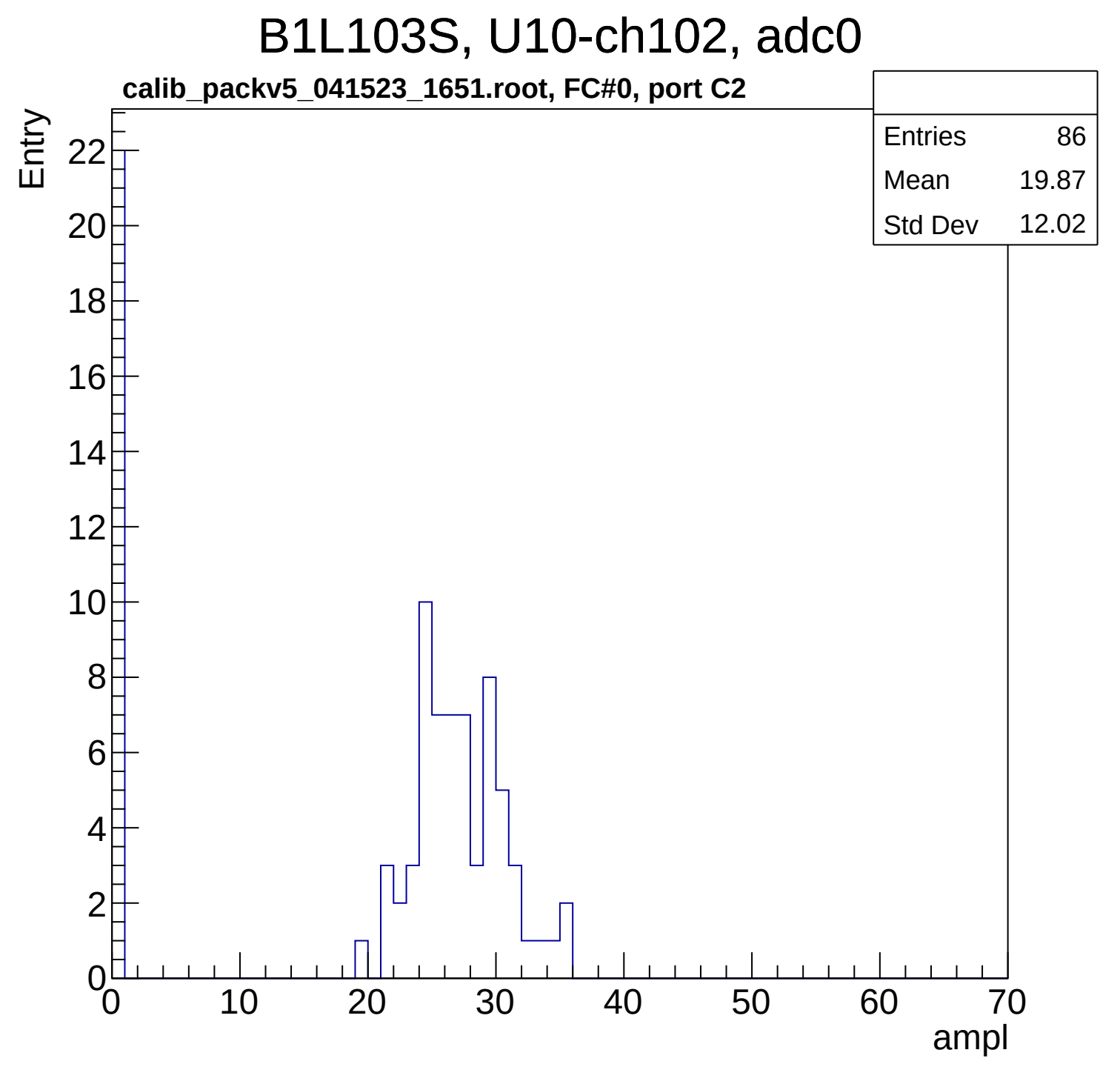
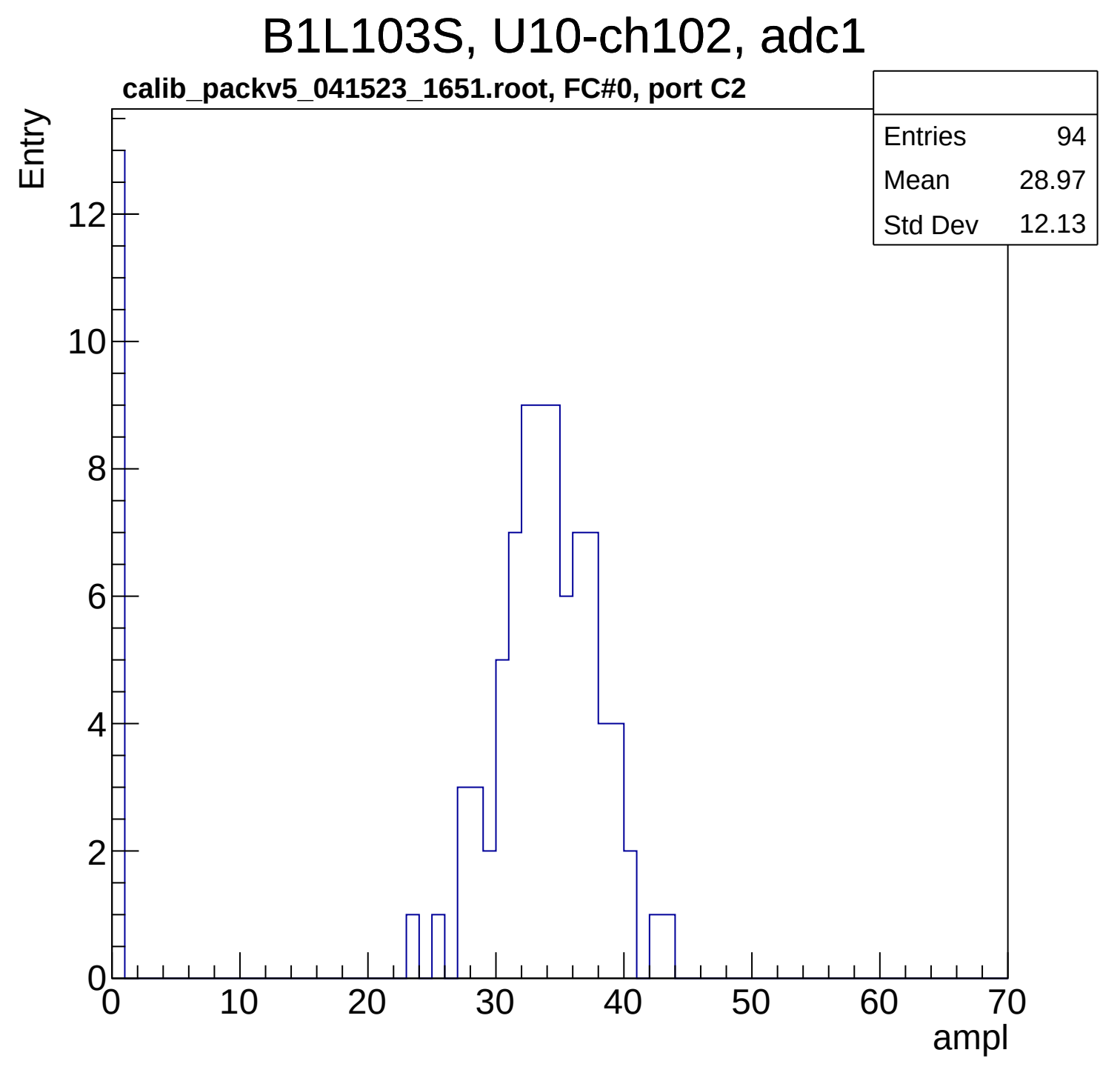
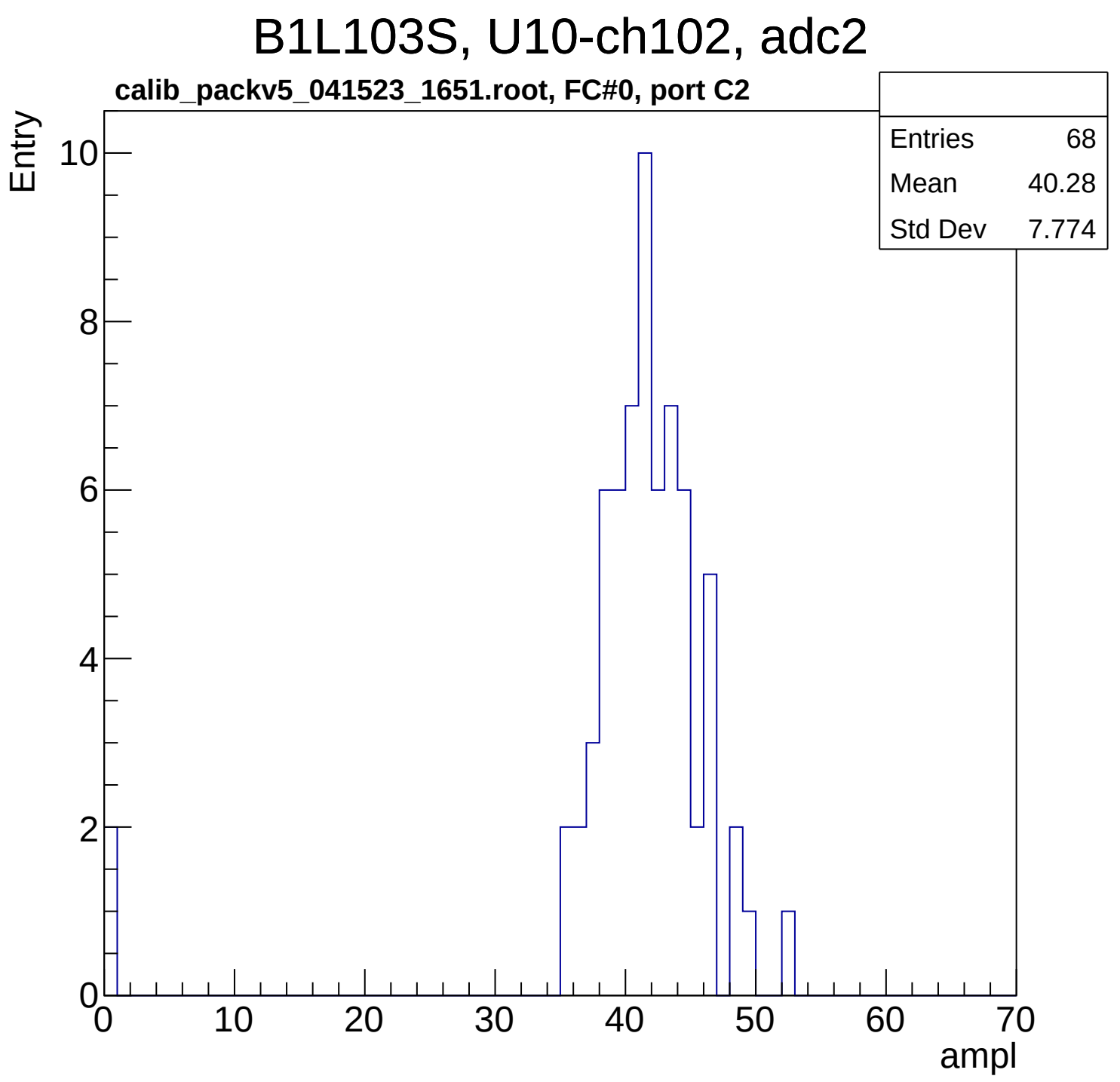

B1L103S, U10-ch101, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 61.28
Std Dev 2.578
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U10-ch101, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0.8421
Std Dev 3.573
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch102, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 19.87
Std Dev 12.02
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
22
0
10
20
30
40
50
60
70


B1L103S, U10-ch102, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 94
Mean 28.97
Std Dev 12.13
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch102, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 40.28
Std Dev 7.774
Entry
ampl
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2
4
6
8
10
0
10
20
30
40
50
60
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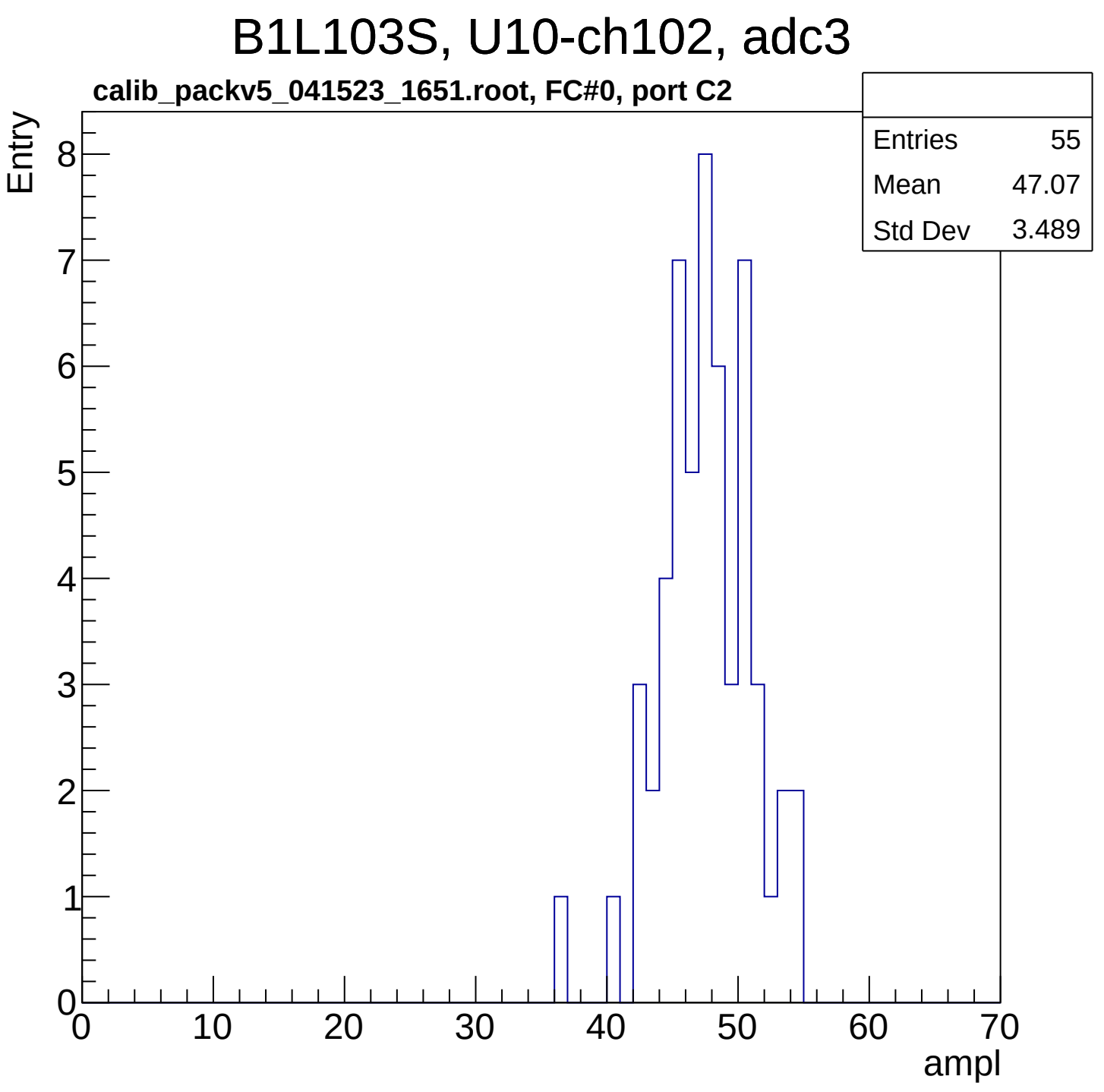
B1L103S, U10-ch102, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 47.07
Std Dev 3.489
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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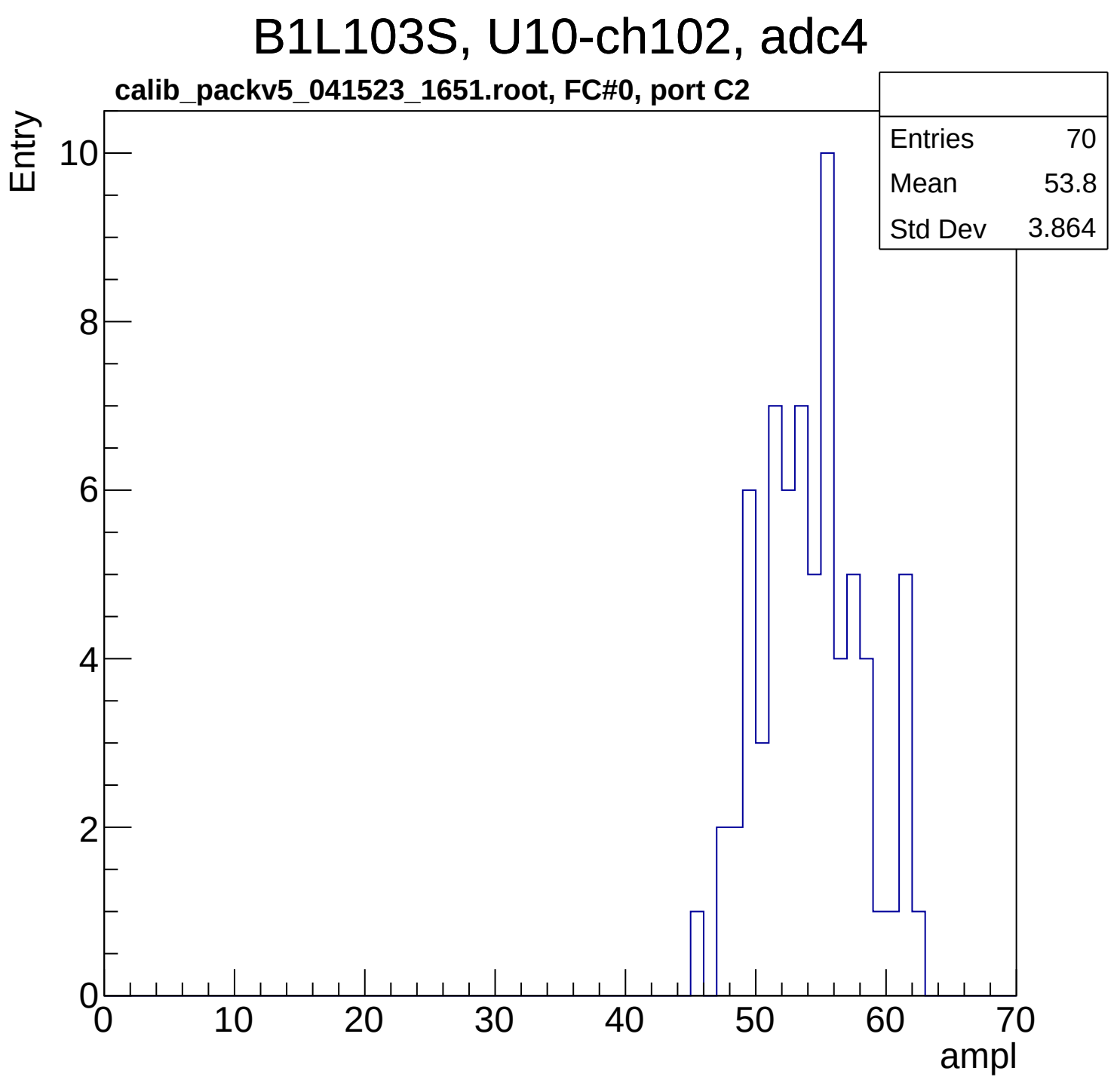
B1L103S, U10-ch102, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 53.8
Std Dev 3.864
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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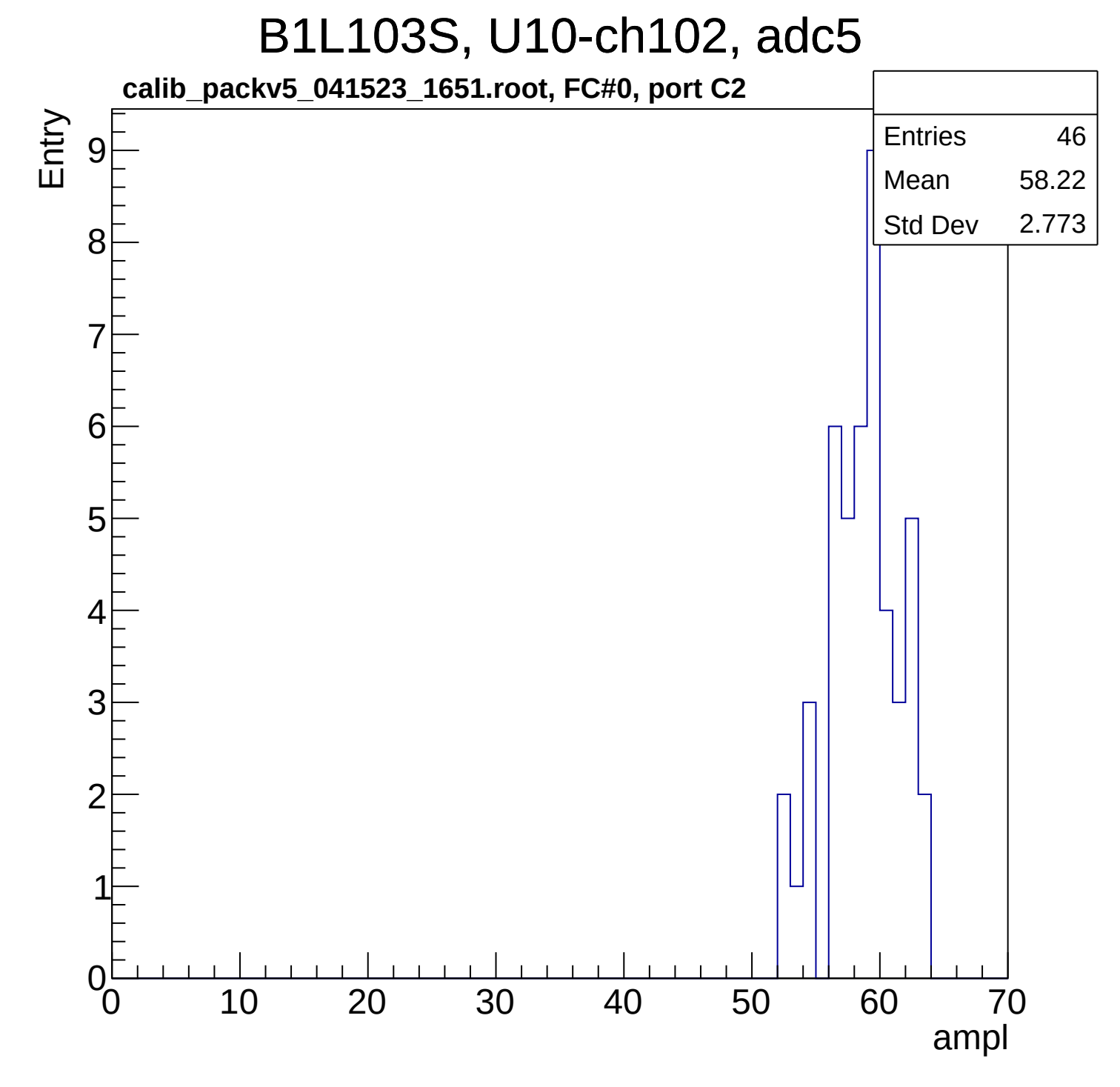
B1L103S, U10-ch102, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 58.22
Std Dev 2.773
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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60
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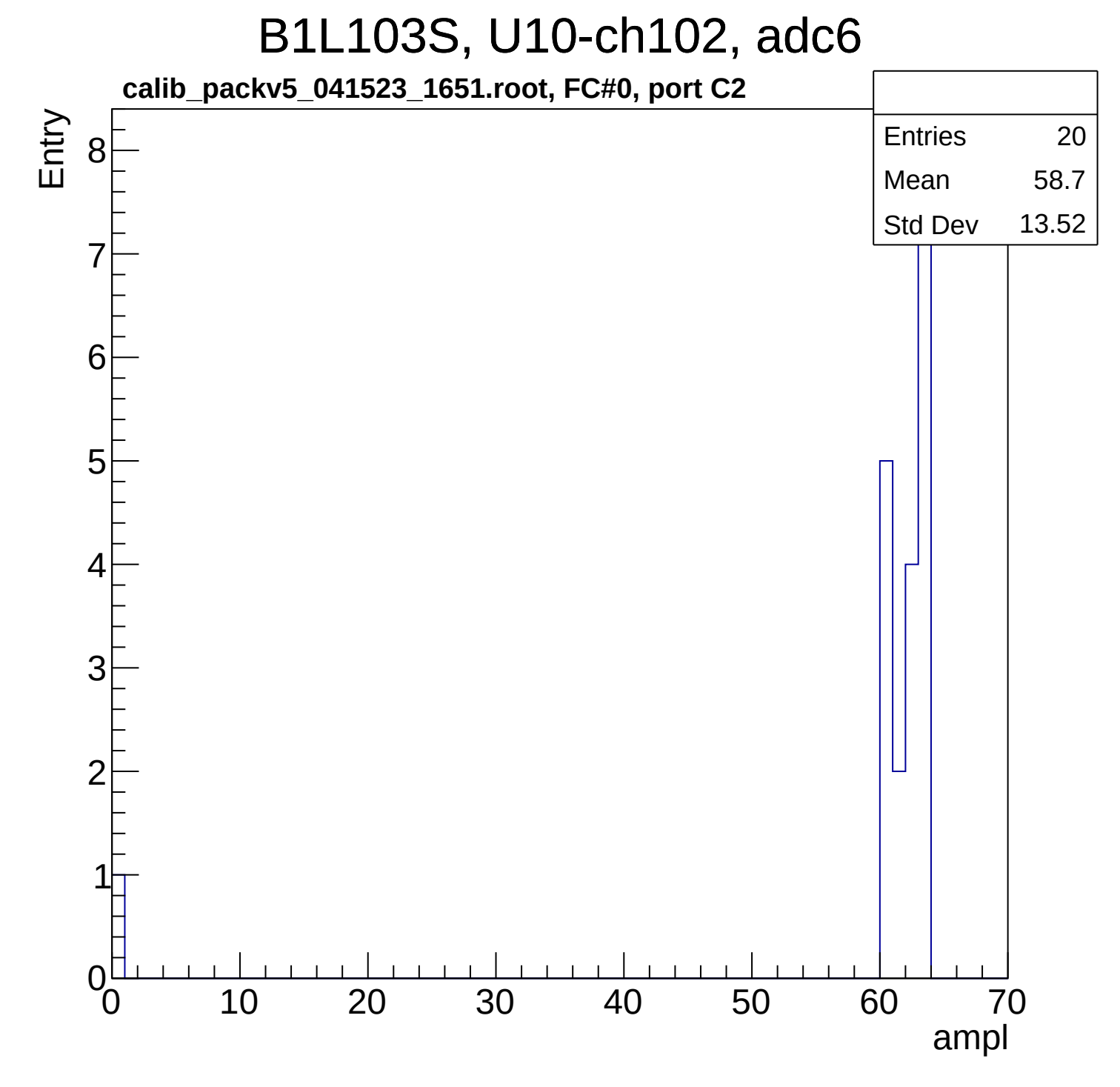
B1L103S, U10-ch102, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 58.7
Std Dev 13.52
Entry
ampl
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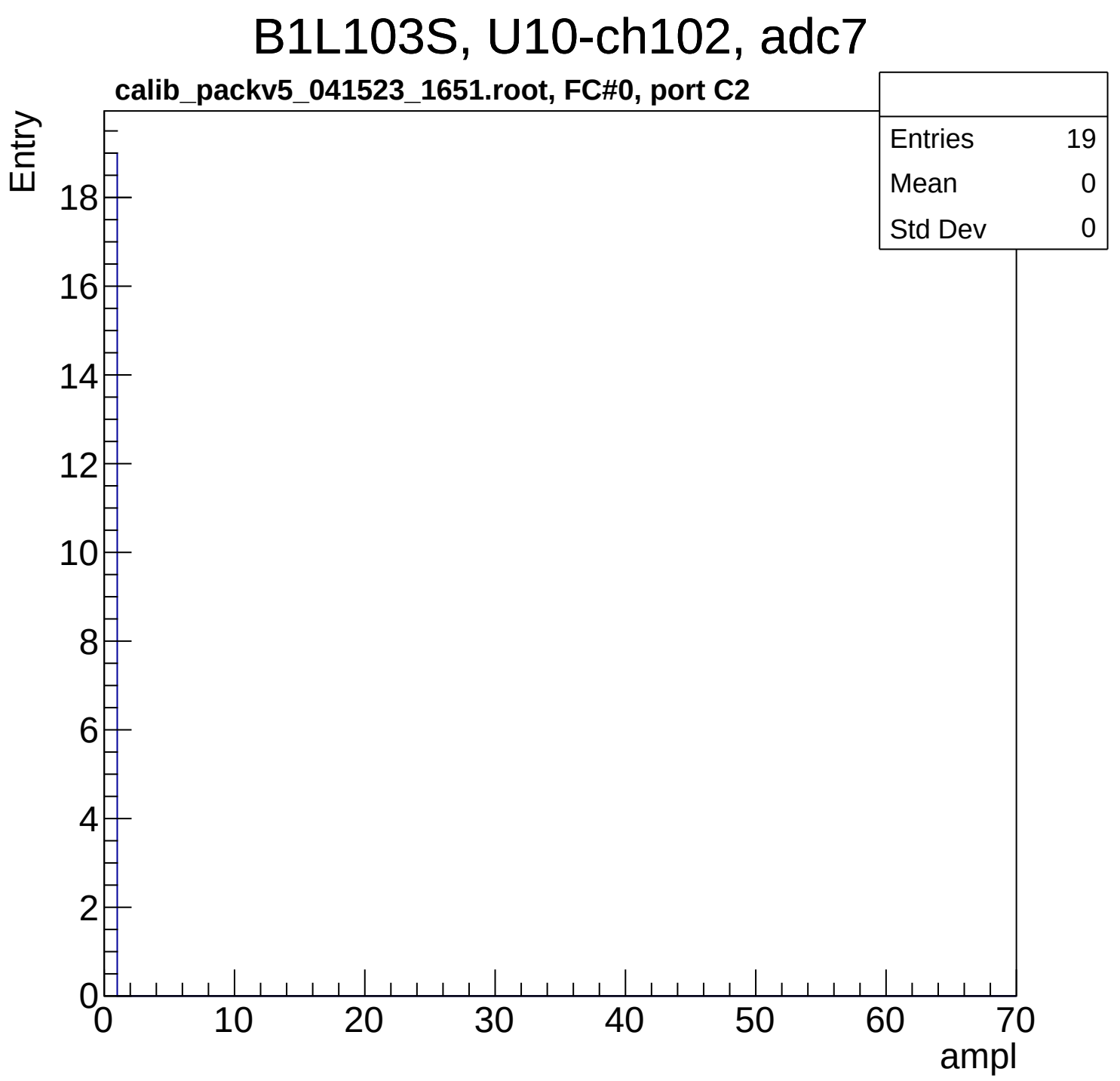
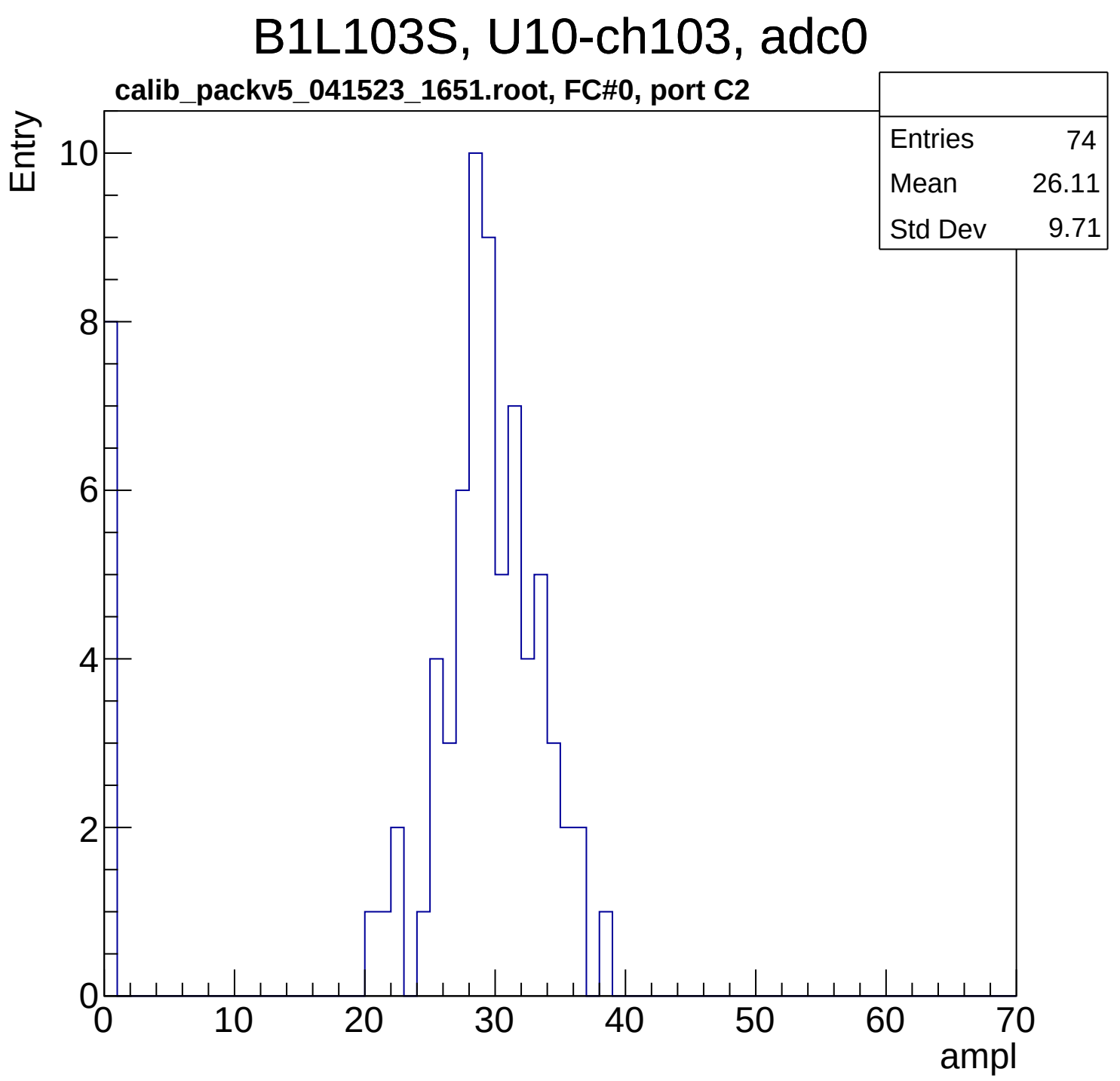
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U10-ch102, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch103, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 26.11
Std Dev 9.71
Entry
ampl
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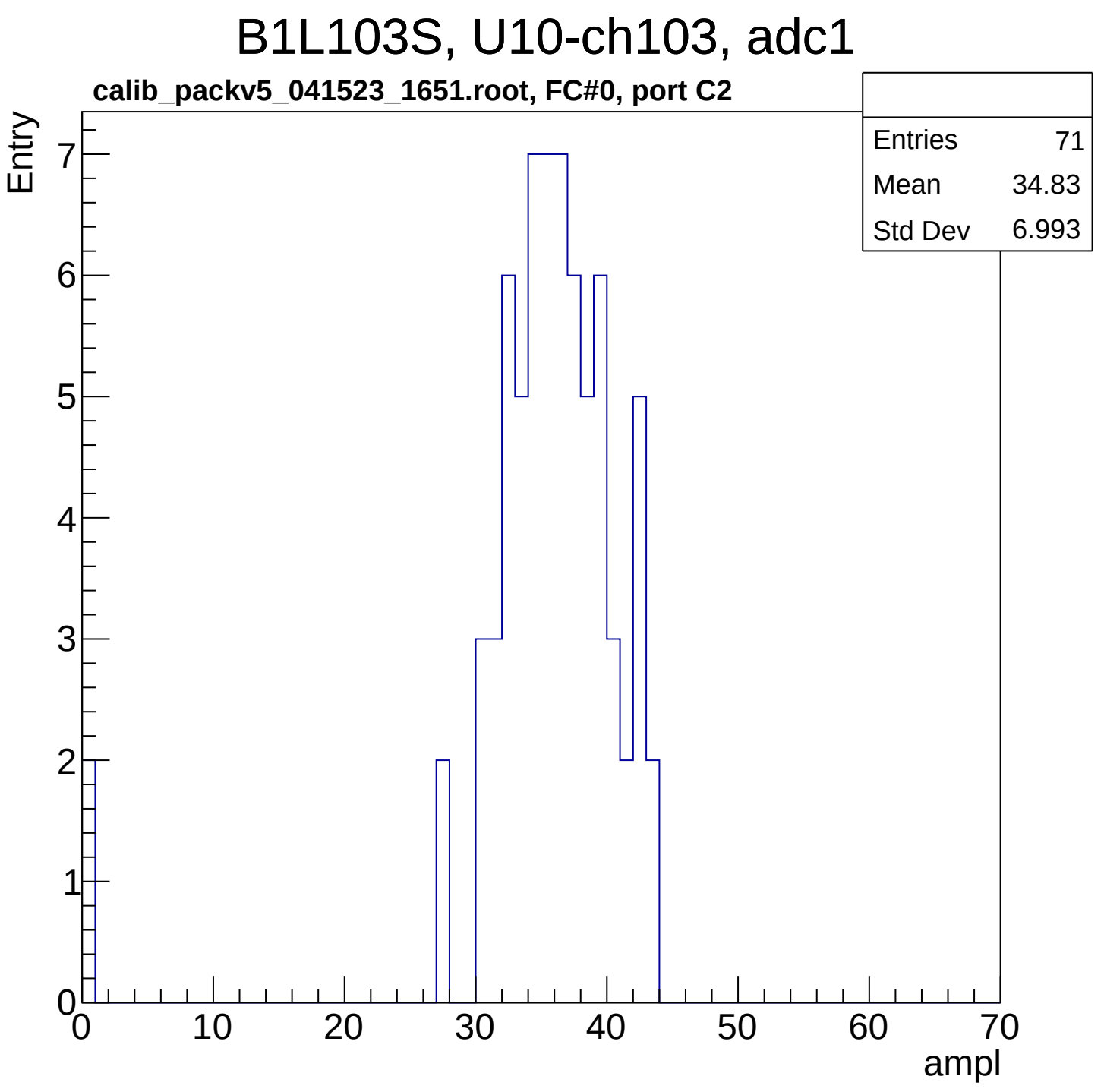
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U10-ch103, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 34.83
Std Dev 6.993
Entry
ampl
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2
3
4
5
6
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0
10
20
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60
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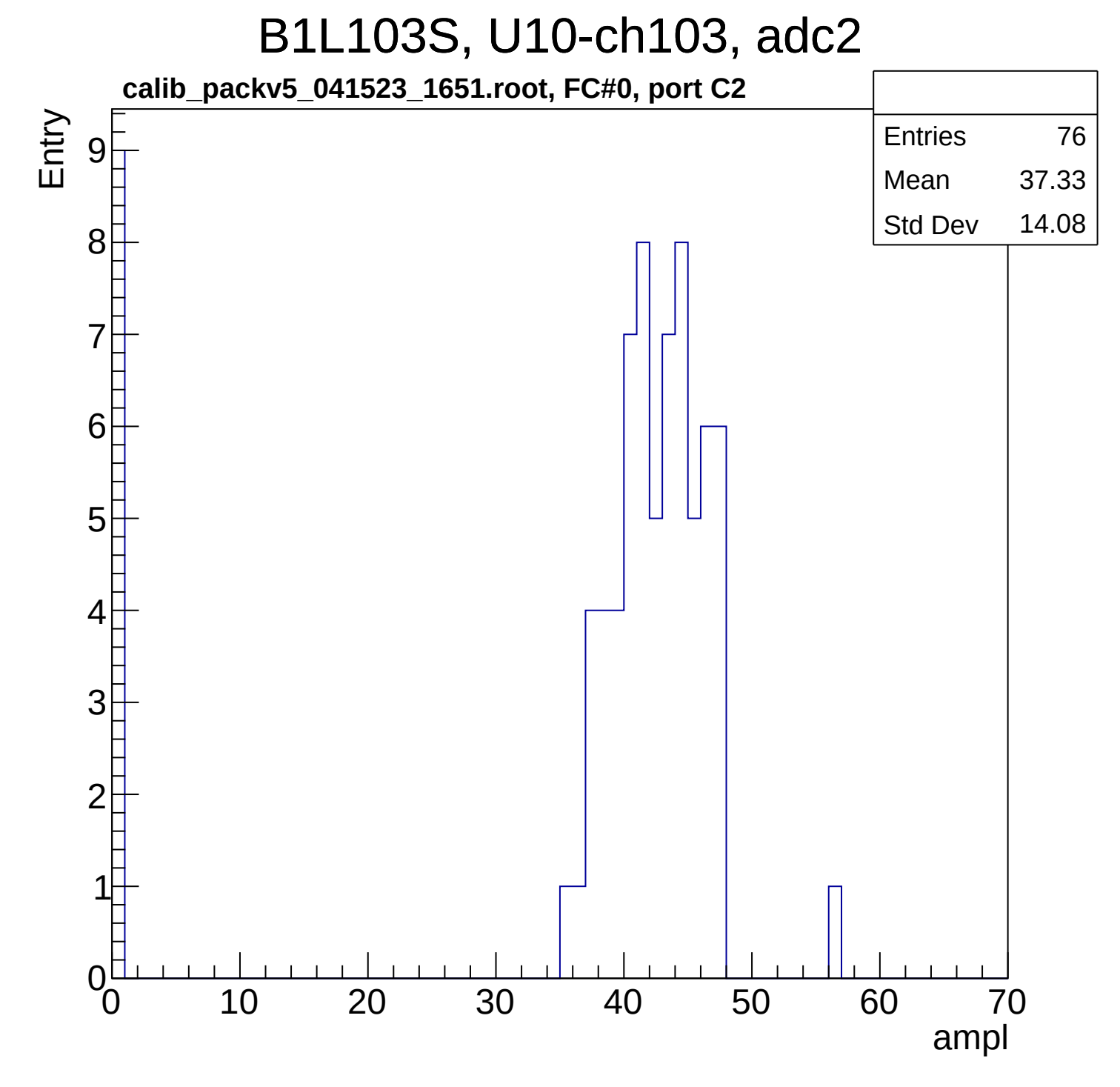
B1L103S, U10-ch103, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 37.33
Std Dev 14.08
Entry
ampl
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2
3
4
5
6
7
8
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0
10
20
30
40
50
60
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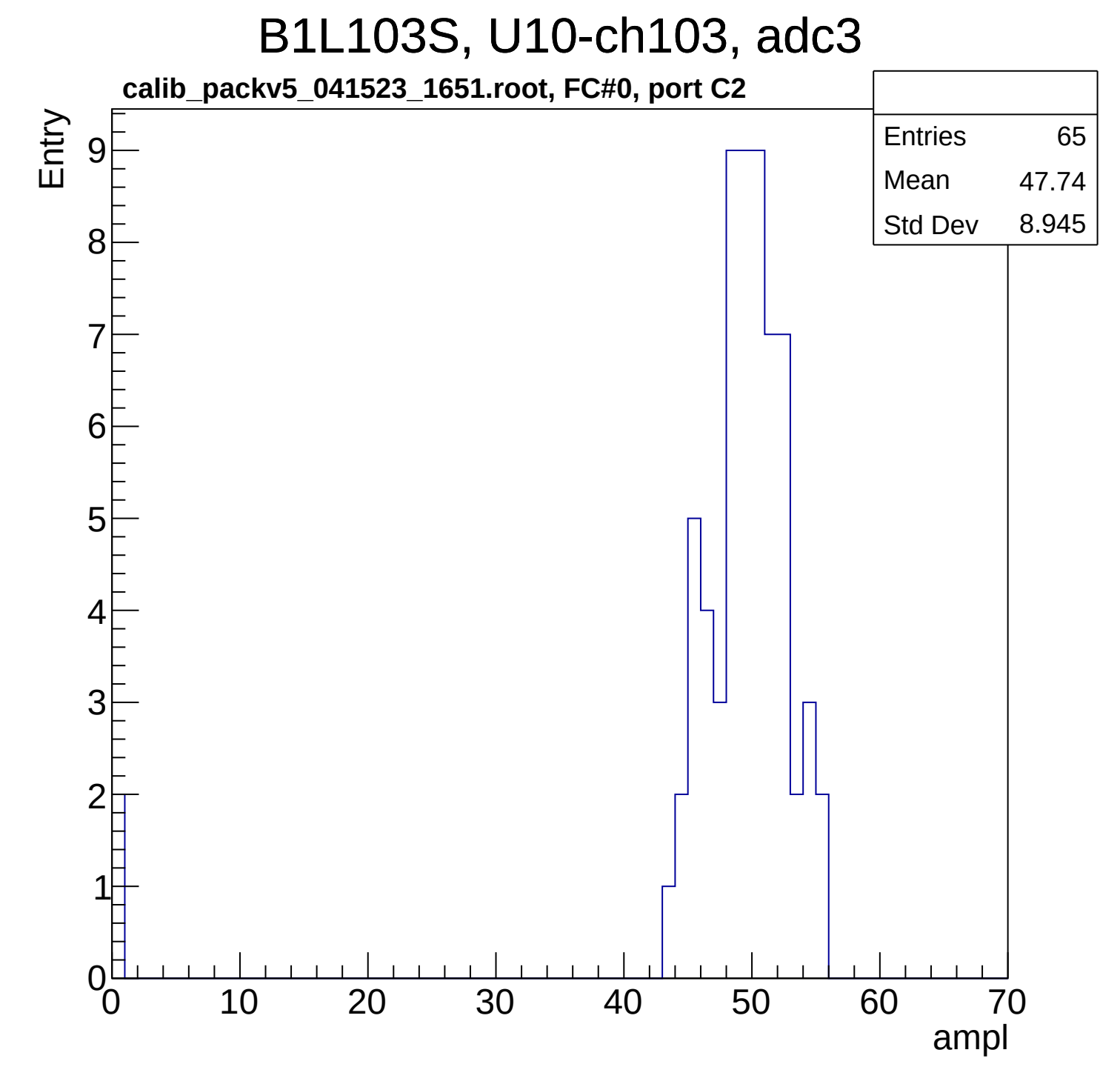
B1L103S, U10-ch103, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 47.74
Std Dev 8.945
Entry
ampl
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3
4
5
6
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8
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0
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60
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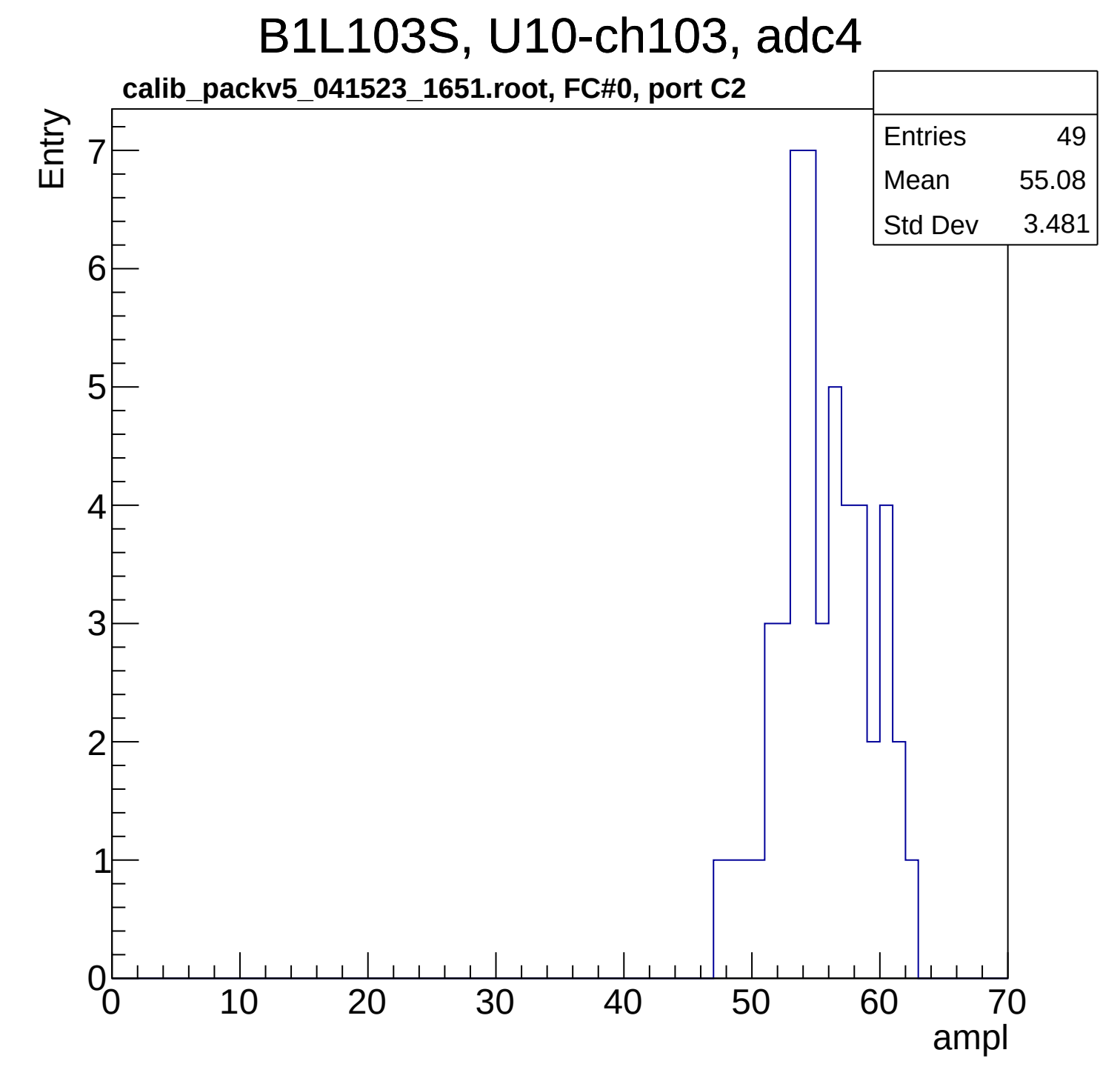
B1L103S, U10-ch103, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 55.08
Std Dev 3.481
Entry
ampl
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2
3
4
5
6
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0
10
20
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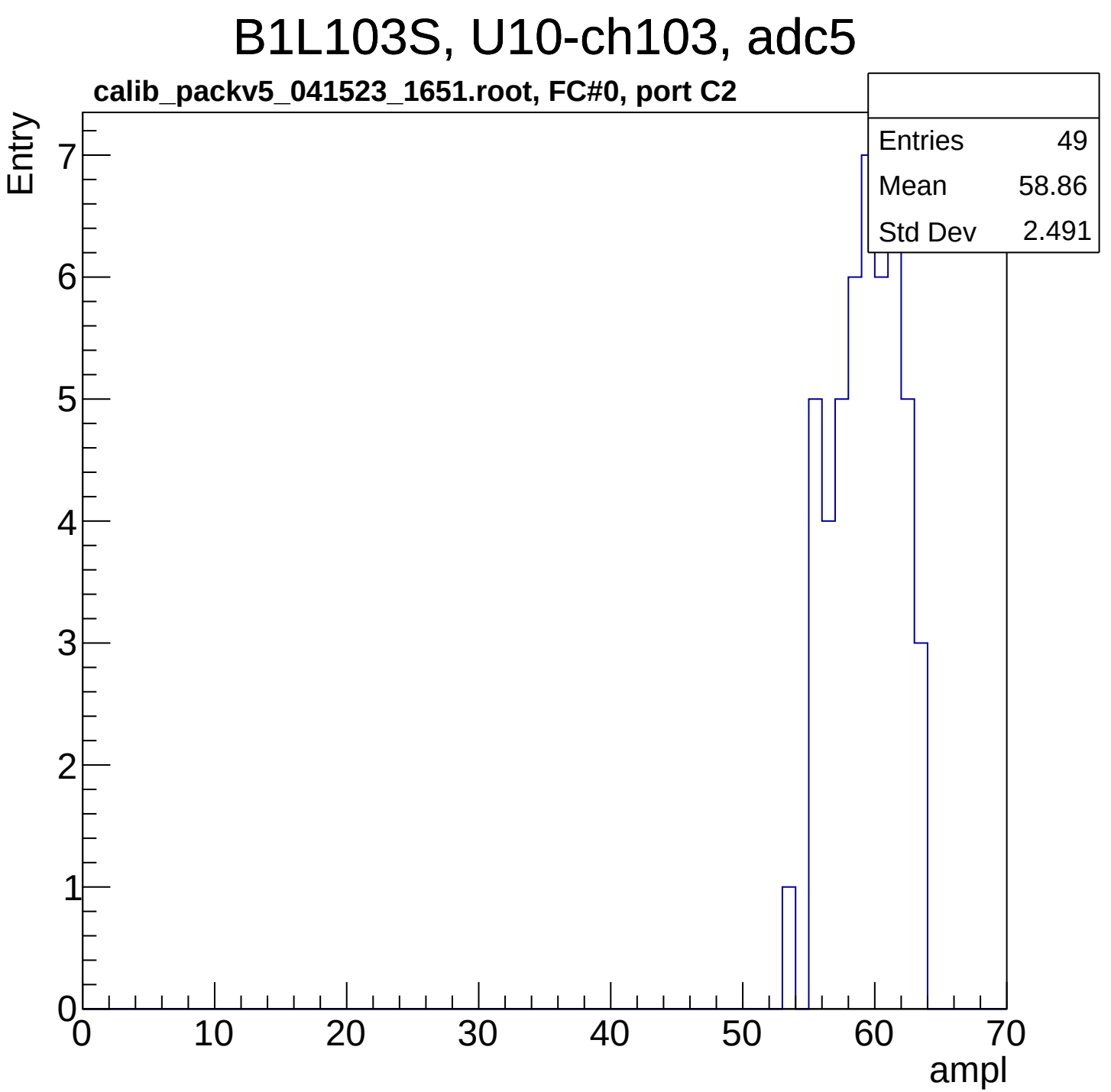
40
50
60
70


B1L103S, U10-ch103, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 58.86
Std Dev 2.491
Entry
ampl
0
1
2
3
4
5
6
7
0
10
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40
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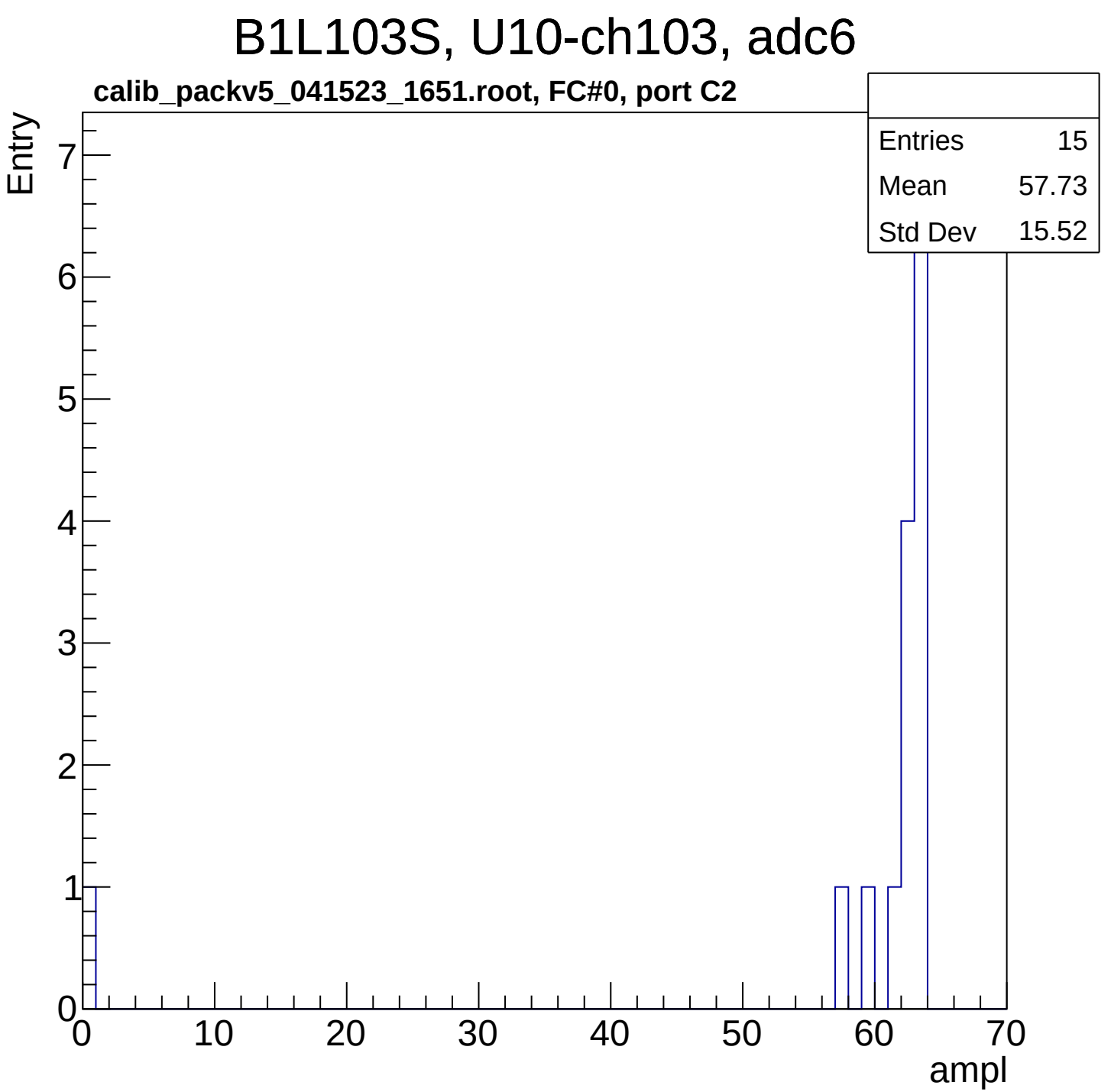
60
70


B1L103S, U10-ch103, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 15
Mean 57.73
Std Dev 15.52
Entry
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2
3
4
5
6
7
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10
20
30
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50
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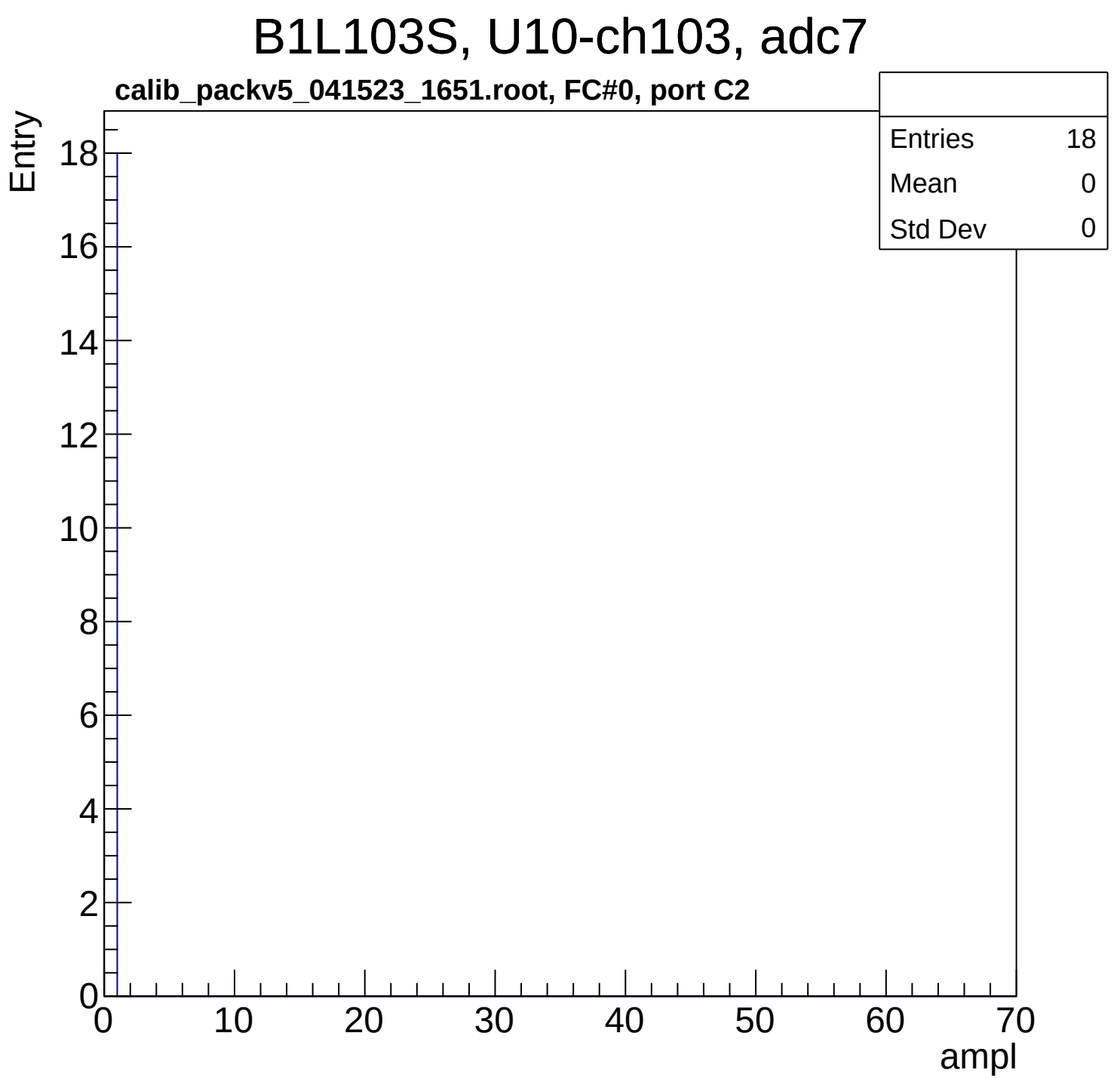
70
ampl


B1L103S, U10-ch103, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
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2
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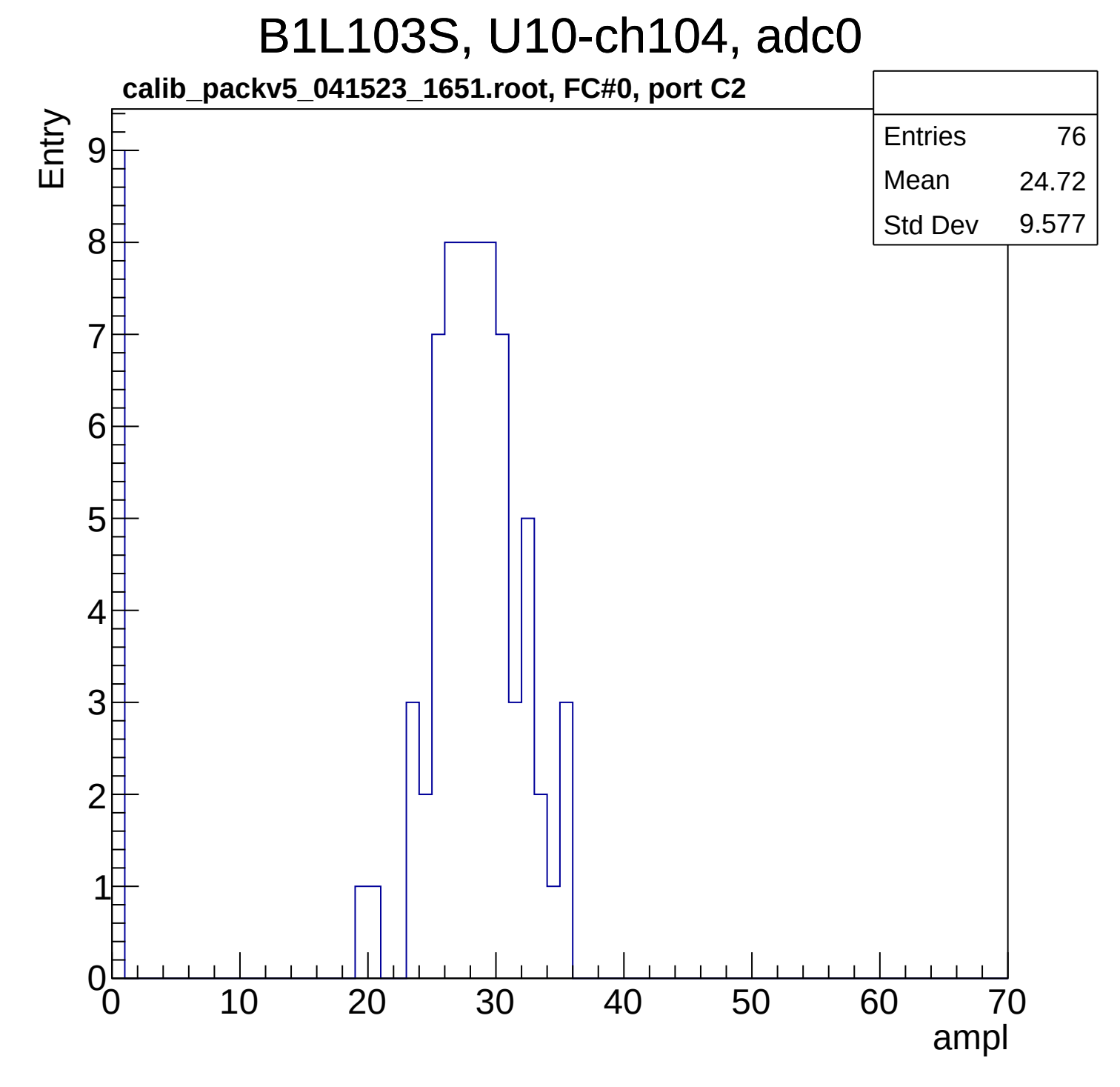
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch104, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 24.72
Std Dev 9.577
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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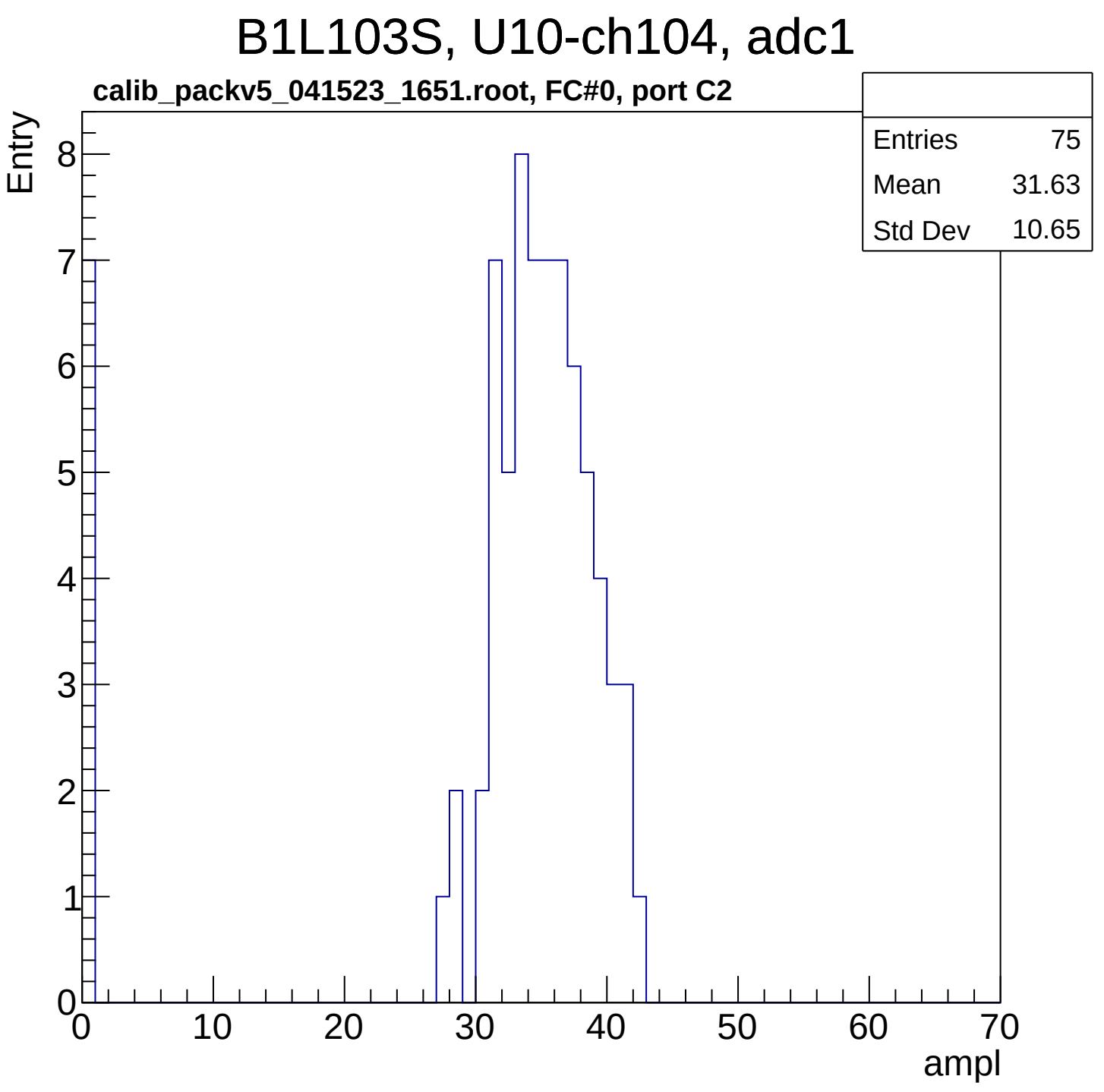
40
50
60
70


B1L103S, U10-ch104, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 31.63
Std Dev 10.65
Entry
ampl
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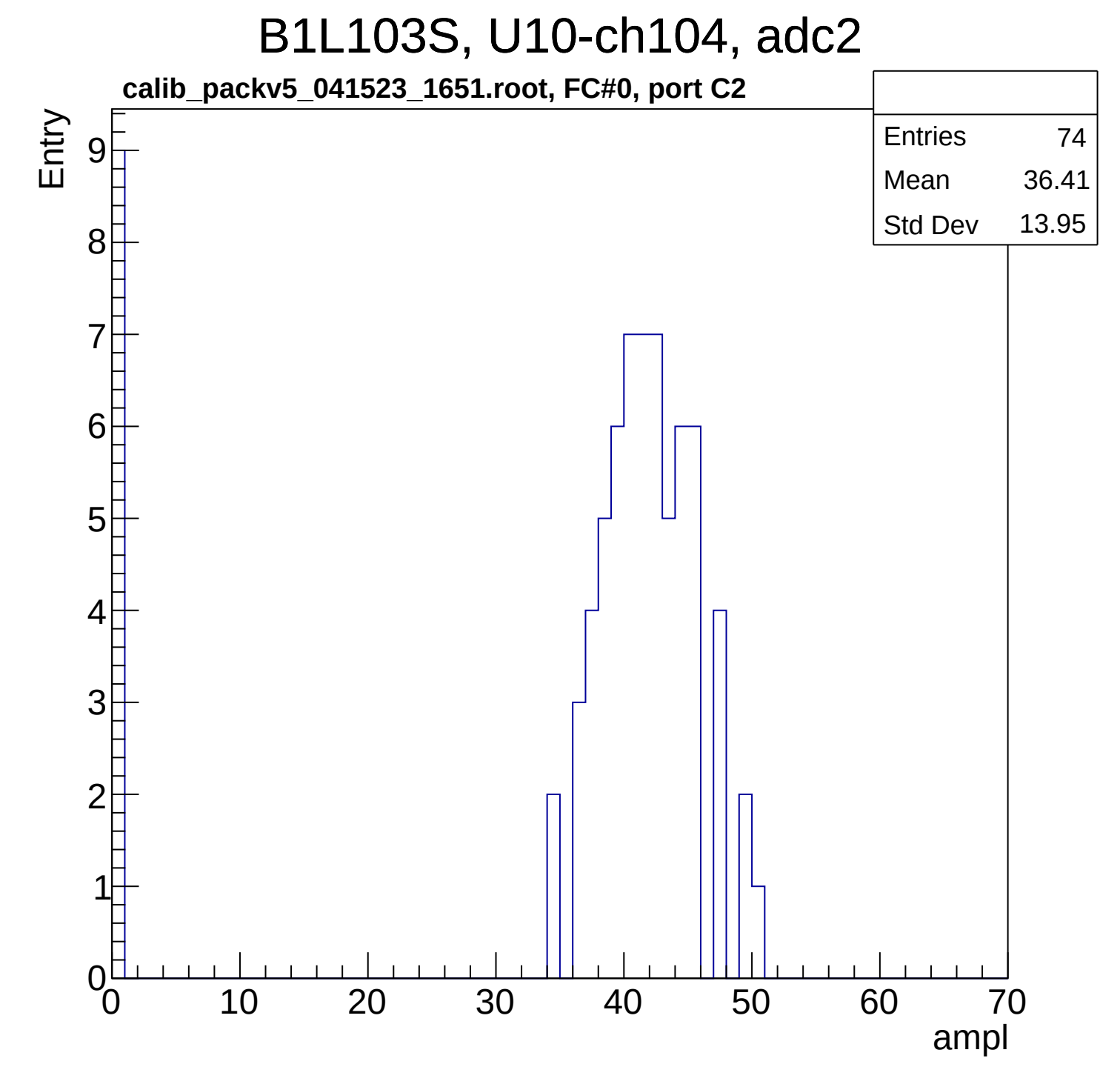
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U10-ch104, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 36.41
Std Dev 13.95
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
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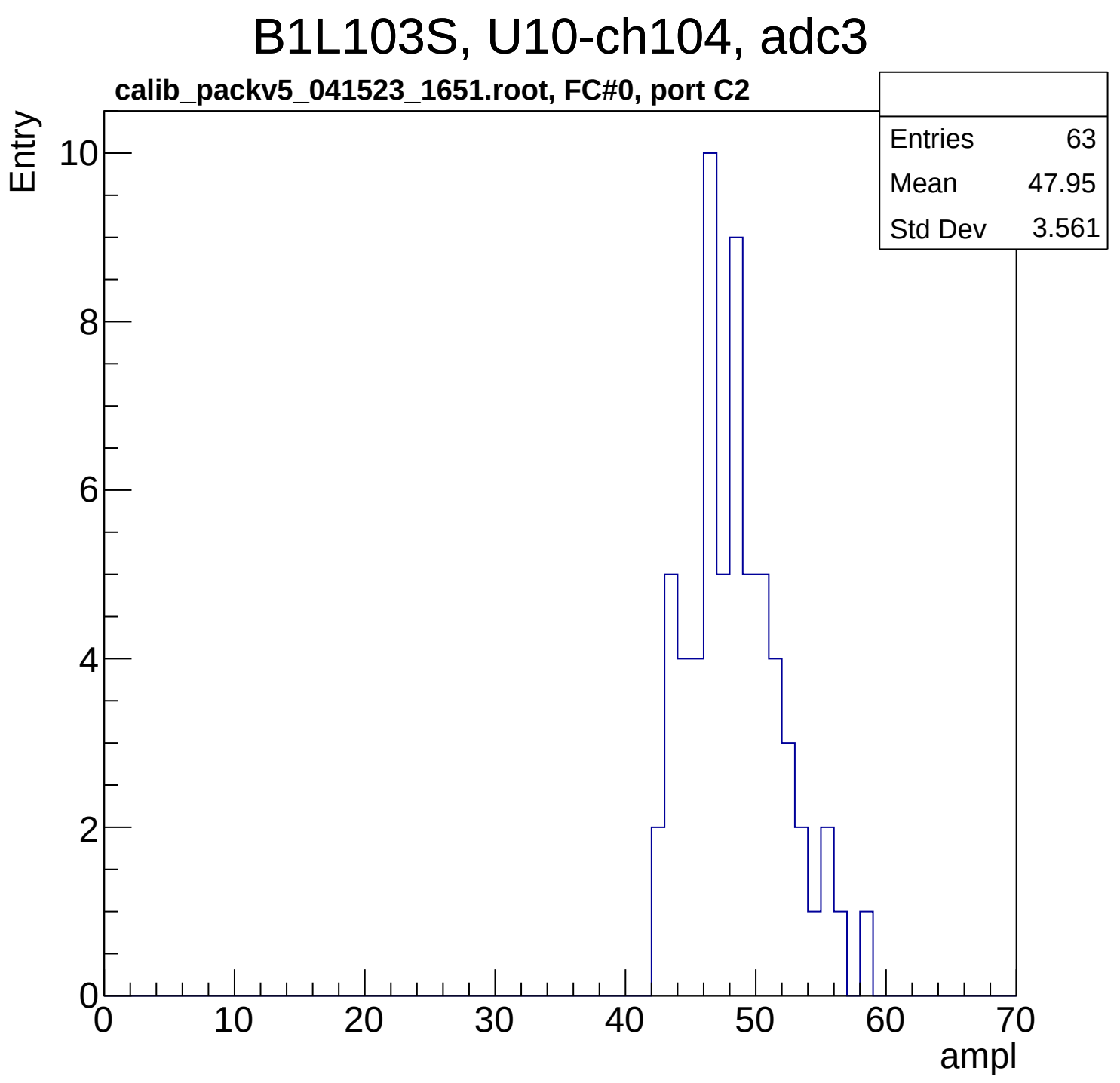
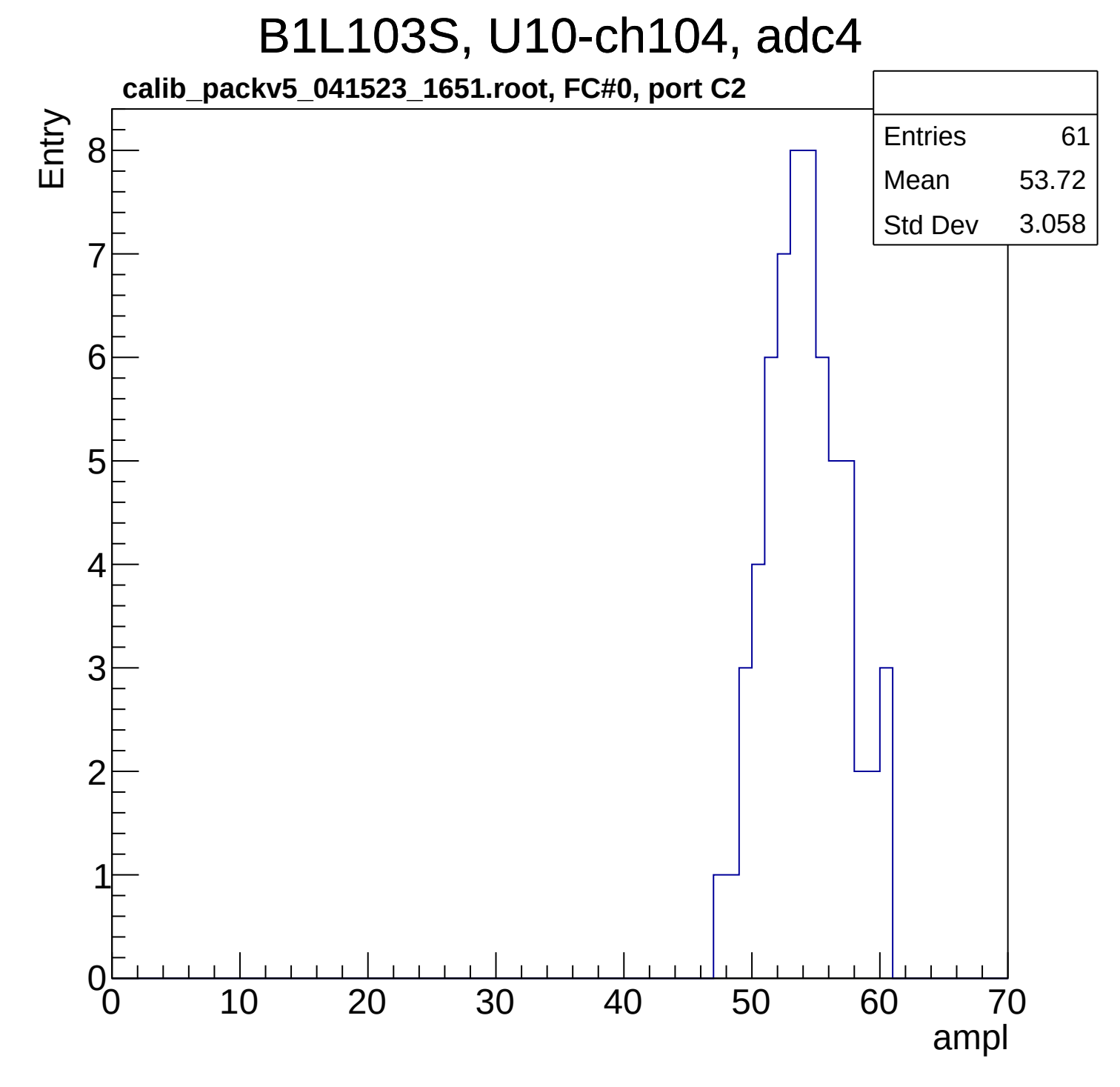
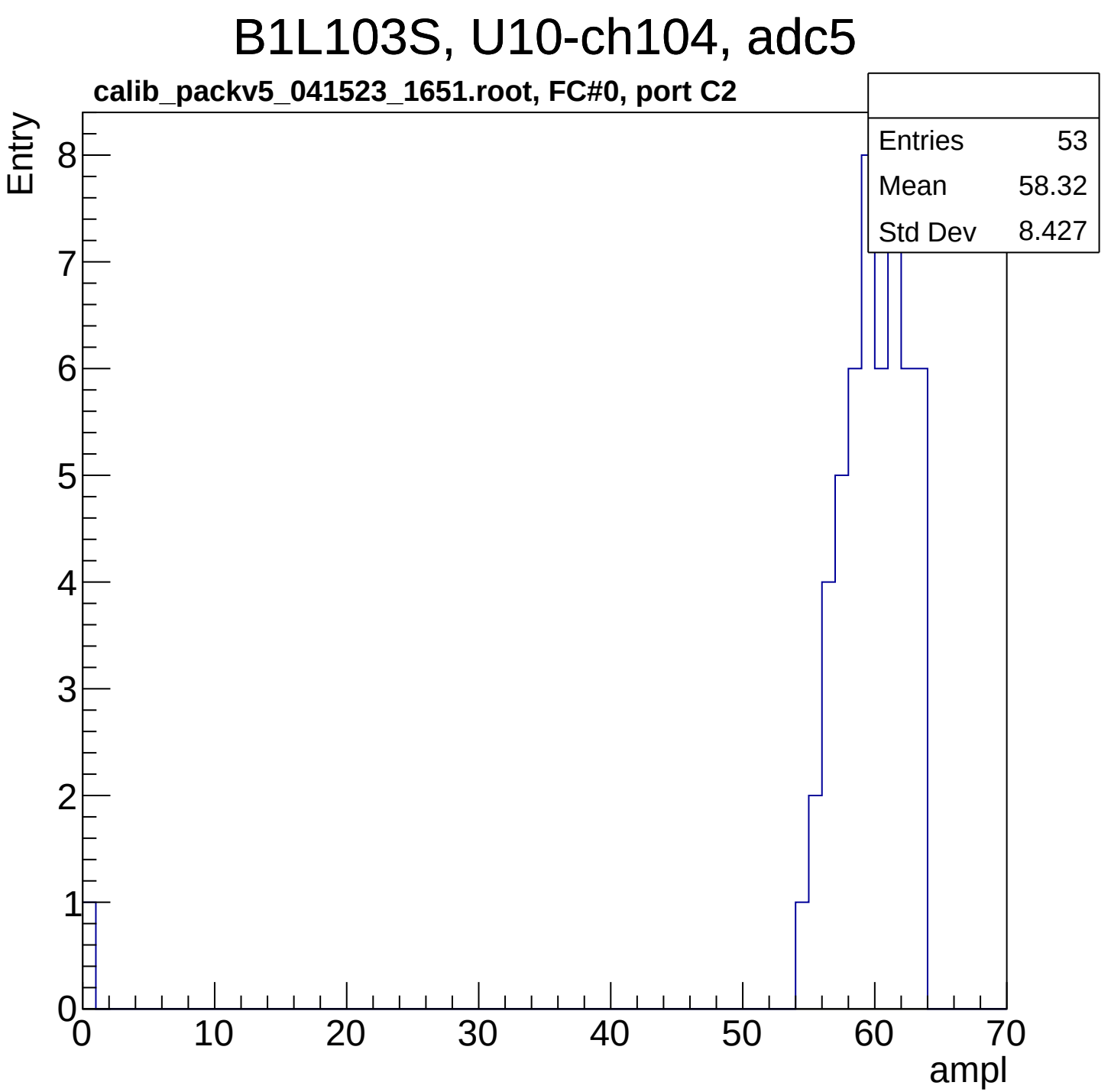

B1L103S, U10-ch104, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 47.95
Std Dev 3.561
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch104, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 53.72
Std Dev 3.058
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U10-ch104, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 58.32
Std Dev 8.427
Entry
ampl
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1
2
3
4
5
6
7
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0
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40
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60
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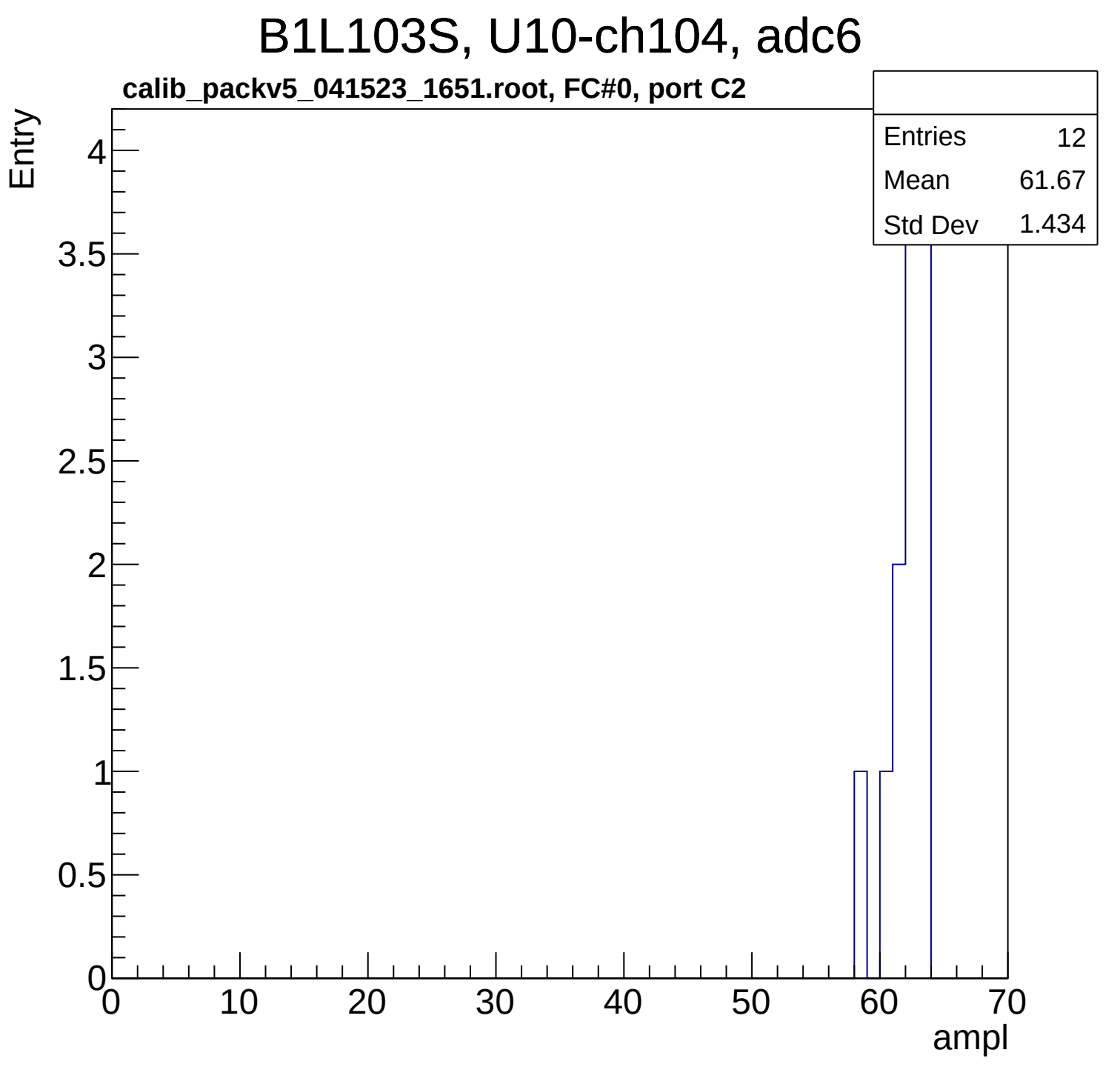
B1L103S, U10-ch104, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 61.67
Std Dev 1.434
Entry
ampl
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1.5
2
2.5
3
3.5
4
0
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40
50
60
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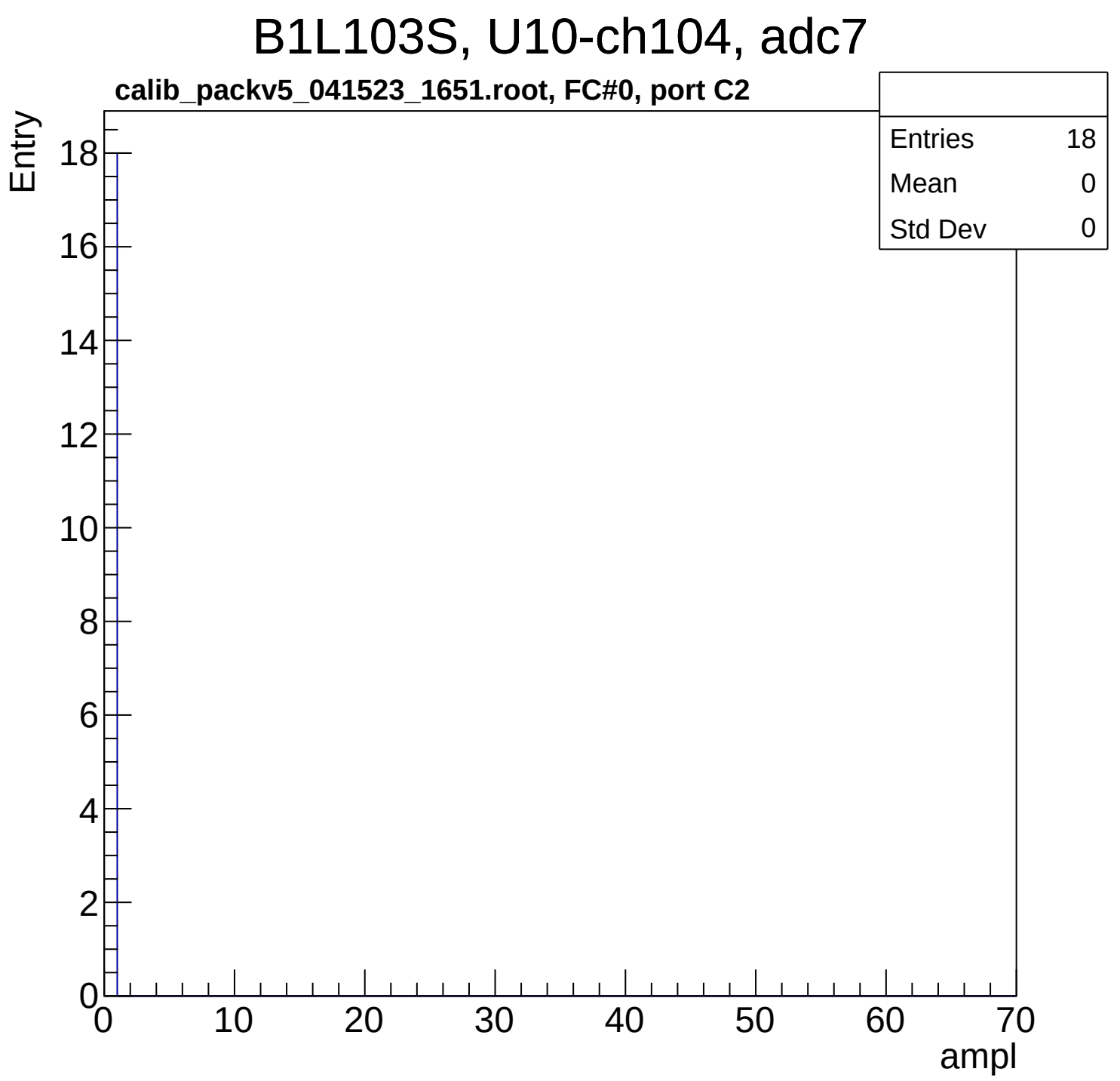
B1L103S, U10-ch104, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
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6
8
10
12
14
16
18
0
10
20
30
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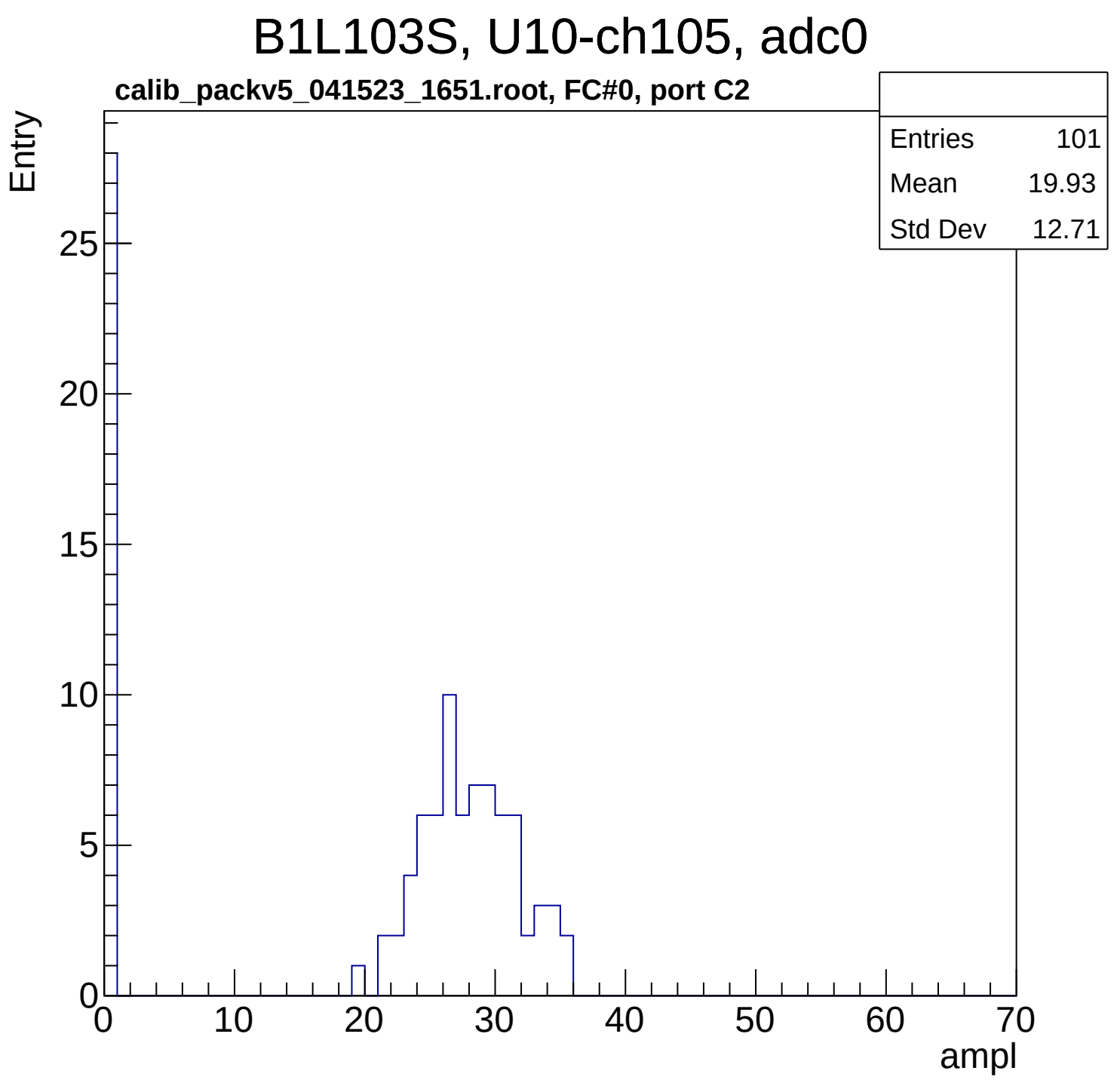
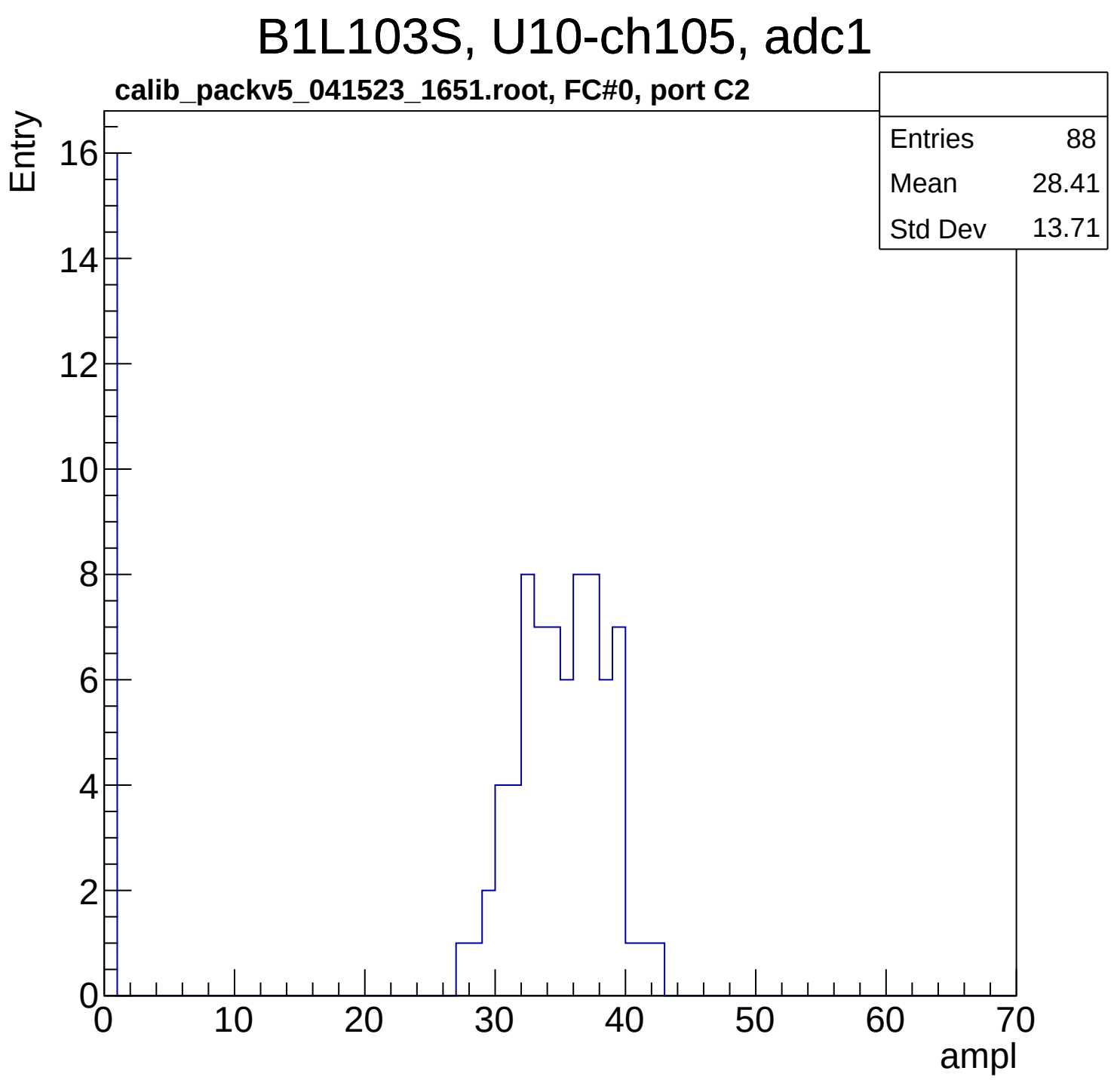
50
60
70
ampl


B1L103S, U10-ch105, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 101
Mean 19.93
Std Dev 12.71
Entry
0
5
10
15
20
25
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch105, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 88
Mean 28.41
Std Dev 13.71
Entry
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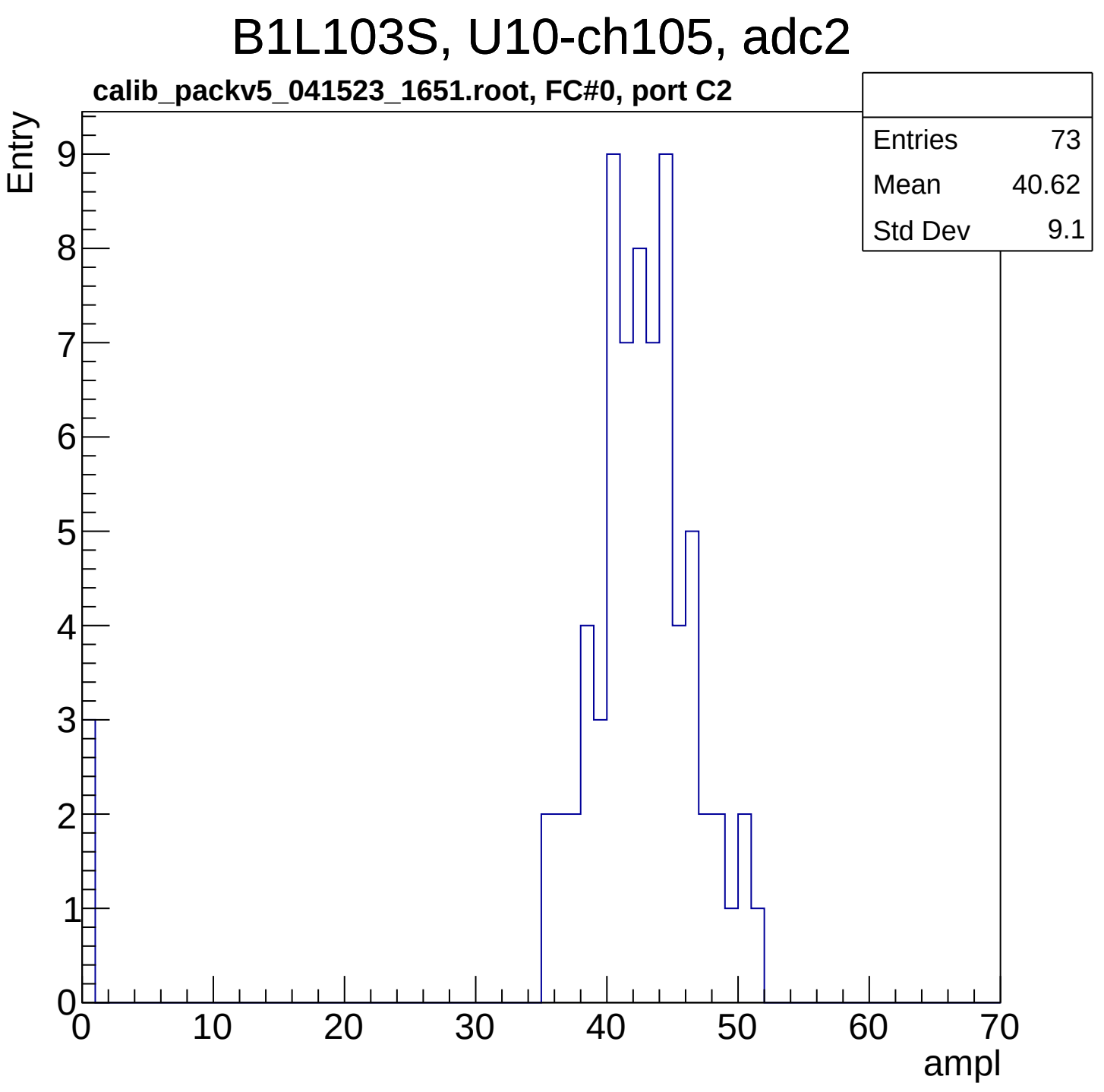
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch105, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 40.62
Std Dev 9.1
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
50
60
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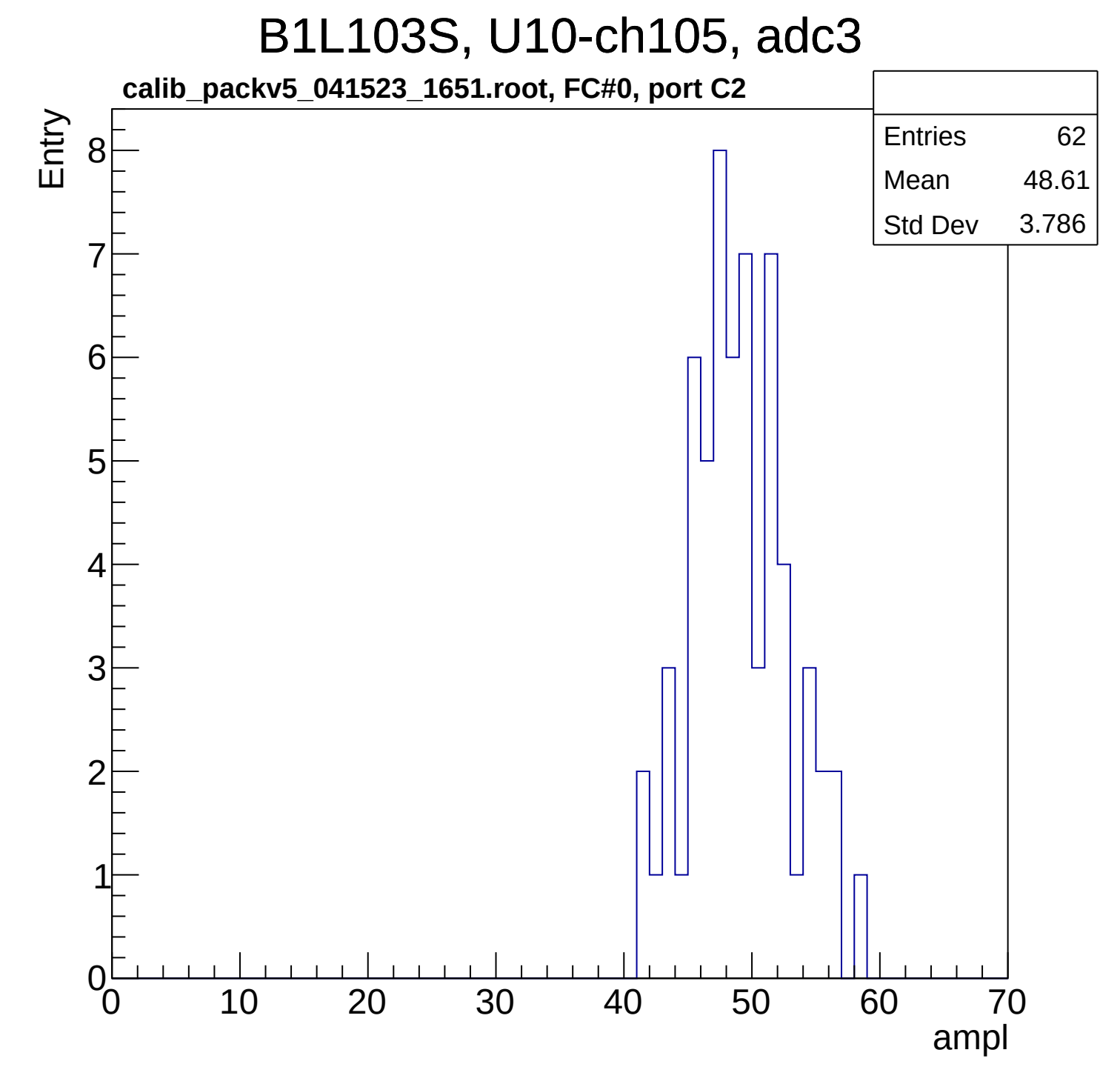
B1L103S, U10-ch105, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 48.61
Std Dev 3.786
Entry
ampl
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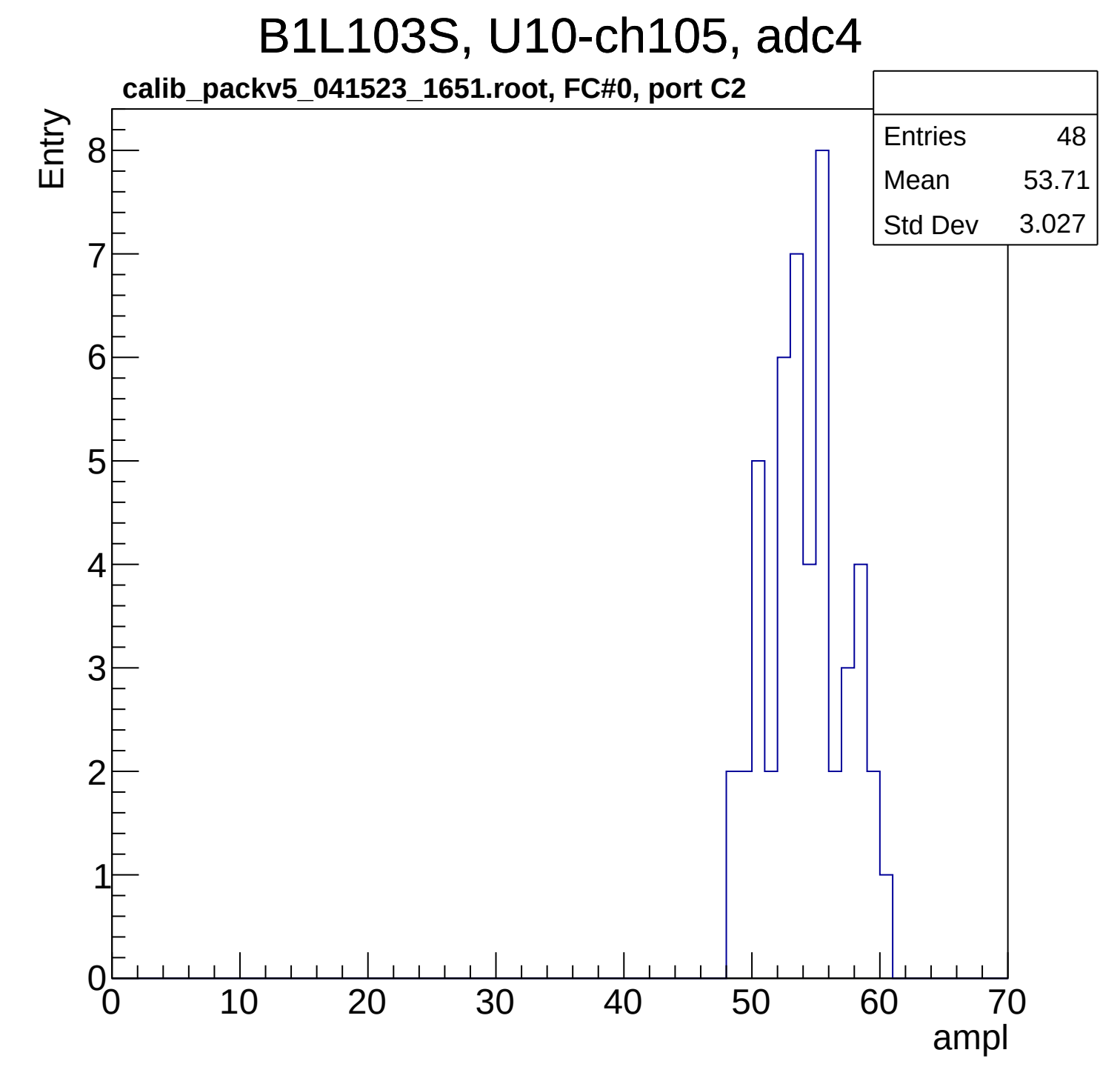
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U10-ch105, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 53.71
Std Dev 3.027
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
30
40
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60
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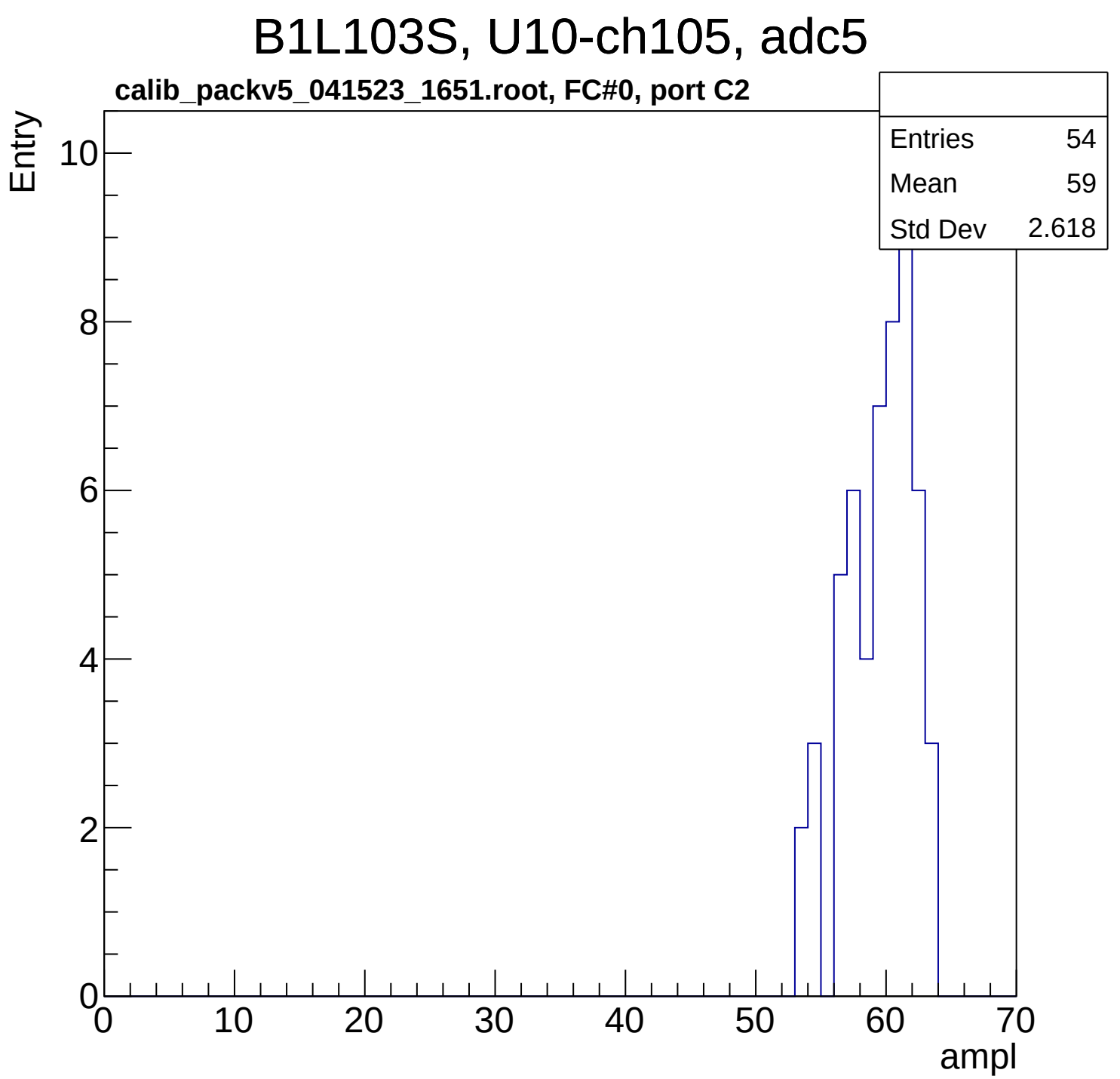
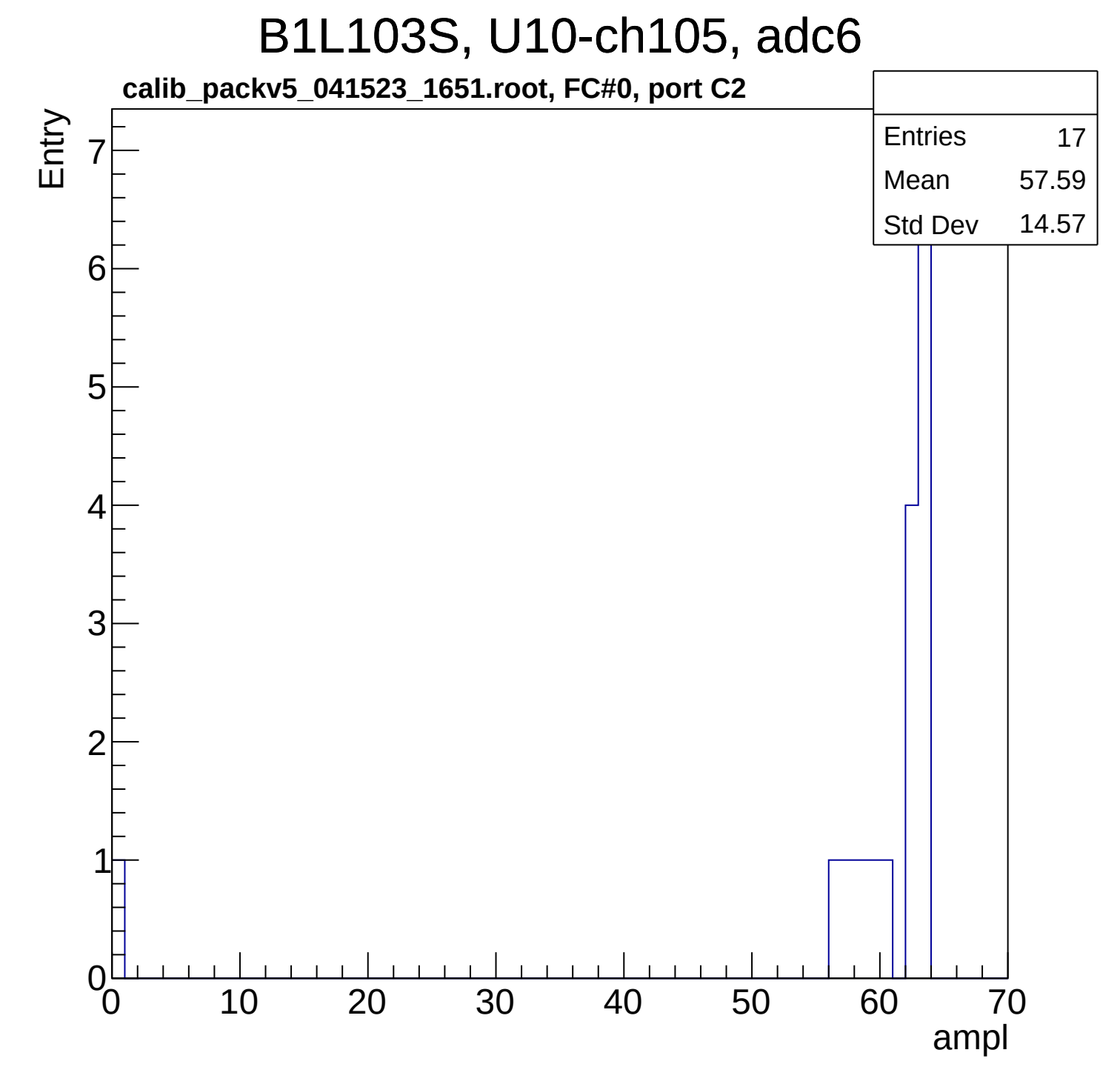
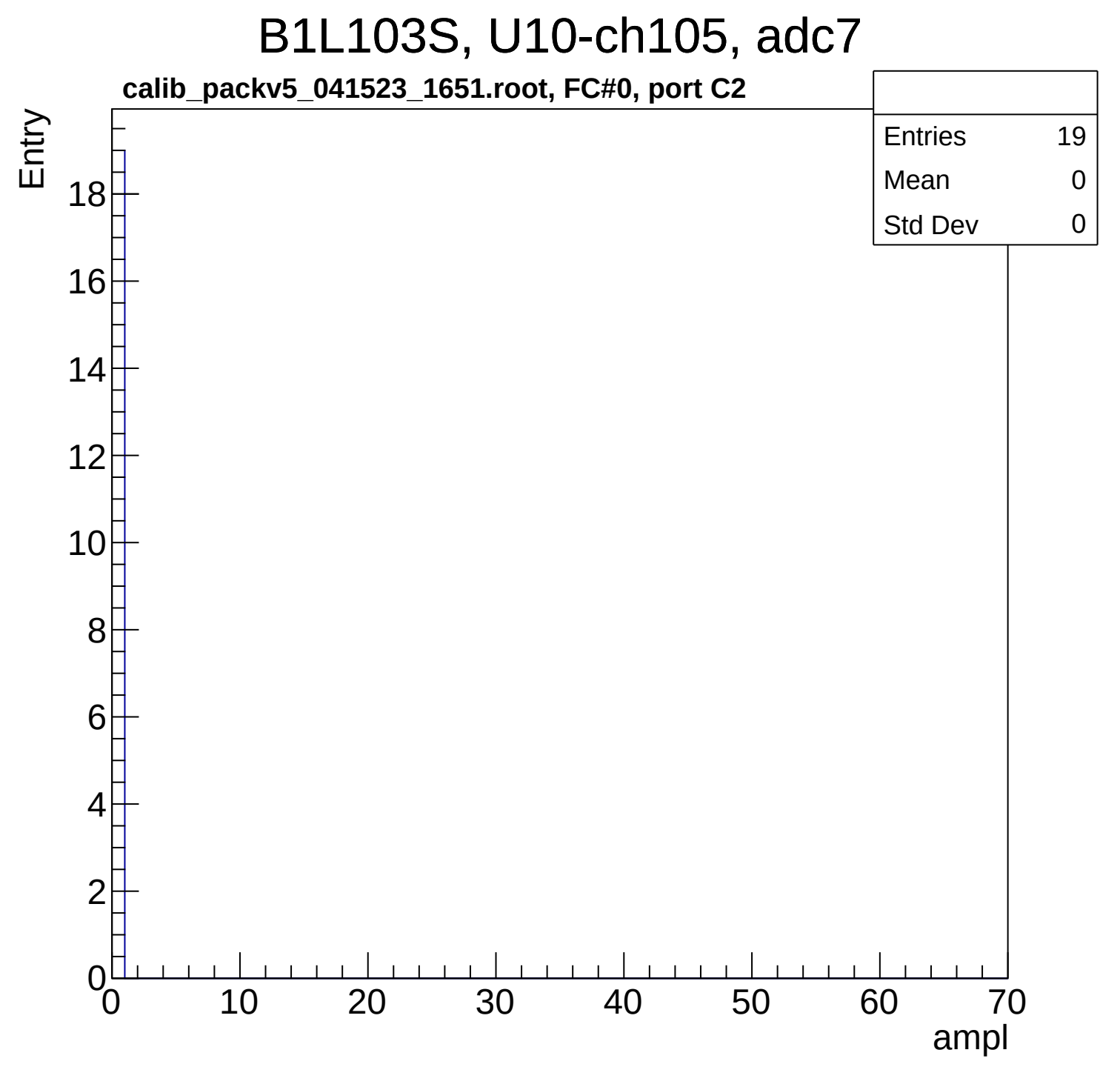
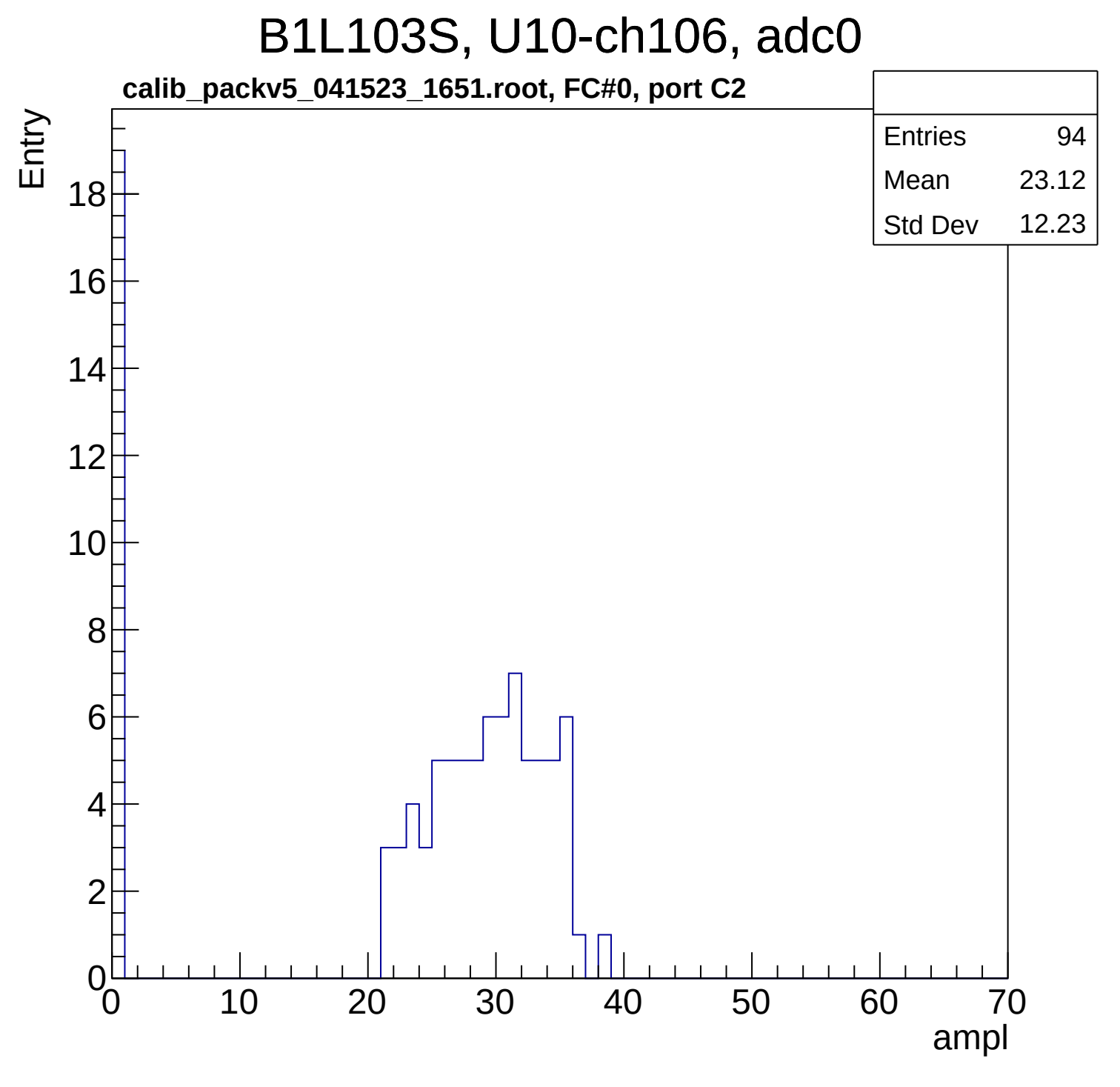
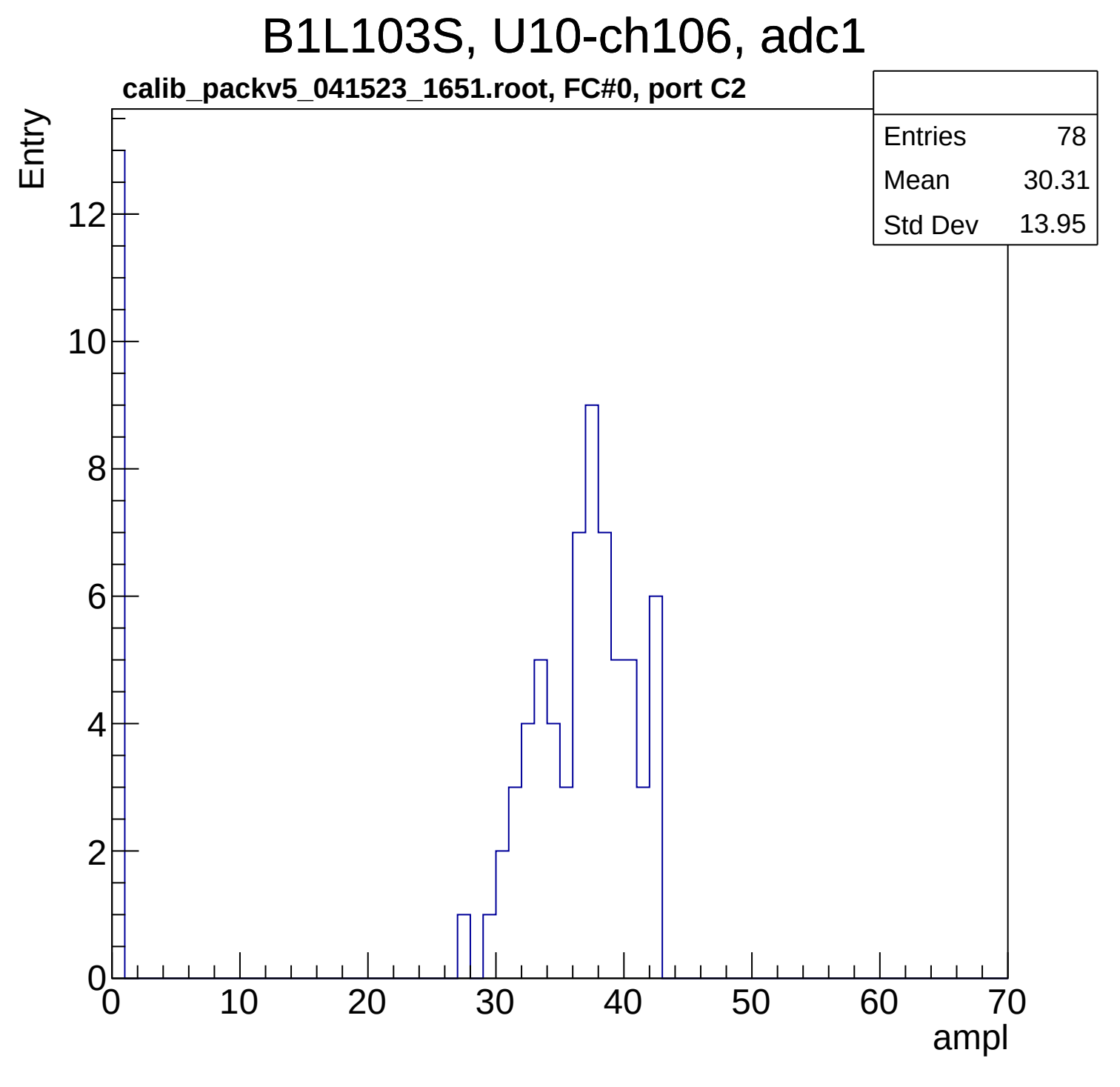
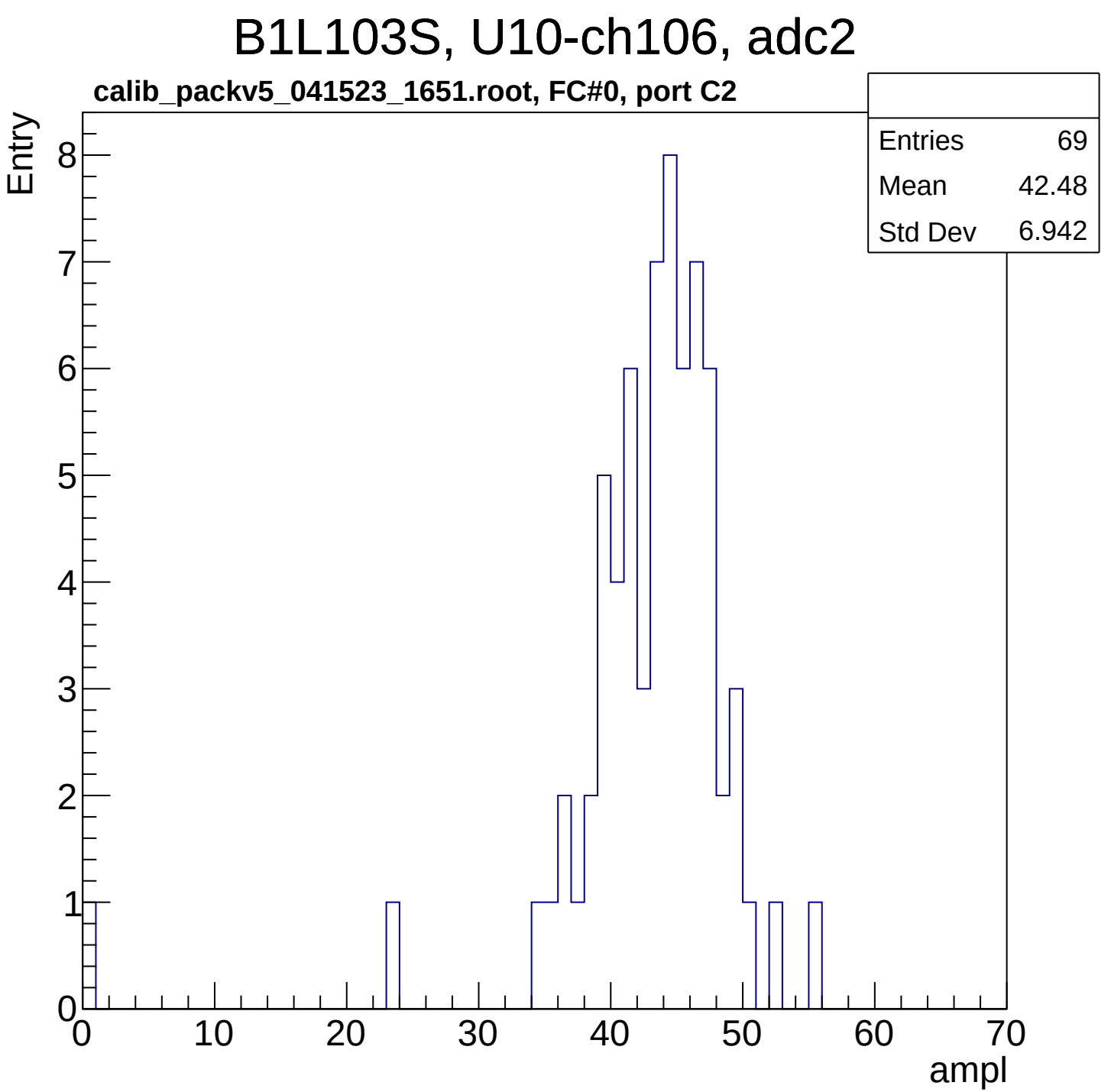

B1L103S, U10-ch105, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 59
Std Dev 2.618
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch105, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 17
Mean 57.59
Std Dev 14.57
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U10-ch105, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch106, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 94
Mean 23.12
Std Dev 12.23
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch106, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 30.31
Std Dev 13.95
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch106, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 42.48
Std Dev 6.942
Entry
ampl
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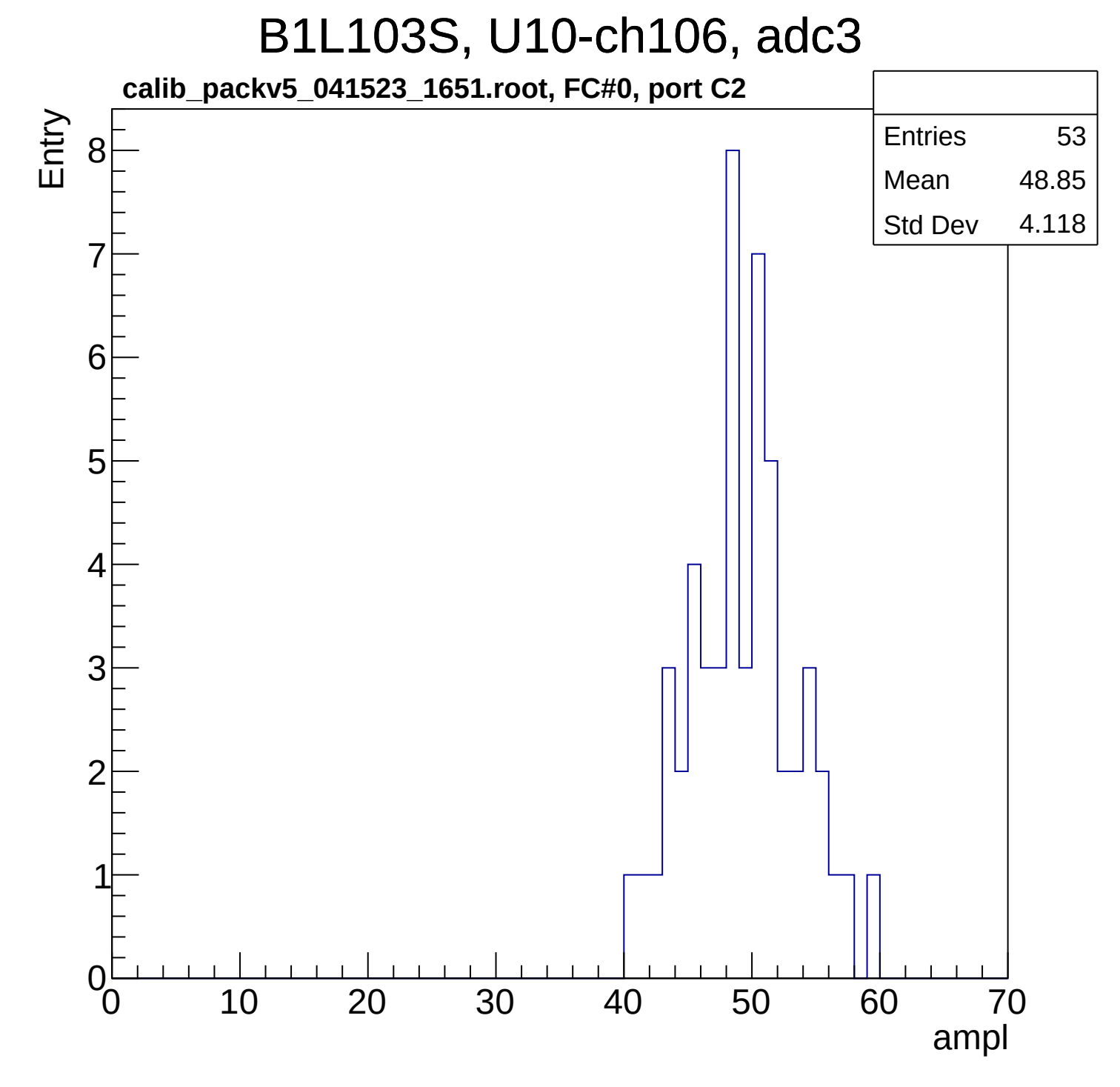
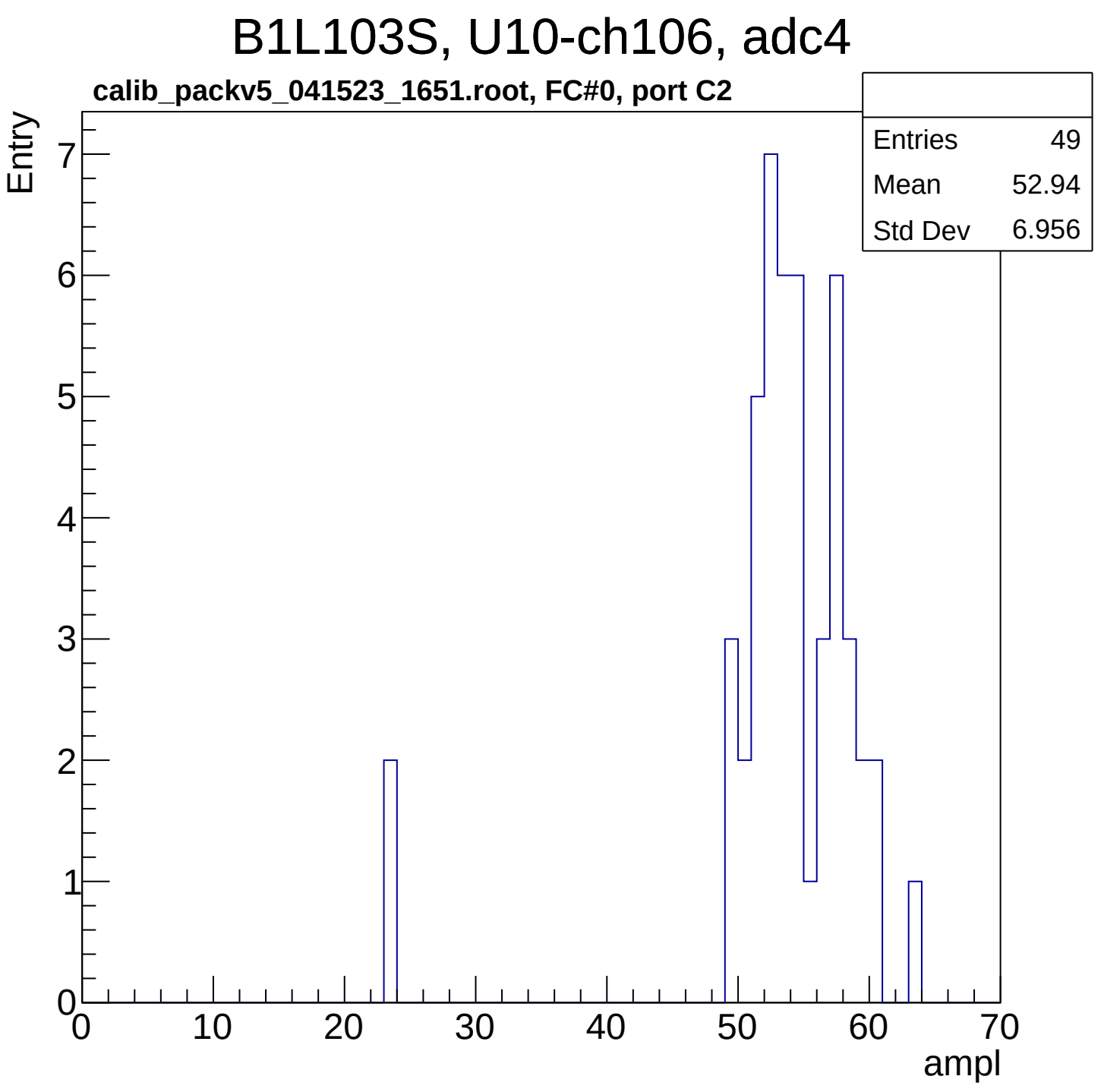
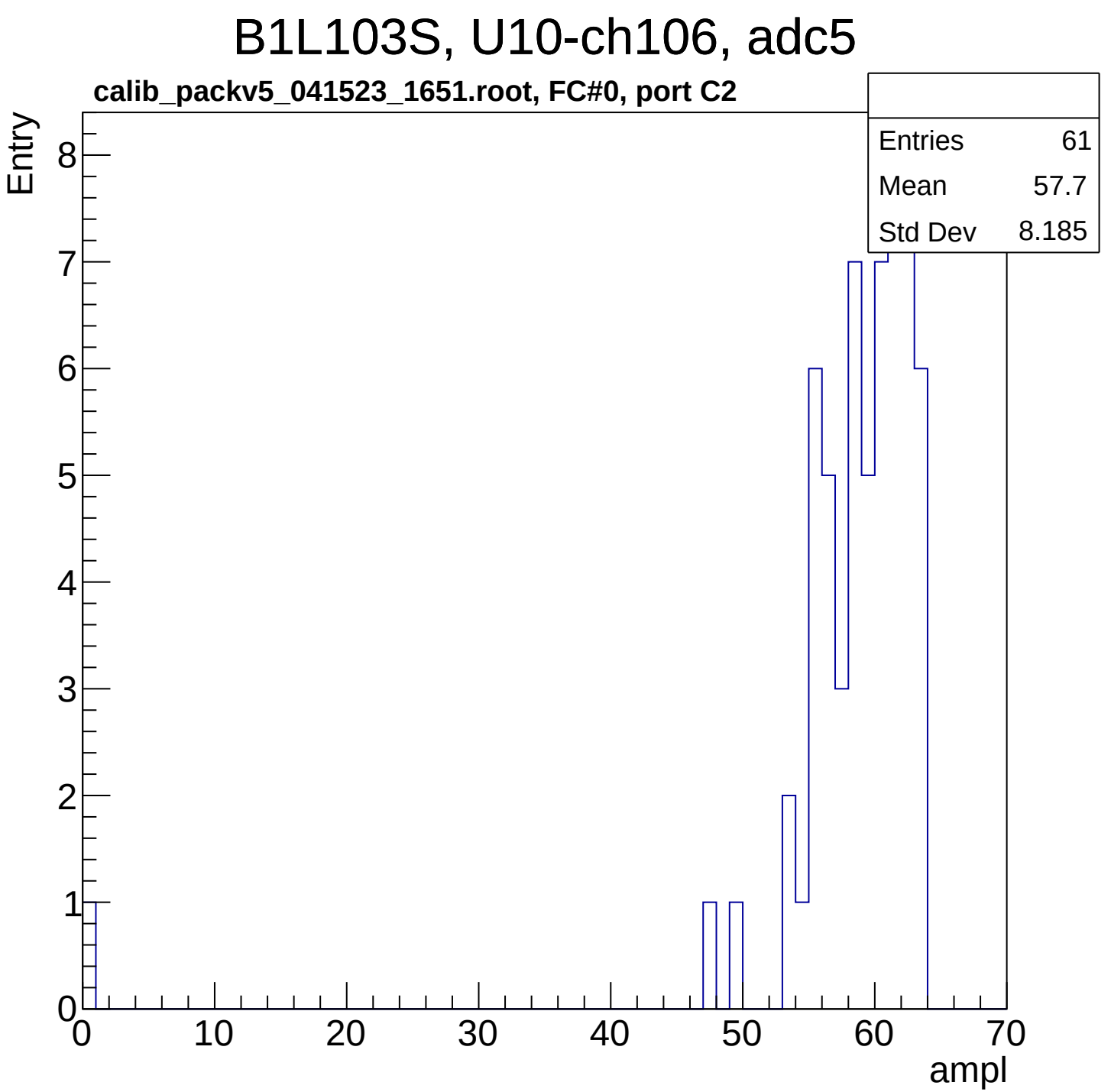
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U10-ch106, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 48.85
Std Dev 4.118
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U10-ch106, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 52.94
Std Dev 6.956
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U10-ch106, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 57.7
Std Dev 8.185
Entry
ampl
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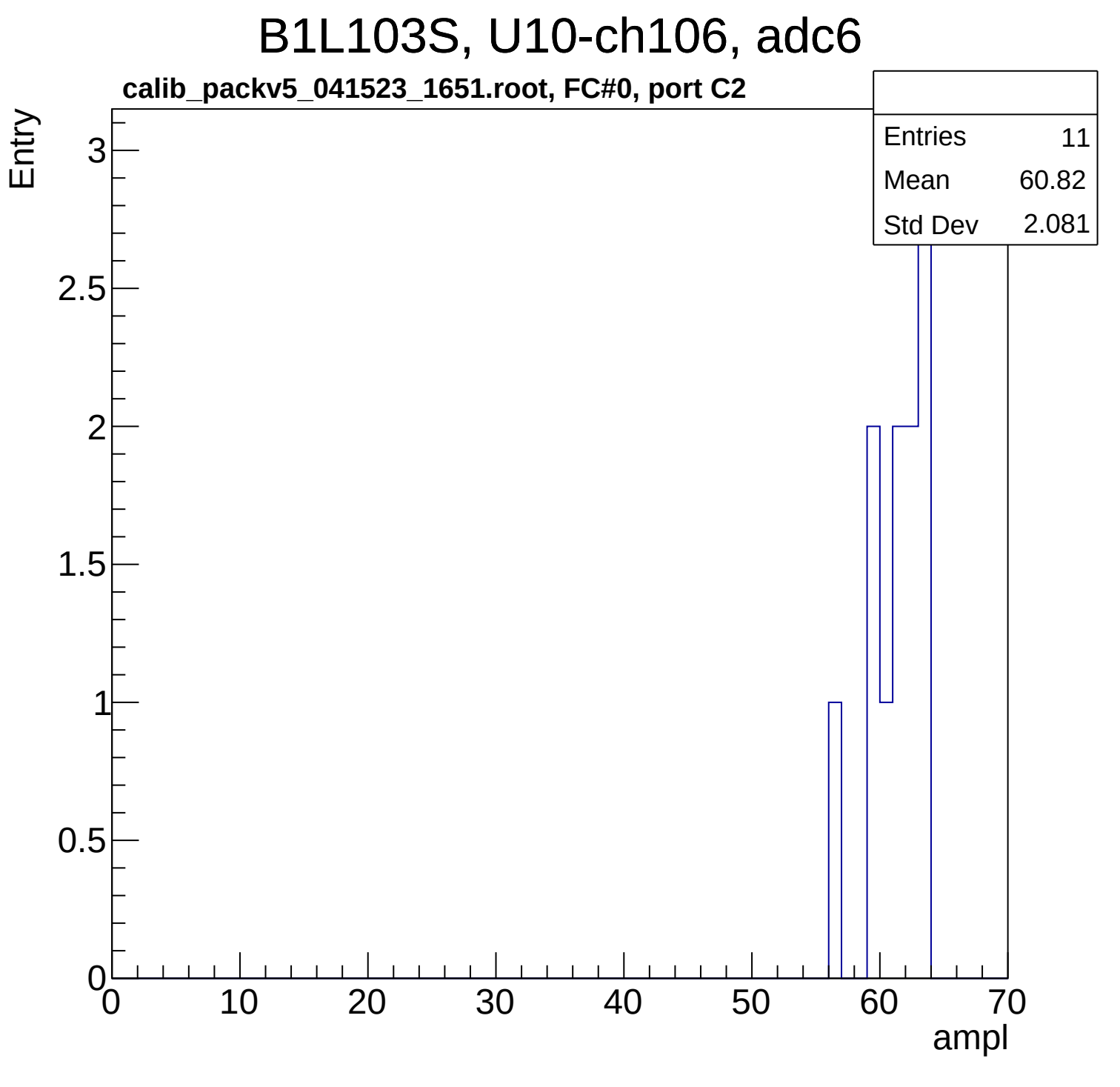
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U10-ch106, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 60.82
Std Dev 2.081
Entry
ampl
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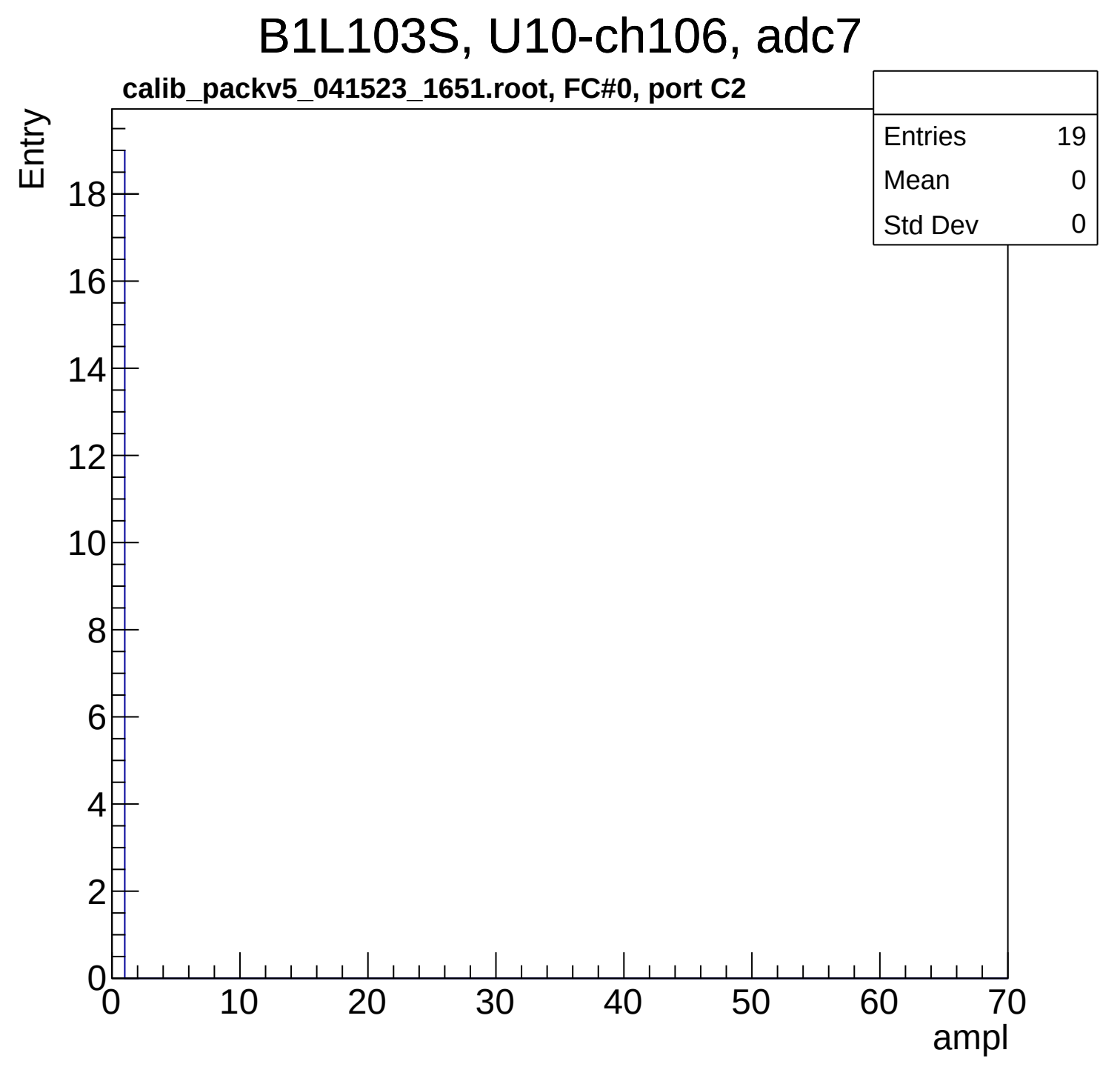
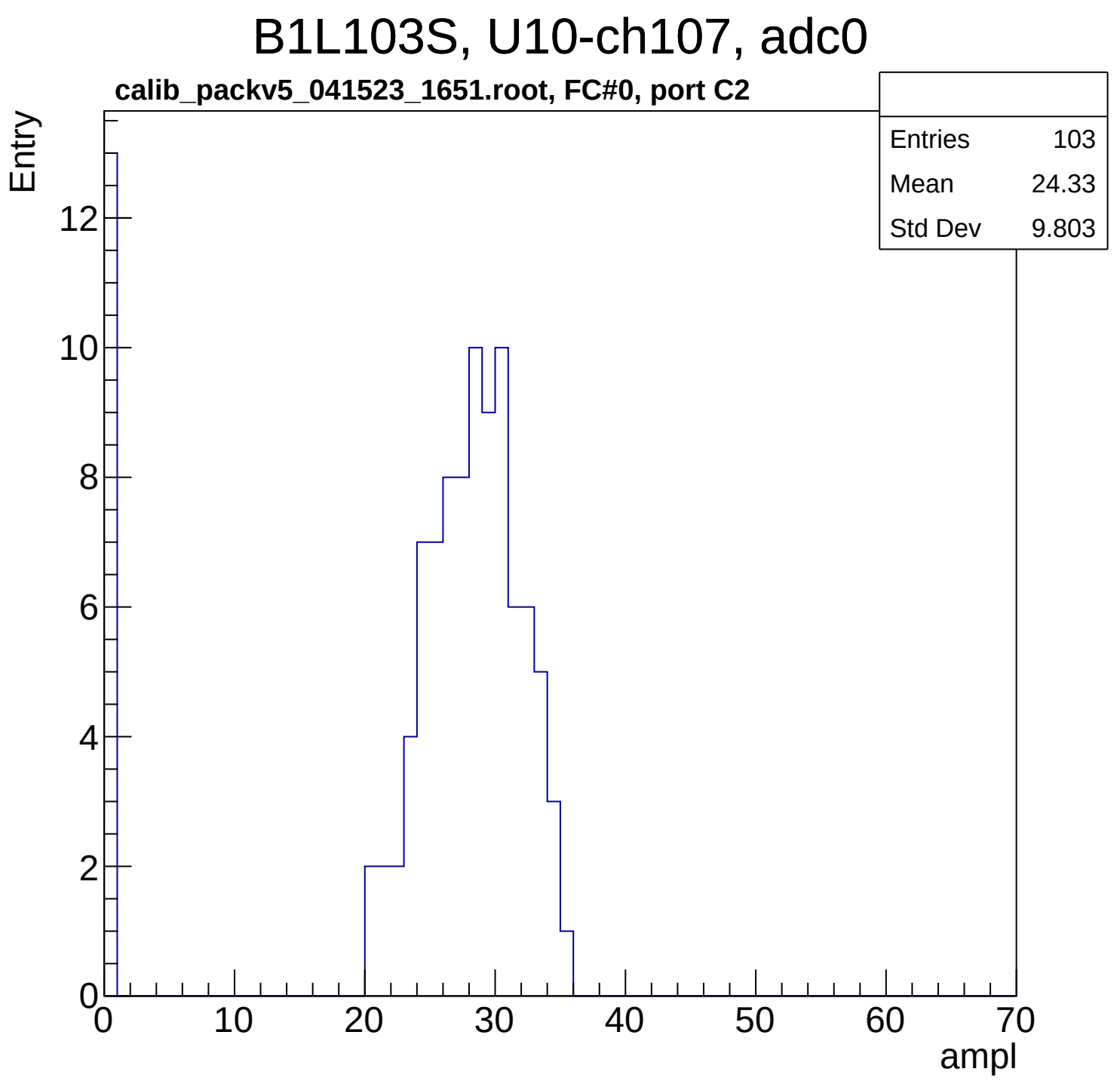
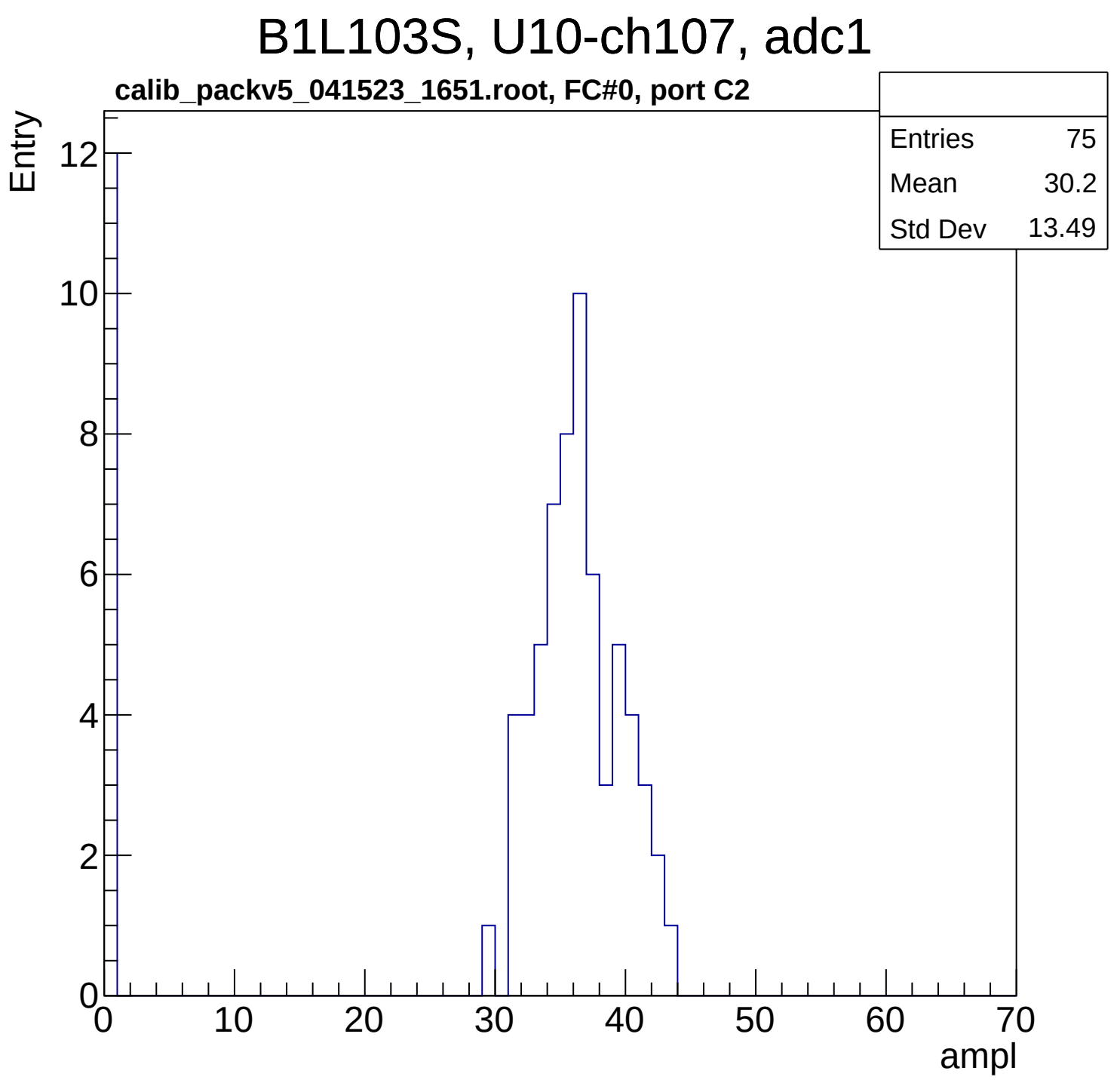
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U10-ch106, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch107, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 103
Mean 24.33
Std Dev 9.803
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch107, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 30.2
Std Dev 13.49
Entry
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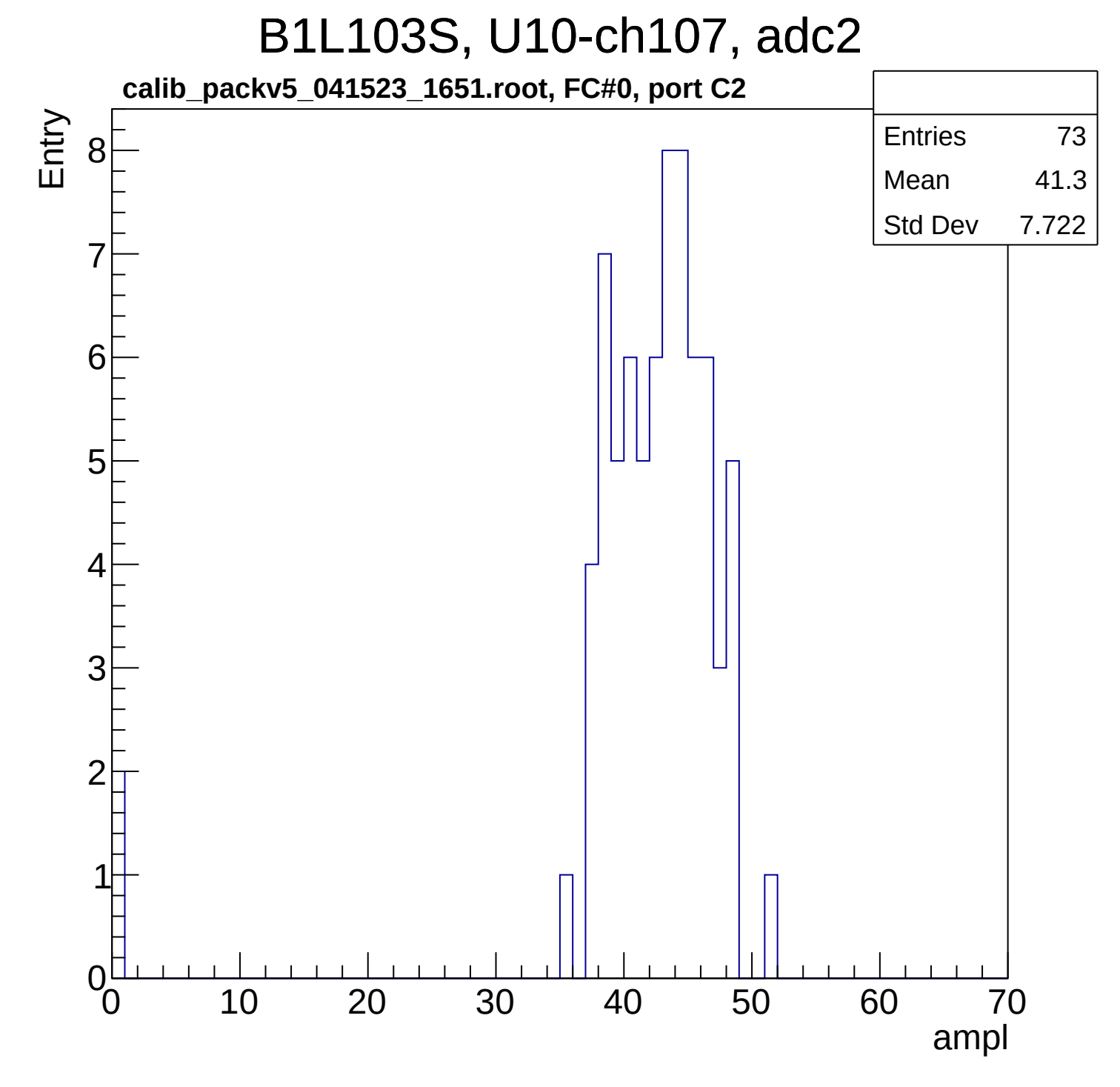
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch107, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 41.3
Std Dev 7.722
Entry
ampl
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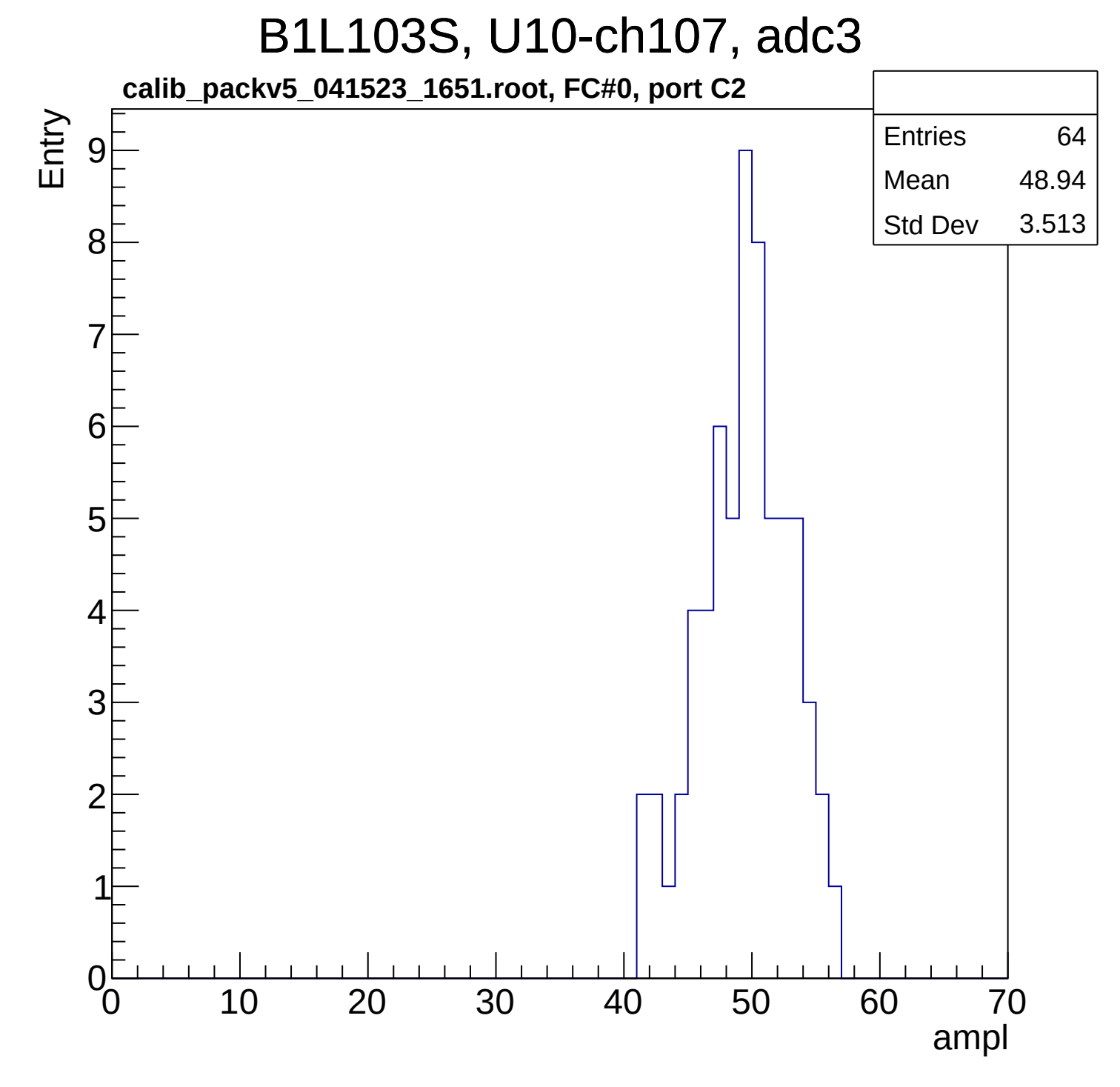
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U10-ch107, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 48.94
Std Dev 3.513
Entry
ampl
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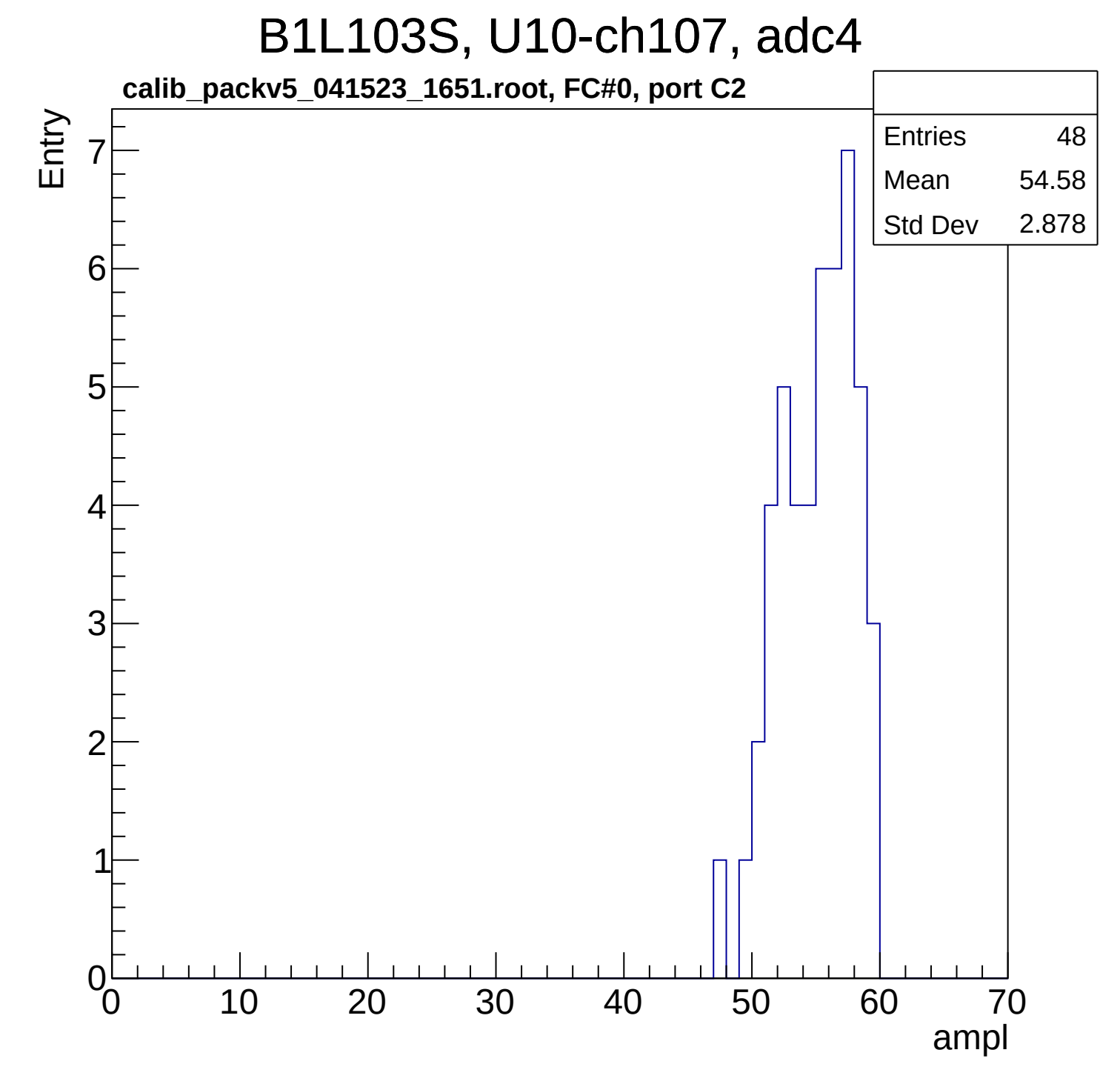
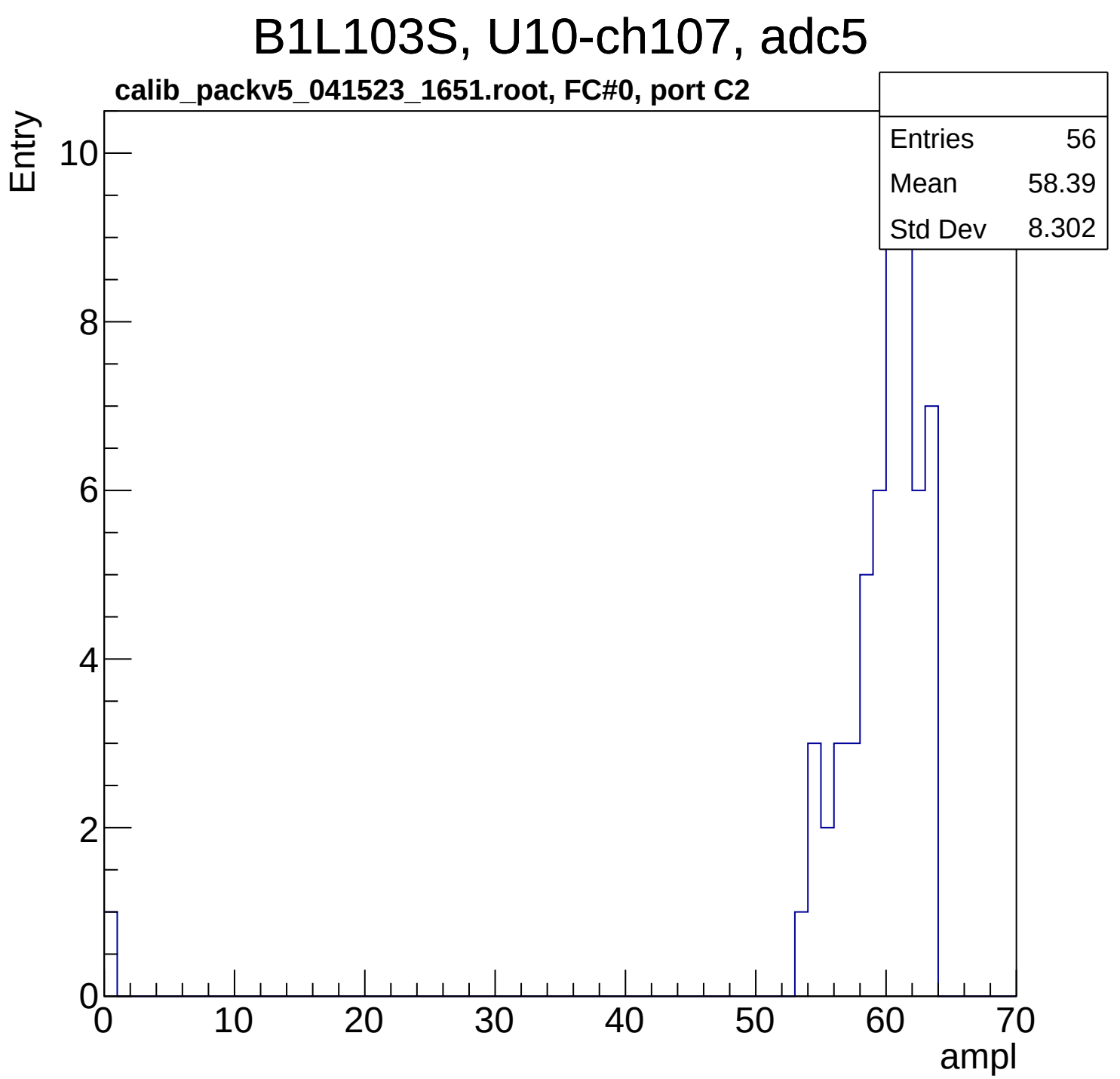
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U10-ch107, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 54.58
Std Dev 2.878
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U10-ch107, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 58.39
Std Dev 8.302
Entry
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4
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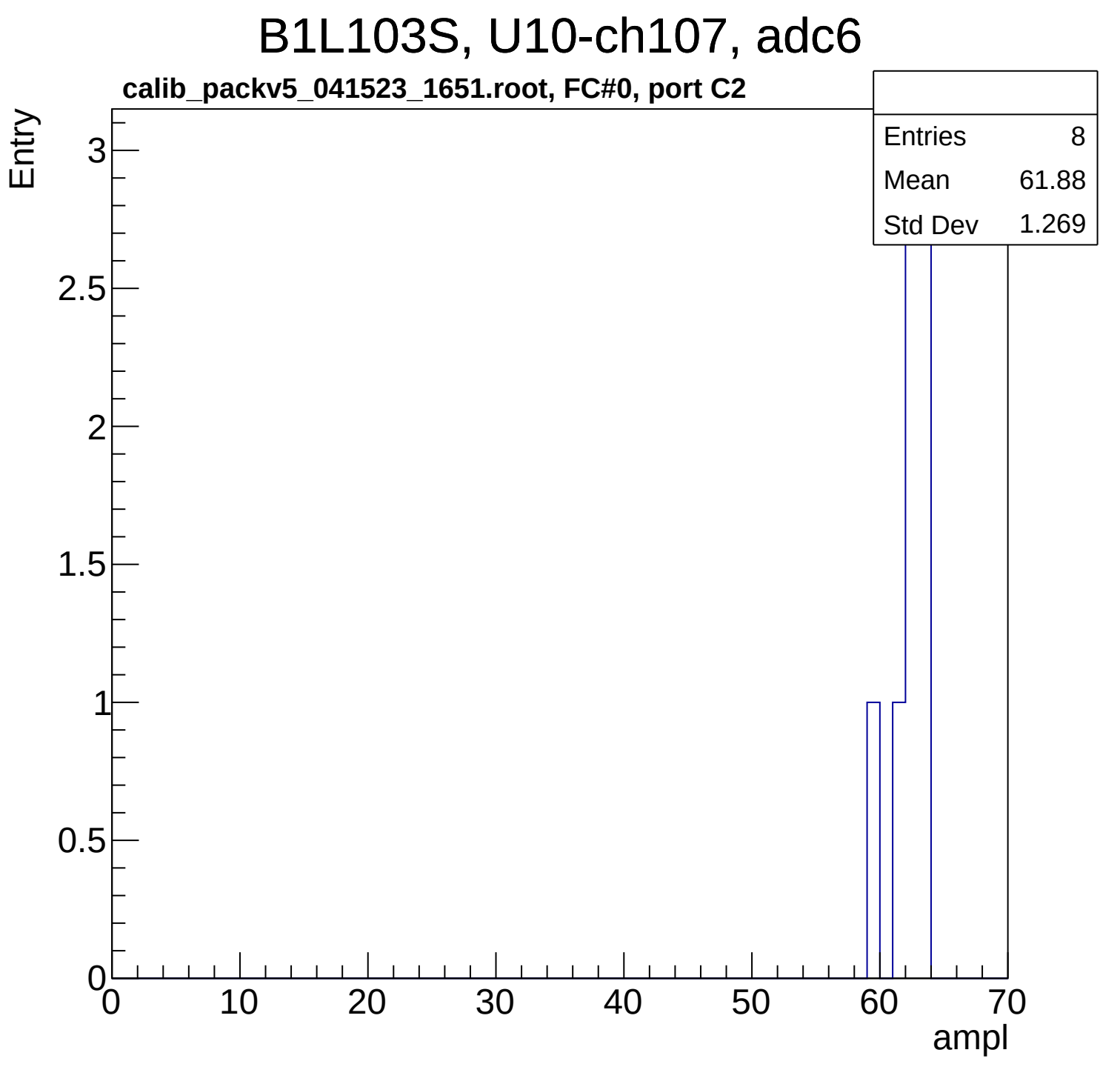
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch107, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 61.88
Std Dev 1.269
Entry
ampl
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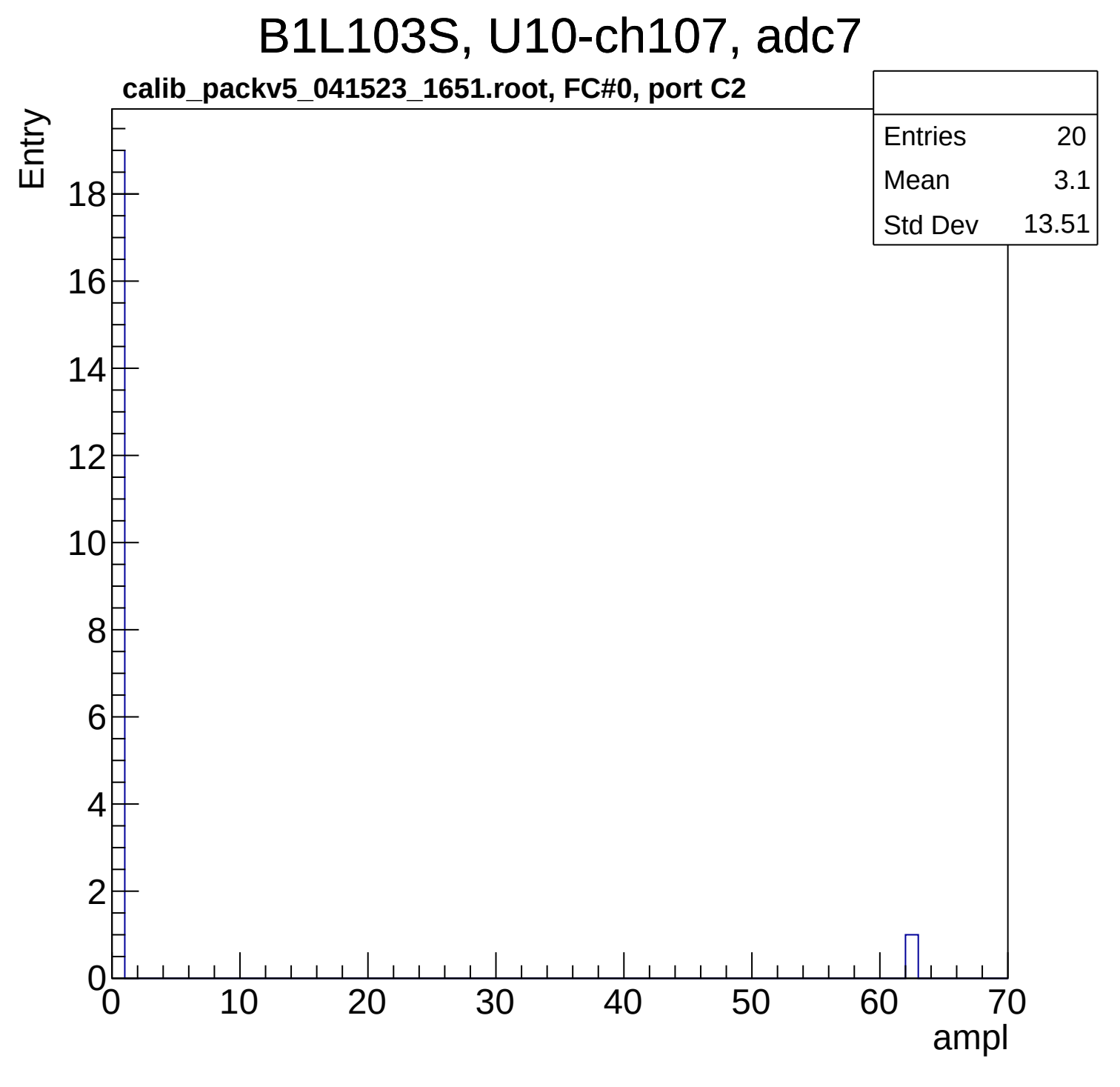
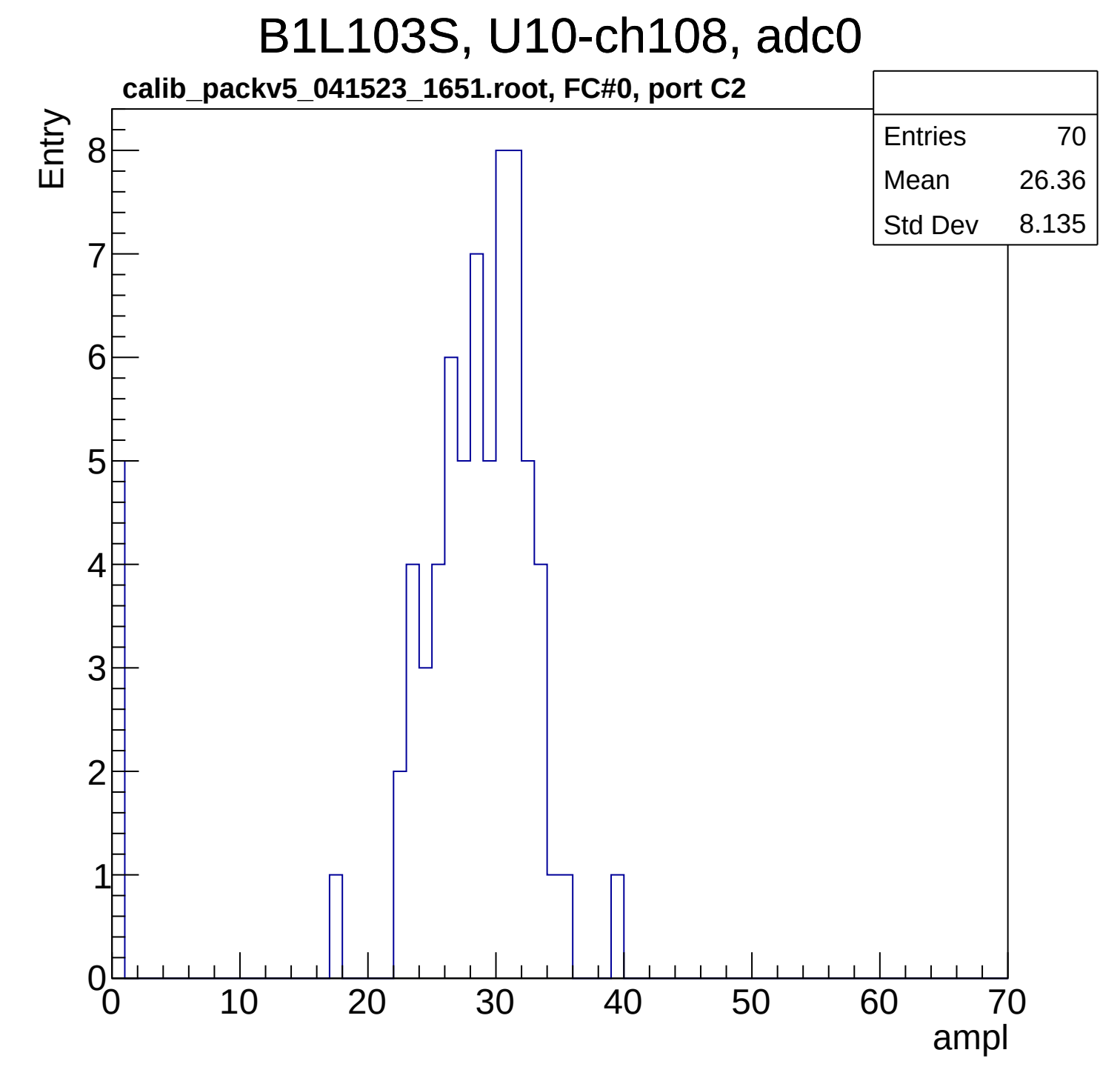
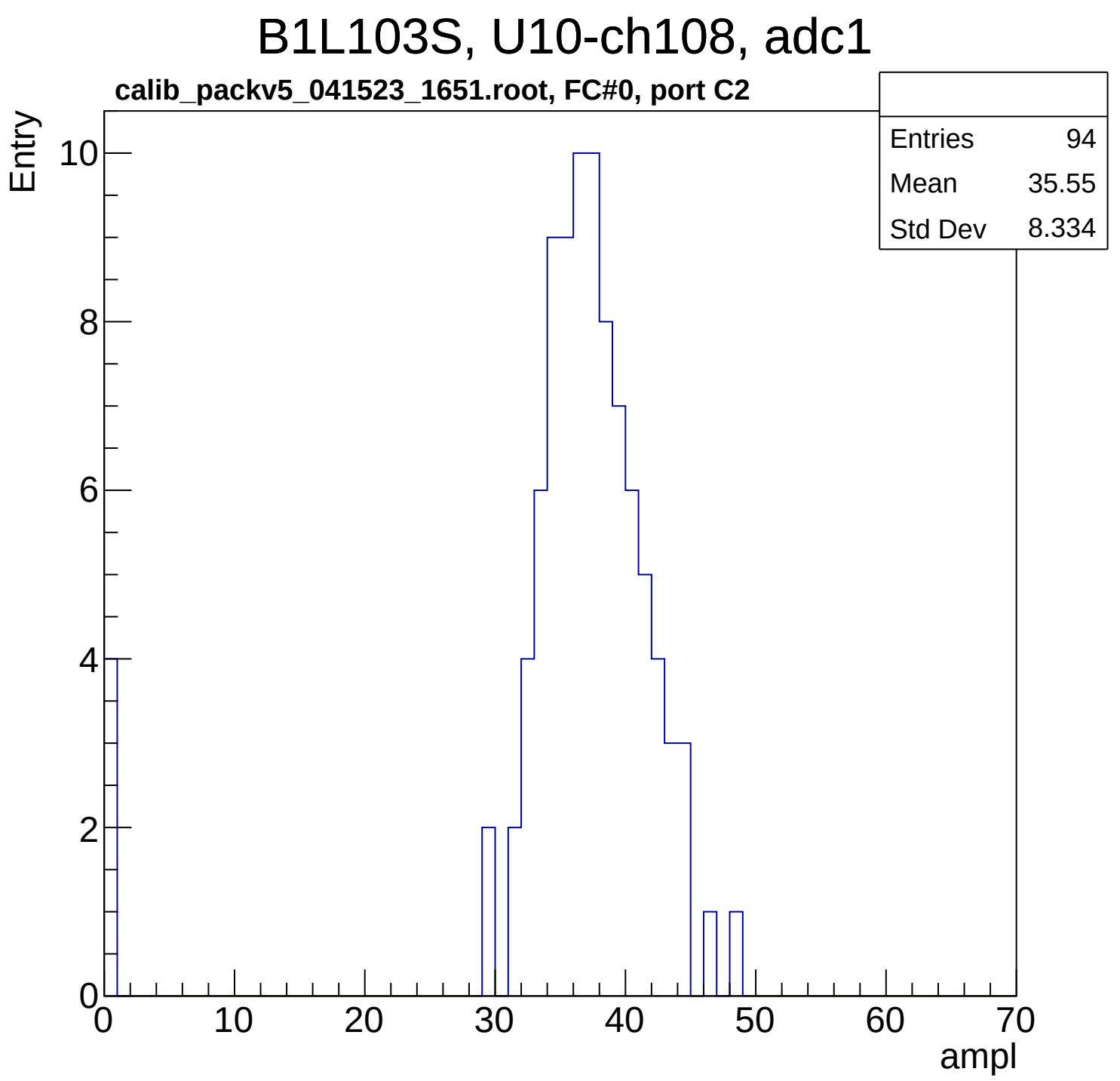
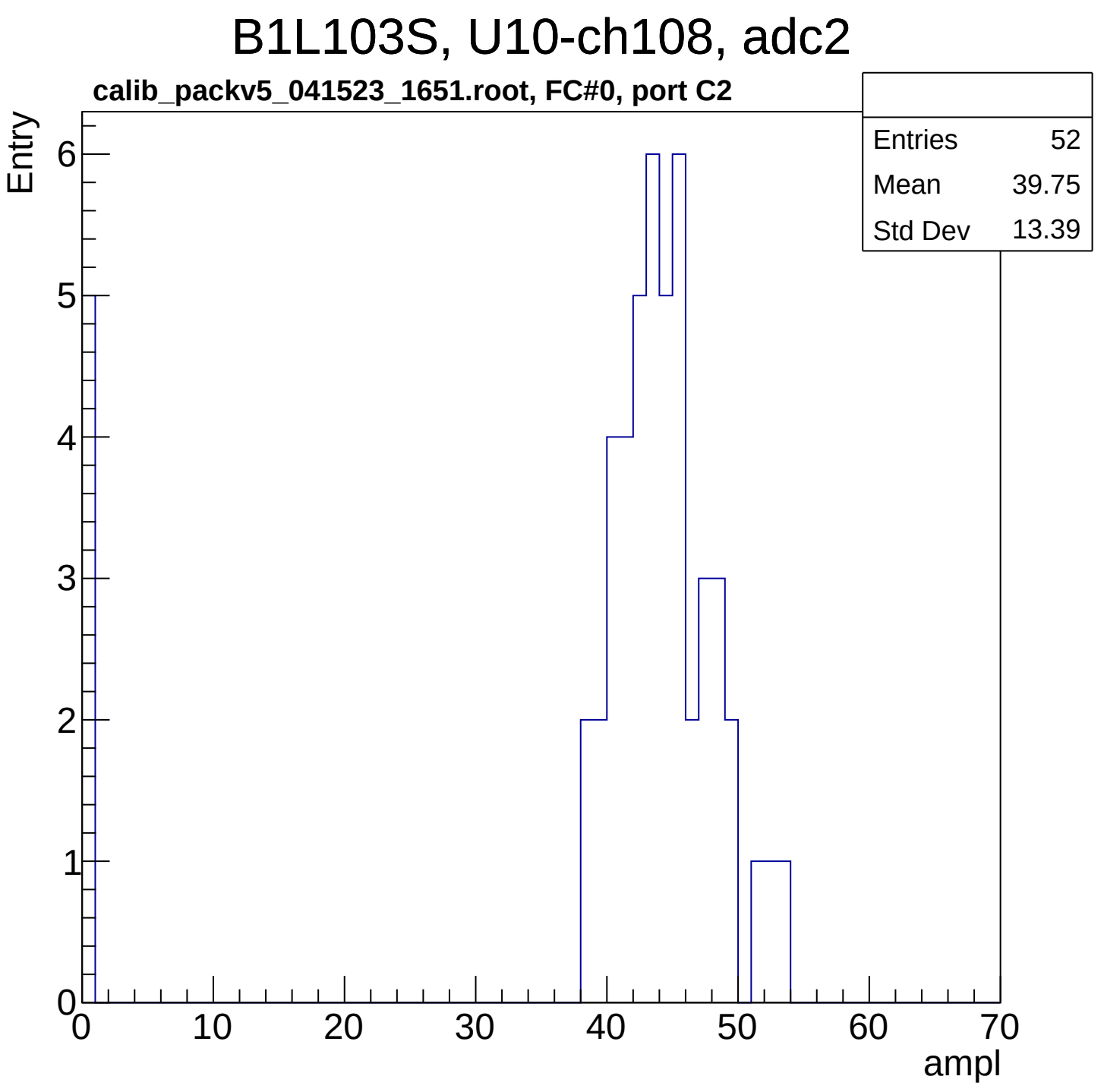
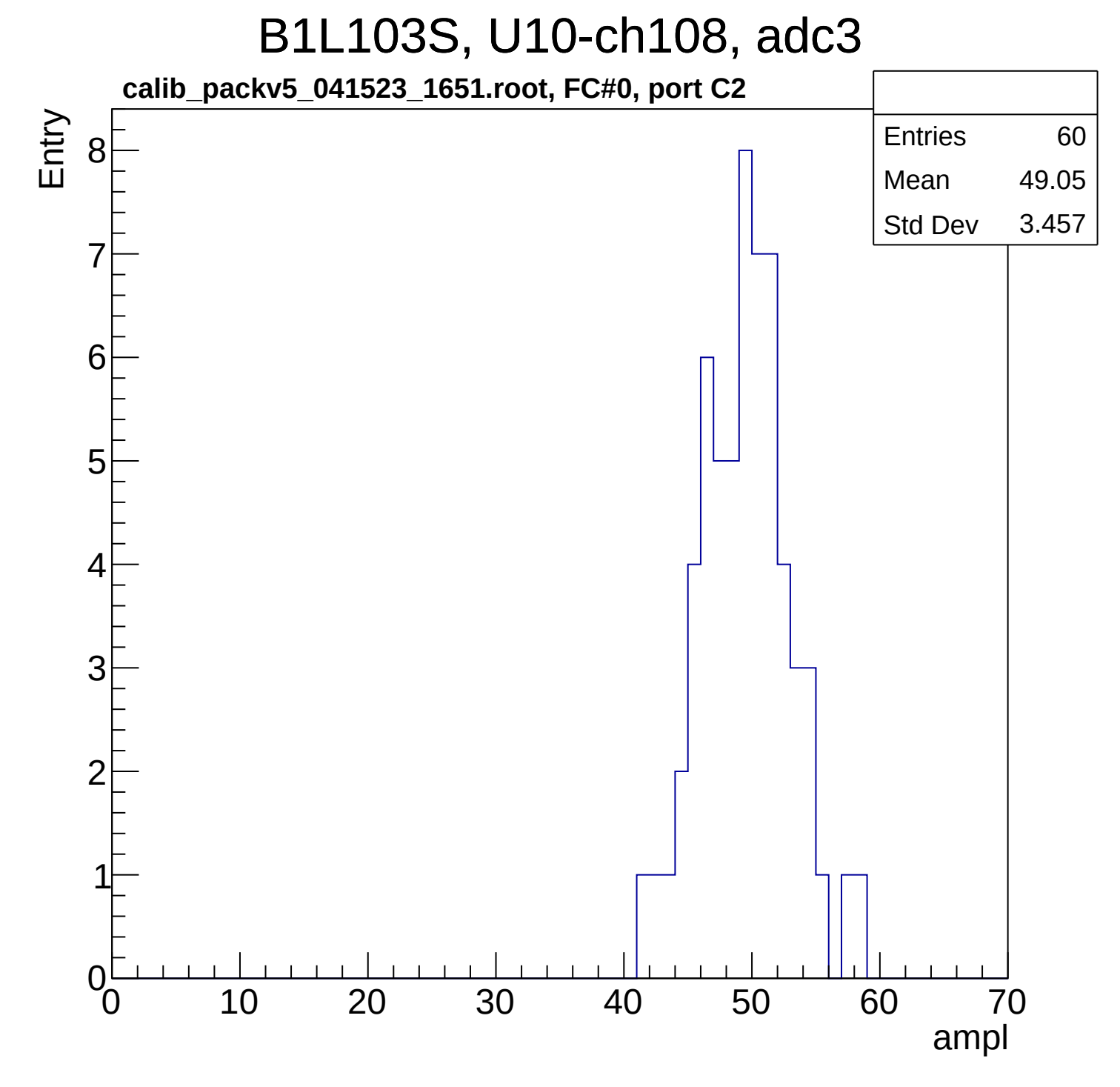
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

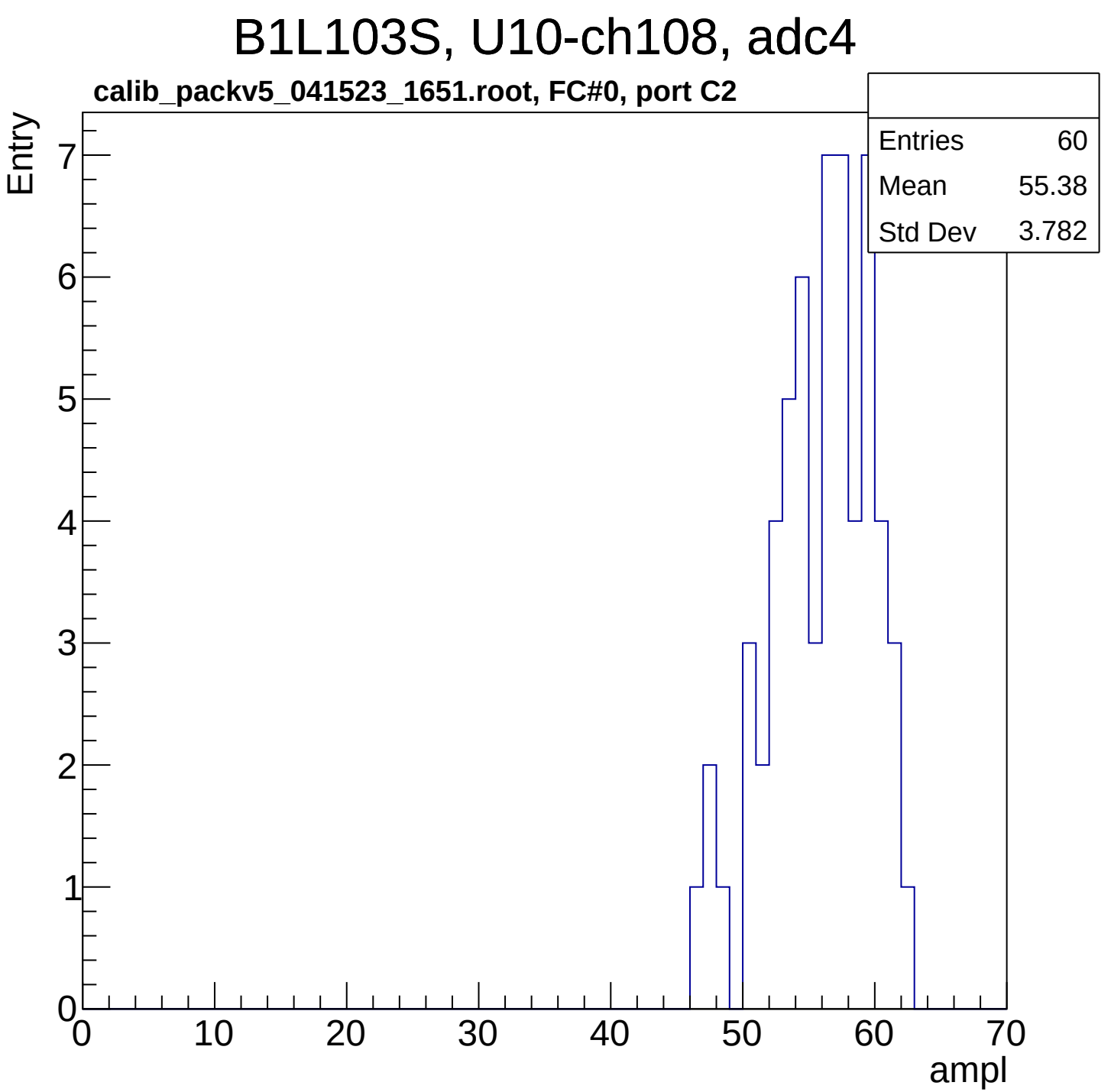

B1L103S, U10-ch107, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.1
Std Dev 13.51
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch108, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 26.36
Std Dev 8.135
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U10-ch108, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 94
Mean 35.55
Std Dev 8.334
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U10-ch108, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 39.75
Std Dev 13.39
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch108, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 49.05
Std Dev 3.457
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U10-ch108, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 55.38
Std Dev 3.782
Entry
ampl
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1
2
3
4
5
6
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0
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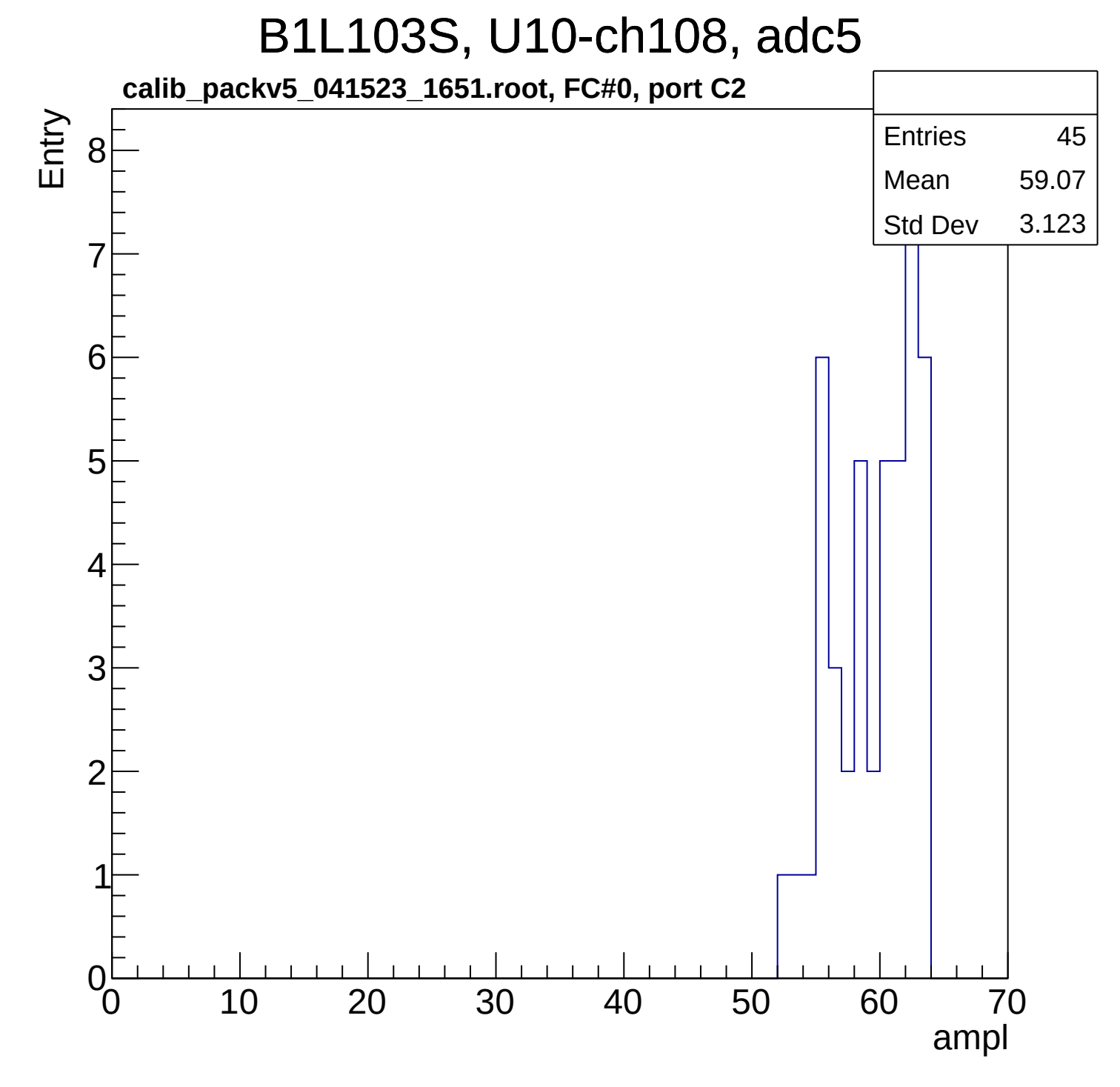
B1L103S, U10-ch108, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 59.07
Std Dev 3.123
Entry
ampl
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7
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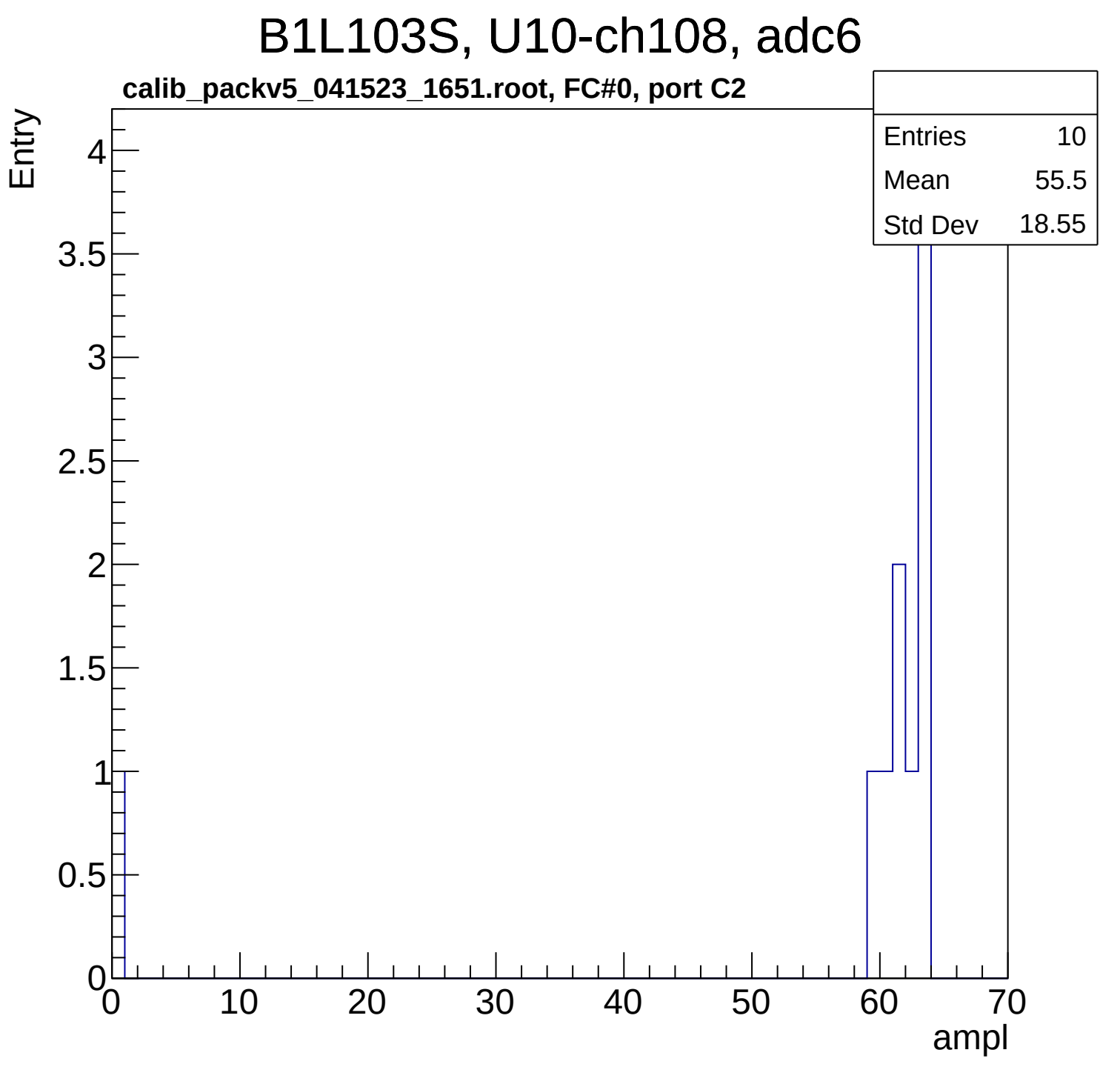
B1L103S, U10-ch108, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 55.5
Std Dev 18.55
Entry
ampl
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1.5
2
2.5
3
3.5
4
0
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60
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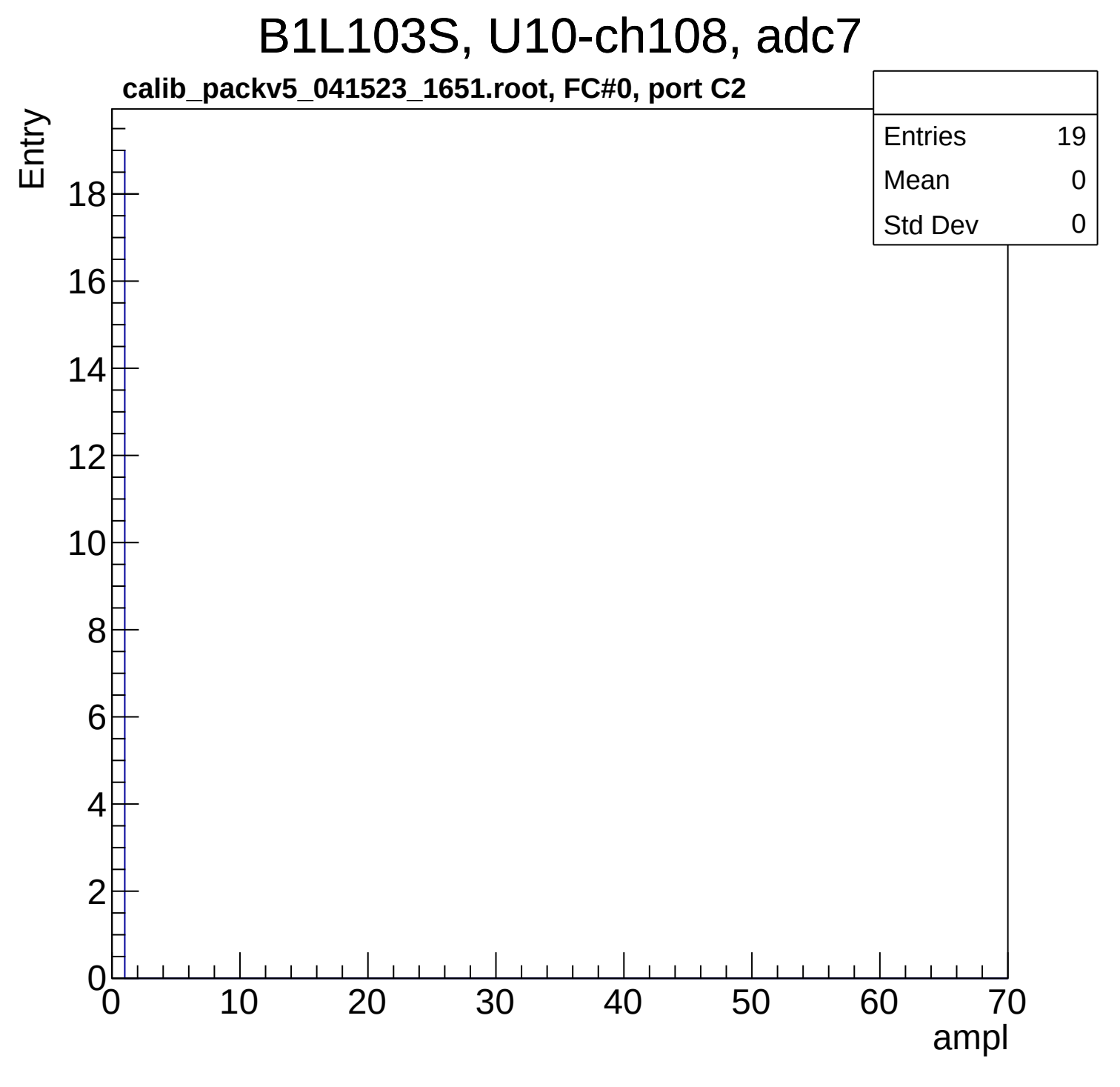
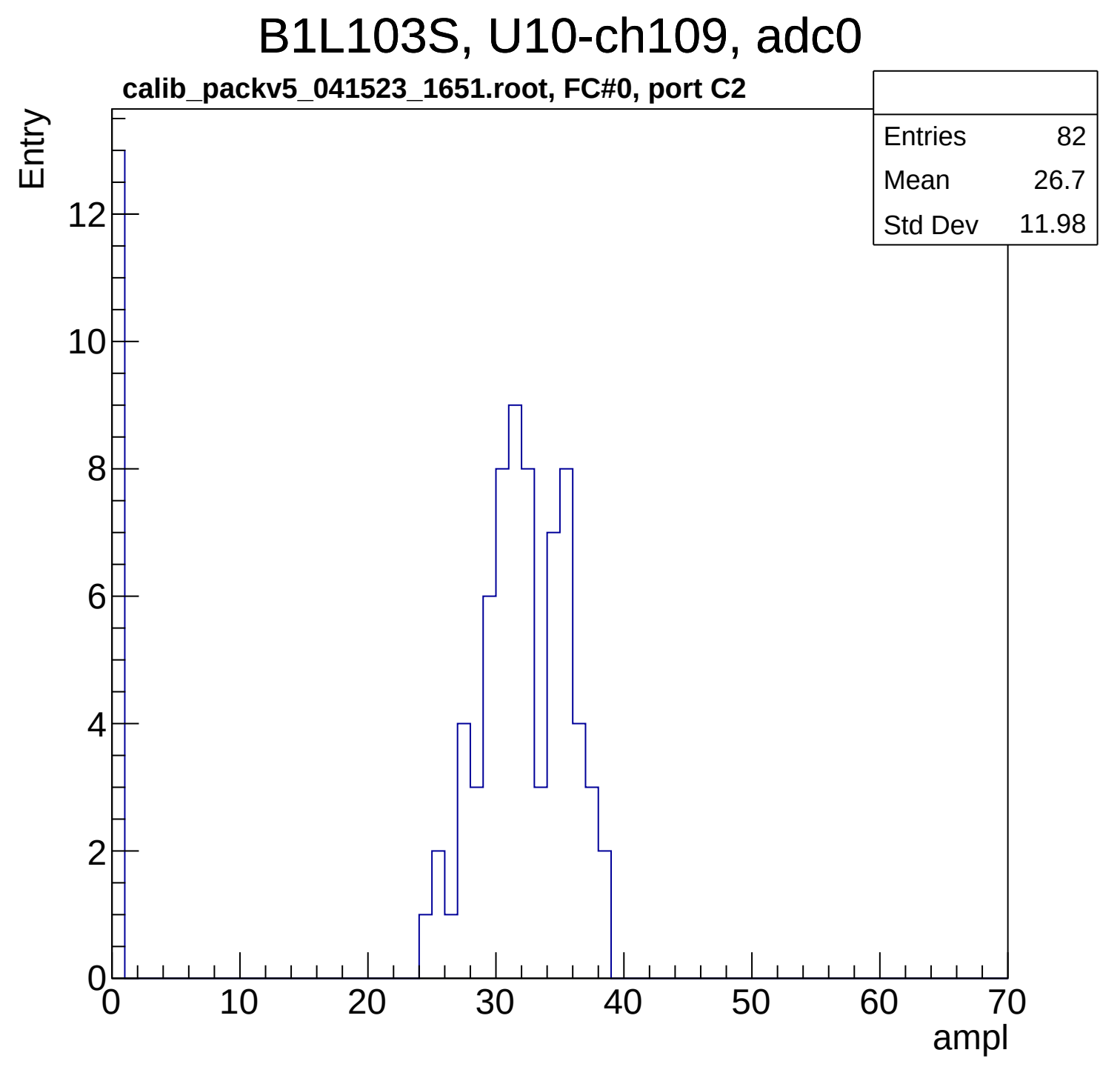

B1L103S, U10-ch108, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch109, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 26.7
Std Dev 11.98
Entry
0
2
4
6
8
10
12
0
10
20
30
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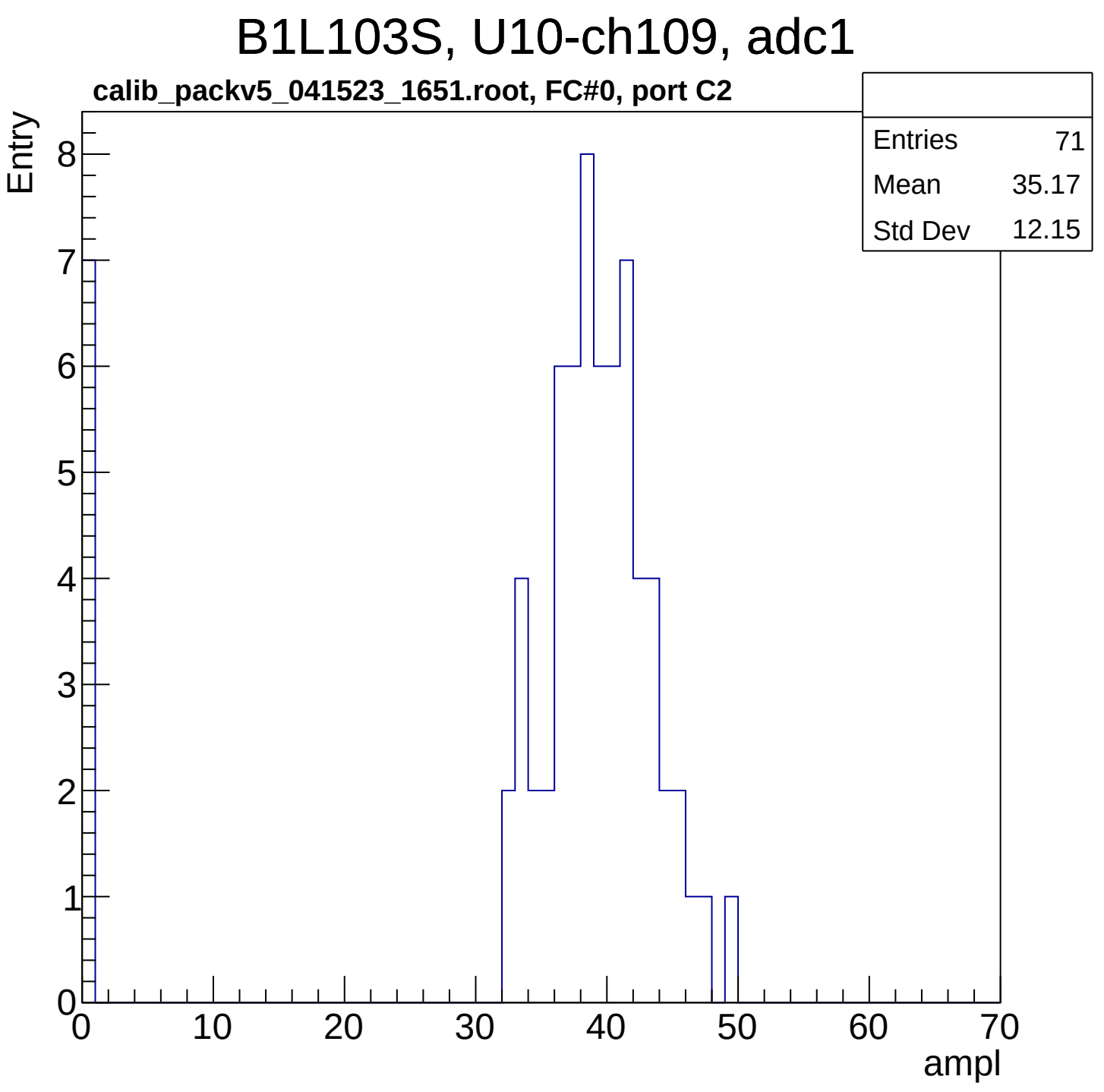
50
60
70
ampl


B1L103S, U10-ch109, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 35.17
Std Dev 12.15
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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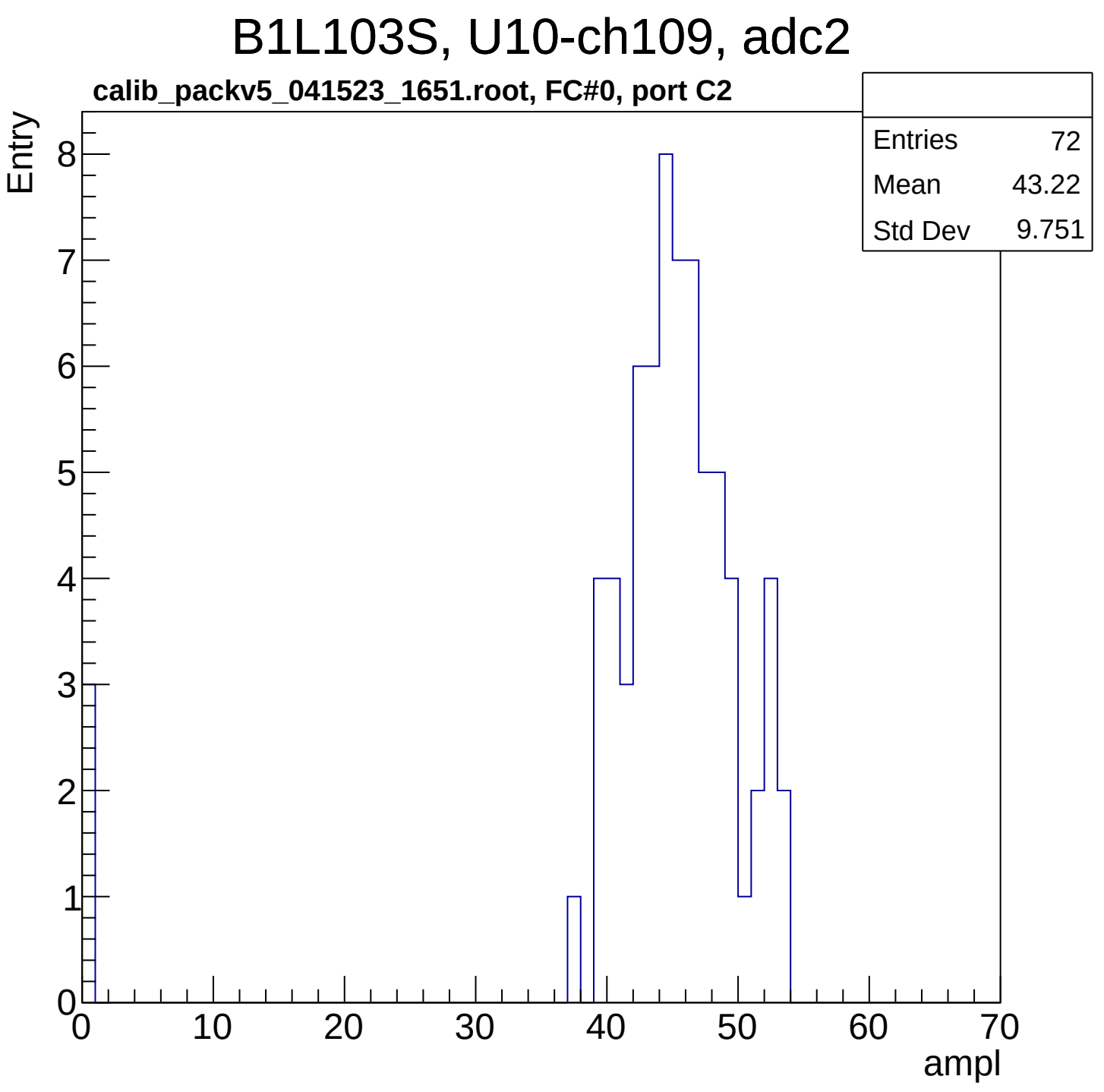
B1L103S, U10-ch109, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 43.22
Std Dev 9.751
Entry
ampl
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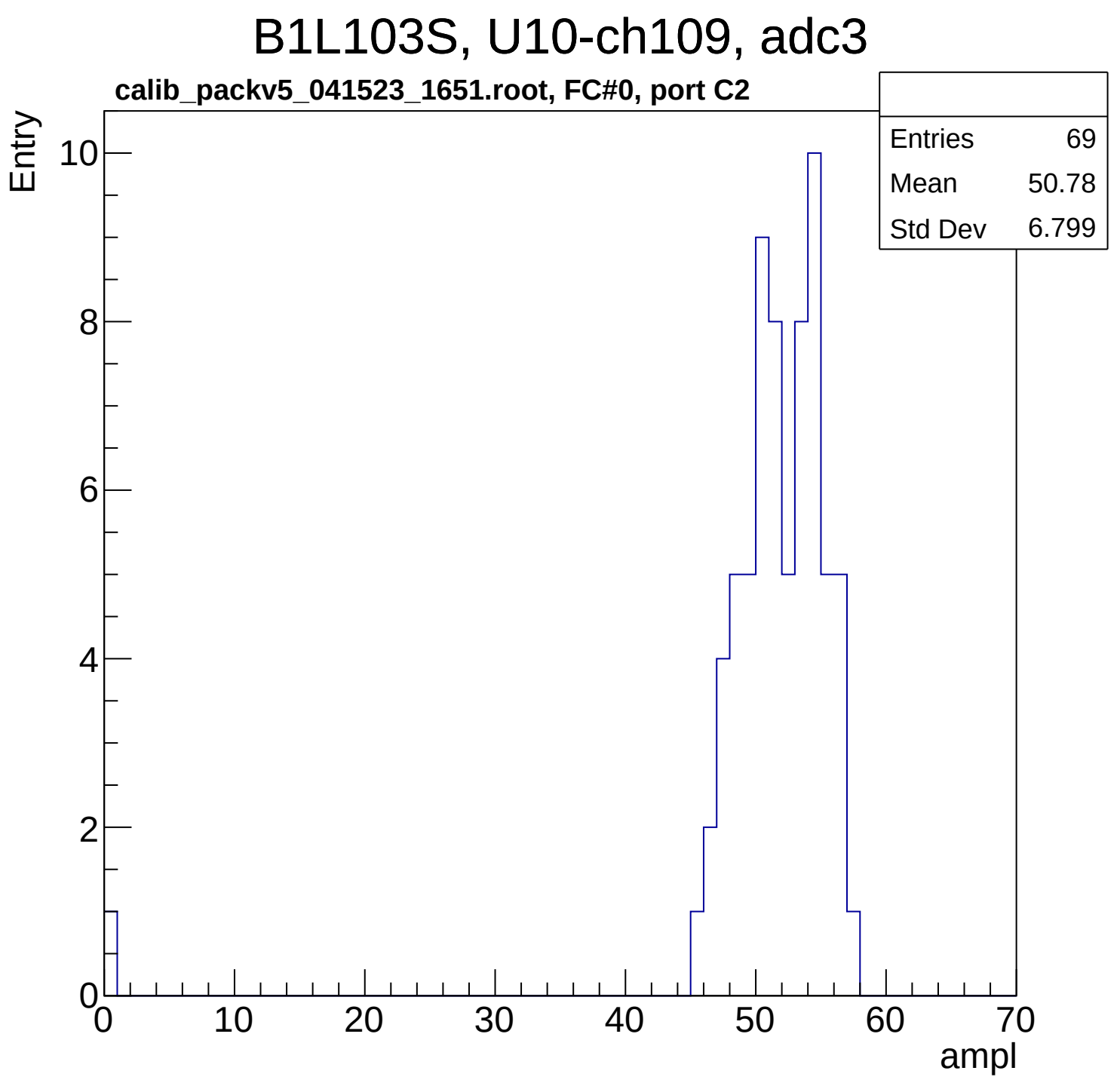
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U10-ch109, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 50.78
Std Dev 6.799
Entry
ampl
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2
4
6
8
10
0
10
20
30
40
50
60
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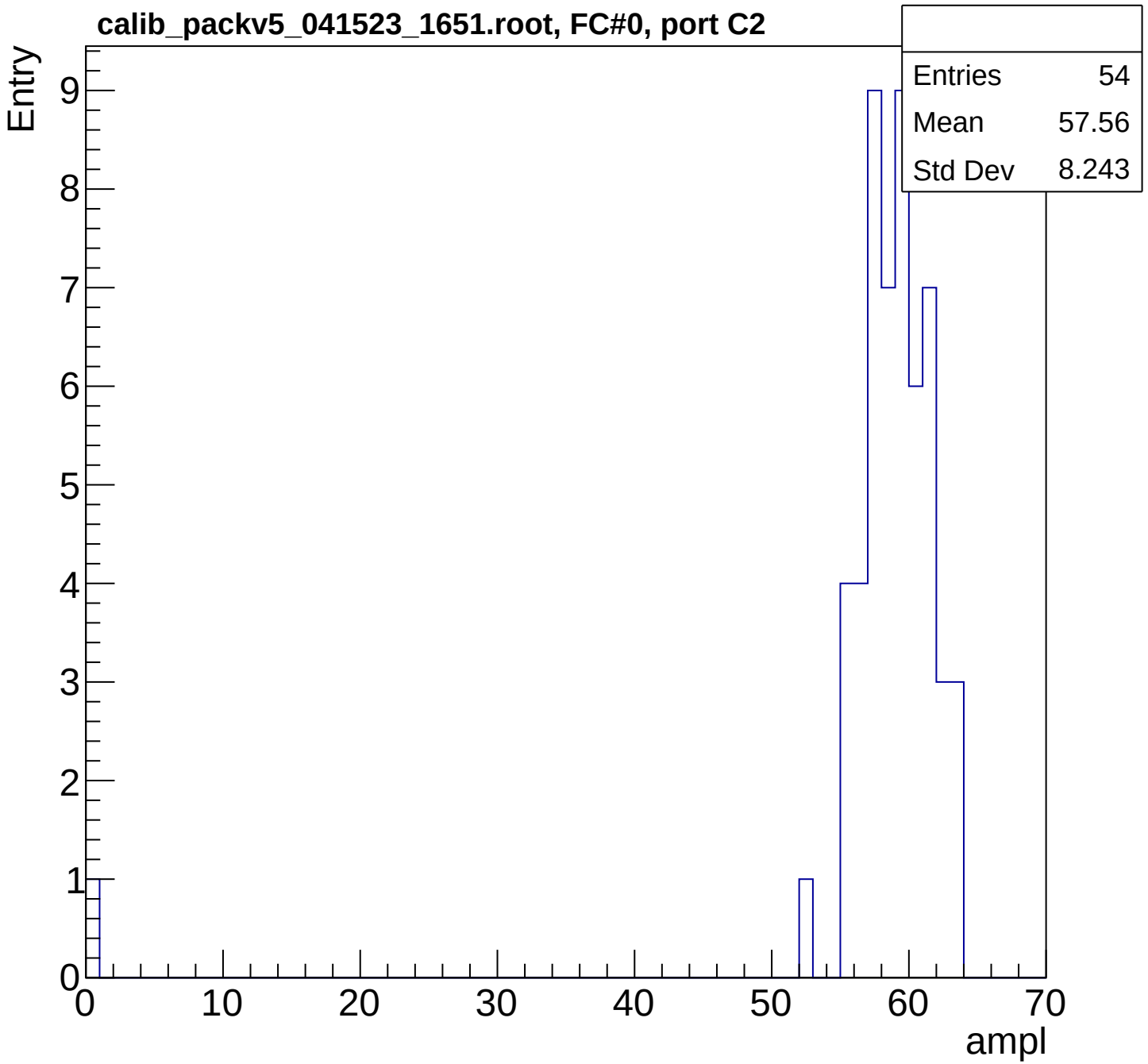
B1L103S, U10-ch109, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 57.56
Std Dev 8.243
Entry
ampl
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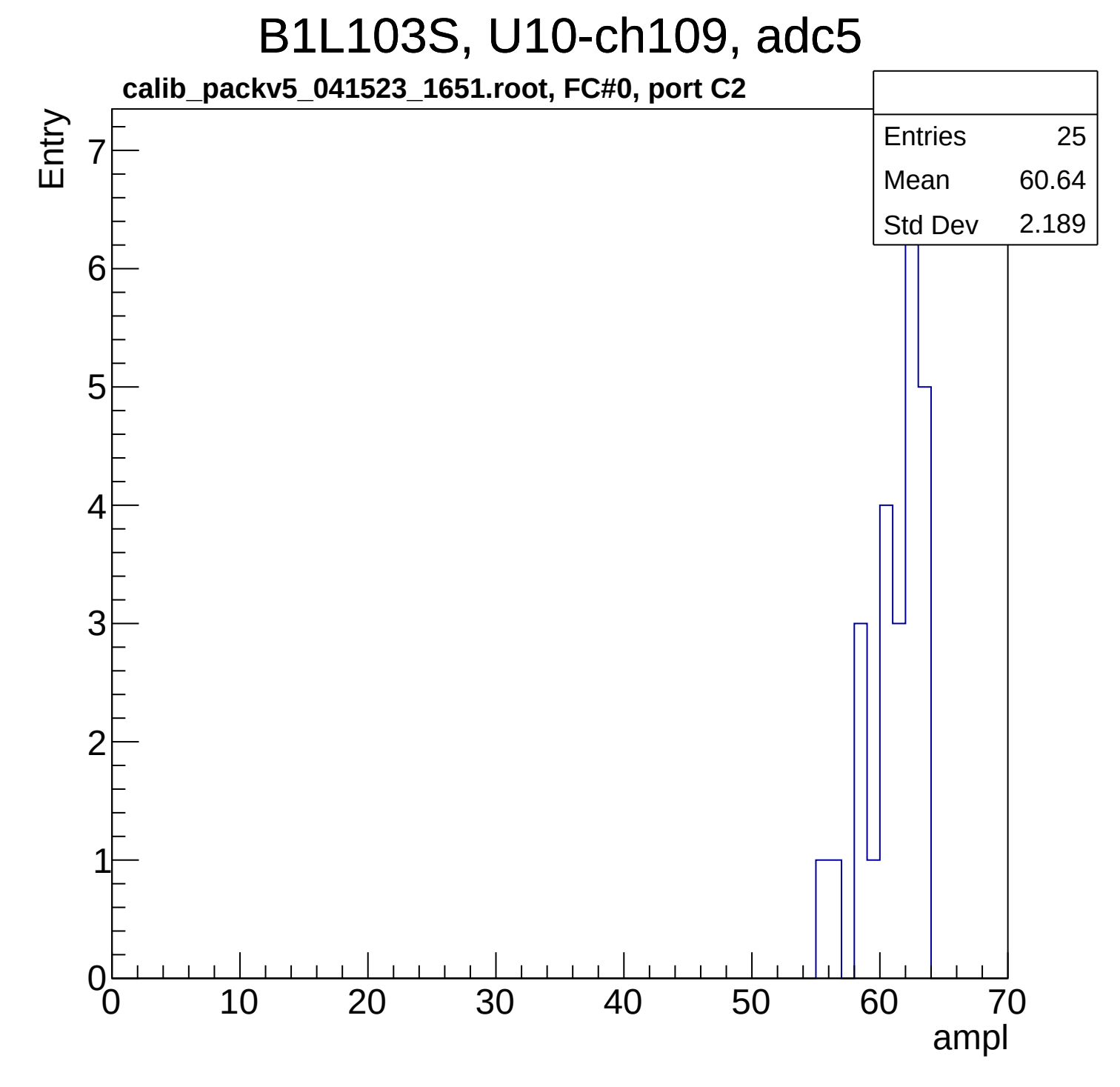
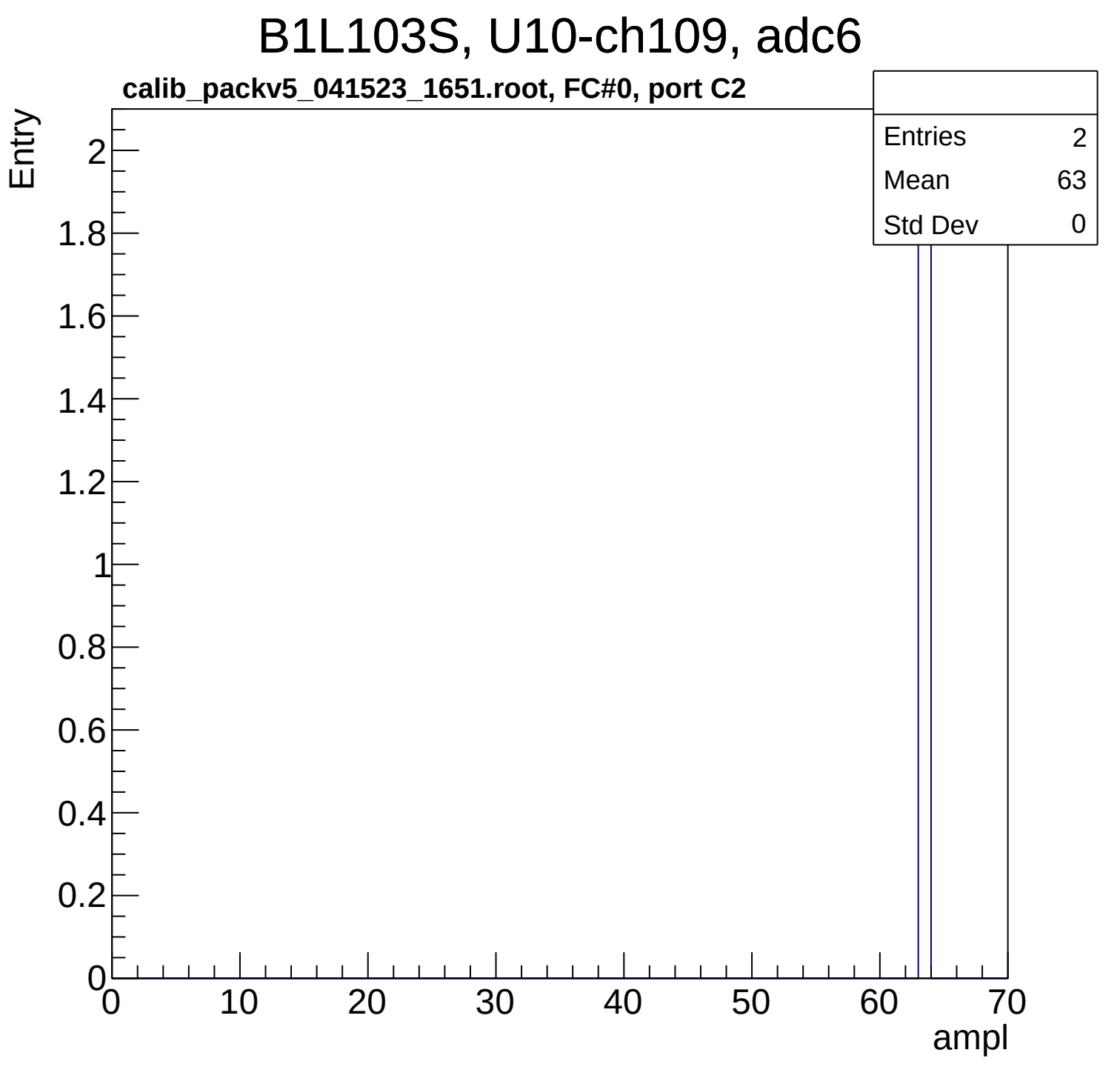
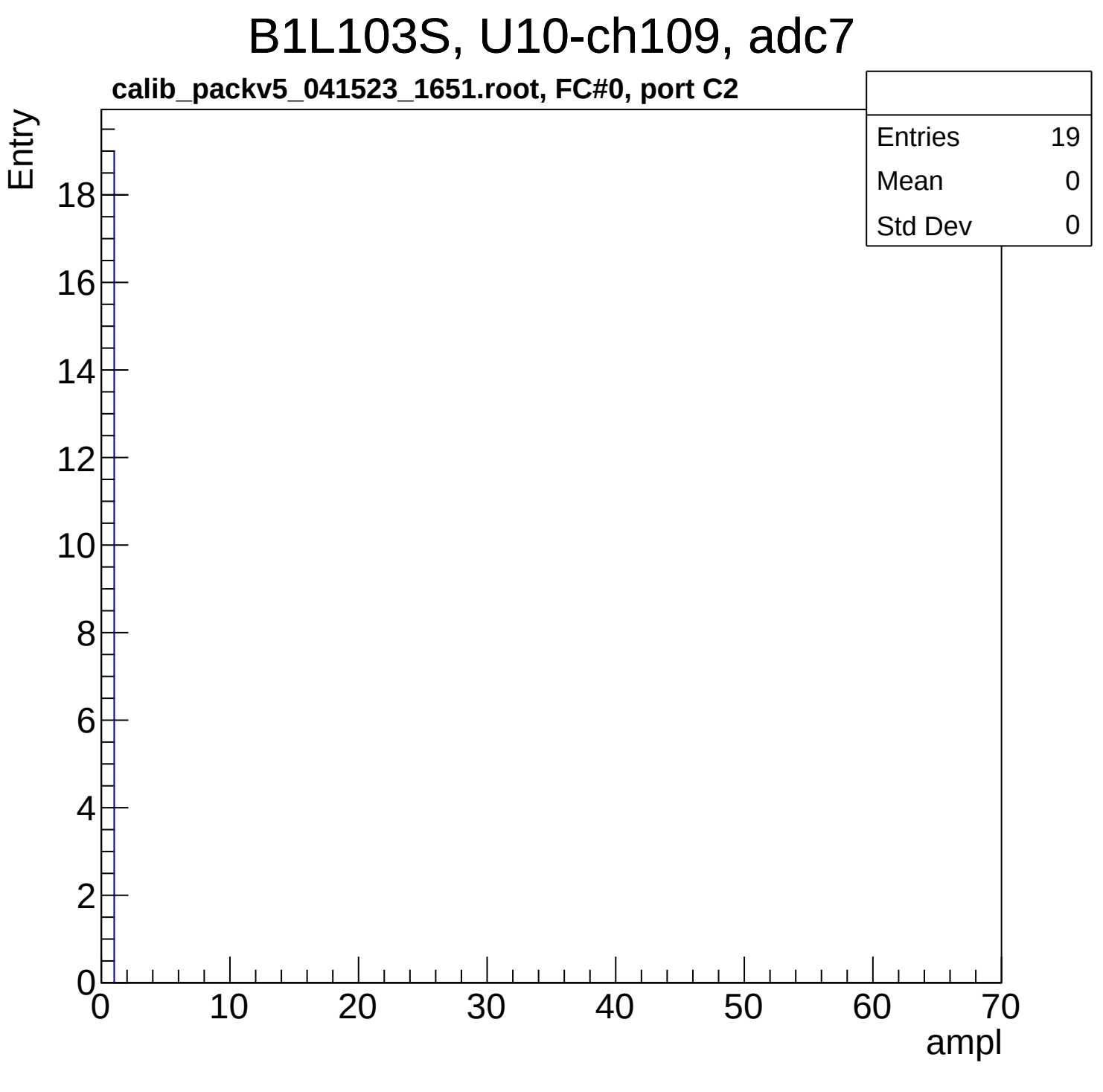
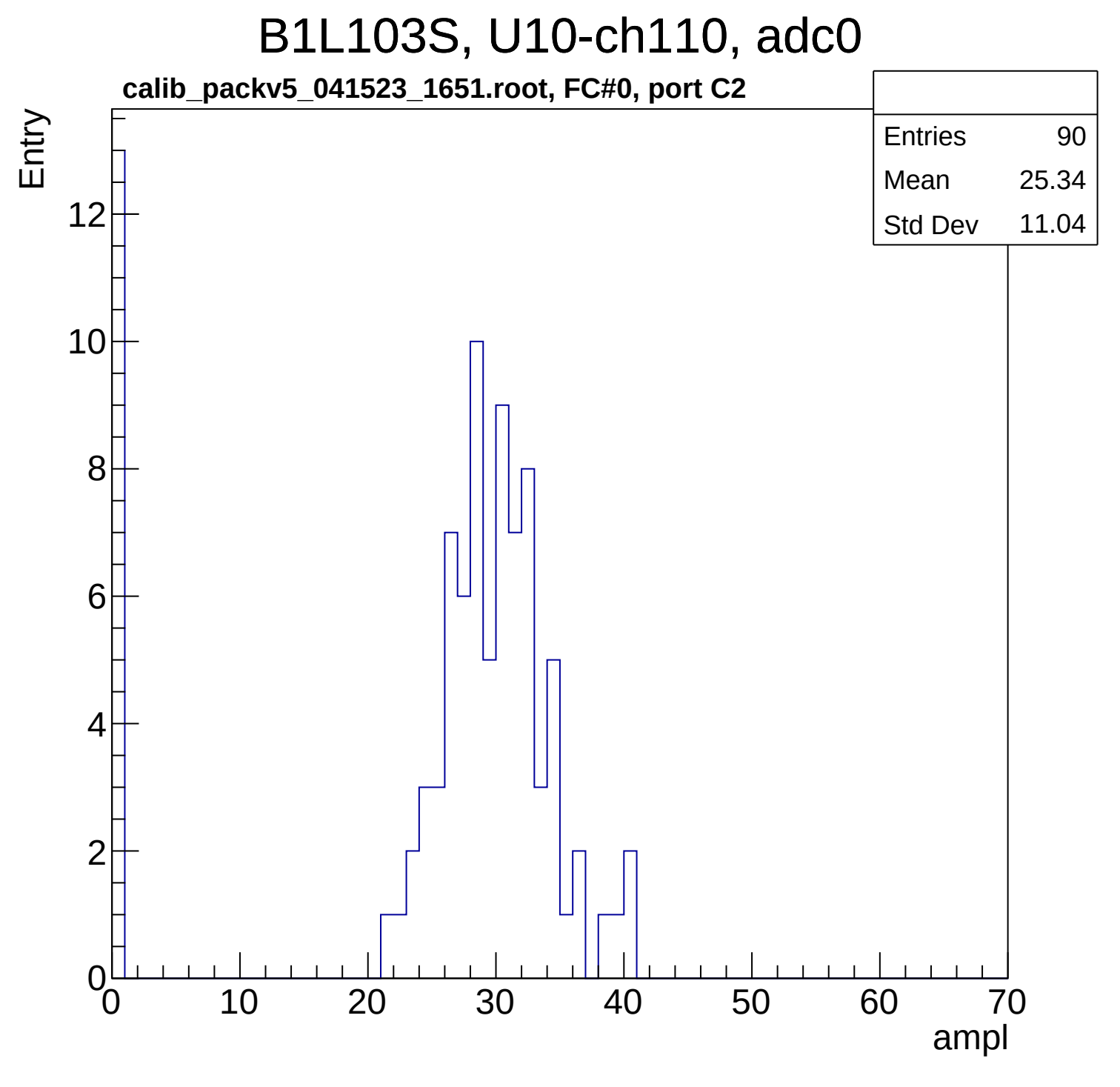
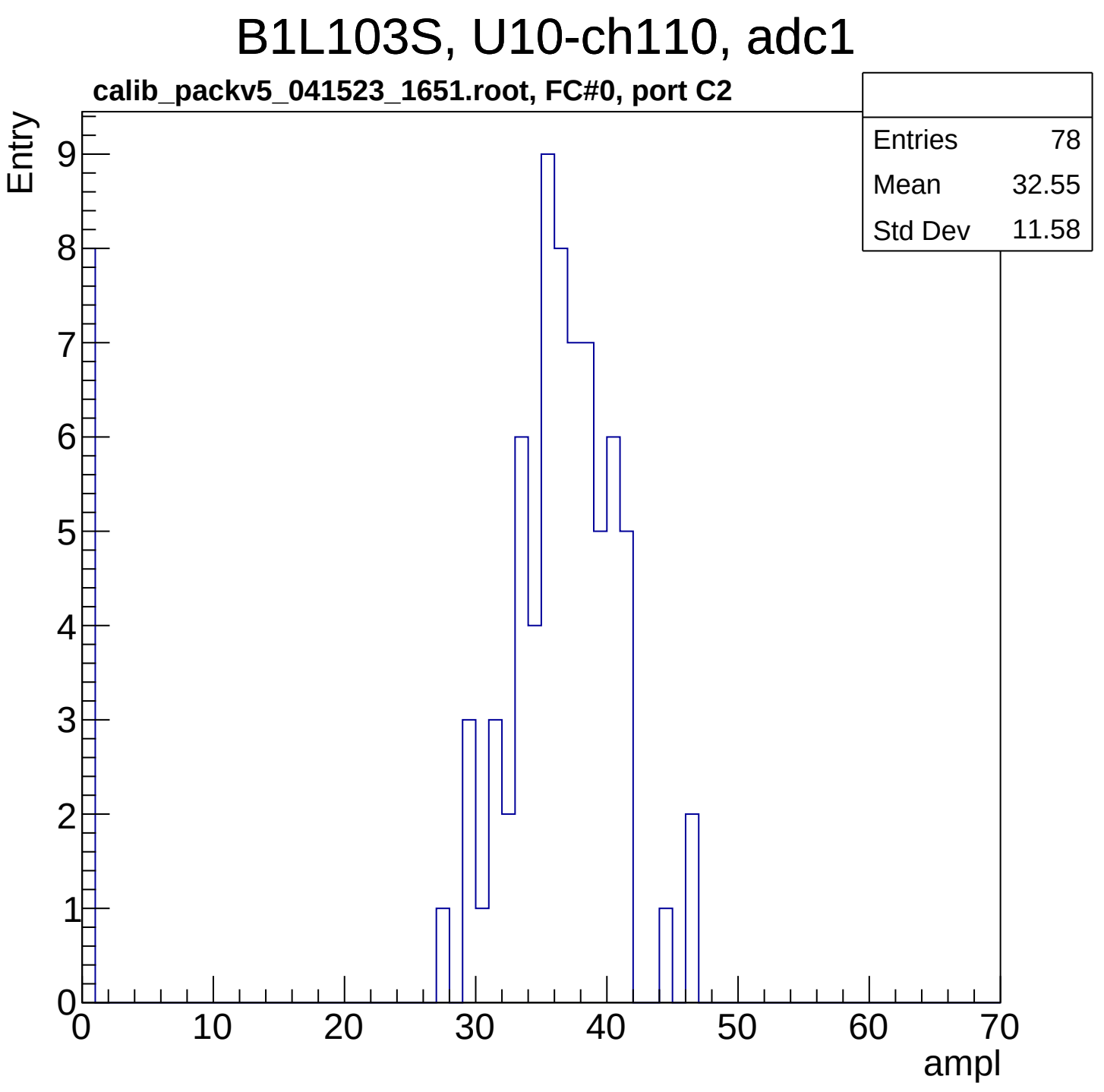
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U10-ch109, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 25
Mean 60.64
Std Dev 2.189
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U10-ch109, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 2
Mean 63
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U10-ch109, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch110, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 90
Mean 25.34
Std Dev 11.04
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch110, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 32.55
Std Dev 11.58
Entry
ampl
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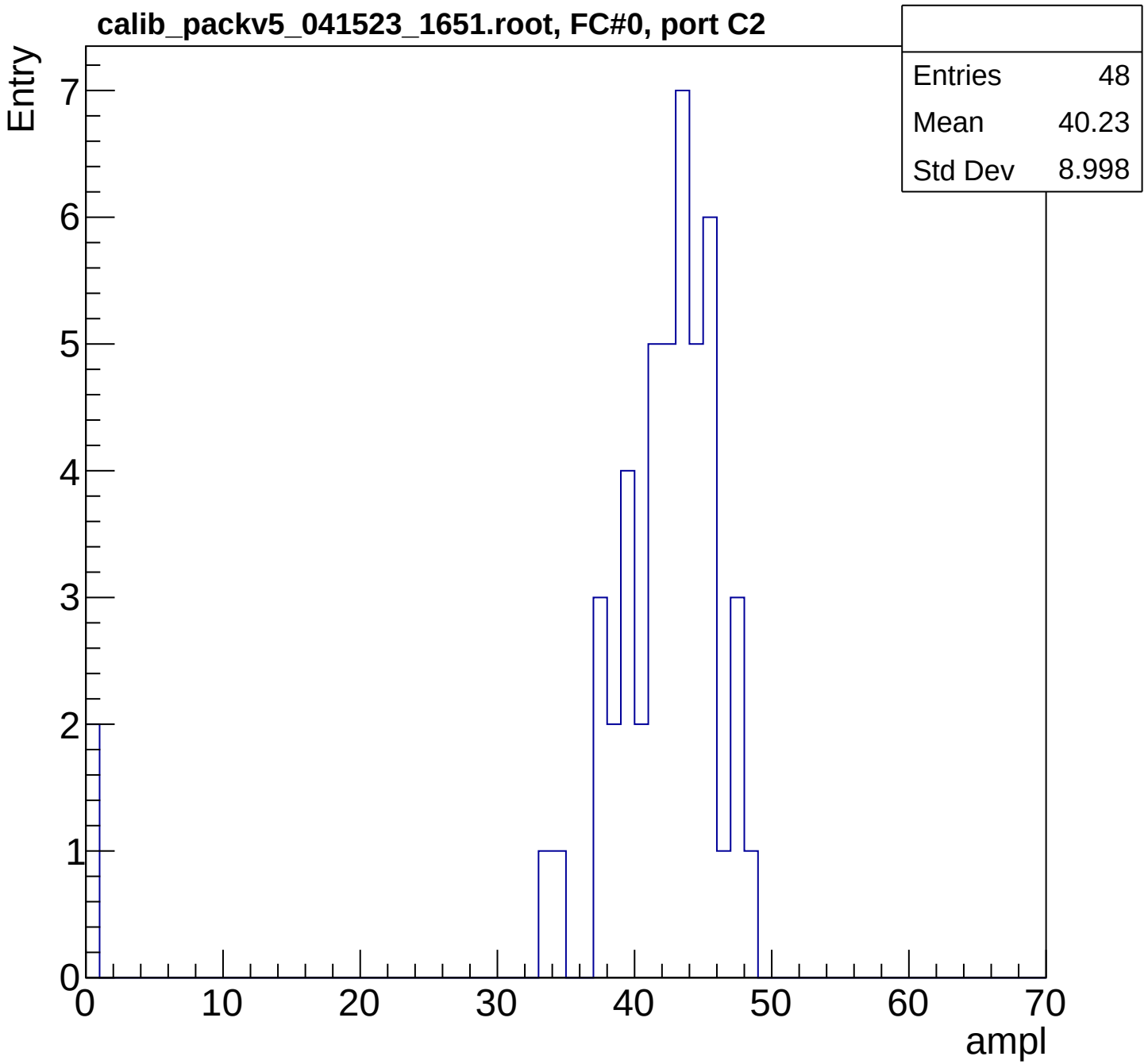
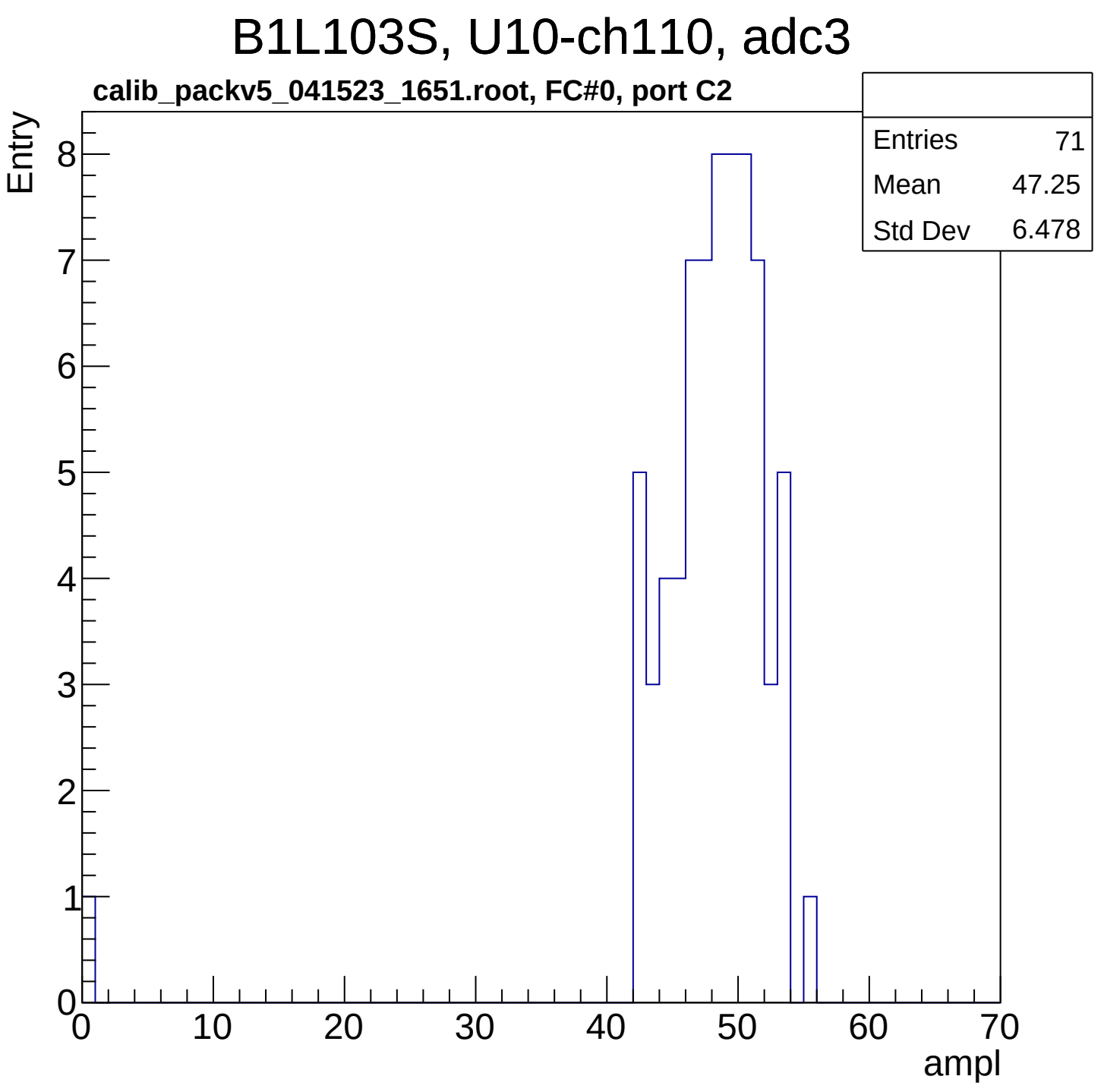
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U10-ch110, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 40.23
Std Dev 8.998
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U10-ch110, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 47.25
Std Dev 6.478
Entry
ampl
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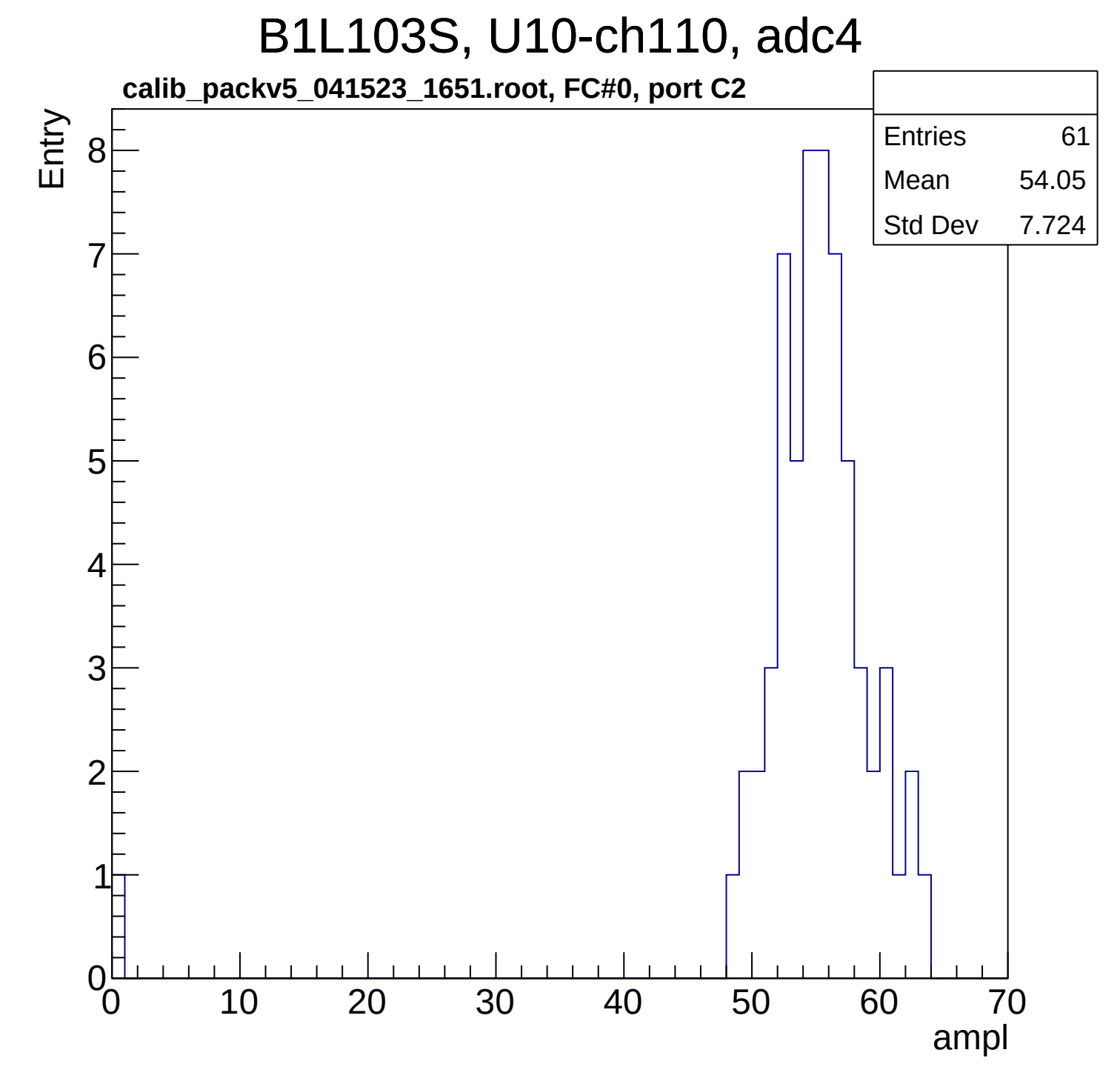
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U10-ch110, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 54.05
Std Dev 7.724
Entry
ampl
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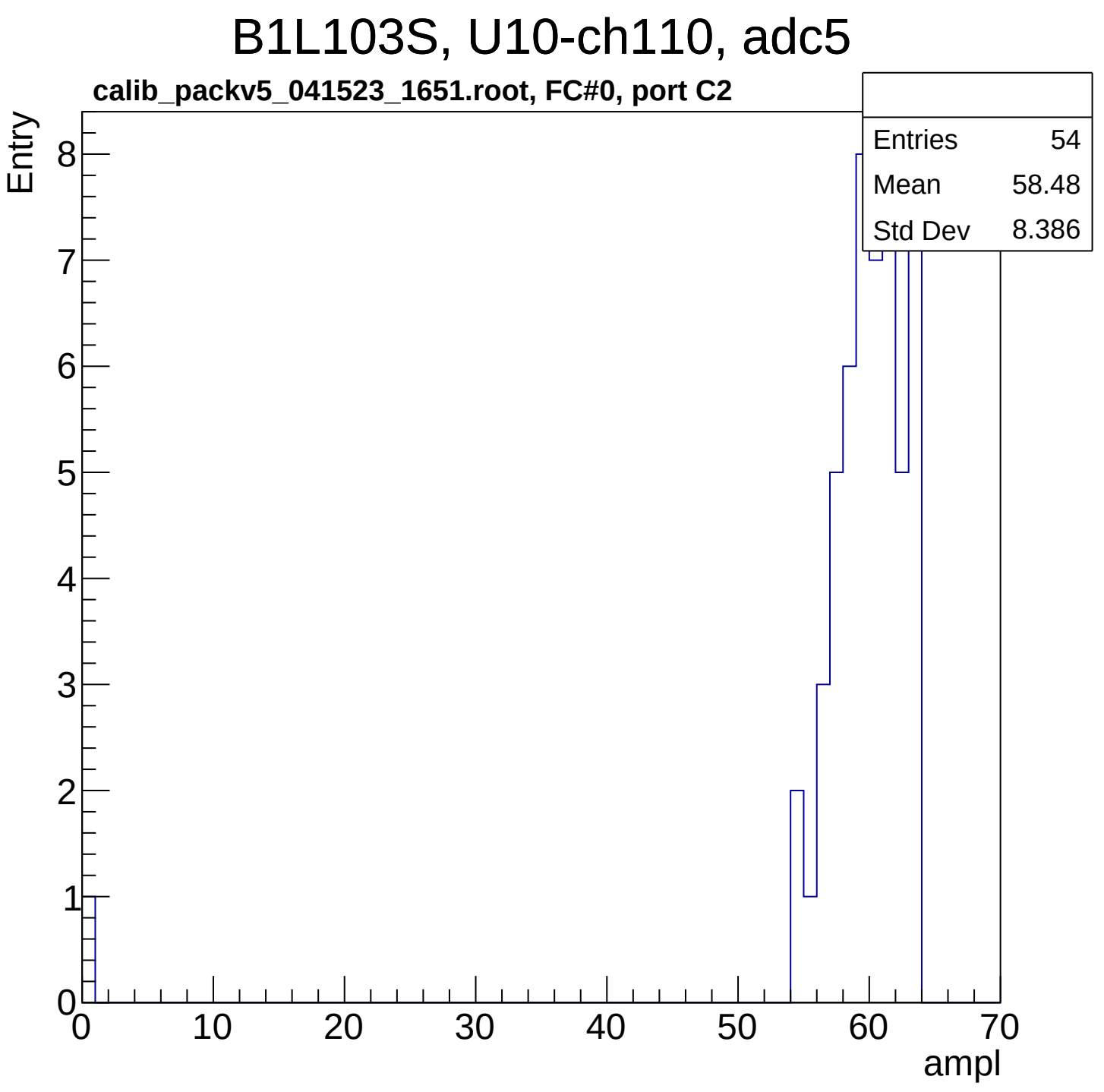
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U10-ch110, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 58.48
Std Dev 8.386
Entry
ampl
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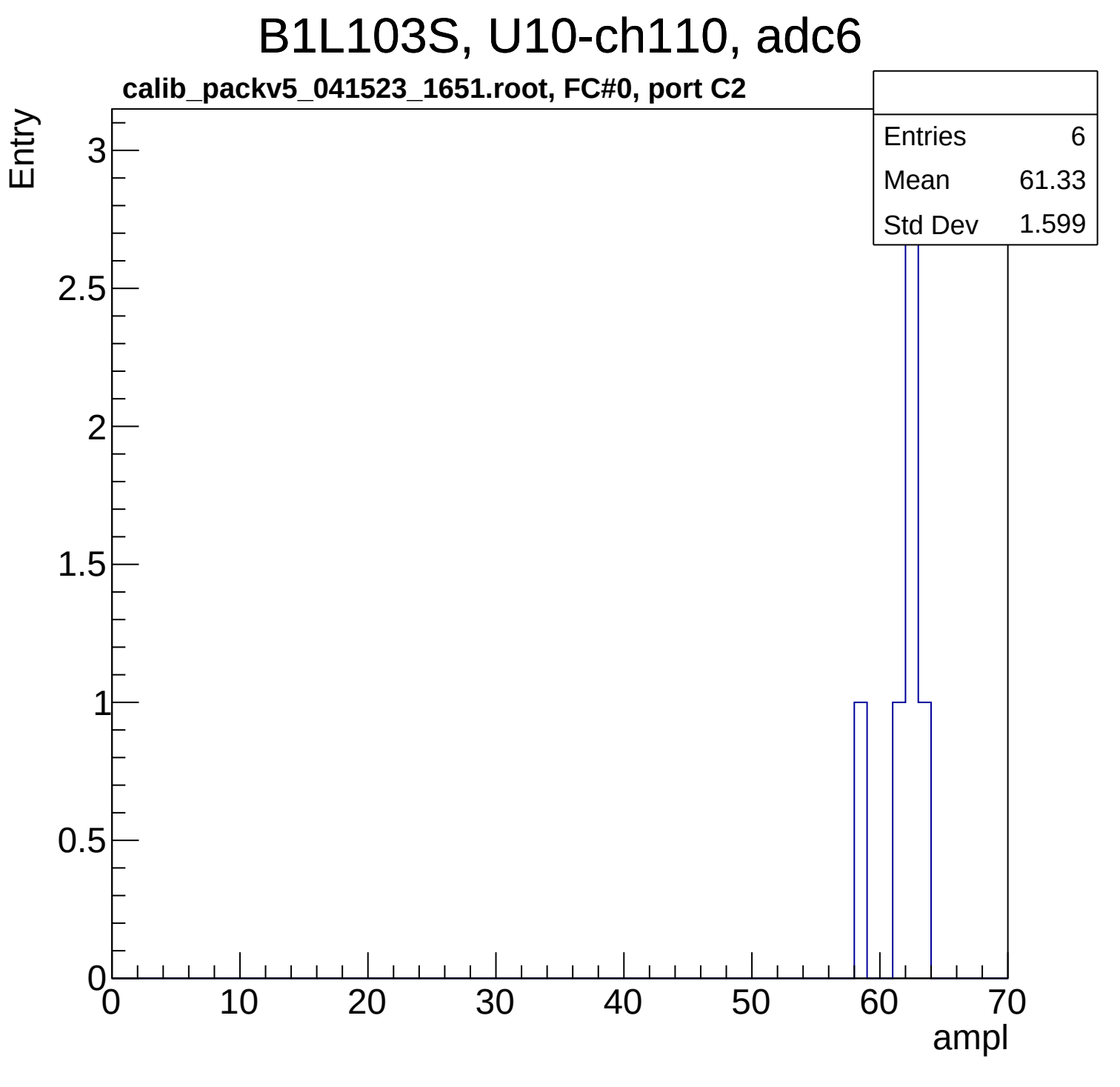
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U10-ch110, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 61.33
Std Dev 1.599
Entry
ampl
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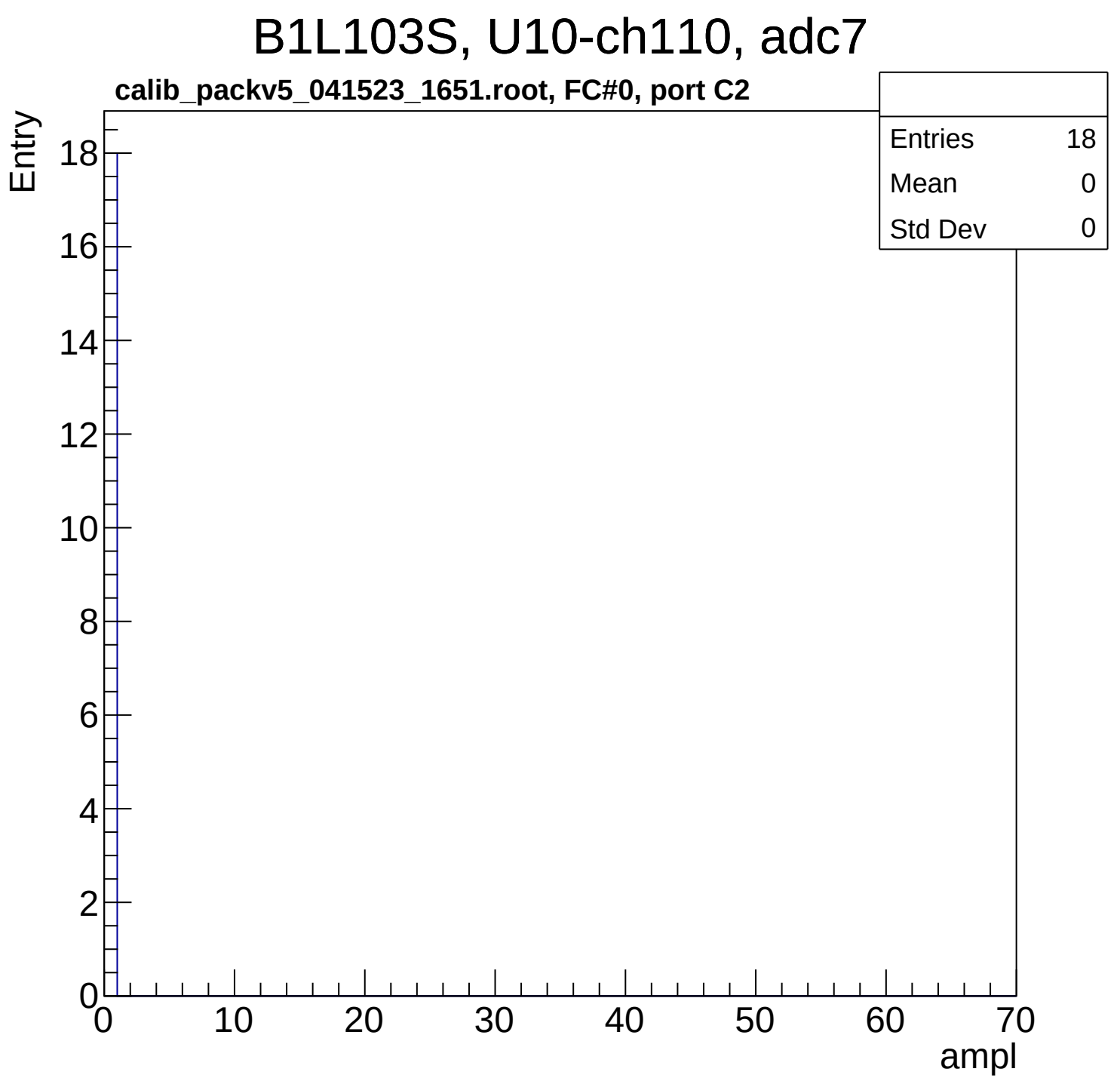
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U10-ch110, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
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2
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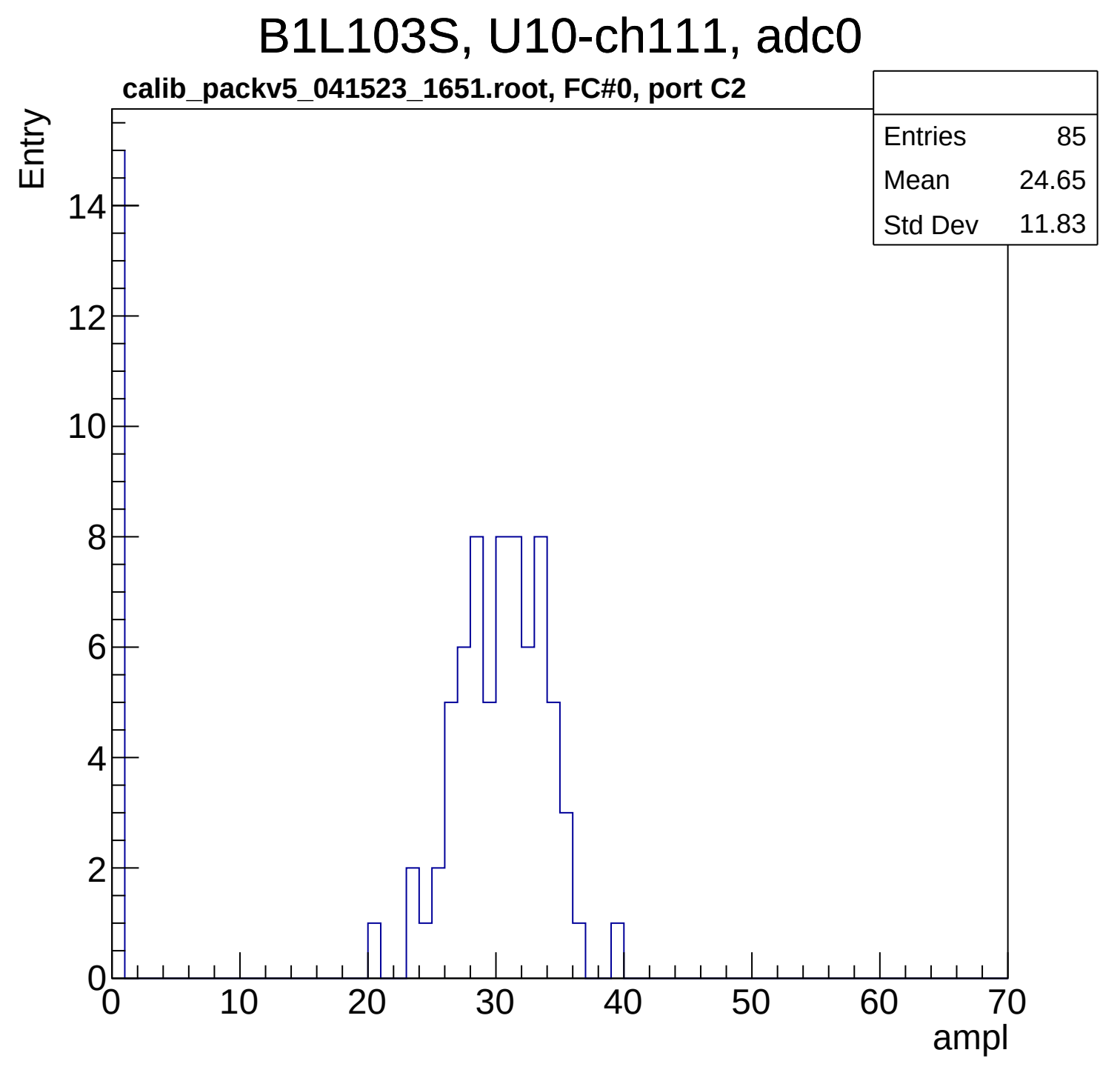
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch111, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 24.65
Std Dev 11.83
Entry
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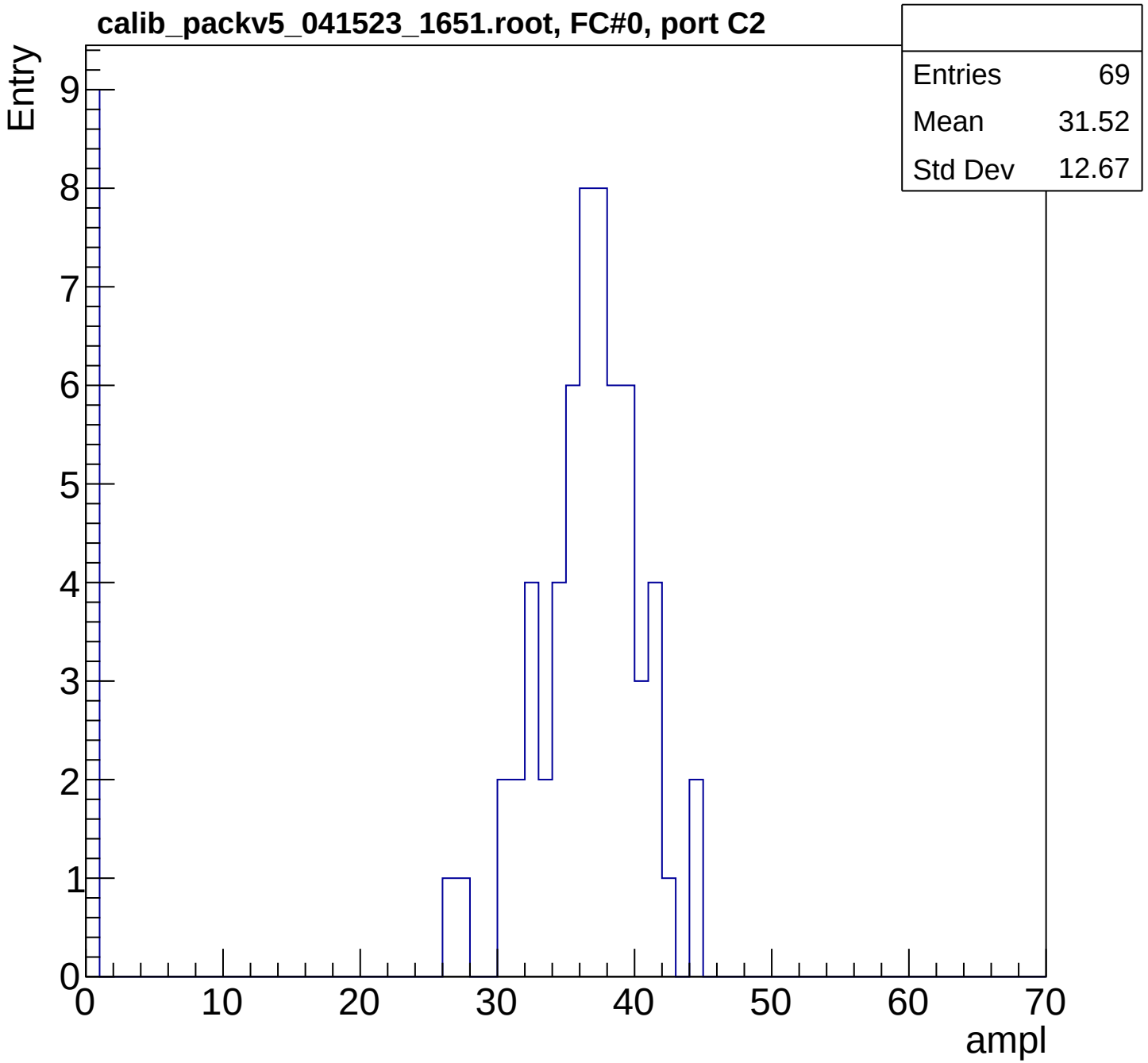
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch111, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 31.52
Std Dev 12.67
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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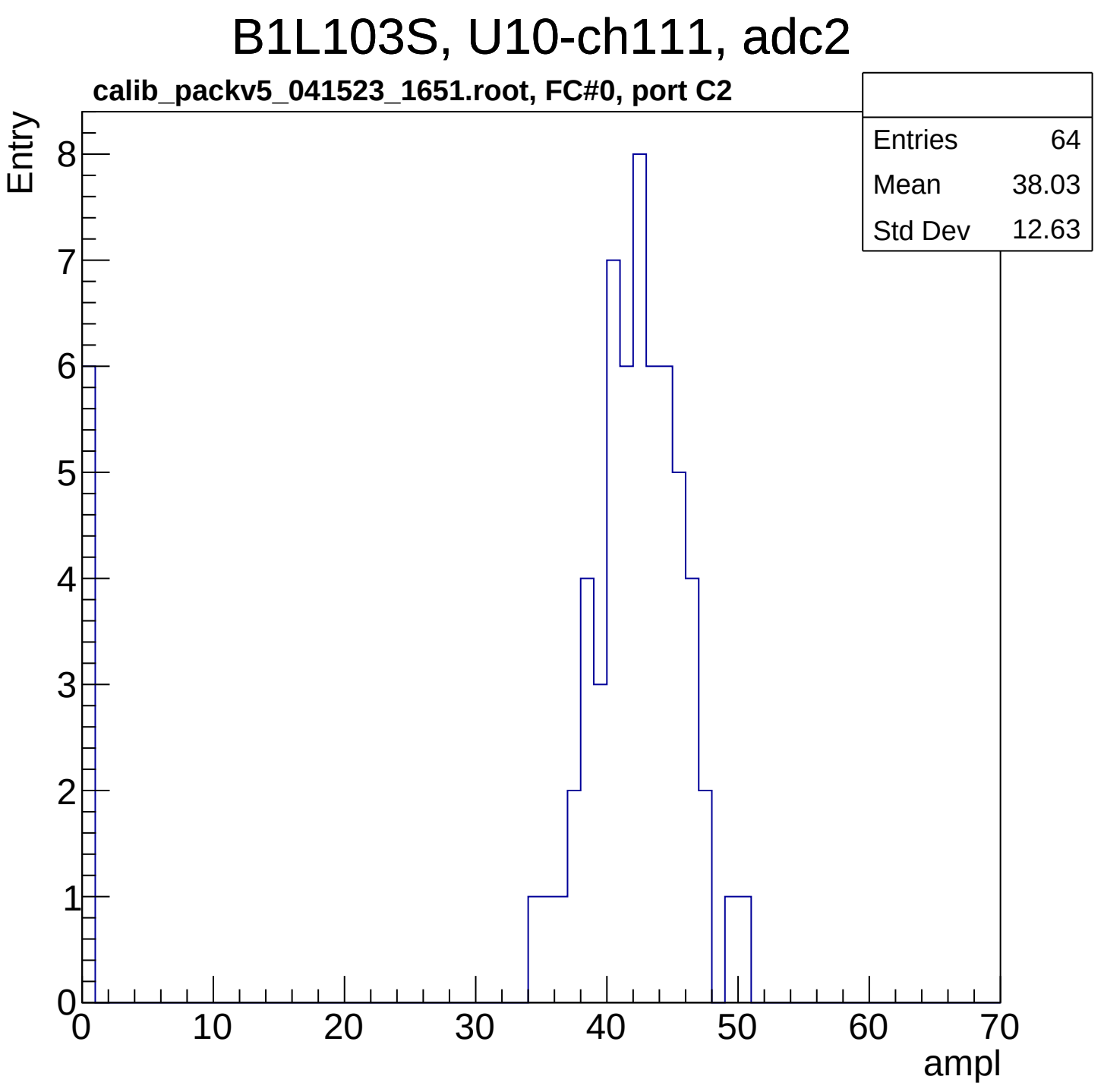
40
50
60
70


B1L103S, U10-ch111, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 38.03
Std Dev 12.63
Entry
ampl
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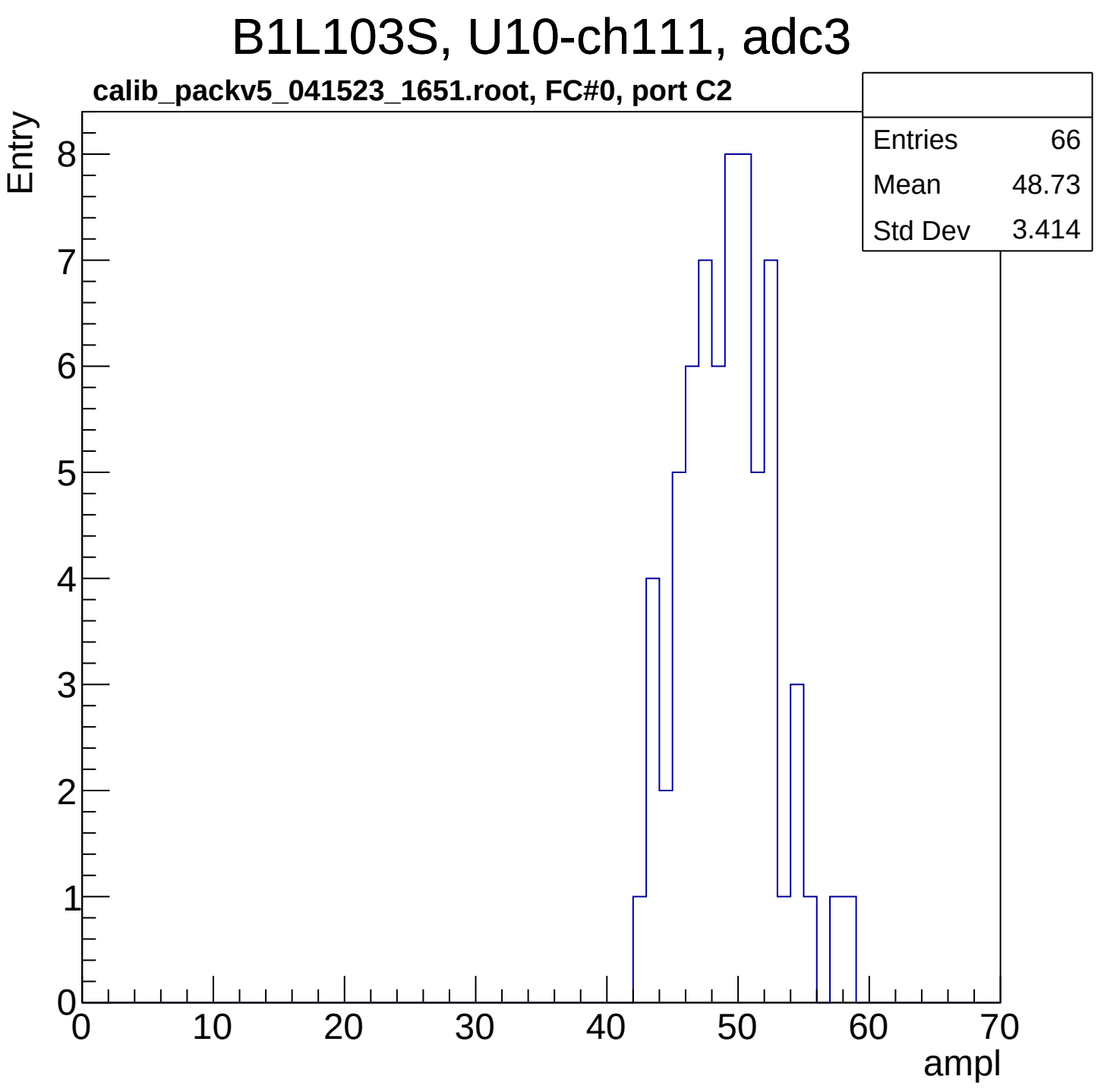
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U10-ch111, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 48.73
Std Dev 3.414
Entry
ampl
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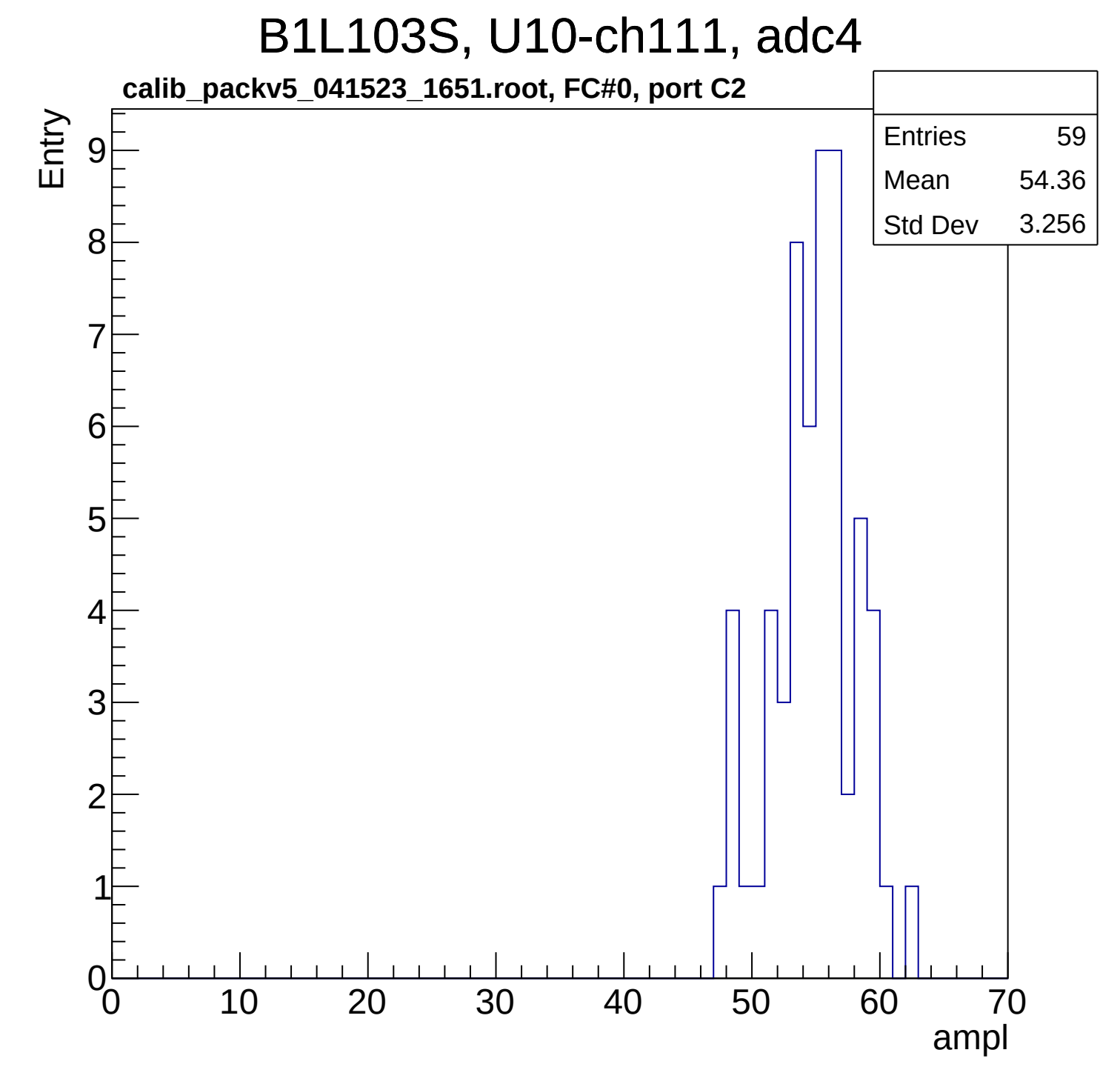
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U10-ch111, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 54.36
Std Dev 3.256
Entry
ampl
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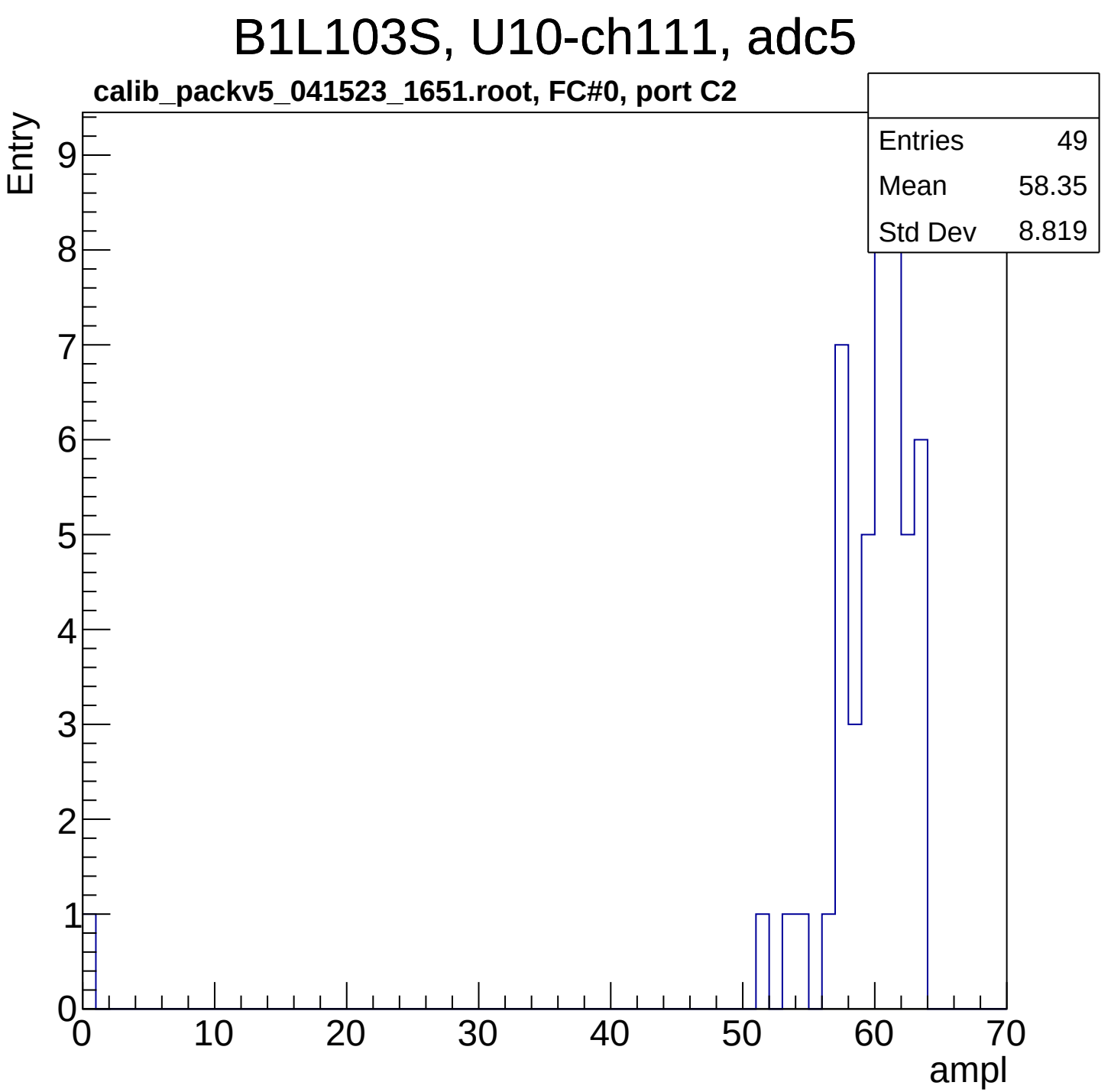
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U10-ch111, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 58.35
Std Dev 8.819
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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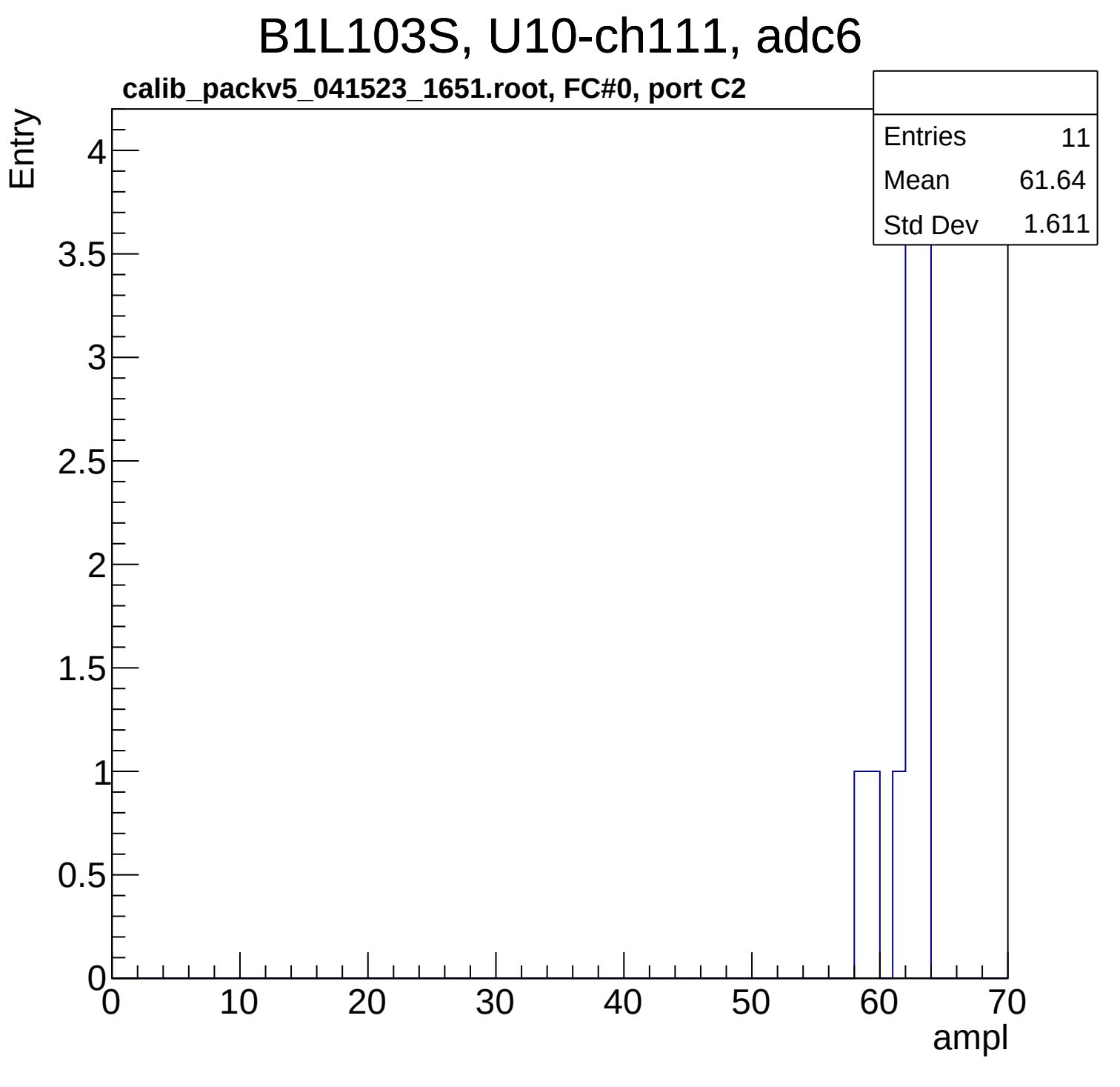
60
70


B1L103S, U10-ch111, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 61.64
Std Dev 1.611
Entry
ampl
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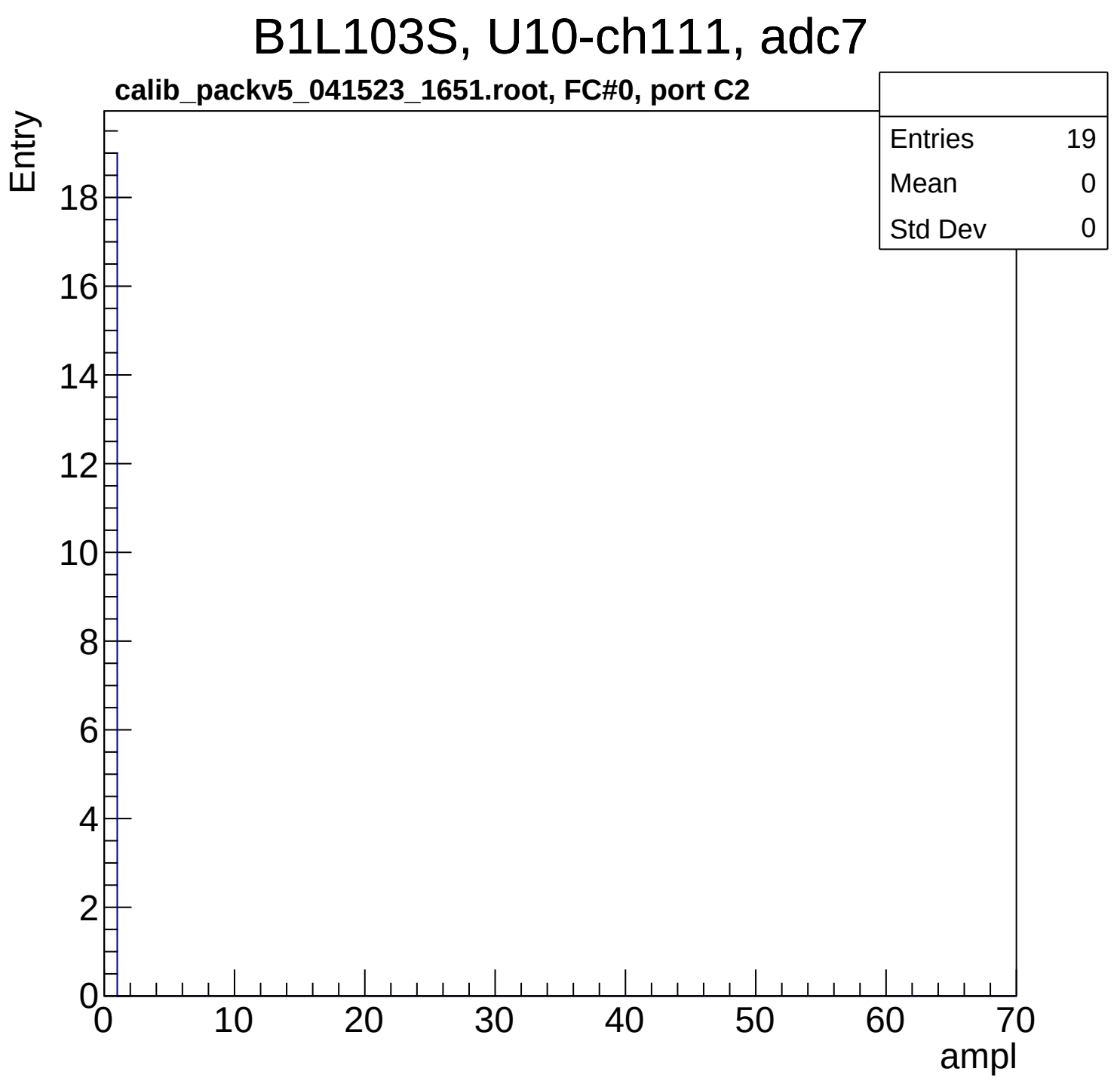
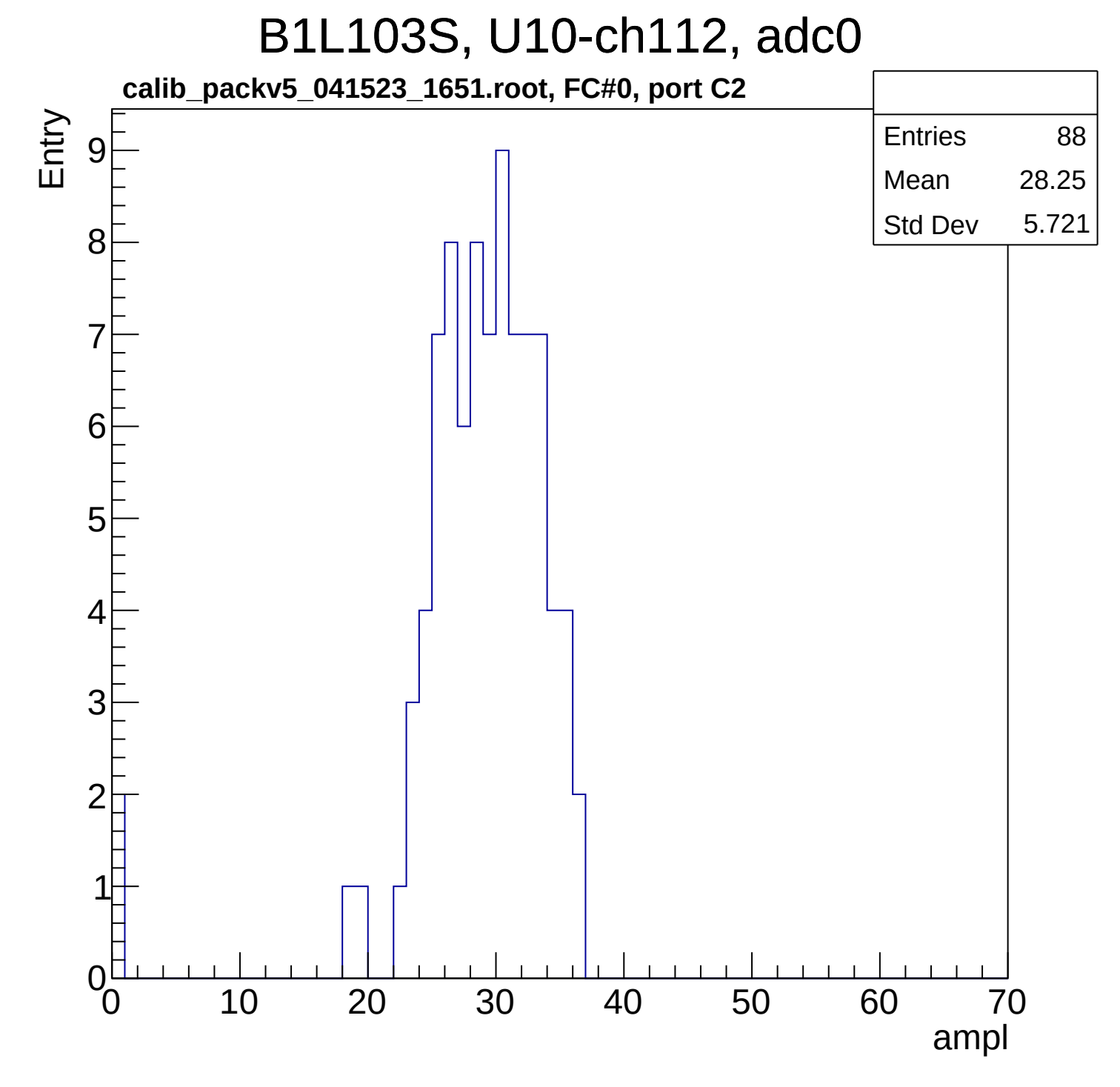
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U10-ch111, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch112, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 88
Mean 28.25
Std Dev 5.721
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
50
60
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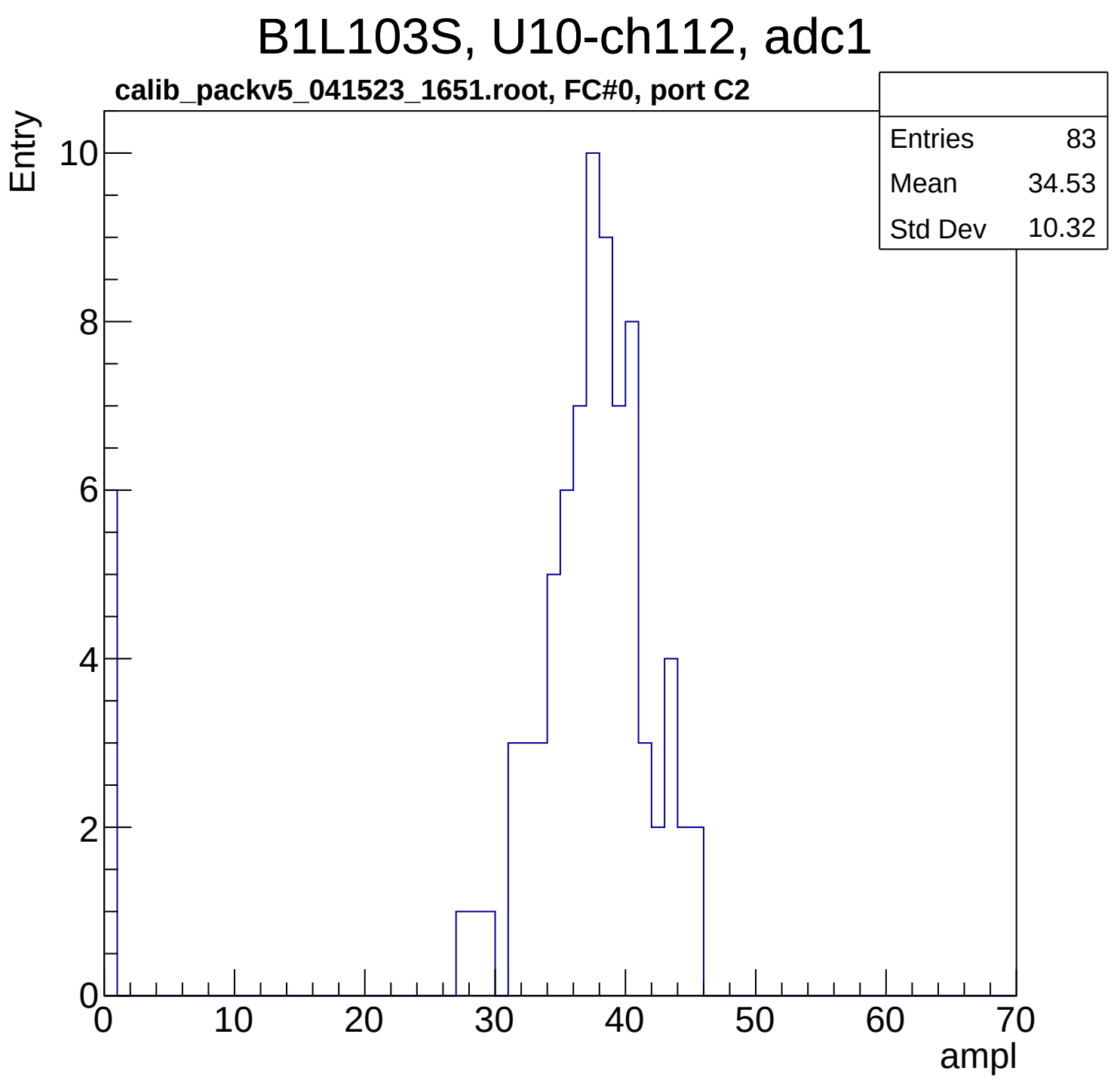
B1L103S, U10-ch112, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 34.53
Std Dev 10.32
Entry
ampl
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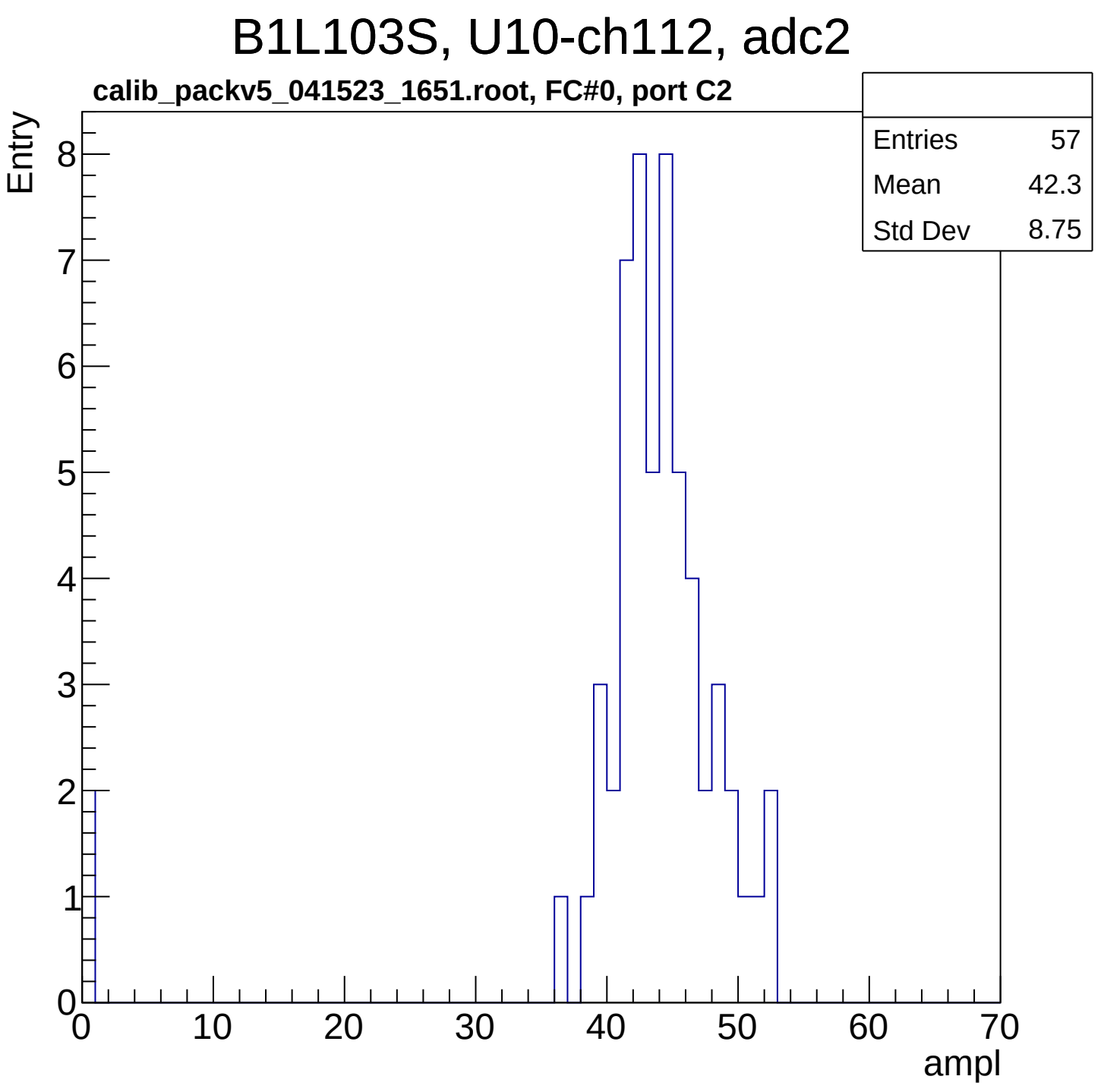
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U10-ch112, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 42.3
Std Dev 8.75
Entry
ampl
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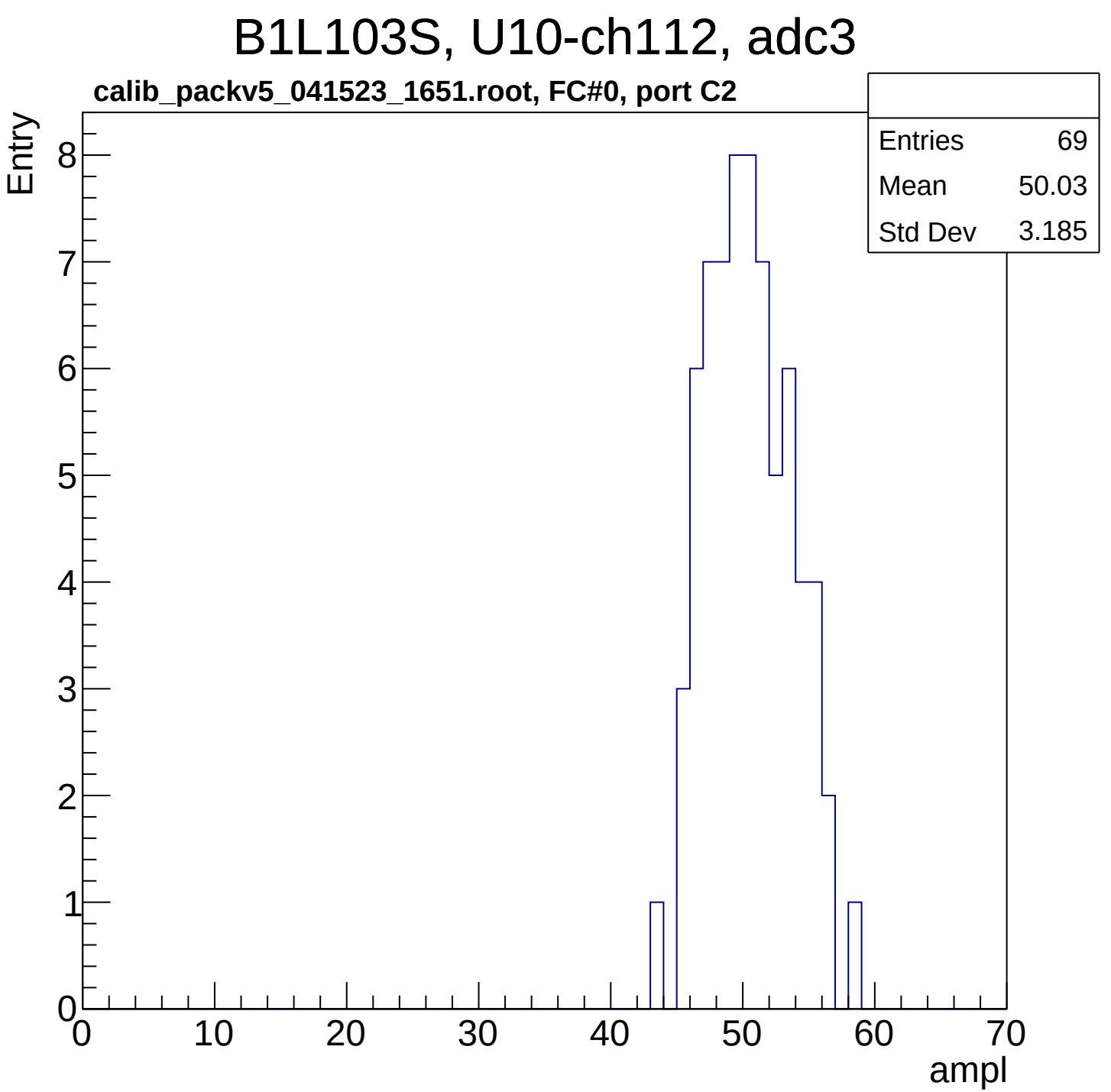
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U10-ch112, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 50.03
Std Dev 3.185
Entry
ampl
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1
2
3
4
5
6
7
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0
10
20
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40
50
60
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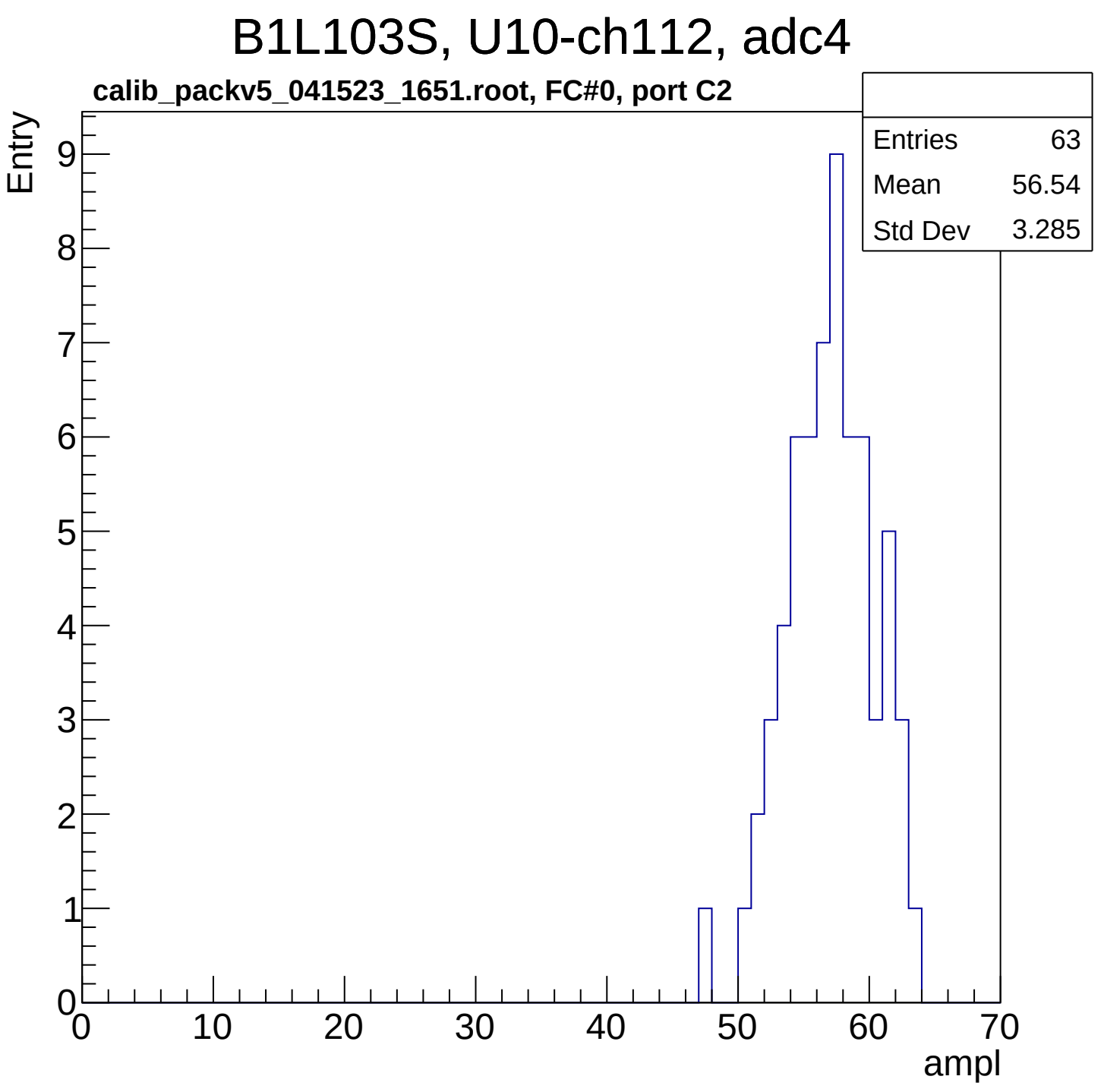
B1L103S, U10-ch112, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 56.54
Std Dev 3.285
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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40
50
60
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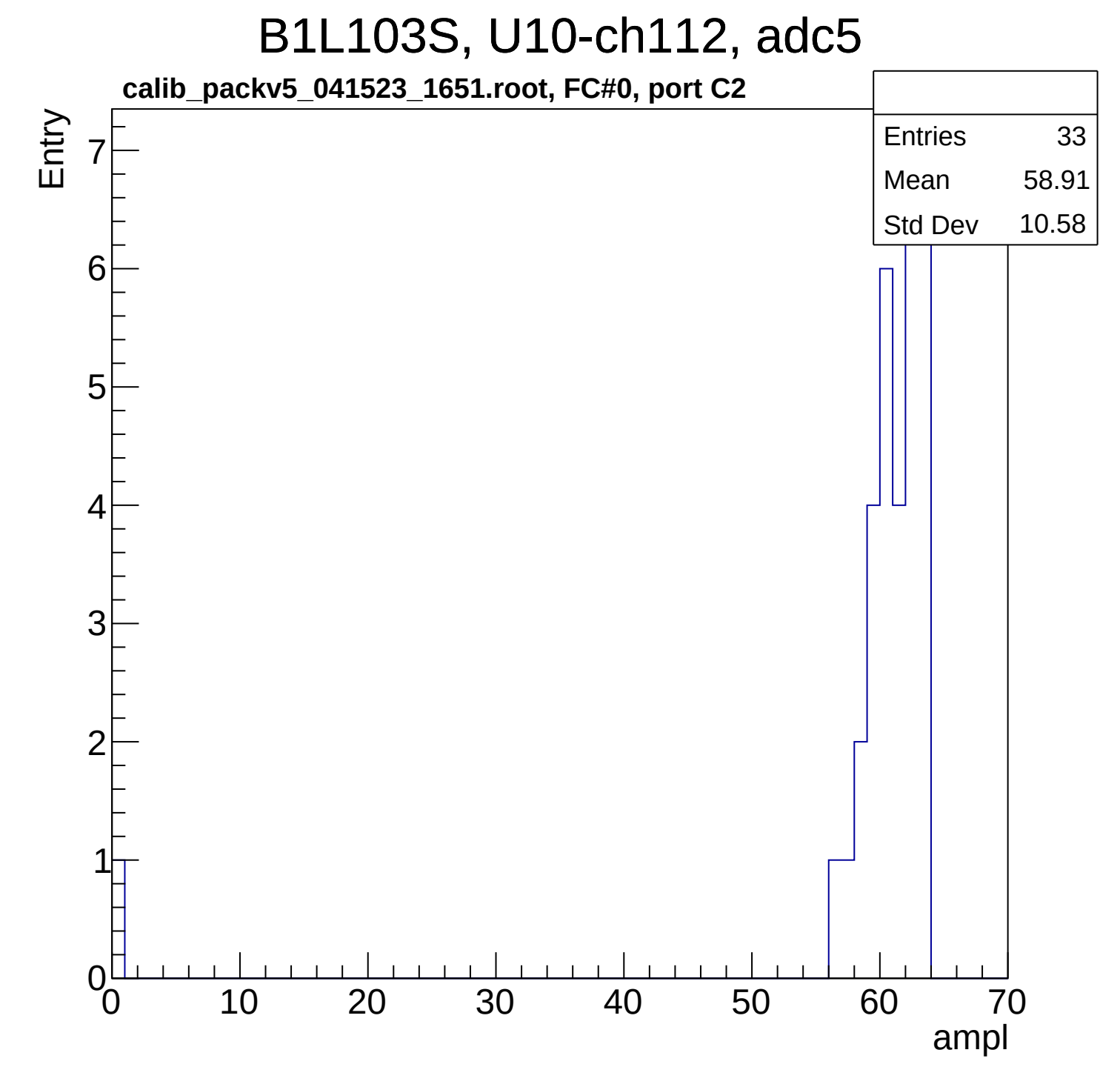
B1L103S, U10-ch112, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 33
Mean 58.91
Std Dev 10.58
Entry
ampl
0
1
2
3
4
5
6
7
0
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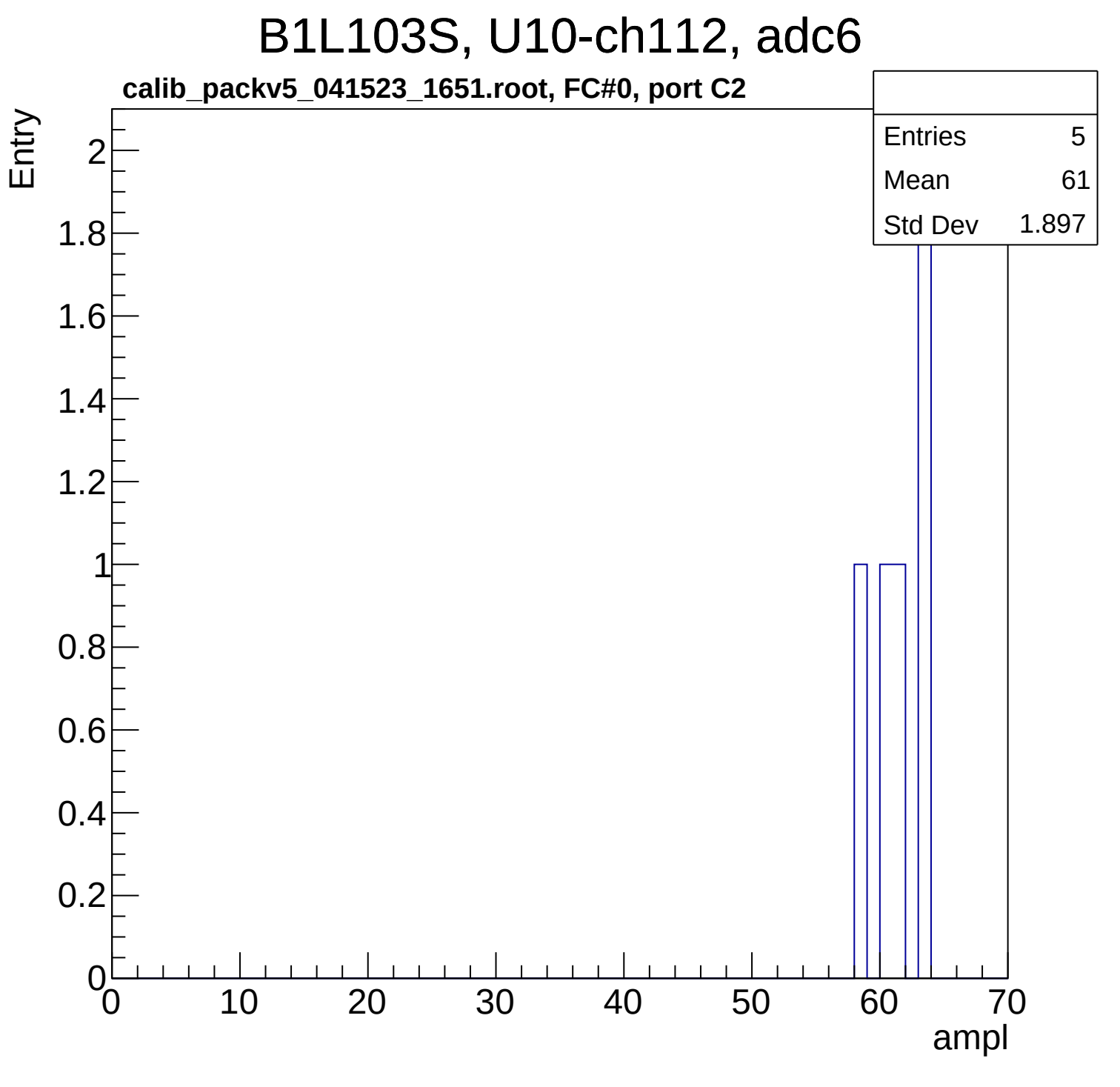
40
50
60
70


B1L103S, U10-ch112, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 5
Mean 61
Std Dev 1.897
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
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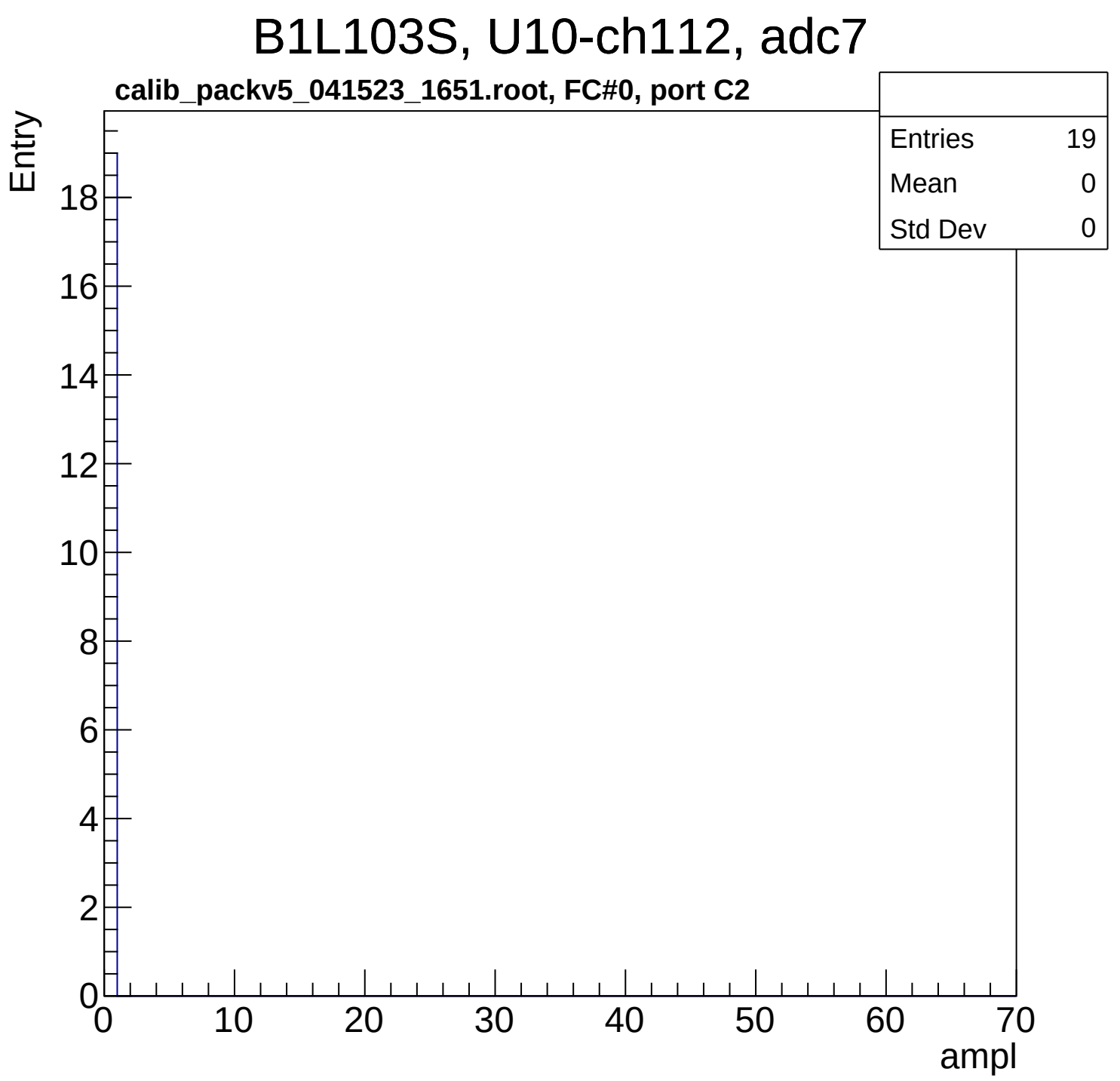
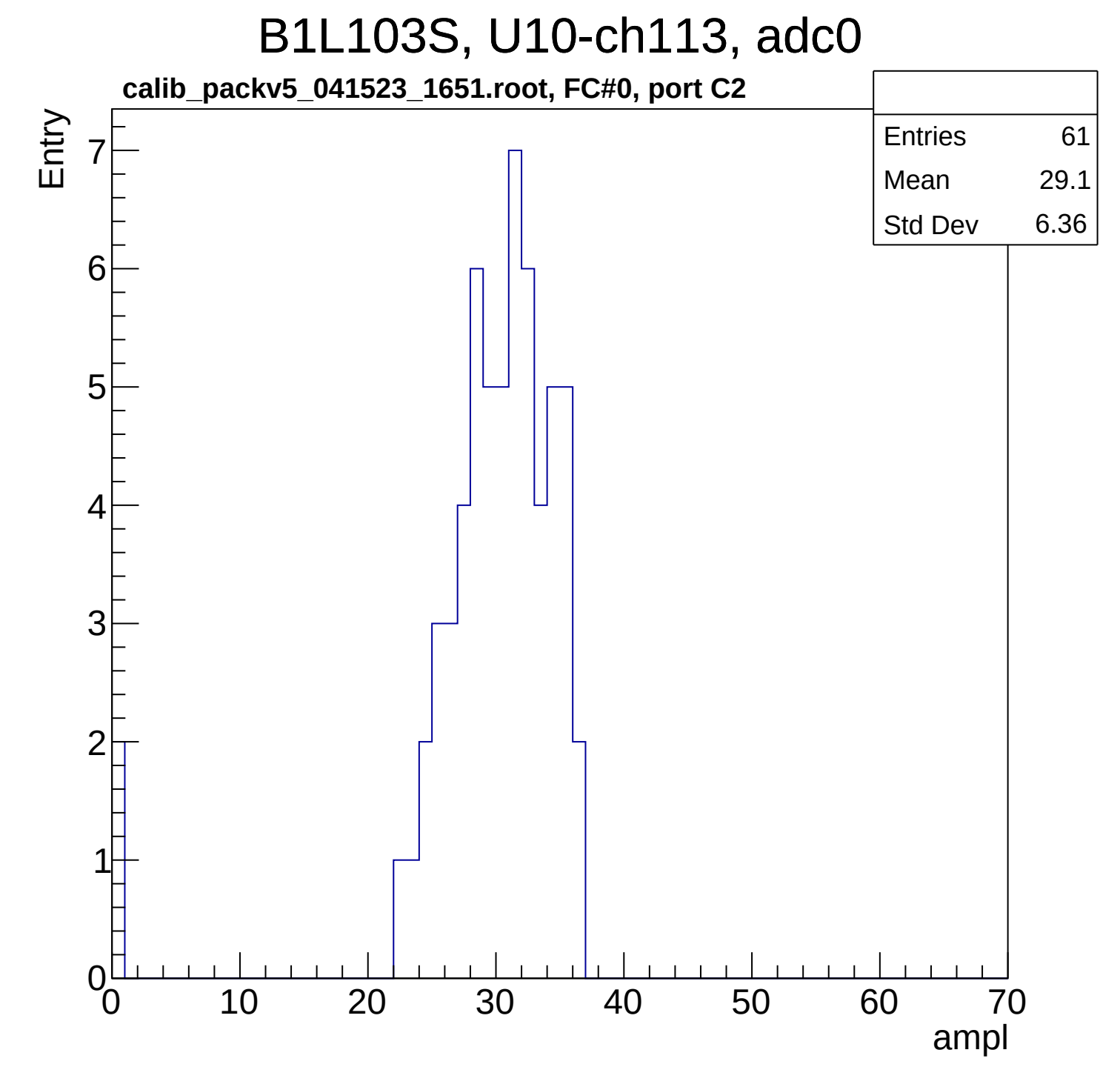
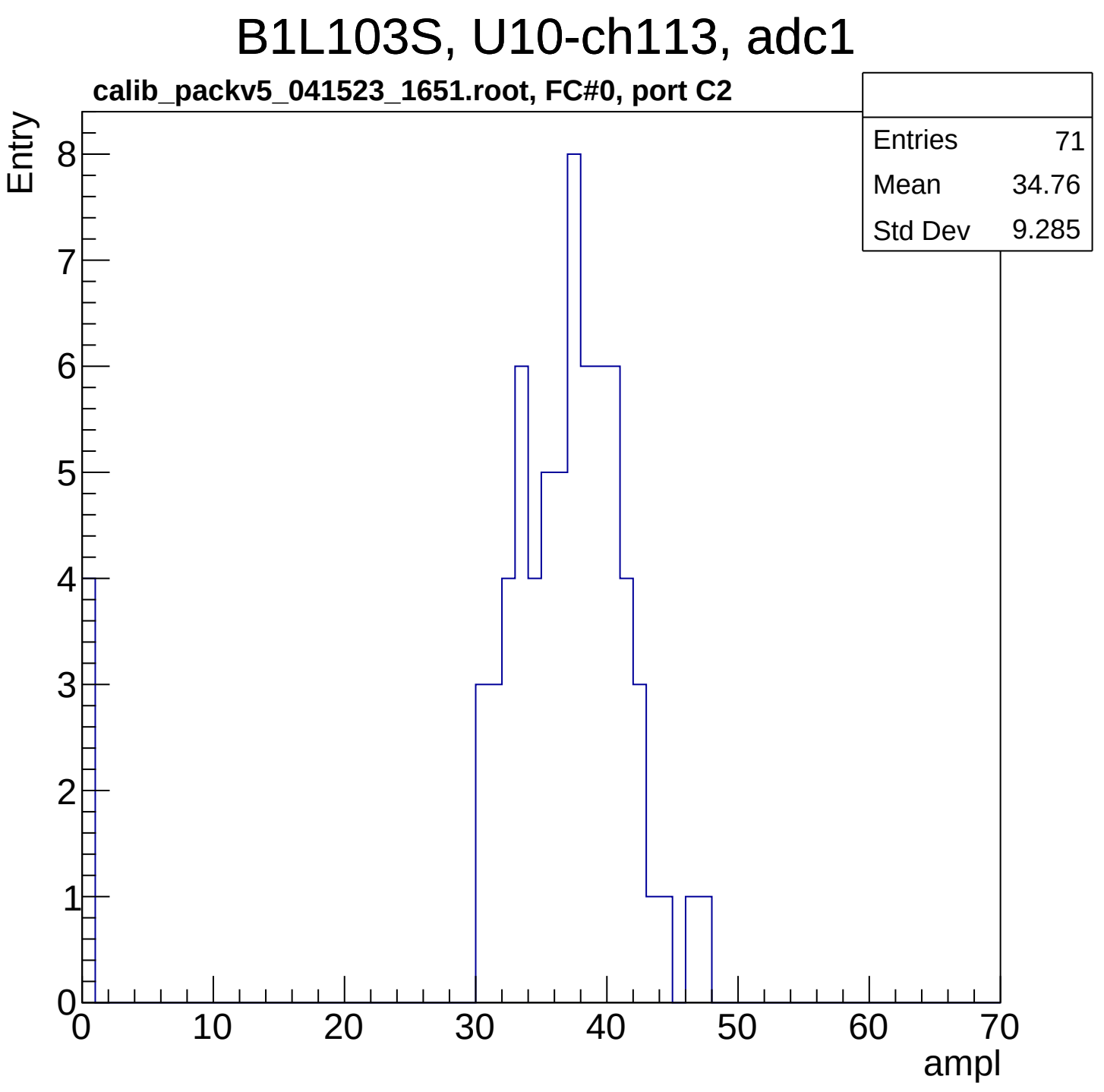
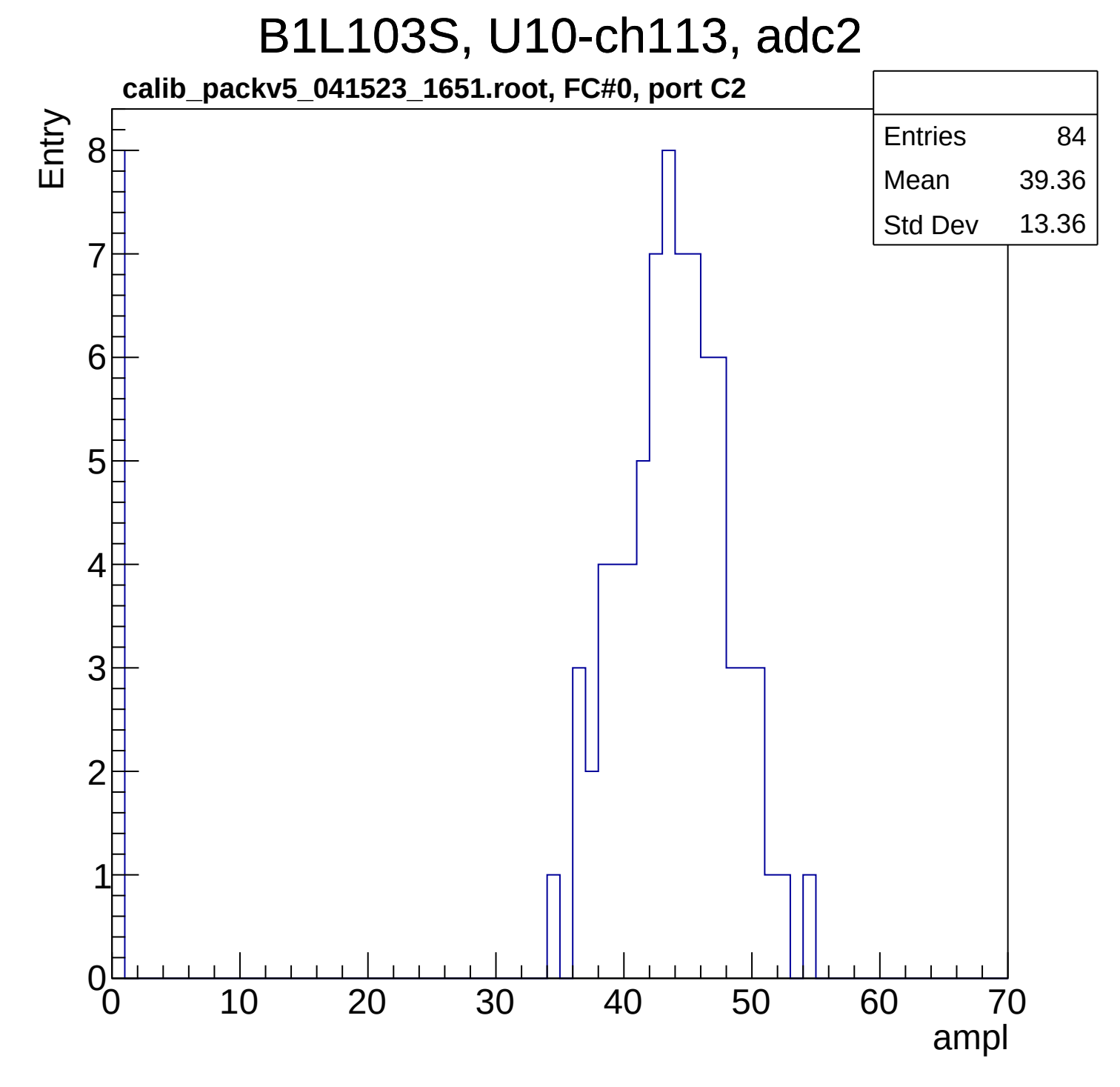
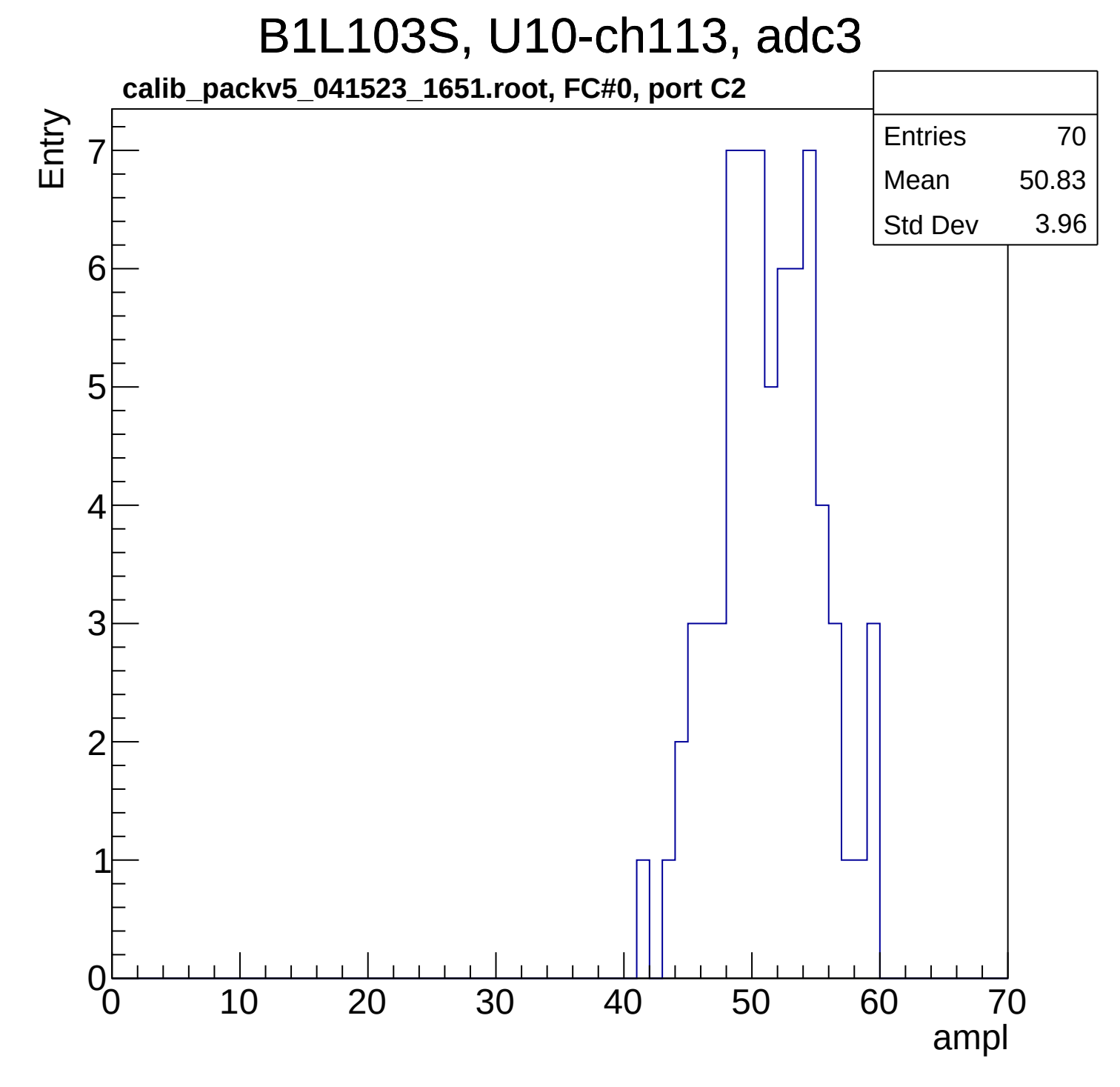
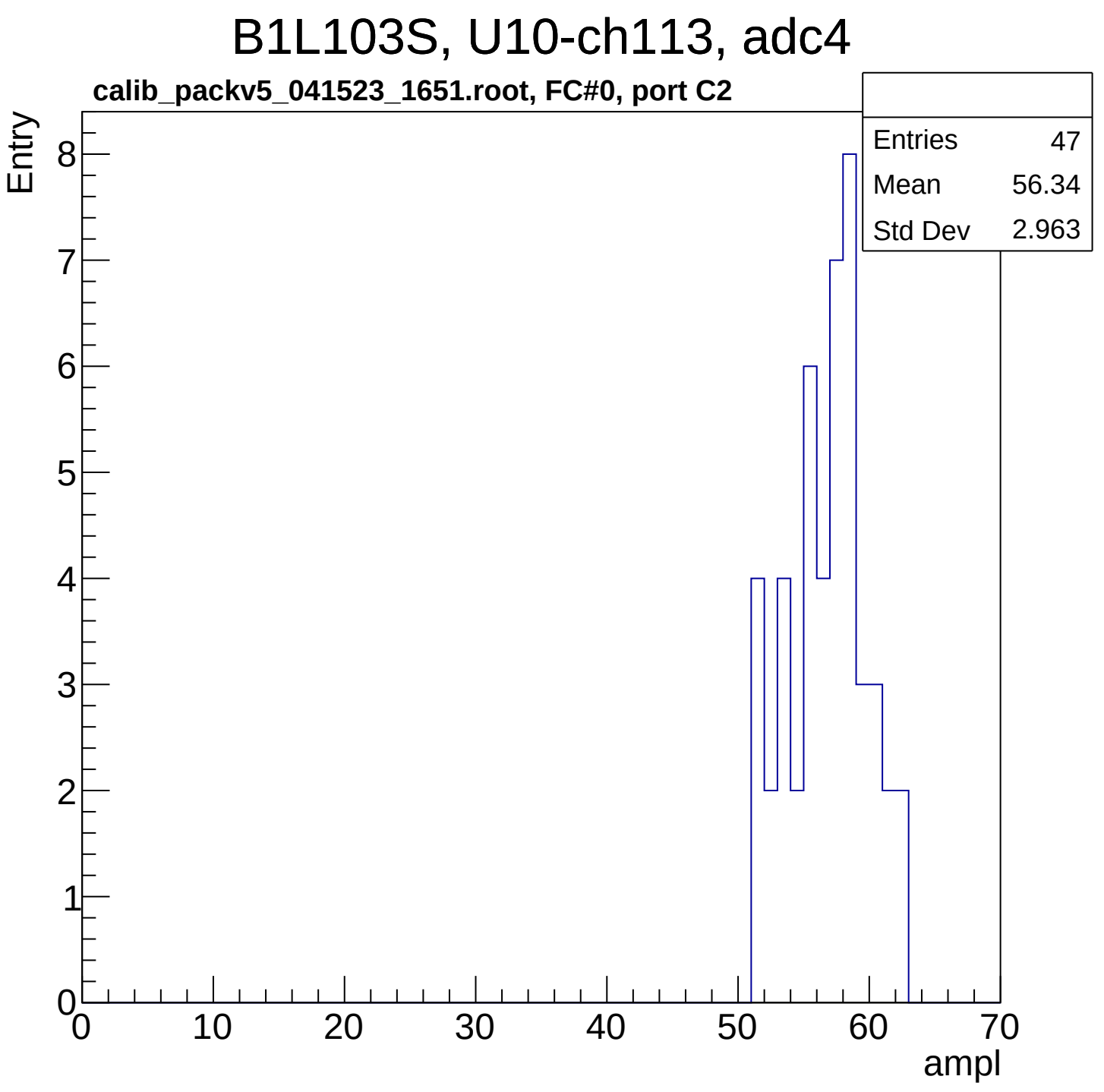

B1L103S, U10-ch112, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

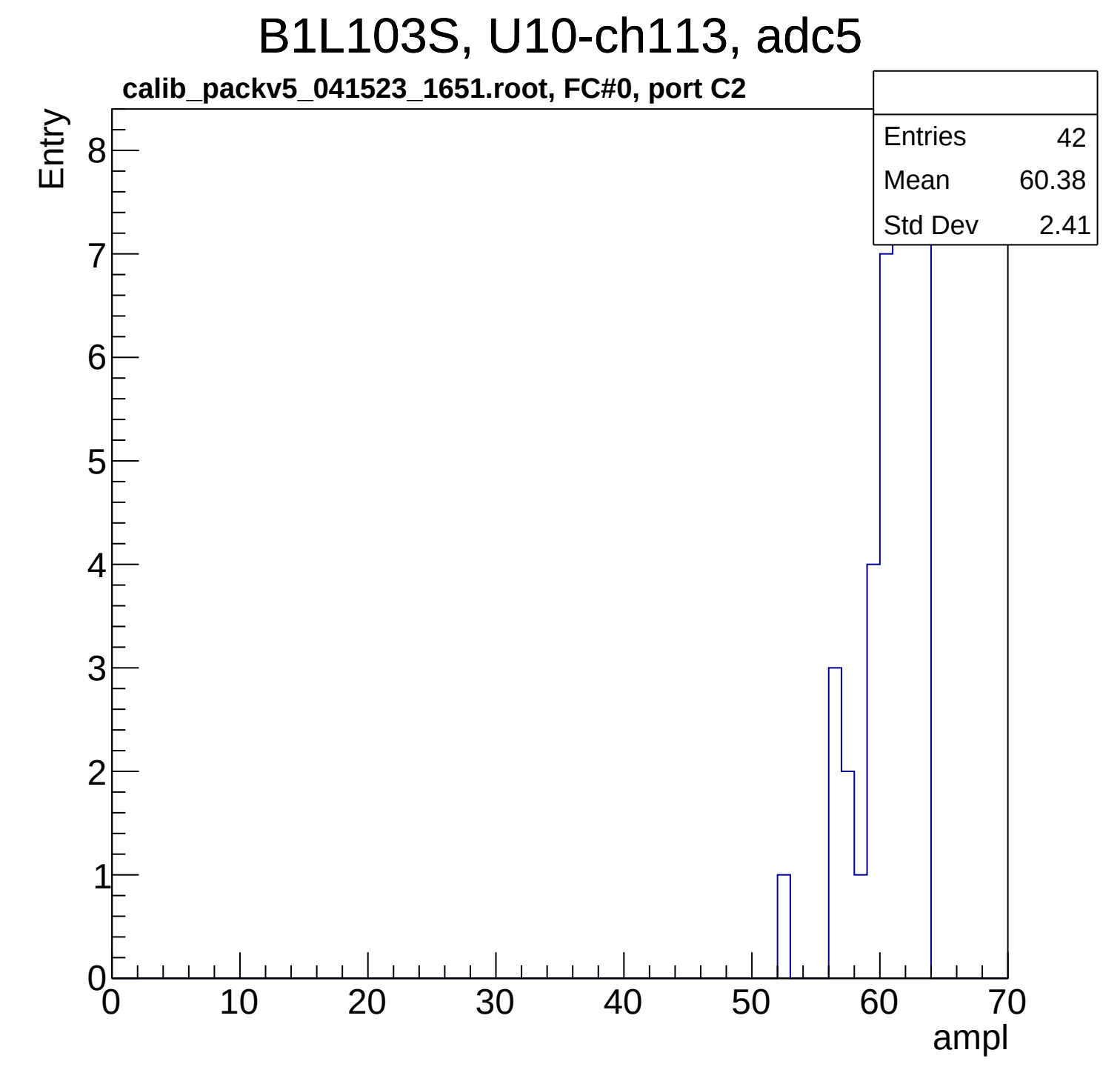

B1L103S, U10-ch113, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 29.1
Std Dev 6.36
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

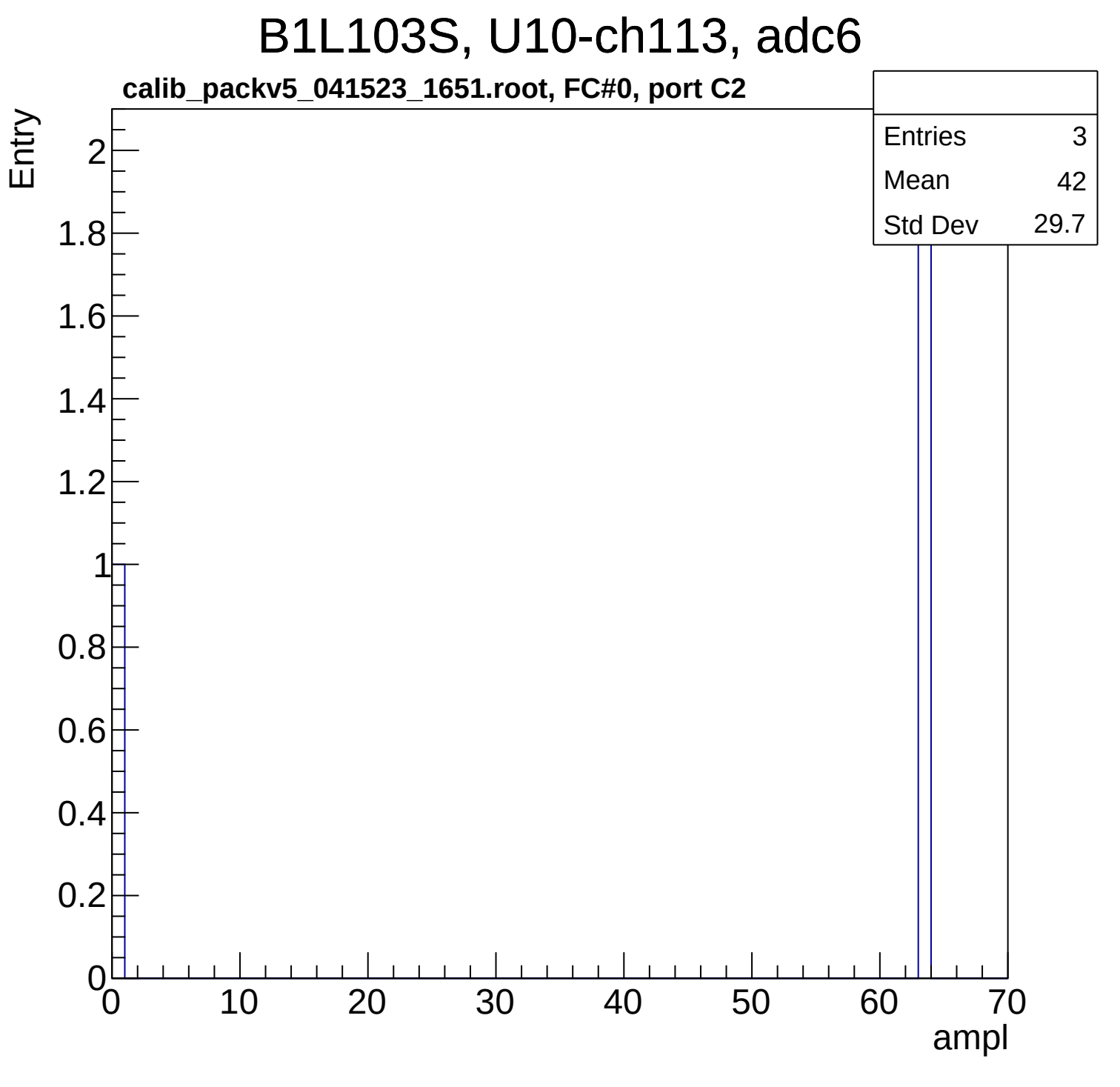

B1L103S, U10-ch113, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 34.76
Std Dev 9.285
Entry
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl

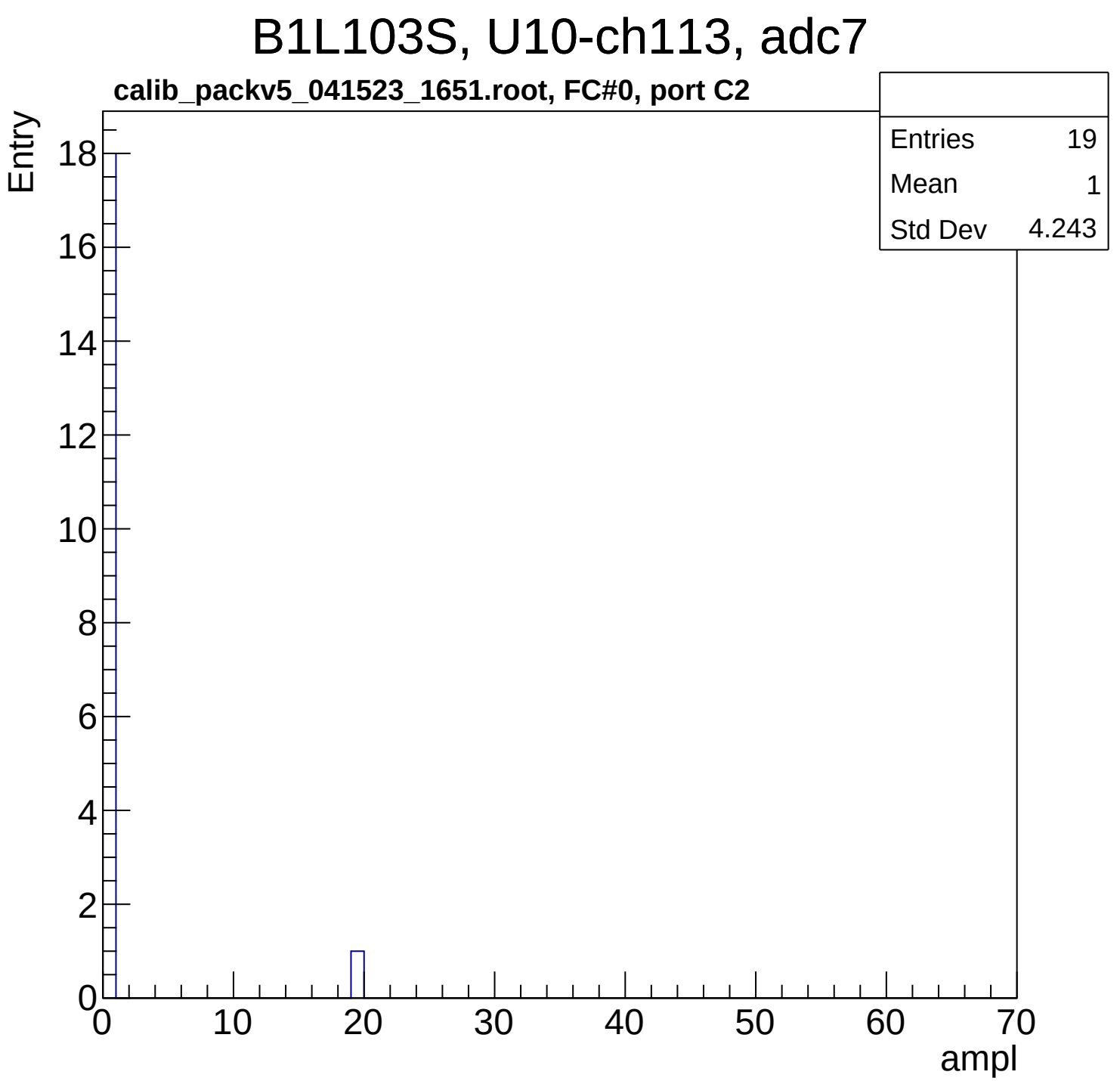

B1L103S, U10-ch113, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 39.36
Std Dev 13.36
Entry
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl

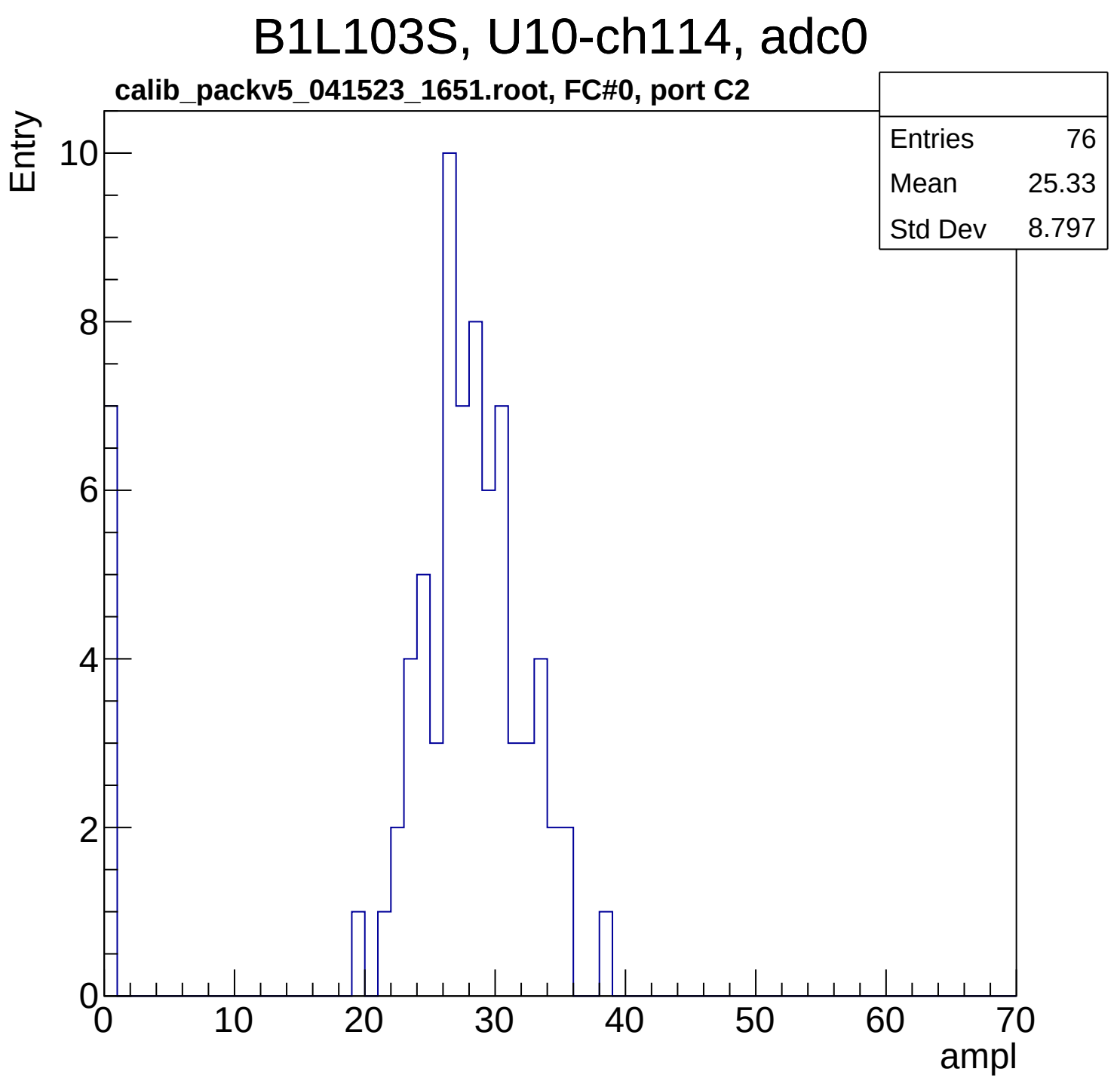

B1L103S, U10-ch113, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 50.83
Std Dev 3.96
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

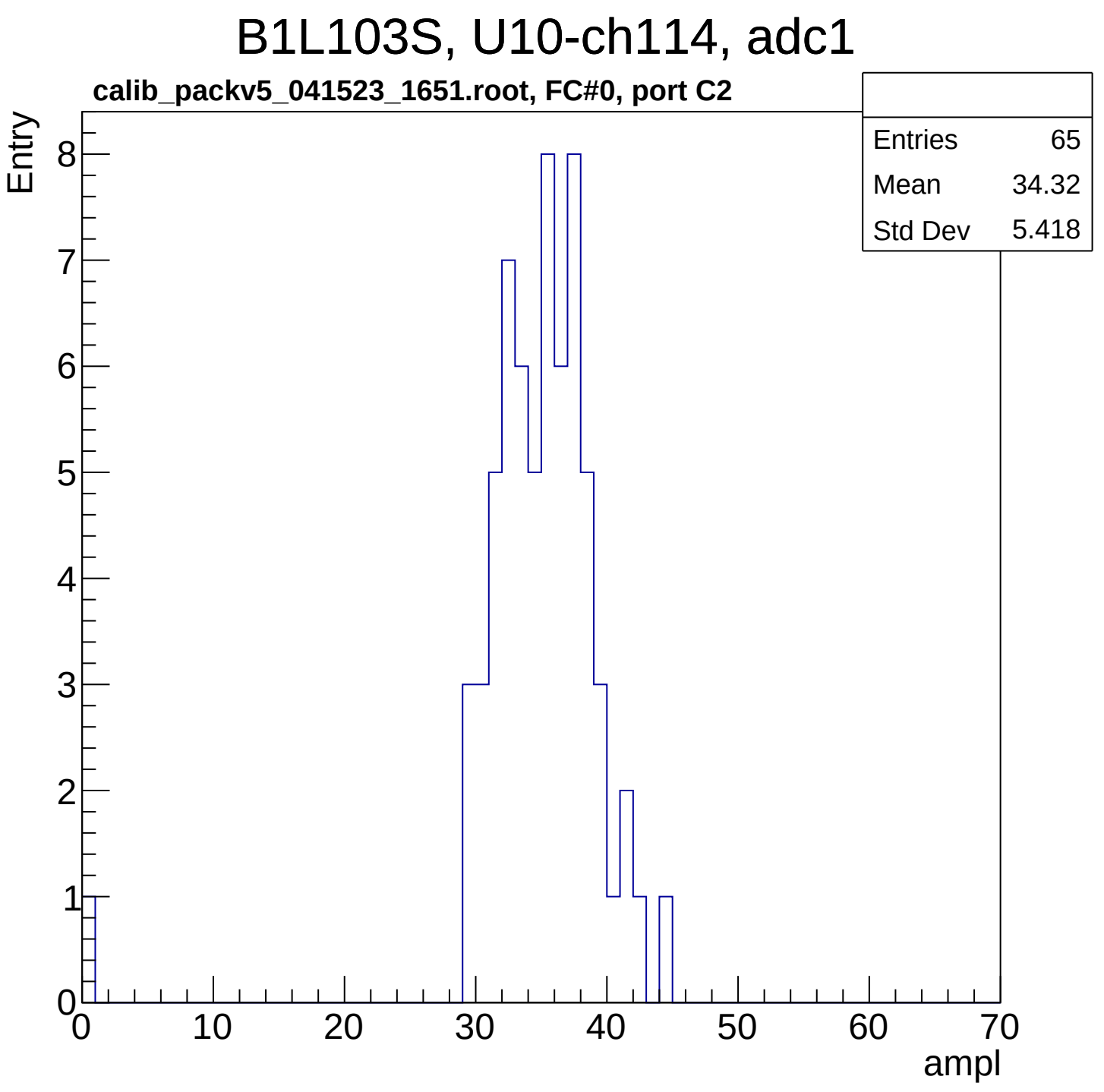

B1L103S, U10-ch113, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 56.34
Std Dev 2.963
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U10-ch113, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 42
Mean 60.38
Std Dev 2.41
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U10-ch113, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 3
Mean 42
Std Dev 29.7
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U10-ch113, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1
Std Dev 4.243
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch114, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 25.33
Std Dev 8.797
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U10-ch114, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 34.32
Std Dev 5.418
Entry
ampl
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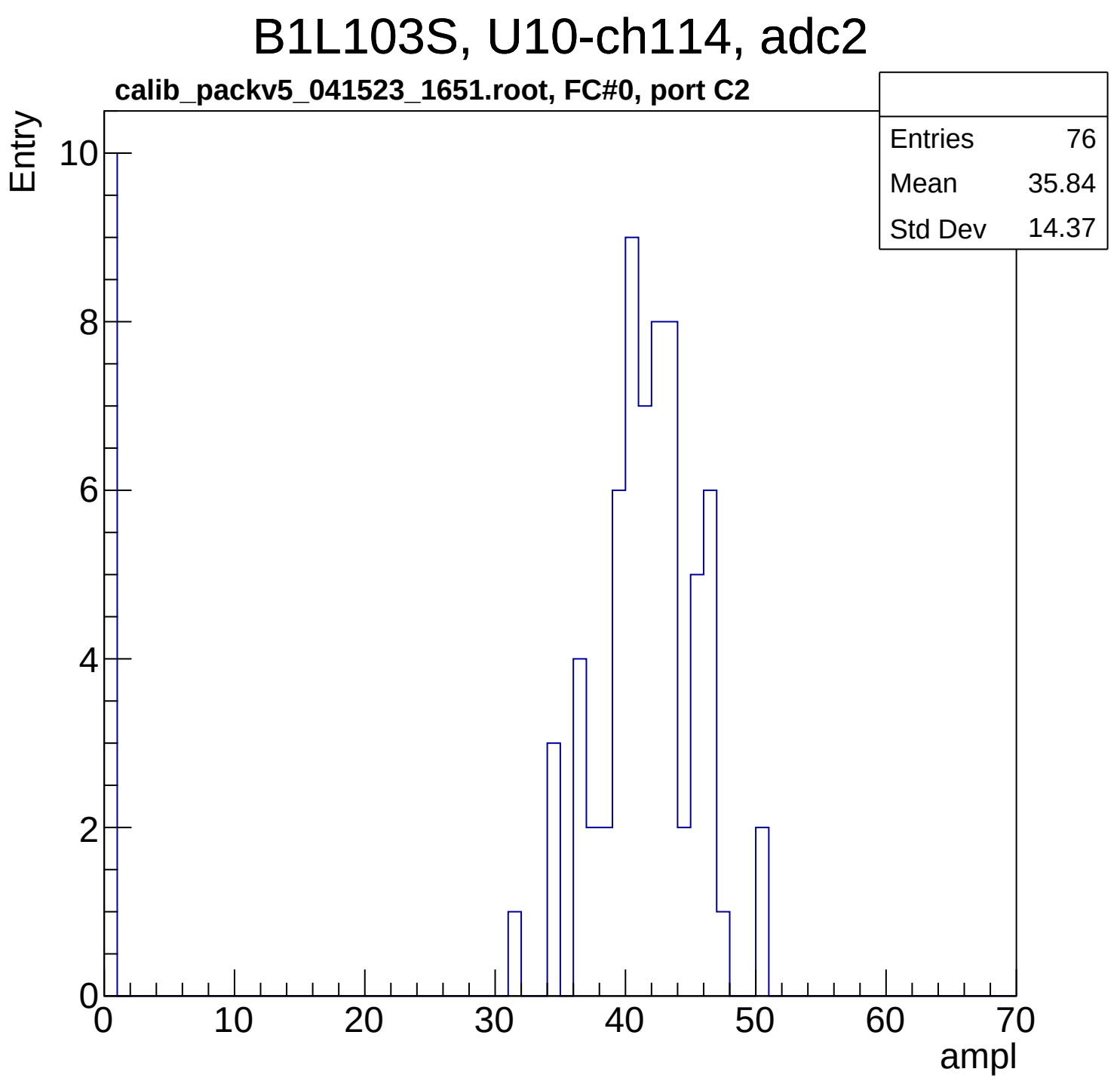
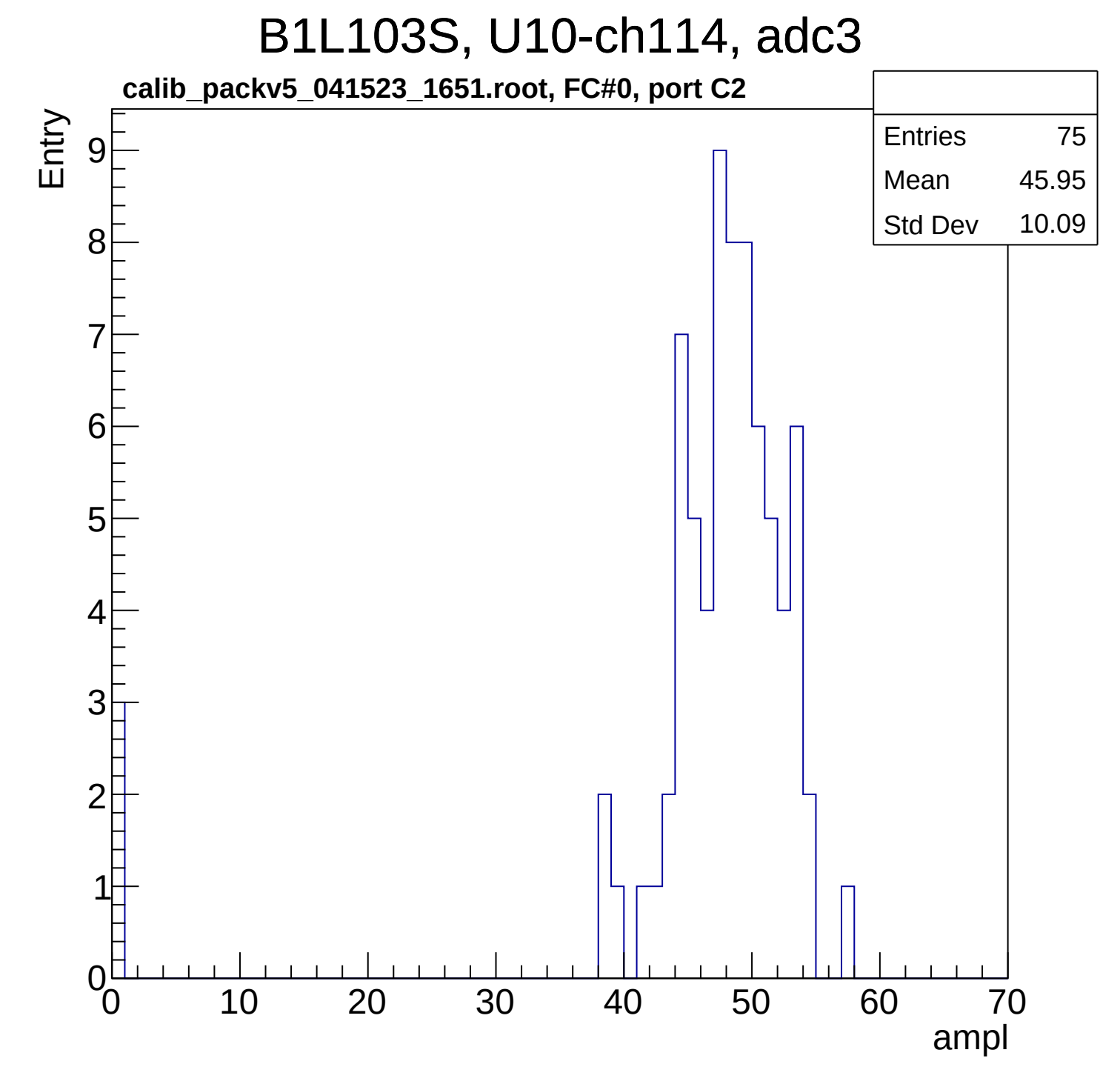
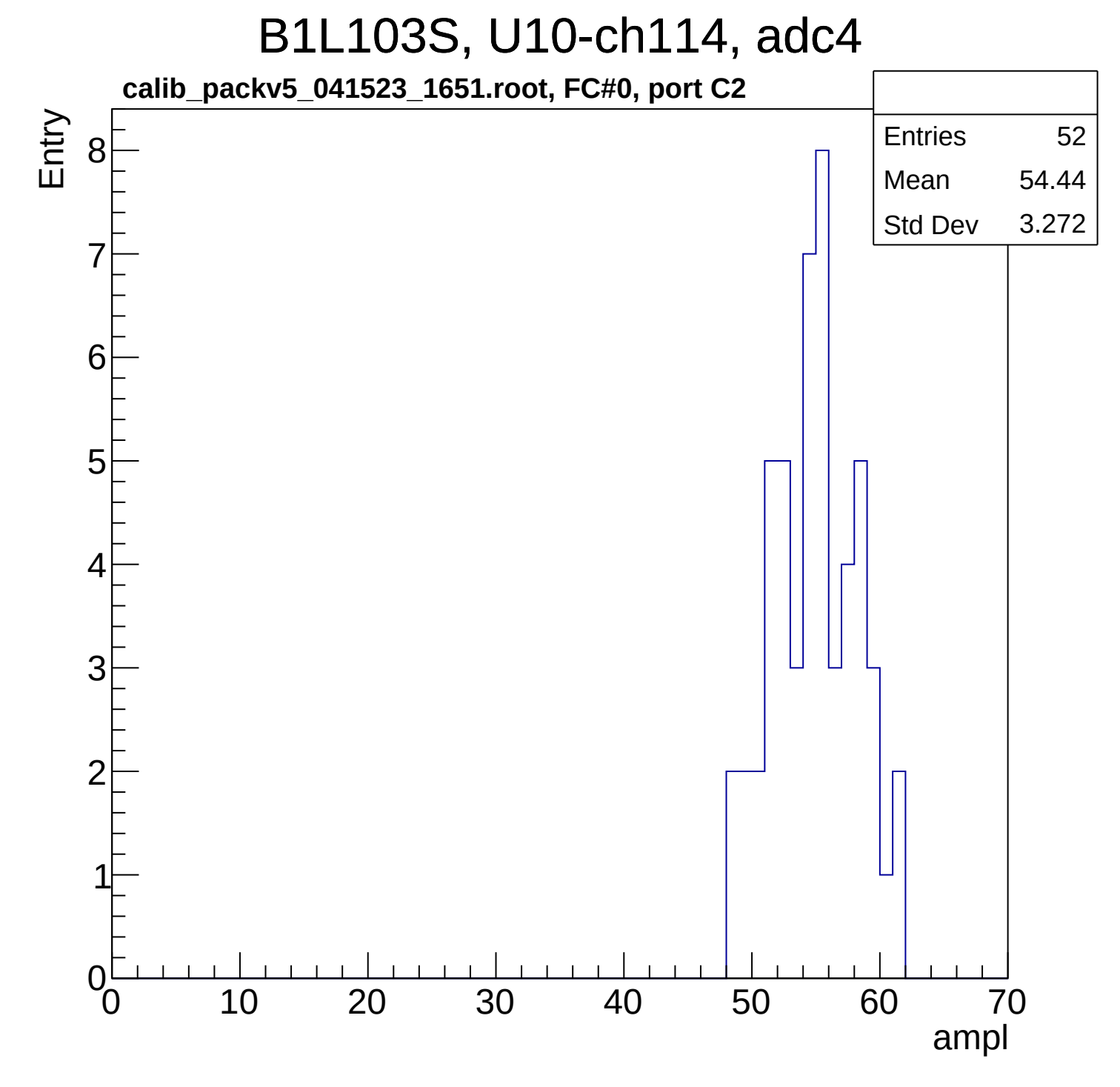
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U10-ch114, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 35.84
Std Dev 14.37
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U10-ch114, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 45.95
Std Dev 10.09
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U10-ch114, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 54.44
Std Dev 3.272
Entry
ampl
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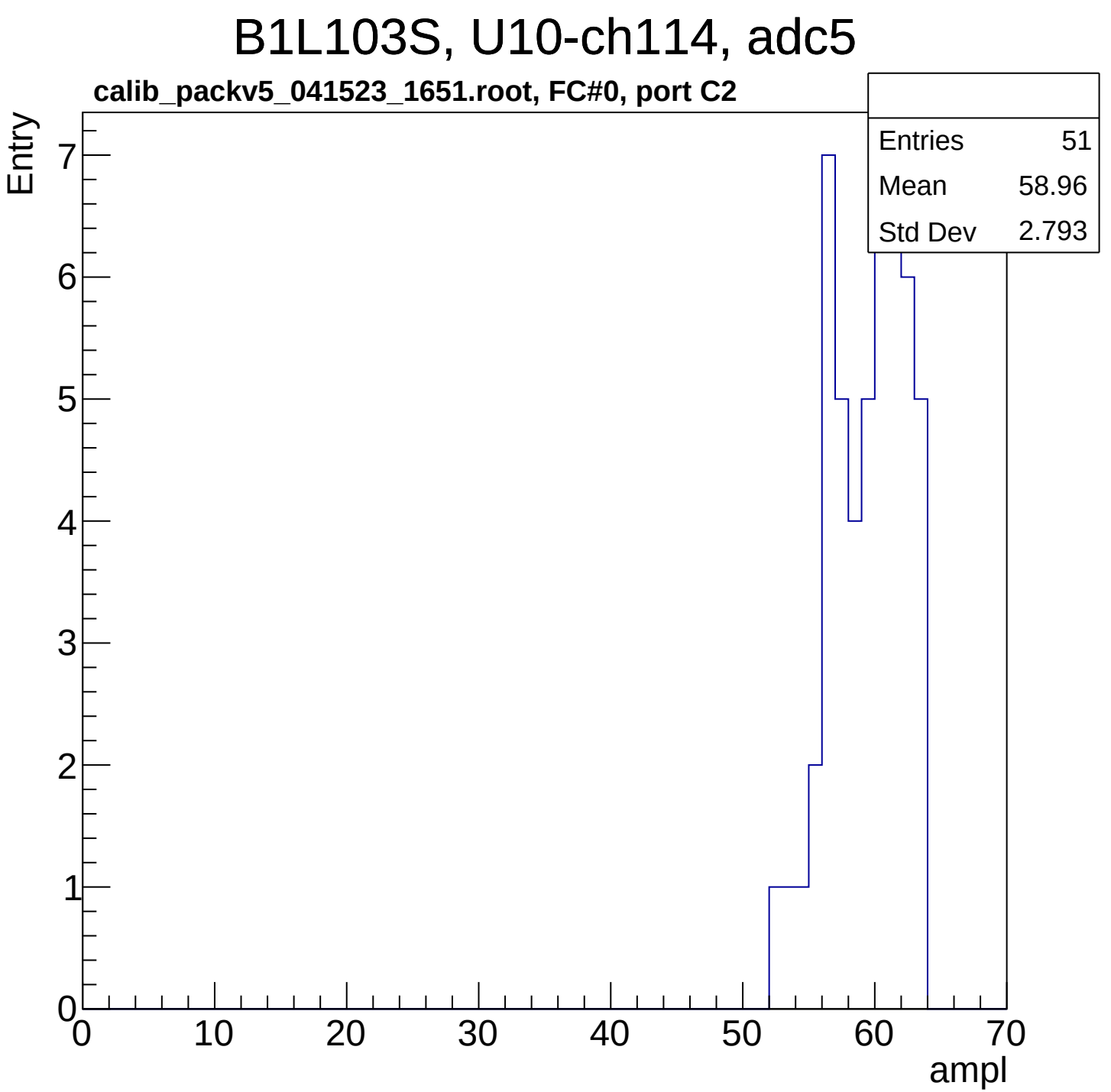
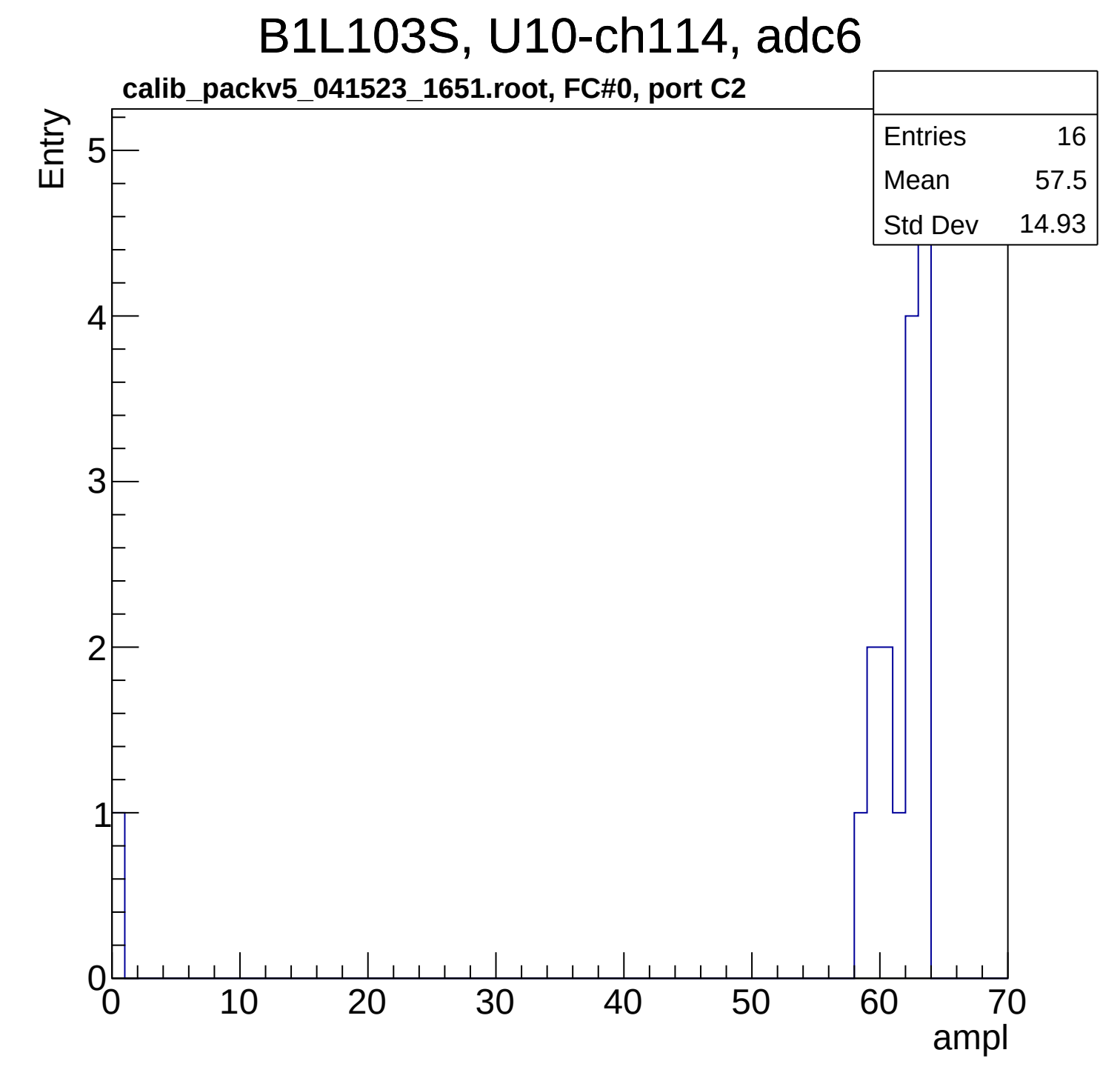
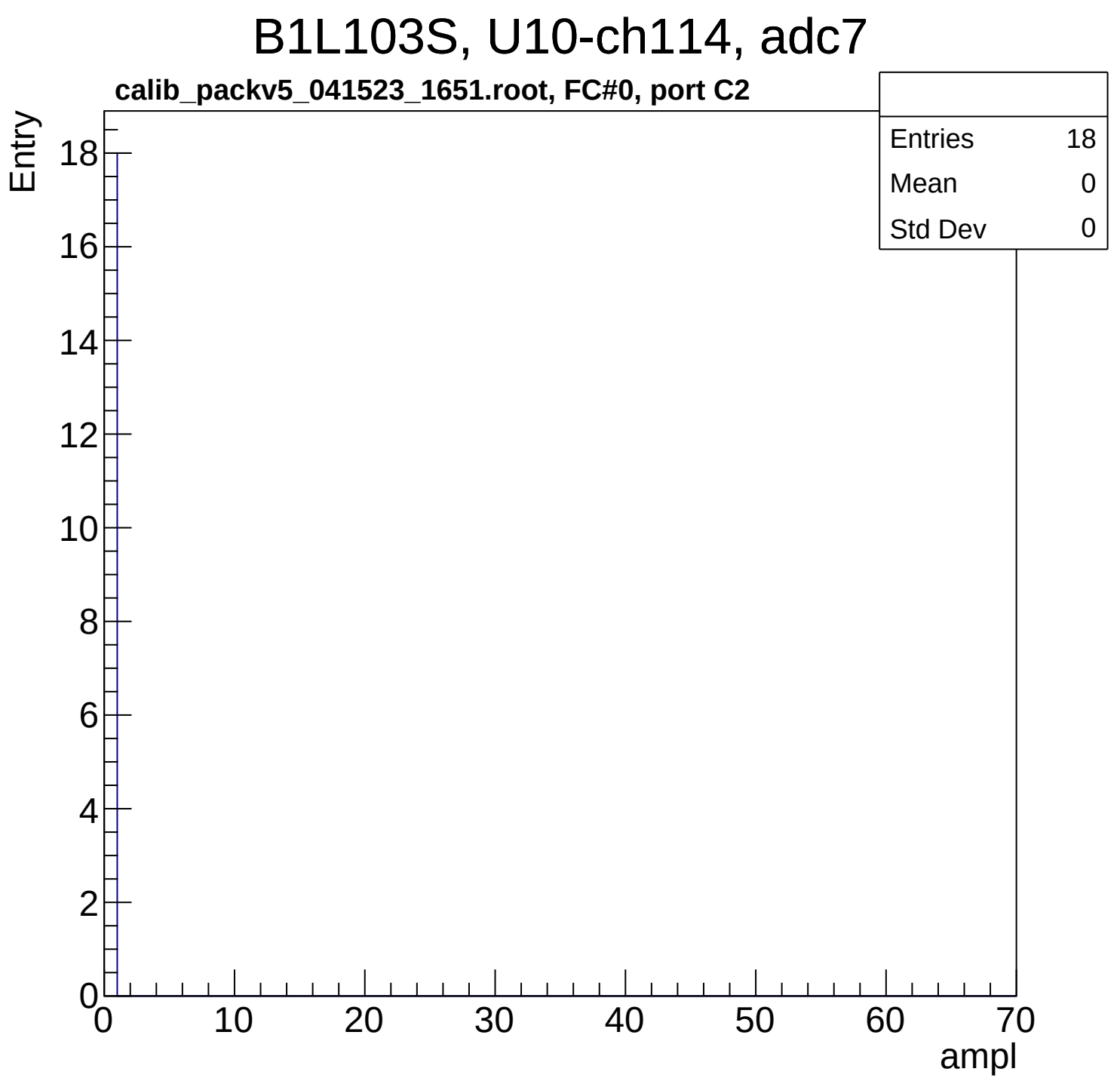
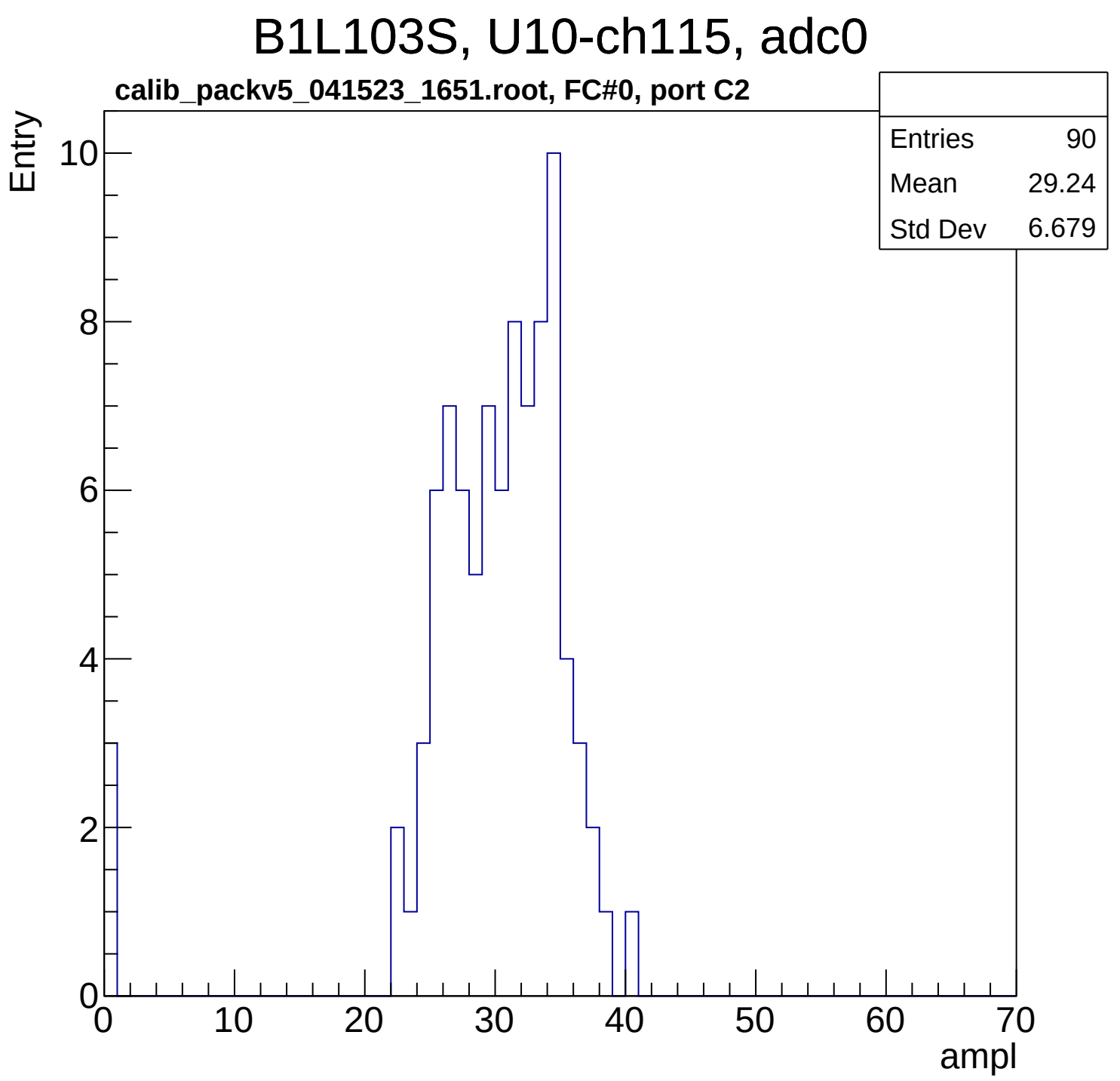
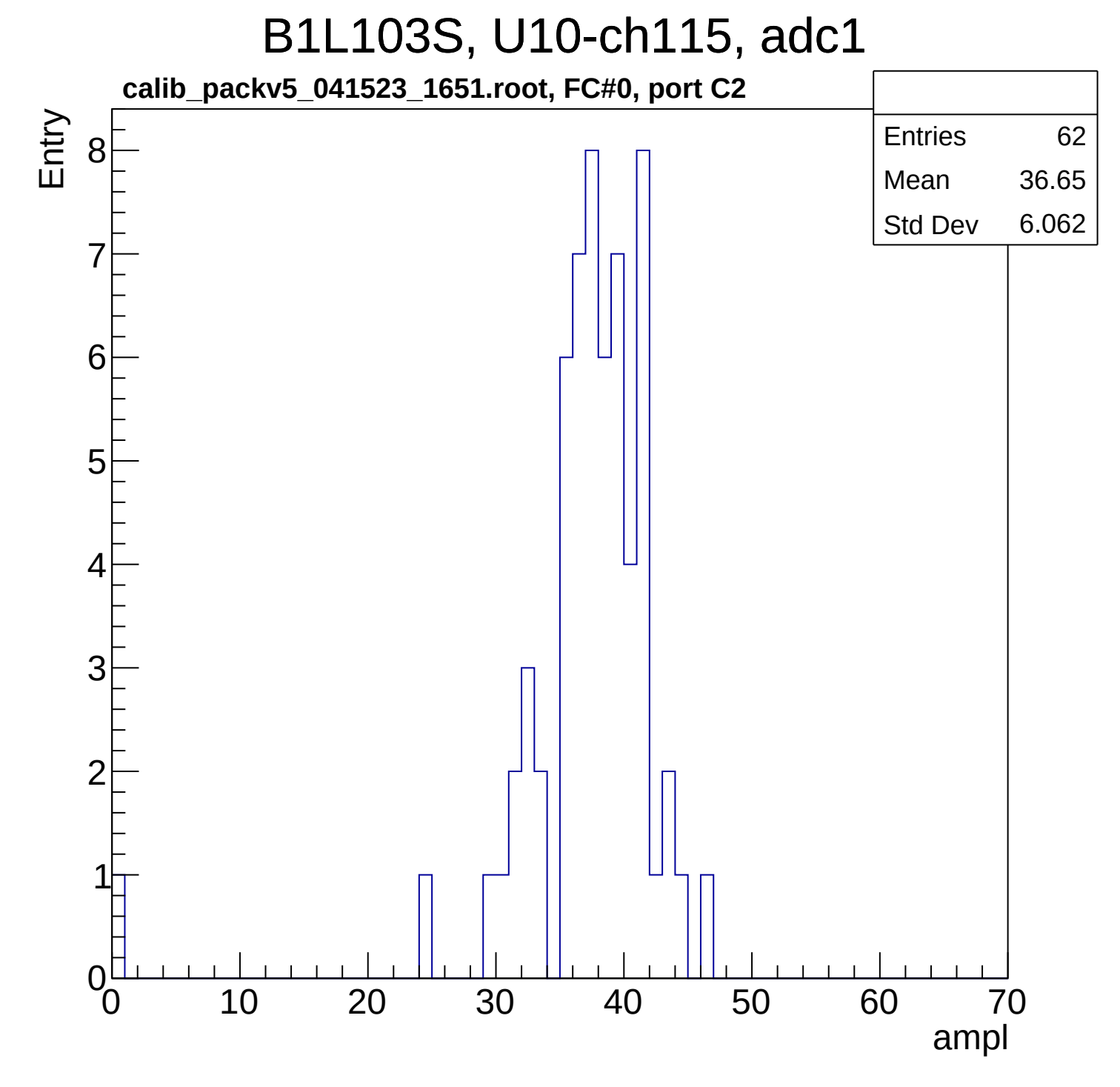
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U10-ch114, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 58.96
Std Dev 2.793
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U10-ch114, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 16
Mean 57.5
Std Dev 14.93
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U10-ch114, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch115, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 90
Mean 29.24
Std Dev 6.679
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U10-ch115, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 36.65
Std Dev 6.062
Entry
ampl
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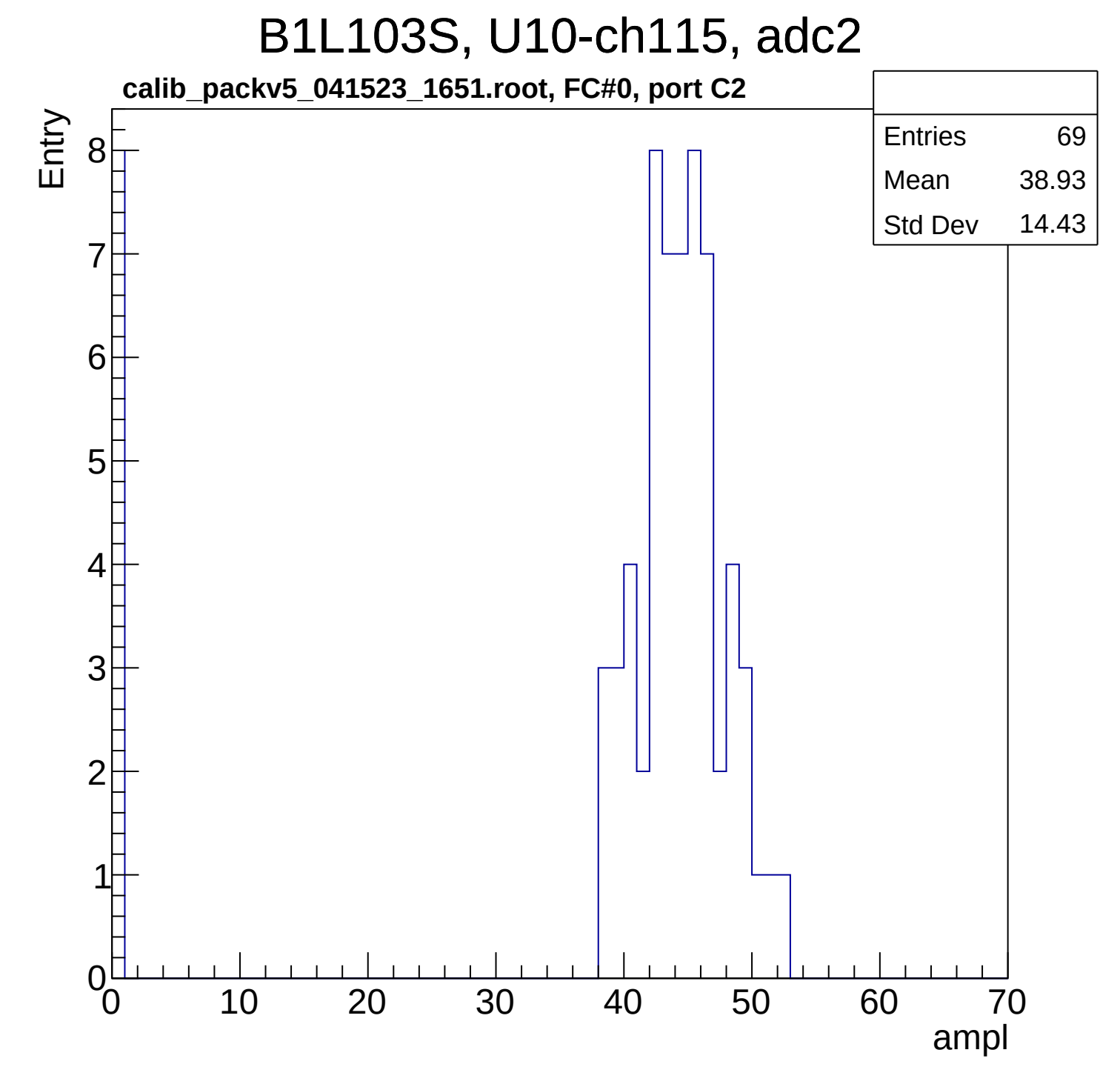
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U10-ch115, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 38.93
Std Dev 14.43
Entry
ampl
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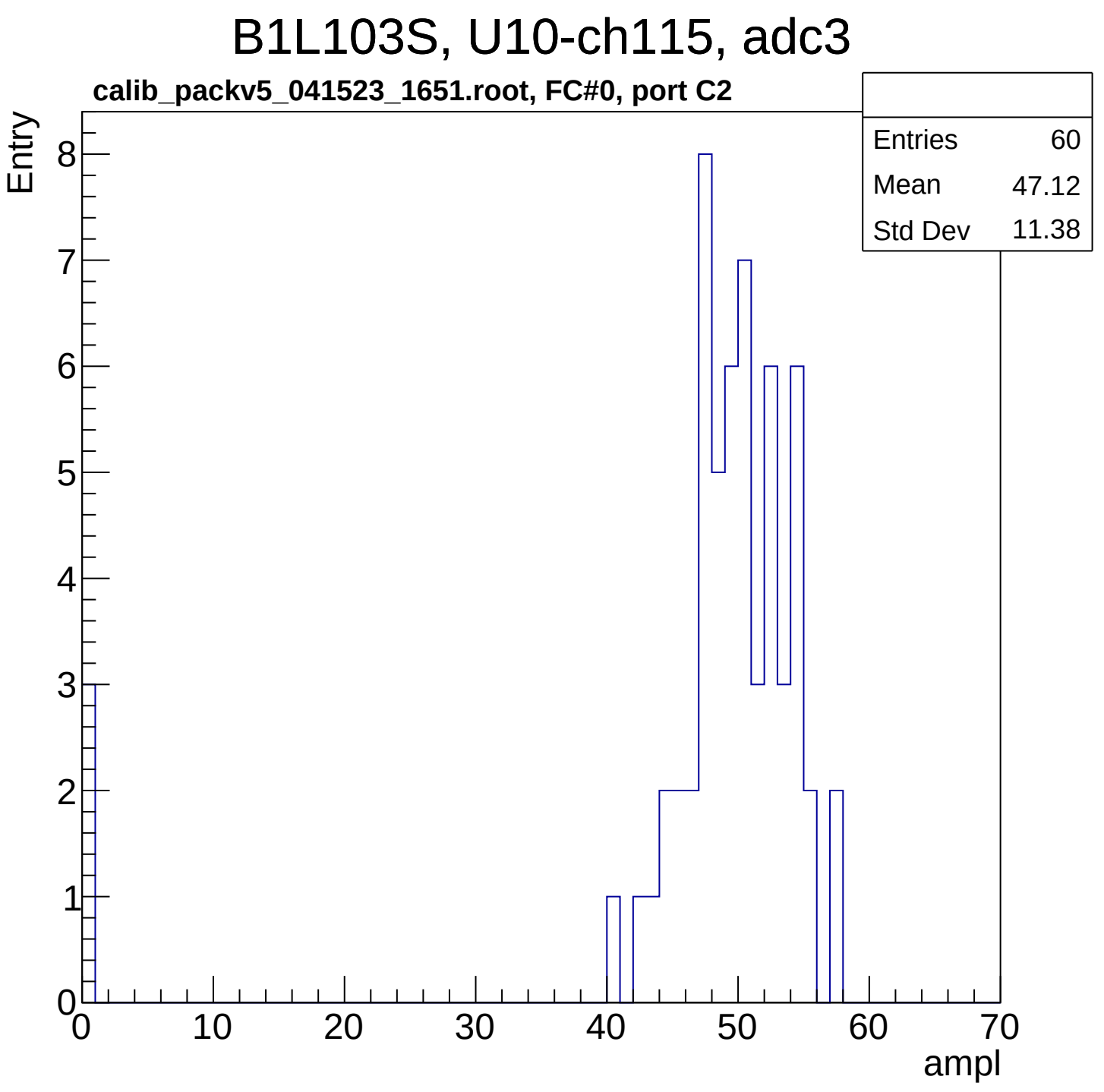
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U10-ch115, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 47.12
Std Dev 11.38
Entry
ampl
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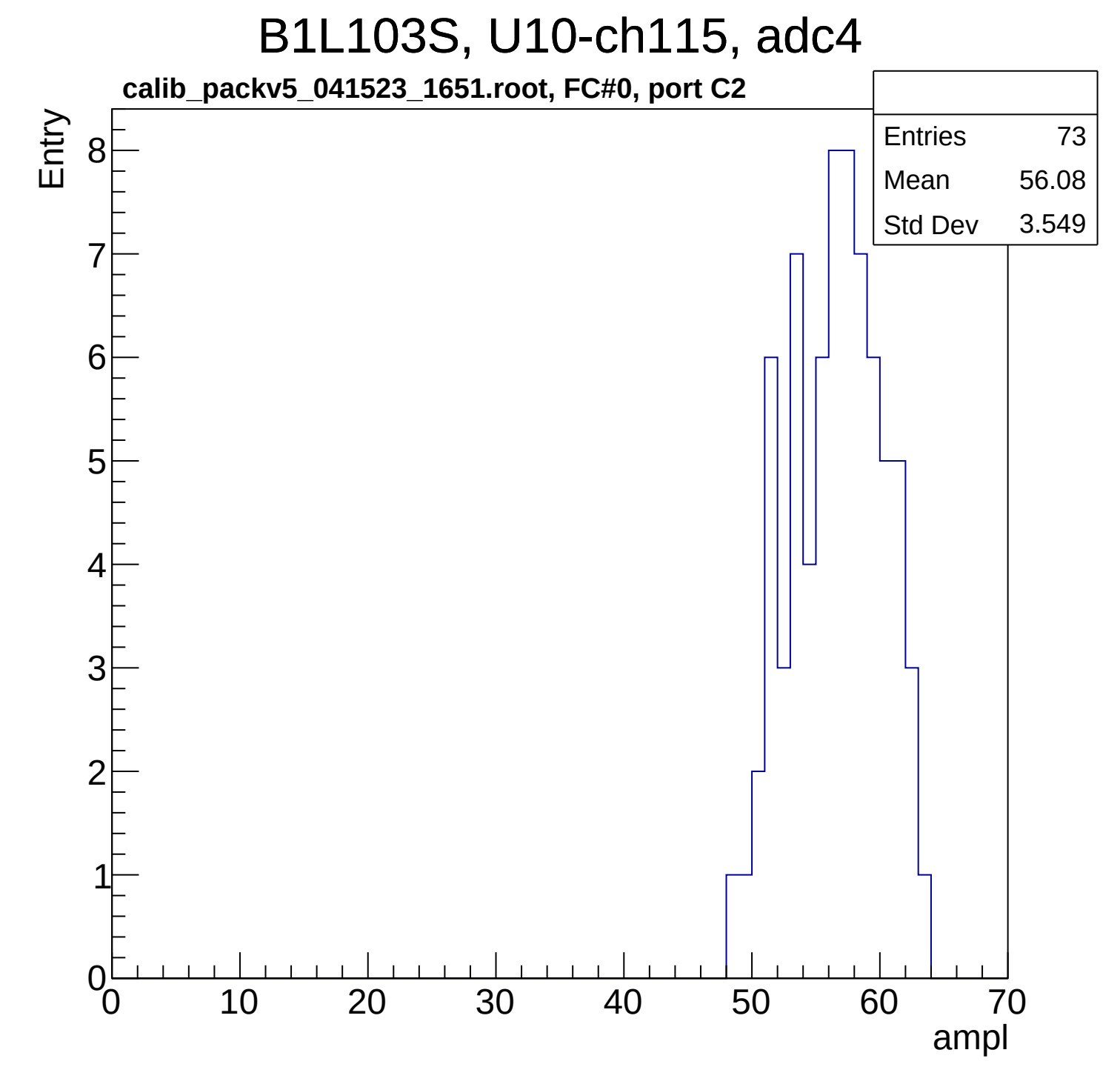
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U10-ch115, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 56.08
Std Dev 3.549
Entry
ampl
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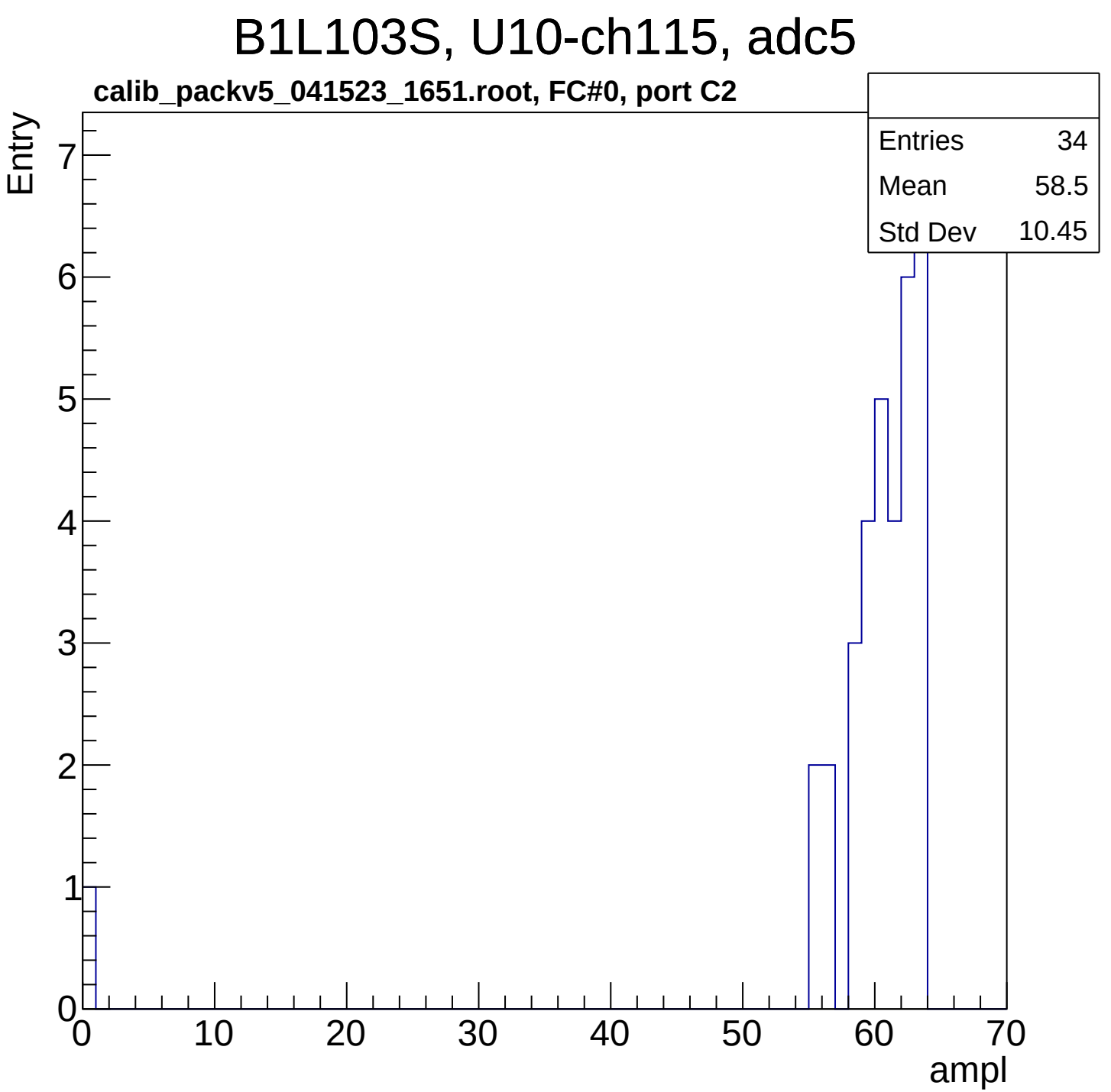
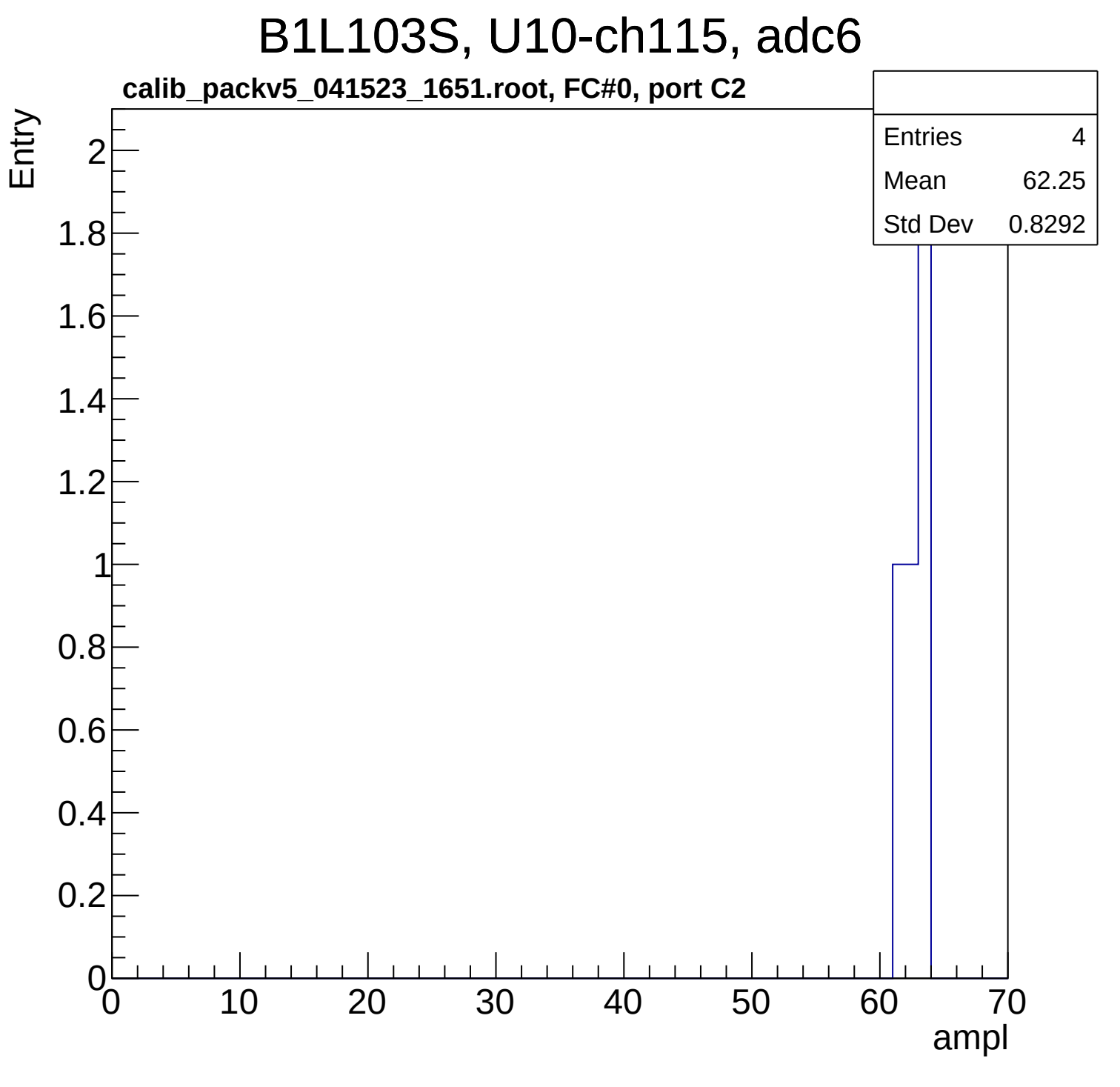
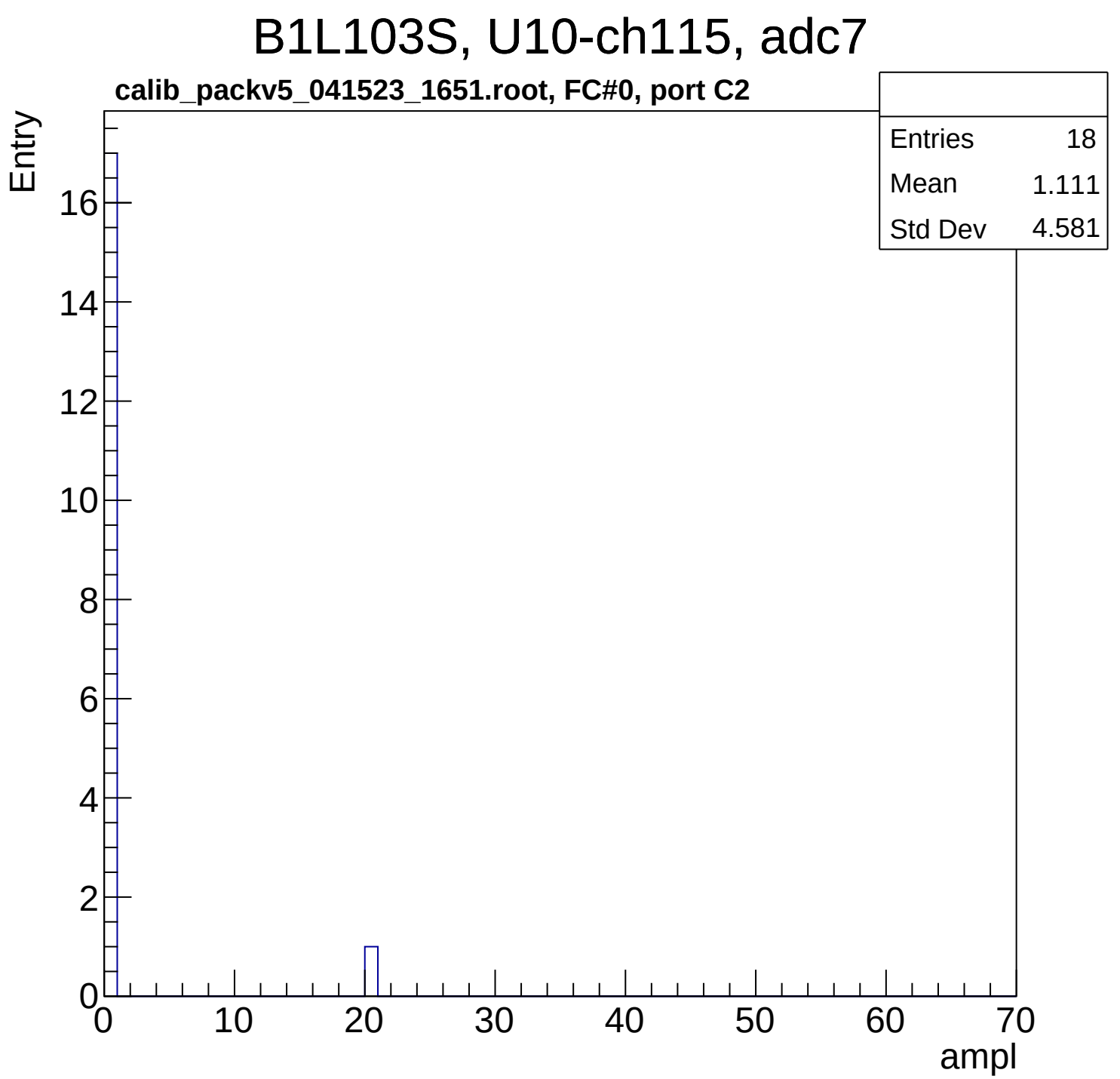
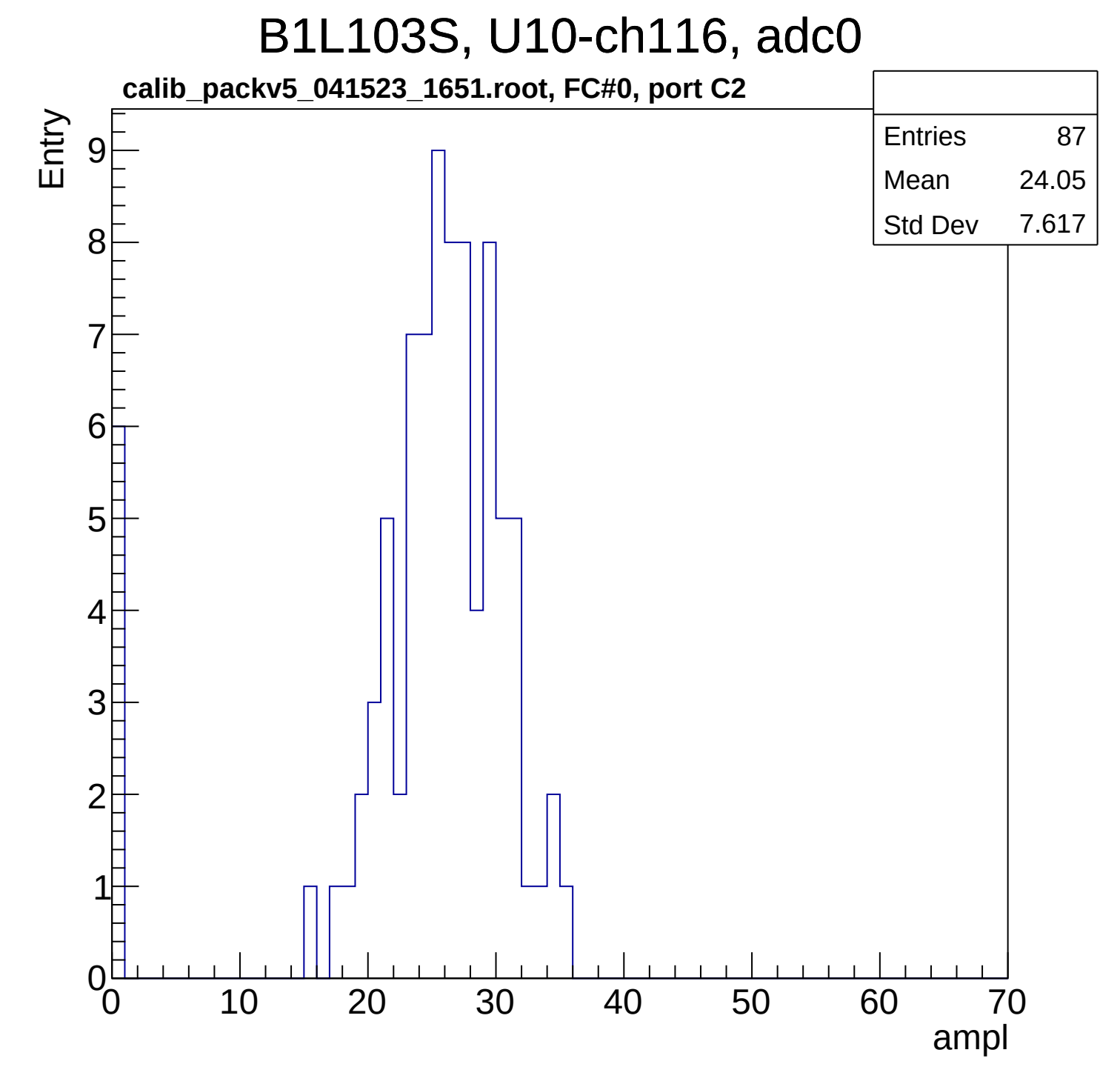
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U10-ch115, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 34
Mean 58.5
Std Dev 10.45
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U10-ch115, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 4
Mean 62.25
Std Dev 0.8292
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U10-ch115, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 1.111
Std Dev 4.581
Entry
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch116, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 87
Mean 24.05
Std Dev 7.617
Entry
ampl
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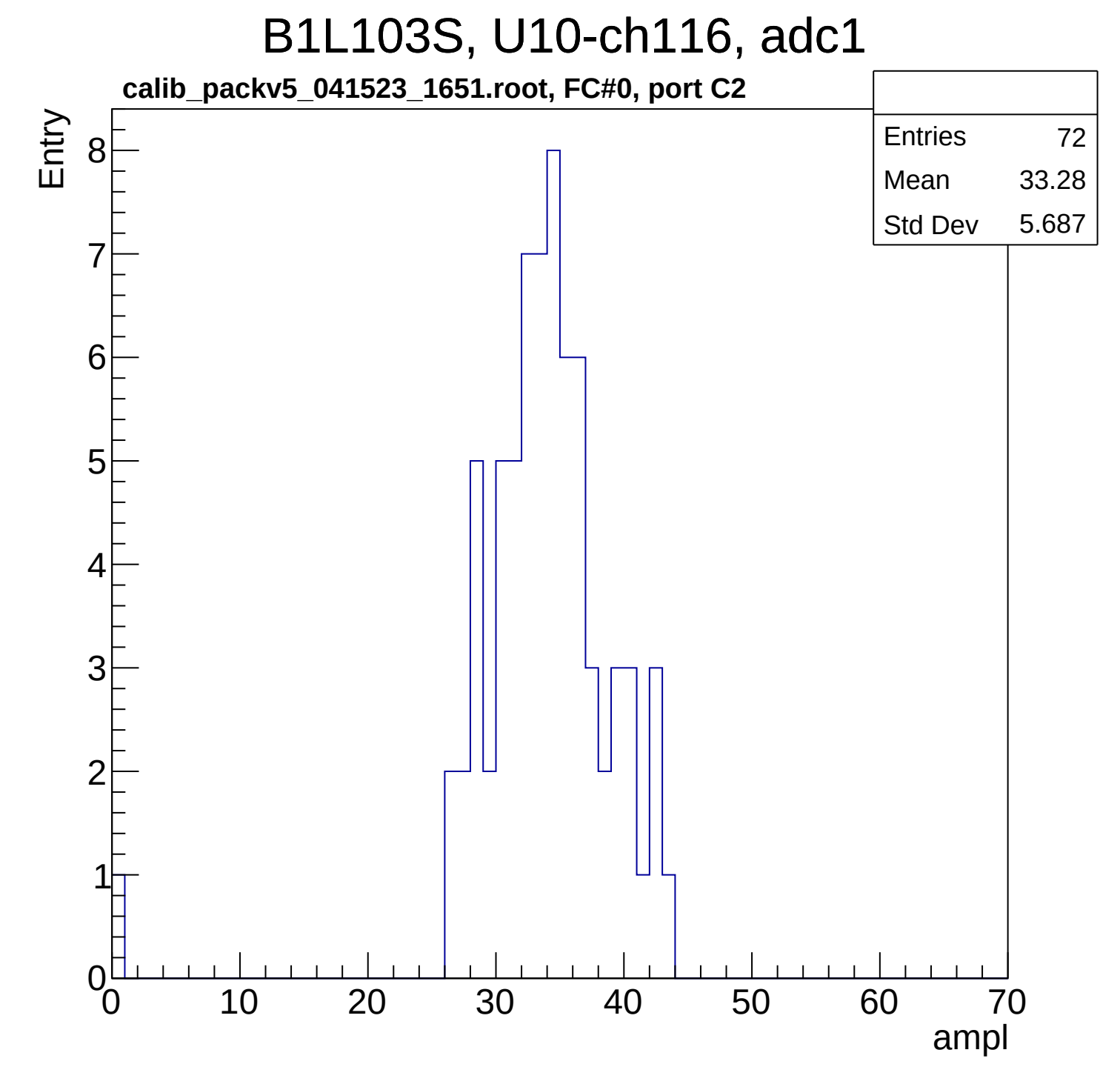
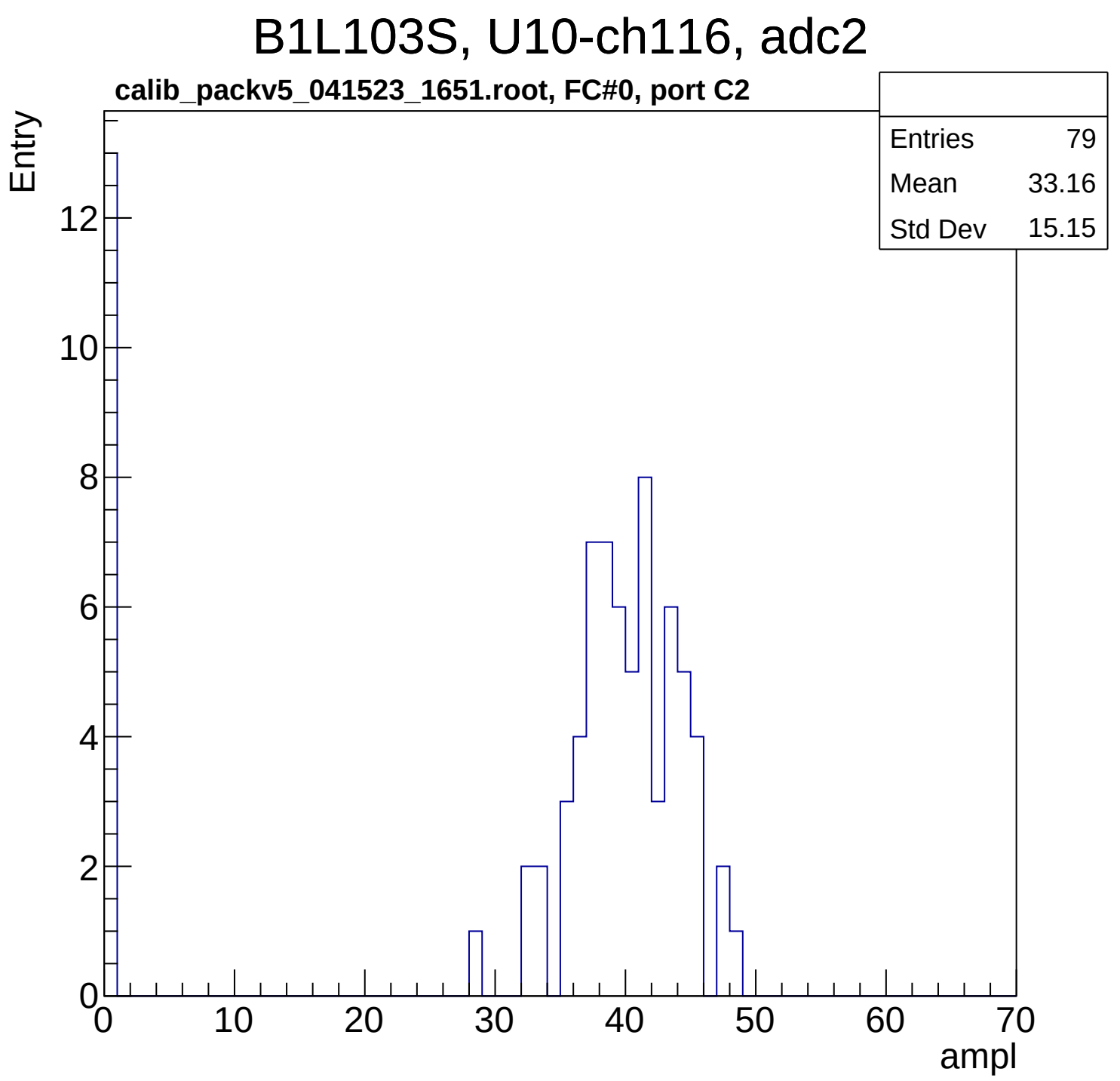
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U10-ch116, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 33.28
Std Dev 5.687
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U10-ch116, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 33.16
Std Dev 15.15
Entry
0
2
4
6
8
10
12
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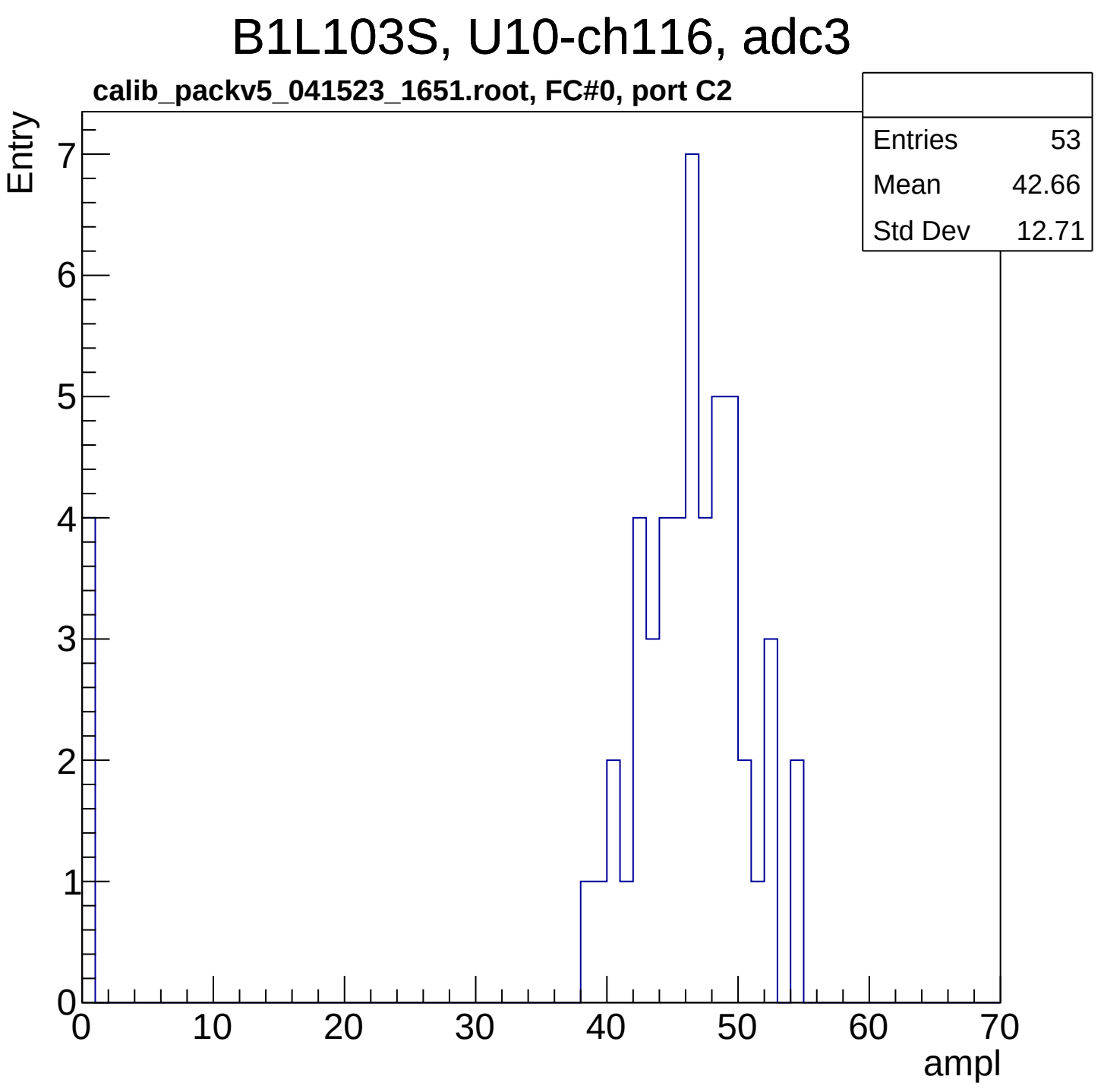
70
ampl


B1L103S, U10-ch116, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 42.66
Std Dev 12.71
Entry
ampl
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1
2
3
4
5
6
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0
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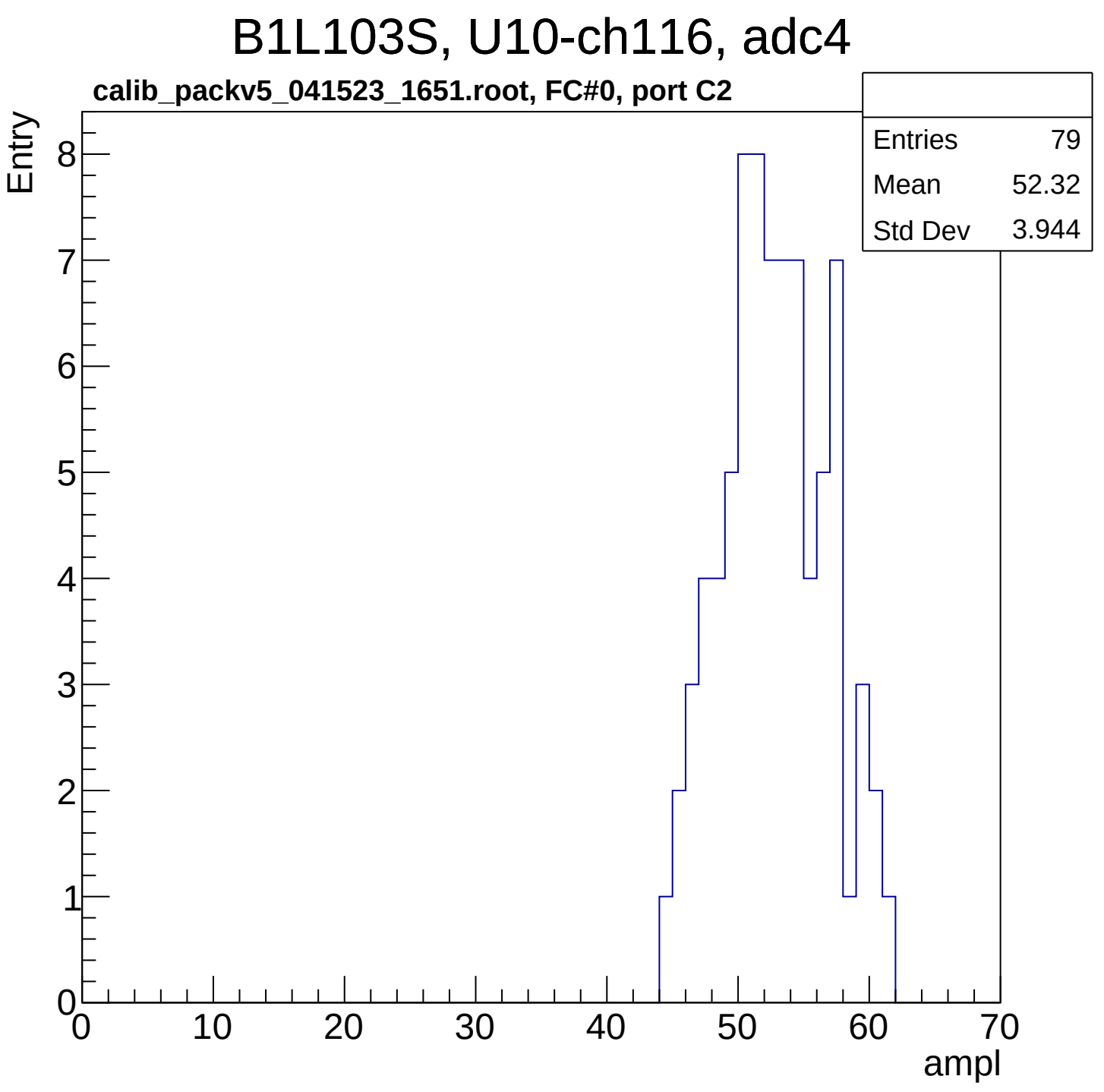
40
50
60
70


B1L103S, U10-ch116, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 52.32
Std Dev 3.944
Entry
ampl
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2
3
4
5
6
7
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0
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40
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60
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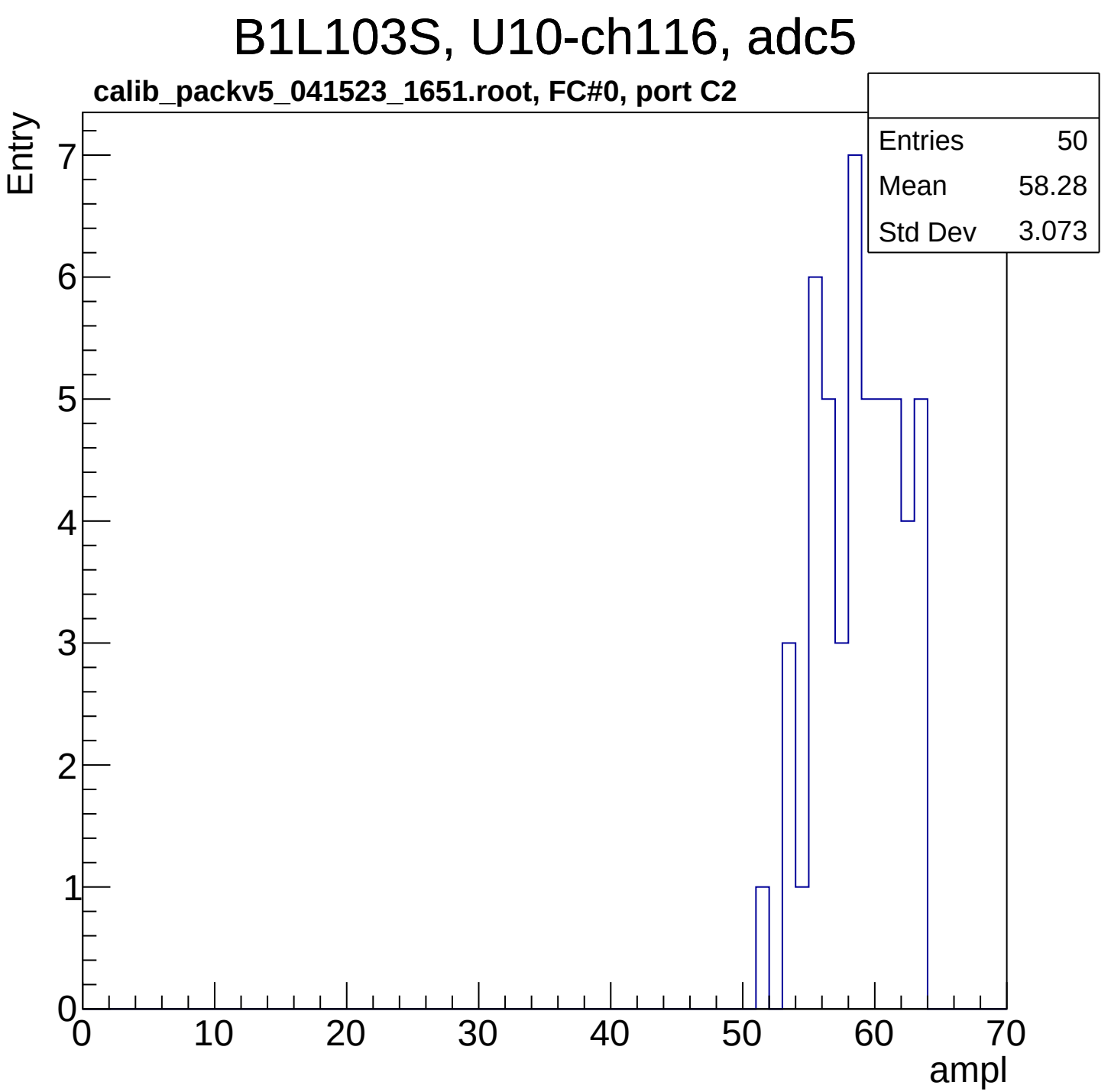
B1L103S, U10-ch116, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 58.28
Std Dev 3.073
Entry
ampl
0
1
2
3
4
5
6
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0
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40
50
60
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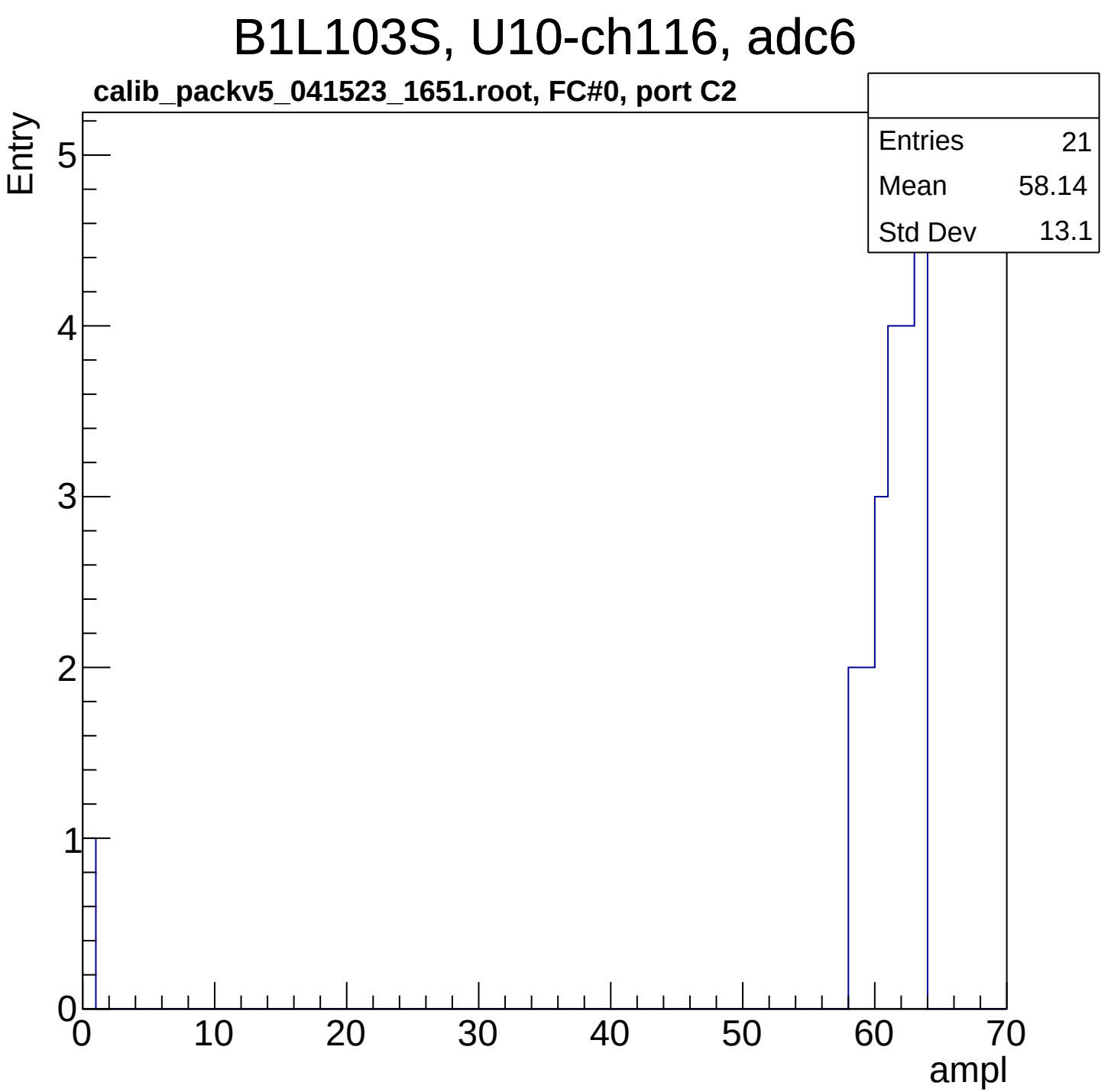
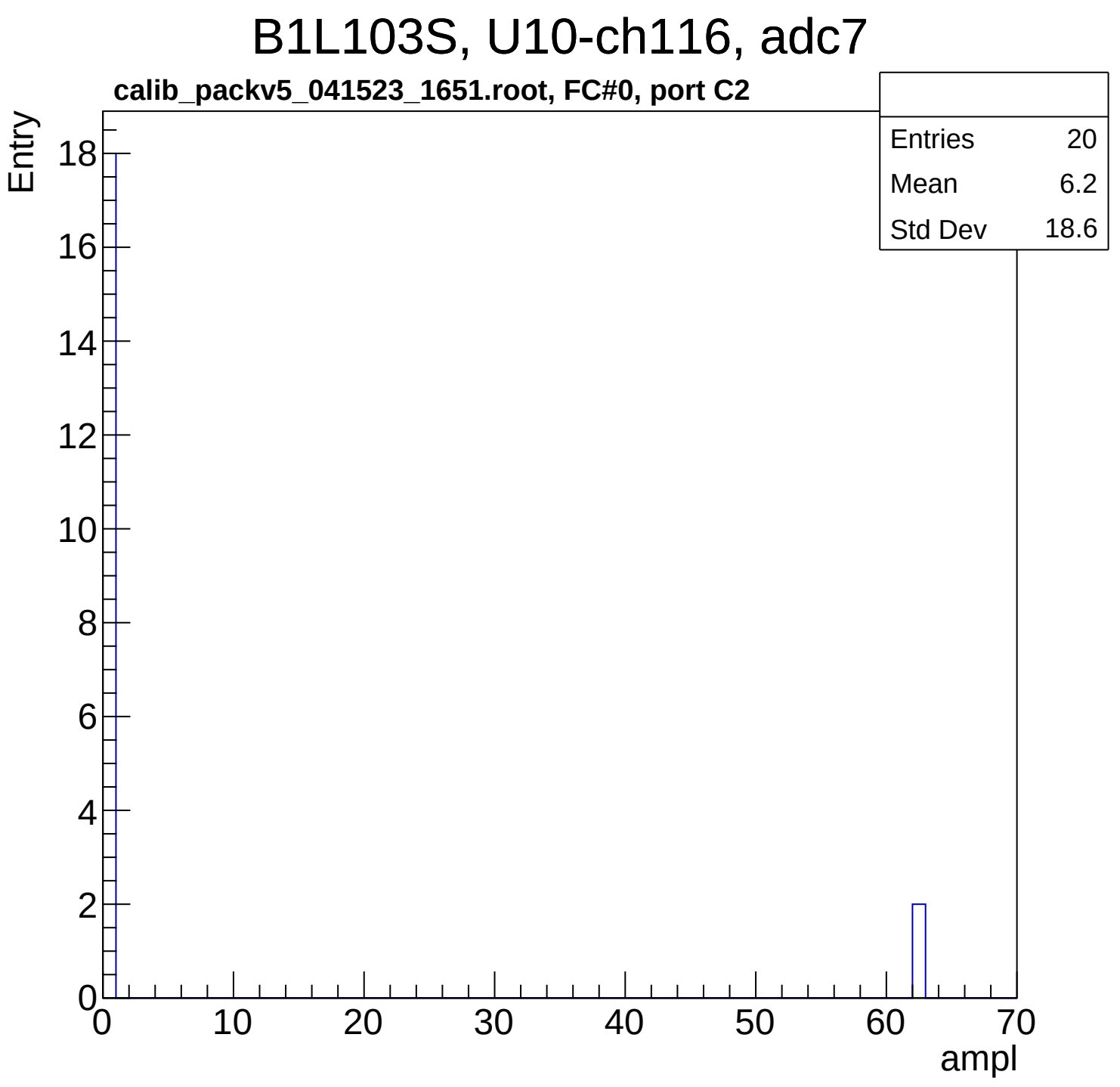
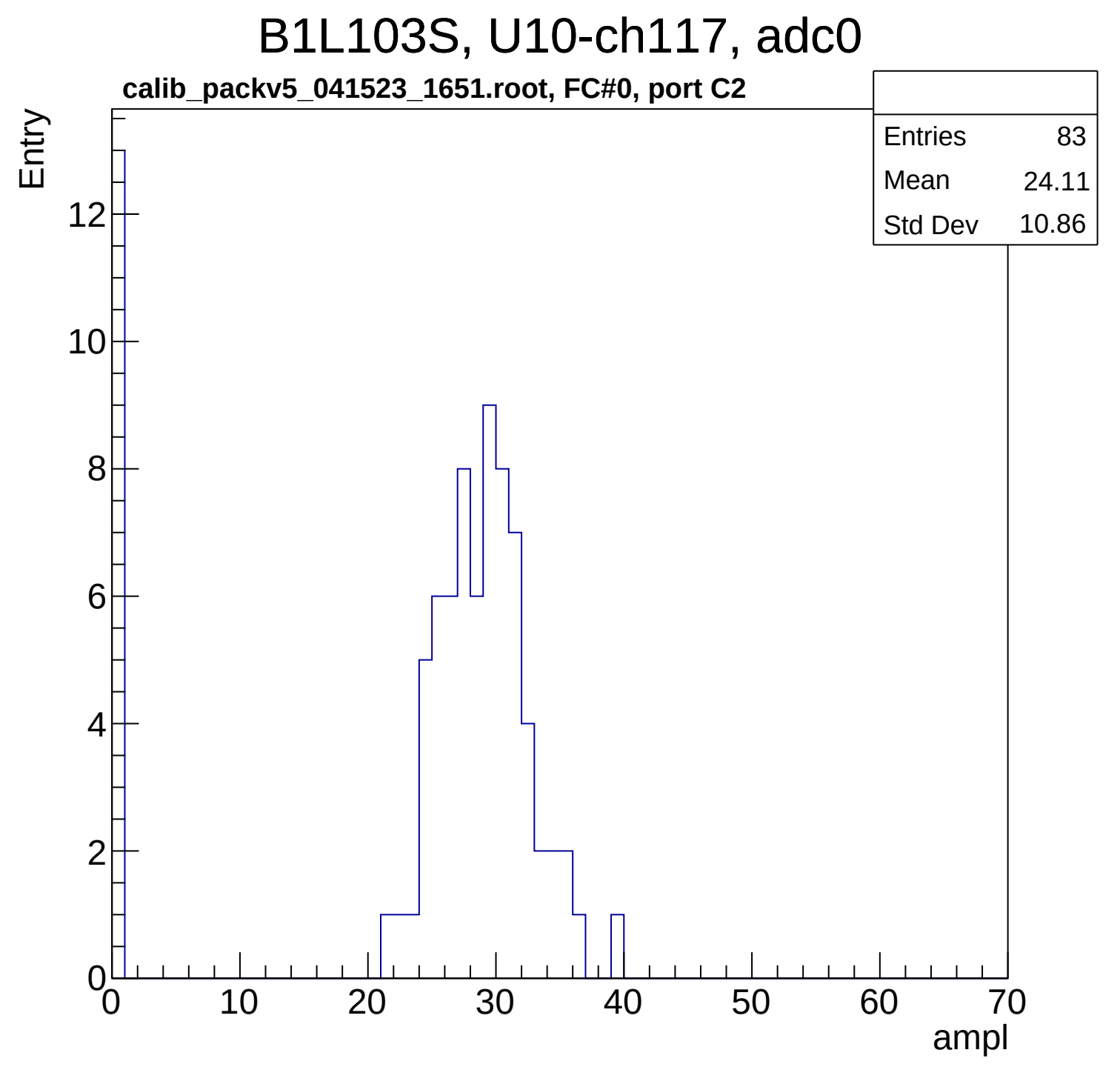
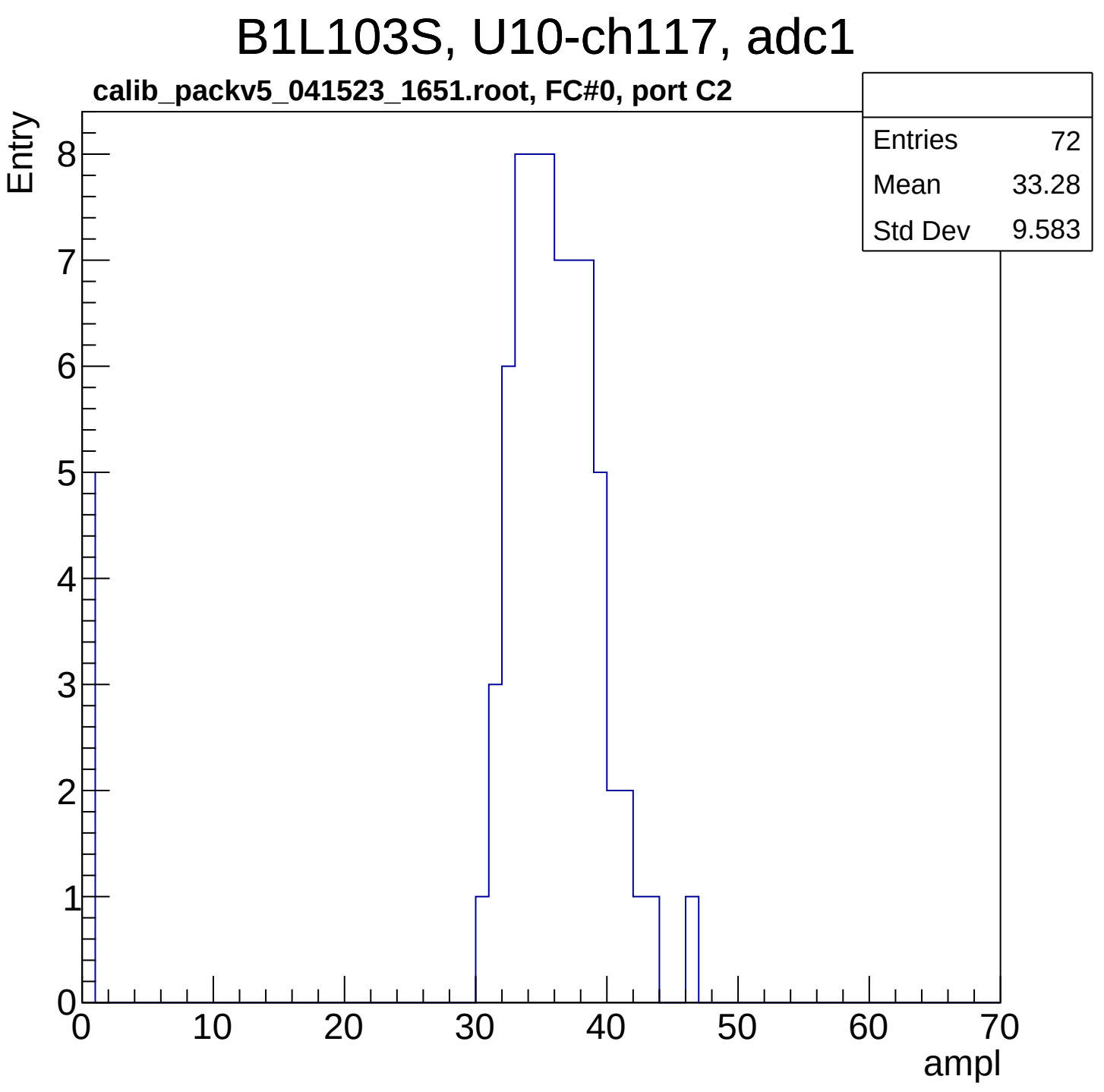

B1L103S, U10-ch116, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 58.14
Std Dev 13.1
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch116, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 6.2
Std Dev 18.6
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch117, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 24.11
Std Dev 10.86
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch117, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 33.28
Std Dev 9.583
Entry
ampl
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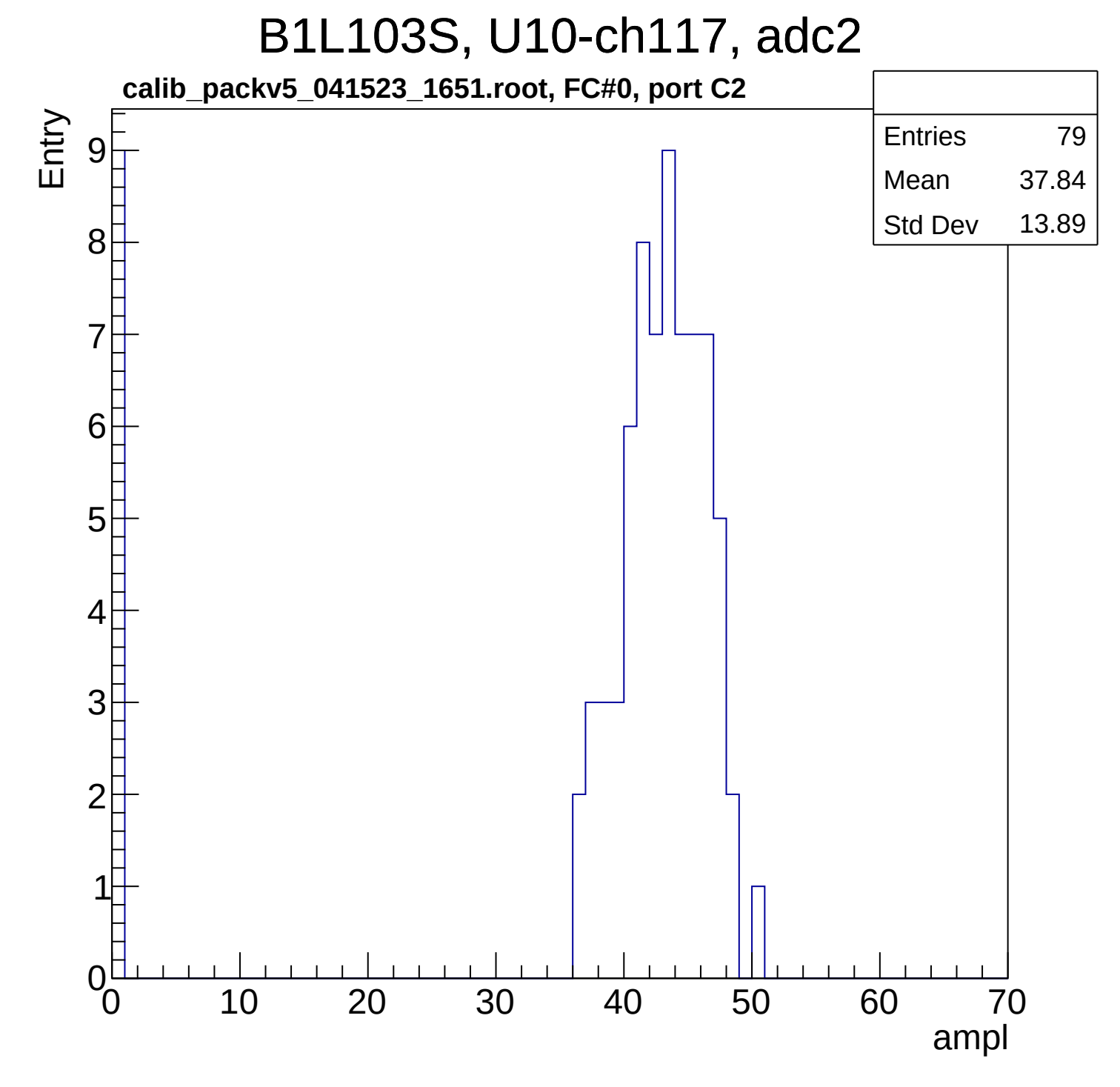
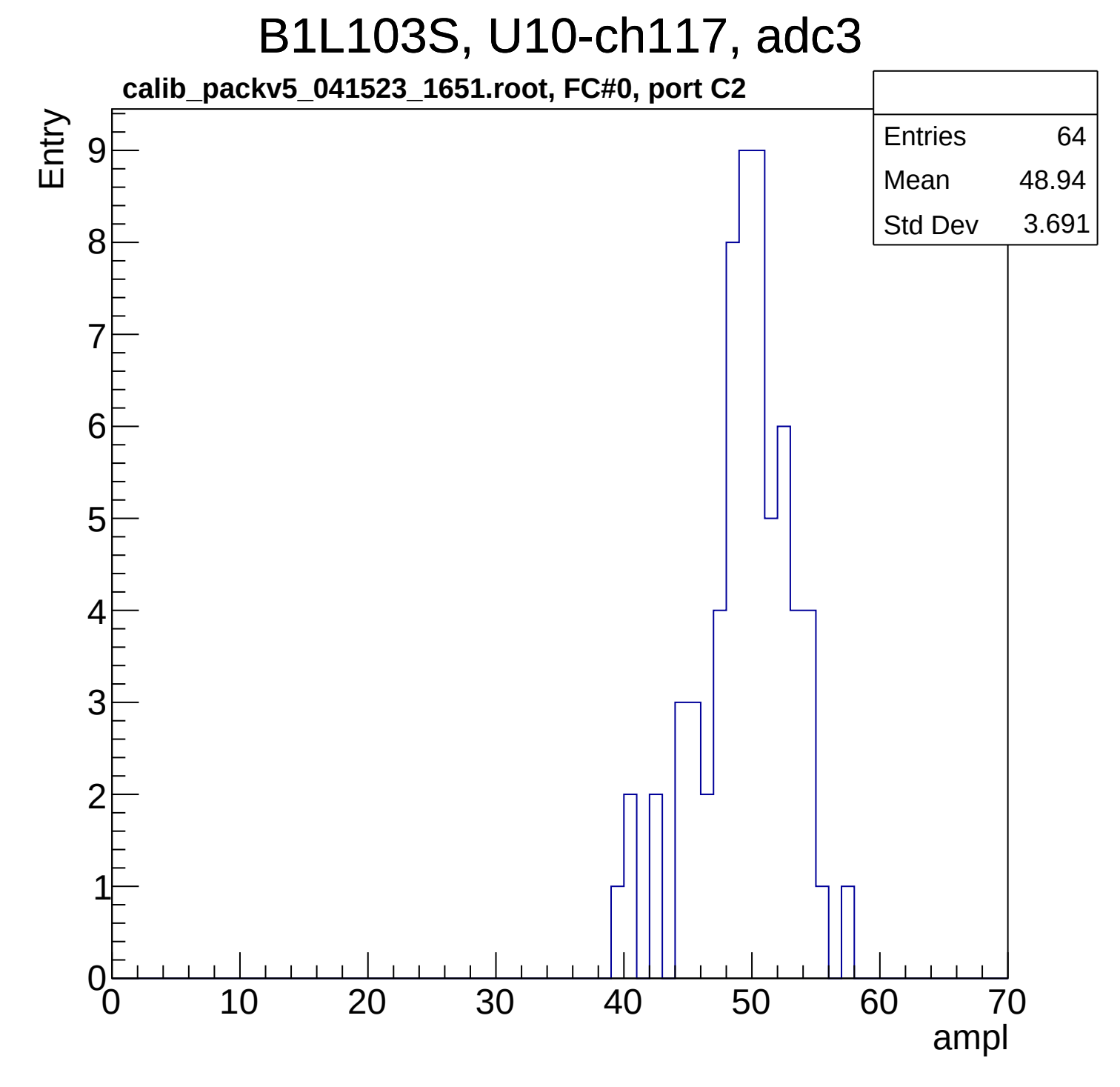
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U10-ch117, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 37.84
Std Dev 13.89
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U10-ch117, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 48.94
Std Dev 3.691
Entry
ampl
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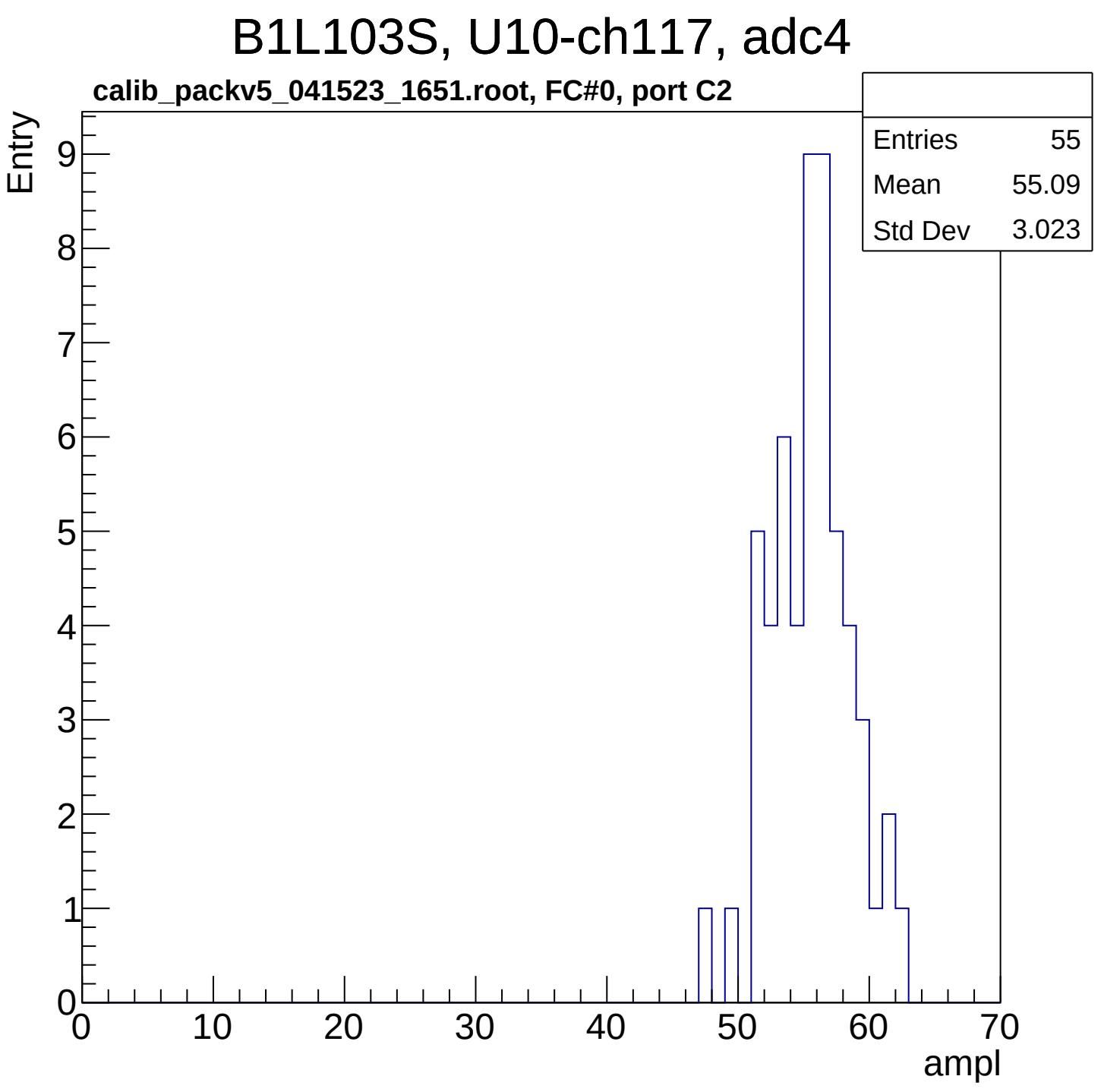
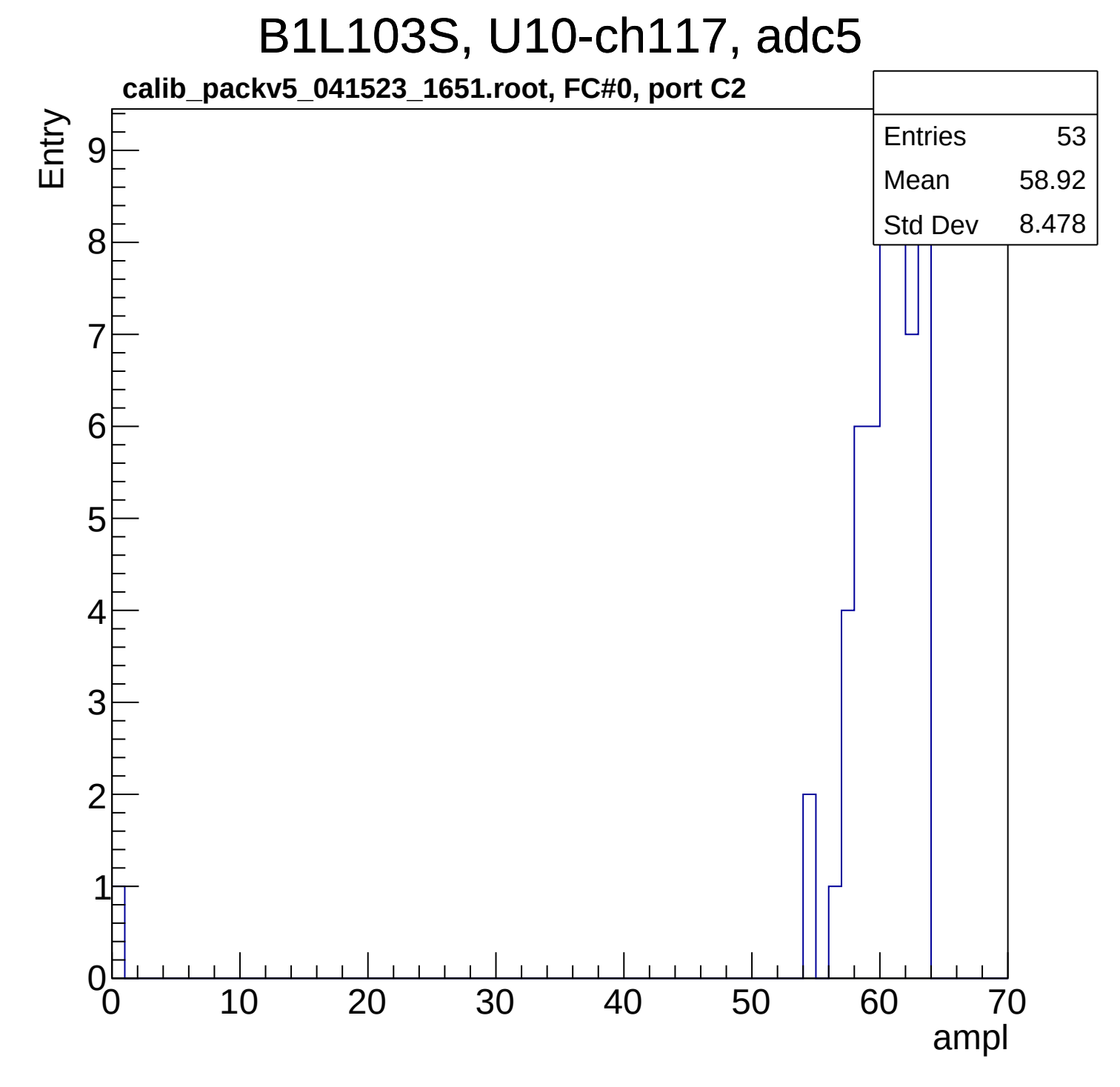
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U10-ch117, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 55.09
Std Dev 3.023
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U10-ch117, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 58.92
Std Dev 8.478
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
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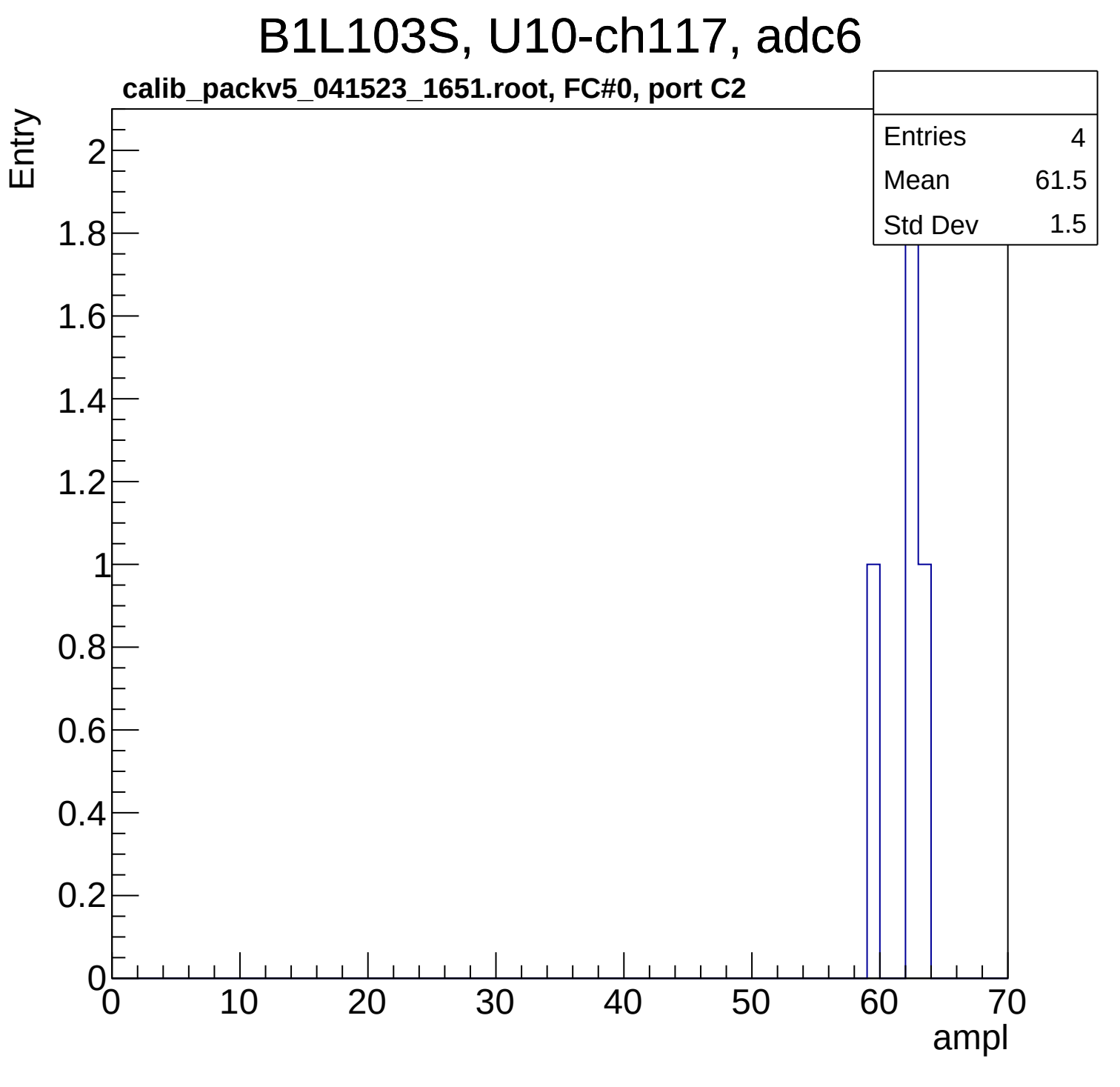
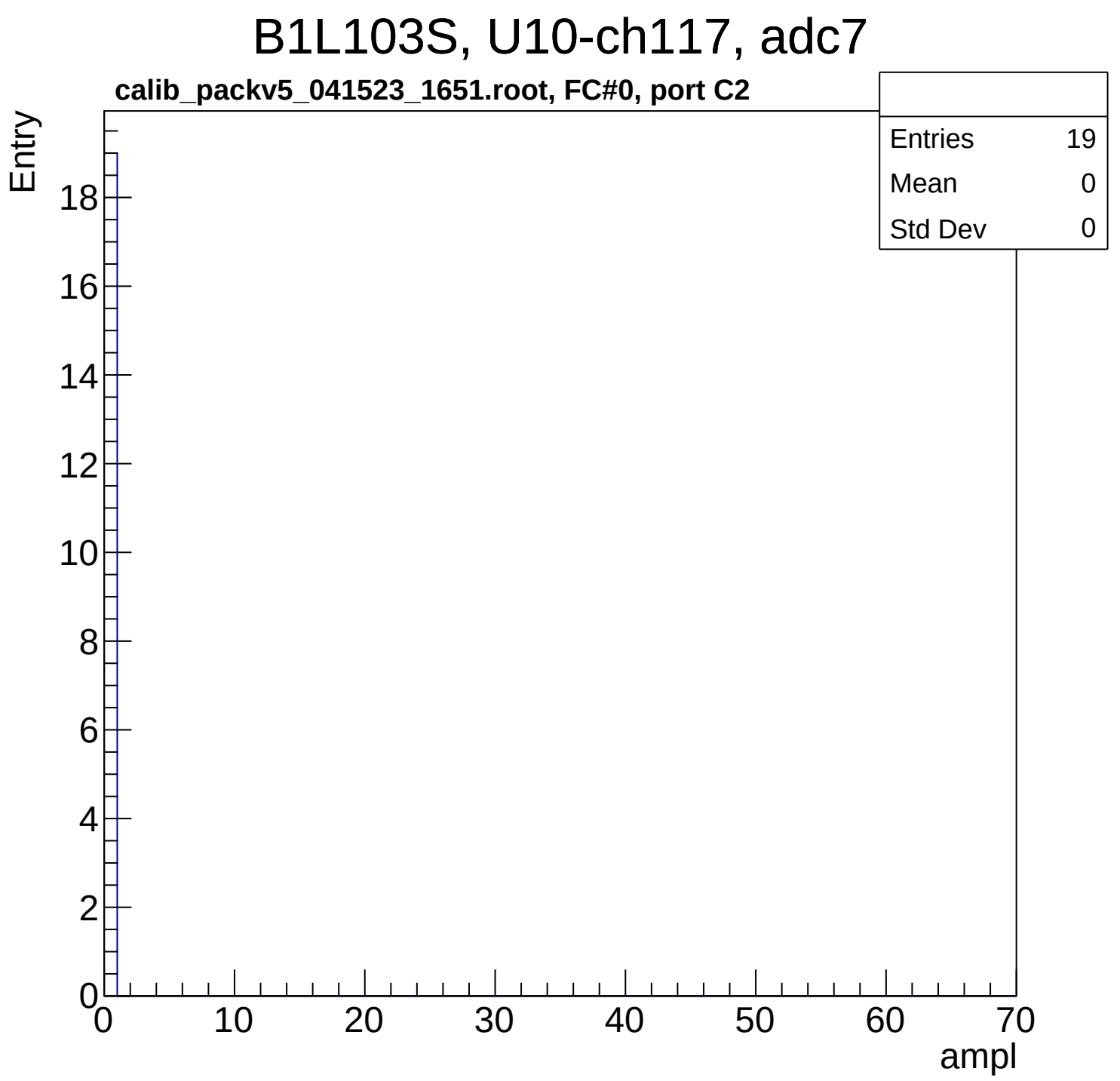
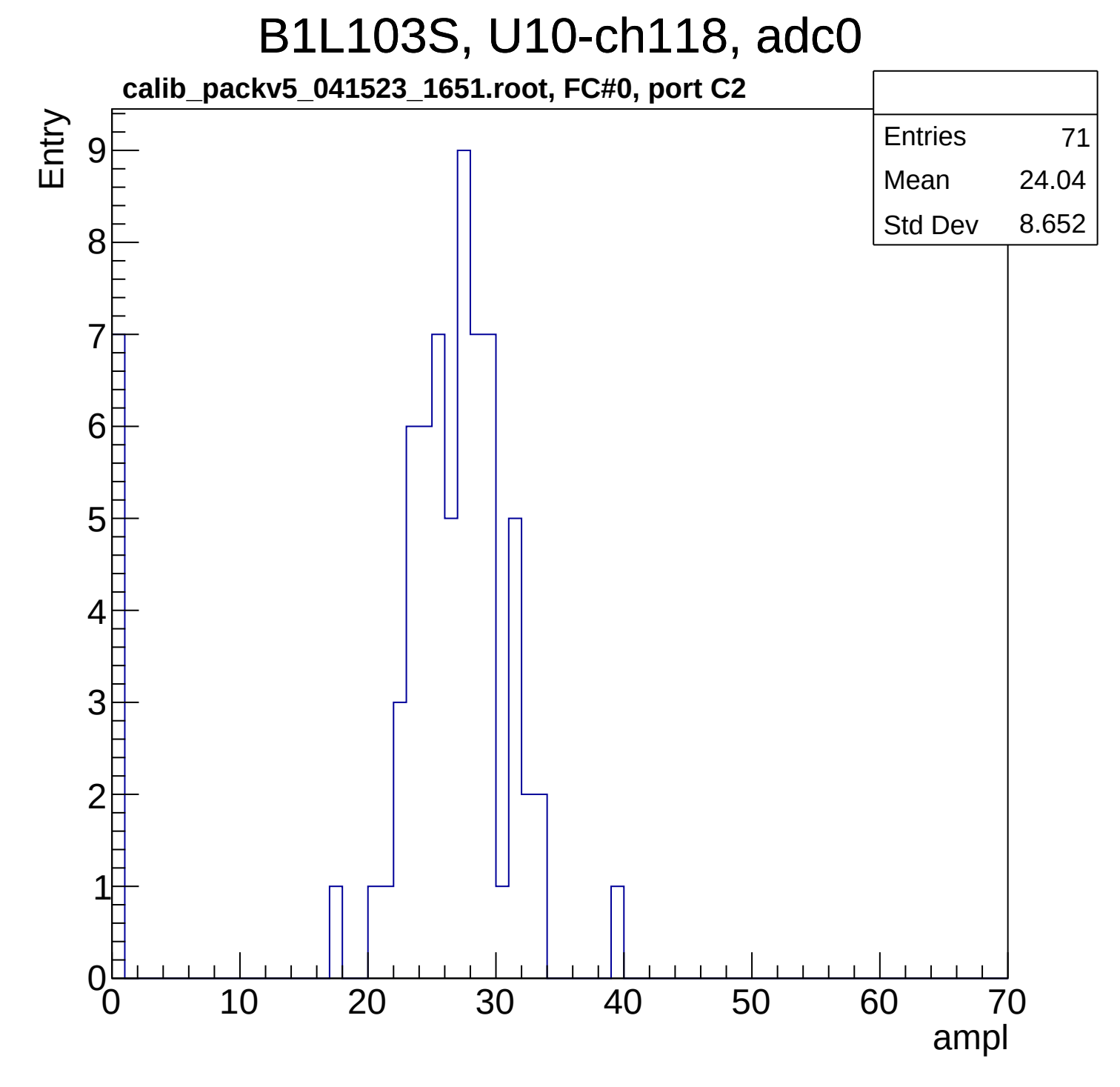
20
30
40
50
60
70


B1L103S, U10-ch117, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 4
Mean 61.5
Std Dev 1.5
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U10-ch117, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch118, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 24.04
Std Dev 8.652
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
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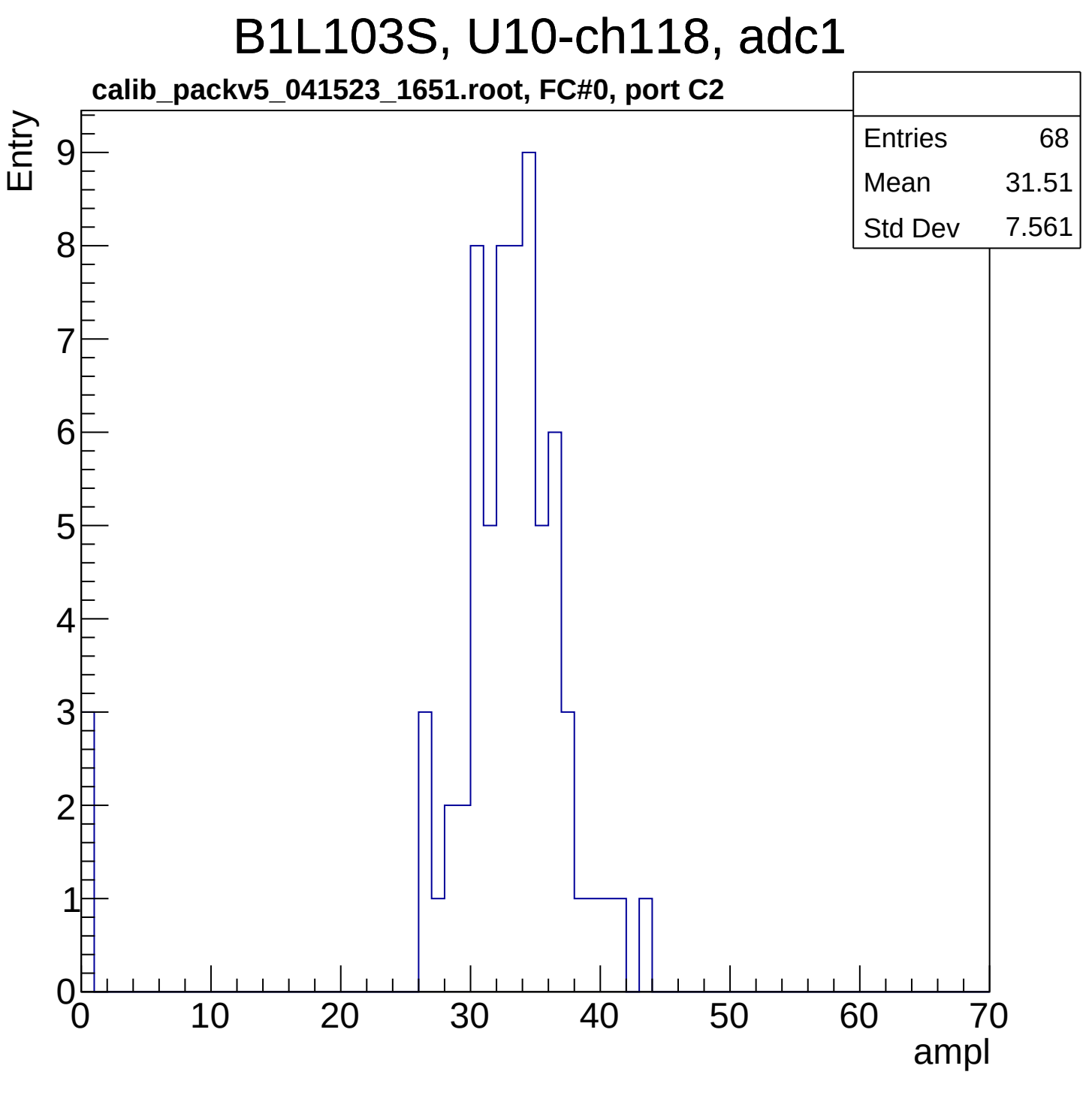
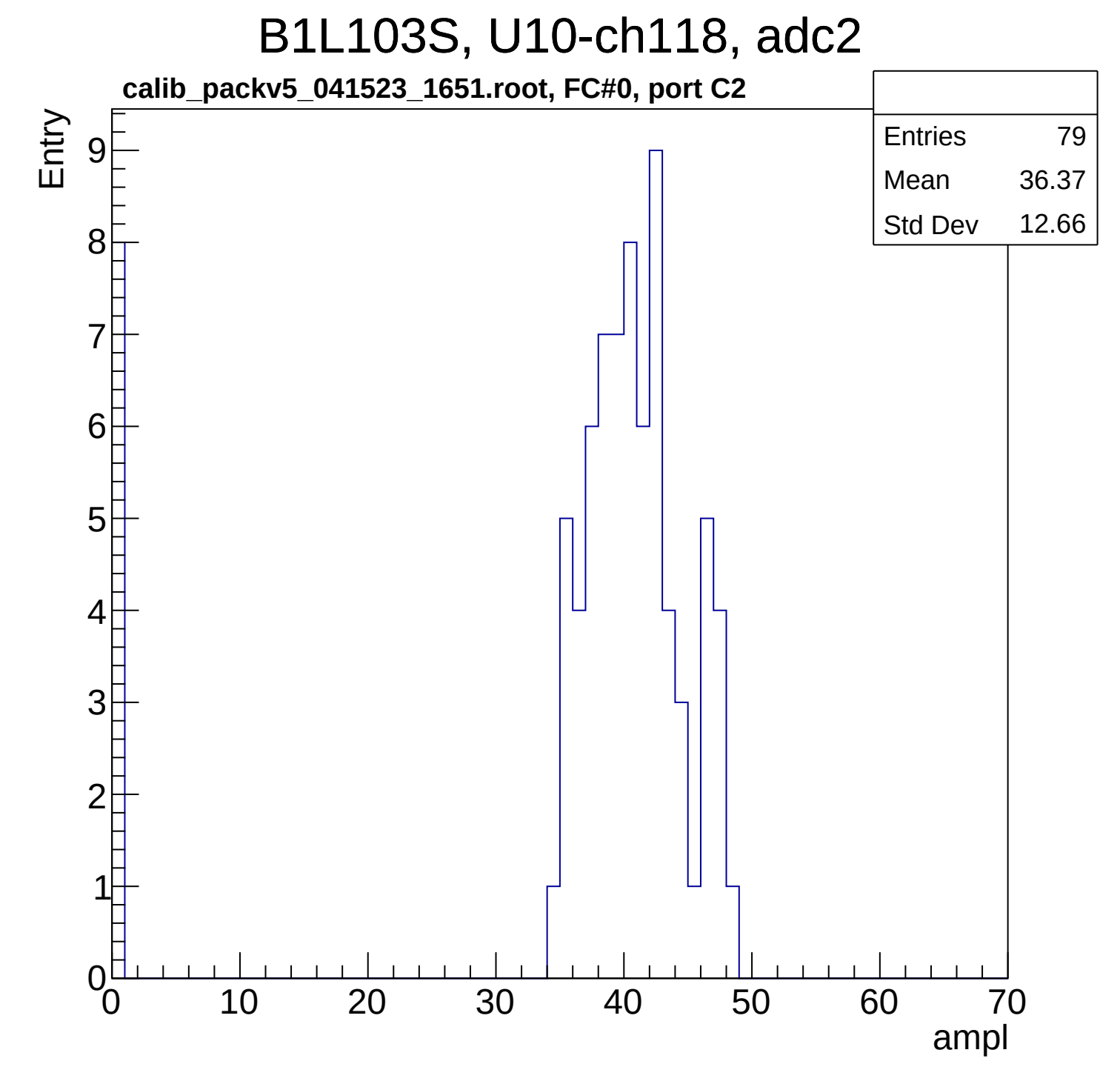
40
50
60
70


B1L103S, U10-ch118, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 31.51
Std Dev 7.561
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U10-ch118, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 36.37
Std Dev 12.66
Entry
ampl
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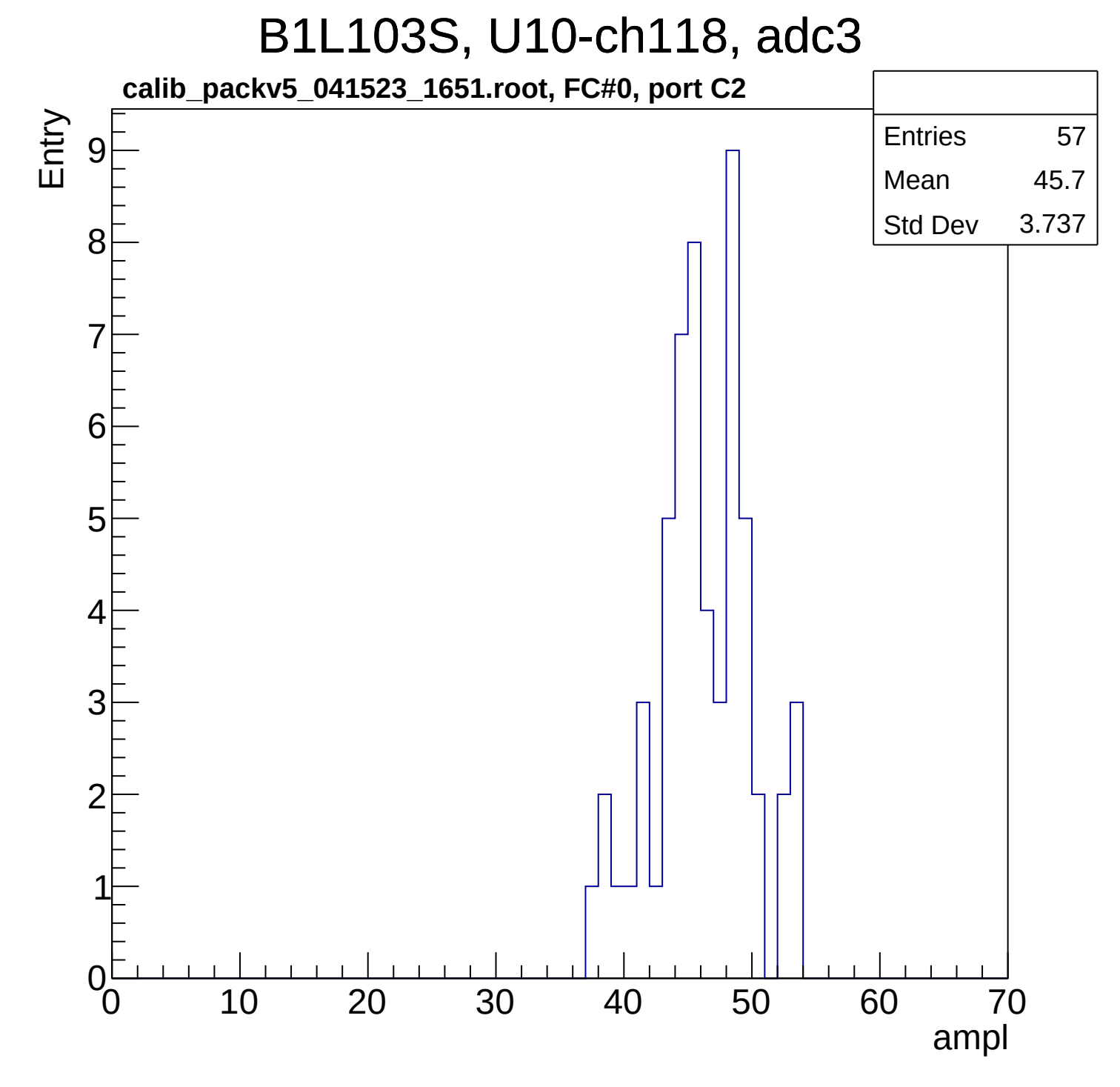
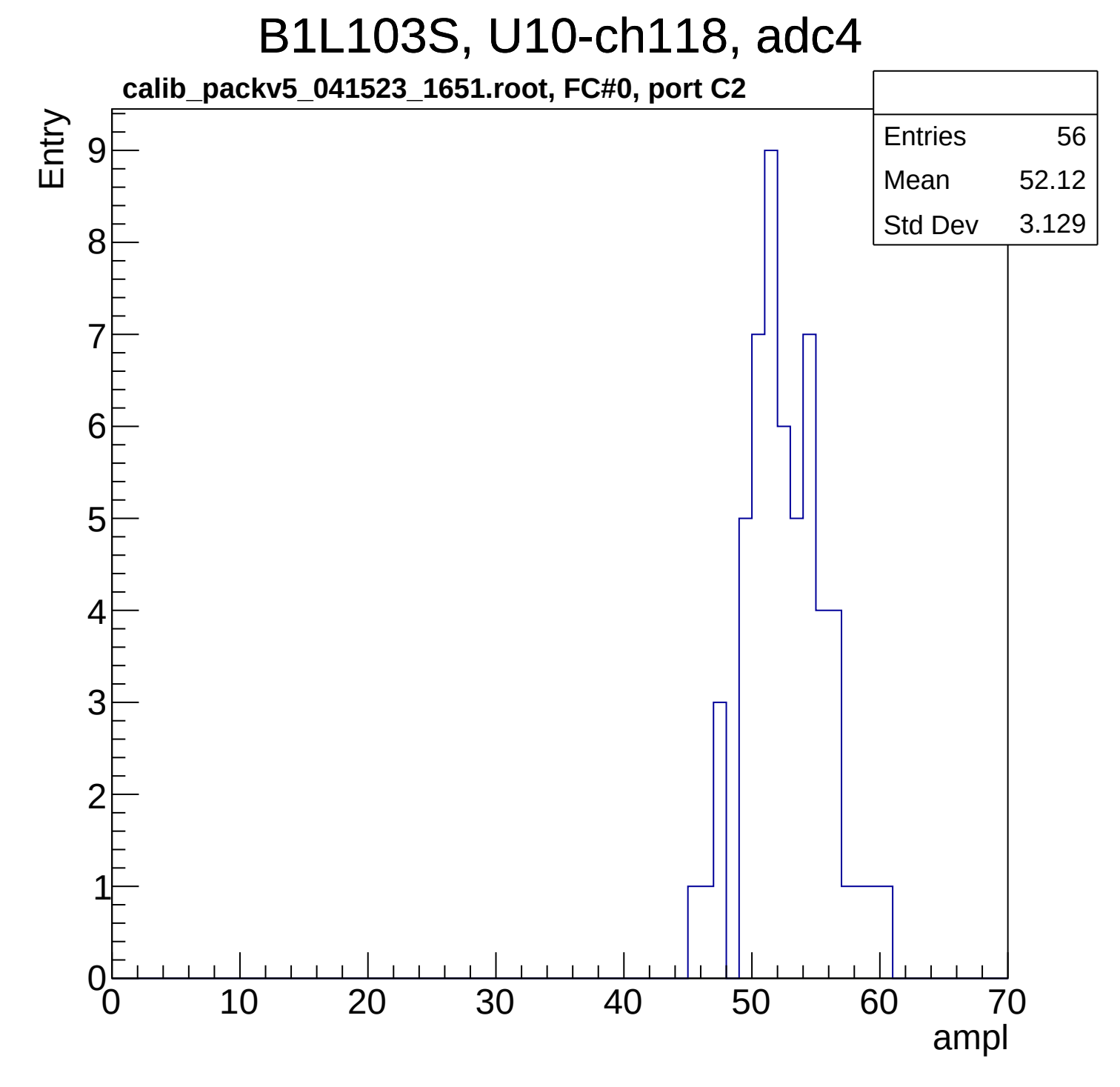
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U10-ch118, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 45.7
Std Dev 3.737
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U10-ch118, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 52.12
Std Dev 3.129
Entry
ampl
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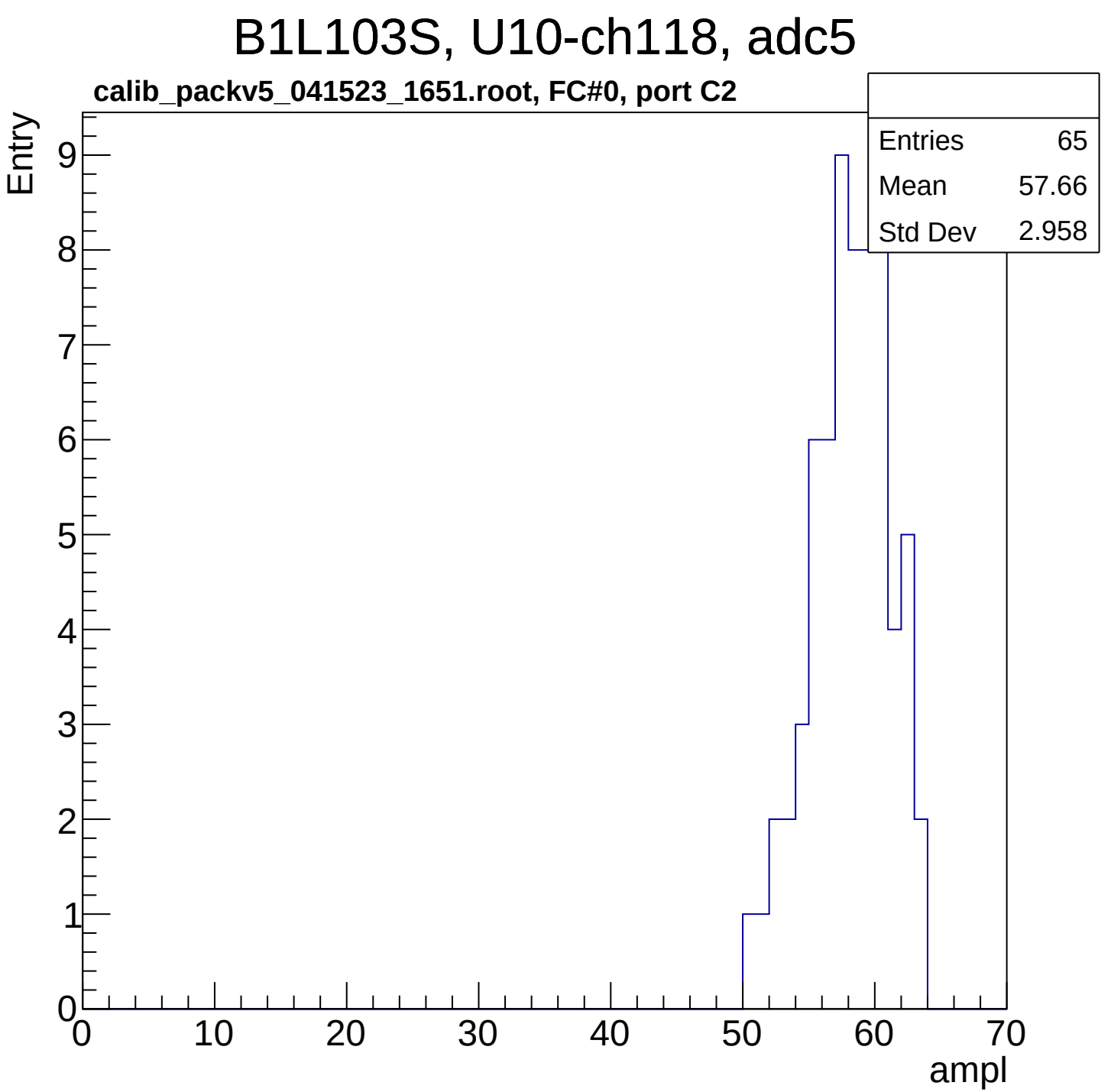
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U10-ch118, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 57.66
Std Dev 2.958
Entry
ampl
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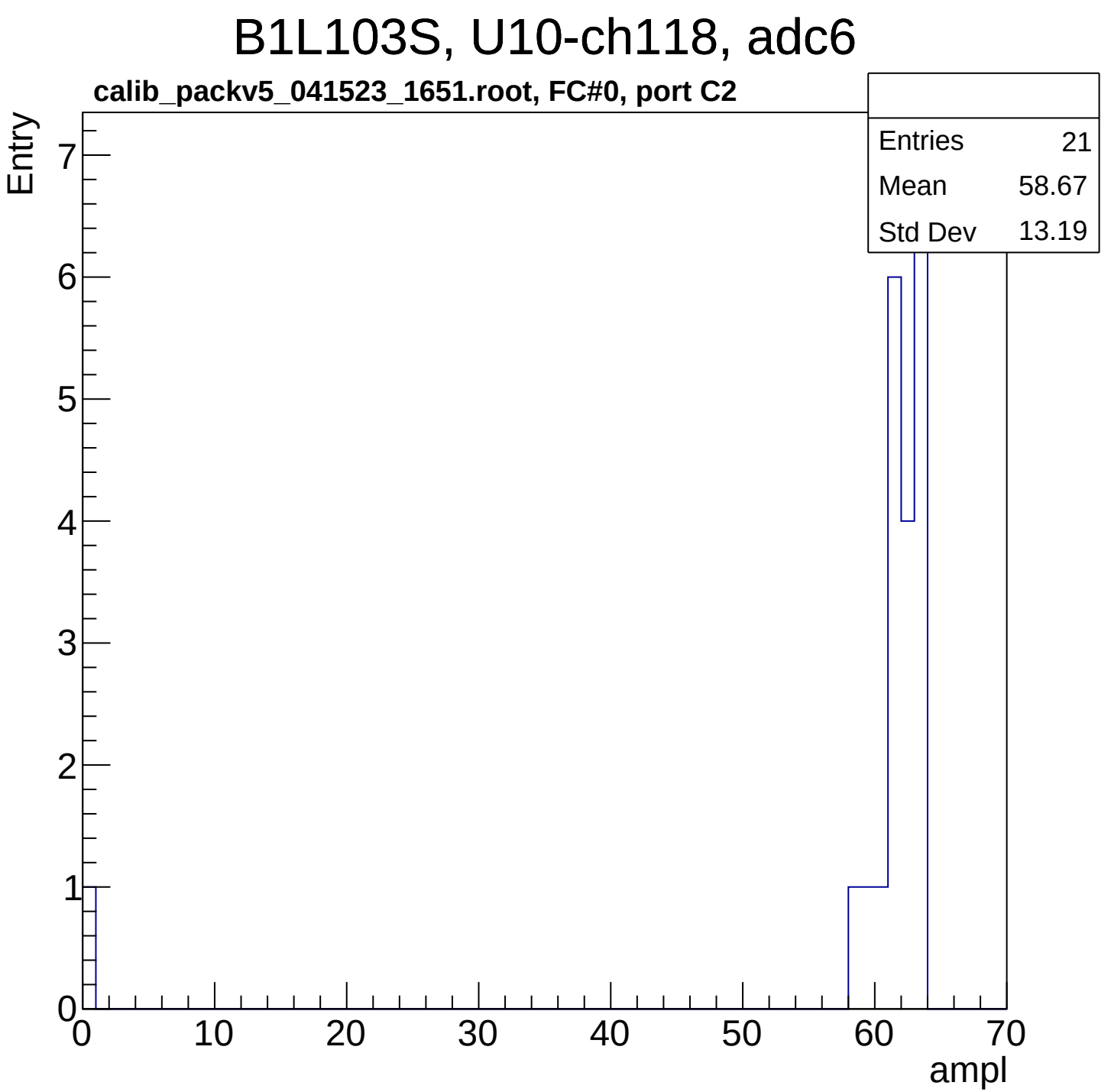
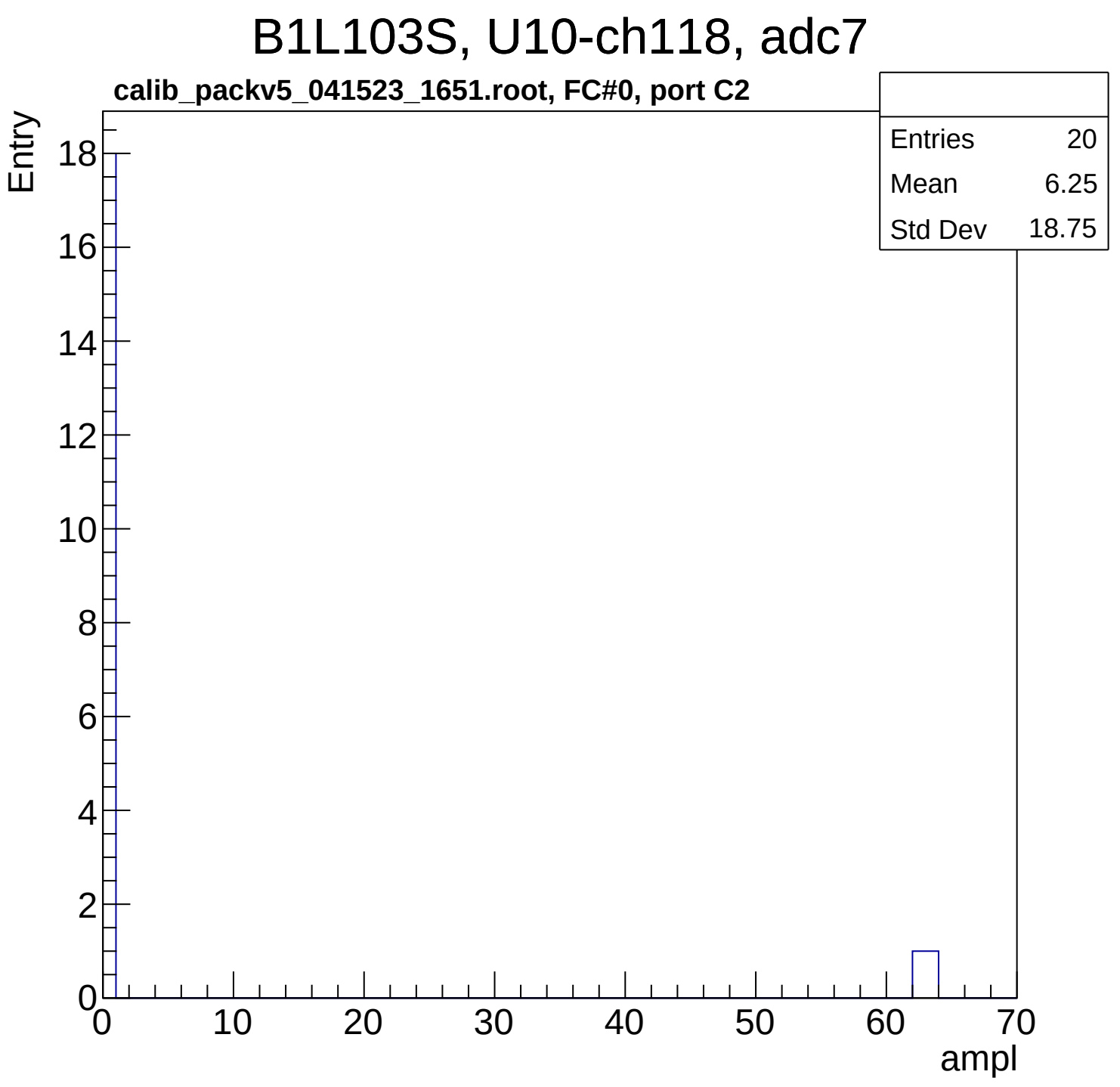
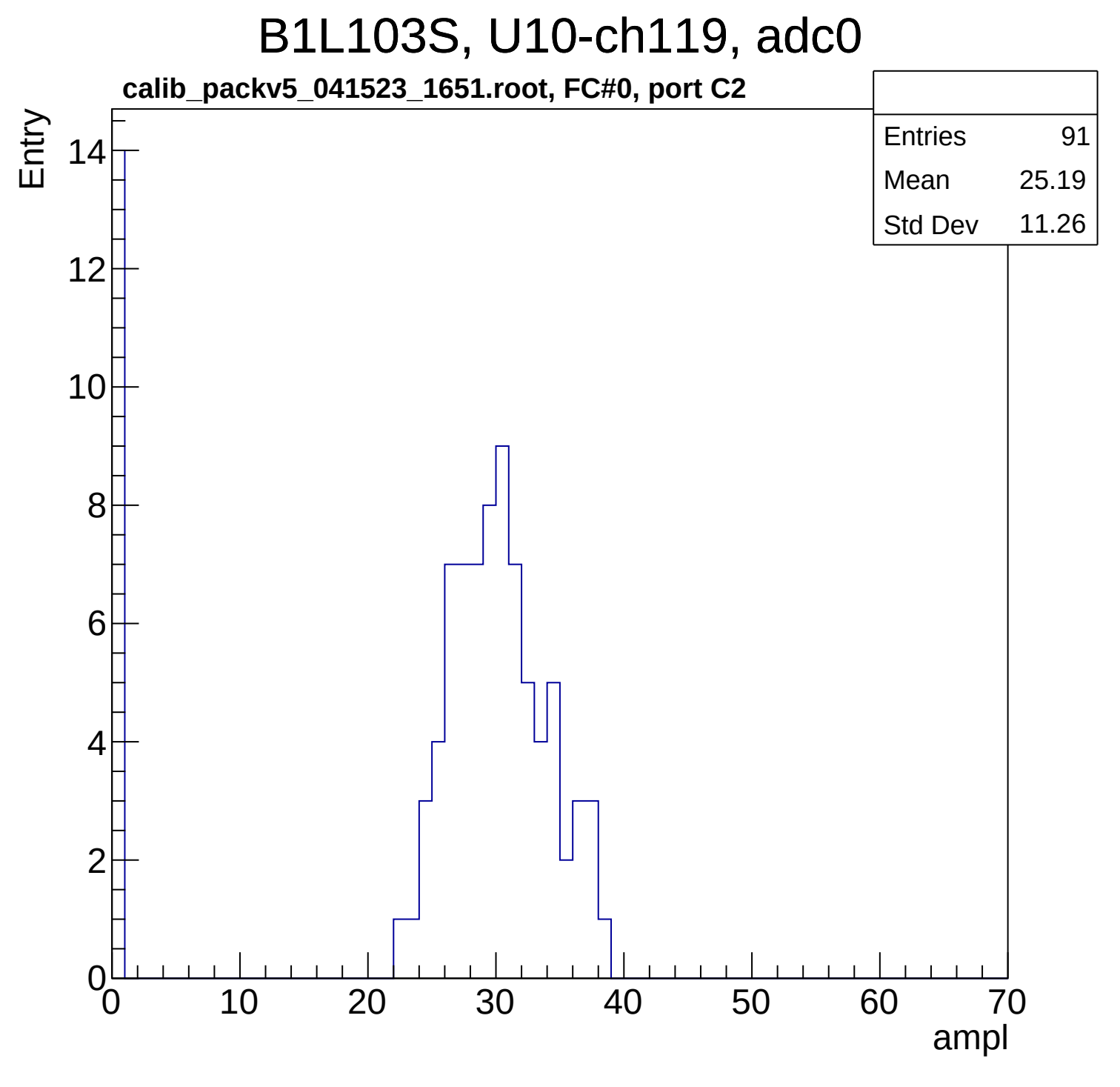
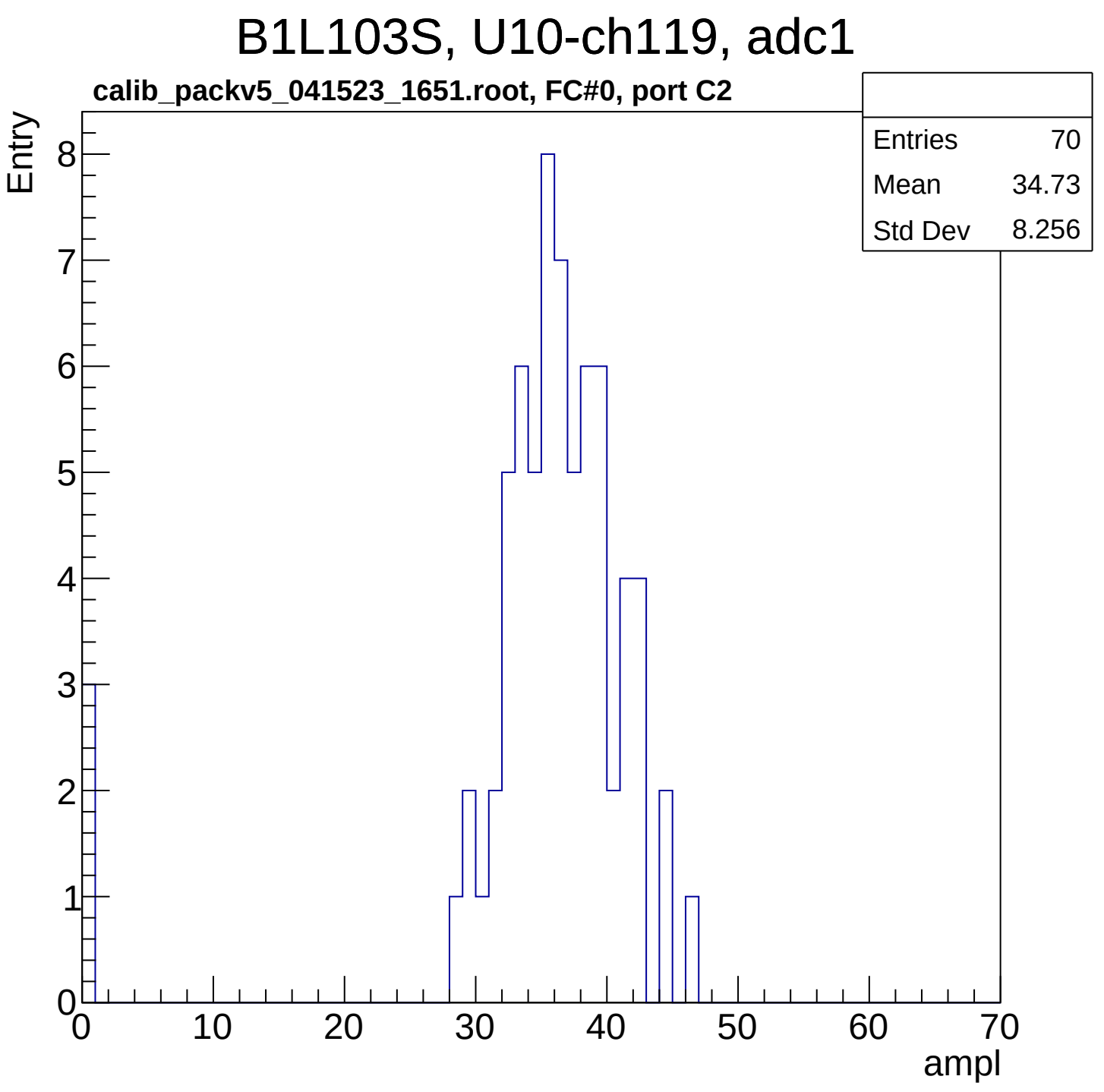
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U10-ch118, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 58.67
Std Dev 13.19
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U10-ch118, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 6.25
Std Dev 18.75
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch119, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 91
Mean 25.19
Std Dev 11.26
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L103S, U10-ch119, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 34.73
Std Dev 8.256
Entry
ampl
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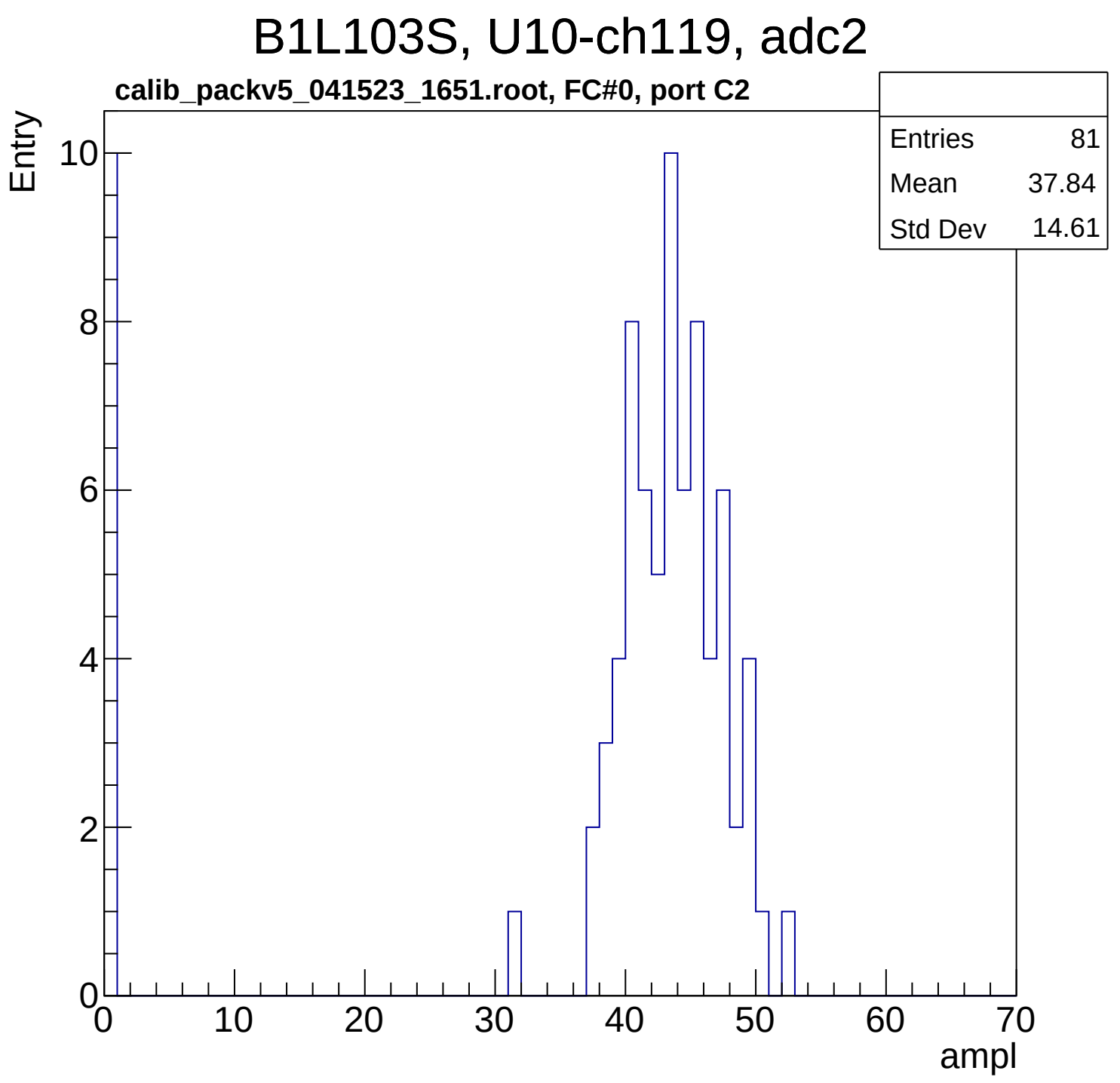
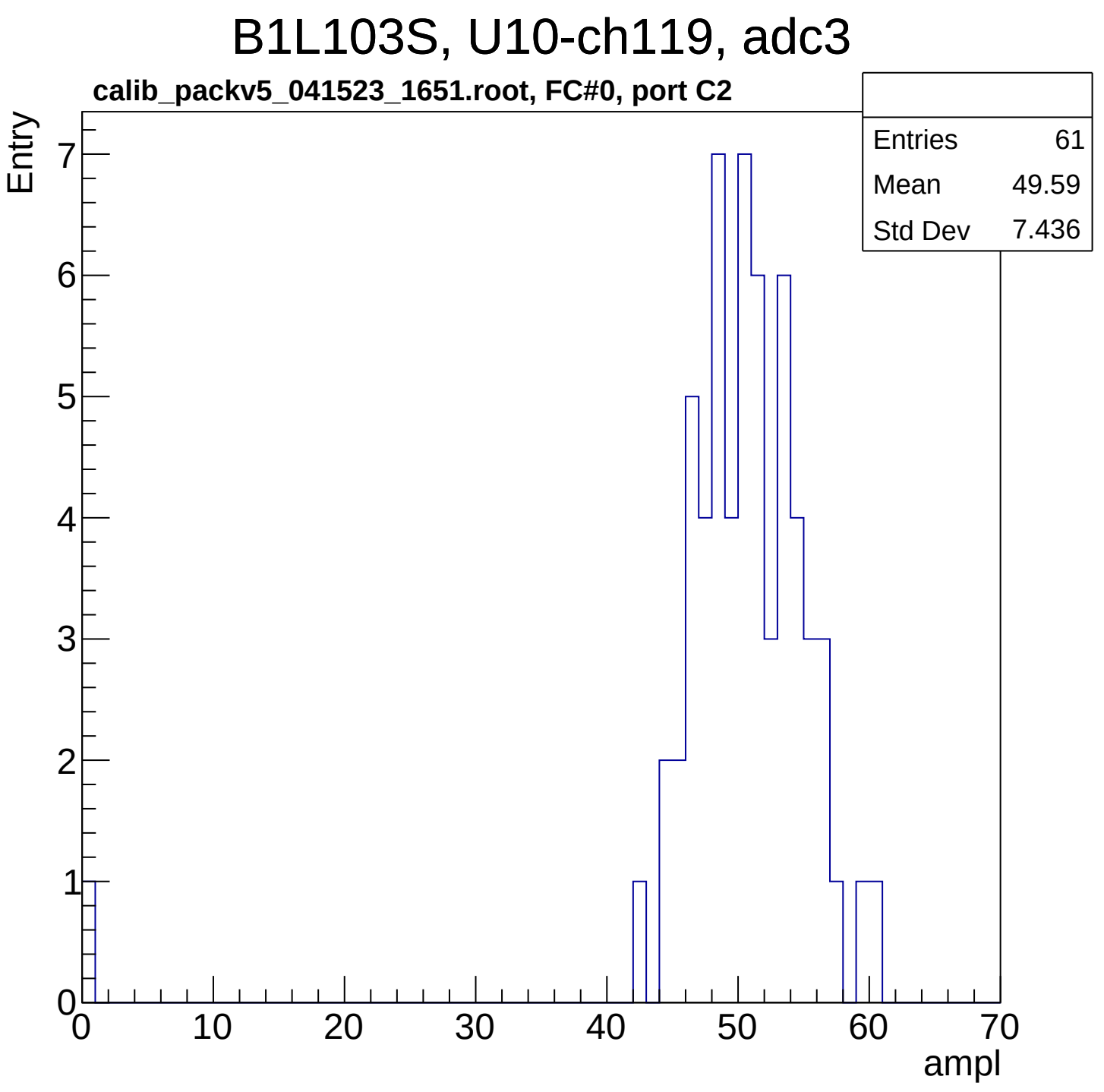
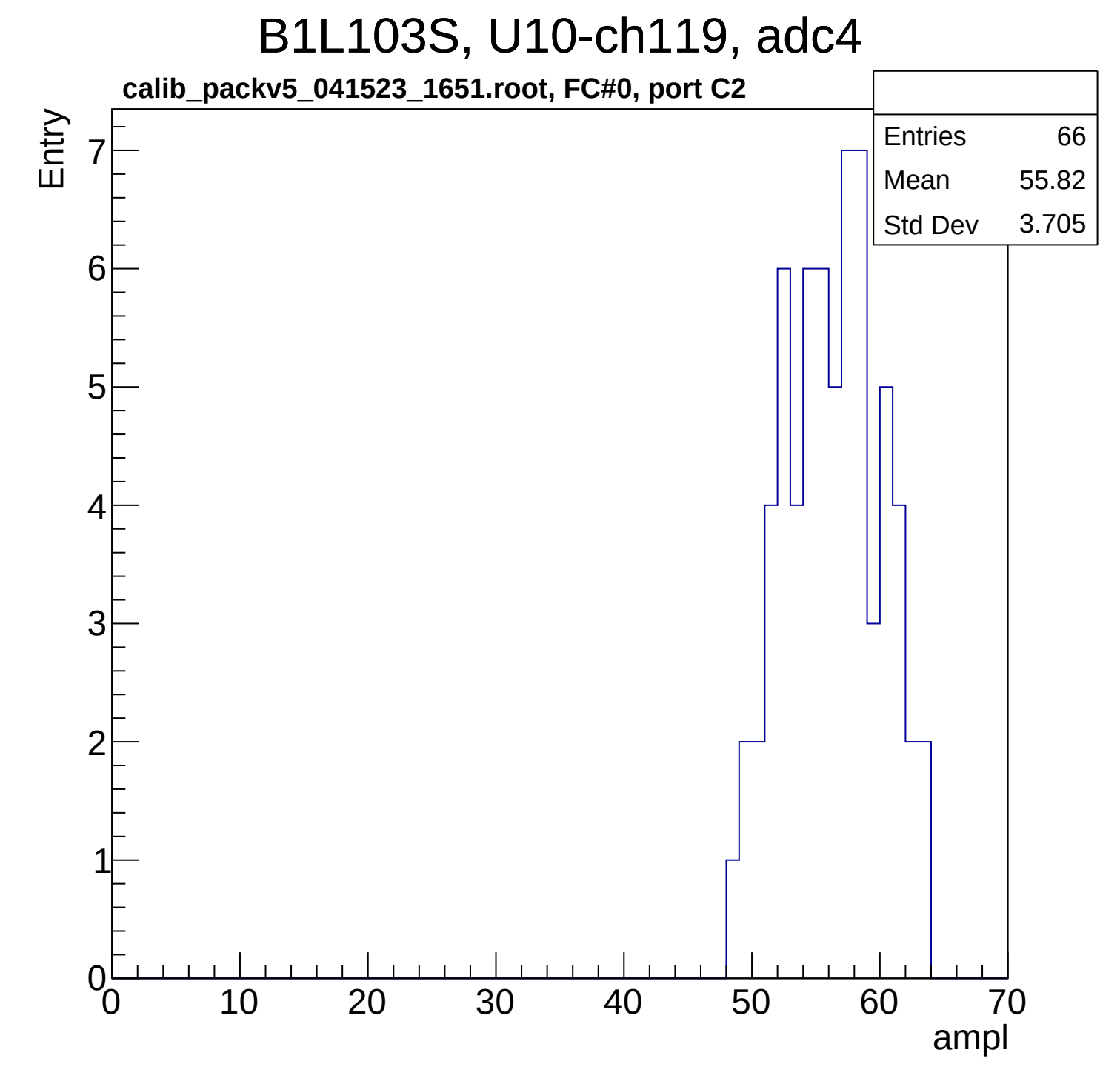
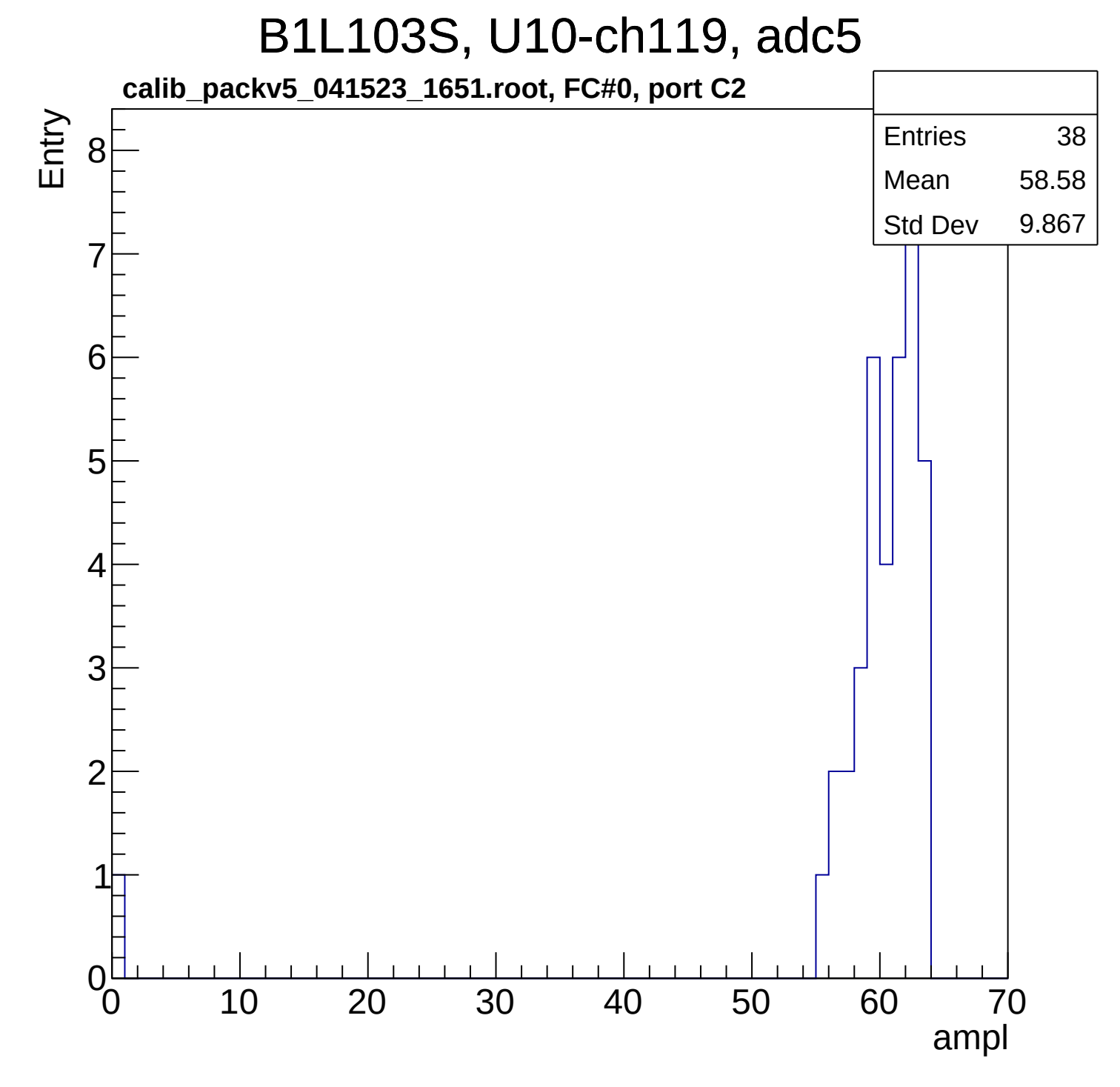
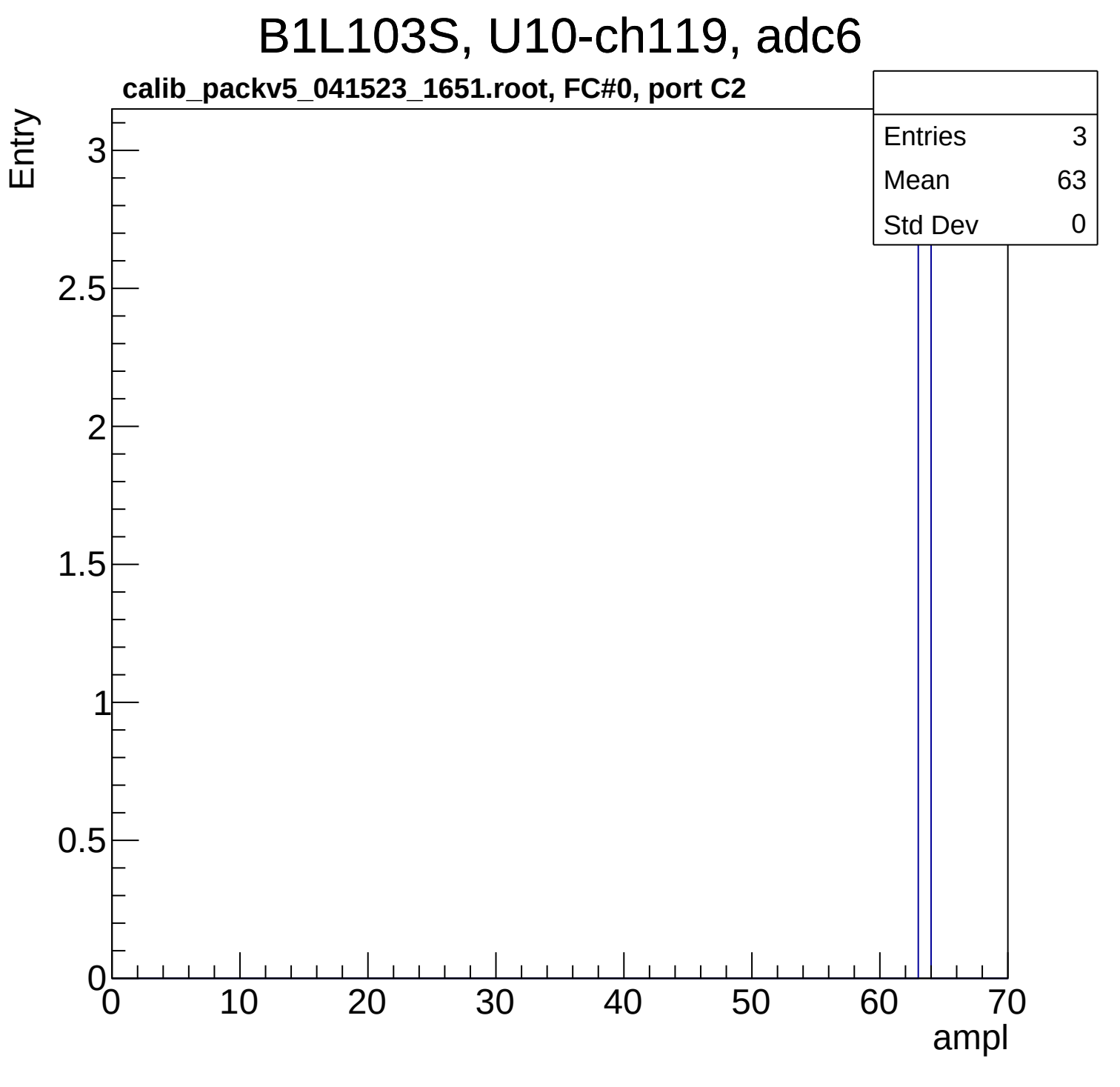
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U10-ch119, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 37.84
Std Dev 14.61
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U10-ch119, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 49.59
Std Dev 7.436
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U10-ch119, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 55.82
Std Dev 3.705
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U10-ch119, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 38
Mean 58.58
Std Dev 9.867
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U10-ch119, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 3
Mean 63
Std Dev 0
Entry
ampl
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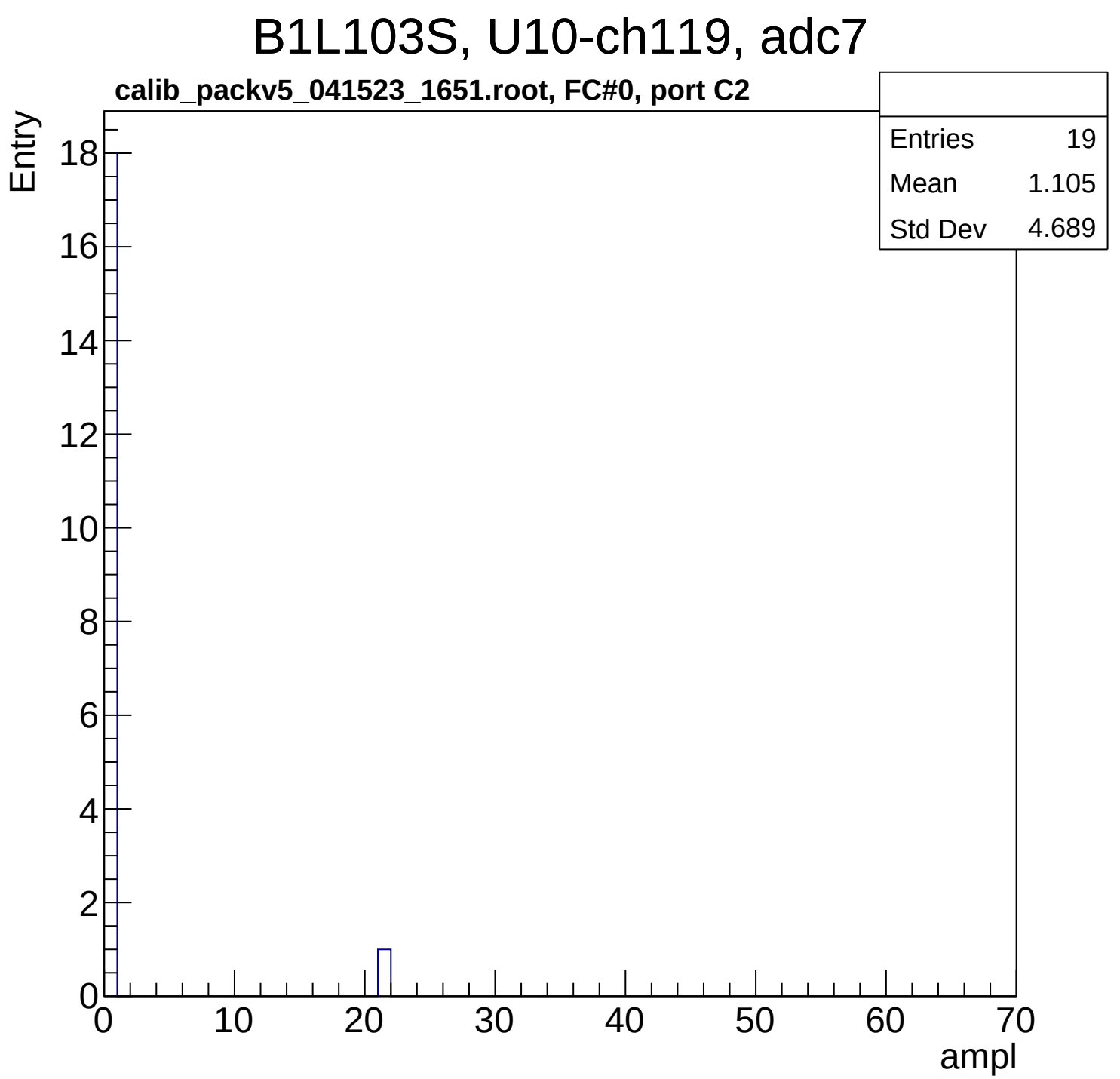
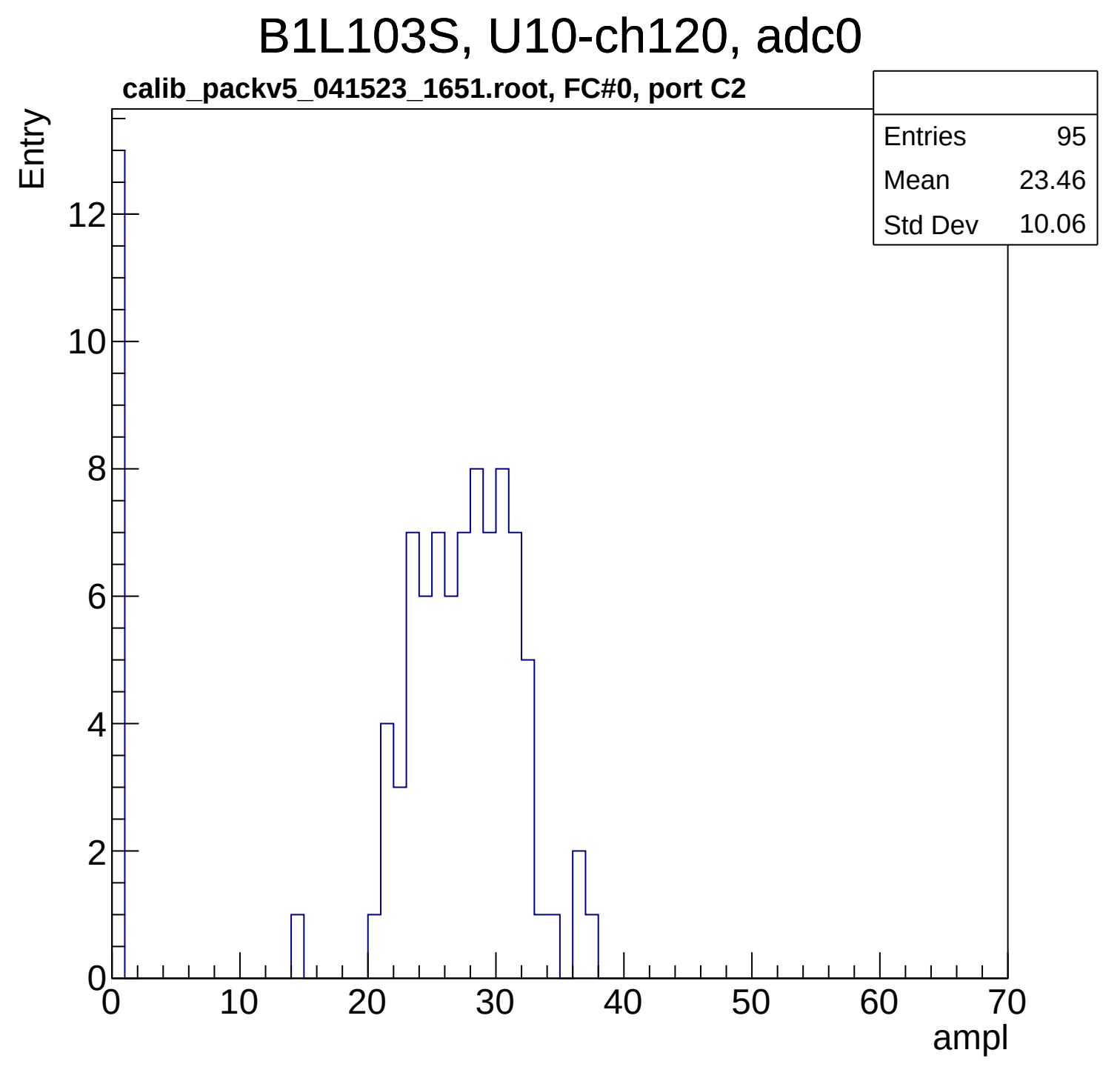
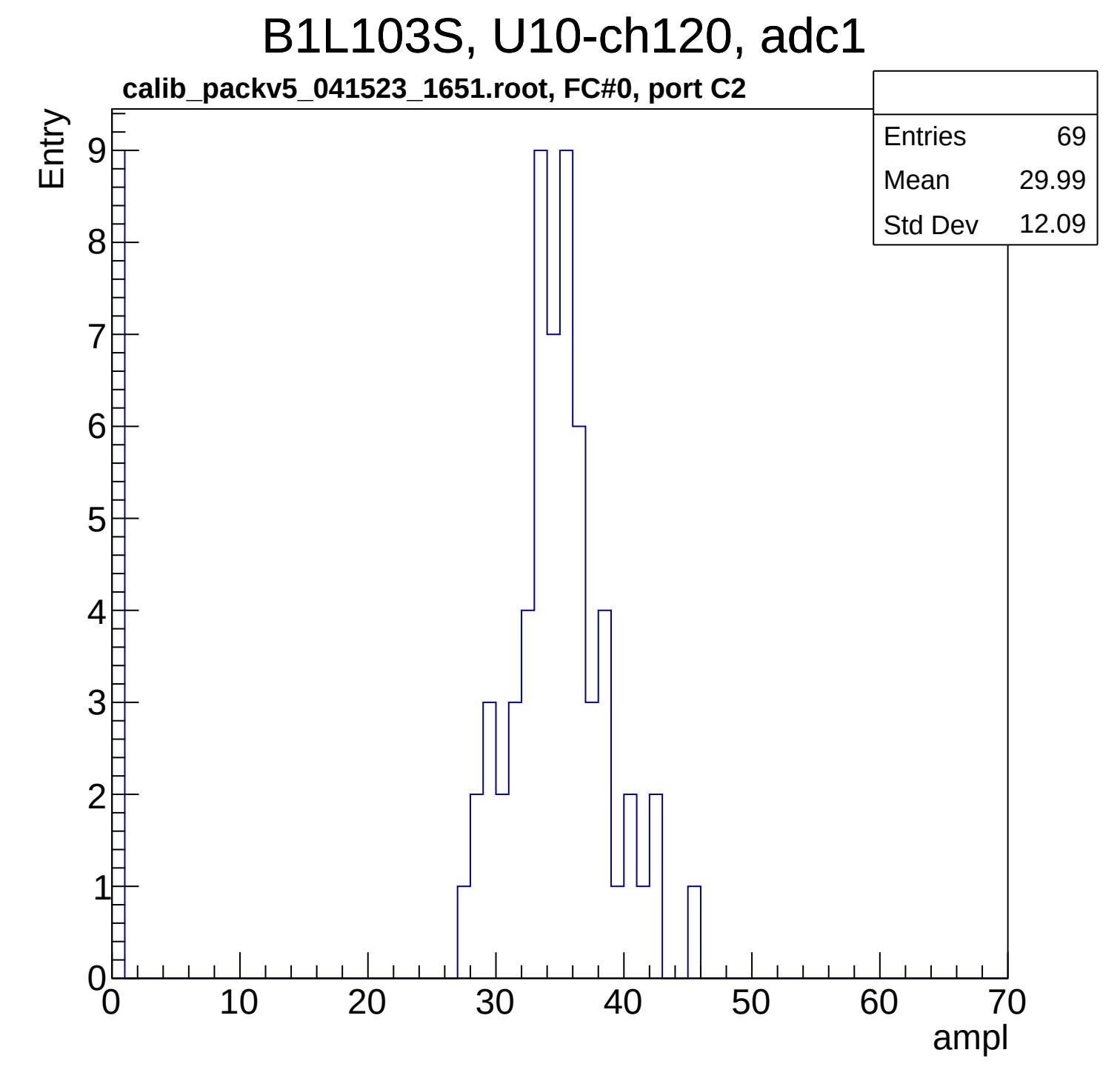
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U10-ch119, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.105
Std Dev 4.689
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch120, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 95
Mean 23.46
Std Dev 10.06
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch120, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 29.99
Std Dev 12.09
Entry
ampl
0
1
2
3
4
5
6
7
8
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0
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60
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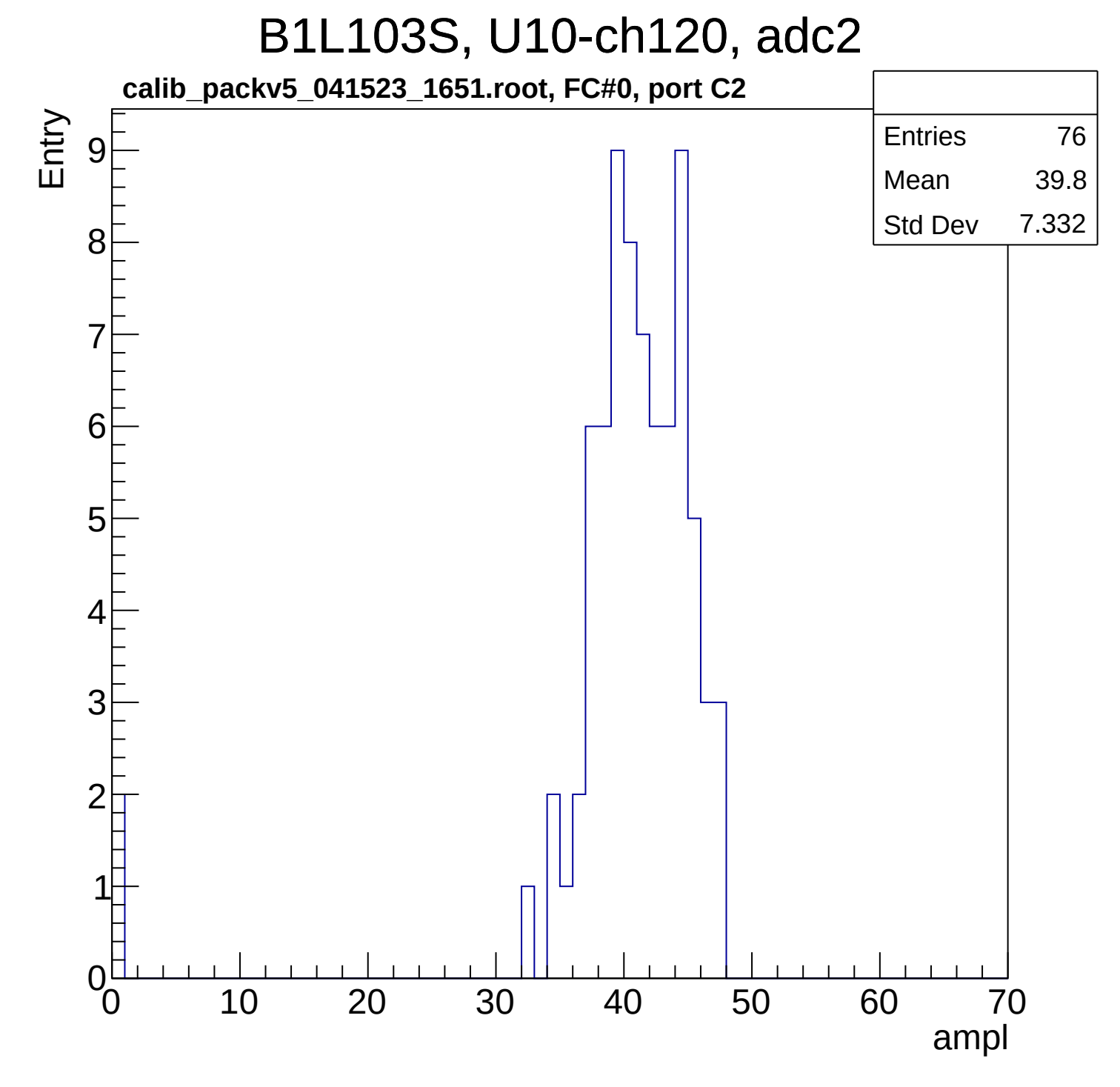
B1L103S, U10-ch120, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 39.8
Std Dev 7.332
Entry
ampl
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3
4
5
6
7
8
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0
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60
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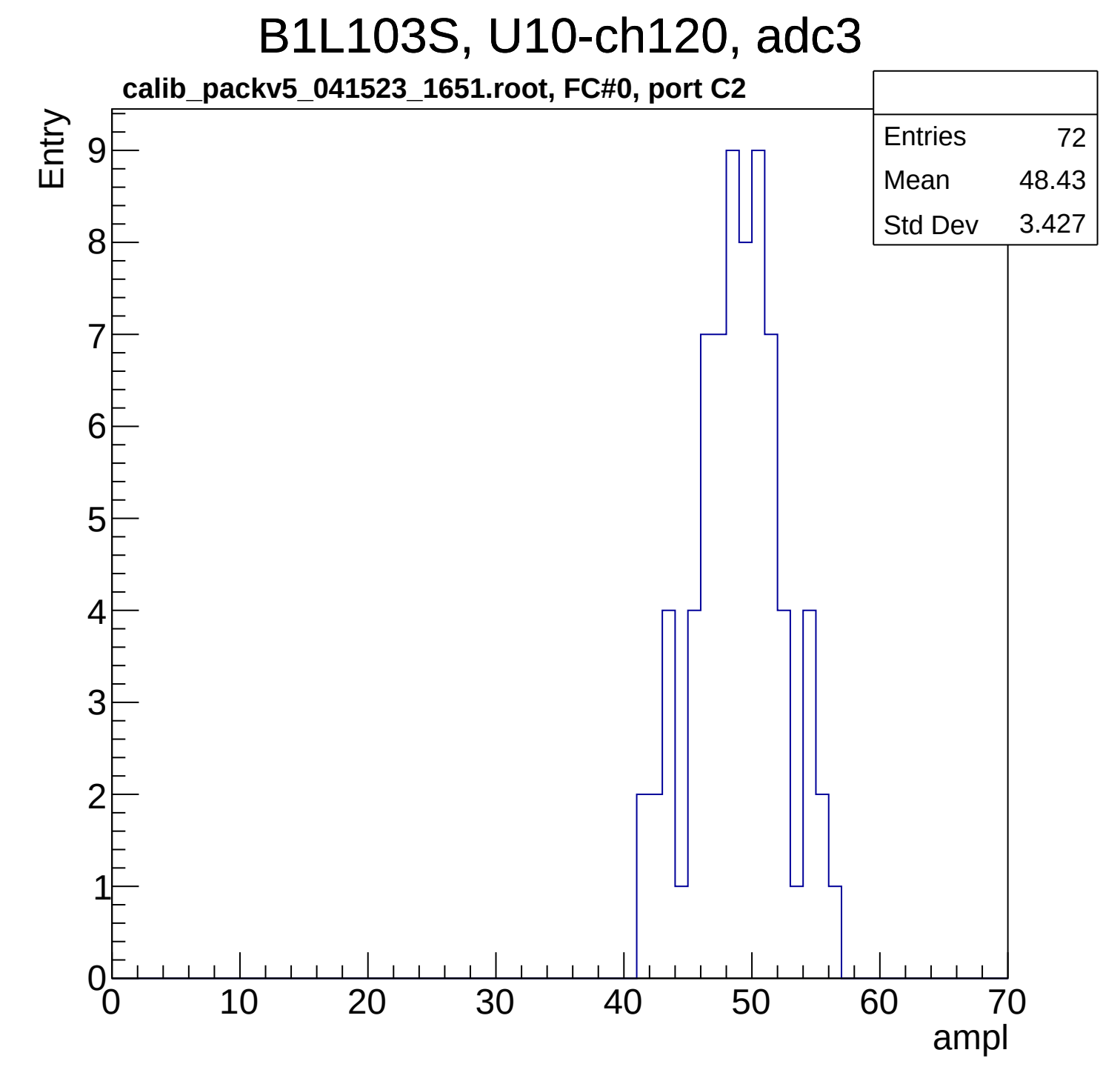
B1L103S, U10-ch120, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 48.43
Std Dev 3.427
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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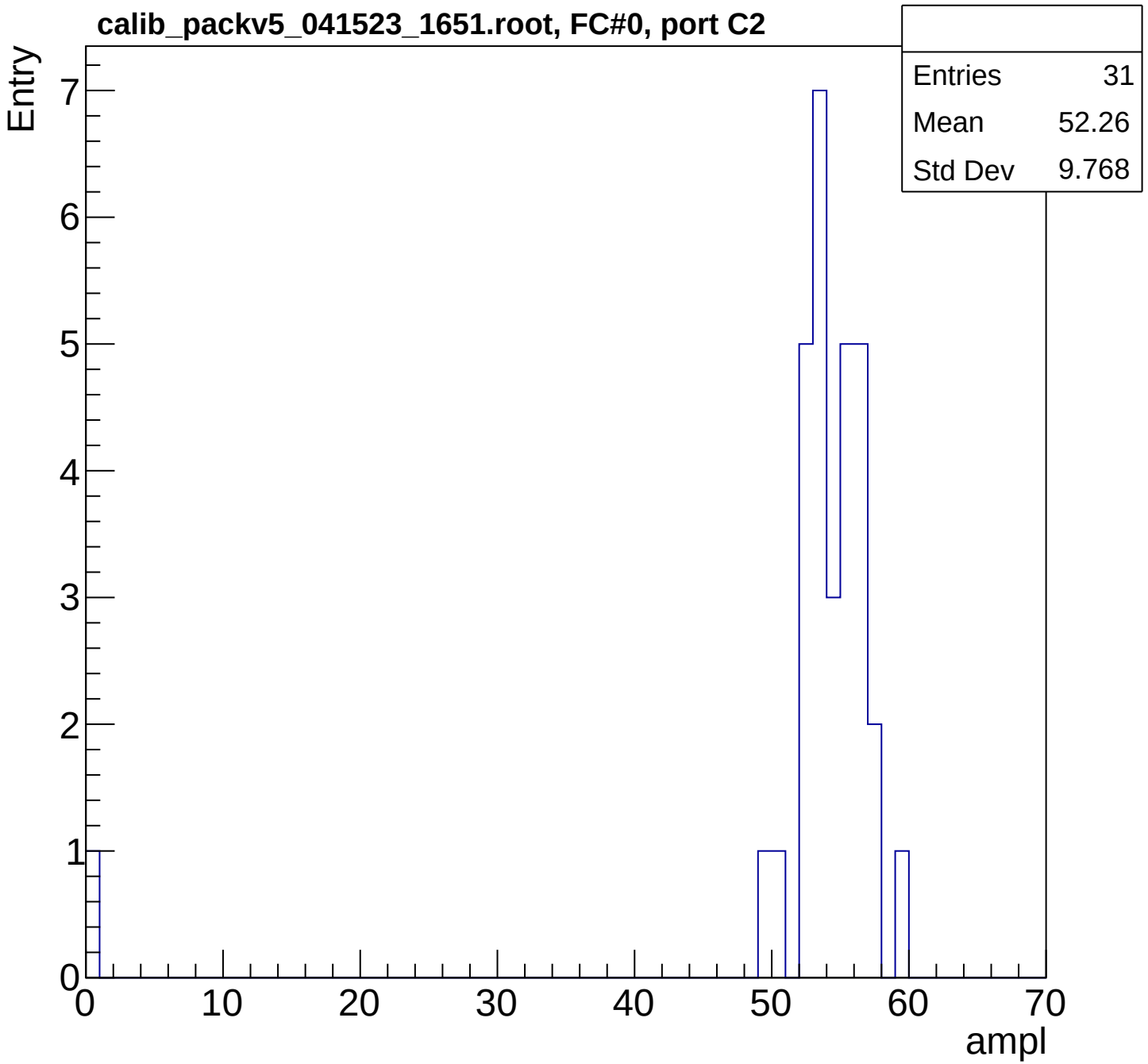
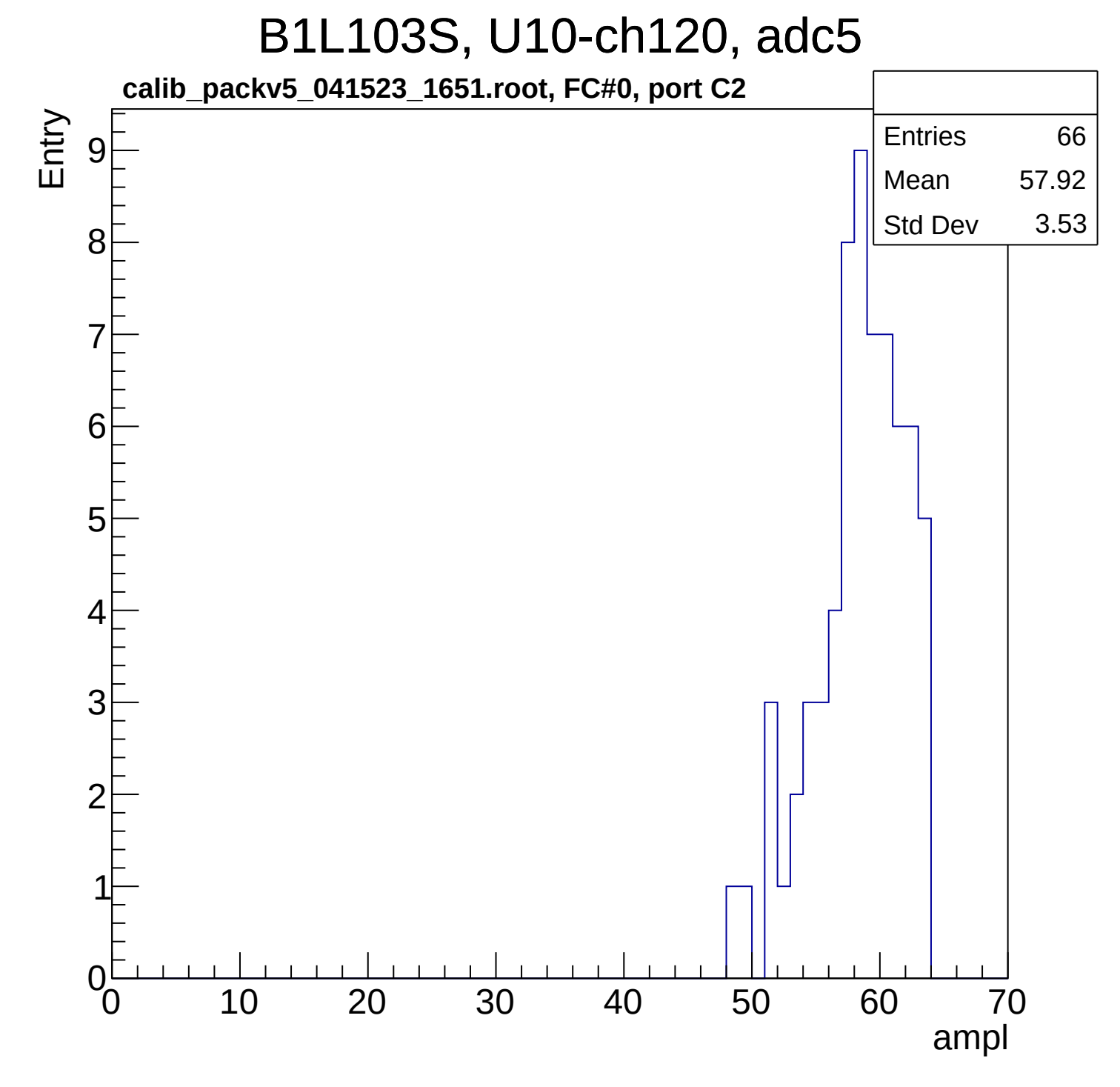
40
50
60
70


B1L103S, U10-ch120, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 31
Mean 52.26
Std Dev 9.768
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U10-ch120, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 57.92
Std Dev 3.53
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
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40
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60
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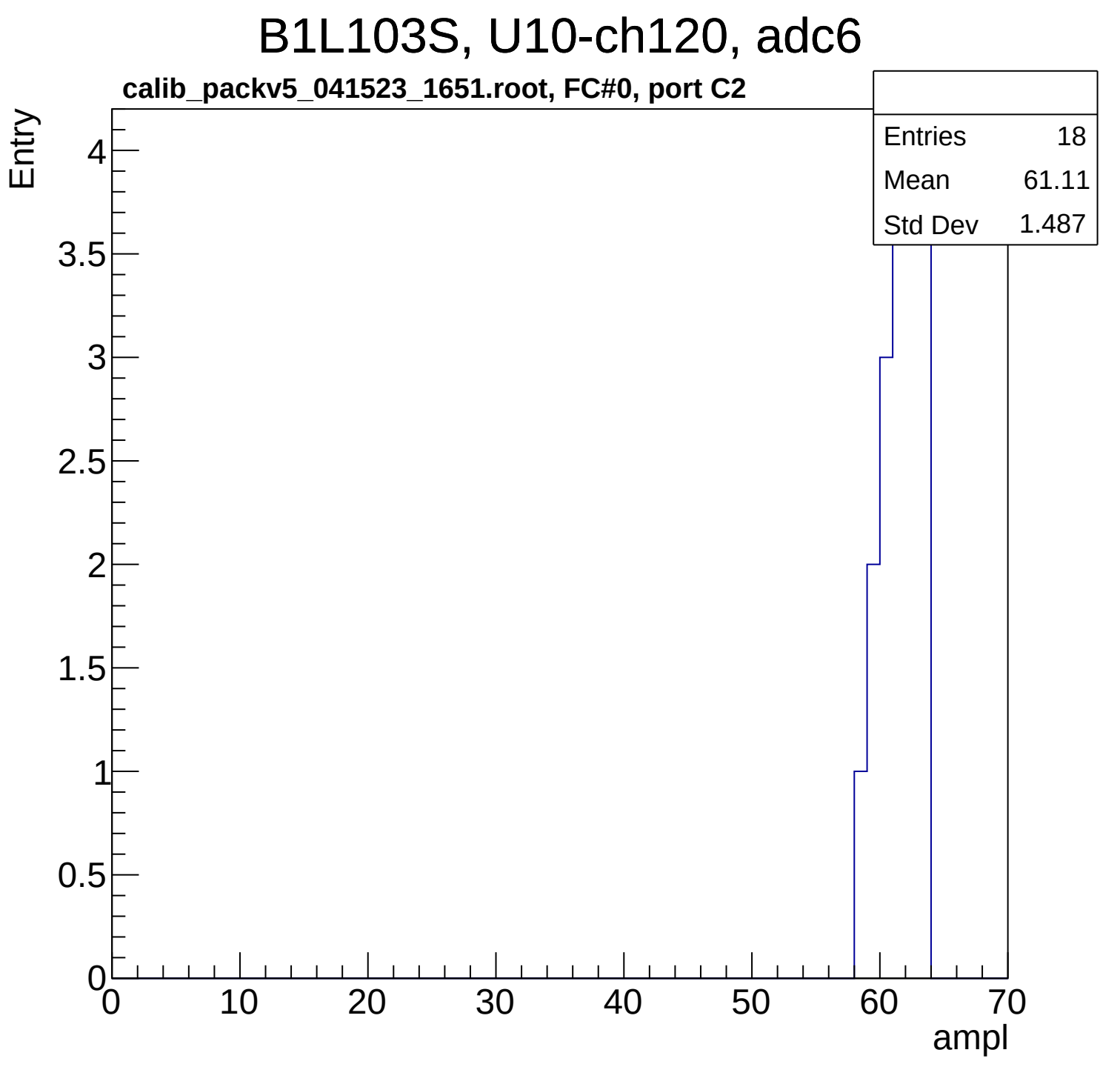
B1L103S, U10-ch120, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 61.11
Std Dev 1.487
Entry
ampl
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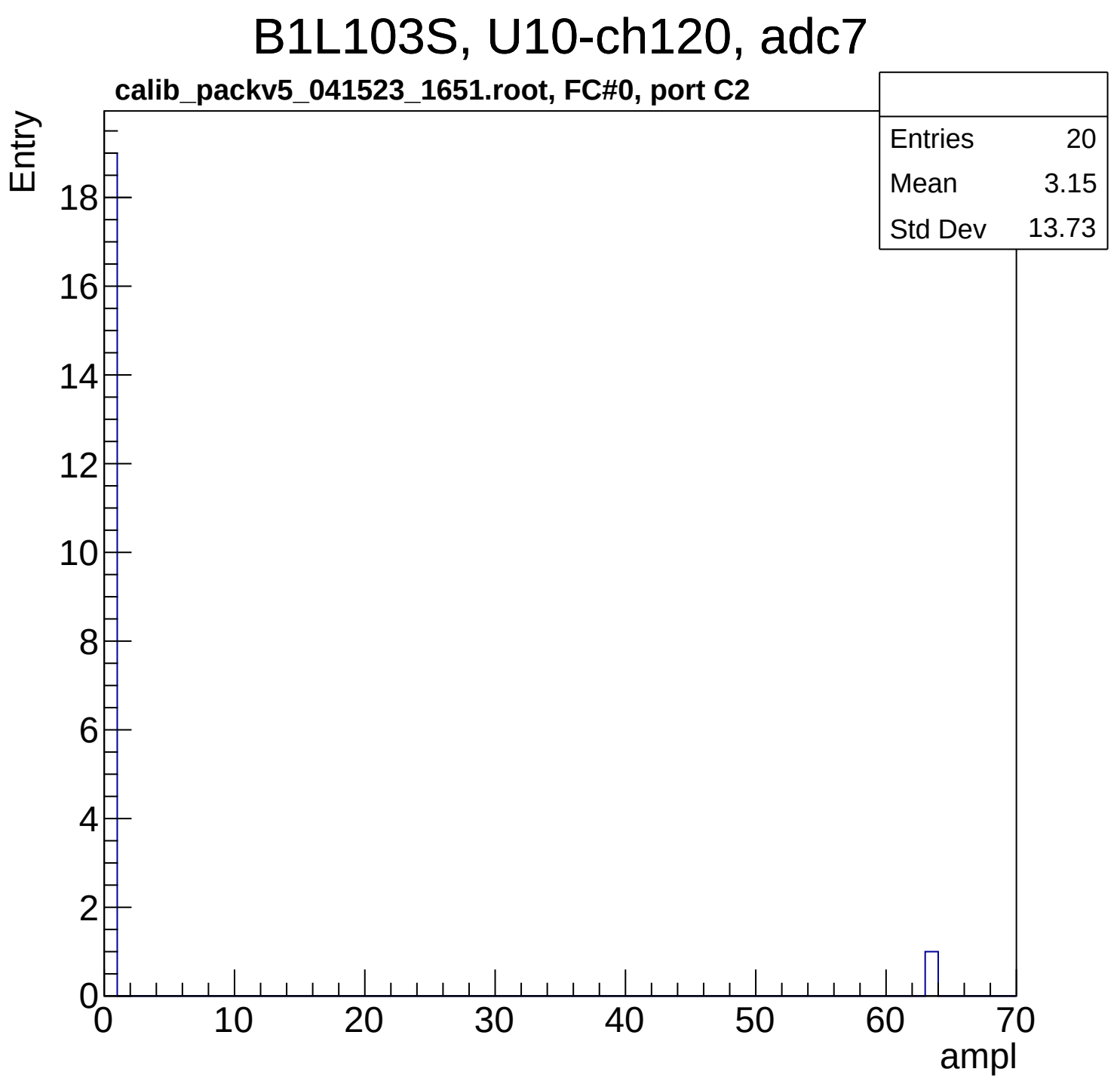
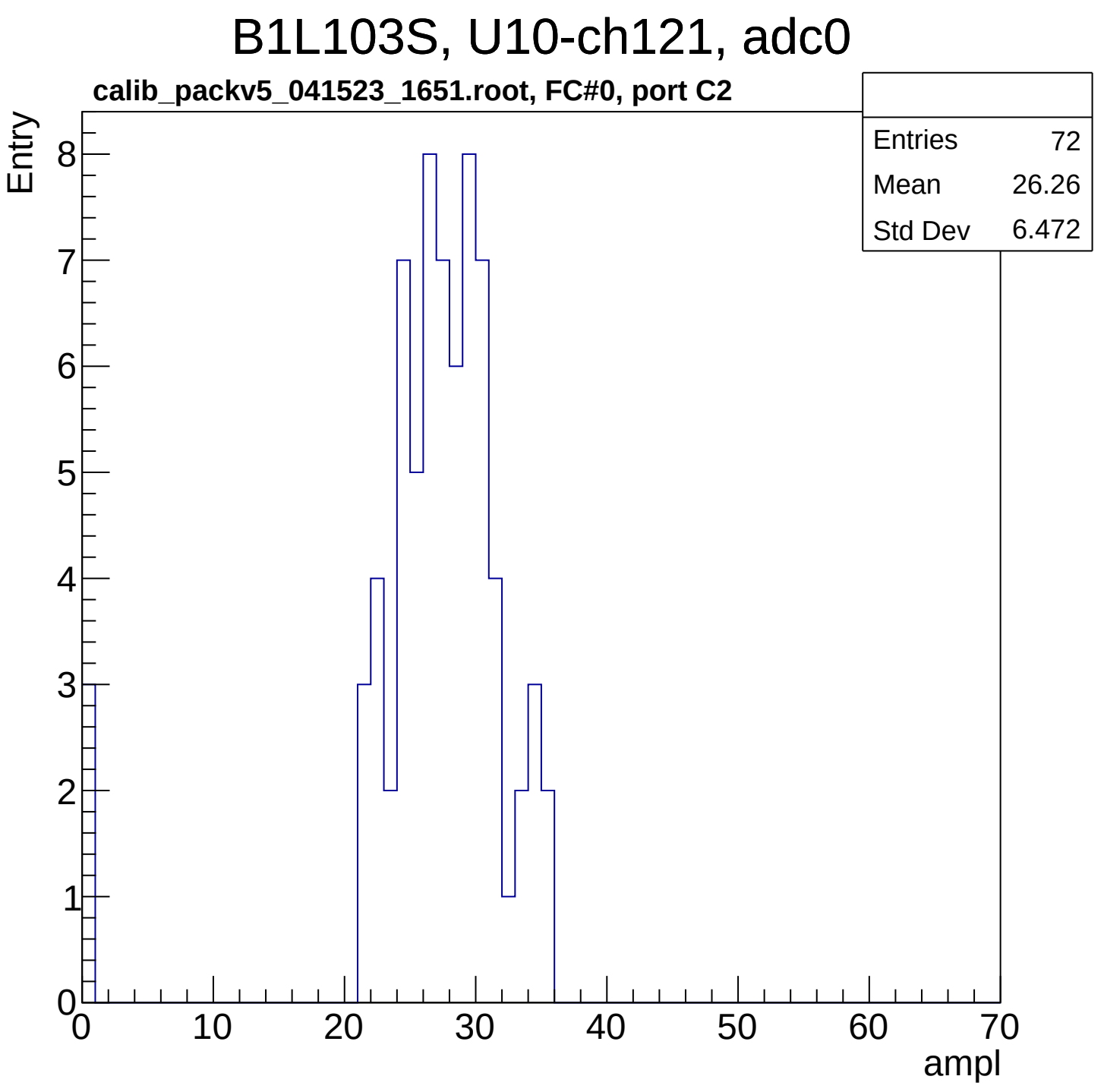
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U10-ch120, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch121, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 26.26
Std Dev 6.472
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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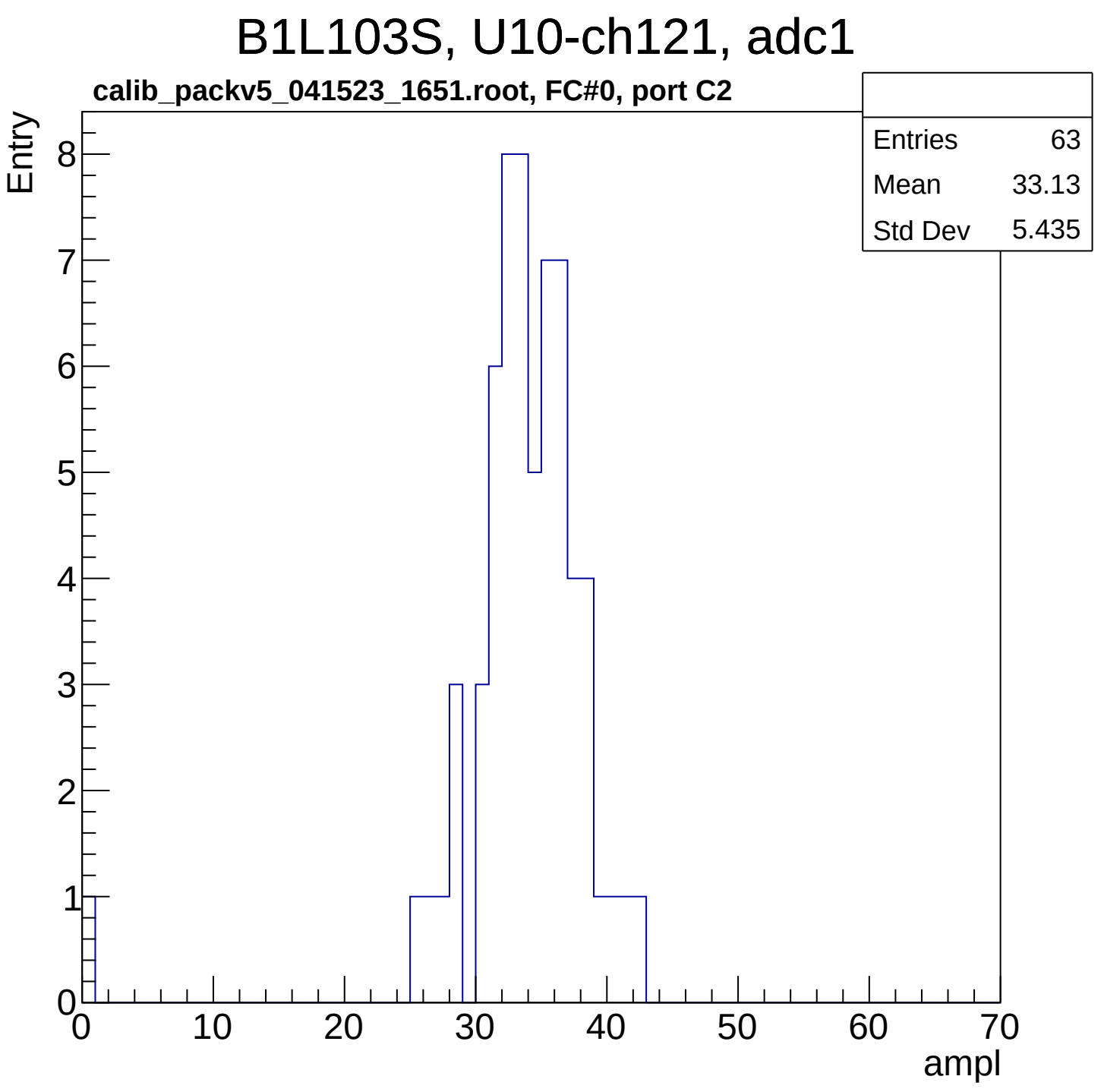
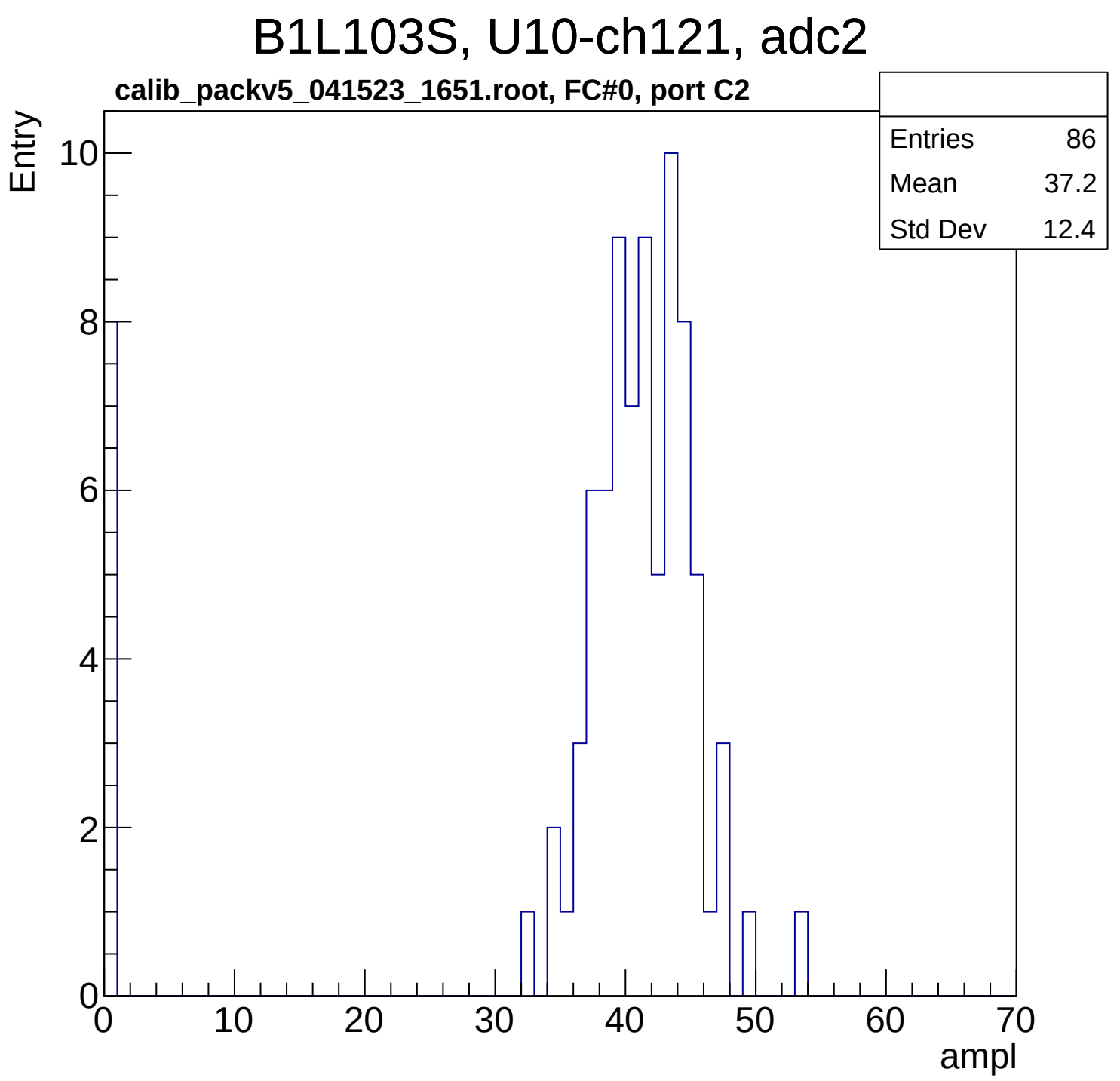
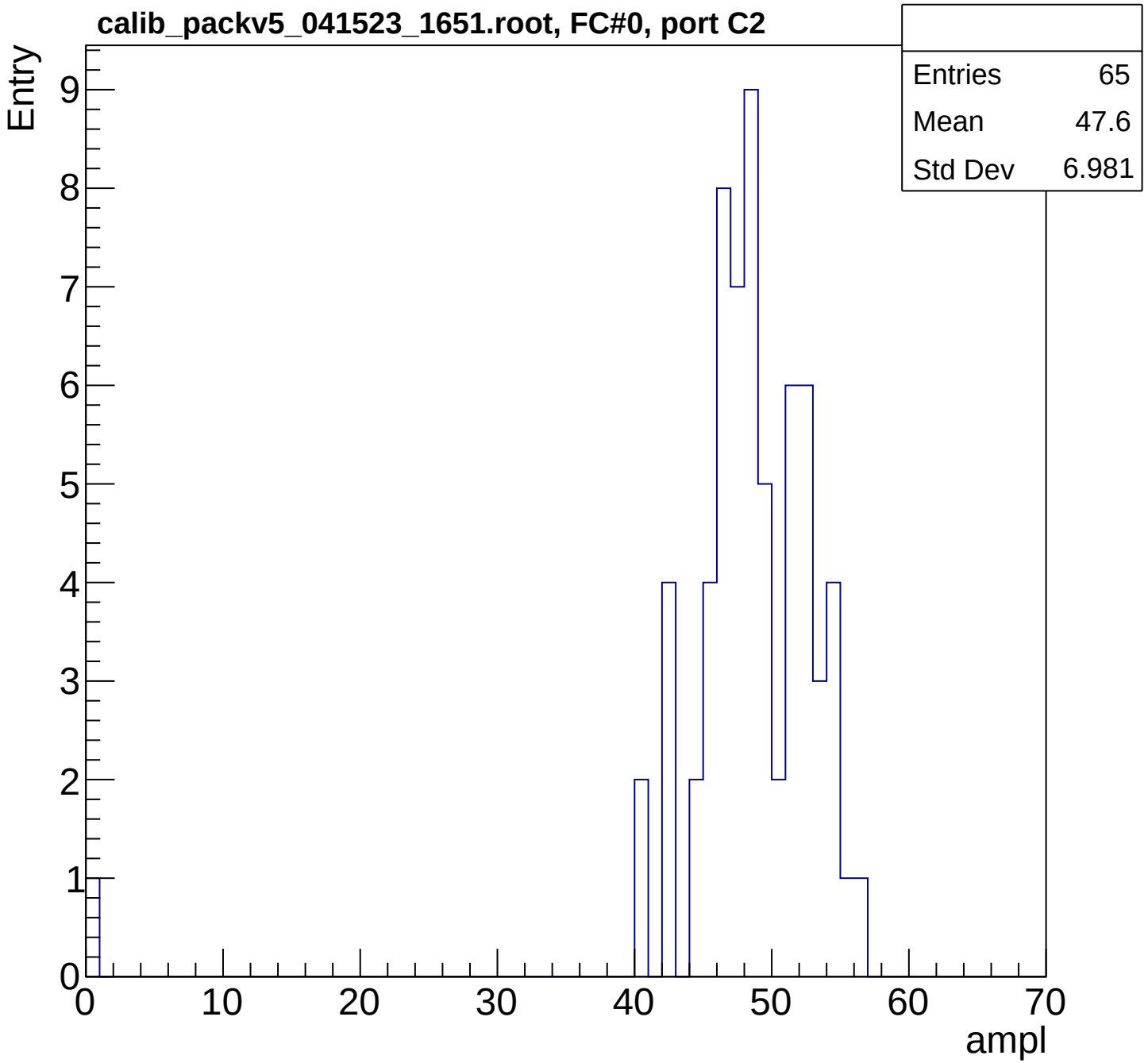
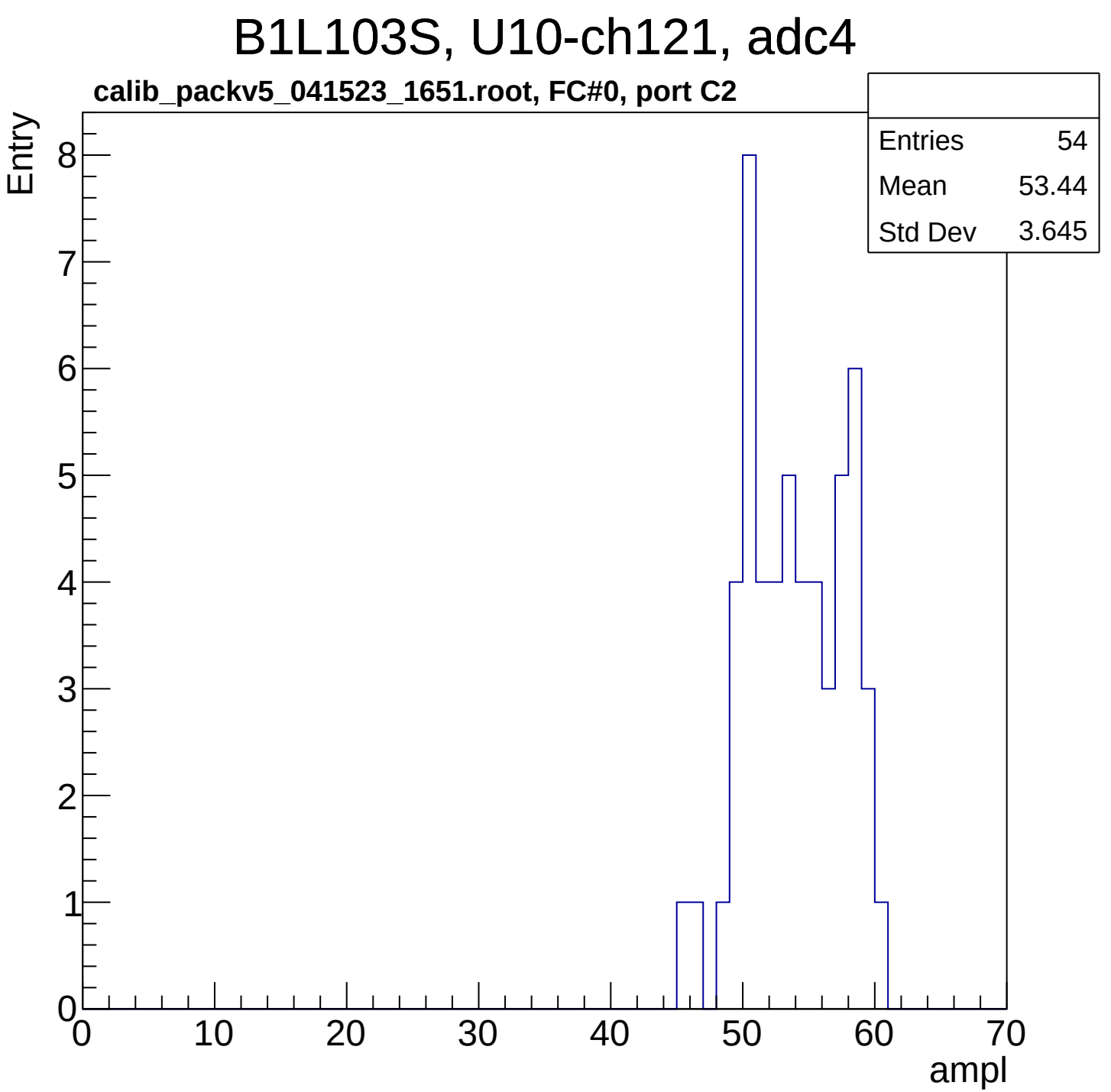

B1L103S, U10-ch121, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 33.13
Std Dev 5.435
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U10-ch121, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 37.2
Std Dev 12.4
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U10-ch121, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 47.6
Std Dev 6.981
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U10-ch121, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 53.44
Std Dev 3.645
Entry
ampl
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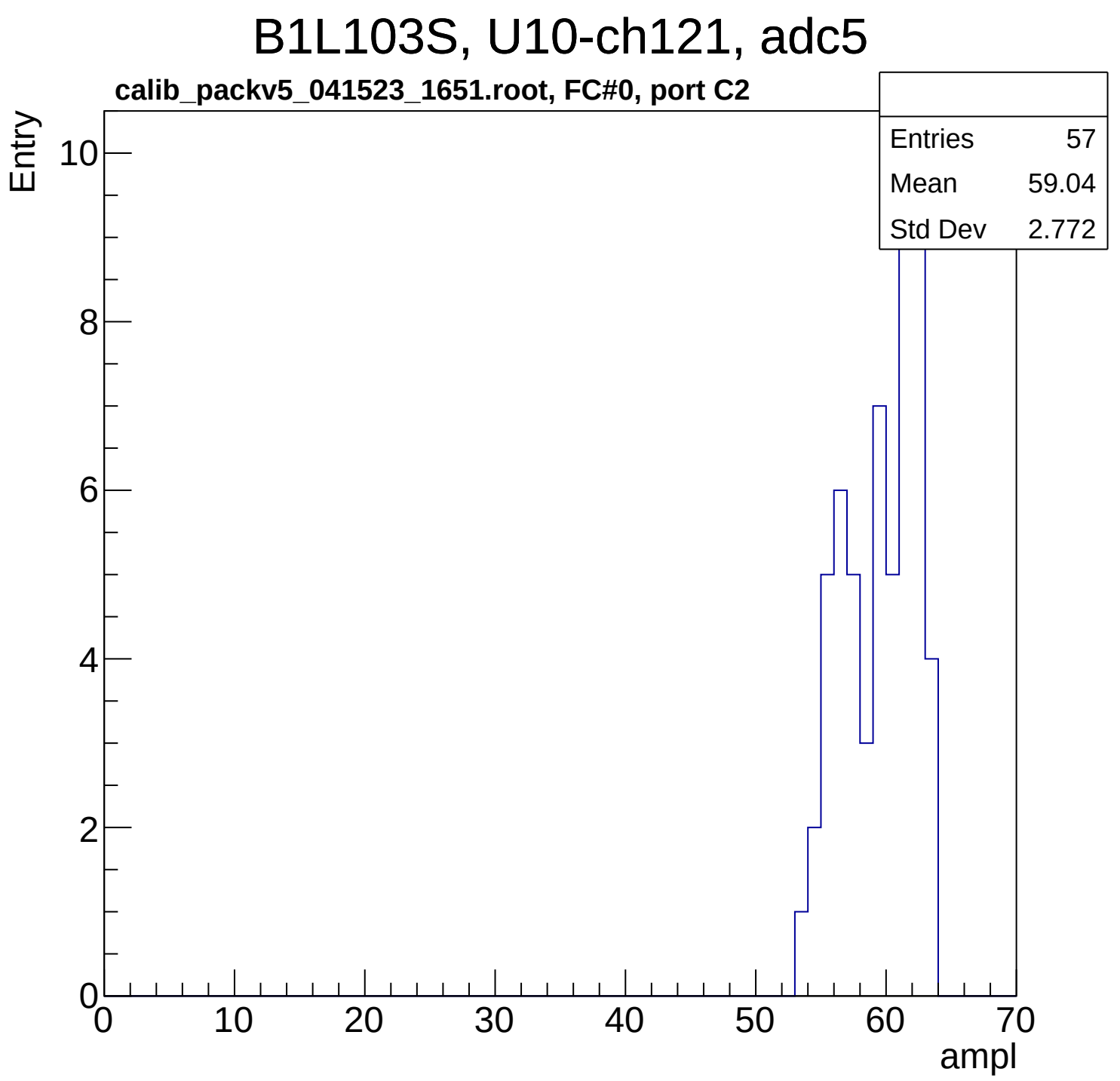
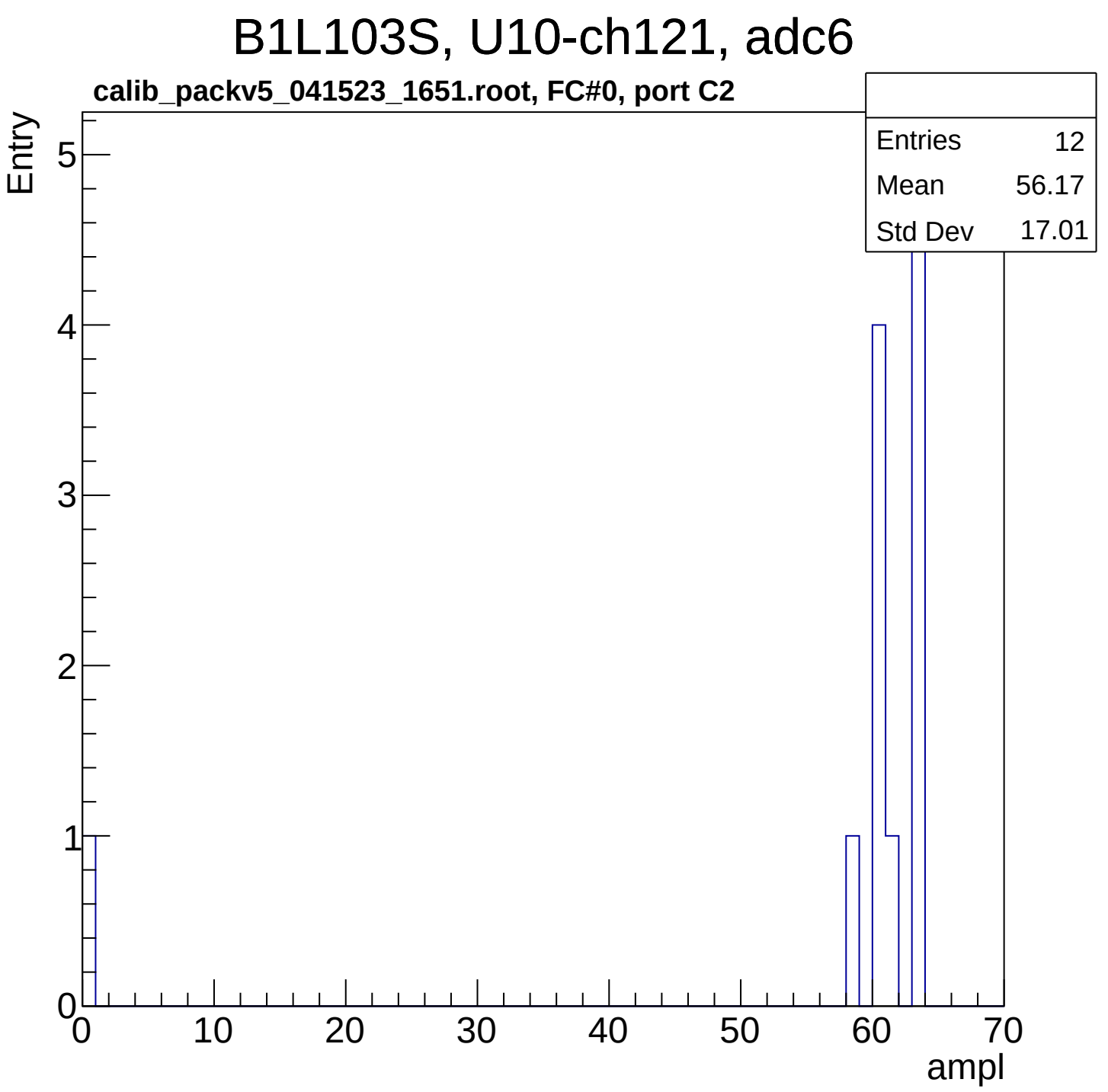
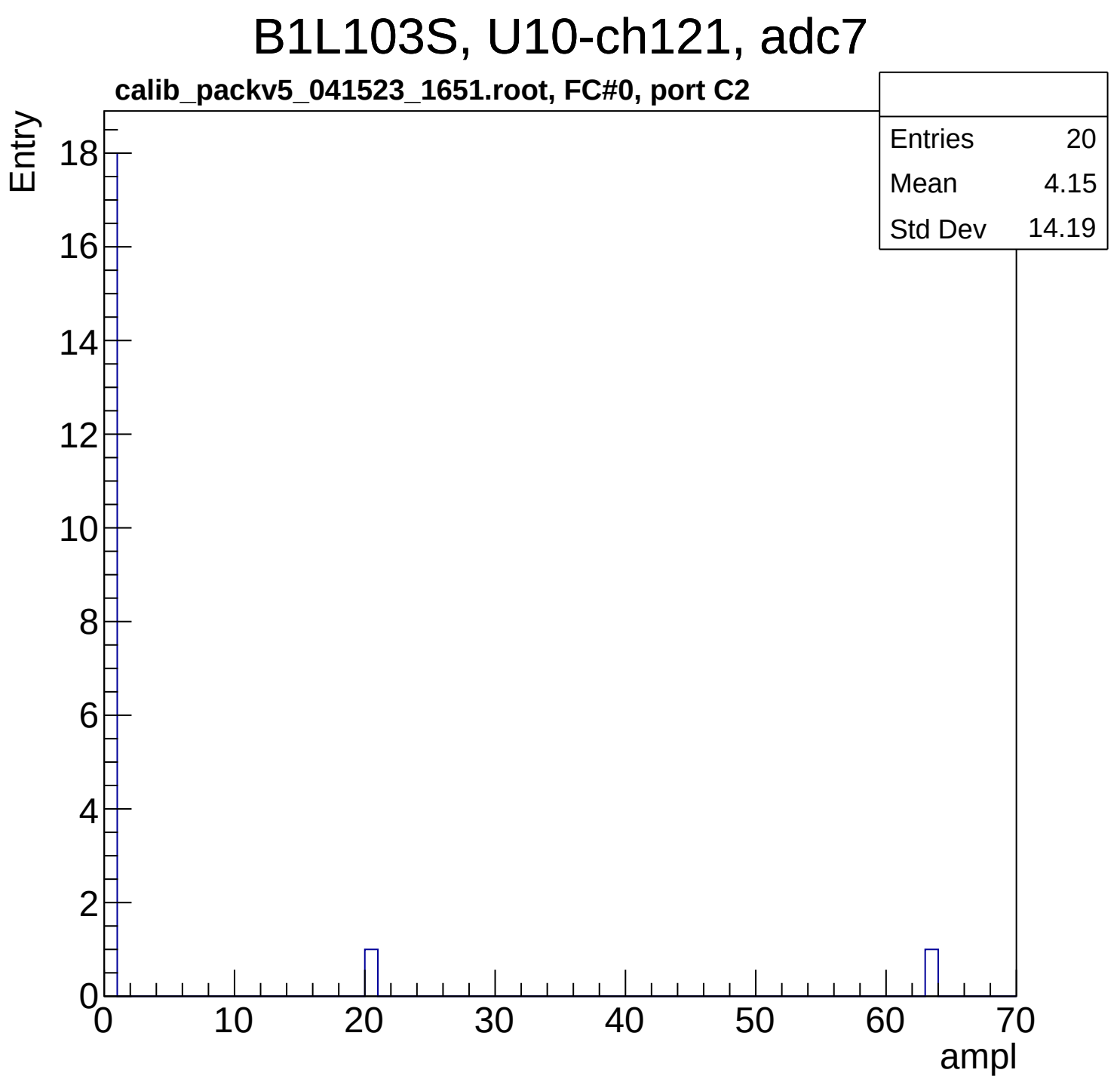
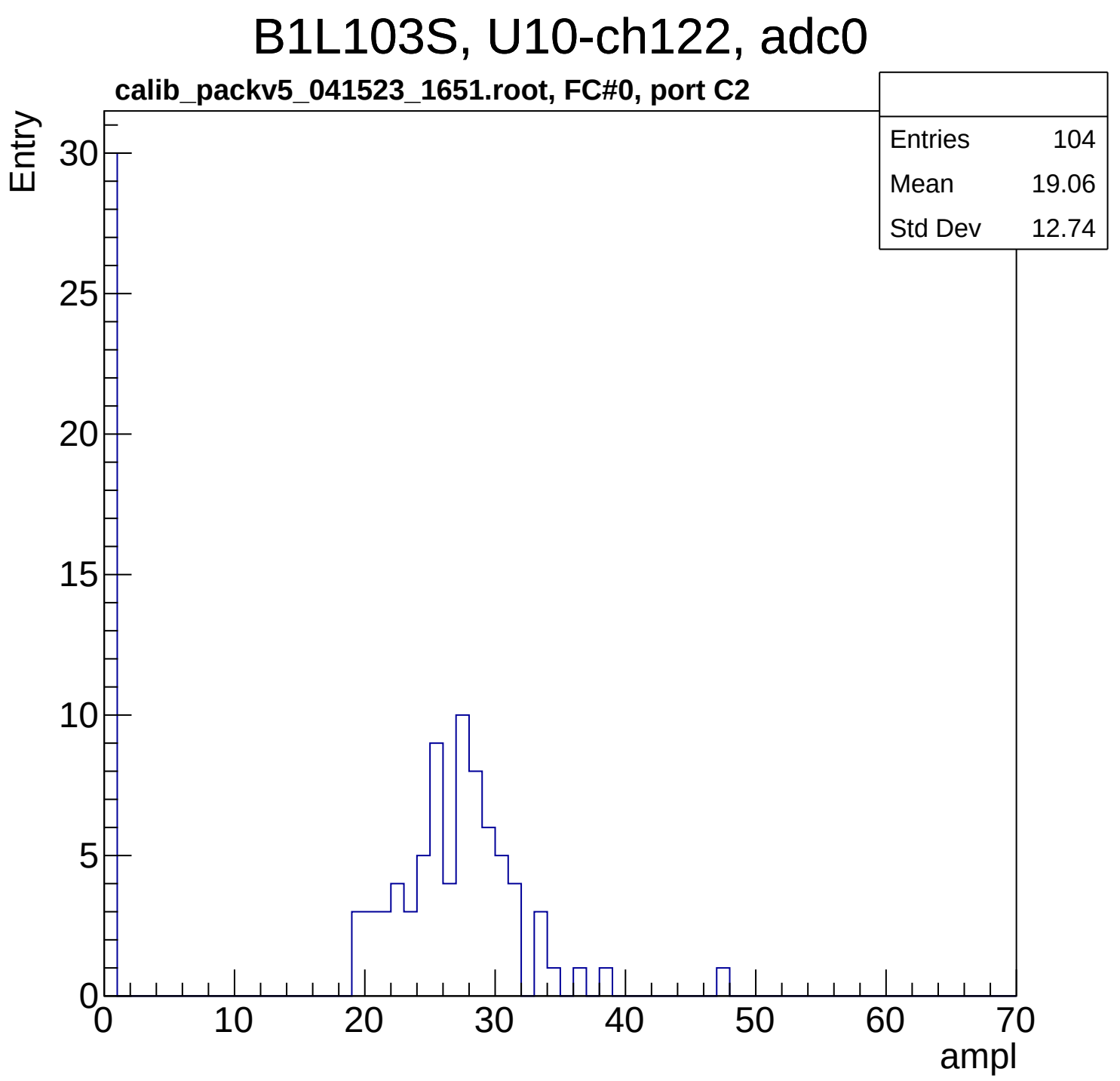
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U10-ch121, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 59.04
Std Dev 2.772
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch121, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 56.17
Std Dev 17.01
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch121, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 4.15
Std Dev 14.19
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch122, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 104
Mean 19.06
Std Dev 12.74
Entry
ampl
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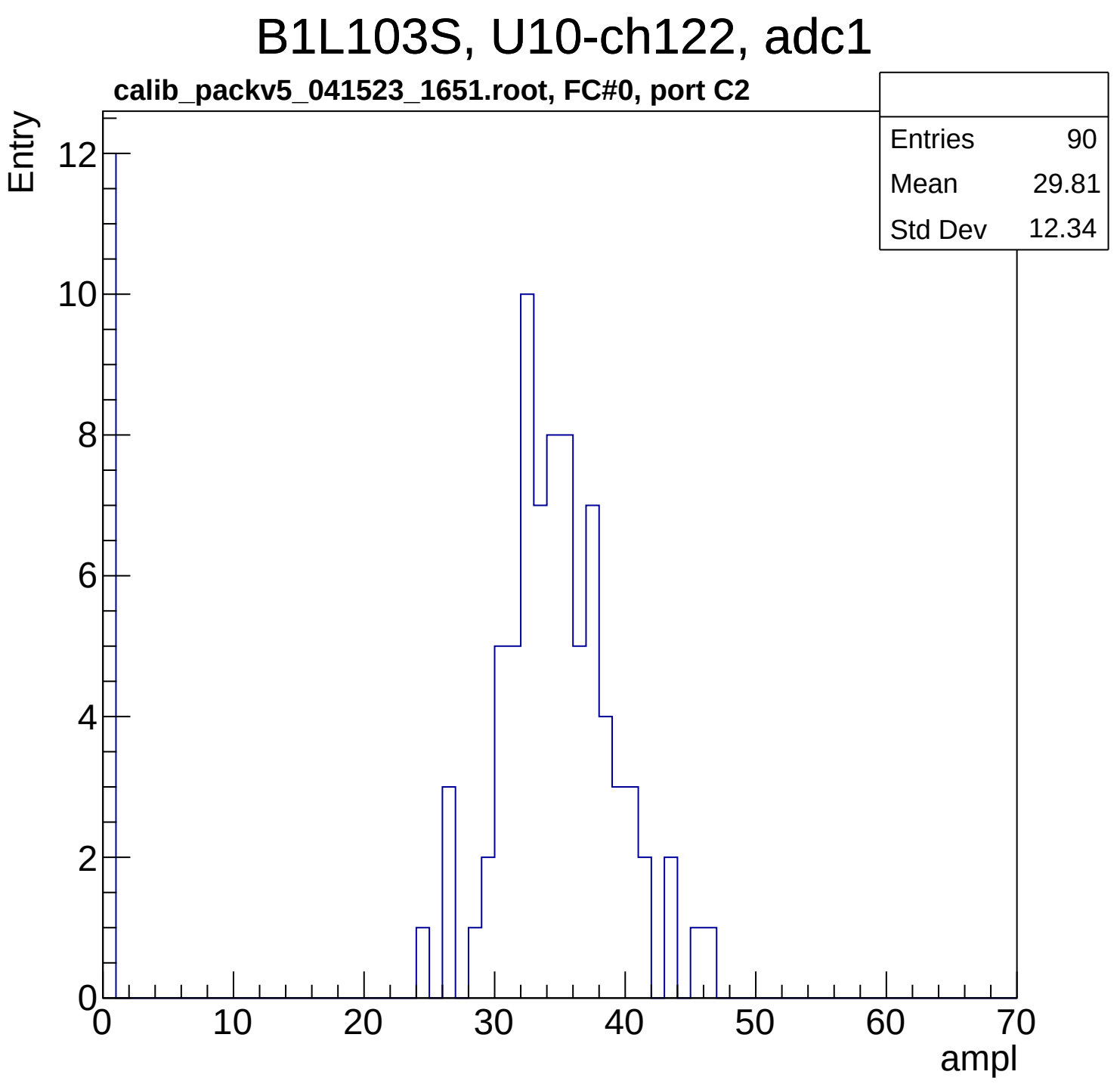
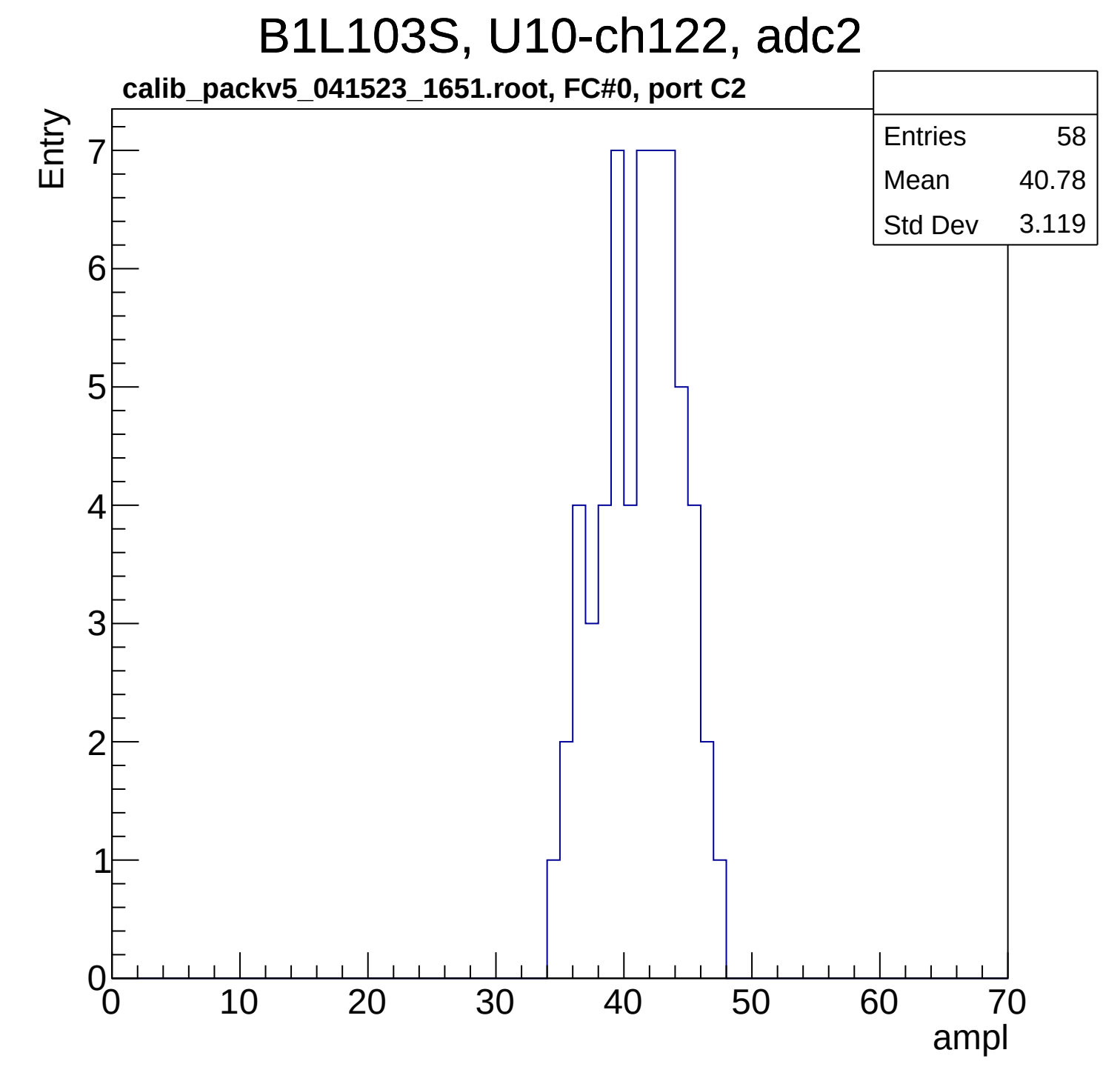
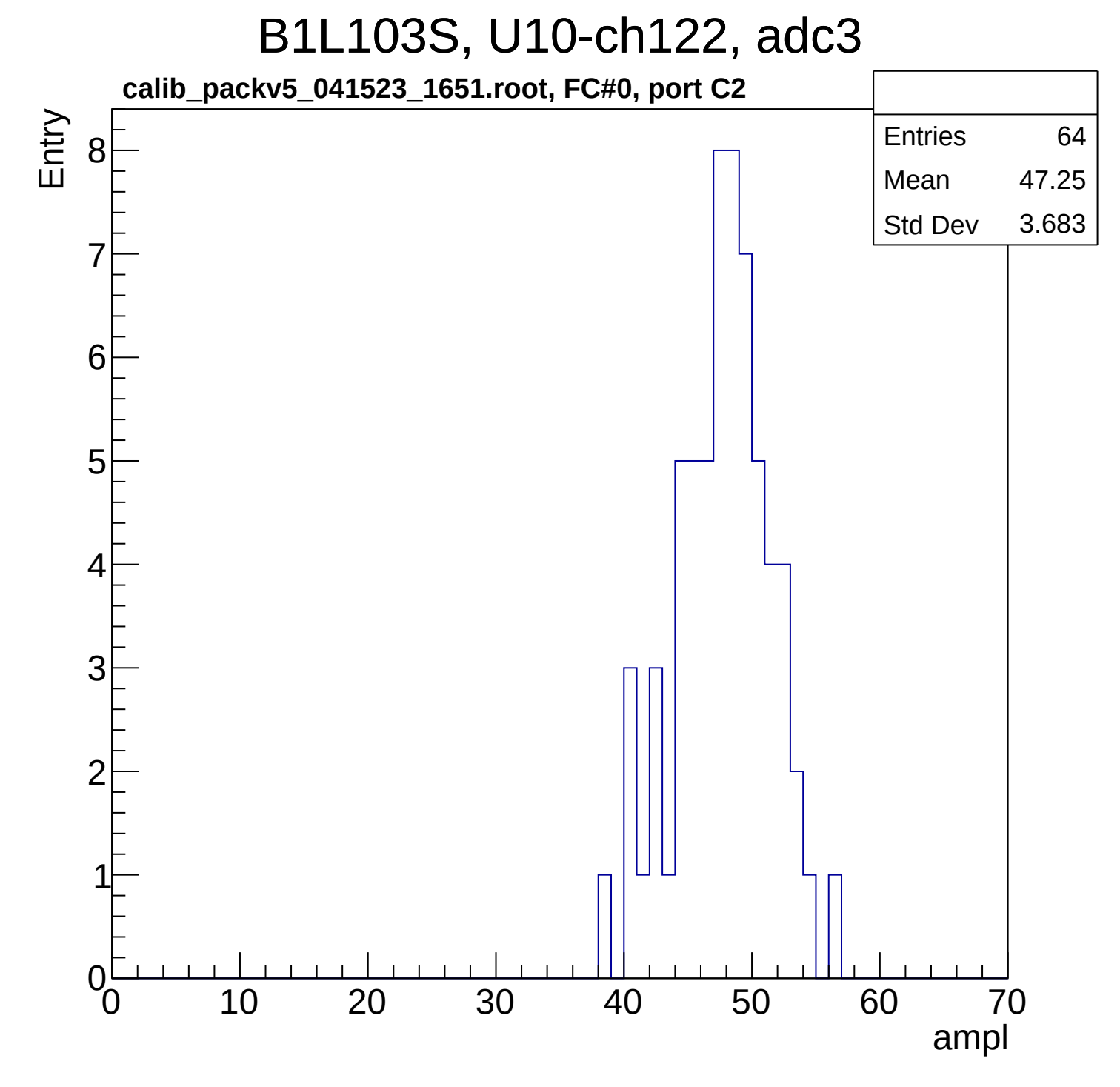
5
10
15
20
25
30
0
10
20
30
40
50
60
70


B1L103S, U10-ch122, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 90
Mean 29.81
Std Dev 12.34
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch122, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 40.78
Std Dev 3.119
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U10-ch122, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 47.25
Std Dev 3.683
Entry
ampl
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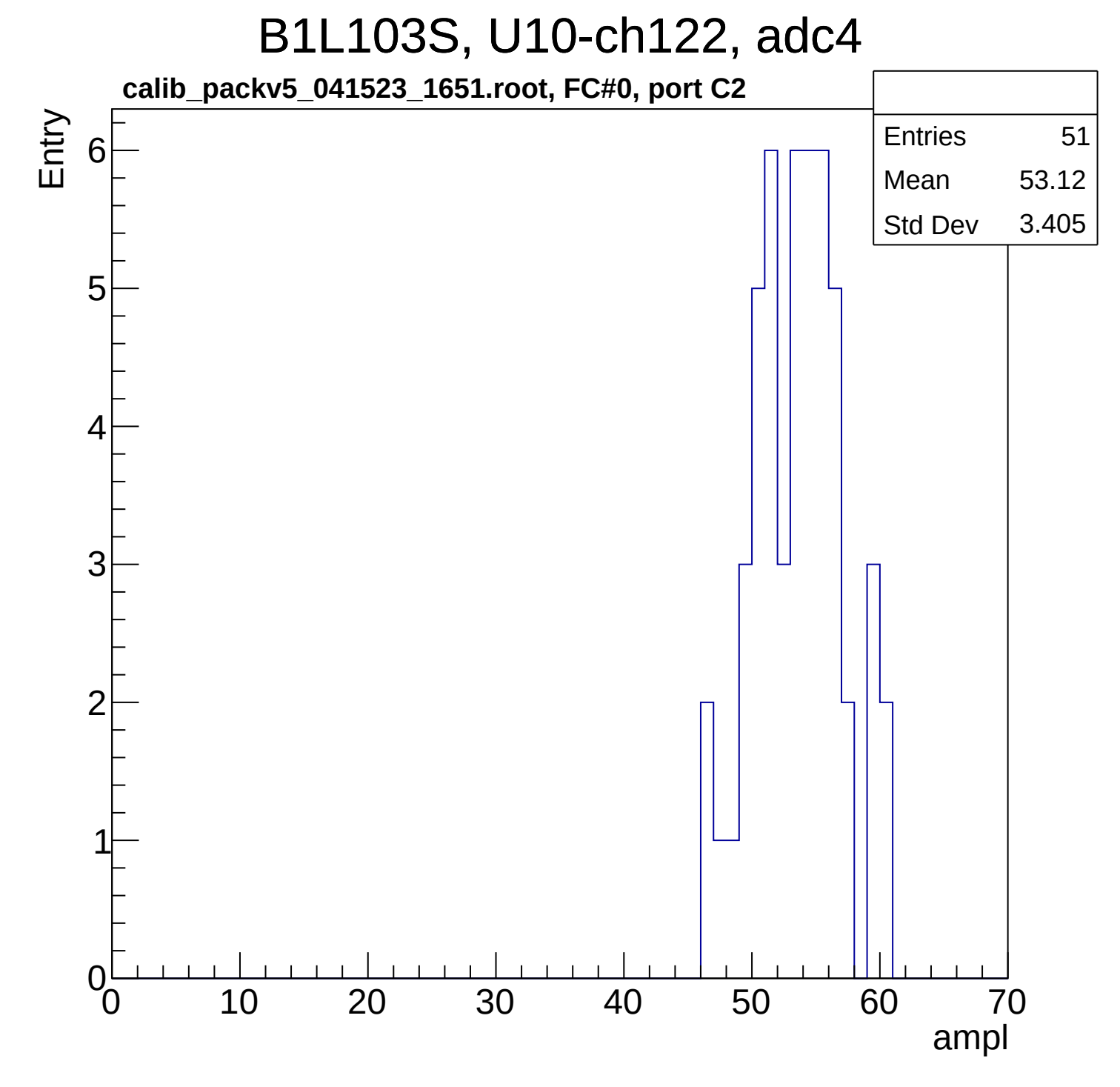
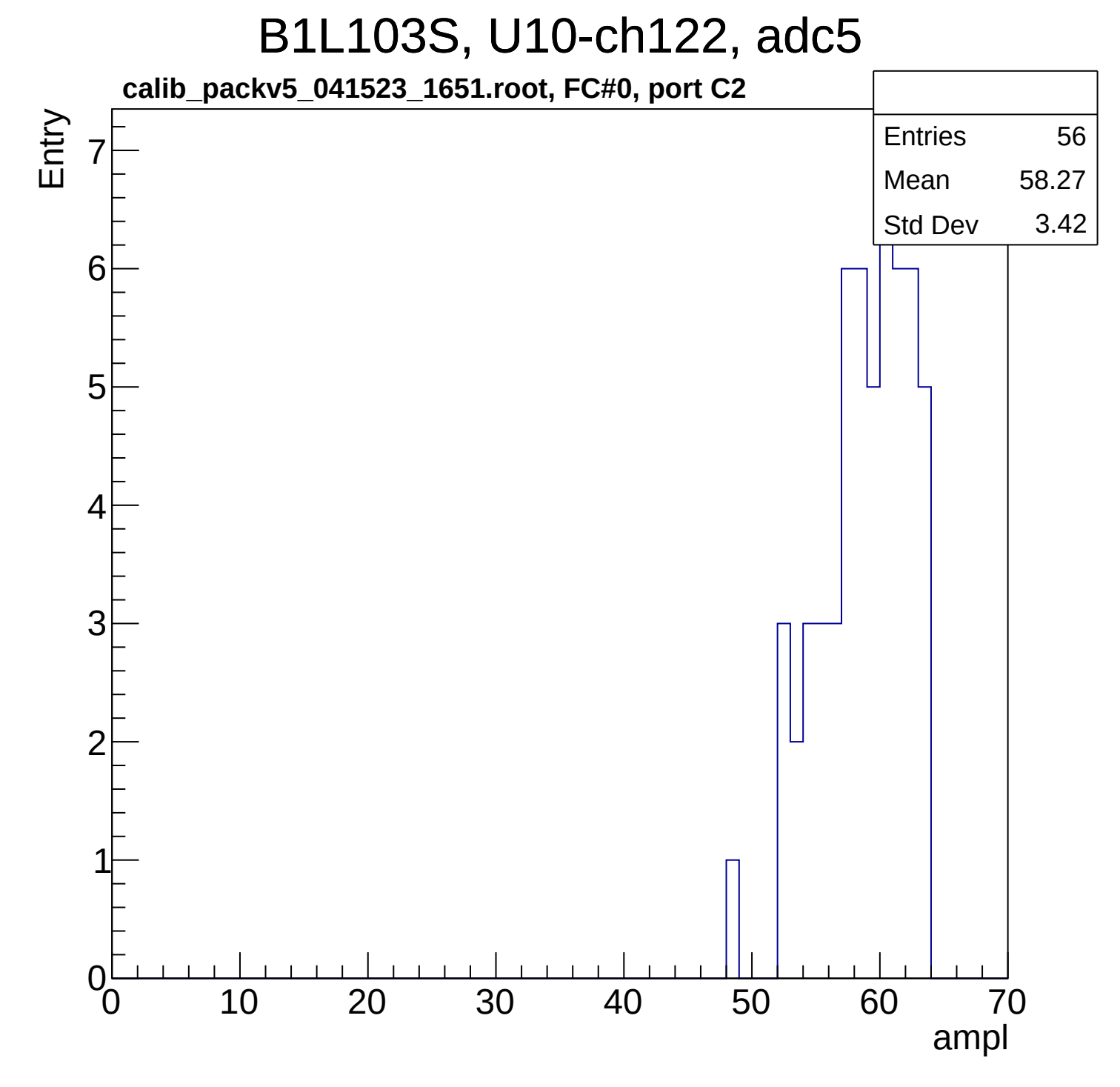
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U10-ch122, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 53.12
Std Dev 3.405
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U10-ch122, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 58.27
Std Dev 3.42
Entry
ampl
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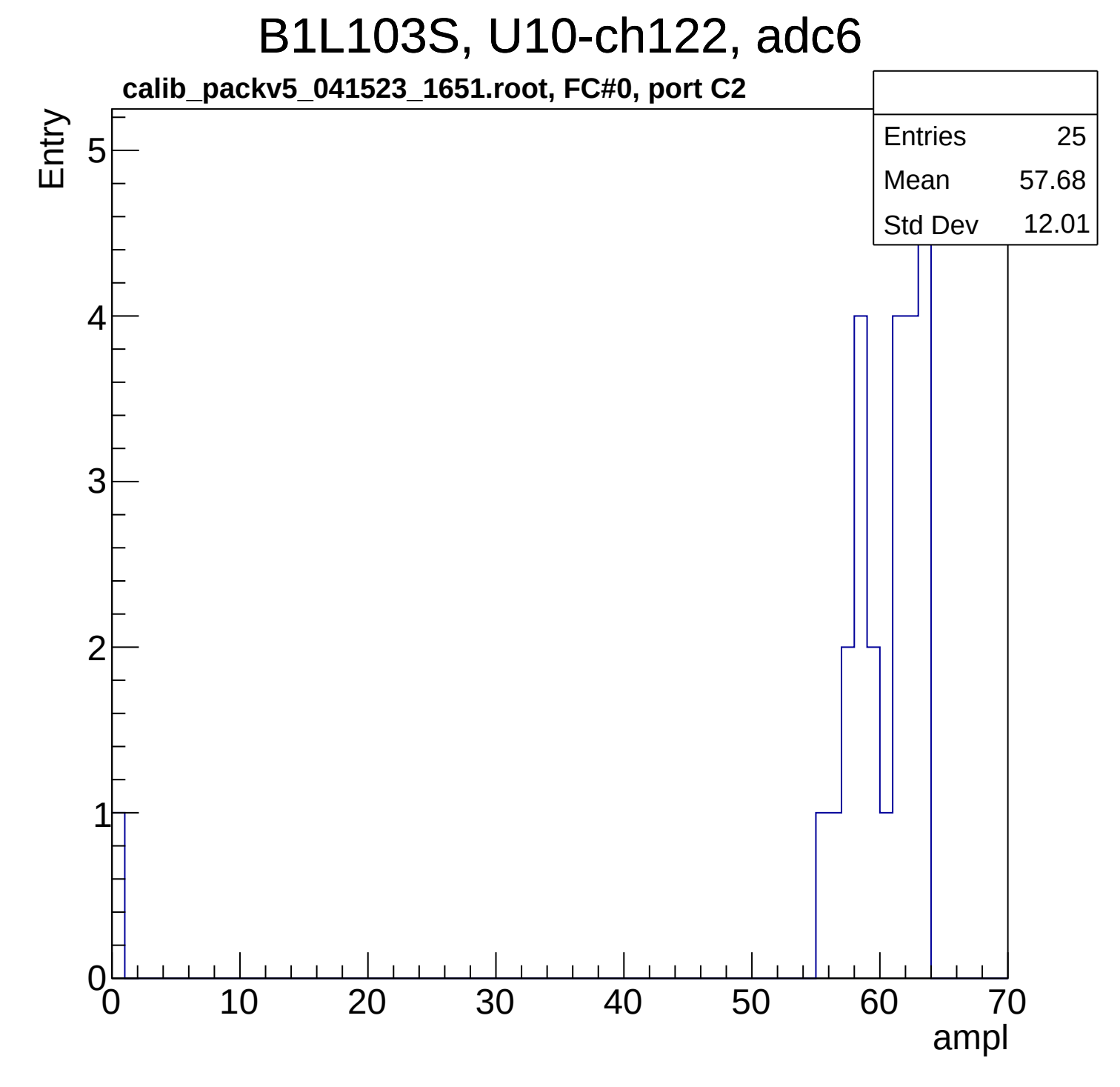
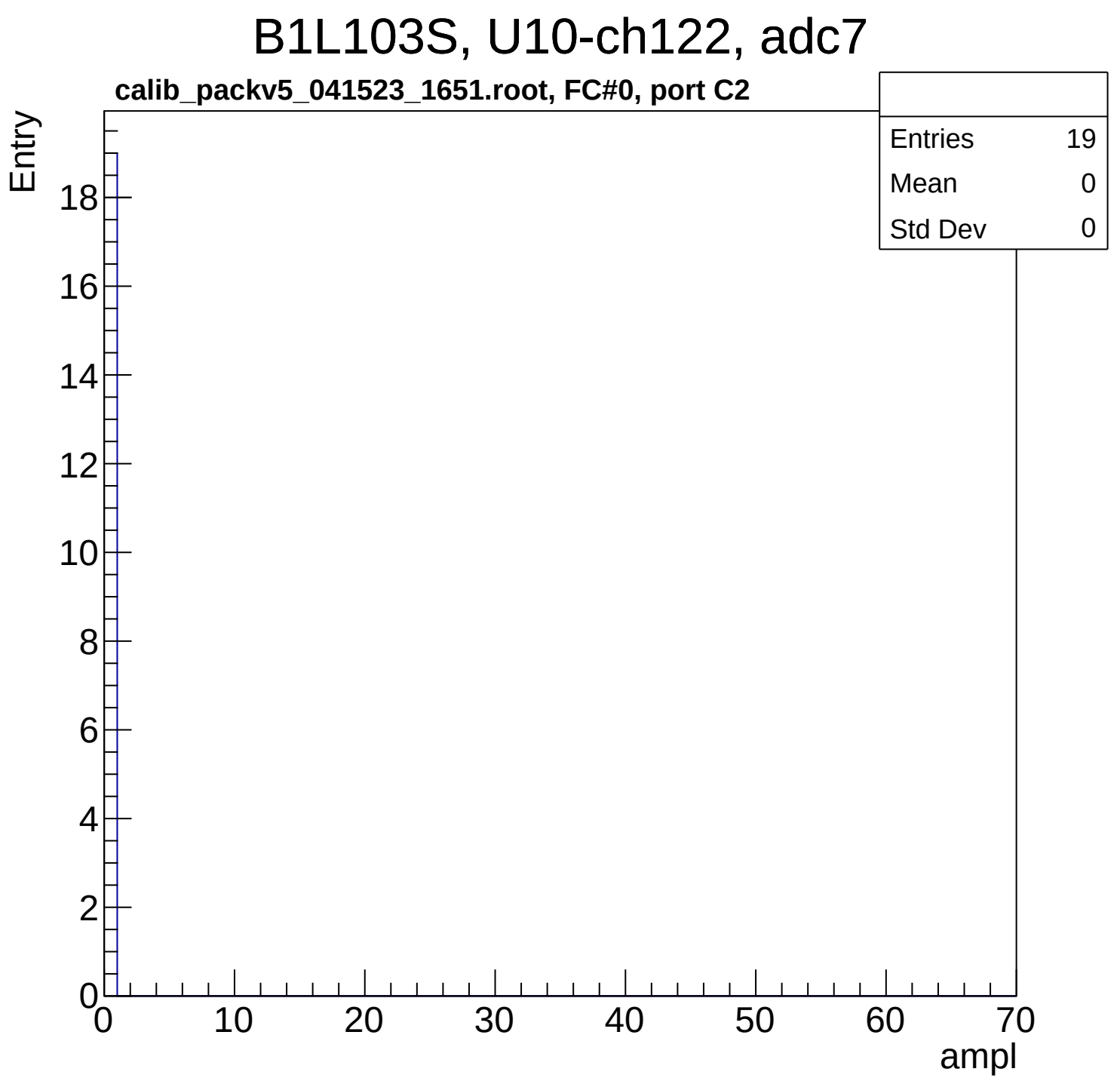
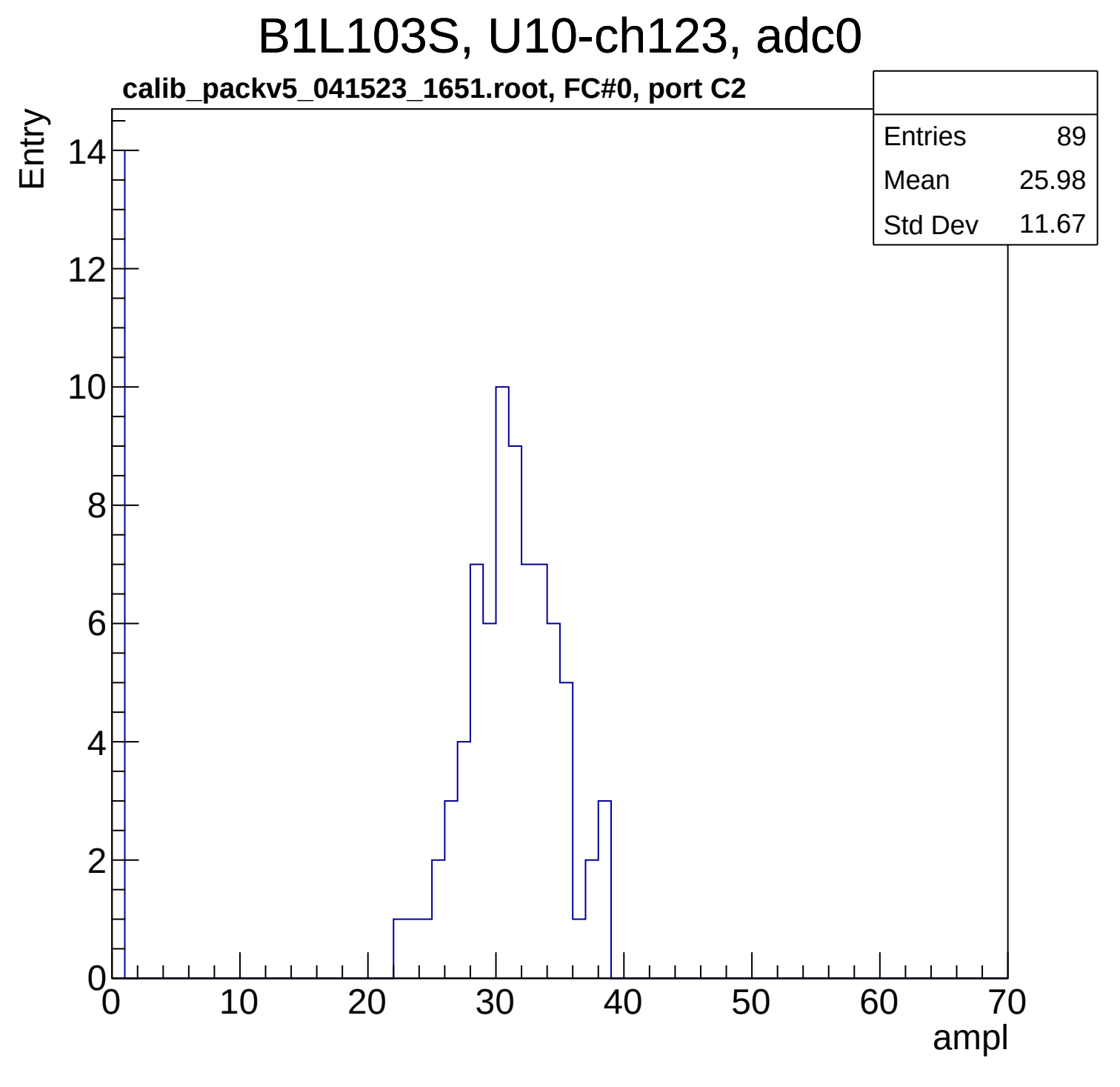
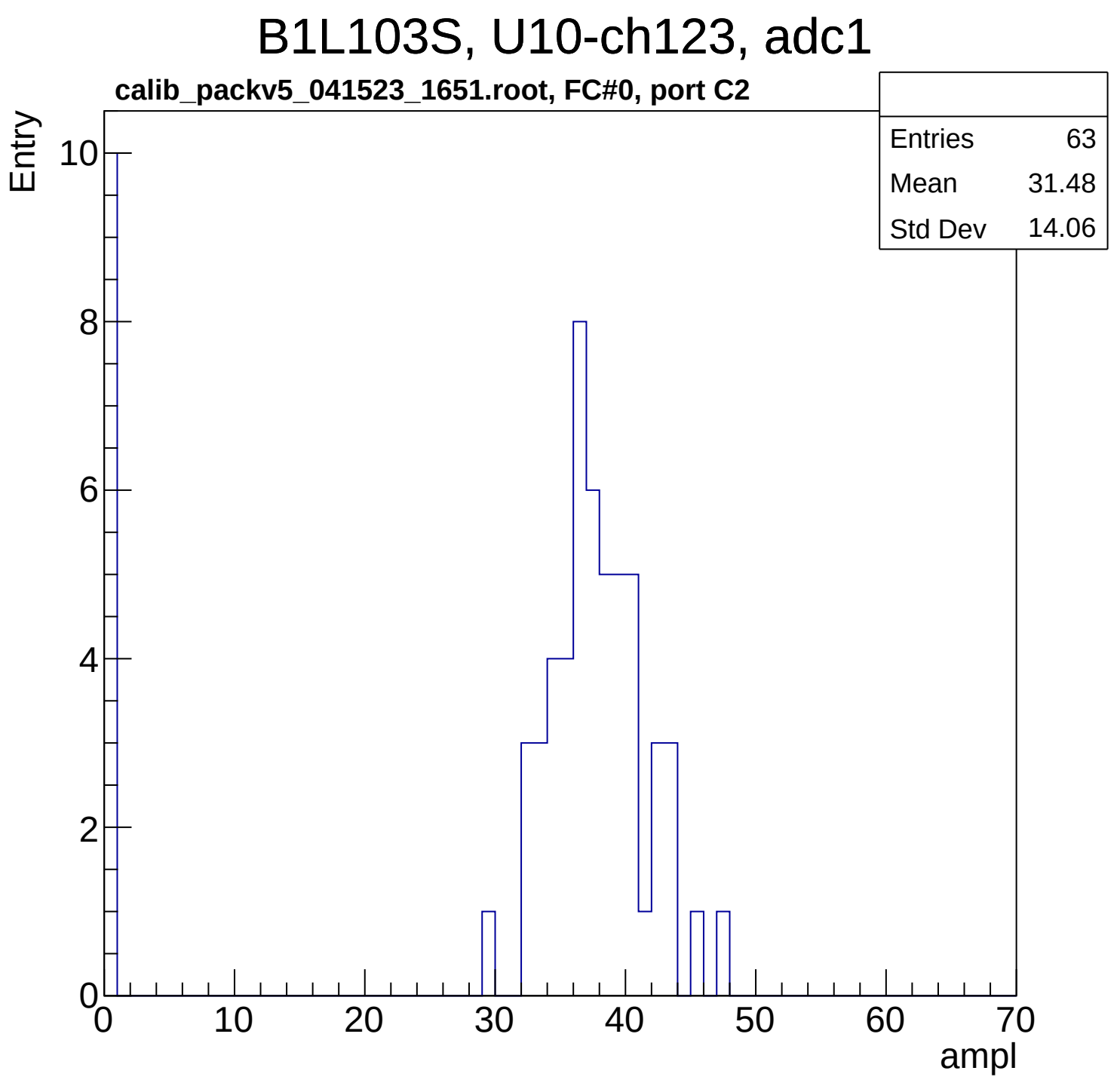
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U10-ch122, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 25
Mean 57.68
Std Dev 12.01
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U10-ch122, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch123, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 89
Mean 25.98
Std Dev 11.67
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L103S, U10-ch123, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 31.48
Std Dev 14.06
Entry
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2
4
6
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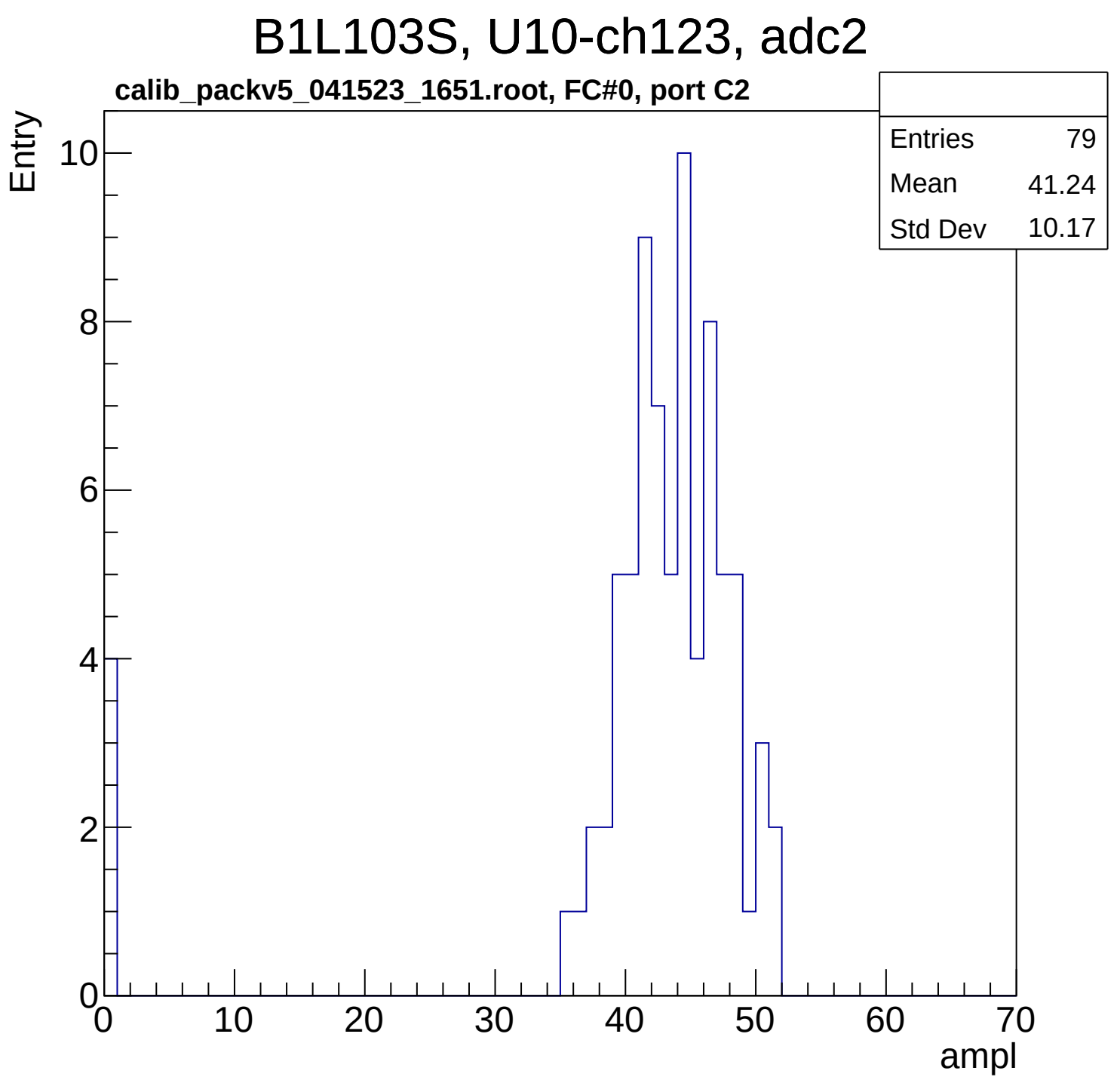
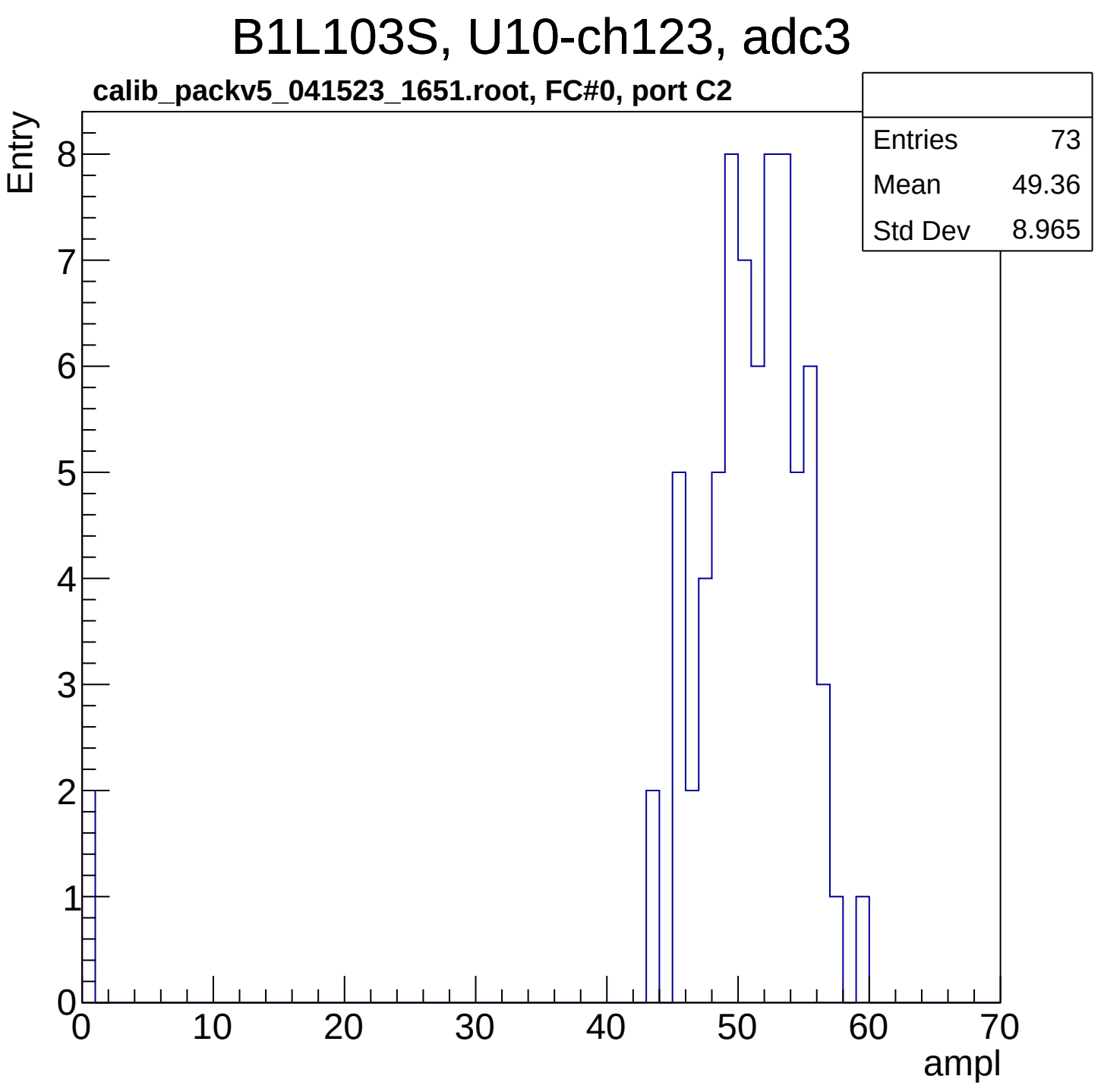
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch123, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 41.24
Std Dev 10.17
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch123, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 49.36
Std Dev 8.965
Entry
ampl
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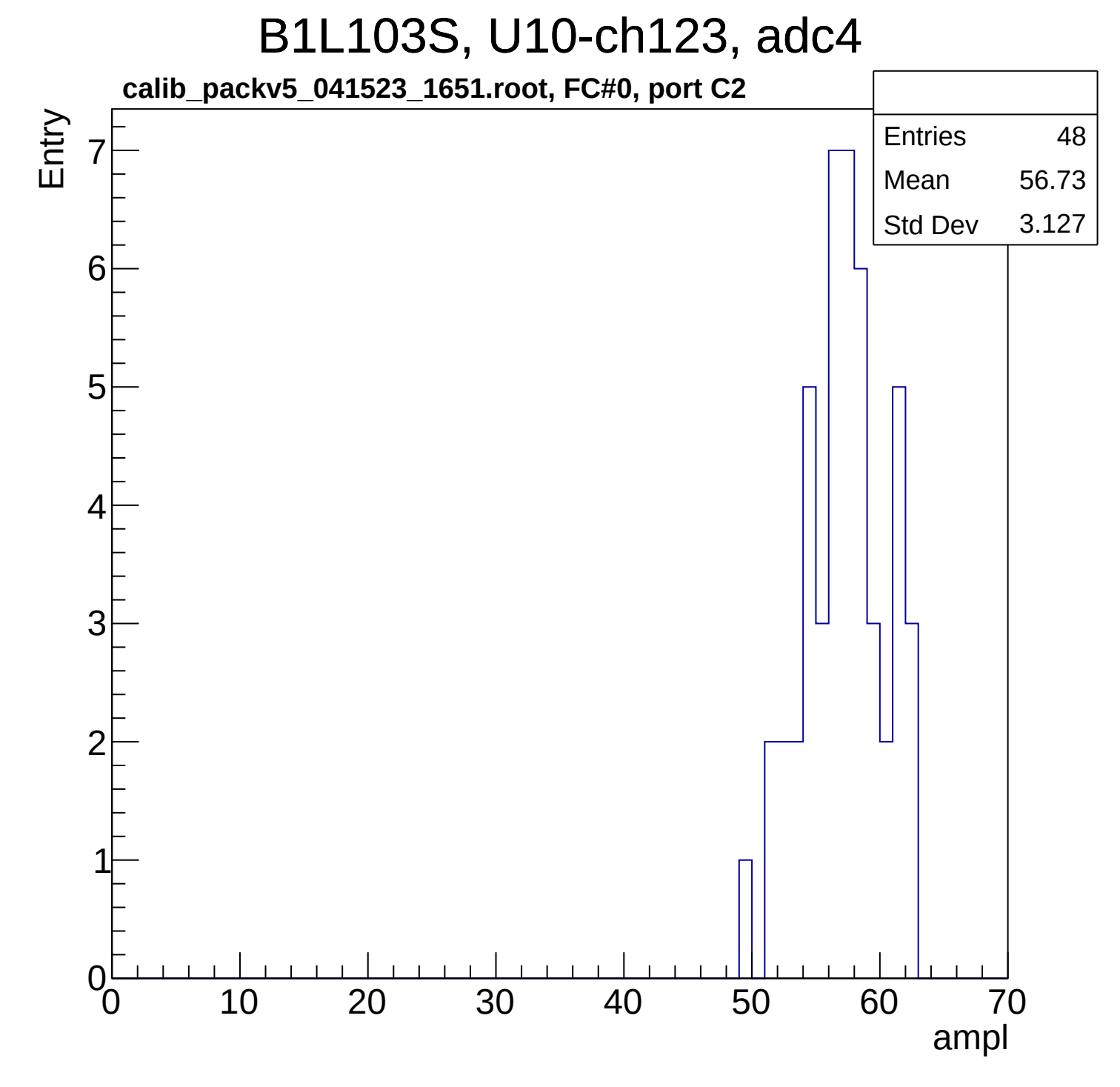
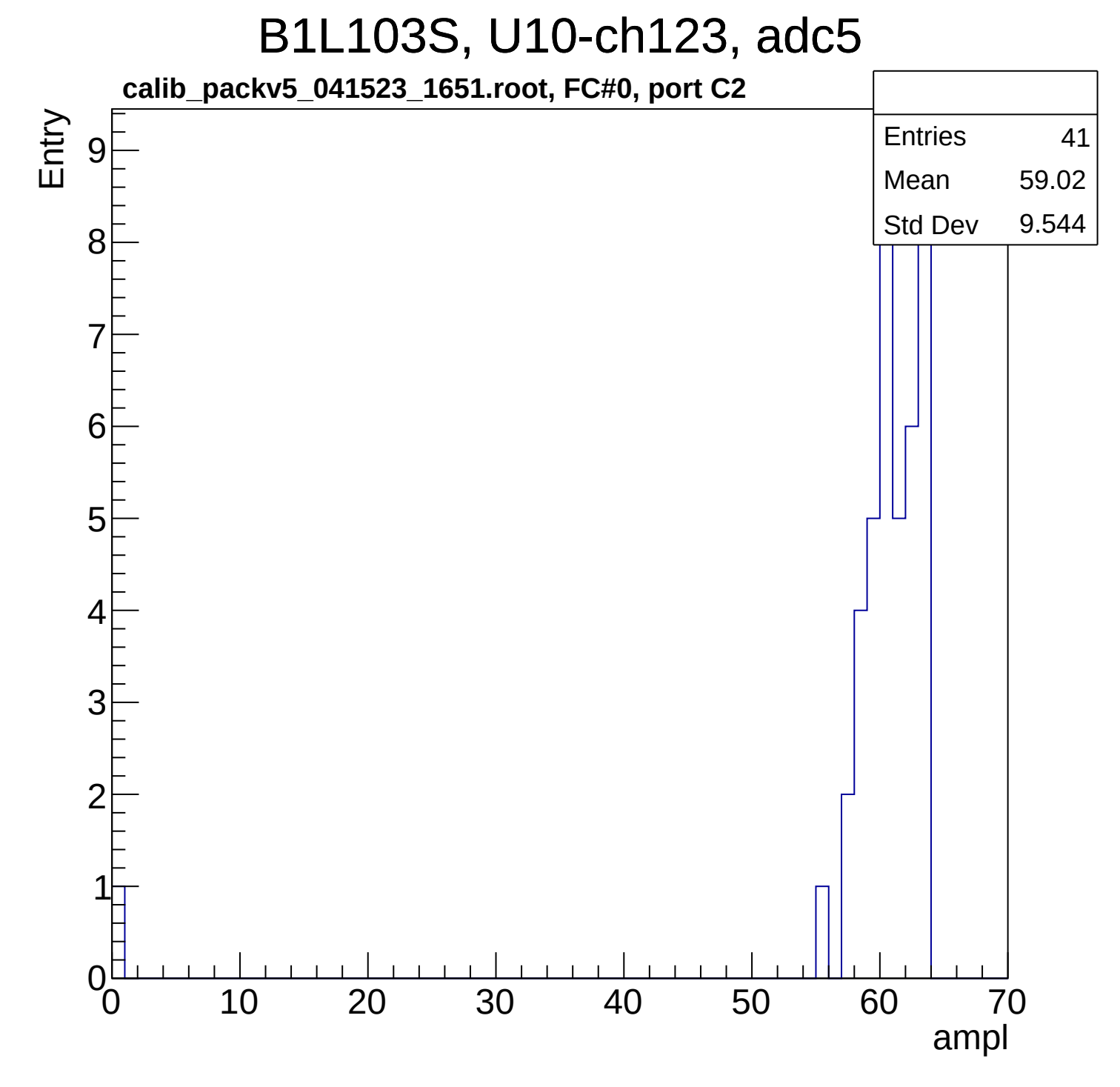
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U10-ch123, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 56.73
Std Dev 3.127
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U10-ch123, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 41
Mean 59.02
Std Dev 9.544
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
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40
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60
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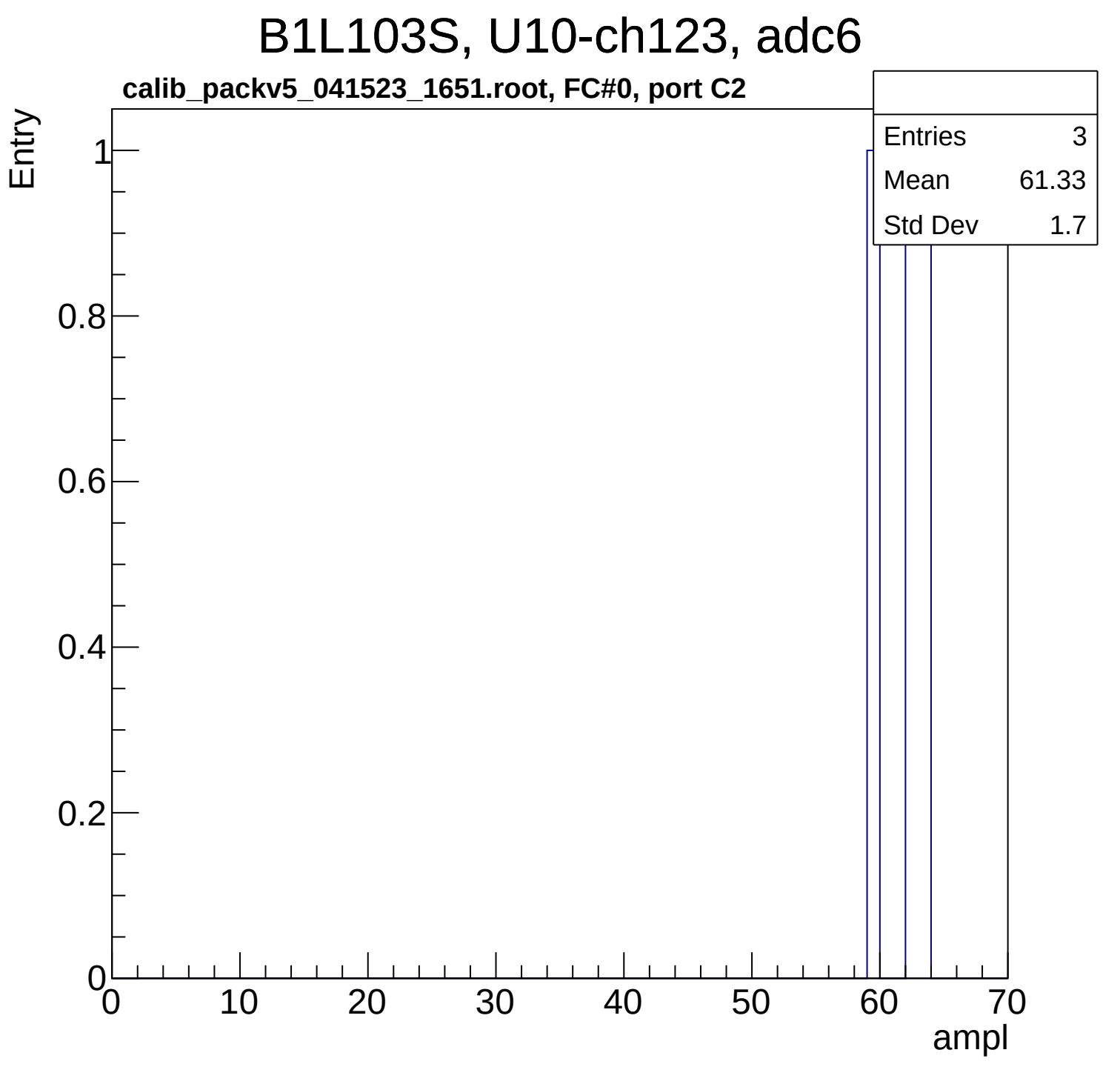
B1L103S, U10-ch123, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 3
Mean 61.33
Std Dev 1.7
Entry
ampl
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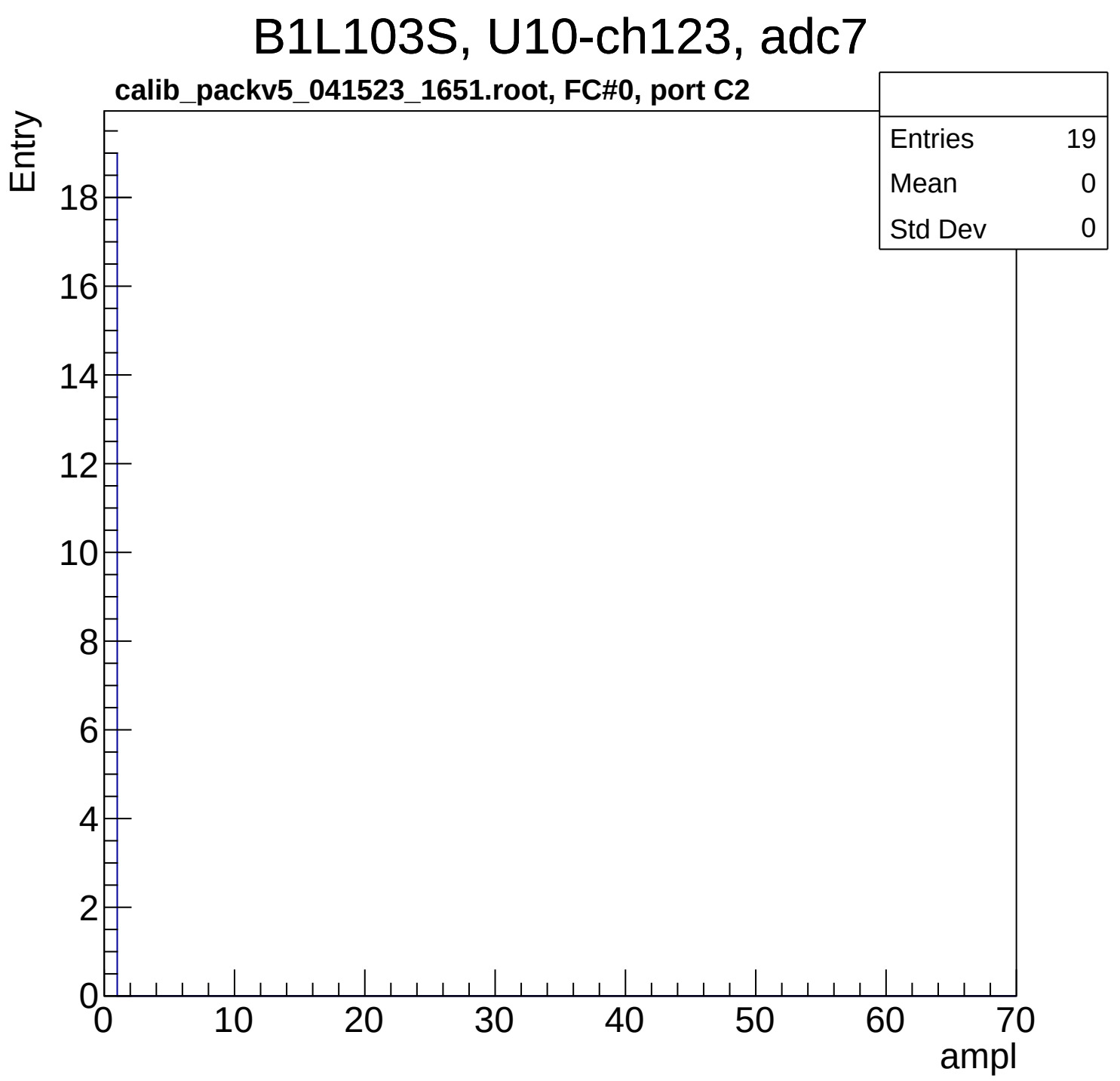
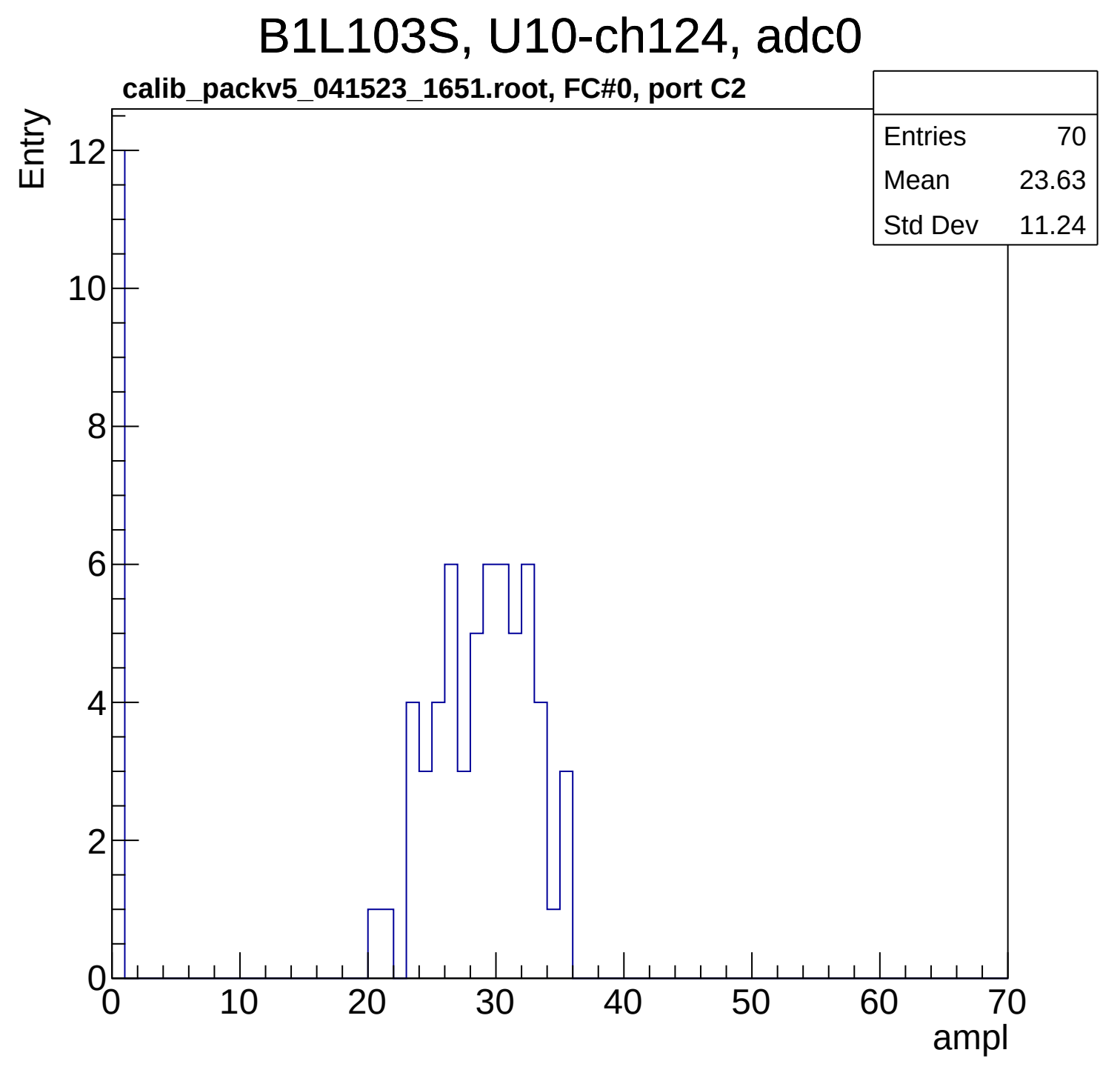
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70


B1L103S, U10-ch123, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch124, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 23.63
Std Dev 11.24
Entry
0
2
4
6
8
10
12
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10
20
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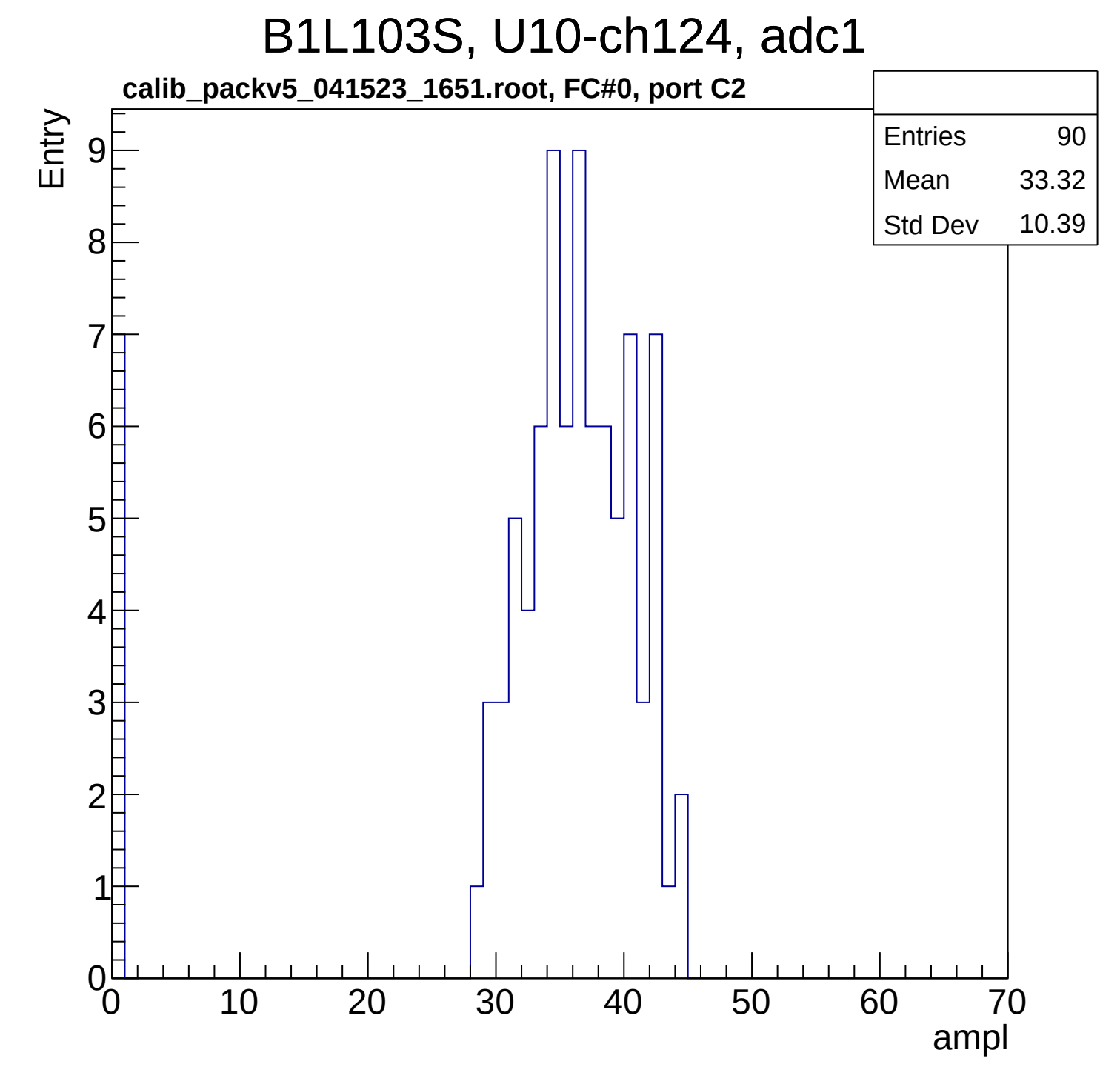
50
60
70
ampl


B1L103S, U10-ch124, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 90
Mean 33.32
Std Dev 10.39
Entry
ampl
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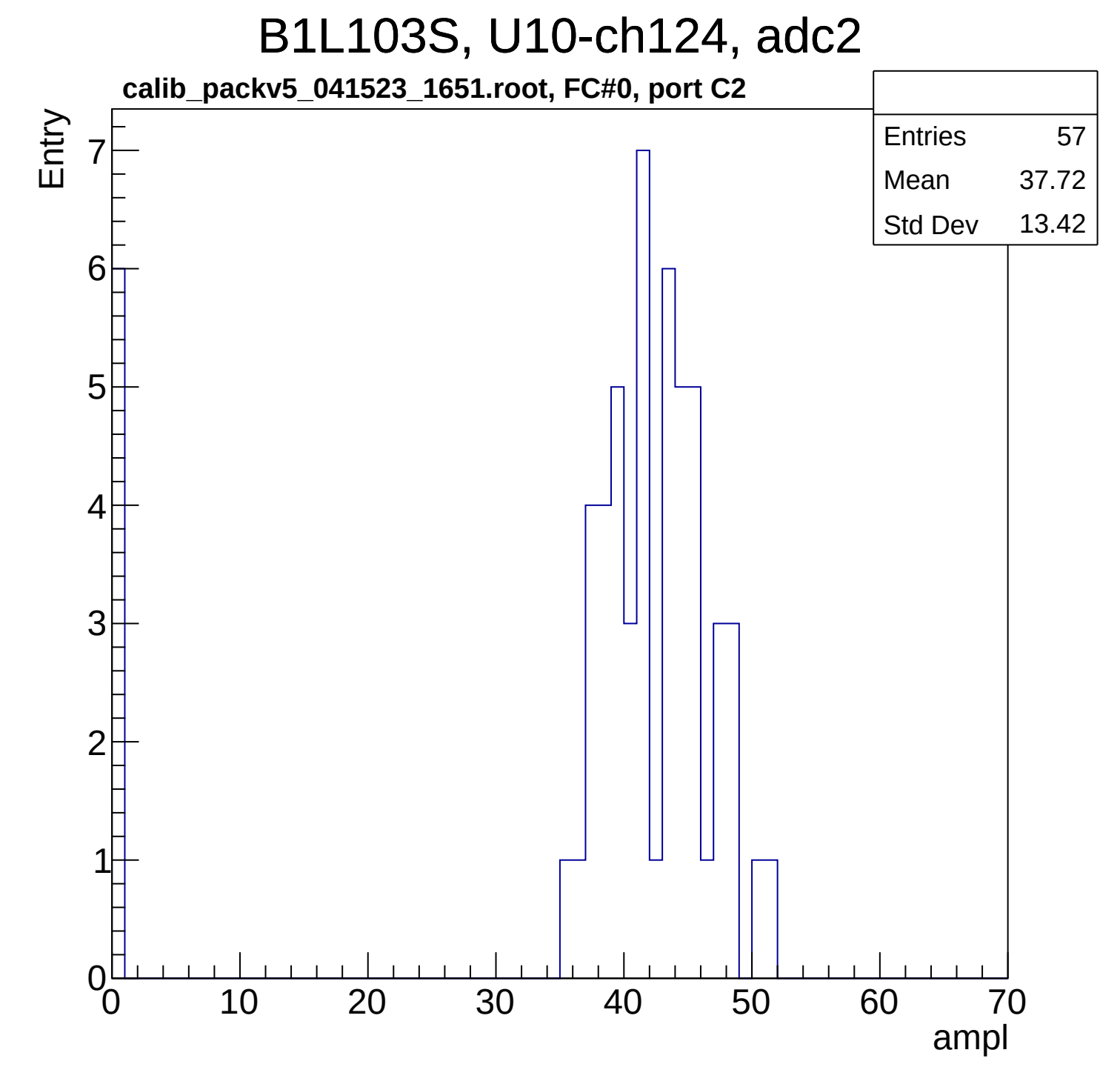
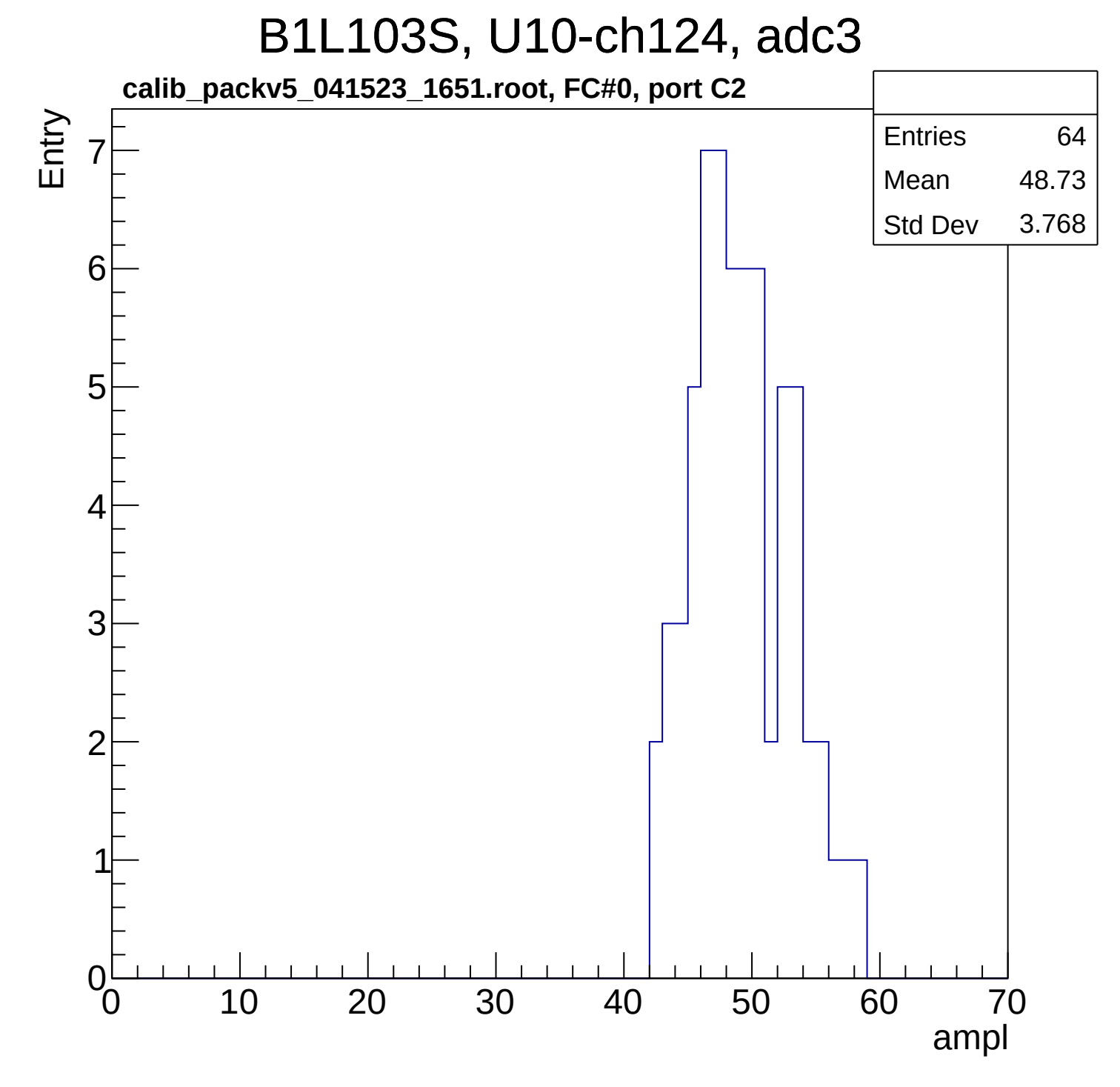
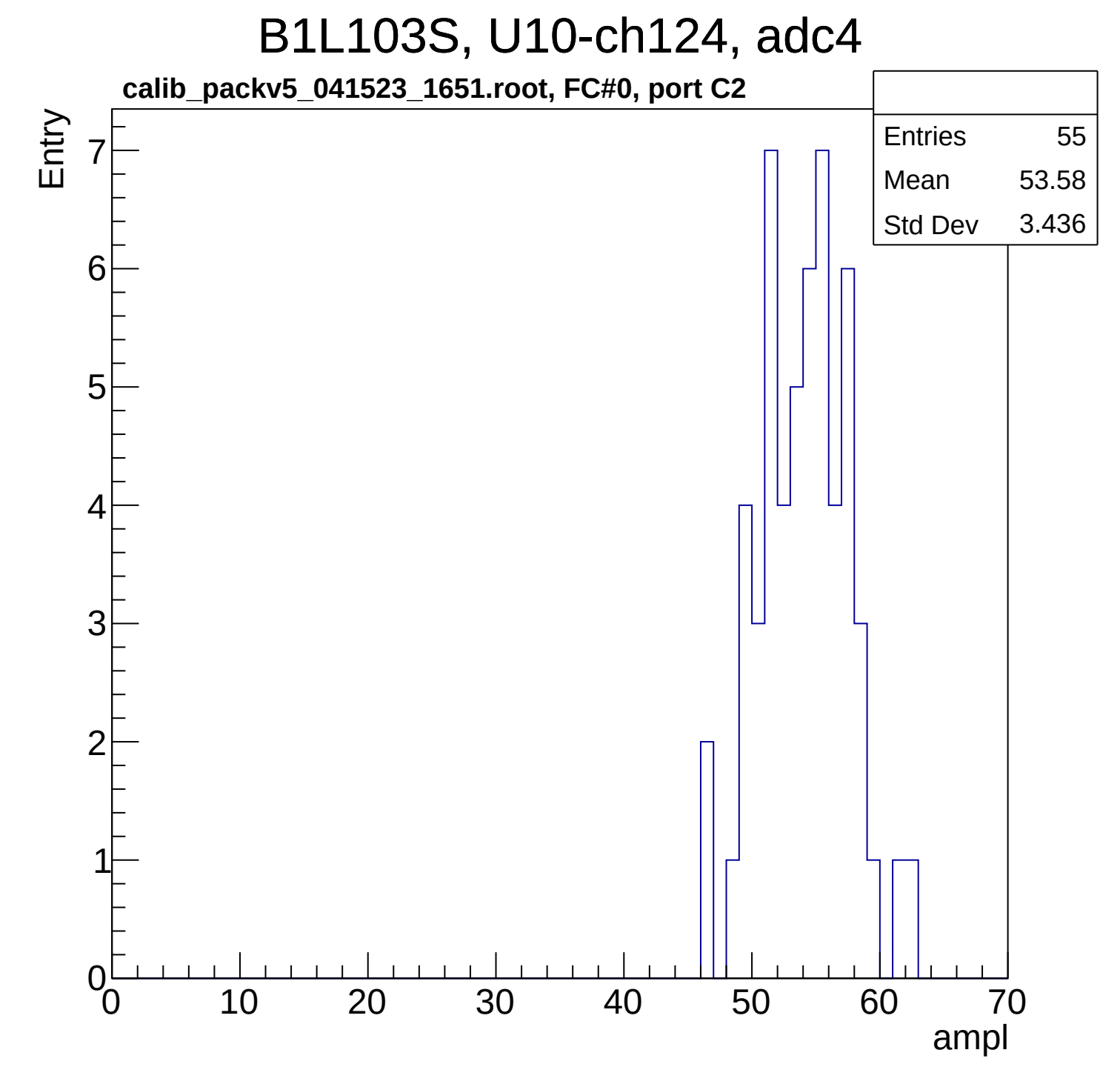
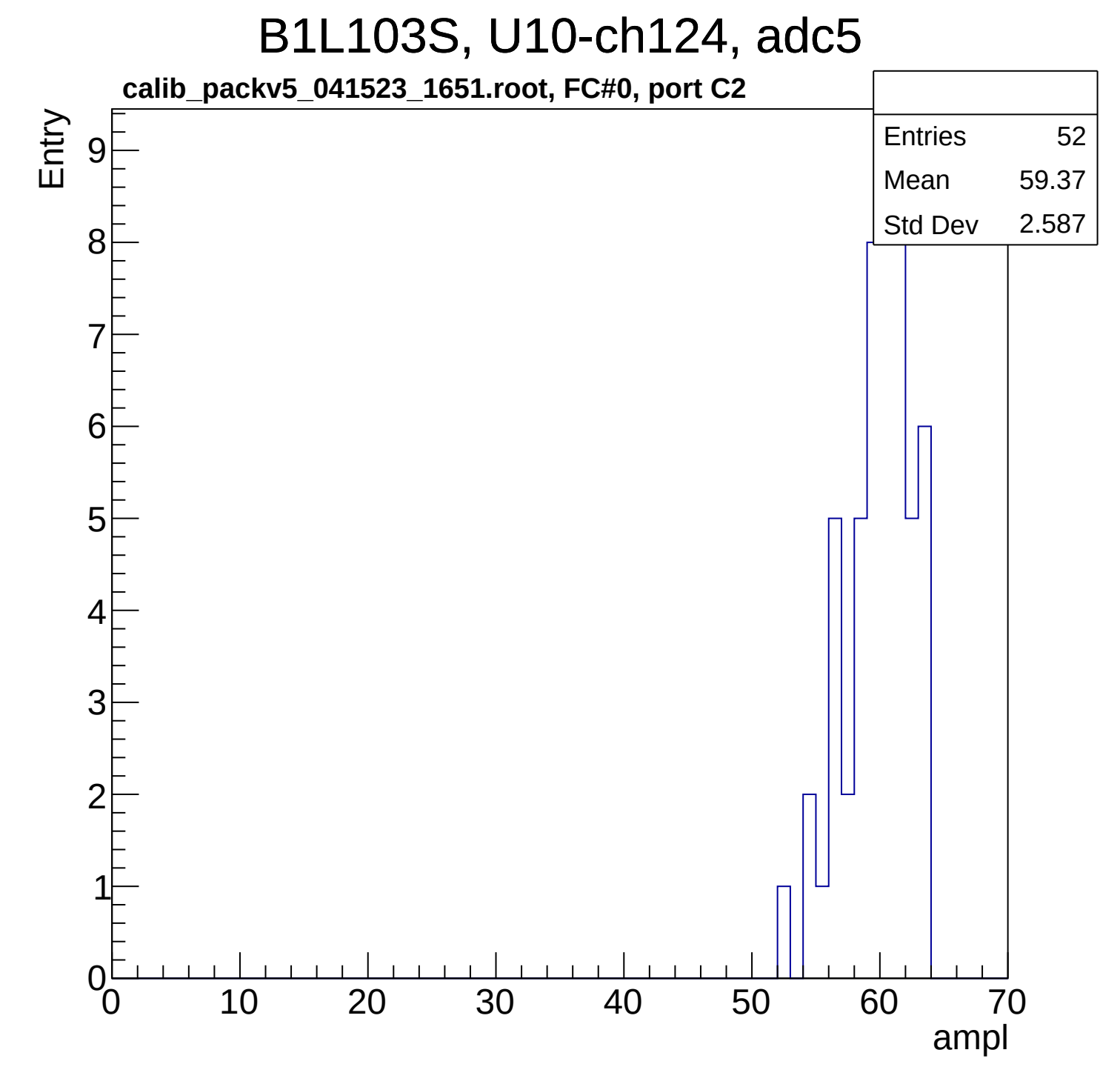
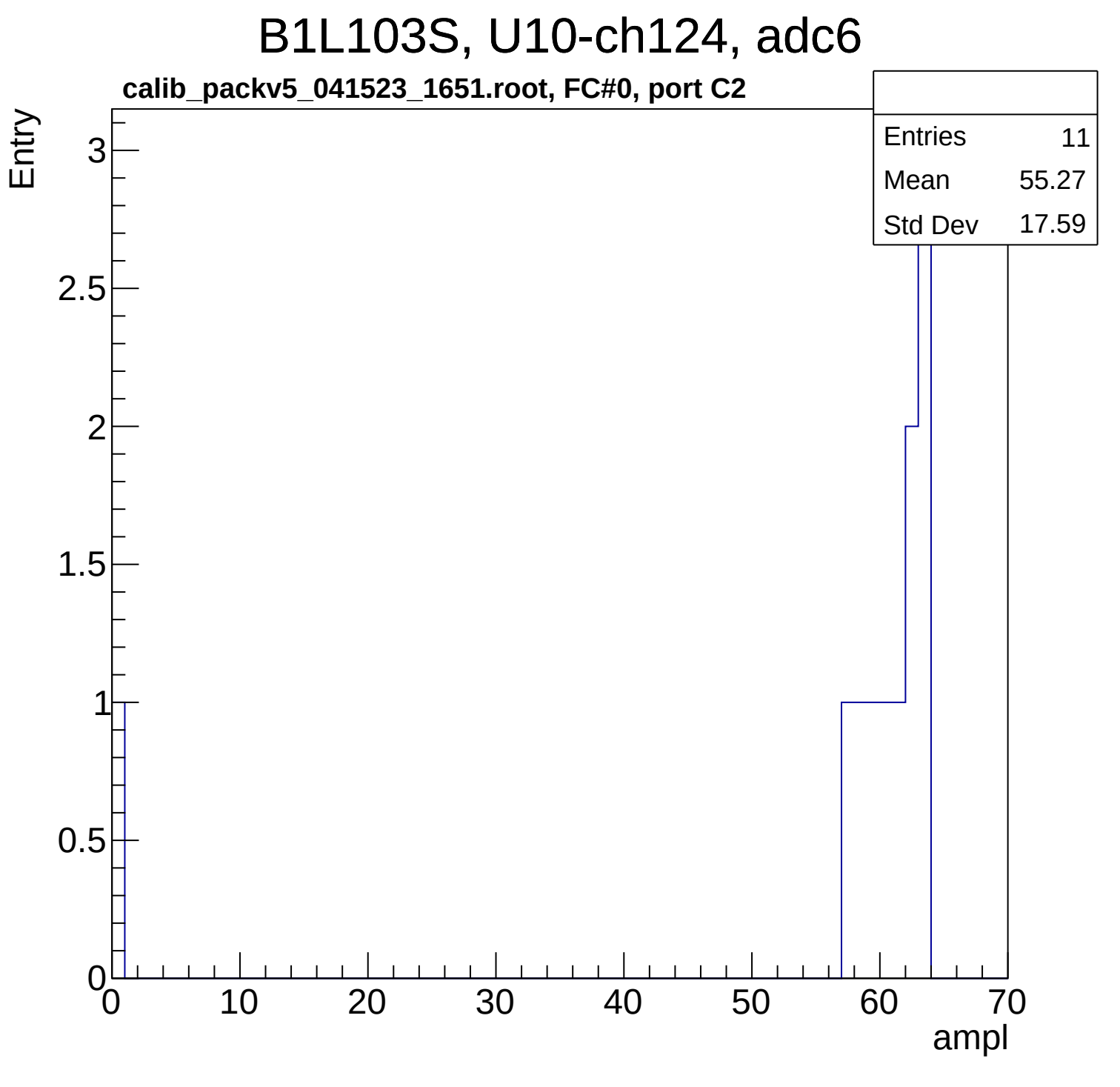
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

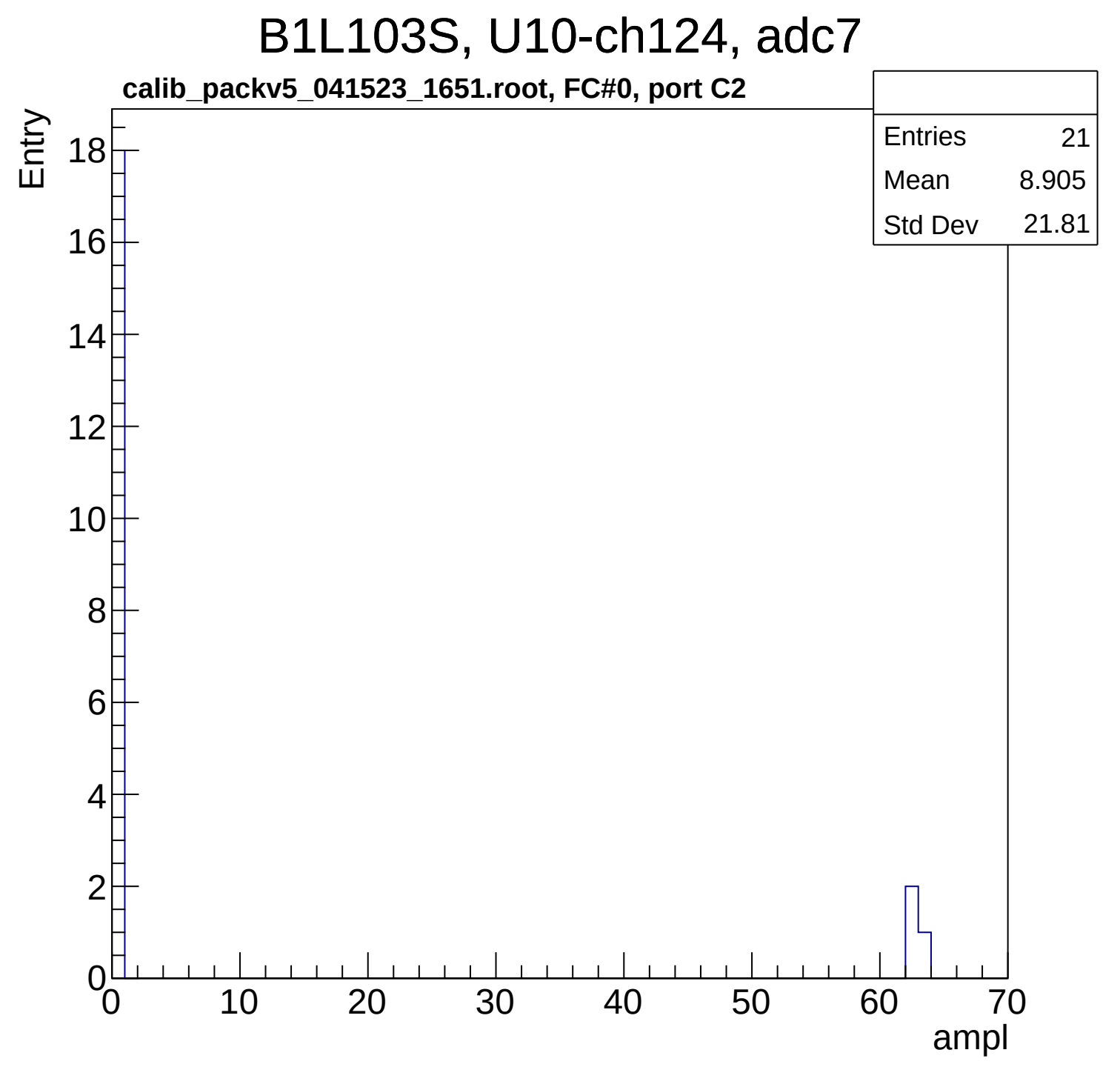

B1L103S, U10-ch124, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 37.72
Std Dev 13.42
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U10-ch124, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 48.73
Std Dev 3.768
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U10-ch124, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 53.58
Std Dev 3.436
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U10-ch124, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 59.37
Std Dev 2.587
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U10-ch124, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 55.27
Std Dev 17.59
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U10-ch124, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 8.905
Std Dev 21.81
Entry
ampl
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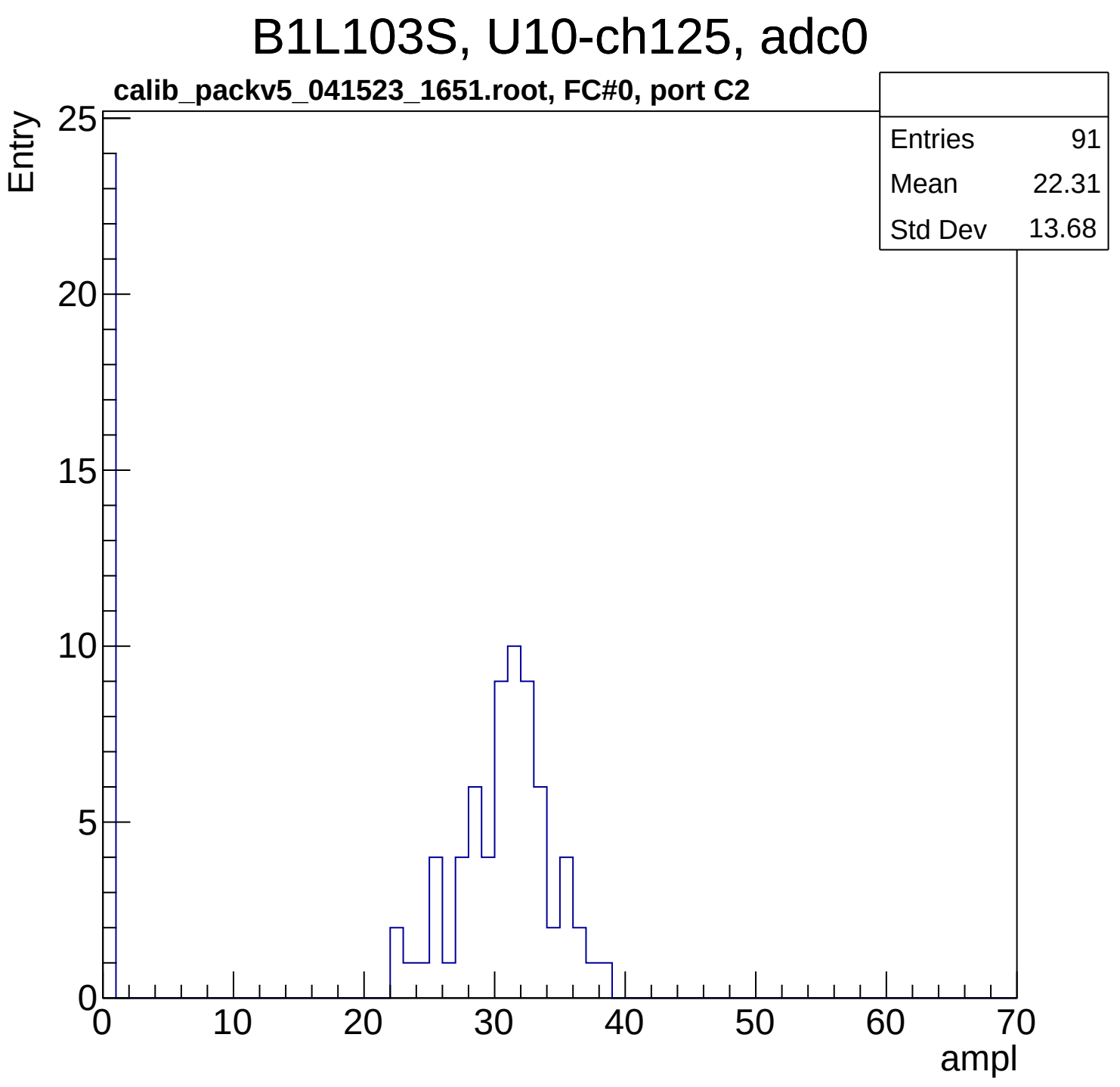
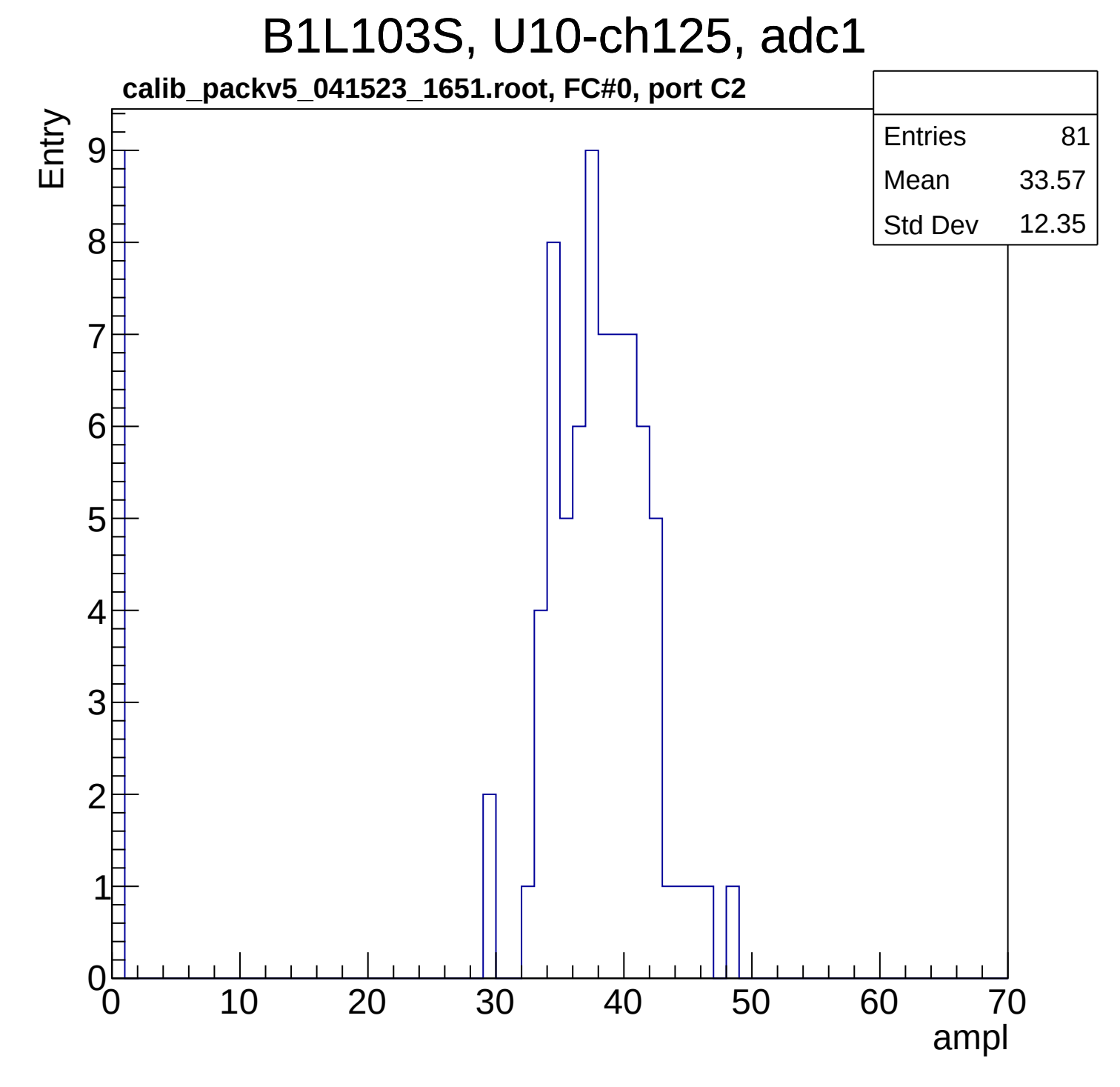
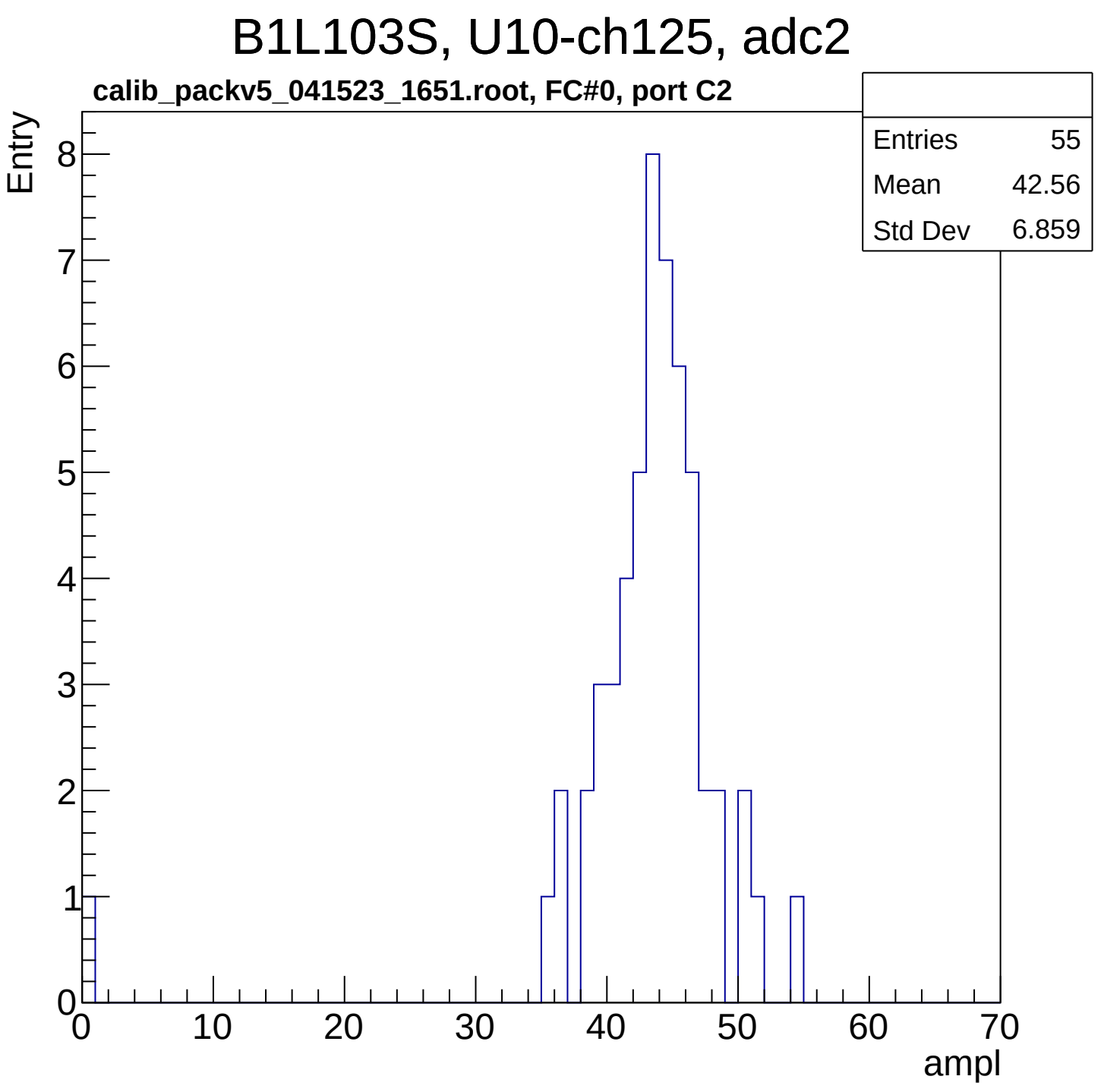
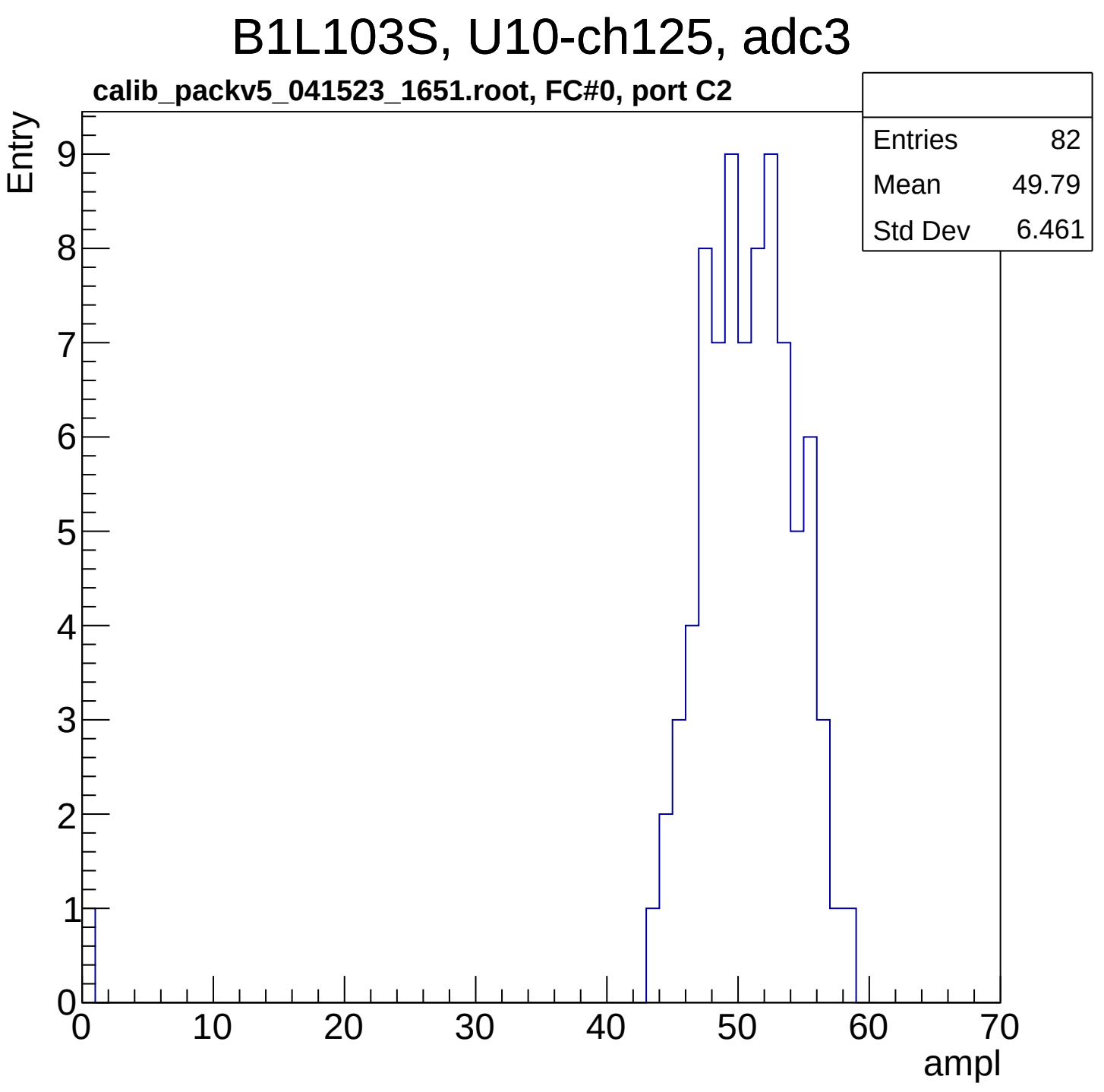
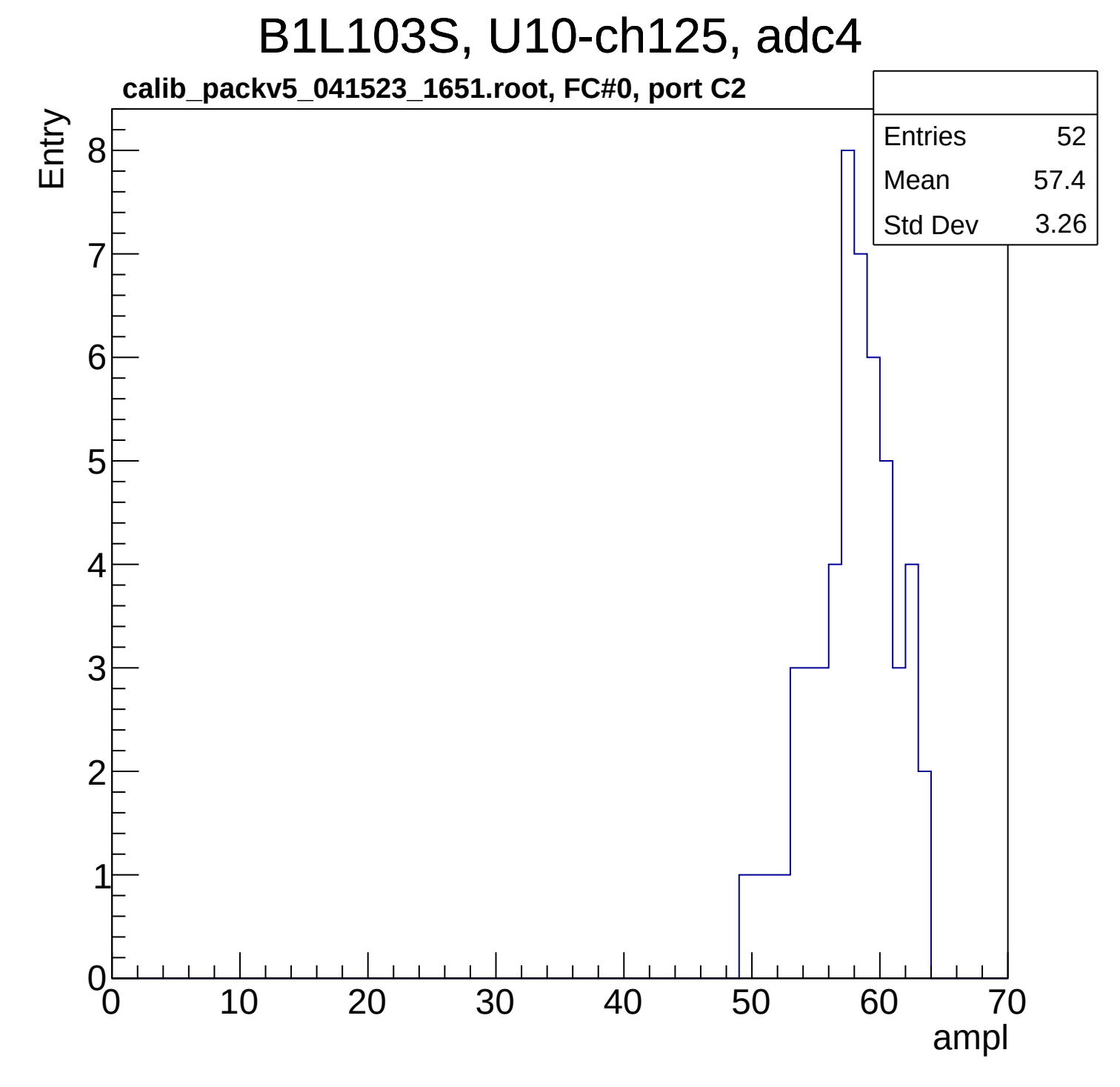
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

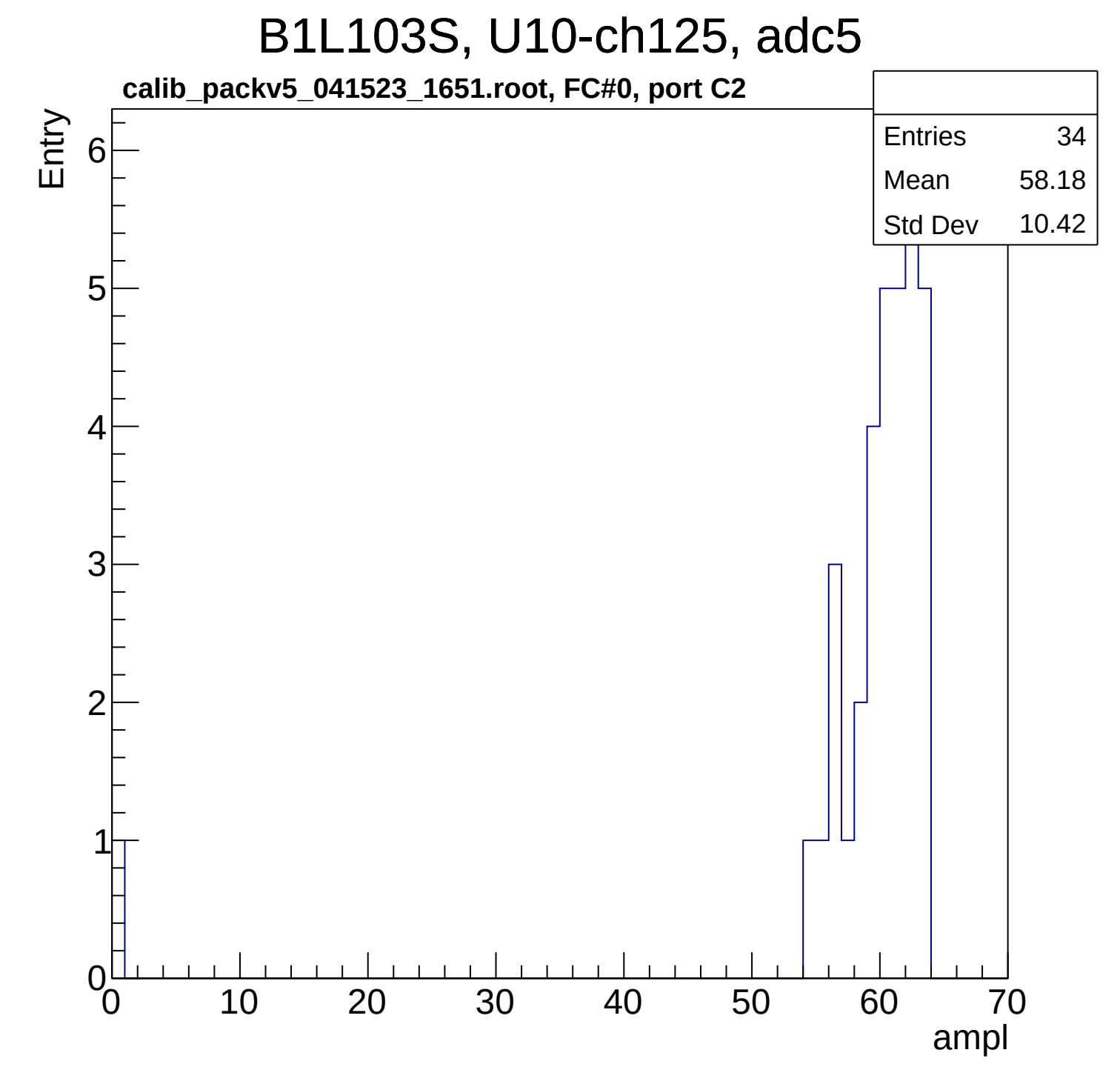

B1L103S, U10-ch125, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 91
Mean 22.31
Std Dev 13.68
Entry
ampl
0
5
10
15
20
25
0
10
20
30
40
50
60
70

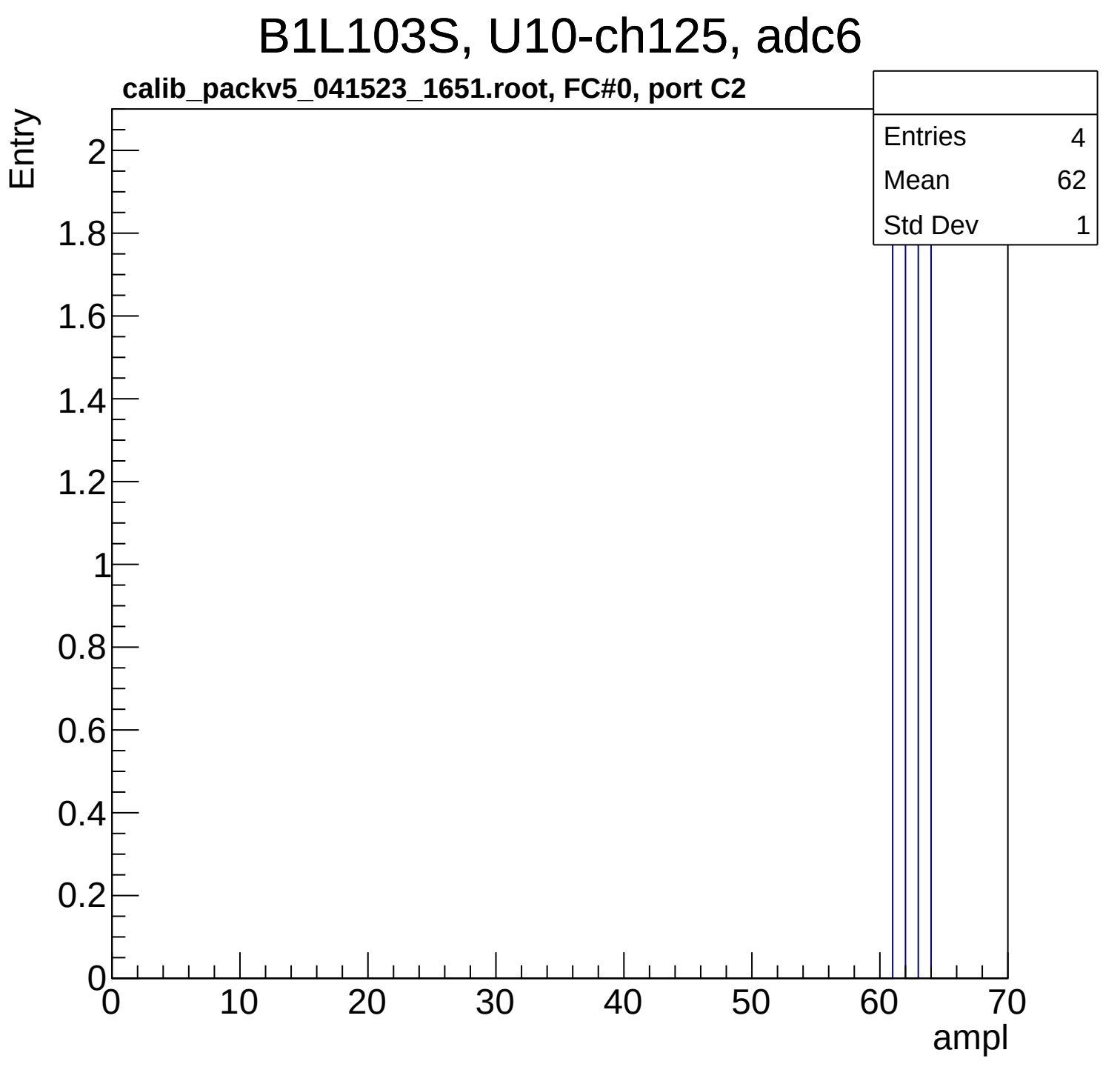

B1L103S, U10-ch125, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 33.57
Std Dev 12.35
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

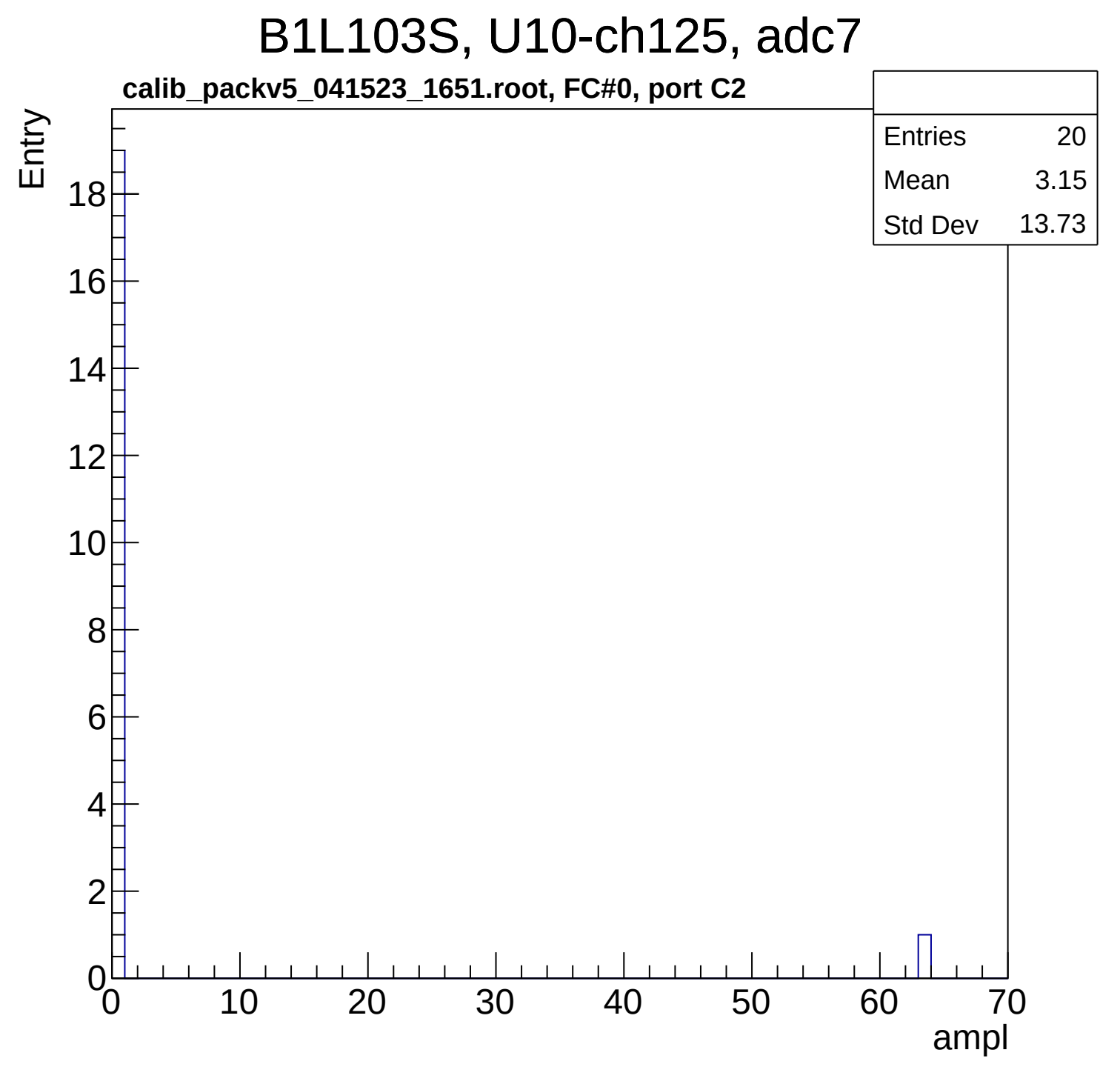

B1L103S, U10-ch125, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 42.56
Std Dev 6.859
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

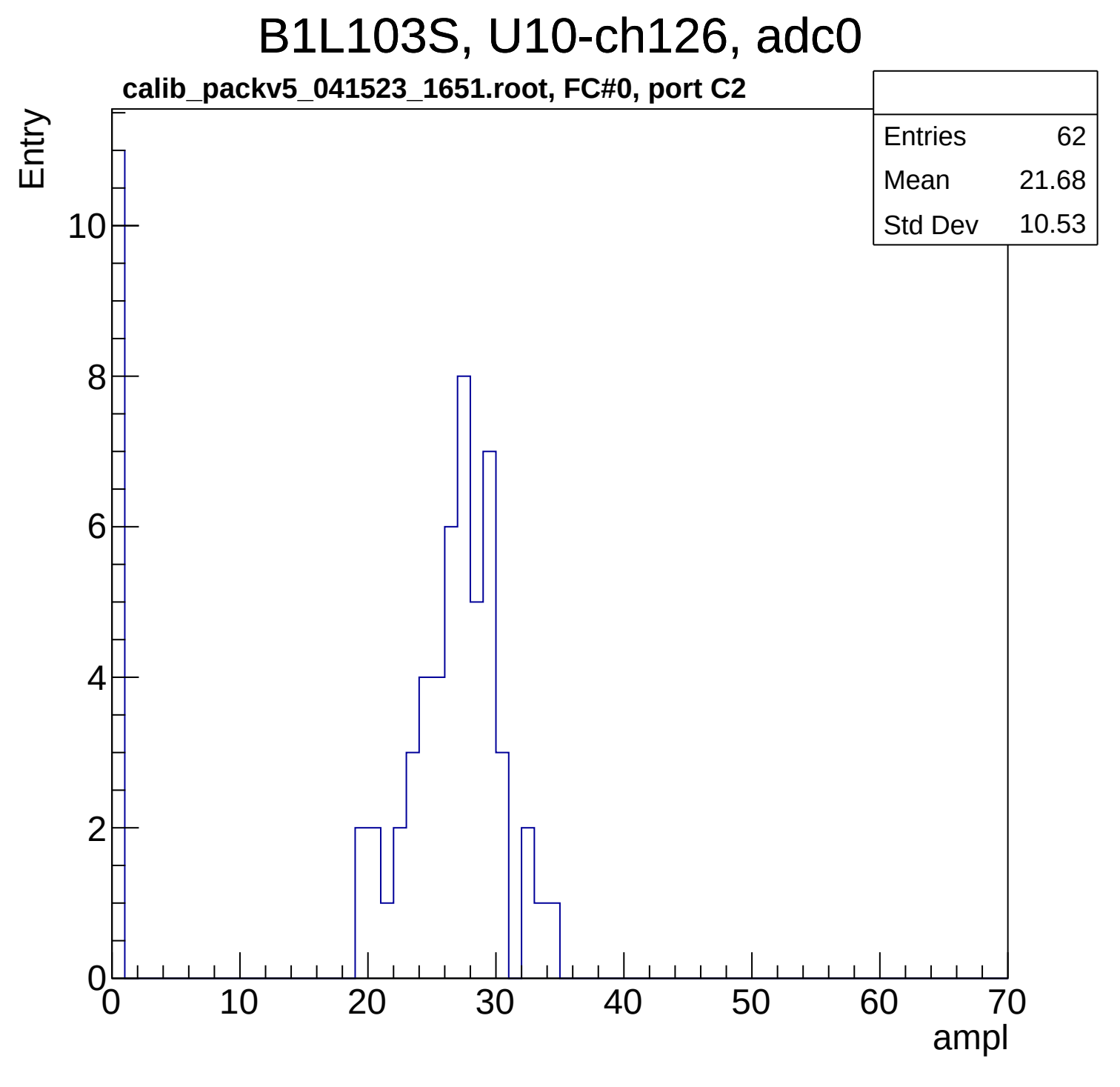

B1L103S, U10-ch125, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 49.79
Std Dev 6.461
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

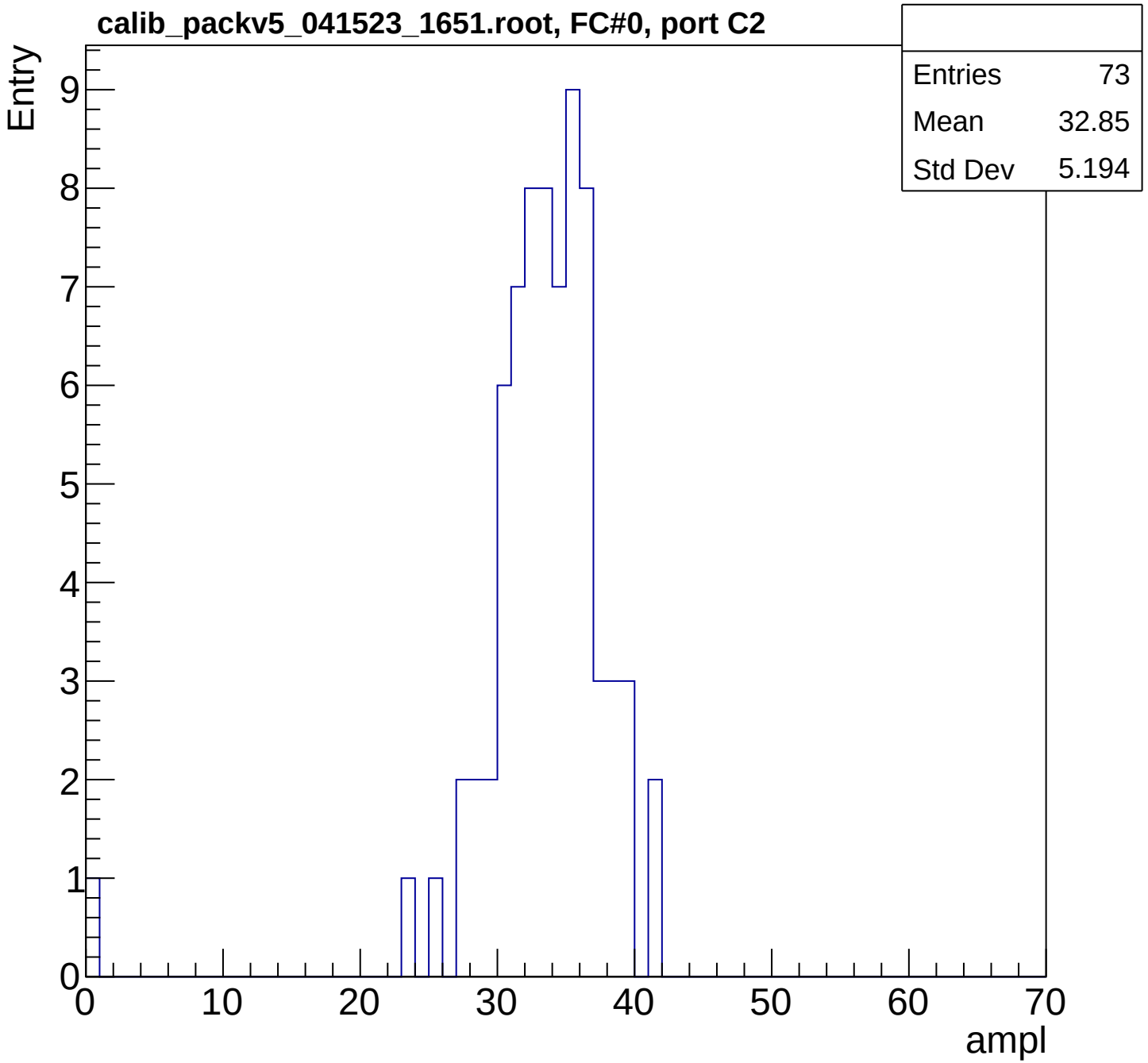

B1L103S, U10-ch125, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 57.4
Std Dev 3.26
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

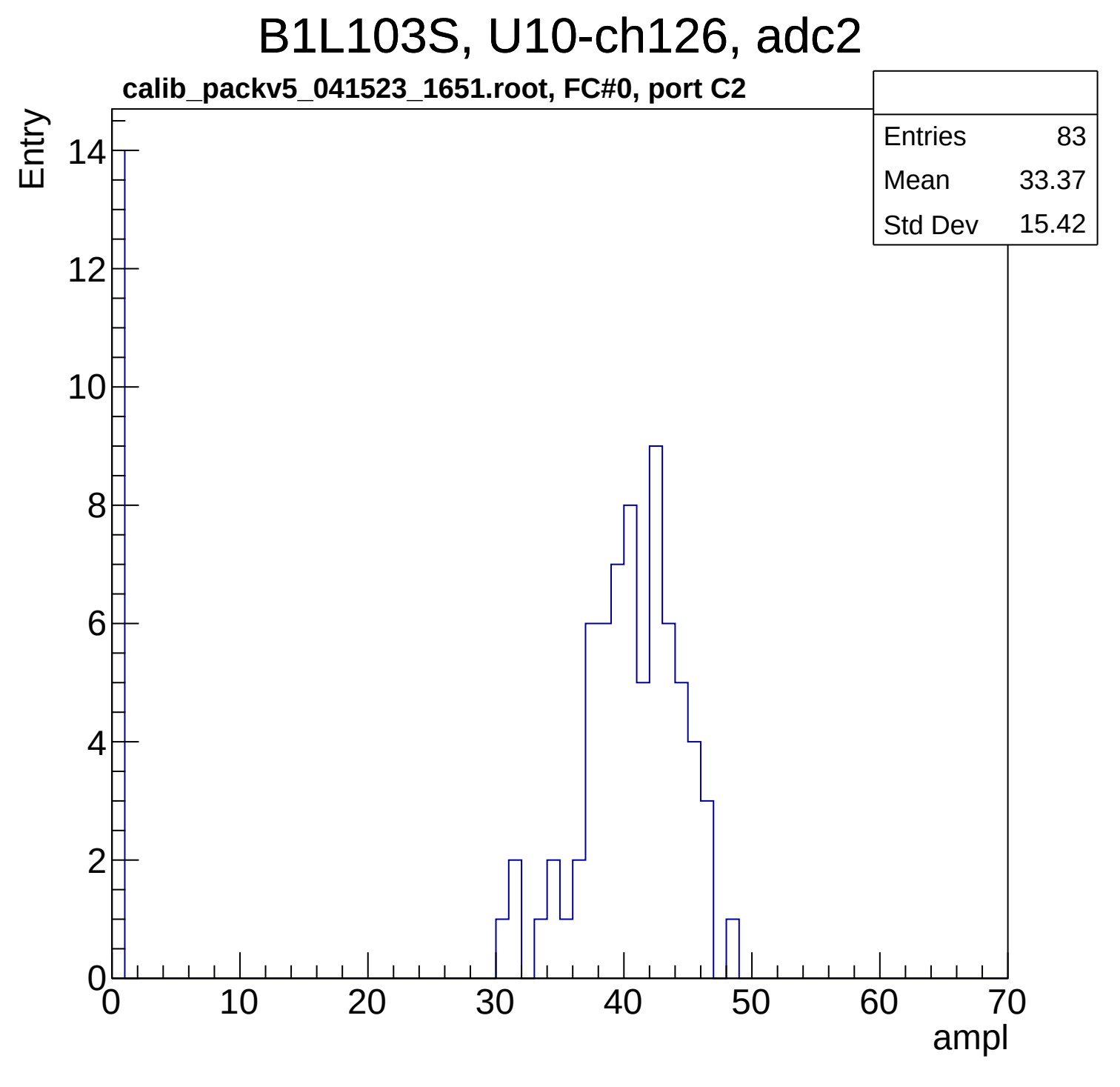

B1L103S, U10-ch125, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 34
Mean 58.18
Std Dev 10.42
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl

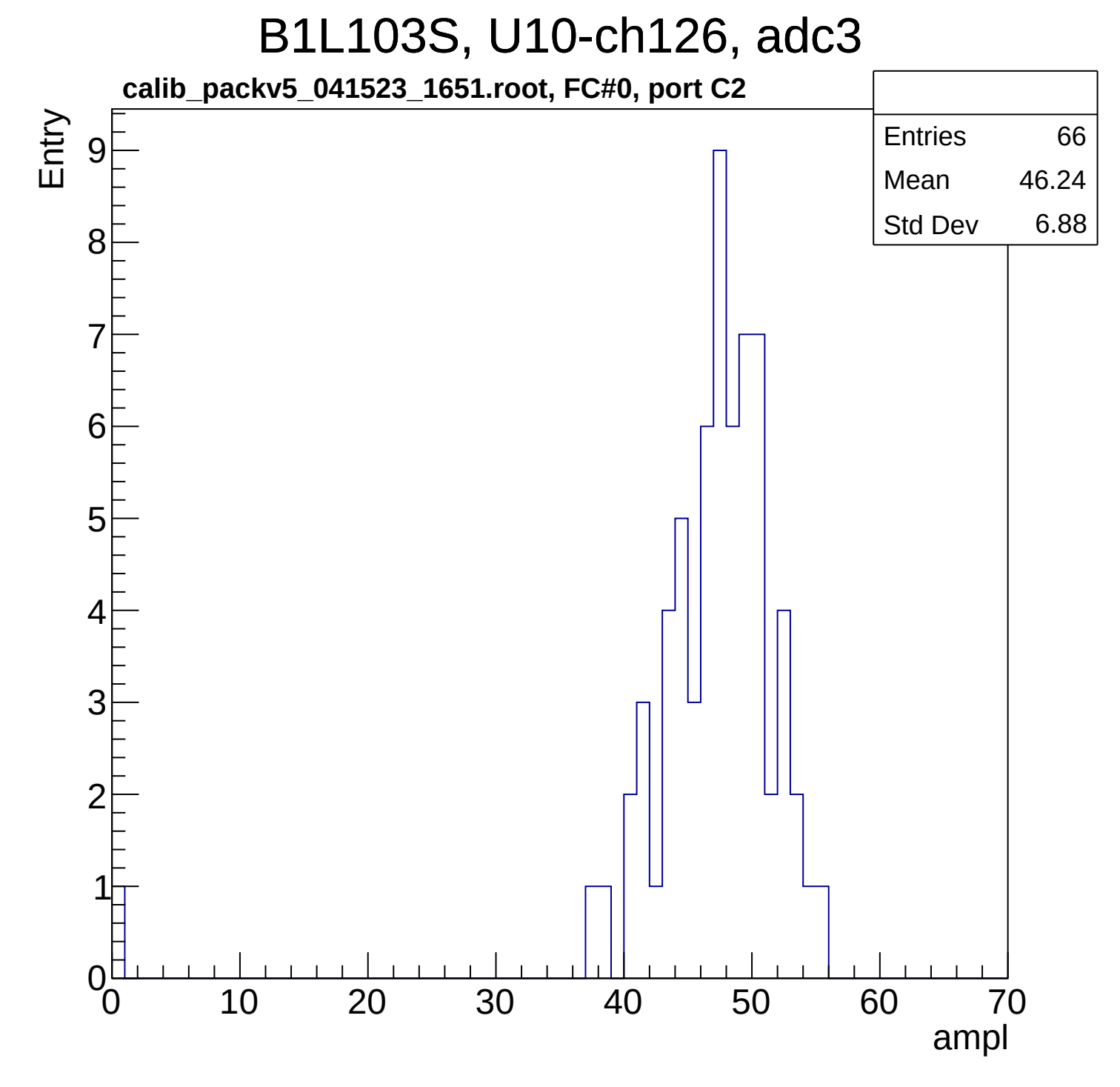

B1L103S, U10-ch125, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 4
Mean 62
Std Dev 1
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U10-ch125, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch126, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 21.68
Std Dev 10.53
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U10-ch126, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 32.85
Std Dev 5.194
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U10-ch126, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 33.37
Std Dev 15.42
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L103S, U10-ch126, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 46.24
Std Dev 6.88
Entry
ampl
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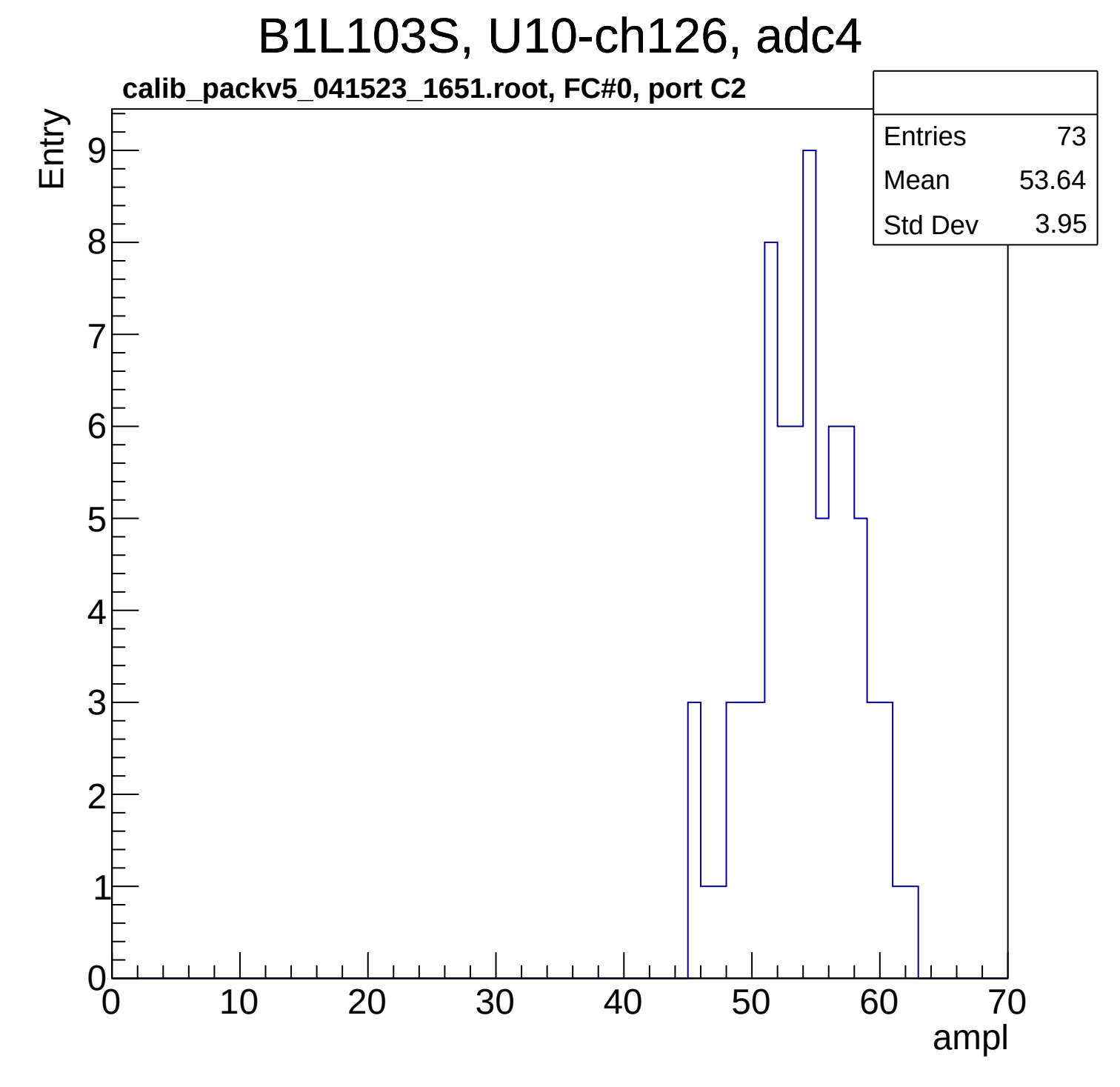
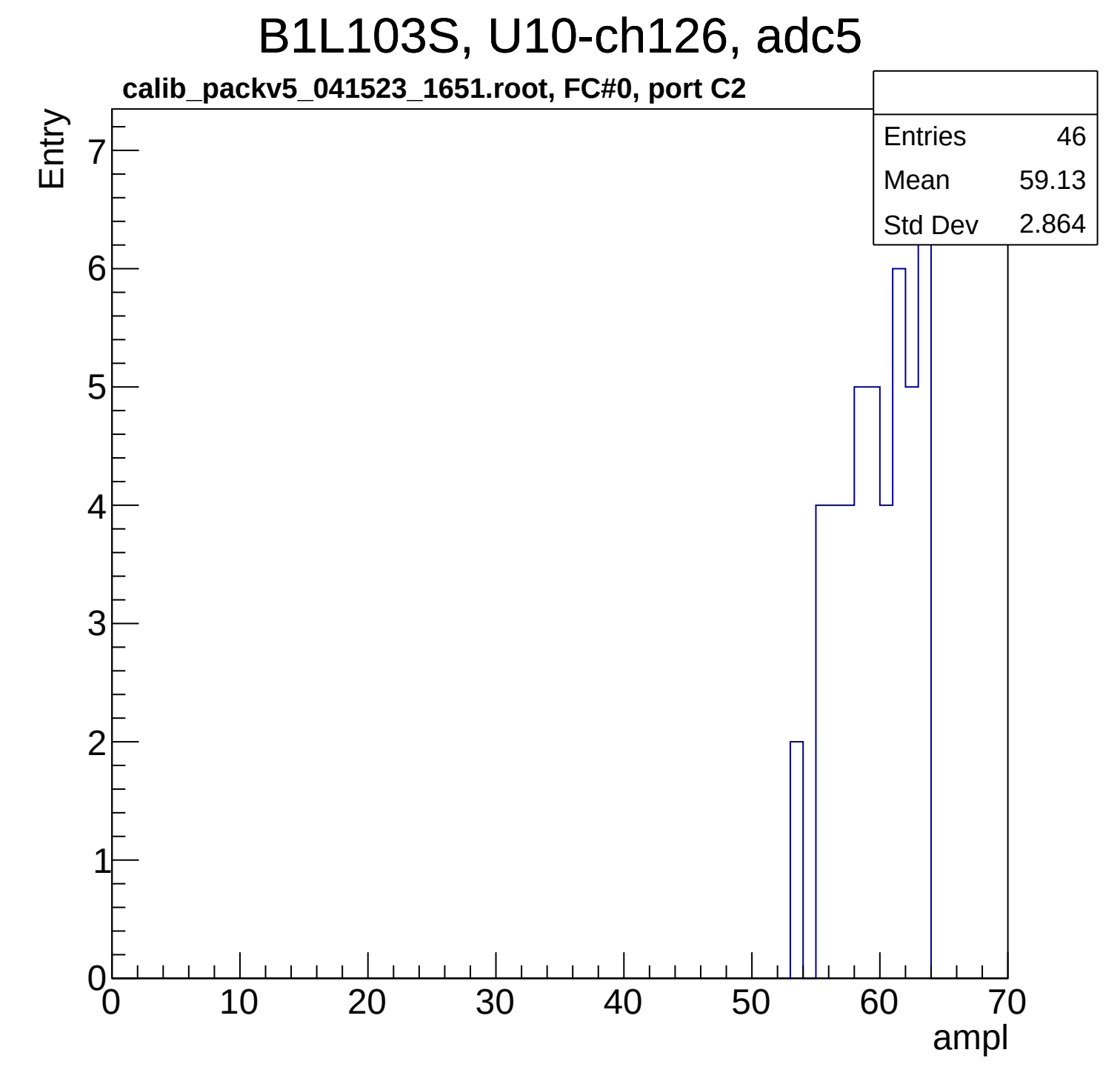
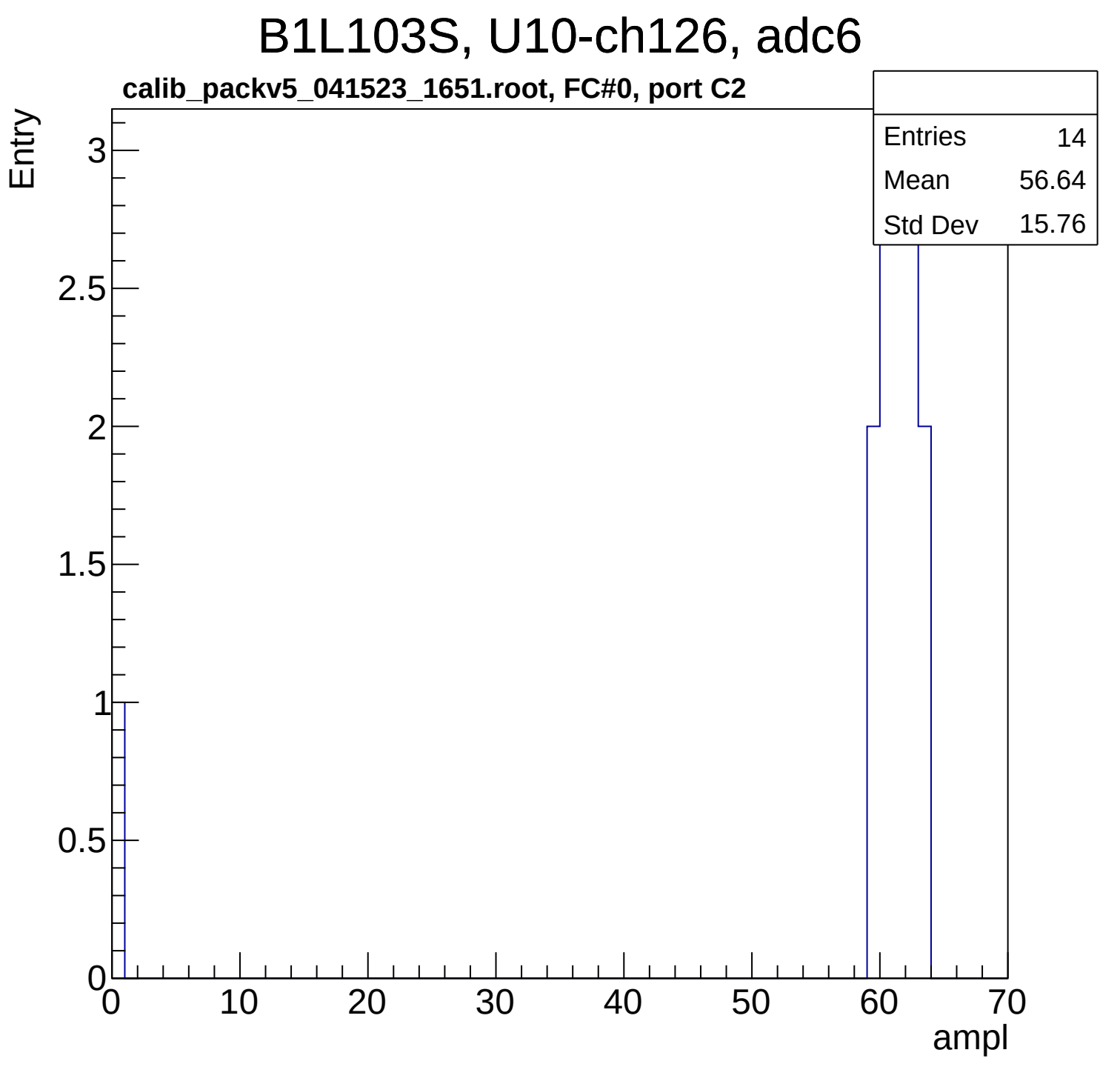
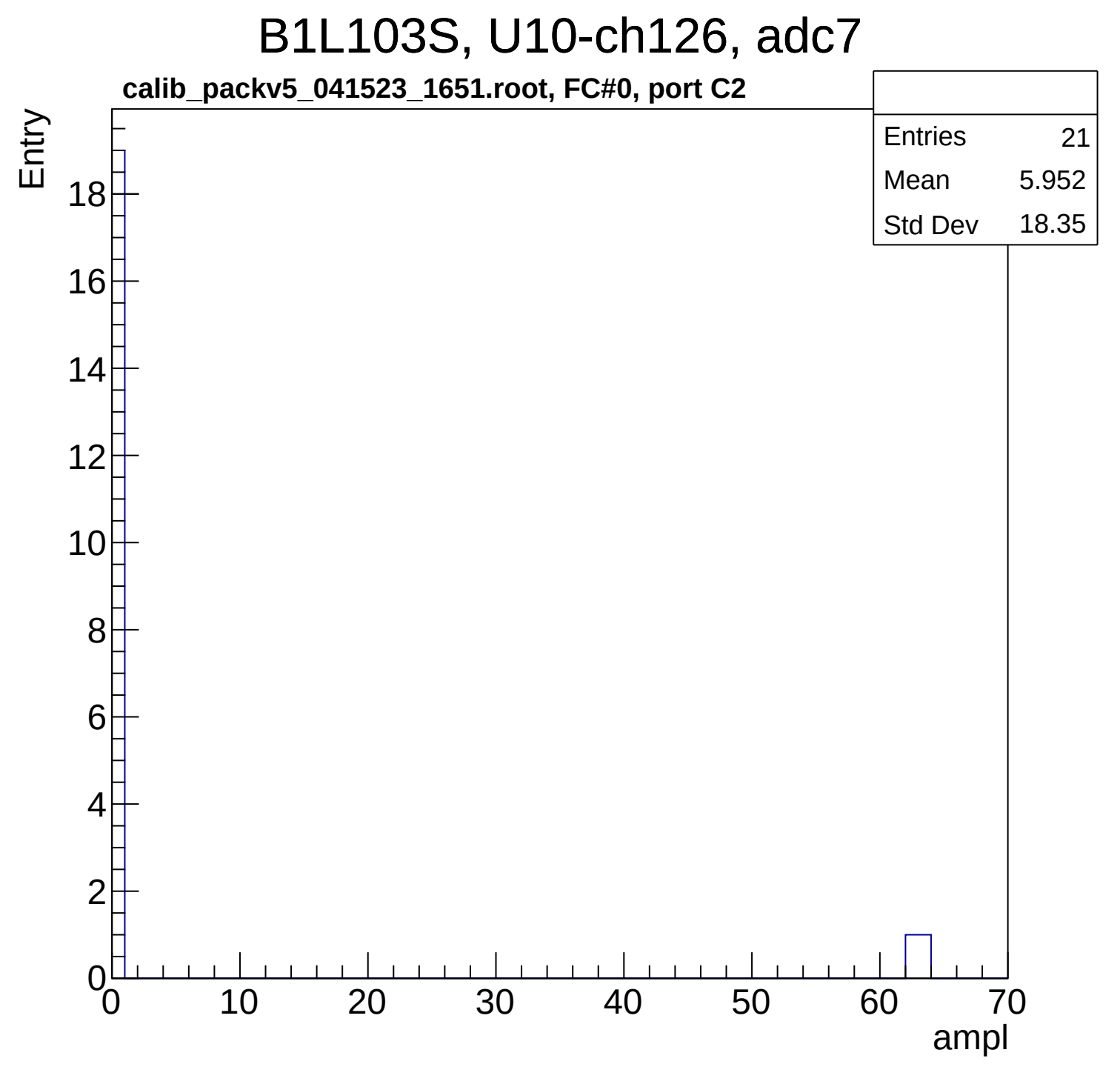
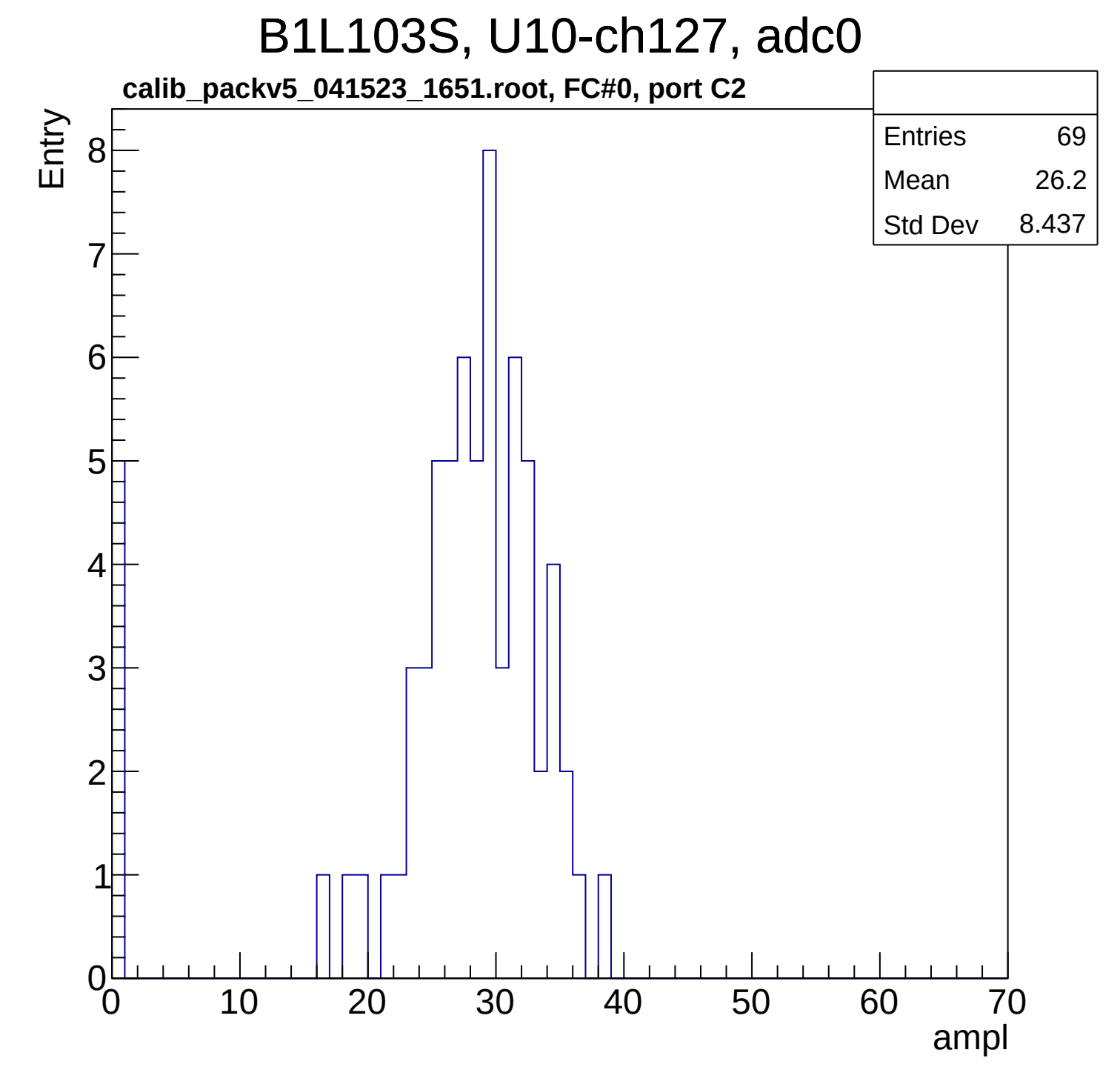
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

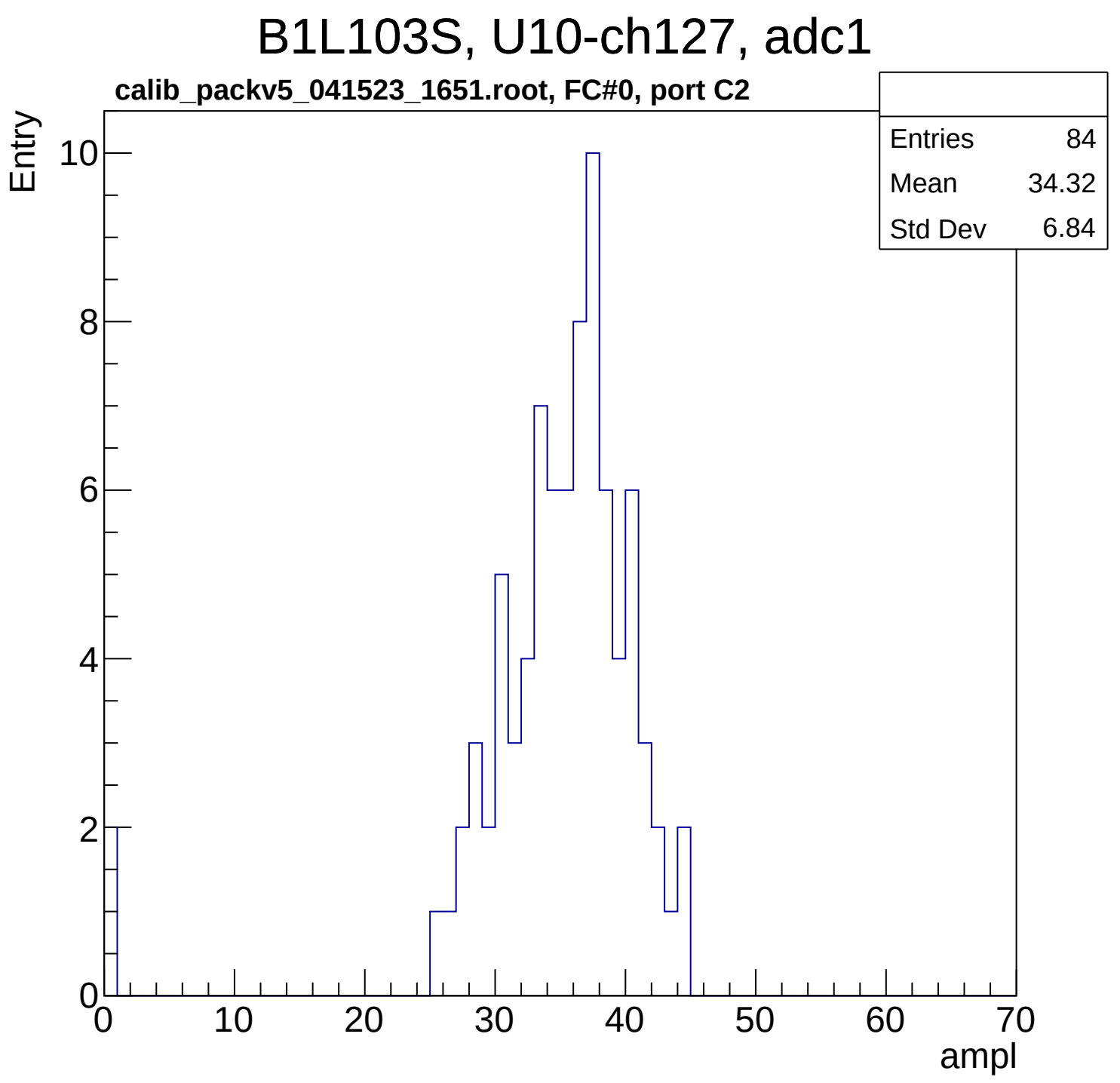

B1L103S, U10-ch126, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 53.64
Std Dev 3.95
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

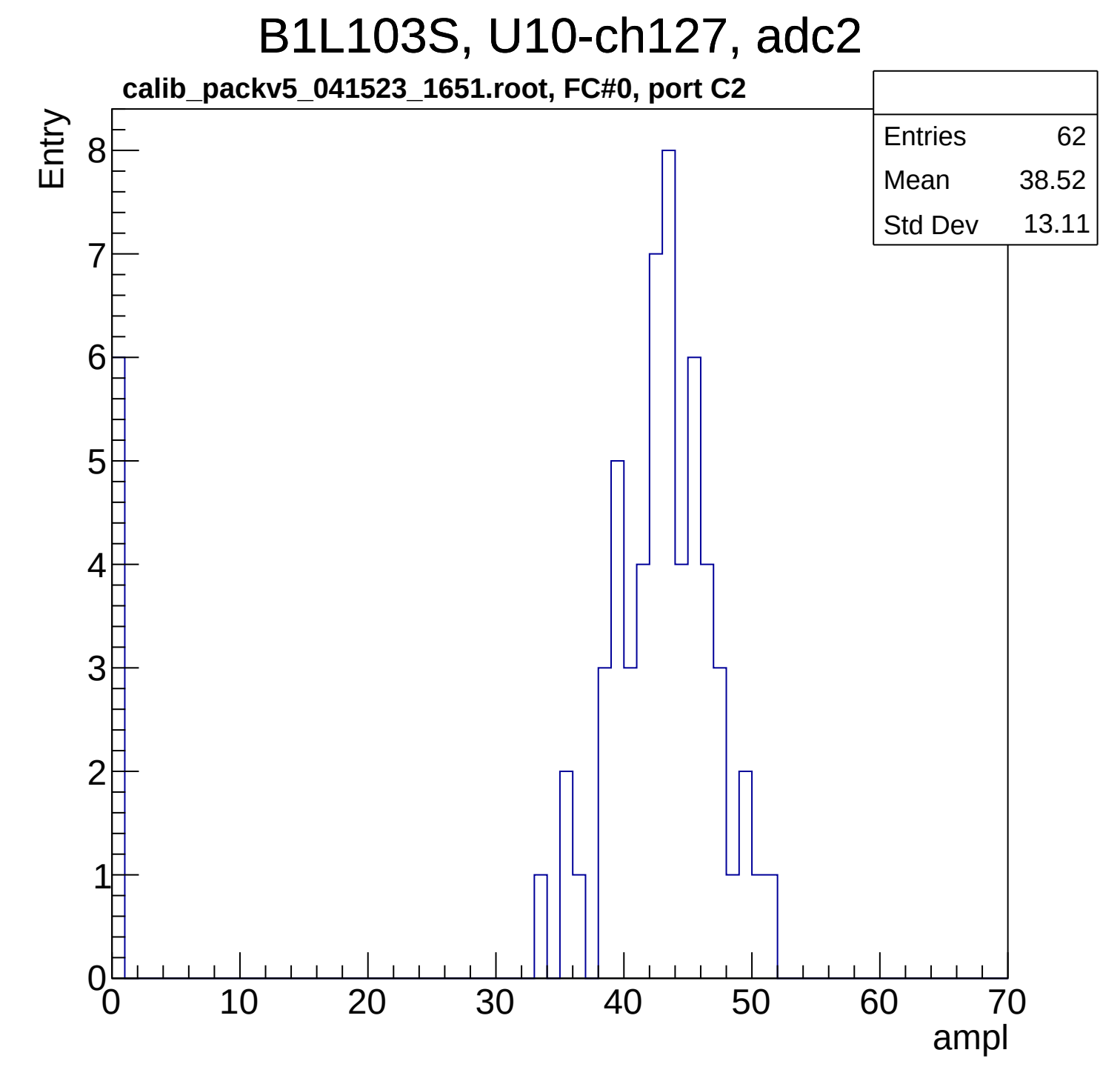

B1L103S, U10-ch126, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 59.13
Std Dev 2.864
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

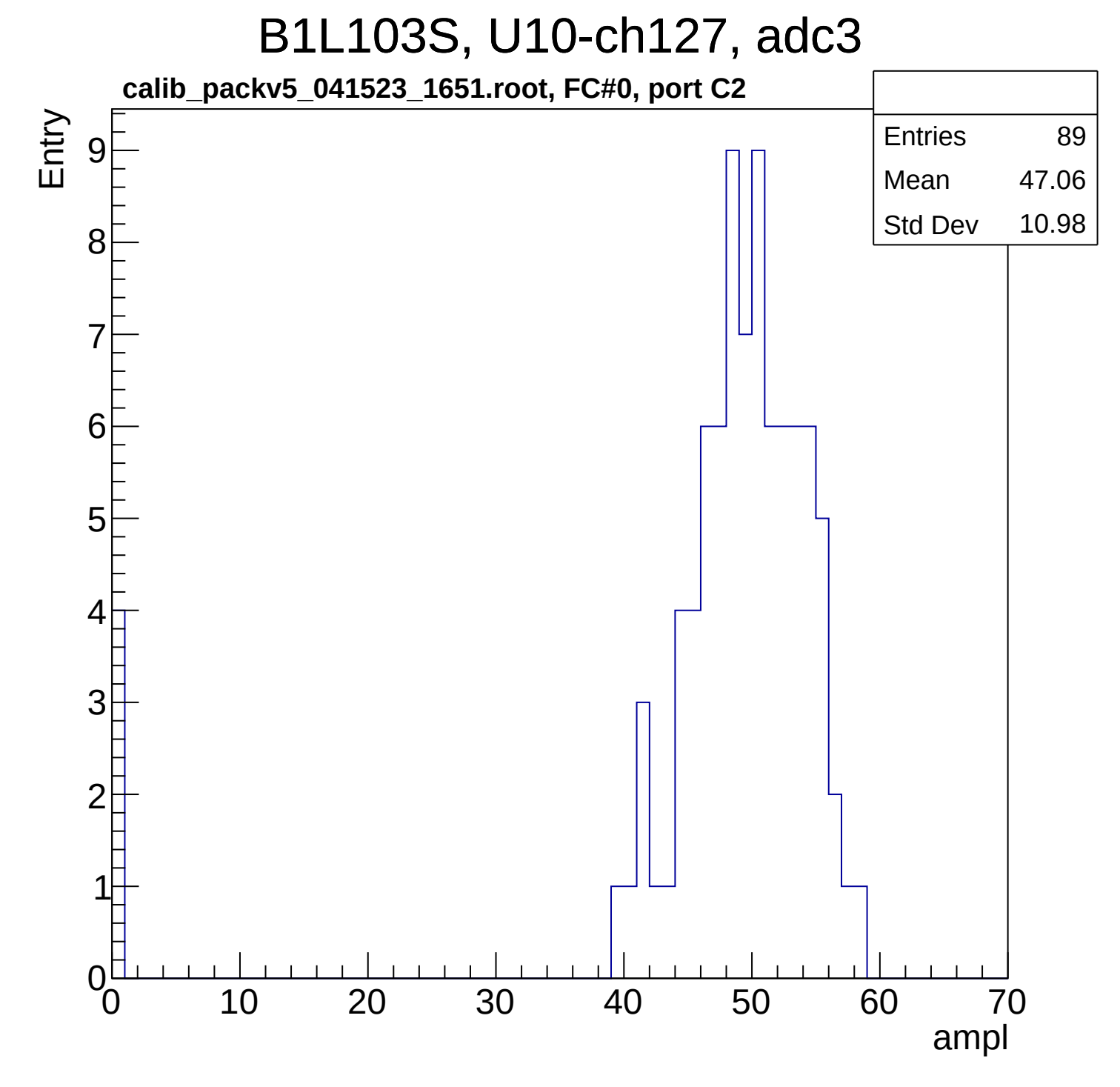

B1L103S, U10-ch126, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 14
Mean 56.64
Std Dev 15.76
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

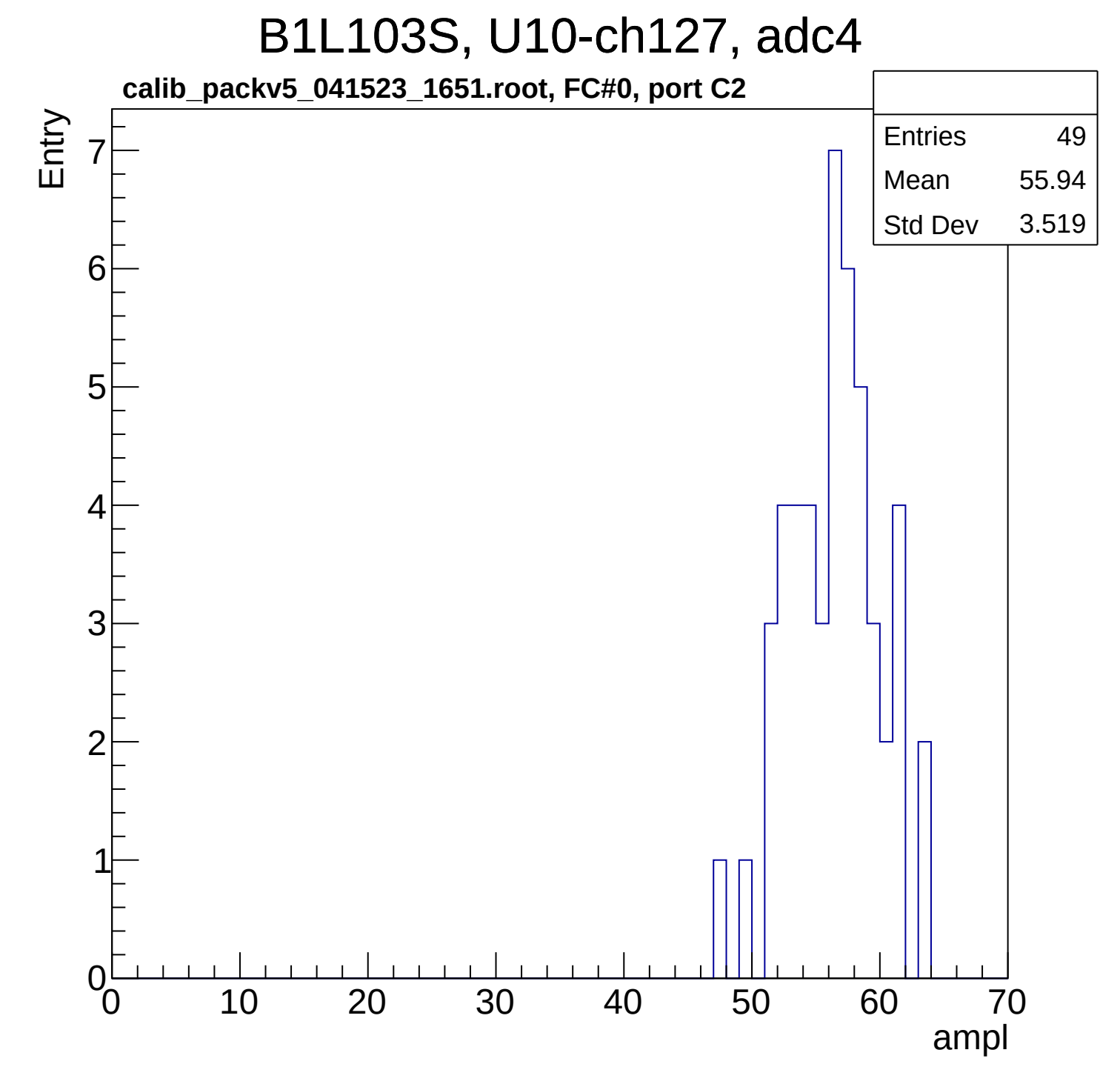

B1L103S, U10-ch126, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 5.952
Std Dev 18.35
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

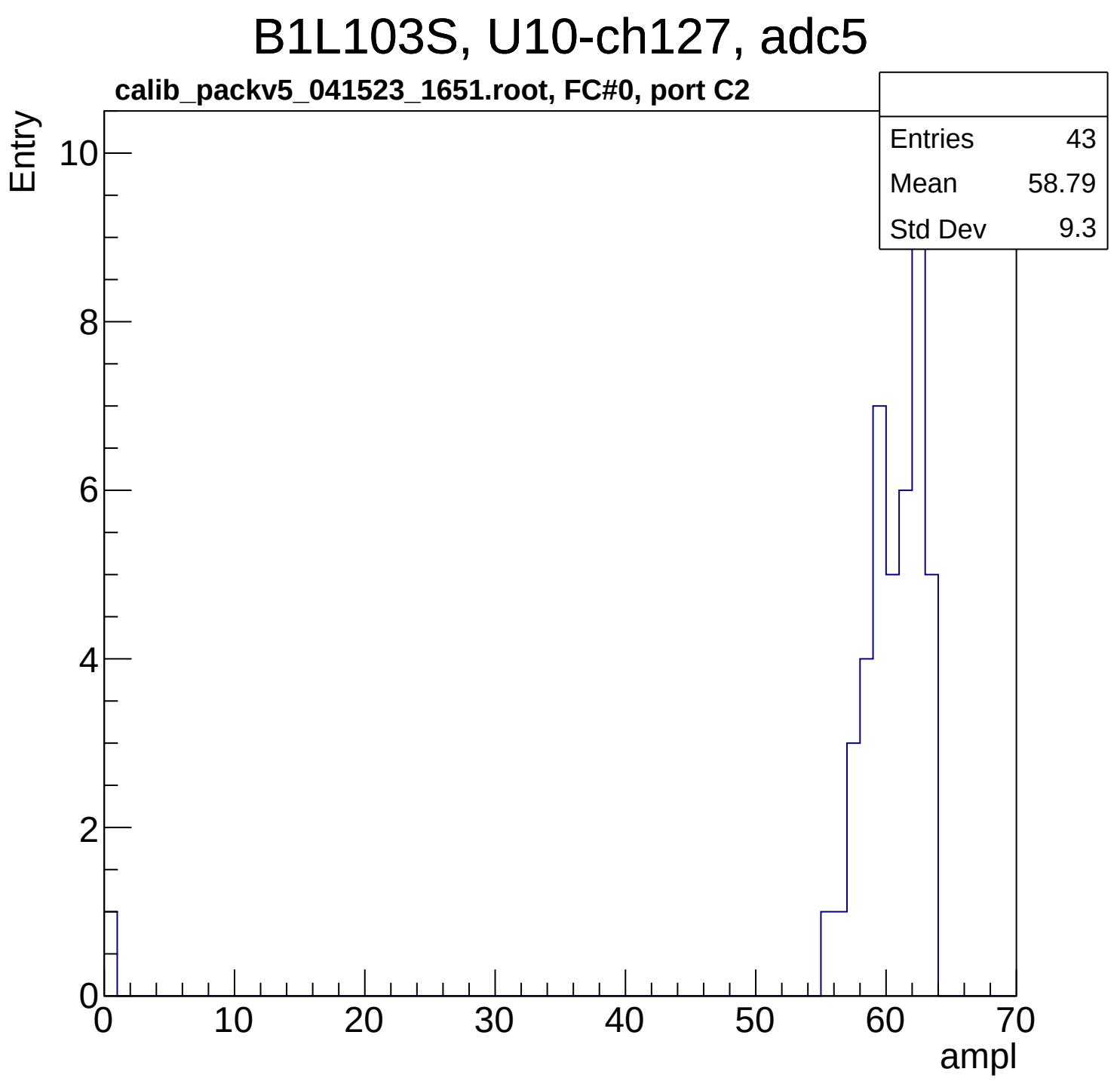

B1L103S, U10-ch127, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 26.2
Std Dev 8.437
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

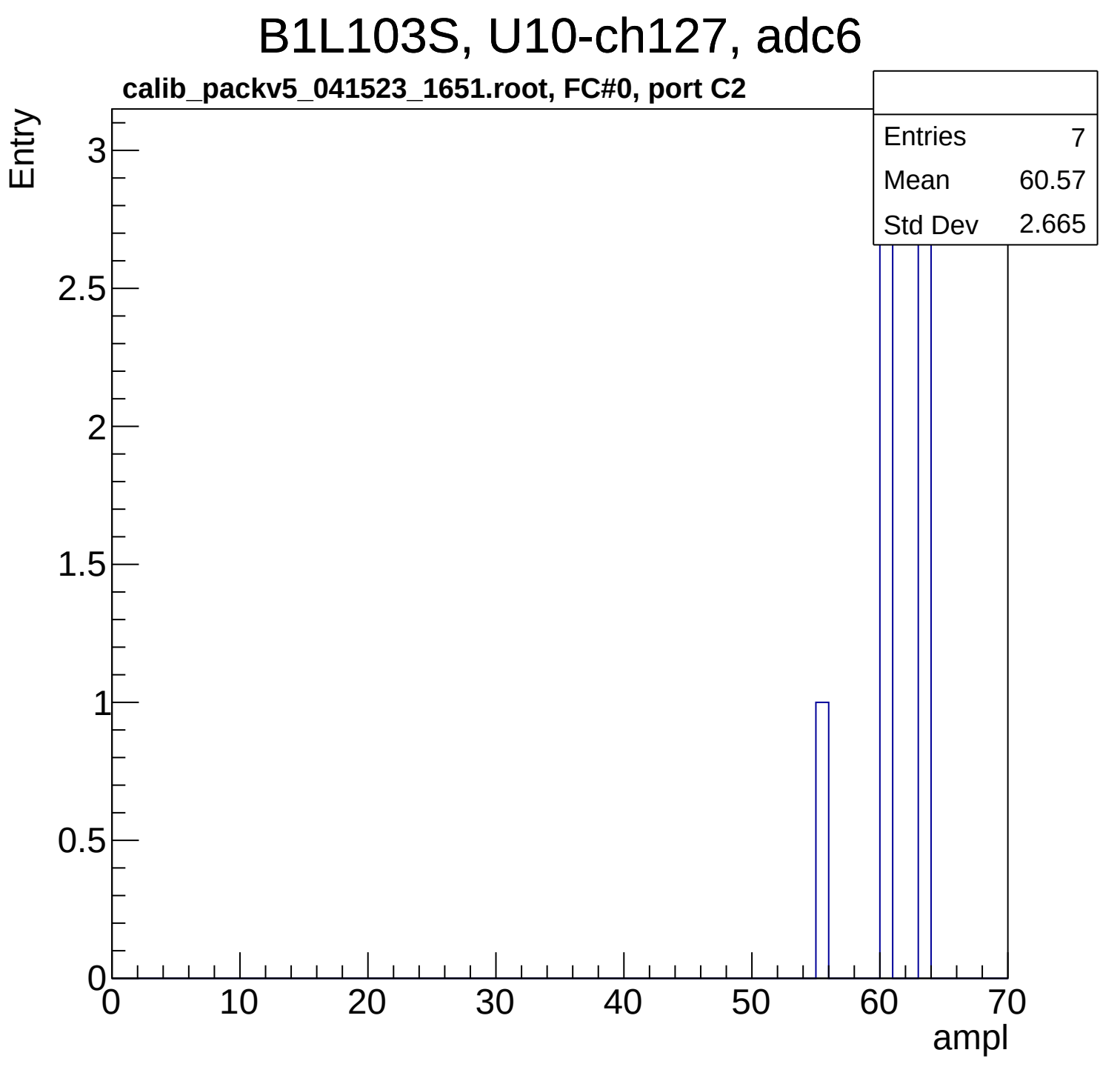

B1L103S, U10-ch127, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 34.32
Std Dev 6.84
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

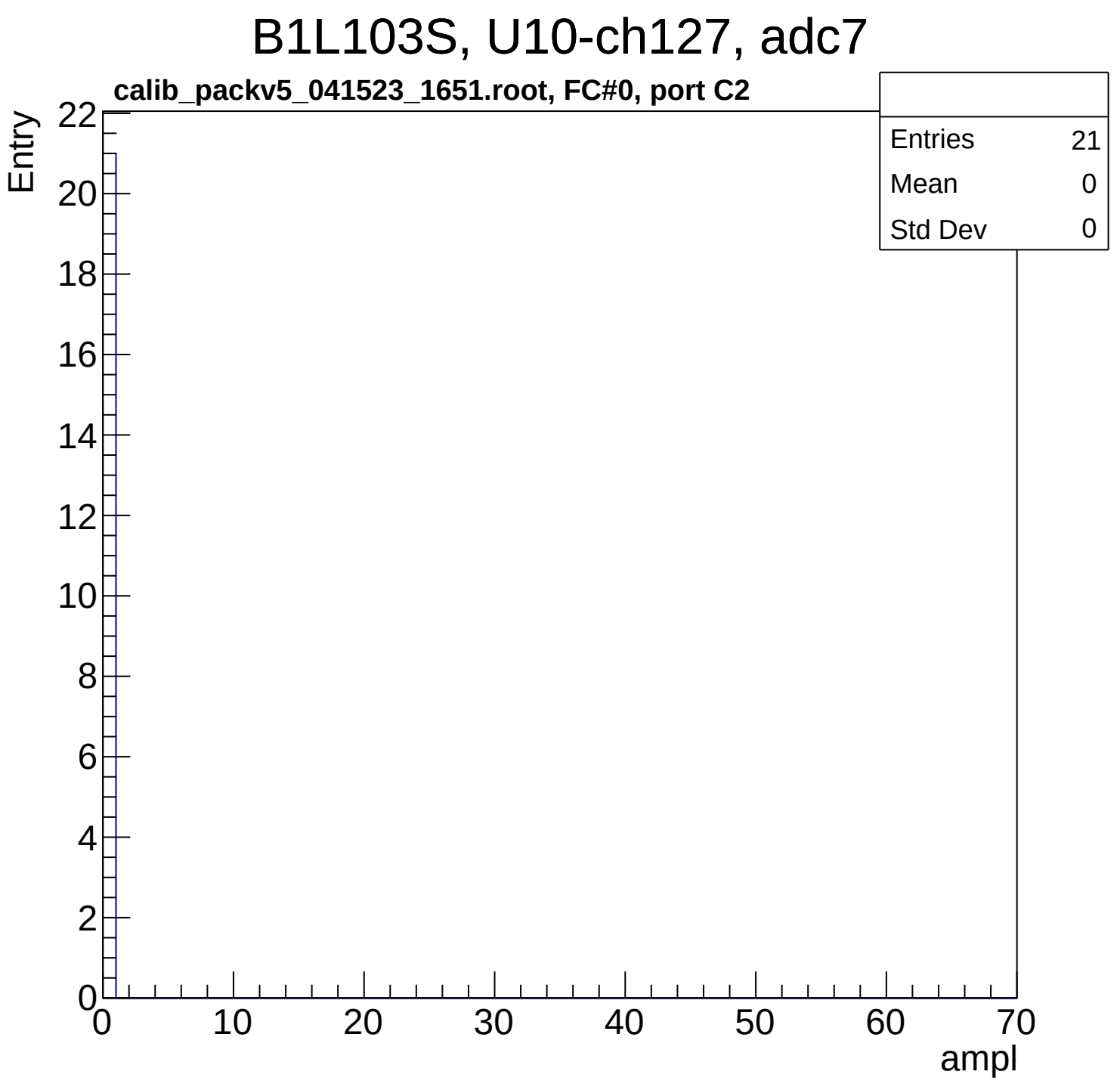

B1L103S, U10-ch127, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 38.52
Std Dev 13.11
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

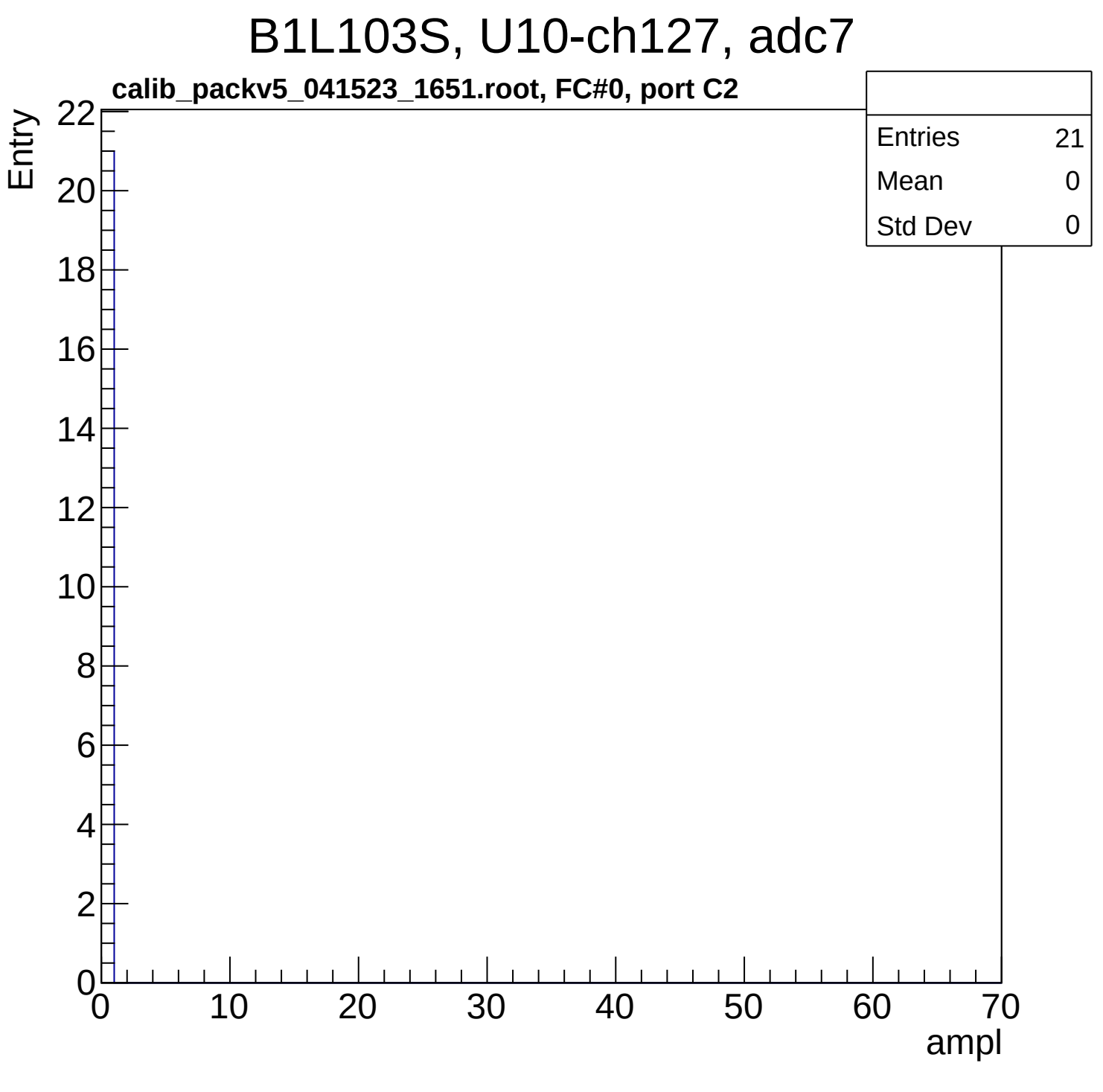

B1L103S, U10-ch127, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 89
Mean 47.06
Std Dev 10.98
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U10-ch127, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 55.94
Std Dev 3.519
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U10-ch127, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 43
Mean 58.79
Std Dev 9.3
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U10-ch127, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 60.57
Std Dev 2.665
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U10-ch127, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 0
Std Dev 0
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
22
0
10
20
30
40
50
60
70


B1L103S, U10-ch127, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 0
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Entry
ampl
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