



# B1L101S, U19-ch0, adc0

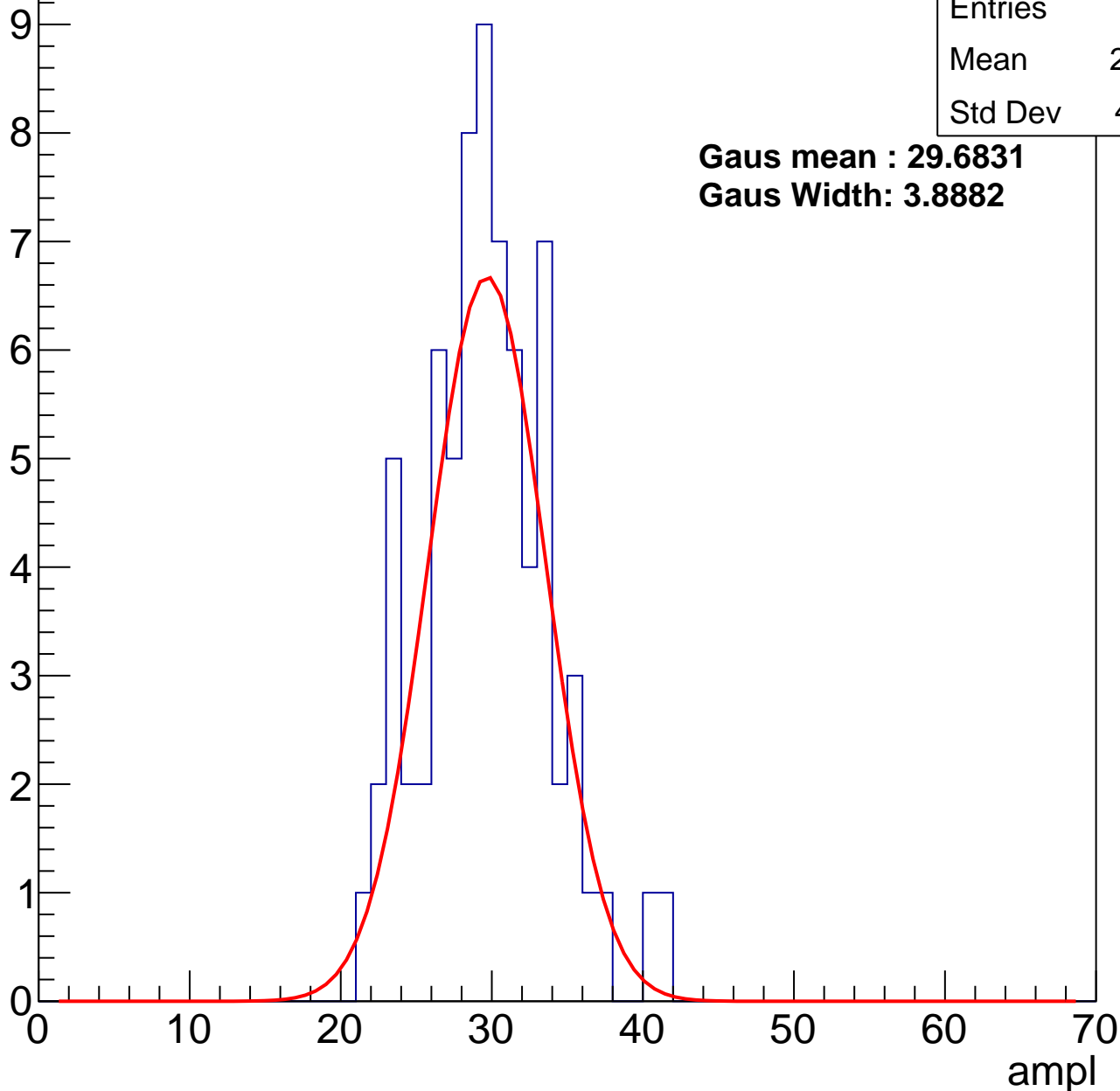
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	73
Mean	29.26
Std Dev	4.081

**Gaus mean : 29.6831**

**Gaus Width: 3.8882**



# B1L101S, U19-ch0, adc1

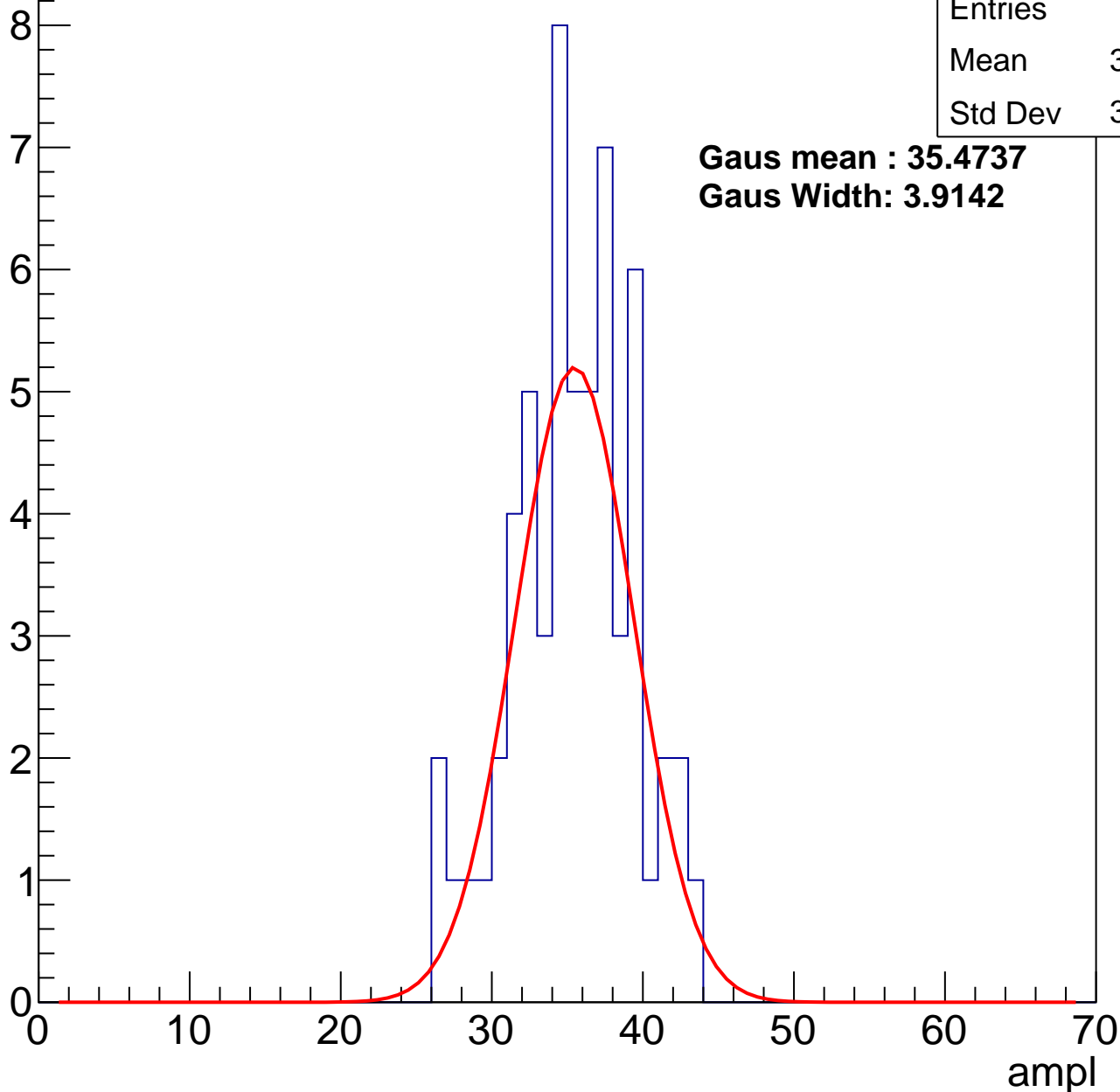
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	59
Mean	34.95
Std Dev	3.916

**Gaus mean : 35.4737**

**Gaus Width: 3.9142**



# B1L101S, U19-ch0, adc2

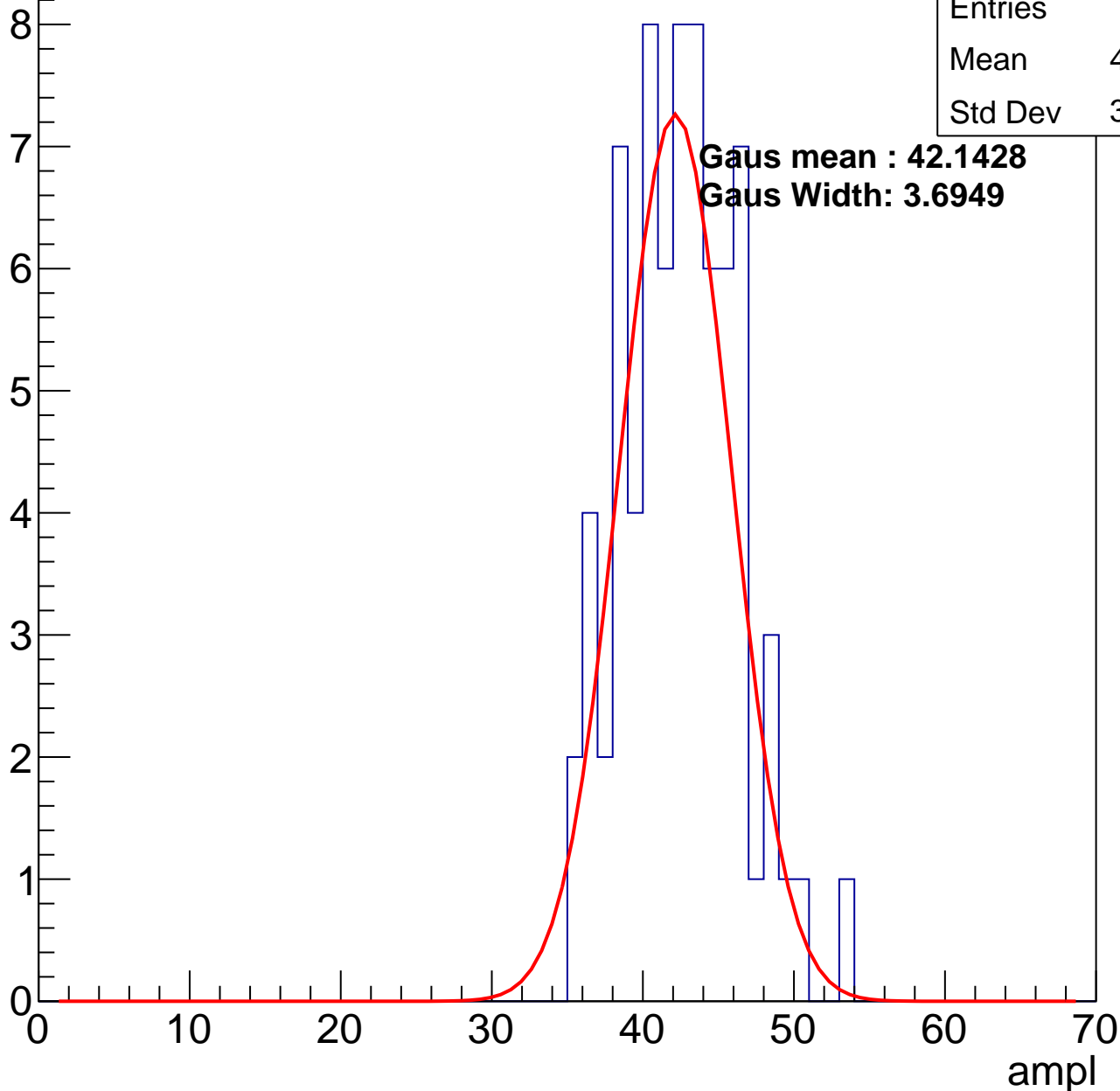
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	75
Mean	42.07
Std Dev	3.729

**Gaus mean : 42.1428**

**Gaus Width: 3.6949**

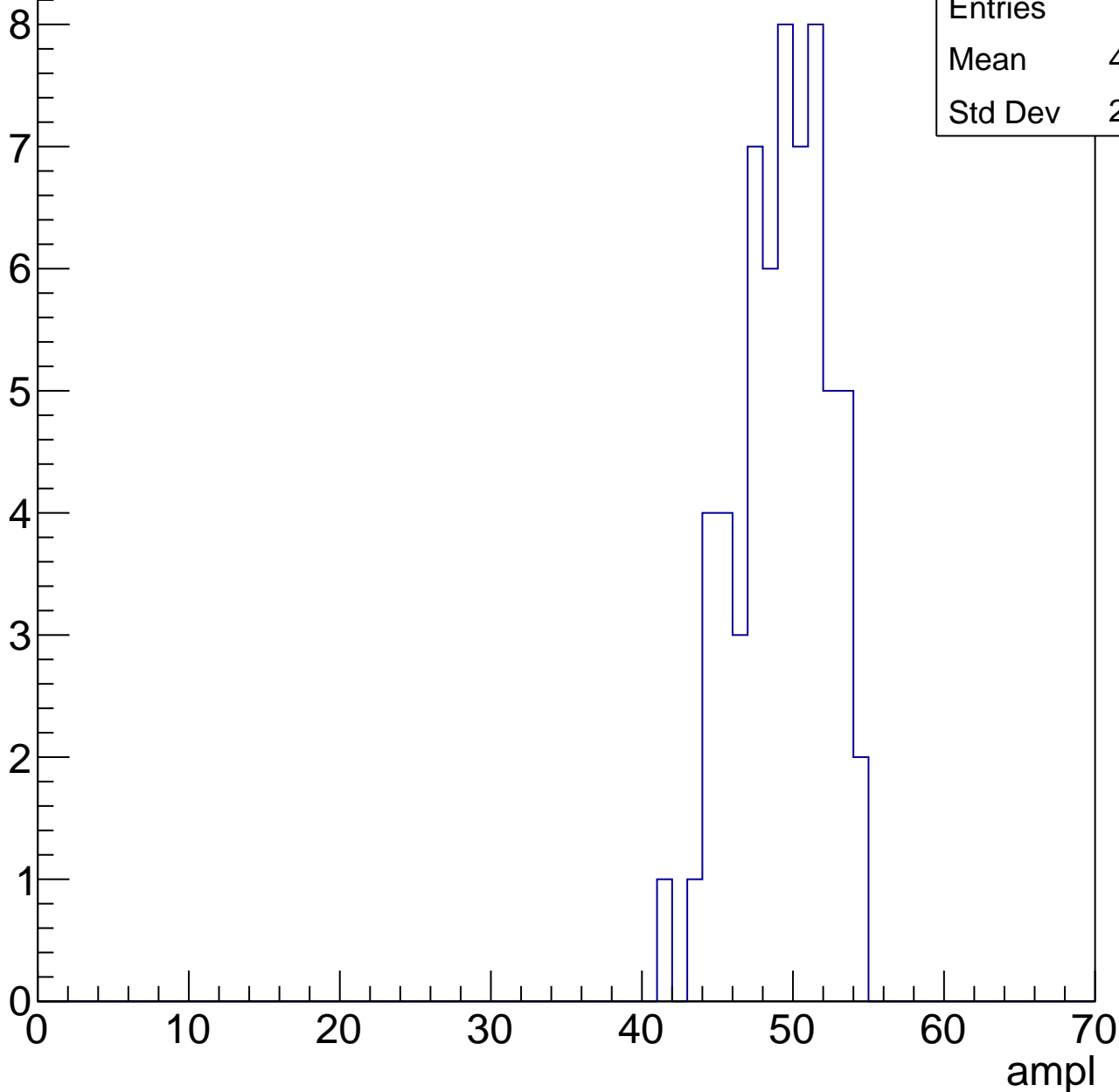


# B1L101S, U19-ch0, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	48.82
Std Dev	2.967

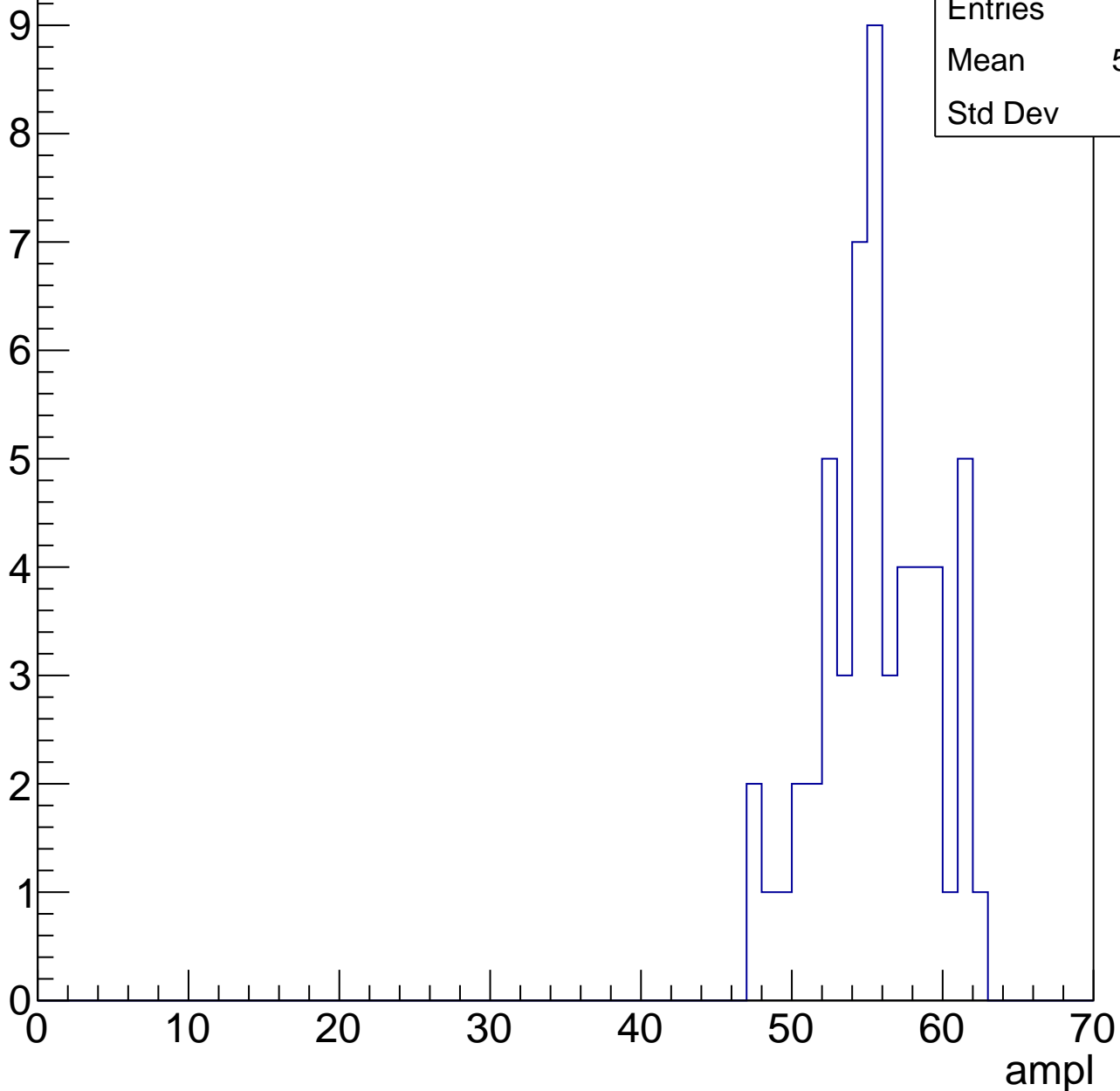


# B1L101S, U19-ch0, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	54
Mean	55.11
Std Dev	3.68

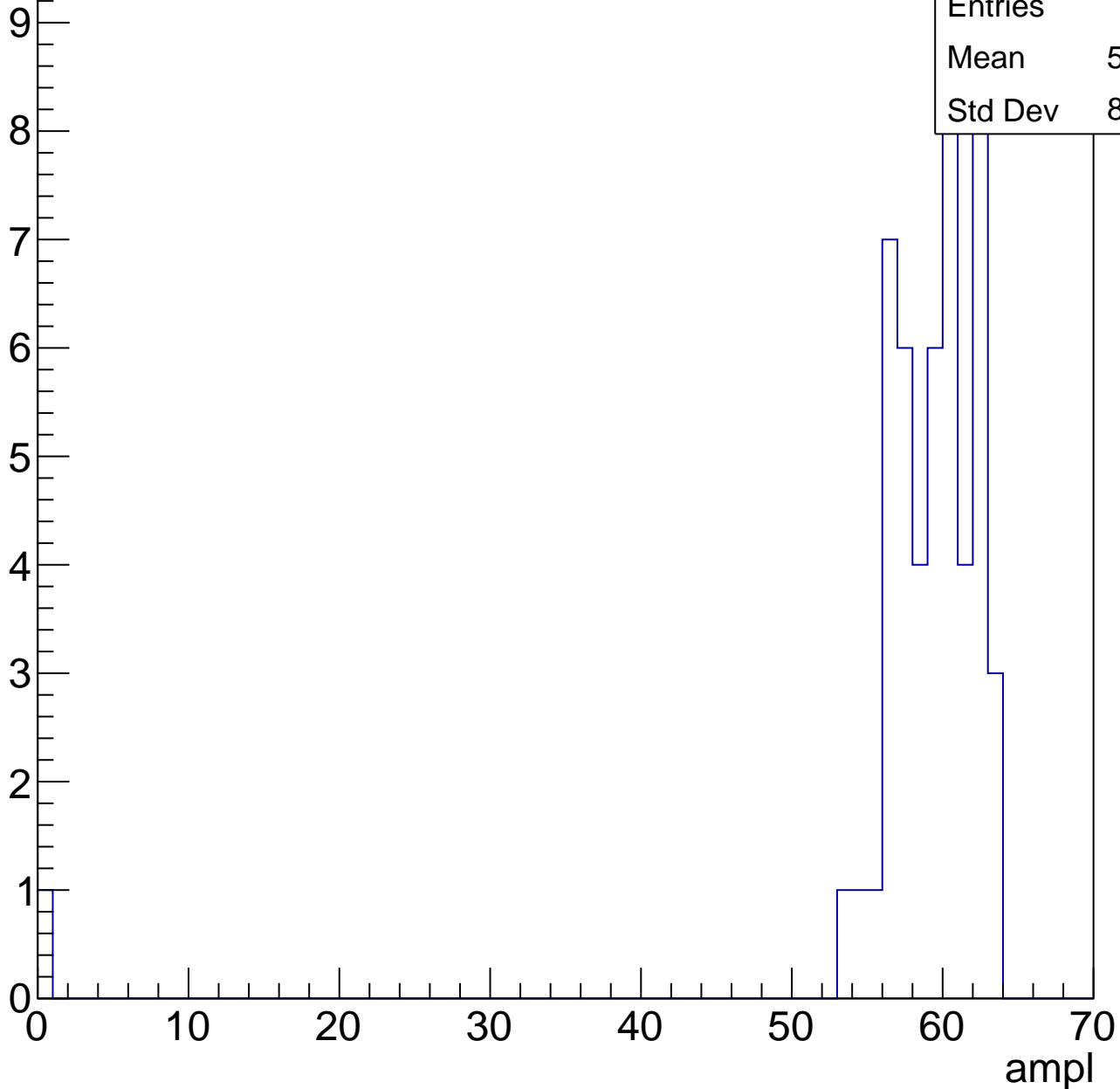


# B1L101S, U19-ch0, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	52
Mean	57.94
Std Dev	8.486

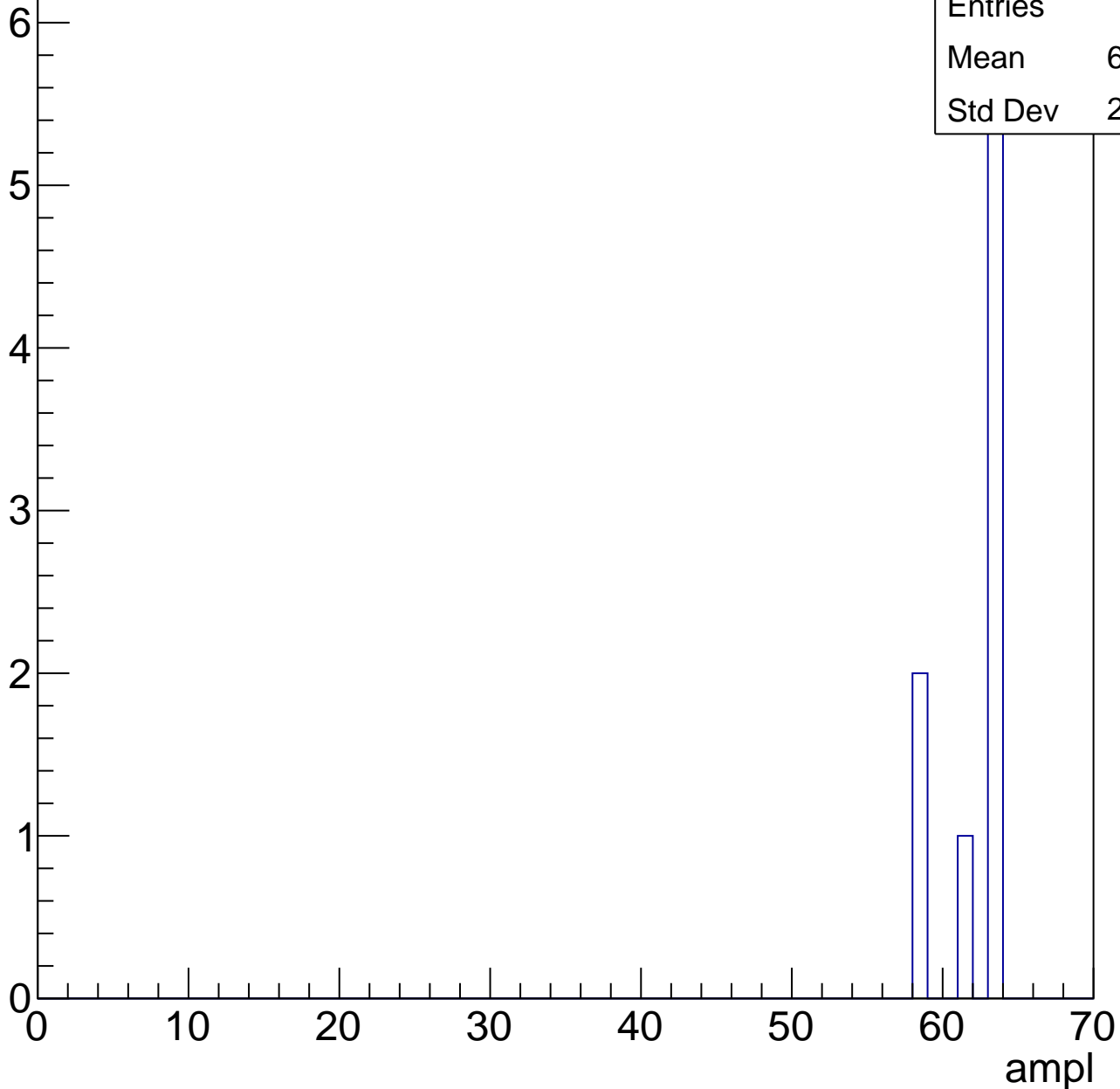


# B1L101S, U19-ch0, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	9
Mean	61.67
Std Dev	2.055

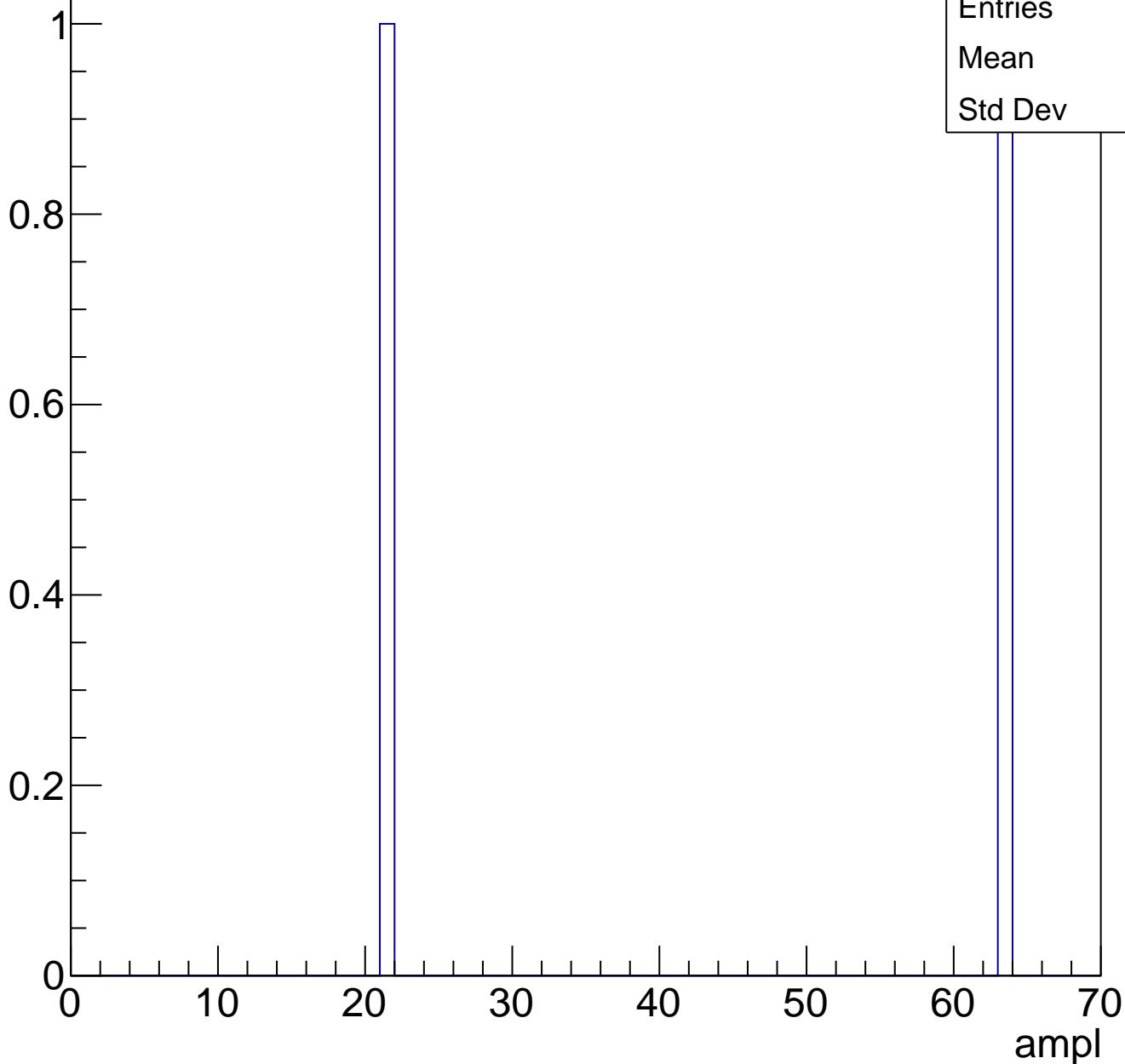




# B1L101S, U19-ch0, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U19-ch1, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	76
Mean	31.39
Std Dev	3.352

**Gaus mean : 32.2401**

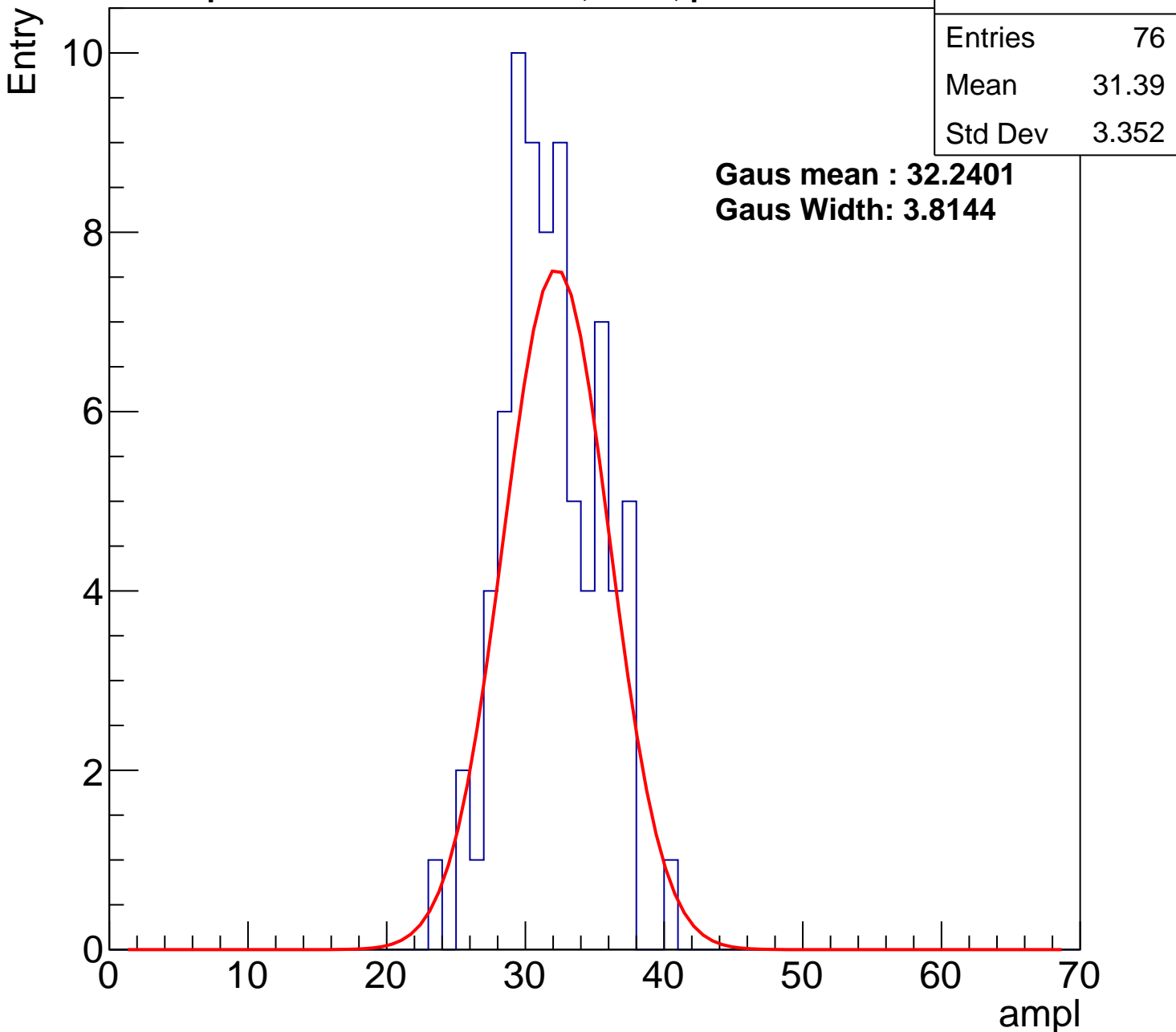
**Gaus Width: 3.8144**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



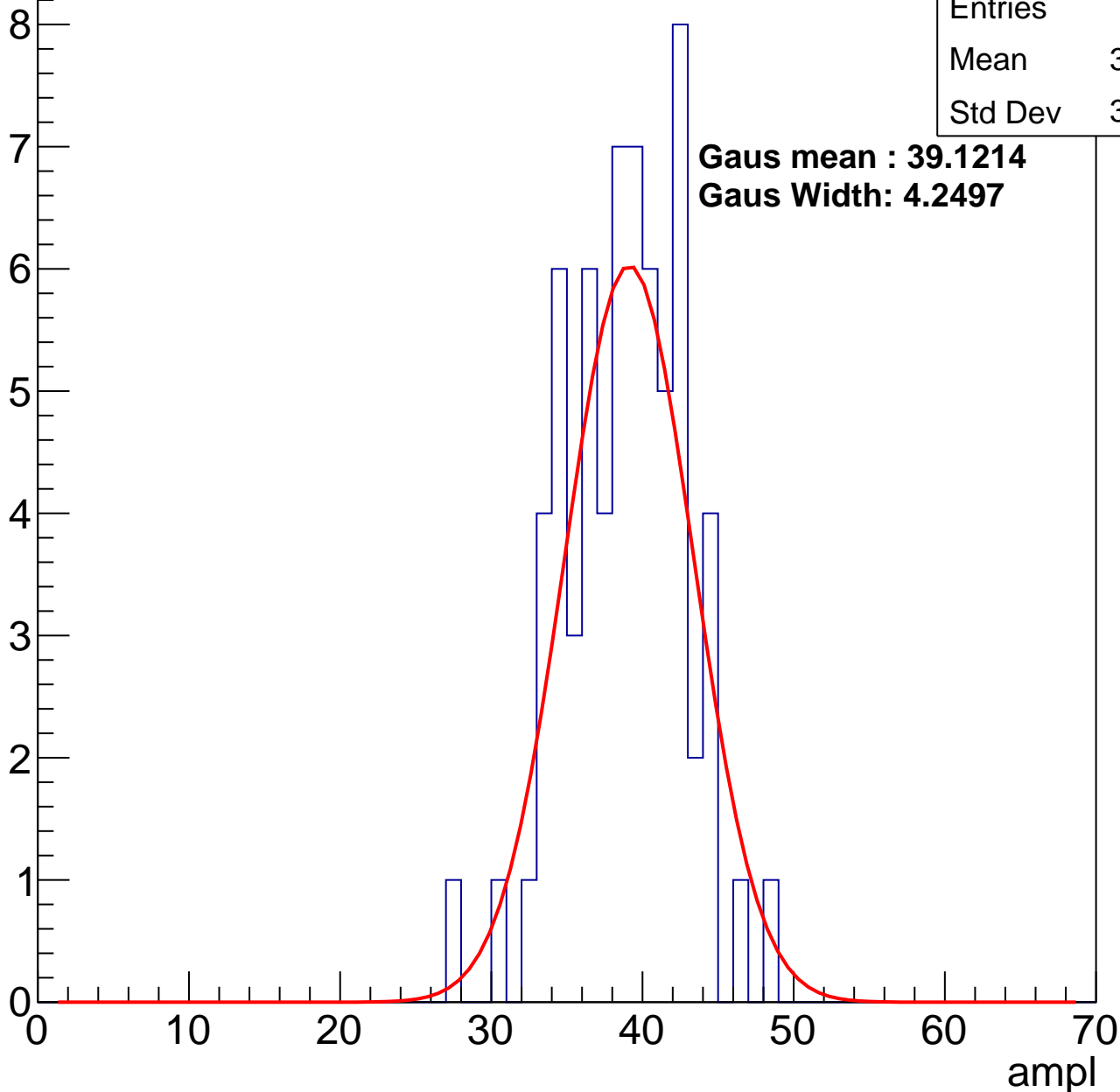
# B1L101S, U19-ch1, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	67
Mean	38.36
Std Dev	3.912

**Gaus mean : 39.1214**  
**Gaus Width: 4.2497**



# B1L101S, U19-ch1, adc2

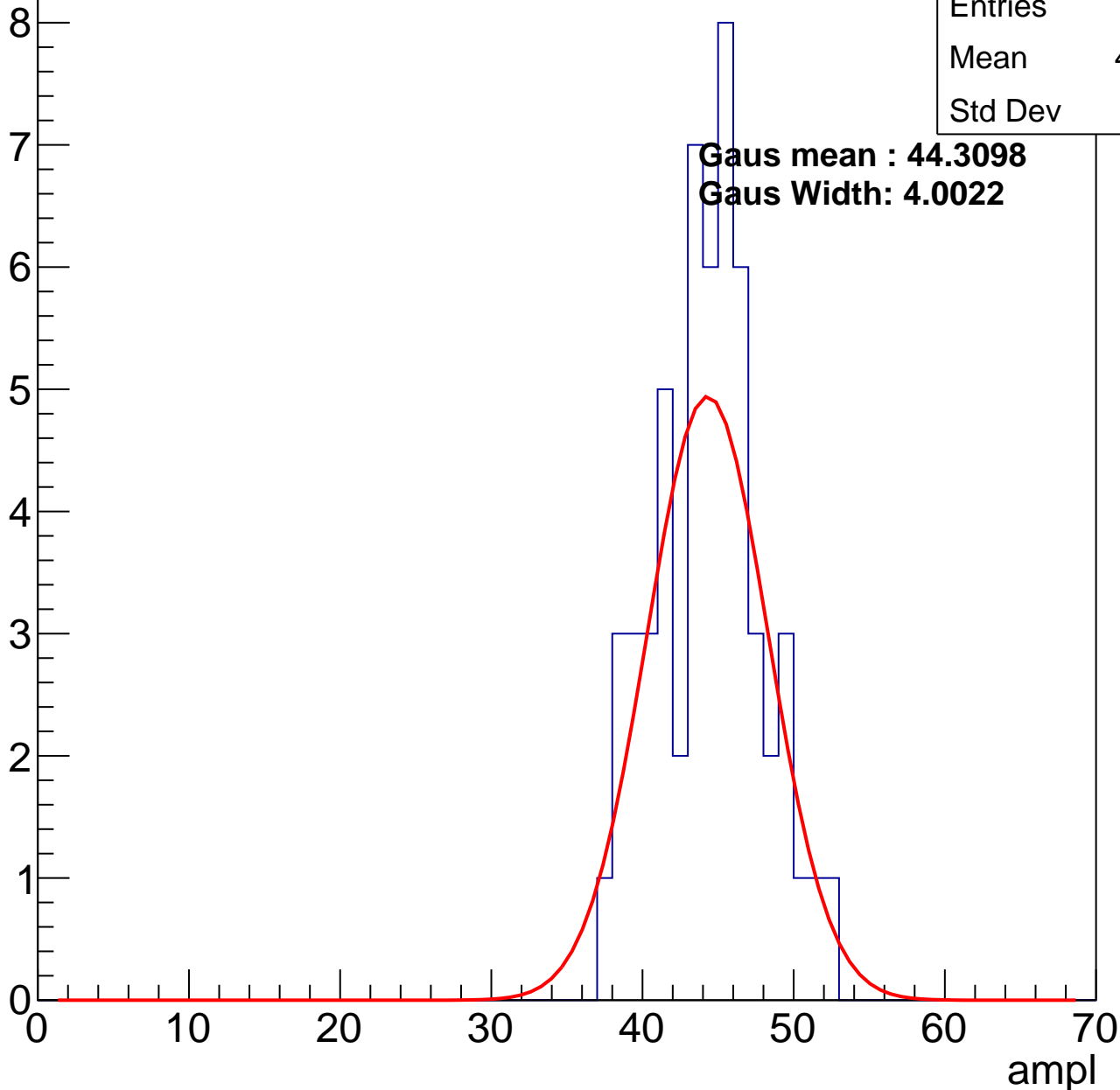
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	55
Mean	43.91
Std Dev	3.45

**Gaus mean : 44.3098**

**Gaus Width: 4.0022**

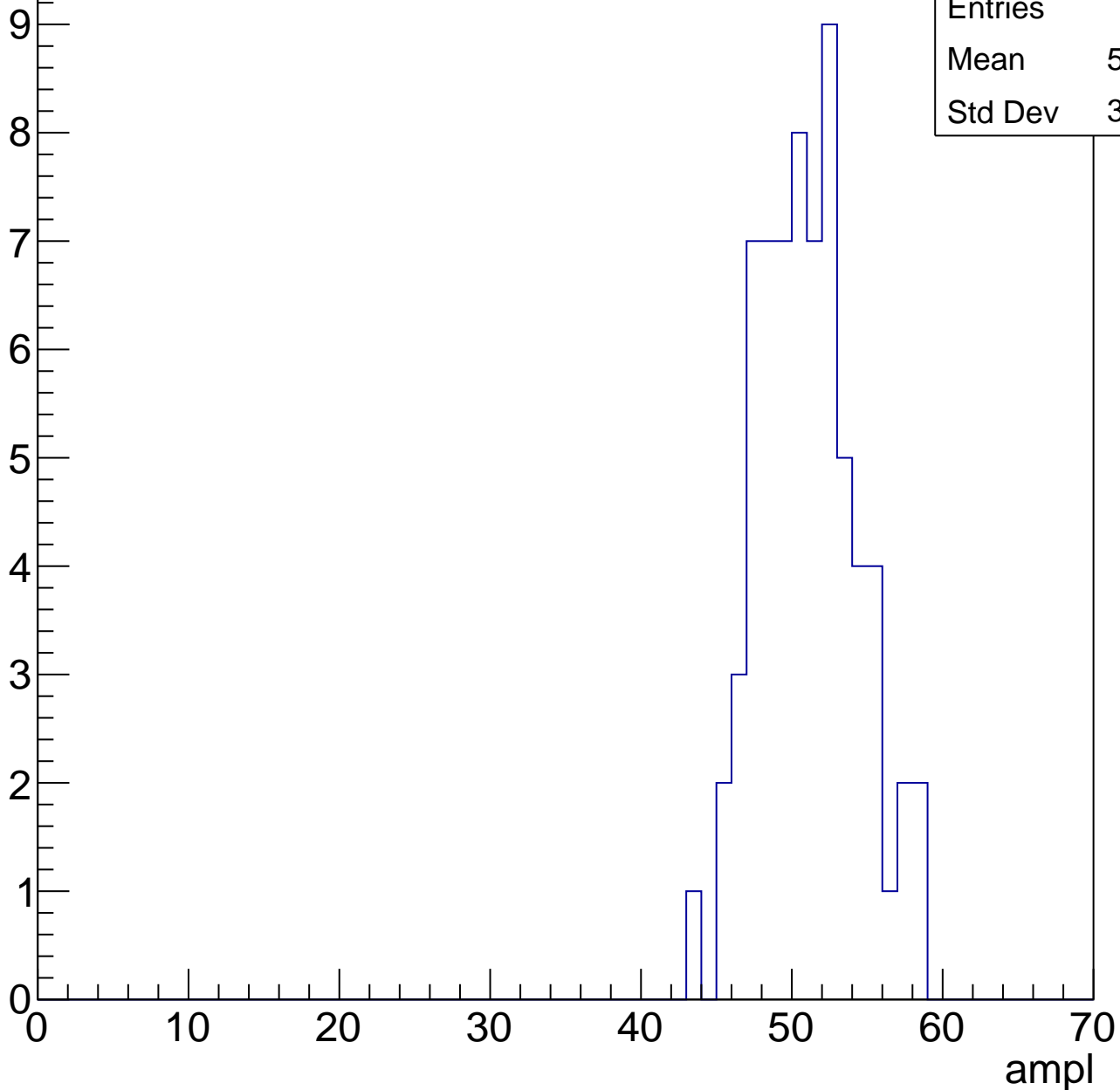


# B1L101S, U19-ch1, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	50.59
Std Dev	3.263

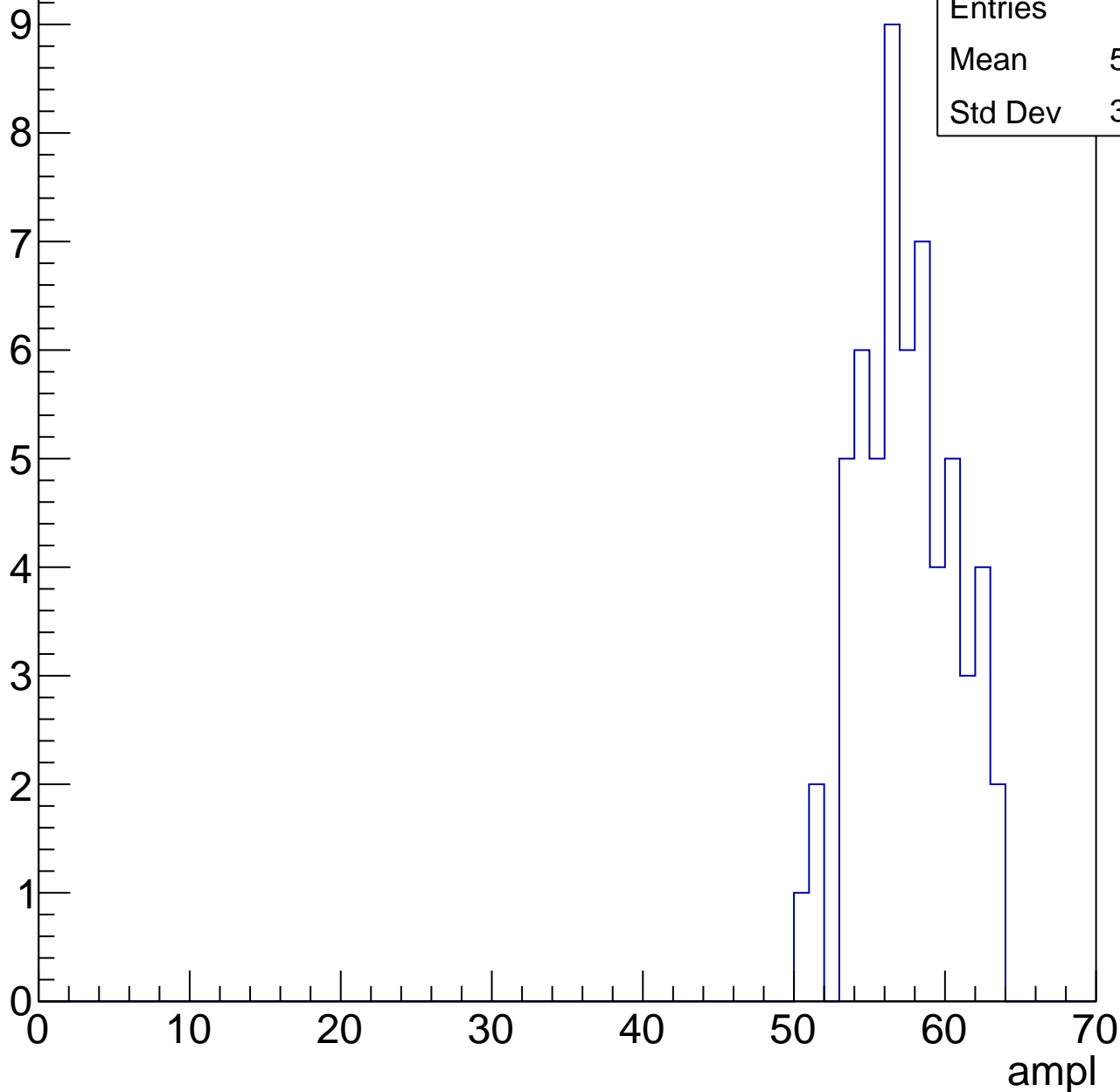


# B1L101S, U19-ch1, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

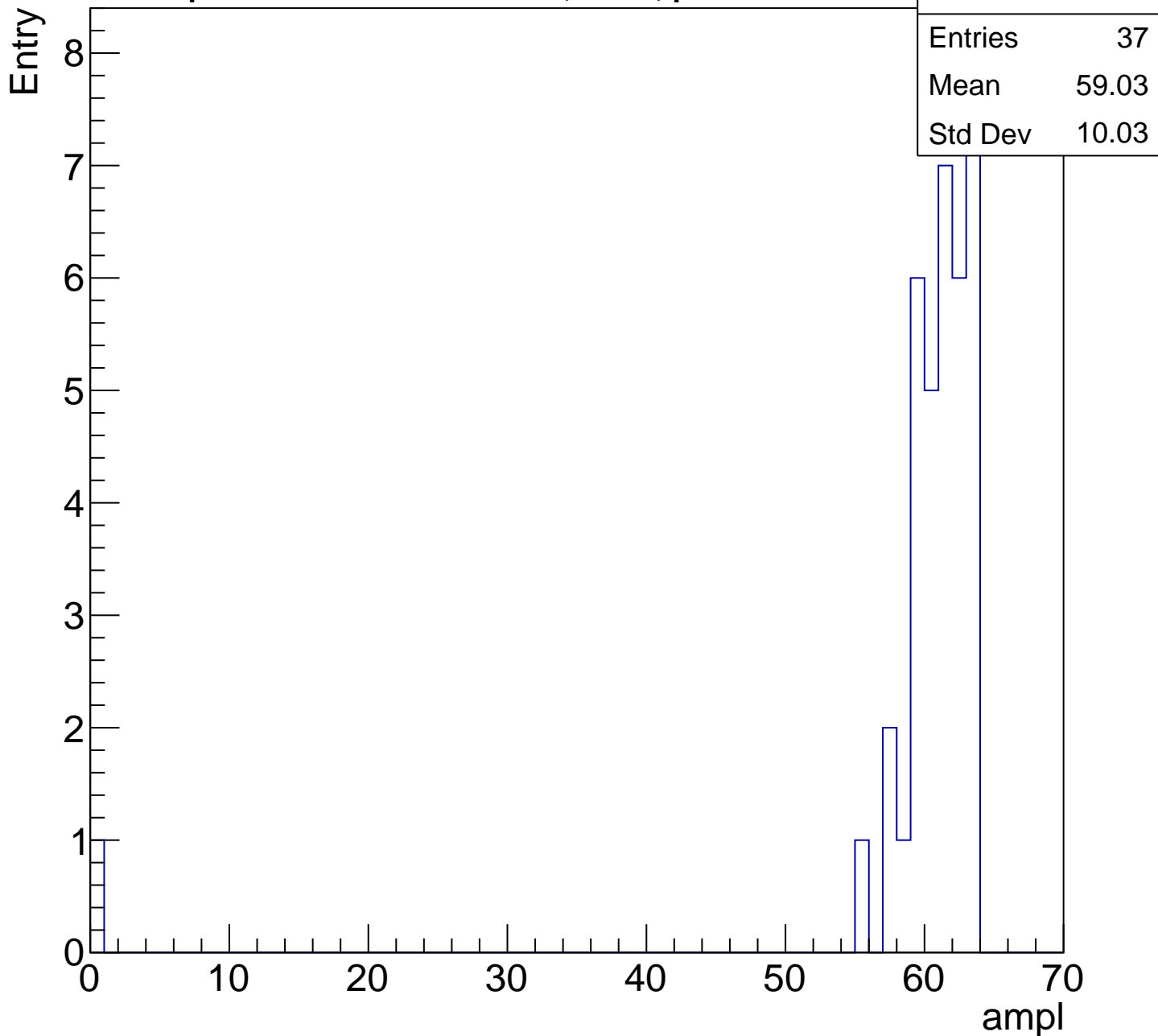
Entry

Entries	59
Mean	56.97
Std Dev	3.113



# B1L101S, U19-ch1, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U19-ch1, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0



# B1L101S, U19-ch1, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U19-ch2, adc0

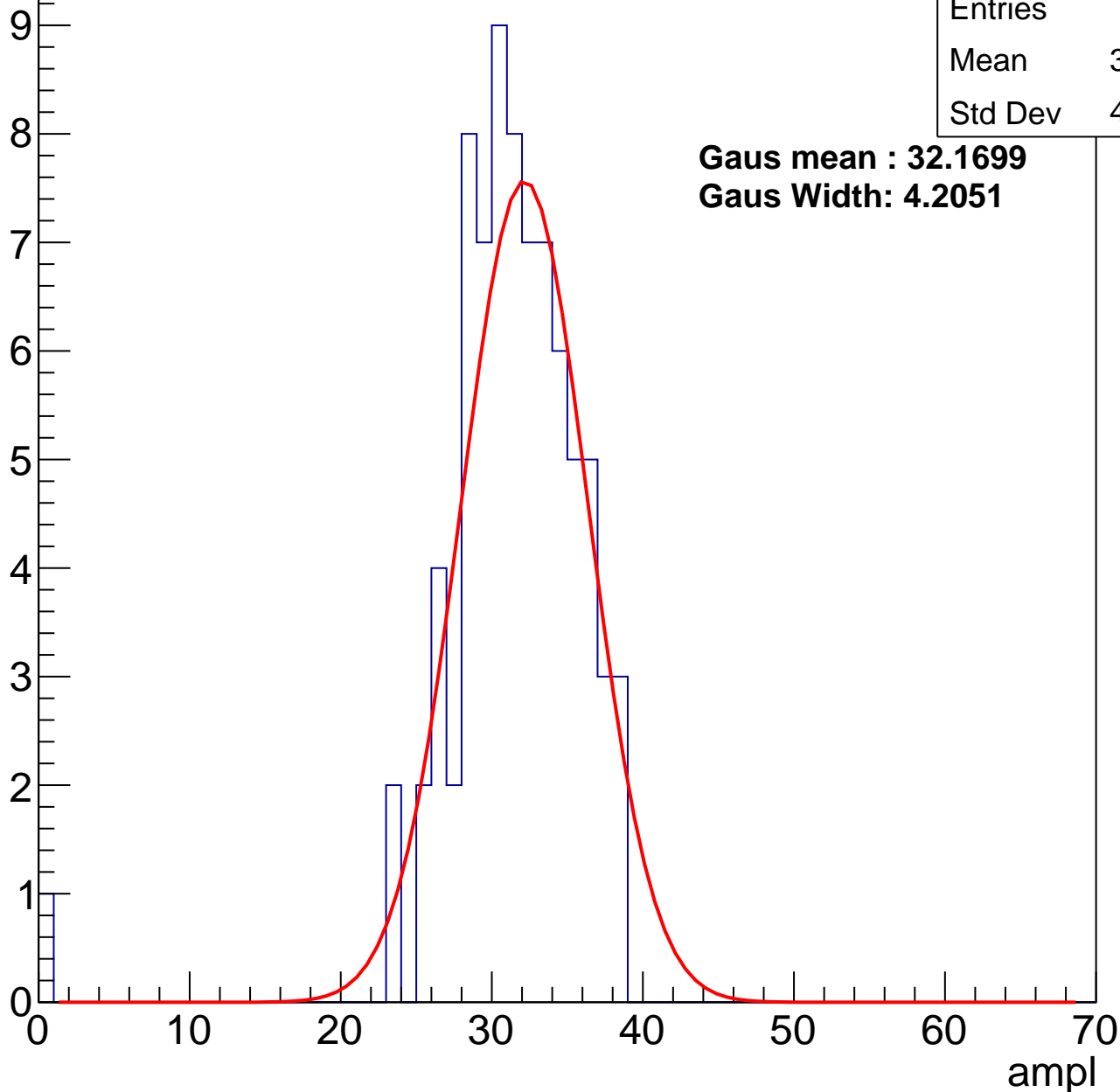
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	79
Mean	30.86
Std Dev	4.968

**Gaus mean : 32.1699**

**Gaus Width: 4.2051**



# B1L101S, U19-ch2, adc1

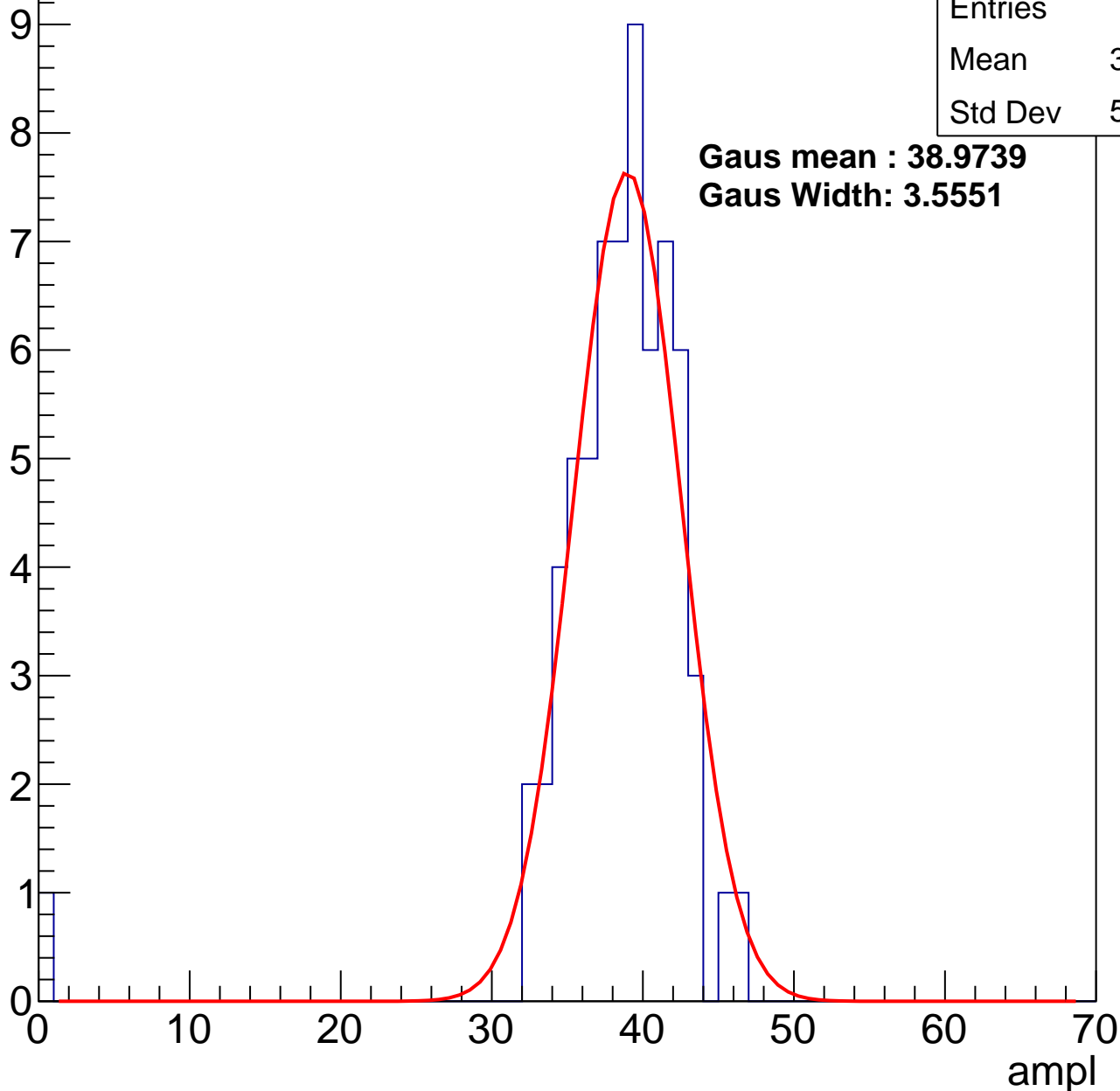
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	66
Mean	37.82
Std Dev	5.614

**Gaus mean : 38.9739**

**Gaus Width: 3.5551**



# B1L101S, U19-ch2, adc2

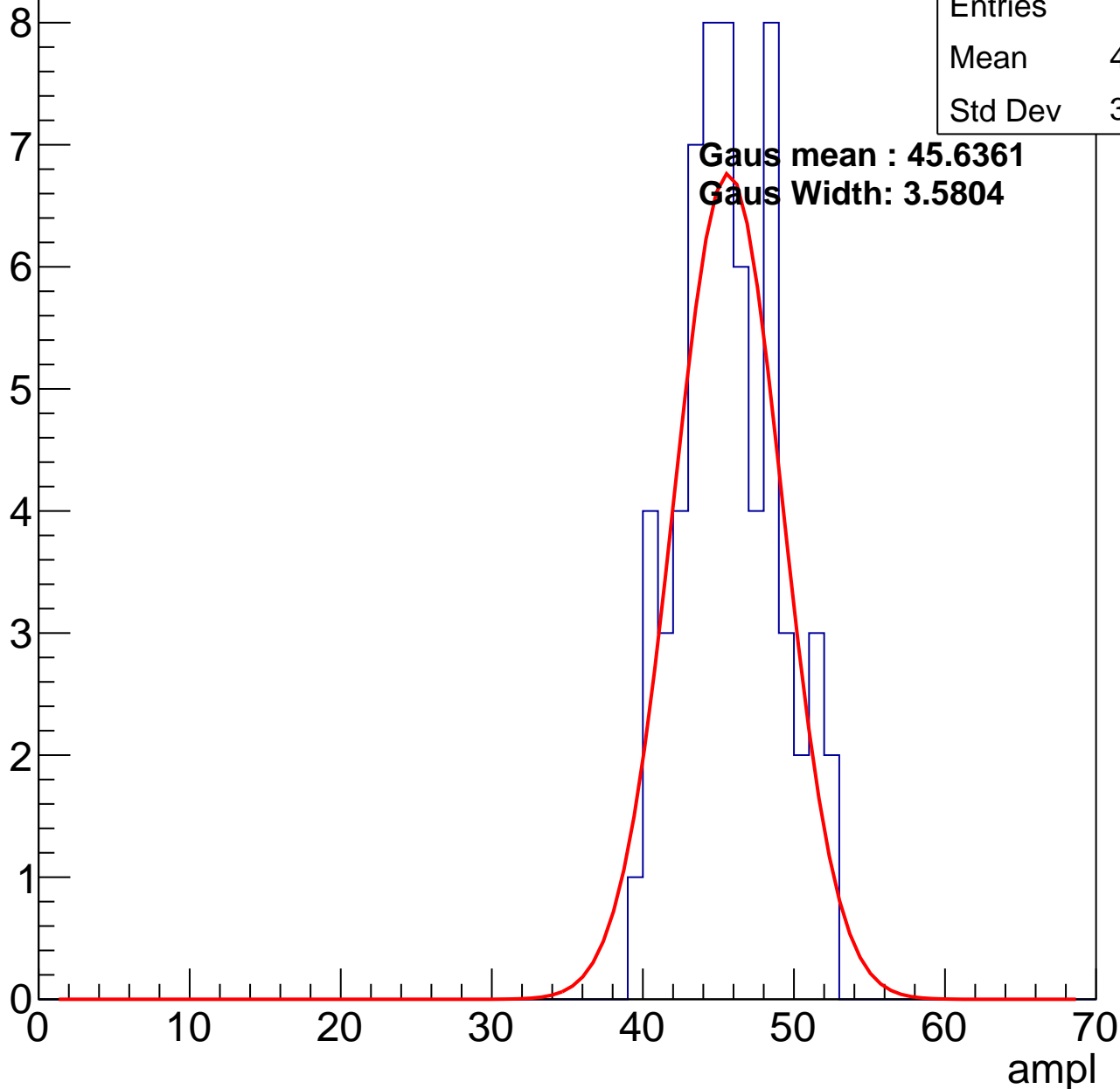
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	45.32
Std Dev	3.206

**Gaus mean : 45.6361**

**Gaus Width: 3.5804**

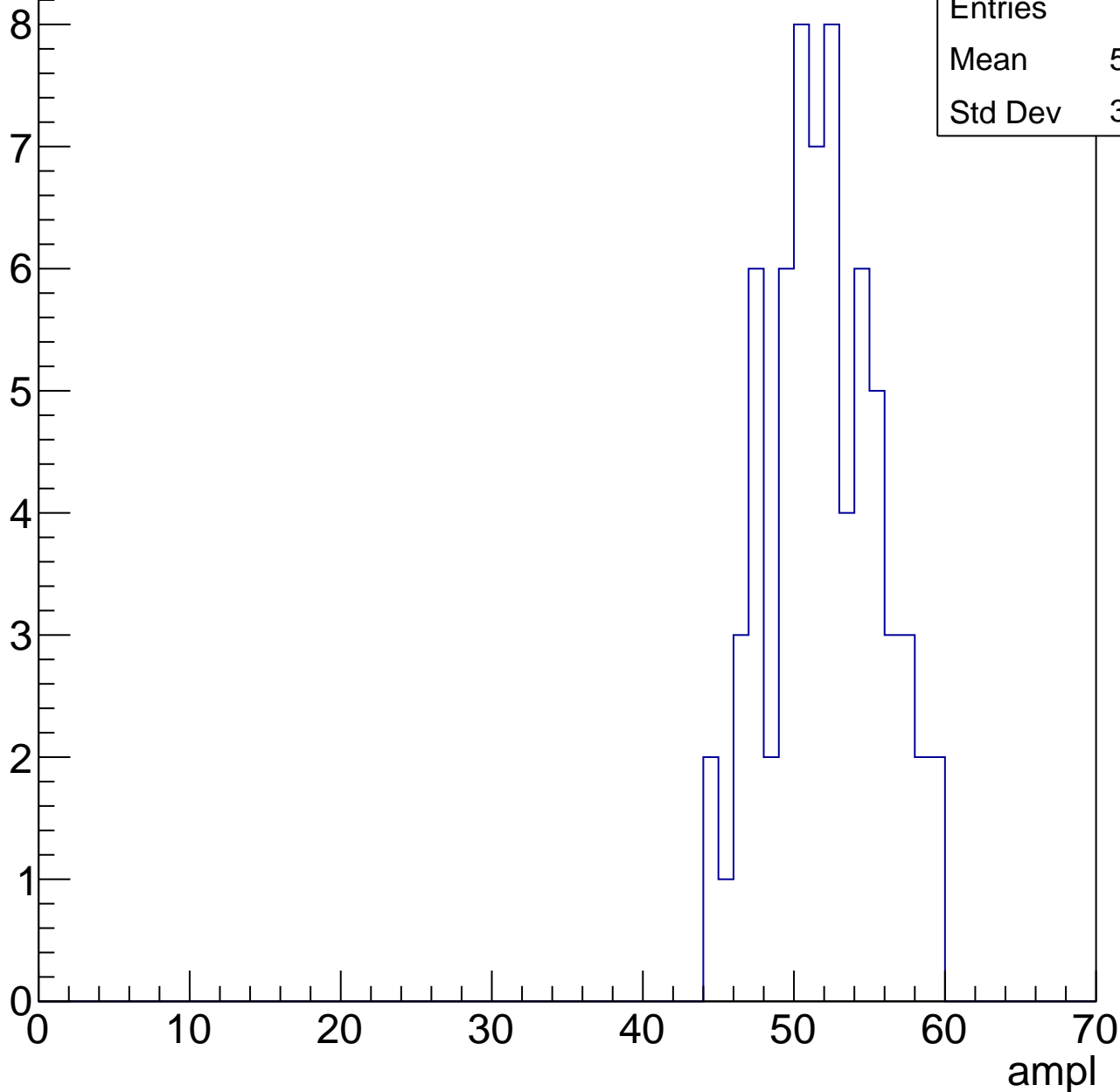


# B1L101S, U19-ch2, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	51.47
Std Dev	3.652

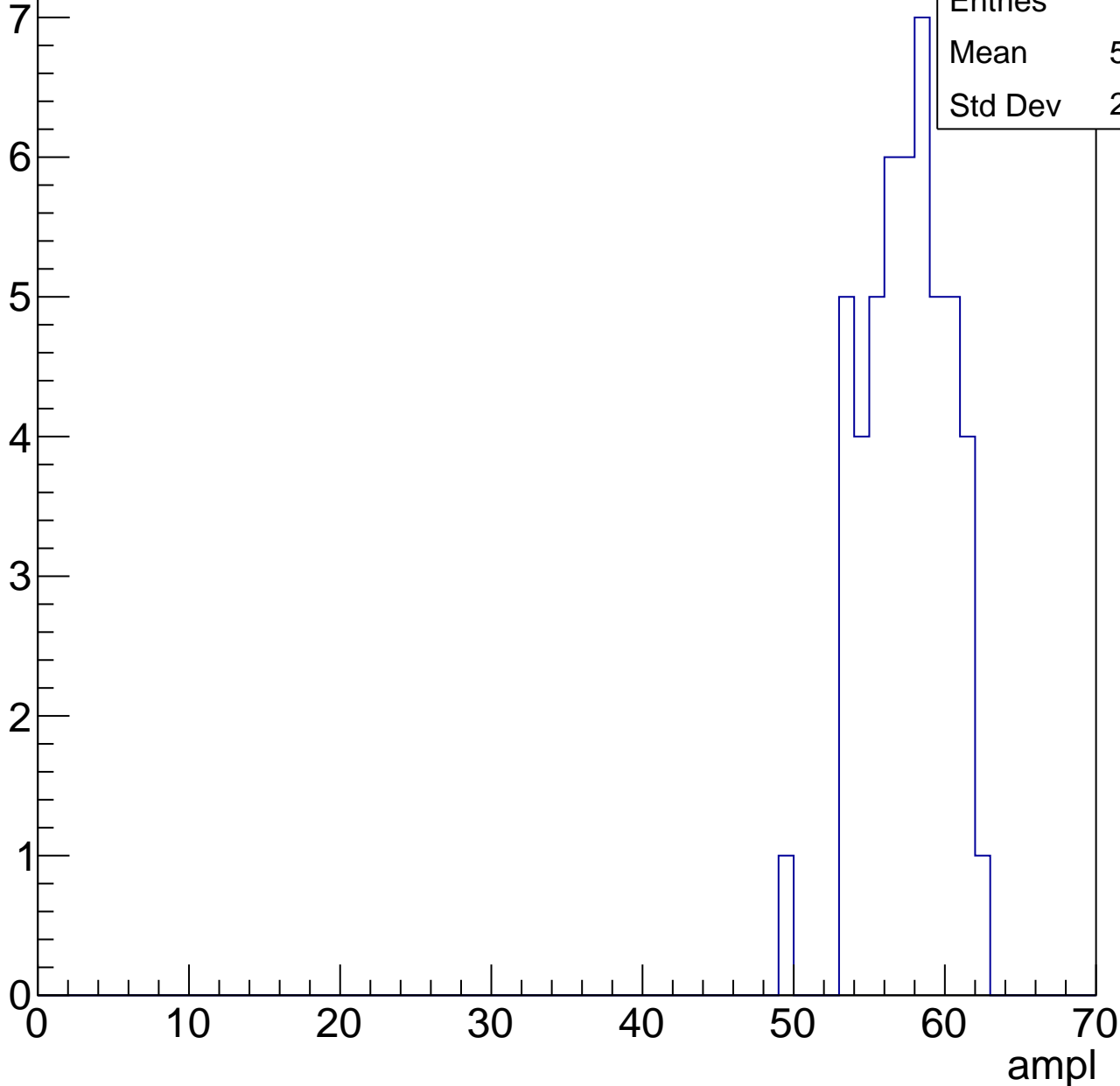


# B1L101S, U19-ch2, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	49
Mean	56.94
Std Dev	2.736

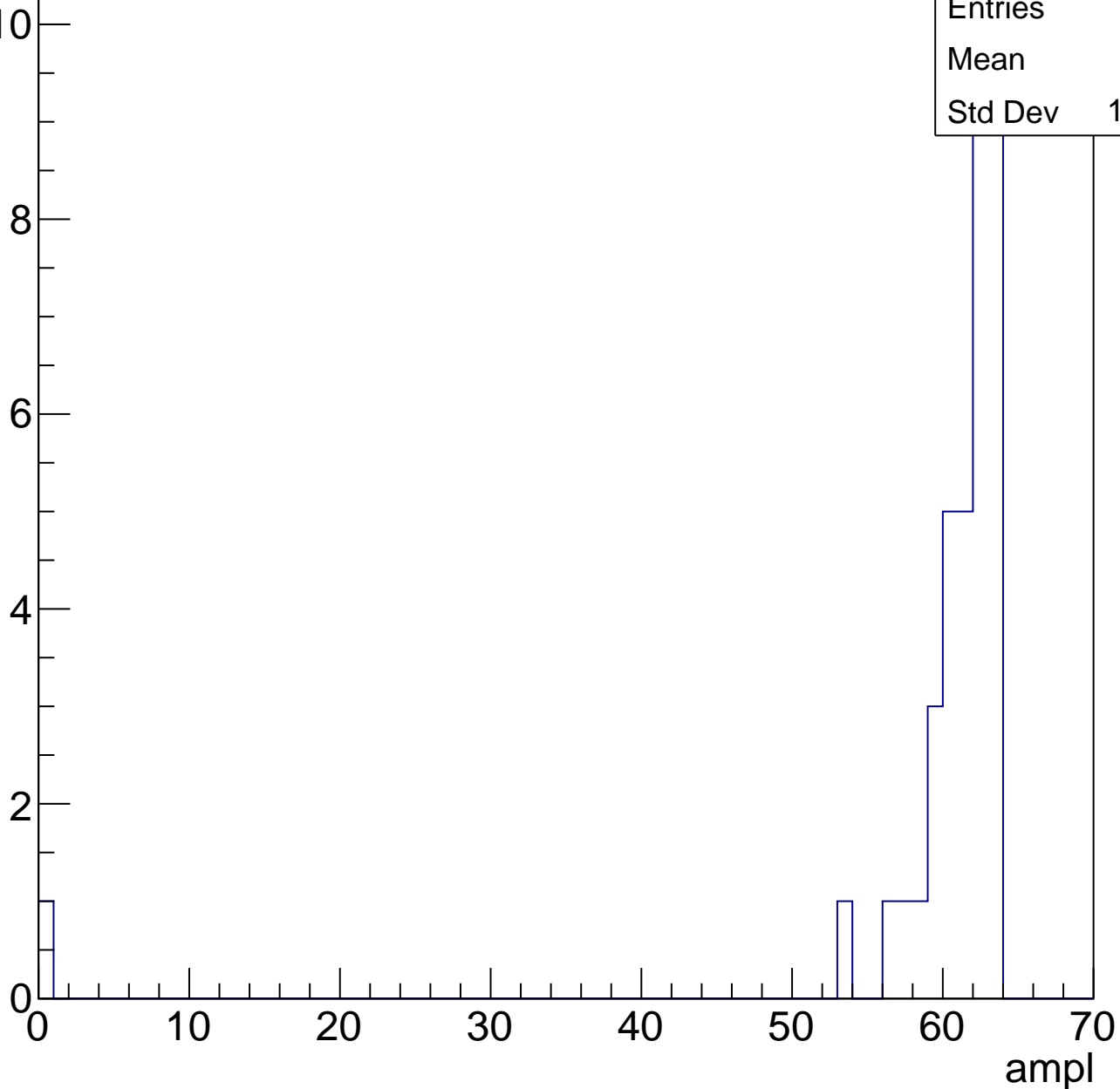


# B1L101S, U19-ch2, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	37
Mean	59.3
Std Dev	10.13



# B1L101S, U19-ch2, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U19-ch2, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U19-ch3, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	82
Mean	31.21
Std Dev	3.595

**Gaus mean : 32.0833**

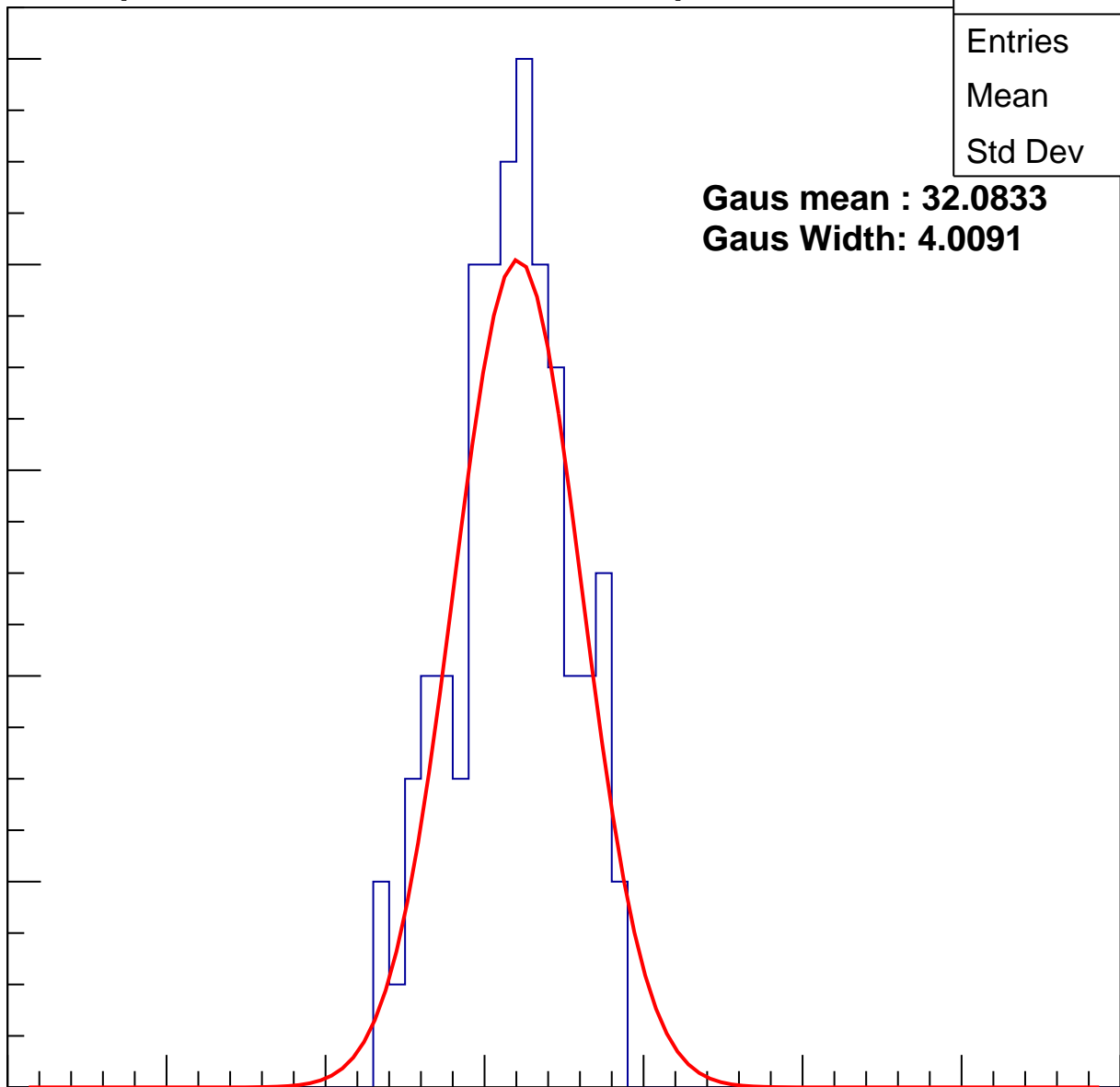
**Gaus Width: 4.0091**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U19-ch3, adc1

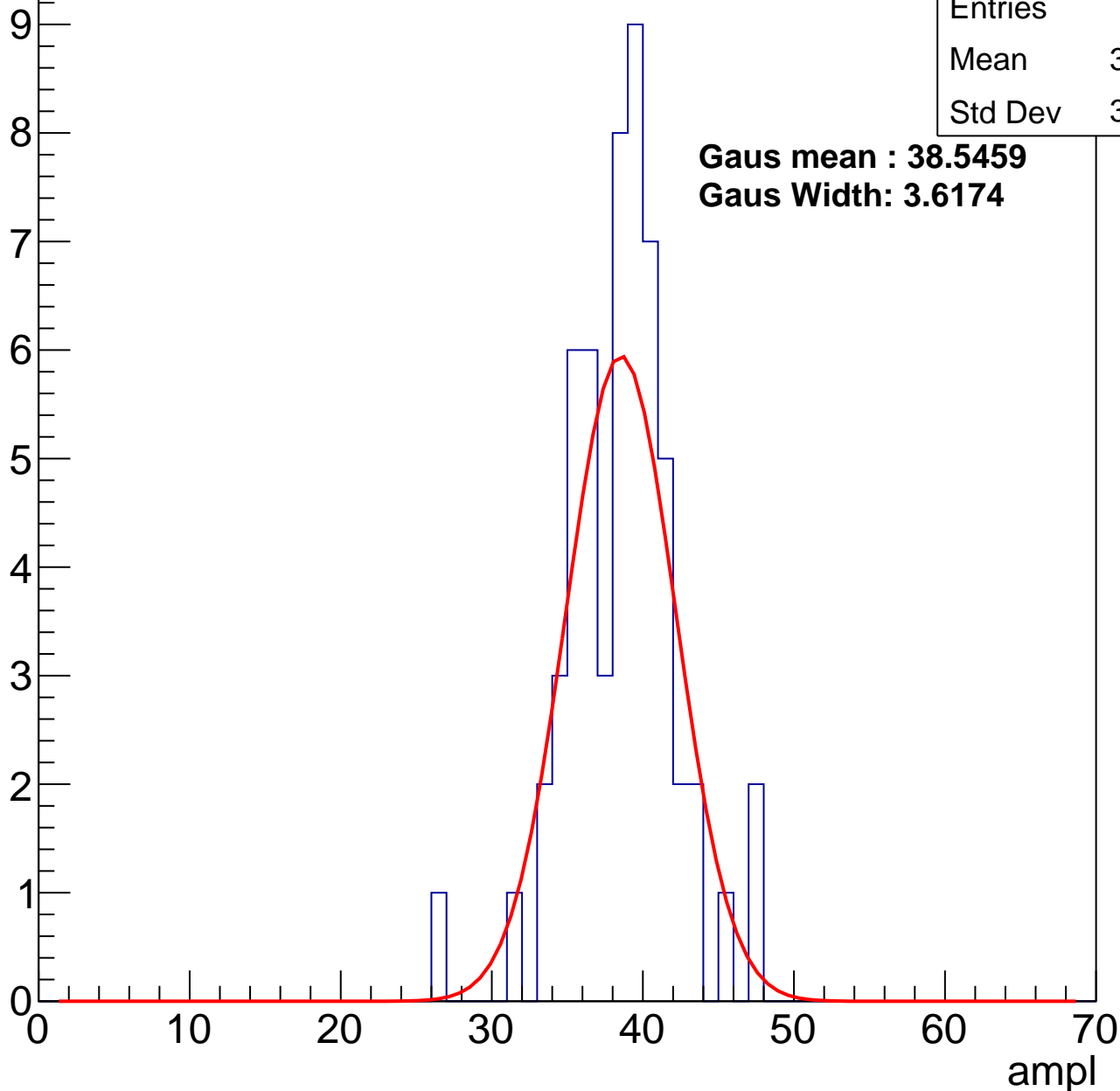
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	58
Mean	38.12
Std Dev	3.587

**Gaus mean : 38.5459**

**Gaus Width: 3.6174**



# B1L101S, U19-ch3, adc2

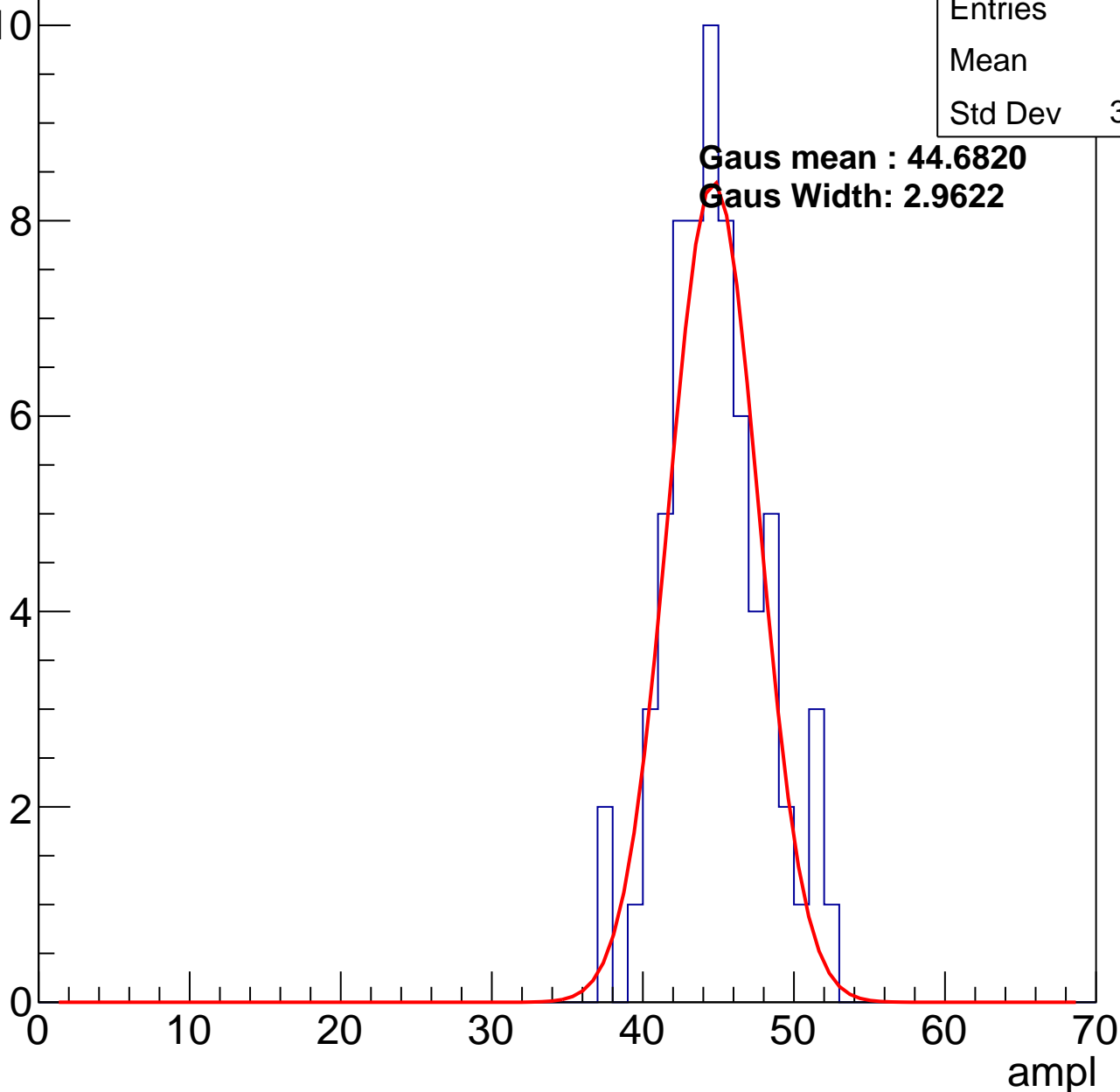
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	67
Mean	44.4
Std Dev	3.209

**Gaus mean : 44.6820**

**Gaus Width: 2.9622**

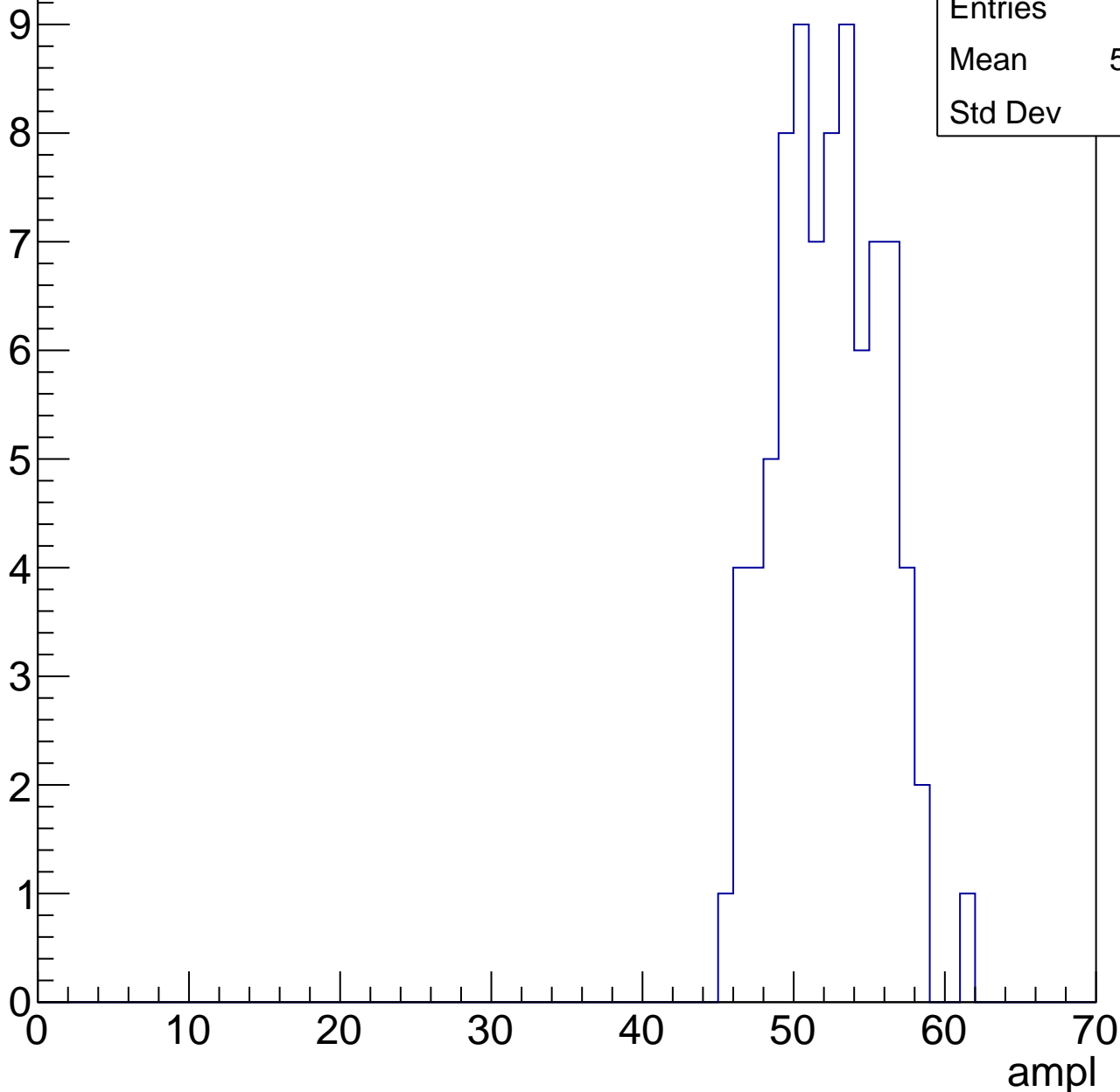


# B1L101S, U19-ch3, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

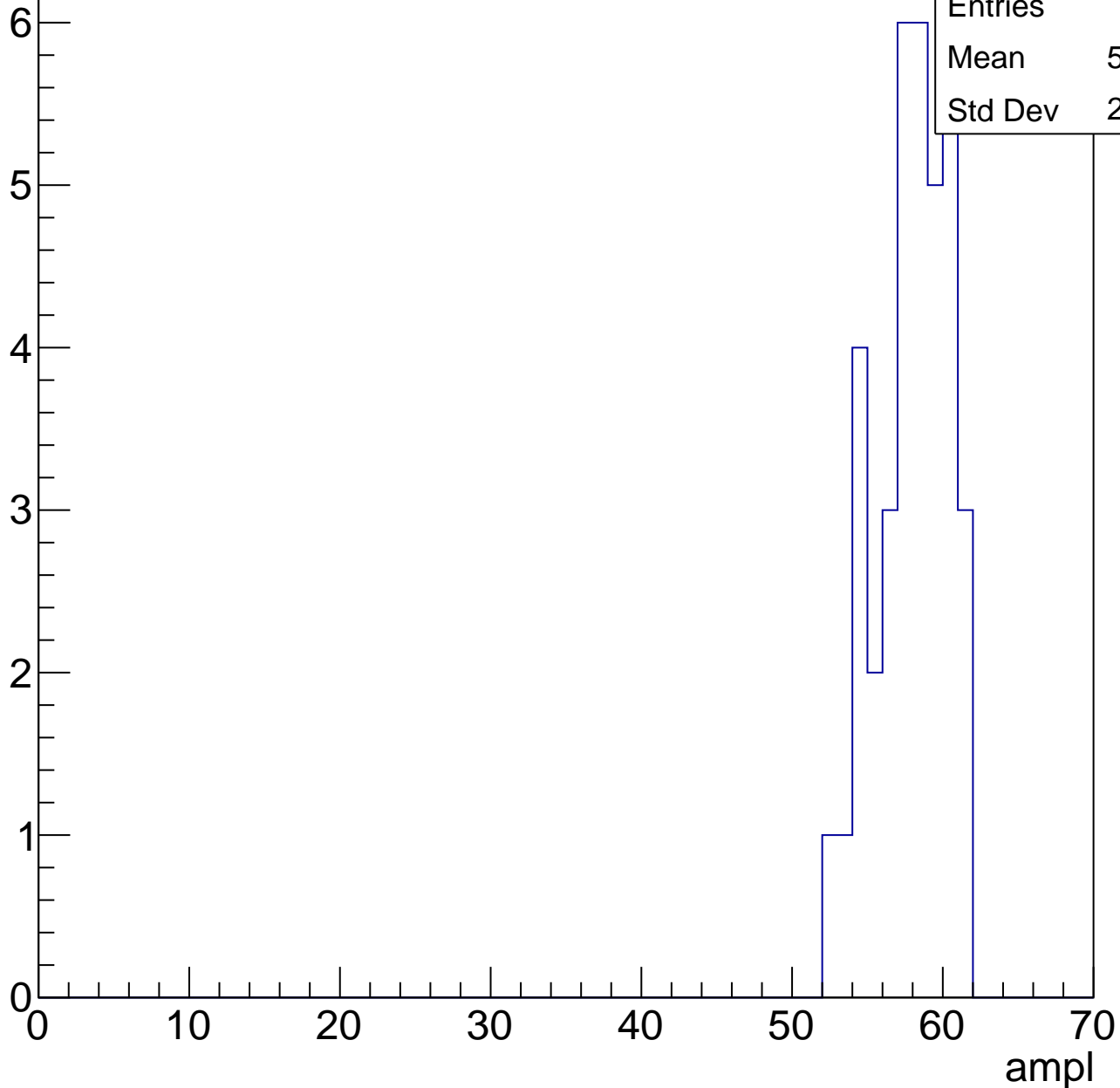
Entries	82
Mean	51.89
Std Dev	3.4



# B1L101S, U19-ch3, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

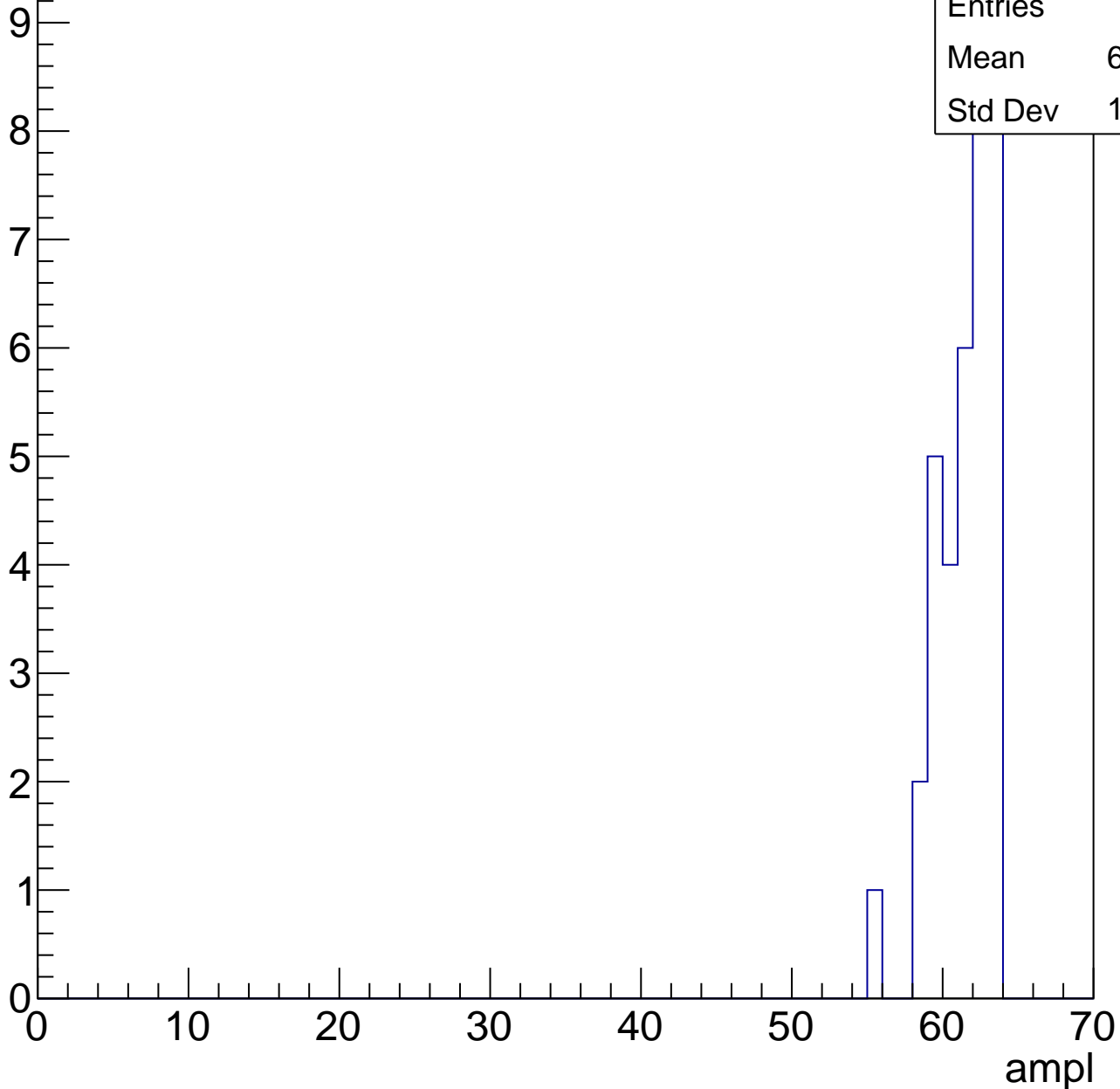


# B1L101S, U19-ch3, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

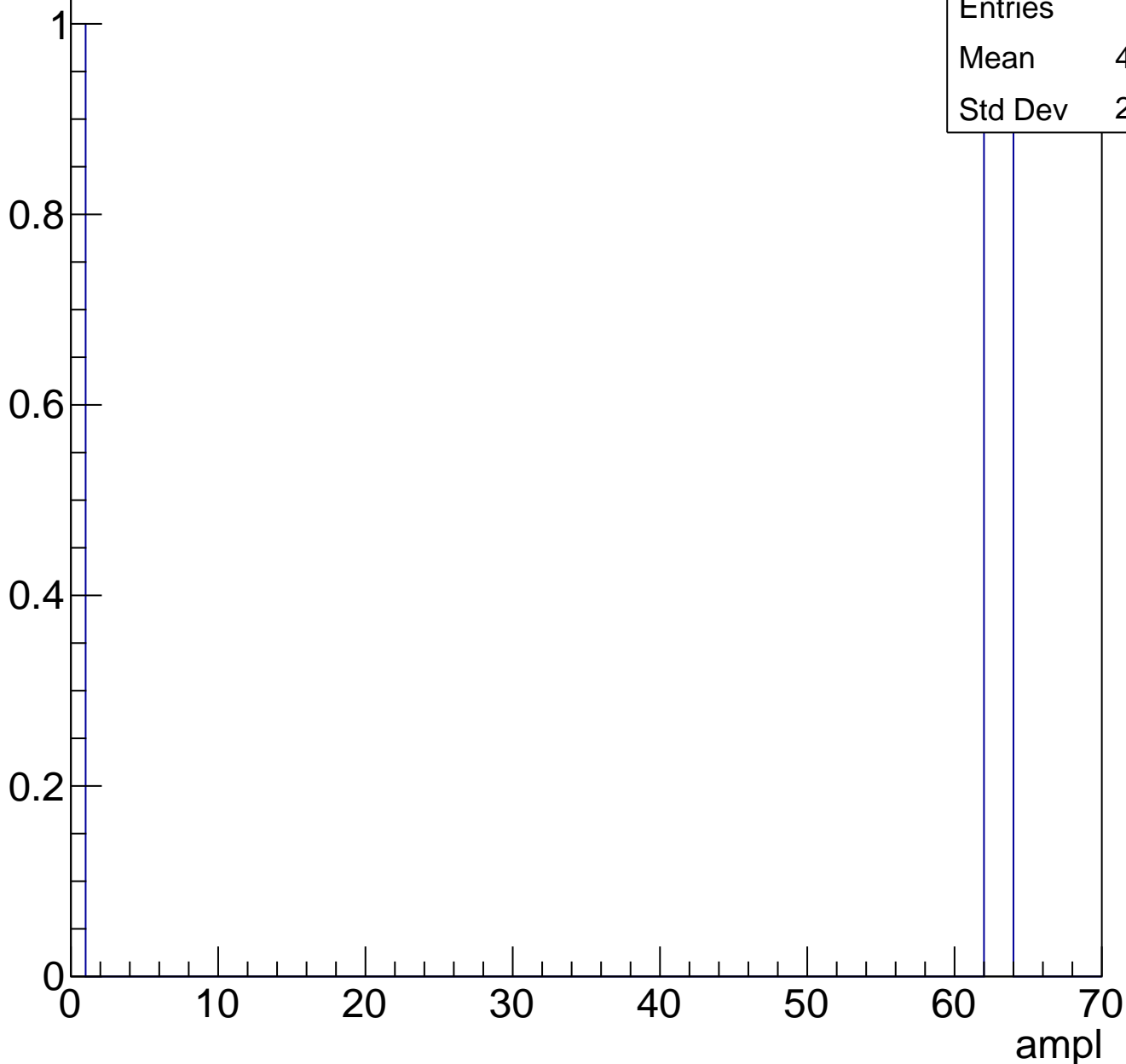
Entries	36
Mean	61.03
Std Dev	1.848



# B1L101S, U19-ch3, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U19-ch3, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U19-ch4, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	67
Mean	30.09
Std Dev	4.753

**Gaus mean : 30.8453**

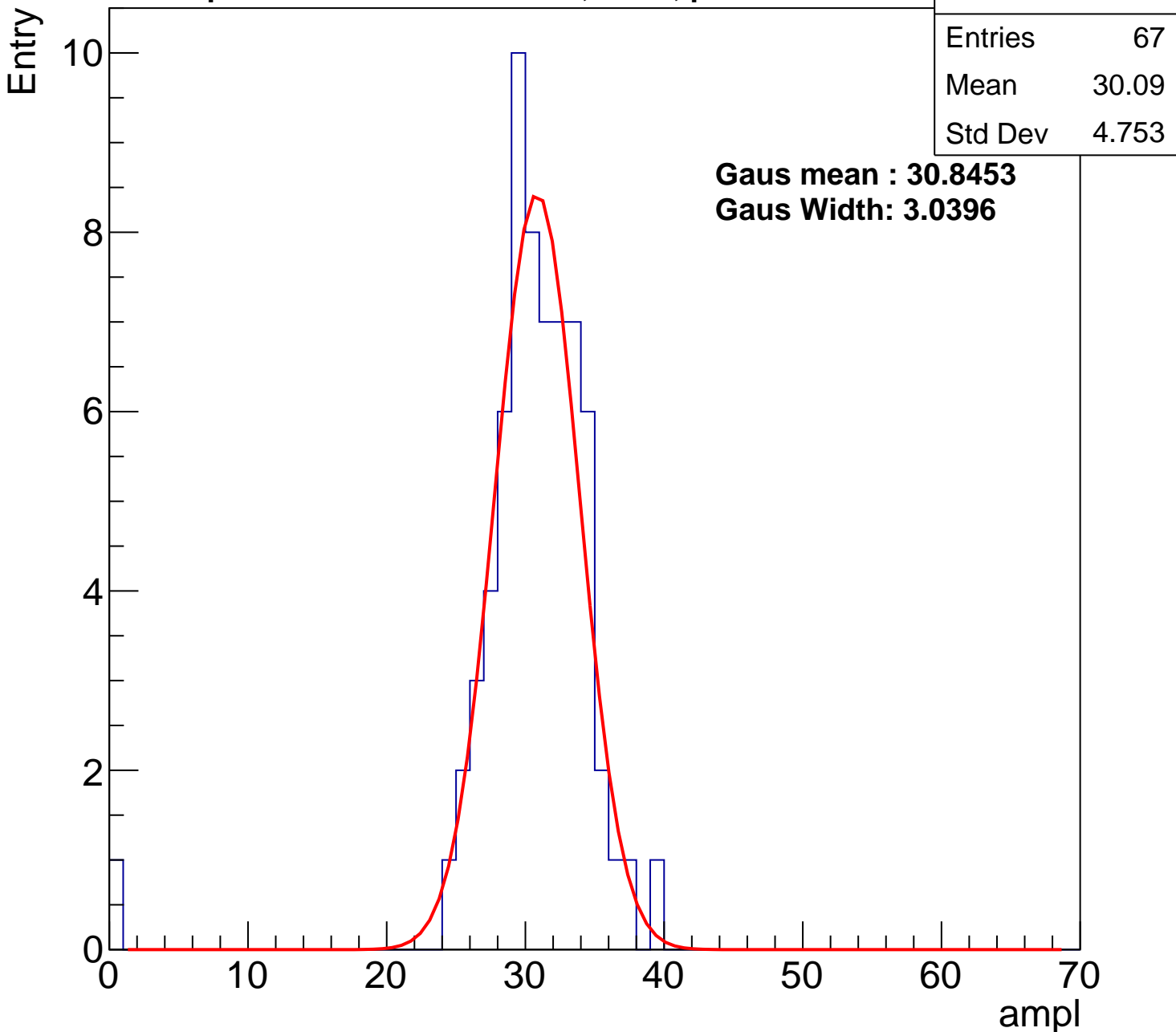
**Gaus Width: 3.0396**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U19-ch4, adc1

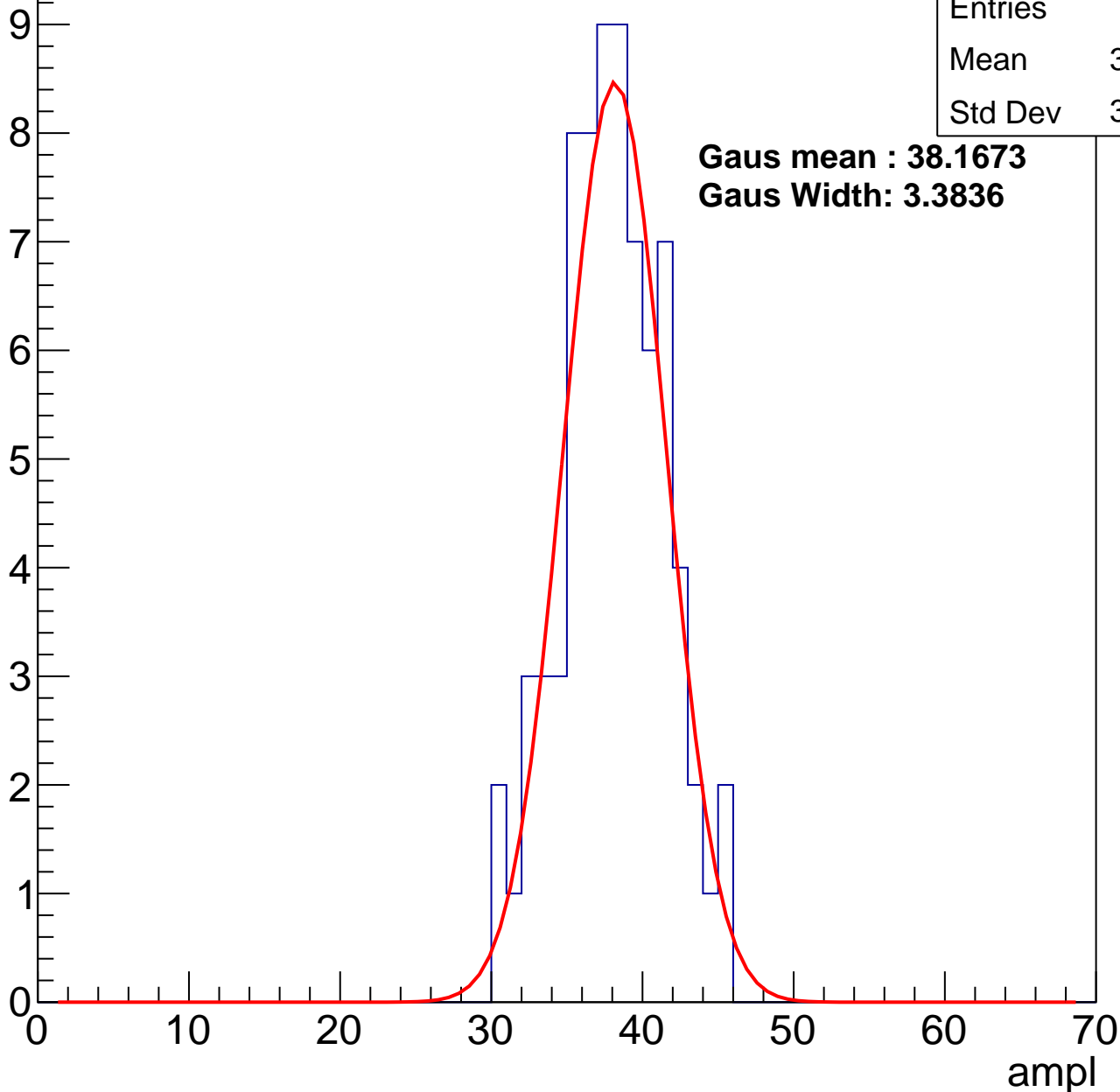
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	75
Mean	37.59
Std Dev	3.367

**Gaus mean : 38.1673**

**Gaus Width: 3.3836**



# B1L101S, U19-ch4, adc2

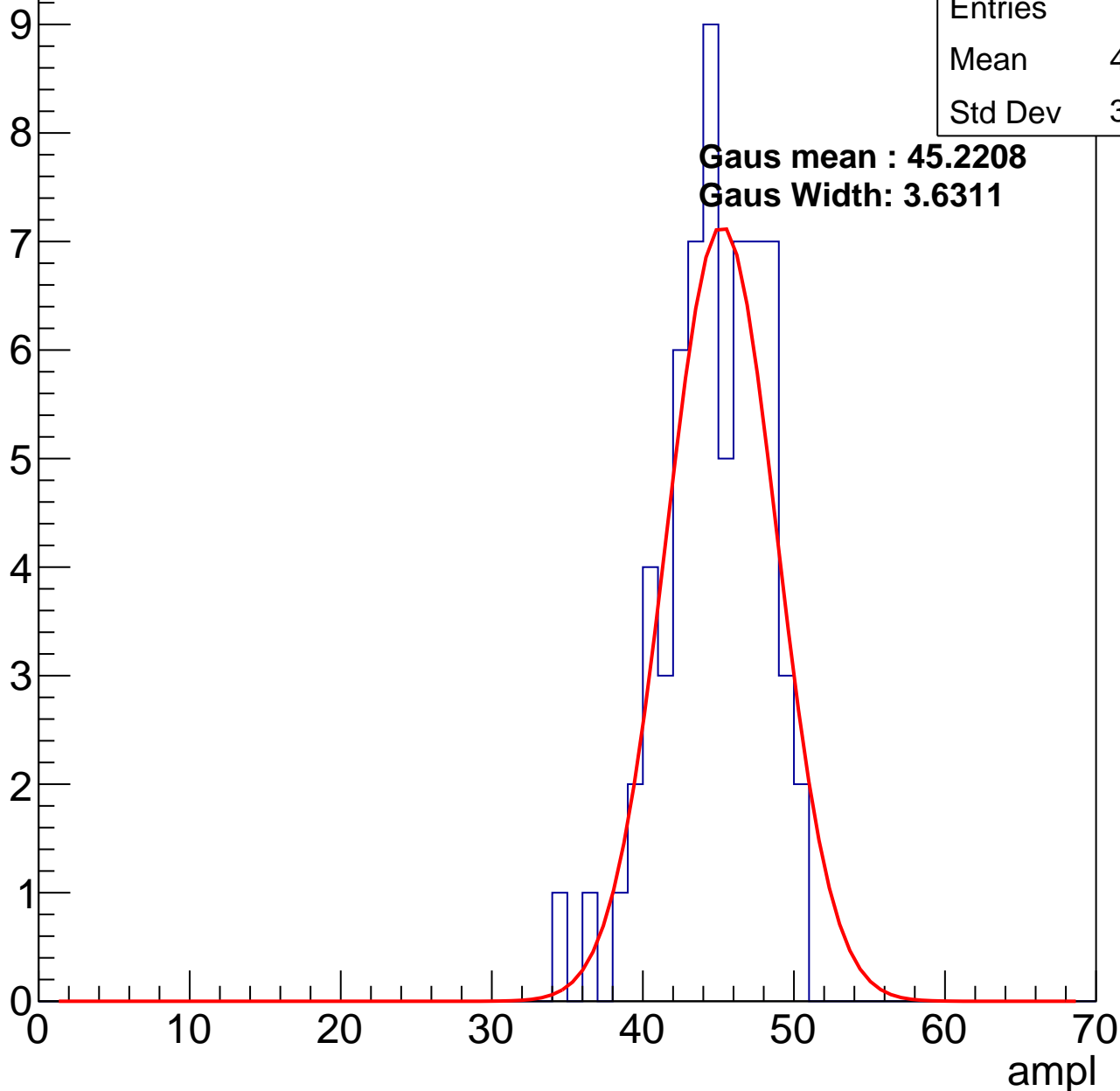
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	44.26
Std Dev	3.334

**Gaus mean : 45.2208**

**Gaus Width: 3.6311**

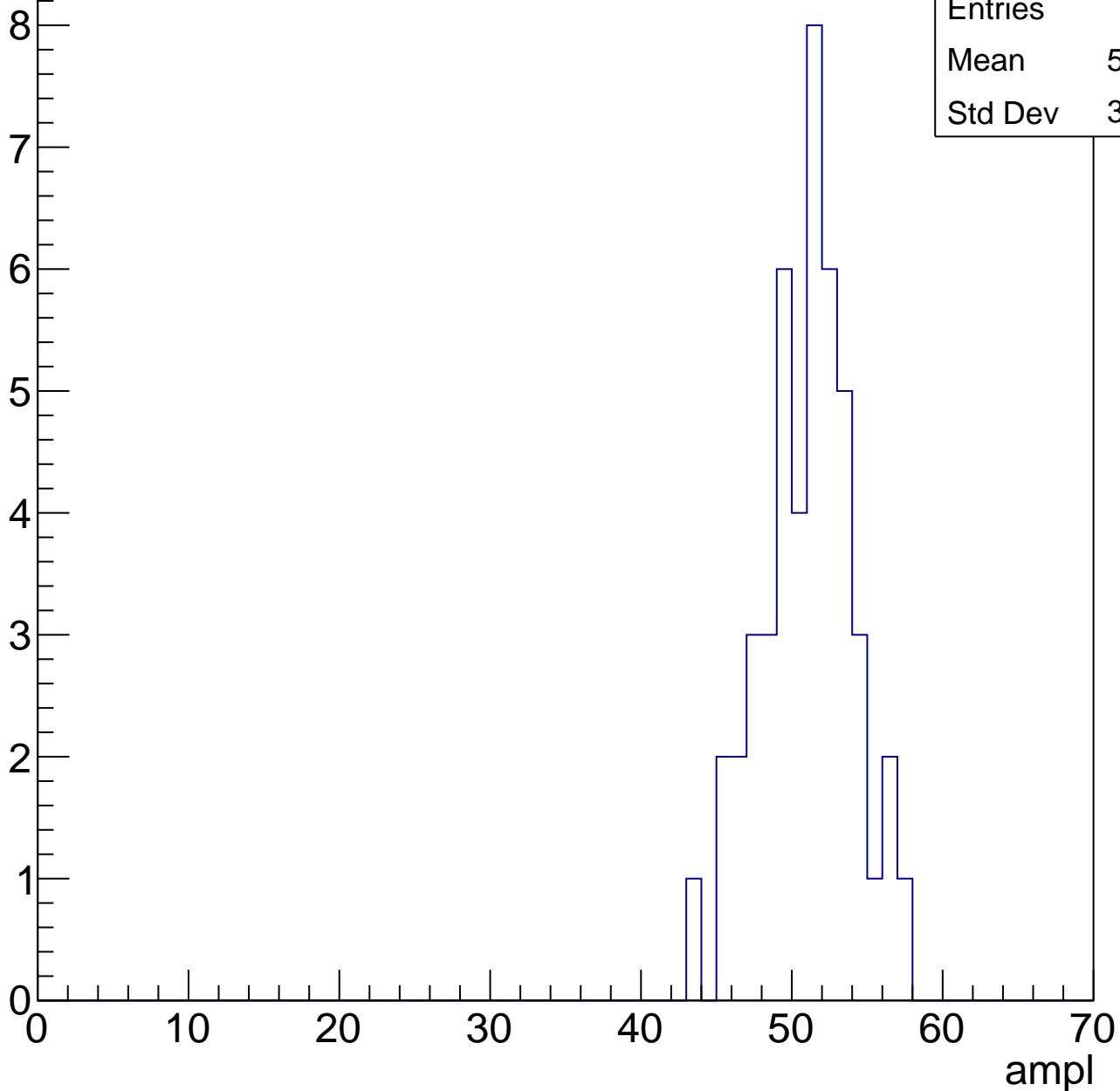


# B1L101S, U19-ch4, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

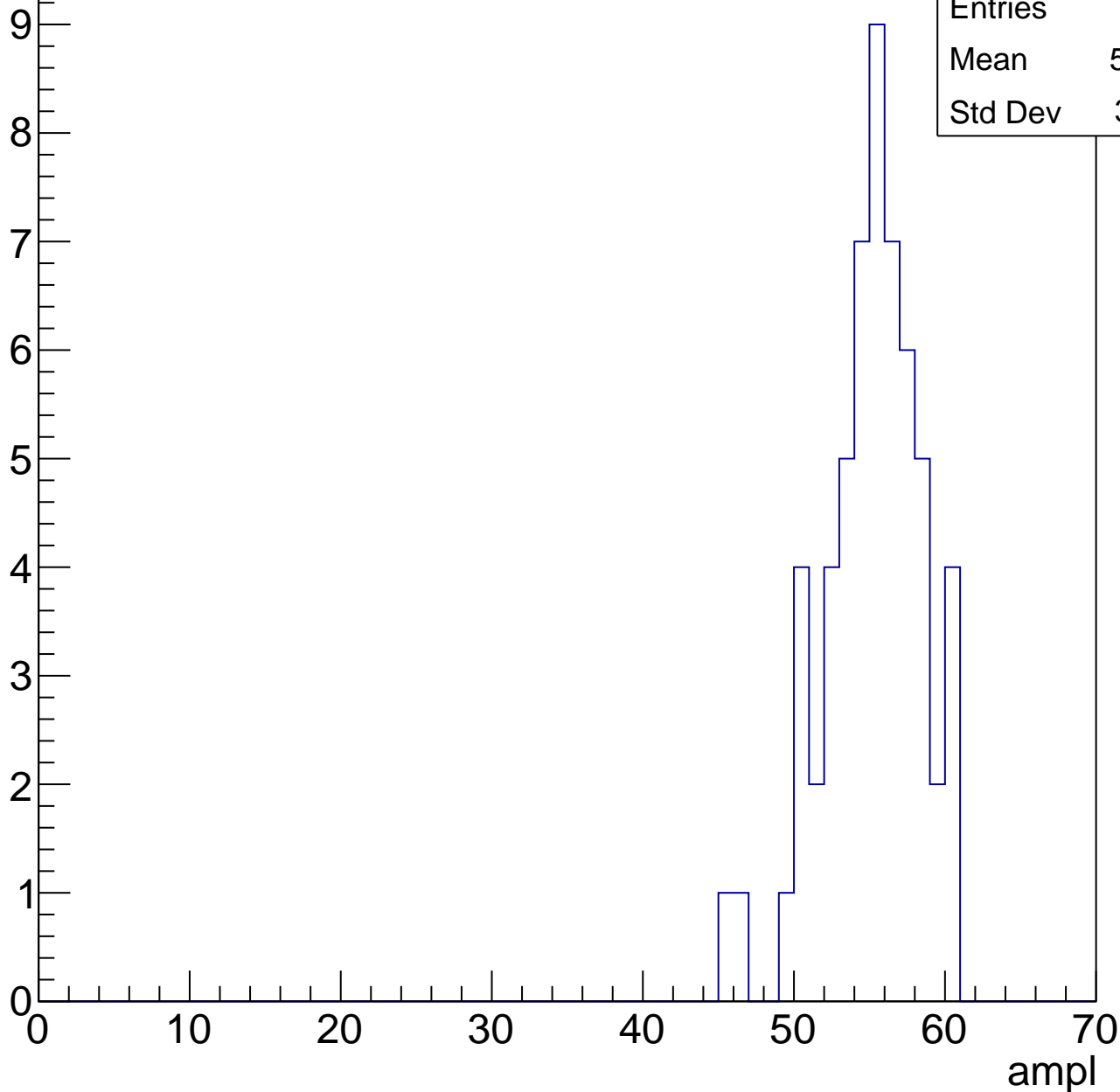
Entries	47
Mean	50.53
Std Dev	3.038



# B1L101S, U19-ch4, adc4

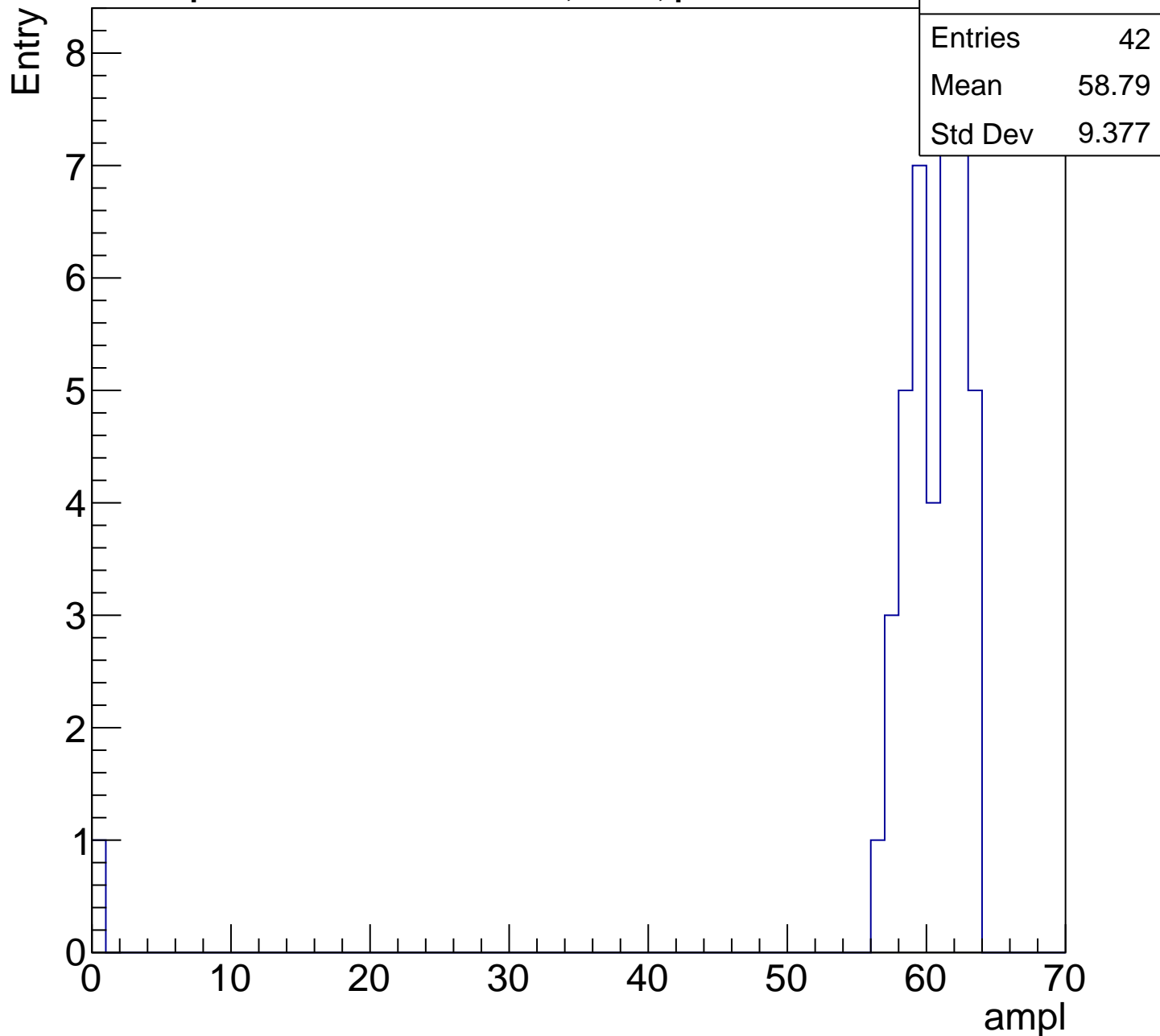
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U19-ch4, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

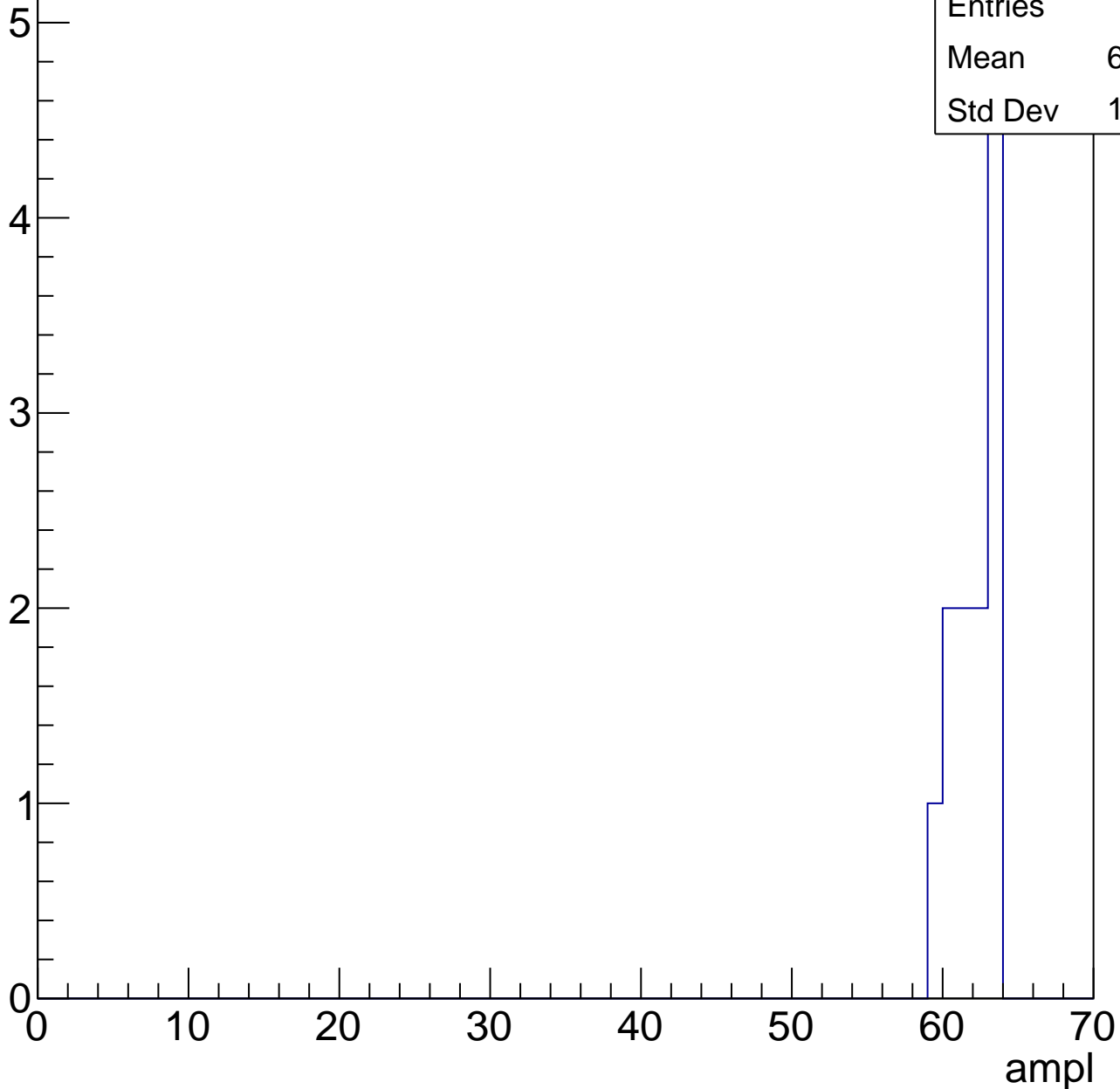


# B1L101S, U19-ch4, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	12
Mean	61.67
Std Dev	1.374





# B1L101S, U19-ch4, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U19-ch5, adc0

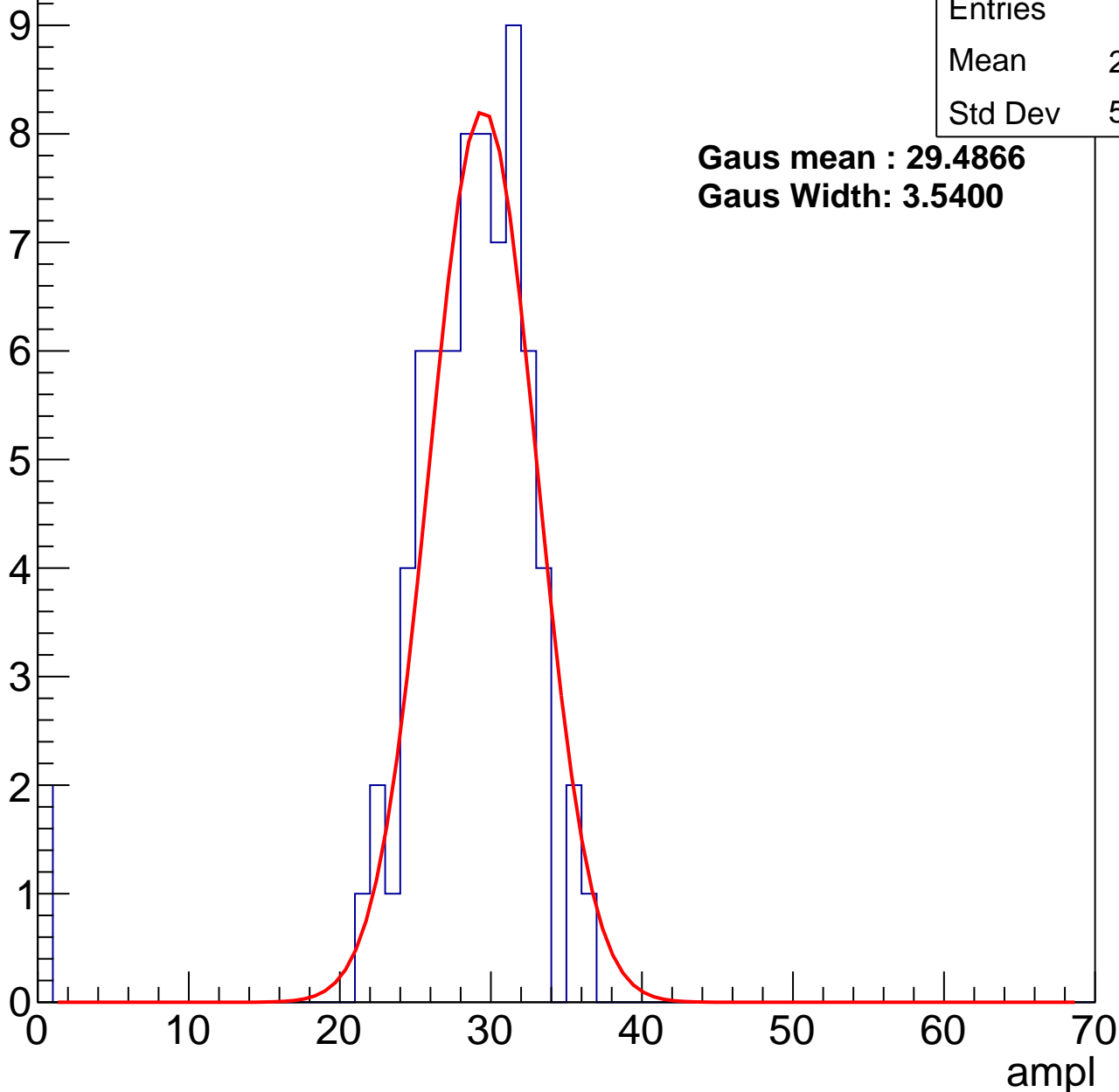
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	73
Mean	27.77
Std Dev	5.653

**Gaus mean : 29.4866**

**Gaus Width: 3.5400**



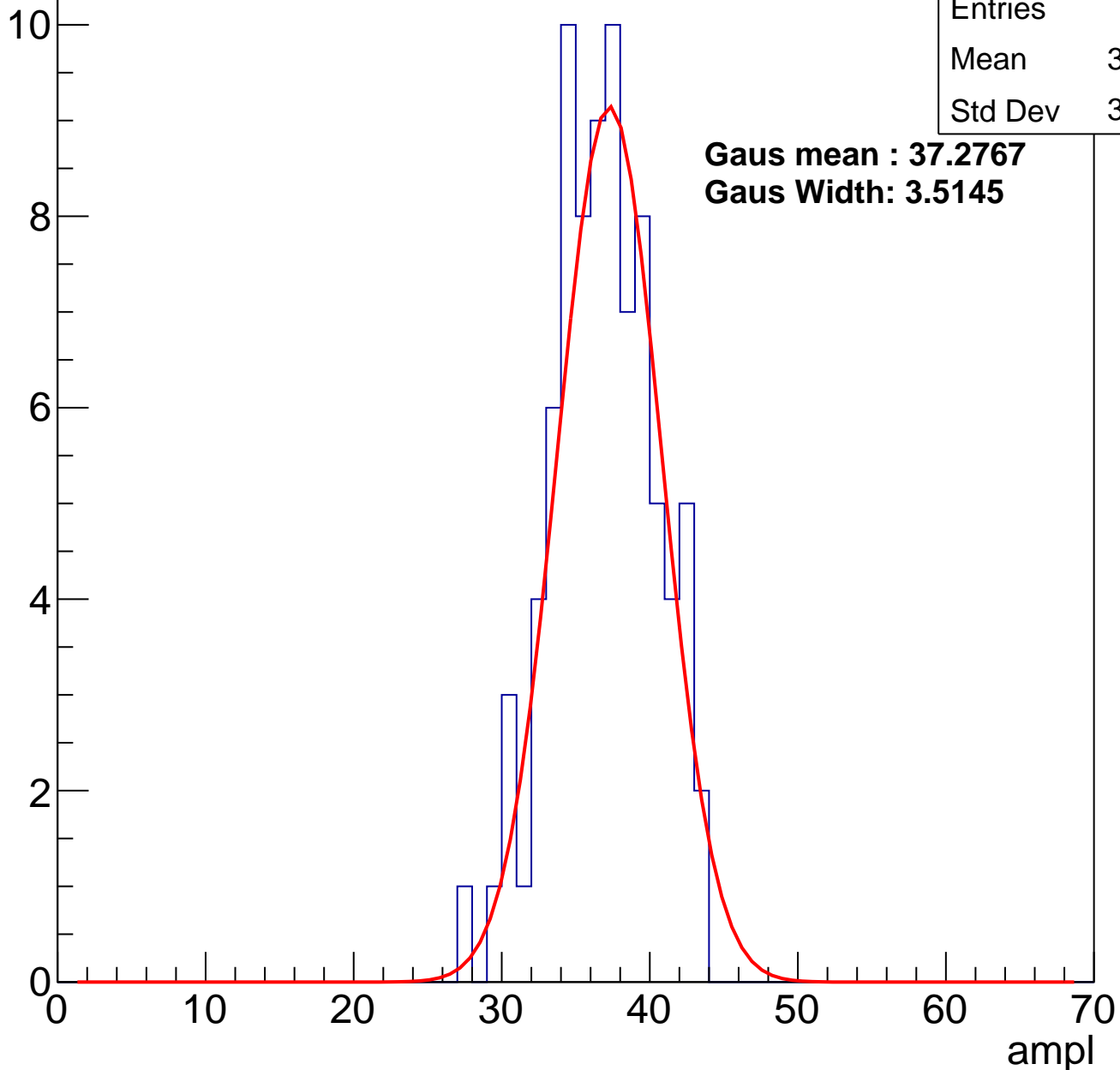
# B1L101S, U19-ch5, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	84
Mean	36.37
Std Dev	3.425

**Gaus mean : 37.2767**  
**Gaus Width: 3.5145**

Entry



# B1L101S, U19-ch5, adc2

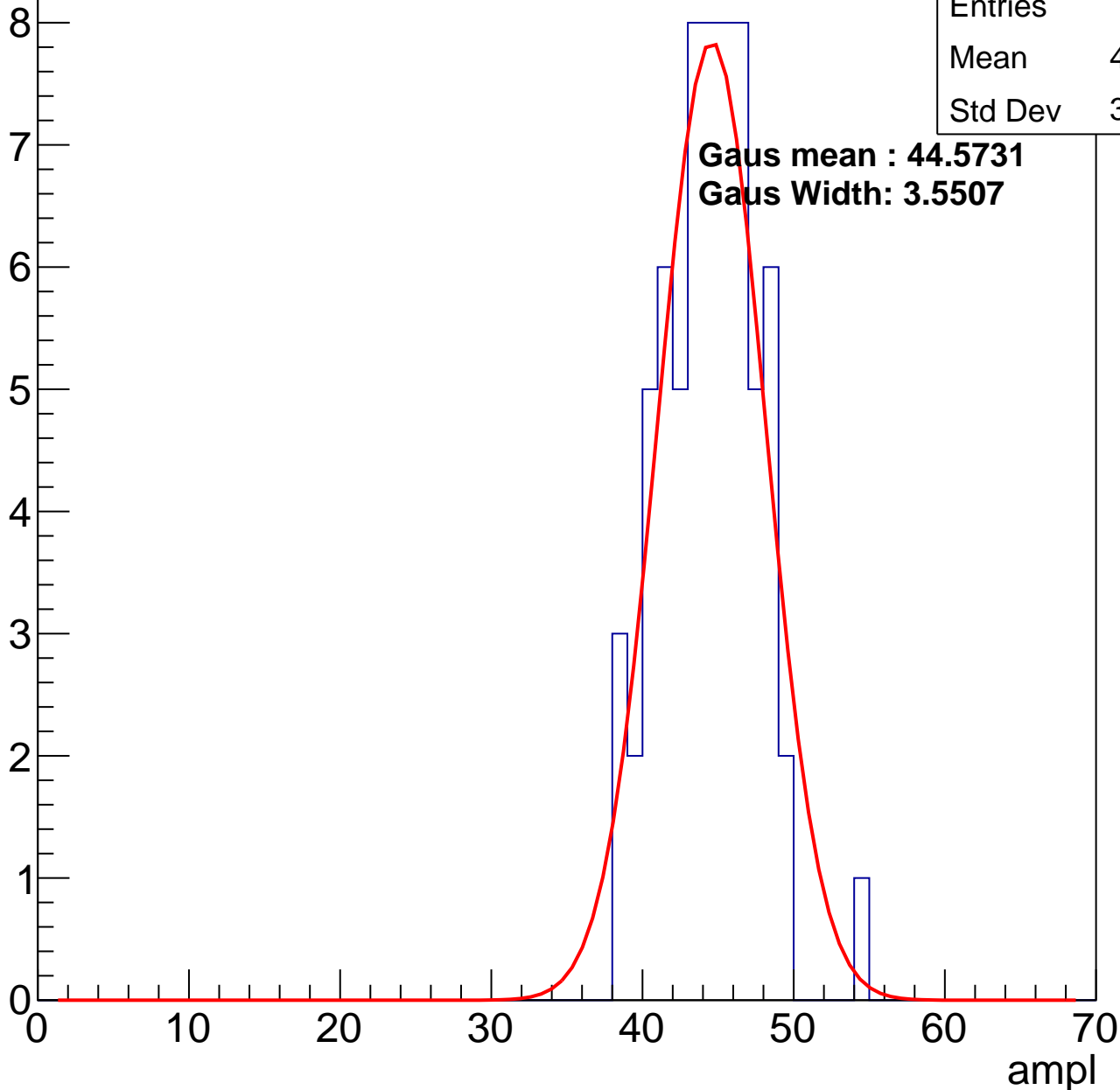
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	67
Mean	43.99
Std Dev	3.117

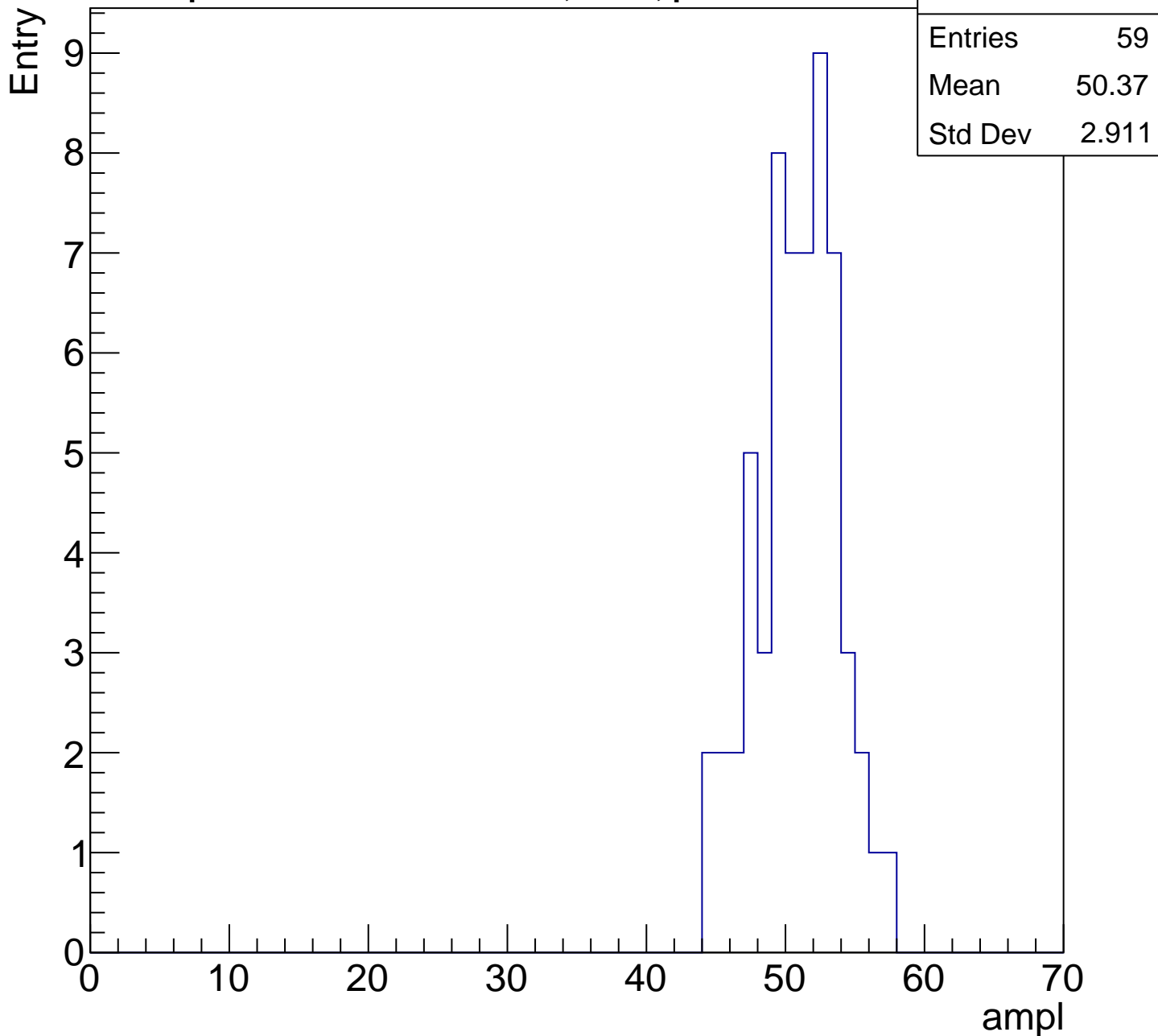
**Gaus mean : 44.5731**

**Gaus Width: 3.5507**



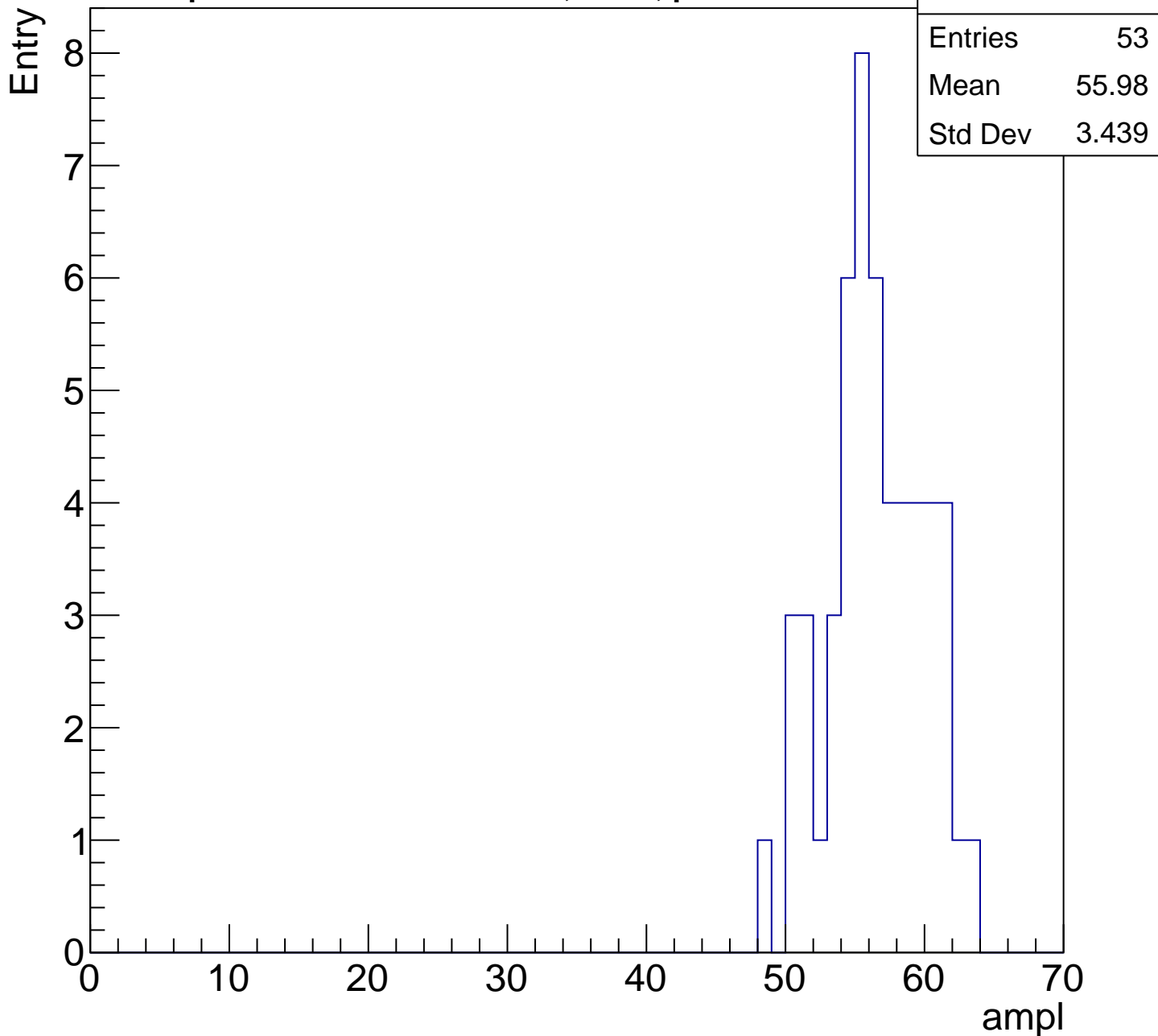
# B1L101S, U19-ch5, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U19-ch5, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

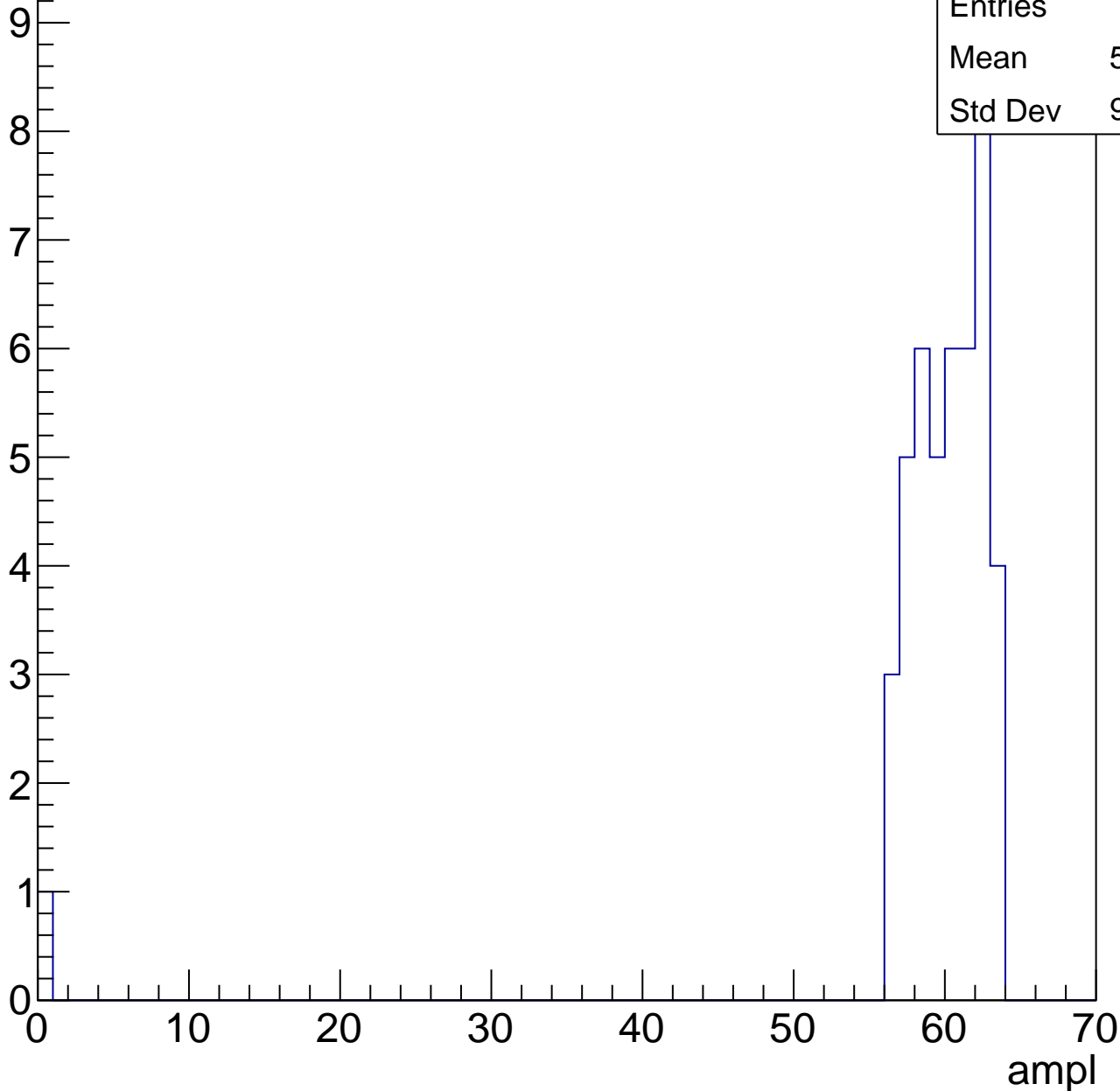


# B1L101S, U19-ch5, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	45
Mean	58.49
Std Dev	9.064



# B1L101S, U19-ch5, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

5

4

3

2

1

0

Entries	6
Mean	62.33
Std Dev	1.491

ampl

0

10

20

30

40

50

60

70



# B1L101S, U19-ch5, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U19-ch6, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	74
Mean	28.14
Std Dev	3.223

**Gaus mean : 28.6363**

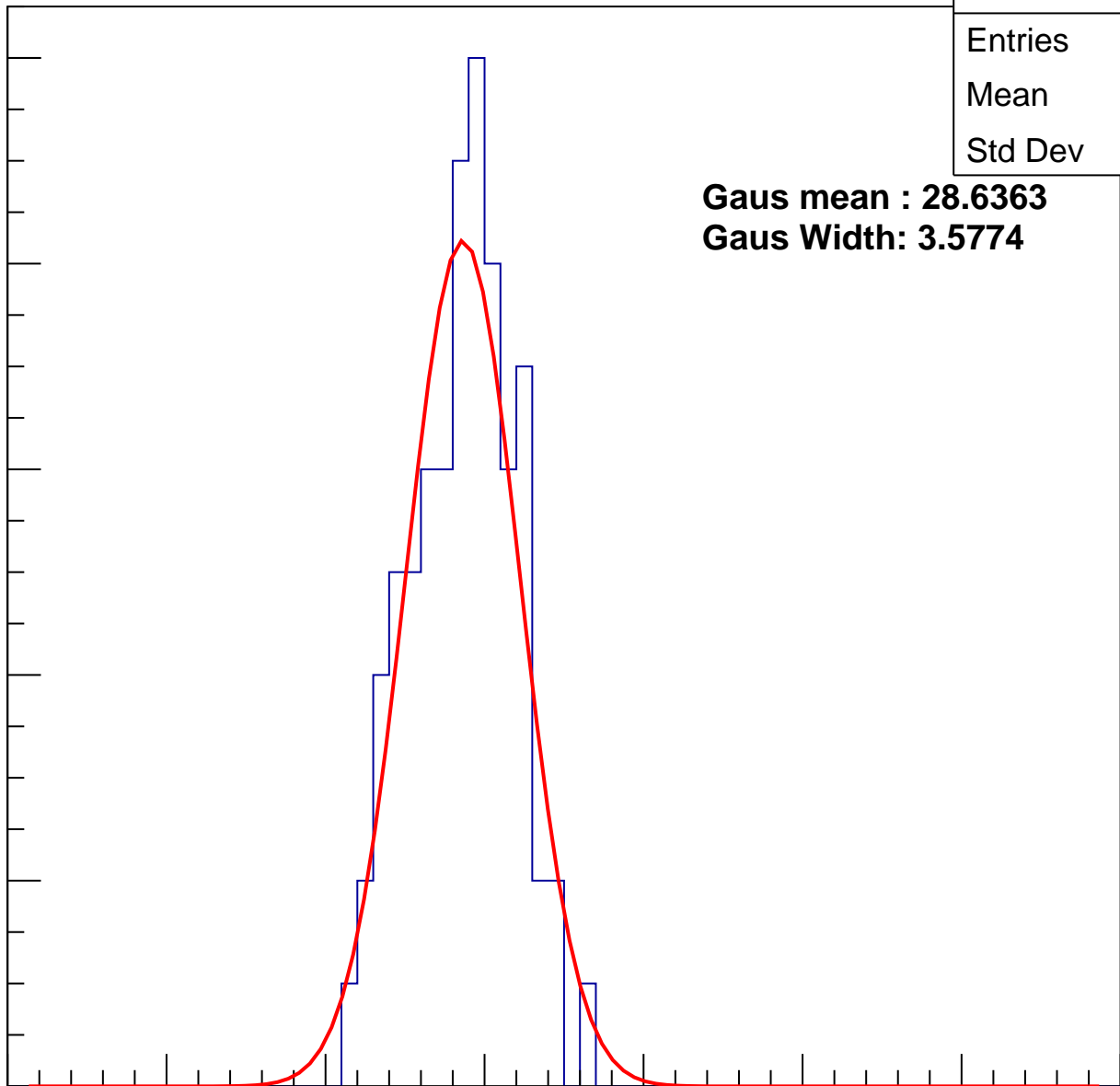
**Gaus Width: 3.5774**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U19-ch6, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	71
Mean	35.69
Std Dev	2.934

**Gaus mean : 36.2980**

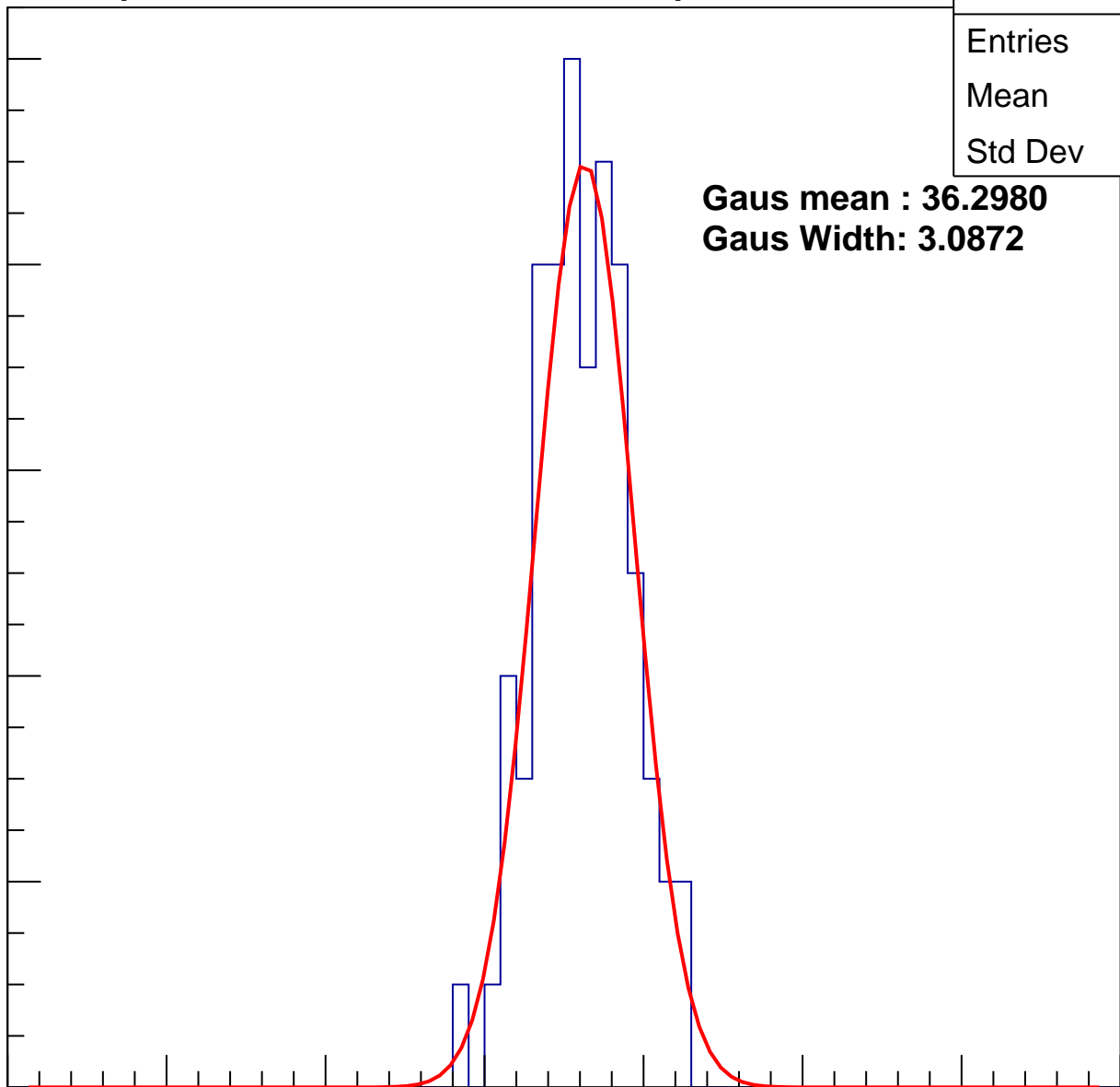
**Gaus Width: 3.0872**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B1L101S, U19-ch6, adc2

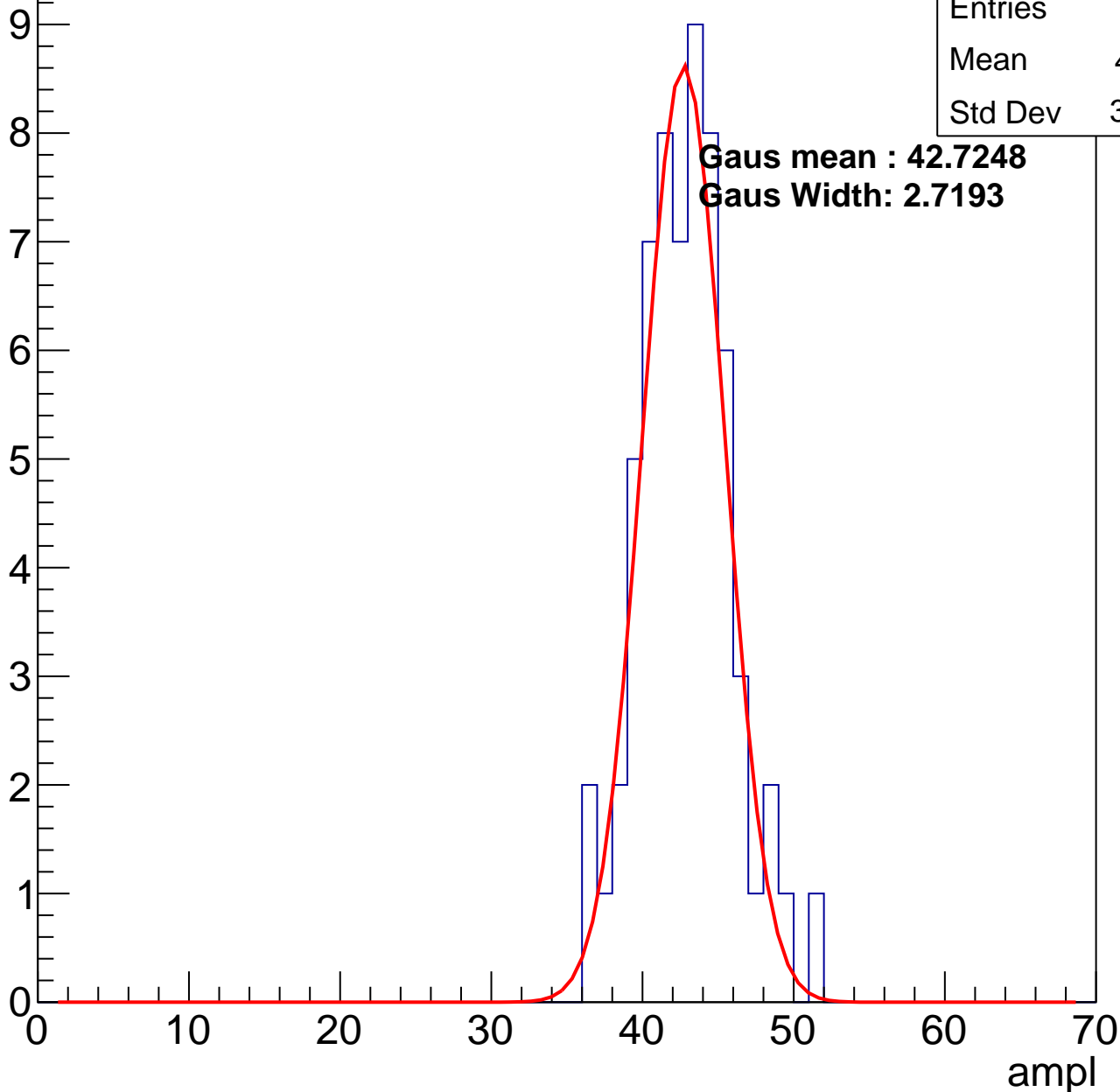
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	42.41
Std Dev	3.006

**Gaus mean : 42.7248**

**Gaus Width: 2.7193**

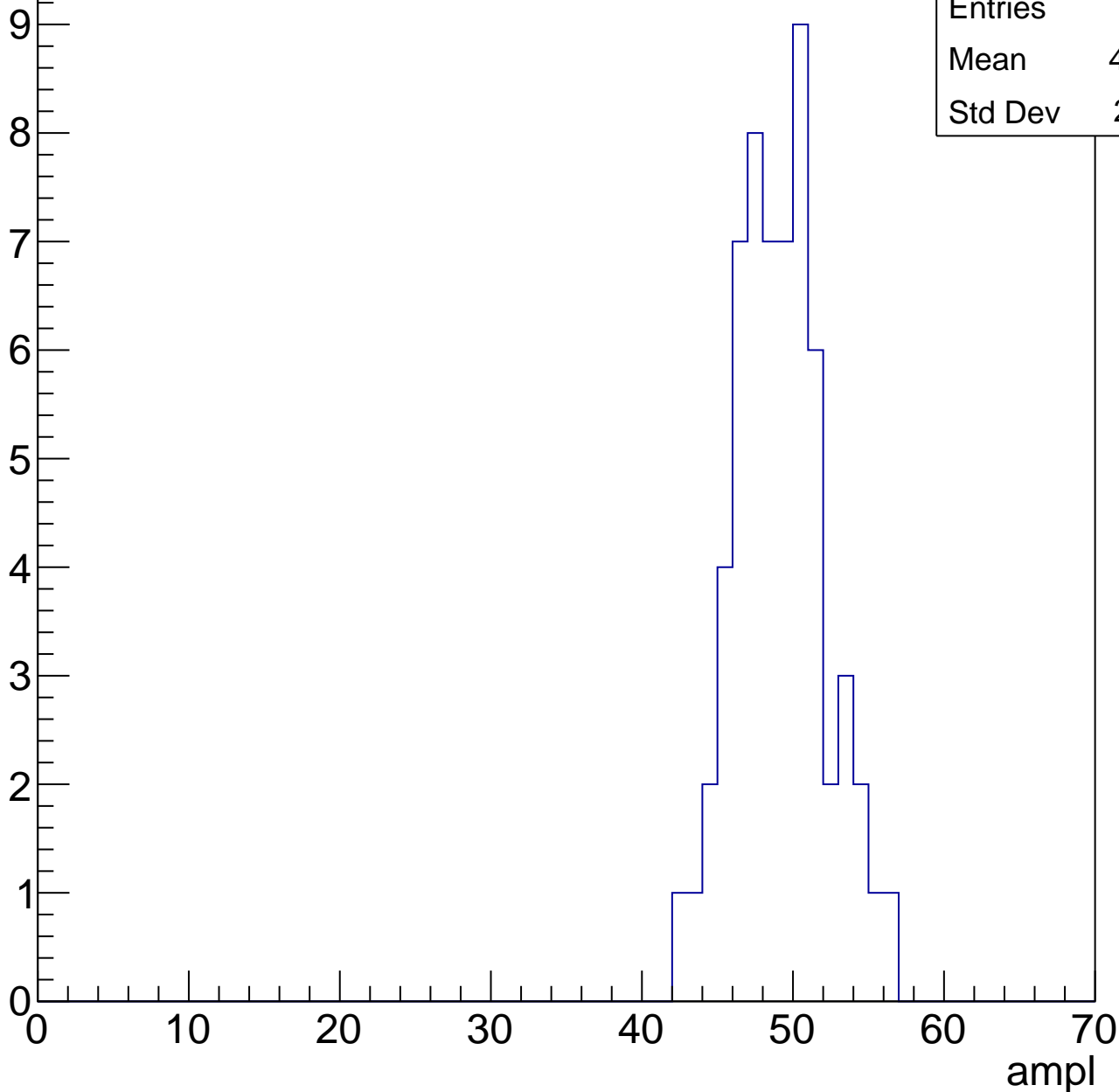


# B1L101S, U19-ch6, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

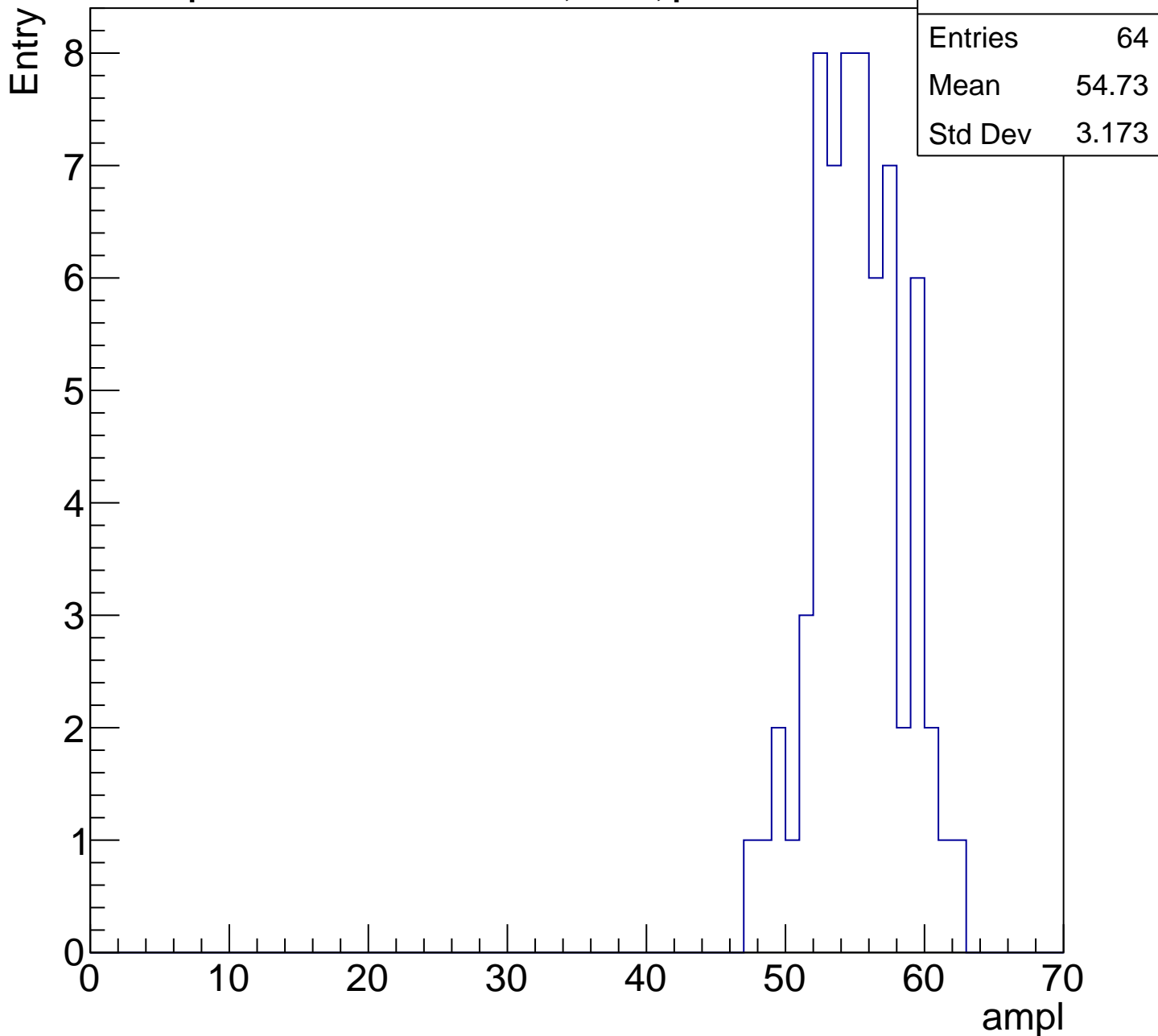
Entry

Entries	61
Mean	48.66
Std Dev	2.941



# B1L101S, U19-ch6, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U19-ch6, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

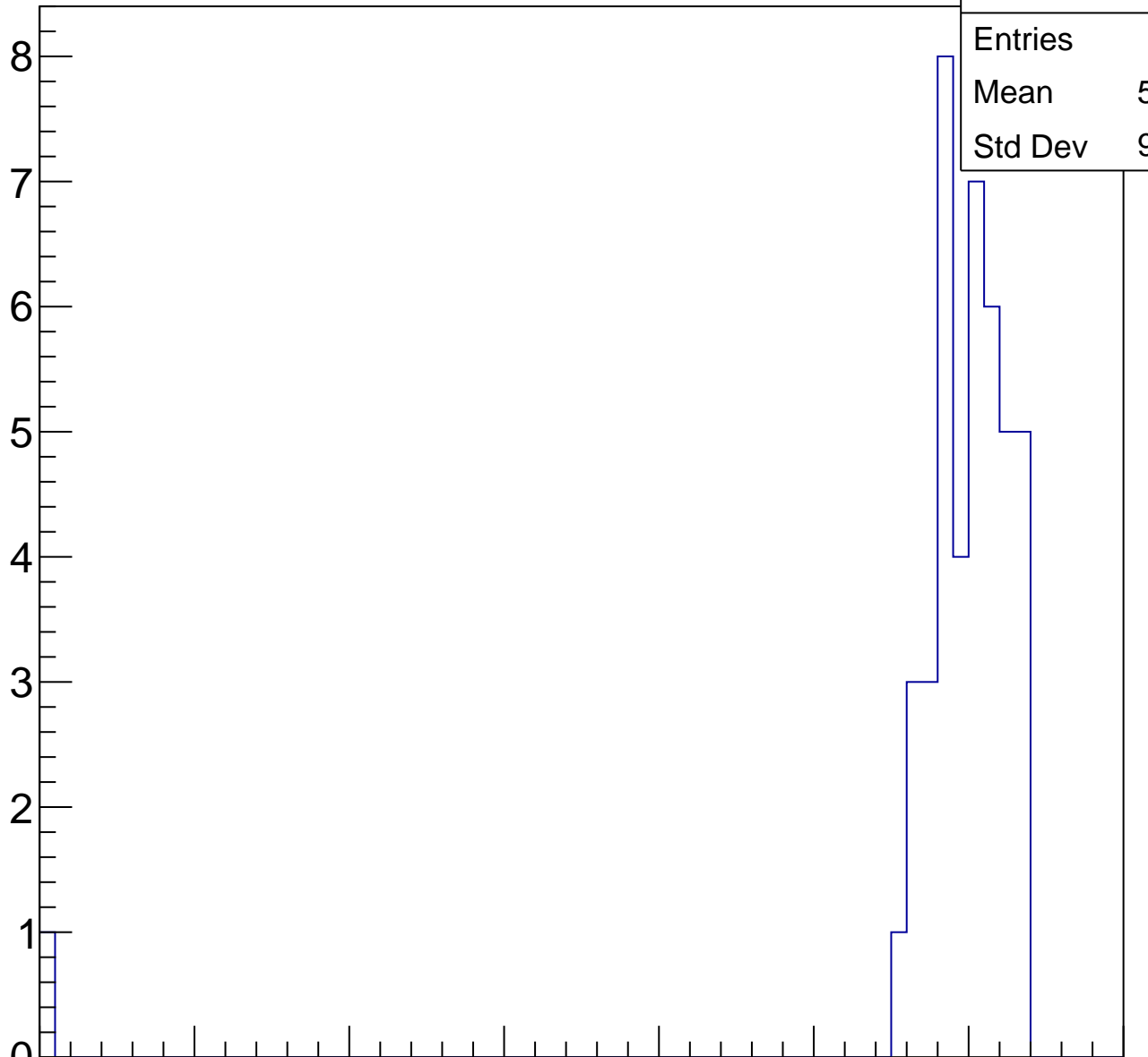
Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	43
Mean	58.26
Std Dev	9.246

ampl

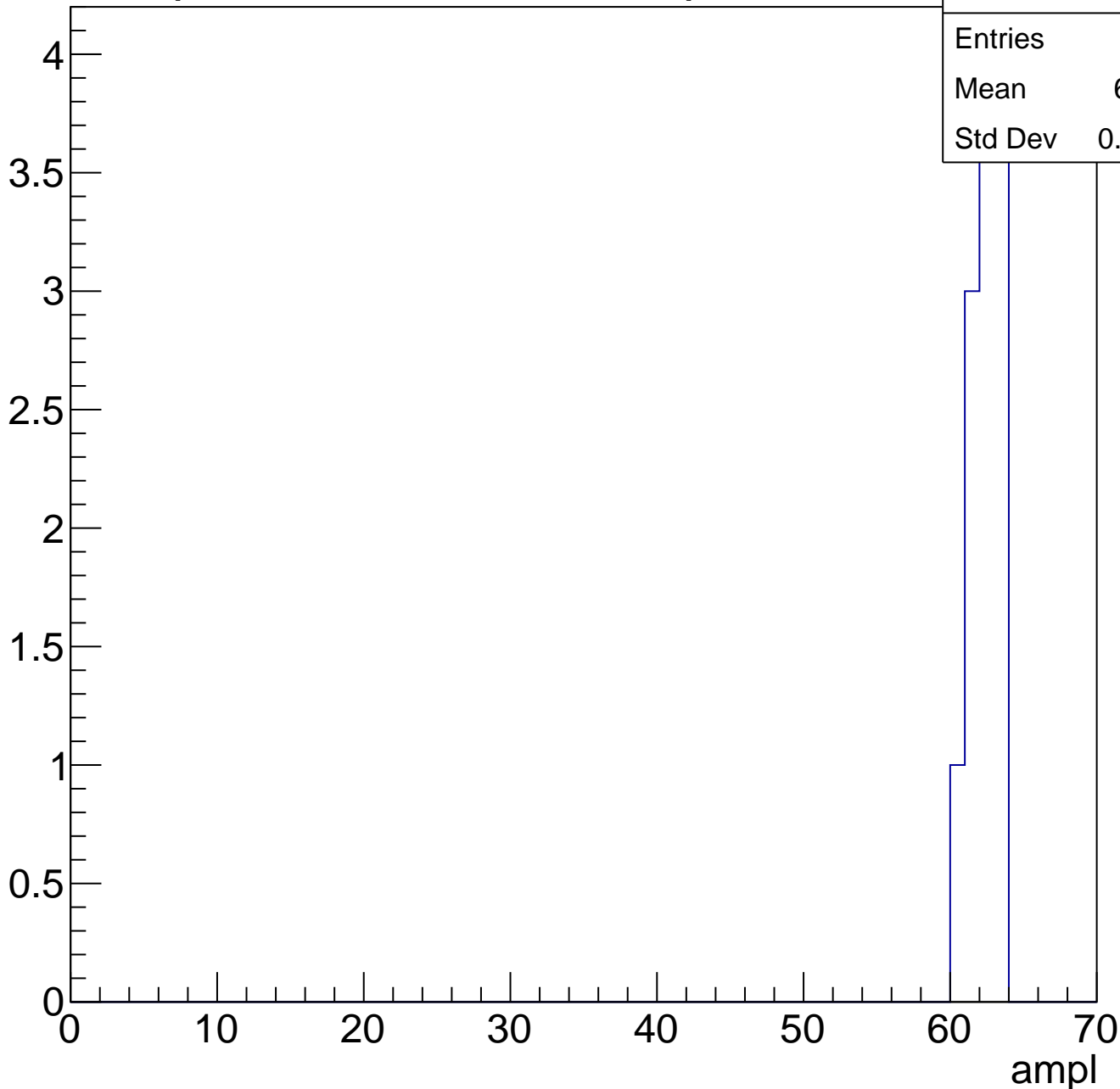
0 10 20 30 40 50 60 70



# B1L101S, U19-ch6, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

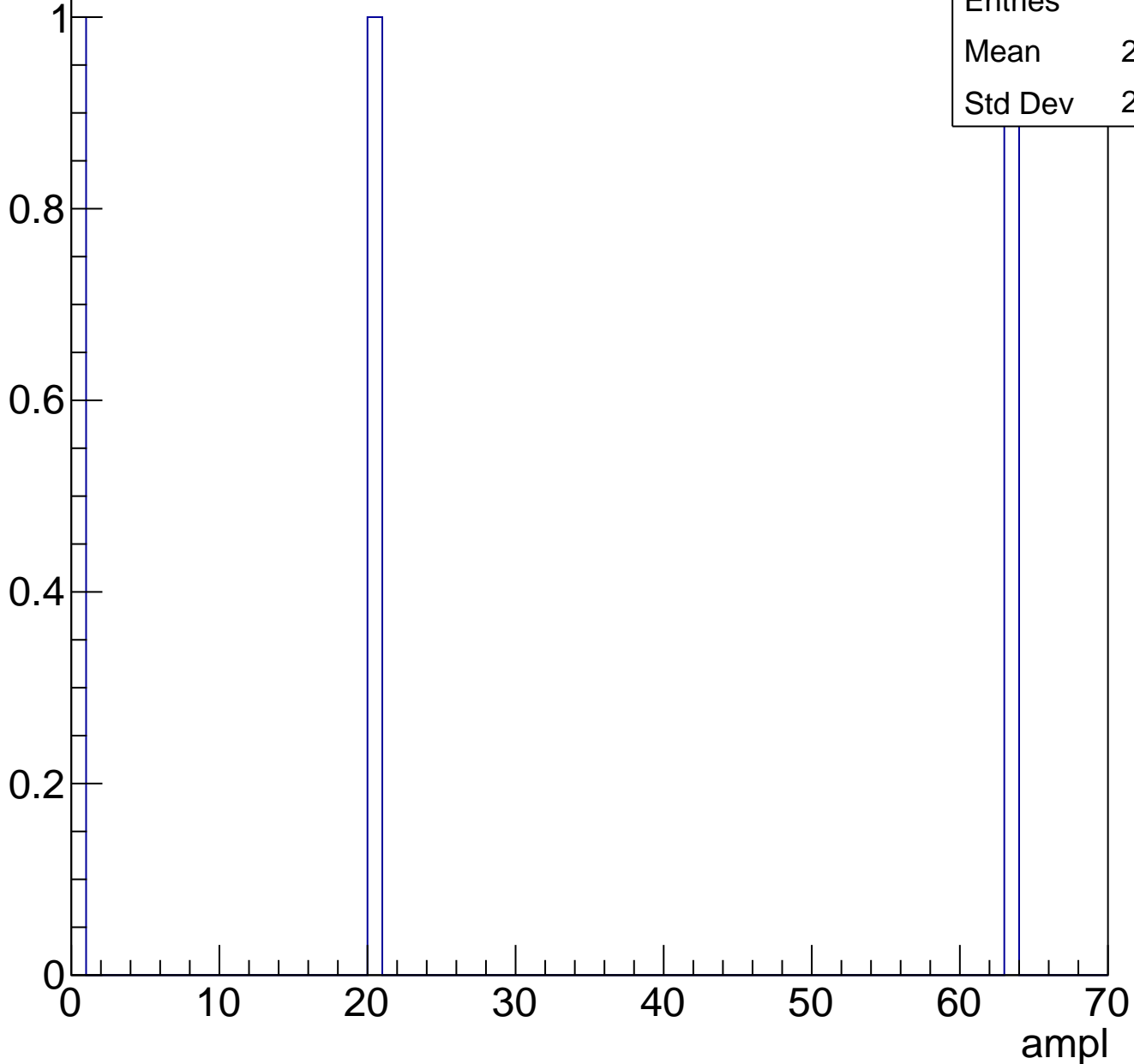




# B1L101S, U19-ch6, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	3
Mean	27.67
Std Dev	26.28

# B1L101S, U19-ch7, adc0

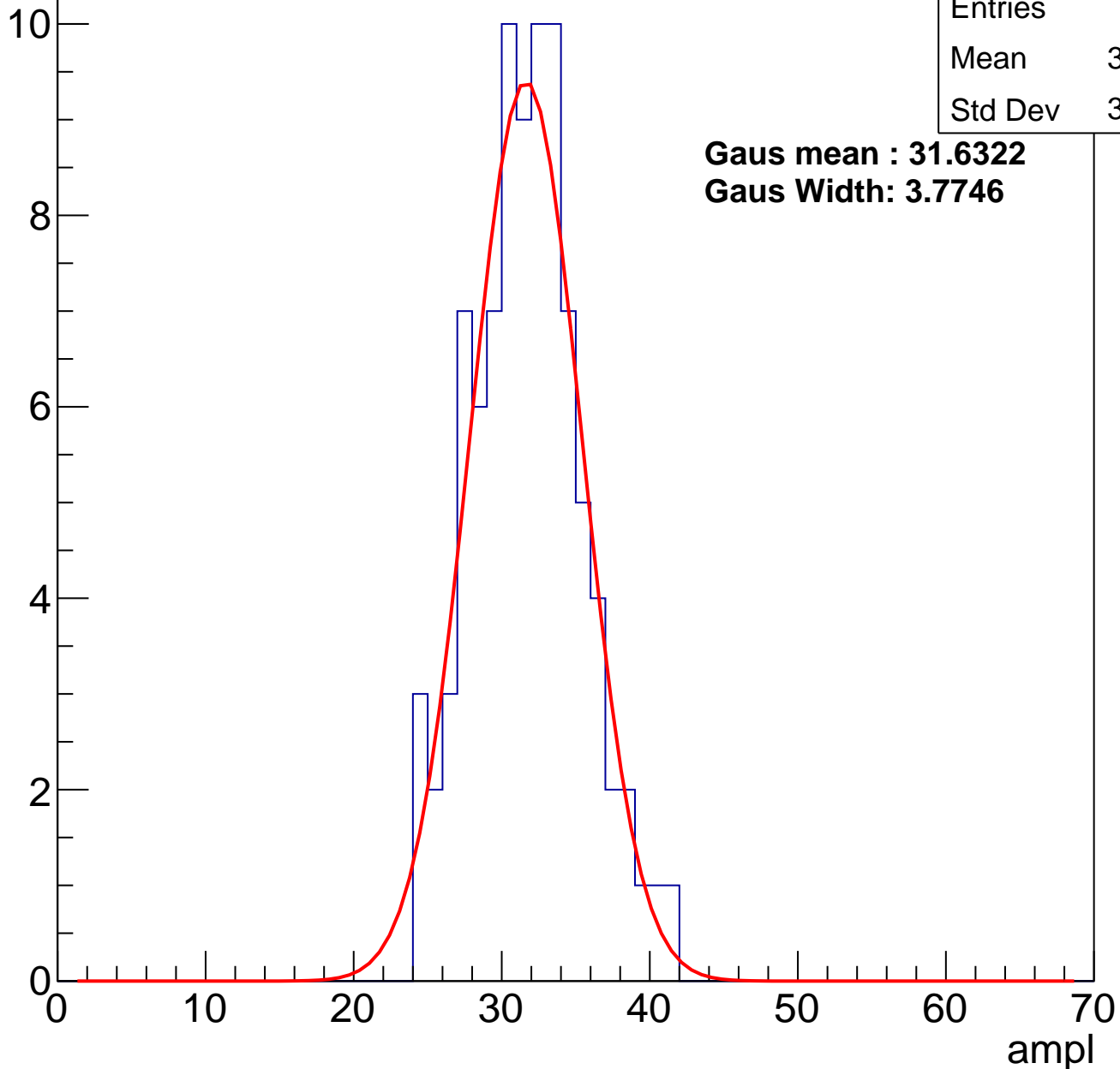
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	90
Mean	31.29
Std Dev	3.649

**Gaus mean : 31.6322**

**Gaus Width: 3.7746**

Entry



# B1L101S, U19-ch7, adc1

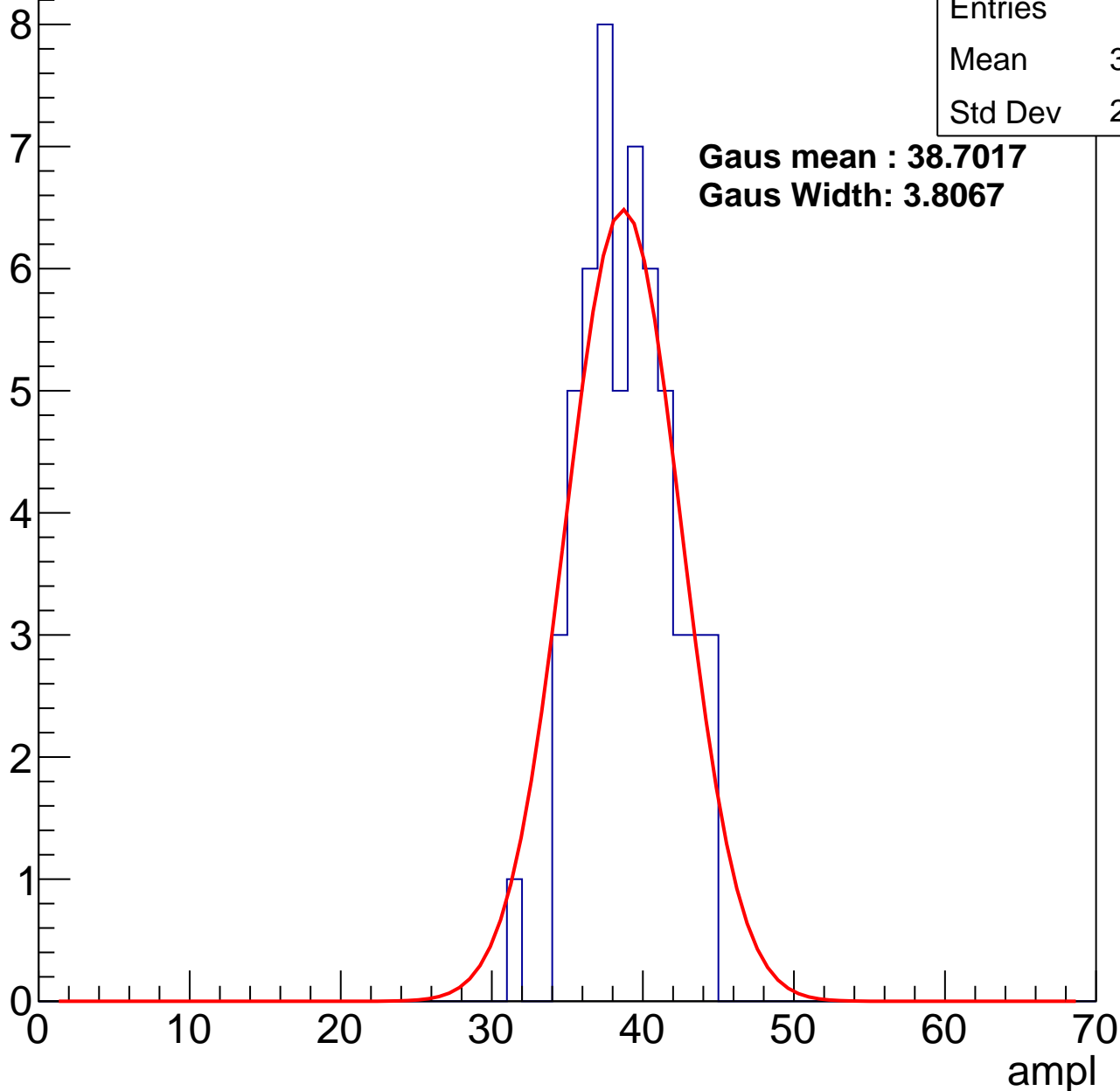
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	55
Mean	38.45
Std Dev	2.922

**Gaus mean : 38.7017**

**Gaus Width: 3.8067**



# B1L101S, U19-ch7, adc2

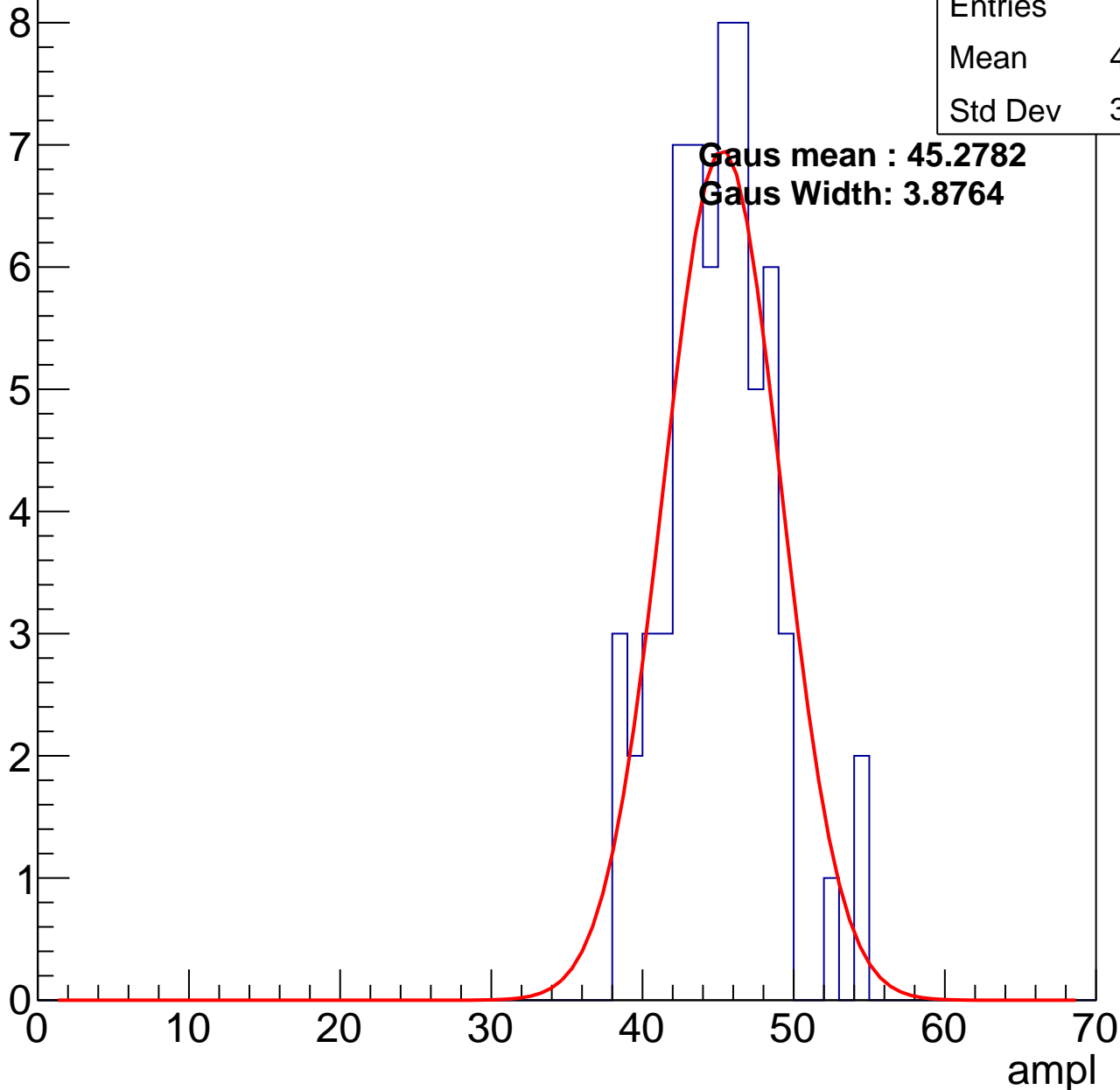
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	44.56
Std Dev	3.464

**Gaus mean : 45.2782**

**Gaus Width: 3.8764**

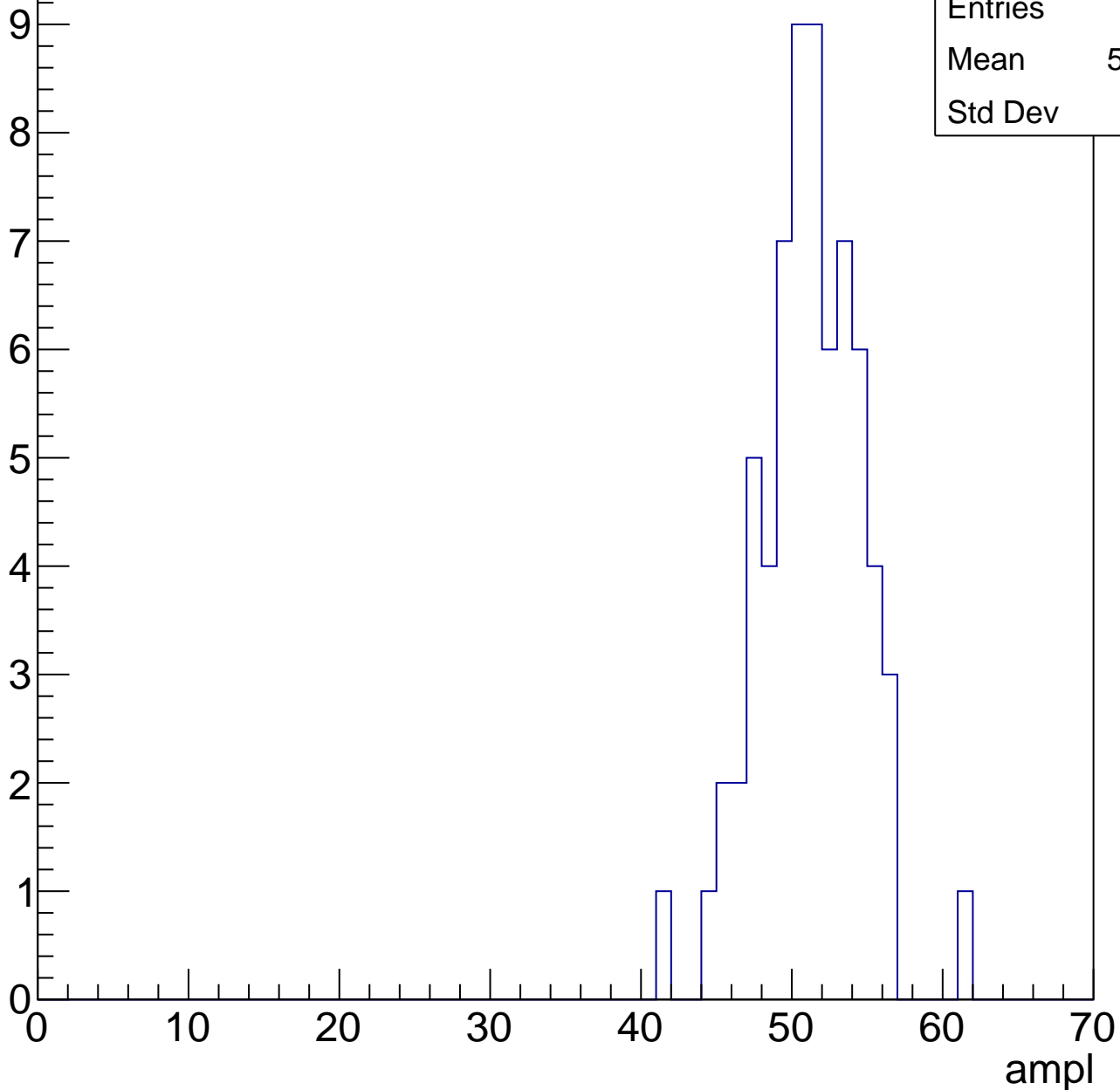


# B1L101S, U19-ch7, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

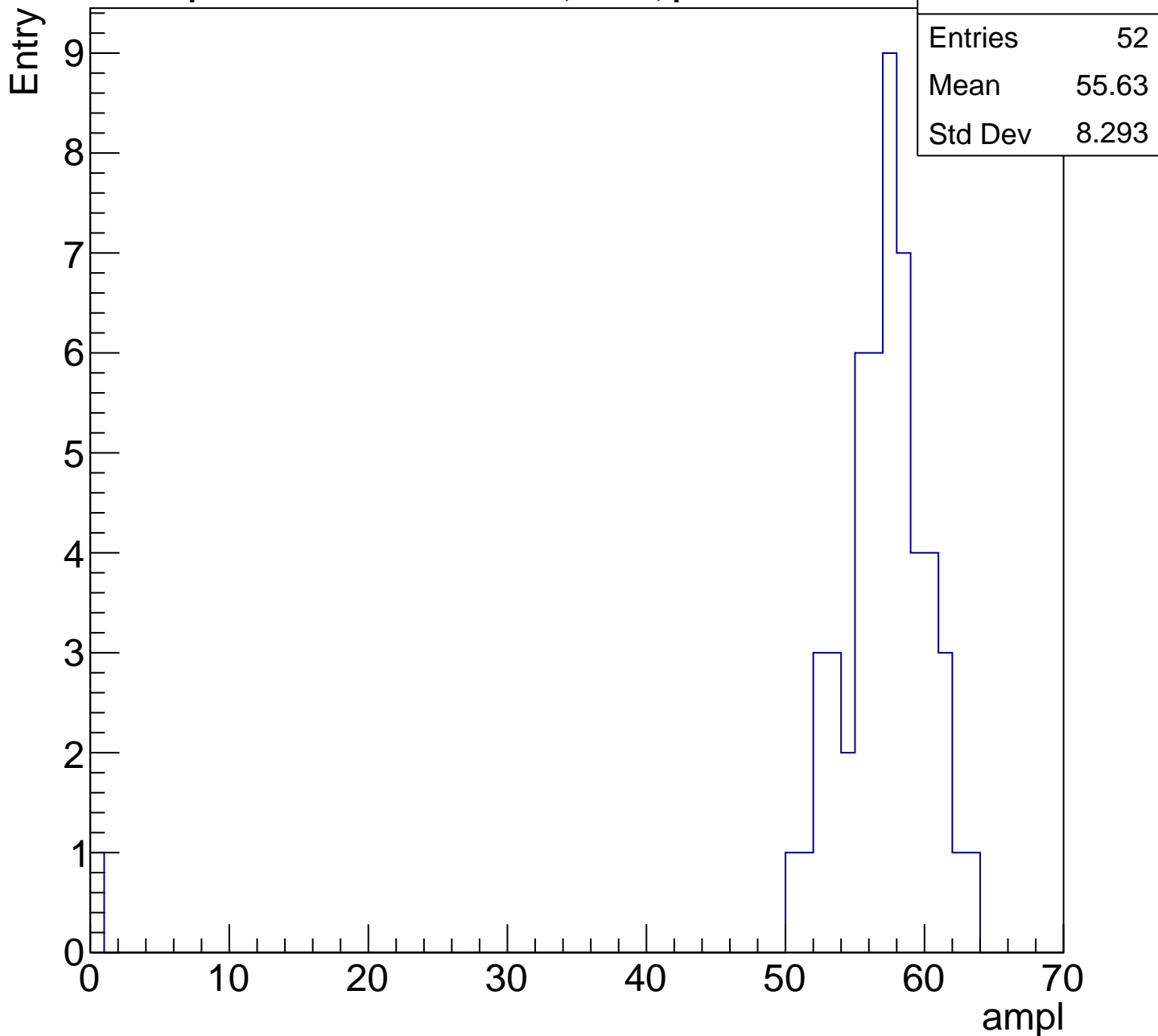
Entry

Entries	67
Mean	50.78
Std Dev	3.34



# B1L101S, U19-ch7, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

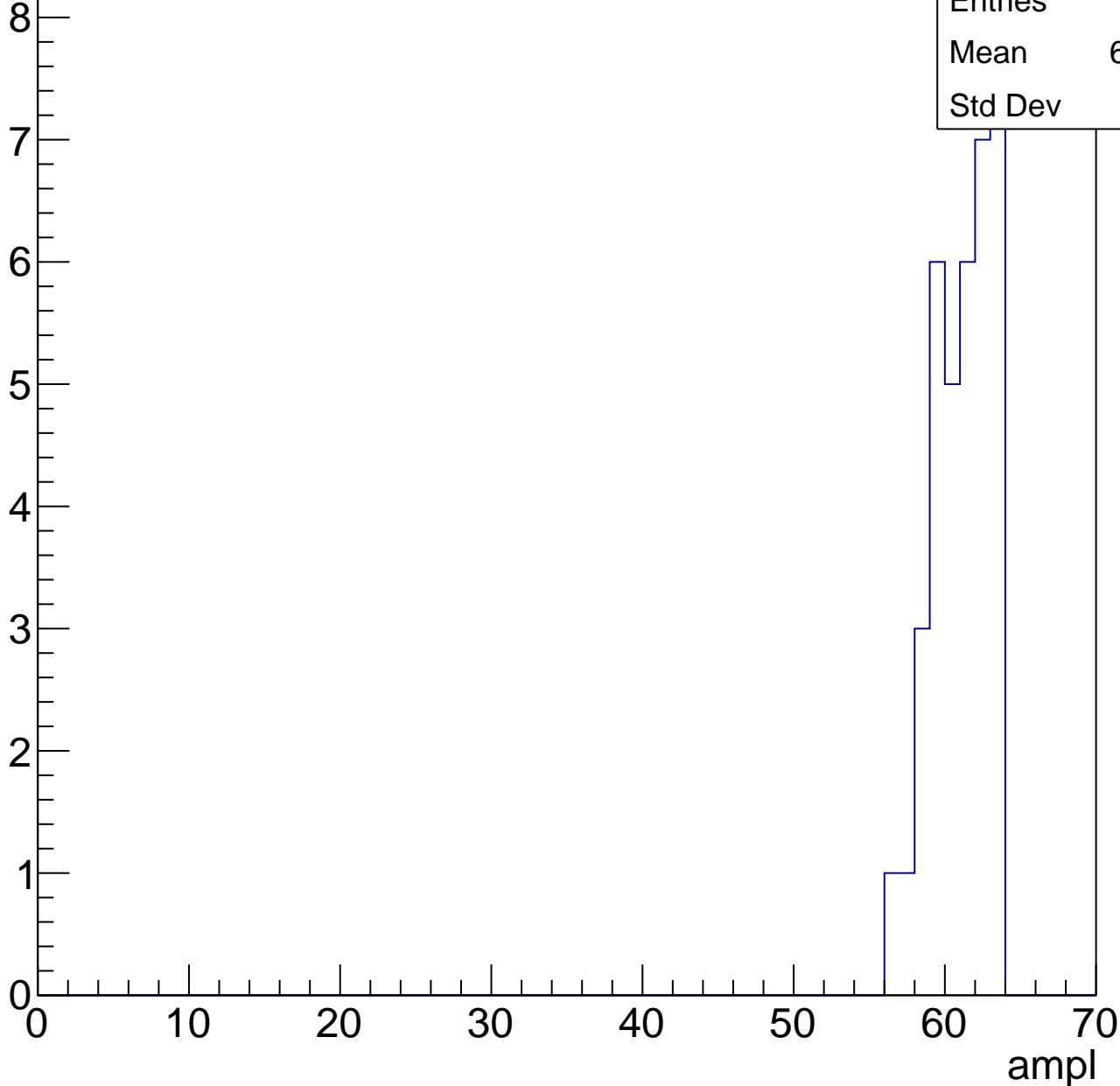


# B1L101S, U19-ch7, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	37
Mean	60.68
Std Dev	1.89



# B1L101S, U19-ch7, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

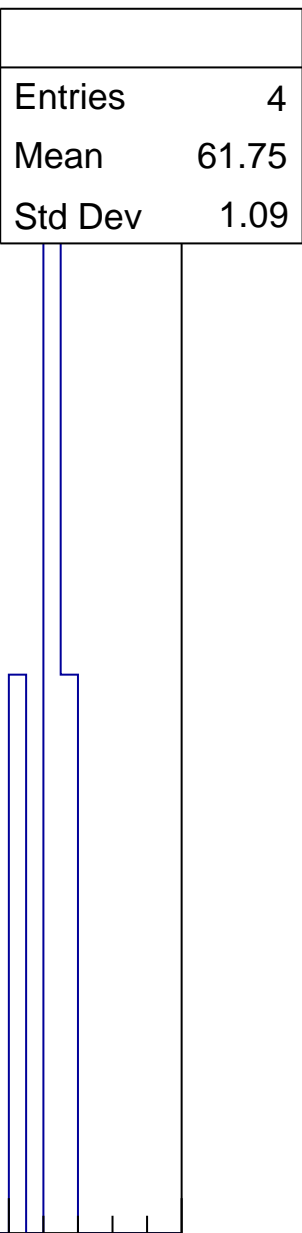
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	4
Mean	61.75
Std Dev	1.09

0 10 20 30 40 50 60 70

ampl





# B1L101S, U19-ch7, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

1  
0.8  
0.6  
0.4  
0.2  
0

Entries	1
Mean	23
Std Dev	0

ampl

# B1L101S, U19-ch8, adc0

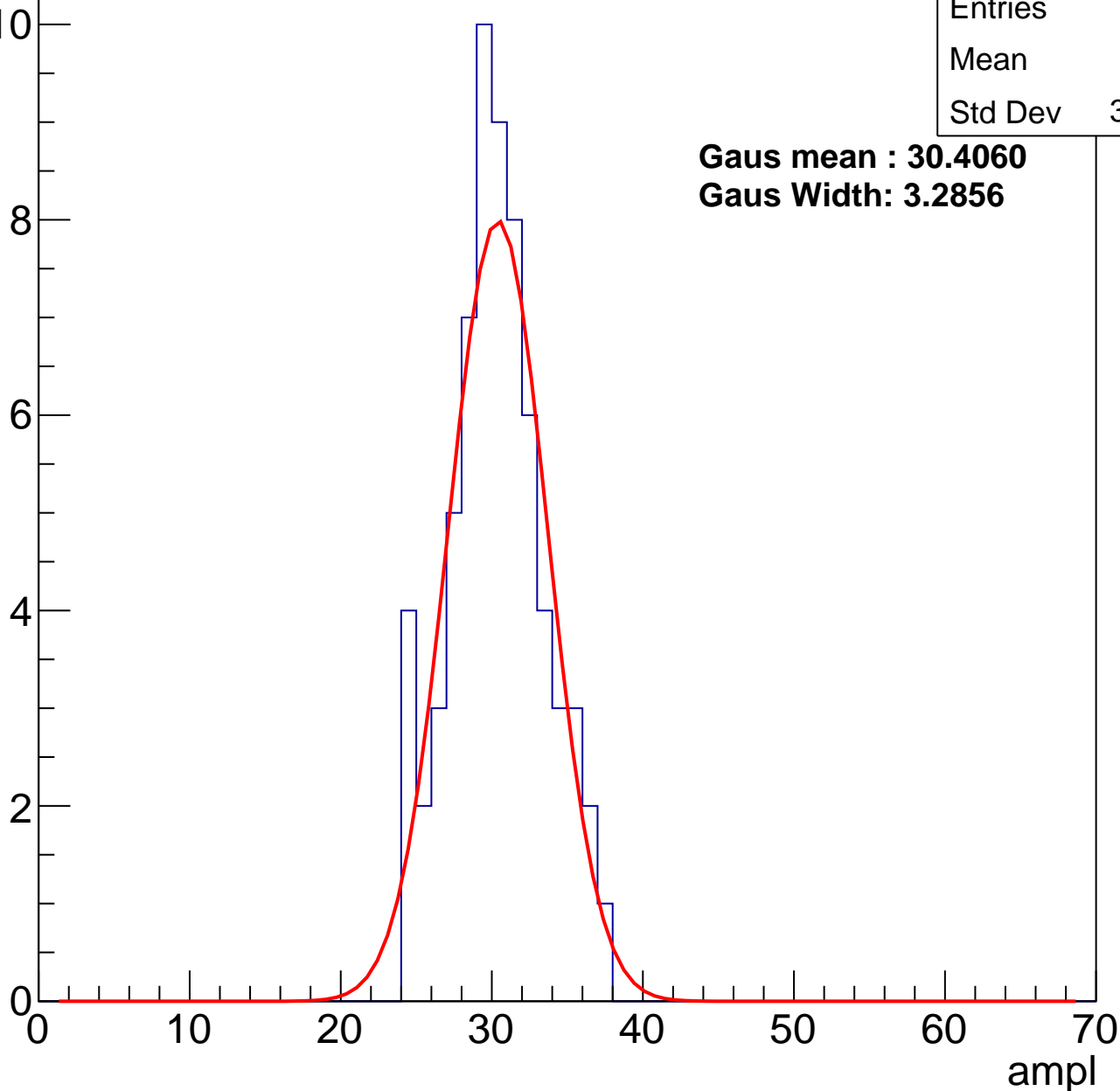
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	67
Mean	29.9
Std Dev	3.082

**Gaus mean : 30.4060**

**Gaus Width: 3.2856**



# B1L101S, U19-ch8, adc1

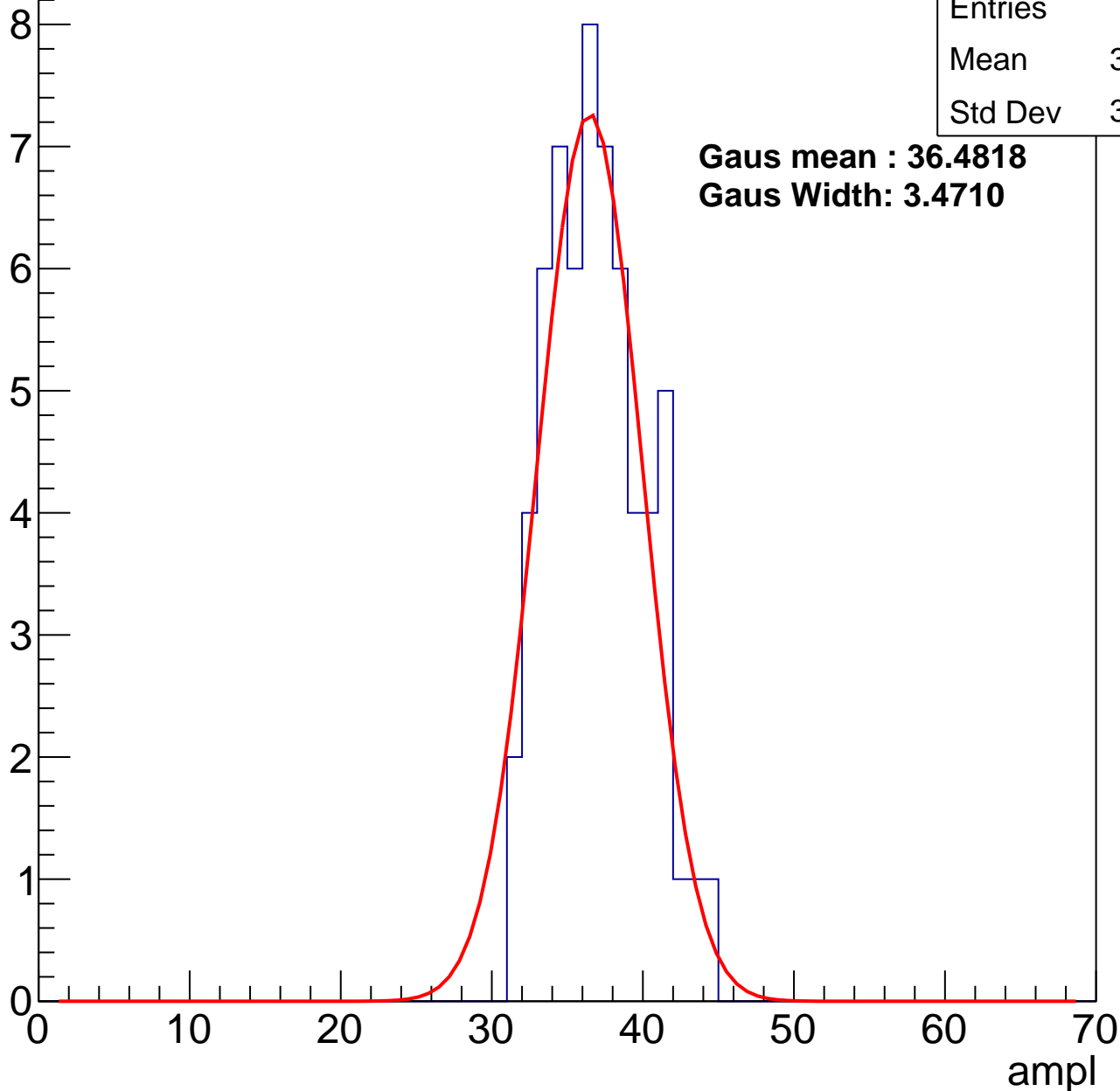
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	36.47
Std Dev	3.094

**Gaus mean : 36.4818**

**Gaus Width: 3.4710**



# B1L101S, U19-ch8, adc2

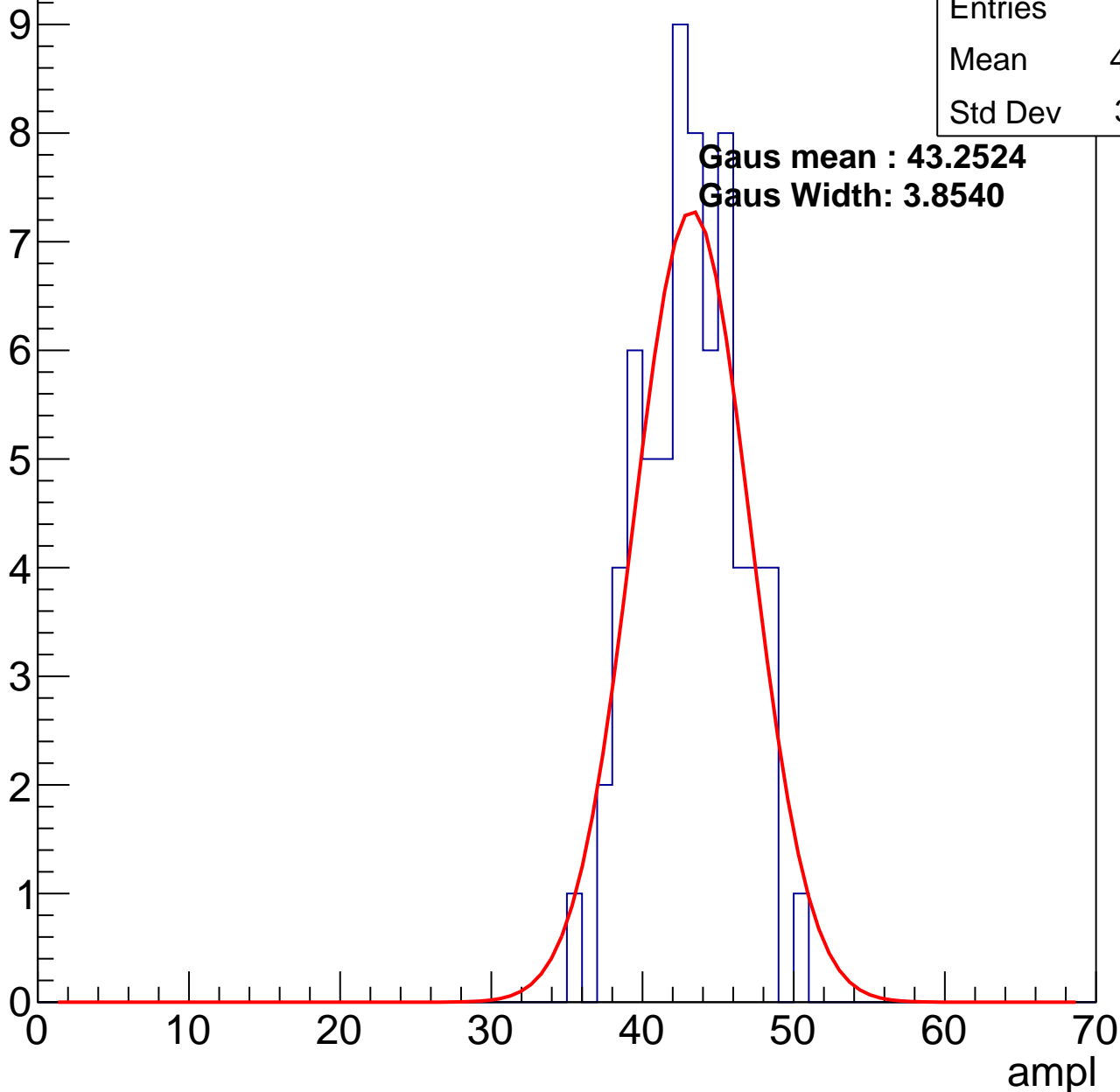
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	67
Mean	42.69
Std Dev	3.201

**Gaus mean : 43.2524**

**Gaus Width: 3.8540**

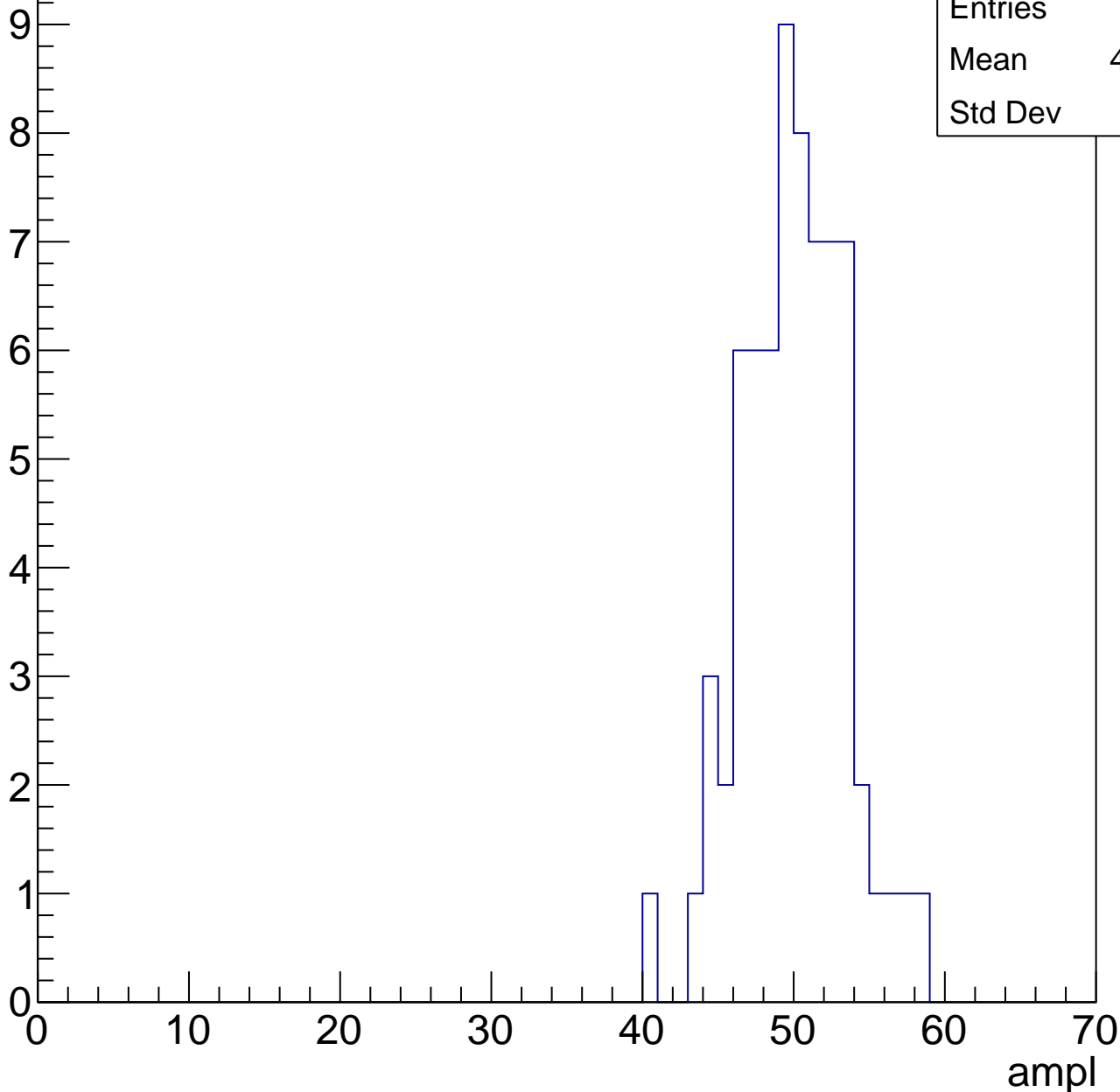


# B1L101S, U19-ch8, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	49.54
Std Dev	3.36

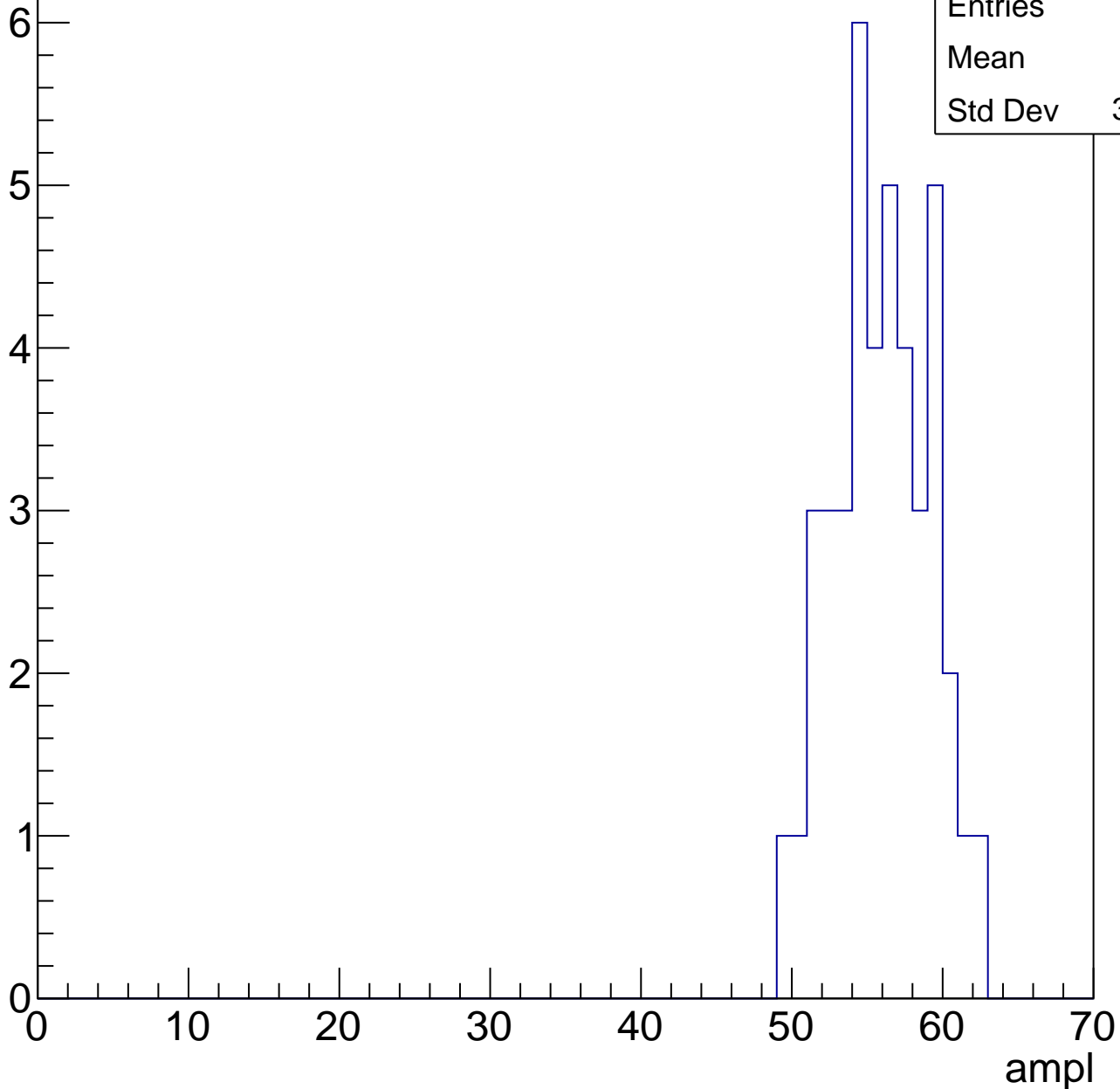


# B1L101S, U19-ch8, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	42
Mean	55.5
Std Dev	3.111

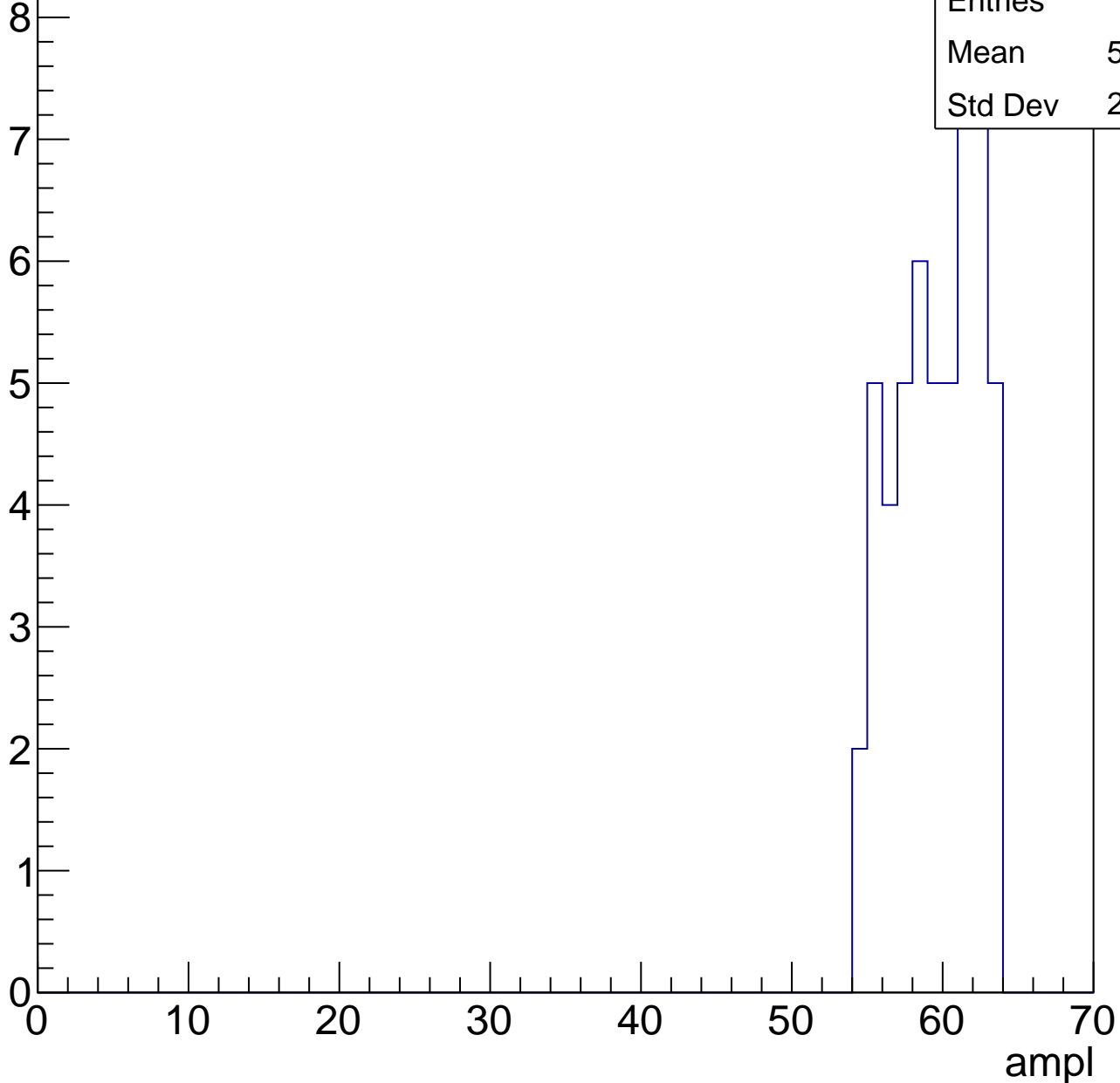


# B1L101S, U19-ch8, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

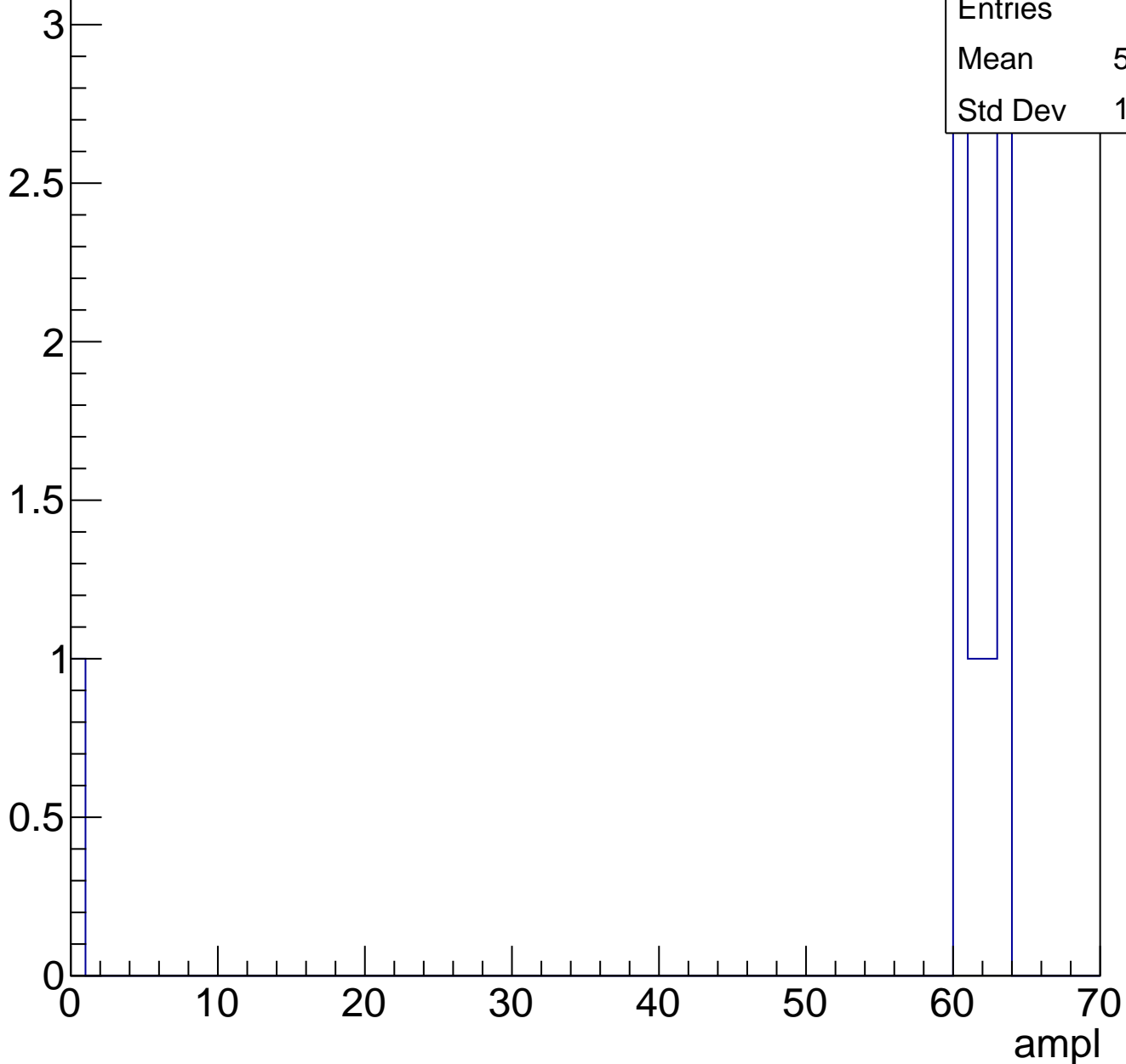
Entries	53
Mean	59.13
Std Dev	2.678



# B1L101S, U19-ch8, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U19-ch8, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U19-ch9, adc0

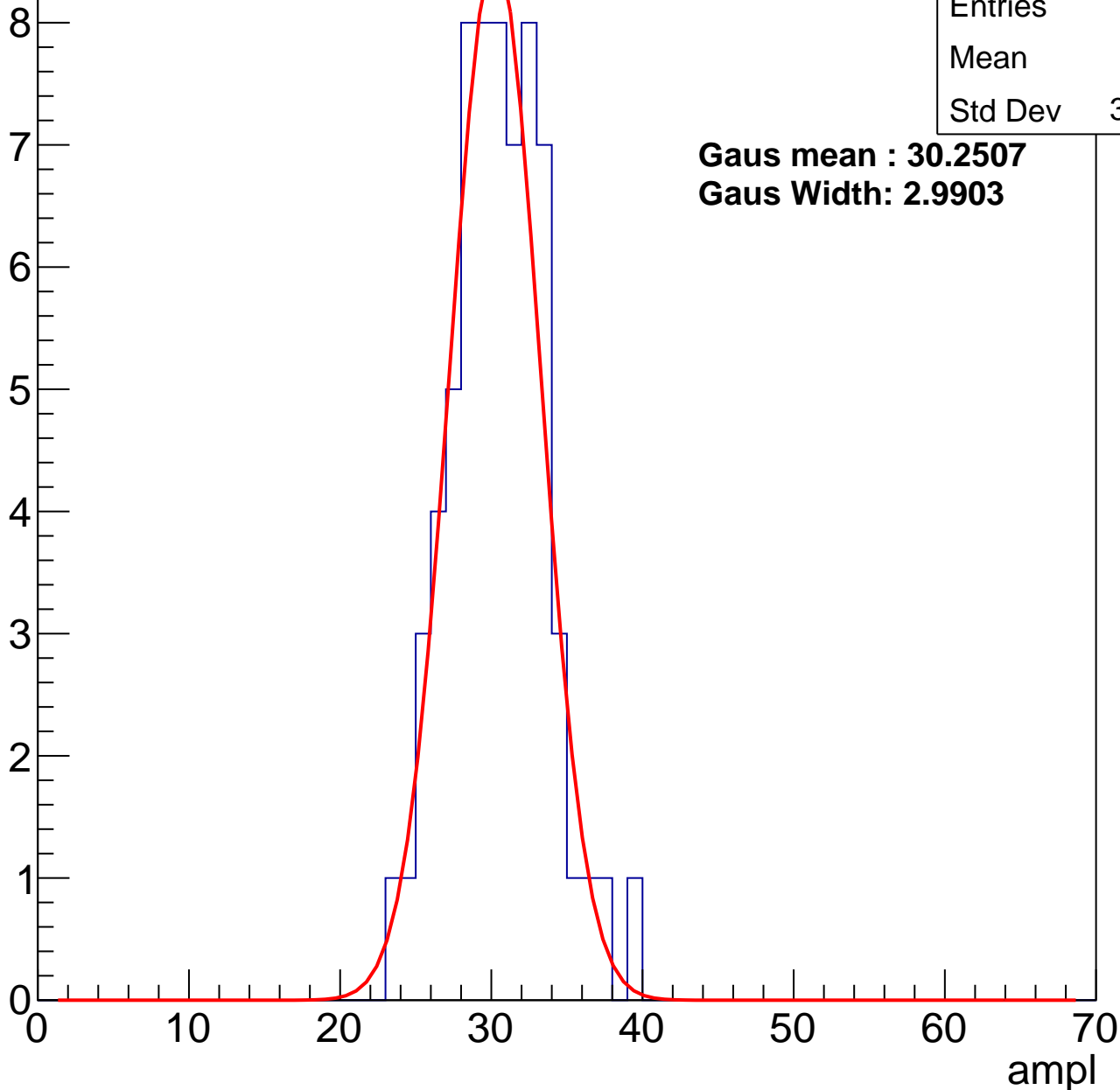
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	67
Mean	30
Std Dev	3.115

**Gaus mean : 30.2507**

**Gaus Width: 2.9903**



# B1L101S, U19-ch9, adc1

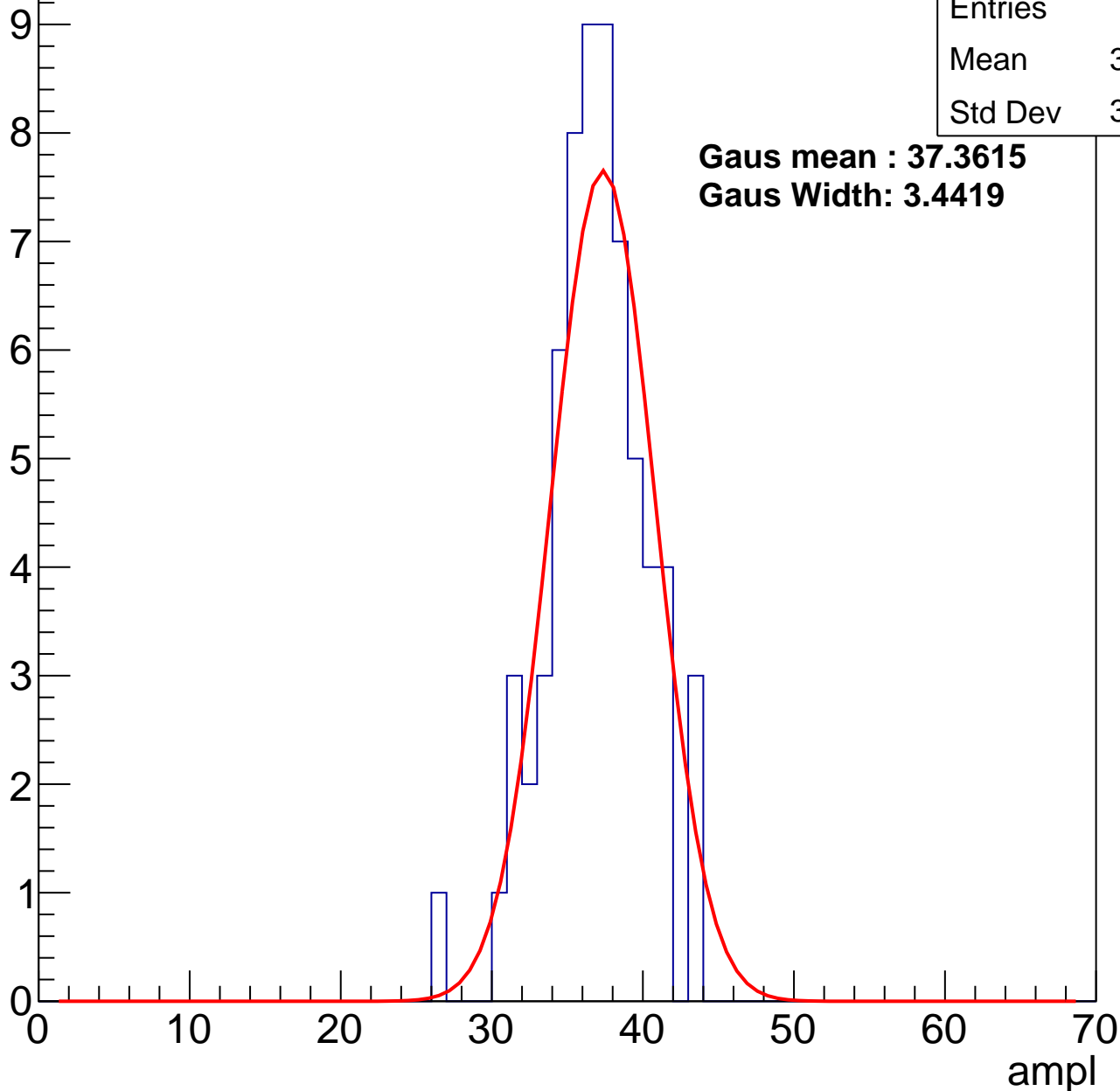
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	36.42
Std Dev	3.243

**Gaus mean : 37.3615**

**Gaus Width: 3.4419**



# B1L101S, U19-ch9, adc2

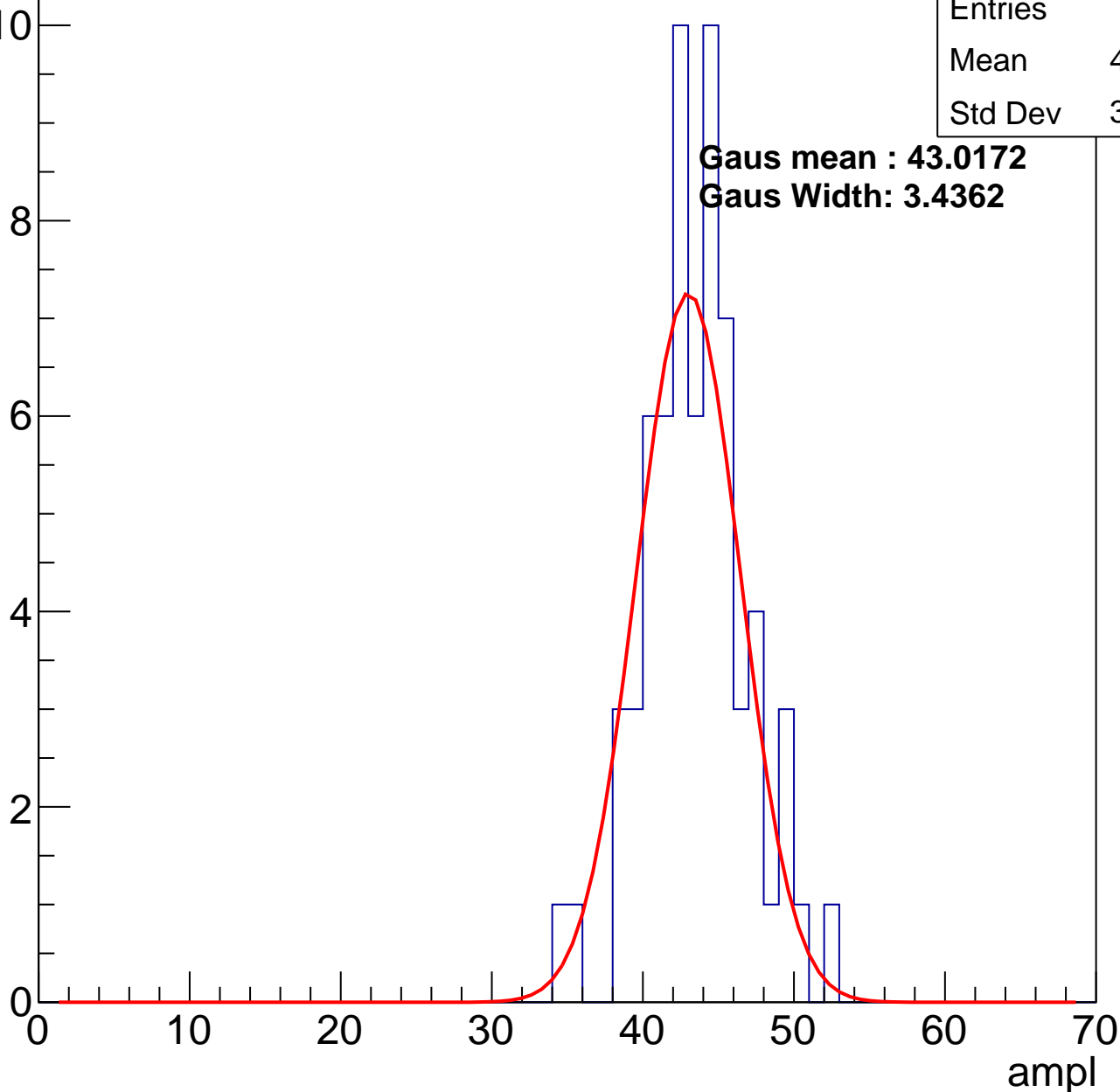
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	66
Mean	43.06
Std Dev	3.366

**Gaus mean : 43.0172**

**Gaus Width: 3.4362**

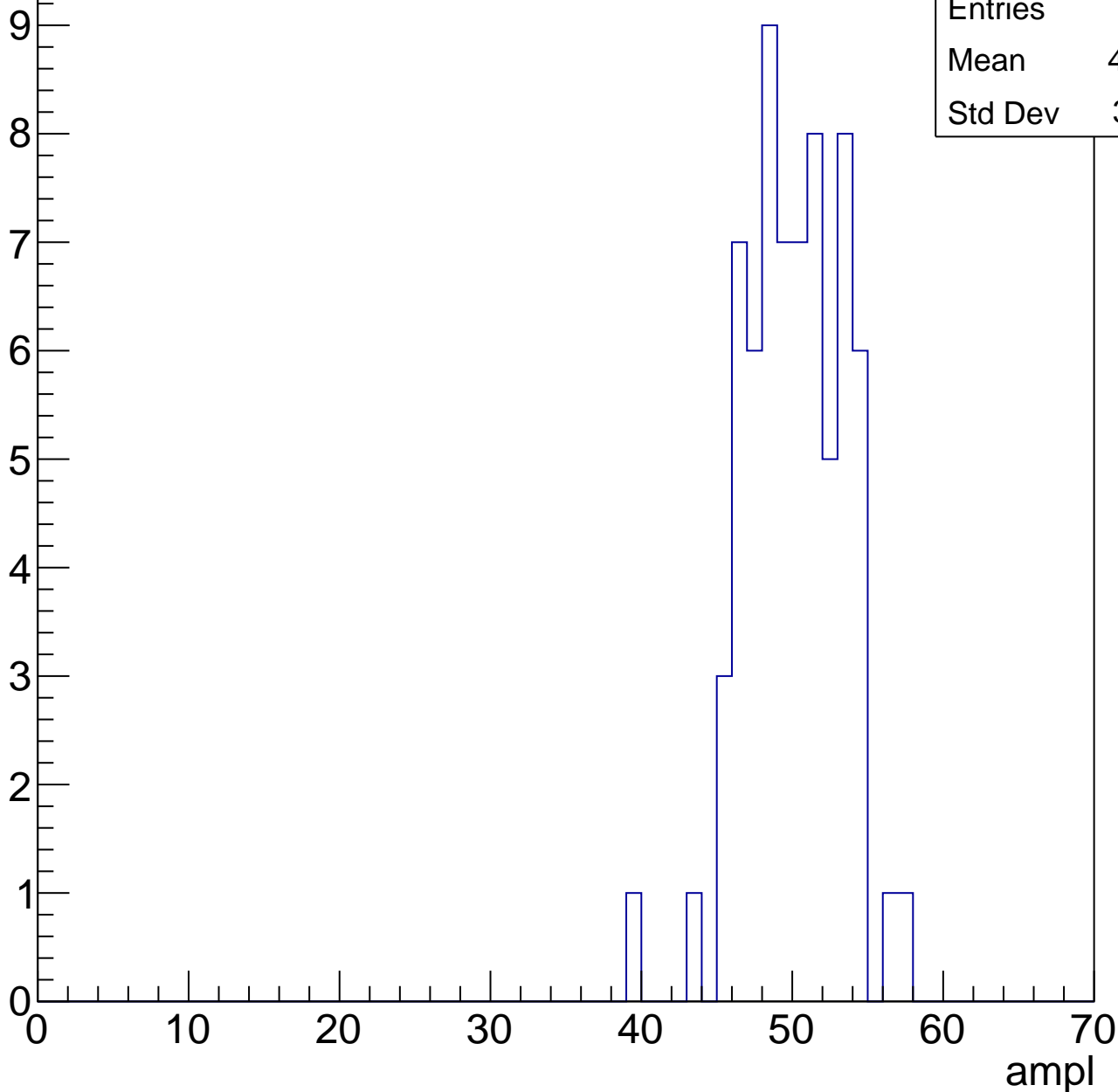


# B1L101S, U19-ch9, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	49.64
Std Dev	3.221

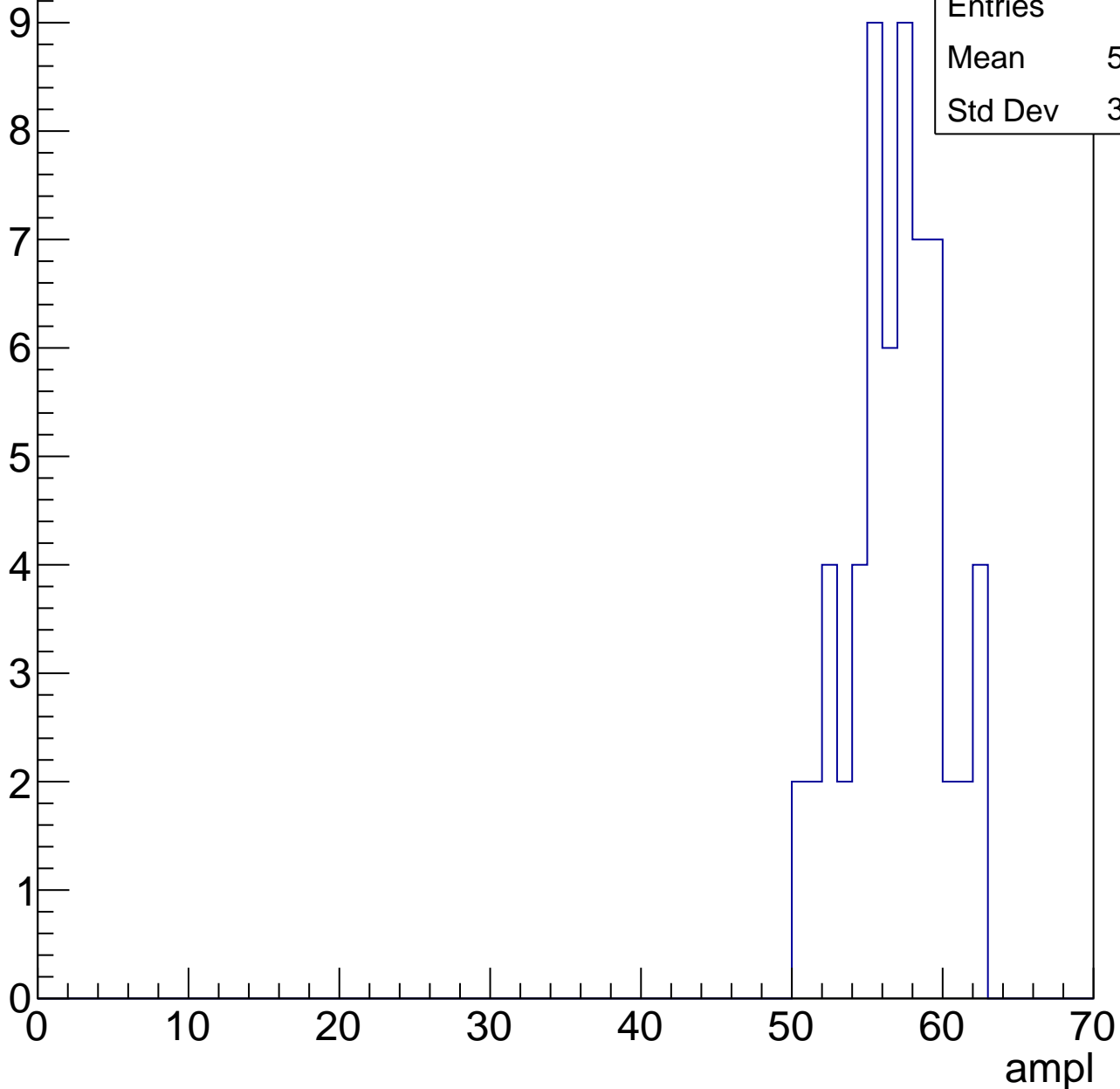


# B1L101S, U19-ch9, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	60
Mean	56.42
Std Dev	3.013

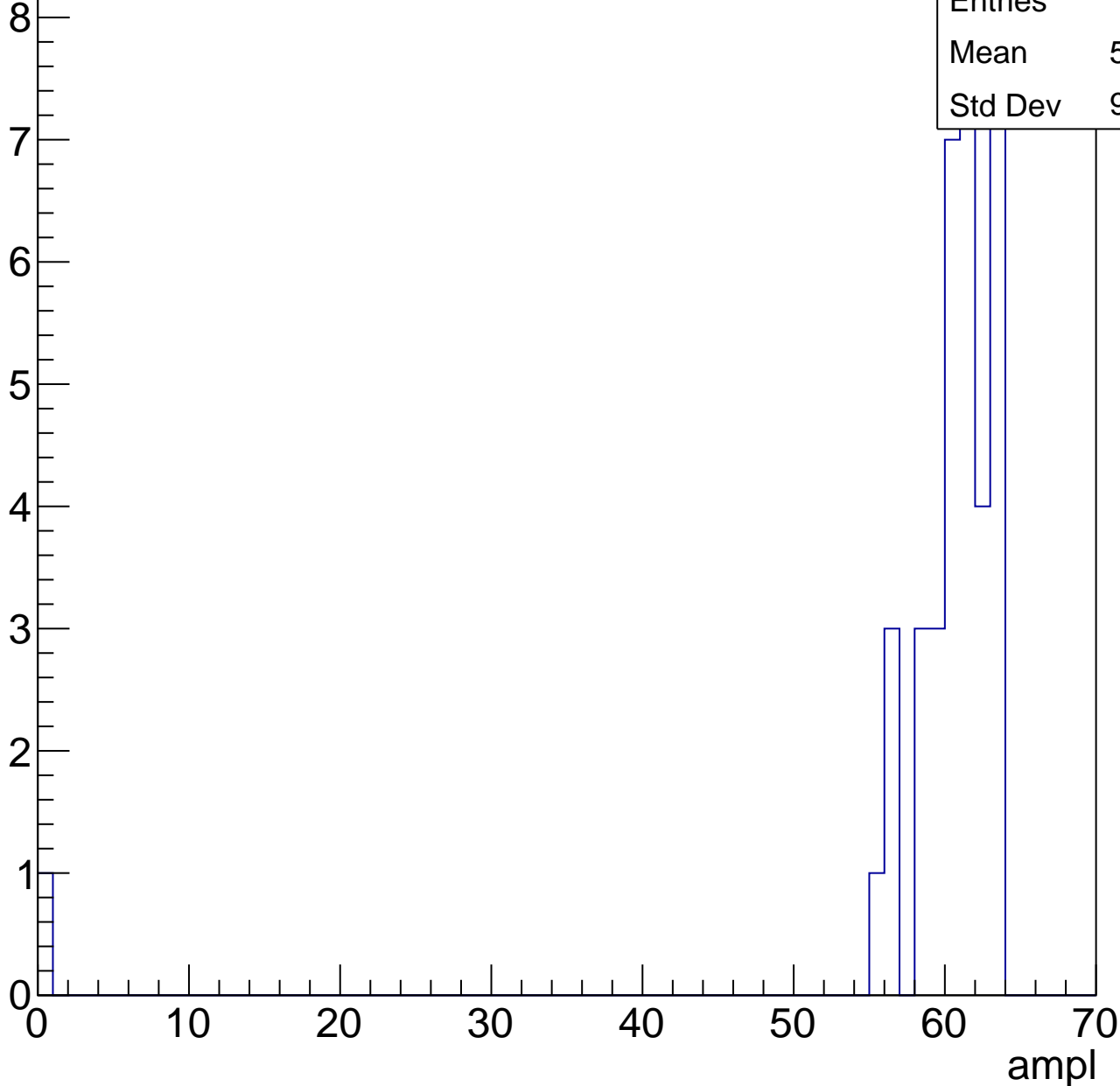


# B1L101S, U19-ch9, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	38
Mean	58.79
Std Dev	9.905



# B1L101S, U19-ch9, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

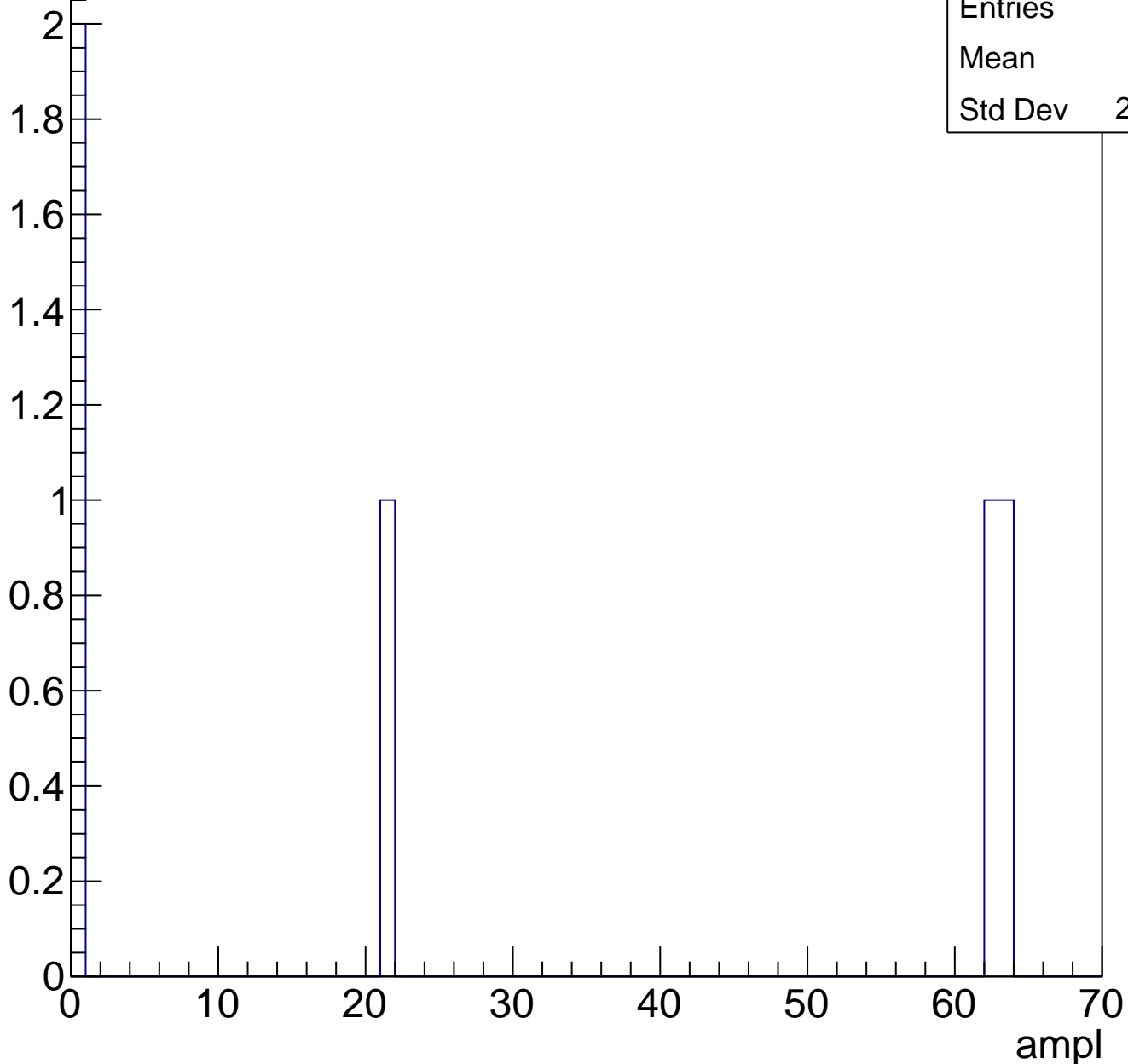




# B1L101S, U19-ch9, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	5
Mean	29.2
Std Dev	28.25

# B1L101S, U19-ch10, adc0

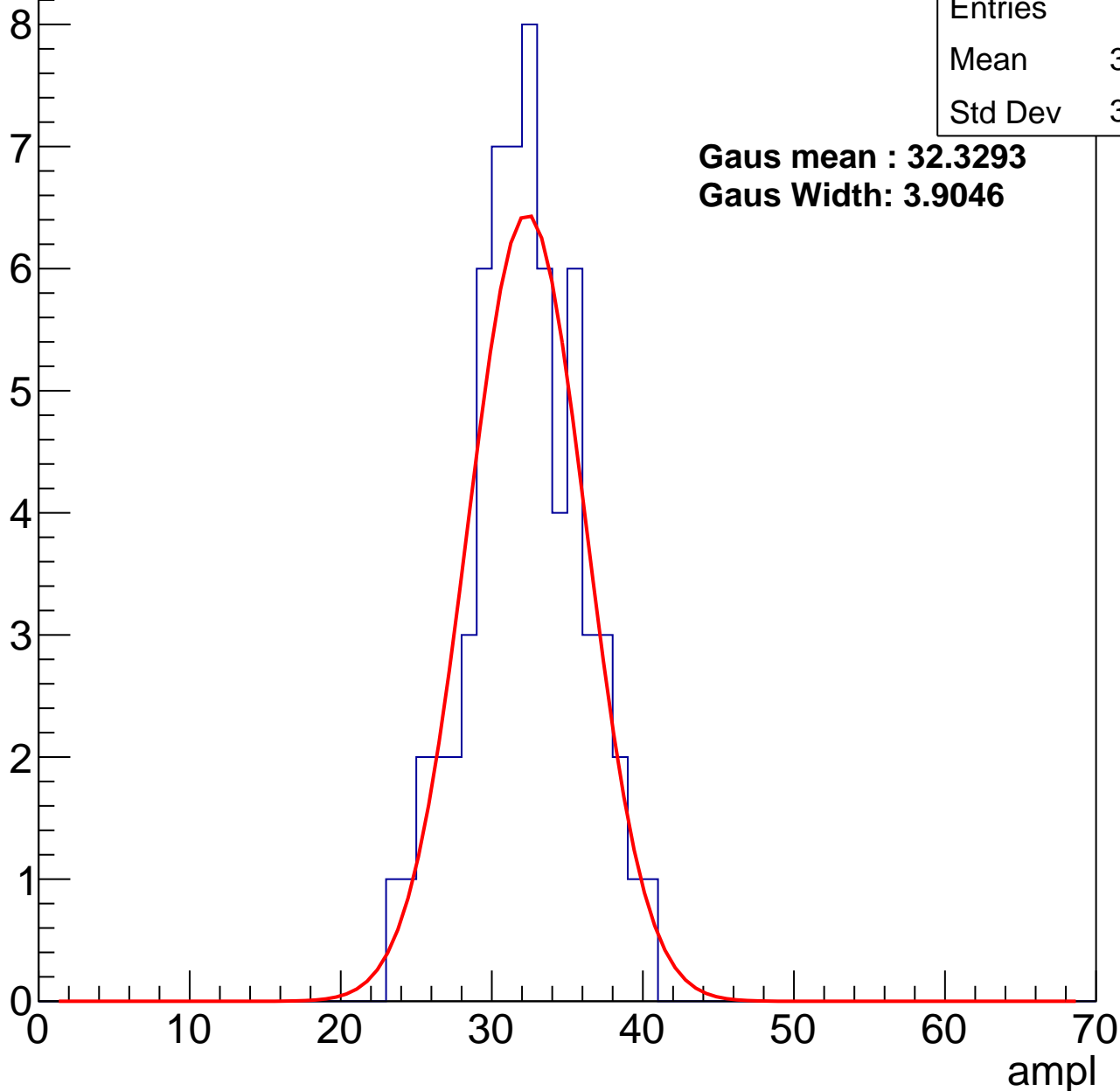
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	31.72
Std Dev	3.682

**Gaus mean : 32.3293**

**Gaus Width: 3.9046**



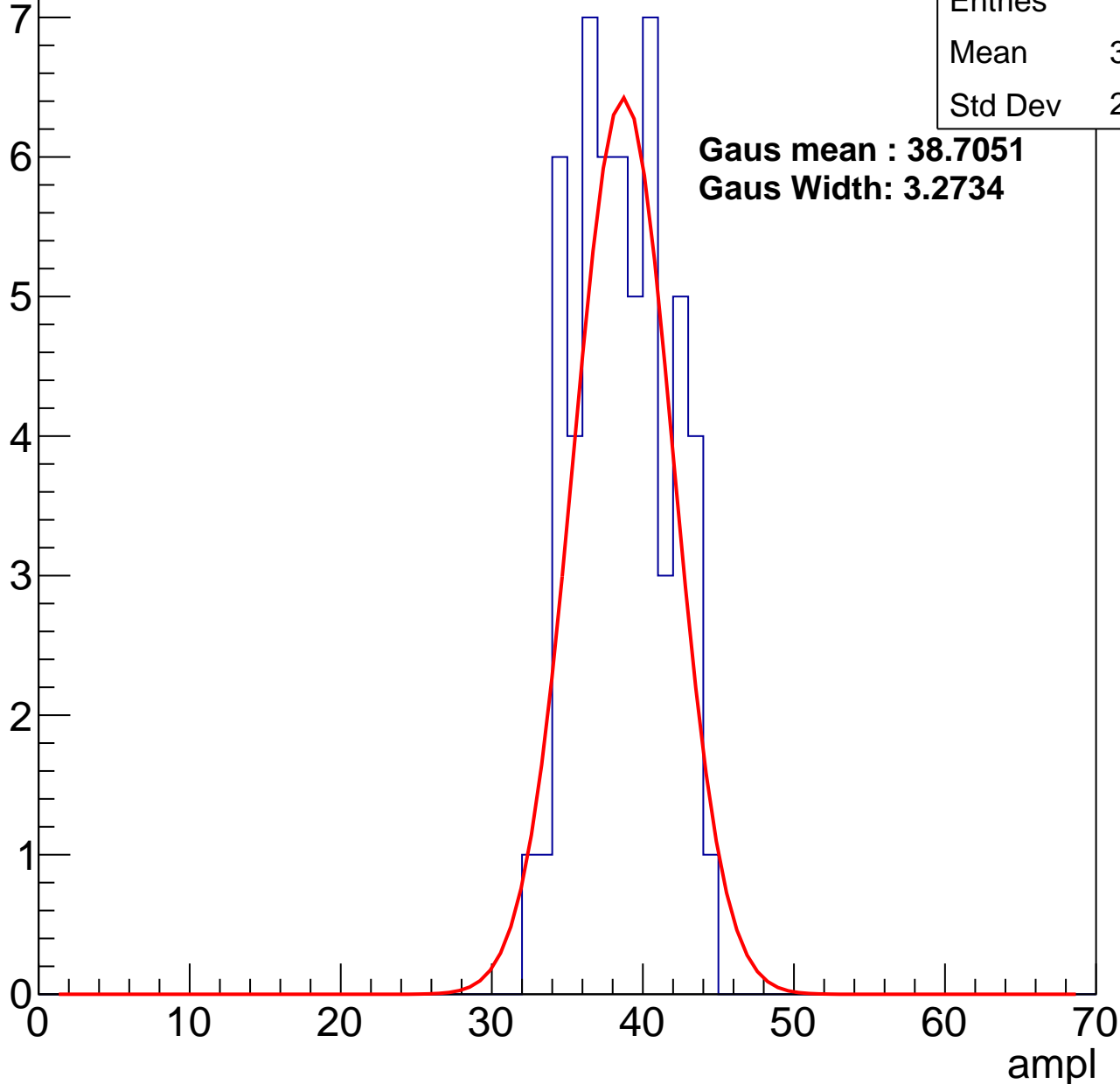
# B1L101S, U19-ch10, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	56
Mean	38.12
Std Dev	2.994

**Gaus mean : 38.7051**  
**Gaus Width: 3.2734**



# B1L101S, U19-ch10, adc2

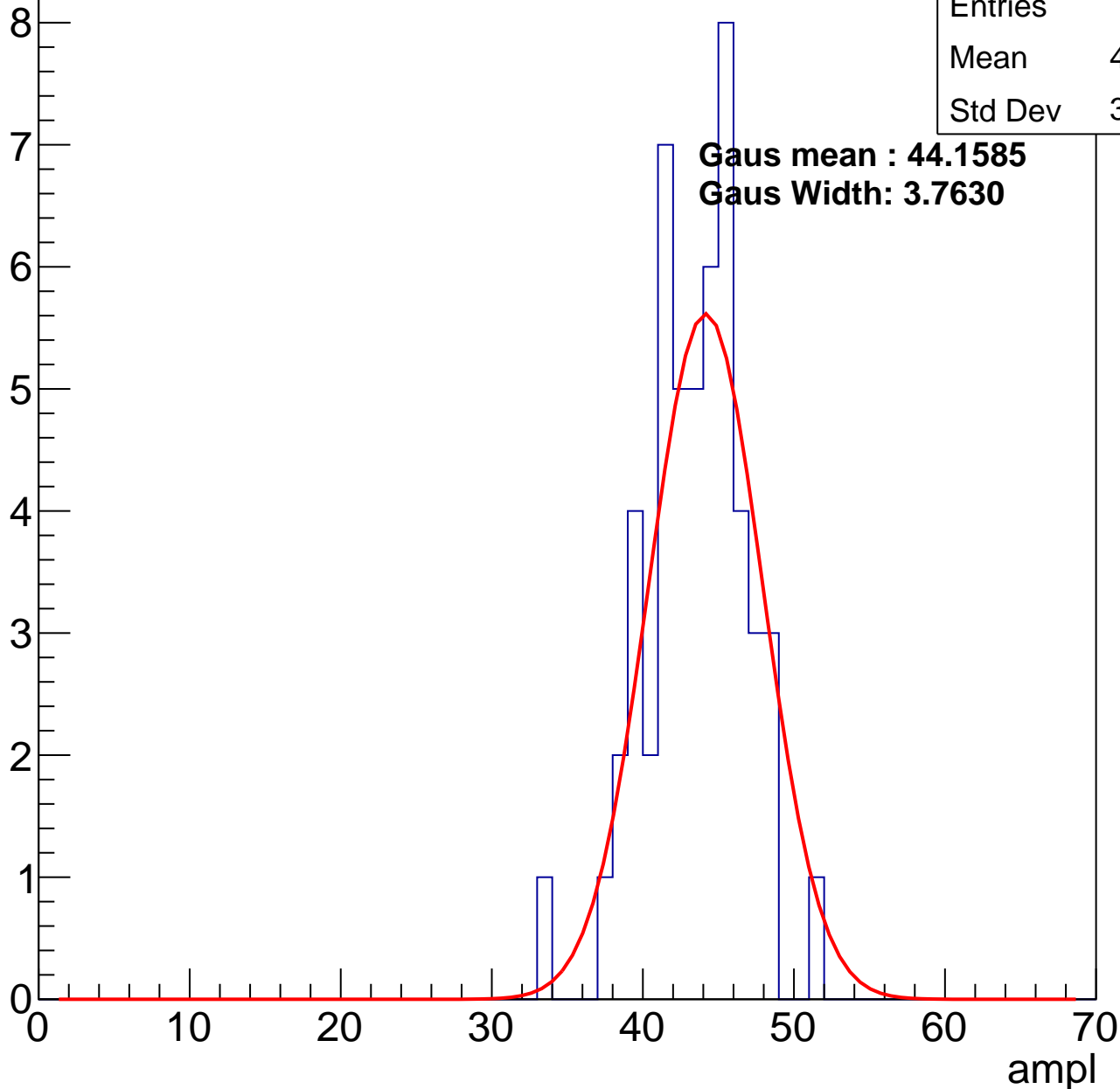
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	52
Mean	43.04
Std Dev	3.287

**Gaus mean : 44.1585**

**Gaus Width: 3.7630**

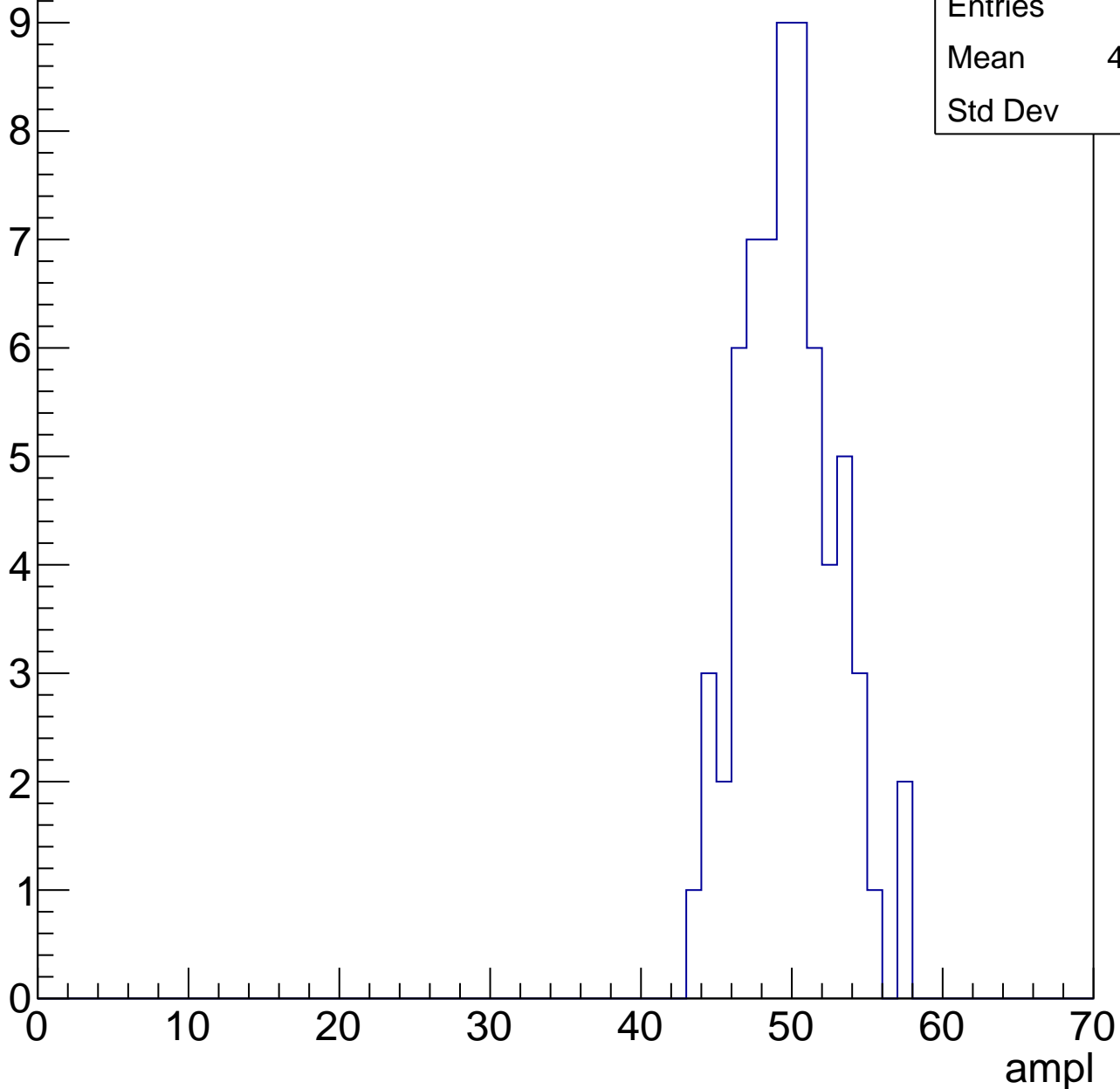


# B1L101S, U19-ch10, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	49.34
Std Dev	3.07

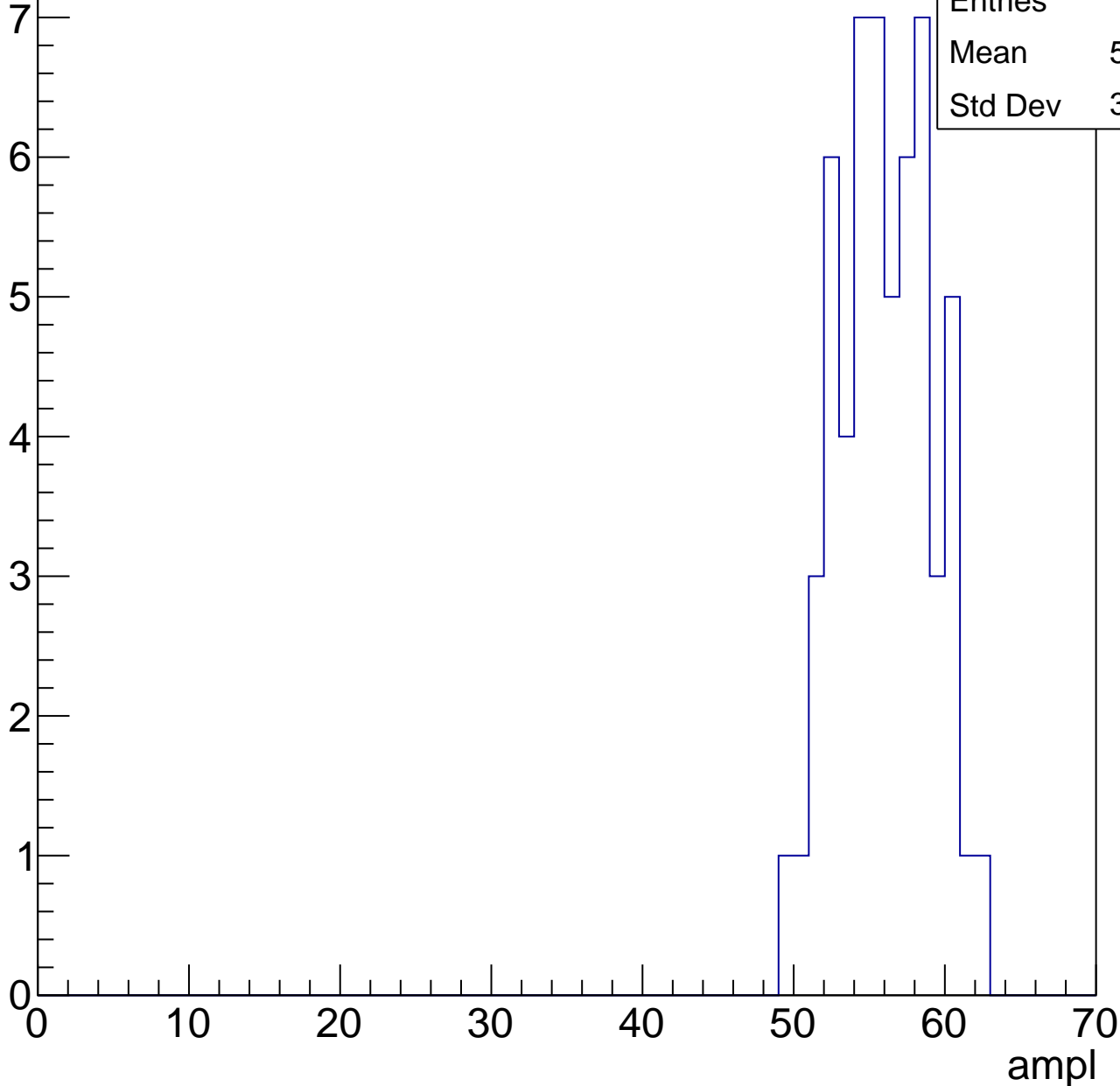


# B1L101S, U19-ch10, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	57
Mean	55.56
Std Dev	3.015



# B1L101S, U19-ch10, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

10

Entries 49

Mean 59.9

Std Dev 2.636

8

6

4

2

0

0

10

20

30

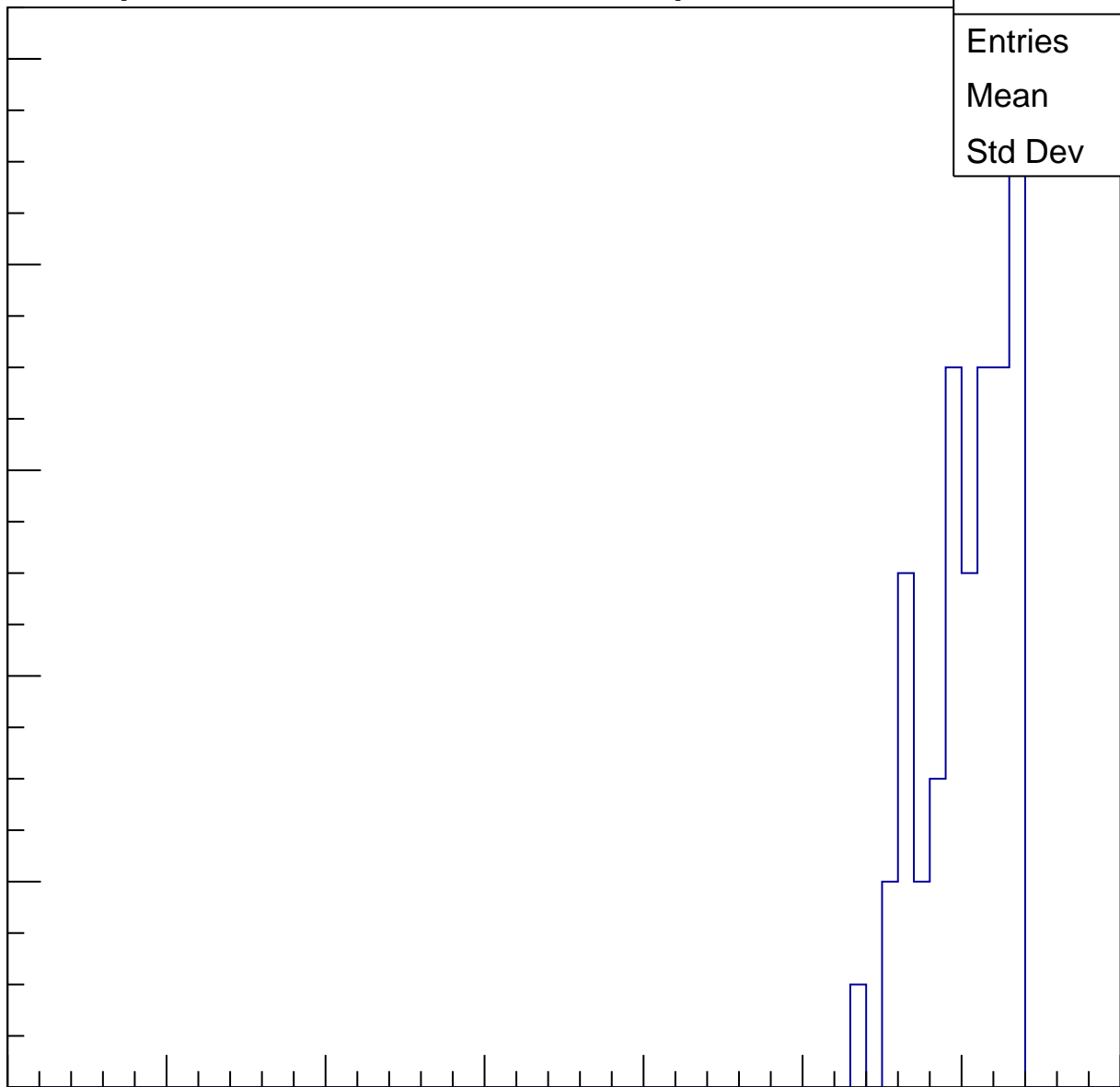
40

50

60

70

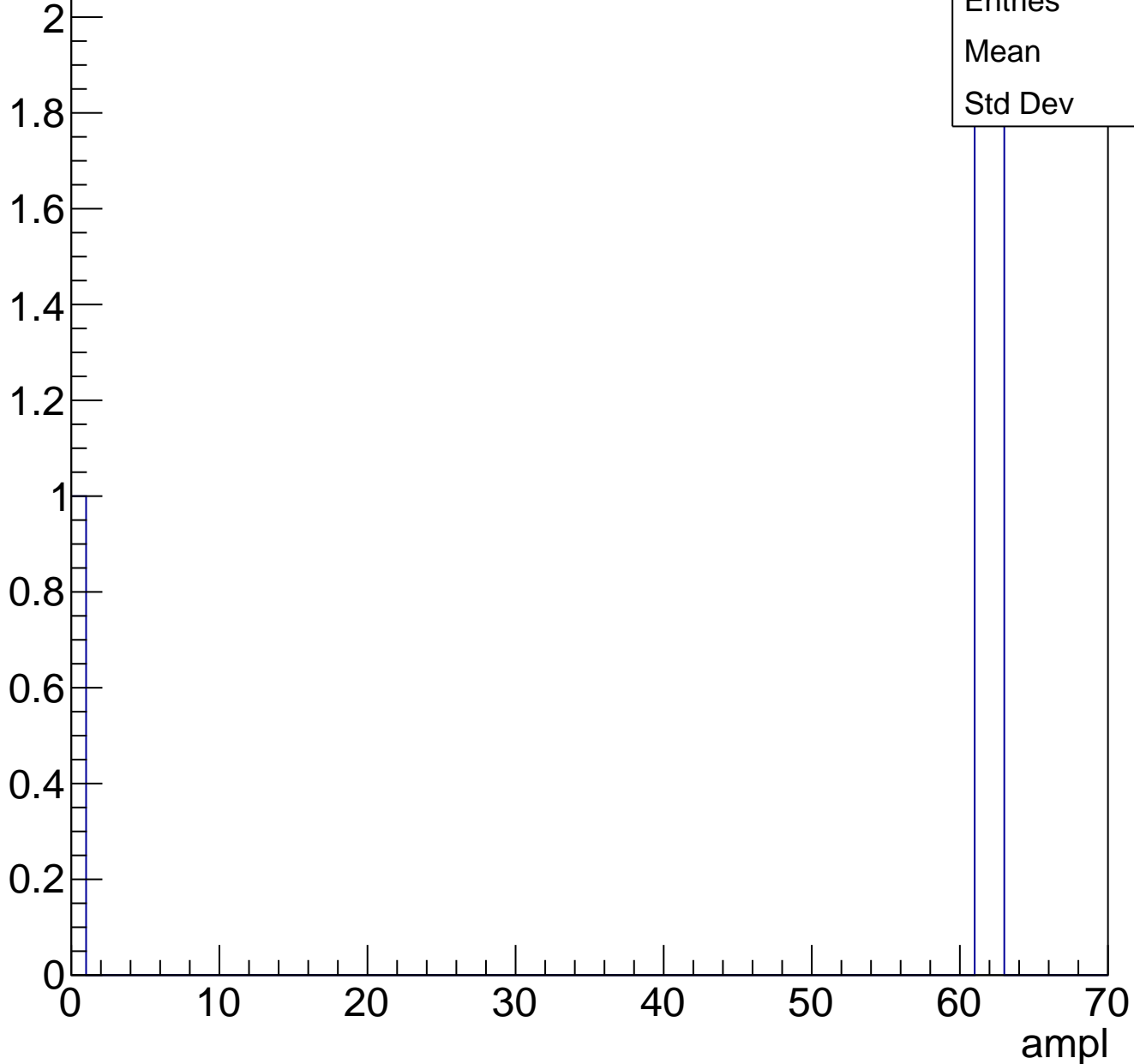
ampl



# B1L101S, U19-ch10, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

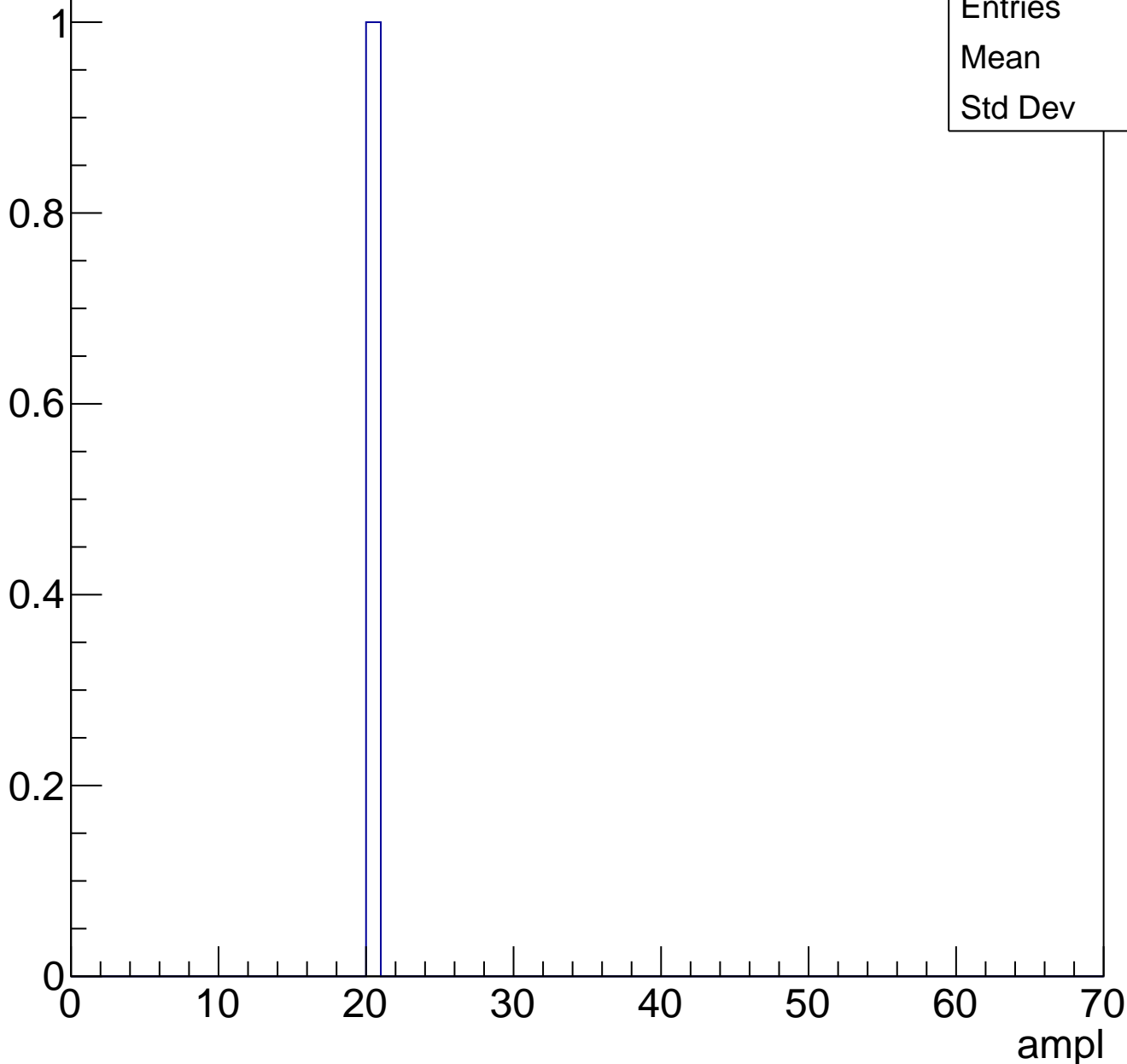




# B1L101S, U19-ch10, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	20
Std Dev	0

# B1L101S, U19-ch11, adc0

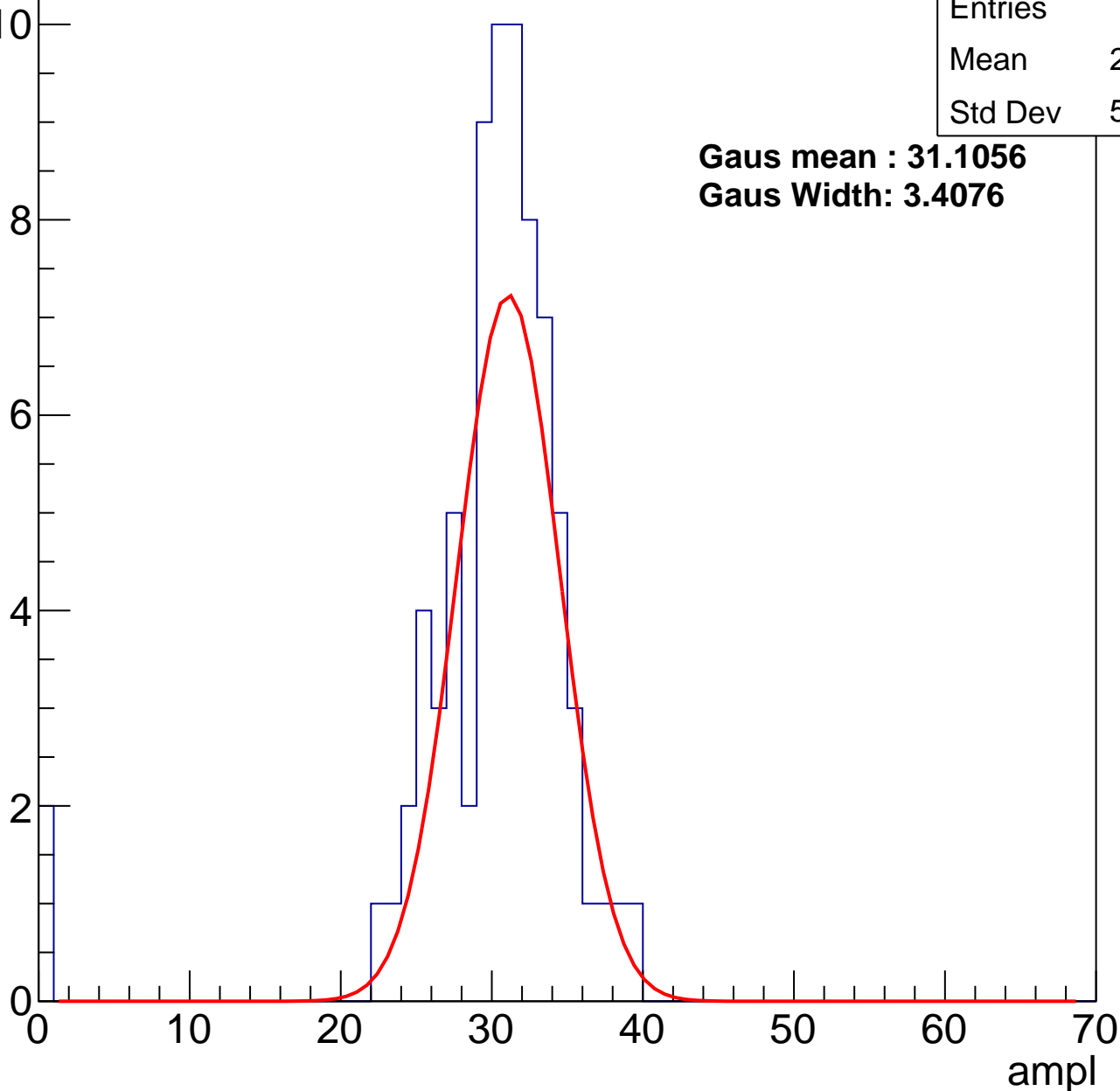
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	76
Mean	29.54
Std Dev	5.926

**Gaus mean : 31.1056**

**Gaus Width: 3.4076**



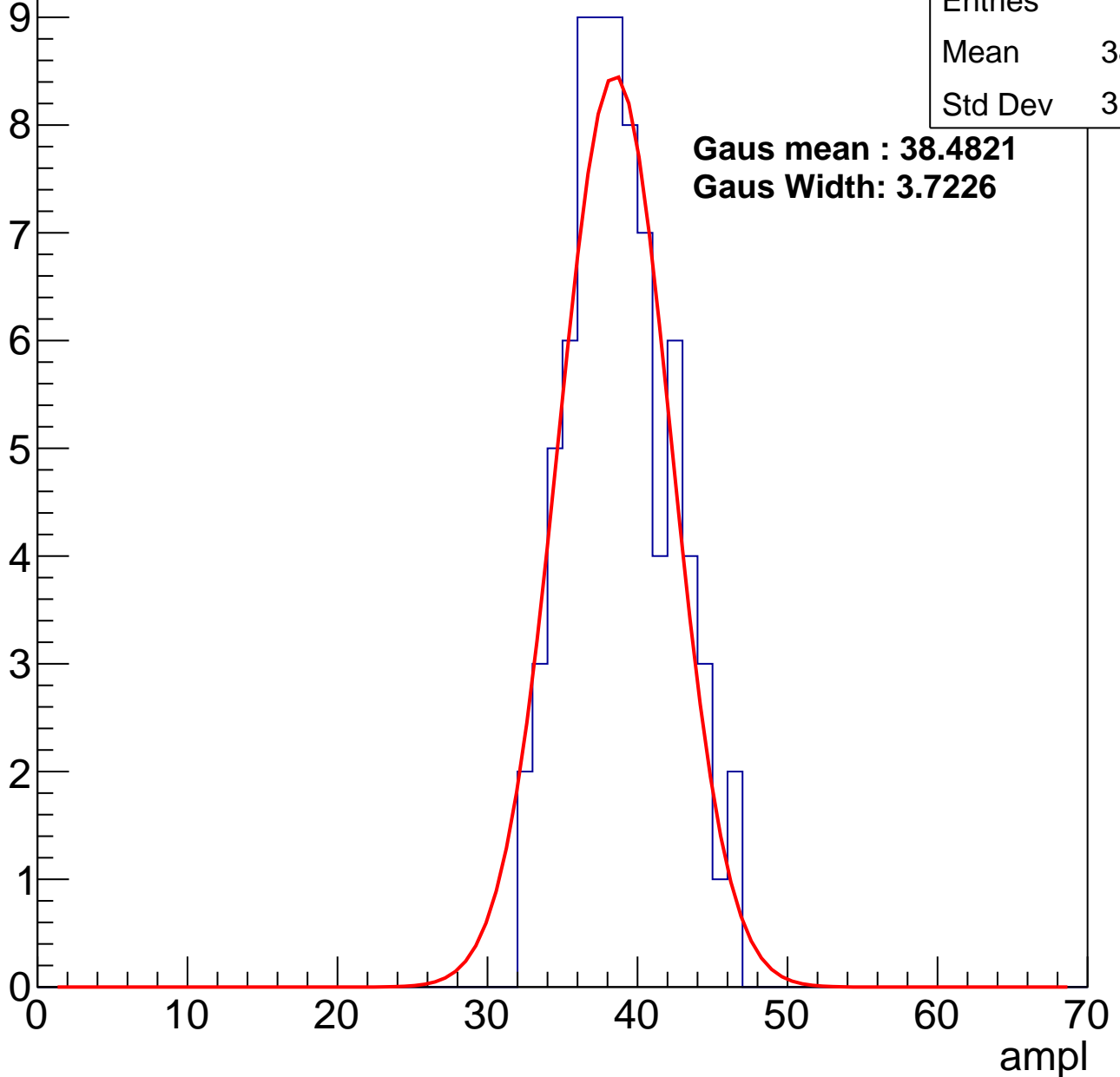
# B1L101S, U19-ch11, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	78
Mean	38.35
Std Dev	3.339

**Gaus mean : 38.4821**  
**Gaus Width: 3.7226**



# B1L101S, U19-ch11, adc2

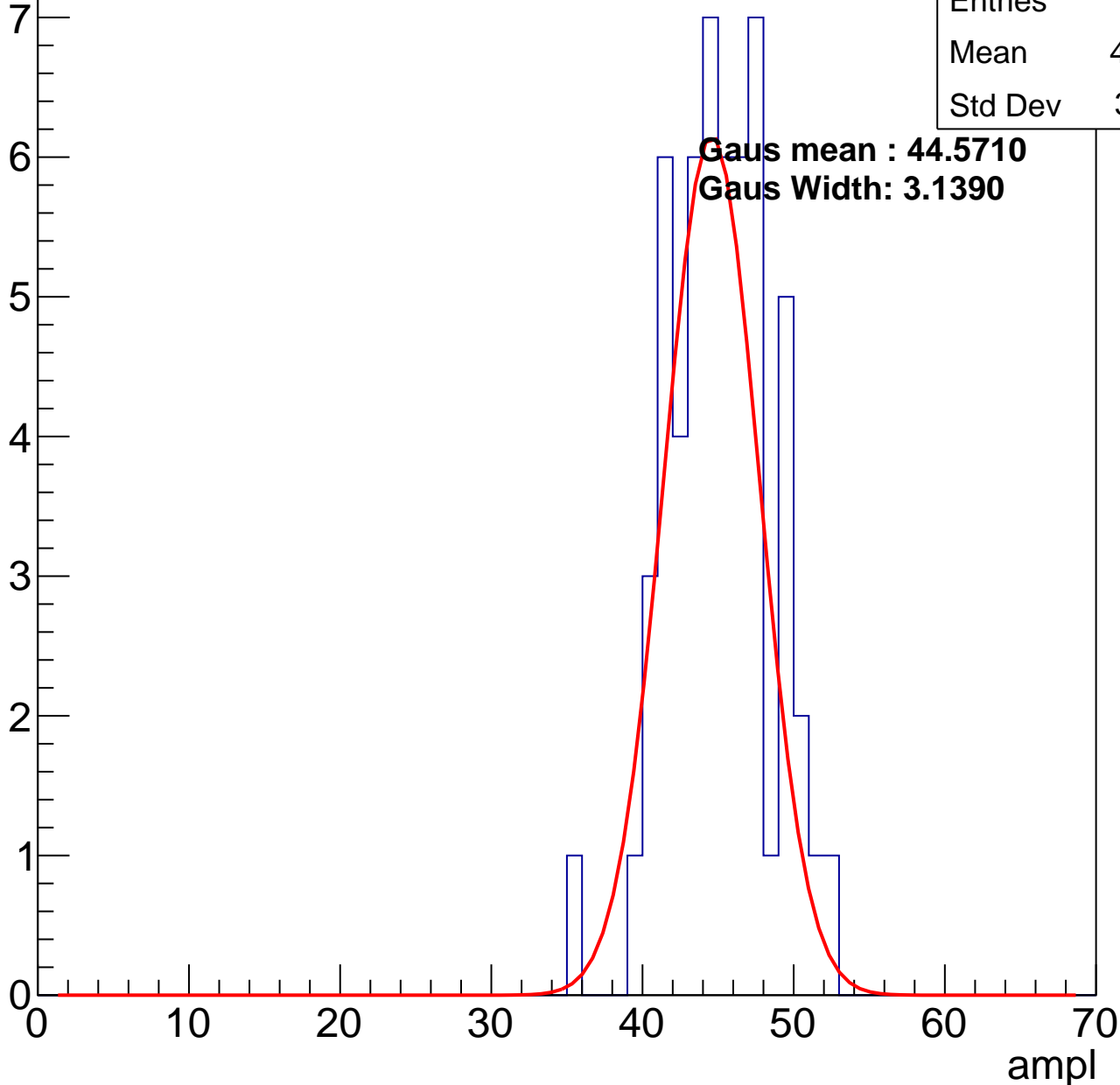
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	57
Mean	44.65
Std Dev	3.311

**Gaus mean : 44.5710**

**Gaus Width: 3.1390**

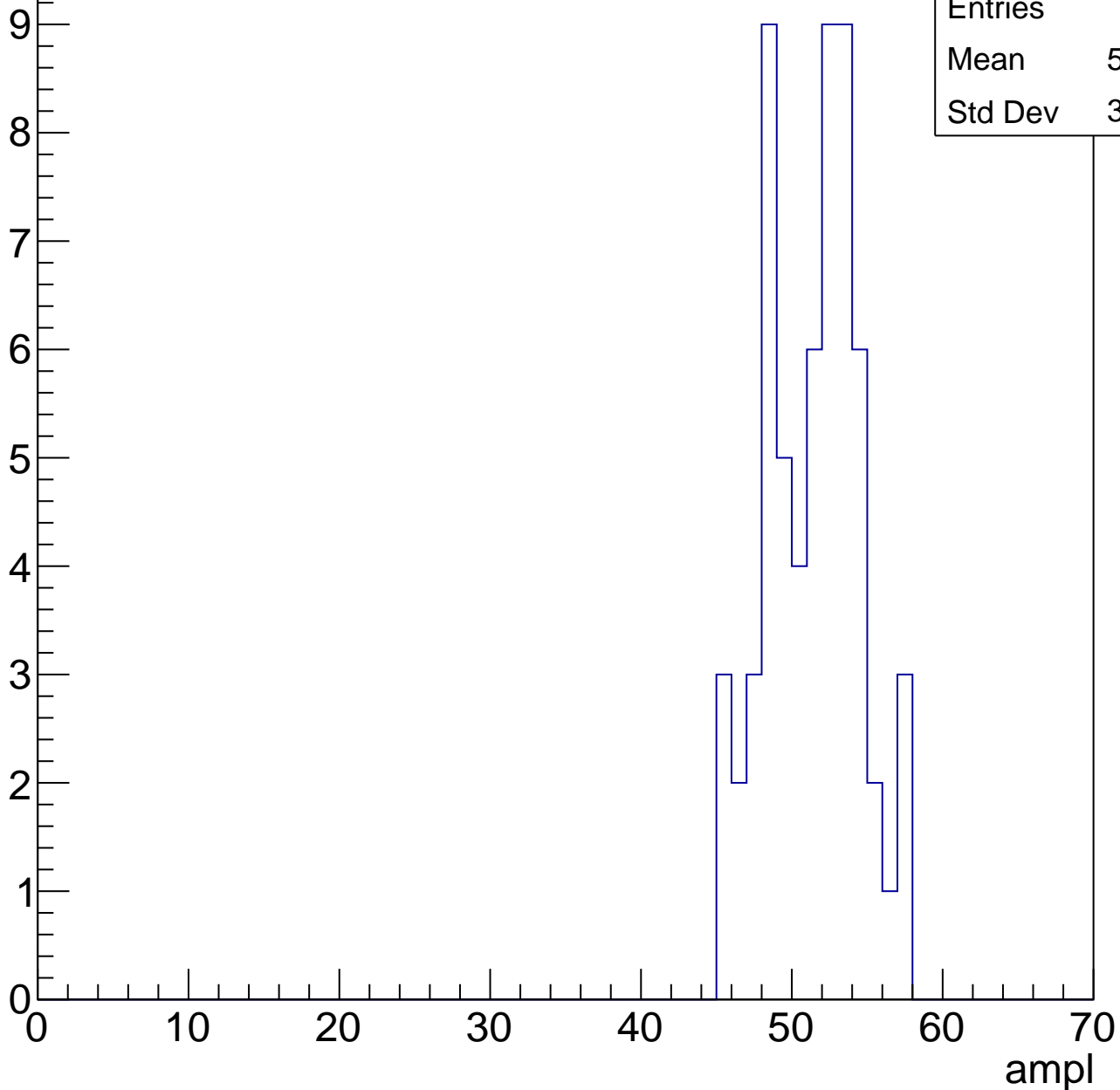


# B1L101S, U19-ch11, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	50.92
Std Dev	3.044

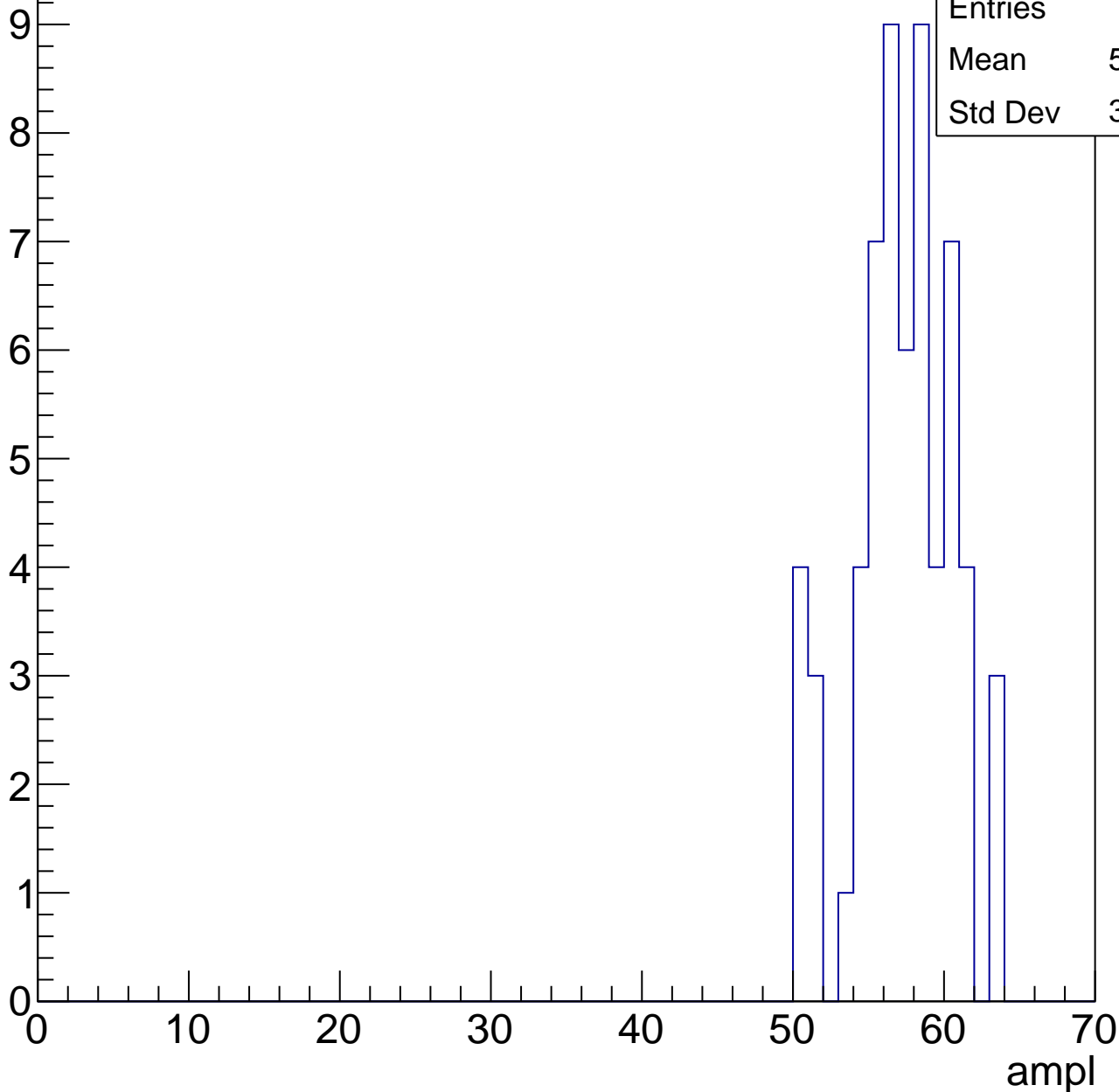


# B1L101S, U19-ch11, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	56.79
Std Dev	3.265

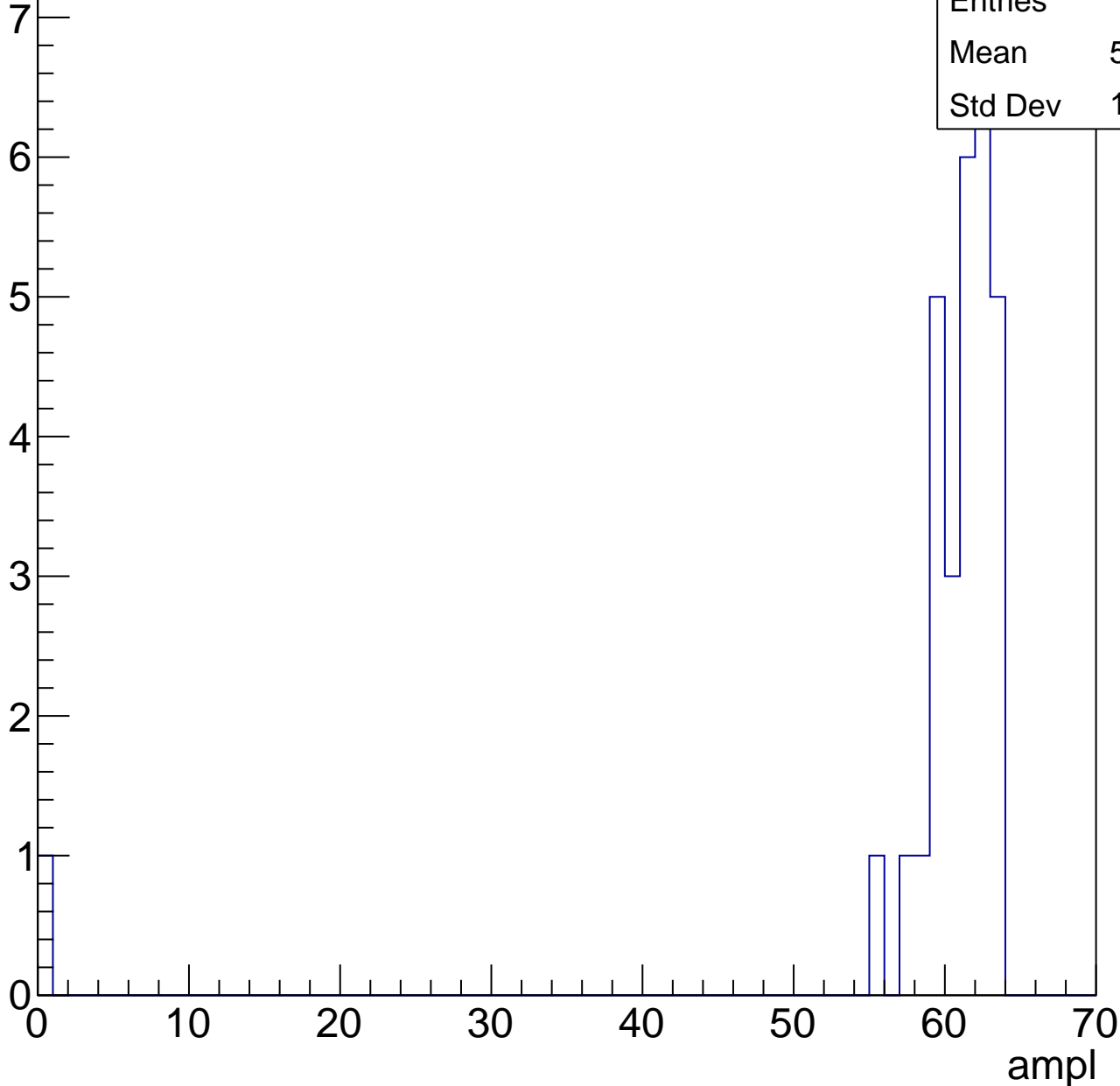


# B1L101S, U19-ch11, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

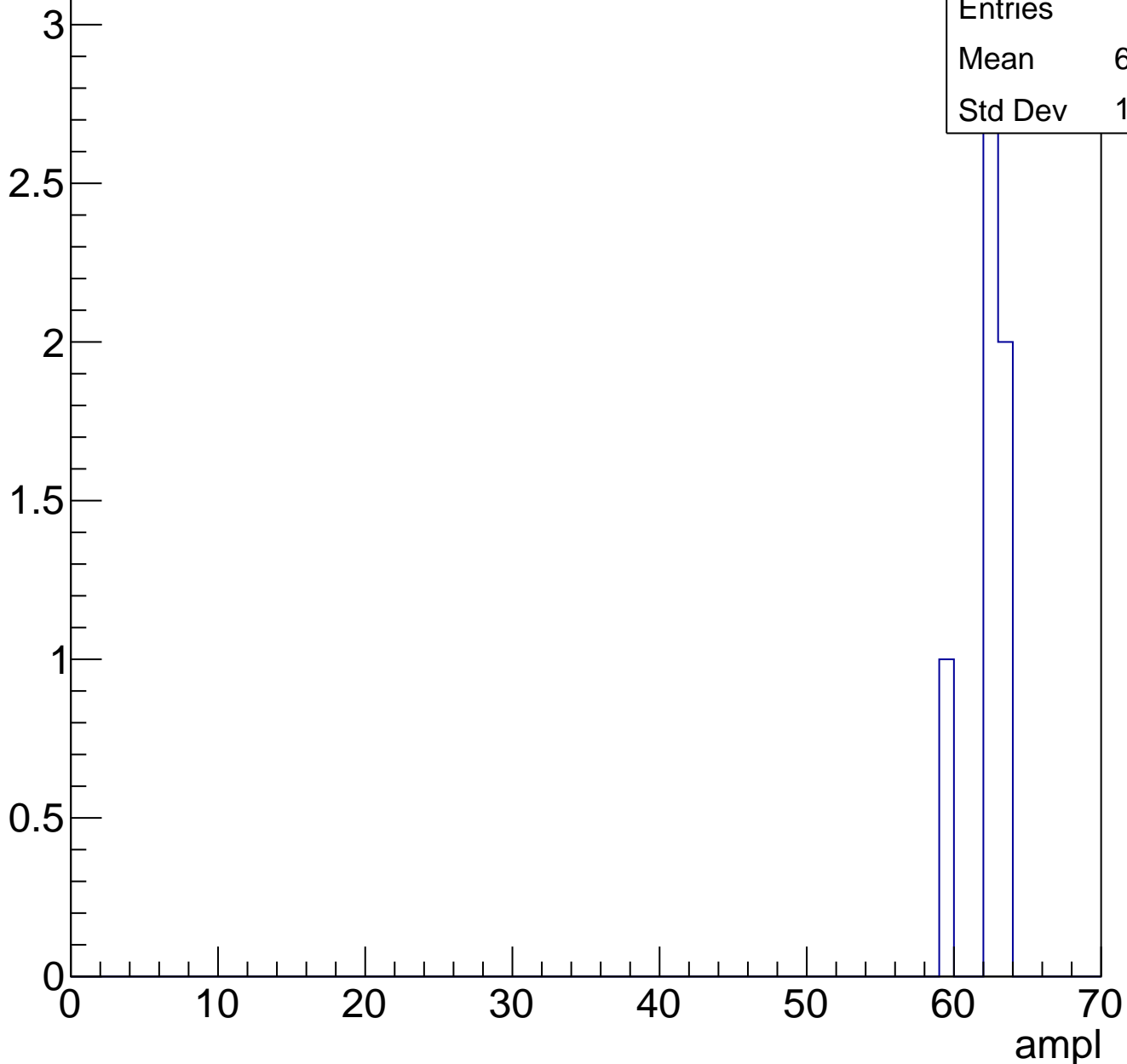
Entries	30
Mean	58.67
Std Dev	11.06



# B1L101S, U19-ch11, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U19-ch11, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U19-ch12, adc0

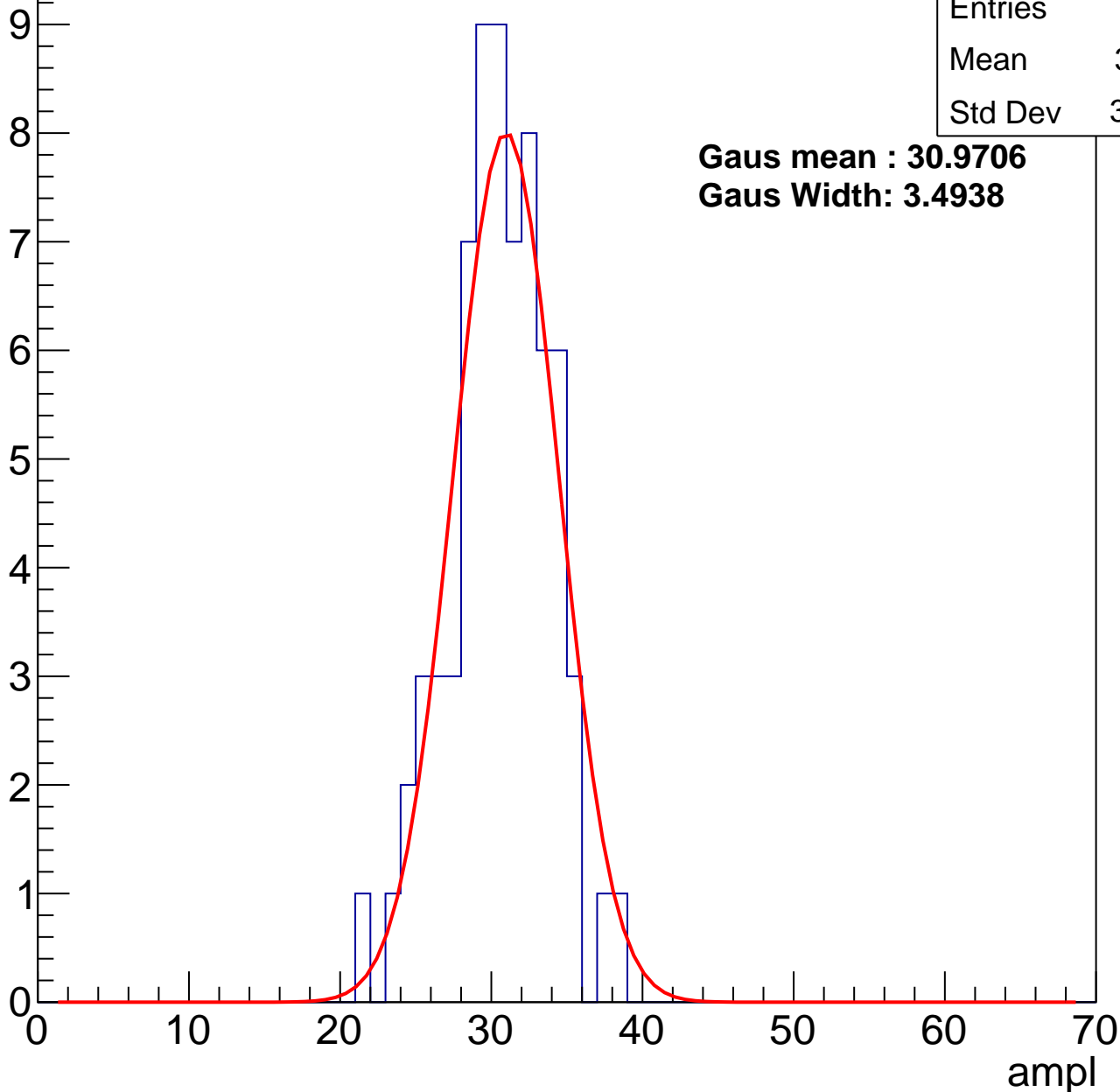
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	30.11
Std Dev	3.306

**Gaus mean : 30.9706**

**Gaus Width: 3.4938**



# B1L101S, U19-ch12, adc1

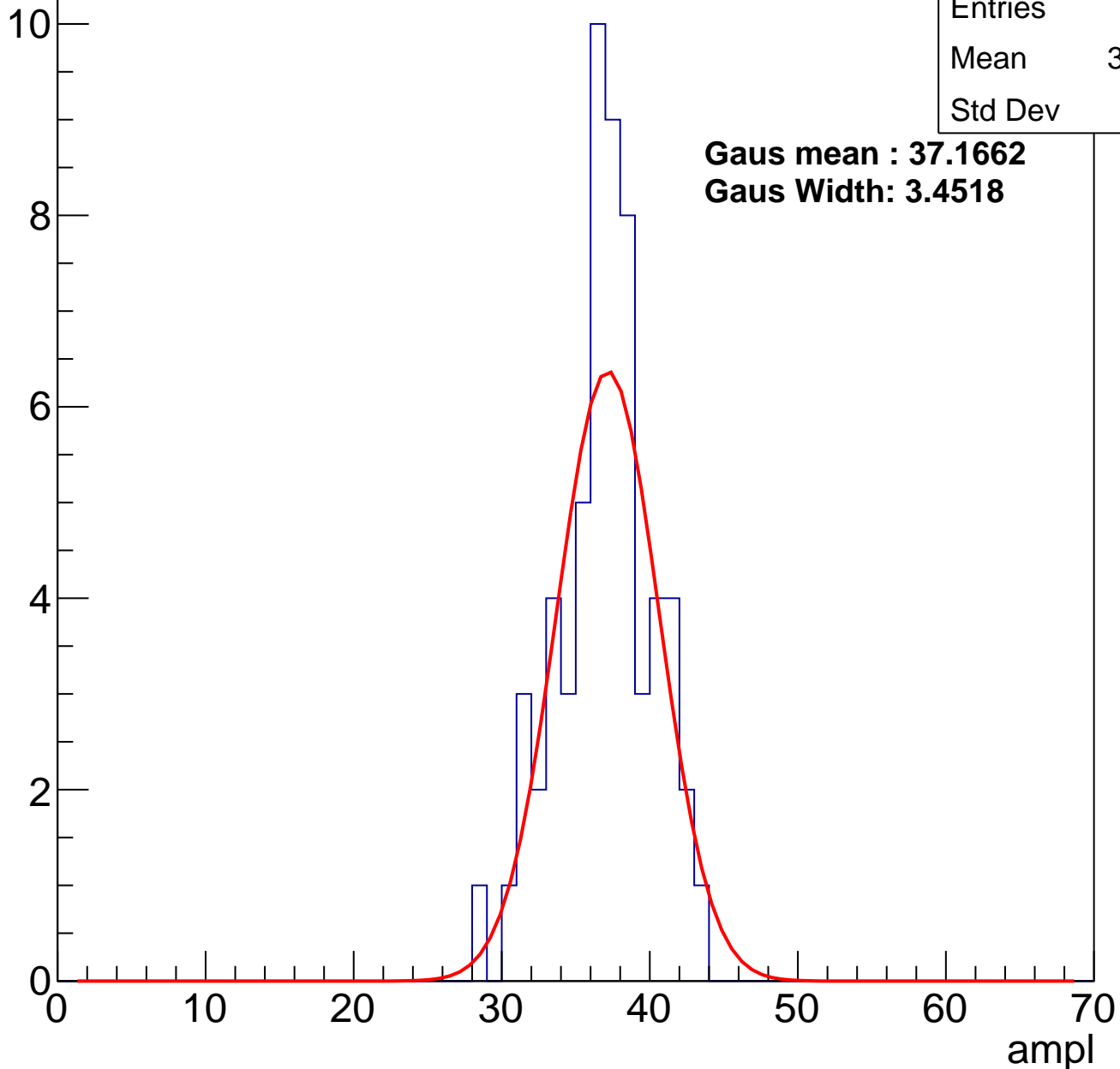
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	60
Mean	36.48
Std Dev	3.16

**Gaus mean : 37.1662**

**Gaus Width: 3.4518**

Entry



# B1L101S, U19-ch12, adc2

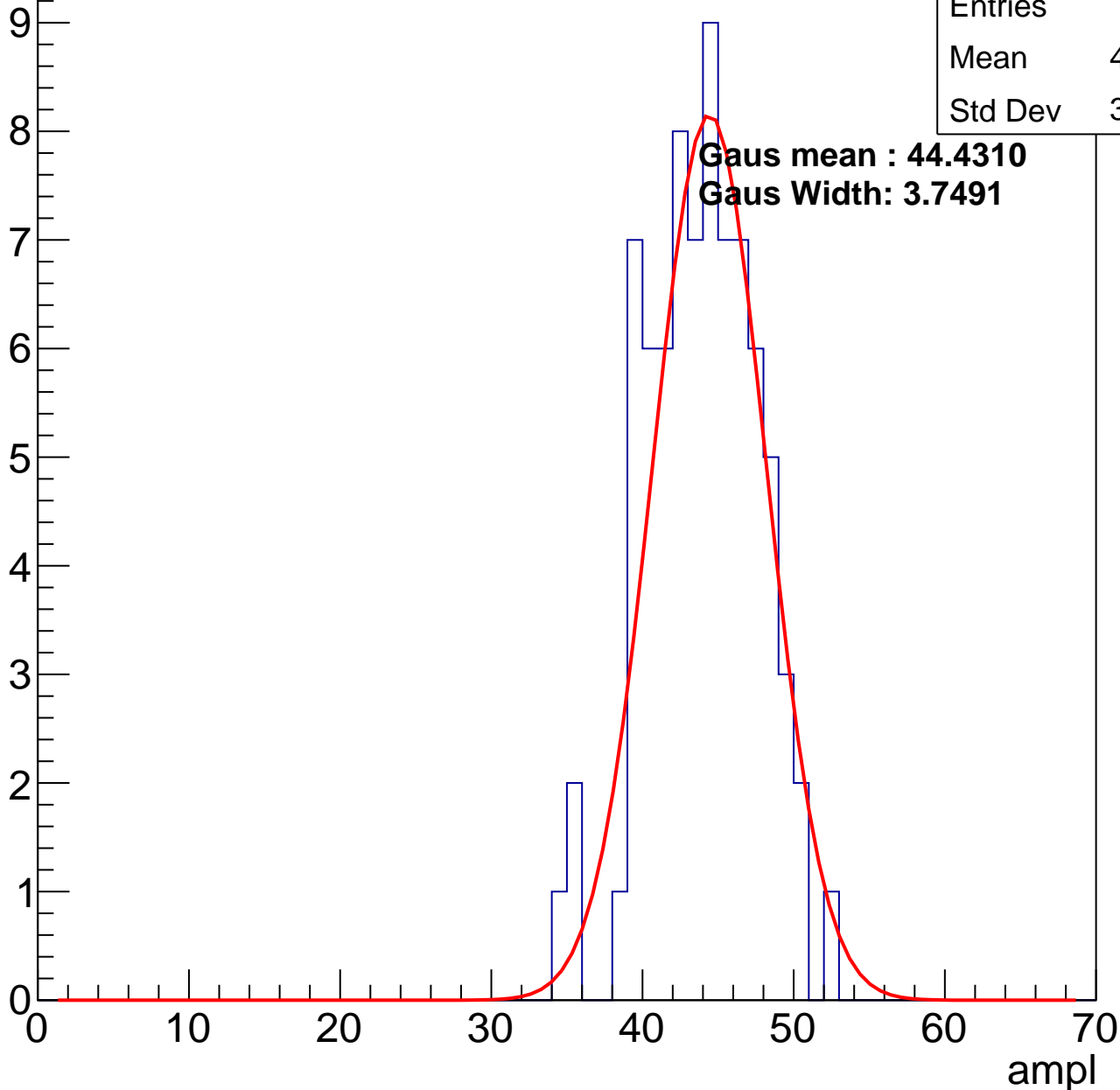
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	78
Mean	43.49
Std Dev	3.619

**Gaus mean : 44.4310**

**Gaus Width: 3.7491**

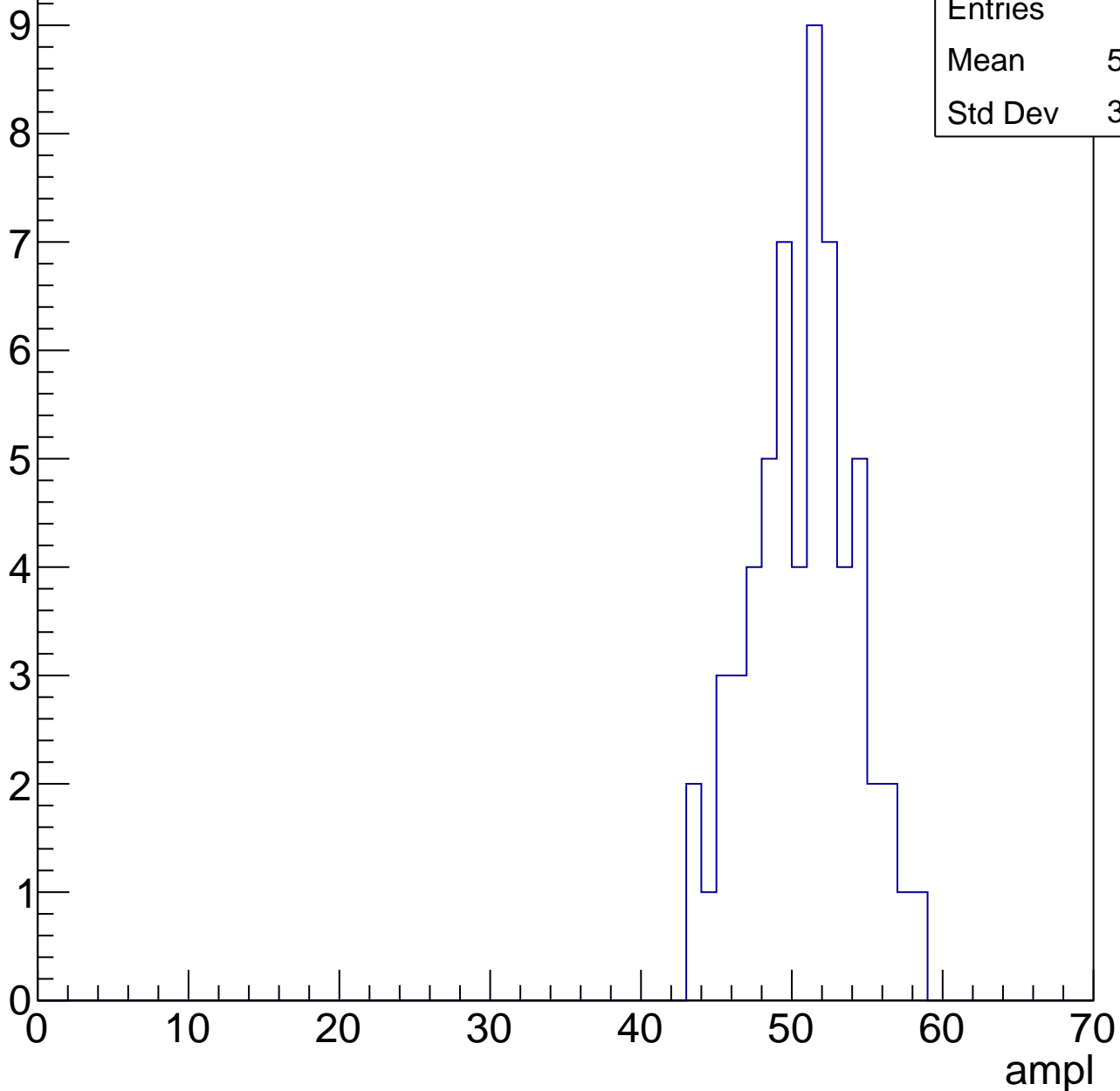


# B1L101S, U19-ch12, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	60
Mean	50.27
Std Dev	3.425

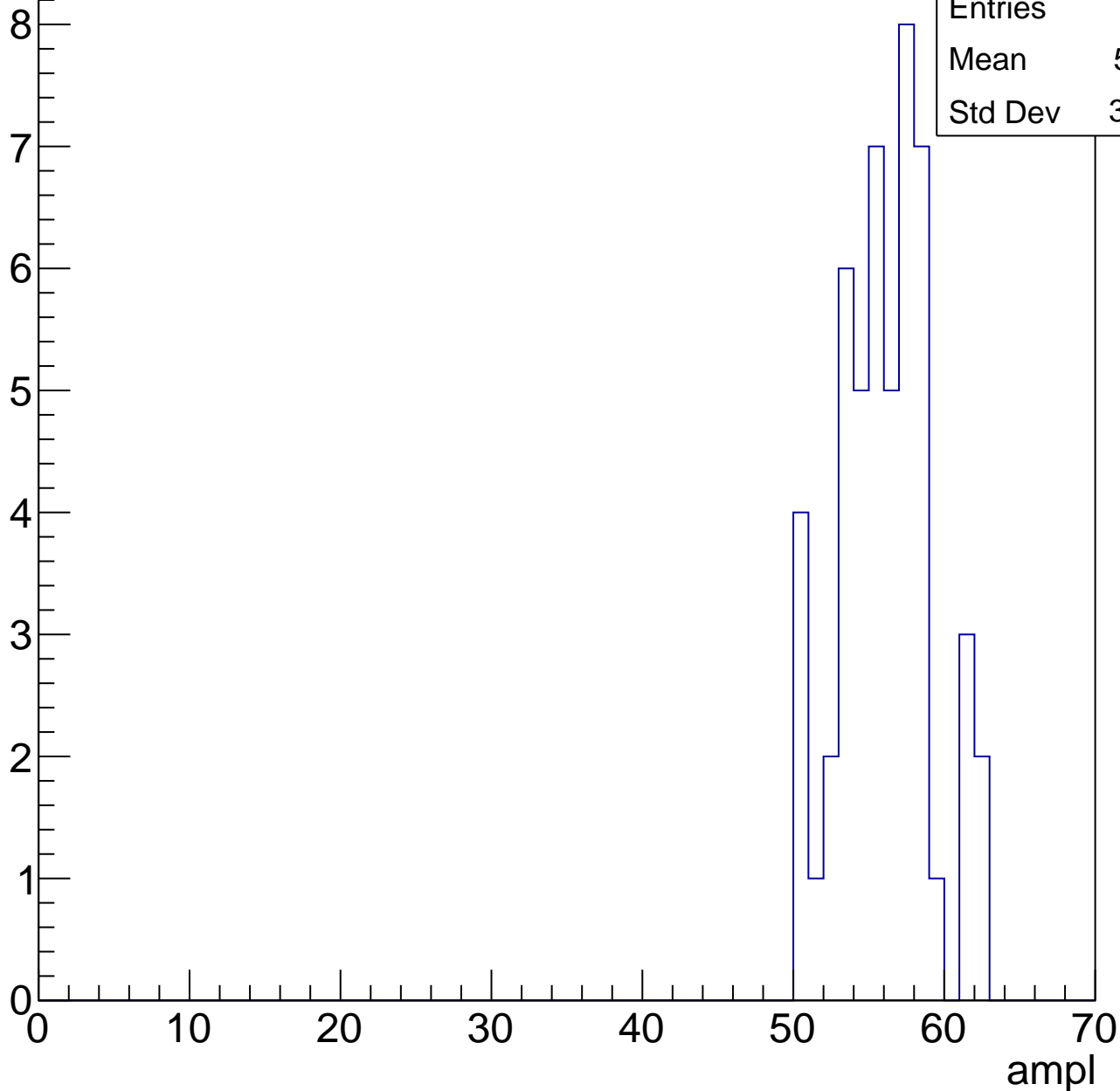


# B1L101S, U19-ch12, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	51
Mean	55.61
Std Dev	3.023



# B1L101S, U19-ch12, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

10

8

6

4

2

0

0

10

20

30

40

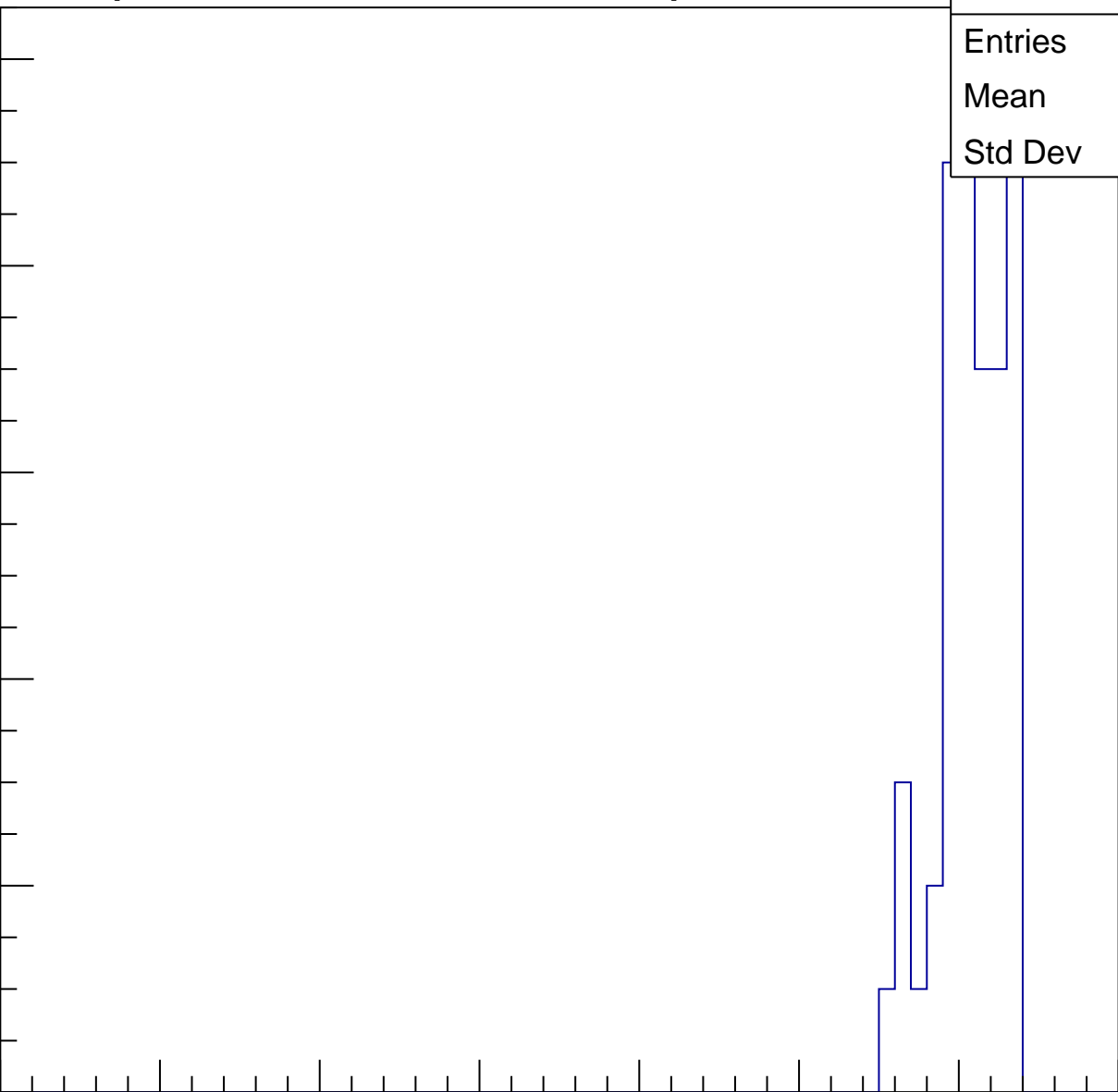
50

60

70

ampl

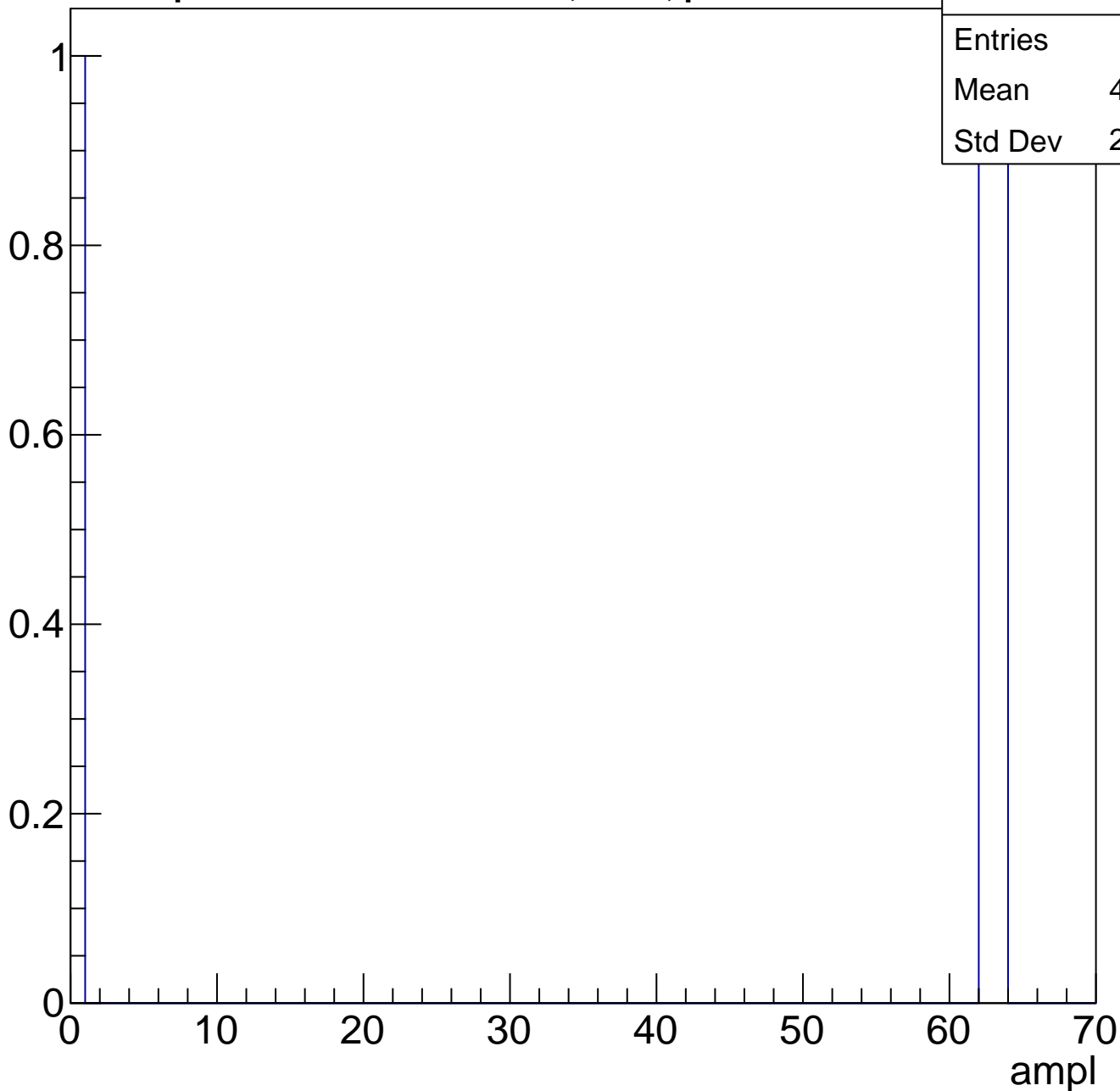
Entries	49
Mean	60.31
Std Dev	2.072



# B1L101S, U19-ch12, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U19-ch12, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U19-ch13, adc0

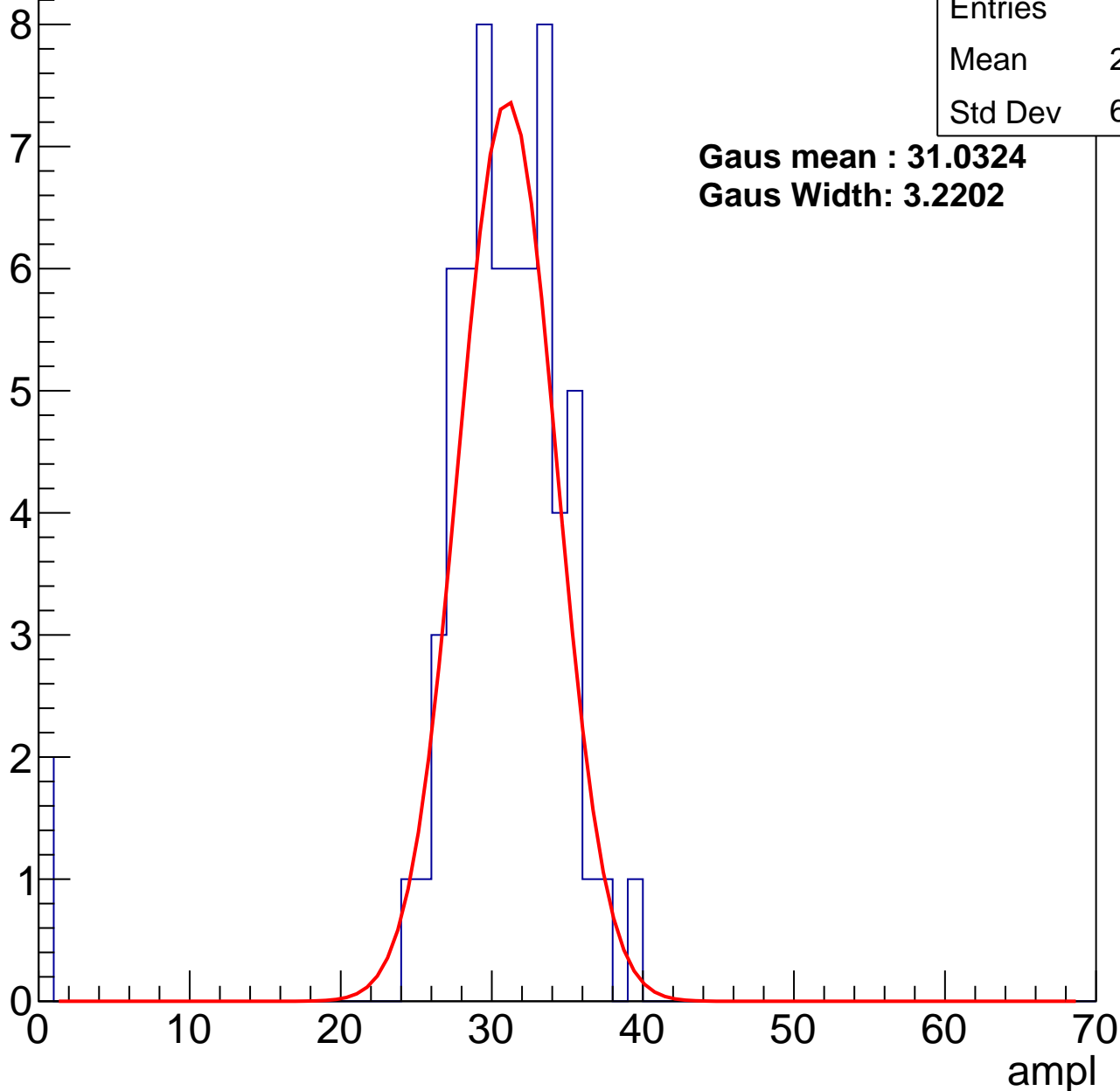
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	29.75
Std Dev	6.137

**Gaus mean : 31.0324**

**Gaus Width: 3.2202**



# B1L101S, U19-ch13, adc1

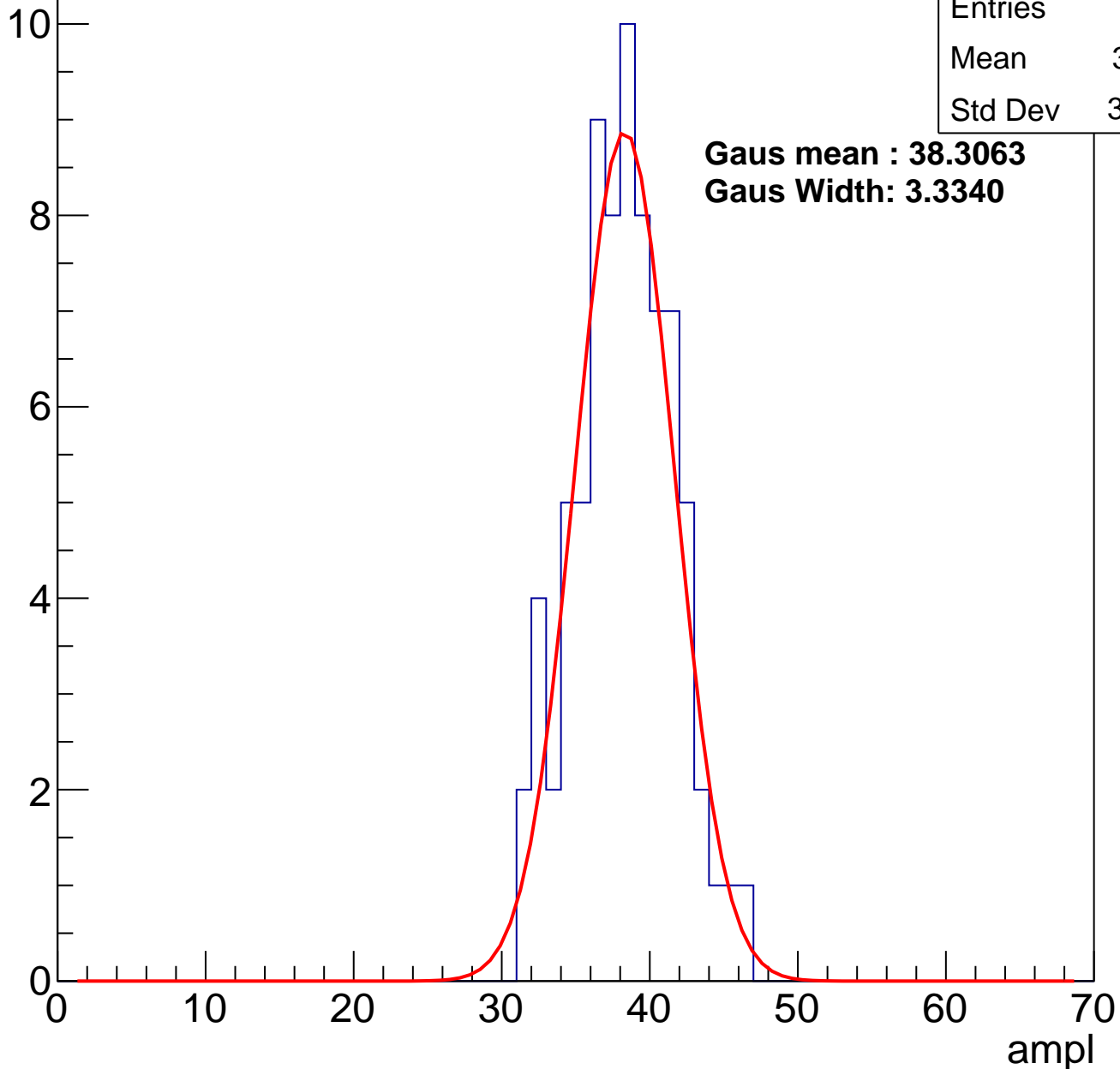
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	77
Mean	37.81
Std Dev	3.295

**Gaus mean : 38.3063**

**Gaus Width: 3.3340**

Entry



# B1L101S, U19-ch13, adc2

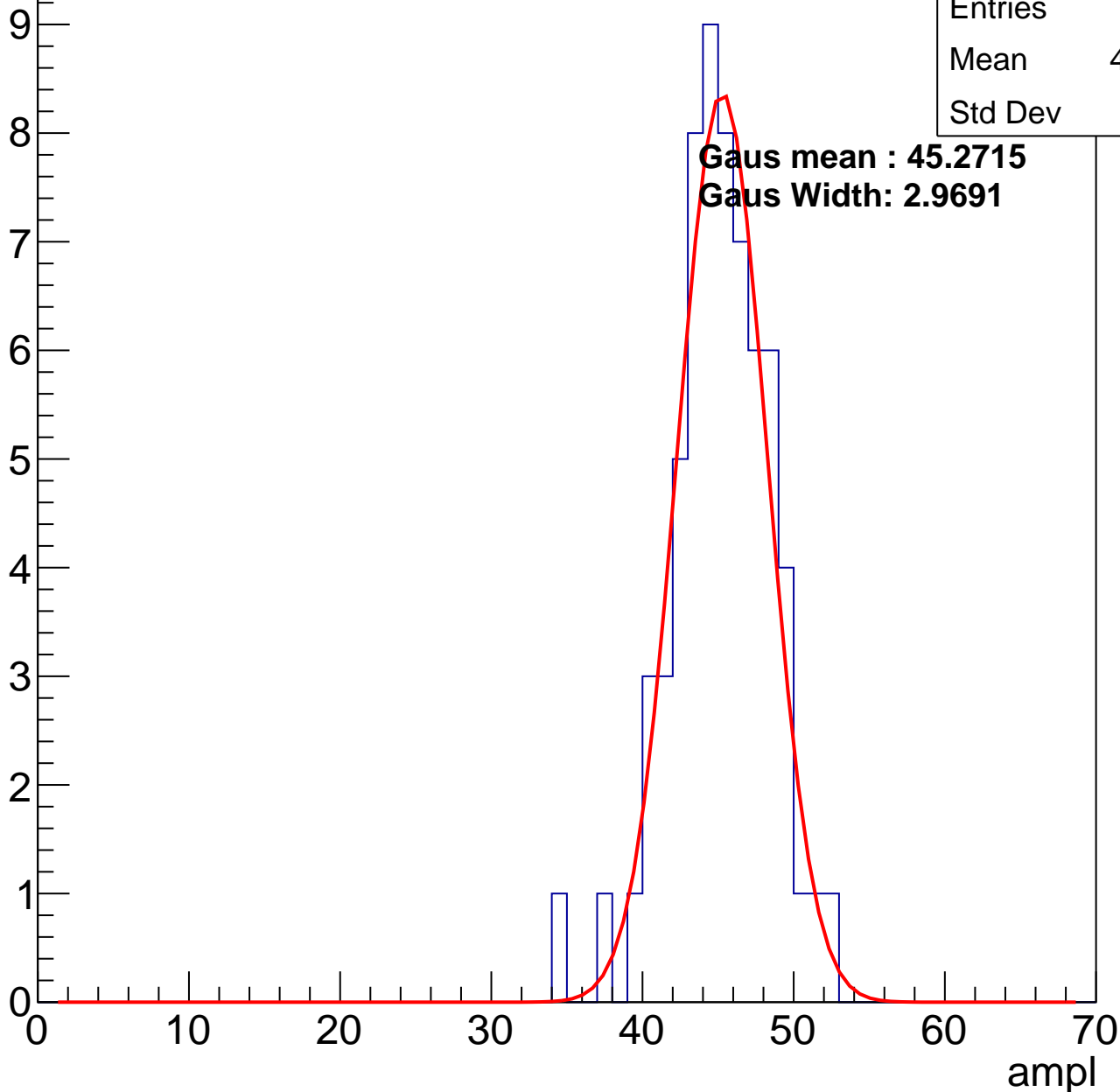
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	44.68
Std Dev	3.24

**Gaus mean : 45.2715**

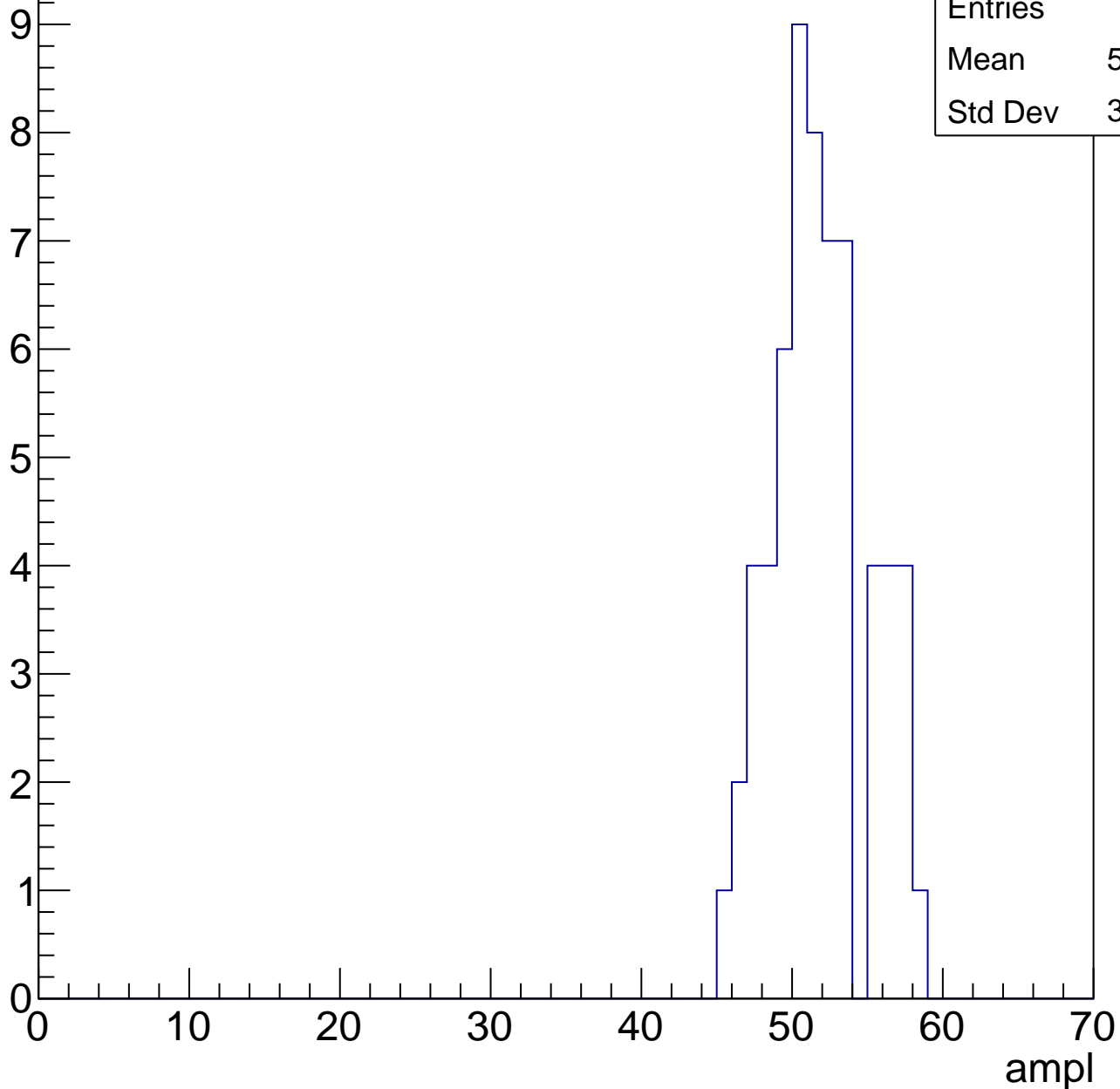
**Gaus Width: 2.9691**



# B1L101S, U19-ch13, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



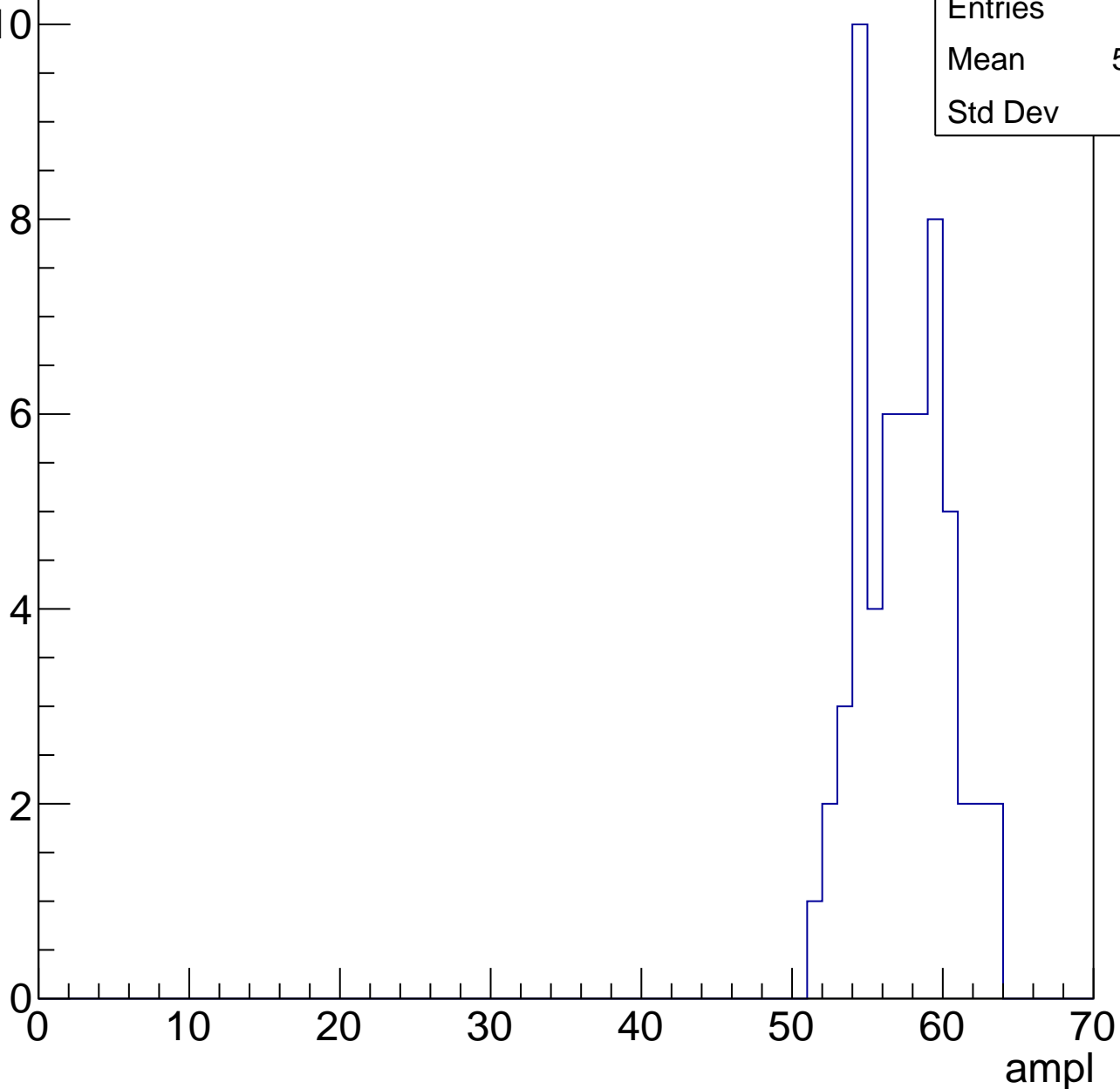
Entries	61
Mean	51.38
Std Dev	3.142

# B1L101S, U19-ch13, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	57
Mean	56.91
Std Dev	2.91

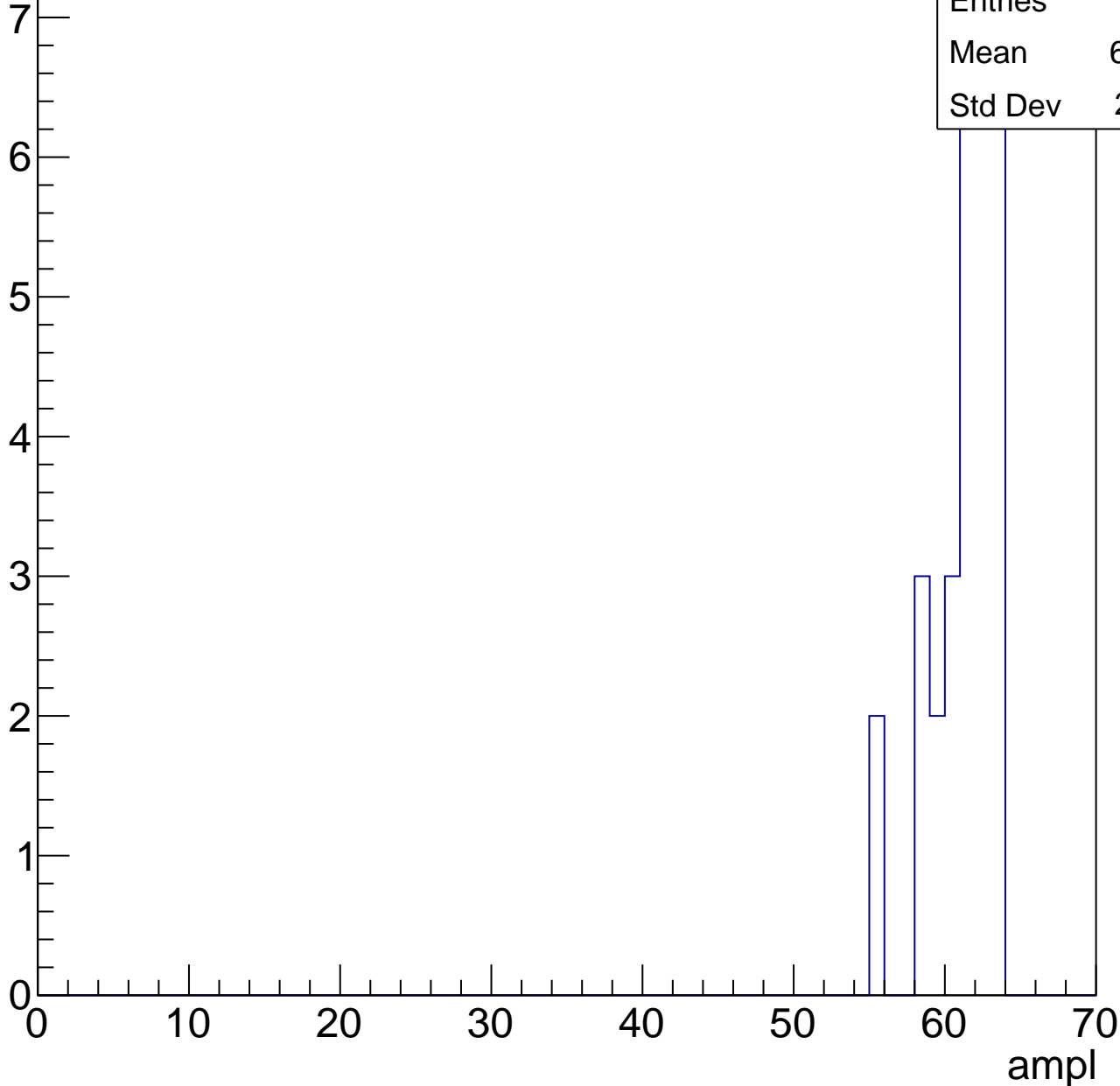


# B1L101S, U19-ch13, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	31
Mean	60.77
Std Dev	2.151



# B1L101S, U19-ch13, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	6
Mean	51
Std Dev	22.83

ampl

0 10 20 30 40 50 60 70



# B1L101S, U19-ch13, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U19-ch14, adc0

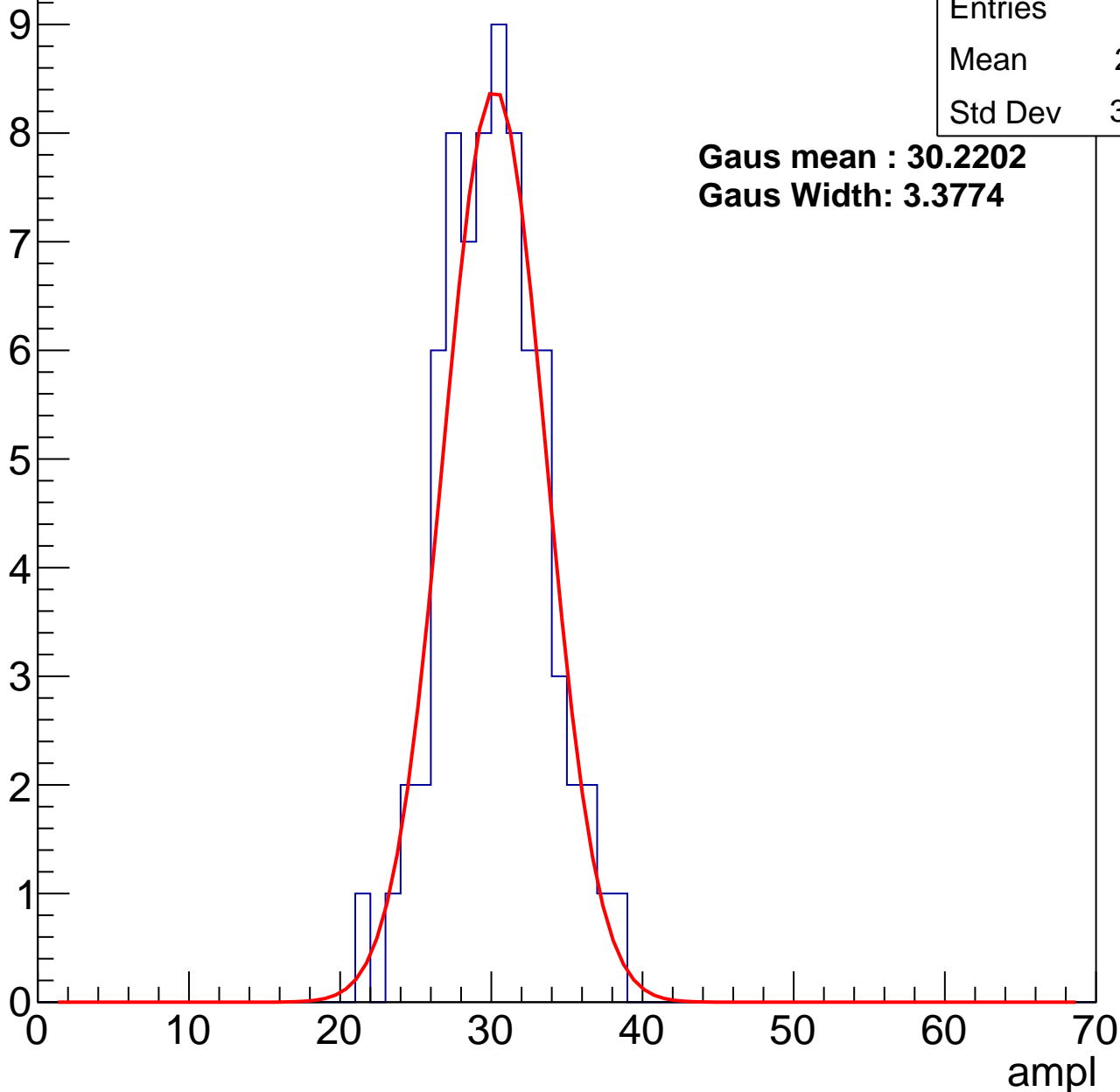
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	73
Mean	29.71
Std Dev	3.349

**Gaus mean : 30.2202**

**Gaus Width: 3.3774**



# B1L101S, U19-ch14, adc1

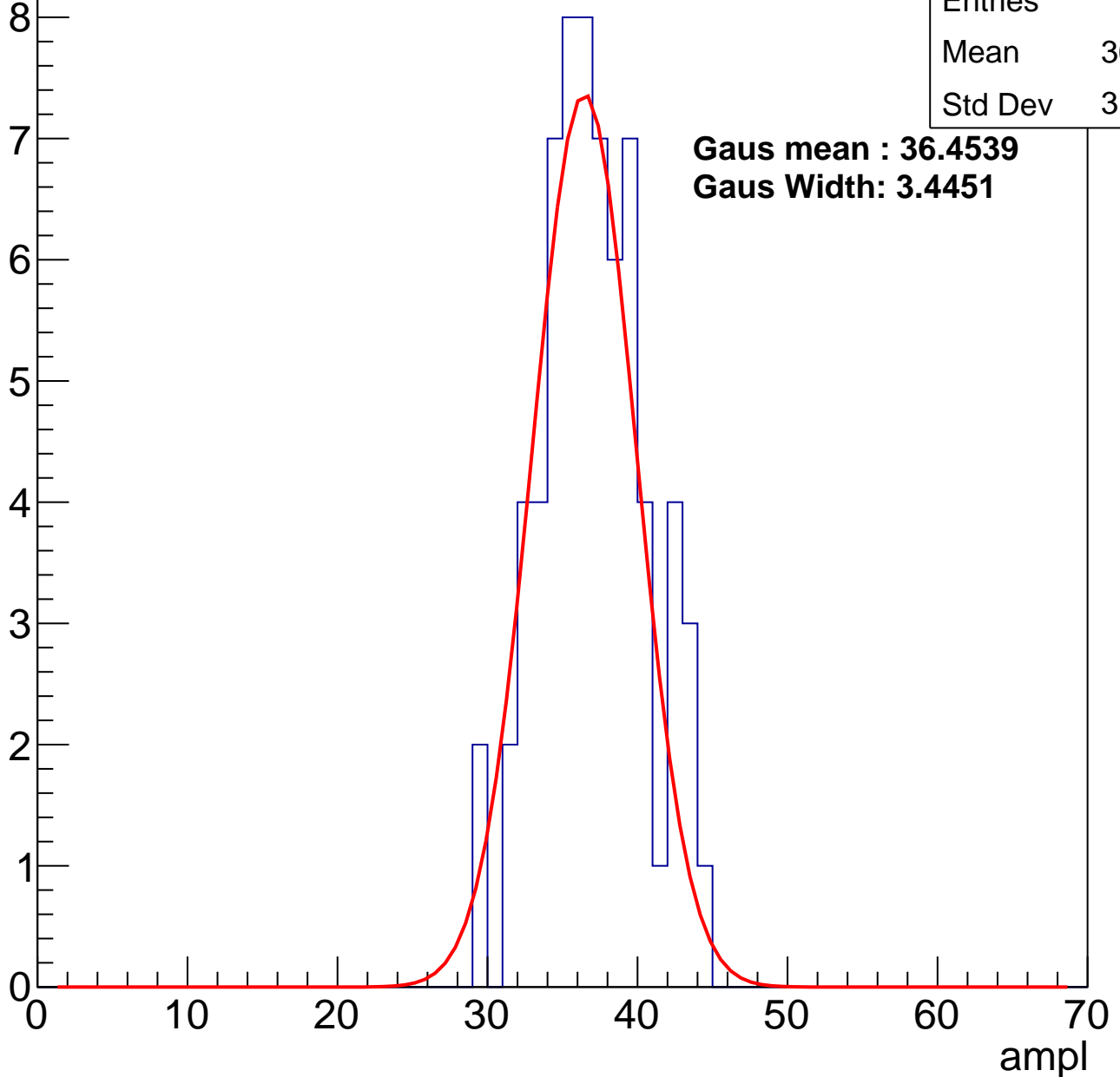
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	36.59
Std Dev	3.427

**Gaus mean : 36.4539**

**Gaus Width: 3.4451**



# B1L101S, U19-ch14, adc2

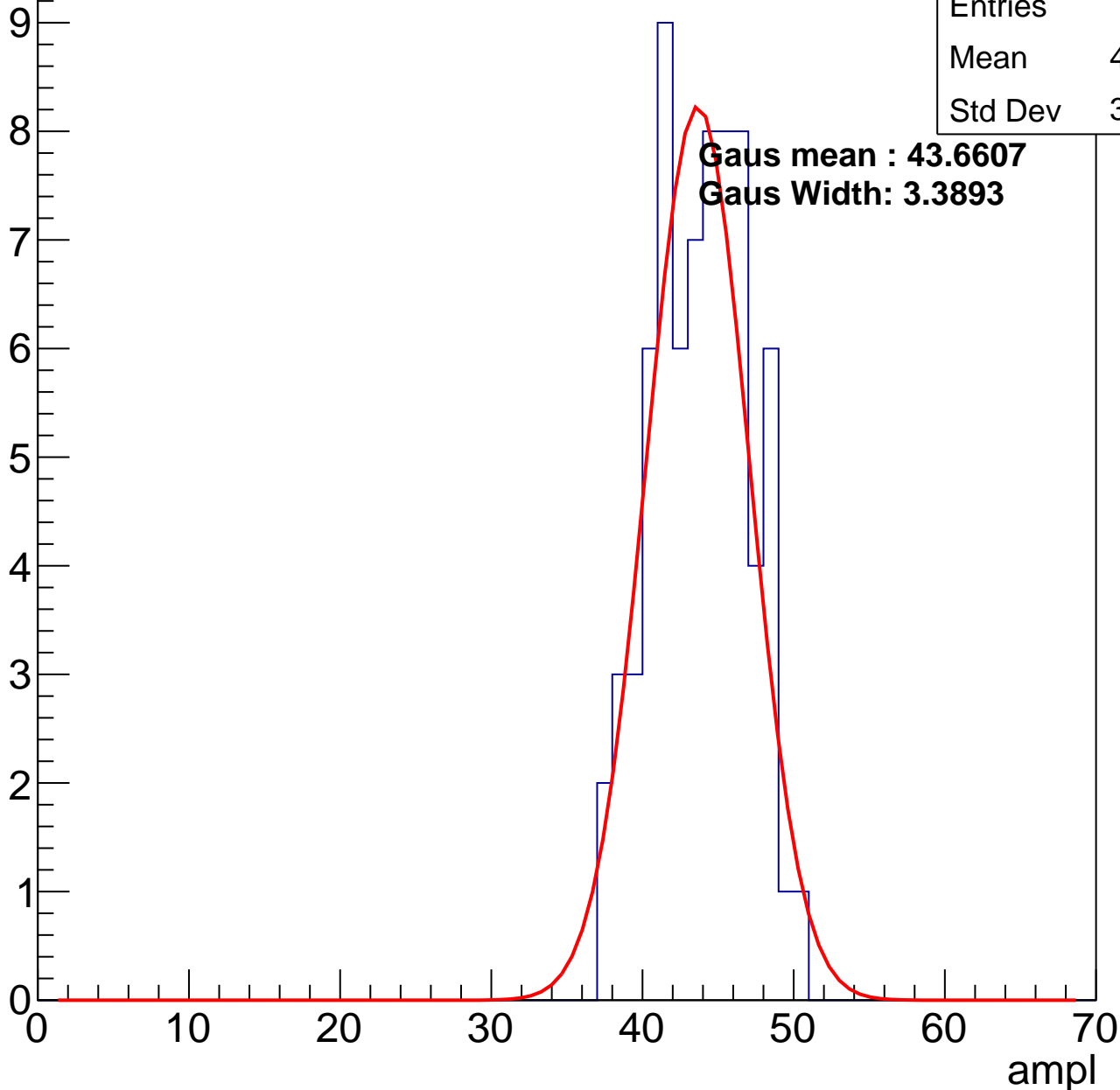
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	72
Mean	43.36
Std Dev	3.102

**Gaus mean : 43.6607**

**Gaus Width: 3.3893**

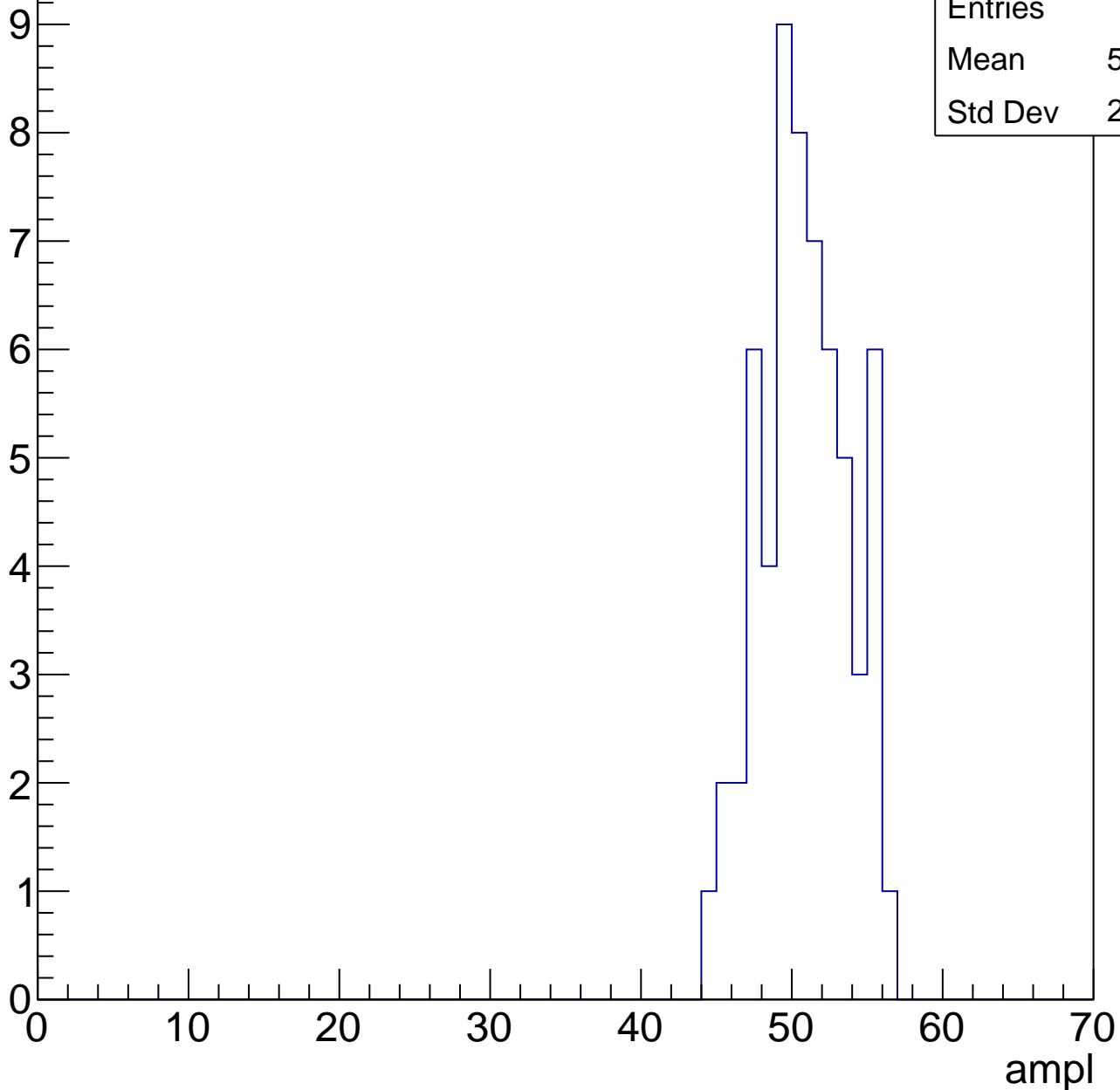


# B1L101S, U19-ch14, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

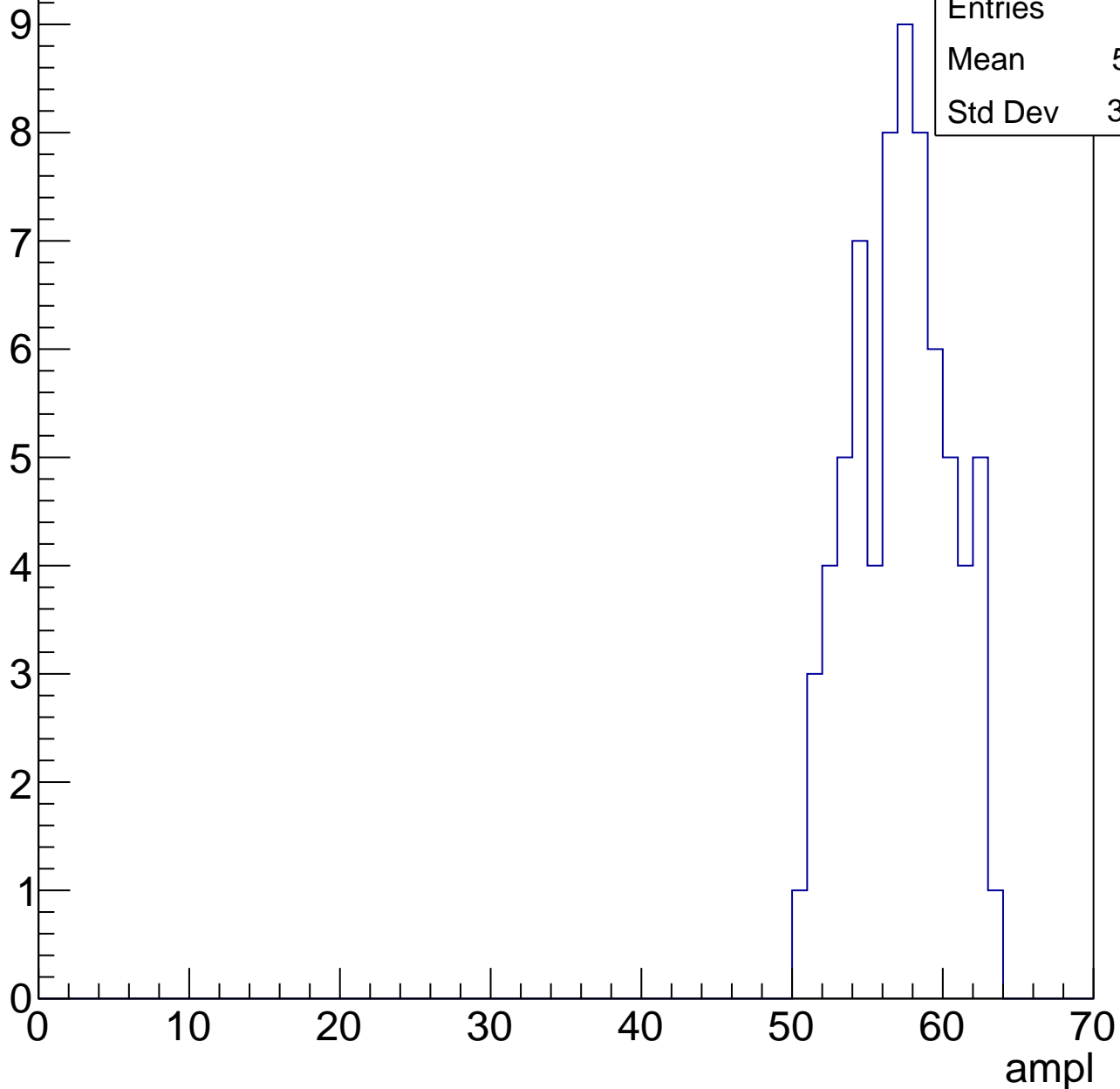
Entries	60
Mean	50.38
Std Dev	2.882



# B1L101S, U19-ch14, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

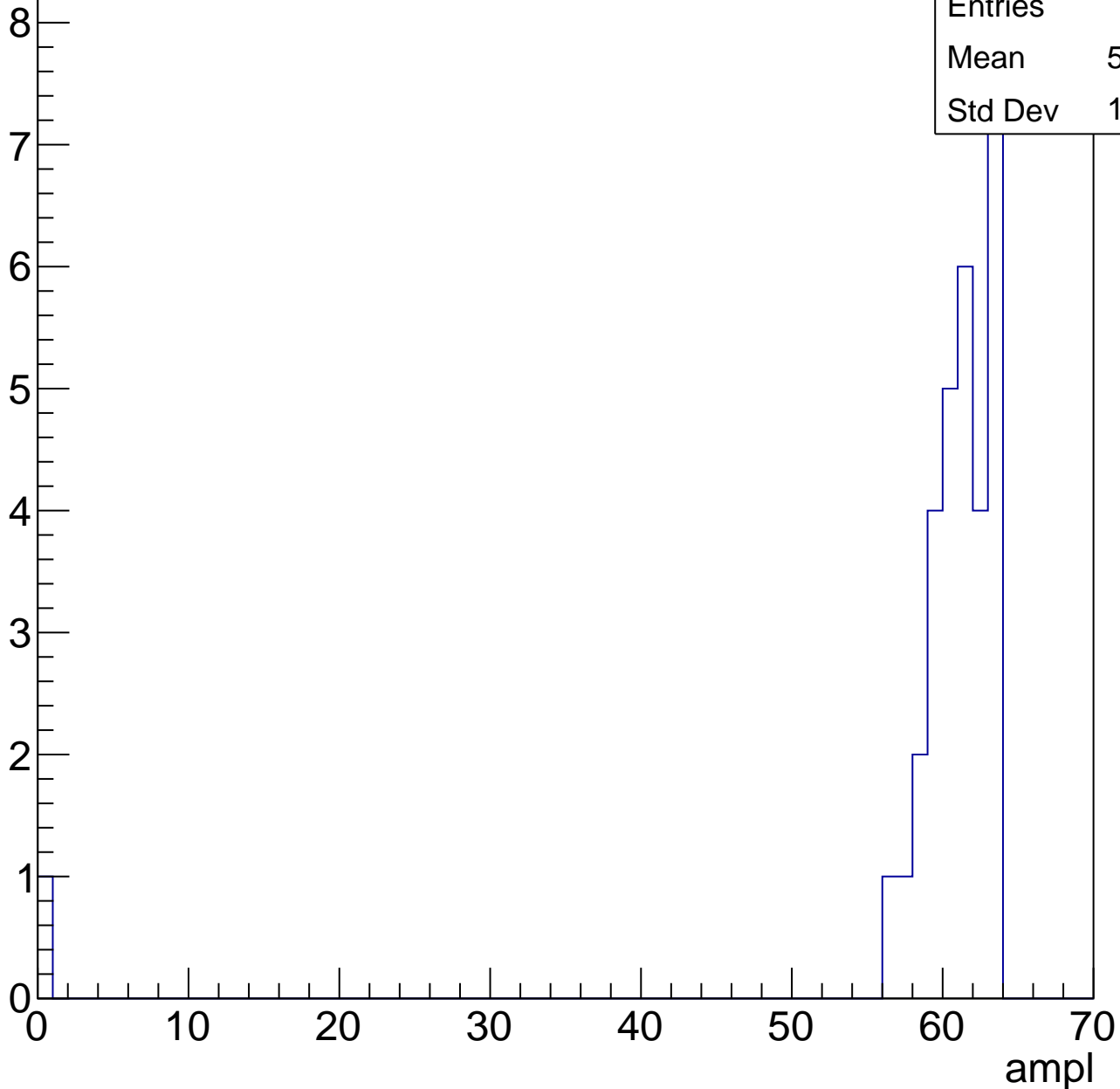


# B1L101S, U19-ch14, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	32
Mean	58.84
Std Dev	10.74



# B1L101S, U19-ch14, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U19-ch14, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L101S, U19-ch15, adc0

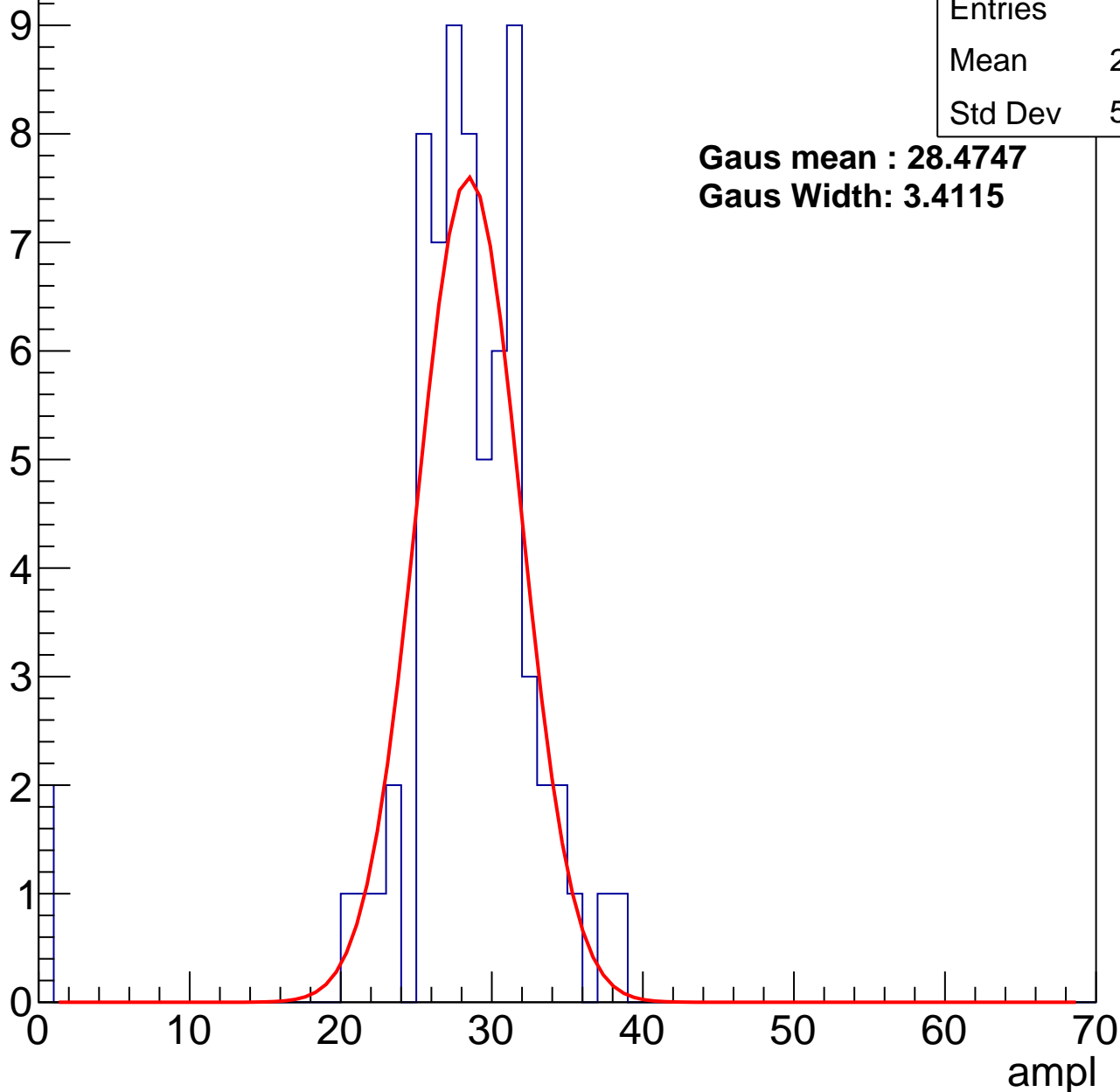
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	27.57
Std Dev	5.864

**Gaus mean : 28.4747**

**Gaus Width: 3.4115**



# B1L101S, U19-ch15, adc1

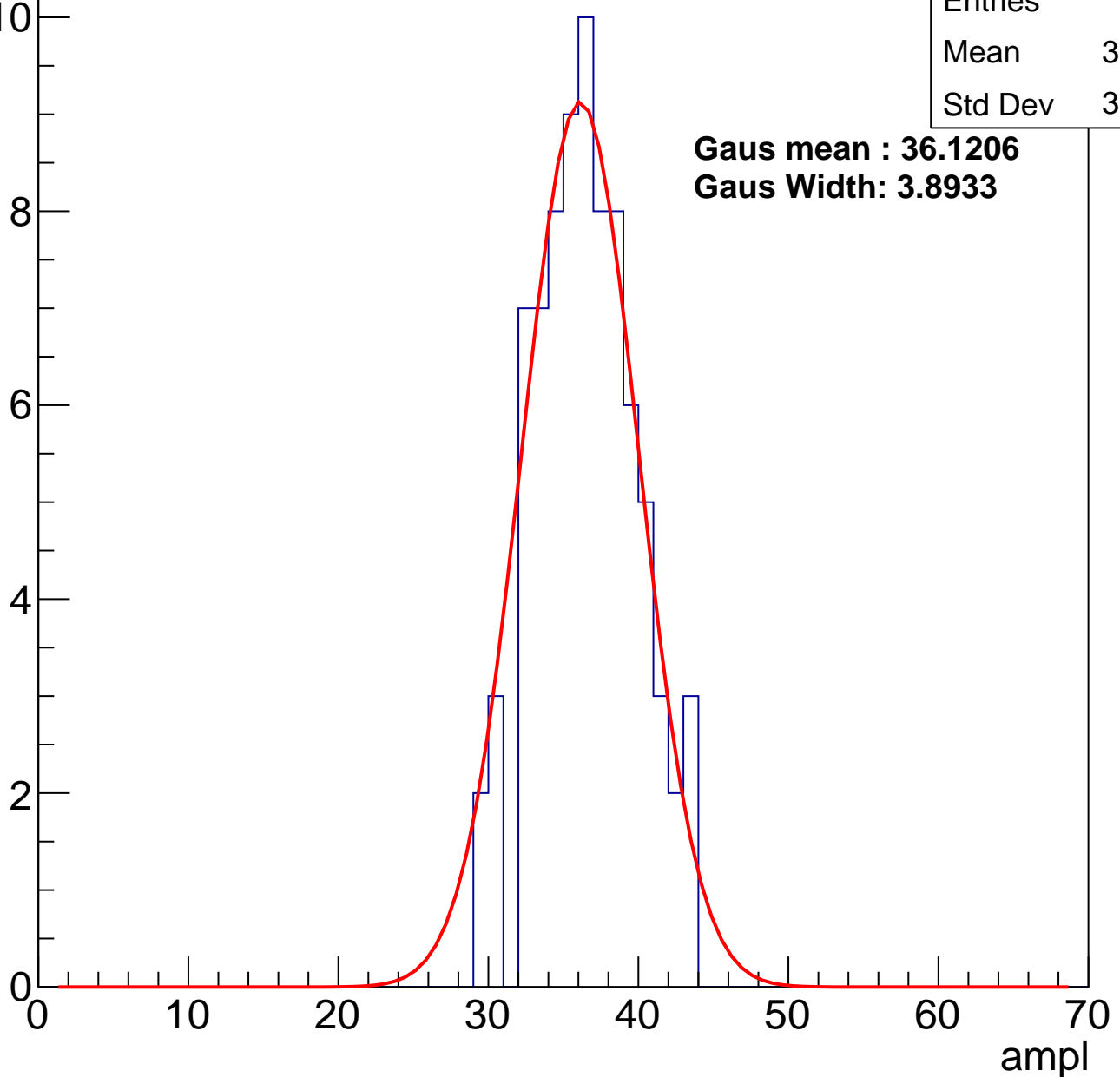
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	81
Mean	36.05
Std Dev	3.314

**Gaus mean : 36.1206**

**Gaus Width: 3.8933**



# B1L101S, U19-ch15, adc2

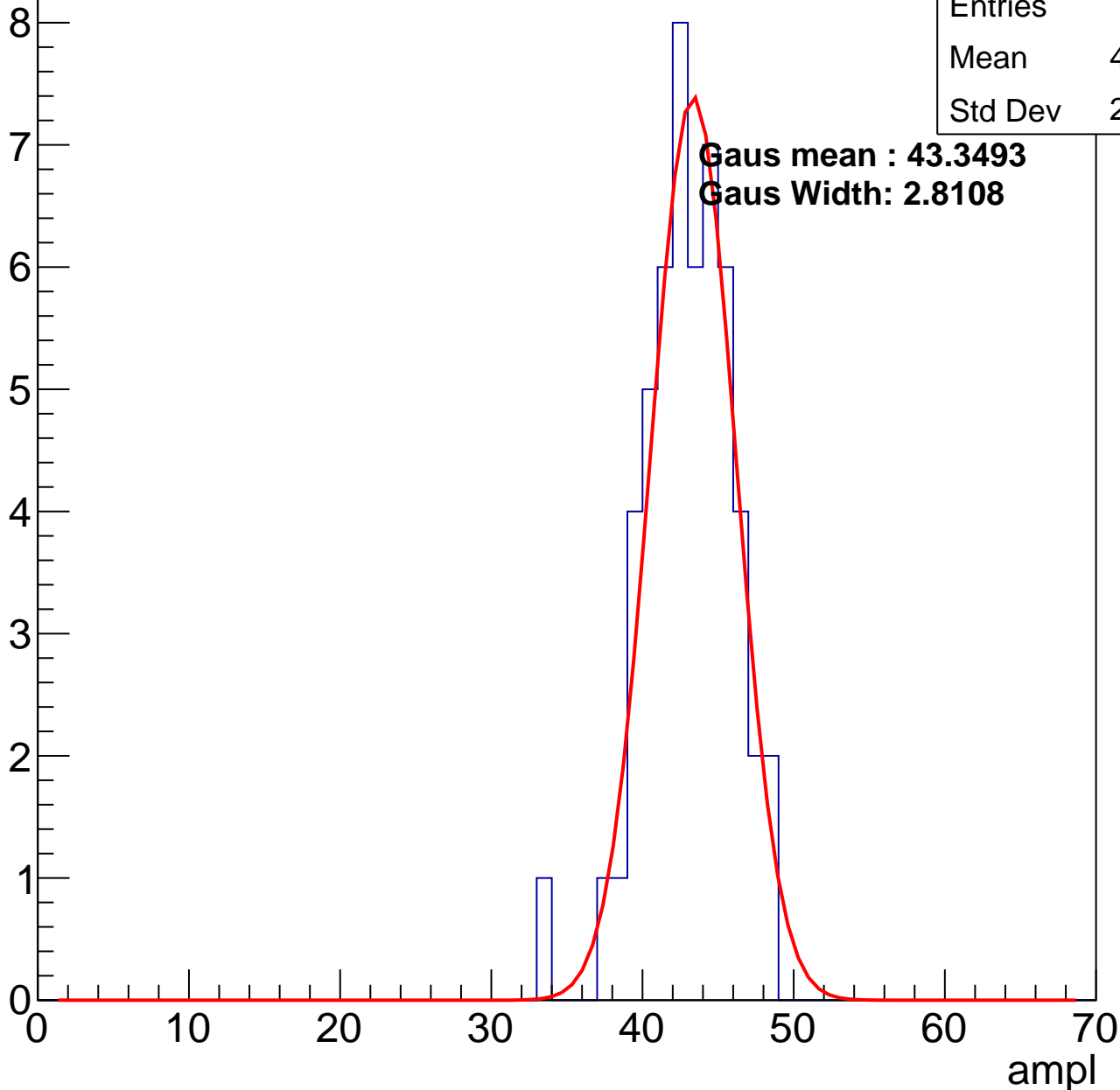
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	53
Mean	42.57
Std Dev	2.885

**Gaus mean : 43.3493**

**Gaus Width: 2.8108**

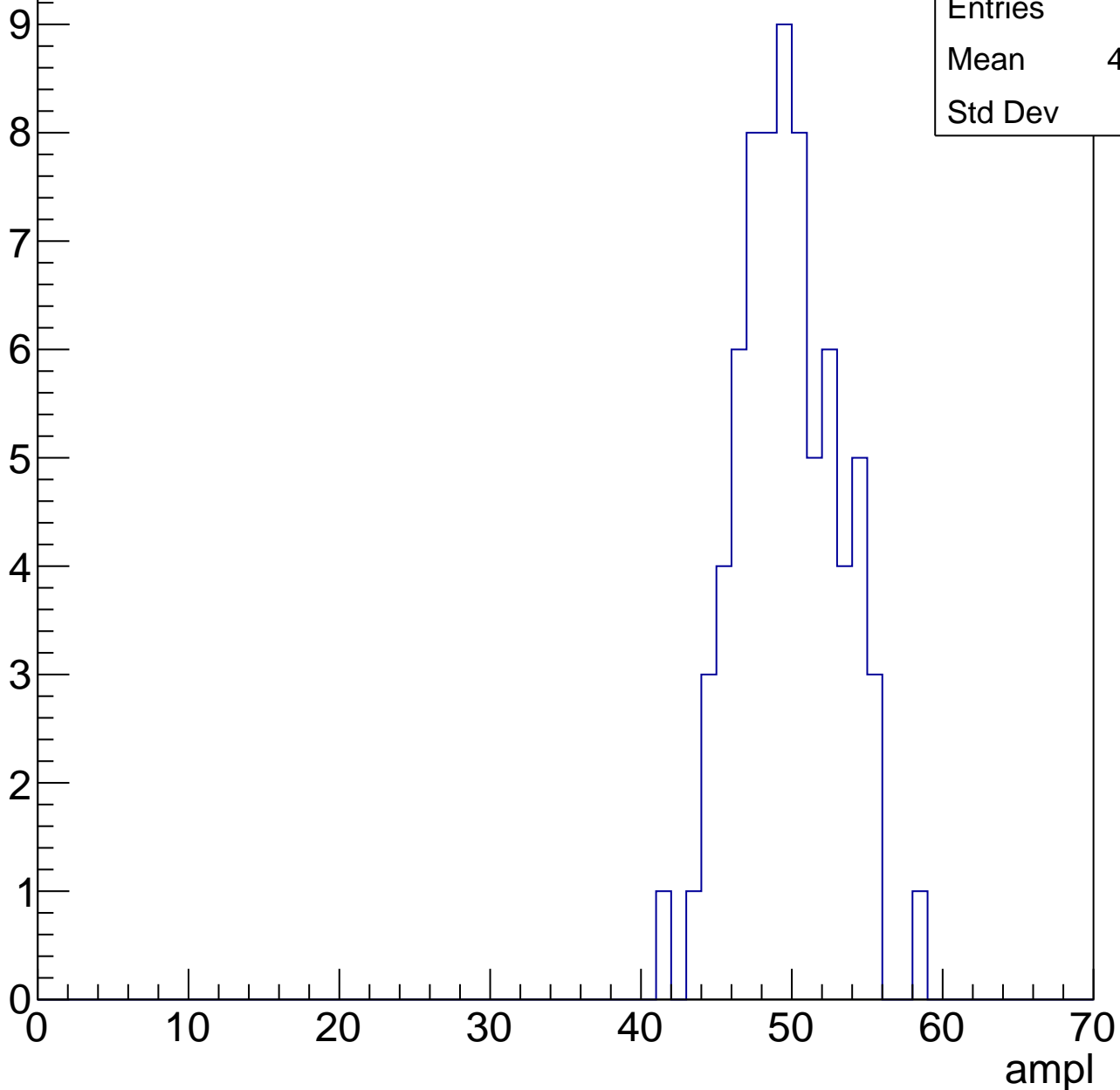


# B1L101S, U19-ch15, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	72
Mean	49.24
Std Dev	3.31

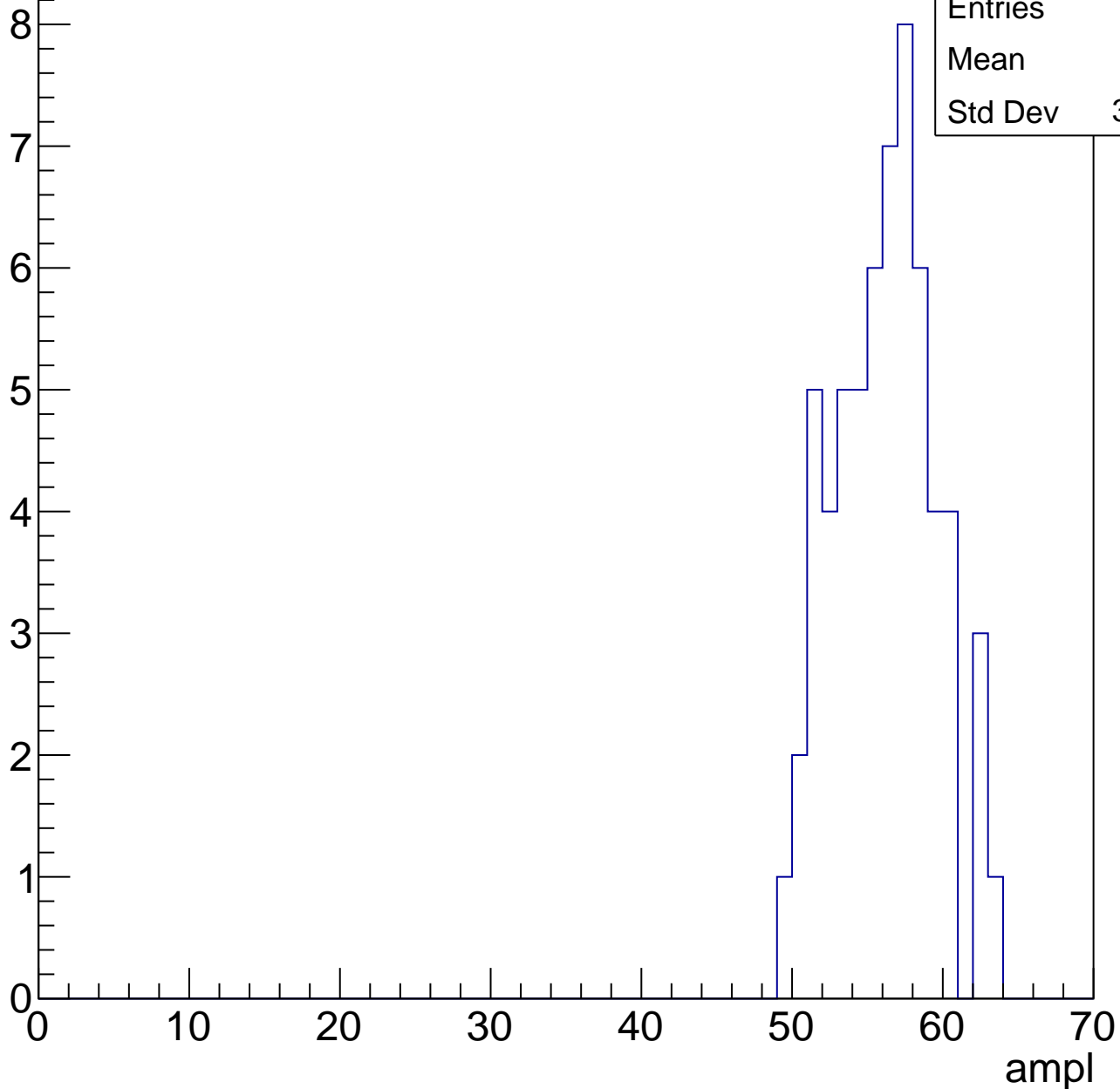


# B1L101S, U19-ch15, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	55.7
Std Dev	3.301

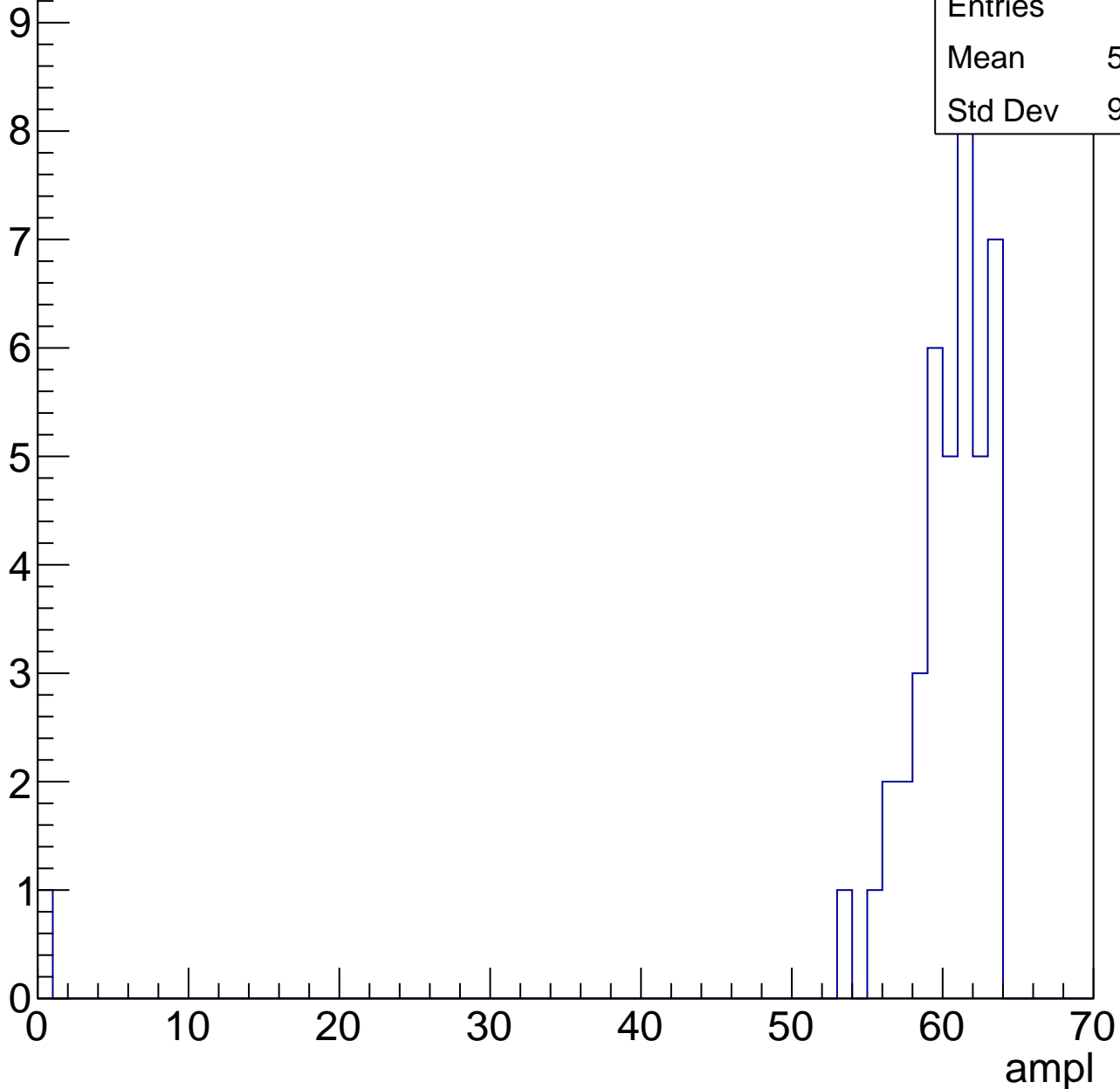


# B1L101S, U19-ch15, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	42
Mean	58.62
Std Dev	9.454



# B1L101S, U19-ch15, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

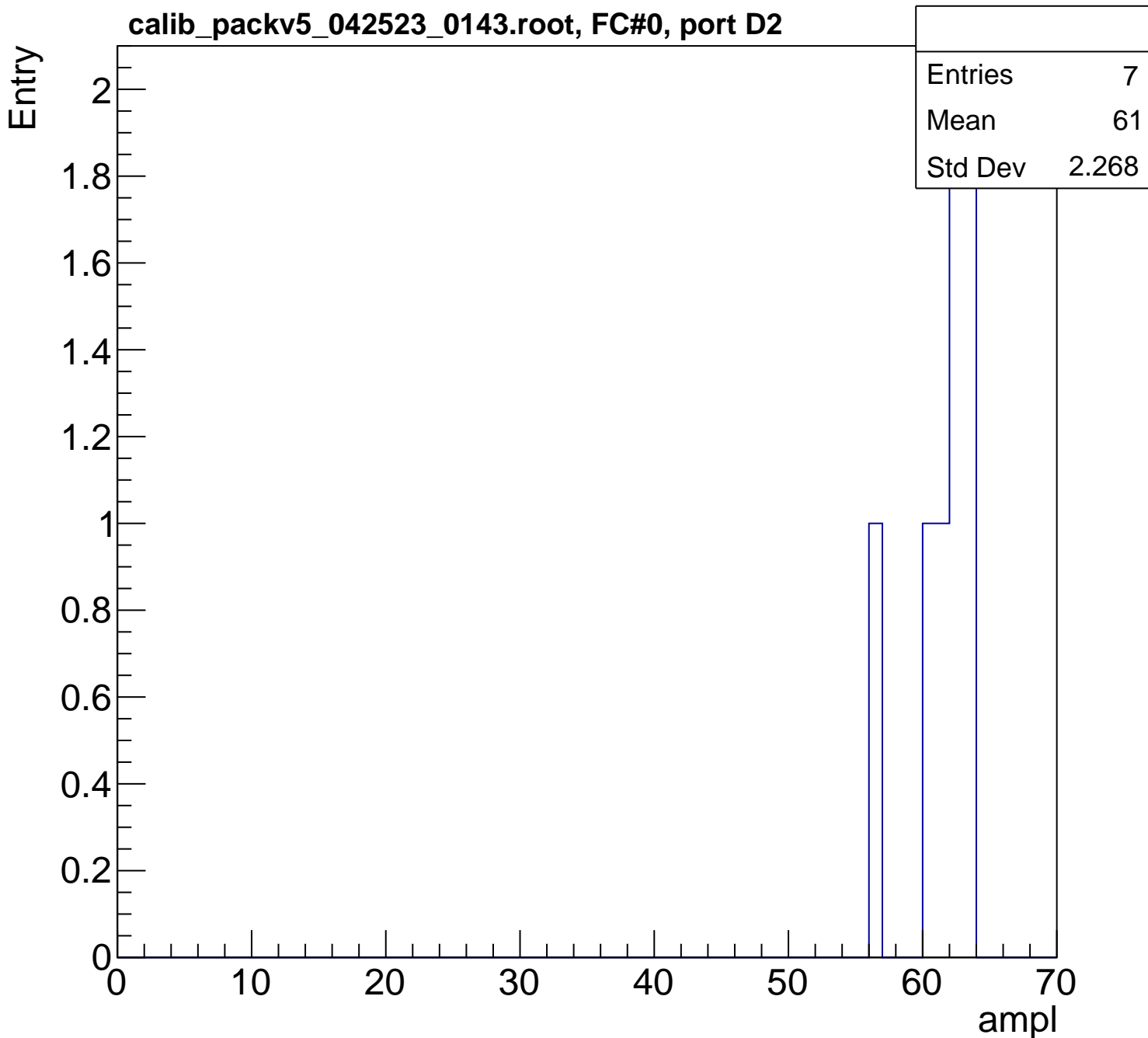
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	7
Mean	61
Std Dev	2.268

ampl

0 10 20 30 40 50 60 70





# B1L101S, U19-ch15, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L101S, U19-ch16, adc0

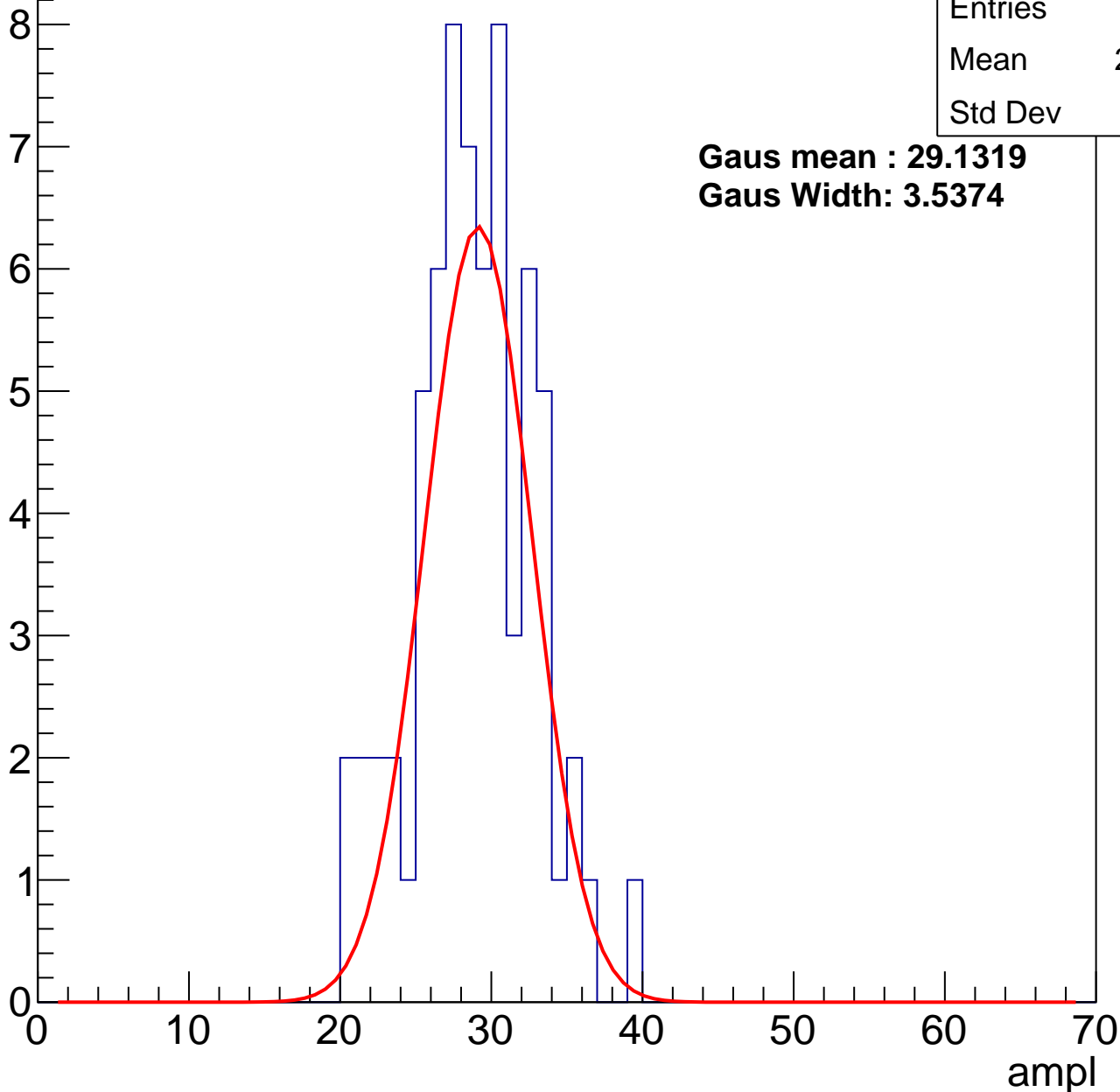
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	28.41
Std Dev	3.9

**Gaus mean : 29.1319**

**Gaus Width: 3.5374**



# B1L101S, U19-ch16, adc1

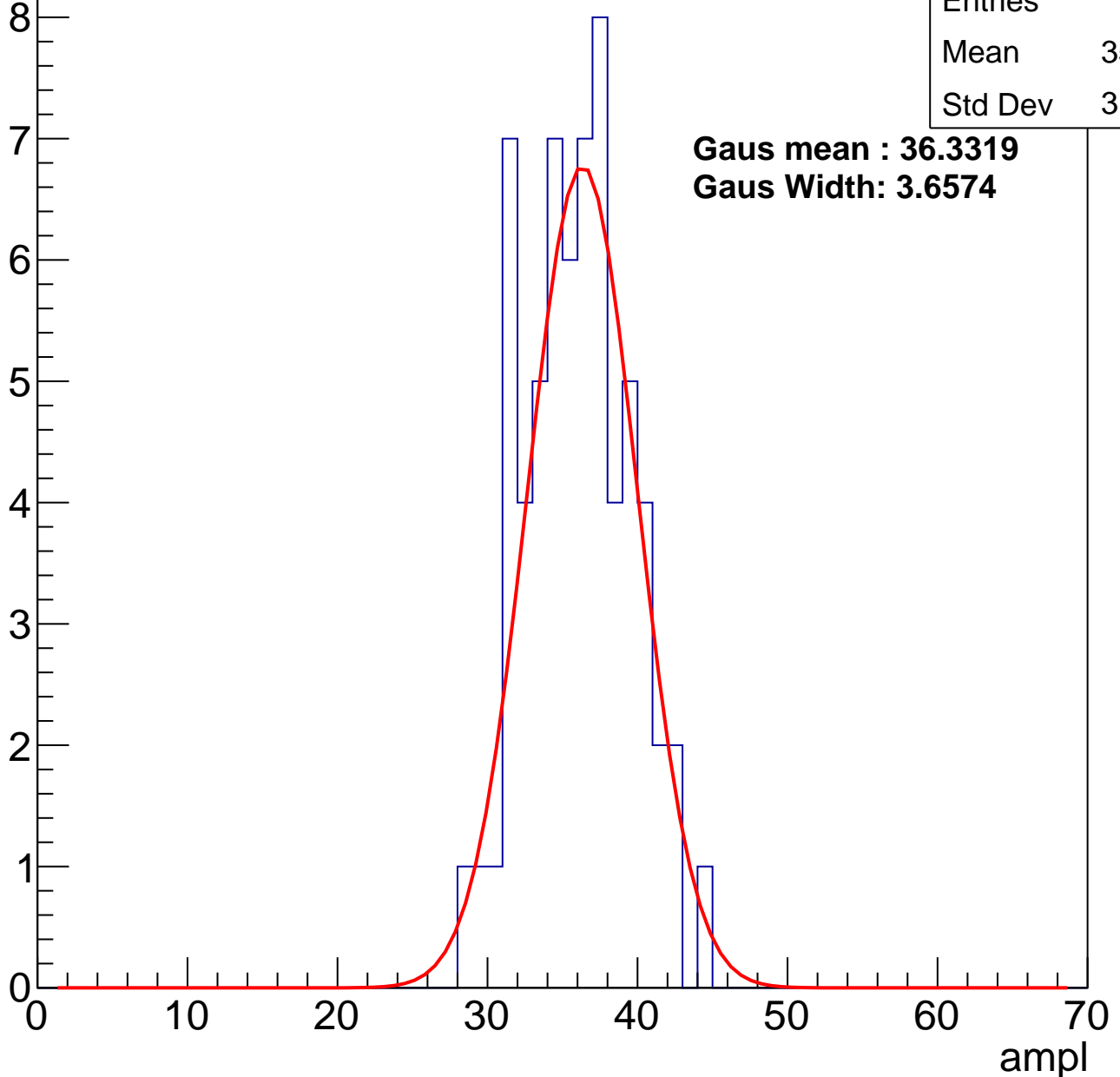
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	35.54
Std Dev	3.447

**Gaus mean : 36.3319**

**Gaus Width: 3.6574**



# B1L101S, U19-ch16, adc2

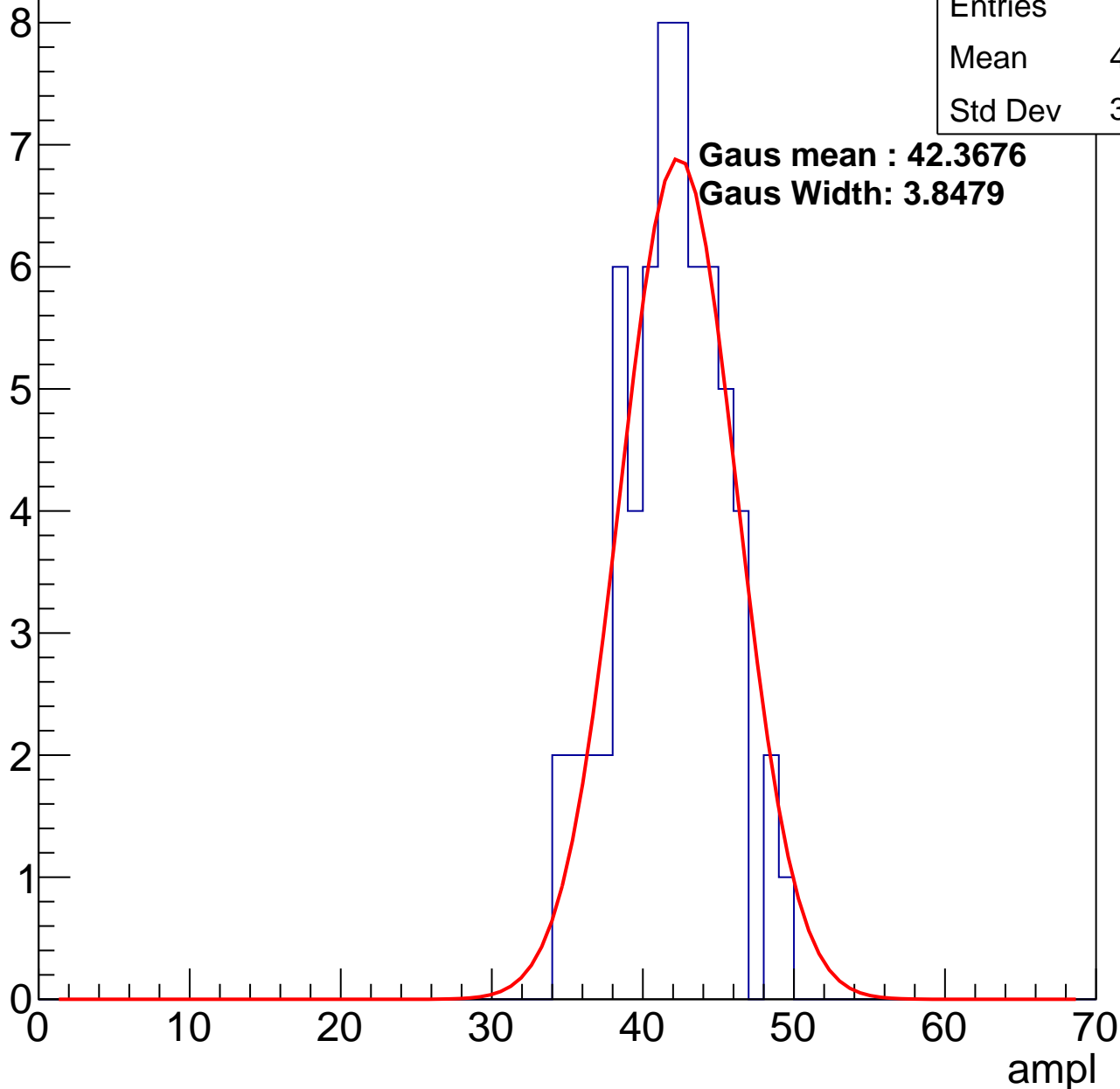
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	41.38
Std Dev	3.416

**Gaus mean : 42.3676**

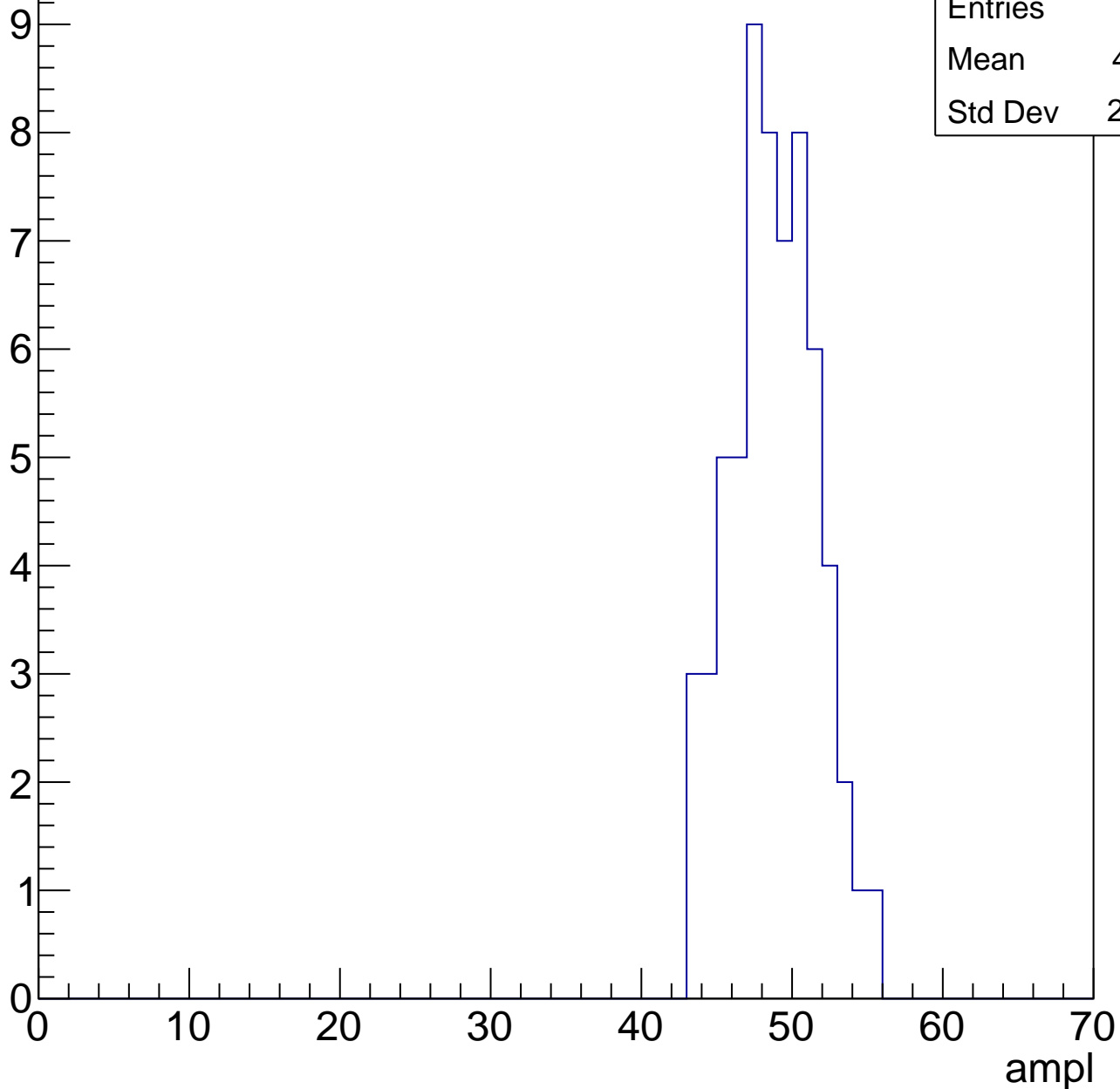
**Gaus Width: 3.8479**



# B1L101S, U19-ch16, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

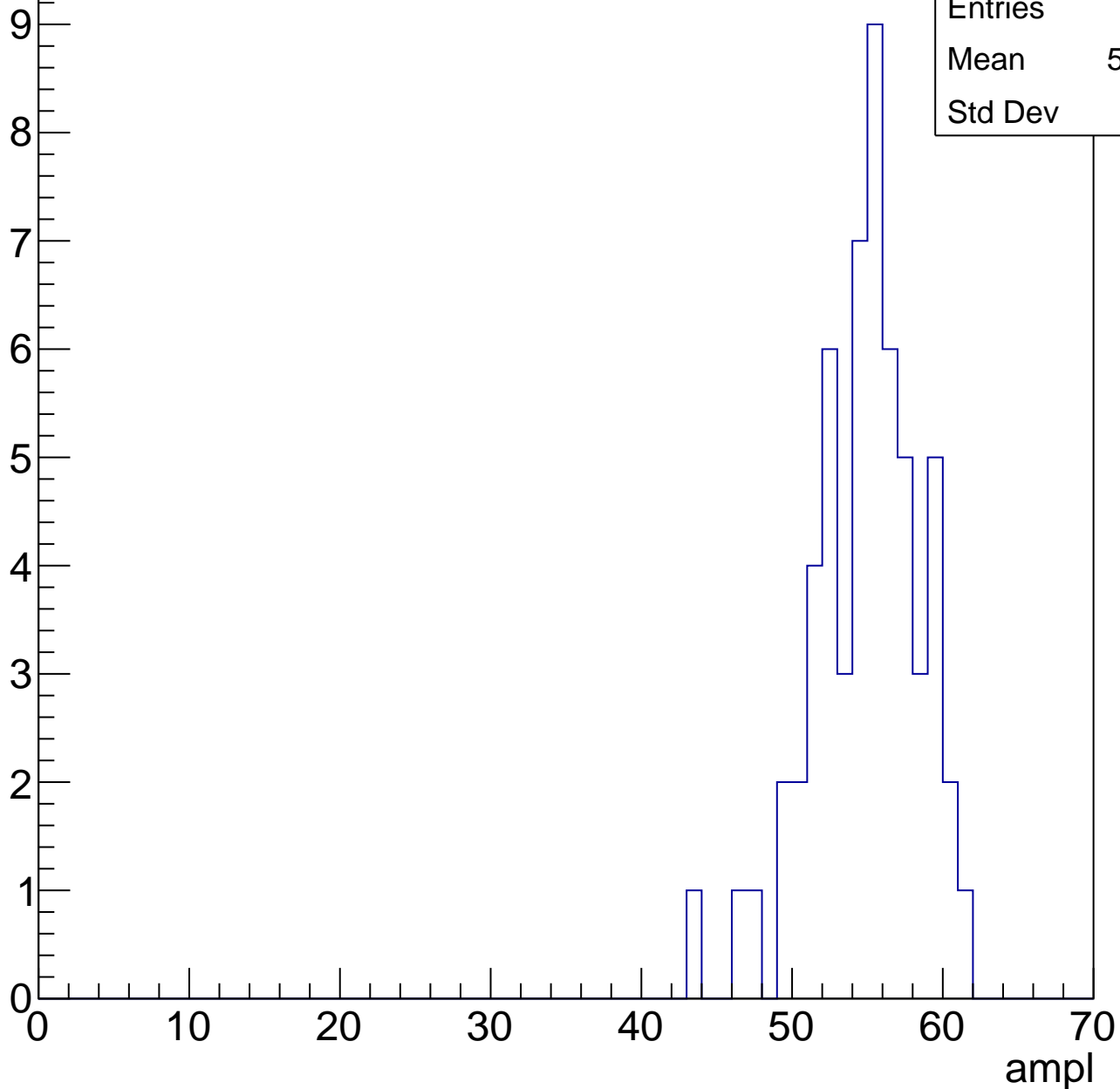


Entries	62
Mean	48.31
Std Dev	2.792

# B1L101S, U19-ch16, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

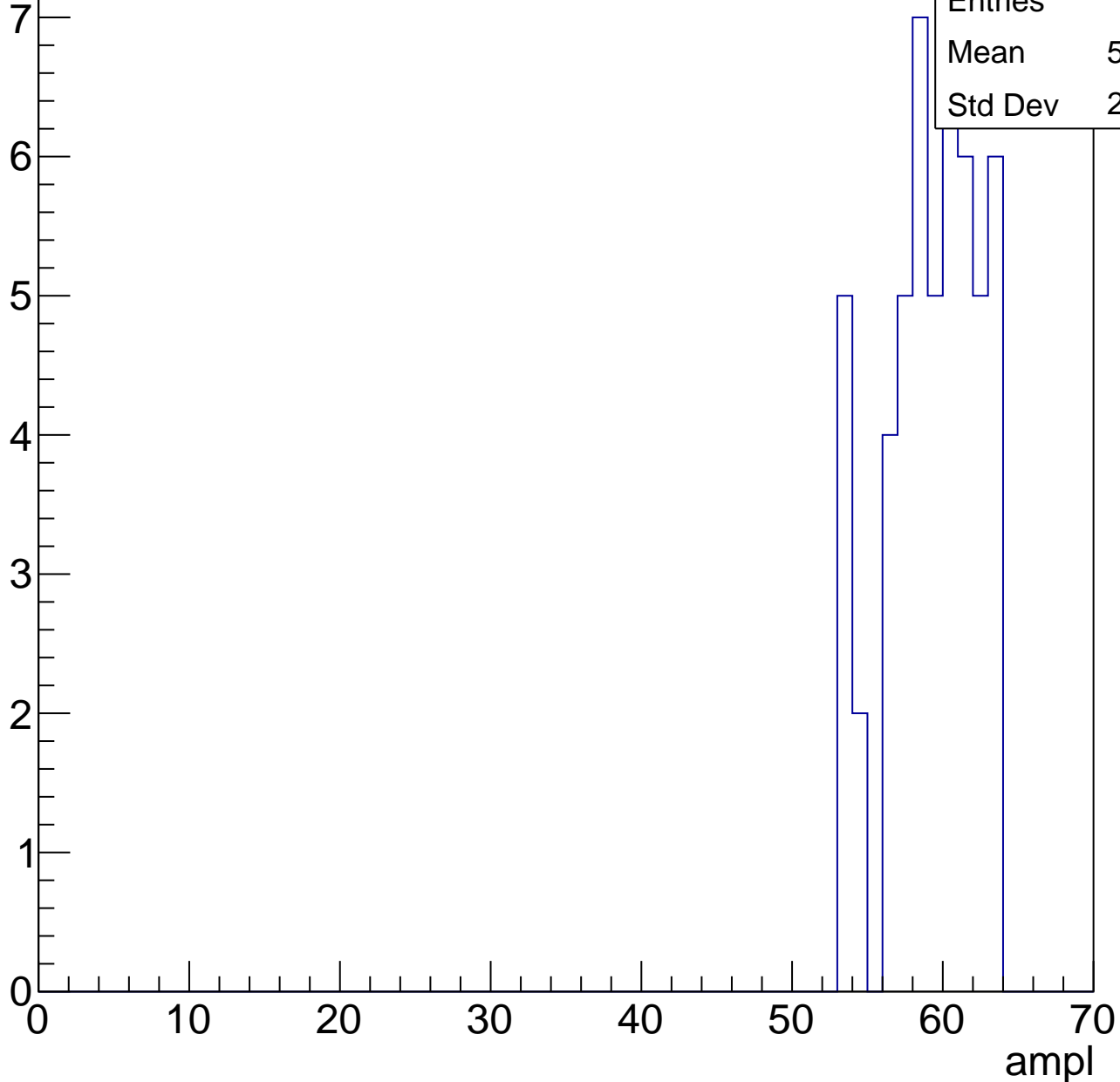


Entries	58
Mean	54.36
Std Dev	3.58

# B1L101S, U19-ch16, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

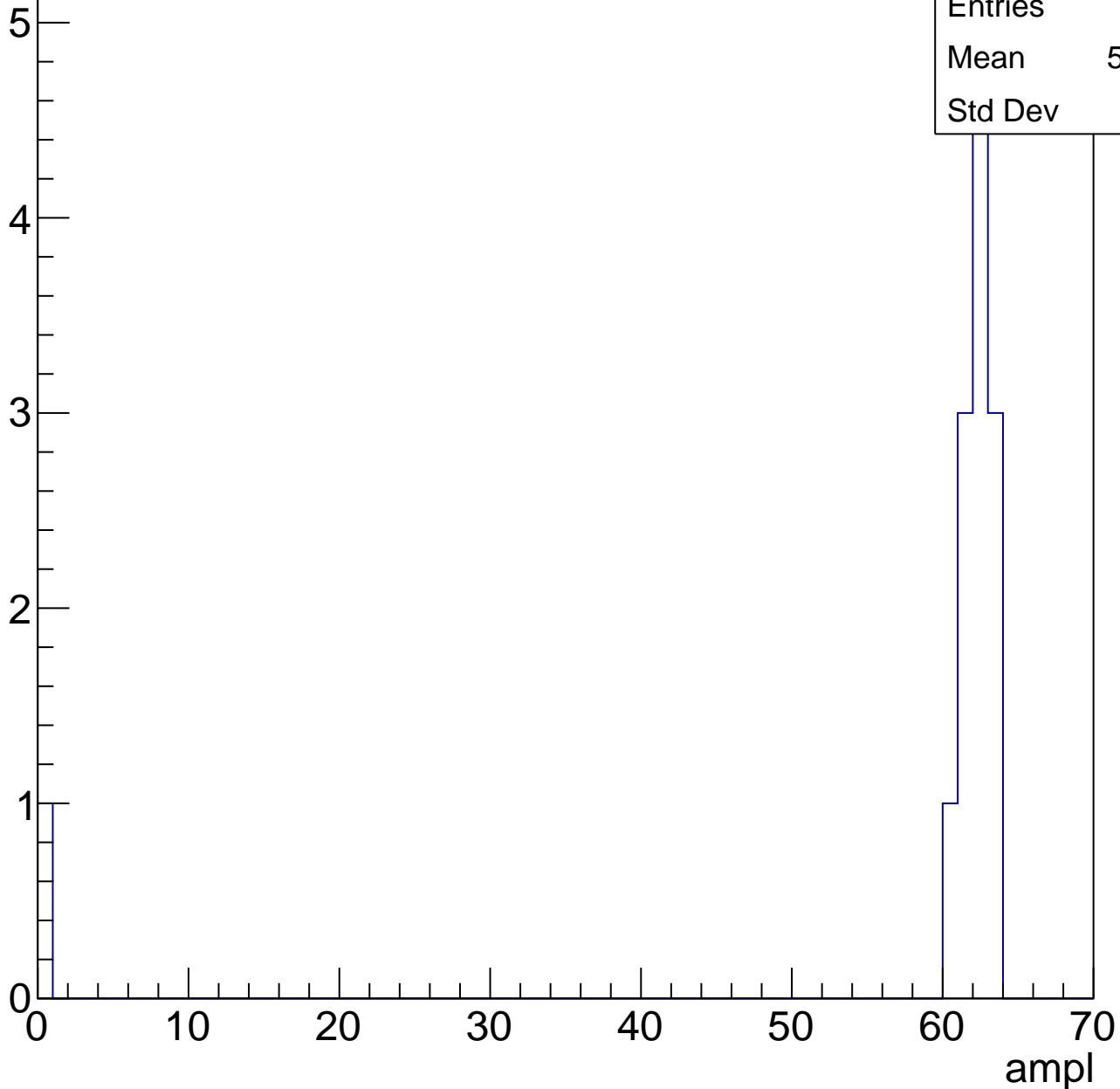


# B1L101S, U19-ch16, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	13
Mean	57.08
Std Dev	16.5





# B1L101S, U19-ch16, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U19-ch17, adc0

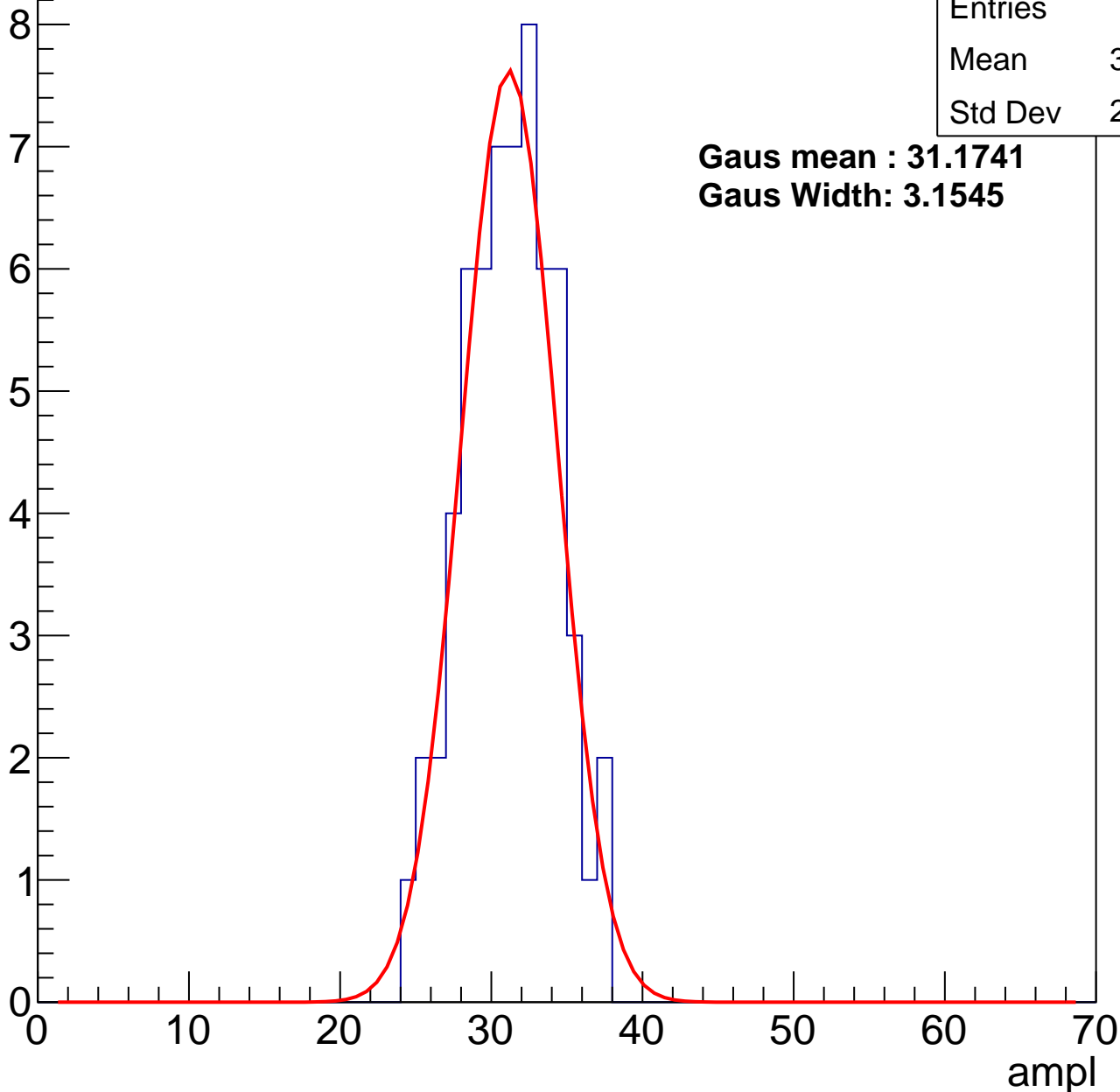
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	30.75
Std Dev	2.995

**Gaus mean : 31.1741**

**Gaus Width: 3.1545**



# B1L101S, U19-ch17, adc1

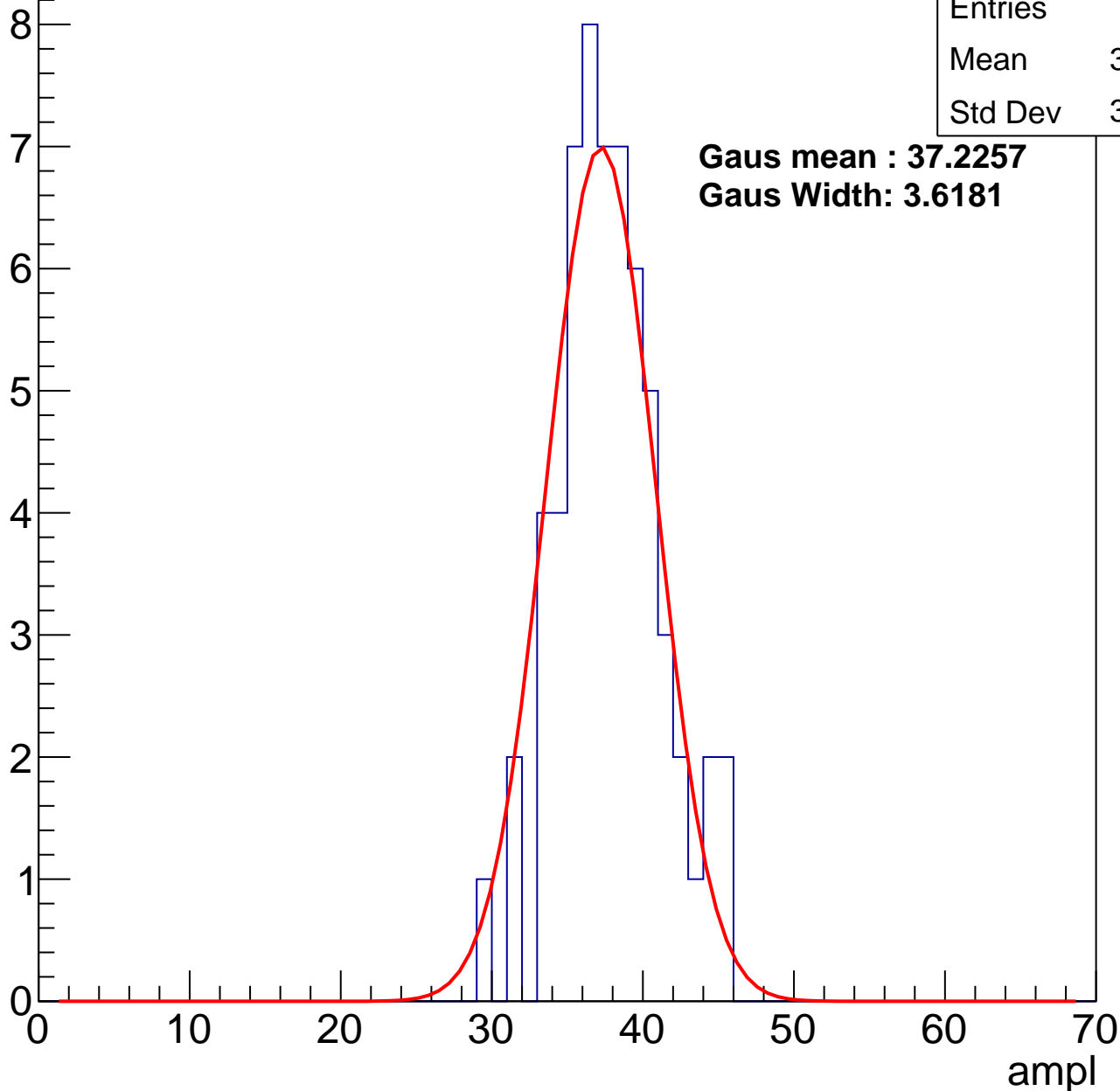
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	37.36
Std Dev	3.388

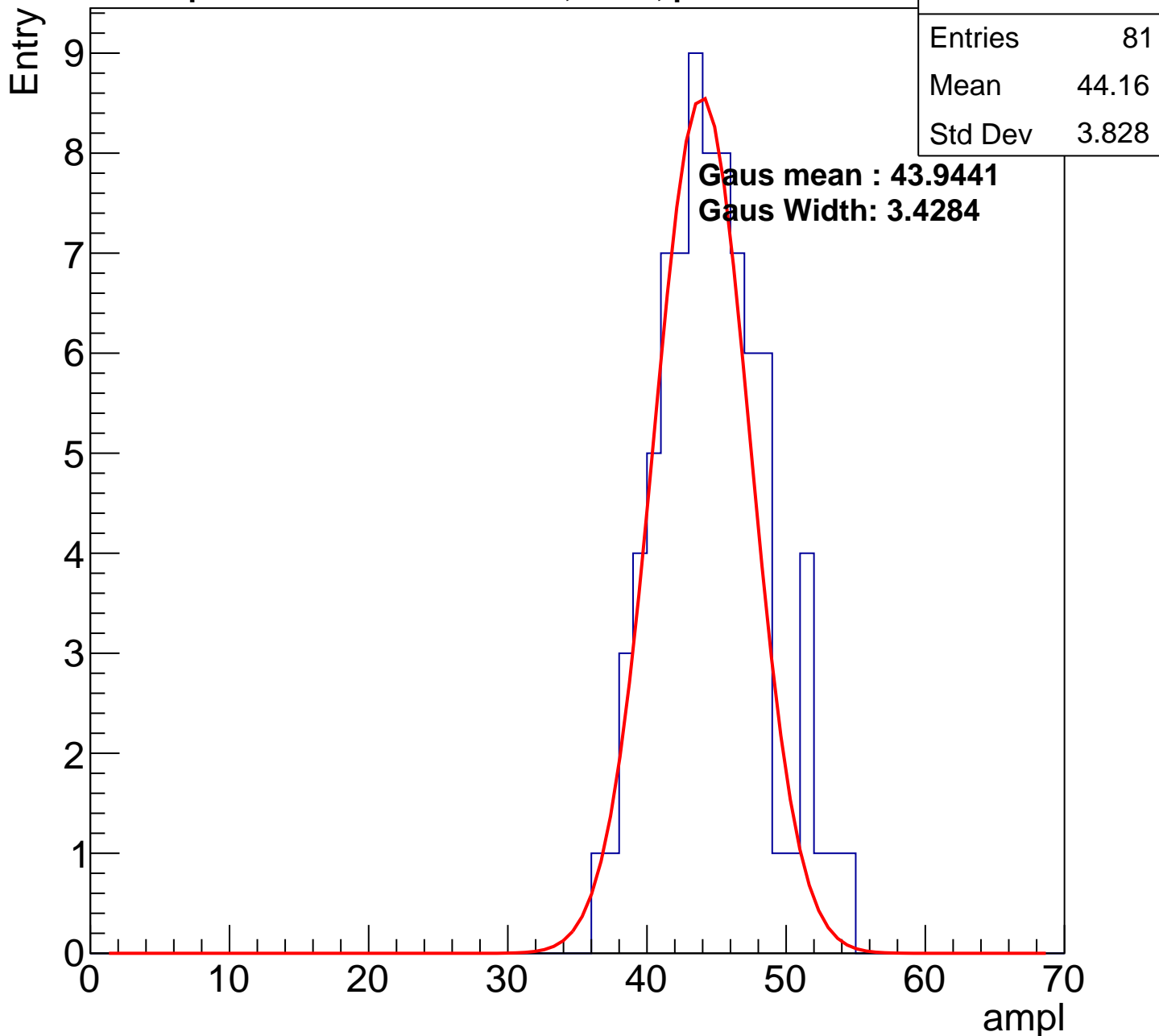
**Gaus mean : 37.2257**

**Gaus Width: 3.6181**



# B1L101S, U19-ch17, adc2

calib\_packv5\_042523\_0143.root, FC#0, port D2

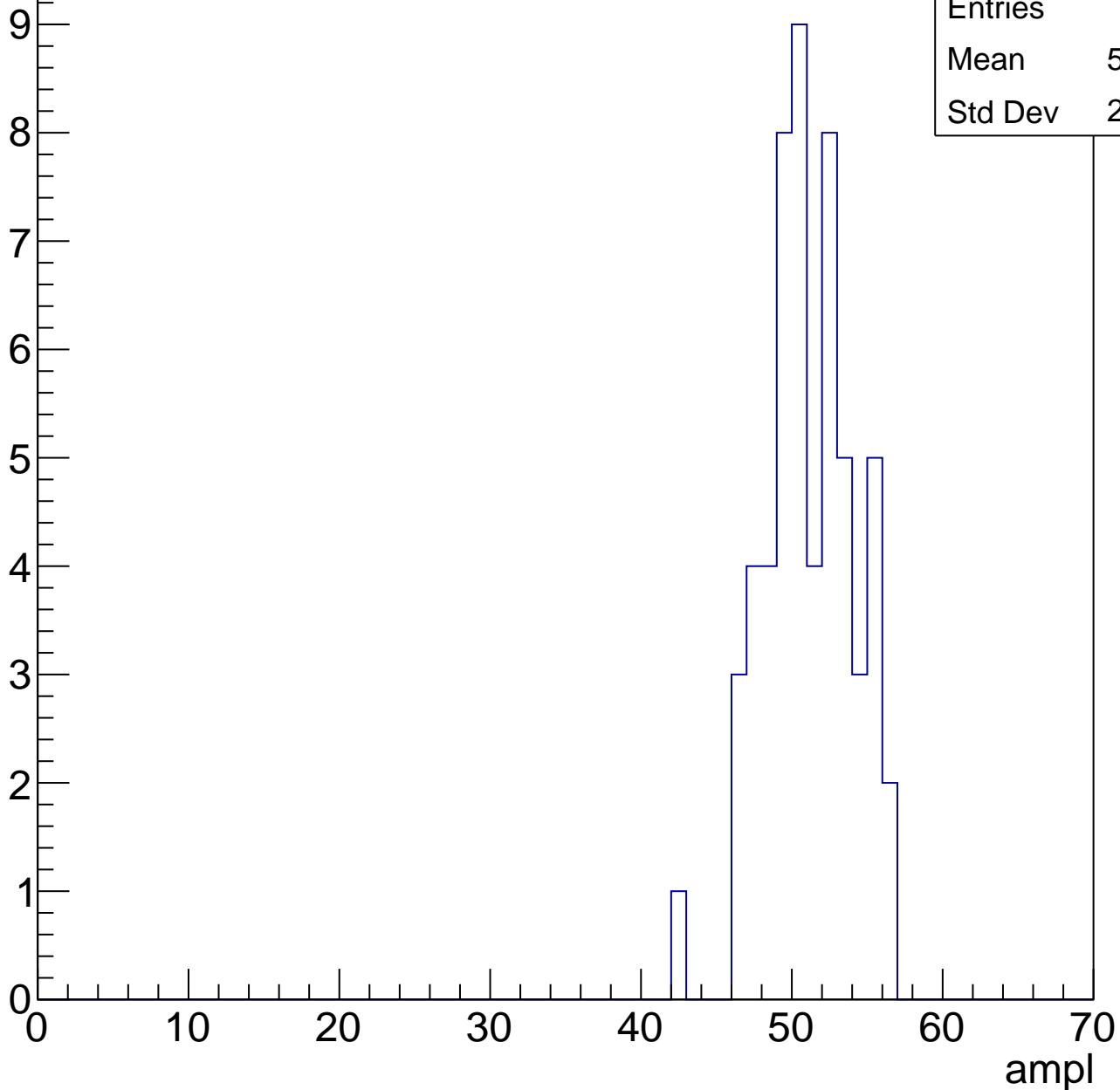


# B1L101S, U19-ch17, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	56
Mean	50.64
Std Dev	2.912

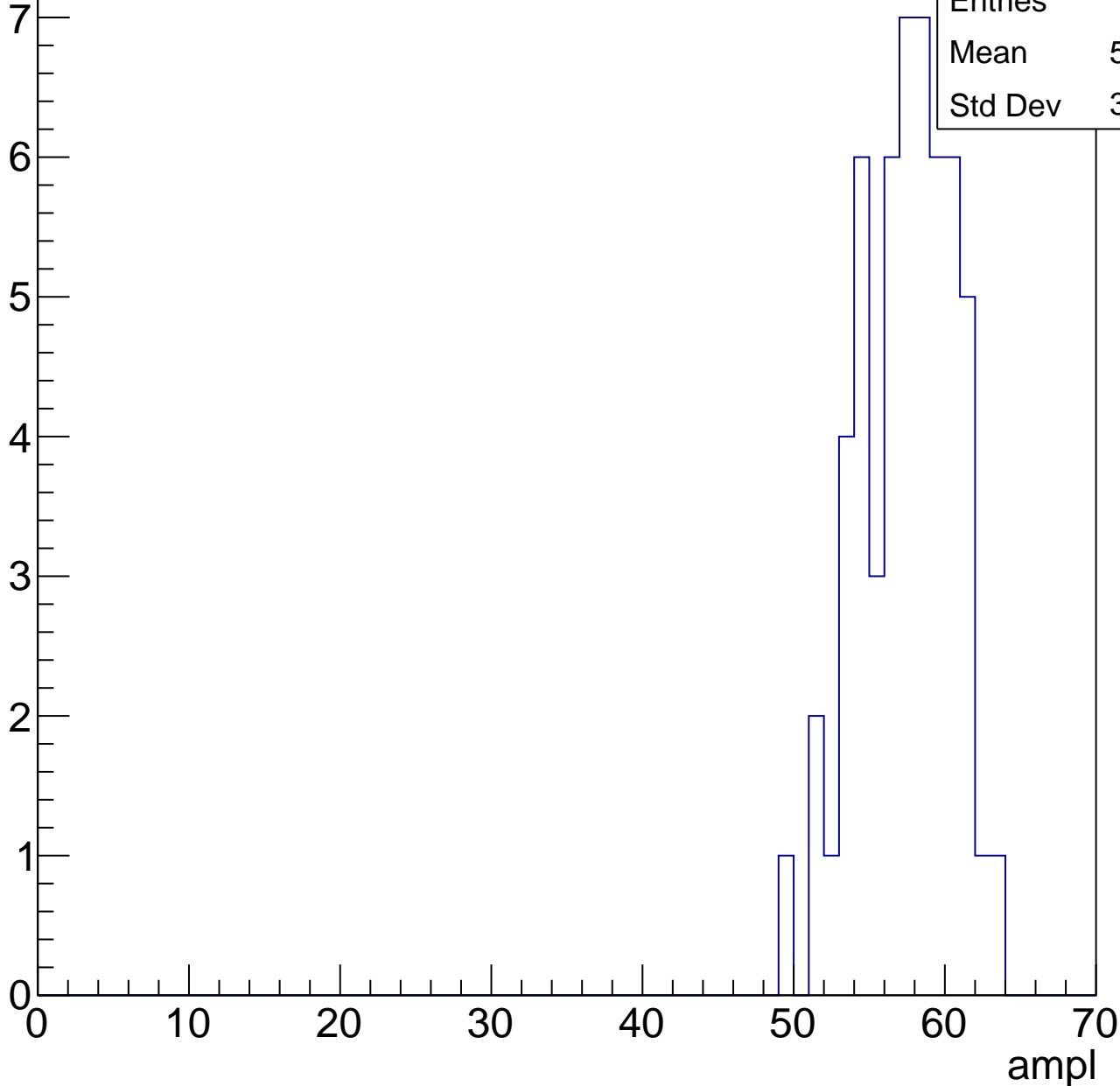


# B1L101S, U19-ch17, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	56
Mean	56.95
Std Dev	3.056

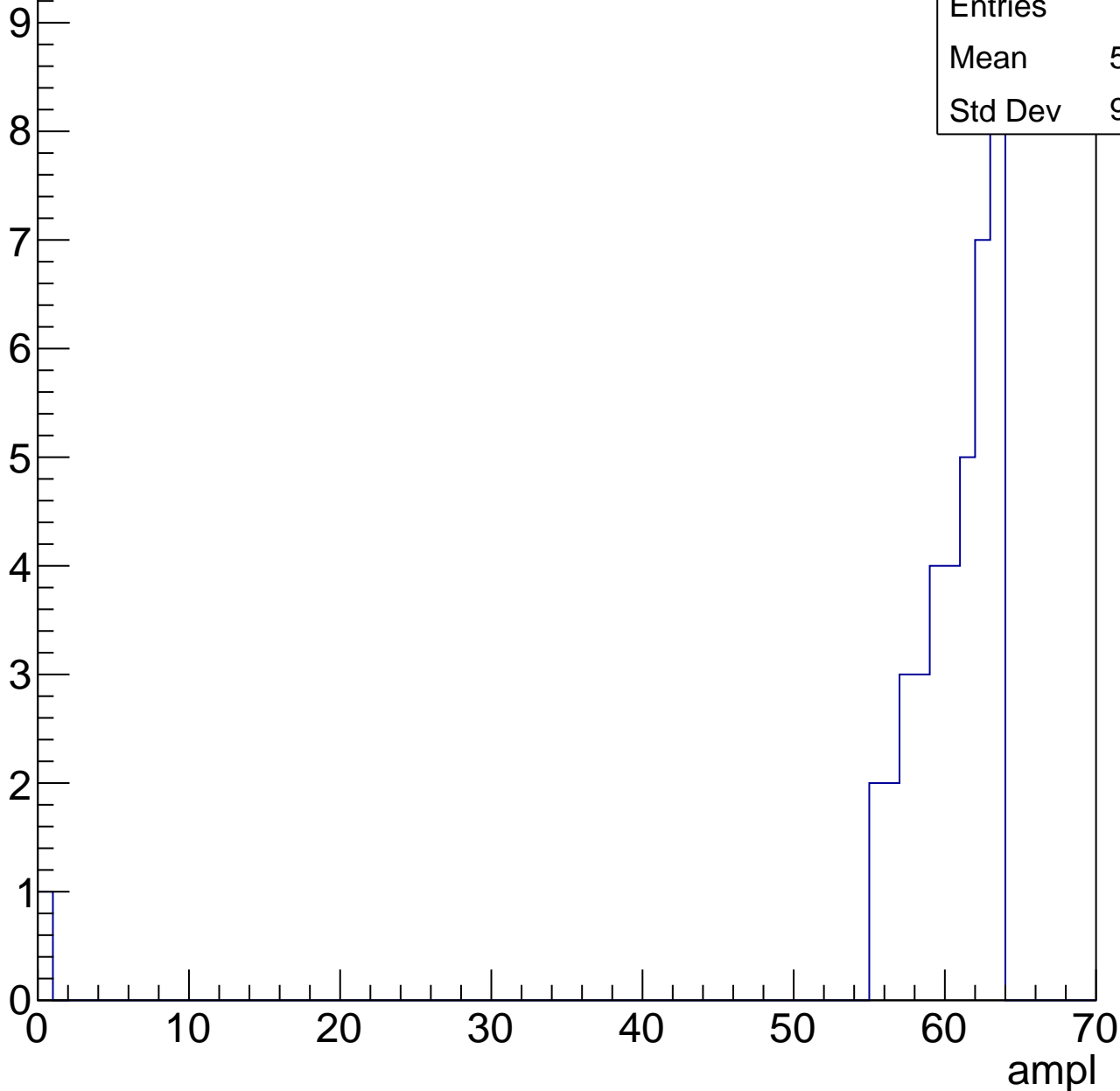


# B1L101S, U19-ch17, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	40
Mean	58.73
Std Dev	9.713



# B1L101S, U19-ch17, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

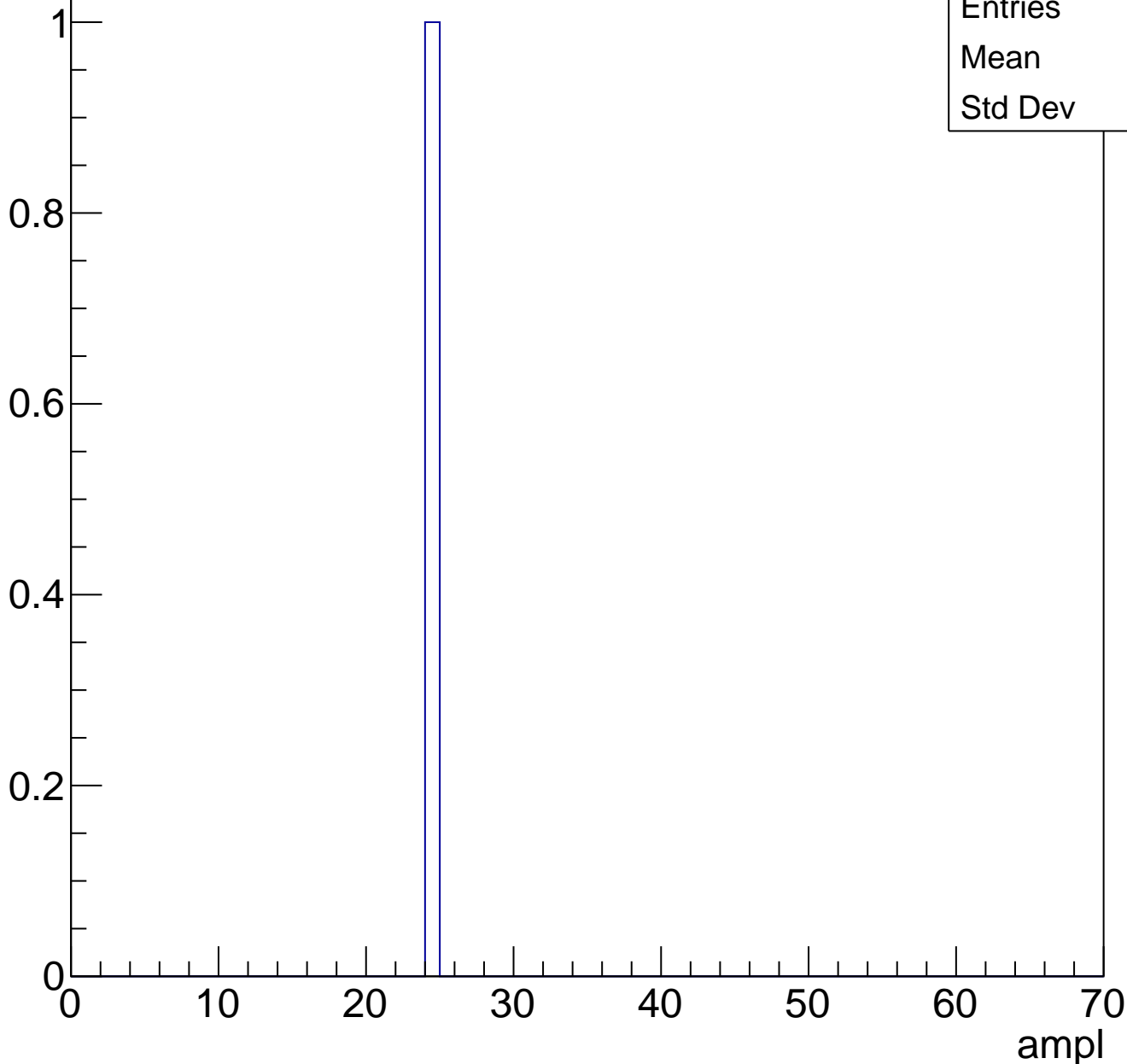




# B1L101S, U19-ch17, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U19-ch18, adc0

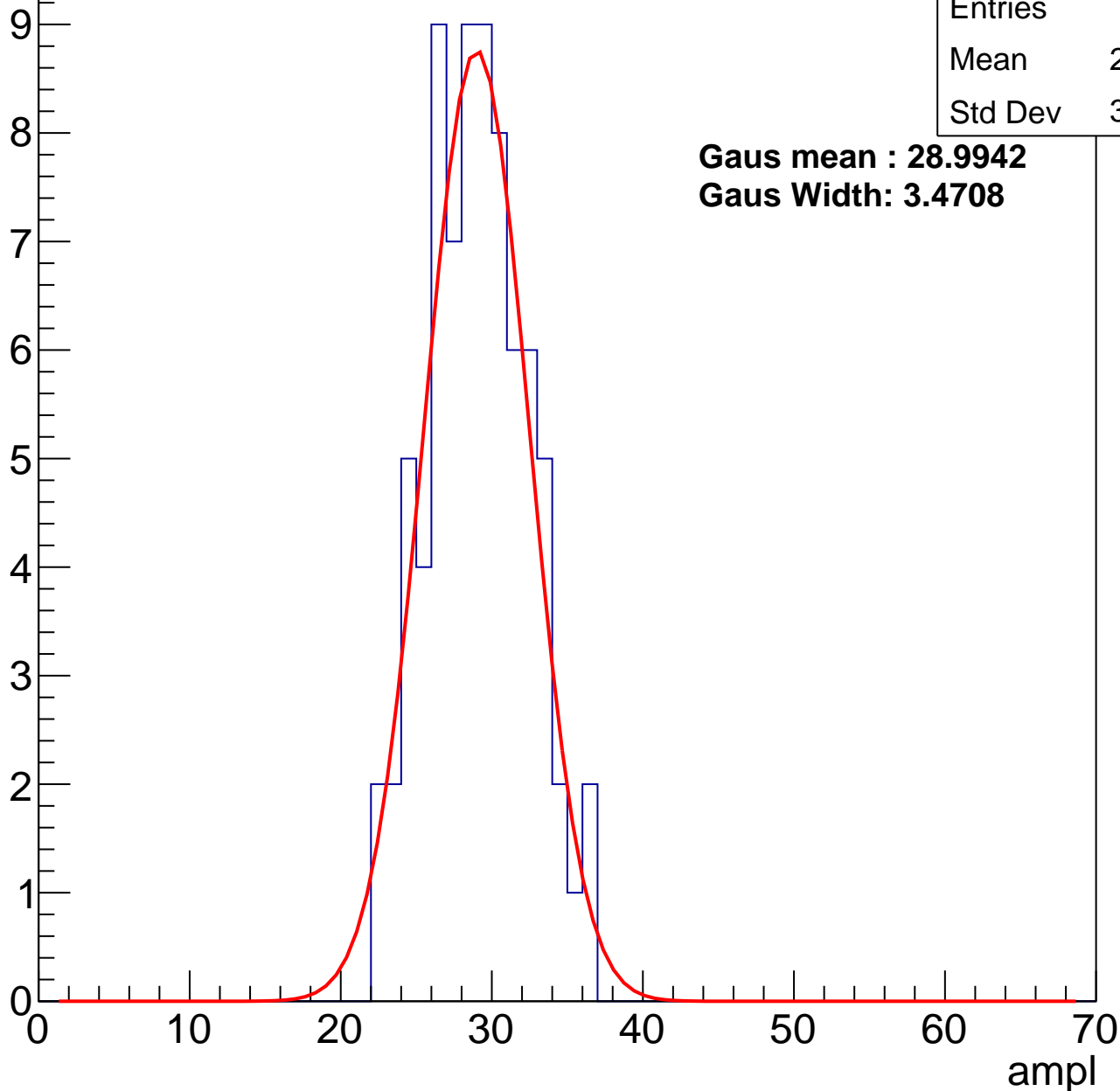
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	77
Mean	28.62
Std Dev	3.256

**Gaus mean : 28.9942**

**Gaus Width: 3.4708**



# B1L101S, U19-ch18, adc1

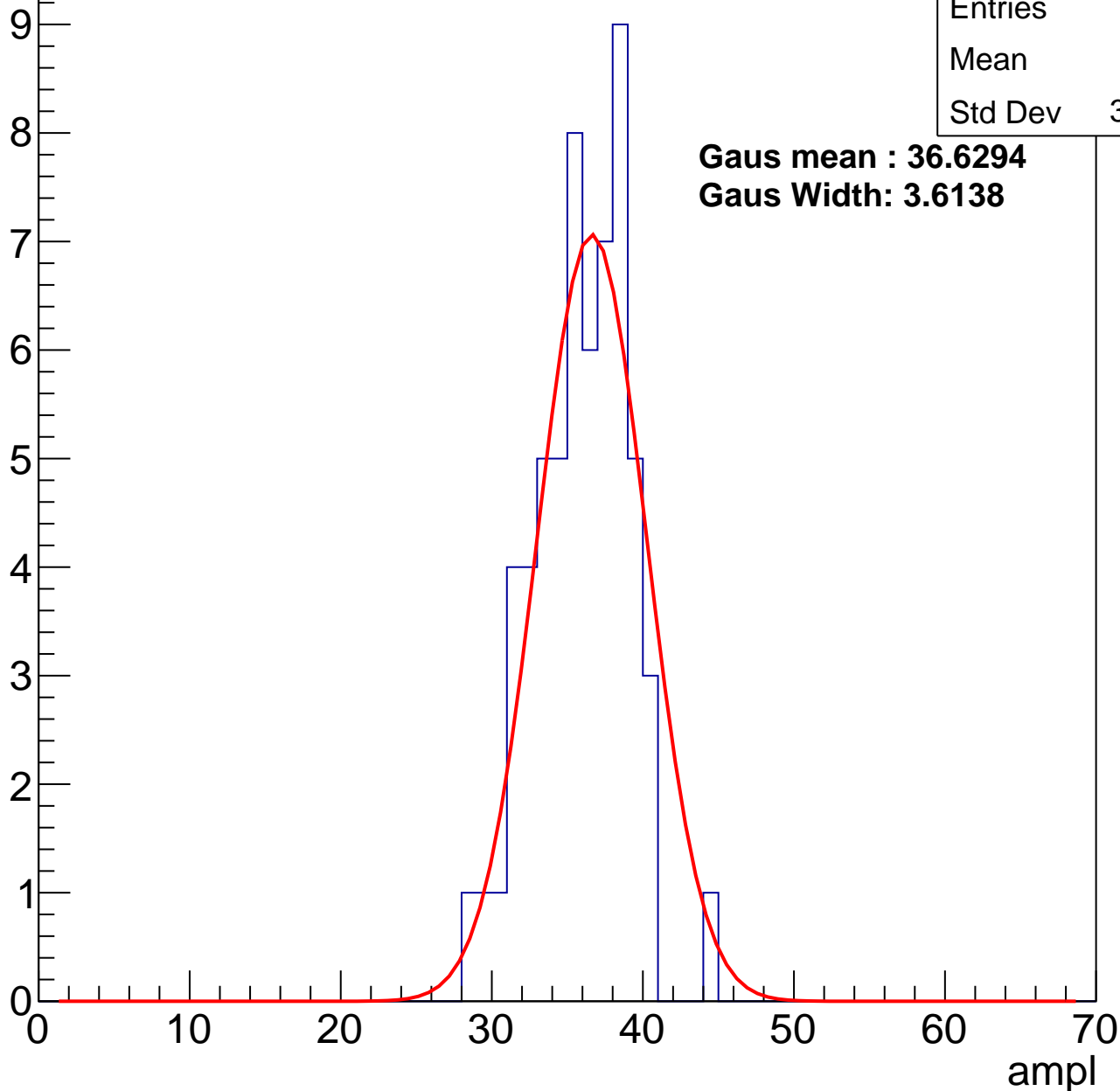
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	60
Mean	35.5
Std Dev	3.085

**Gaus mean : 36.6294**

**Gaus Width: 3.6138**



# B1L101S, U19-ch18, adc2

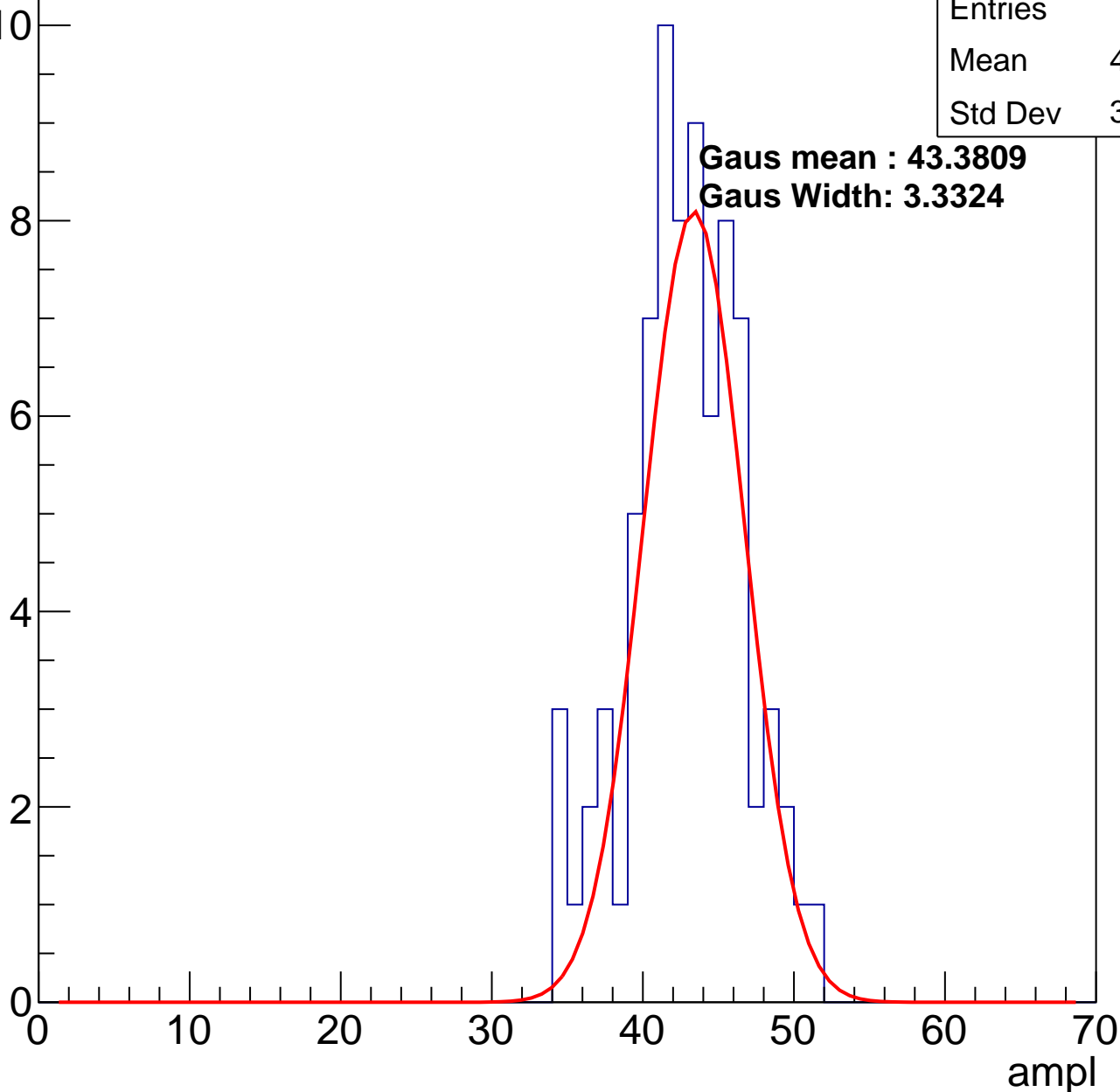
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	79
Mean	42.39
Std Dev	3.719

**Gaus mean : 43.3809**

**Gaus Width: 3.3324**

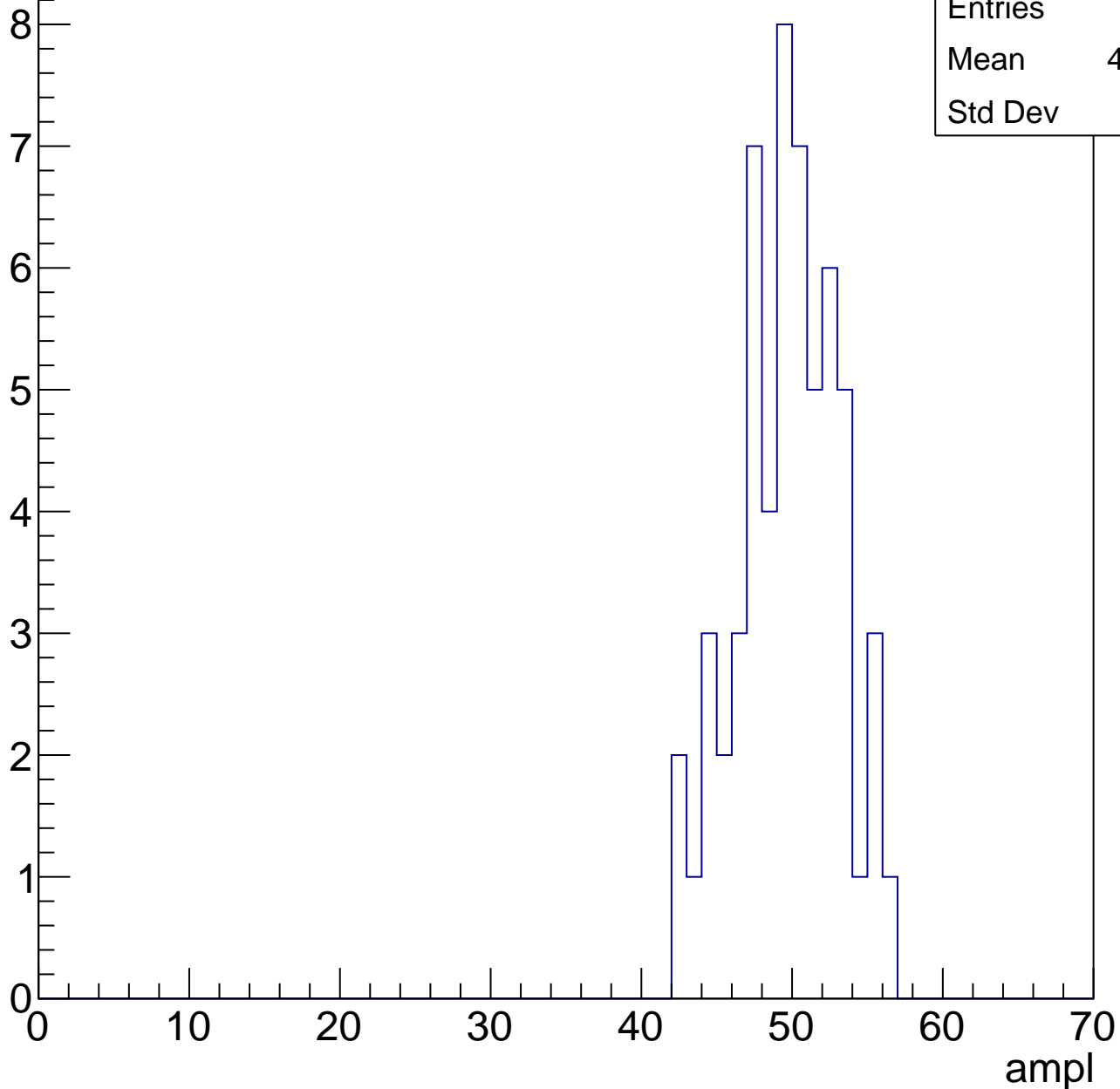


# B1L101S, U19-ch18, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	58
Mean	49.26
Std Dev	3.32

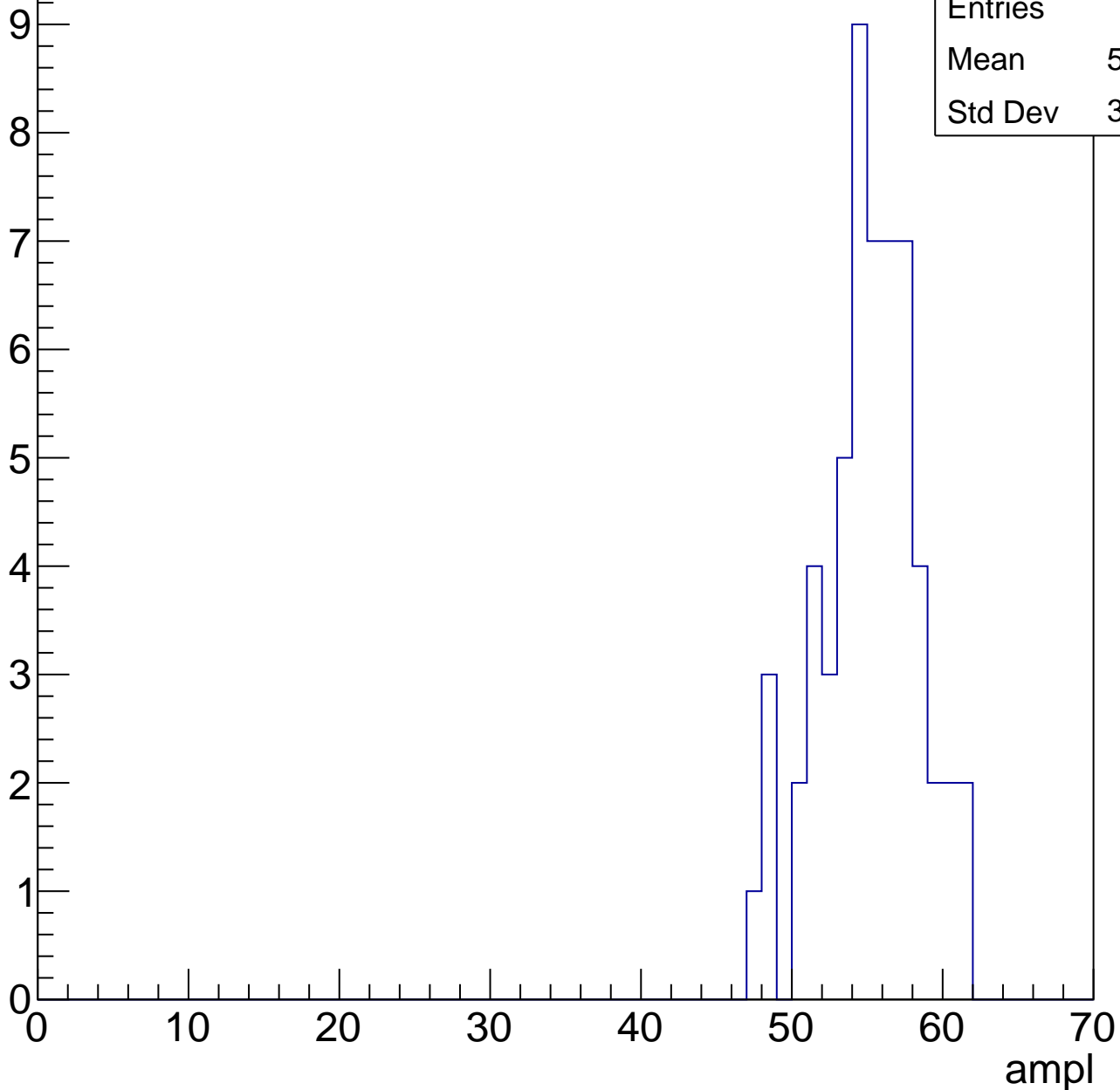


# B1L101S, U19-ch18, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

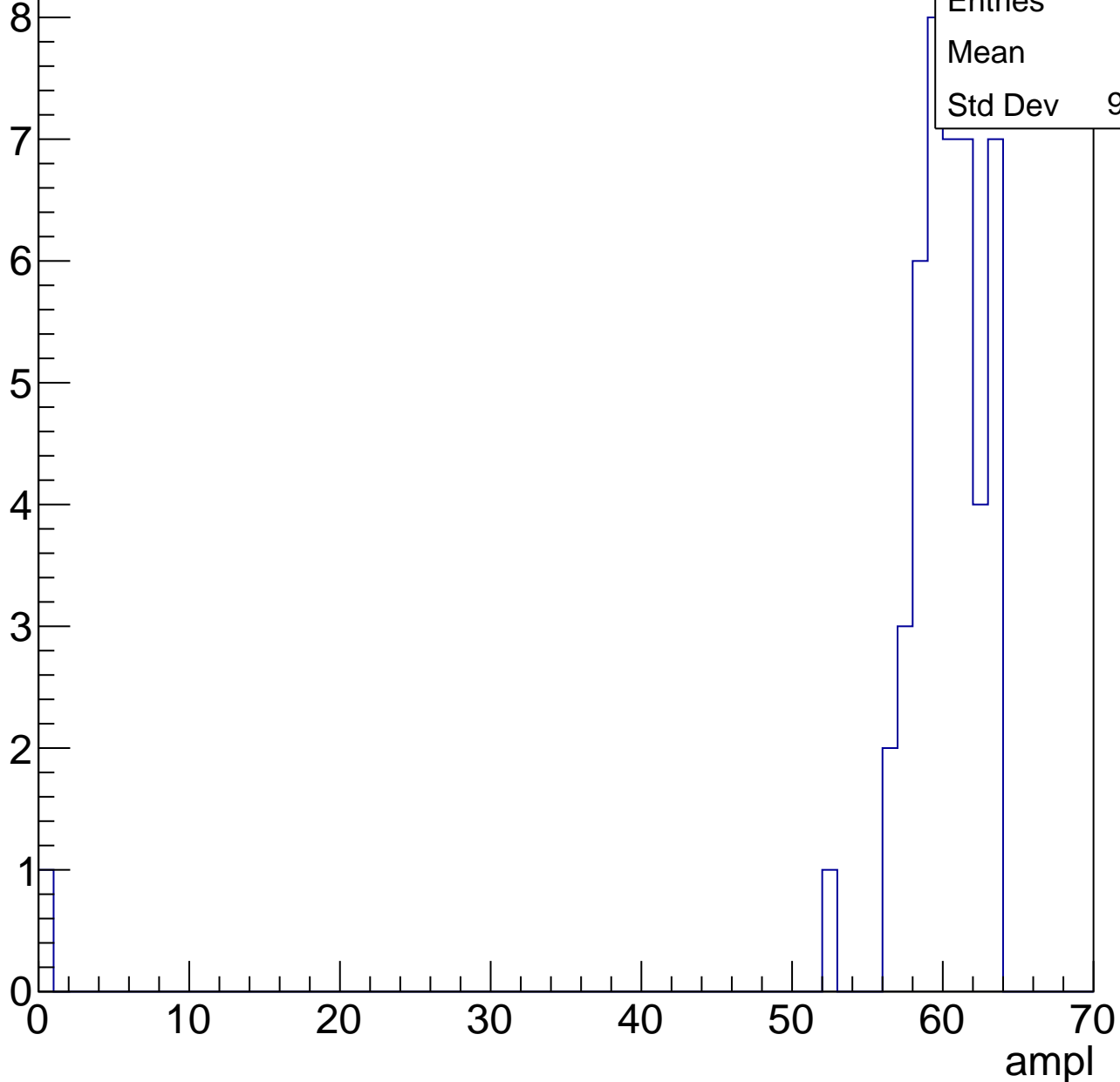
Entries	58
Mean	54.66
Std Dev	3.214



# B1L101S, U19-ch18, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



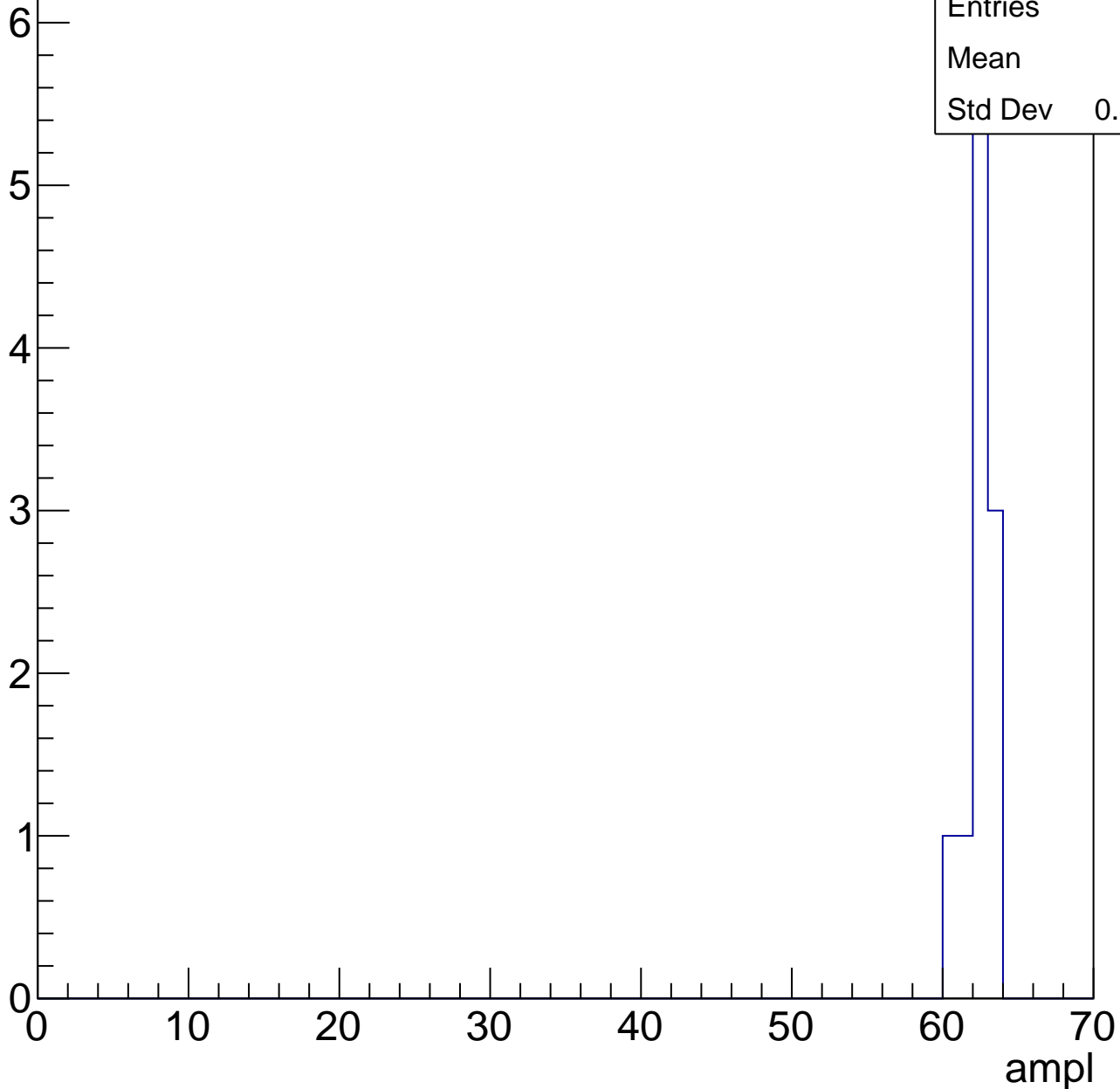
Entries	46
Mean	58.5
Std Dev	9.014

# B1L101S, U19-ch18, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	11
Mean	62
Std Dev	0.8528





# B1L101S, U19-ch18, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	3
Mean	6
Std Dev	8.485

# B1L101S, U19-ch19, adc0

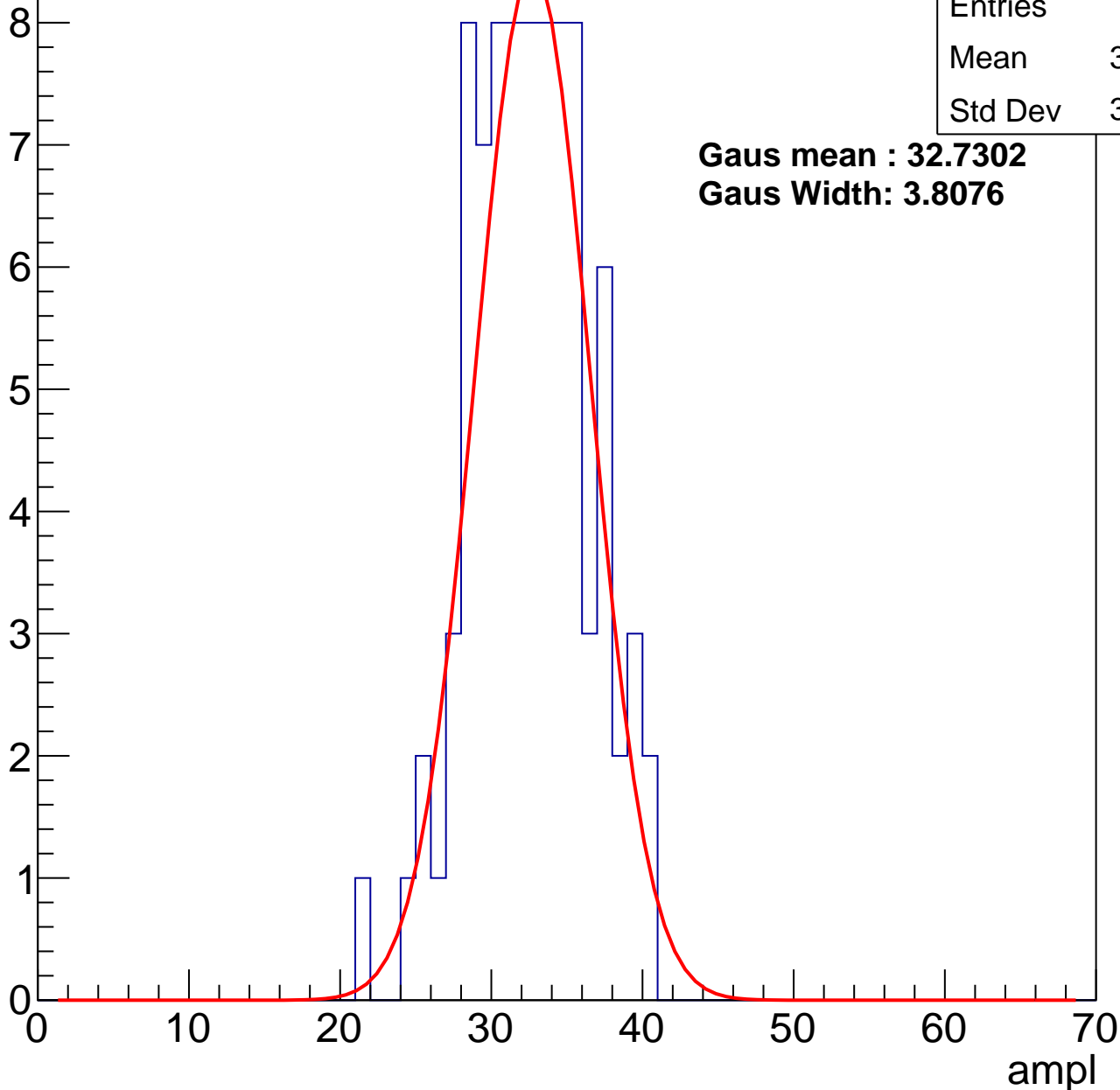
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	87
Mean	32.09
Std Dev	3.838

**Gaus mean : 32.7302**

**Gaus Width: 3.8076**



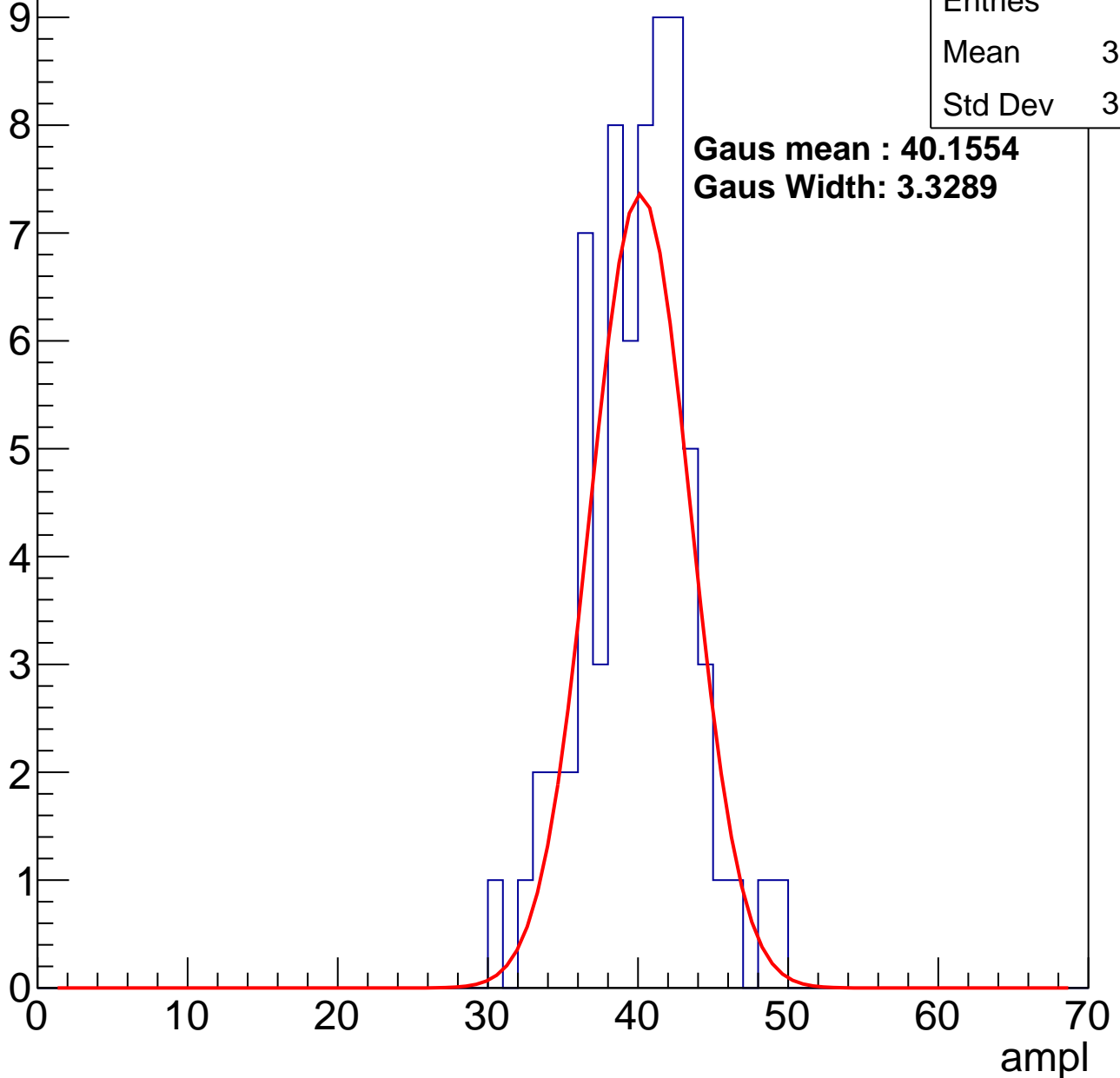
# B1L101S, U19-ch19, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	39.56
Std Dev	3.568

**Gaus mean : 40.1554**  
**Gaus Width: 3.3289**



# B1L101S, U19-ch19, adc2

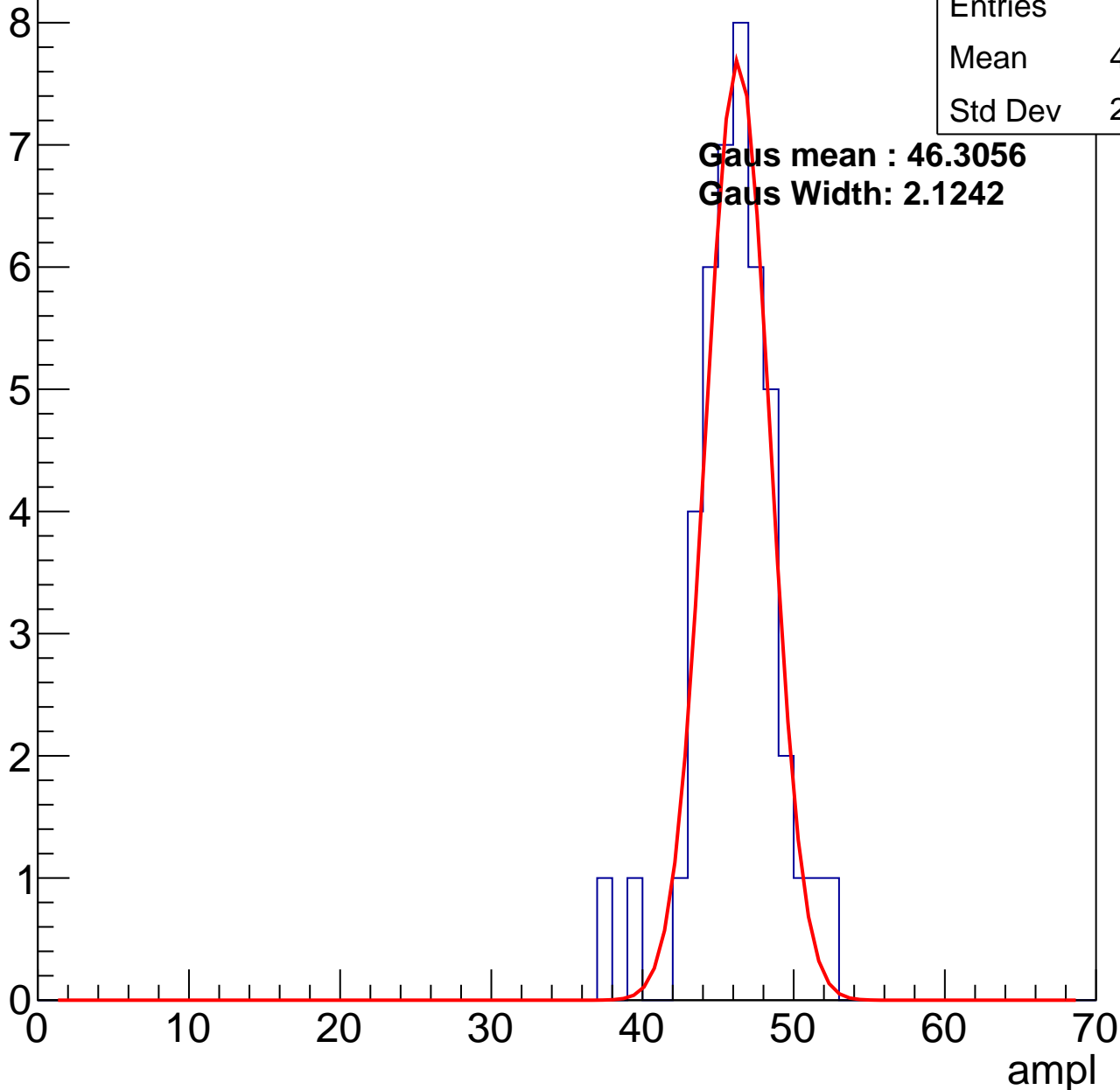
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	44
Mean	45.68
Std Dev	2.737

**Gaus mean : 46.3056**

**Gaus Width: 2.1242**

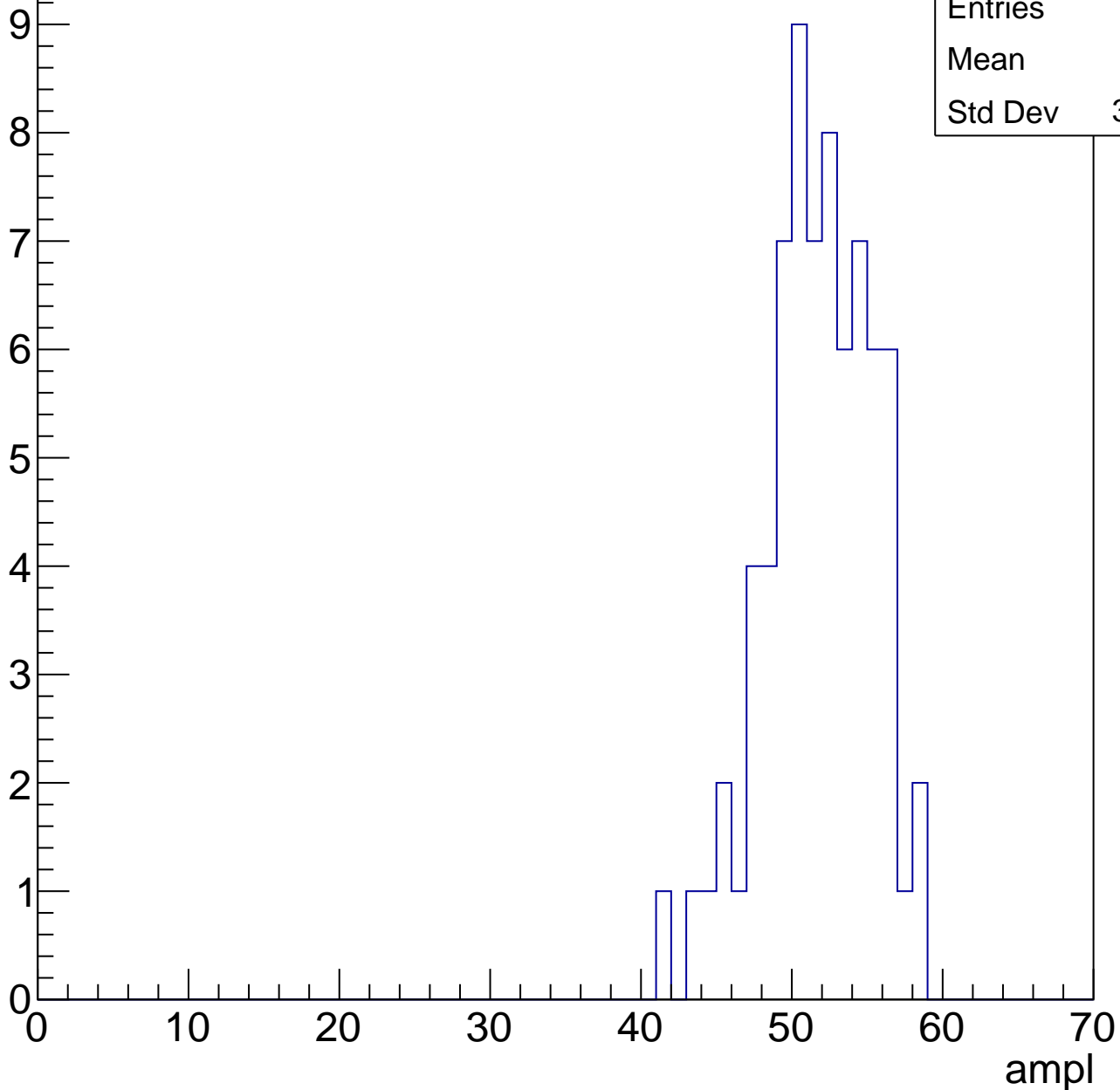


# B1L101S, U19-ch19, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	73
Mean	51.3
Std Dev	3.541

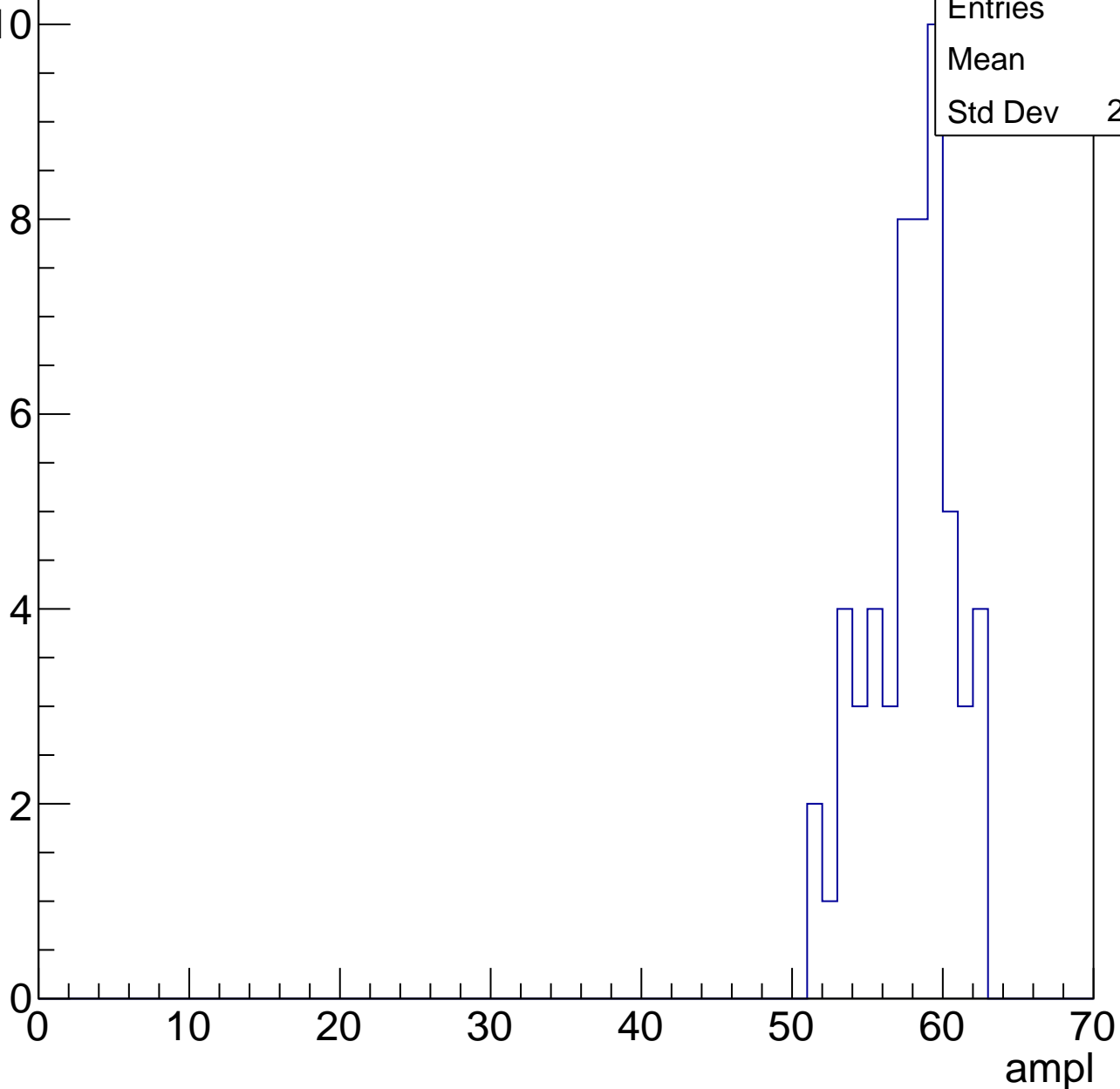


# B1L101S, U19-ch19, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	55
Mean	57.4
Std Dev	2.826

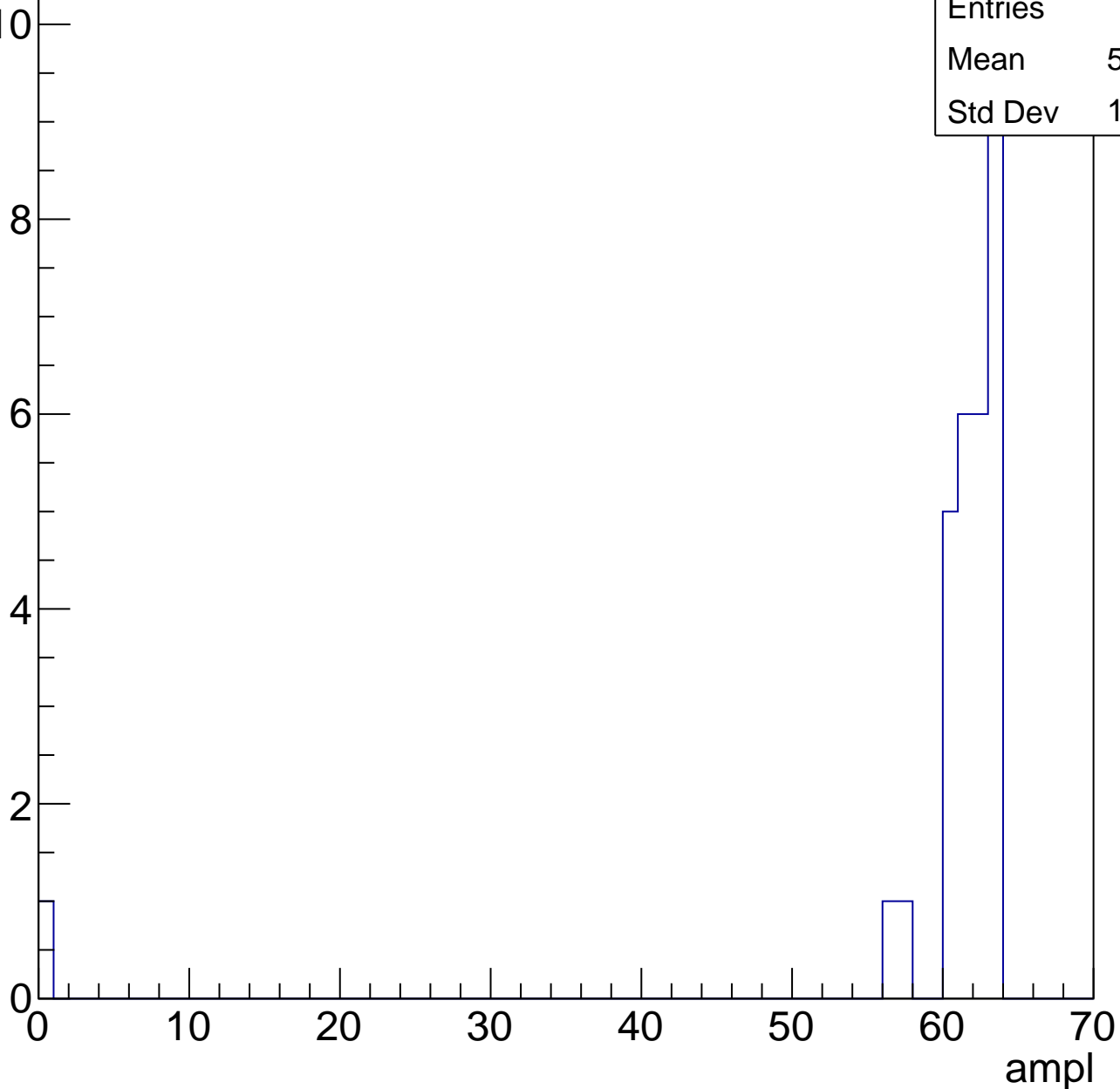


# B1L101S, U19-ch19, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	30
Mean	59.37
Std Dev	11.15



# B1L101S, U19-ch19, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	61
Std Dev	0



# B1L101S, U19-ch19, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U19-ch20, adc0

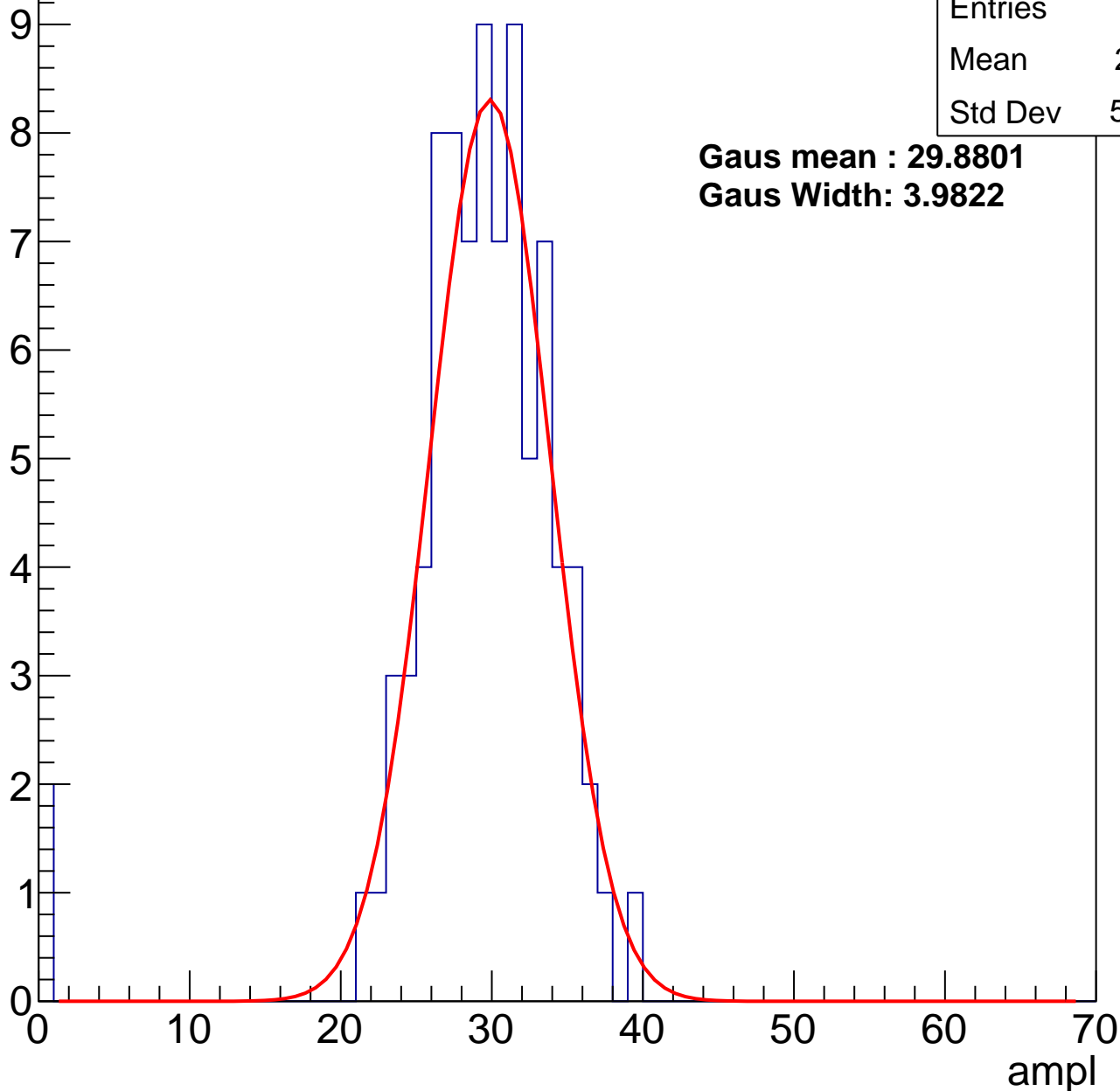
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	86
Mean	28.71
Std Dev	5.758

**Gaus mean : 29.8801**

**Gaus Width: 3.9822**



# B1L101S, U19-ch20, adc1

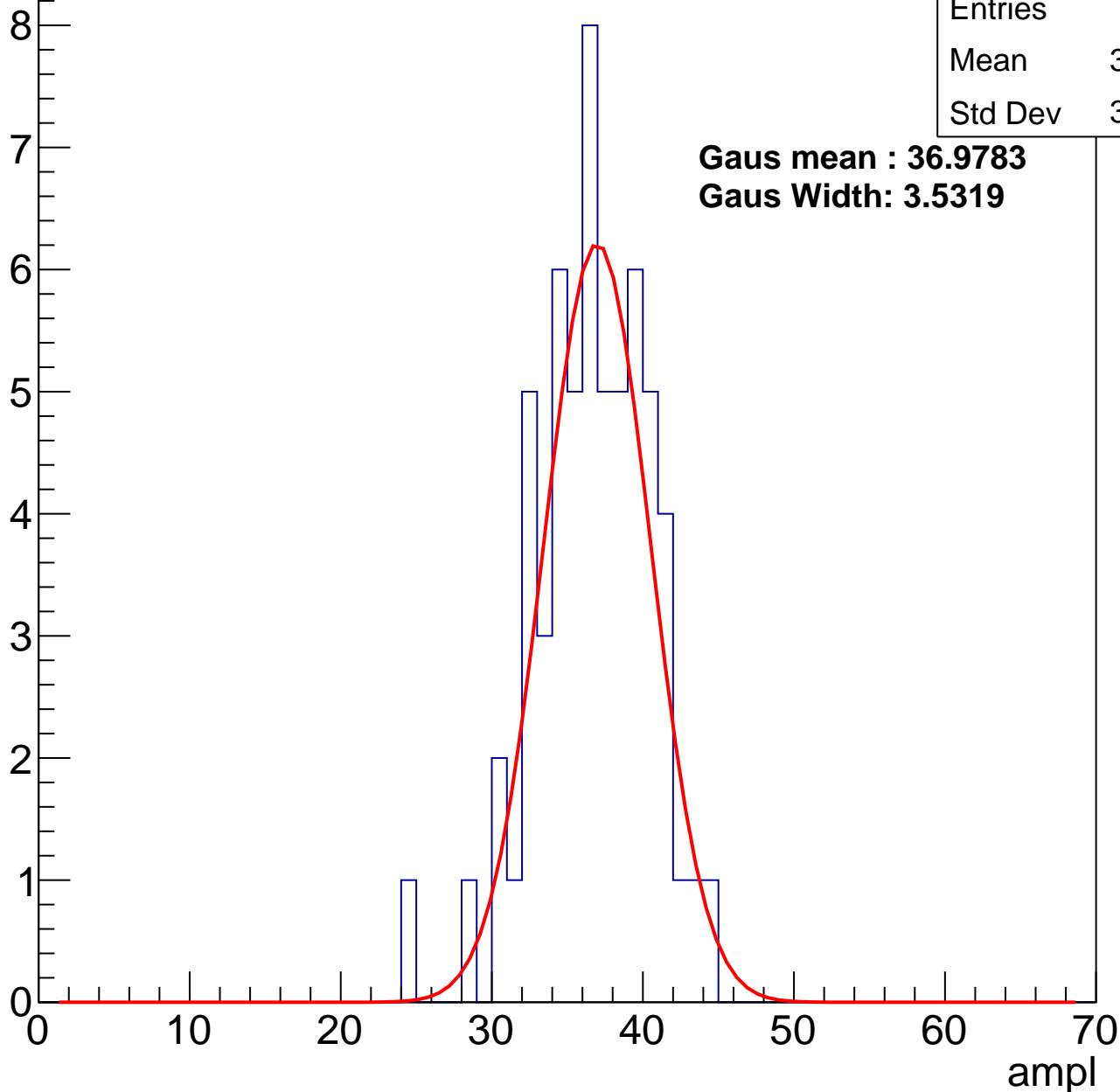
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	60
Mean	36.18
Std Dev	3.757

**Gaus mean : 36.9783**

**Gaus Width: 3.5319**



# B1L101S, U19-ch20, adc2

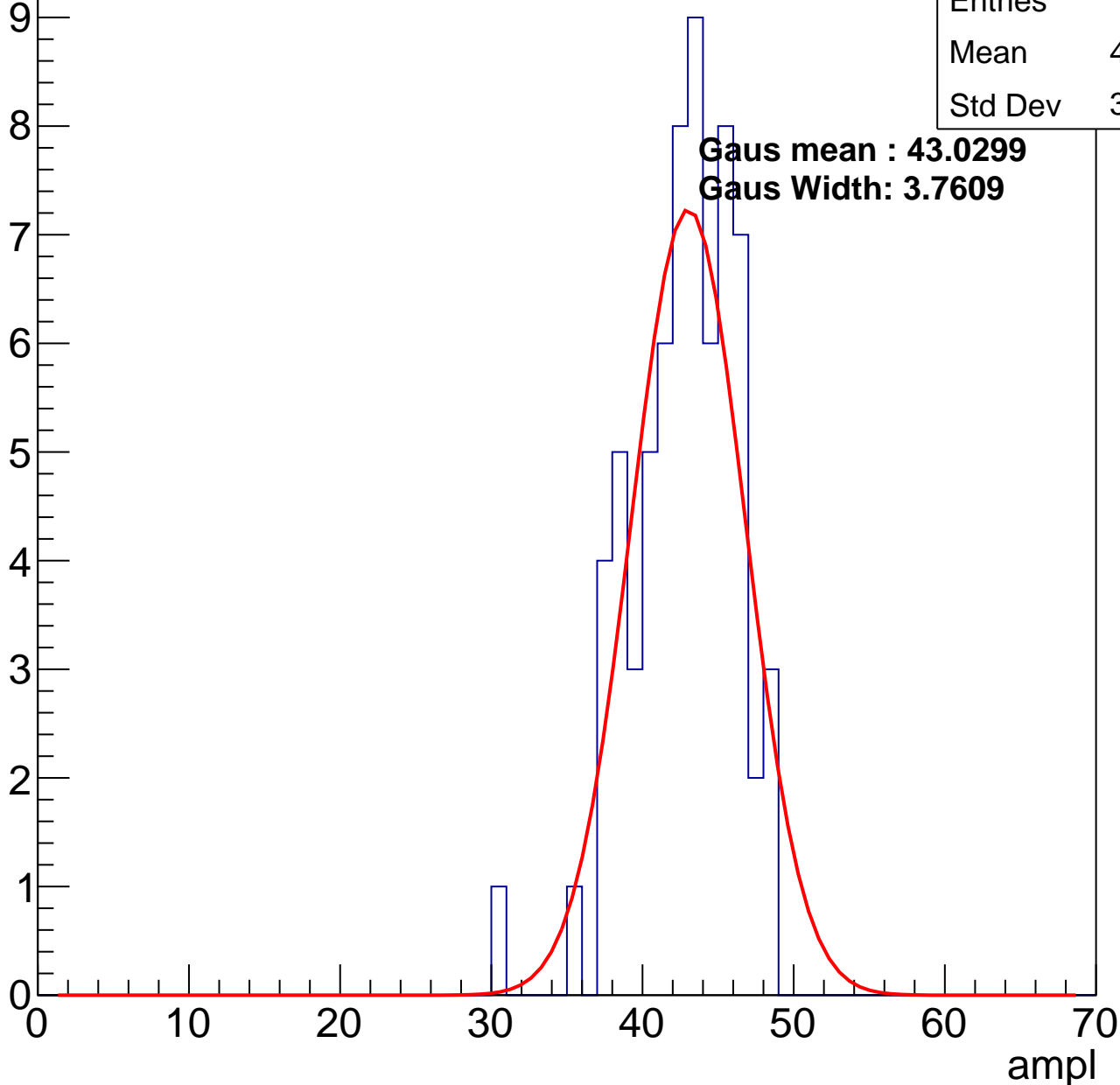
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	42.25
Std Dev	3.423

**Gaus mean : 43.0299**

**Gaus Width: 3.7609**

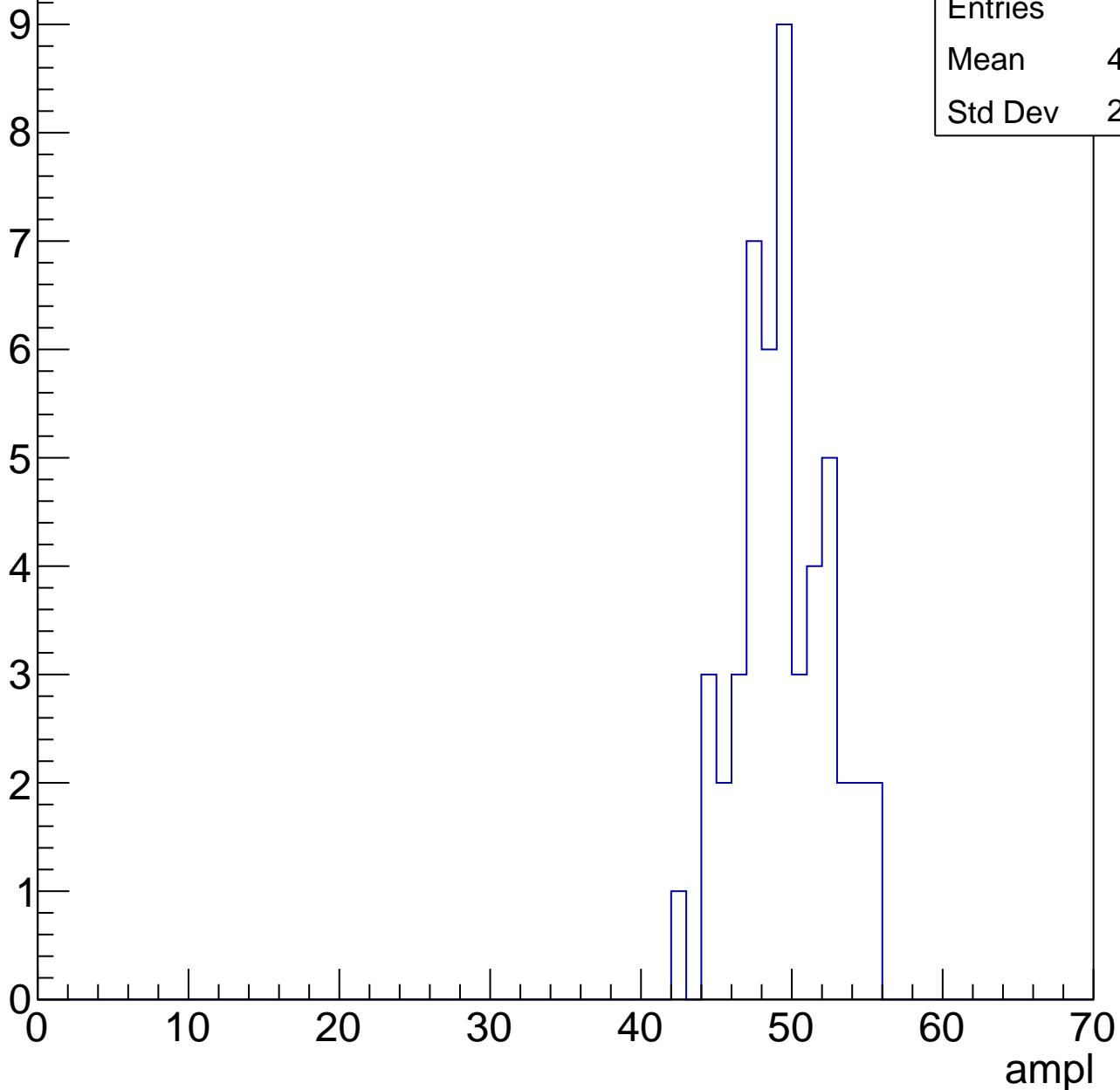


# B1L101S, U19-ch20, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	49
Mean	48.94
Std Dev	2.979

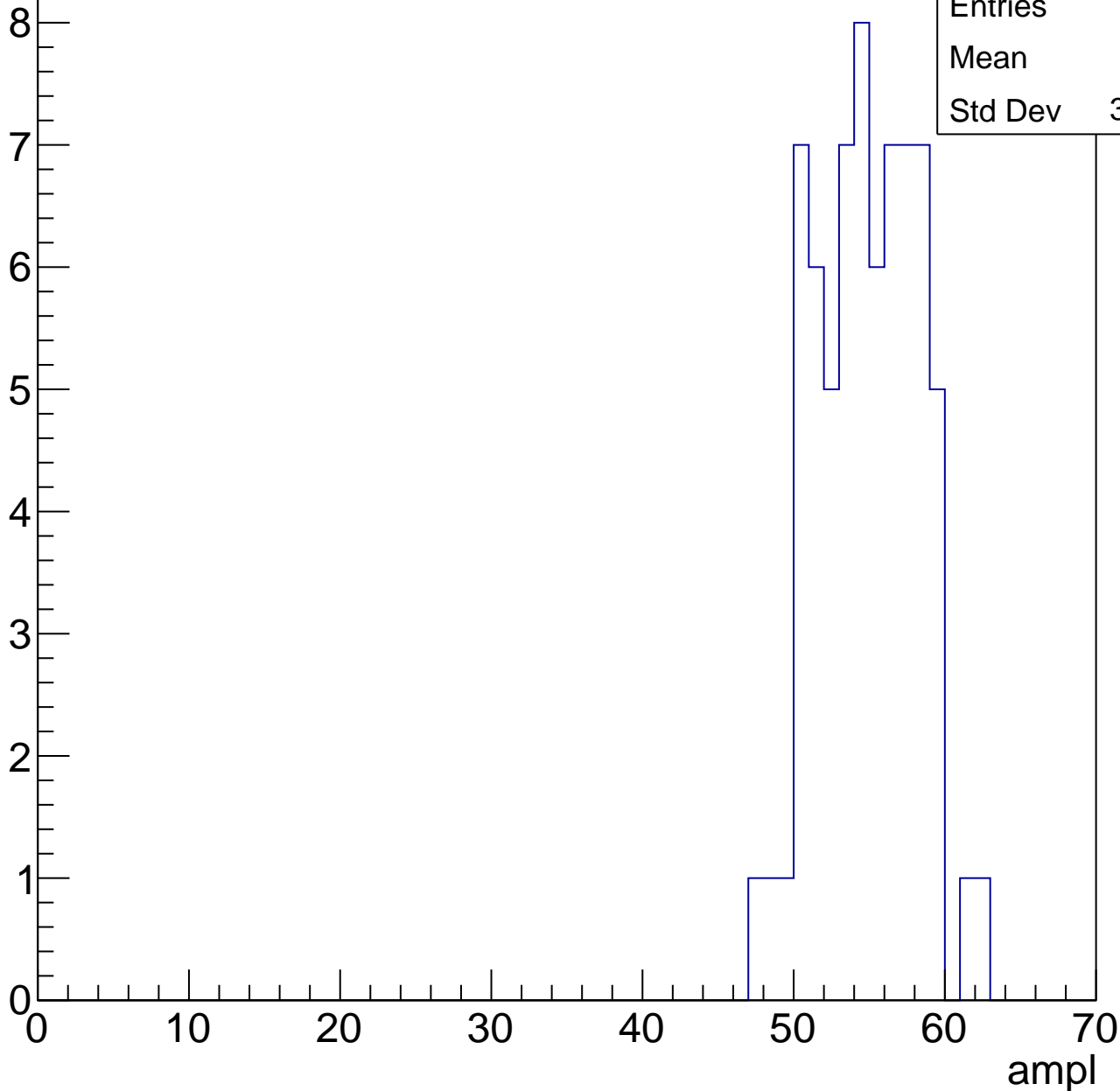


# B1L101S, U19-ch20, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

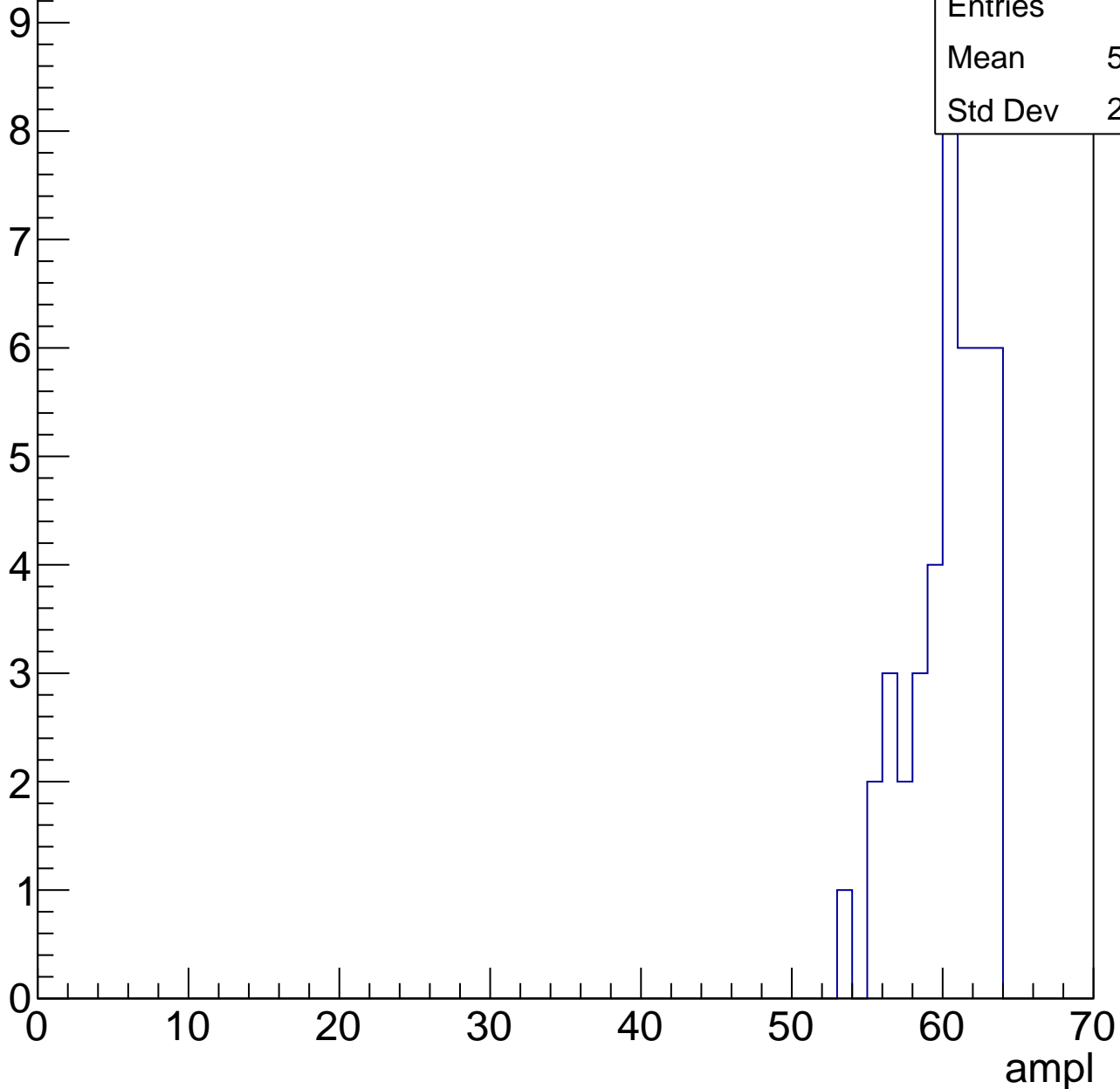
Entries	70
Mean	54.4
Std Dev	3.249



# B1L101S, U19-ch20, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

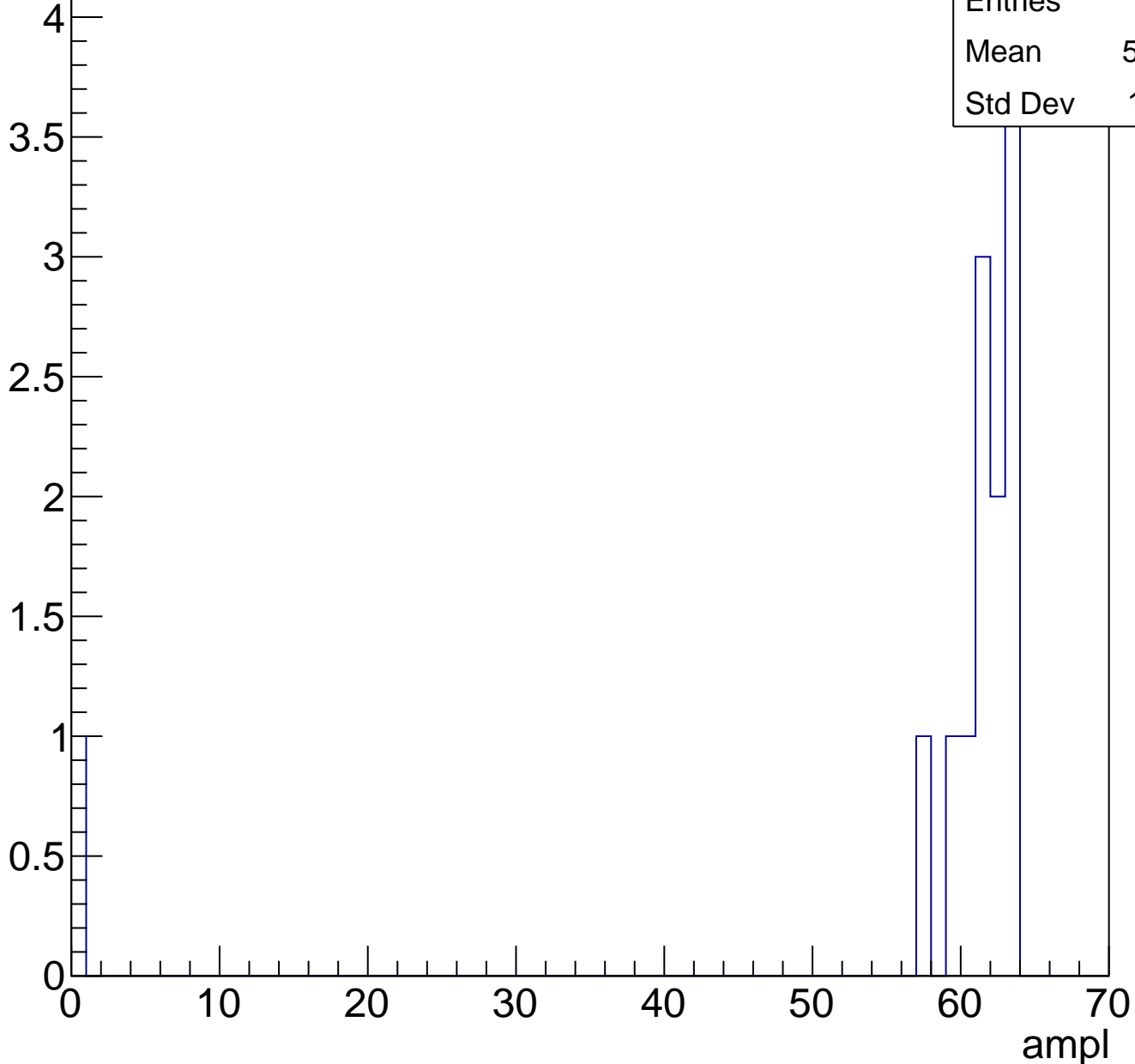
Entry



# B1L101S, U19-ch20, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



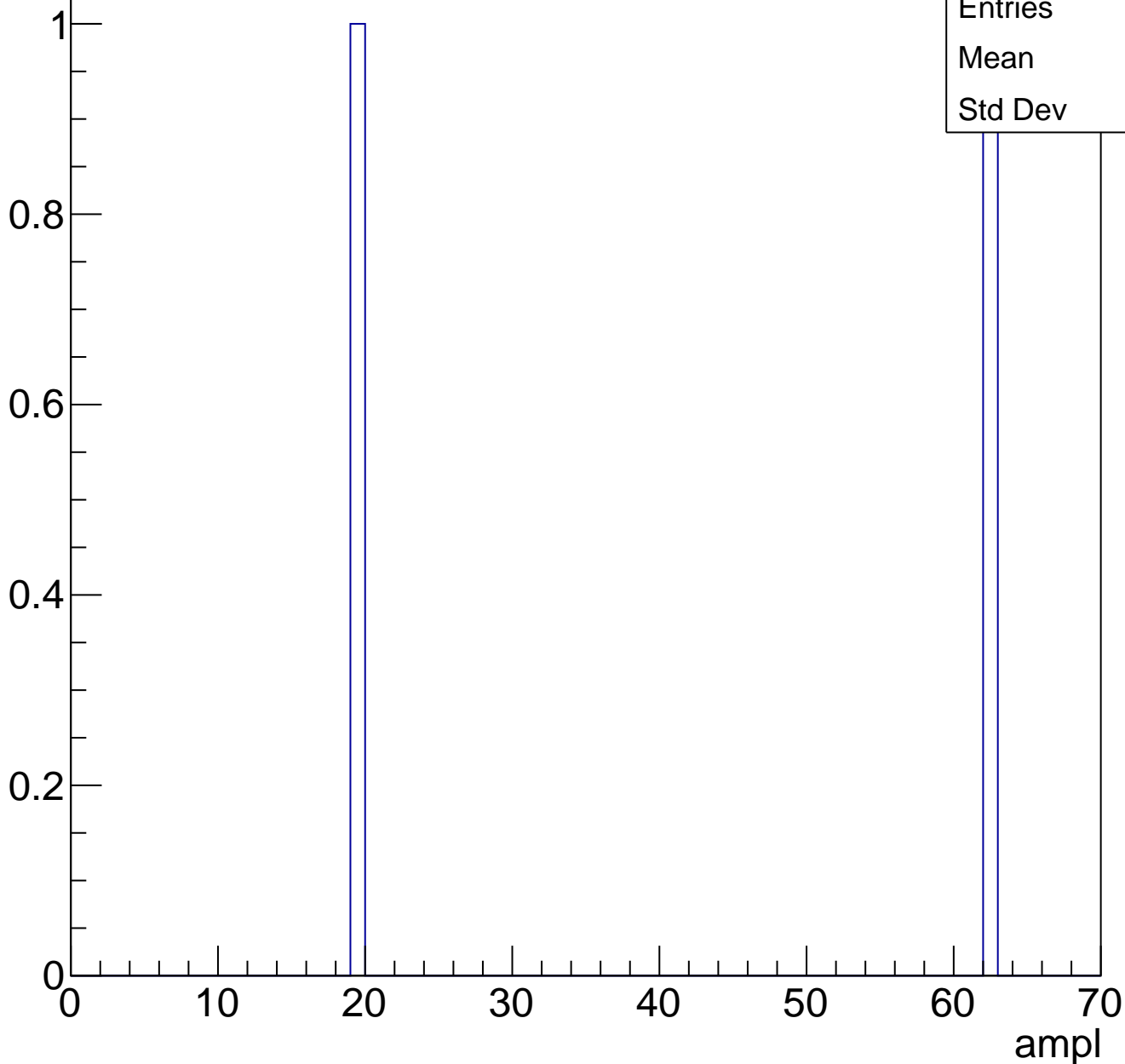
Entries	13
Mean	56.54
Std Dev	16.41



# B1L101S, U19-ch20, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U19-ch21, adc0

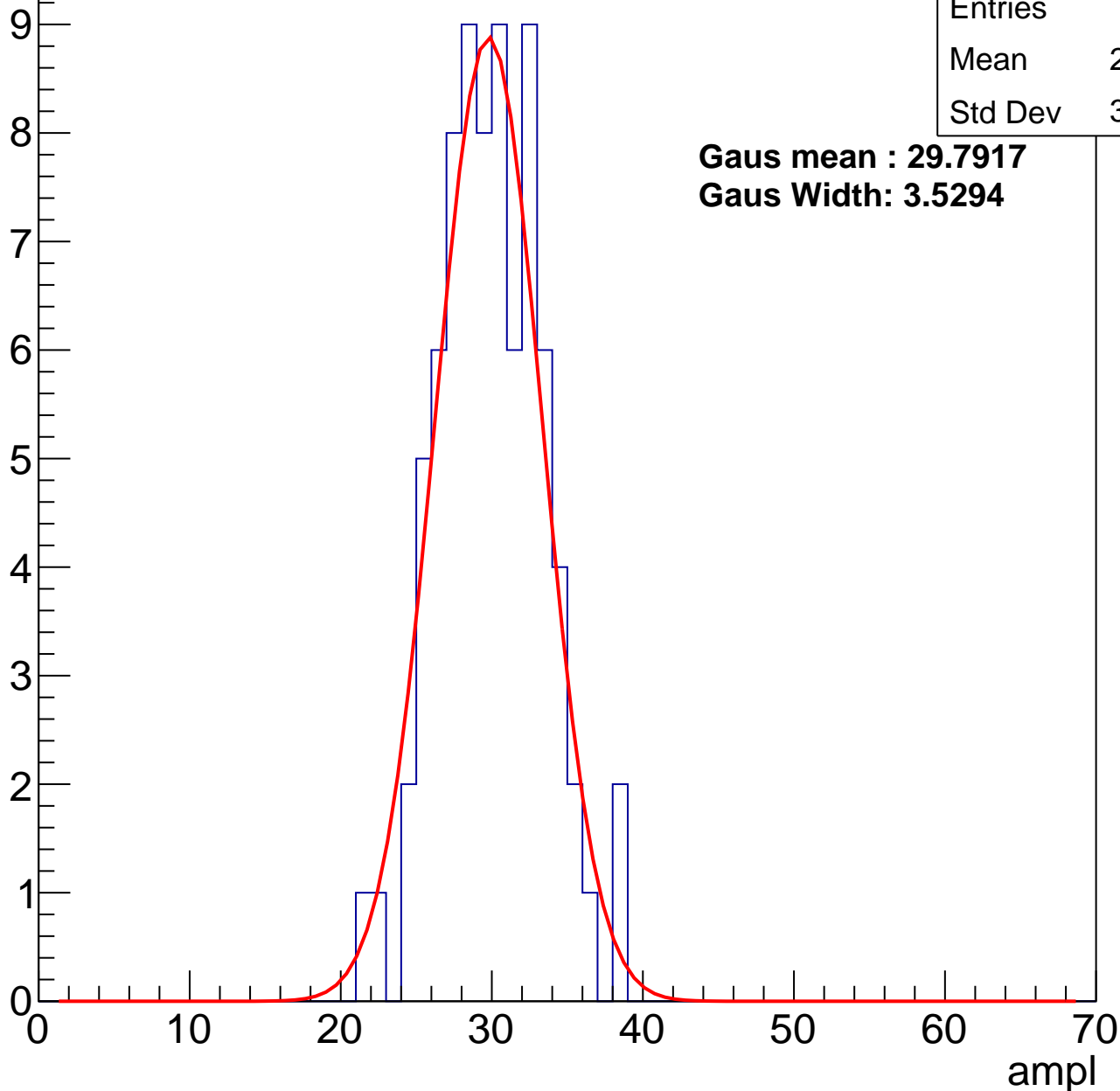
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	79
Mean	29.52
Std Dev	3.393

**Gaus mean : 29.7917**

**Gaus Width: 3.5294**



# B1L101S, U19-ch21, adc1

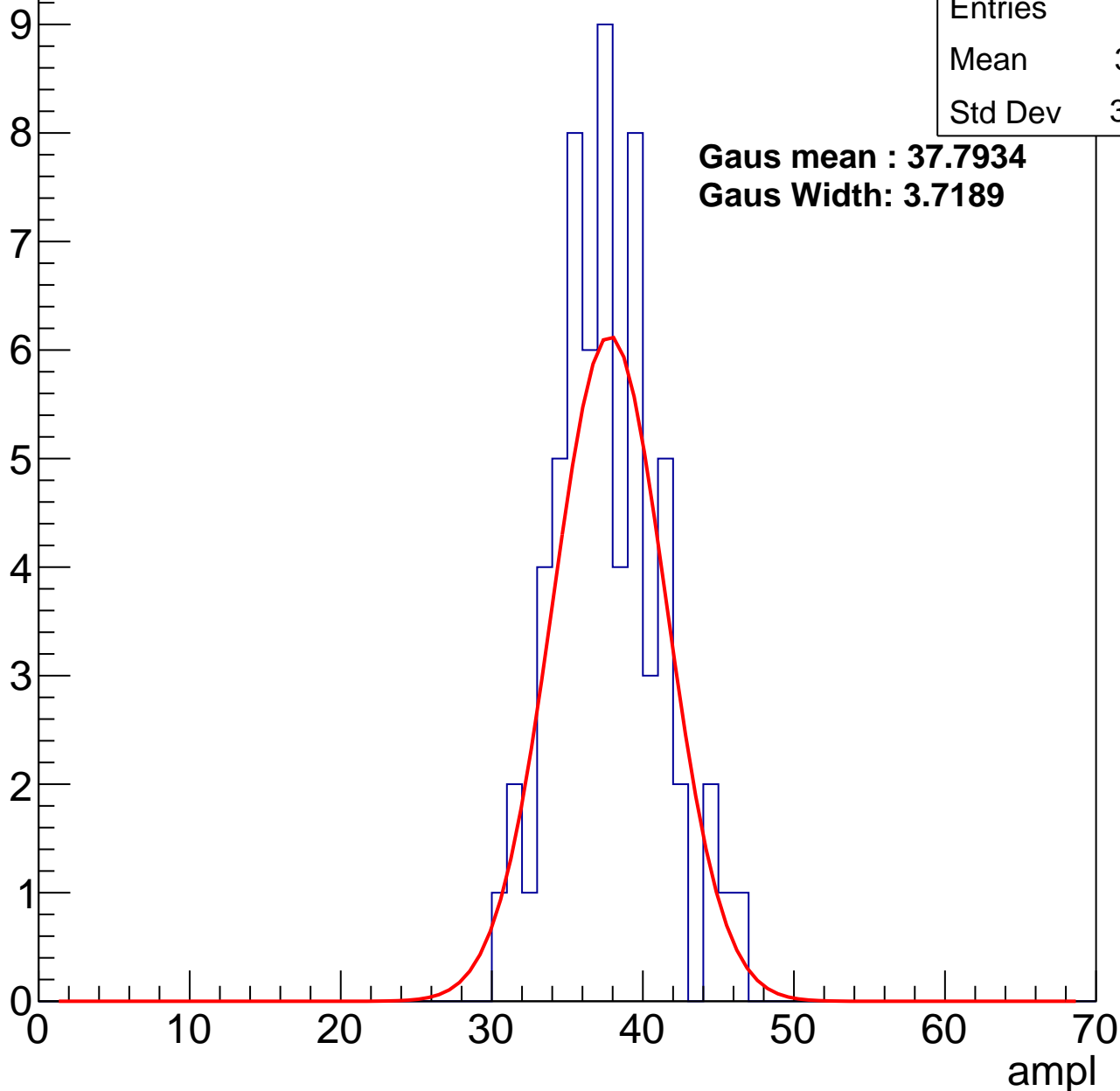
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	37.21
Std Dev	3.423

**Gaus mean : 37.7934**

**Gaus Width: 3.7189**



# B1L101S, U19-ch21, adc2

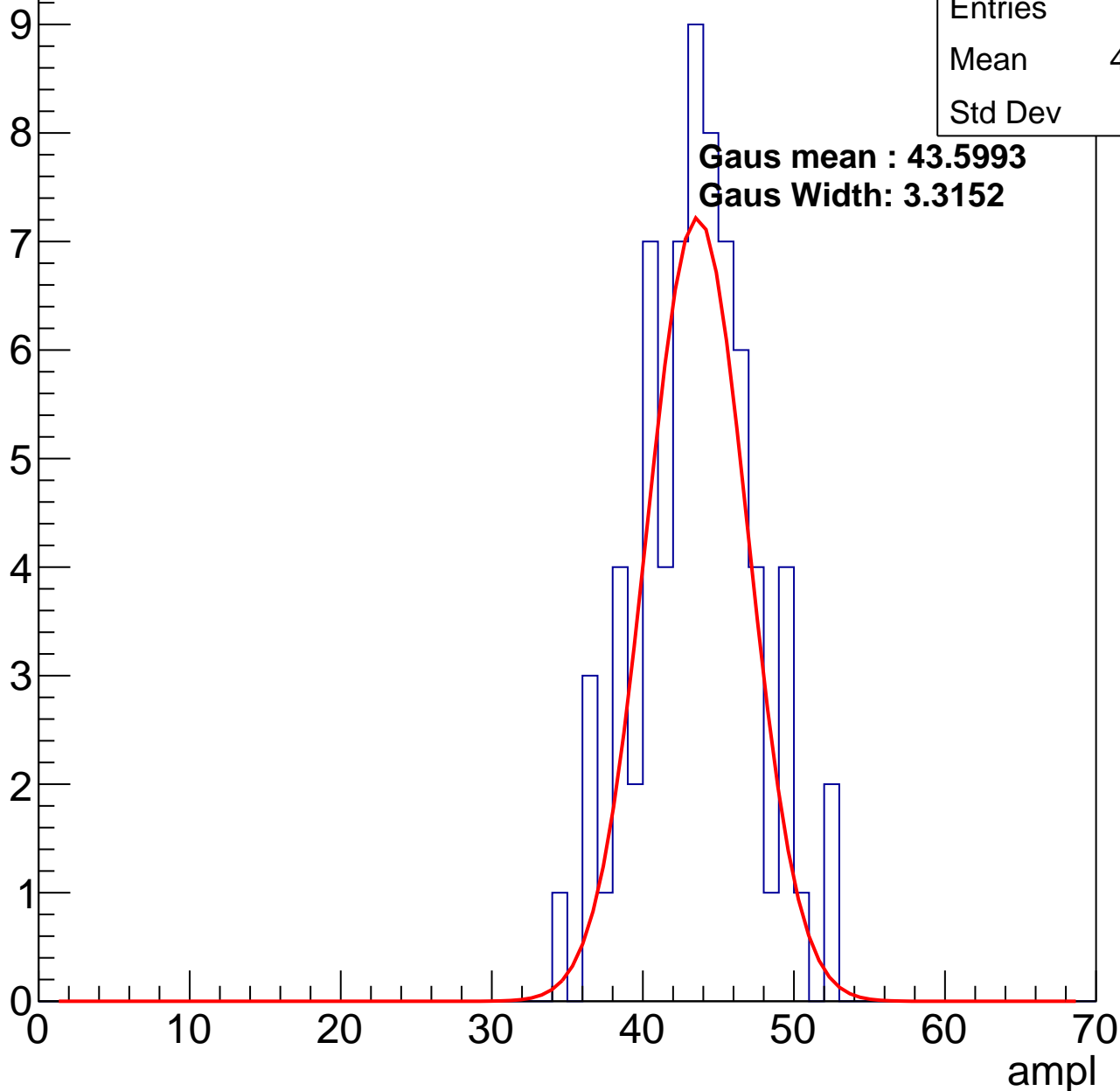
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	71
Mean	43.14
Std Dev	3.78

**Gaus mean : 43.5993**

**Gaus Width: 3.3152**

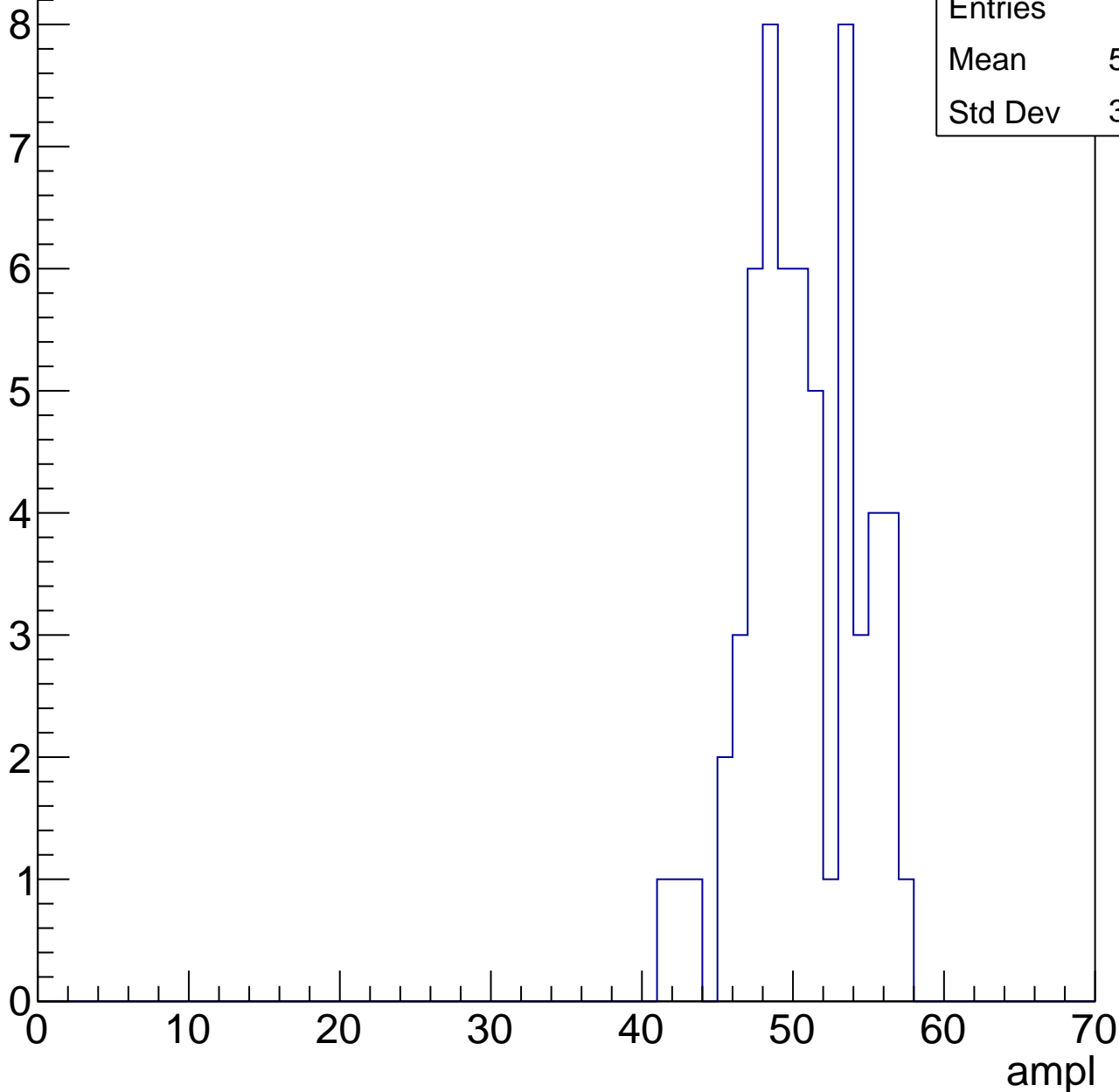


# B1L101S, U19-ch21, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	60
Mean	50.13
Std Dev	3.663

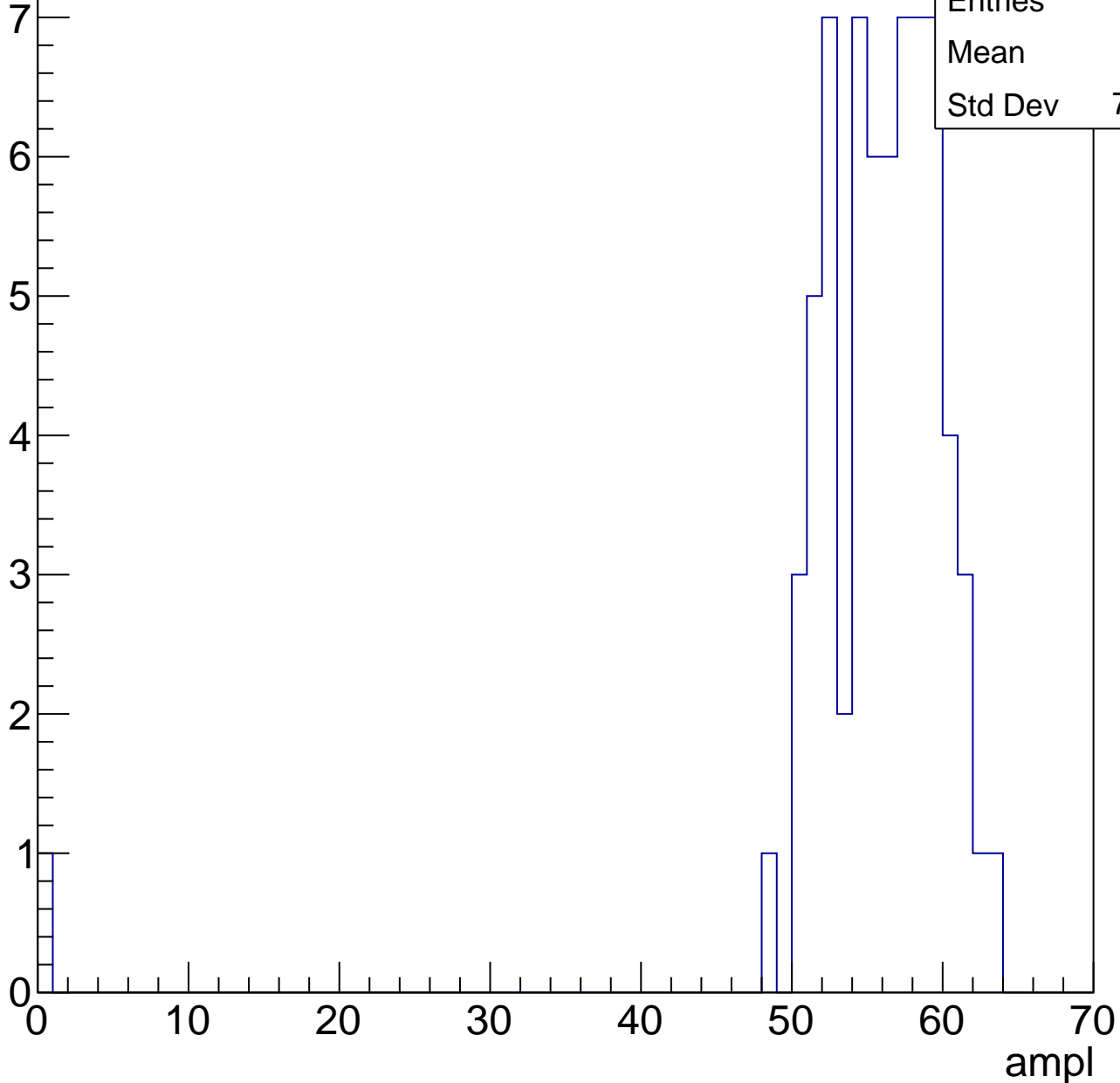


# B1L101S, U19-ch21, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	54.9
Std Dev	7.511



# B1L101S, U19-ch21, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

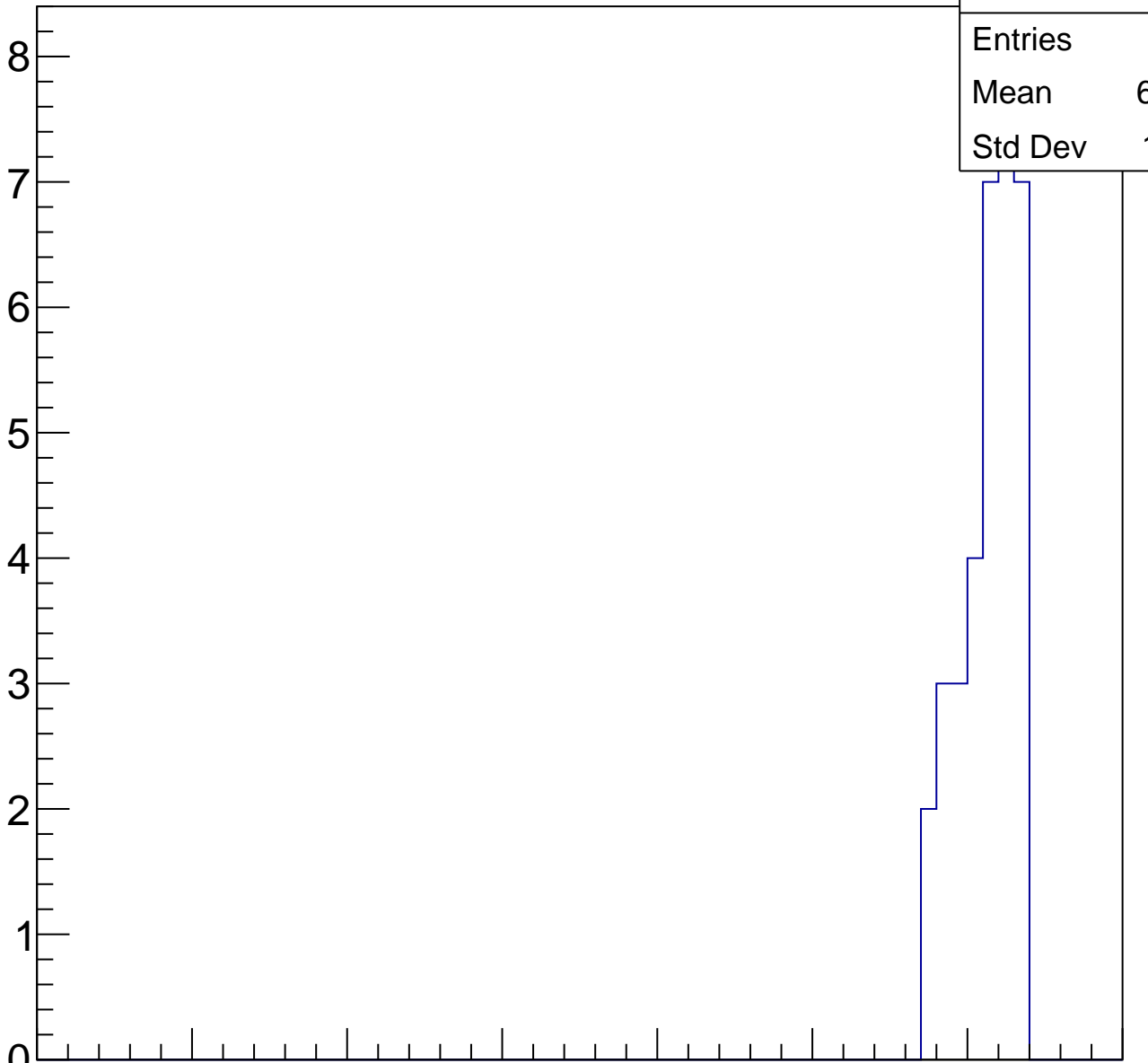
Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	34
Mean	60.85
Std Dev	1.801

ampl

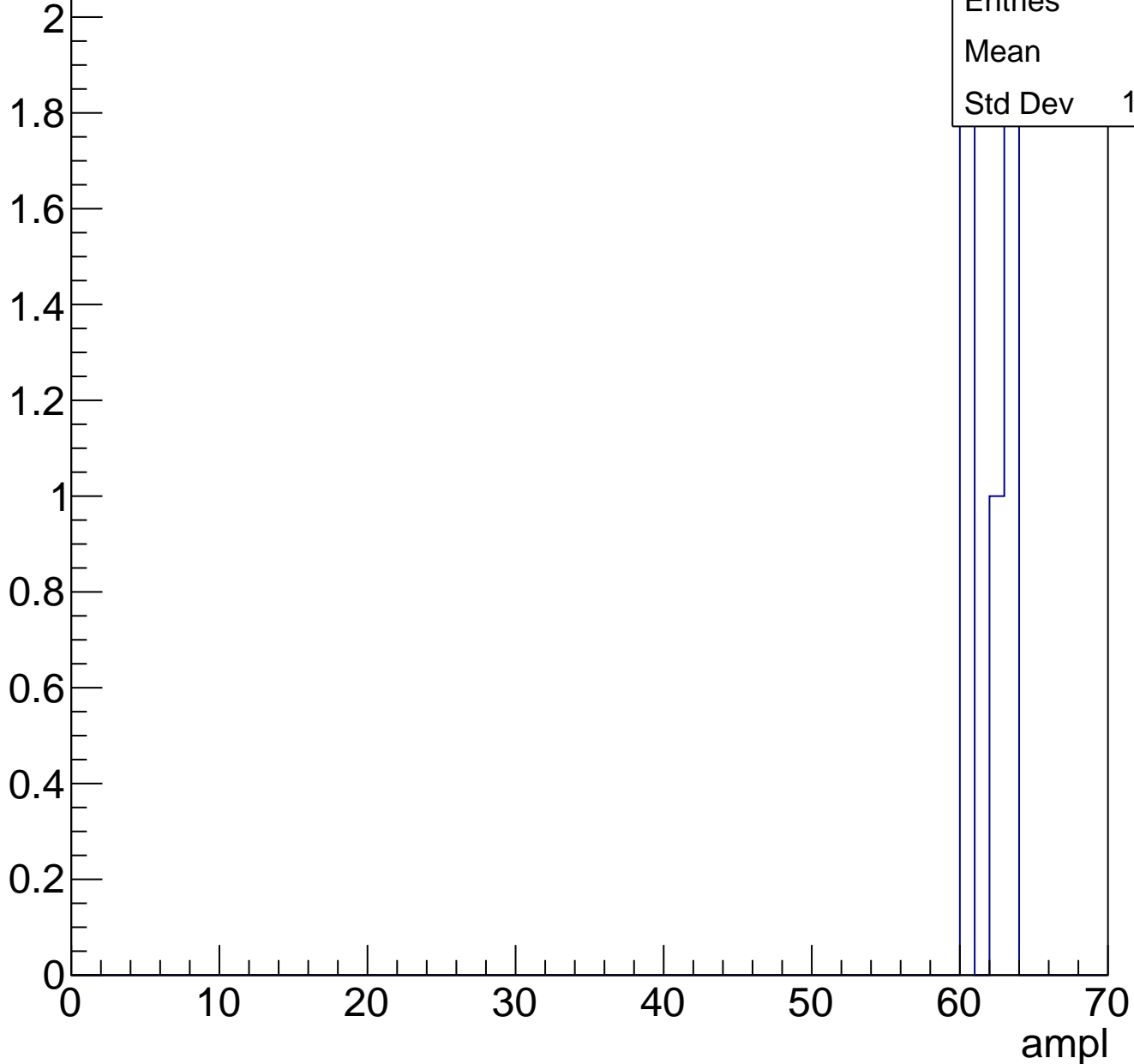
0 10 20 30 40 50 60 70



# B1L101S, U19-ch21, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U19-ch21, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U19-ch22, adc0

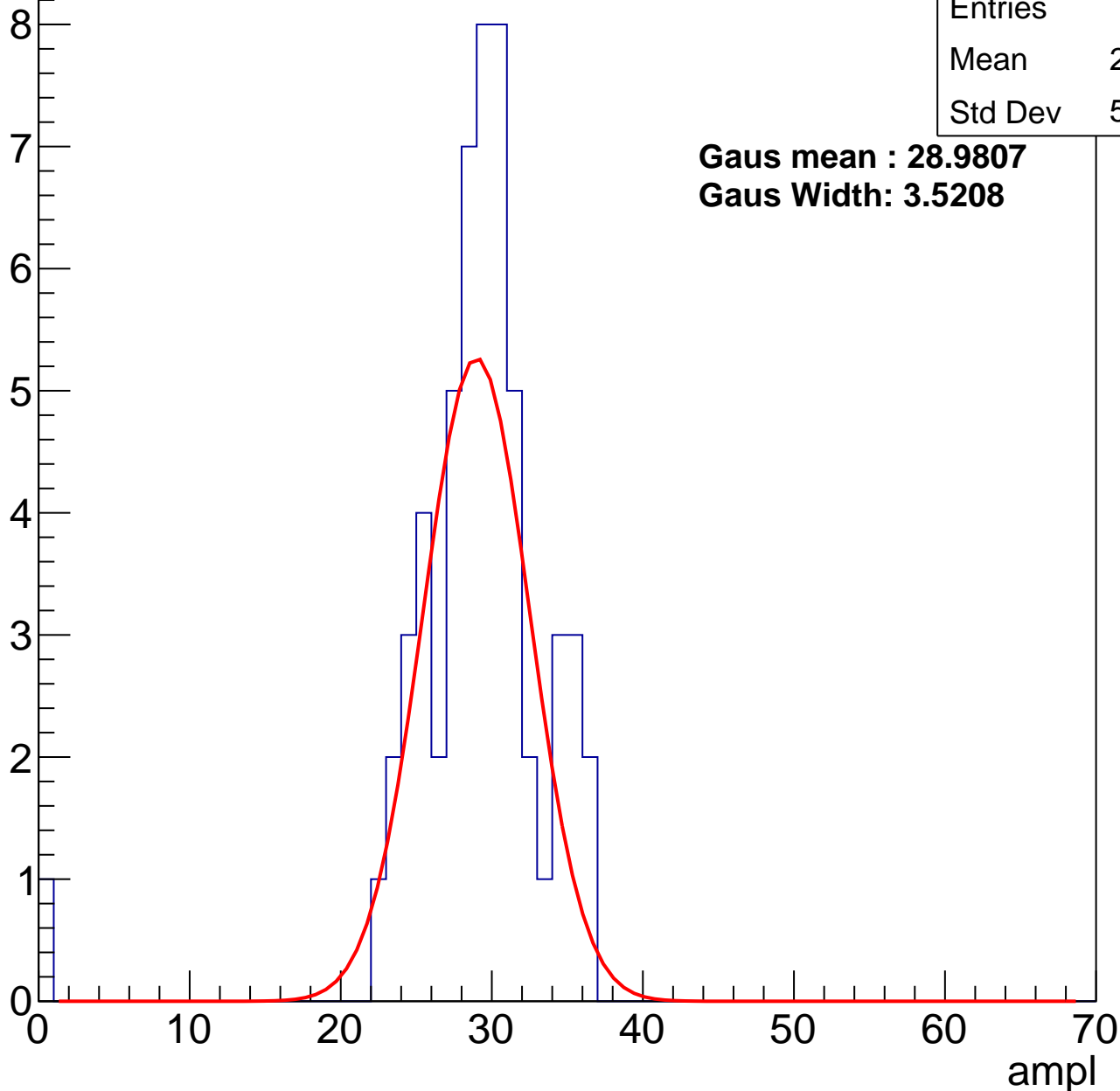
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	57
Mean	28.53
Std Dev	5.089

**Gaus mean : 28.9807**

**Gaus Width: 3.5208**



# B1L101S, U19-ch22, adc1

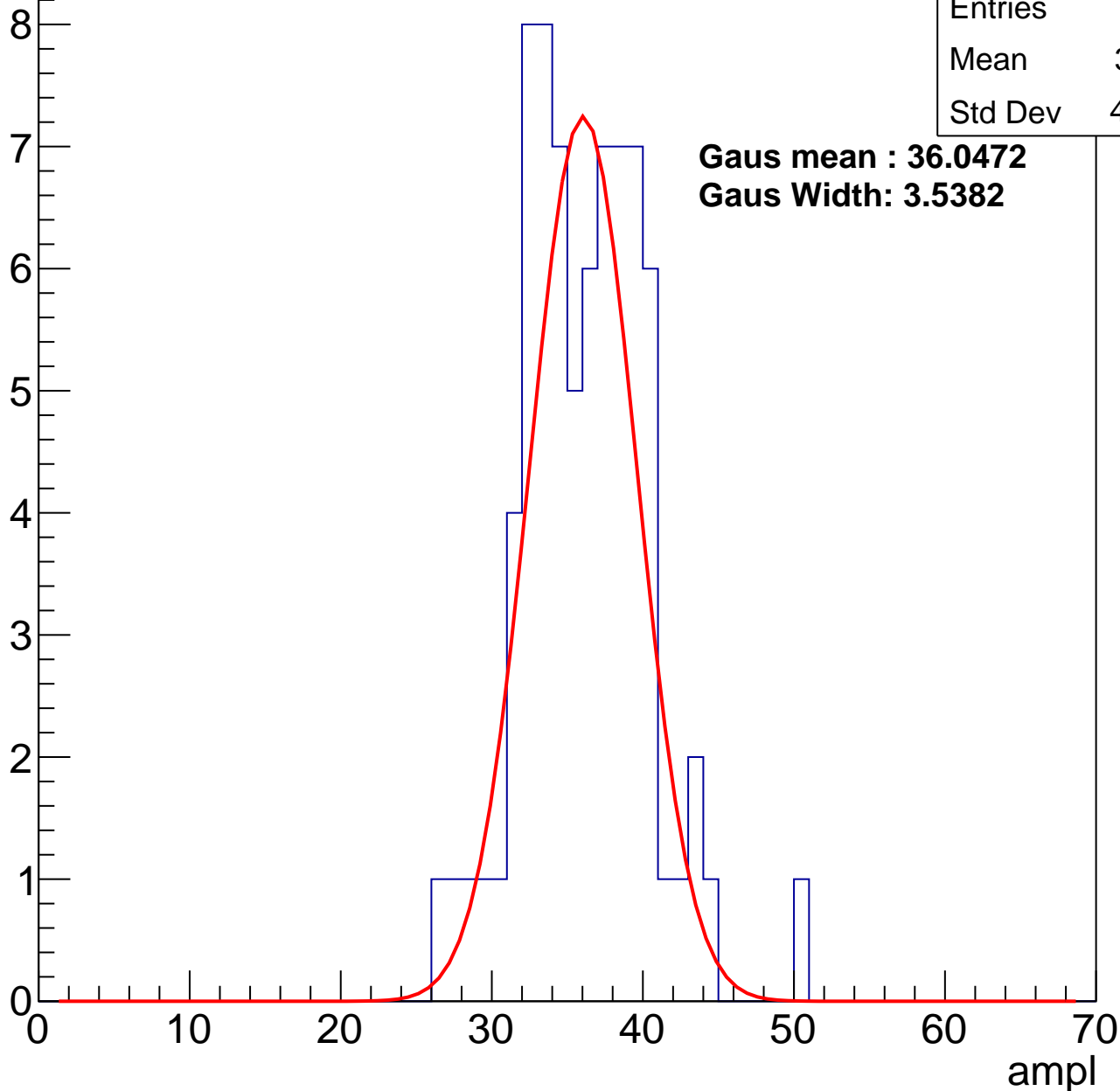
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	76
Mean	35.71
Std Dev	4.087

**Gaus mean : 36.0472**

**Gaus Width: 3.5382**



# B1L101S, U19-ch22, adc2

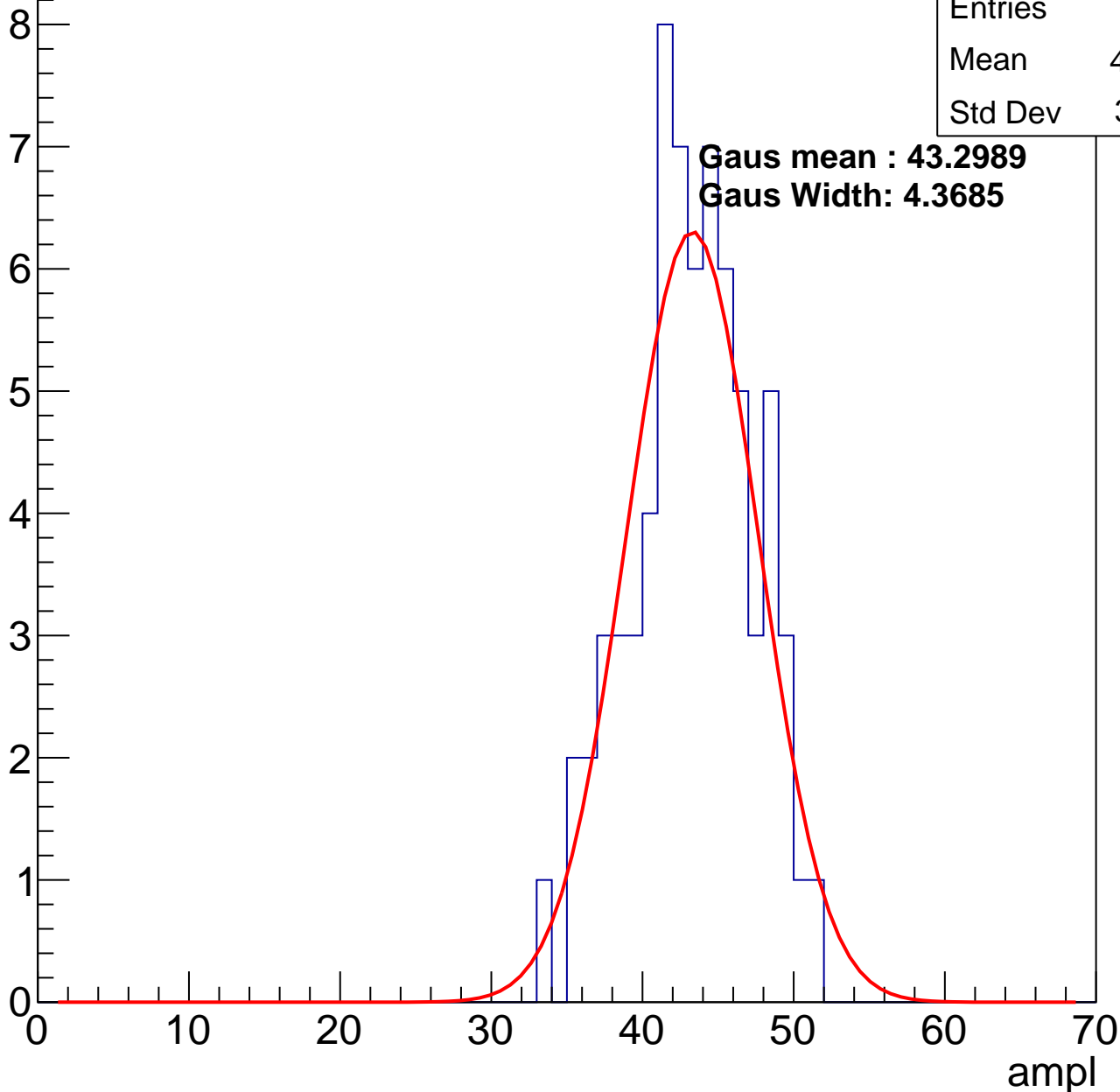
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	42.77
Std Dev	3.961

**Gaus mean : 43.2989**

**Gaus Width: 4.3685**

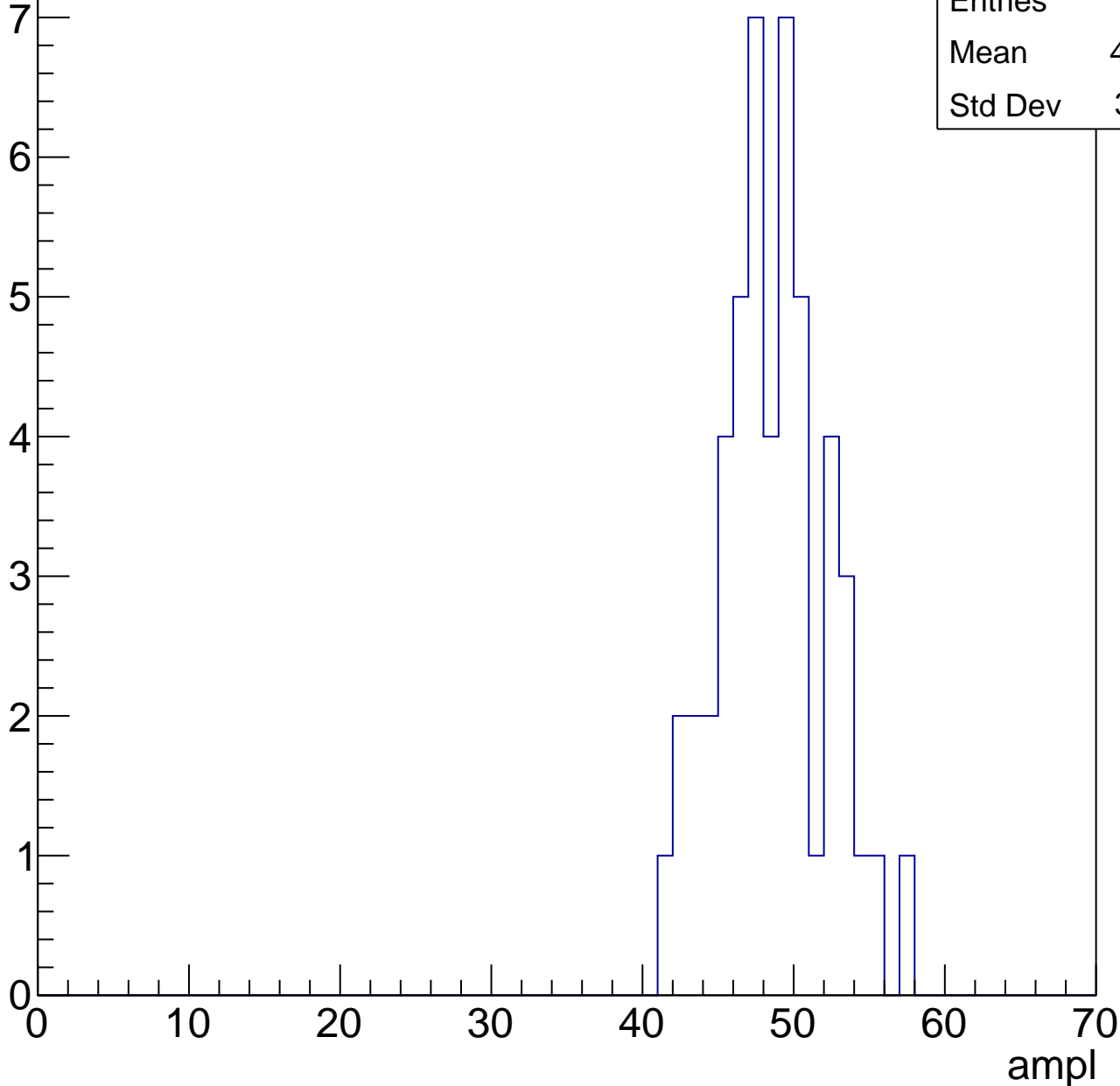


# B1L101S, U19-ch22, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	50
Mean	48.14
Std Dev	3.481

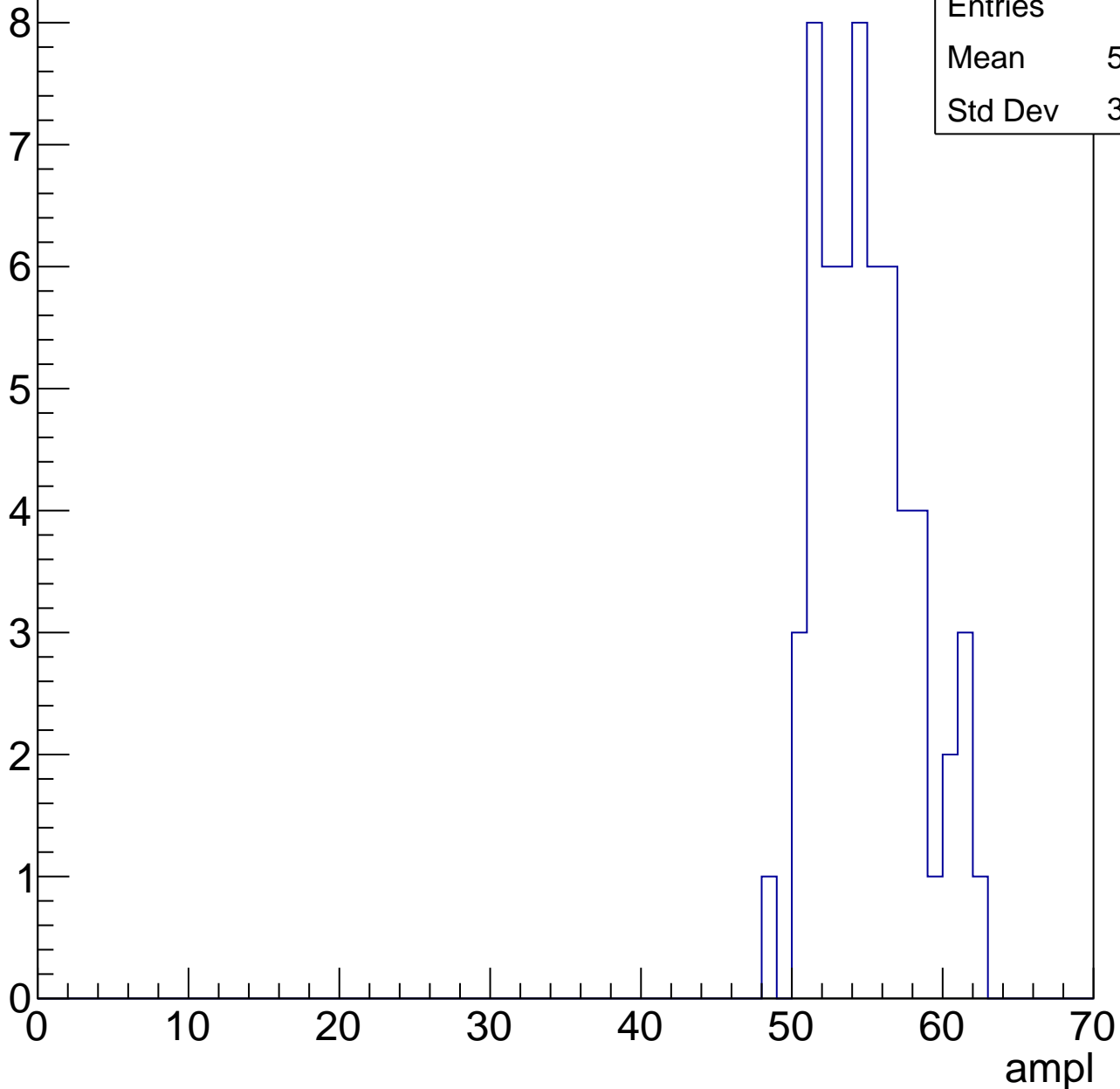


# B1L101S, U19-ch22, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	59
Mean	54.54
Std Dev	3.207

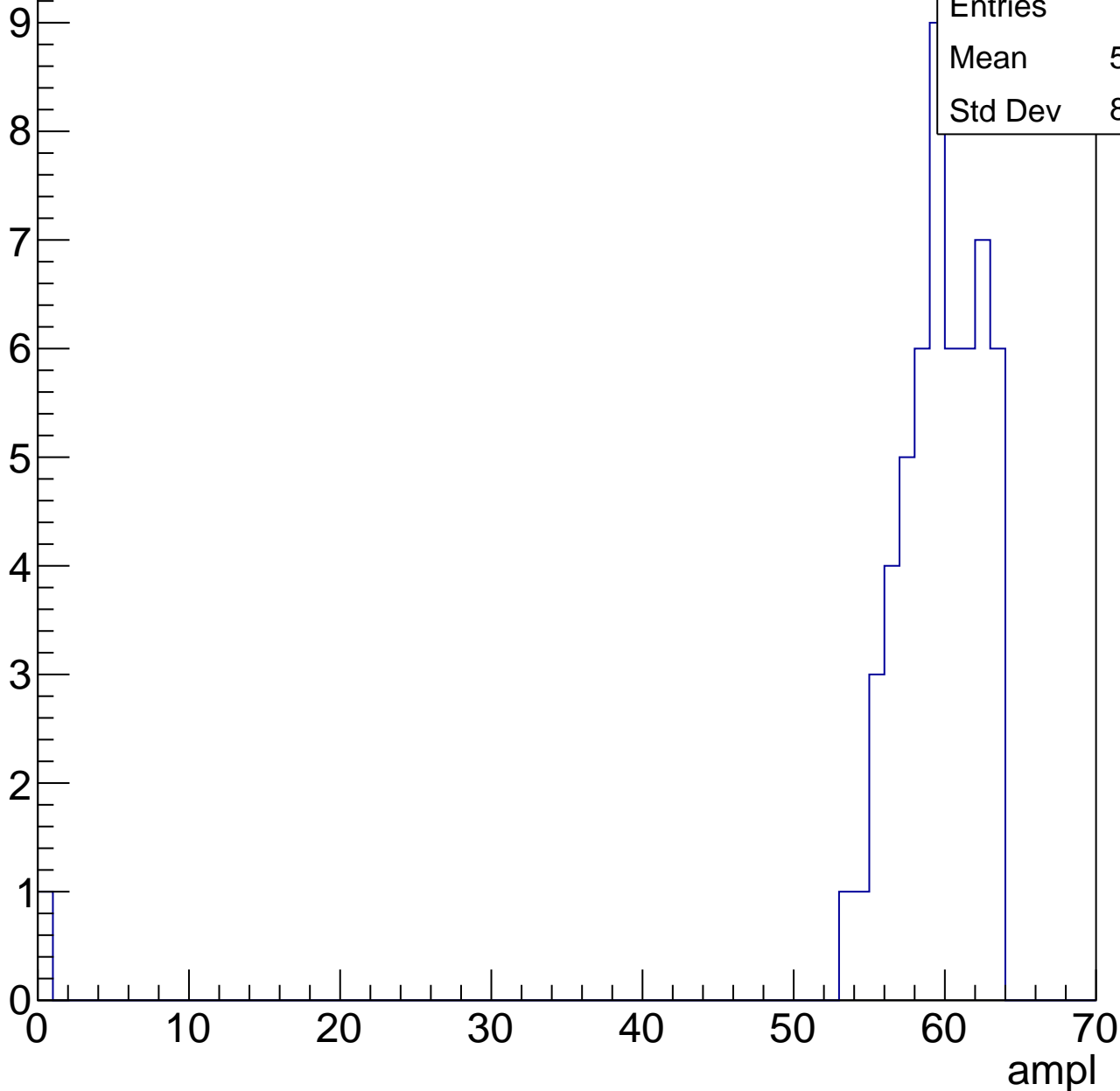


# B1L101S, U19-ch22, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

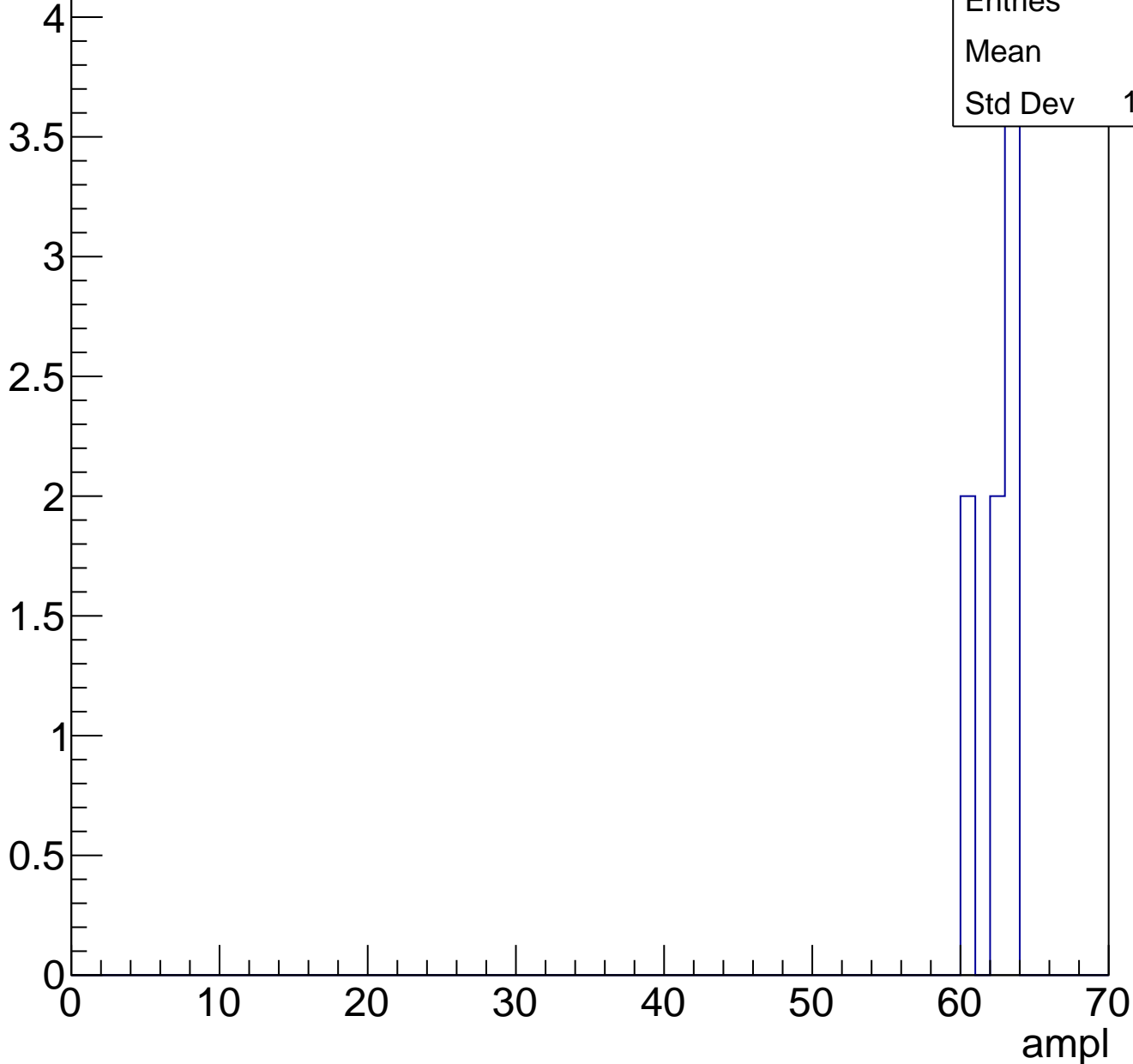
Entries	55
Mean	58.15
Std Dev	8.313



# B1L101S, U19-ch22, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

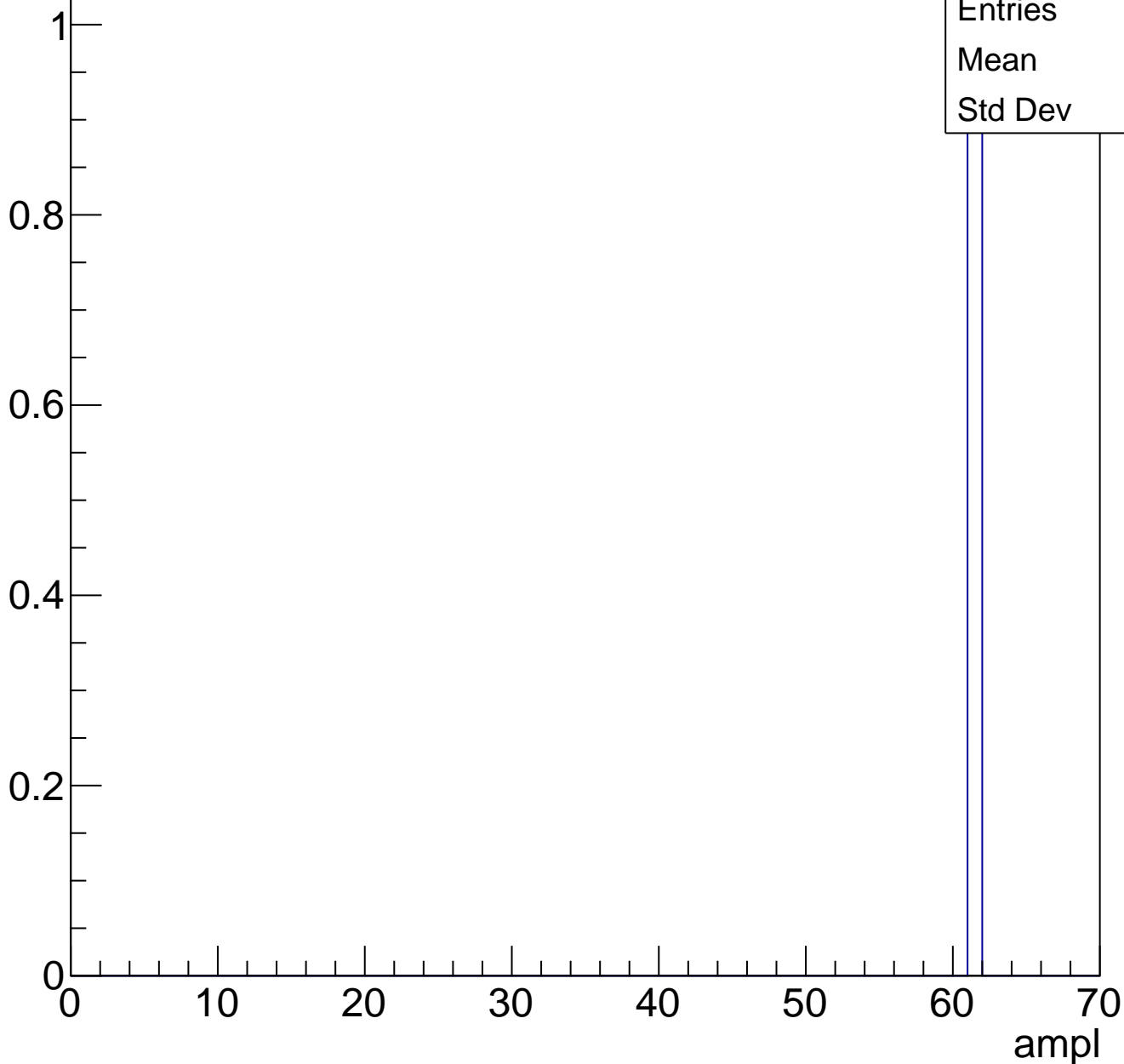




# B1L101S, U19-ch22, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U19-ch23, adc0

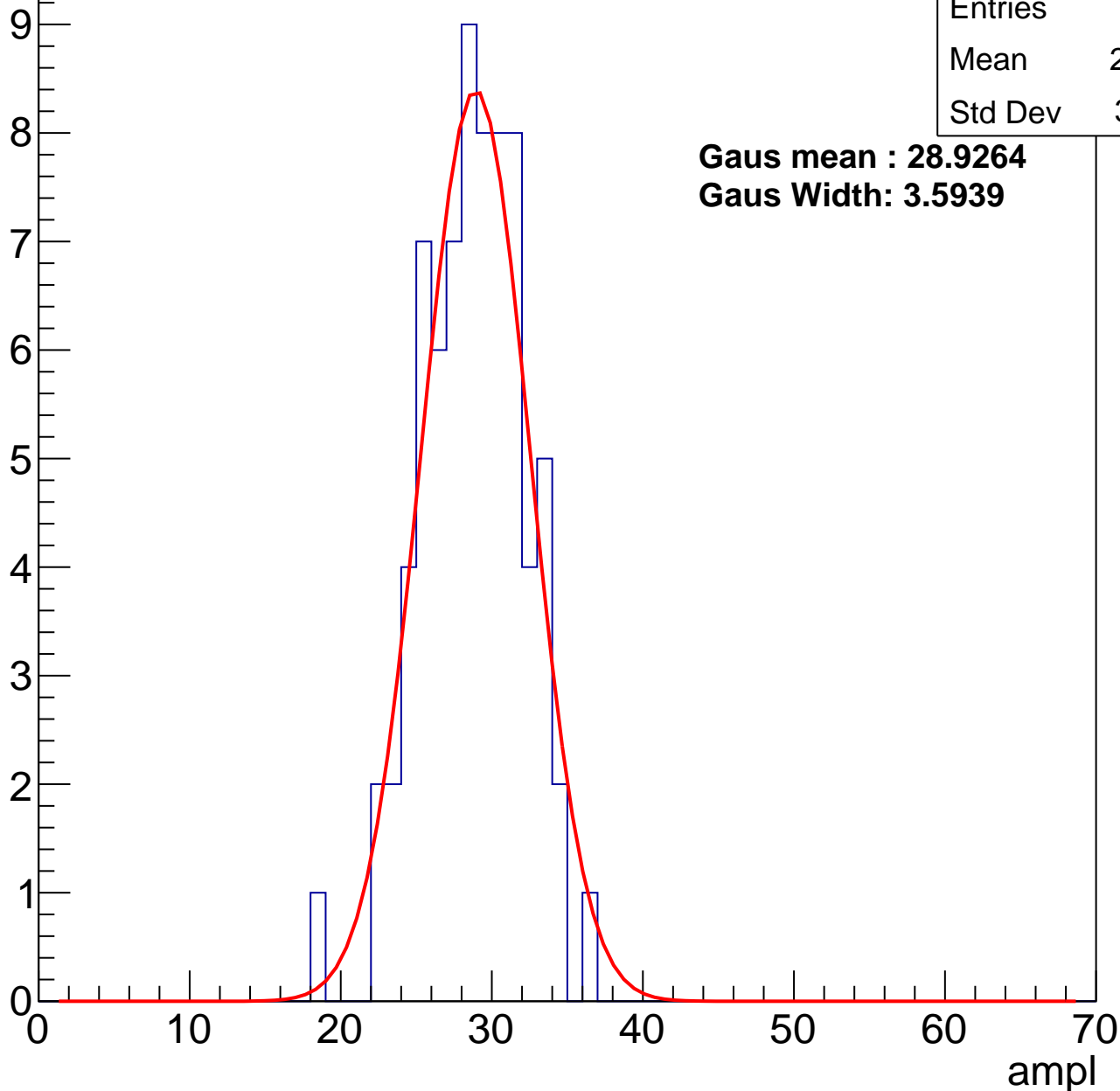
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	74
Mean	28.28
Std Dev	3.311

**Gaus mean : 28.9264**

**Gaus Width: 3.5939**



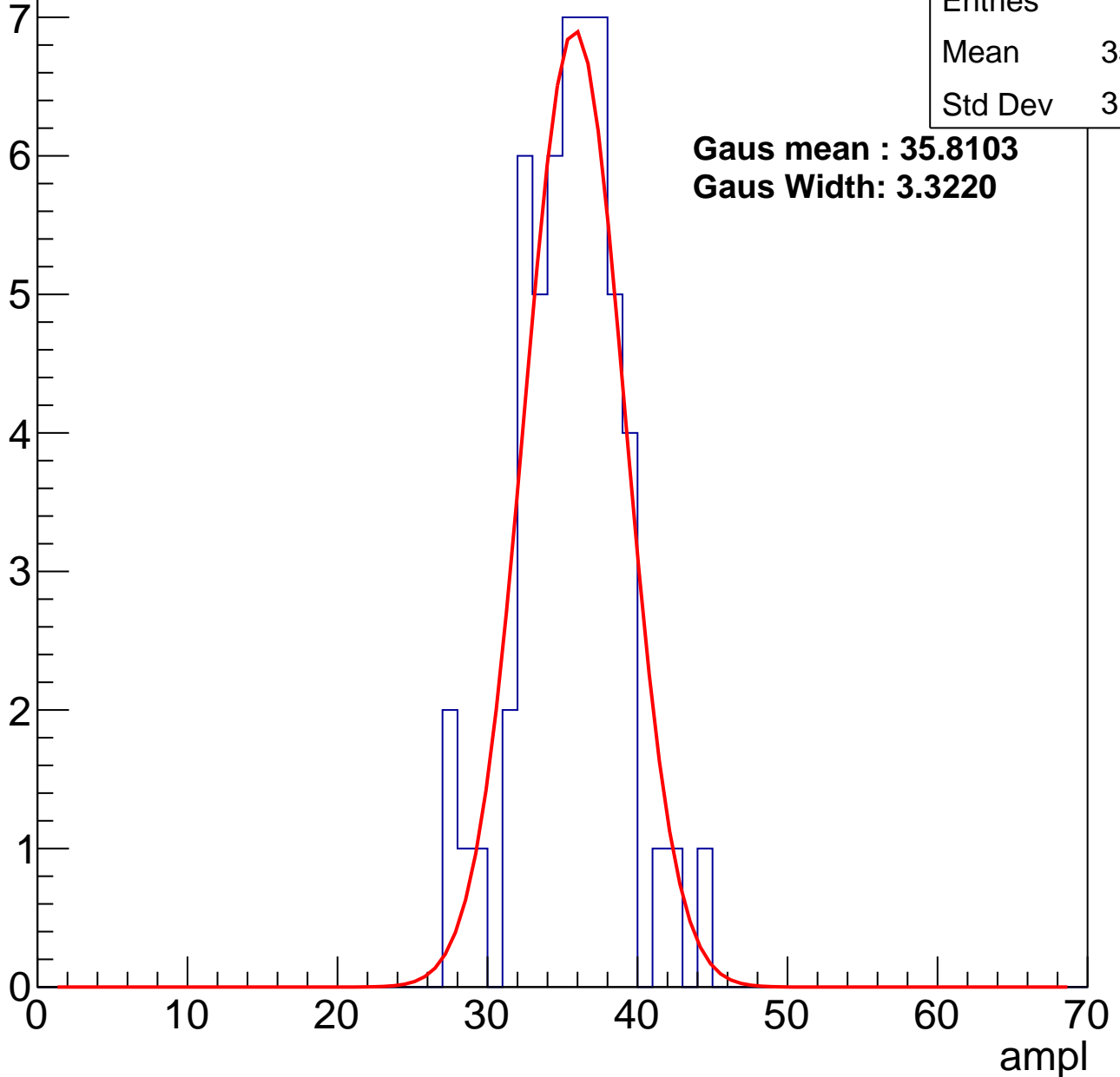
# B1L101S, U19-ch23, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	56
Mean	35.05
Std Dev	3.367

**Gaus mean : 35.8103**  
**Gaus Width: 3.3220**



# B1L101S, U19-ch23, adc2

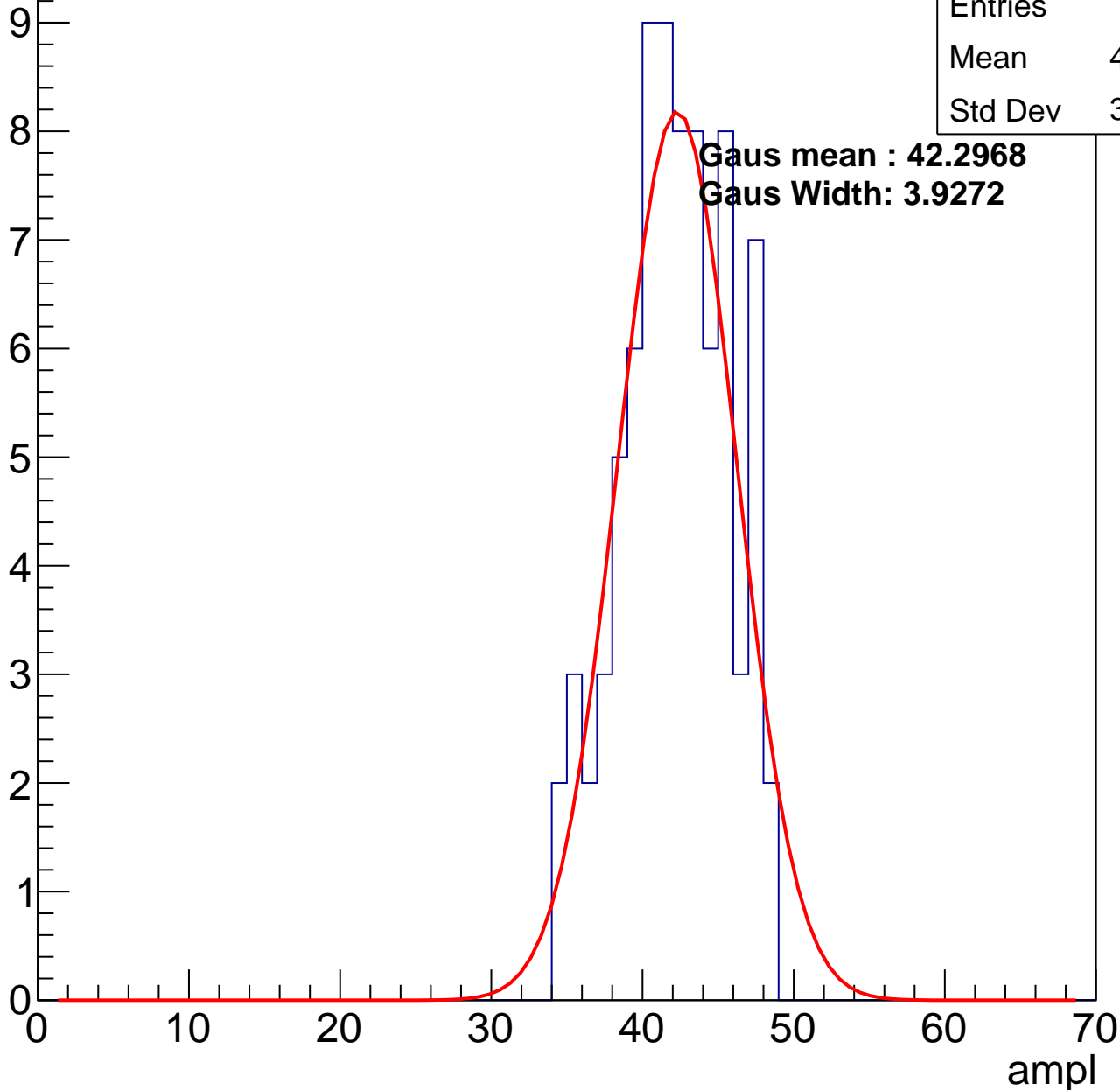
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	81
Mean	41.68
Std Dev	3.499

**Gaus mean : 42.2968**

**Gaus Width: 3.9272**



# B1L101S, U19-ch23, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	69
Mean	49.28
Std Dev	3.459

Entry

10

8

6

4

2

0

0

10

20

30

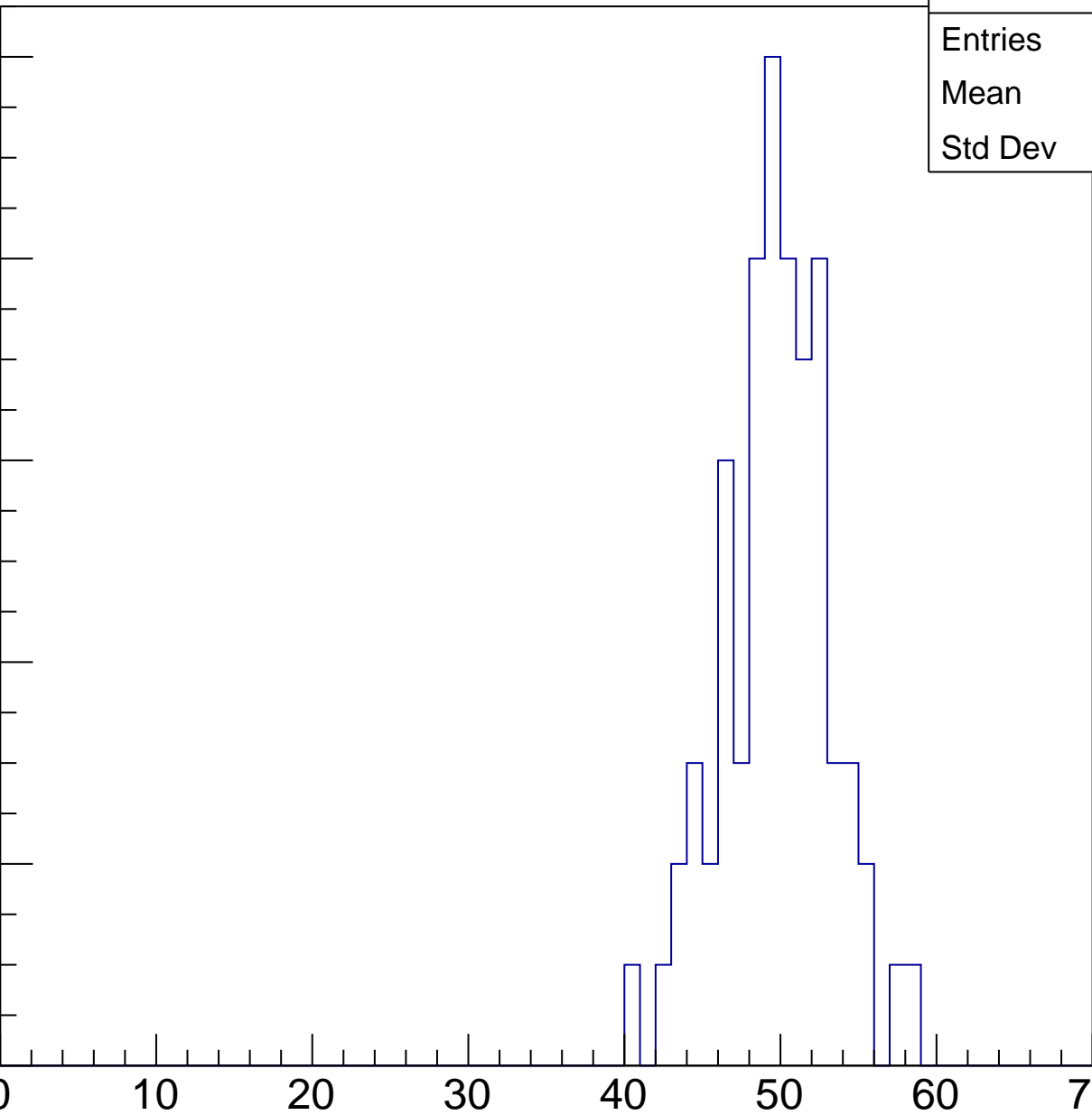
40

50

60

ampl

70

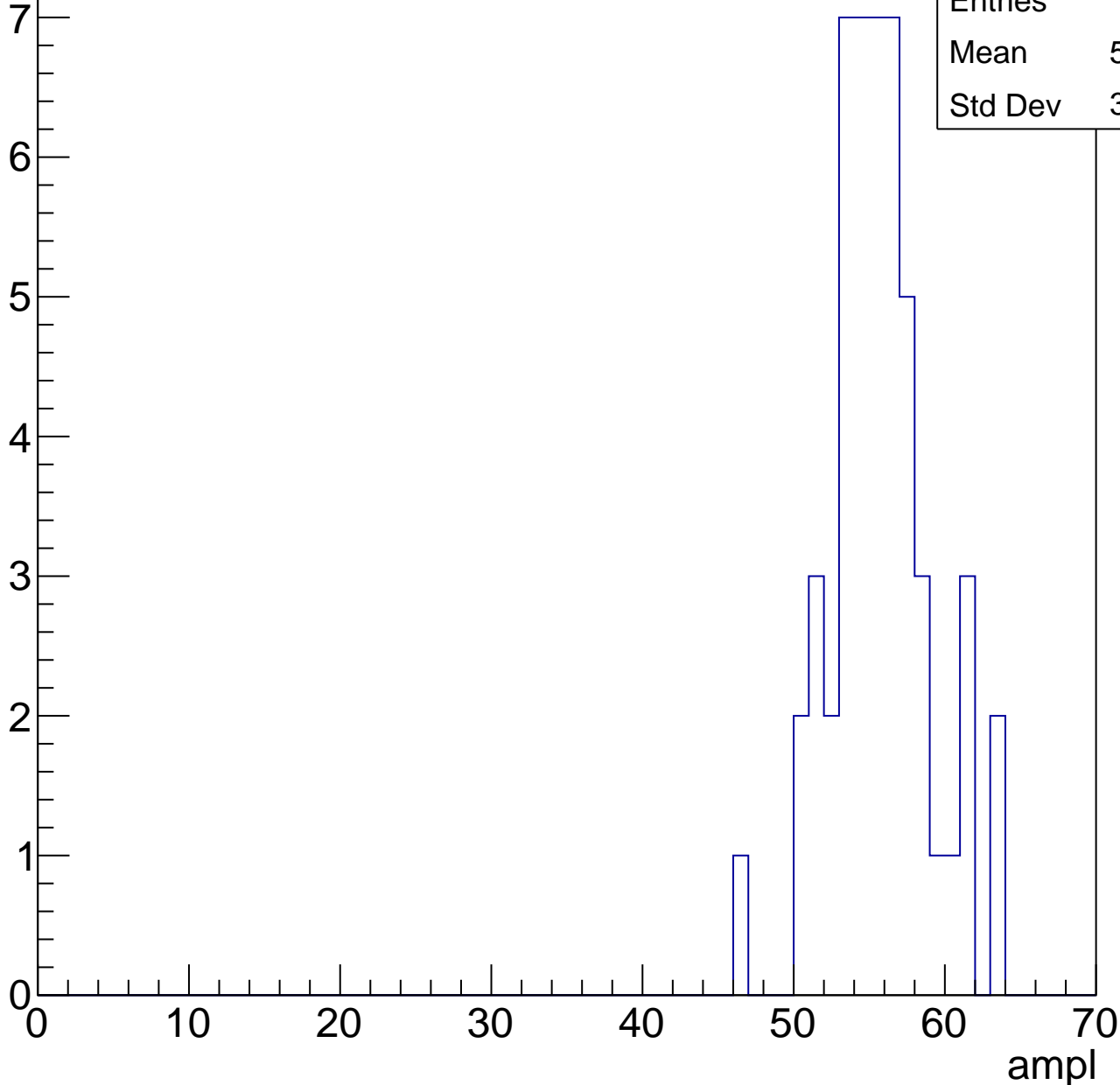


# B1L101S, U19-ch23, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

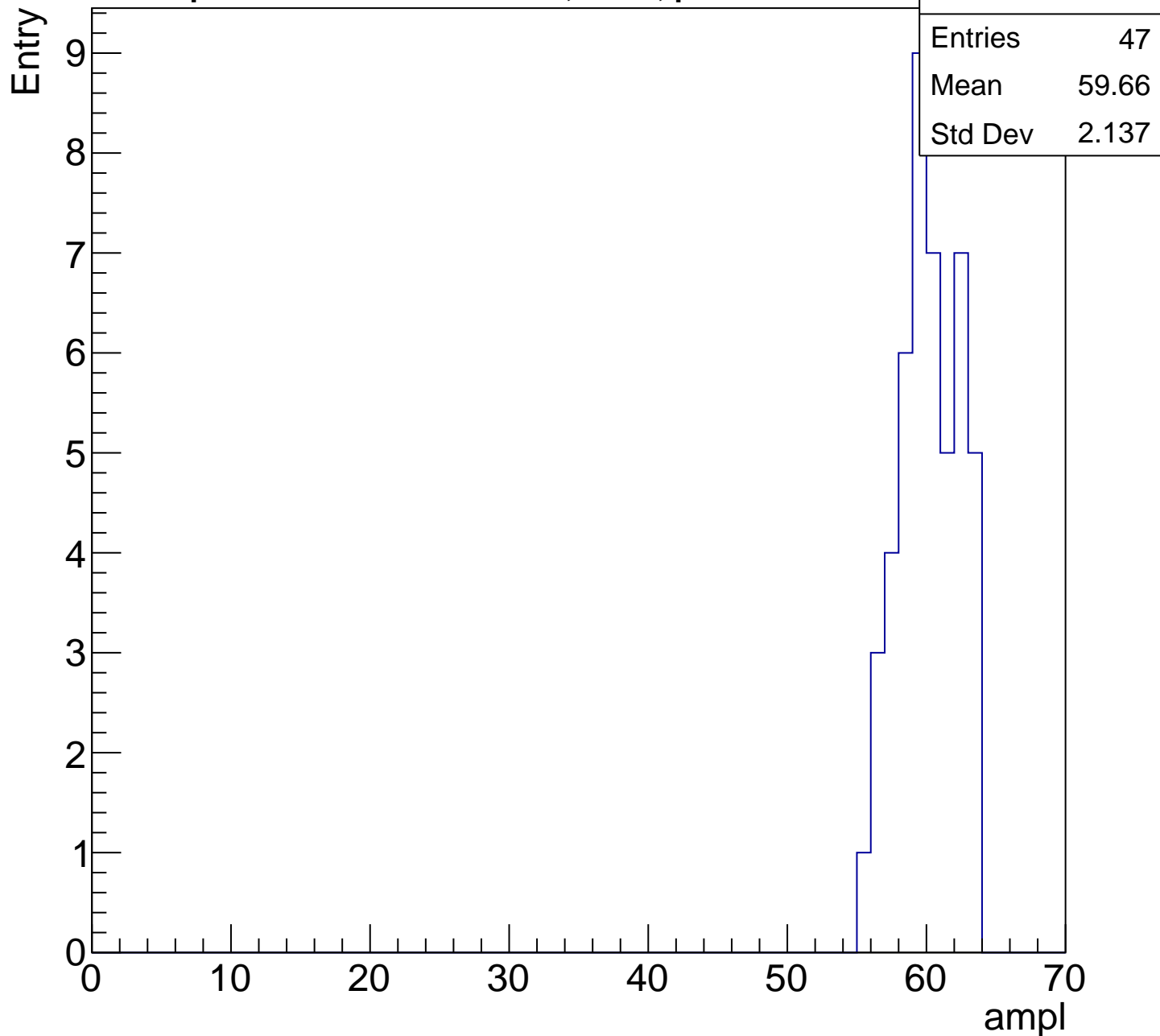
Entry

Entries	51
Mean	55.22
Std Dev	3.316



# B1L101S, U19-ch23, adc5

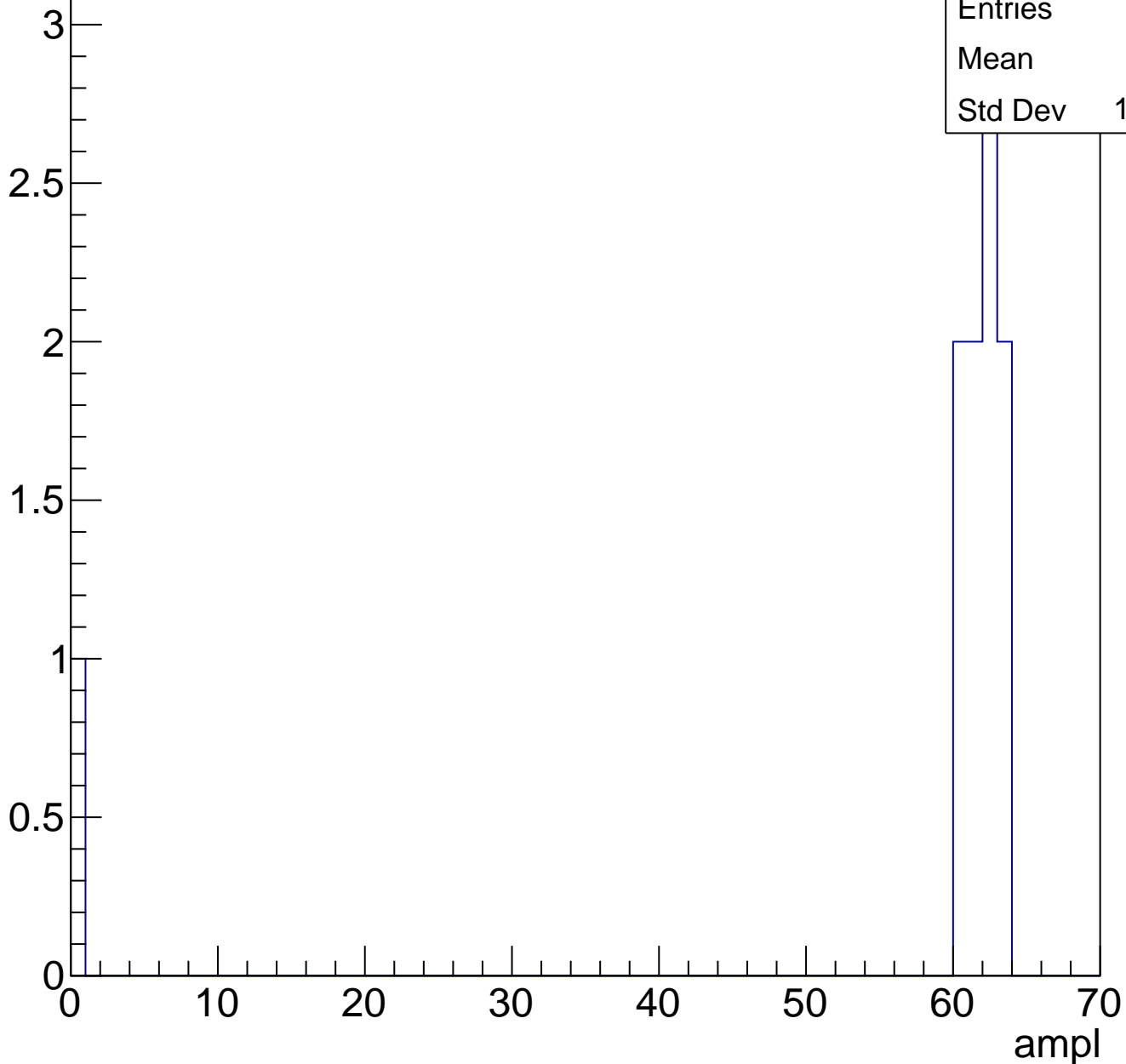
calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U19-ch23, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U19-ch23, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U19-ch24, adc0

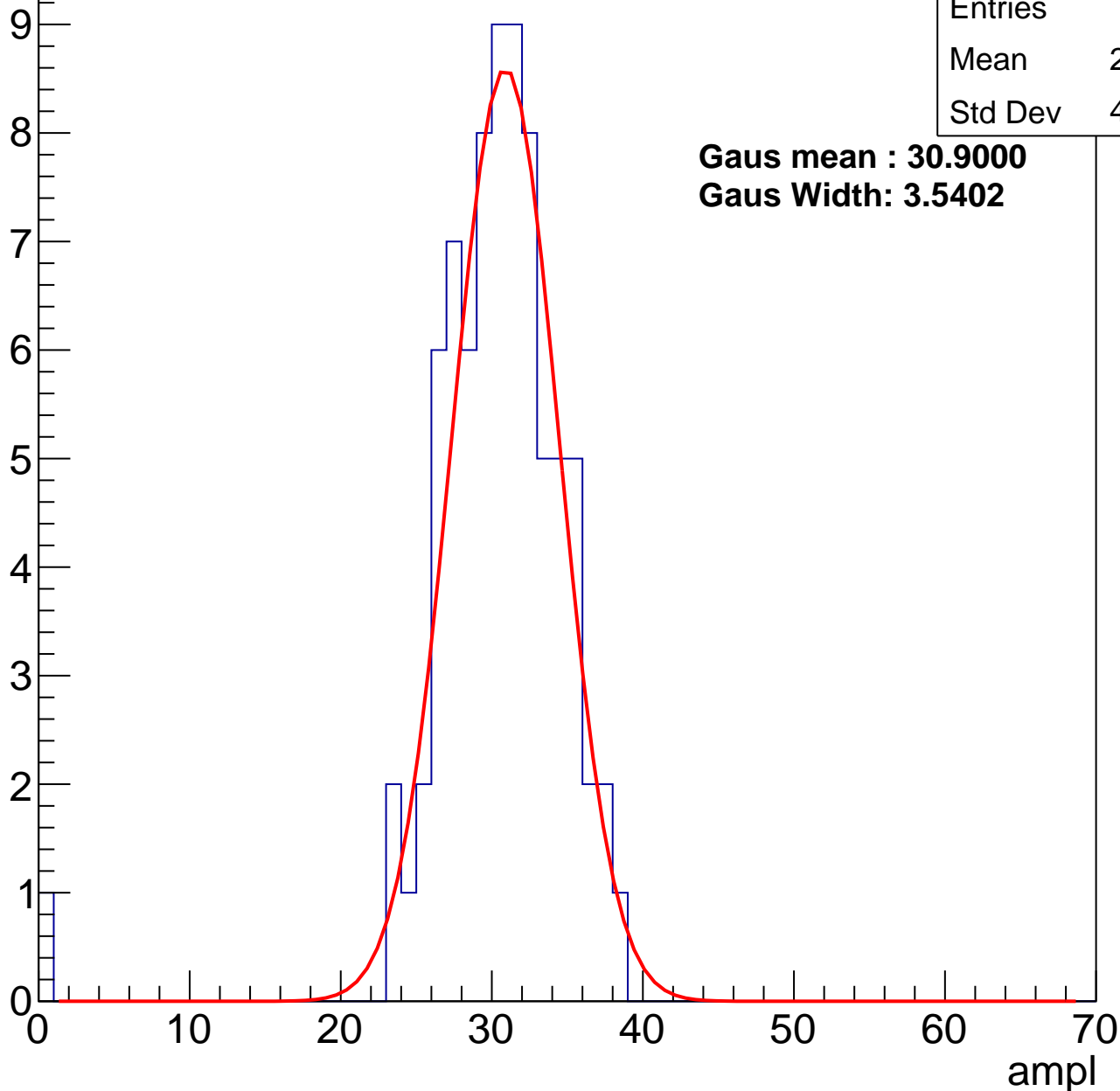
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	79
Mean	29.92
Std Dev	4.773

**Gaus mean : 30.9000**

**Gaus Width: 3.5402**



# B1L101S, U19-ch24, adc1

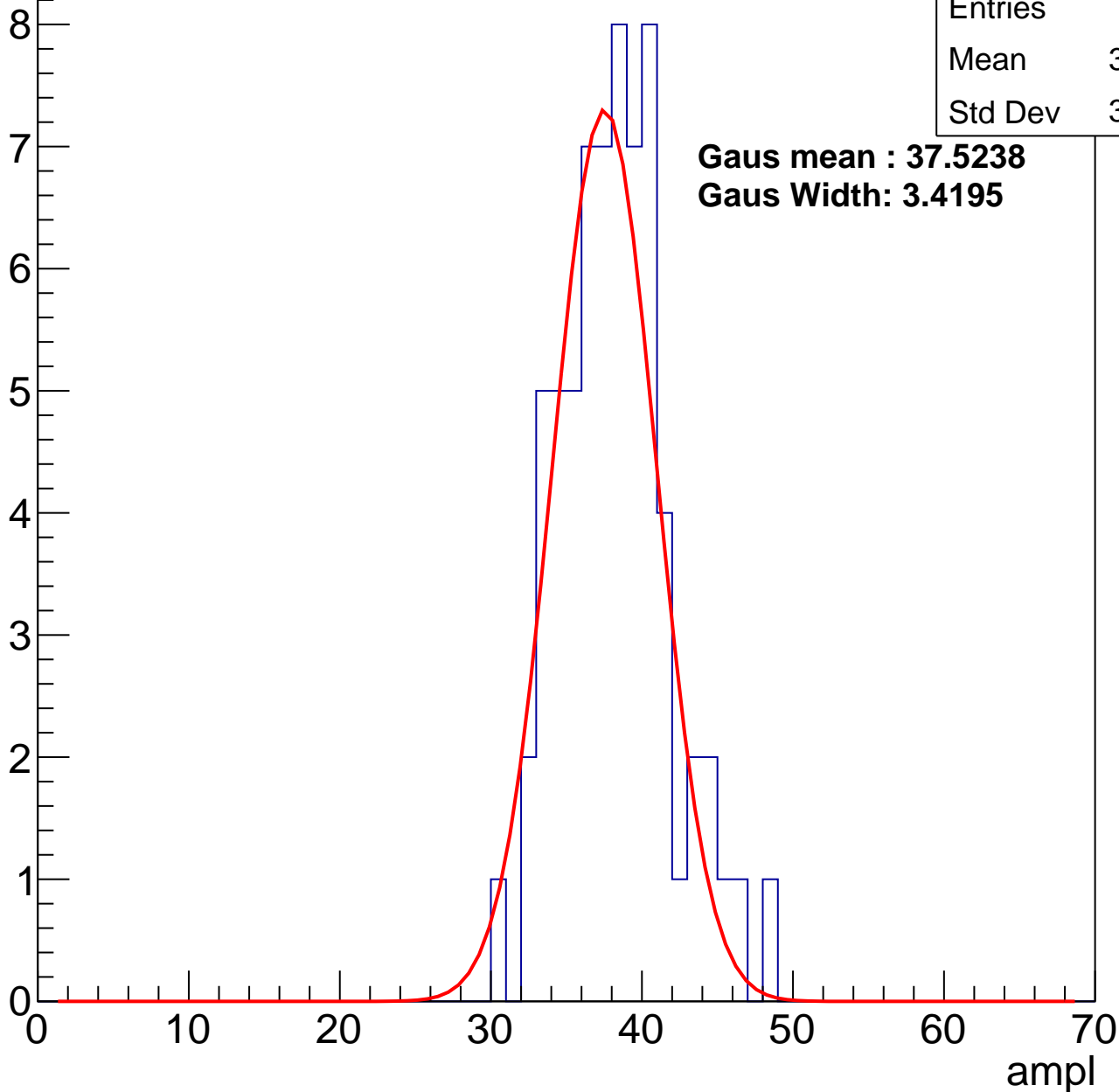
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	67
Mean	37.78
Std Dev	3.548

**Gaus mean : 37.5238**

**Gaus Width: 3.4195**



# B1L101S, U19-ch24, adc2

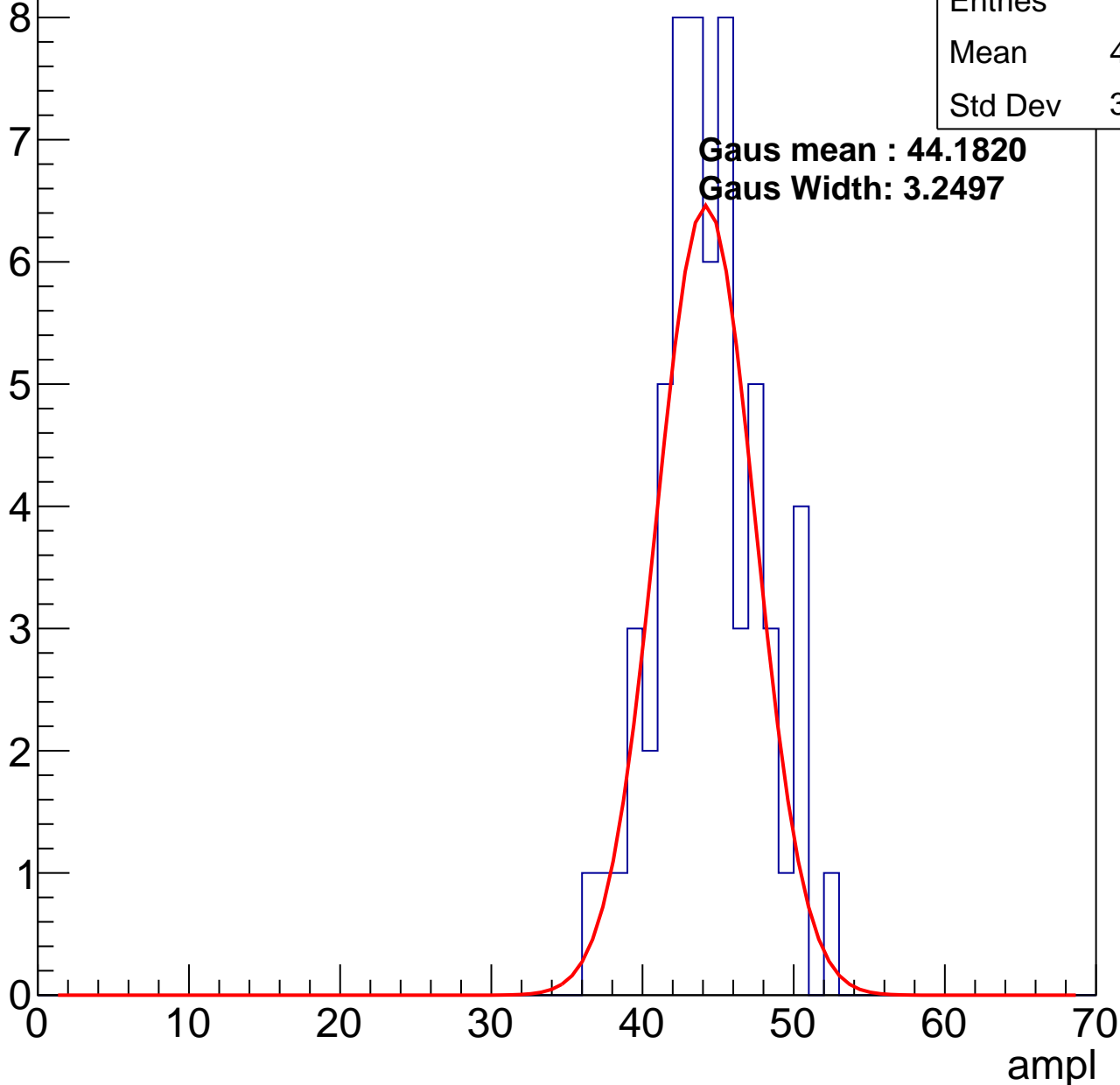
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	60
Mean	43.92
Std Dev	3.383

**Gaus mean : 44.1820**

**Gaus Width: 3.2497**

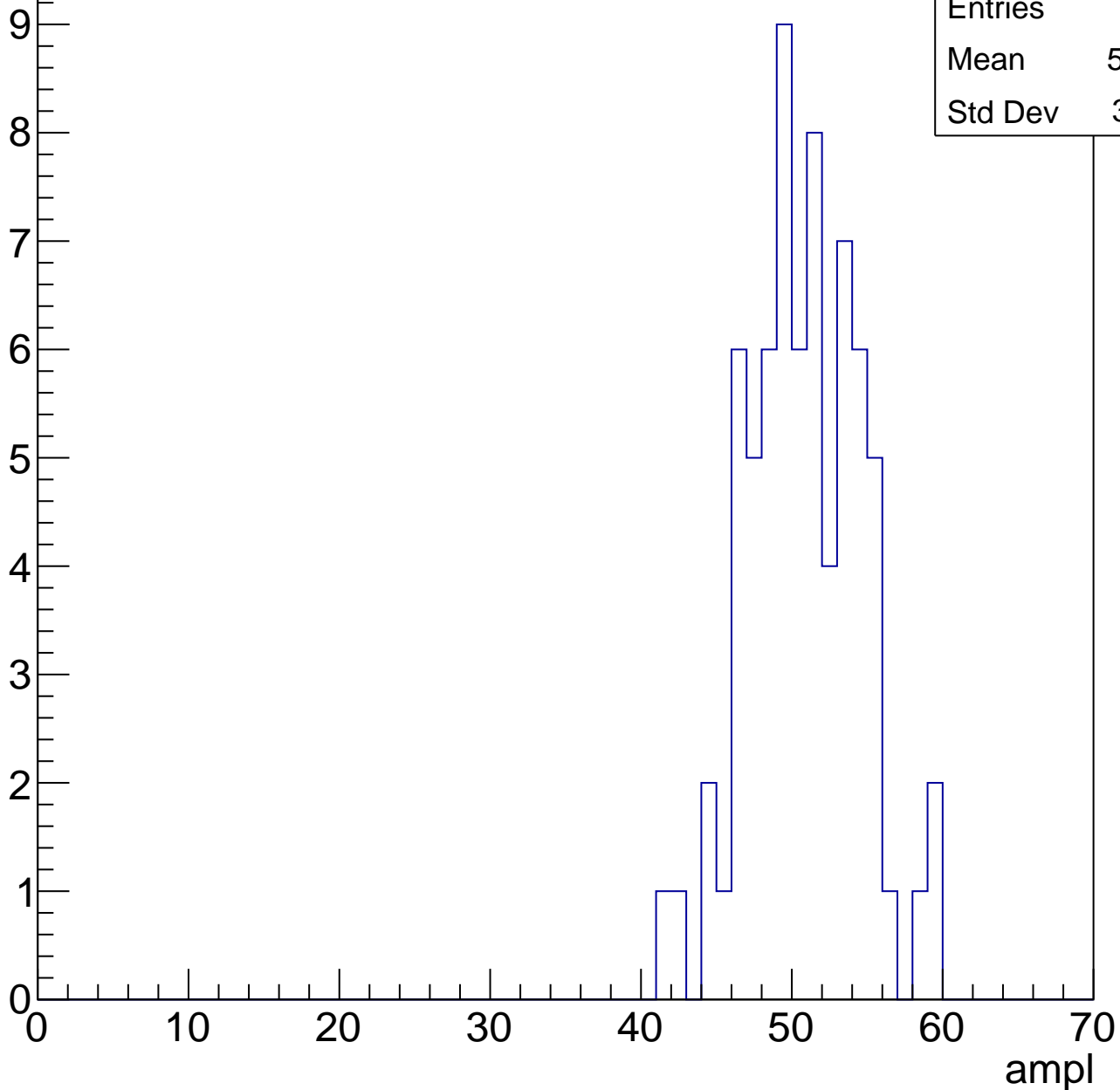


# B1L101S, U19-ch24, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

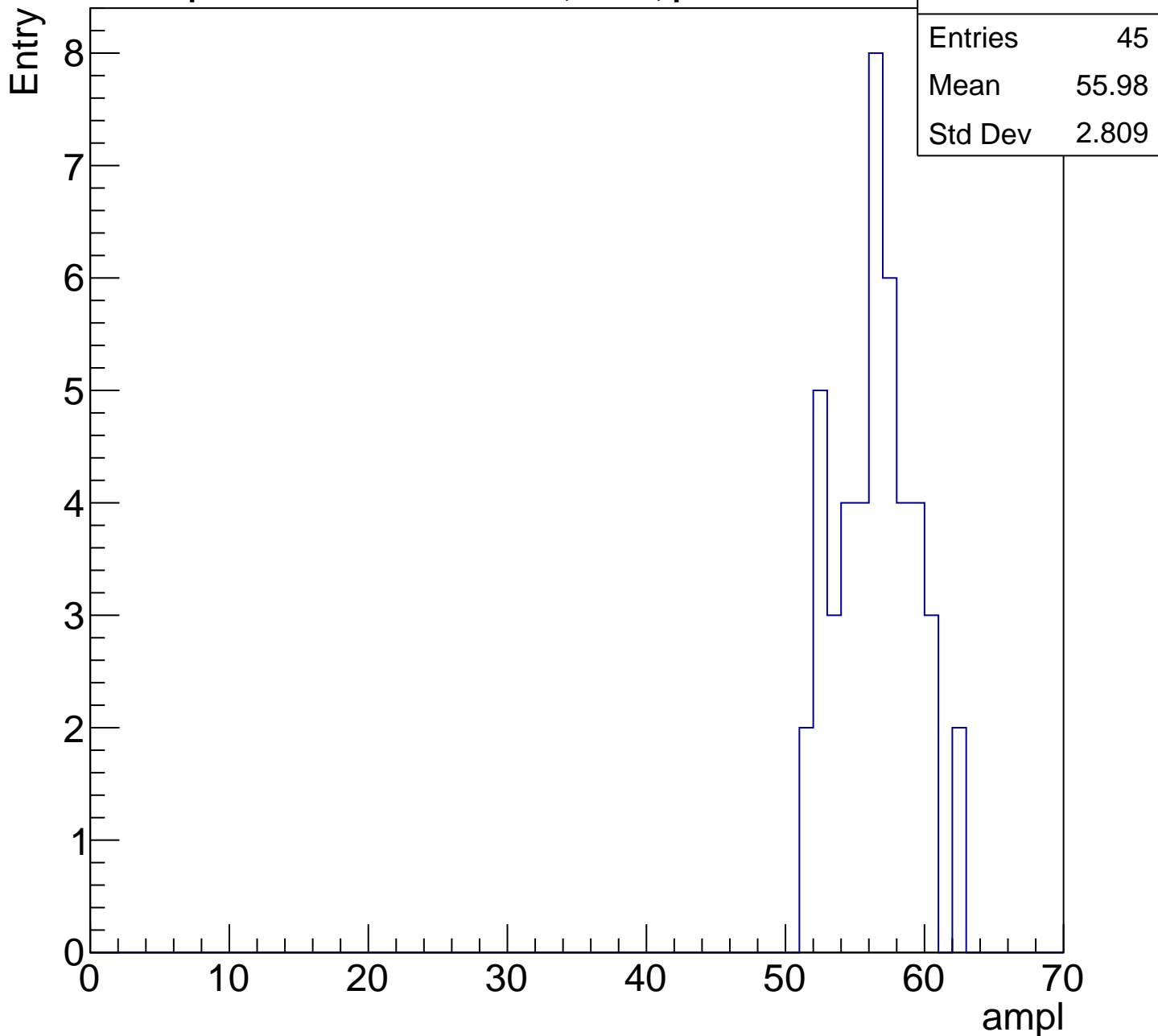
Entry

Entries	71
Mean	50.34
Std Dev	3.711



# B1L101S, U19-ch24, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

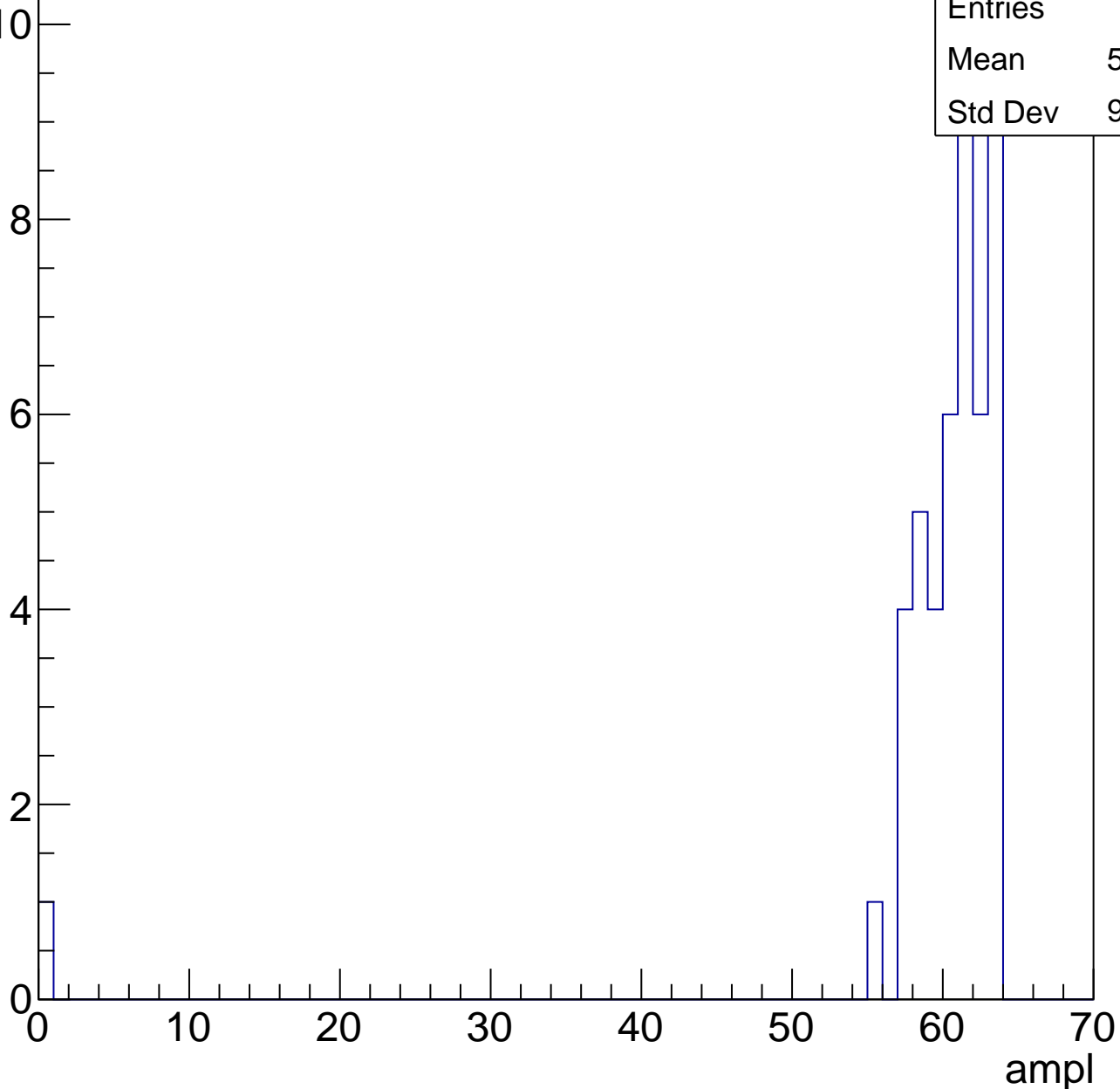


# B1L101S, U19-ch24, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

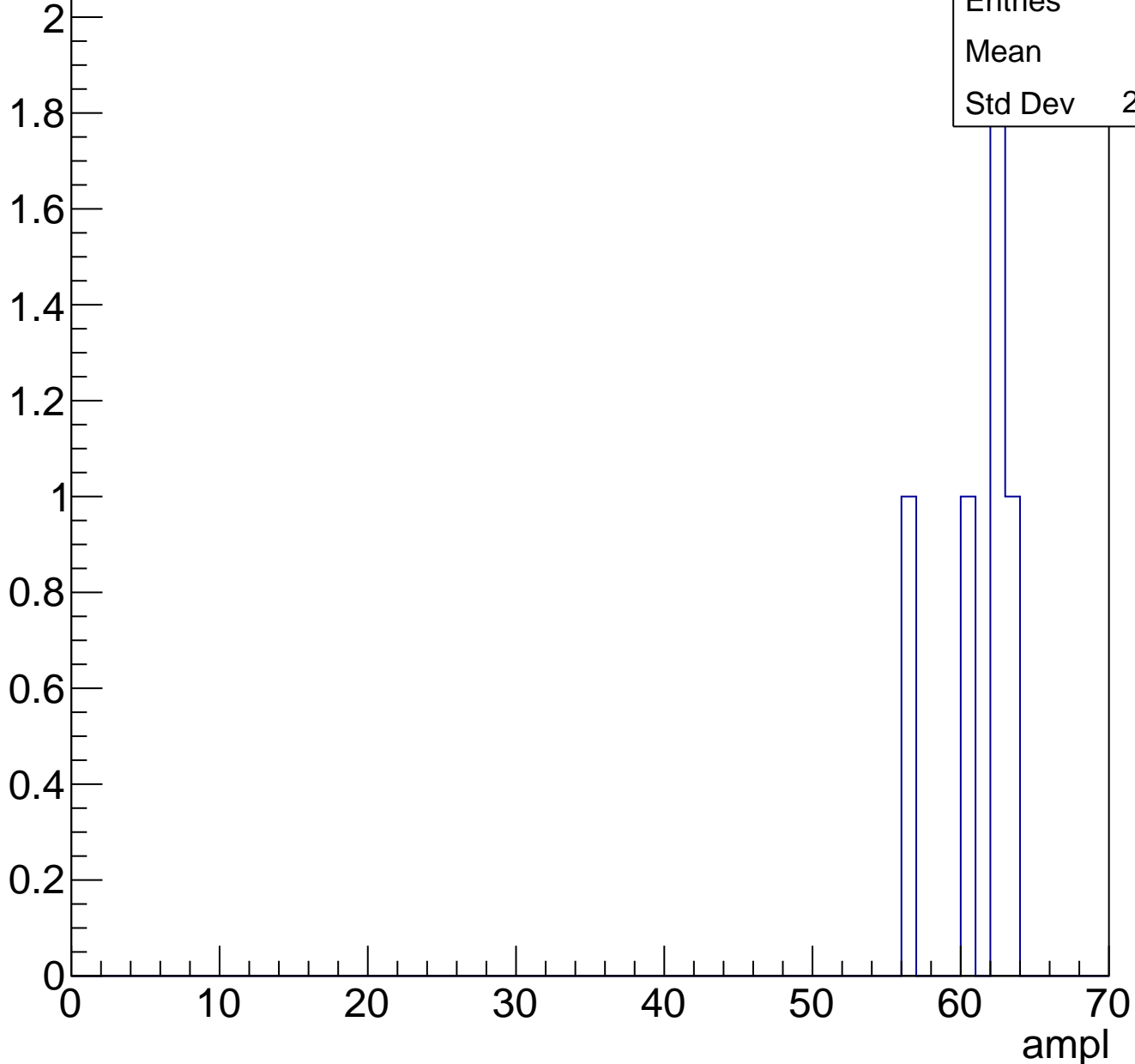
Entries	46
Mean	59.09
Std Dev	9.043



# B1L101S, U19-ch24, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	5
Mean	60.6
Std Dev	2.498



# B1L101S, U19-ch24, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L101S, U19-ch25, adc0

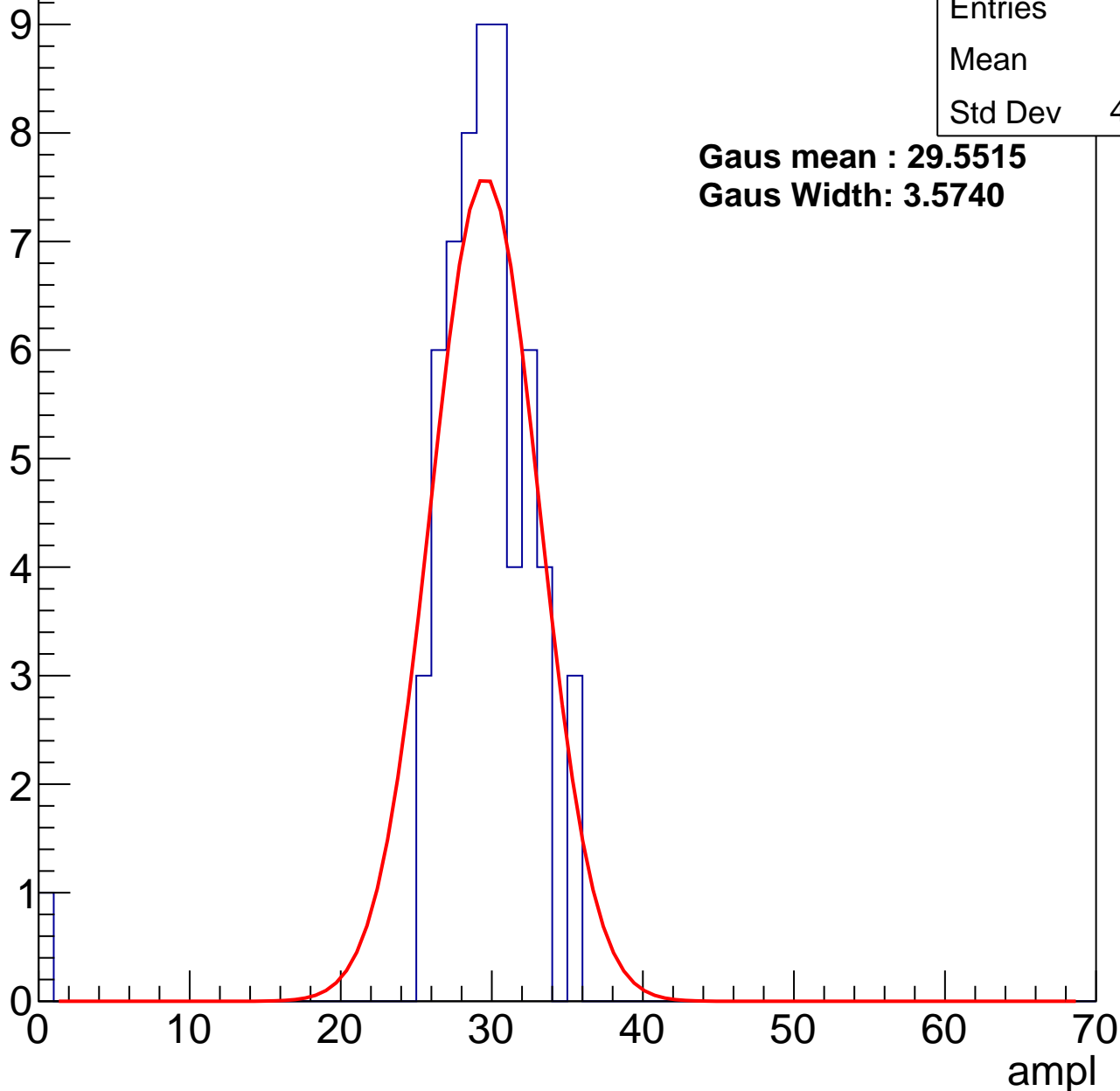
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	60
Mean	28.8
Std Dev	4.523

**Gaus mean : 29.5515**

**Gaus Width: 3.5740**



# B1L101S, U19-ch25, adc1

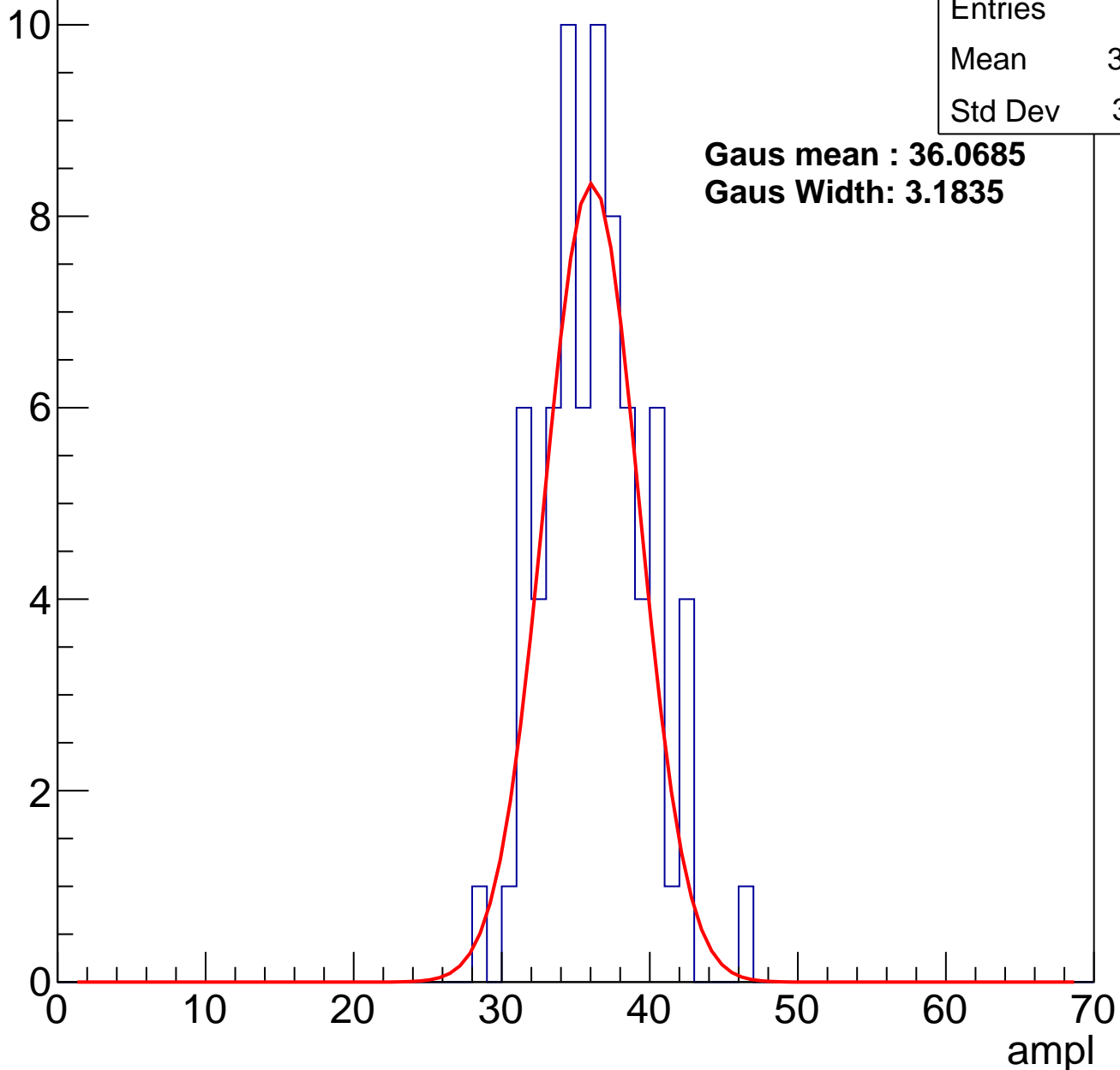
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	74
Mean	35.88
Std Dev	3.381

**Gaus mean : 36.0685**

**Gaus Width: 3.1835**

Entry



# B1L101S, U19-ch25, adc2

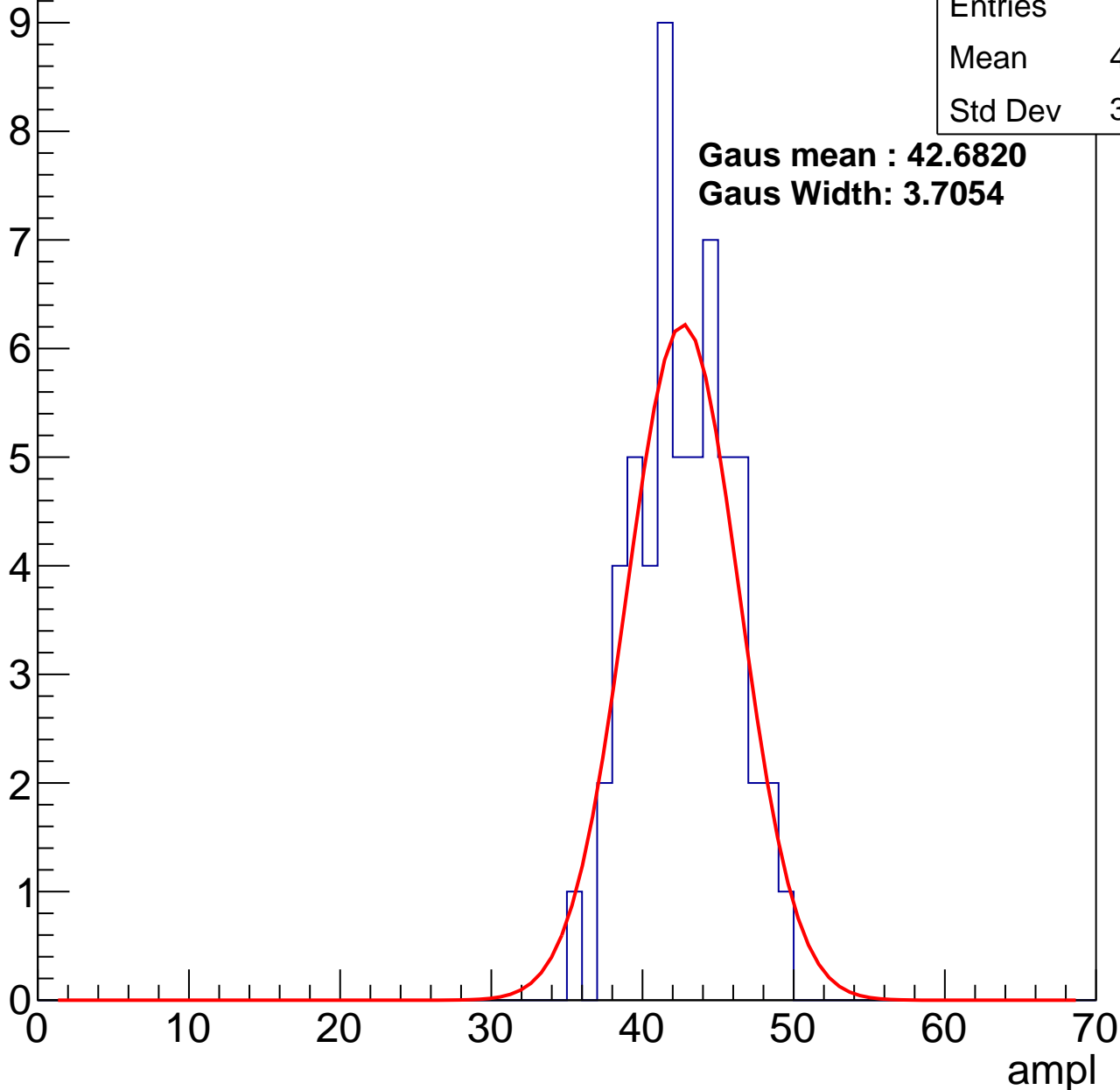
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	57
Mean	42.32
Std Dev	3.124

**Gaus mean : 42.6820**

**Gaus Width: 3.7054**



# B1L101S, U19-ch25, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	67
Mean	48.45
Std Dev	3.534

Entry

10

8

6

4

2

0

0

10

20

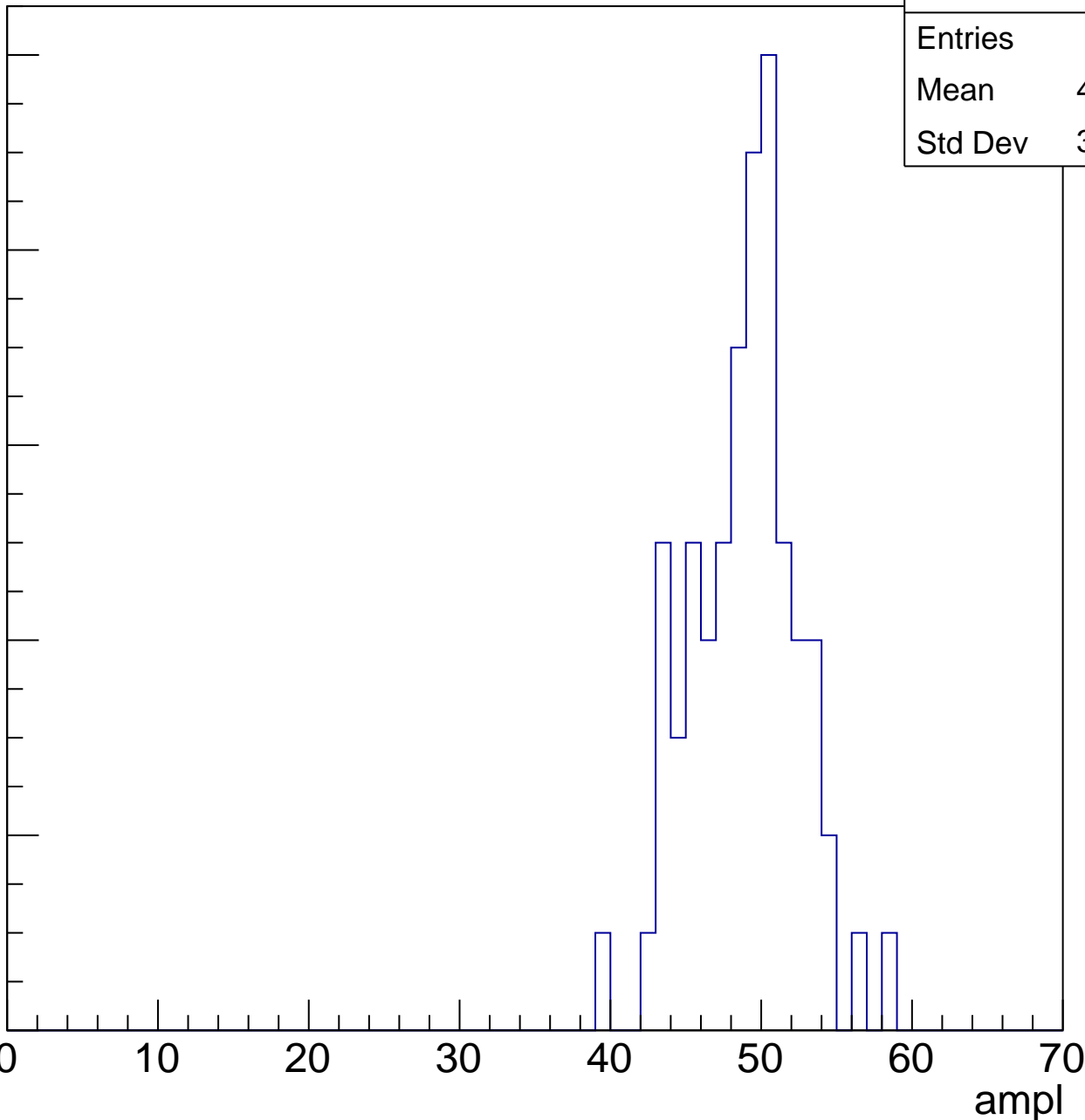
30

40

50

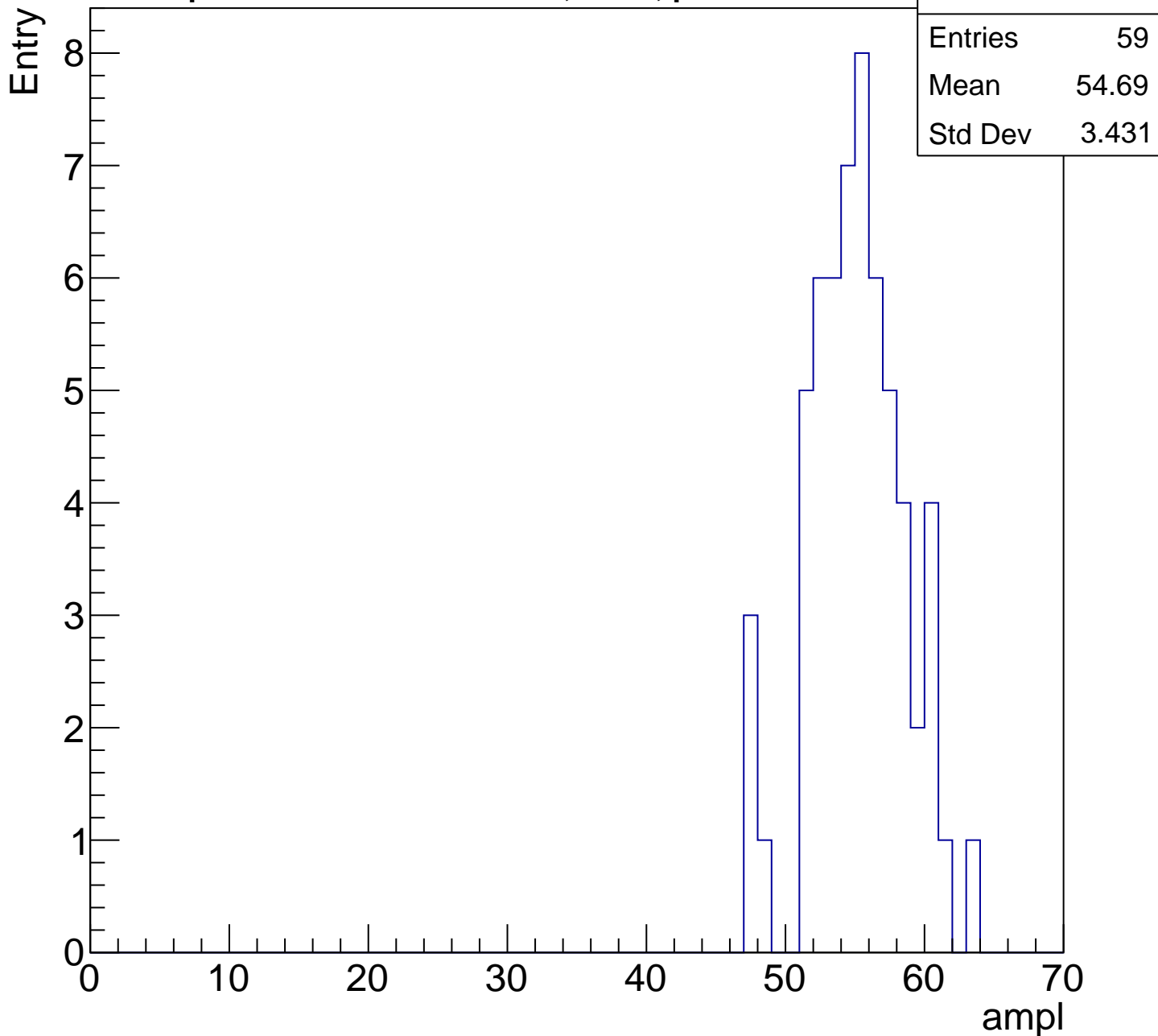
60

ampl



# B1L101S, U19-ch25, adc4

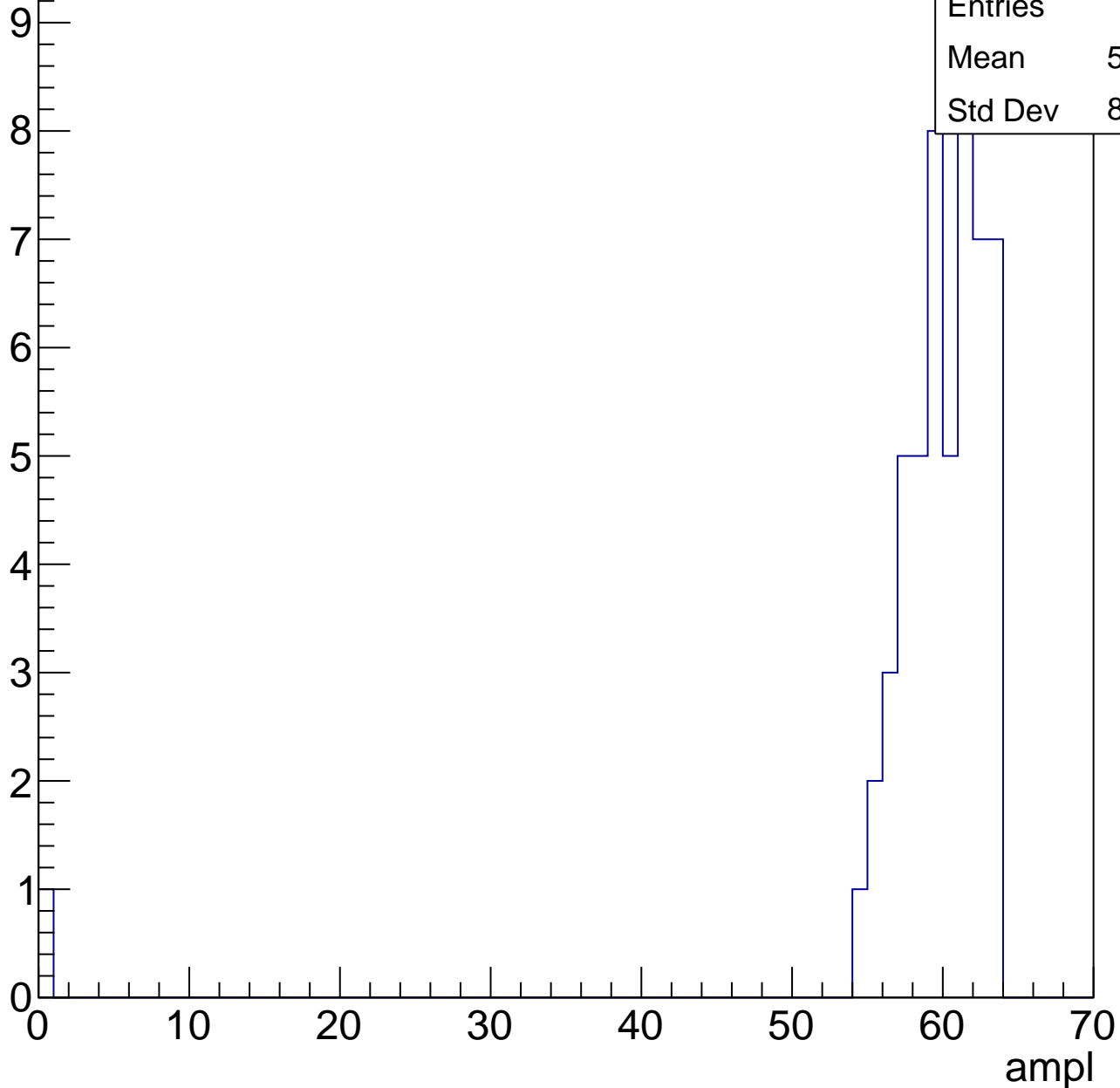
calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U19-ch25, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	53
Mean	58.55
Std Dev	8.462

# B1L101S, U19-ch25, adc6

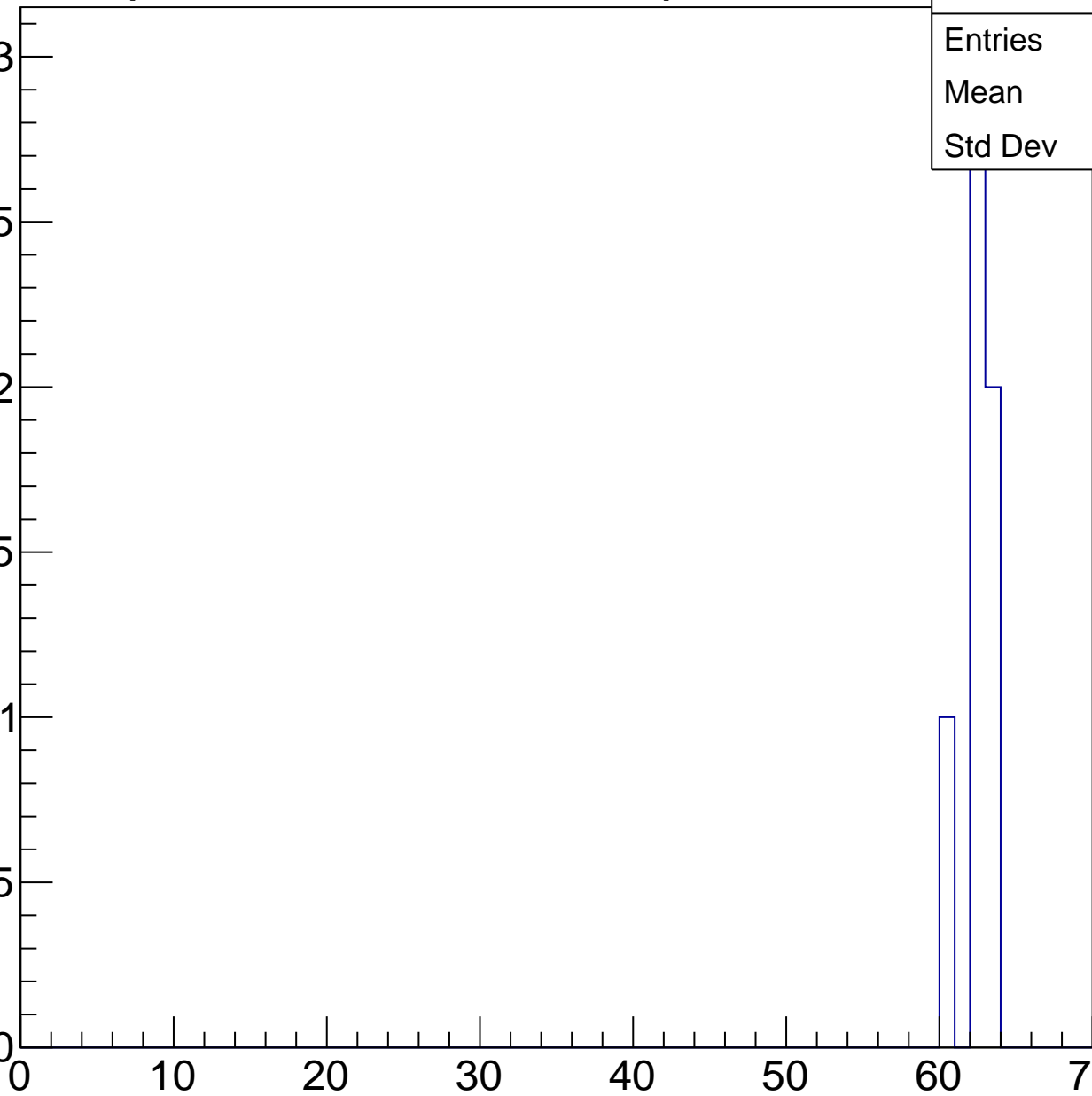
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

3  
2.5  
2  
1.5  
1  
0.5  
0

Entries	6
Mean	62
Std Dev	1

ampl





# B1L101S, U19-ch25, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U19-ch26, adc0

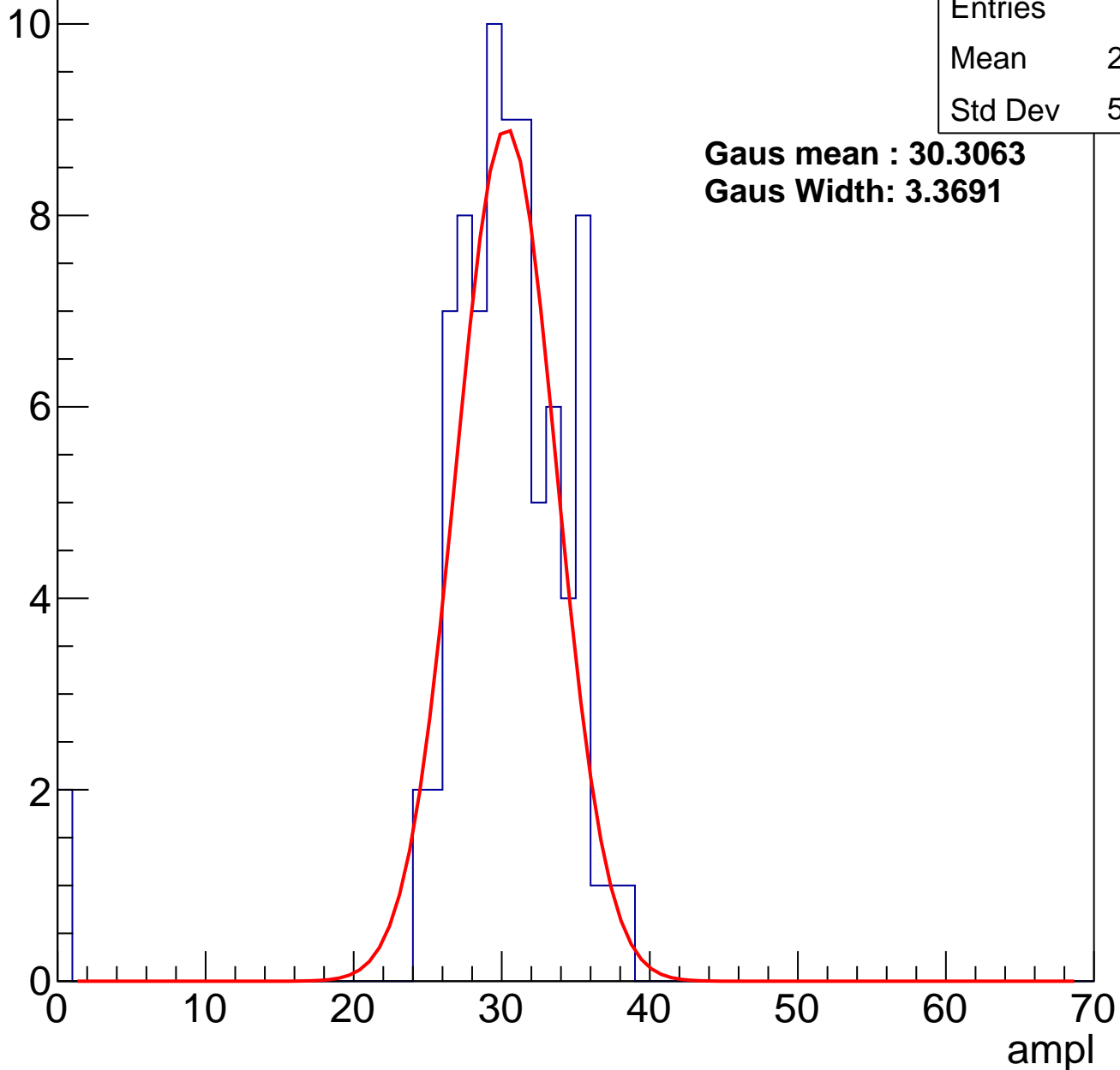
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	82
Mean	29.46
Std Dev	5.649

**Gaus mean : 30.3063**

**Gaus Width: 3.3691**

Entry



# B1L101S, U19-ch26, adc1

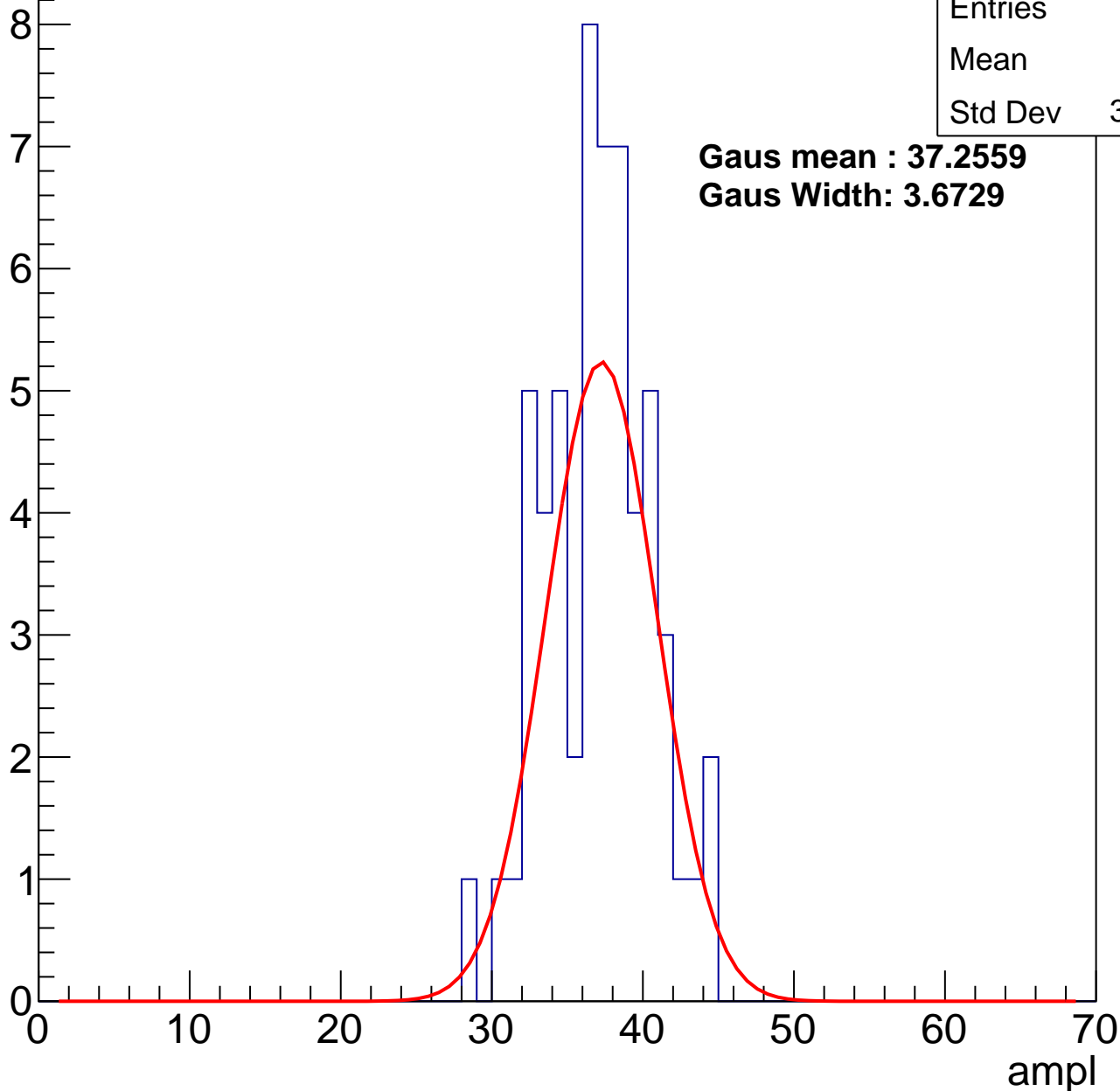
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	57
Mean	36.6
Std Dev	3.458

**Gaus mean : 37.2559**

**Gaus Width: 3.6729**



# B1L101S, U19-ch26, adc2

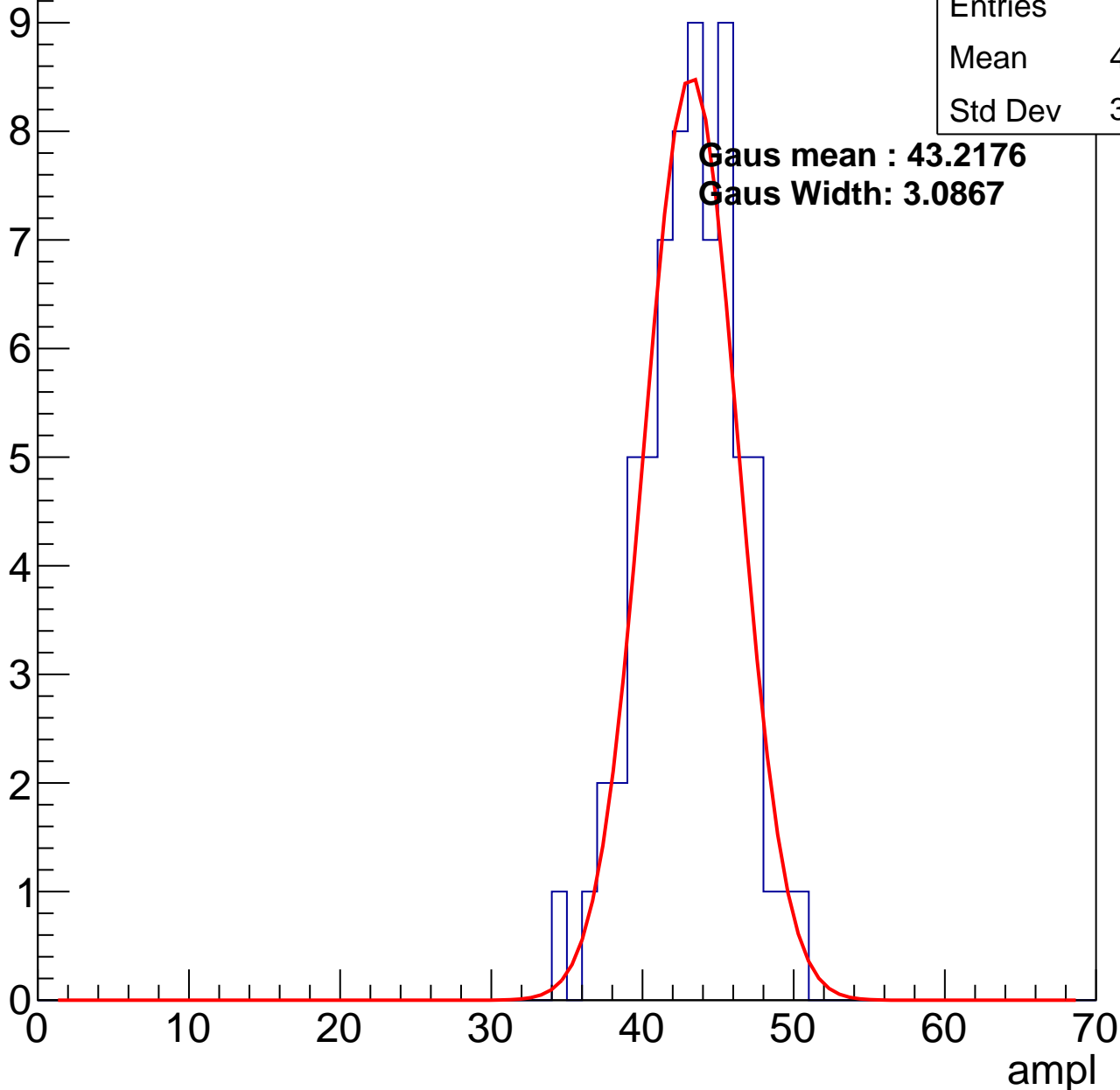
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	42.75
Std Dev	3.155

**Gaus mean : 43.2176**

**Gaus Width: 3.0867**

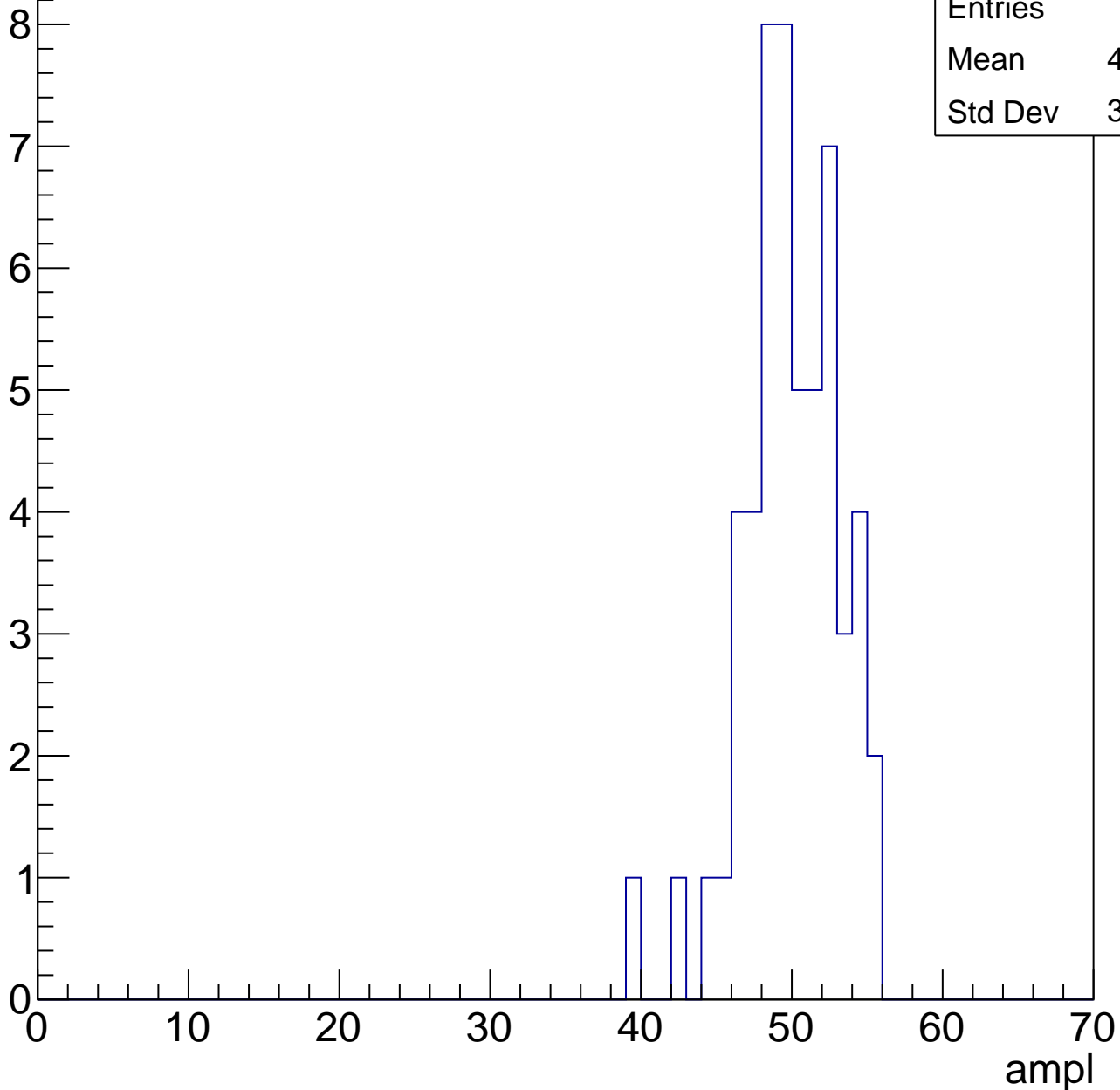


# B1L101S, U19-ch26, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	54
Mean	49.48
Std Dev	3.178

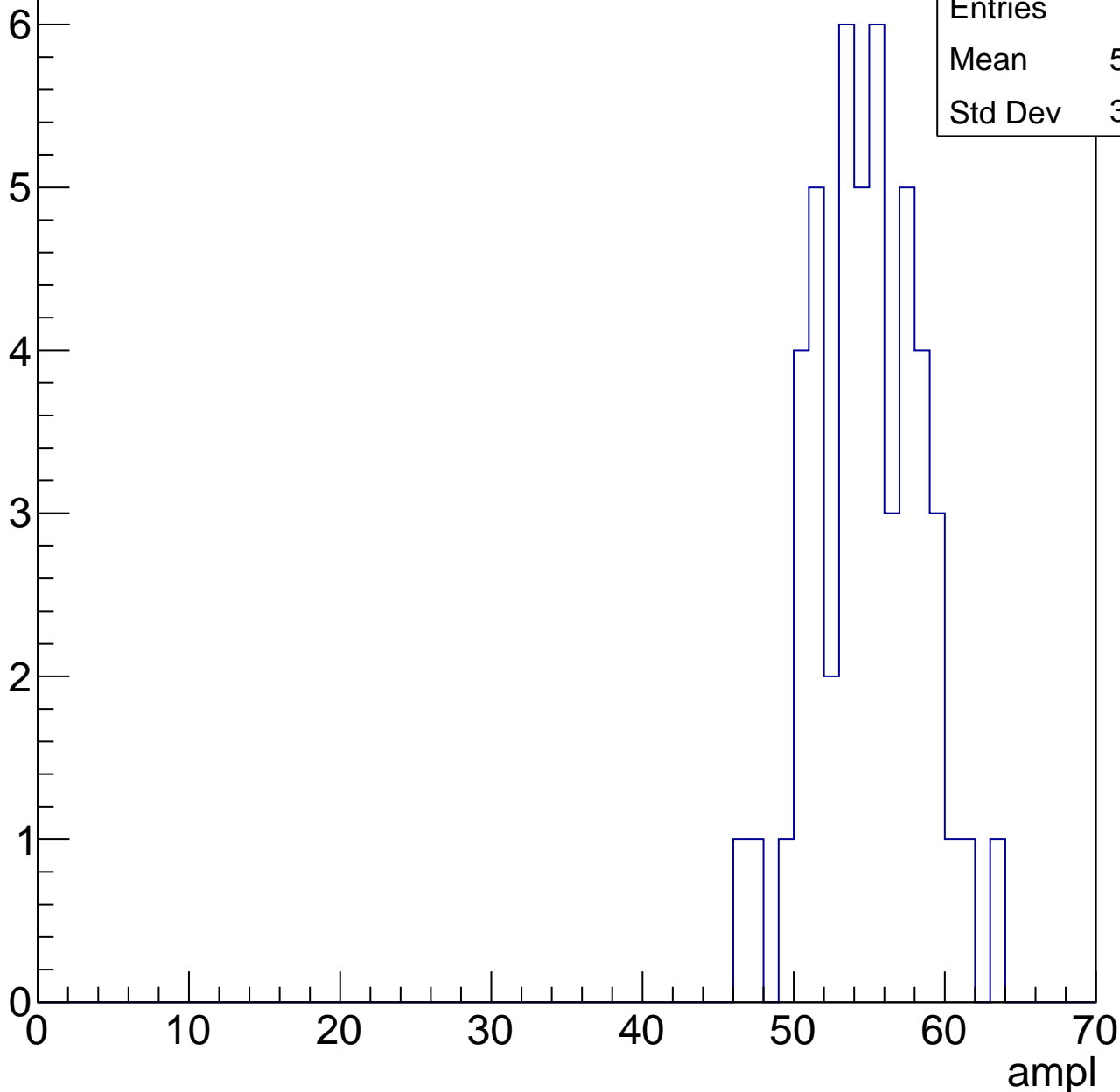


# B1L101S, U19-ch26, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	49
Mean	54.39
Std Dev	3.562



# B1L101S, U19-ch26, adc5

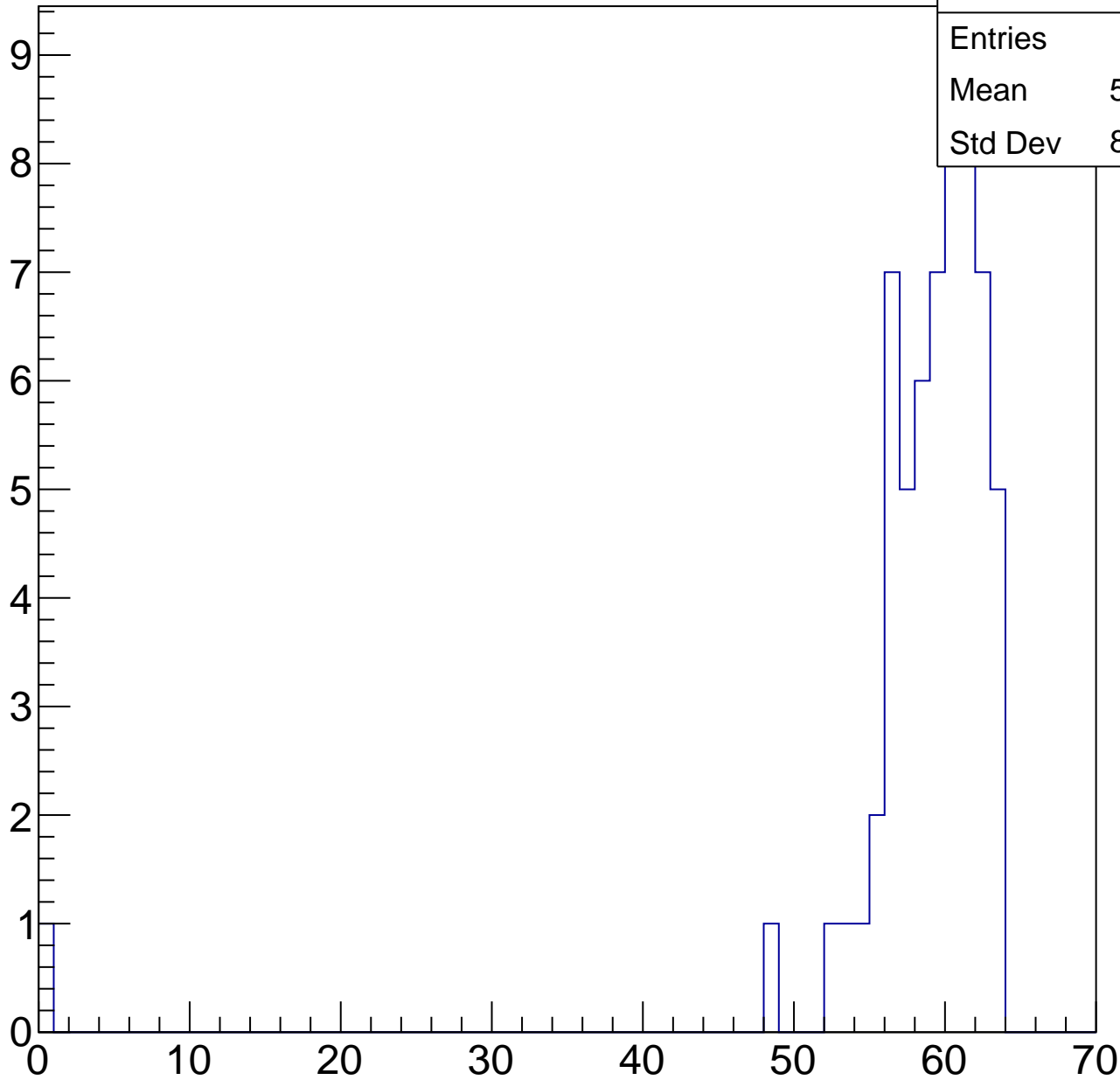
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	61
Mean	57.92
Std Dev	8.046

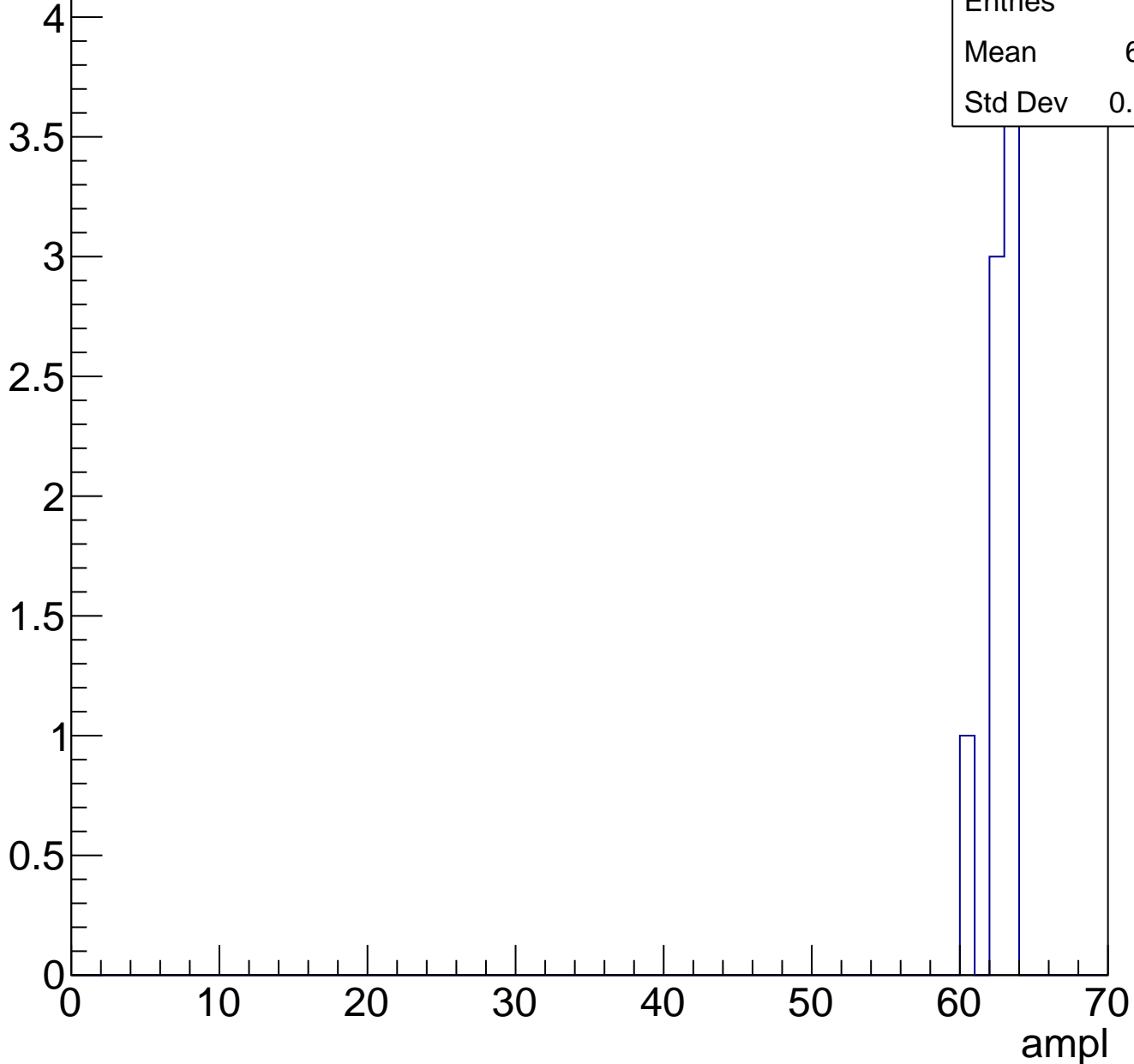
ampl



# B1L101S, U19-ch26, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U19-ch26, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U19-ch27, adc0

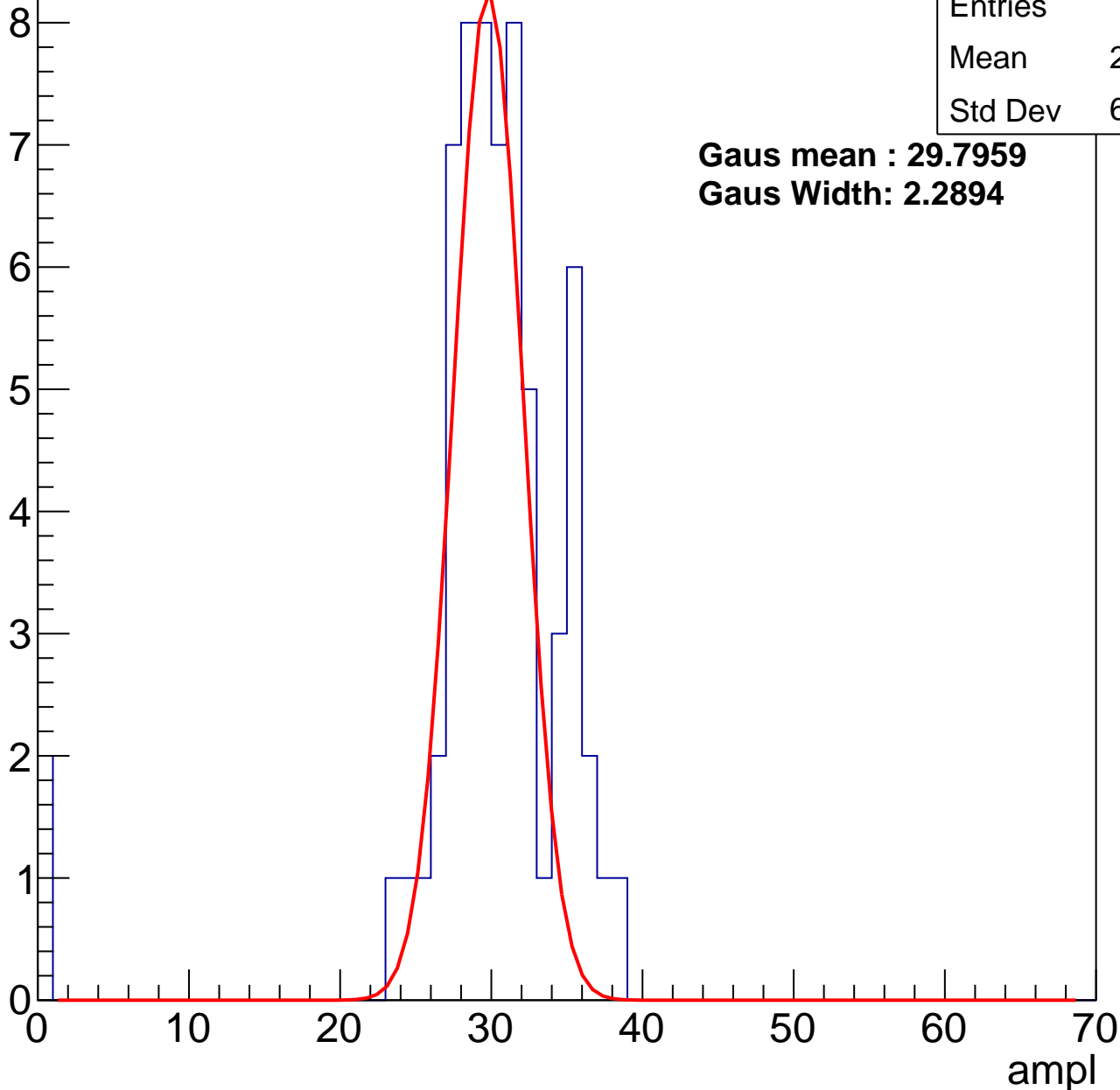
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	29.36
Std Dev	6.173

**Gaus mean : 29.7959**

**Gaus Width: 2.2894**



# B1L101S, U19-ch27, adc1

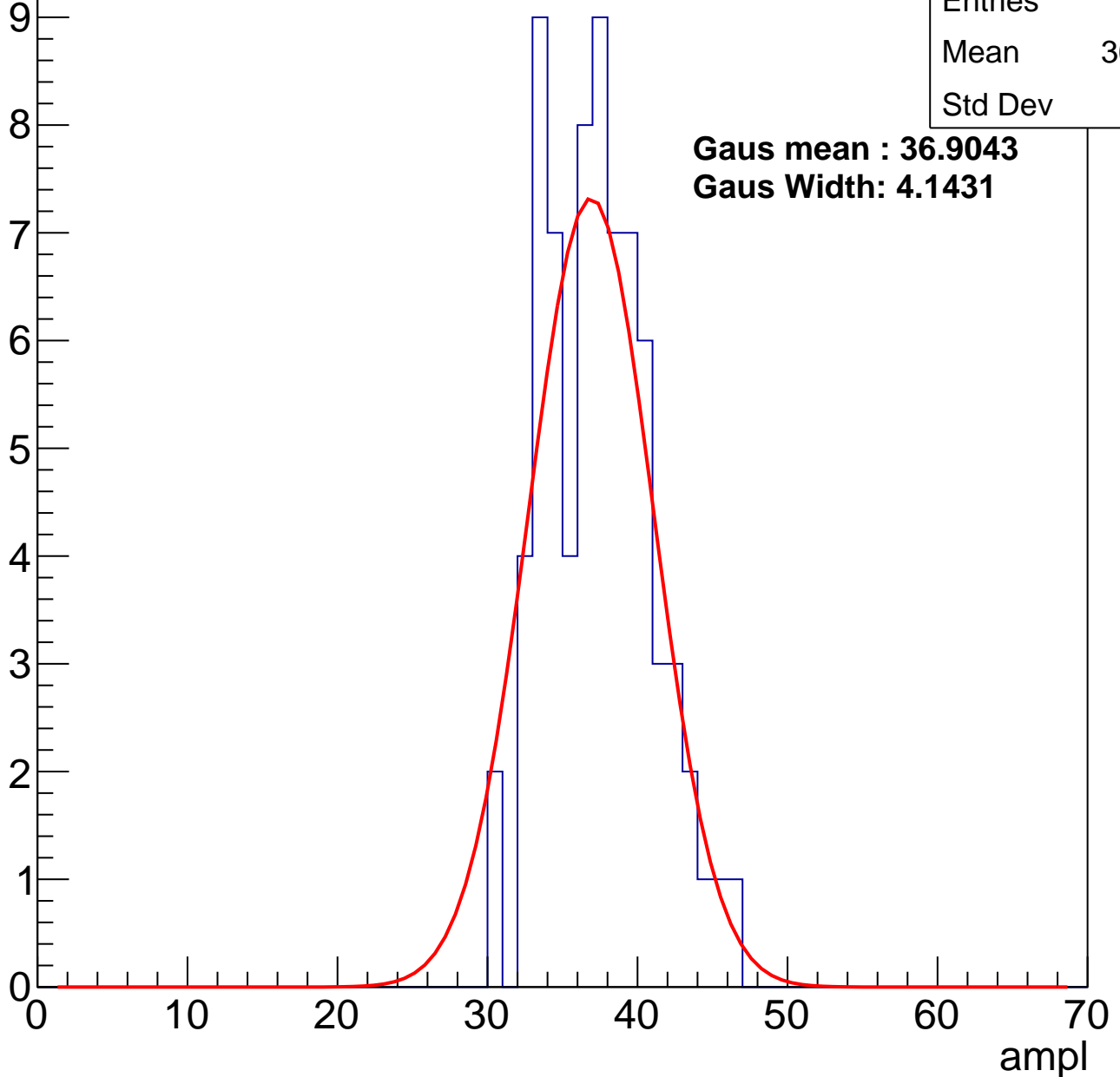
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	74
Mean	36.93
Std Dev	3.5

**Gaus mean : 36.9043**

**Gaus Width: 4.1431**



# B1L101S, U19-ch27, adc2

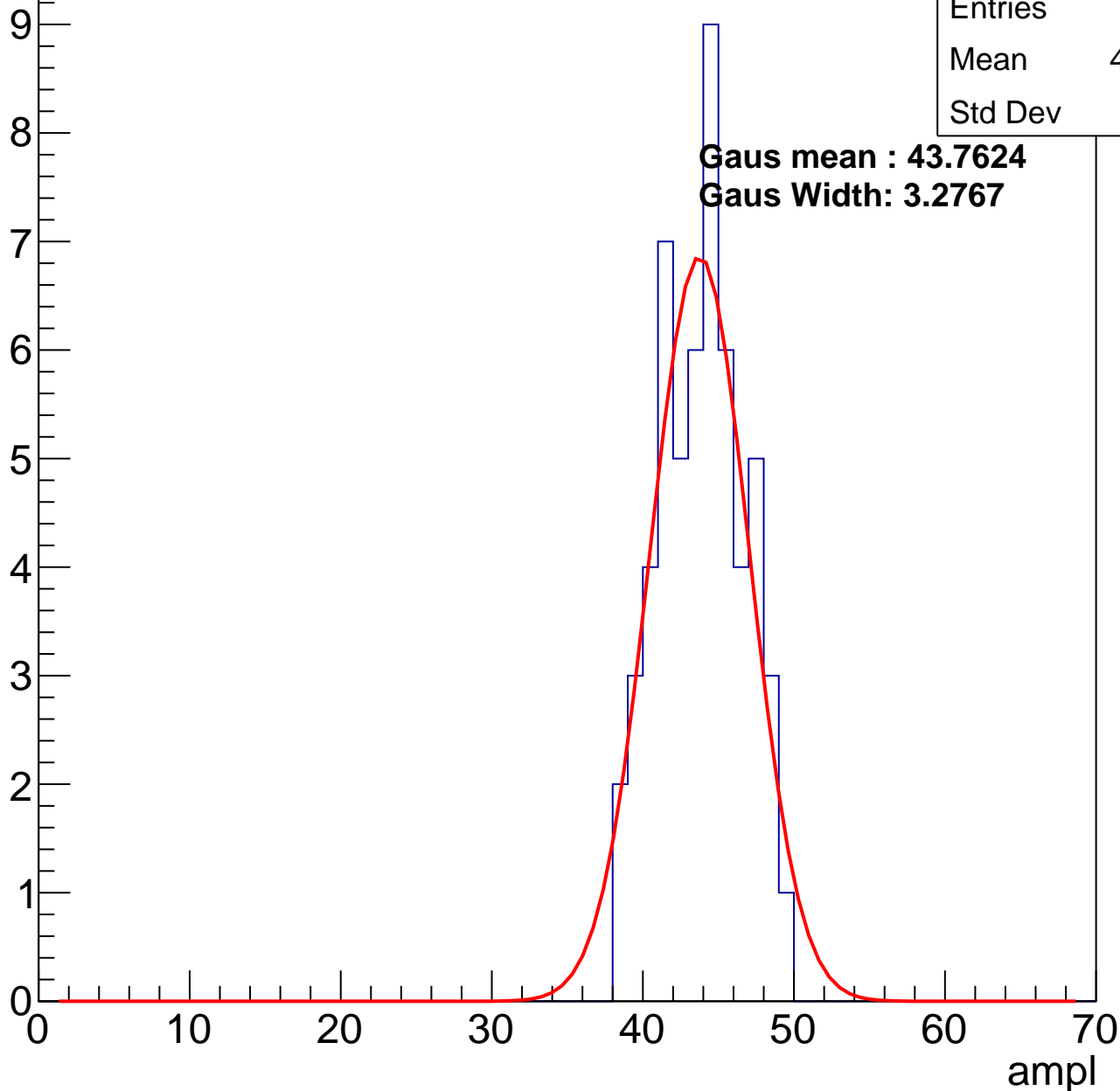
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	55
Mean	43.38
Std Dev	2.76

**Gaus mean : 43.7624**

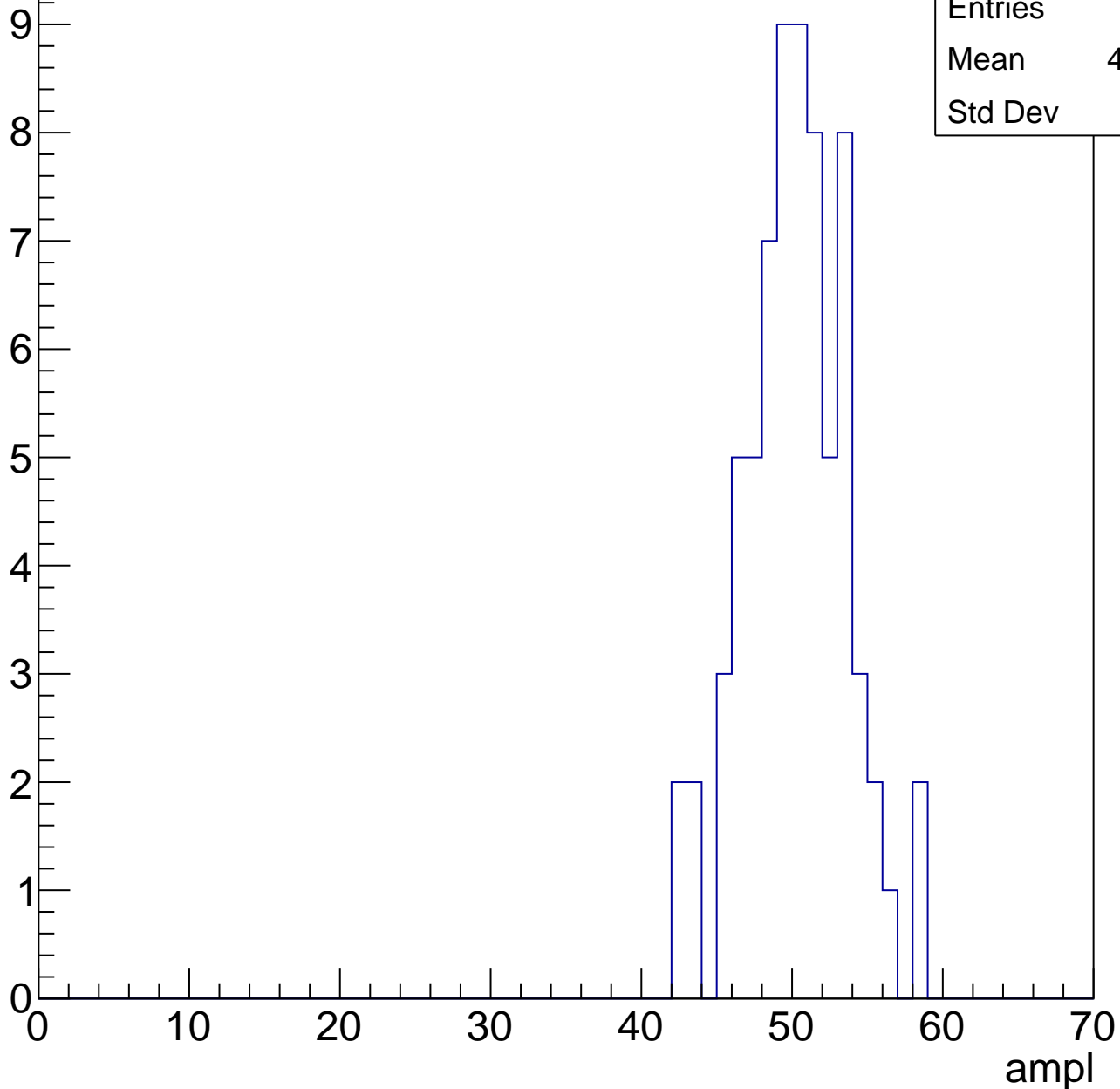
**Gaus Width: 3.2767**



# B1L101S, U19-ch27, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

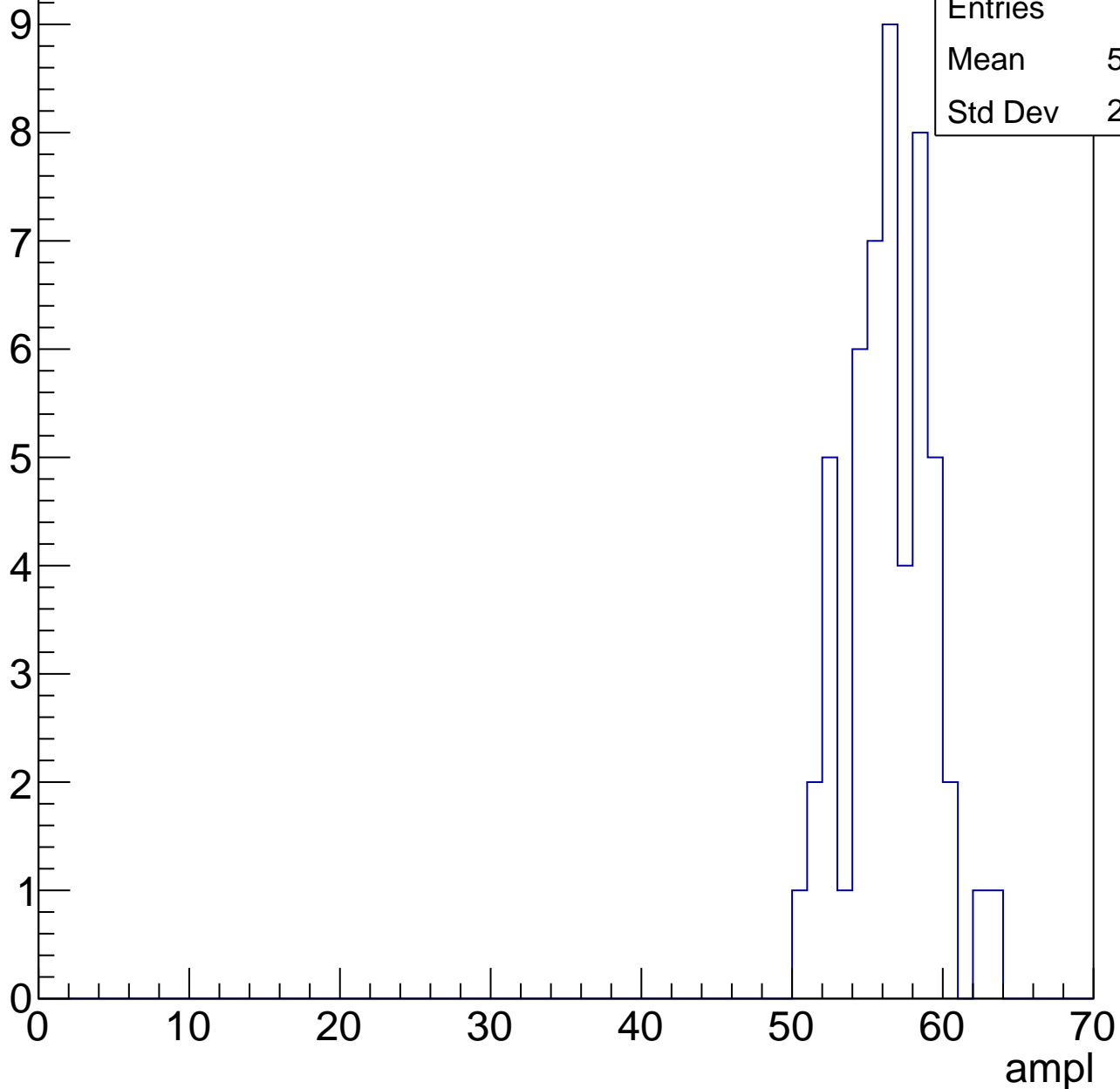
Entry



# B1L101S, U19-ch27, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

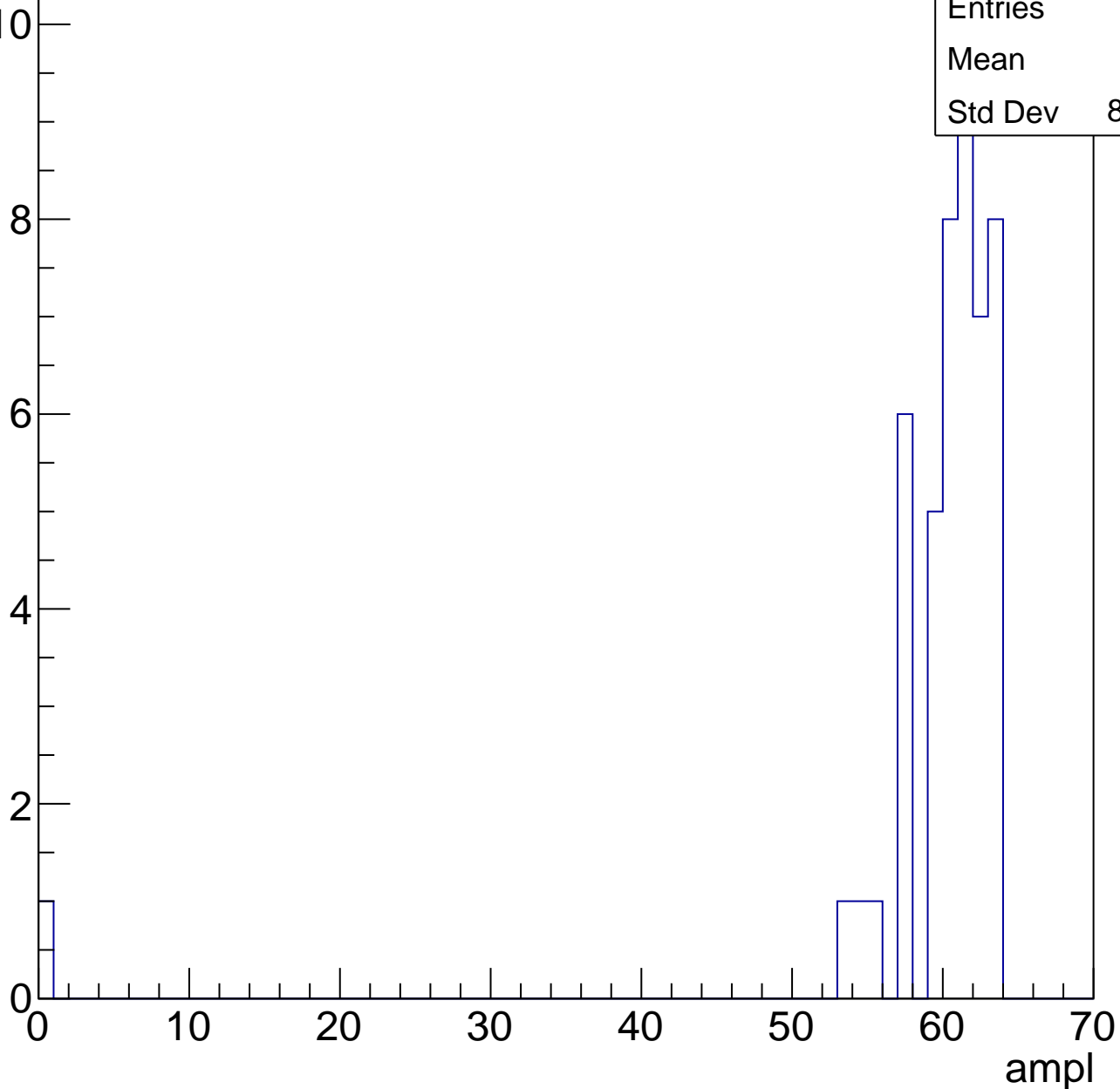


# B1L101S, U19-ch27, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	48
Mean	58.9
Std Dev	8.922



# B1L101S, U19-ch27, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U19-ch27, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U19-ch28, adc0

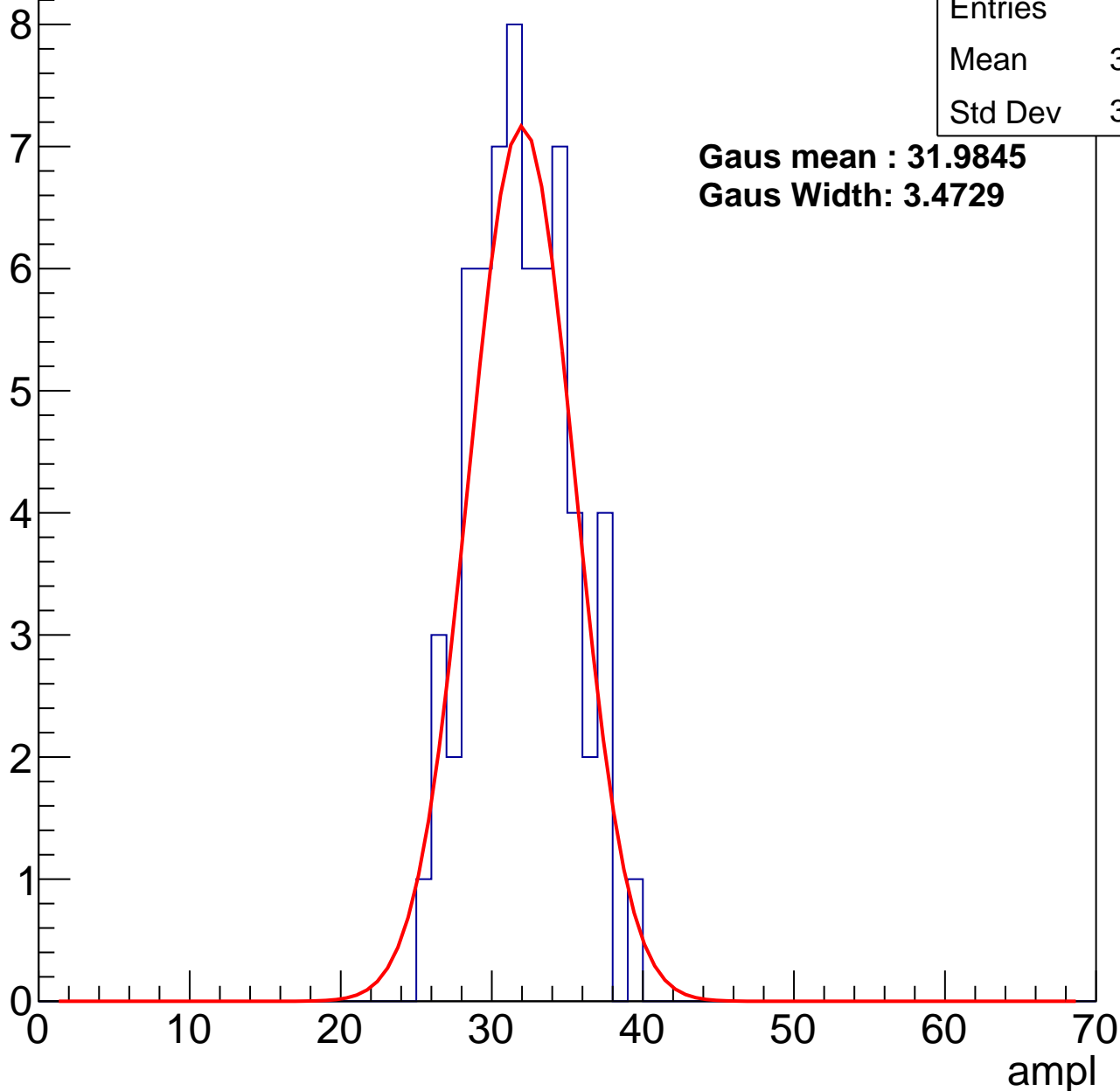
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	31.49
Std Dev	3.157

**Gaus mean : 31.9845**

**Gaus Width: 3.4729**



# B1L101S, U19-ch28, adc1

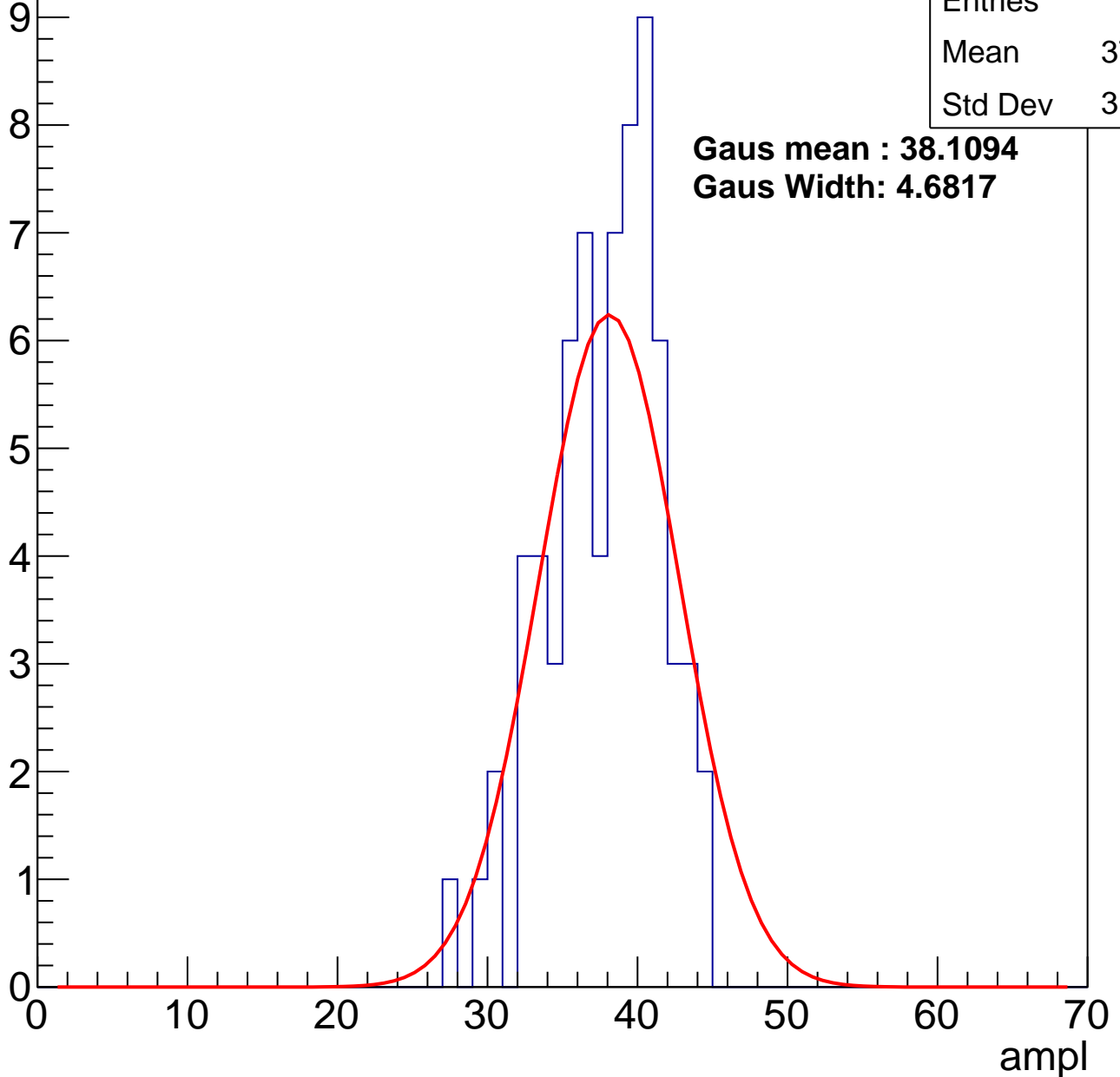
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	37.36
Std Dev	3.726

**Gaus mean : 38.1094**

**Gaus Width: 4.6817**



# B1L101S, U19-ch28, adc2

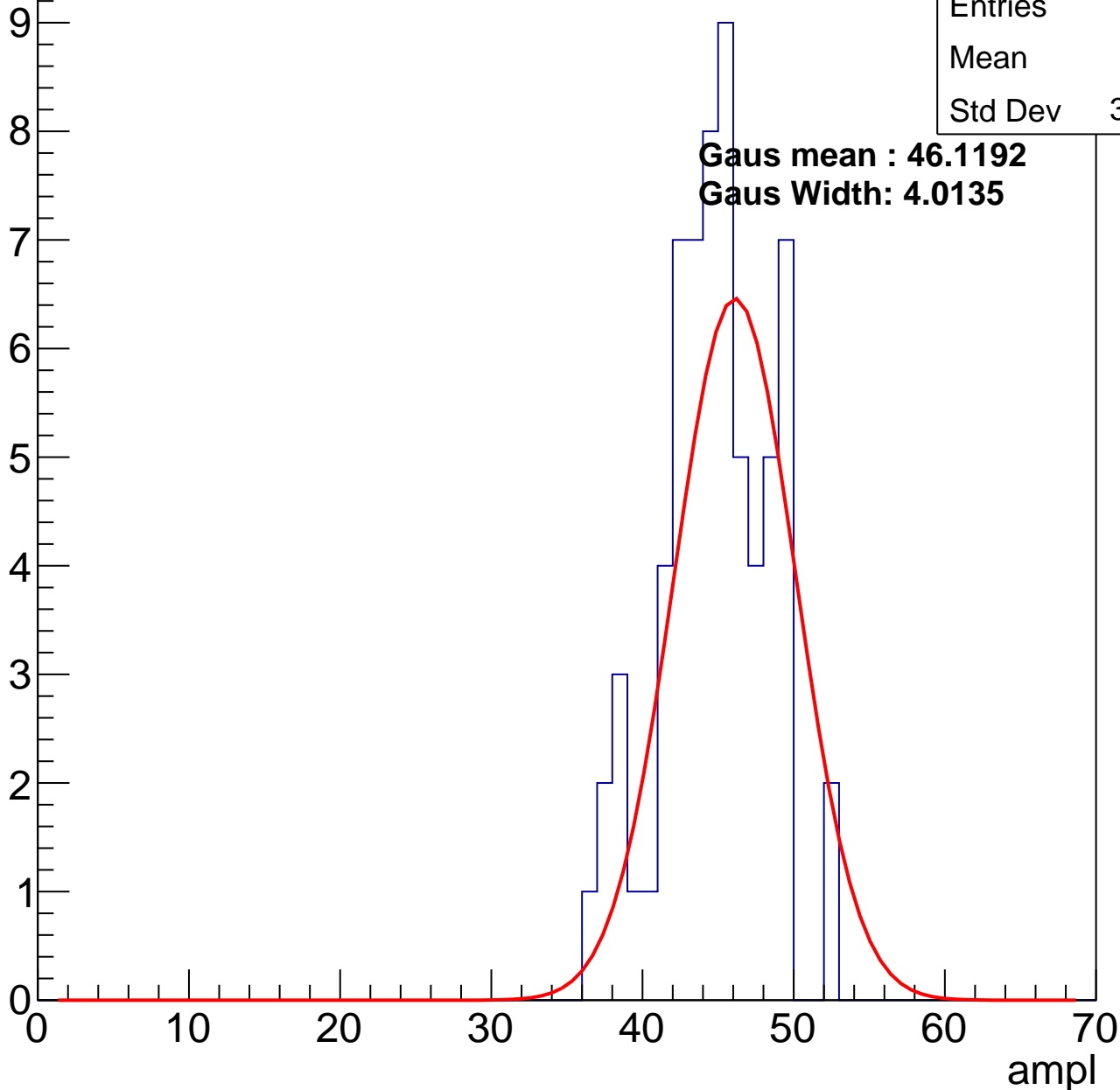
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	66
Mean	44.3
Std Dev	3.533

**Gaus mean : 46.1192**

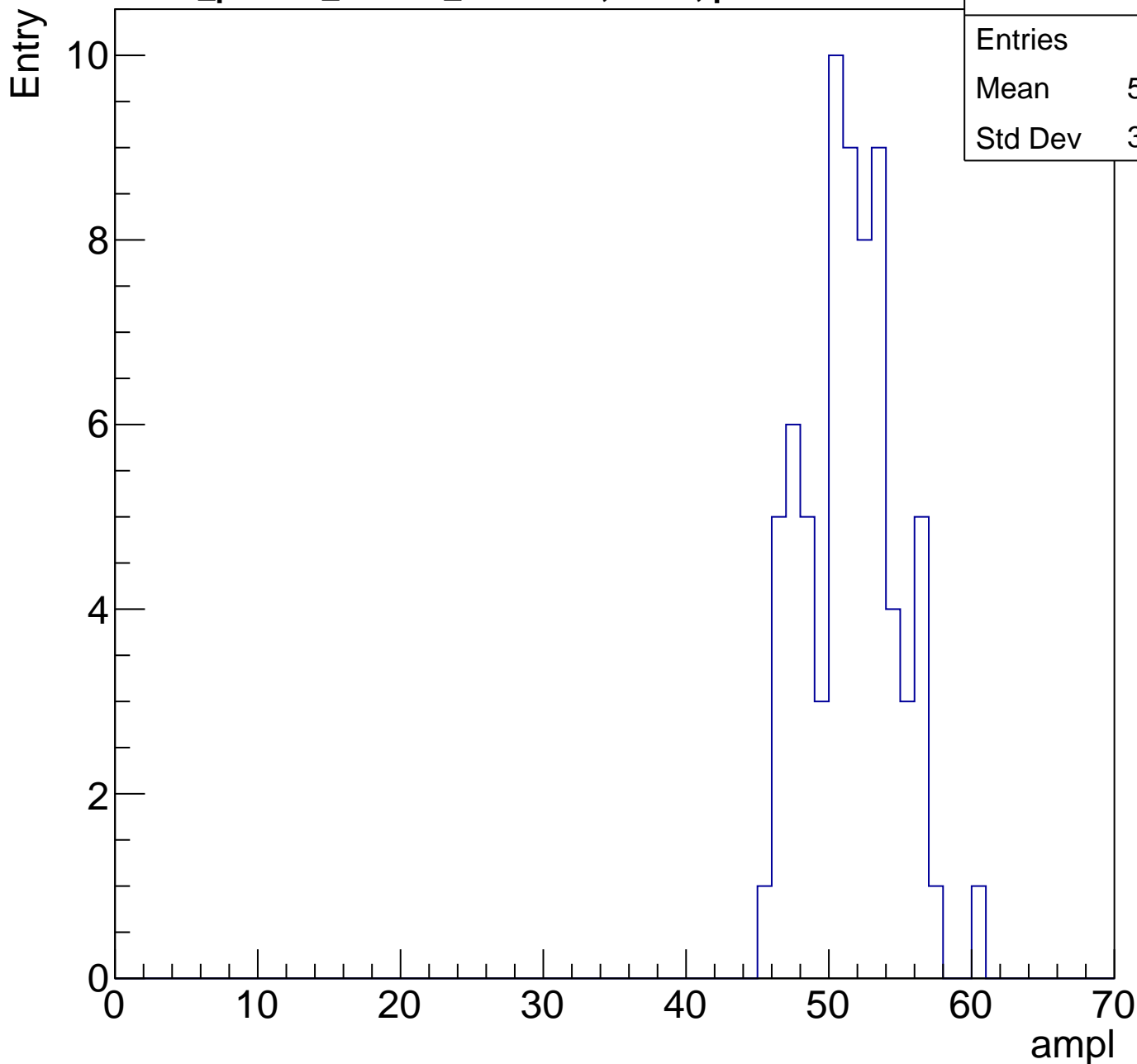
**Gaus Width: 4.0135**



# B1L101S, U19-ch28, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	70
Mean	51.06
Std Dev	3.148

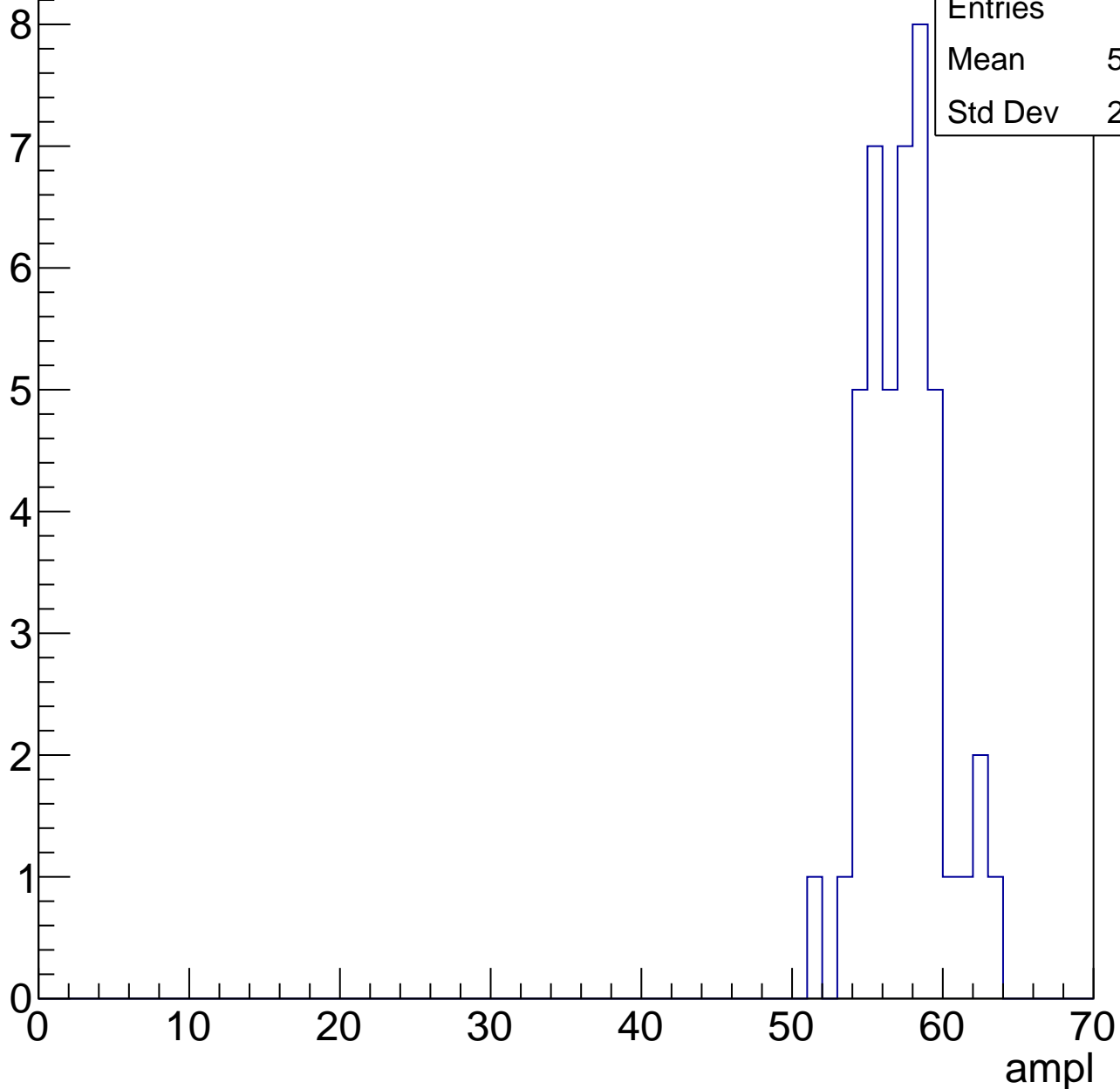


# B1L101S, U19-ch28, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	44
Mean	56.93
Std Dev	2.472



# B1L101S, U19-ch28, adc5

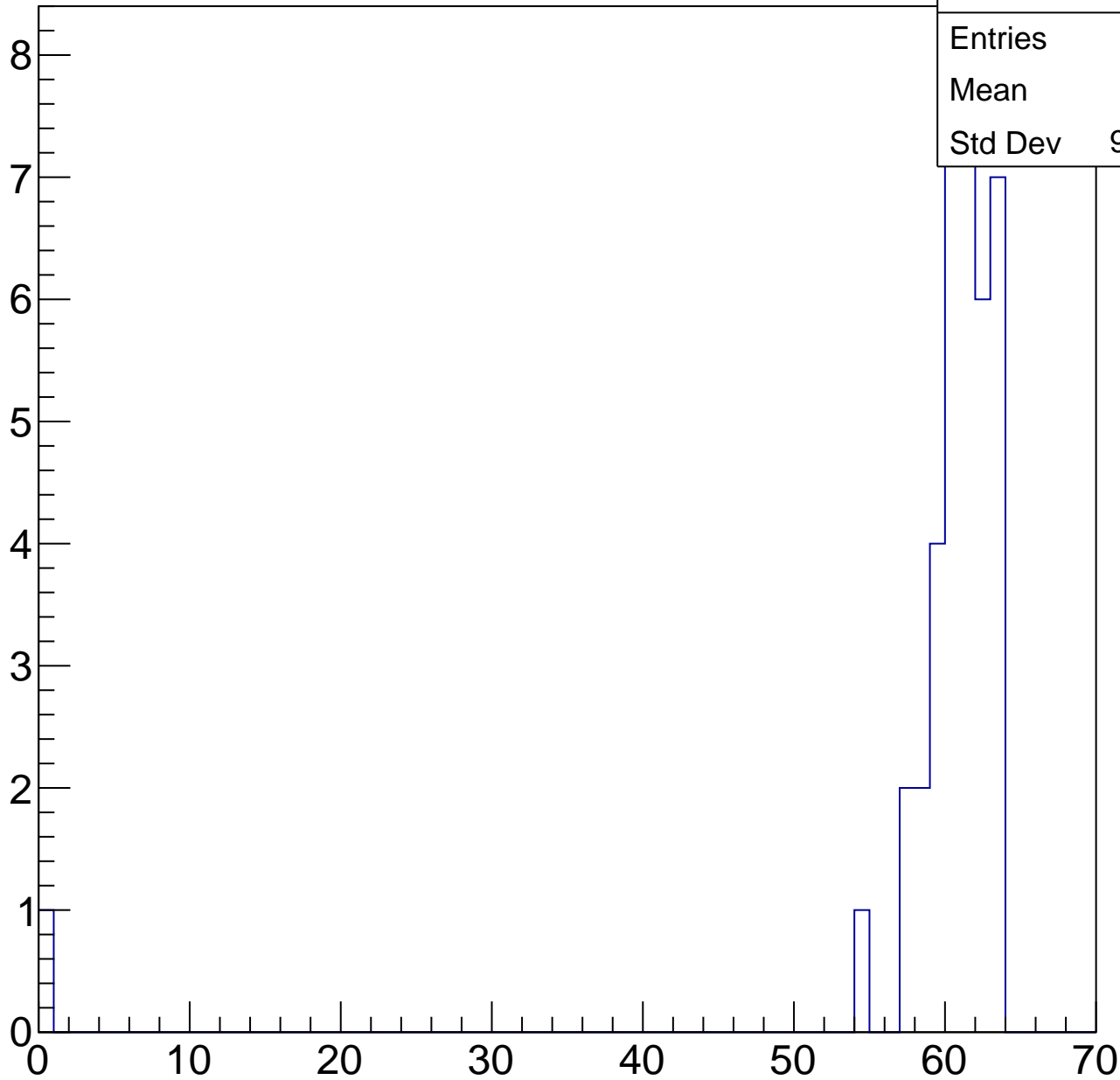
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	39
Mean	59
Std Dev	9.769

ampl



# B1L101S, U19-ch28, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	5
Mean	62.2
Std Dev	0.7483

ampl

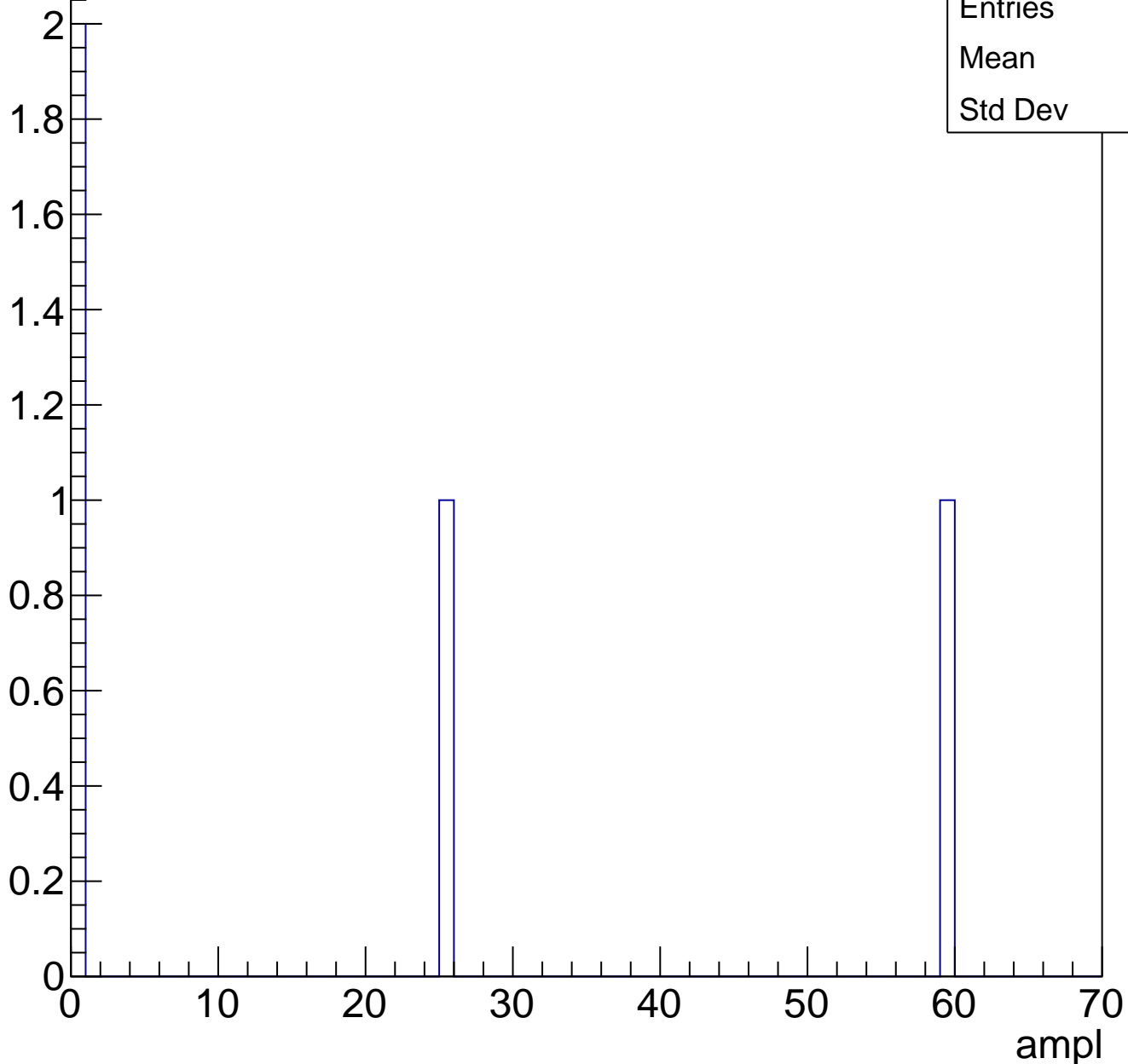
0 10 20 30 40 50 60 70



# B1L101S, U19-ch28, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	4
Mean	21
Std Dev	24.2

# B1L101S, U19-ch29, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	51
Mean	30.51
Std Dev	2.57

**Gaus mean : 30.9199**

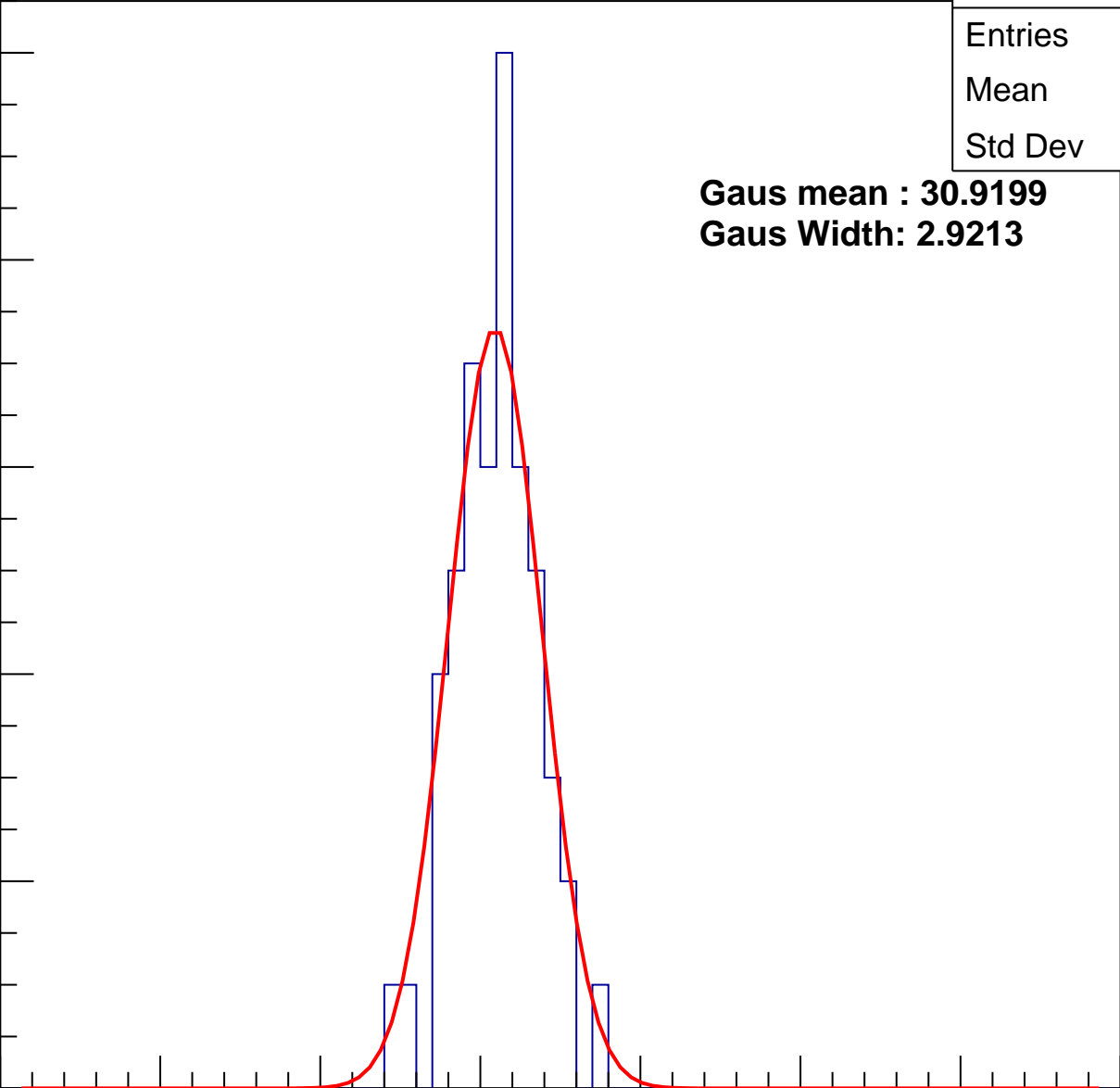
**Gaus Width: 2.9213**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U19-ch29, adc1

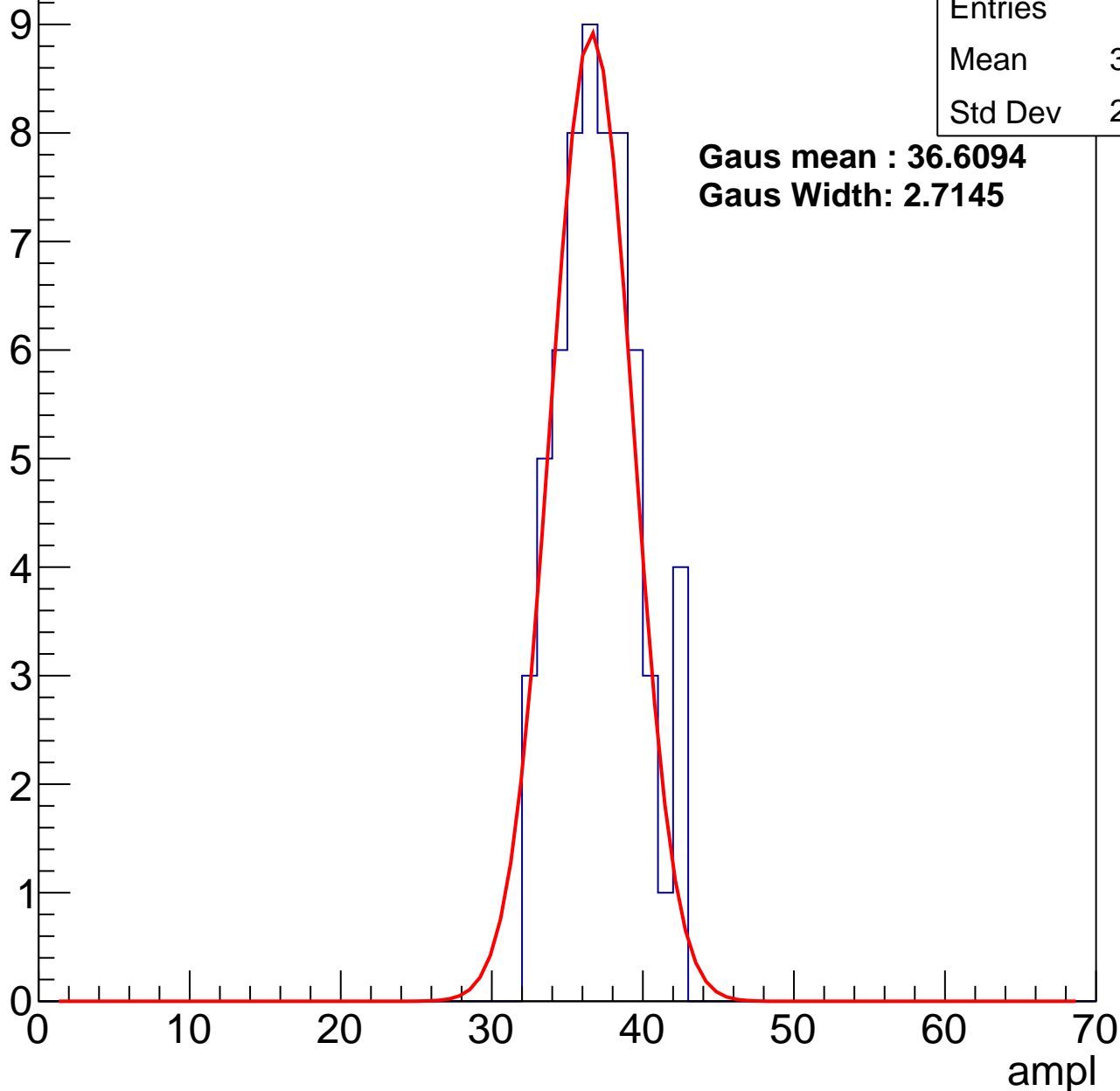
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	36.59
Std Dev	2.608

**Gaus mean : 36.6094**

**Gaus Width: 2.7145**



# B1L101S, U19-ch29, adc2

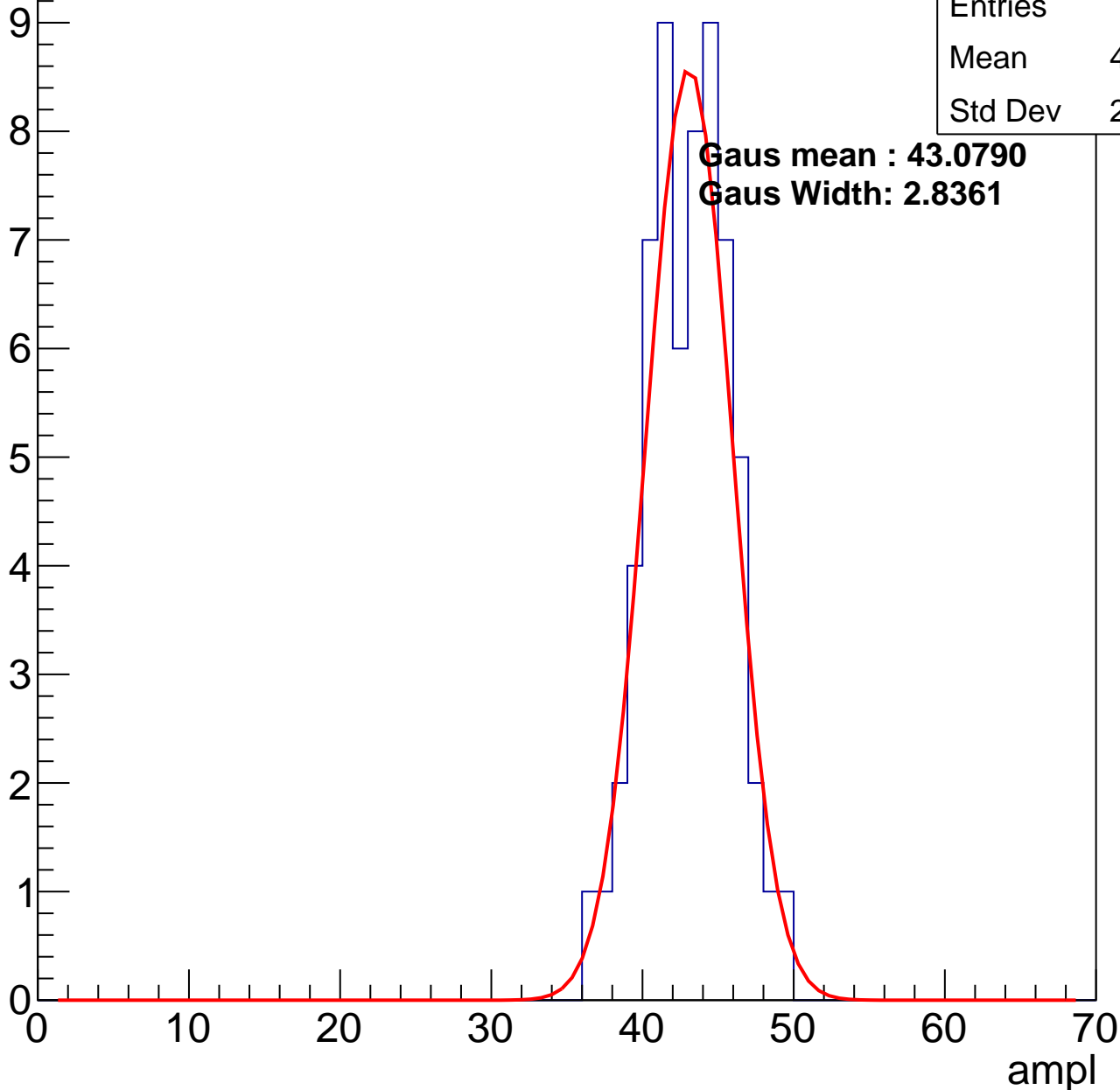
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	42.57
Std Dev	2.724

**Gaus mean : 43.0790**

**Gaus Width: 2.8361**

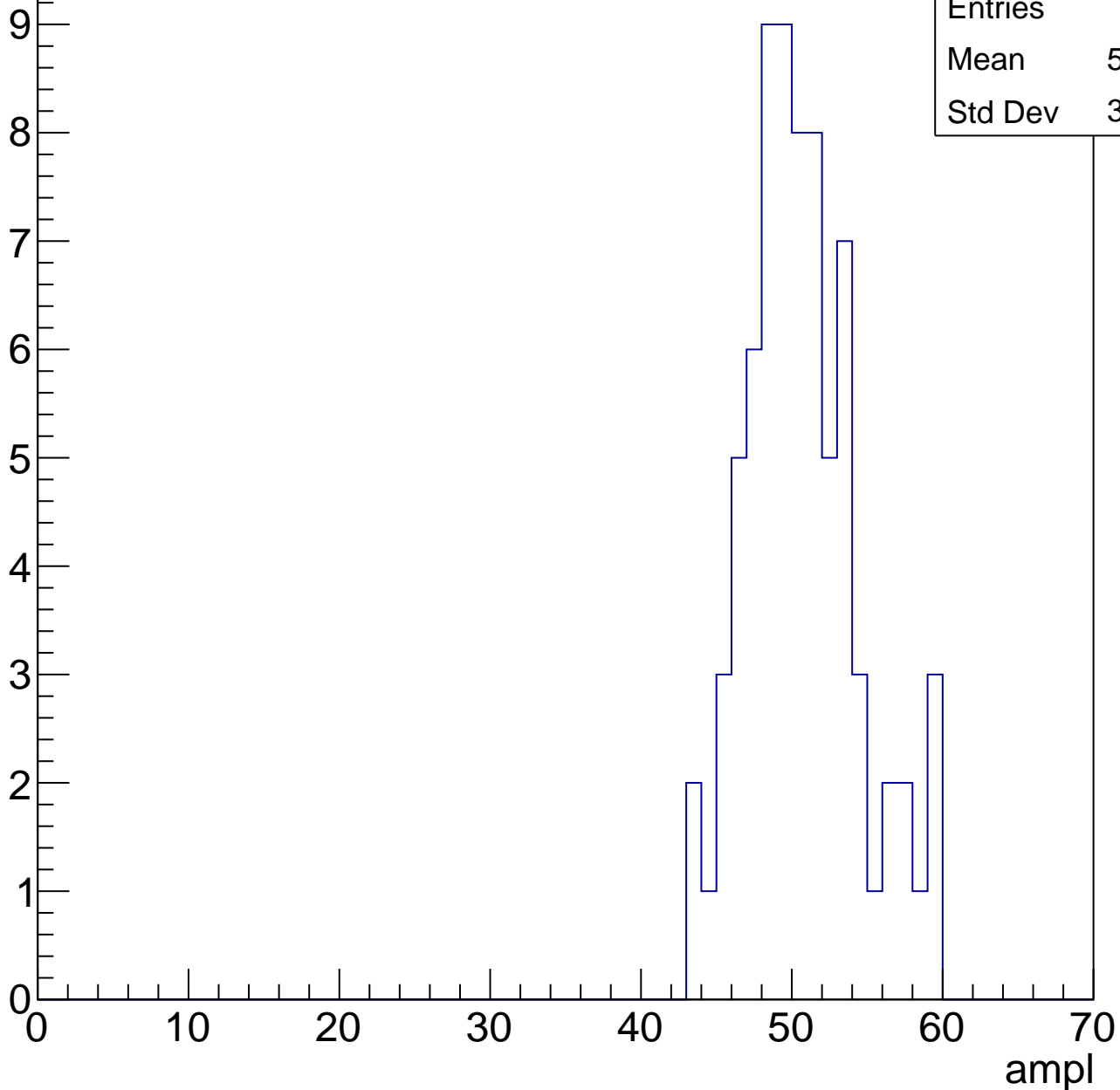


# B1L101S, U19-ch29, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

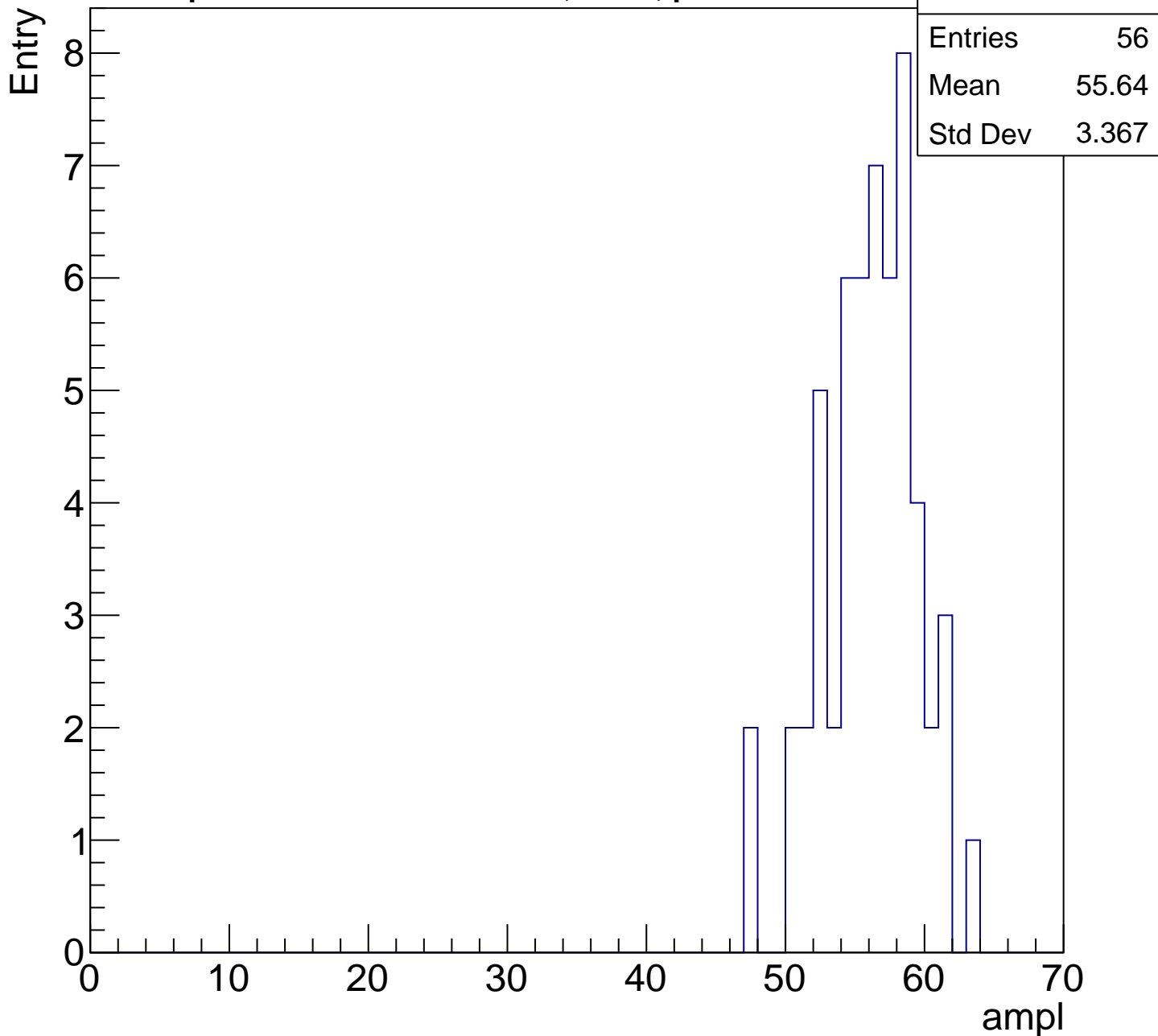
Entry

Entries	75
Mean	50.23
Std Dev	3.697



# B1L101S, U19-ch29, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U19-ch29, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

10

Entries 45

Mean 58.82

Std Dev 9.258

8

6

4

2

0

0

10

20

30

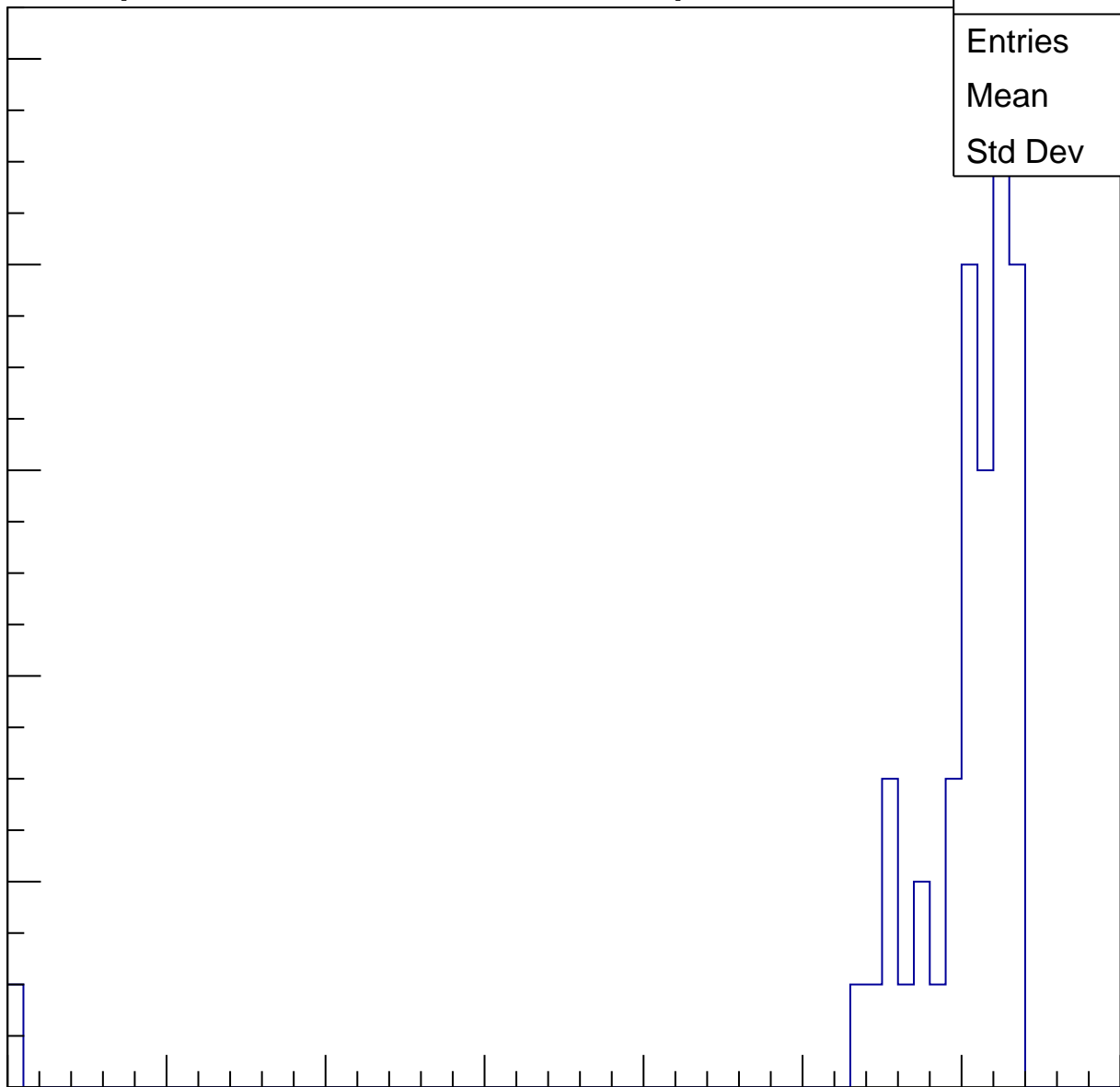
40

50

60

70

ampl



# B1L101S, U19-ch29, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U19-ch29, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L101S, U19-ch30, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	84
Mean	30.02
Std Dev	3.703

**Gaus mean : 31.1333**

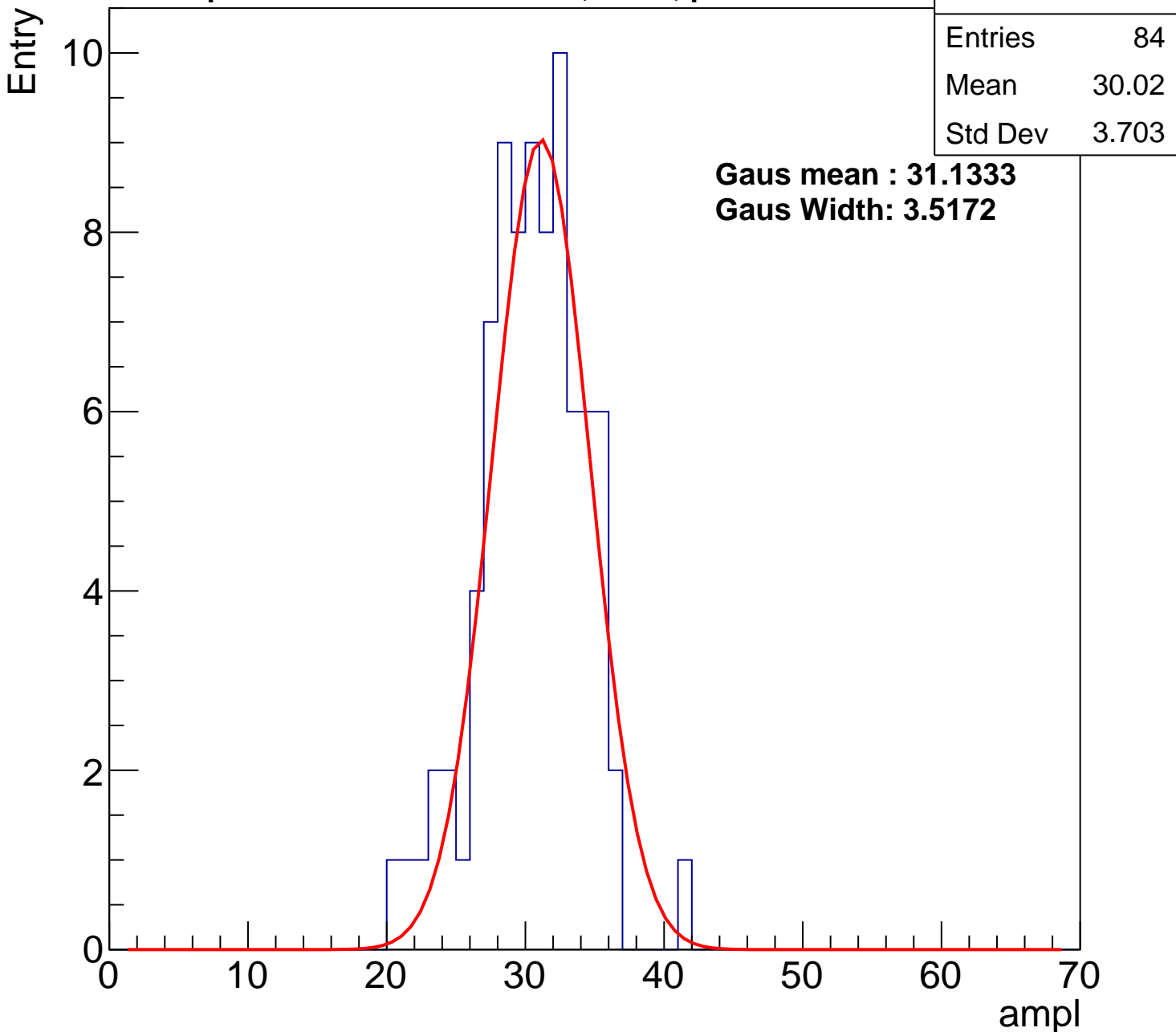
**Gaus Width: 3.5172**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U19-ch30, adc1

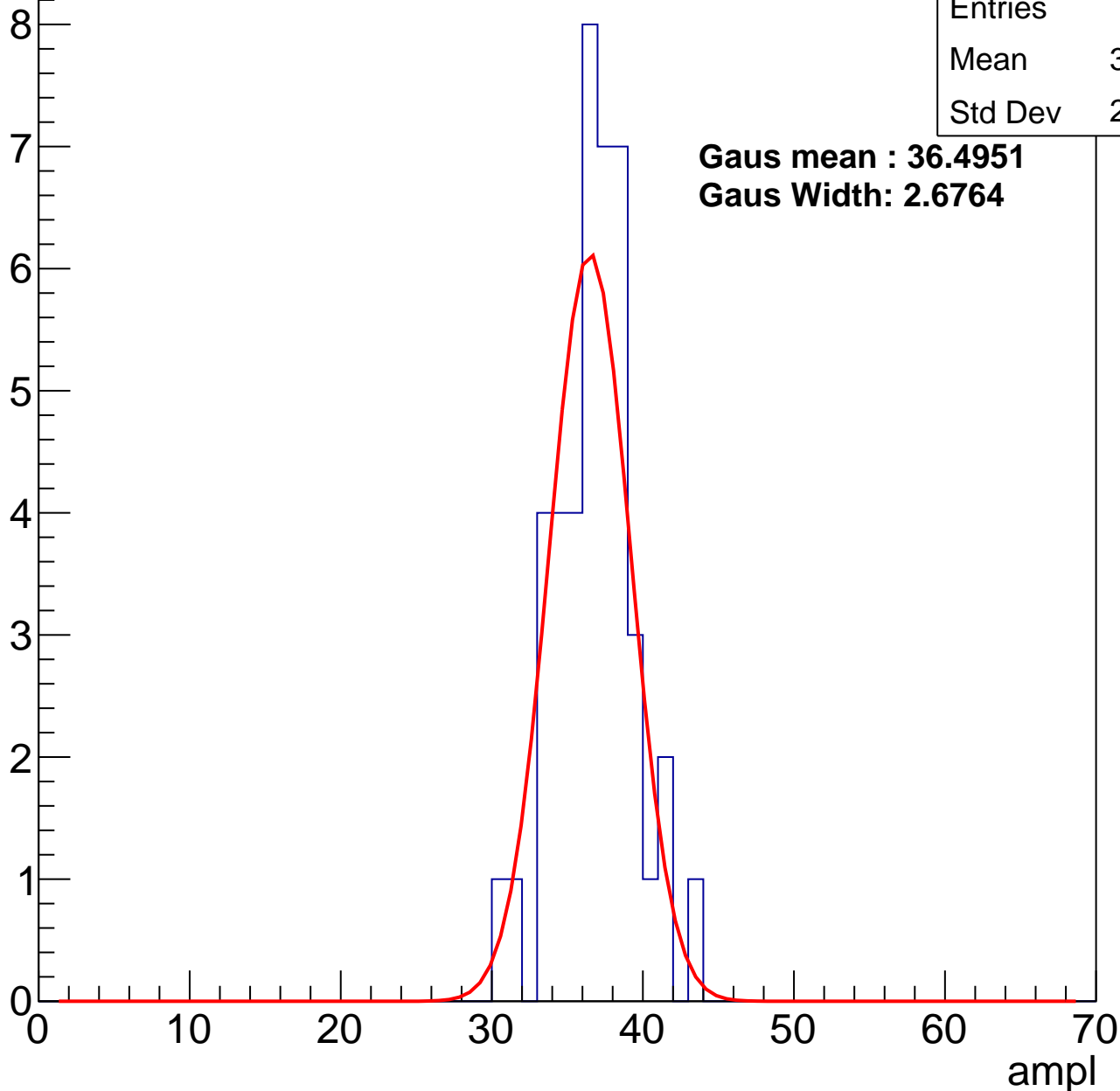
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	43
Mean	36.37
Std Dev	2.588

**Gaus mean : 36.4951**

**Gaus Width: 2.6764**



# B1L101S, U19-ch30, adc2

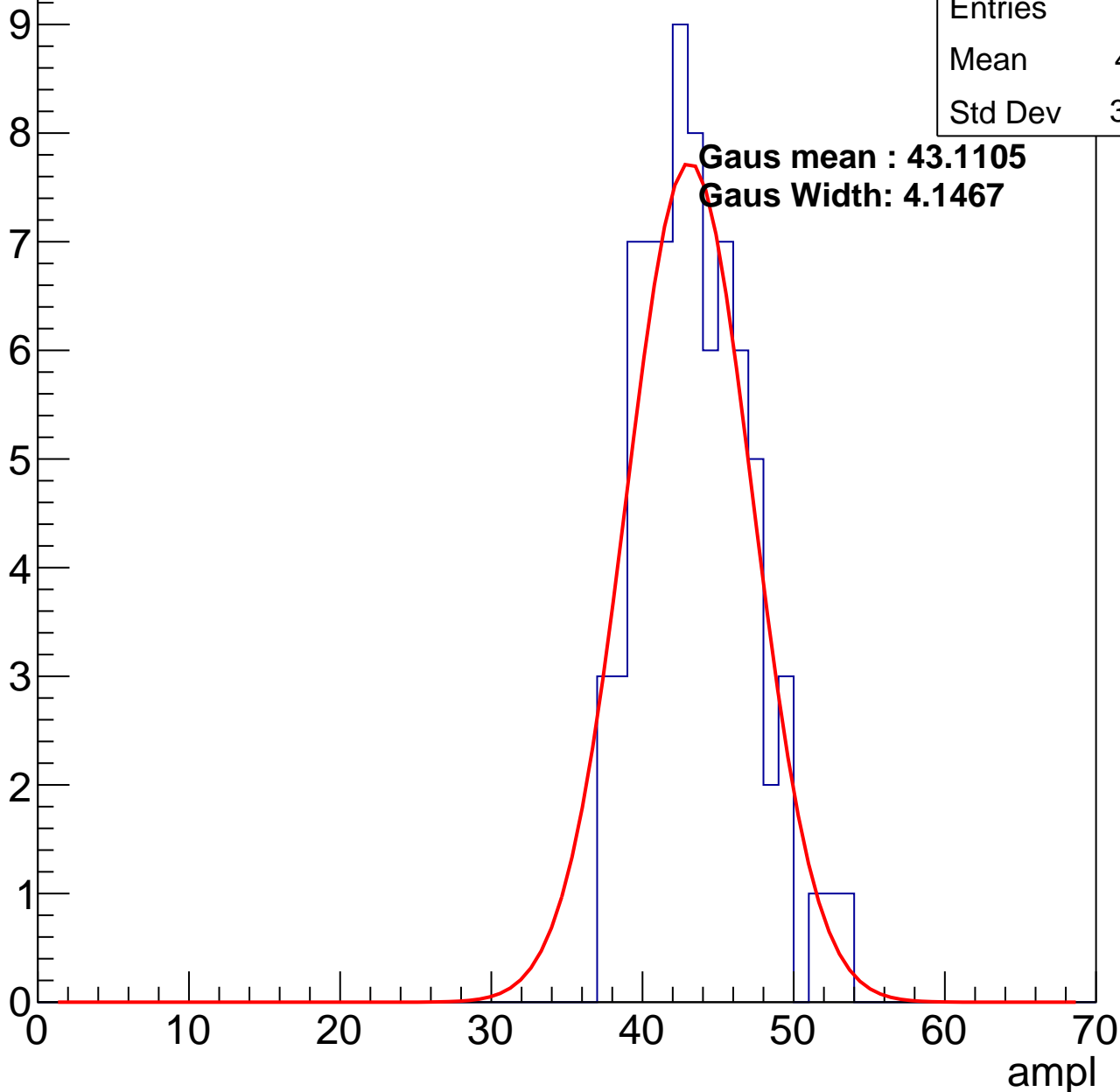
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	76
Mean	43.11
Std Dev	3.564

**Gaus mean : 43.1105**

**Gaus Width: 4.1467**

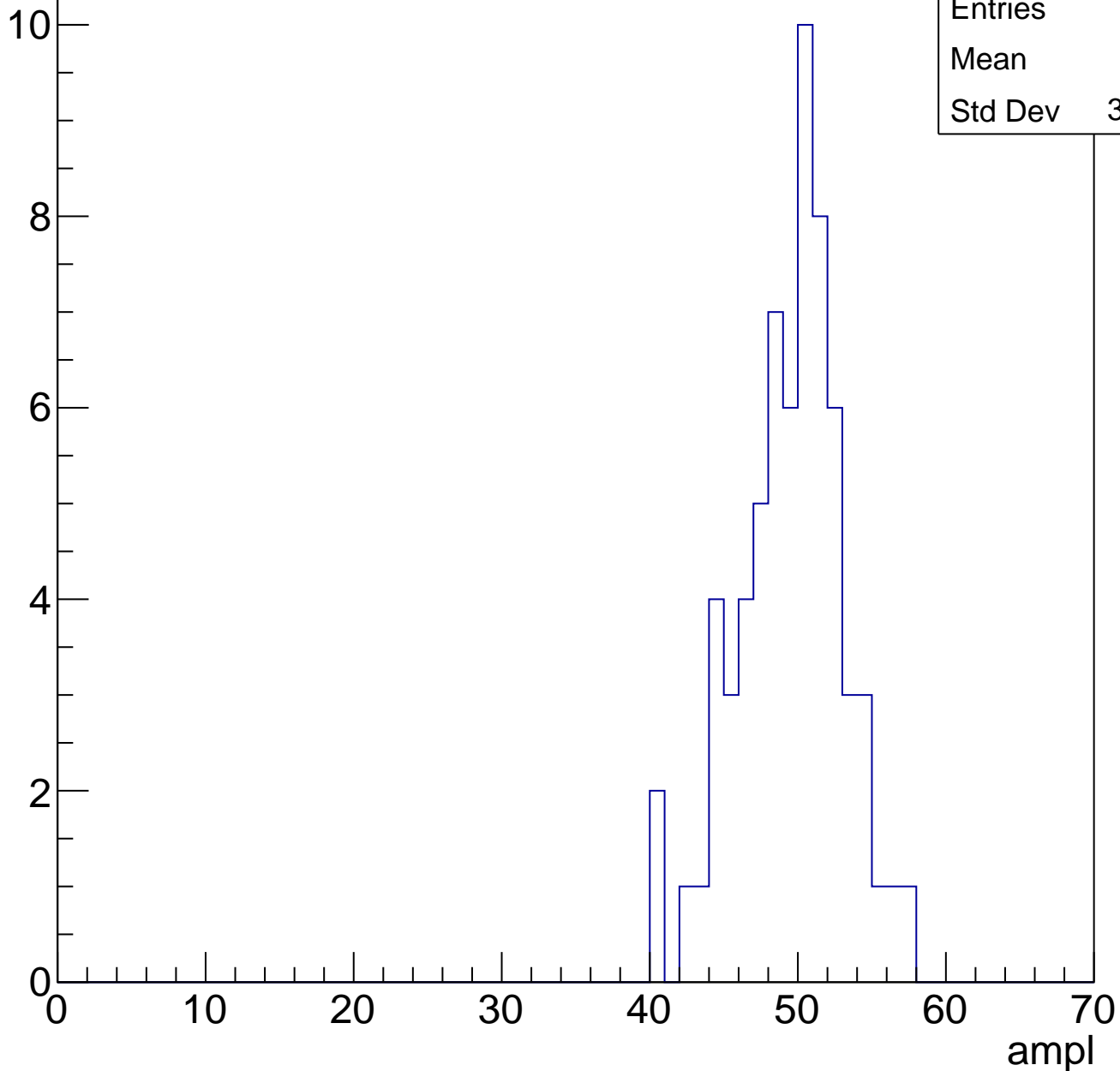


# B1L101S, U19-ch30, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	66
Mean	49
Std Dev	3.538

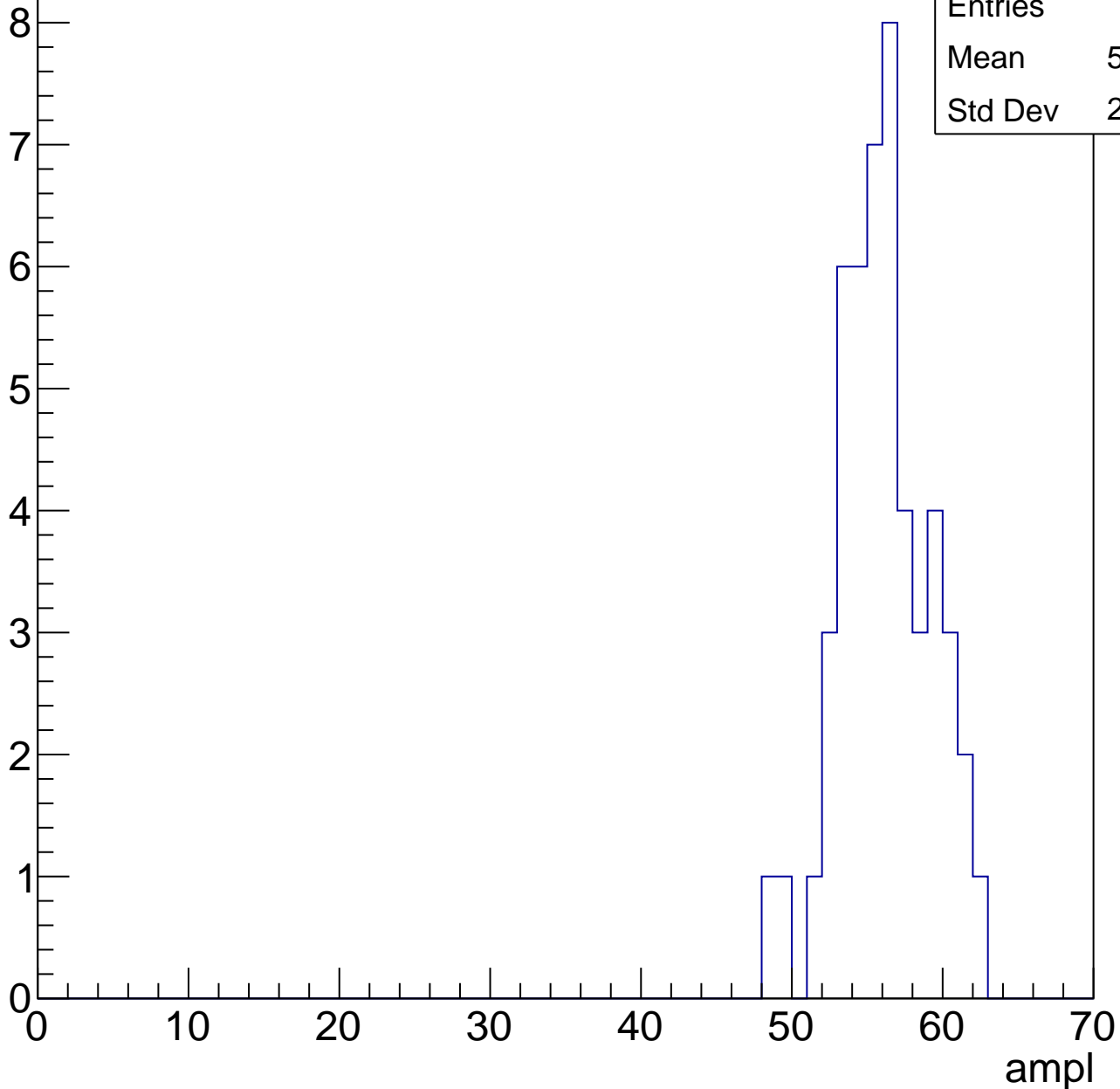


# B1L101S, U19-ch30, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	50
Mean	55.62
Std Dev	2.999

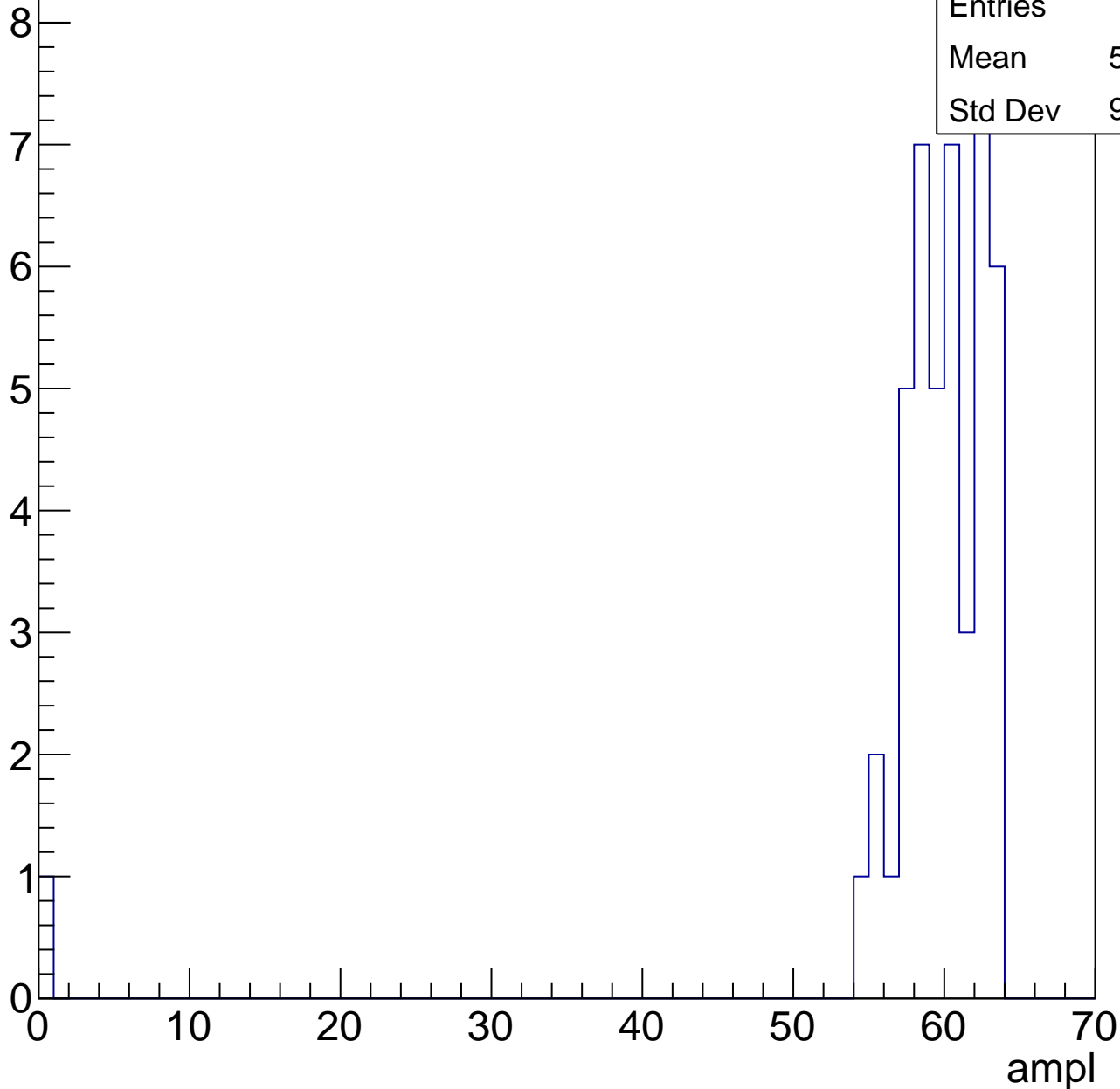


# B1L101S, U19-ch30, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	46
Mean	58.33
Std Dev	9.017

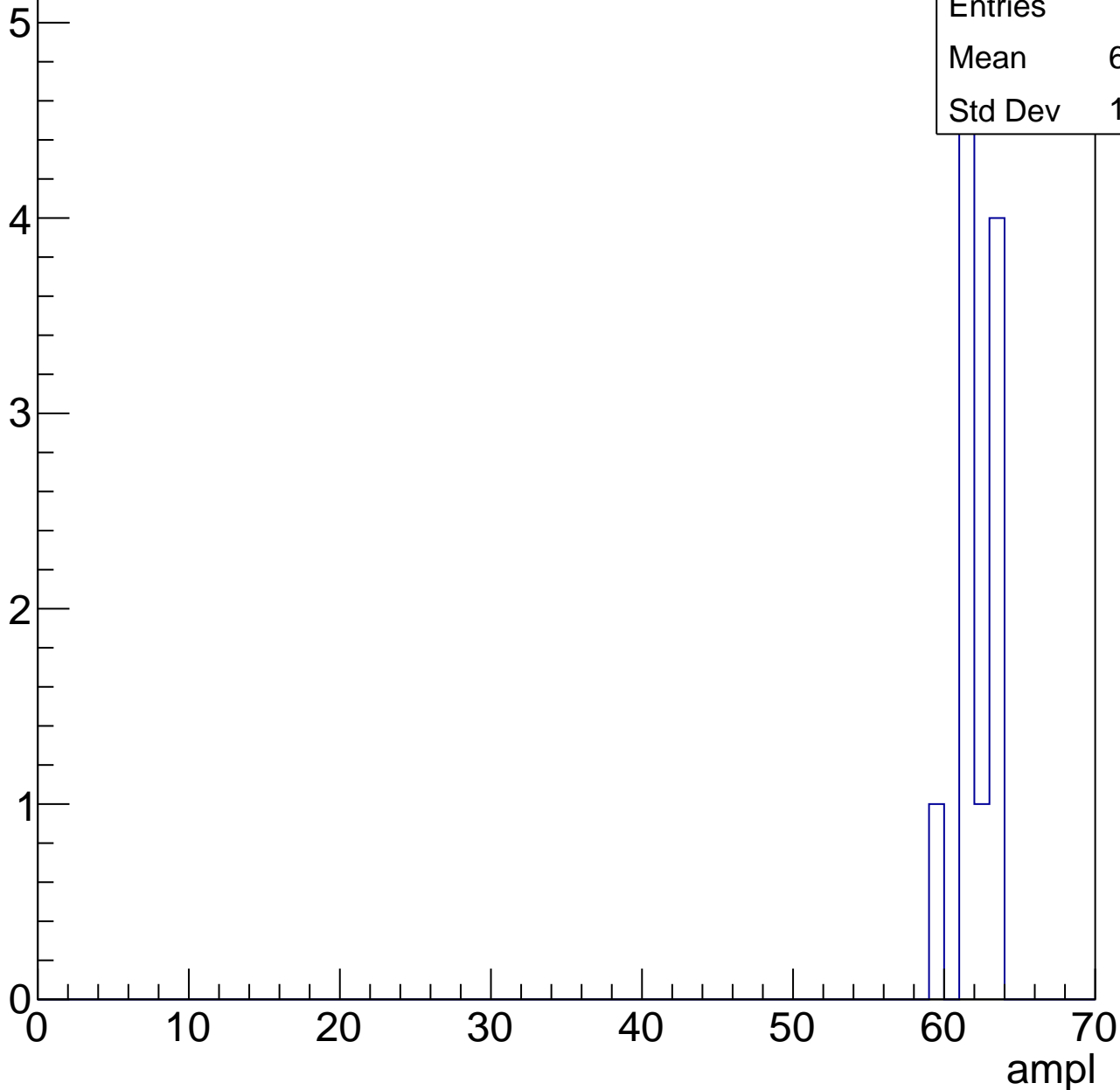


# B1L101S, U19-ch30, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	11
Mean	61.64
Std Dev	1.226





# B1L101S, U19-ch30, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U19-ch31, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	87
Mean	28.33
Std Dev	5.477

**Gaus mean : 29.2526**

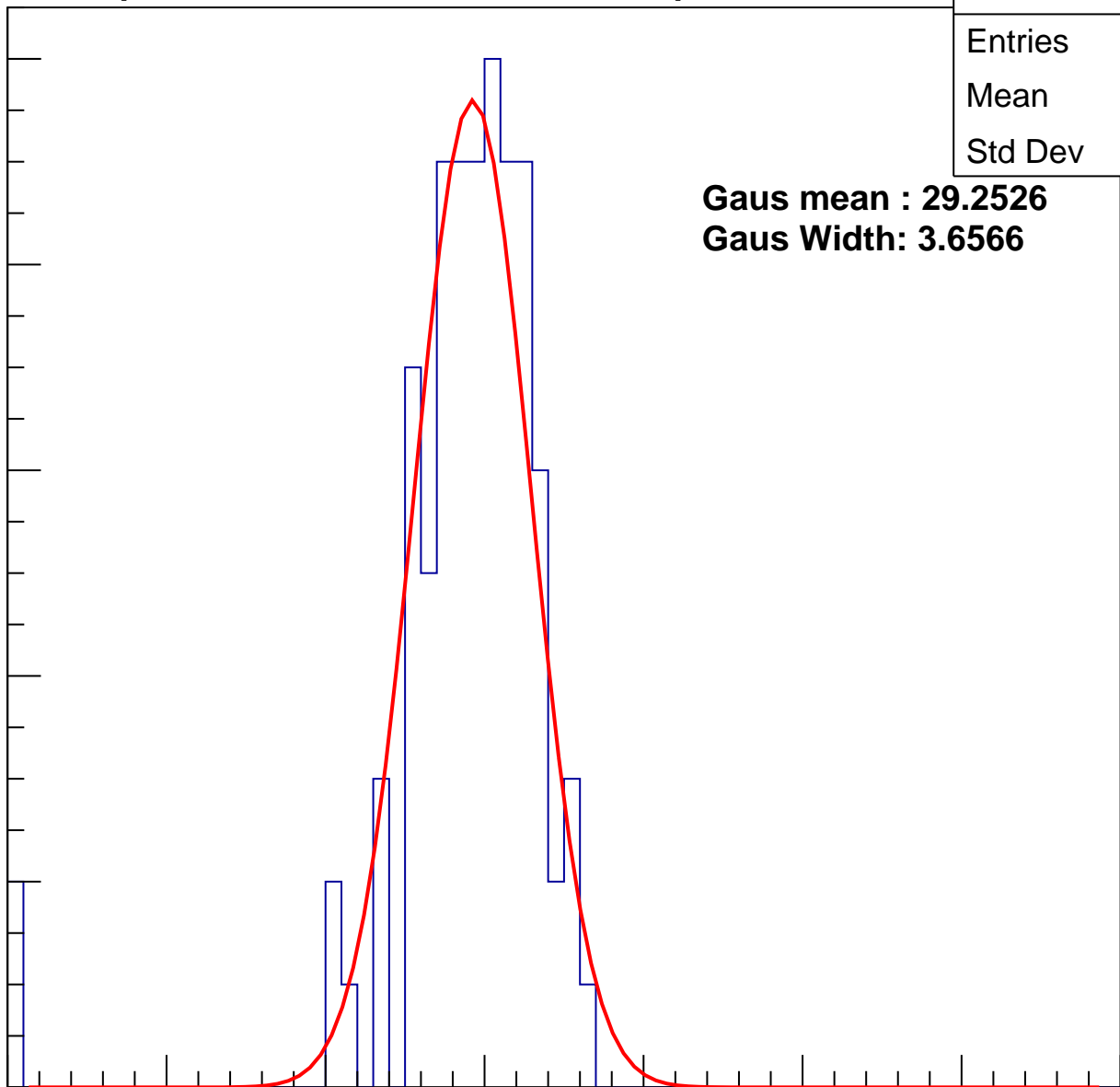
**Gaus Width: 3.6566**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U19-ch31, adc1

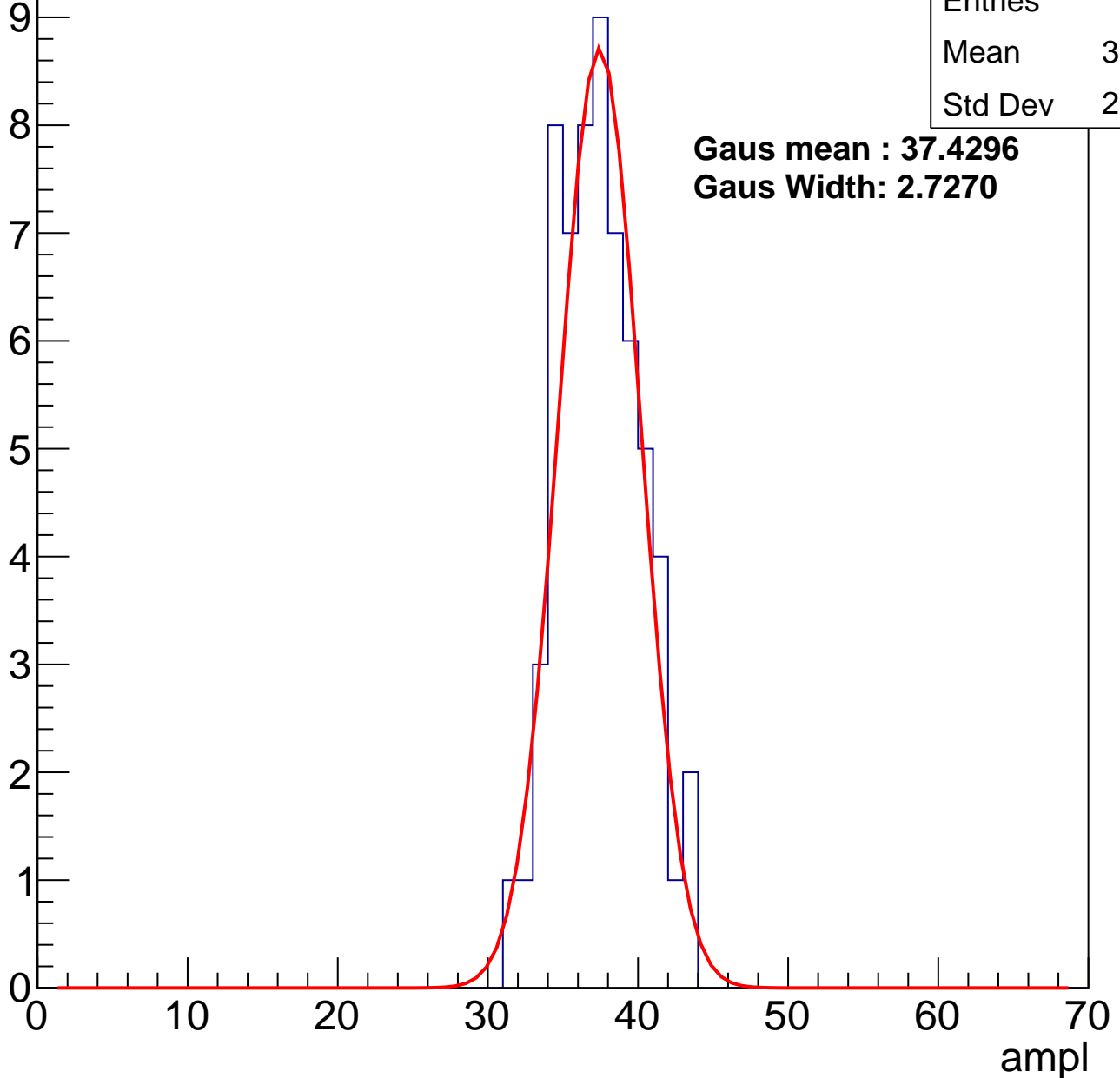
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	36.97
Std Dev	2.706

**Gaus mean : 37.4296**

**Gaus Width: 2.7270**



# B1L101S, U19-ch31, adc2

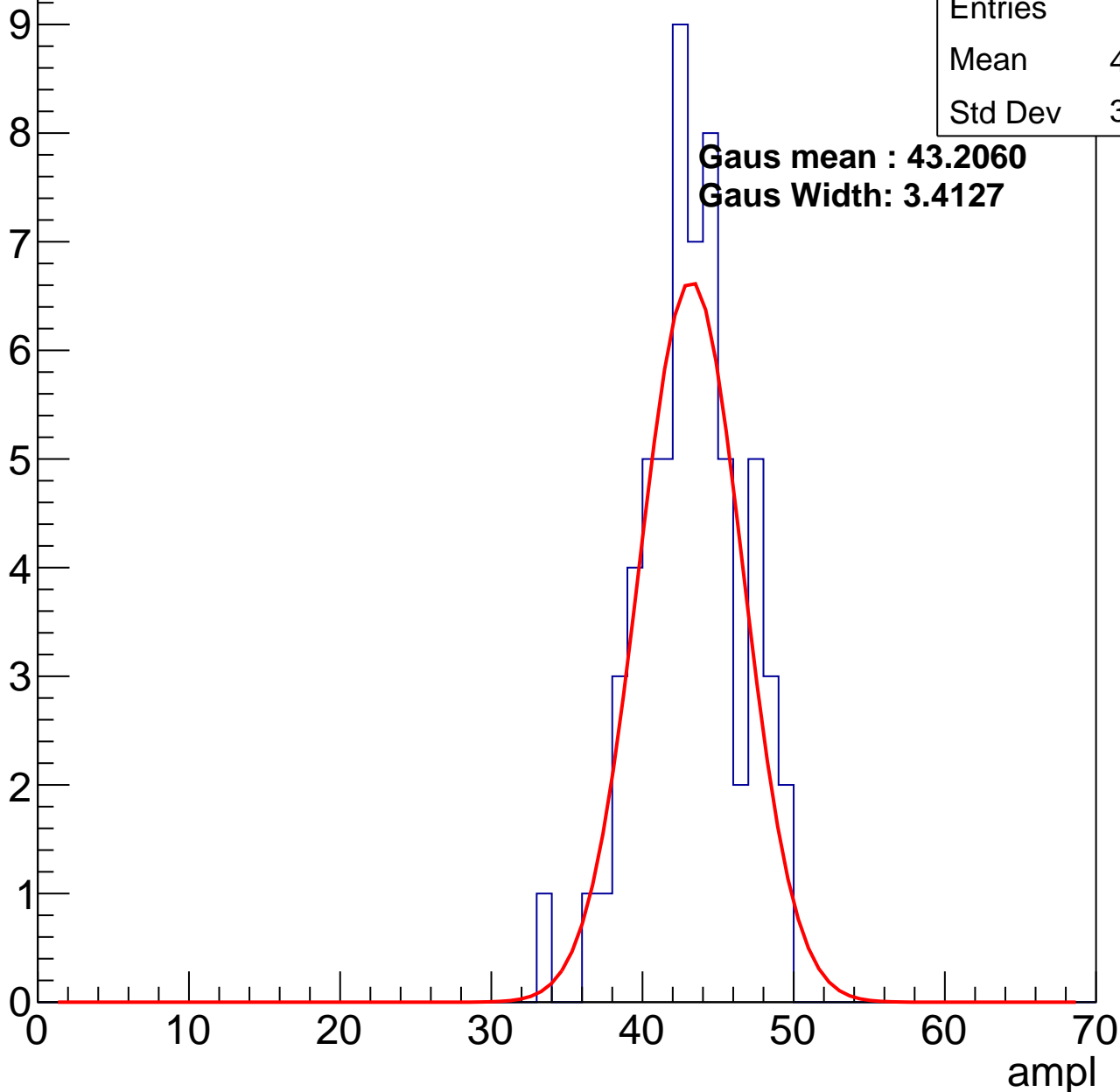
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	42.72
Std Dev	3.305

**Gaus mean : 43.2060**

**Gaus Width: 3.4127**

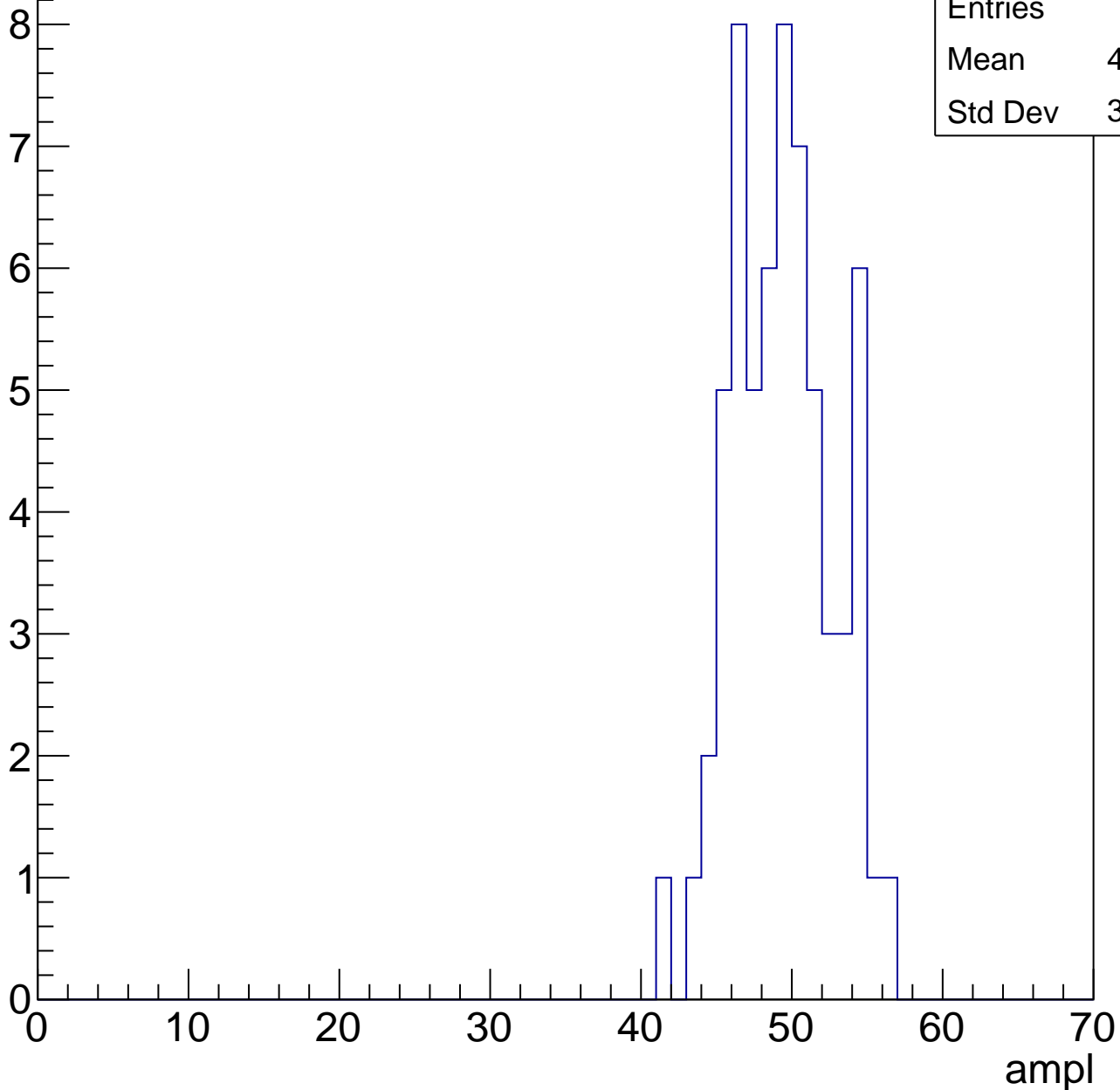


# B1L101S, U19-ch31, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

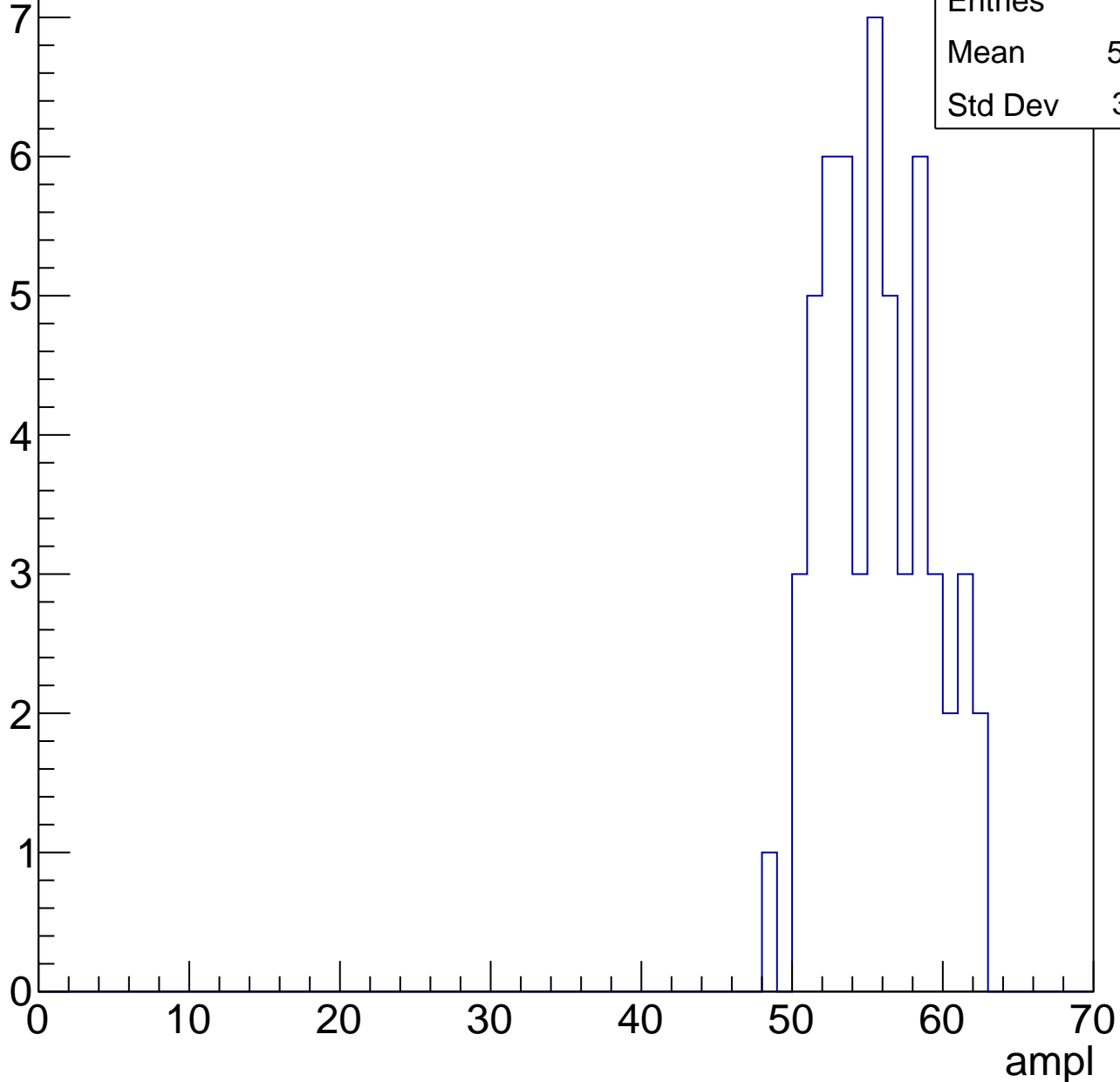
Entries	62
Mean	48.95
Std Dev	3.275



# B1L101S, U19-ch31, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

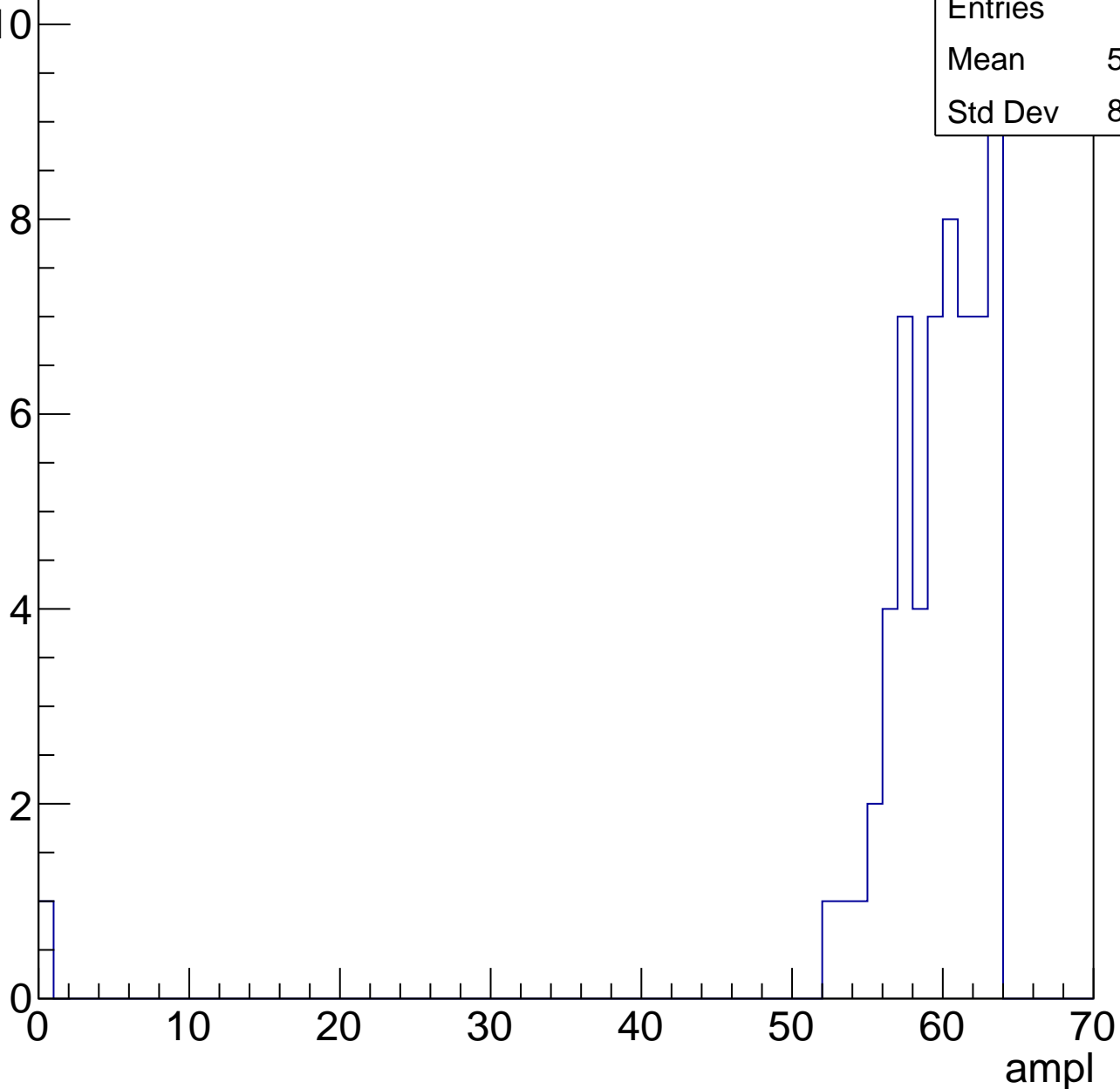


# B1L101S, U19-ch31, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	60
Mean	58.47
Std Dev	8.096



# B1L101S, U19-ch31, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U19-ch31, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U19-ch32, adc0

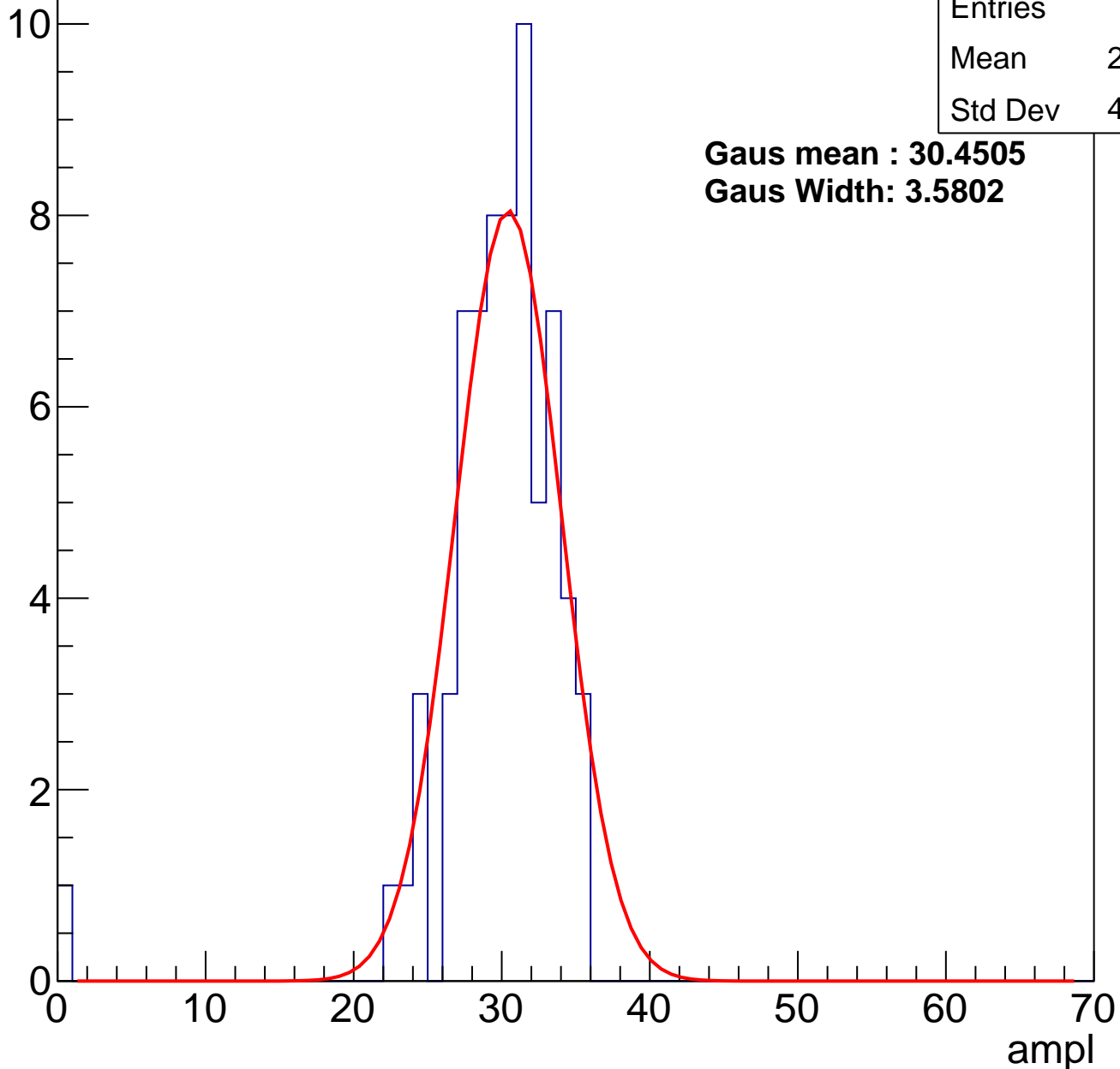
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	68
Mean	29.32
Std Dev	4.648

**Gaus mean : 30.4505**

**Gaus Width: 3.5802**

Entry



# B1L101S, U19-ch32, adc1

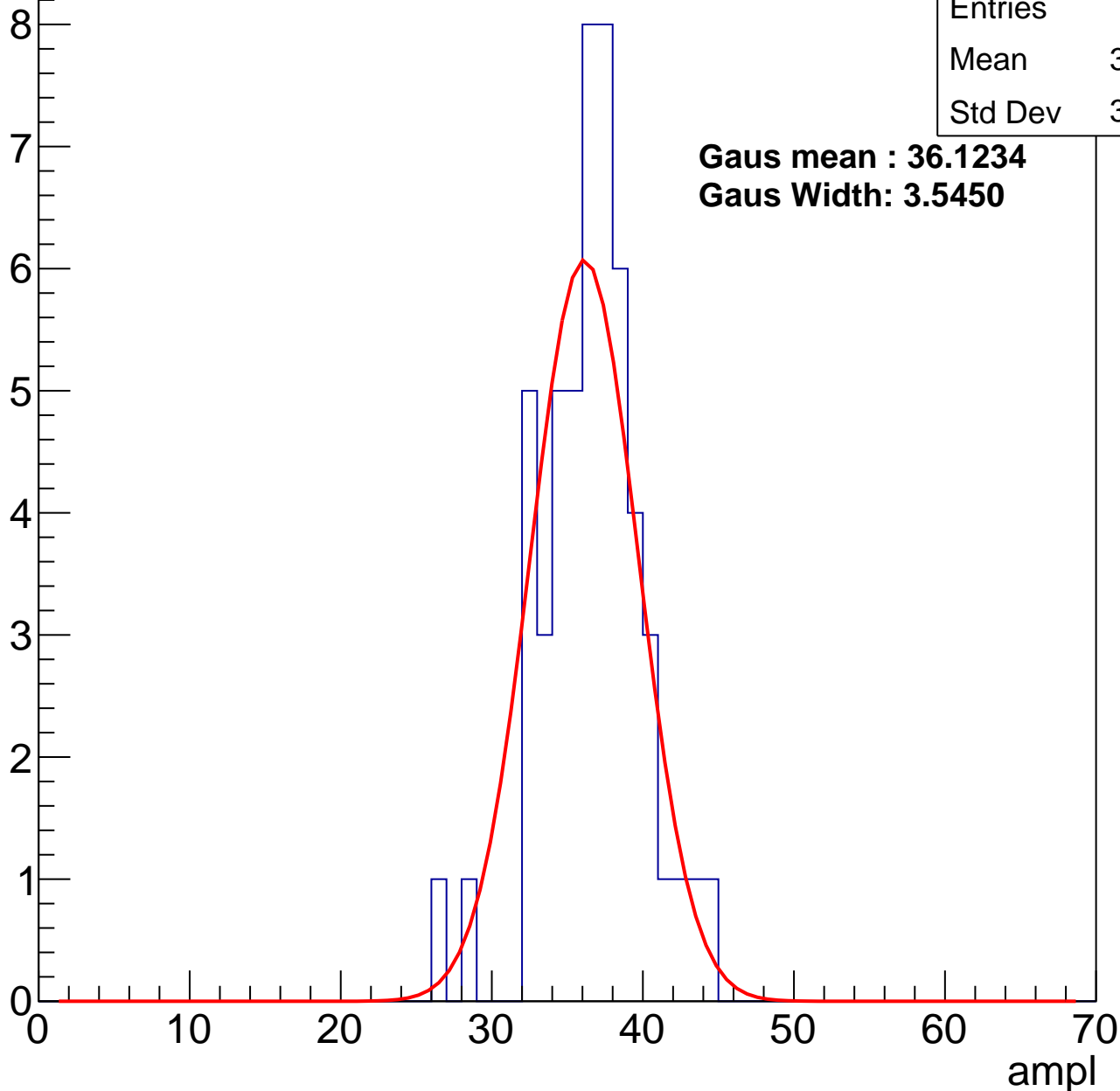
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	53
Mean	36.15
Std Dev	3.322

**Gaus mean : 36.1234**

**Gaus Width: 3.5450**



# B1L101S, U19-ch32, adc2

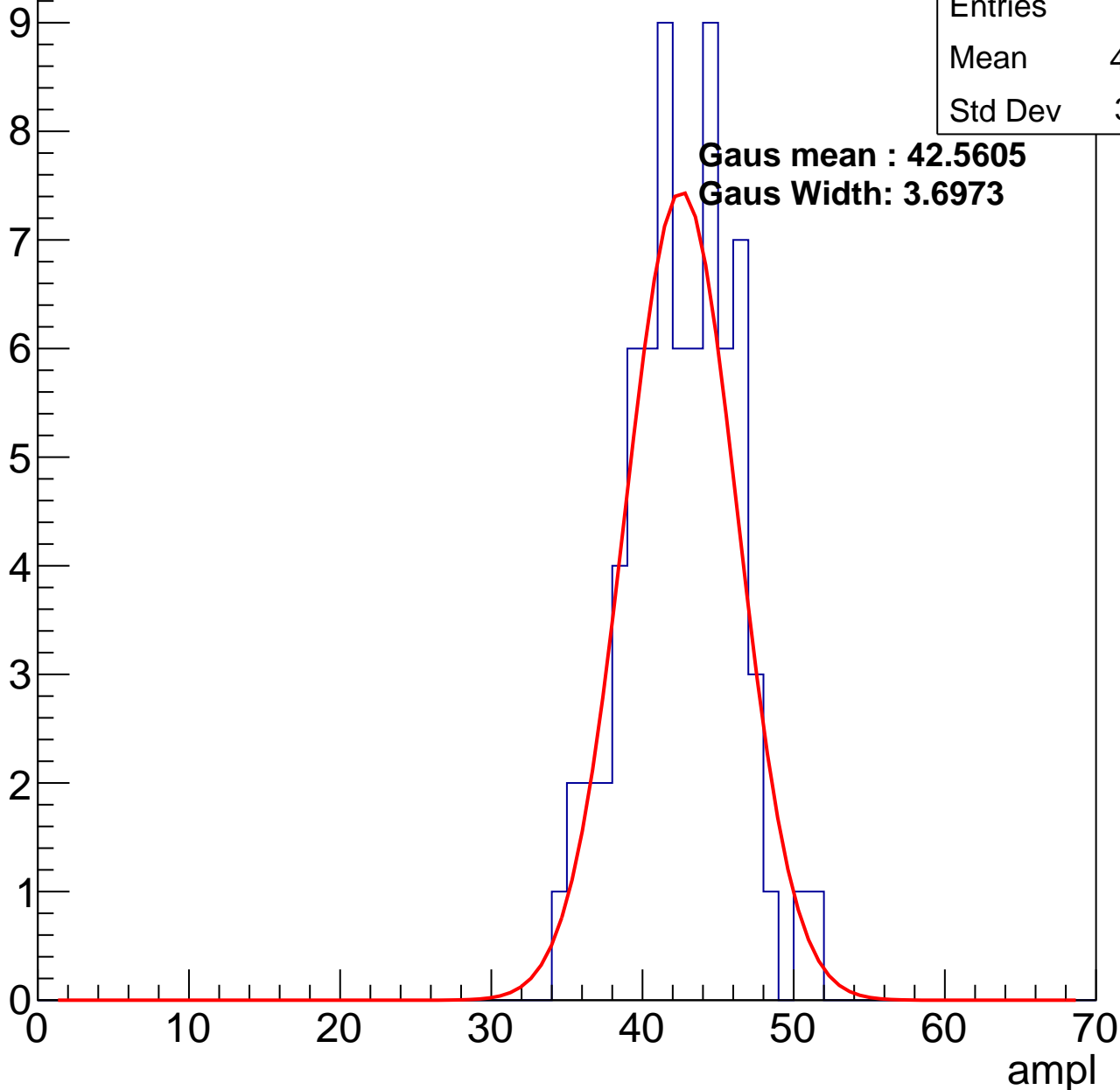
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	72
Mean	42.12
Std Dev	3.531

**Gaus mean : 42.5605**

**Gaus Width: 3.6973**

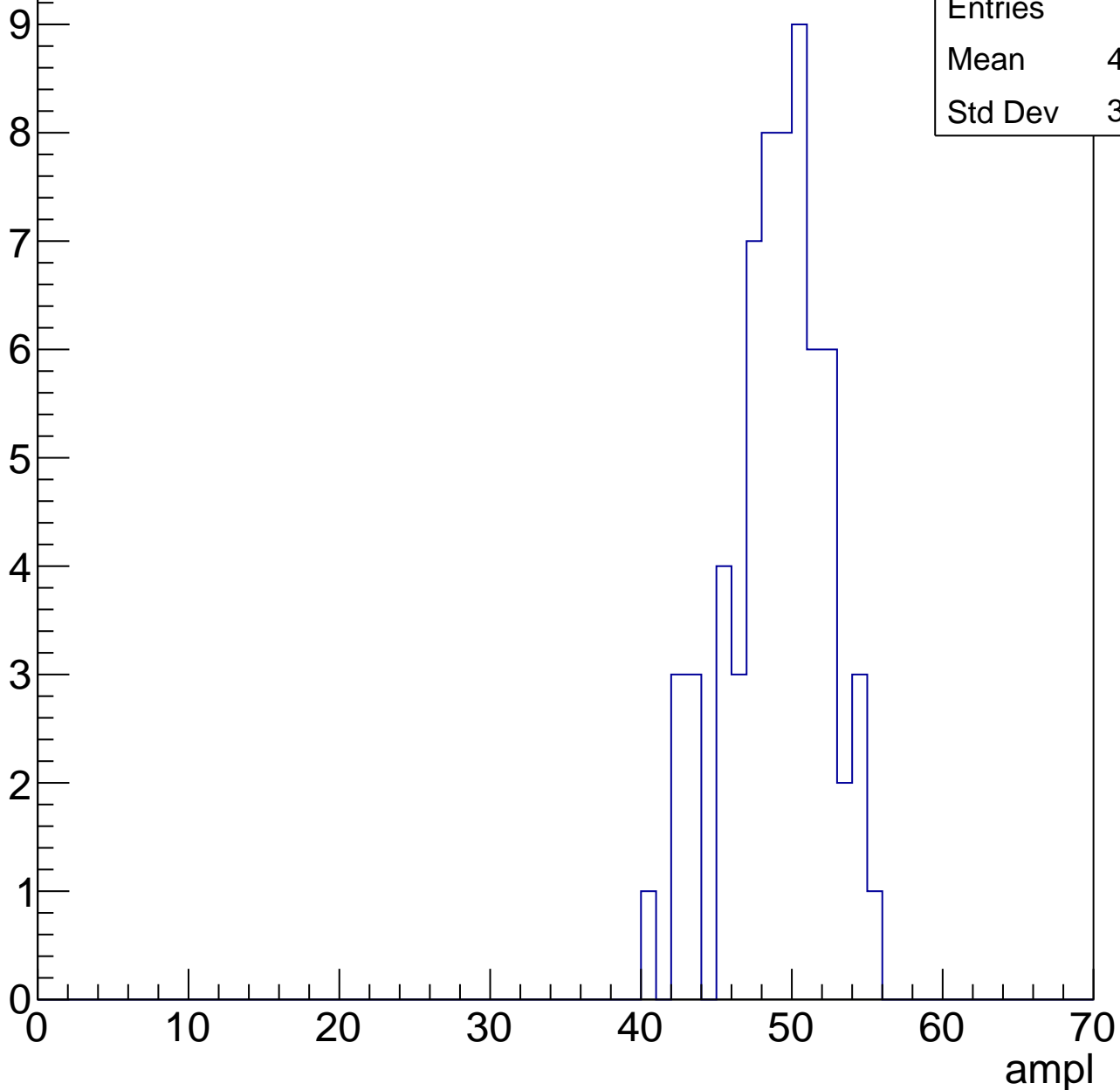


# B1L101S, U19-ch32, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	48.58
Std Dev	3.263

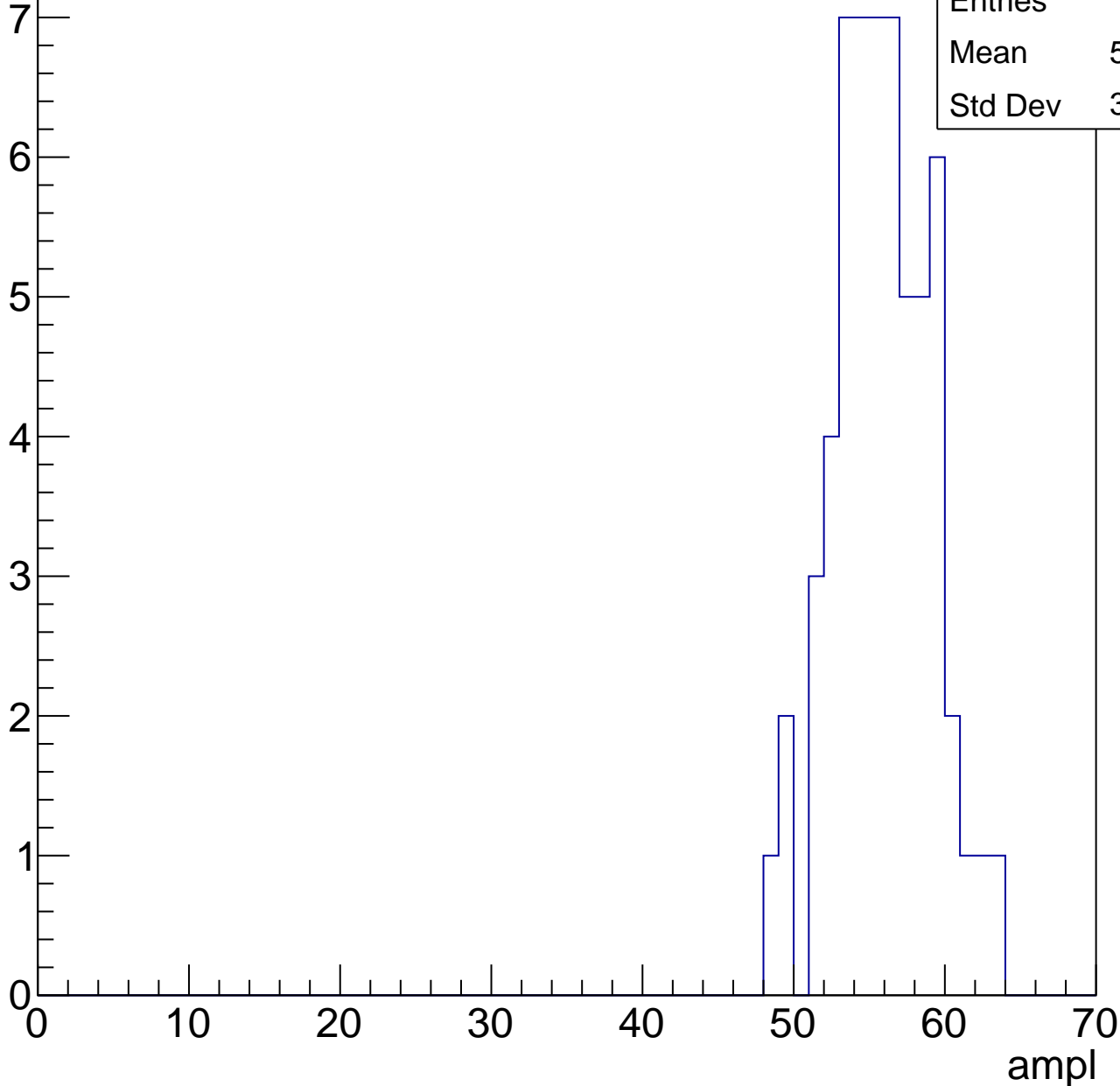


# B1L101S, U19-ch32, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	59
Mean	55.39
Std Dev	3.184

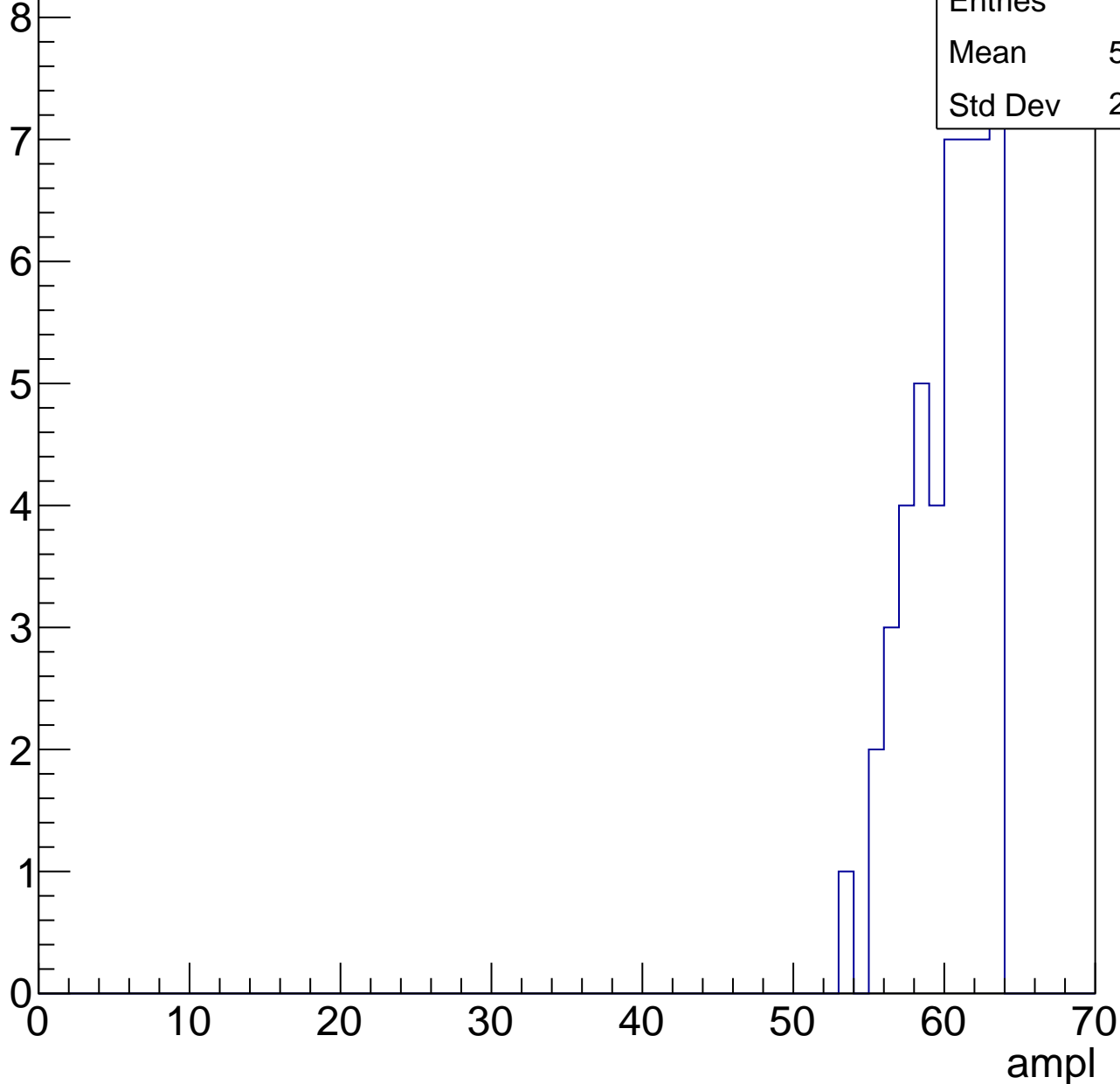


# B1L101S, U19-ch32, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

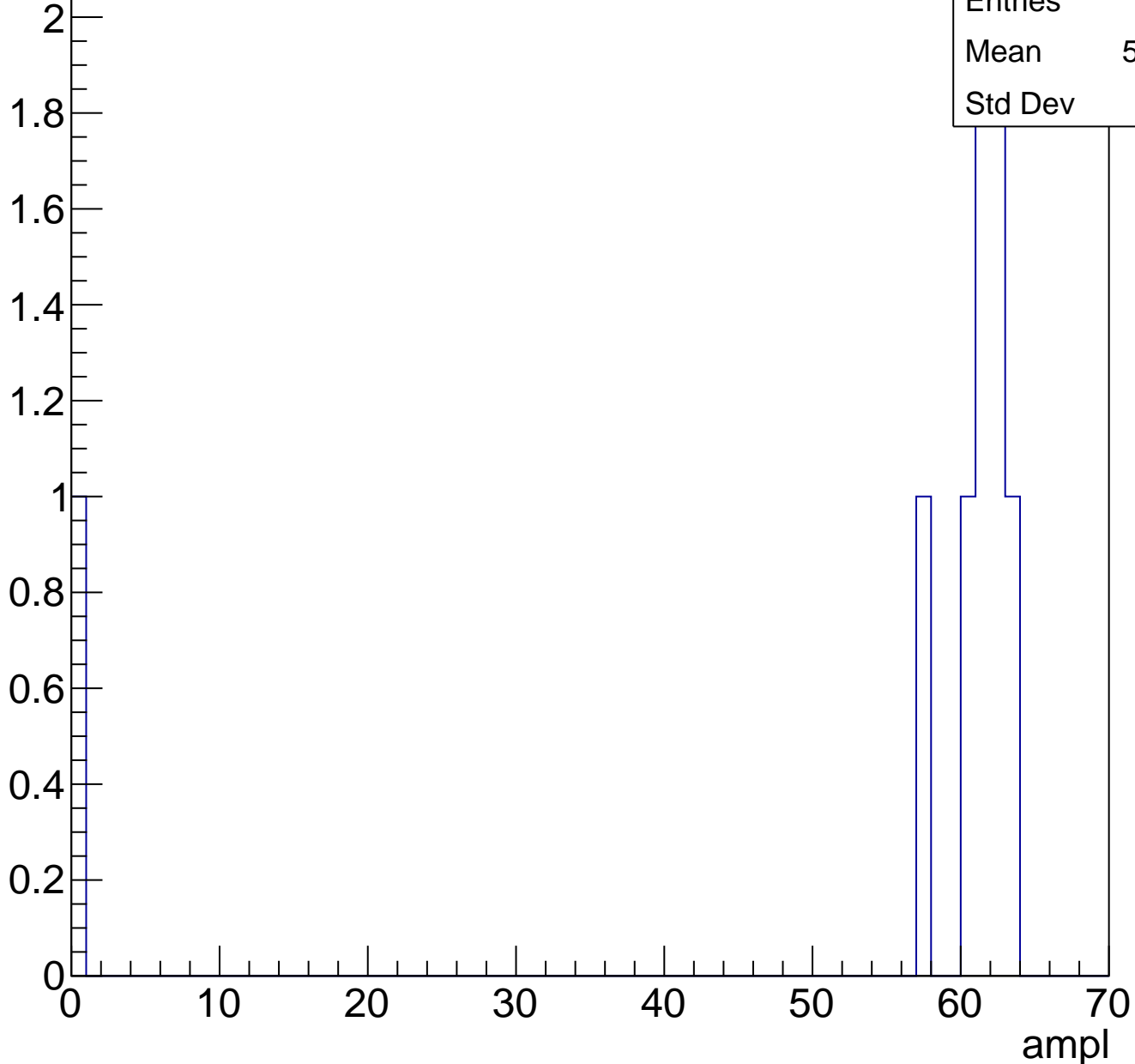
Entries	48
Mean	59.79
Std Dev	2.549



# B1L101S, U19-ch32, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U19-ch32, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U19-ch33, adc0

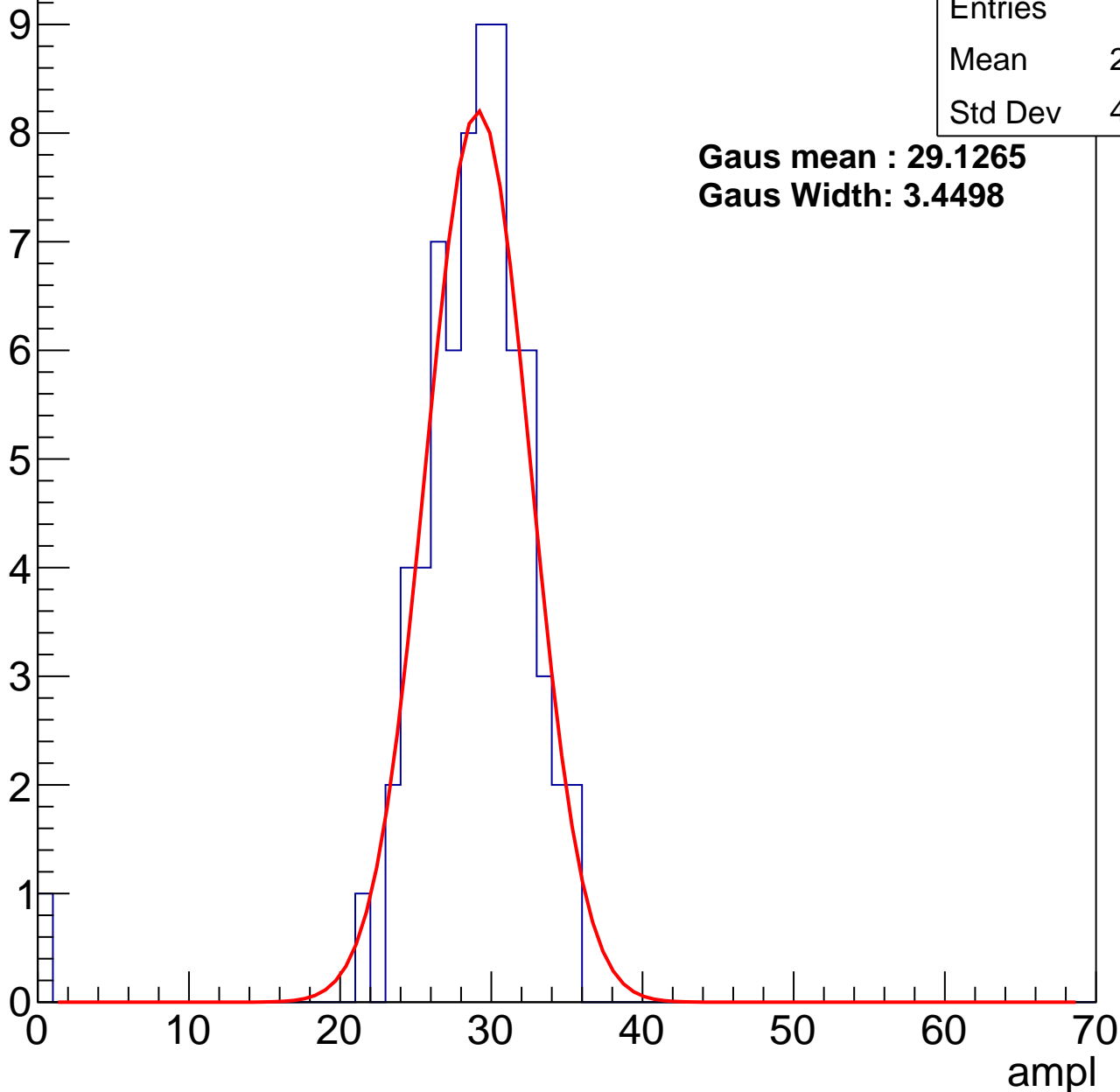
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	28.24
Std Dev	4.556

**Gaus mean : 29.1265**

**Gaus Width: 3.4498**



# B1L101S, U19-ch33, adc1

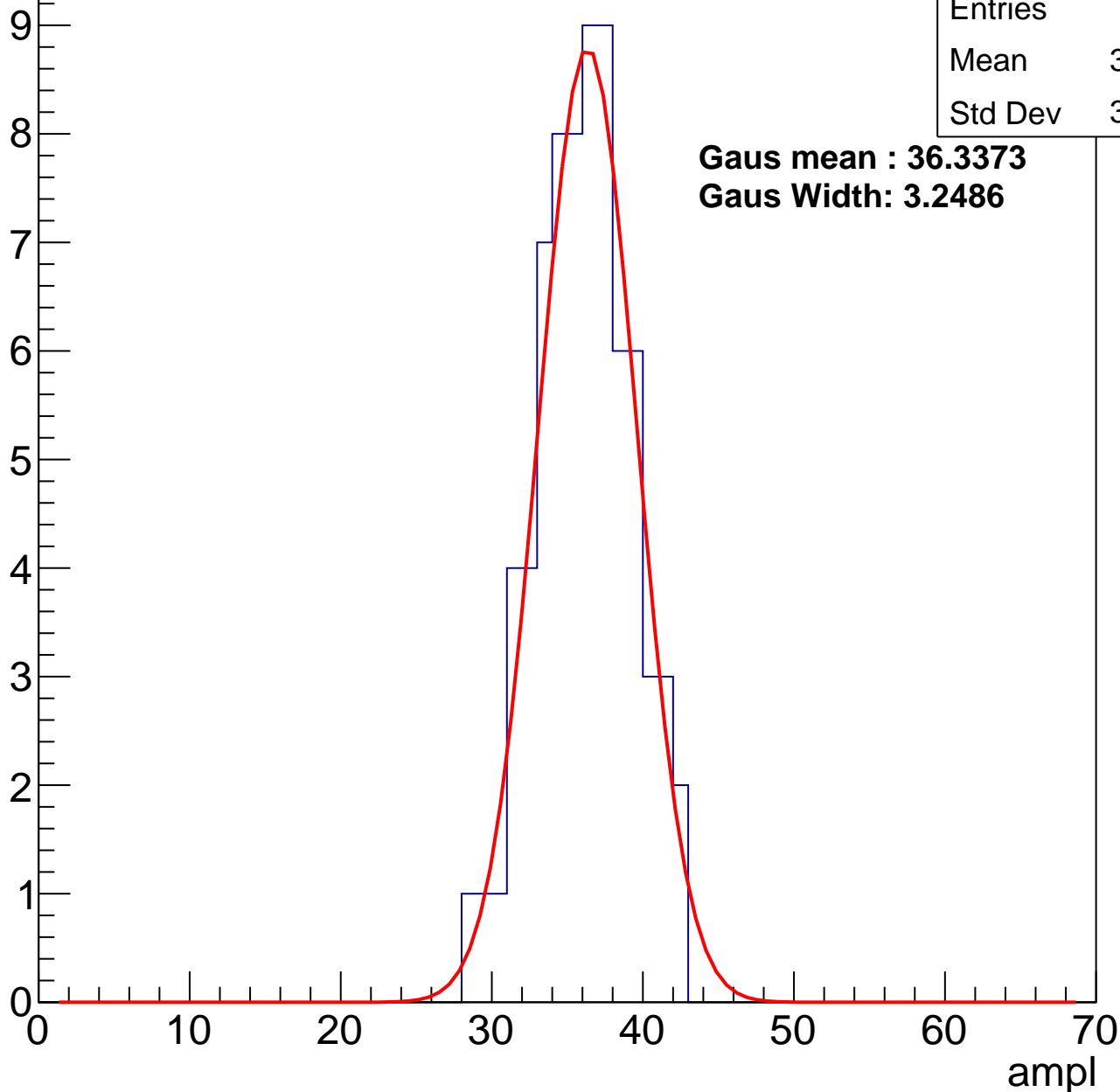
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	72
Mean	35.67
Std Dev	3.096

**Gaus mean : 36.3373**

**Gaus Width: 3.2486**



# B1L101S, U19-ch33, adc2

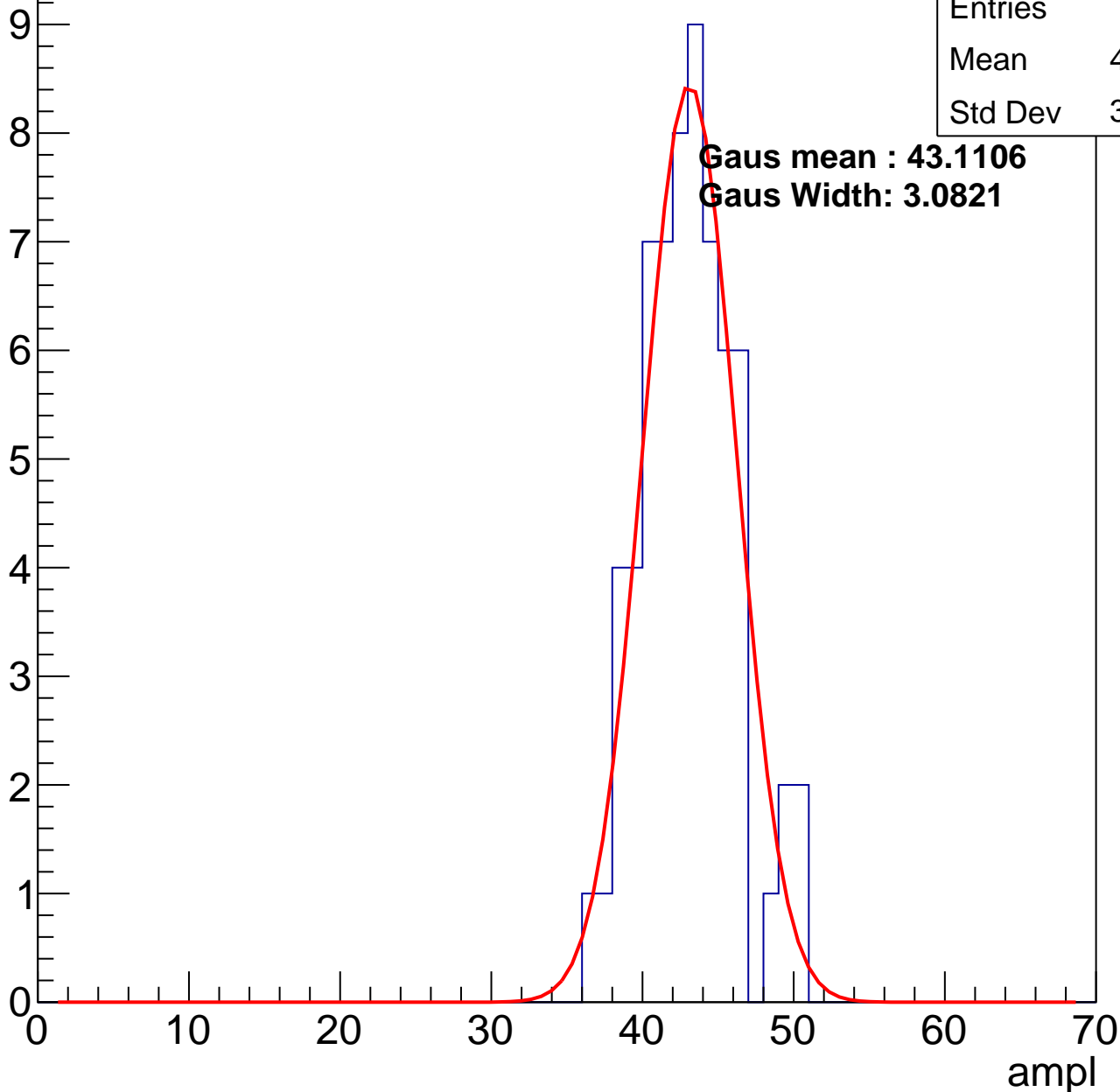
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	42.63
Std Dev	3.086

**Gaus mean : 43.1106**

**Gaus Width: 3.0821**



# B1L101S, U19-ch33, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	58
Mean	48.86
Std Dev	3.008

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

1

2

3

4

5

6

7

8

9

10

11

12

13

14

15

16

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18

19

20

21

22

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24

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31

32

33

34

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40

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42

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49

50

51

52

53

54

55

56

57

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64

65

66

67

68

69

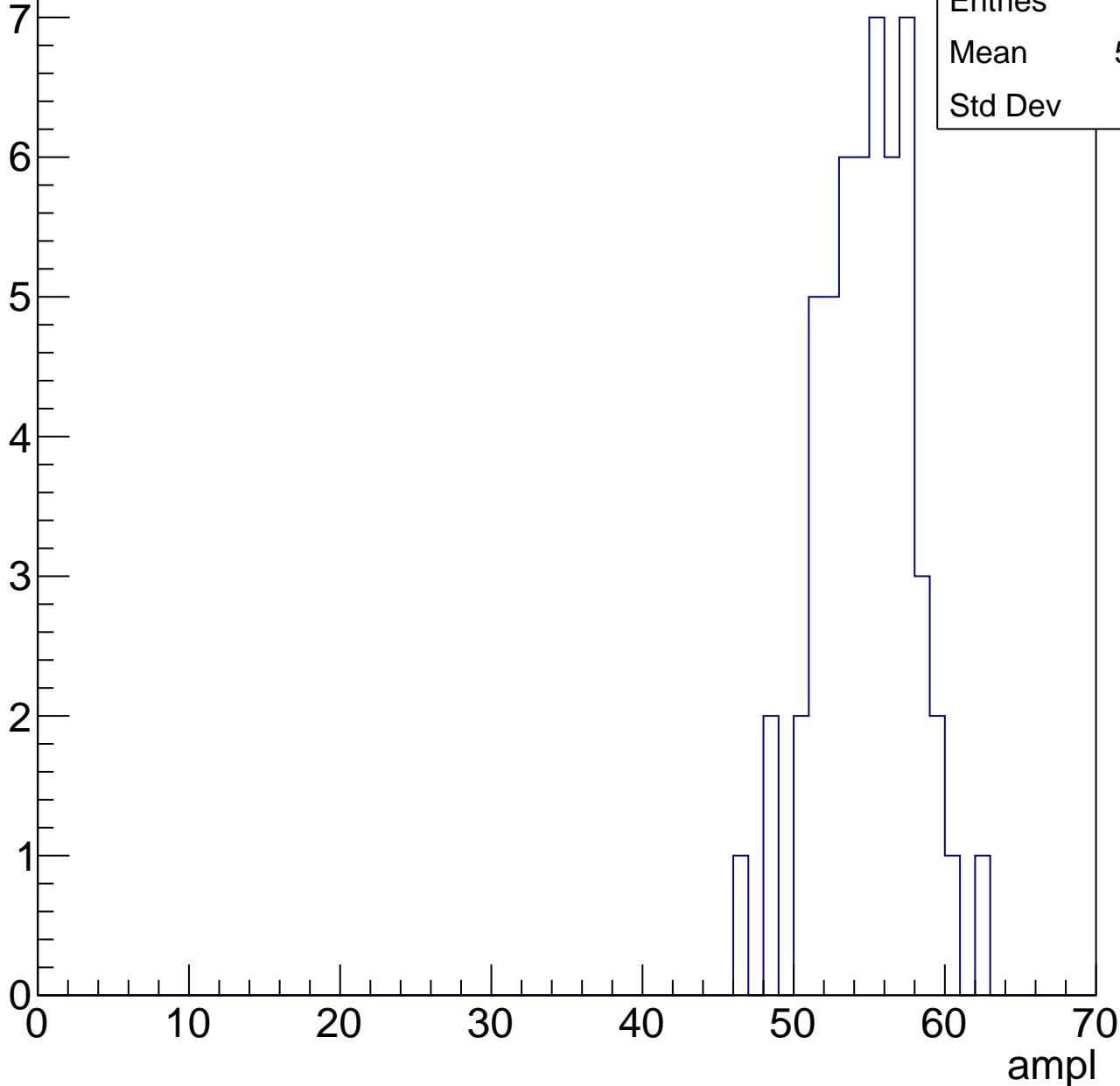
70

# B1L101S, U19-ch33, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	54
Mean	54.31
Std Dev	3.12

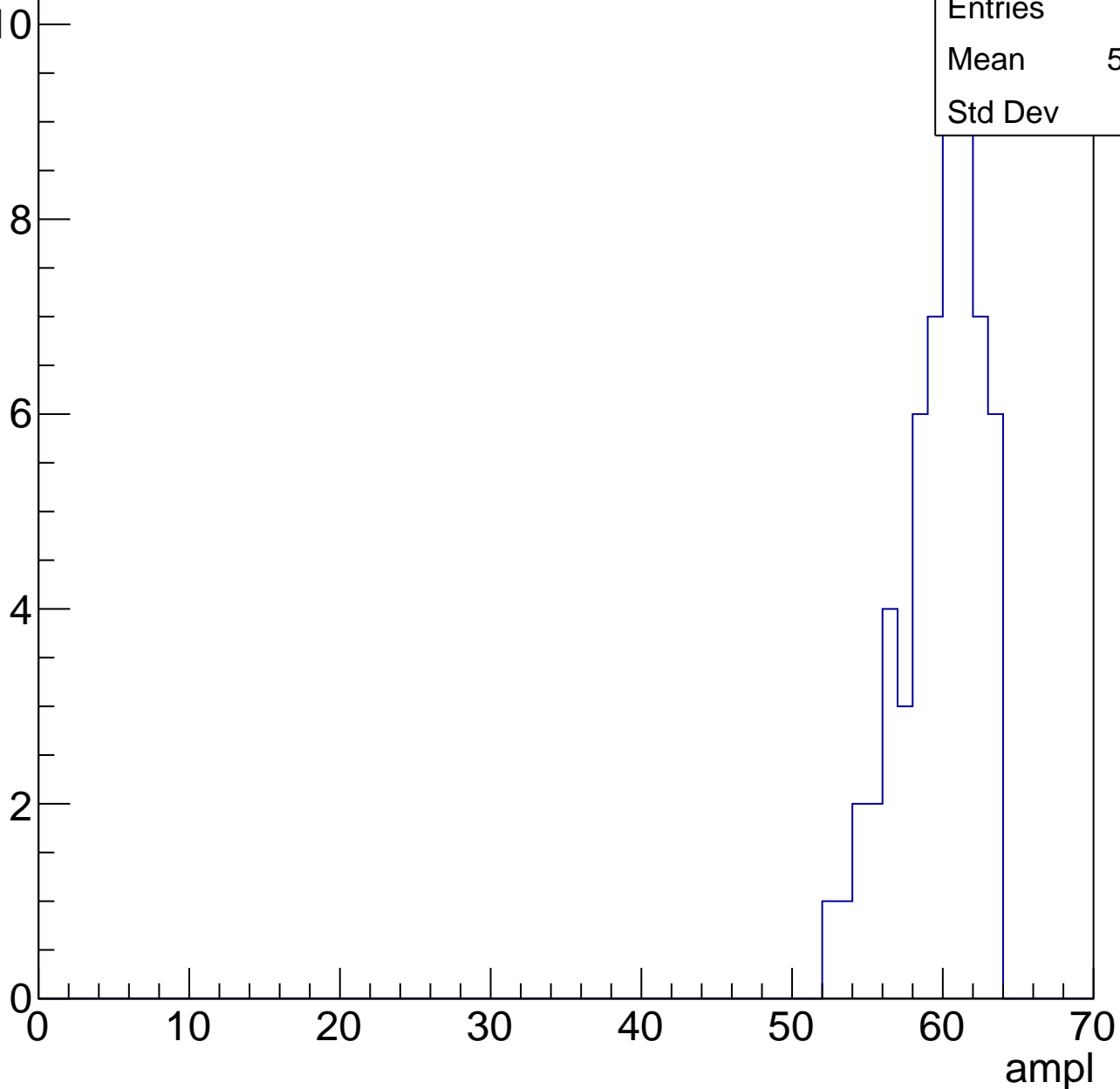


# B1L101S, U19-ch33, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

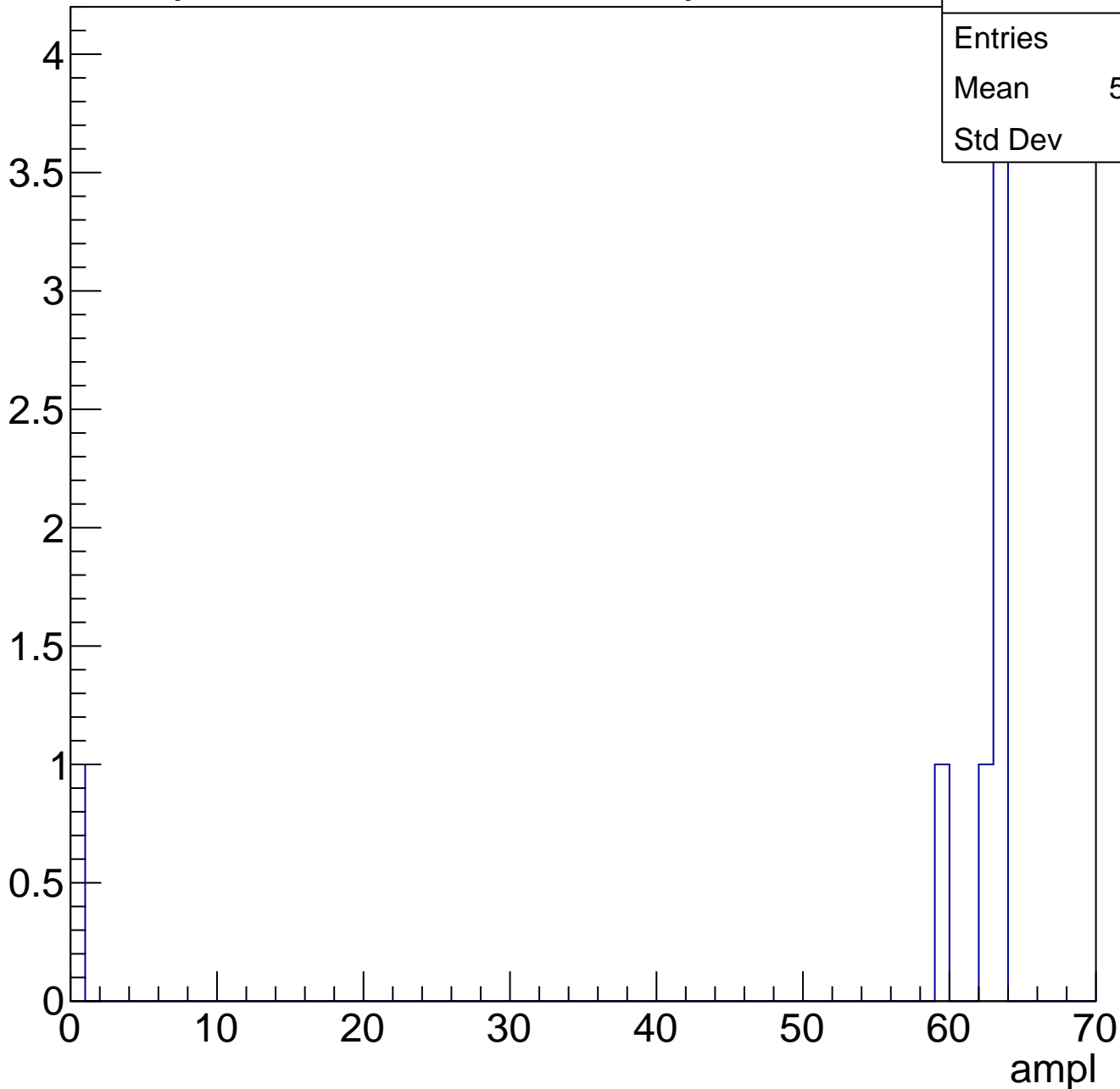
Entries	58
Mean	59.33
Std Dev	2.7



# B1L101S, U19-ch33, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U19-ch33, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U19-ch34, adc0

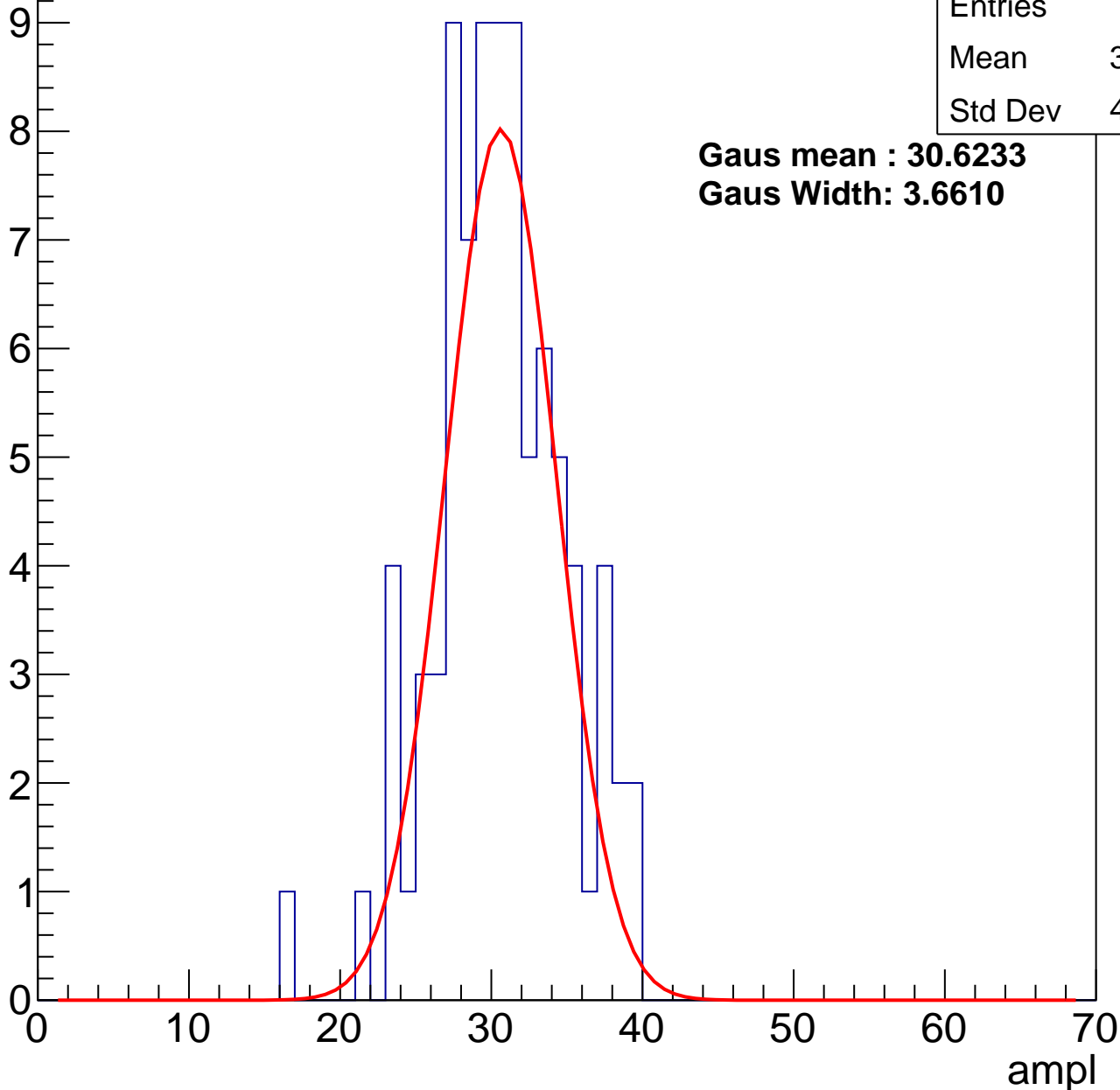
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	85
Mean	30.13
Std Dev	4.248

**Gaus mean : 30.6233**

**Gaus Width: 3.6610**



# B1L101S, U19-ch34, adc1

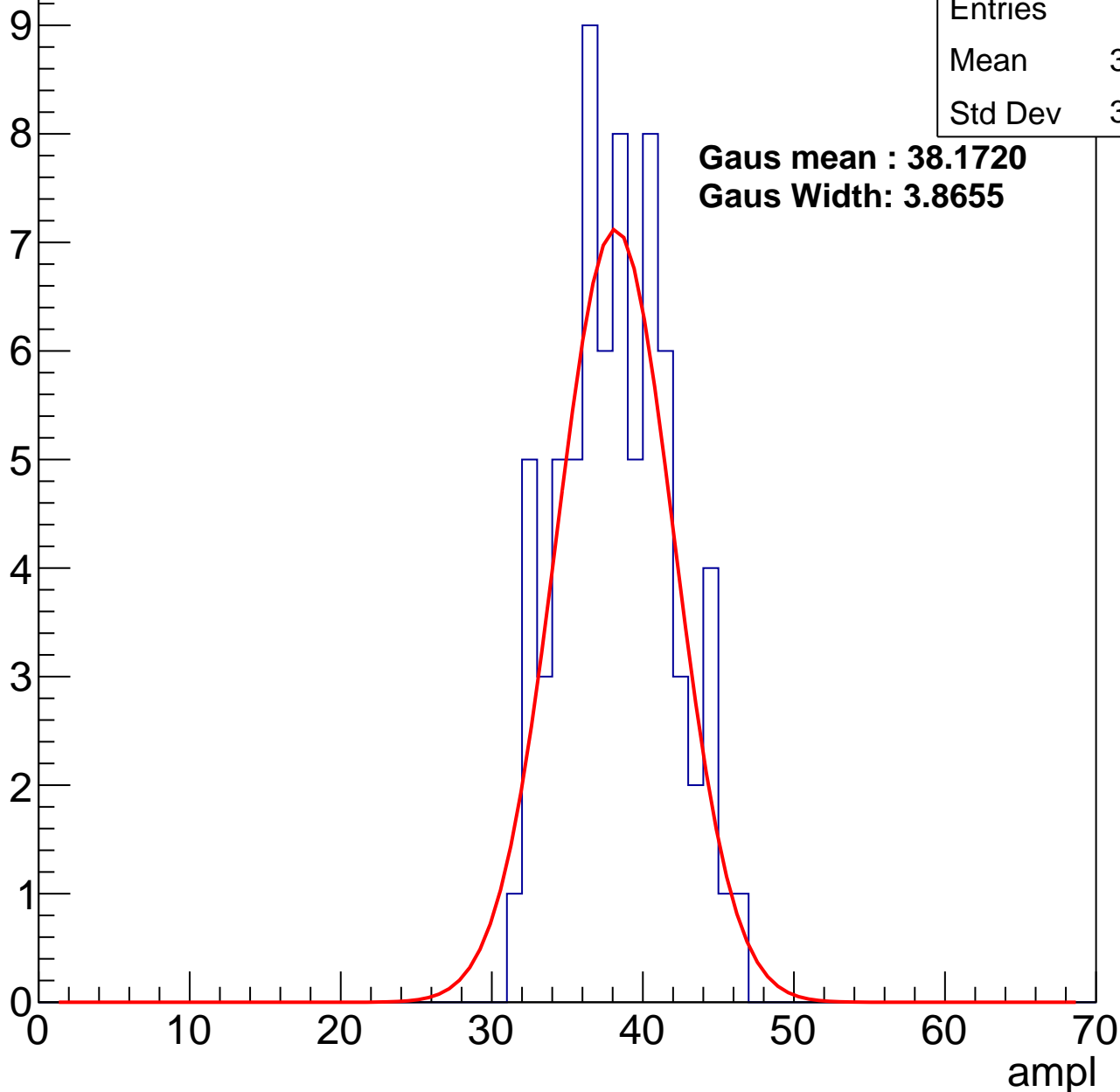
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	72
Mean	37.85
Std Dev	3.565

**Gaus mean : 38.1720**

**Gaus Width: 3.8655**



# B1L101S, U19-ch34, adc2

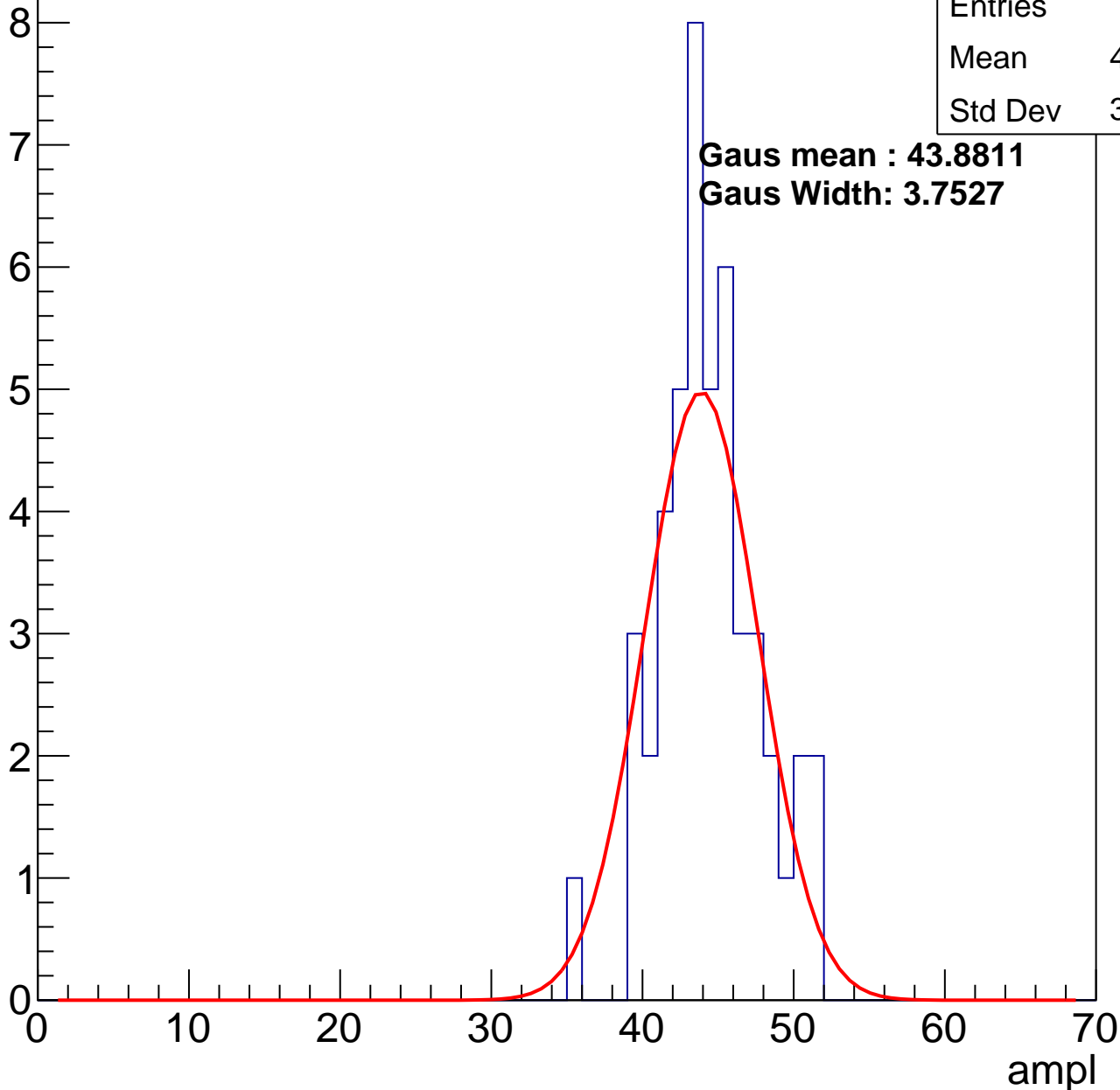
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	47
Mean	43.96
Std Dev	3.339

**Gaus mean : 43.8811**

**Gaus Width: 3.7527**

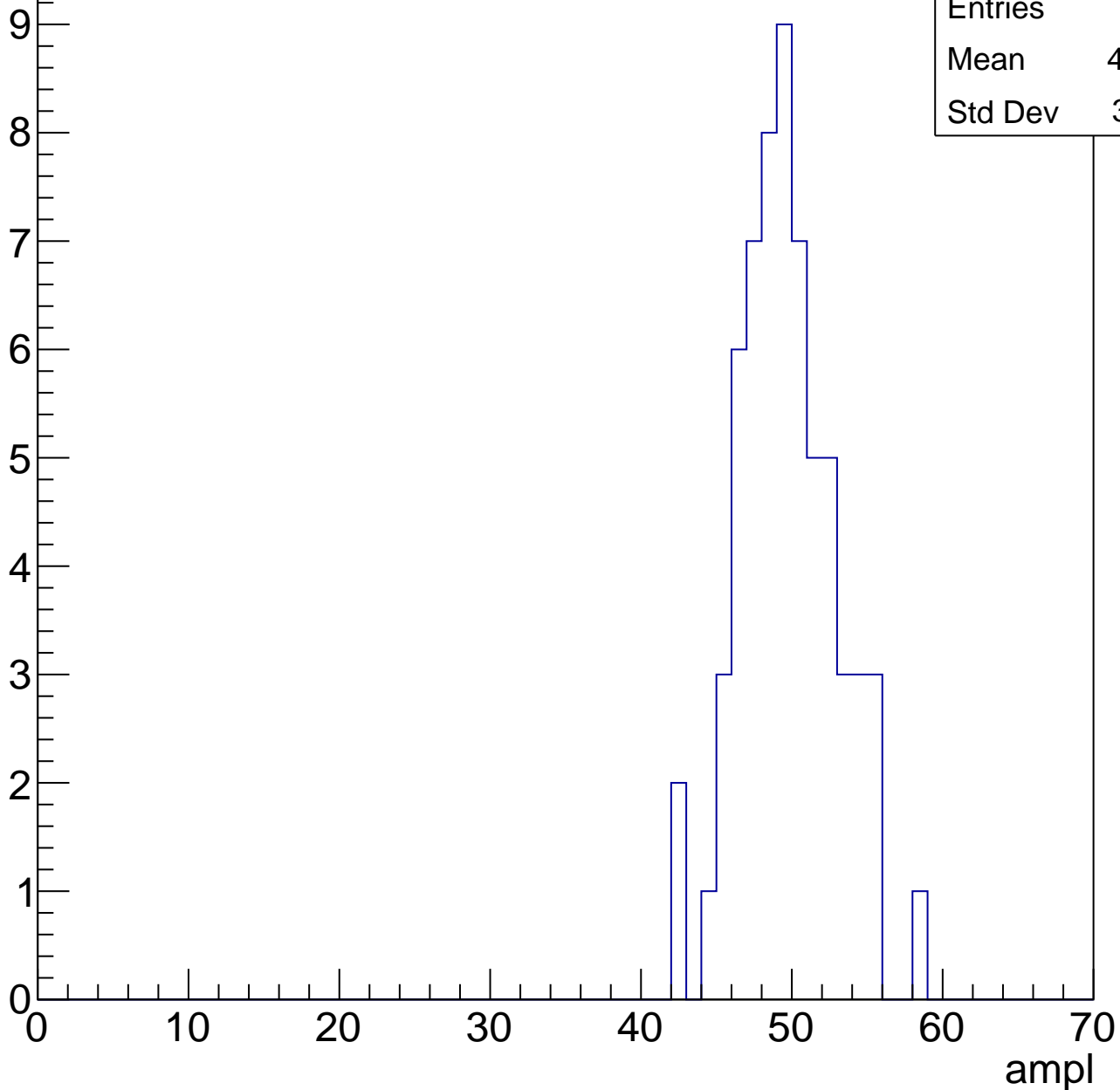


# B1L101S, U19-ch34, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	49.24
Std Dev	3.191

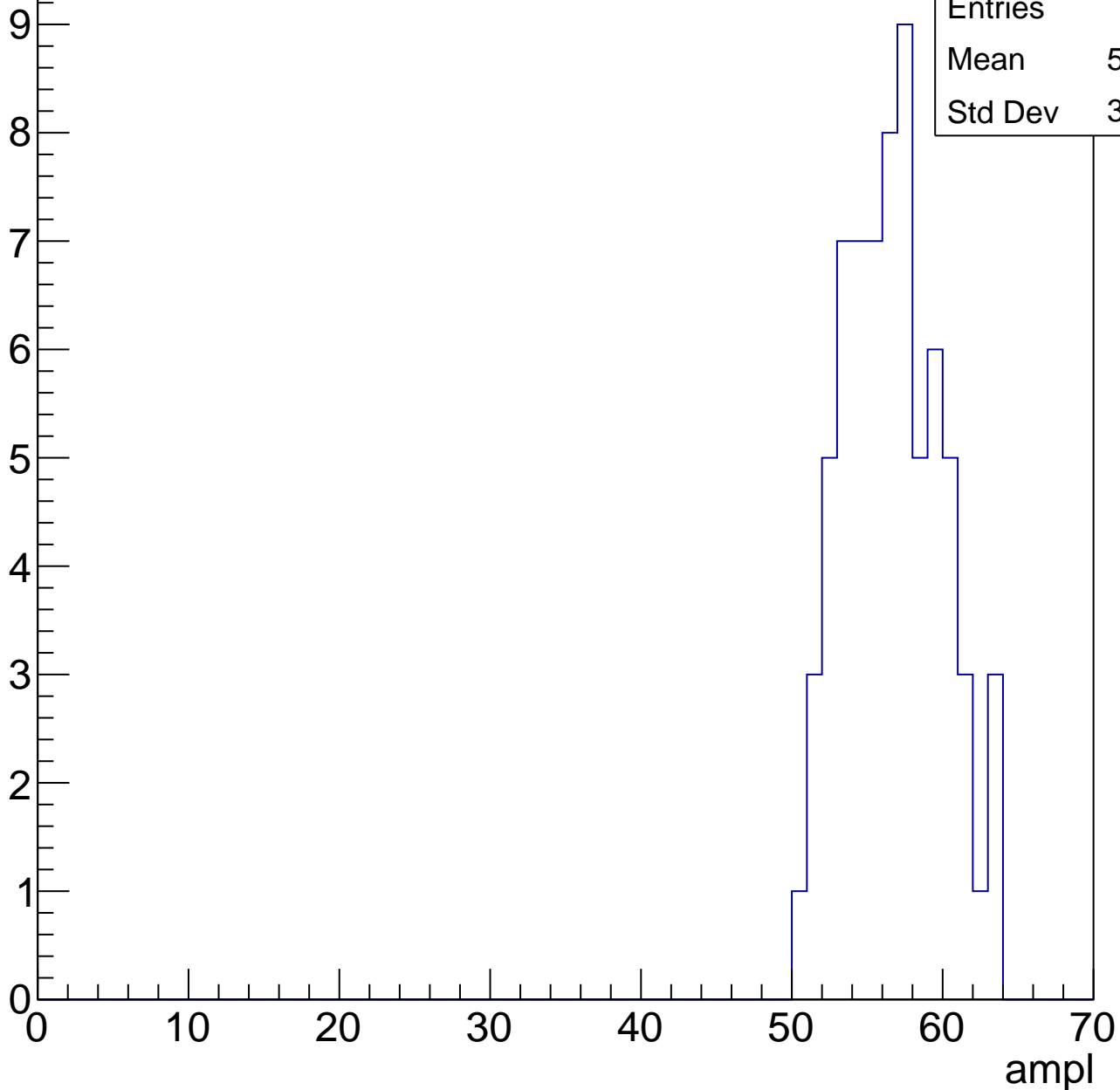


# B1L101S, U19-ch34, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	56.23
Std Dev	3.177

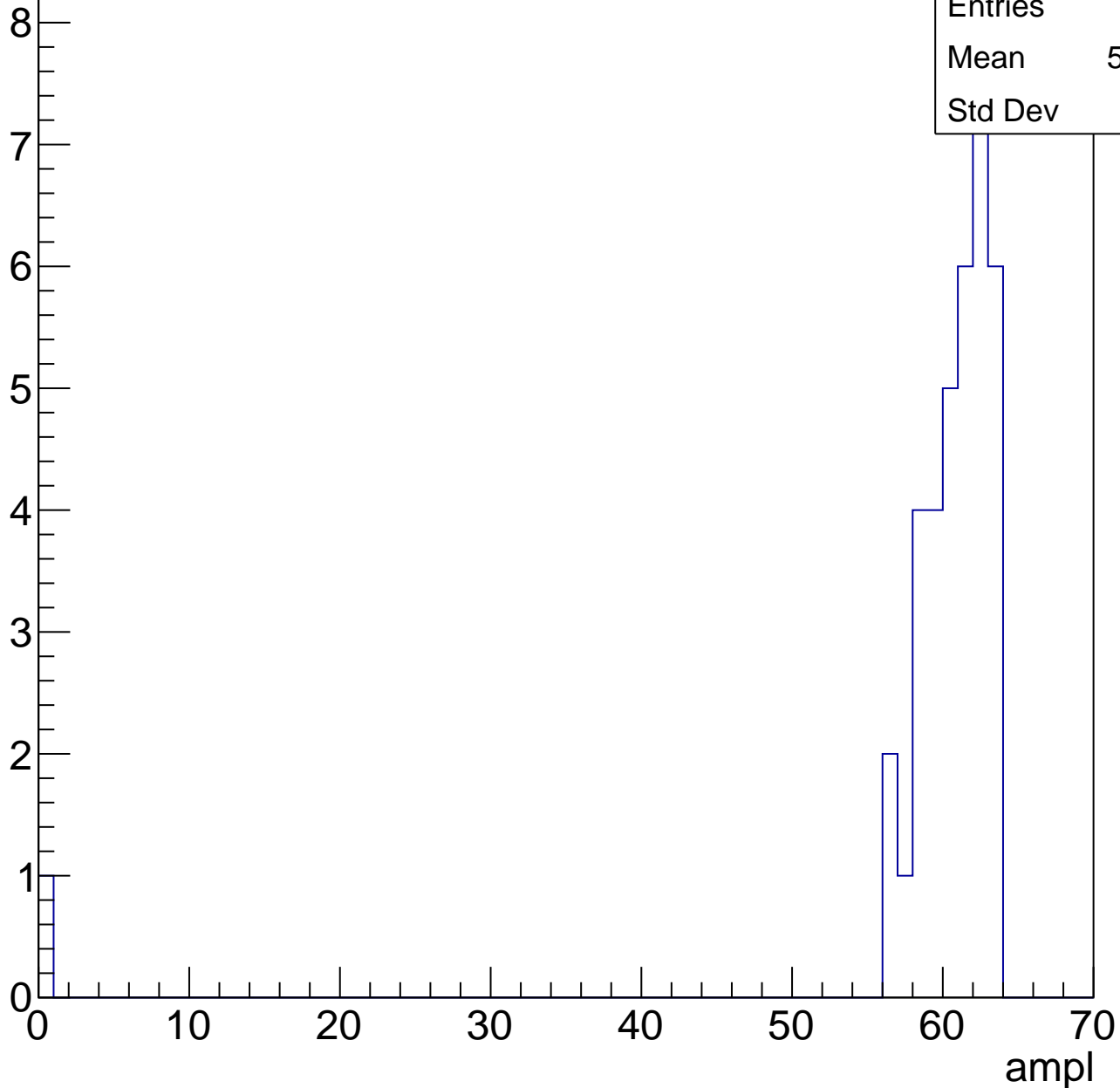


# B1L101S, U19-ch34, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	37
Mean	58.84
Std Dev	10



# B1L101S, U19-ch34, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U19-ch34, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U19-ch35, adc0

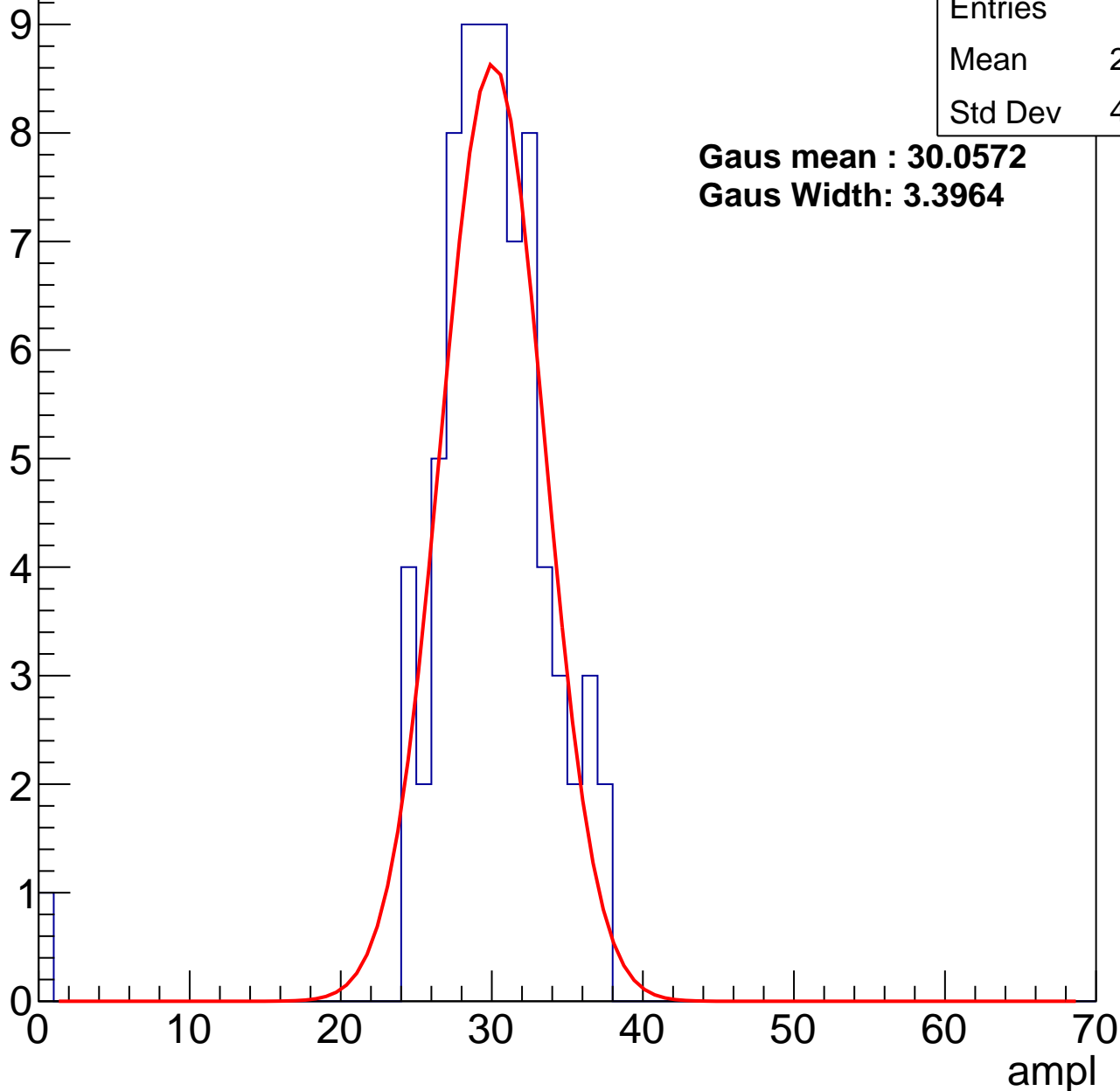
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	76
Mean	29.39
Std Dev	4.648

**Gaus mean : 30.0572**

**Gaus Width: 3.3964**



# B1L101S, U19-ch35, adc1

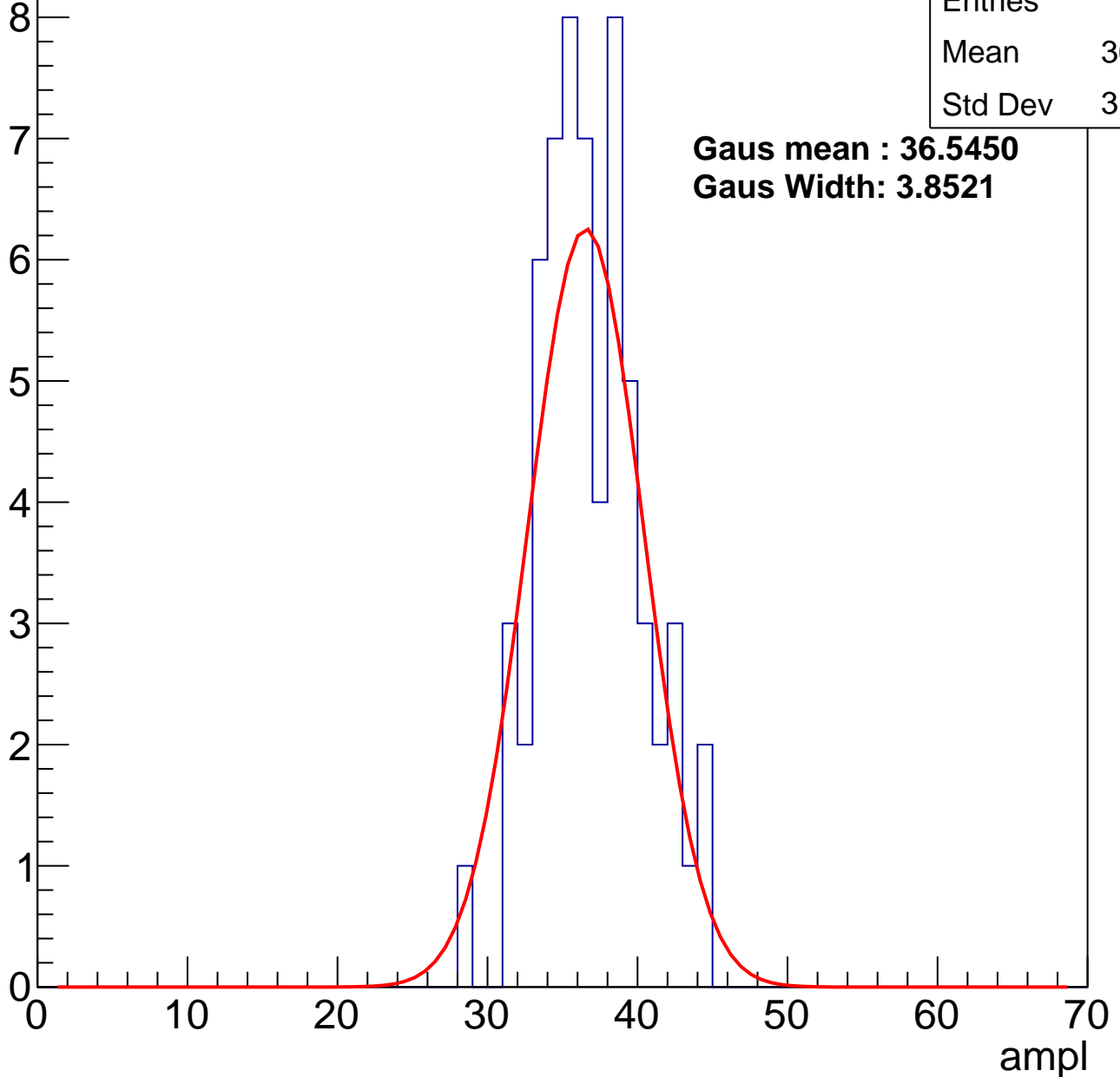
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	36.44
Std Dev	3.392

**Gaus mean : 36.5450**

**Gaus Width: 3.8521**



# B1L101S, U19-ch35, adc2

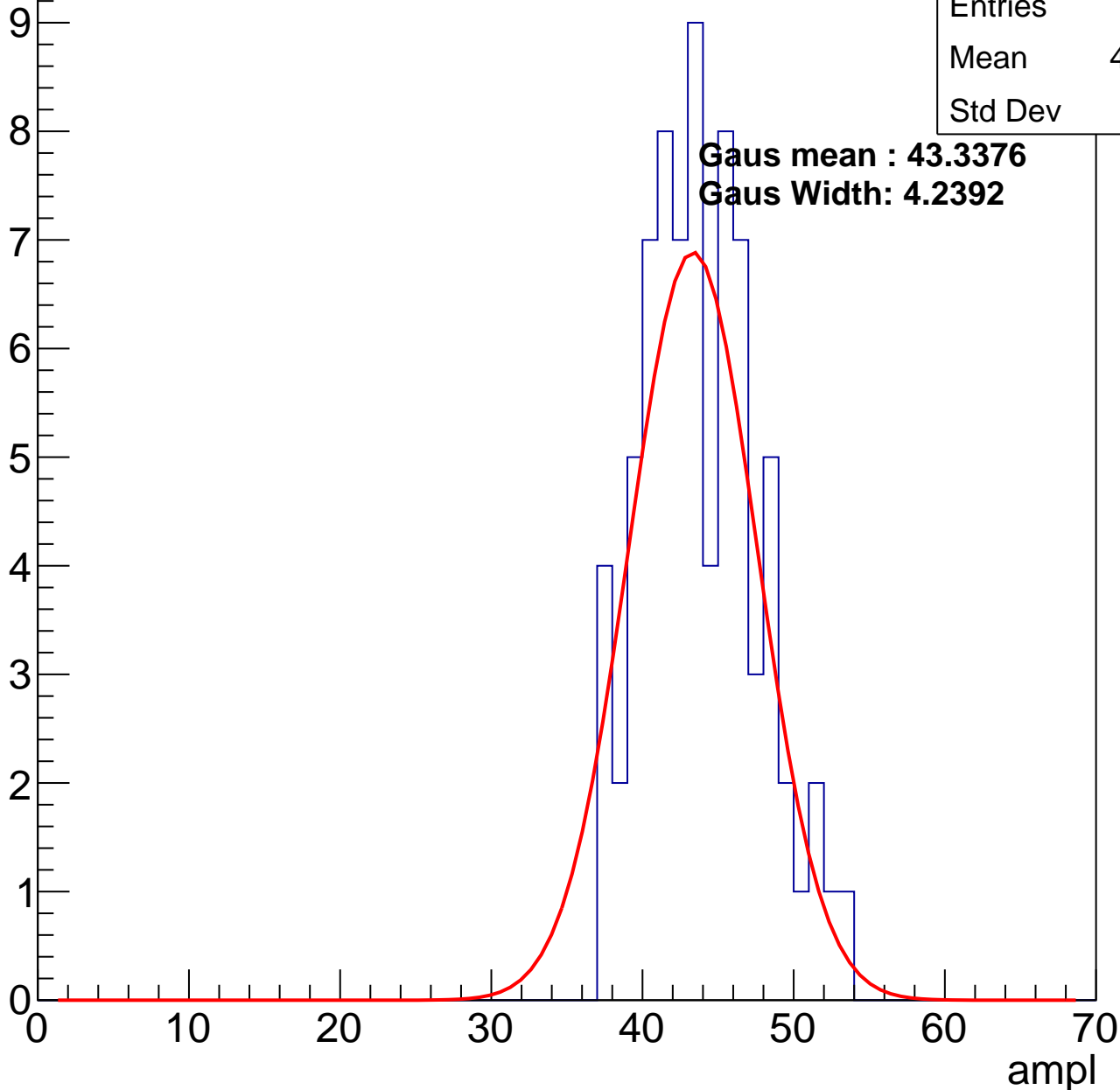
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	76
Mean	43.45
Std Dev	3.74

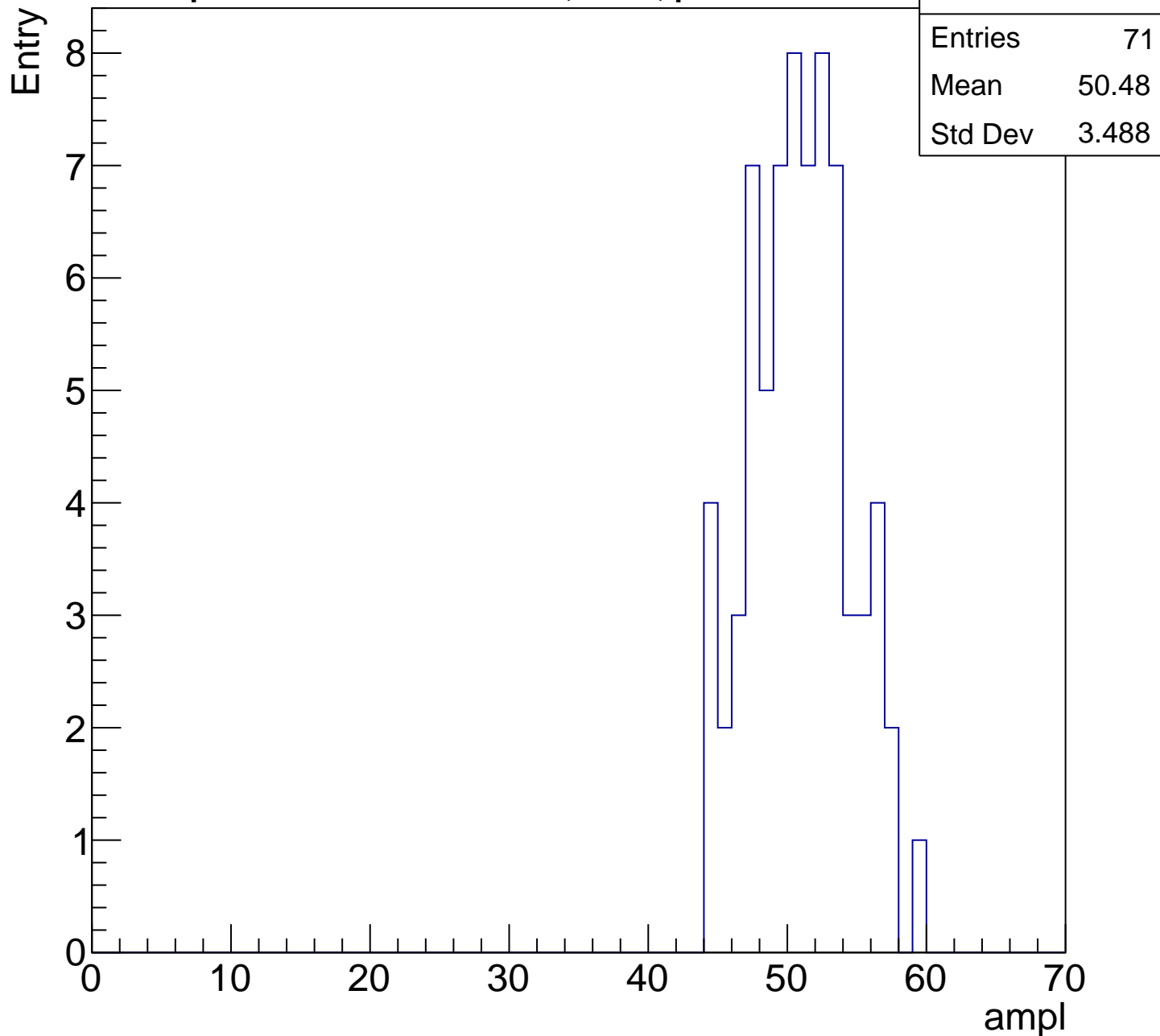
**Gaus mean : 43.3376**

**Gaus Width: 4.2392**



# B1L101S, U19-ch35, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

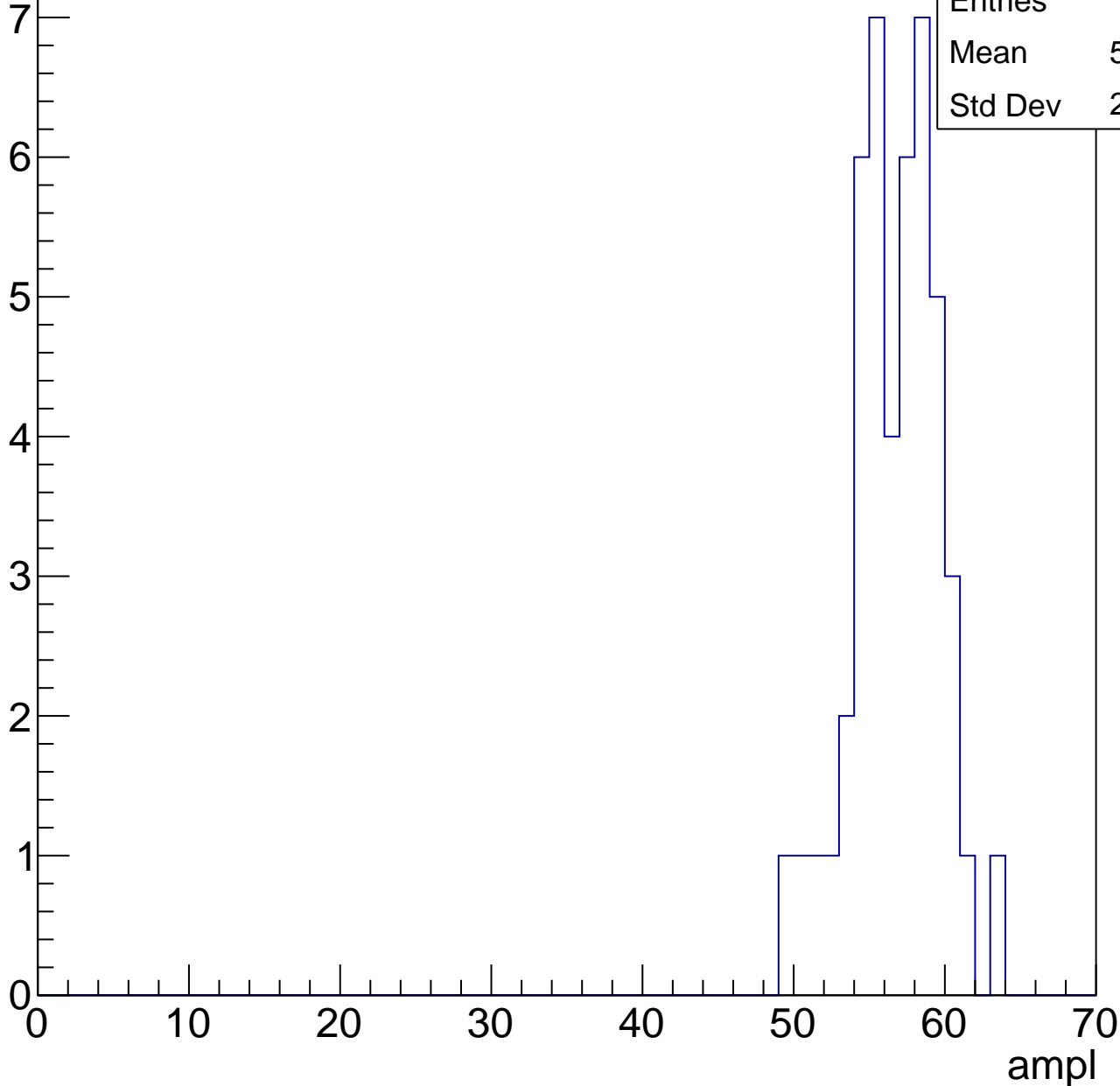


# B1L101S, U19-ch35, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	46
Mean	56.26
Std Dev	2.847

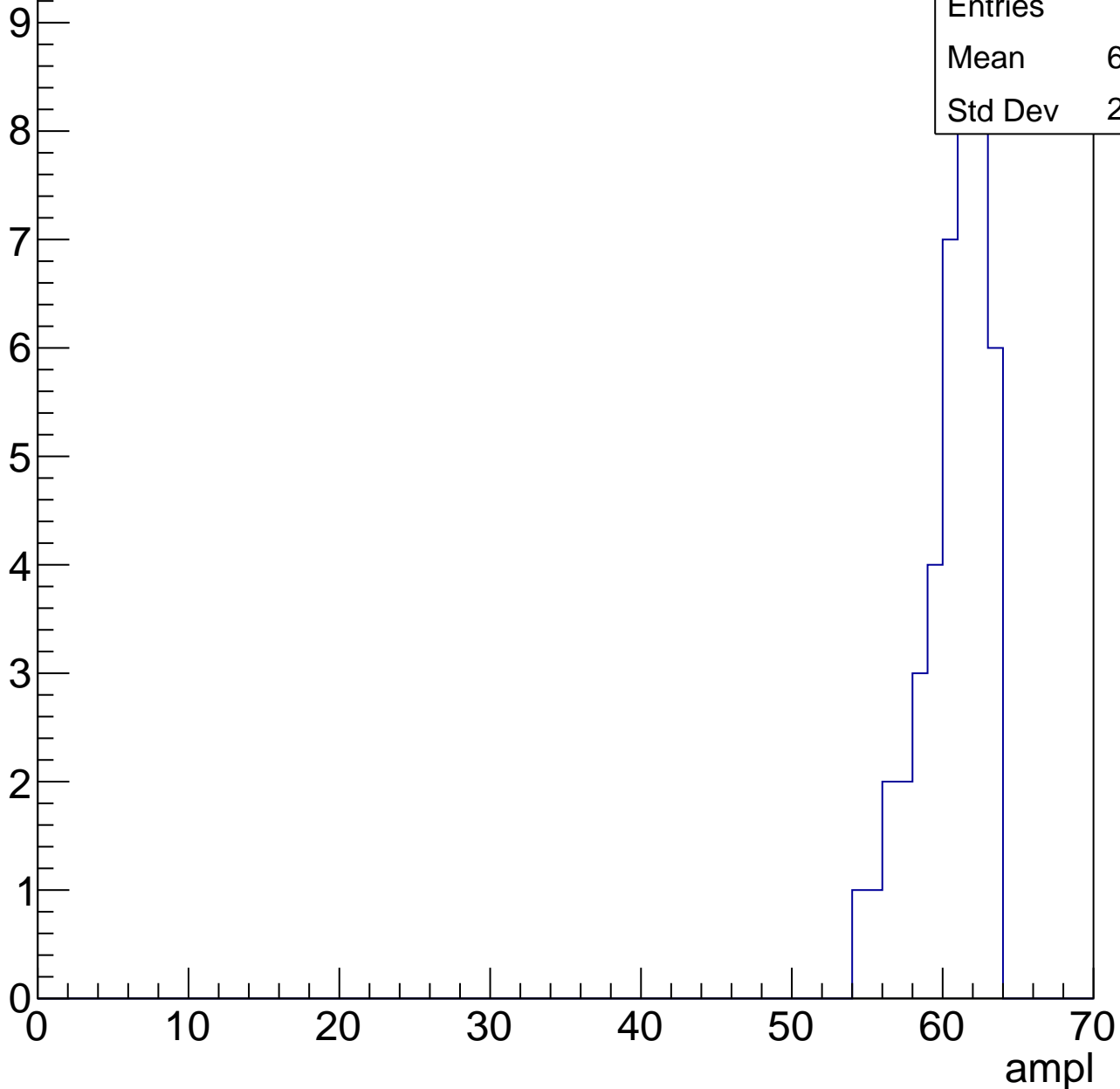


# B1L101S, U19-ch35, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	43
Mean	60.19
Std Dev	2.265



# B1L101S, U19-ch35, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U19-ch35, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U19-ch36, adc0

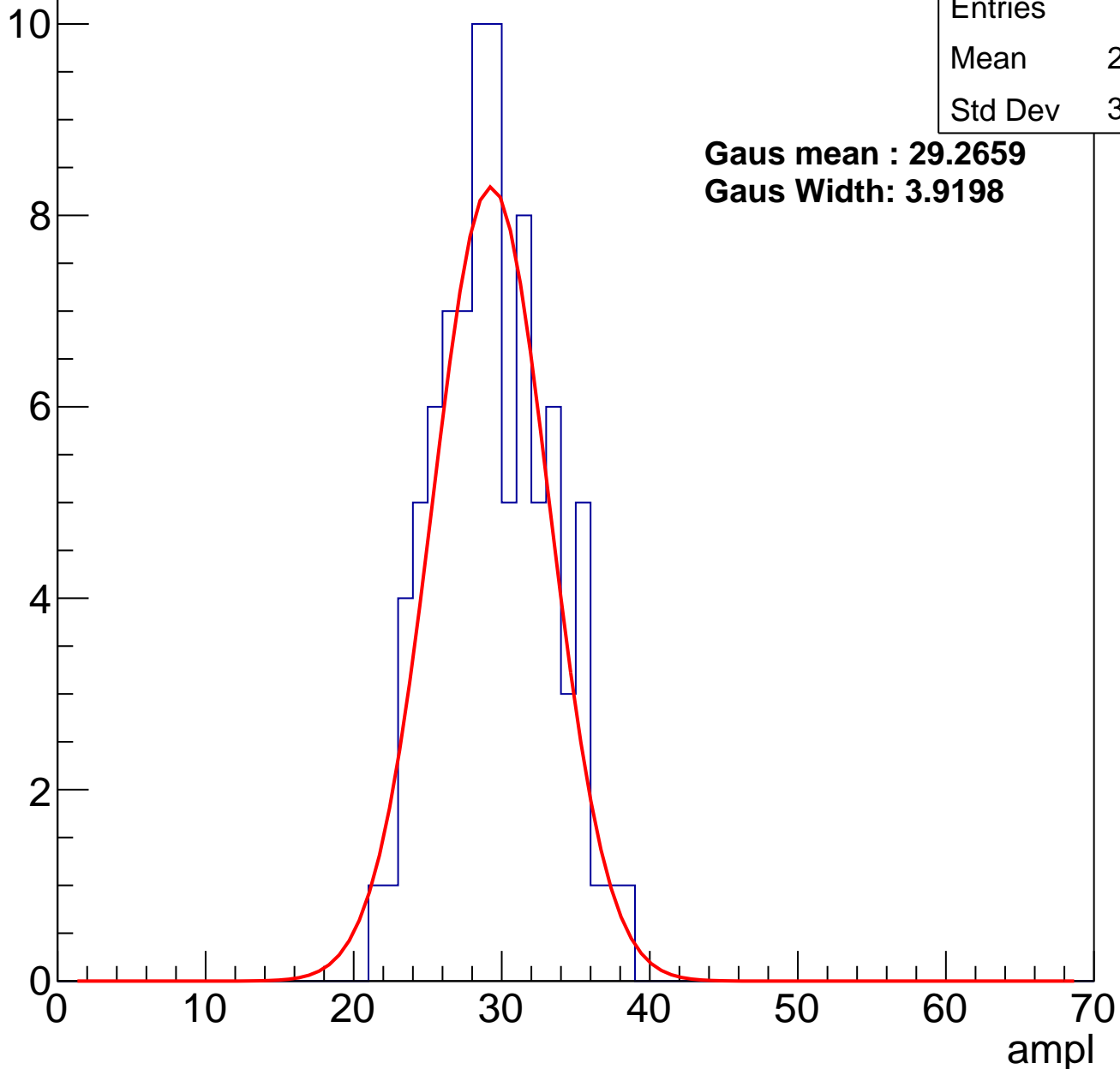
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	86
Mean	28.95
Std Dev	3.744

**Gaus mean : 29.2659**

**Gaus Width: 3.9198**

Entry



# B1L101S, U19-ch36, adc1

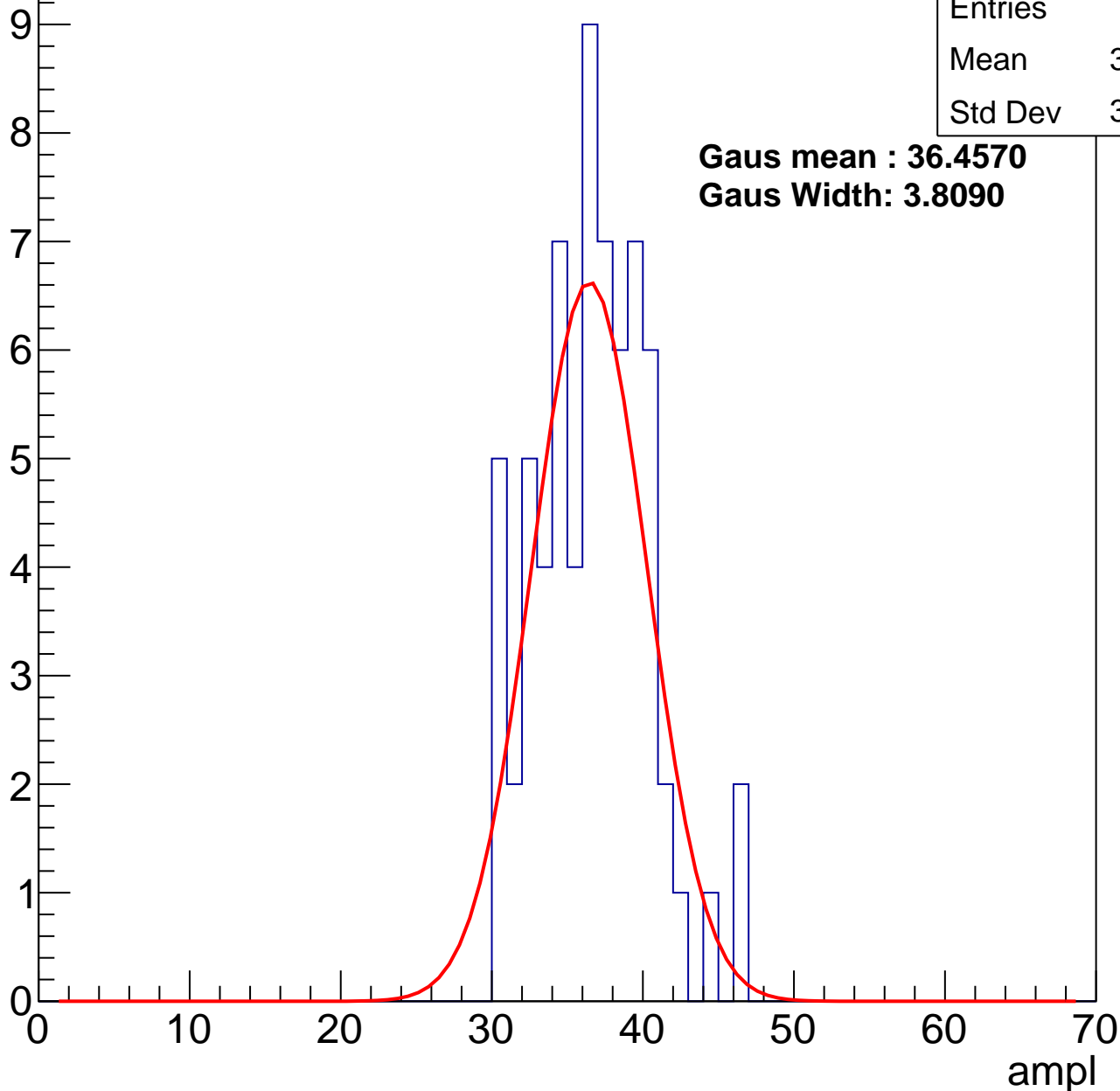
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	36.26
Std Dev	3.665

**Gaus mean : 36.4570**

**Gaus Width: 3.8090**

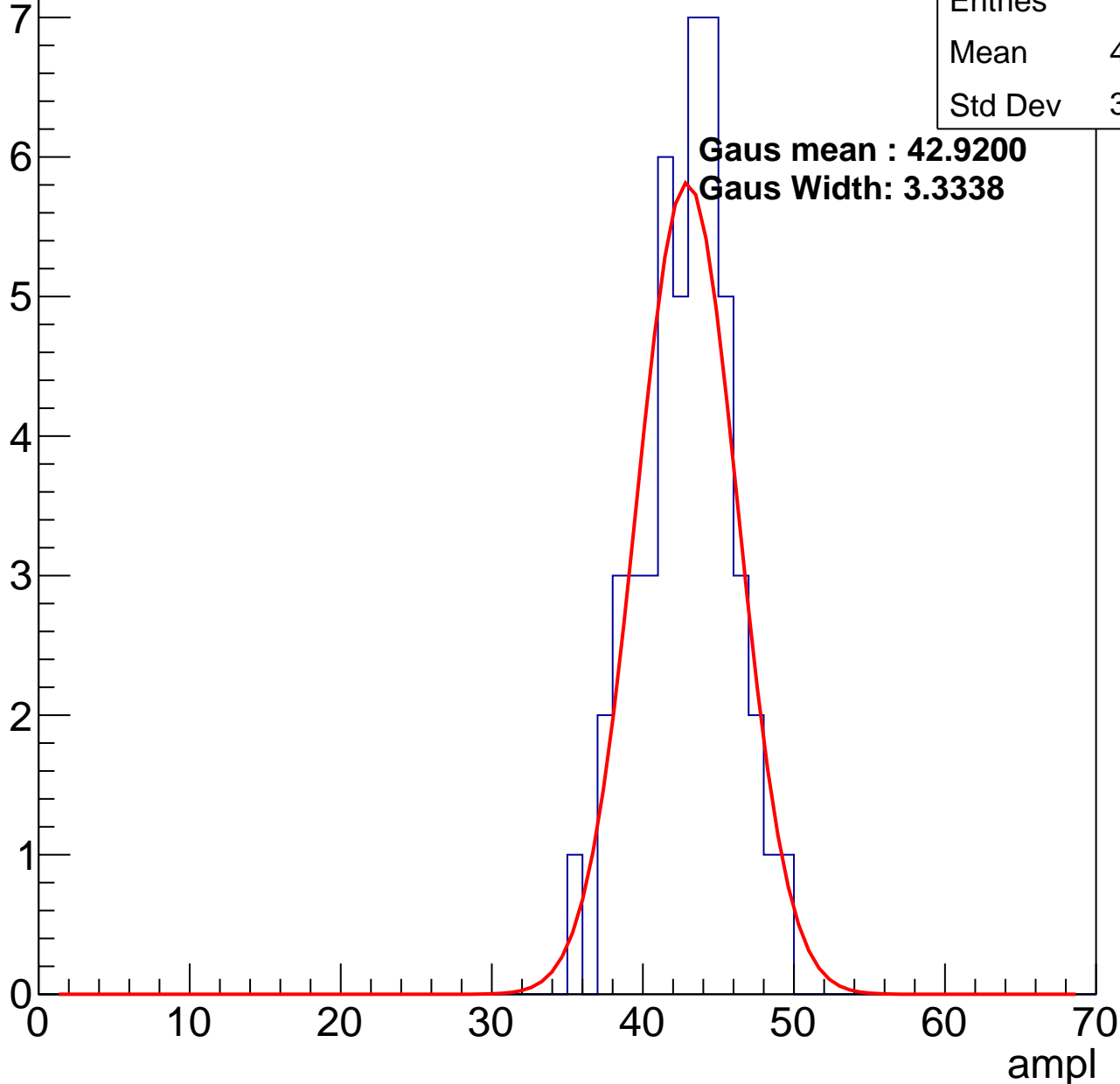


# B1L101S, U19-ch36, adc2

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	49
Mean	42.43
Std Dev	3.017

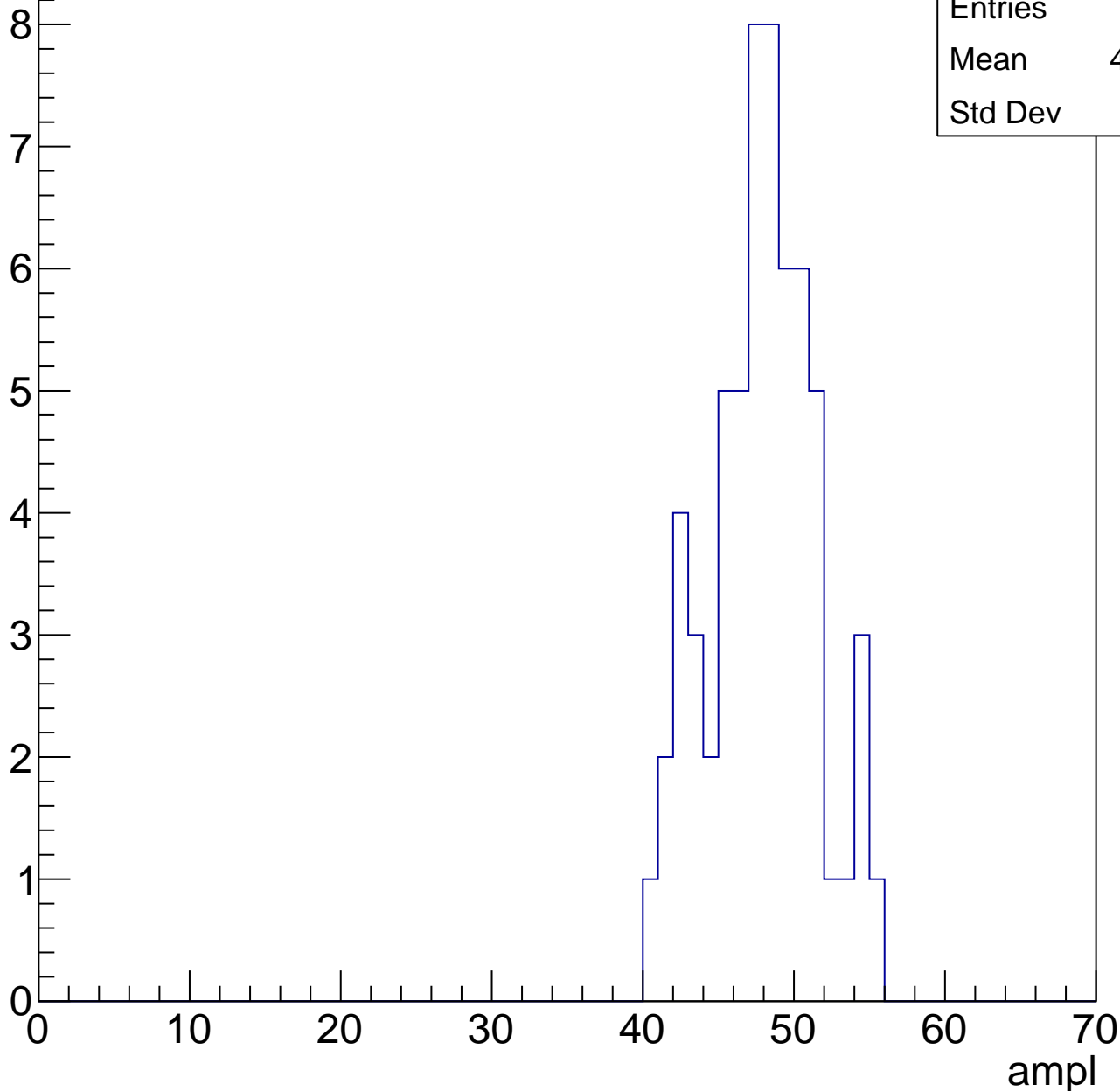


# B1L101S, U19-ch36, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

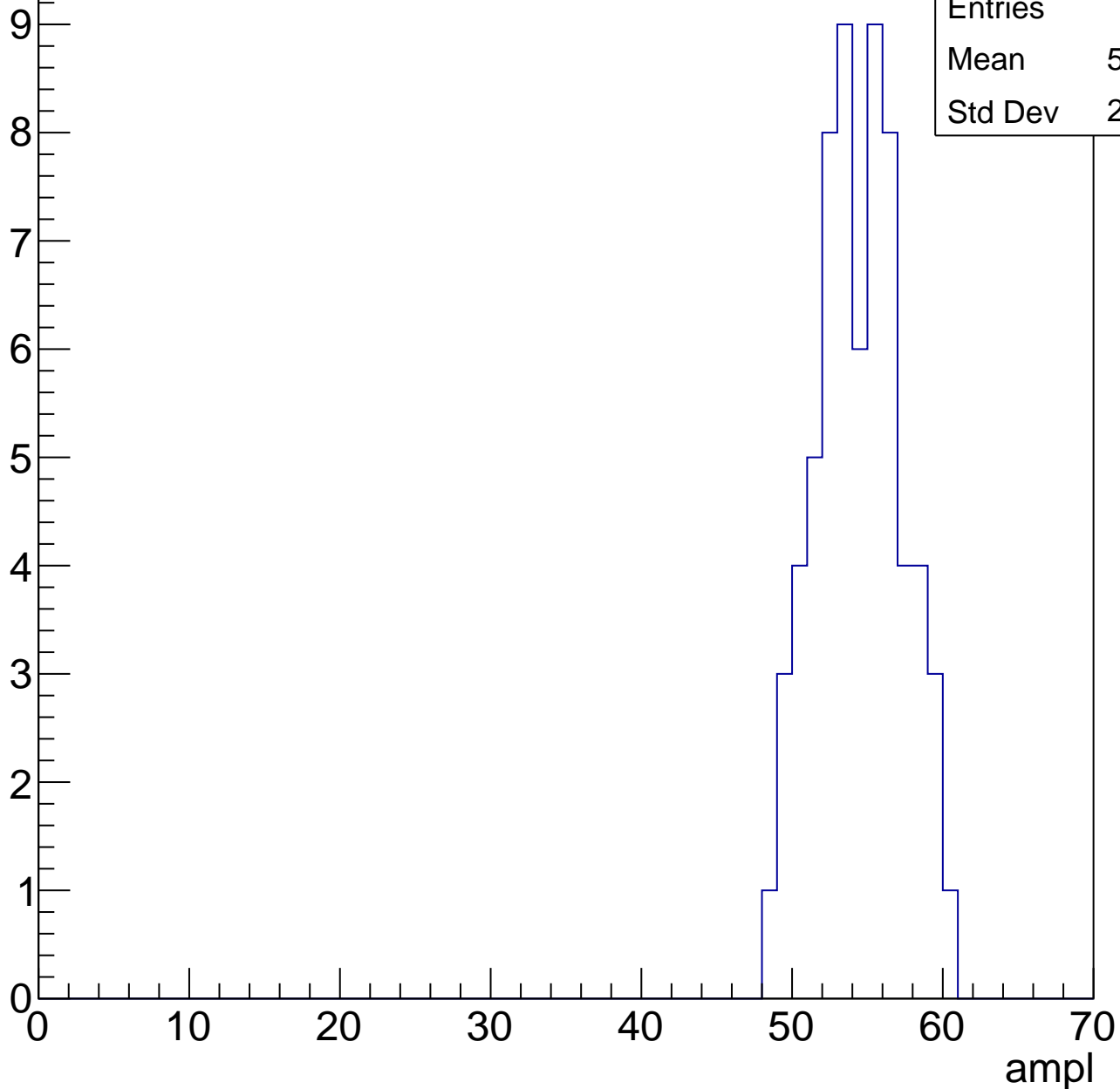
Entries	61
Mean	47.43
Std Dev	3.48



# B1L101S, U19-ch36, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



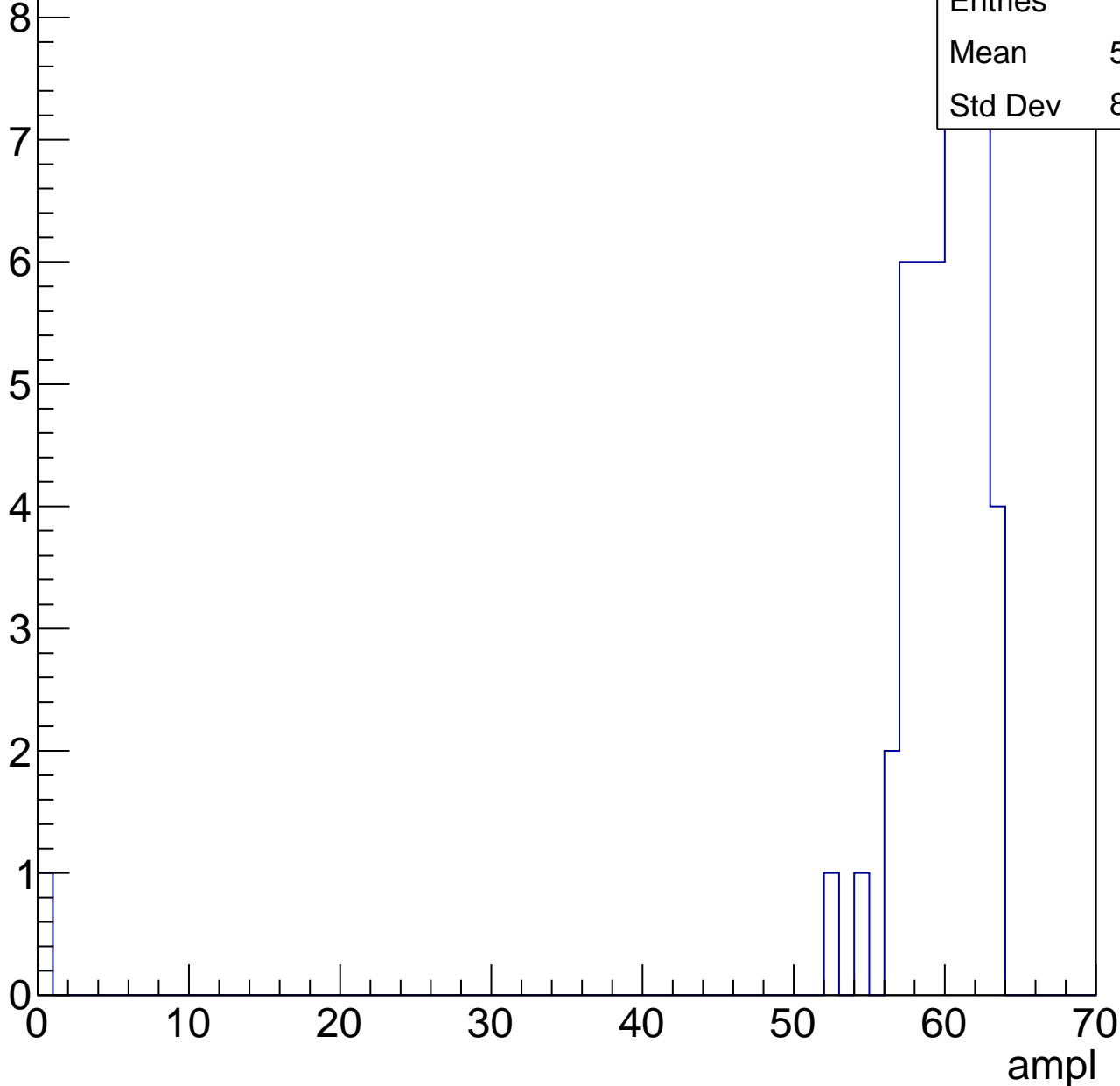
Entries	65
Mean	53.95
Std Dev	2.809

# B1L101S, U19-ch36, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	51
Mean	58.39
Std Dev	8.587

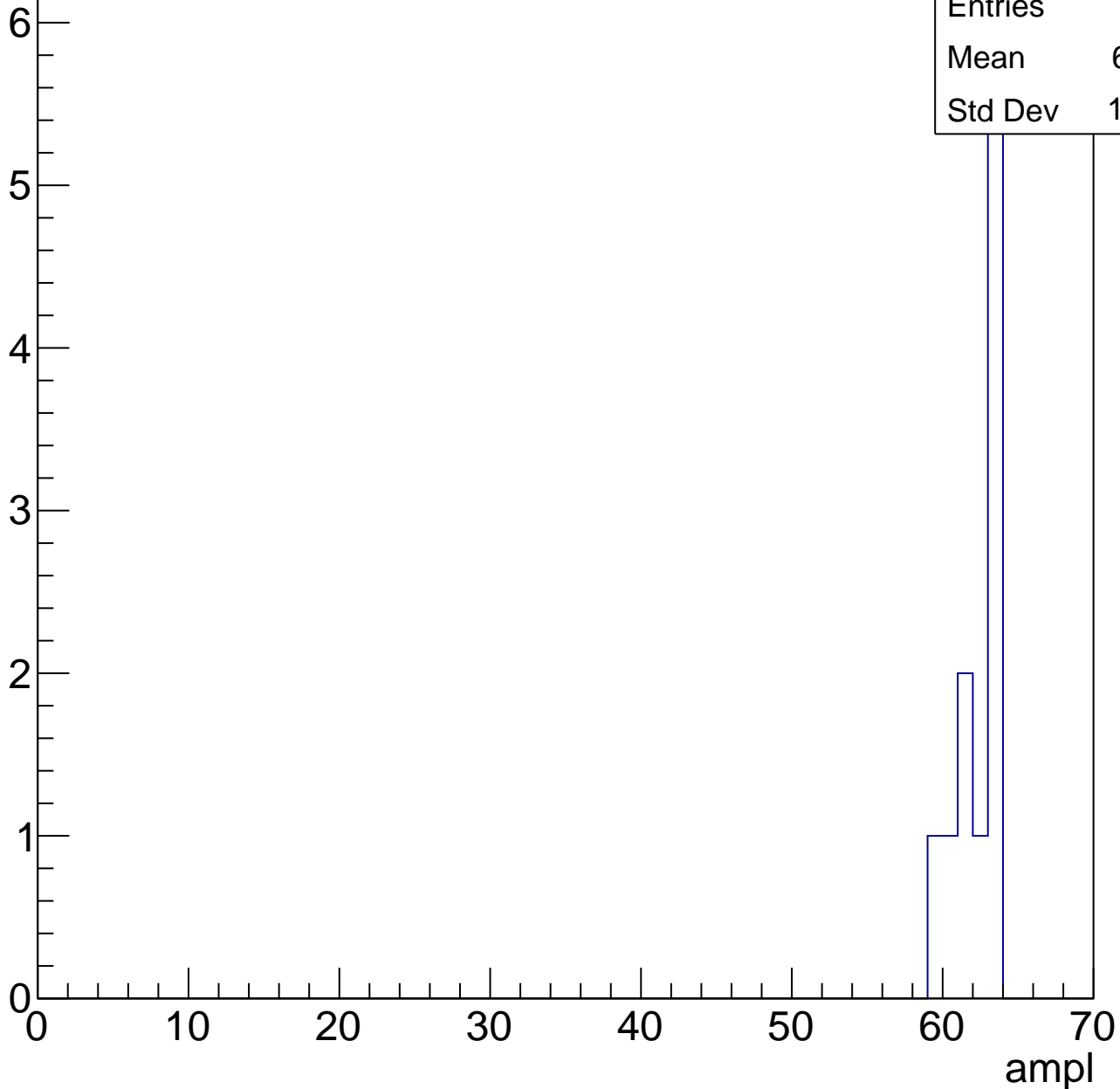


# B1L101S, U19-ch36, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	11
Mean	61.91
Std Dev	1.379





# B1L101S, U19-ch36, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U19-ch37, adc0

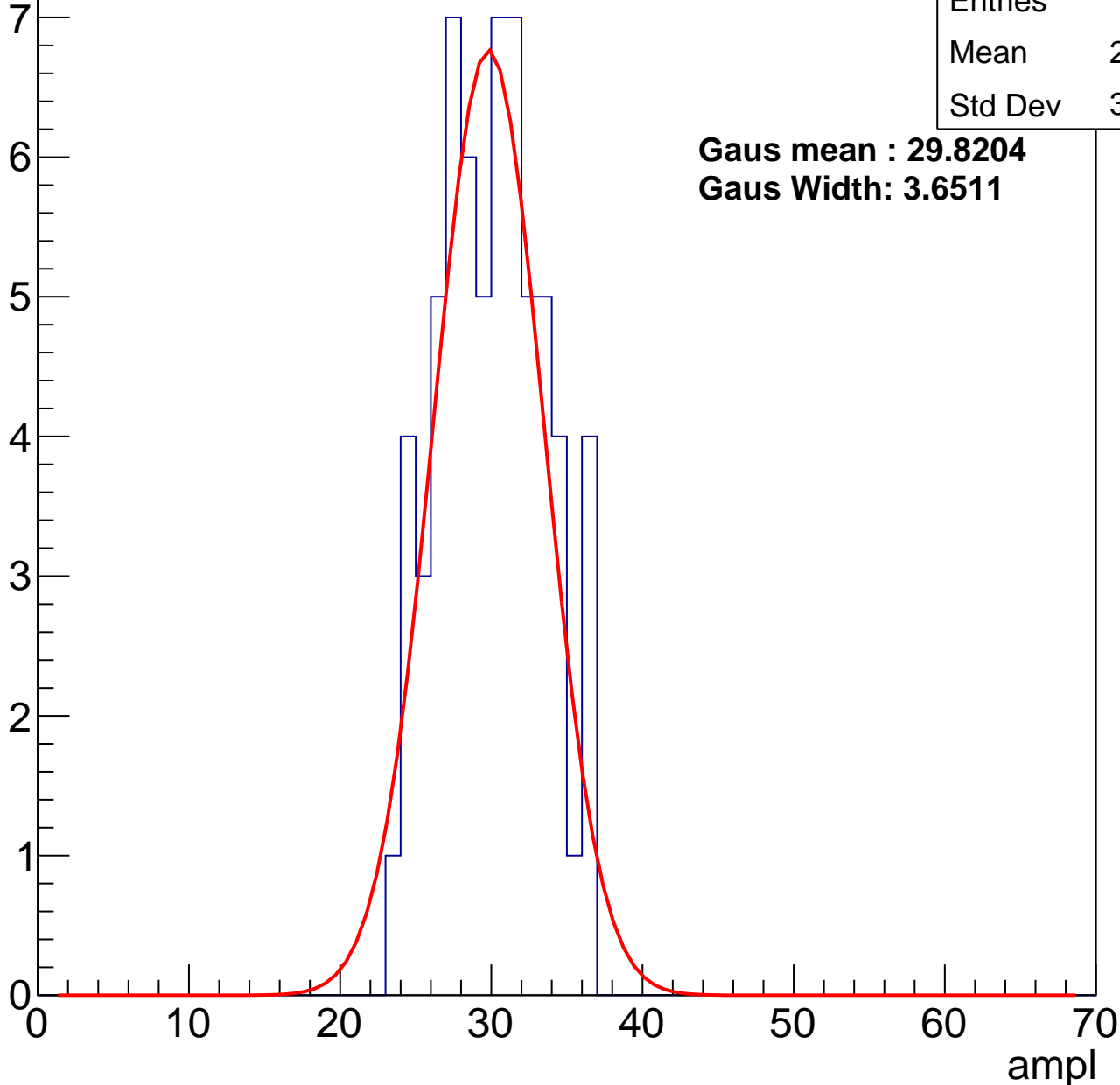
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	29.58
Std Dev	3.386

**Gaus mean : 29.8204**

**Gaus Width: 3.6511**



# B1L101S, U19-ch37, adc1

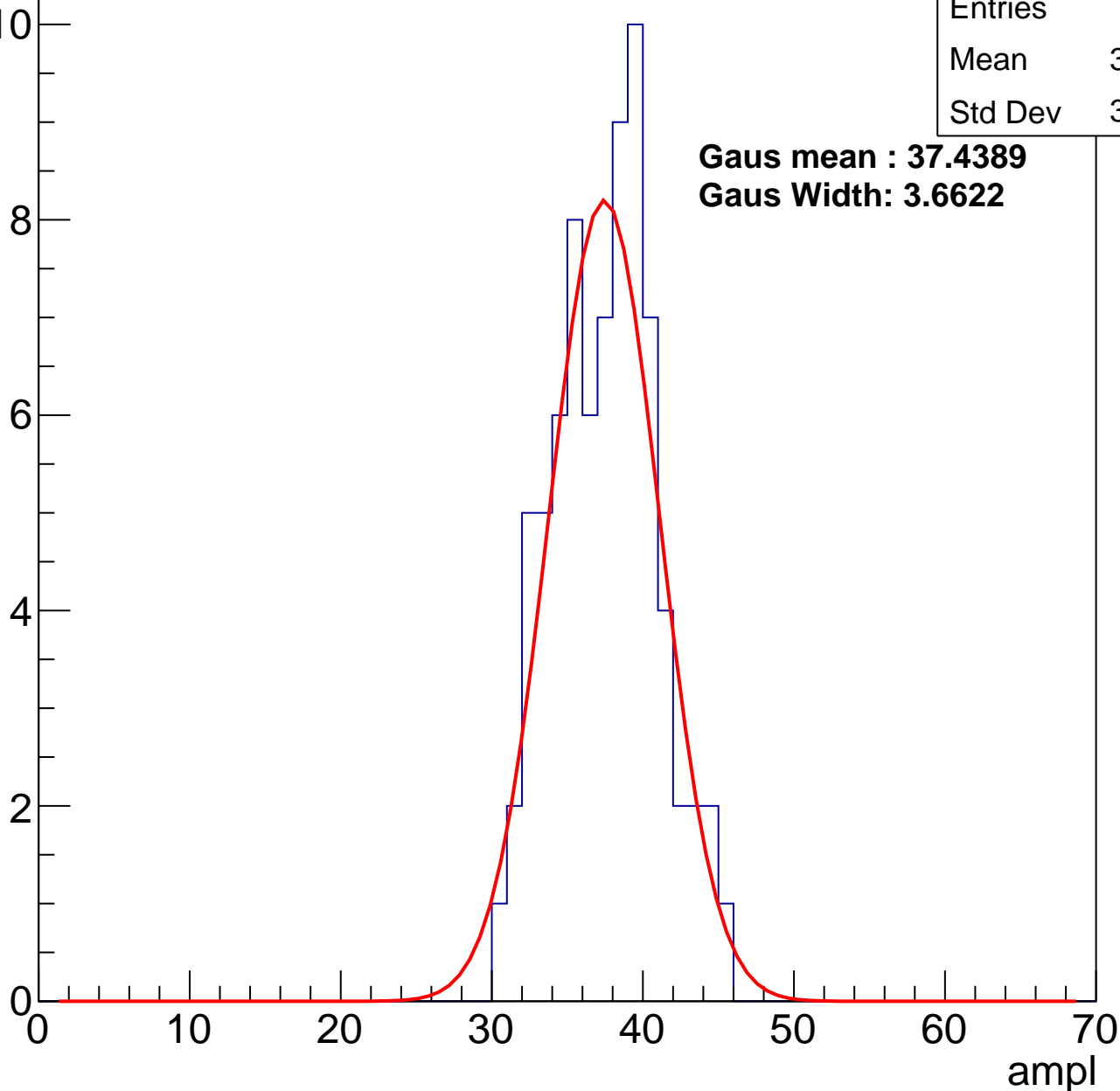
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	77
Mean	37.08
Std Dev	3.376

**Gaus mean : 37.4389**

**Gaus Width: 3.6622**



# B1L101S, U19-ch37, adc2

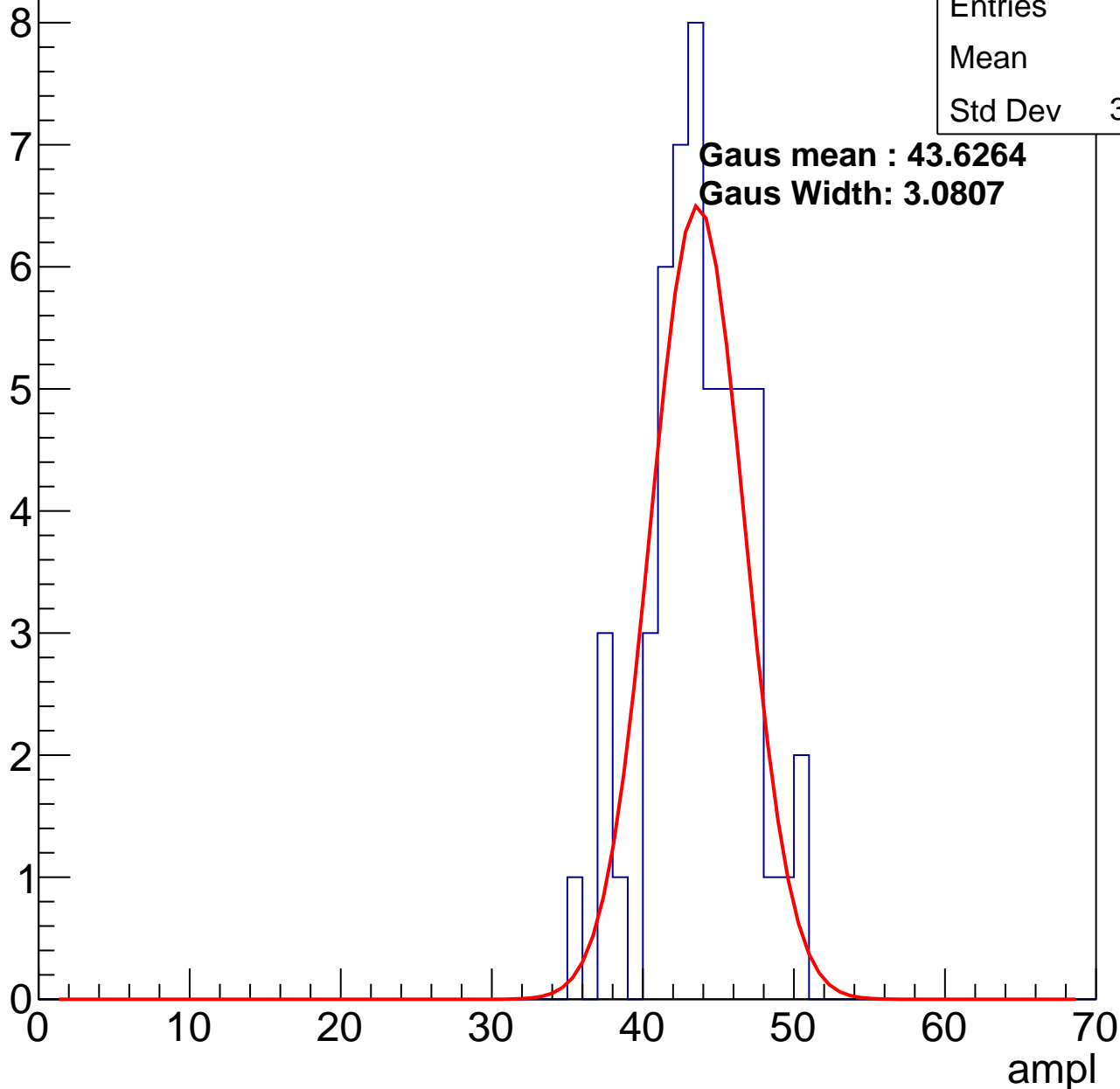
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	53
Mean	43.3
Std Dev	3.248

**Gaus mean : 43.6264**

**Gaus Width: 3.0807**

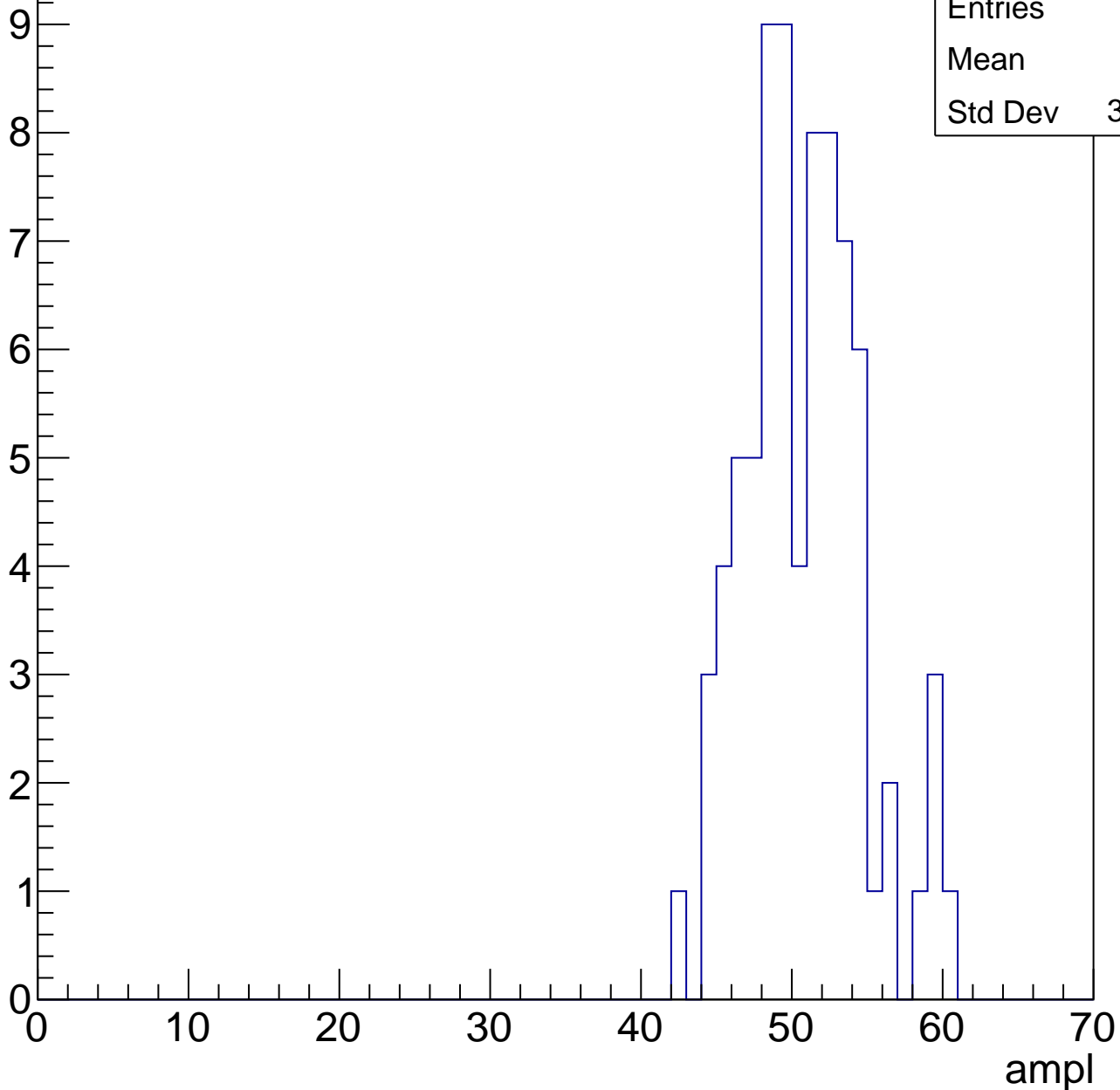


# B1L101S, U19-ch37, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

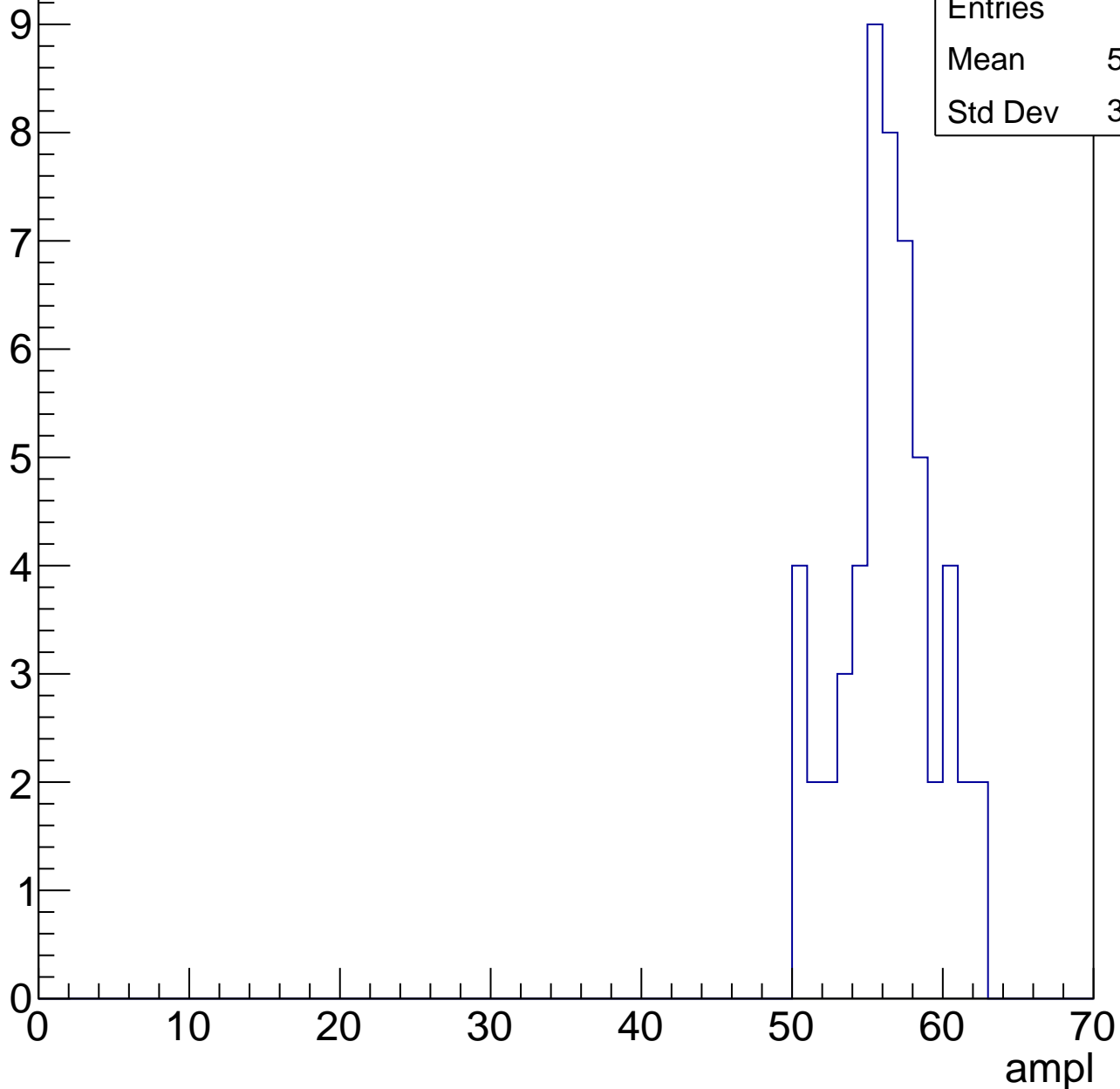
Entries	77
Mean	50.3
Std Dev	3.845



# B1L101S, U19-ch37, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U19-ch37, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	43
Mean	59.3
Std Dev	9.342

Entry

10

8

6

4

2

0

0

10

20

30

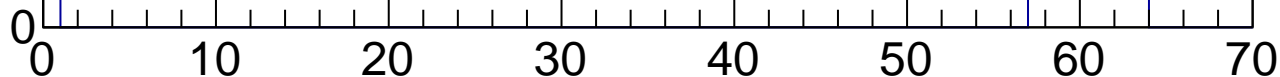
40

50

60

70

ampl



# B1L101S, U19-ch37, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	62
Std Dev	0



# B1L101S, U19-ch37, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U19-ch38, adc0

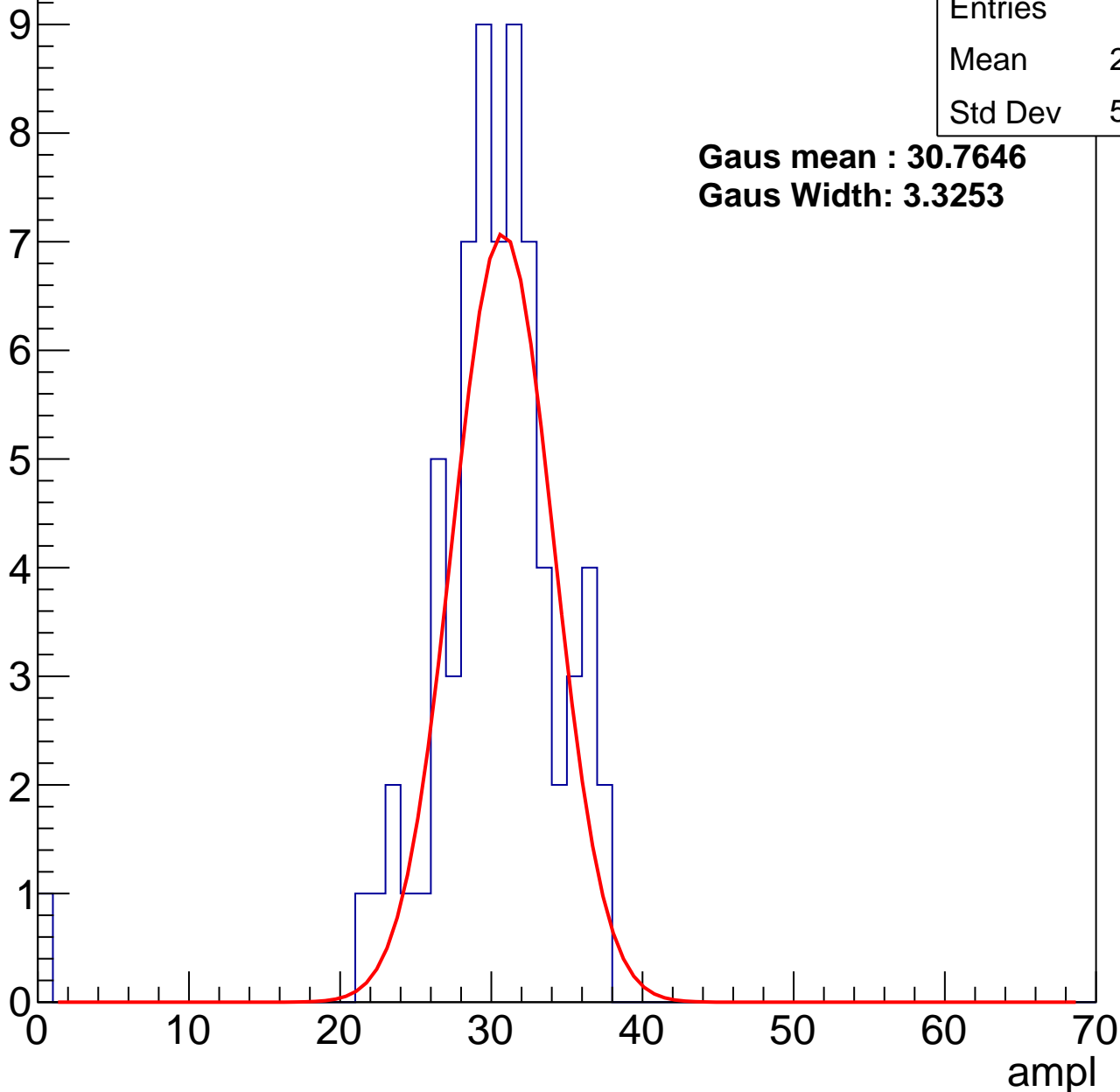
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	29.59
Std Dev	5.049

**Gaus mean : 30.7646**

**Gaus Width: 3.3253**



# B1L101S, U19-ch38, adc1

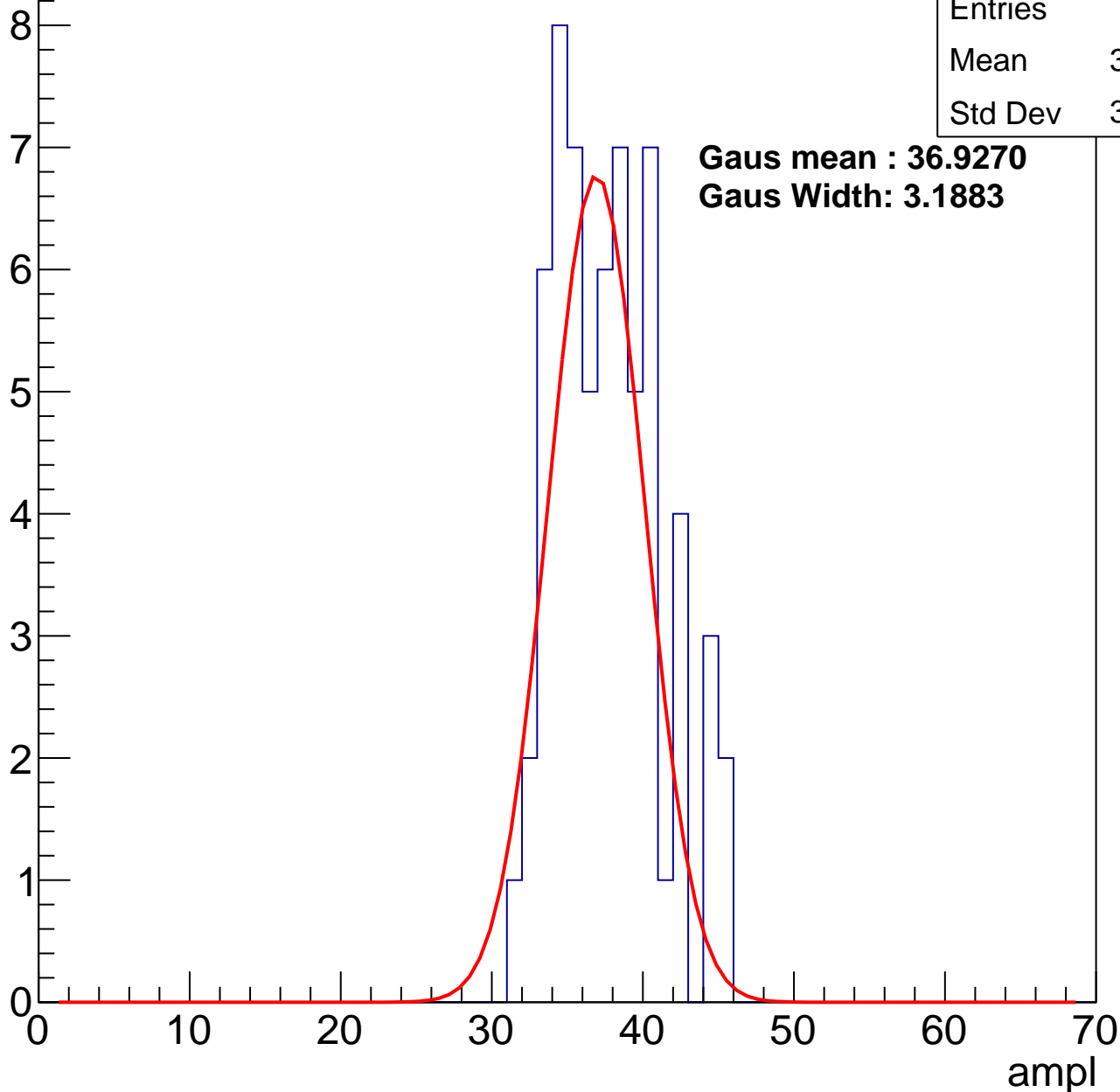
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	37.25
Std Dev	3.455

**Gaus mean : 36.9270**

**Gaus Width: 3.1883**



# B1L101S, U19-ch38, adc2

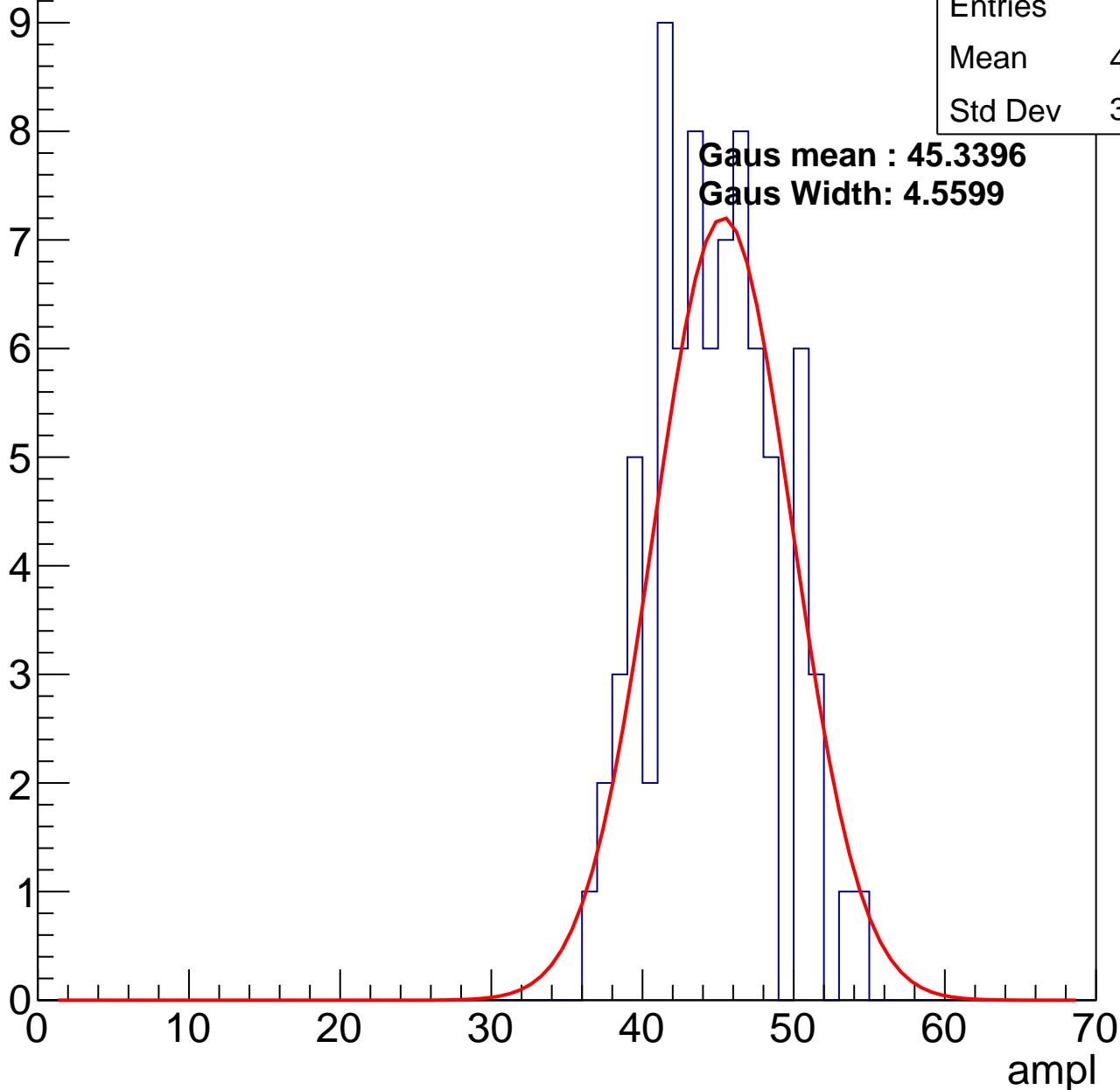
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	79
Mean	44.22
Std Dev	3.983

**Gaus mean : 45.3396**

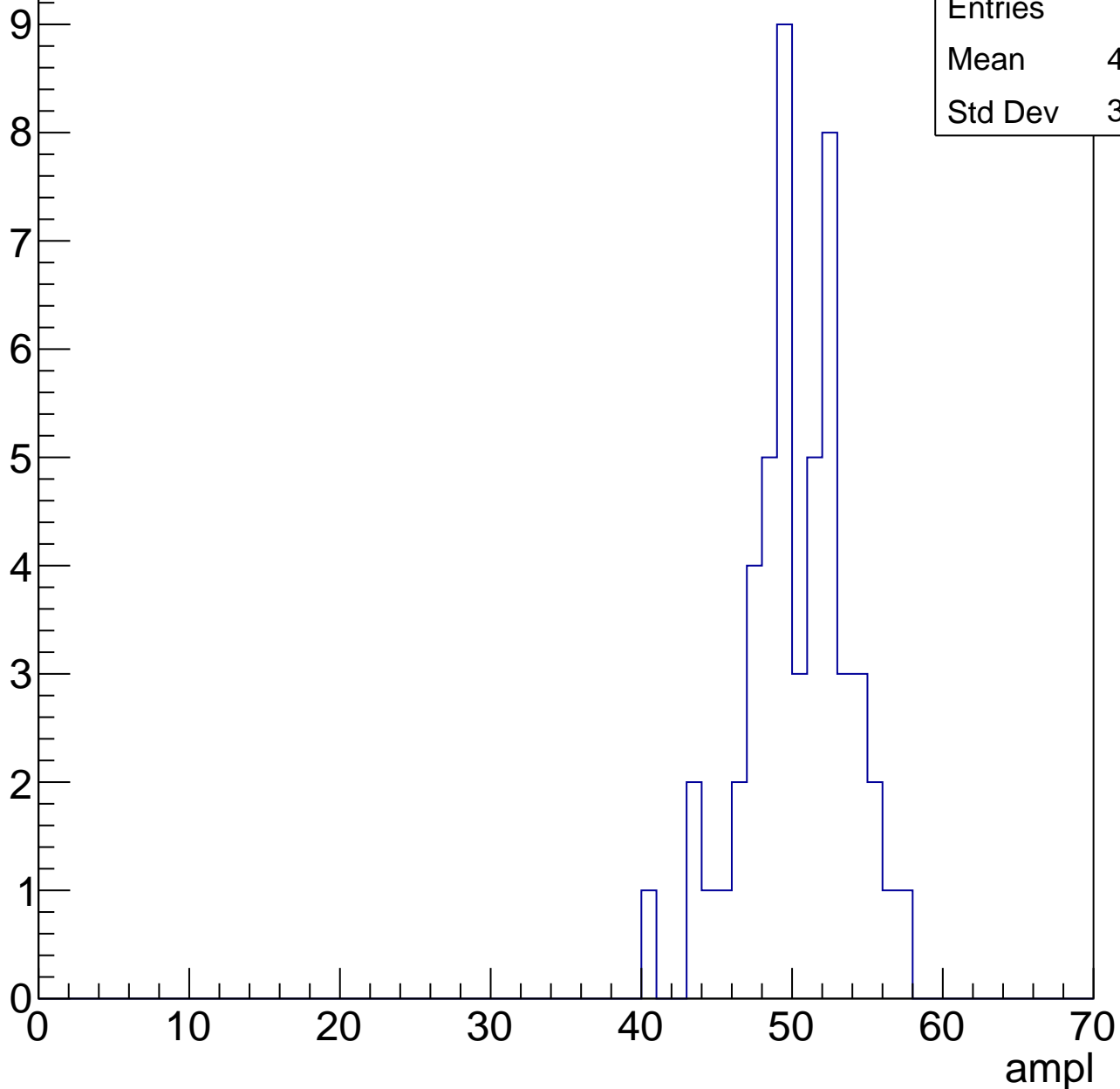
**Gaus Width: 4.5599**



# B1L101S, U19-ch38, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

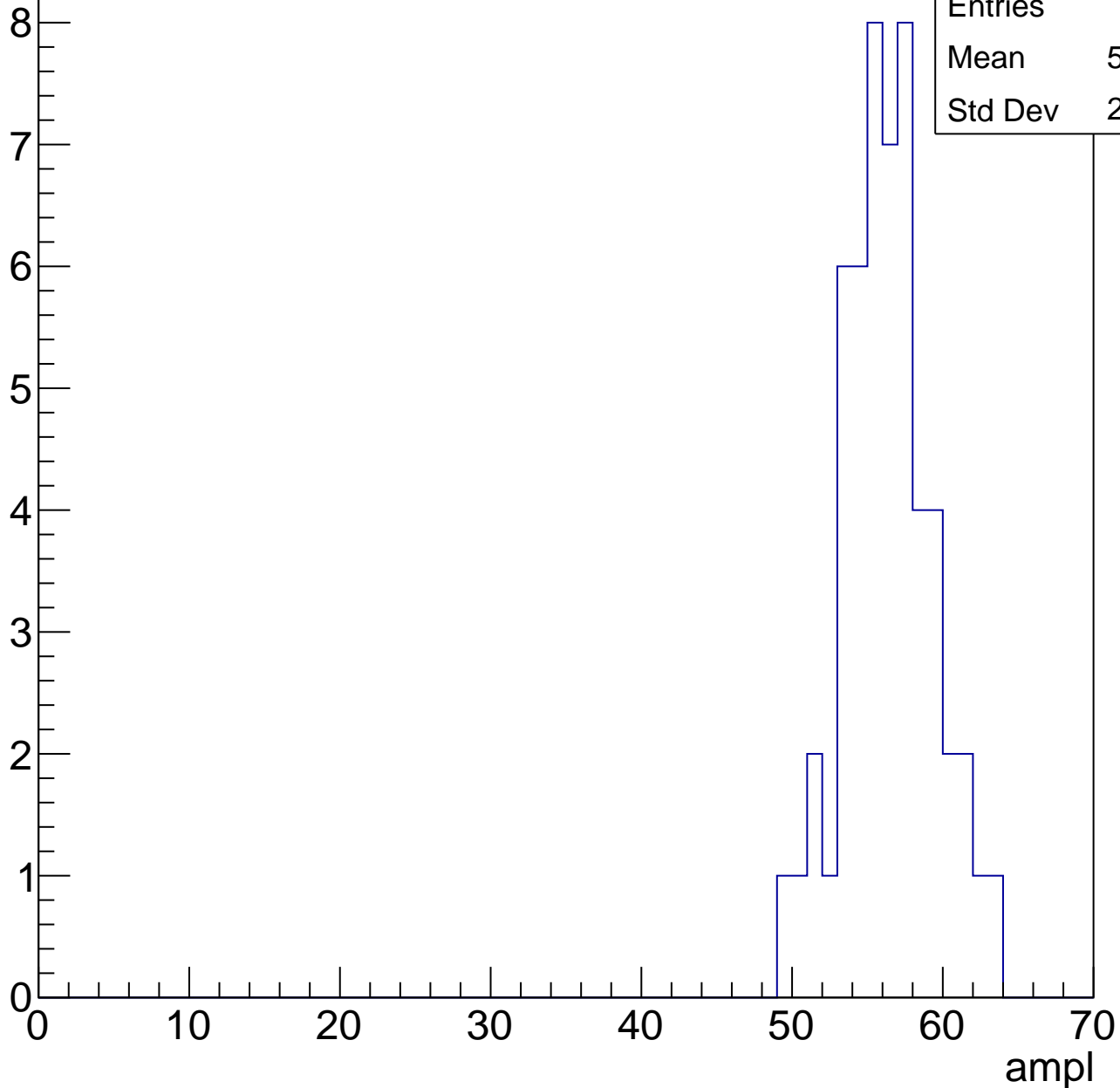
Entry



# B1L101S, U19-ch38, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

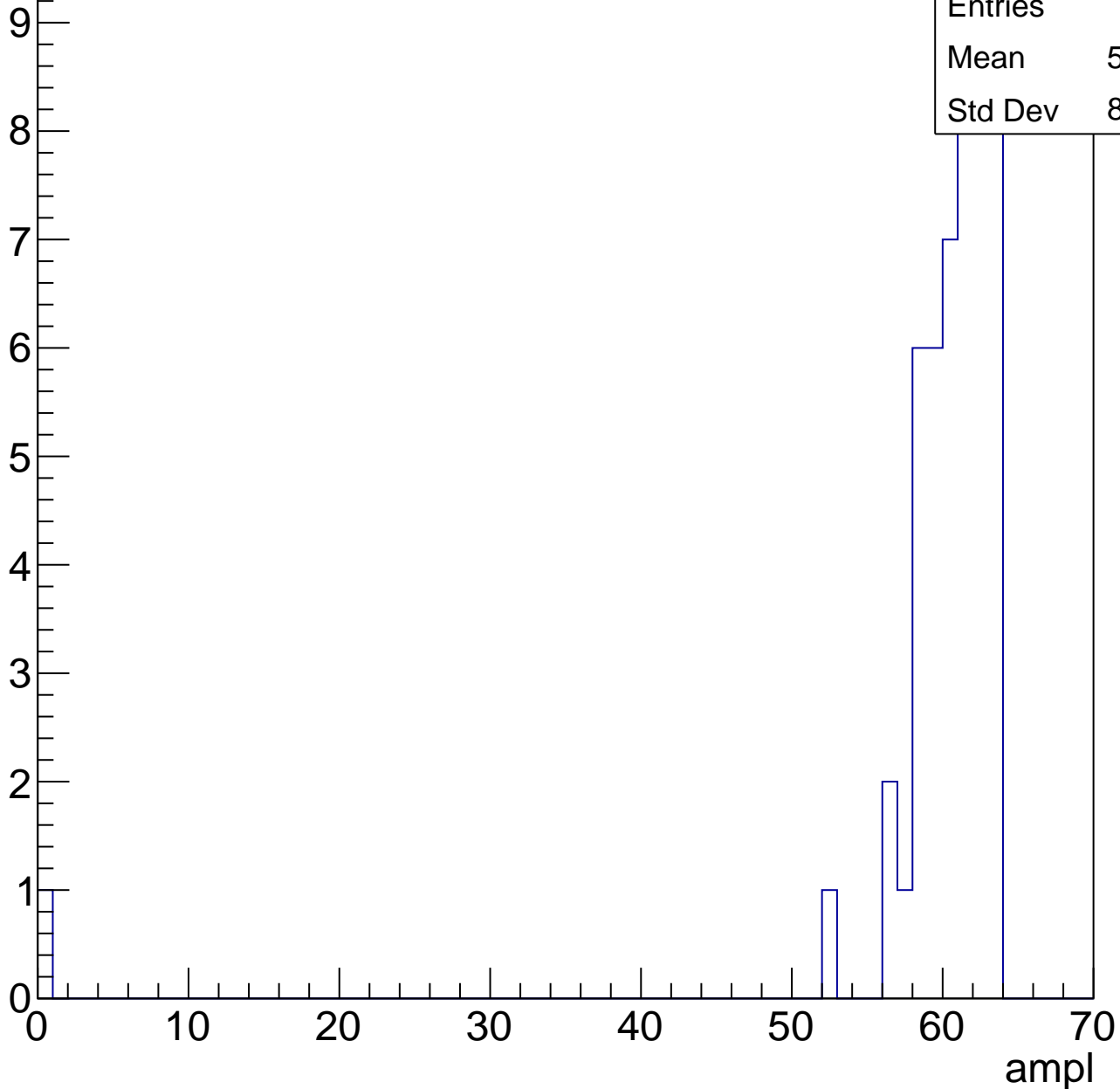


# B1L101S, U19-ch38, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	49
Mean	59.04
Std Dev	8.813



# B1L101S, U19-ch38, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U19-ch38, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U19-ch39, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	71
Mean	29.31
Std Dev	3.093

**Gaus mean : 29.9024**

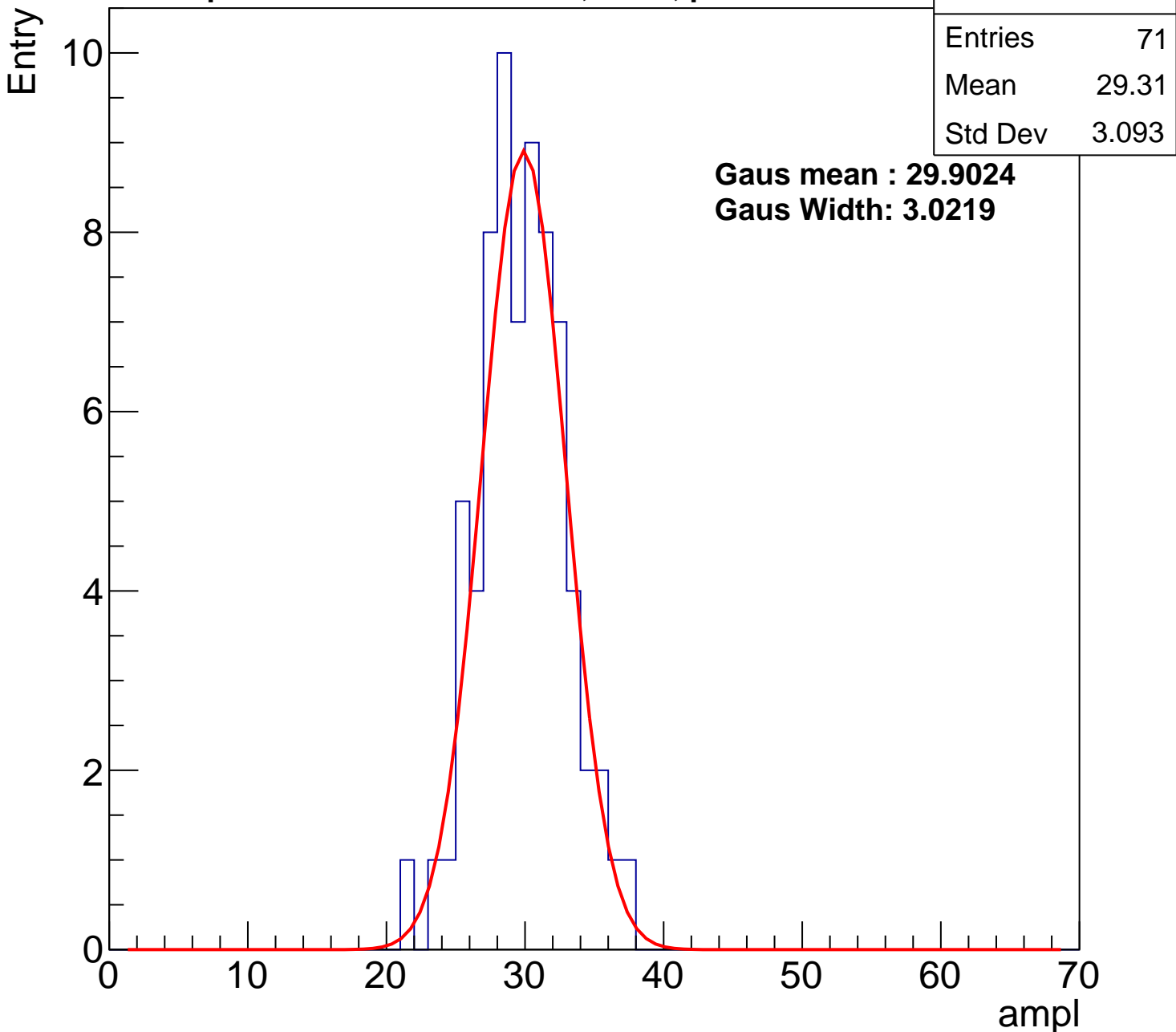
**Gaus Width: 3.0219**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



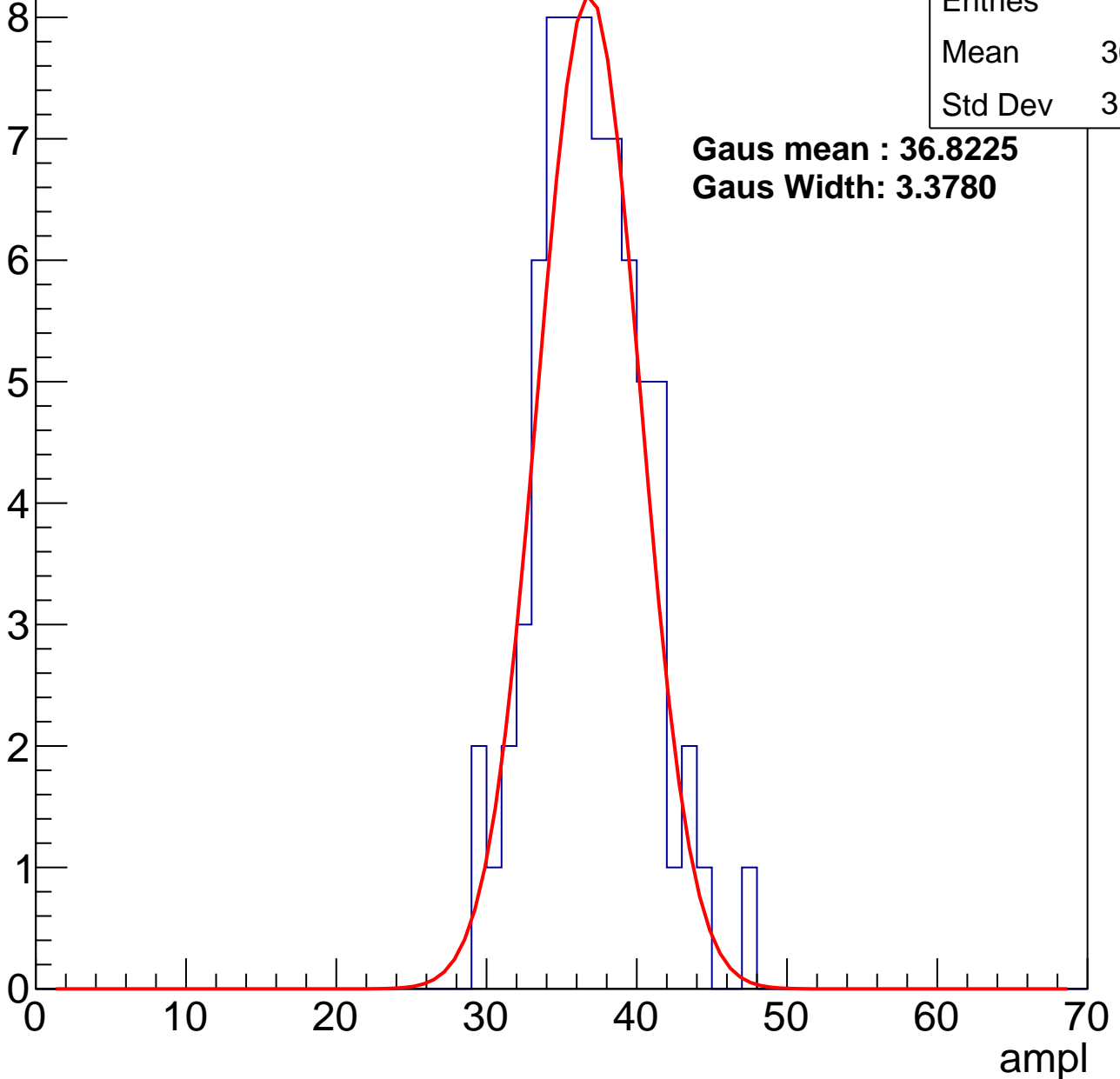
# B1L101S, U19-ch39, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	73
Mean	36.53
Std Dev	3.546

**Gaus mean : 36.8225**  
**Gaus Width: 3.3780**

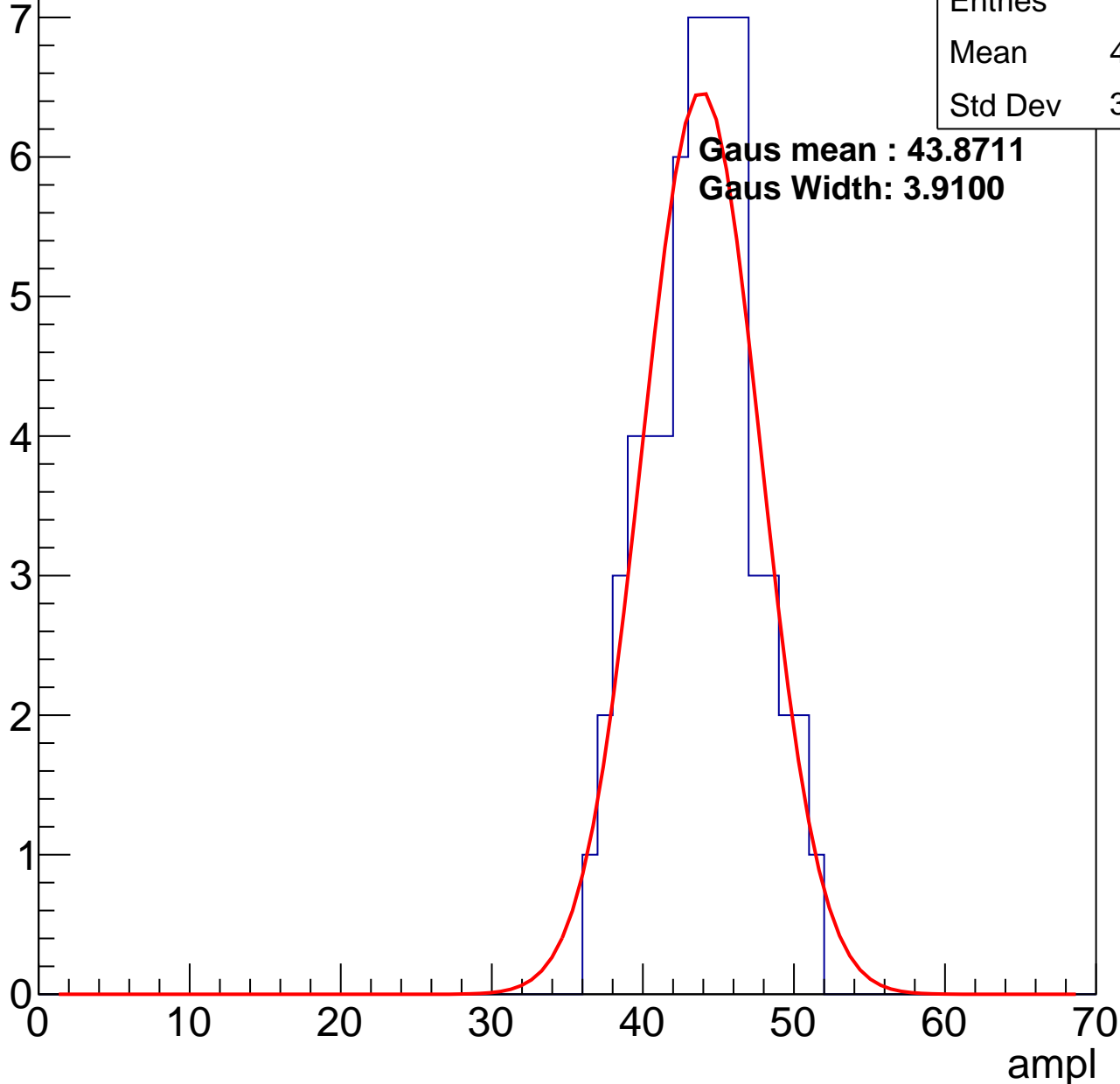


# B1L101S, U19-ch39, adc2

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

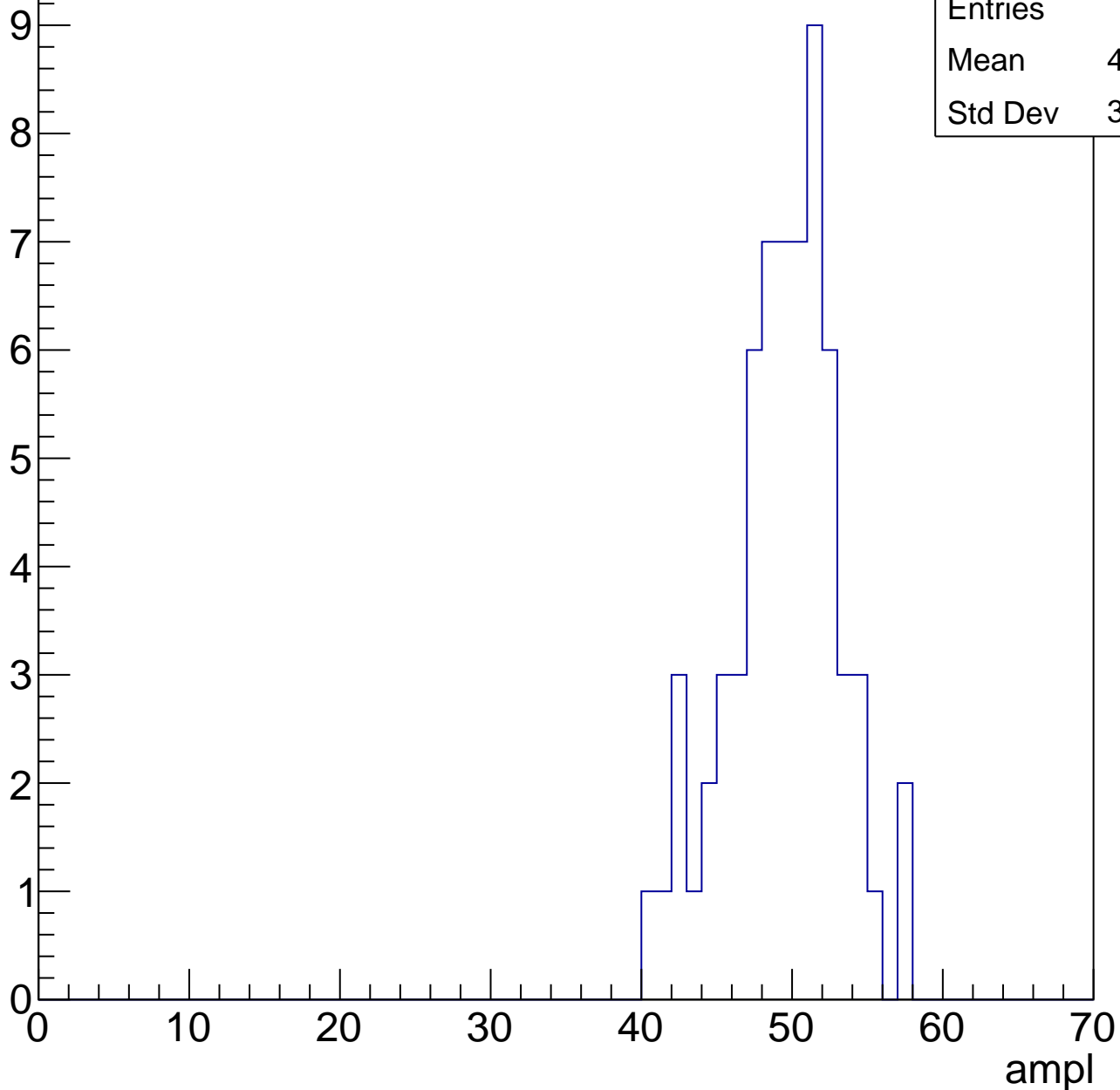
Entries	63
Mean	43.43
Std Dev	3.477



# B1L101S, U19-ch39, adc3

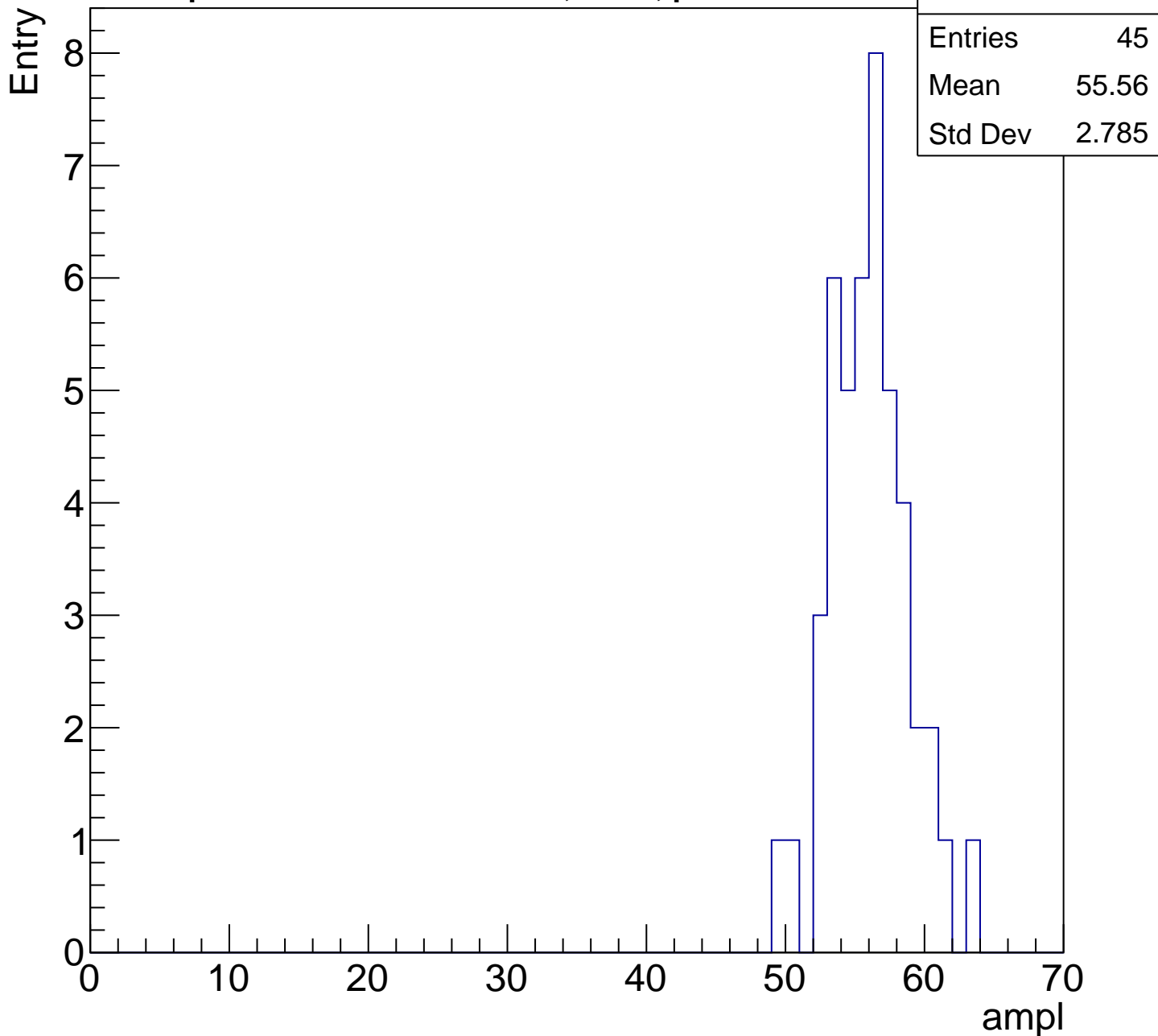
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U19-ch39, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U19-ch39, adc5

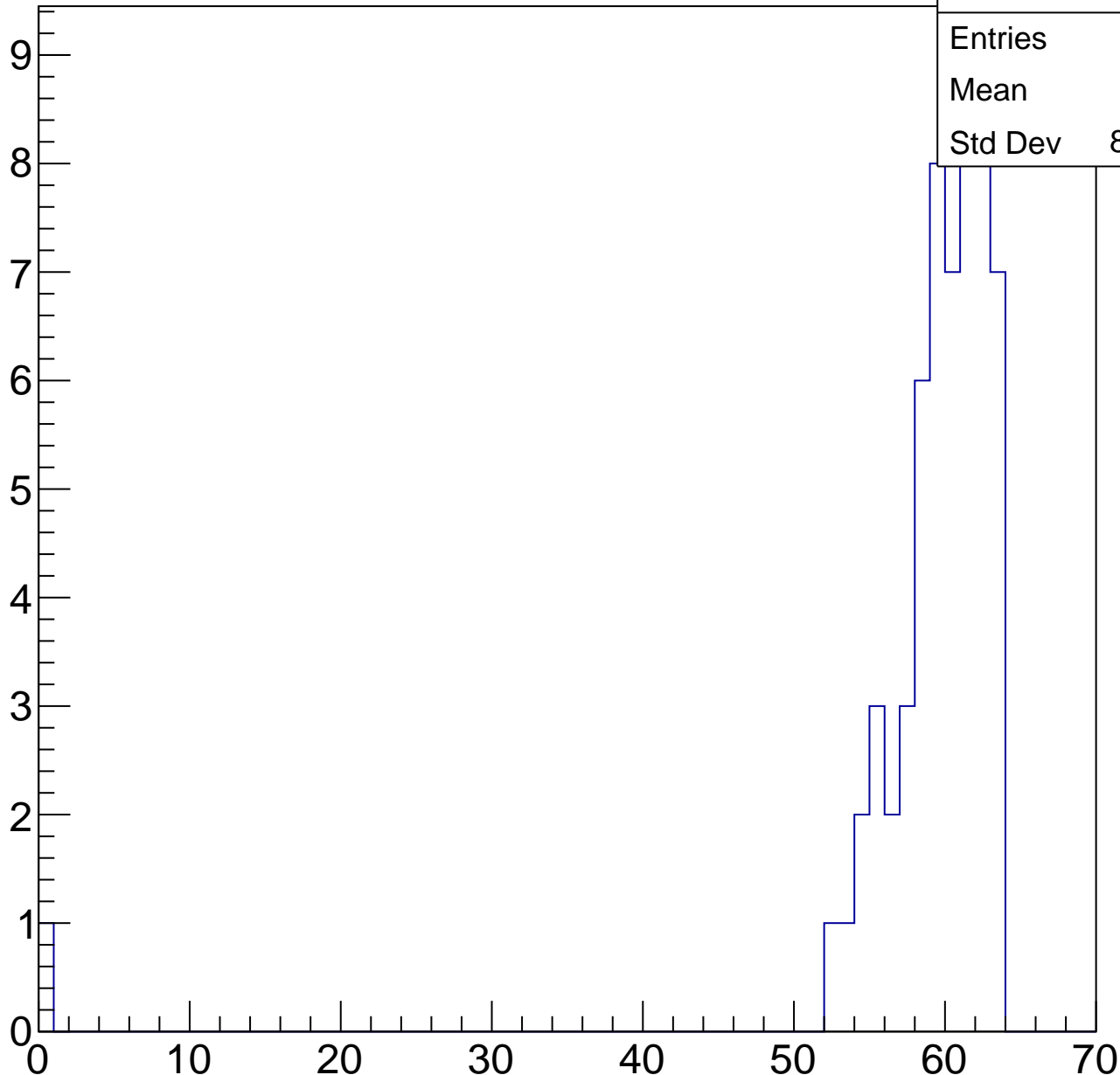
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	58
Mean	58.4
Std Dev	8.206

ampl



# B1L101S, U19-ch39, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	4
Mean	61.75
Std Dev	1.09

ampl

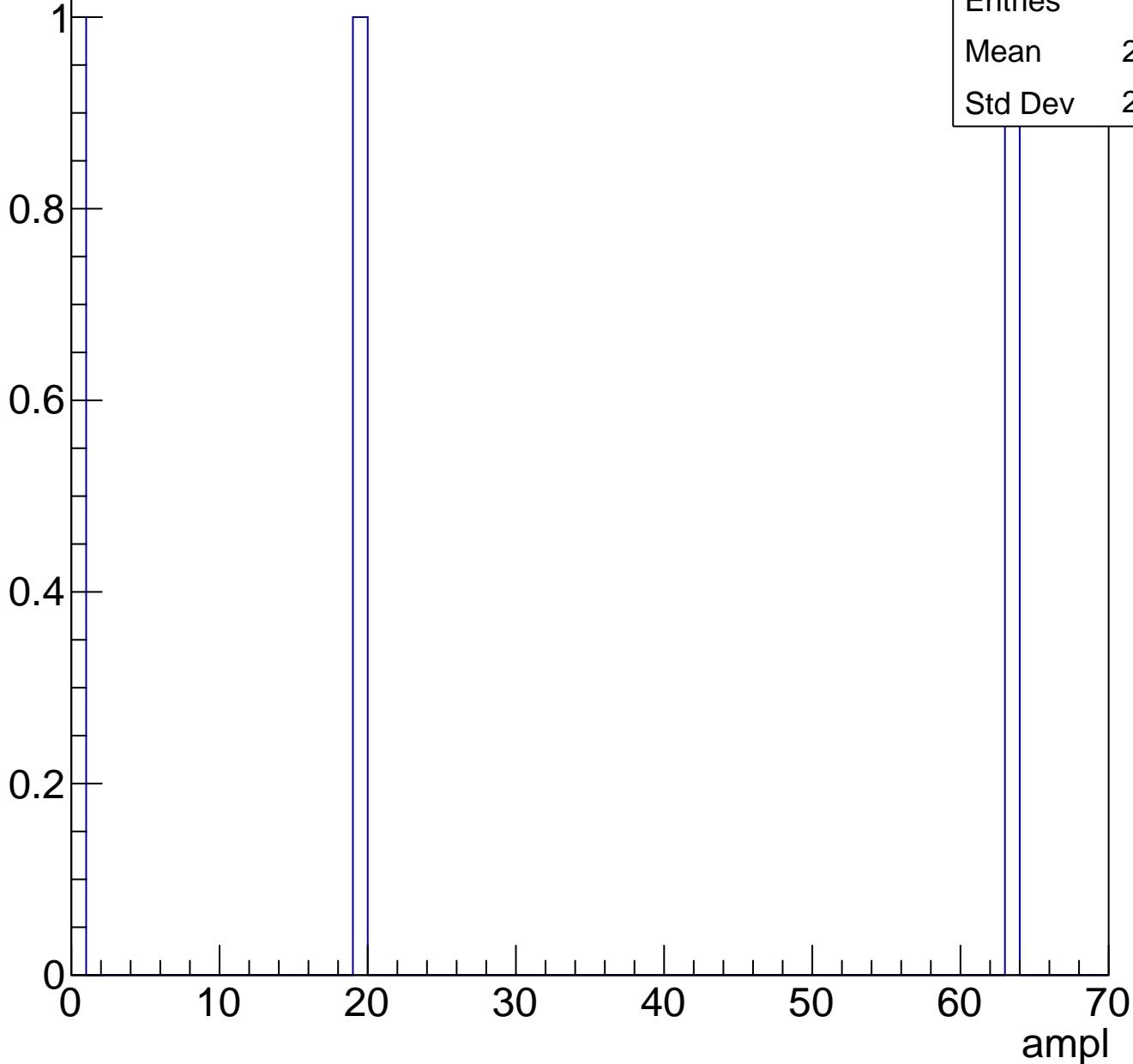
0 10 20 30 40 50 60 70



# B1L101S, U19-ch39, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U19-ch40, adc0

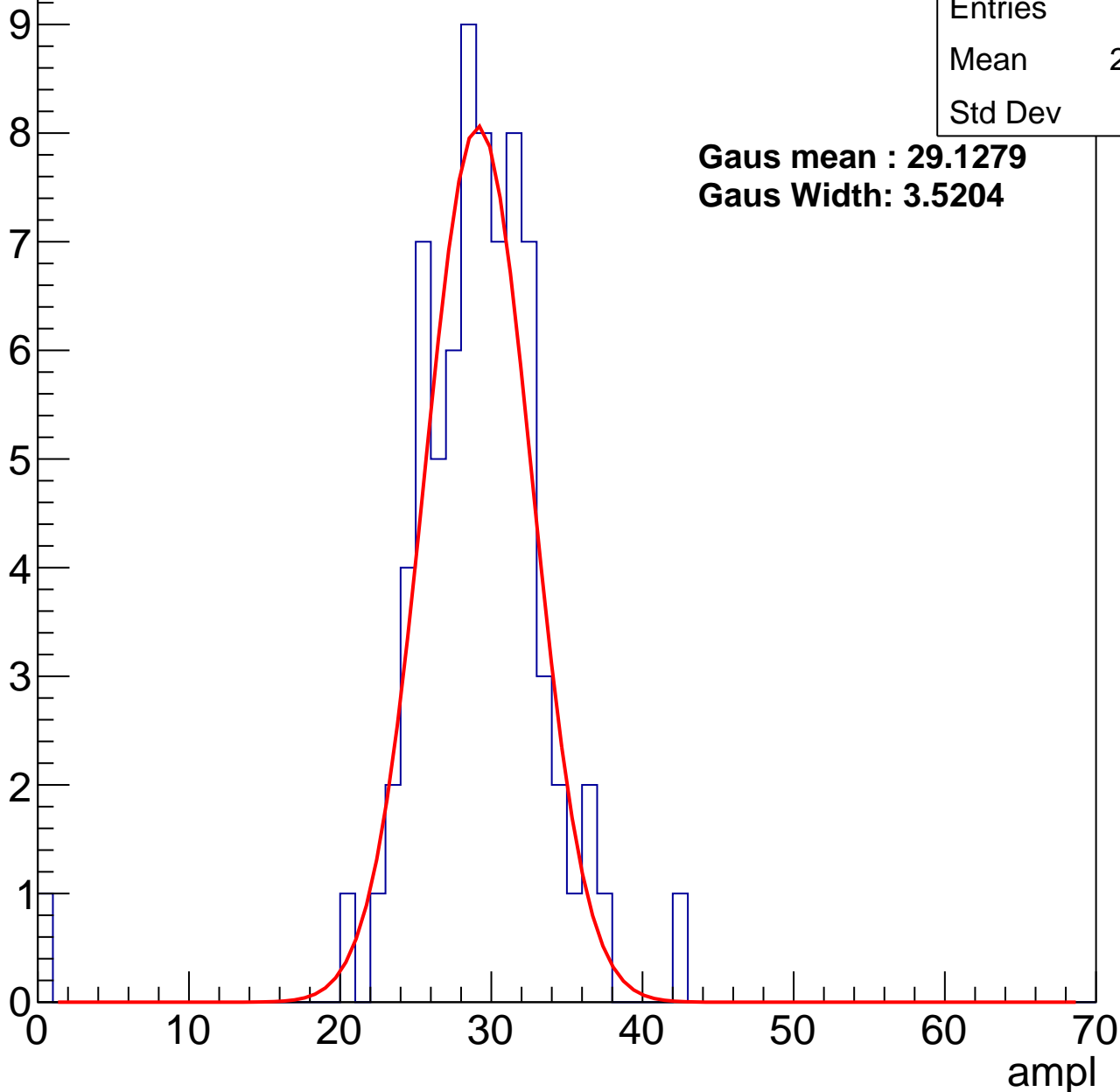
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	76
Mean	28.55
Std Dev	4.98

**Gaus mean : 29.1279**

**Gaus Width: 3.5204**



# B1L101S, U19-ch40, adc1

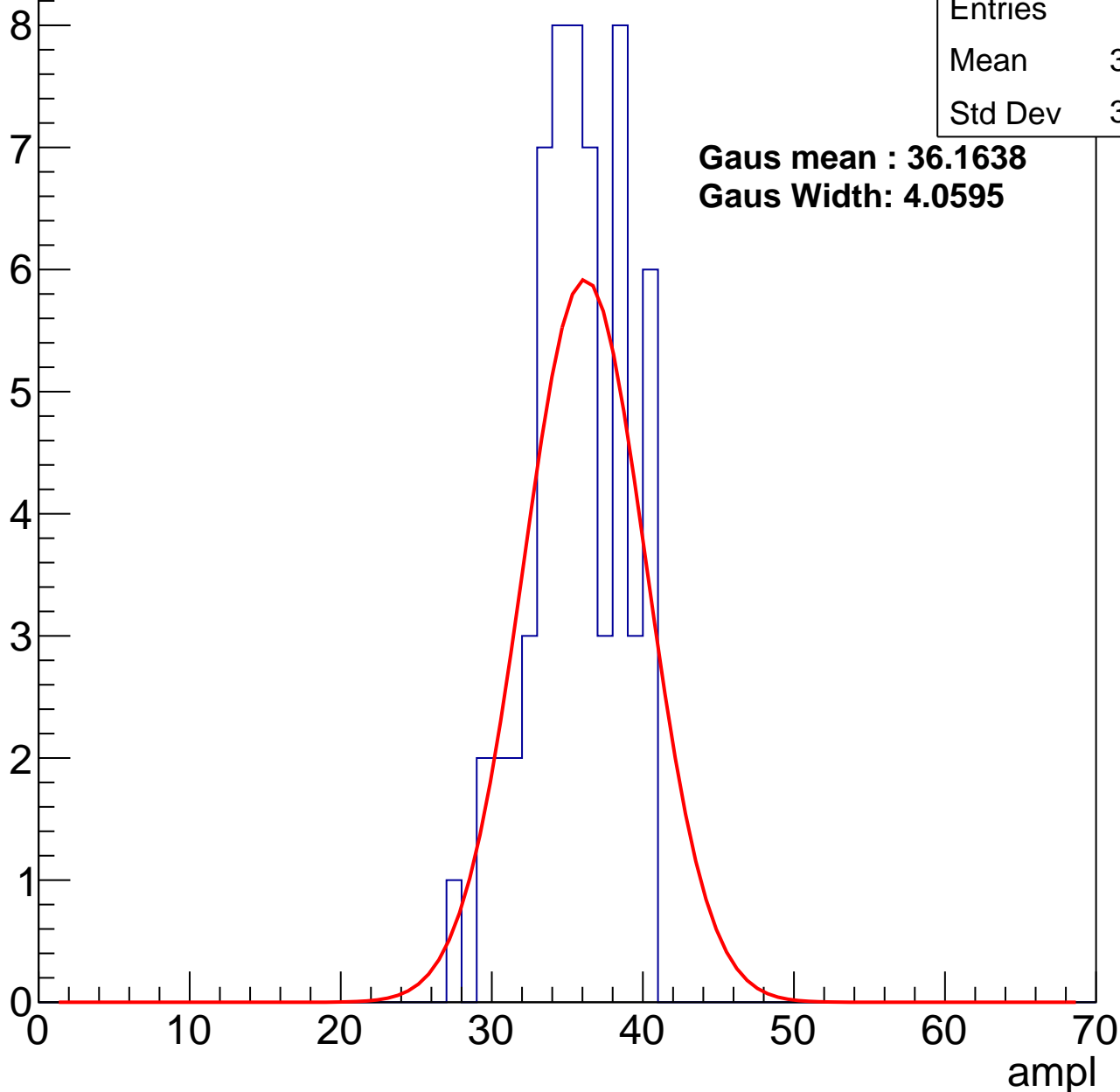
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	60
Mean	35.17
Std Dev	3.078

**Gaus mean : 36.1638**

**Gaus Width: 4.0595**



# B1L101S, U19-ch40, adc2

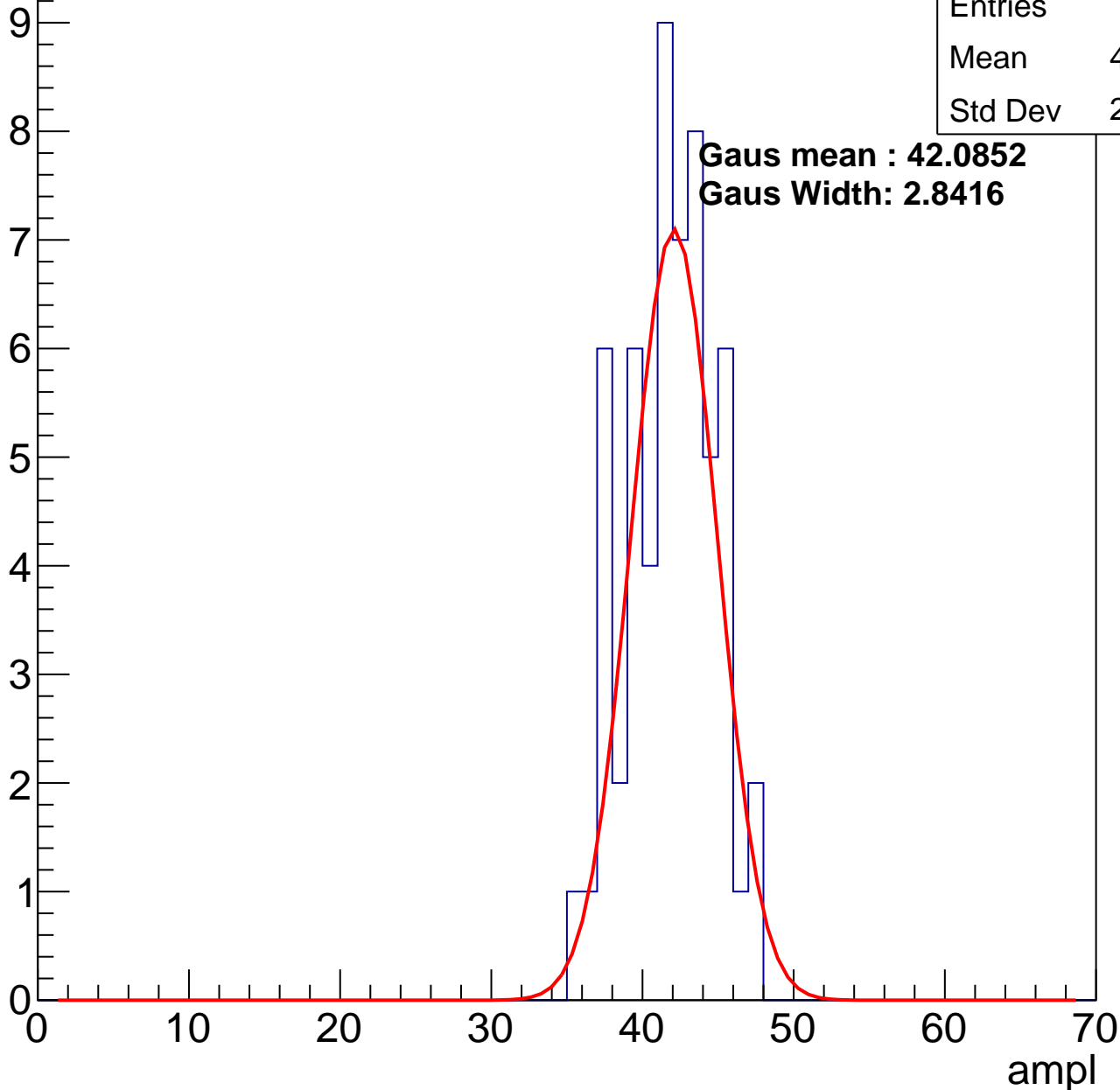
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	58
Mean	41.38
Std Dev	2.852

**Gaus mean : 42.0852**

**Gaus Width: 2.8416**

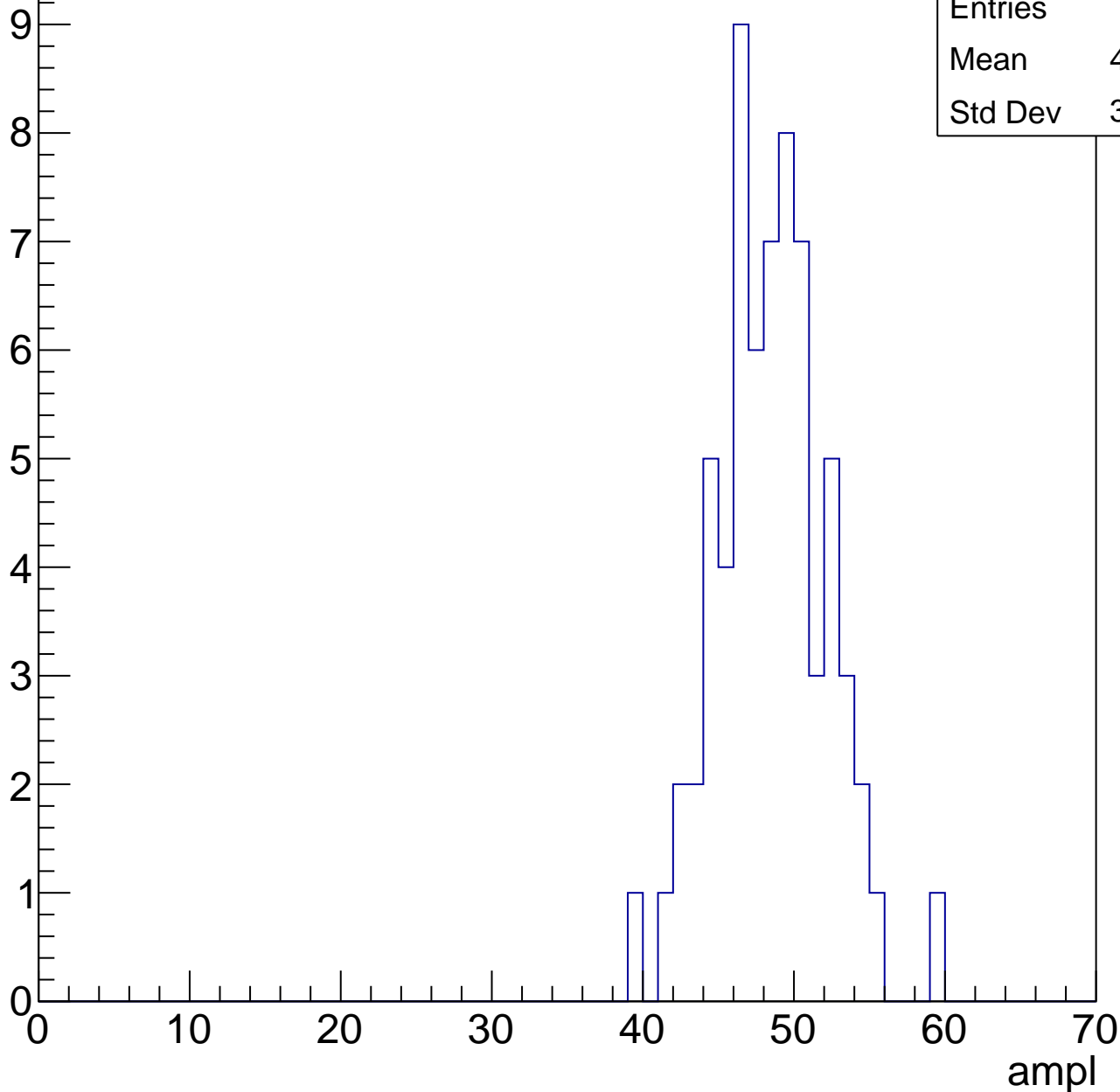


# B1L101S, U19-ch40, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	67
Mean	48.03
Std Dev	3.603

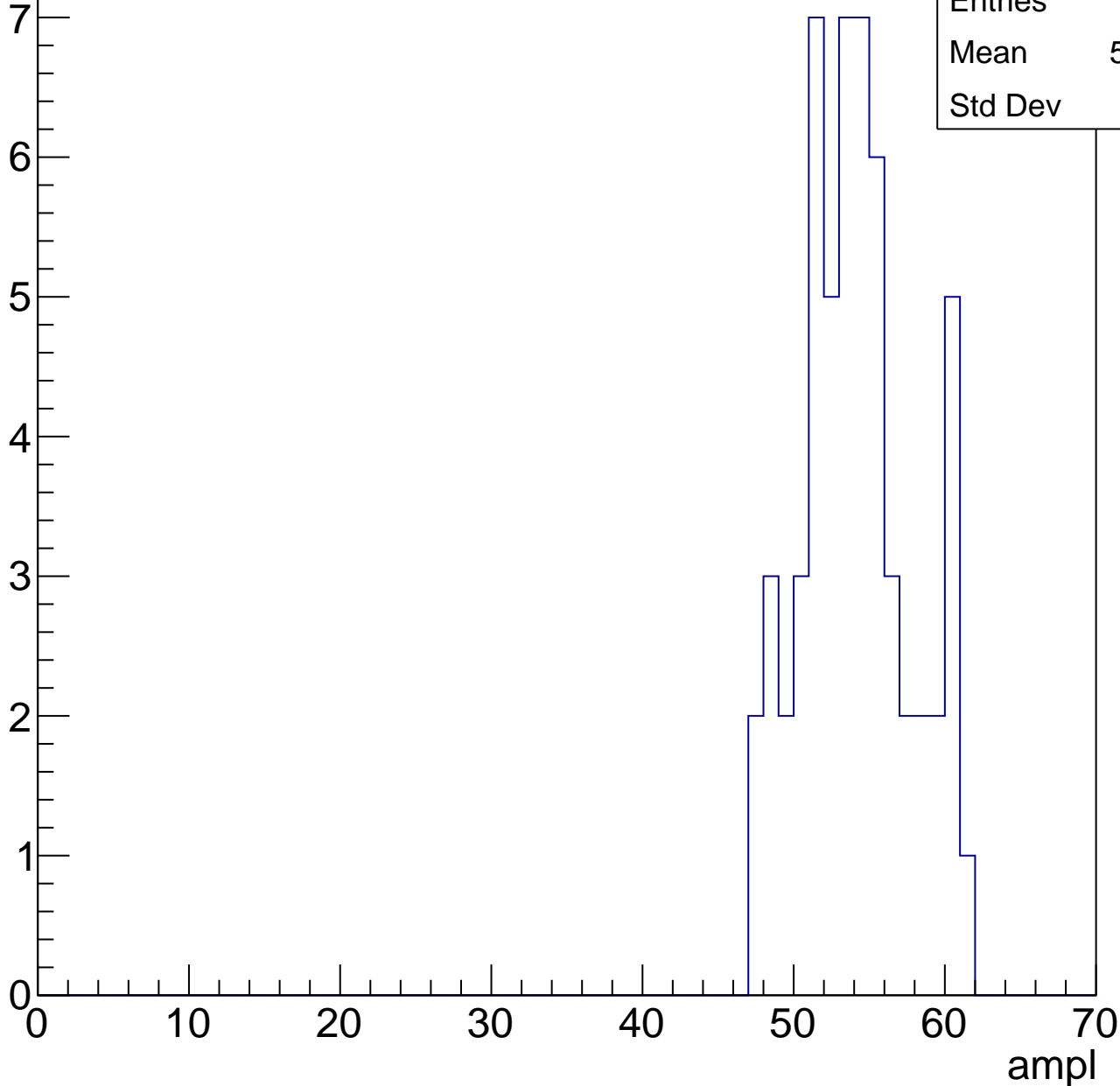


# B1L101S, U19-ch40, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

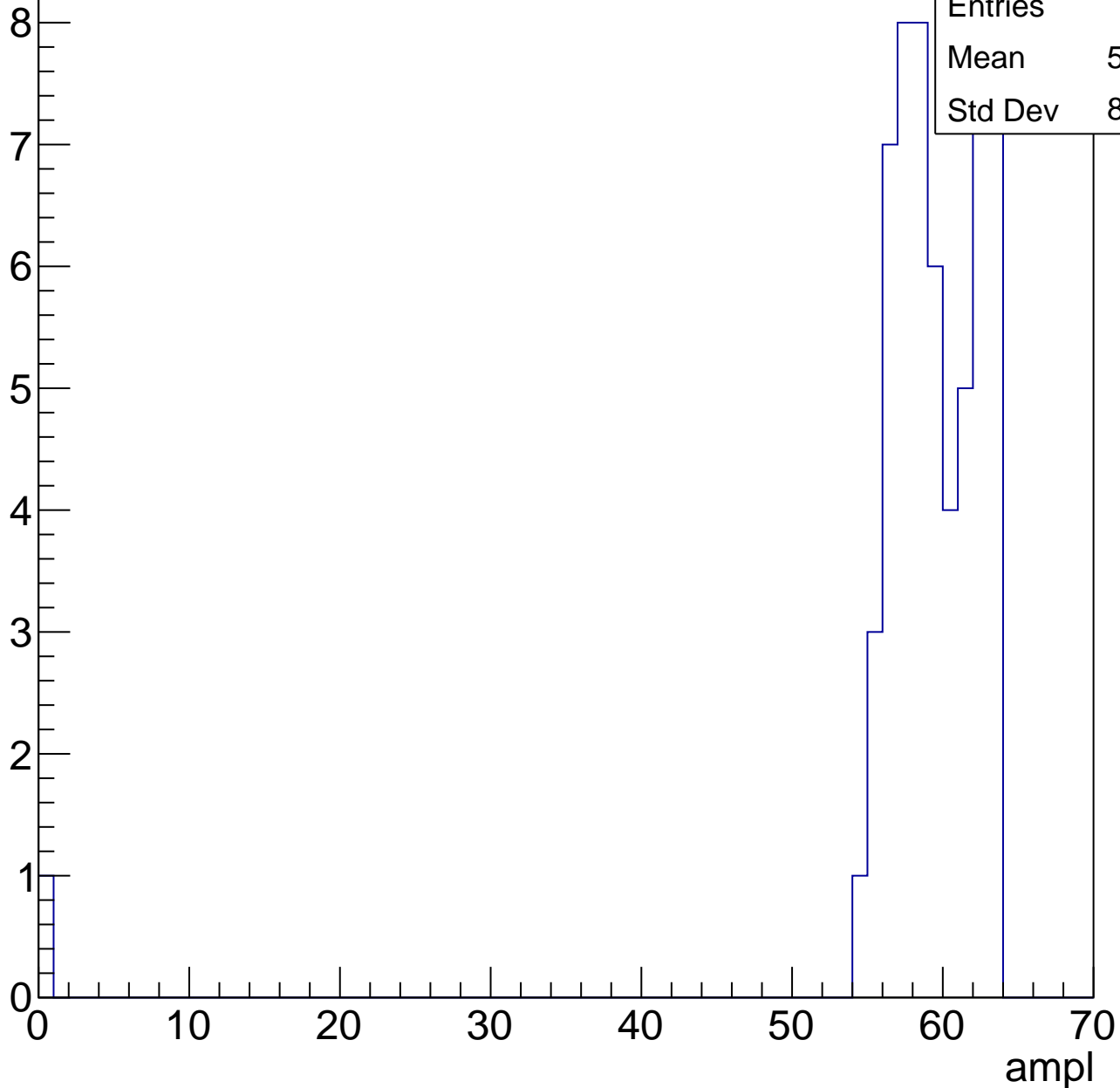
Entries	57
Mean	53.67
Std Dev	3.59



# B1L101S, U19-ch40, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

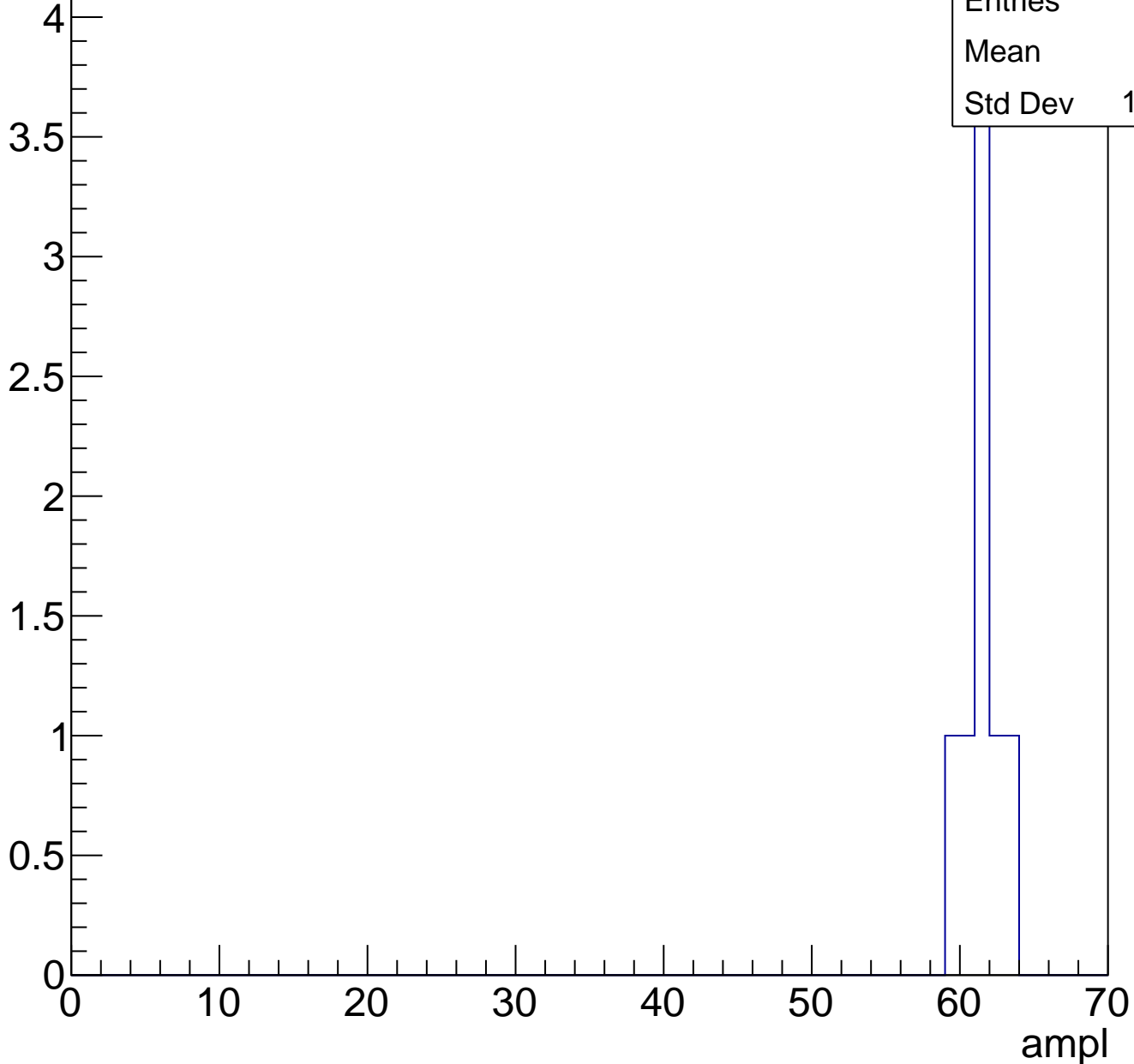
Entry



# B1L101S, U19-ch40, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U19-ch40, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	4
Mean	31.25
Std Dev	31.25

# B1L101S, U19-ch41, adc0

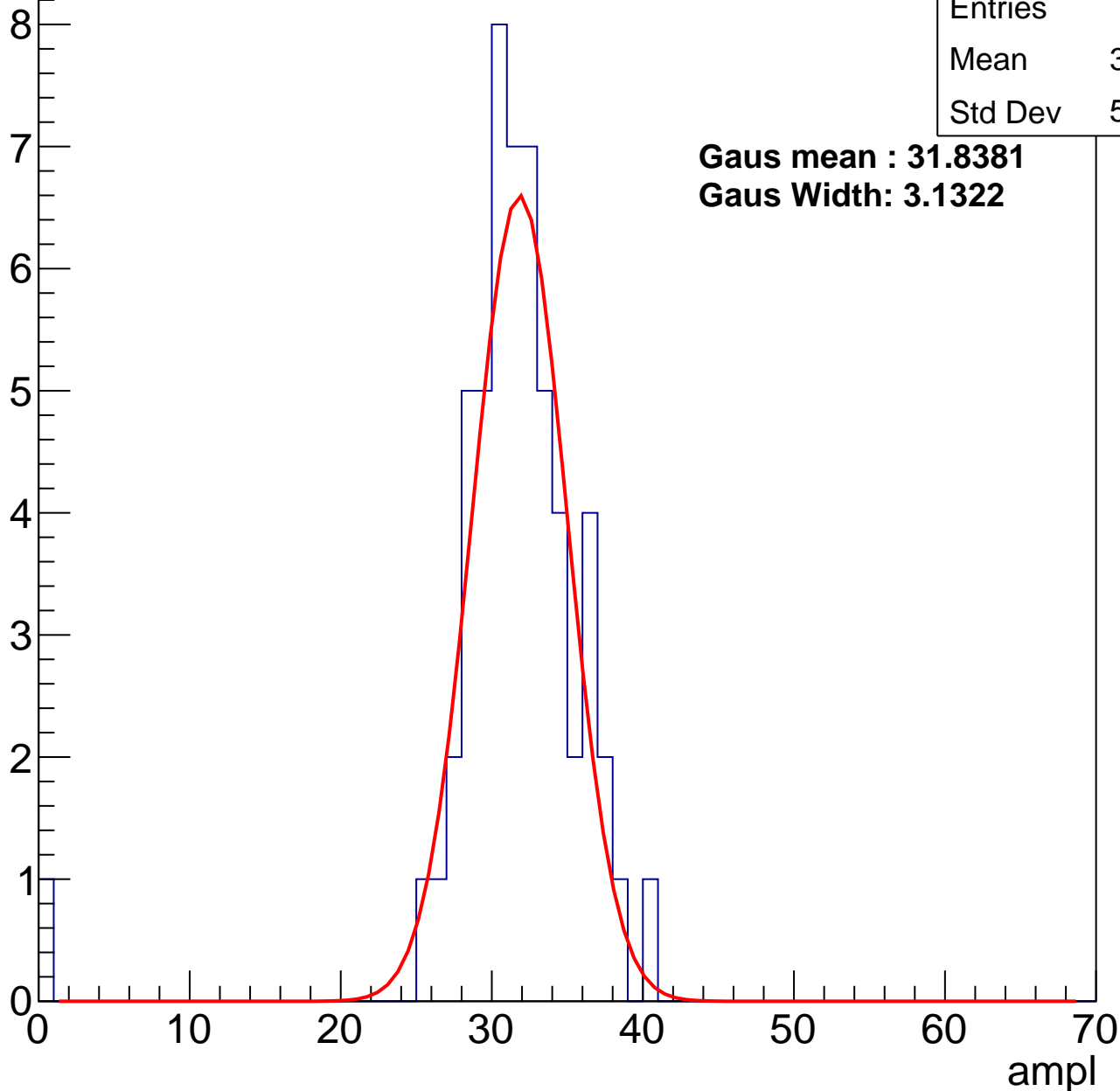
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	56
Mean	31.04
Std Dev	5.217

**Gaus mean : 31.8381**

**Gaus Width: 3.1322**



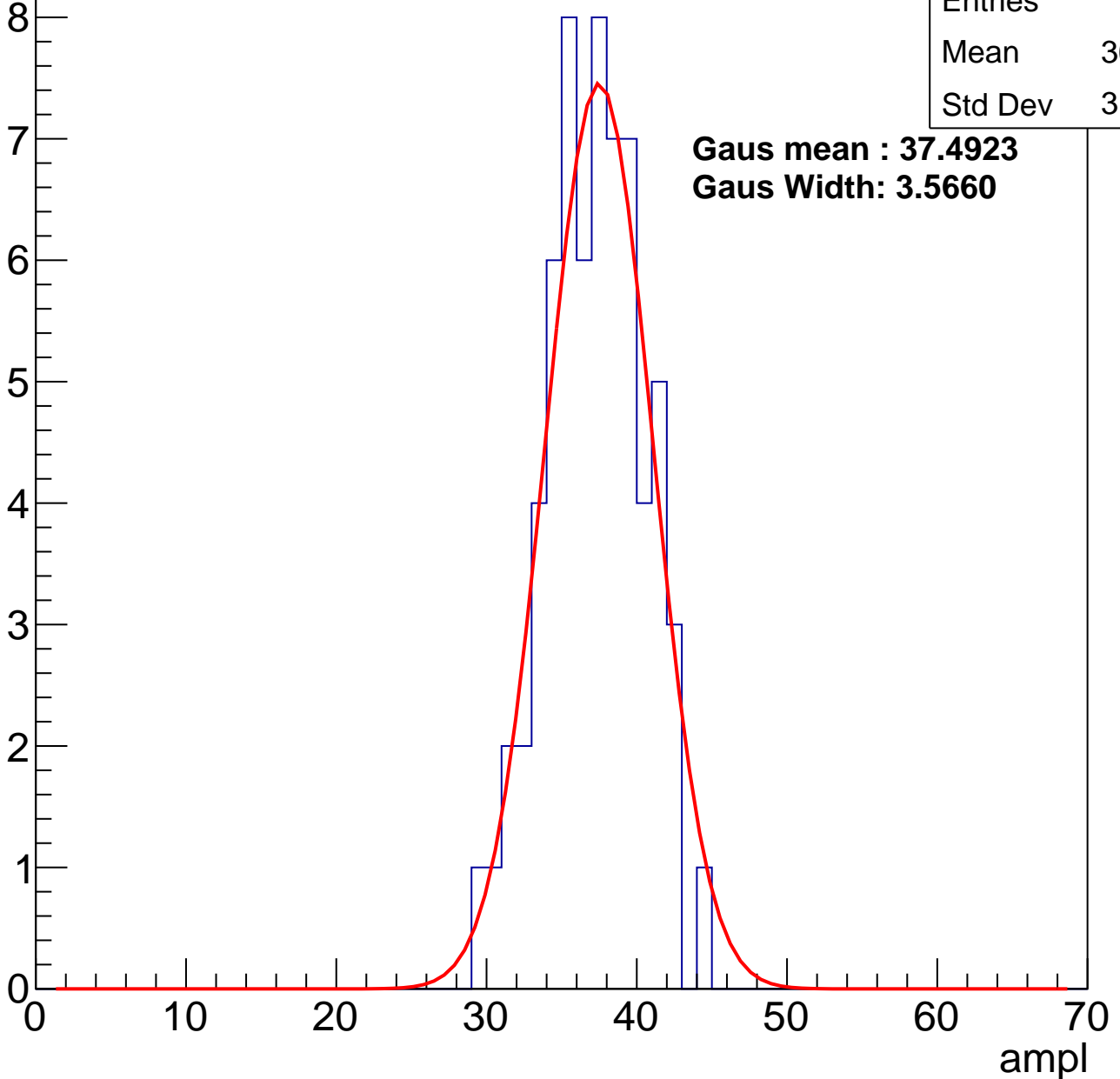
# B1L101S, U19-ch41, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

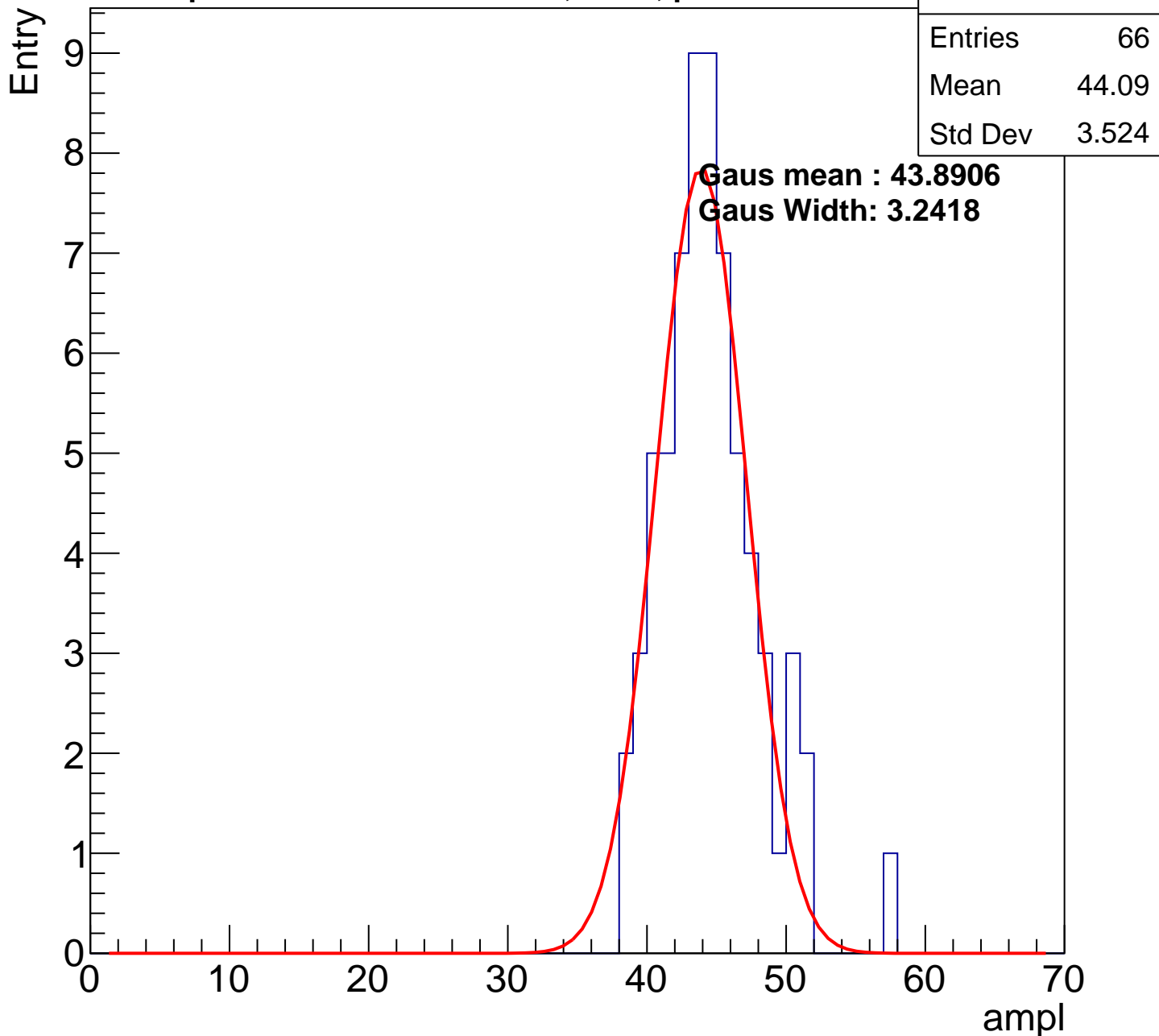
Entries	65
Mean	36.72
Std Dev	3.189

**Gaus mean : 37.4923**  
**Gaus Width: 3.5660**



# B1L101S, U19-ch41, adc2

calib\_packv5\_042523\_0143.root, FC#0, port D2

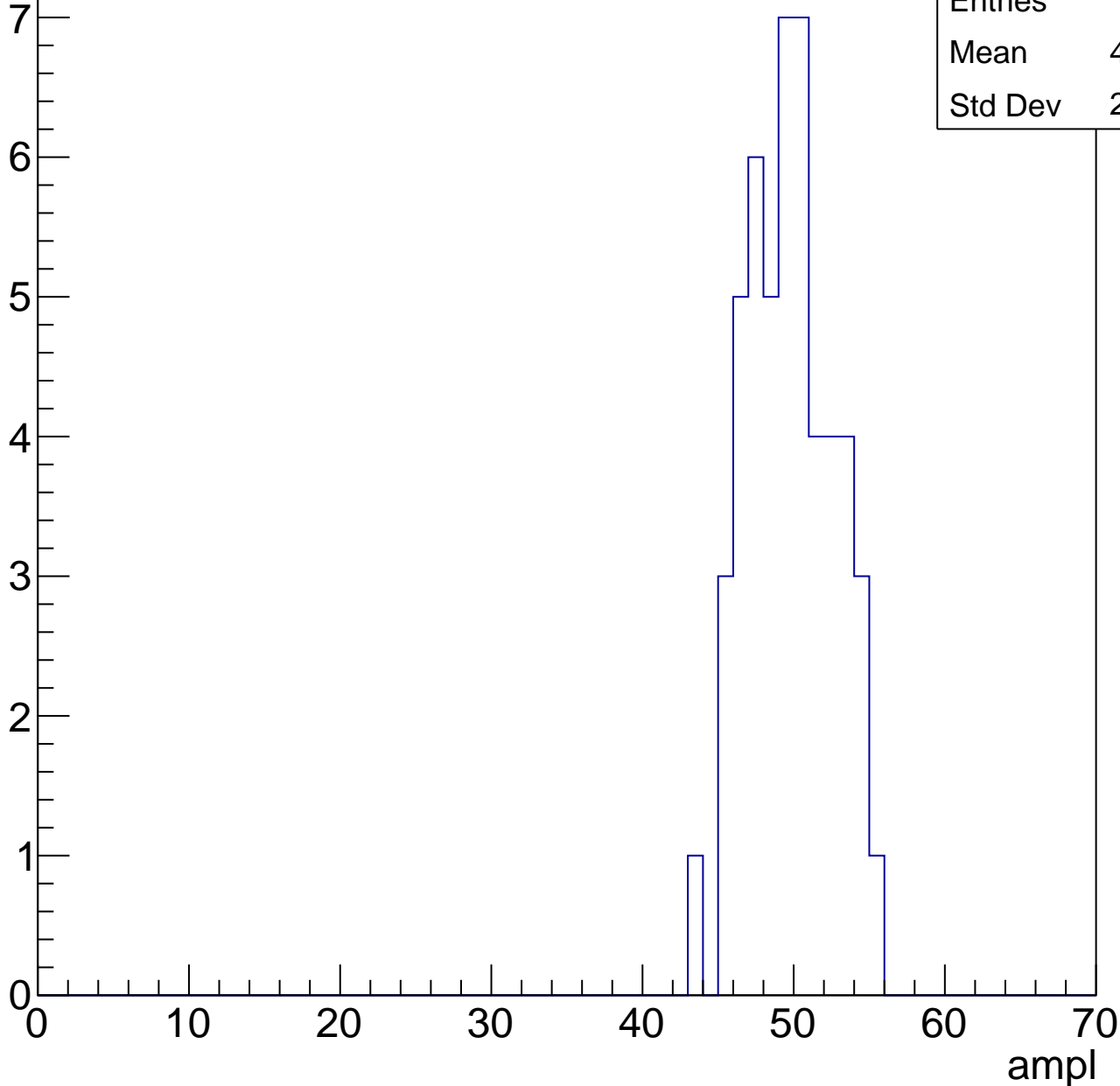


# B1L101S, U19-ch41, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	50
Mean	49.28
Std Dev	2.786

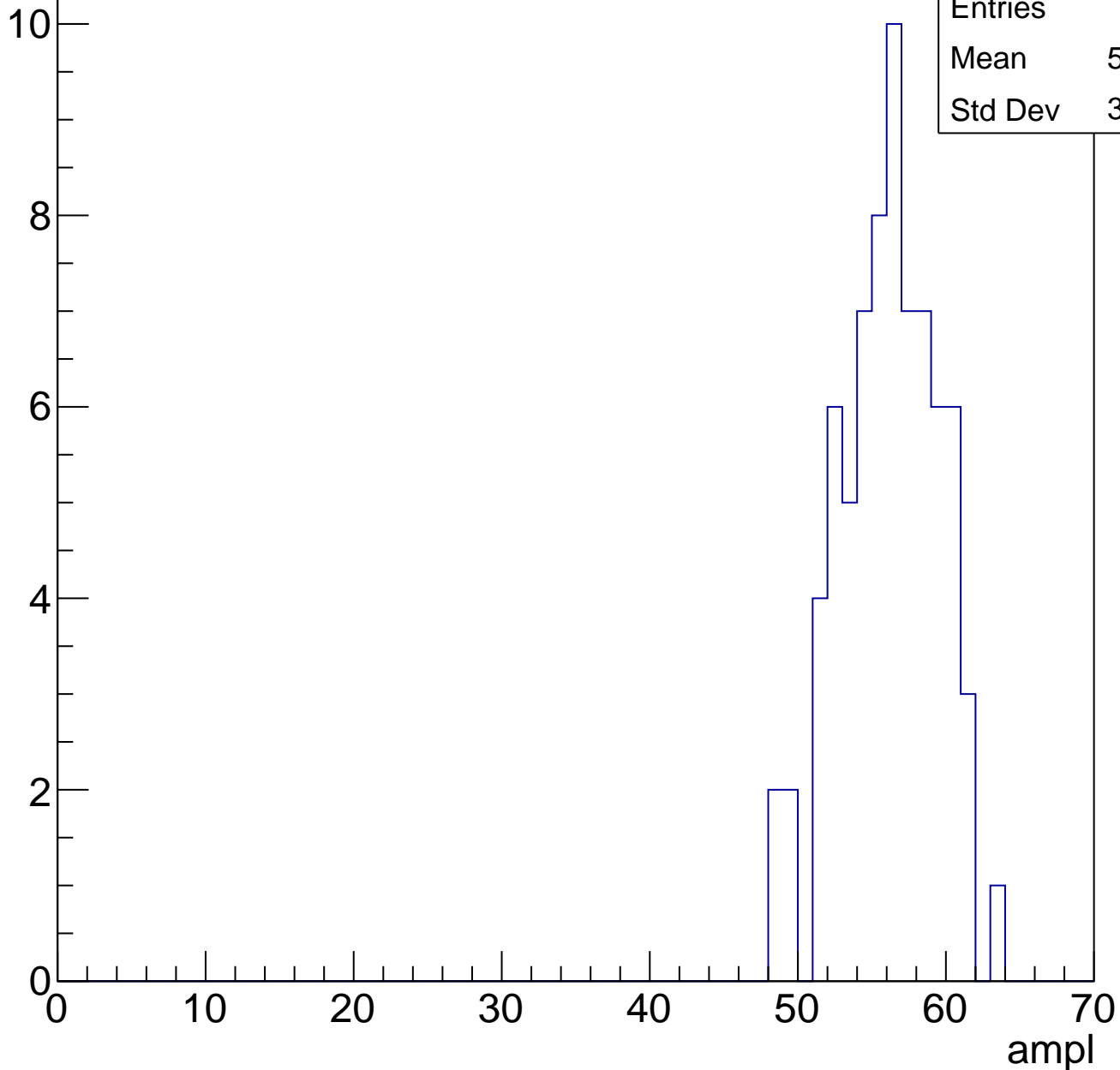


# B1L101S, U19-ch41, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	74
Mean	55.65
Std Dev	3.294

Entry

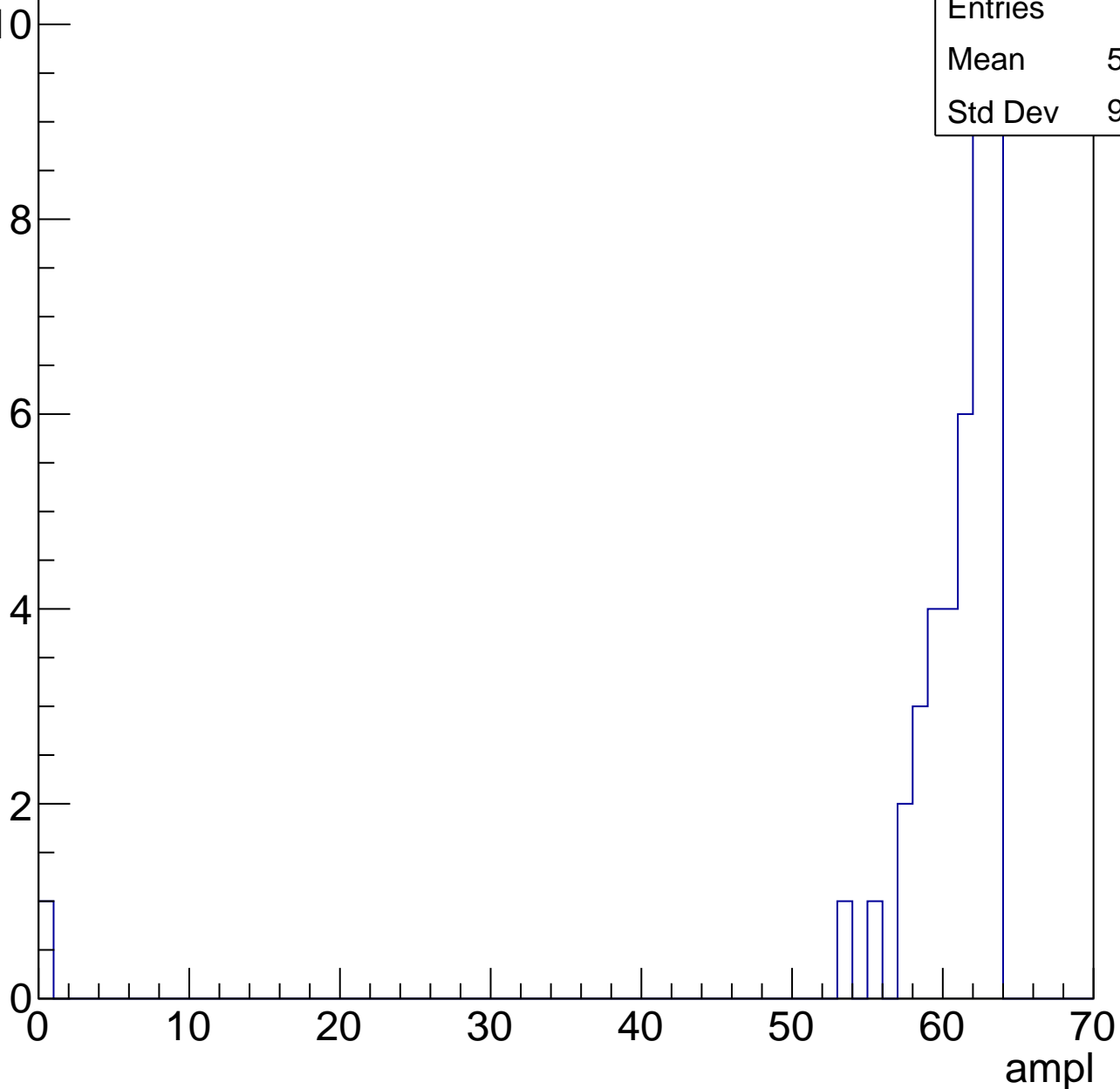


# B1L101S, U19-ch41, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	41
Mean	59.15
Std Dev	9.634



# B1L101S, U19-ch41, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U19-ch41, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U19-ch42, adc0

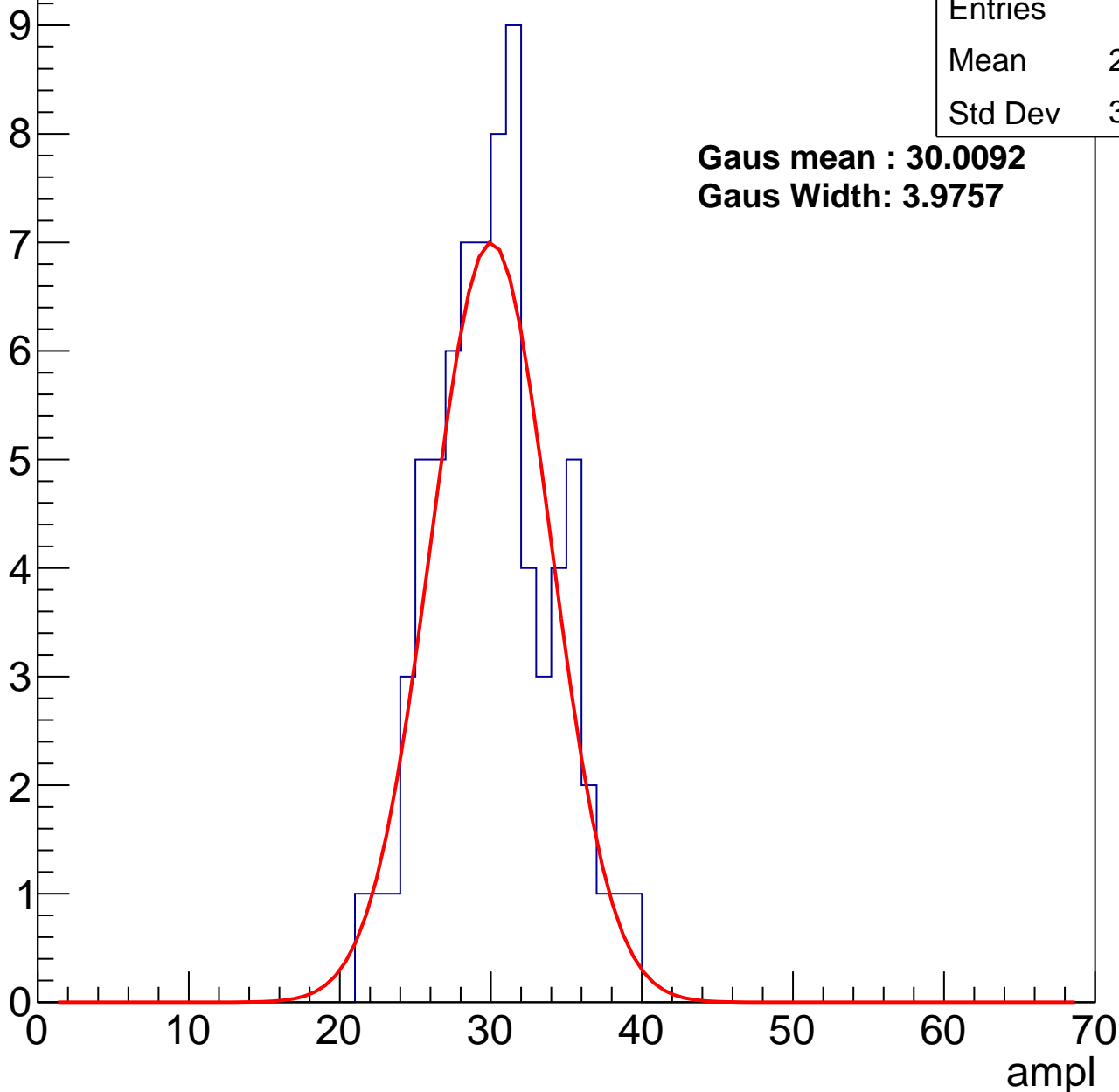
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	74
Mean	29.69
Std Dev	3.848

**Gaus mean : 30.0092**

**Gaus Width: 3.9757**



# B1L101S, U19-ch42, adc1

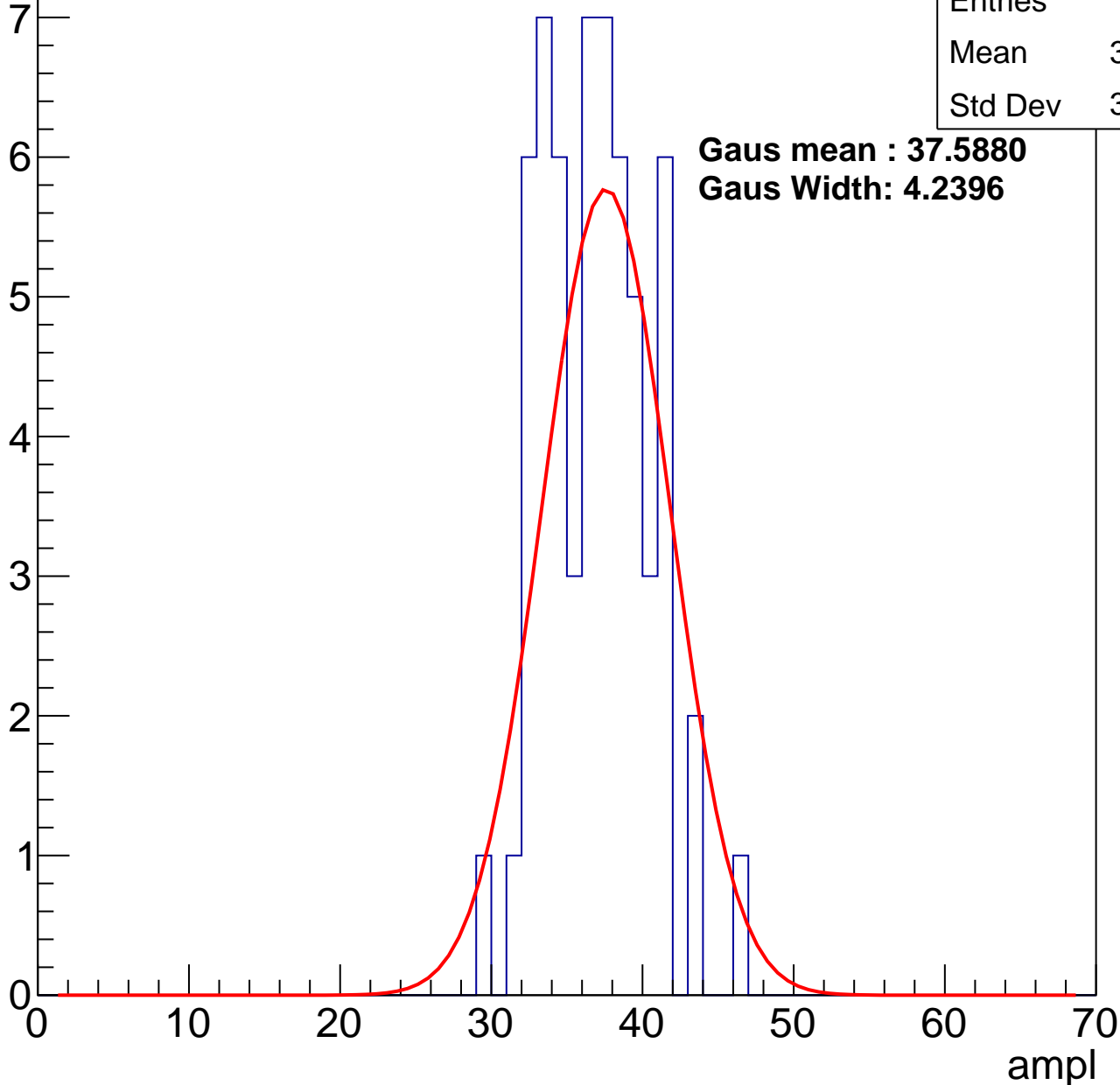
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	36.46
Std Dev	3.434

**Gaus mean : 37.5880**

**Gaus Width: 4.2396**



# B1L101S, U19-ch42, adc2

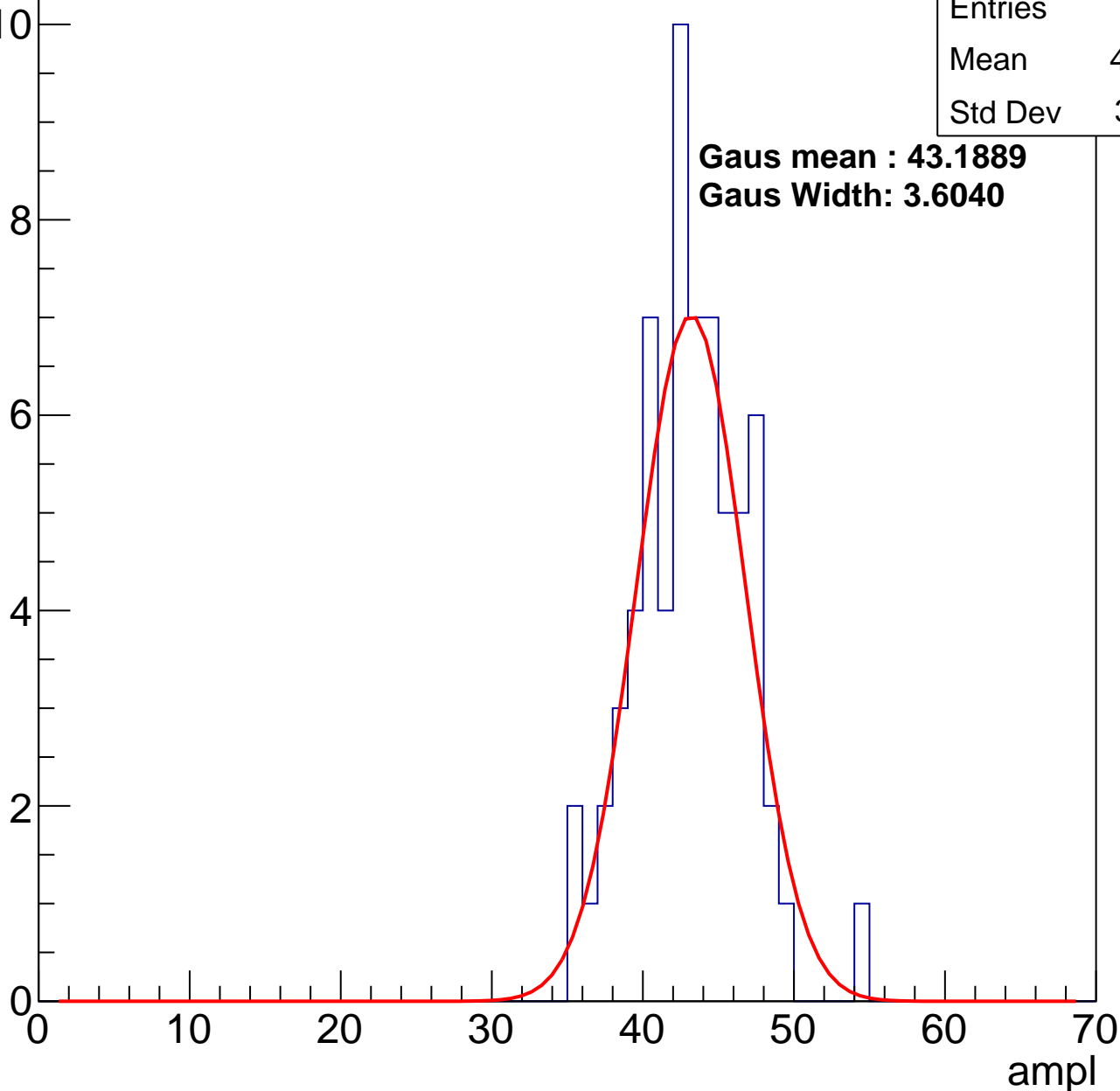
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	67
Mean	42.67
Std Dev	3.551

**Gaus mean : 43.1889**

**Gaus Width: 3.6040**

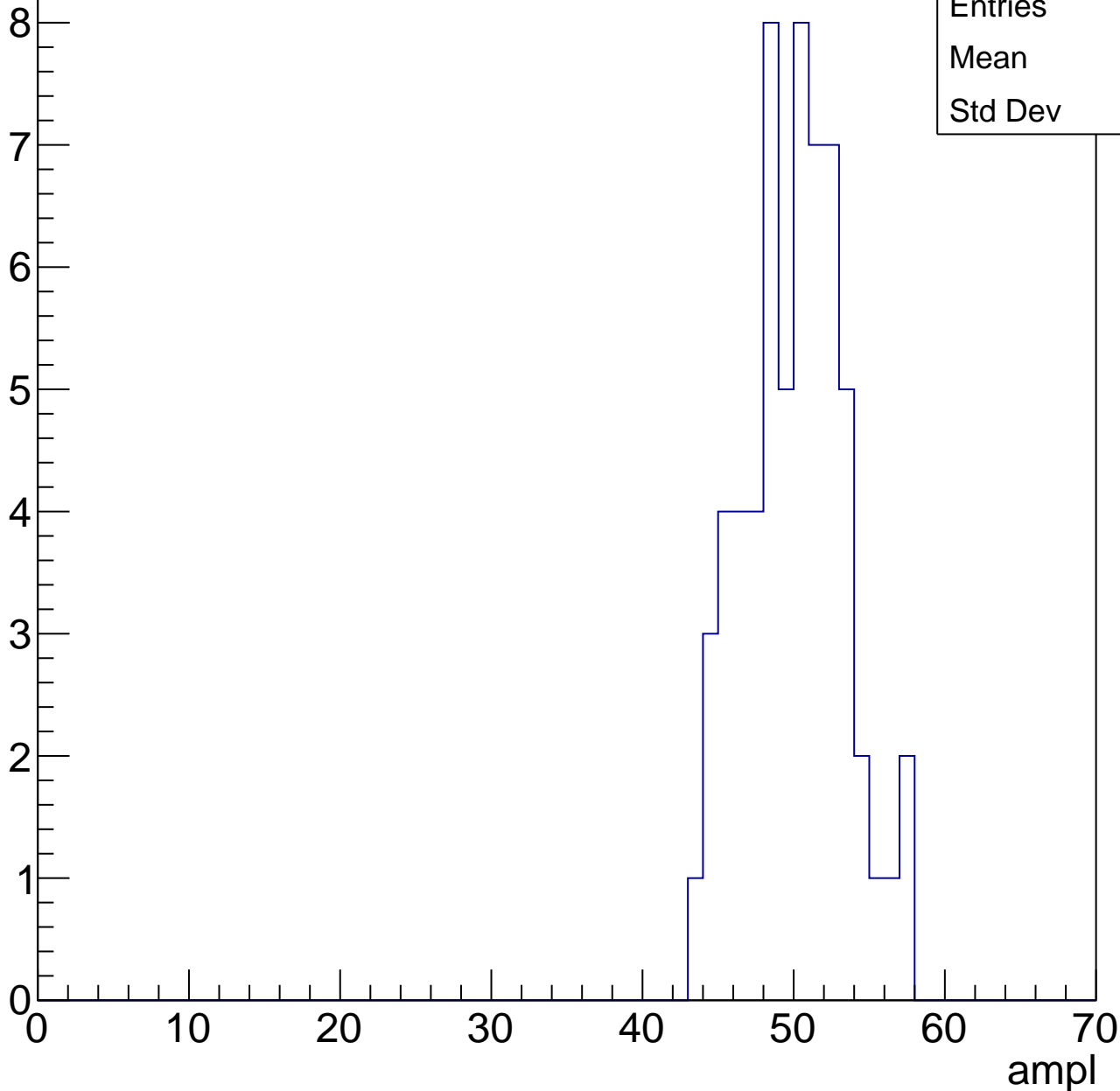


# B1L101S, U19-ch42, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	49.6
Std Dev	3.25

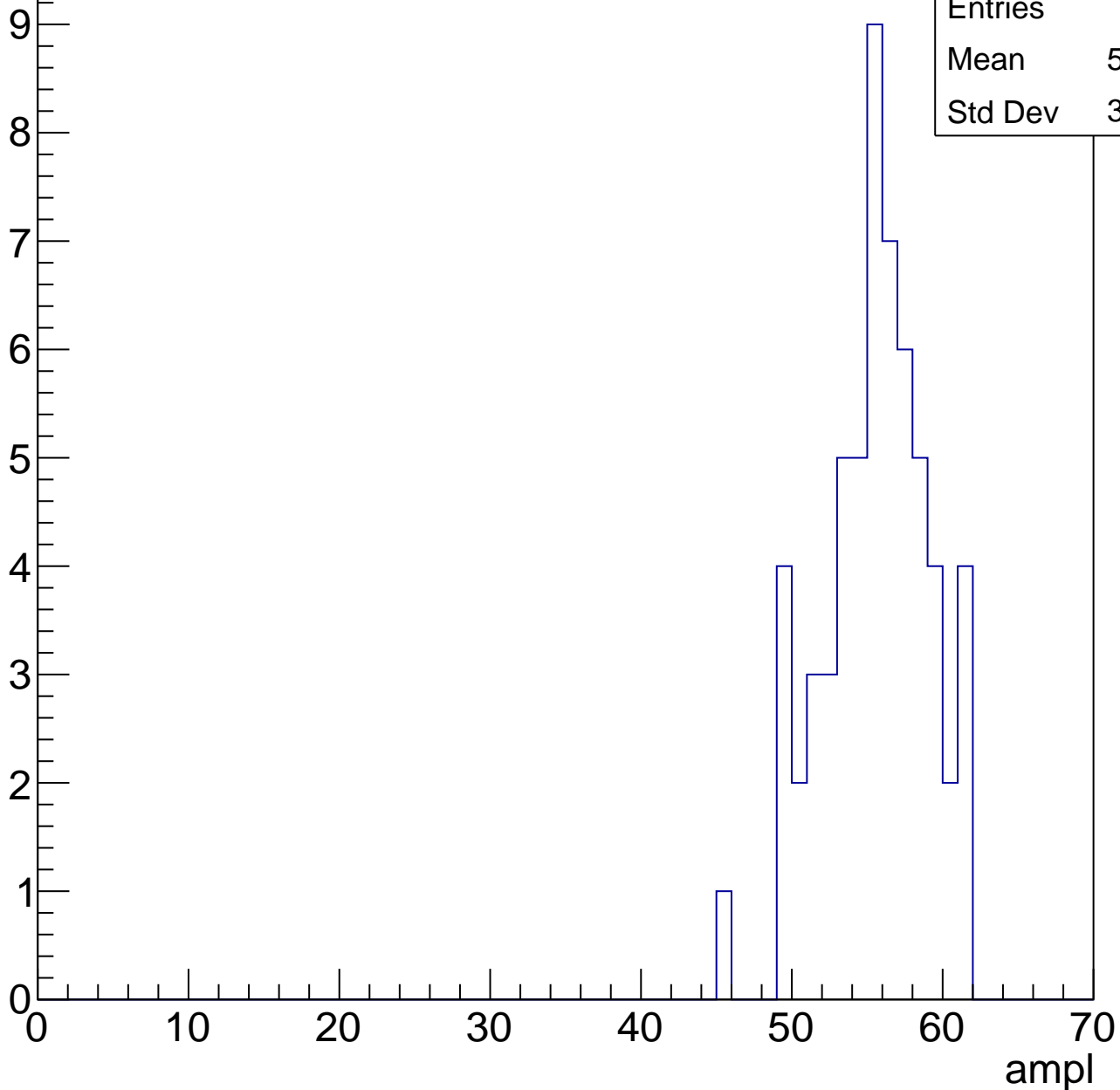


# B1L101S, U19-ch42, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	60
Mean	55.07
Std Dev	3.483

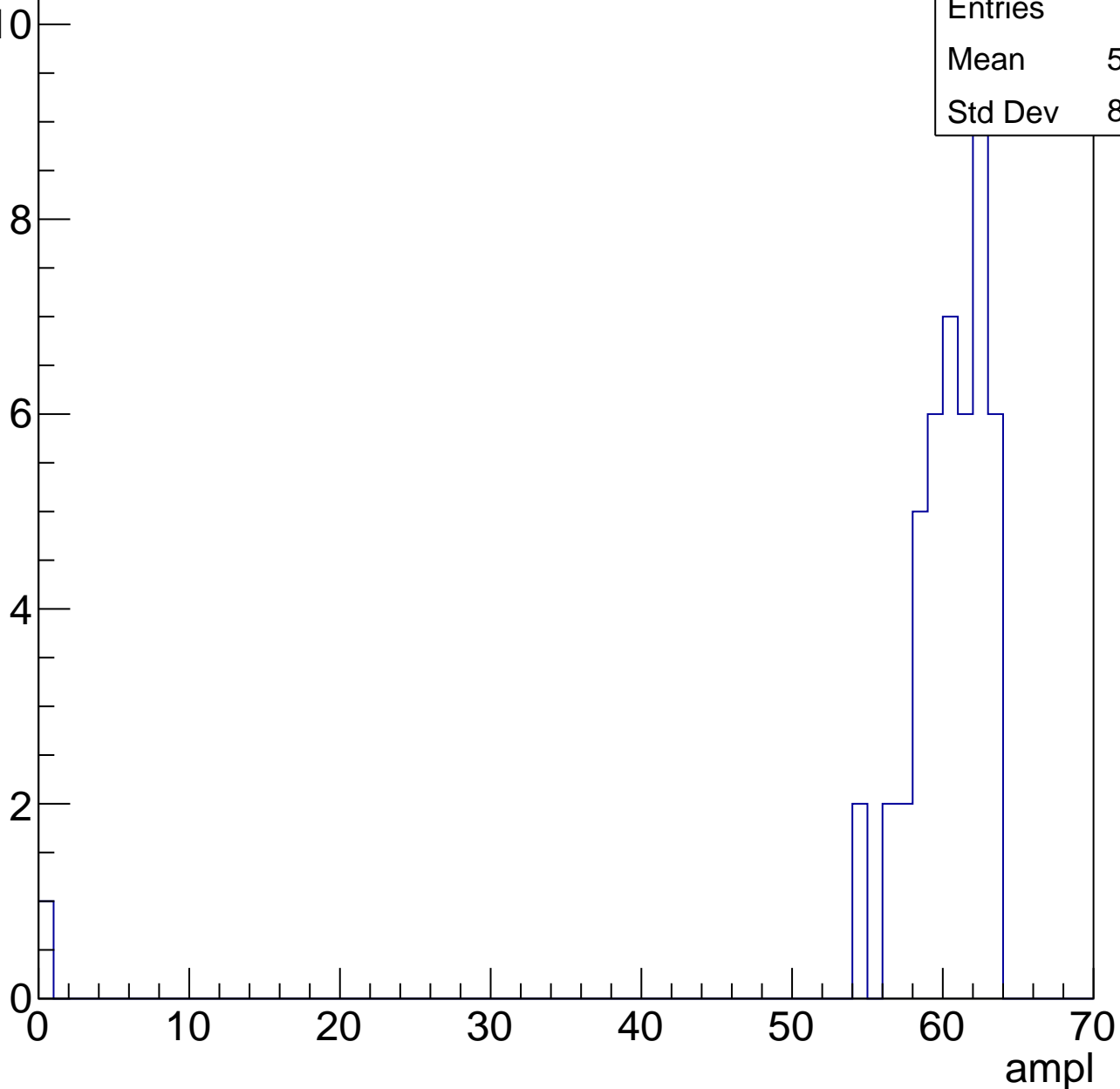


# B1L101S, U19-ch42, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

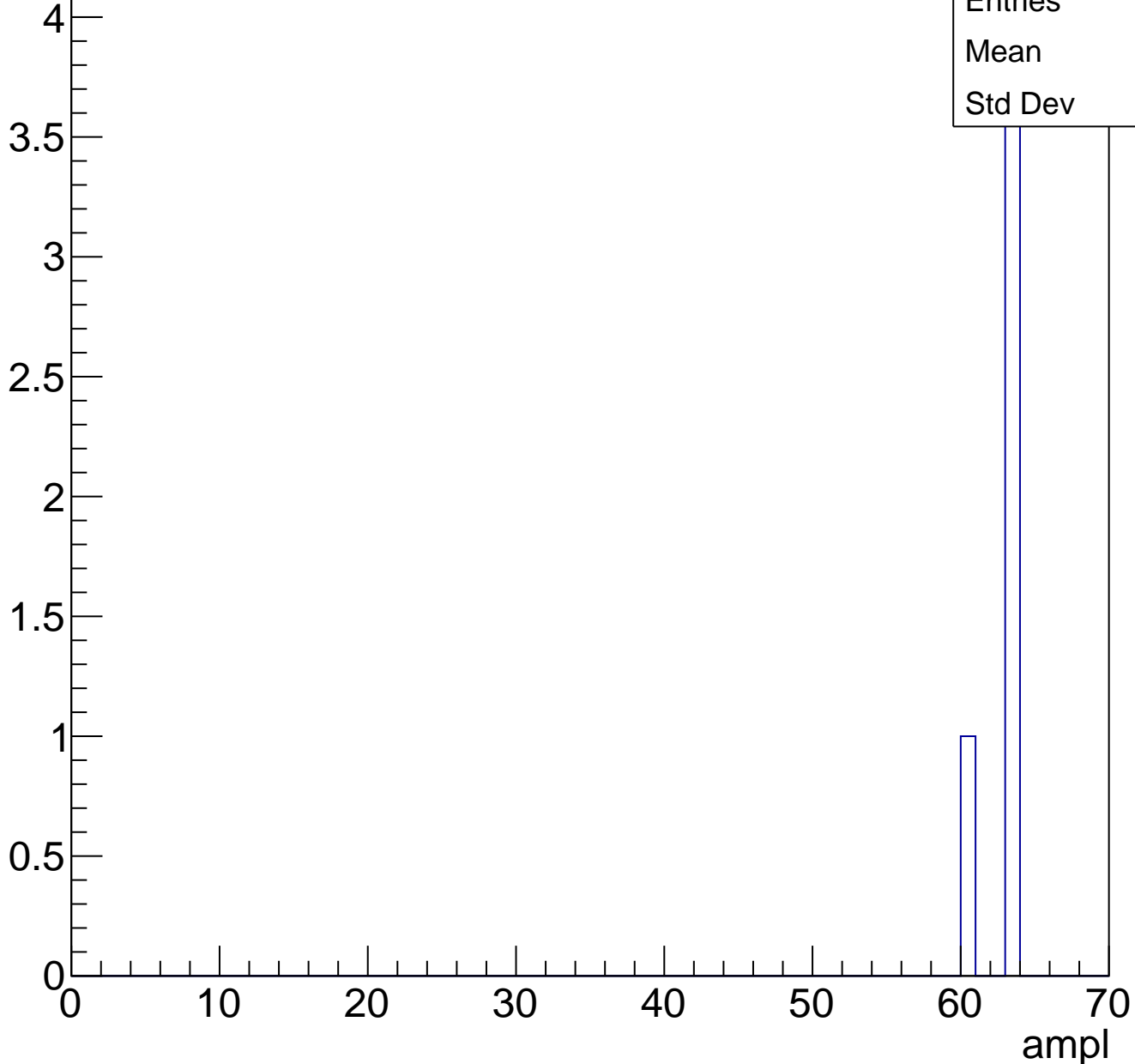
Entries	47
Mean	58.77
Std Dev	8.964



# B1L101S, U19-ch42, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U19-ch42, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U19-ch43, adc0

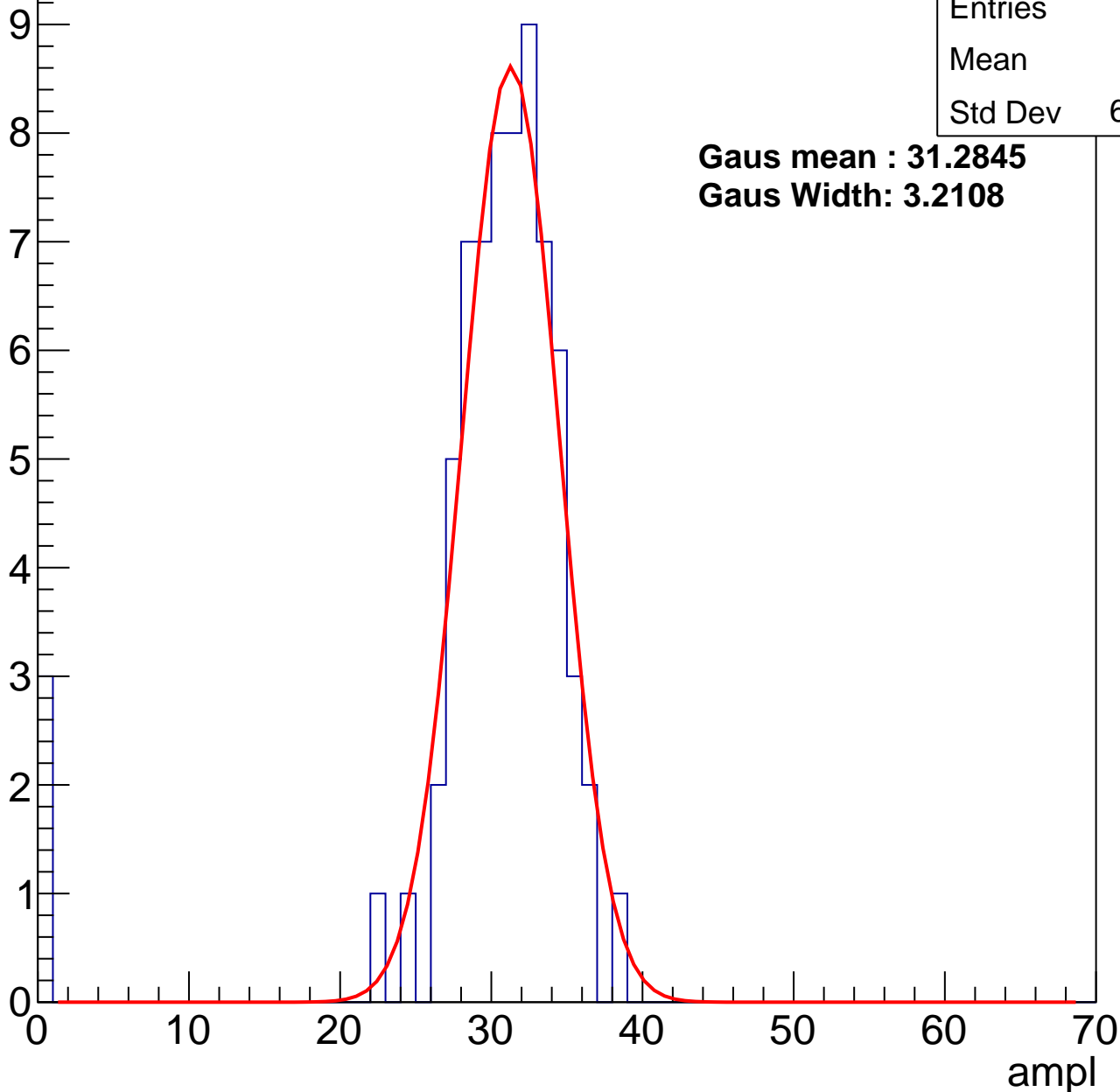
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	29.4
Std Dev	6.867

**Gaus mean : 31.2845**

**Gaus Width: 3.2108**



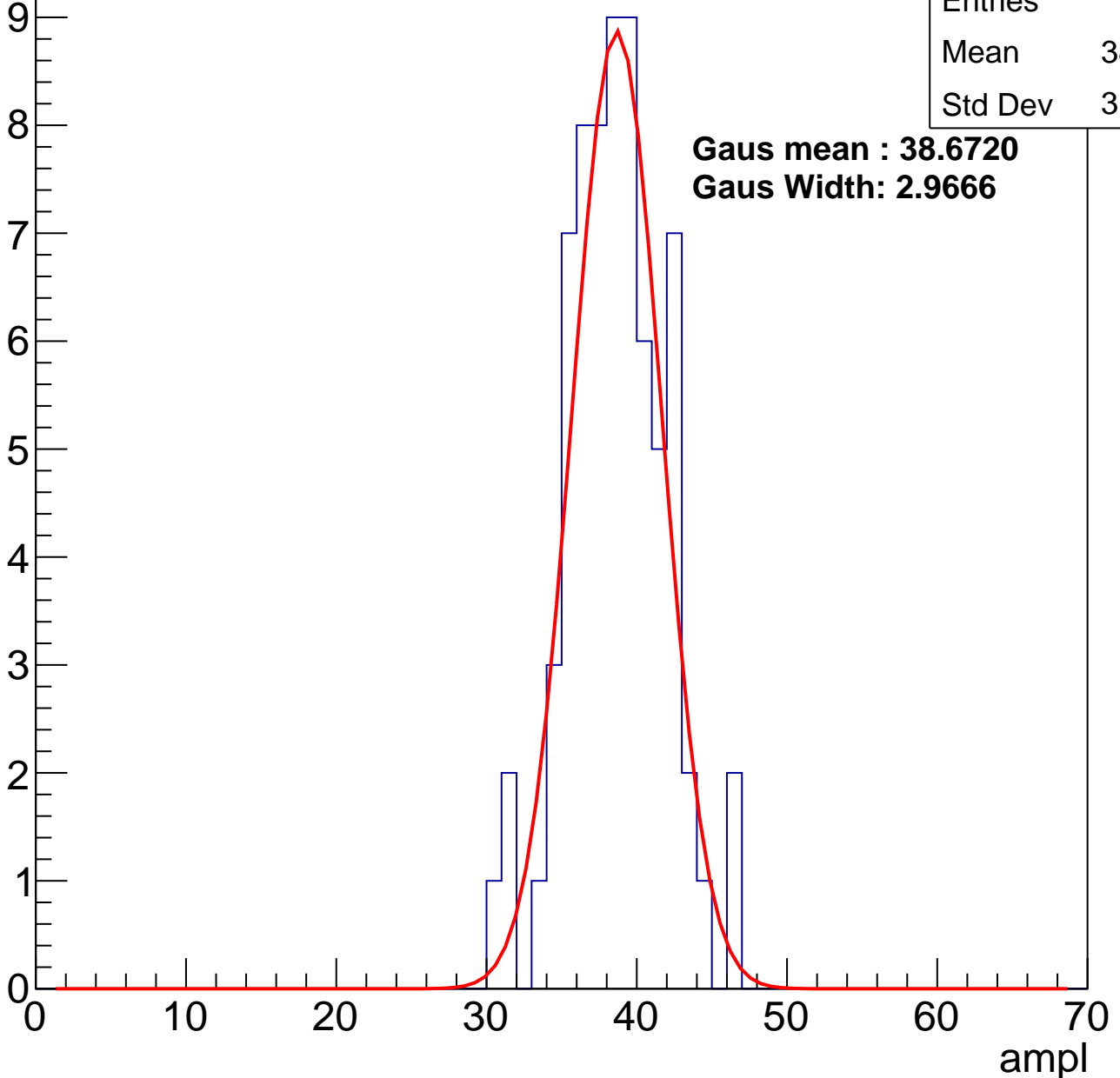
# B1L101S, U19-ch43, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	71
Mean	38.17
Std Dev	3.228

**Gaus mean : 38.6720**  
**Gaus Width: 2.9666**



# B1L101S, U19-ch43, adc2

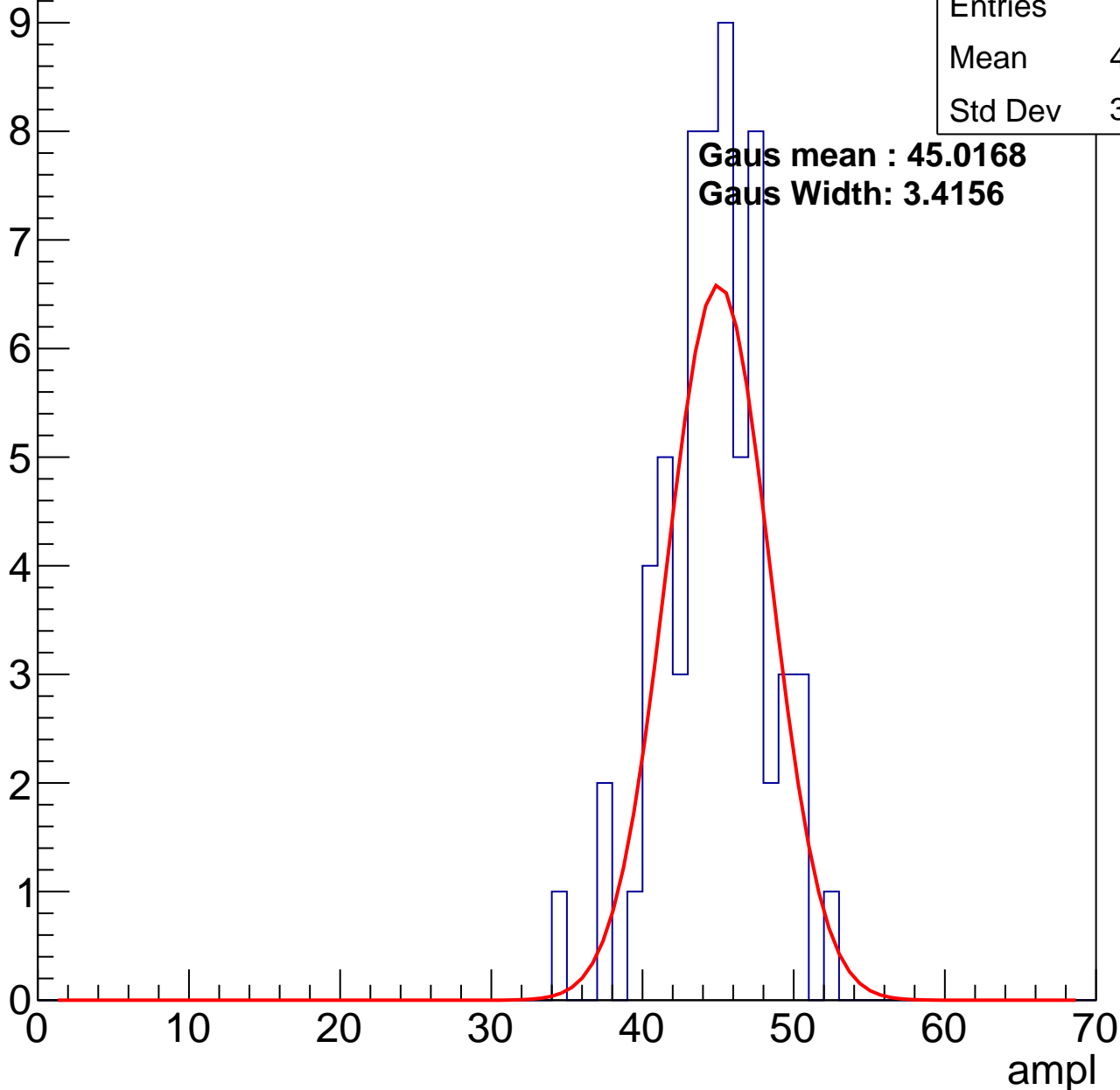
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	44.29
Std Dev	3.397

**Gaus mean : 45.0168**

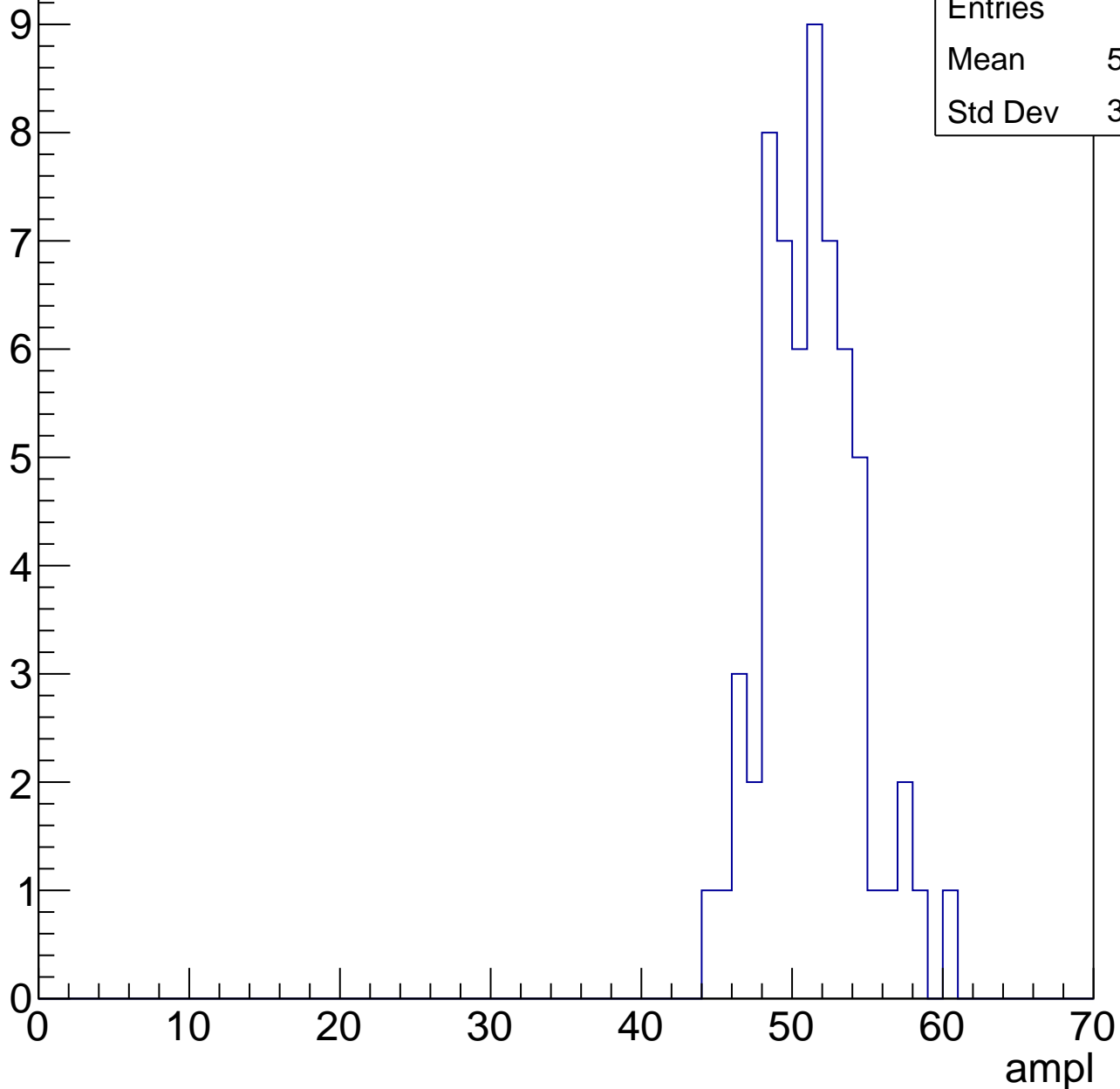
**Gaus Width: 3.4156**



# B1L101S, U19-ch43, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

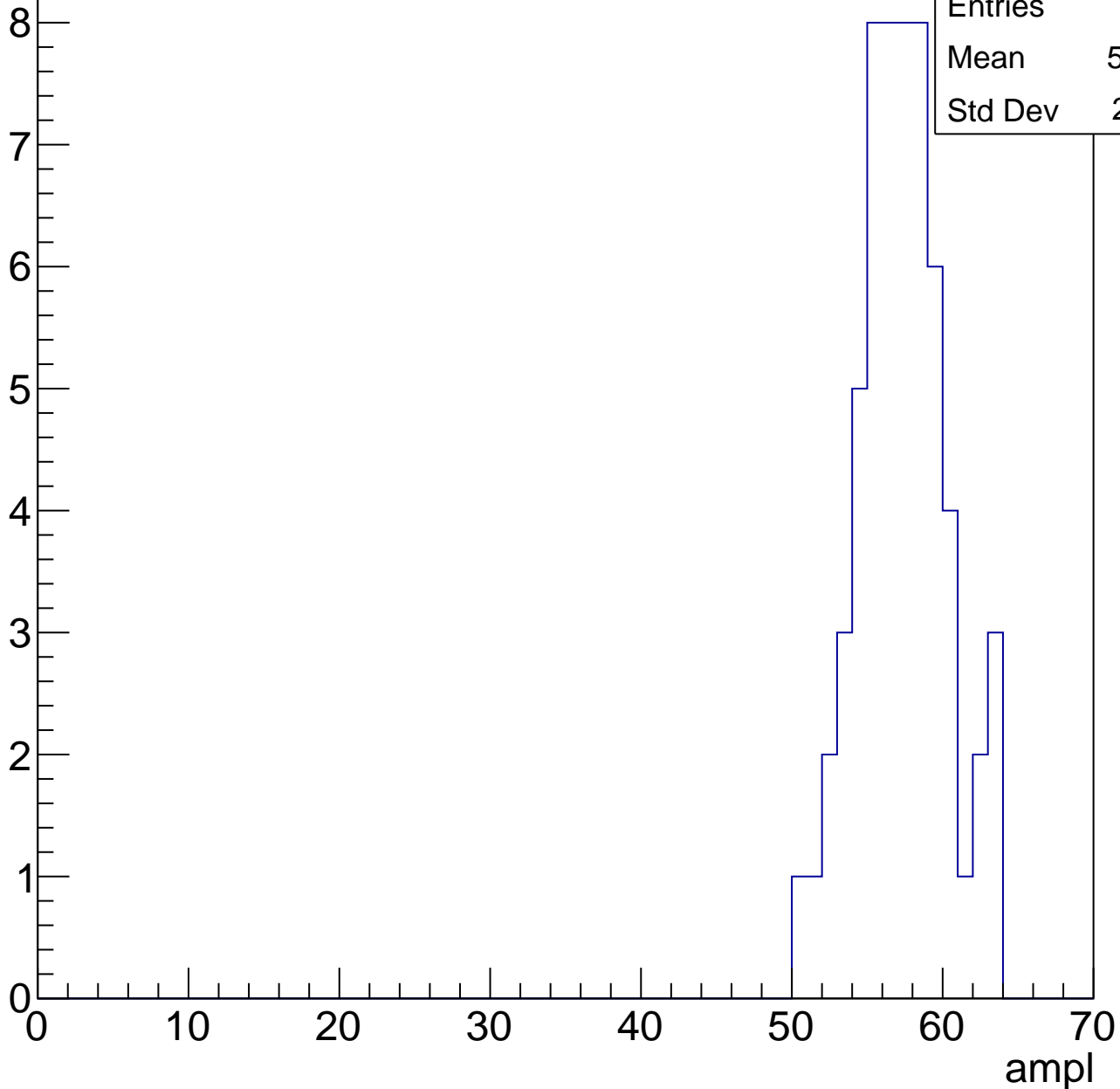


# B1L101S, U19-ch43, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	60
Mean	56.83
Std Dev	2.911

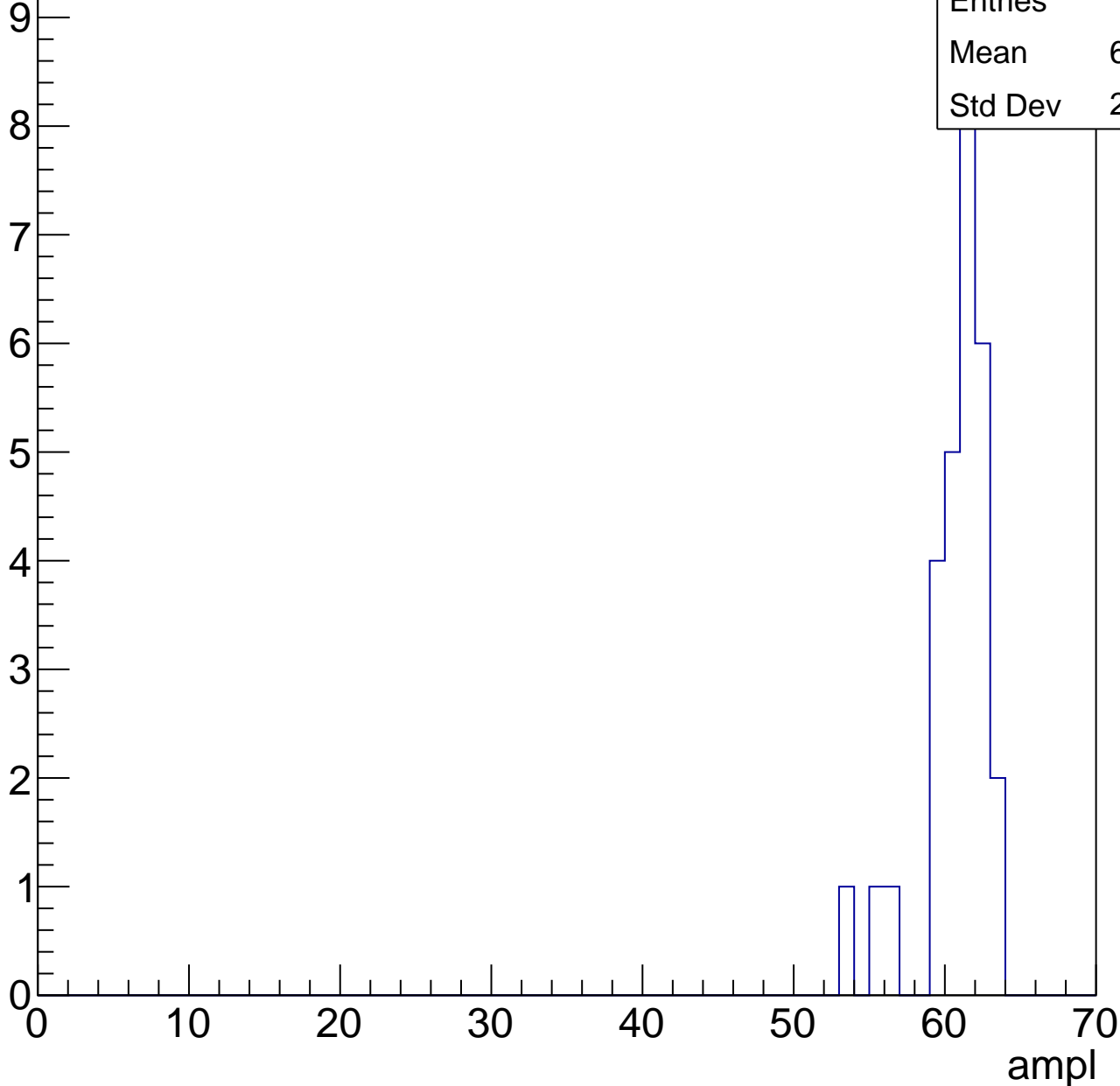


# B1L101S, U19-ch43, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	29
Mean	60.24
Std Dev	2.223

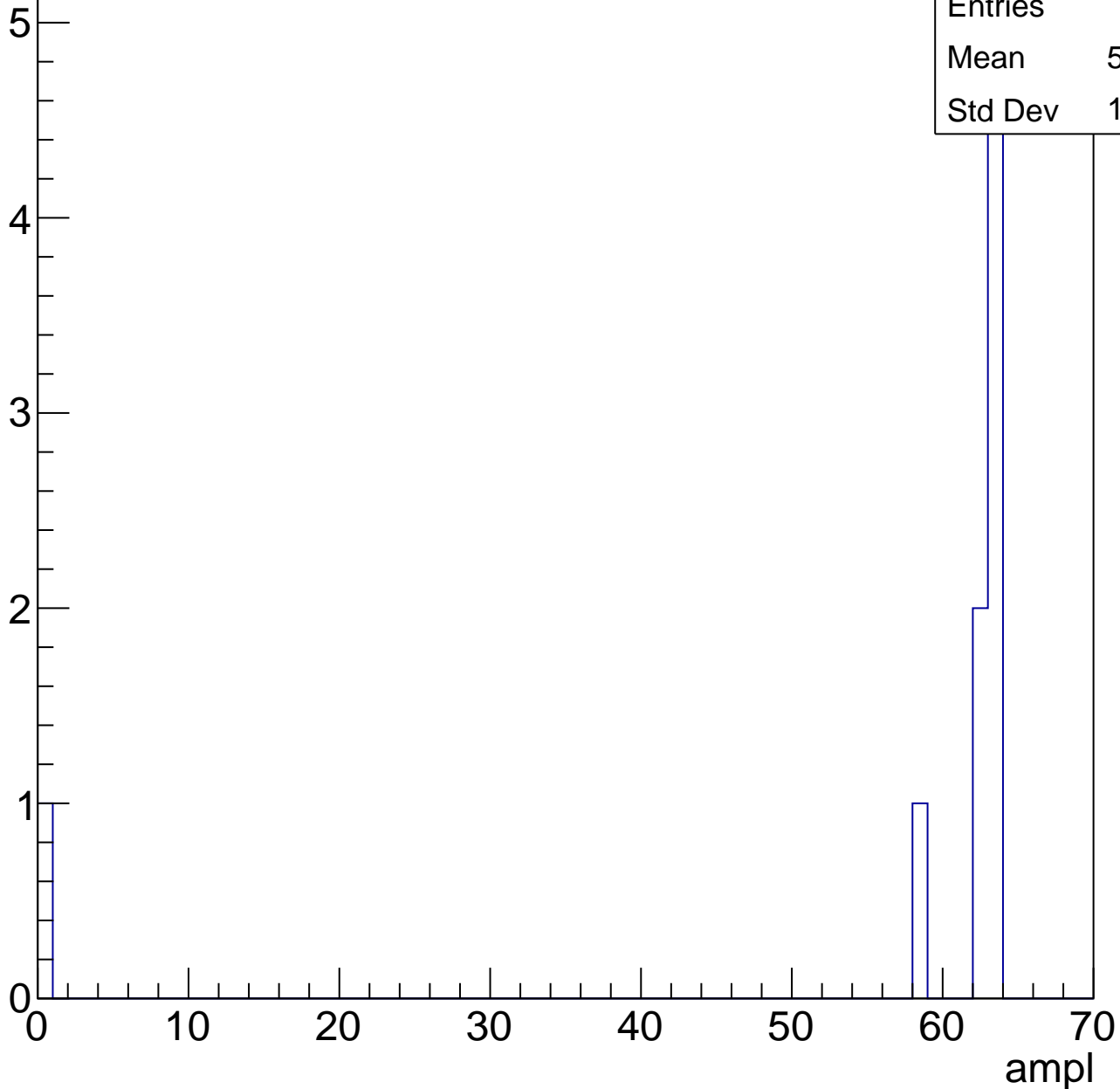


# B1L101S, U19-ch43, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	9
Mean	55.22
Std Dev	19.58





# B1L101S, U19-ch43, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L101S, U19-ch44, adc0

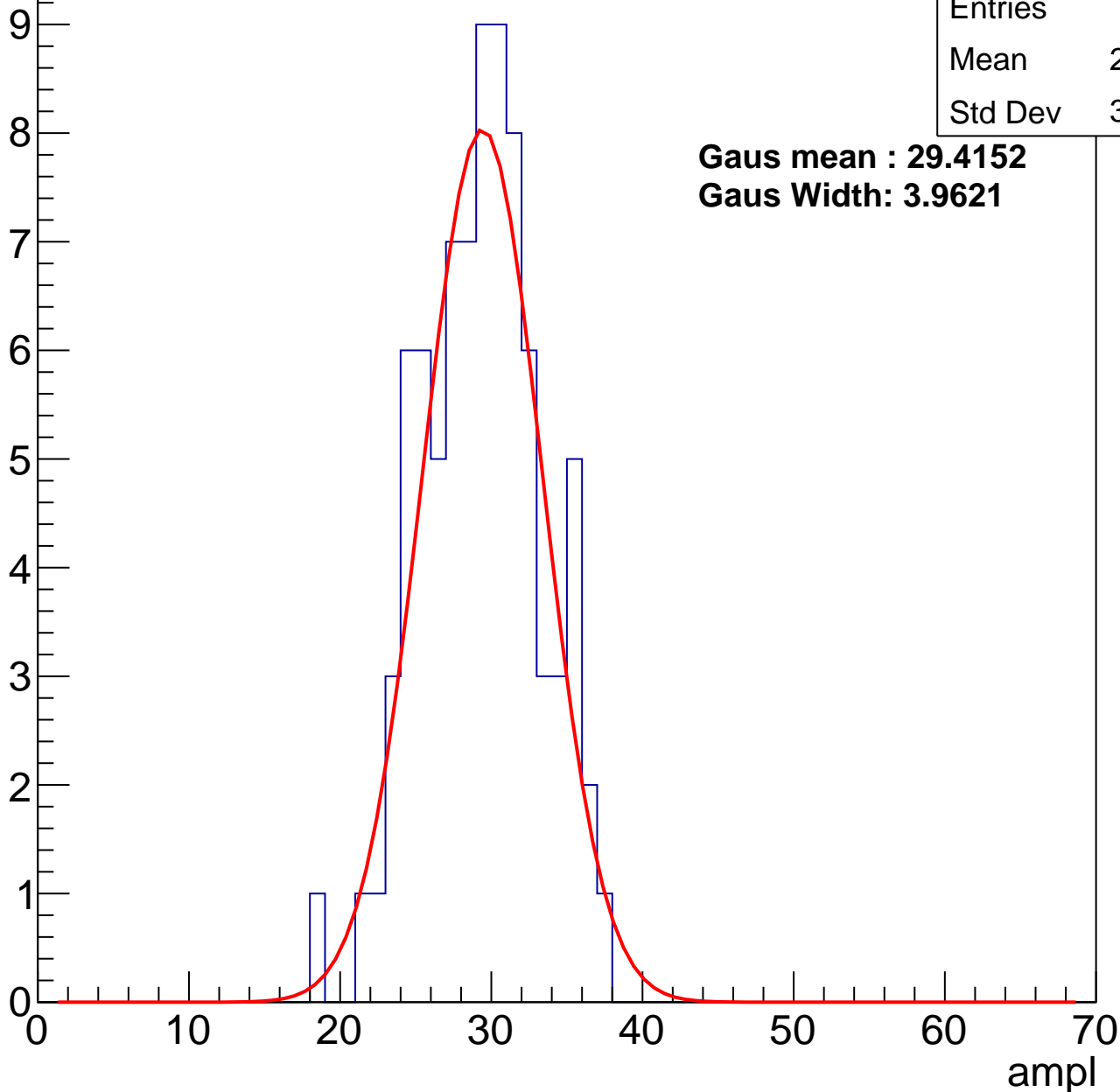
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	83
Mean	28.86
Std Dev	3.844

**Gaus mean : 29.4152**

**Gaus Width: 3.9621**



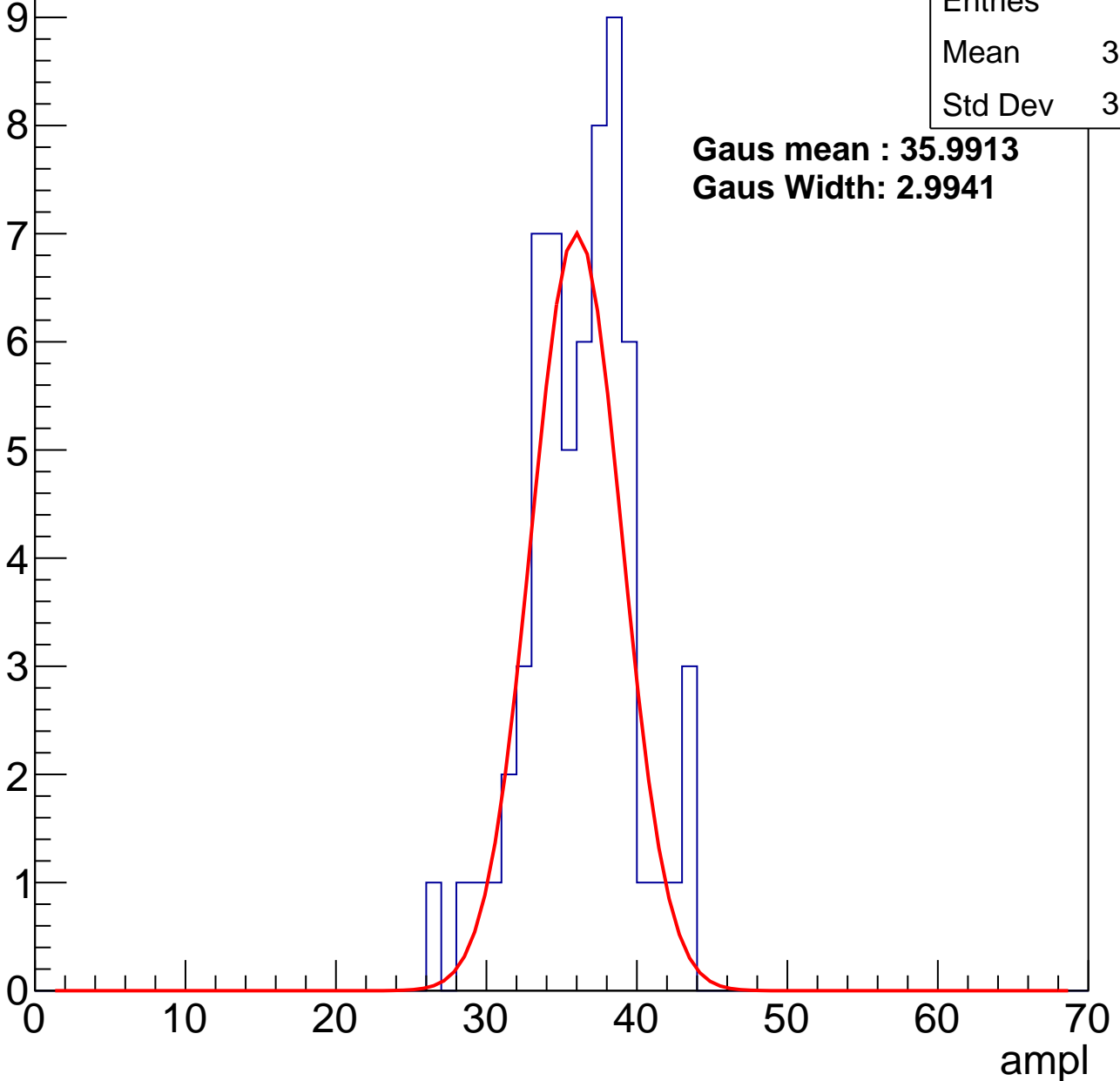
# B1L101S, U19-ch44, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	35.79
Std Dev	3.479

**Gaus mean : 35.9913**  
**Gaus Width: 2.9941**



# B1L101S, U19-ch44, adc2

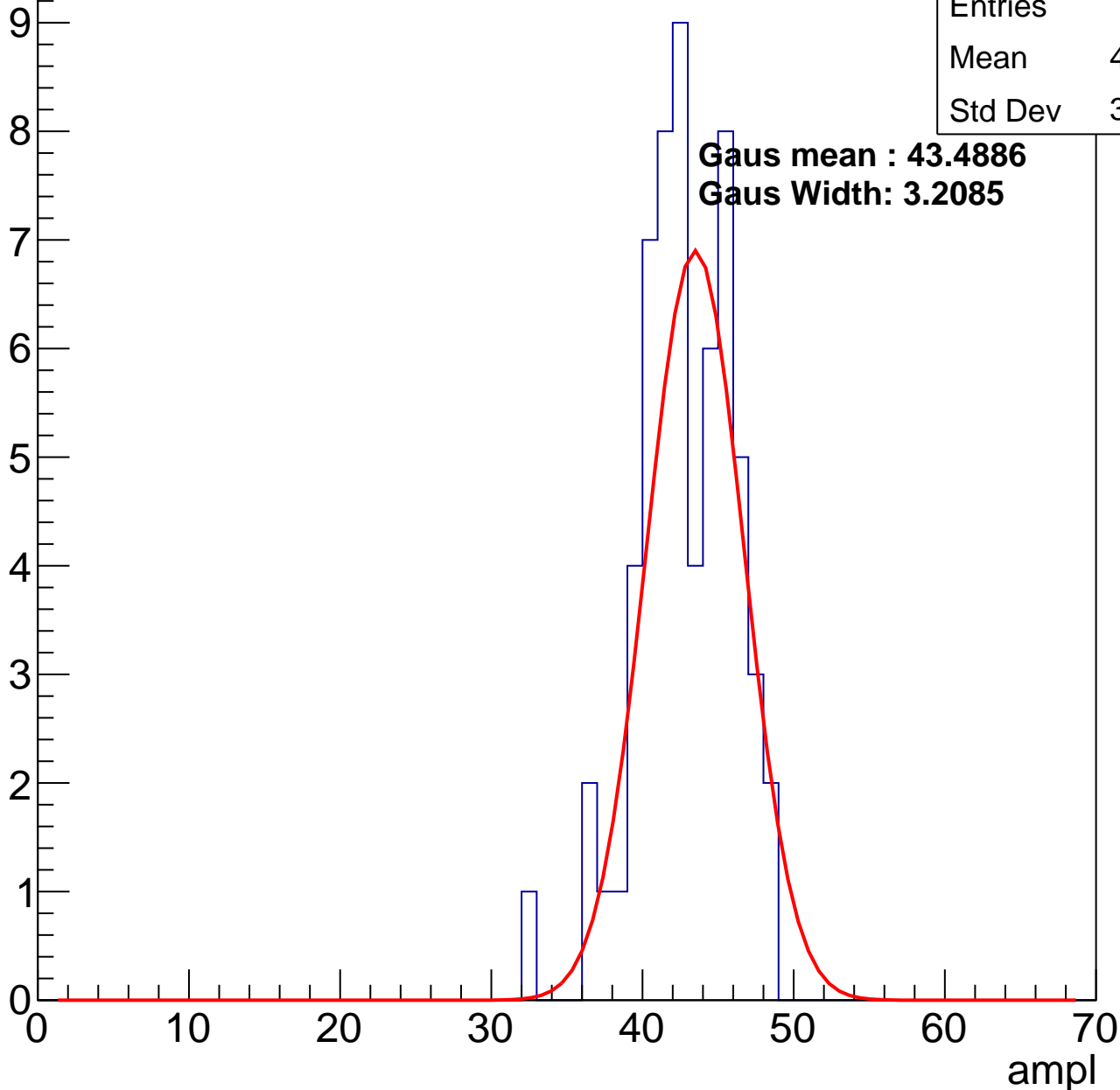
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	42.36
Std Dev	3.147

**Gaus mean : 43.4886**

**Gaus Width: 3.2085**

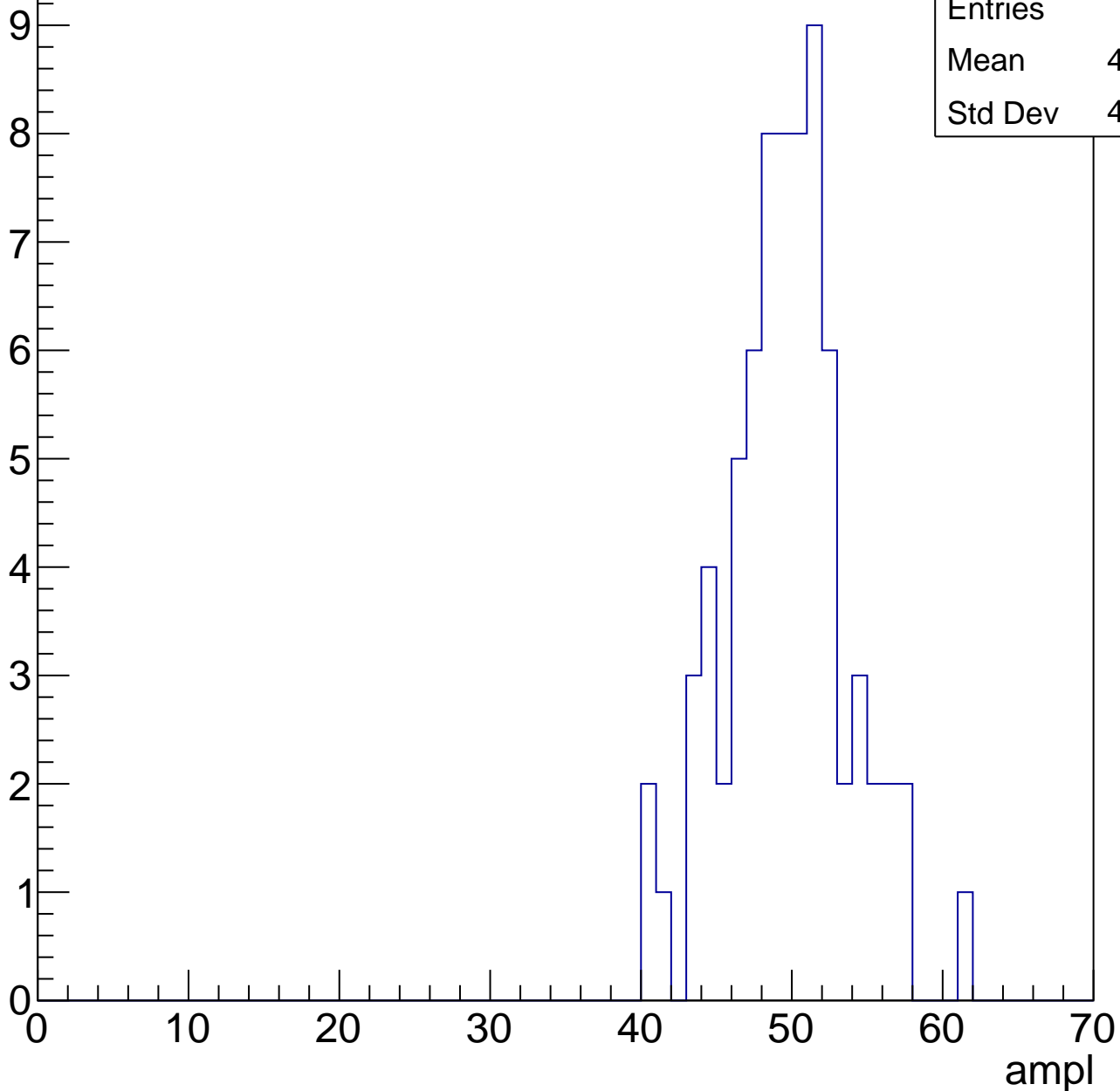


# B1L101S, U19-ch44, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

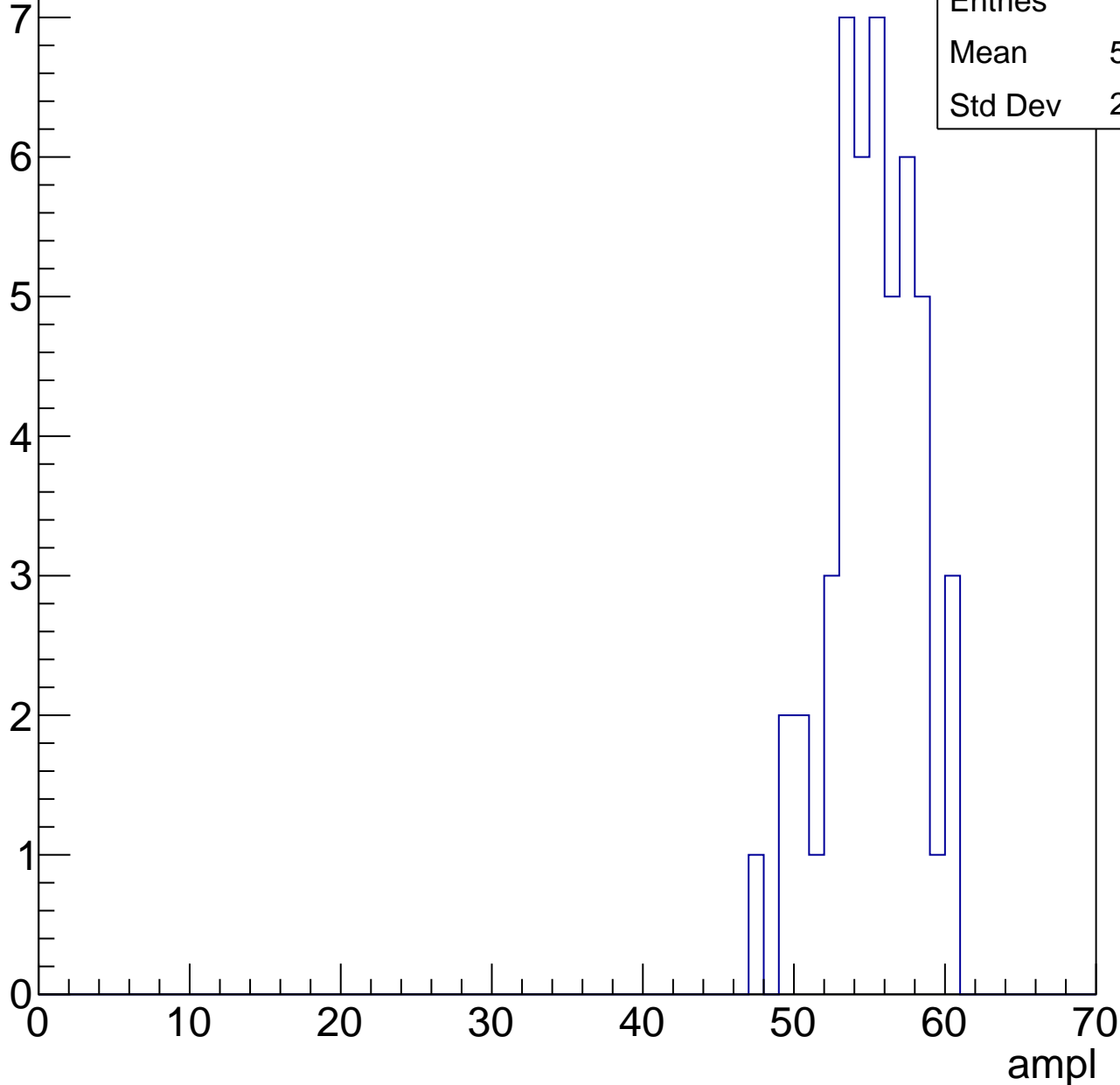
Entries	74
Mean	49.19
Std Dev	4.006



# B1L101S, U19-ch44, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

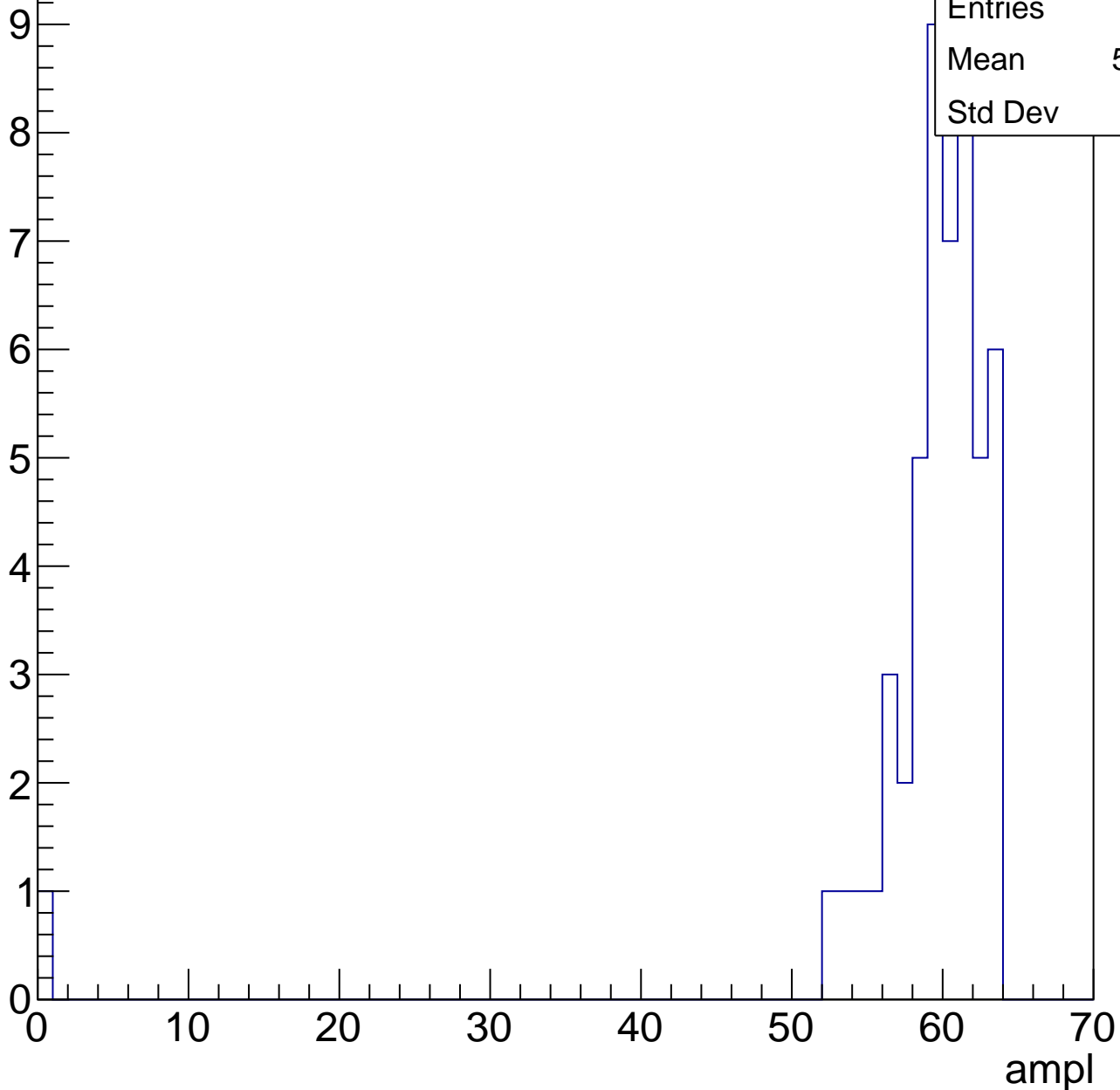
Entry



# B1L101S, U19-ch44, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

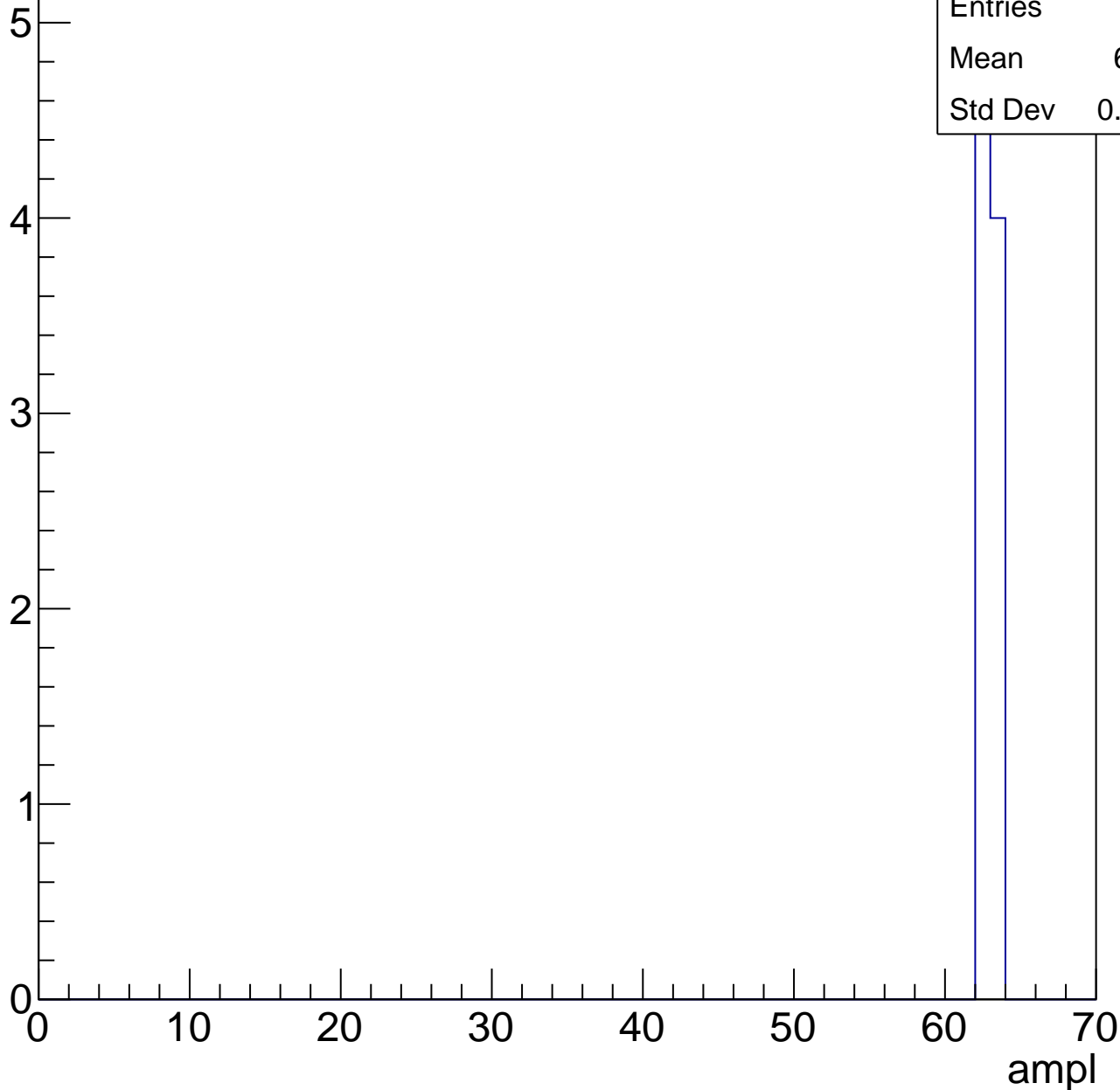


# B1L101S, U19-ch44, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	9
Mean	62.44
Std Dev	0.4969





# B1L101S, U19-ch44, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U19-ch45, adc0

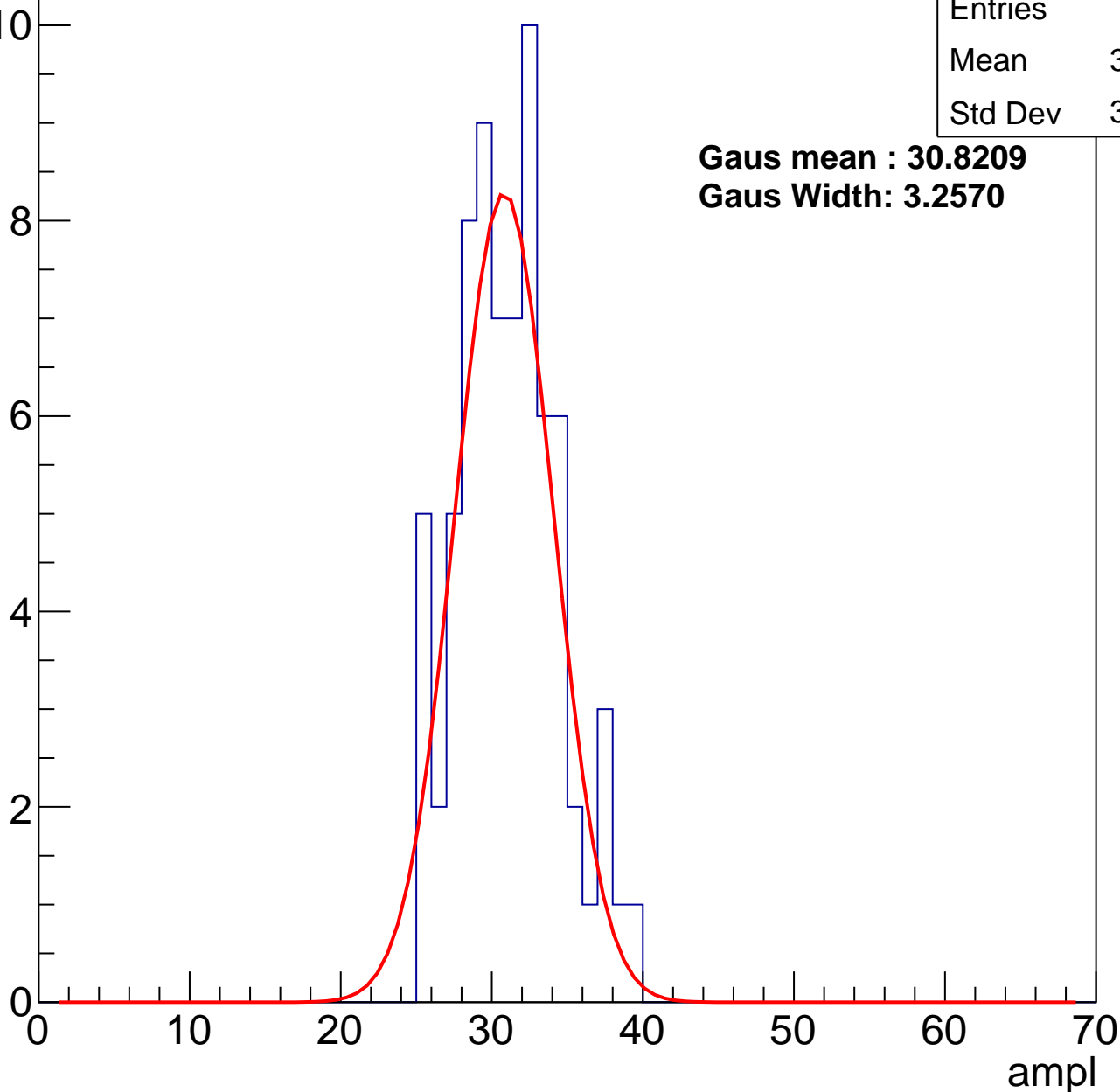
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	73
Mean	30.68
Std Dev	3.277

**Gaus mean : 30.8209**

**Gaus Width: 3.2570**



# B1L101S, U19-ch45, adc1

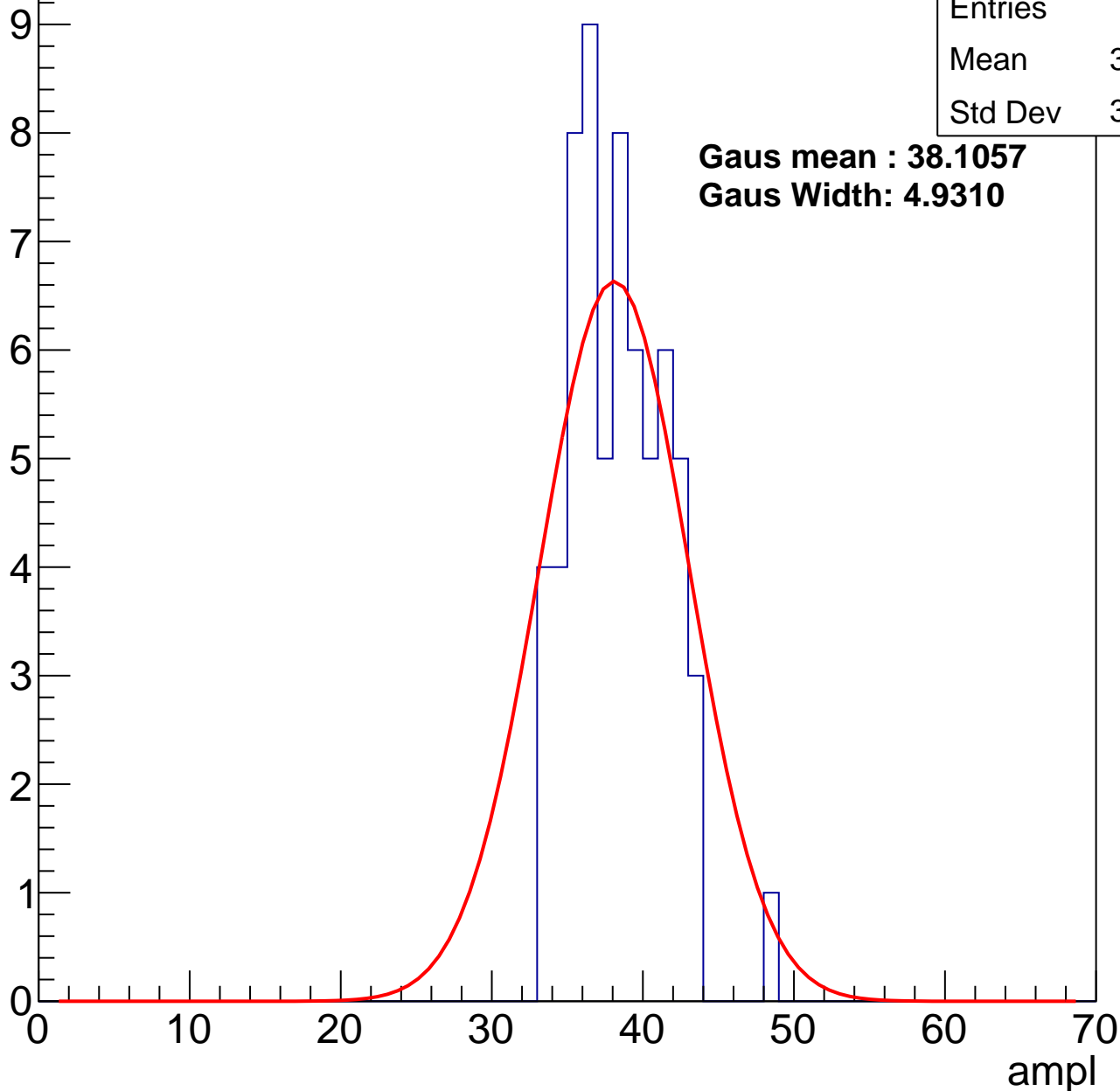
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	37.94
Std Dev	3.092

**Gaus mean : 38.1057**

**Gaus Width: 4.9310**



# B1L101S, U19-ch45, adc2

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	71
Mean	44.2
Std Dev	3.138

**Gaus mean : 45.0592**

**Gaus Width: 3.5004**

10

8

6

4

2

0

0

10

20

30

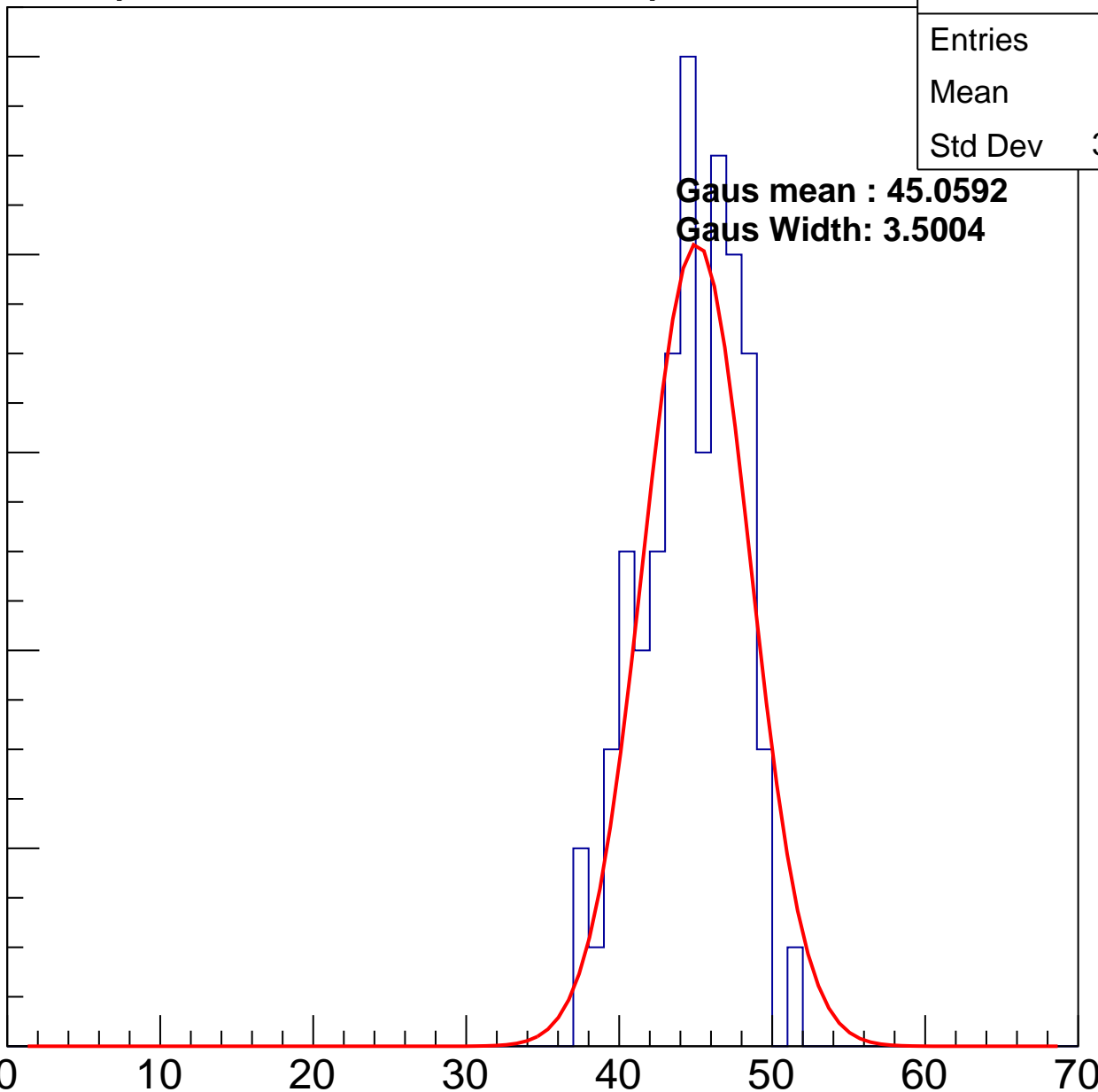
40

50

60

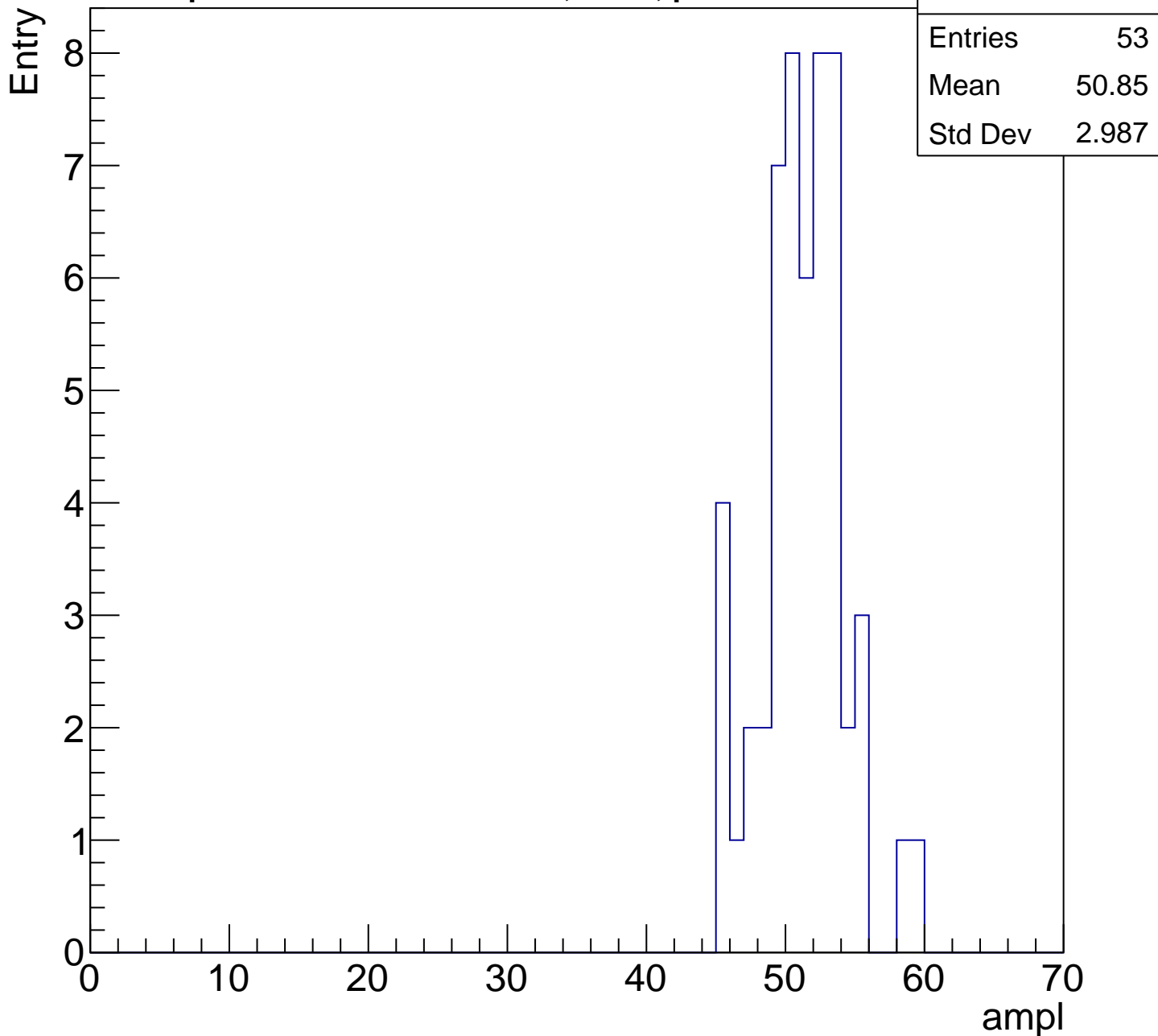
70

ampl



# B1L101S, U19-ch45, adc3

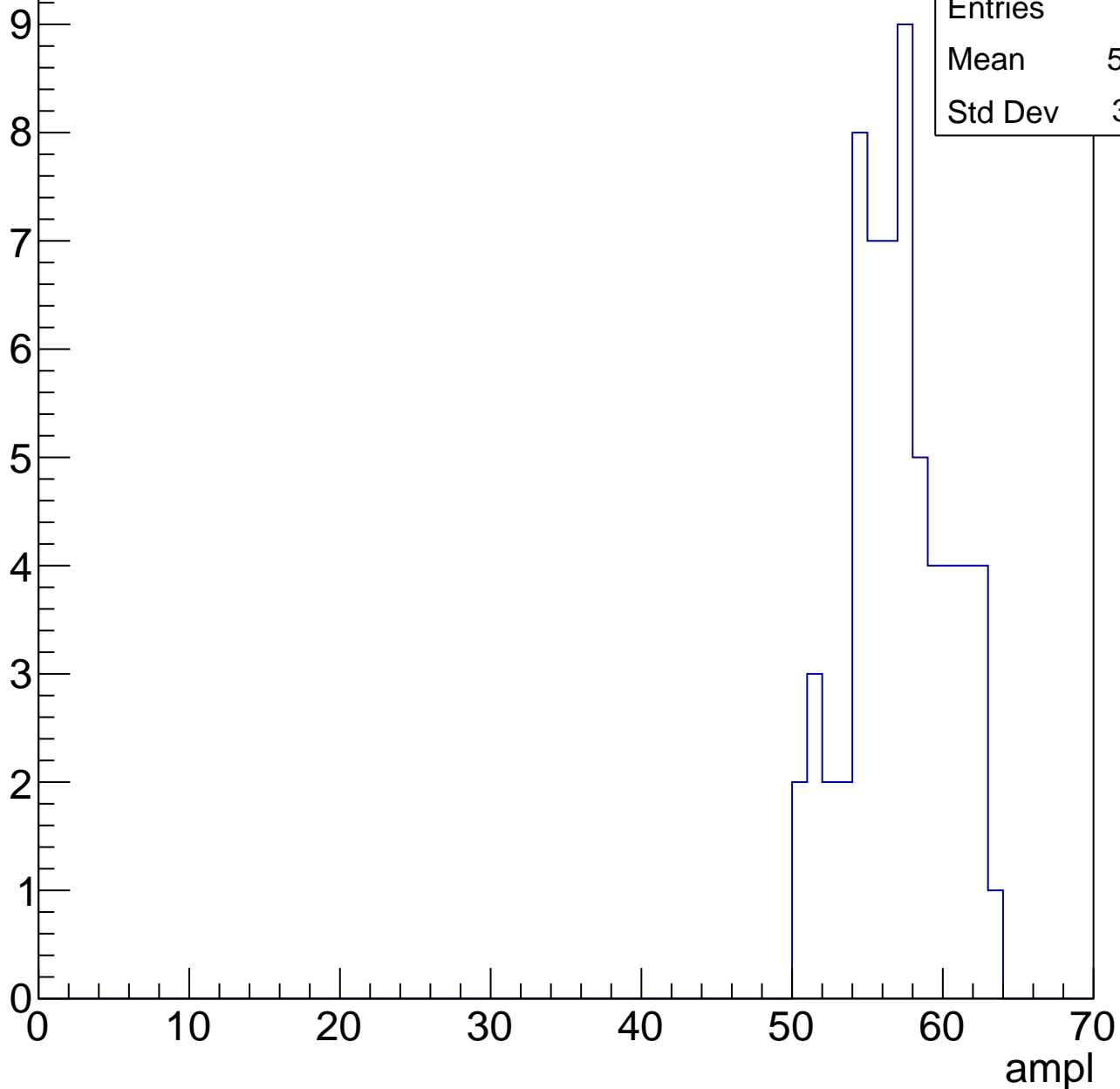
calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U19-ch45, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



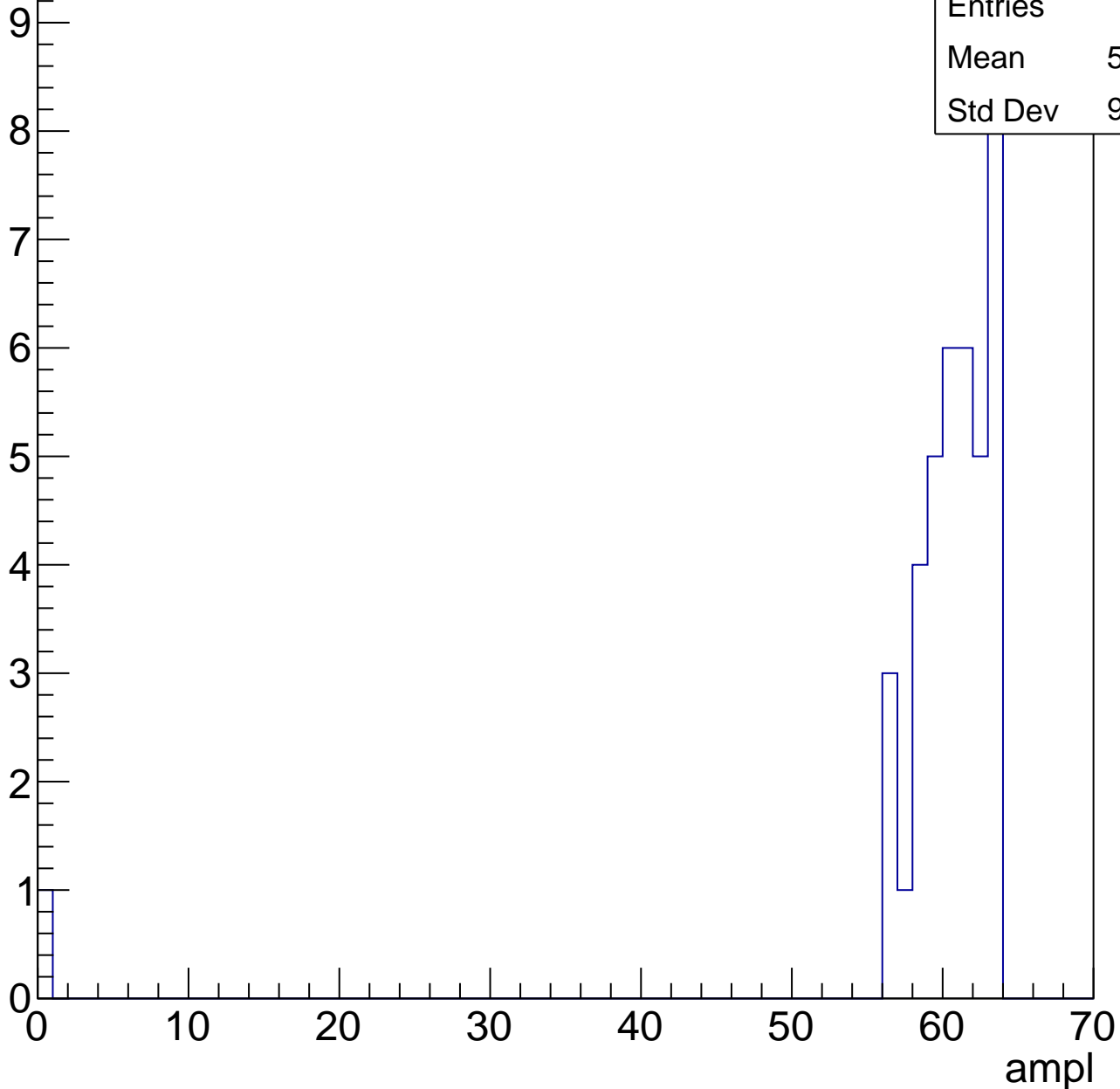
Entries	62
Mean	56.55
Std Dev	3.211

# B1L101S, U19-ch45, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	40
Mean	58.88
Std Dev	9.662



# B1L101S, U19-ch45, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	62
Std Dev	0



# B1L101S, U19-ch45, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U19-ch46, adc0

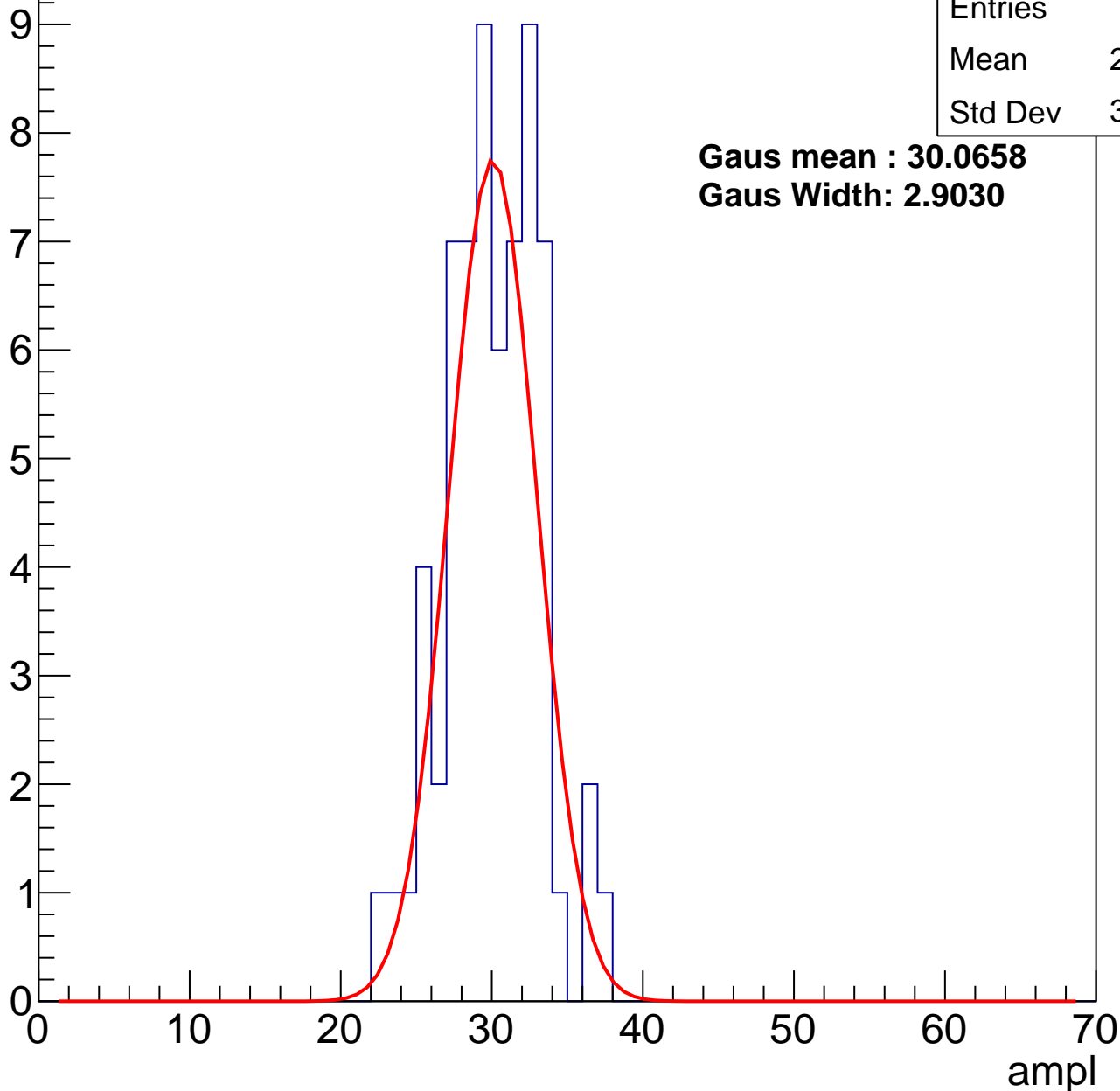
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	29.63
Std Dev	3.076

**Gaus mean : 30.0658**

**Gaus Width: 2.9030**



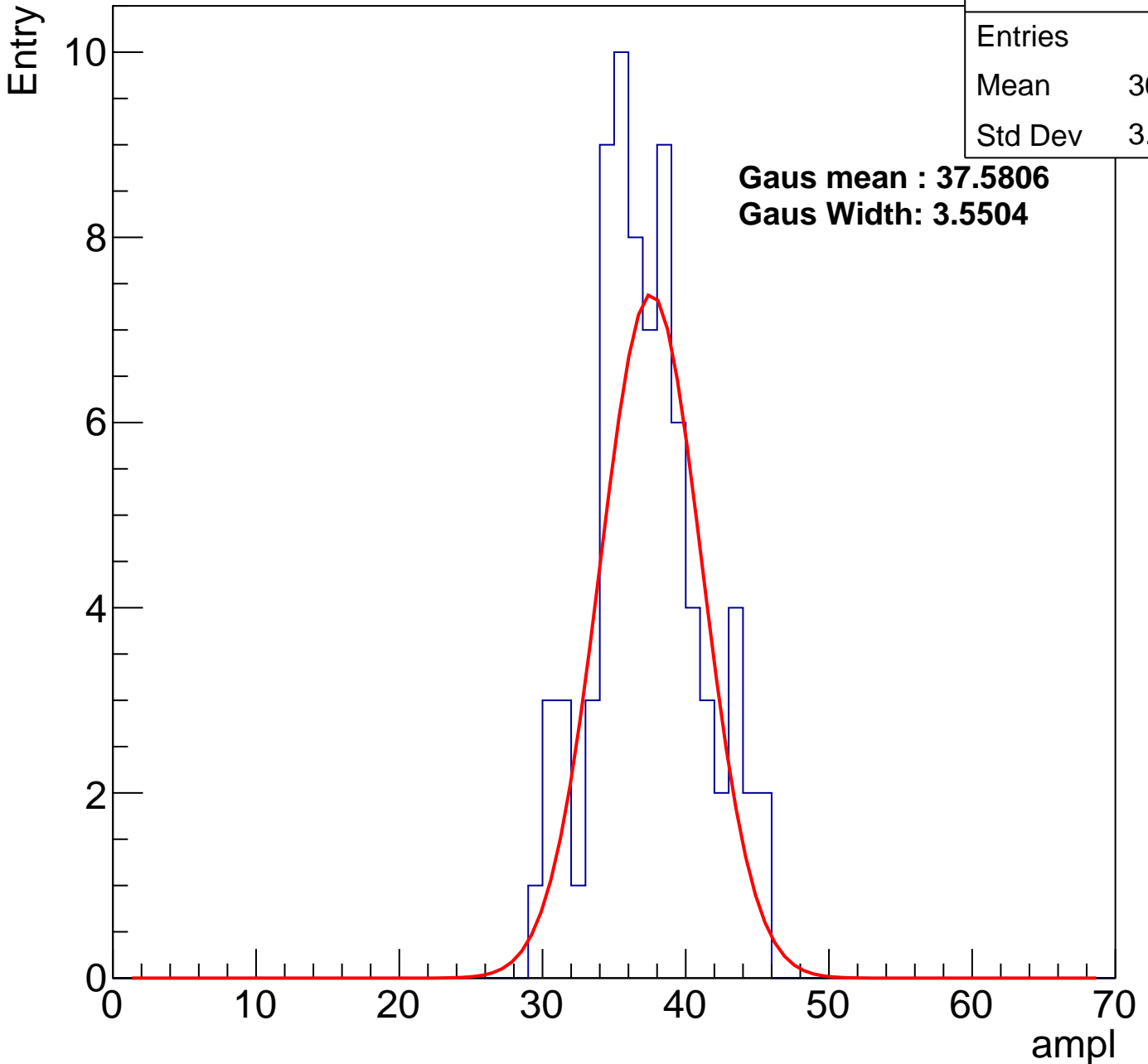
# B1L101S, U19-ch46, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	77
Mean	36.87
Std Dev	3.705

**Gaus mean : 37.5806**

**Gaus Width: 3.5504**



# B1L101S, U19-ch46, adc2

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

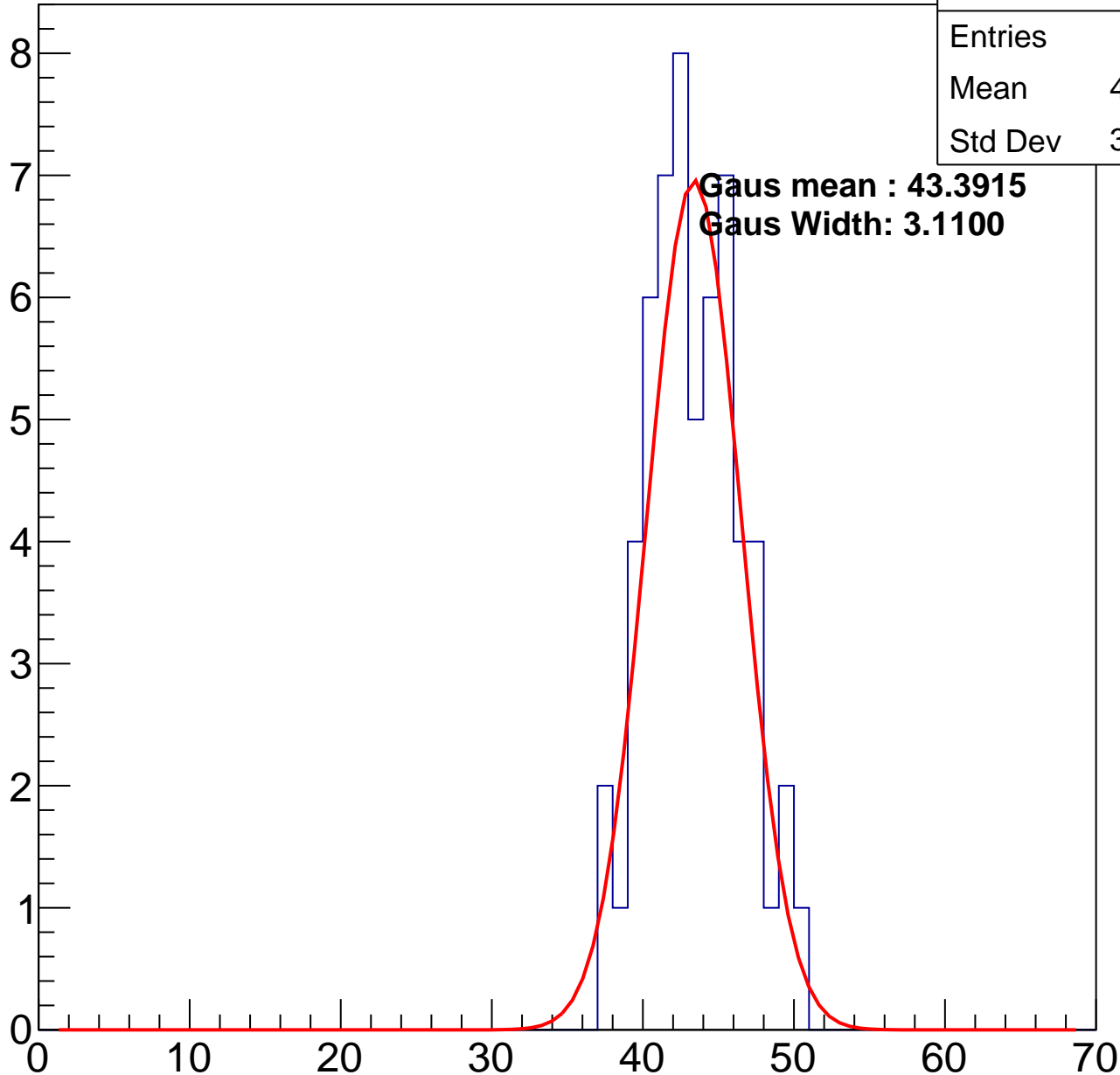
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	58
Mean	42.98
Std Dev	3.026

**Gaus mean : 43.3915**

**Gaus Width: 3.1100**

ampl



# B1L101S, U19-ch46, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

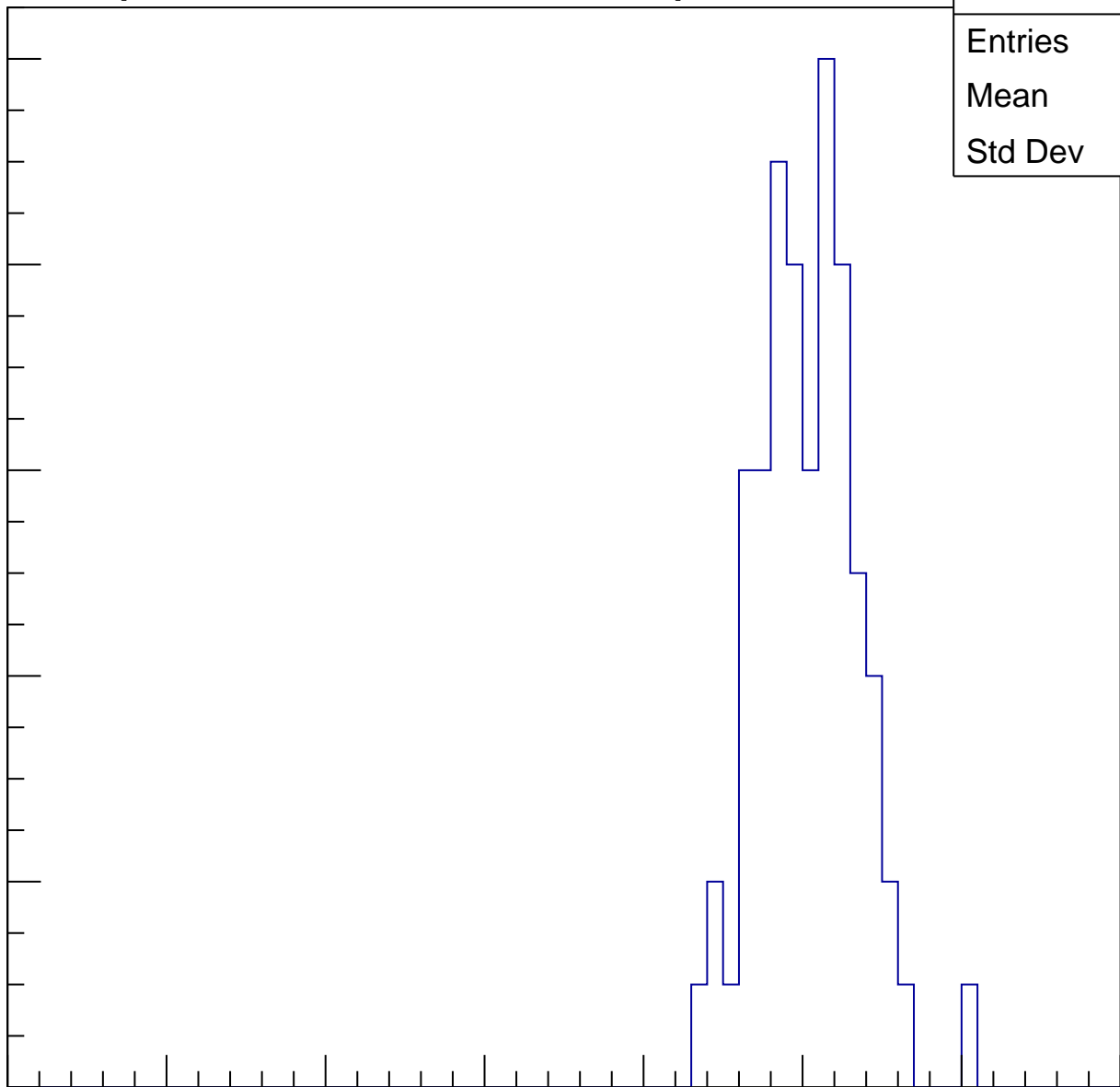
Entries	70
Mean	49.87
Std Dev	3.107

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

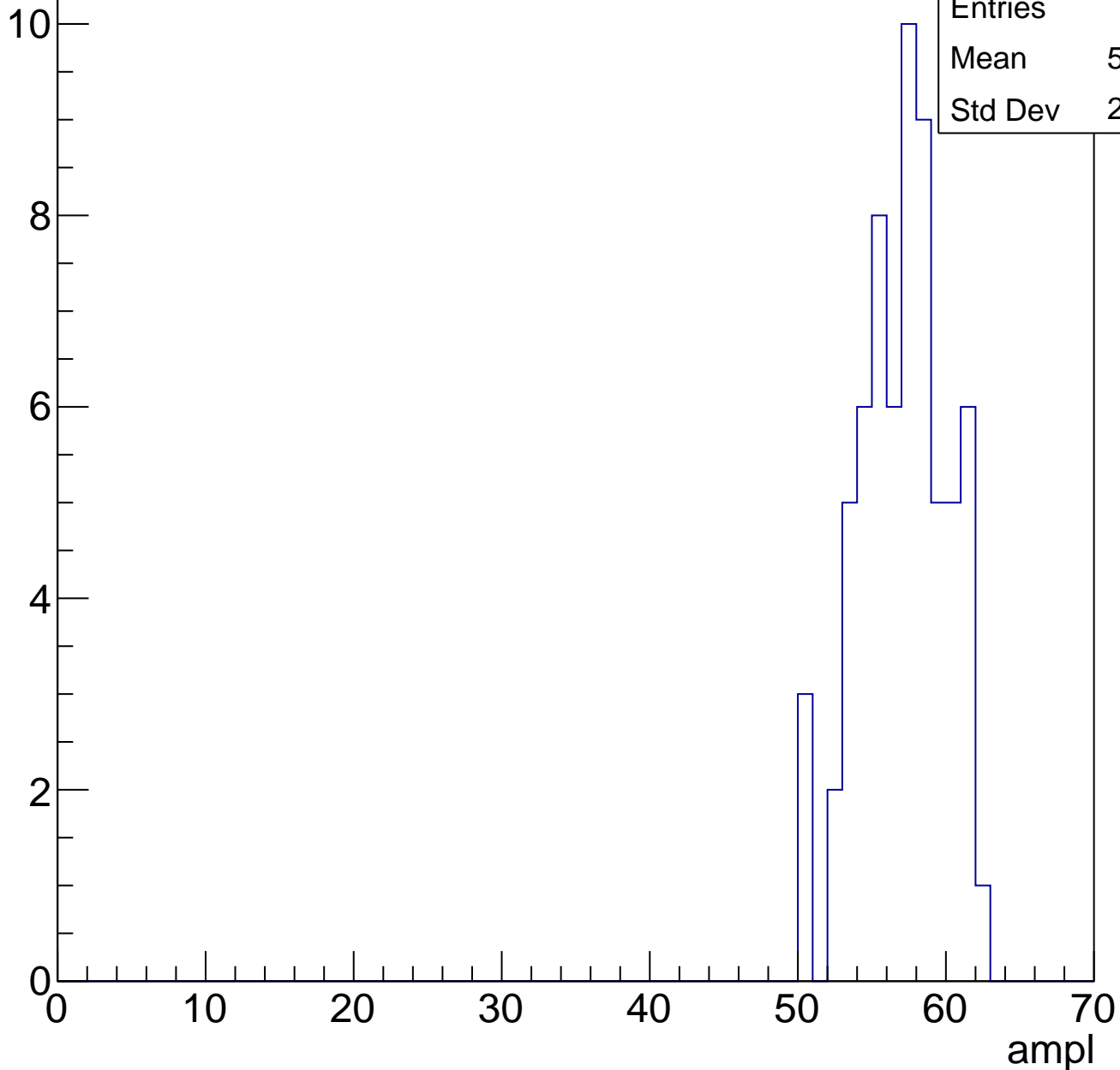


# B1L101S, U19-ch46, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	66
Mean	56.58
Std Dev	2.892

Entry

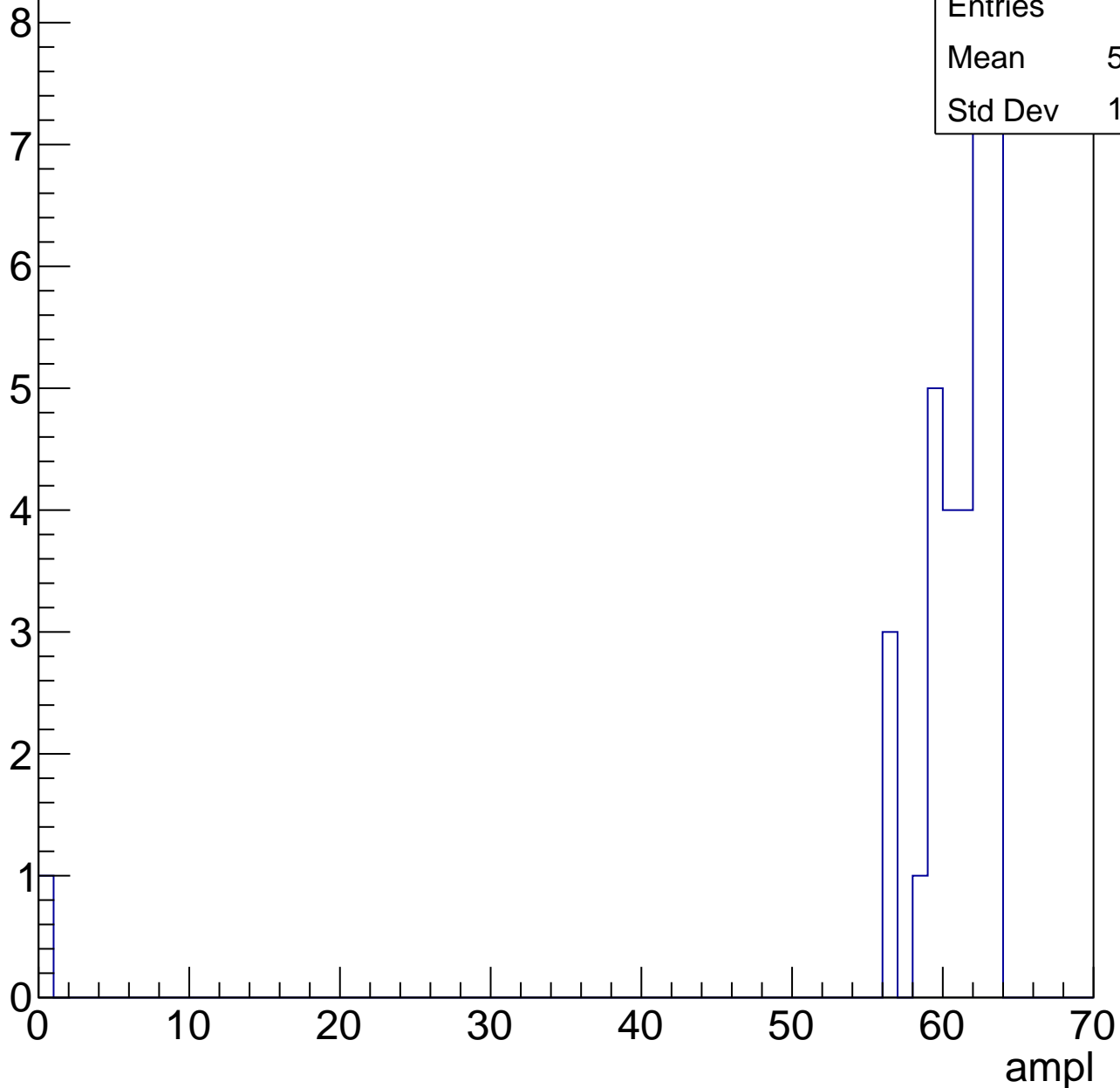


# B1L101S, U19-ch46, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	34
Mean	58.97
Std Dev	10.47



# B1L101S, U19-ch46, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U19-ch46, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U19-ch47, adc0

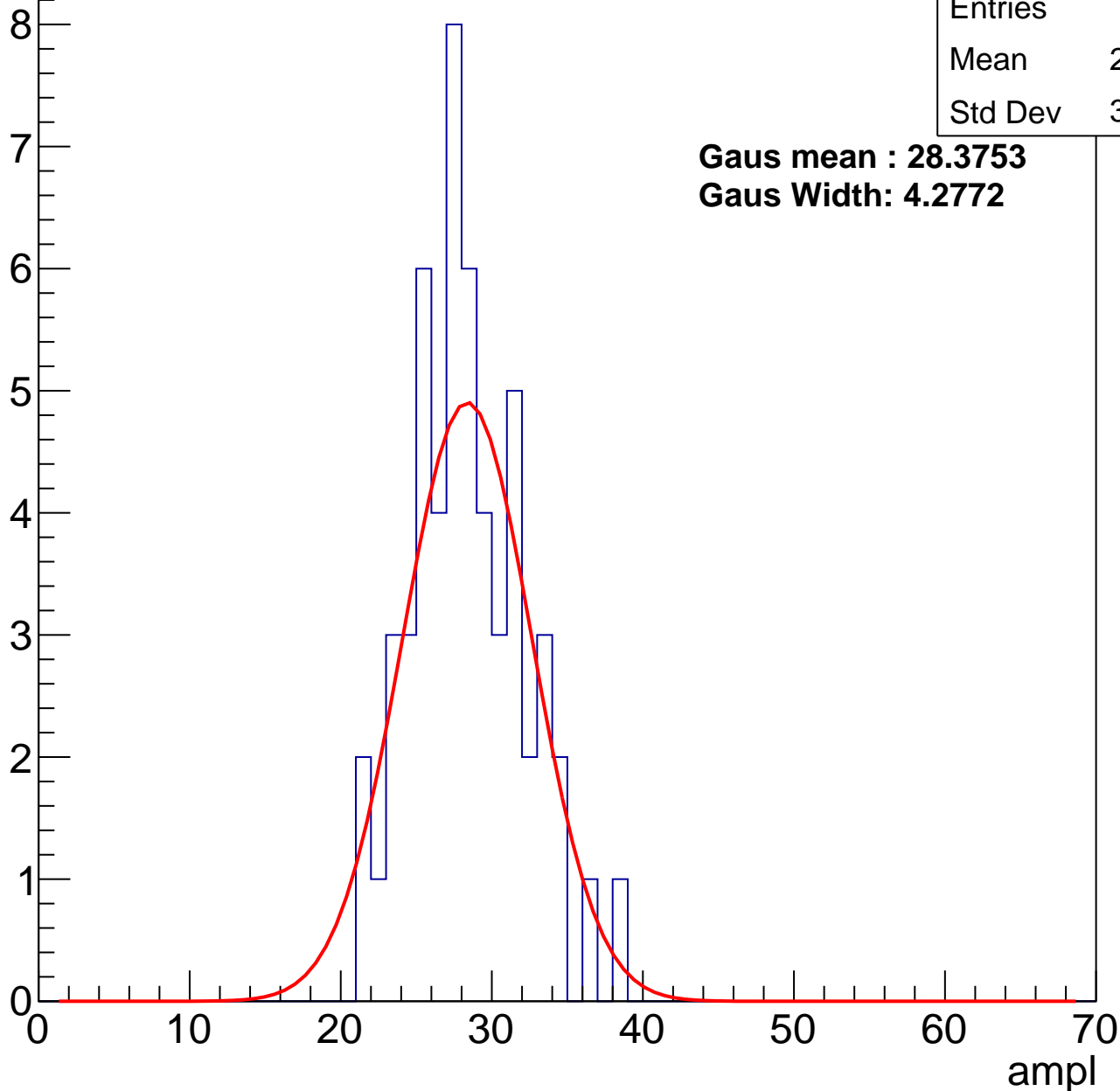
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	54
Mean	27.94
Std Dev	3.699

**Gaus mean : 28.3753**

**Gaus Width: 4.2772**

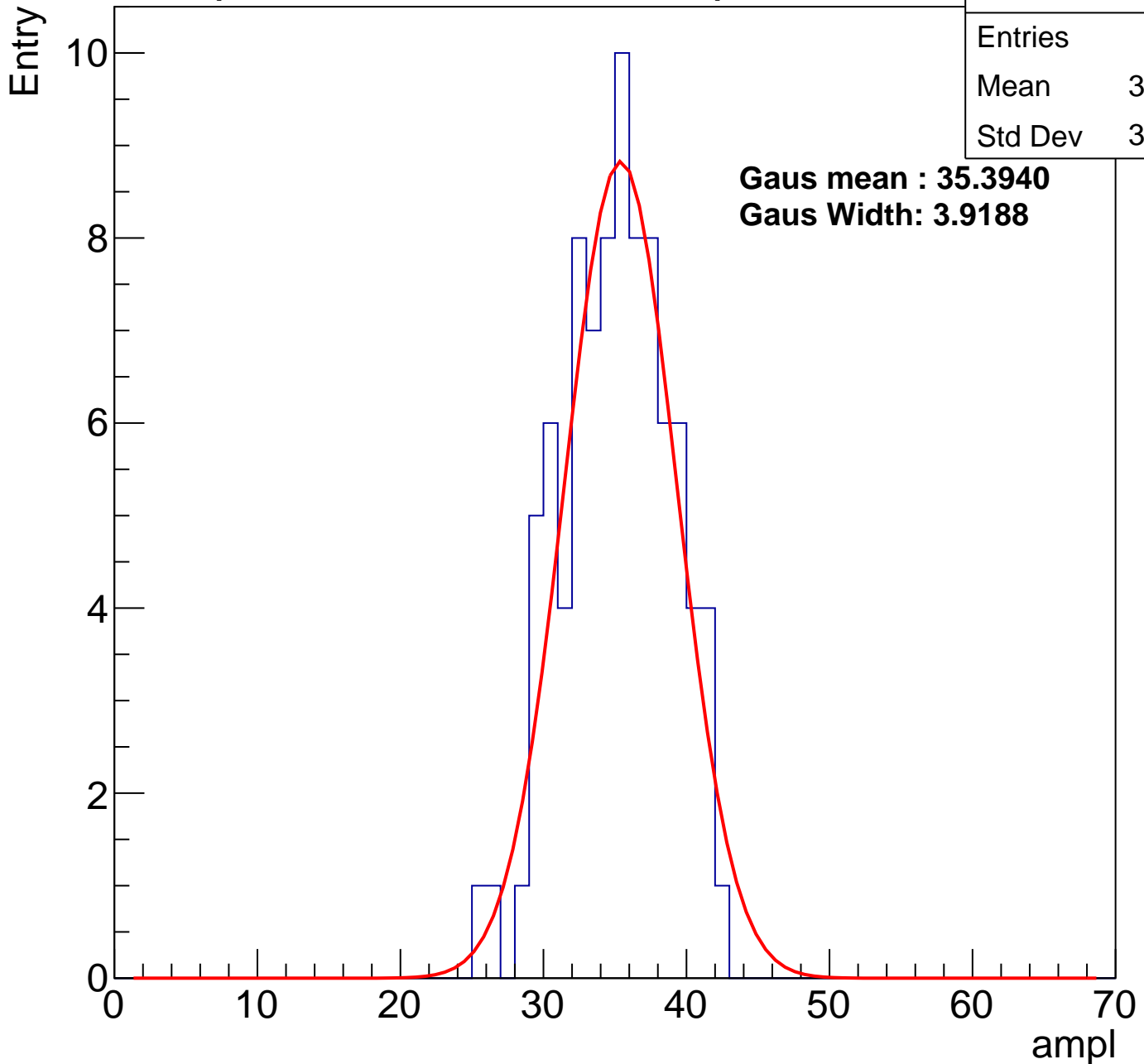


# B1L101S, U19-ch47, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	88
Mean	34.65
Std Dev	3.699

**Gaus mean : 35.3940**  
**Gaus Width: 3.9188**



# B1L101S, U19-ch47, adc2

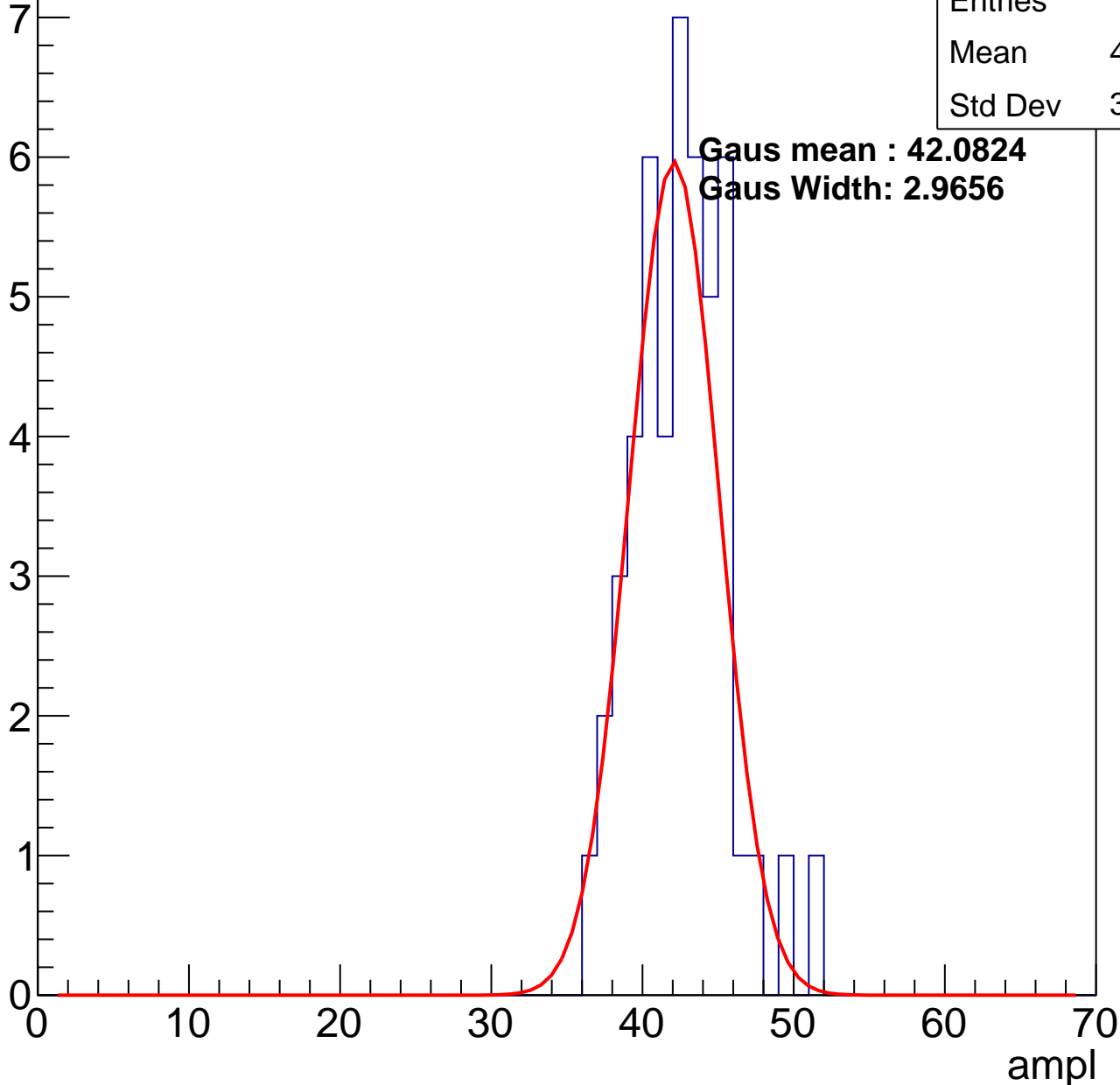
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	48
Mean	42.06
Std Dev	3.058

Gaus mean : 42.0824

Gaus Width: 2.9656

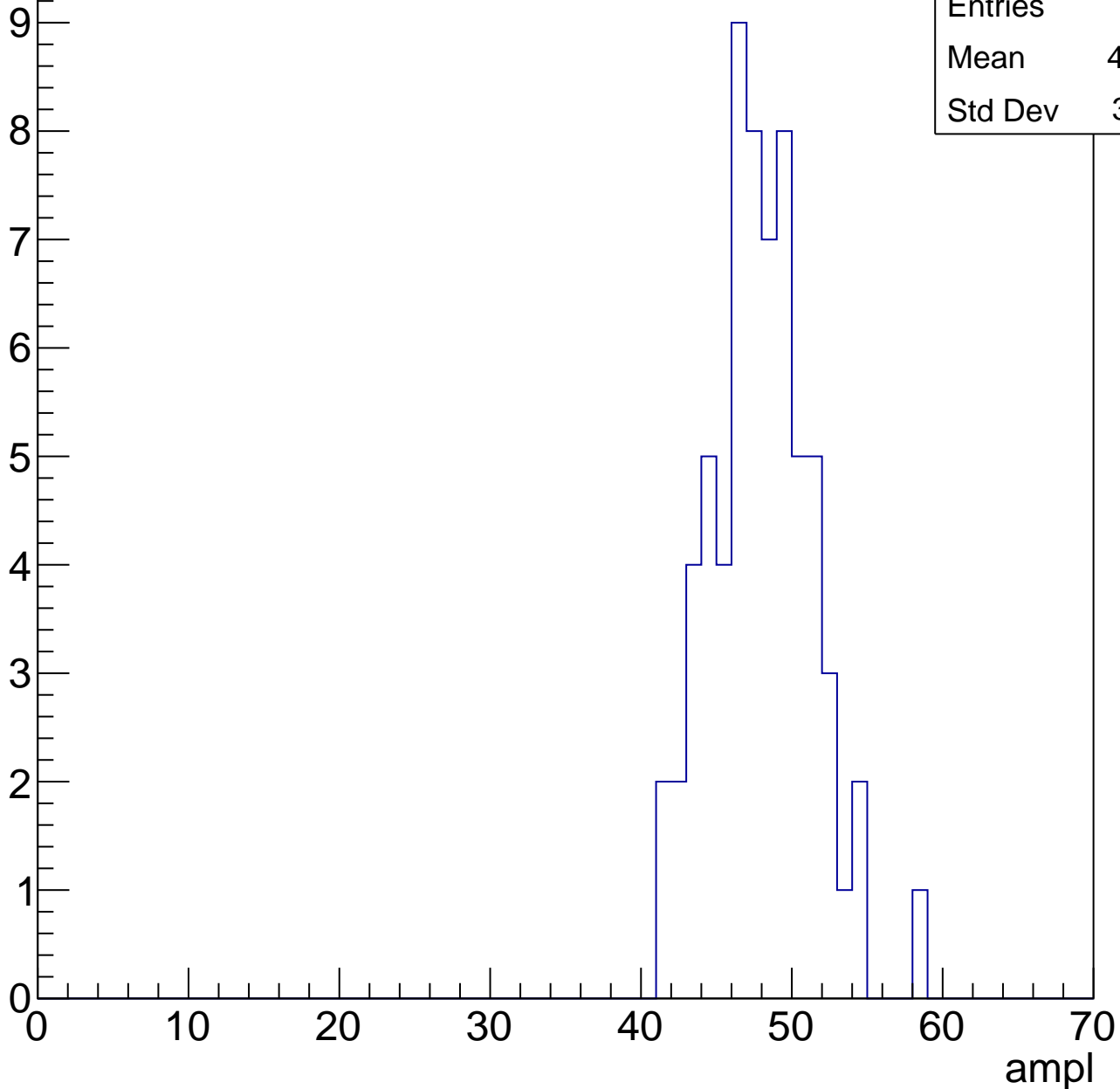


# B1L101S, U19-ch47, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	66
Mean	47.52
Std Dev	3.331



# B1L101S, U19-ch47, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

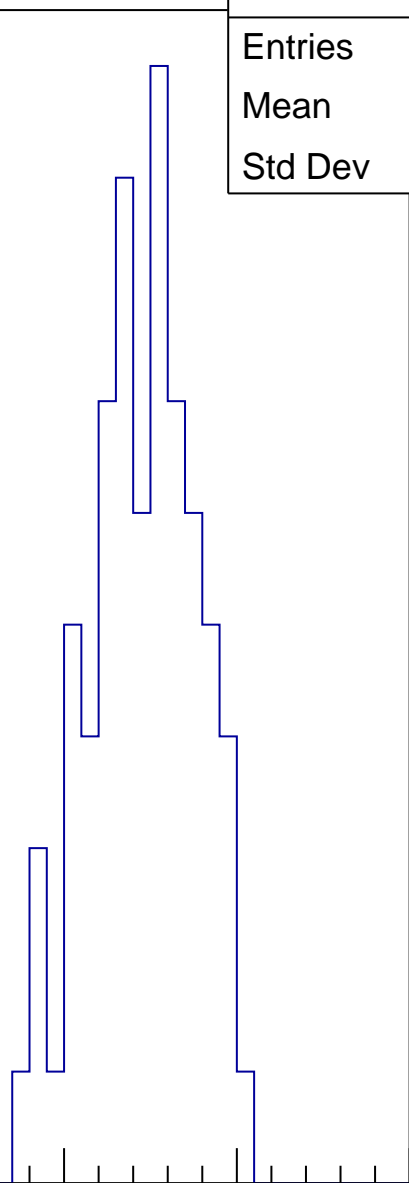
Entries	69
Mean	54.04
Std Dev	3.052

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

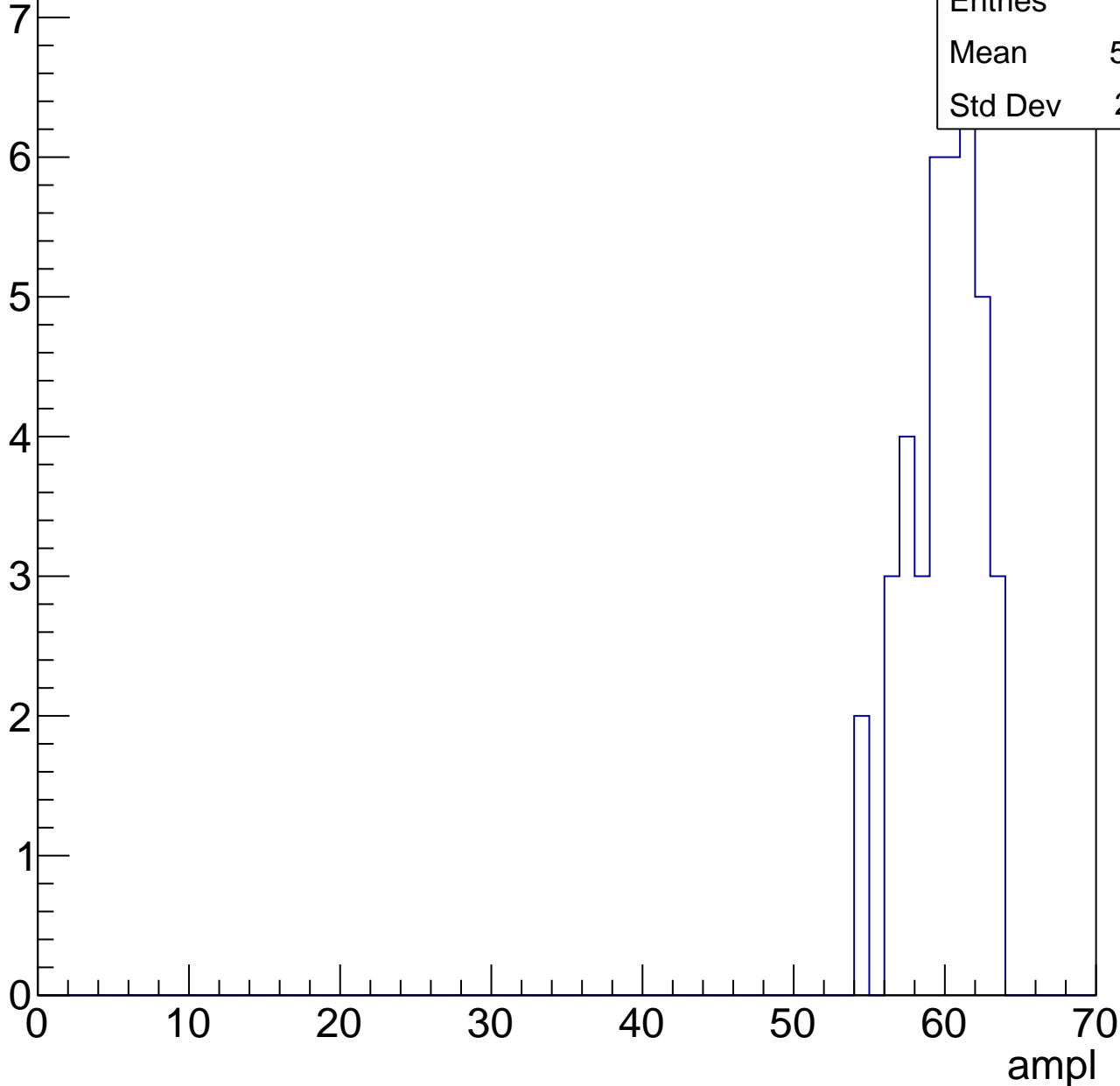


# B1L101S, U19-ch47, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	39
Mean	59.44
Std Dev	2.351

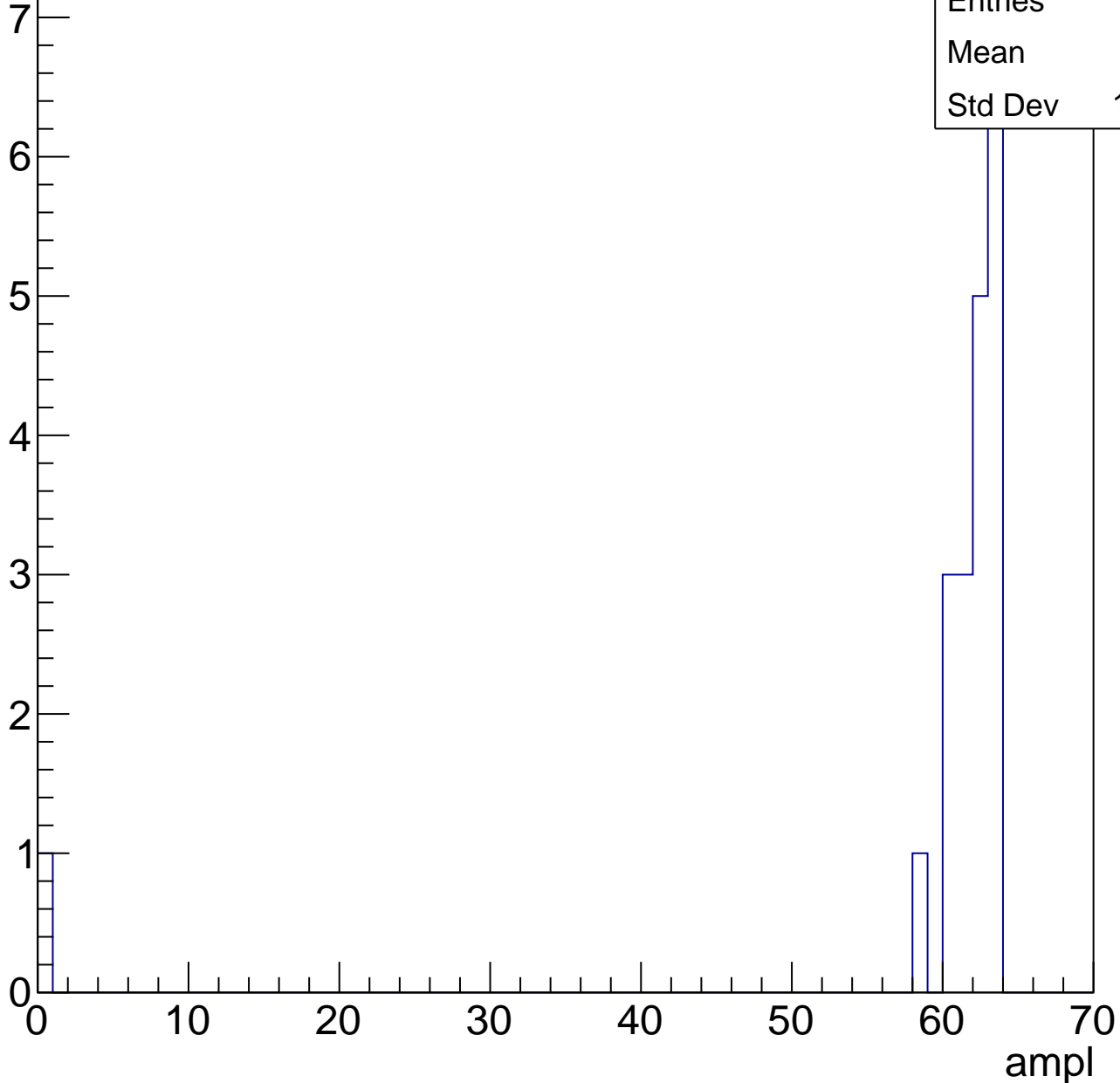


# B1L101S, U19-ch47, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	20
Mean	58.6
Std Dev	13.51





# B1L101S, U19-ch47, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L101S, U19-ch48, adc0

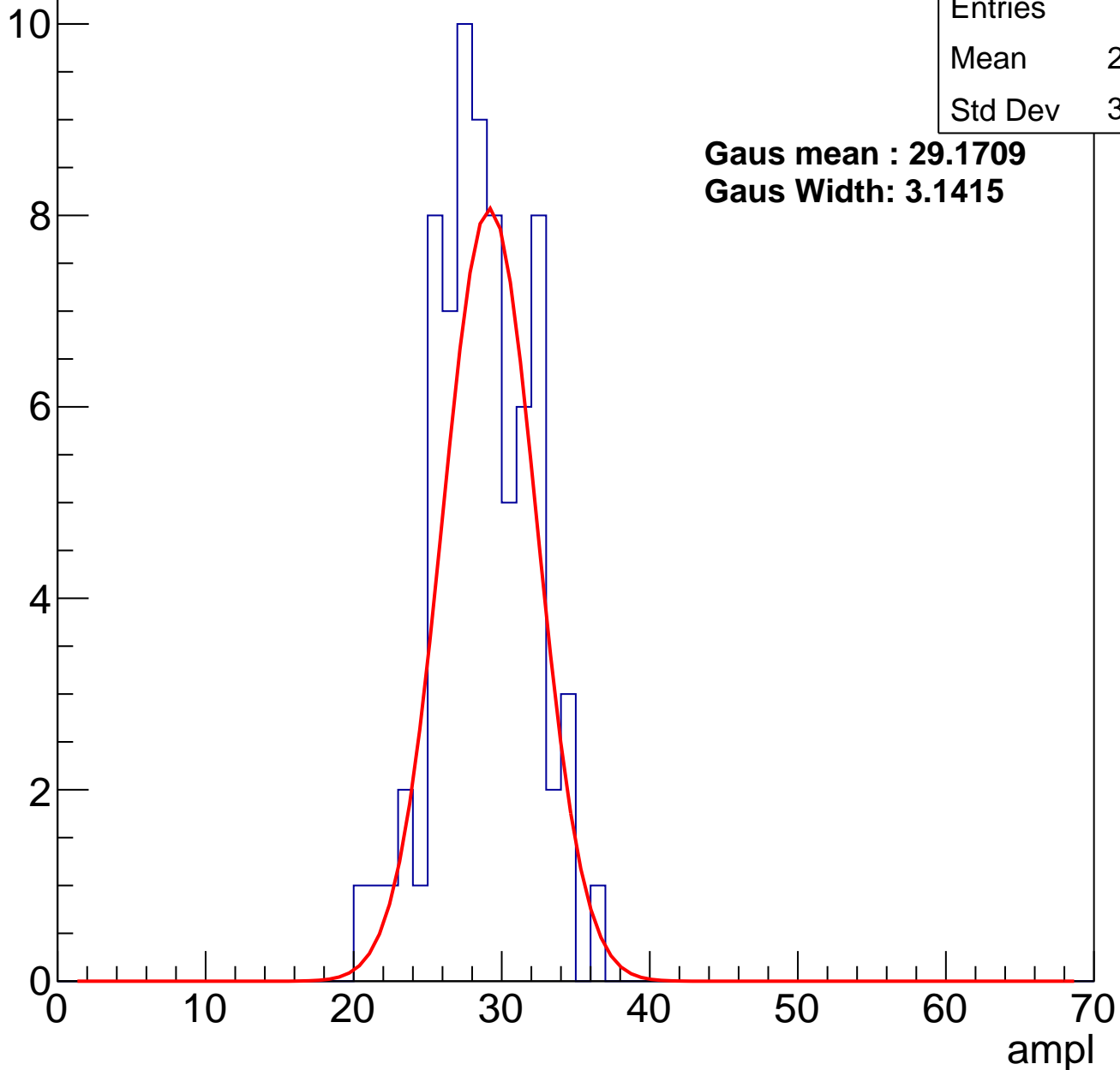
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	73
Mean	28.29
Std Dev	3.207

**Gaus mean : 29.1709**

**Gaus Width: 3.1415**

Entry



# B1L101S, U19-ch48, adc1

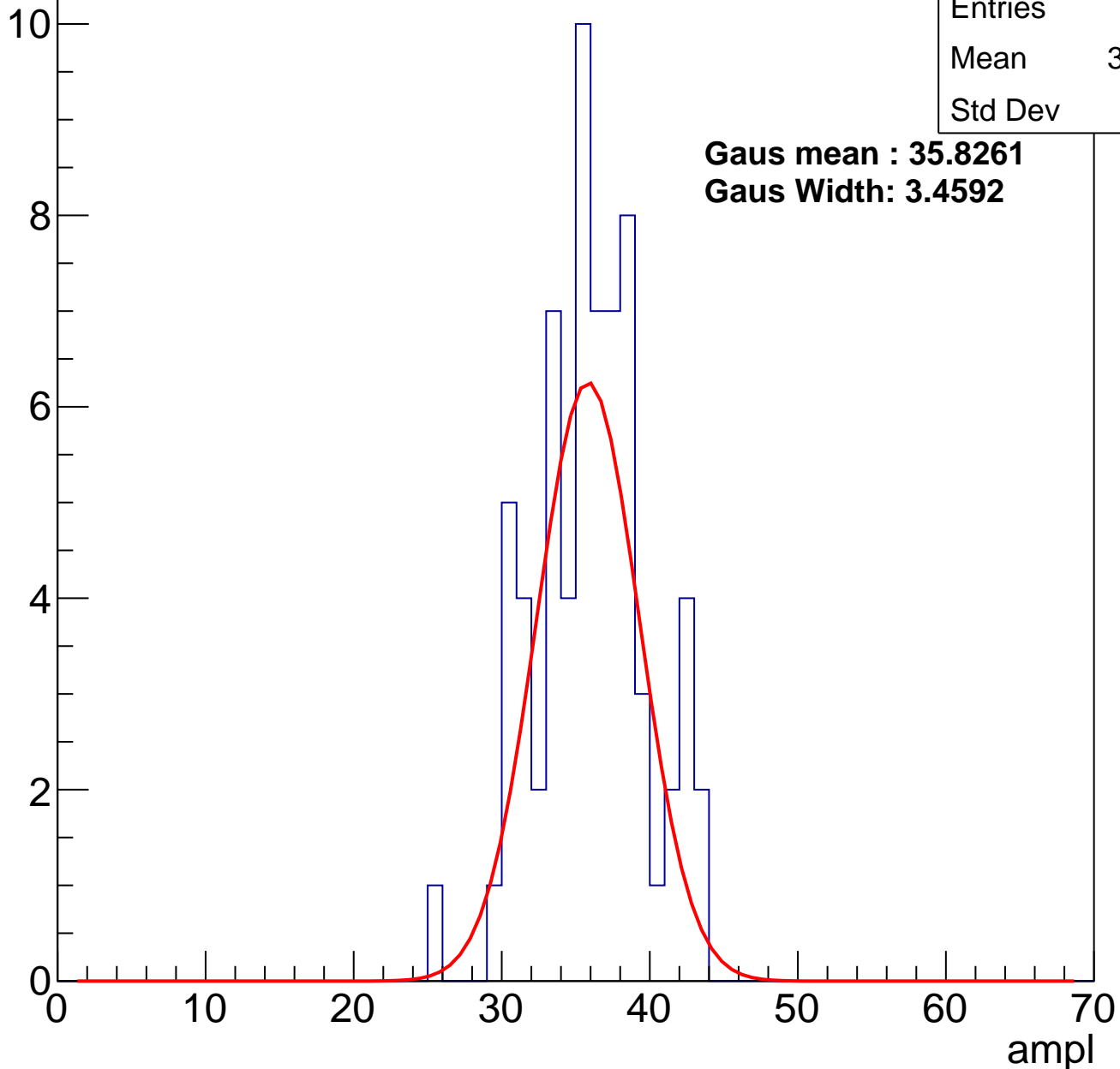
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	68
Mean	35.54
Std Dev	3.7

**Gaus mean : 35.8261**

**Gaus Width: 3.4592**

Entry



# B1L101S, U19-ch48, adc2

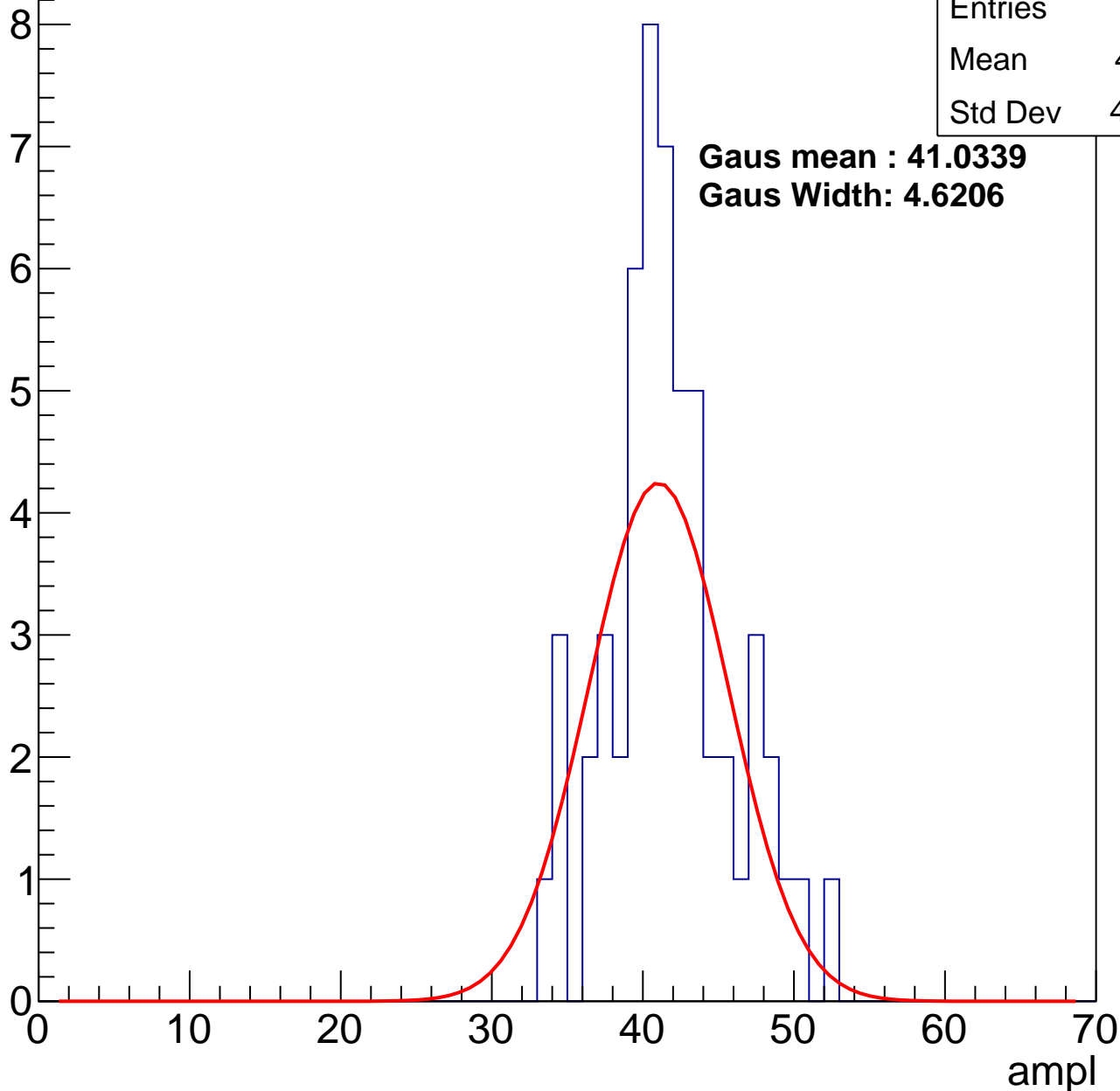
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	55
Mean	41.31
Std Dev	4.103

**Gaus mean : 41.0339**

**Gaus Width: 4.6206**

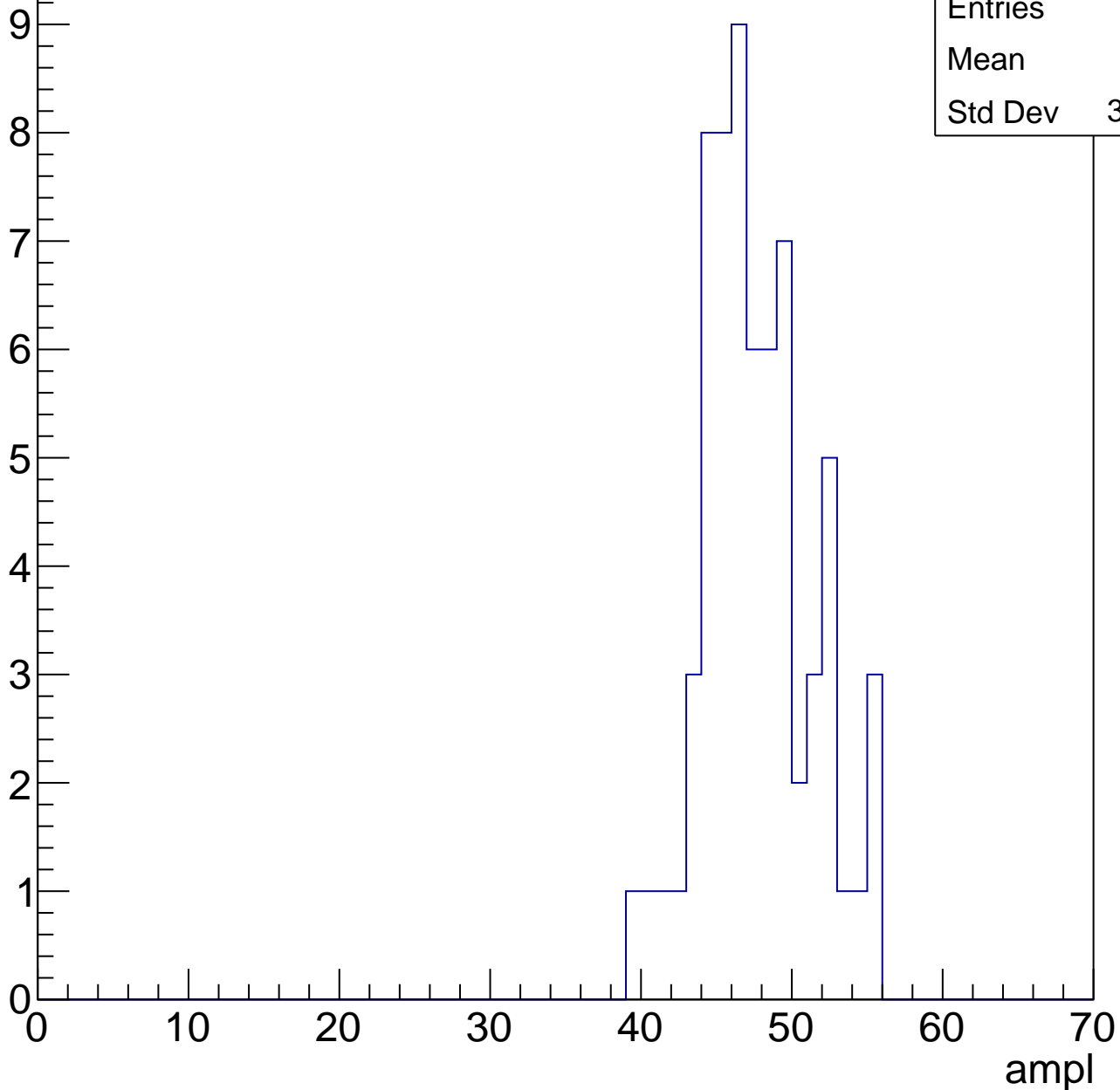


# B1L101S, U19-ch48, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	66
Mean	47.2
Std Dev	3.556

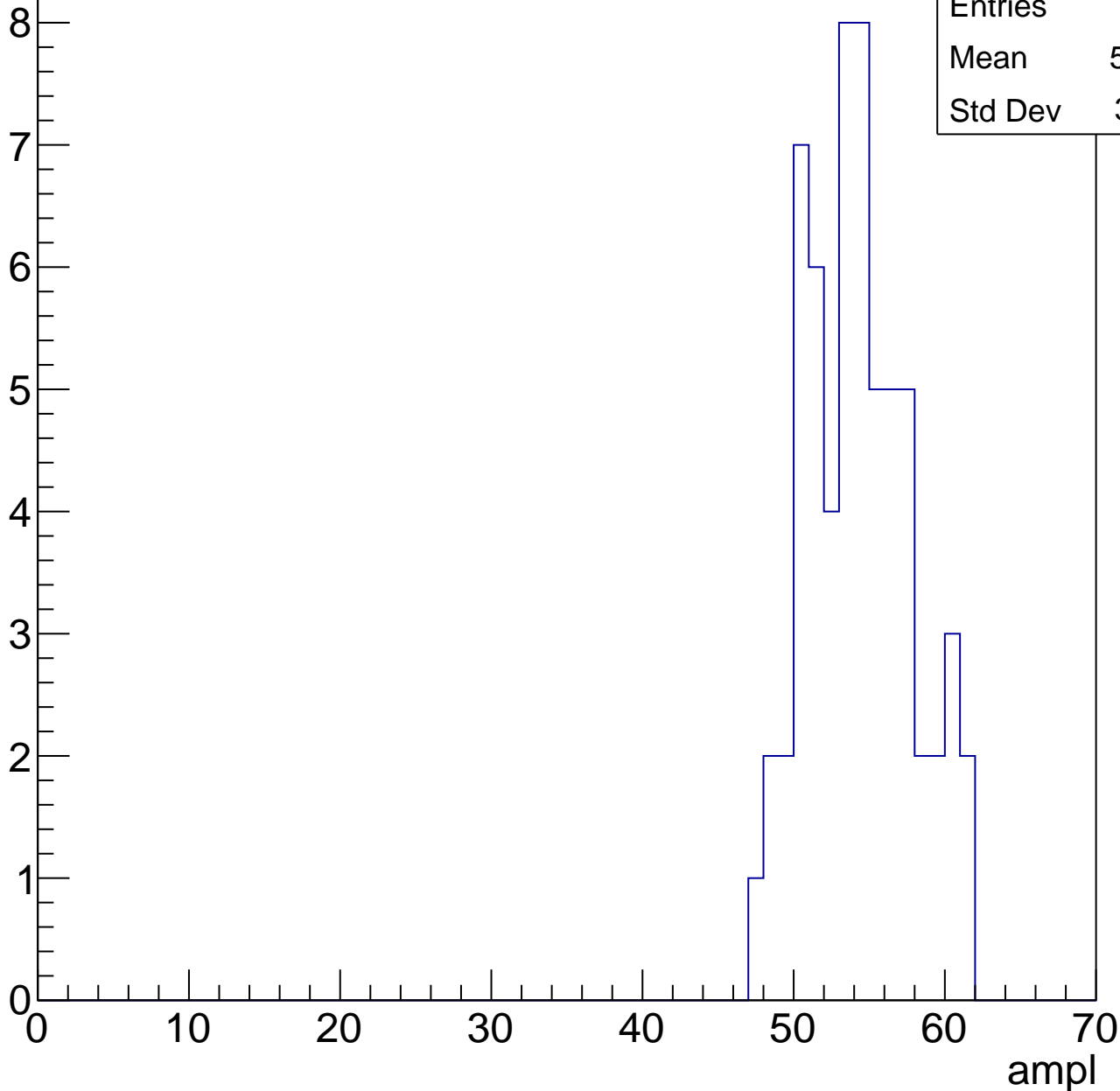


# B1L101S, U19-ch48, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

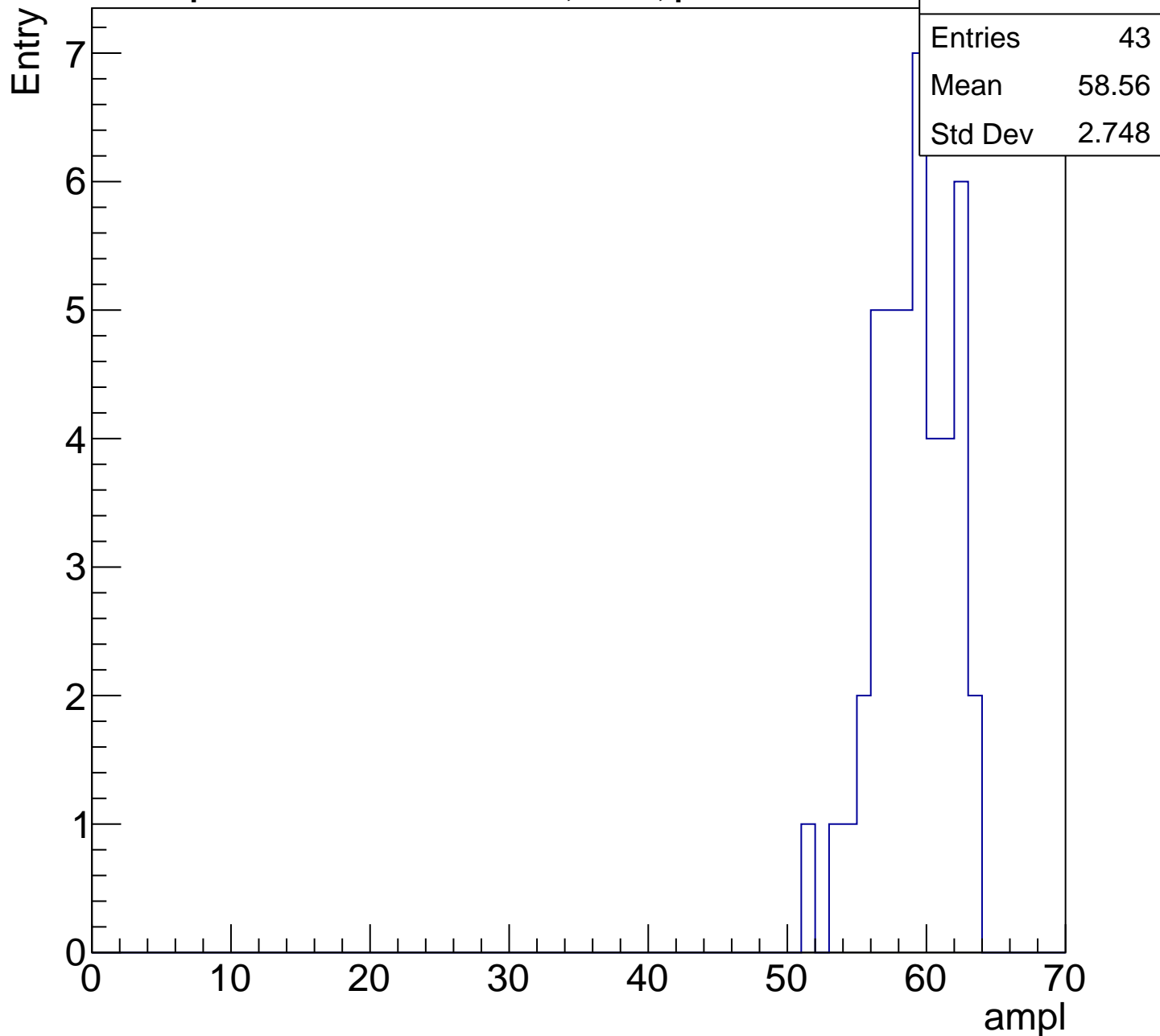
Entry

Entries	62
Mean	53.82
Std Dev	3.401



# B1L101S, U19-ch48, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U19-ch48, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

7

6

5

4

3

2

1

0

Entries

22

Mean

61.18

Std Dev

1.722

ampl

0

10

20

30

40

50

60

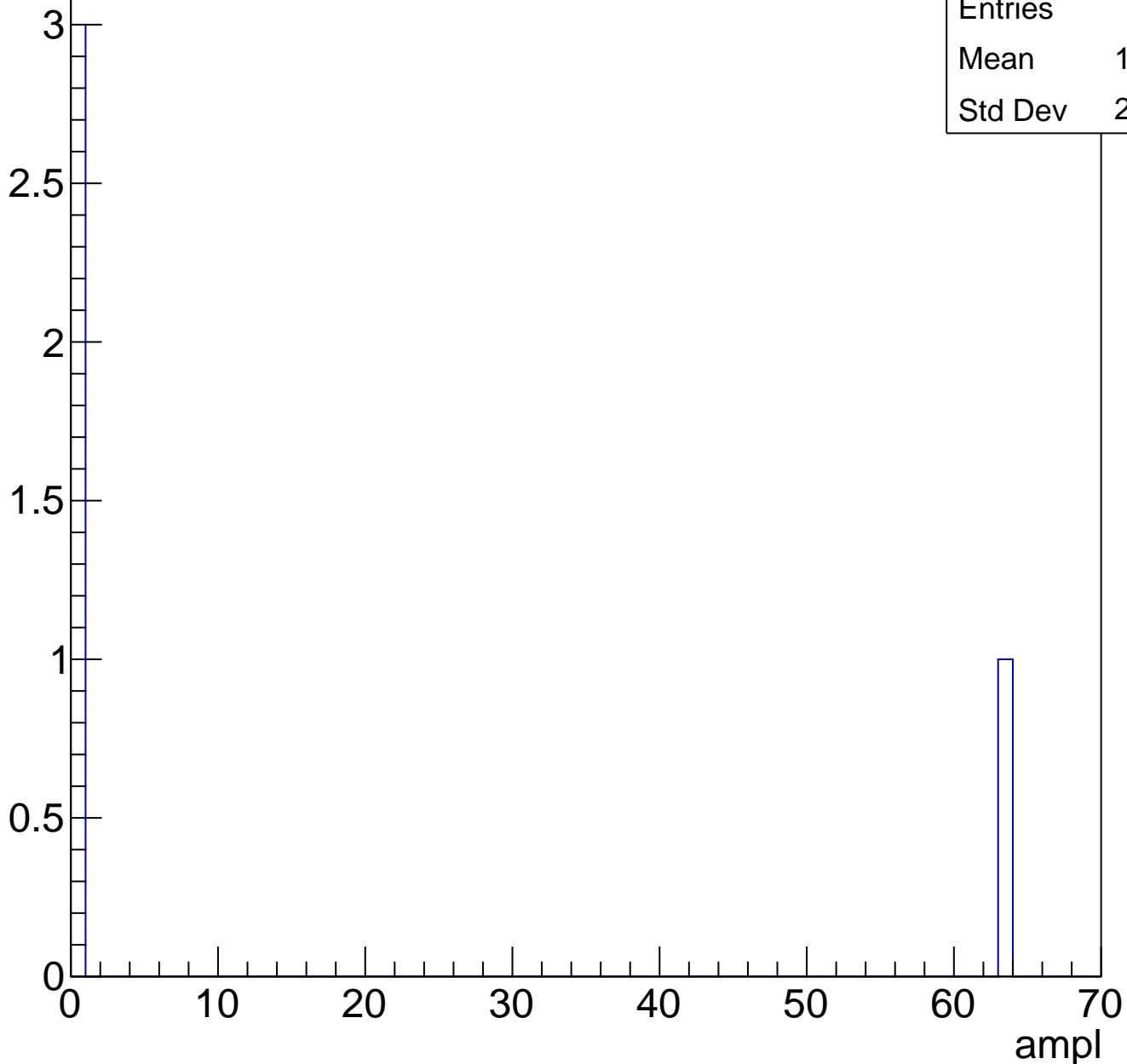
70



# B1L101S, U19-ch48, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U19-ch49, adc0

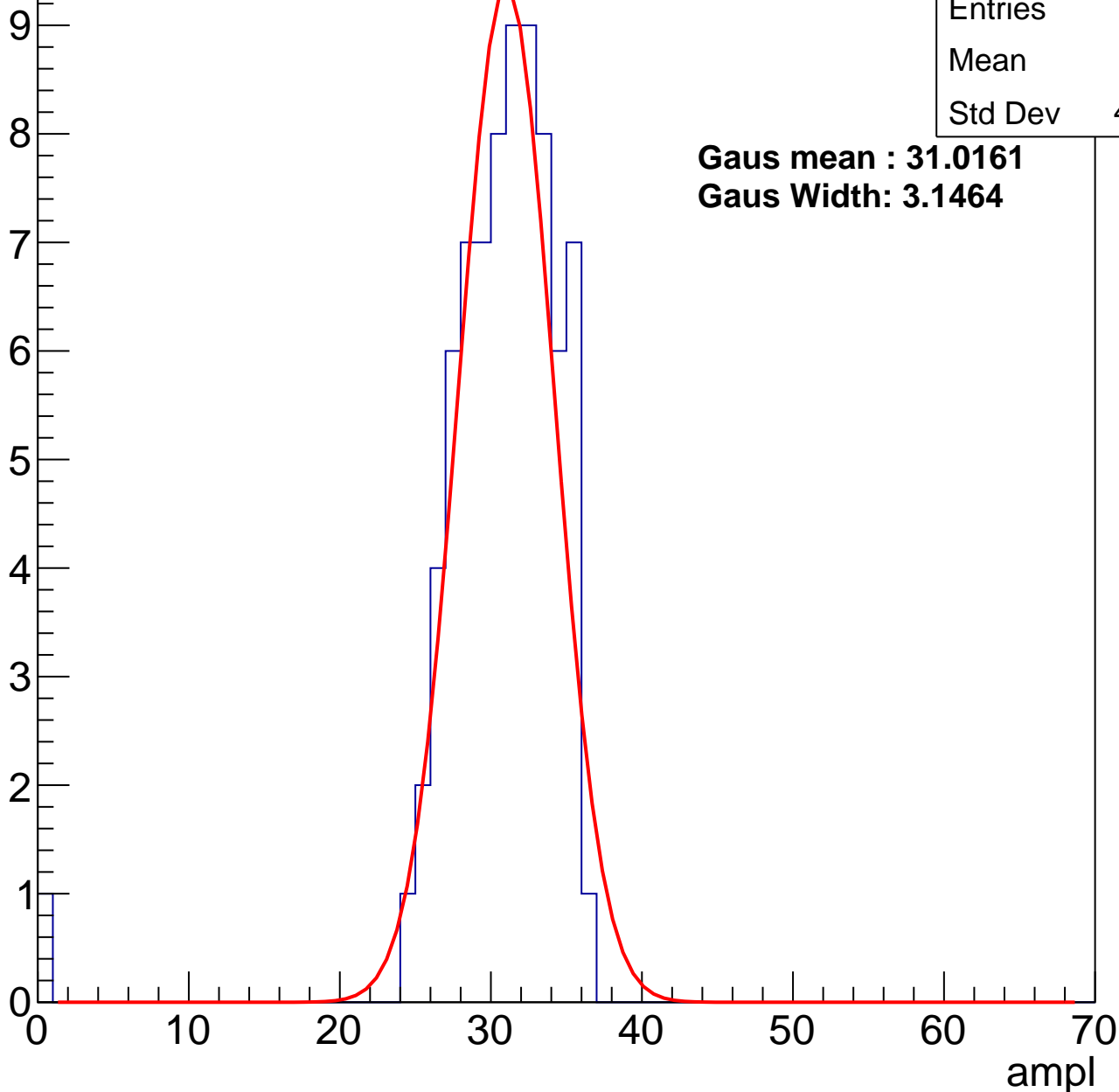
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	76
Mean	30.2
Std Dev	4.531

**Gaus mean : 31.0161**

**Gaus Width: 3.1464**



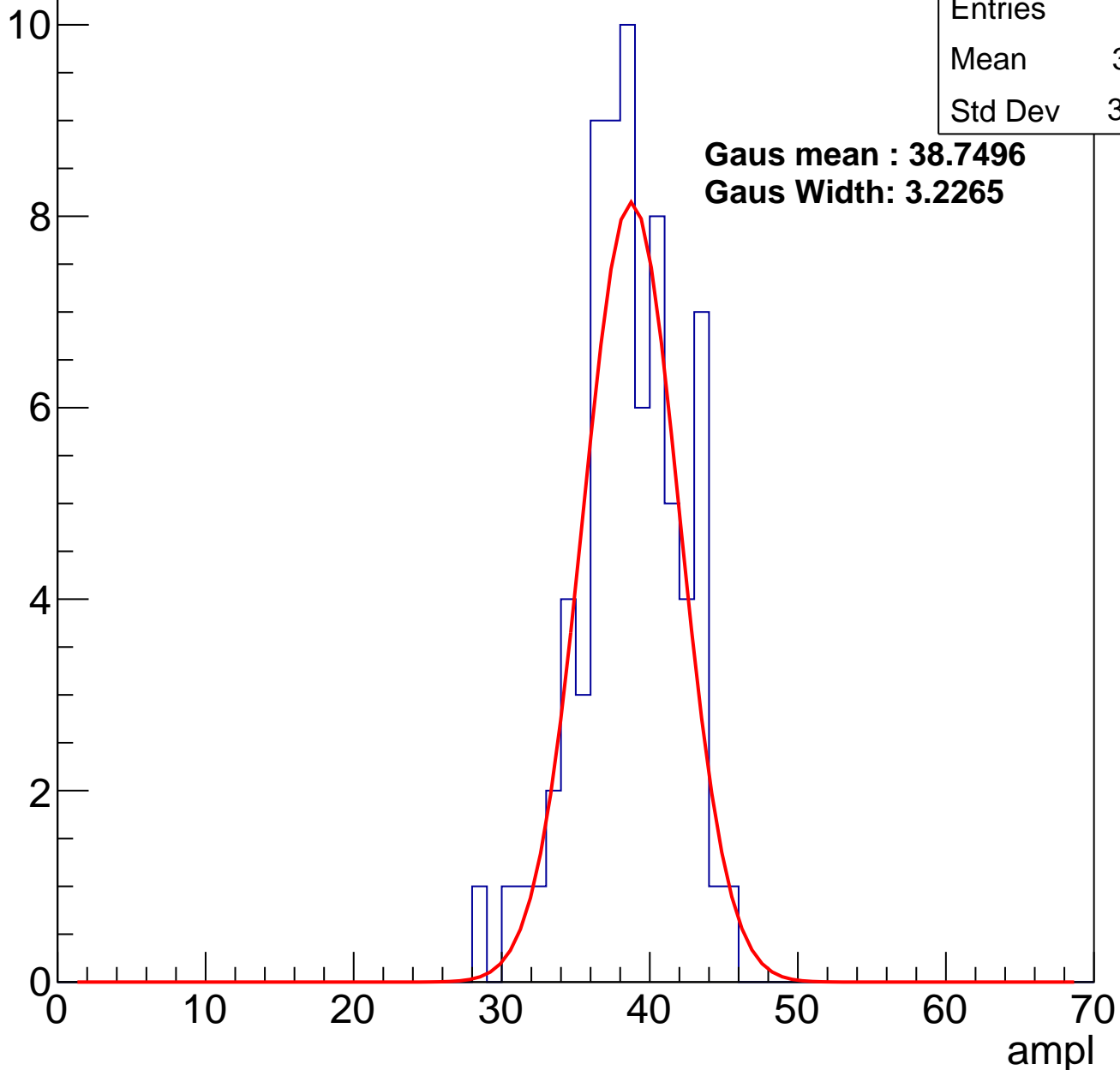
# B1L101S, U19-ch49, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	73
Mean	38.11
Std Dev	3.394

**Gaus mean : 38.7496**  
**Gaus Width: 3.2265**

Entry



# B1L101S, U19-ch49, adc2

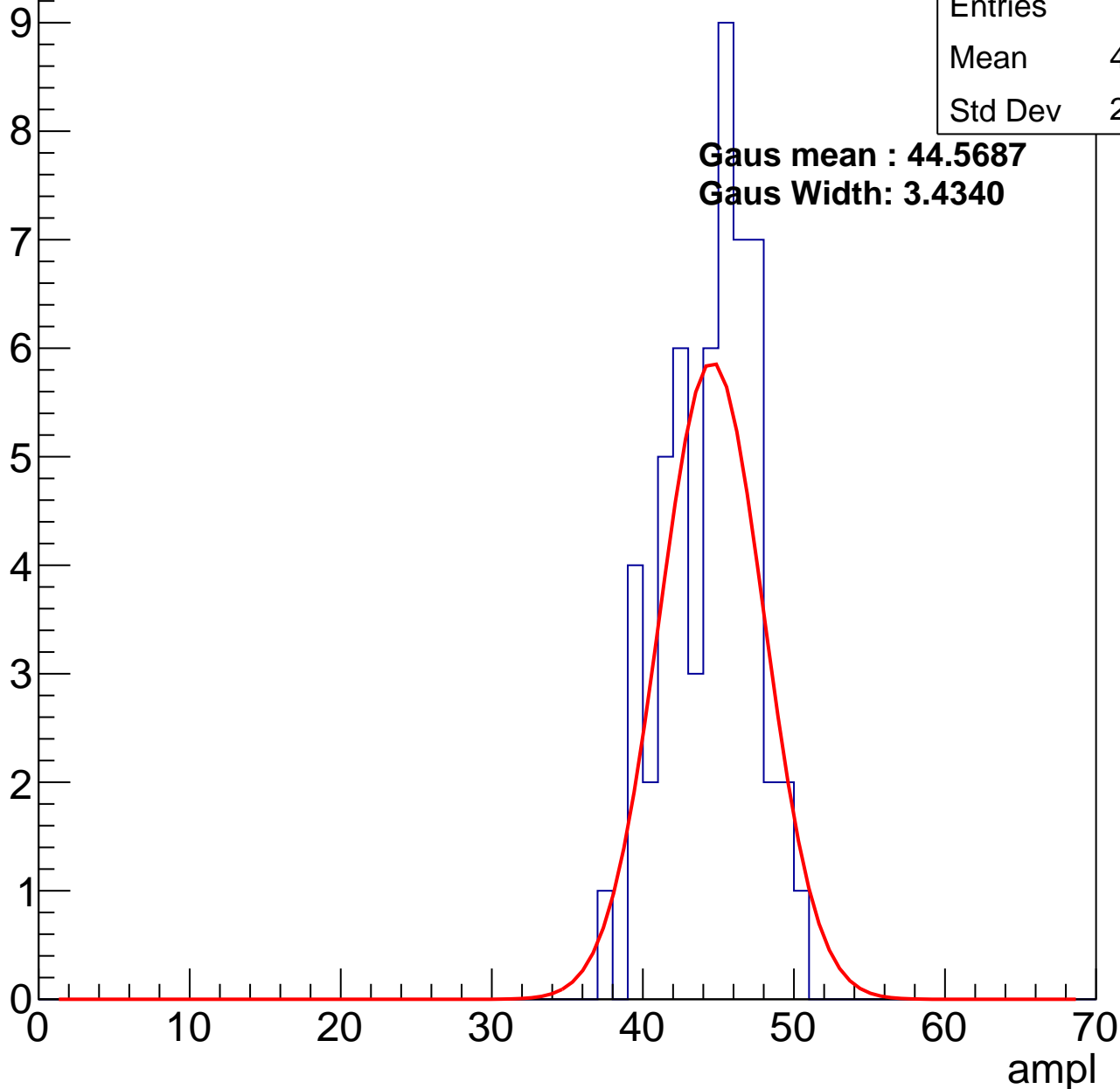
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	55
Mean	44.05
Std Dev	2.926

**Gaus mean : 44.5687**

**Gaus Width: 3.4340**

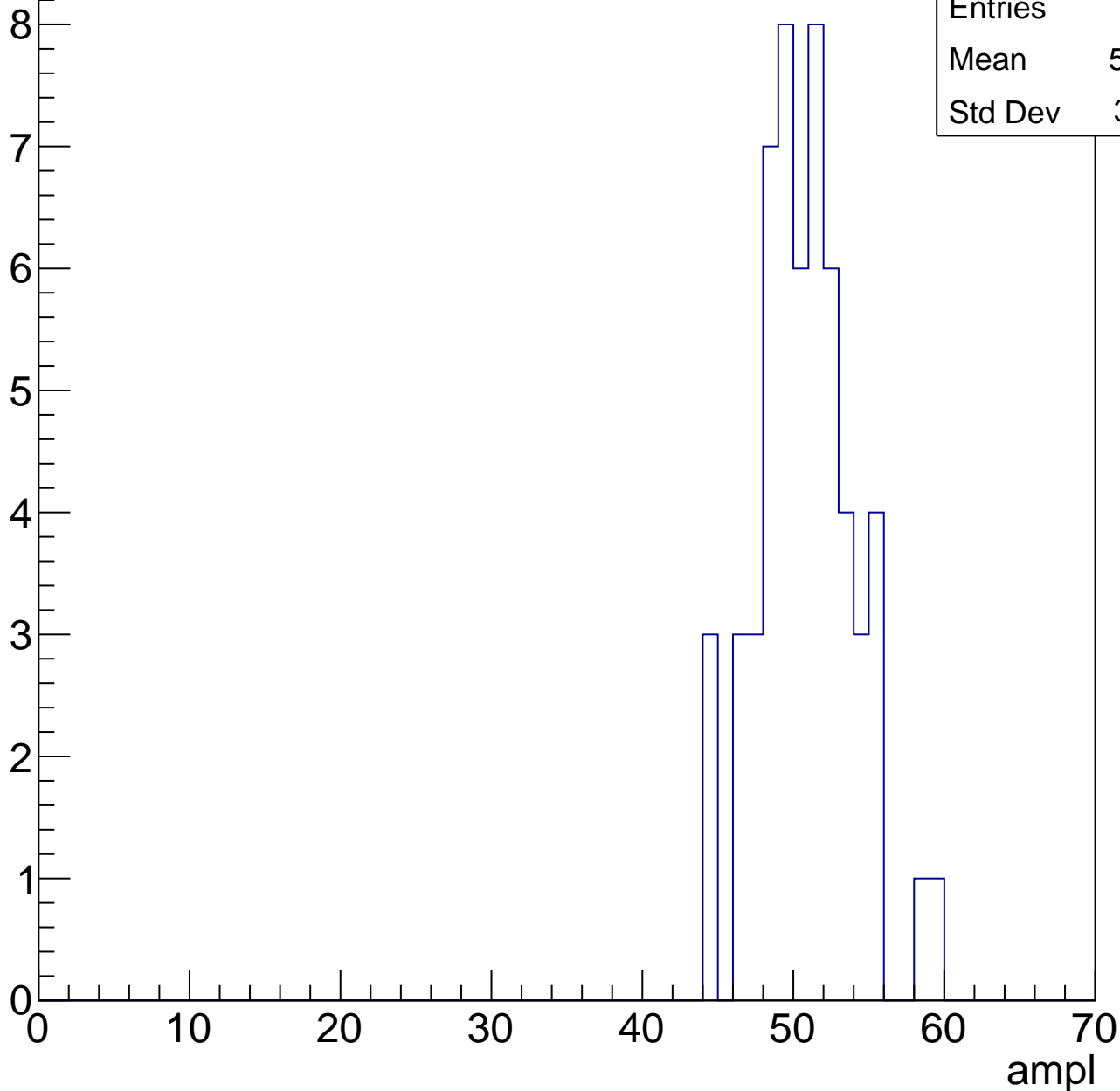


# B1L101S, U19-ch49, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

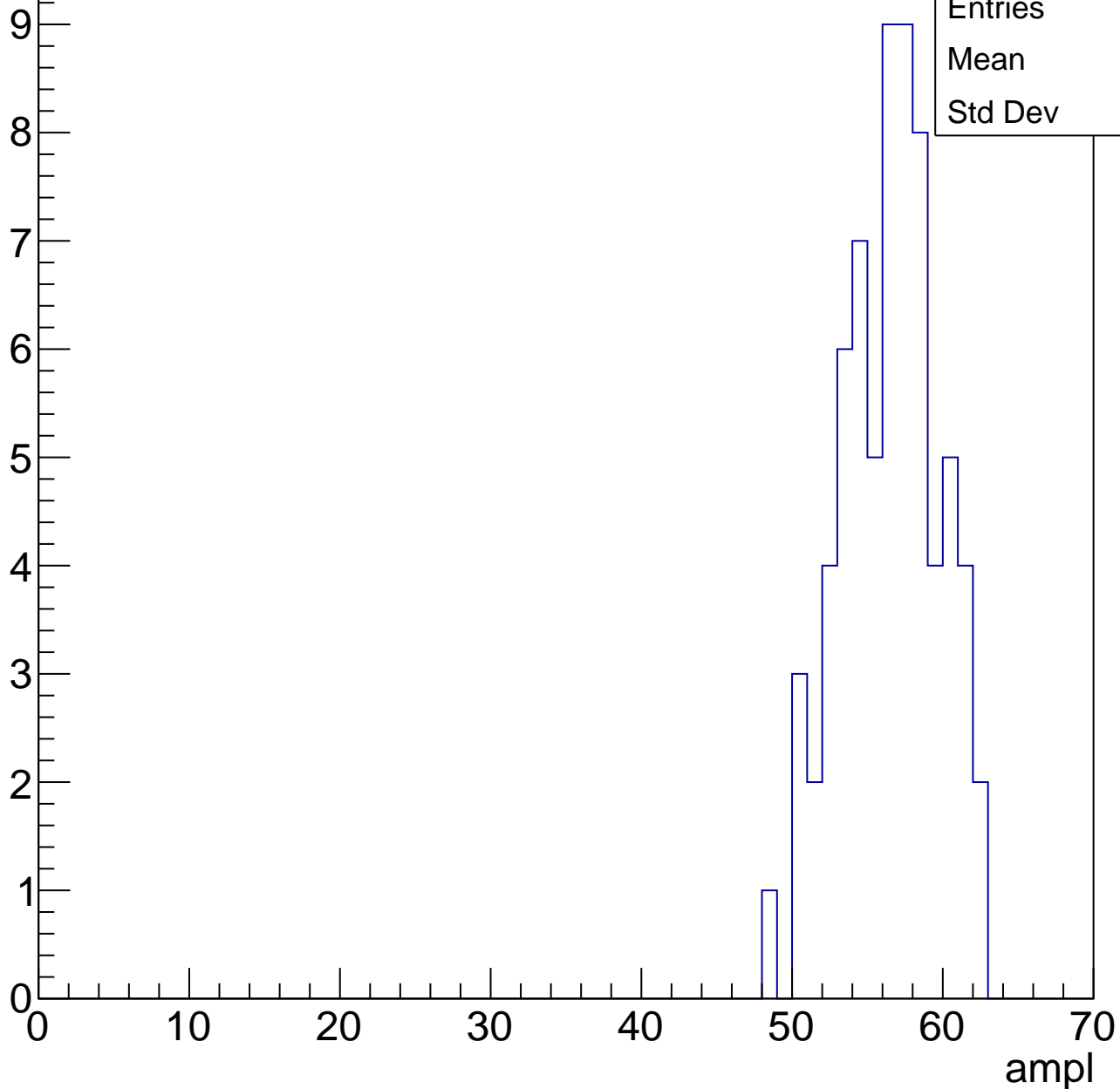
Entries	57
Mean	50.35
Std Dev	3.171



# B1L101S, U19-ch49, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U19-ch49, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

7

6

5

4

3

2

1

0

Entries

35

Mean

58.91

Std Dev

10.3

ampl

0

10

20

30

40

50

60

70

# B1L101S, U19-ch49, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U19-ch49, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L101S, U19-ch50, adc0

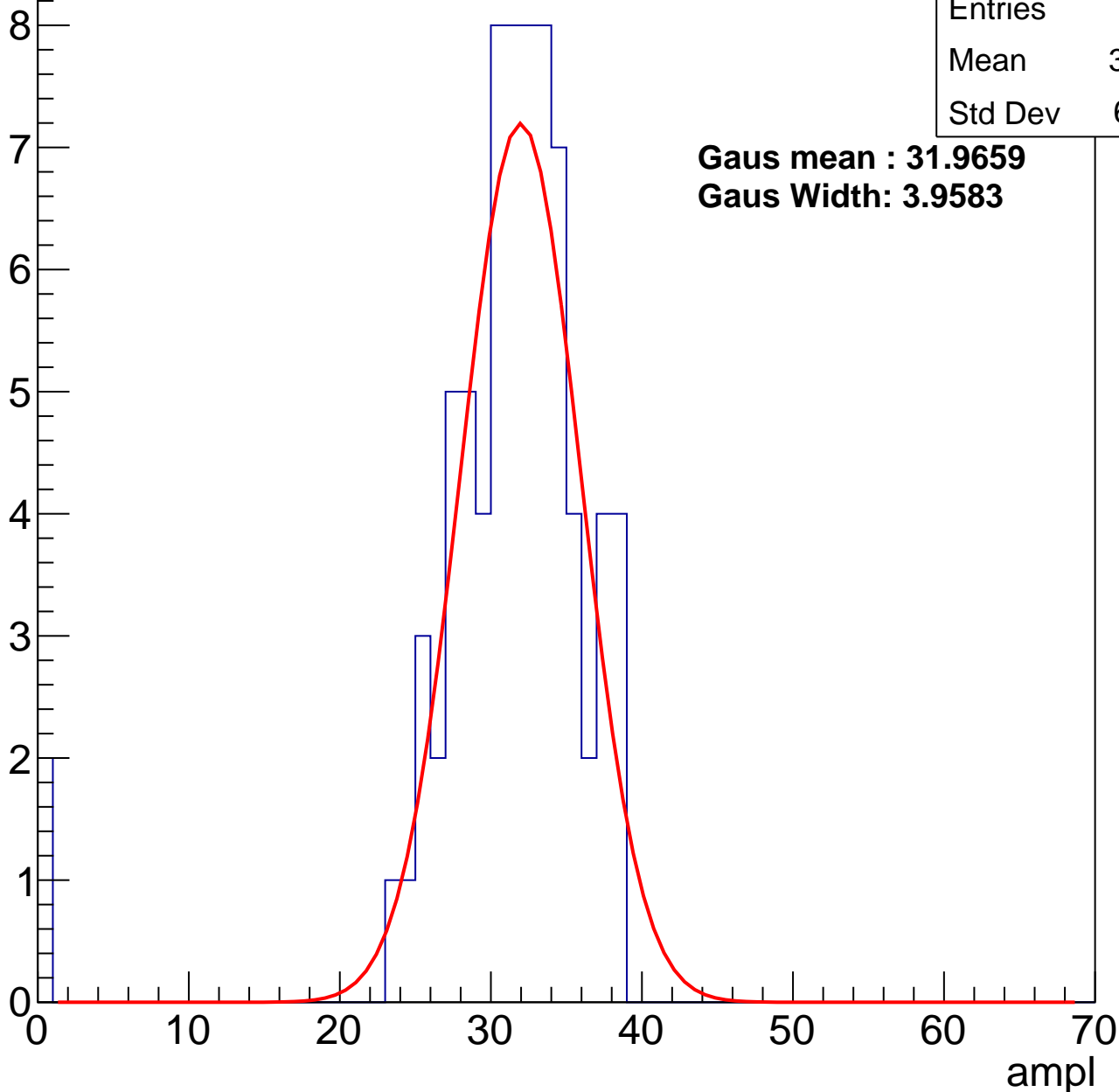
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	76
Mean	30.57
Std Dev	6.161

**Gaus mean : 31.9659**

**Gaus Width: 3.9583**



# B1L101S, U19-ch50, adc1

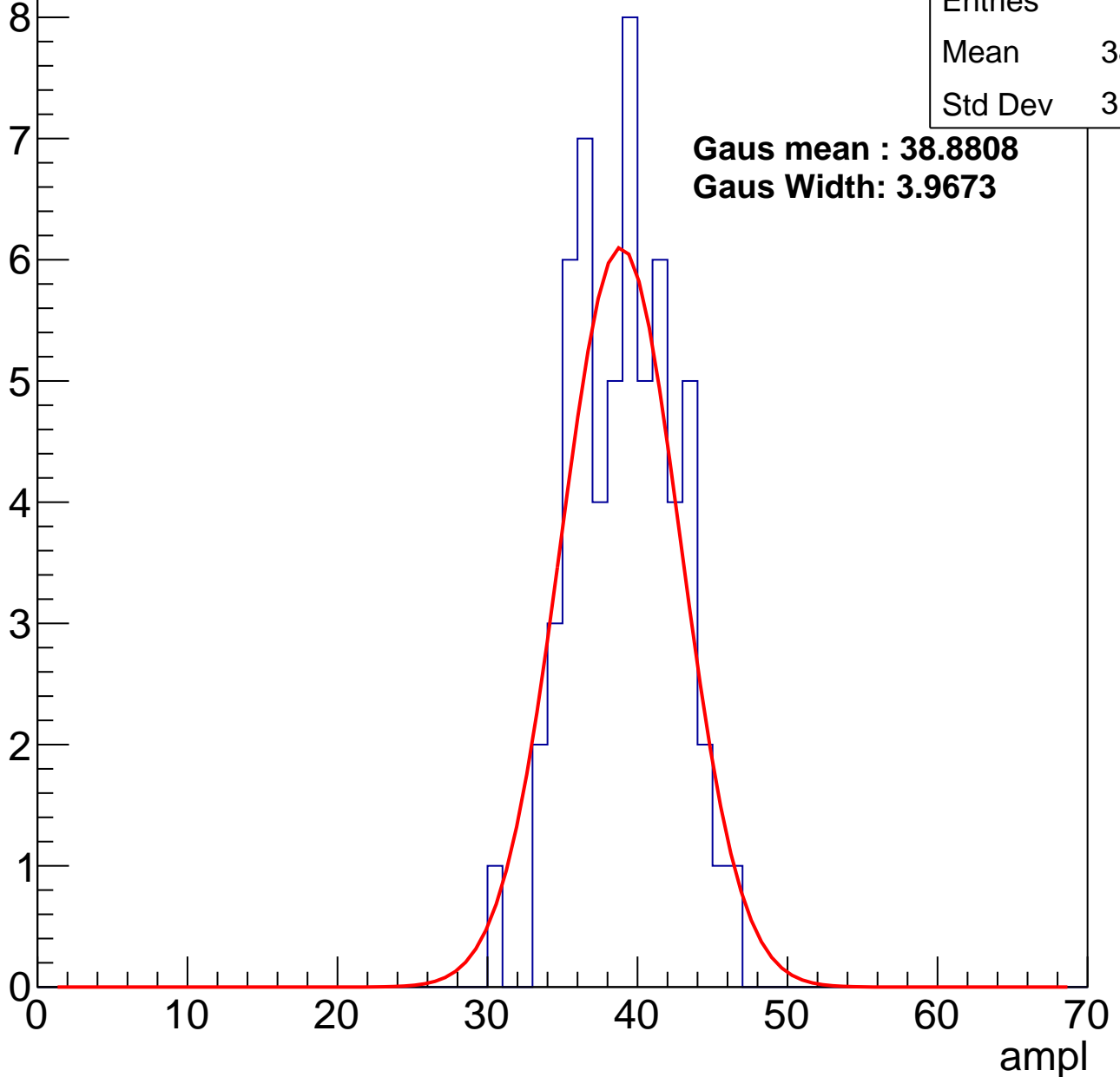
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	60
Mean	38.63
Std Dev	3.366

**Gaus mean : 38.8808**

**Gaus Width: 3.9673**



# B1L101S, U19-ch50, adc2

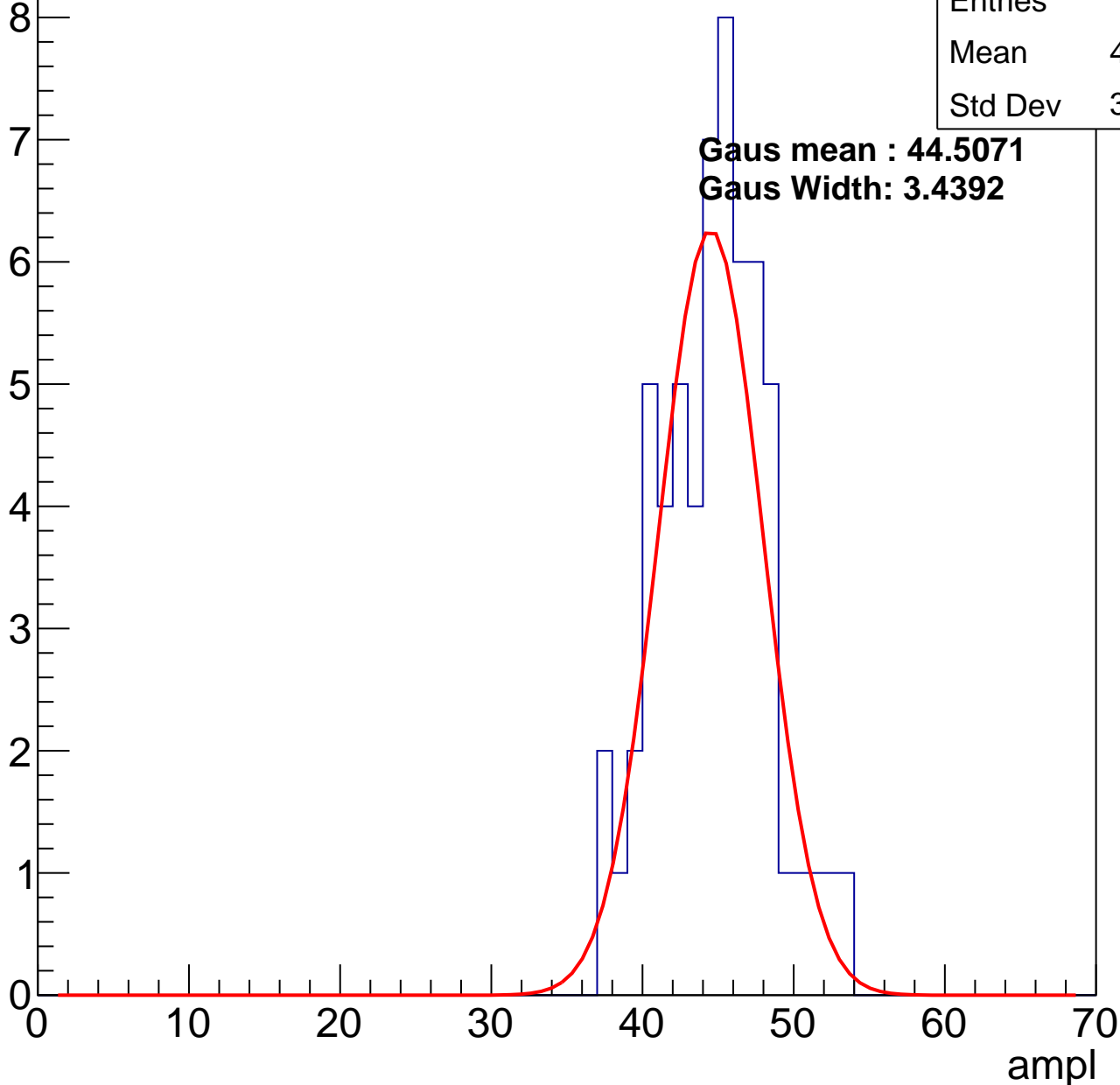
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	60
Mean	44.28
Std Dev	3.512

**Gaus mean : 44.5071**

**Gaus Width: 3.4392**

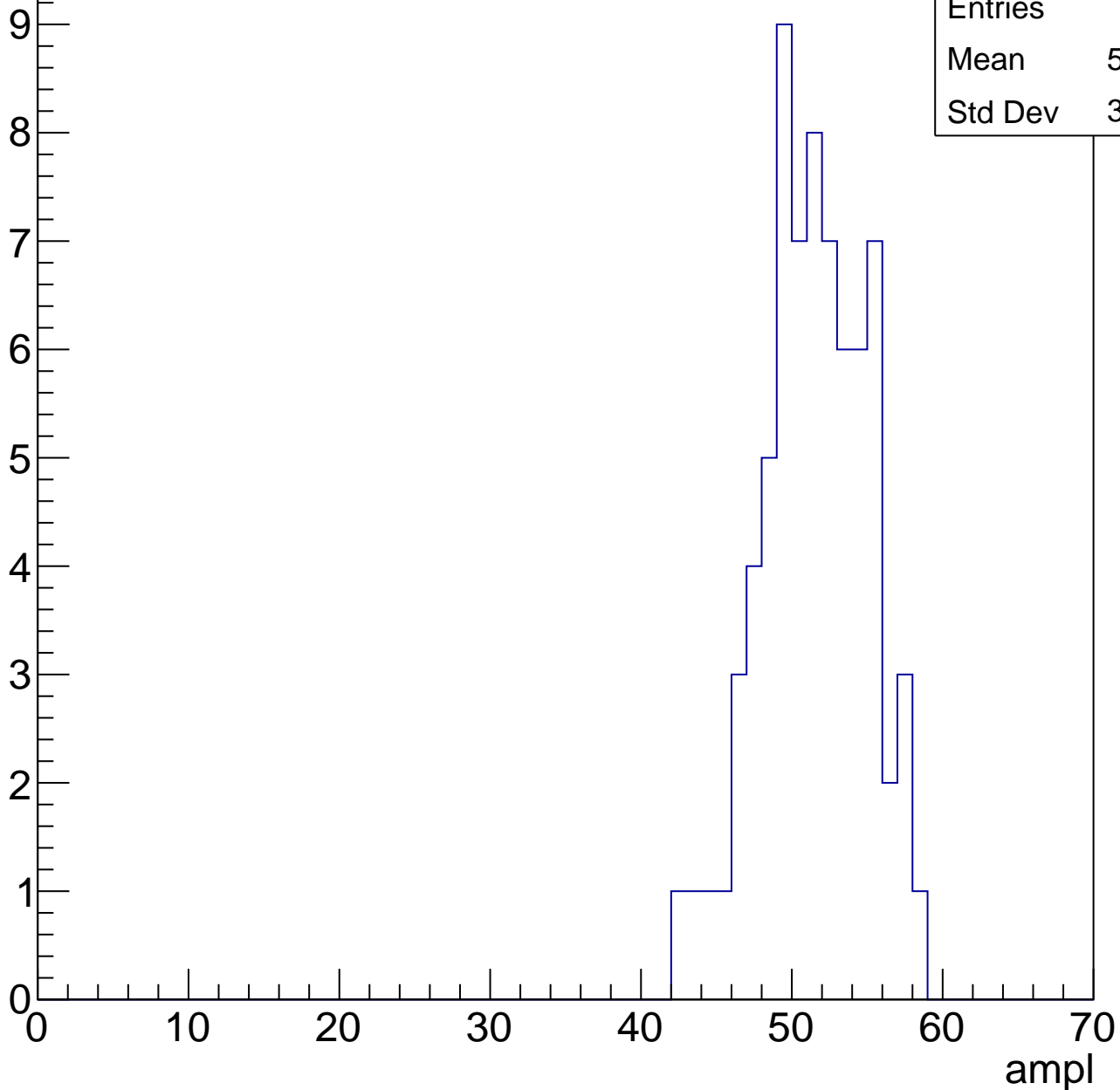


# B1L101S, U19-ch50, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

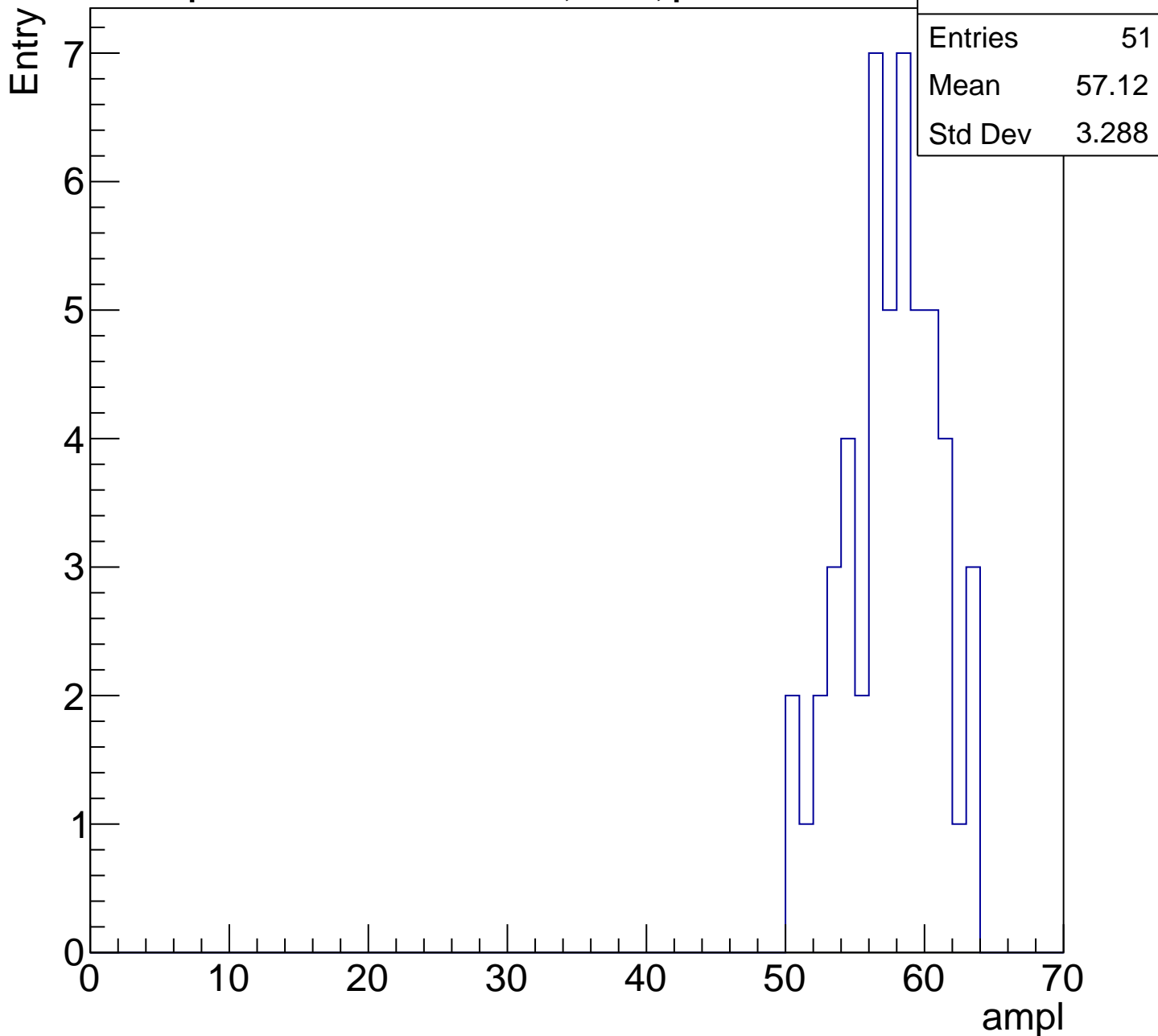
Entry

Entries	72
Mean	50.99
Std Dev	3.458



# B1L101S, U19-ch50, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U19-ch50, adc5

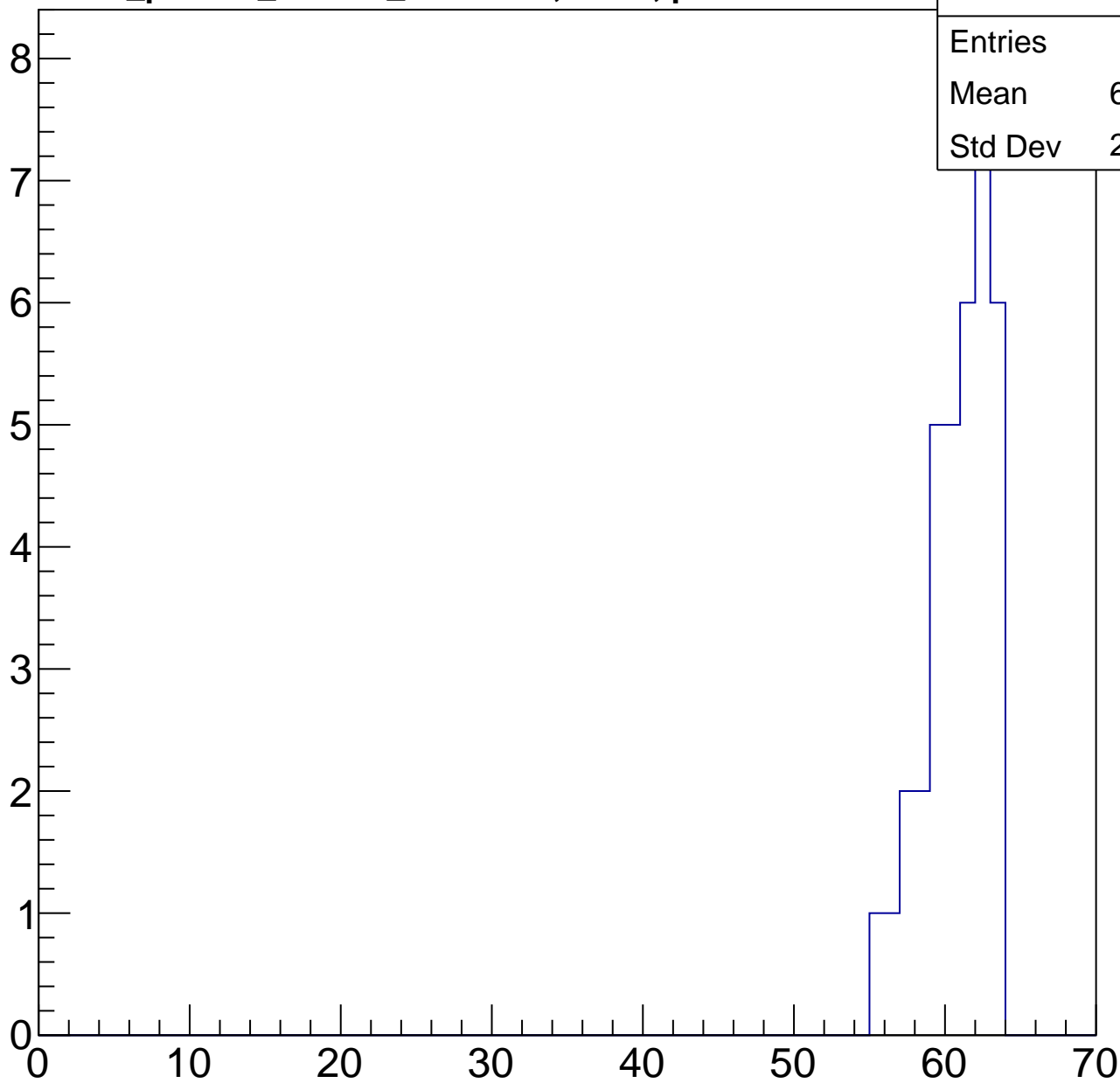
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	36
Mean	60.44
Std Dev	2.088

ampl



# B1L101S, U19-ch50, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U19-ch50, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U19-ch51, adc0

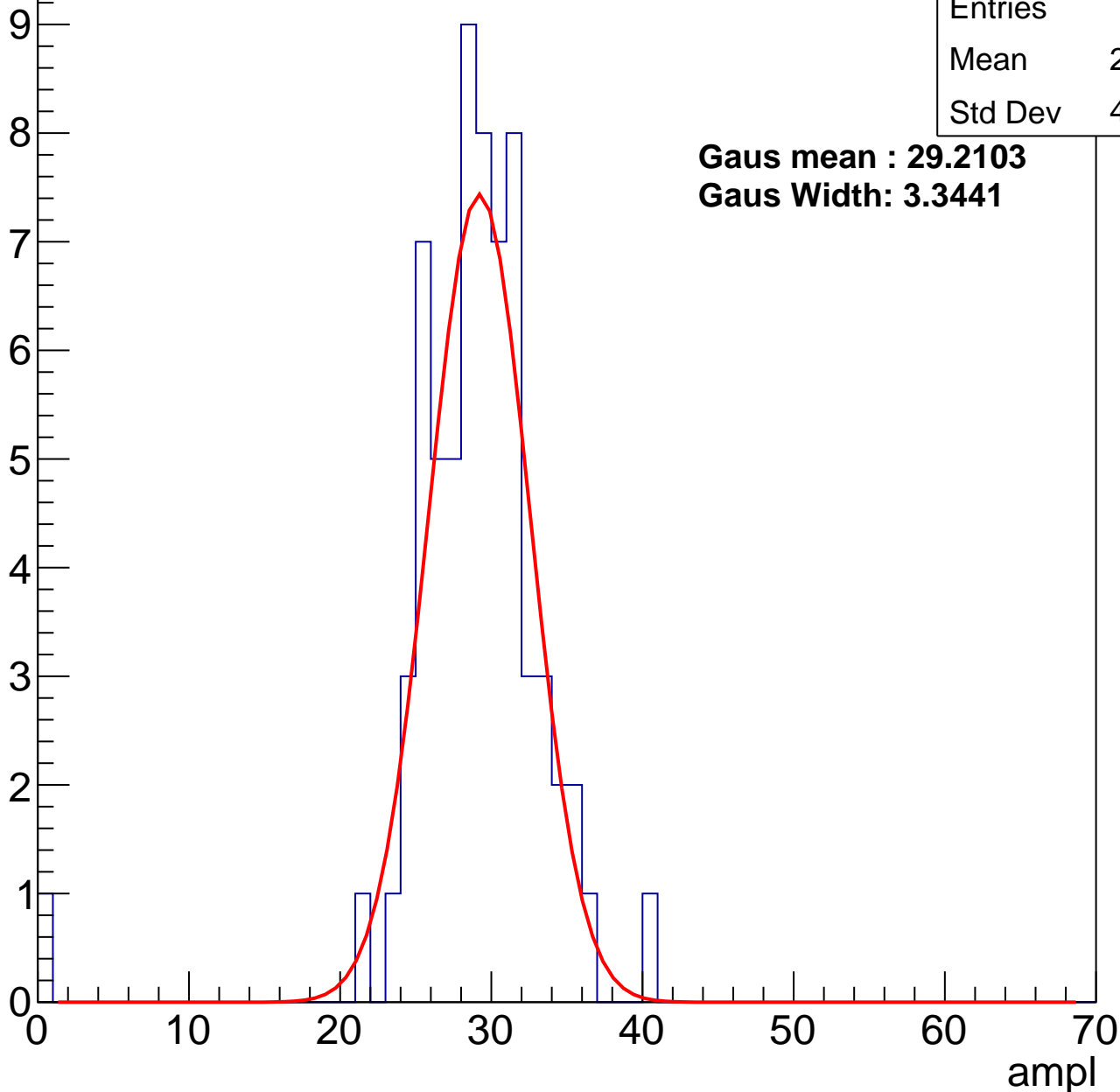
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	67
Mean	28.46
Std Dev	4.869

**Gaus mean : 29.2103**

**Gaus Width: 3.3441**



# B1L101S, U19-ch51, adc1

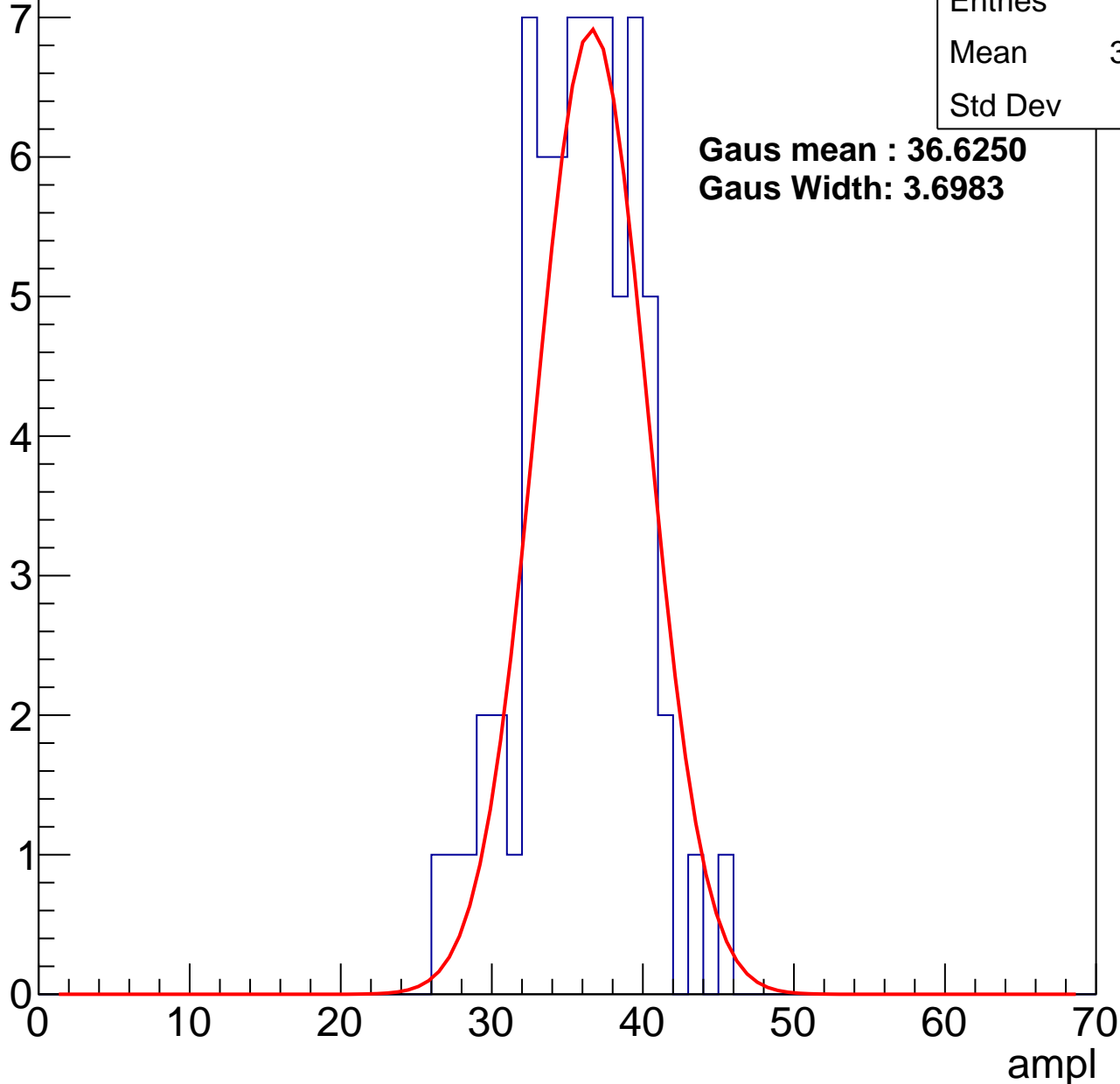
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	35.43
Std Dev	3.74

**Gaus mean : 36.6250**

**Gaus Width: 3.6983**



# B1L101S, U19-ch51, adc2

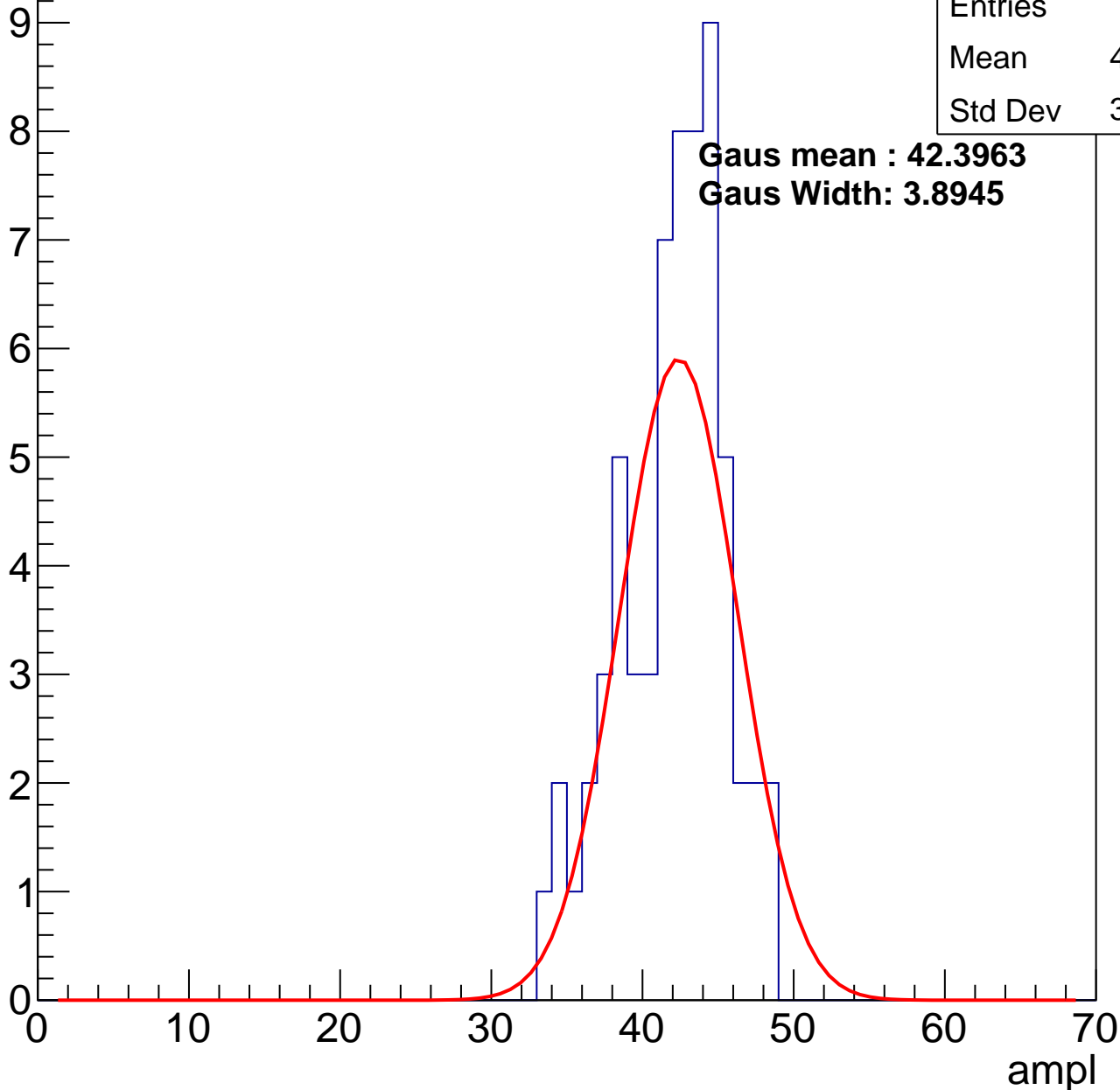
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	41.52
Std Dev	3.473

**Gaus mean : 42.3963**

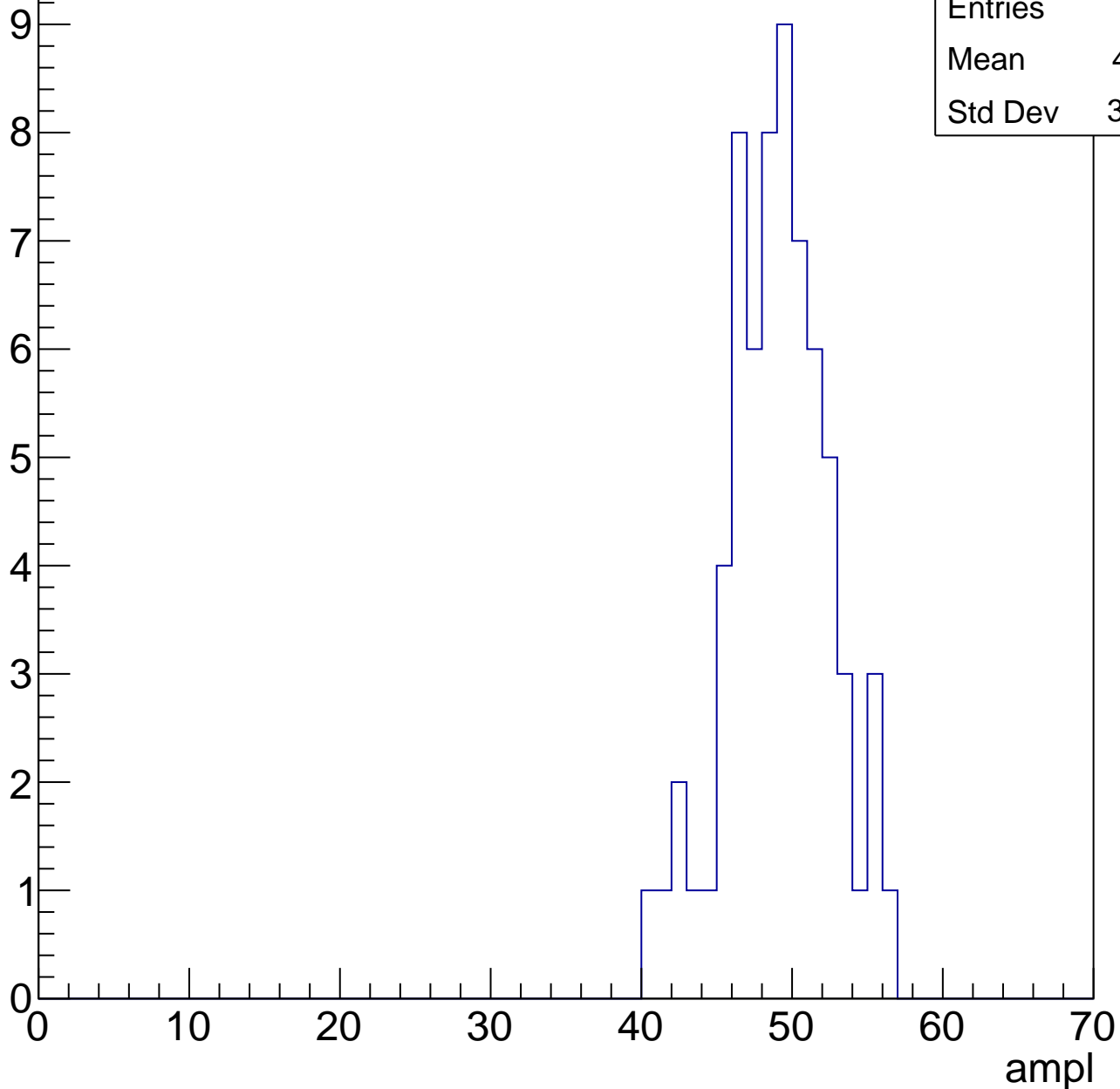
**Gaus Width: 3.8945**



# B1L101S, U19-ch51, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



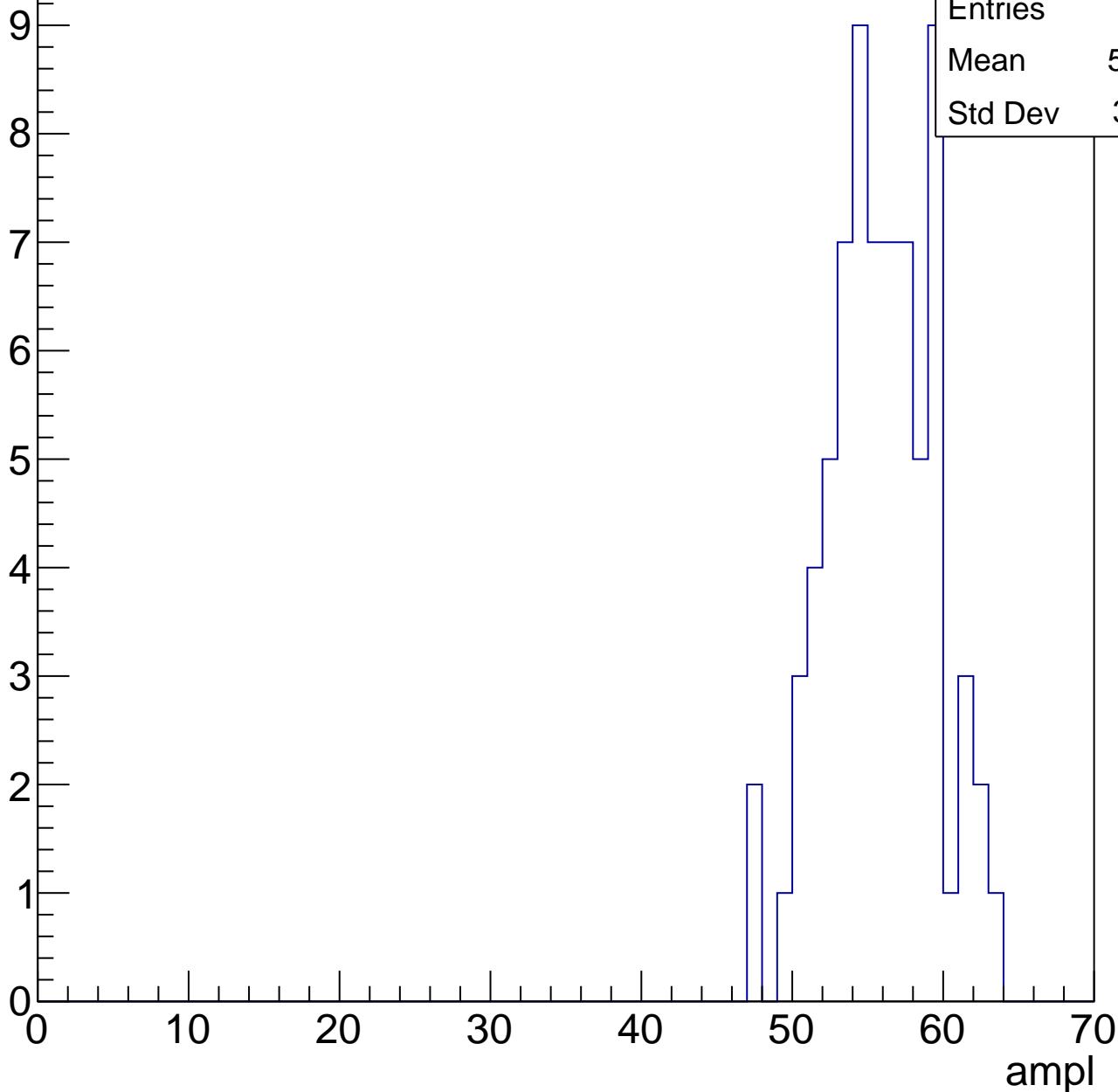
Entries	67
Mean	48.61
Std Dev	3.385

# B1L101S, U19-ch51, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	73
Mean	55.36
Std Dev	3.501



# B1L101S, U19-ch51, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

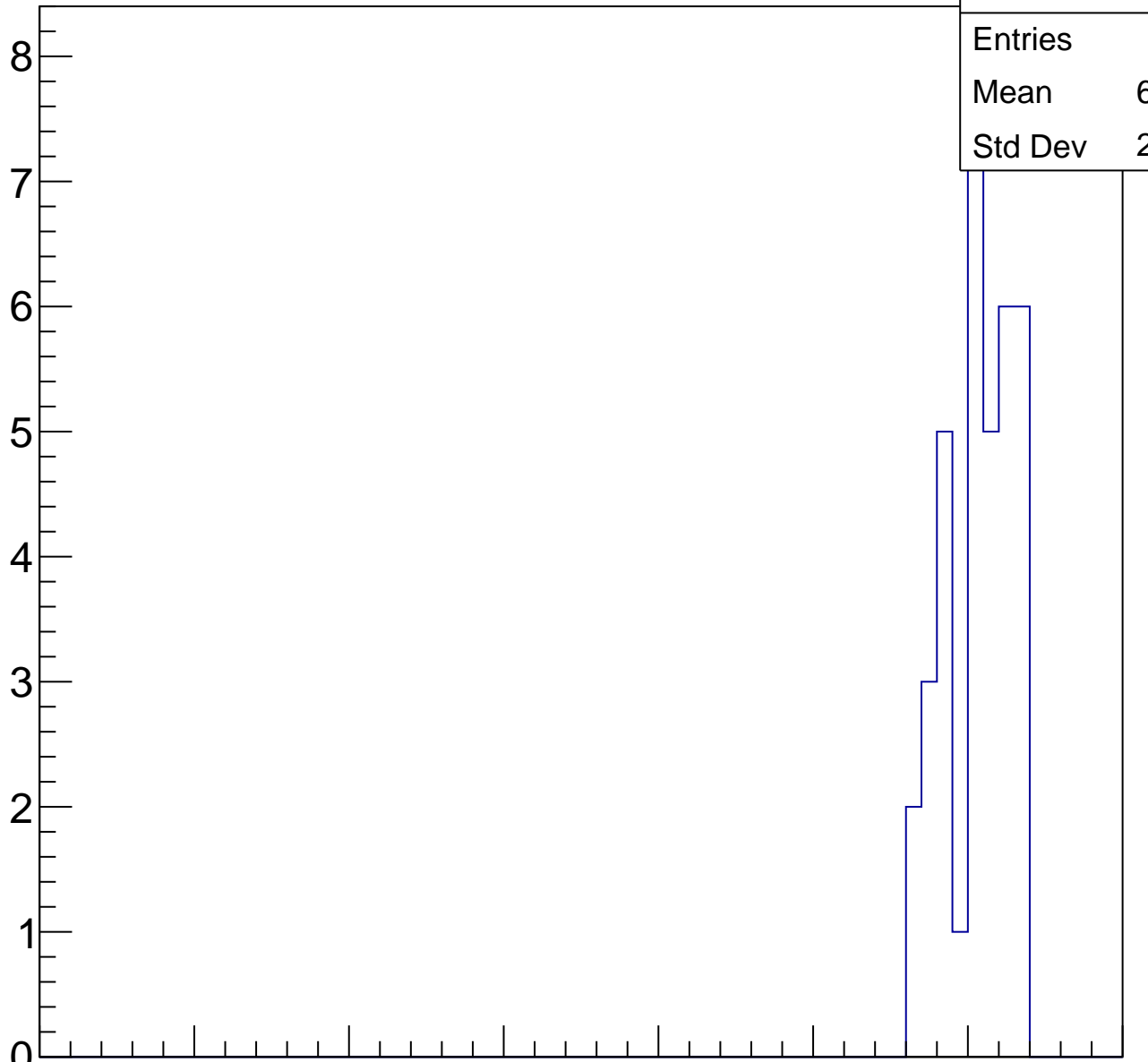
Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	36
Mean	60.19
Std Dev	2.119

ampl

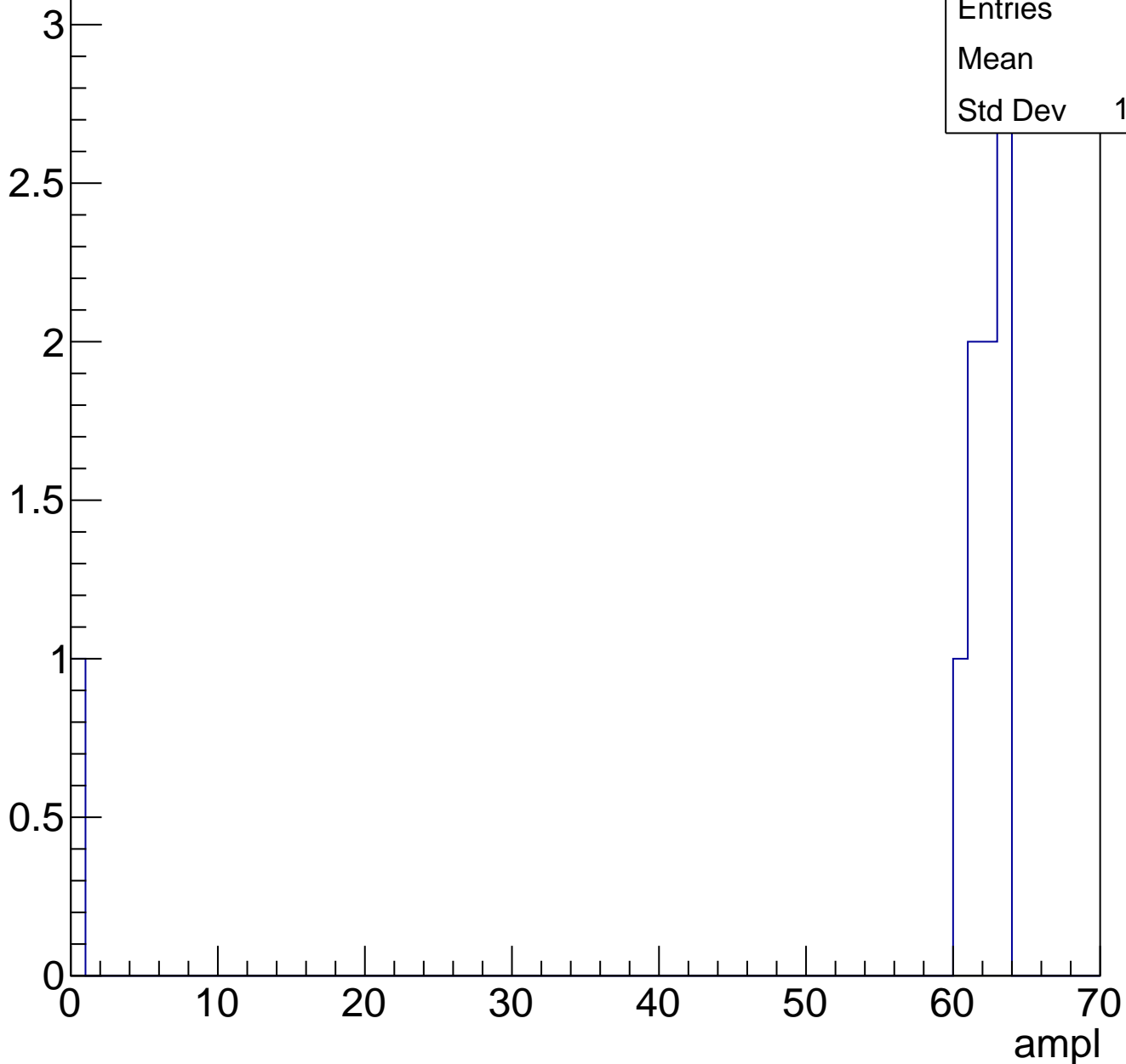
0 10 20 30 40 50 60 70



# B1L101S, U19-ch51, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U19-ch51, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L101S, U19-ch52, adc0

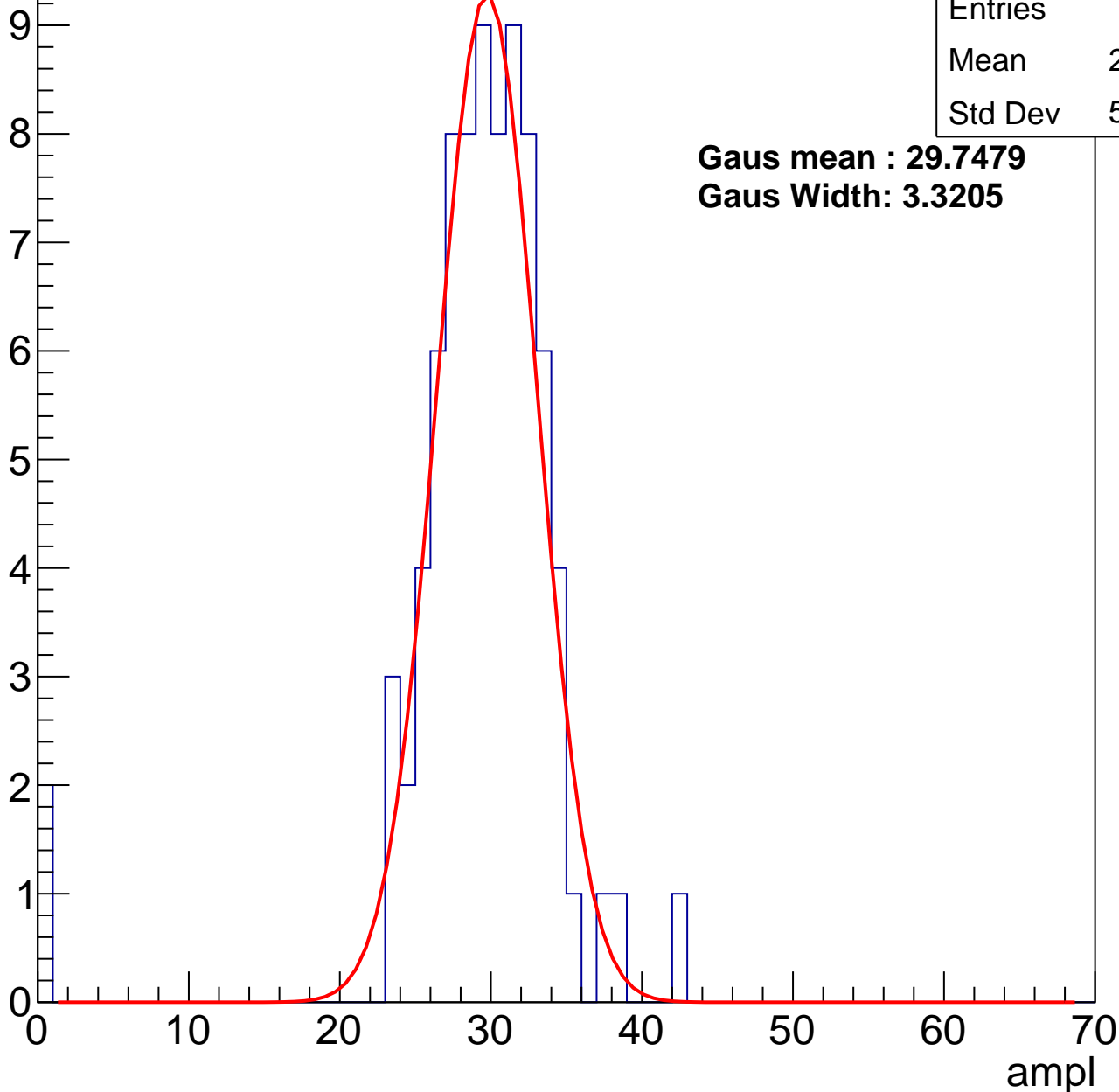
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	81
Mean	28.83
Std Dev	5.728

**Gaus mean : 29.7479**

**Gaus Width: 3.3205**



# B1L101S, U19-ch52, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	69
Mean	37.09
Std Dev	3.391

**Gaus mean : 37.5497**

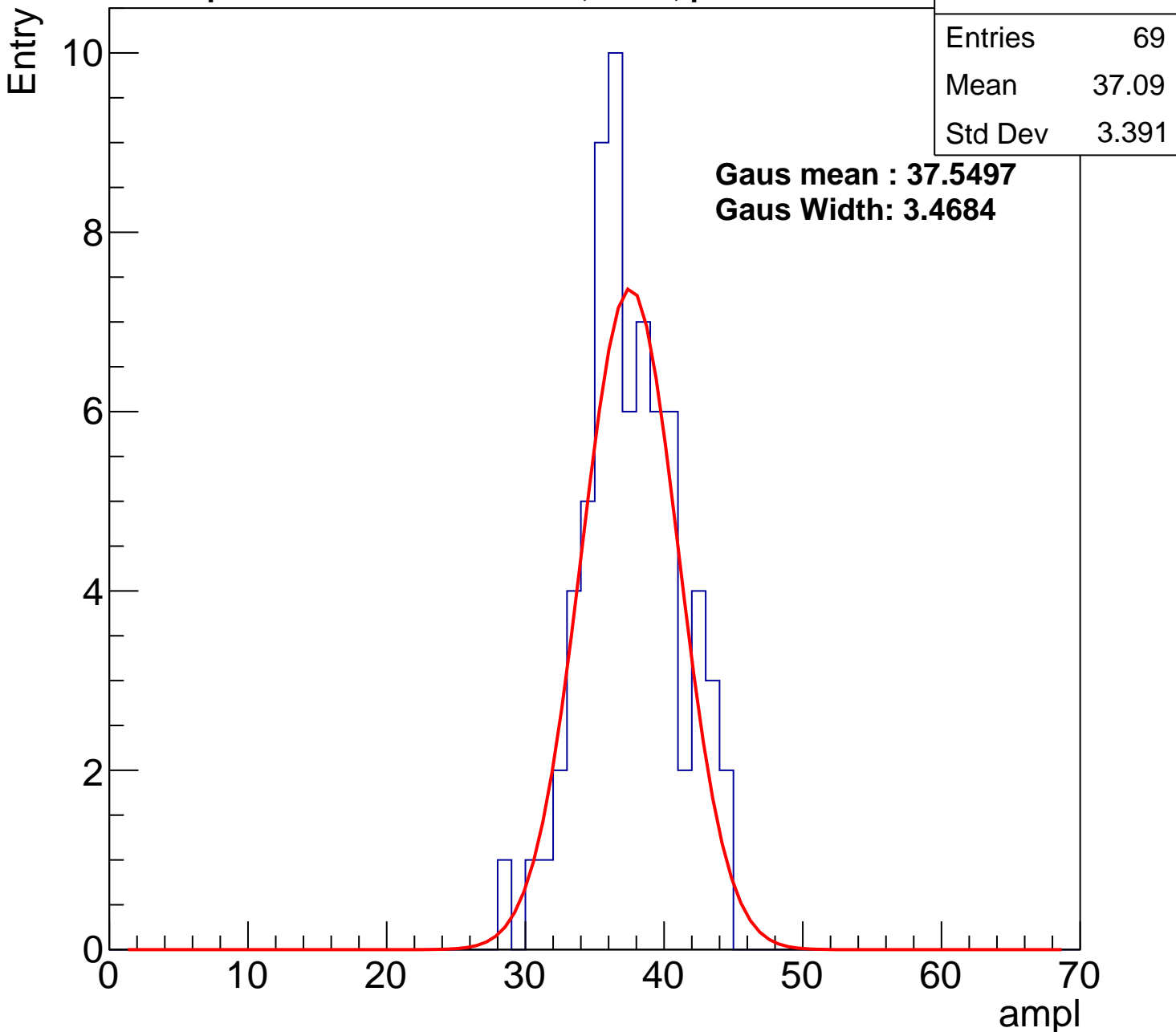
**Gaus Width: 3.4684**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U19-ch52, adc2

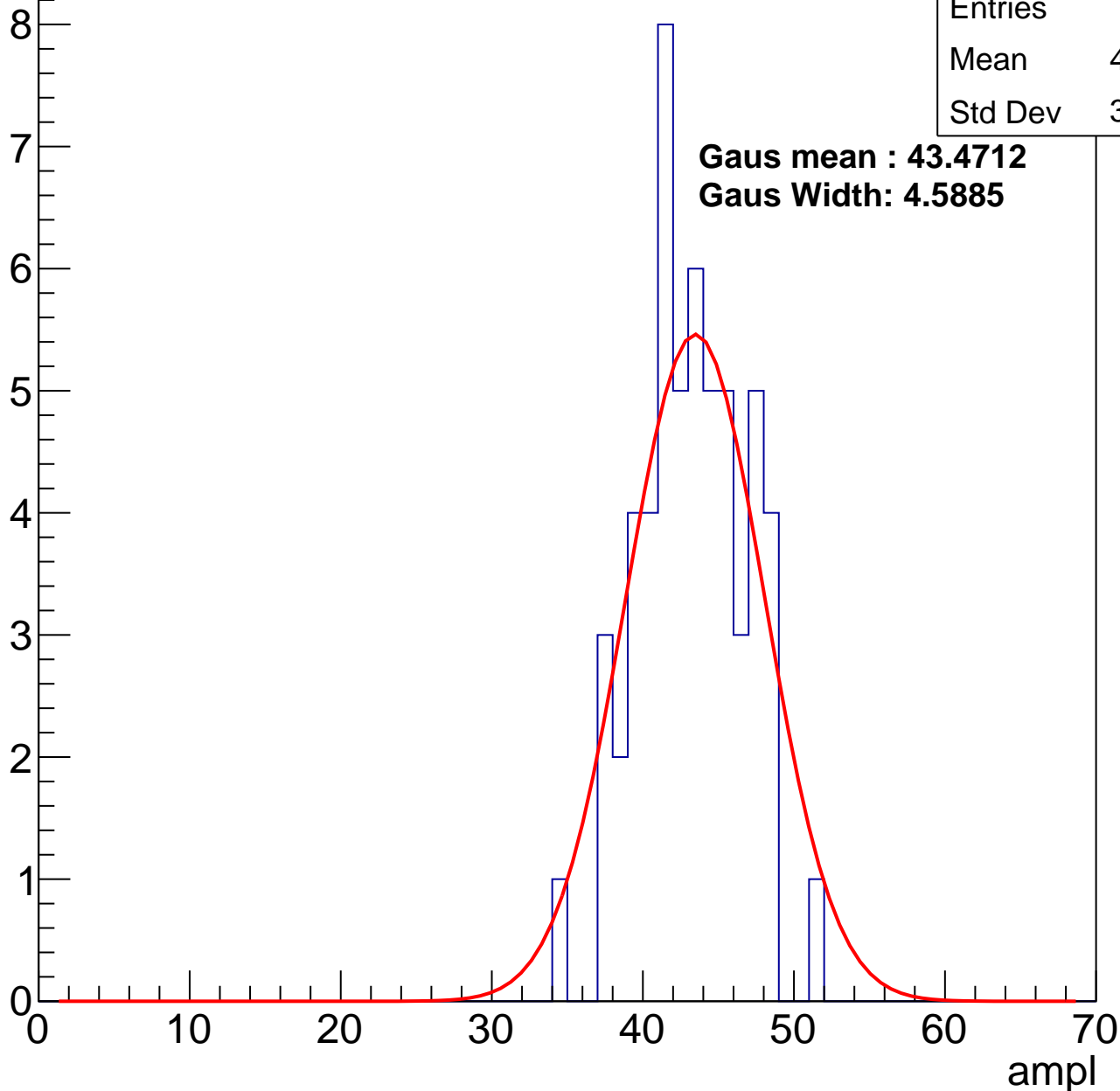
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	56
Mean	42.75
Std Dev	3.455

**Gaus mean : 43.4712**

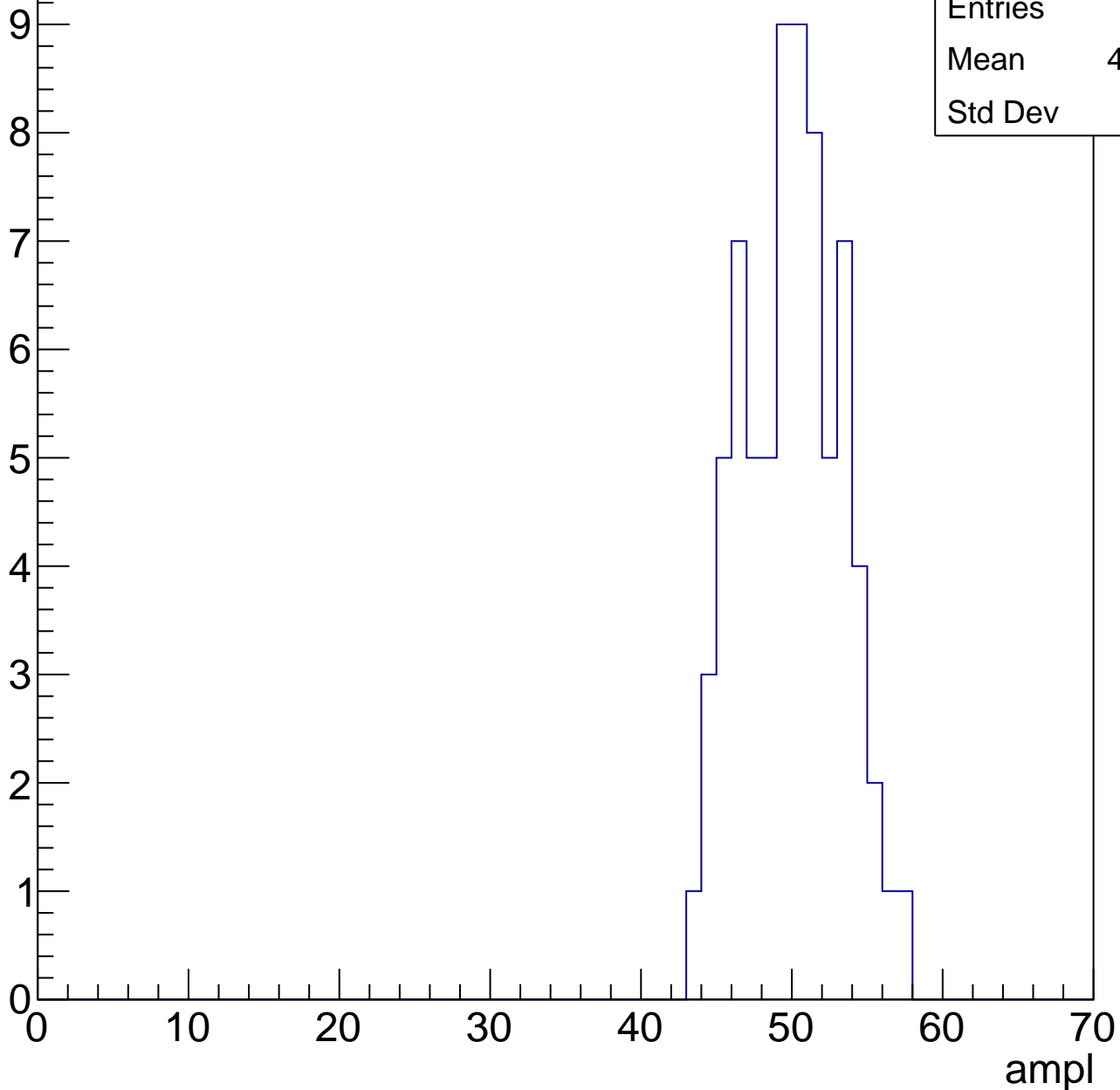
**Gaus Width: 4.5885**



# B1L101S, U19-ch52, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



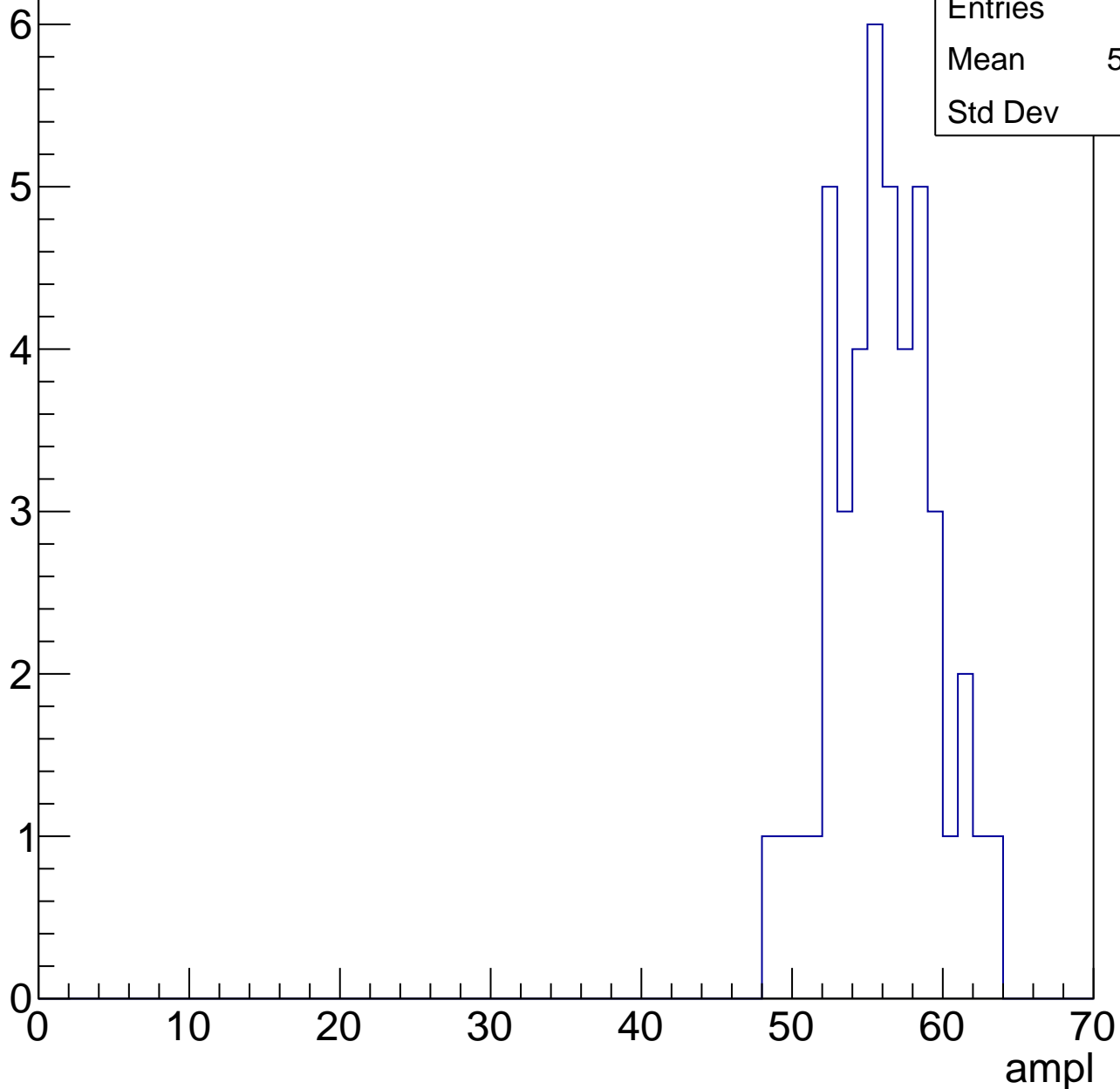
Entries	72
Mean	49.53
Std Dev	3.21

# B1L101S, U19-ch52, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

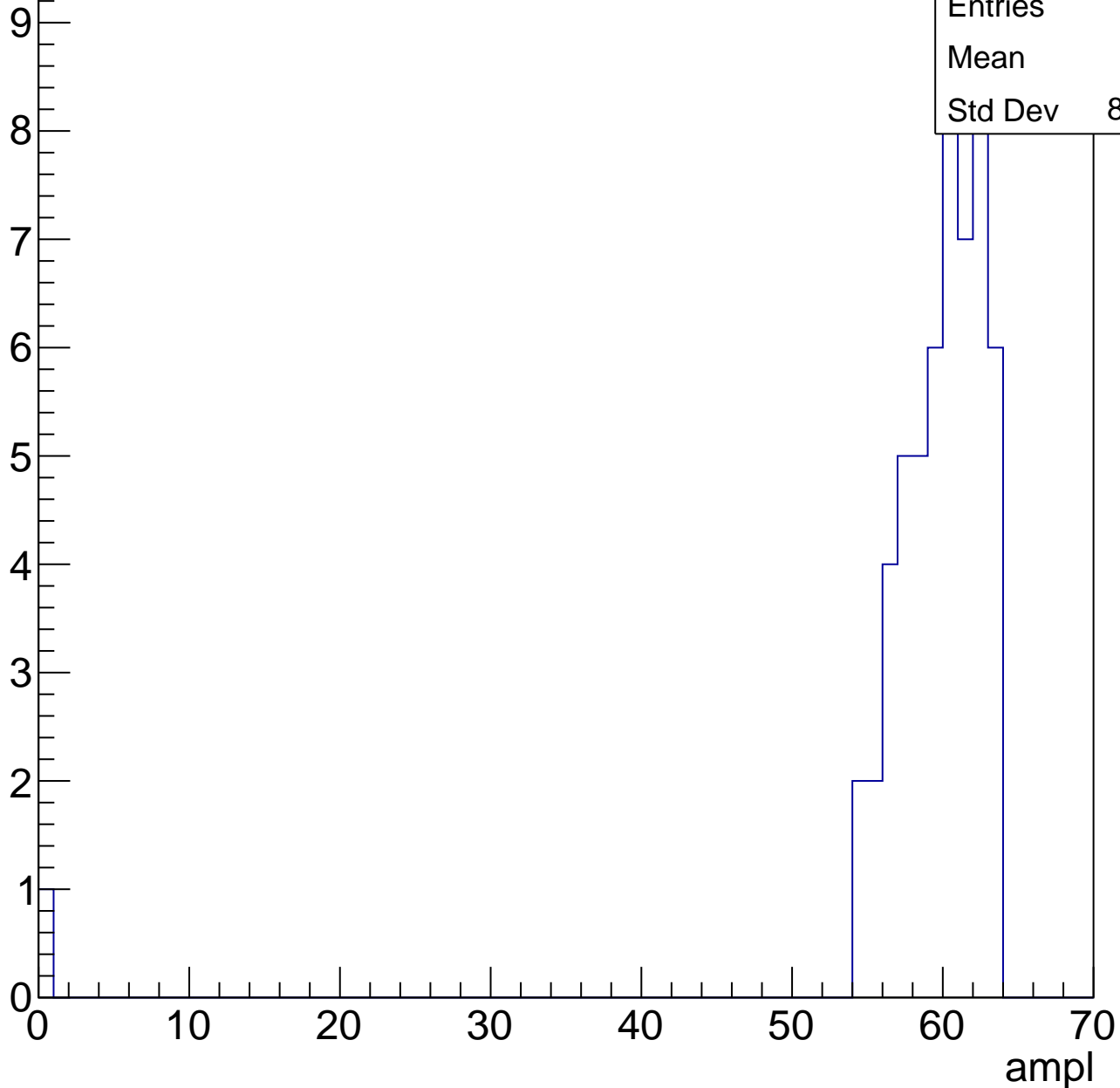
Entries	44
Mean	55.57
Std Dev	3.36



# B1L101S, U19-ch52, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

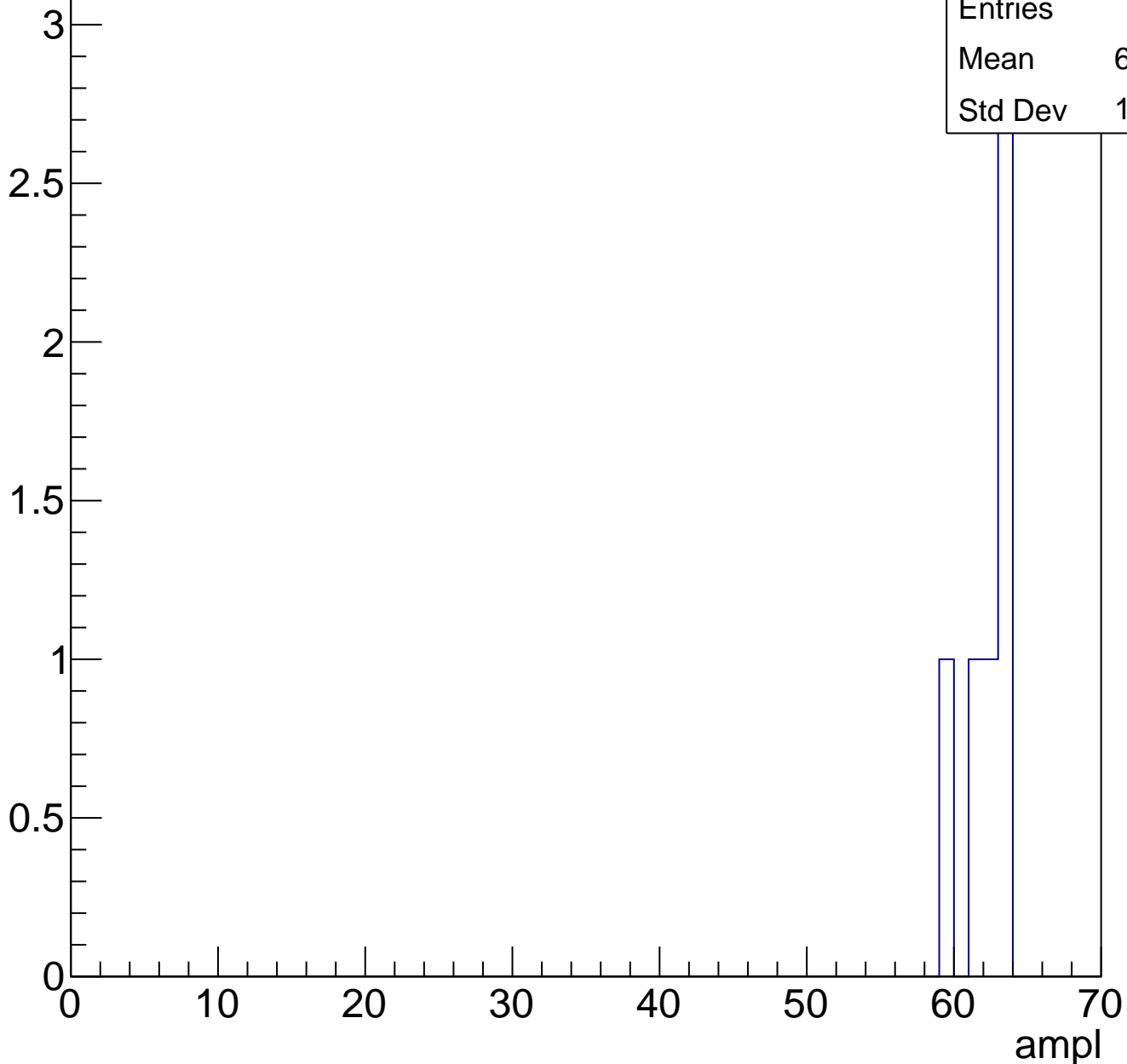
Entry



# B1L101S, U19-ch52, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	6
Mean	61.83
Std Dev	1.462



# B1L101S, U19-ch52, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L101S, U19-ch53, adc0

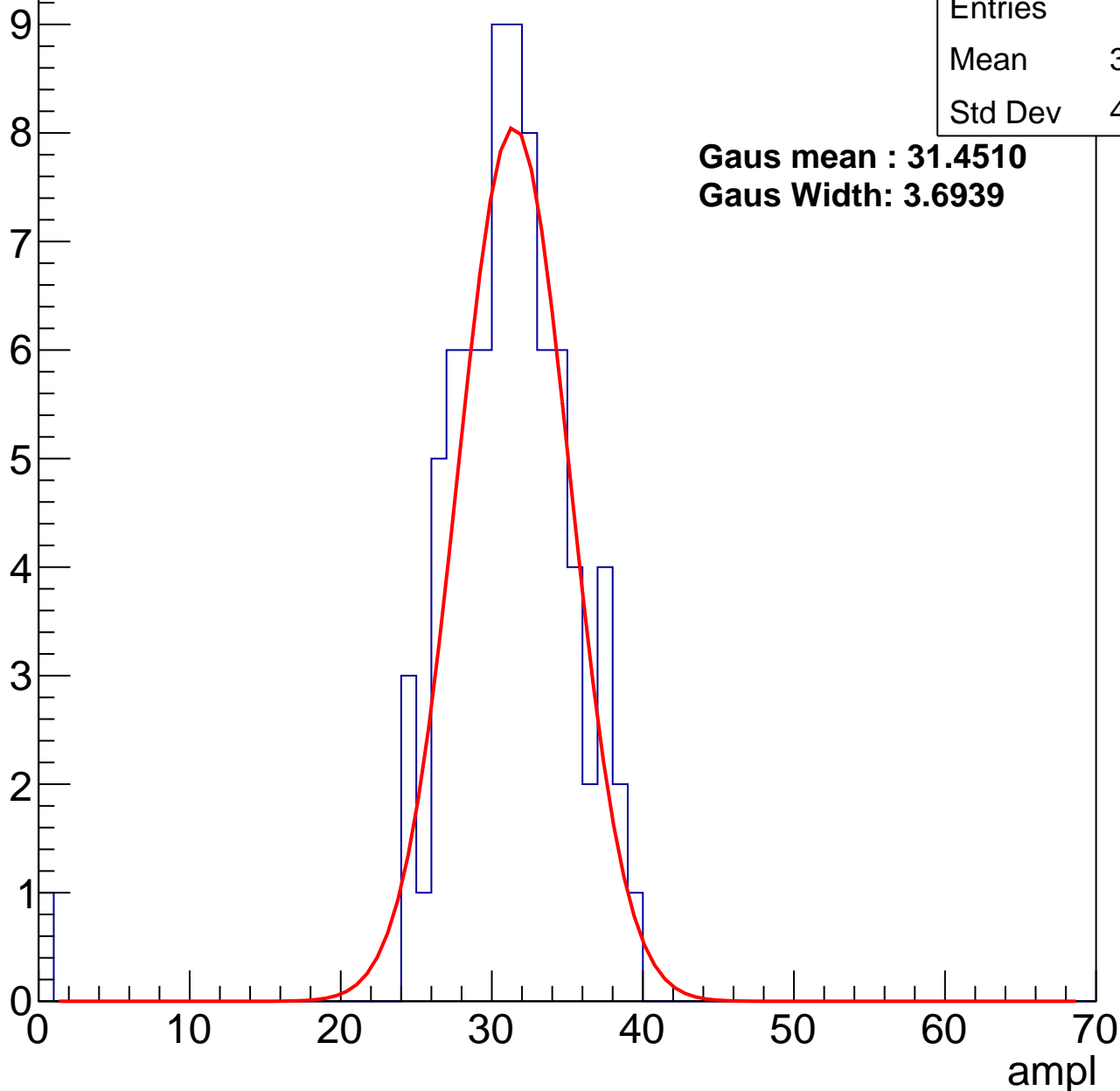
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	79
Mean	30.54
Std Dev	4.958

**Gaus mean : 31.4510**

**Gaus Width: 3.6939**



# B1L101S, U19-ch53, adc1

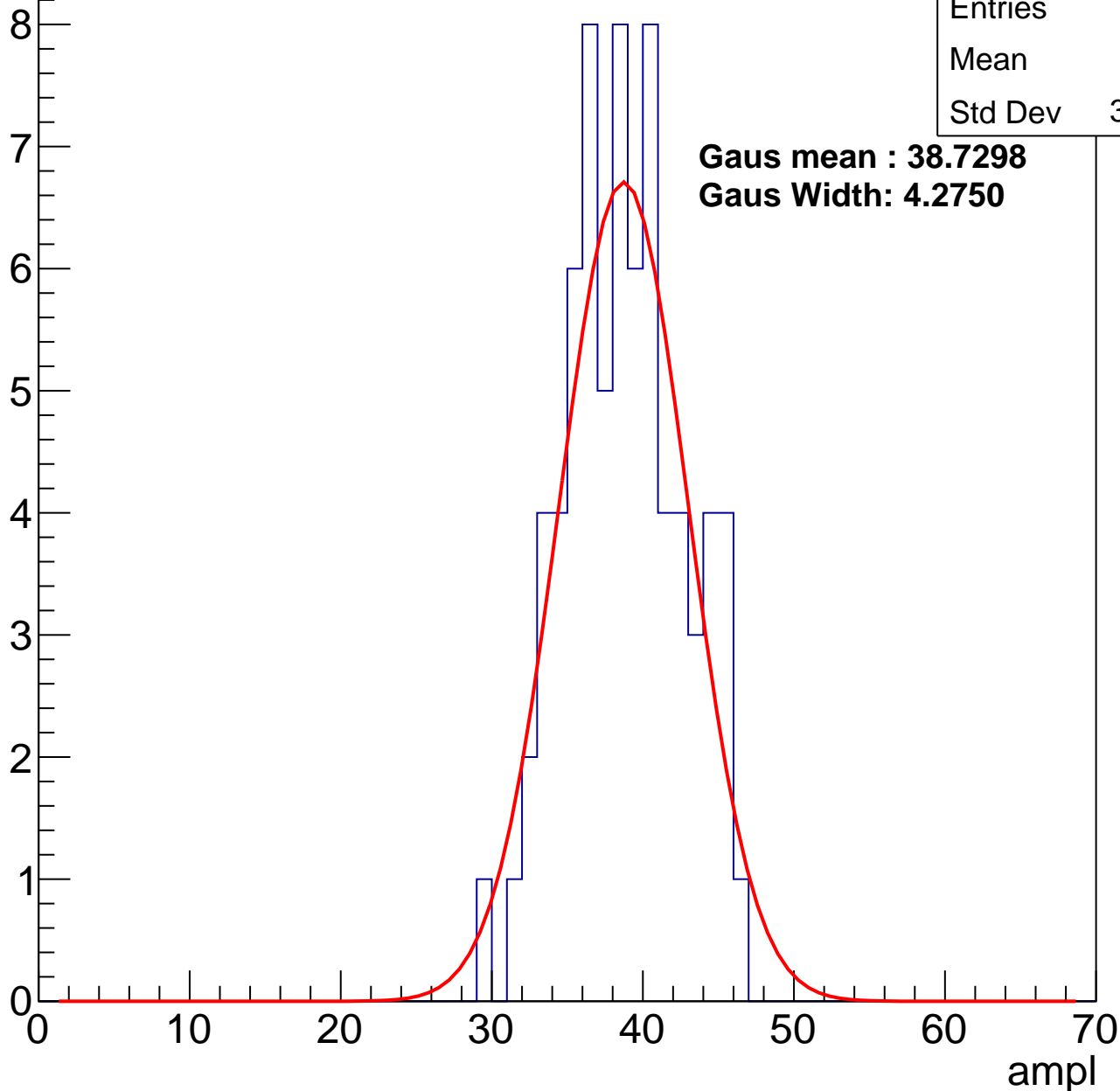
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	73
Mean	38.3
Std Dev	3.824

**Gaus mean : 38.7298**

**Gaus Width: 4.2750**

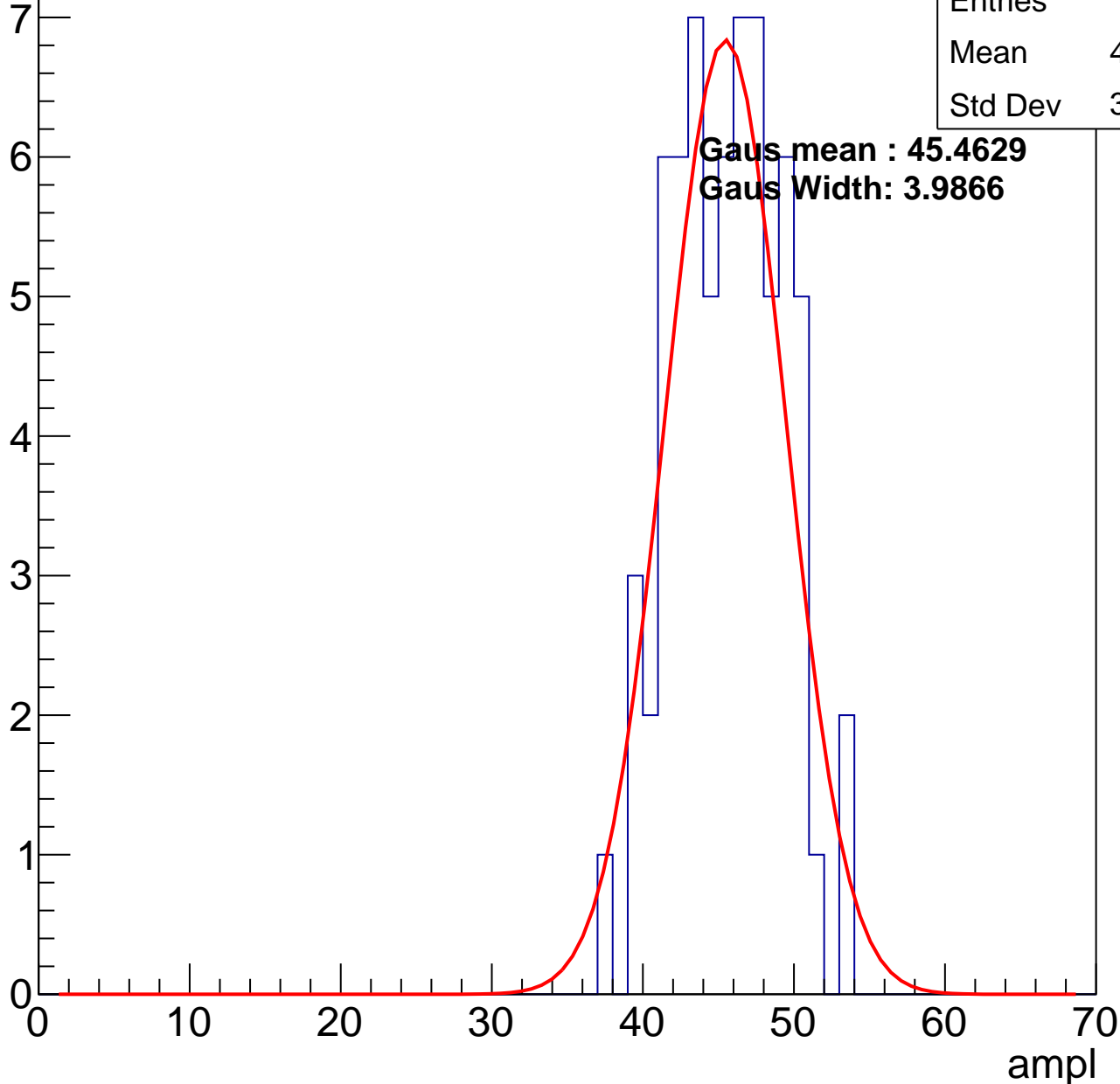


# B1L101S, U19-ch53, adc2

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	45.14
Std Dev	3.548

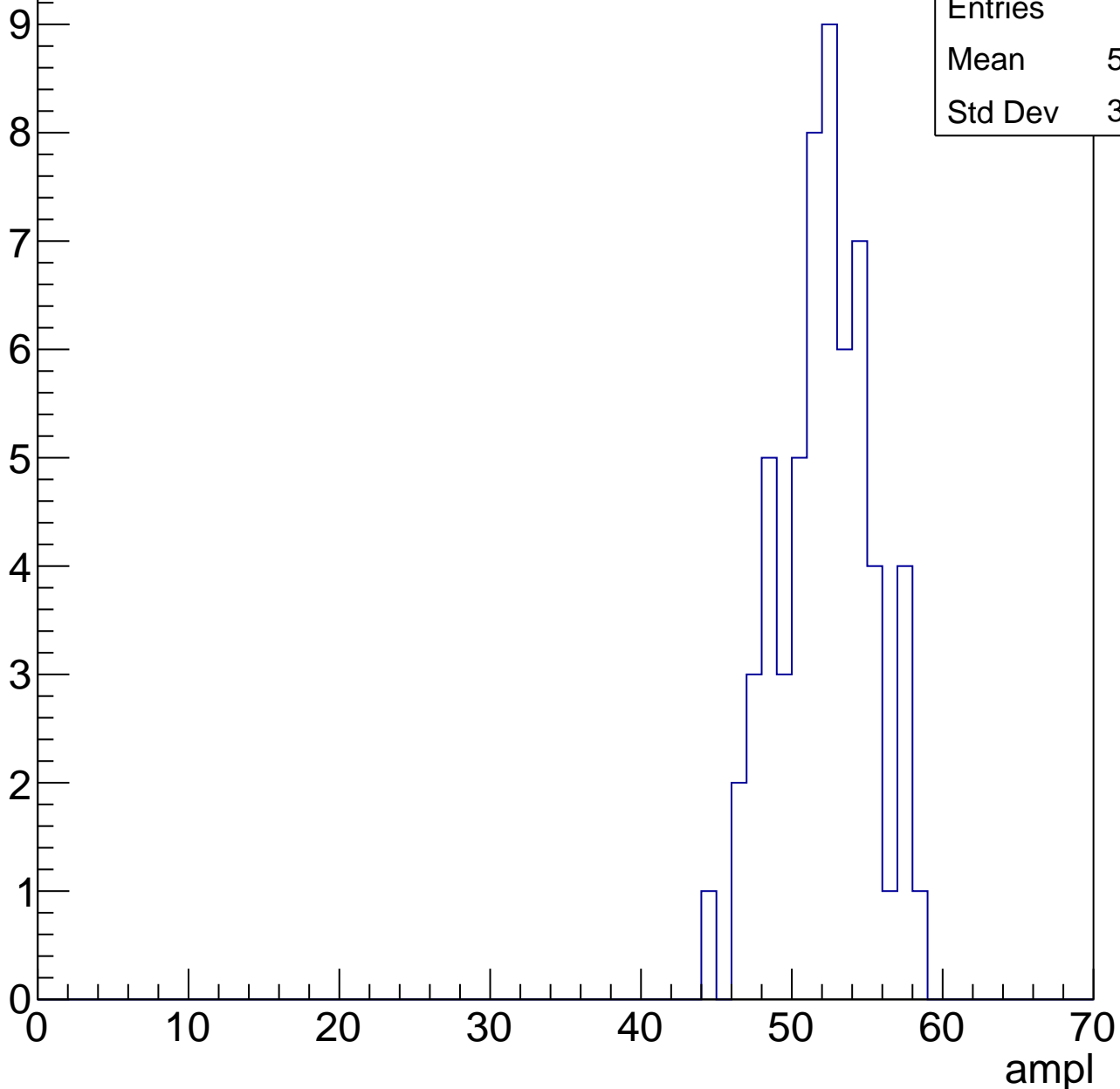


# B1L101S, U19-ch53, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	59
Mean	51.66
Std Dev	3.084

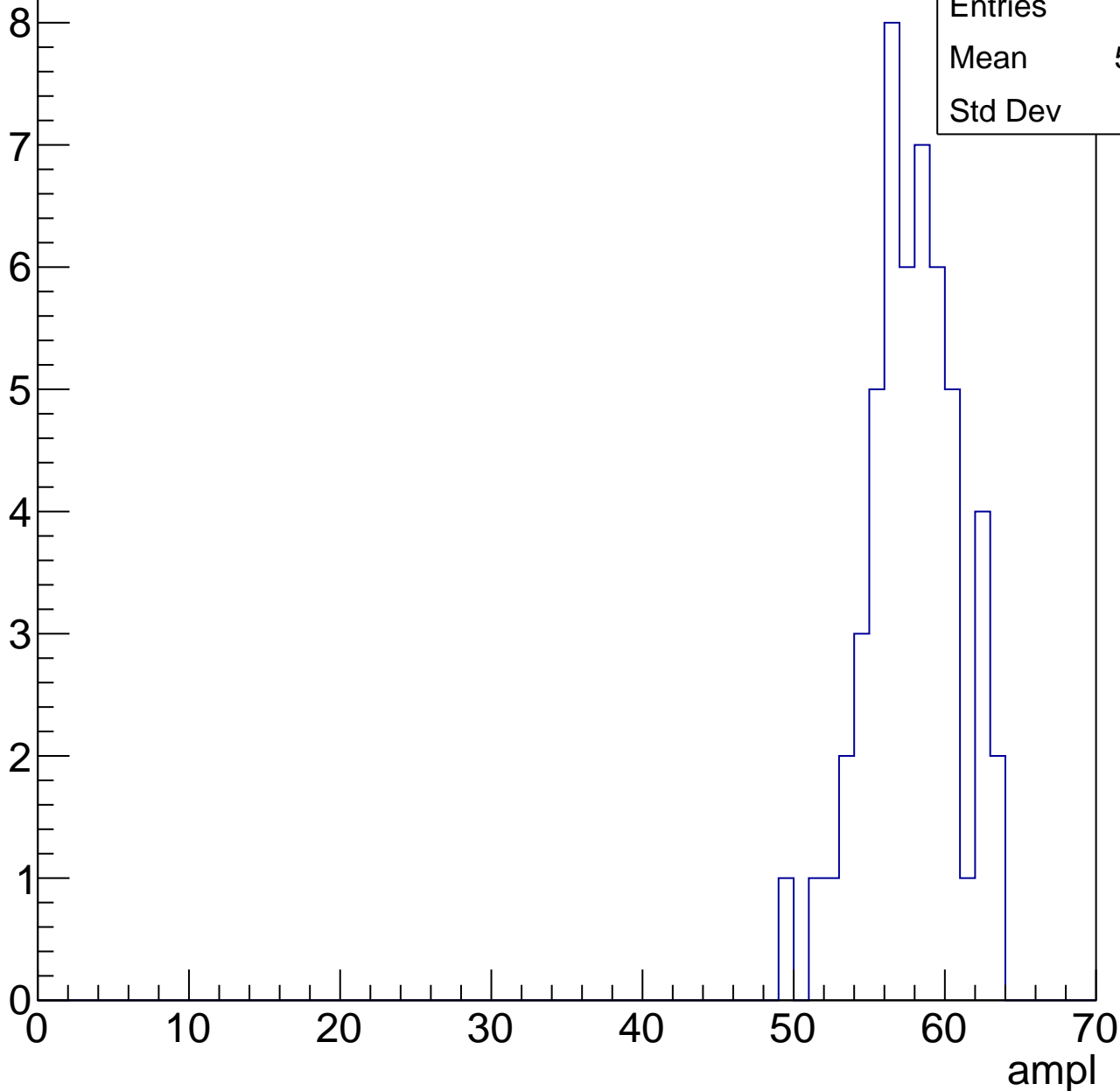


# B1L101S, U19-ch53, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	52
Mean	57.31
Std Dev	3.01

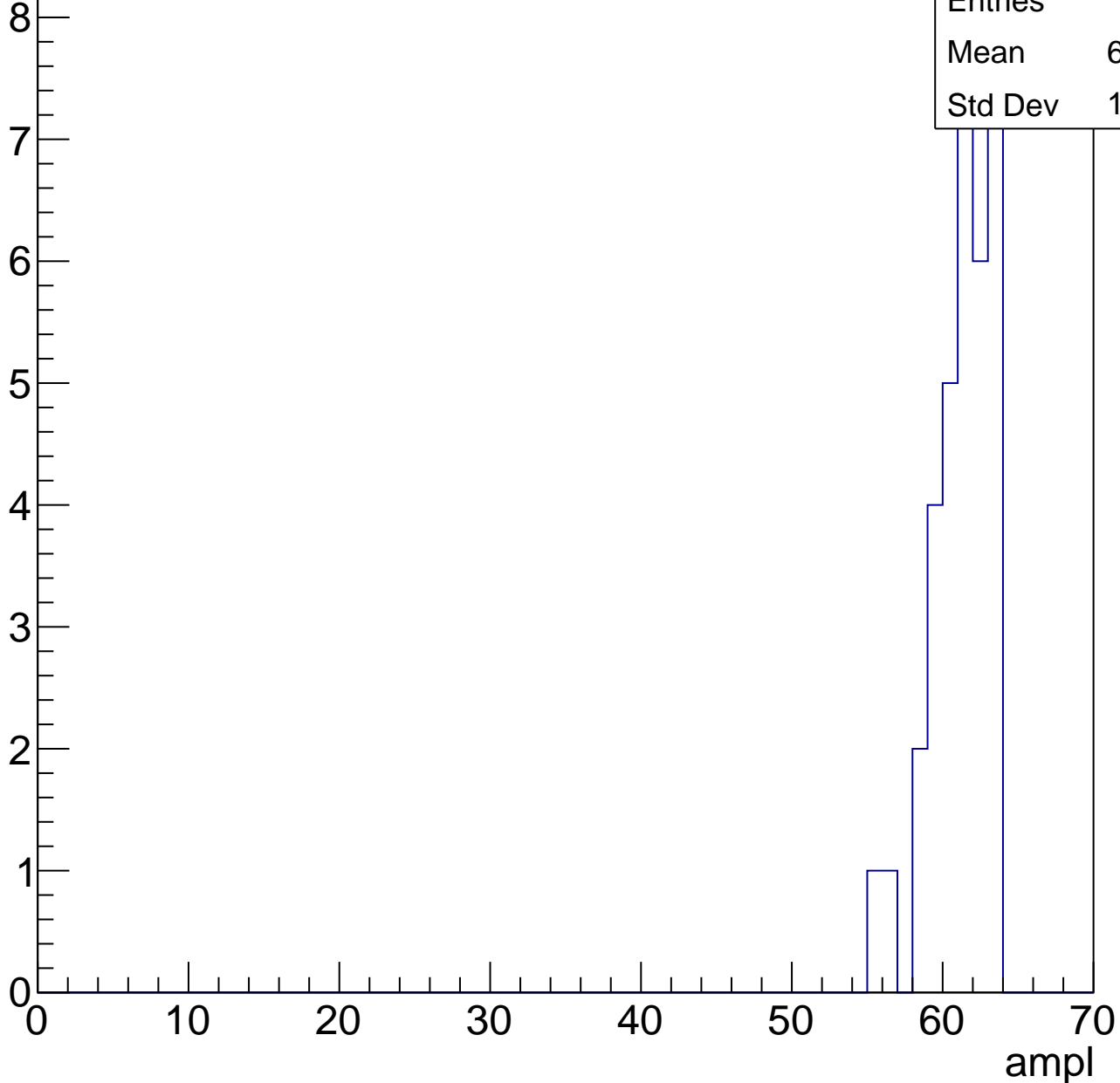


# B1L101S, U19-ch53, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

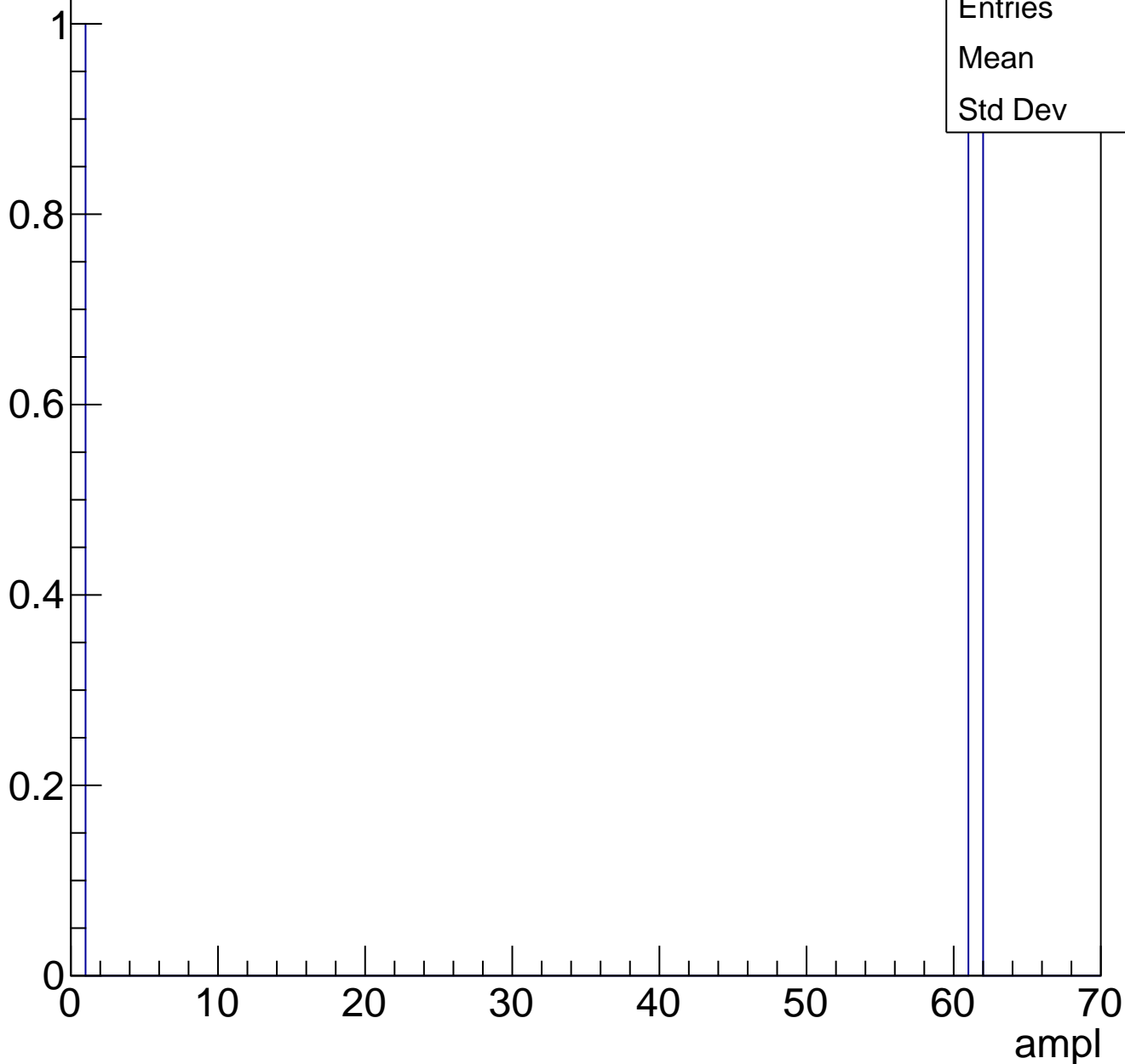
Entries	35
Mean	60.77
Std Dev	1.972



# B1L101S, U19-ch53, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U19-ch53, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U19-ch54, adc0

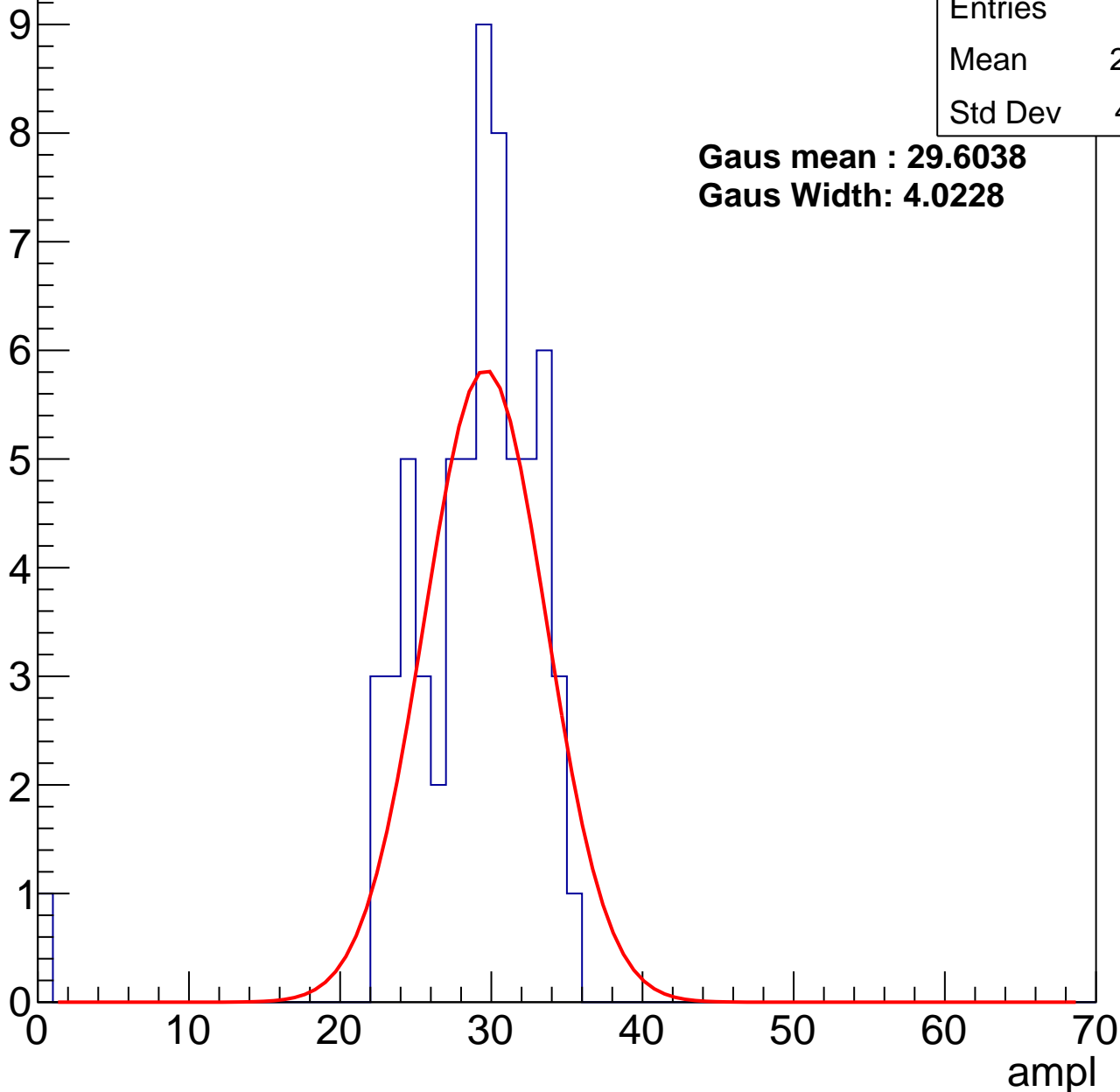
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	28.25
Std Dev	4.931

**Gaus mean : 29.6038**

**Gaus Width: 4.0228**



# B1L101S, U19-ch54, adc1

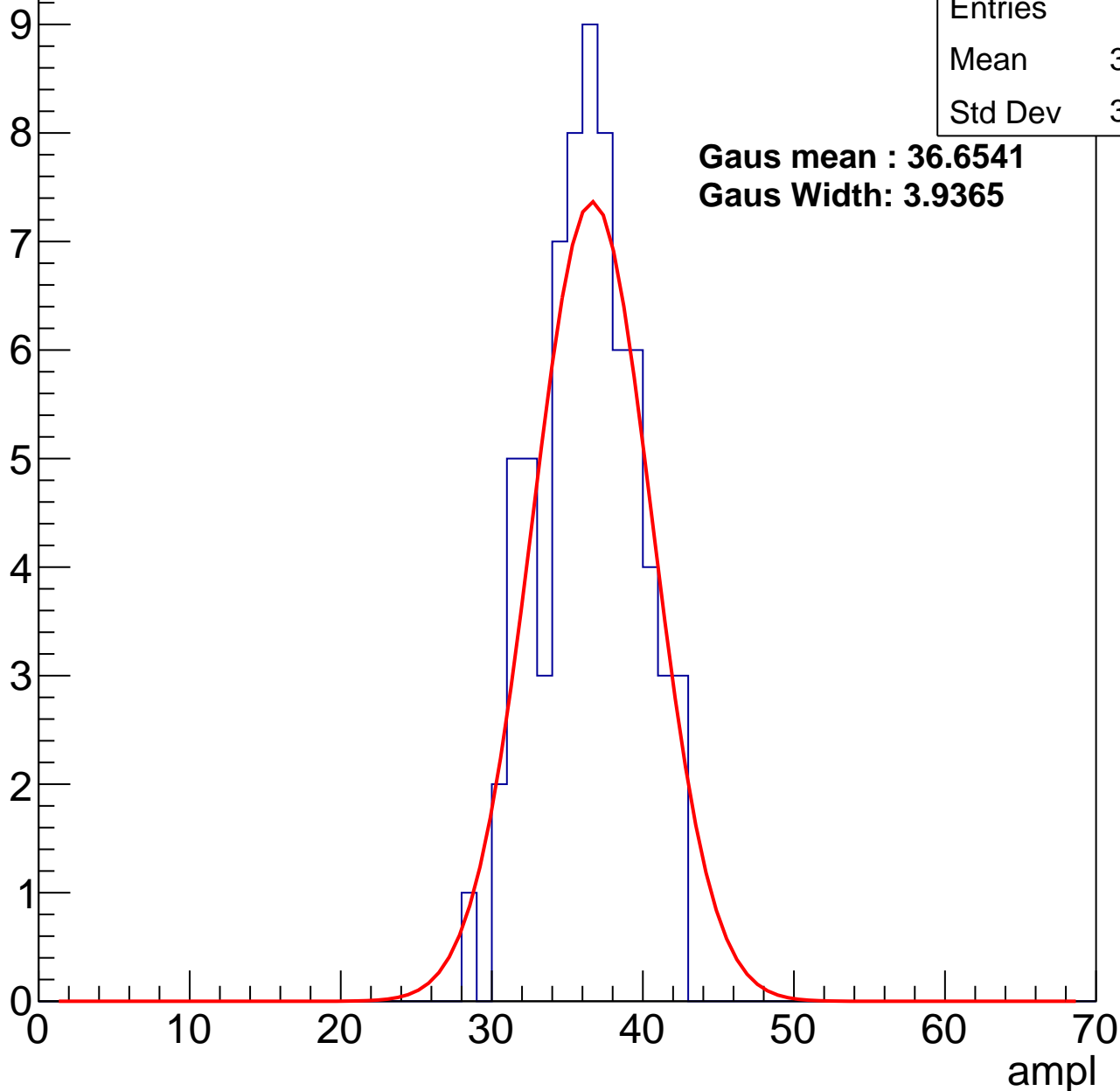
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	35.87
Std Dev	3.242

**Gaus mean : 36.6541**

**Gaus Width: 3.9365**



# B1L101S, U19-ch54, adc2

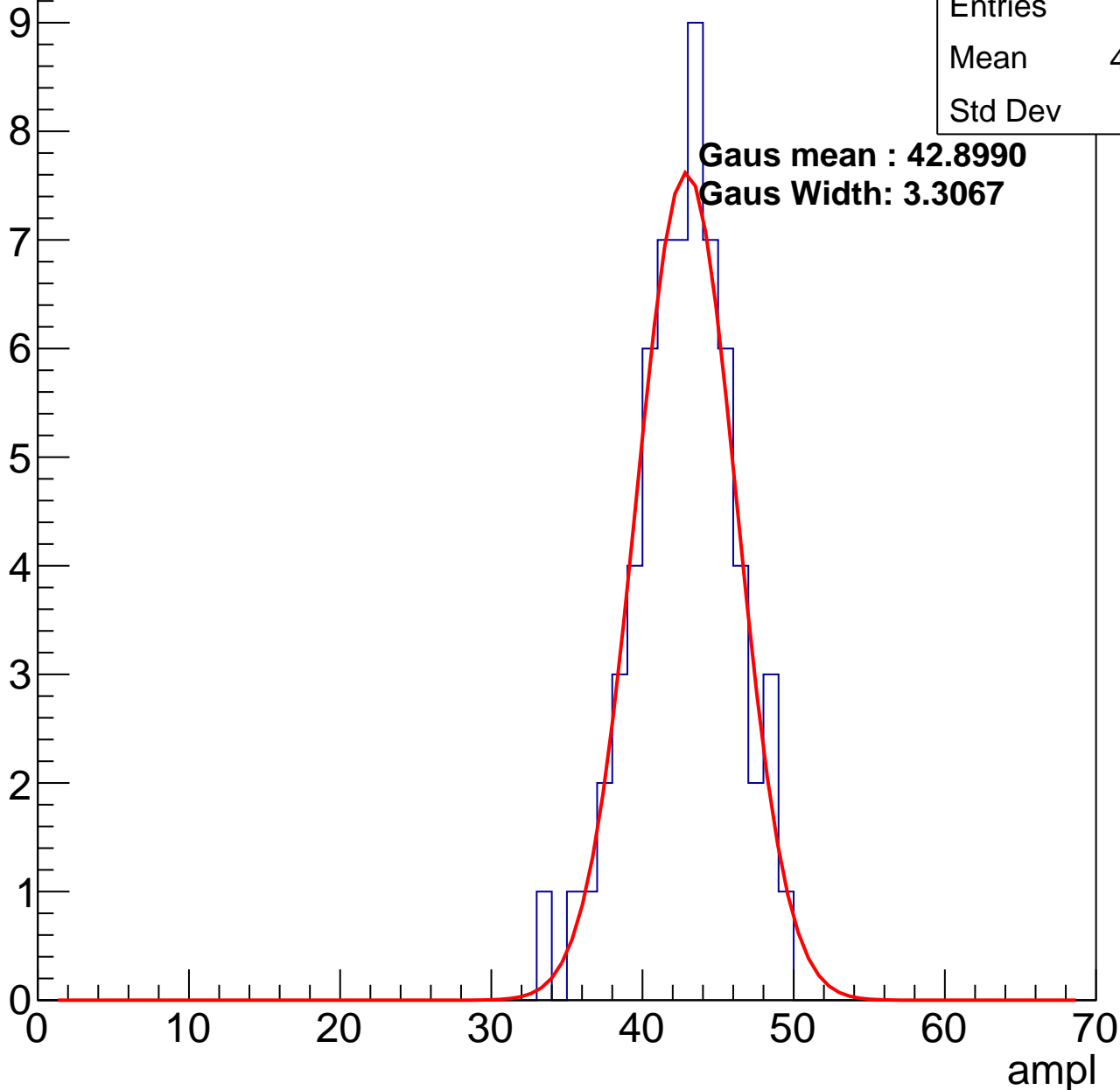
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	42.27
Std Dev	3.28

**Gaus mean : 42.8990**

**Gaus Width: 3.3067**

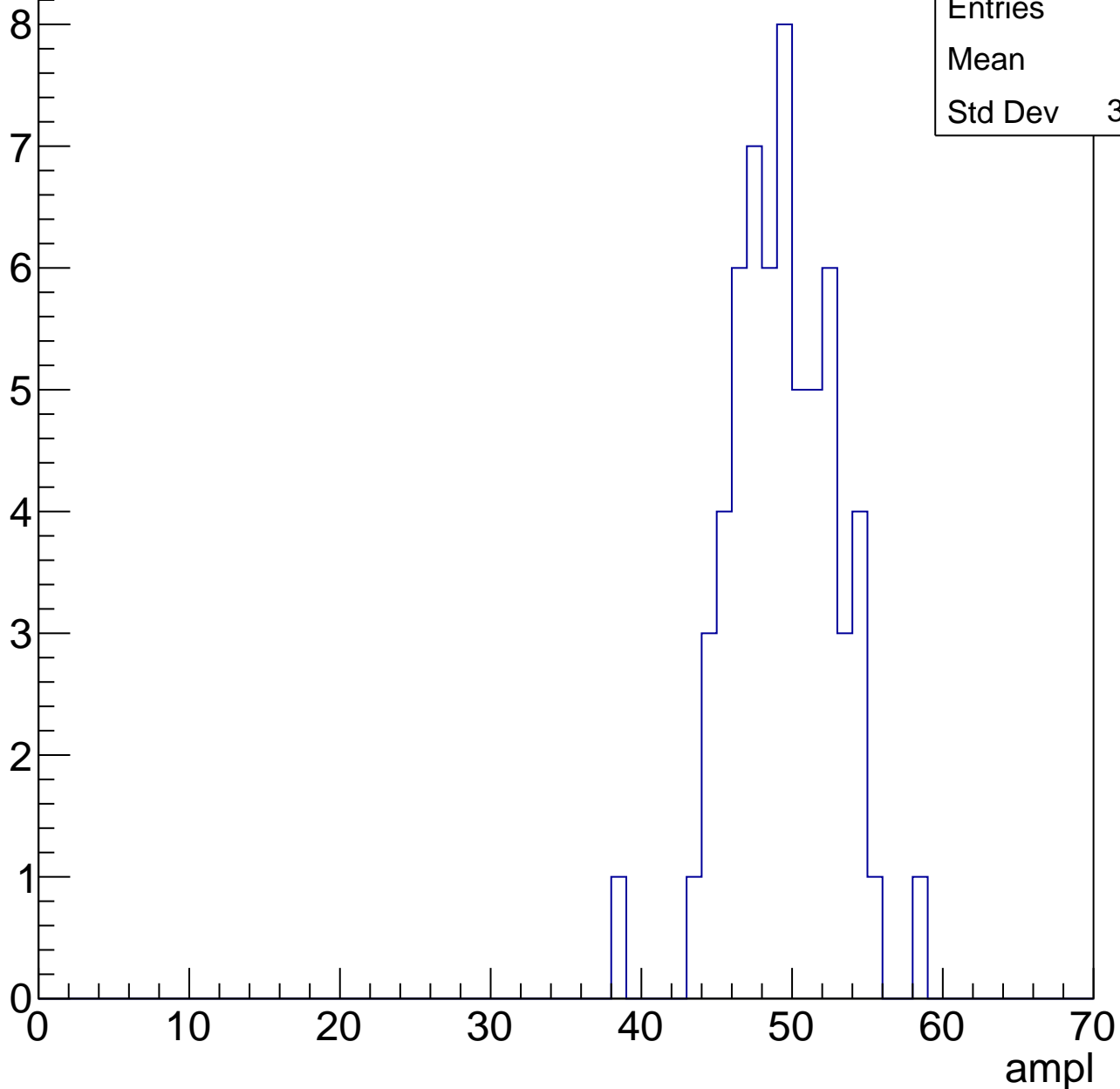


# B1L101S, U19-ch54, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

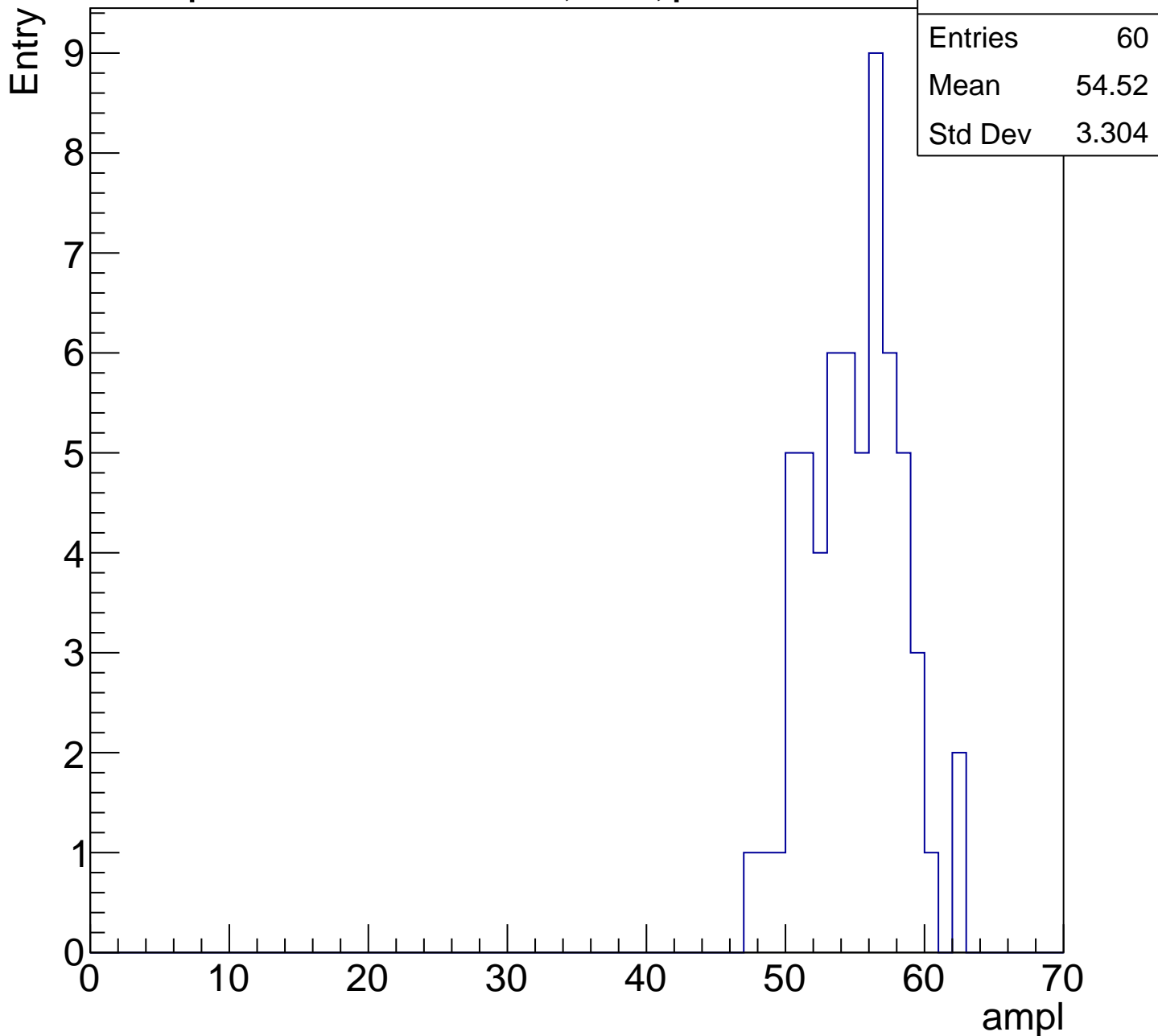
Entry

Entries	61
Mean	48.9
Std Dev	3.453



# B1L101S, U19-ch54, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U19-ch54, adc5

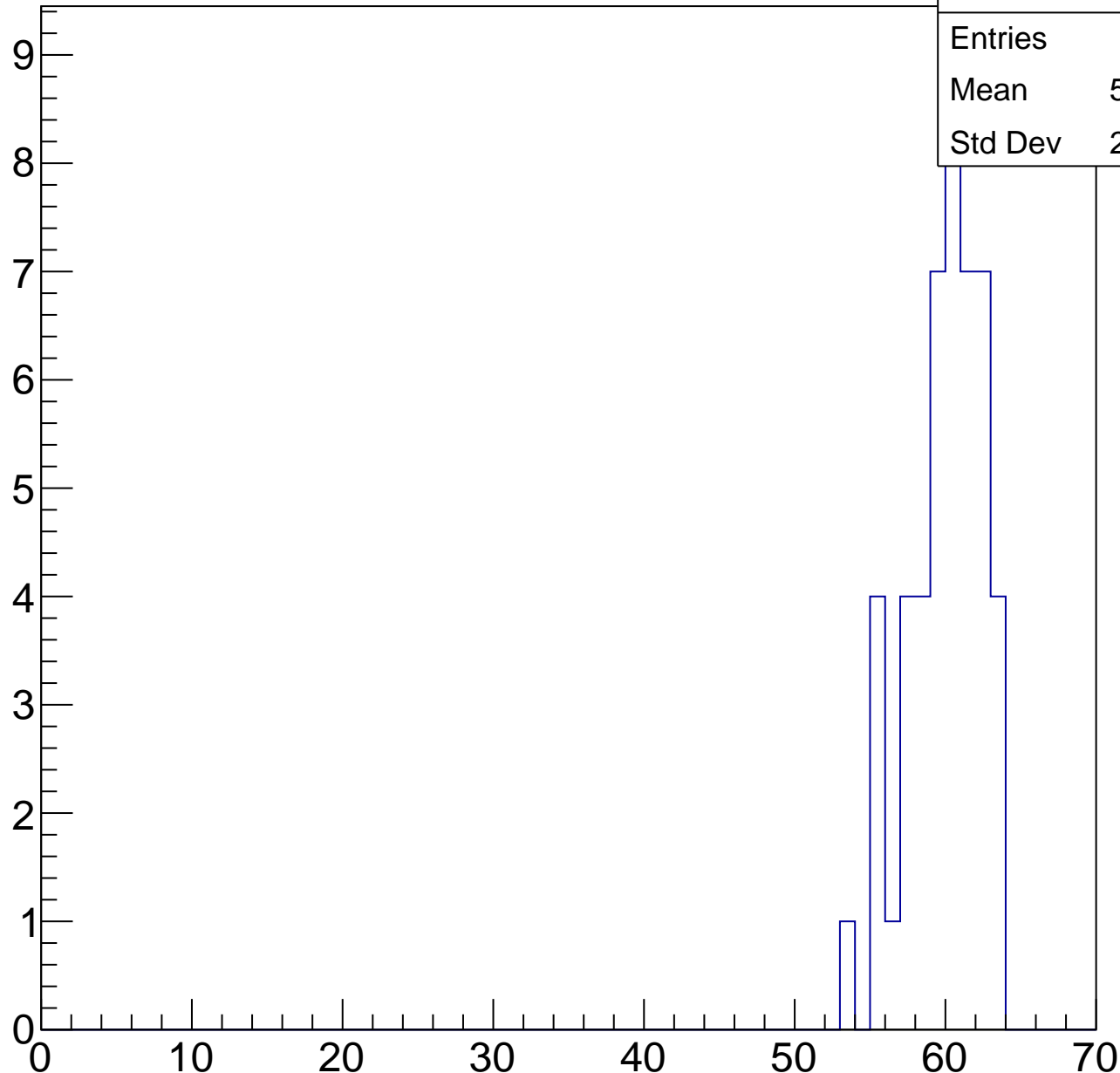
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	48
Mean	59.48
Std Dev	2.424

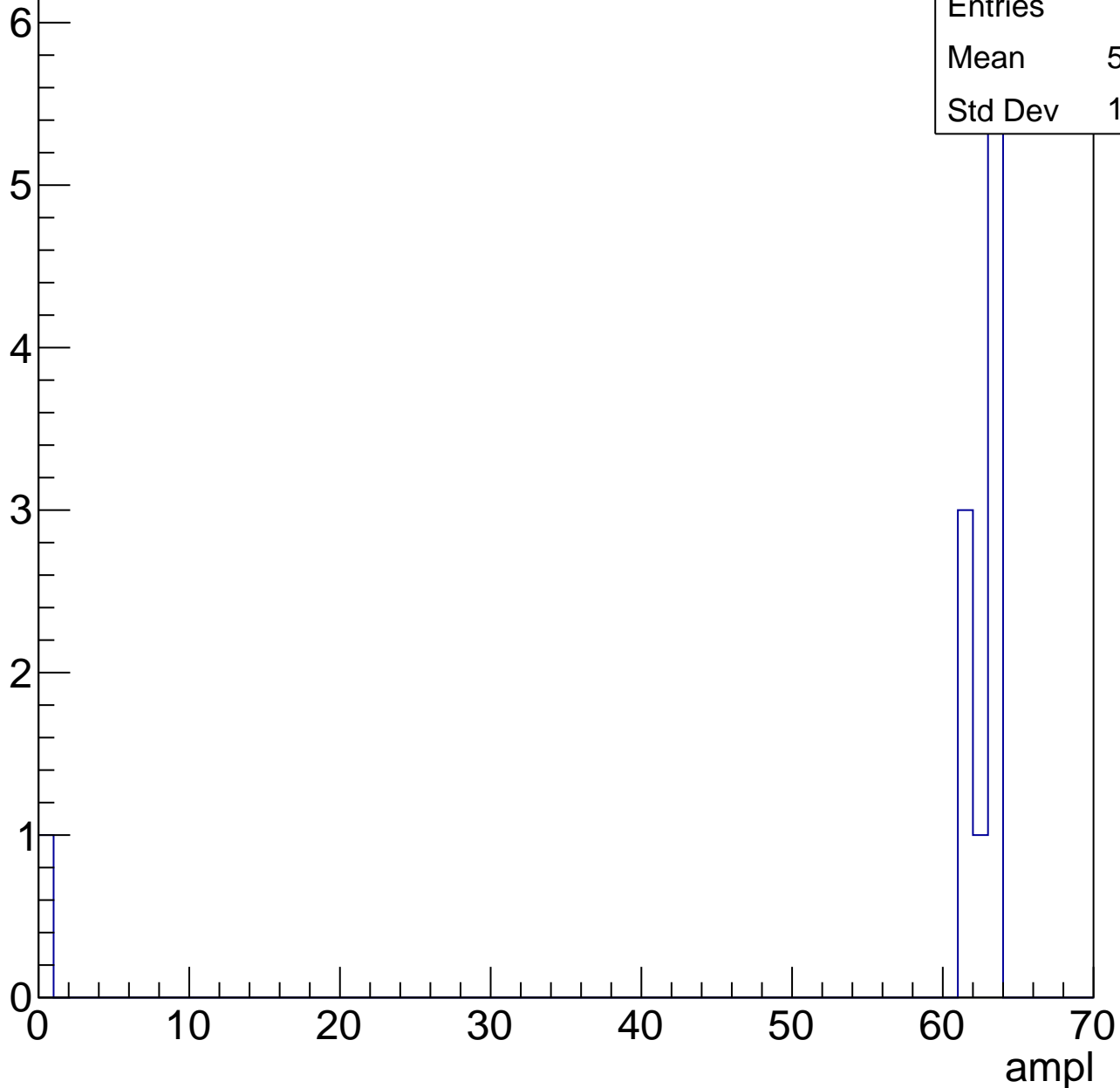
ampl



# B1L101S, U19-ch54, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U19-ch54, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U19-ch55, adc0

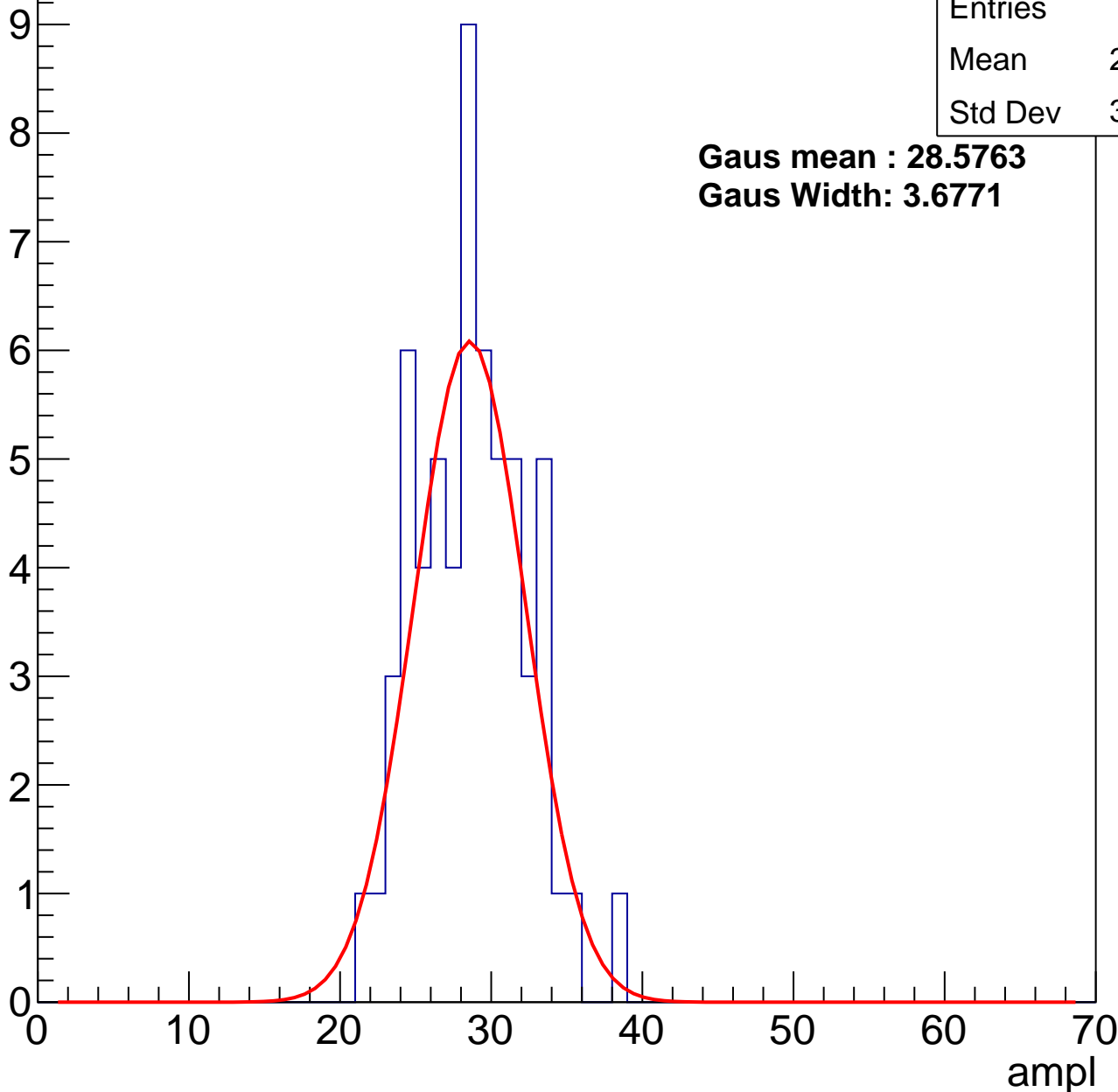
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	60
Mean	28.22
Std Dev	3.517

**Gaus mean : 28.5763**

**Gaus Width: 3.6771**



# B1L101S, U19-ch55, adc1

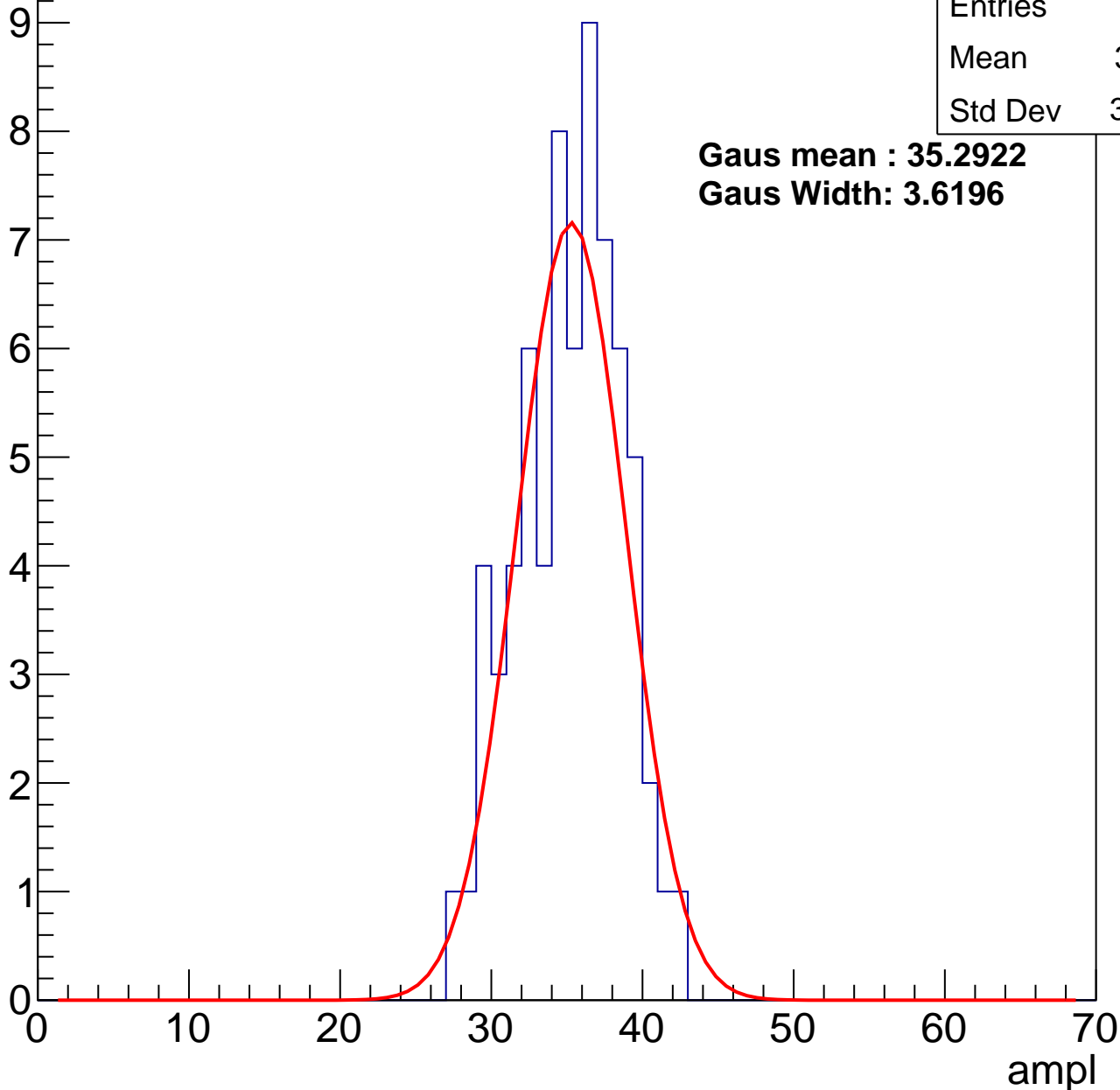
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	34.71
Std Dev	3.374

**Gaus mean : 35.2922**

**Gaus Width: 3.6196**



# B1L101S, U19-ch55, adc2

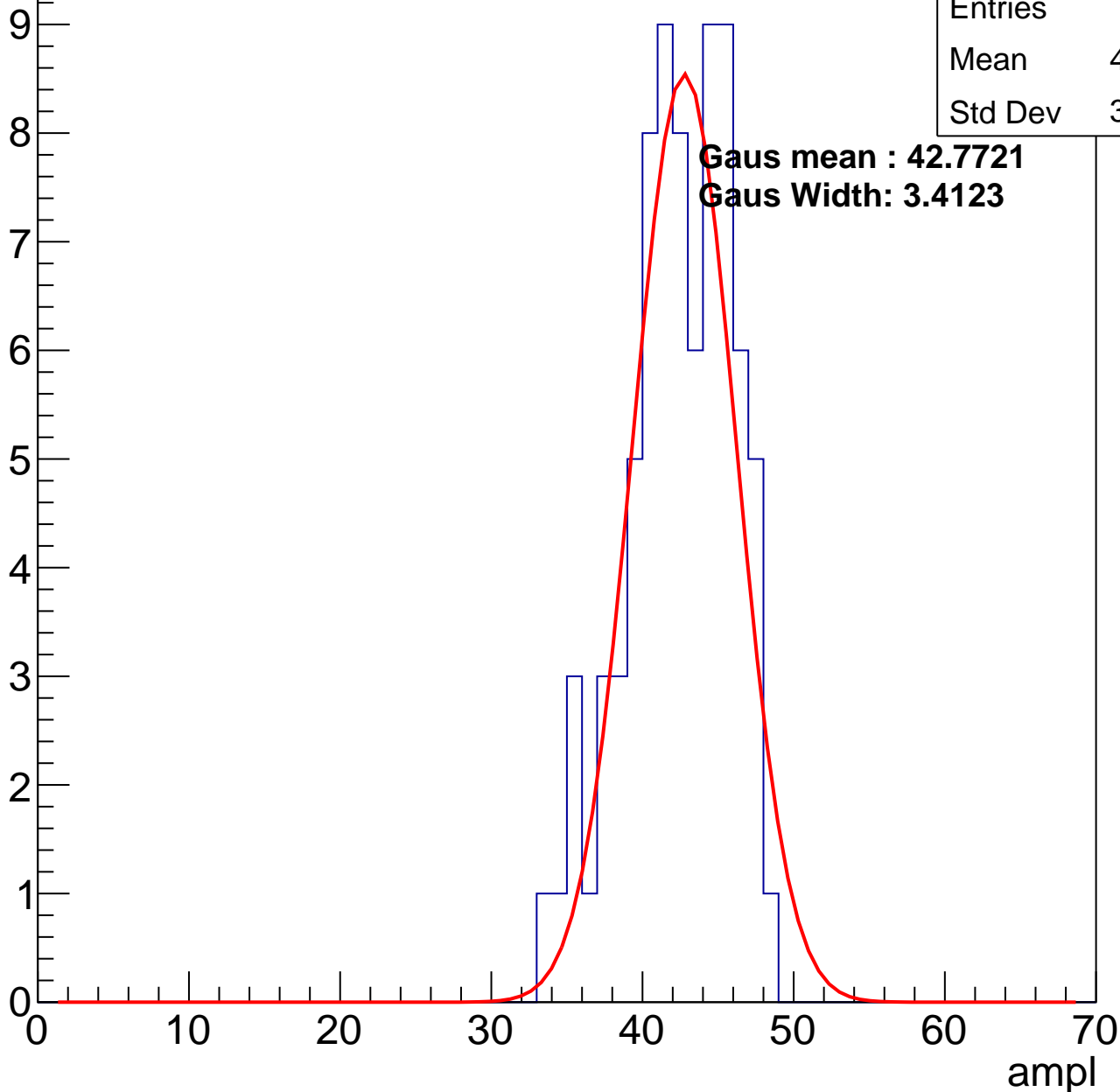
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	78
Mean	41.94
Std Dev	3.428

**Gaus mean : 42.7721**

**Gaus Width: 3.4123**

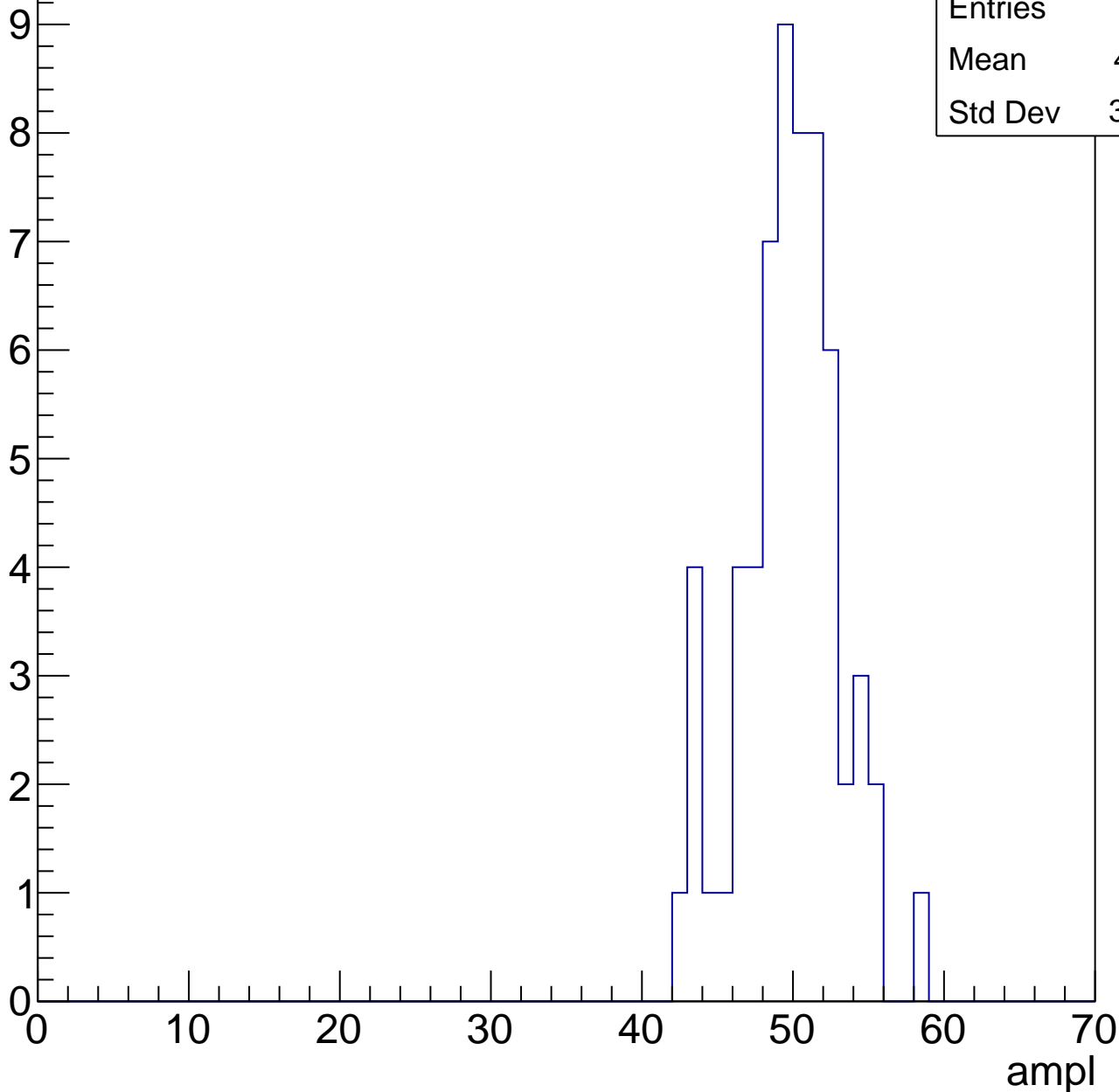


# B1L101S, U19-ch55, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

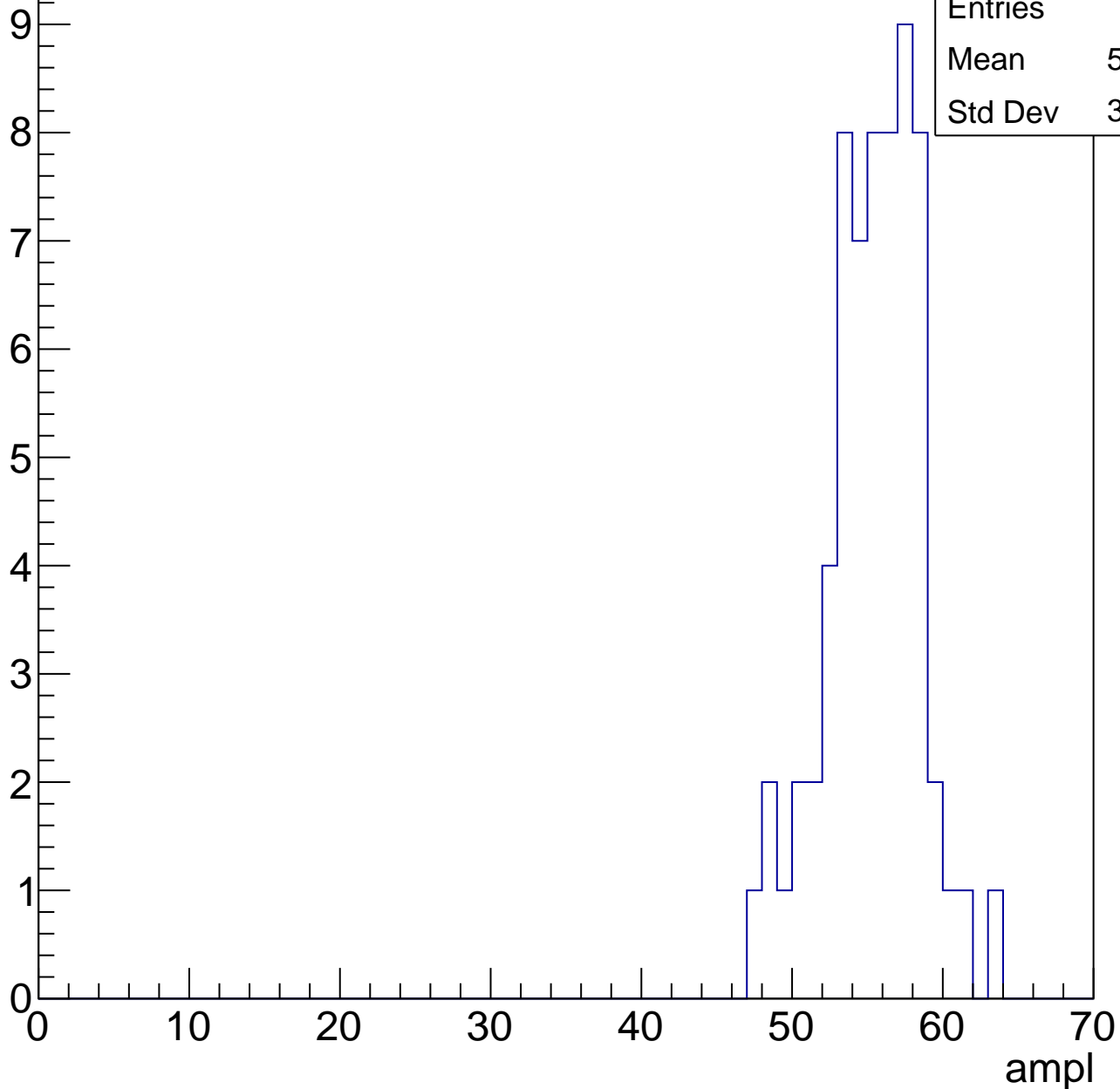
Entries	61
Mean	49.31
Std Dev	3.242



# B1L101S, U19-ch55, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

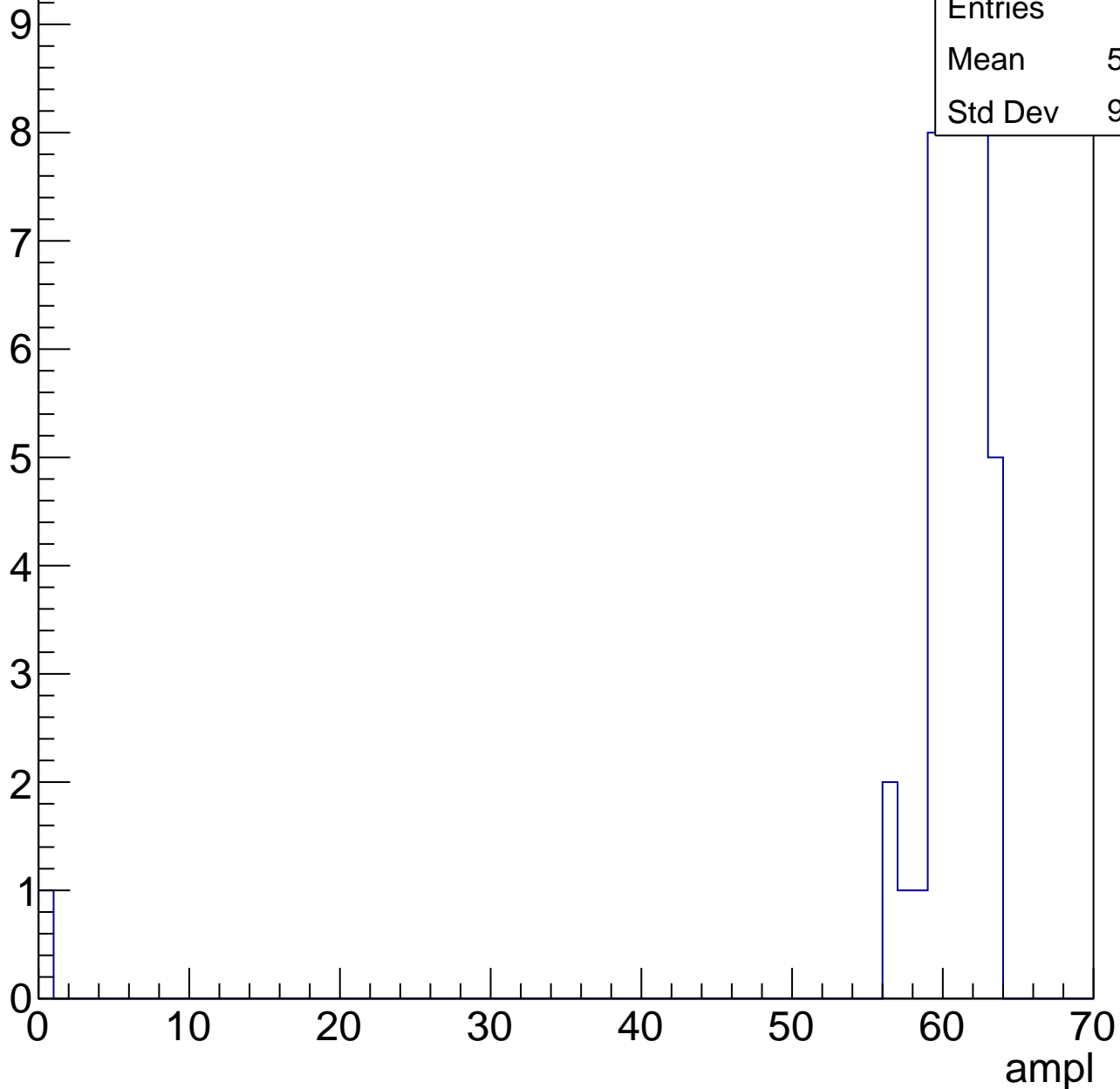
Entry



# B1L101S, U19-ch55, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U19-ch55, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	6
Mean	62.5
Std Dev	0.7638



# B1L101S, U19-ch55, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U19-ch56, adc0

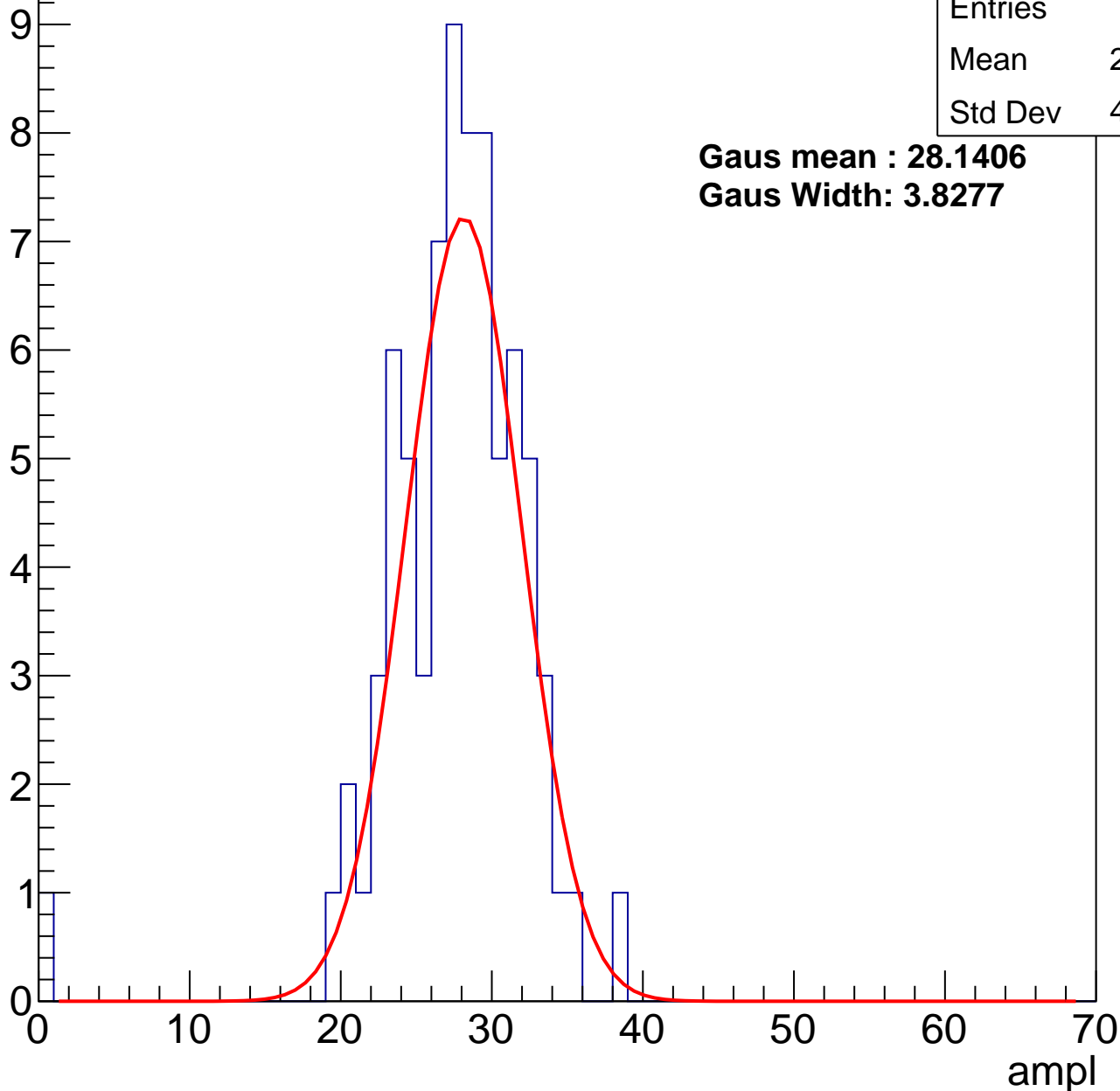
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	76
Mean	27.13
Std Dev	4.878

**Gaus mean : 28.1406**

**Gaus Width: 3.8277**



# B1L101S, U19-ch56, adc1

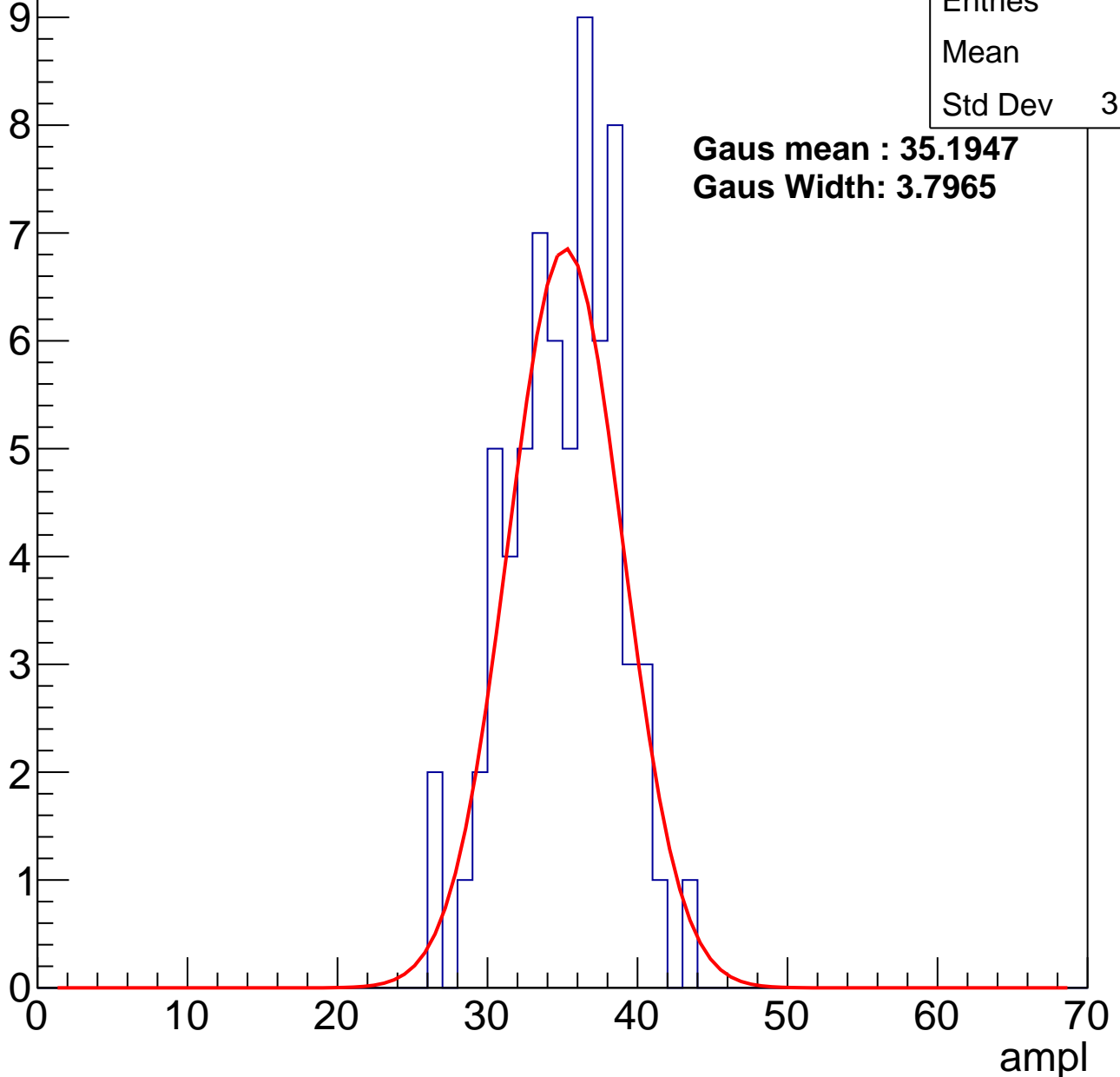
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	34.6
Std Dev	3.573

**Gaus mean : 35.1947**

**Gaus Width: 3.7965**



# B1L101S, U19-ch56, adc2

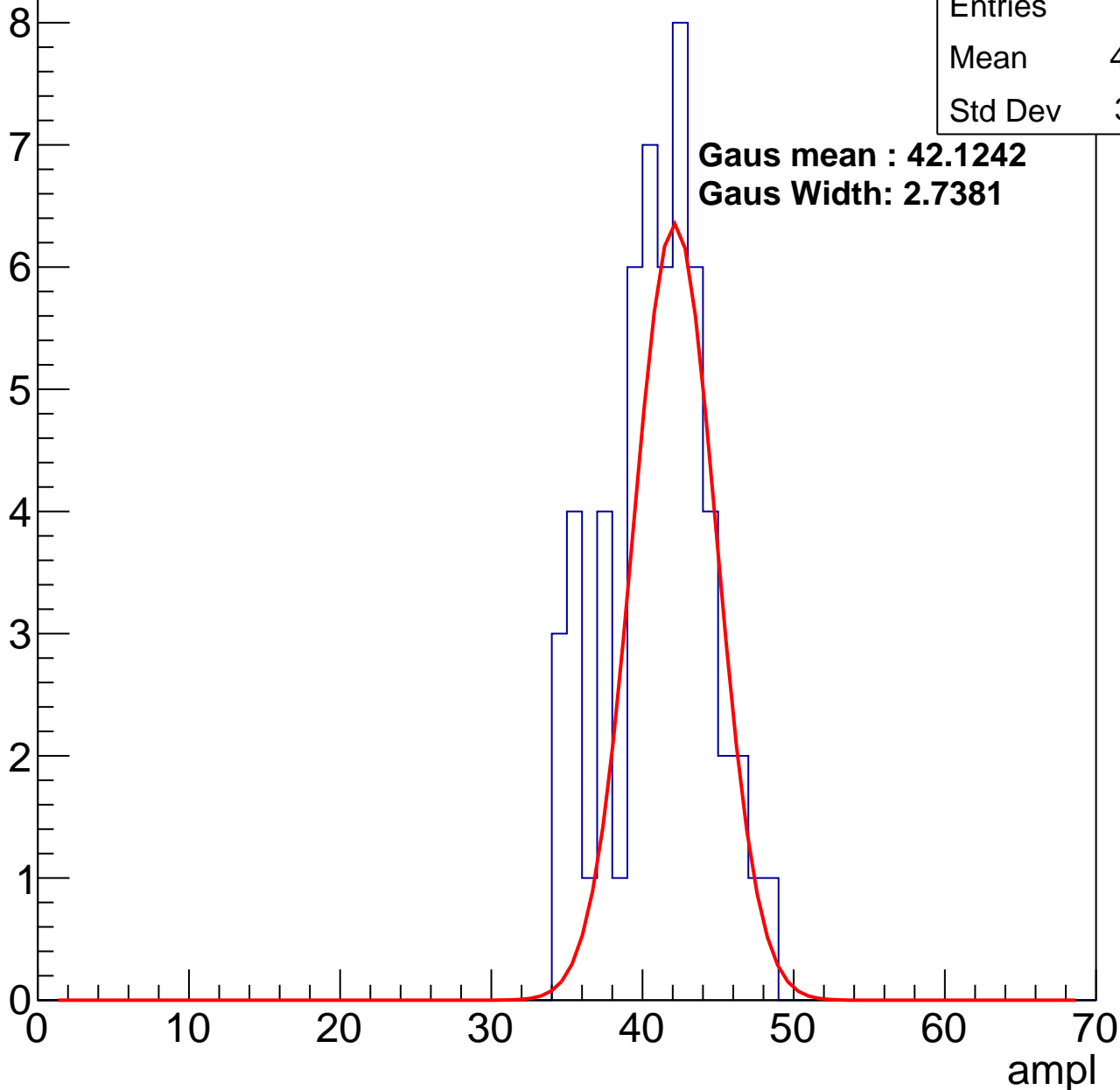
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	56
Mean	40.55
Std Dev	3.391

**Gaus mean : 42.1242**

**Gaus Width: 2.7381**

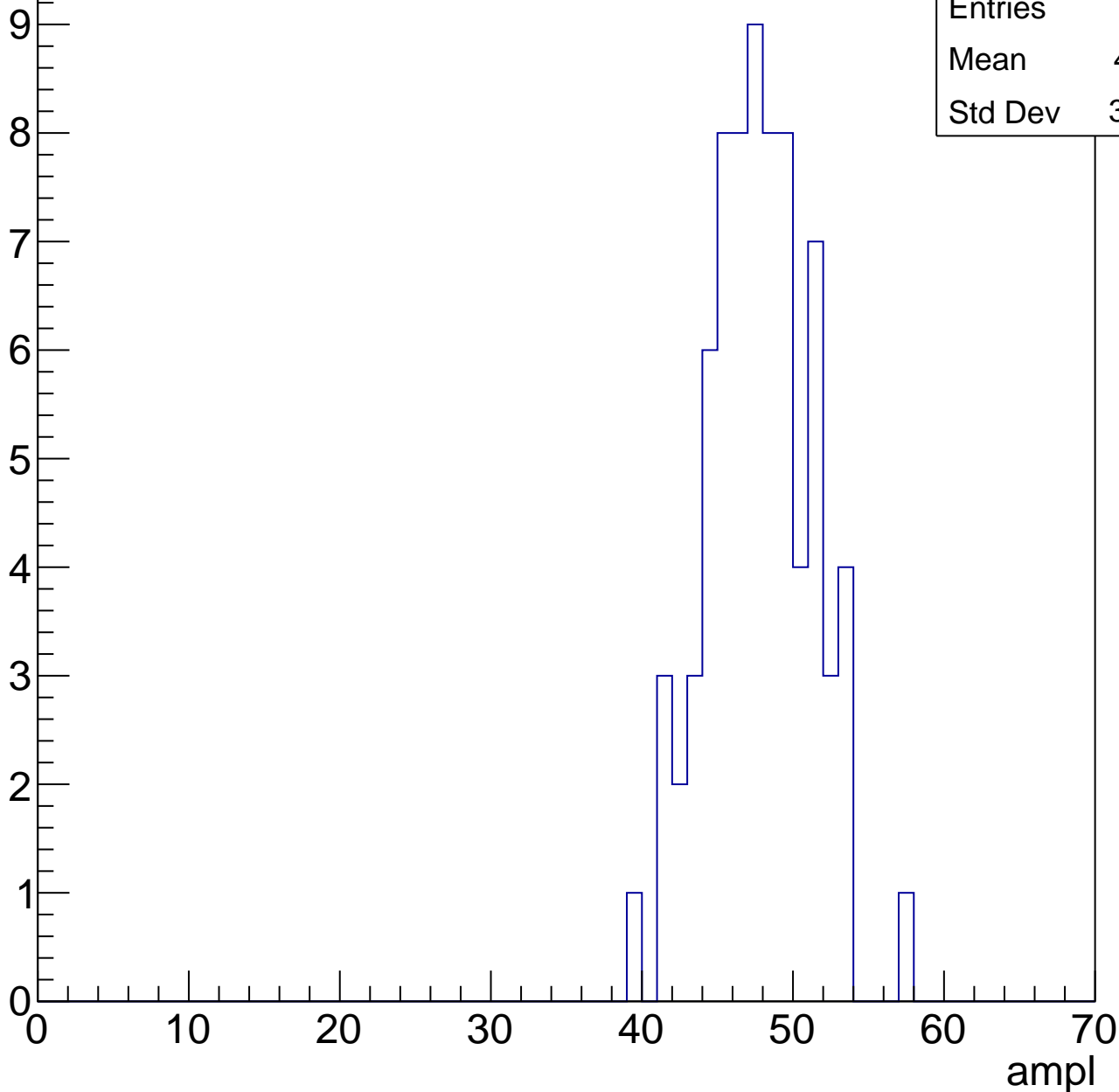


# B1L101S, U19-ch56, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	75
Mean	47.31
Std Dev	3.394

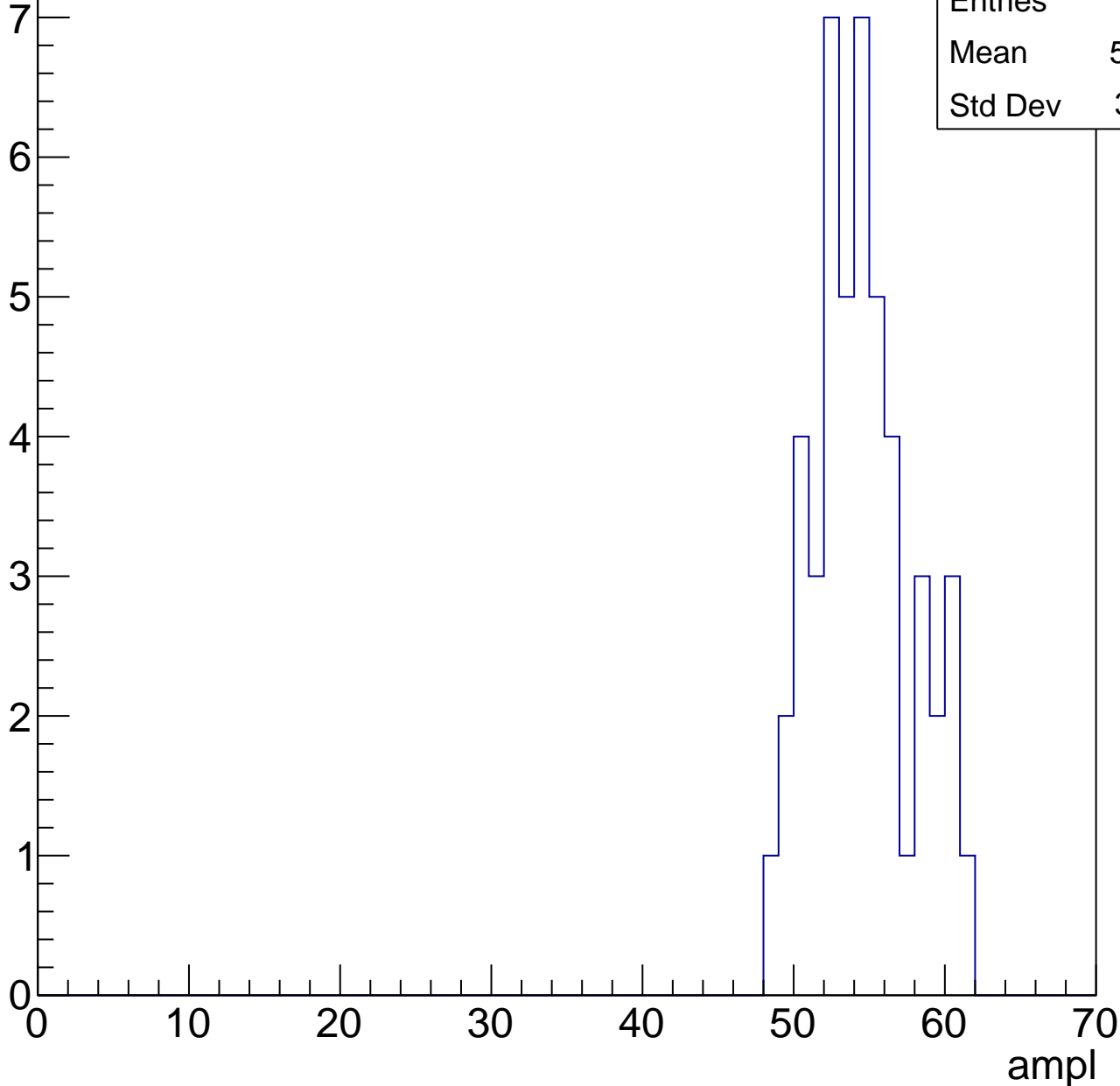


# B1L101S, U19-ch56, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

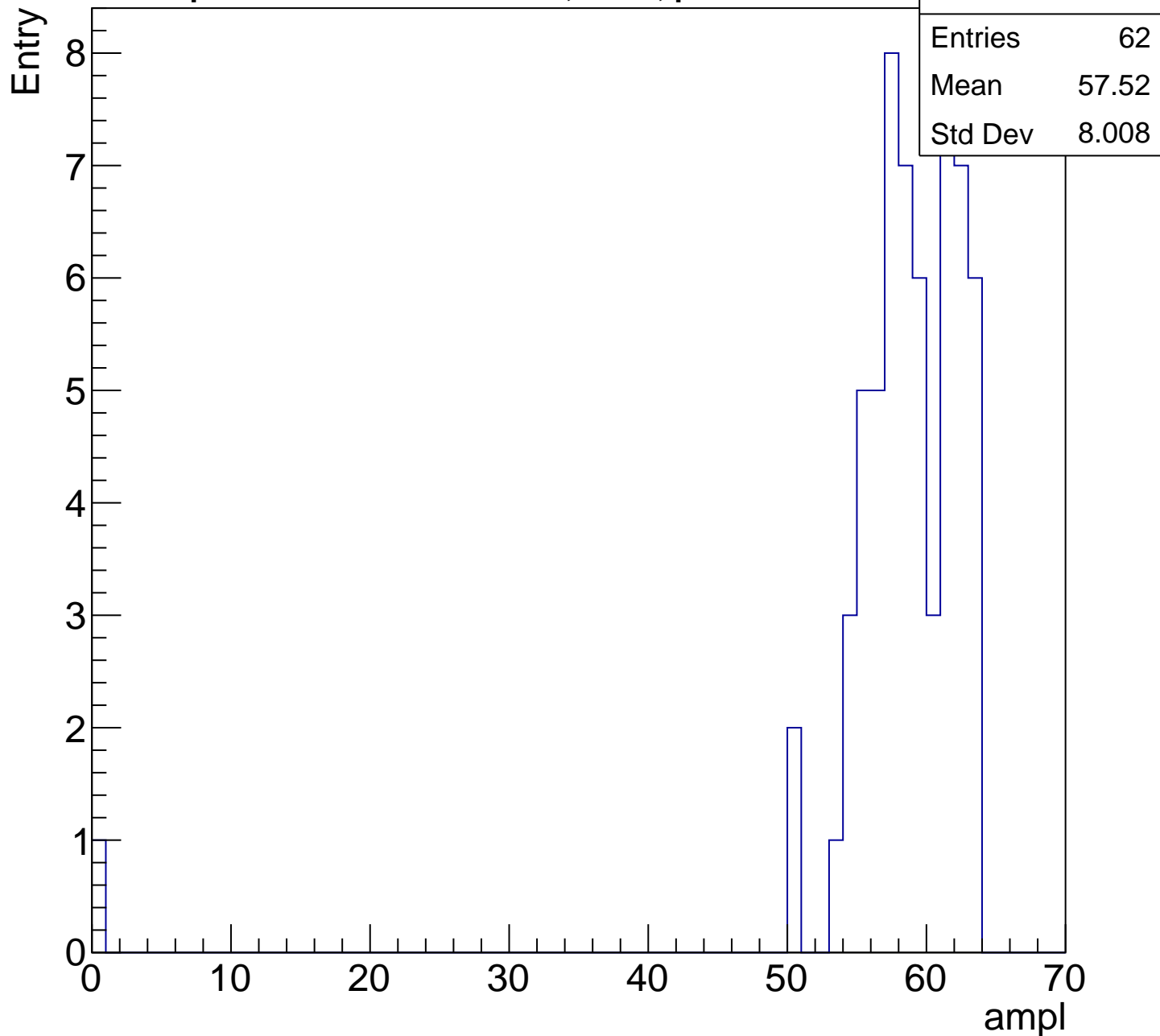
Entry

Entries	48
Mean	54.06
Std Dev	3.211



# B1L101S, U19-ch56, adc5

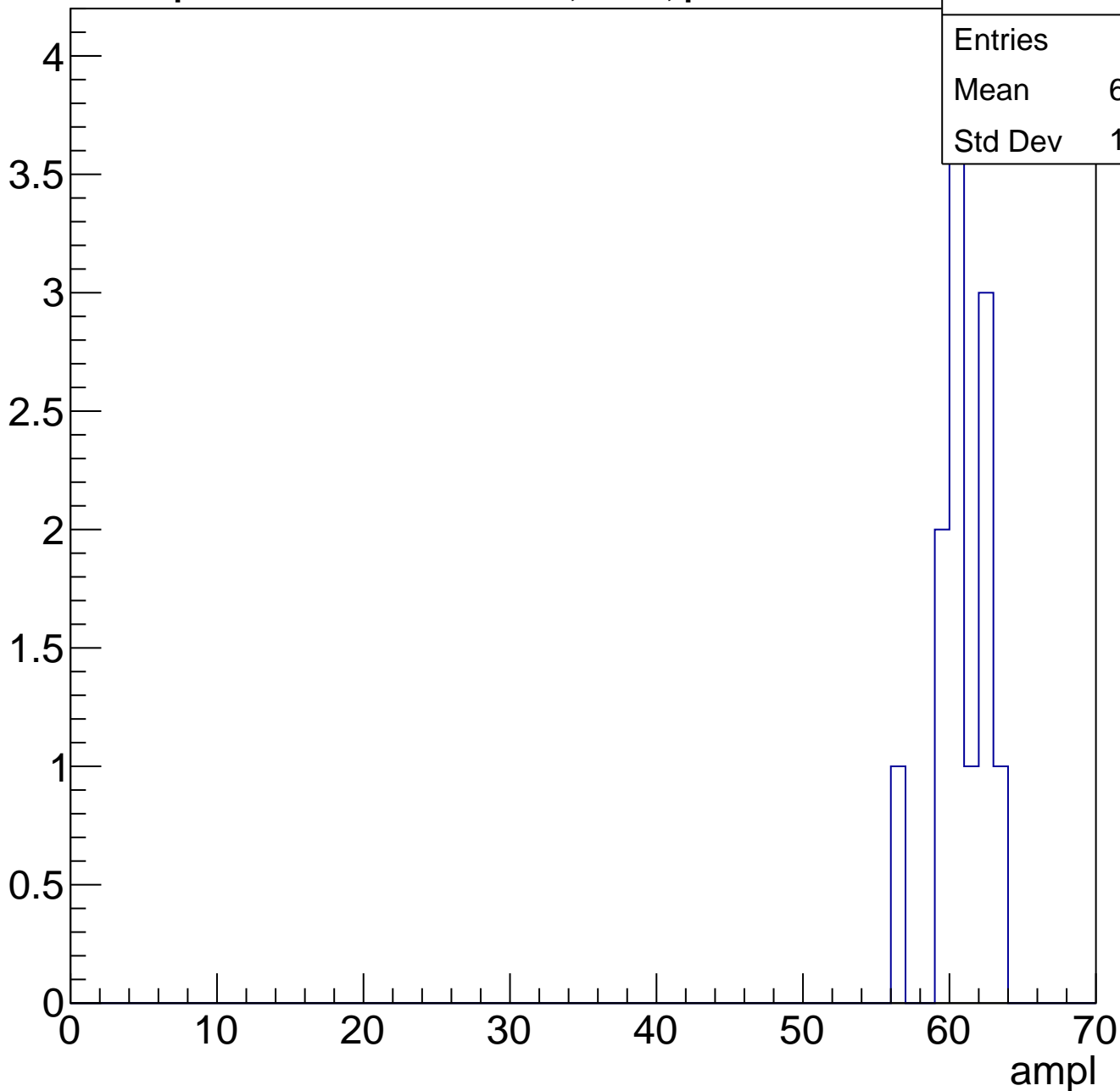
calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U19-ch56, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



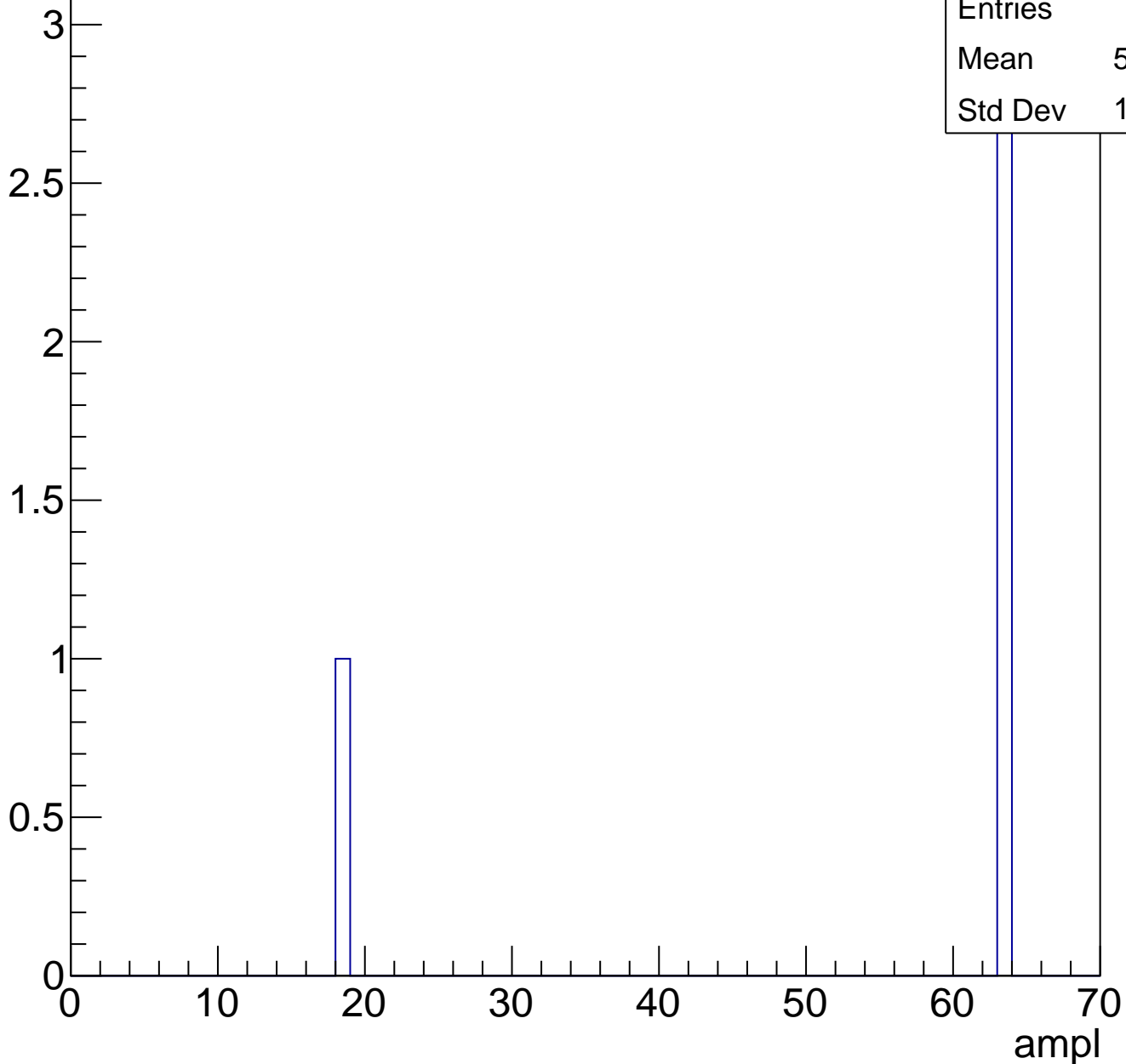
Entries	12
Mean	60.33
Std Dev	1.795



# B1L101S, U19-ch56, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U19-ch57, adc0

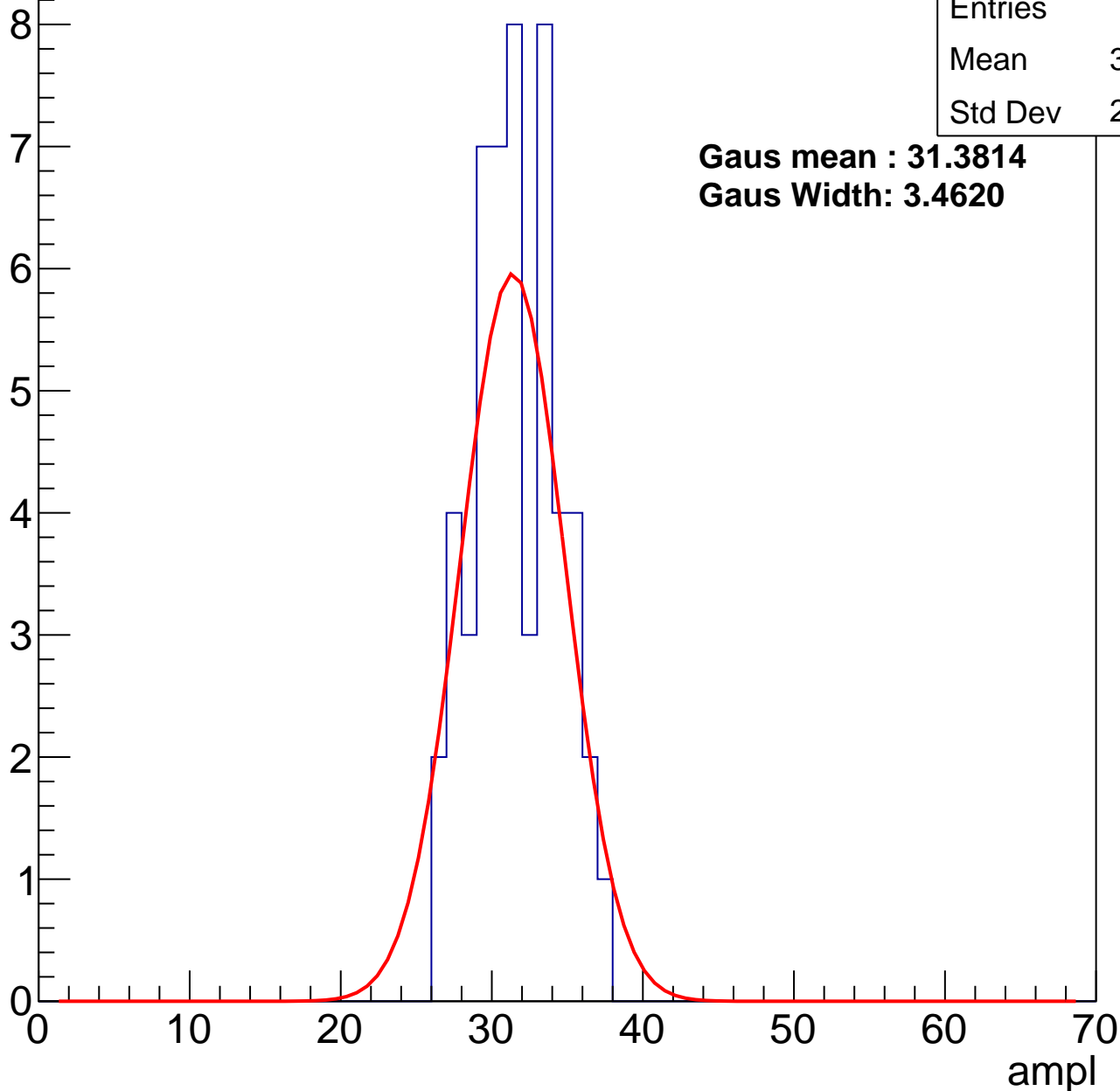
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	53
Mean	31.13
Std Dev	2.734

**Gaus mean : 31.3814**

**Gaus Width: 3.4620**



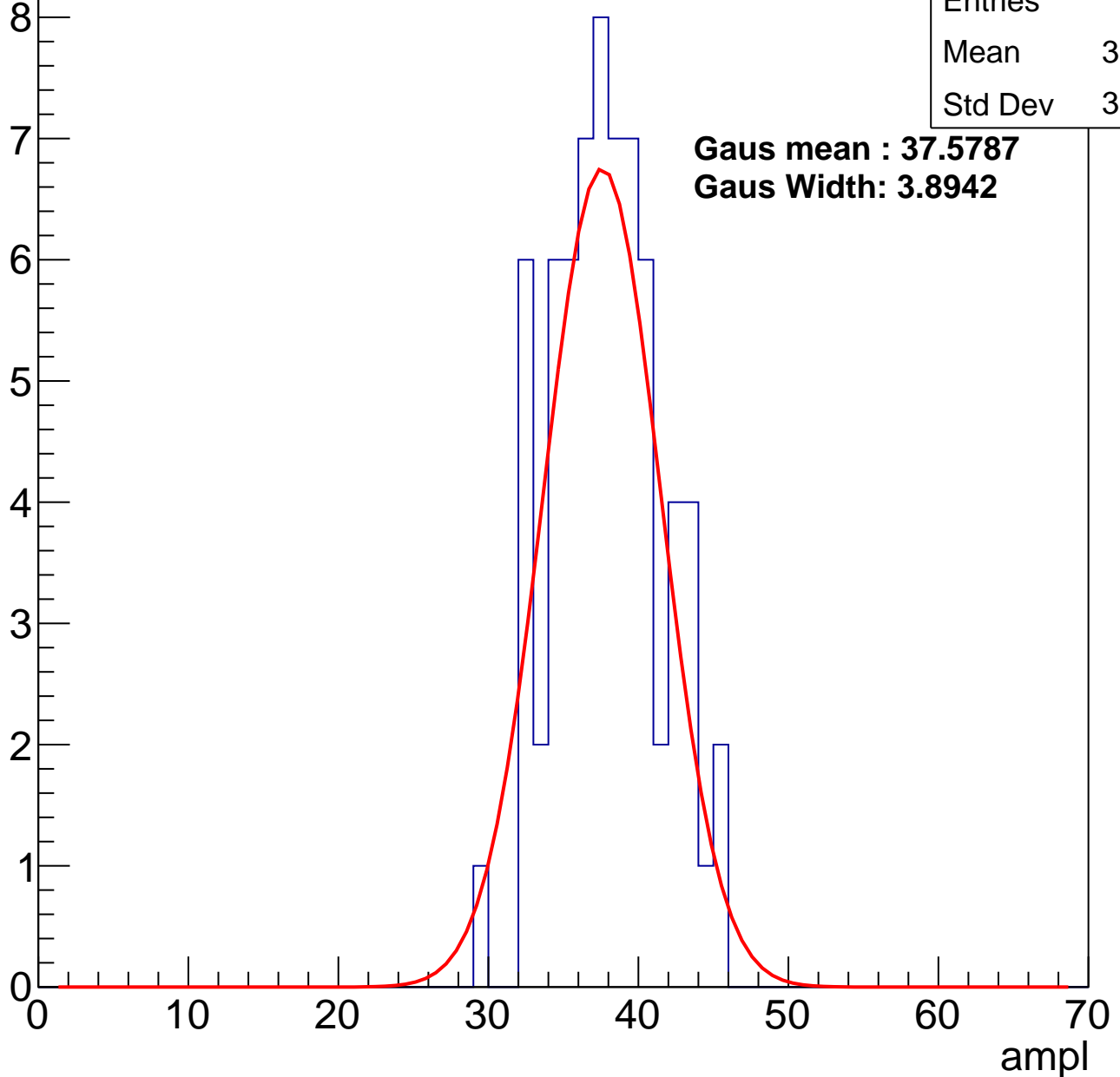
# B1L101S, U19-ch57, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	37.45
Std Dev	3.529

**Gaus mean : 37.5787**  
**Gaus Width: 3.8942**



# B1L101S, U19-ch57, adc2

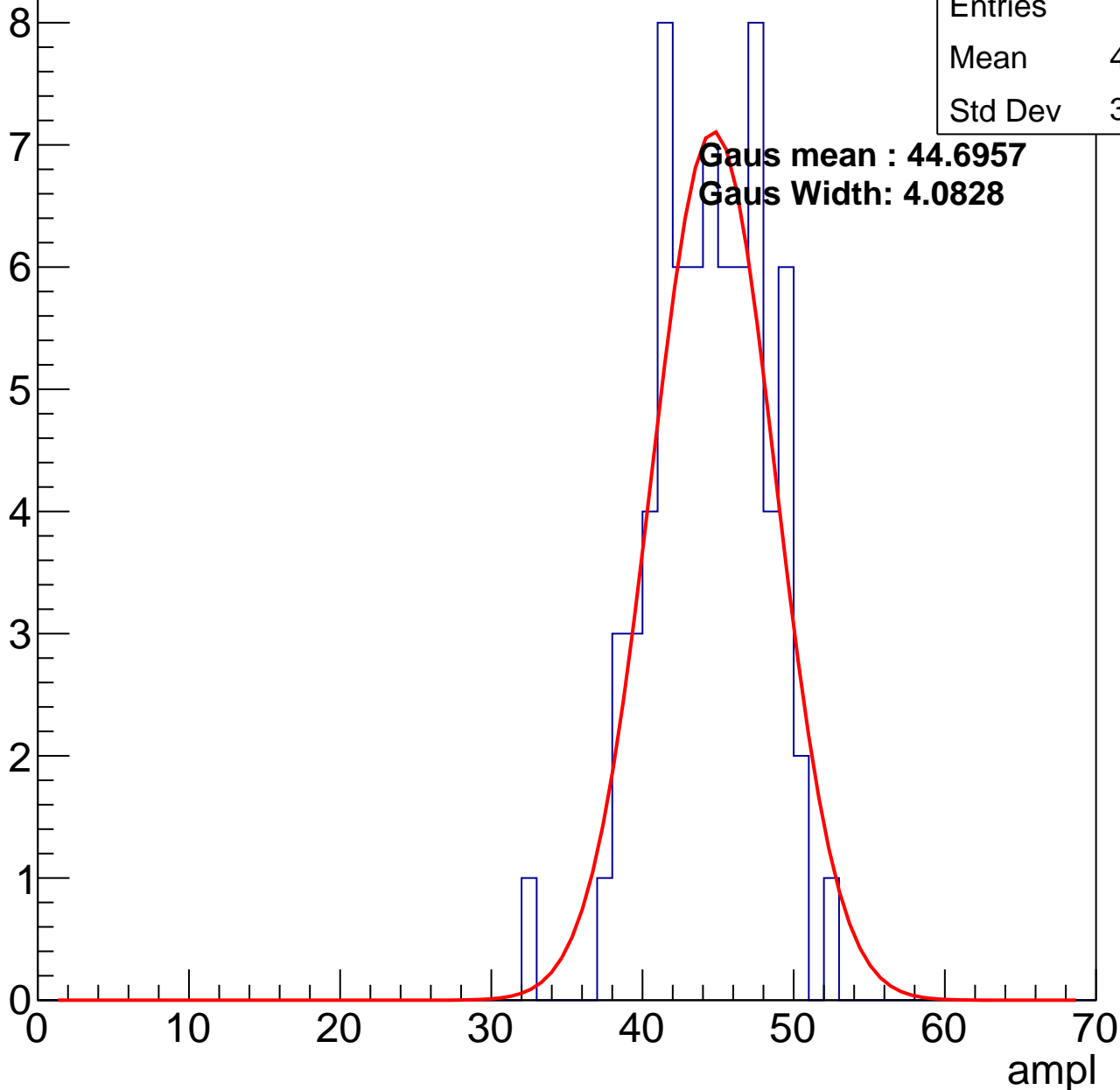
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	72
Mean	43.97
Std Dev	3.715

**Gaus mean : 44.6957**

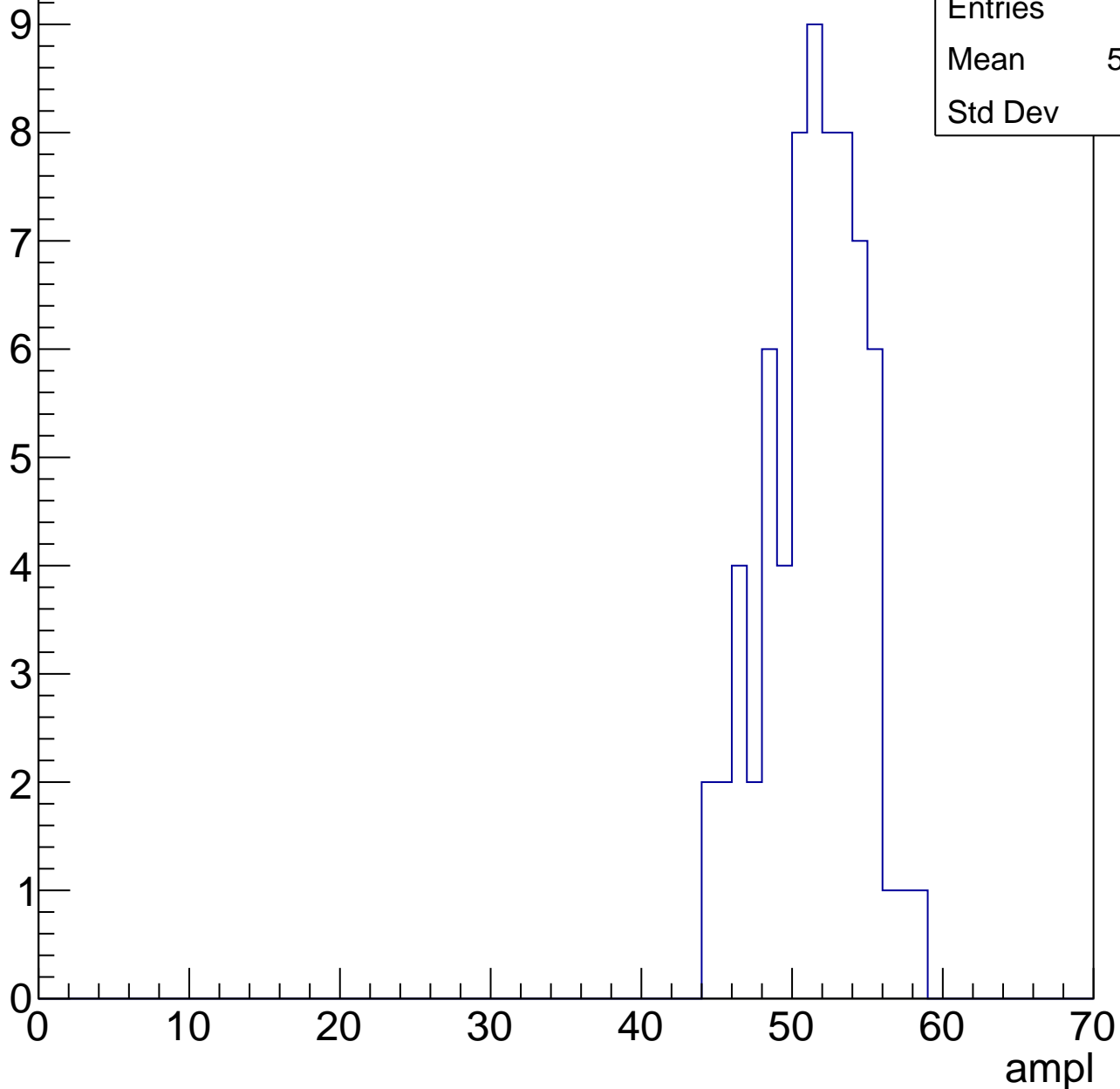
**Gaus Width: 4.0828**



# B1L101S, U19-ch57, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



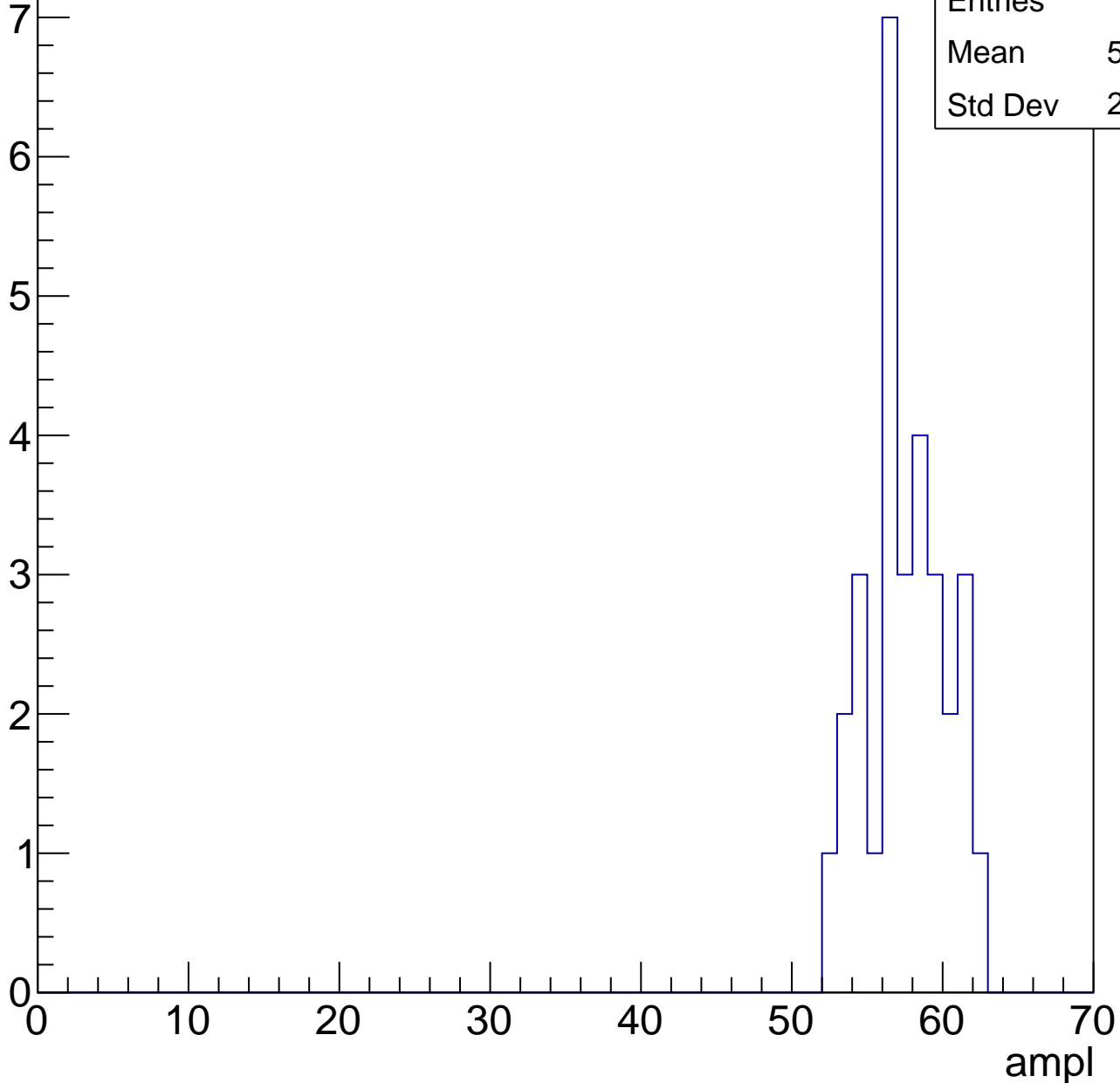
Entries	69
Mean	50.99
Std Dev	3.16

# B1L101S, U19-ch57, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	30
Mean	57.07
Std Dev	2.594



# B1L101S, U19-ch57, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	57
Mean	59.79
Std Dev	2.647

Entry

10

8

6

4

2

0

0

10

20

30

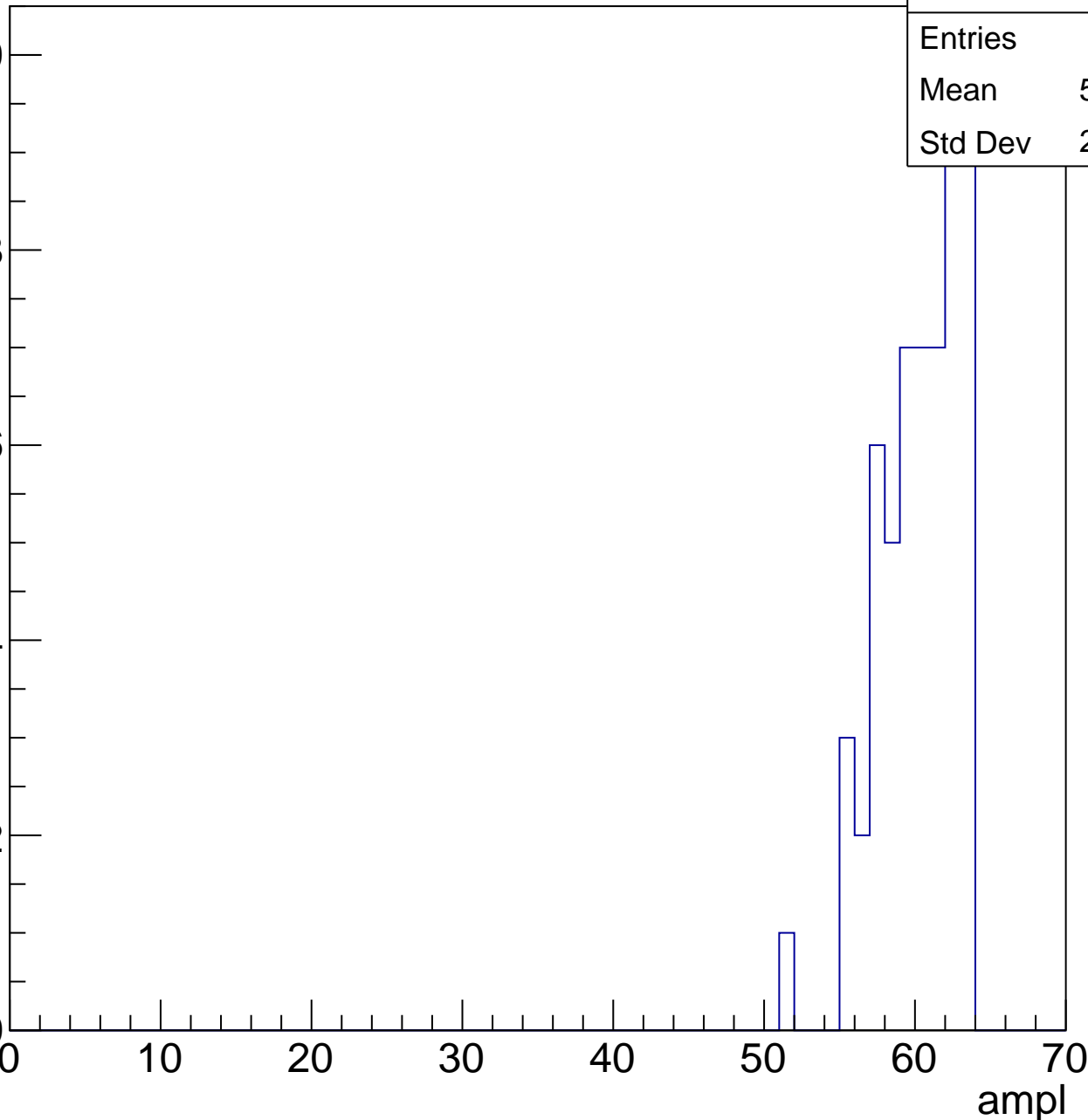
40

50

60

70

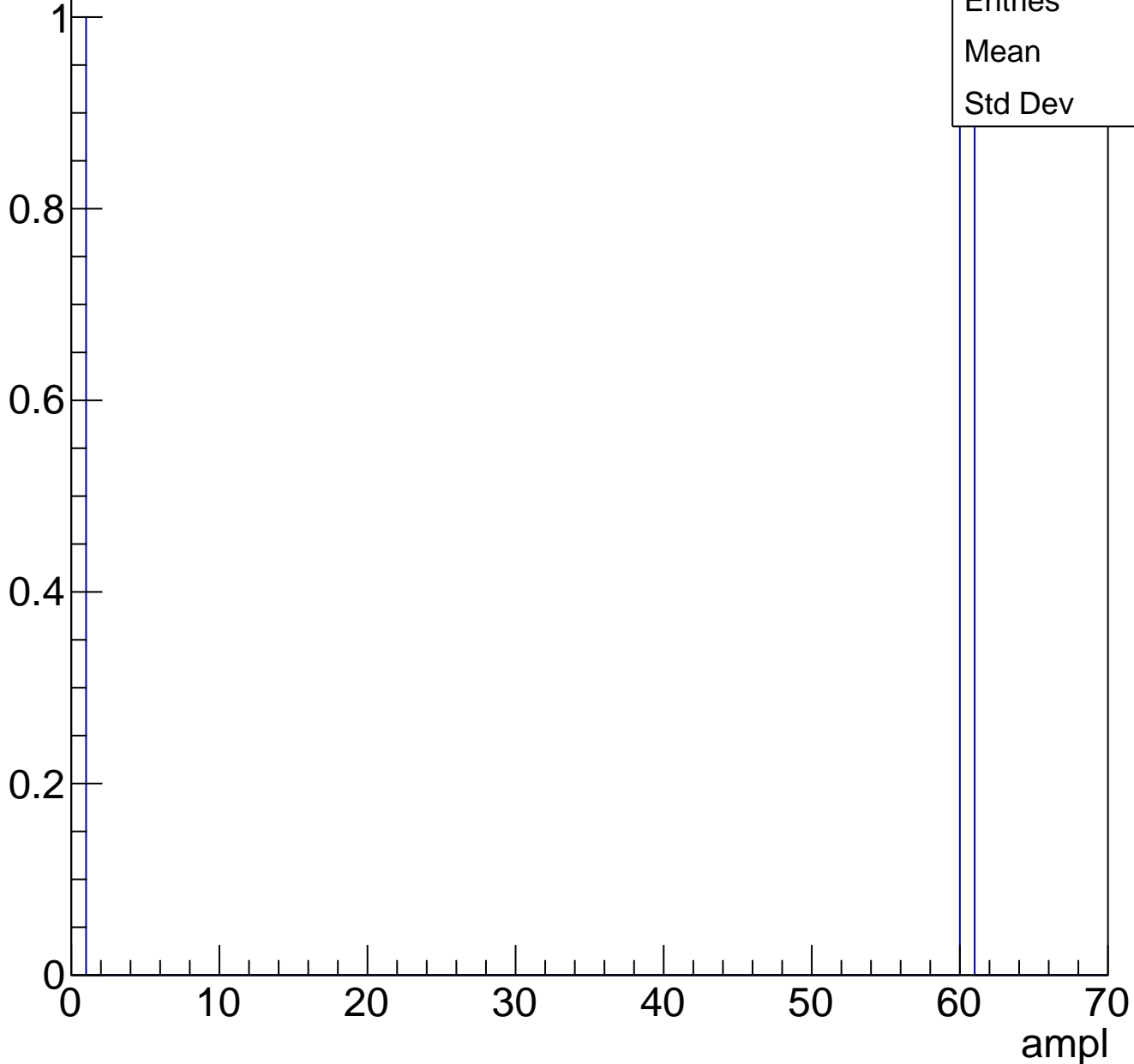
ampl



# B1L101S, U19-ch57, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U19-ch57, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U19-ch58, adc0

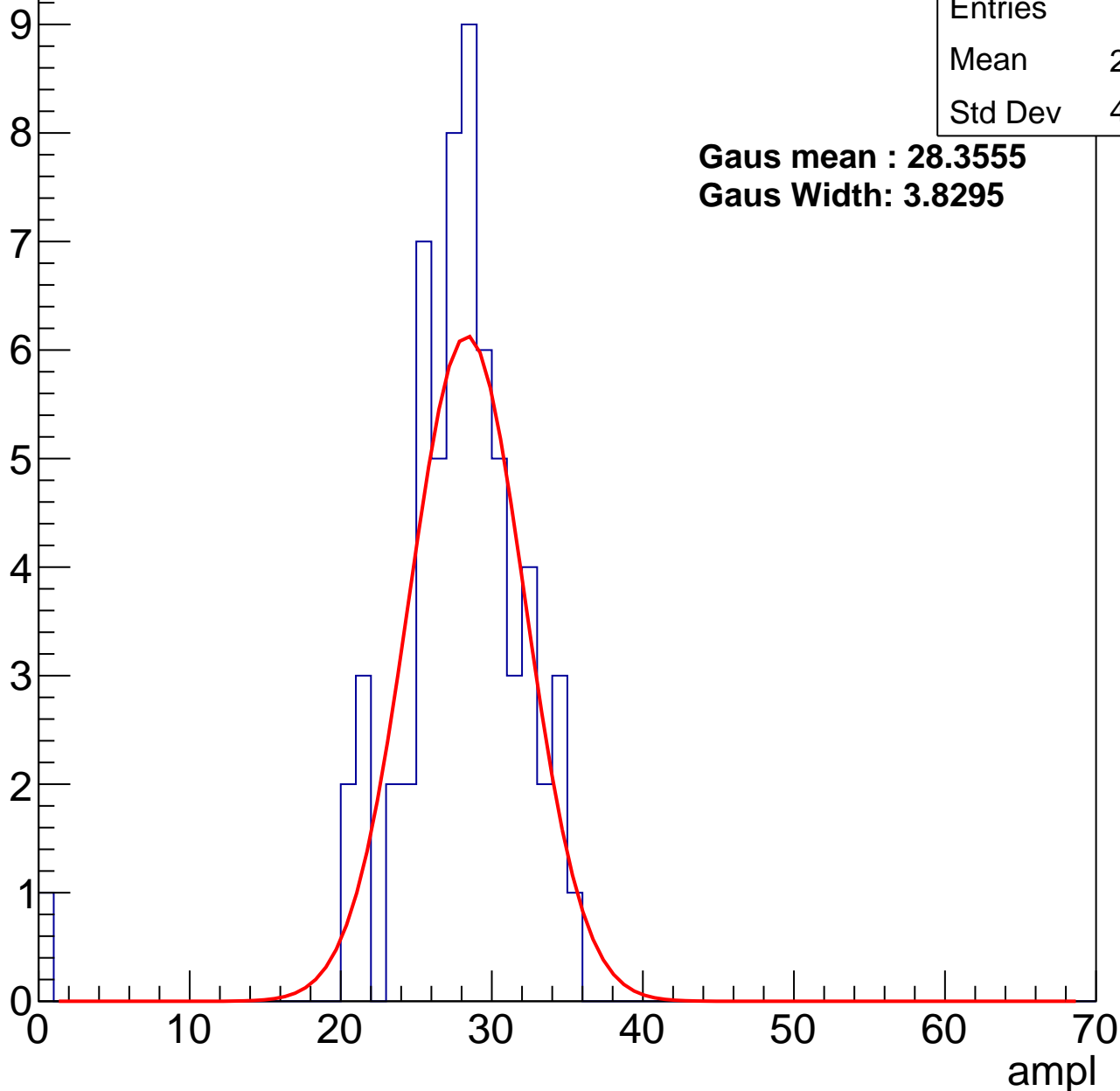
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	27.27
Std Dev	4.916

**Gaus mean : 28.3555**

**Gaus Width: 3.8295**



# B1L101S, U19-ch58, adc1

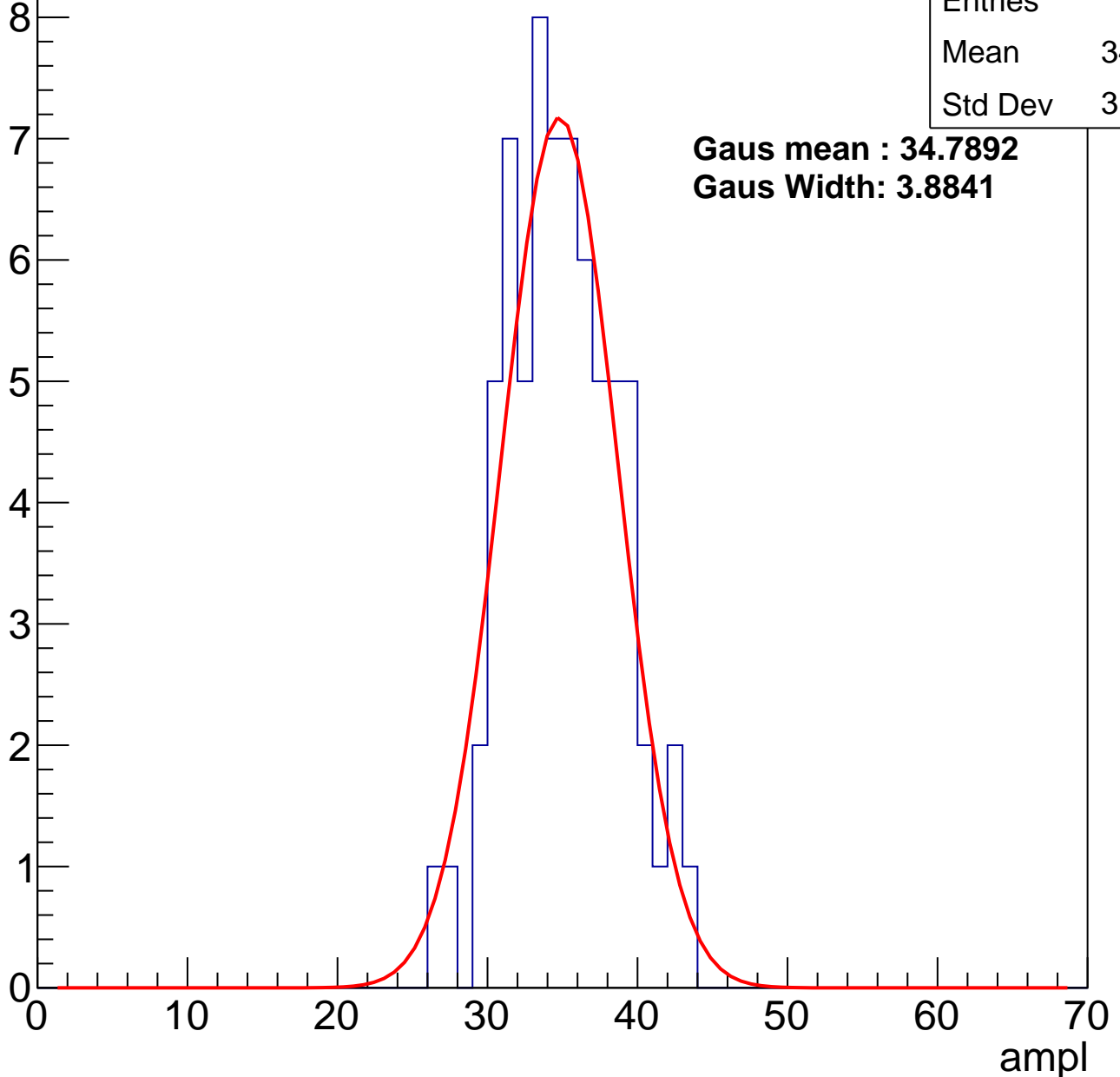
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	34.56
Std Dev	3.632

**Gaus mean : 34.7892**

**Gaus Width: 3.8841**



# B1L101S, U19-ch58, adc2

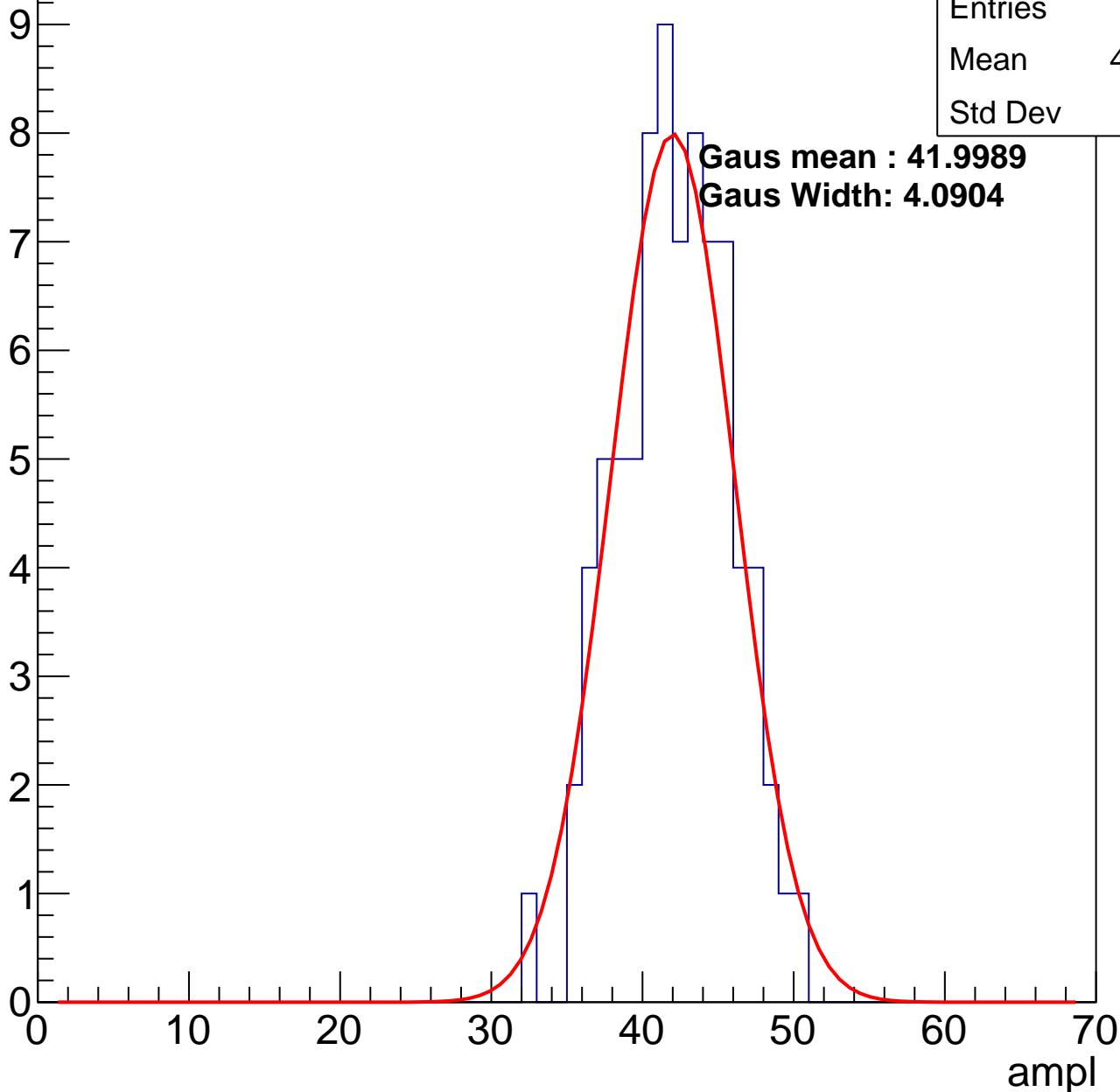
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	80
Mean	41.66
Std Dev	3.66

**Gaus mean : 41.9989**

**Gaus Width: 4.0904**

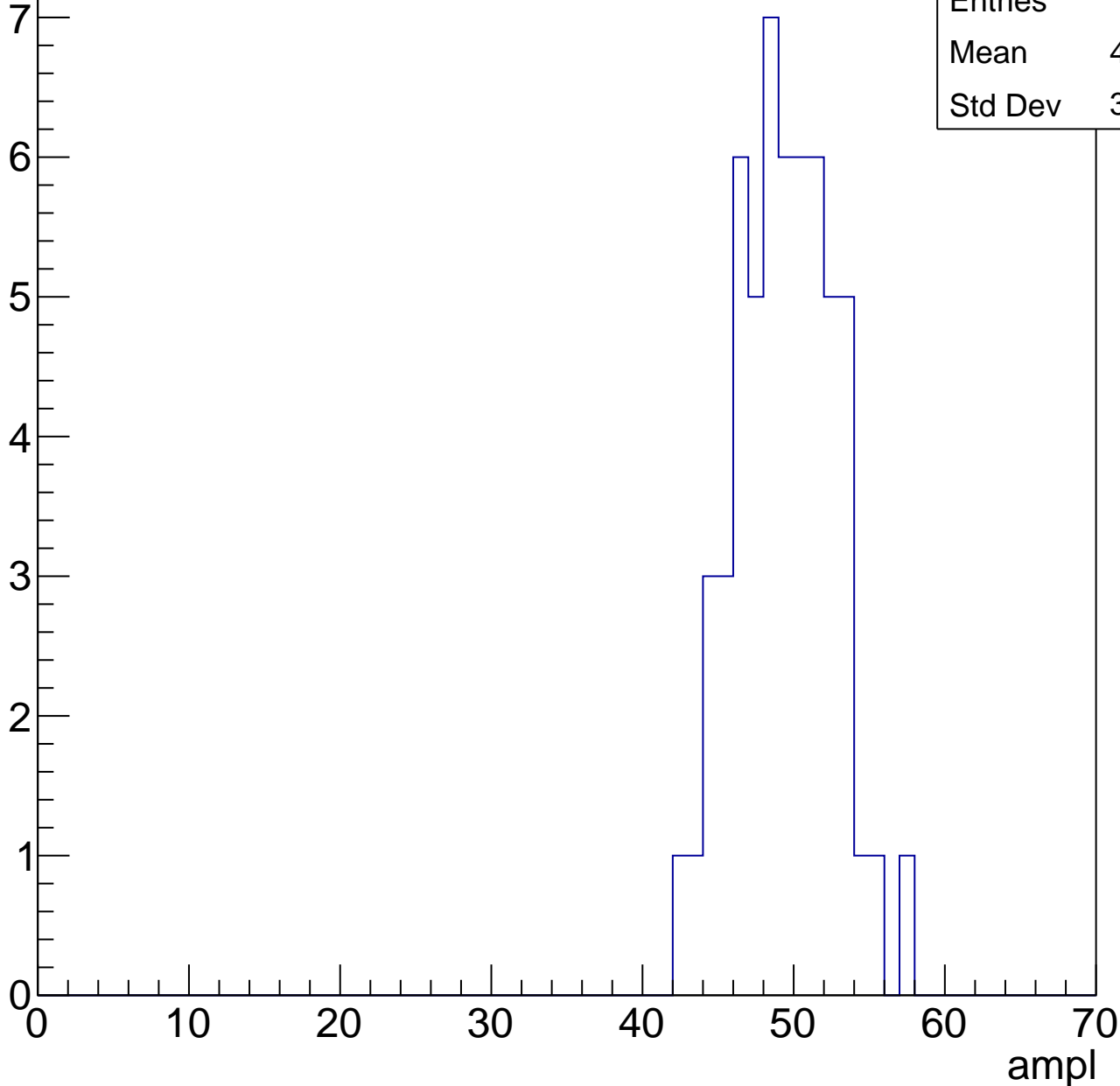


# B1L101S, U19-ch58, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	57
Mean	48.95
Std Dev	3.159

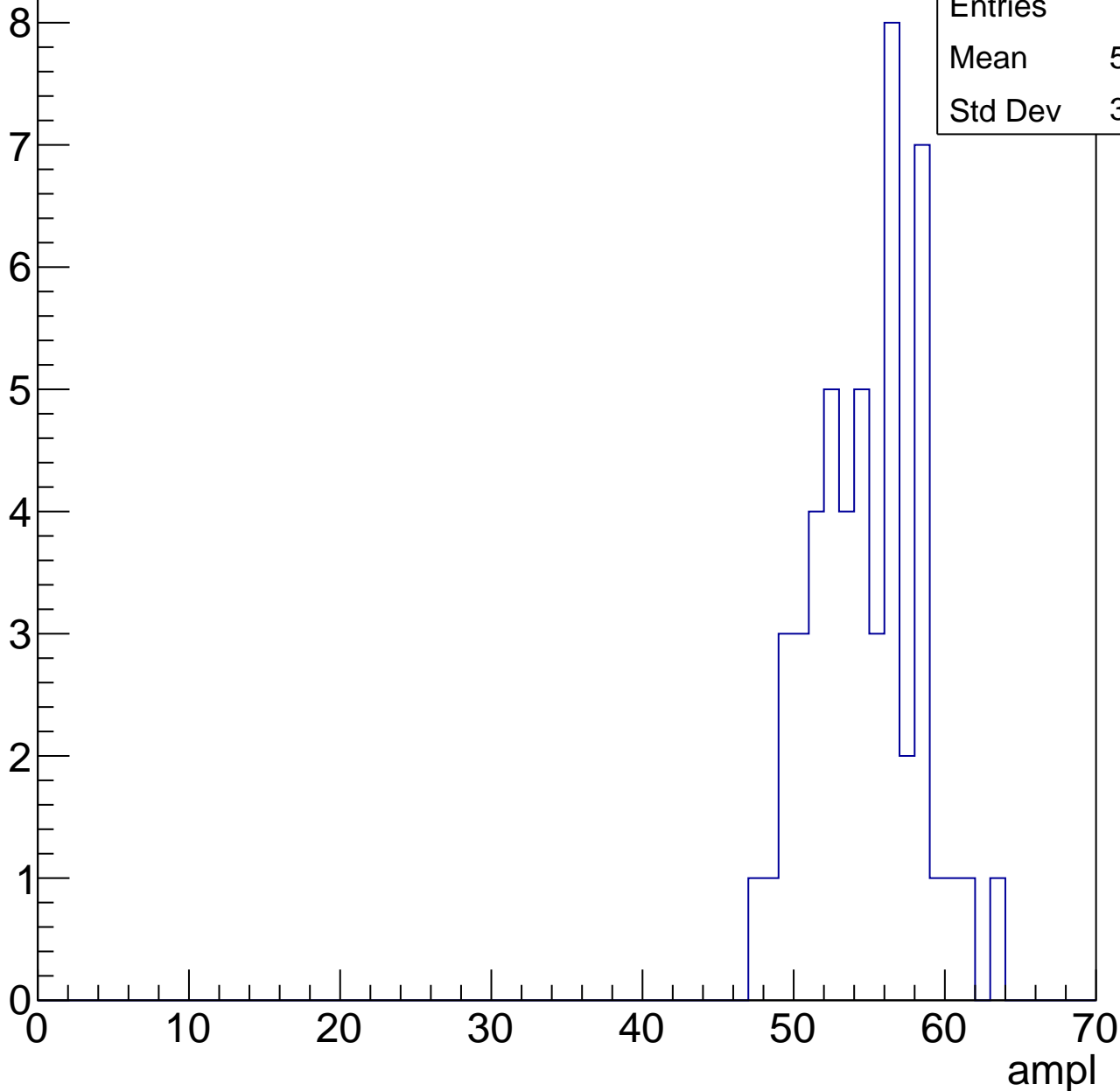


# B1L101S, U19-ch58, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	50
Mean	54.28
Std Dev	3.522



# B1L101S, U19-ch58, adc5

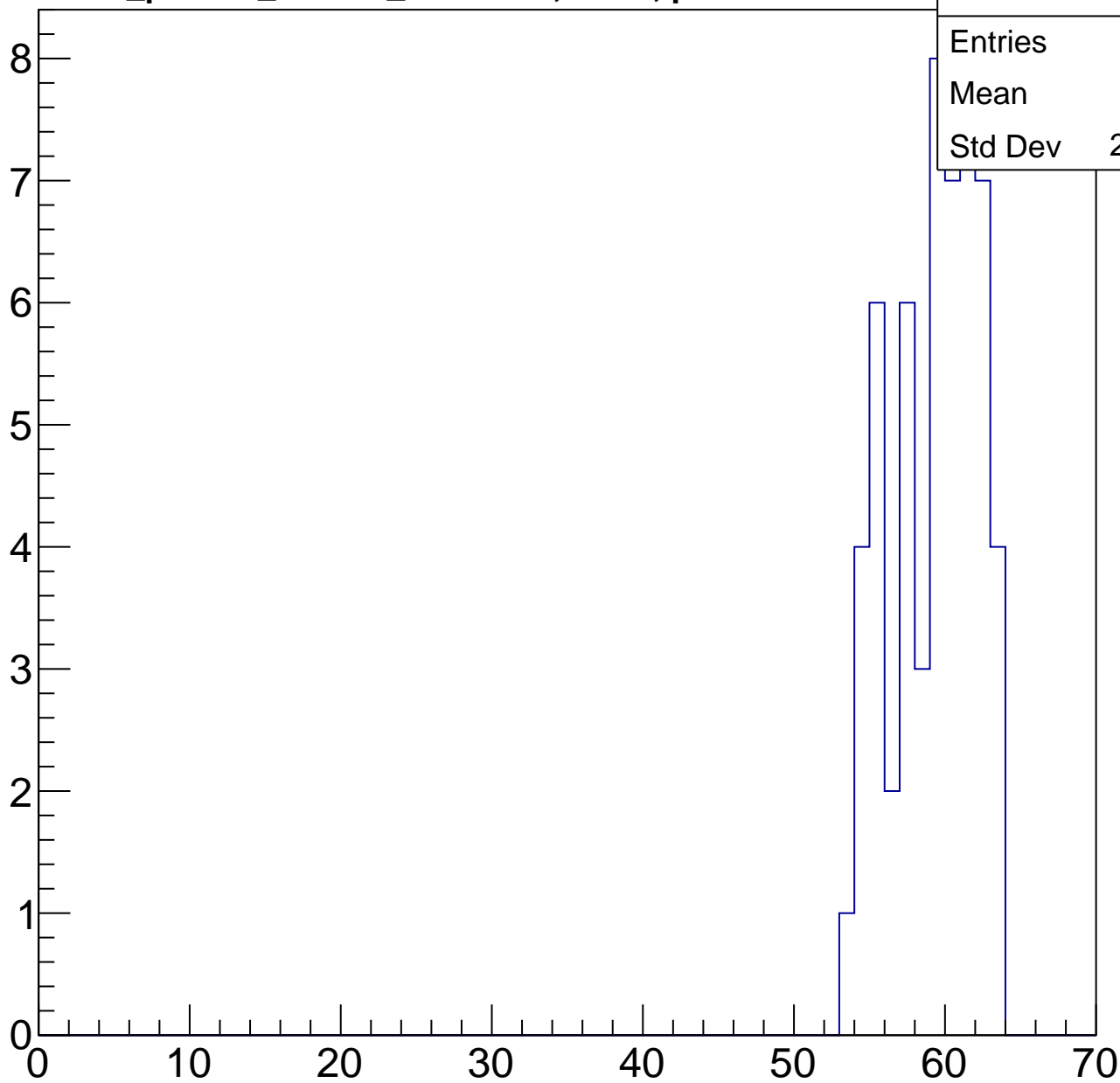
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	56
Mean	58.8
Std Dev	2.806

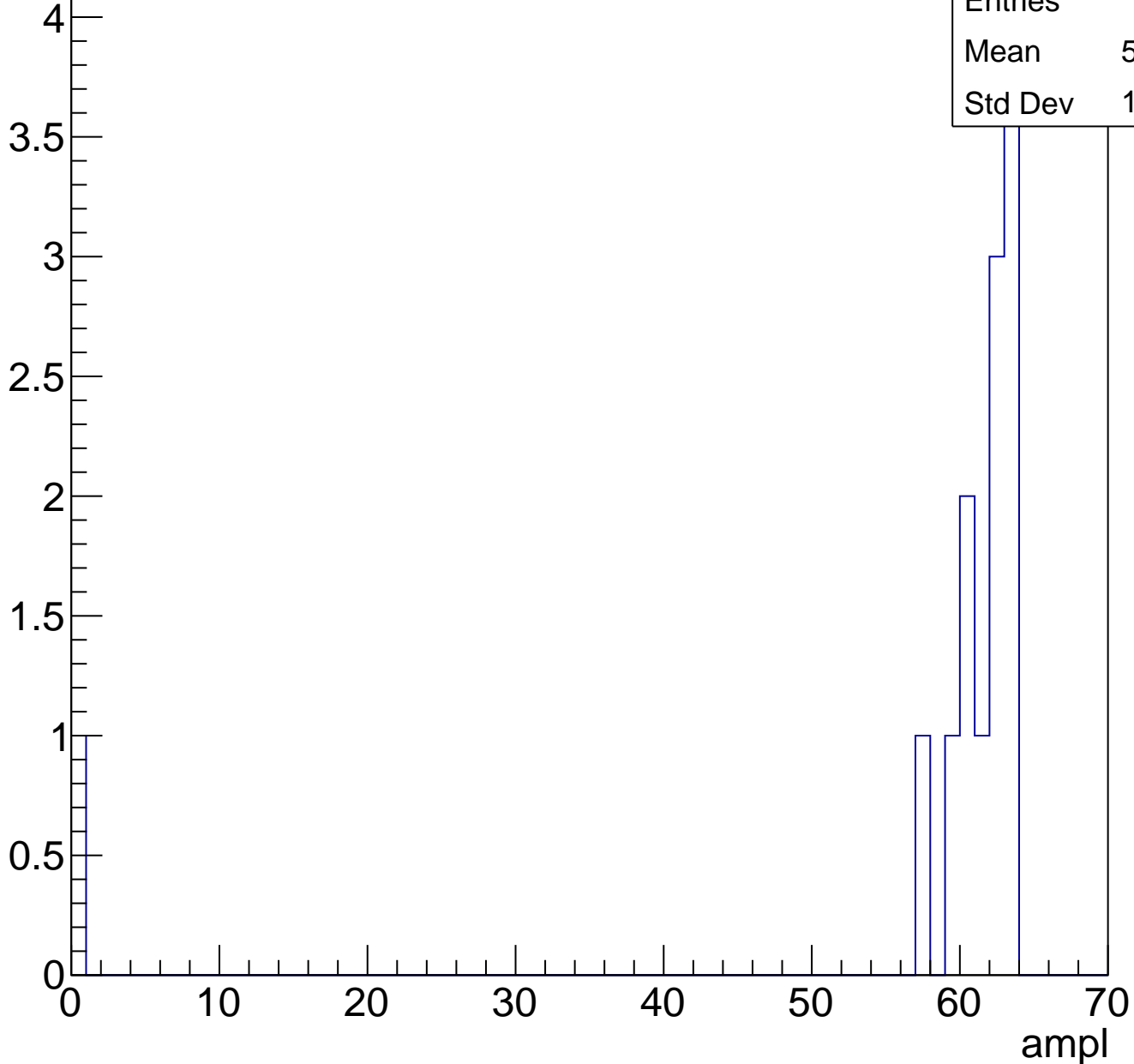
ampl



# B1L101S, U19-ch58, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U19-ch58, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U19-ch59, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	71
Mean	29.73
Std Dev	3.108

**Gaus mean : 31.1270**

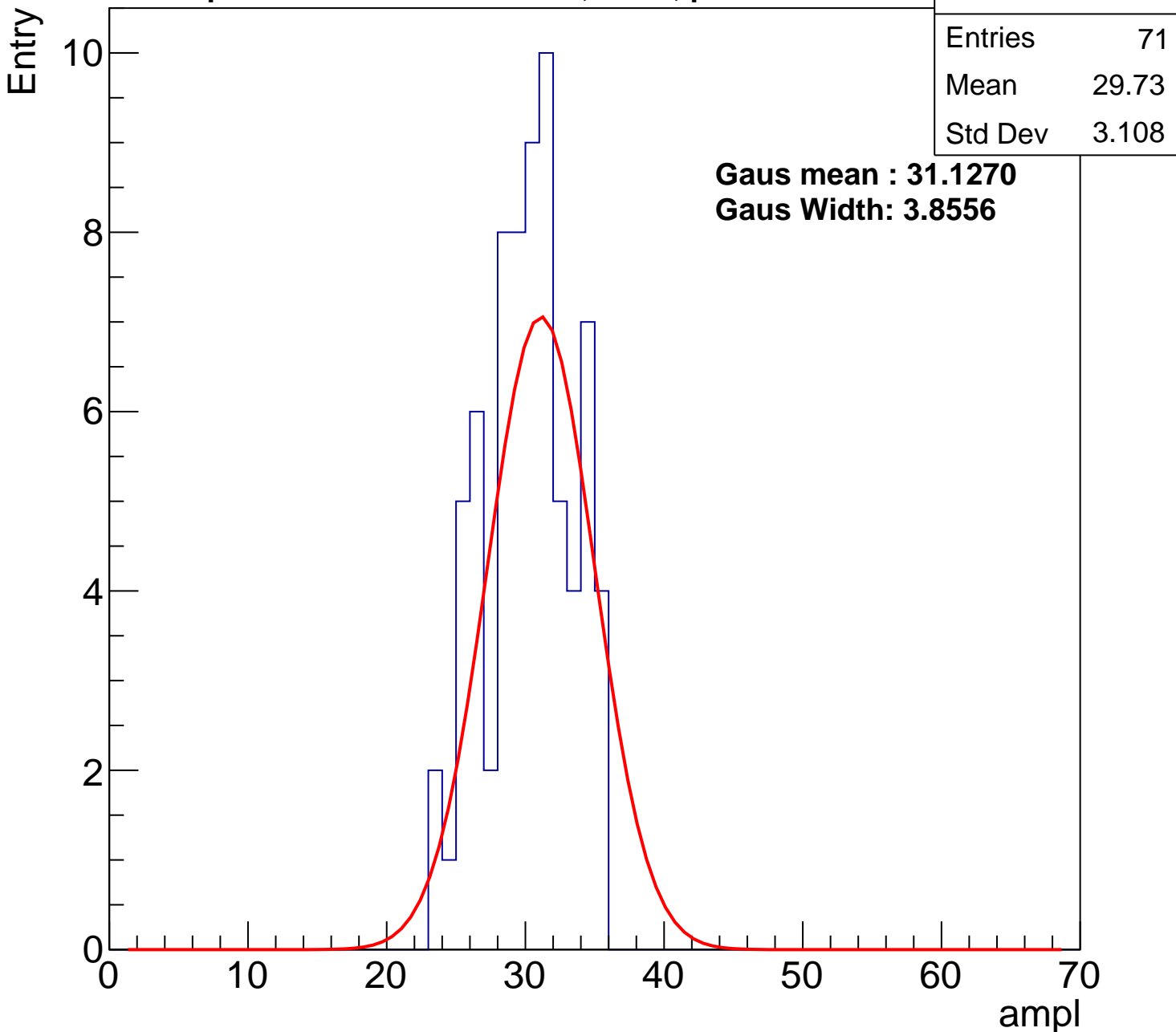
**Gaus Width: 3.8556**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U19-ch59, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	74
Mean	37.19
Std Dev	3.368

**Gaus mean : 37.6382**

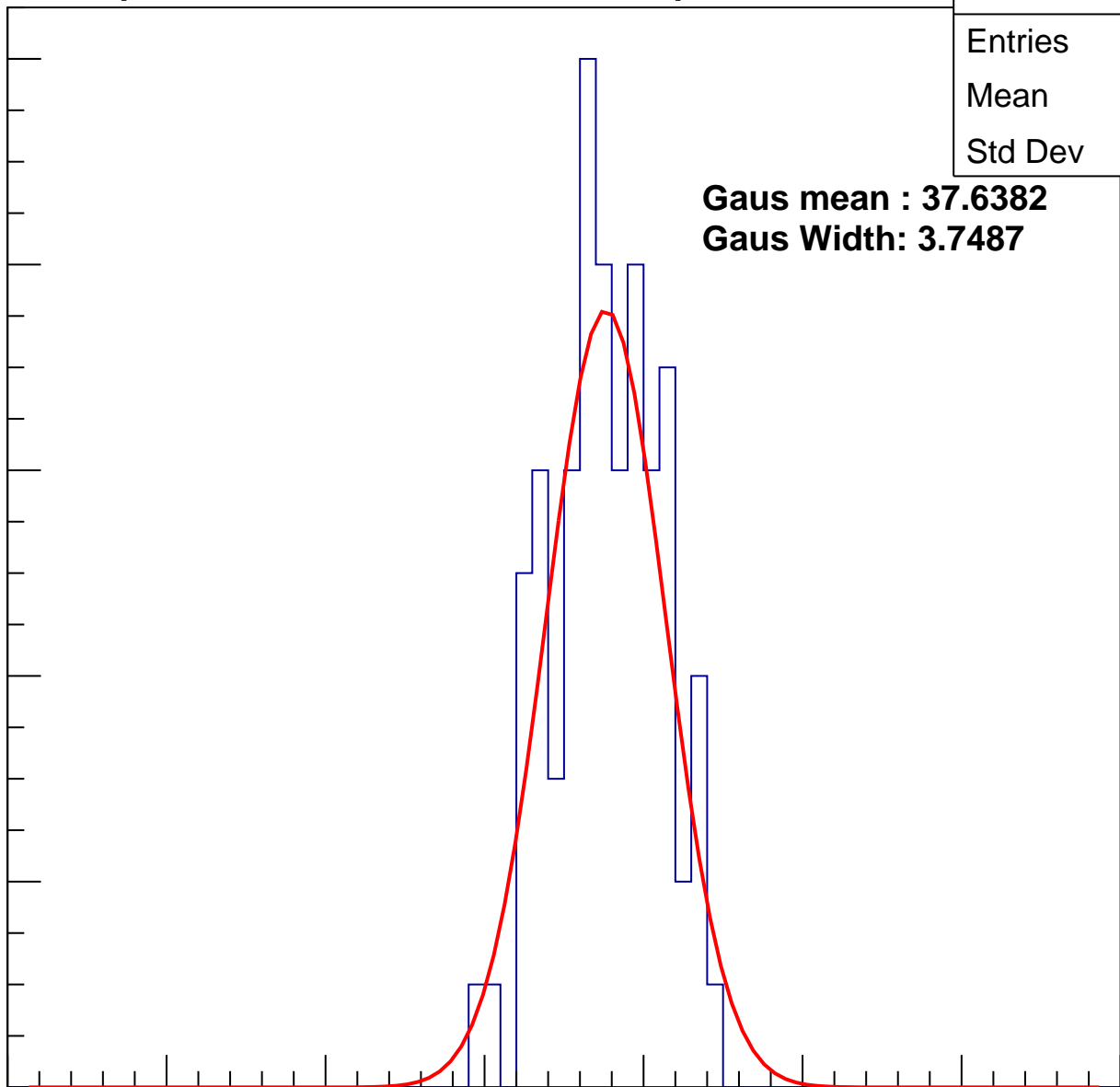
**Gaus Width: 3.7487**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U19-ch59, adc2

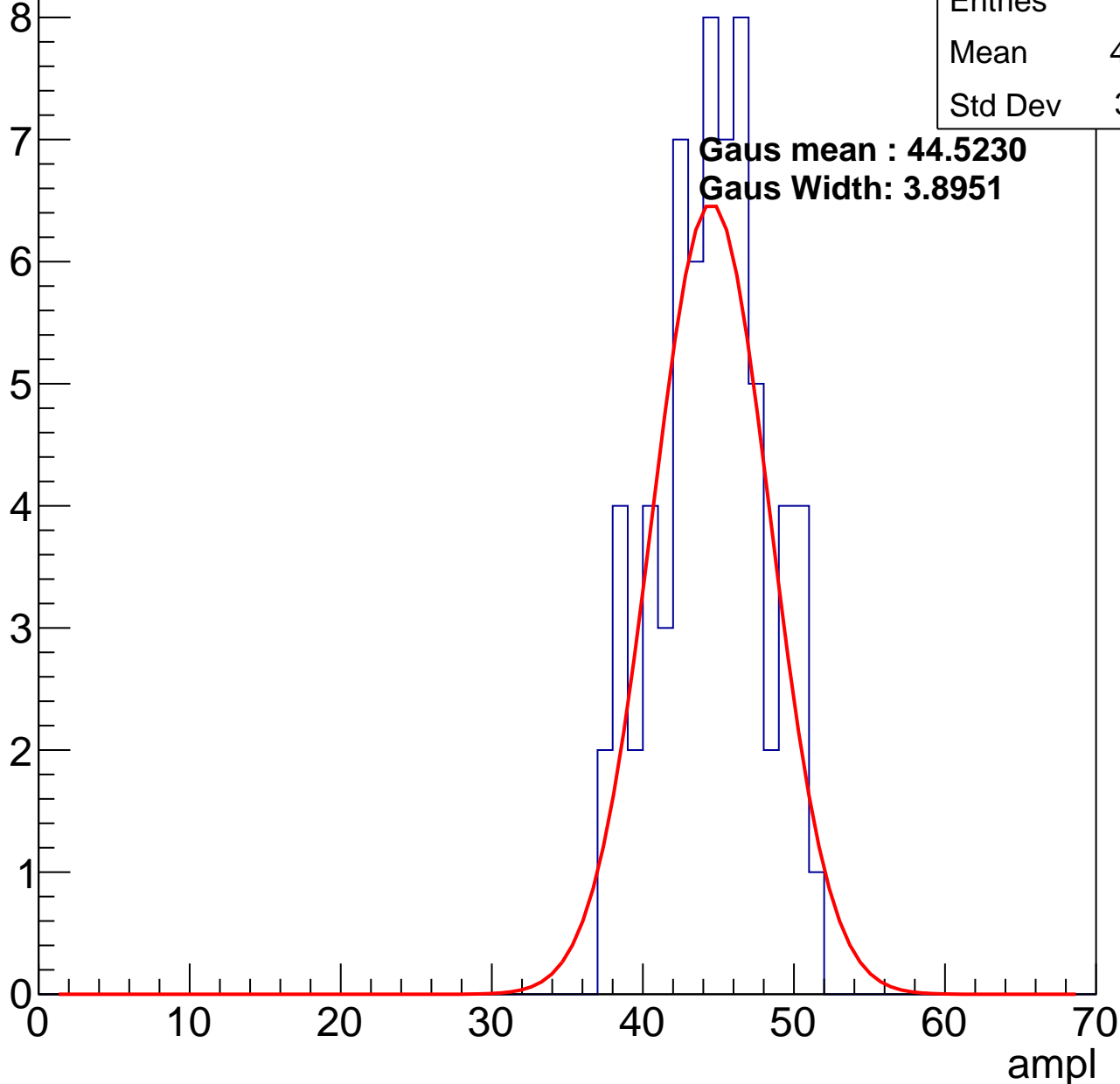
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	67
Mean	44.06
Std Dev	3.511

**Gaus mean : 44.5230**

**Gaus Width: 3.8951**

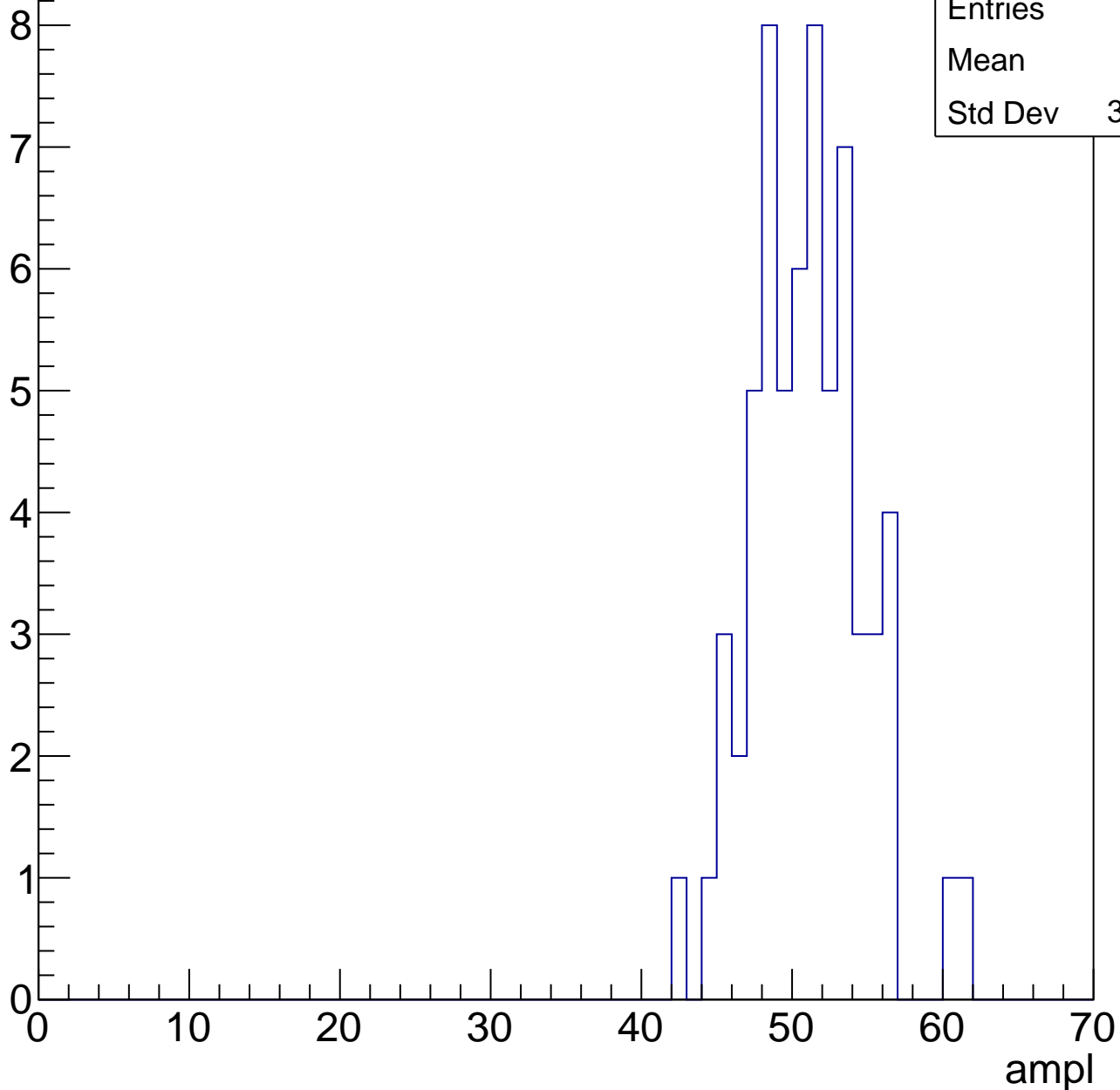


# B1L101S, U19-ch59, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

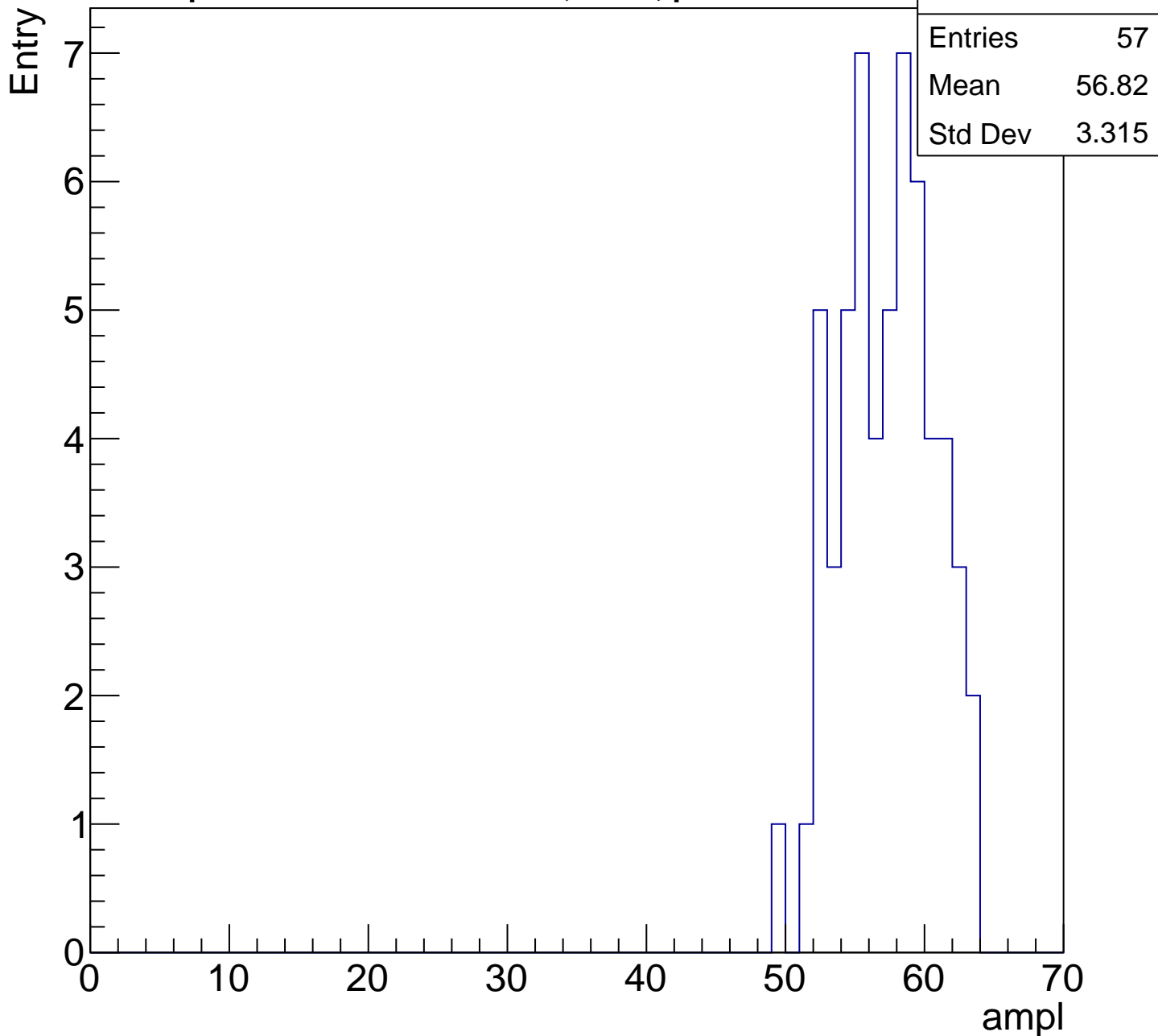
Entry

Entries	63
Mean	50.6
Std Dev	3.663



# B1L101S, U19-ch59, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

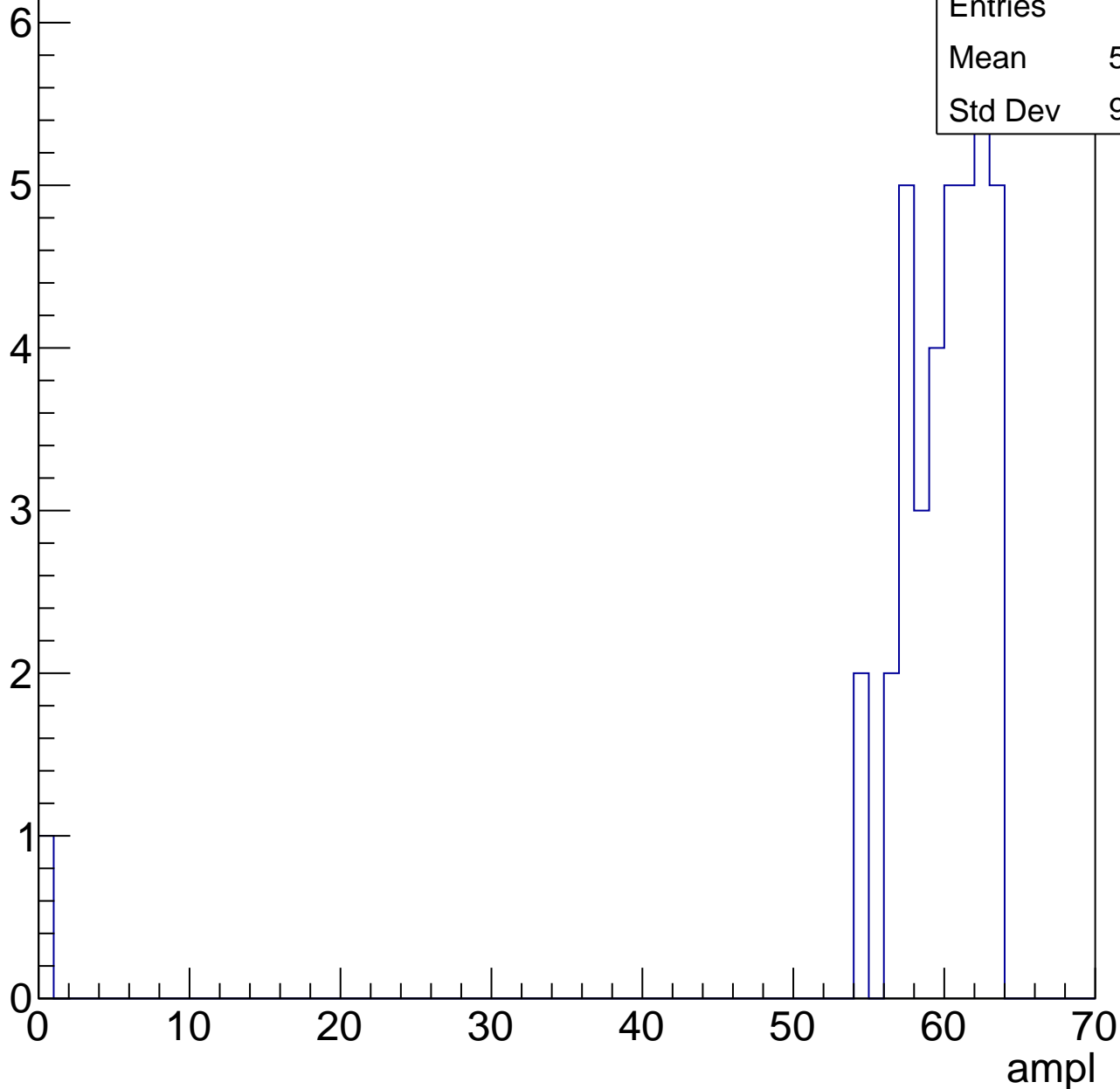


# B1L101S, U19-ch59, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	38
Mean	58.08
Std Dev	9.866



# B1L101S, U19-ch59, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

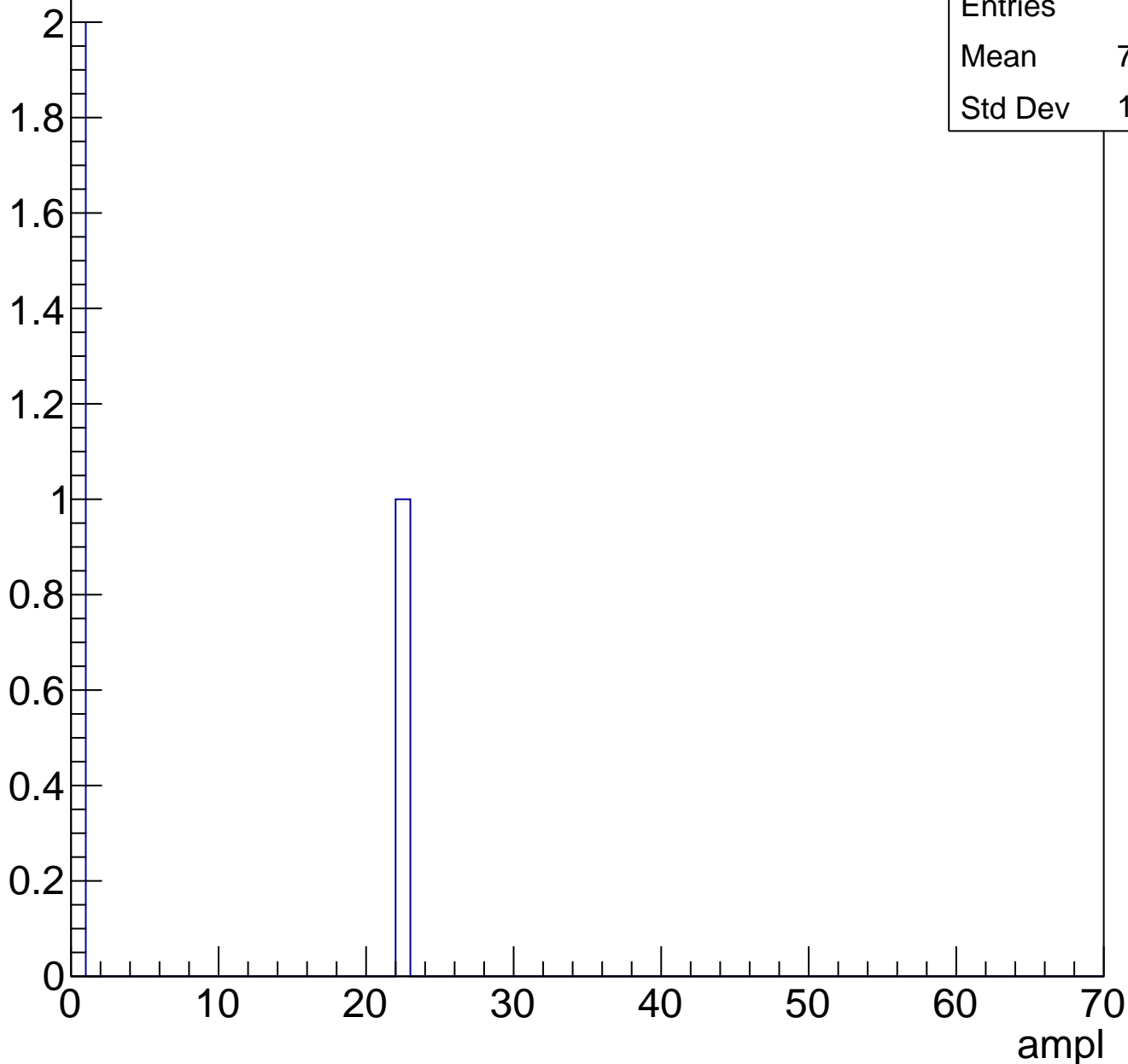




# B1L101S, U19-ch59, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U19-ch60, adc0

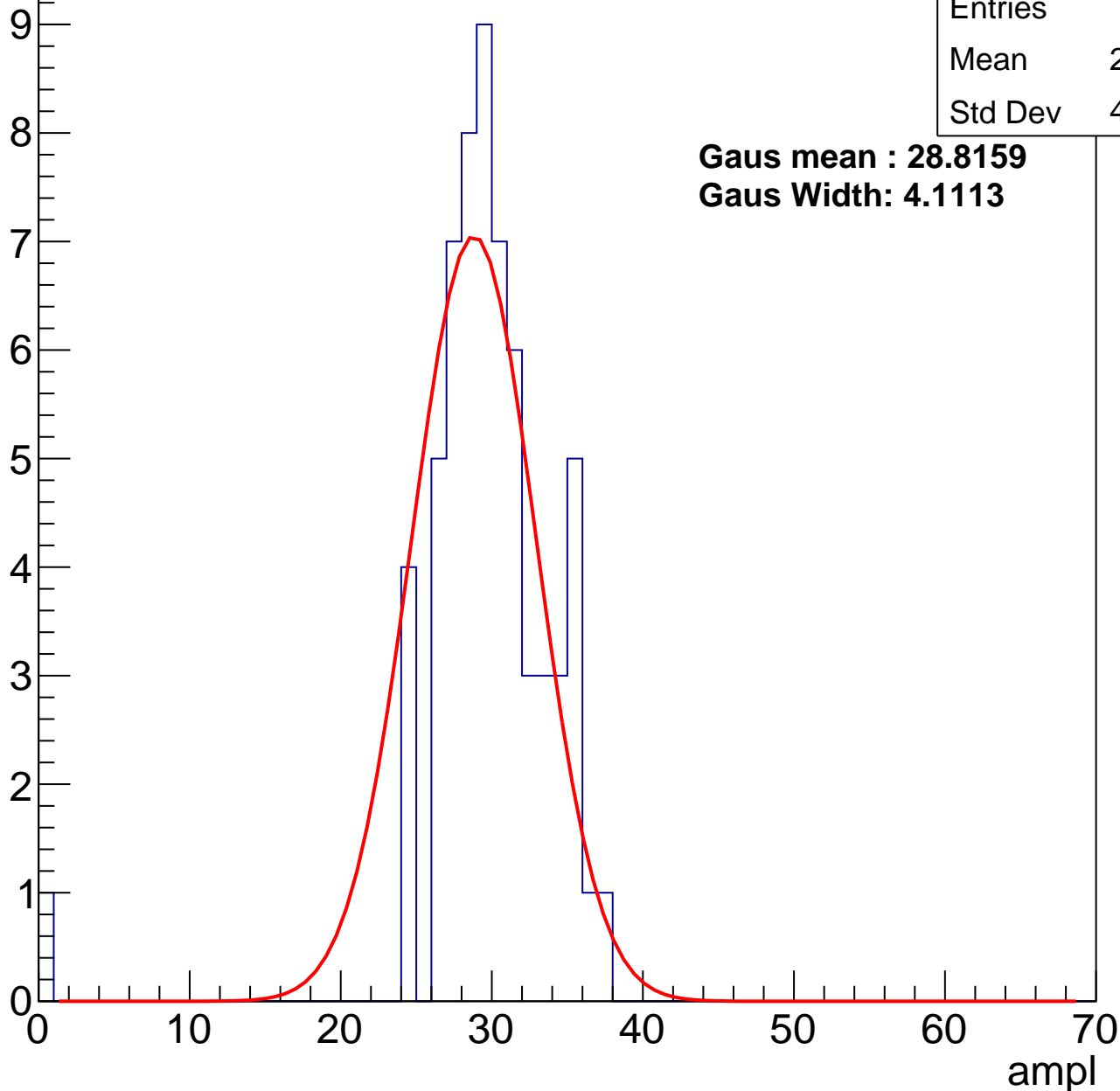
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	29.22
Std Dev	4.868

**Gaus mean : 28.8159**

**Gaus Width: 4.1113**



# B1L101S, U19-ch60, adc1

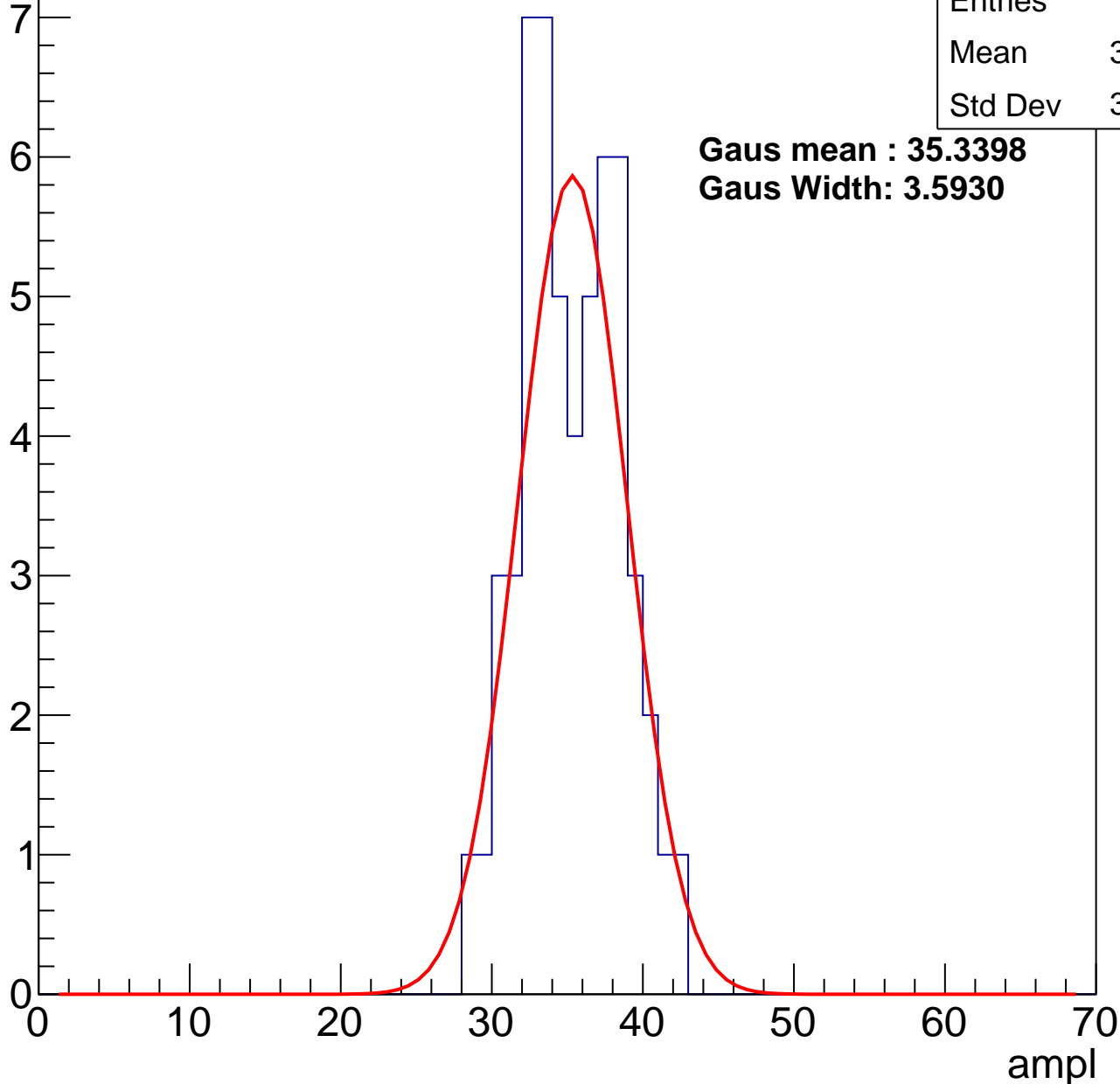
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	55
Mean	34.82
Std Dev	3.214

**Gaus mean : 35.3398**

**Gaus Width: 3.5930**



# B1L101S, U19-ch60, adc2

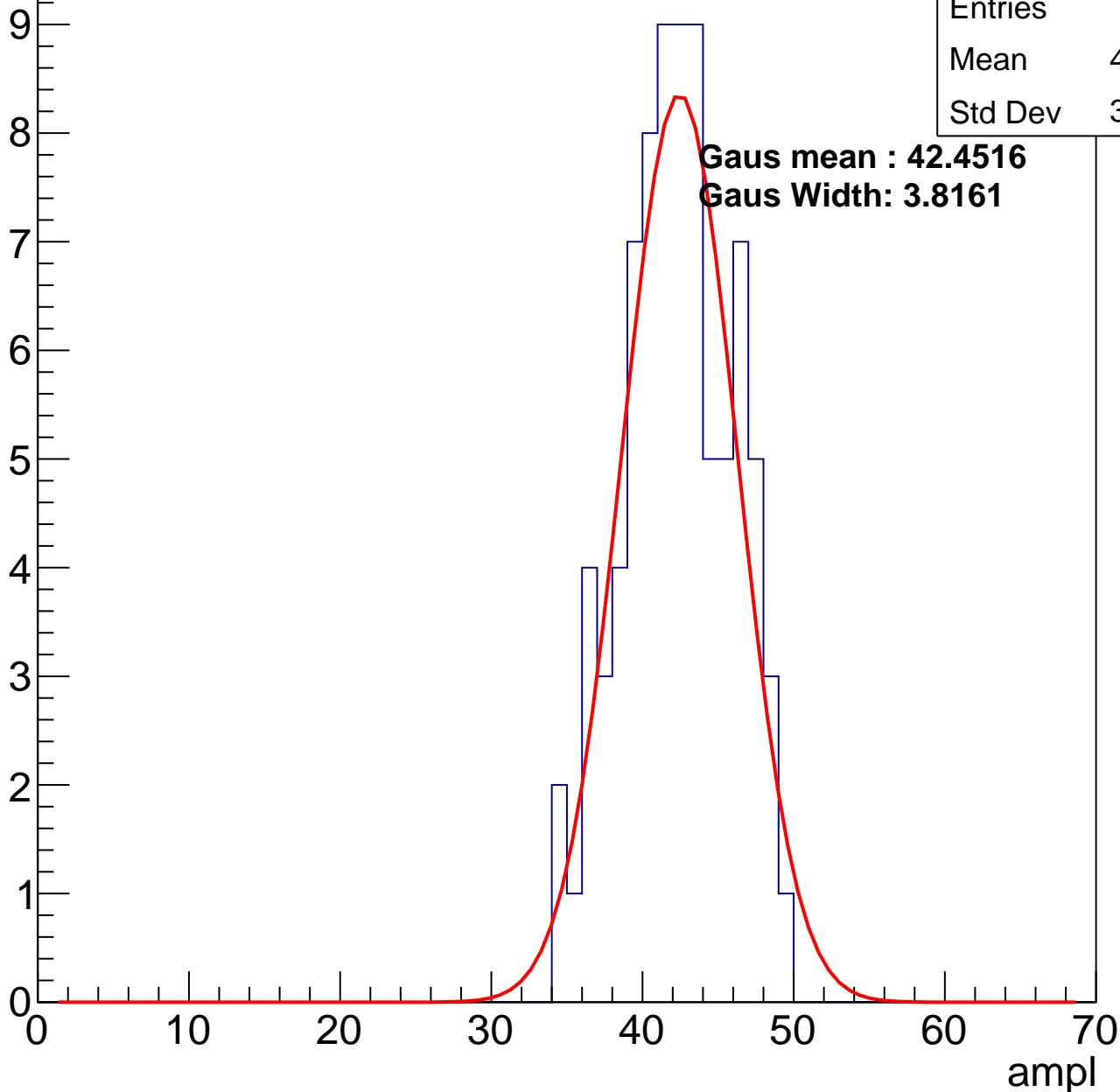
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	82
Mean	41.85
Std Dev	3.545

**Gaus mean : 42.4516**

**Gaus Width: 3.8161**

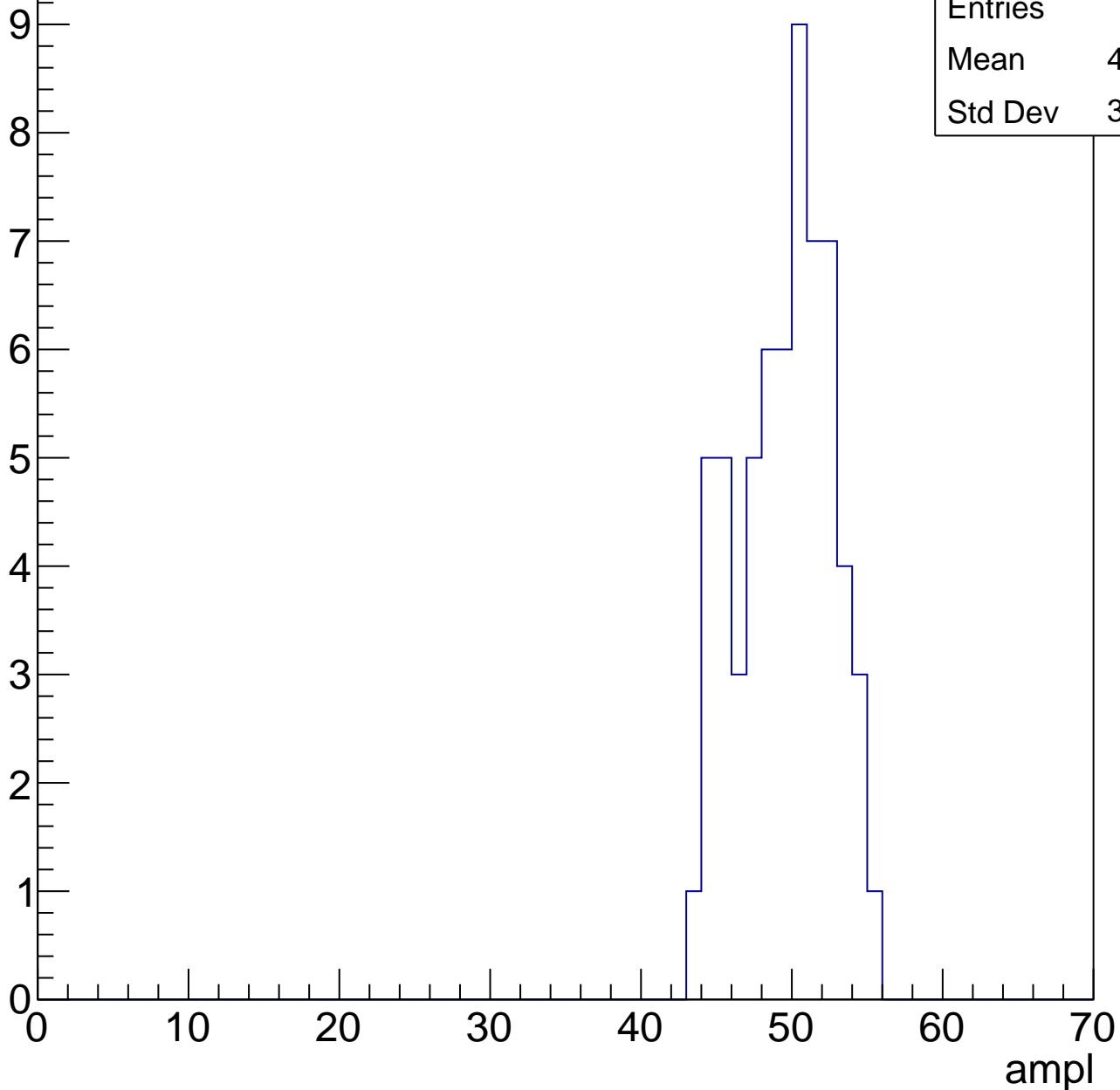


# B1L101S, U19-ch60, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	49.08
Std Dev	3.028

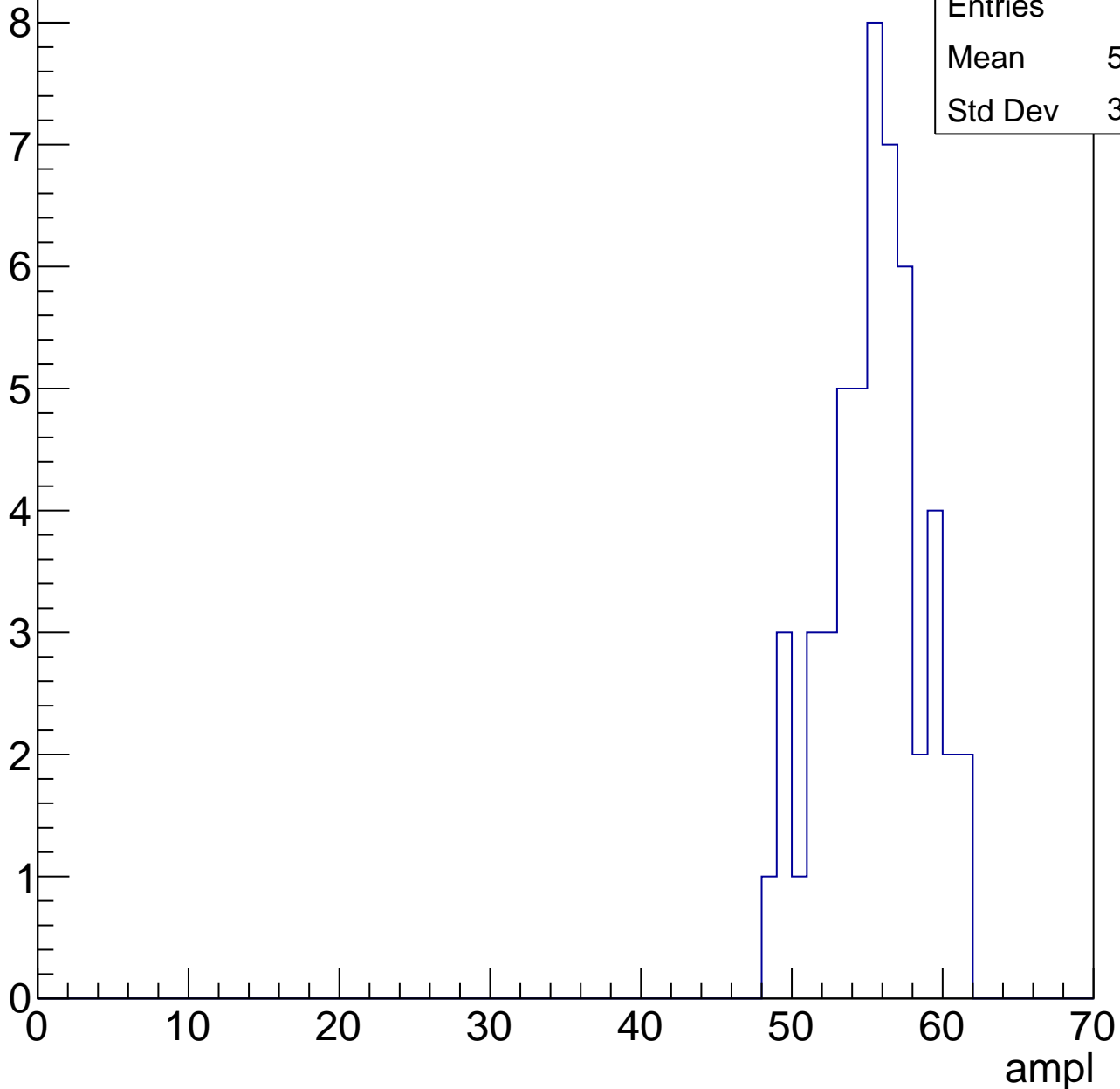


# B1L101S, U19-ch60, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	52
Mean	54.94
Std Dev	3.153

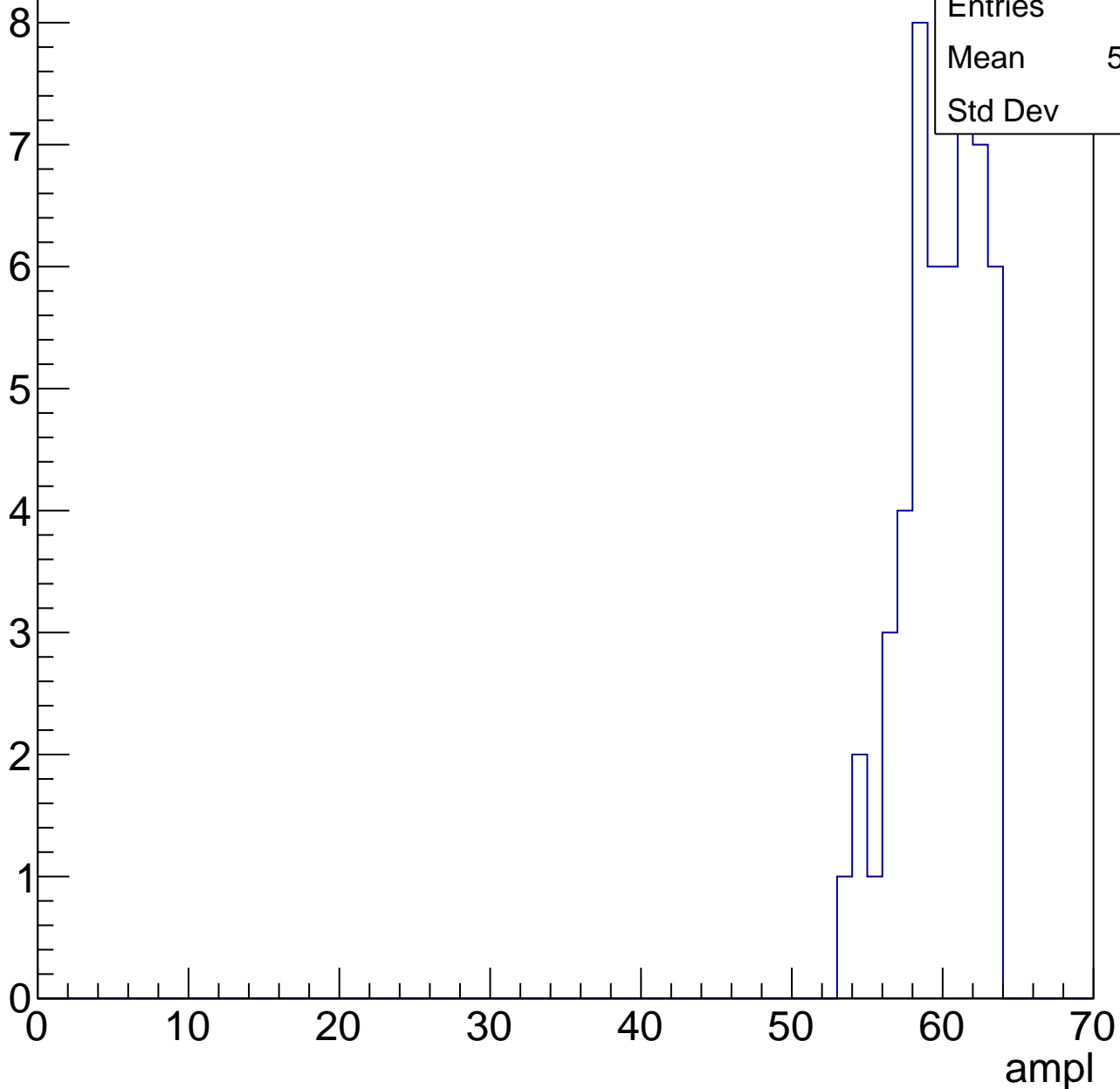


# B1L101S, U19-ch60, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

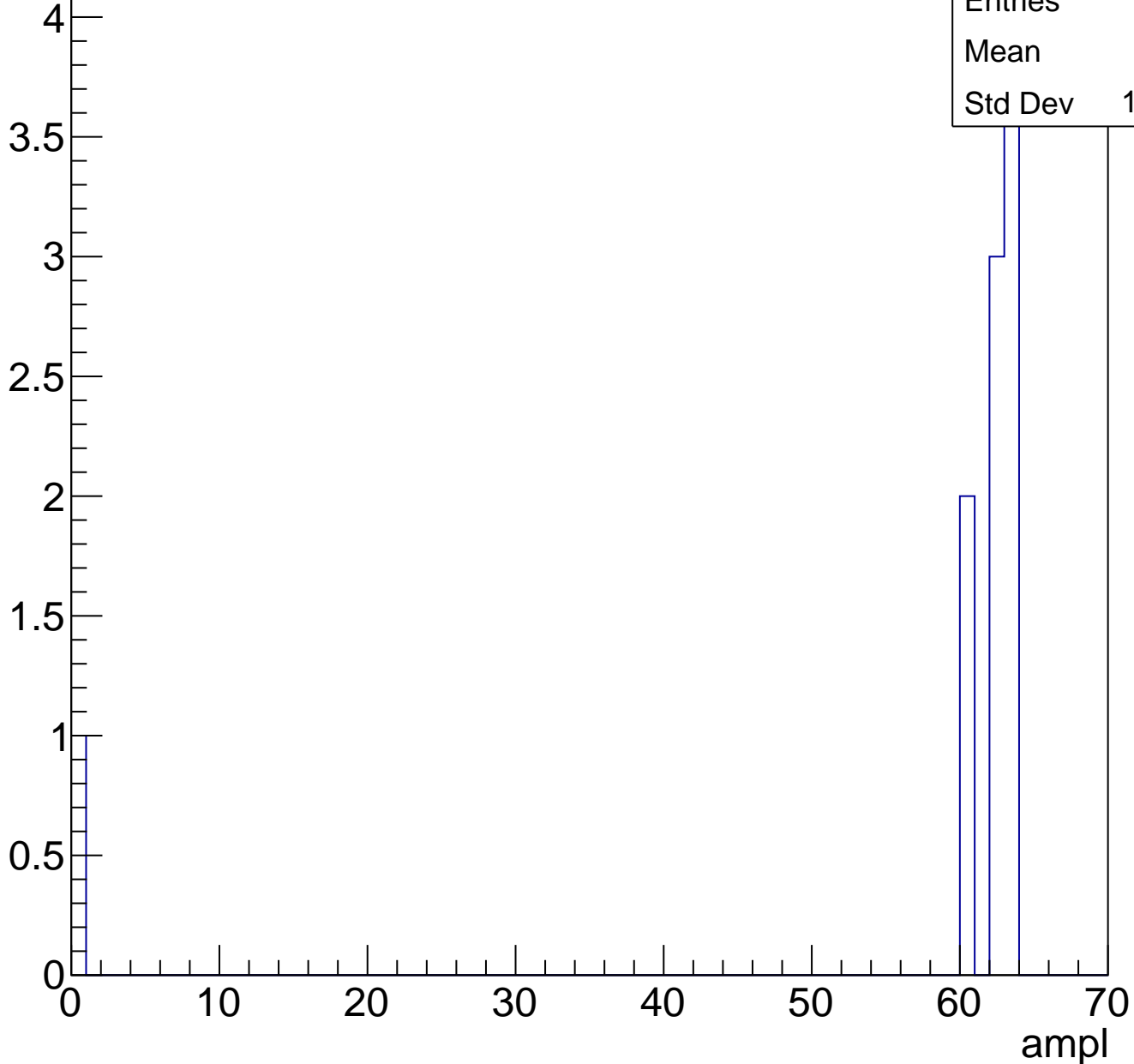
Entries	52
Mean	59.42
Std Dev	2.56



# B1L101S, U19-ch60, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U19-ch60, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U19-ch61, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

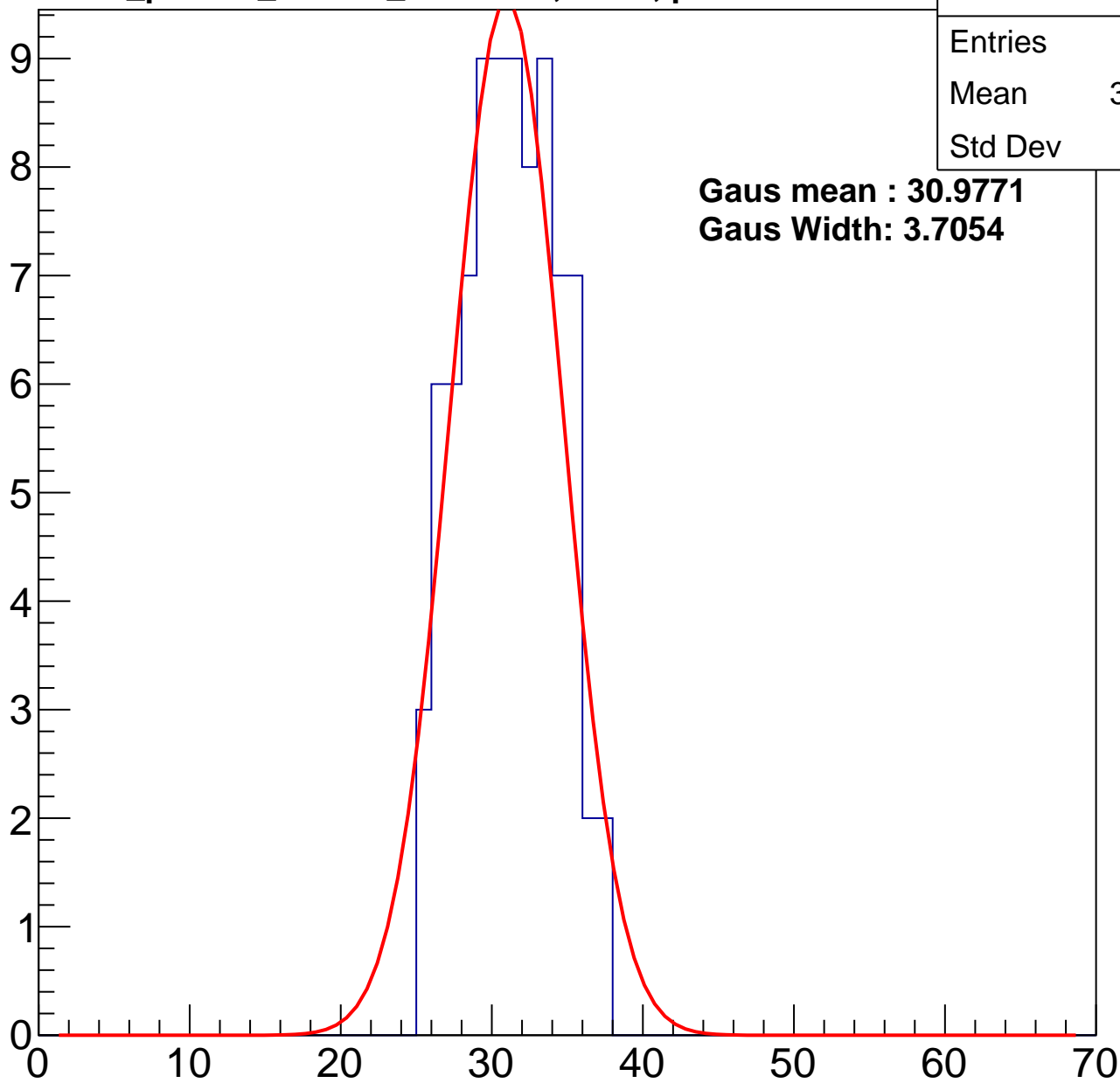
9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	84
Mean	30.73
Std Dev	3.08

**Gaus mean : 30.9771**

**Gaus Width: 3.7054**

ampl



# B1L101S, U19-ch61, adc1

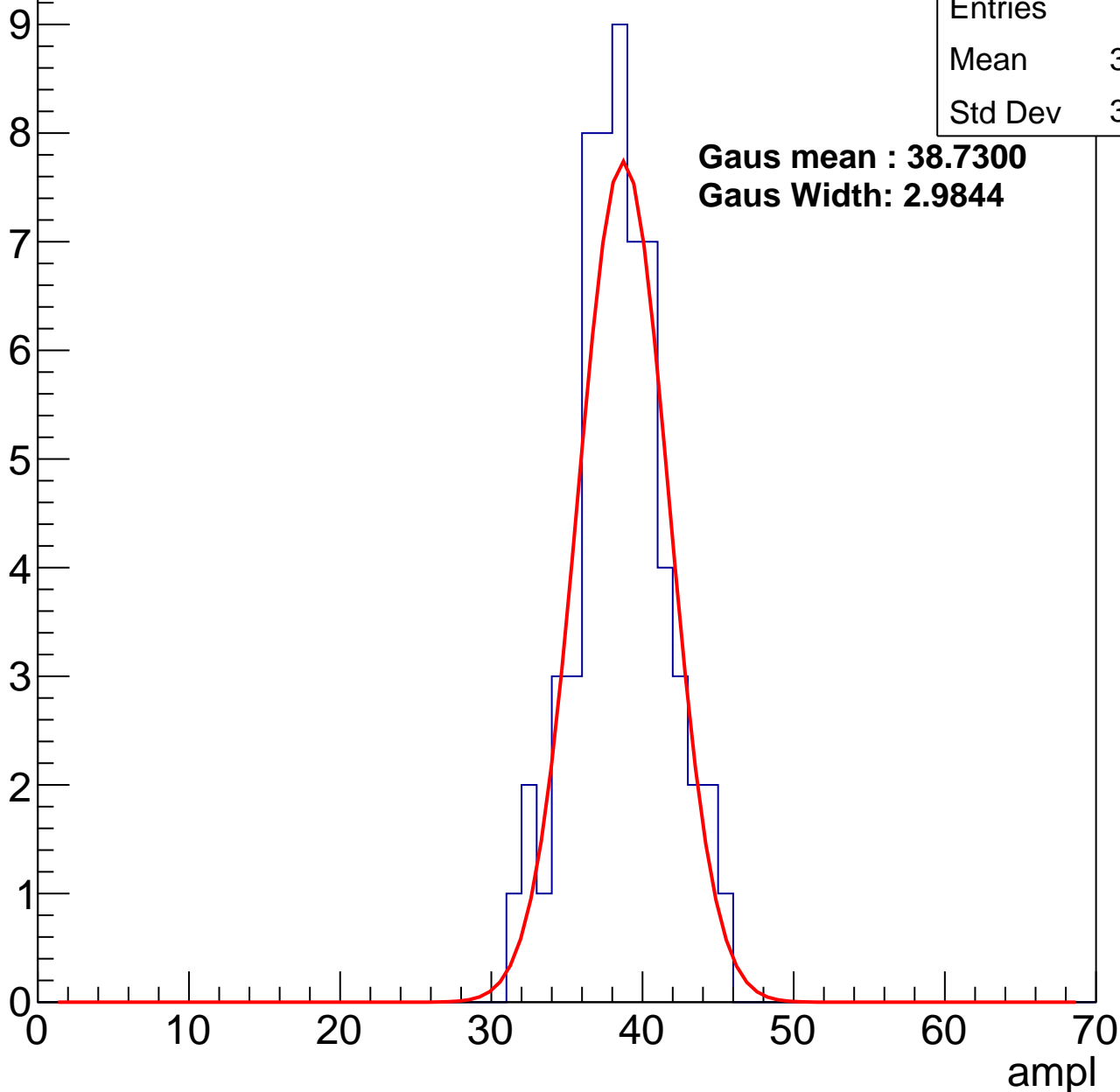
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	38.08
Std Dev	3.004

**Gaus mean : 38.7300**

**Gaus Width: 2.9844**



# B1L101S, U19-ch61, adc2

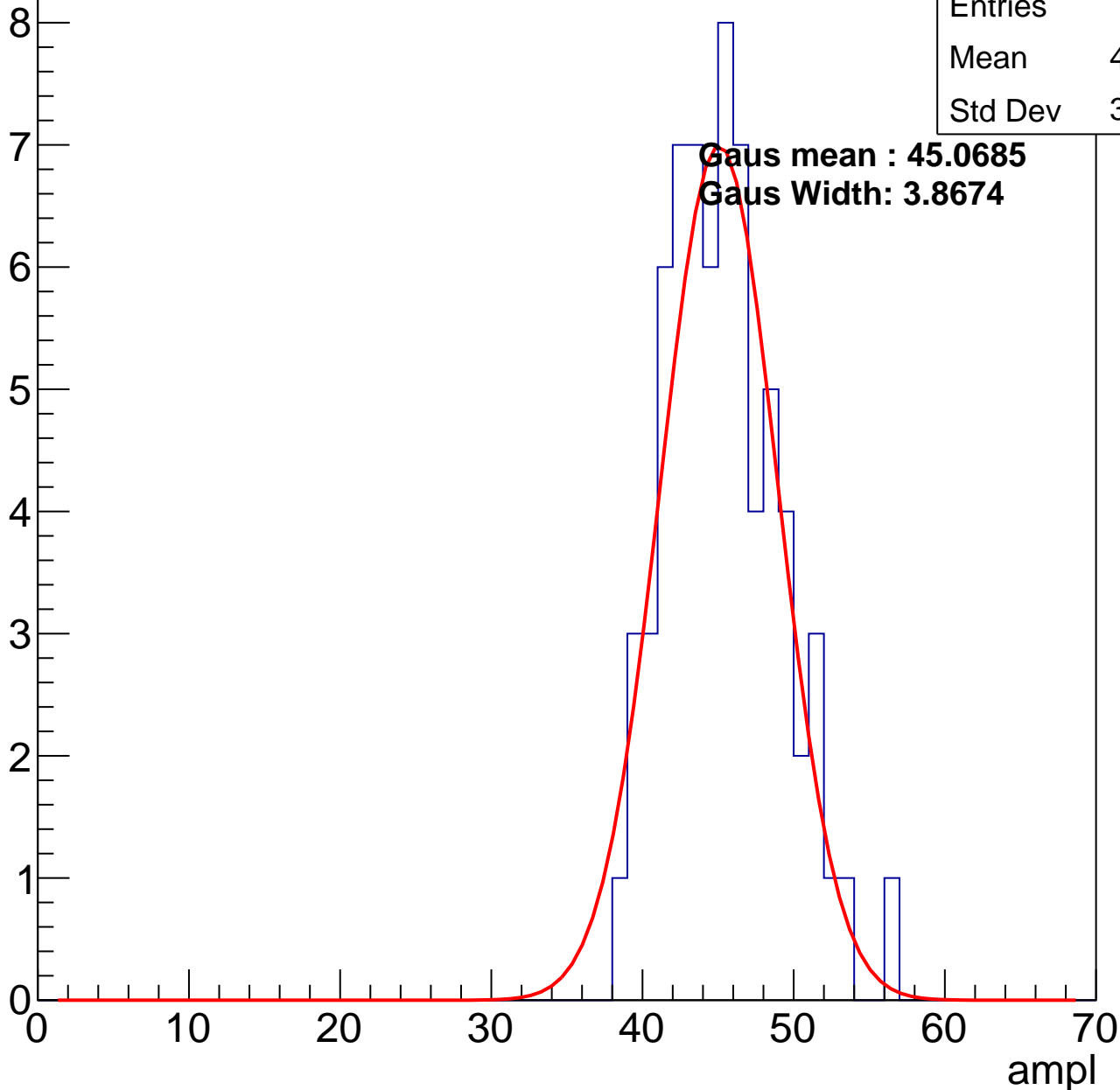
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	44.93
Std Dev	3.708

**Gaus mean : 45.0685**

**Gaus Width: 3.8674**

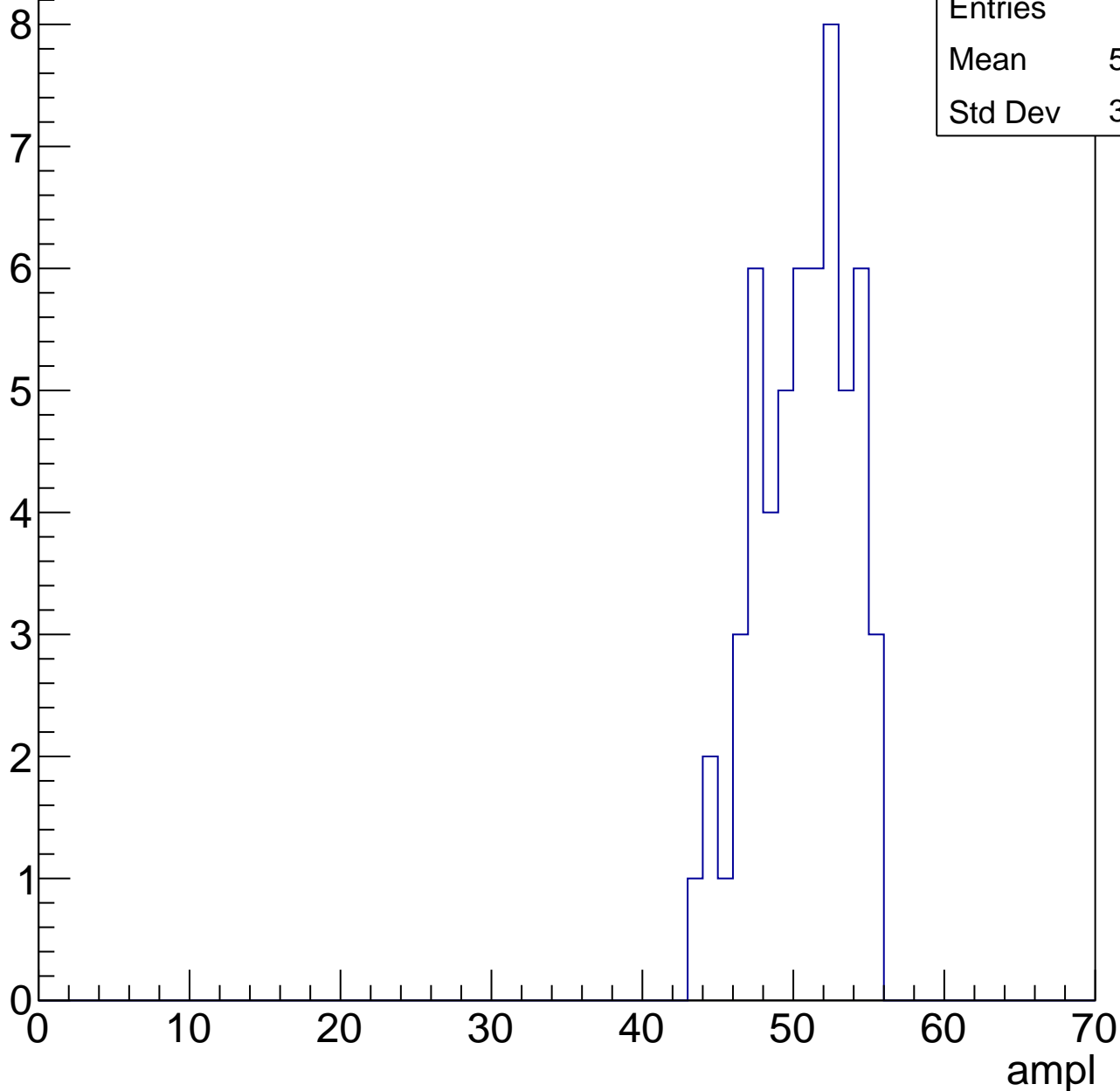


# B1L101S, U19-ch61, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	56
Mean	50.16
Std Dev	3.052

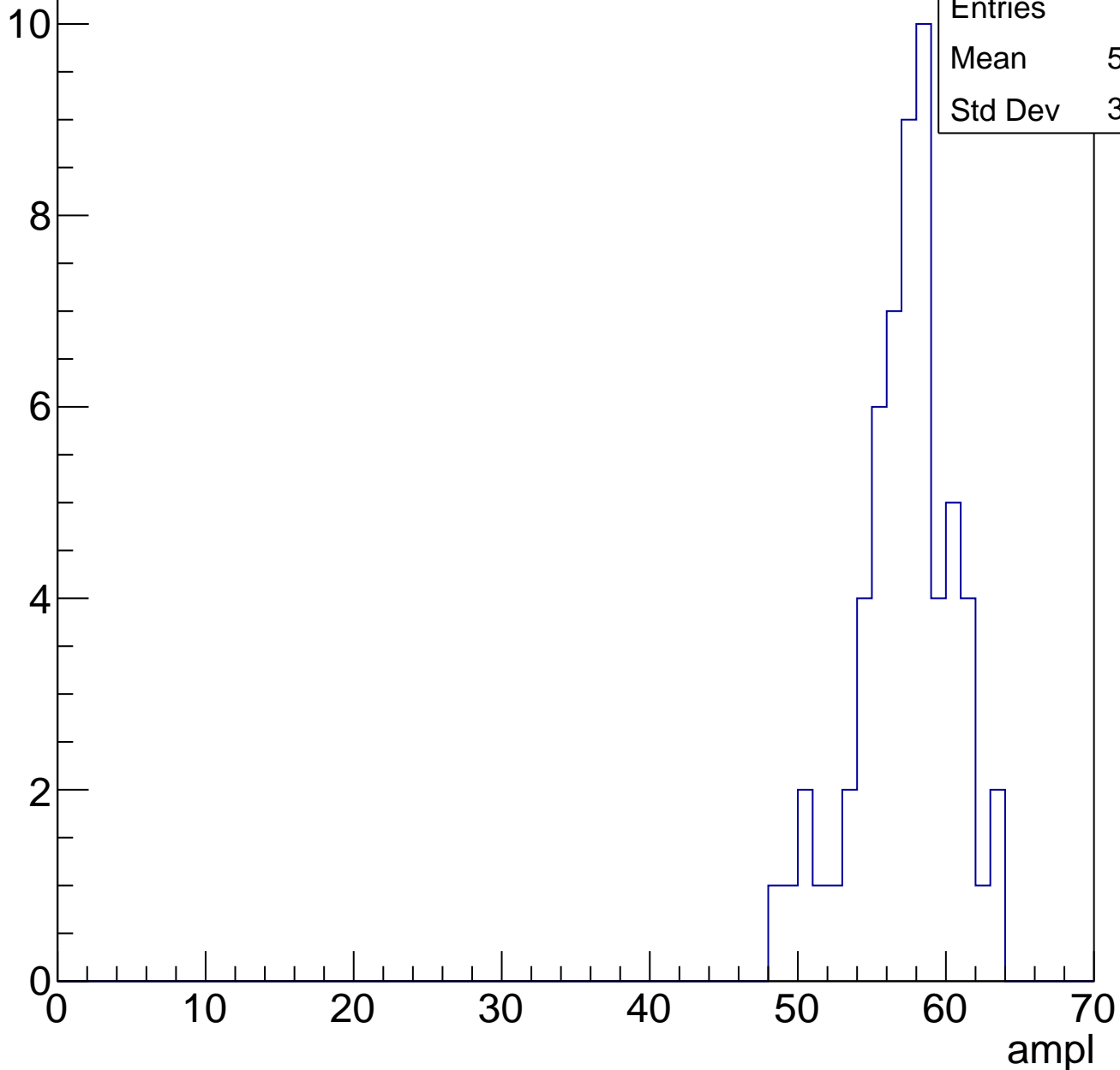


# B1L101S, U19-ch61, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	60
Mean	56.75
Std Dev	3.244

Entry

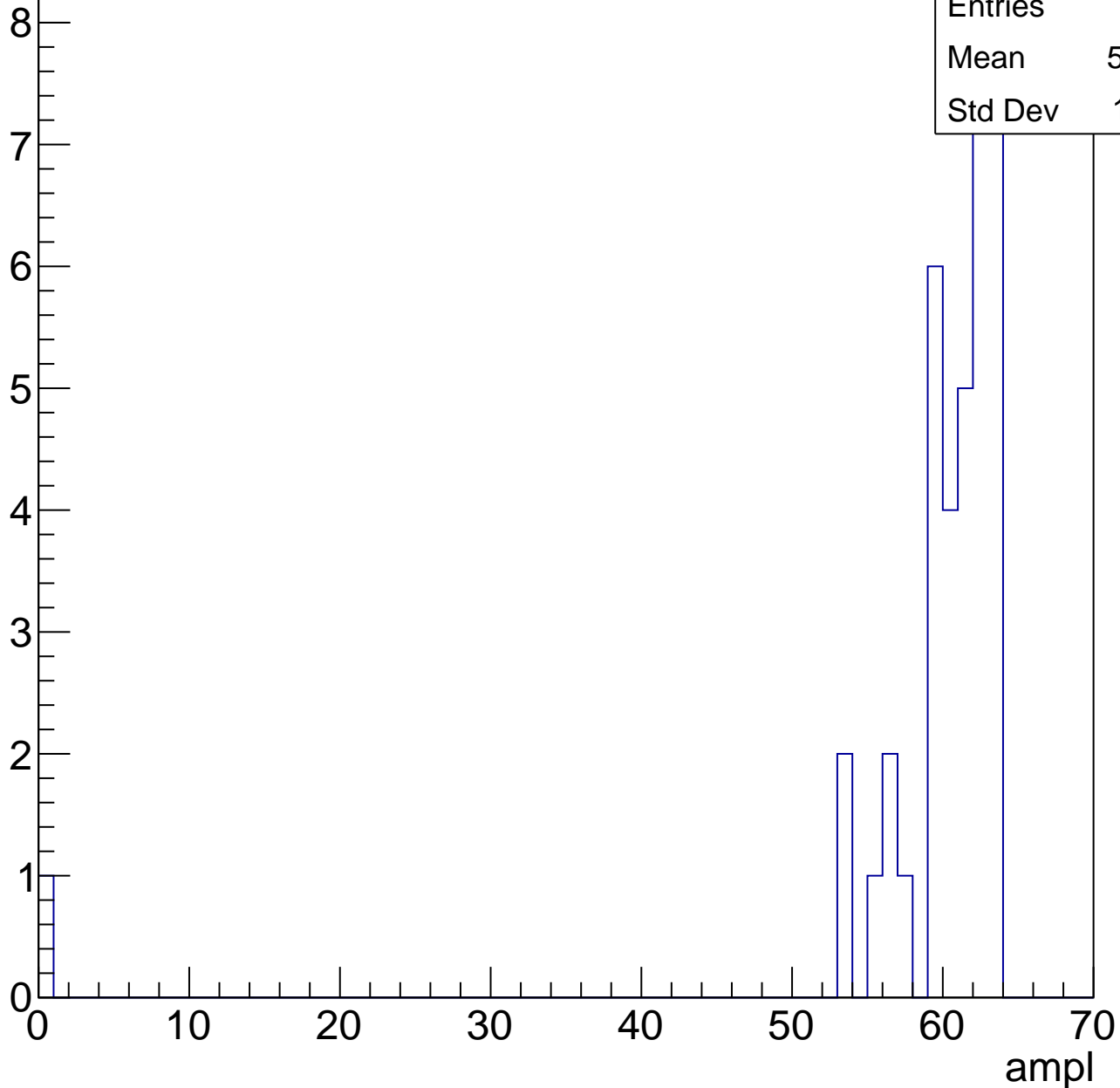


# B1L101S, U19-ch61, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	38
Mean	58.66
Std Dev	10.01



# B1L101S, U19-ch61, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U19-ch61, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	23
Std Dev	0

# B1L101S, U19-ch62, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	69
Mean	28.88
Std Dev	5.904

**Gaus mean : 30.2342**

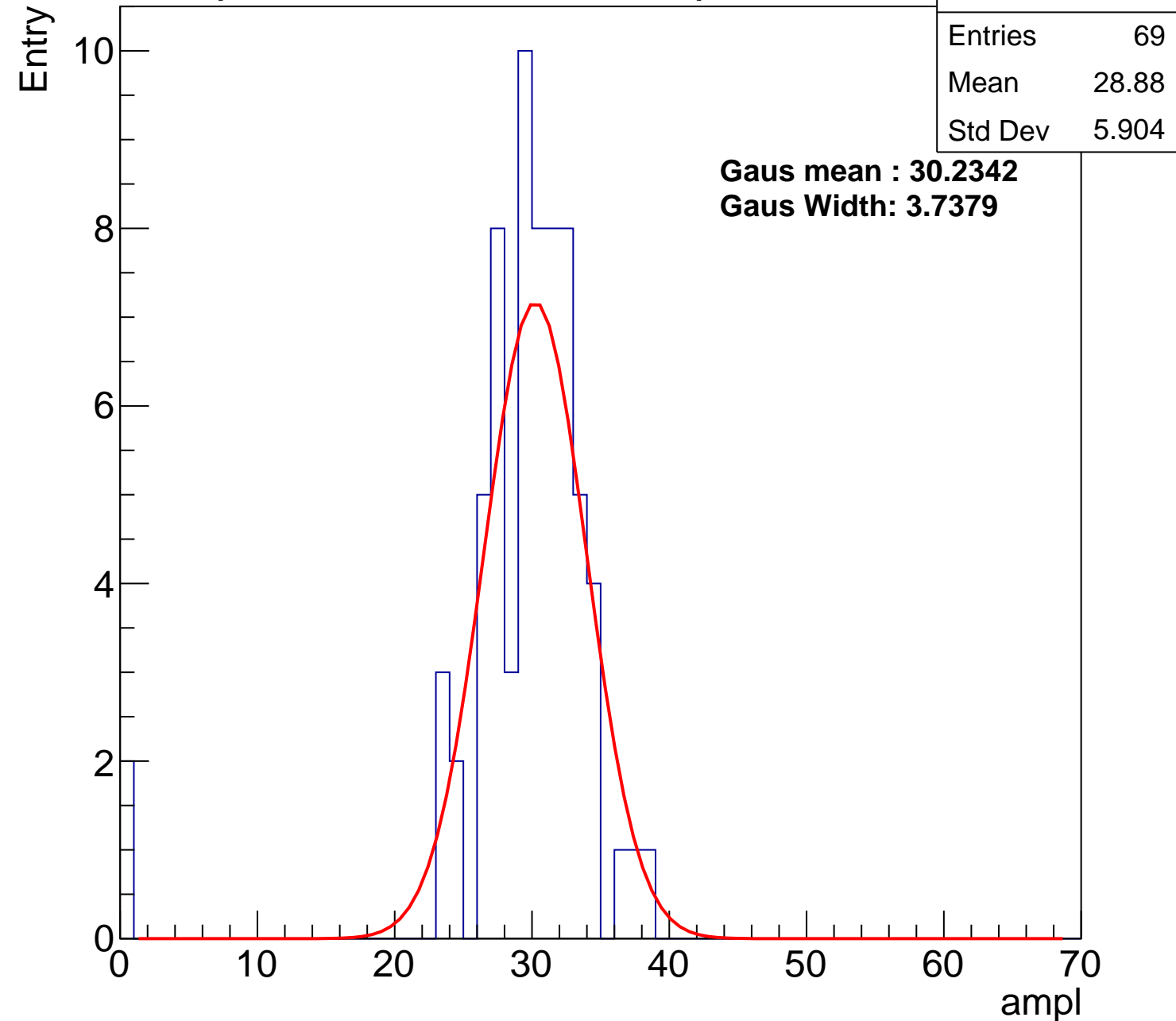
**Gaus Width: 3.7379**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U19-ch62, adc1

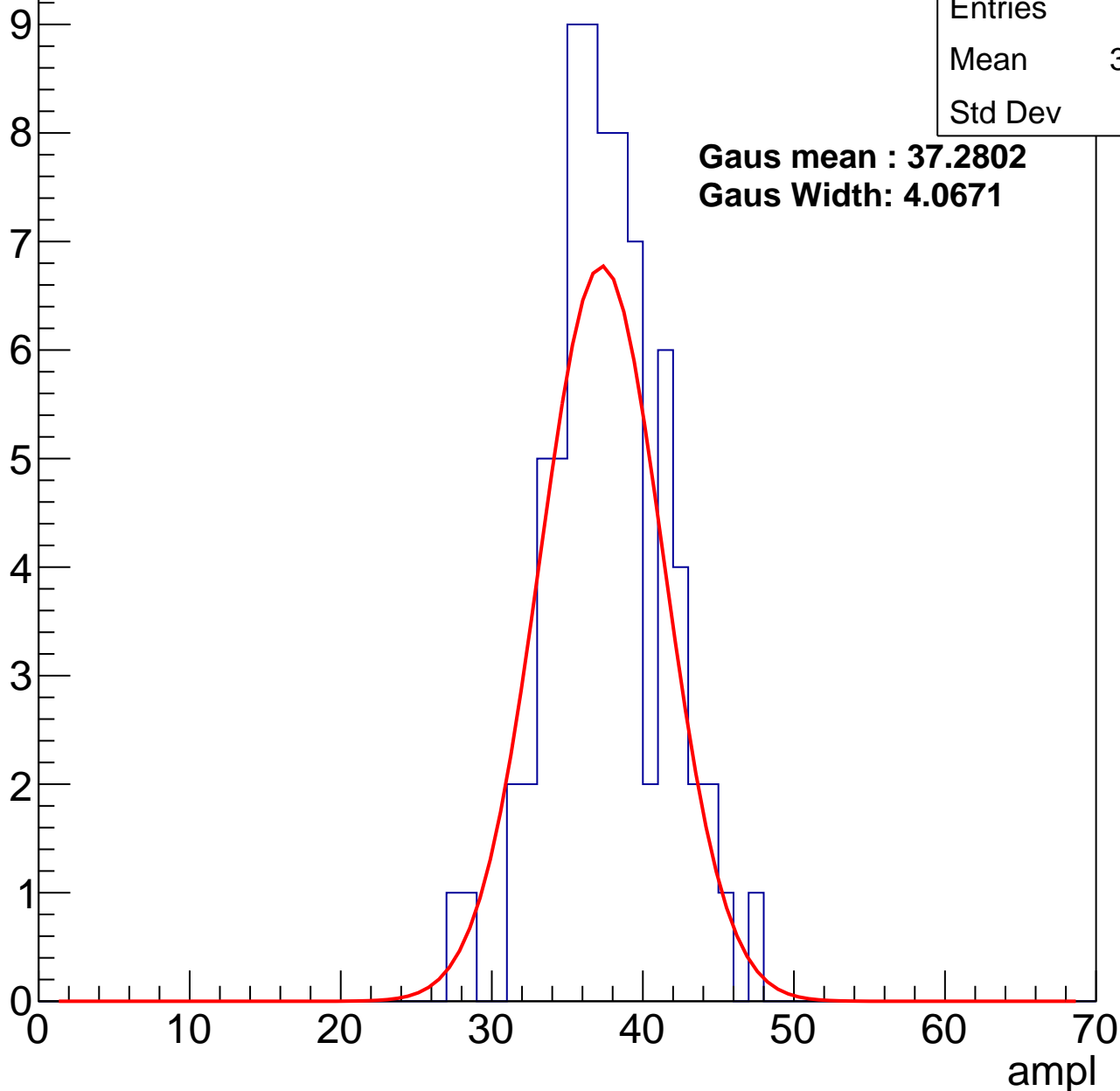
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	75
Mean	37.17
Std Dev	3.75

**Gaus mean : 37.2802**

**Gaus Width: 4.0671**



# B1L101S, U19-ch62, adc2

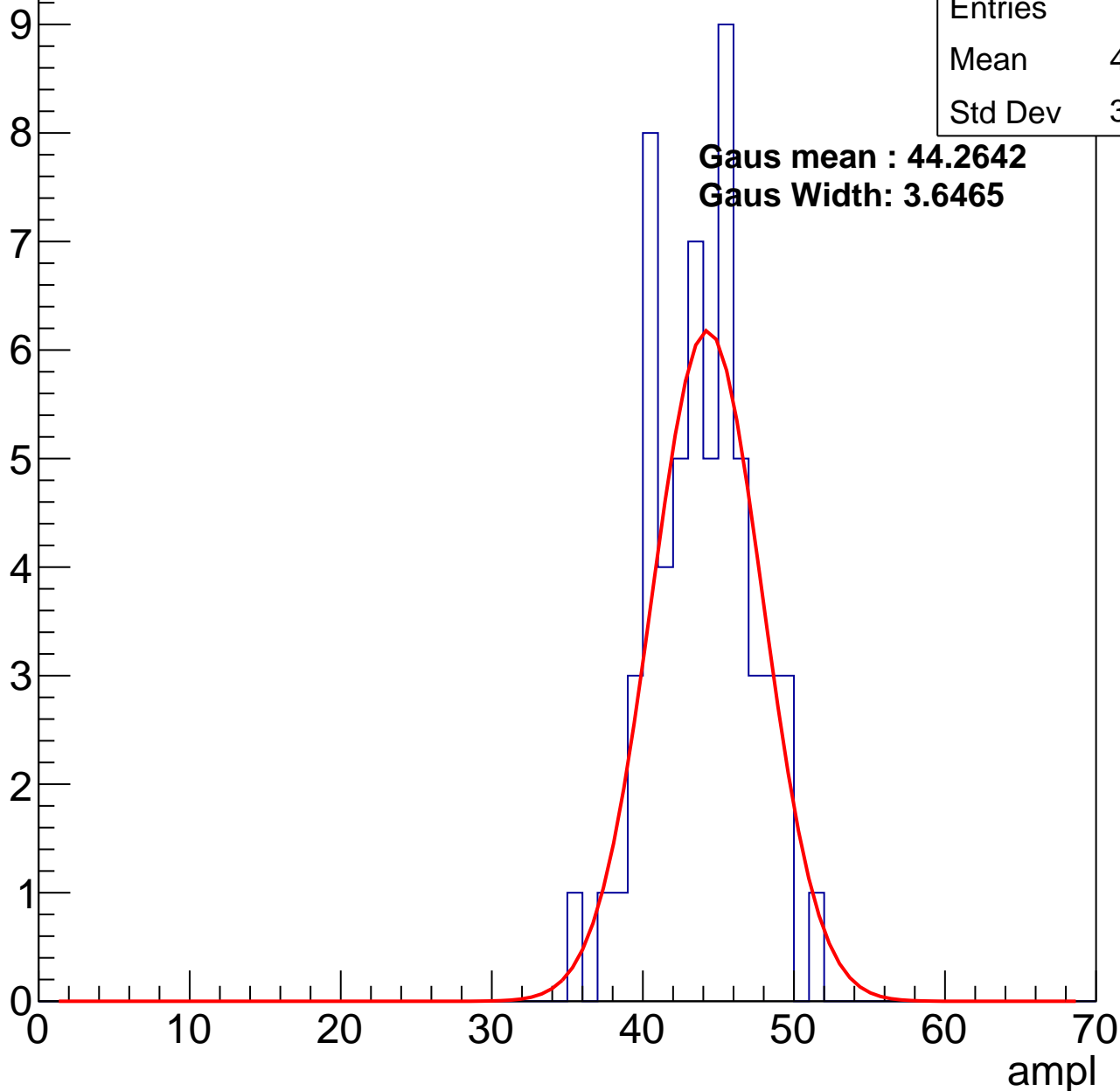
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	59
Mean	43.39
Std Dev	3.288

**Gaus mean : 44.2642**

**Gaus Width: 3.6465**



# B1L101S, U19-ch62, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	59
Mean	49.34
Std Dev	2.92

Entry

10

8

6

4

2

0

0

10

20

30

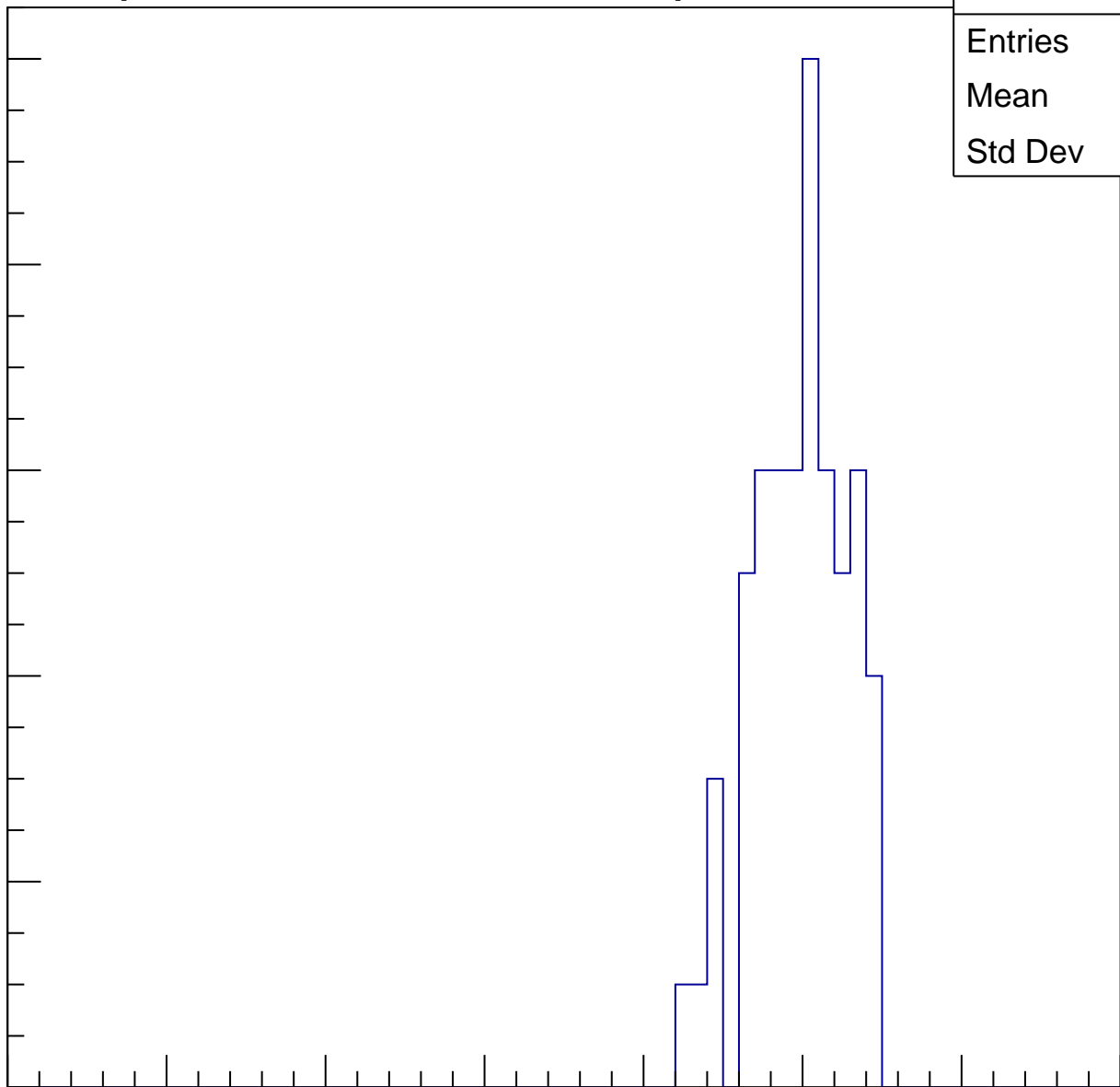
40

50

60

70

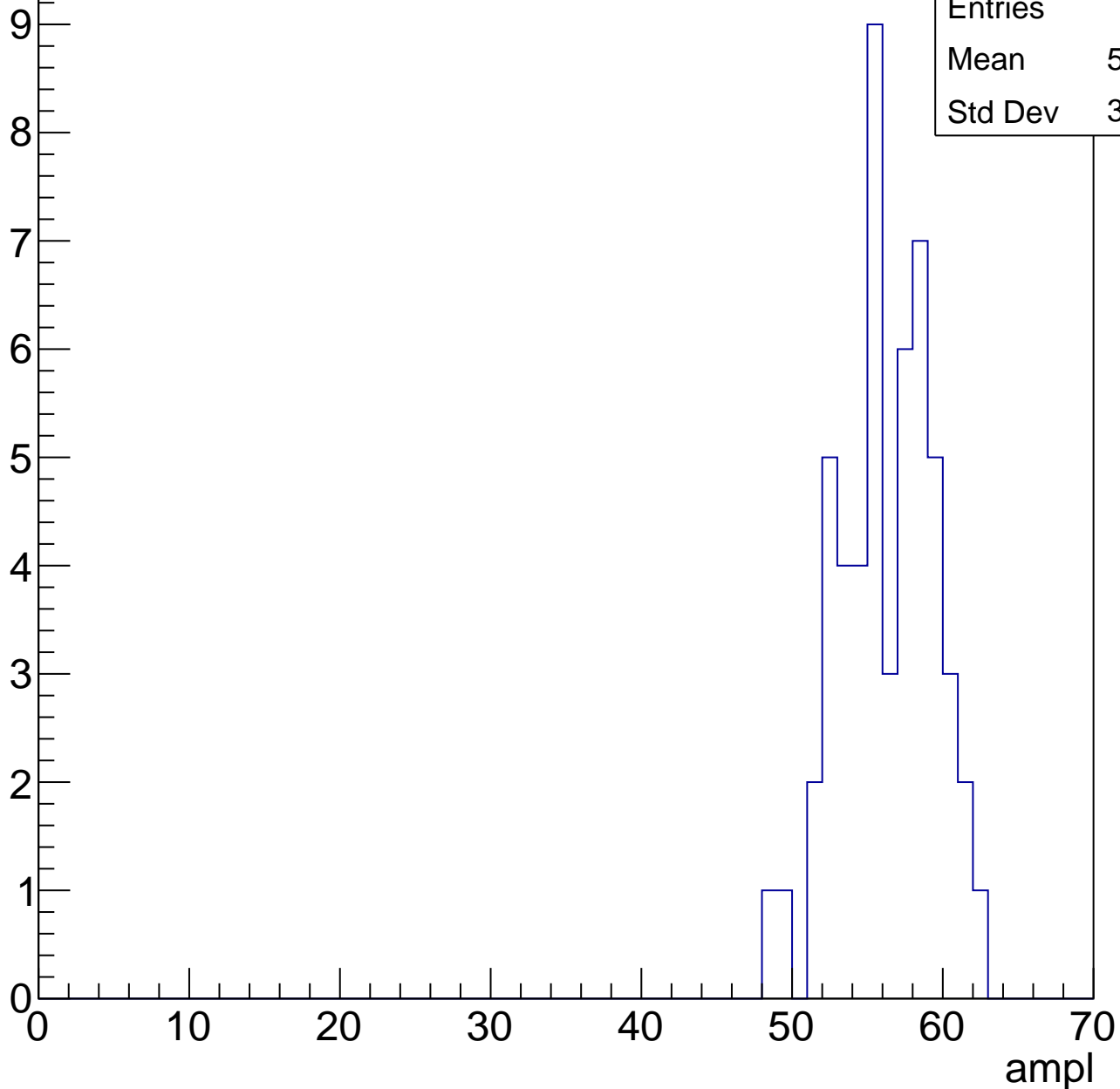
ampl



# B1L101S, U19-ch62, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

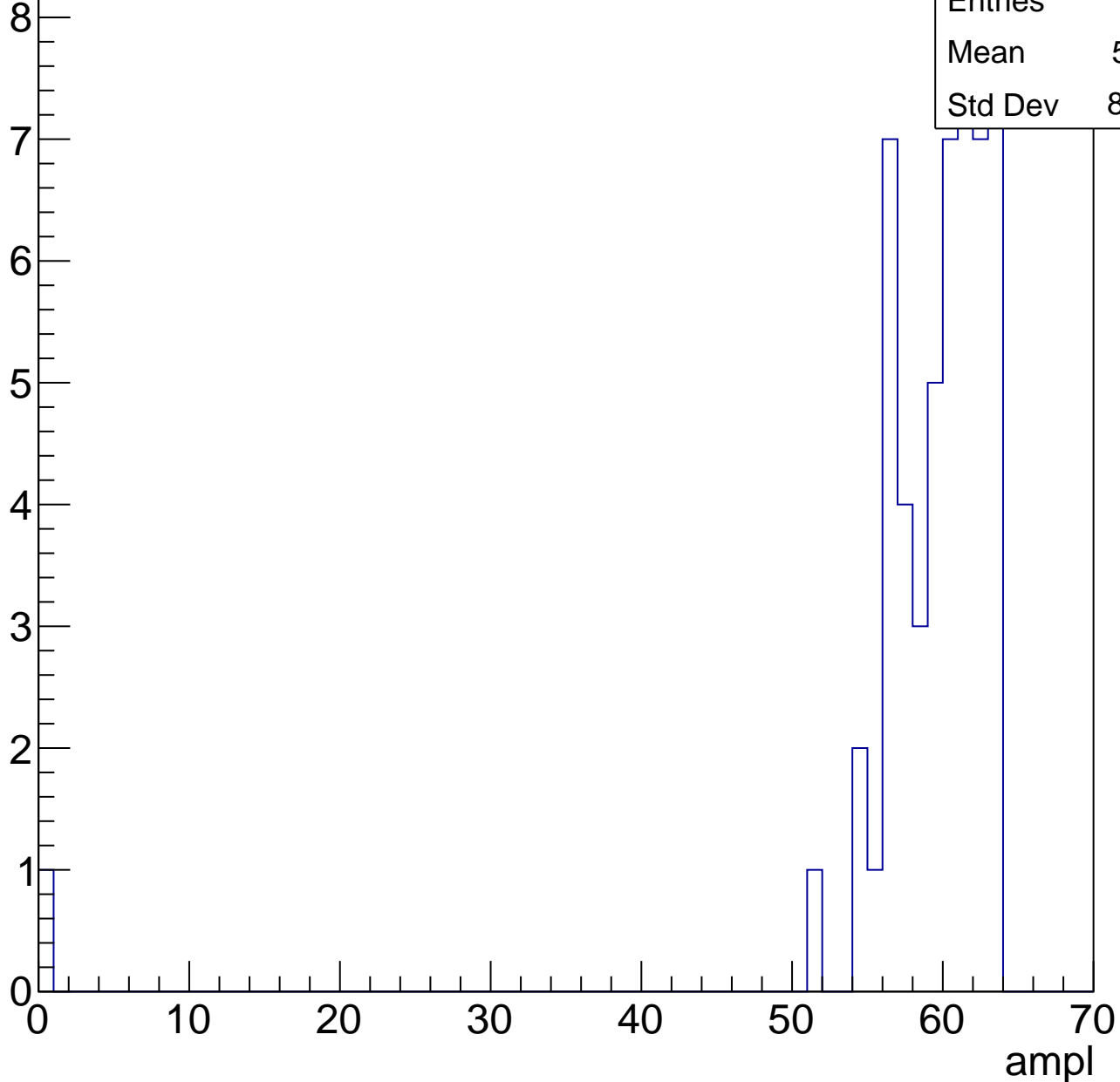


# B1L101S, U19-ch62, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	54
Mean	58.31
Std Dev	8.496



# B1L101S, U19-ch62, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	3
Mean	62.67
Std Dev	0.4714

ampl

0 10 20 30 40 50 60 70



# B1L101S, U19-ch62, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U19-ch63, adc0

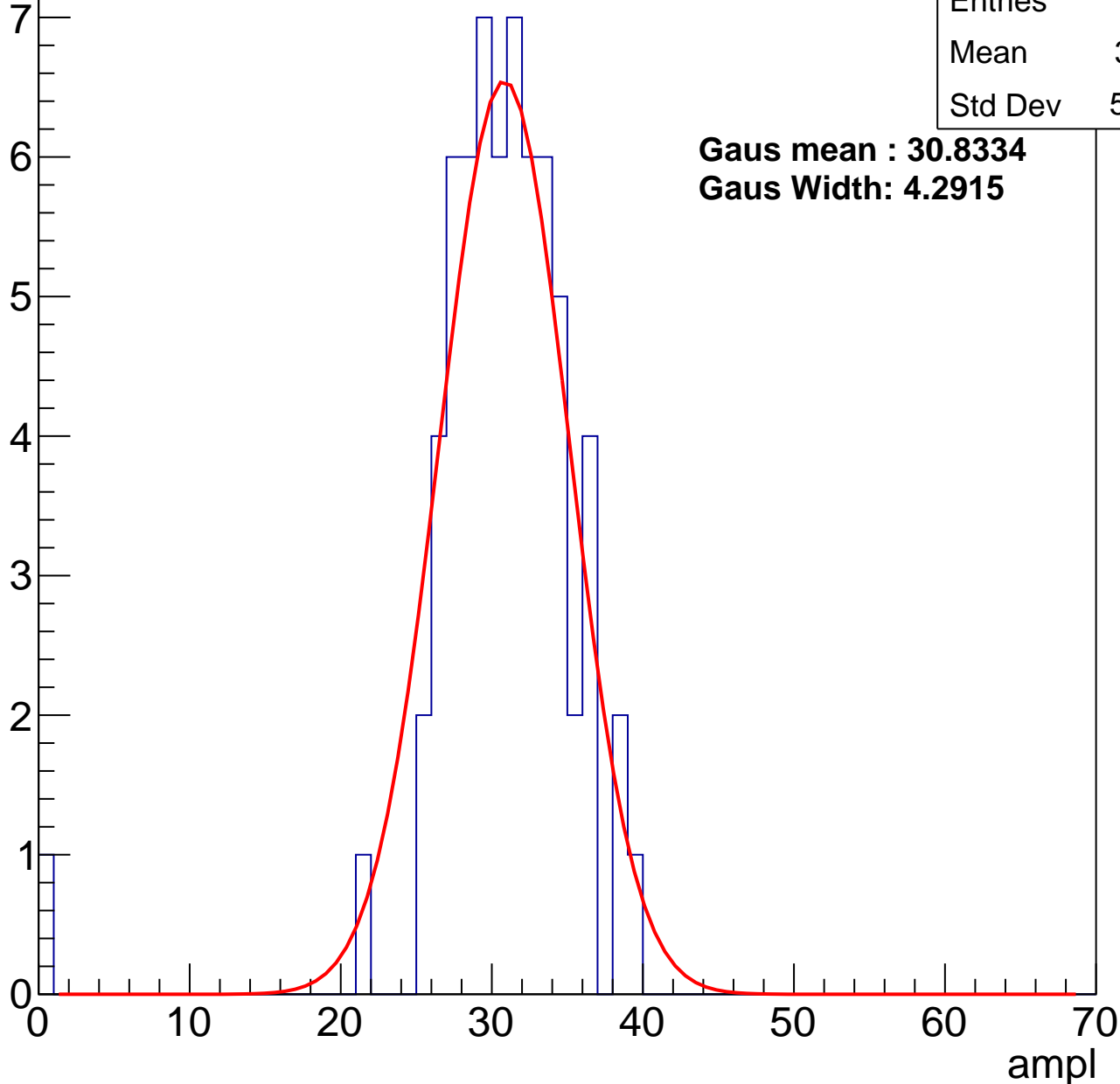
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	66
Mean	30.21
Std Dev	5.142

**Gaus mean : 30.8334**

**Gaus Width: 4.2915**



# B1L101S, U19-ch63, adc1

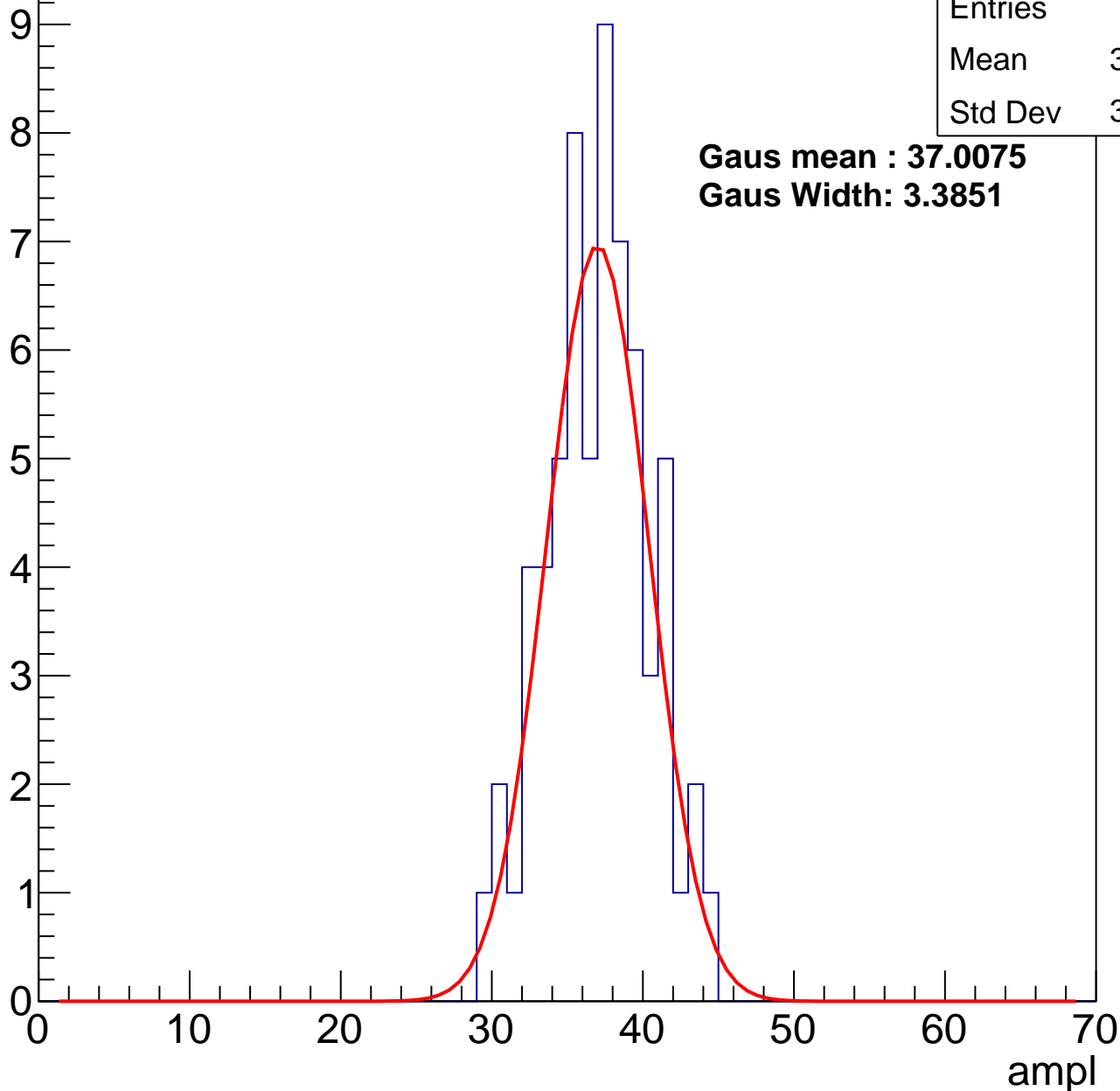
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	36.56
Std Dev	3.344

**Gaus mean : 37.0075**

**Gaus Width: 3.3851**



# B1L101S, U19-ch63, adc2

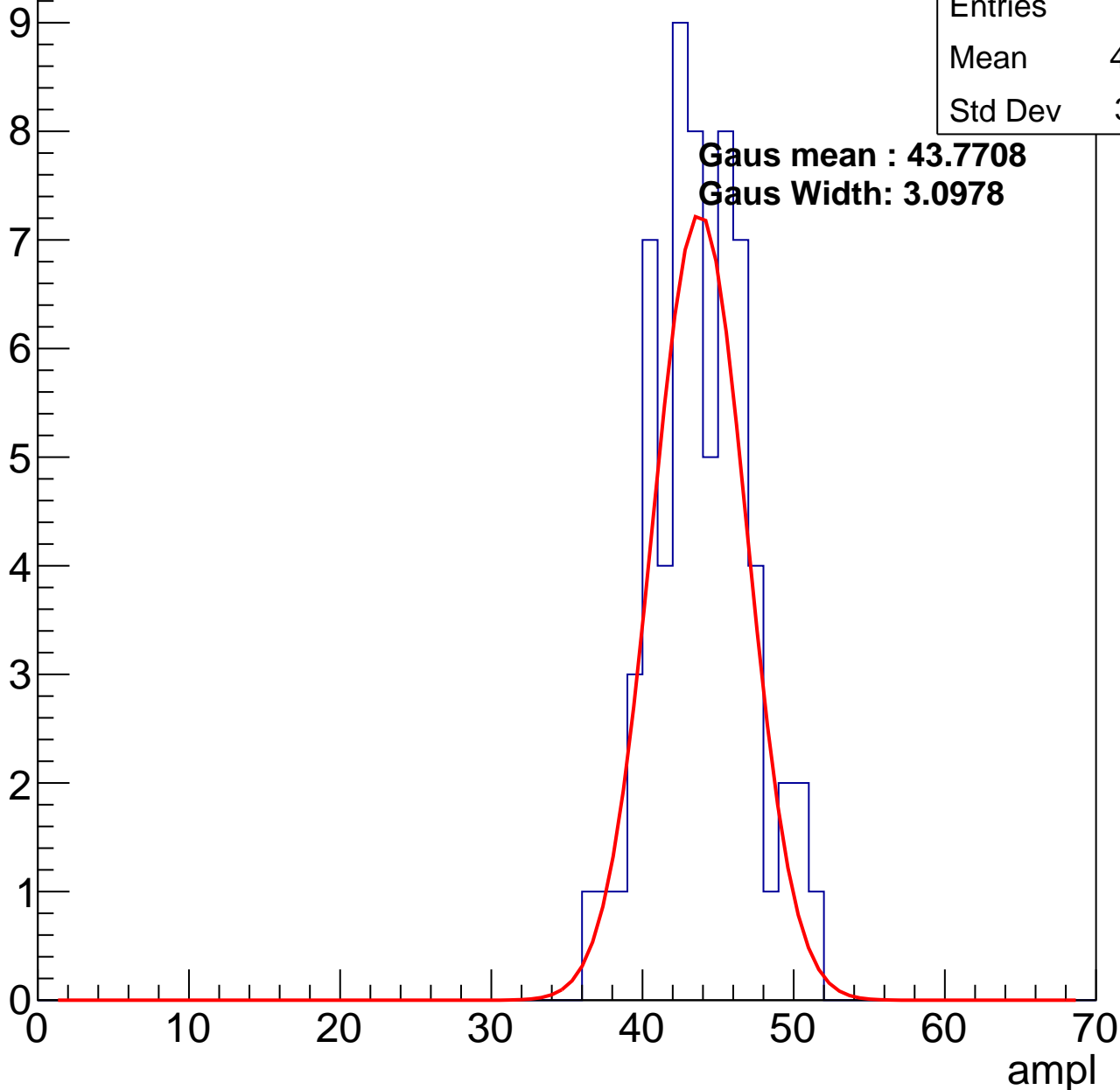
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	43.45
Std Dev	3.201

**Gaus mean : 43.7708**

**Gaus Width: 3.0978**

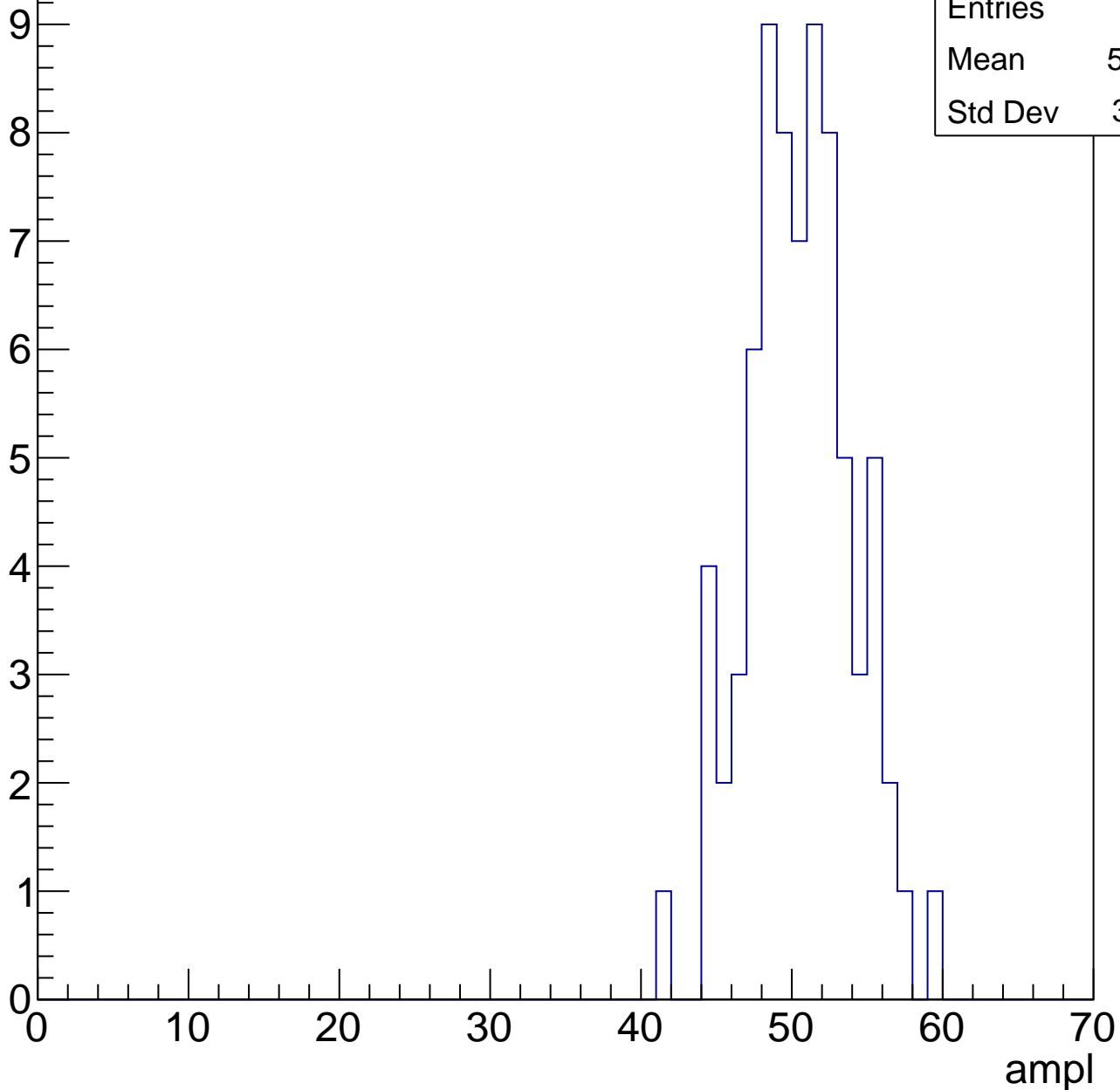


# B1L101S, U19-ch63, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	74
Mean	50.08
Std Dev	3.451

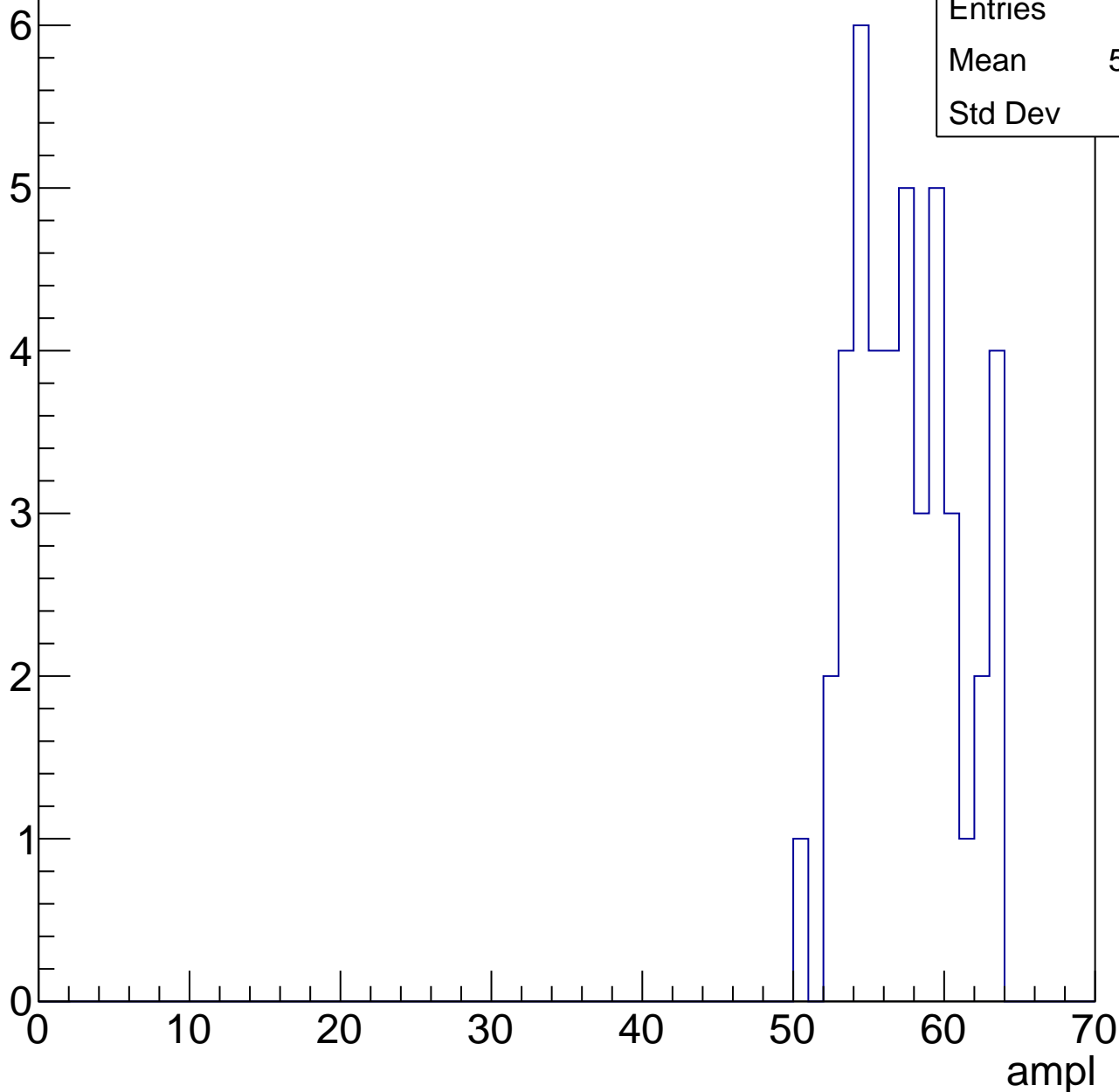


# B1L101S, U19-ch63, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

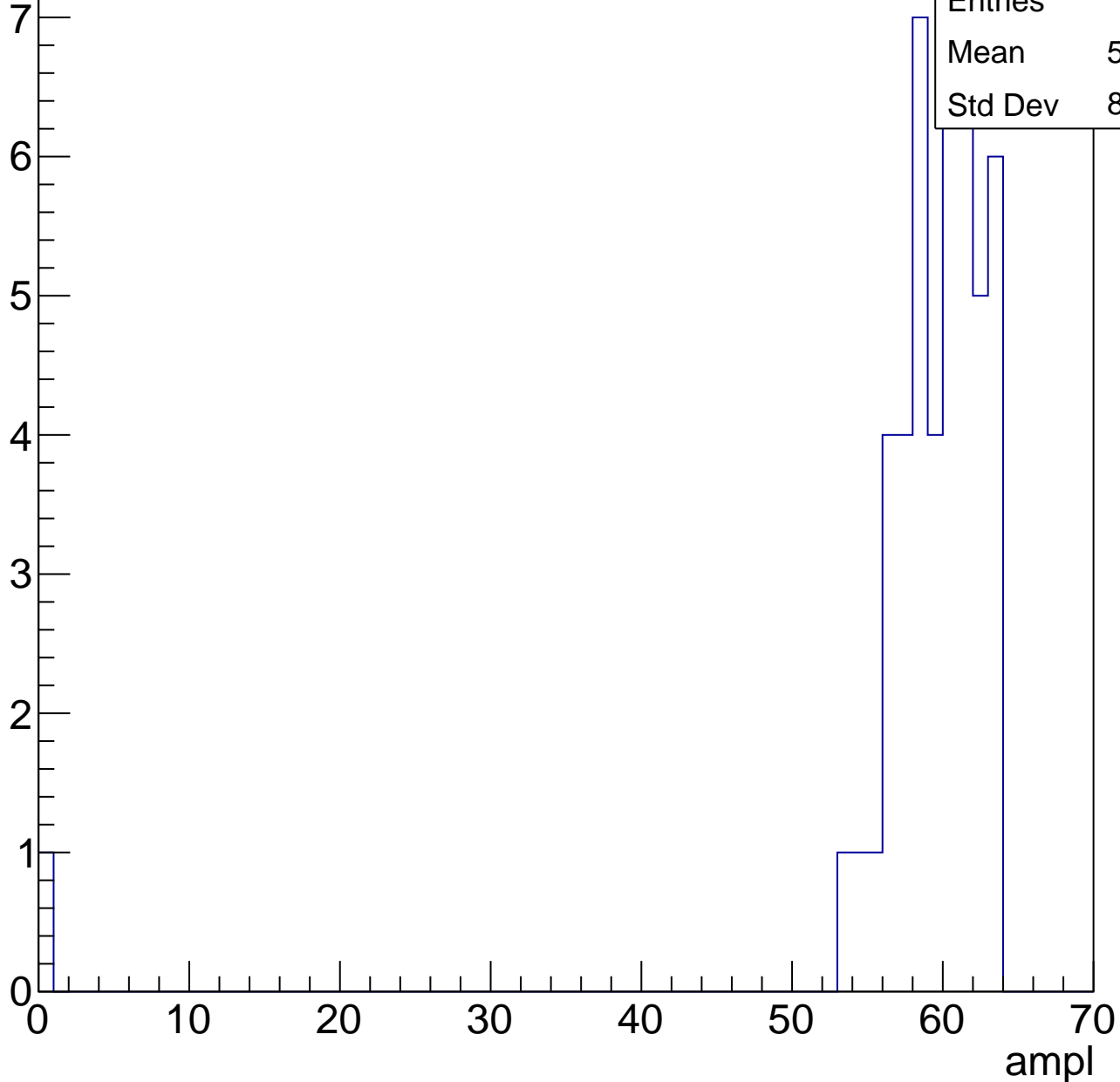
Entries	44
Mean	56.93
Std Dev	3.36



# B1L101S, U19-ch63, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

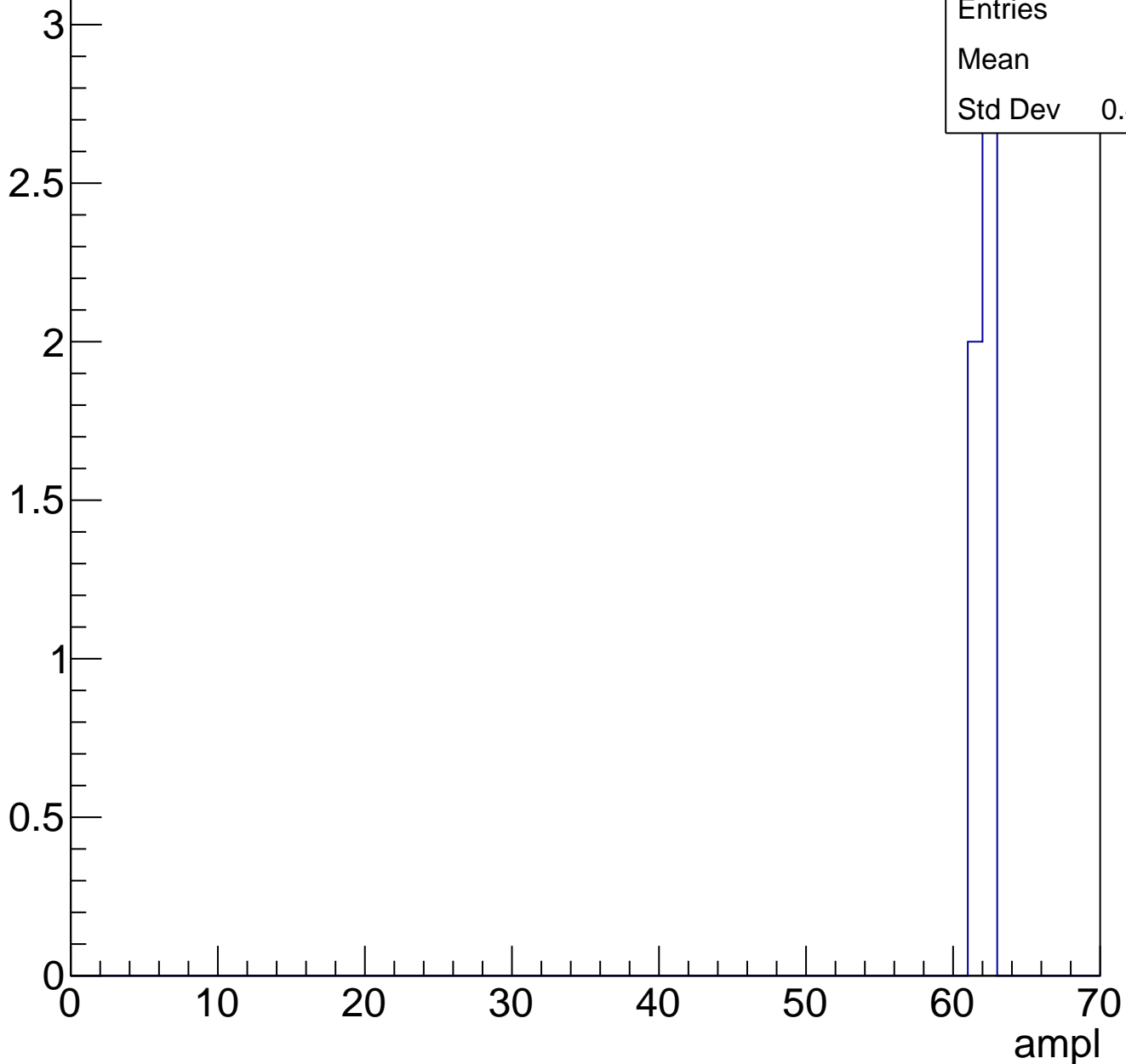
Entry



# B1L101S, U19-ch63, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U19-ch63, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L101S, U19-ch64, adc0

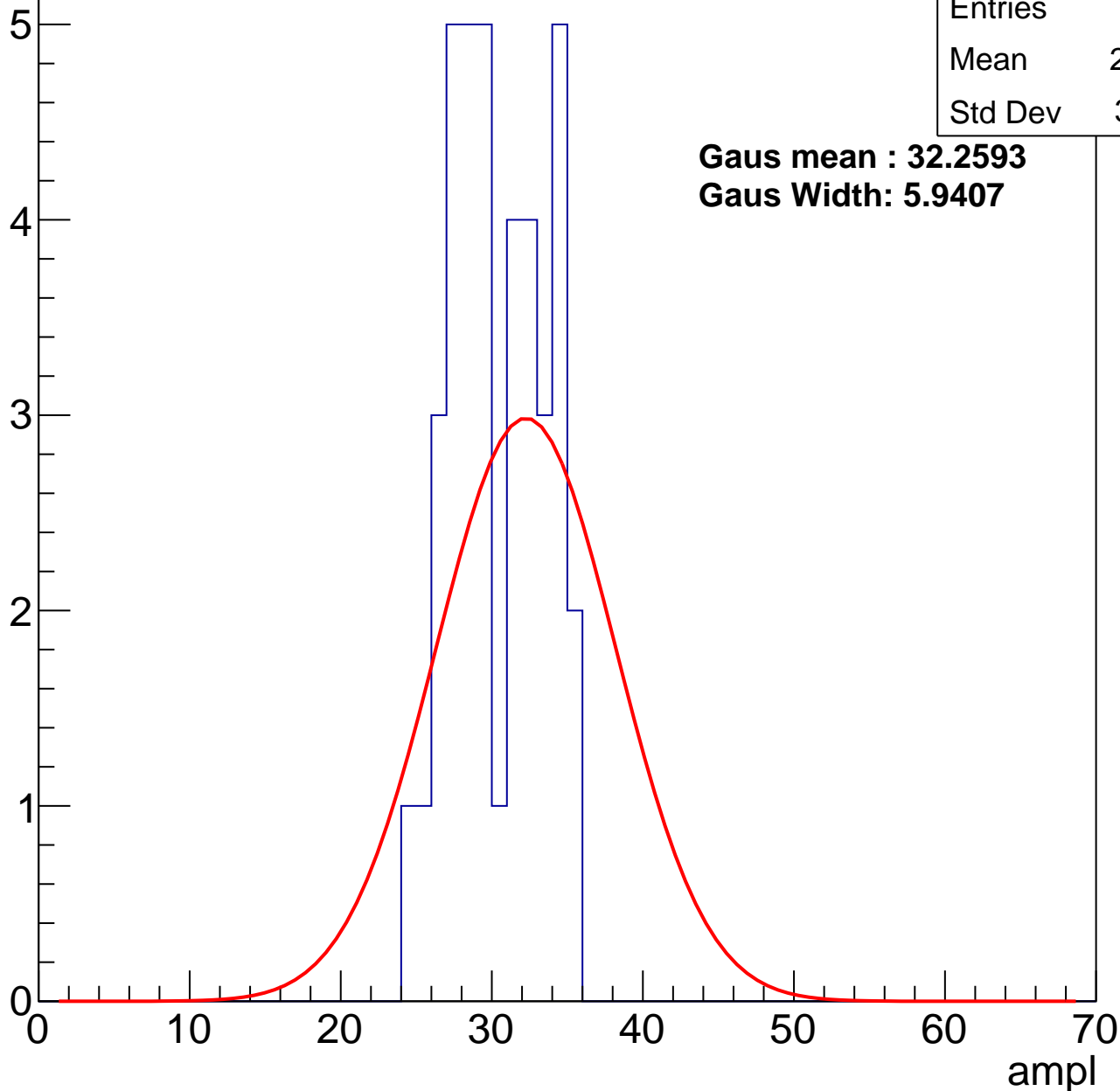
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	39
Mean	29.95
Std Dev	3.021

**Gaus mean : 32.2593**

**Gaus Width: 5.9407**



# B1L101S, U19-ch64, adc1

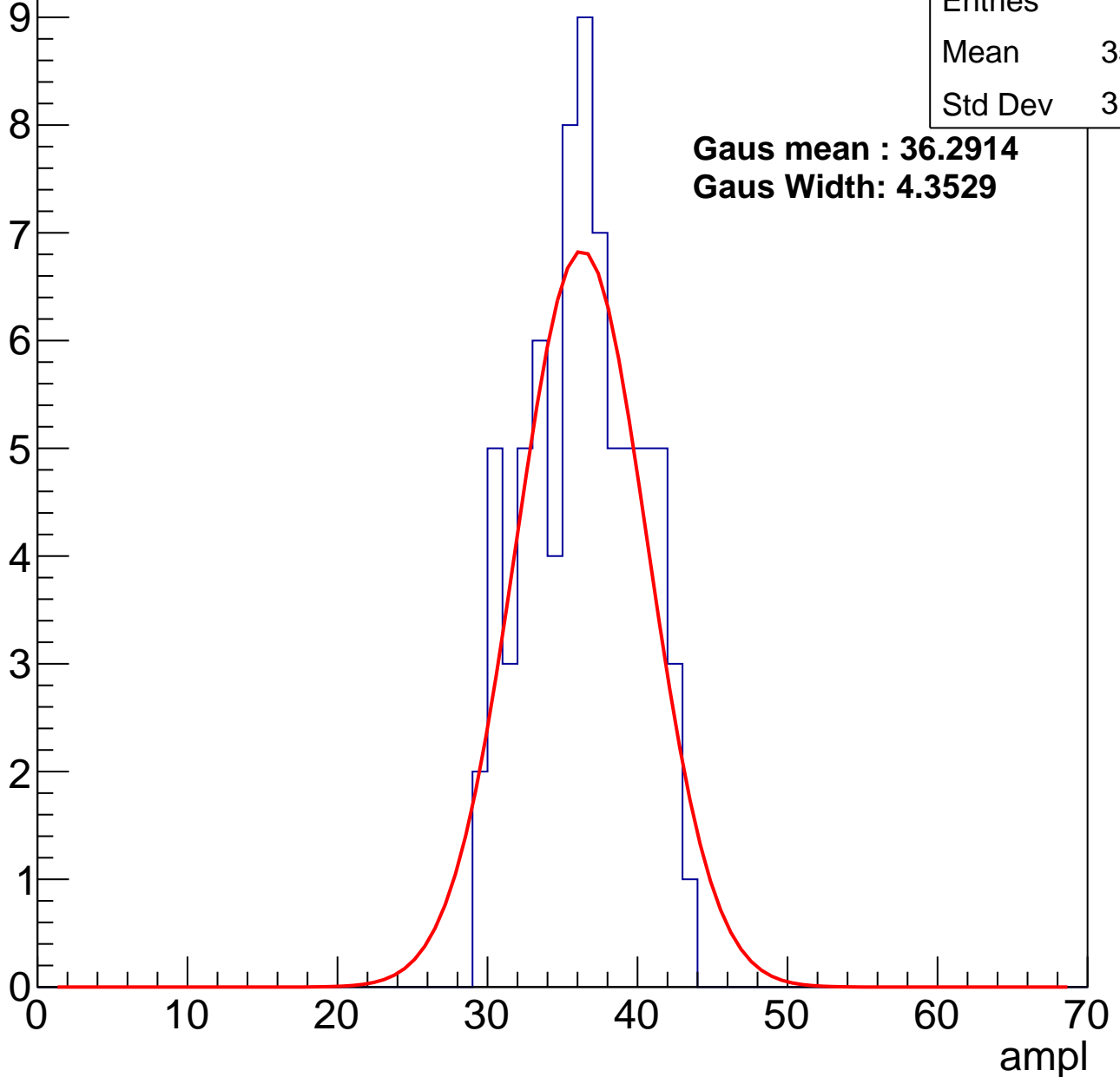
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	73
Mean	35.85
Std Dev	3.595

**Gaus mean : 36.2914**

**Gaus Width: 4.3529**



# B1L101S, U19-ch64, adc2

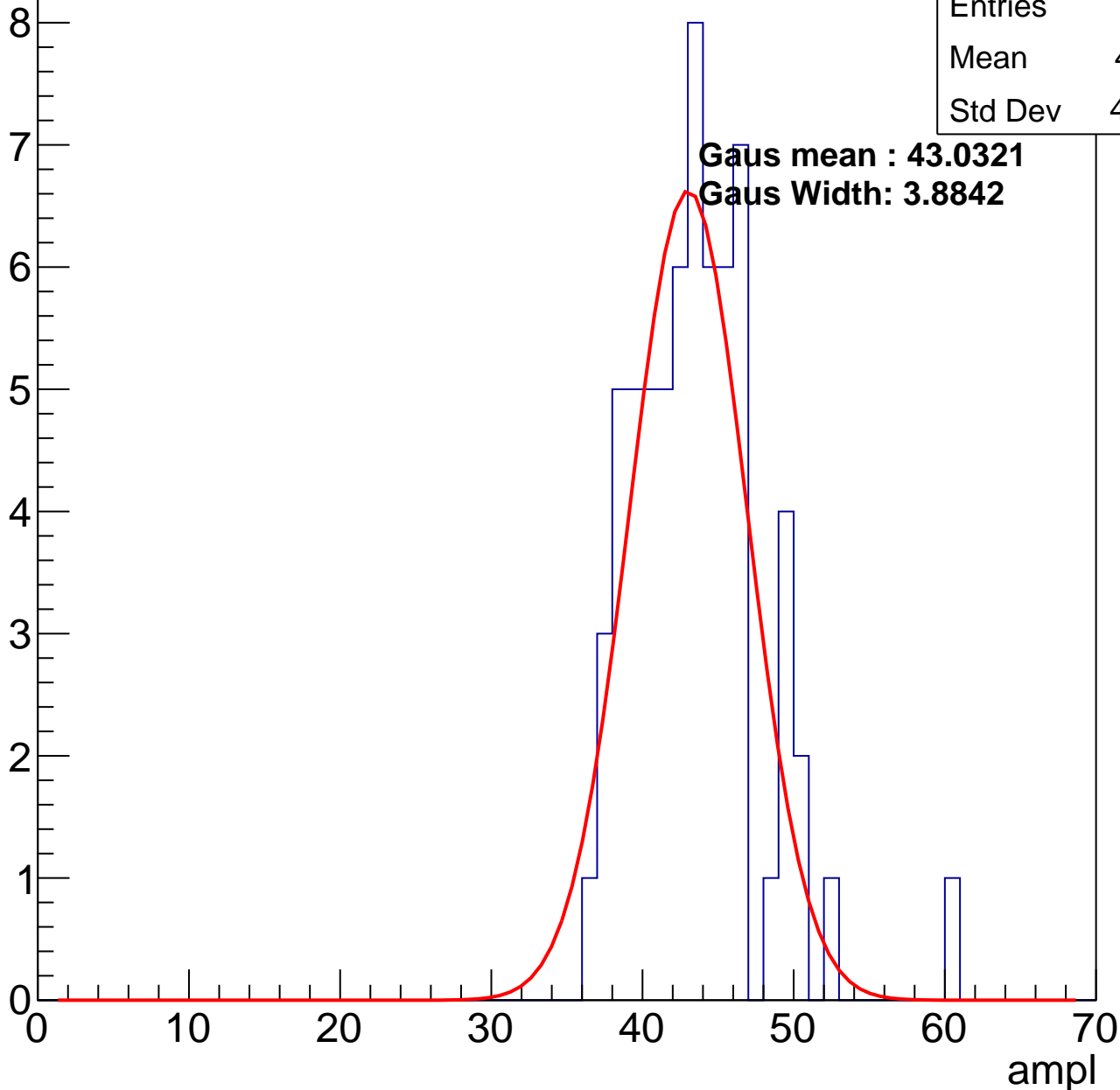
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	66
Mean	43.11
Std Dev	4.196

**Gaus mean : 43.0321**

**Gaus Width: 3.8842**



# B1L101S, U19-ch64, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

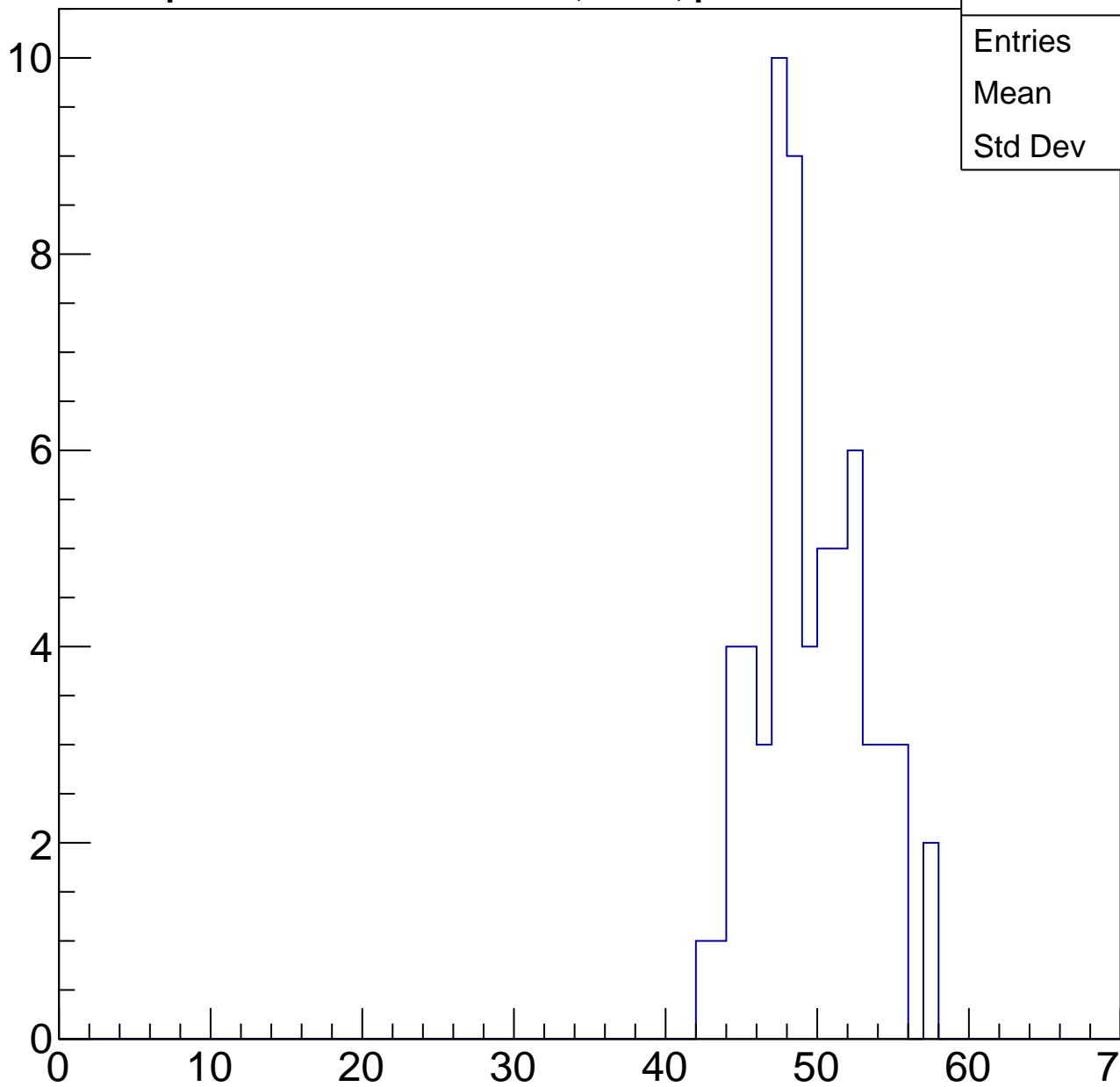
Entries	63
Mean	49.11
Std Dev	3.478

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

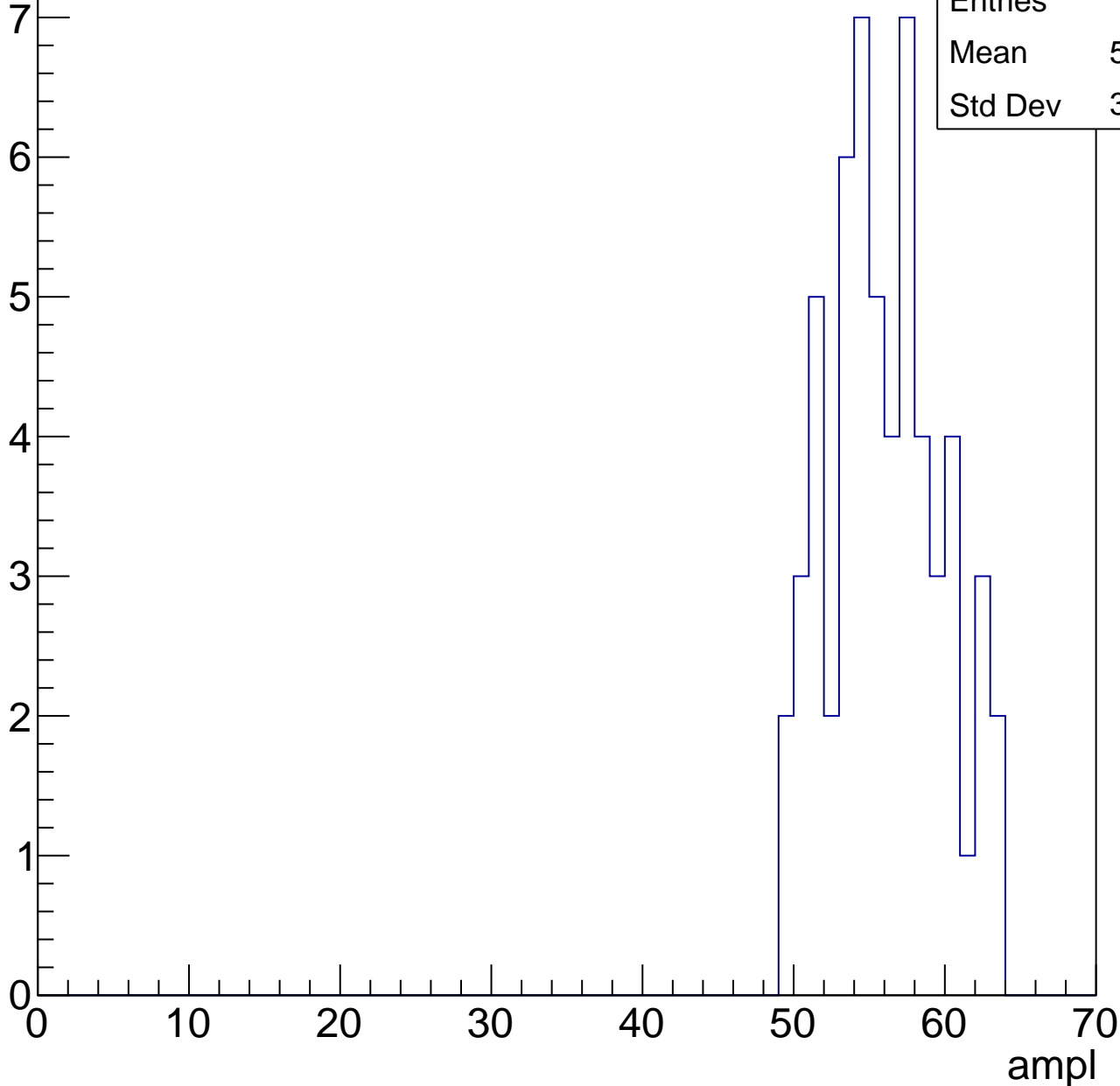


# B1L101S, U19-ch64, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	58
Mean	55.57
Std Dev	3.677

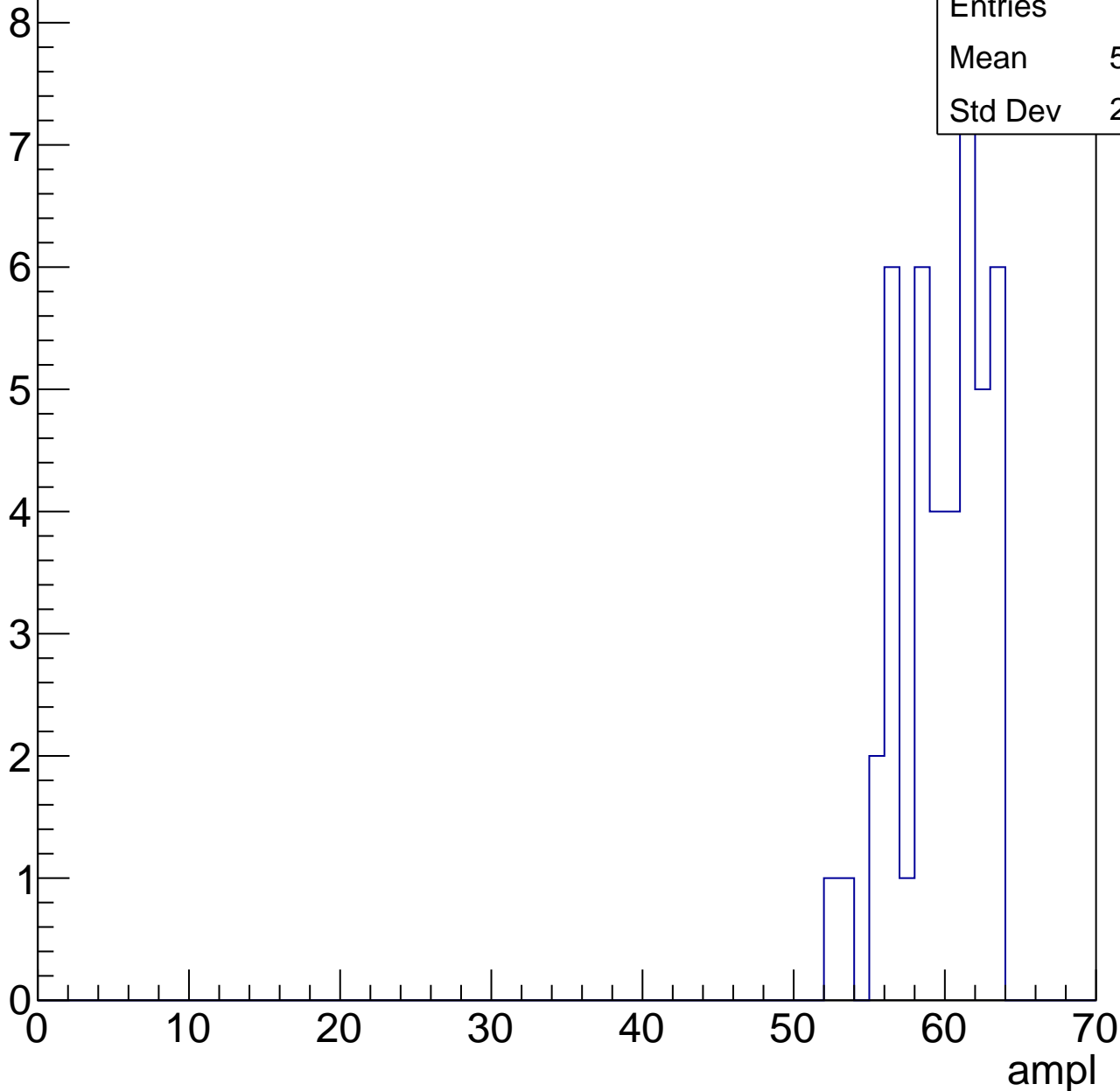


# B1L101S, U19-ch64, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

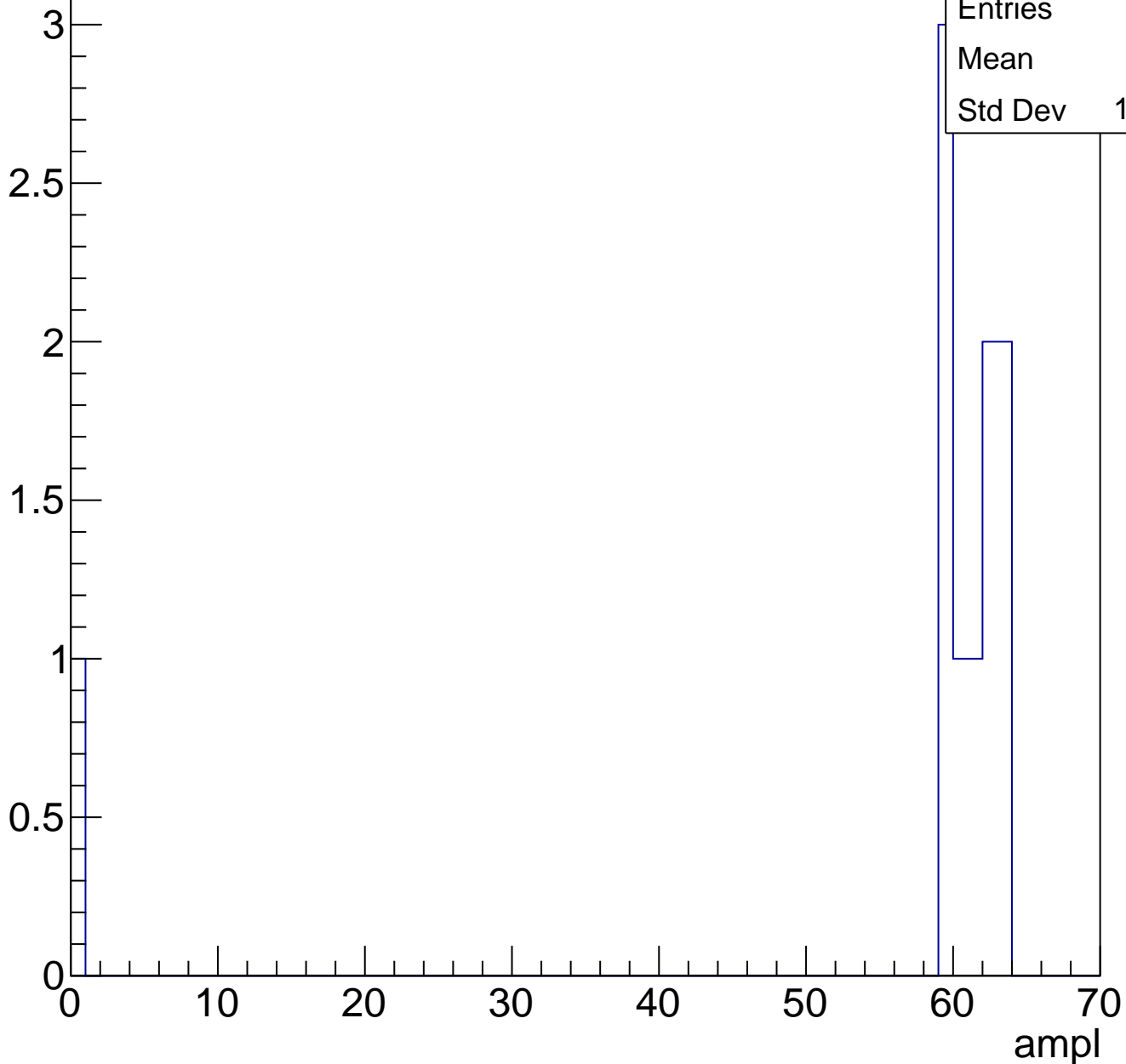
Entries	44
Mean	59.27
Std Dev	2.839



# B1L101S, U19-ch64, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U19-ch64, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L101S, U19-ch65, adc0

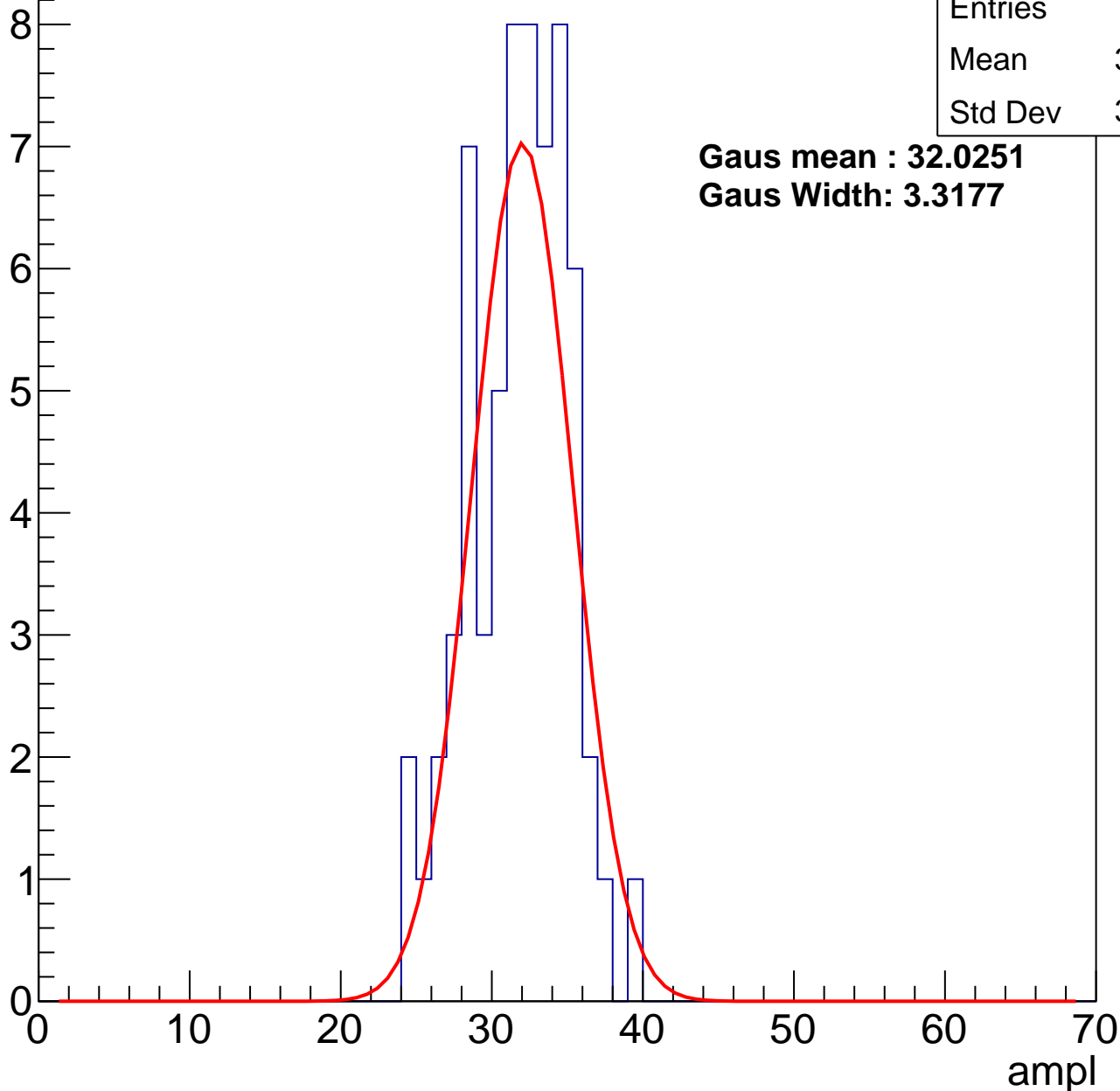
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	31.31
Std Dev	3.211

**Gaus mean : 32.0251**

**Gaus Width: 3.3177**



# B1L101S, U19-ch65, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	82
Mean	39.12
Std Dev	3.746

**Gaus mean : 39.6140**

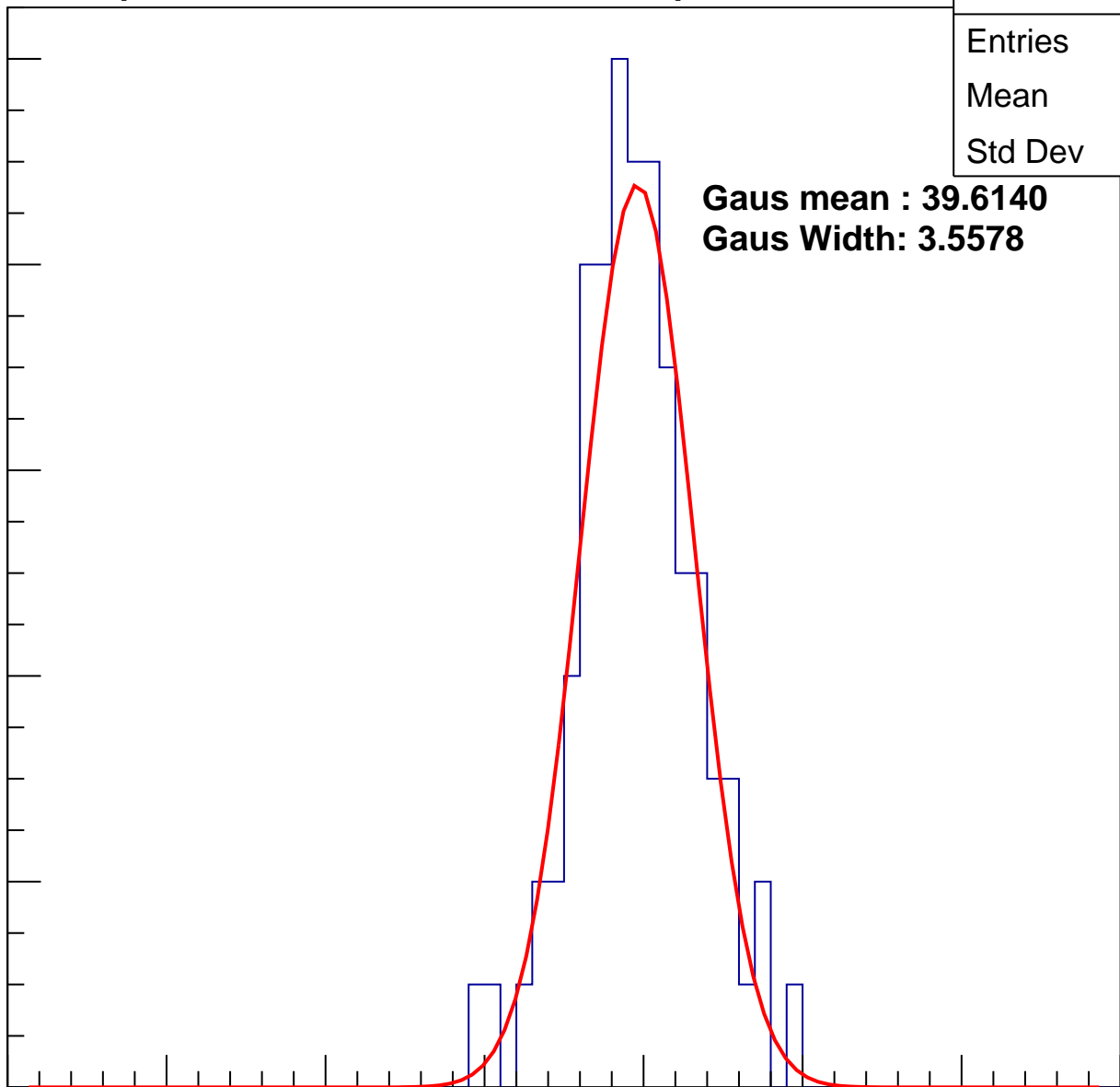
**Gaus Width: 3.5578**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B1L101S, U19-ch65, adc2

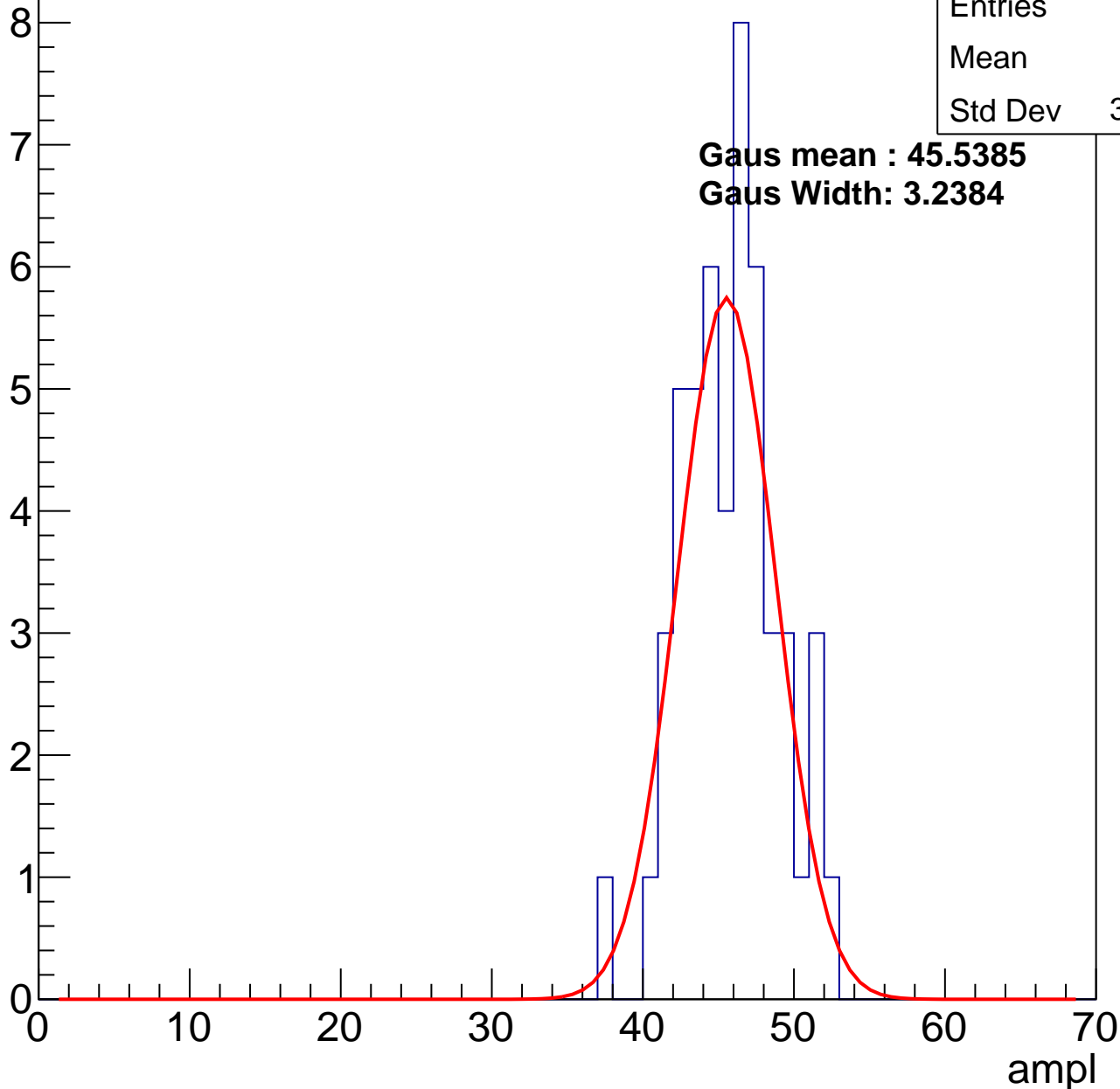
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	50
Mean	45.3
Std Dev	3.138

**Gaus mean : 45.5385**

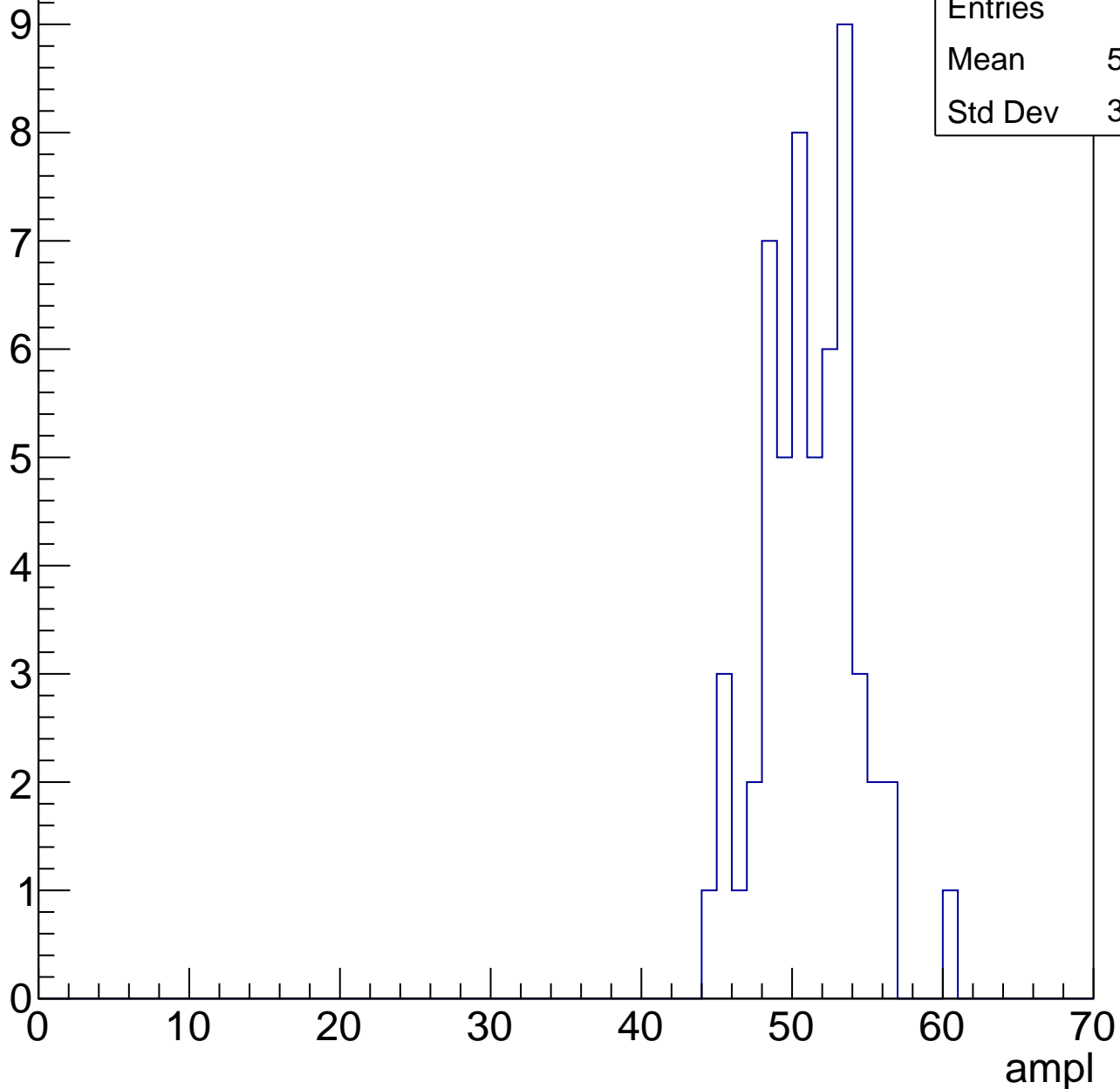
**Gaus Width: 3.2384**



# B1L101S, U19-ch65, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

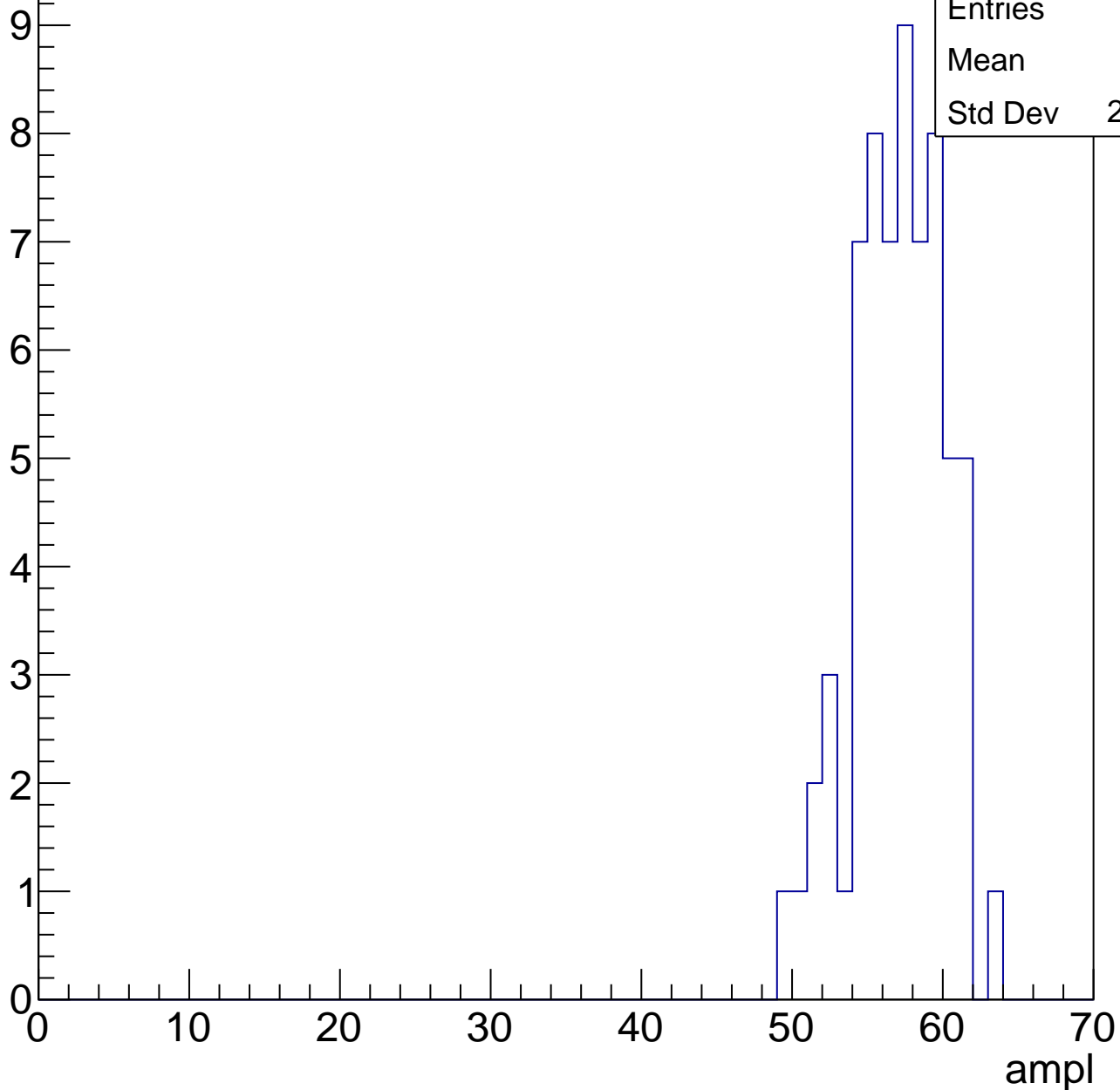
Entry



# B1L101S, U19-ch65, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

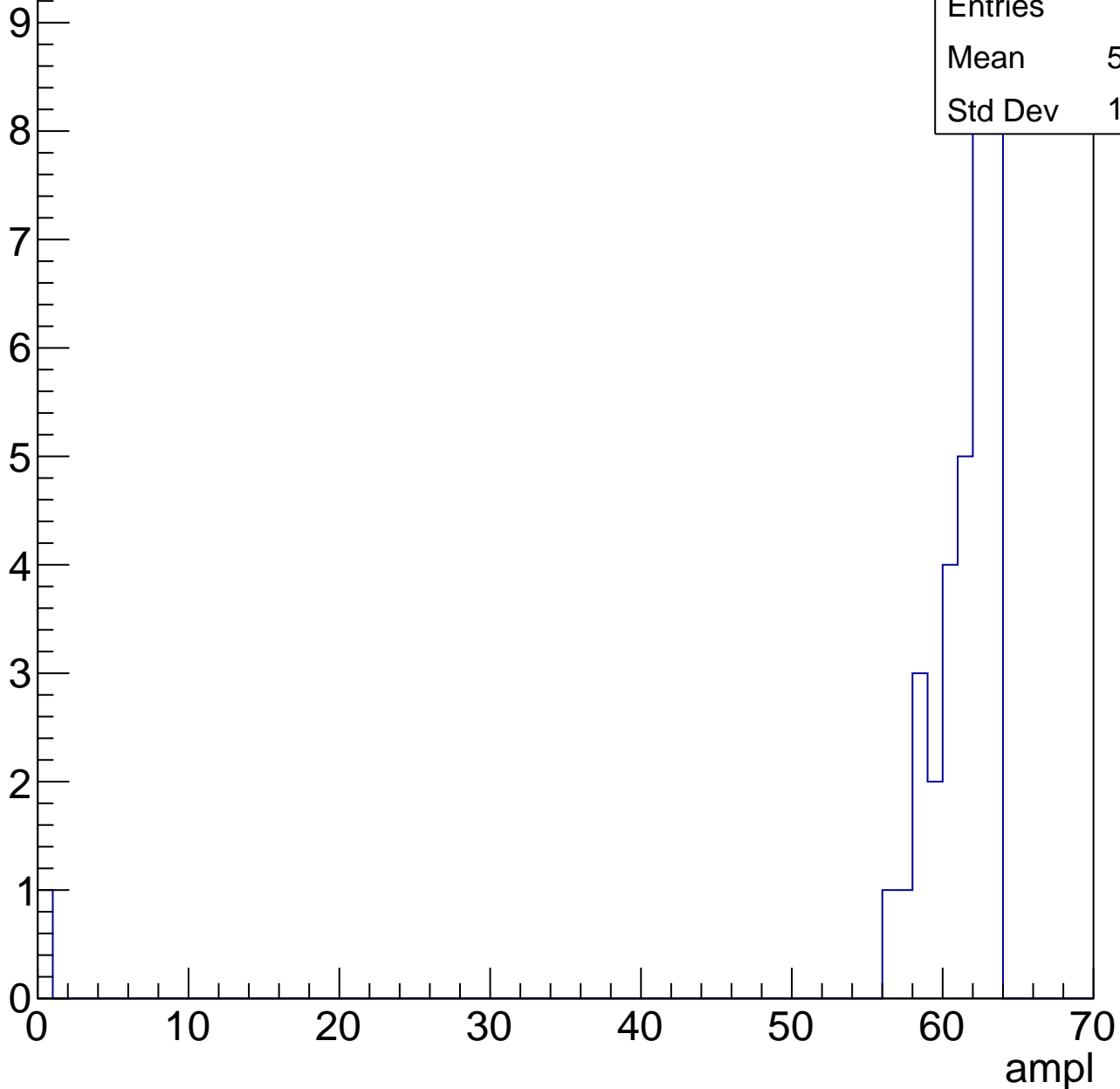


# B1L101S, U19-ch65, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	35
Mean	59.29
Std Dev	10.34



# B1L101S, U19-ch65, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U19-ch65, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U19-ch66, adc0

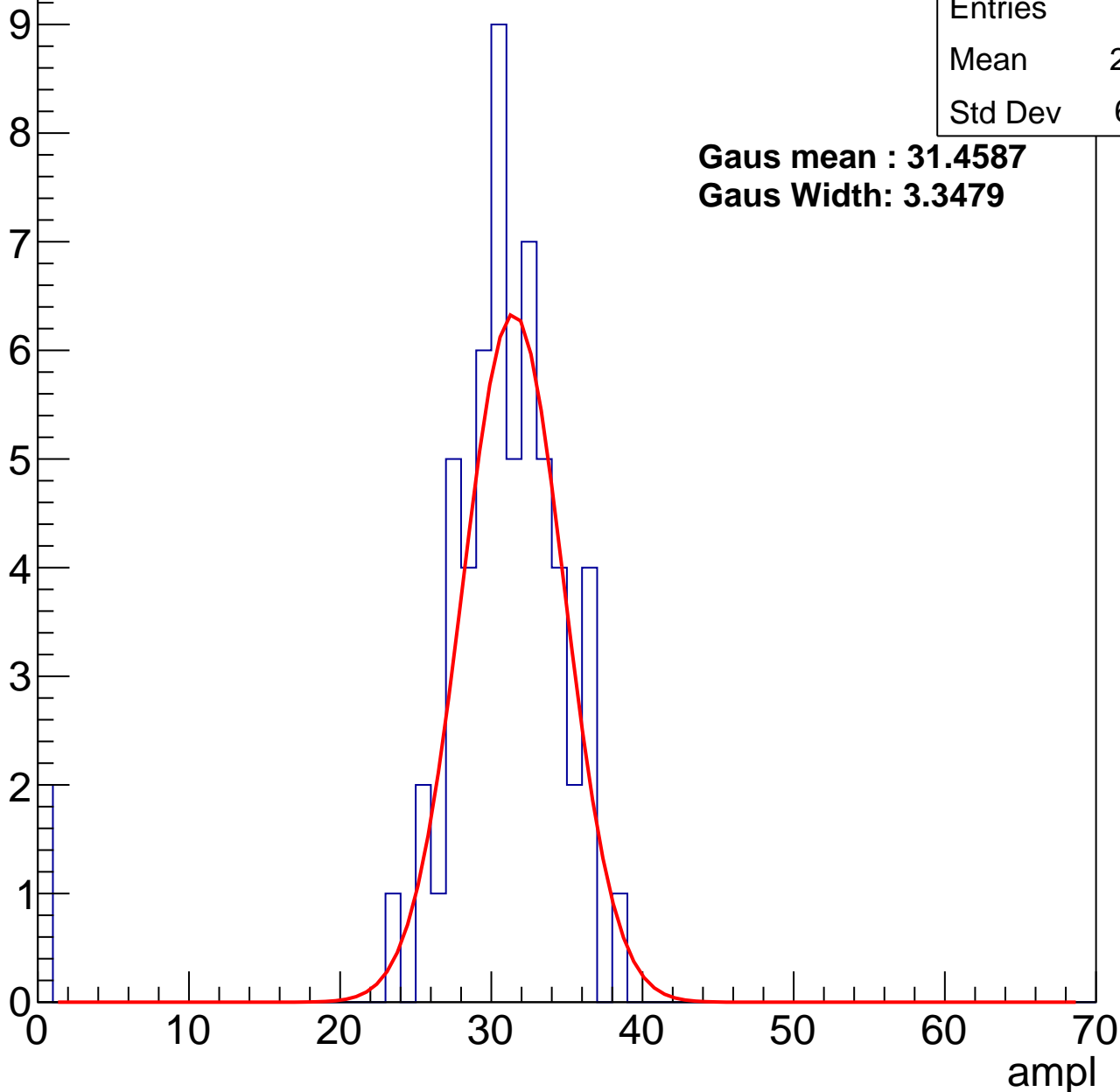
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	58
Mean	29.69
Std Dev	6.401

**Gaus mean : 31.4587**

**Gaus Width: 3.3479**



# B1L101S, U19-ch66, adc1

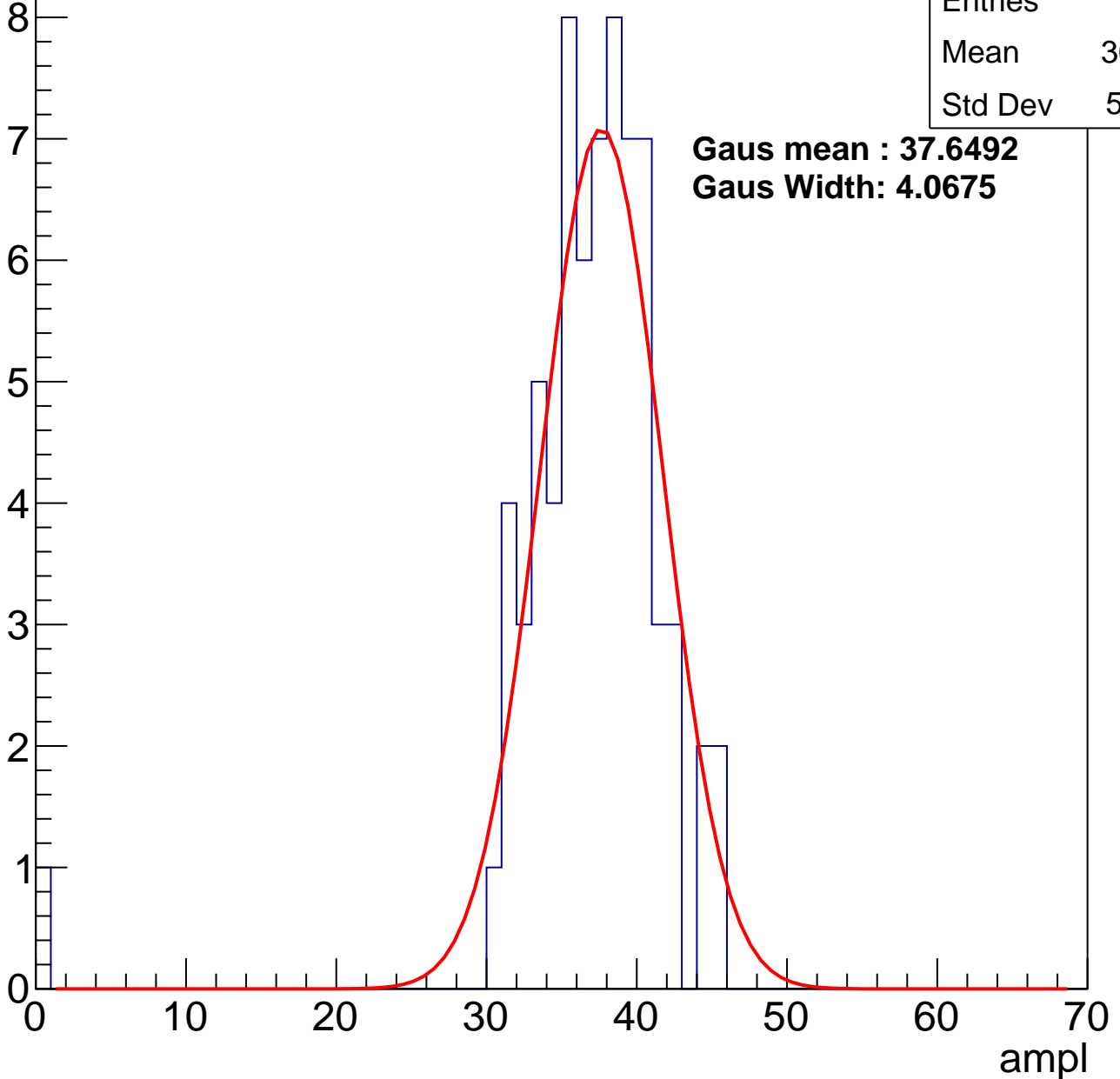
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	71
Mean	36.48
Std Dev	5.591

**Gaus mean : 37.6492**

**Gaus Width: 4.0675**



# B1L101S, U19-ch66, adc2

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	81
Mean	44.21
Std Dev	3.968

**Gaus mean : 44.9914**

**Gaus Width: 3.7226**

10

8

6

4

2

0

0

10

20

30

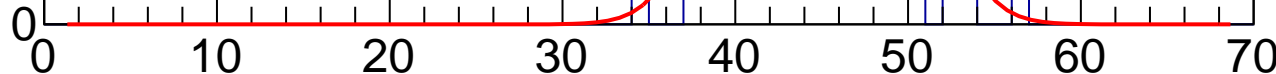
40

50

60

70

ampl

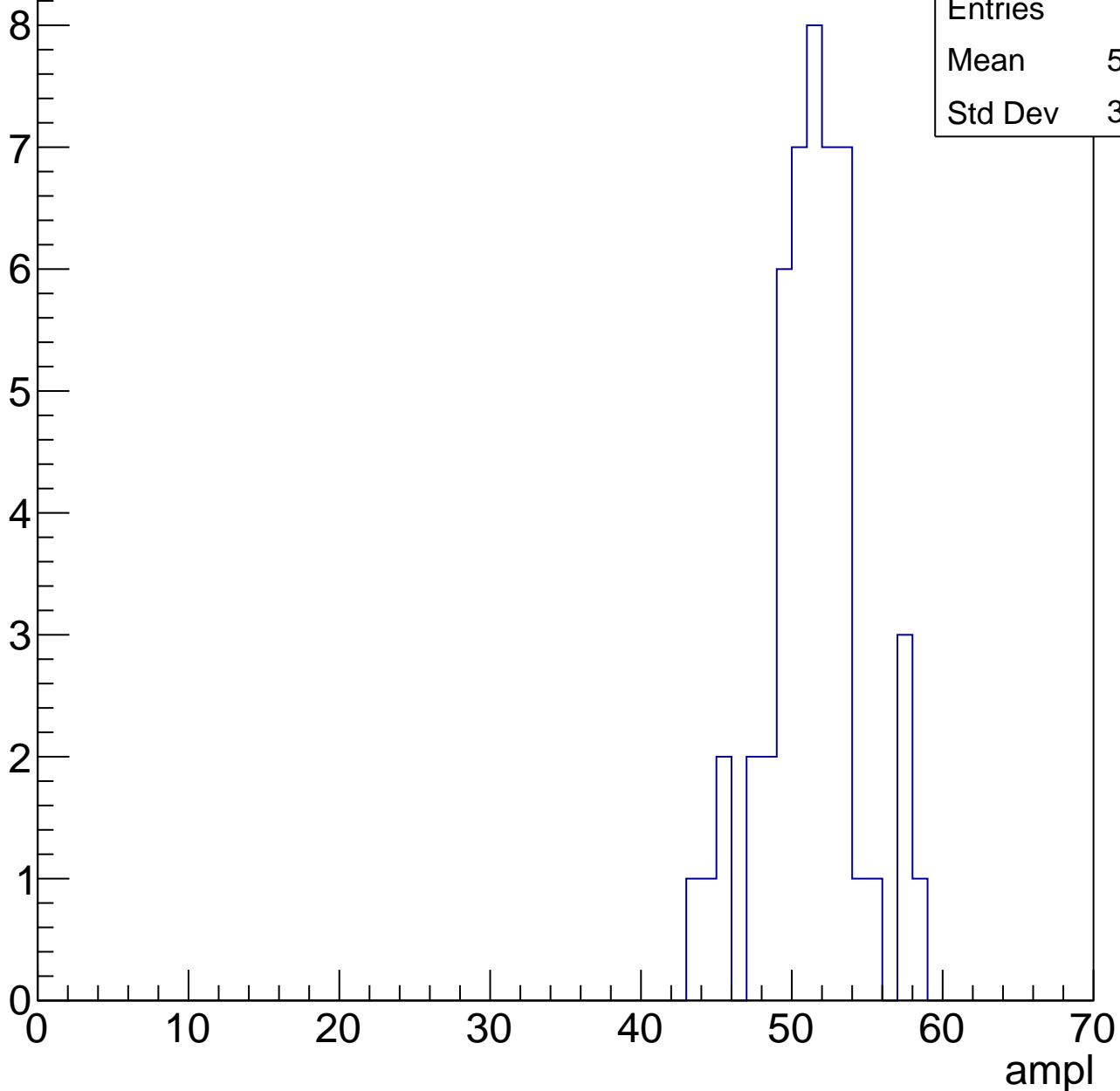


# B1L101S, U19-ch66, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	49
Mean	50.86
Std Dev	3.136

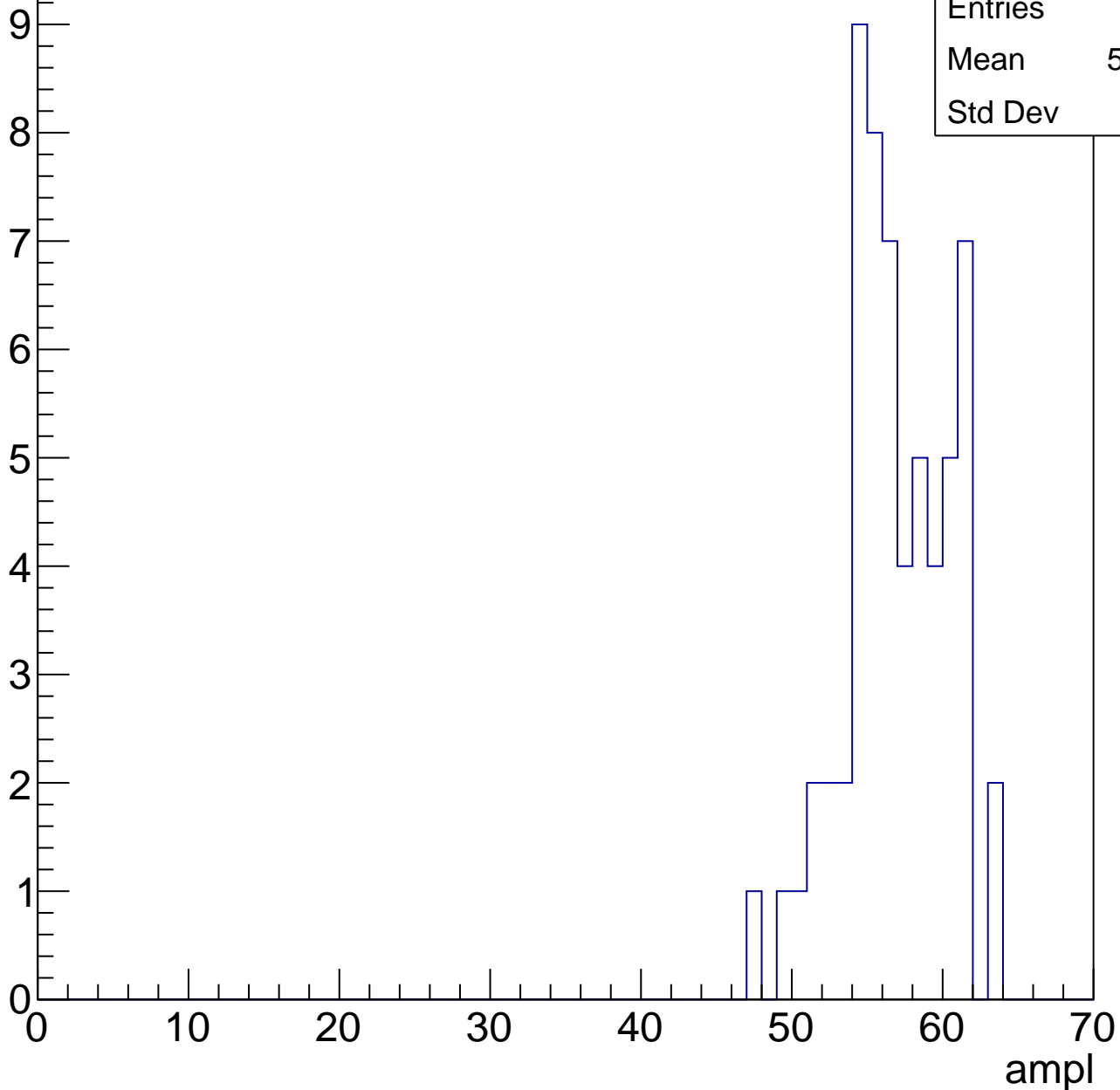


# B1L101S, U19-ch66, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	60
Mean	56.38
Std Dev	3.45

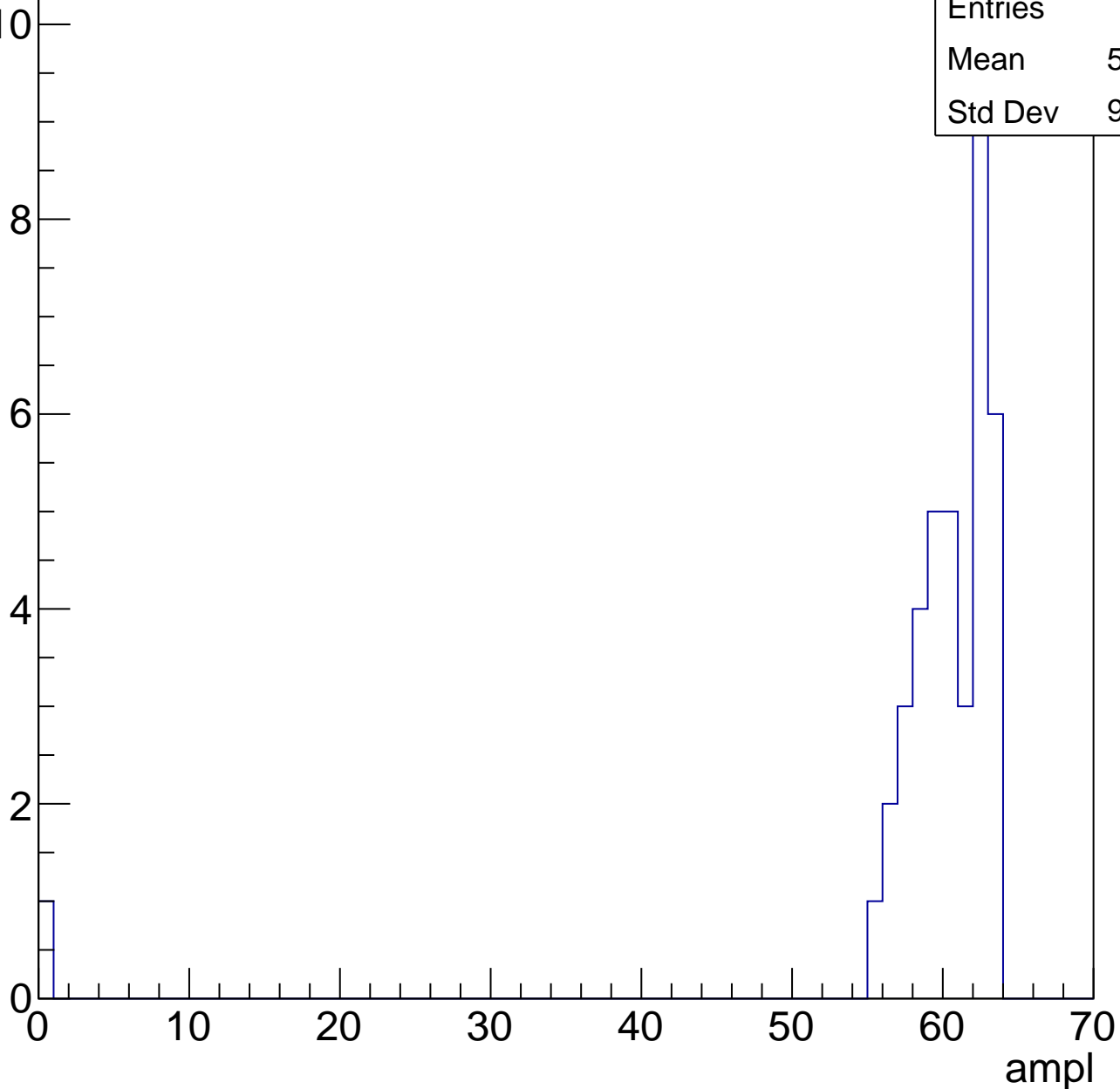


# B1L101S, U19-ch66, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	40
Mean	58.65
Std Dev	9.655



# B1L101S, U19-ch66, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

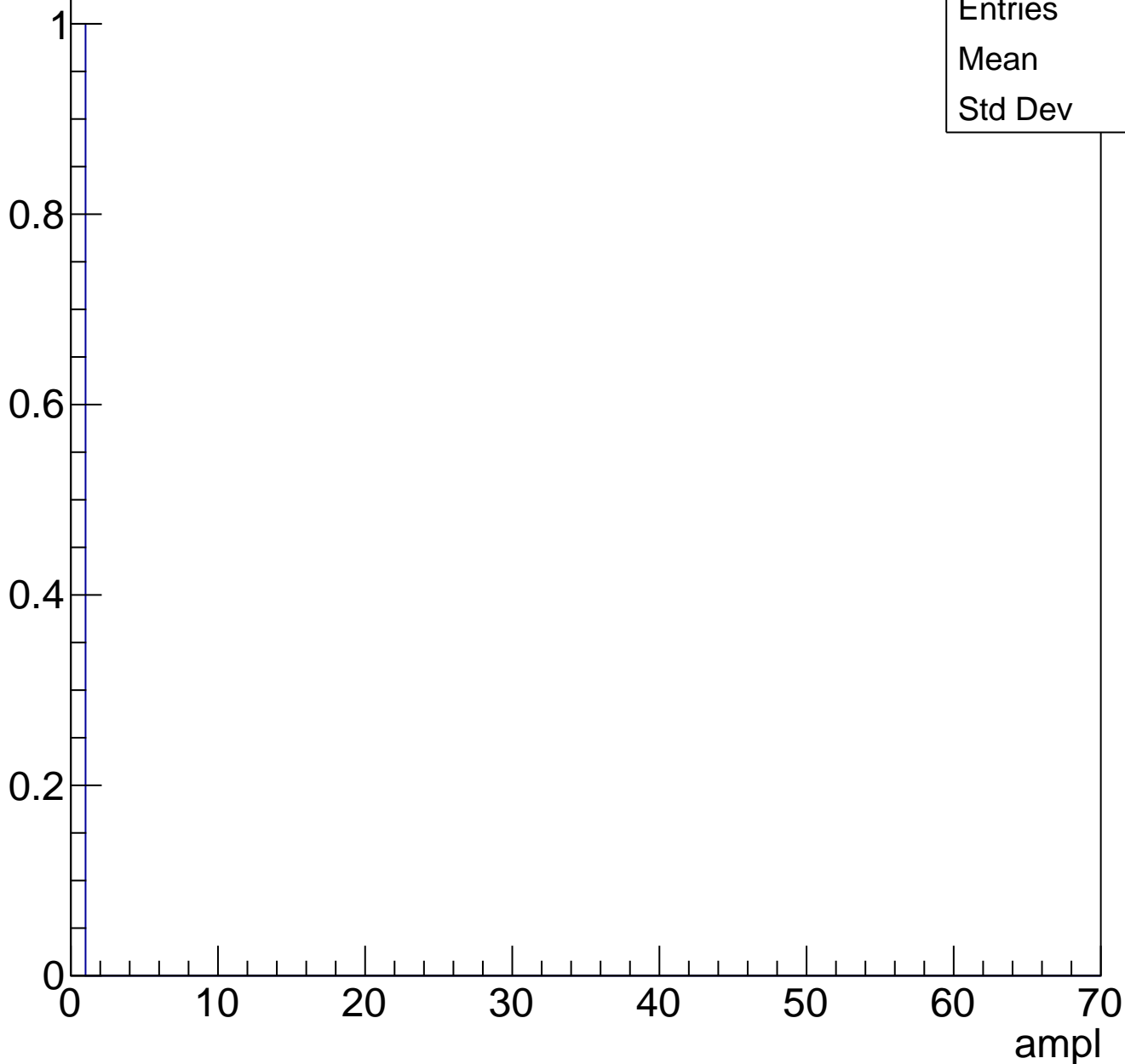




# B1L101S, U19-ch66, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U19-ch67, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	77
Mean	28.94
Std Dev	5.843

**Gaus mean : 29.9890**

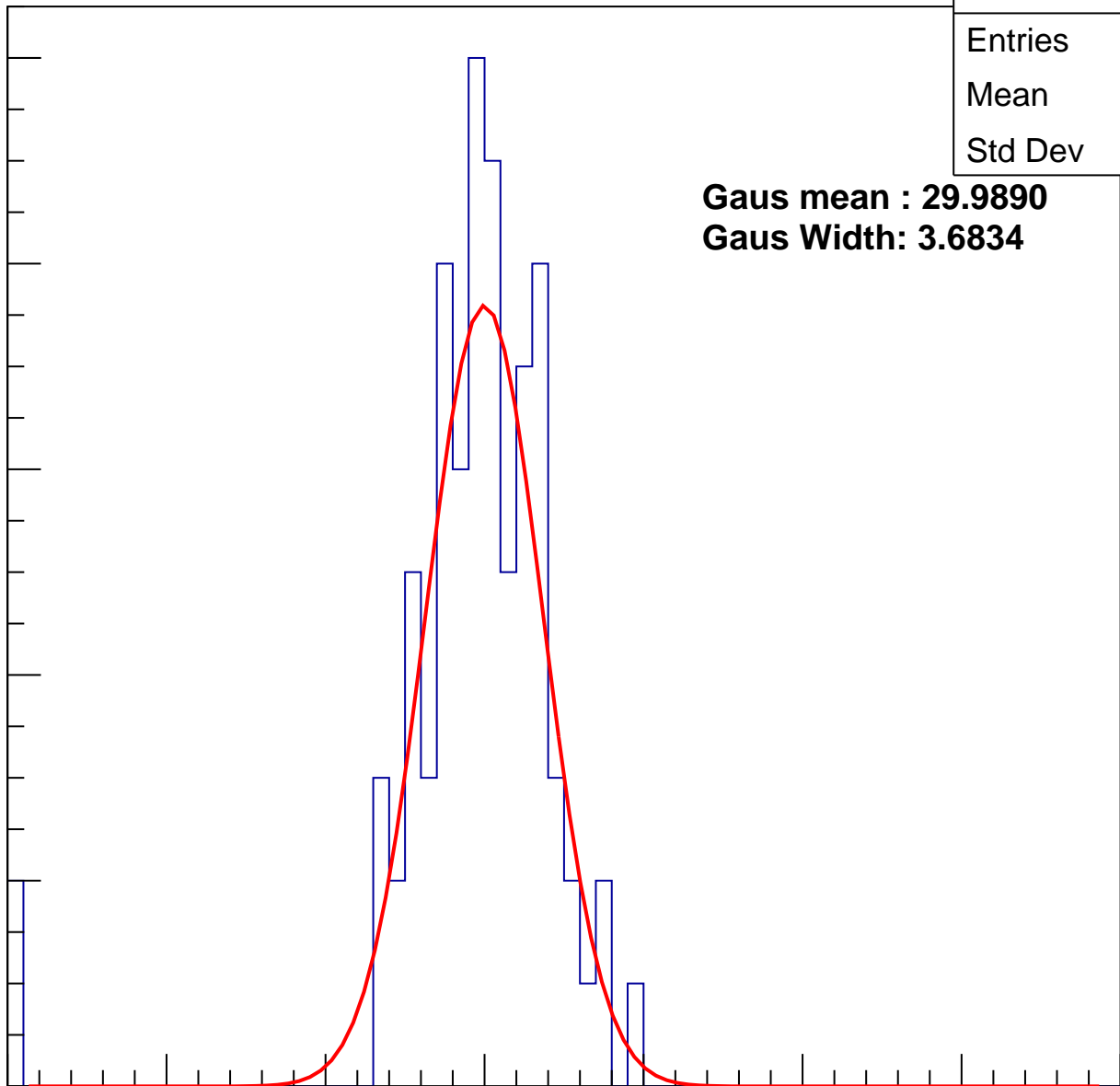
**Gaus Width: 3.6834**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



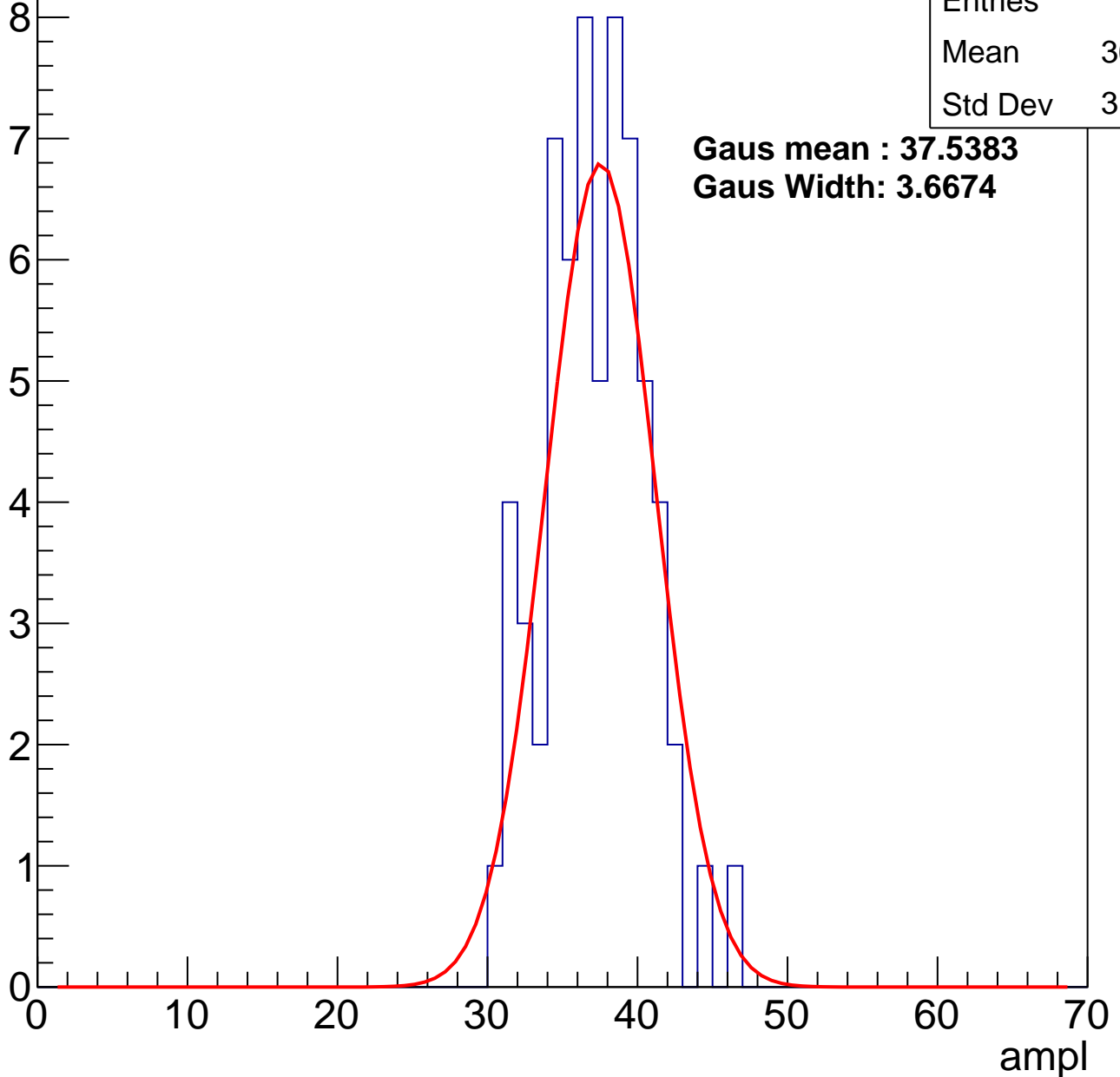
# B1L101S, U19-ch67, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	36.75
Std Dev	3.345

**Gaus mean : 37.5383**  
**Gaus Width: 3.6674**



# B1L101S, U19-ch67, adc2

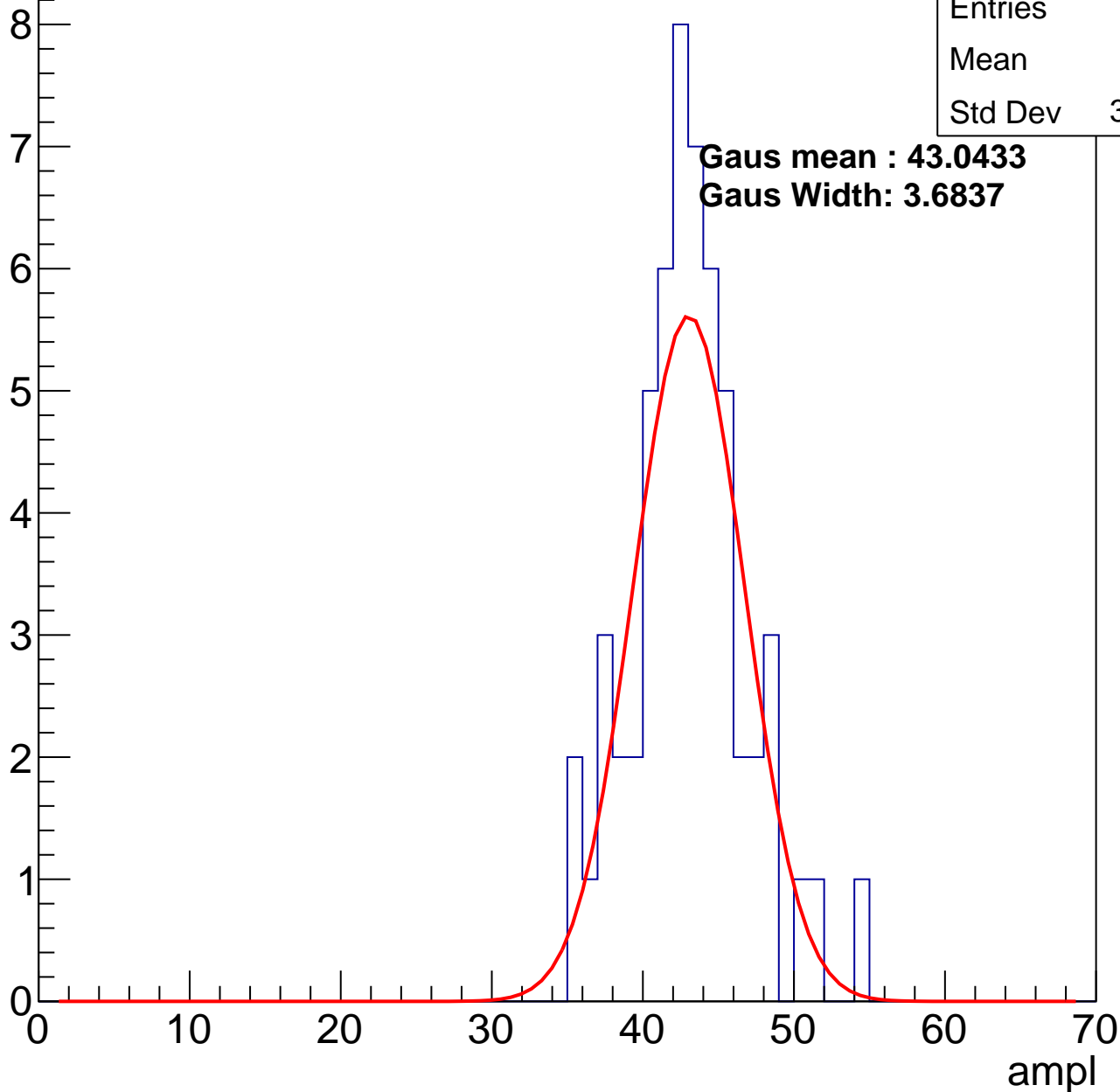
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	57
Mean	42.6
Std Dev	3.792

**Gaus mean : 43.0433**

**Gaus Width: 3.6837**



# B1L101S, U19-ch67, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	85
Mean	49.74
Std Dev	3.508

Entry

10

8

6

4

2

0

0

10

20

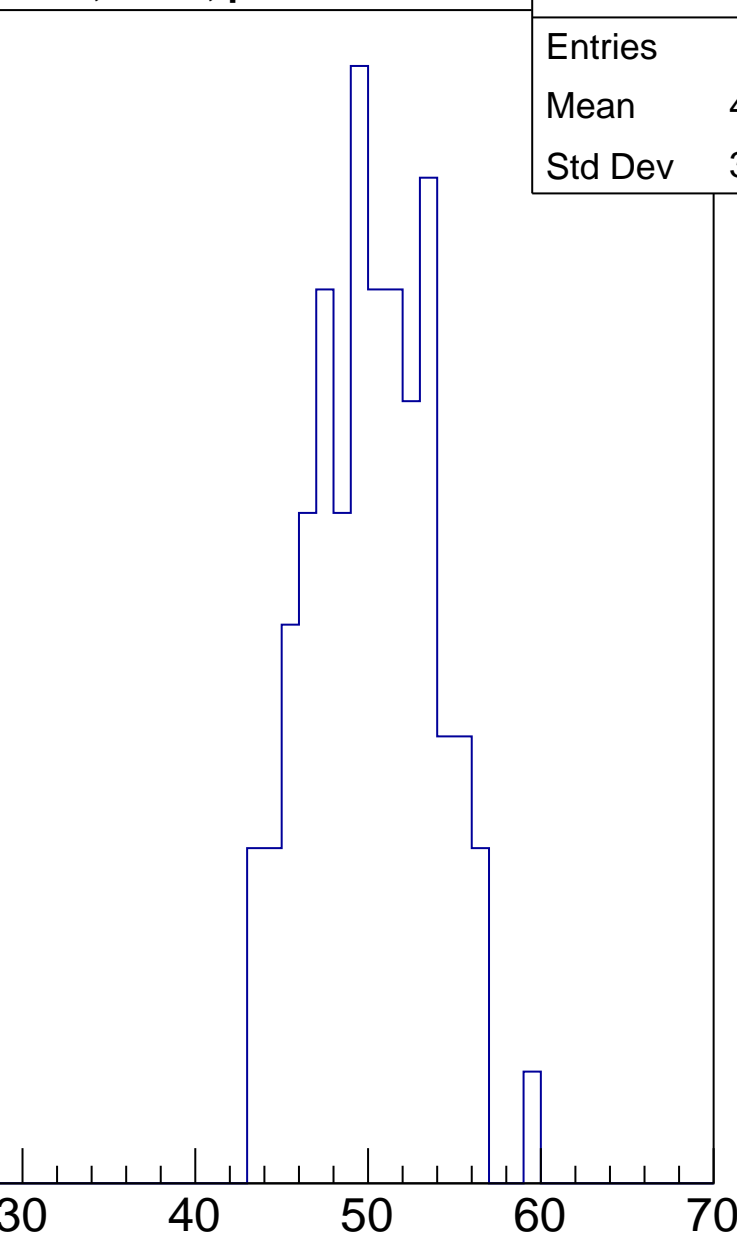
30

40

50

60

ampl

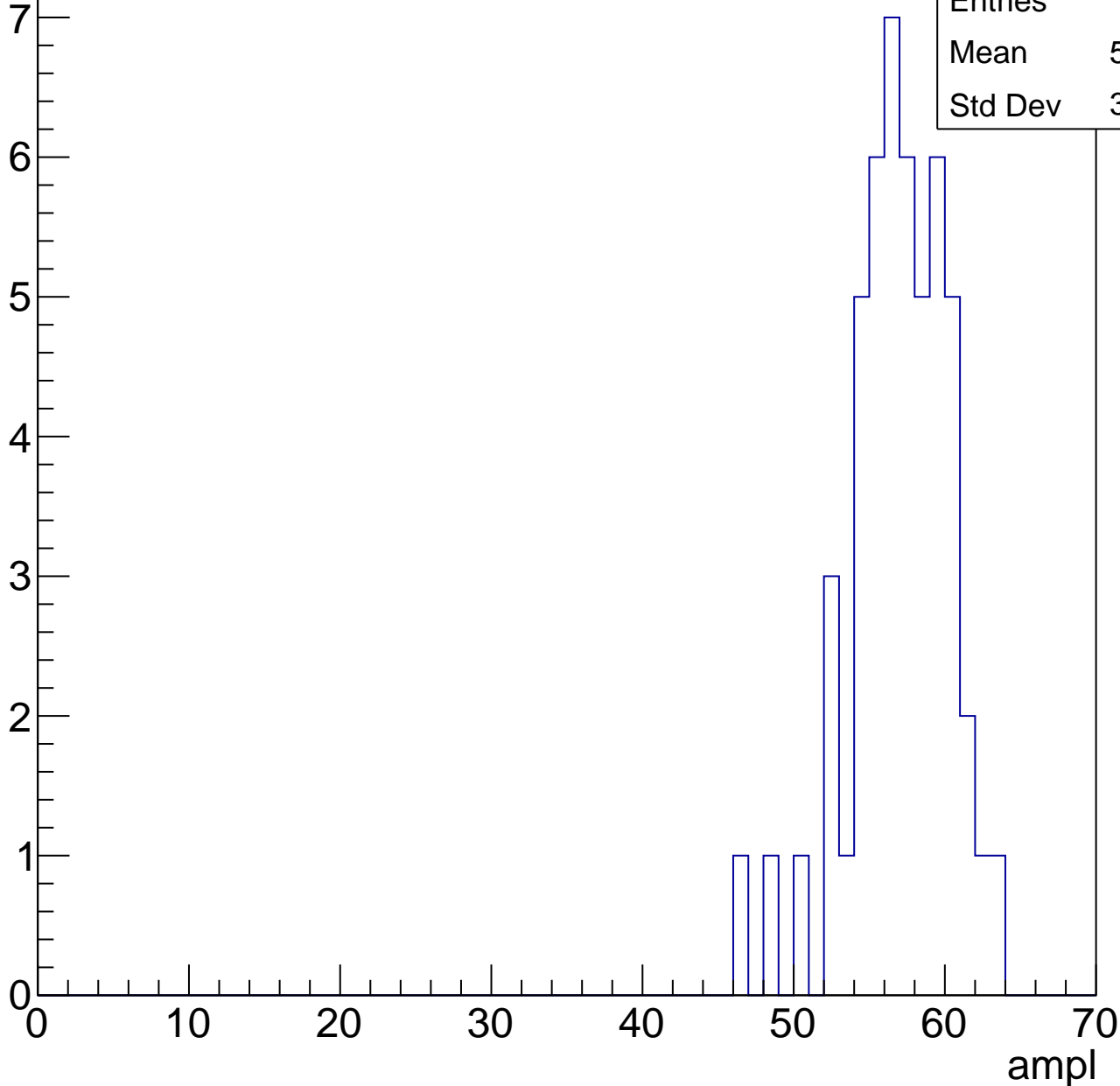


# B1L101S, U19-ch67, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	51
Mean	56.43
Std Dev	3.339

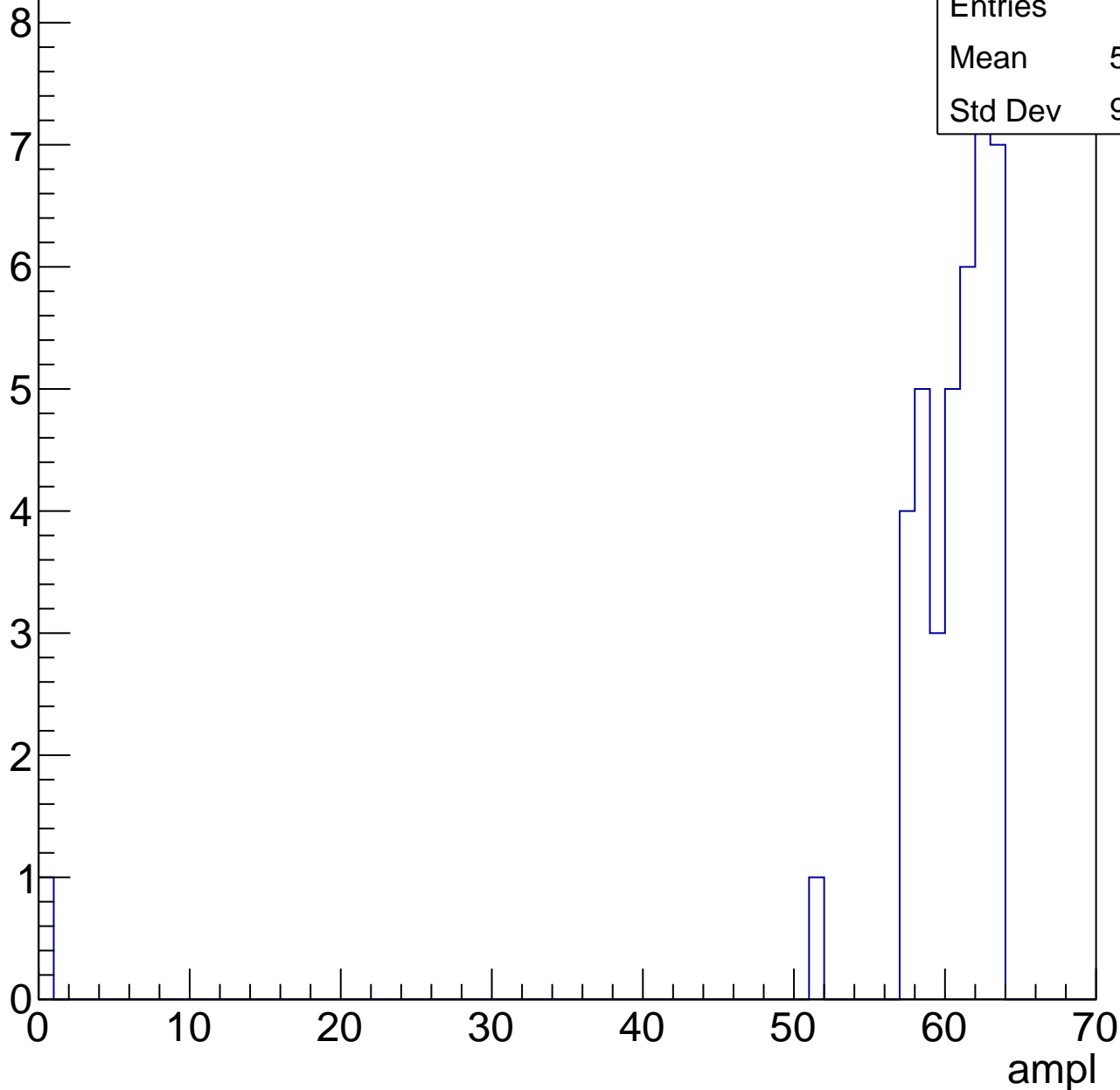


# B1L101S, U19-ch67, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	40
Mean	58.73
Std Dev	9.716



# B1L101S, U19-ch67, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

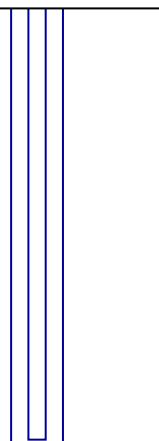
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	5
Mean	62
Std Dev	0.8944

0 10 20 30 40 50 60 70

ampl





# B1L101S, U19-ch67, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

1  
0.8  
0.6  
0.4  
0.2  
0

Entries	1
Mean	22
Std Dev	0

ampl

# B1L101S, U19-ch68, adc0

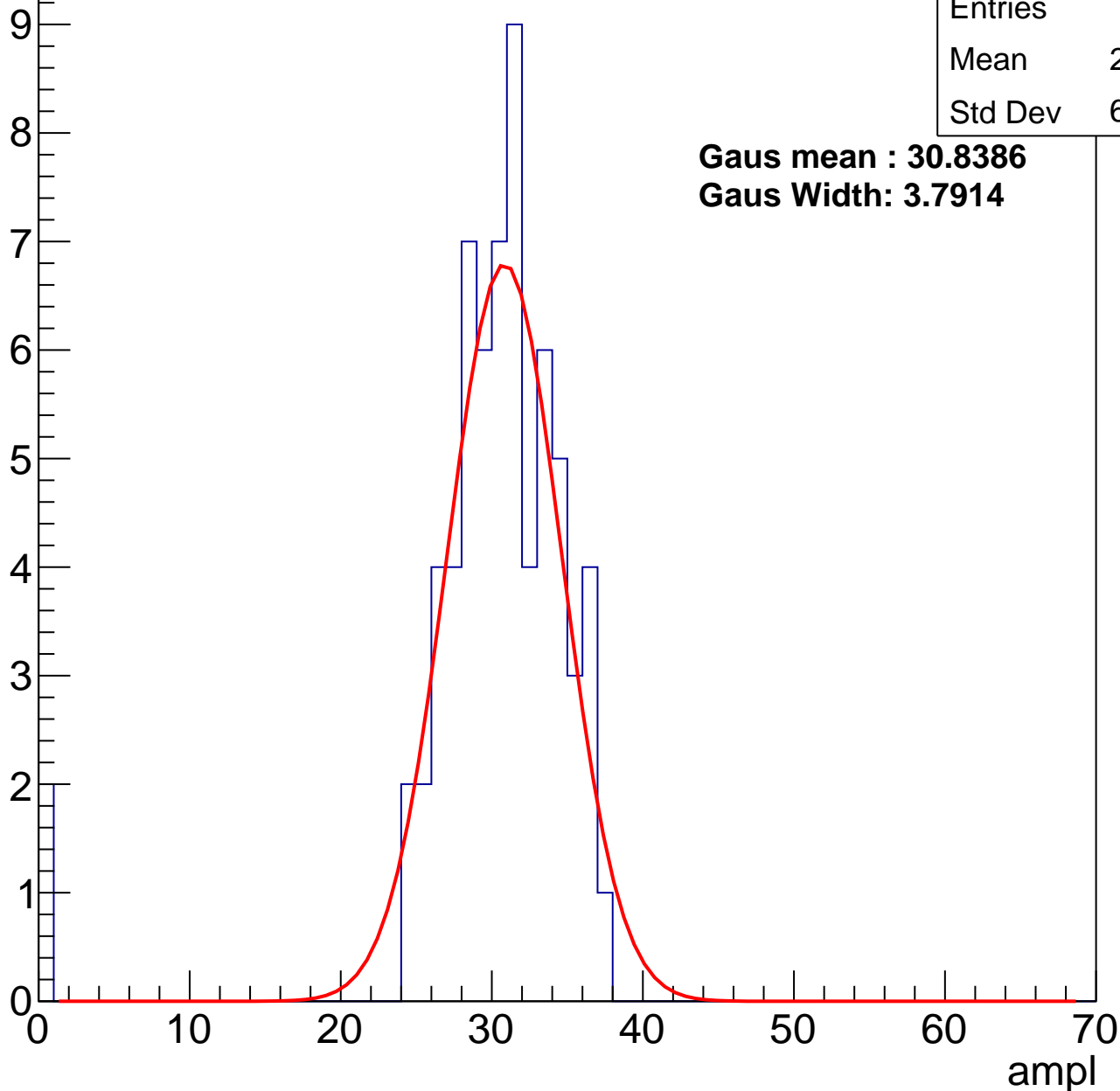
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	66
Mean	29.56
Std Dev	6.118

**Gaus mean : 30.8386**

**Gaus Width: 3.7914**



# B1L101S, U19-ch68, adc1

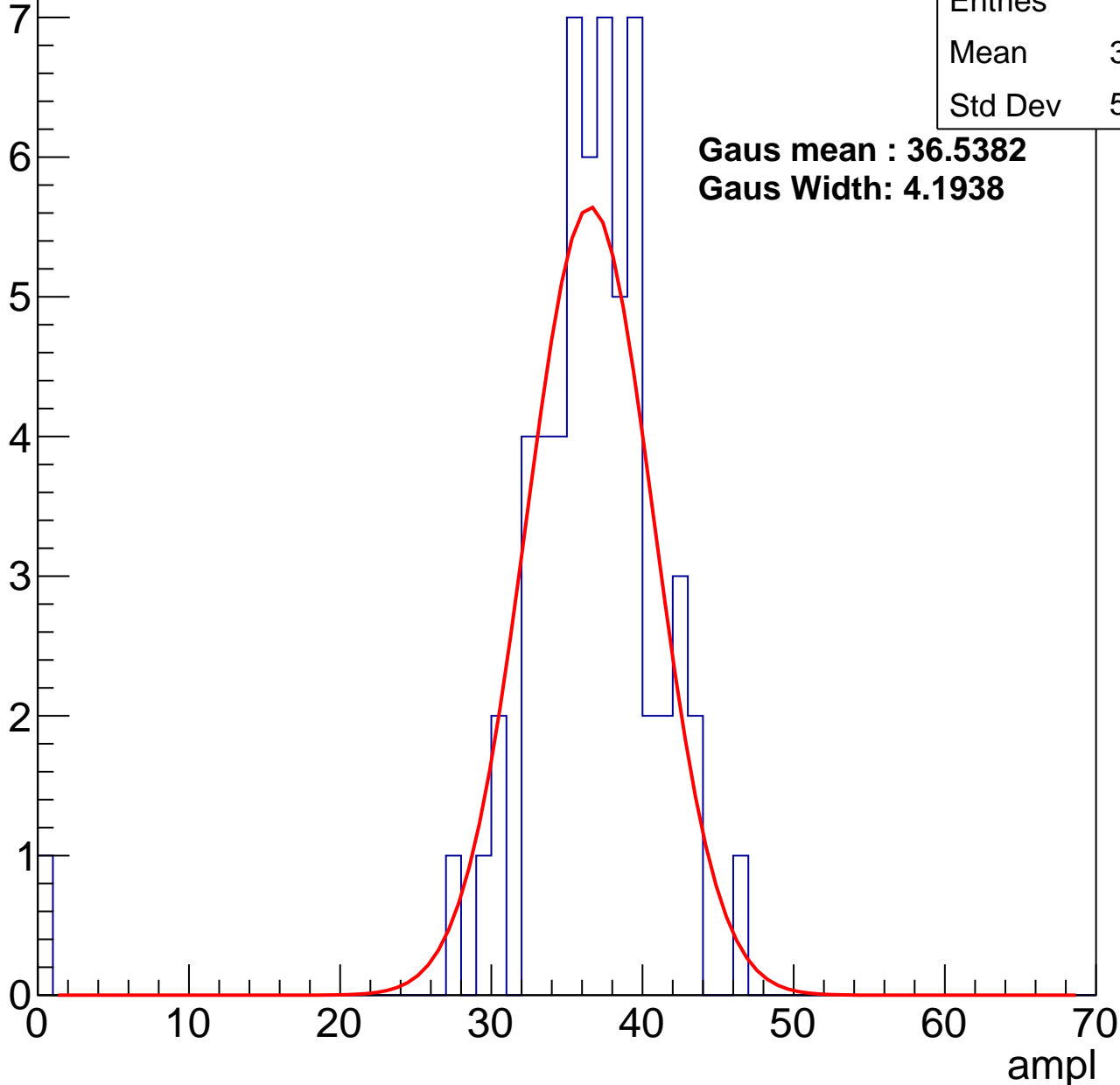
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	59
Mean	35.85
Std Dev	5.963

**Gaus mean : 36.5382**

**Gaus Width: 4.1938**



# B1L101S, U19-ch68, adc2

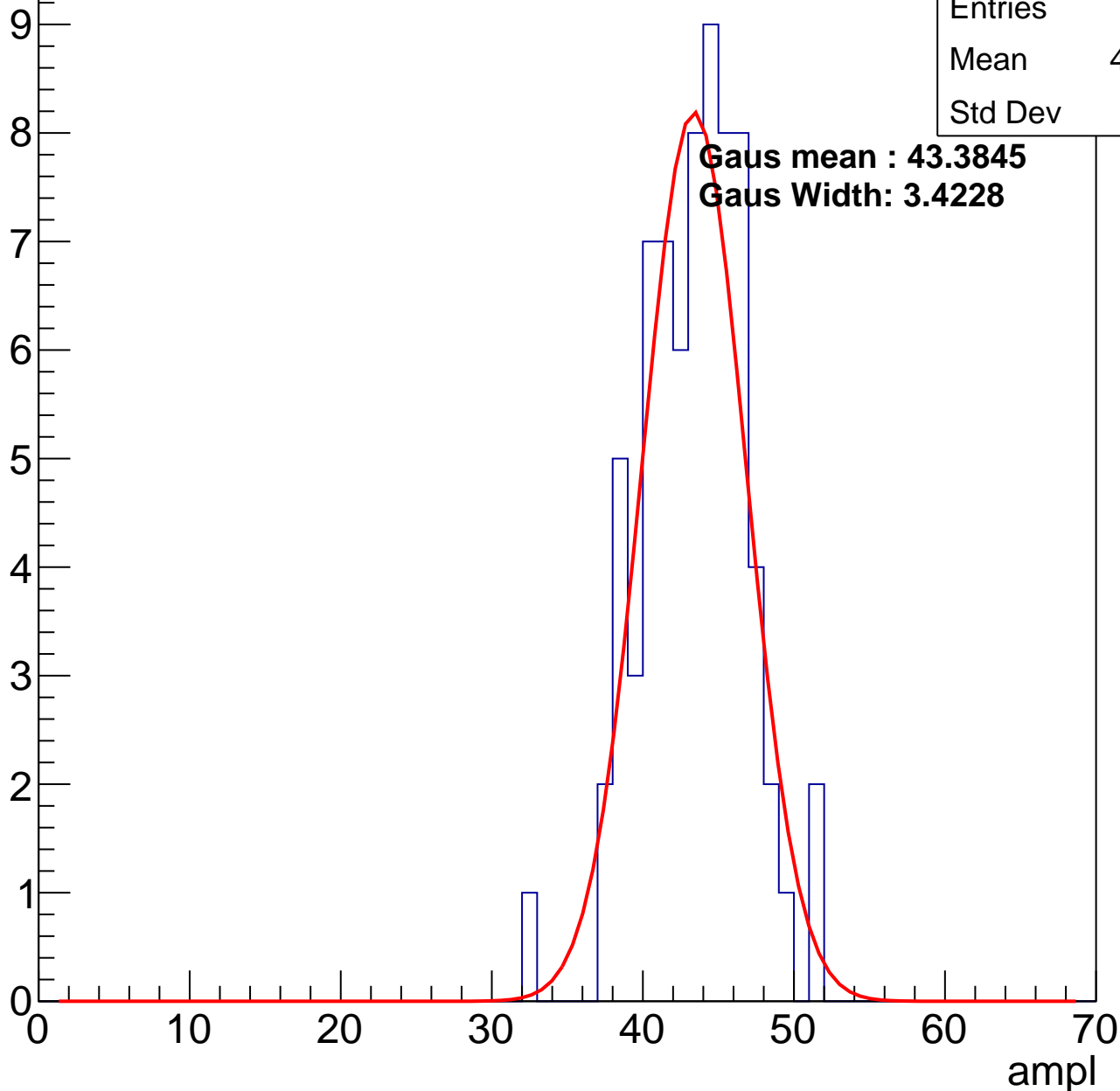
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	73
Mean	42.95
Std Dev	3.42

**Gaus mean : 43.3845**

**Gaus Width: 3.4228**

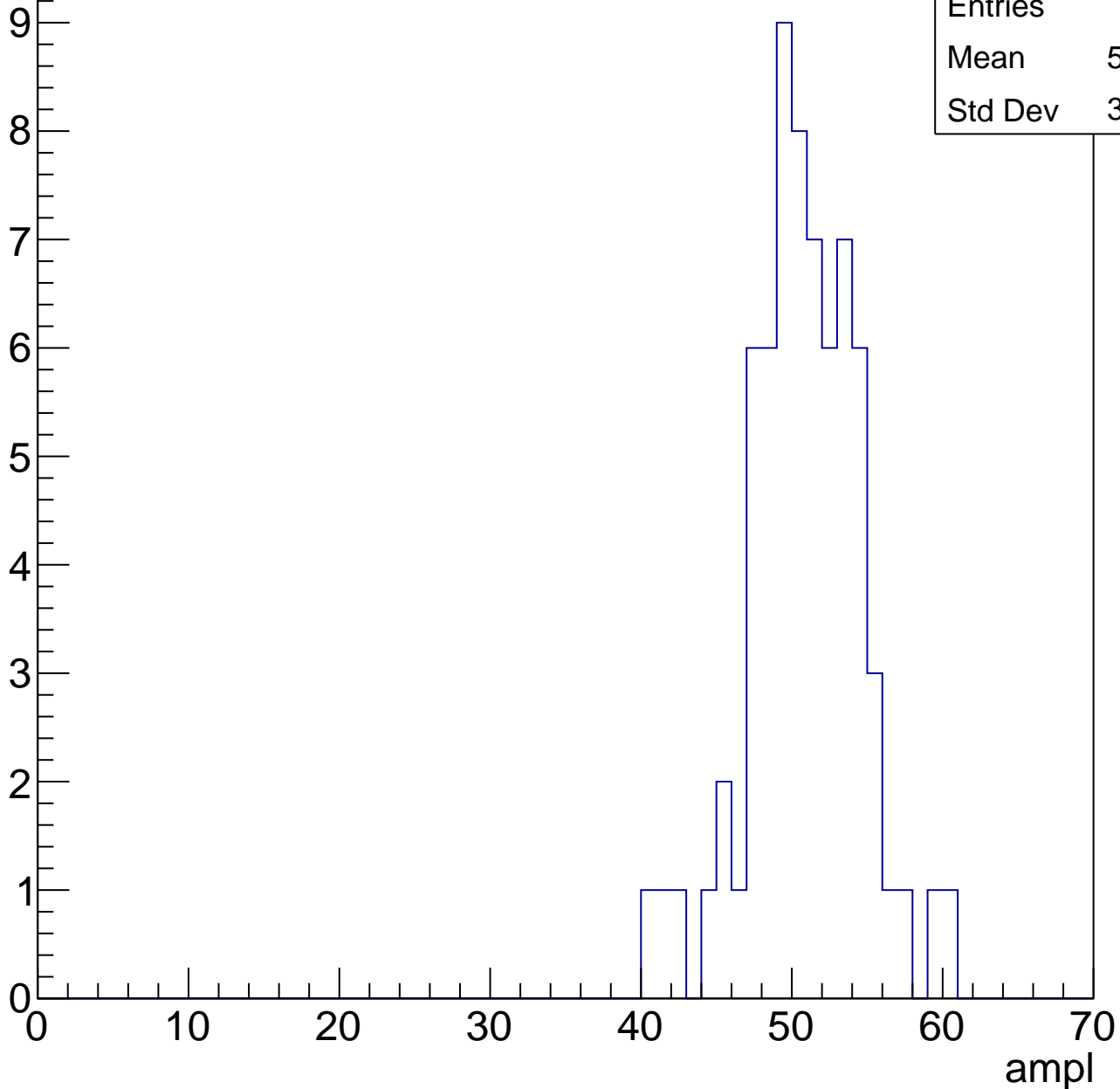


# B1L101S, U19-ch68, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	50.36
Std Dev	3.722

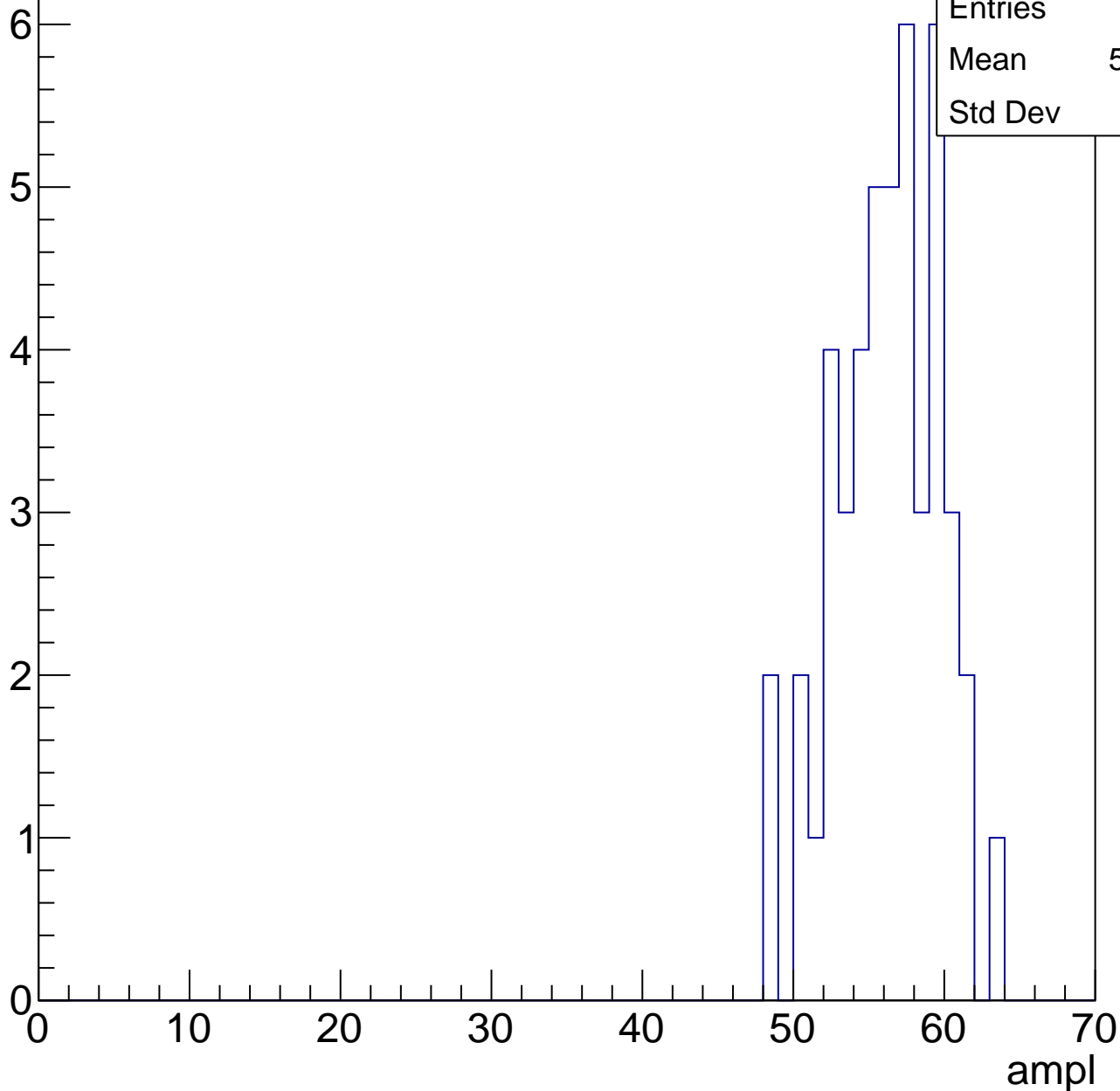


# B1L101S, U19-ch68, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

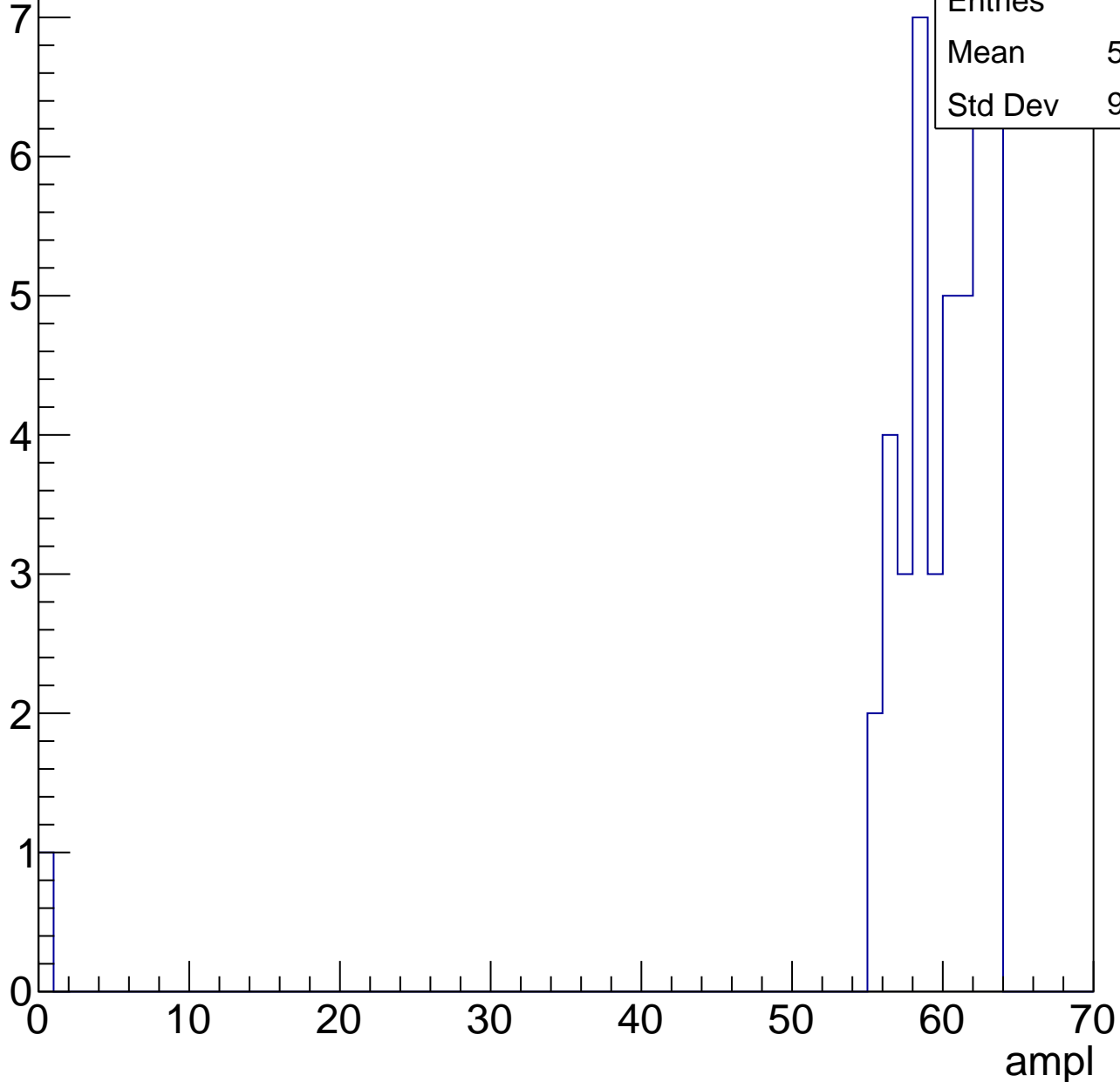
Entries	47
Mean	55.74
Std Dev	3.43



# B1L101S, U19-ch68, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

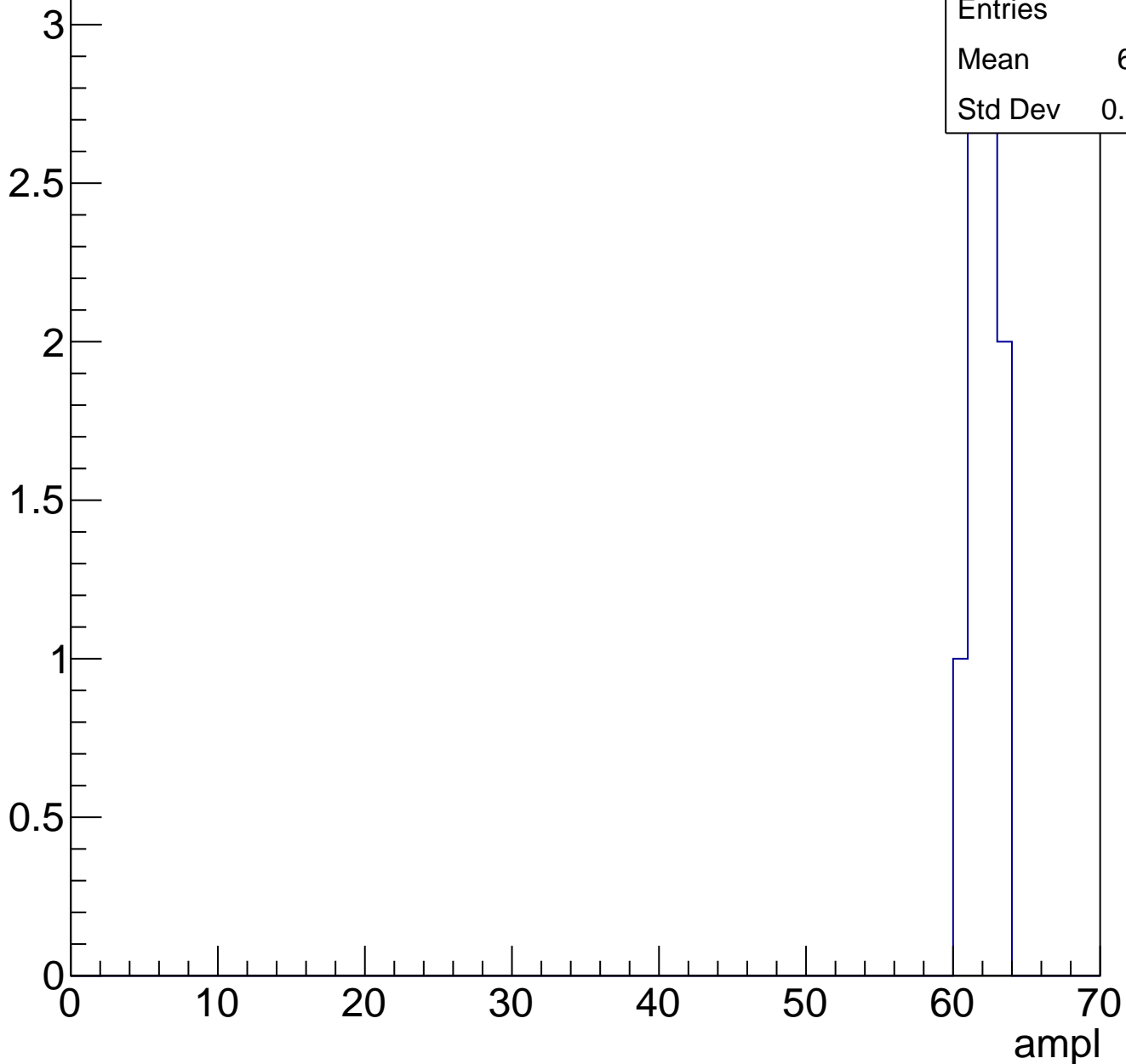
Entry



# B1L101S, U19-ch68, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U19-ch68, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U19-ch69, adc0

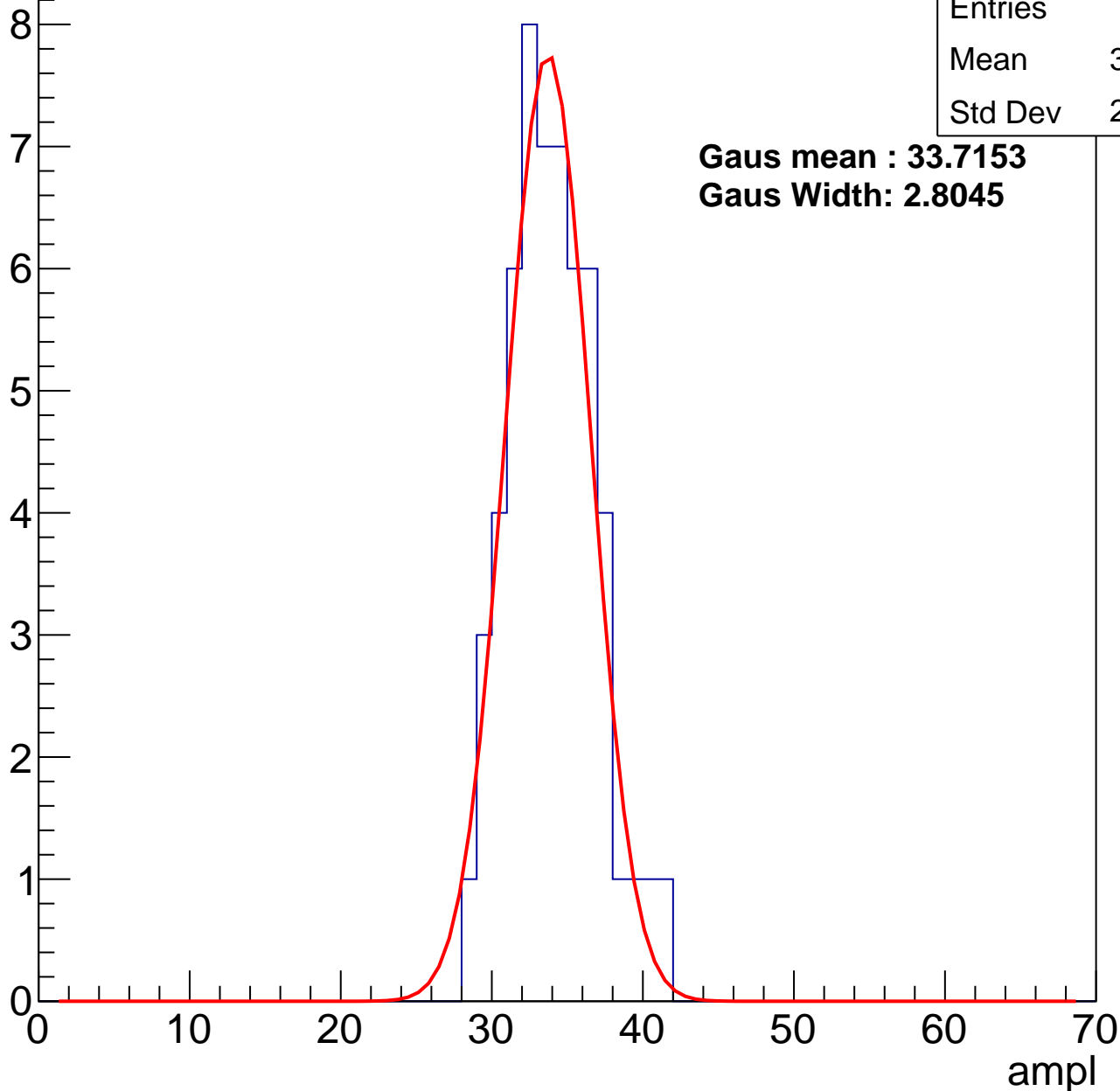
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	56
Mean	33.54
Std Dev	2.828

**Gaus mean : 33.7153**

**Gaus Width: 2.8045**



# B1L101S, U19-ch69, adc1

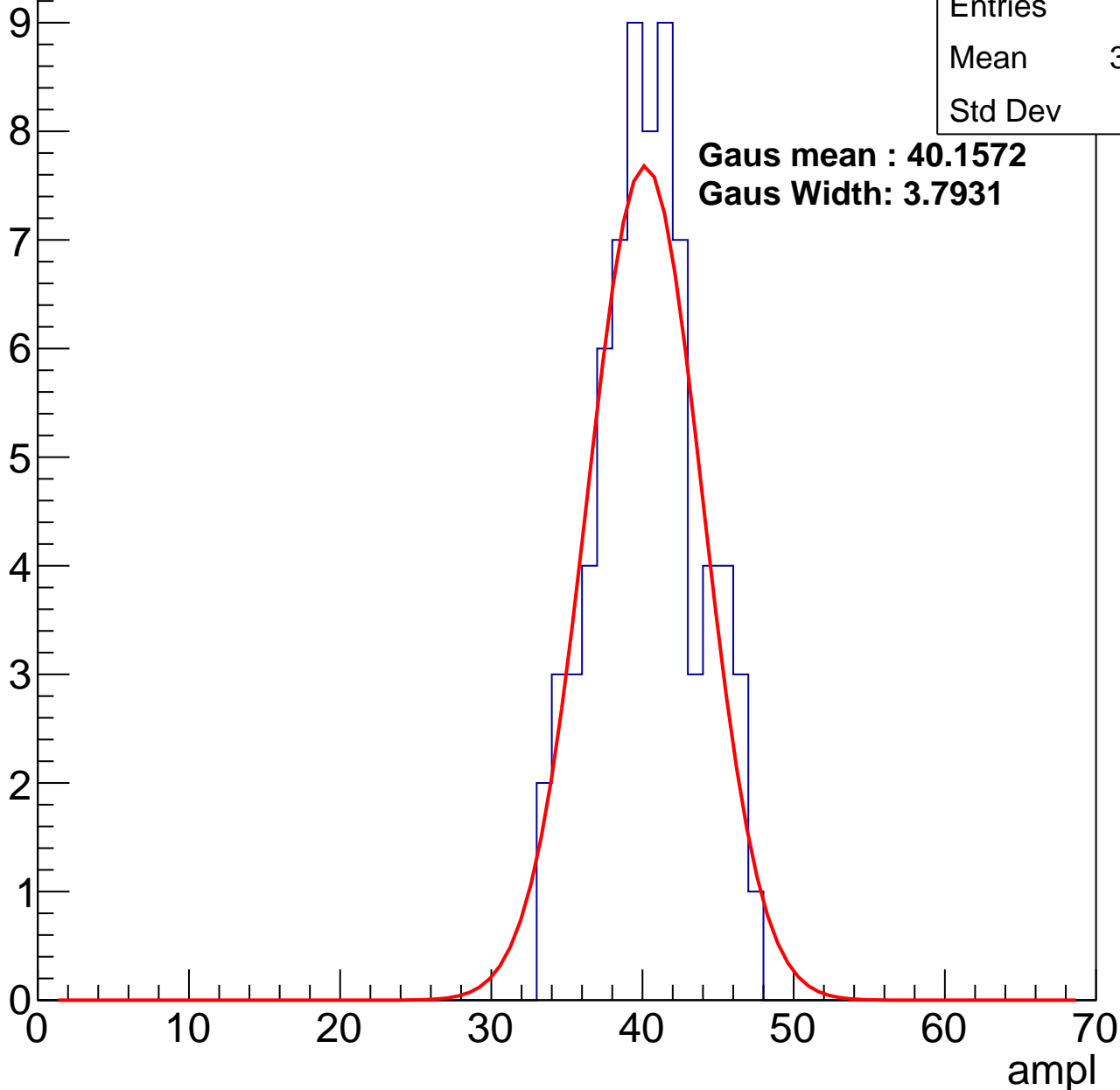
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	73
Mean	39.85
Std Dev	3.35

**Gaus mean : 40.1572**

**Gaus Width: 3.7931**



# B1L101S, U19-ch69, adc2

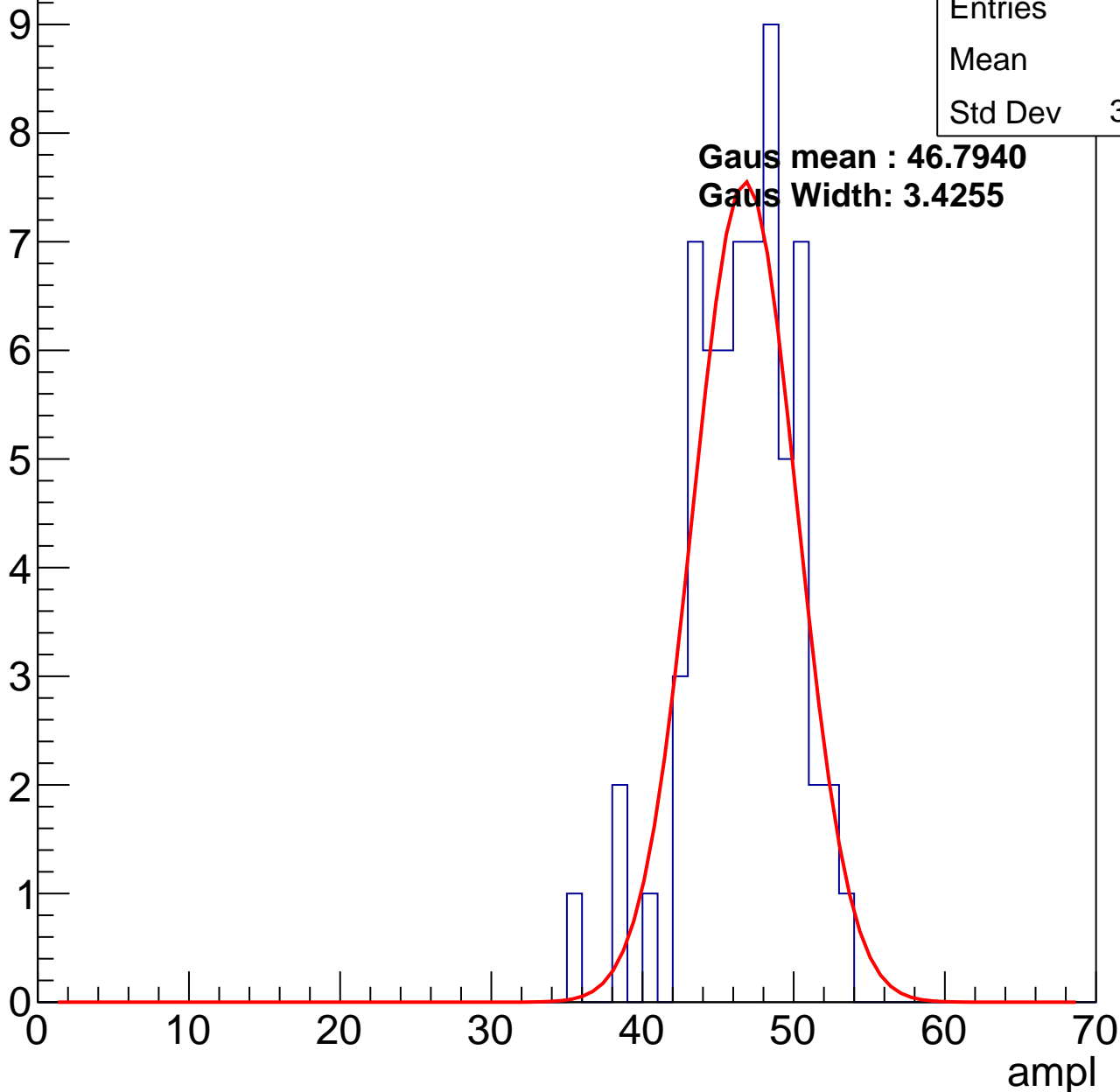
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	66
Mean	46.2
Std Dev	3.469

**Gaus mean : 46.7940**

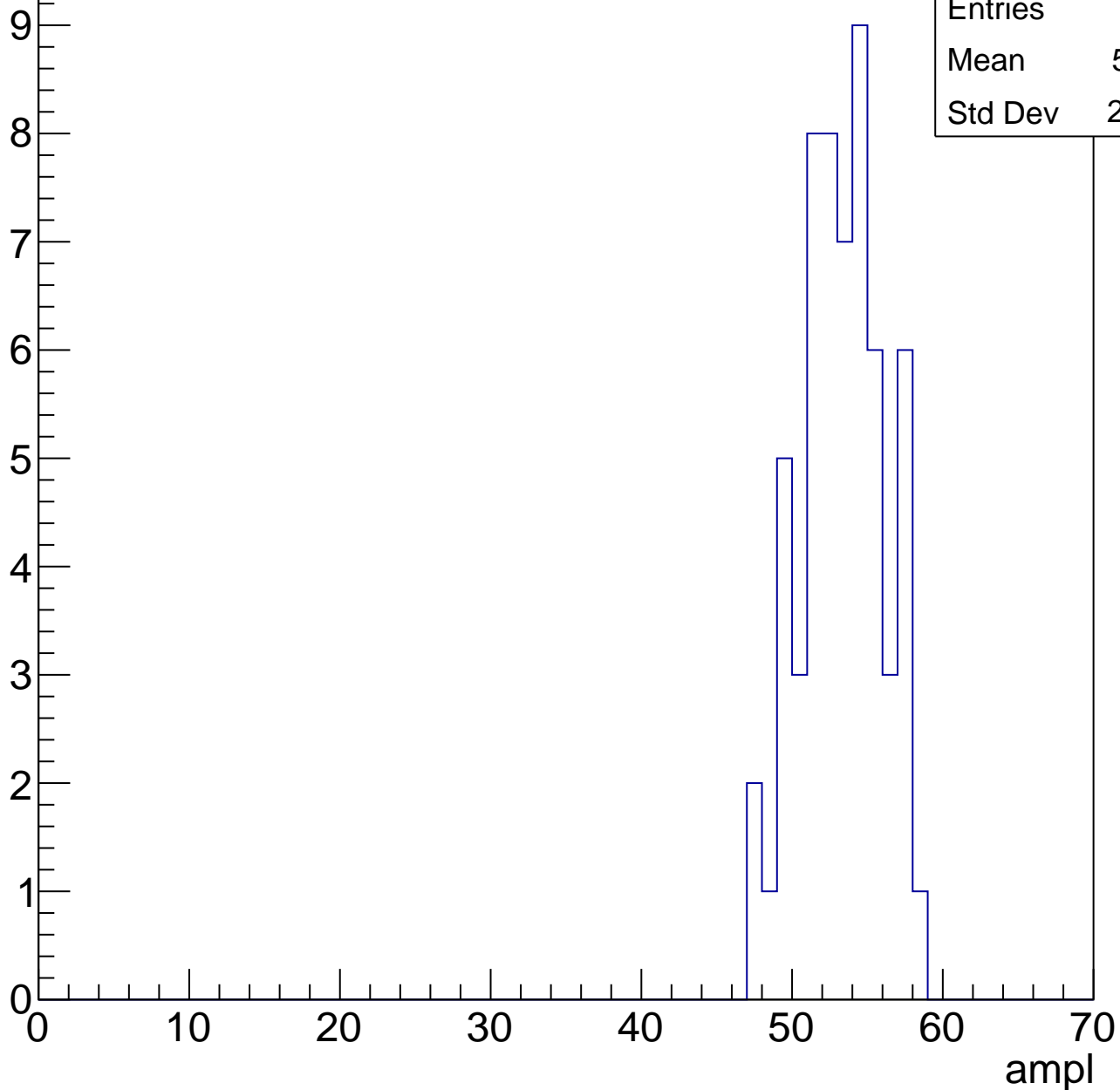
**Gaus Width: 3.4255**



# B1L101S, U19-ch69, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U19-ch69, adc4

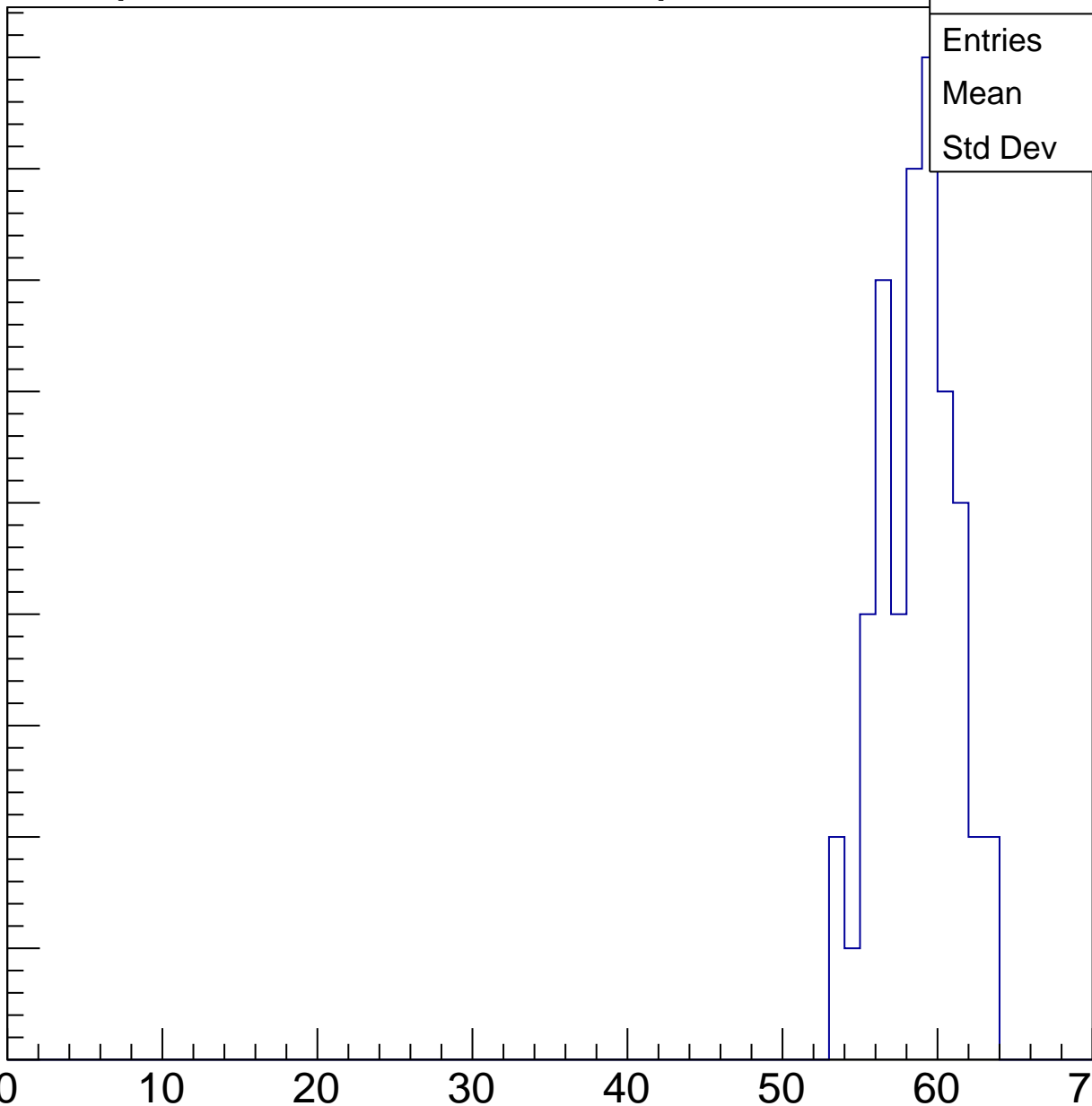
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	50
Mean	58.2
Std Dev	2.417

ampl

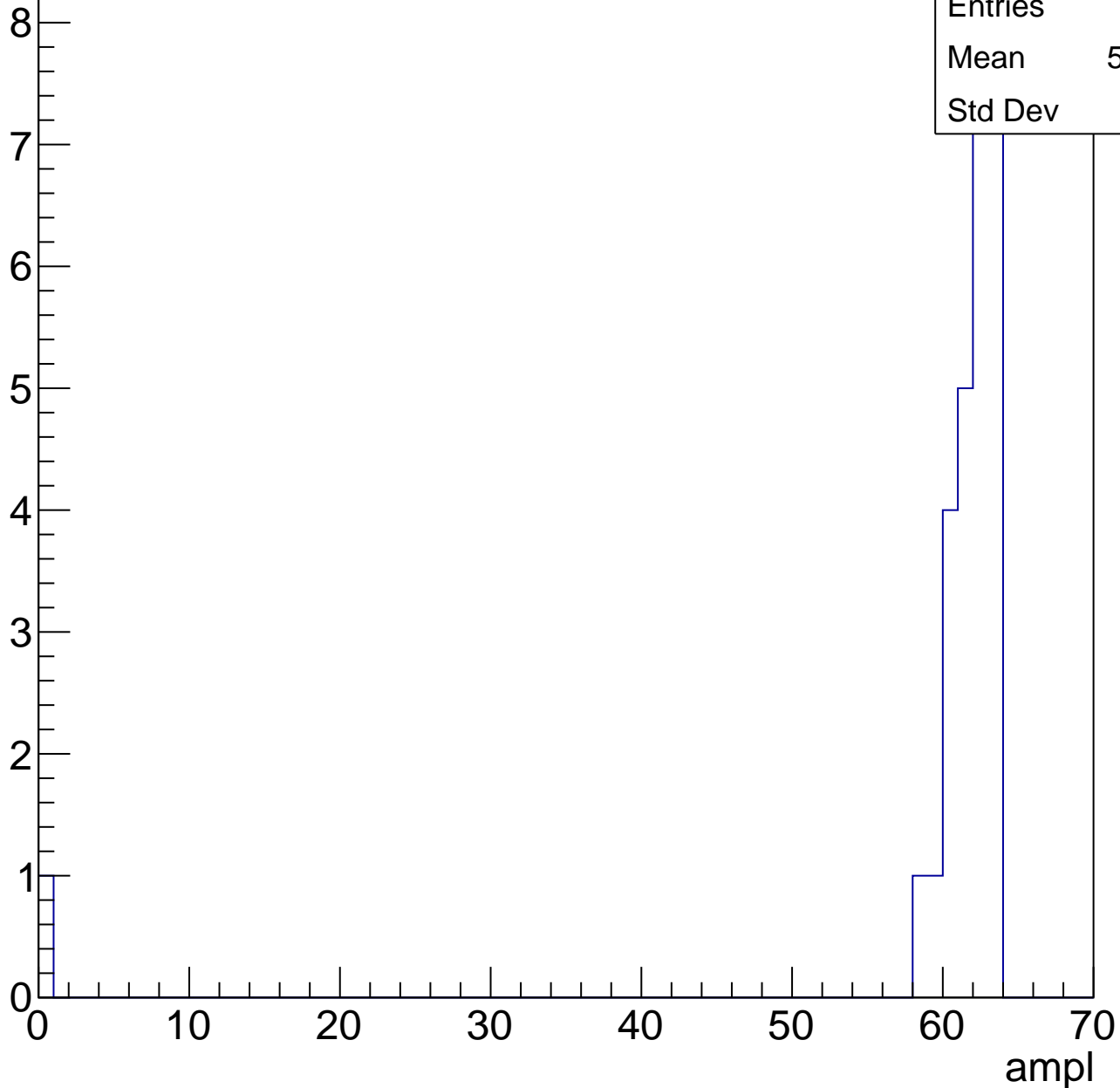


# B1L101S, U19-ch69, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	28
Mean	59.36
Std Dev	11.5



# B1L101S, U19-ch69, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0



# B1L101S, U19-ch69, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U19-ch70, adc0

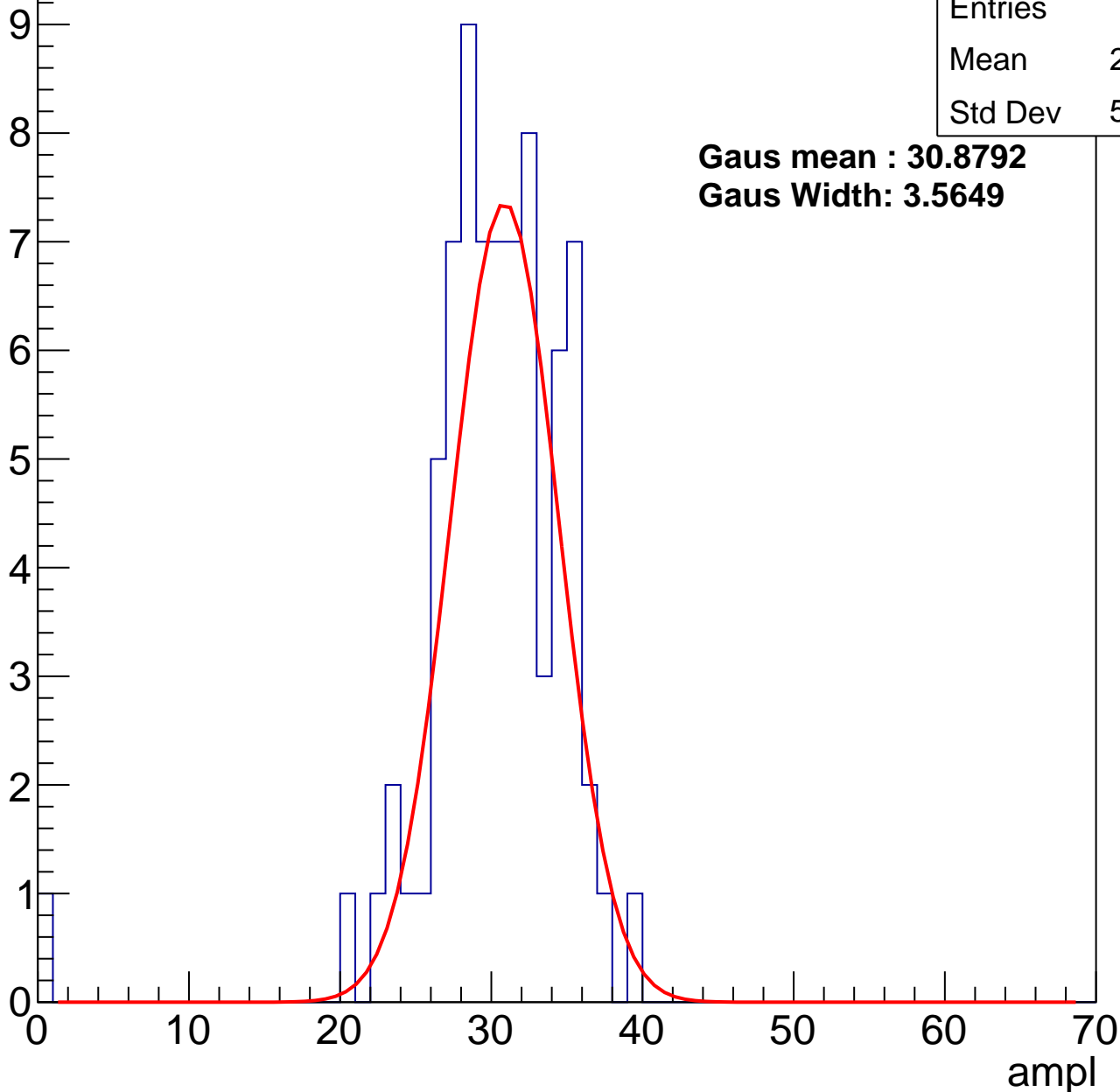
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	77
Mean	29.74
Std Dev	5.023

**Gaus mean : 30.8792**

**Gaus Width: 3.5649**



# B1L101S, U19-ch70, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	70
Mean	36.41
Std Dev	5.579

**Gaus mean : 37.4186**

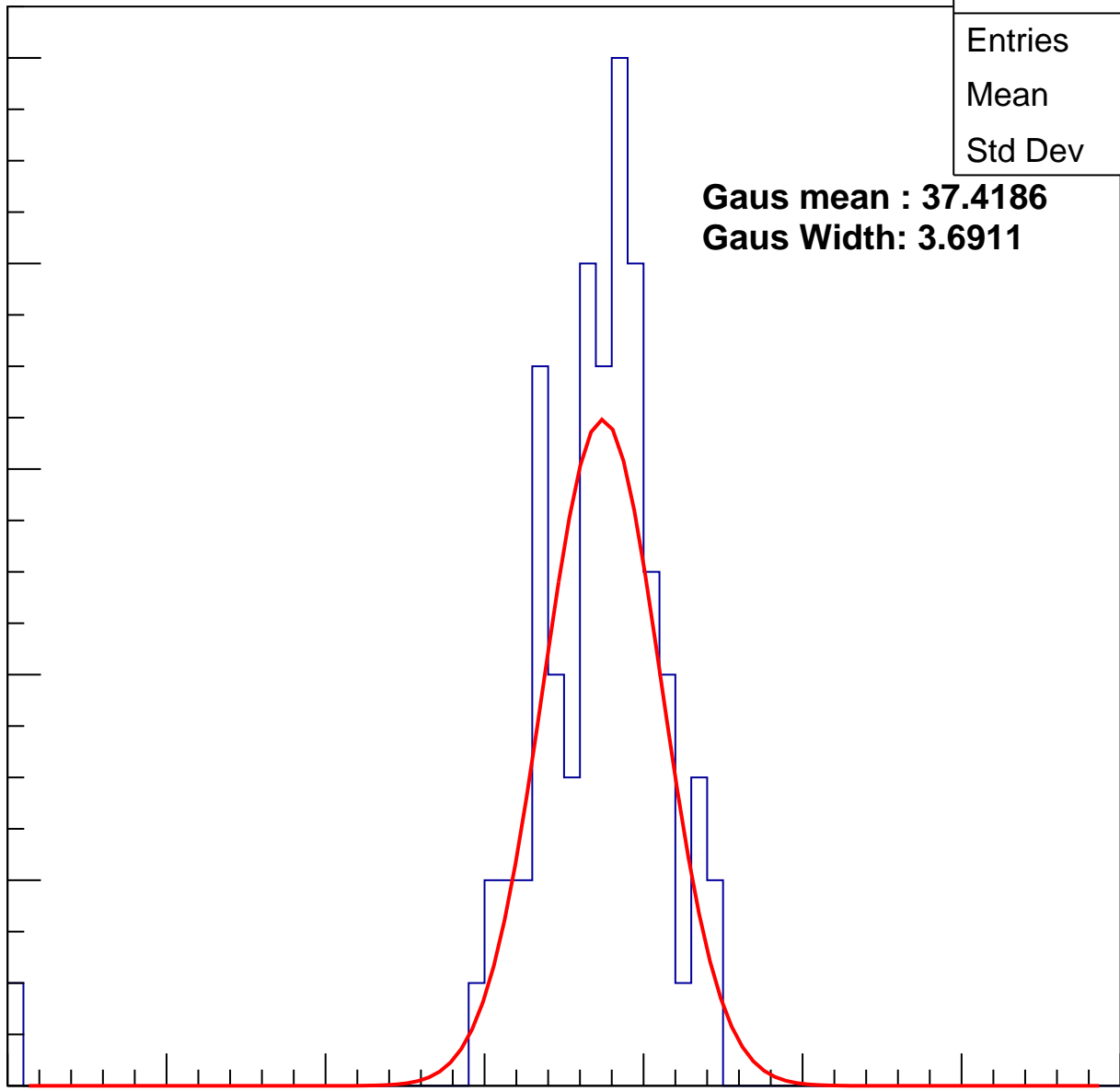
**Gaus Width: 3.6911**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U19-ch70, adc2

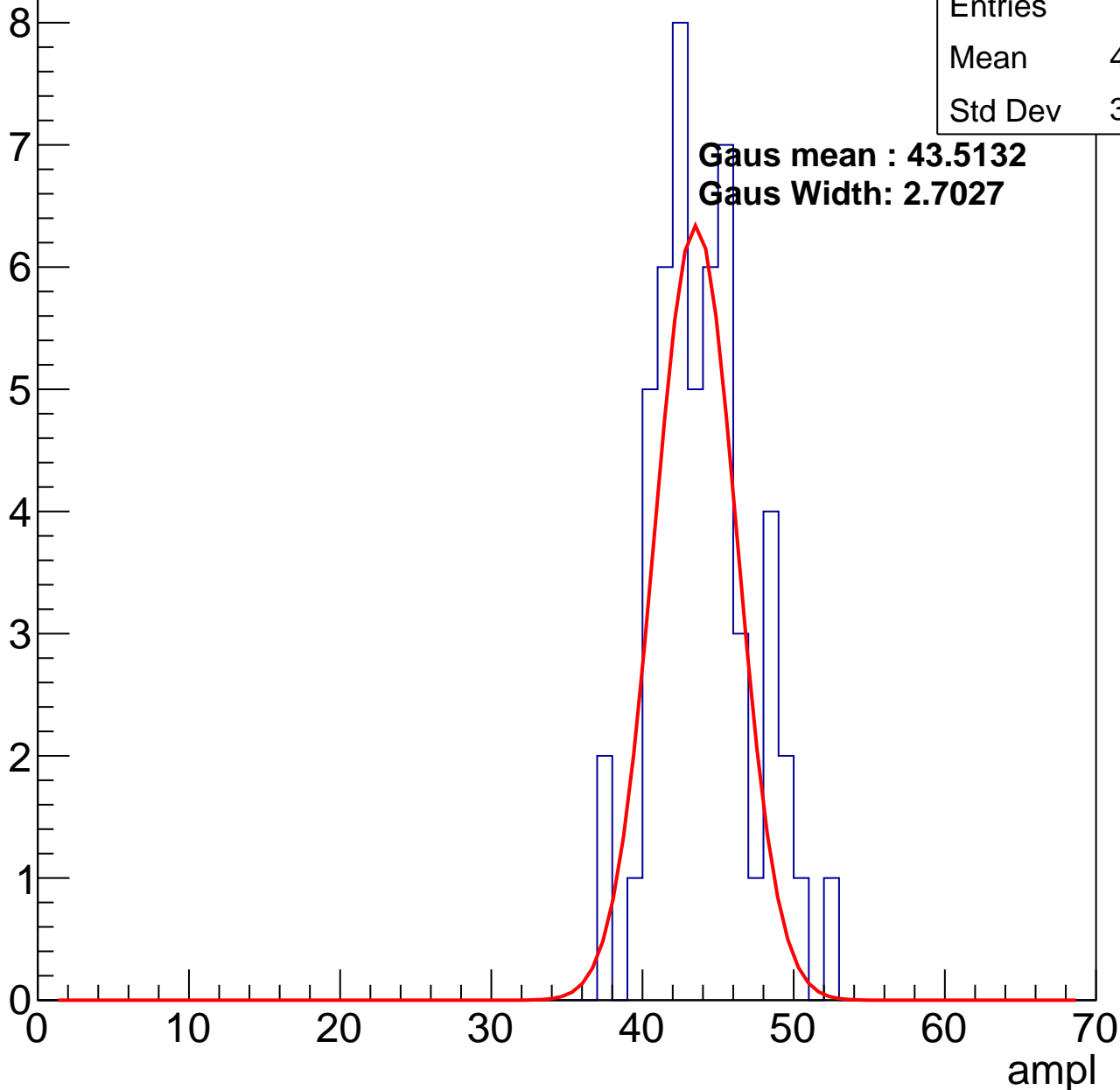
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	52
Mean	43.58
Std Dev	3.183

**Gaus mean : 43.5132**

**Gaus Width: 2.7027**

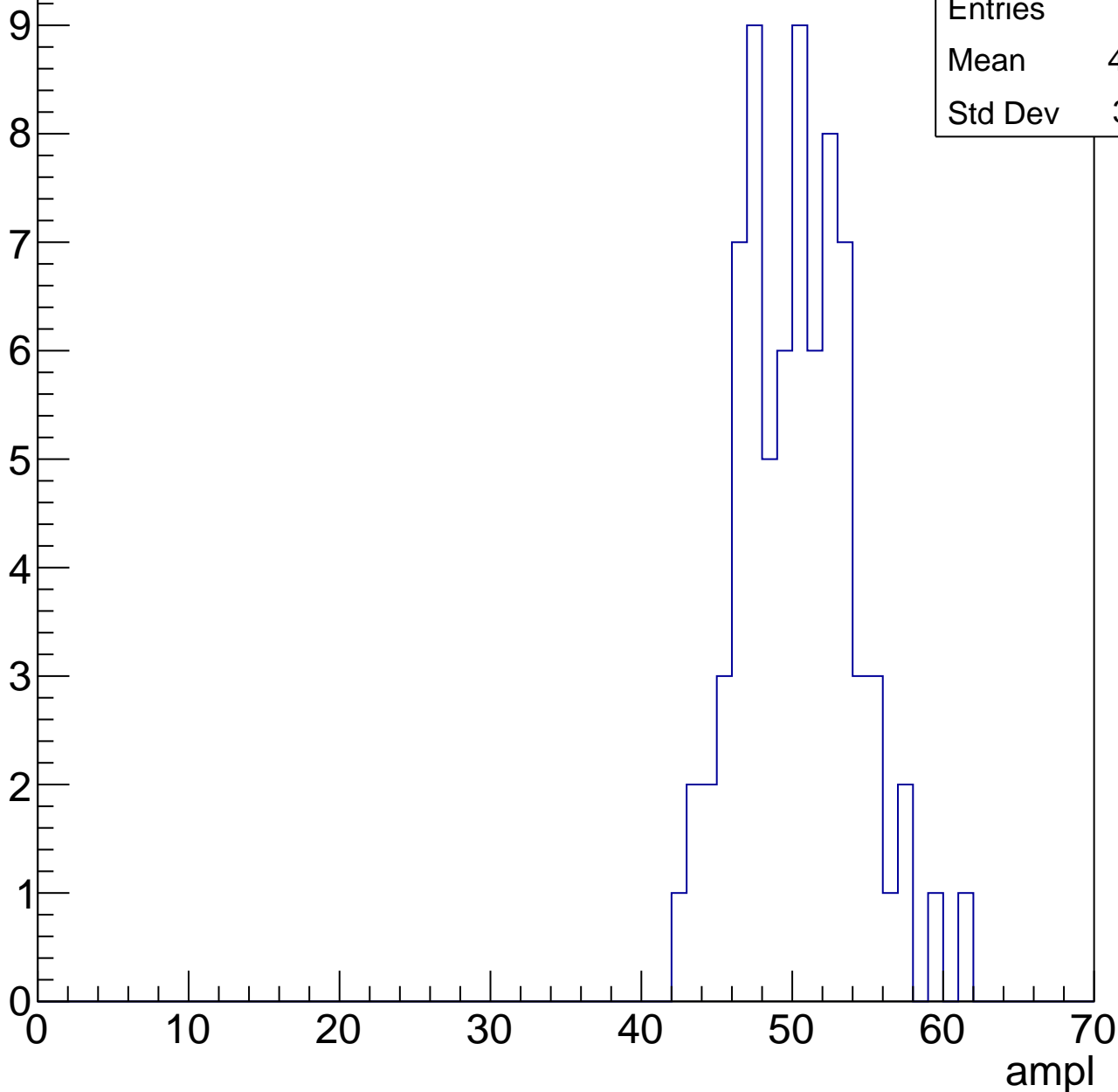


# B1L101S, U19-ch70, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	76
Mean	49.87
Std Dev	3.781

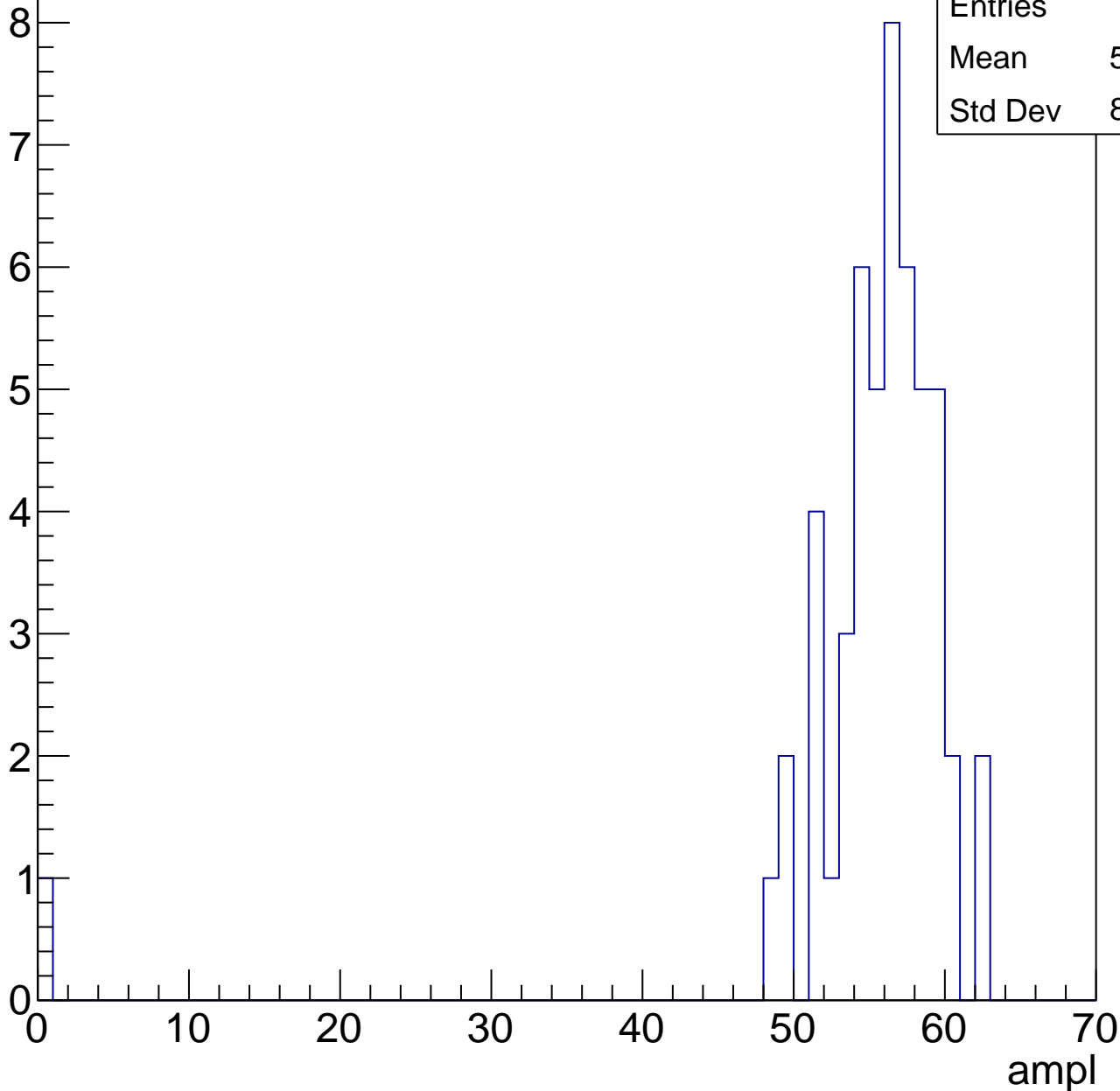


# B1L101S, U19-ch70, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	51
Mean	54.49
Std Dev	8.318



# B1L101S, U19-ch70, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

10

8

6

4

2

0

0

10

20

30

40

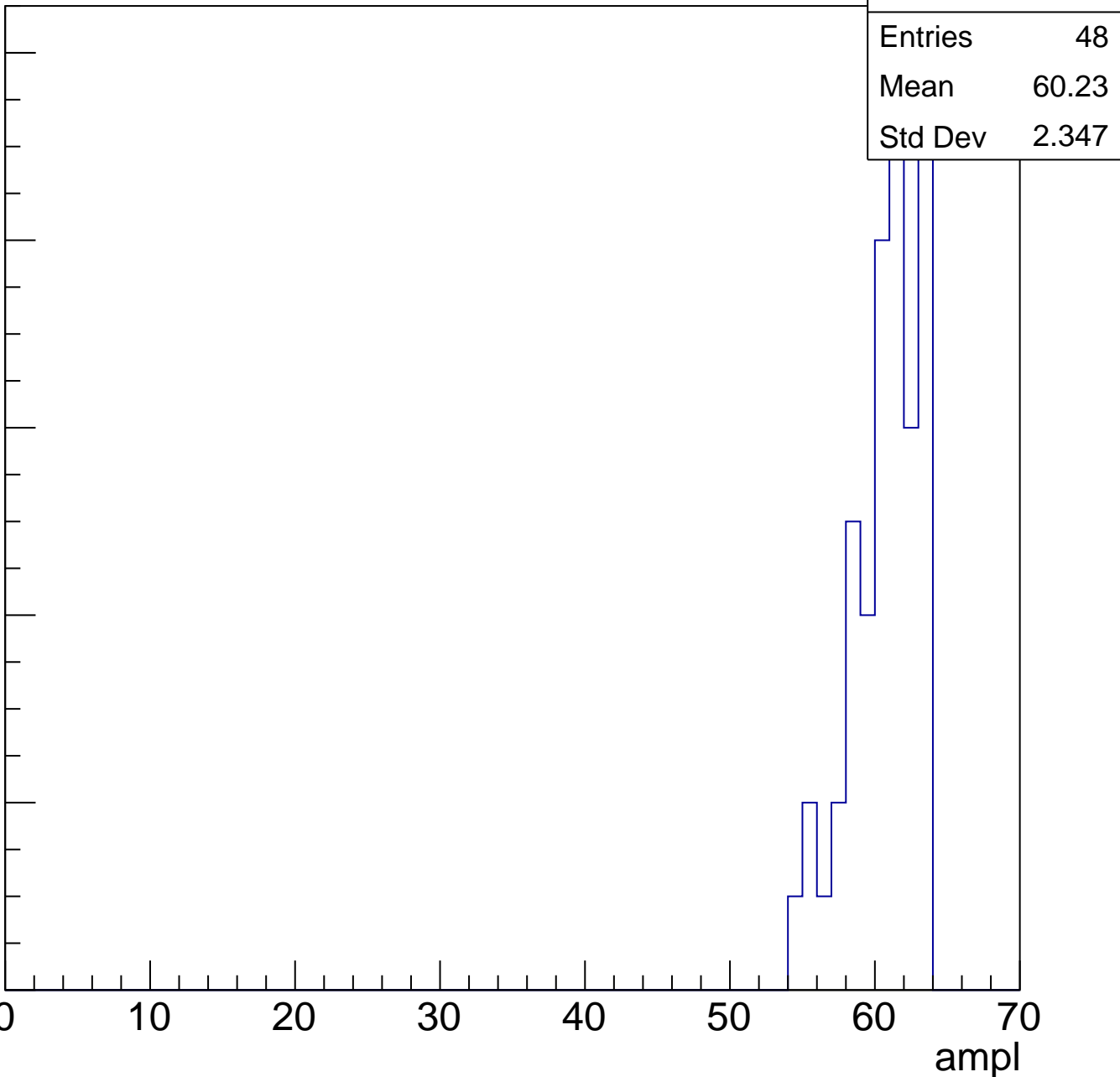
50

60

70

ampl

Entries	48
Mean	60.23
Std Dev	2.347



# B1L101S, U19-ch70, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U19-ch70, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U19-ch71, adc0

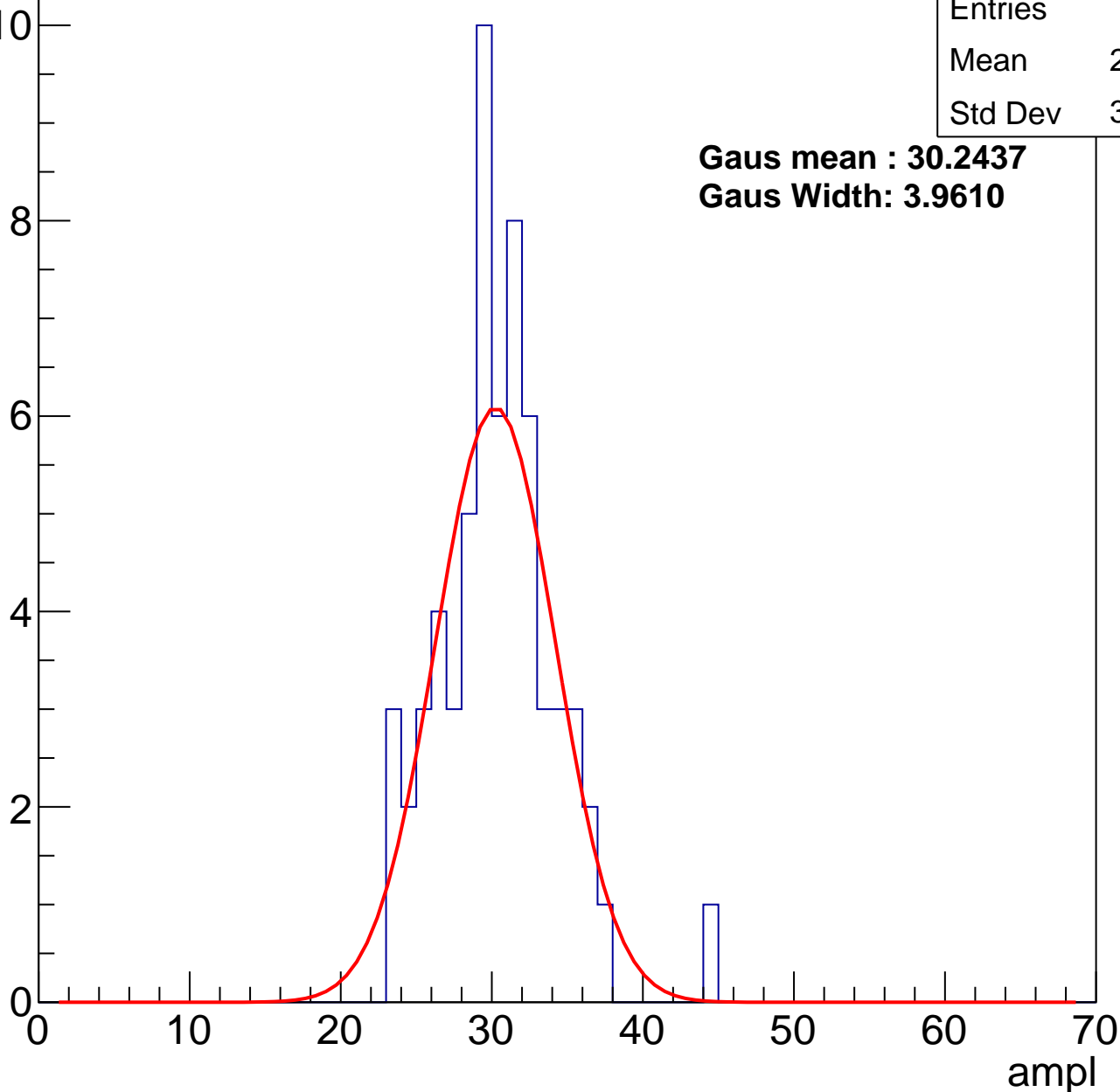
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	29.94
Std Dev	3.808

**Gaus mean : 30.2437**

**Gaus Width: 3.9610**



# B1L101S, U19-ch71, adc1

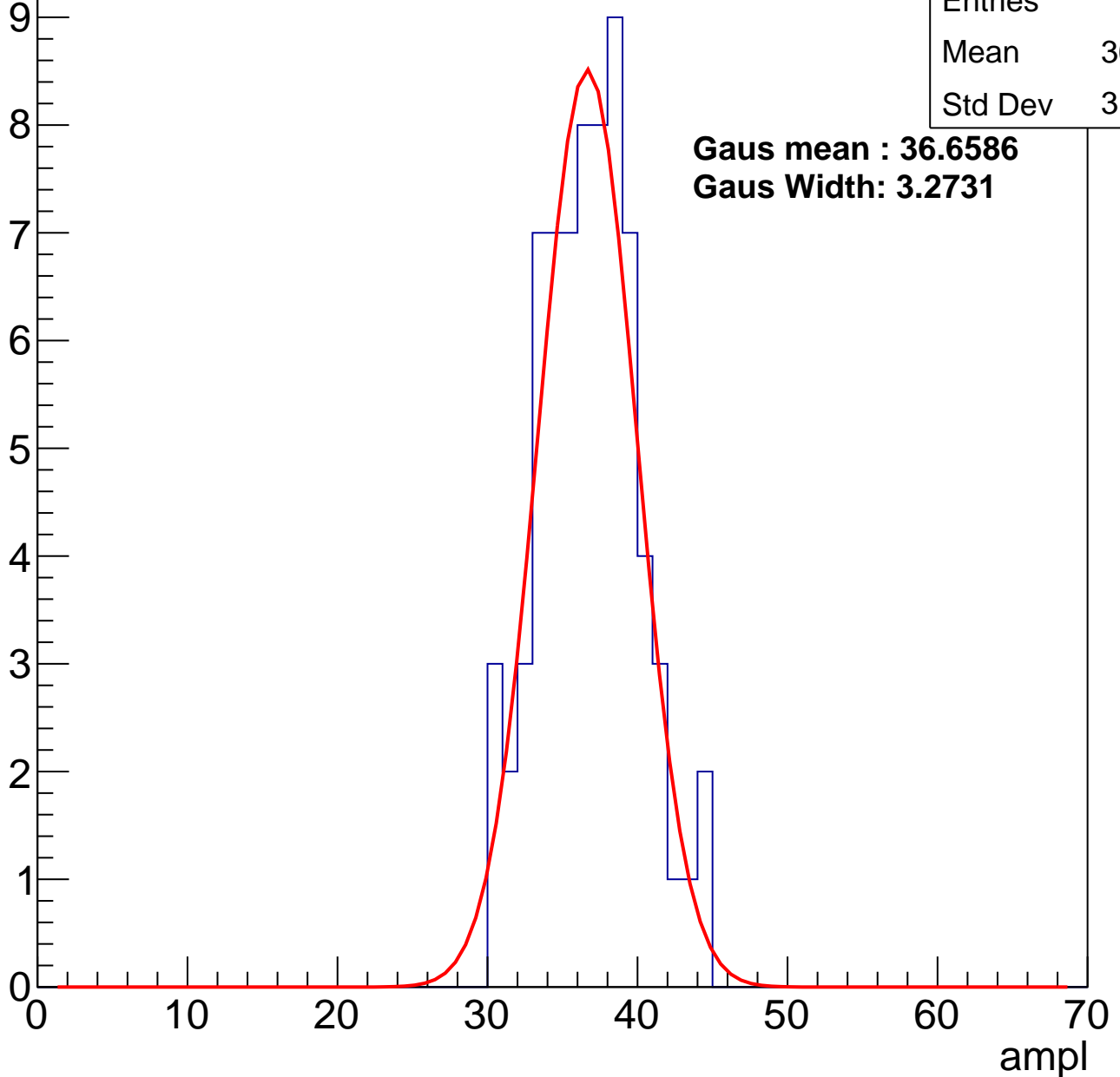
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	72
Mean	36.35
Std Dev	3.237

**Gaus mean : 36.6586**

**Gaus Width: 3.2731**



# B1L101S, U19-ch71, adc2

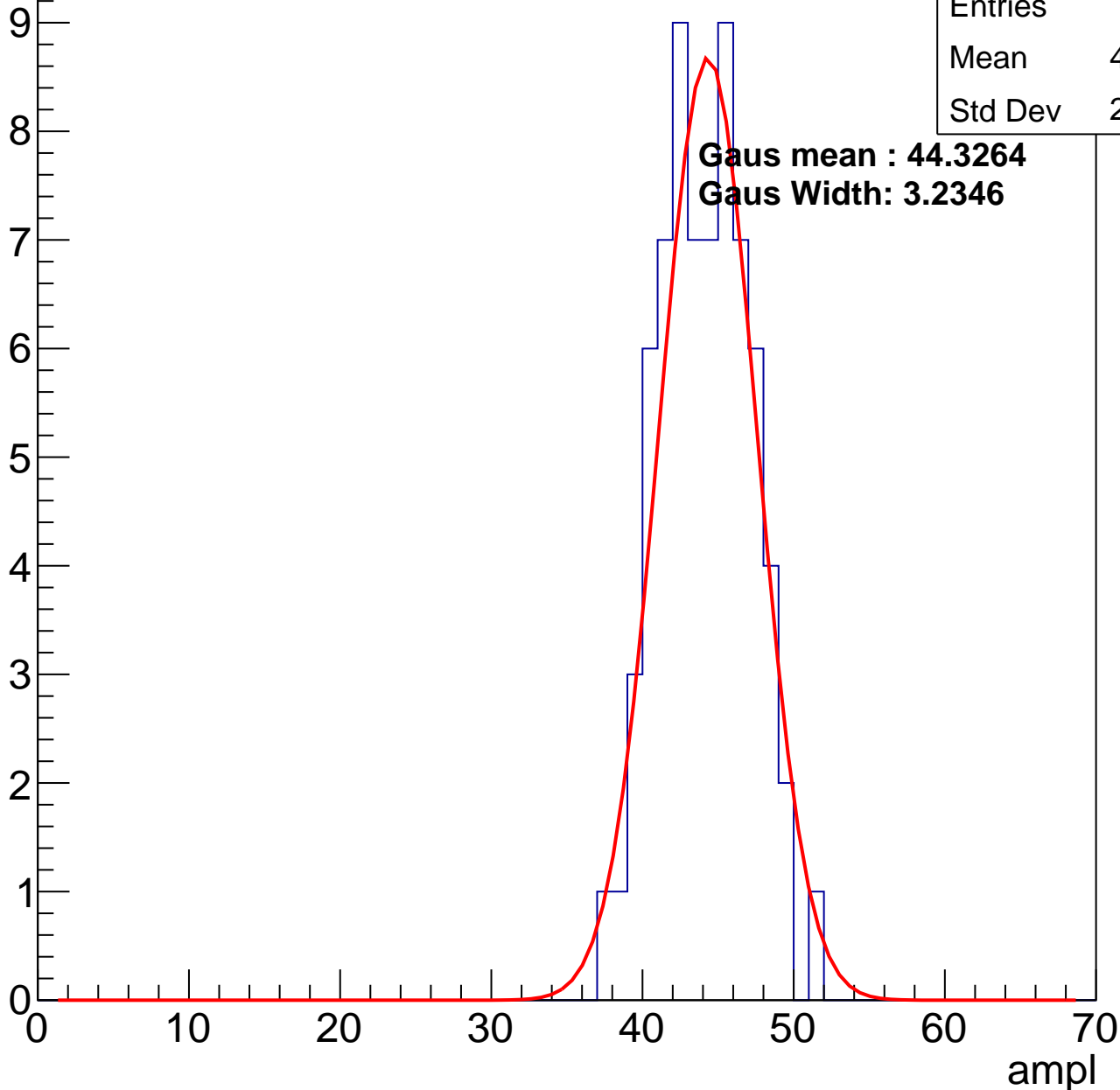
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	43.66
Std Dev	2.947

**Gaus mean : 44.3264**

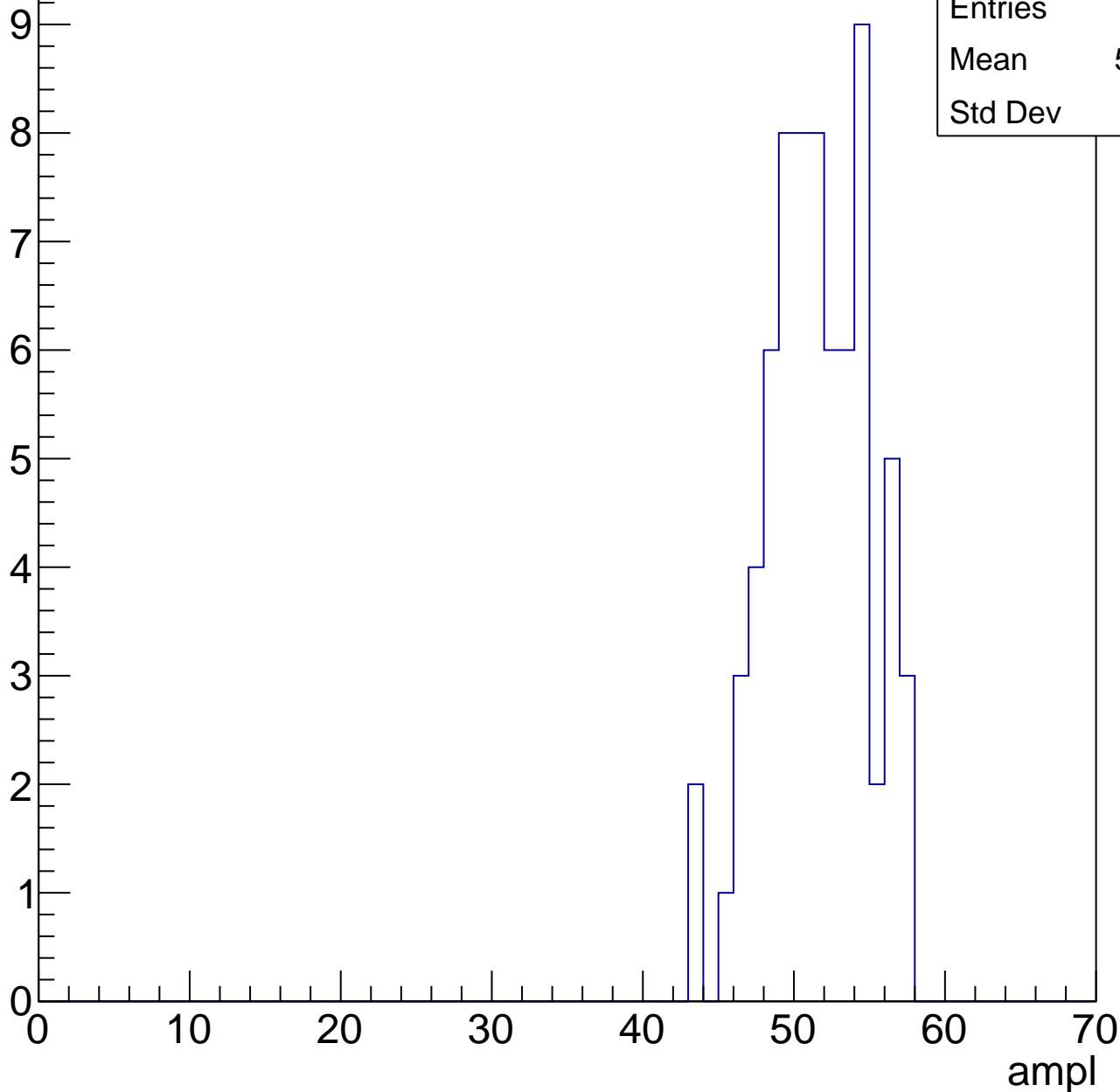
**Gaus Width: 3.2346**



# B1L101S, U19-ch71, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

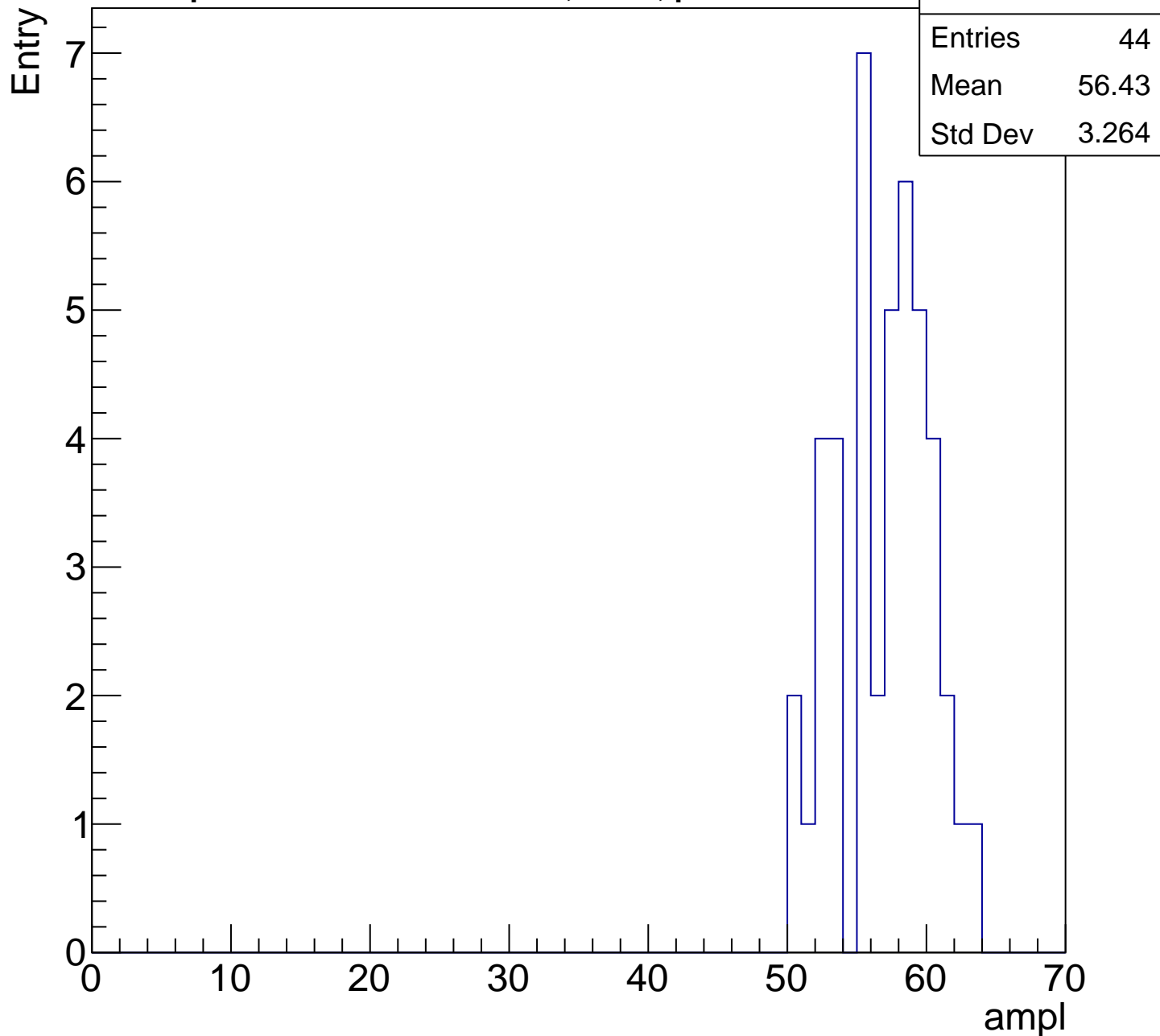
Entry



Entries	71
Mean	51.01
Std Dev	3.3

# B1L101S, U19-ch71, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

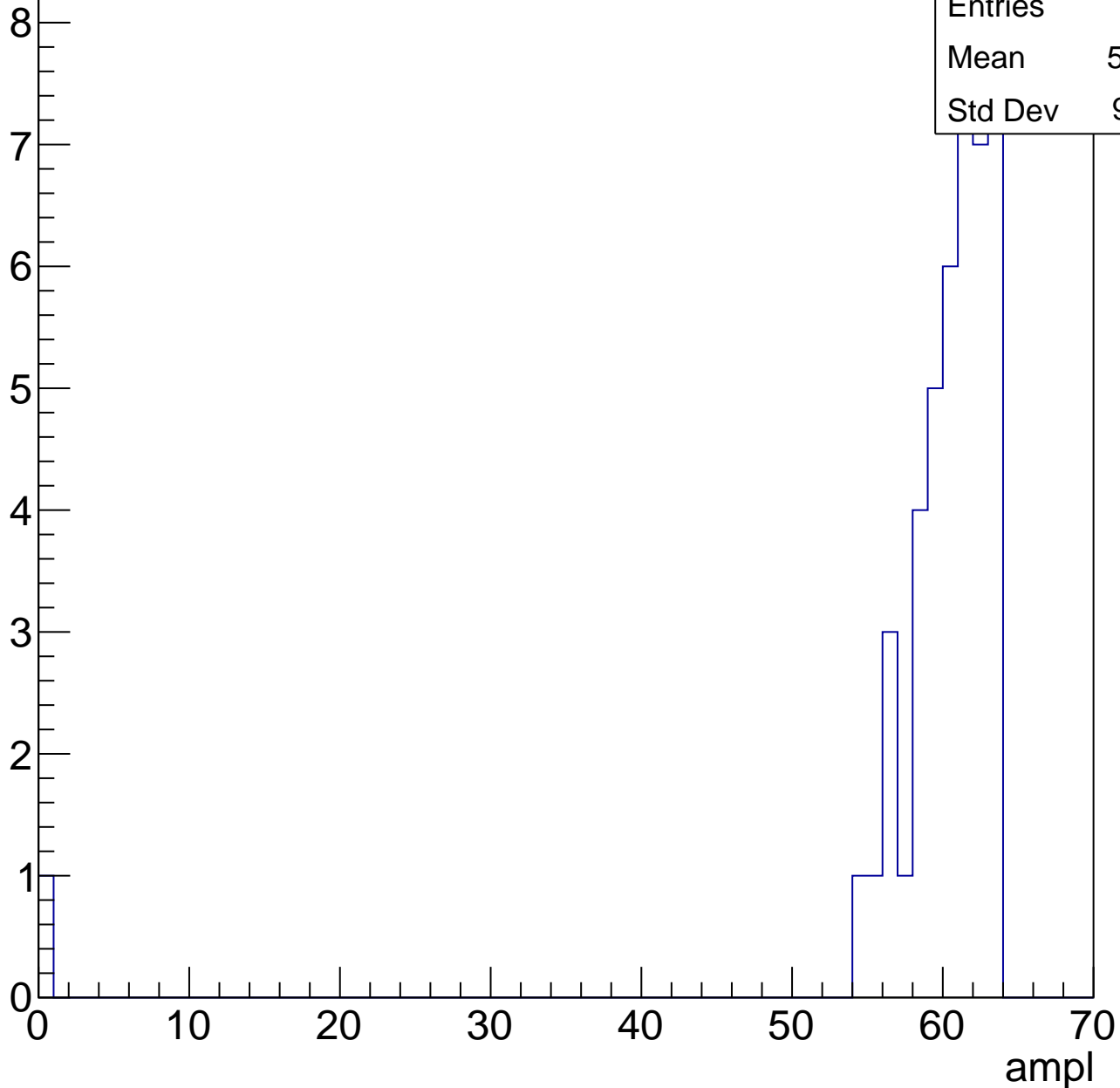


# B1L101S, U19-ch71, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

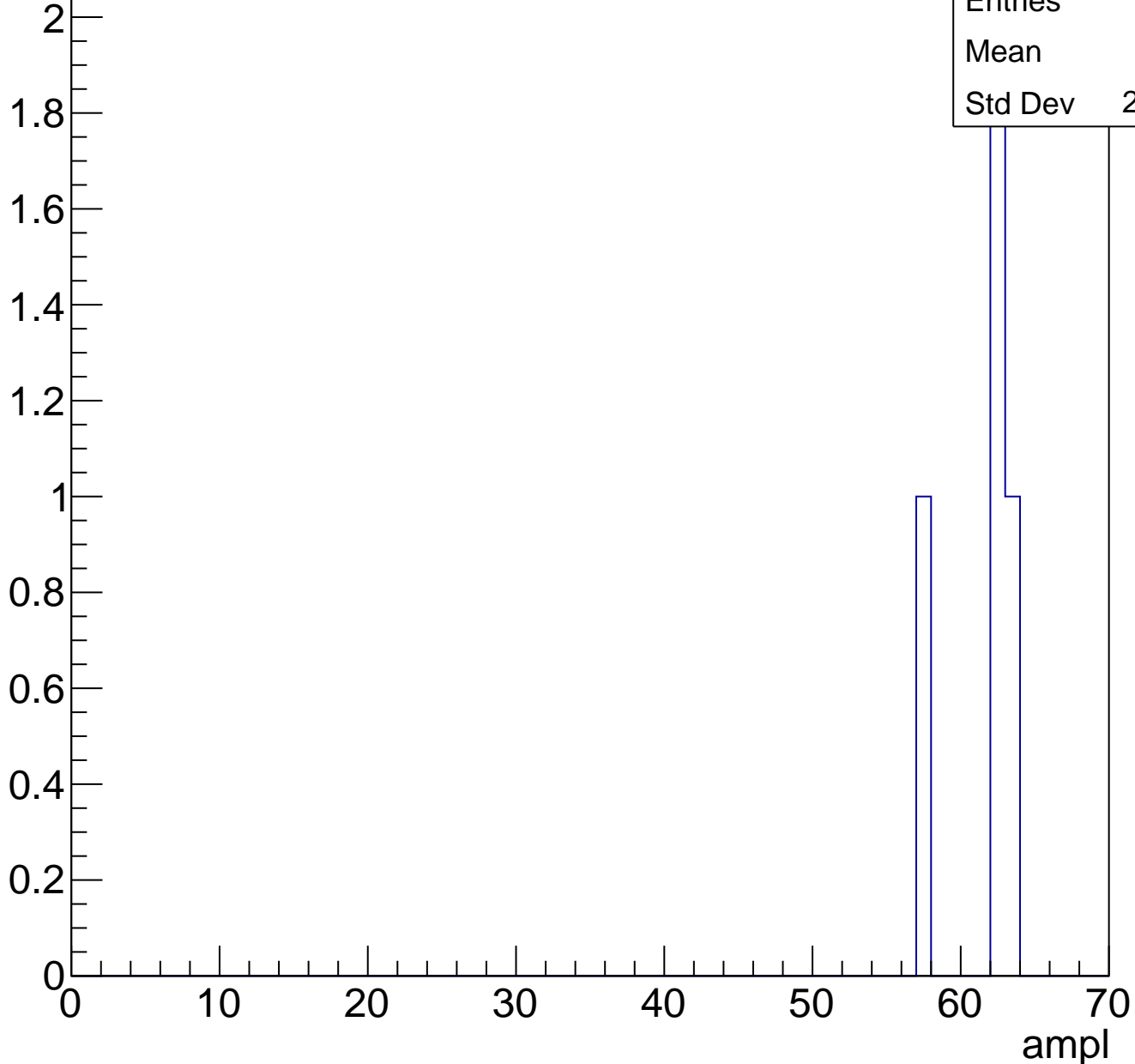
Entries	45
Mean	58.82
Std Dev	9.171



# B1L101S, U19-ch71, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

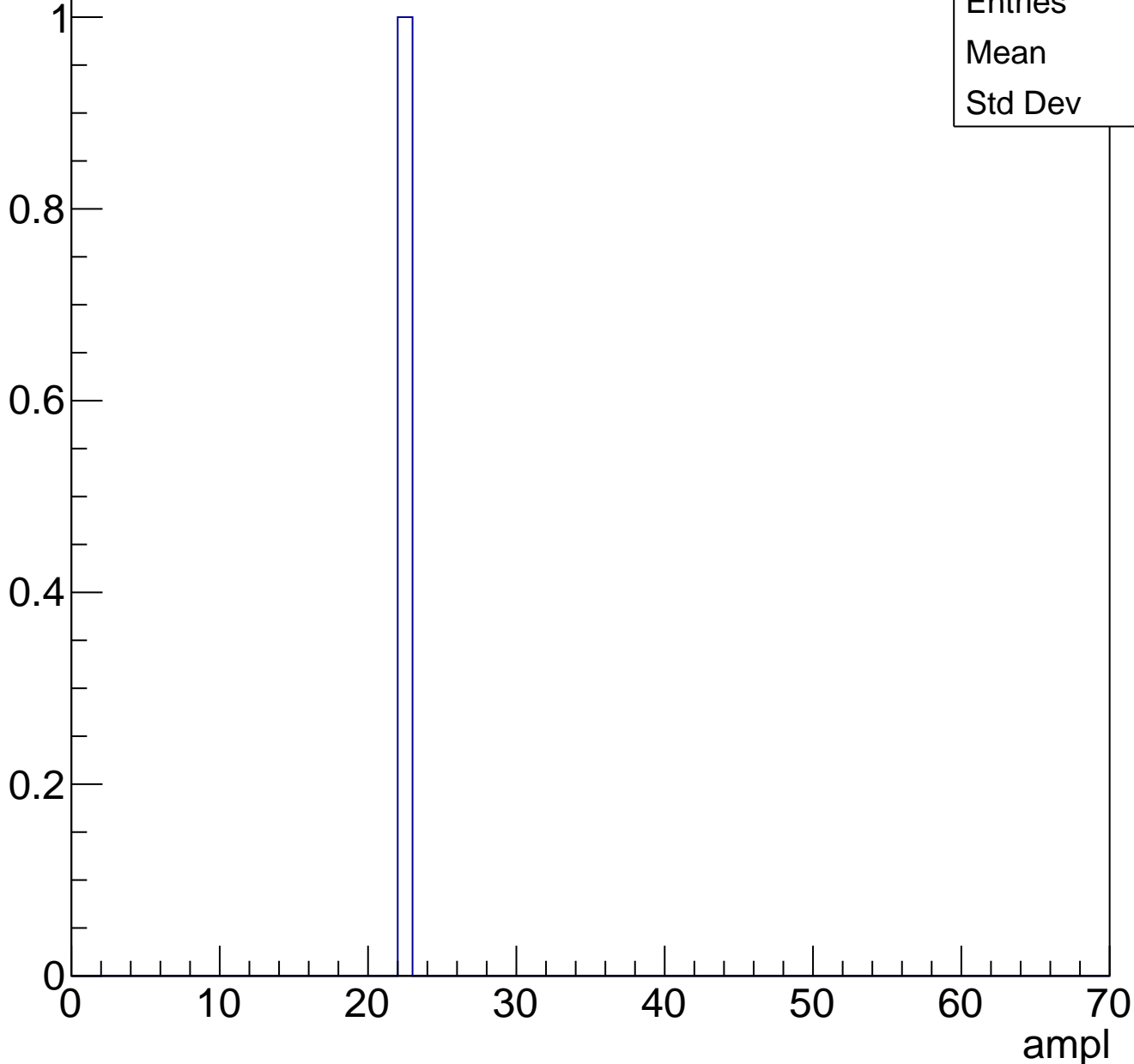




# B1L101S, U19-ch71, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U19-ch72, adc0

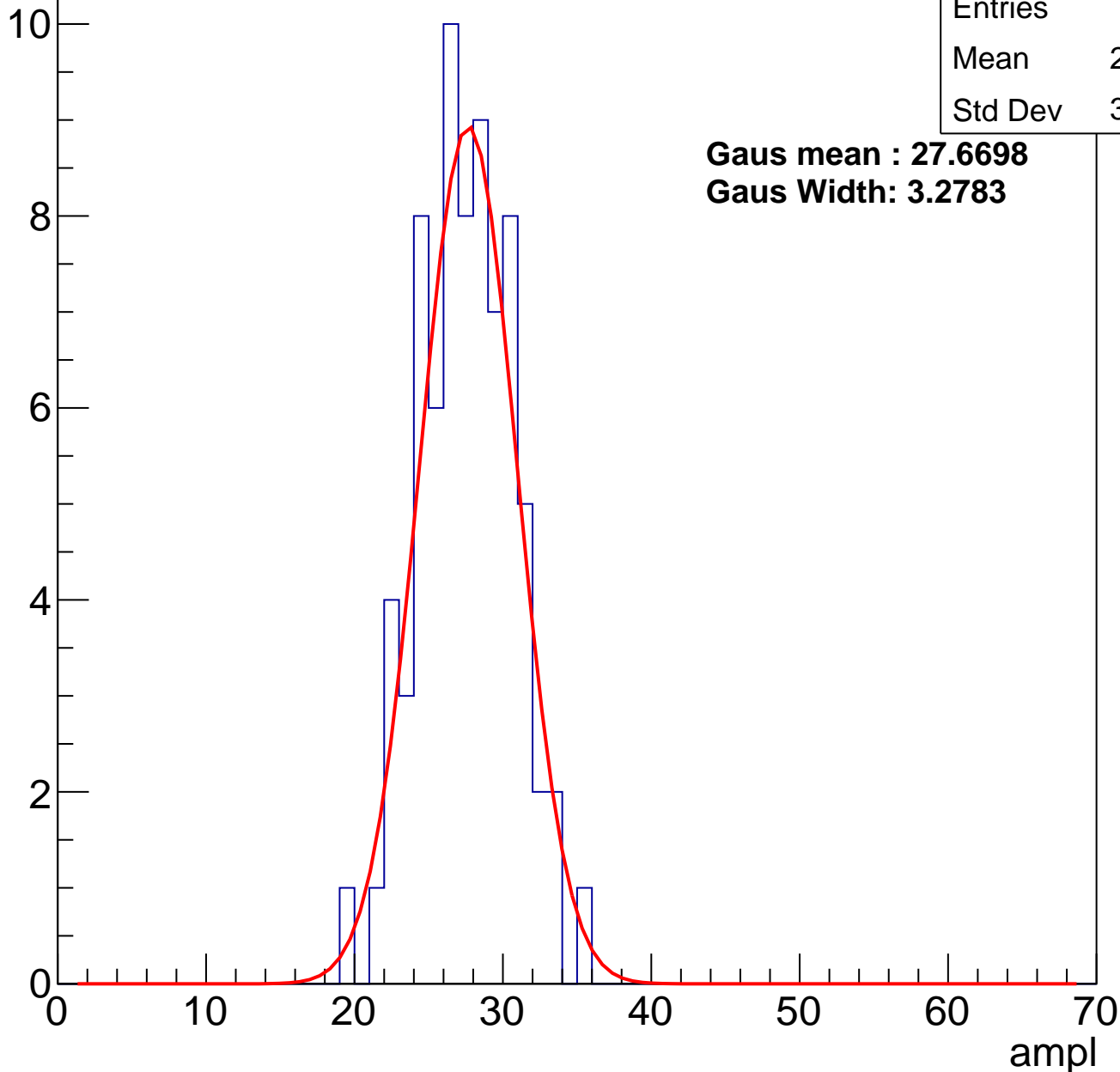
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	75
Mean	27.07
Std Dev	3.117

**Gaus mean : 27.6698**

**Gaus Width: 3.2783**

Entry



# B1L101S, U19-ch72, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	72
Mean	34.82
Std Dev	3.289

**Gaus mean : 35.1406**

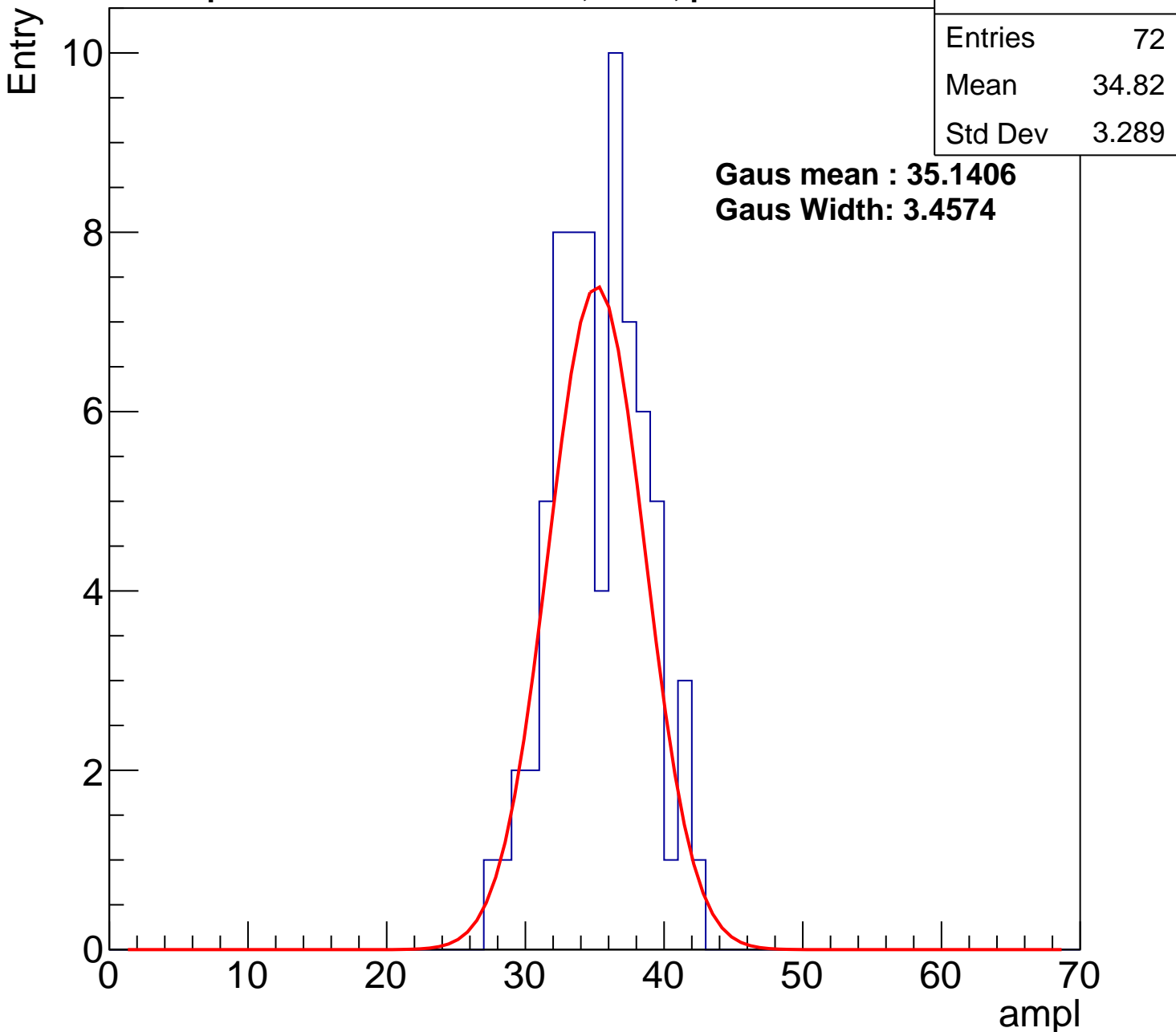
**Gaus Width: 3.4574**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U19-ch72, adc2

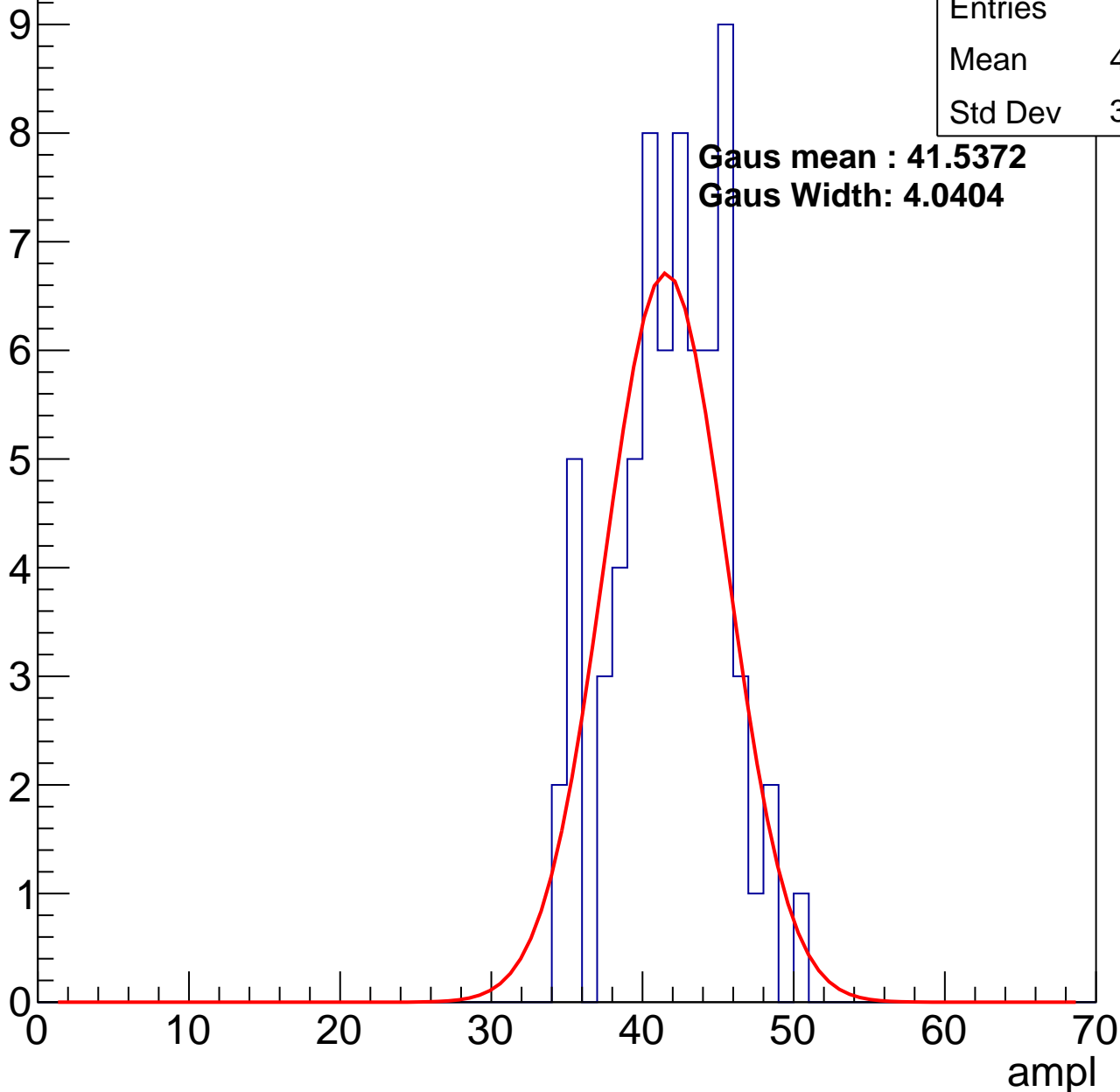
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	41.46
Std Dev	3.602

**Gaus mean : 41.5372**

**Gaus Width: 4.0404**

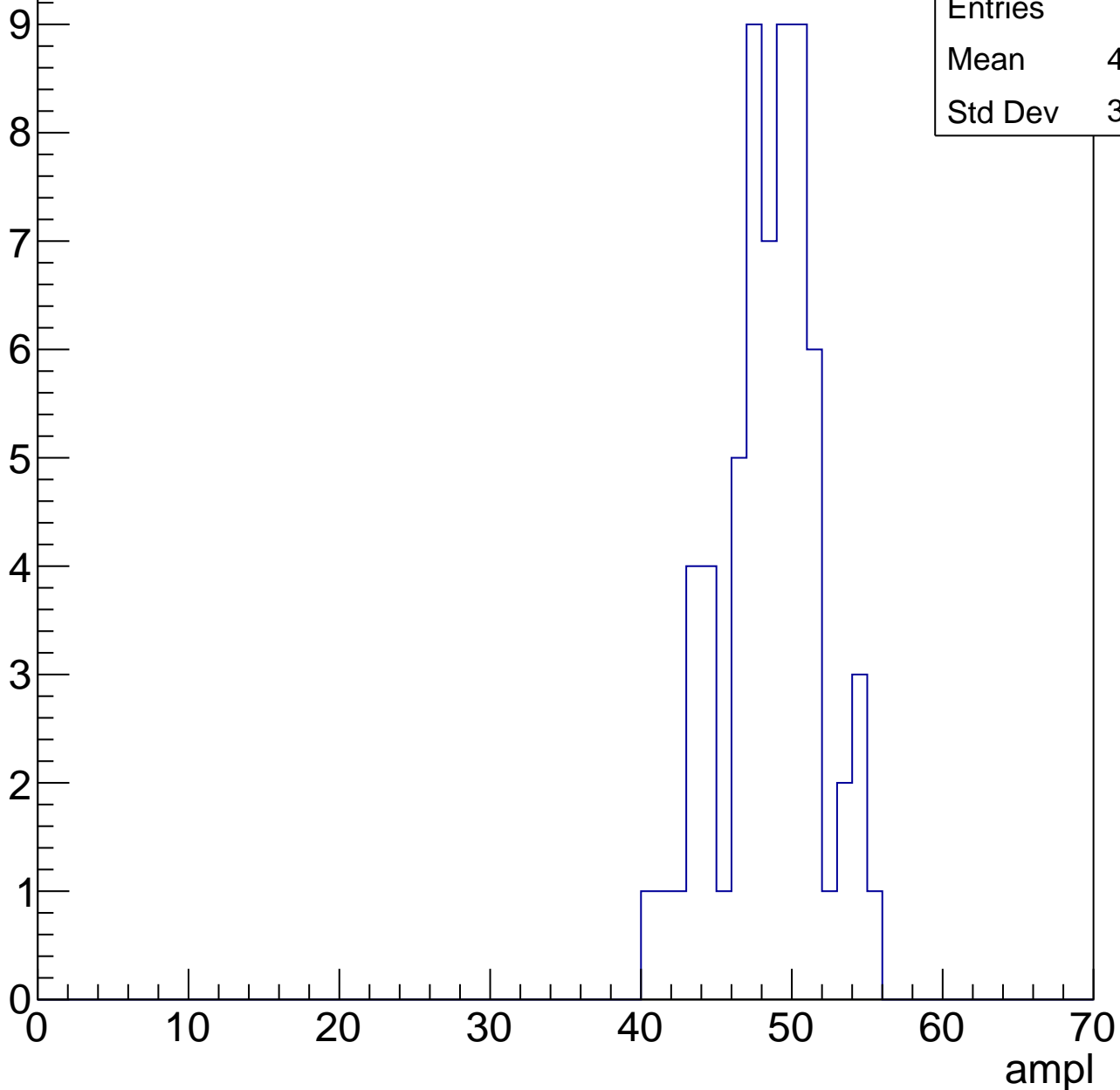


# B1L101S, U19-ch72, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	48.08
Std Dev	3.242

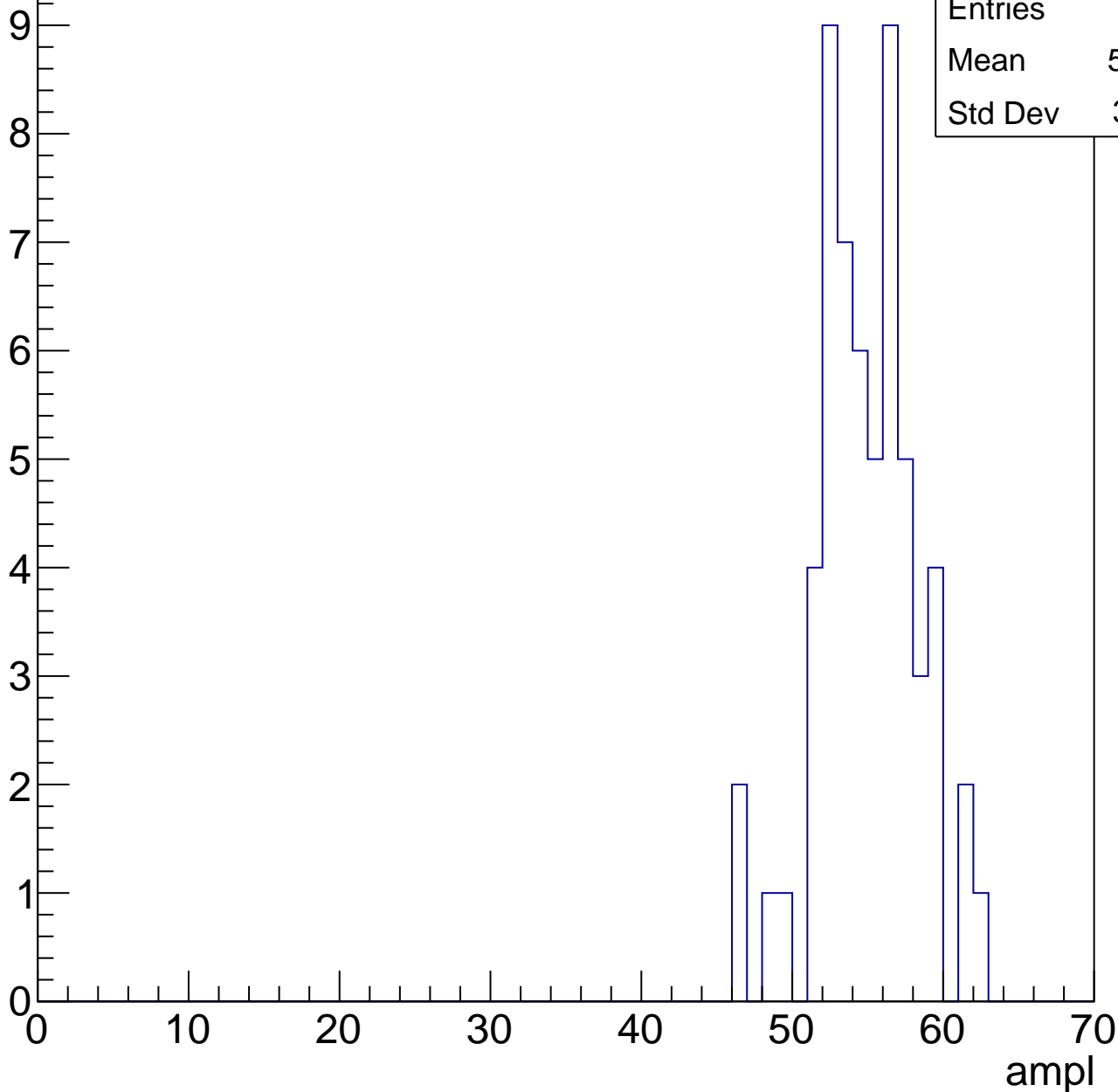


# B1L101S, U19-ch72, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

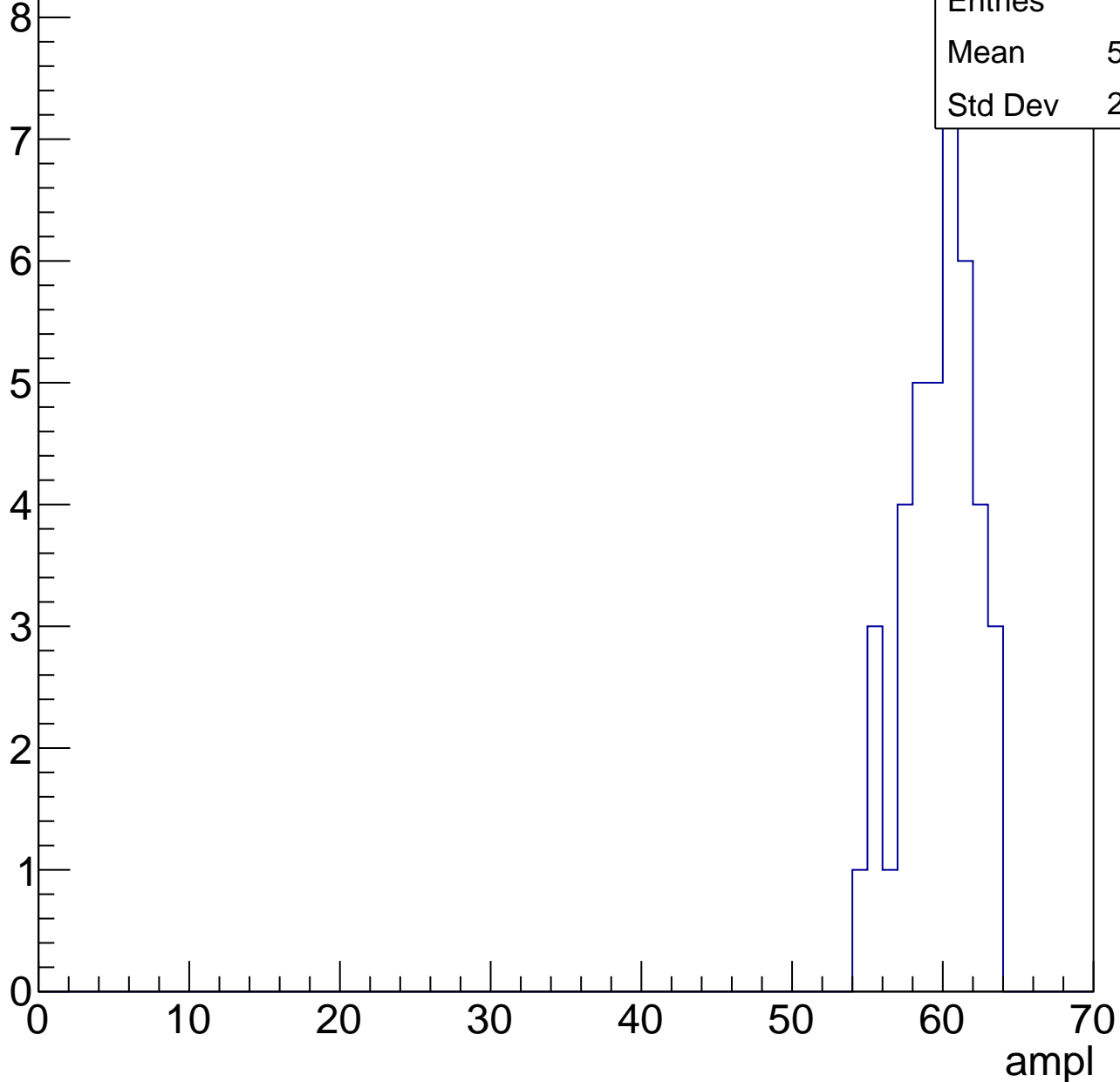
Entries	59
Mean	54.47
Std Dev	3.321



# B1L101S, U19-ch72, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

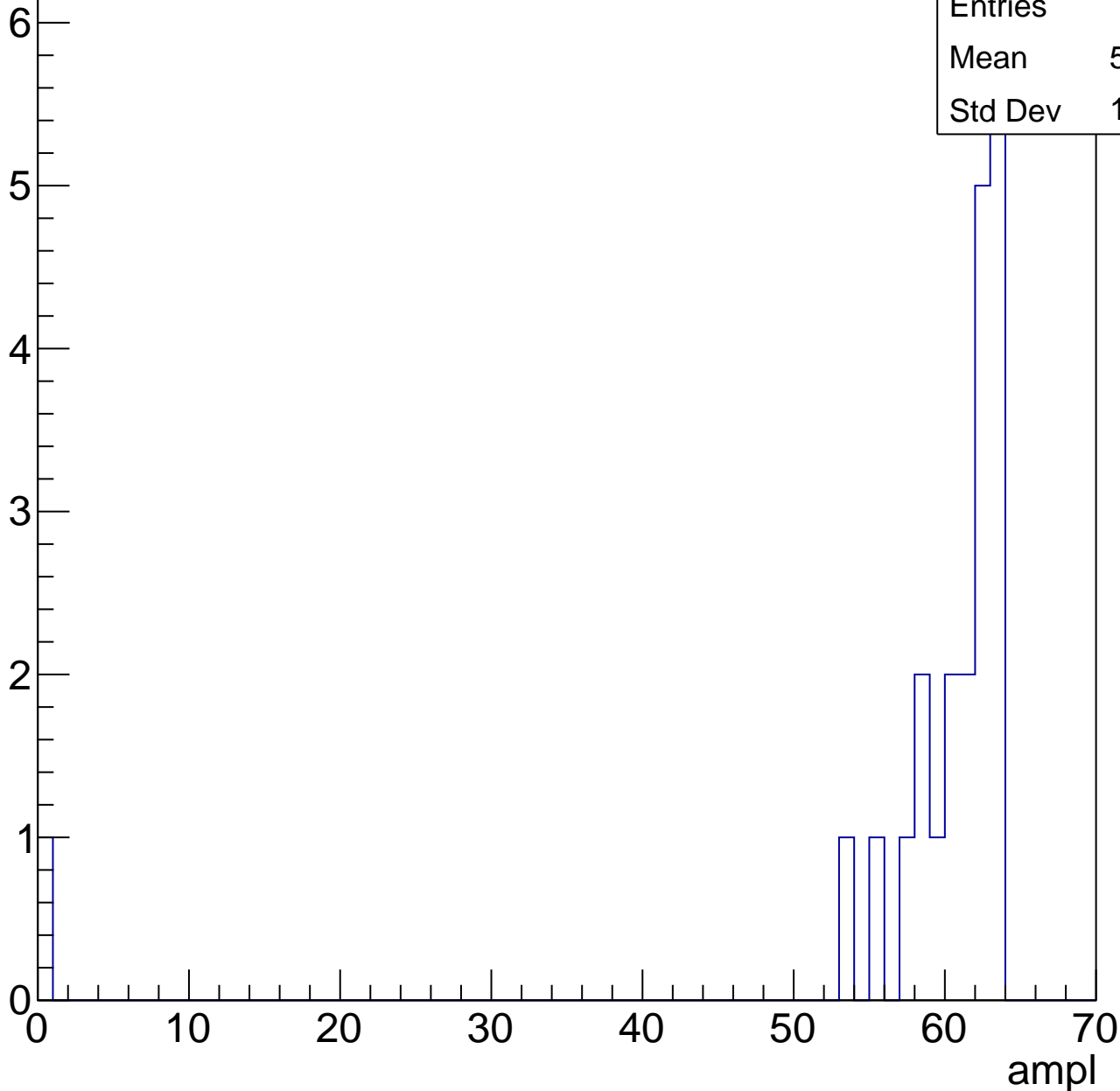


# B1L101S, U19-ch72, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	22
Mean	57.73
Std Dev	12.89

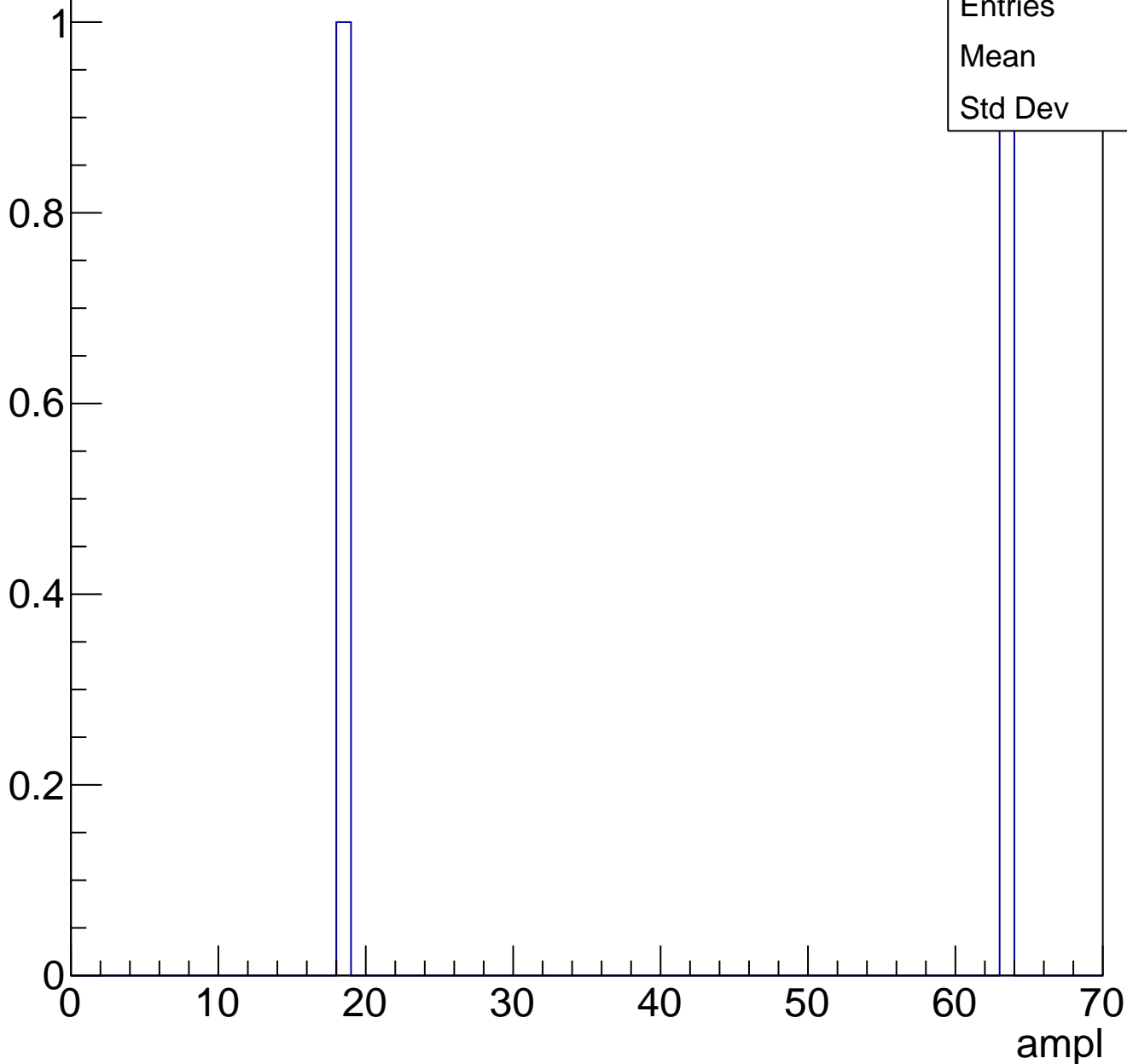




# B1L101S, U19-ch72, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U19-ch73, adc0

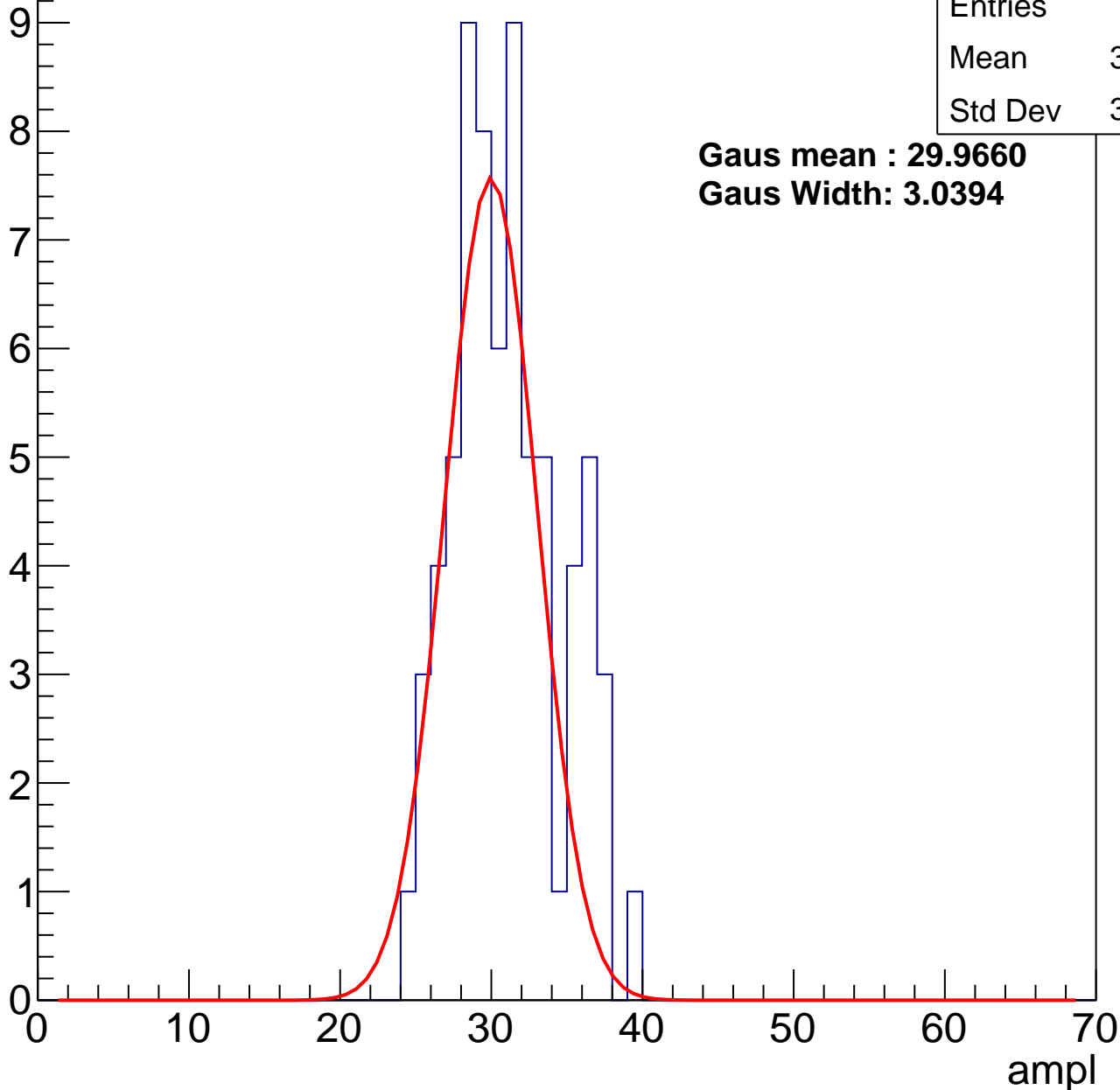
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	30.58
Std Dev	3.487

**Gaus mean : 29.9660**

**Gaus Width: 3.0394**



# B1L101S, U19-ch73, adc1

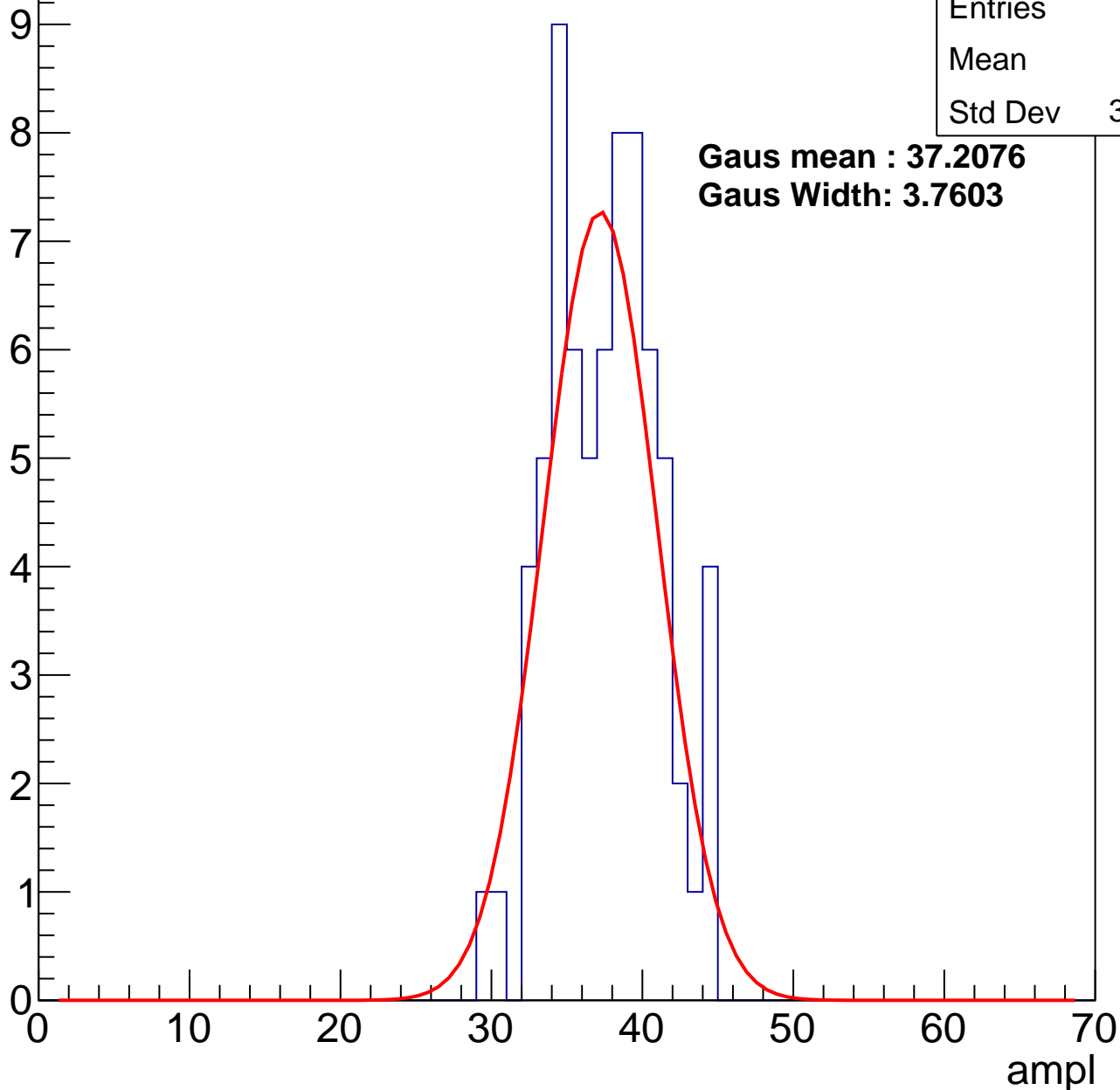
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	71
Mean	37.1
Std Dev	3.477

**Gaus mean : 37.2076**

**Gaus Width: 3.7603**



# B1L101S, U19-ch73, adc2

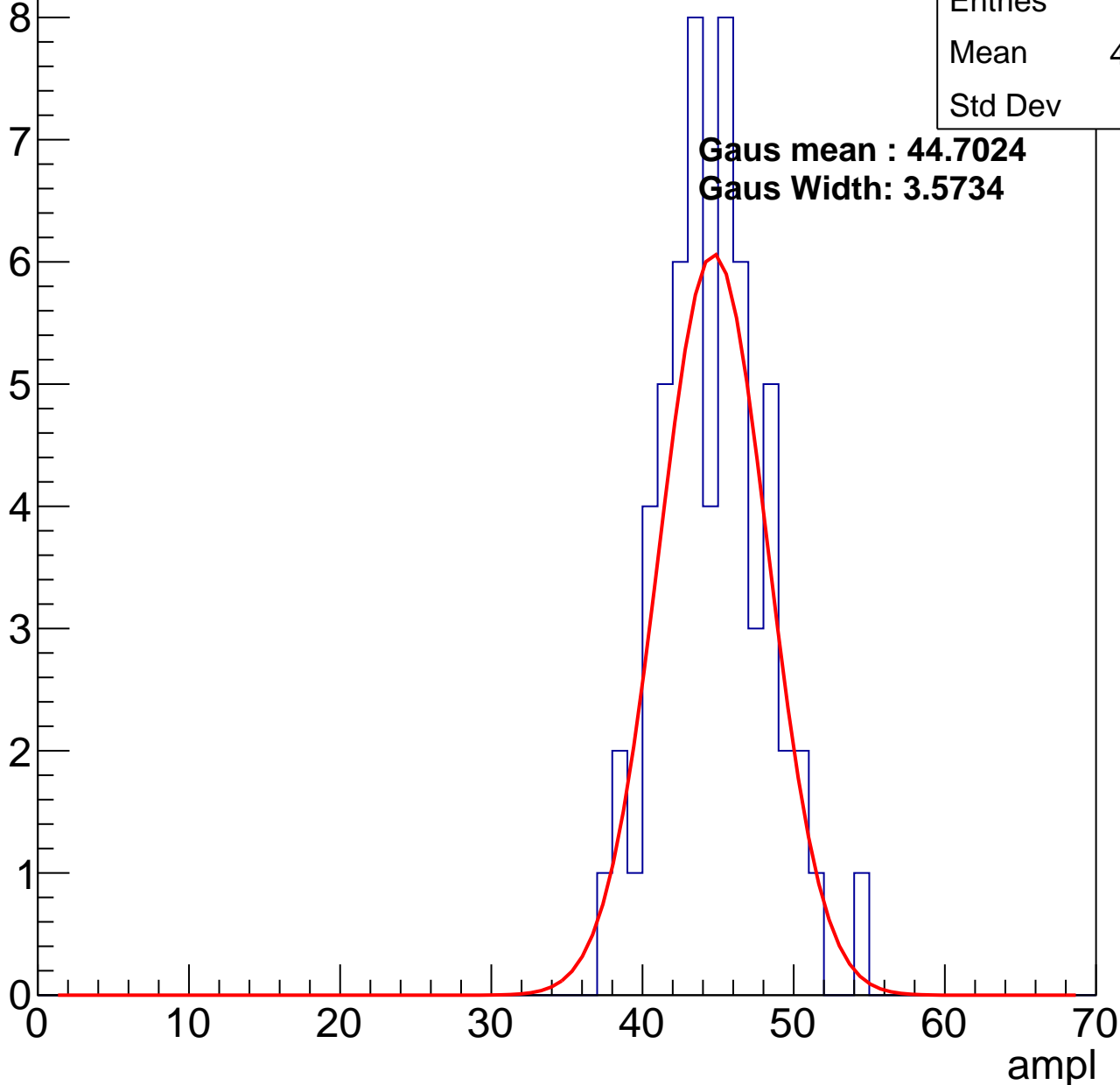
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	59
Mean	44.22
Std Dev	3.43

**Gaus mean : 44.7024**

**Gaus Width: 3.5734**

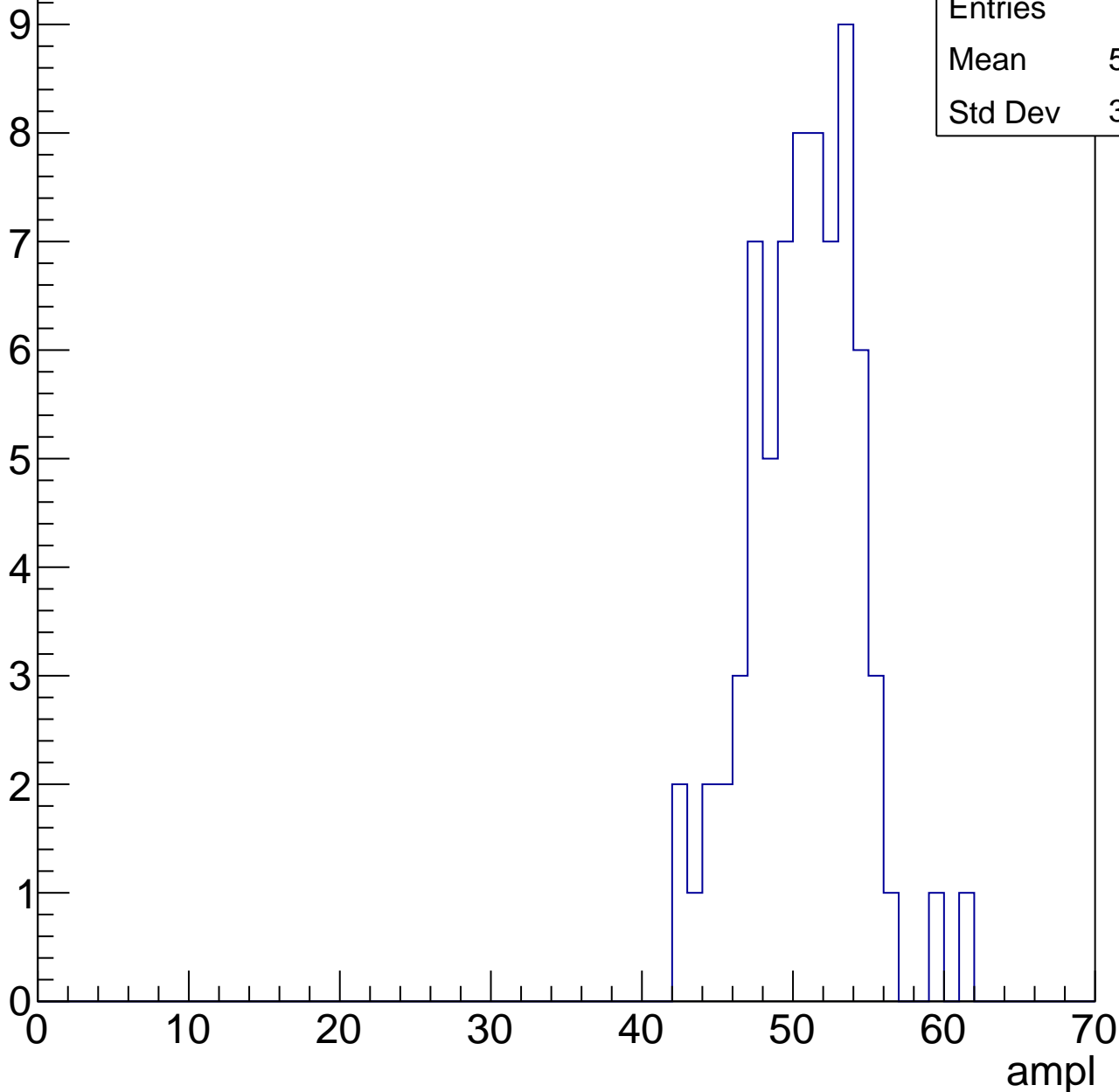


# B1L101S, U19-ch73, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	73
Mean	50.26
Std Dev	3.623

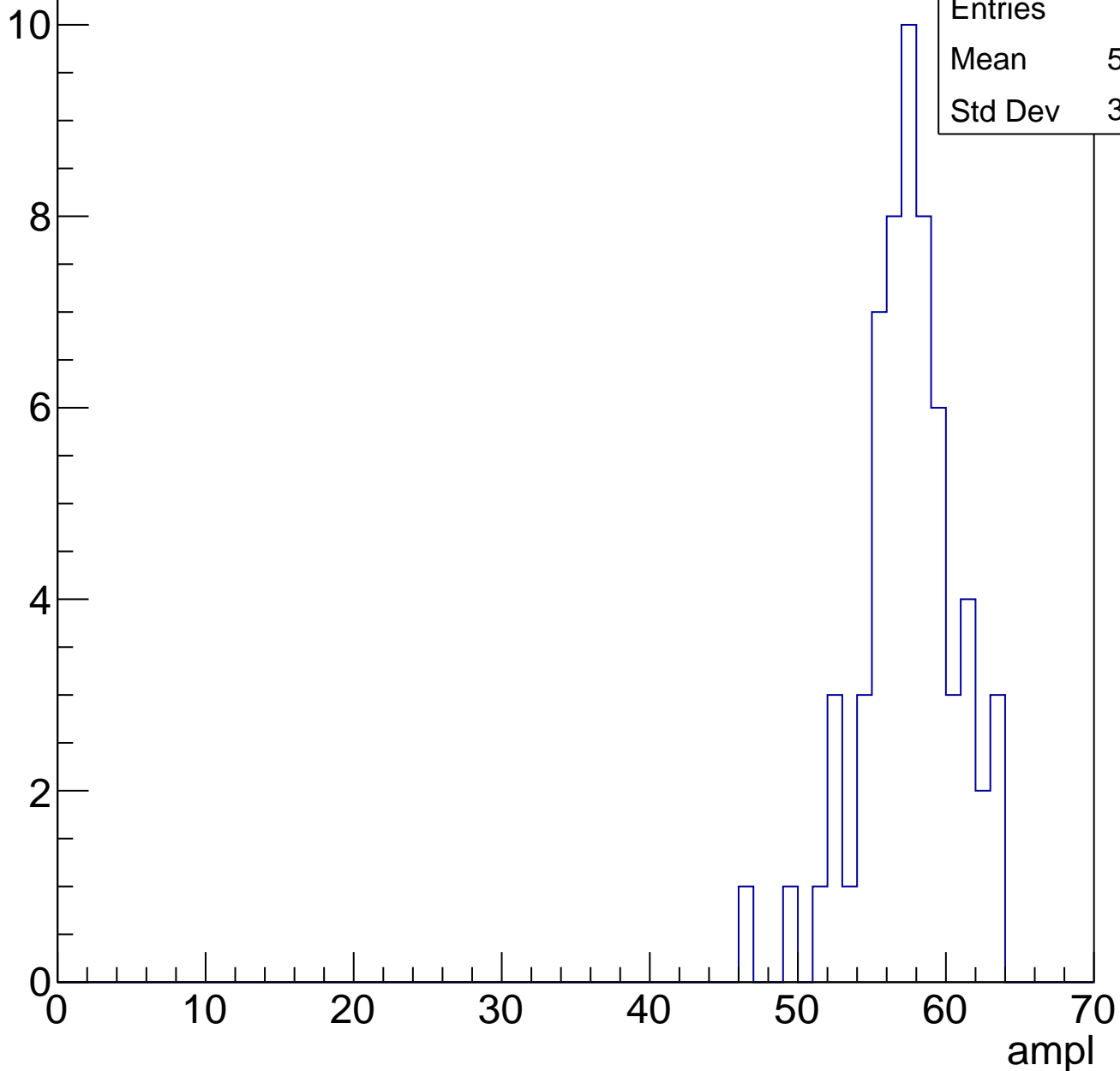


# B1L101S, U19-ch73, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	56.97
Std Dev	3.279

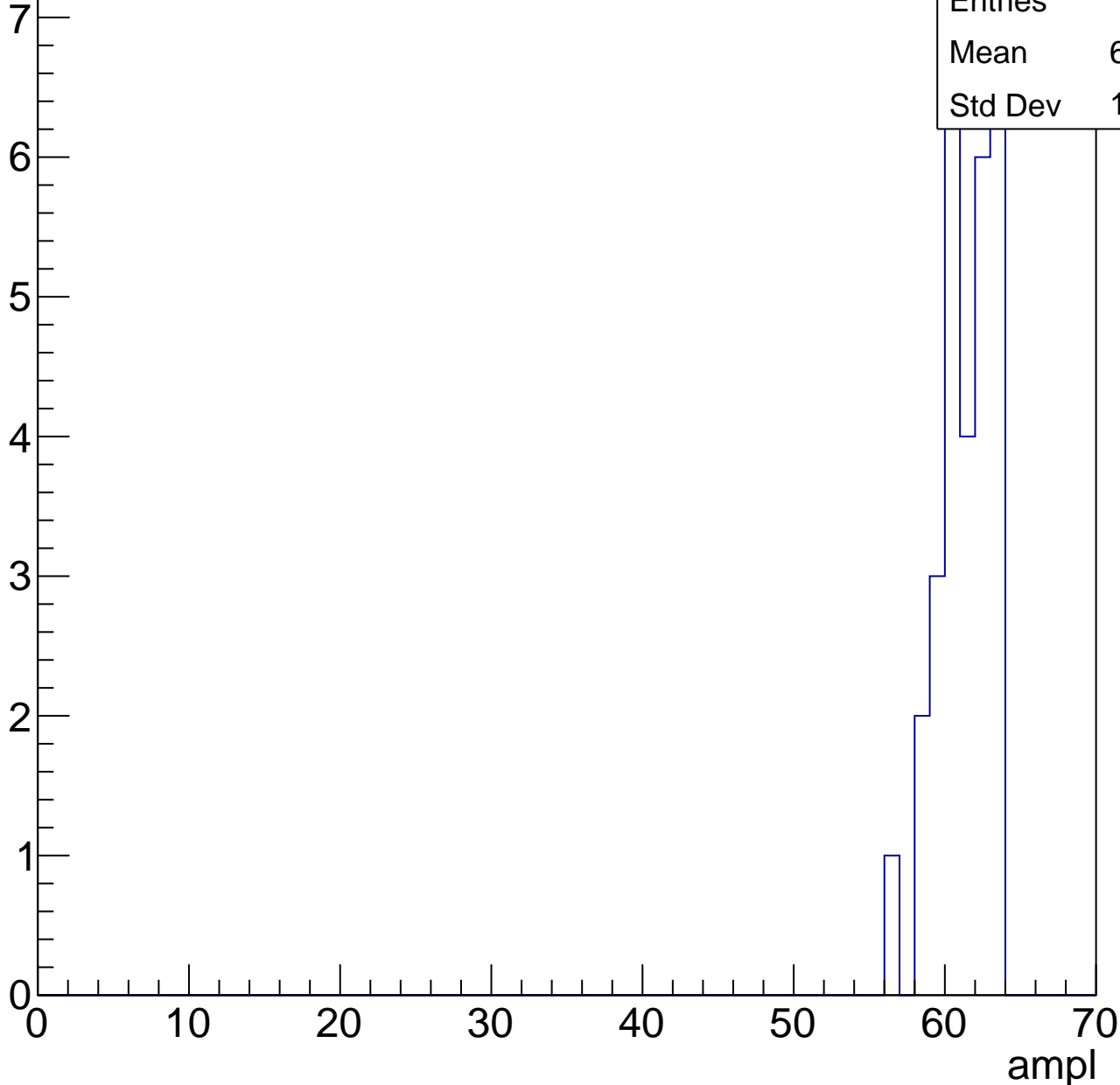


# B1L101S, U19-ch73, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

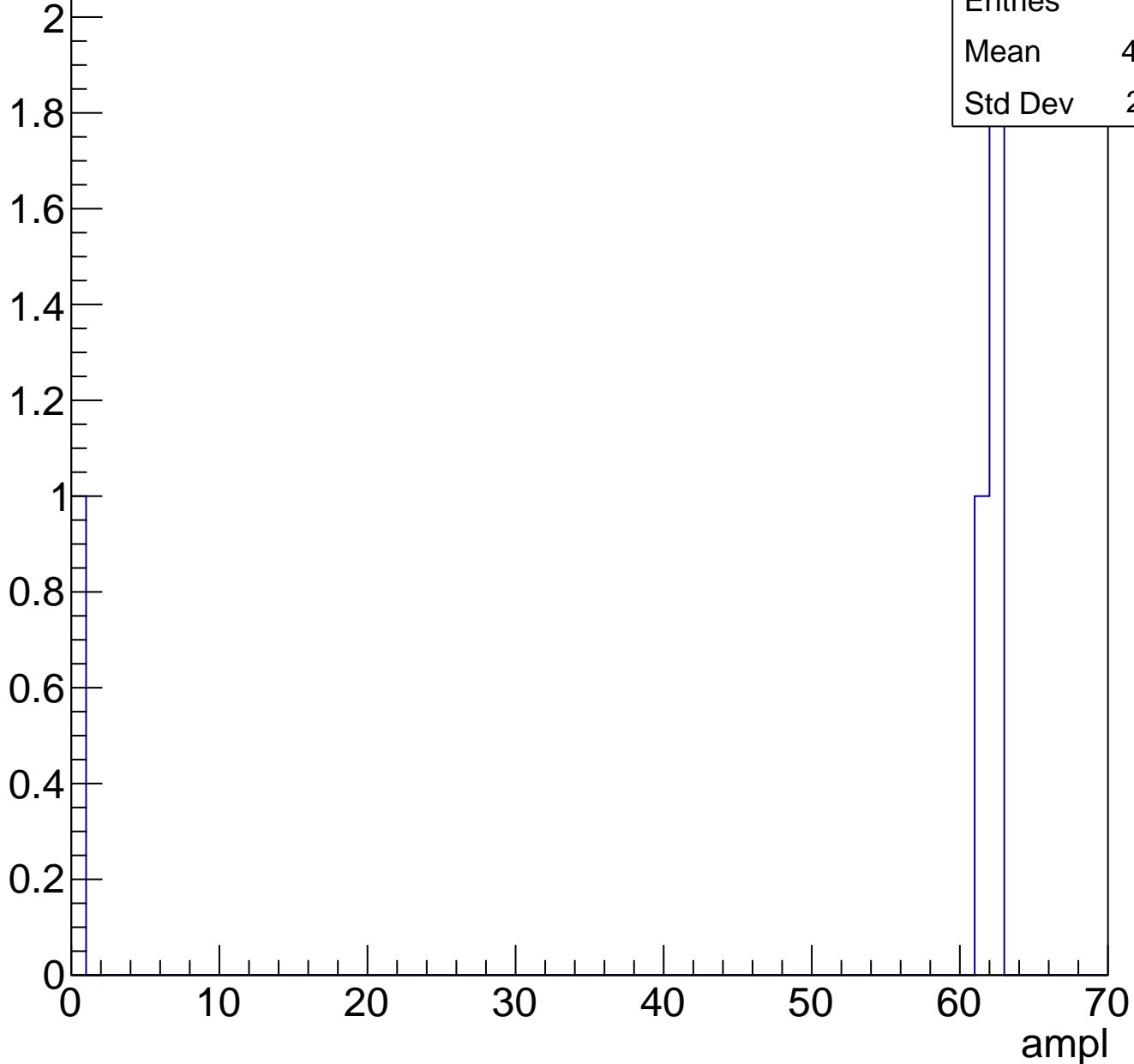
Entries	30
Mean	60.87
Std Dev	1.784



# B1L101S, U19-ch73, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U19-ch73, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U19-ch74, adc0

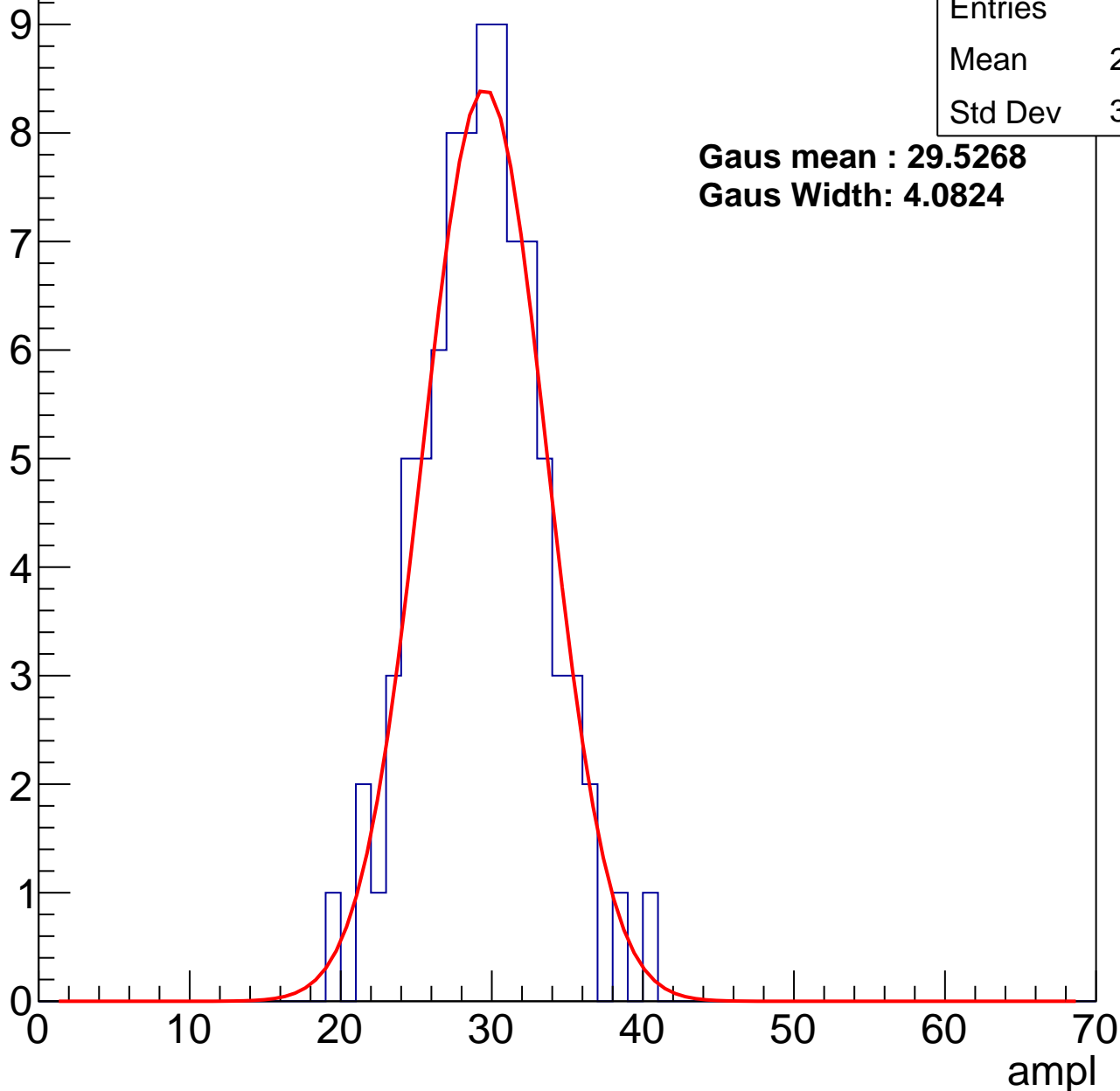
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	86
Mean	28.92
Std Dev	3.957

**Gaus mean : 29.5268**

**Gaus Width: 4.0824**



# B1L101S, U19-ch74, adc1

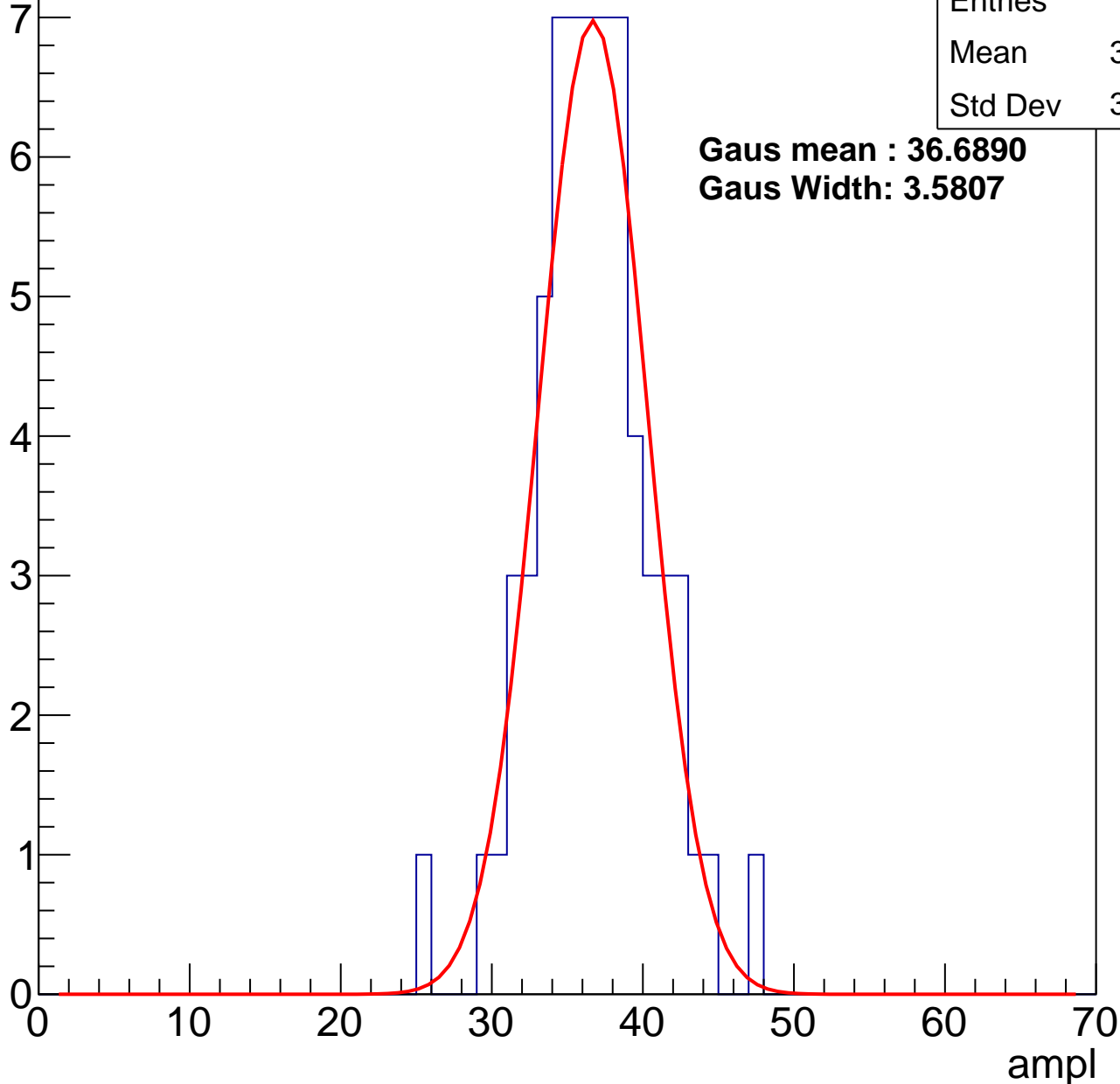
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	36.26
Std Dev	3.804

**Gaus mean : 36.6890**

**Gaus Width: 3.5807**



# B1L101S, U19-ch74, adc2

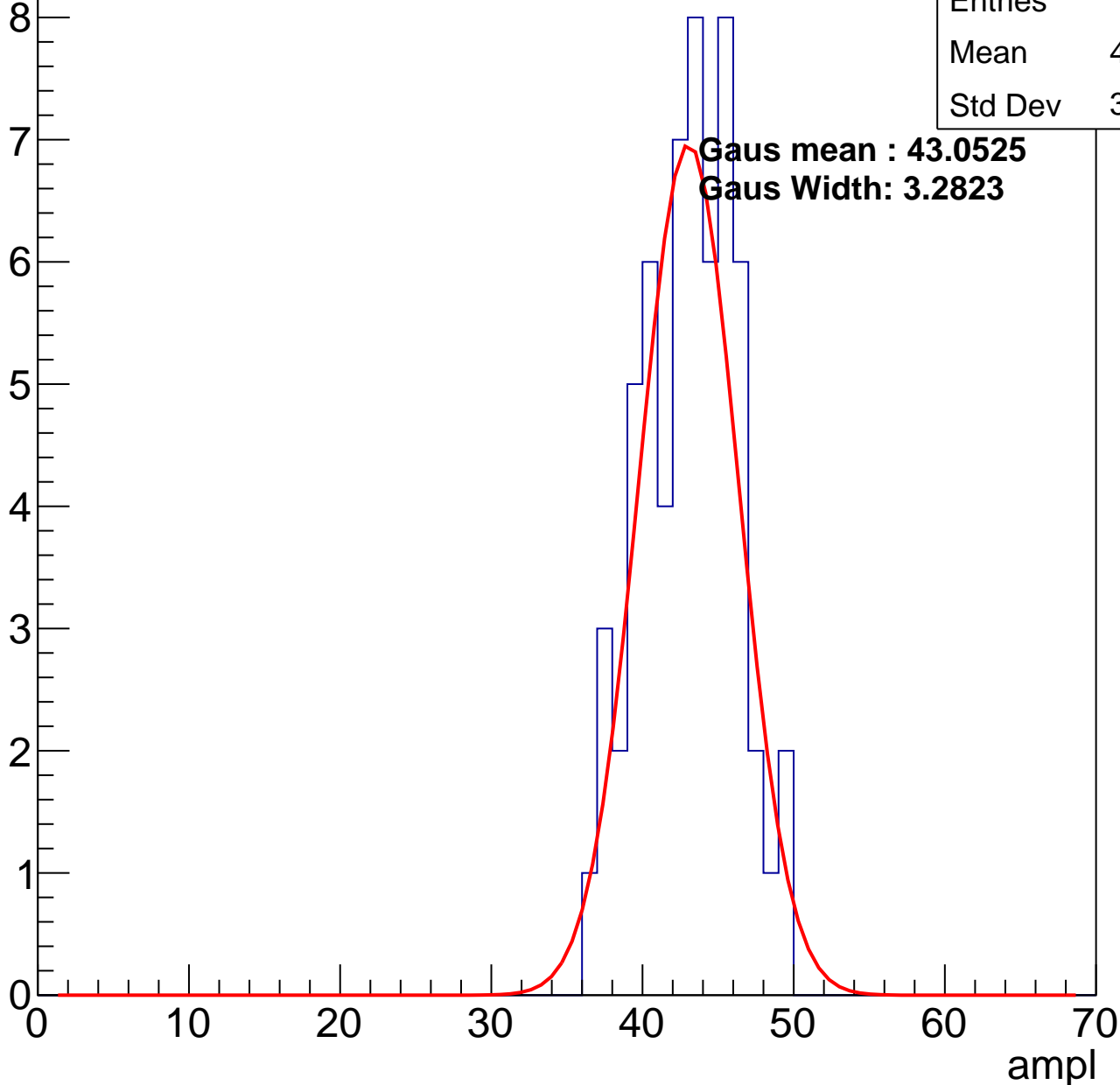
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	42.62
Std Dev	3.074

**Gaus mean : 43.0525**

**Gaus Width: 3.2823**

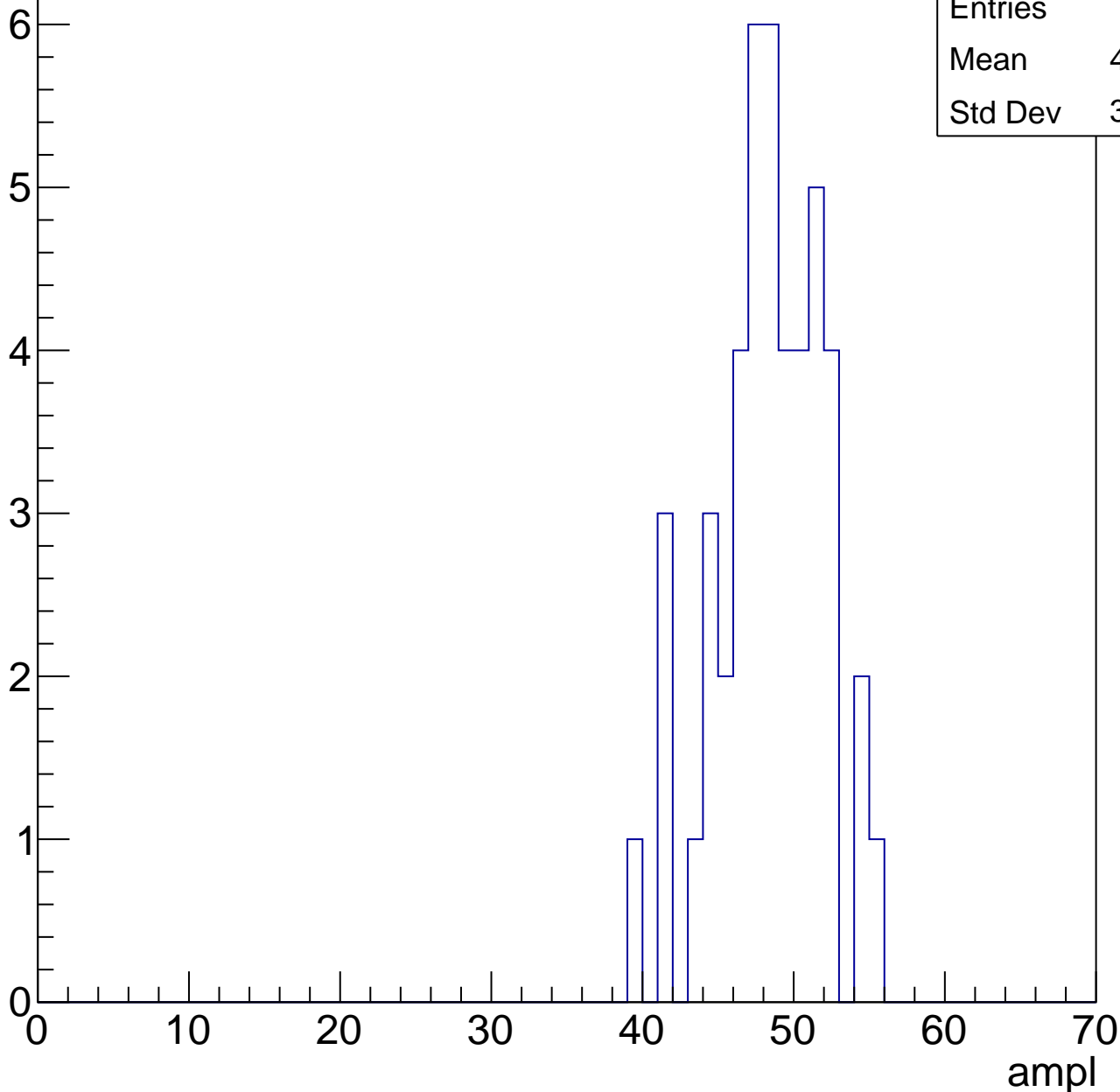


# B1L101S, U19-ch74, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

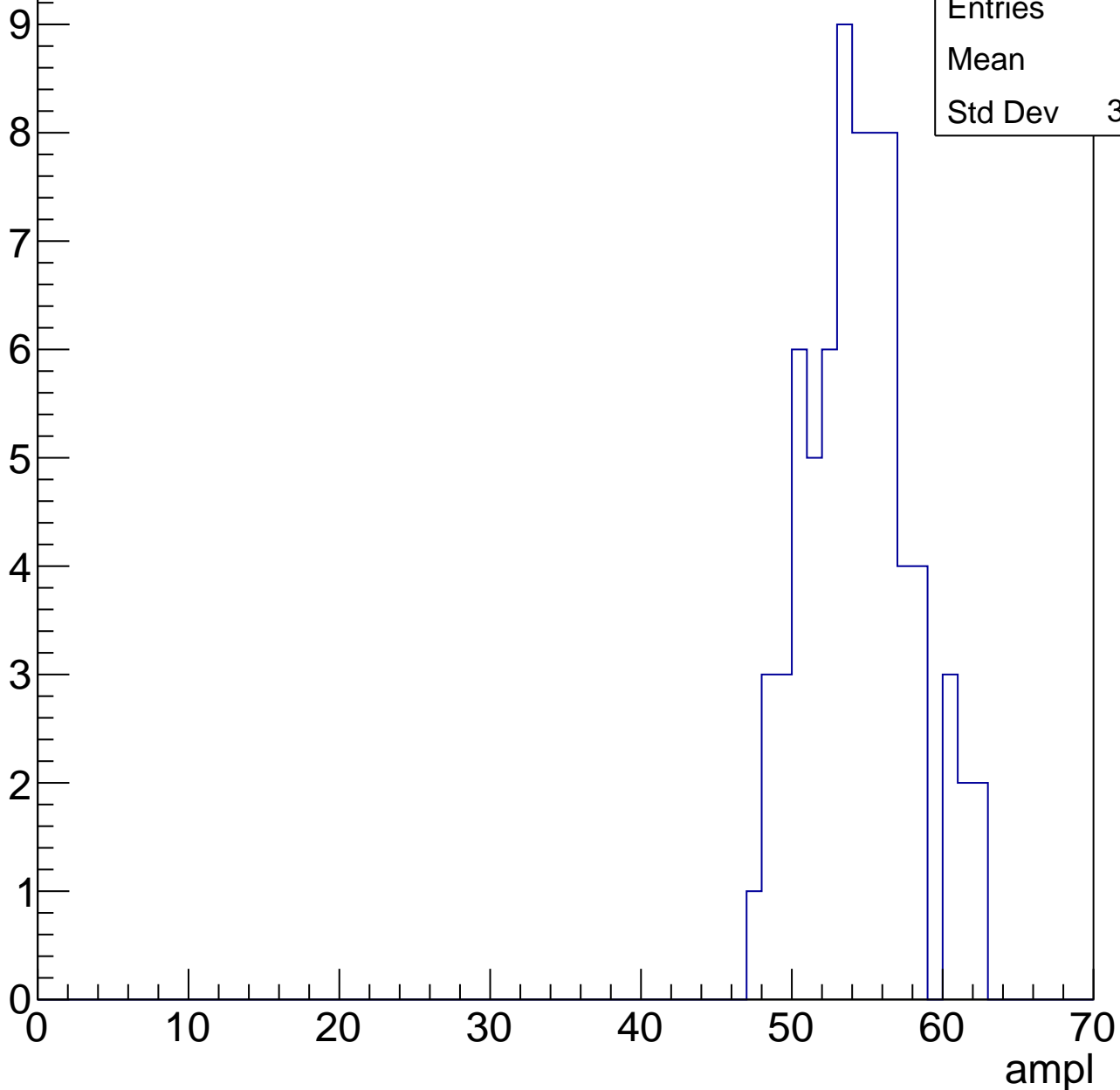
Entries	46
Mean	47.89
Std Dev	3.583



# B1L101S, U19-ch74, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



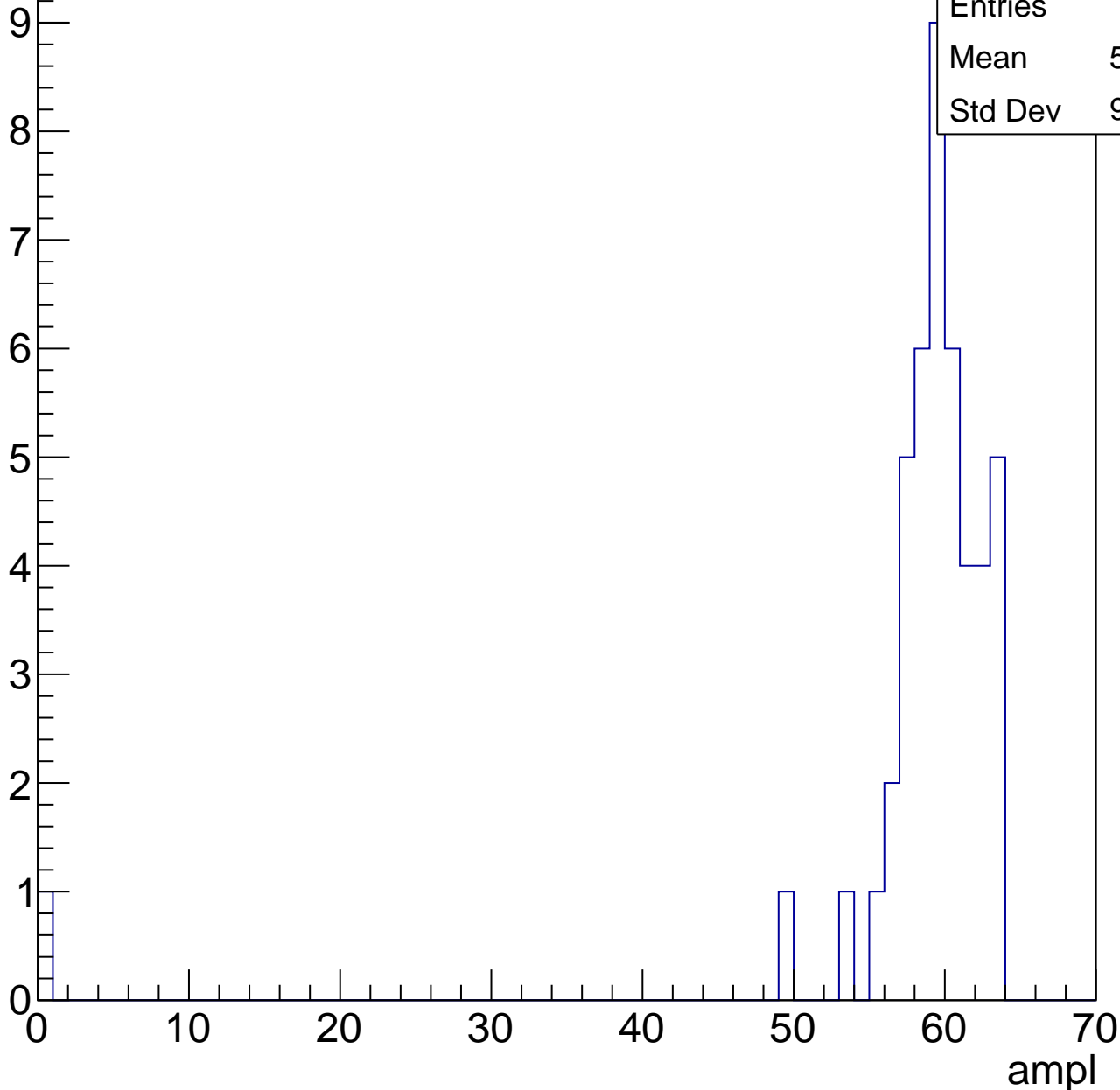
Entries	72
Mean	54
Std Dev	3.496

# B1L101S, U19-ch74, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	45
Mean	57.78
Std Dev	9.126

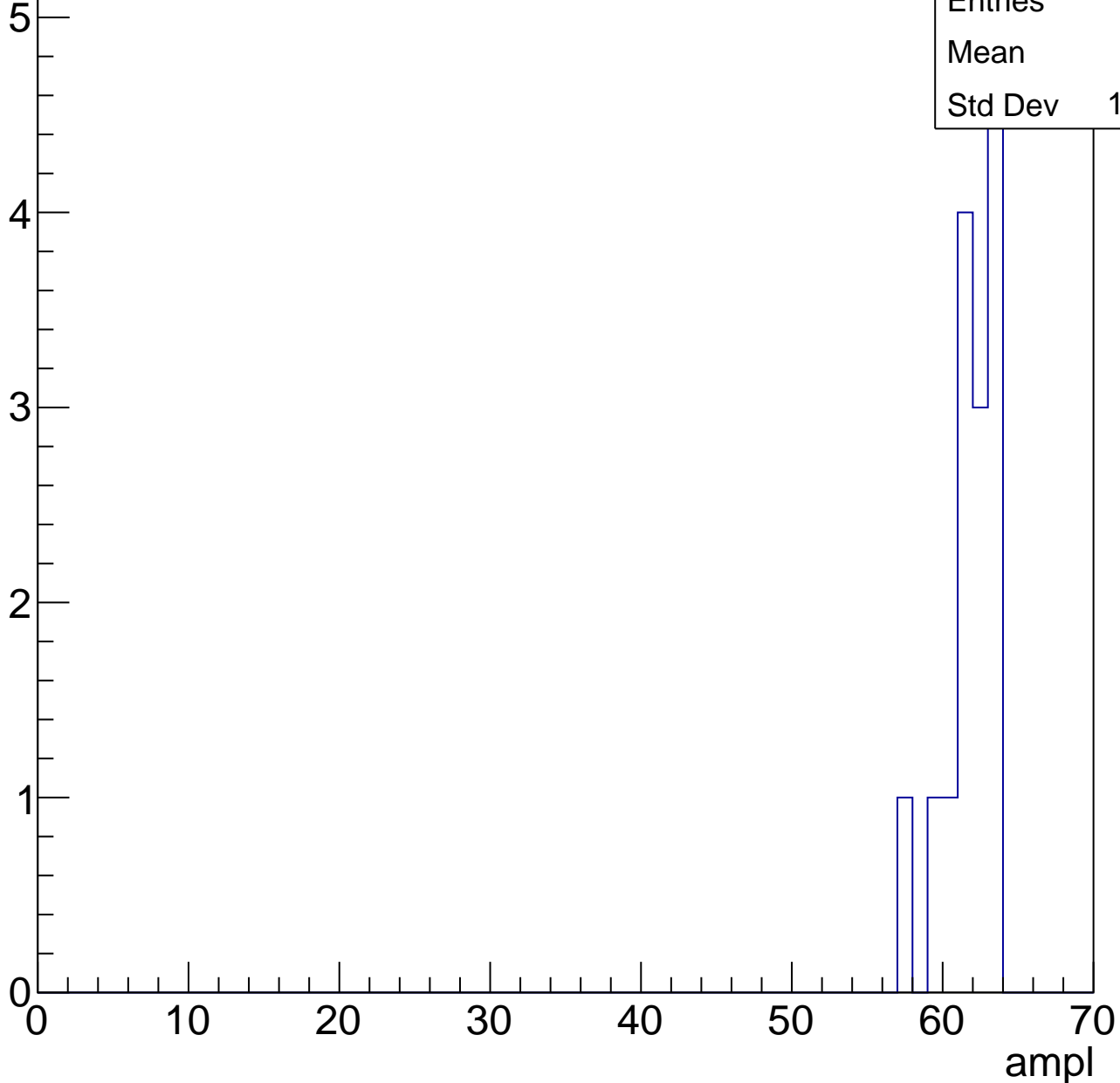


# B1L101S, U19-ch74, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	15
Mean	61.4
Std Dev	1.665





# B1L101S, U19-ch74, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U19-ch75, adc0

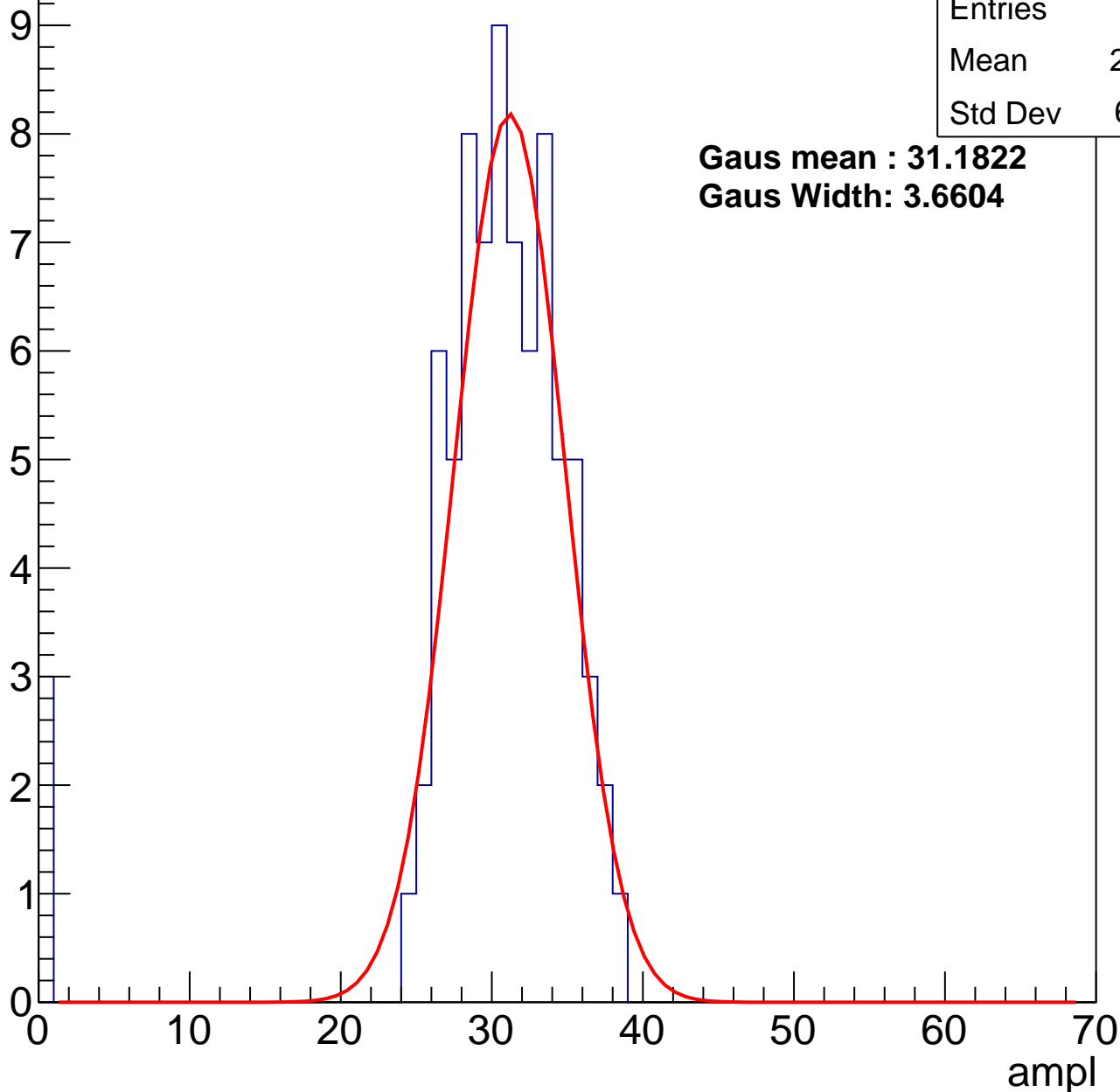
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	78
Mean	29.49
Std Dev	6.721

**Gaus mean : 31.1822**

**Gaus Width: 3.6604**



# B1L101S, U19-ch75, adc1

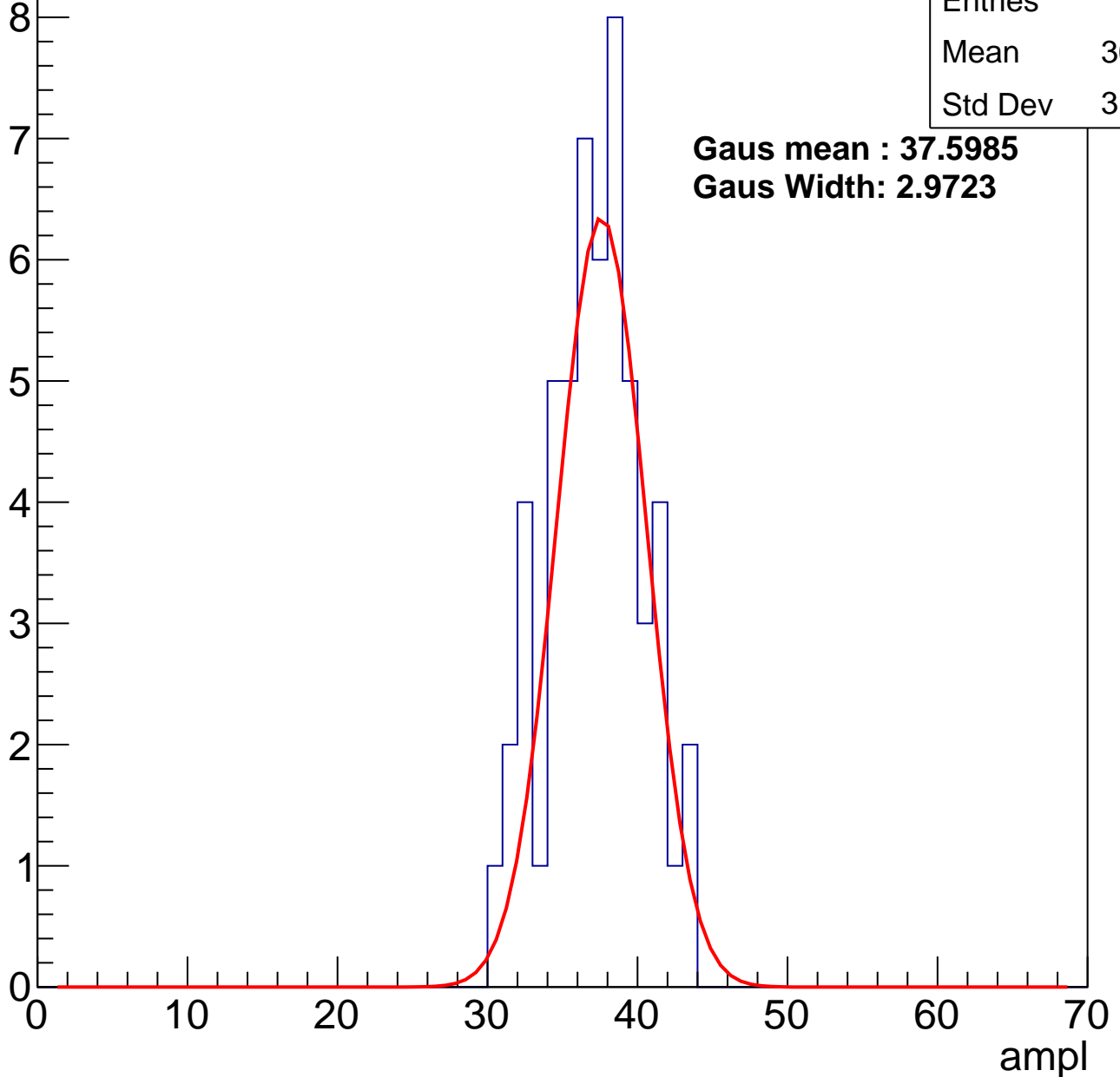
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	54
Mean	36.72
Std Dev	3.106

**Gaus mean : 37.5985**

**Gaus Width: 2.9723**



# B1L101S, U19-ch75, adc2

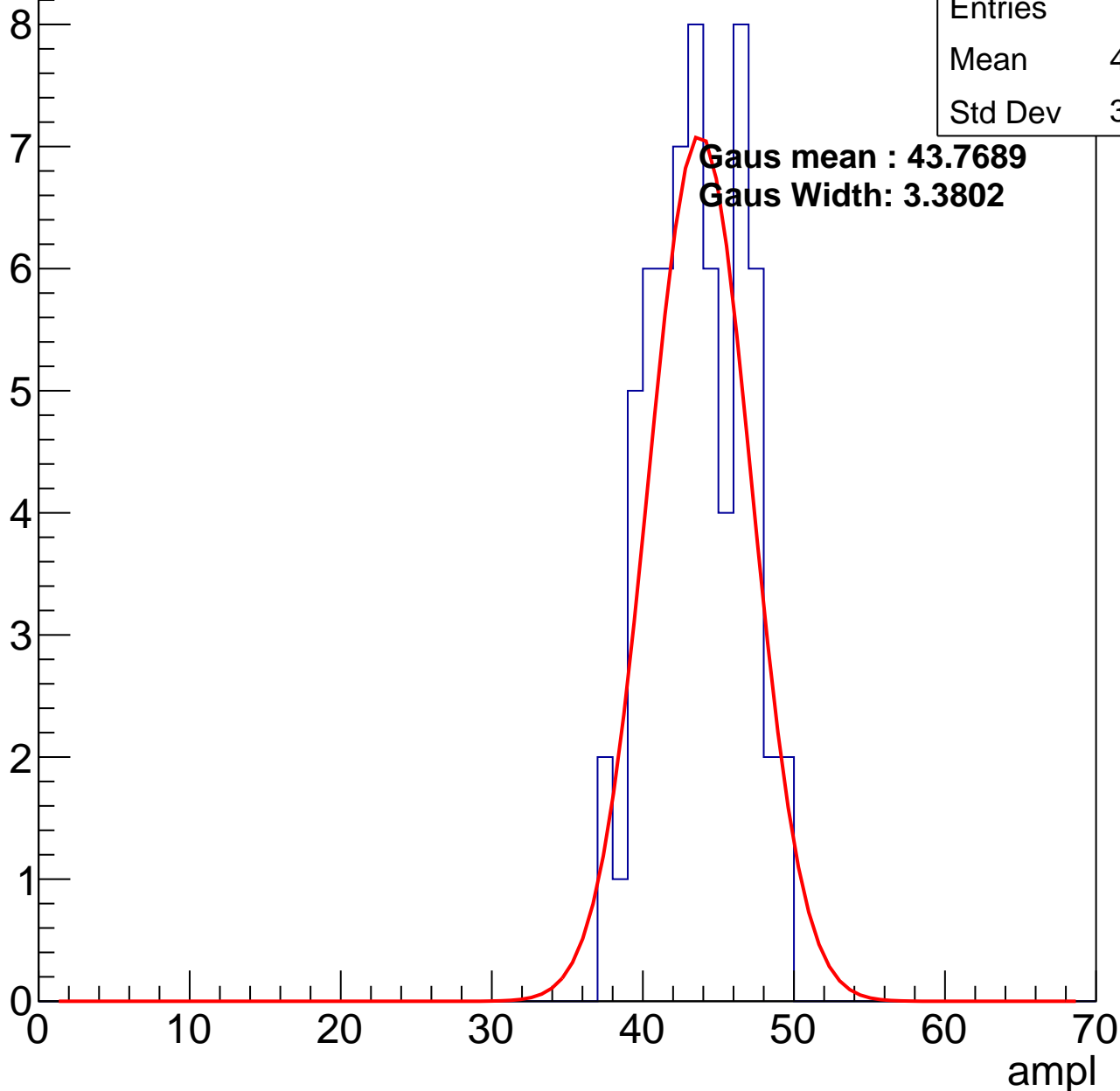
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	43.16
Std Dev	3.014

**Gaus mean : 43.7689**

**Gaus Width: 3.3802**

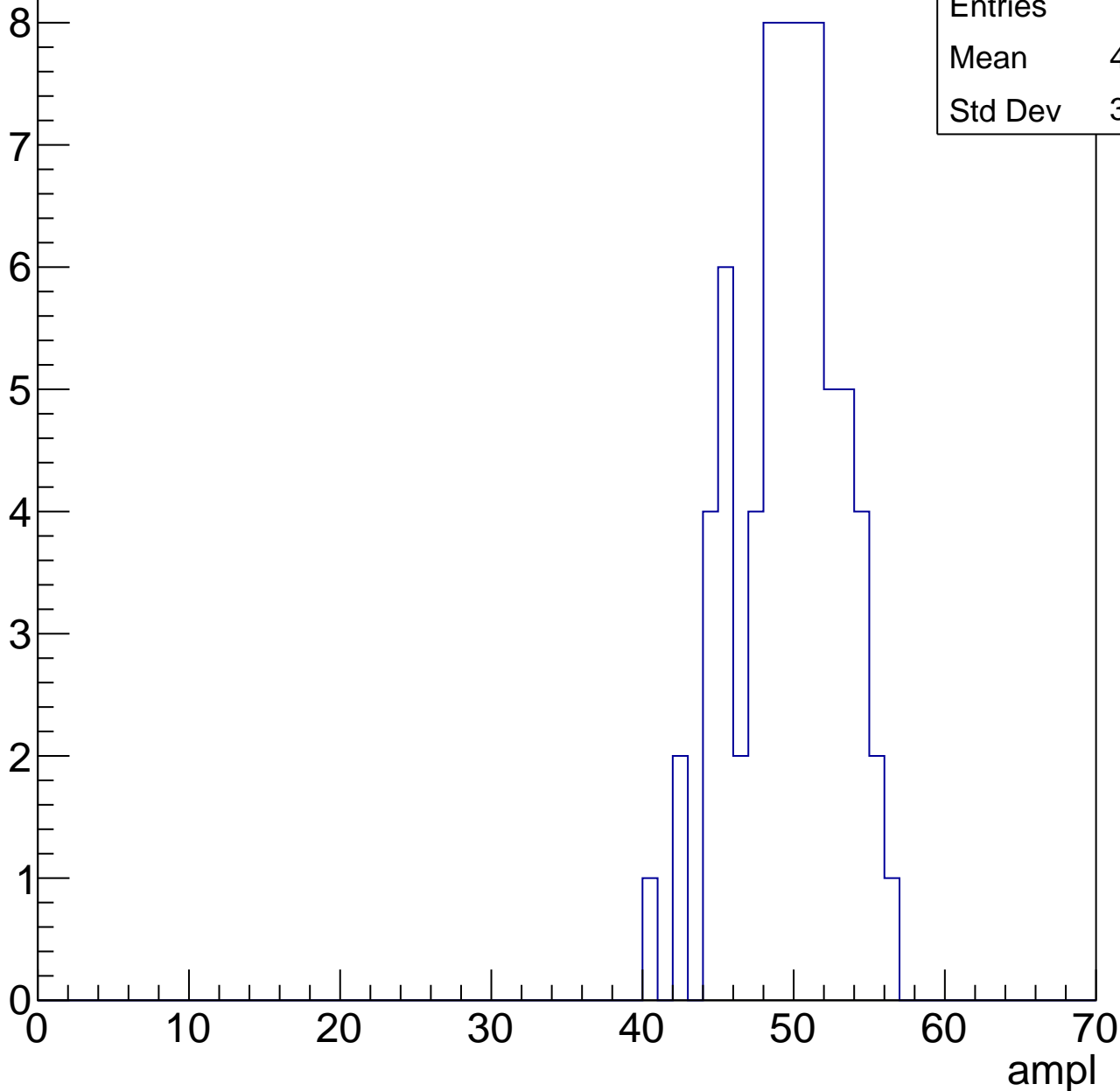


# B1L101S, U19-ch75, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	49.13
Std Dev	3.434

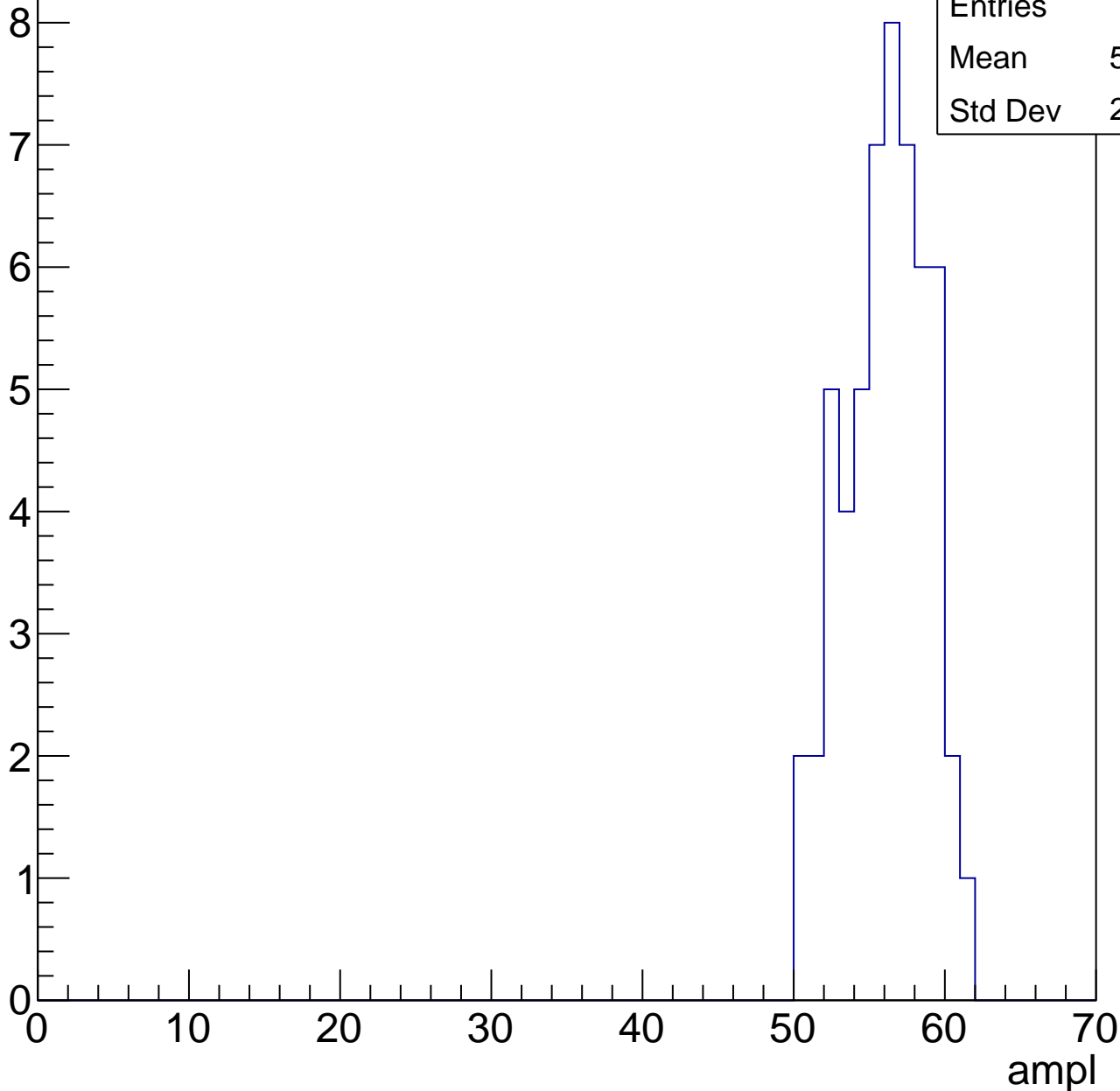


# B1L101S, U19-ch75, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

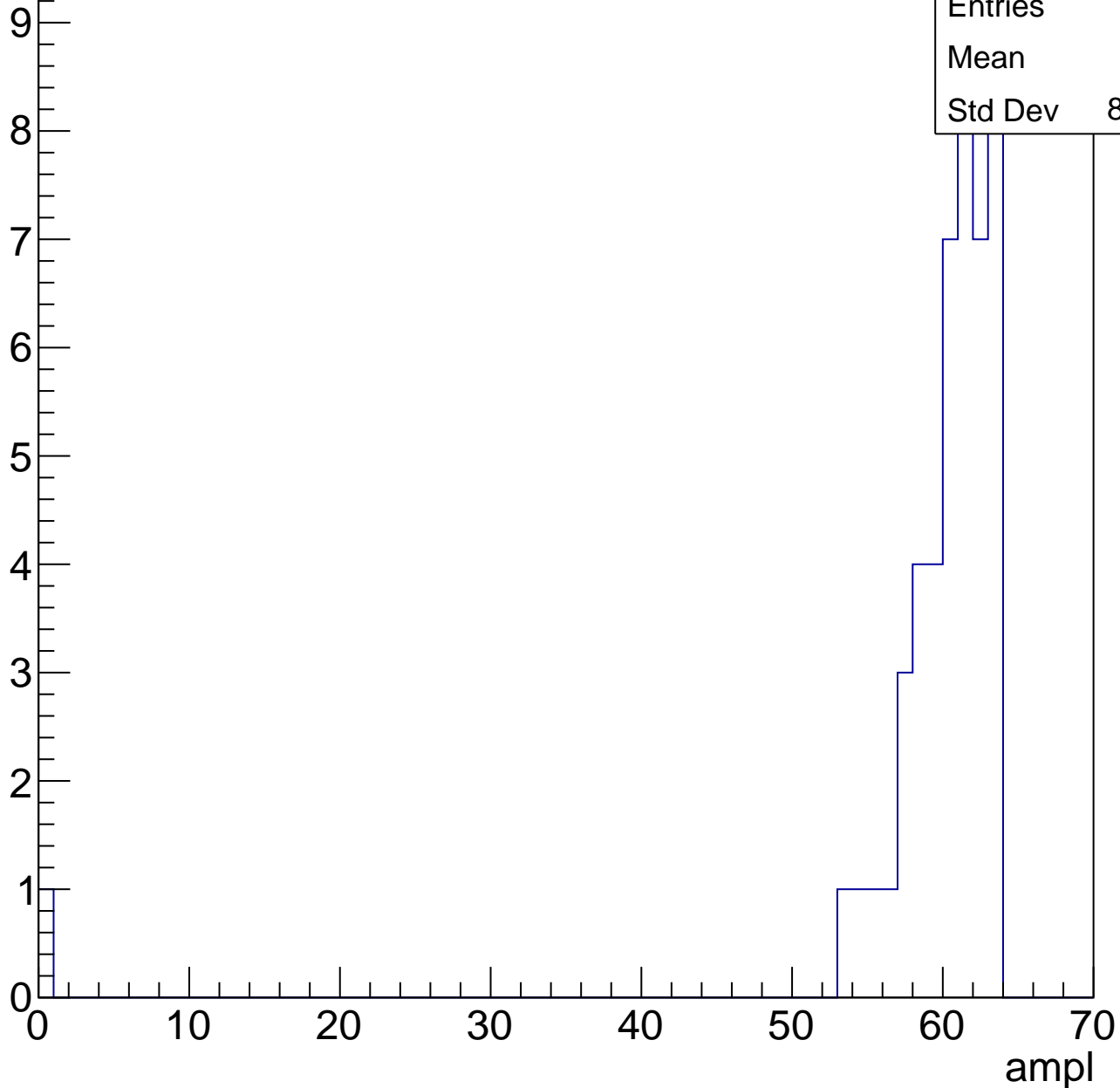
Entries	55
Mean	55.62
Std Dev	2.693



# B1L101S, U19-ch75, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

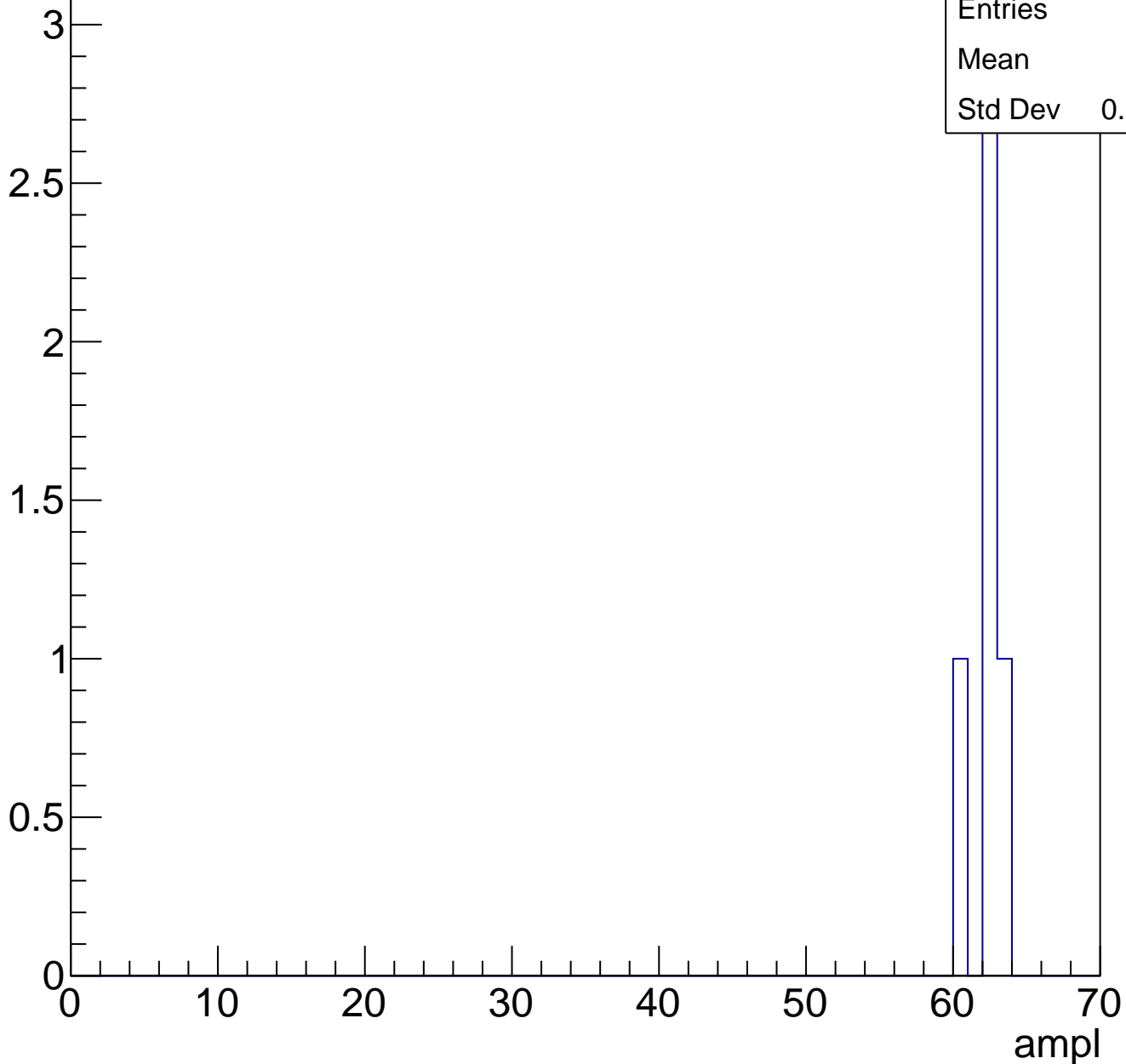


Entries	48
Mean	58.9
Std Dev	8.936

# B1L101S, U19-ch75, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U19-ch75, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L101S, U19-ch76, adc0

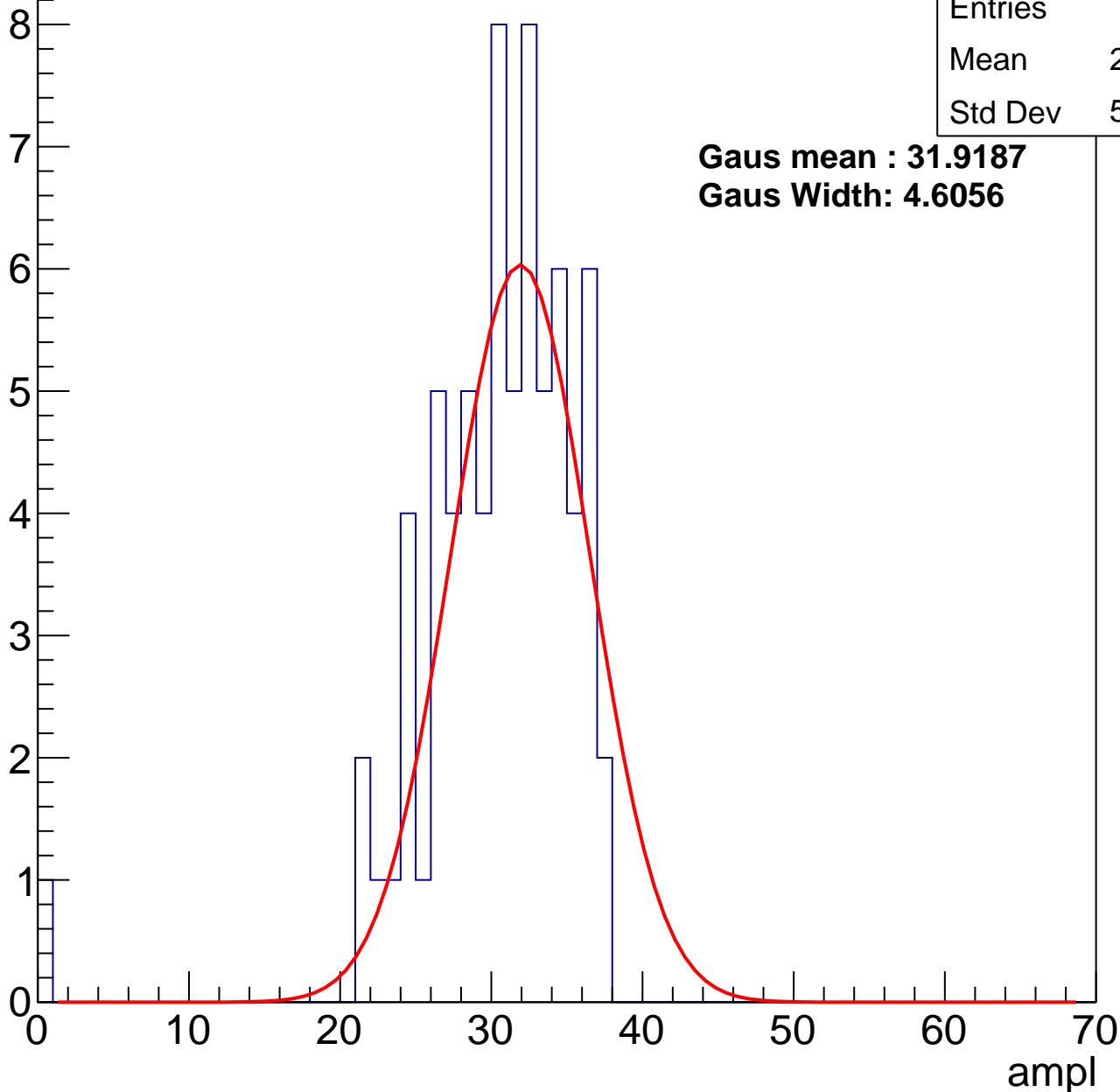
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	72
Mean	29.89
Std Dev	5.369

**Gaus mean : 31.9187**

**Gaus Width: 4.6056**



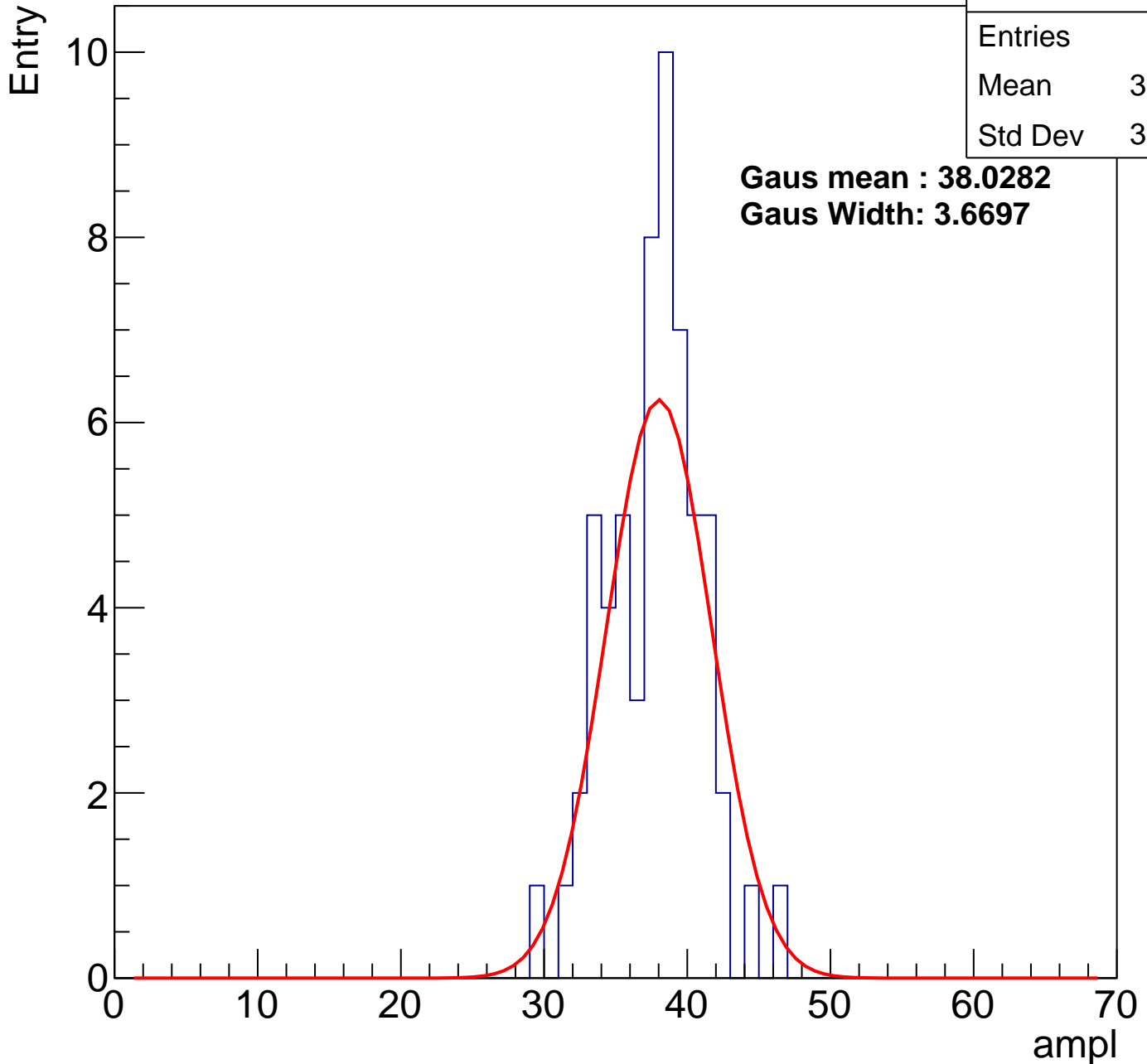
# B1L101S, U19-ch76, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	60
Mean	37.27
Std Dev	3.235

**Gaus mean : 38.0282**

**Gaus Width: 3.6697**



# B1L101S, U19-ch76, adc2

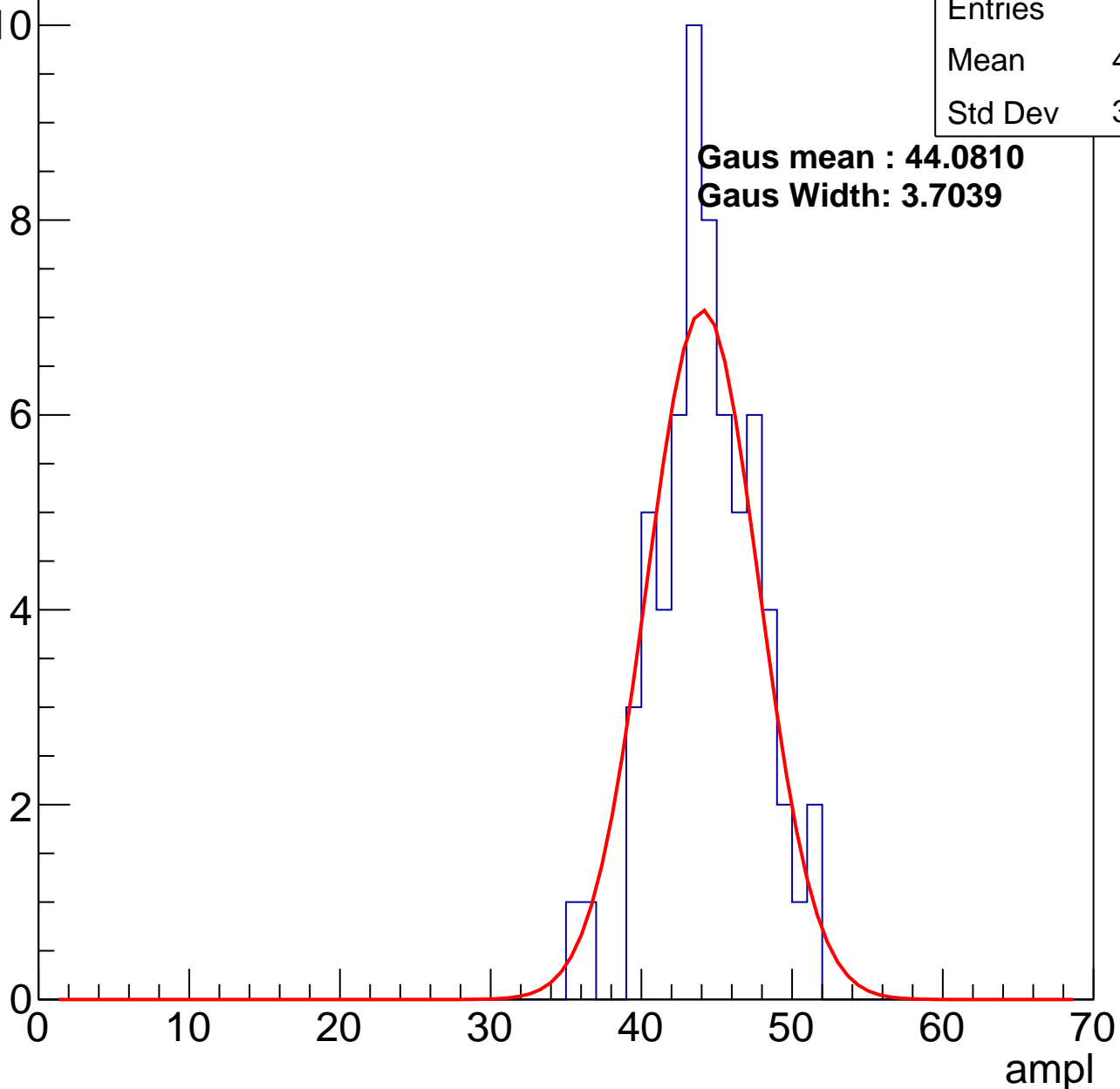
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	43.91
Std Dev	3.301

**Gaus mean : 44.0810**

**Gaus Width: 3.7039**

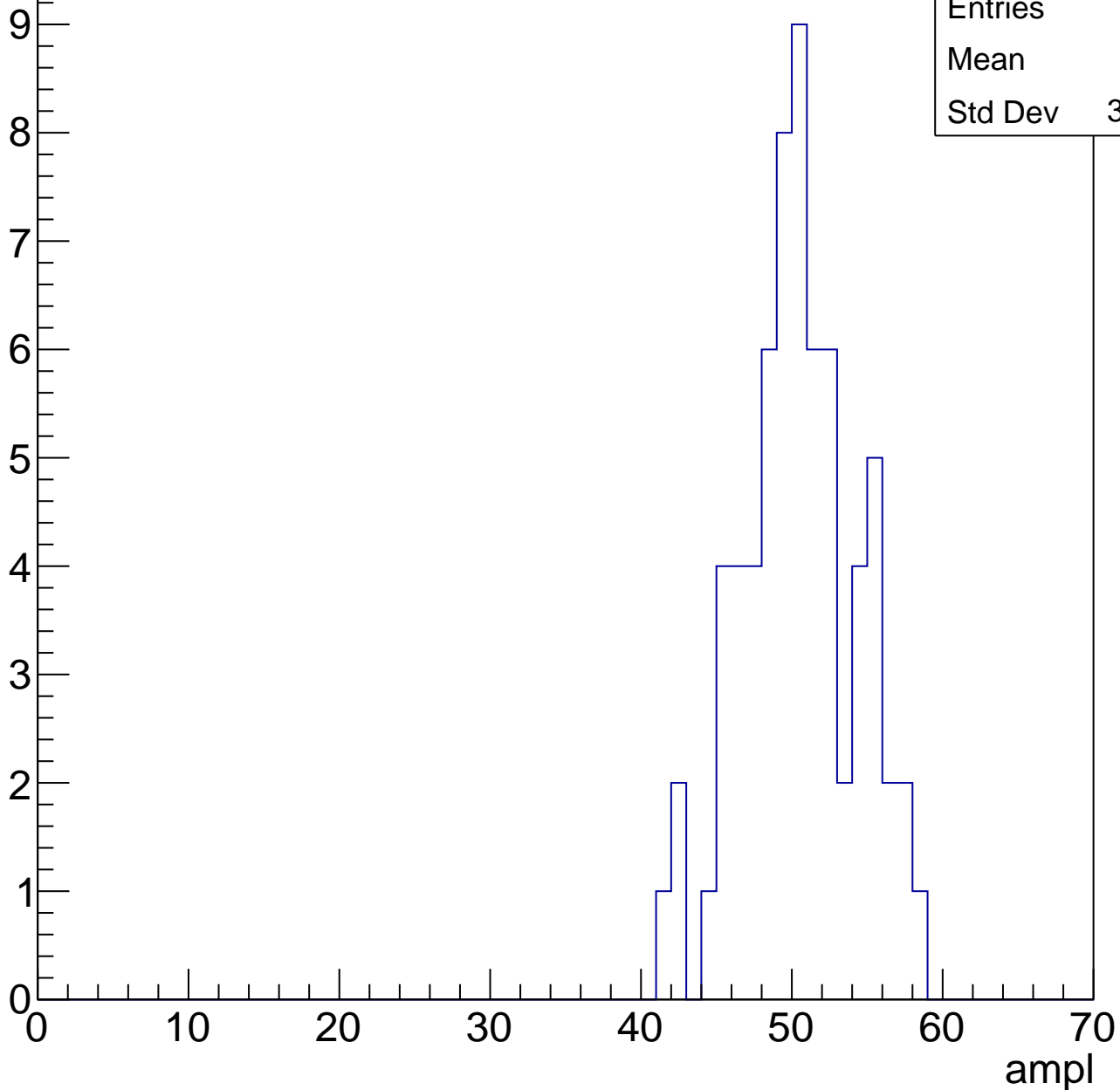


# B1L101S, U19-ch76, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

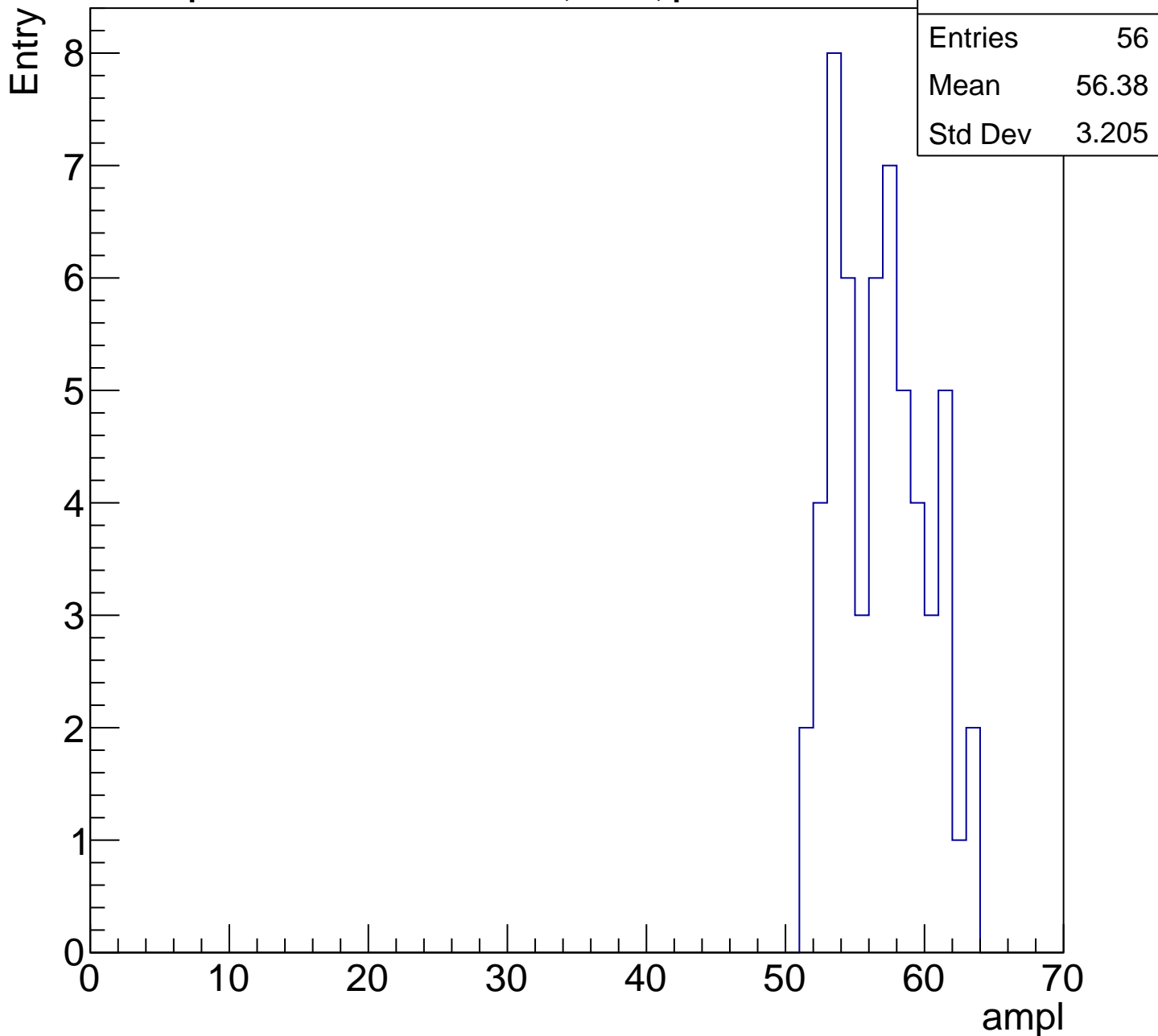
Entry

Entries	67
Mean	50
Std Dev	3.762



# B1L101S, U19-ch76, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

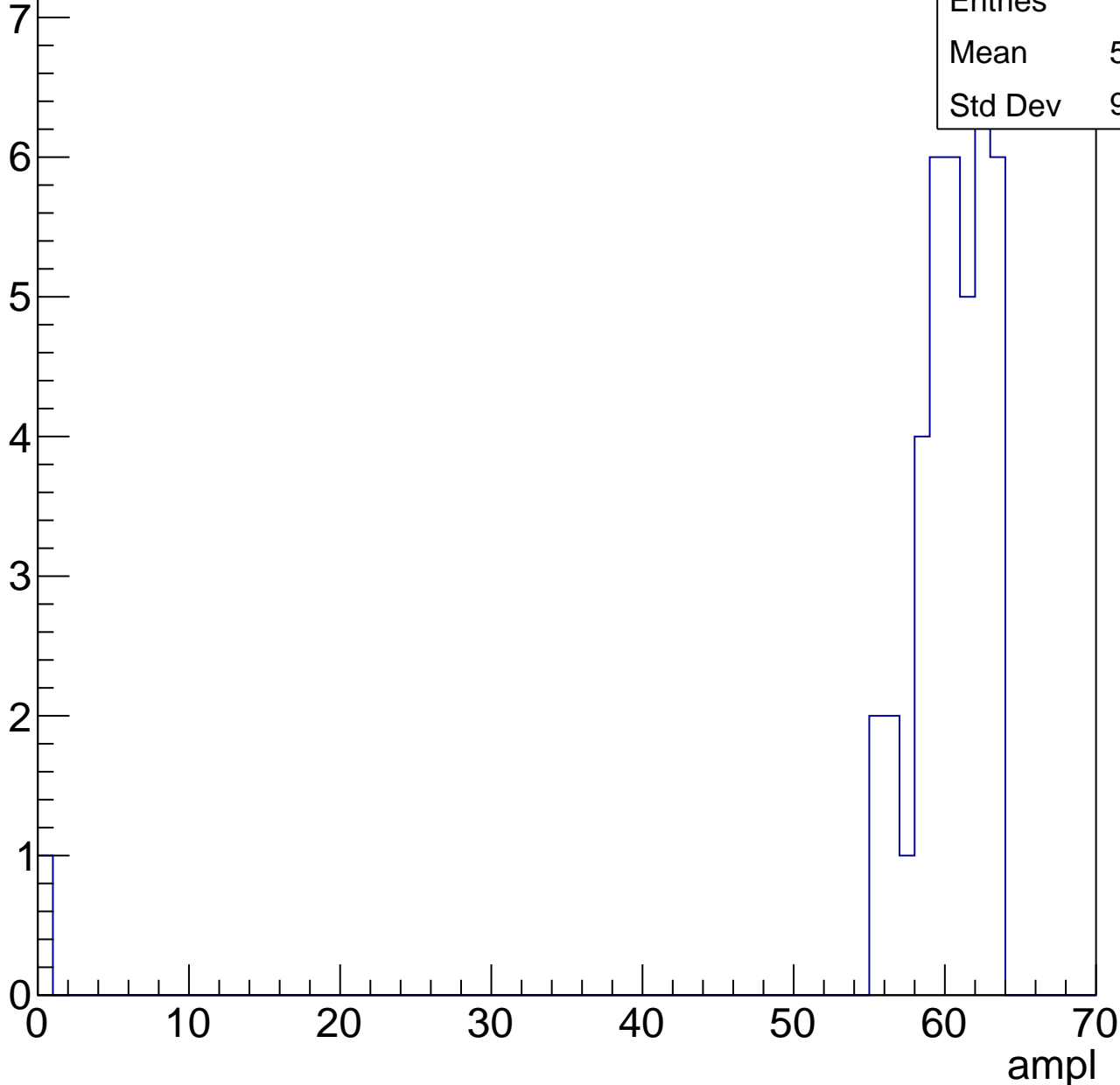


# B1L101S, U19-ch76, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

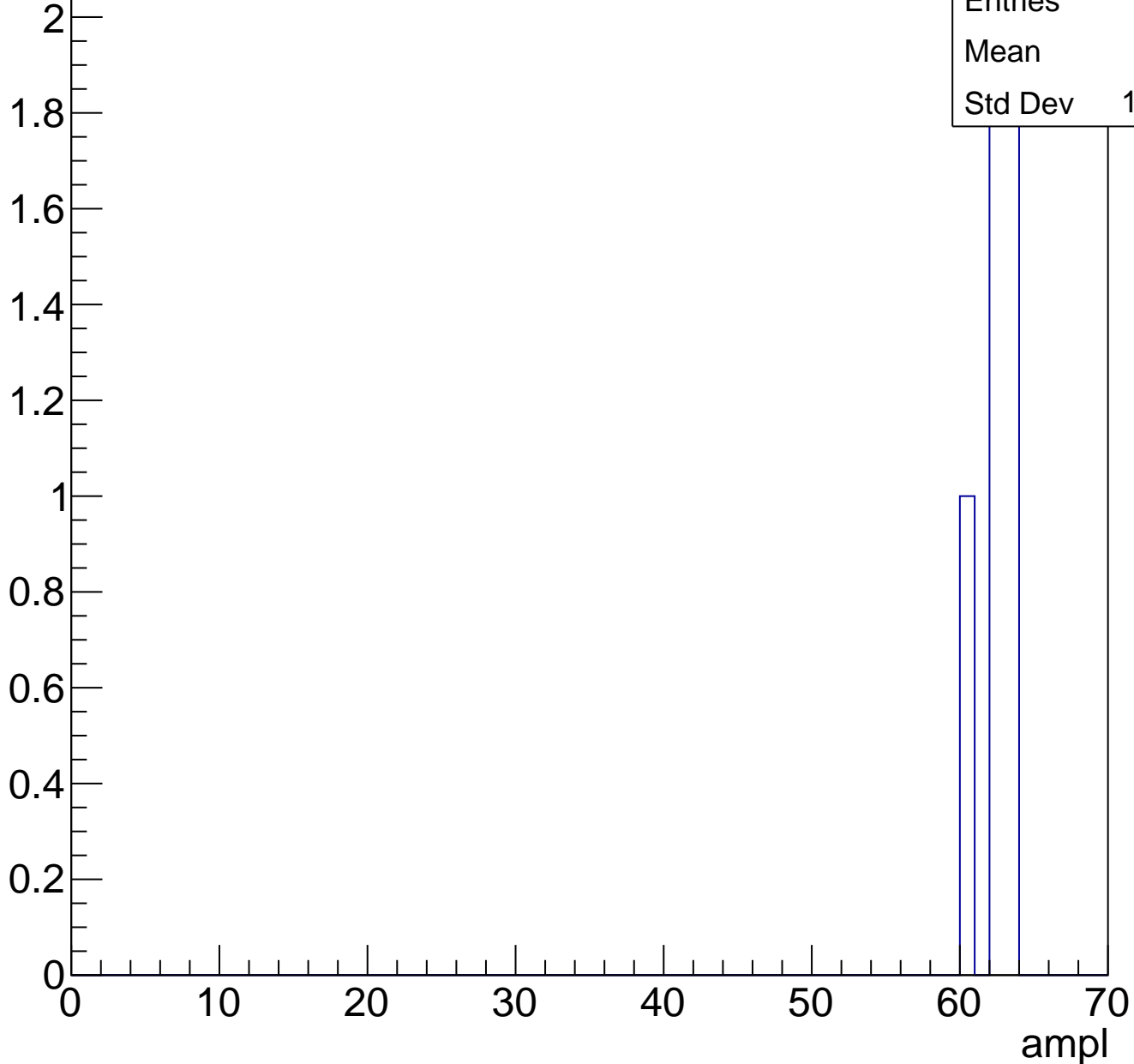
Entries	40
Mean	58.55
Std Dev	9.638



# B1L101S, U19-ch76, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U19-ch76, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	3
Mean	0
Std Dev	0

# B1L101S, U19-ch77, adc0

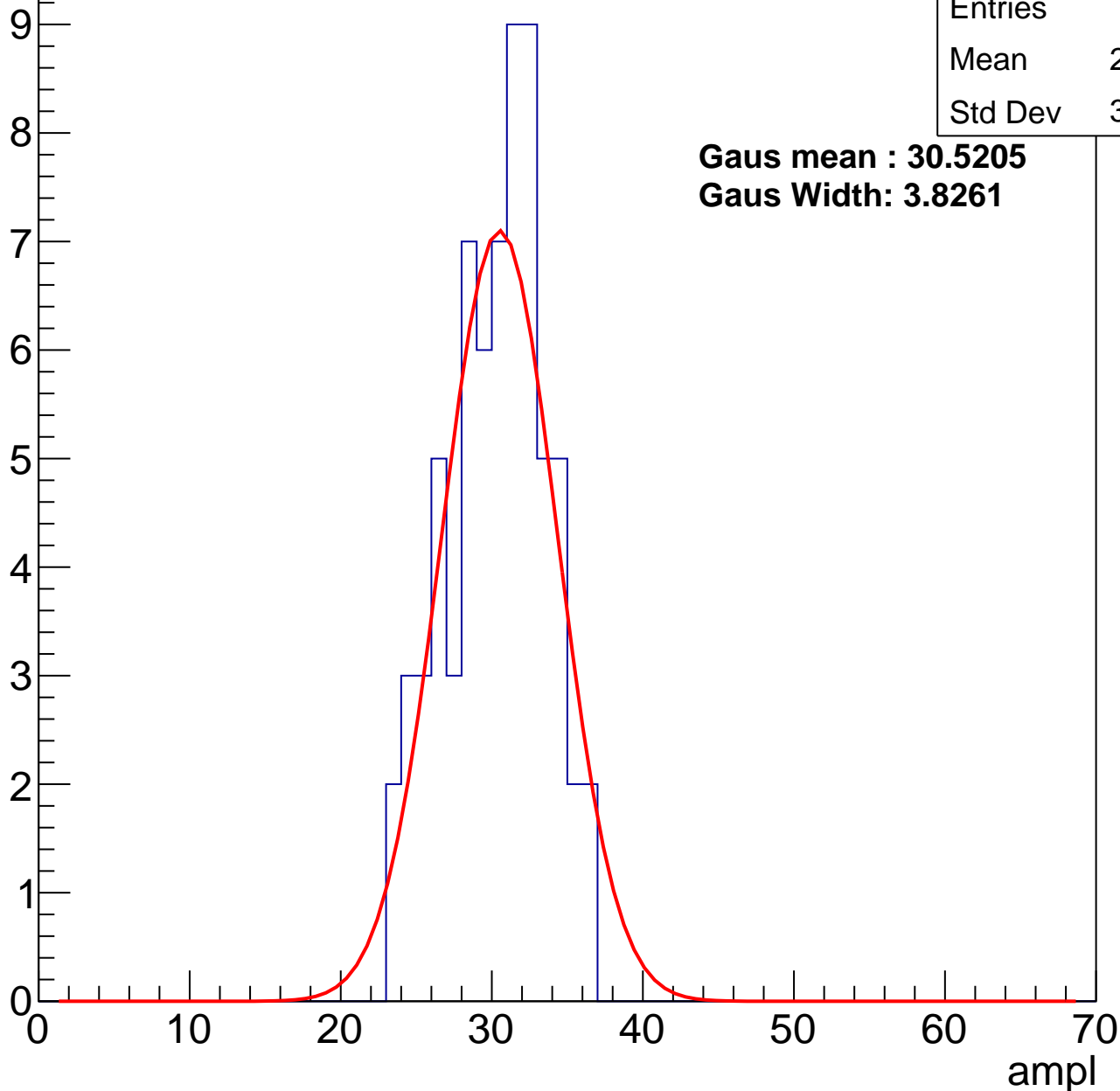
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	29.82
Std Dev	3.236

**Gaus mean : 30.5205**

**Gaus Width: 3.8261**



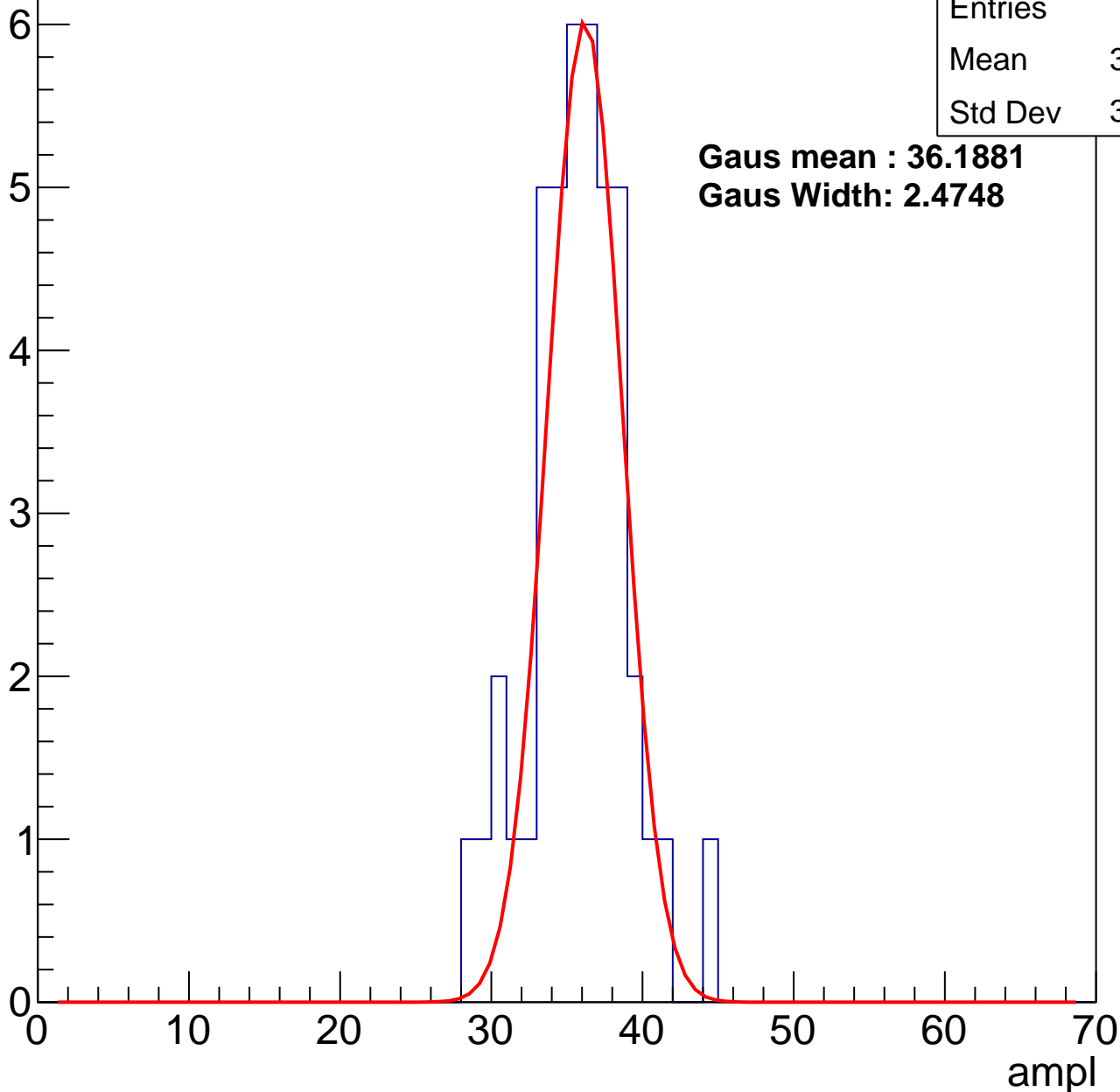
# B1L101S, U19-ch77, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	43
Mean	35.33
Std Dev	3.145

**Gaus mean : 36.1881**  
**Gaus Width: 2.4748**



# B1L101S, U19-ch77, adc2

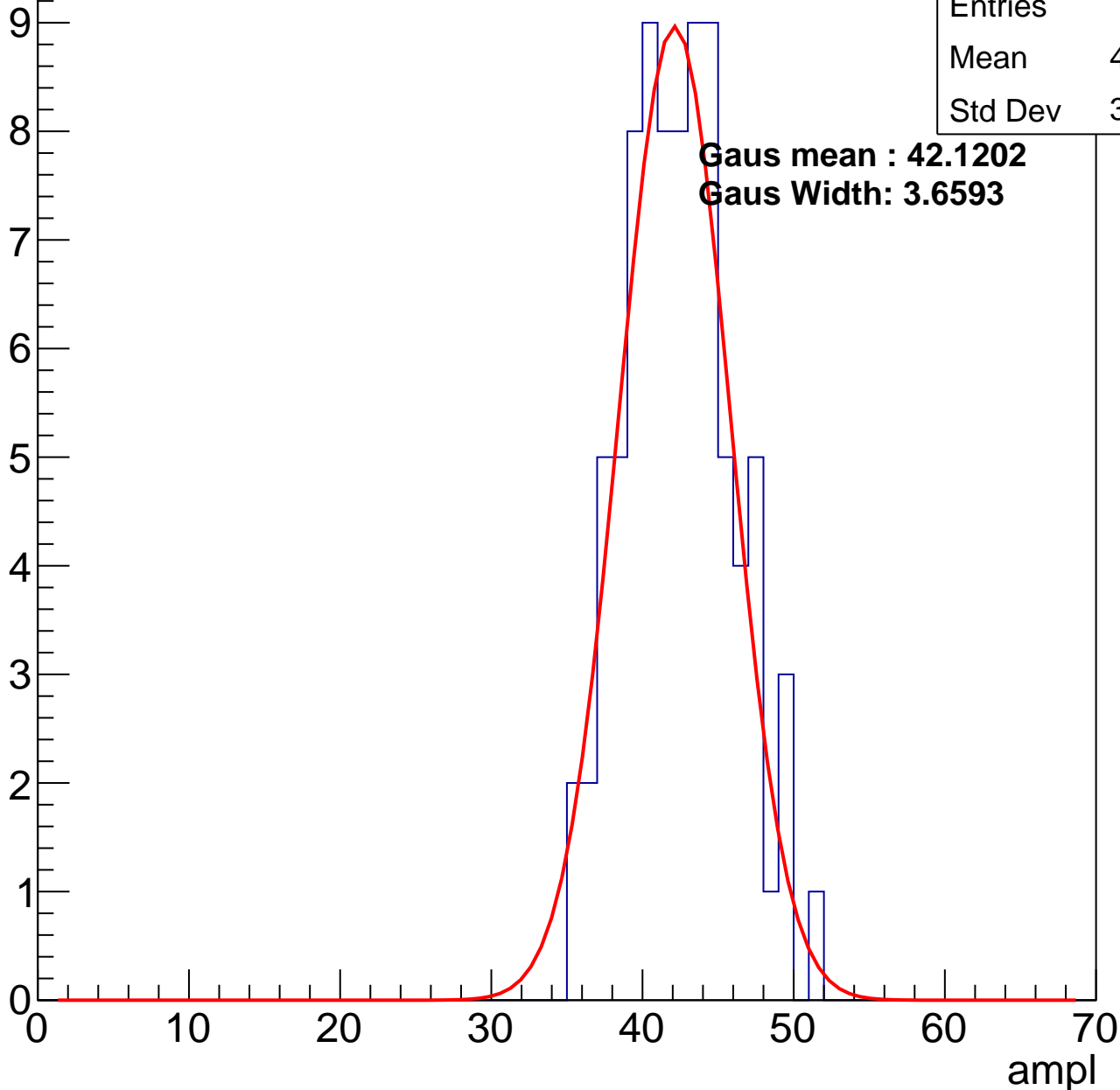
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	84
Mean	41.98
Std Dev	3.508

**Gaus mean : 42.1202**

**Gaus Width: 3.6593**

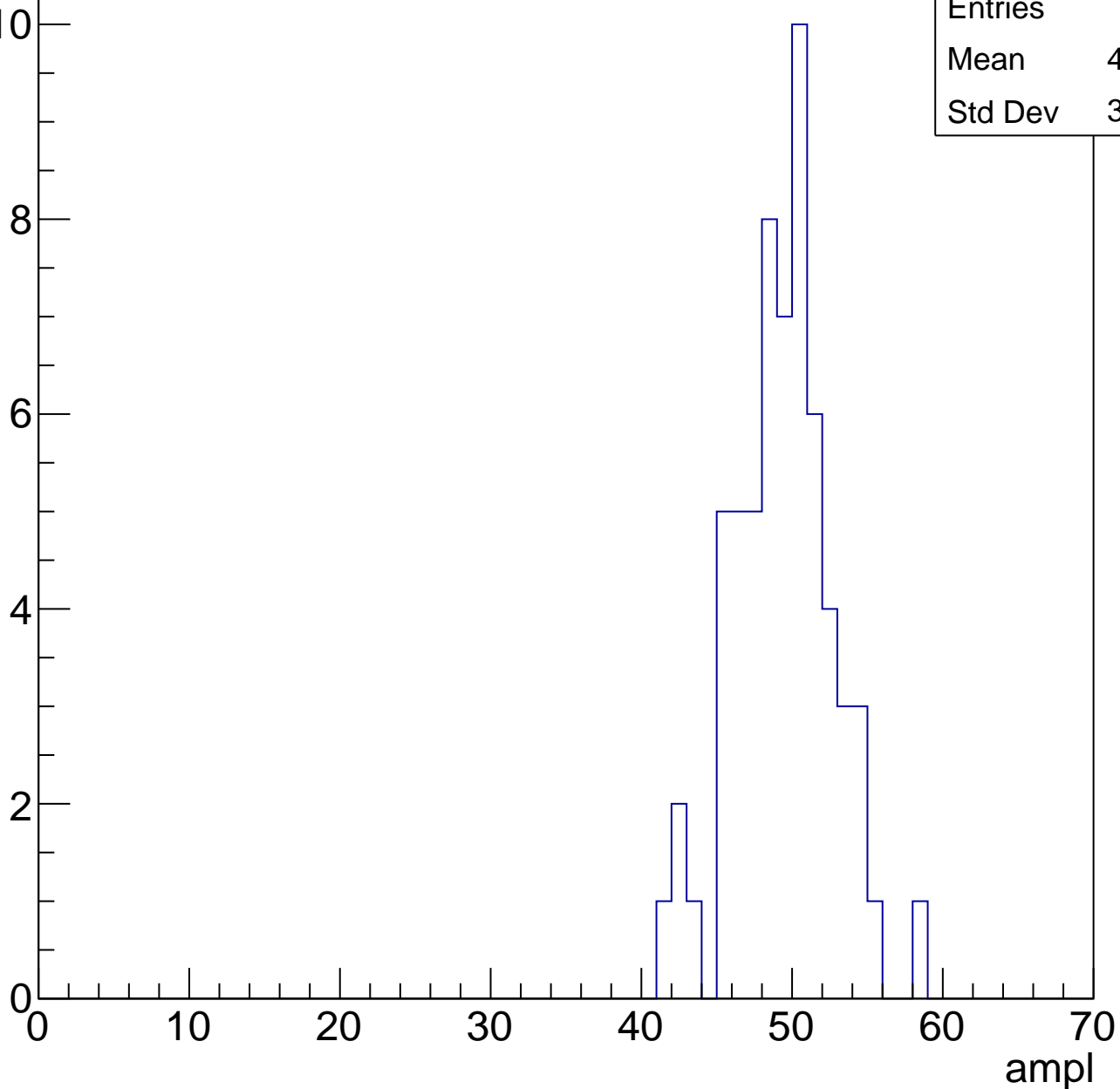


# B1L101S, U19-ch77, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	48.92
Std Dev	3.264

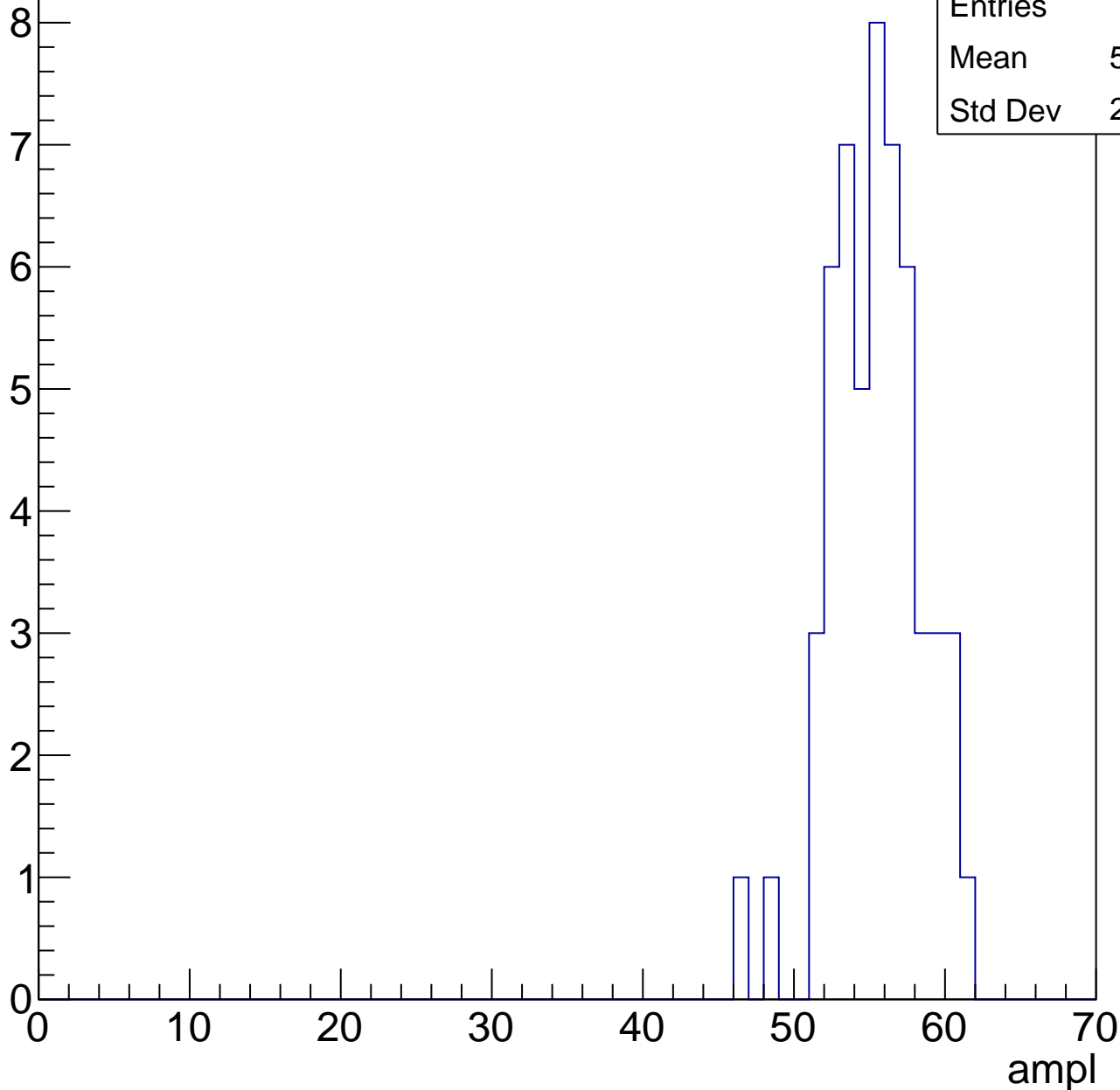


# B1L101S, U19-ch77, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	54
Mean	54.93
Std Dev	2.987



# B1L101S, U19-ch77, adc5

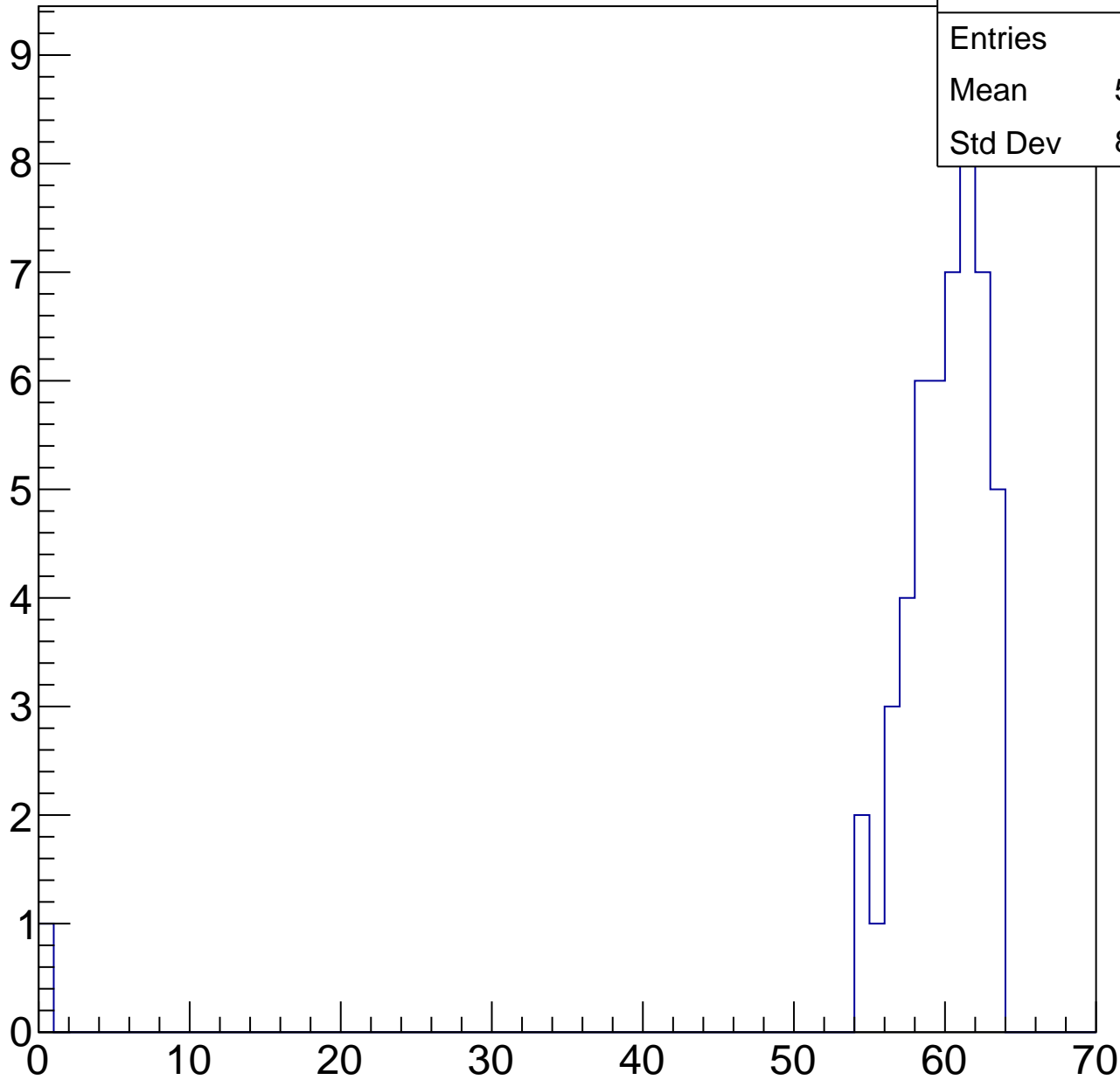
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	51
Mean	58.41
Std Dev	8.591

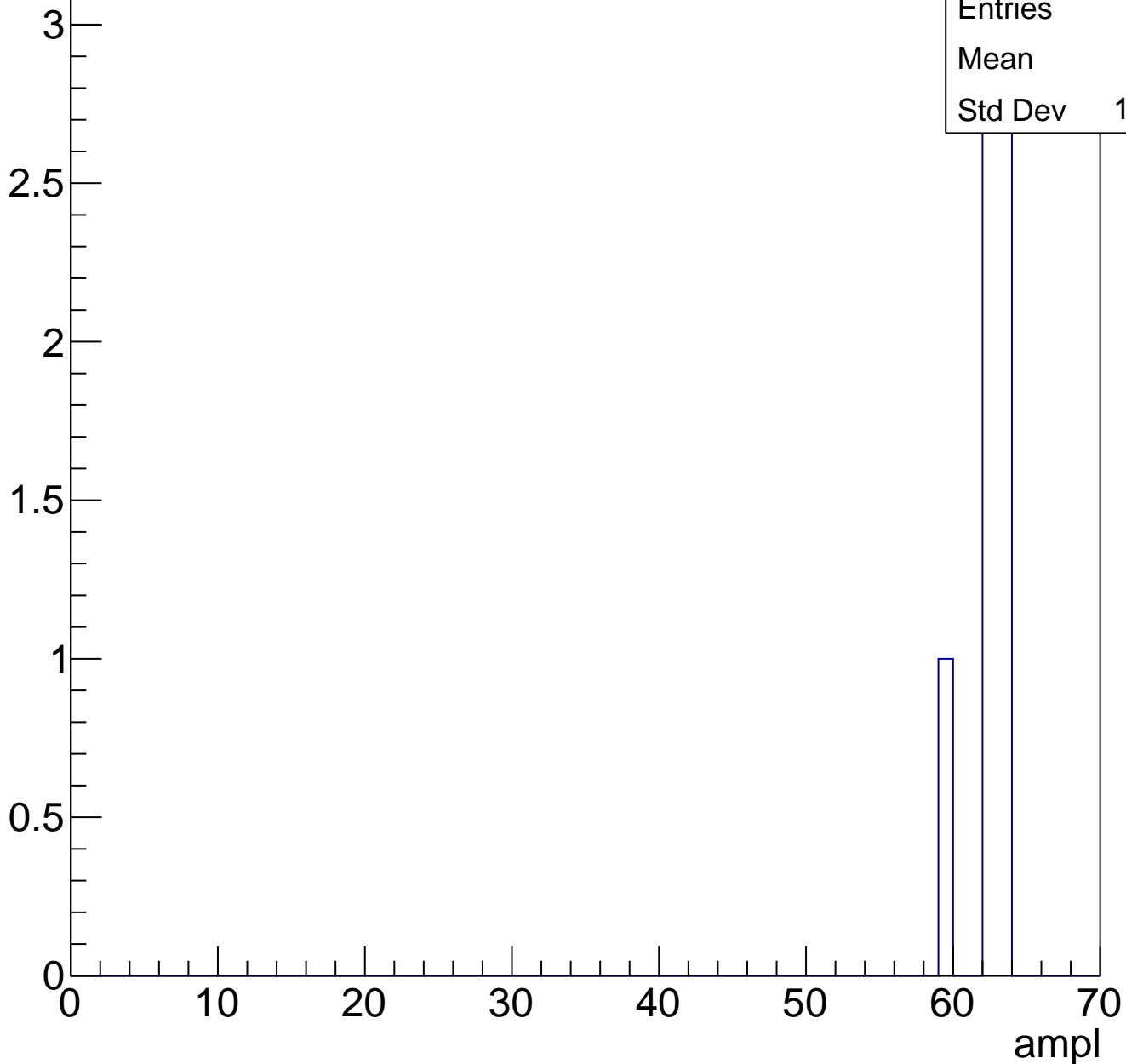
ampl



# B1L101S, U19-ch77, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

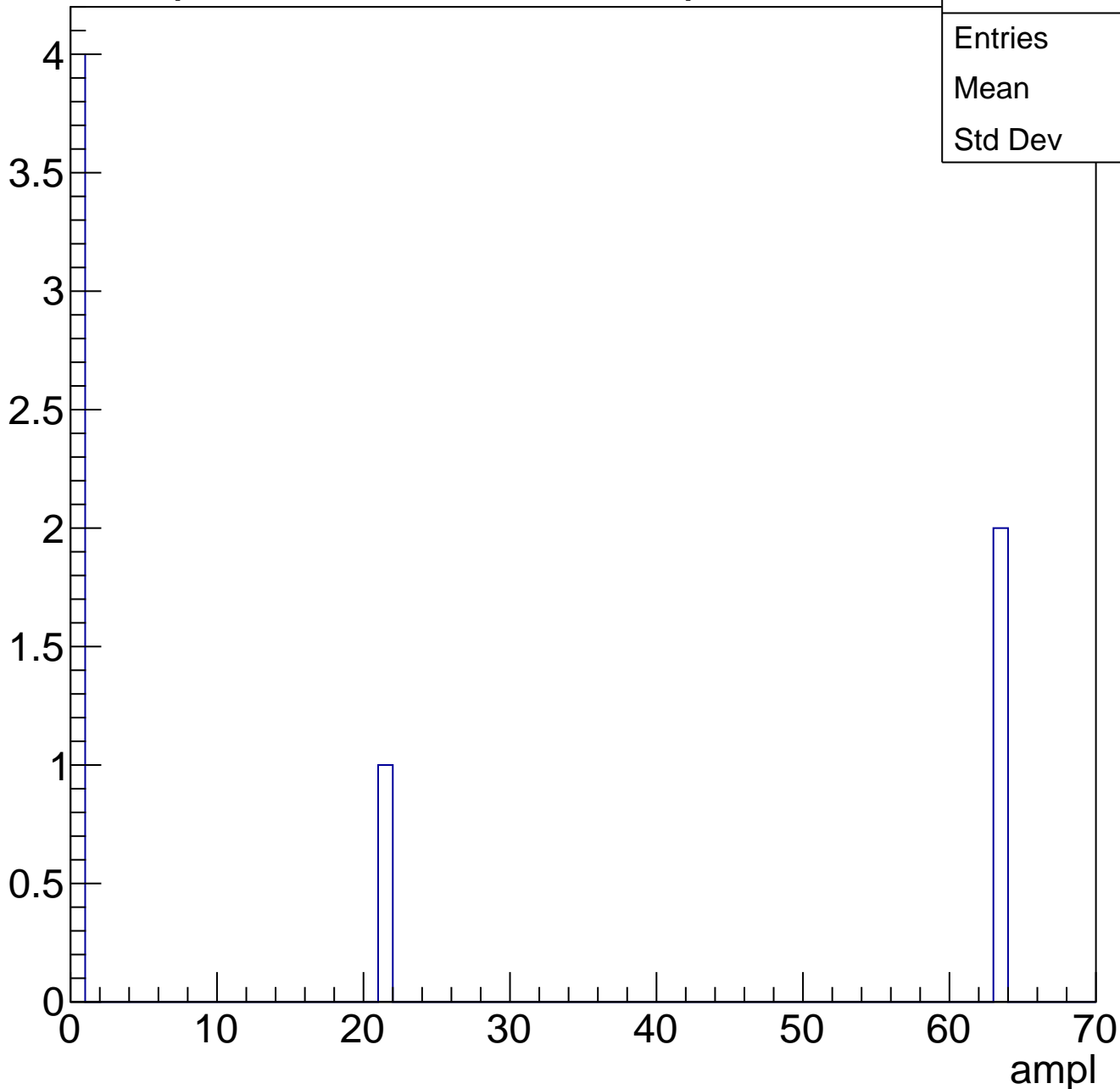




# B1L101S, U19-ch77, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	7
Mean	21
Std Dev	27.5

# B1L101S, U19-ch78, adc0

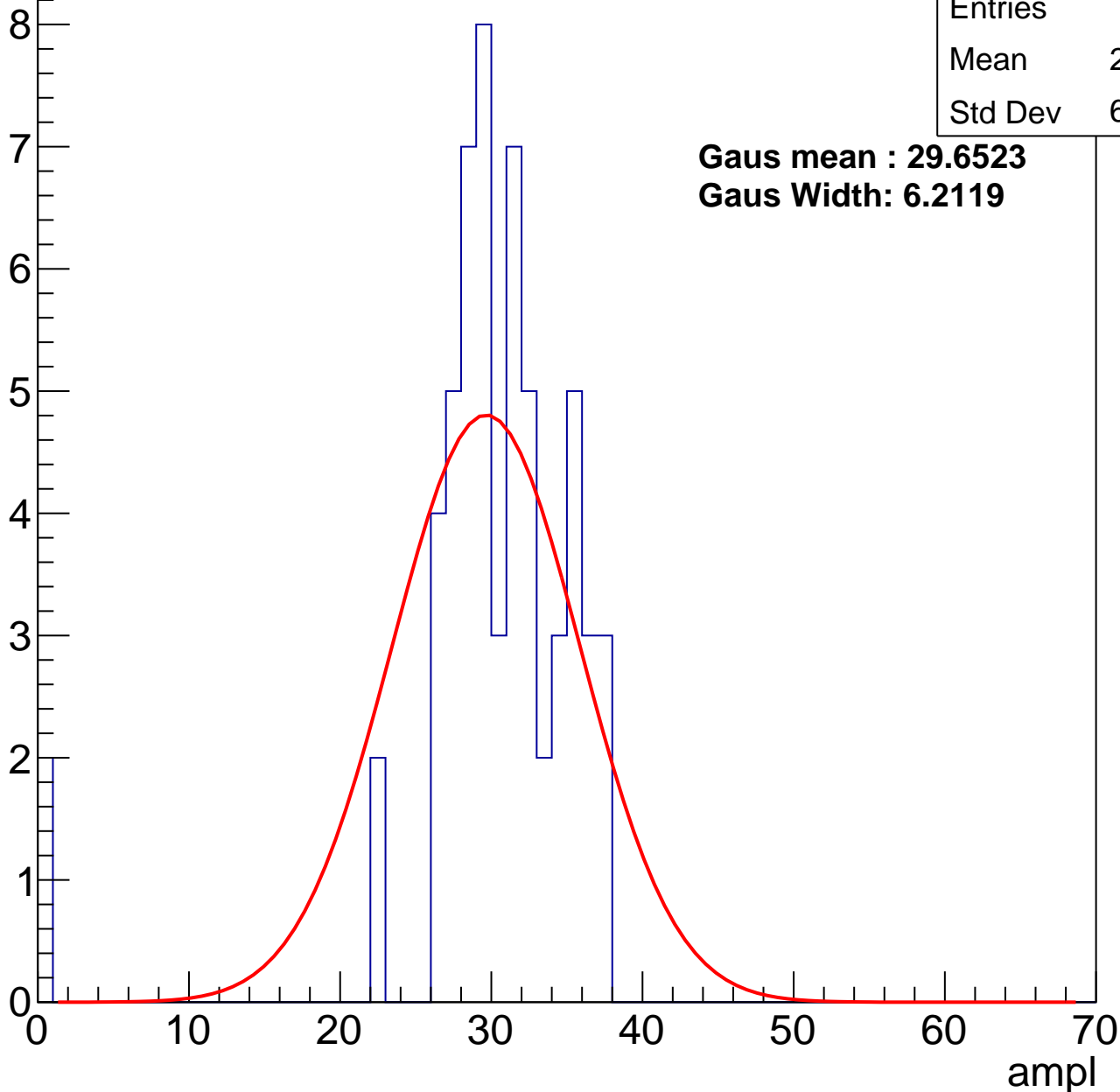
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	59
Mean	29.49
Std Dev	6.549

**Gaus mean : 29.6523**

**Gaus Width: 6.2119**



# B1L101S, U19-ch78, adc1

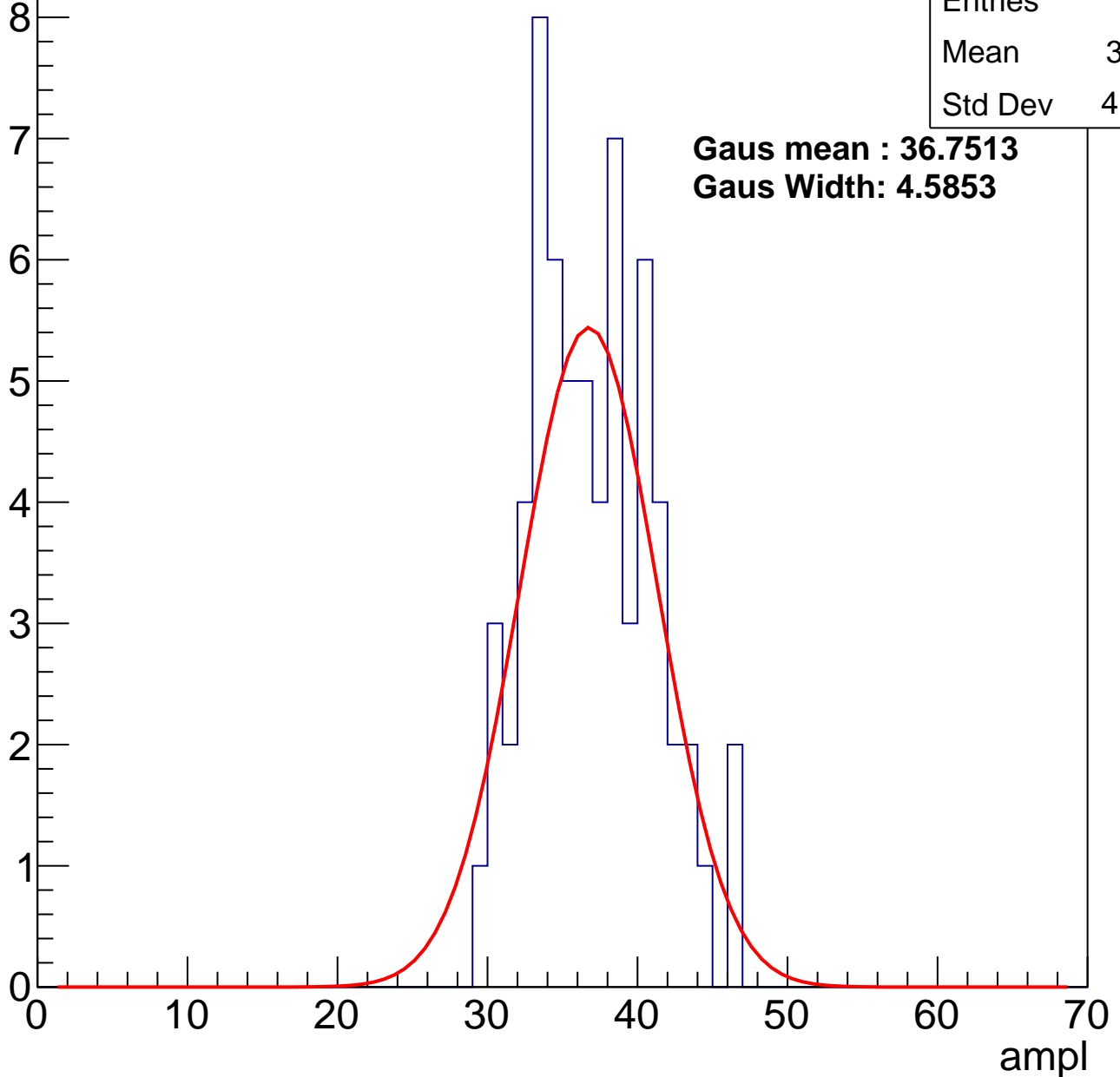
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	36.51
Std Dev	4.008

**Gaus mean : 36.7513**

**Gaus Width: 4.5853**



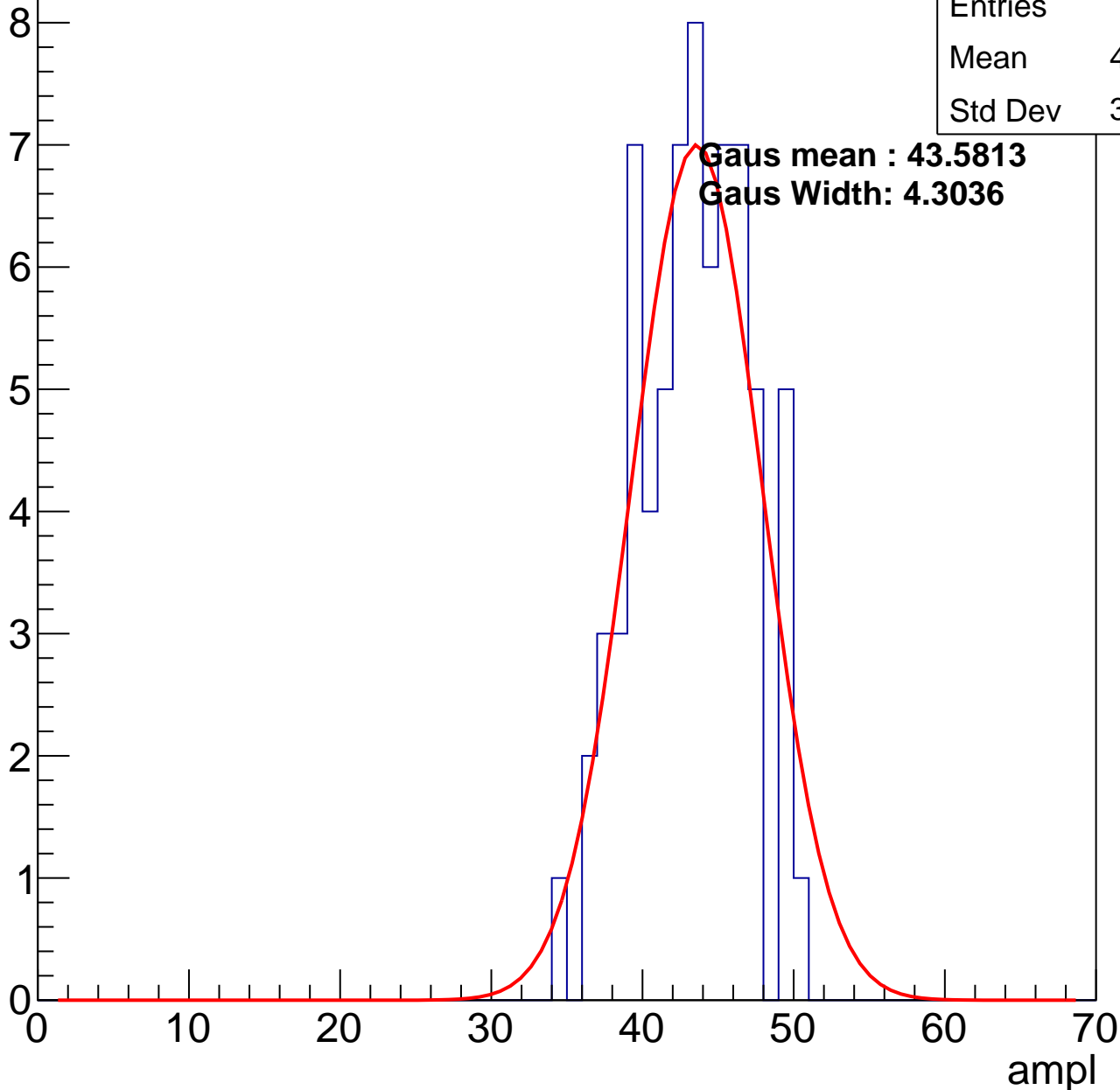
# B1L101S, U19-ch78, adc2

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	71
Mean	42.79
Std Dev	3.638

**Gaus mean : 43.5813**  
**Gaus Width: 4.3036**

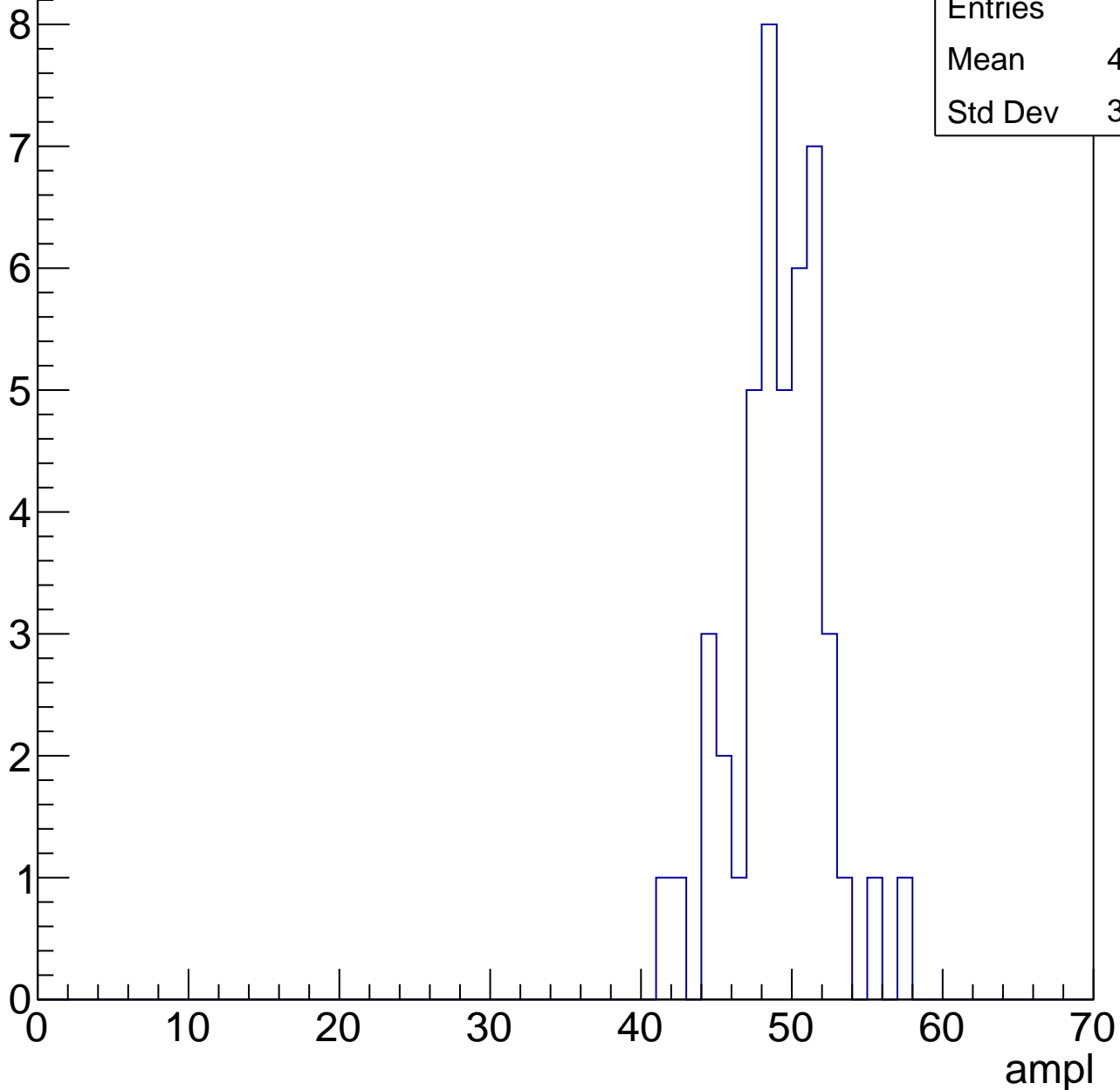


# B1L101S, U19-ch78, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	45
Mean	48.73
Std Dev	3.094



# B1L101S, U19-ch78, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

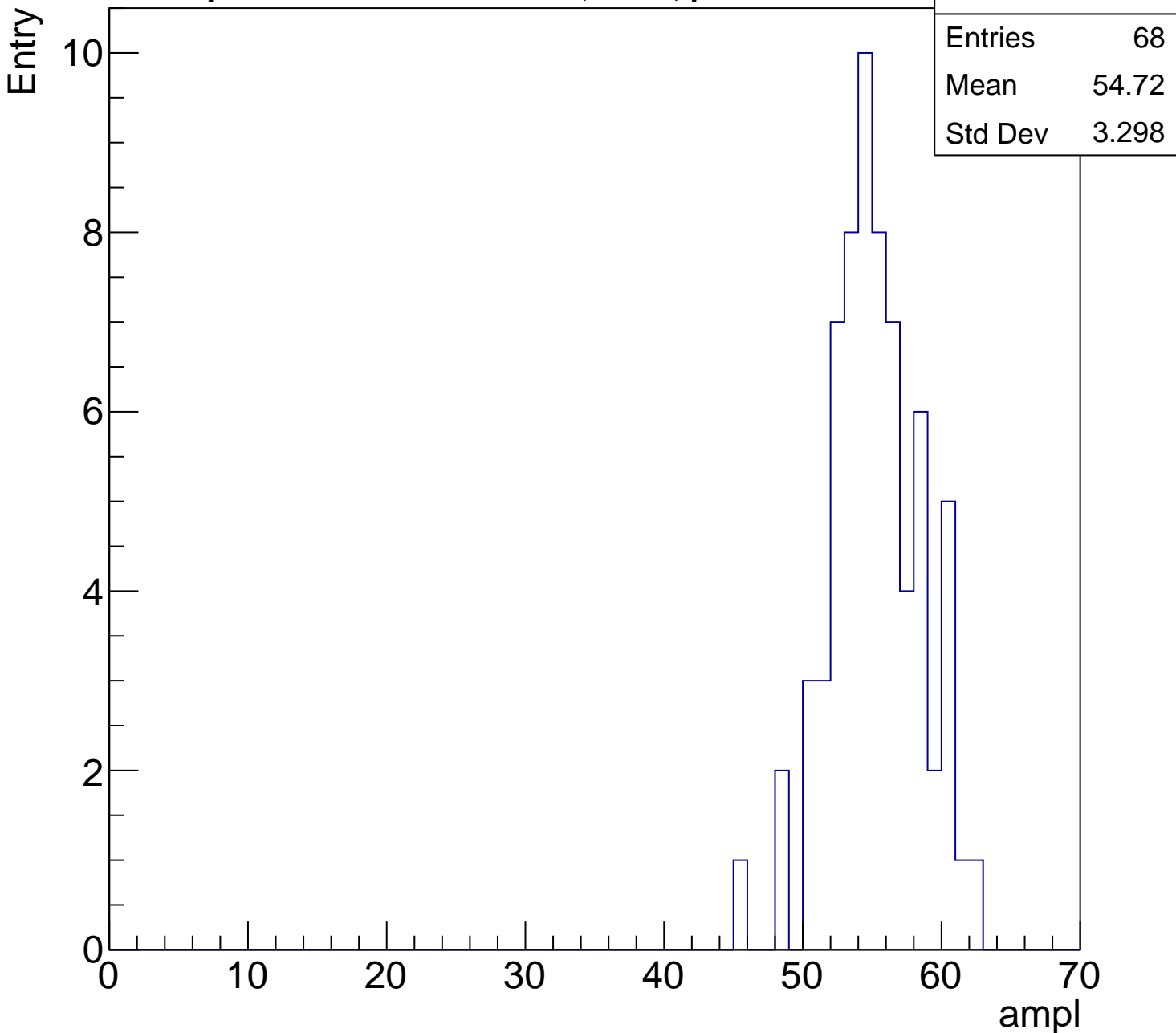
Entries	68
Mean	54.72
Std Dev	3.298

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B1L101S, U19-ch78, adc5

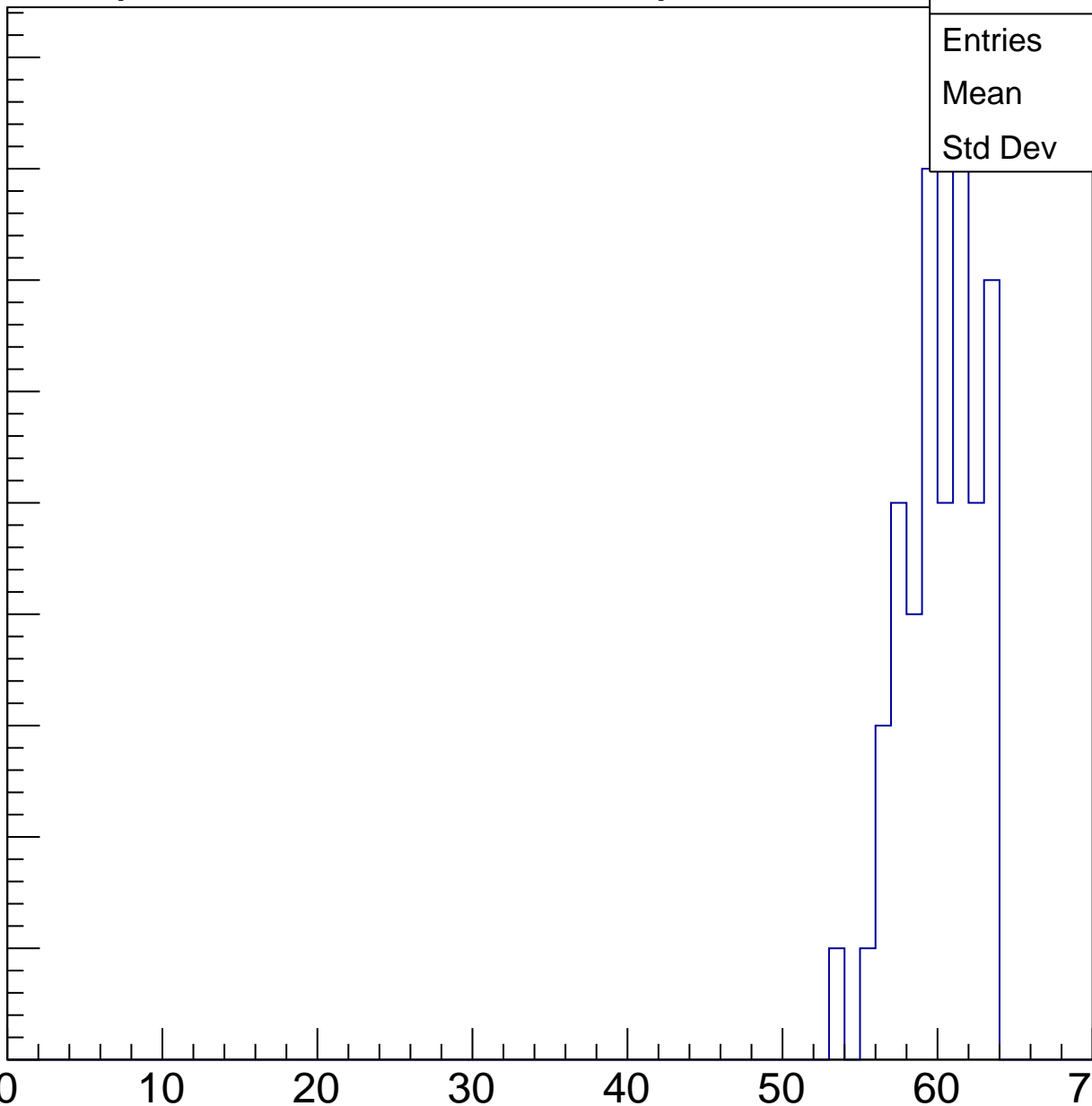
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	48
Mean	59.69
Std Dev	2.408

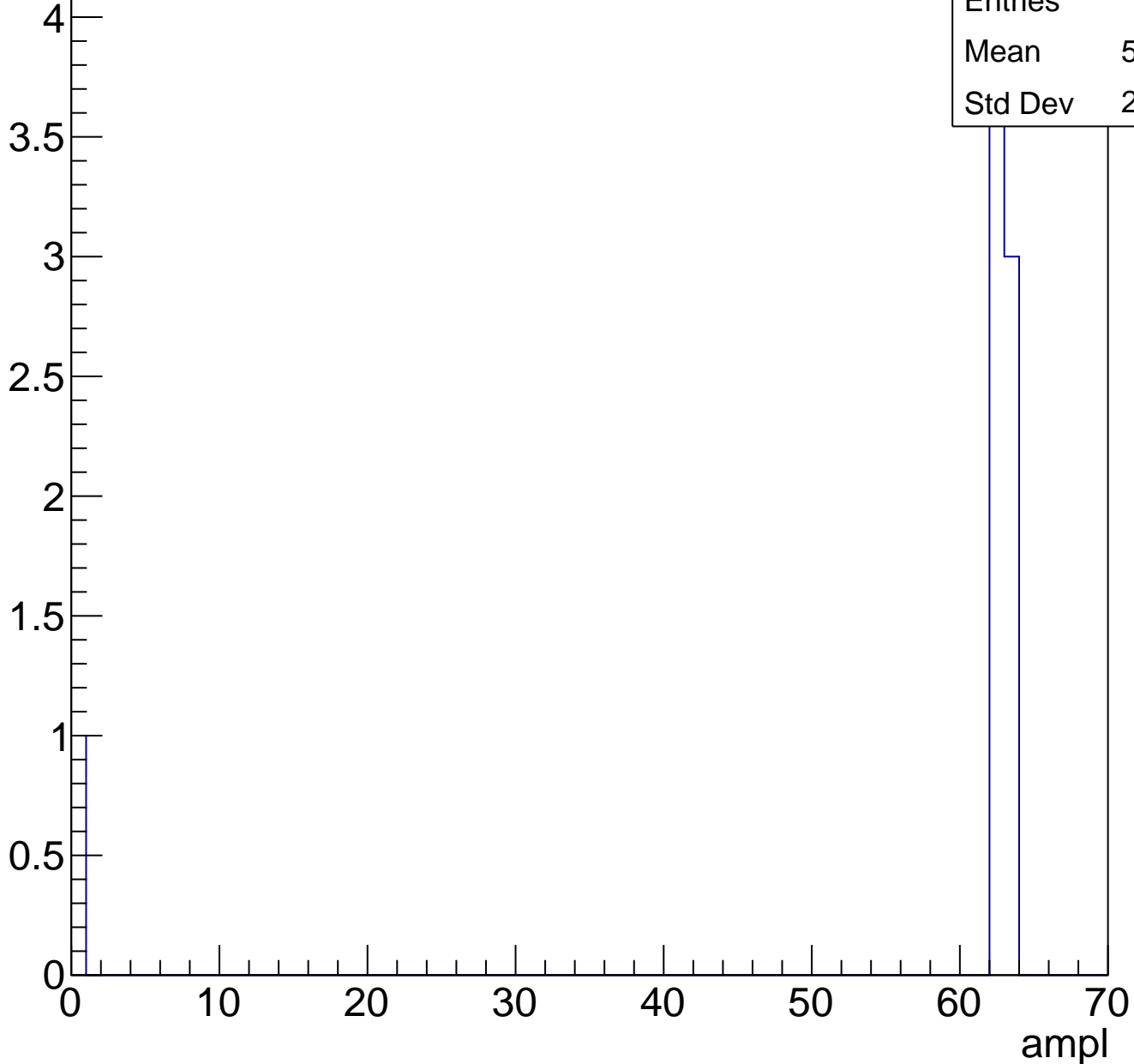
ampl



# B1L101S, U19-ch78, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	8
Mean	54.62
Std Dev	20.65



# B1L101S, U19-ch78, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L101S, U19-ch79, adc0

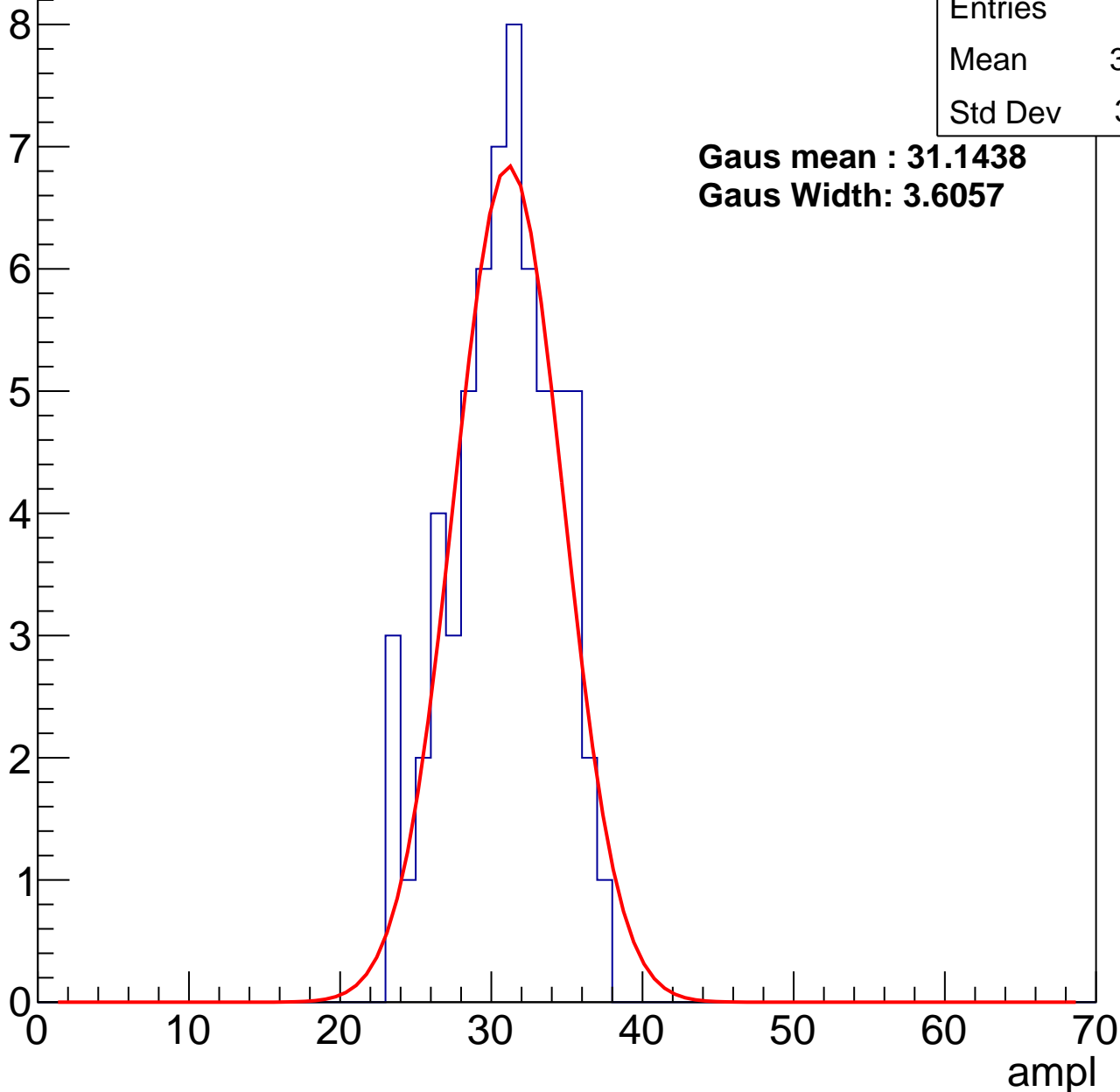
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	30.33
Std Dev	3.441

**Gaus mean : 31.1438**

**Gaus Width: 3.6057**



# B1L101S, U19-ch79, adc1

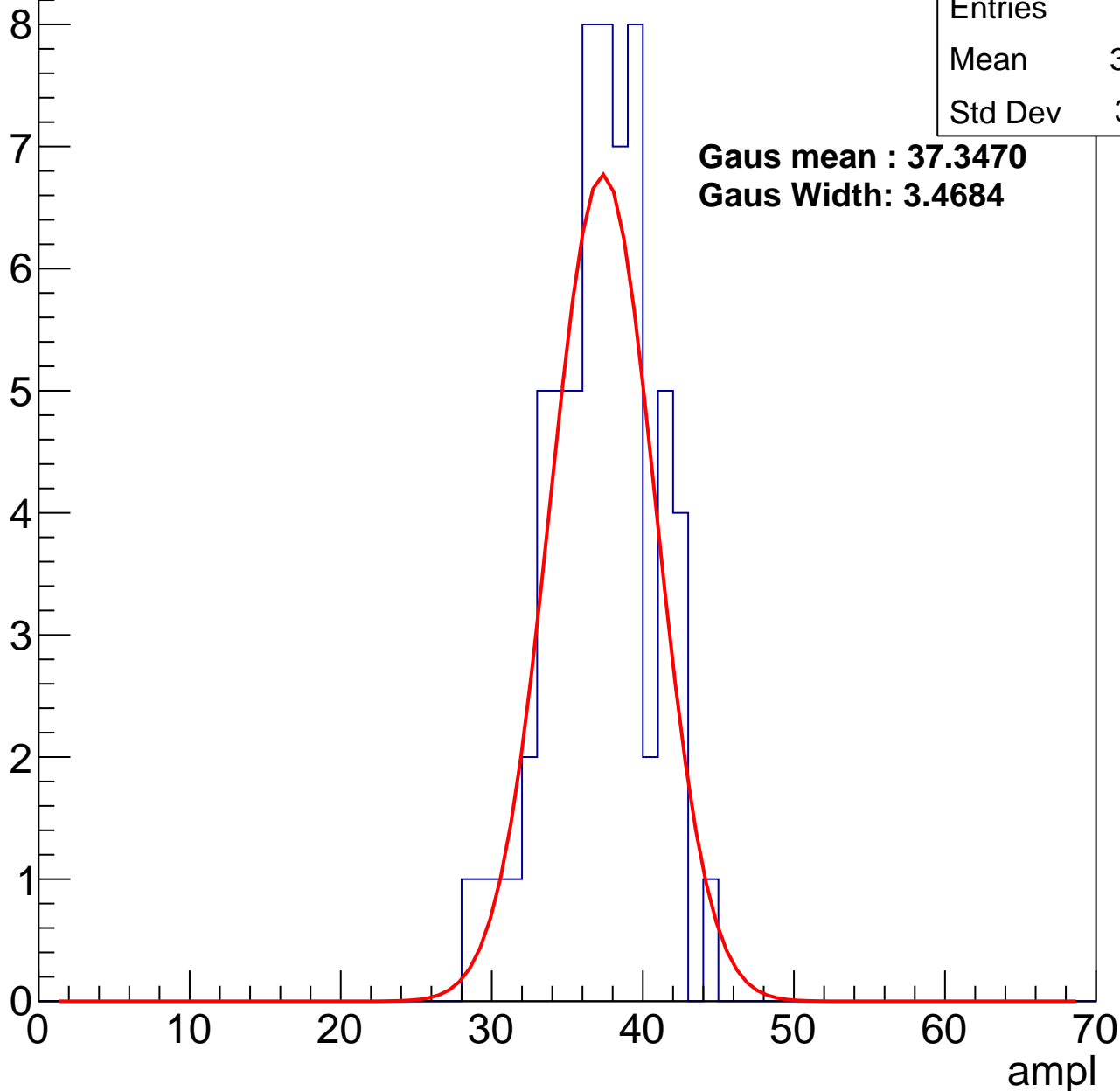
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	36.73
Std Dev	3.341

**Gaus mean : 37.3470**

**Gaus Width: 3.4684**



# B1L101S, U19-ch79, adc2

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	43.49
Std Dev	2.994

**Gaus mean : 44.1221**

**Gaus Width: 3.1677**

10

8

6

4

2

0

0

10

20

30

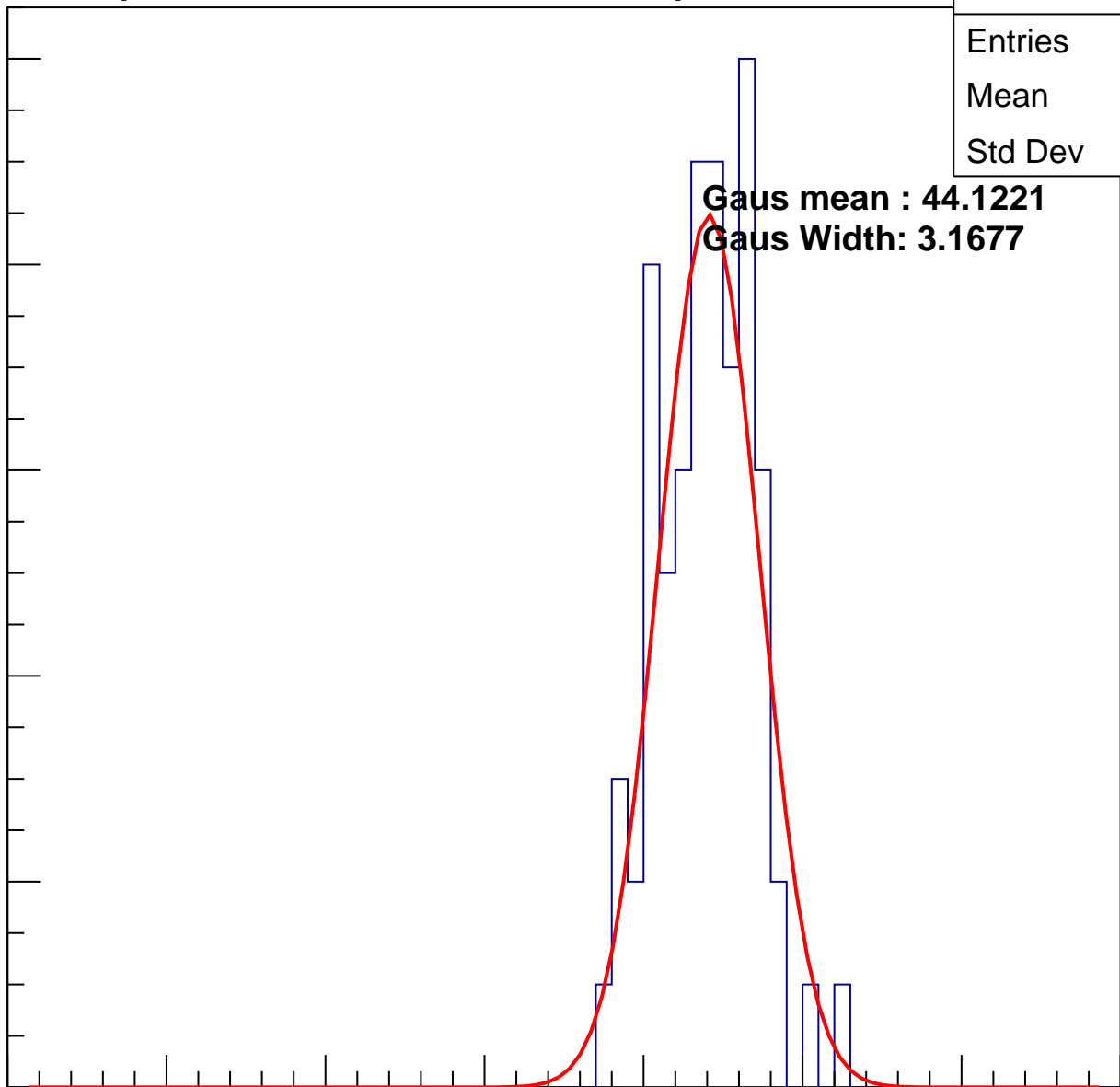
40

50

60

70

ampl

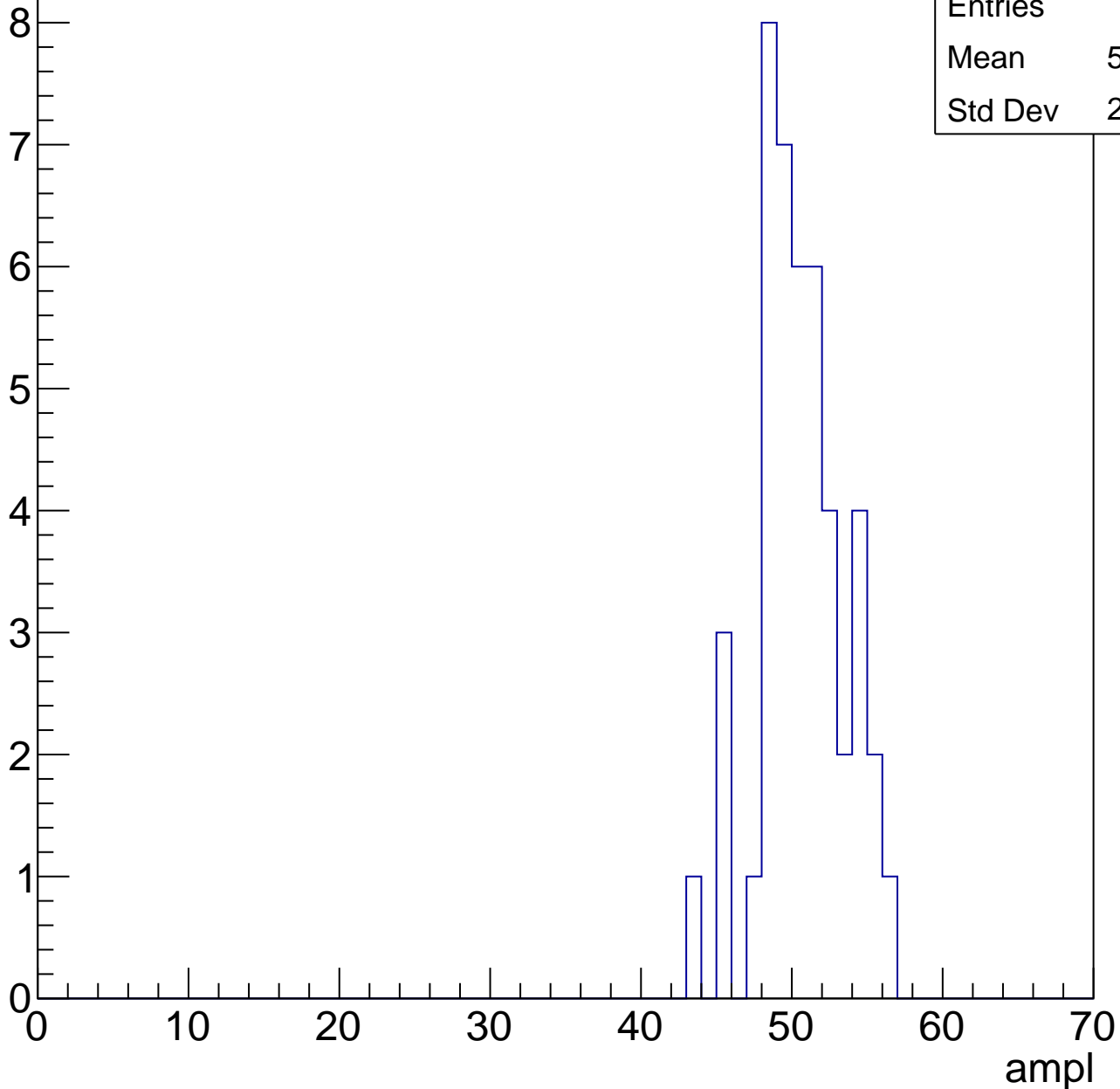


# B1L101S, U19-ch79, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

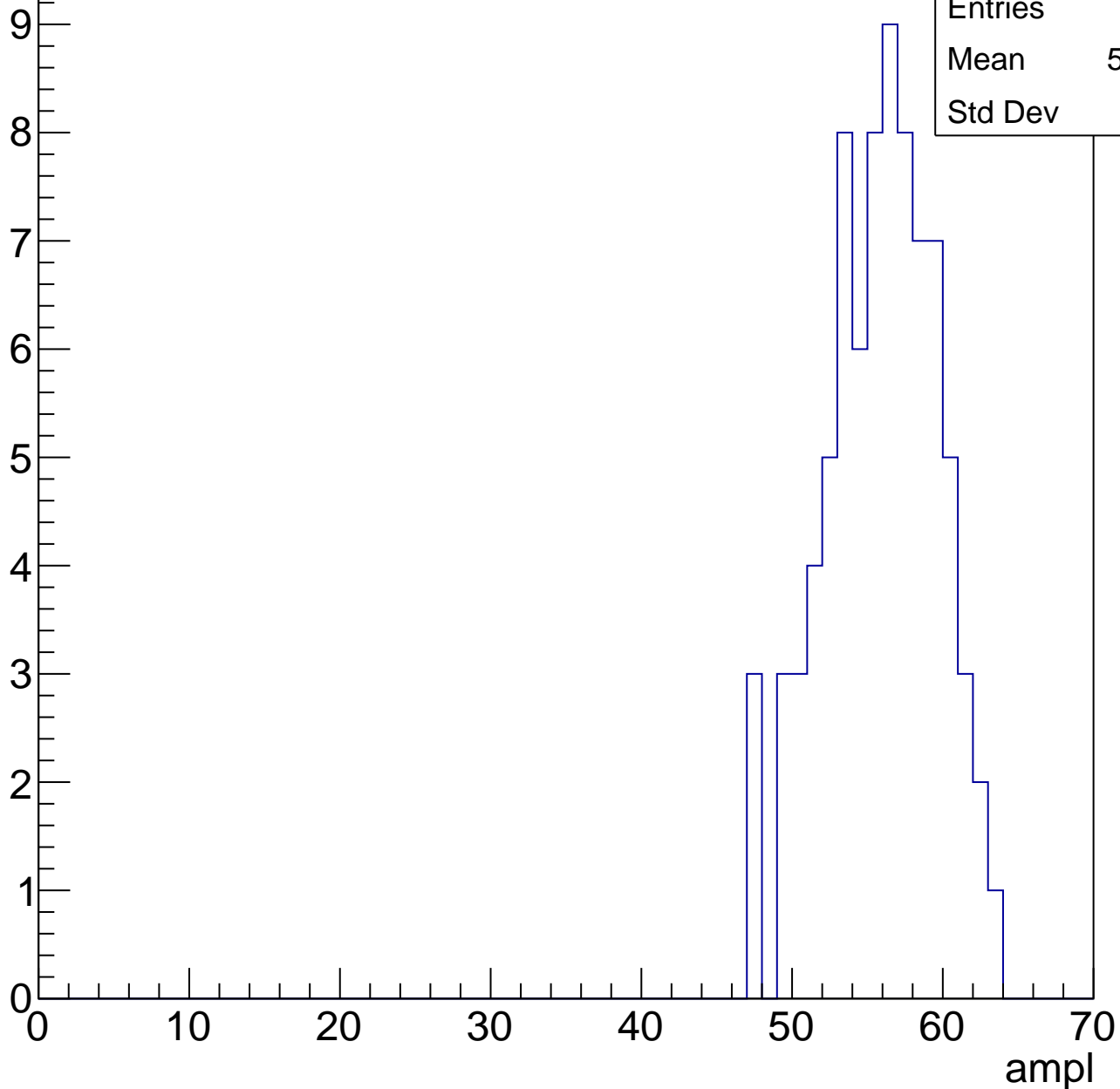
Entries	45
Mean	50.09
Std Dev	2.835



# B1L101S, U19-ch79, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

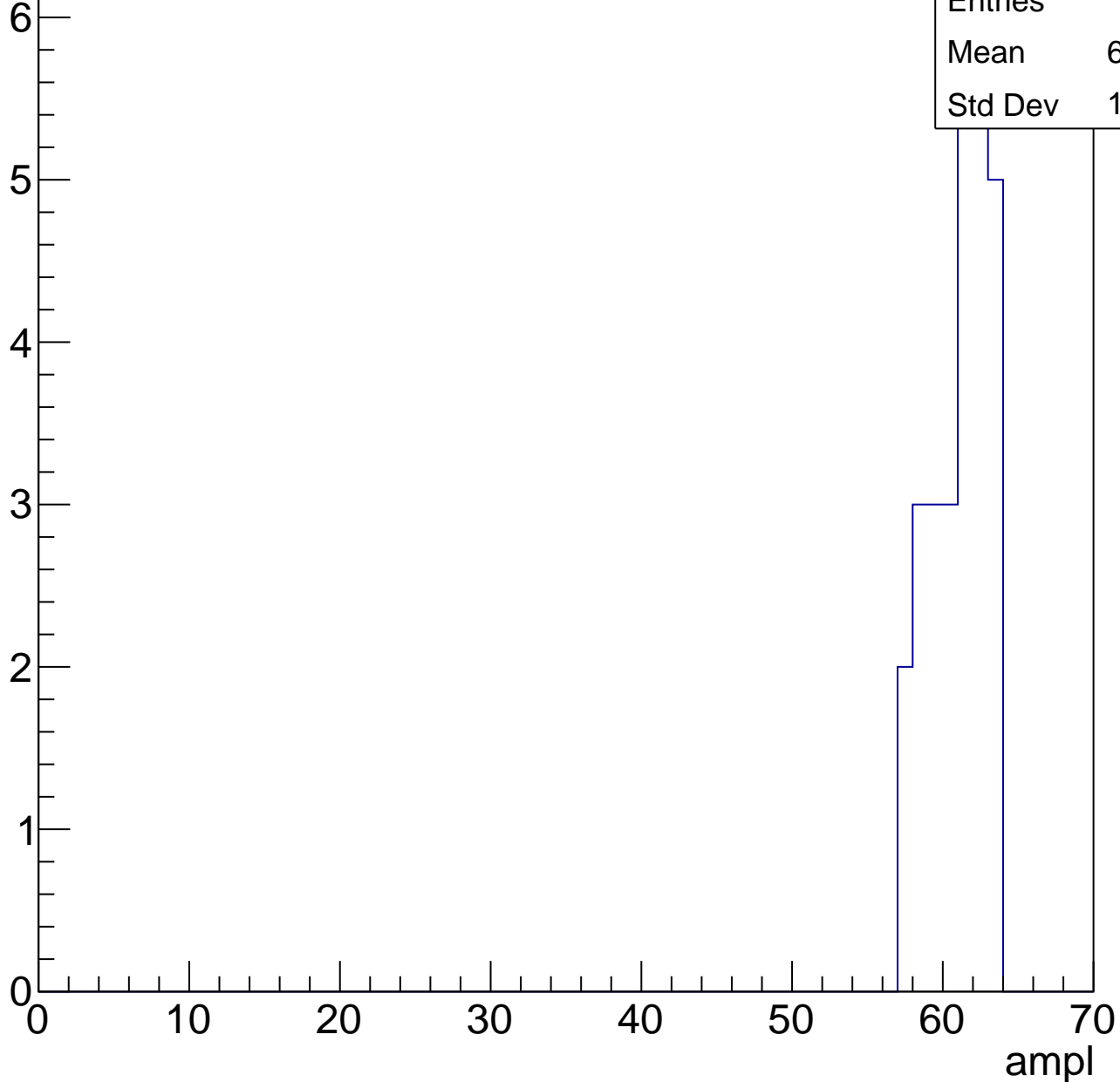


Entries	82
Mean	55.35
Std Dev	3.7

# B1L101S, U19-ch79, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

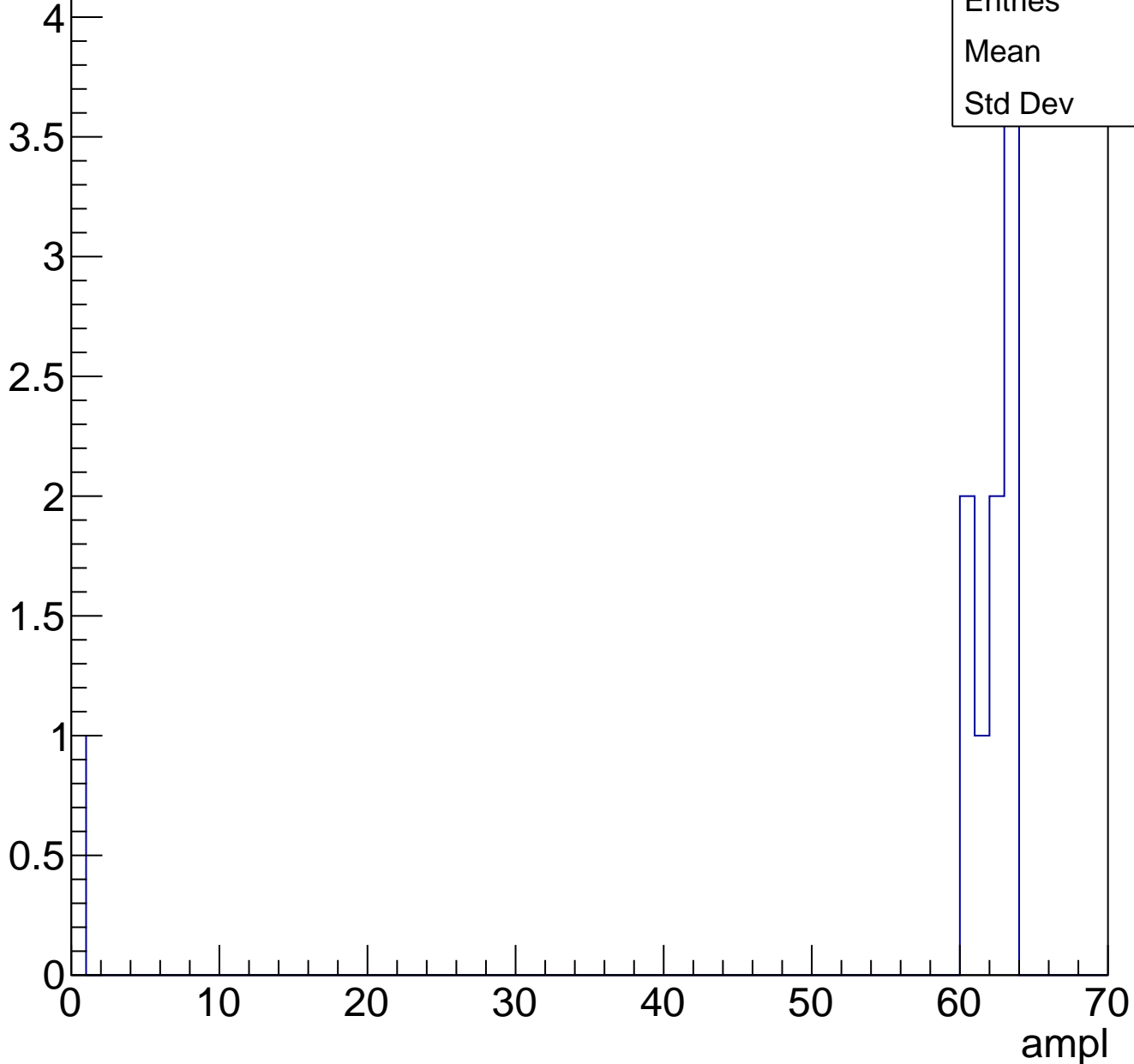
Entry



# B1L101S, U19-ch79, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U19-ch79, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L101S, U19-ch80, adc0

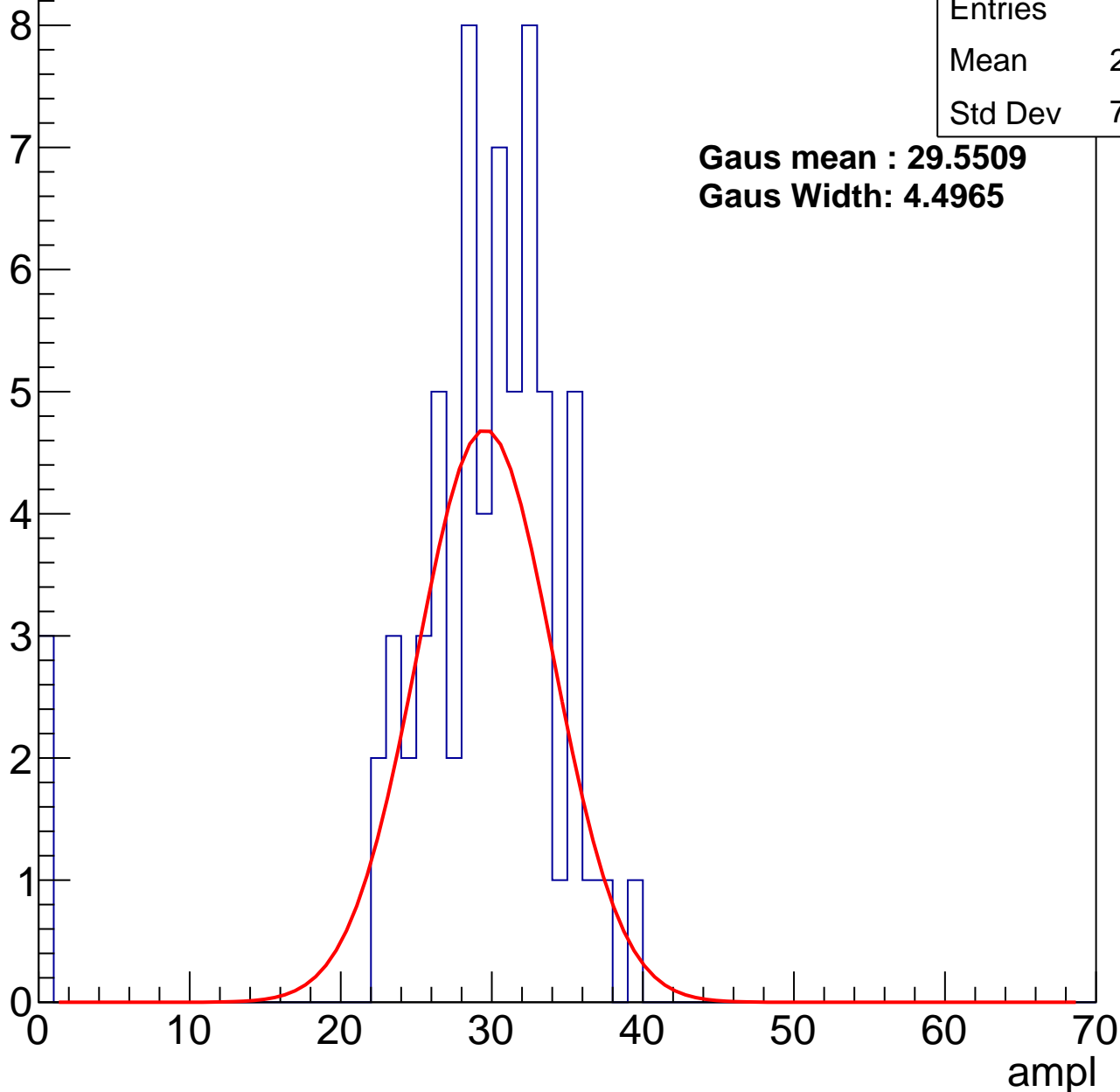
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	66
Mean	28.29
Std Dev	7.232

**Gaus mean : 29.5509**

**Gaus Width: 4.4965**



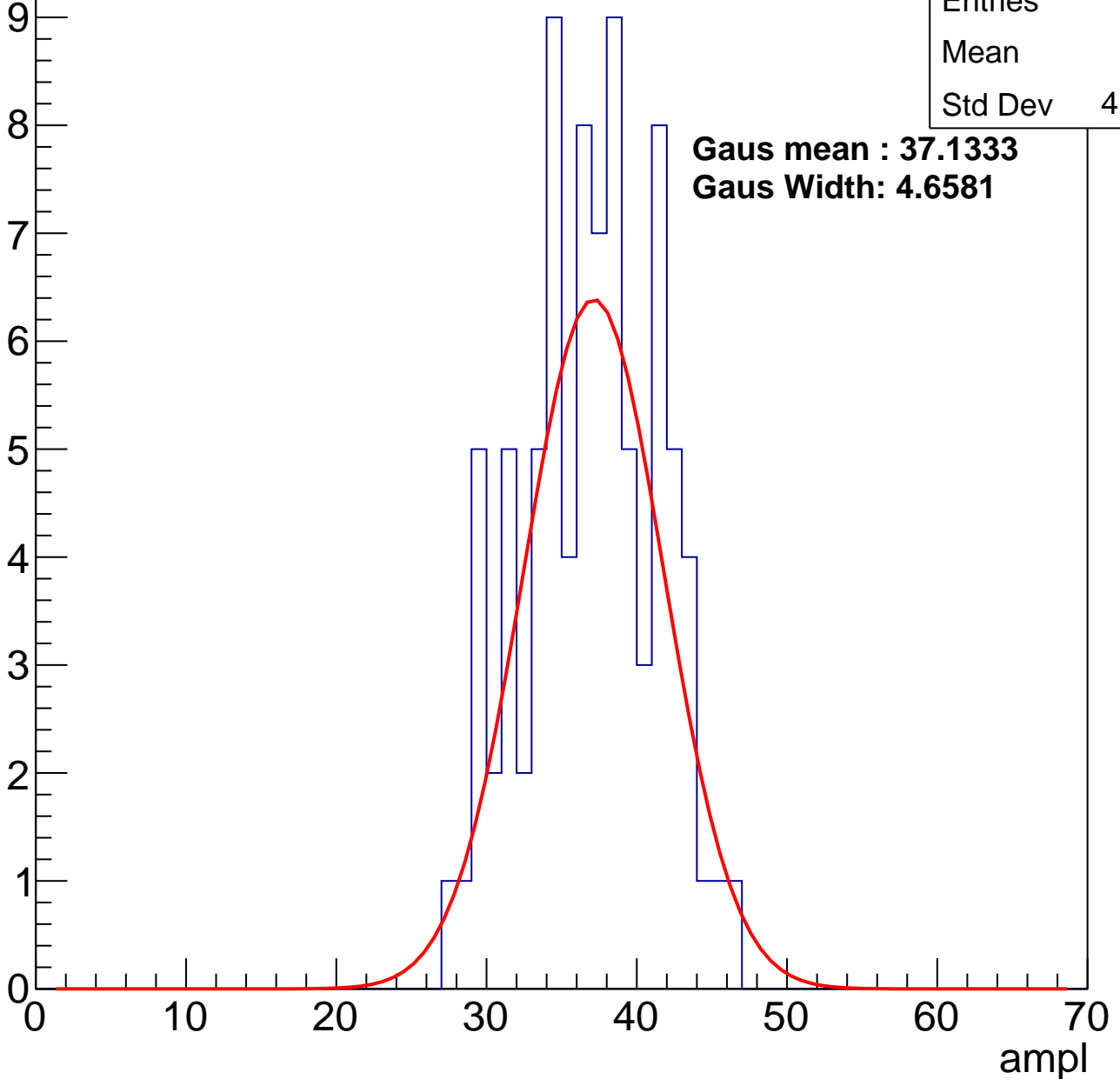
# B1L101S, U19-ch80, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	86
Mean	36.5
Std Dev	4.366

**Gaus mean : 37.1333**  
**Gaus Width: 4.6581**



# B1L101S, U19-ch80, adc2

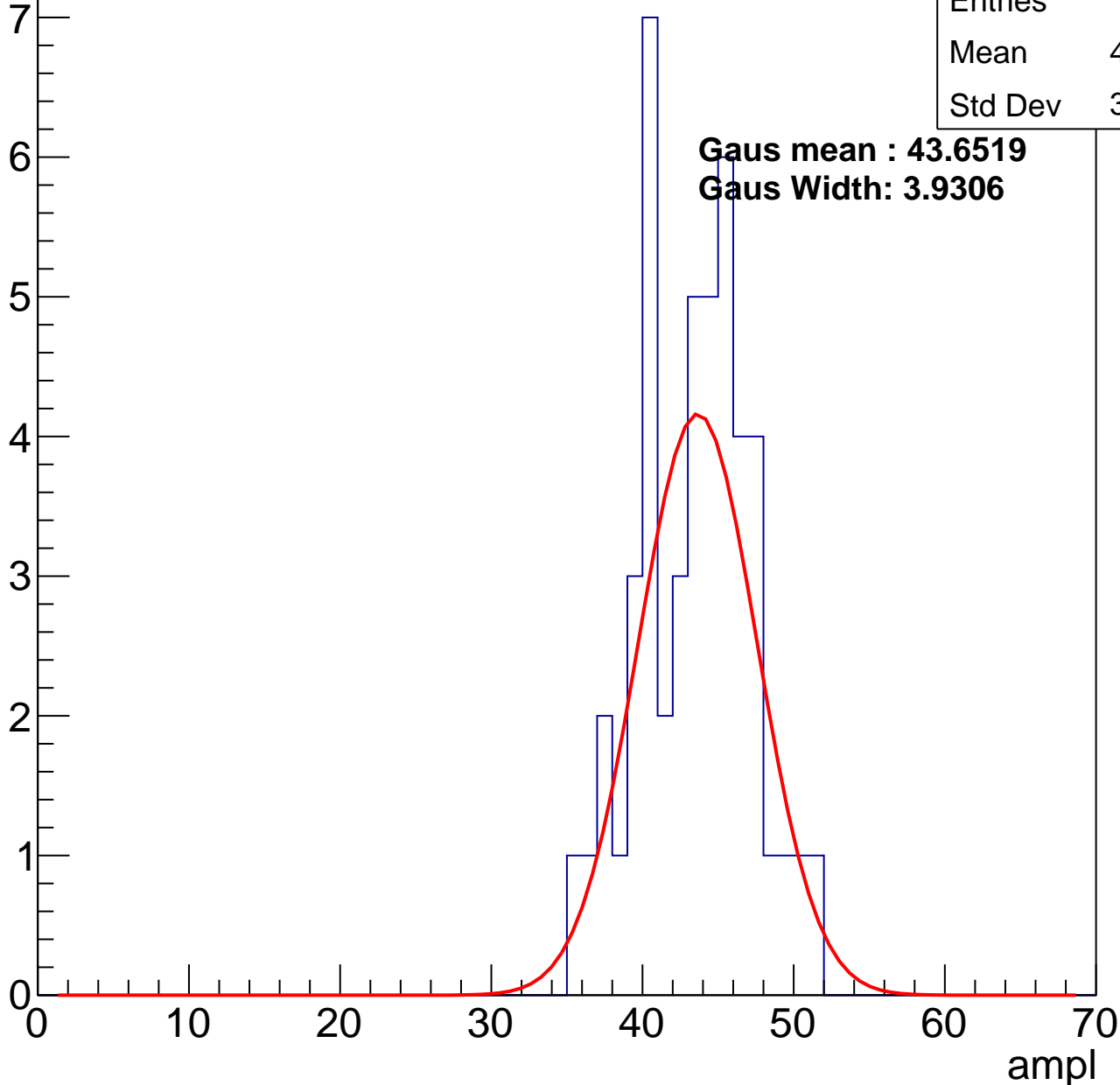
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	48
Mean	42.98
Std Dev	3.637

**Gaus mean : 43.6519**

**Gaus Width: 3.9306**

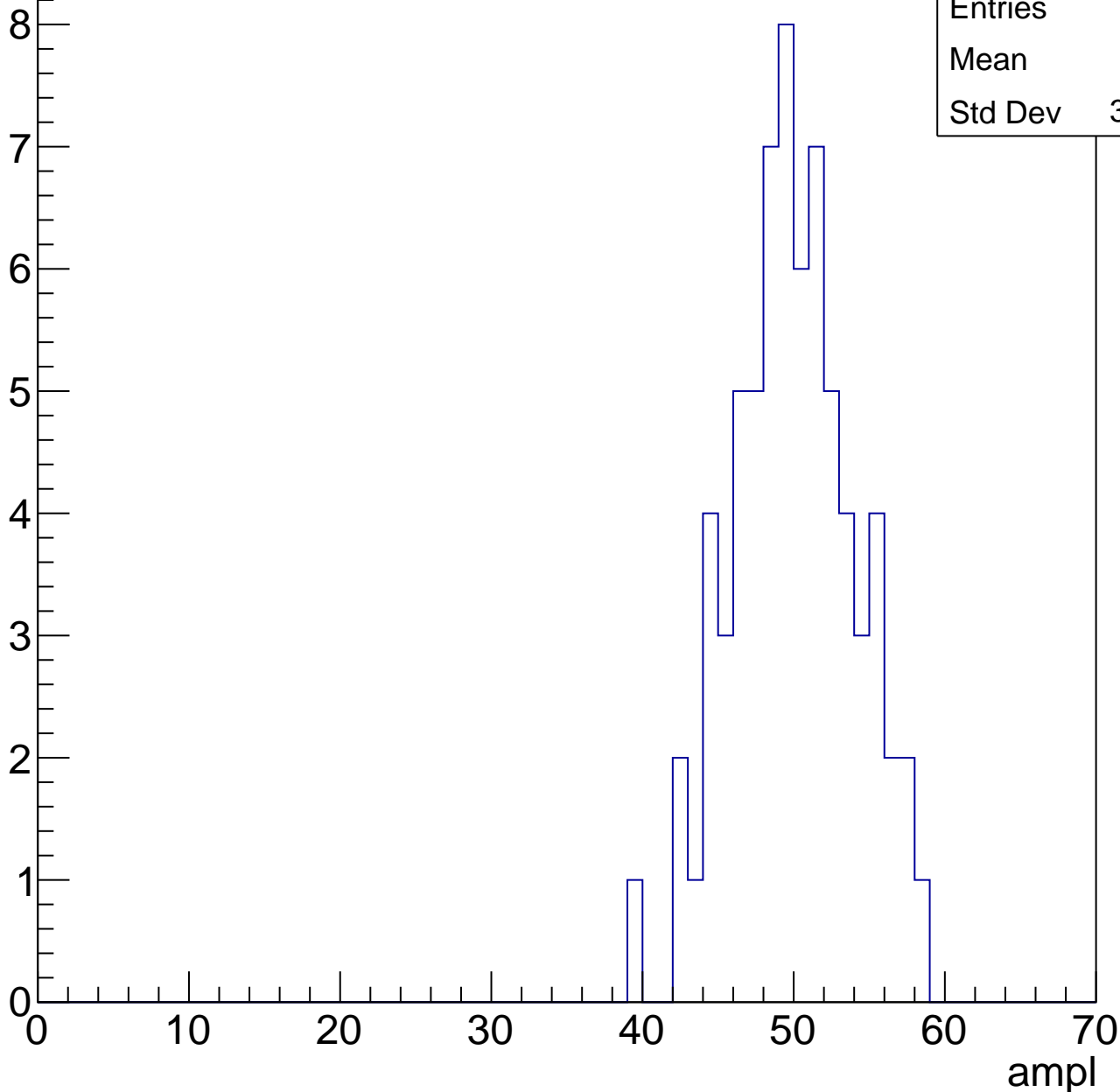


# B1L101S, U19-ch80, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	49.5
Std Dev	3.974

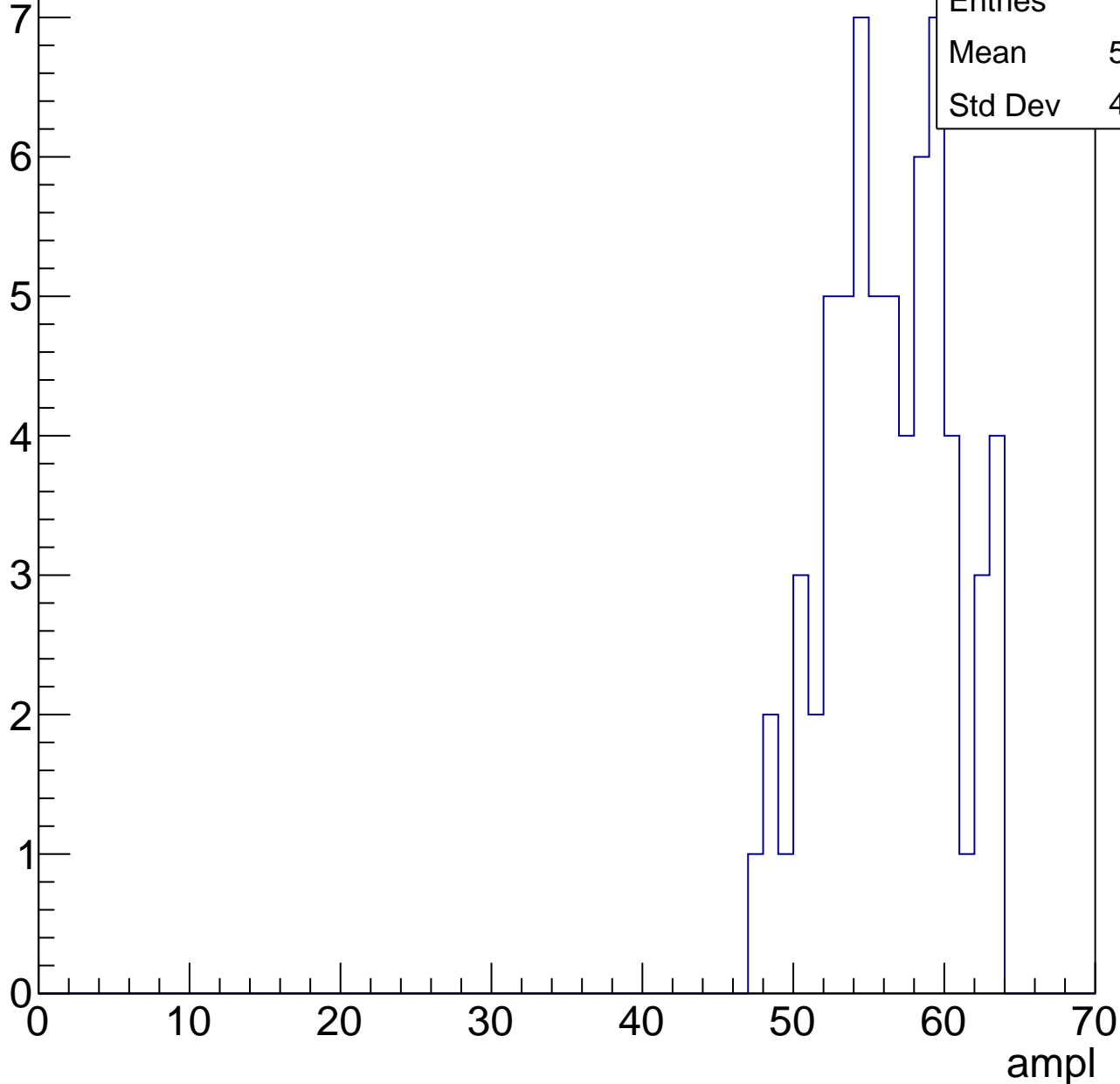


# B1L101S, U19-ch80, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

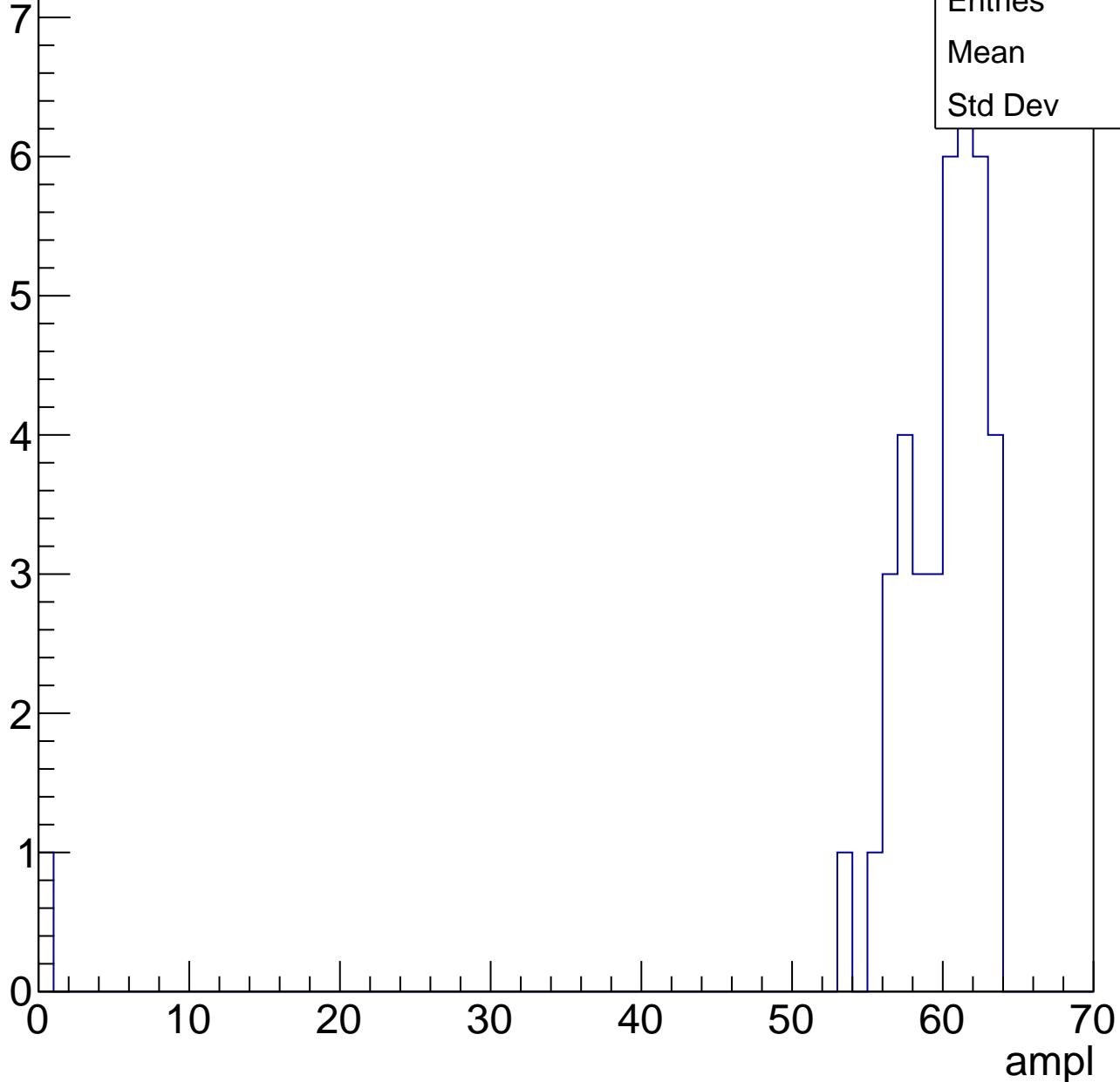
Entries	65
Mean	55.85
Std Dev	4.032



# B1L101S, U19-ch80, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U19-ch80, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	4
Mean	62
Std Dev	1

ampl



# B1L101S, U19-ch80, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U19-ch81, adc0

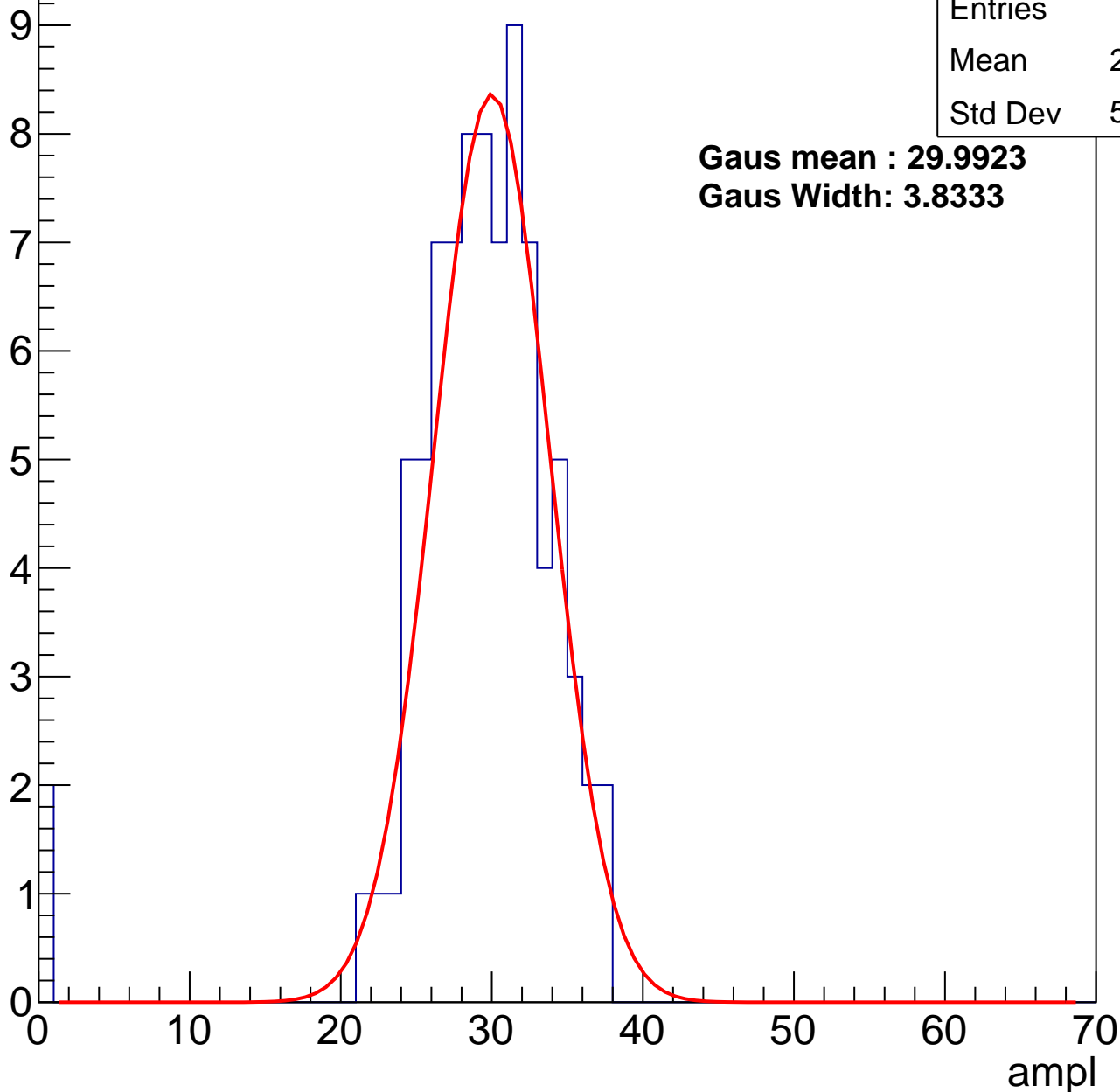
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	84
Mean	28.62
Std Dev	5.724

**Gaus mean : 29.9923**

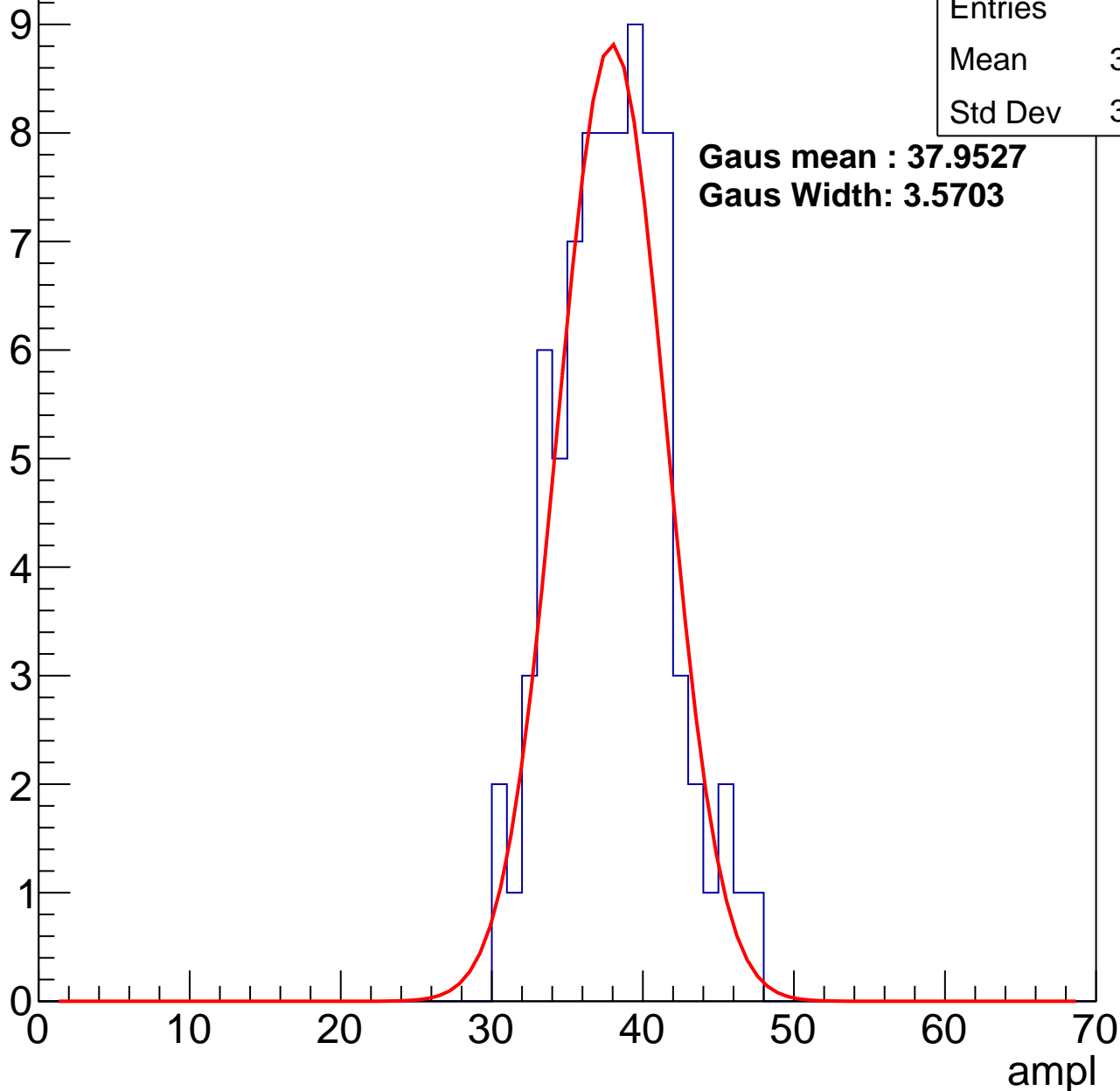
**Gaus Width: 3.8333**



# B1L101S, U19-ch81, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U19-ch81, adc2

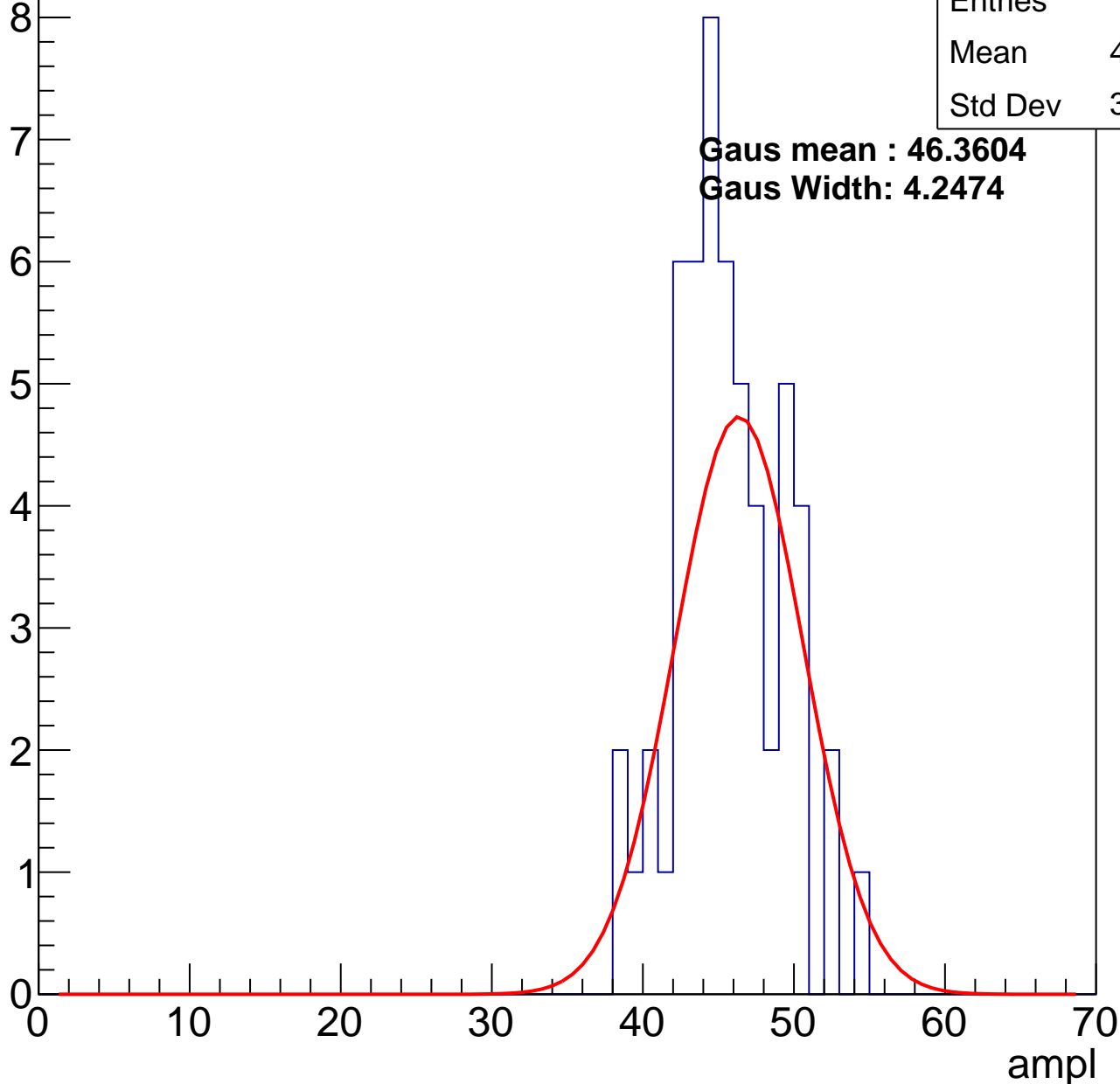
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	55
Mean	45.18
Std Dev	3.522

**Gaus mean : 46.3604**

**Gaus Width: 4.2474**

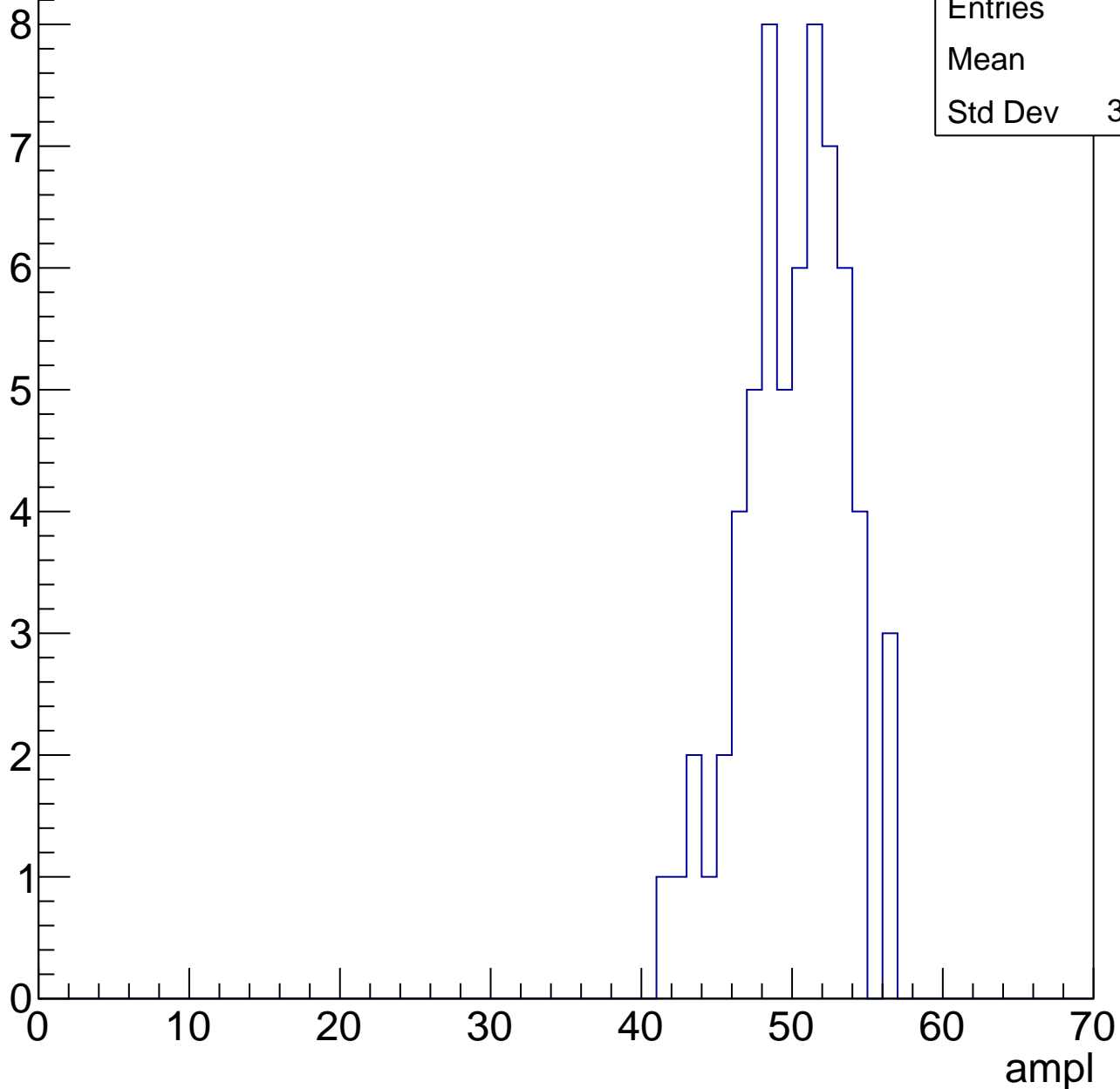


# B1L101S, U19-ch81, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

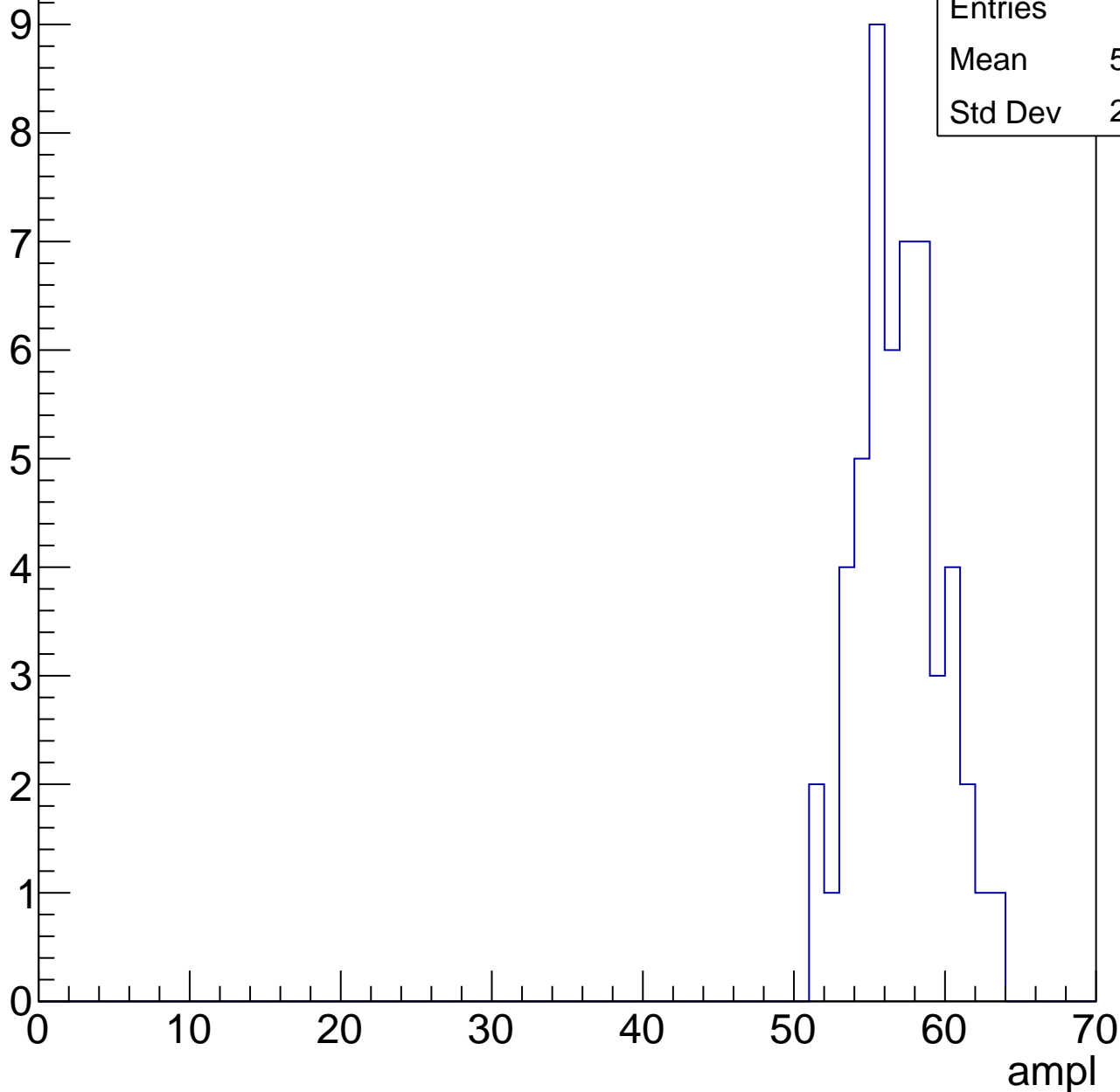
Entries	63
Mean	49.6
Std Dev	3.397



# B1L101S, U19-ch81, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

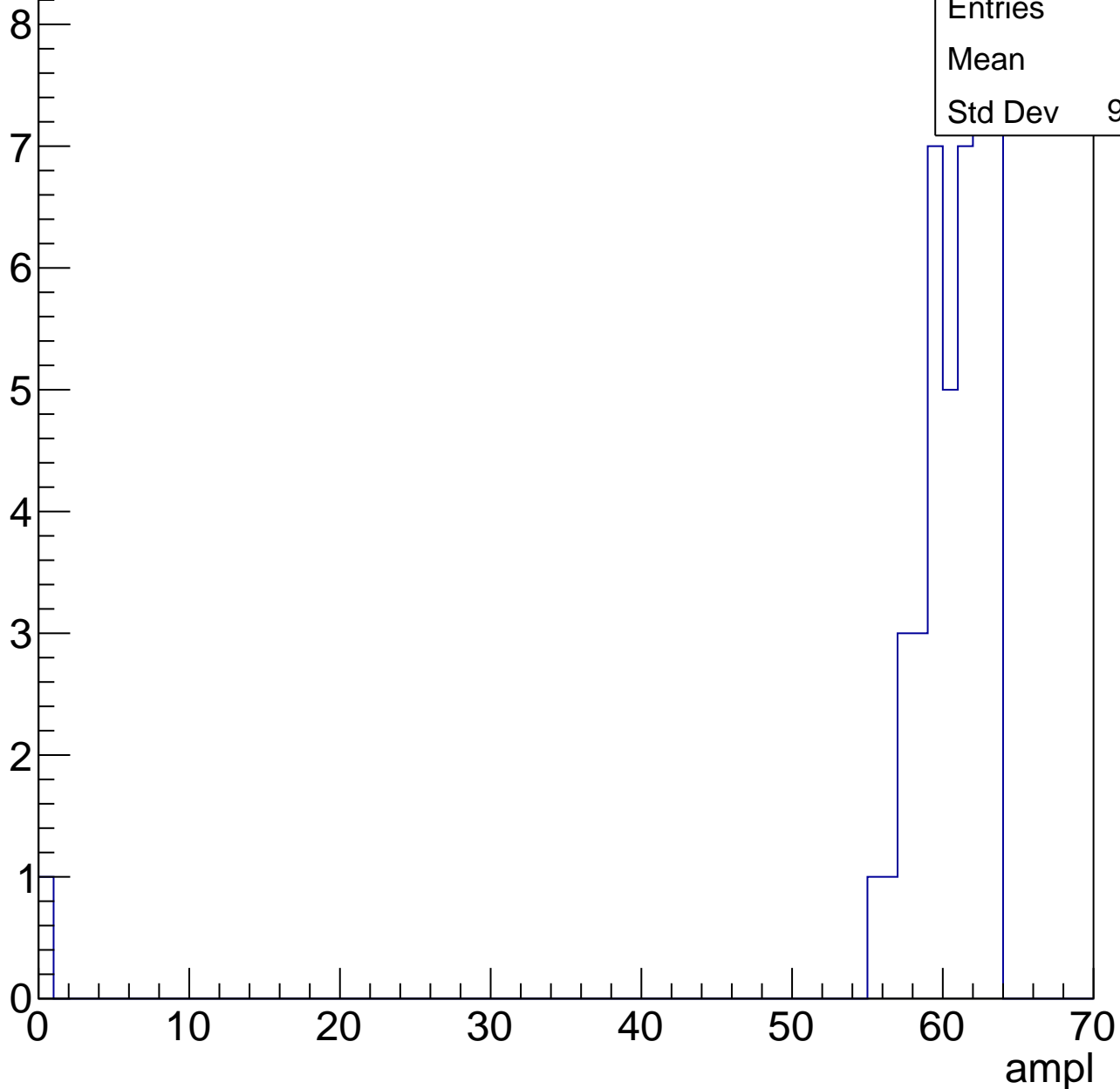


Entries	52
Mean	56.46
Std Dev	2.707

# B1L101S, U19-ch81, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U19-ch81, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

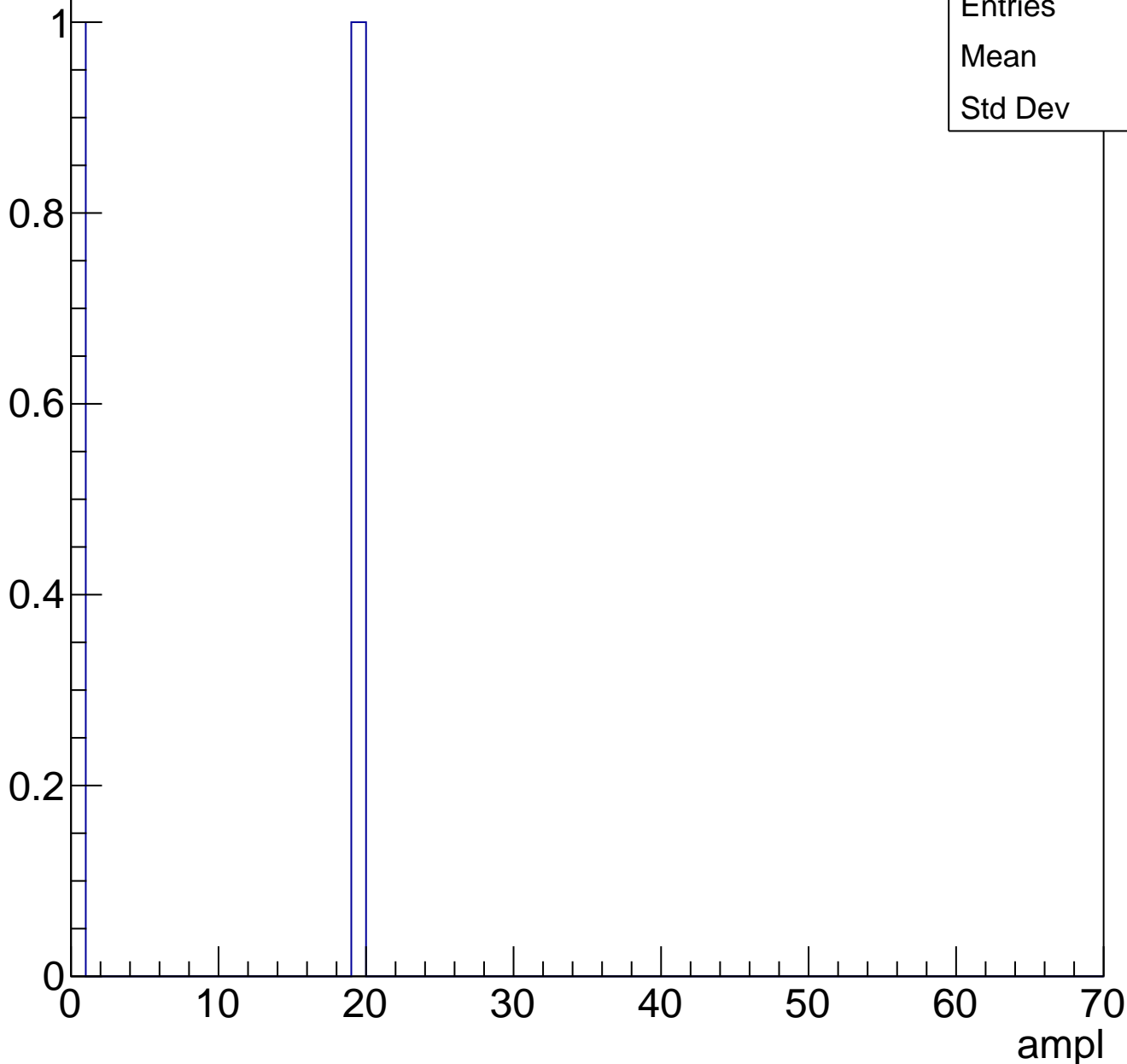




# B1L101S, U19-ch81, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	2
Mean	9.5
Std Dev	9.5

# B1L101S, U19-ch82, adc0

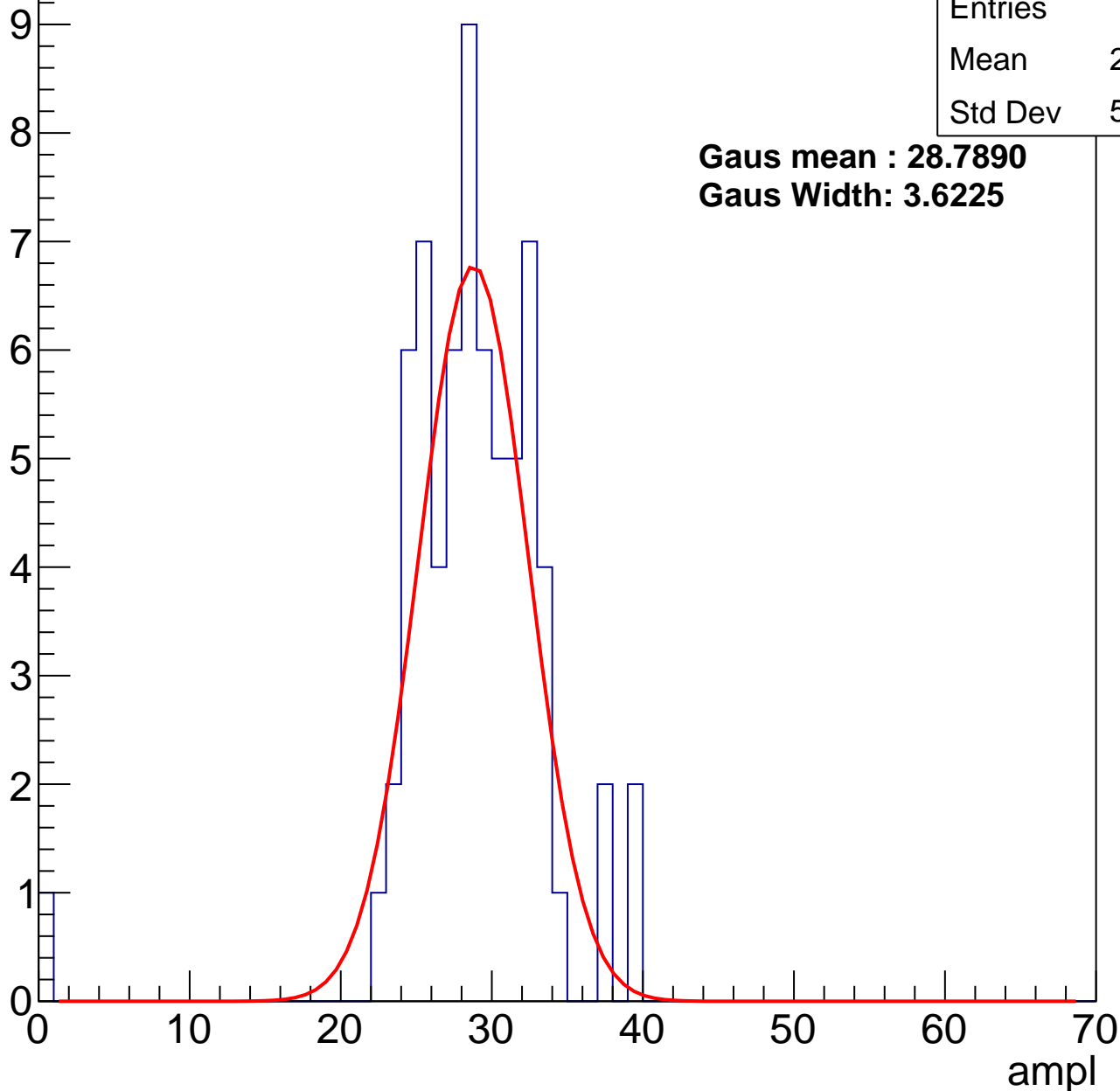
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	28.32
Std Dev	5.097

**Gaus mean : 28.7890**

**Gaus Width: 3.6225**



# B1L101S, U19-ch82, adc1

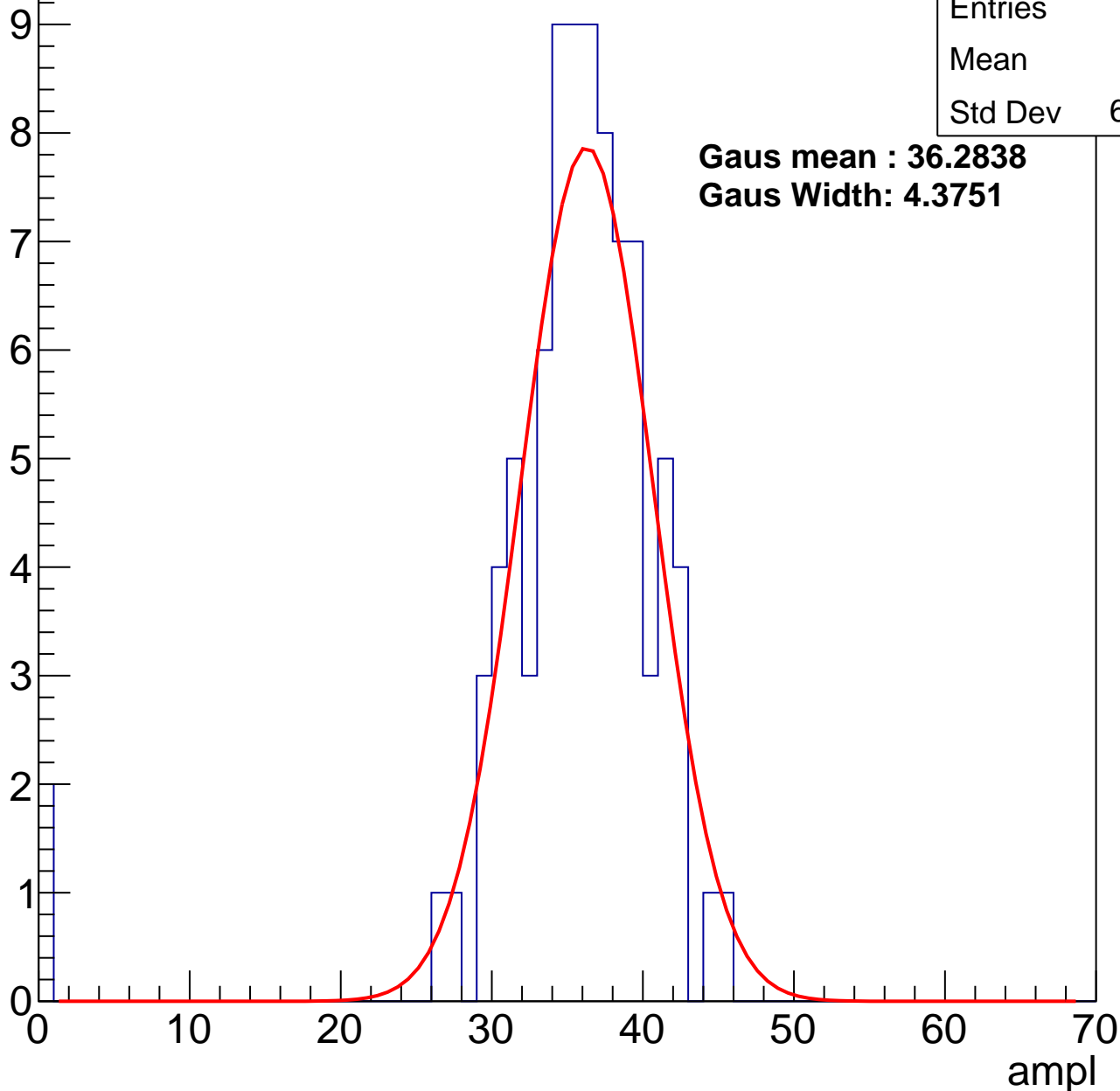
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	88
Mean	34.9
Std Dev	6.563

**Gaus mean : 36.2838**

**Gaus Width: 4.3751**



# B1L101S, U19-ch82, adc2

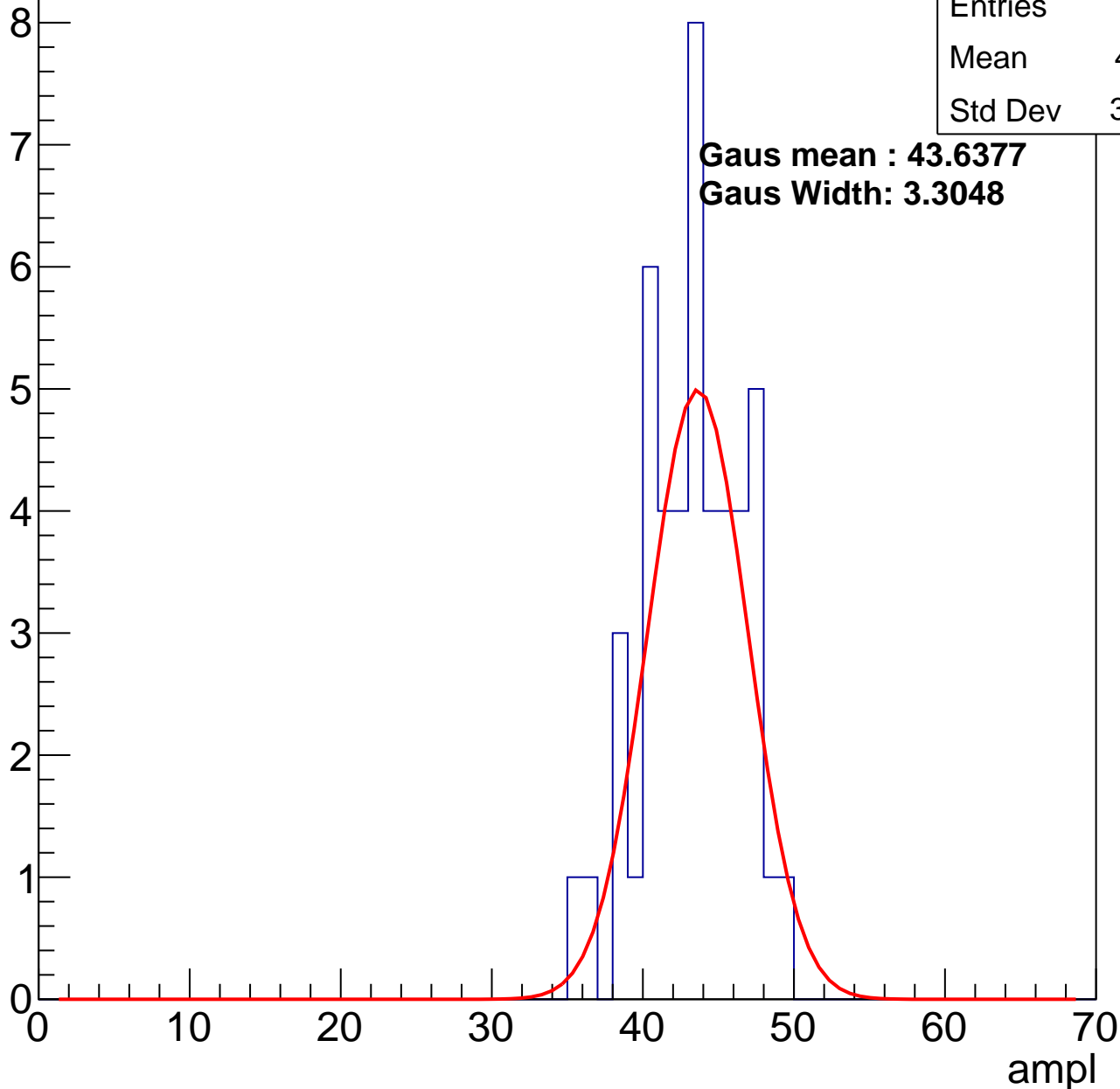
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	47
Mean	42.81
Std Dev	3.173

**Gaus mean : 43.6377**

**Gaus Width: 3.3048**



# B1L101S, U19-ch82, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	75
Mean	48.71
Std Dev	3.687

Entry

10

8

6

4

2

0

0

10

20

30

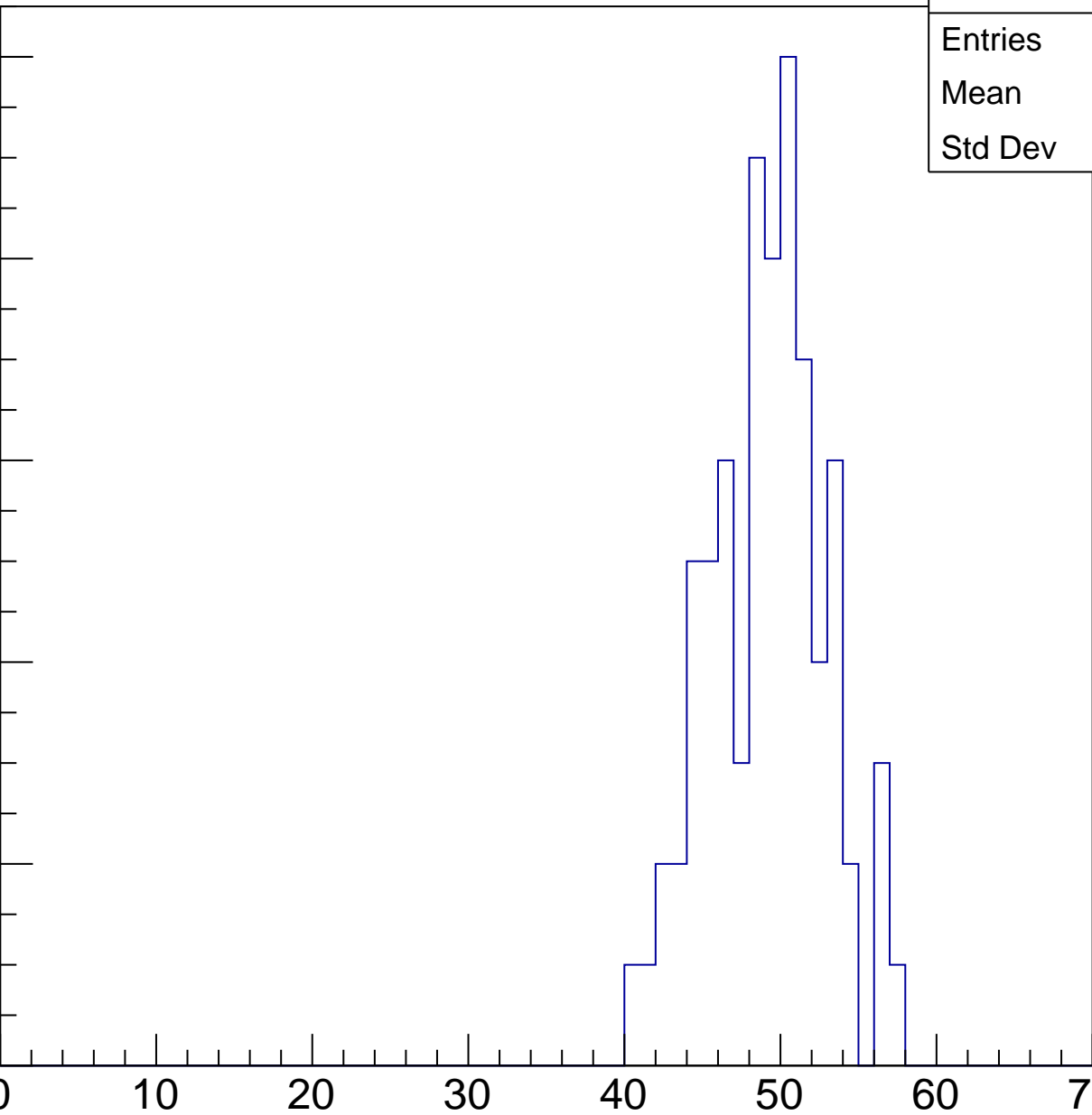
40

50

60

ampl

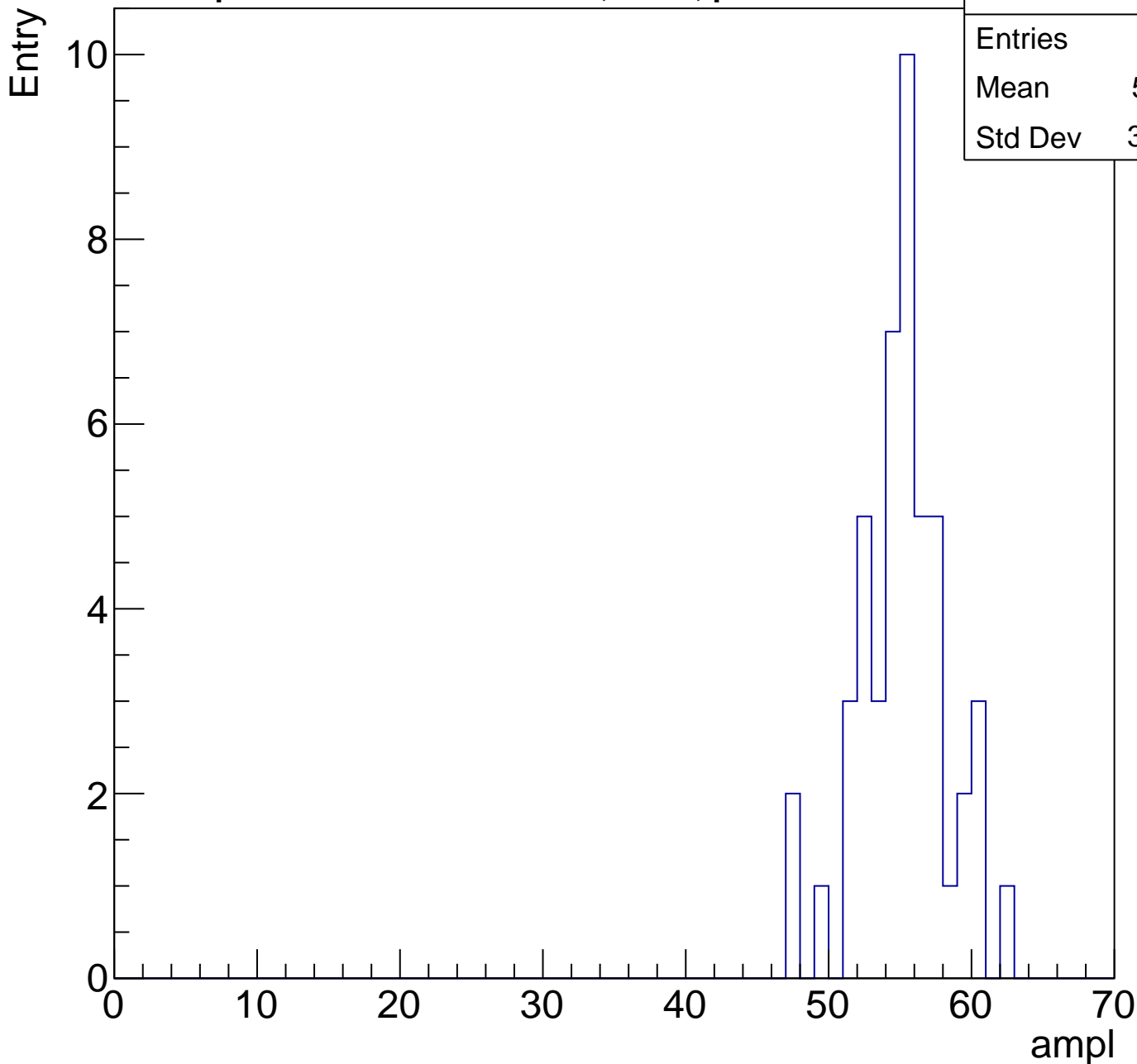
70



# B1L101S, U19-ch82, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

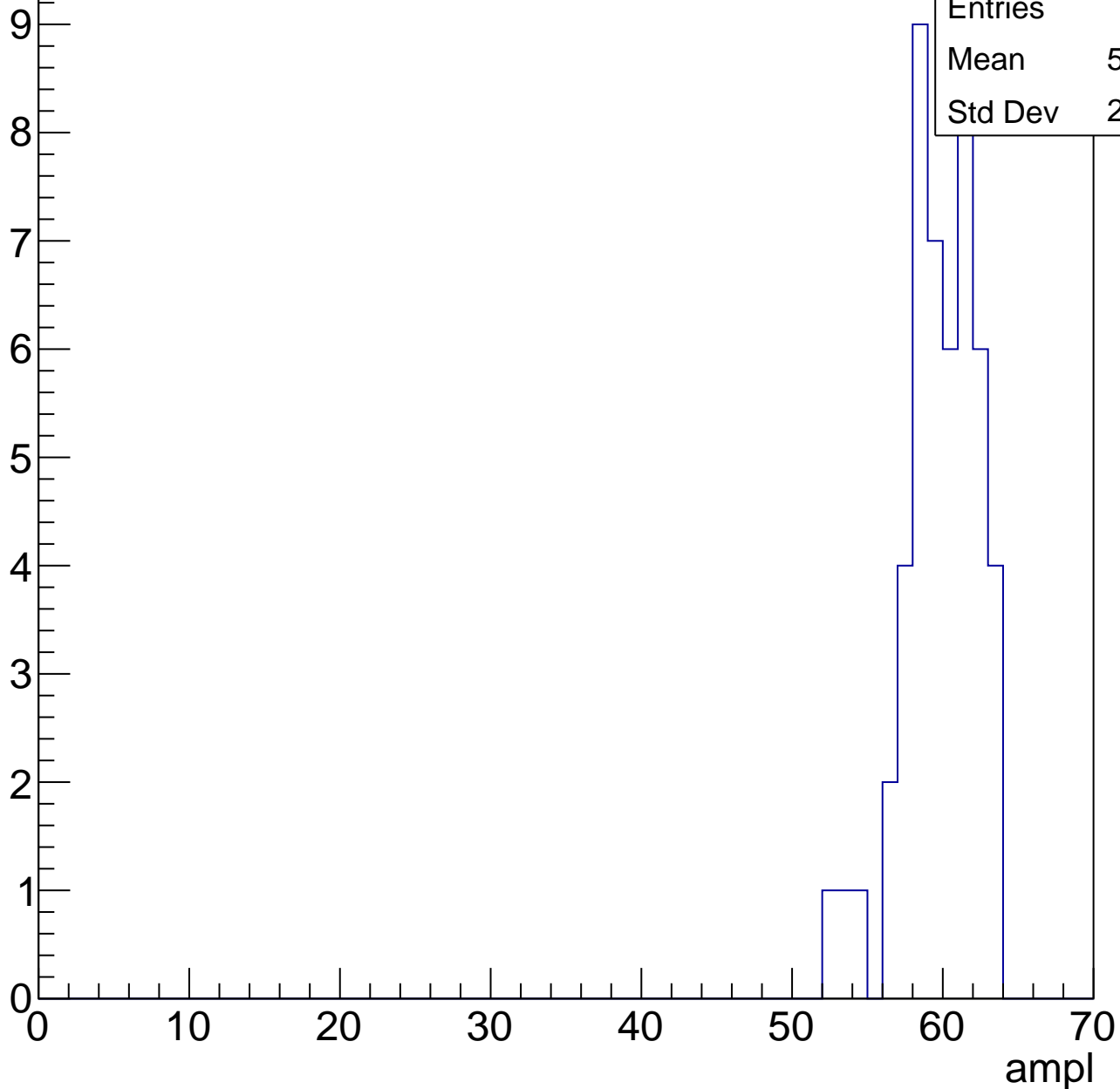
Entries	48
Mean	54.71
Std Dev	3.102



# B1L101S, U19-ch82, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



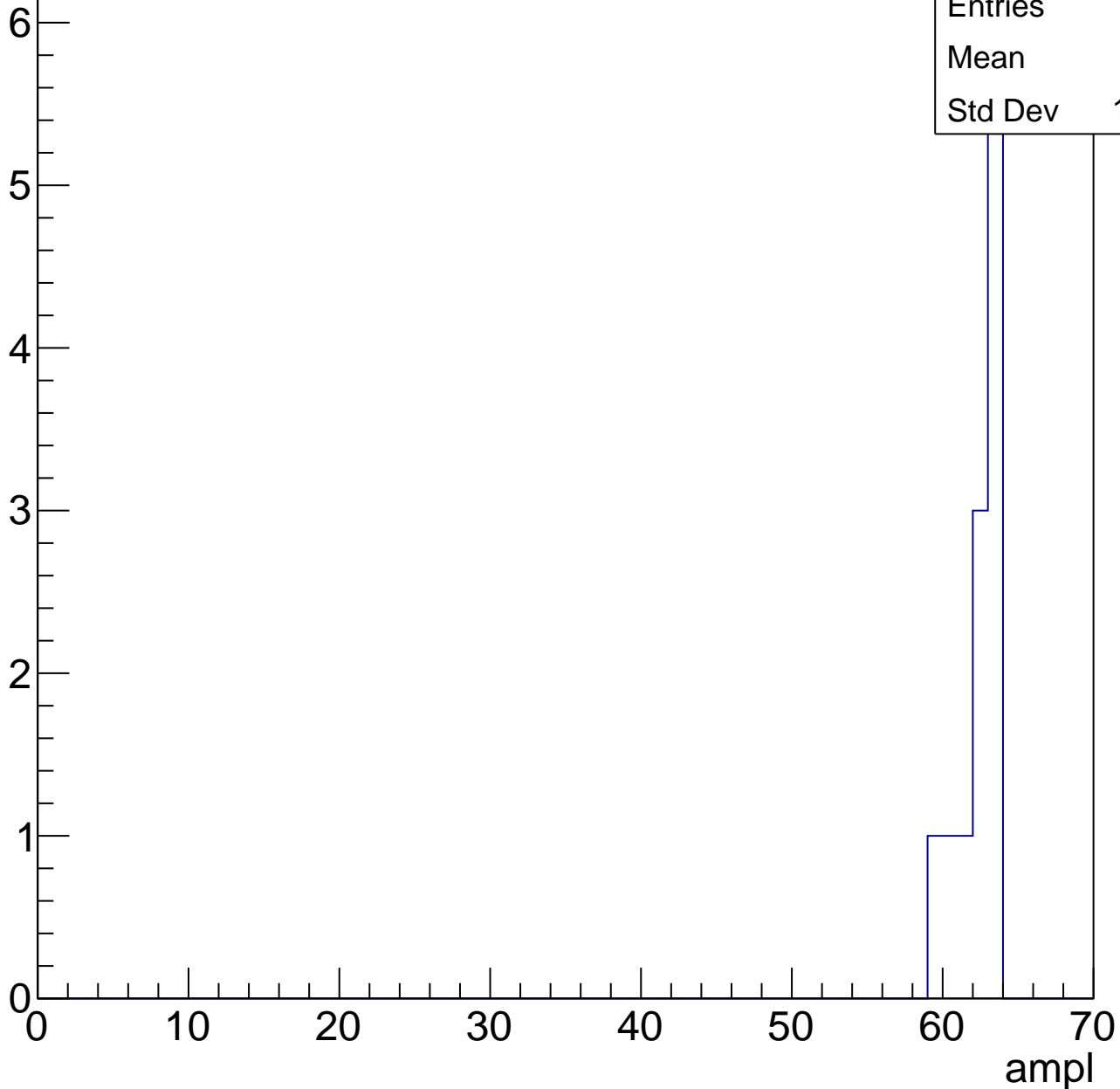
Entries	50
Mean	59.34
Std Dev	2.479

# B1L101S, U19-ch82, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	12
Mean	62
Std Dev	1.291





# B1L101S, U19-ch82, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	2
Mean	9.5
Std Dev	9.5

# B1L101S, U19-ch83, adc0

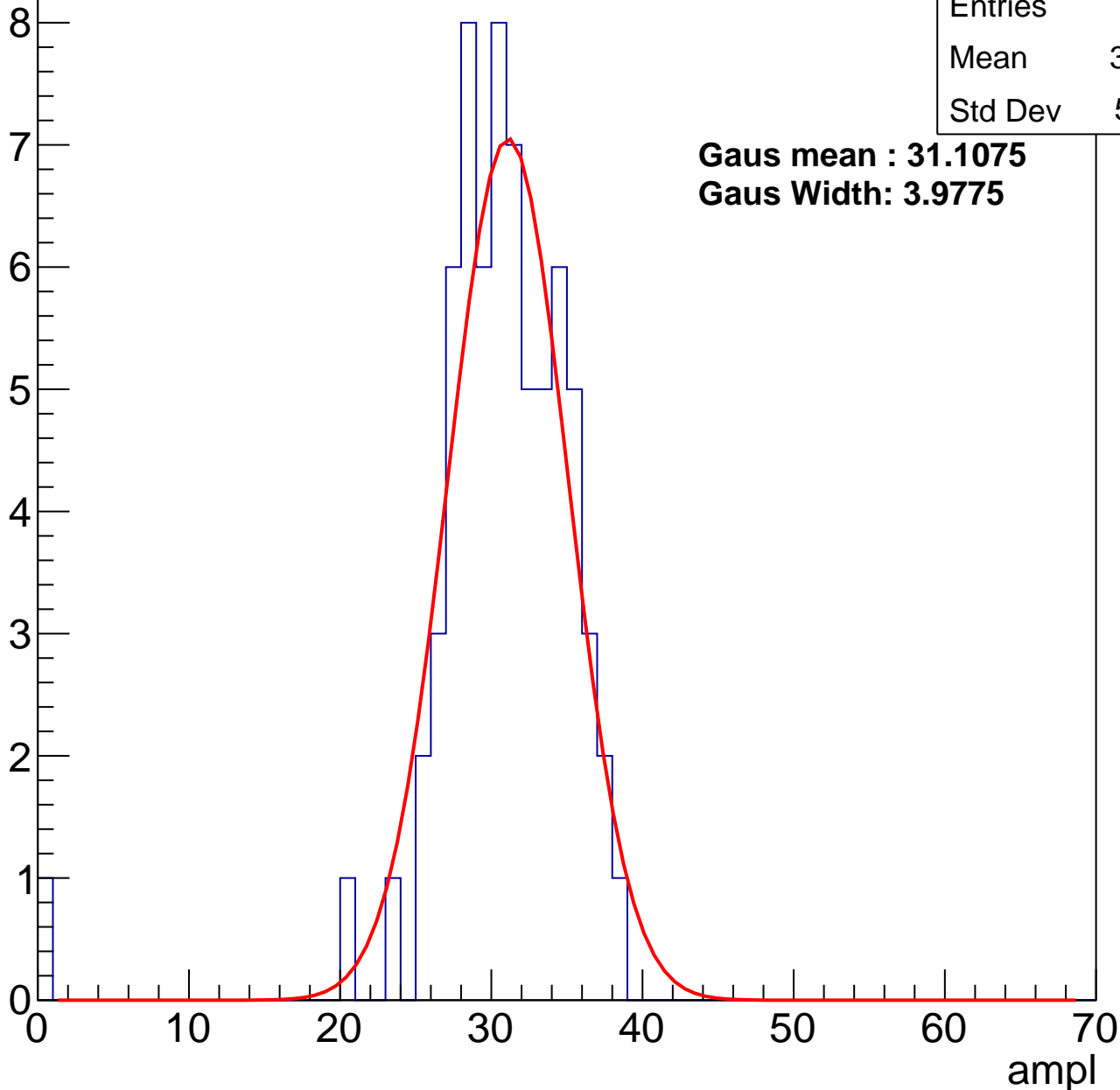
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	30.17
Std Dev	5.071

**Gaus mean : 31.1075**

**Gaus Width: 3.9775**



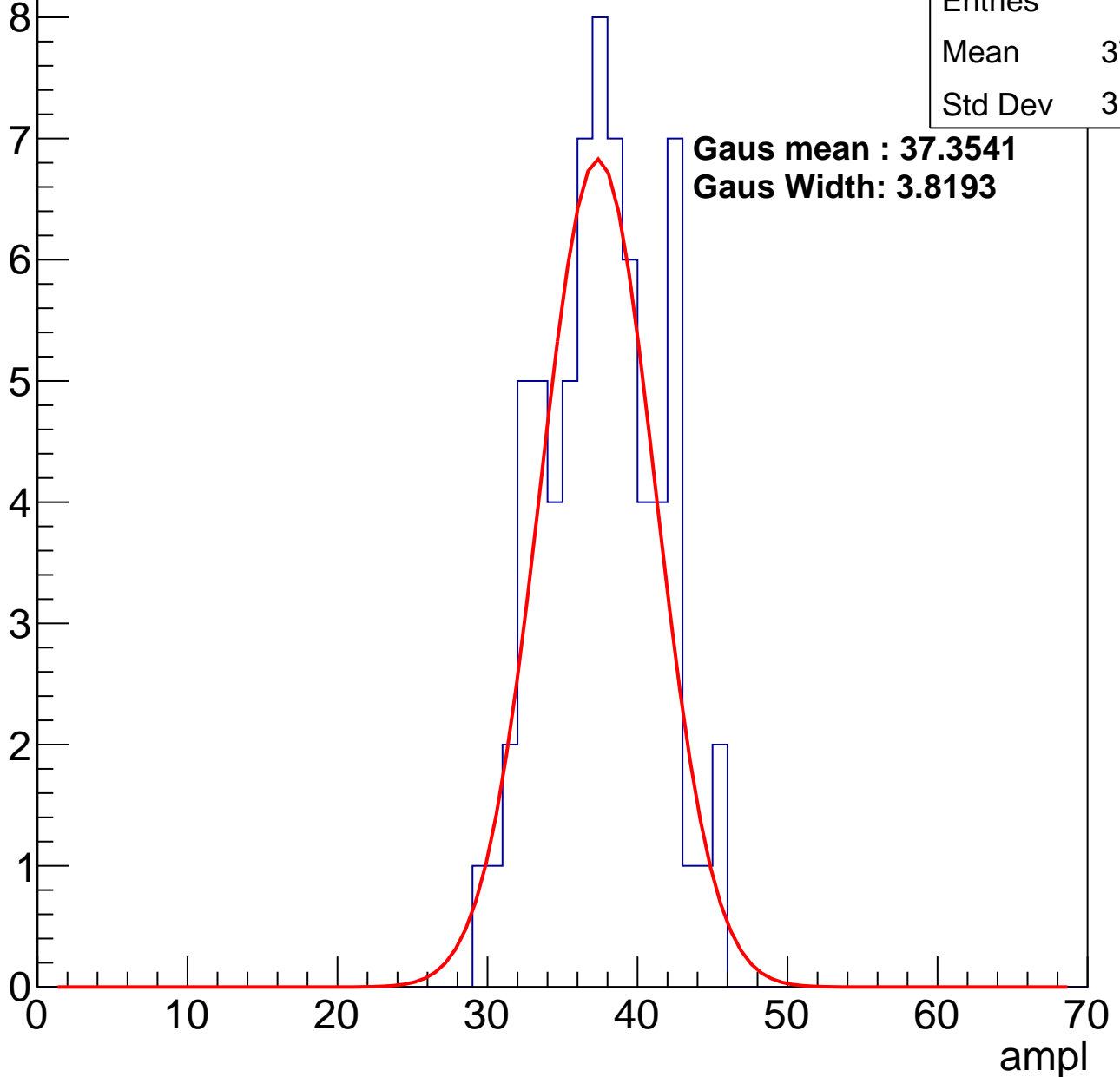
# B1L101S, U19-ch83, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	37.14
Std Dev	3.724

**Gaus mean : 37.3541**  
**Gaus Width: 3.8193**



# B1L101S, U19-ch83, adc2

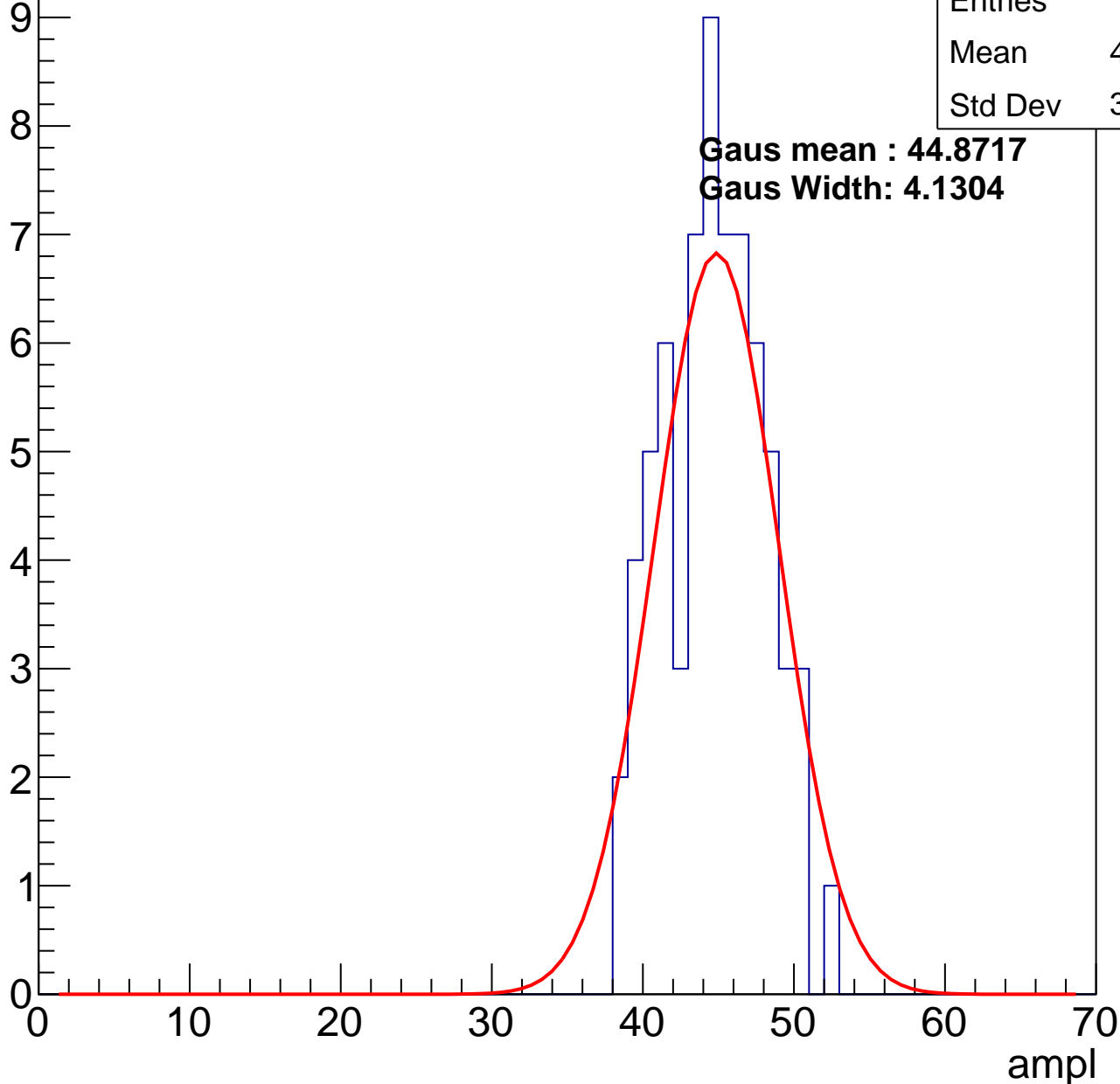
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	44.25
Std Dev	3.292

**Gaus mean : 44.8717**

**Gaus Width: 4.1304**



# B1L101S, U19-ch83, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

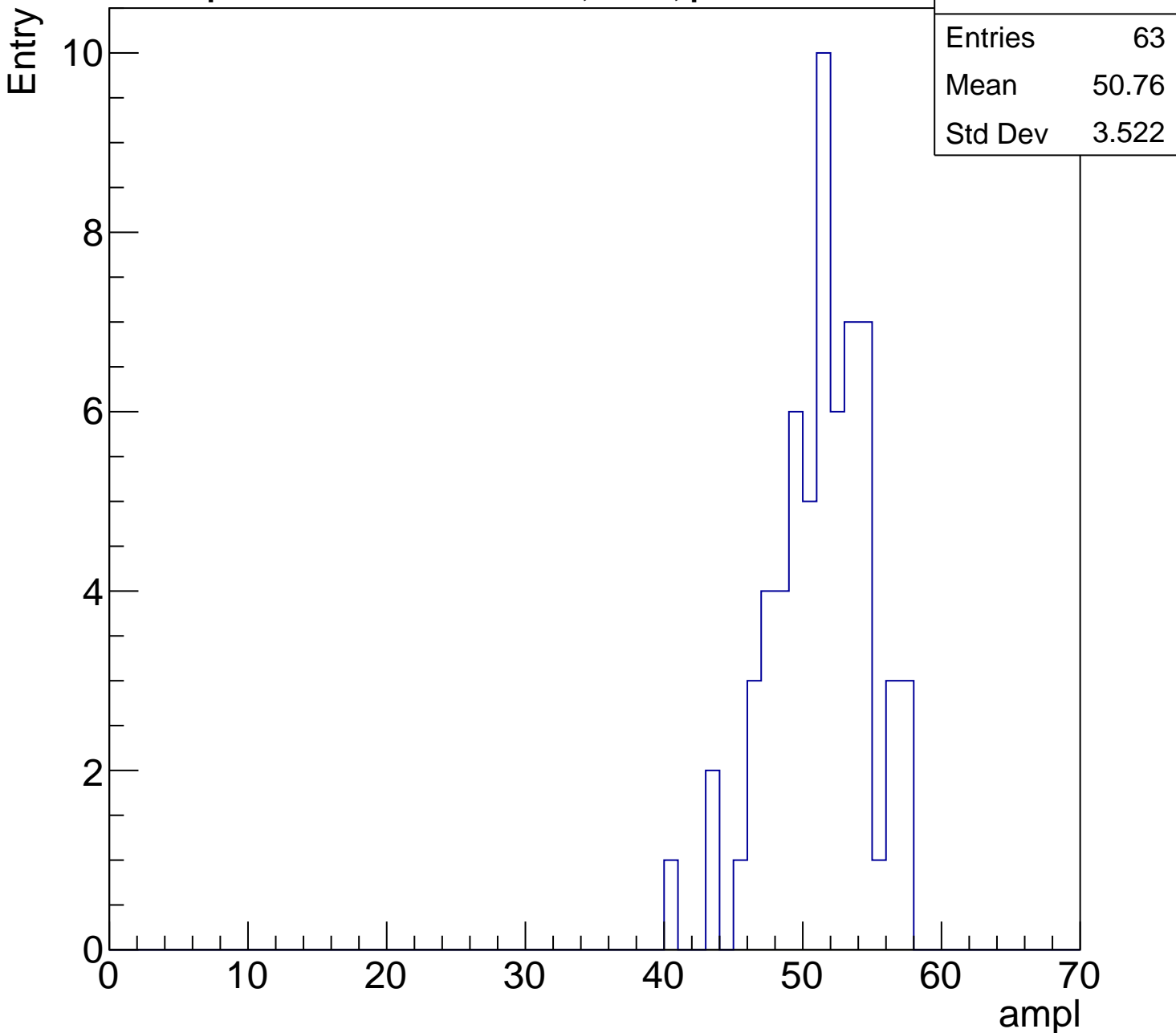
Entries	63
Mean	50.76
Std Dev	3.522

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

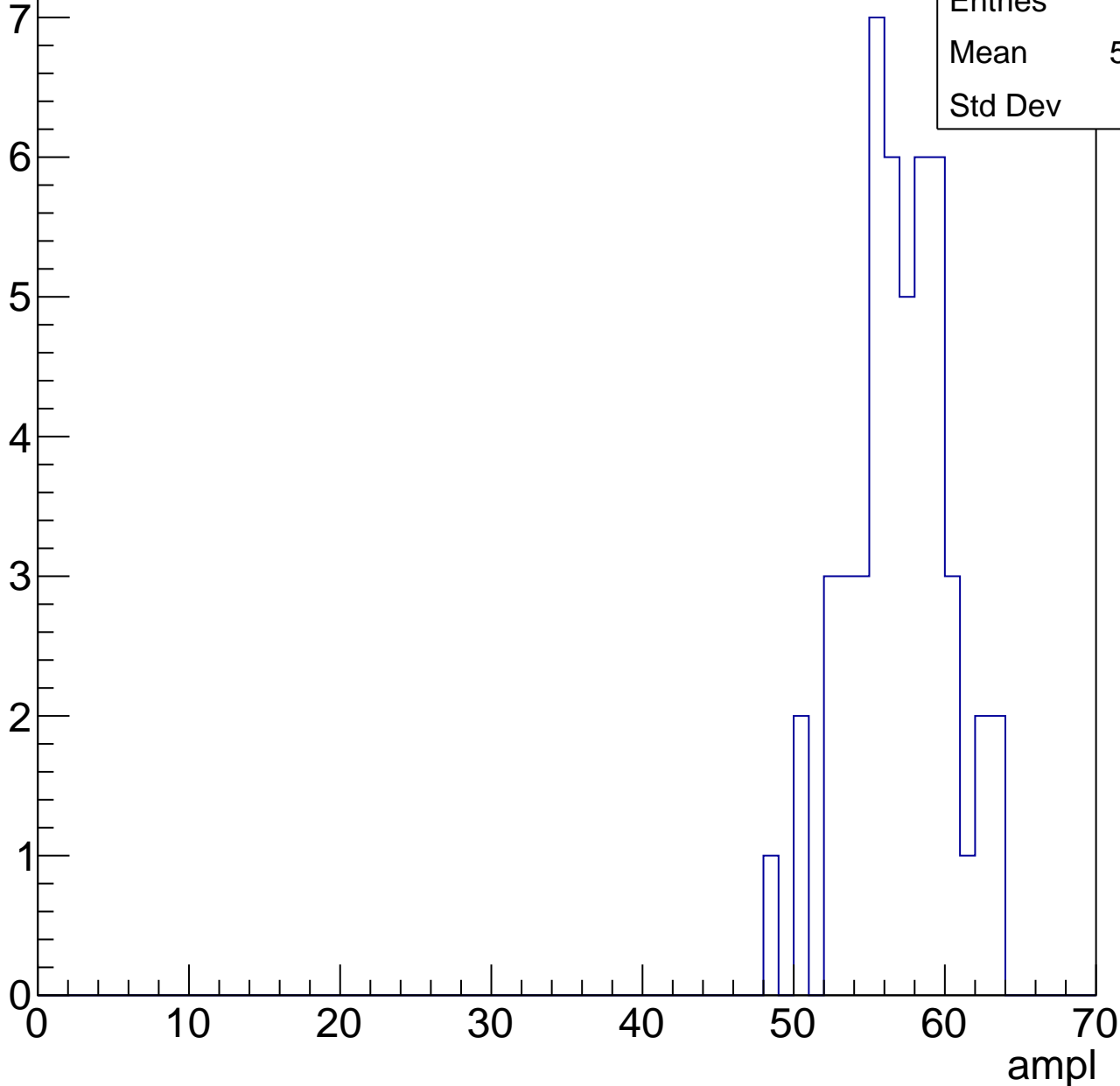


# B1L101S, U19-ch83, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

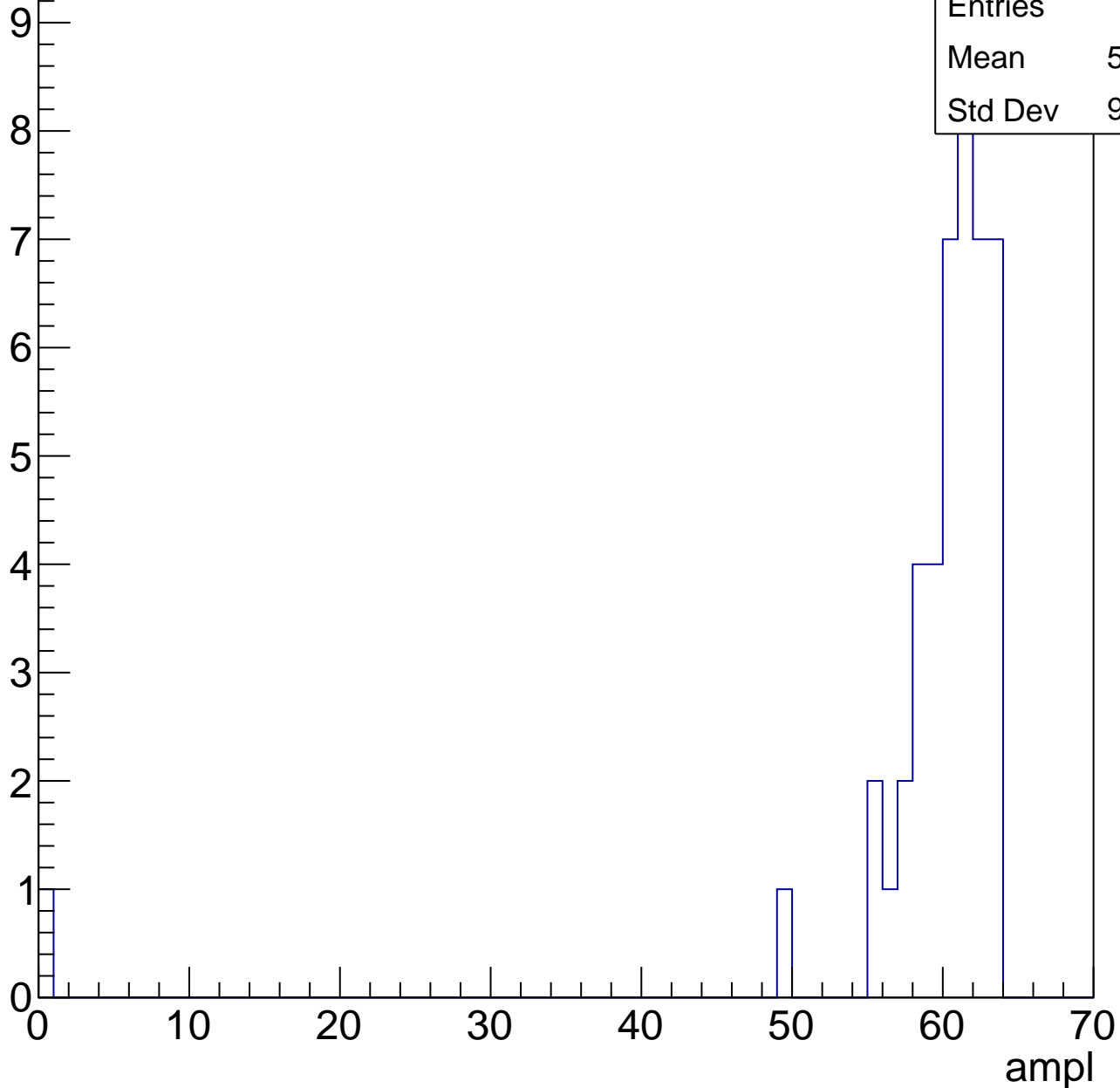
Entries	50
Mean	56.48
Std Dev	3.3



# B1L101S, U19-ch83, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U19-ch83, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U19-ch83, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U19-ch84, adc0

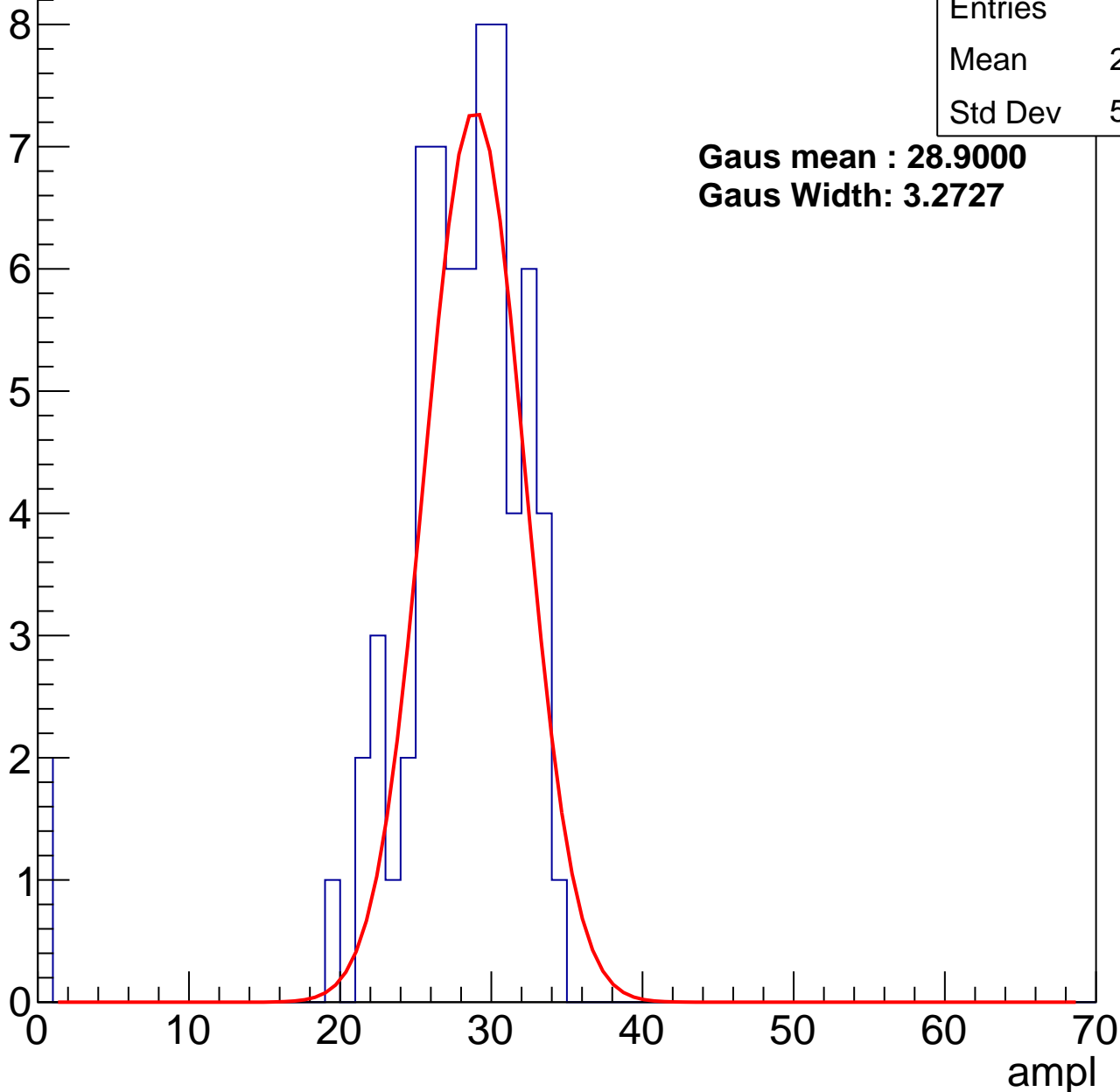
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	27.04
Std Dev	5.758

**Gaus mean : 28.9000**

**Gaus Width: 3.2727**



# B1L101S, U19-ch84, adc1

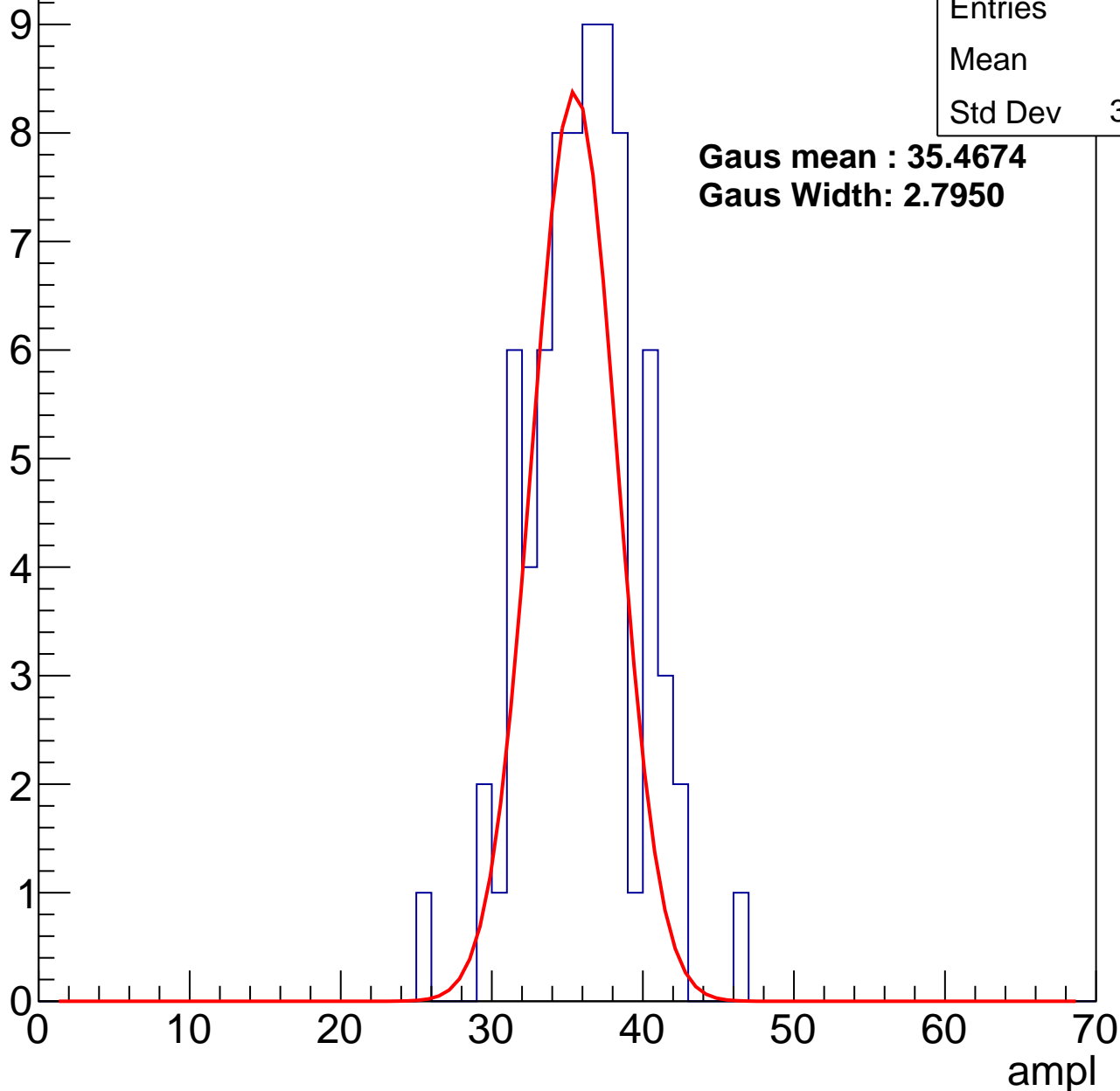
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	75
Mean	35.6
Std Dev	3.548

**Gaus mean : 35.4674**

**Gaus Width: 2.7950**



# B1L101S, U19-ch84, adc2

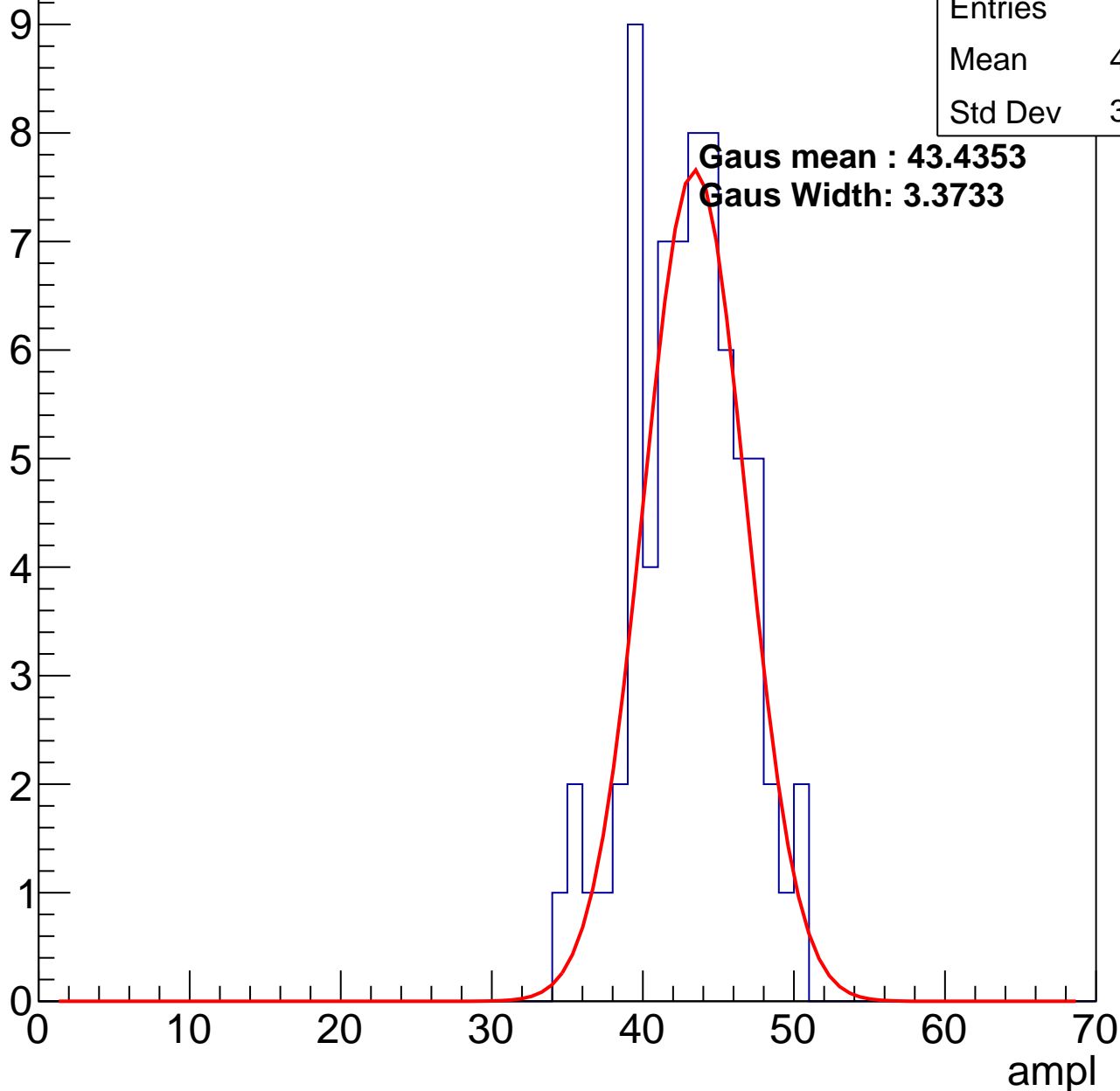
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	71
Mean	42.55
Std Dev	3.532

**Gaus mean : 43.4353**

**Gaus Width: 3.3733**

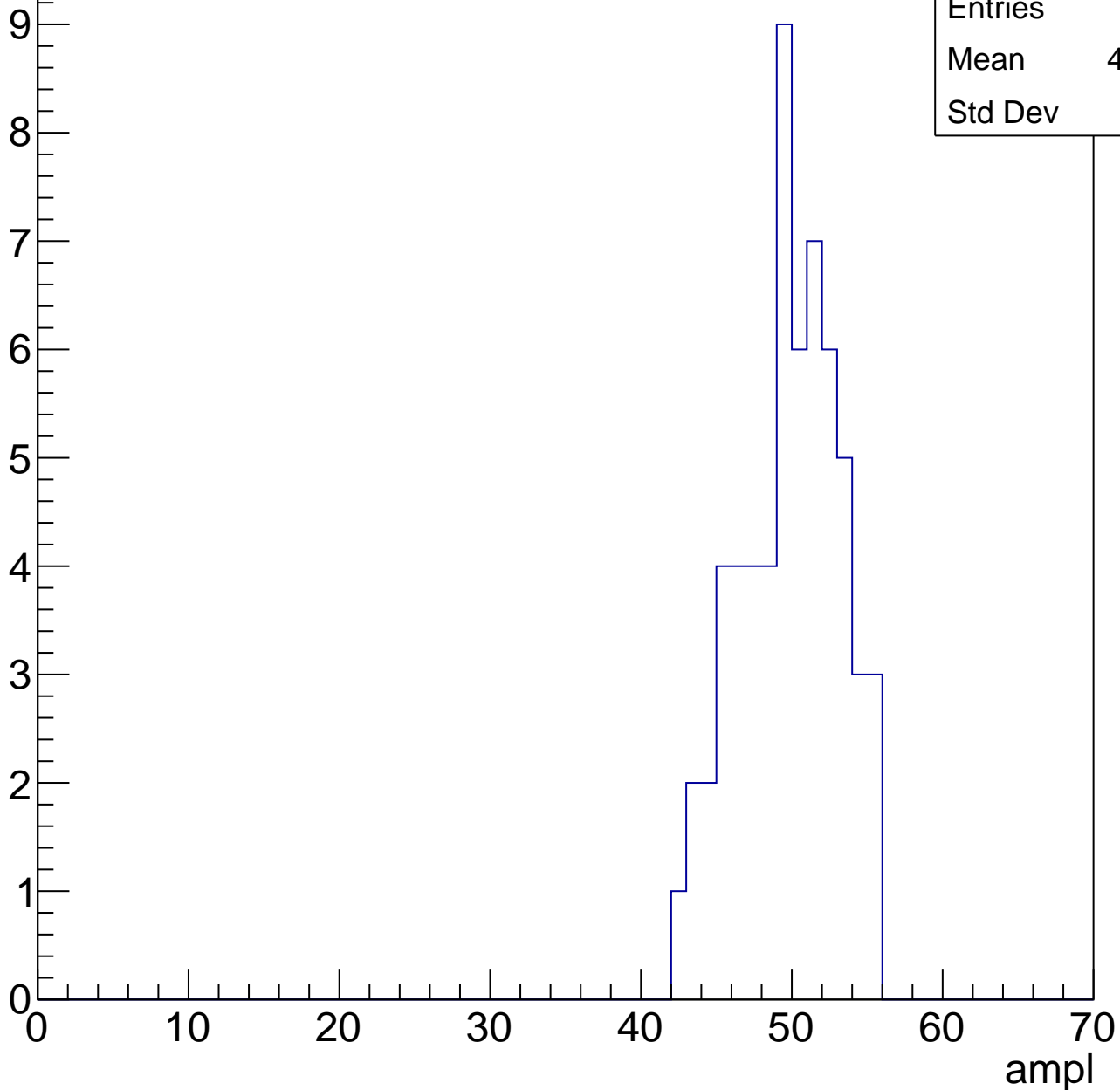


# B1L101S, U19-ch84, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	60
Mean	49.37
Std Dev	3.25

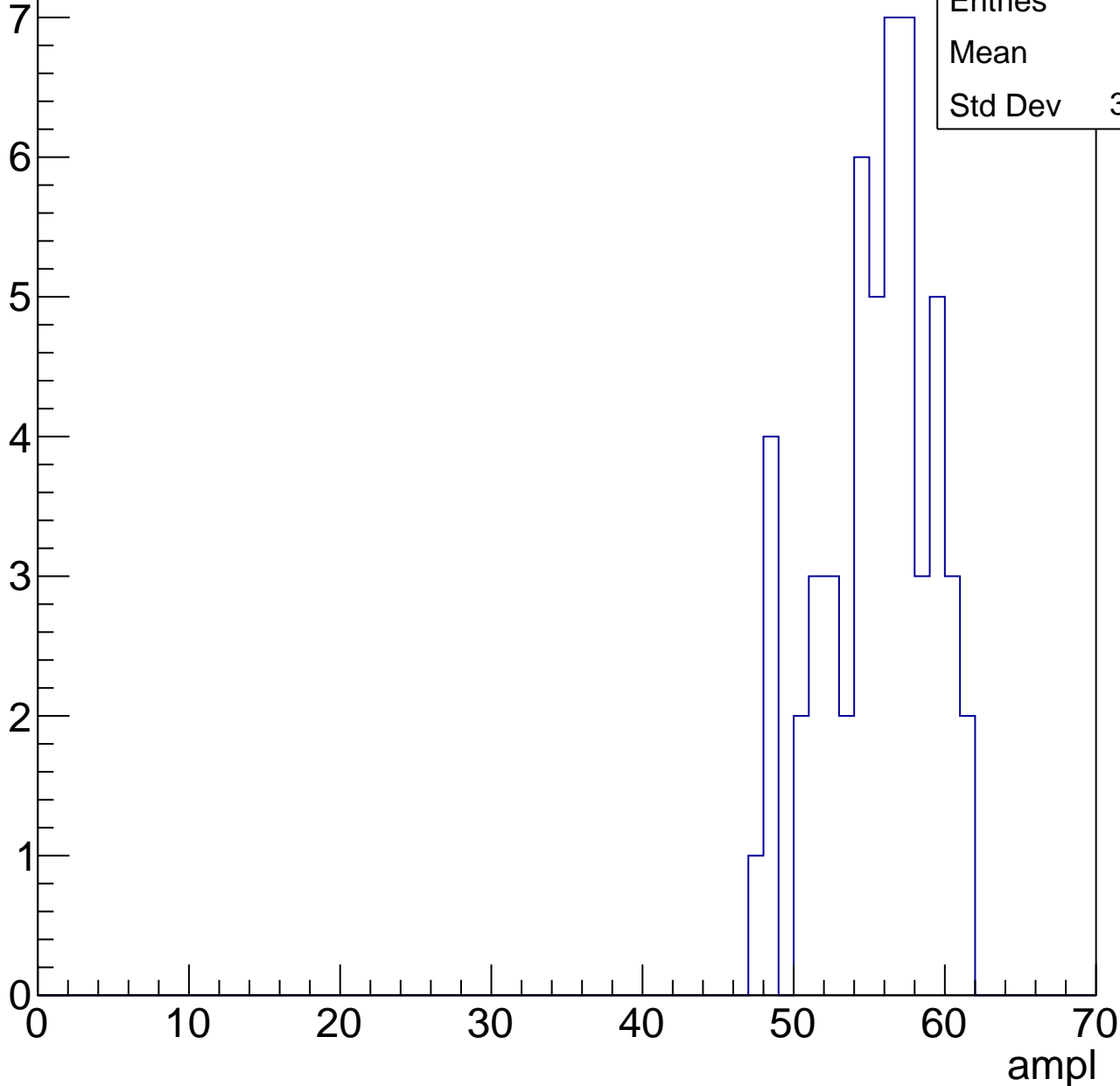


# B1L101S, U19-ch84, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	53
Mean	55
Std Dev	3.603

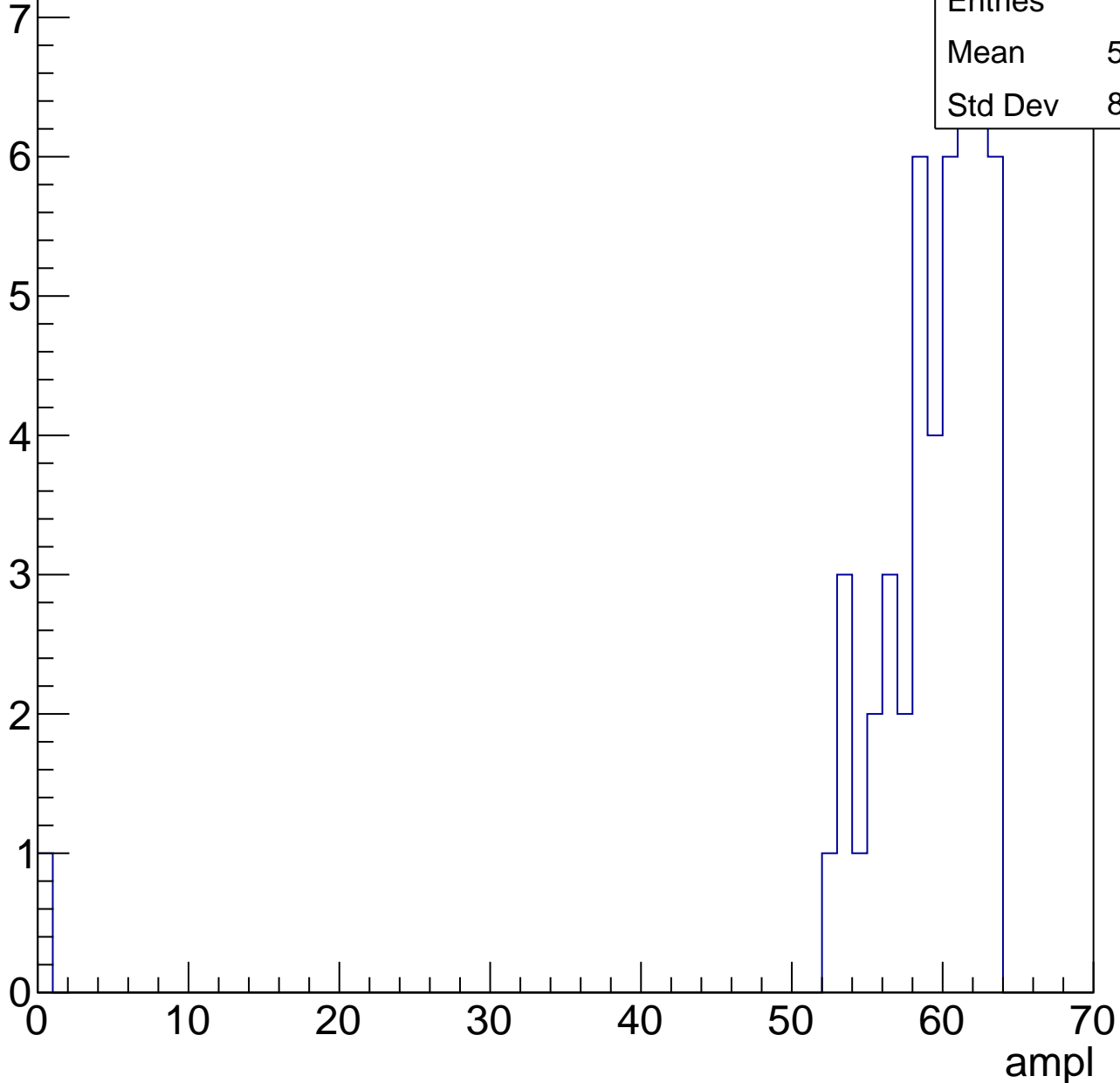


# B1L101S, U19-ch84, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

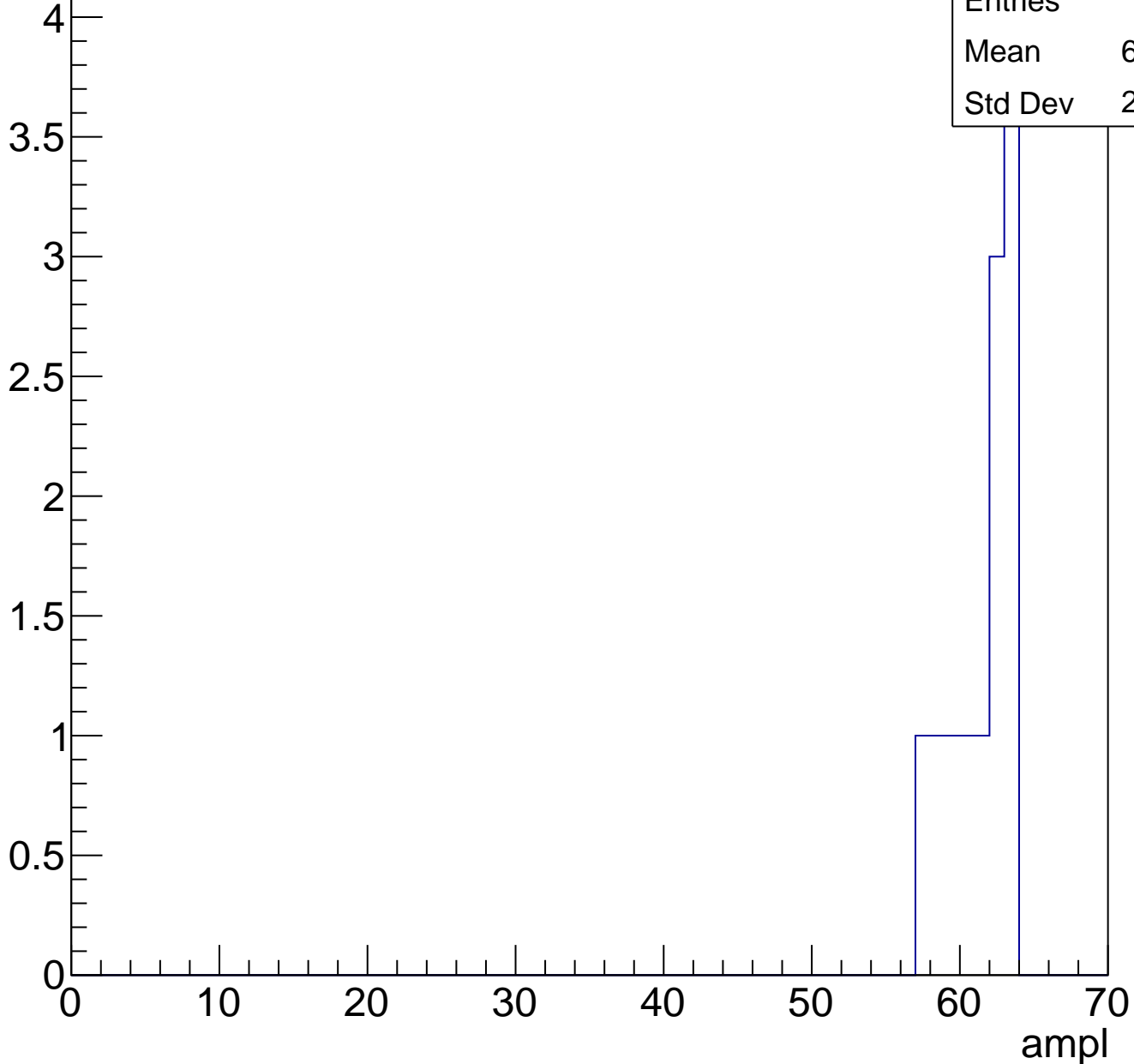
Entries	49
Mean	57.96
Std Dev	8.894



# B1L101S, U19-ch84, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U19-ch84, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U19-ch85, adc0

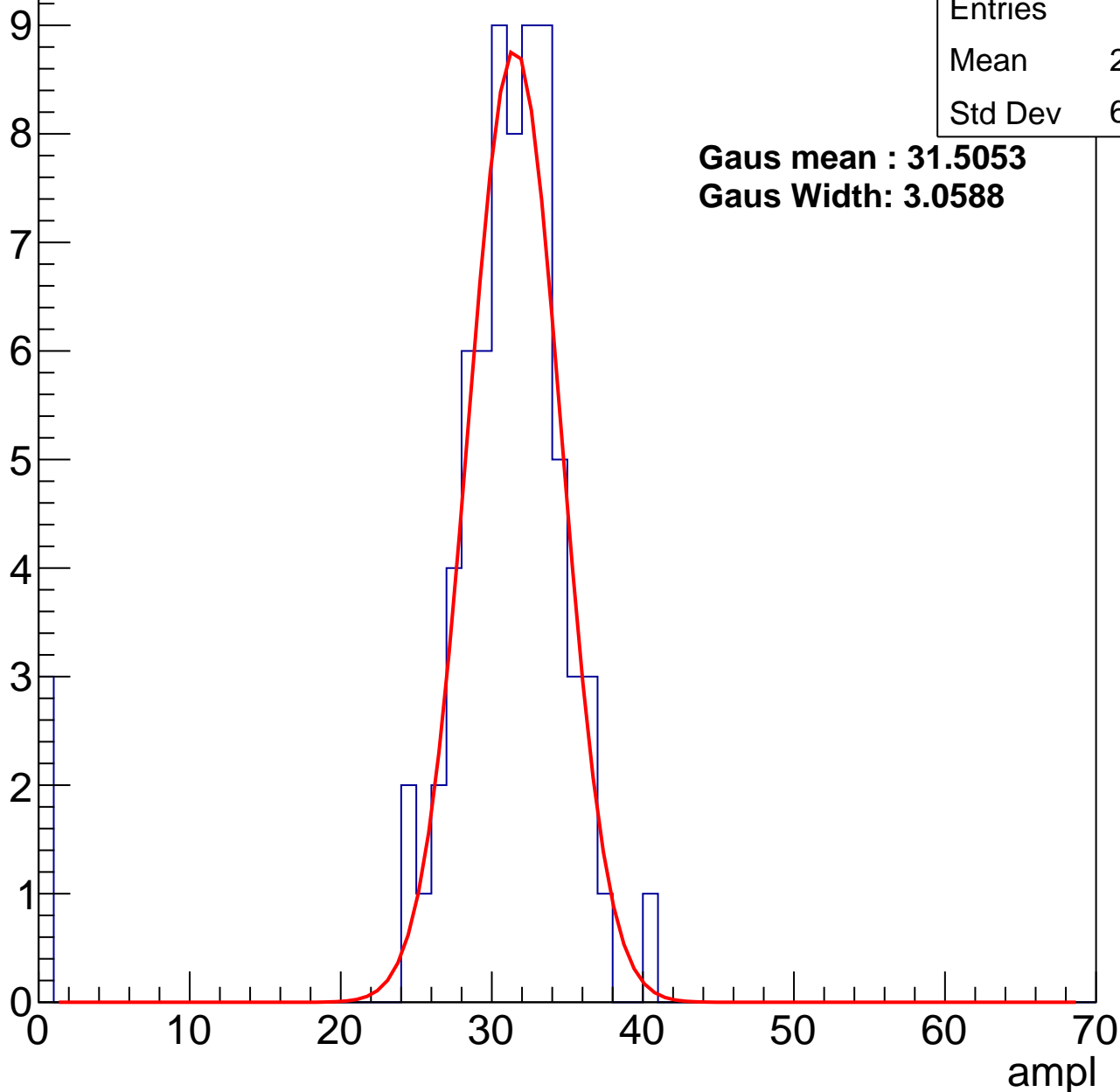
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	72
Mean	29.69
Std Dev	6.897

**Gaus mean : 31.5053**

**Gaus Width: 3.0588**



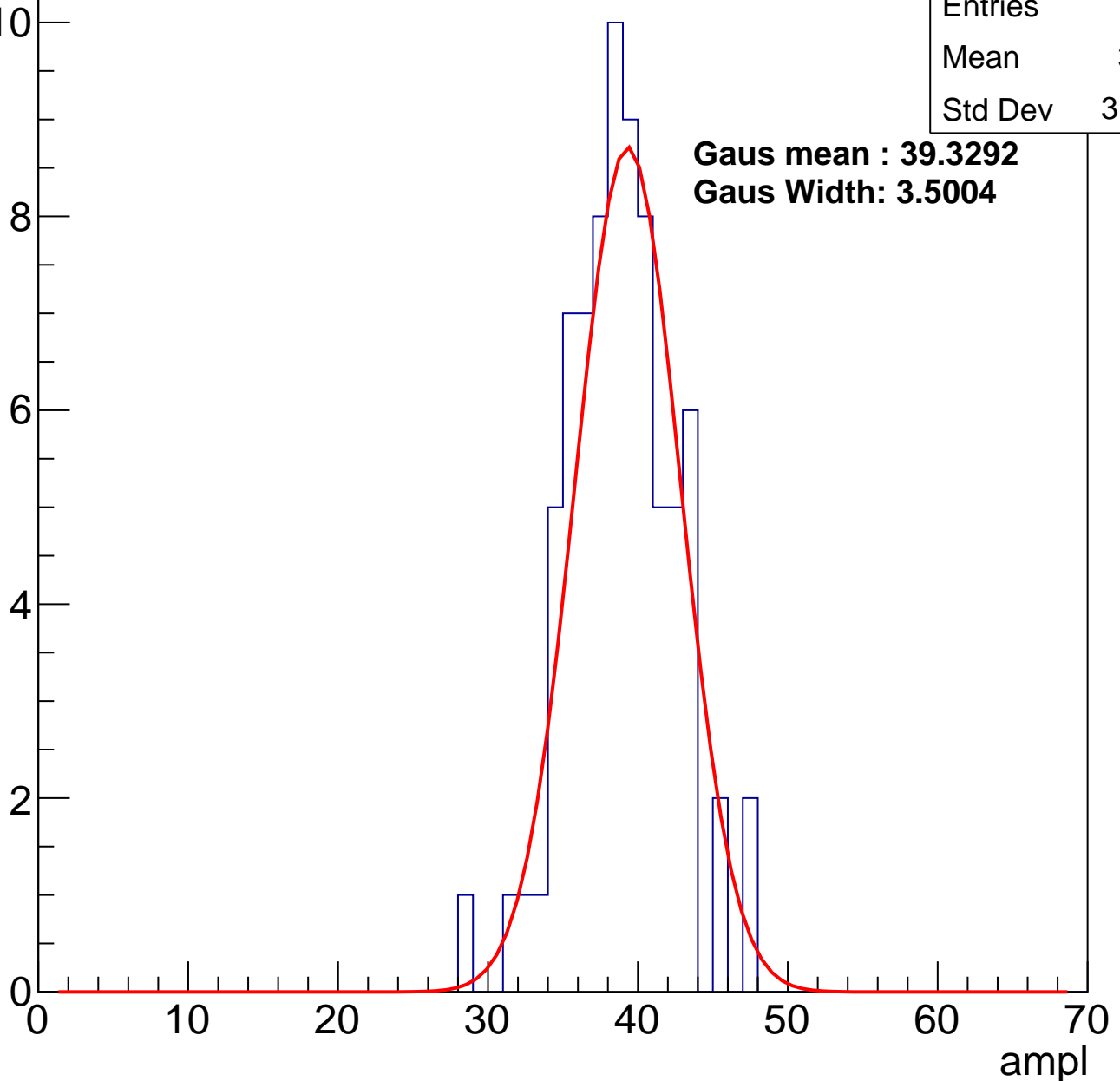
# B1L101S, U19-ch85, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	78
Mean	38.4
Std Dev	3.495

**Gaus mean : 39.3292**  
**Gaus Width: 3.5004**



# B1L101S, U19-ch85, adc2

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	60
Mean	45.12
Std Dev	3.194

**Gaus mean : 45.3256**

**Gaus Width: 2.5162**

10

8

6

4

2

0

0

10

20

30

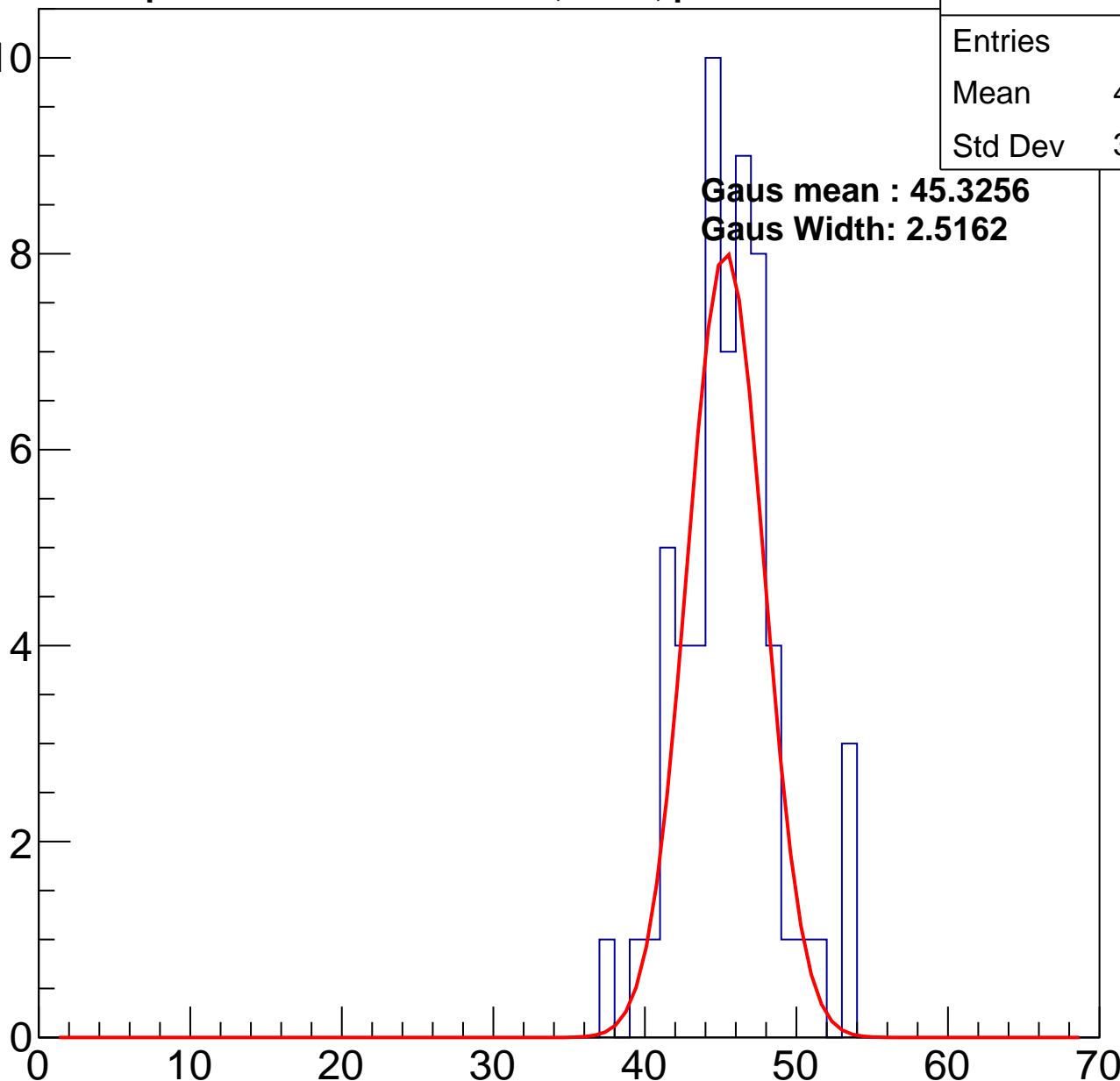
40

50

60

70

ampl

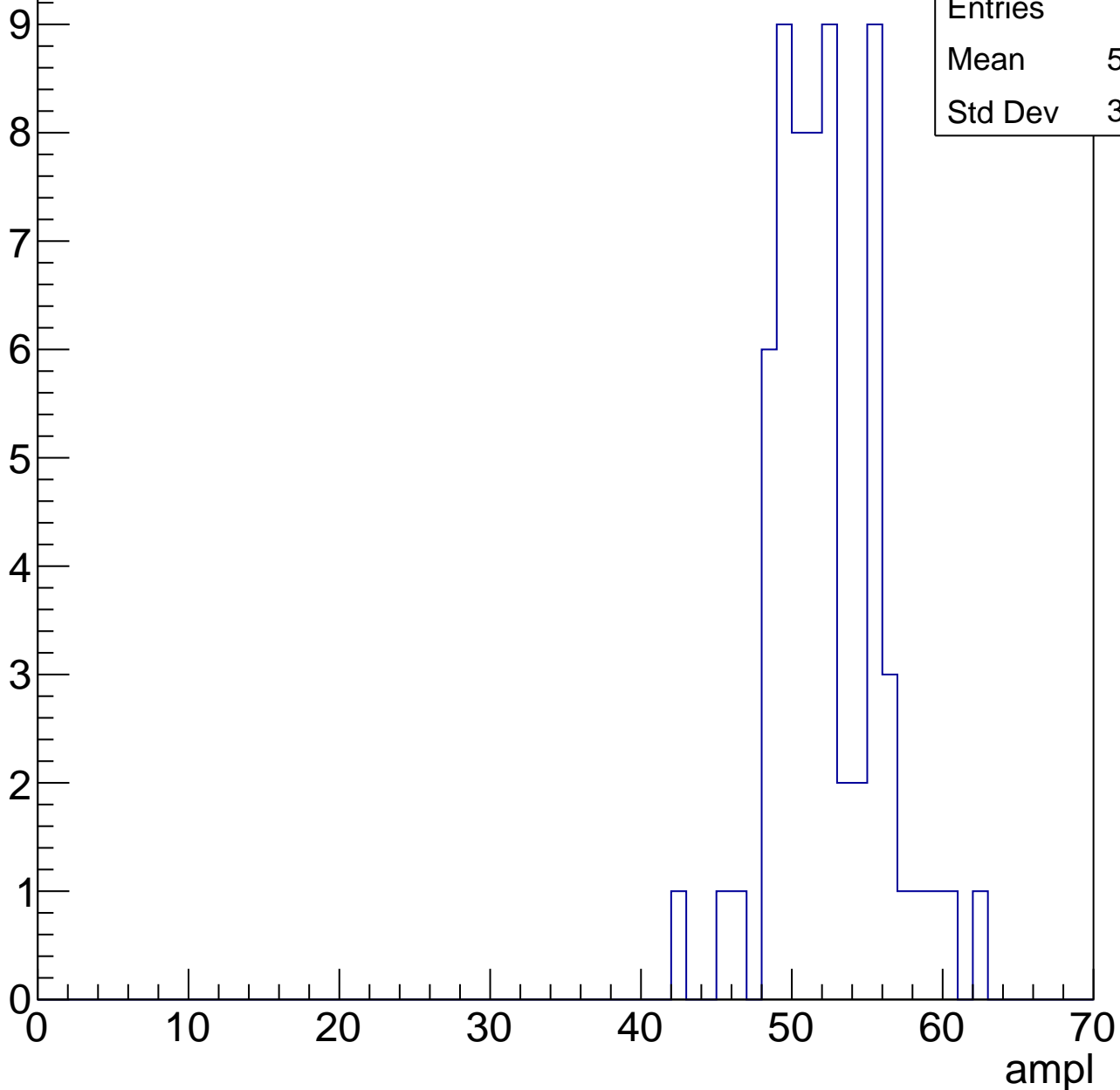


# B1L101S, U19-ch85, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

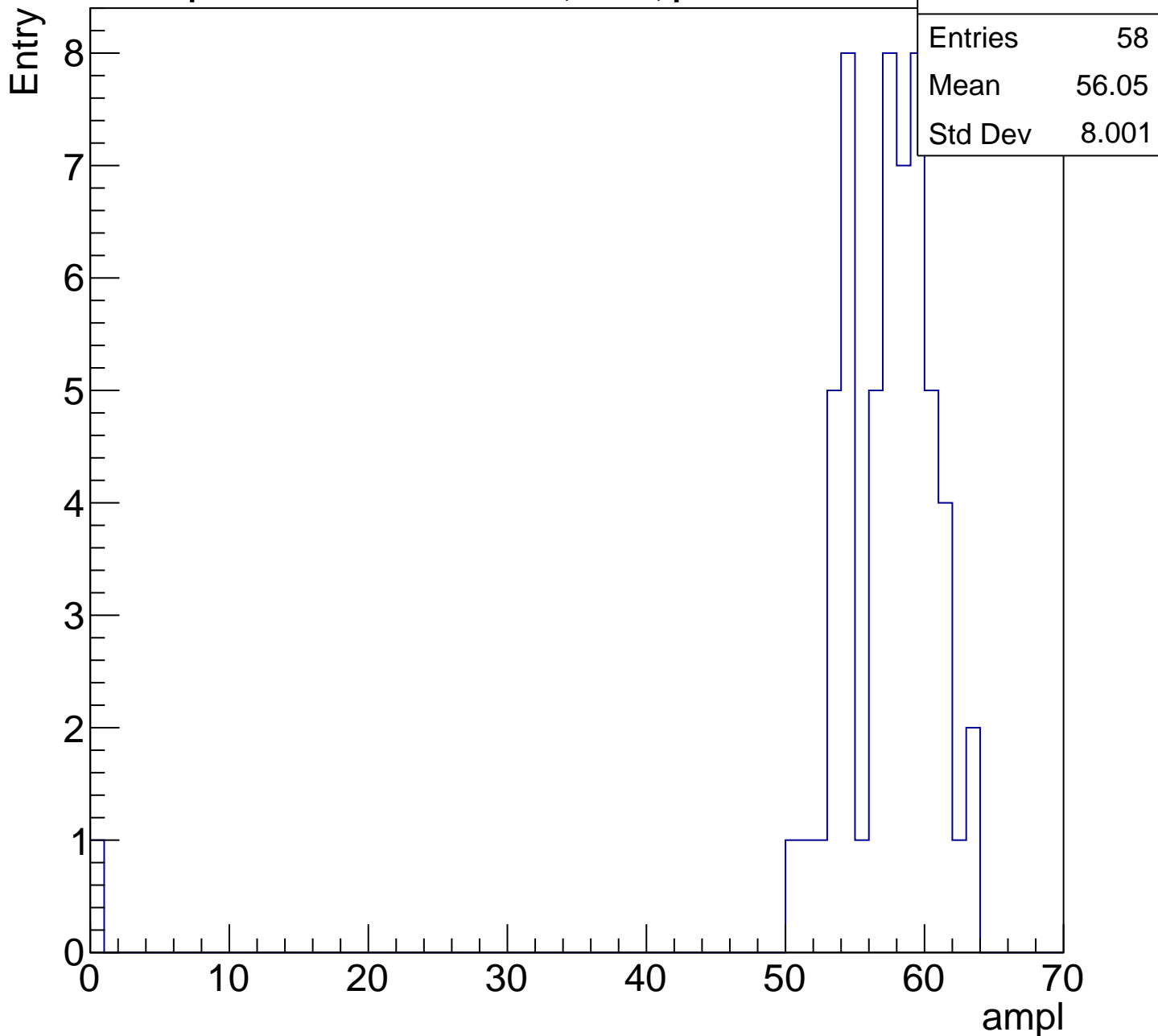
Entry

Entries	64
Mean	51.73
Std Dev	3.559



# B1L101S, U19-ch85, adc4

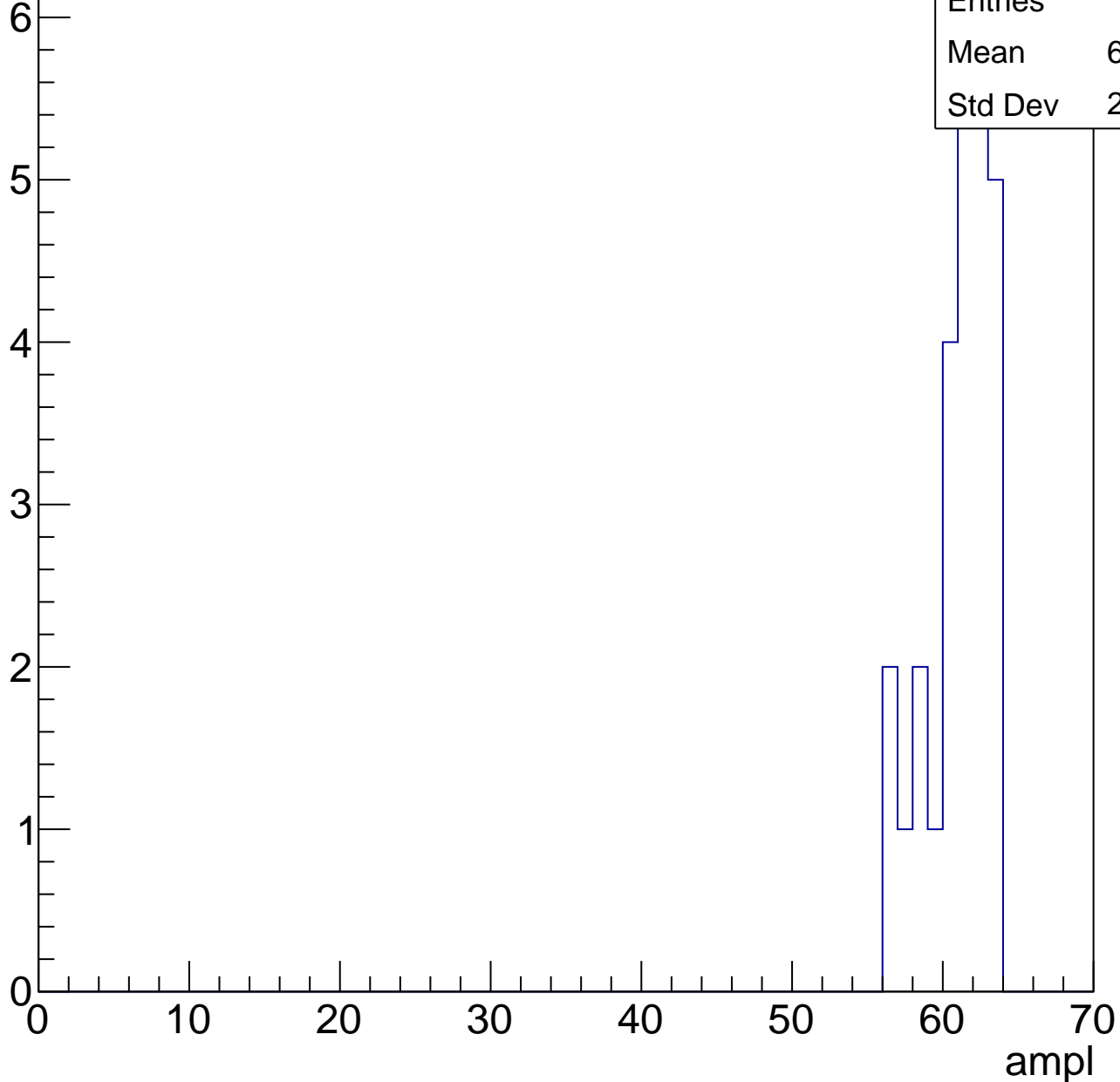
calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U19-ch85, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U19-ch85, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U19-ch85, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U19-ch86, adc0

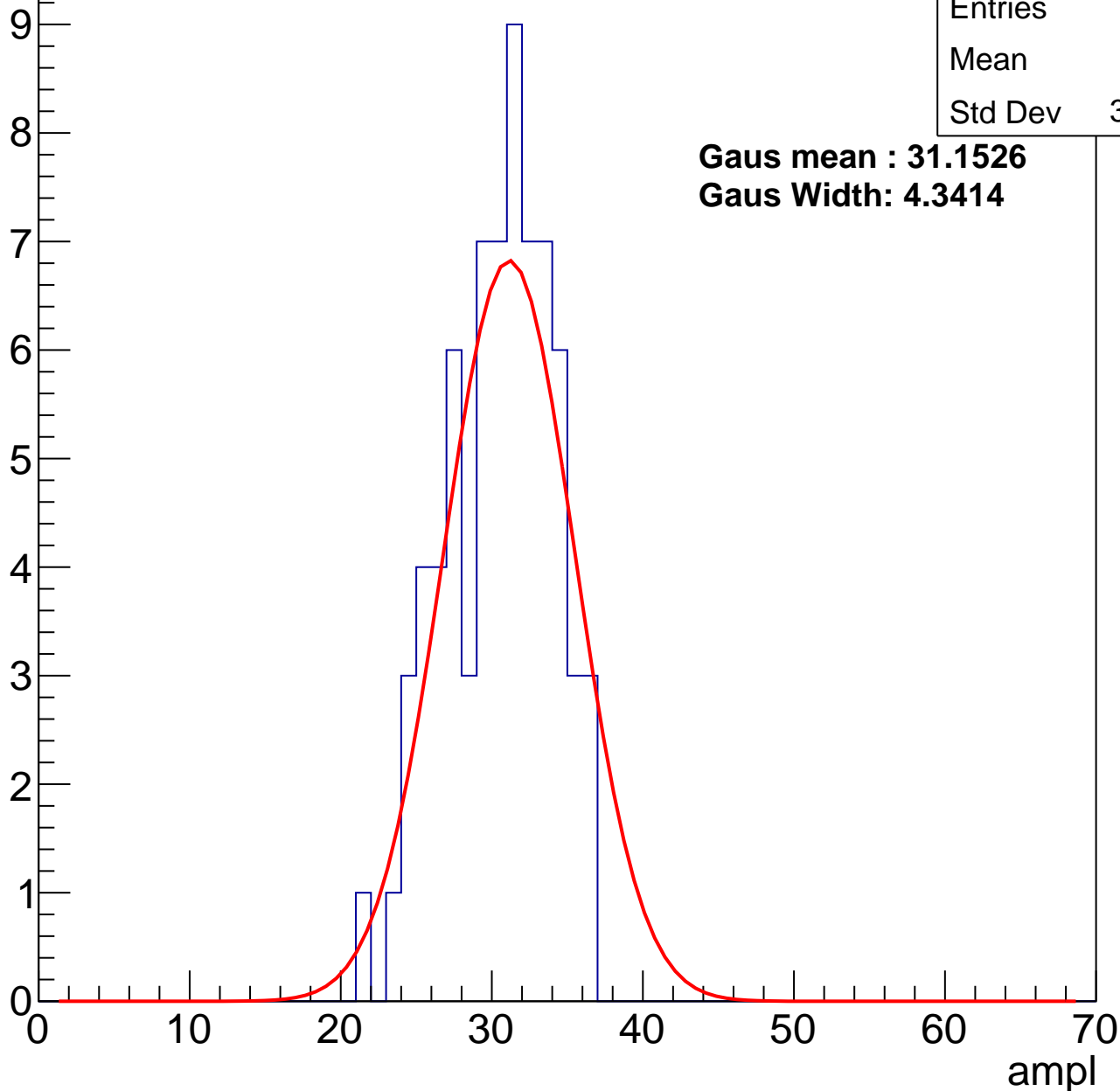
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	71
Mean	30
Std Dev	3.468

**Gaus mean : 31.1526**

**Gaus Width: 4.3414**



# B1L101S, U19-ch86, adc1

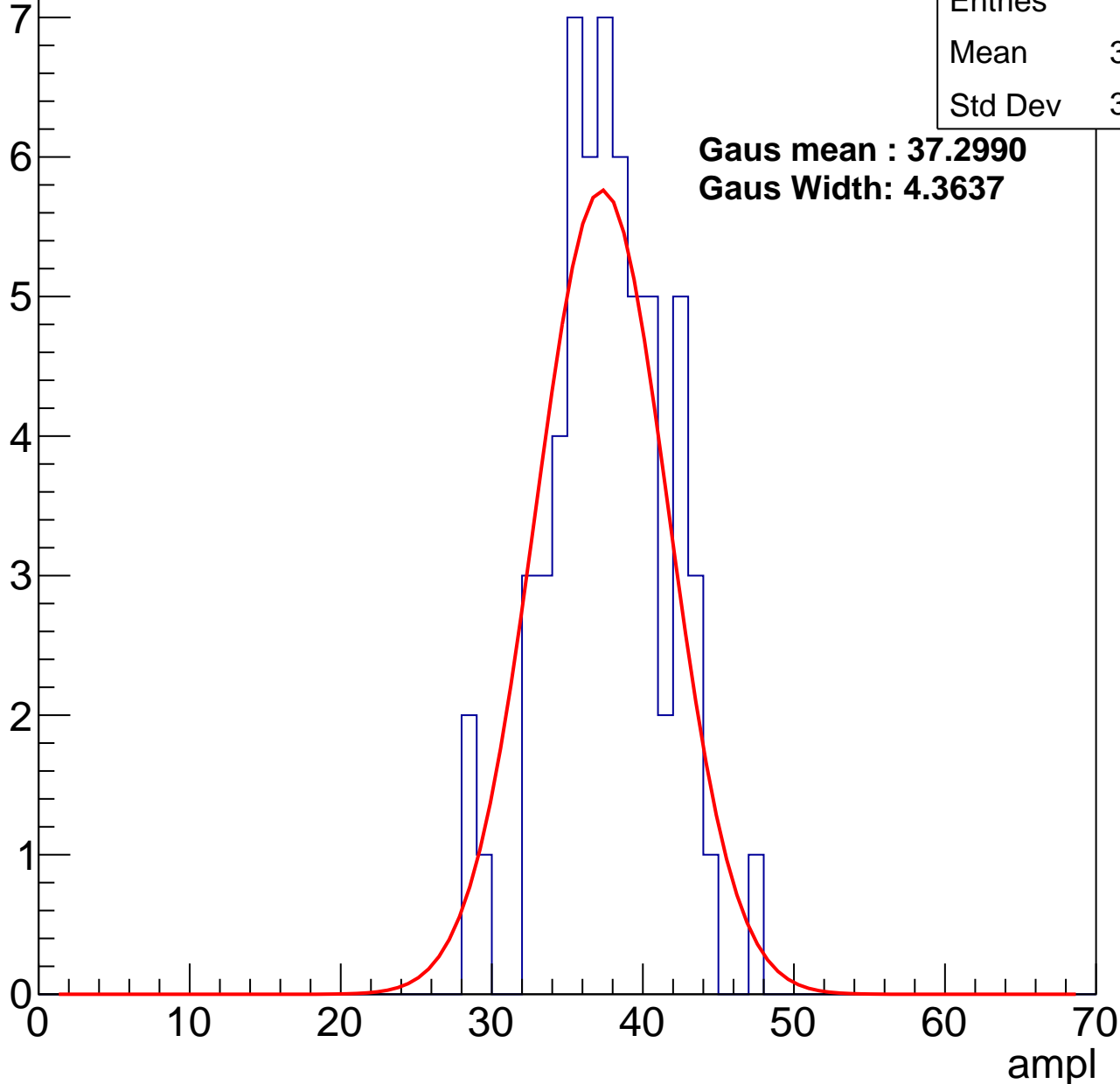
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	37.23
Std Dev	3.843

**Gaus mean : 37.2990**

**Gaus Width: 4.3637**



# B1L101S, U19-ch86, adc2

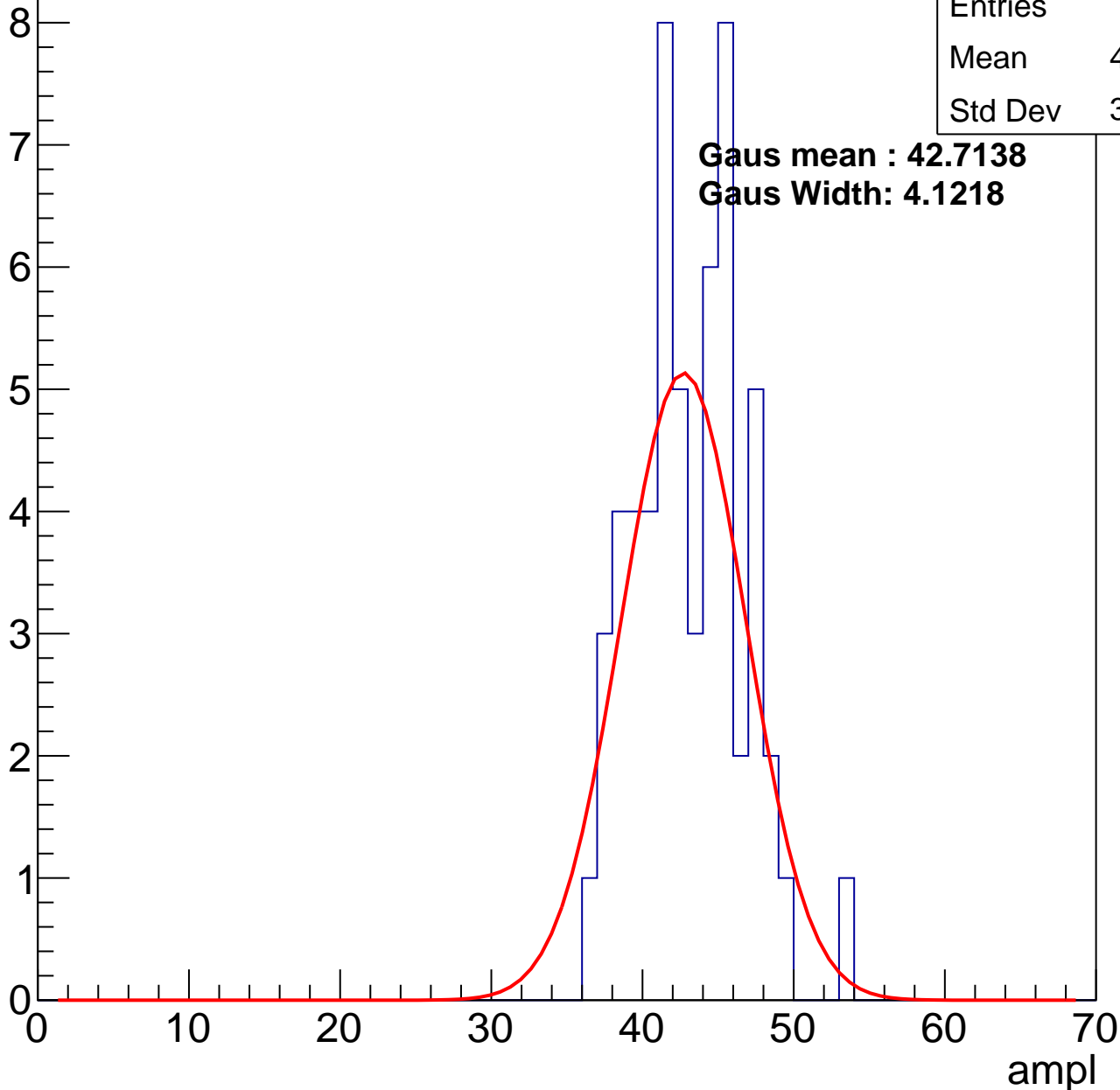
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	57
Mean	42.65
Std Dev	3.527

**Gaus mean : 42.7138**

**Gaus Width: 4.1218**

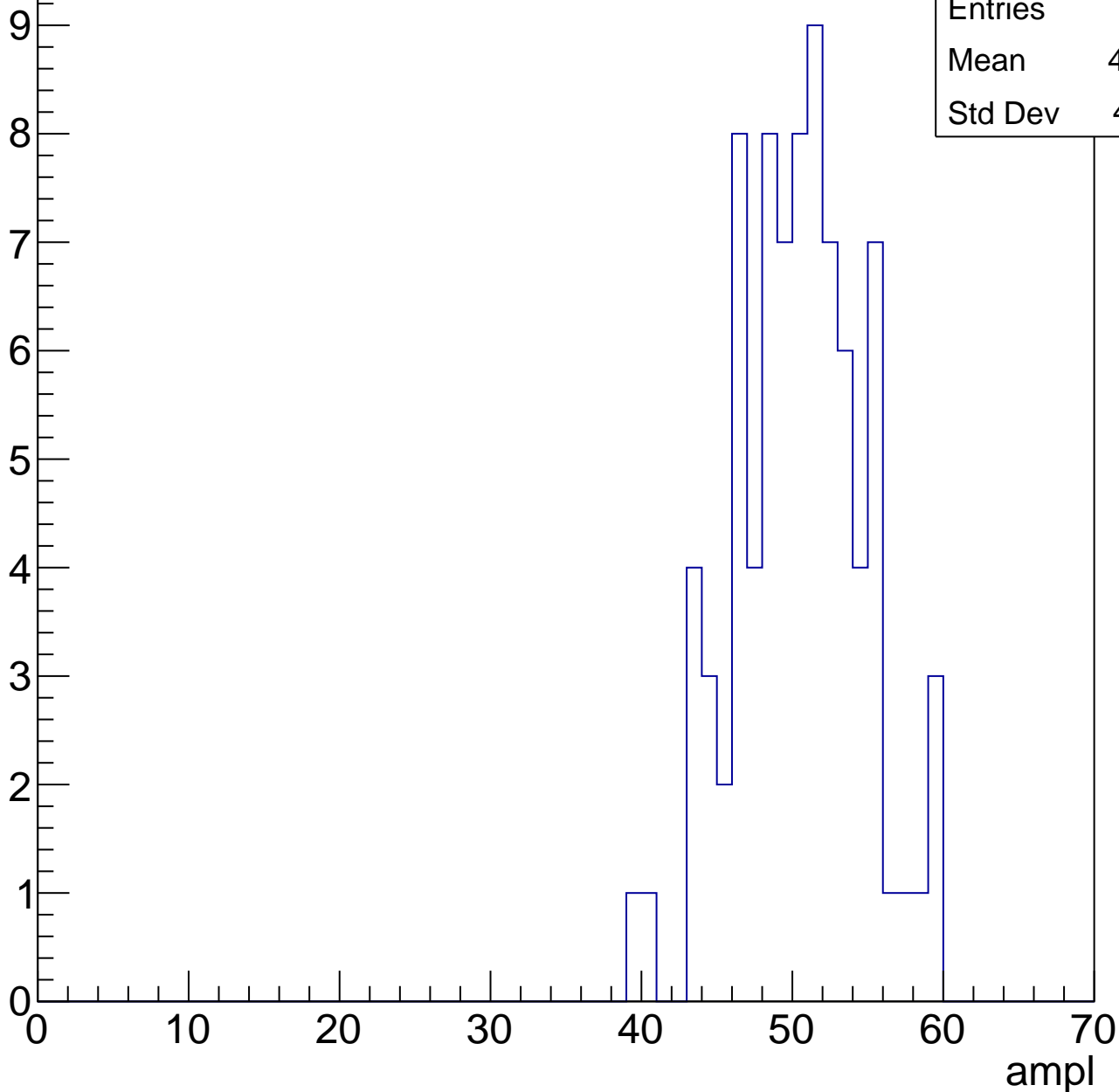


# B1L101S, U19-ch86, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	85
Mean	49.95
Std Dev	4.201

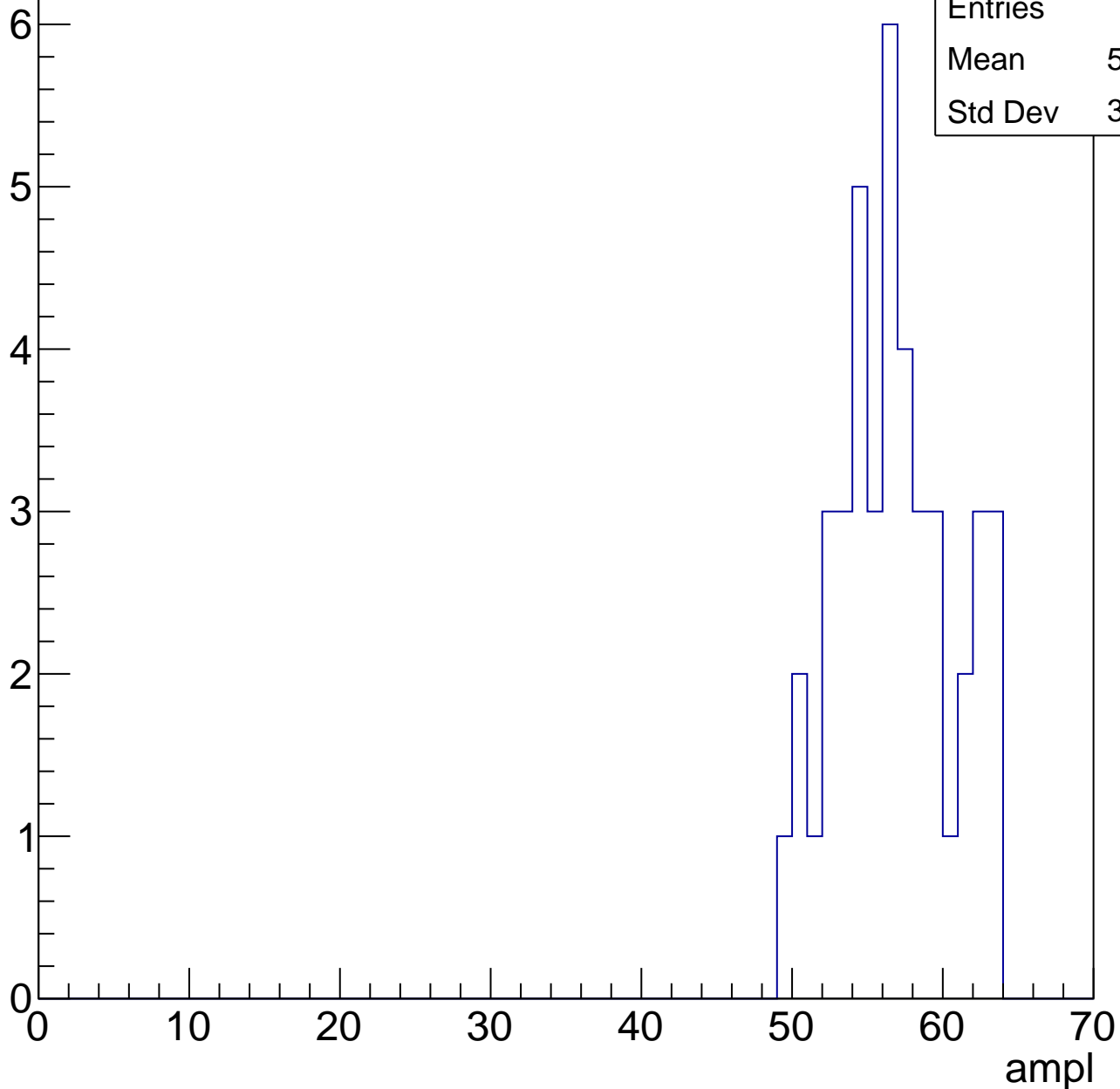


# B1L101S, U19-ch86, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	43
Mean	56.33
Std Dev	3.746

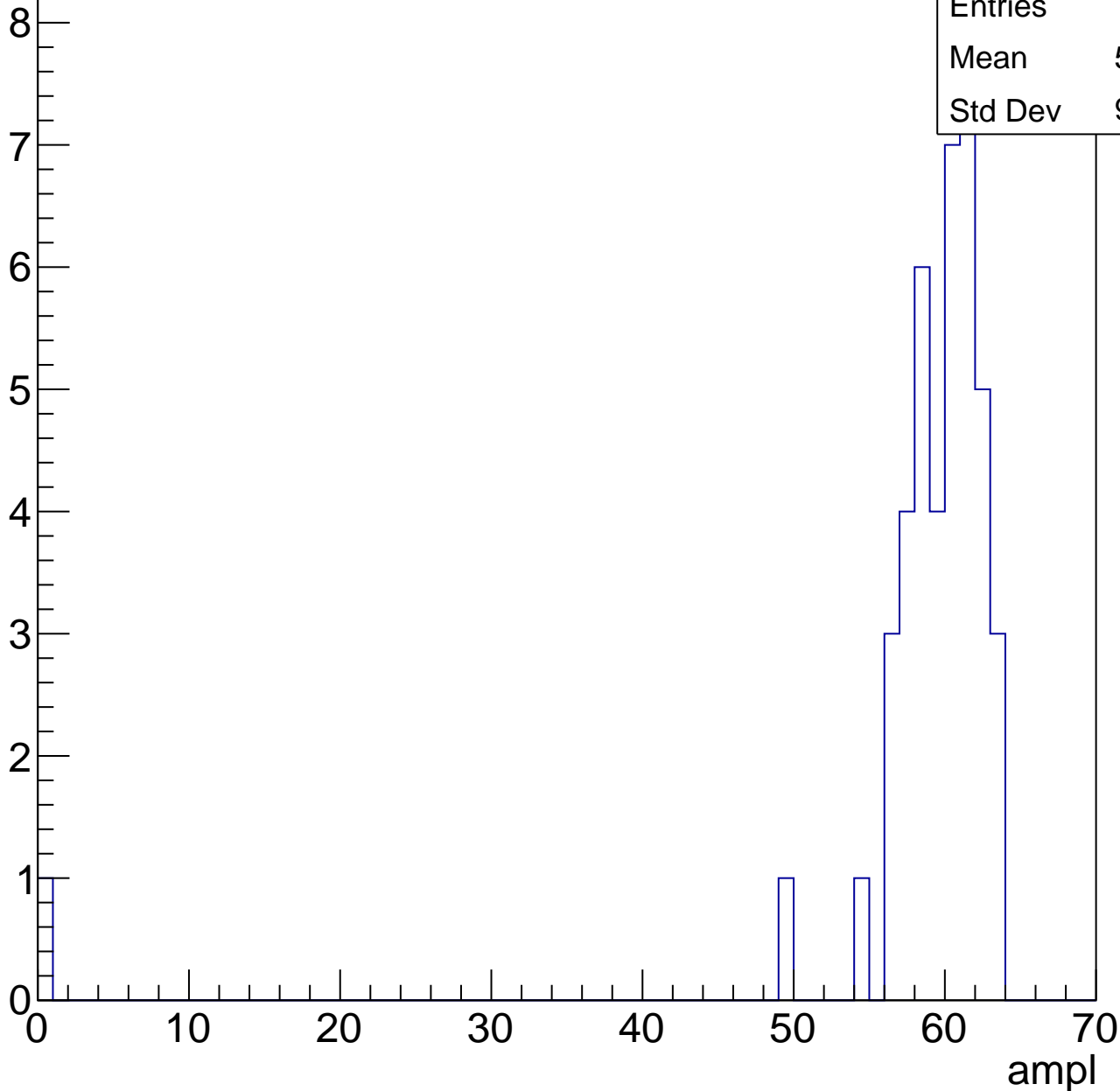


# B1L101S, U19-ch86, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

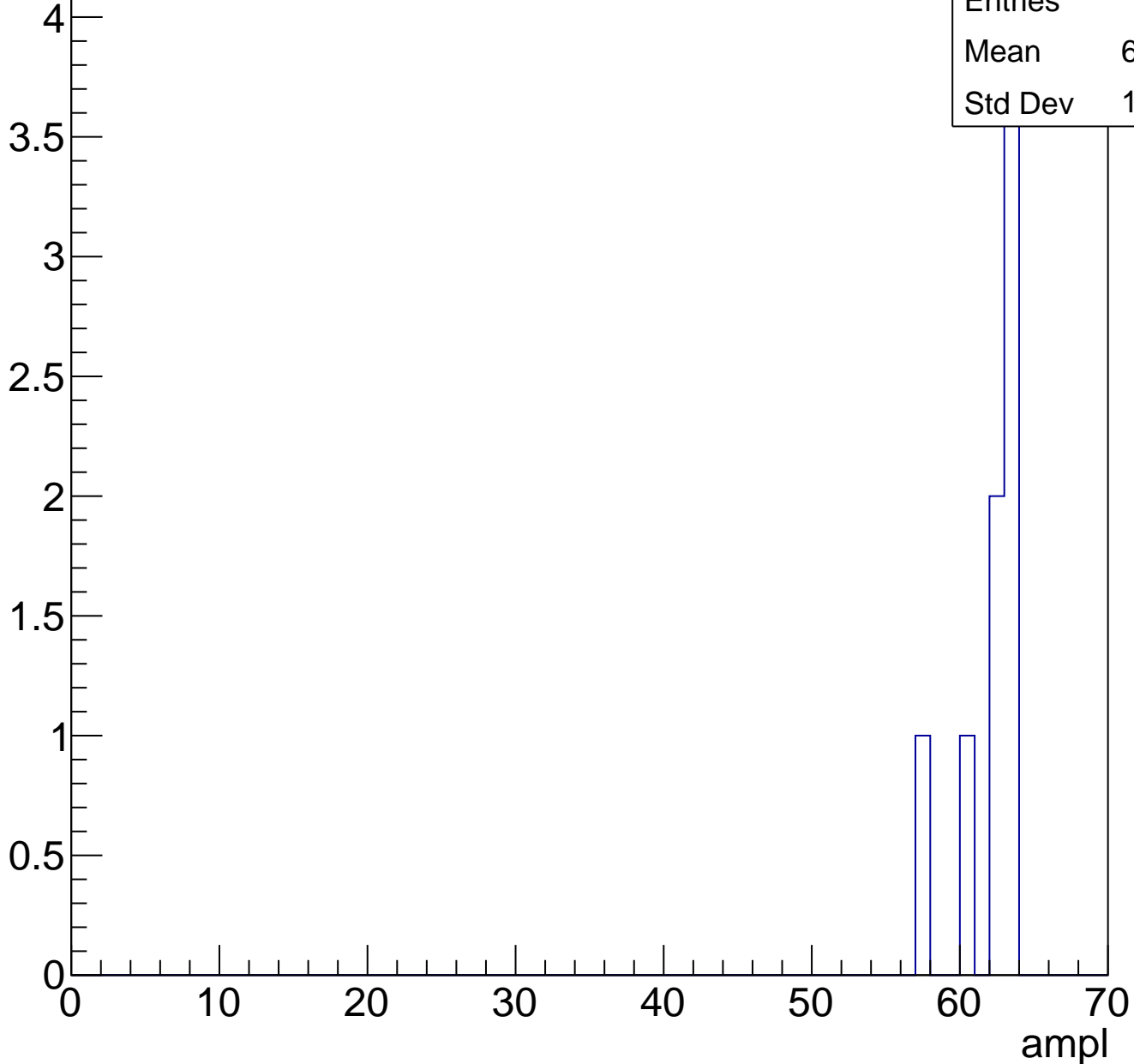
Entries	43
Mean	57.91
Std Dev	9.321



# B1L101S, U19-ch86, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



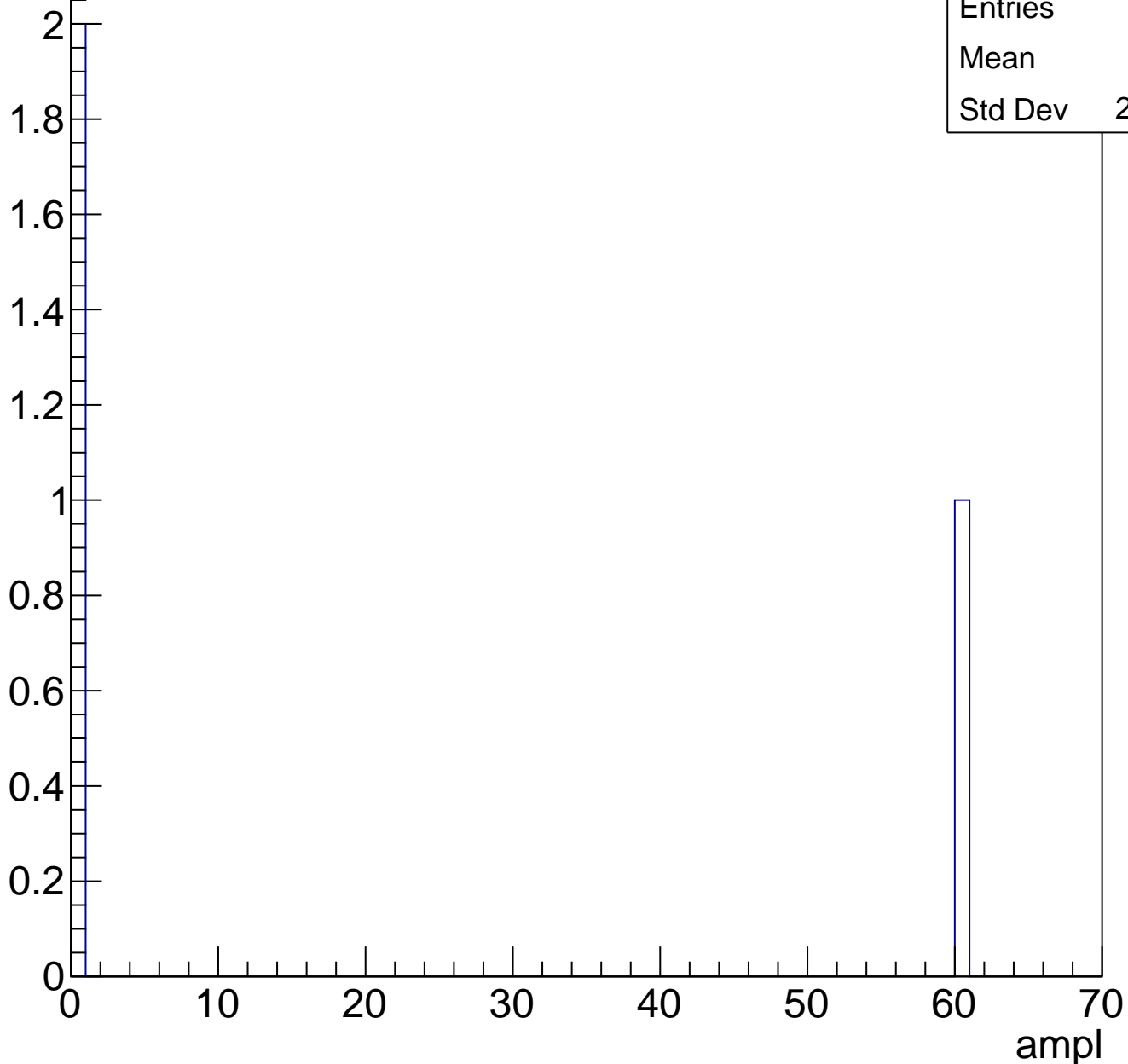
Entries	8
Mean	61.62
Std Dev	1.996



# B1L101S, U19-ch86, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	3
Mean	20
Std Dev	28.28

# B1L101S, U19-ch87, adc0

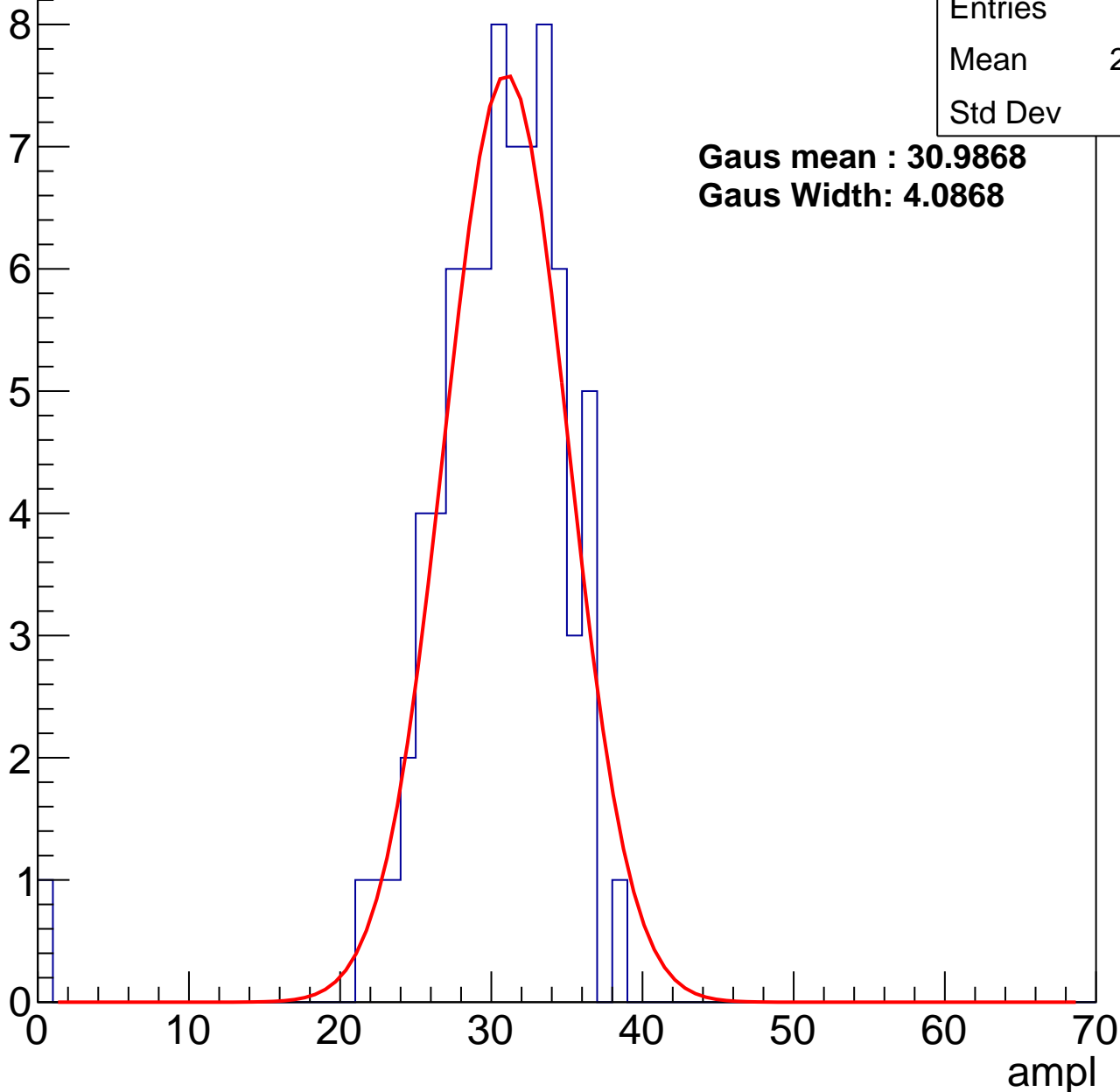
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	77
Mean	29.79
Std Dev	5.01

**Gaus mean : 30.9868**

**Gaus Width: 4.0868**



# B1L101S, U19-ch87, adc1

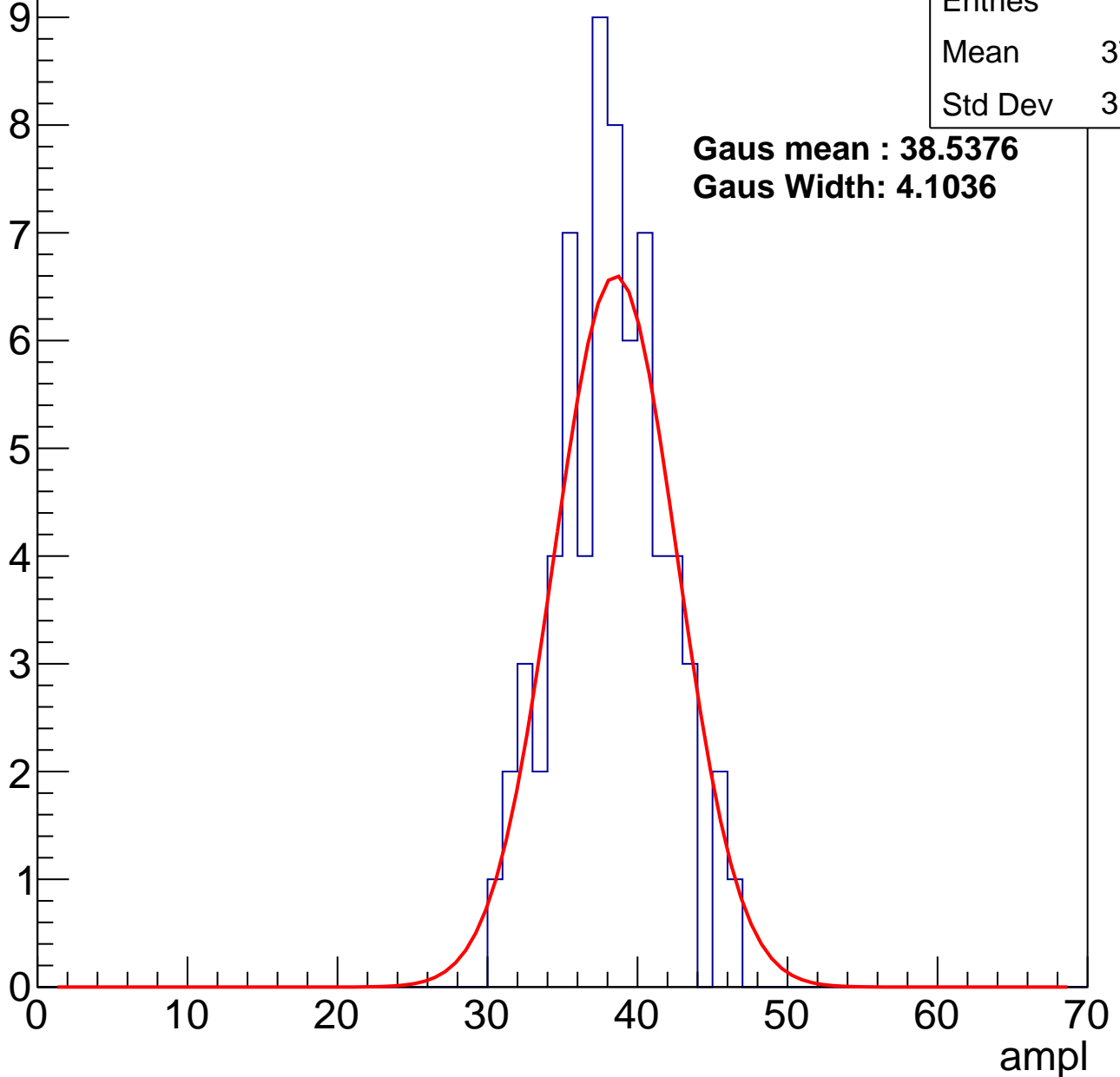
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	67
Mean	37.72
Std Dev	3.536

**Gaus mean : 38.5376**

**Gaus Width: 4.1036**



# B1L101S, U19-ch87, adc2

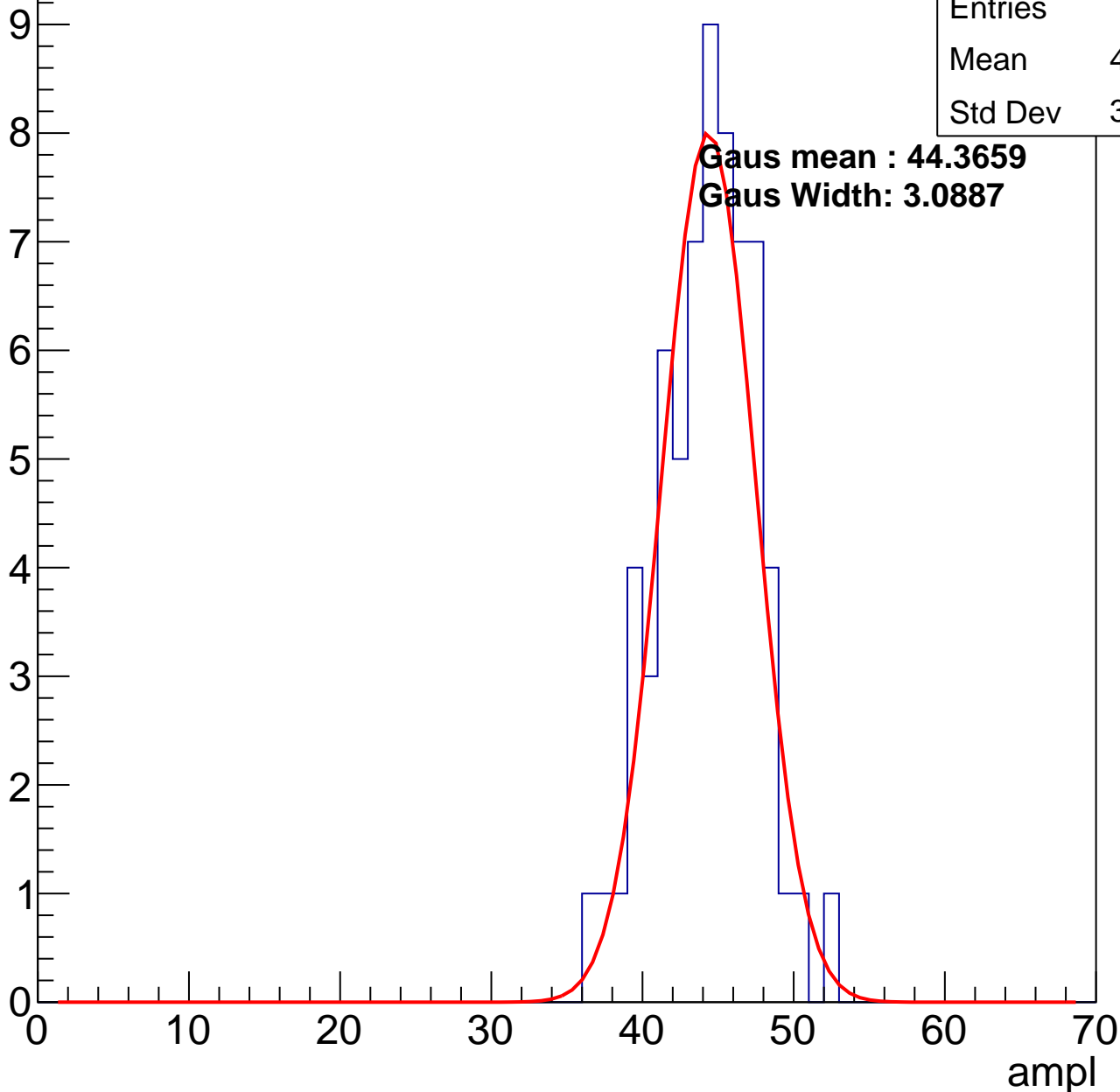
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	66
Mean	43.85
Std Dev	3.173

**Gaus mean : 44.3659**

**Gaus Width: 3.0887**

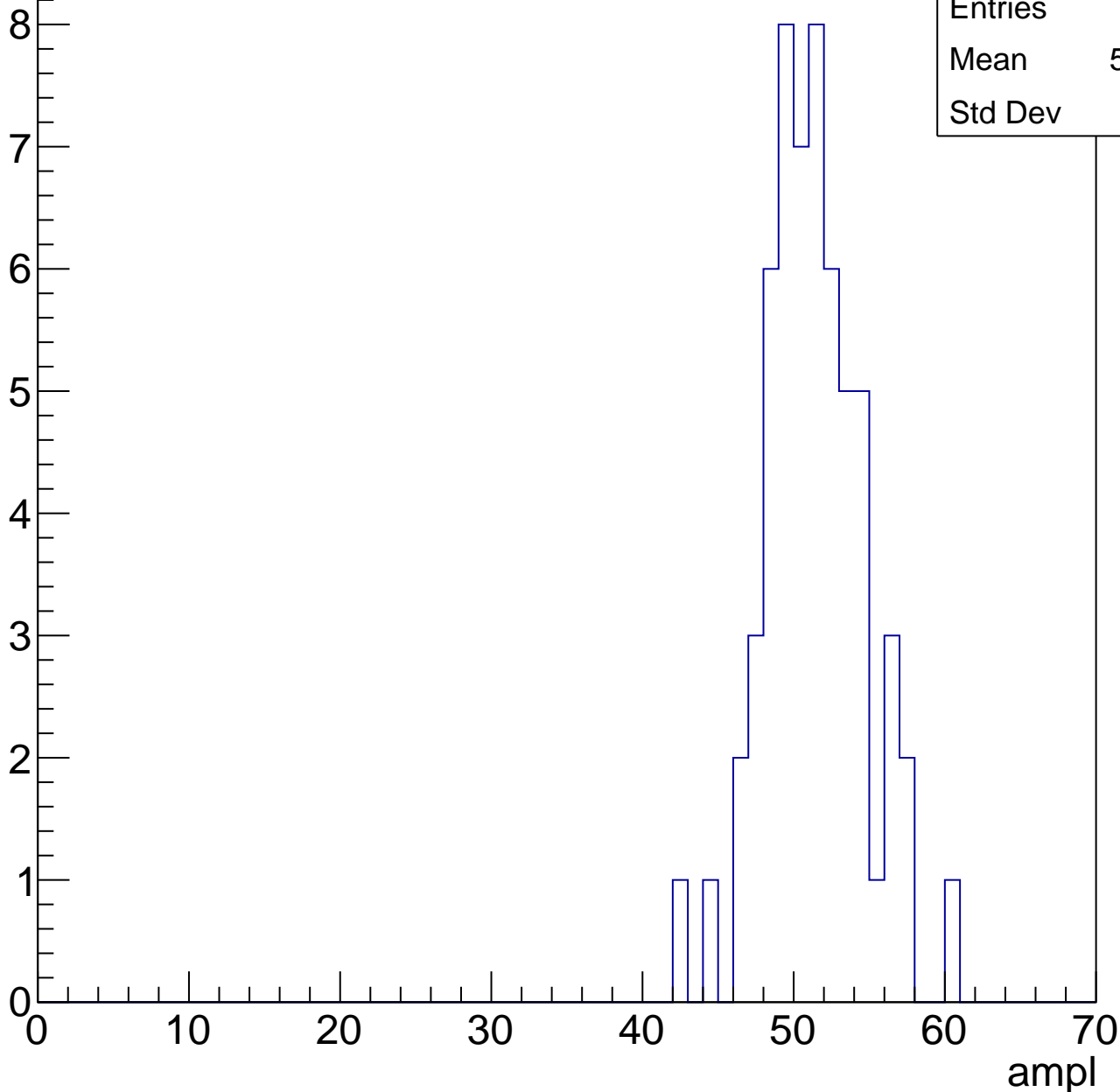


# B1L101S, U19-ch87, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

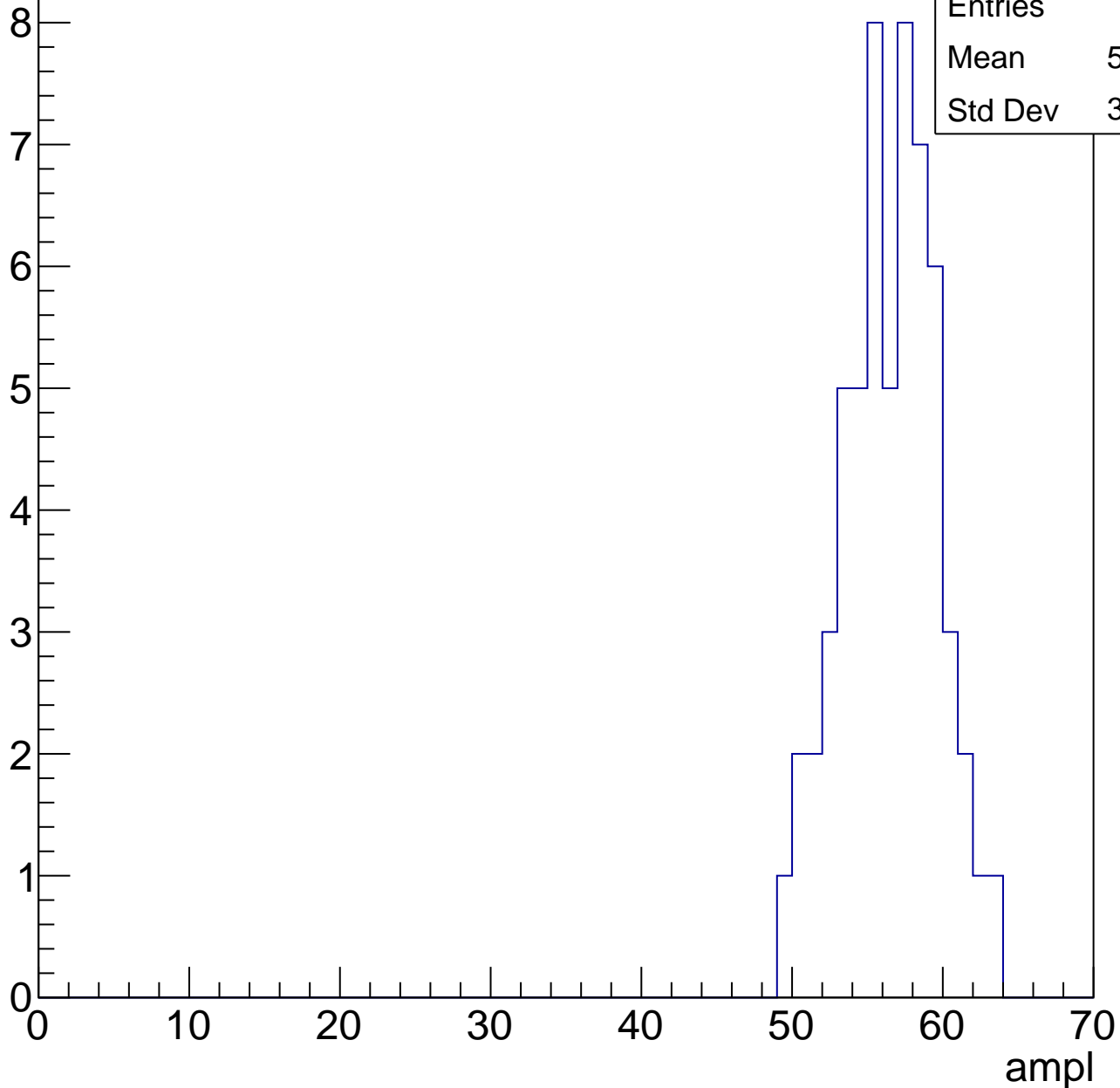
Entries	59
Mean	50.86
Std Dev	3.28



# B1L101S, U19-ch87, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	59
Mean	56.02
Std Dev	3.095

# B1L101S, U19-ch87, adc5

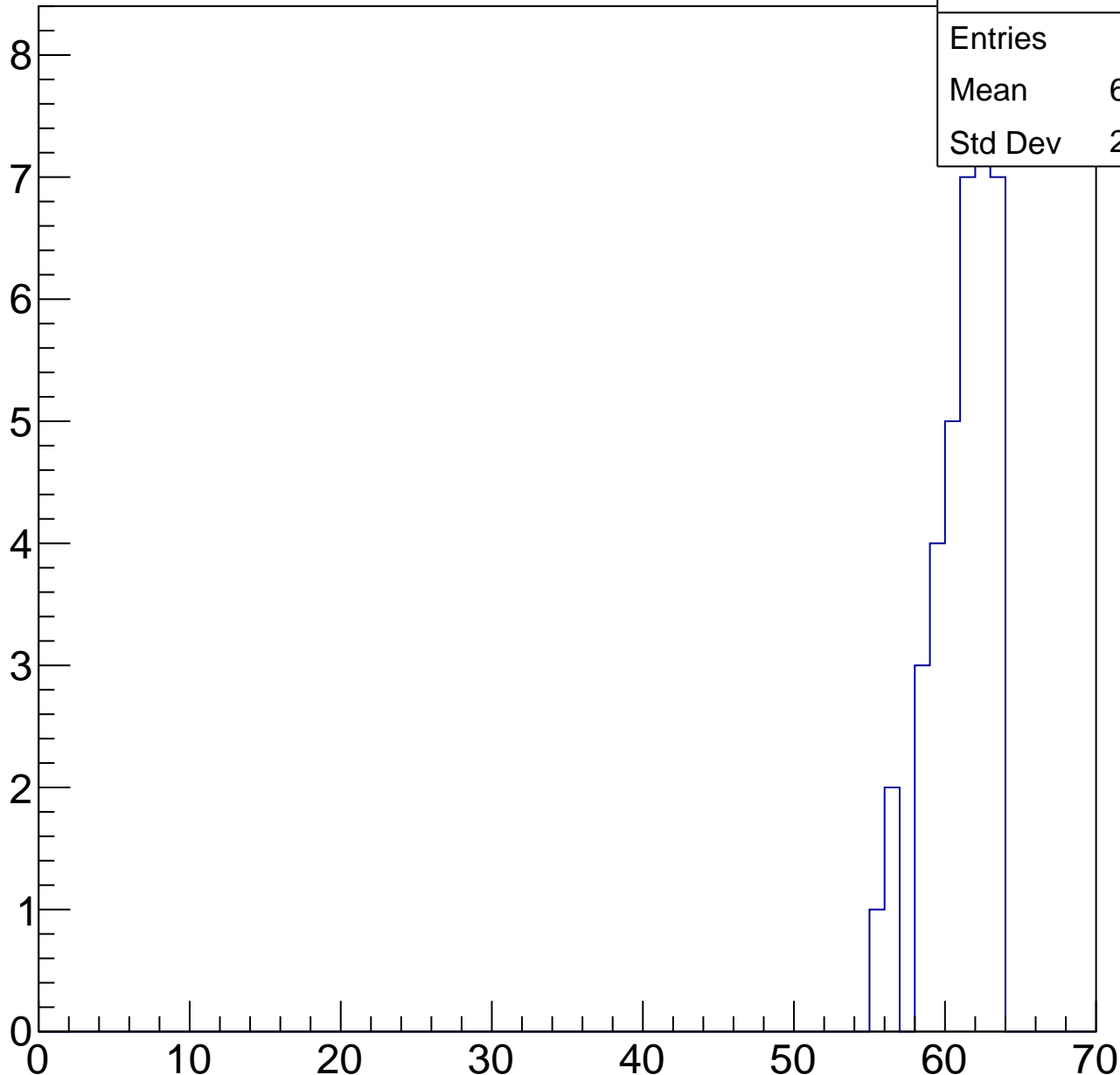
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	37
Mean	60.57
Std Dev	2.099

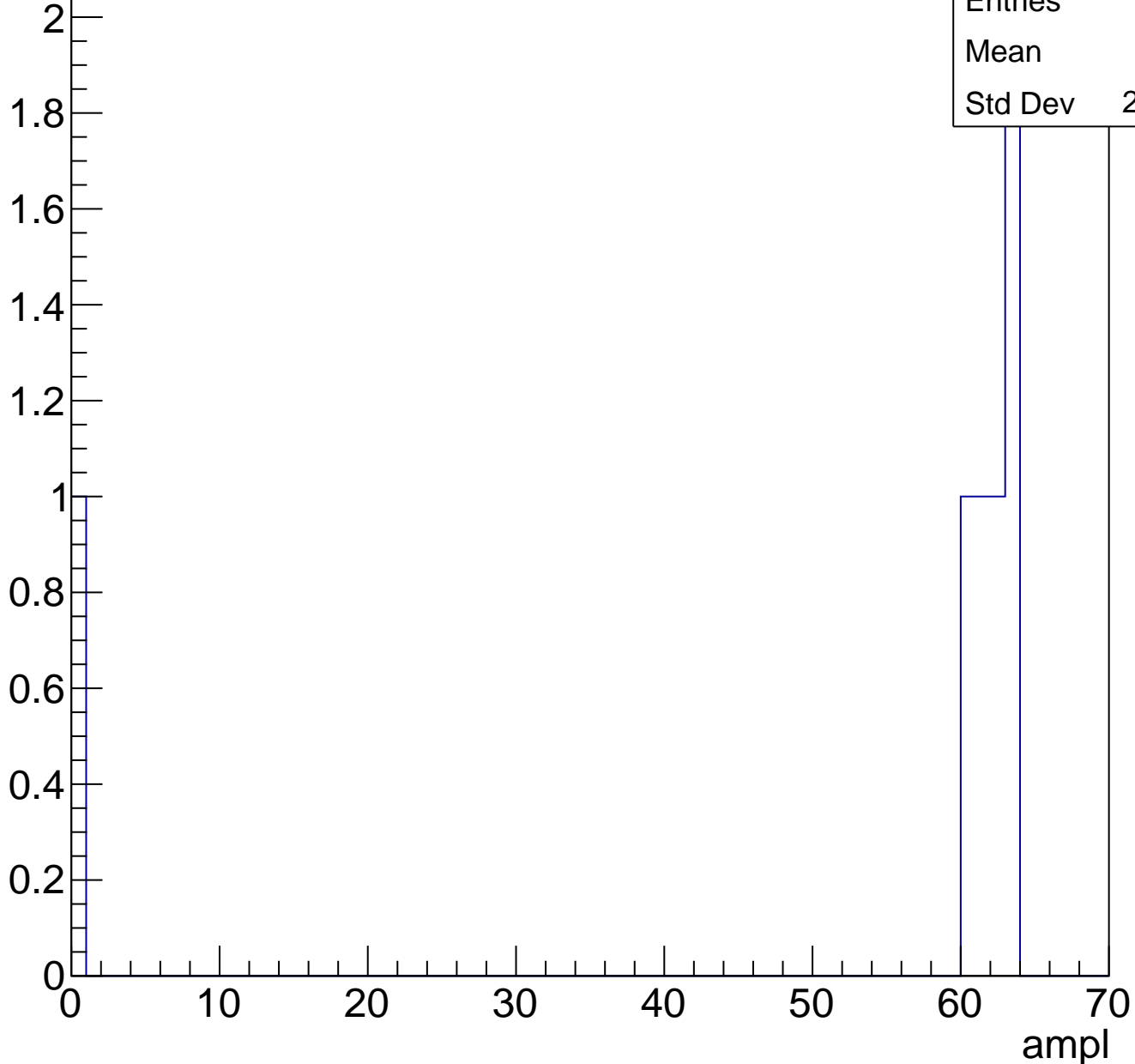
ampl



# B1L101S, U19-ch87, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U19-ch87, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L101S, U19-ch88, adc0

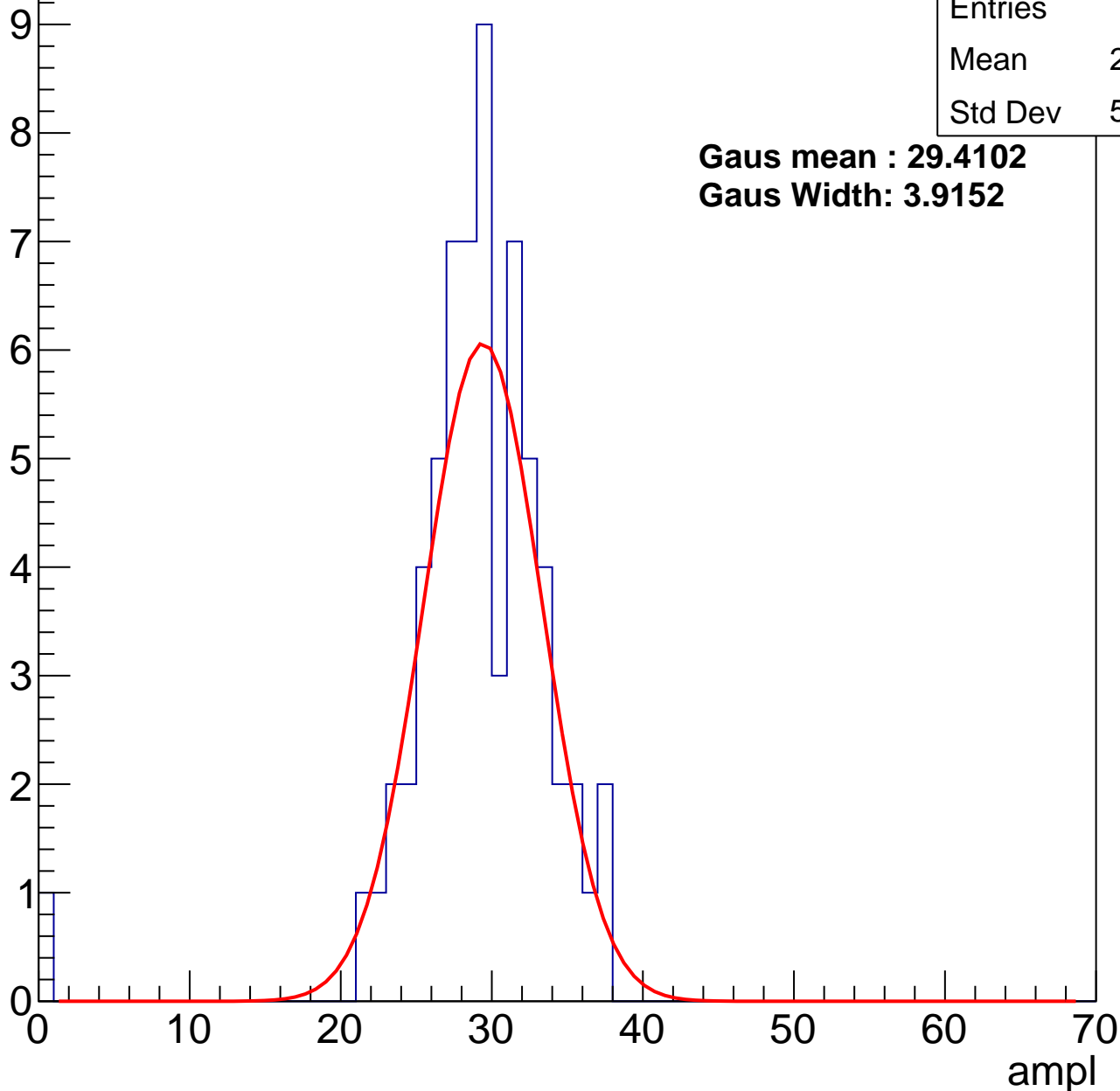
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	28.62
Std Dev	5.037

**Gaus mean : 29.4102**

**Gaus Width: 3.9152**



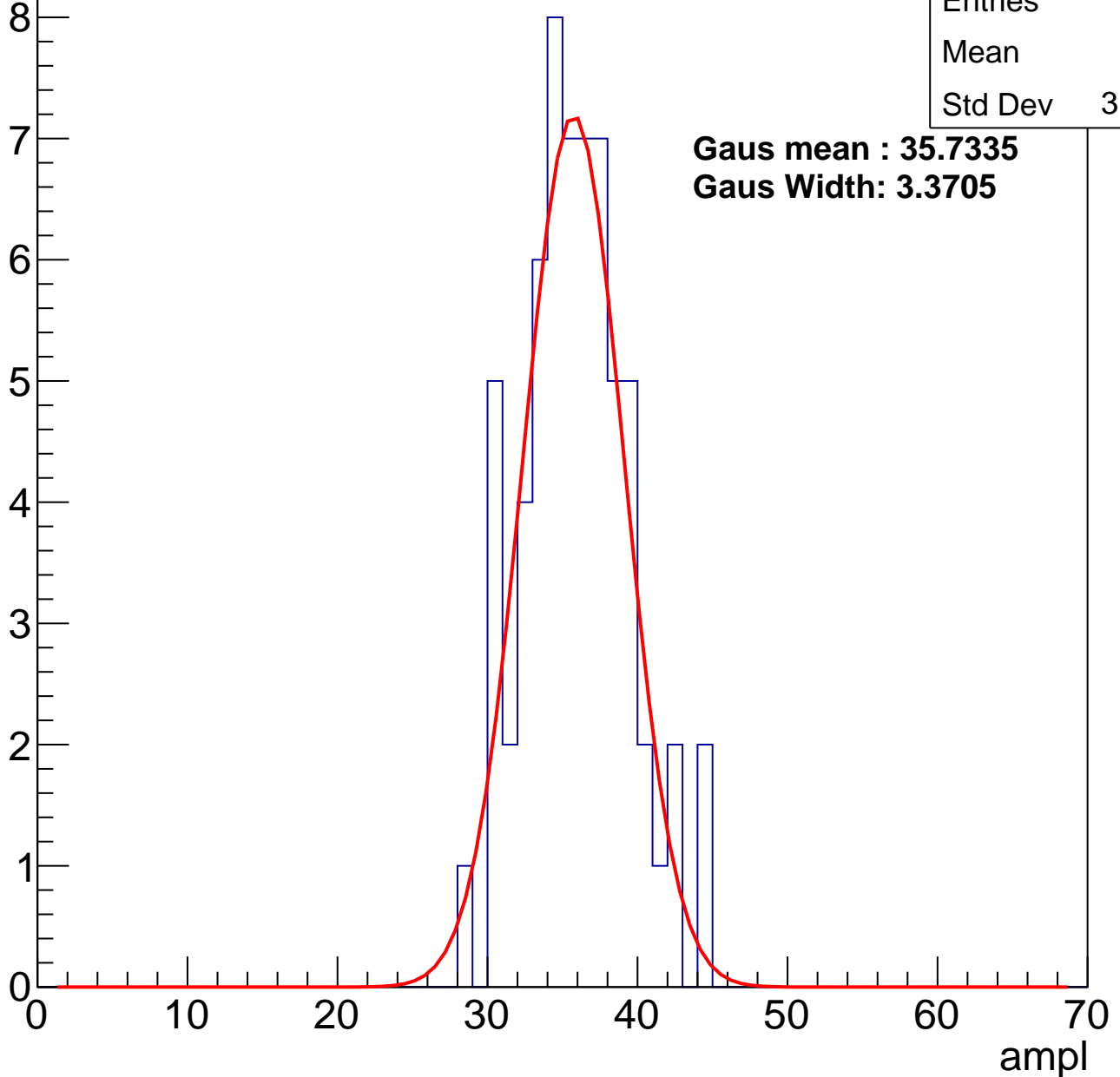
# B1L101S, U19-ch88, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	35.5
Std Dev	3.455

**Gaus mean : 35.7335**  
**Gaus Width: 3.3705**



# B1L101S, U19-ch88, adc2

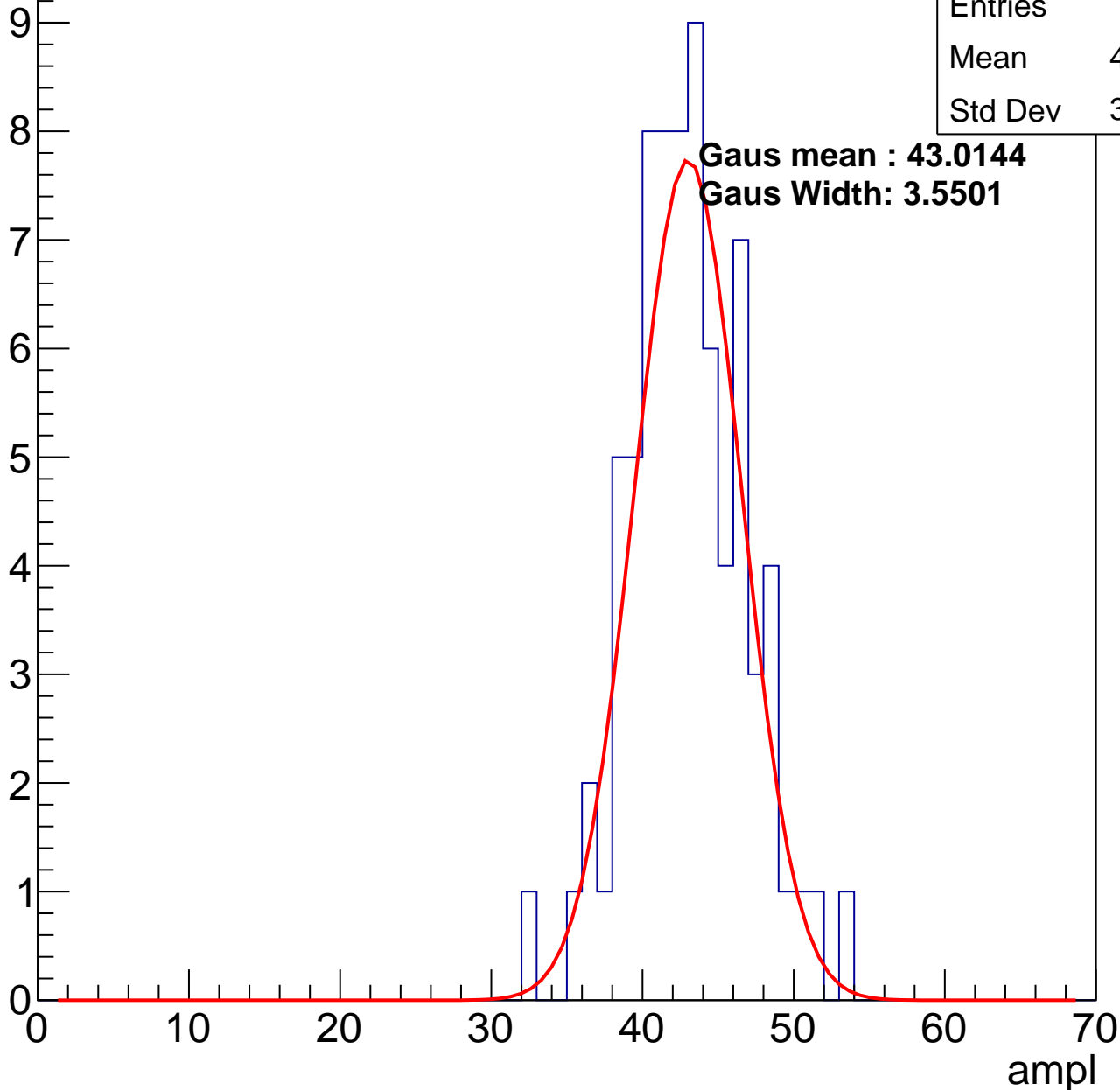
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	76
Mean	42.55
Std Dev	3.809

**Gaus mean : 43.0144**

**Gaus Width: 3.5501**

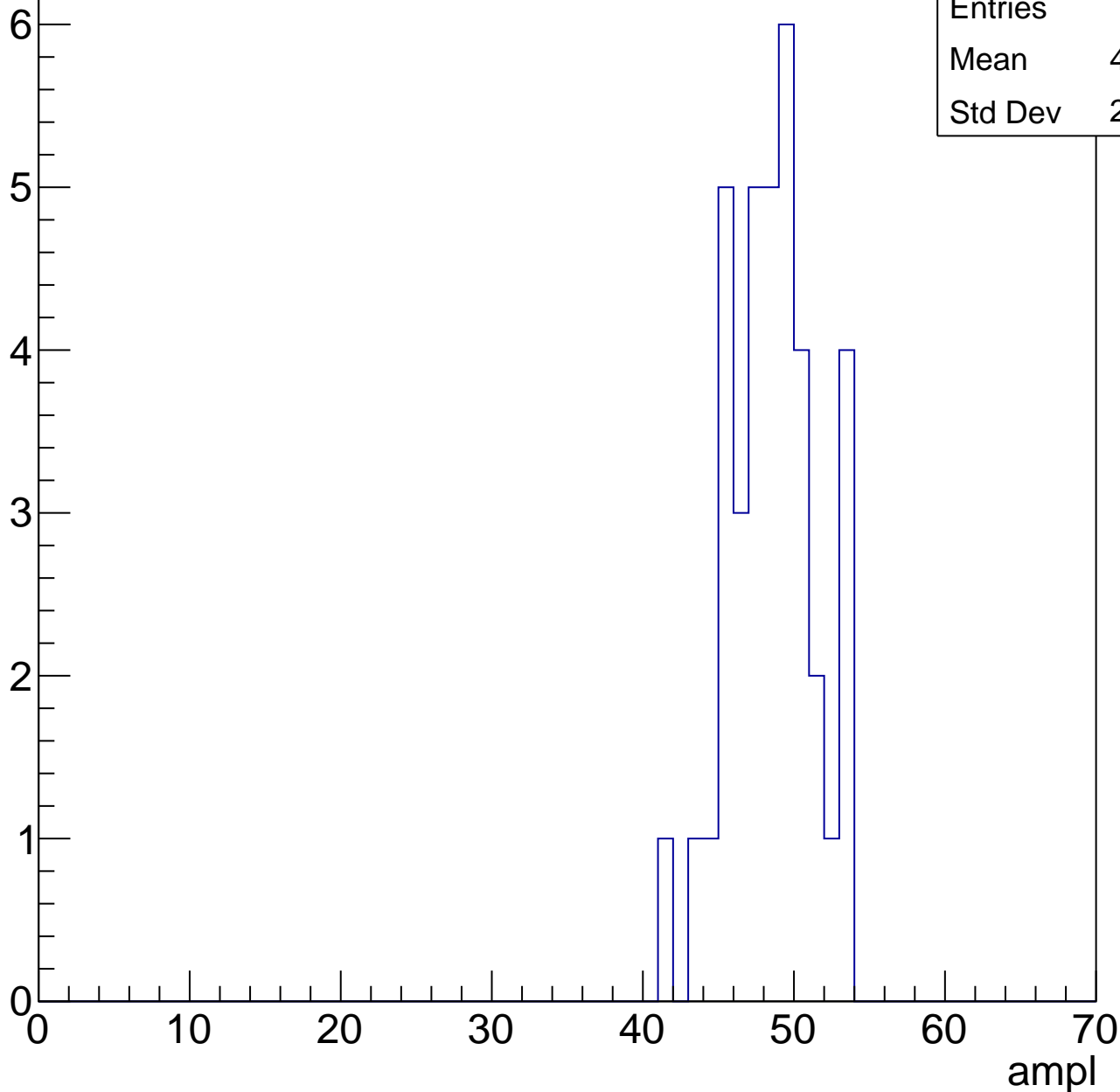


# B1L101S, U19-ch88, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	38
Mean	48.05
Std Dev	2.846

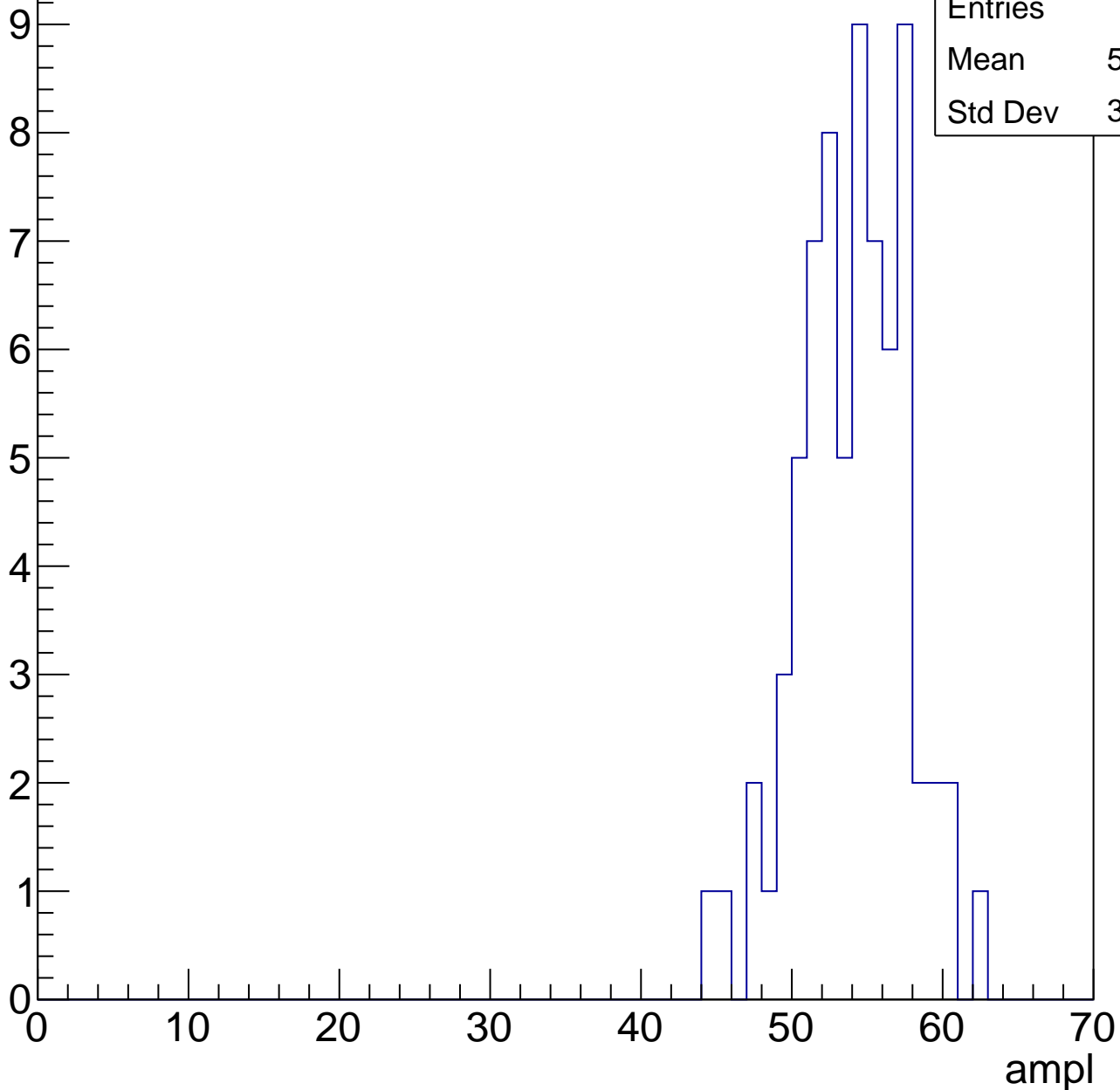


# B1L101S, U19-ch88, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

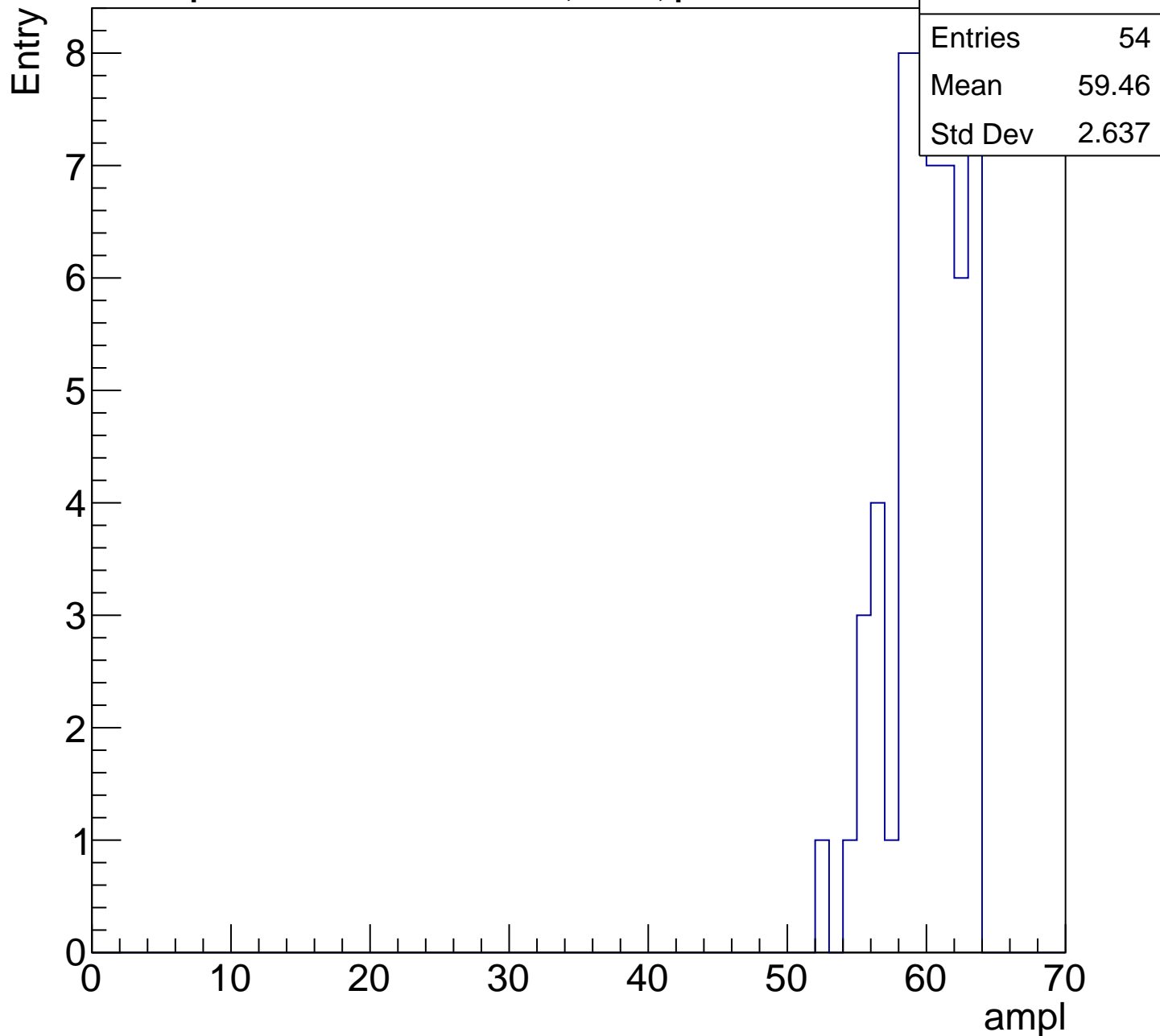
Entry

Entries	71
Mean	53.55
Std Dev	3.532



# B1L101S, U19-ch88, adc5

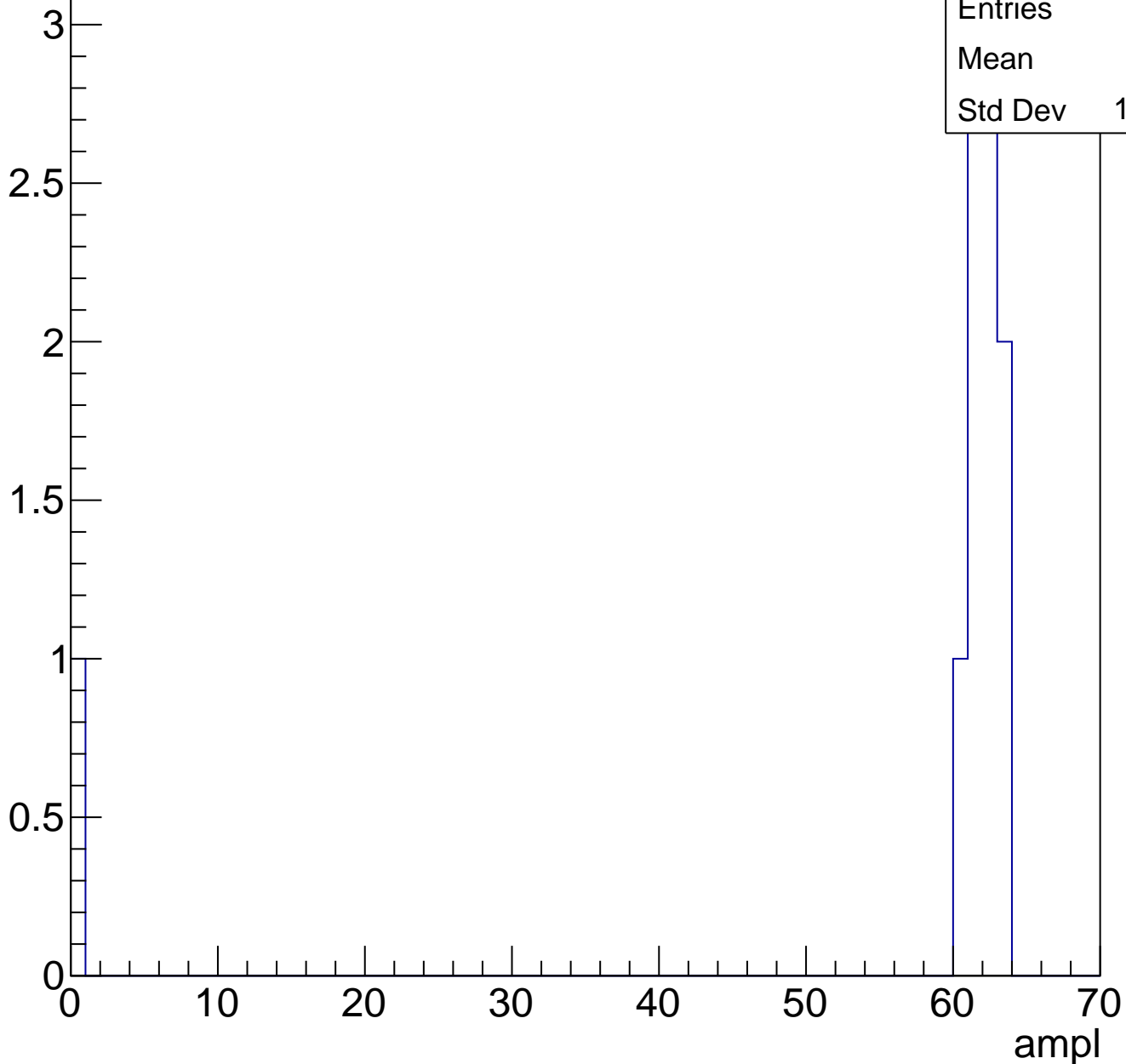
calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U19-ch88, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U19-ch88, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L101S, U19-ch89, adc0

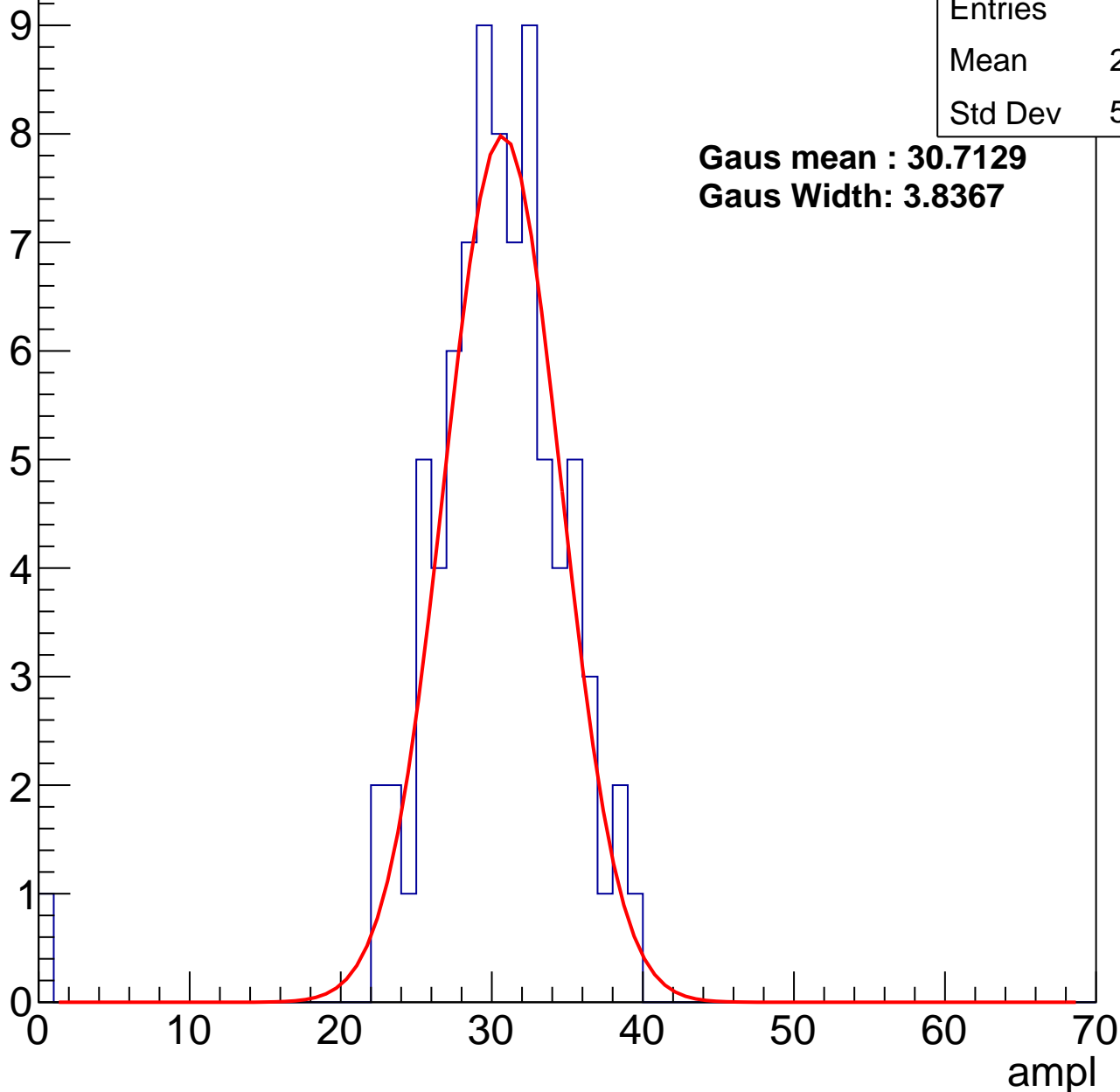
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	82
Mean	29.79
Std Dev	5.038

**Gaus mean : 30.7129**

**Gaus Width: 3.8367**



# B1L101S, U19-ch89, adc1

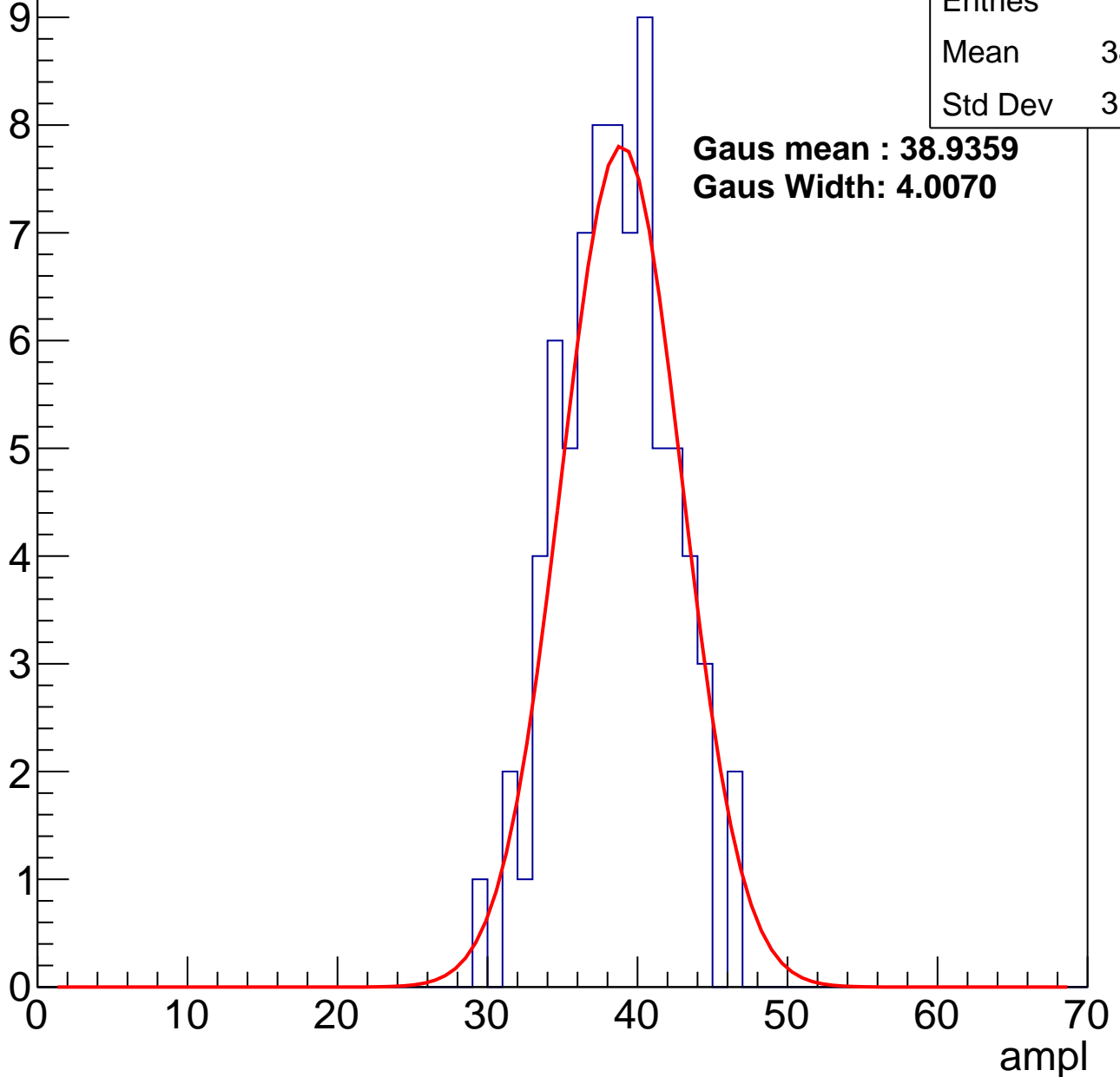
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	77
Mean	38.05
Std Dev	3.596

**Gaus mean : 38.9359**

**Gaus Width: 4.0070**



# B1L101S, U19-ch89, adc2

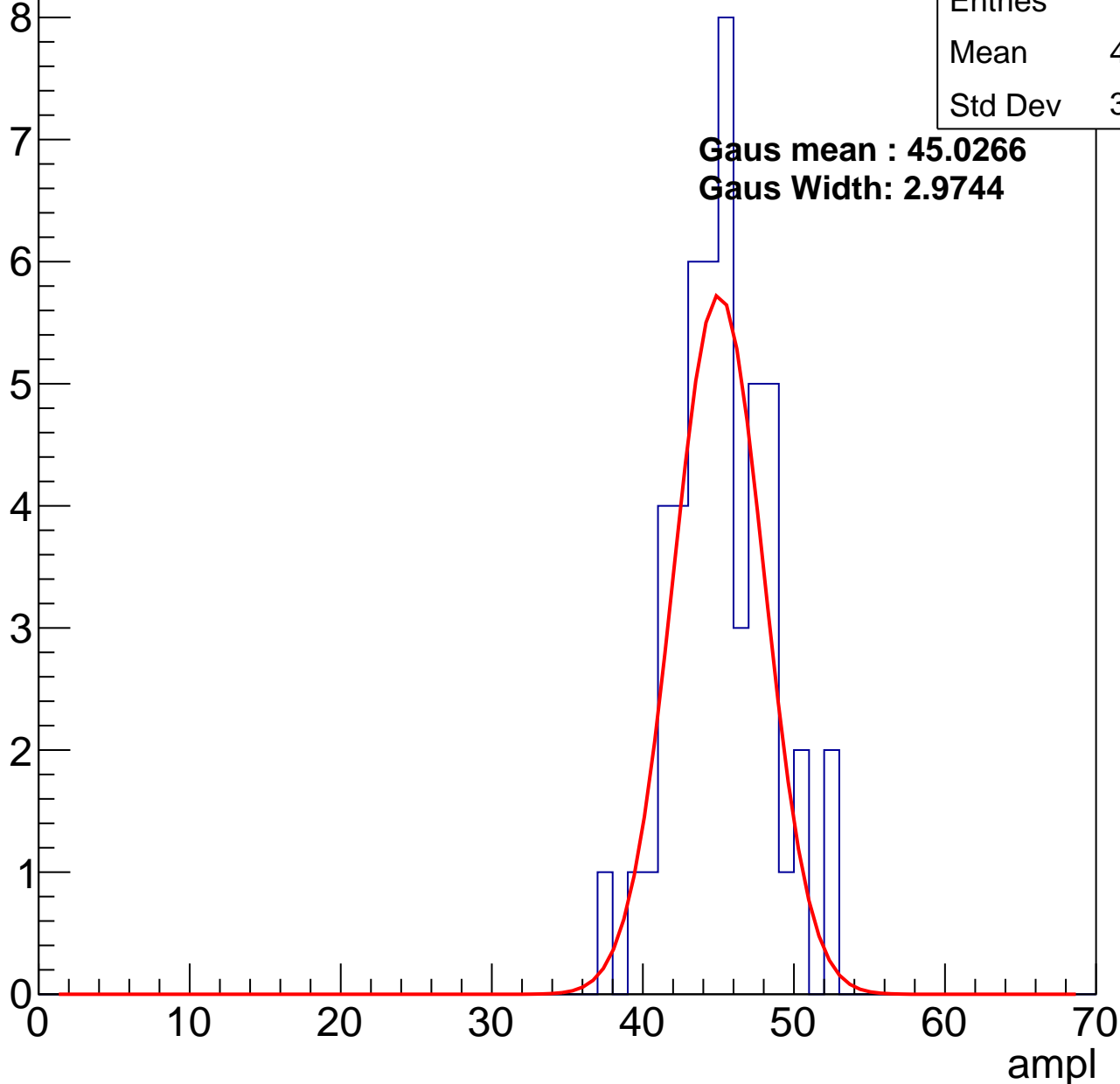
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	49
Mean	44.82
Std Dev	3.147

**Gaus mean : 45.0266**

**Gaus Width: 2.9744**

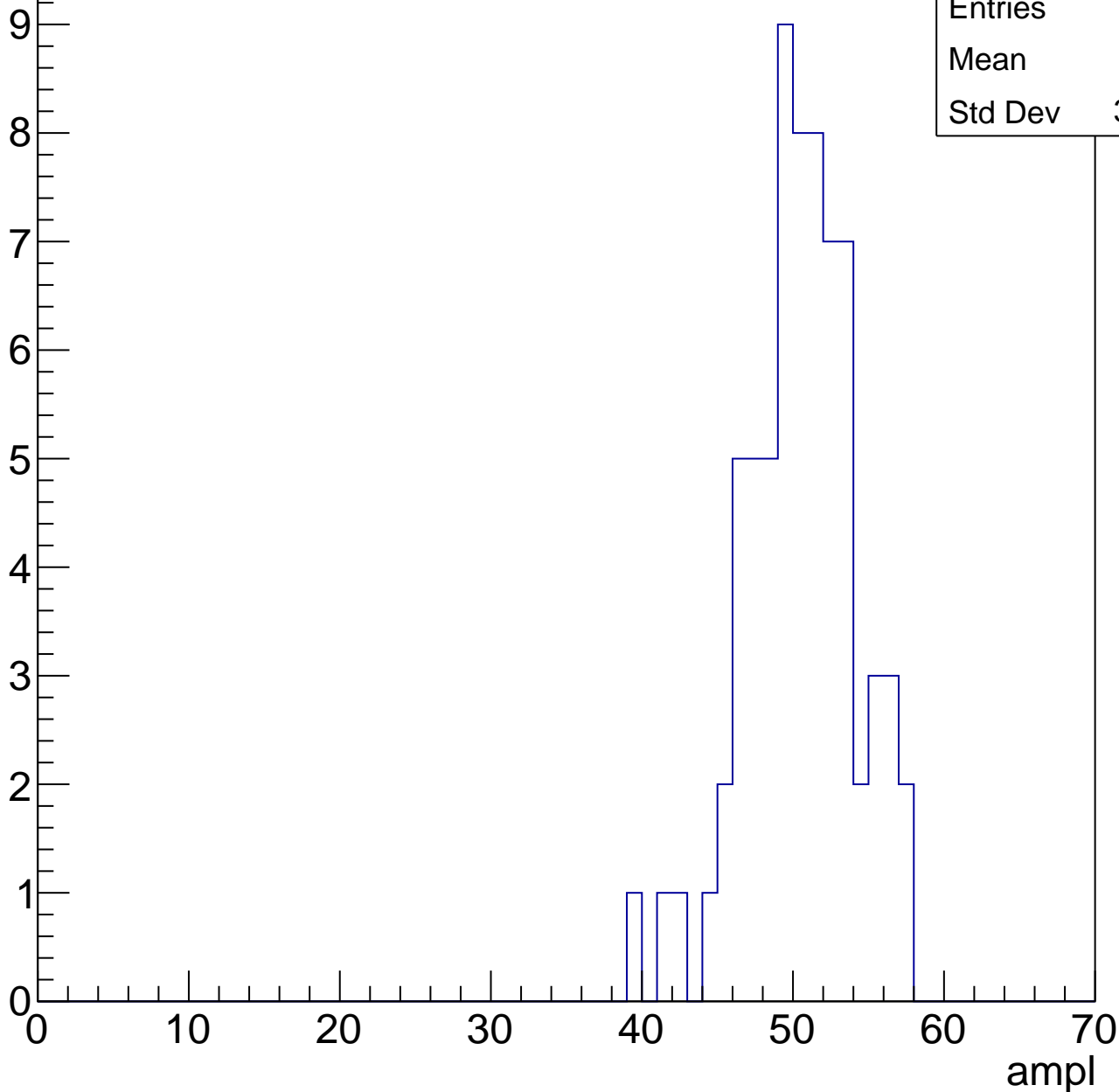


# B1L101S, U19-ch89, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	50
Std Dev	3.621

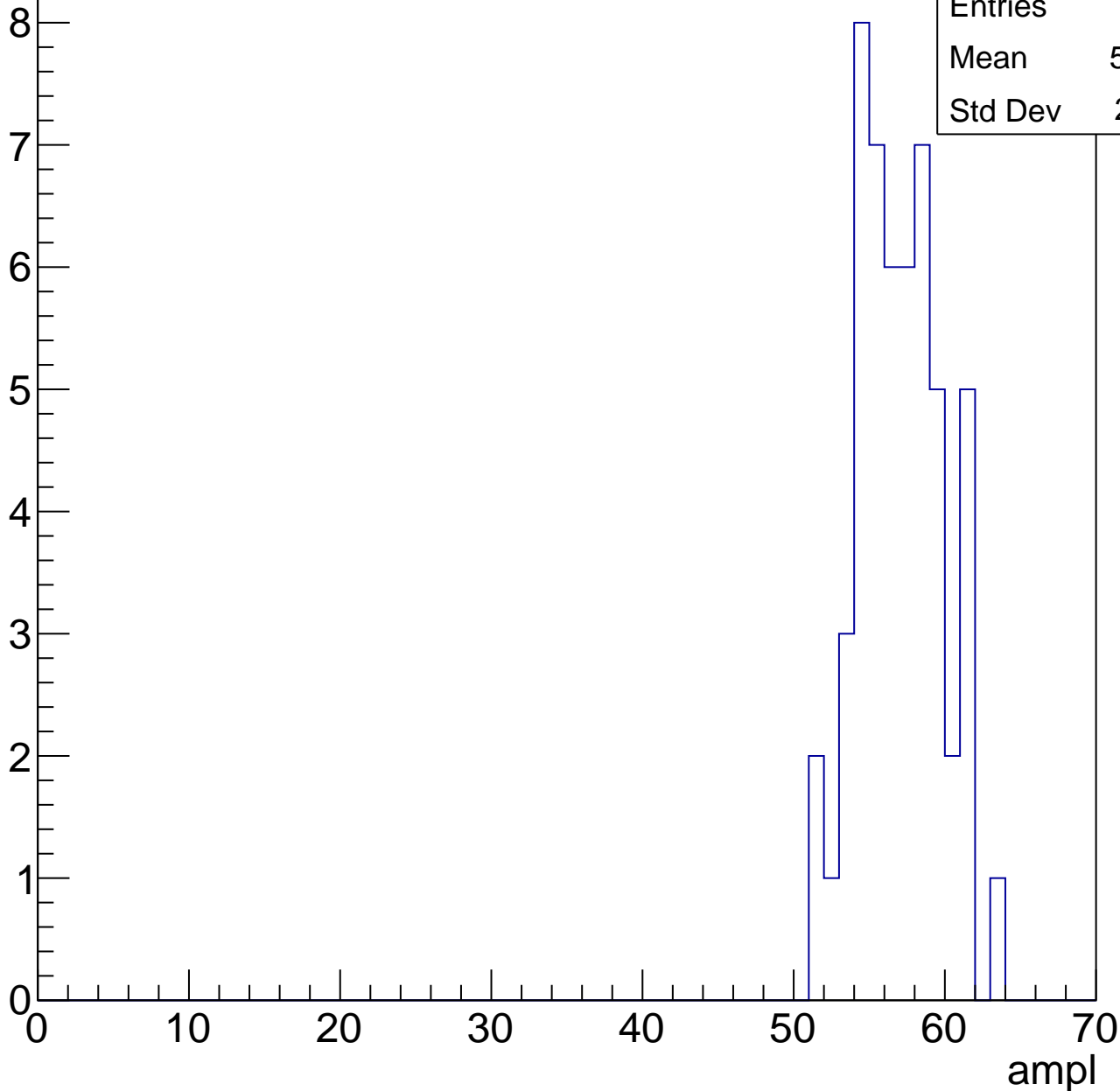


# B1L101S, U19-ch89, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

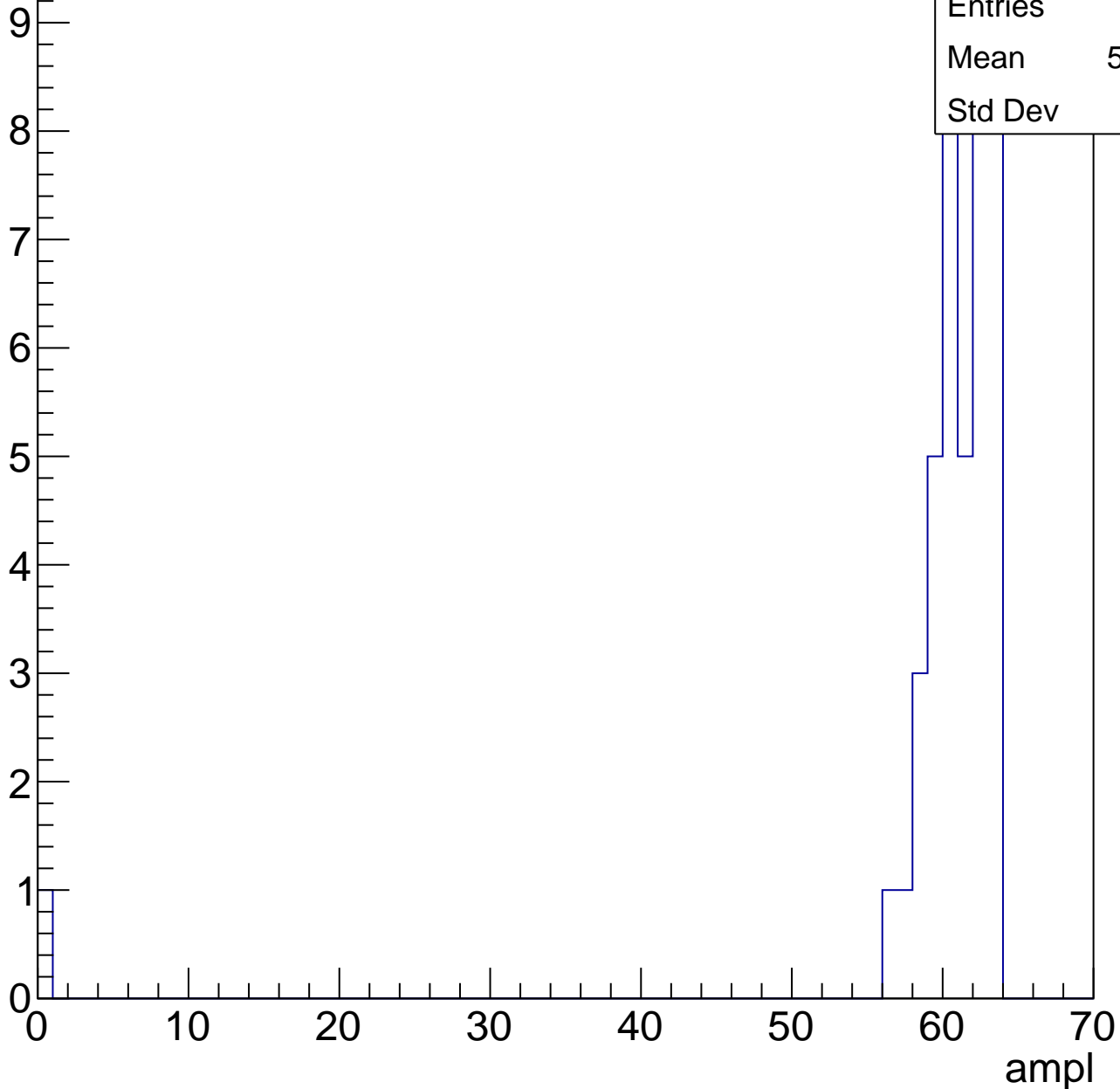
Entries	53
Mean	56.55
Std Dev	2.751



# B1L101S, U19-ch89, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	41
Mean	59.24
Std Dev	9.54

# B1L101S, U19-ch89, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

1

0.8

0.6

0.4

0.2

0

0

10

20

30

40

50

60

70

ampl

Entries

3

Mean

60.67

Std Dev

2.625



# B1L101S, U19-ch89, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U19-ch90, adc0

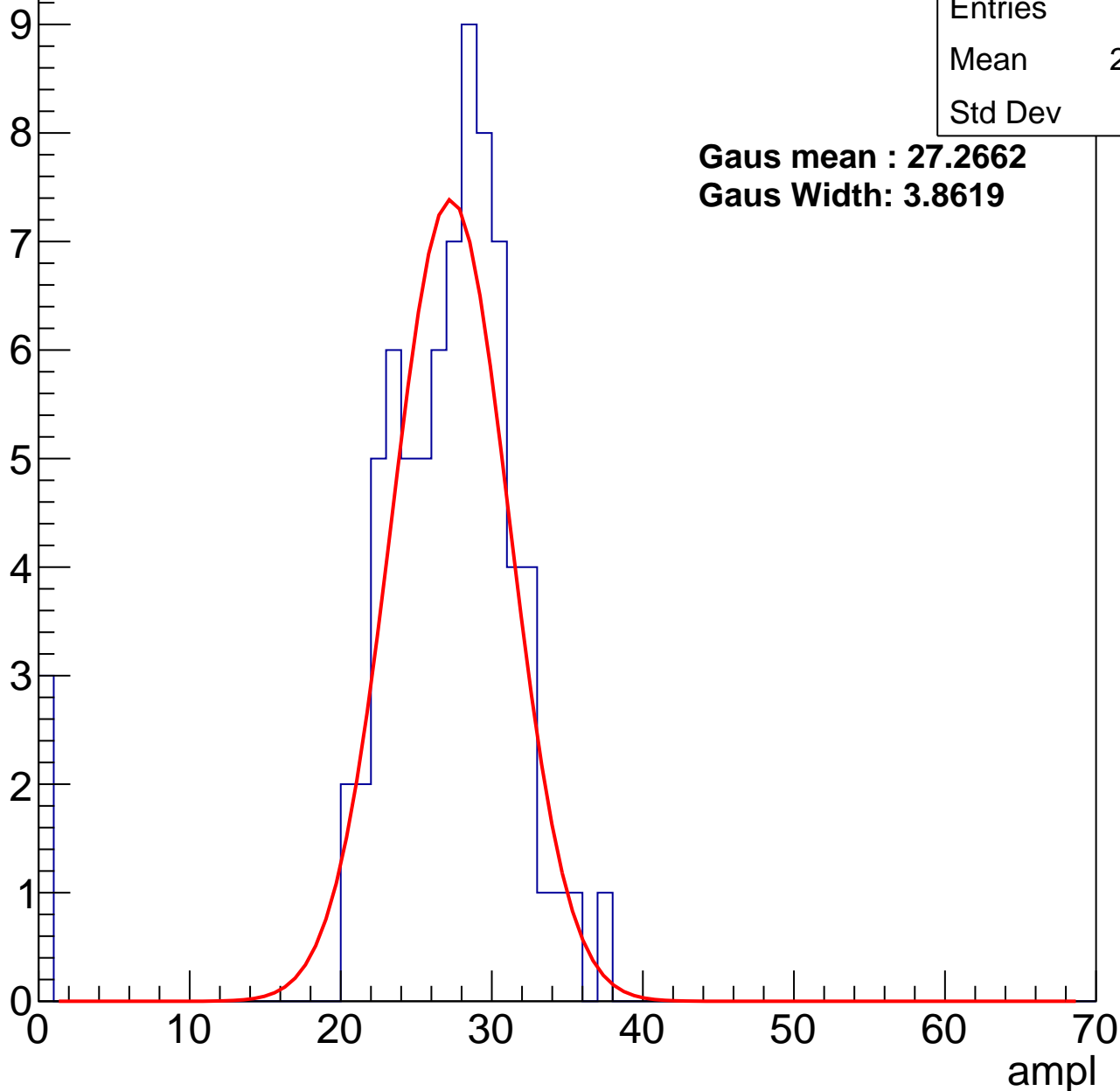
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	77
Mean	26.04
Std Dev	6.34

**Gaus mean : 27.2662**

**Gaus Width: 3.8619**



# B1L101S, U19-ch90, adc1

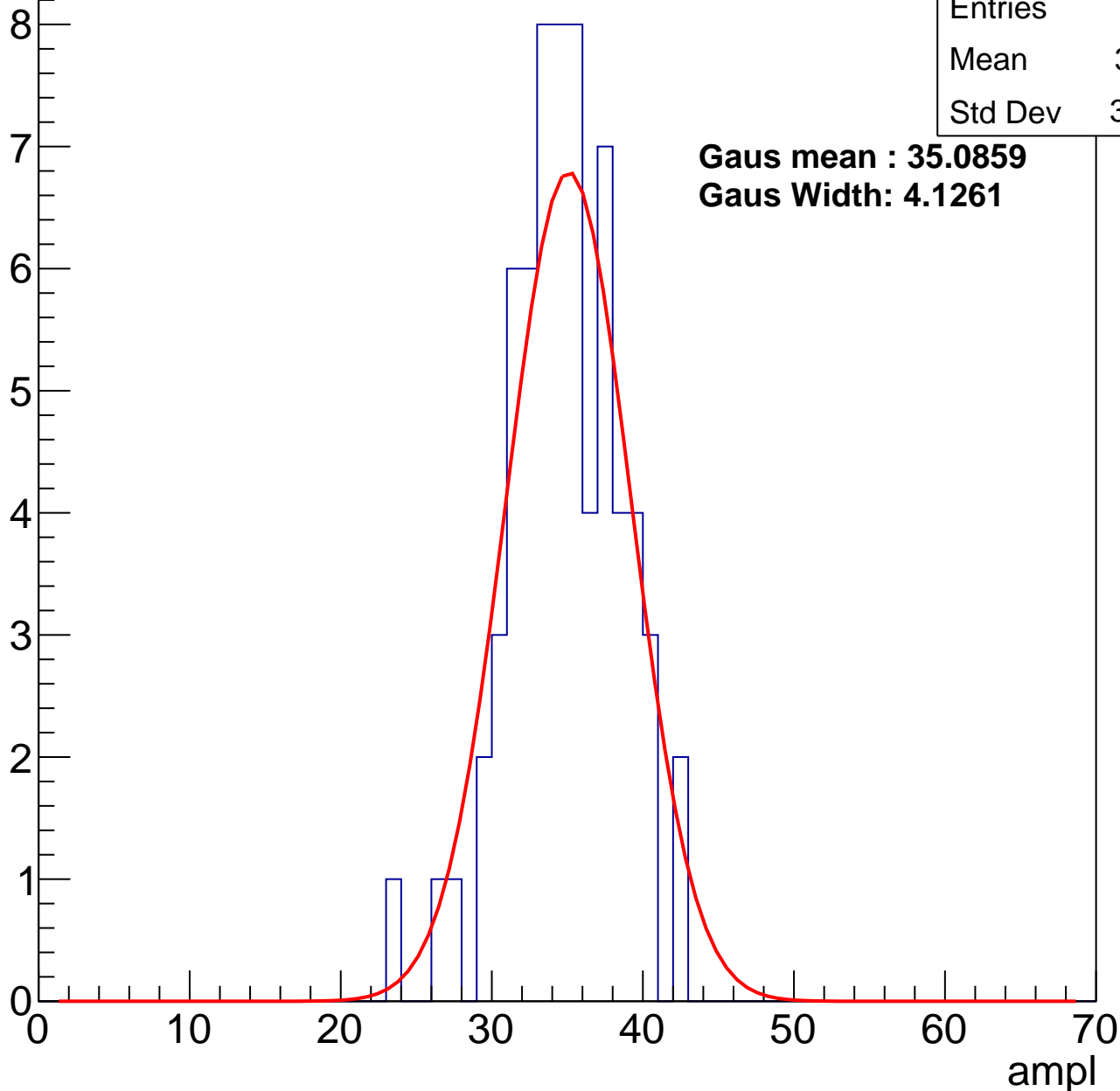
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	34.31
Std Dev	3.635

**Gaus mean : 35.0859**

**Gaus Width: 4.1261**



# B1L101S, U19-ch90, adc2

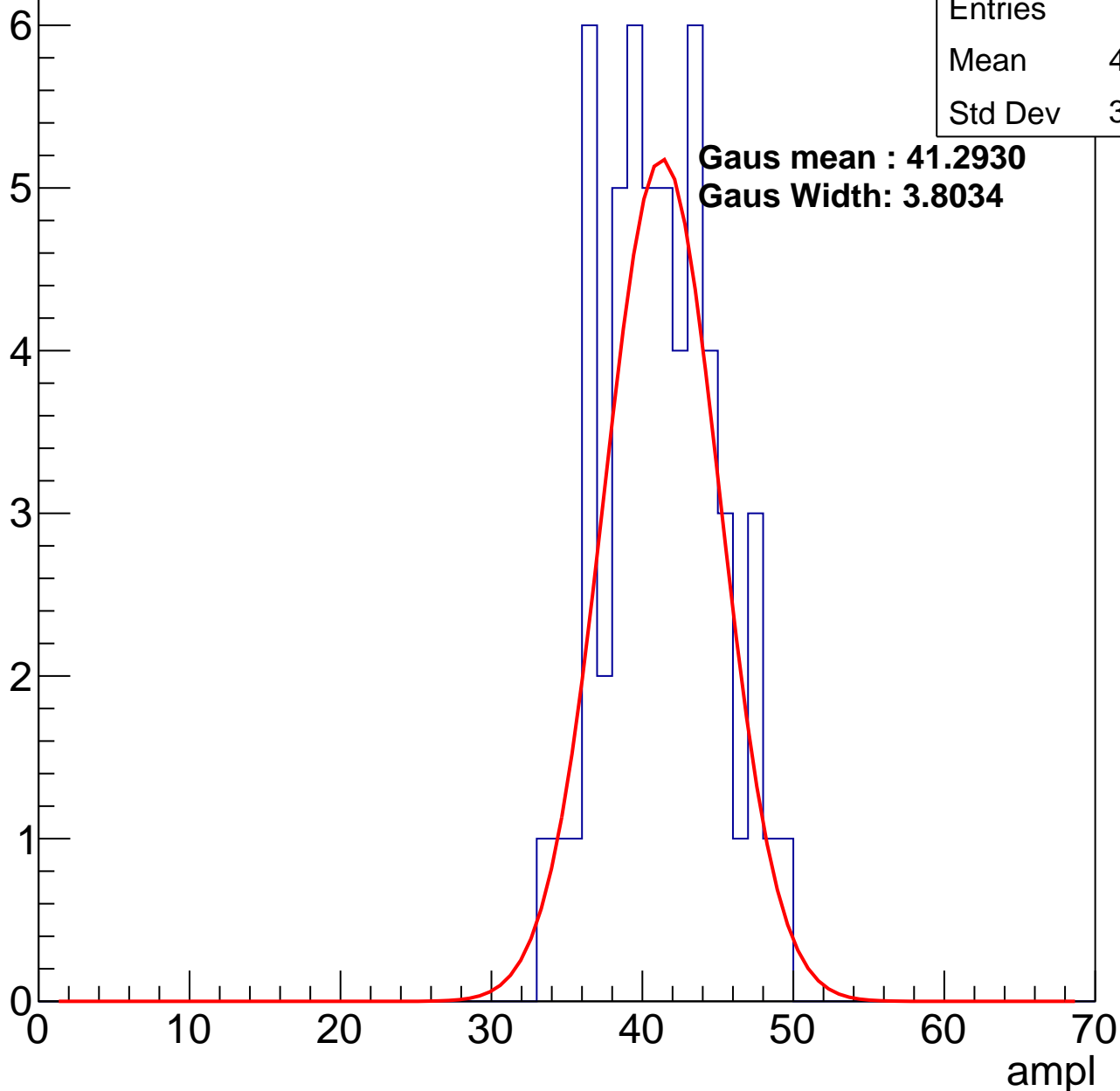
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	55
Mean	40.76
Std Dev	3.717

**Gaus mean : 41.2930**

**Gaus Width: 3.8034**

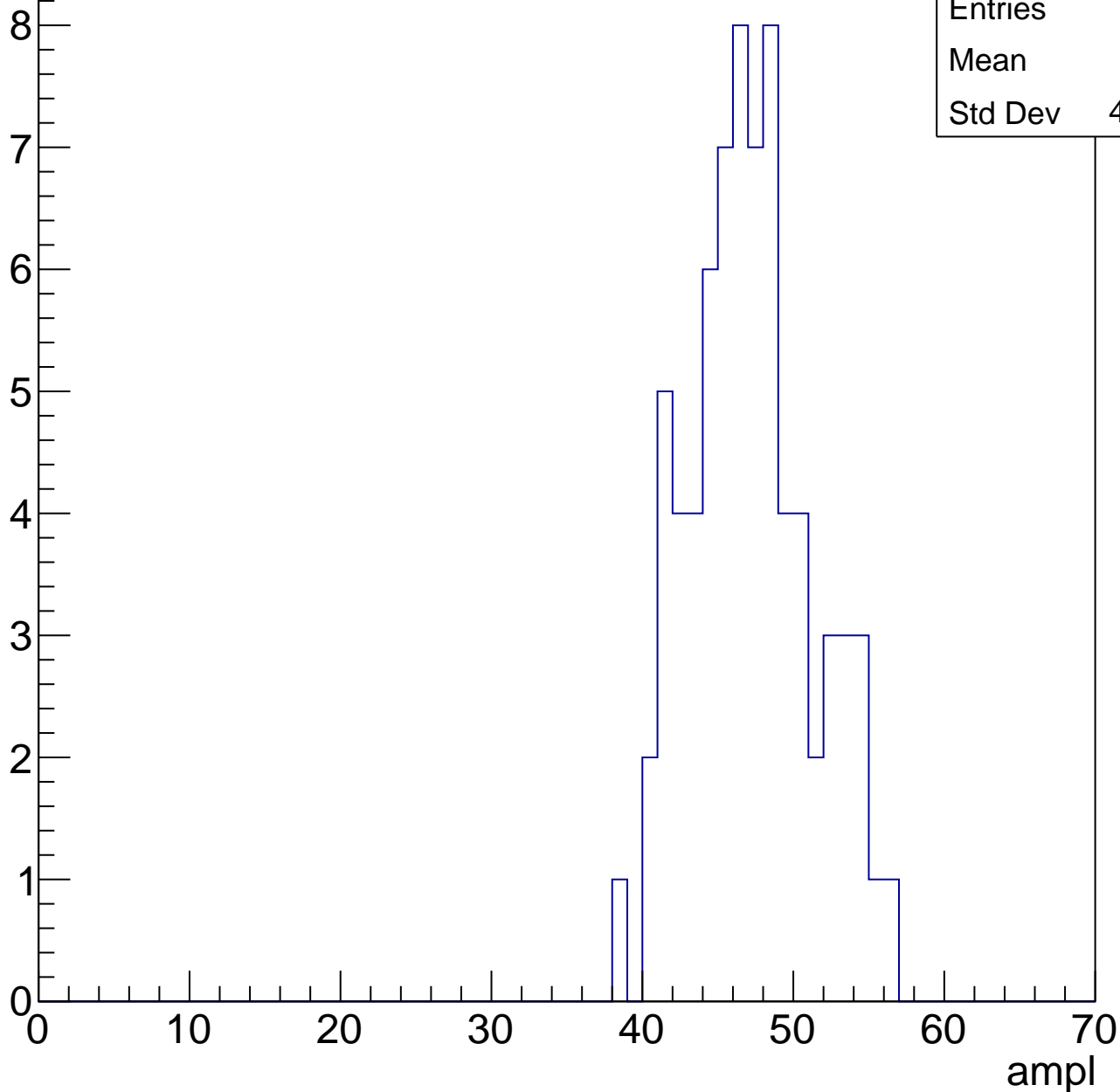


# B1L101S, U19-ch90, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	73
Mean	46.7
Std Dev	4.009

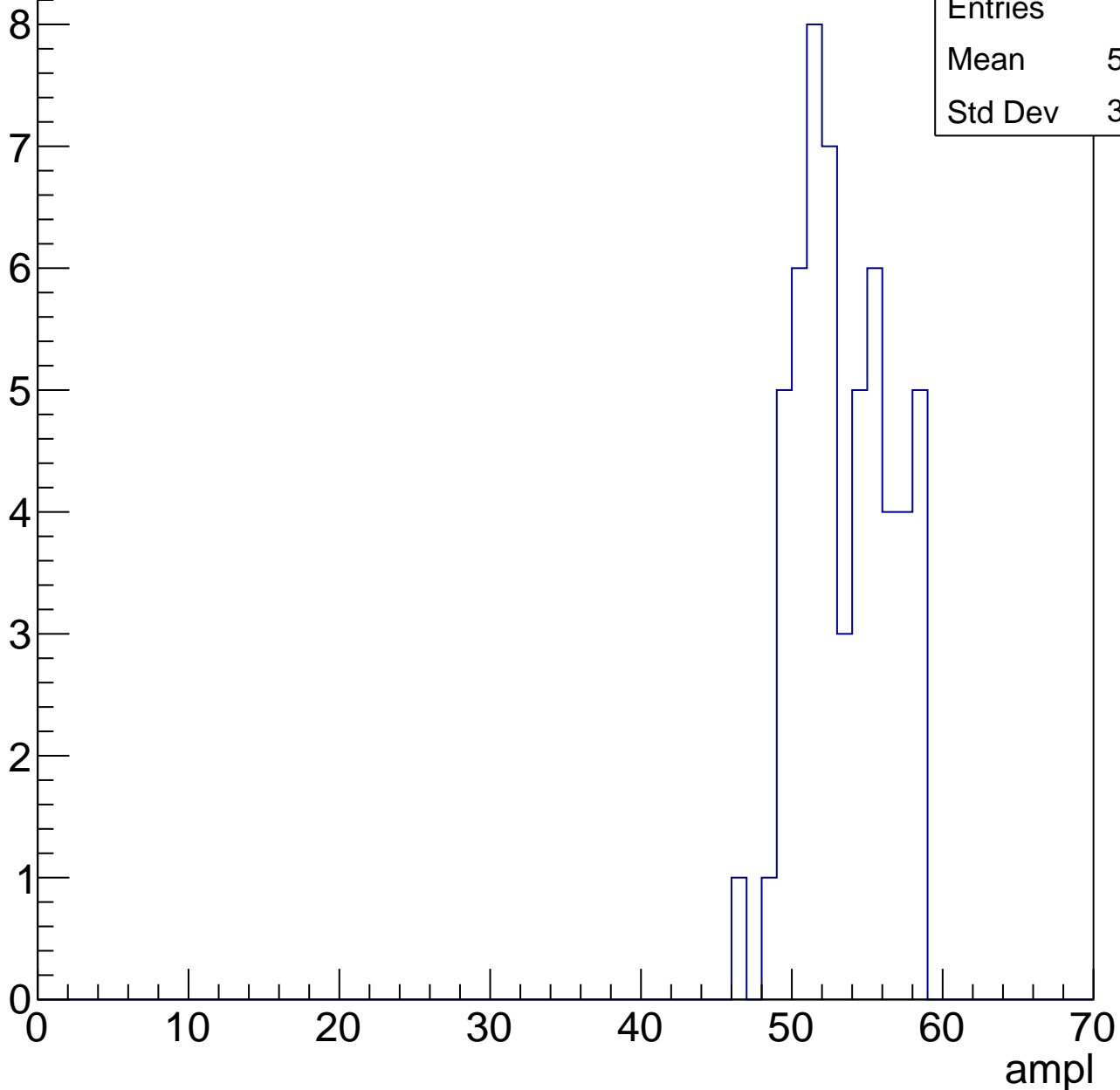


# B1L101S, U19-ch90, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	55
Mean	52.95
Std Dev	3.018



# B1L101S, U19-ch90, adc5

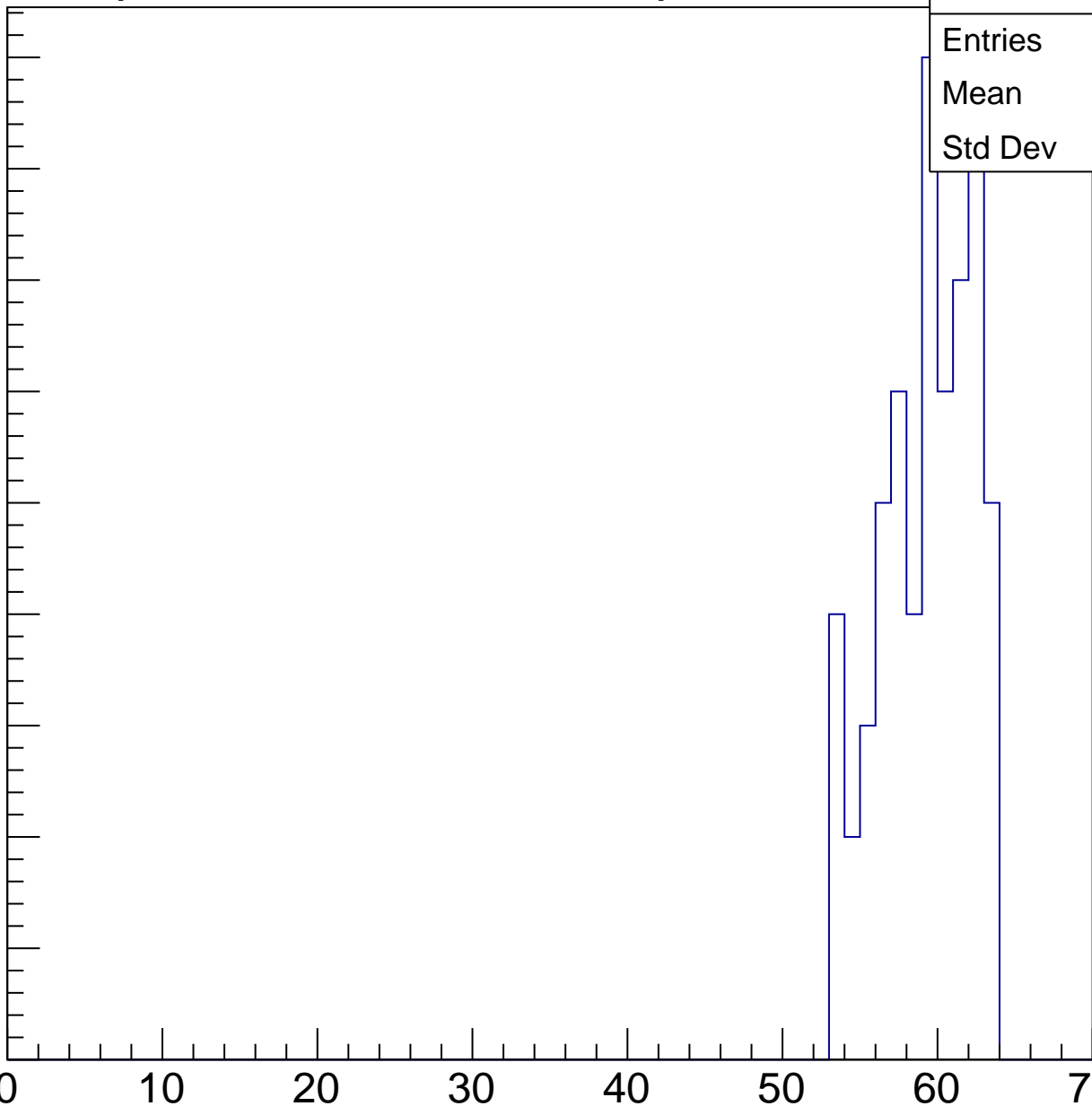
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	60
Mean	58.83
Std Dev	2.911

ampl

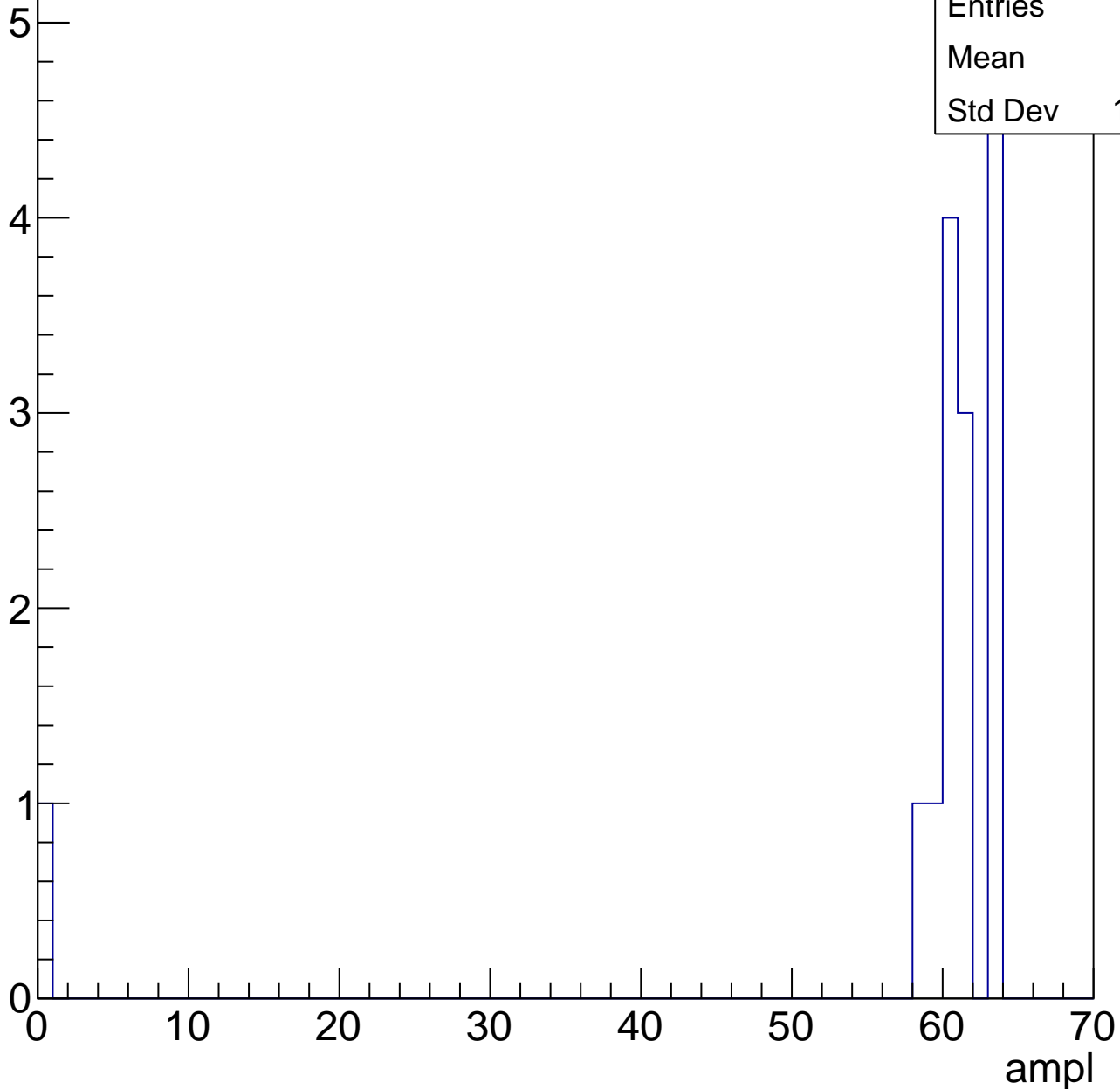


# B1L101S, U19-ch90, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	15
Mean	57
Std Dev	15.31





# B1L101S, U19-ch90, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U19-ch91, adc0

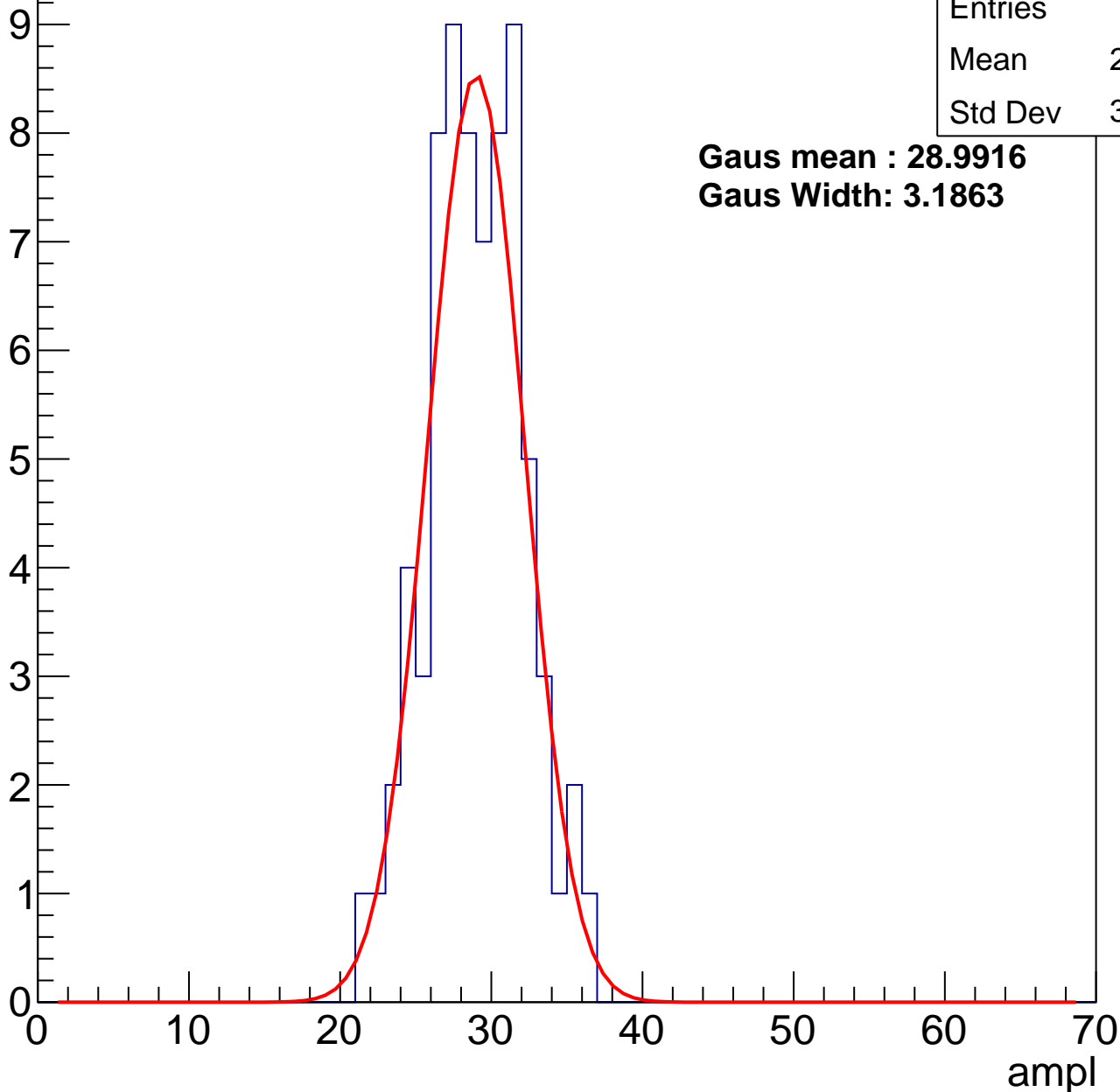
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	72
Mean	28.56
Std Dev	3.157

**Gaus mean : 28.9916**

**Gaus Width: 3.1863**



# B1L101S, U19-ch91, adc1

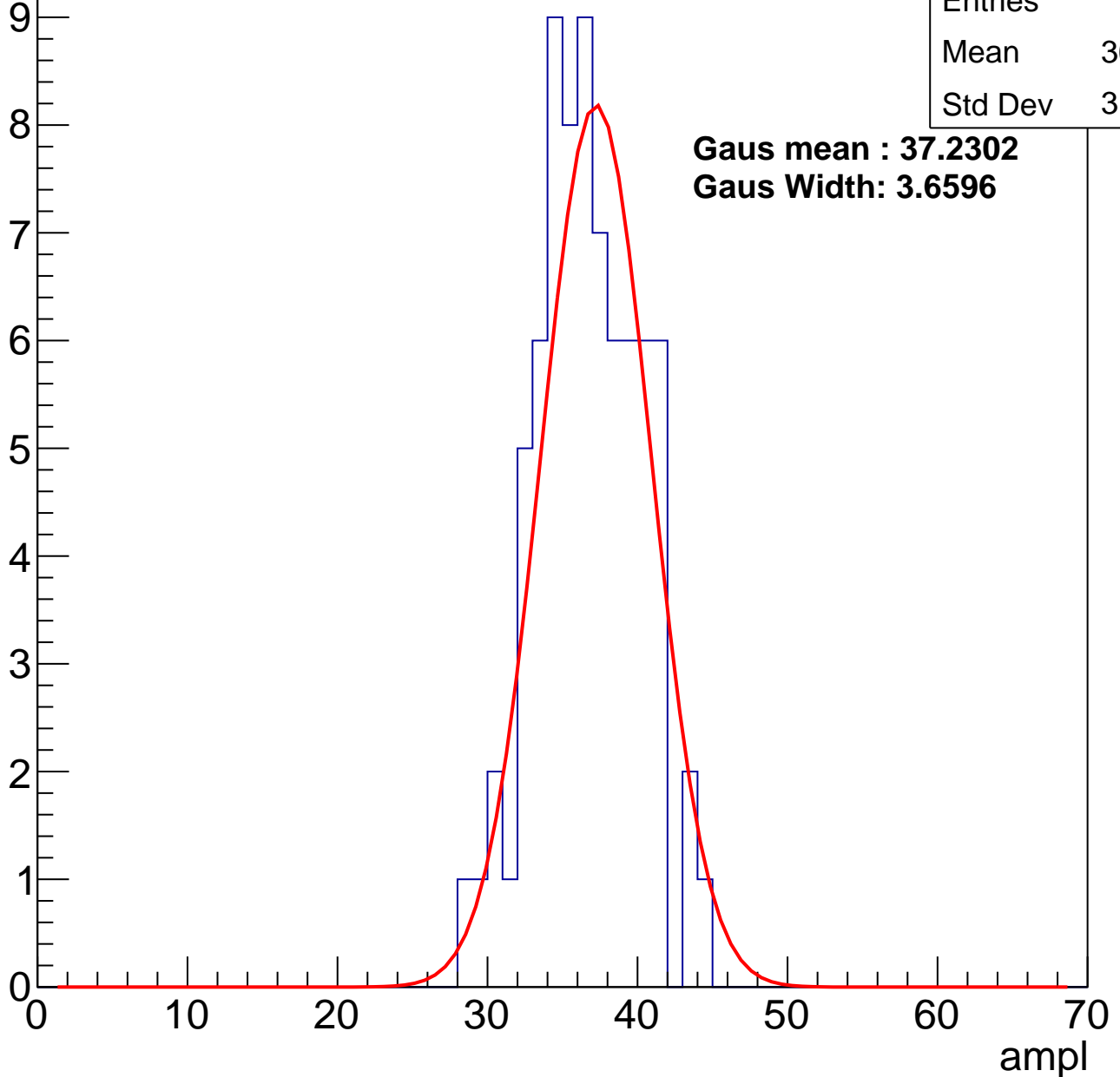
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	76
Mean	36.22
Std Dev	3.397

**Gaus mean : 37.2302**

**Gaus Width: 3.6596**



# B1L101S, U19-ch91, adc2

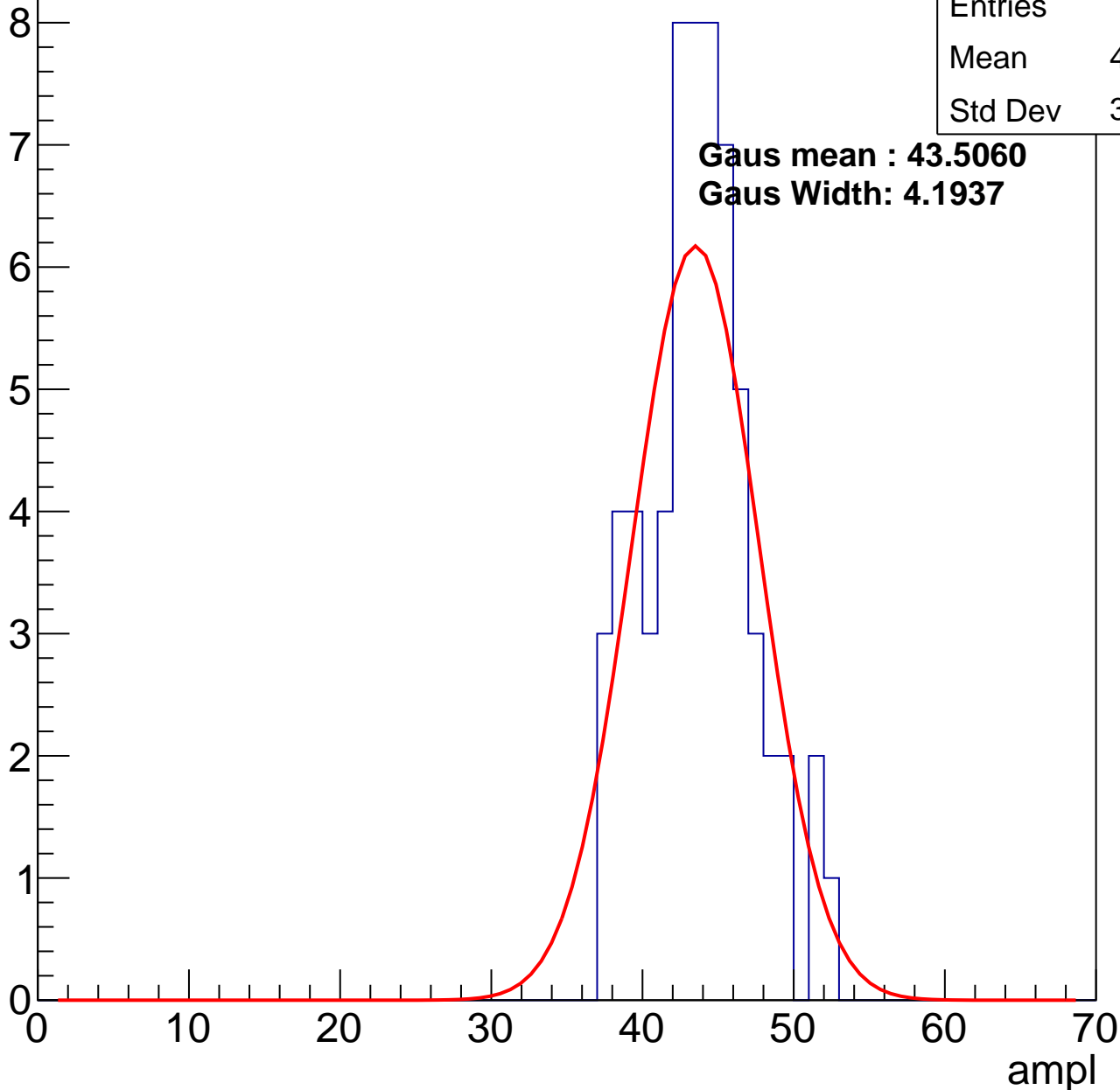
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	43.27
Std Dev	3.488

**Gaus mean : 43.5060**

**Gaus Width: 4.1937**

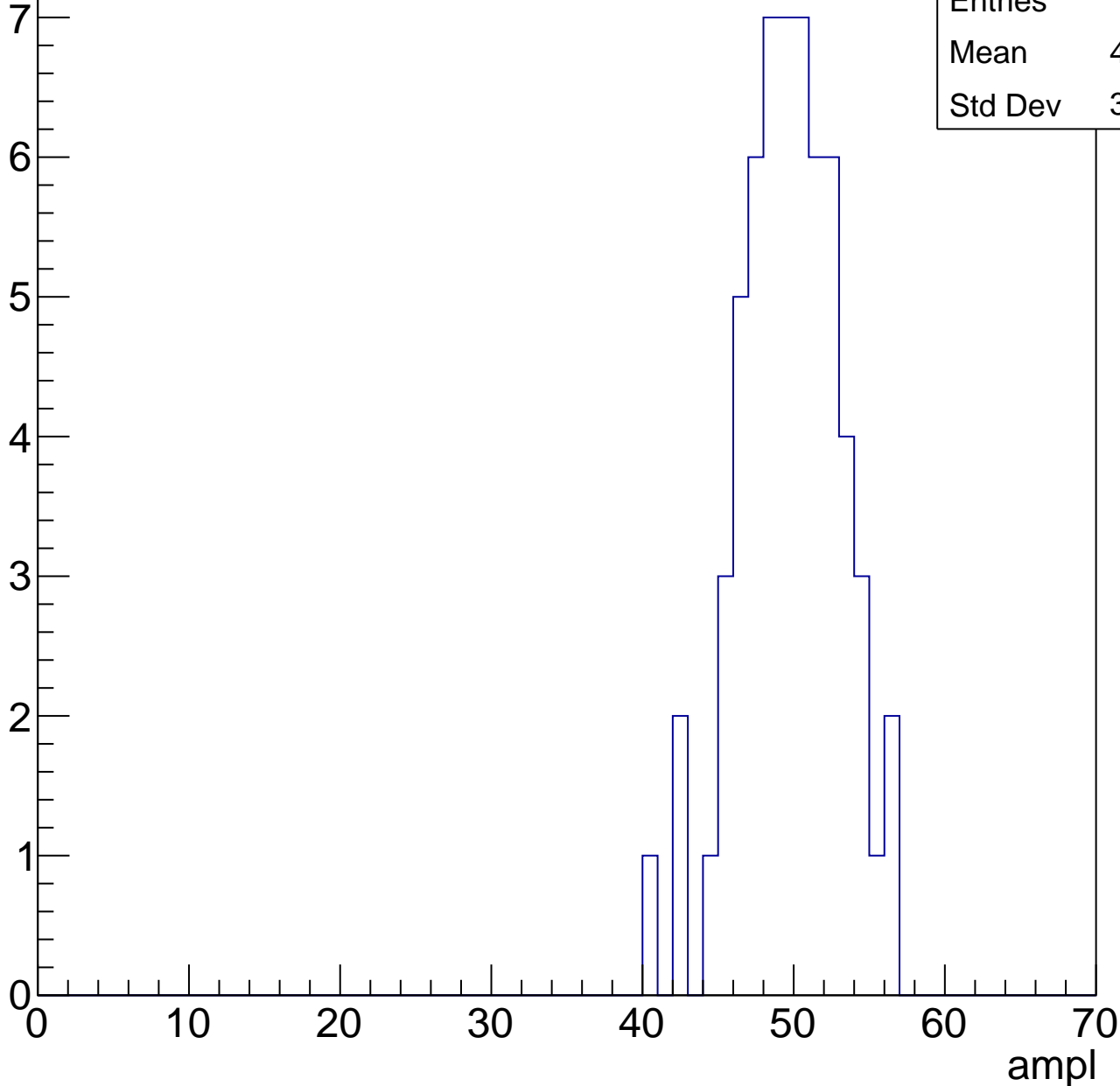


# B1L101S, U19-ch91, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	49.23
Std Dev	3.346

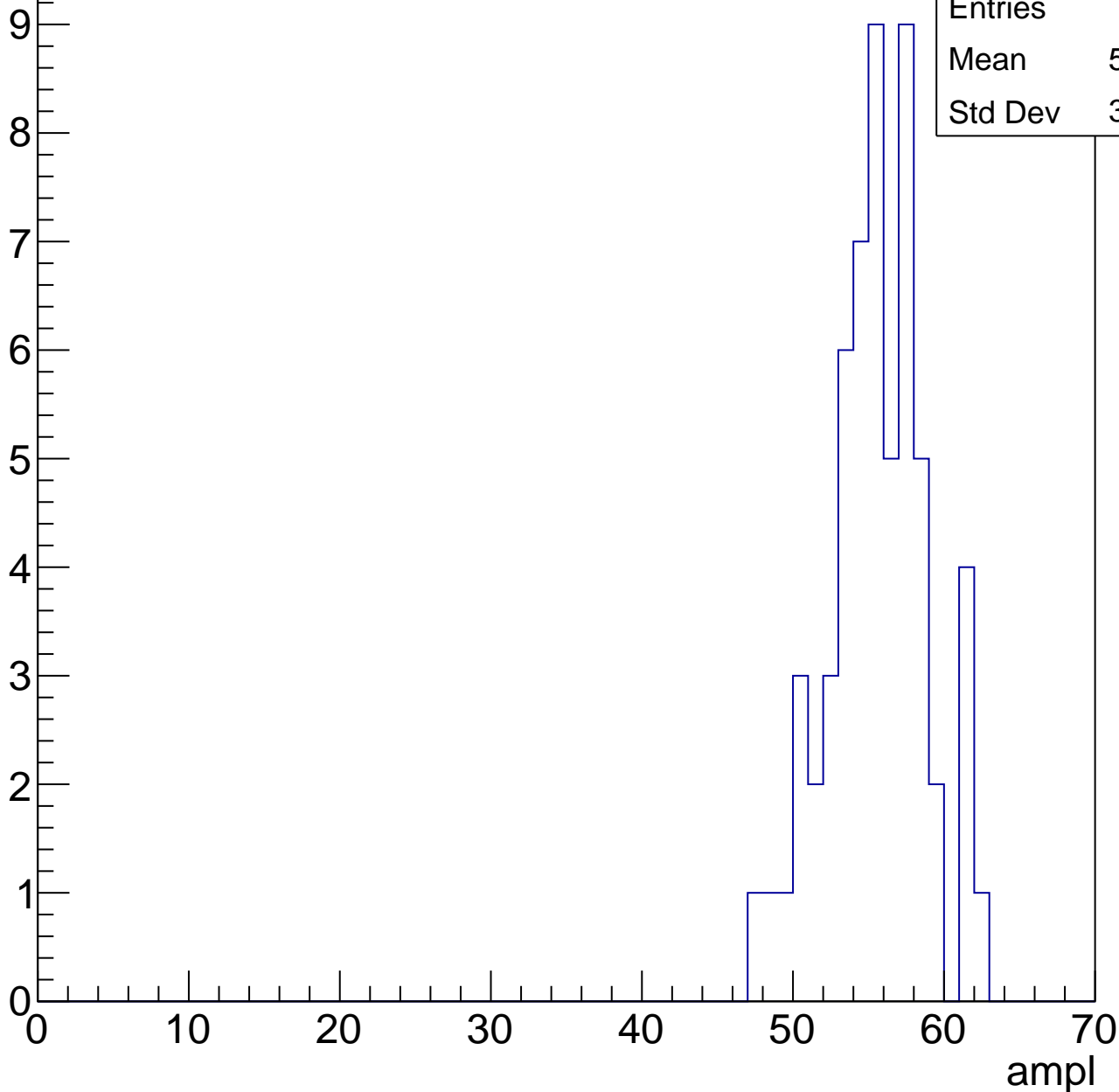


# B1L101S, U19-ch91, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	59
Mean	55.08
Std Dev	3.254



# B1L101S, U19-ch91, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

10

8

6

4

2

0

0

10

20

30

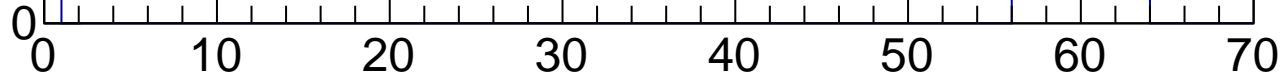
40

50

60

ampl

Entries	52
Mean	59.21
Std Dev	8.527



# B1L101S, U19-ch91, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U19-ch91, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L101S, U19-ch92, adc0

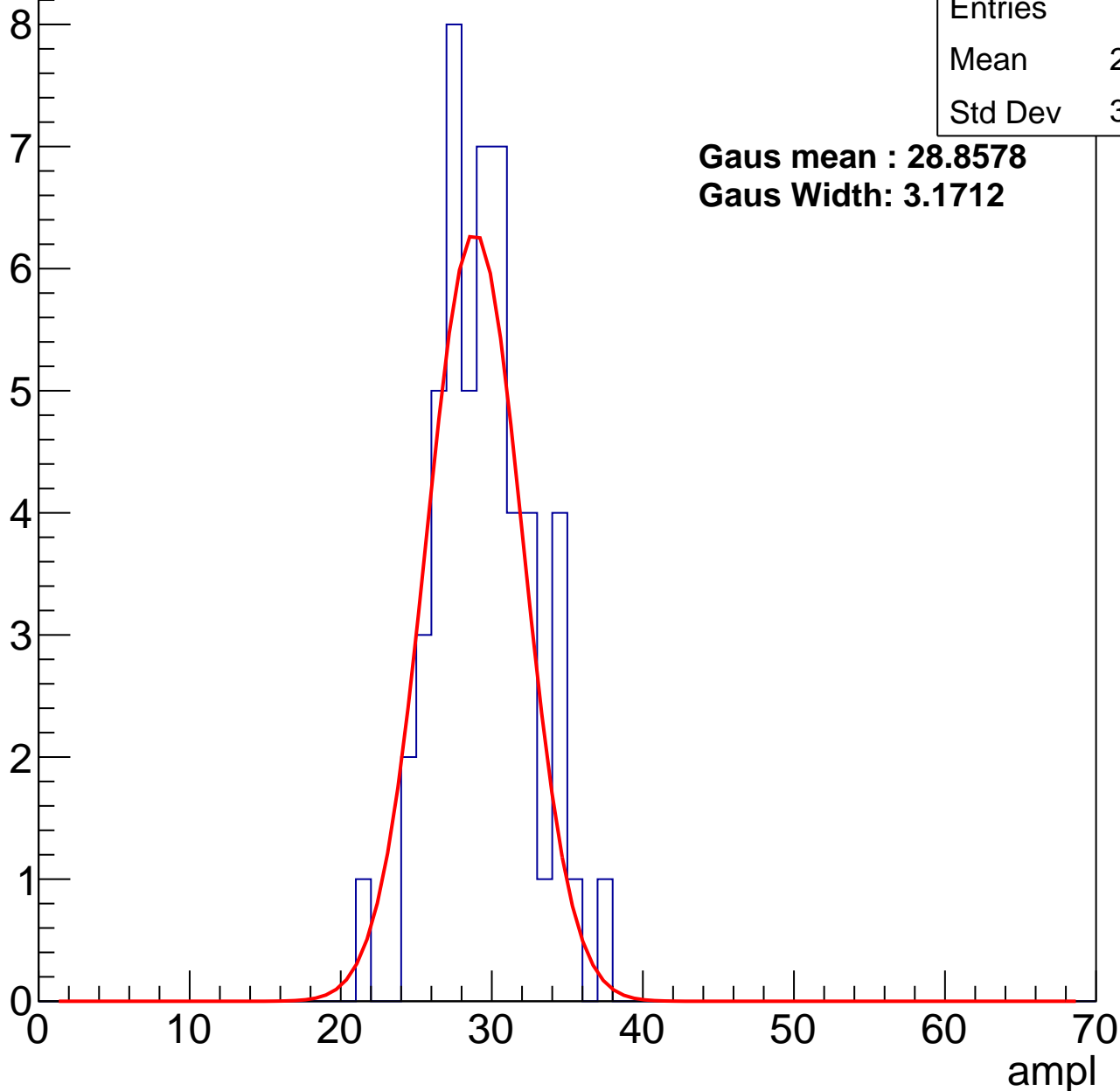
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	53
Mean	28.98
Std Dev	3.129

**Gaus mean : 28.8578**

**Gaus Width: 3.1712**



# B1L101S, U19-ch92, adc1

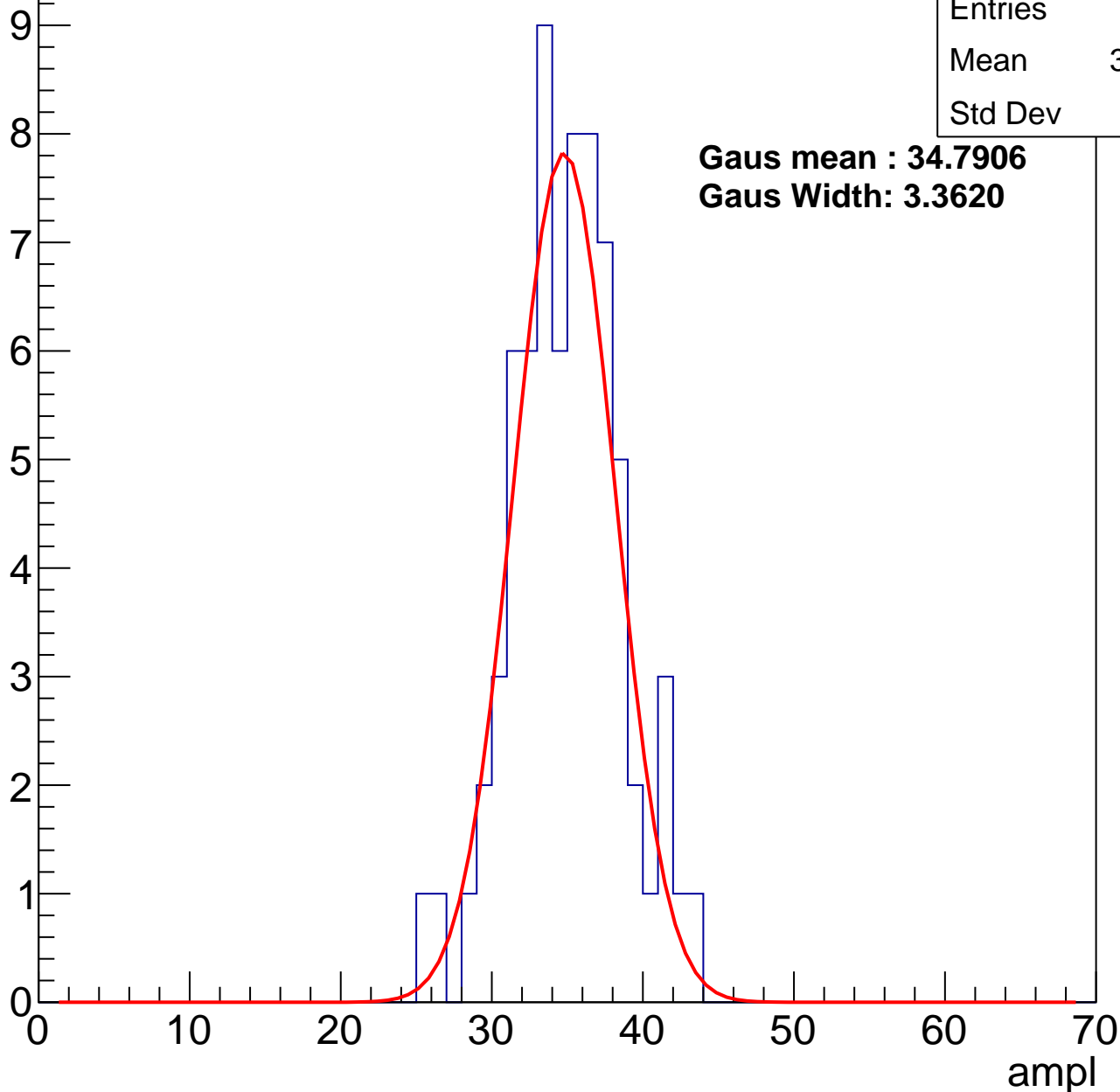
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	71
Mean	34.49
Std Dev	3.58

**Gaus mean : 34.7906**

**Gaus Width: 3.3620**



# B1L101S, U19-ch92, adc2

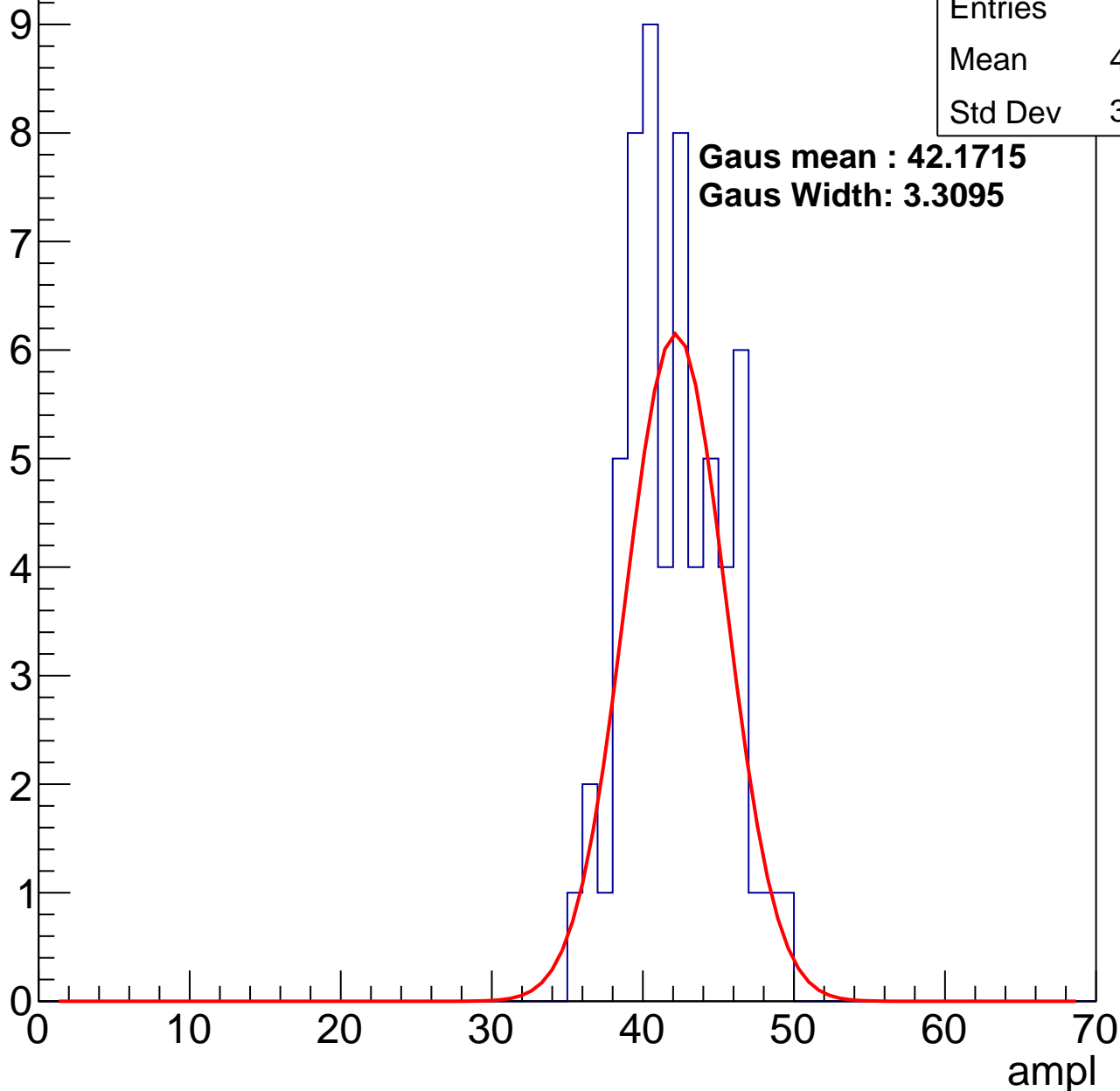
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	60
Mean	41.63
Std Dev	3.152

**Gaus mean : 42.1715**

**Gaus Width: 3.3095**

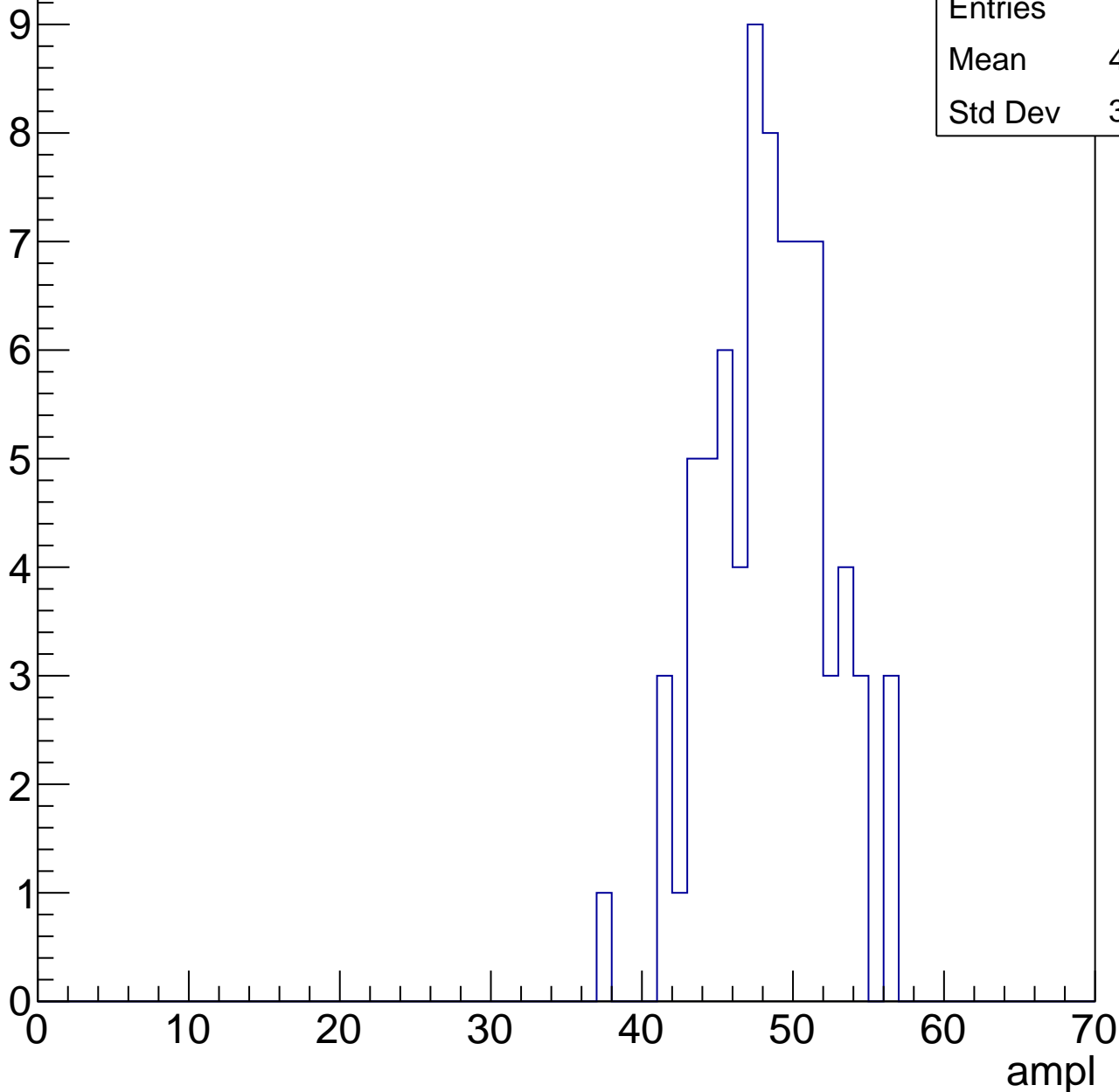


# B1L101S, U19-ch92, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

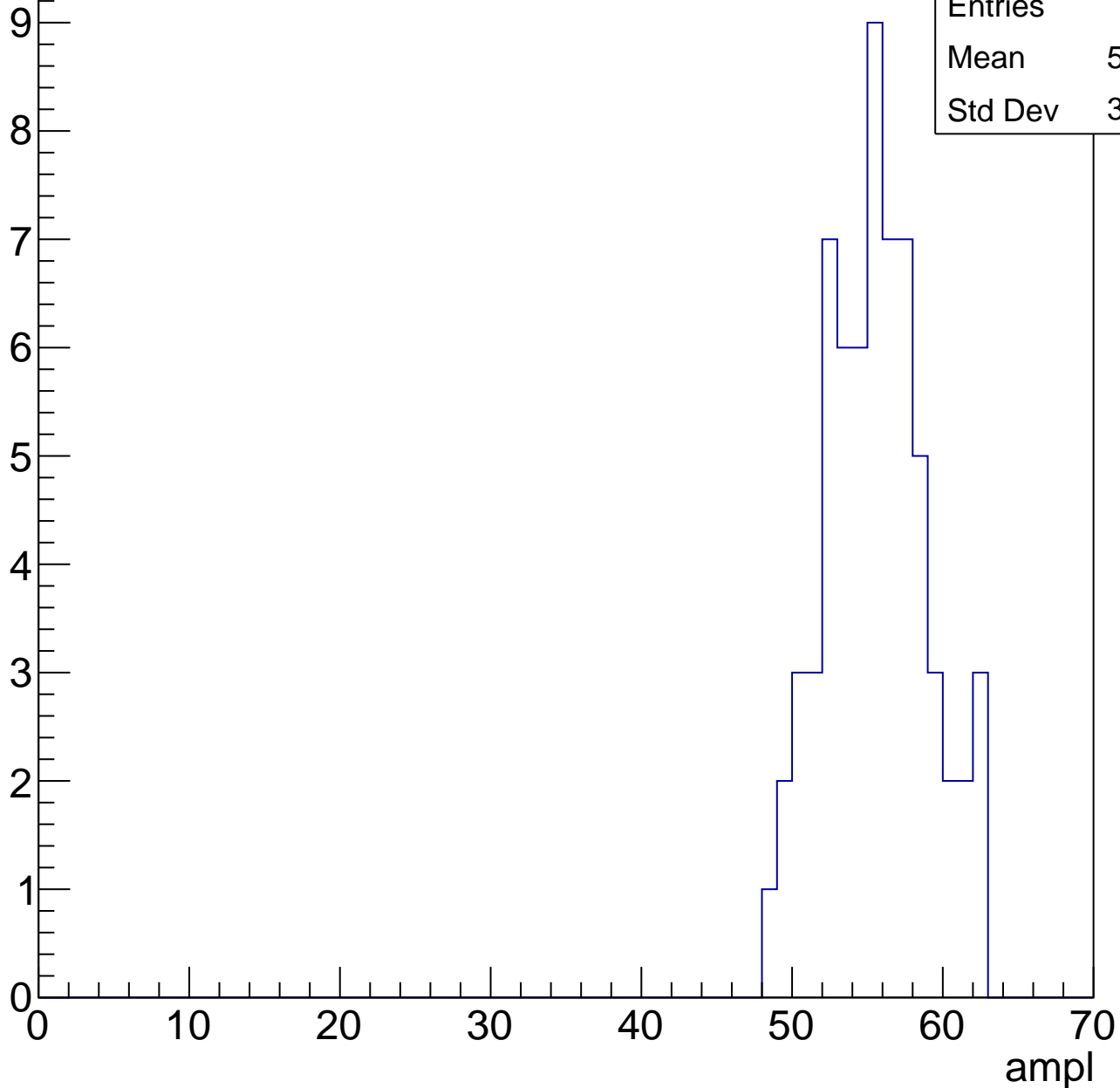
Entries	76
Mean	47.97
Std Dev	3.863



# B1L101S, U19-ch92, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



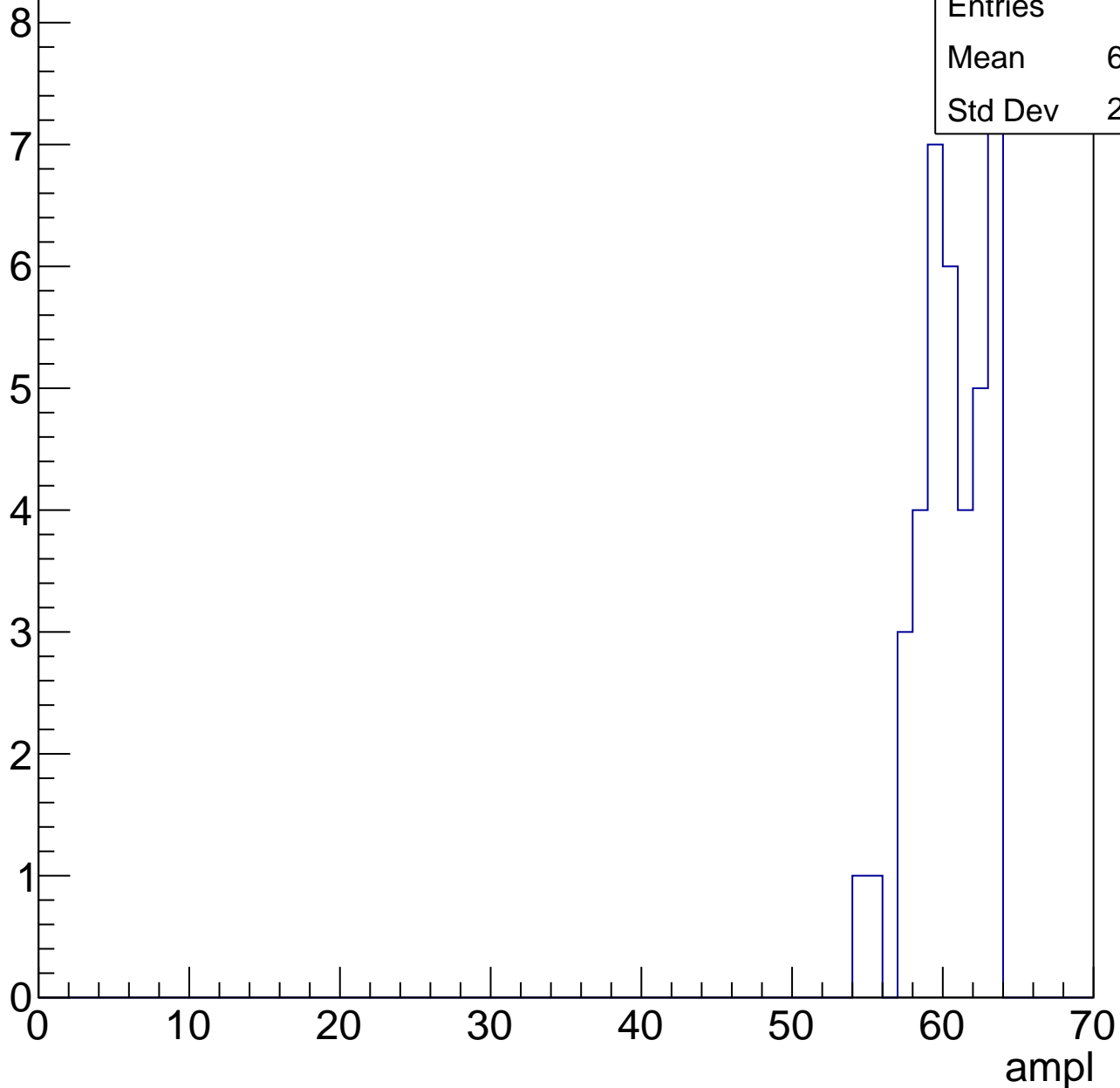
Entries	66
Mean	55.09
Std Dev	3.334

# B1L101S, U19-ch92, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

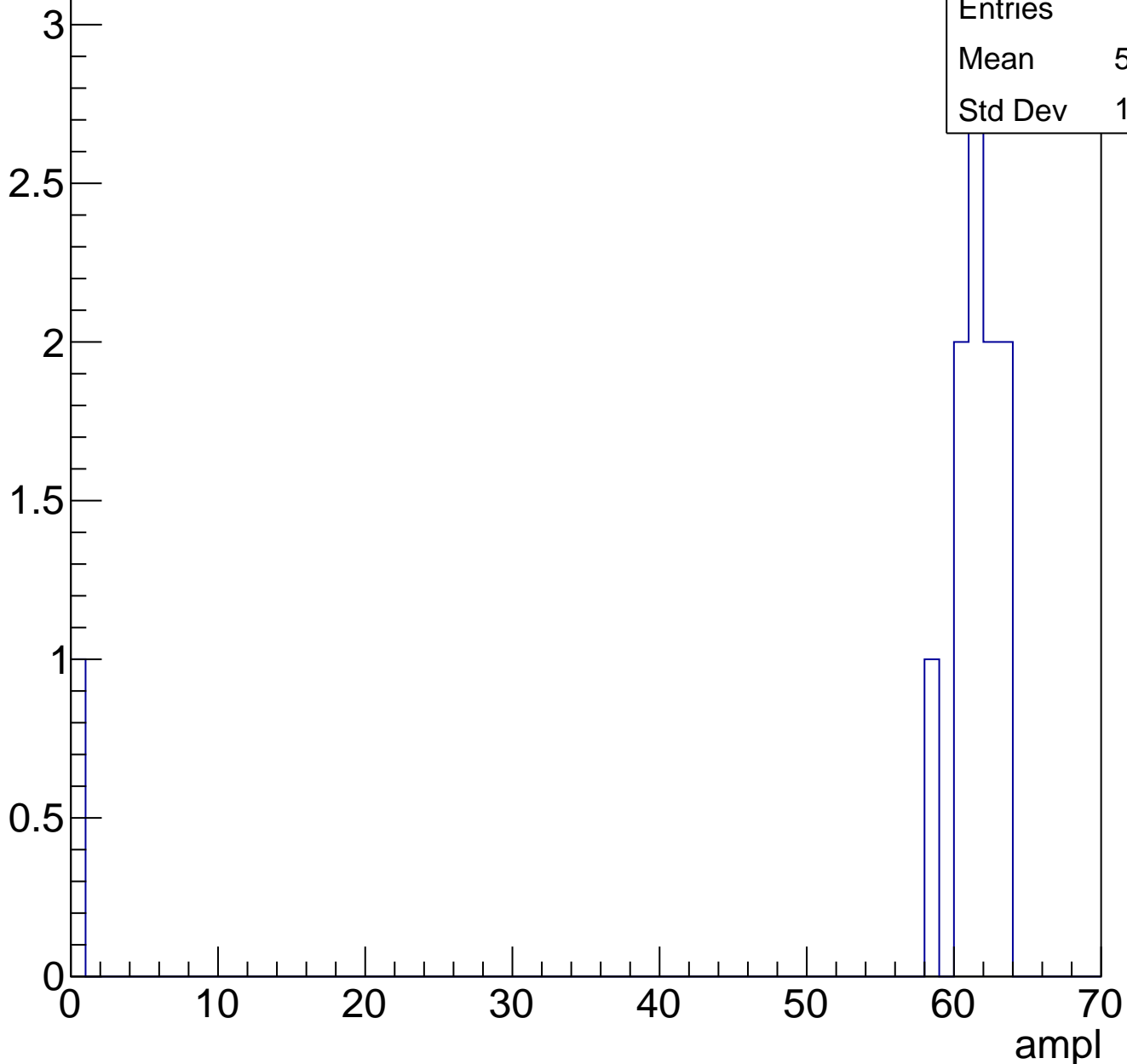
Entries	39
Mean	60.08
Std Dev	2.303



# B1L101S, U19-ch92, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

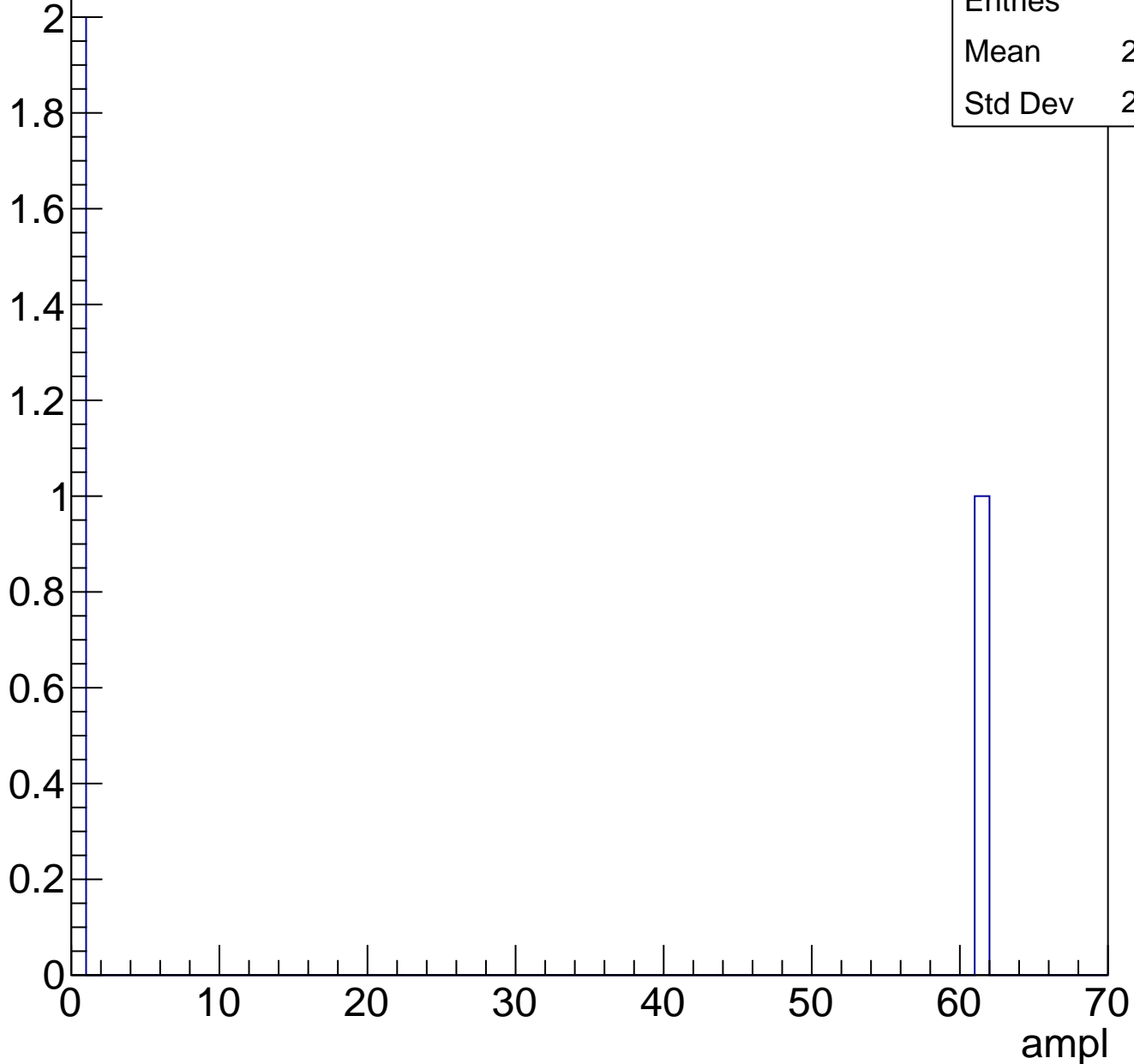




# B1L101S, U19-ch92, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U19-ch93, adc0

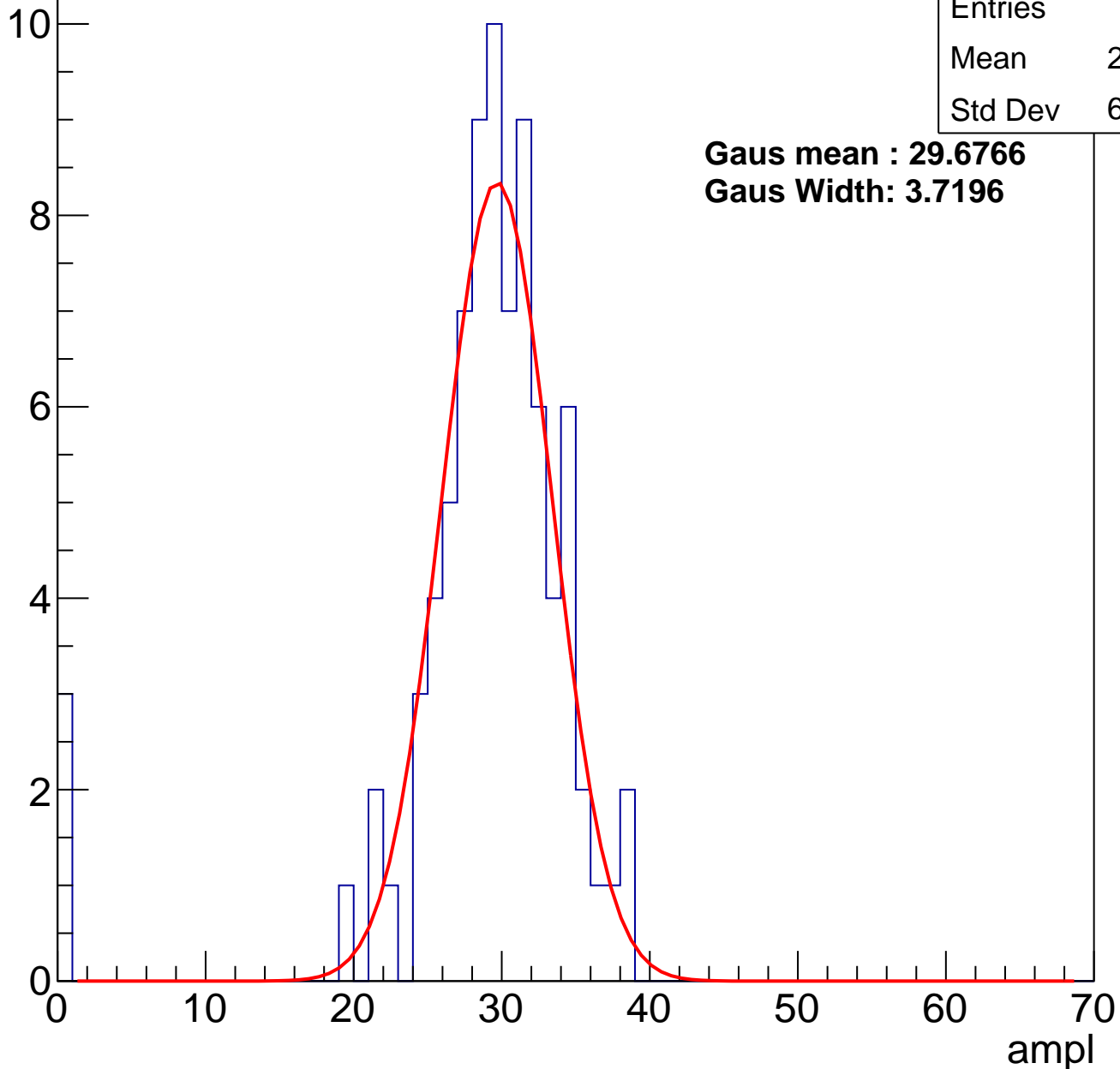
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	83
Mean	28.34
Std Dev	6.625

**Gaus mean : 29.6766**

**Gaus Width: 3.7196**

Entry



# B1L101S, U19-ch93, adc1

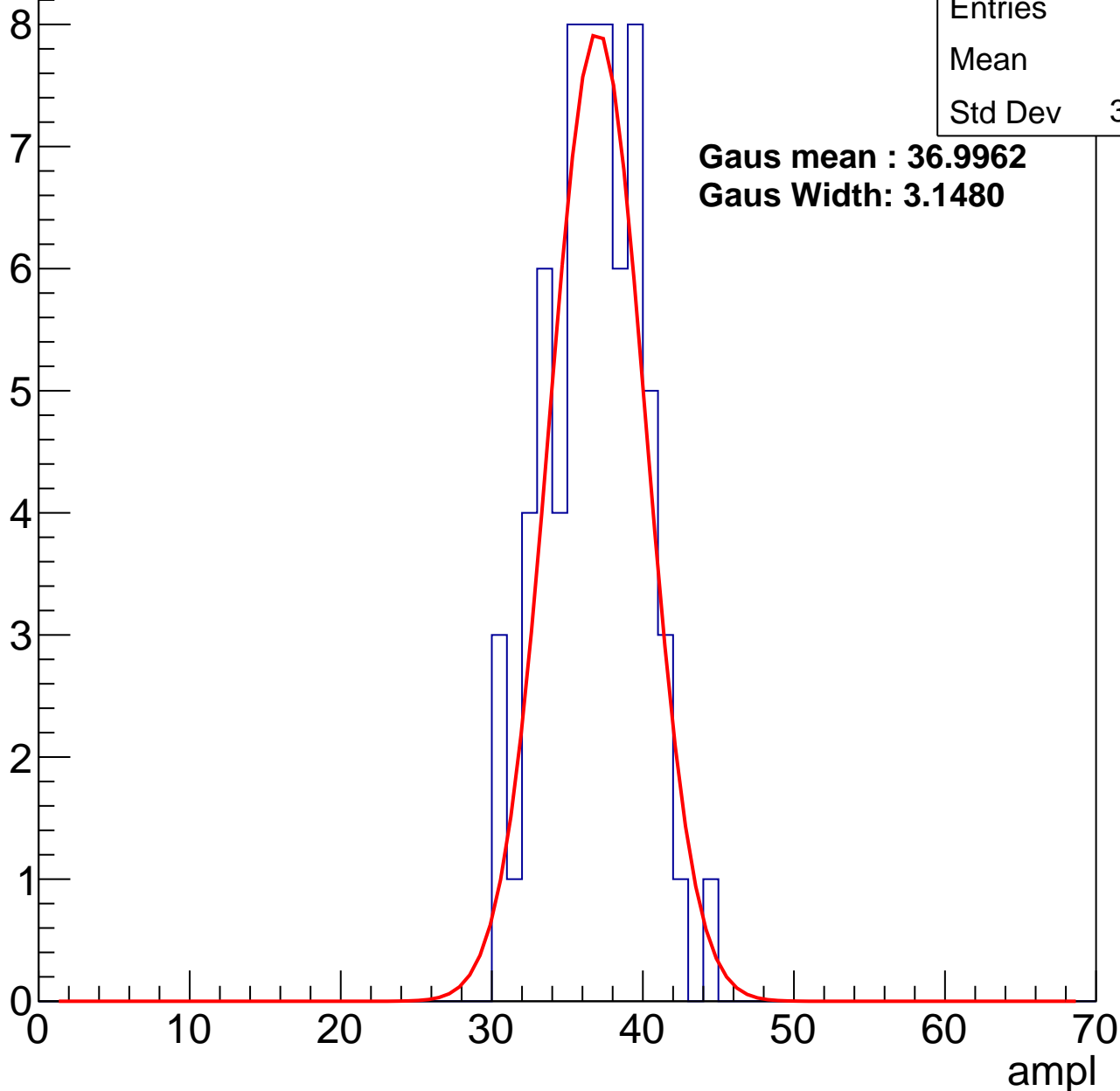
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	66
Mean	36.3
Std Dev	3.085

**Gaus mean : 36.9962**

**Gaus Width: 3.1480**



# B1L101S, U19-ch93, adc2

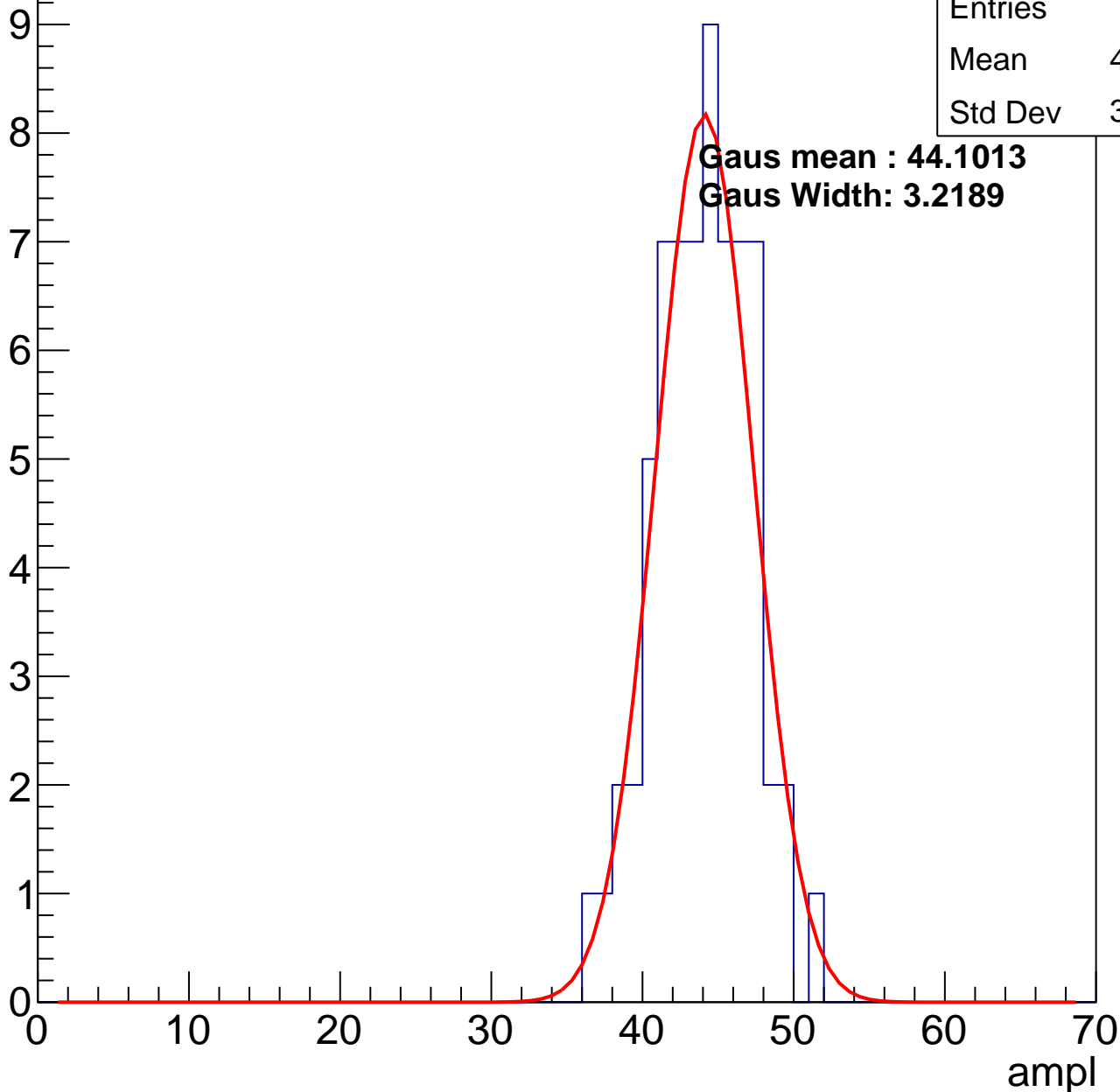
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	67
Mean	43.52
Std Dev	3.058

**Gaus mean : 44.1013**

**Gaus Width: 3.2189**

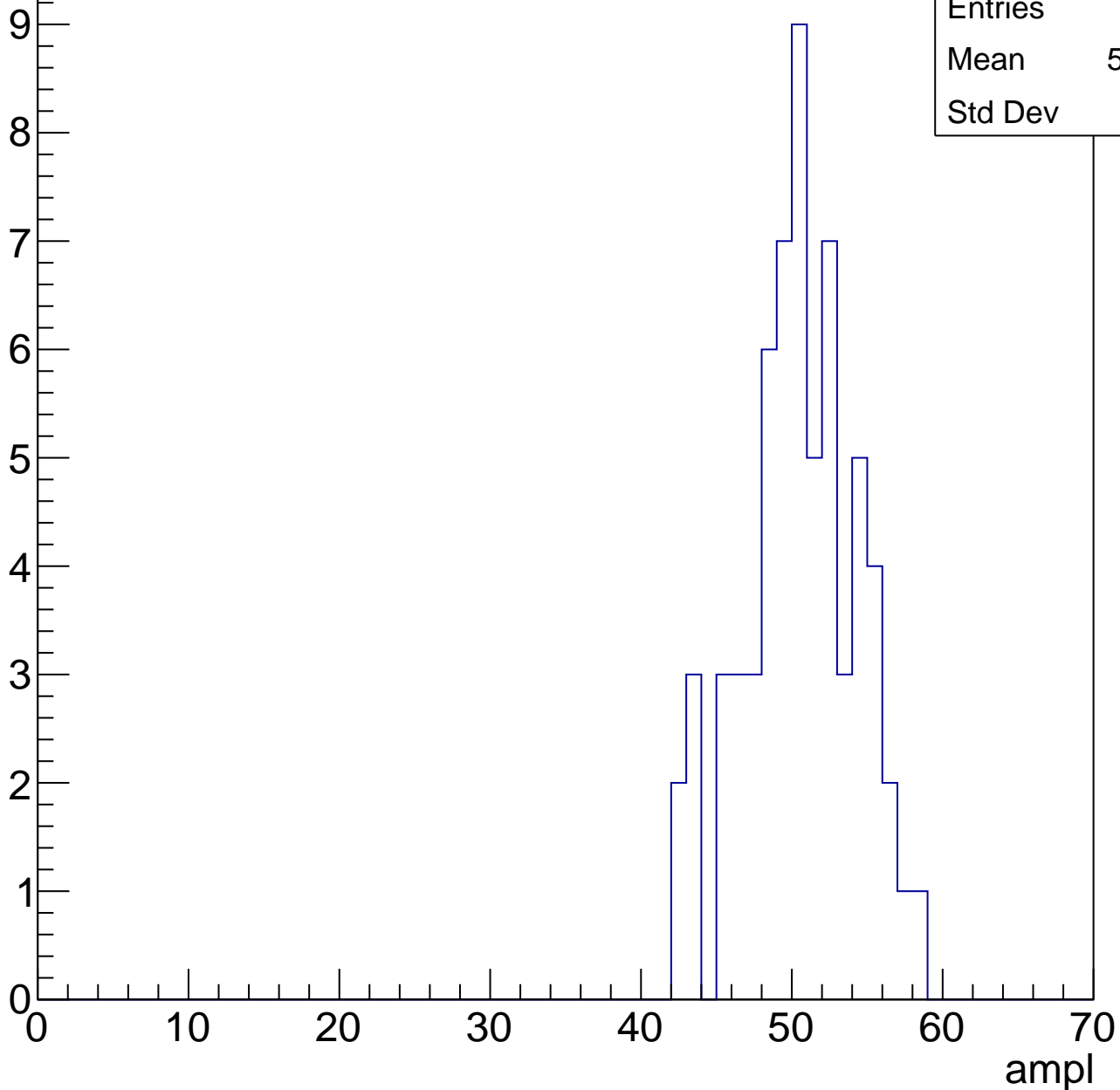


# B1L101S, U19-ch93, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

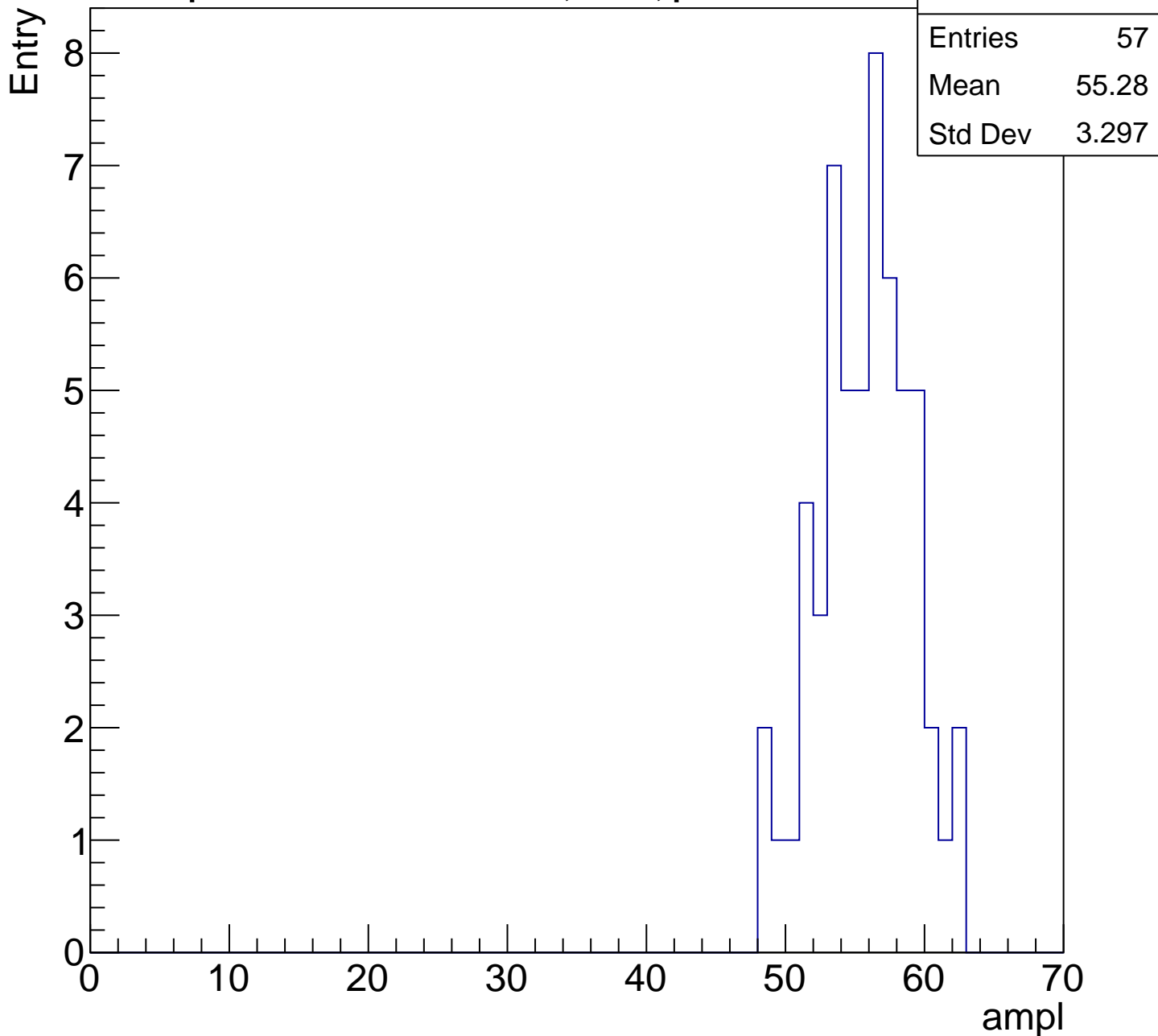
Entry

Entries	64
Mean	50.05
Std Dev	3.71



# B1L101S, U19-ch93, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

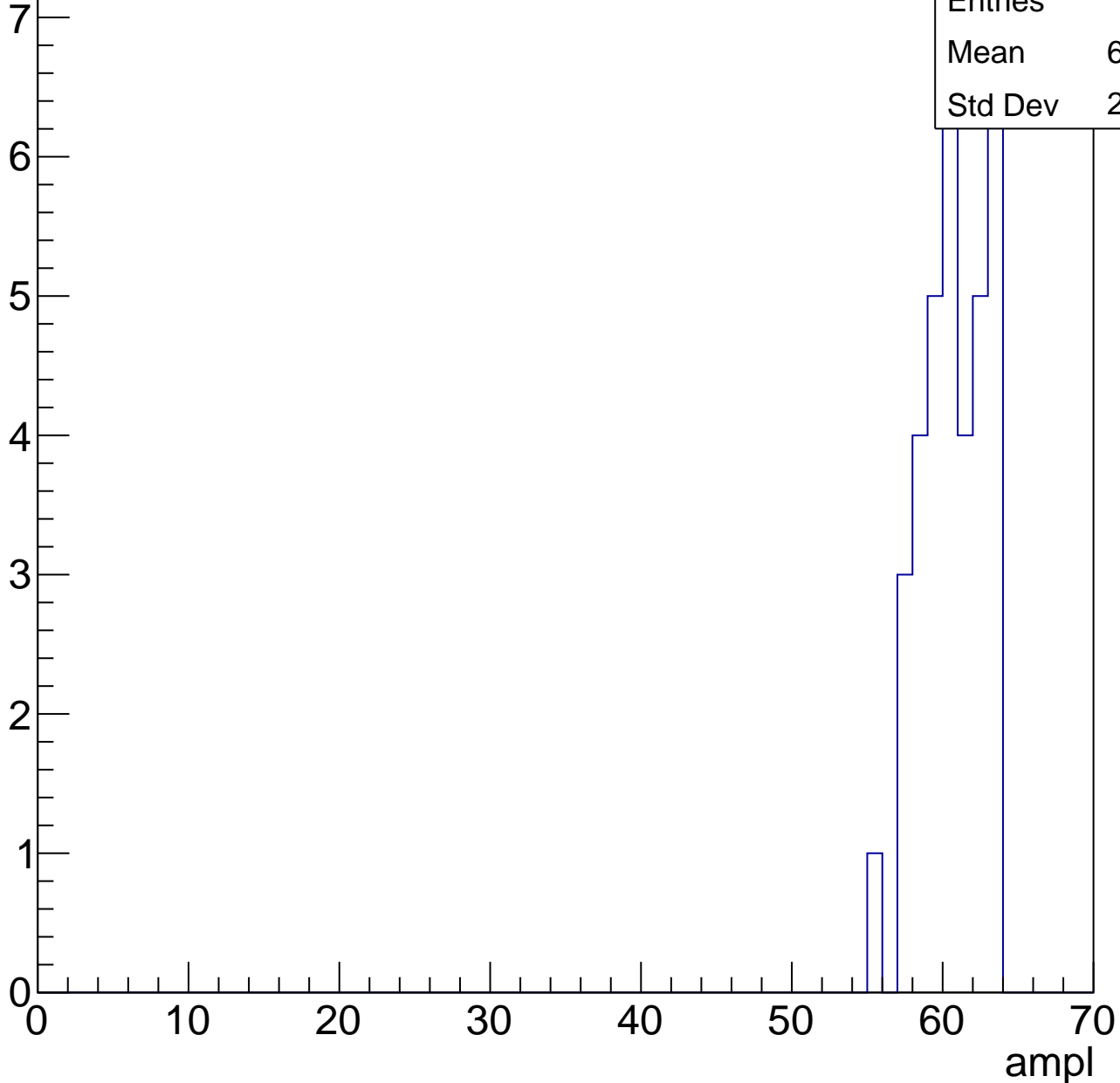


# B1L101S, U19-ch93, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	36
Mean	60.22
Std Dev	2.096

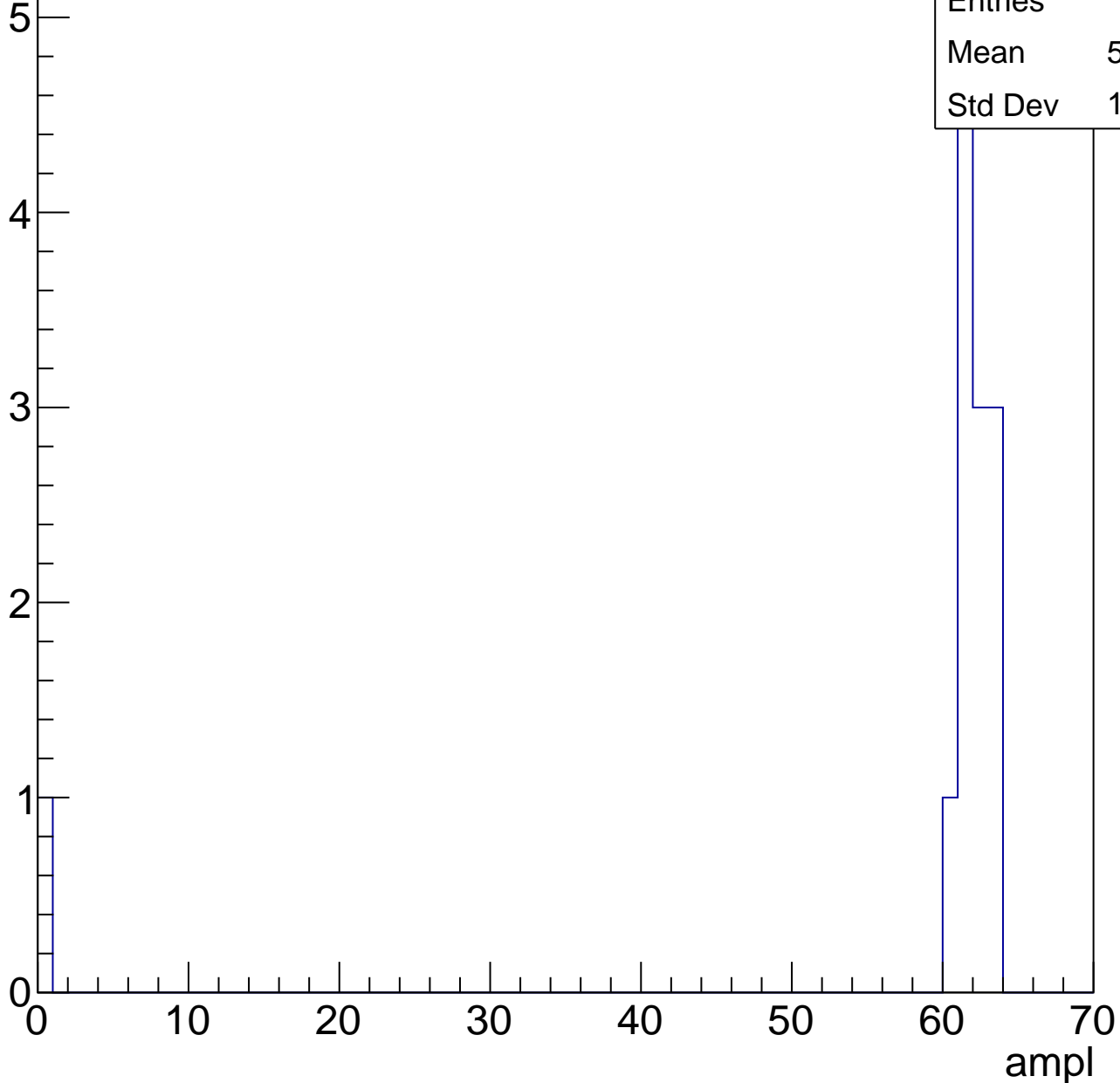


# B1L101S, U19-ch93, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	13
Mean	56.92
Std Dev	16.46





# B1L101S, U19-ch93, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U19-ch94, adc0

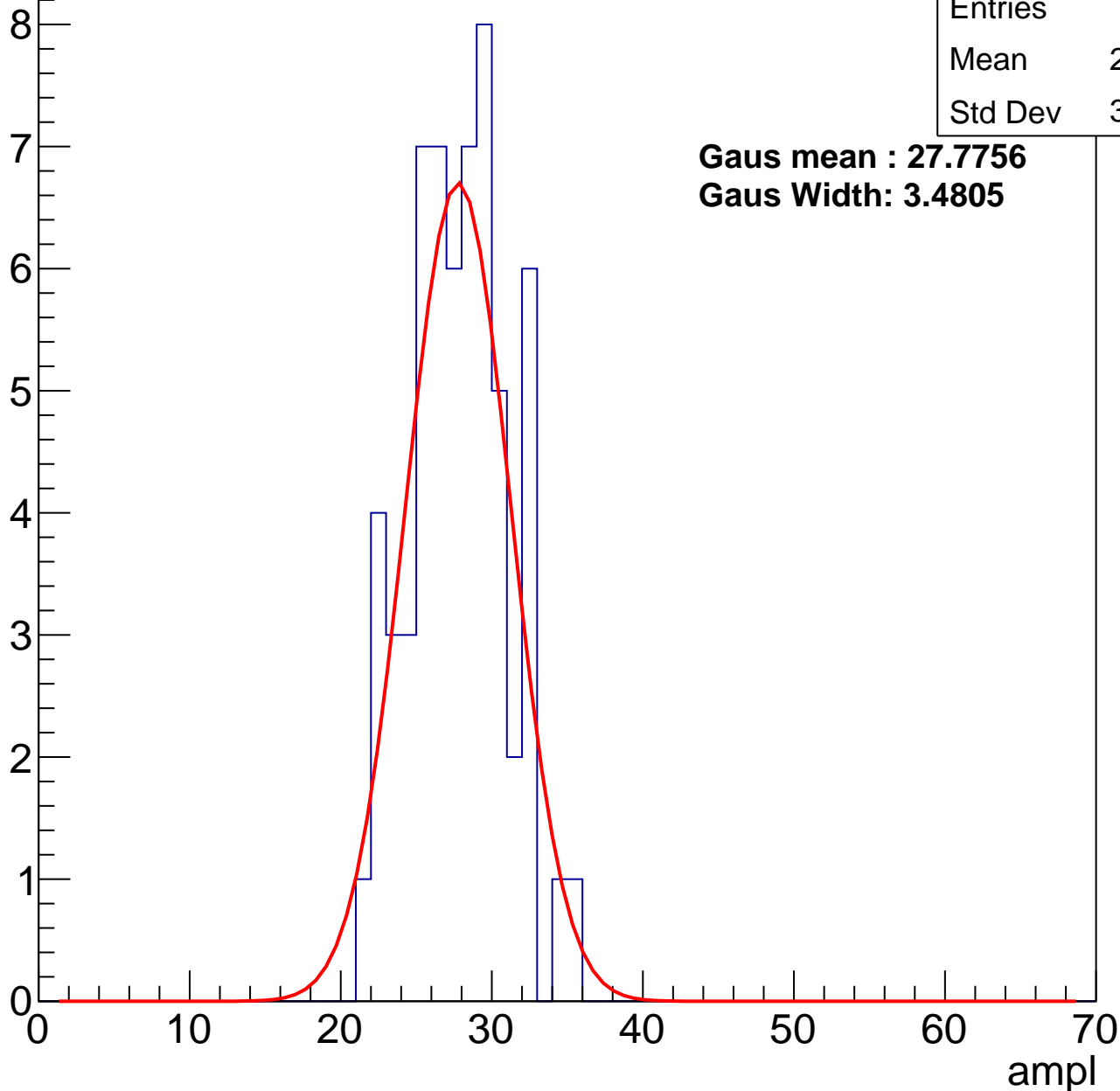
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	27.38
Std Dev	3.179

**Gaus mean : 27.7756**

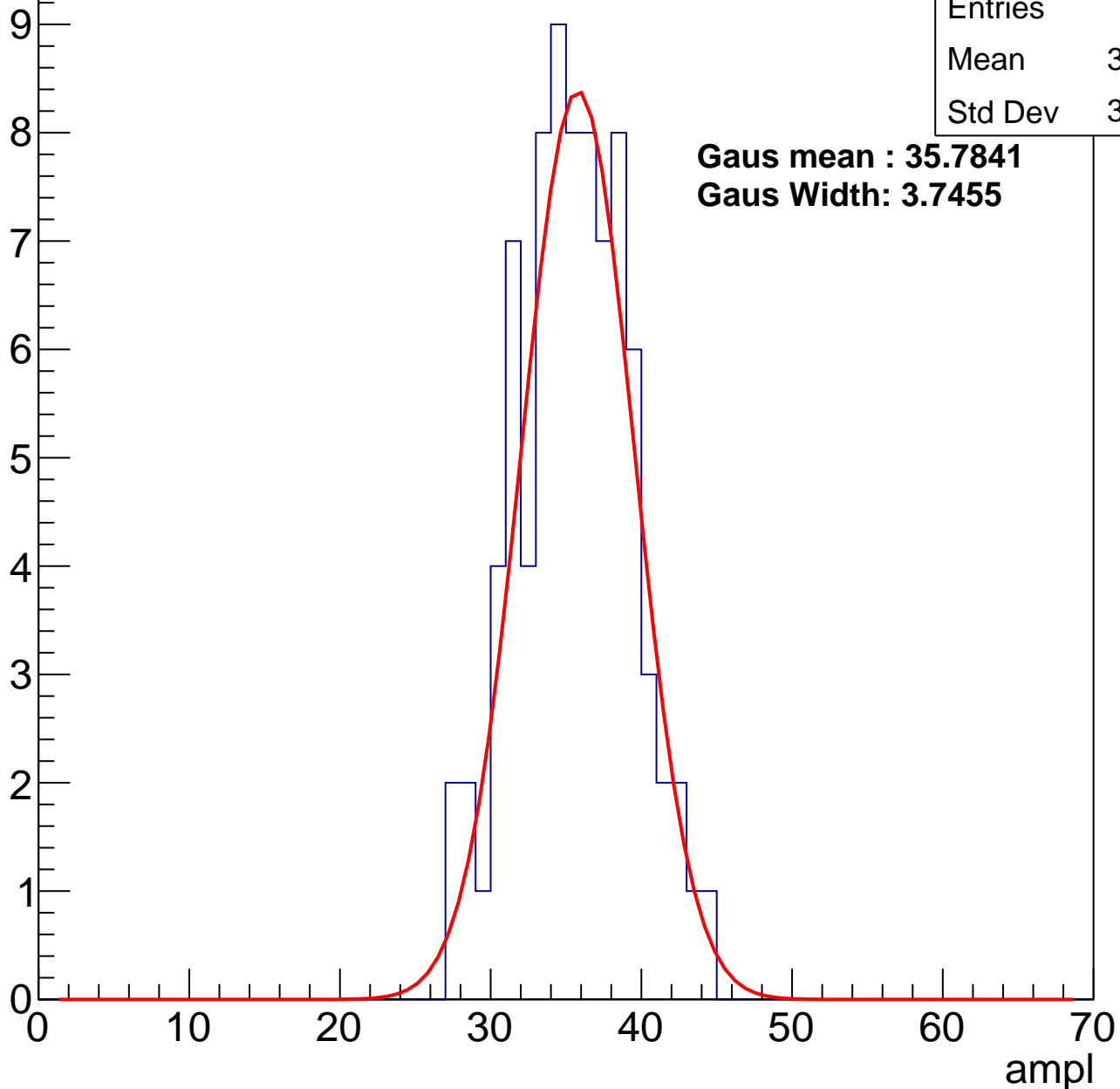
**Gaus Width: 3.4805**



# B1L101S, U19-ch94, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U19-ch94, adc2

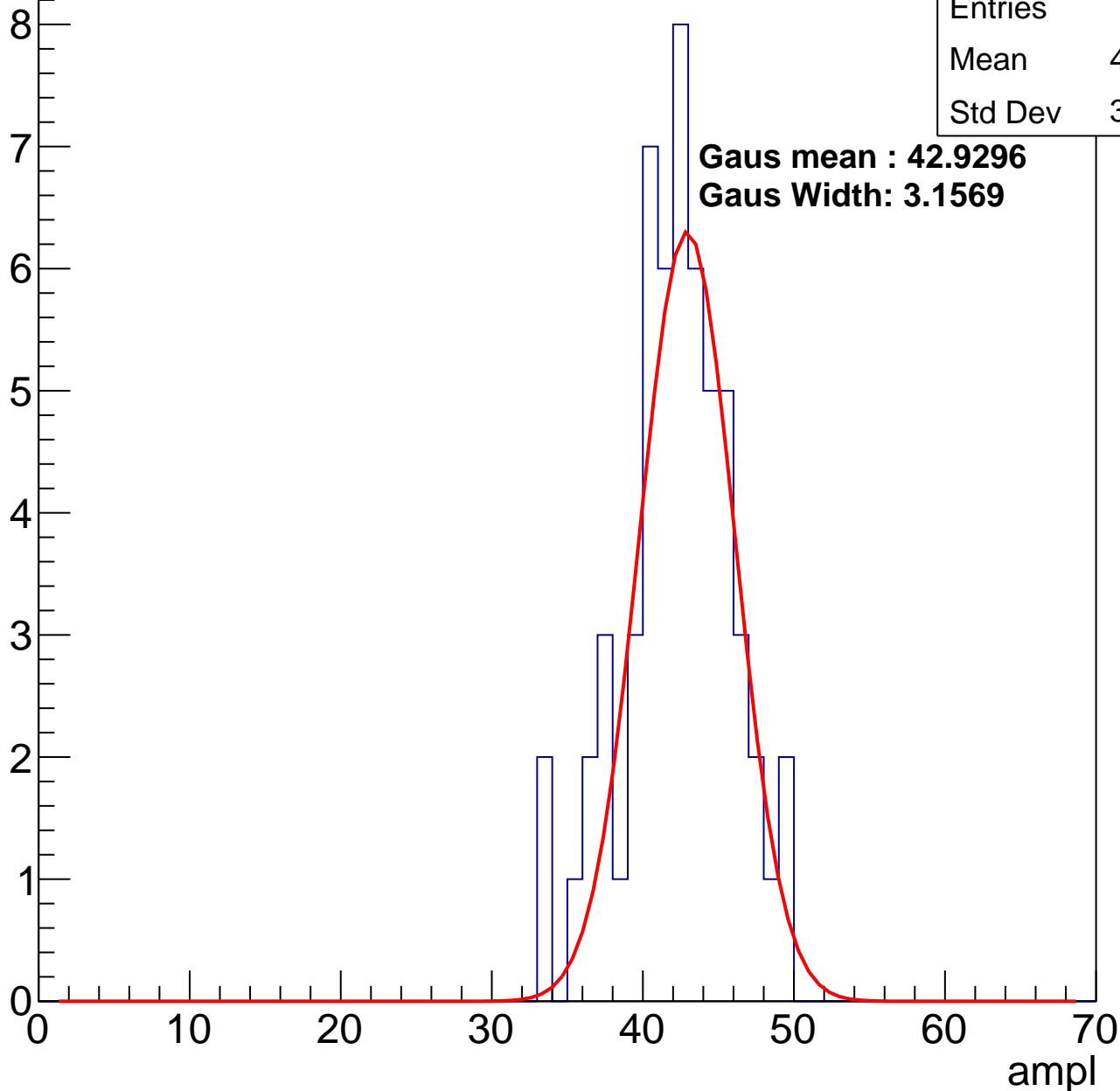
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	57
Mean	41.79
Std Dev	3.592

**Gaus mean : 42.9296**

**Gaus Width: 3.1569**

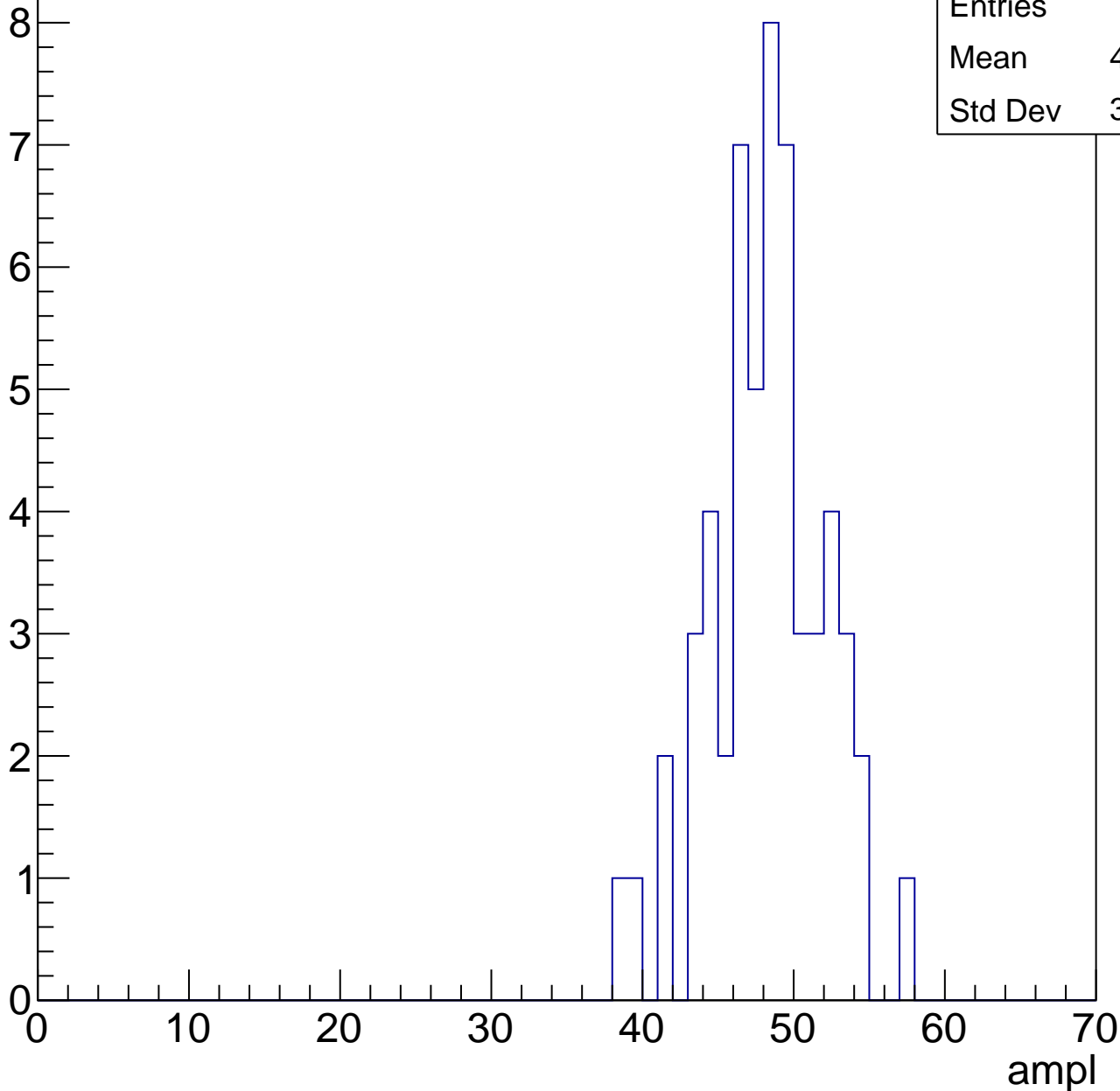


# B1L101S, U19-ch94, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	56
Mean	47.73
Std Dev	3.787

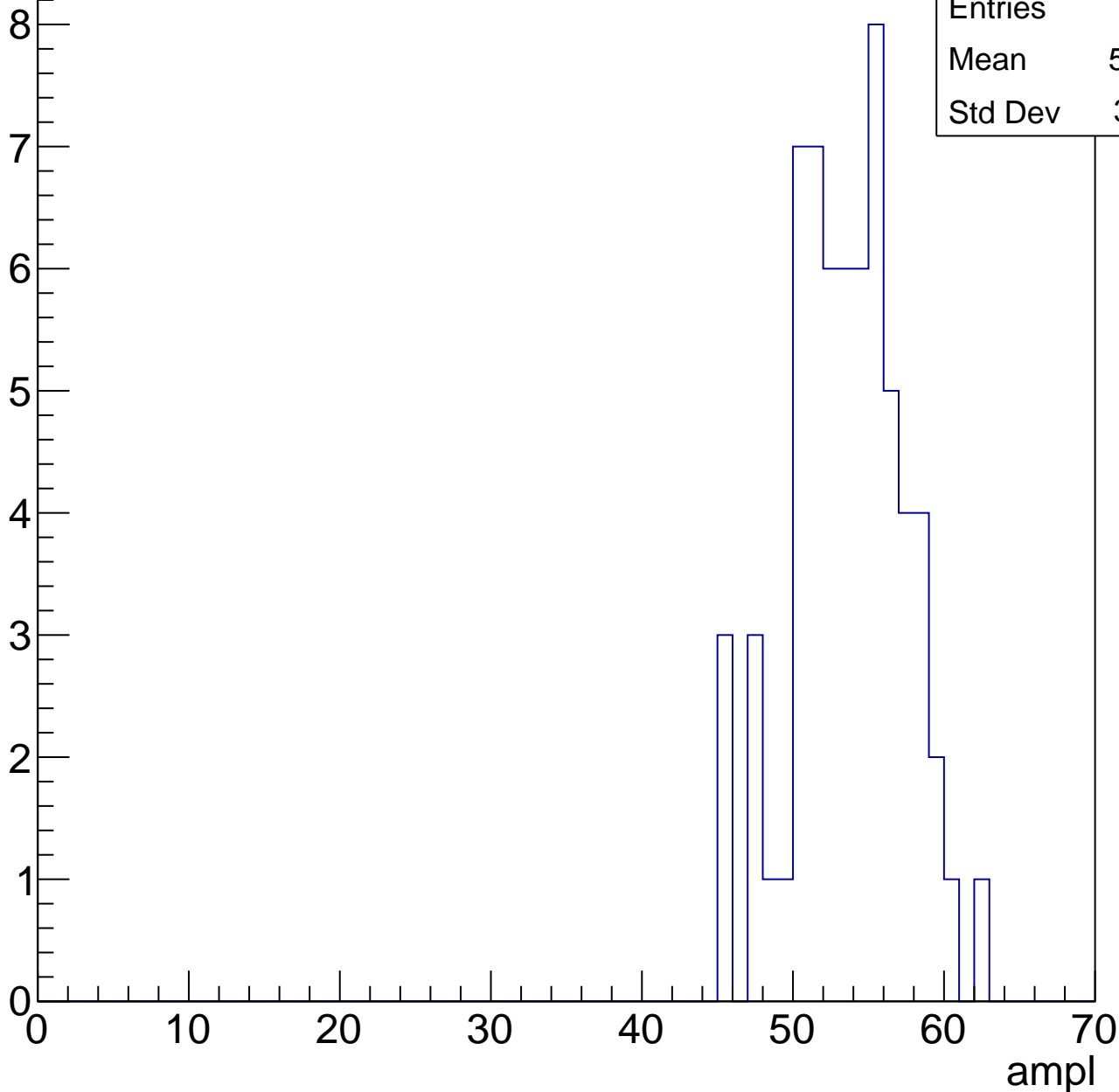


# B1L101S, U19-ch94, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	53.14
Std Dev	3.691



# B1L101S, U19-ch94, adc5

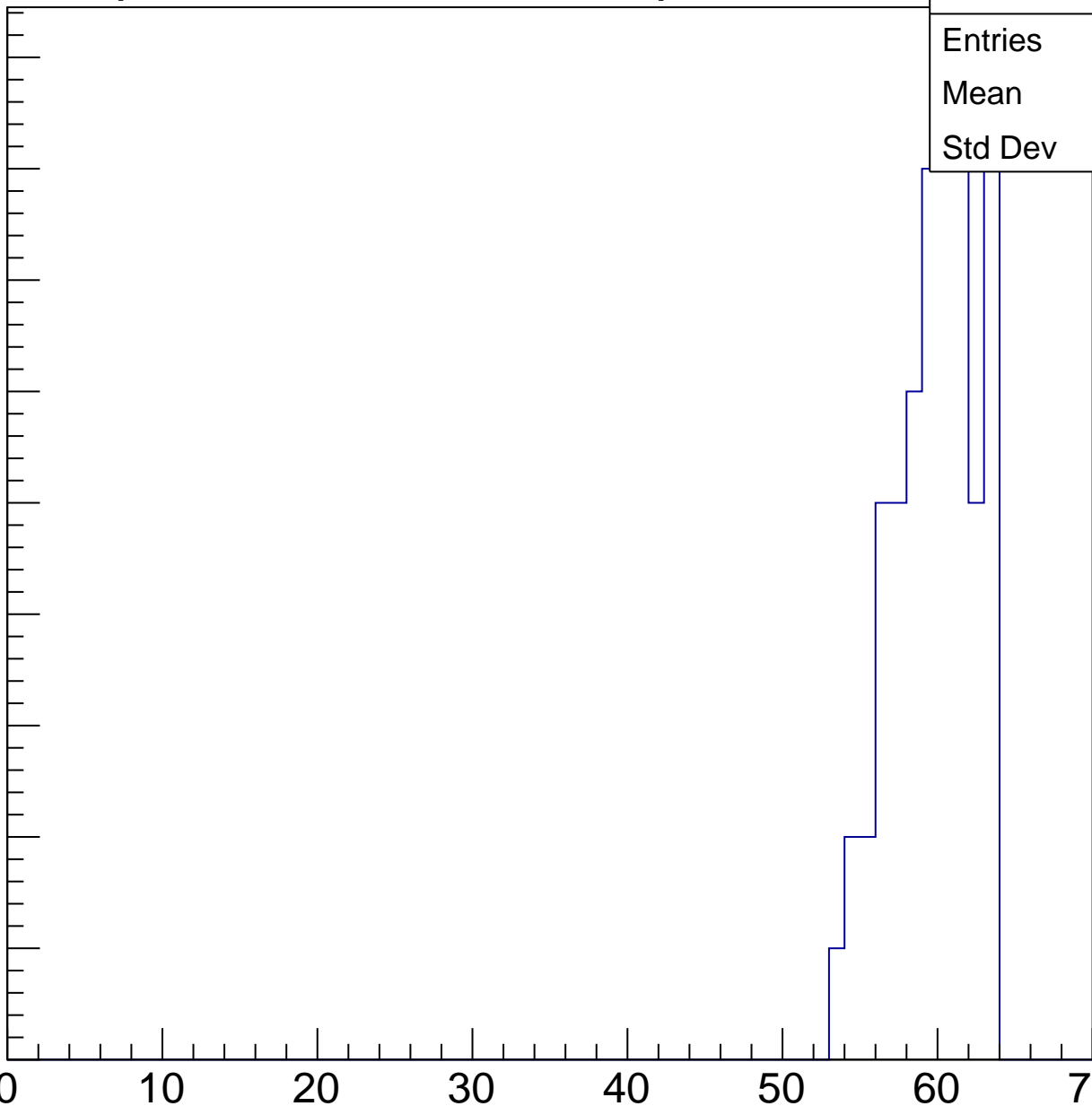
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	59
Mean	59.34
Std Dev	2.64

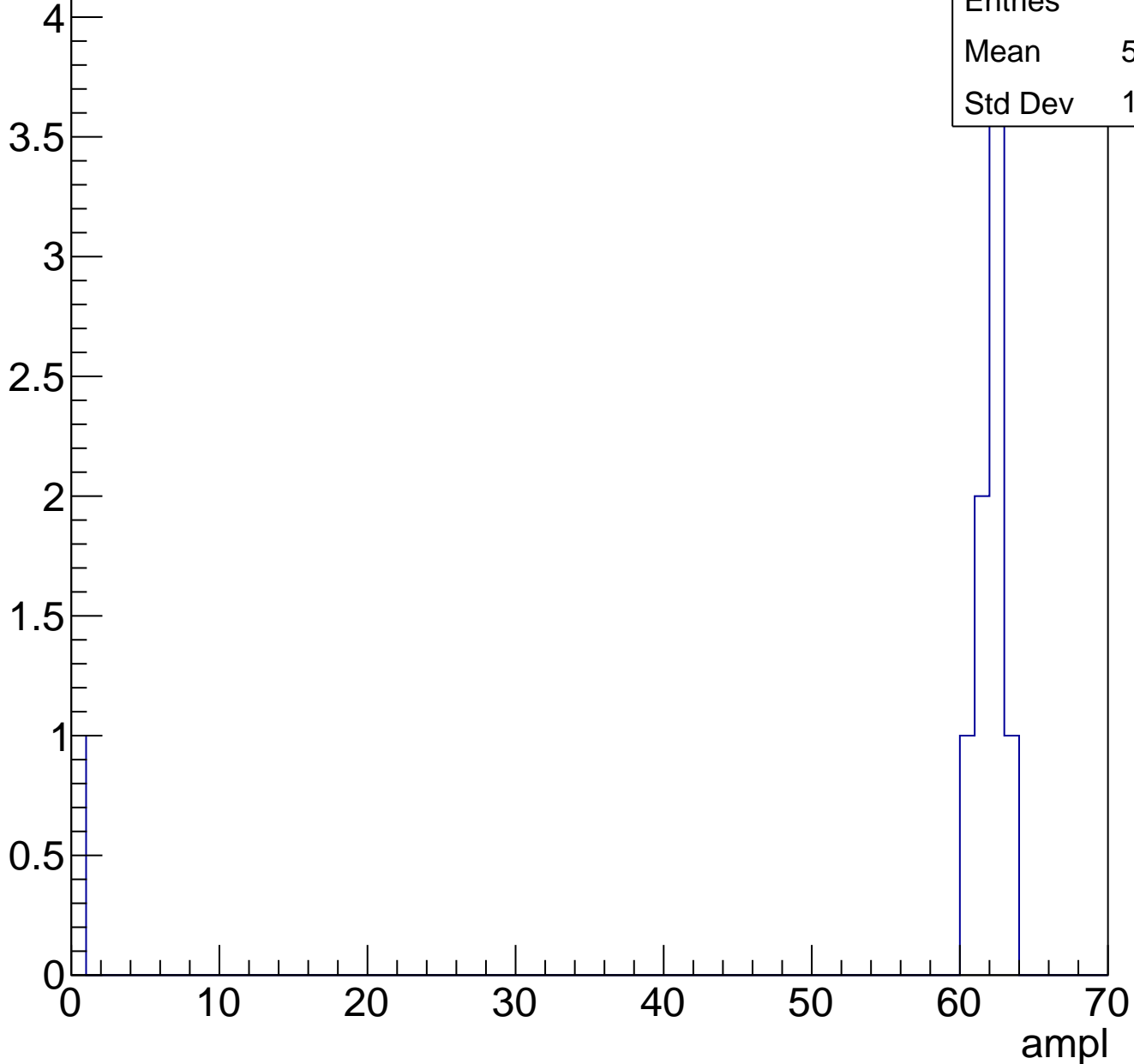
ampl



# B1L101S, U19-ch94, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U19-ch94, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U19-ch95, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	67
Mean	29.58
Std Dev	5.073

**Gaus mean : 30.5695**

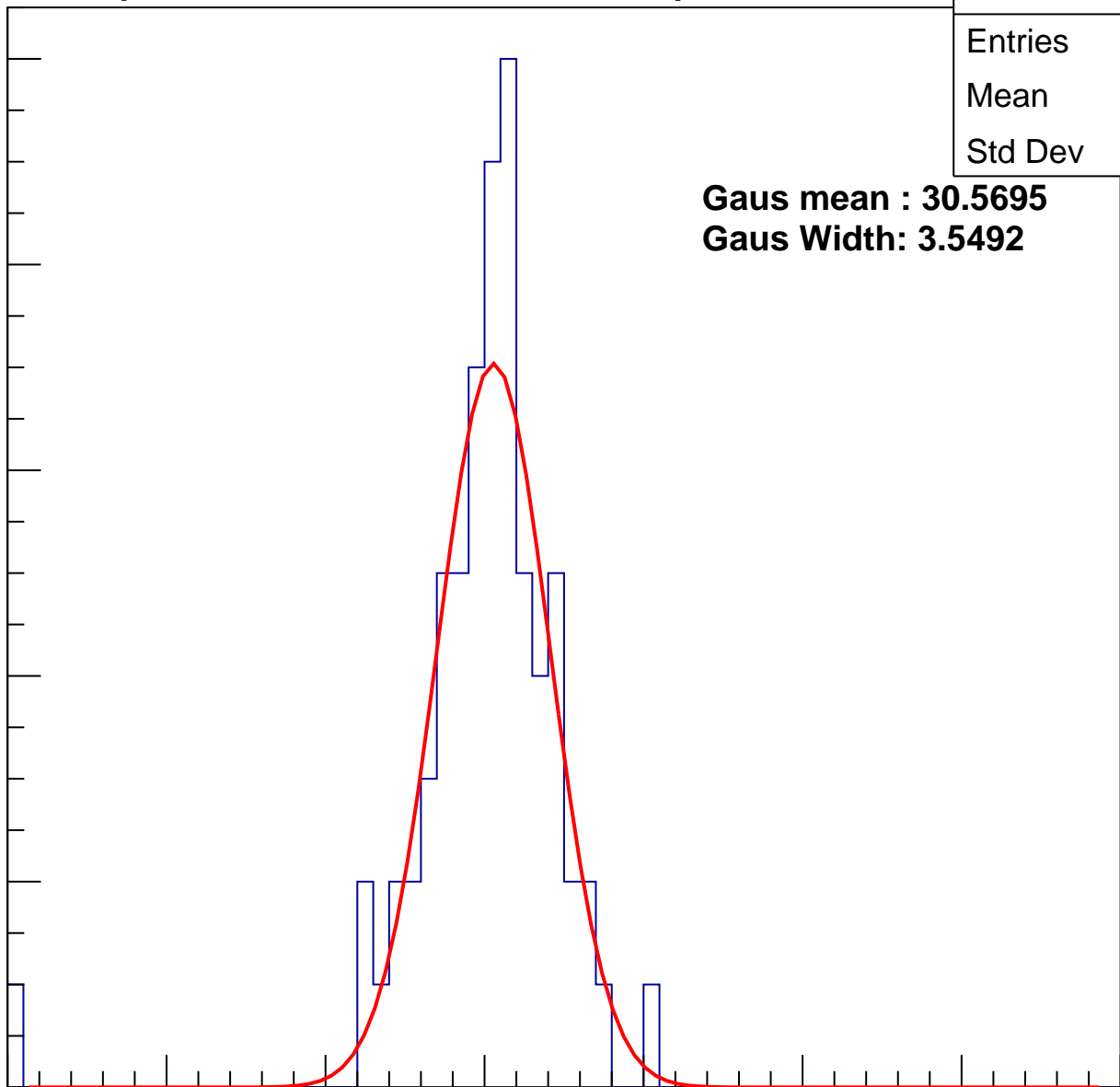
**Gaus Width: 3.5492**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U19-ch95, adc1

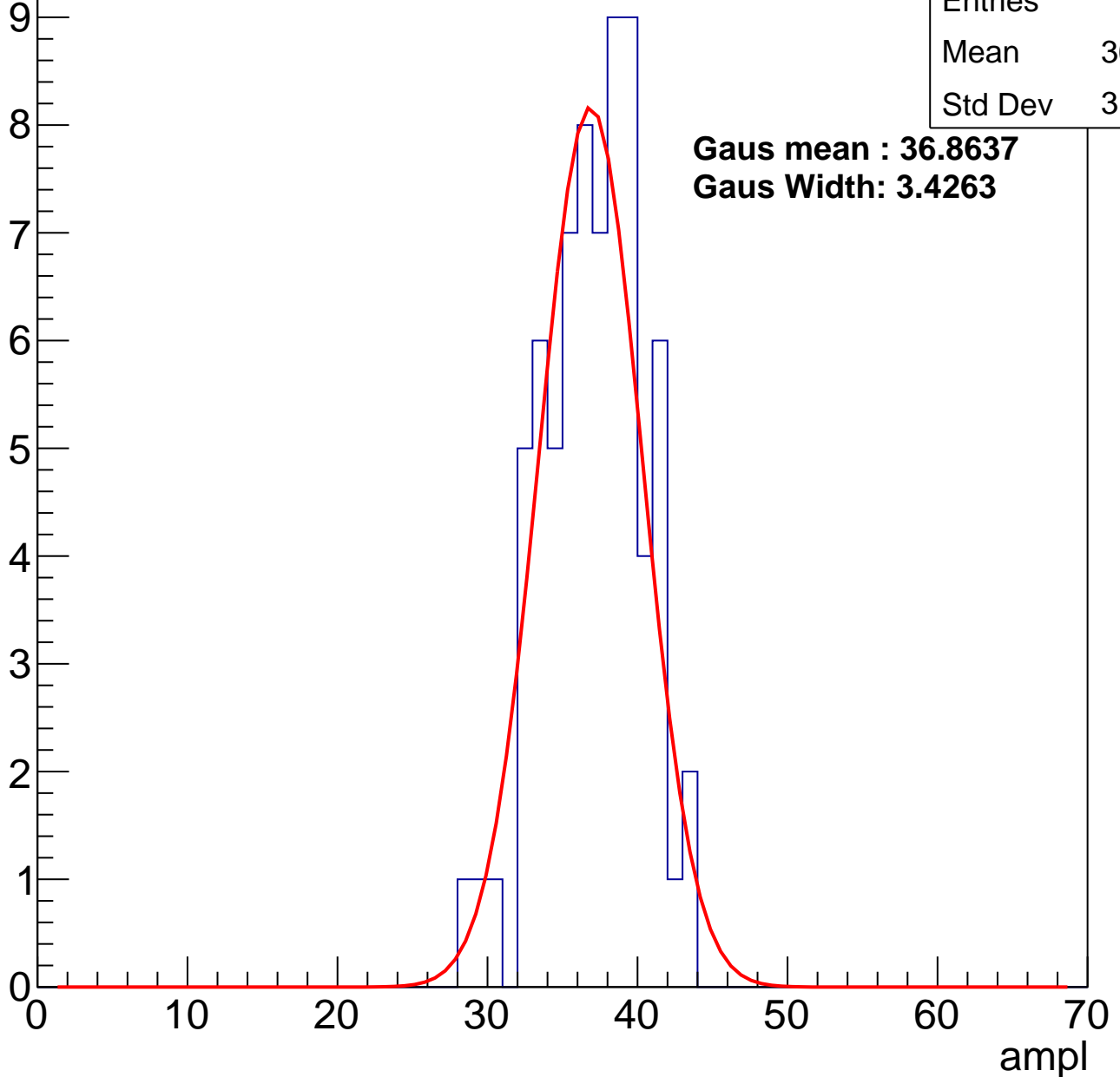
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	72
Mean	36.58
Std Dev	3.244

**Gaus mean : 36.8637**

**Gaus Width: 3.4263**



# B1L101S, U19-ch95, adc2

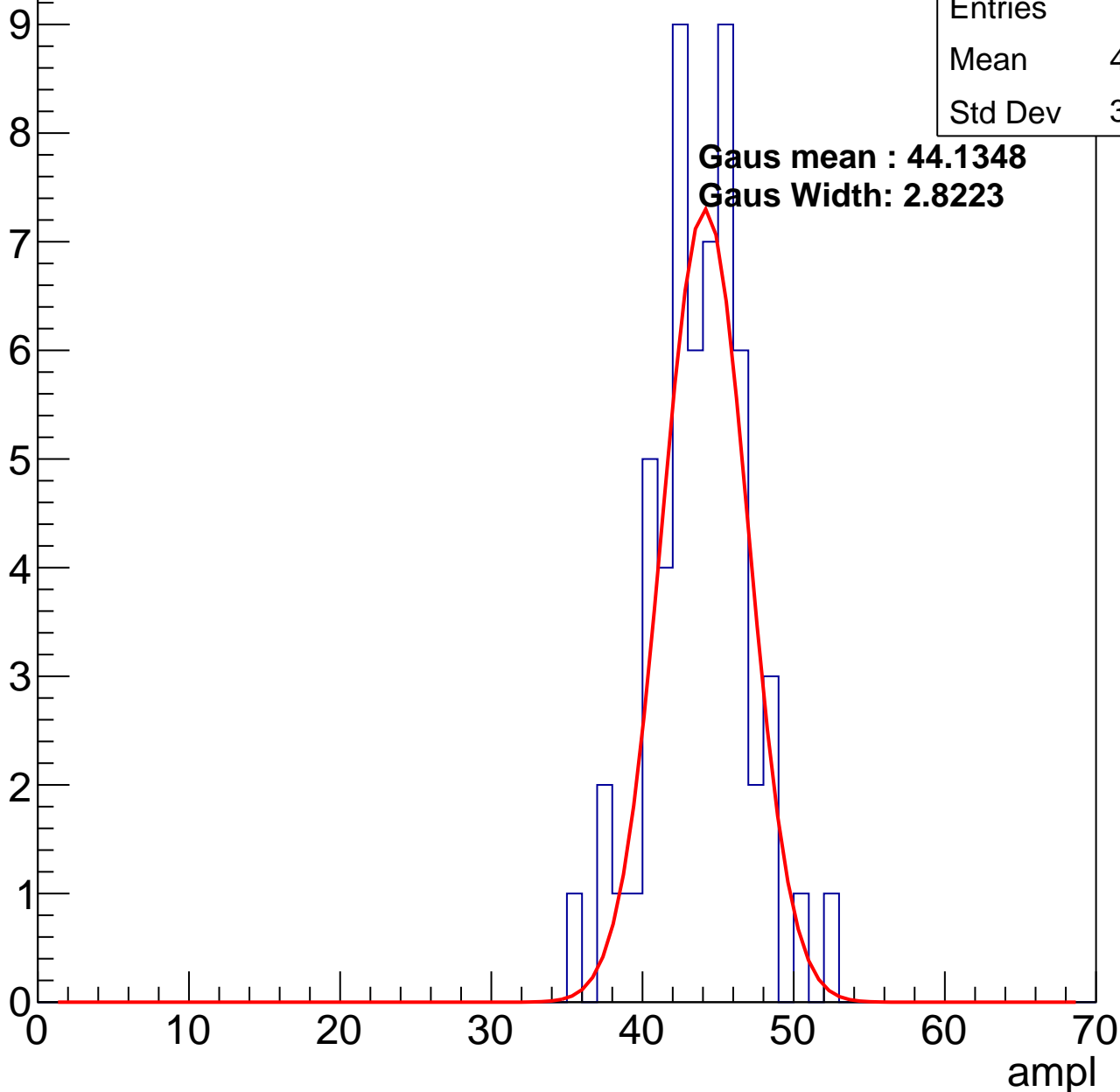
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	58
Mean	43.36
Std Dev	3.144

**Gaus mean : 44.1348**

**Gaus Width: 2.8223**

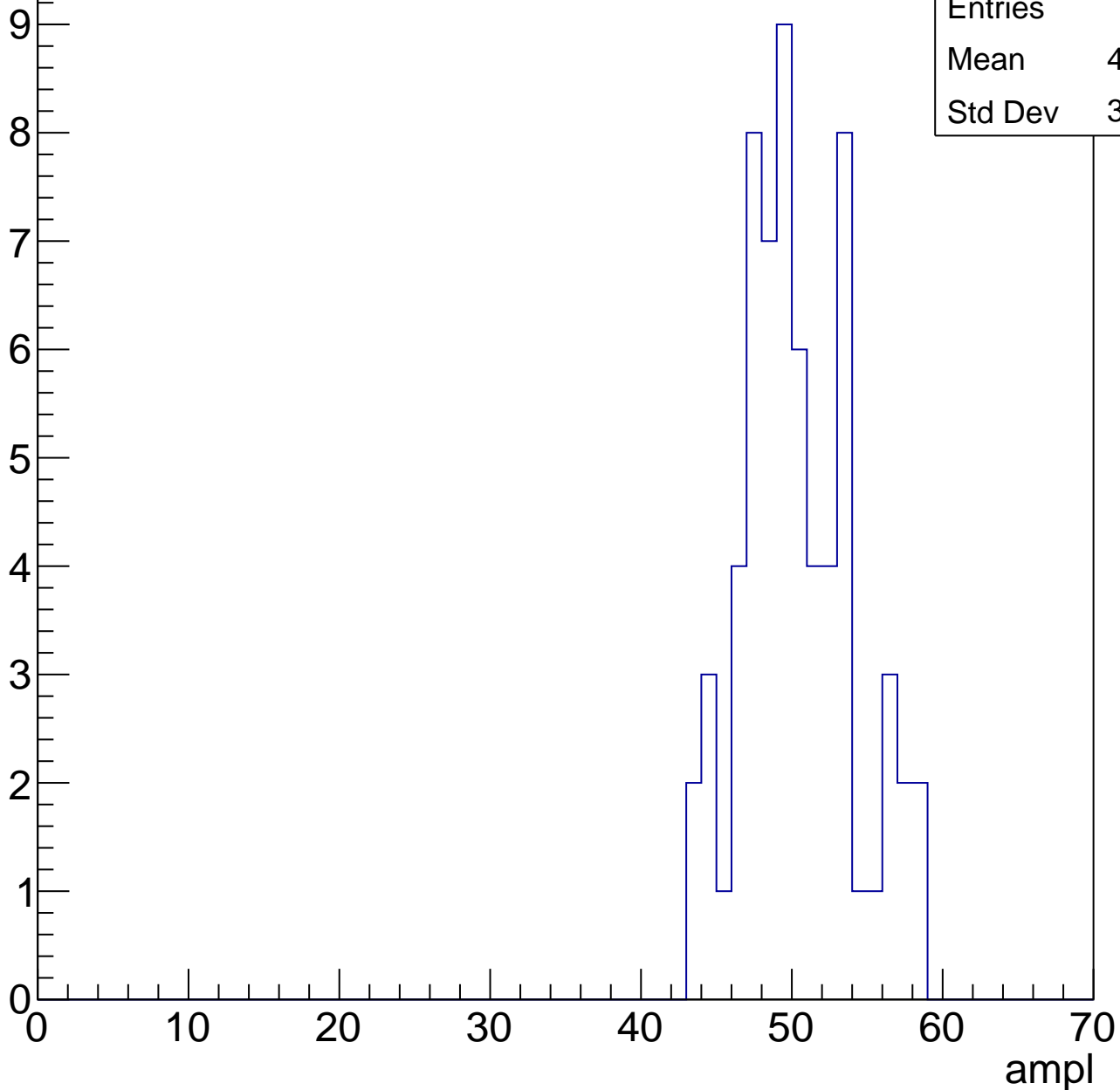


# B1L101S, U19-ch95, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	49.89
Std Dev	3.659

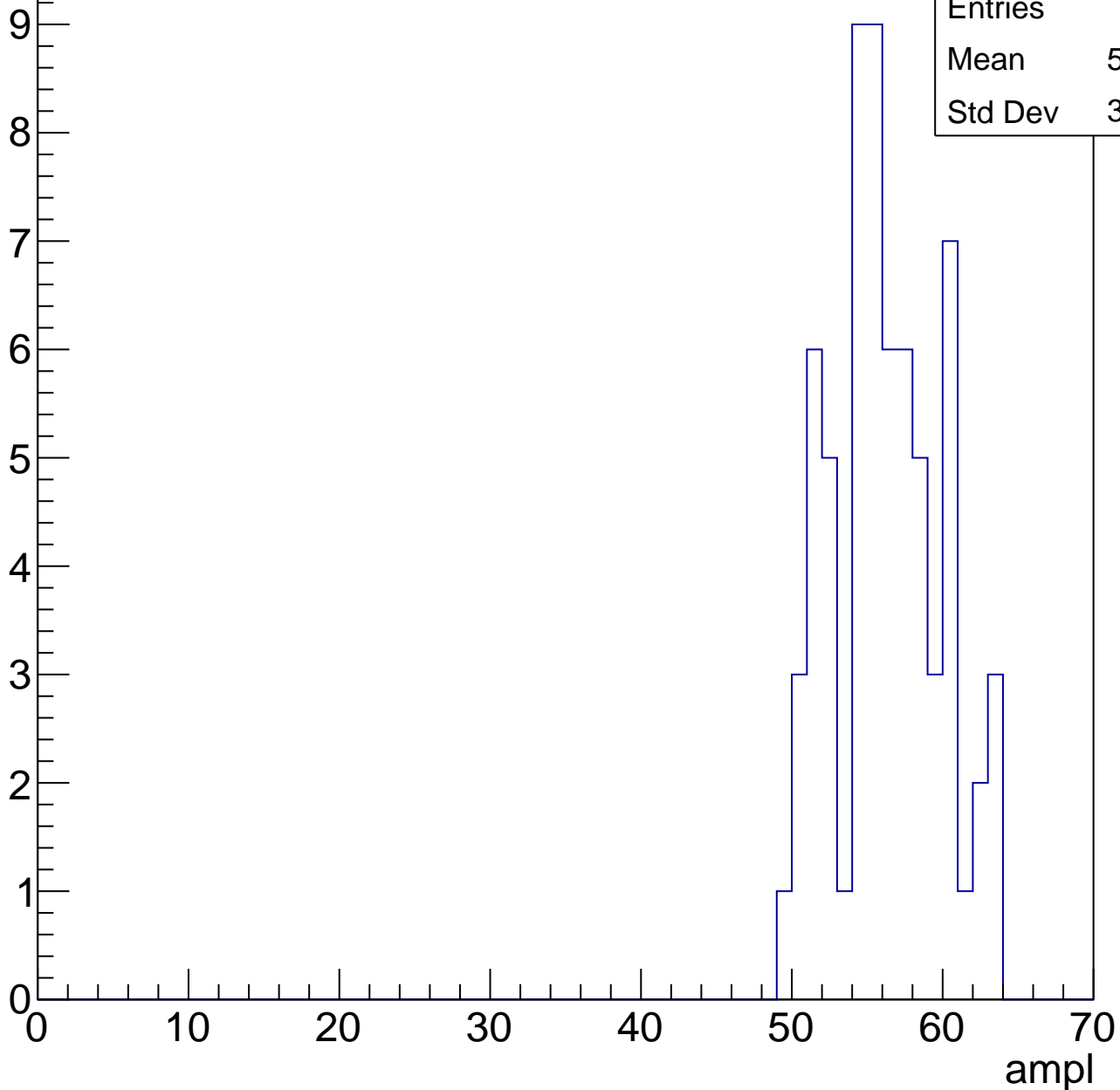


# B1L101S, U19-ch95, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	67
Mean	55.79
Std Dev	3.556

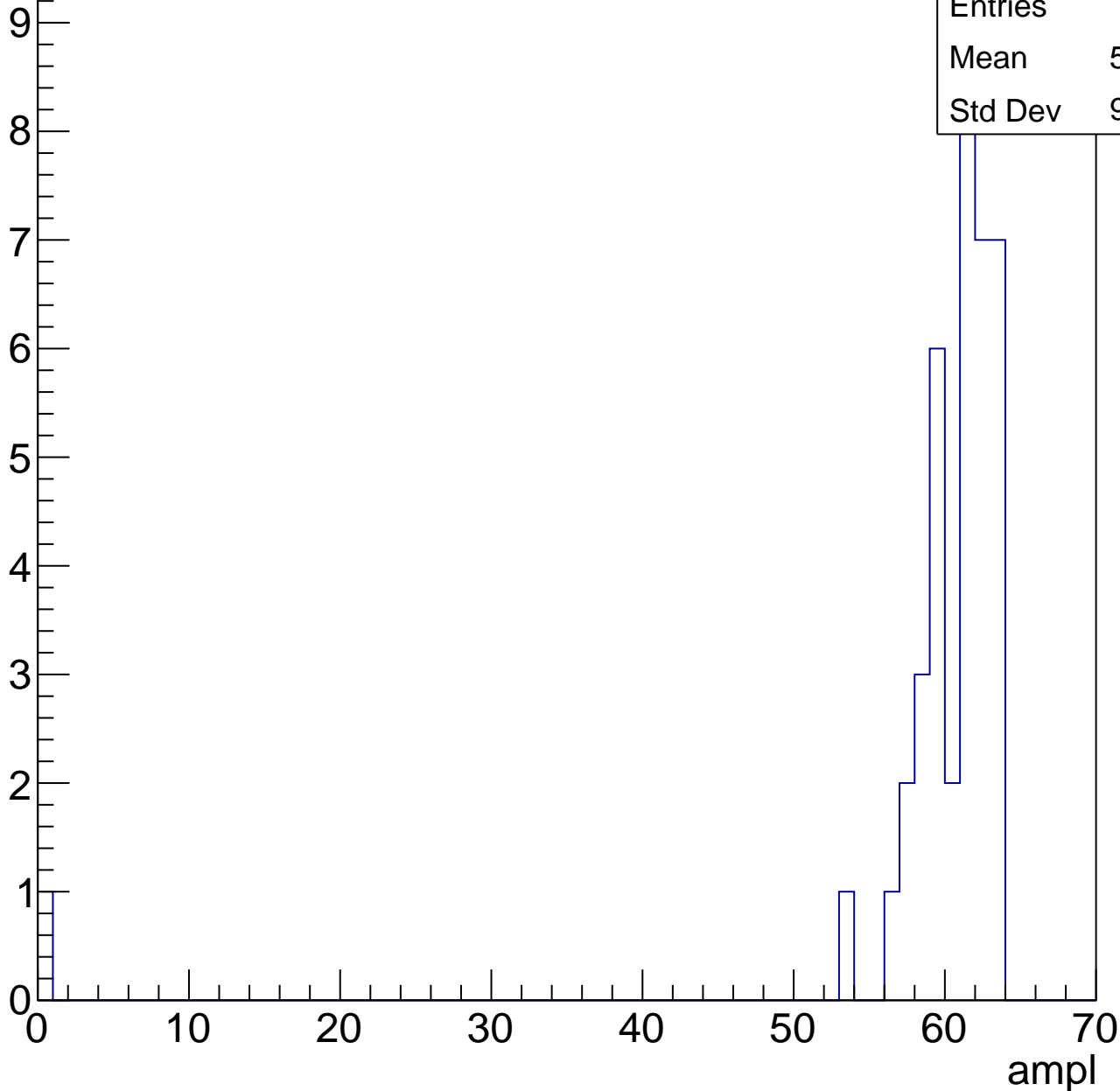


# B1L101S, U19-ch95, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

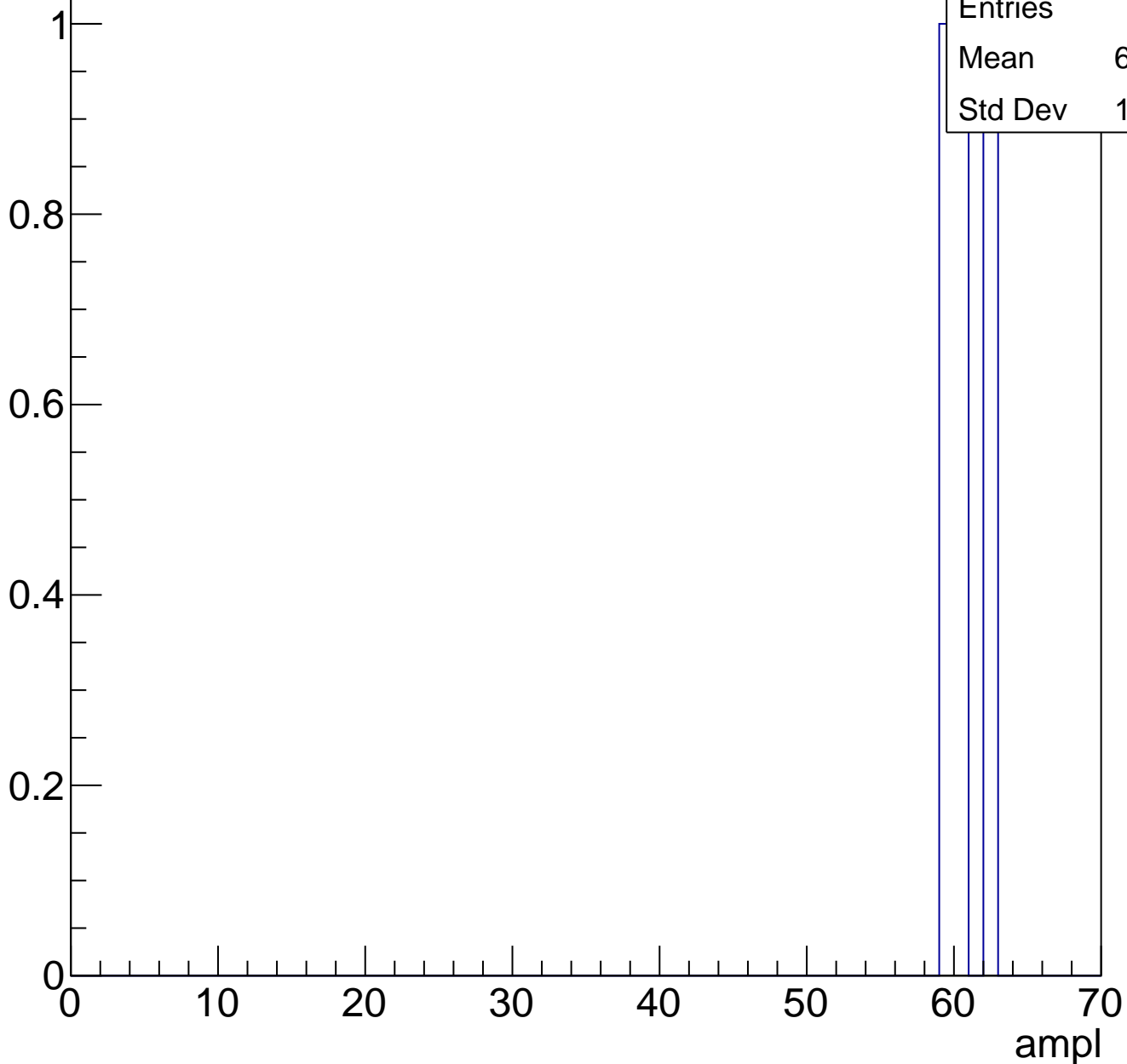
Entries	39
Mean	58.85
Std Dev	9.805



# B1L101S, U19-ch95, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U19-ch95, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L101S, U19-ch96, adc0

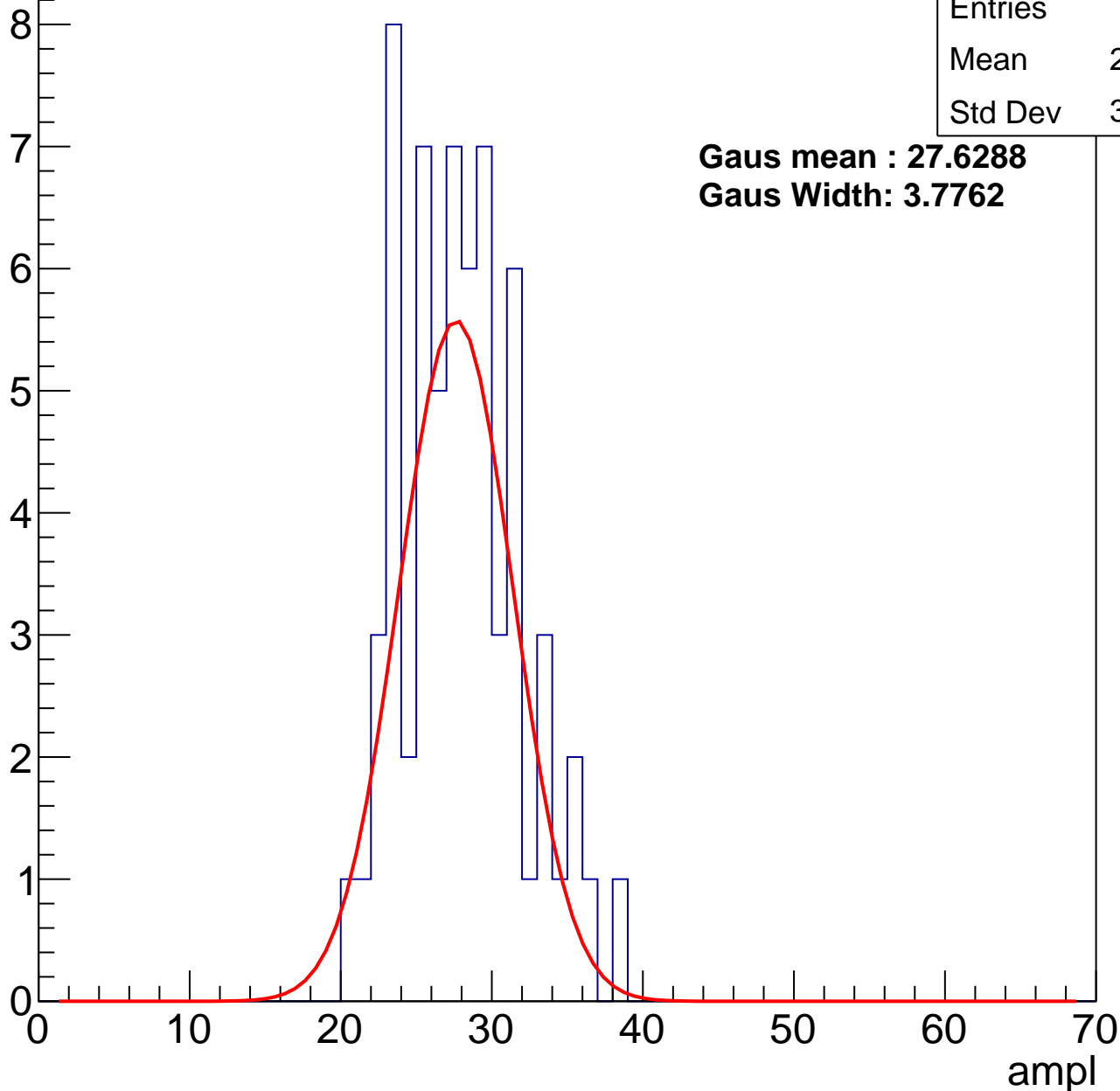
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	27.52
Std Dev	3.903

**Gaus mean : 27.6288**

**Gaus Width: 3.7762**



# B1L101S, U19-ch96, adc1

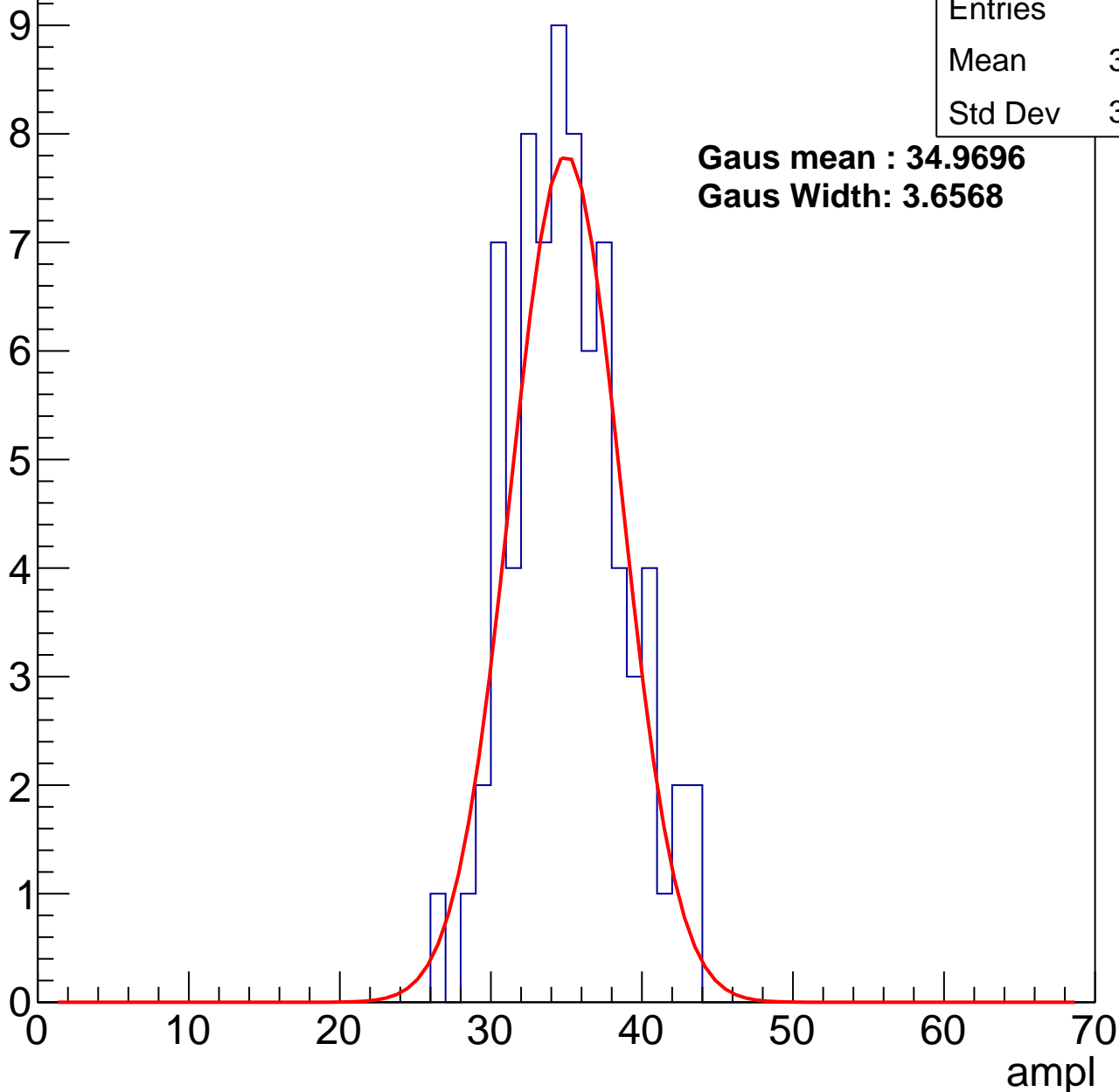
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	76
Mean	34.66
Std Dev	3.665

**Gaus mean : 34.9696**

**Gaus Width: 3.6568**



# B1L101S, U19-ch96, adc2

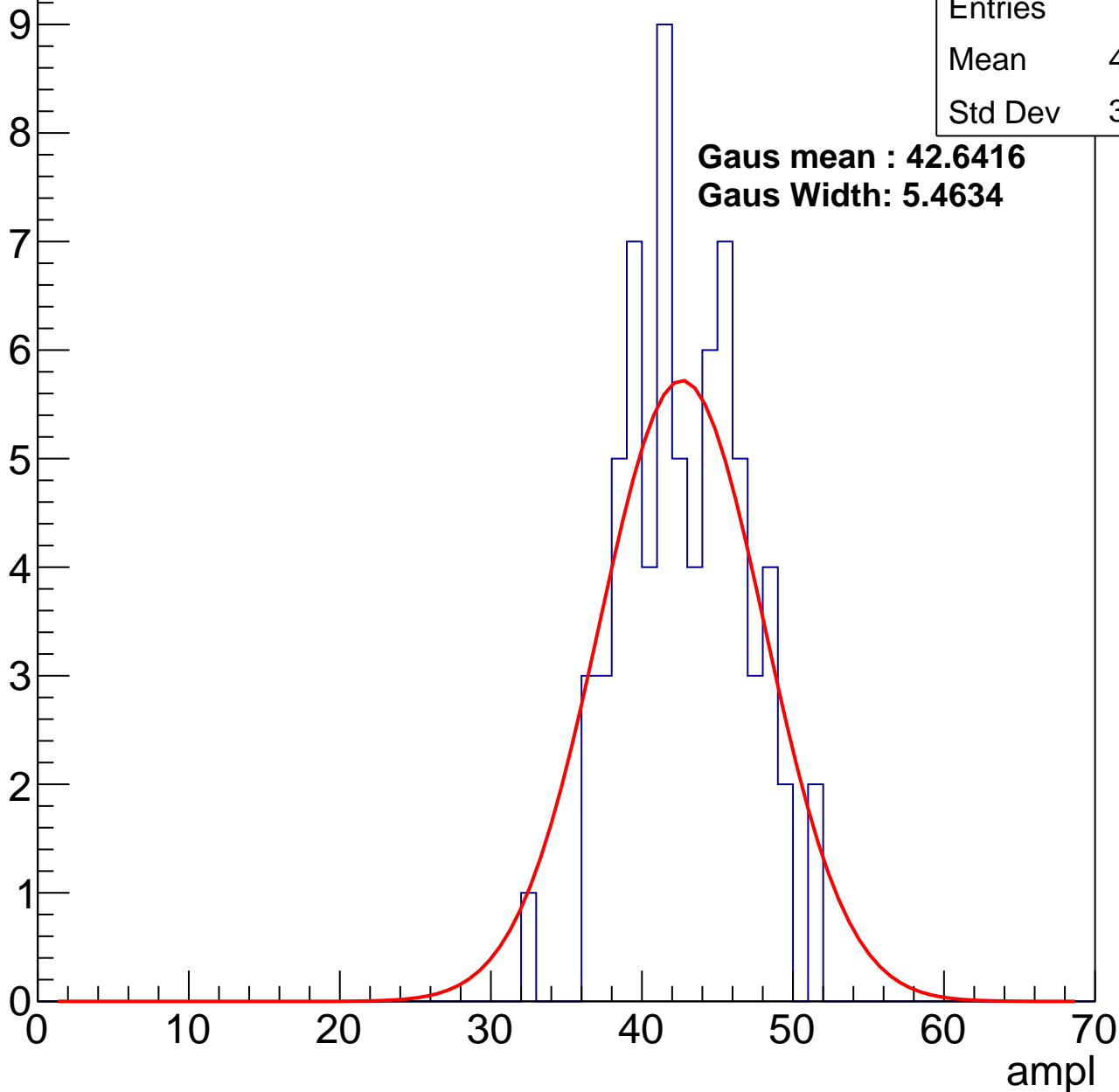
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	42.39
Std Dev	3.947

**Gaus mean : 42.6416**

**Gaus Width: 5.4634**

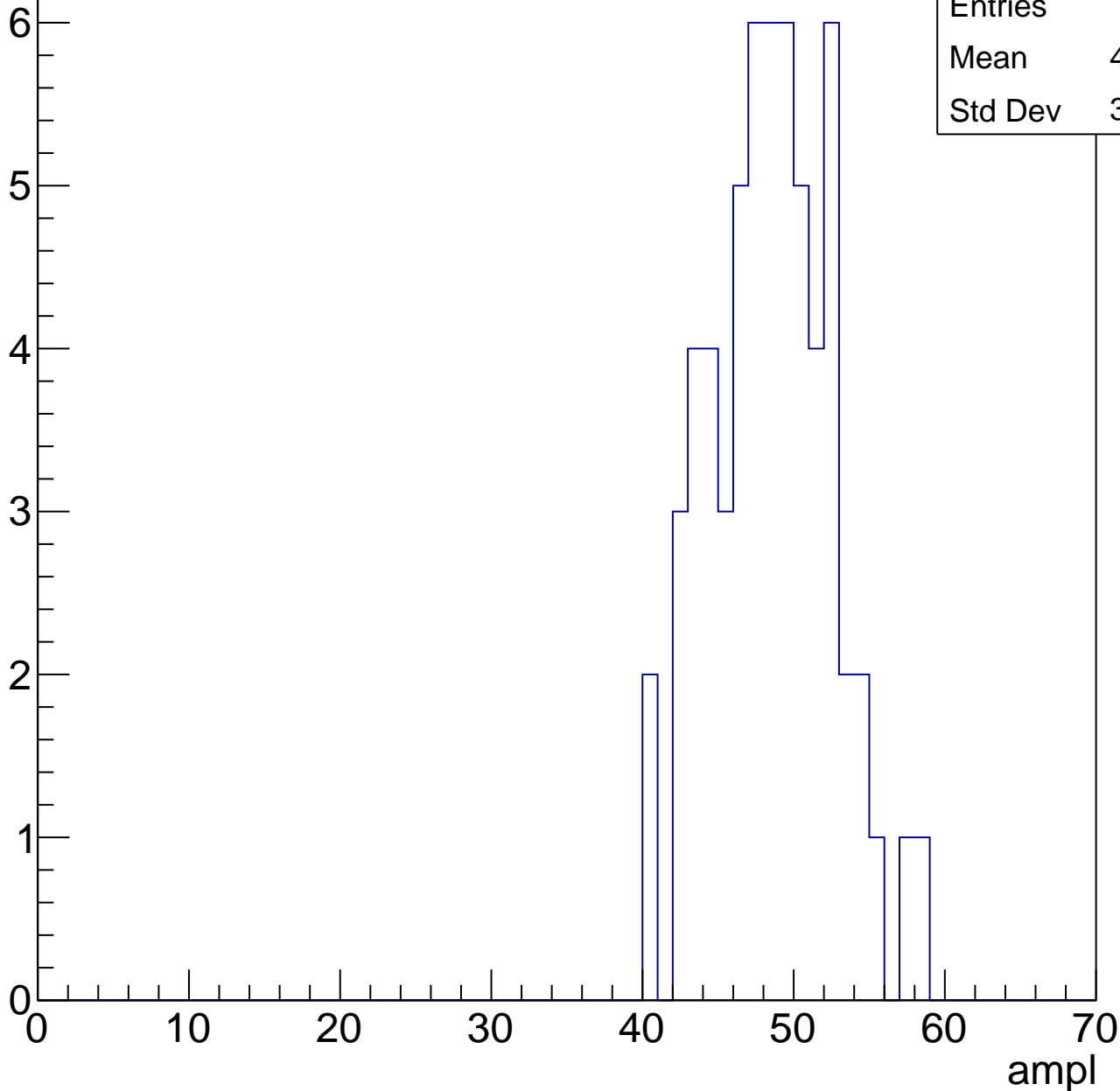


# B1L101S, U19-ch96, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	48.08
Std Dev	3.972

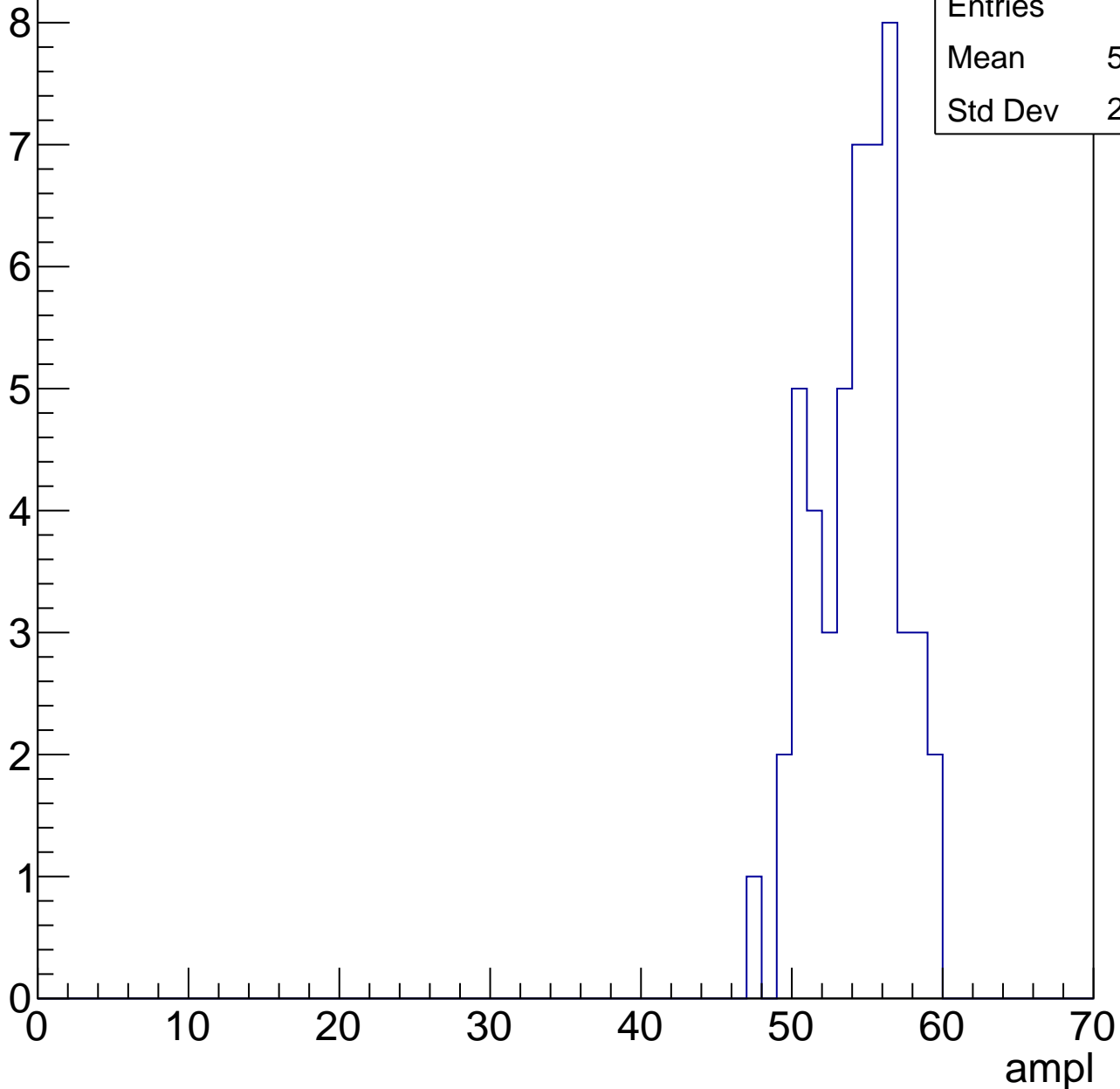


# B1L101S, U19-ch96, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

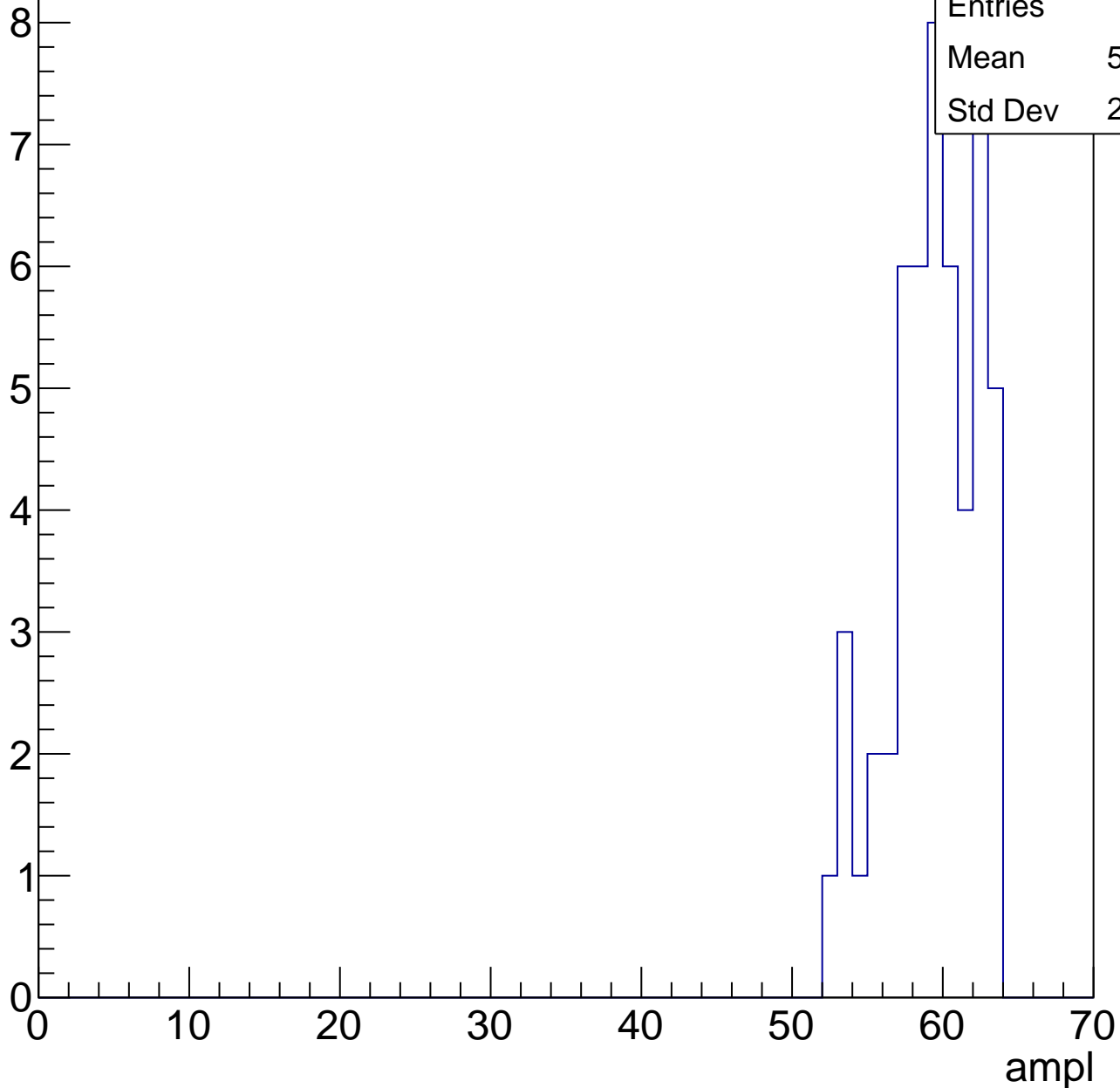
Entries	50
Mean	53.88
Std Dev	2.812



# B1L101S, U19-ch96, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

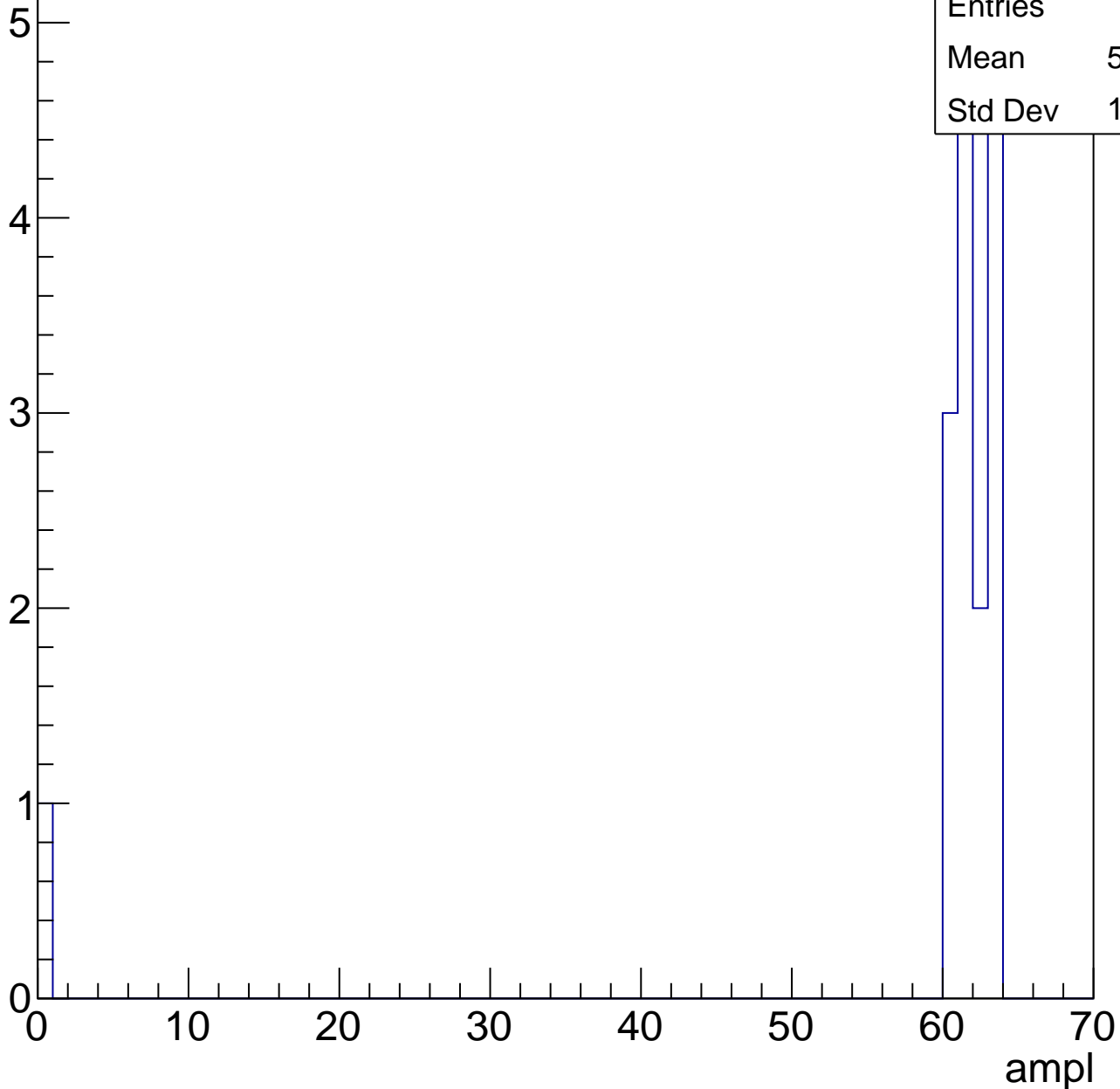


# B1L101S, U19-ch96, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	16
Mean	57.75
Std Dev	14.95

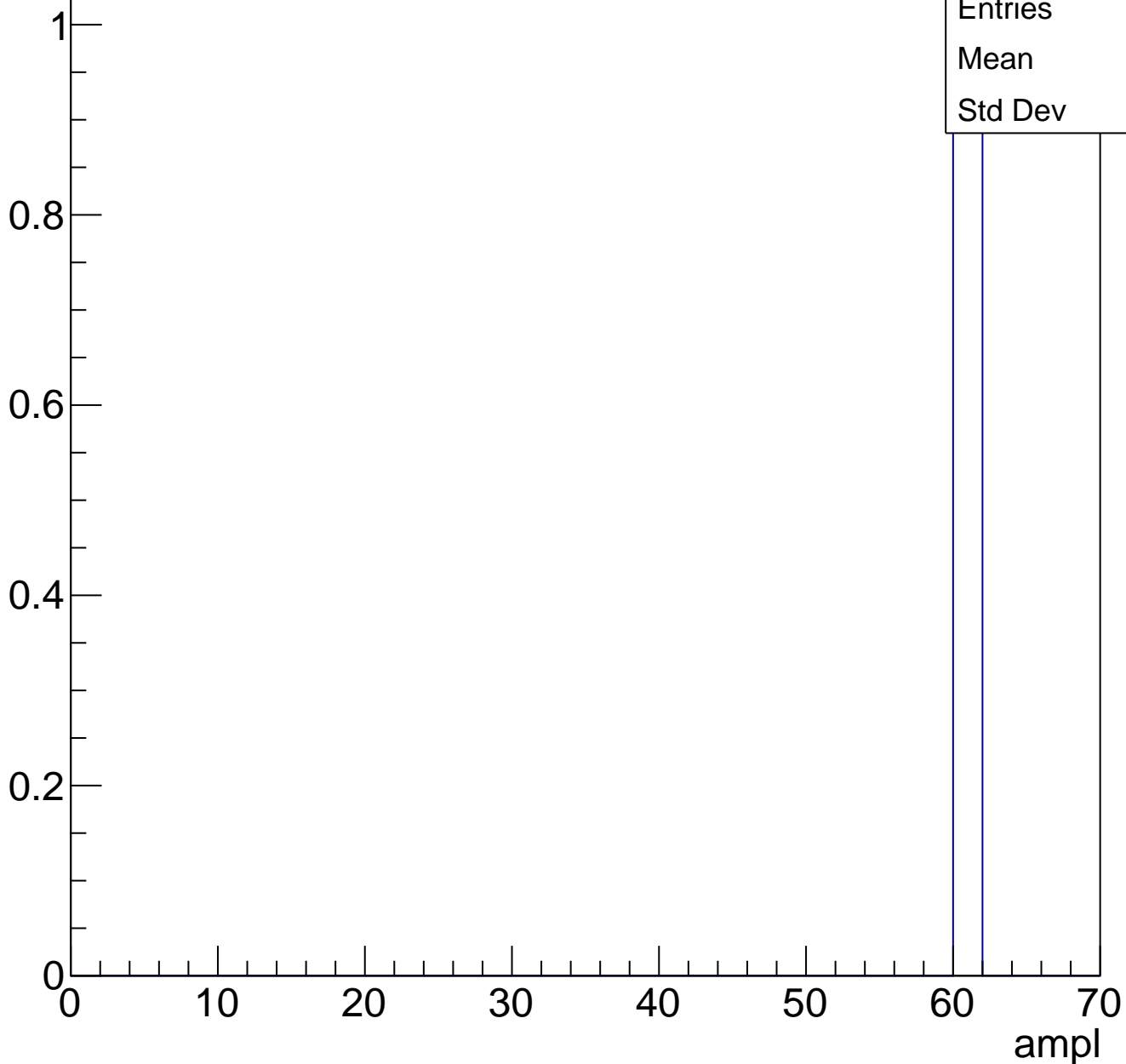




# B1L101S, U19-ch96, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U19-ch97, adc0

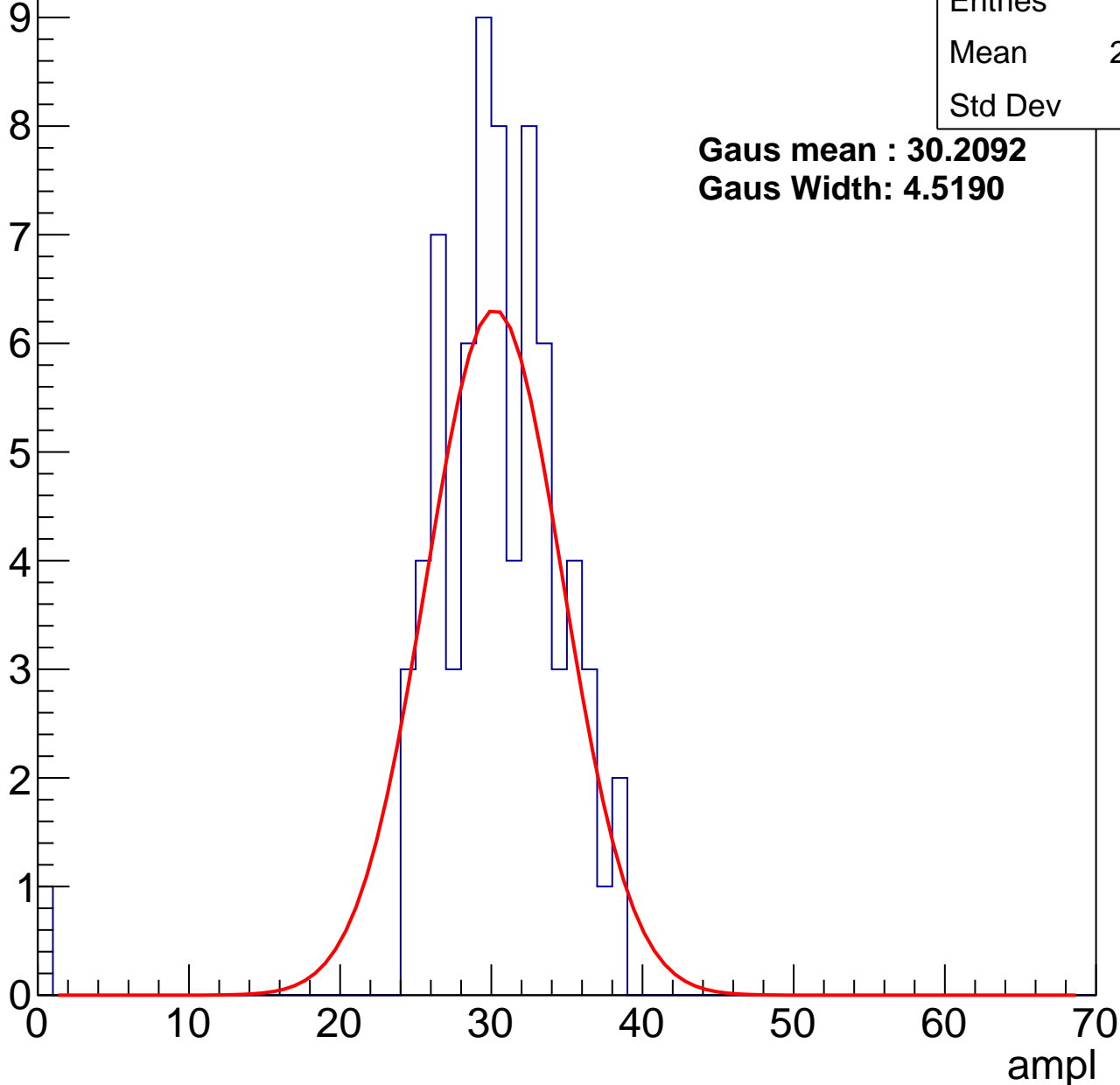
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	72
Mean	29.79
Std Dev	5

**Gaus mean : 30.2092**

**Gaus Width: 4.5190**



# B1L101S, U19-ch97, adc1

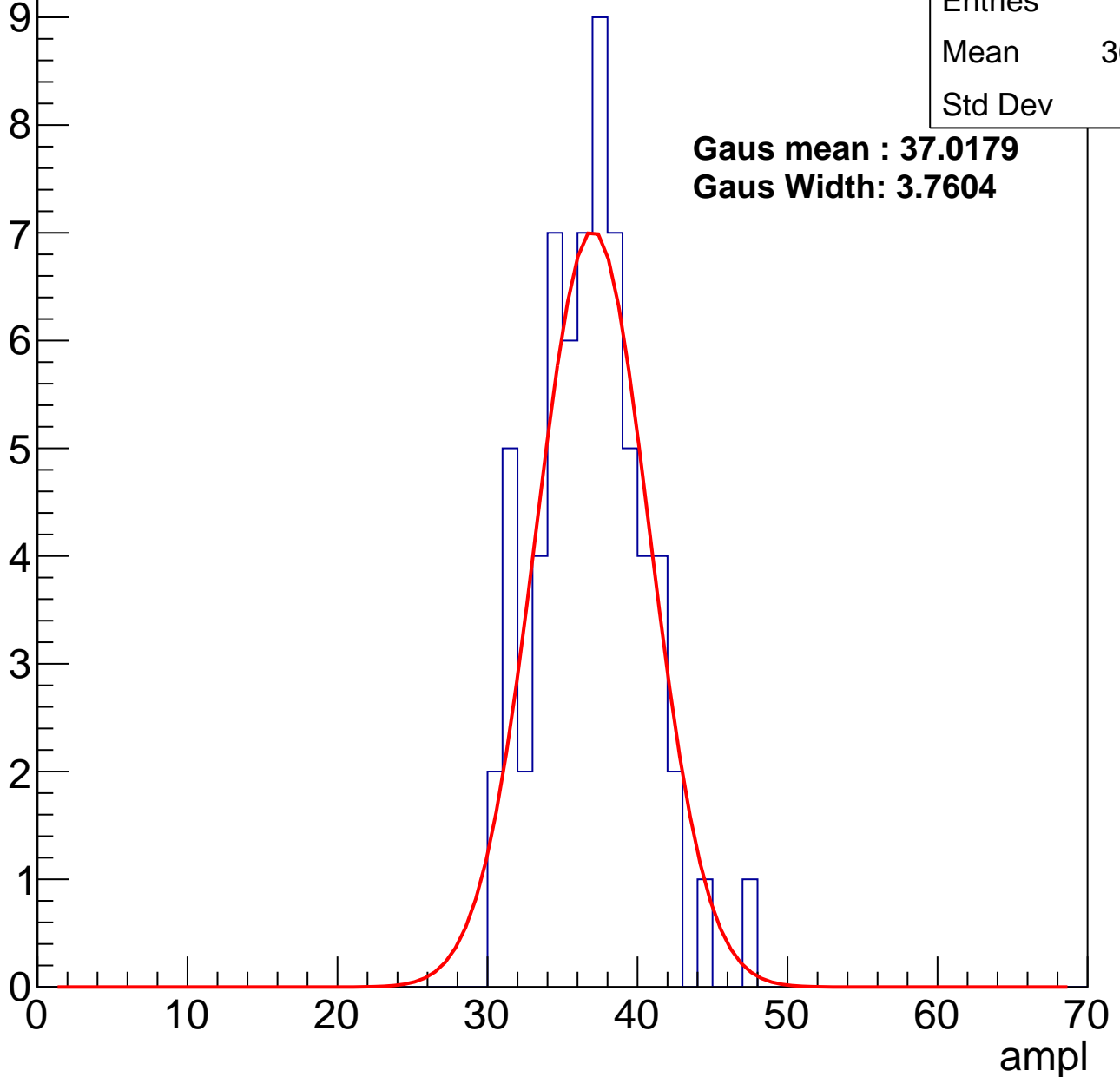
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	66
Mean	36.42
Std Dev	3.46

**Gaus mean : 37.0179**

**Gaus Width: 3.7604**



# B1L101S, U19-ch97, adc2

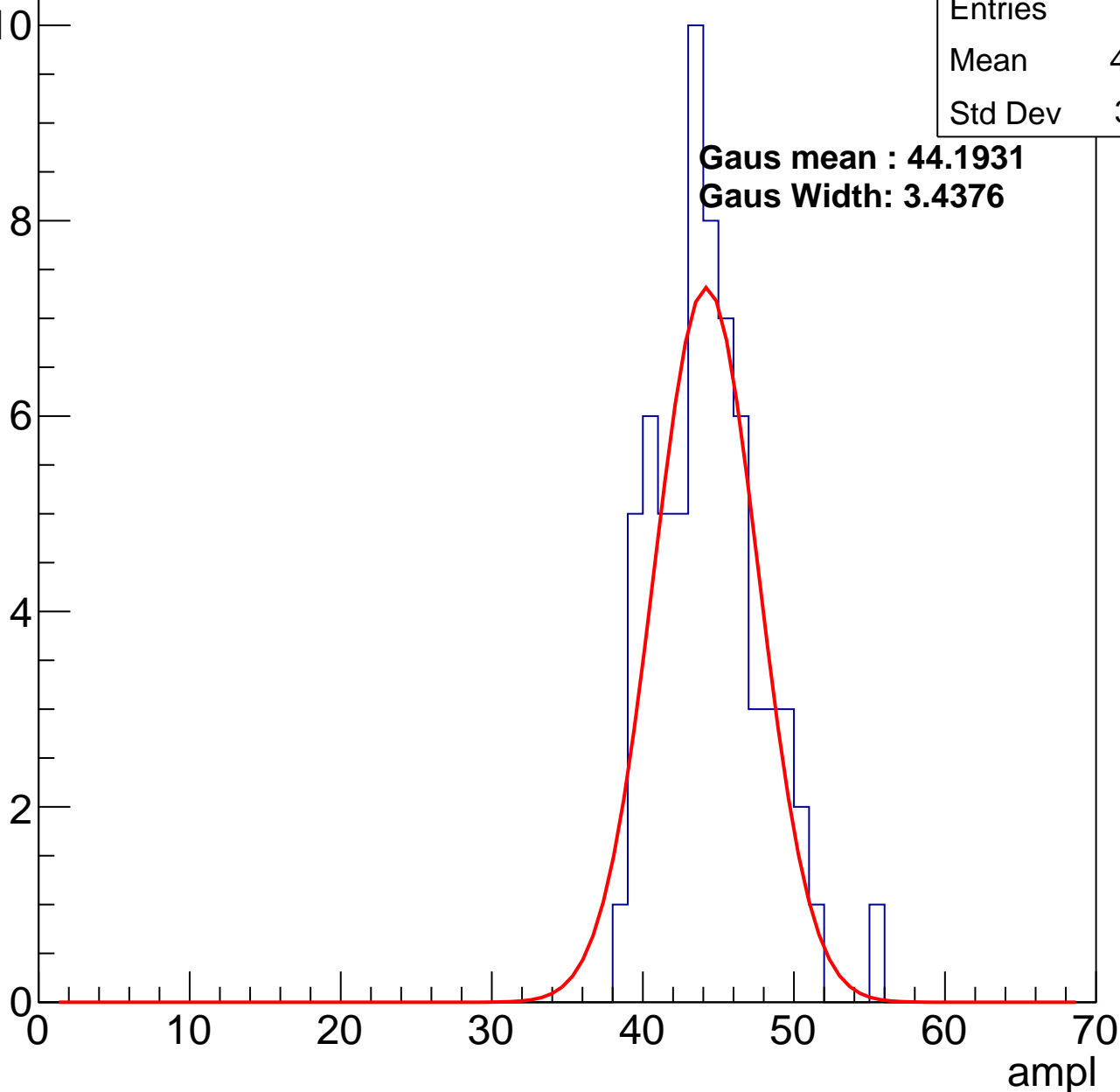
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	66
Mean	43.92
Std Dev	3.381

**Gaus mean : 44.1931**

**Gaus Width: 3.4376**

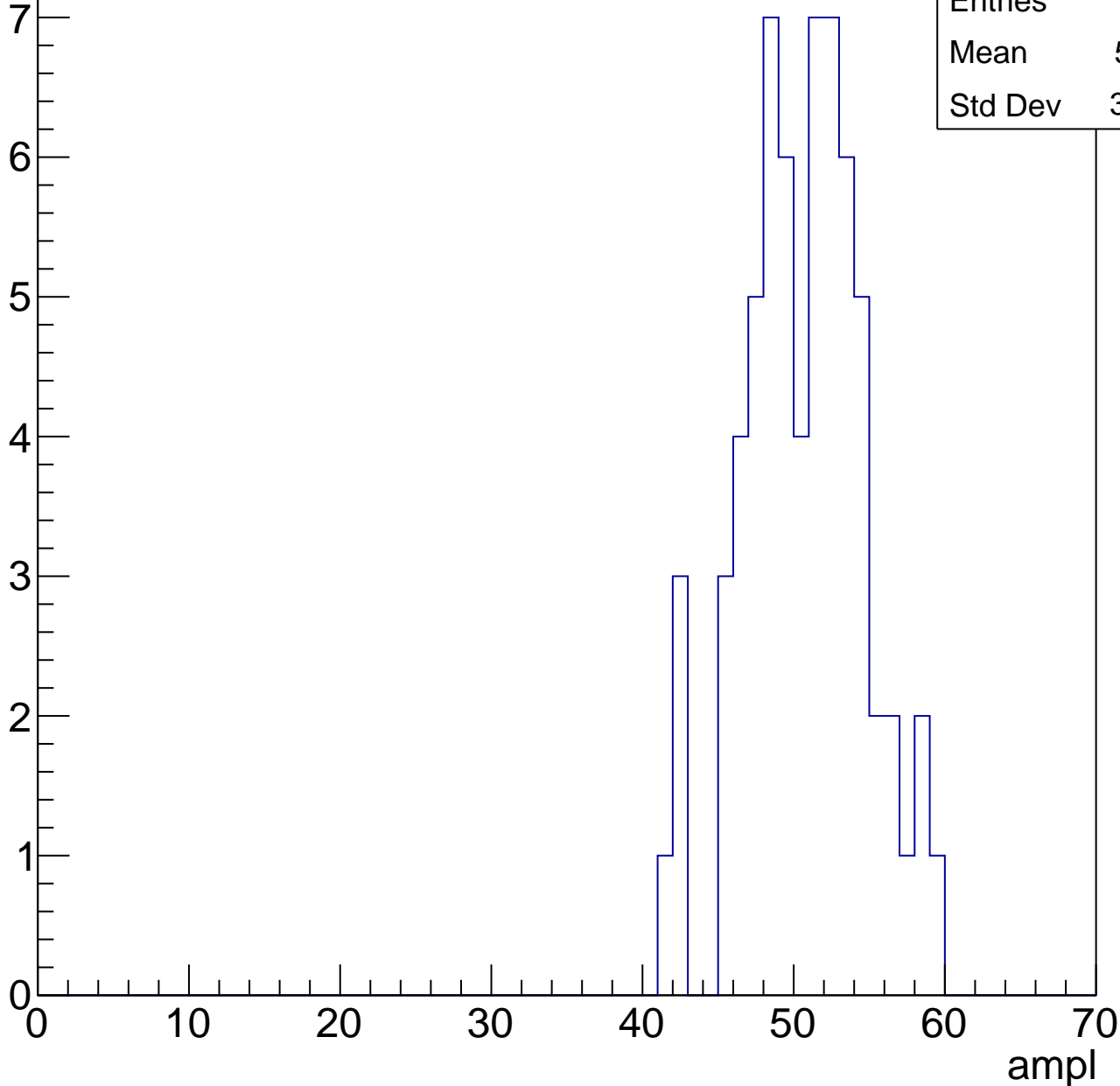


# B1L101S, U19-ch97, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	66
Mean	50.21
Std Dev	3.964

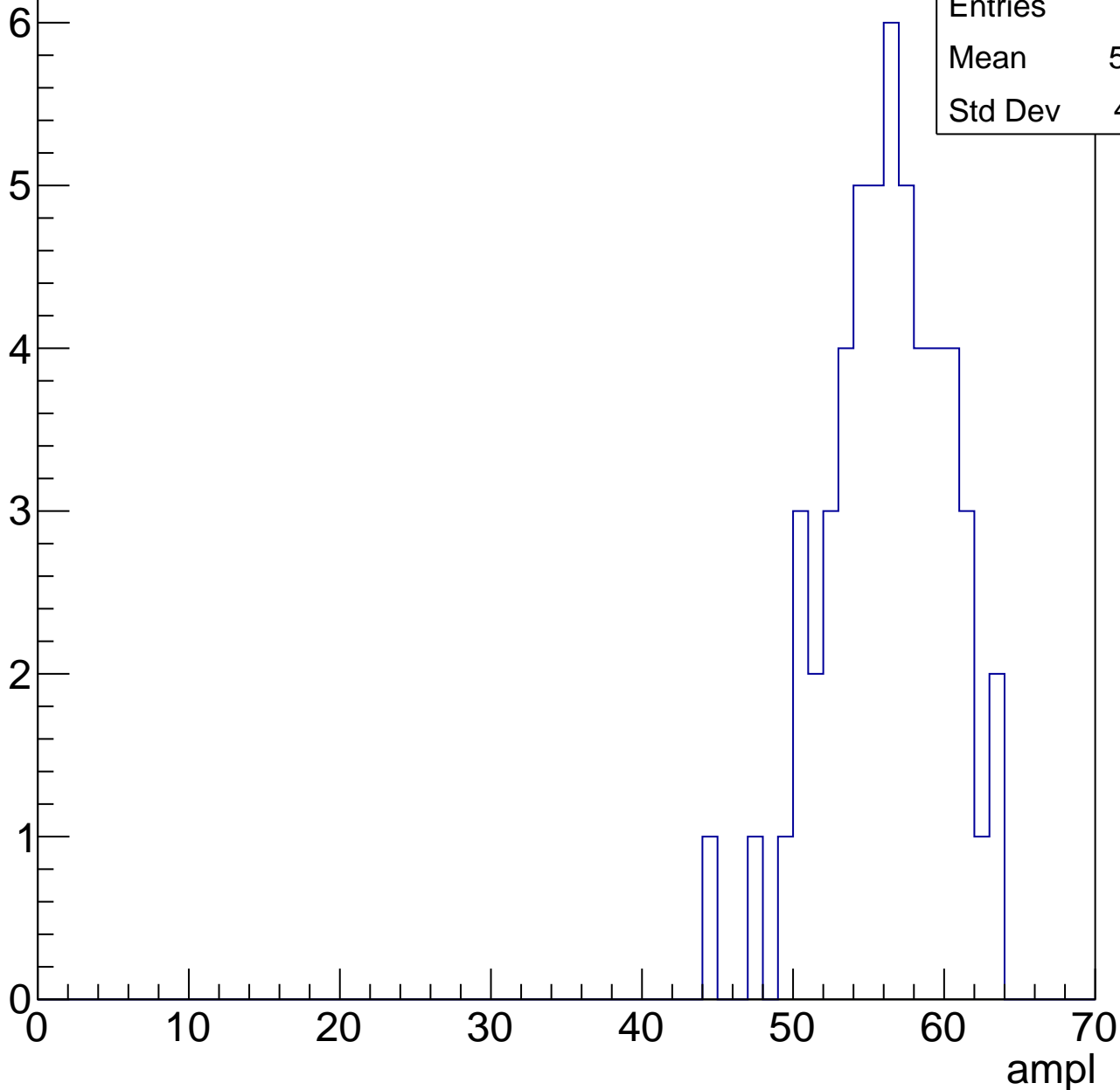


# B1L101S, U19-ch97, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

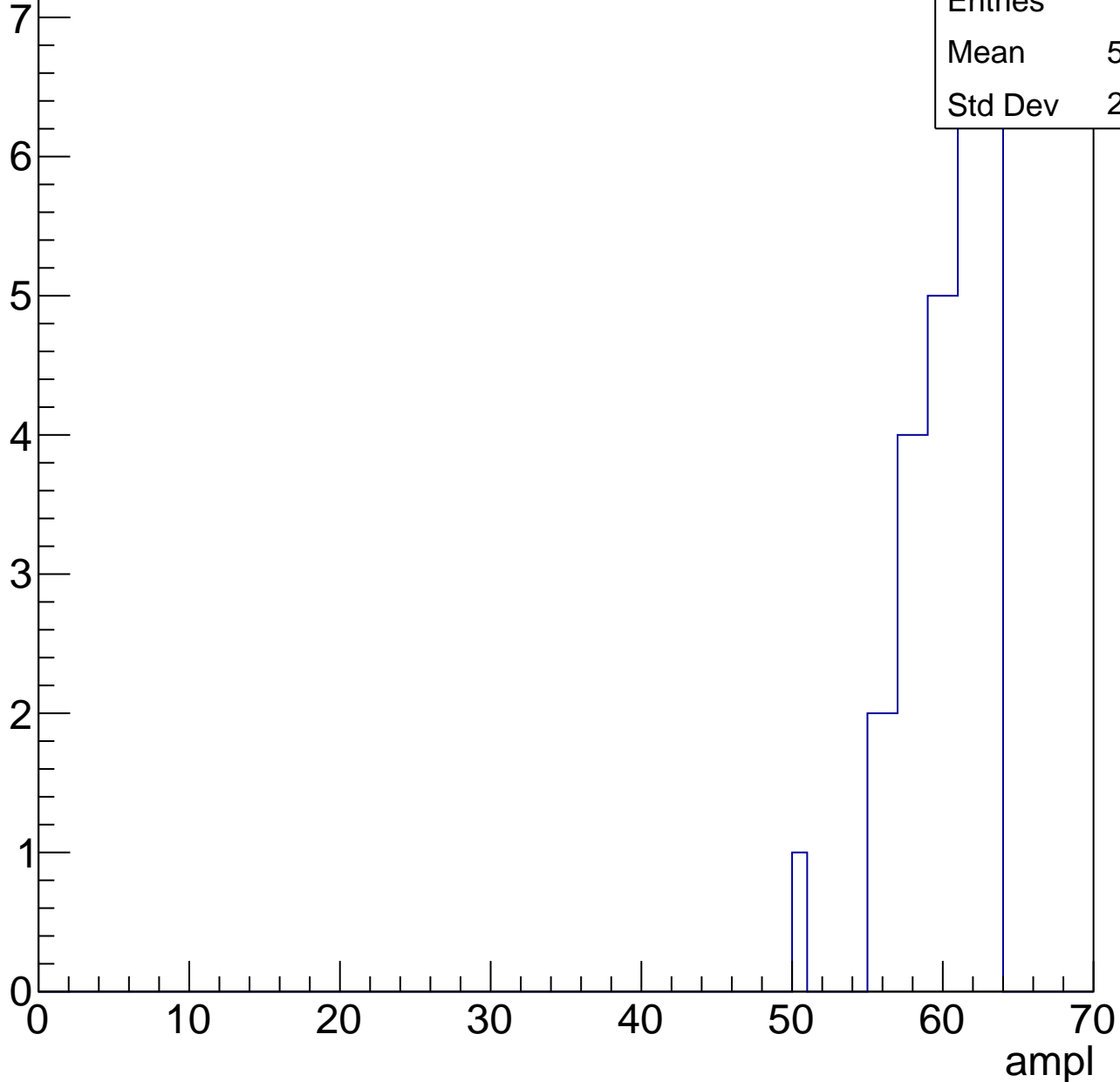
Entries	54
Mean	55.65
Std Dev	4.001



# B1L101S, U19-ch97, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U19-ch97, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

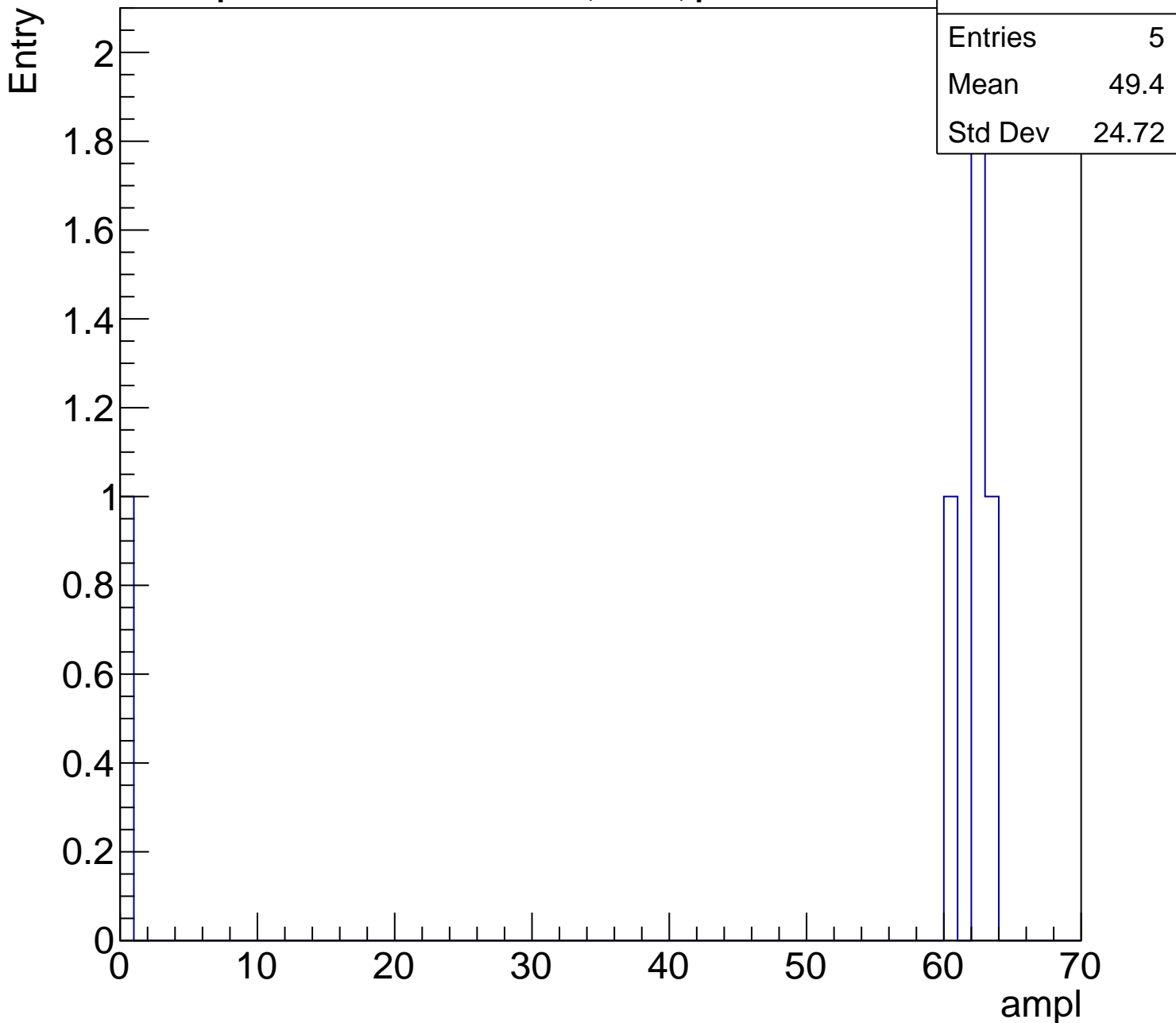
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	5
Mean	49.4
Std Dev	24.72

0 10 20 30 40 50 60 70

ampl





# B1L101S, U19-ch97, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	3
Mean	8
Std Dev	11.31

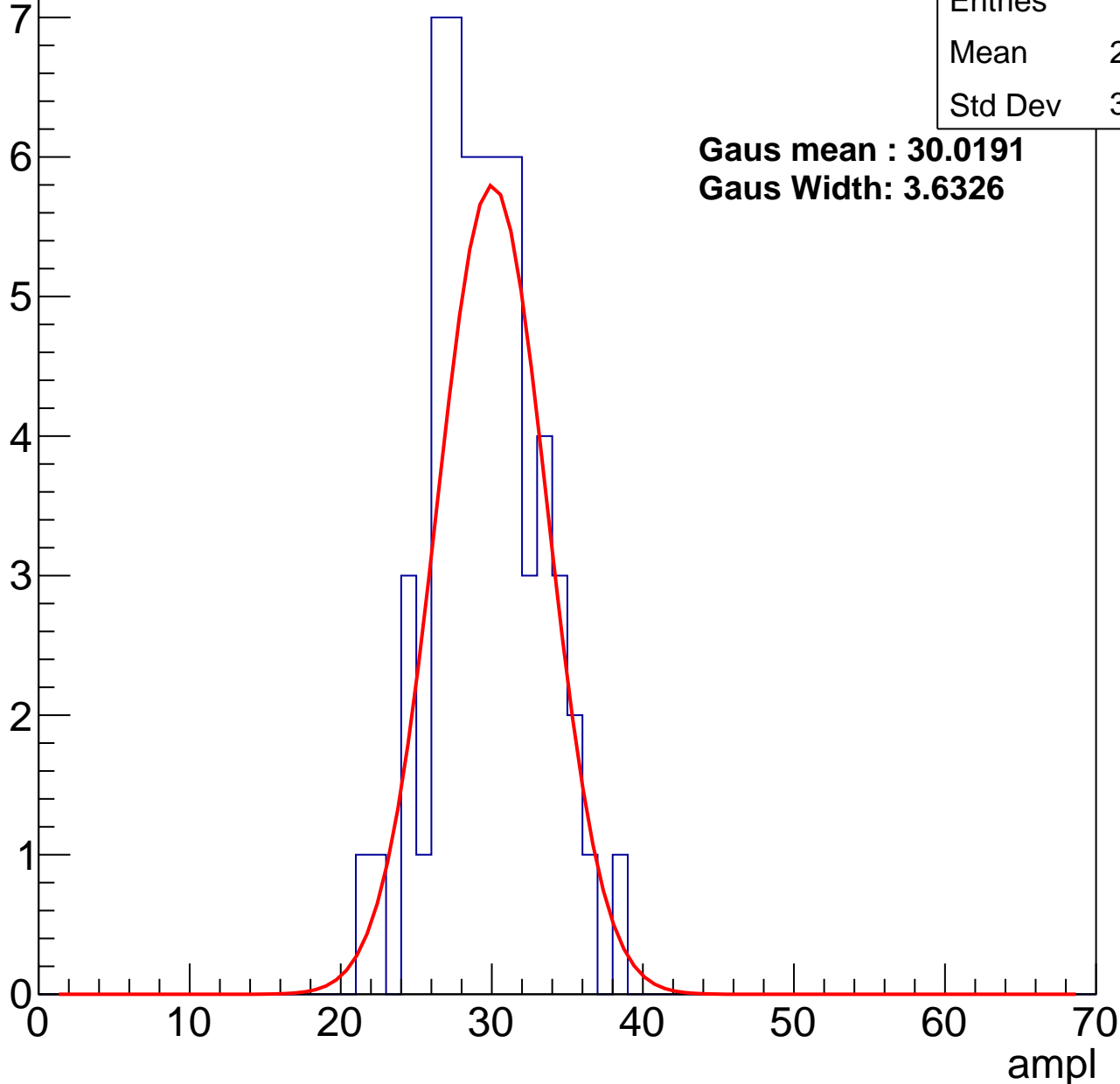
# B1L101S, U19-ch98, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	58
Mean	29.19
Std Dev	3.466

**Gaus mean : 30.0191**  
**Gaus Width: 3.6326**



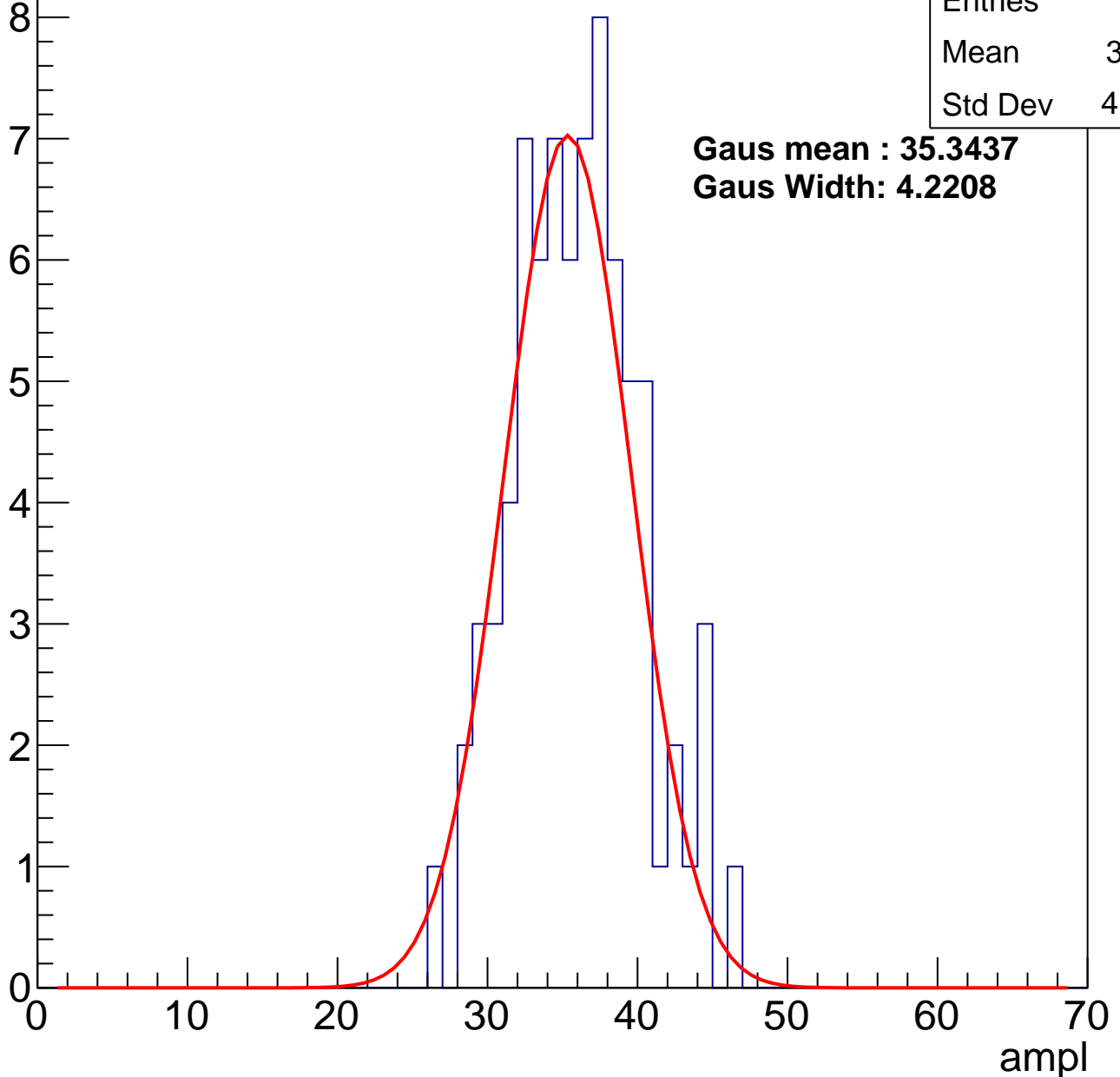
# B1L101S, U19-ch98, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	78
Mean	35.51
Std Dev	4.175

**Gaus mean : 35.3437**  
**Gaus Width: 4.2208**



# B1L101S, U19-ch98, adc2

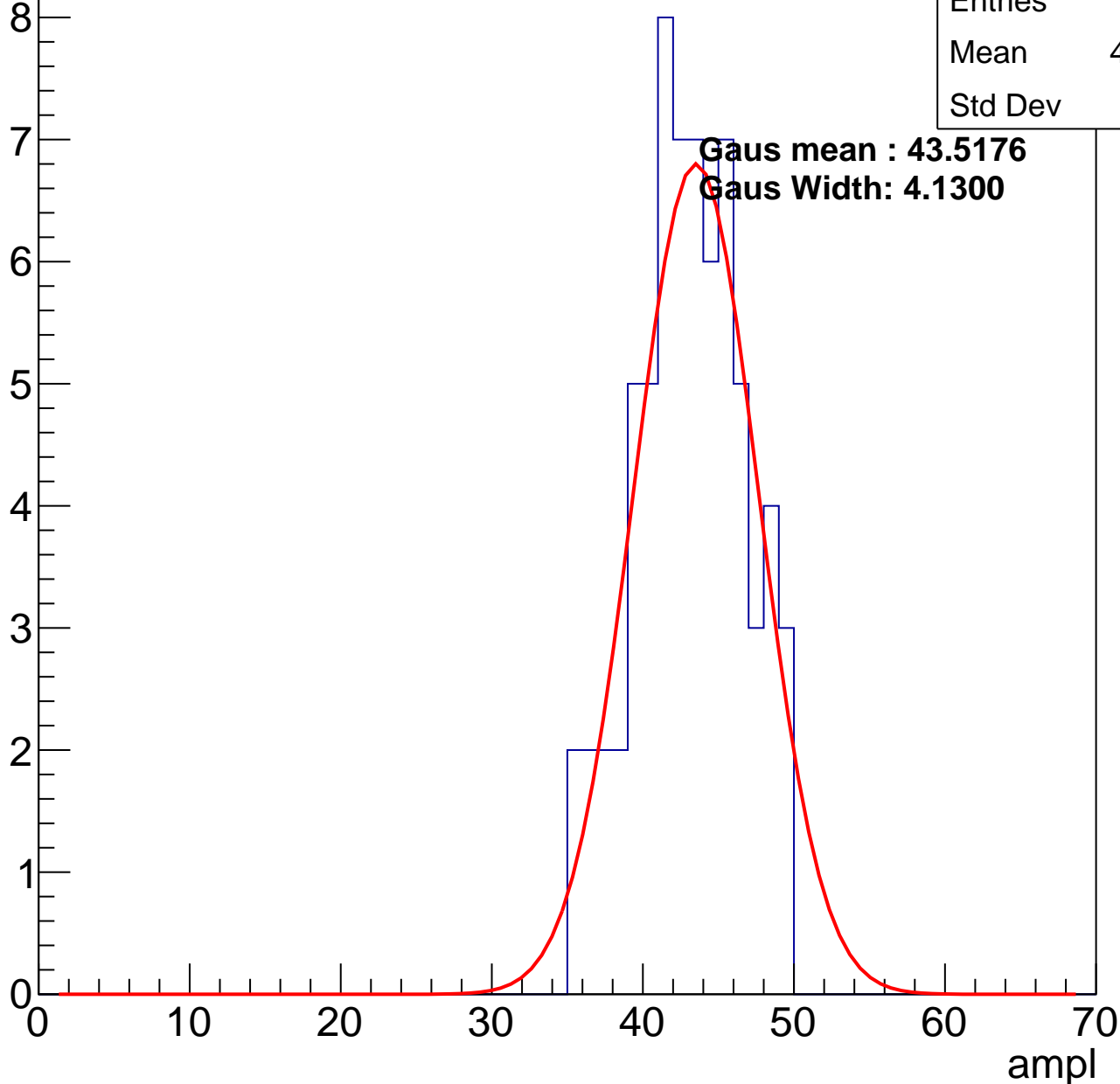
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	42.63
Std Dev	3.51

Gaus mean : 43.5176

Gaus Width: 4.1300

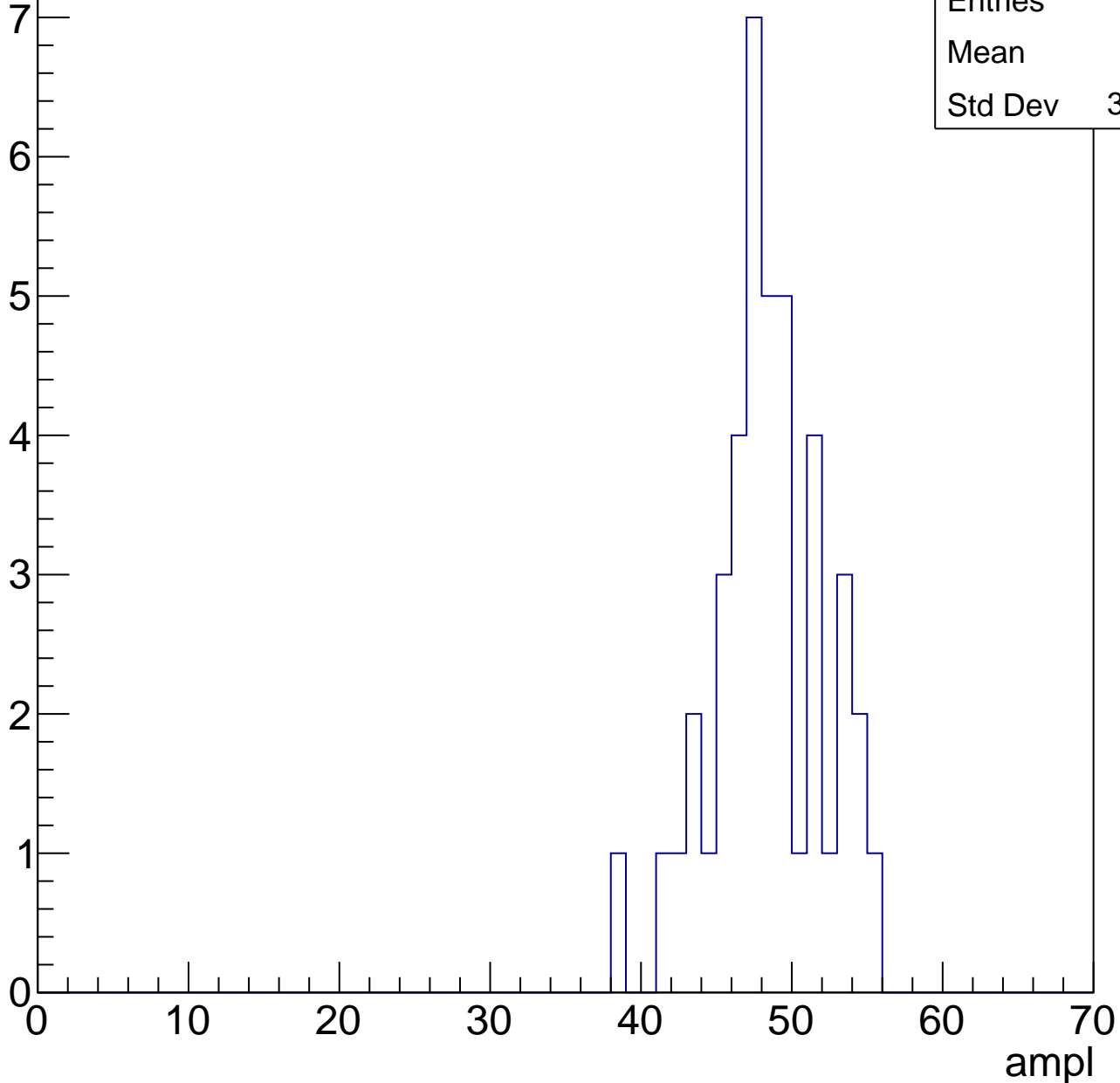


# B1L101S, U19-ch98, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

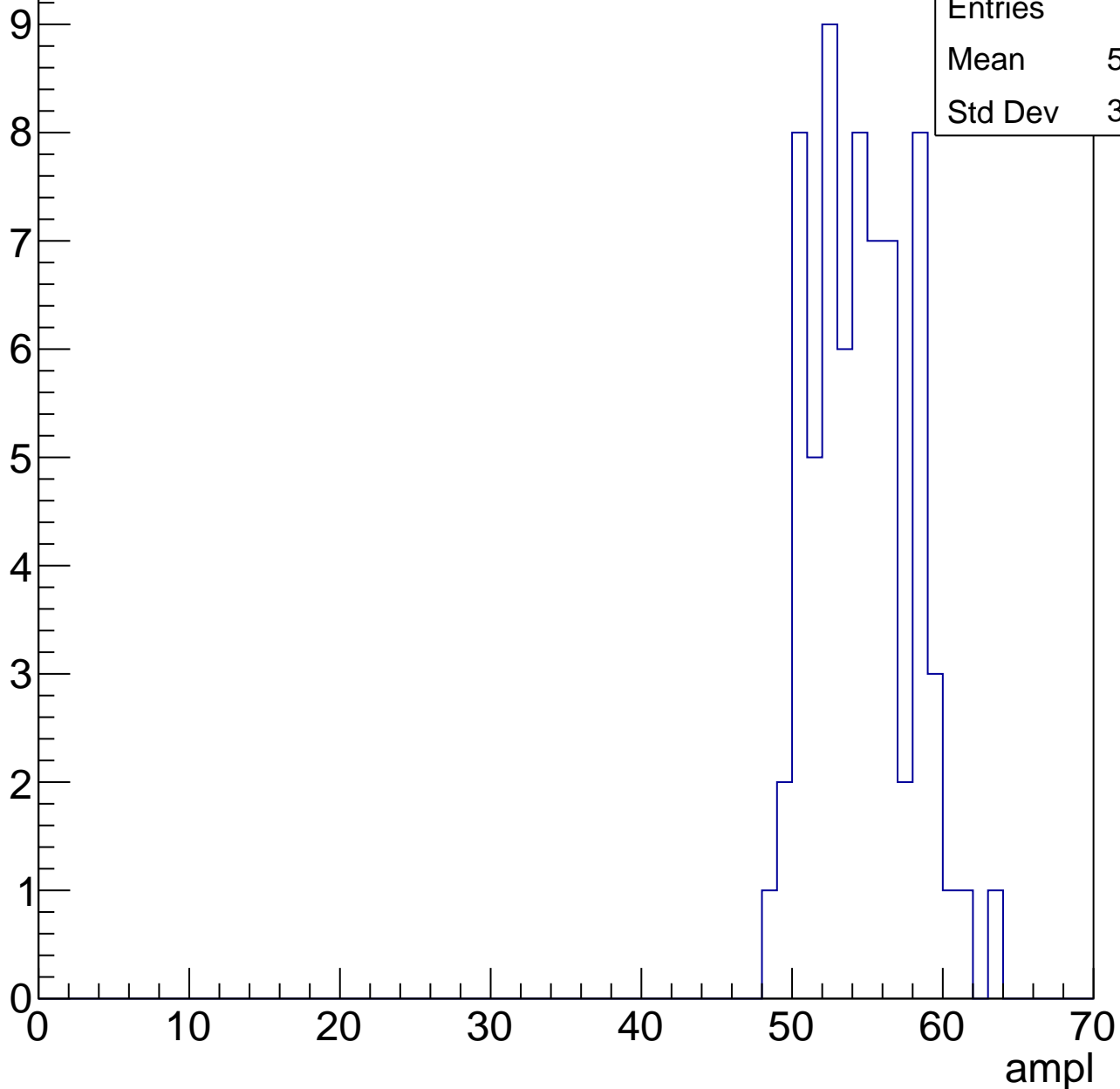
Entries	42
Mean	47.9
Std Dev	3.644



# B1L101S, U19-ch98, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

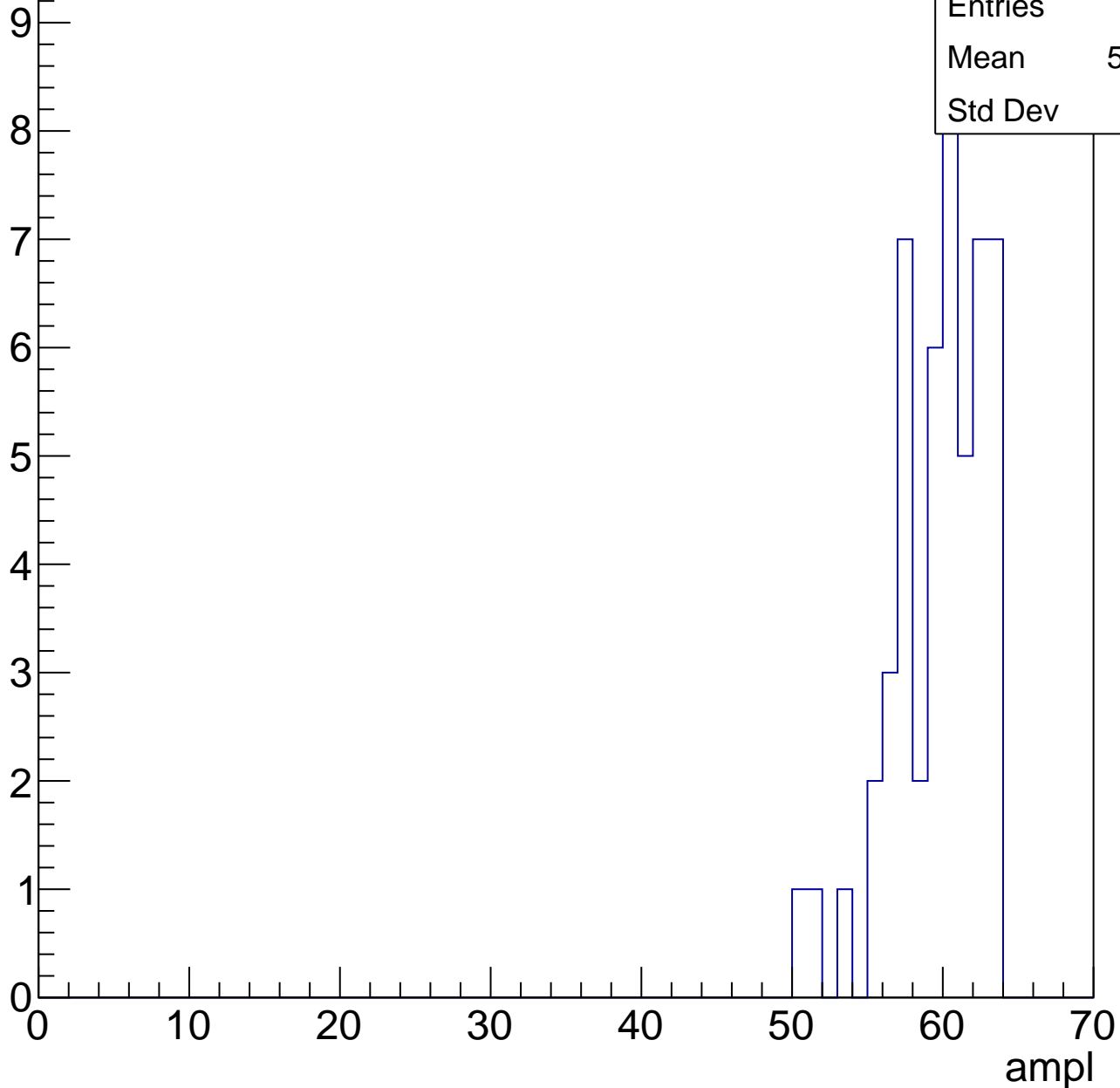
Entry



# B1L101S, U19-ch98, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

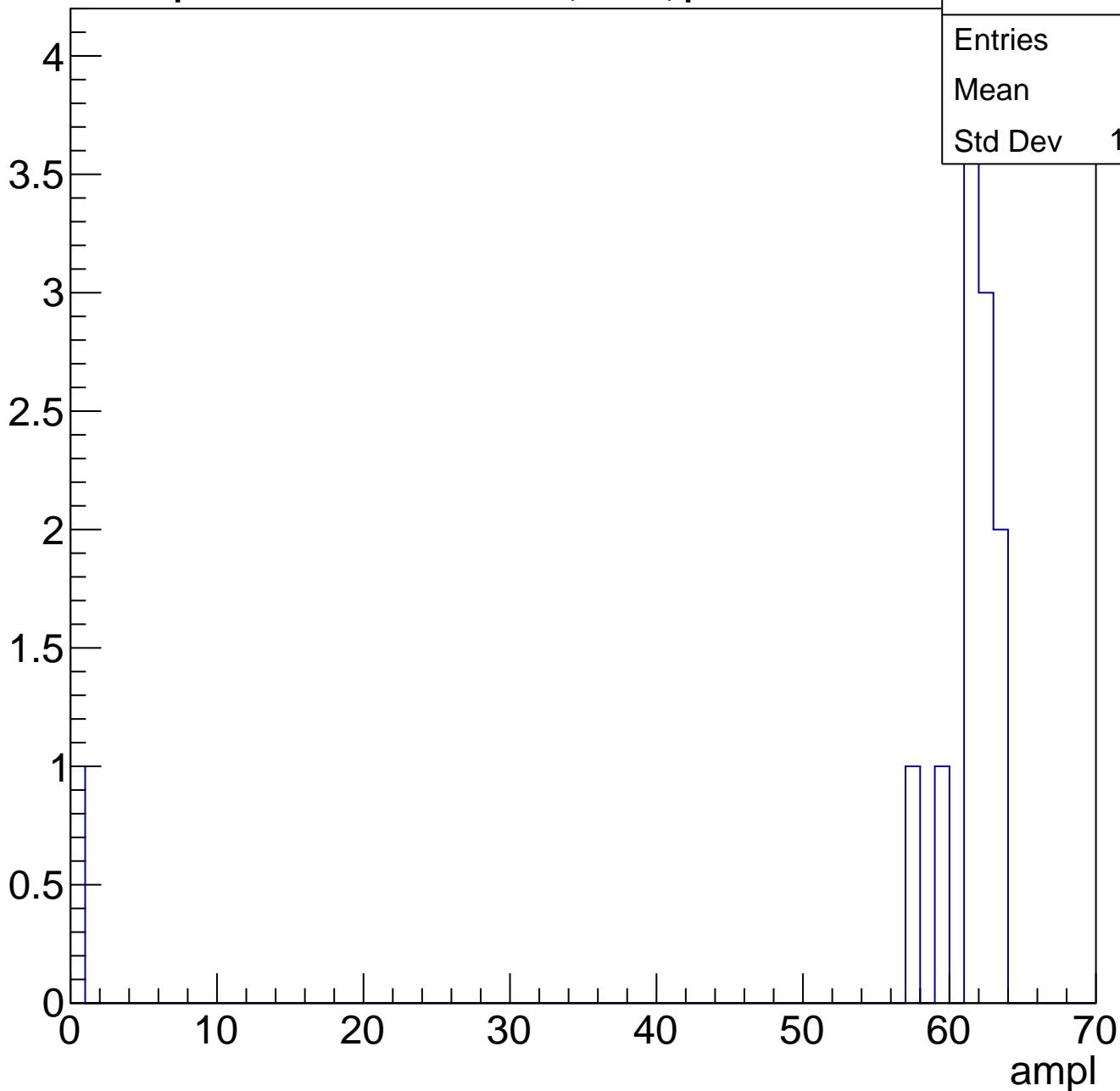
Entry



# B1L101S, U19-ch98, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U19-ch98, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	3
Mean	0
Std Dev	0

# B1L101S, U19-ch99, adc0

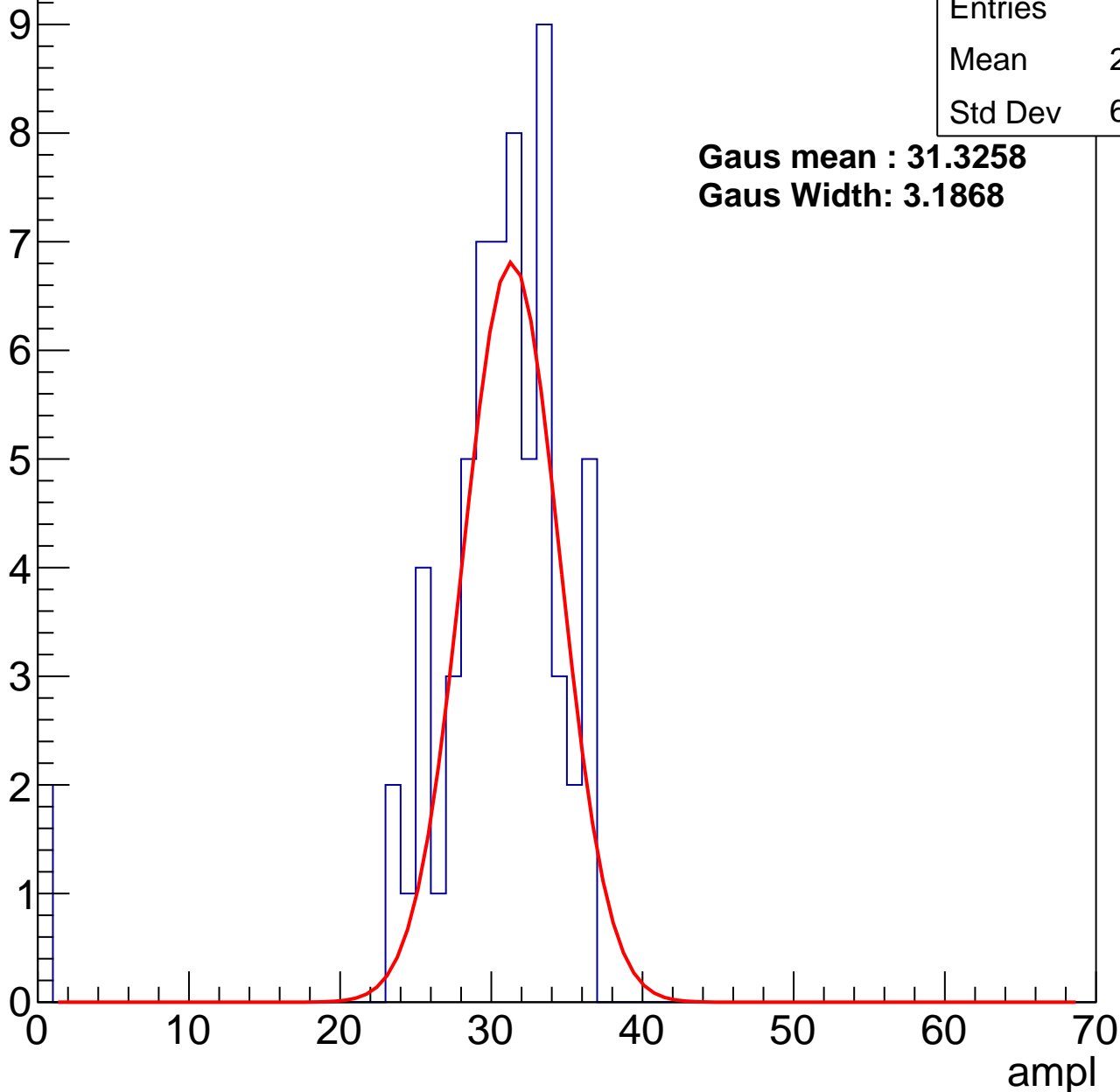
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	29.48
Std Dev	6.217

**Gaus mean : 31.3258**

**Gaus Width: 3.1868**



# B1L101S, U19-ch99, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	63
Mean	37.1
Std Dev	3.105

**Gaus mean : 37.9505**

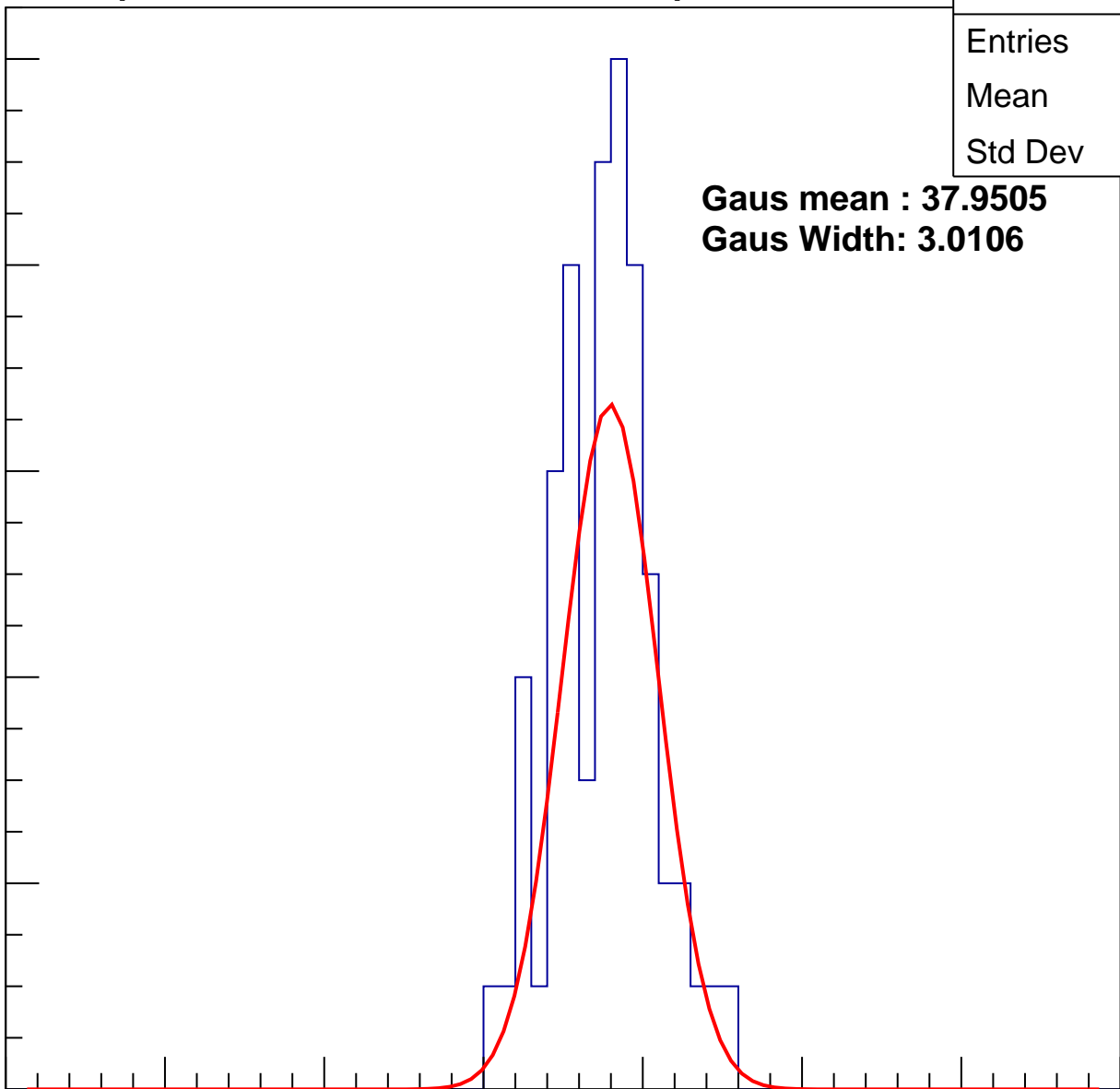
**Gaus Width: 3.0106**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U19-ch99, adc2

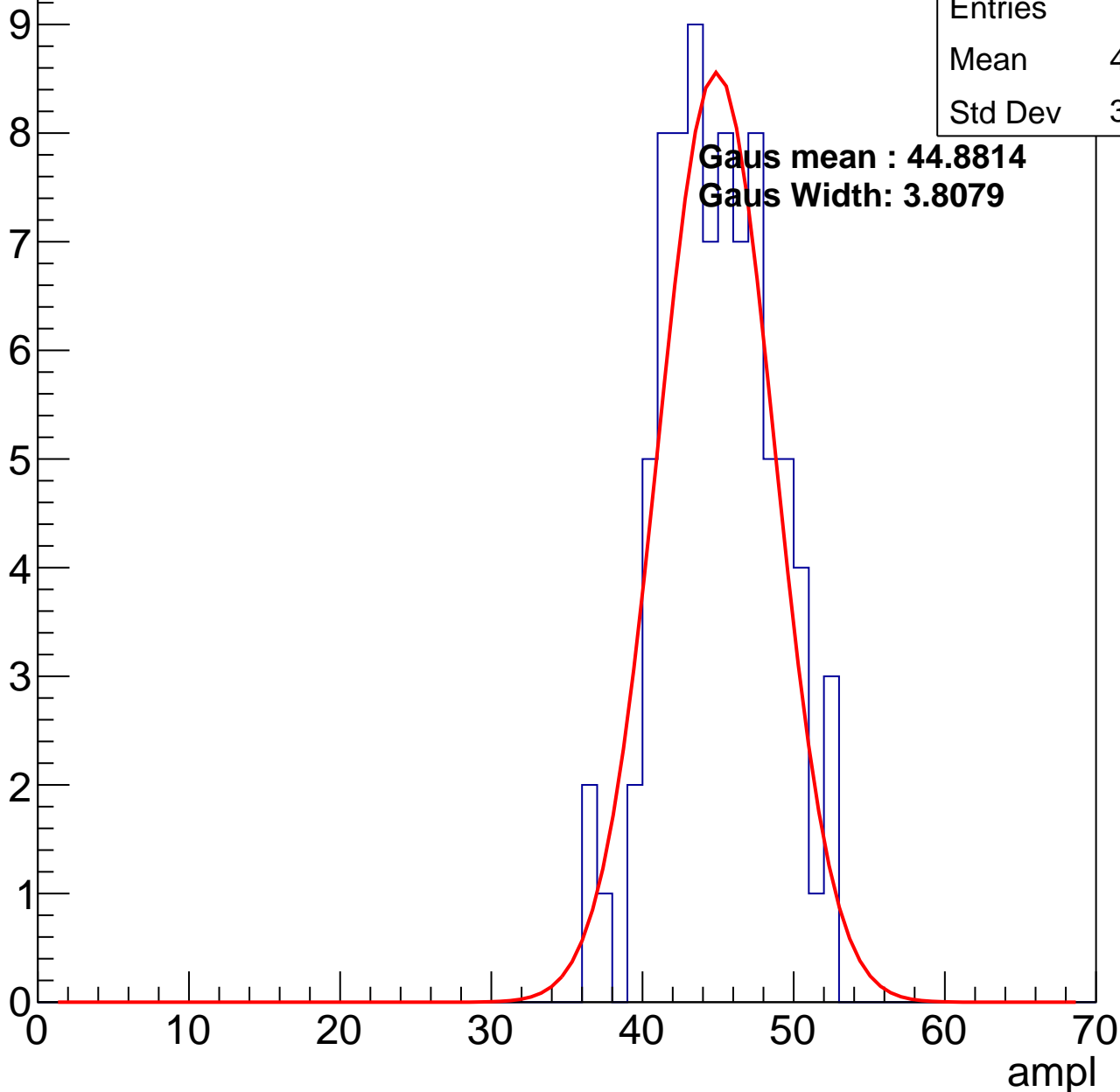
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	83
Mean	44.53
Std Dev	3.632

**Gaus mean : 44.8814**

**Gaus Width: 3.8079**

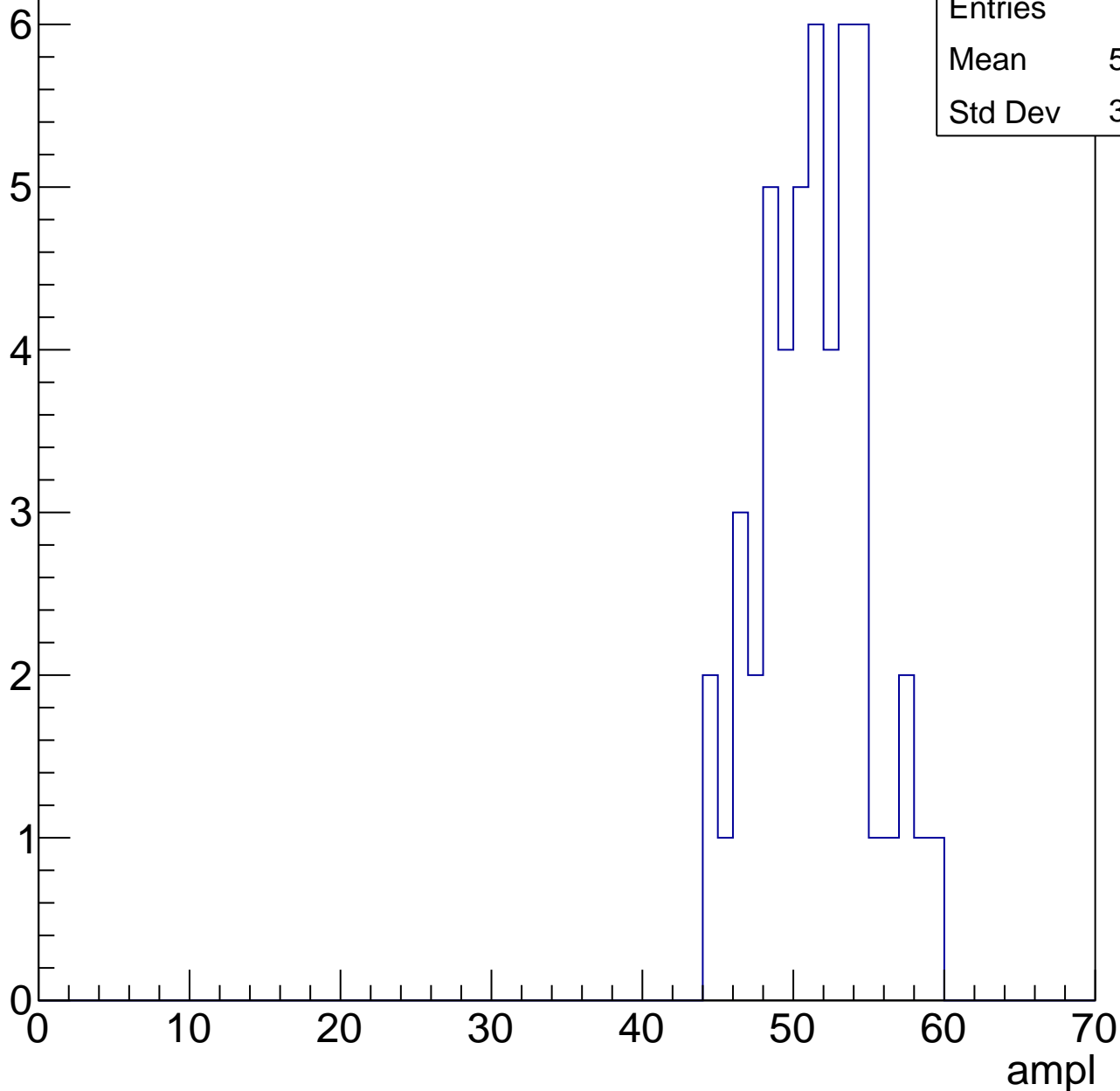


# B1L101S, U19-ch99, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

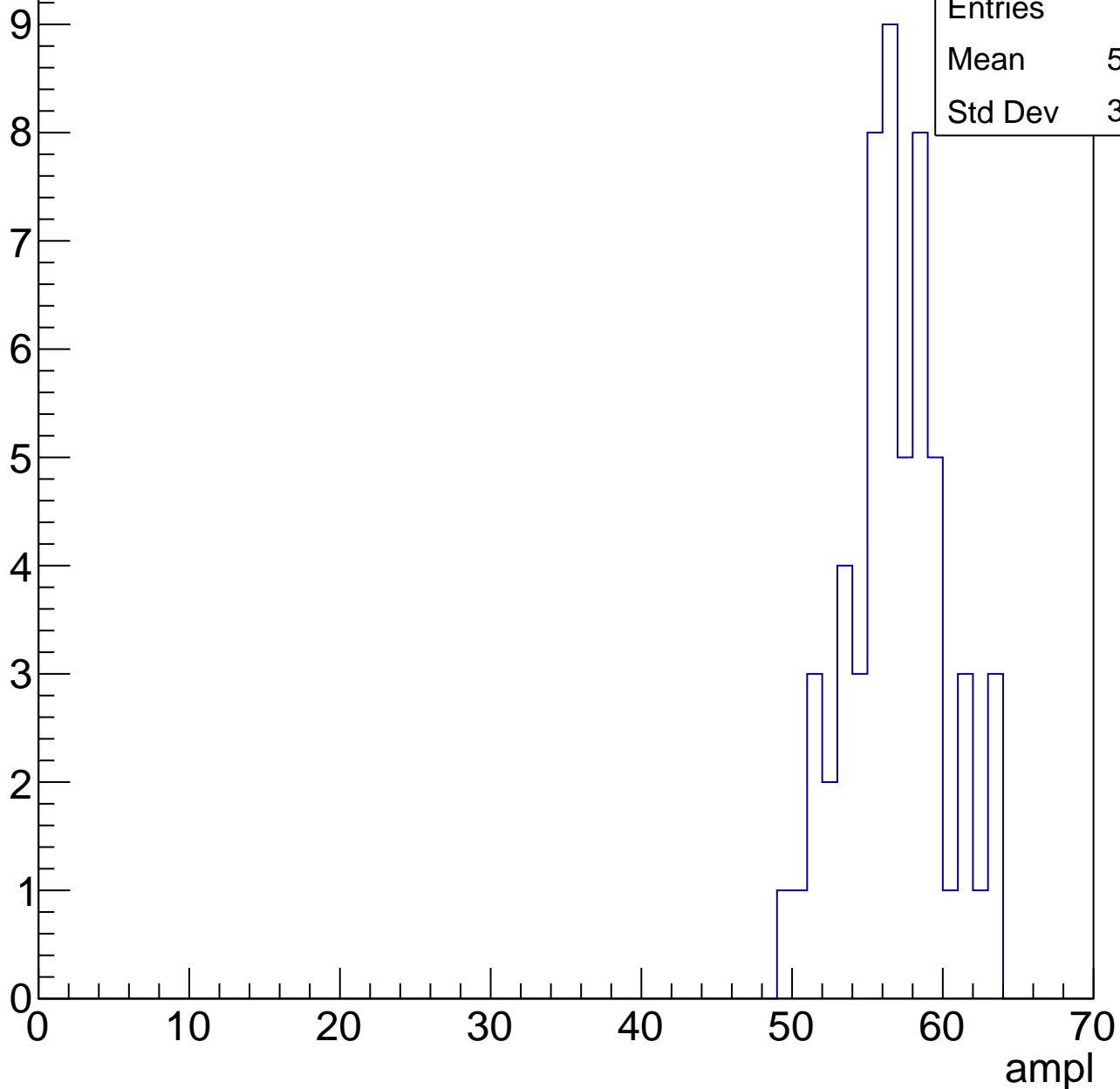
Entries	50
Mean	50.98
Std Dev	3.507



# B1L101S, U19-ch99, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

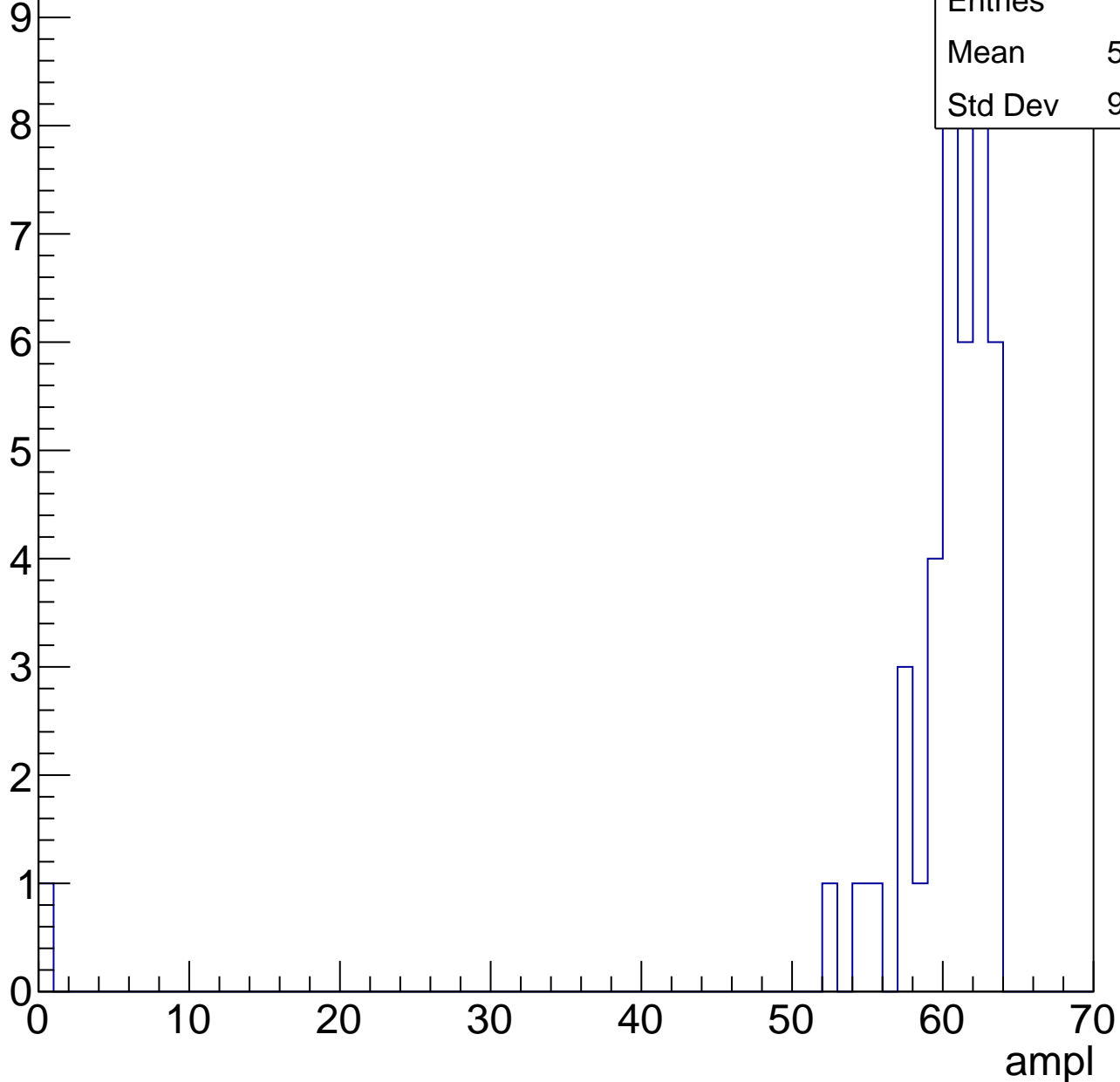


Entries	57
Mean	56.35
Std Dev	3.236

# B1L101S, U19-ch99, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U19-ch99, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U19-ch99, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U19-ch100, adc0

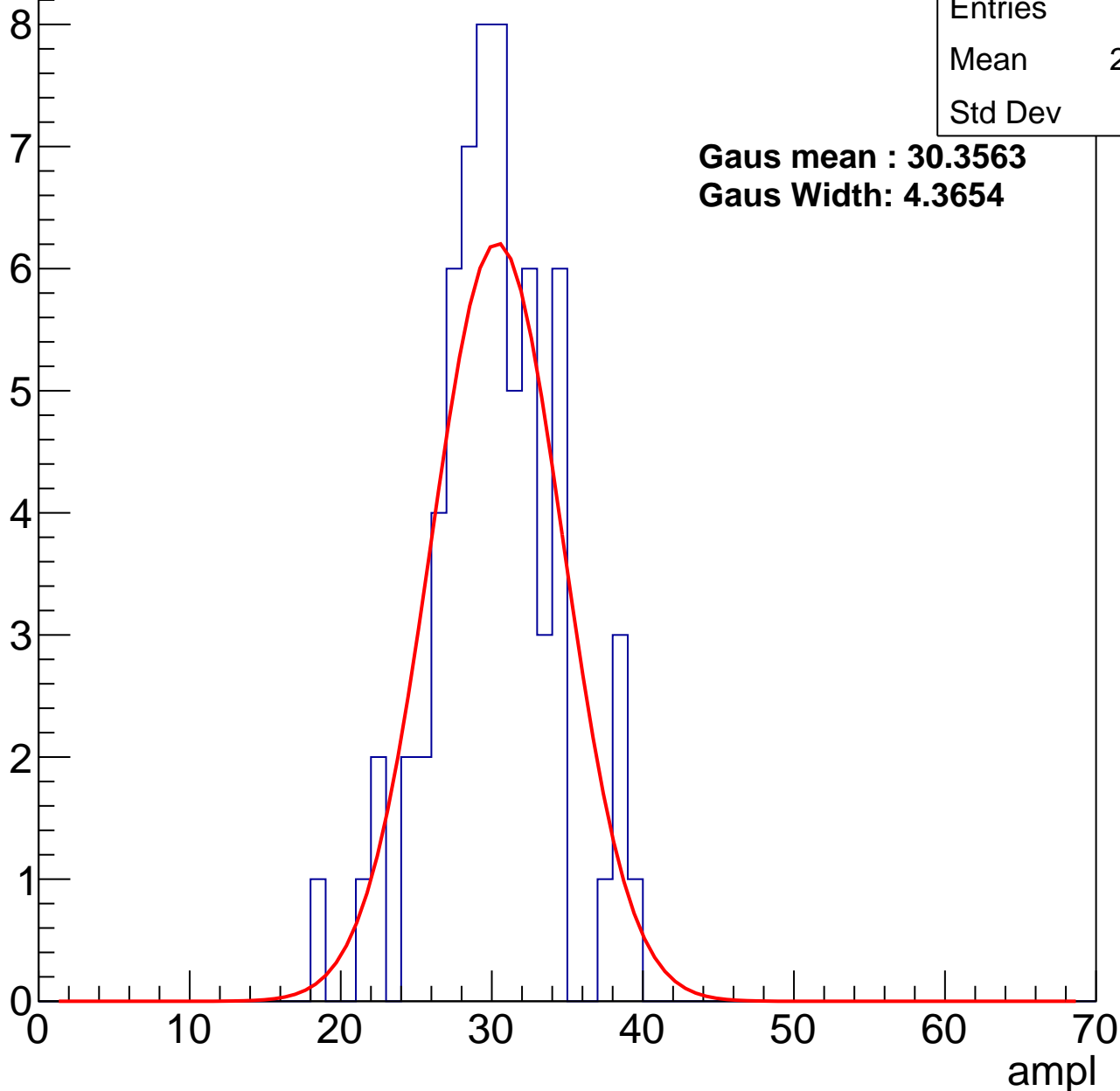
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	66
Mean	29.62
Std Dev	4.07

**Gaus mean : 30.3563**

**Gaus Width: 4.3654**



# B1L101S, U19-ch100, adc1

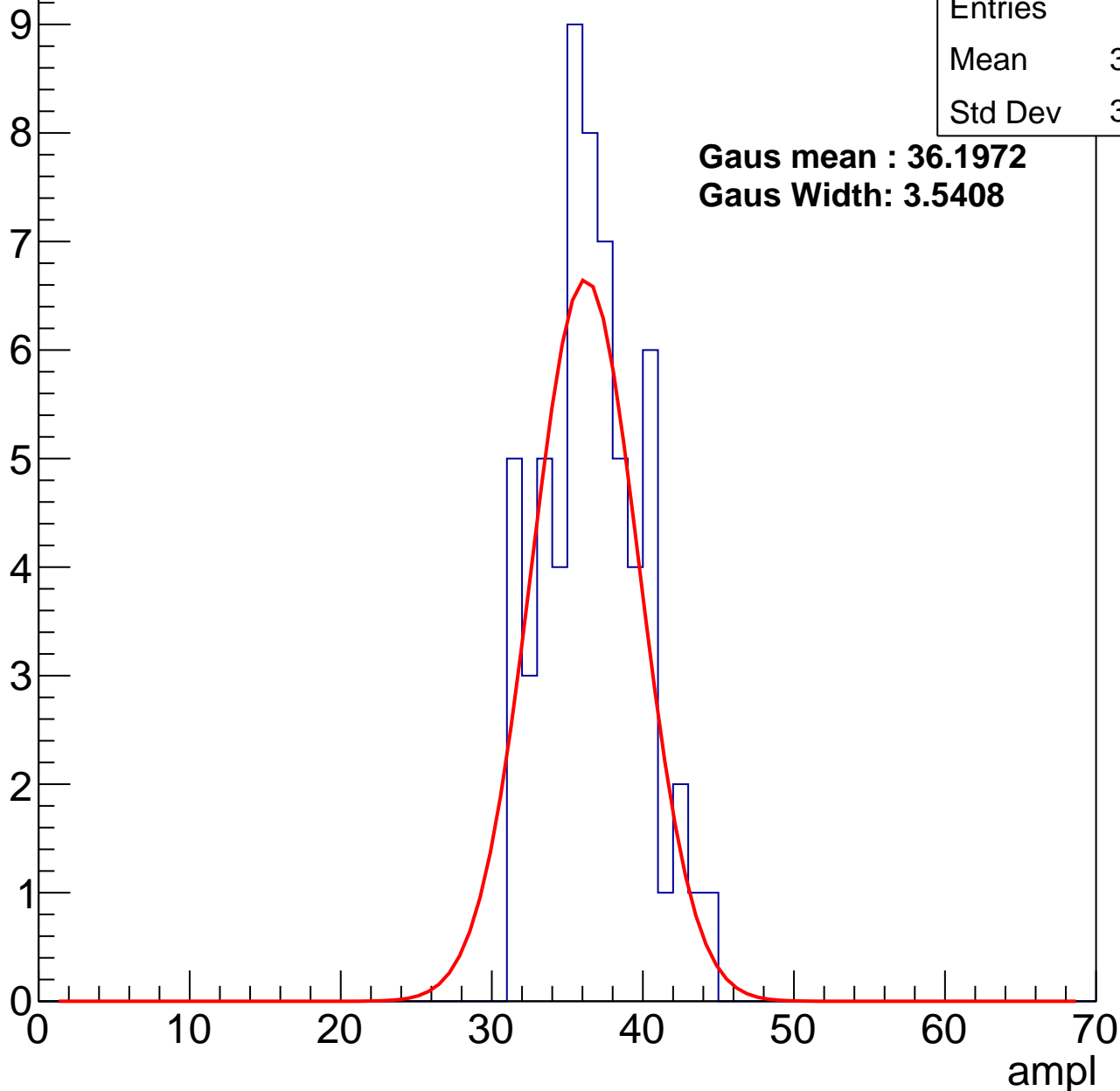
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	36.26
Std Dev	3.157

**Gaus mean : 36.1972**

**Gaus Width: 3.5408**



# B1L101S, U19-ch100, adc2

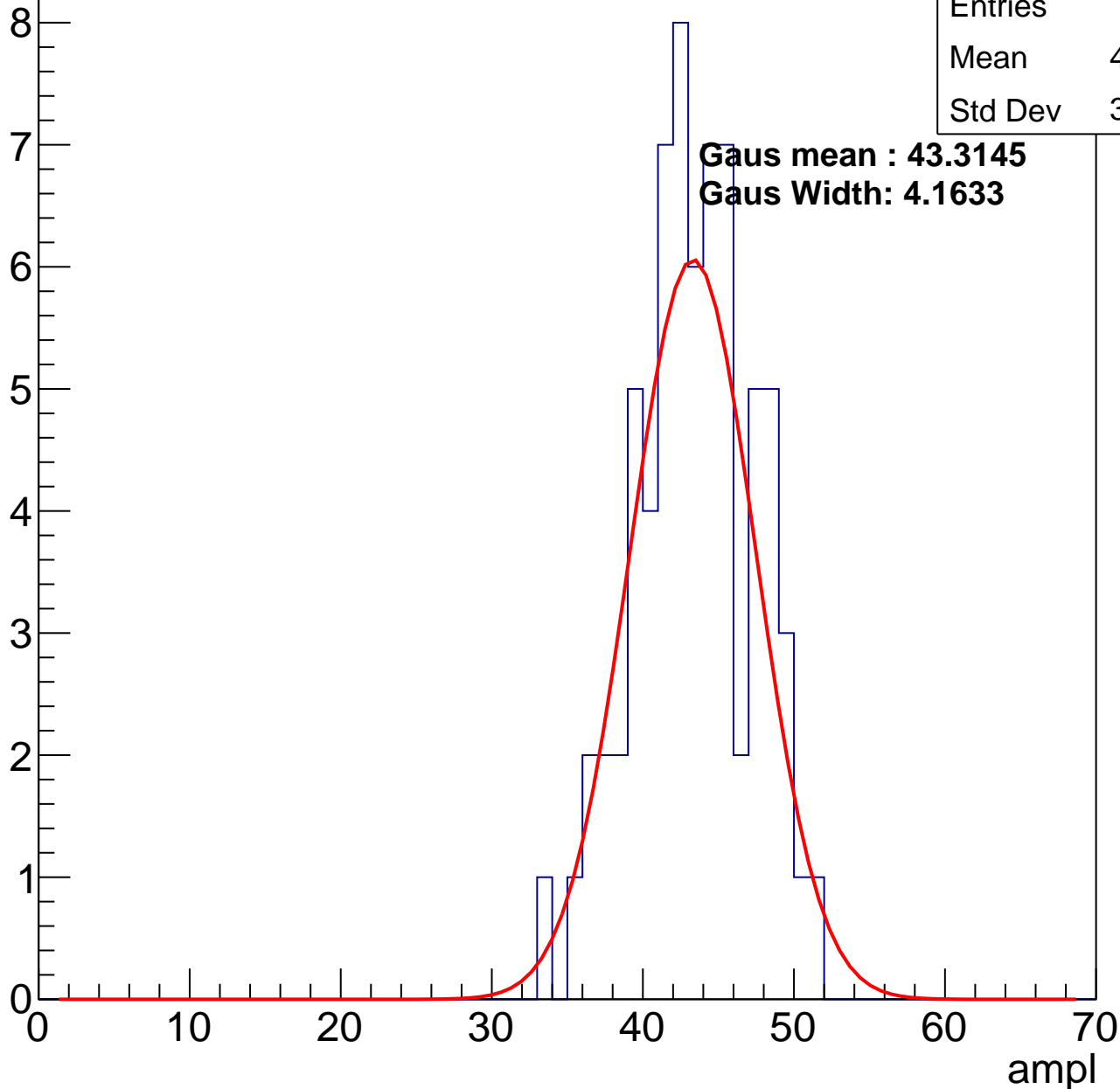
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	42.96
Std Dev	3.835

**Gaus mean : 43.3145**

**Gaus Width: 4.1633**

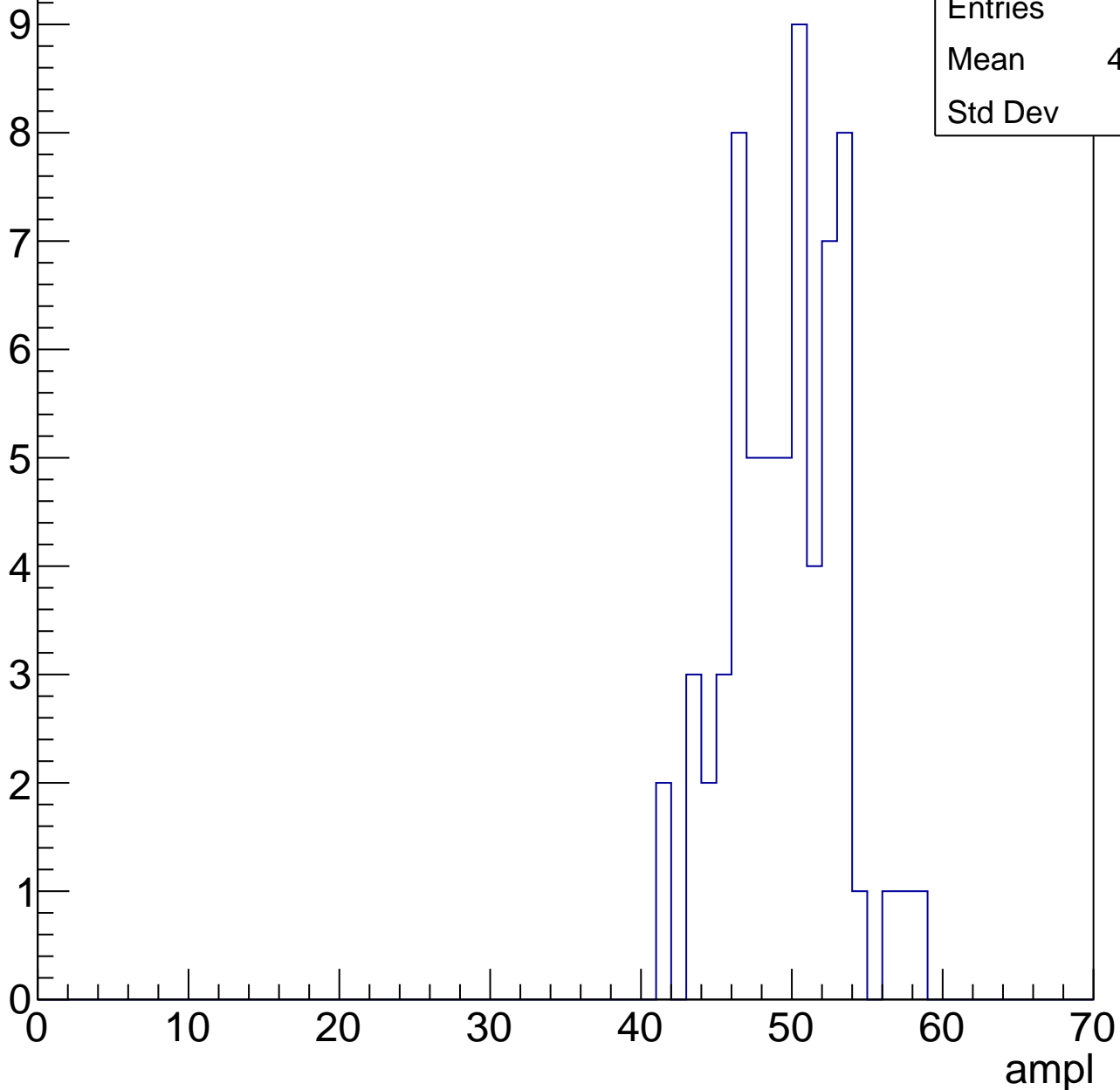


# B1L101S, U19-ch100, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

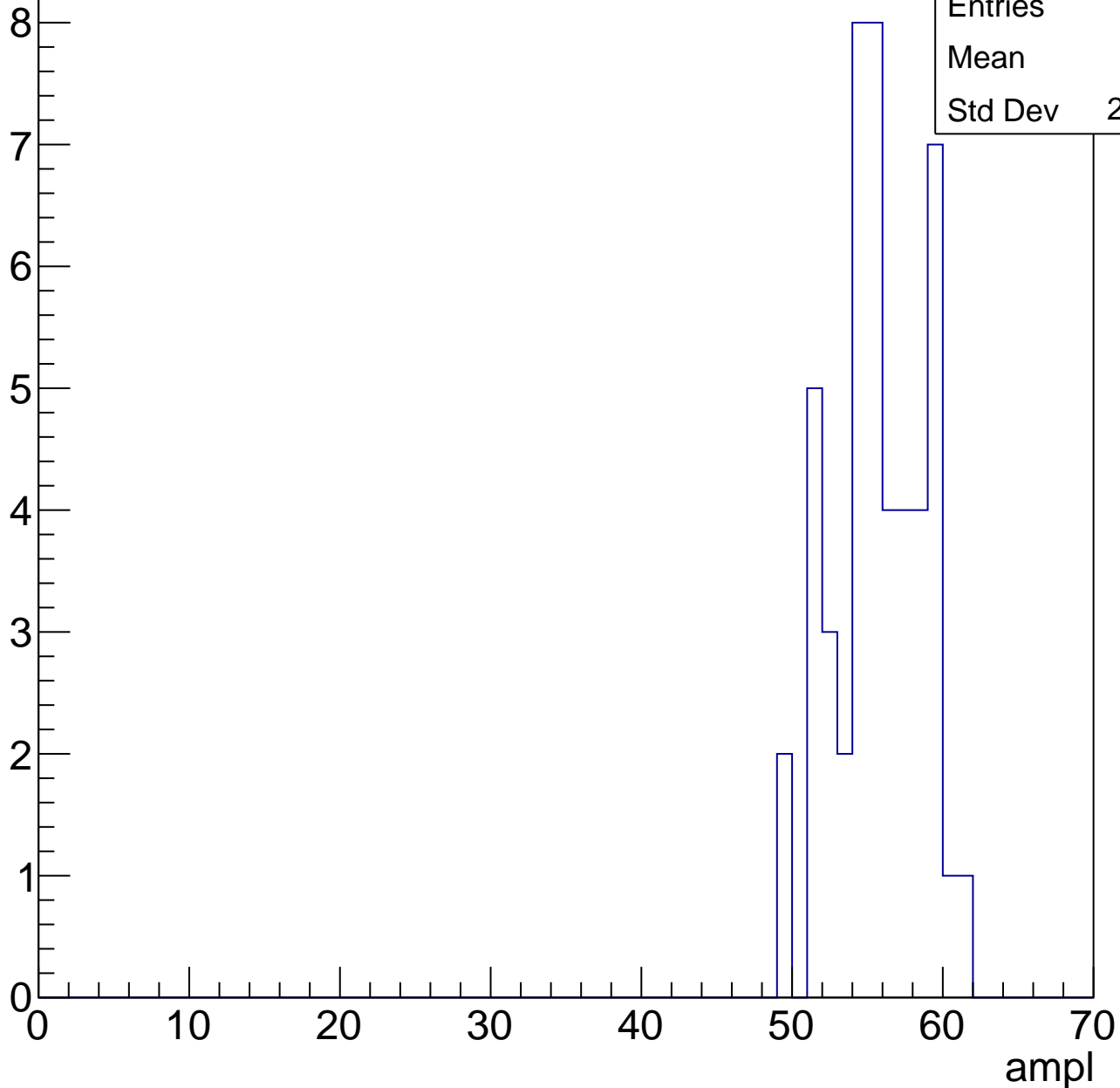
Entries	65
Mean	49.06
Std Dev	3.65



# B1L101S, U19-ch100, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



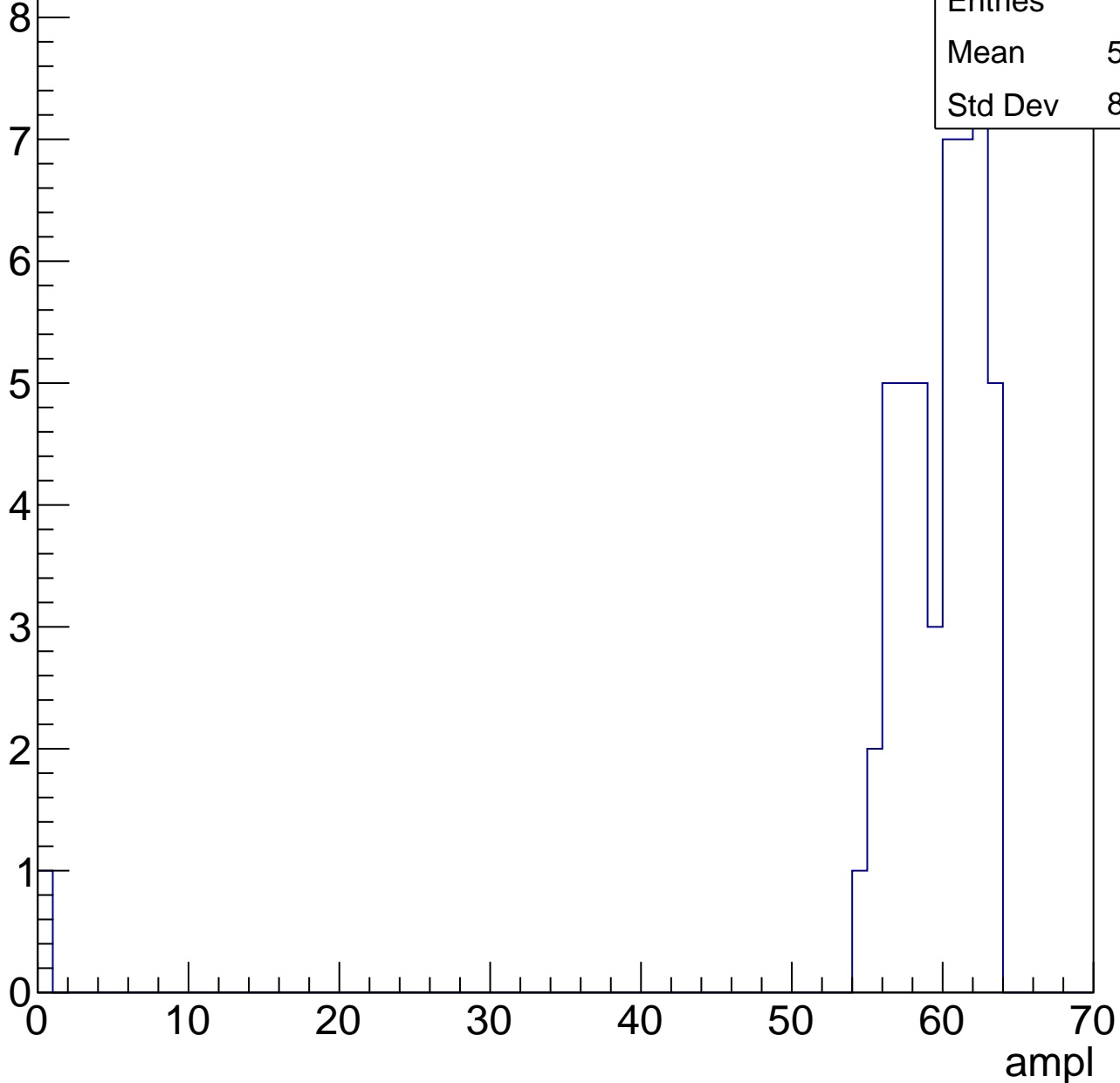
Entries	49
Mean	55.2
Std Dev	2.935

# B1L101S, U19-ch100, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	49
Mean	58.24
Std Dev	8.768

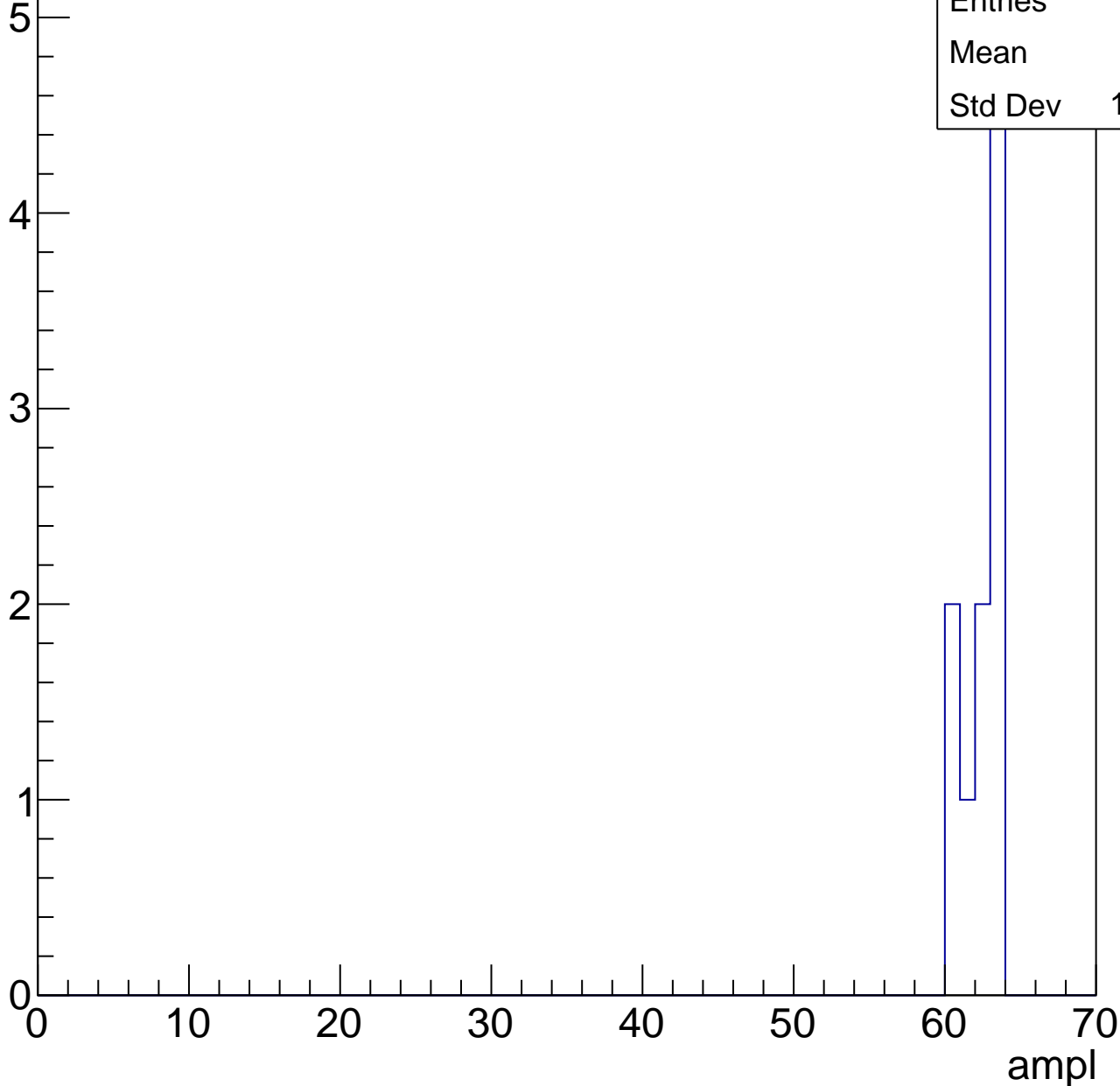


# B1L101S, U19-ch100, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	10
Mean	62
Std Dev	1.183





# B1L101S, U19-ch100, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U19-ch101, adc0

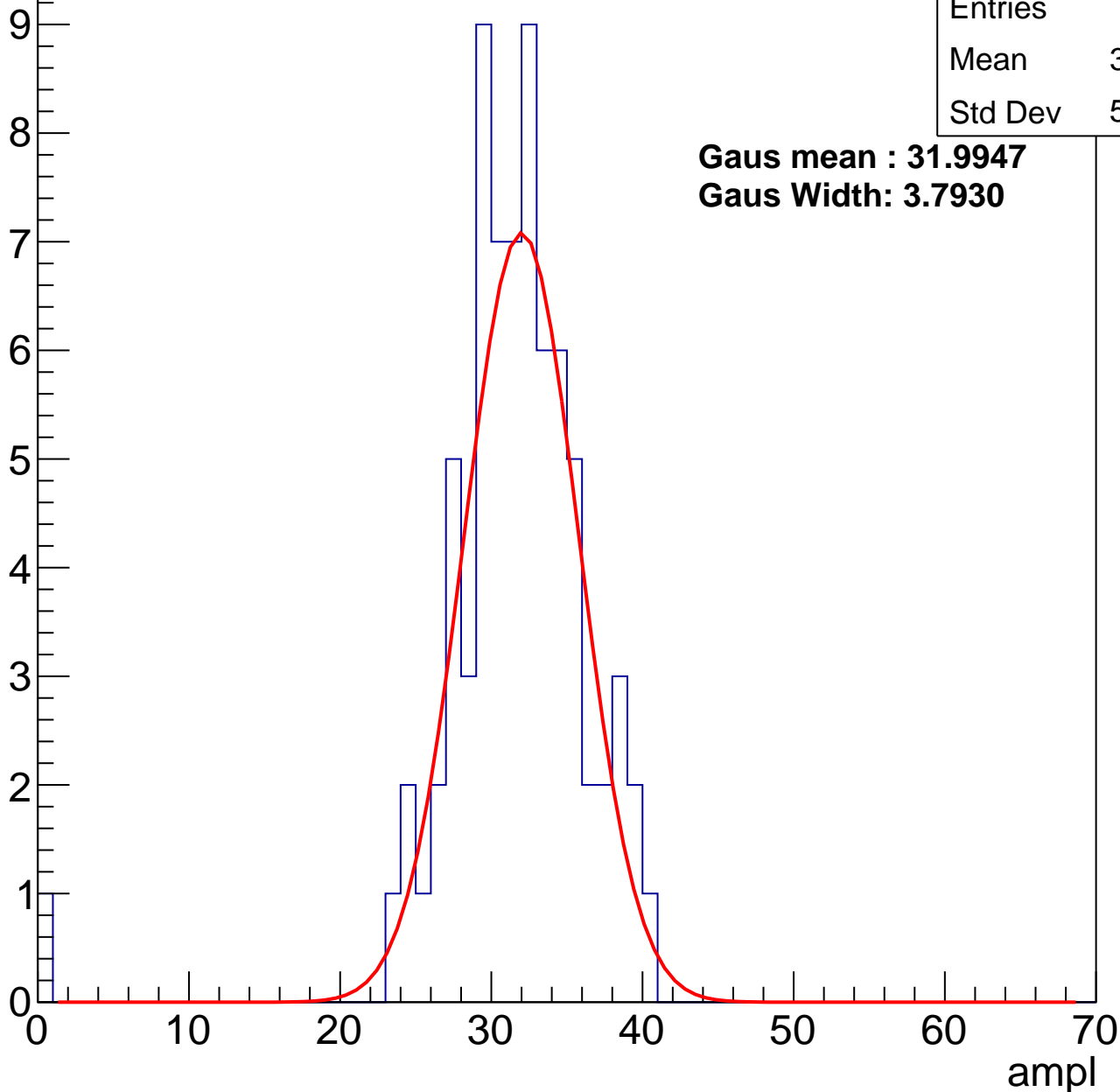
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	74
Mean	31.05
Std Dev	5.204

**Gaus mean : 31.9947**

**Gaus Width: 3.7930**



# B1L101S, U19-ch101, adc1

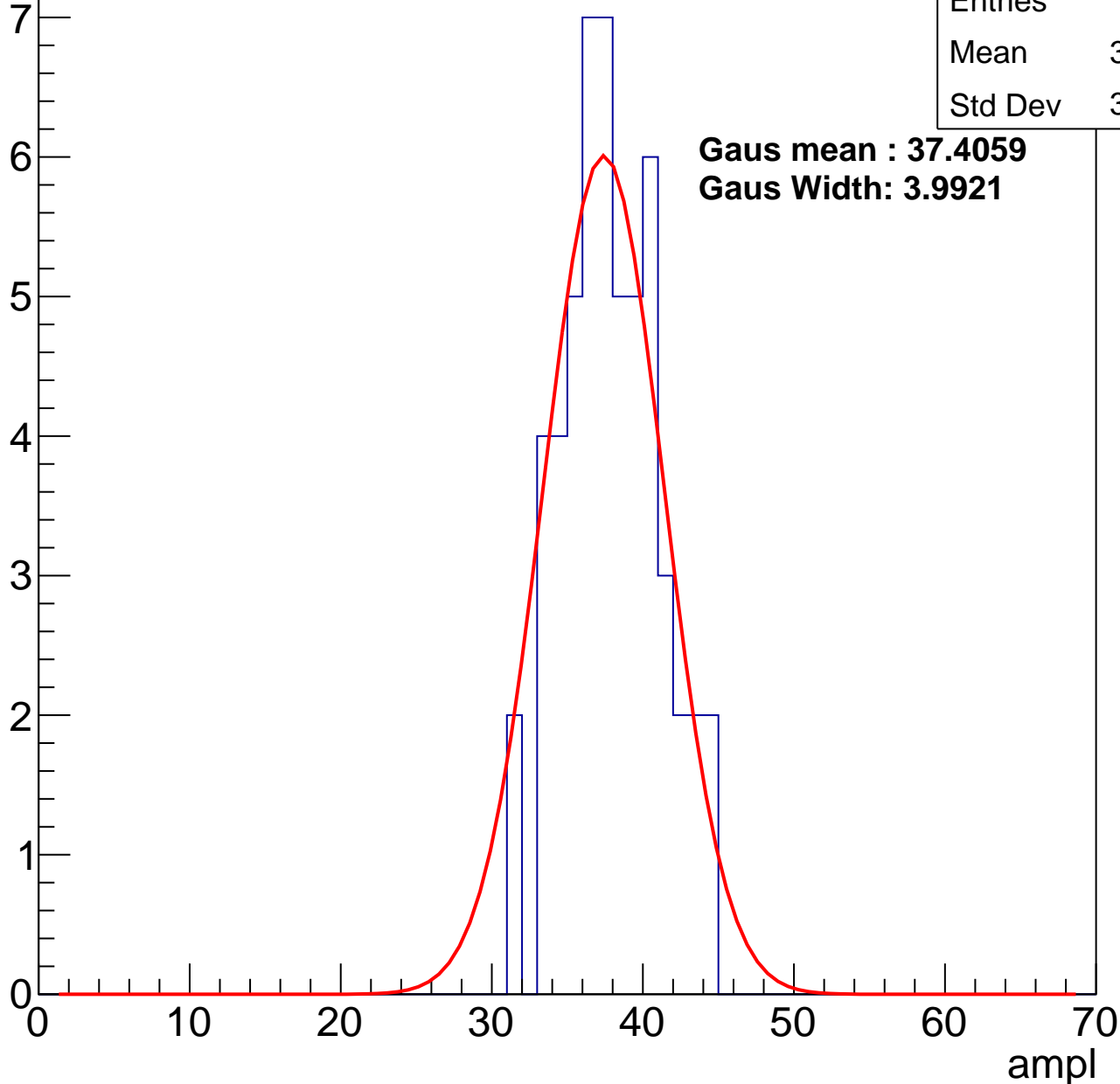
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	54
Mean	37.44
Std Dev	3.149

**Gaus mean : 37.4059**

**Gaus Width: 3.9921**



# B1L101S, U19-ch101, adc2

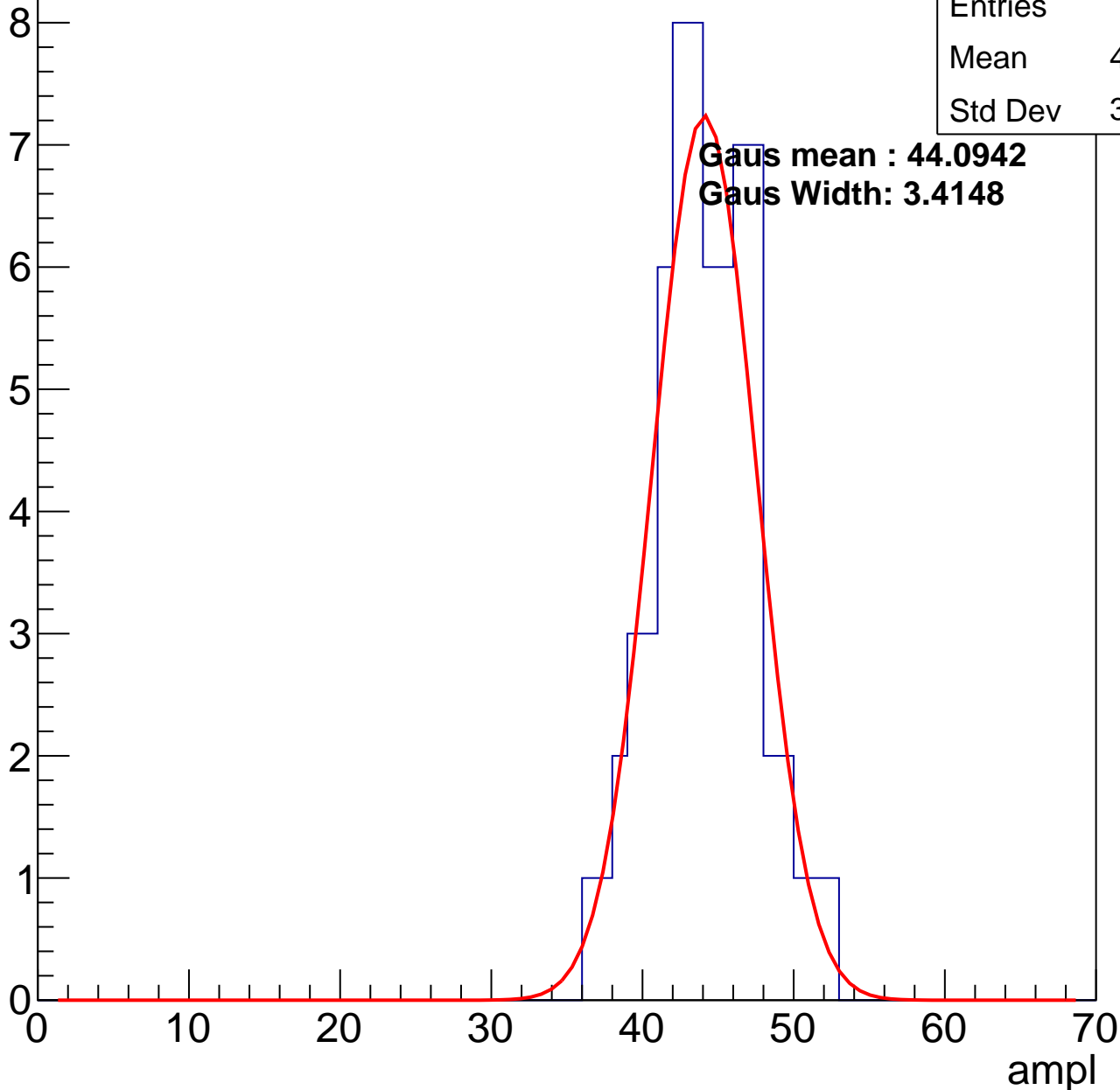
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	43.75
Std Dev	3.342

**Gaus mean : 44.0942**

**Gaus Width: 3.4148**

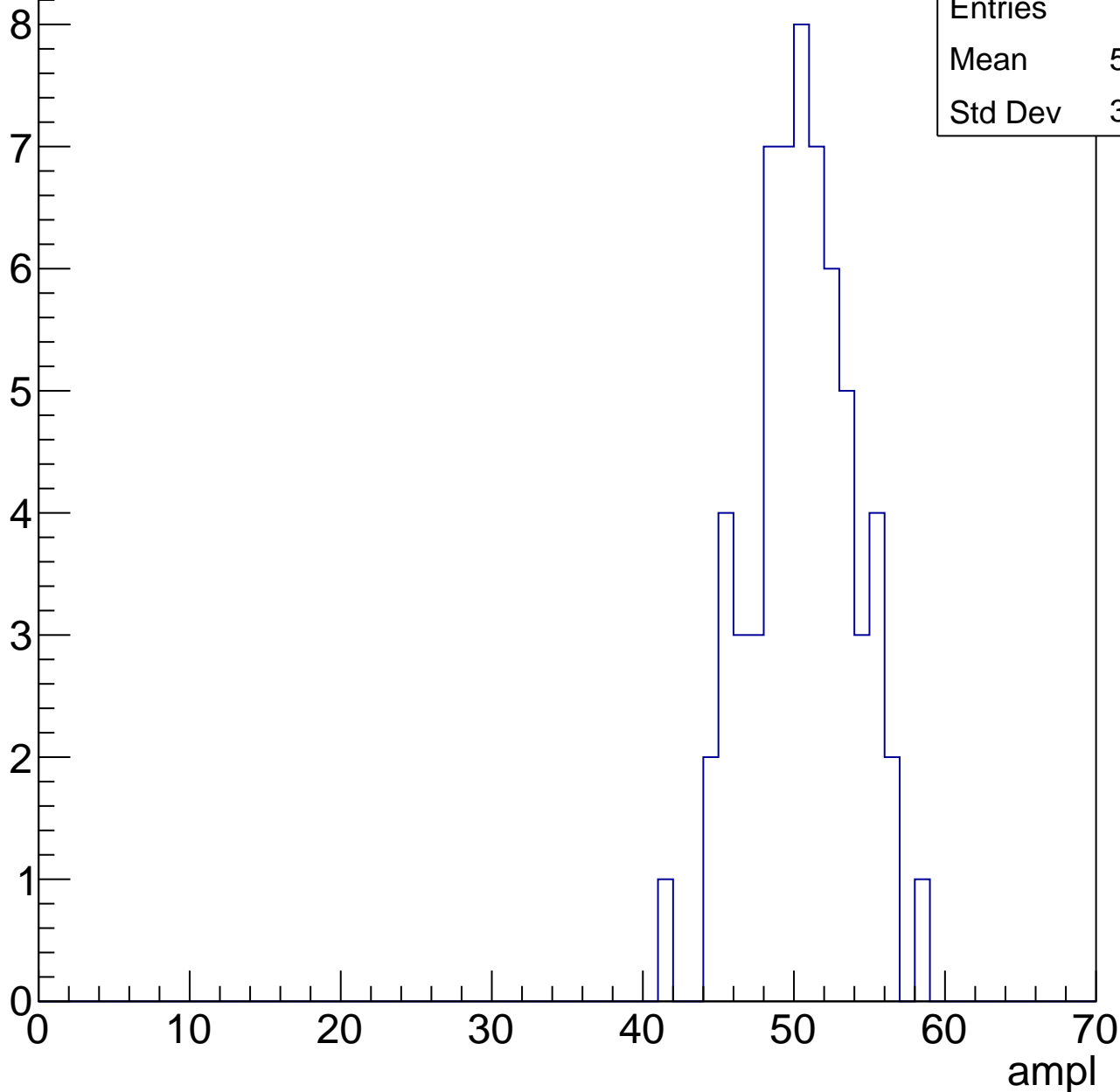


# B1L101S, U19-ch101, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	50.05
Std Dev	3.387

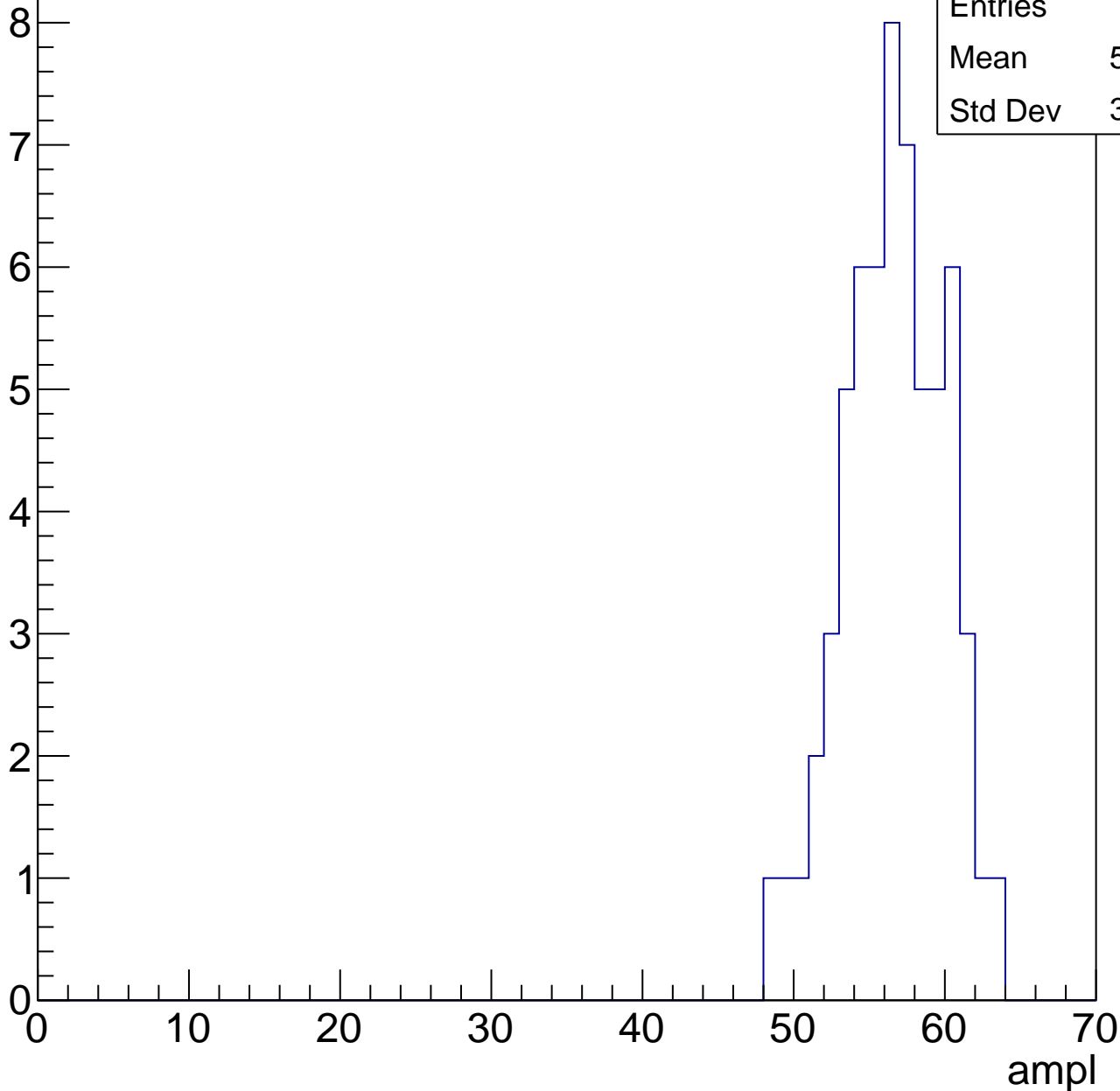


# B1L101S, U19-ch101, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	56.13
Std Dev	3.262

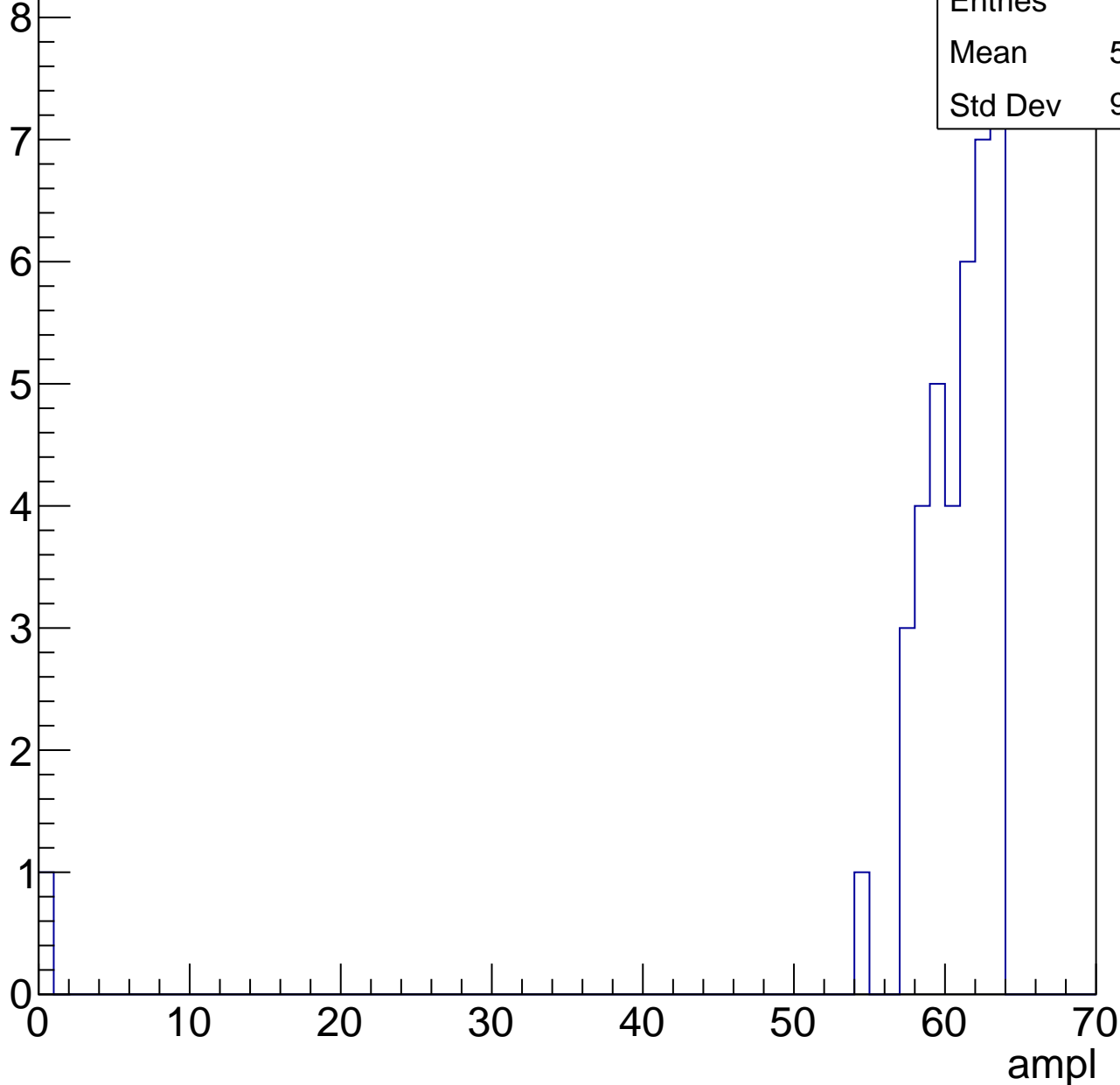


# B1L101S, U19-ch101, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	39
Mean	58.87
Std Dev	9.793



# B1L101S, U19-ch101, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	4
Mean	62
Std Dev	0.7071



# B1L101S, U19-ch101, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L101S, U19-ch102, adc0

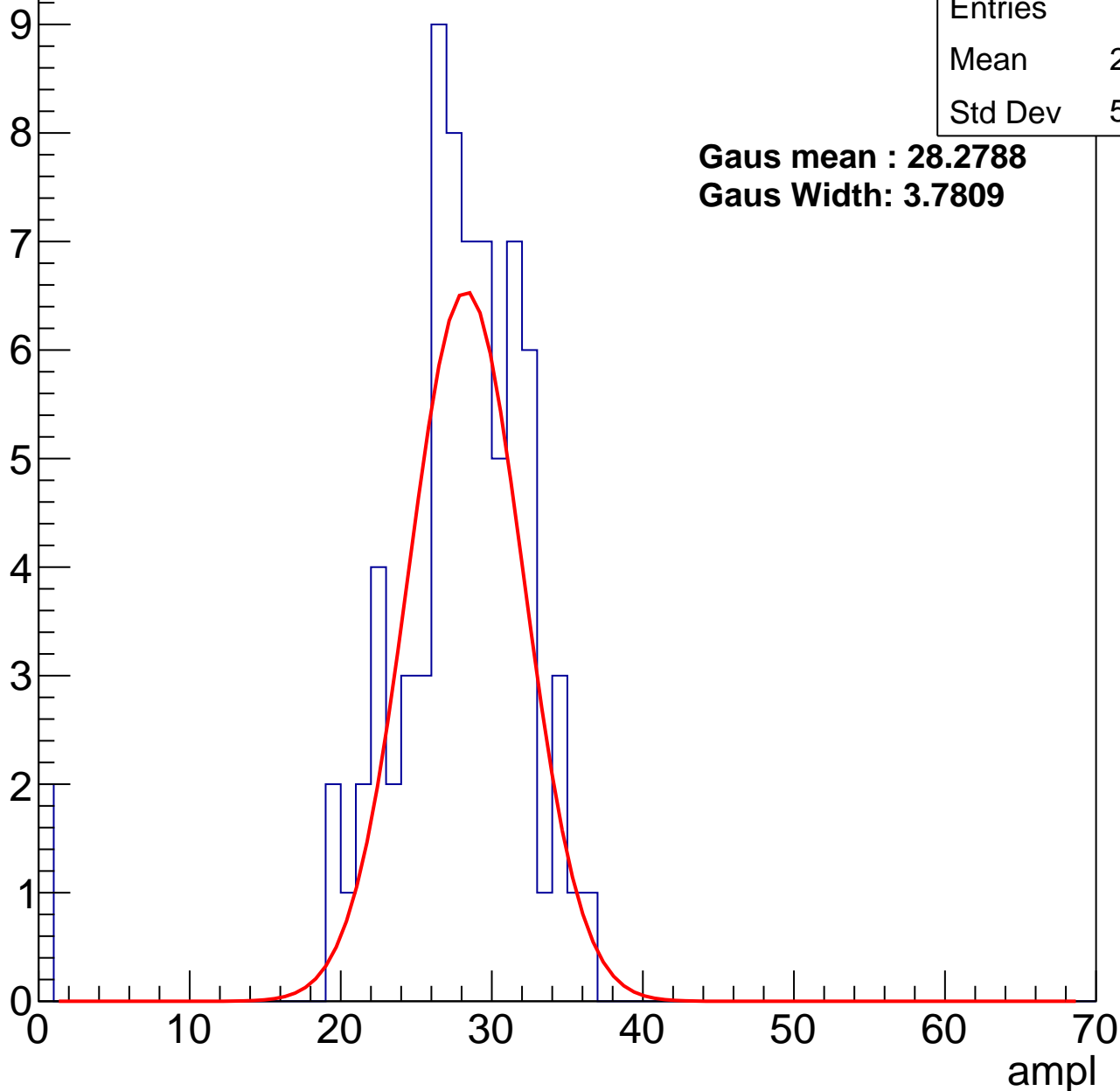
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	74
Mean	26.96
Std Dev	5.878

**Gaus mean : 28.2788**

**Gaus Width: 3.7809**



# B1L101S, U19-ch102, adc1

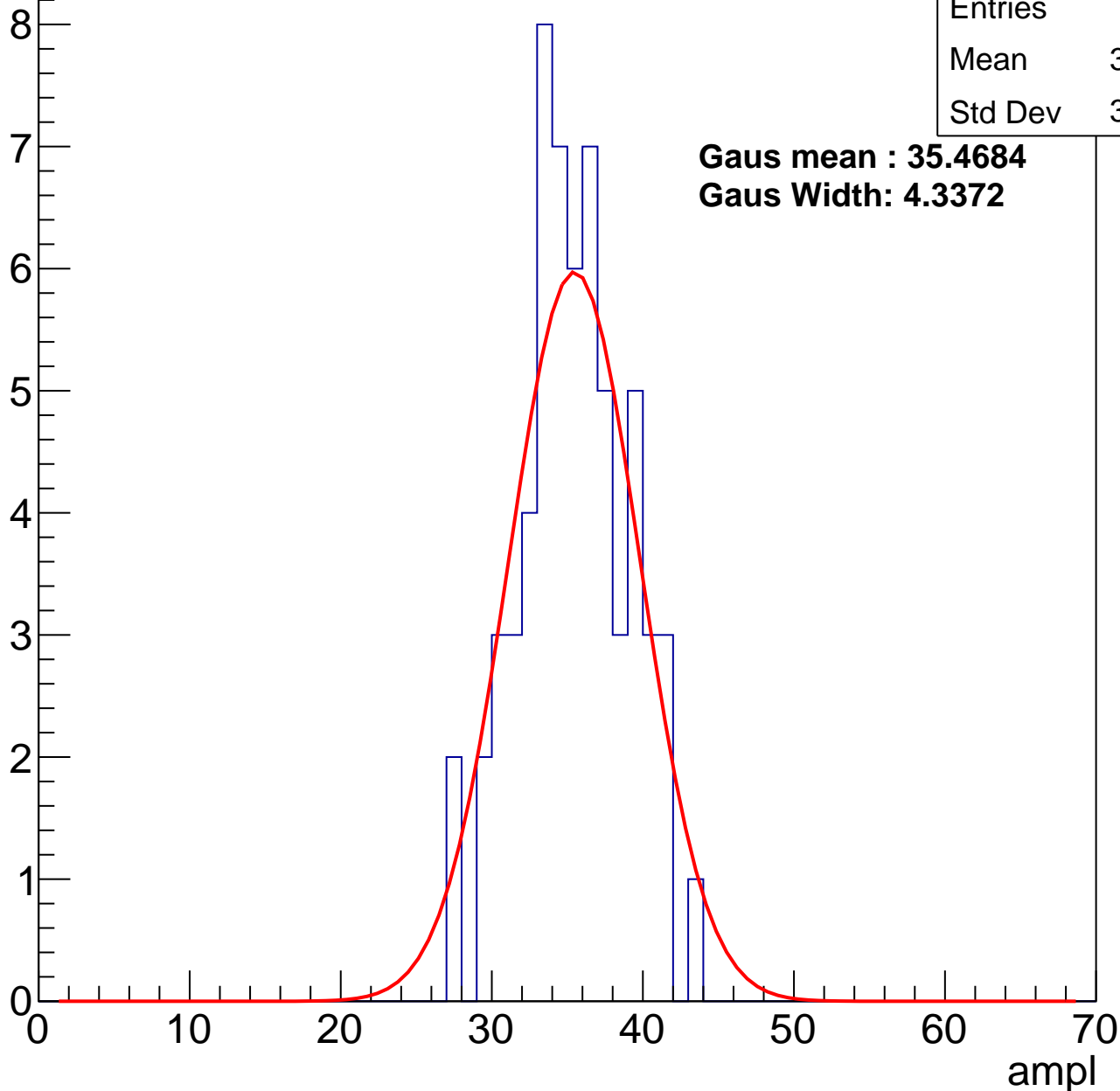
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	34.95
Std Dev	3.544

**Gaus mean : 35.4684**

**Gaus Width: 4.3372**



# B1L101S, U19-ch102, adc2

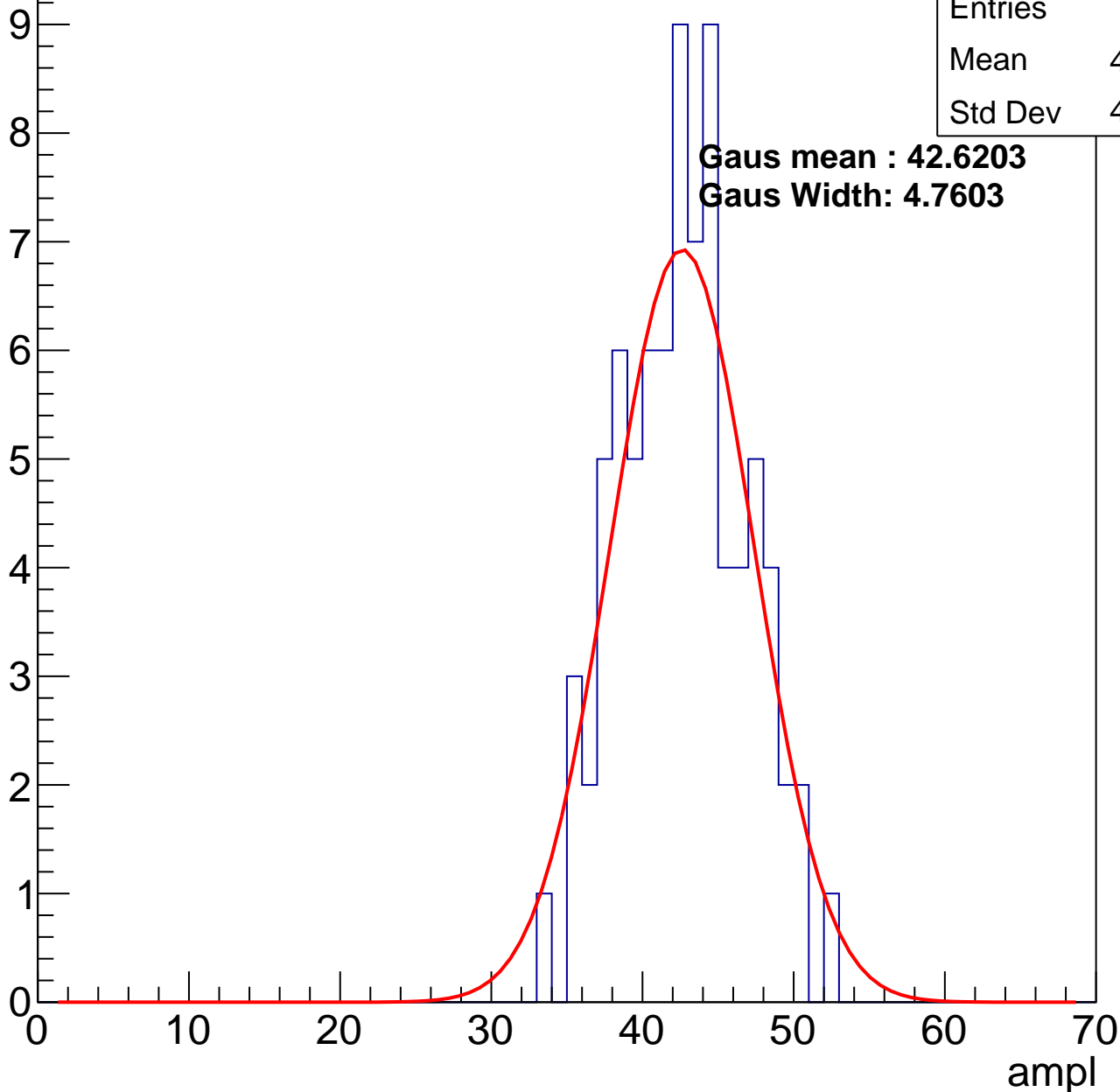
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	81
Mean	42.22
Std Dev	4.052

**Gaus mean : 42.6203**

**Gaus Width: 4.7603**

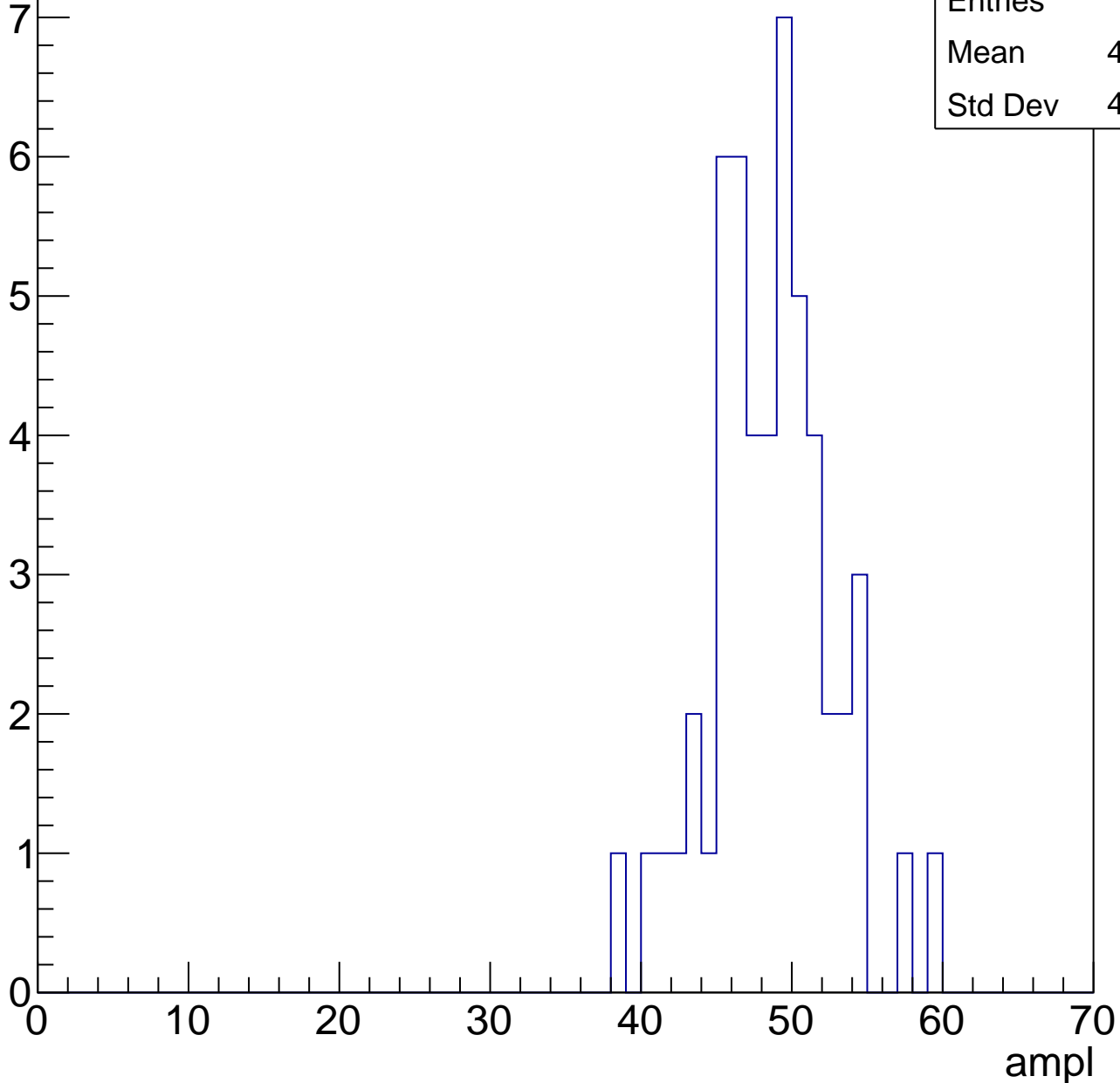


# B1L101S, U19-ch102, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	52
Mean	48.12
Std Dev	4.046

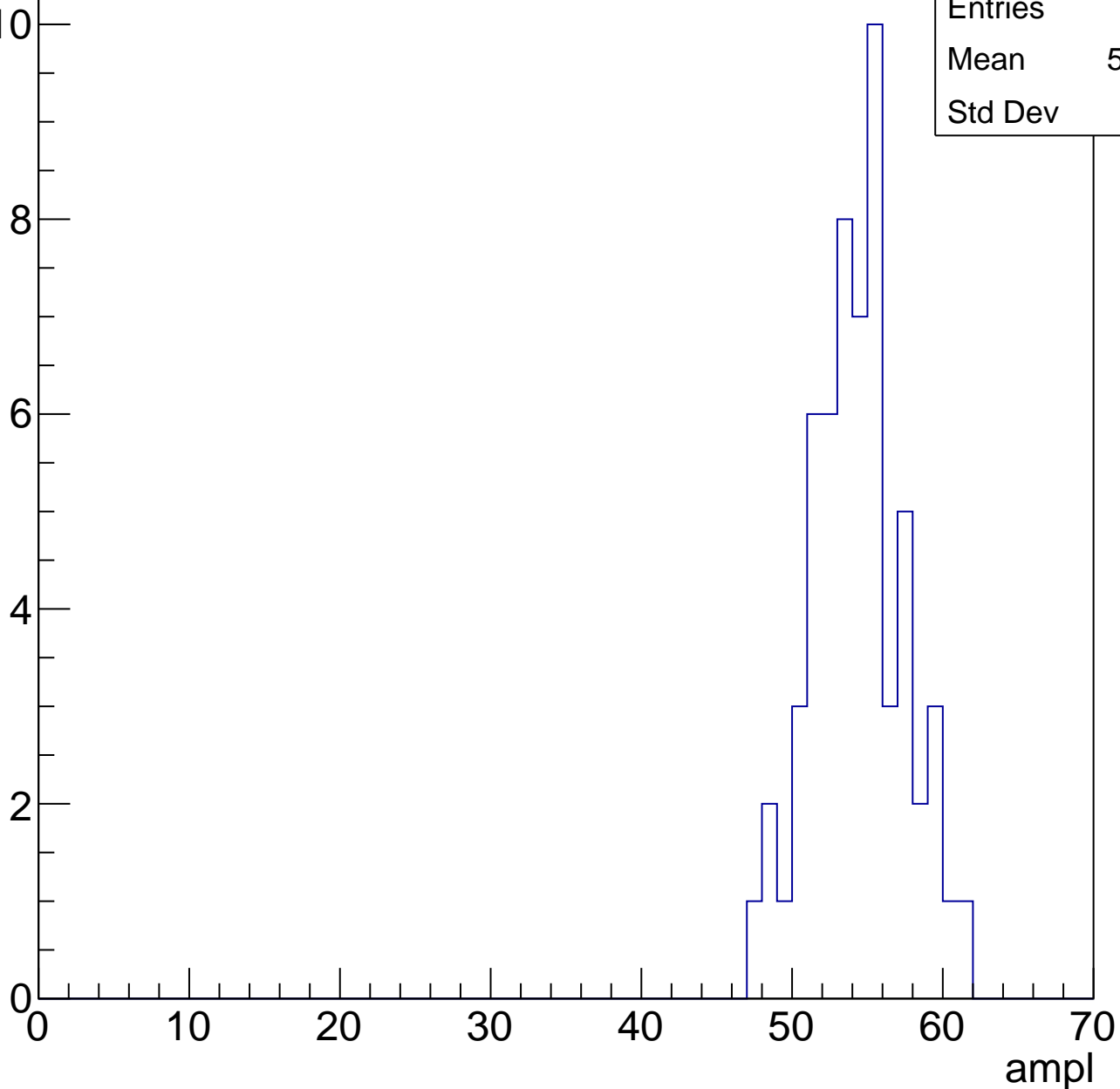


# B1L101S, U19-ch102, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	59
Mean	53.88
Std Dev	3.02

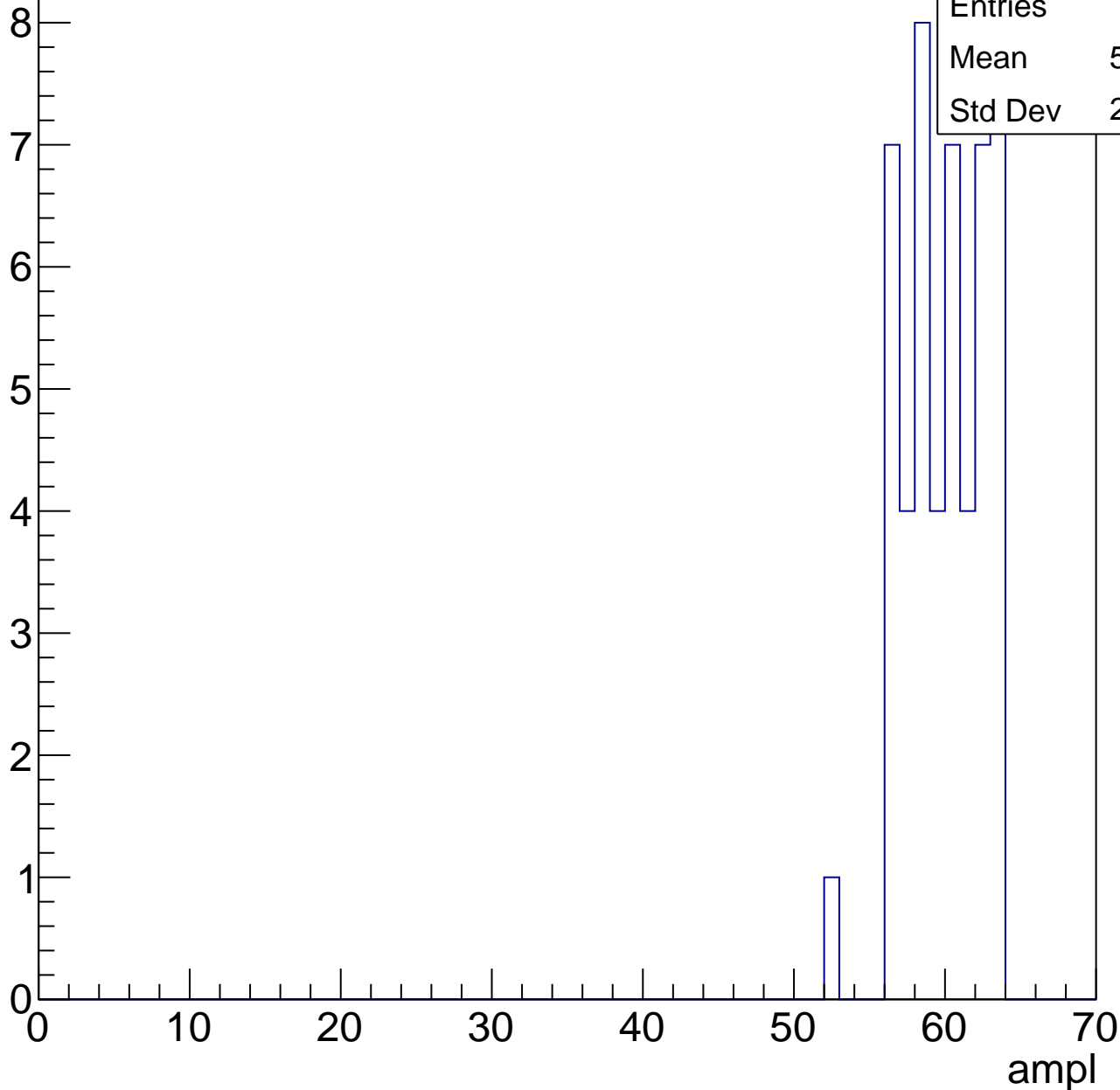


# B1L101S, U19-ch102, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	50
Mean	59.48
Std Dev	2.602

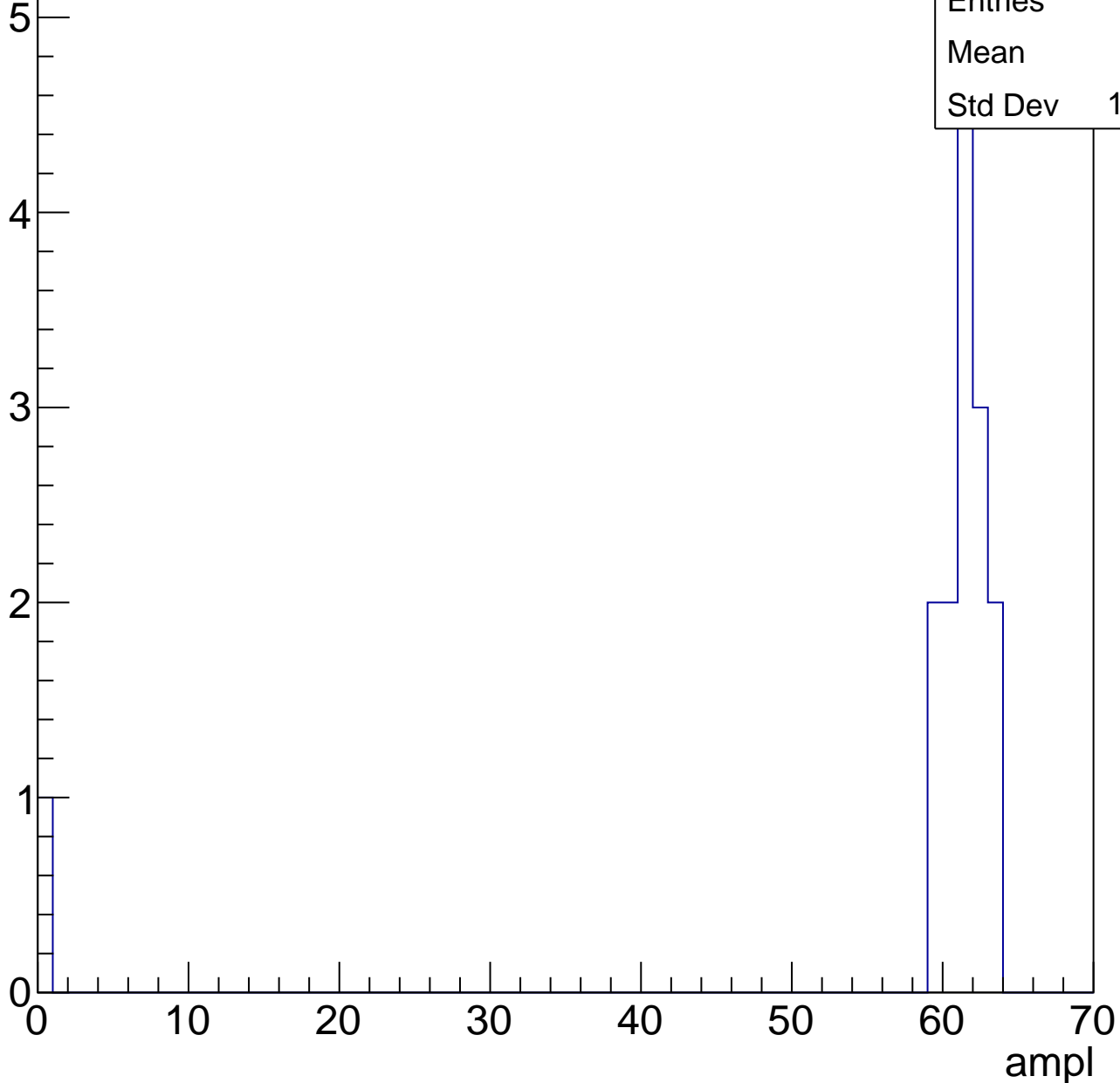


# B1L101S, U19-ch102, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	15
Mean	57
Std Dev	15.28





# B1L101S, U19-ch102, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L101S, U19-ch103, adc0

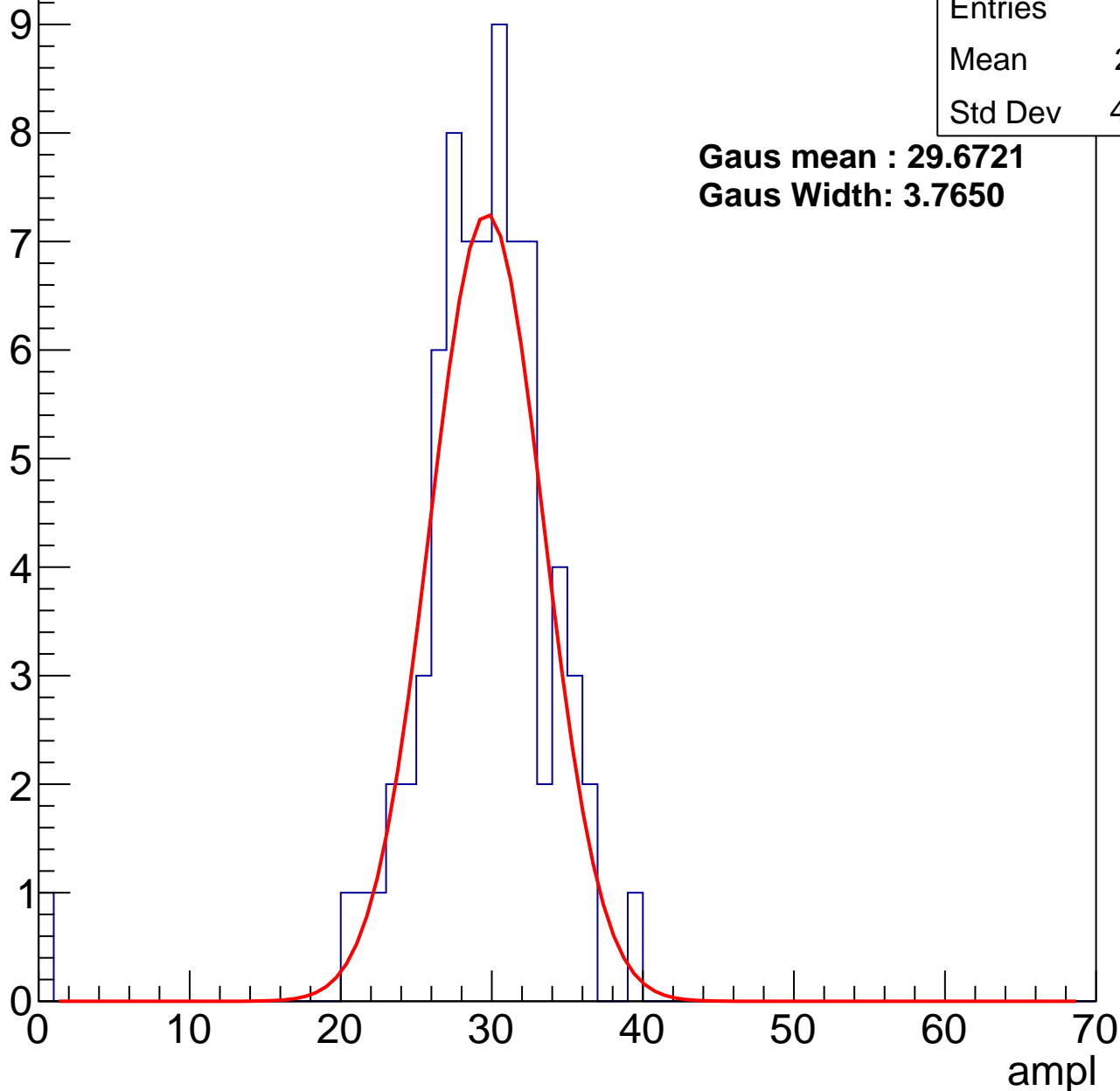
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	74
Mean	28.81
Std Dev	4.977

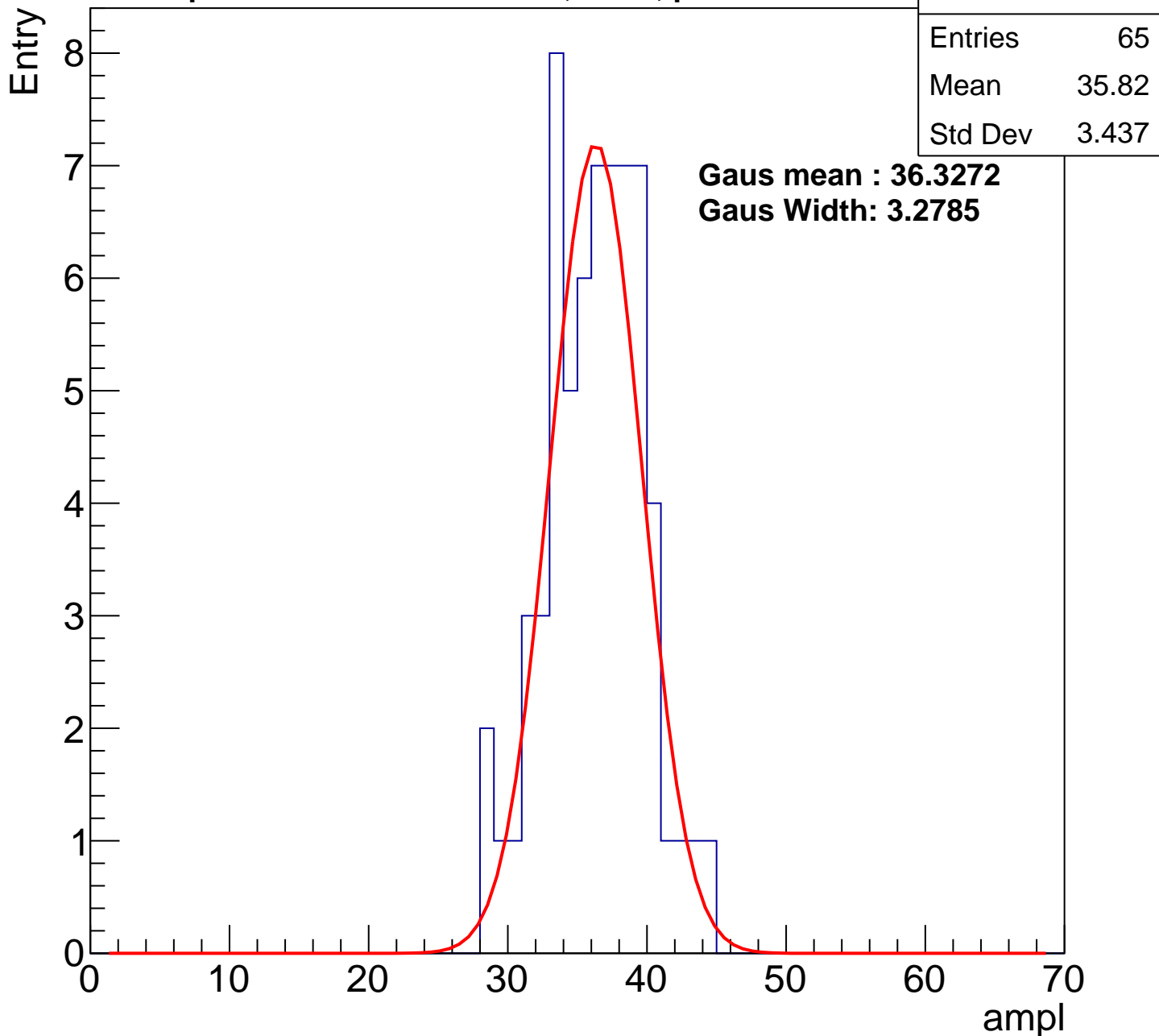
**Gaus mean : 29.6721**

**Gaus Width: 3.7650**



# B1L101S, U19-ch103, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U19-ch103, adc2

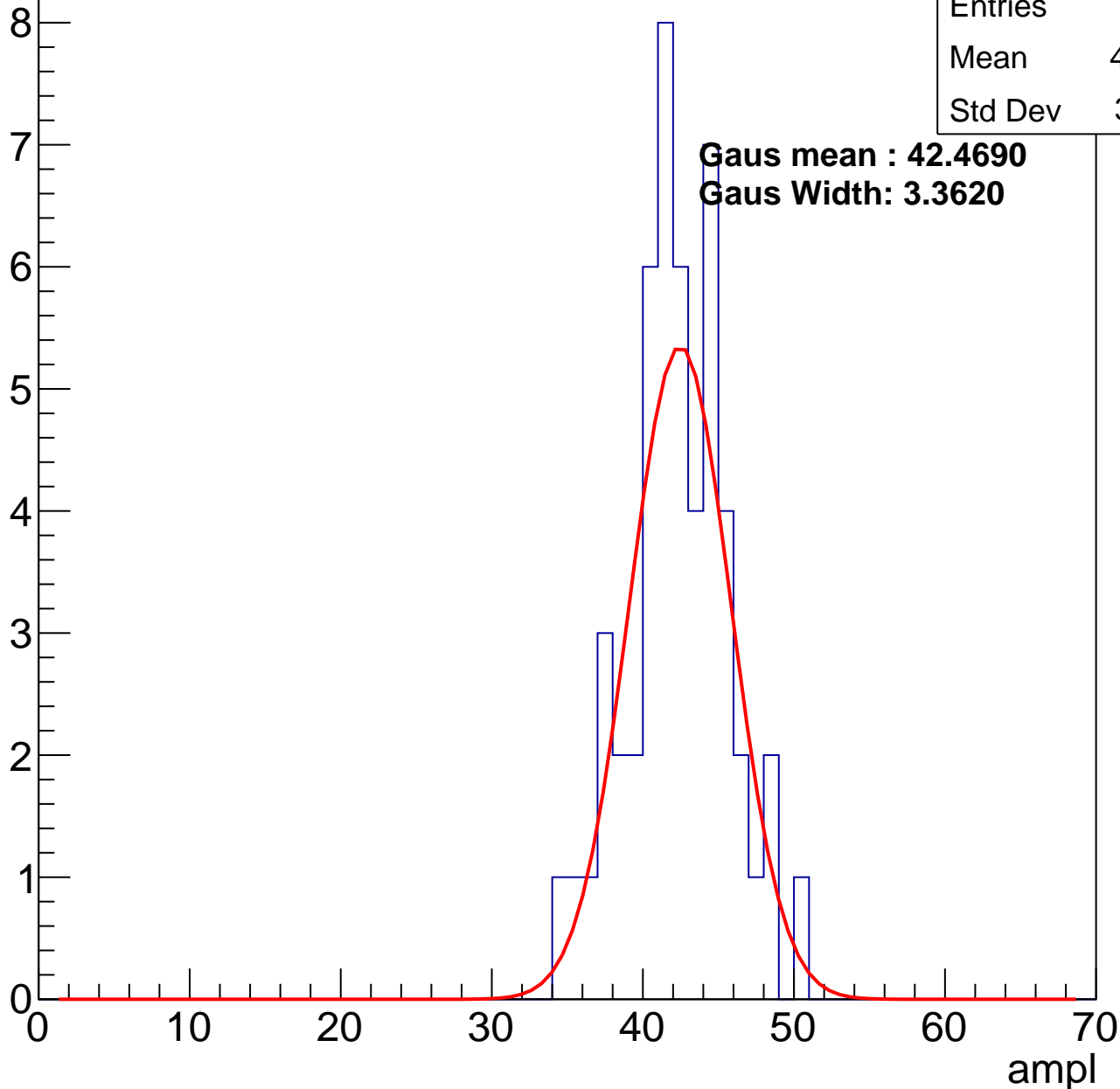
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	51
Mean	41.86
Std Dev	3.331

**Gaus mean : 42.4690**

**Gaus Width: 3.3620**

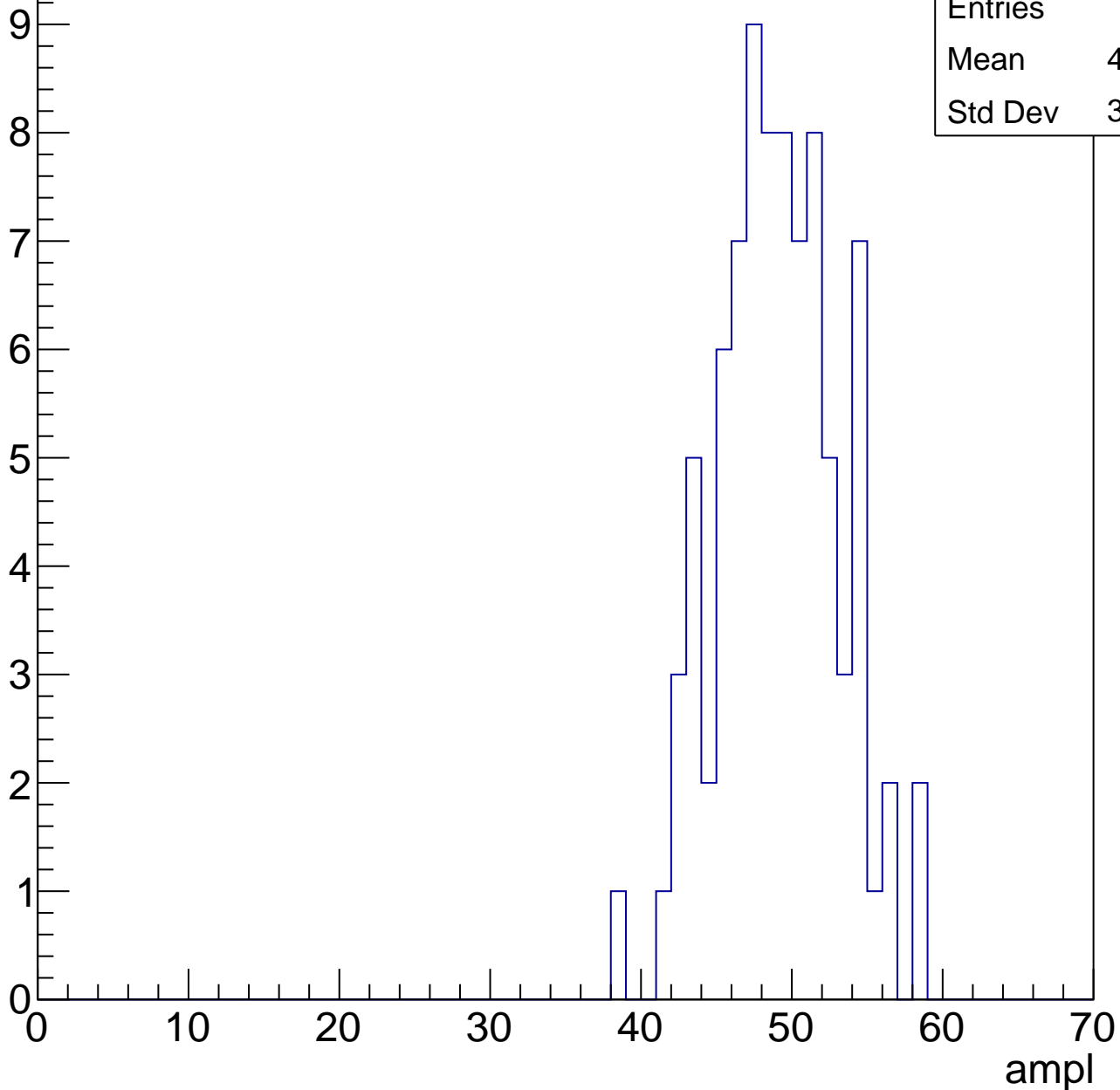


# B1L101S, U19-ch103, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	85
Mean	48.67
Std Dev	3.998

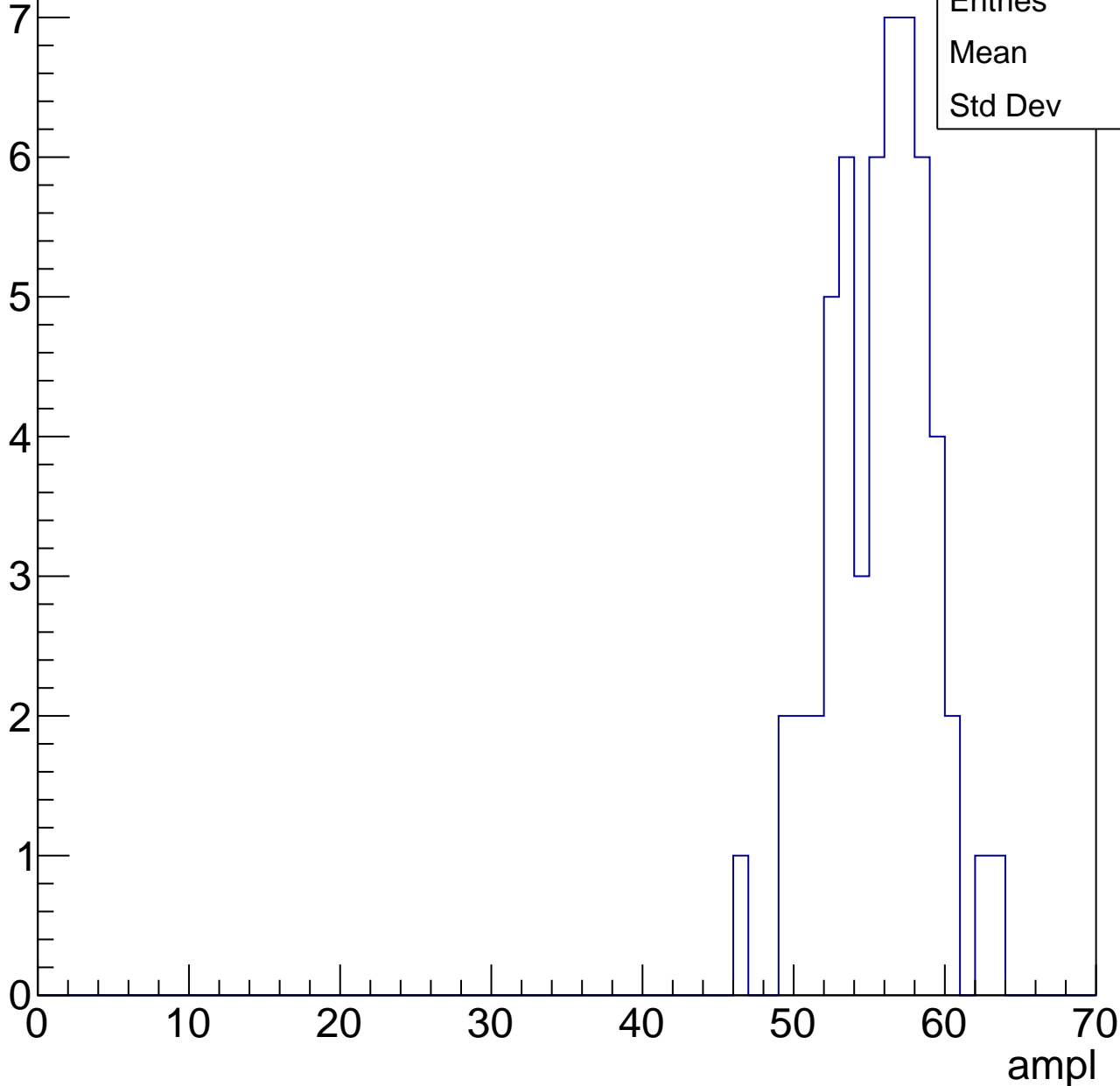


# B1L101S, U19-ch103, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	55
Mean	55.2
Std Dev	3.36



# B1L101S, U19-ch103, adc5

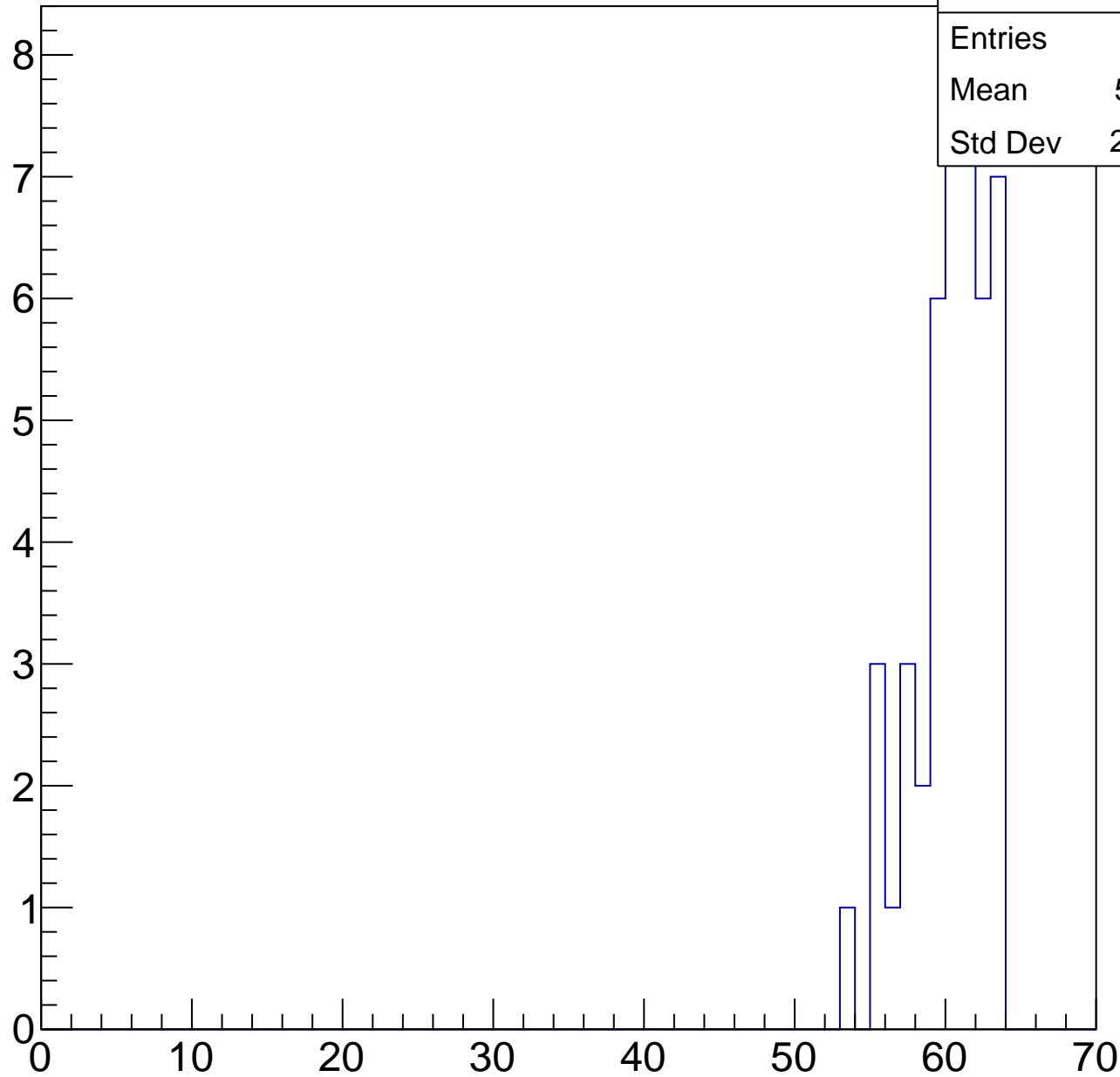
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	45
Mean	59.91
Std Dev	2.475

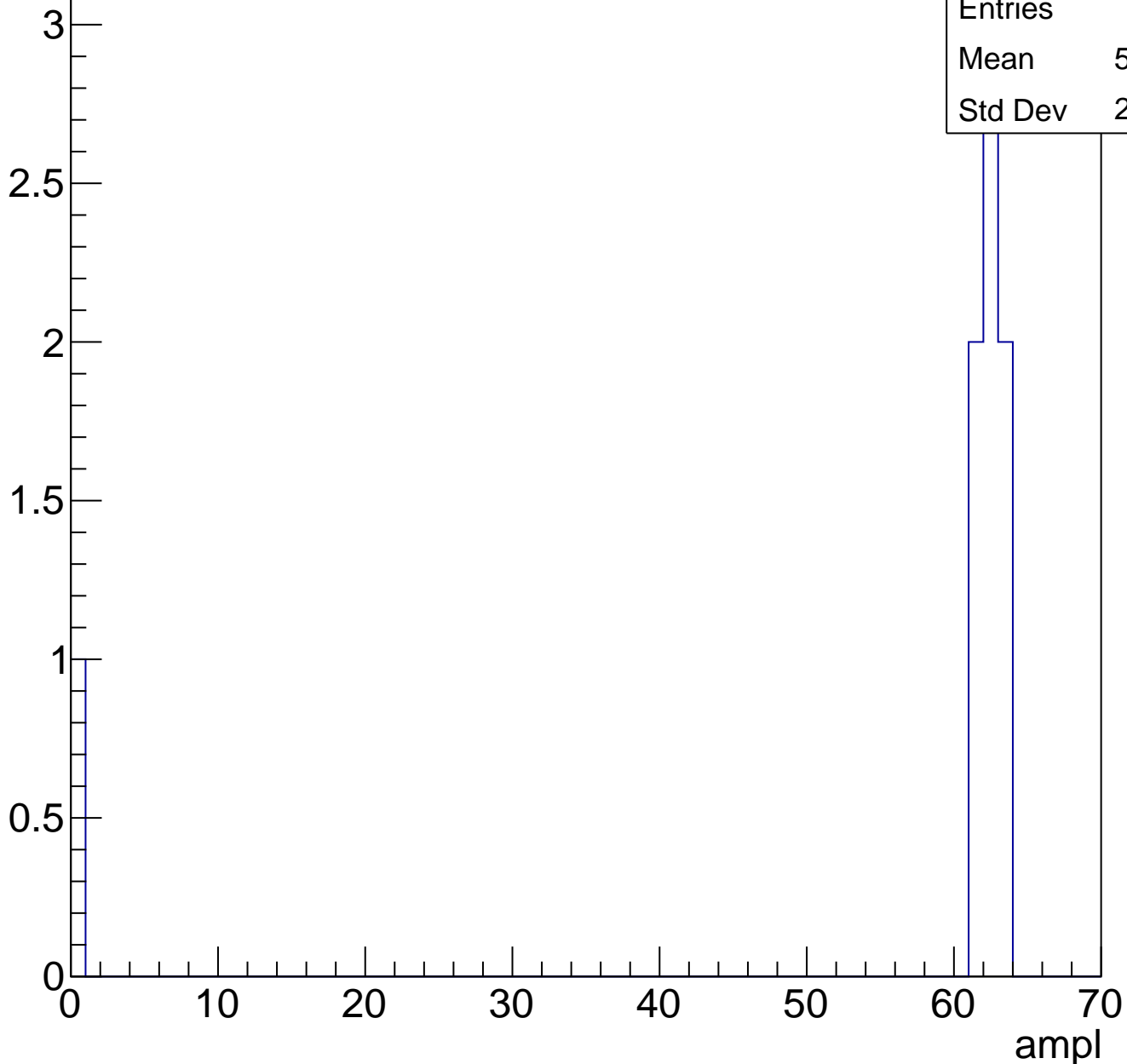
ampl



# B1L101S, U19-ch103, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



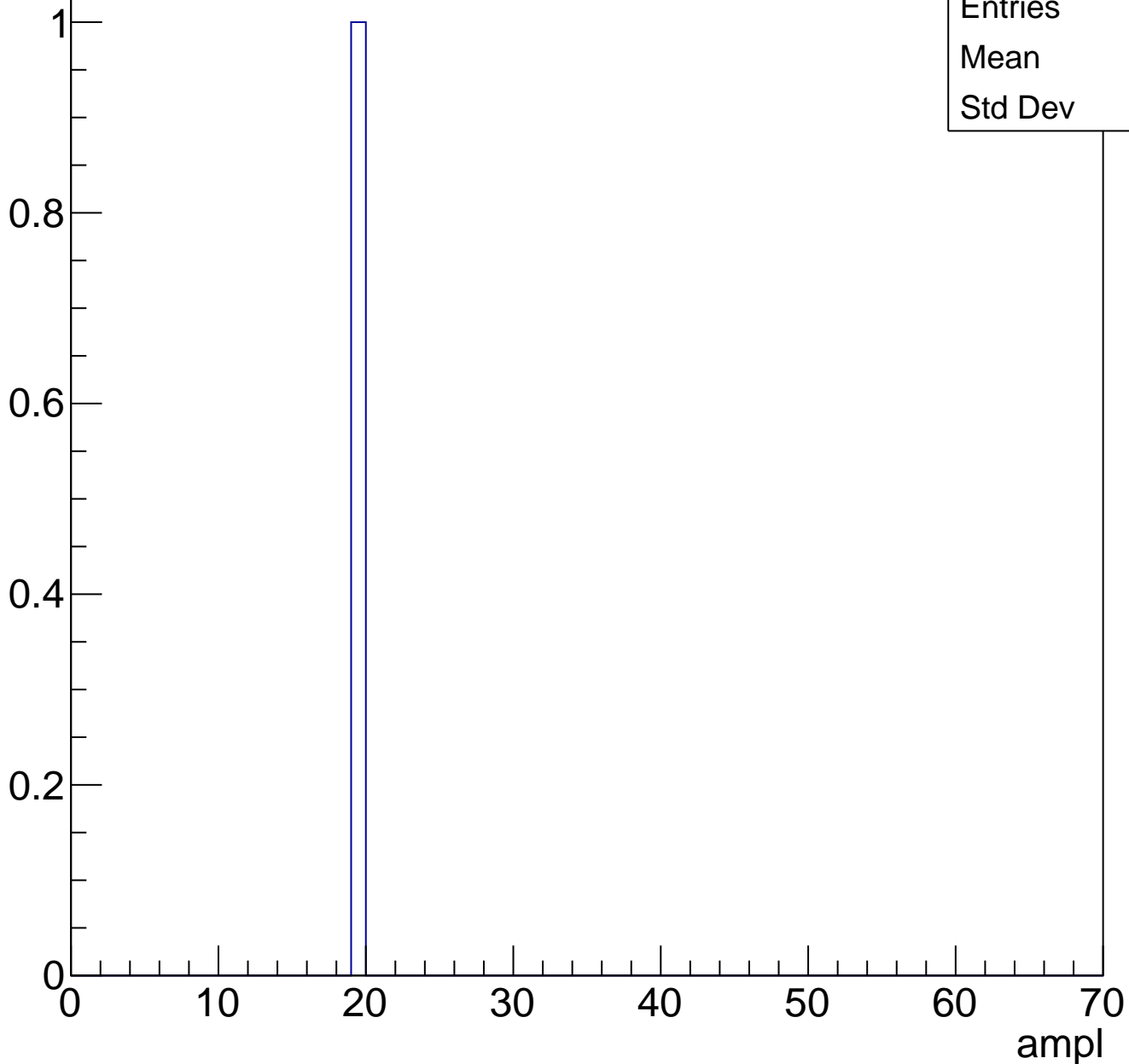
Entries	8
Mean	54.25
Std Dev	20.52



# B1L101S, U19-ch103, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U19-ch104, adc0

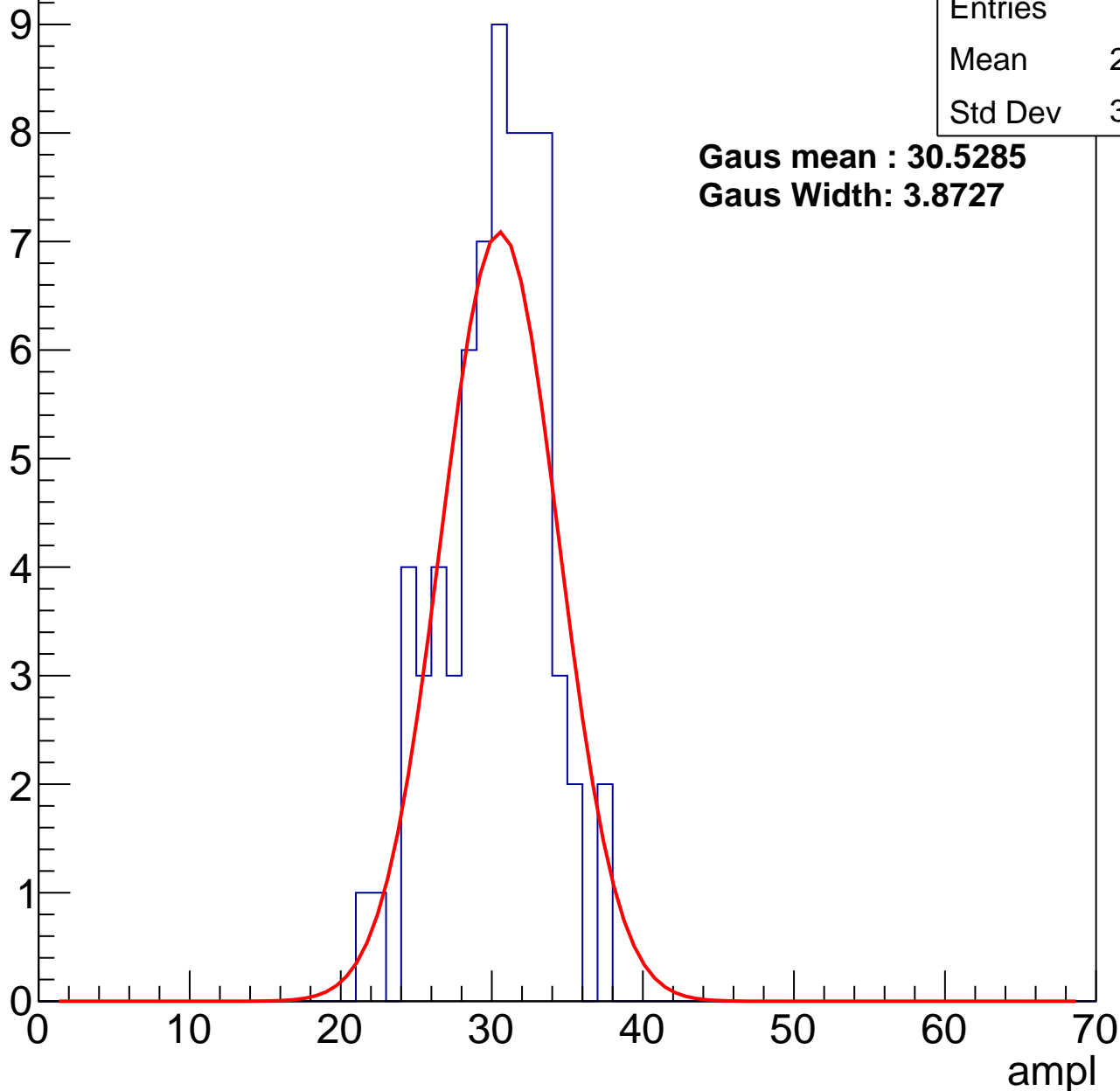
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	29.77
Std Dev	3.384

**Gaus mean : 30.5285**

**Gaus Width: 3.8727**



# B1L101S, U19-ch104, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	60
Mean	36.32
Std Dev	5.67

**Gaus mean : 37.1451**

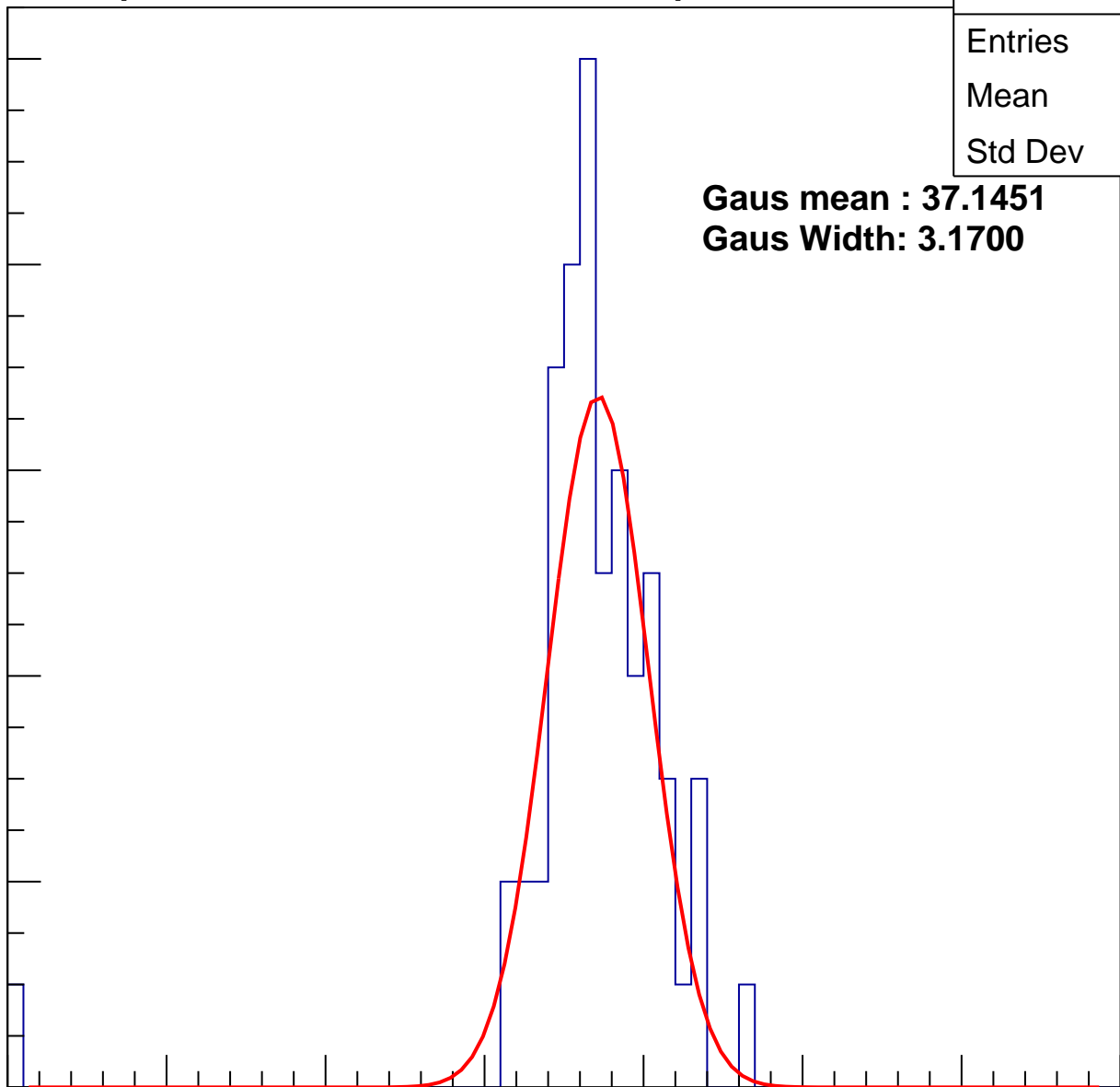
**Gaus Width: 3.1700**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U19-ch104, adc2

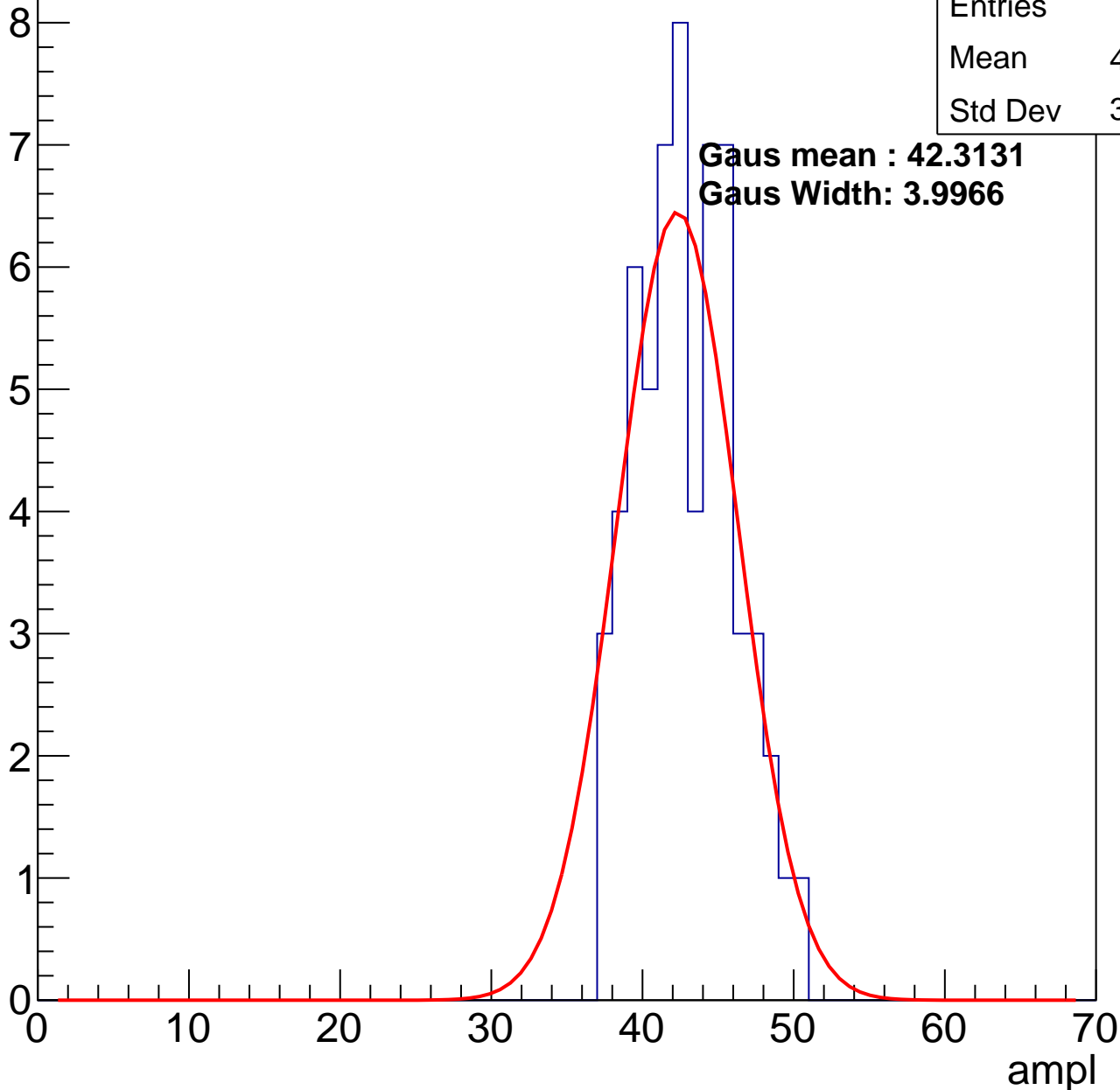
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	42.44
Std Dev	3.165

**Gaus mean : 42.3131**

**Gaus Width: 3.9966**

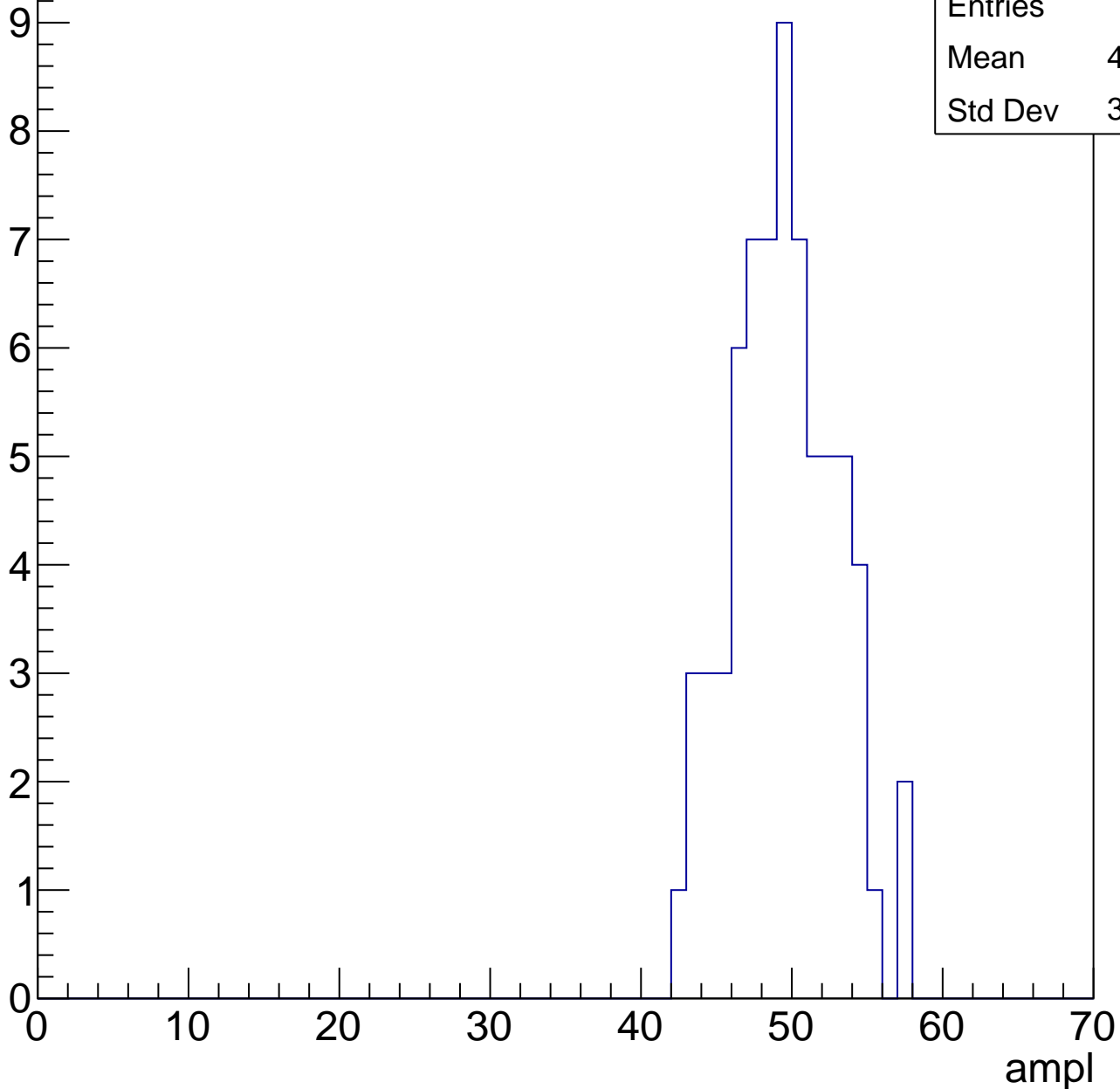


# B1L101S, U19-ch104, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	49.04
Std Dev	3.397

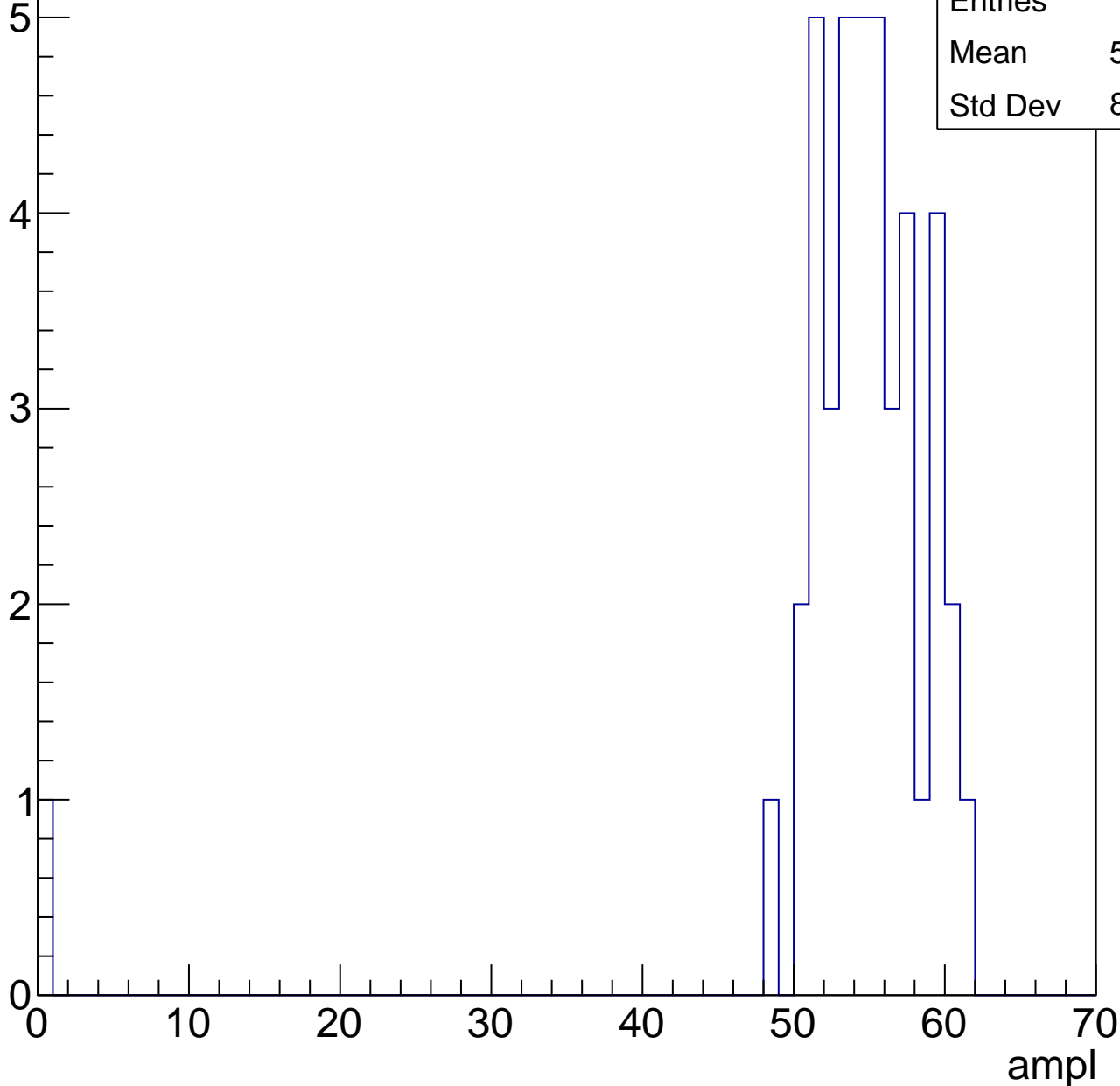


# B1L101S, U19-ch104, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	42
Mean	53.33
Std Dev	8.887

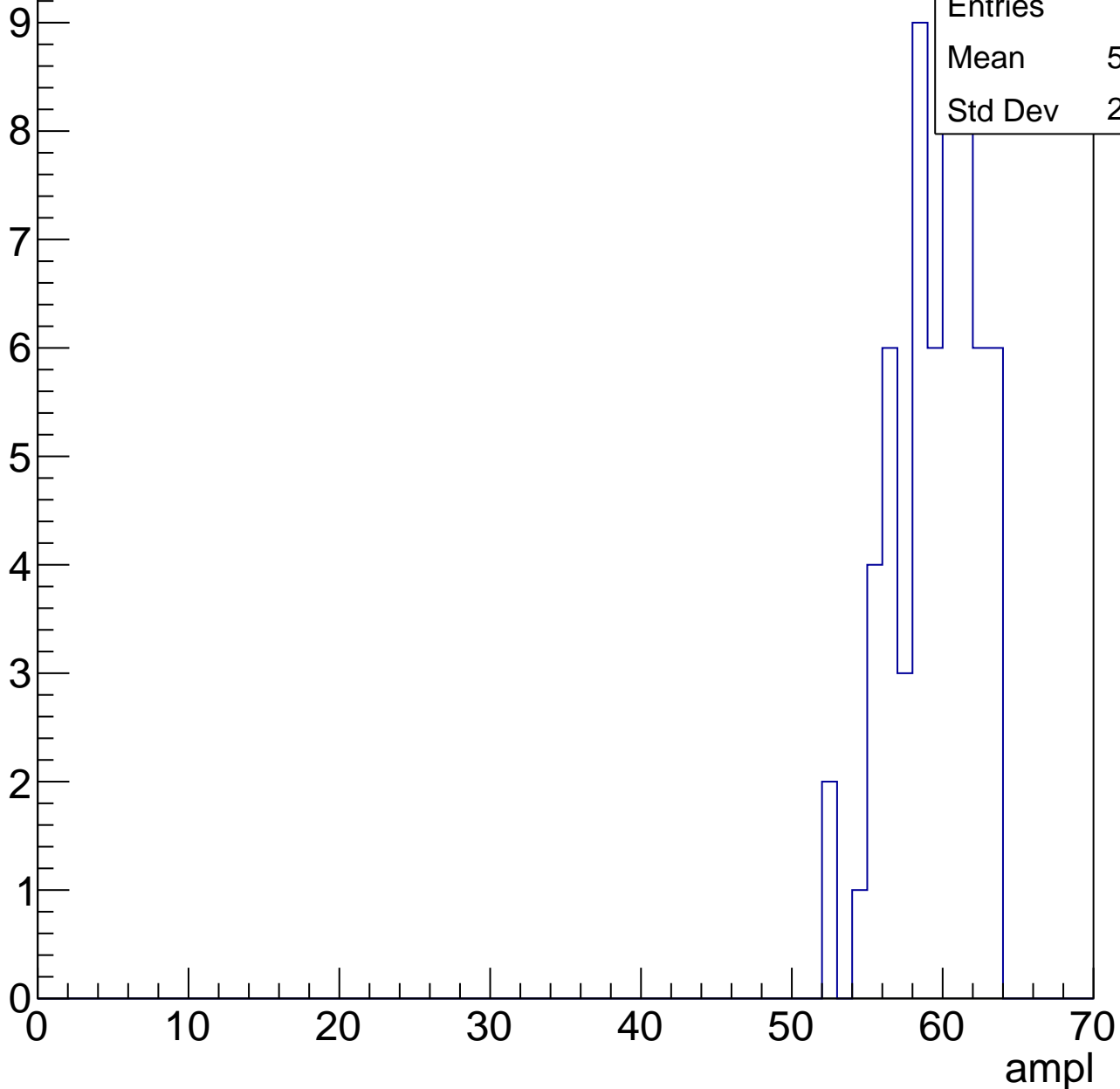


# B1L101S, U19-ch104, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

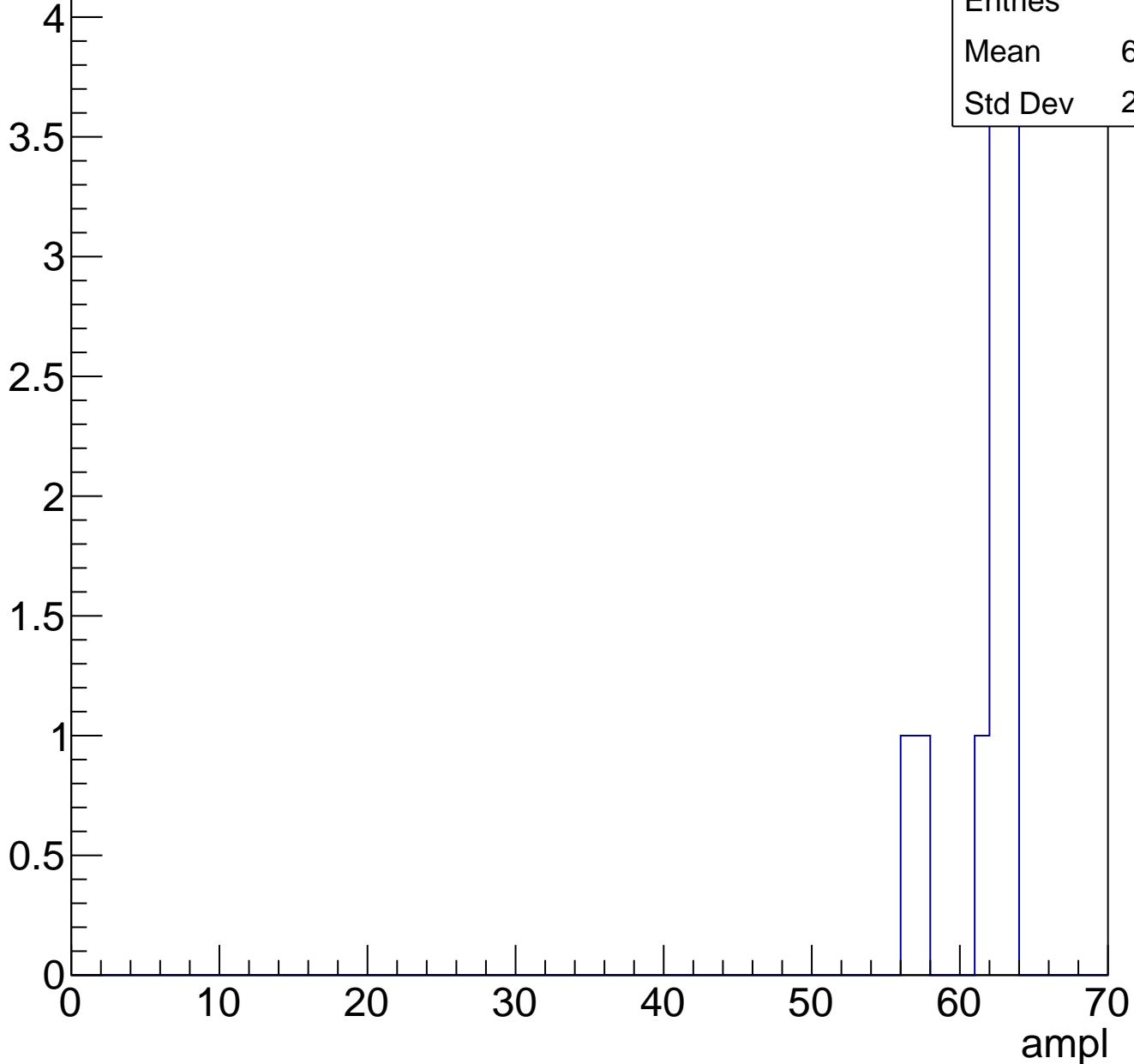
Entries	59
Mean	58.97
Std Dev	2.768



# B1L101S, U19-ch104, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



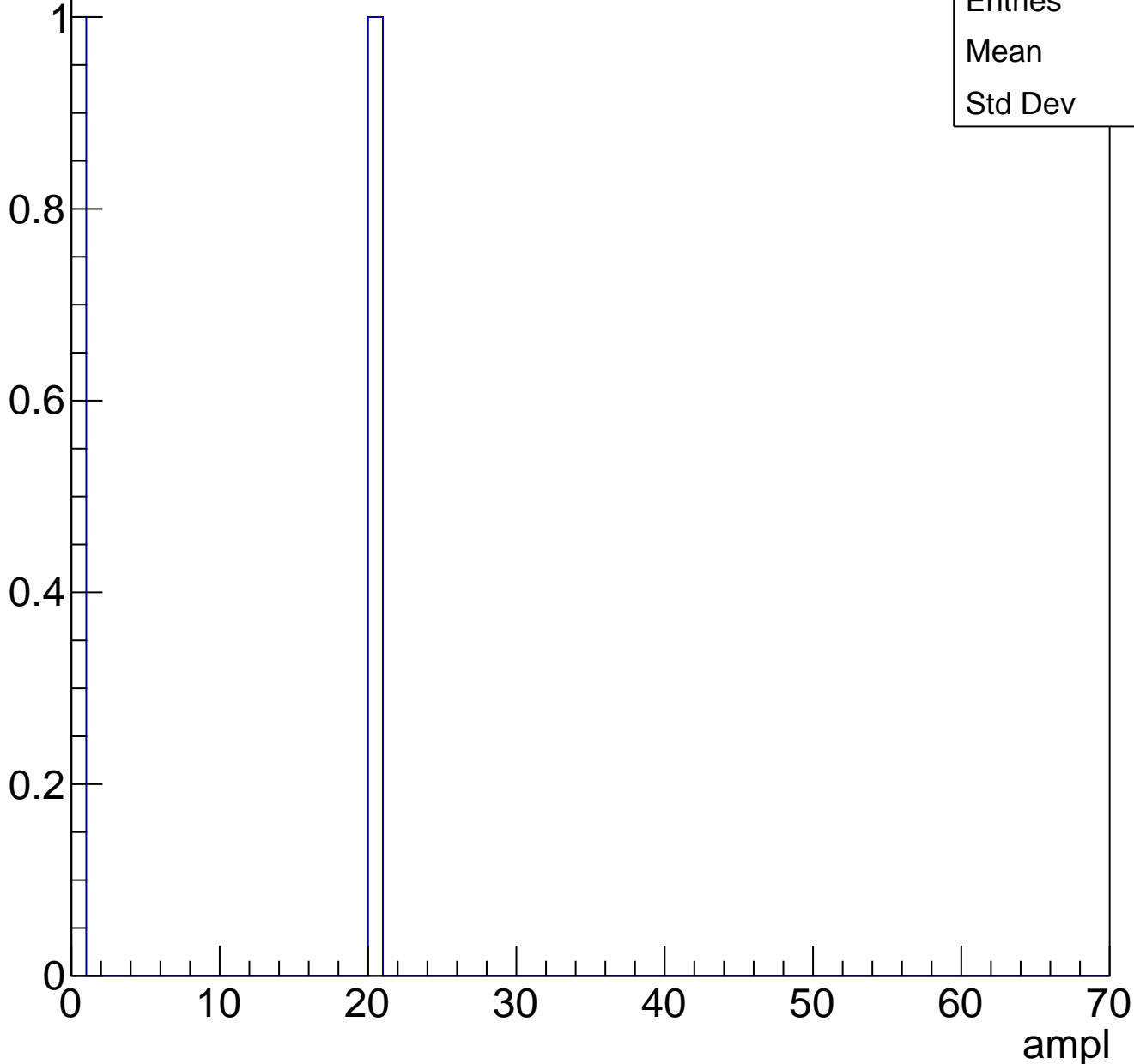
Entries	11
Mean	61.27
Std Dev	2.339



# B1L101S, U19-ch104, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U19-ch105, adc0

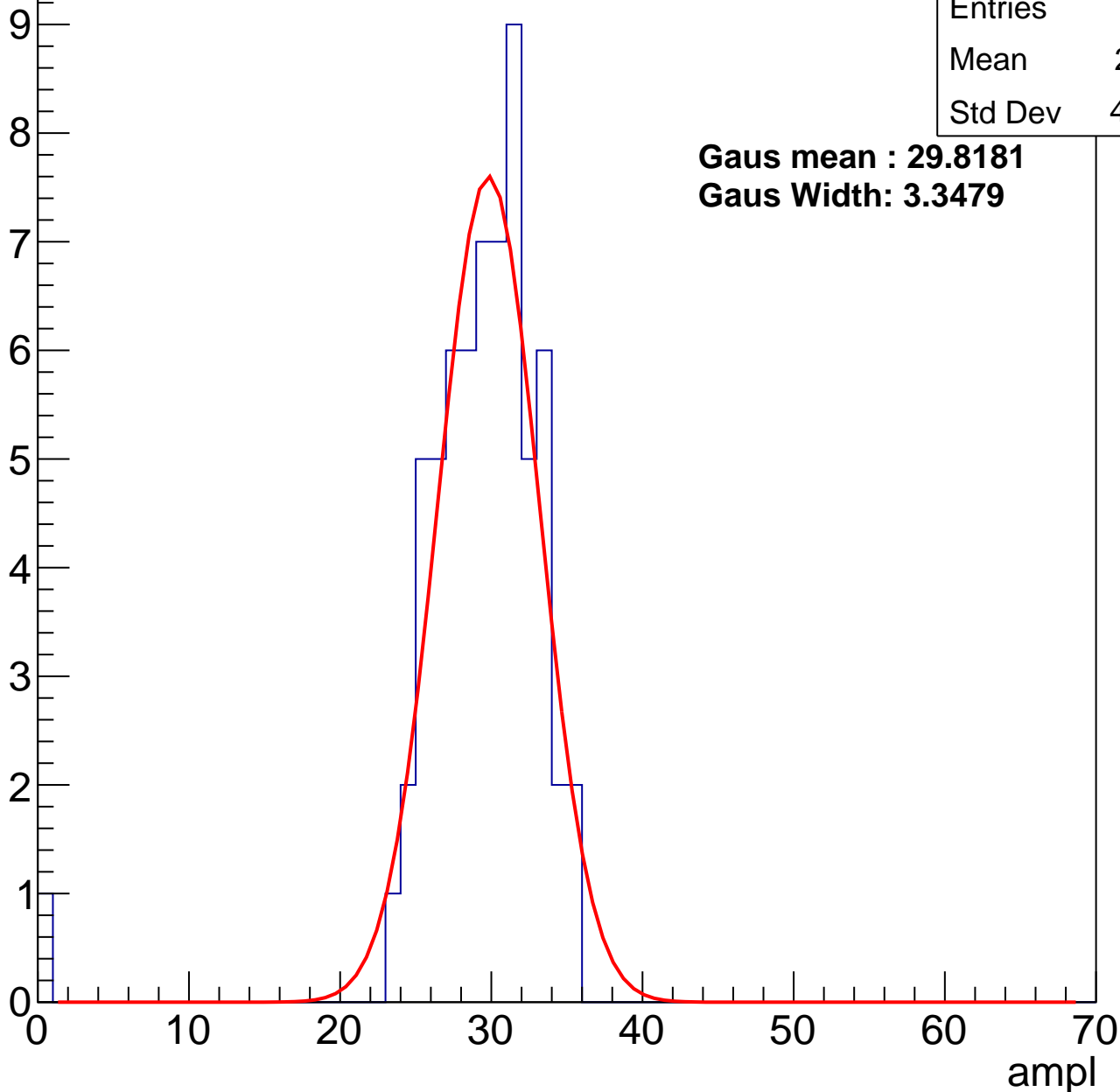
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	28.81
Std Dev	4.653

**Gaus mean : 29.8181**

**Gaus Width: 3.3479**



# B1L101S, U19-ch105, adc1

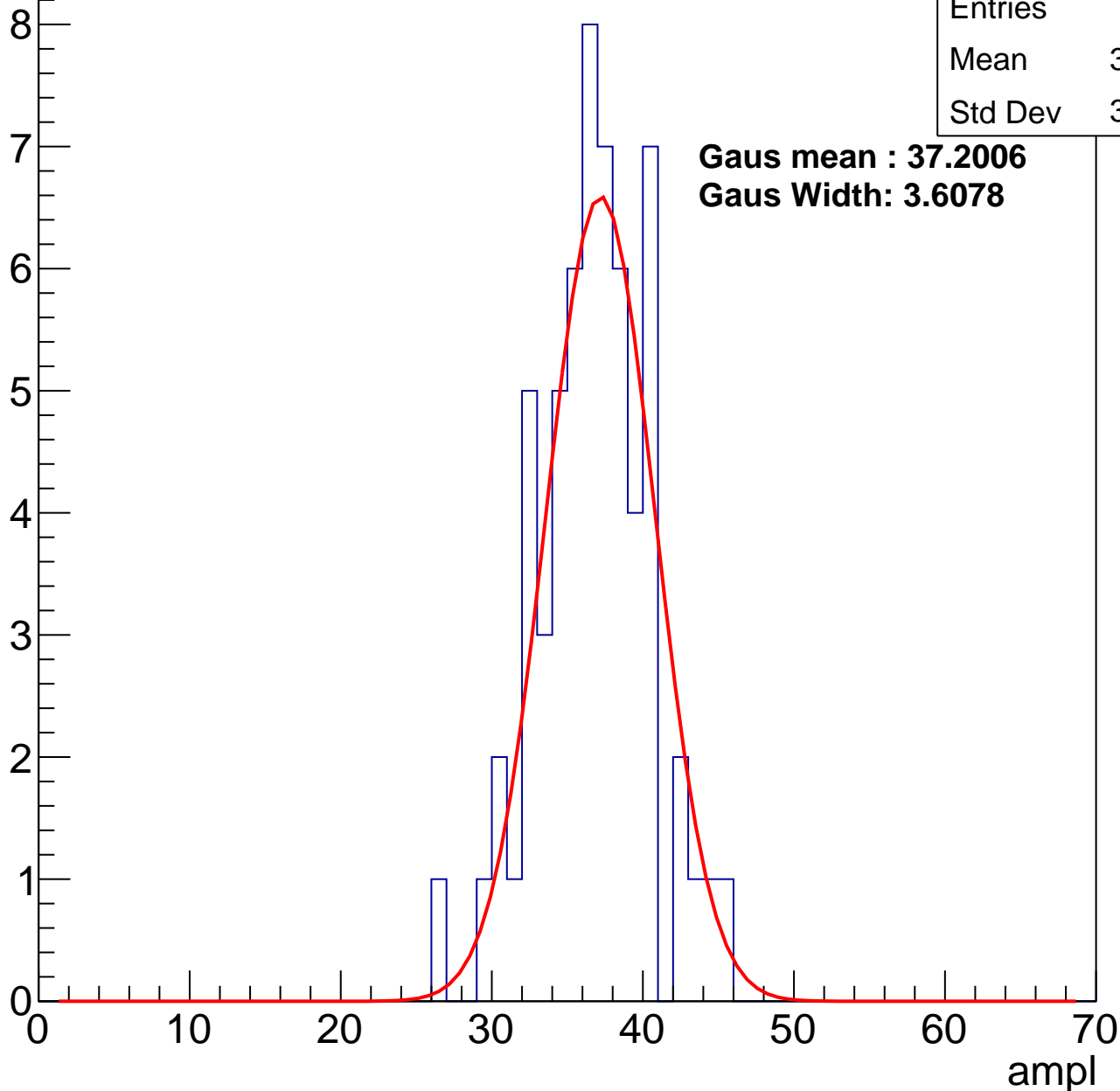
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	36.26
Std Dev	3.666

**Gaus mean : 37.2006**

**Gaus Width: 3.6078**



# B1L101S, U19-ch105, adc2

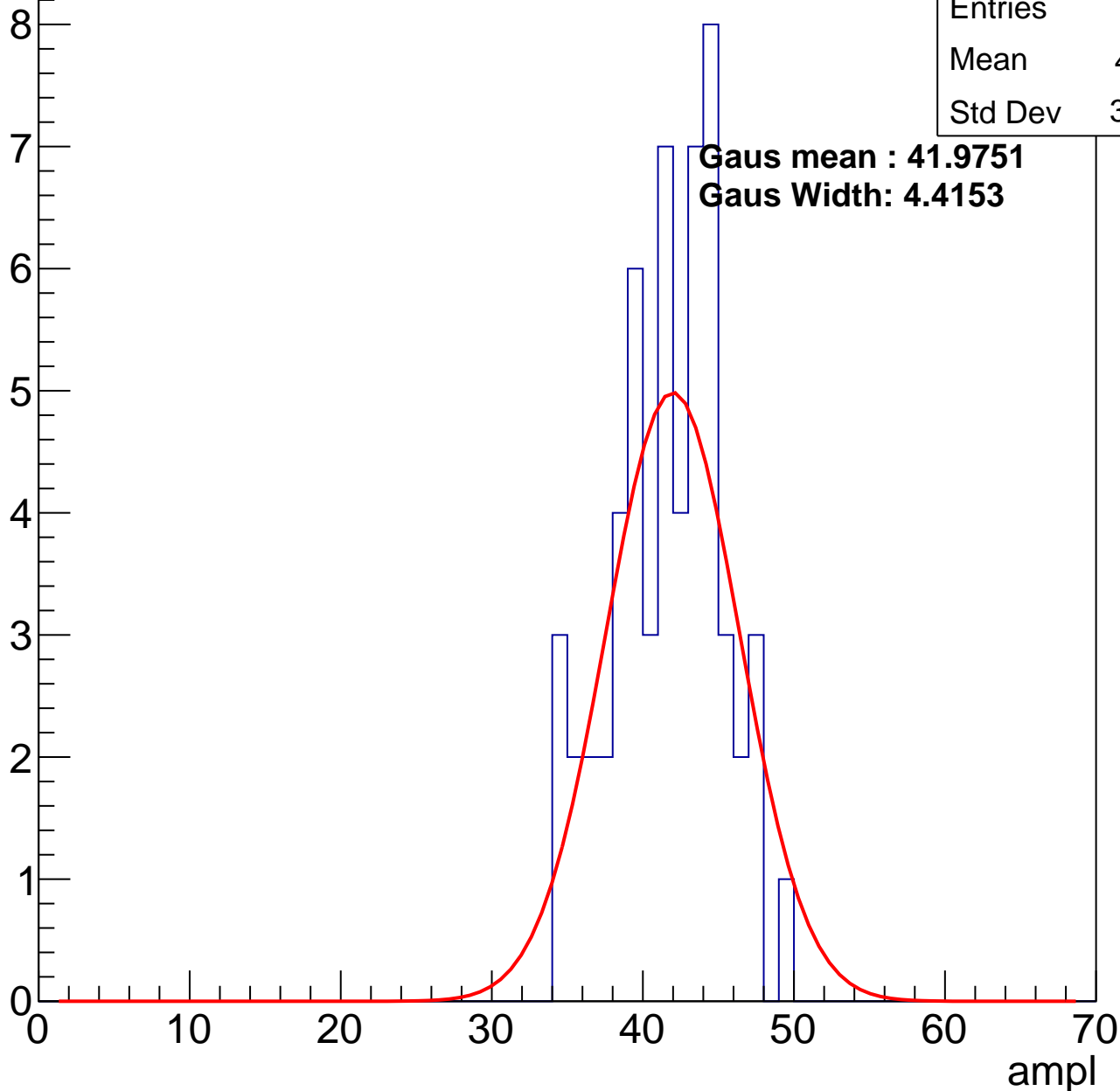
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	57
Mean	41.21
Std Dev	3.592

**Gaus mean : 41.9751**

**Gaus Width: 4.4153**



# B1L101S, U19-ch105, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

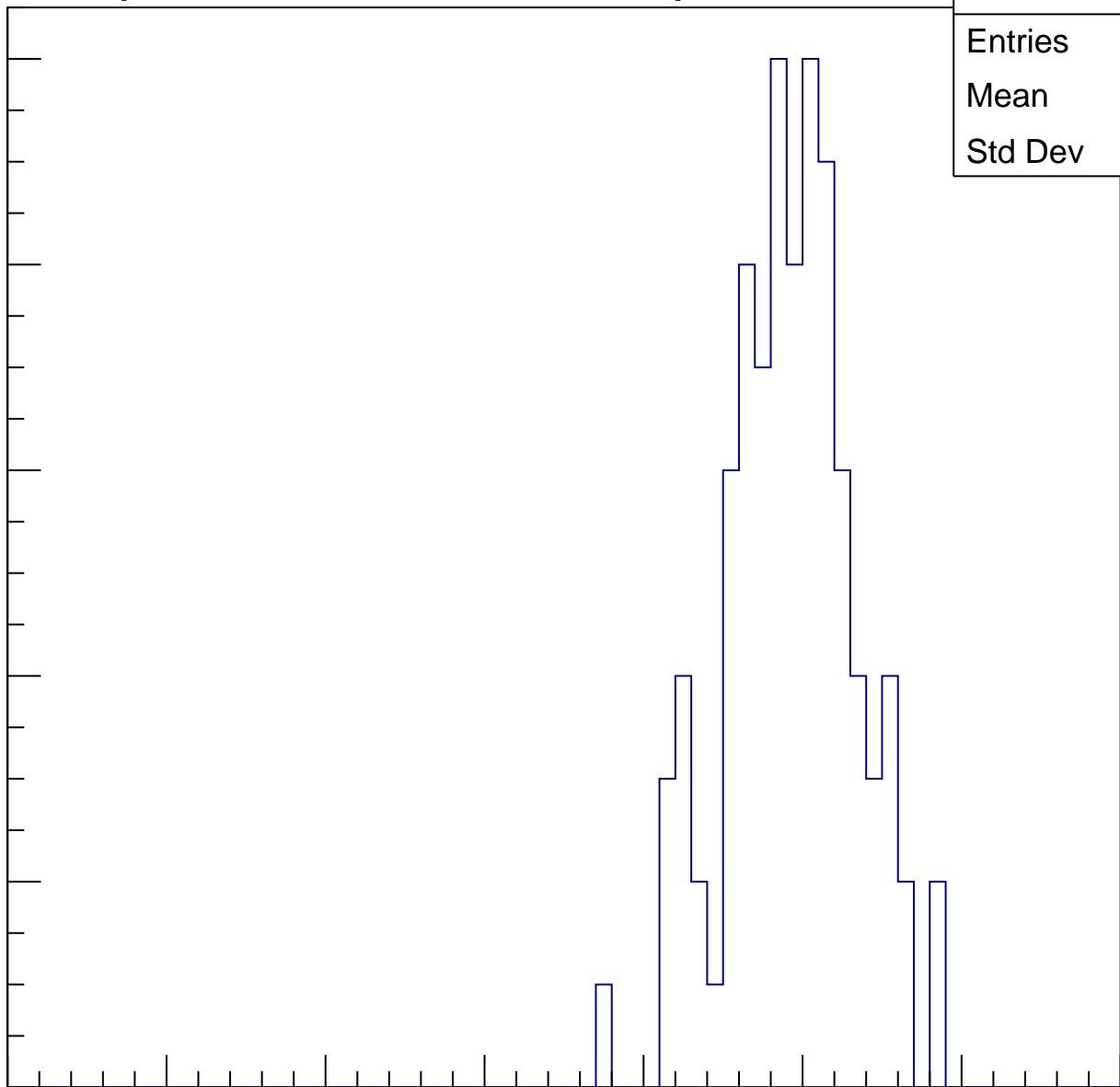
Entries	90
Mean	48.78
Std Dev	4.046

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

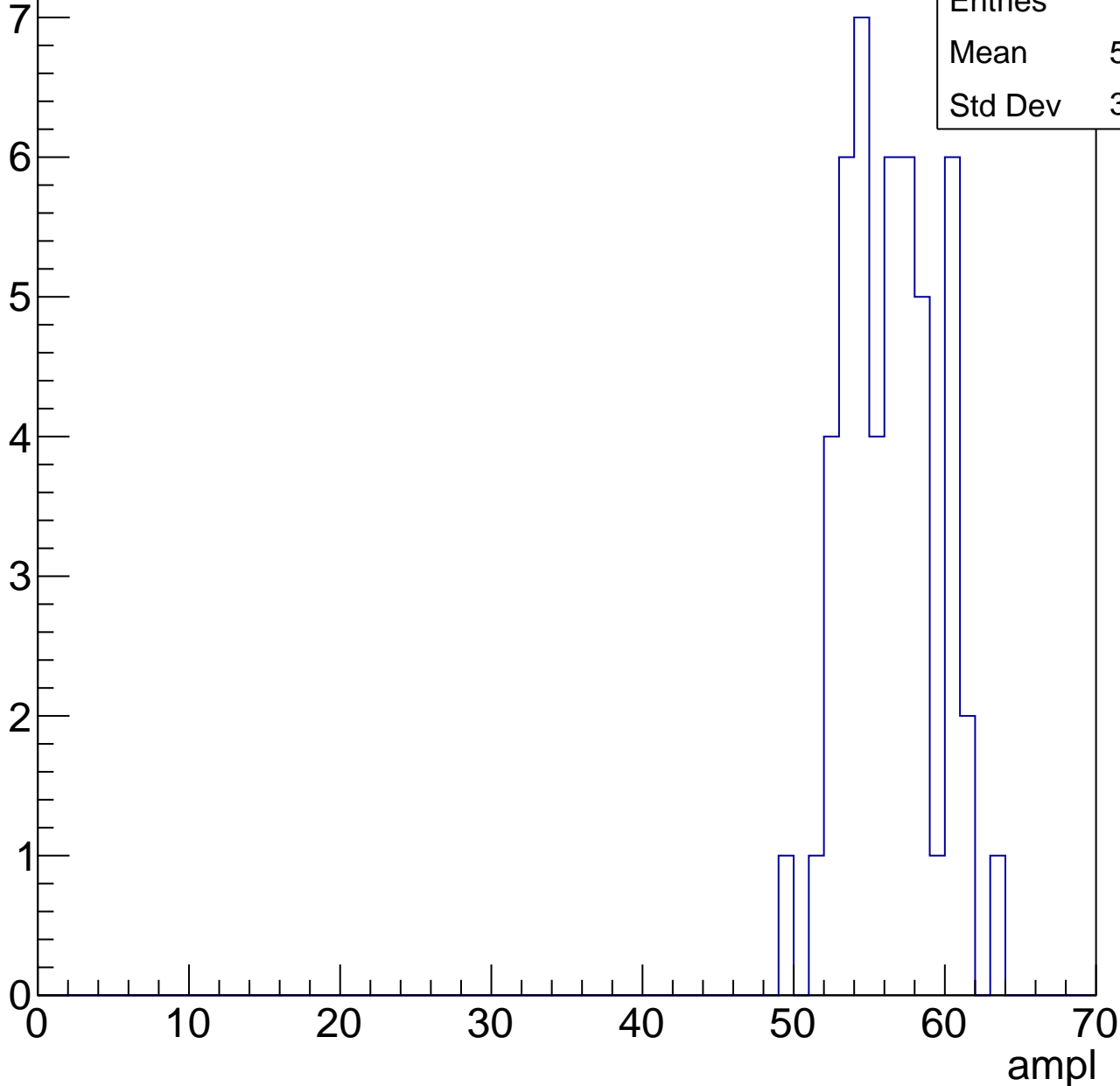


# B1L101S, U19-ch105, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

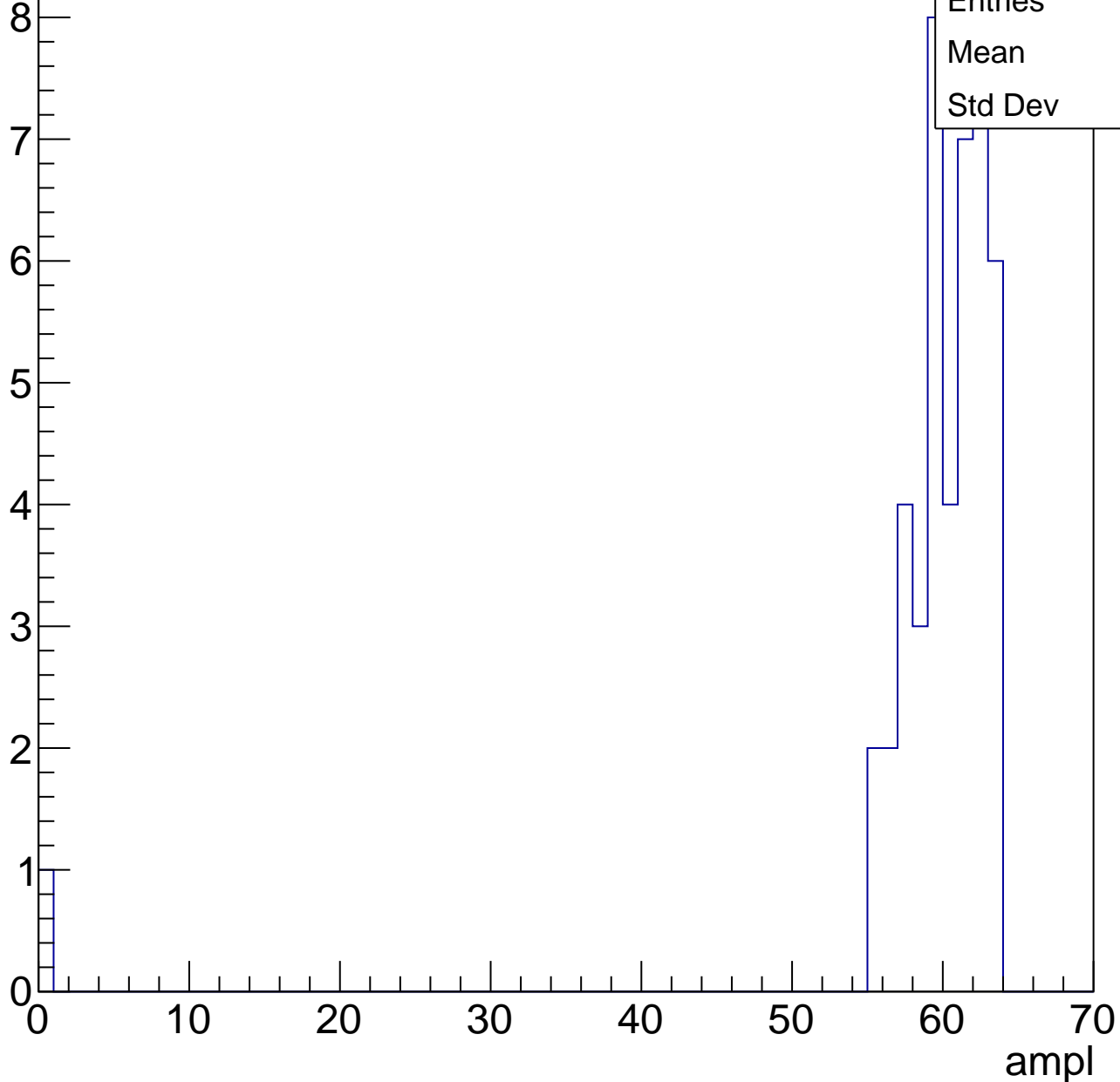
Entries	50
Mean	55.92
Std Dev	3.012



# B1L101S, U19-ch105, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U19-ch105, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U19-ch105, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U19-ch106, adc0

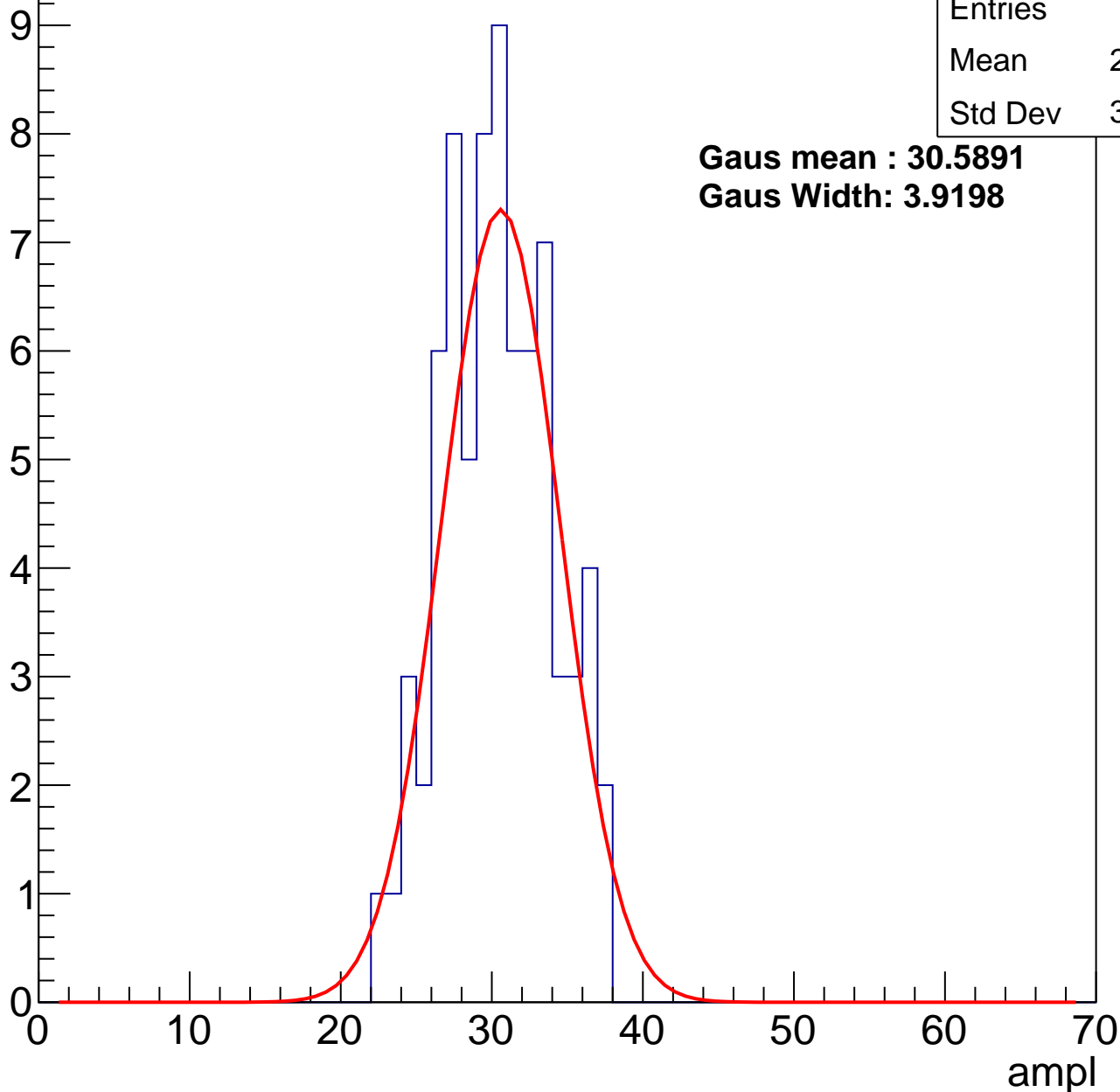
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	74
Mean	29.93
Std Dev	3.535

**Gaus mean : 30.5891**

**Gaus Width: 3.9198**



# B1L101S, U19-ch106, adc1

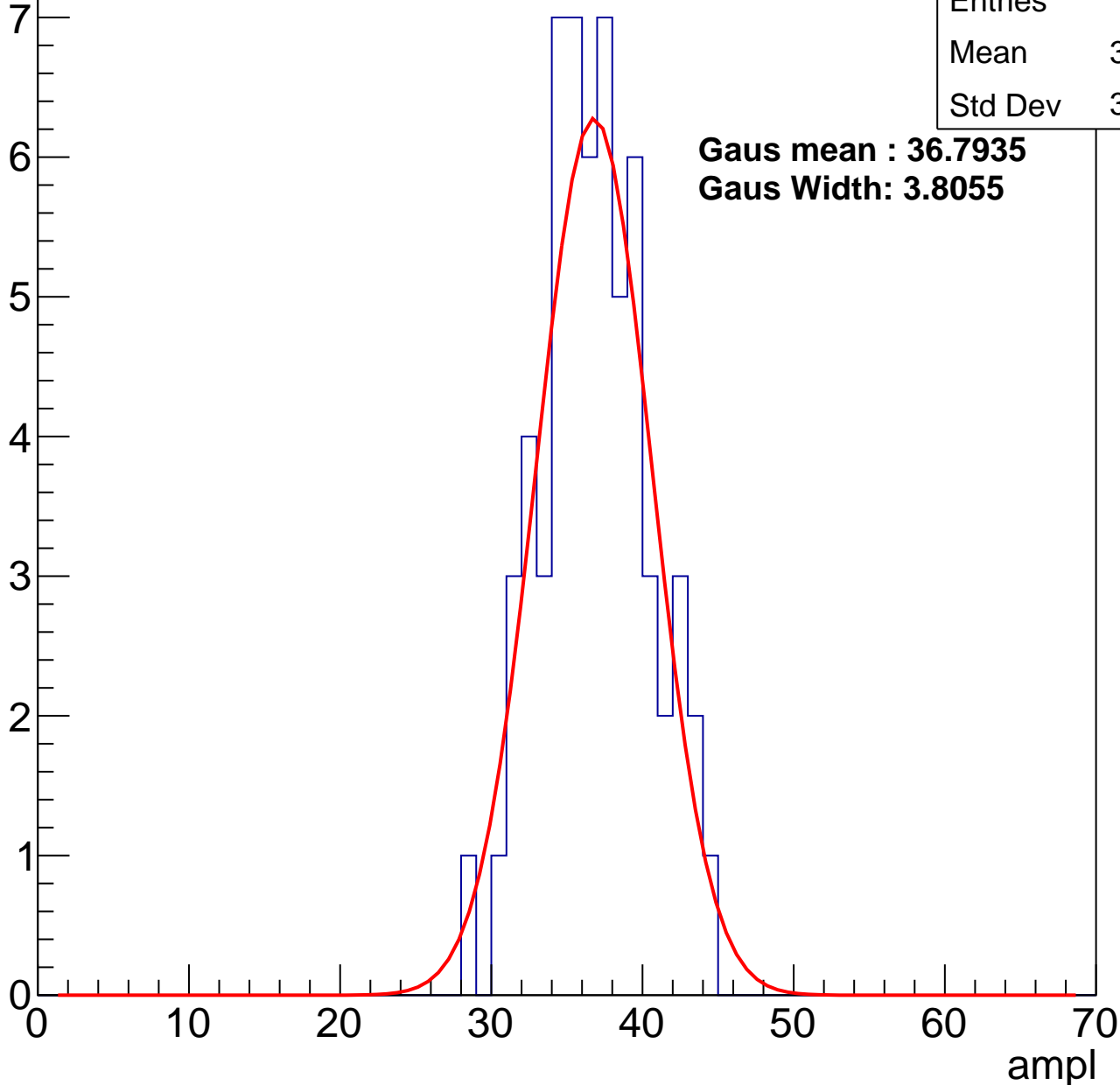
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	36.36
Std Dev	3.488

**Gaus mean : 36.7935**

**Gaus Width: 3.8055**



# B1L101S, U19-ch106, adc2

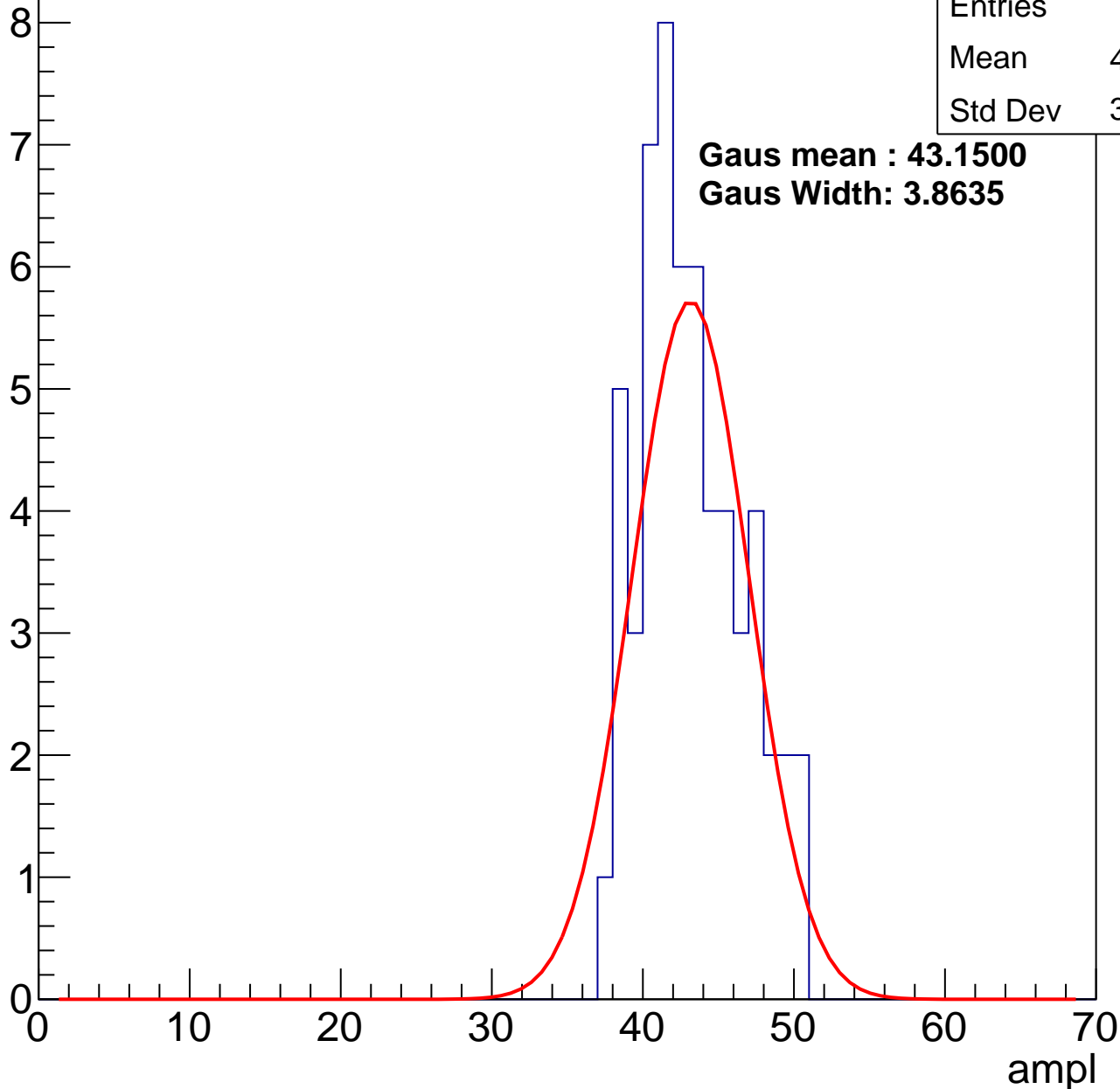
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	57
Mean	42.77
Std Dev	3.346

**Gaus mean : 43.1500**

**Gaus Width: 3.8635**

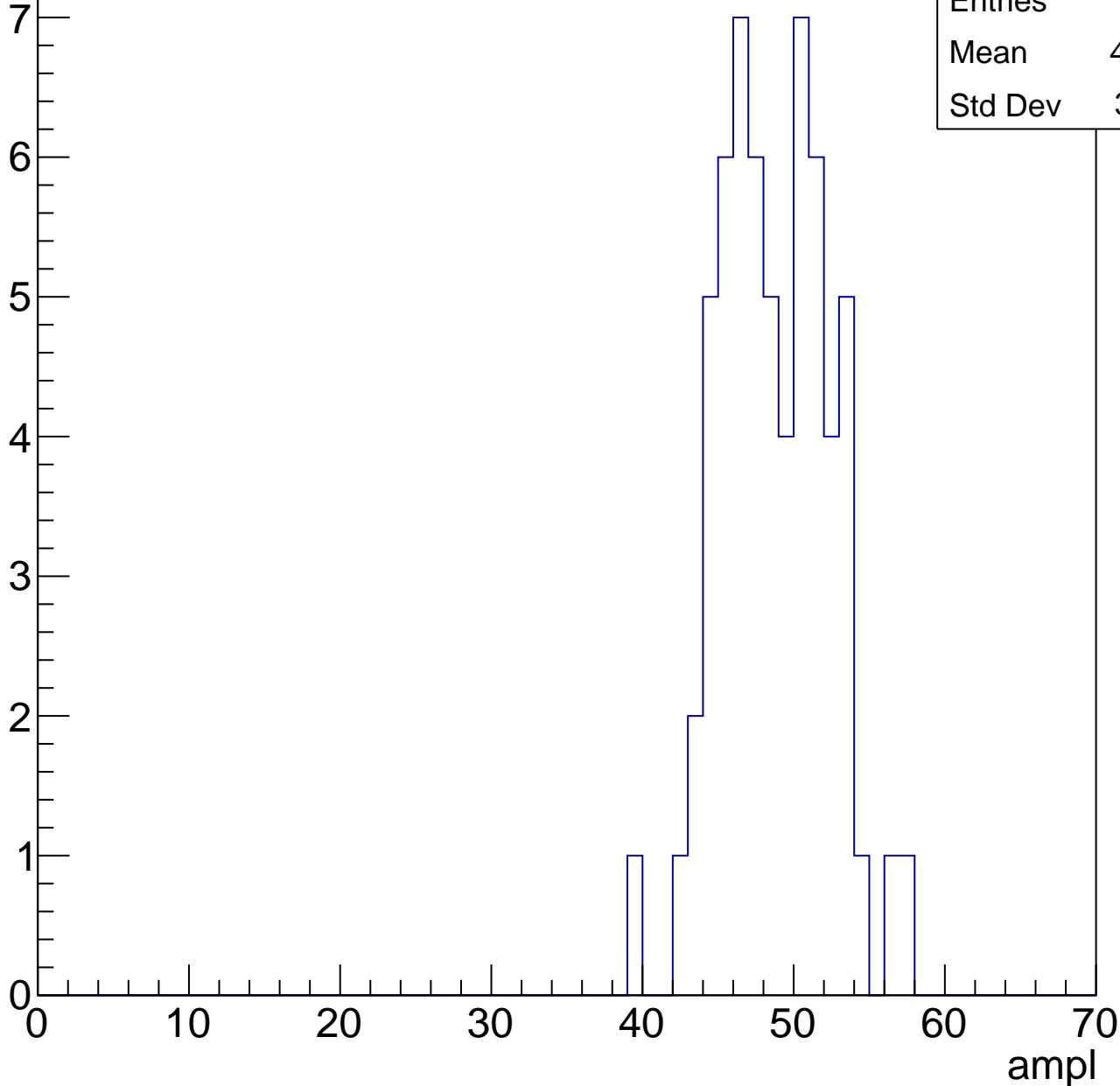


# B1L101S, U19-ch106, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	48.27
Std Dev	3.561

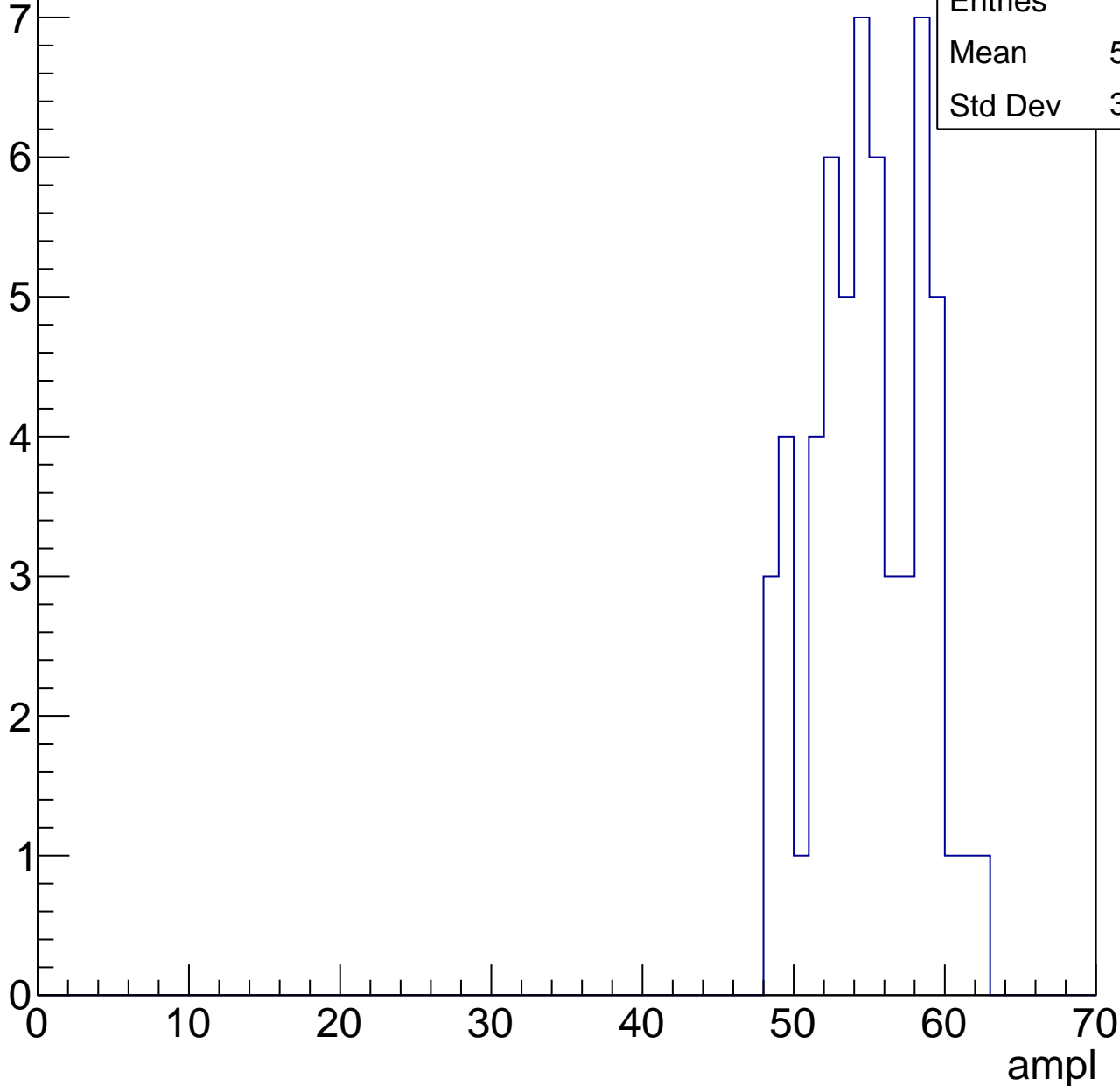


# B1L101S, U19-ch106, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	57
Mean	54.42
Std Dev	3.529

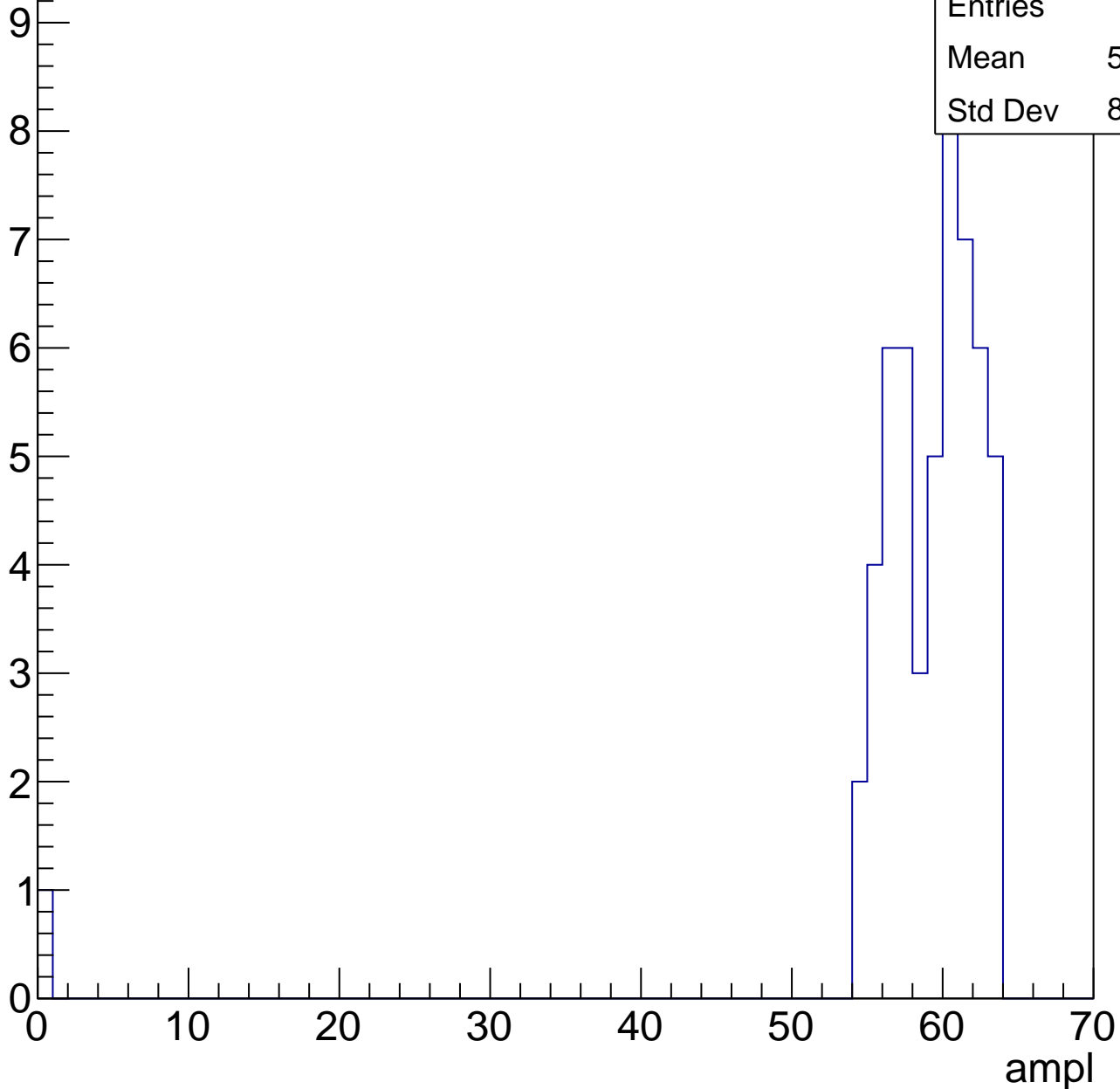


# B1L101S, U19-ch106, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	54
Mean	57.94
Std Dev	8.374

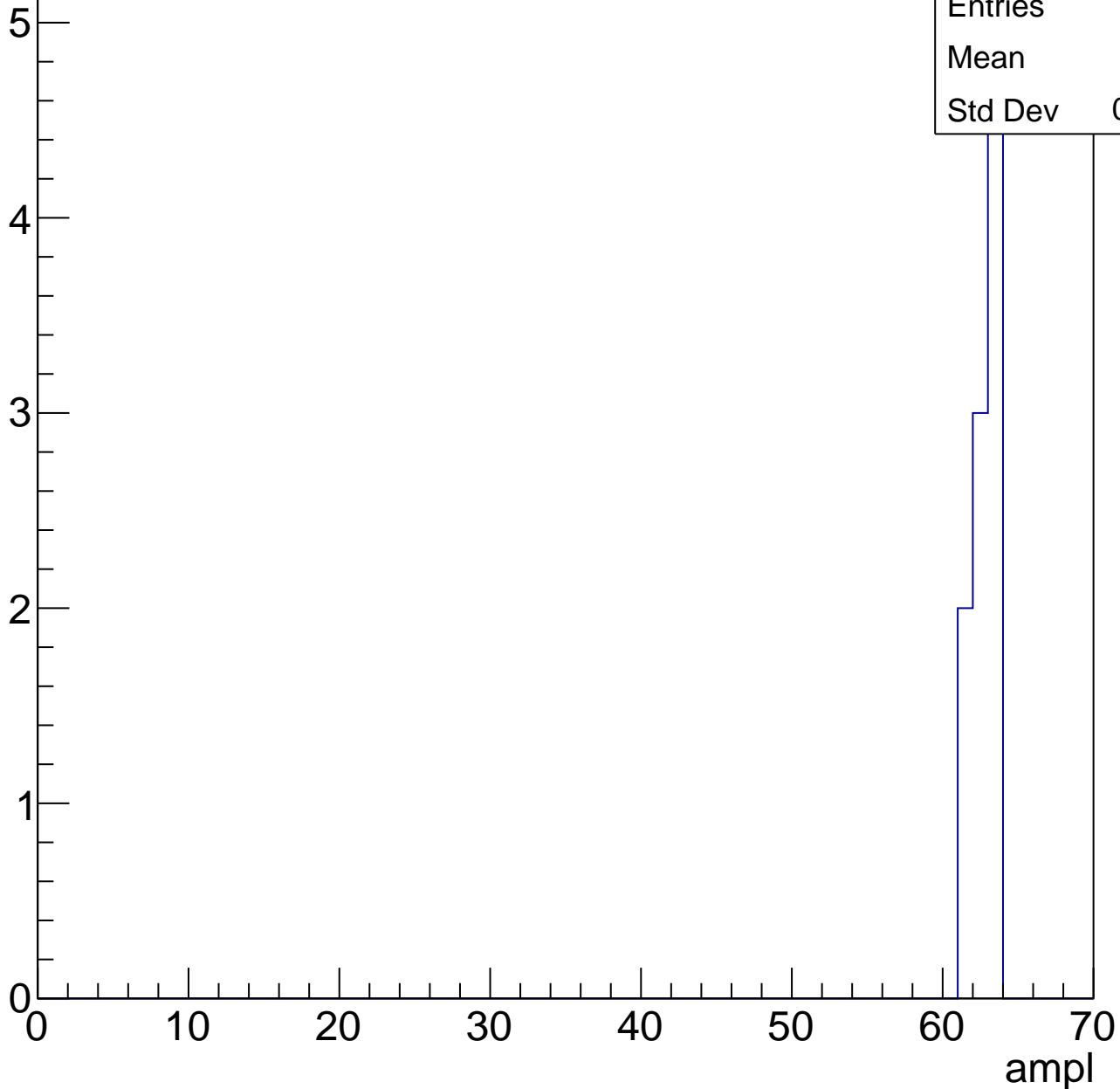


# B1L101S, U19-ch106, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	10
Mean	62.3
Std Dev	0.781





# B1L101S, U19-ch106, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U19-ch107, adc0

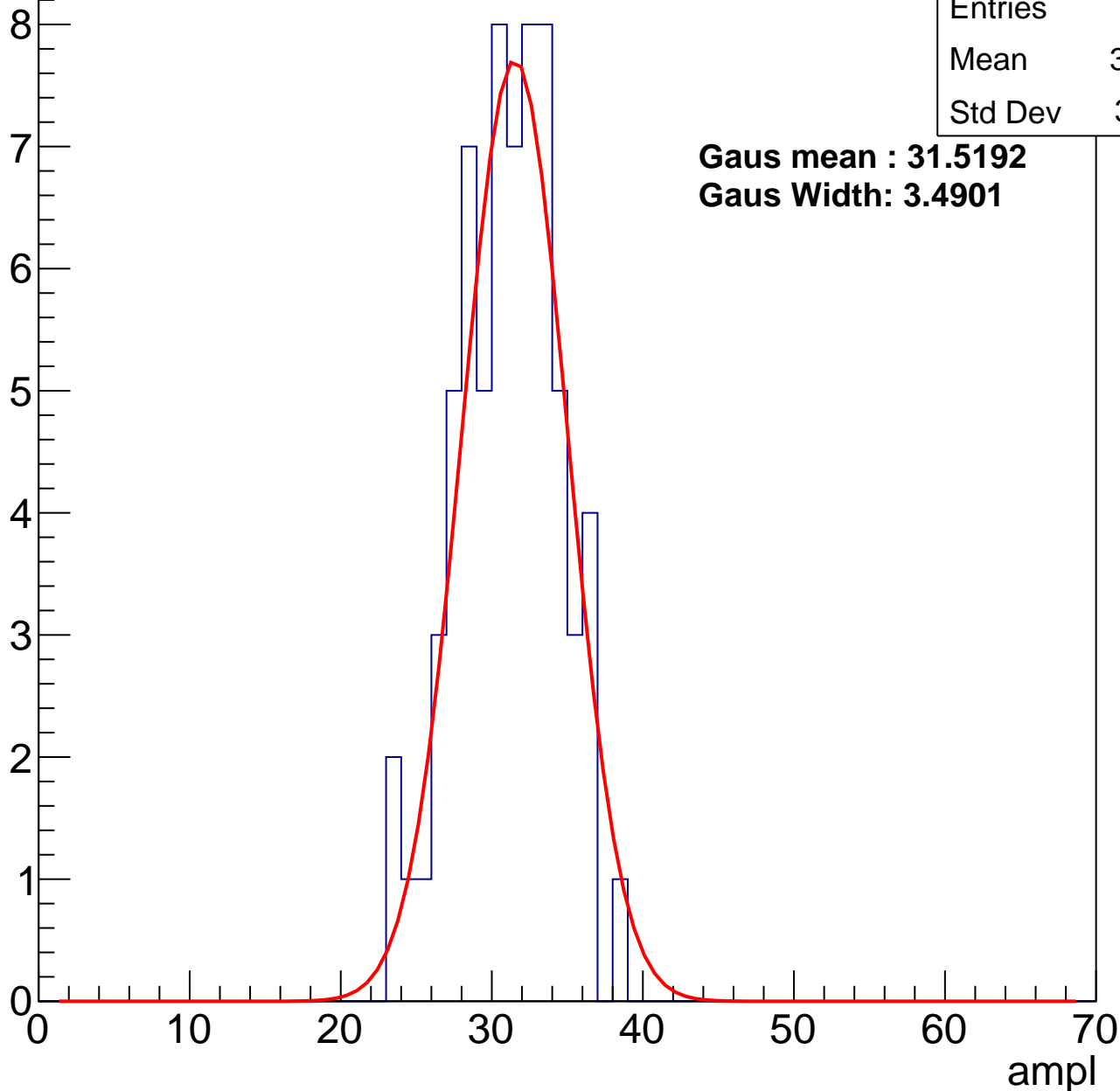
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	30.63
Std Dev	3.281

**Gaus mean : 31.5192**

**Gaus Width: 3.4901**



# B1L101S, U19-ch107, adc1

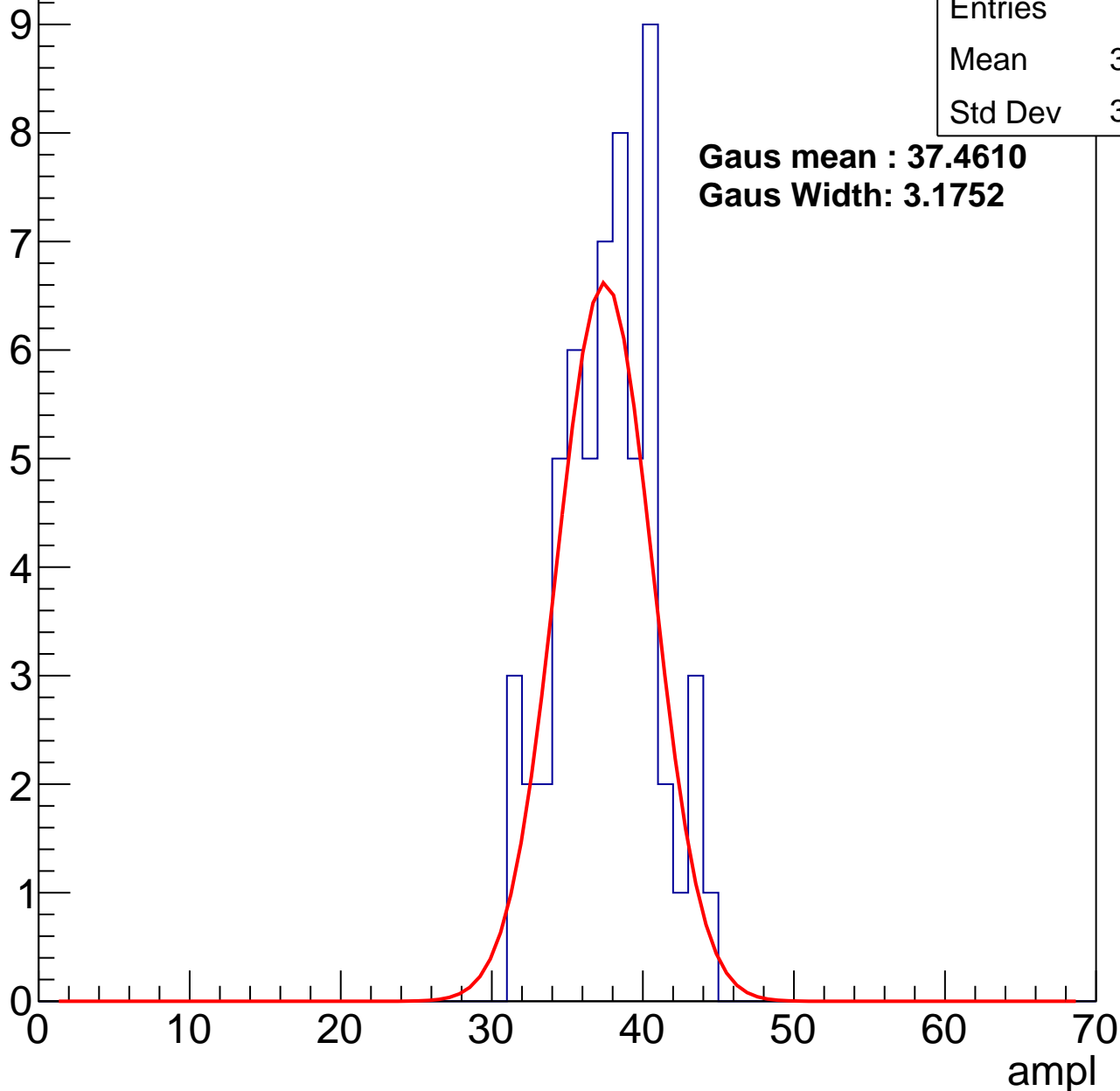
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	59
Mean	37.25
Std Dev	3.144

**Gaus mean : 37.4610**

**Gaus Width: 3.1752**



# B1L101S, U19-ch107, adc2

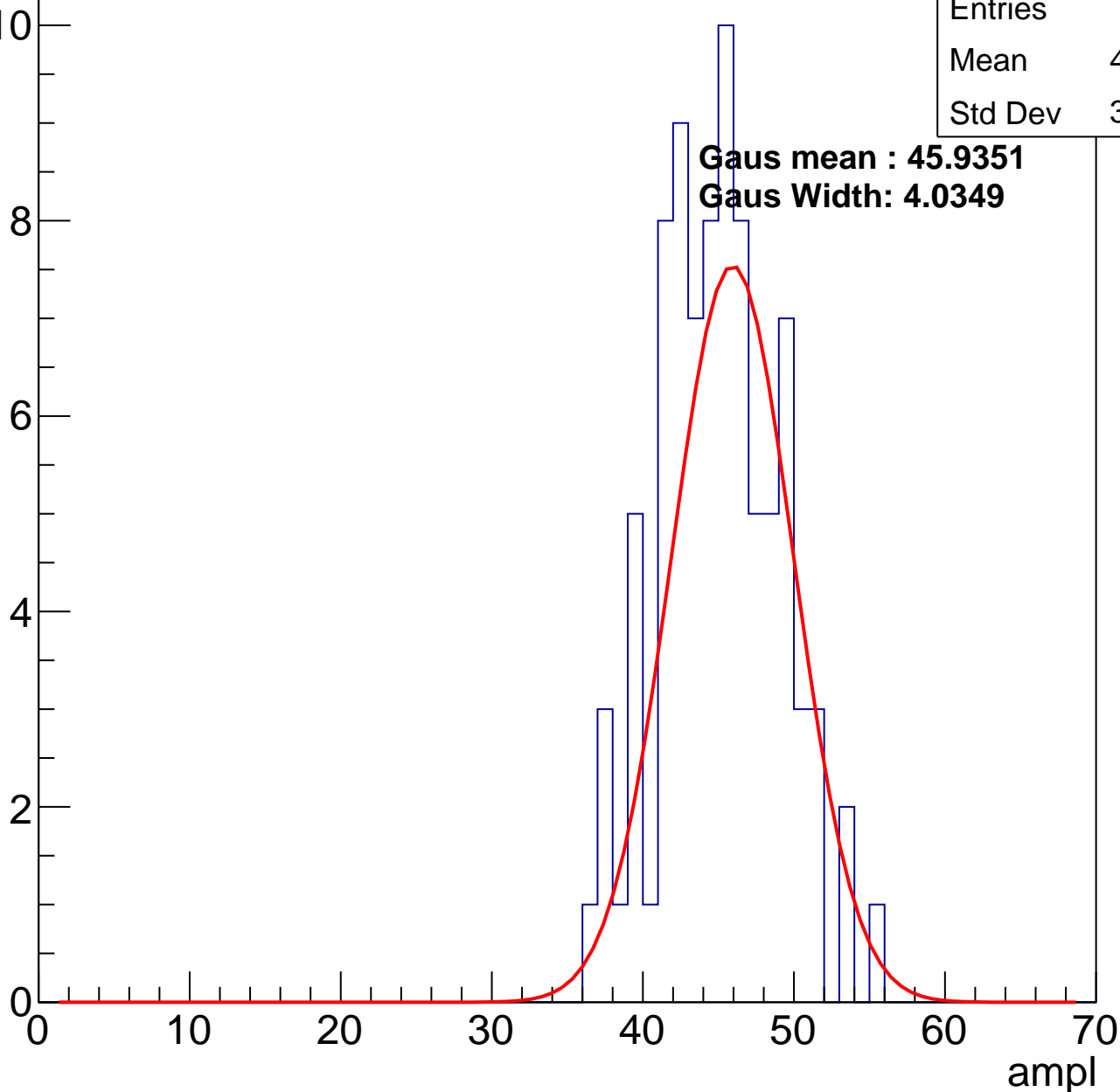
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	87
Mean	44.59
Std Dev	3.944

**Gaus mean : 45.9351**

**Gaus Width: 4.0349**

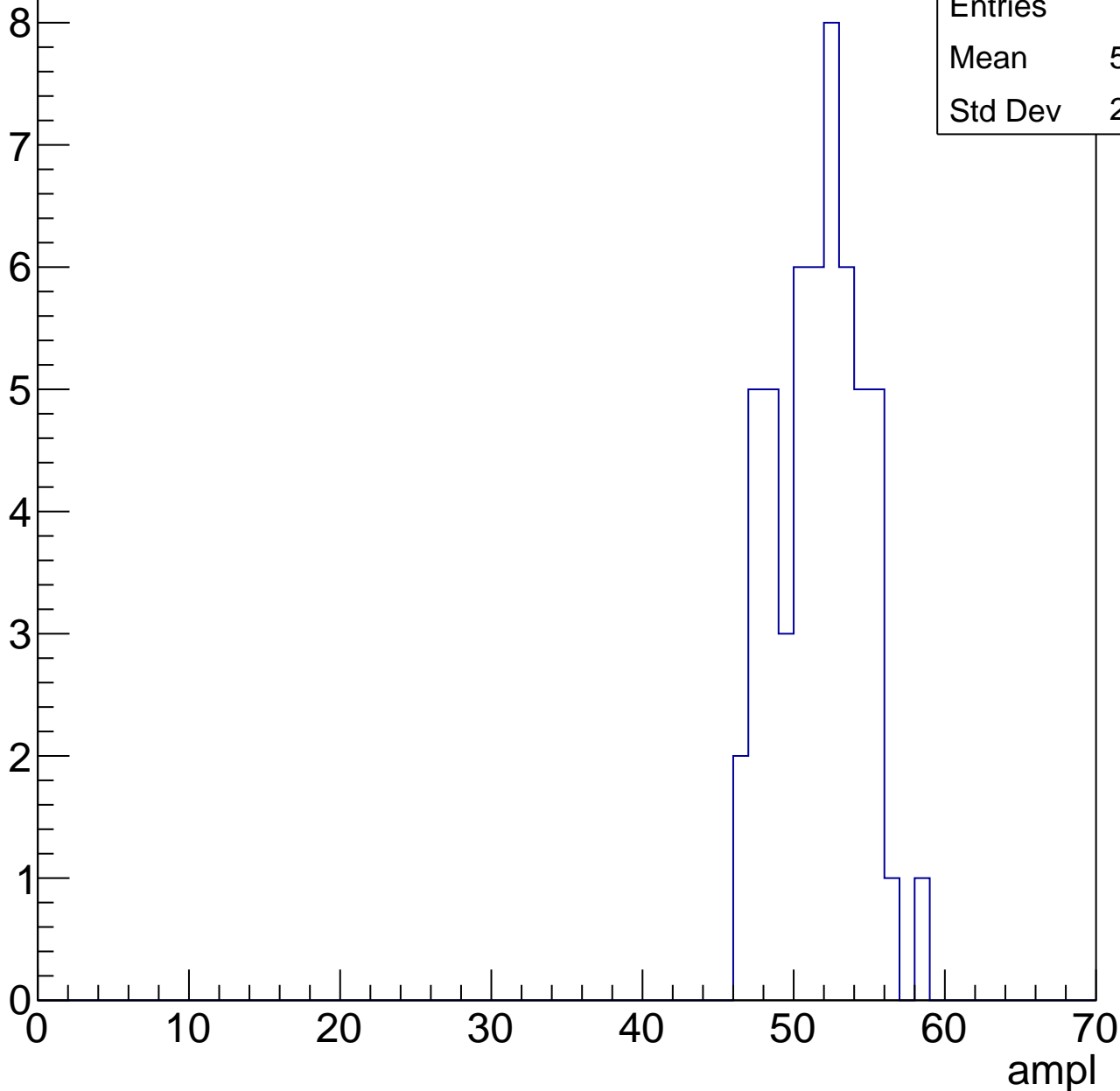


# B1L101S, U19-ch107, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	53
Mean	51.19
Std Dev	2.822

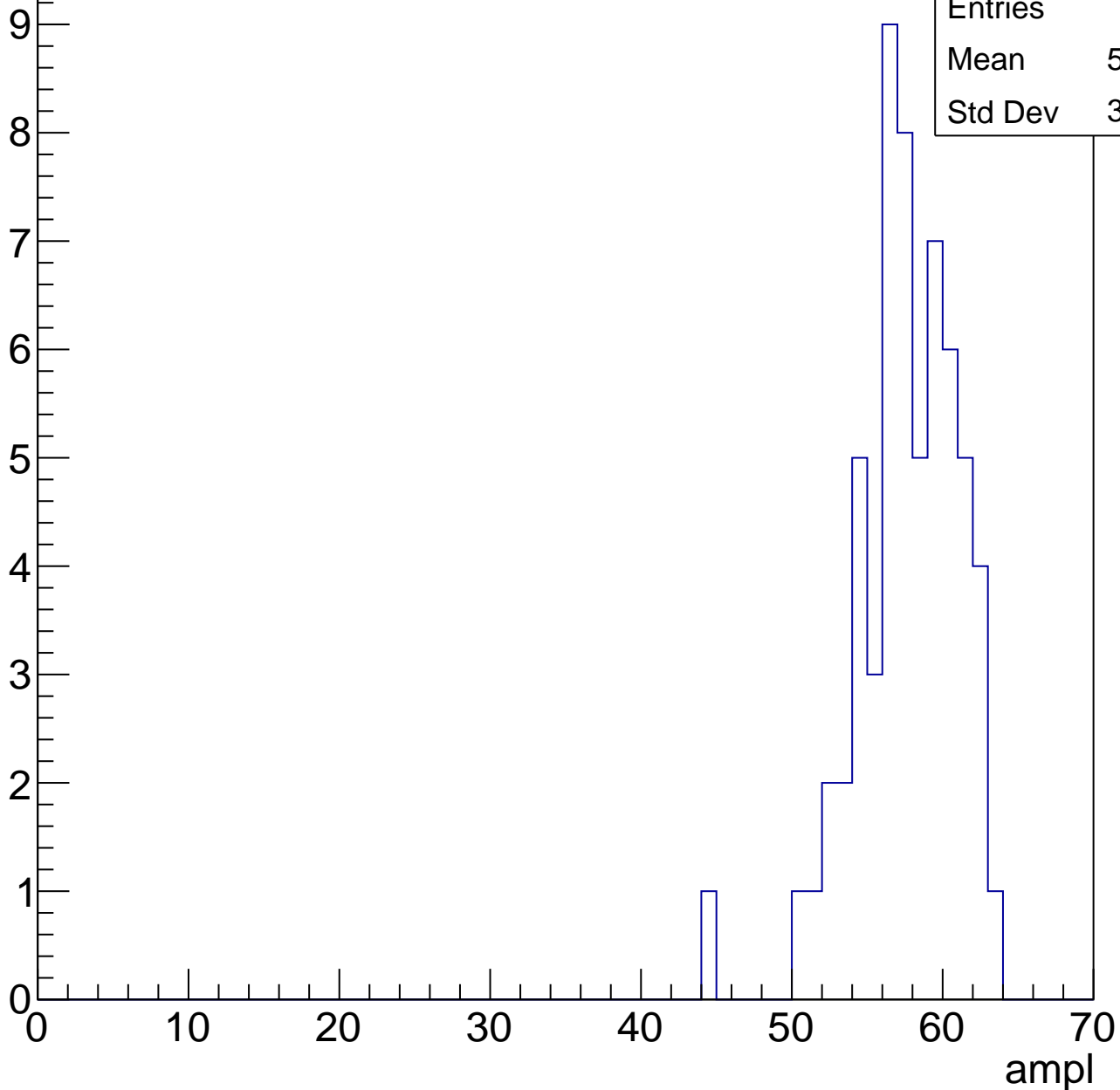


# B1L101S, U19-ch107, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	60
Mean	57.15
Std Dev	3.425

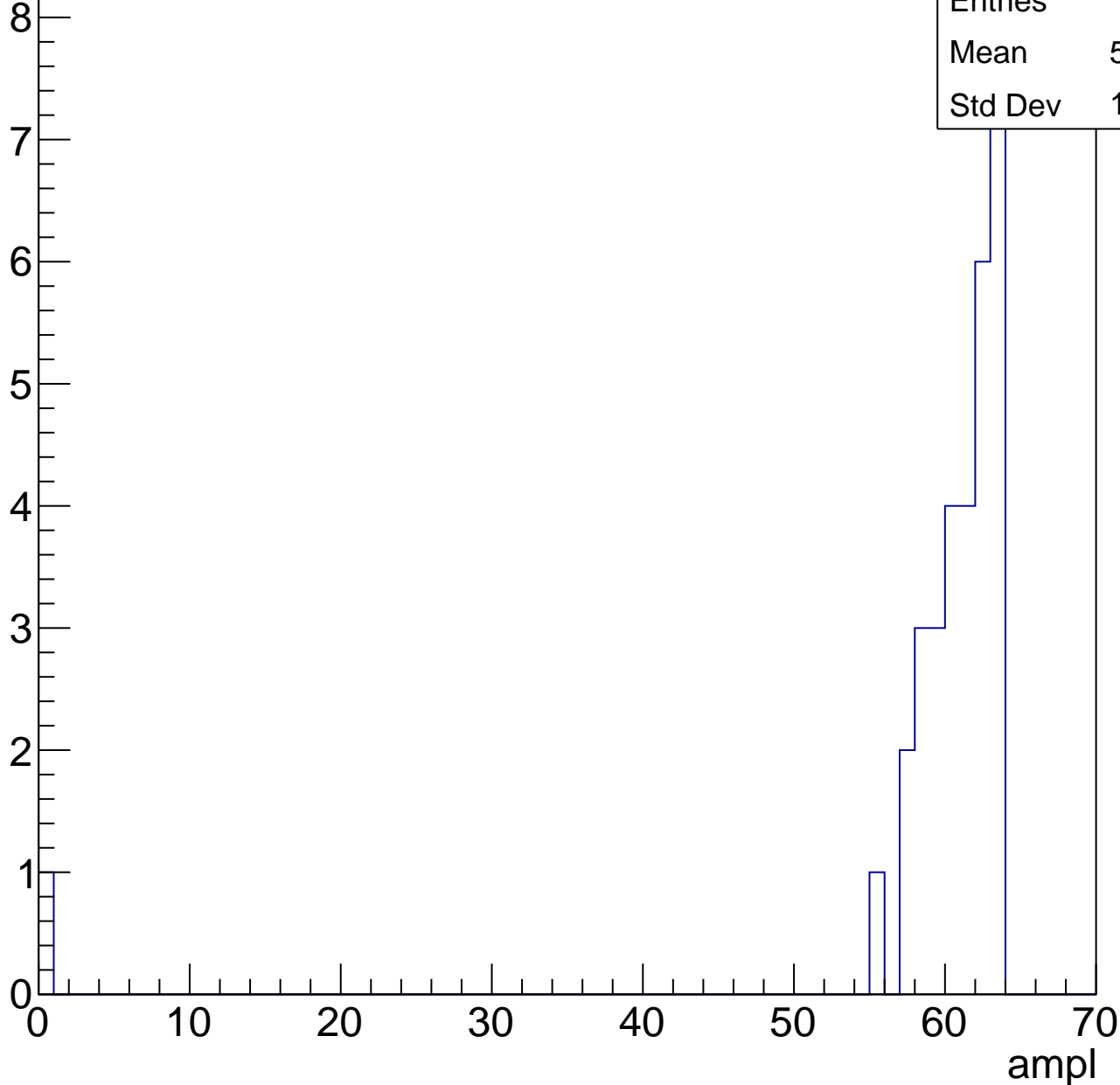


# B1L101S, U19-ch107, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

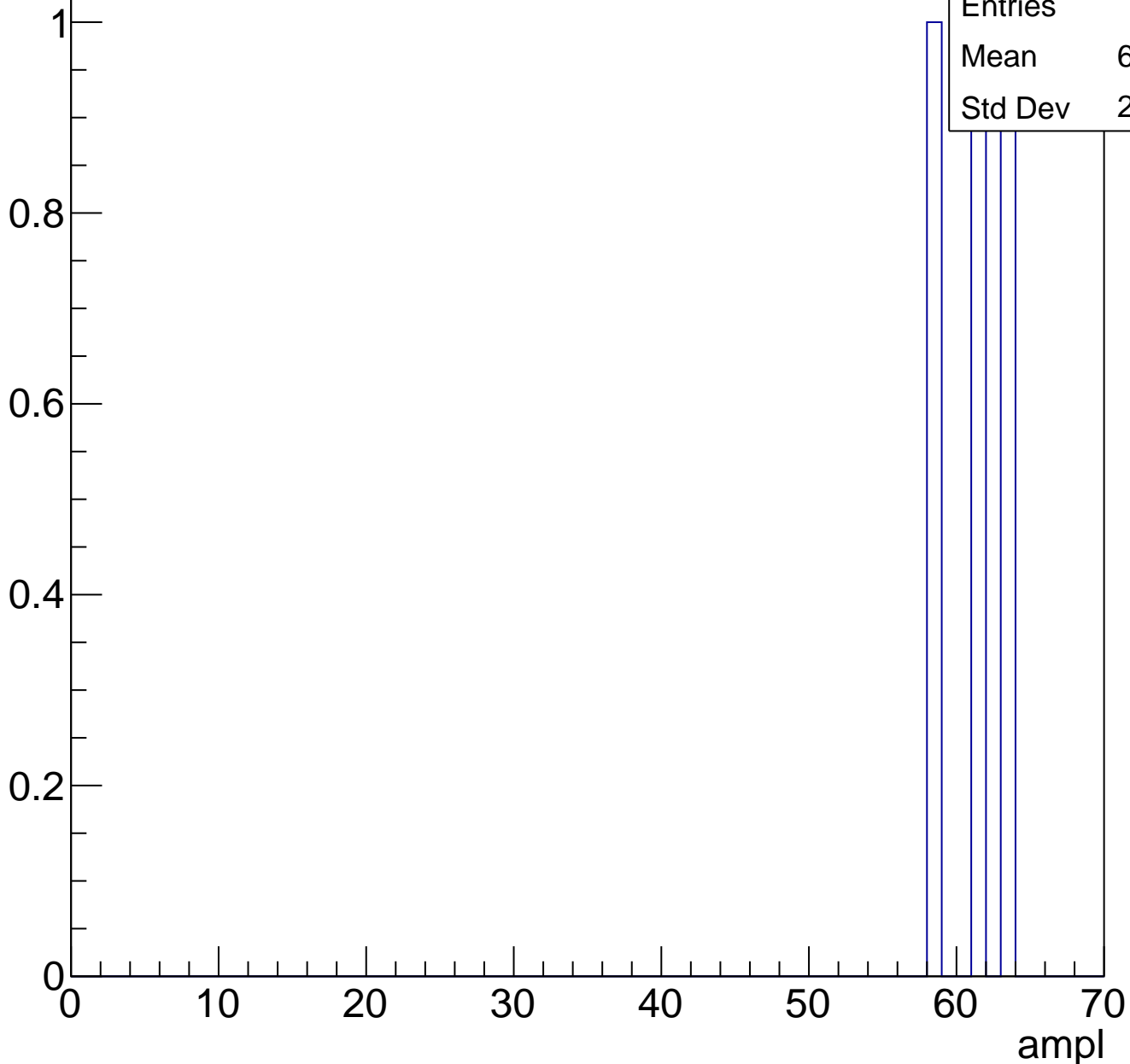
Entries	32
Mean	58.75
Std Dev	10.76



# B1L101S, U19-ch107, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U19-ch107, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L101S, U19-ch108, adc0

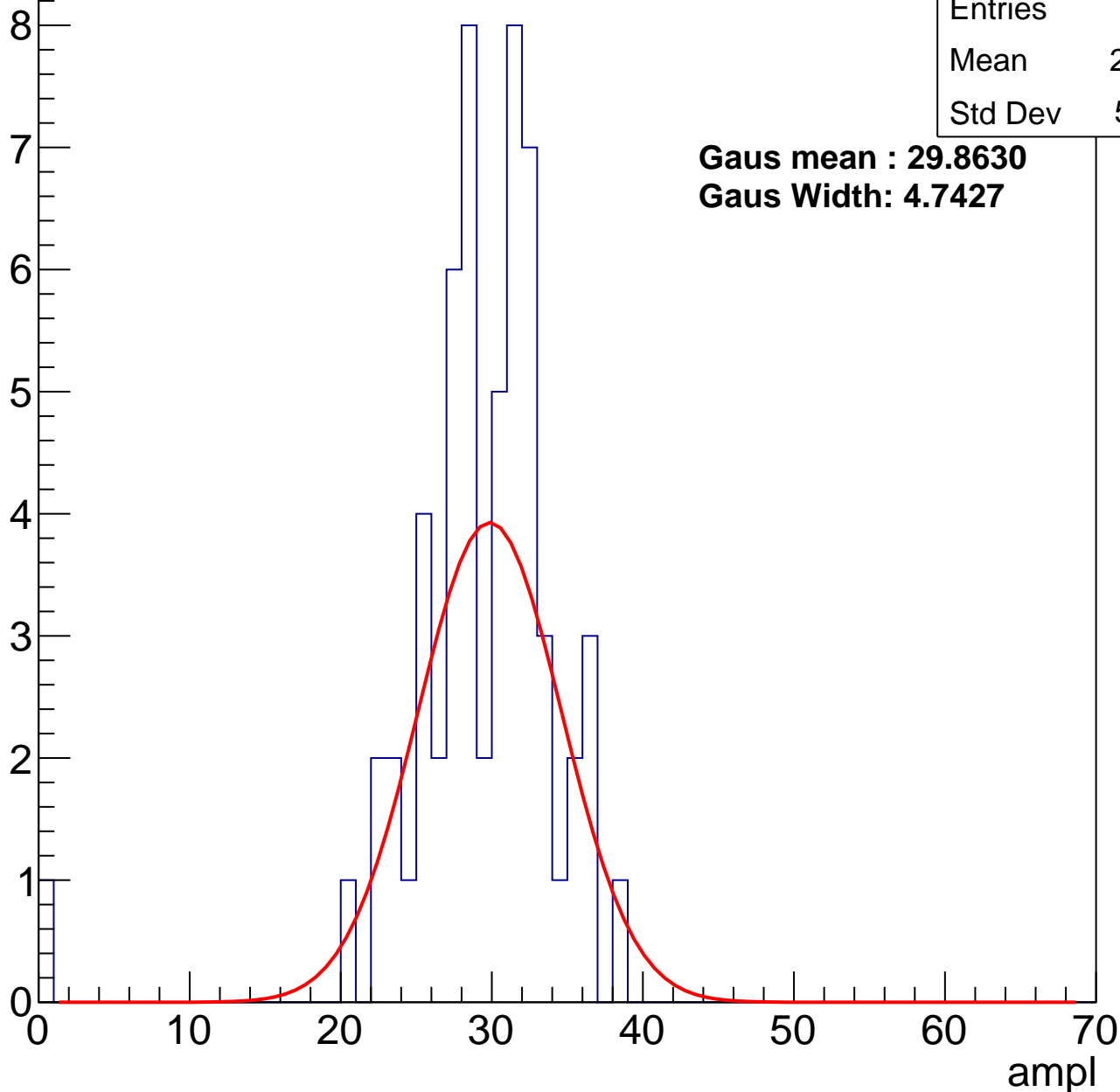
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	59
Mean	28.83
Std Dev	5.371

**Gaus mean : 29.8630**

**Gaus Width: 4.7427**



# B1L101S, U19-ch108, adc1

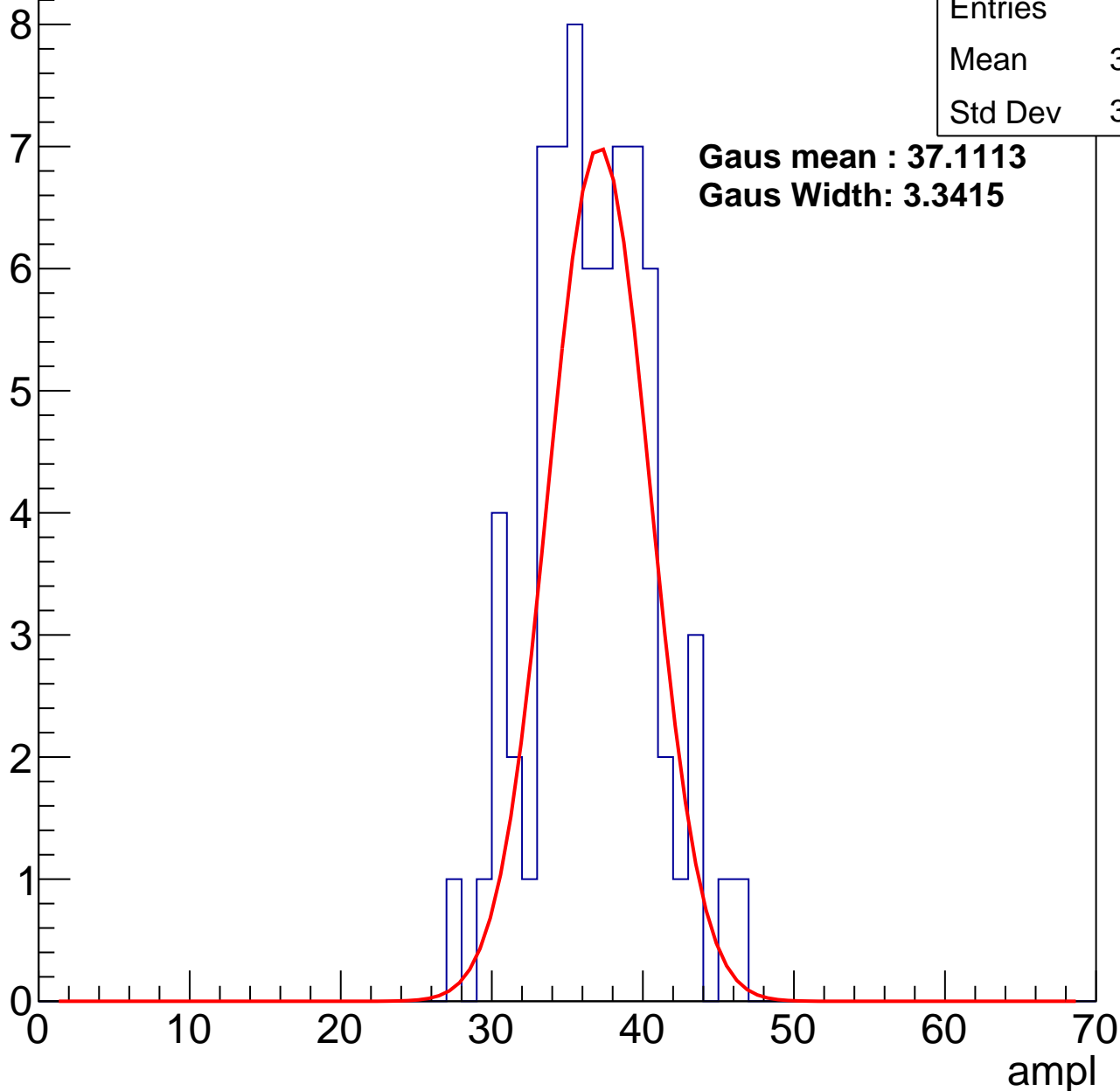
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	71
Mean	36.34
Std Dev	3.823

**Gaus mean : 37.1113**

**Gaus Width: 3.3415**



# B1L101S, U19-ch108, adc2

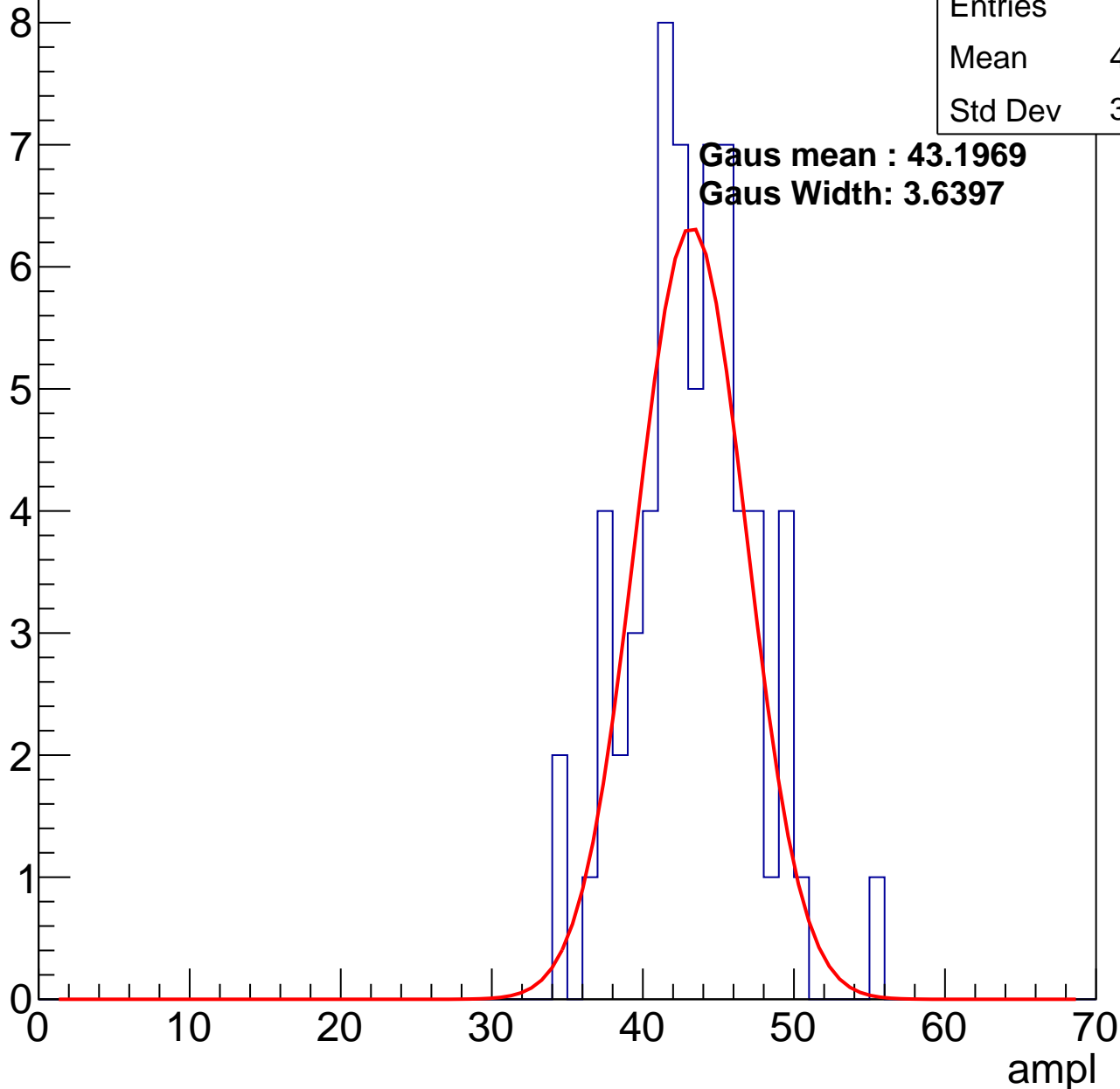
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	42.86
Std Dev	3.969

**Gaus mean : 43.1969**

**Gaus Width: 3.6397**

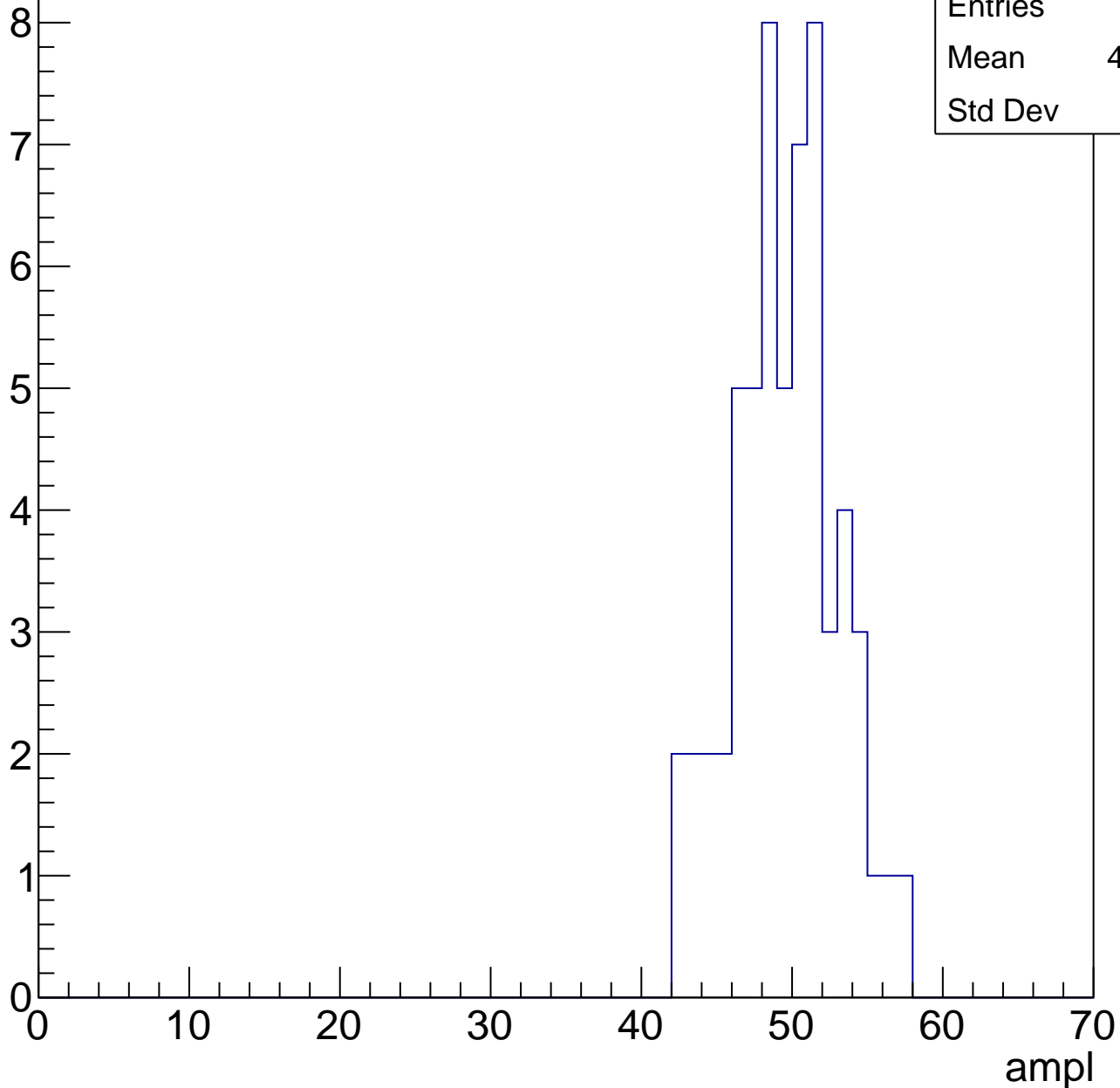


# B1L101S, U19-ch108, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	59
Mean	49.12
Std Dev	3.39

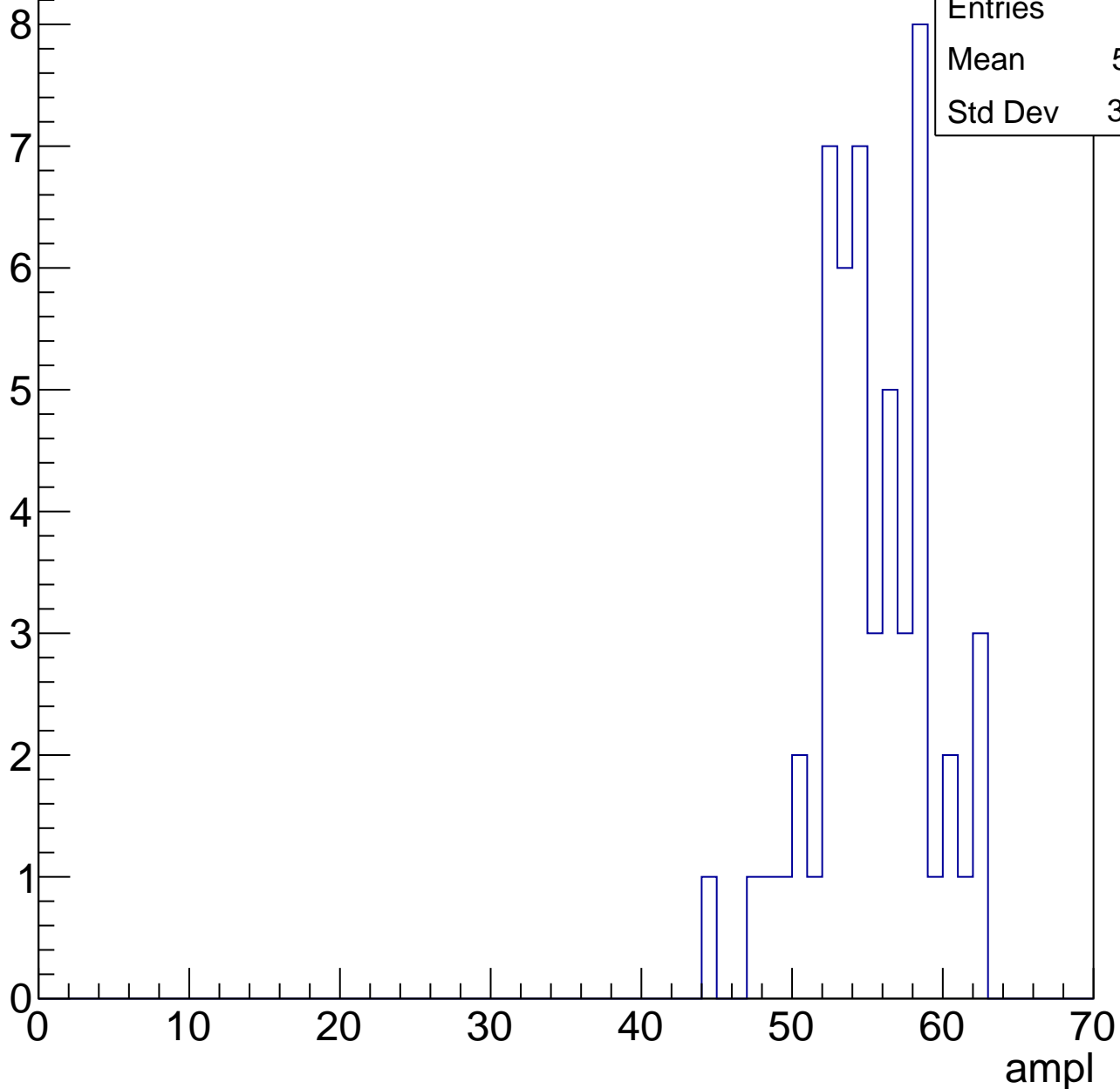


# B1L101S, U19-ch108, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	53
Mean	54.81
Std Dev	3.802

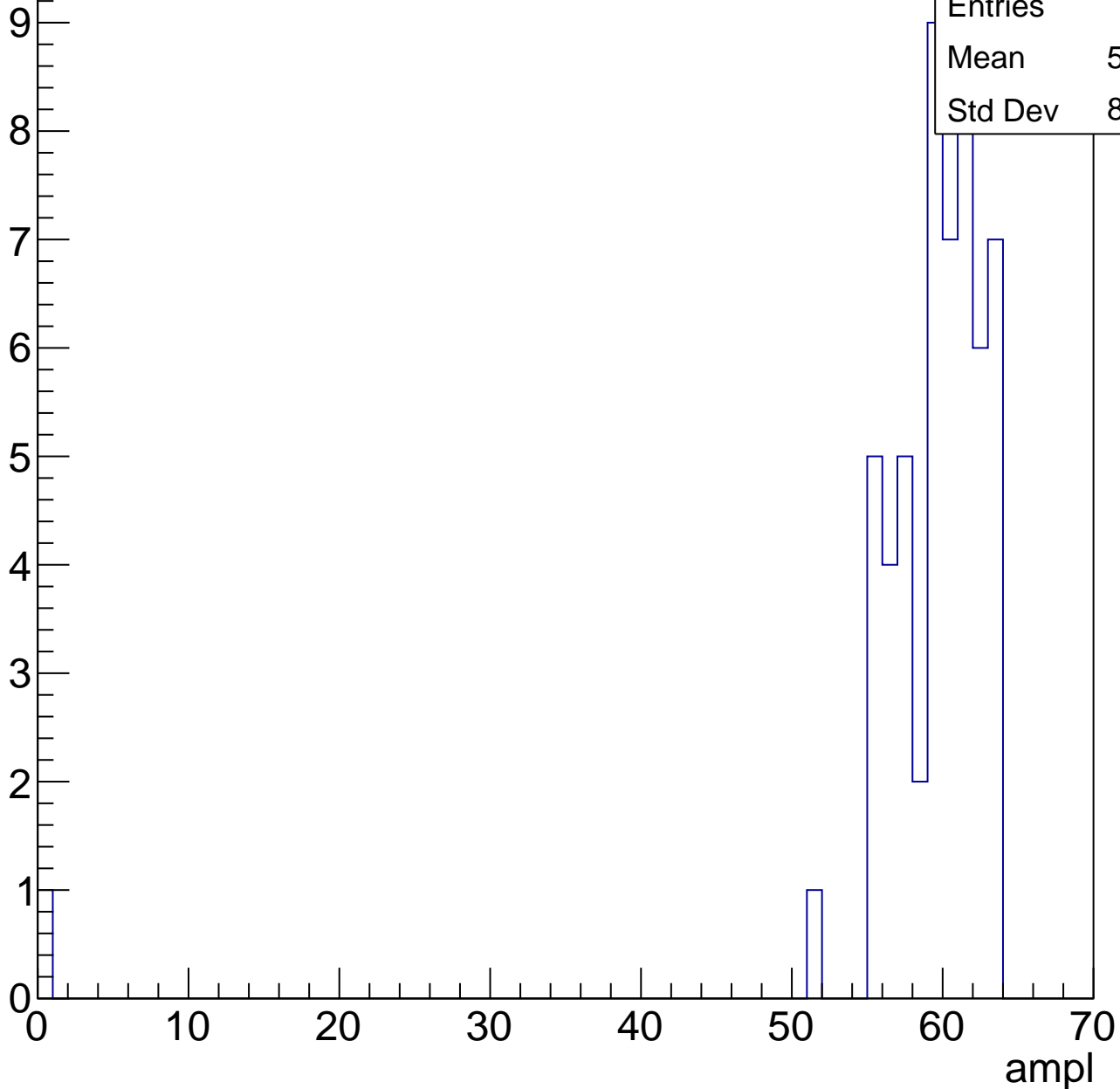


# B1L101S, U19-ch108, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

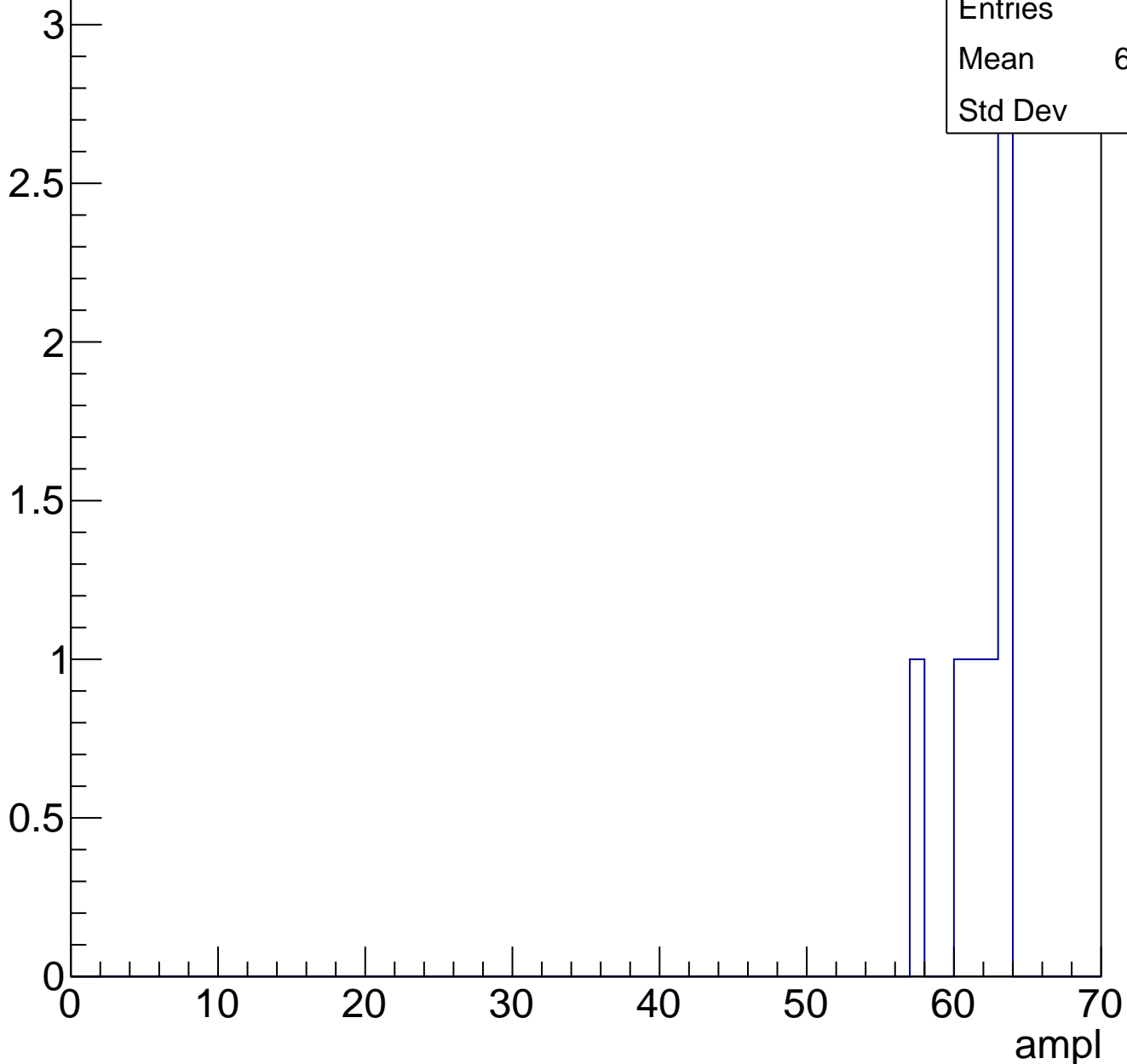
Entries	55
Mean	58.24
Std Dev	8.373



# B1L101S, U19-ch108, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U19-ch108, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U19-ch109, adc0

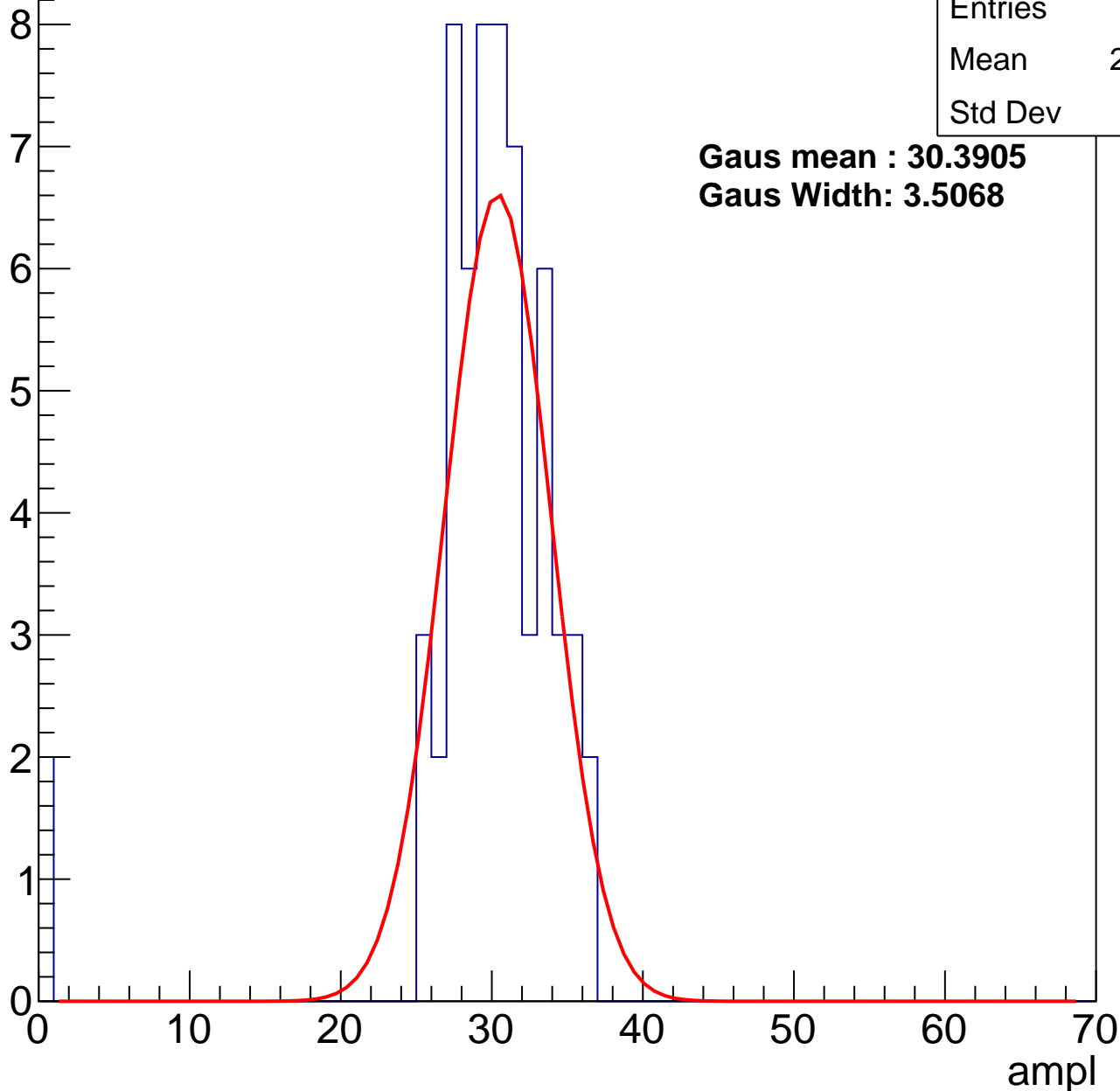
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	29.07
Std Dev	6.04

**Gaus mean : 30.3905**

**Gaus Width: 3.5068**



# B1L101S, U19-ch109, adc1

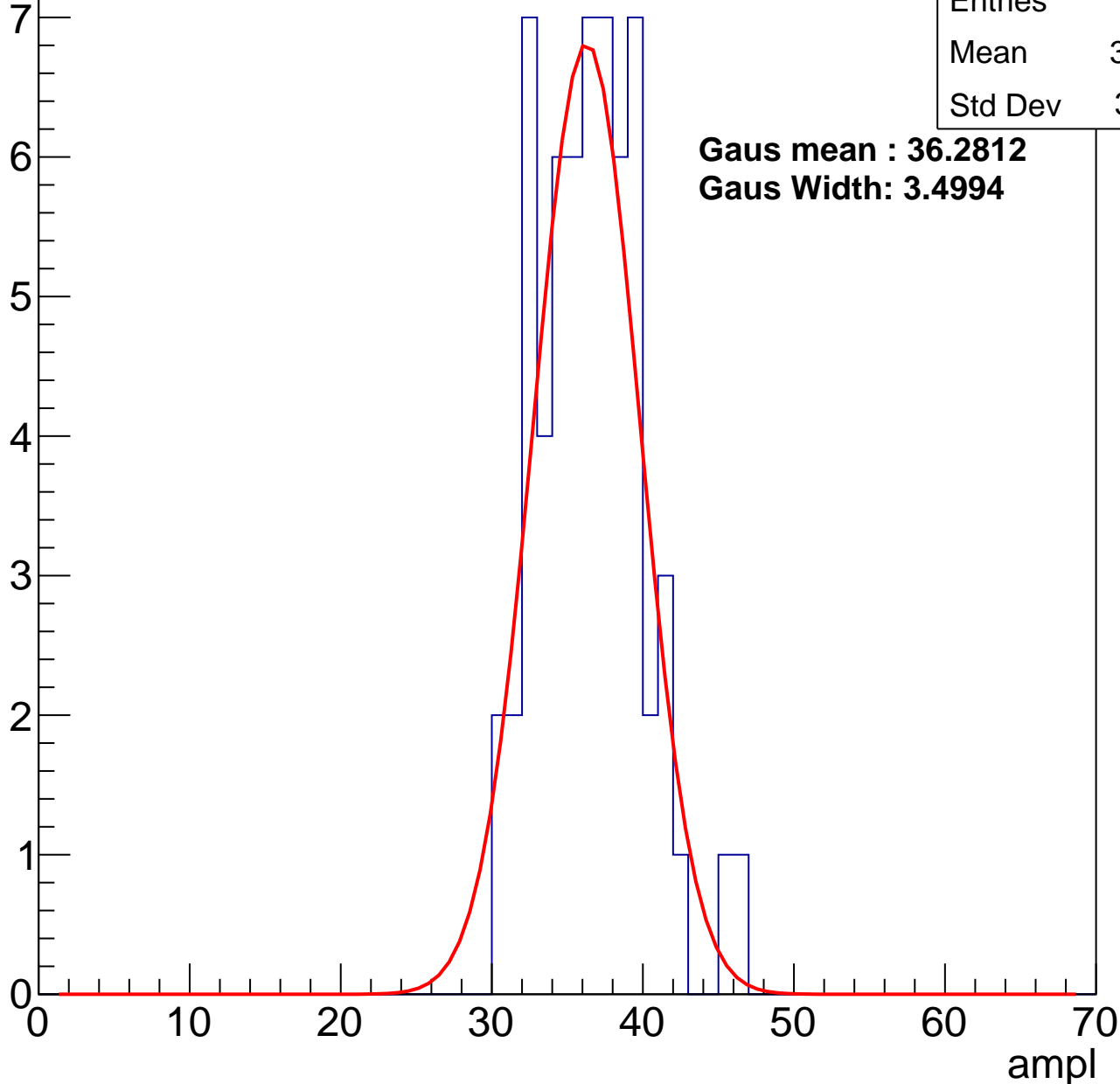
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	36.13
Std Dev	3.401

**Gaus mean : 36.2812**

**Gaus Width: 3.4994**



# B1L101S, U19-ch109, adc2

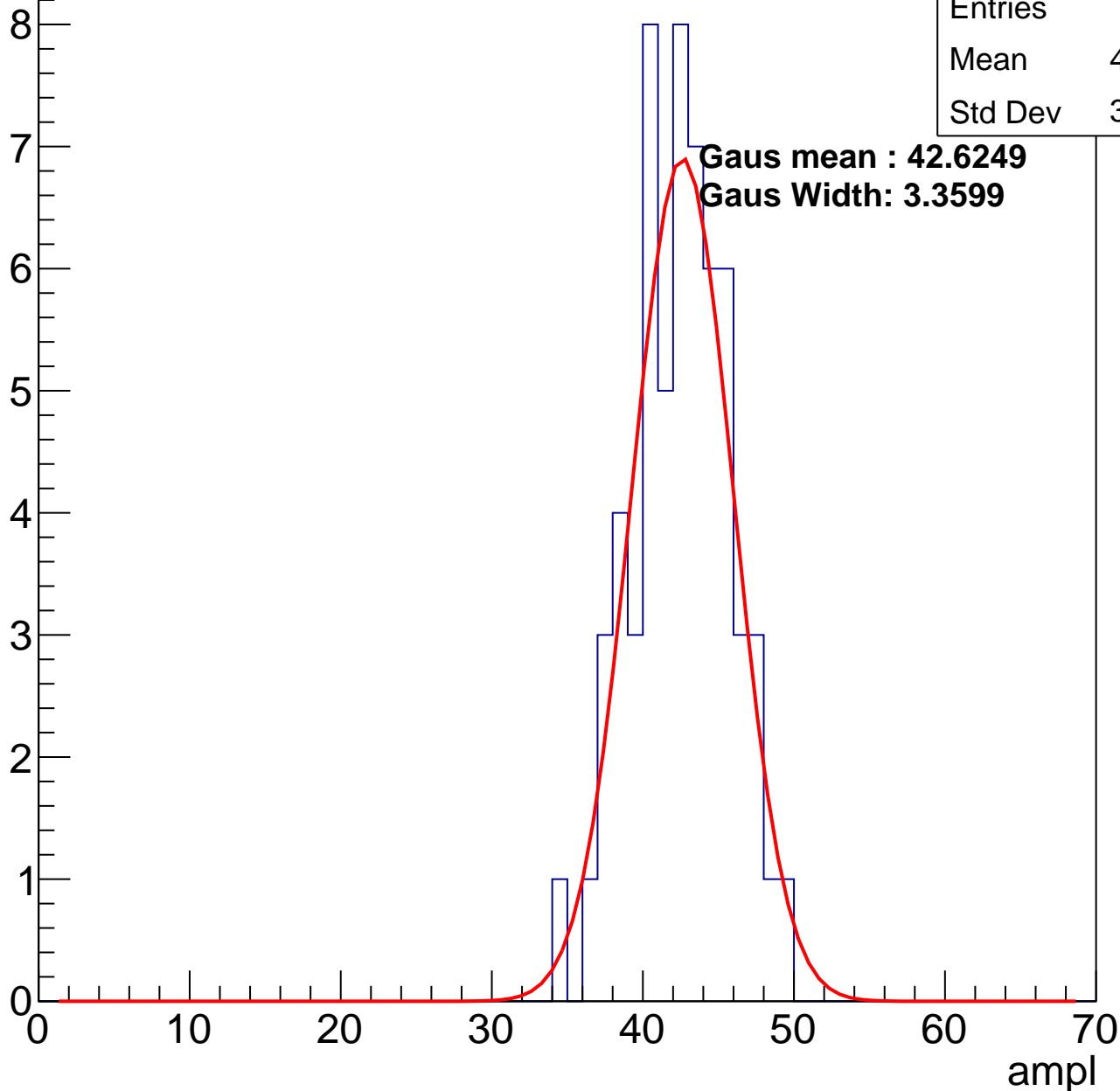
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	60
Mean	42.03
Std Dev	3.152

**Gaus mean : 42.6249**

**Gaus Width: 3.3599**

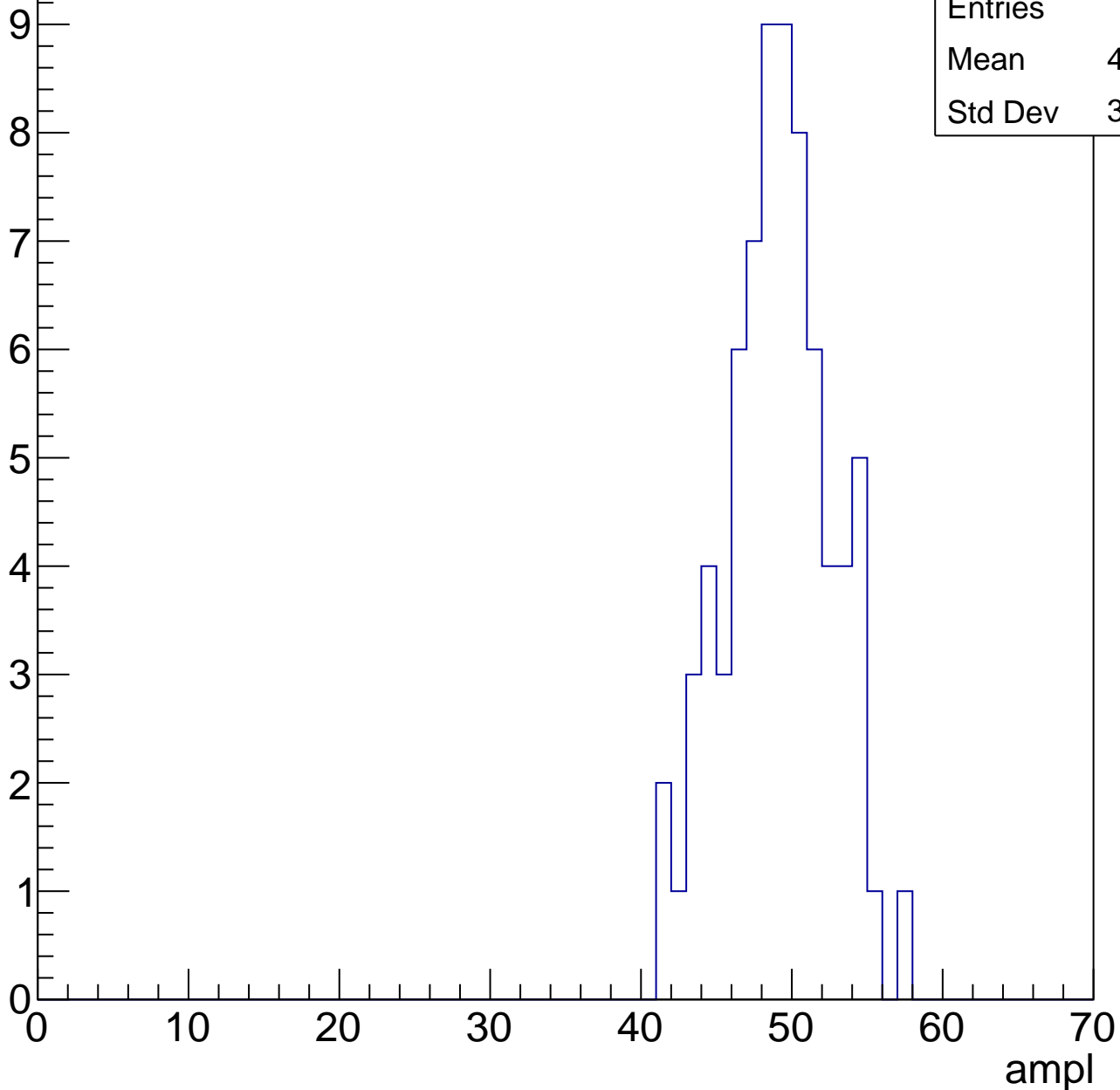


# B1L101S, U19-ch109, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

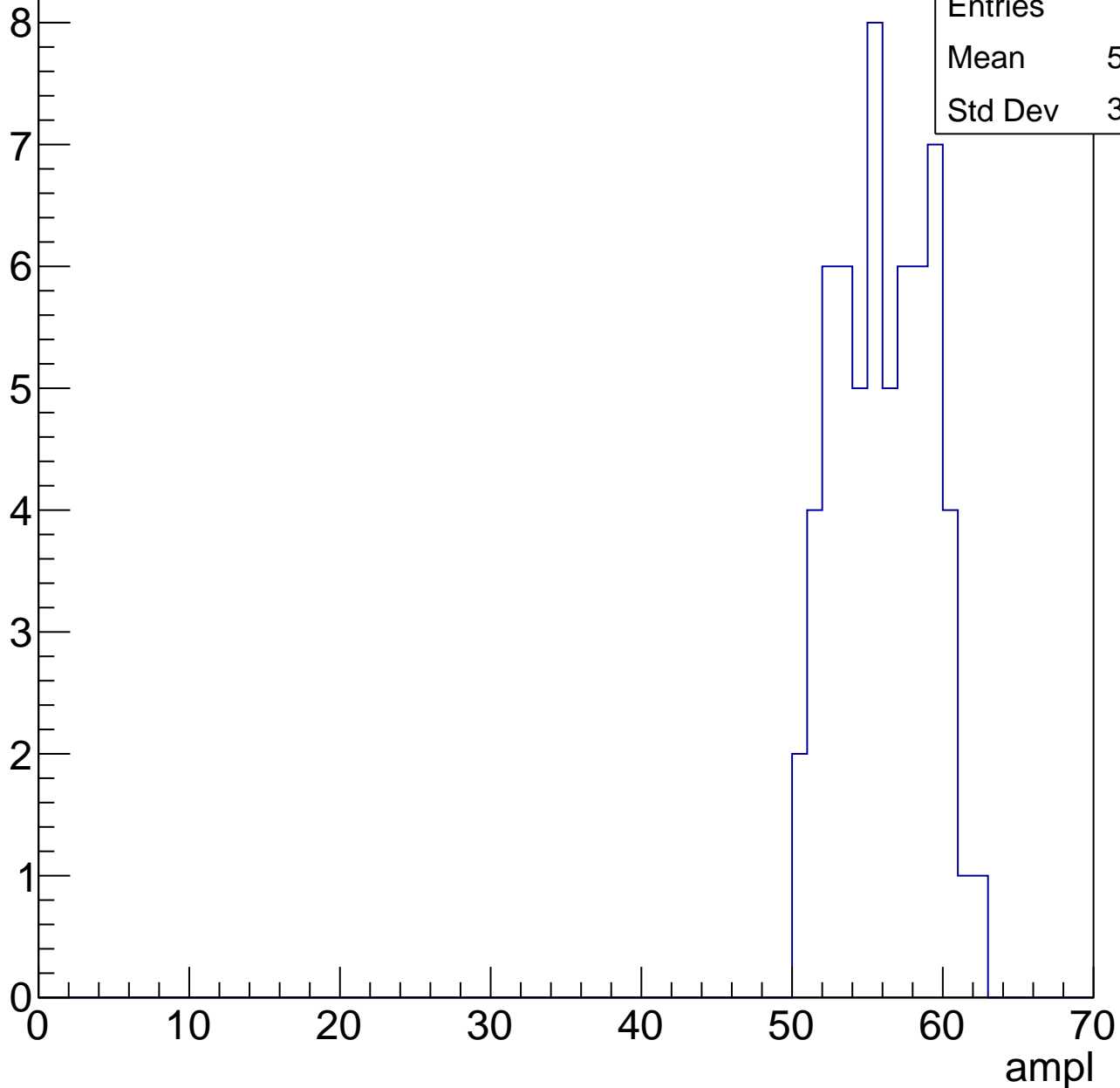
Entries	73
Mean	48.63
Std Dev	3.454



# B1L101S, U19-ch109, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

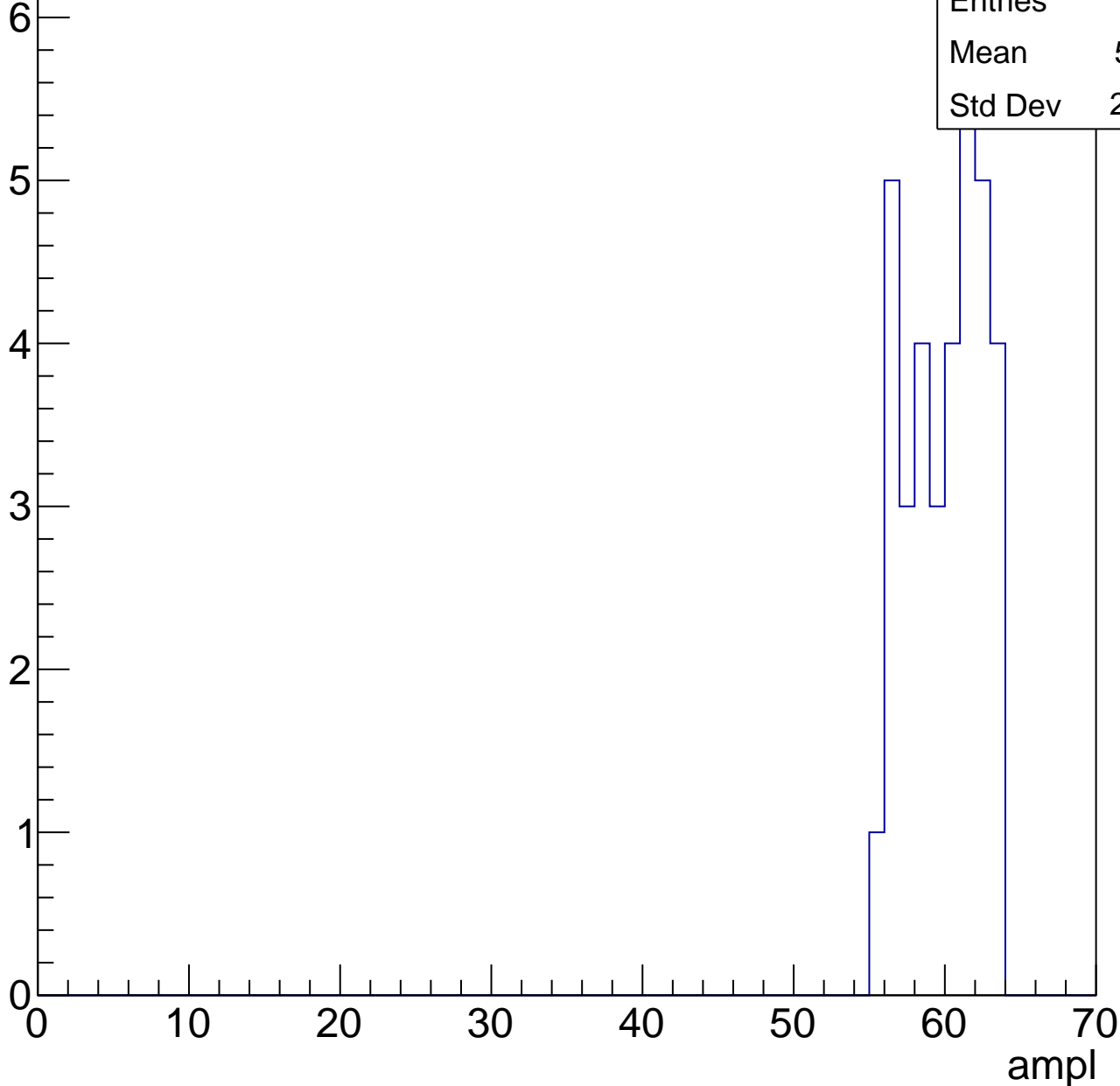


# B1L101S, U19-ch109, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	35
Mean	59.51
Std Dev	2.419

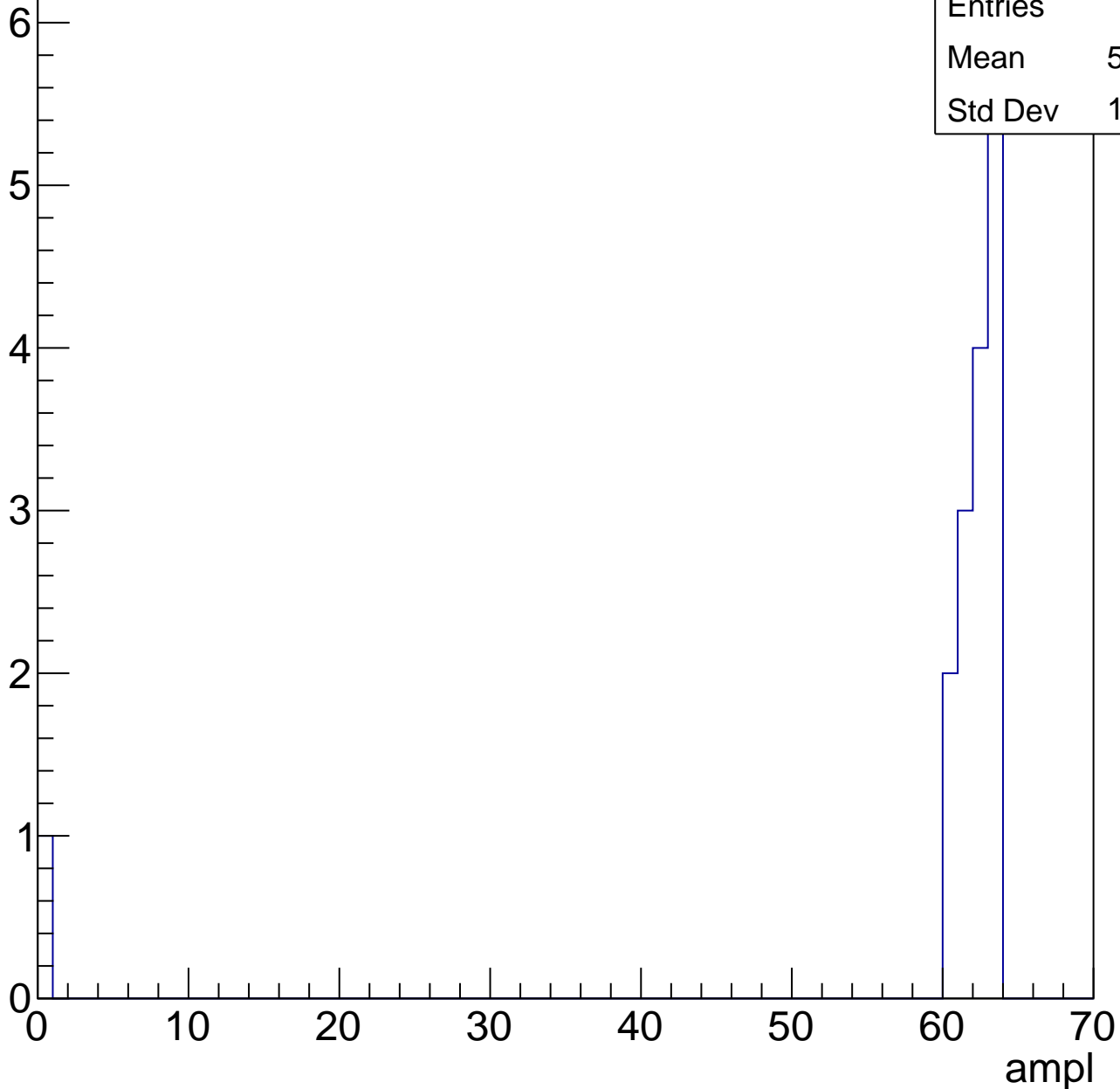


# B1L101S, U19-ch109, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	16
Mean	58.06
Std Dev	15.03





# B1L101S, U19-ch109, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U19-ch110, adc0

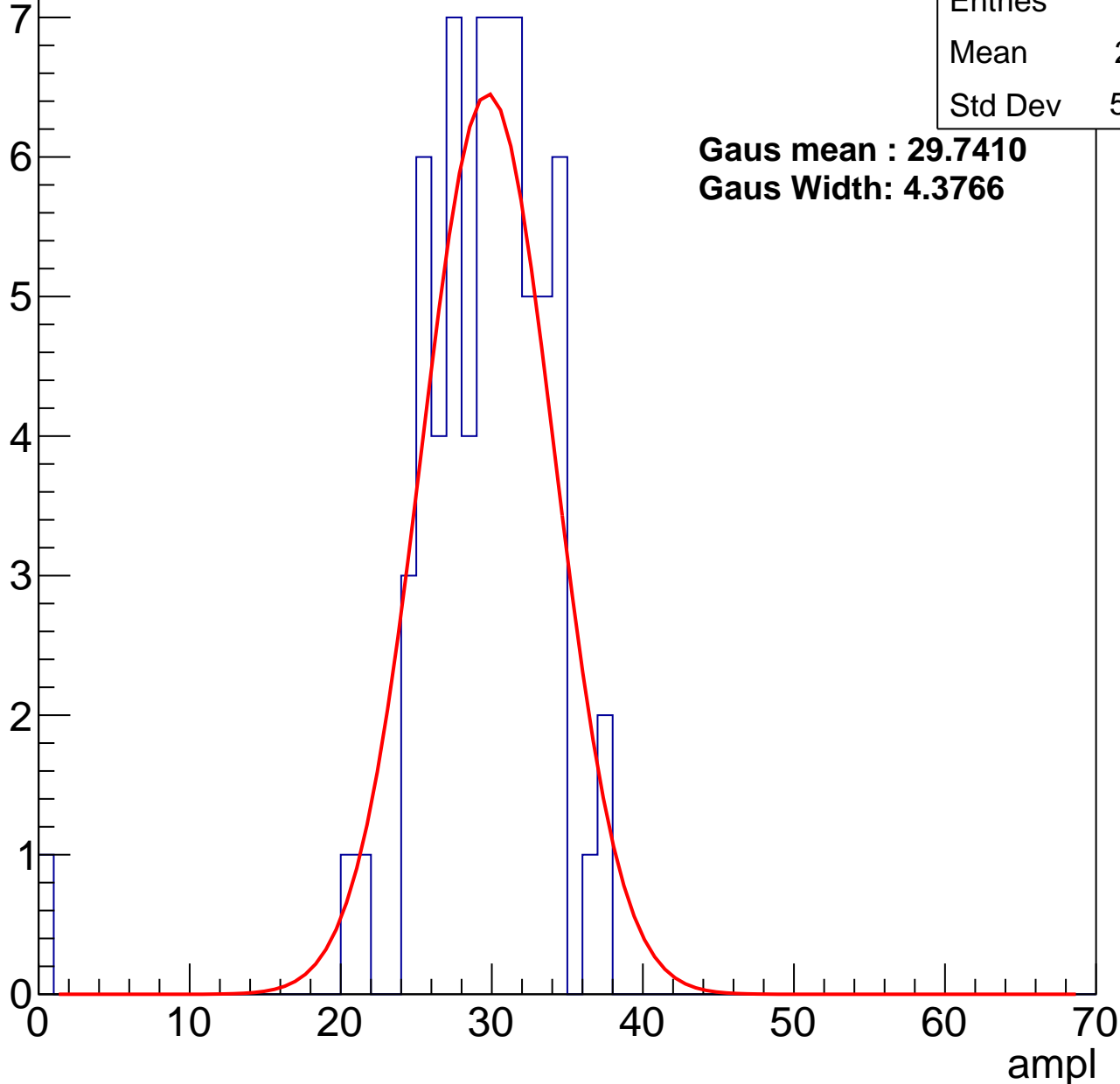
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	67
Mean	28.91
Std Dev	5.054

**Gaus mean : 29.7410**

**Gaus Width: 4.3766**



# B1L101S, U19-ch110, adc1

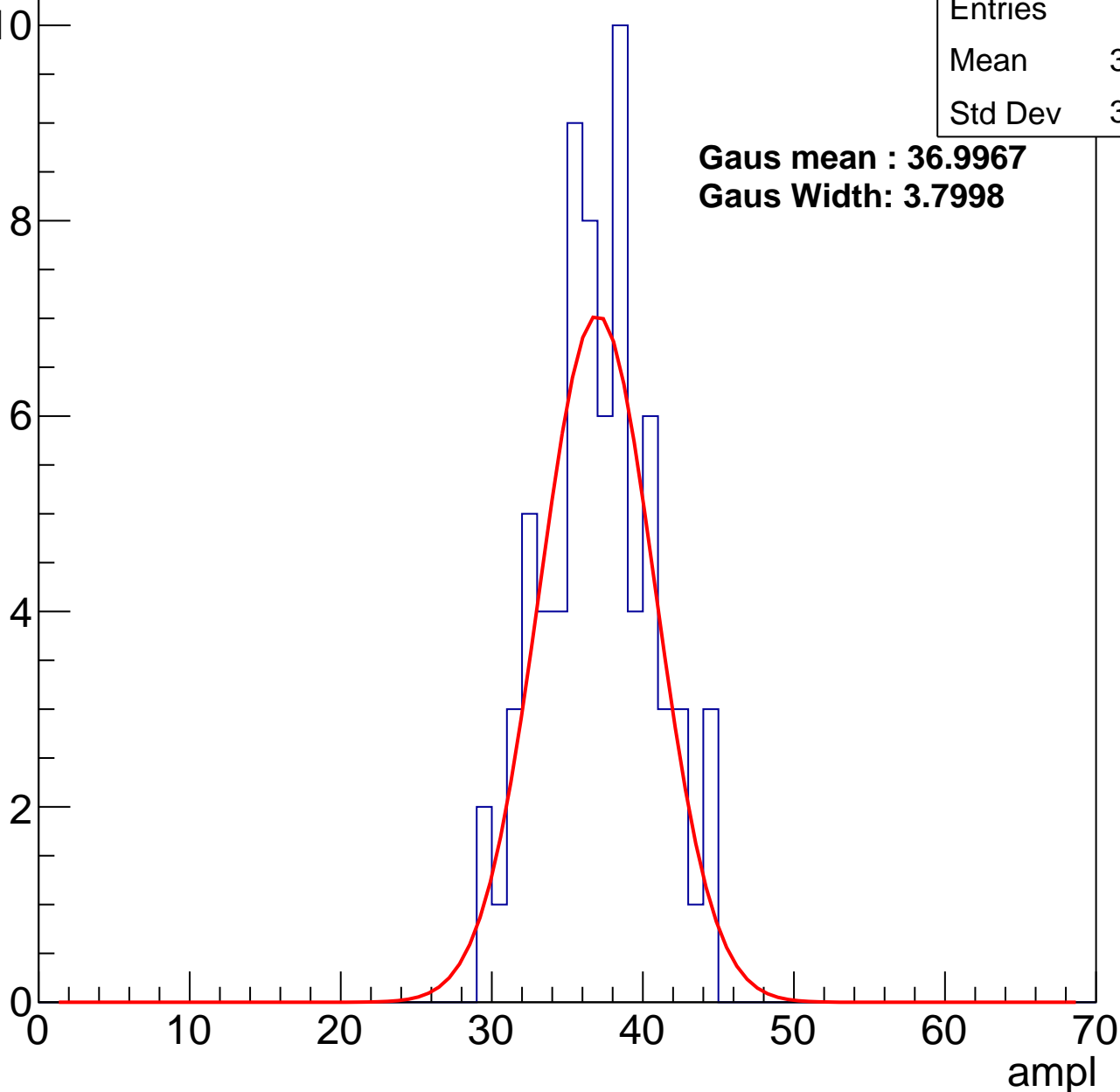
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	72
Mean	36.58
Std Dev	3.589

**Gaus mean : 36.9967**

**Gaus Width: 3.7998**



# B1L101S, U19-ch110, adc2

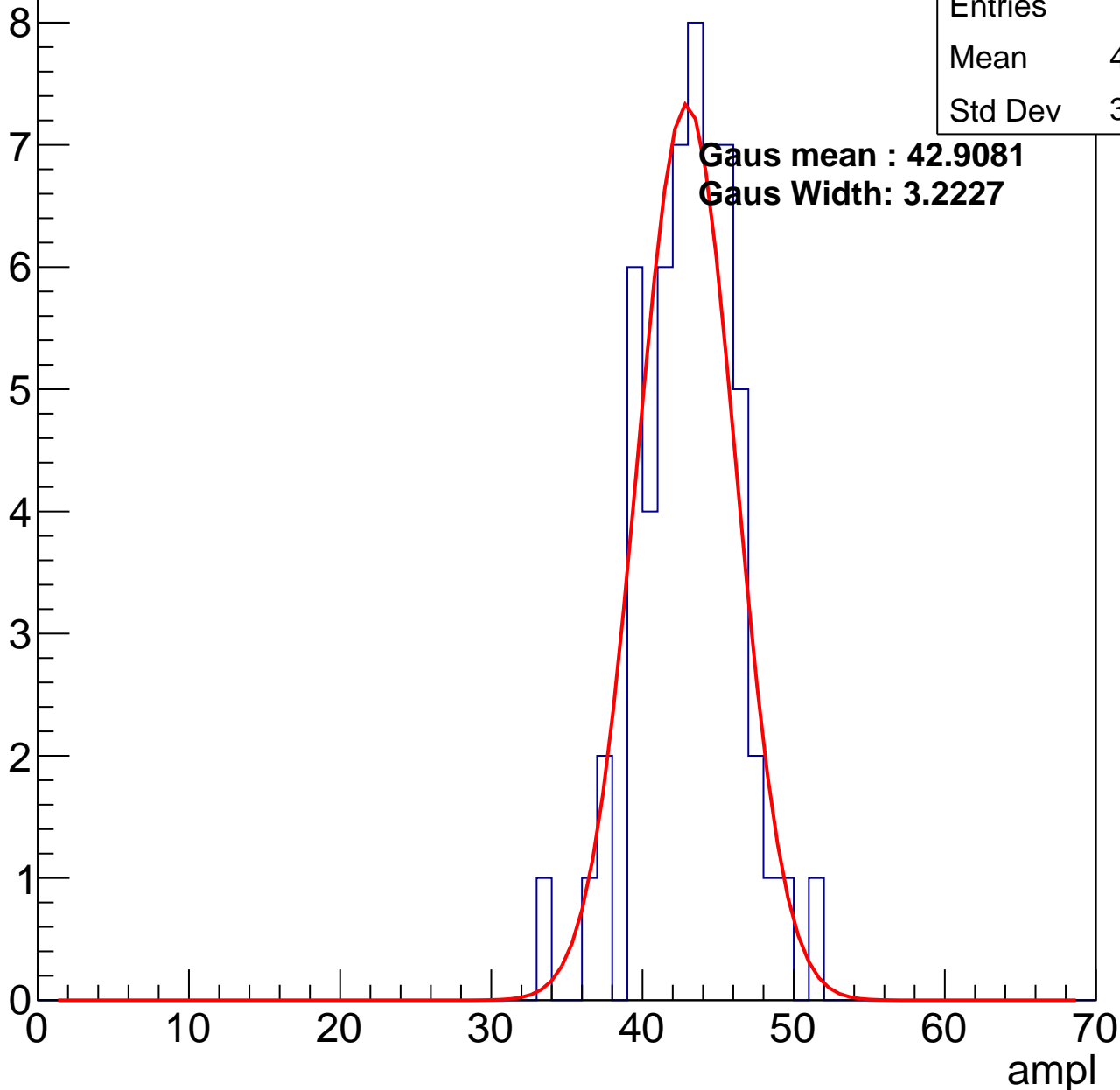
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	59
Mean	42.64
Std Dev	3.225

**Gaus mean : 42.9081**

**Gaus Width: 3.2227**

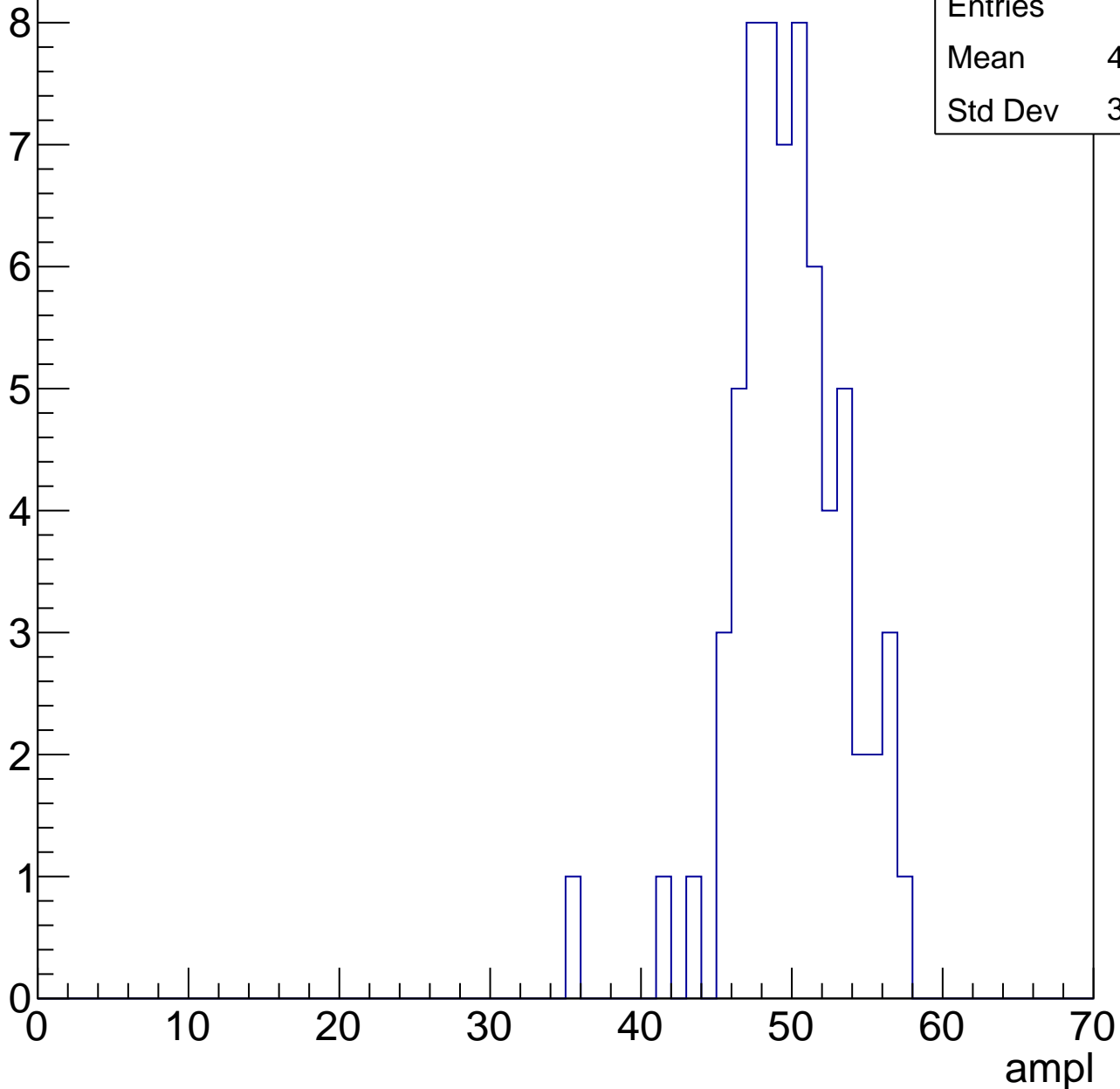


# B1L101S, U19-ch110, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	49.37
Std Dev	3.723

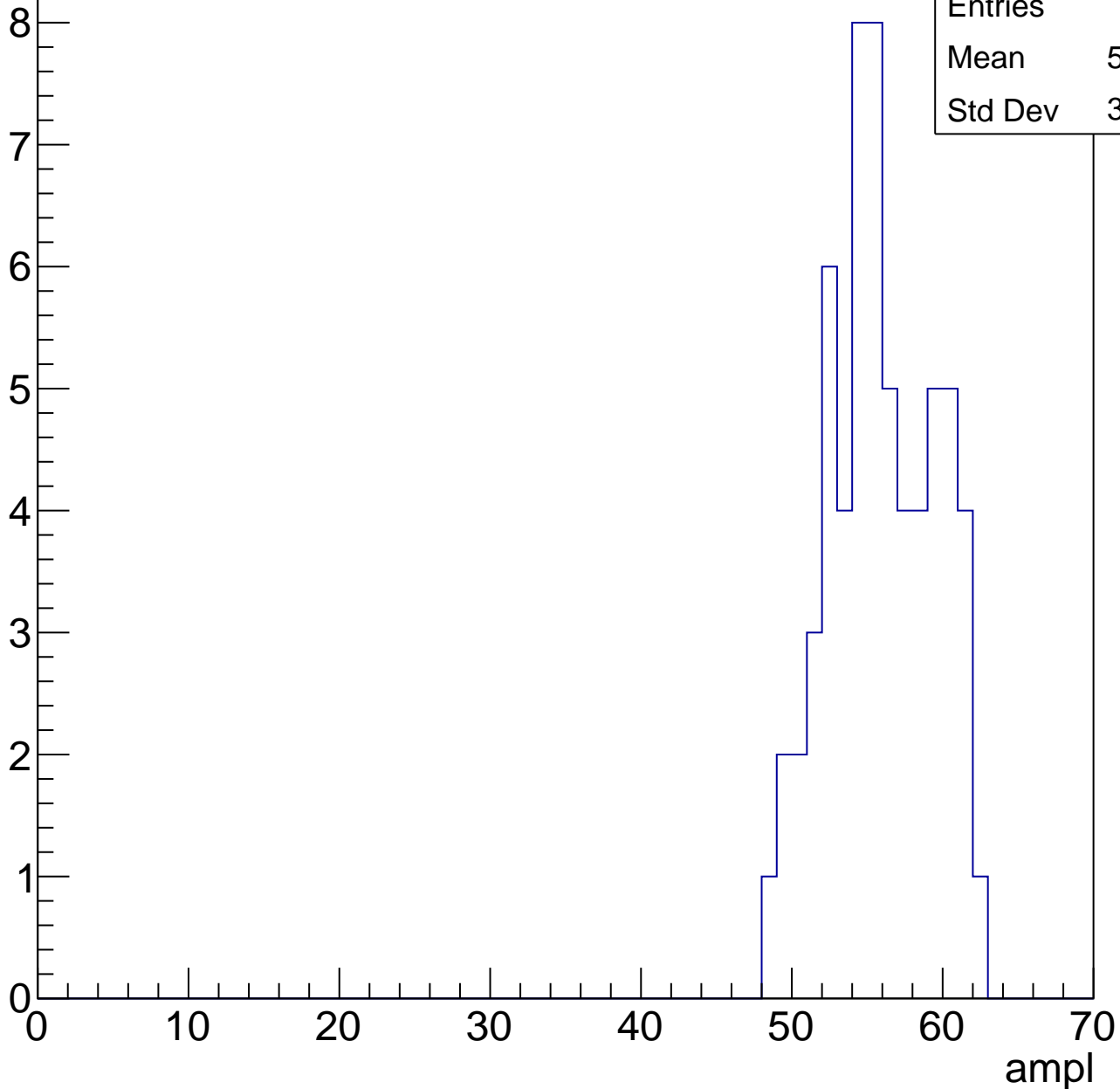


# B1L101S, U19-ch110, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	55.42
Std Dev	3.457

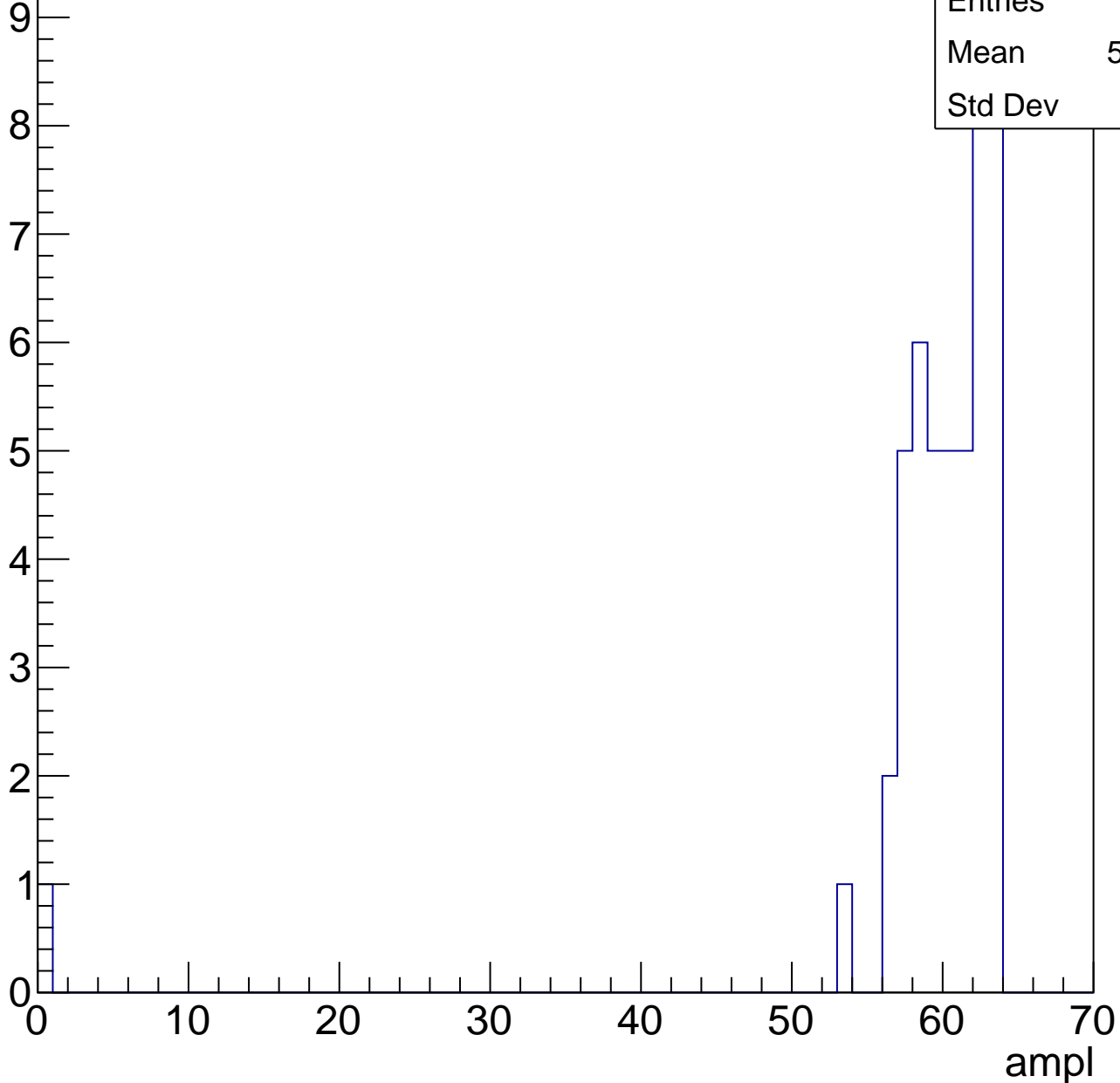


# B1L101S, U19-ch110, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	47
Mean	58.74
Std Dev	8.99



# B1L101S, U19-ch110, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U19-ch110, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U19-ch111, adc0

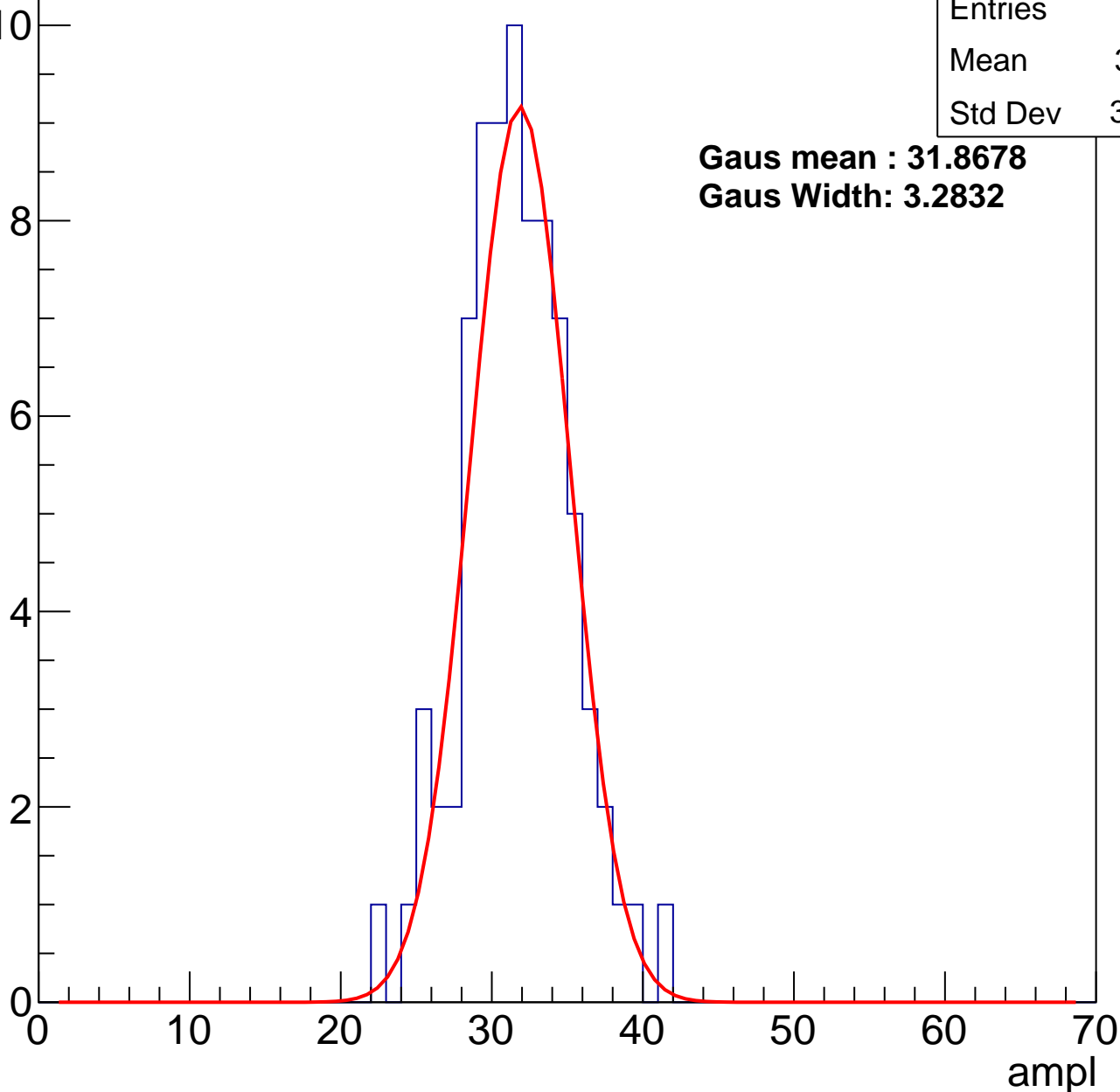
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	80
Mean	31.21
Std Dev	3.477

**Gaus mean : 31.8678**

**Gaus Width: 3.2832**



# B1L101S, U19-ch111, adc1

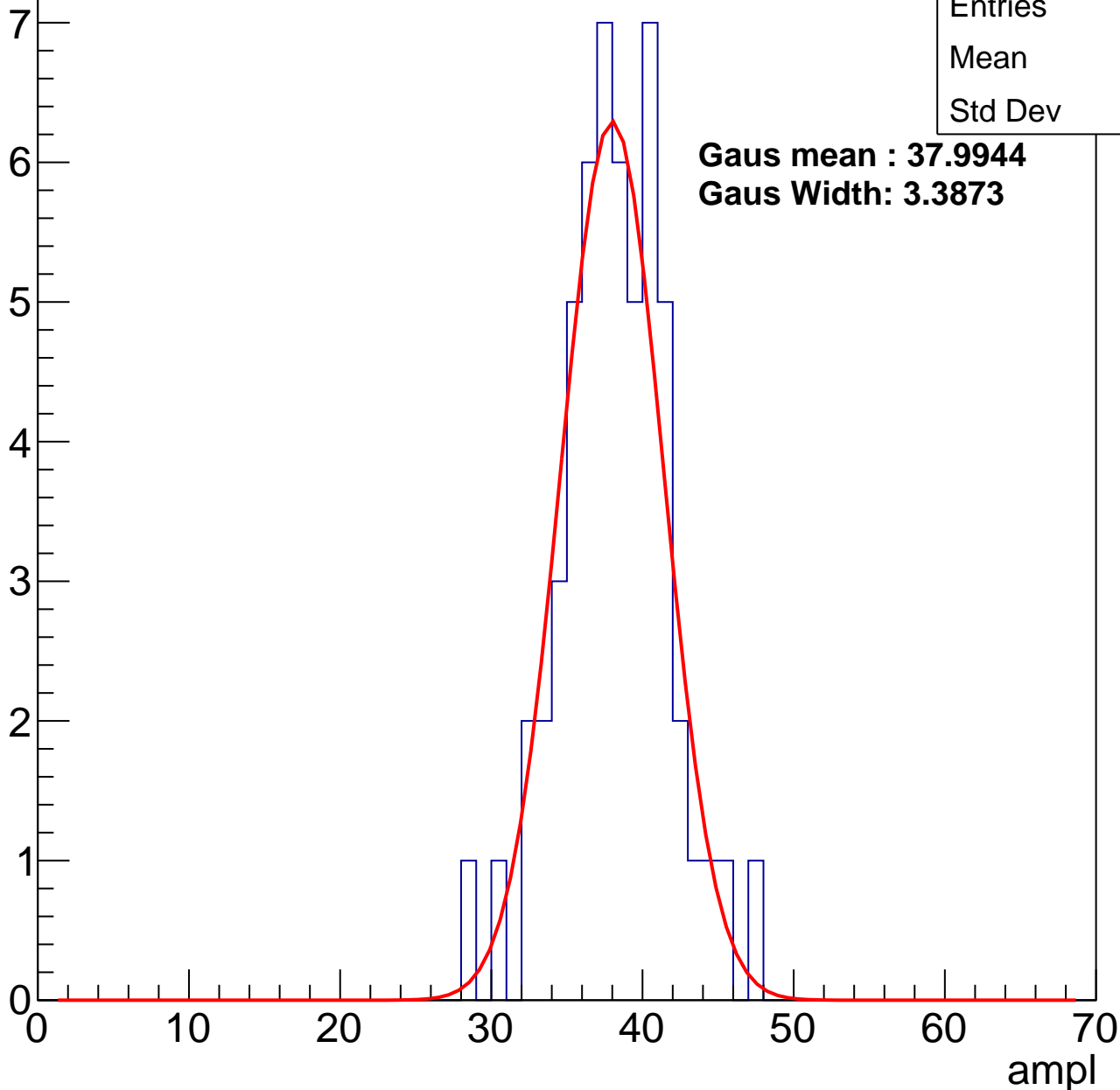
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	56
Mean	37.7
Std Dev	3.55

**Gaus mean : 37.9944**

**Gaus Width: 3.3873**



# B1L101S, U19-ch111, adc2

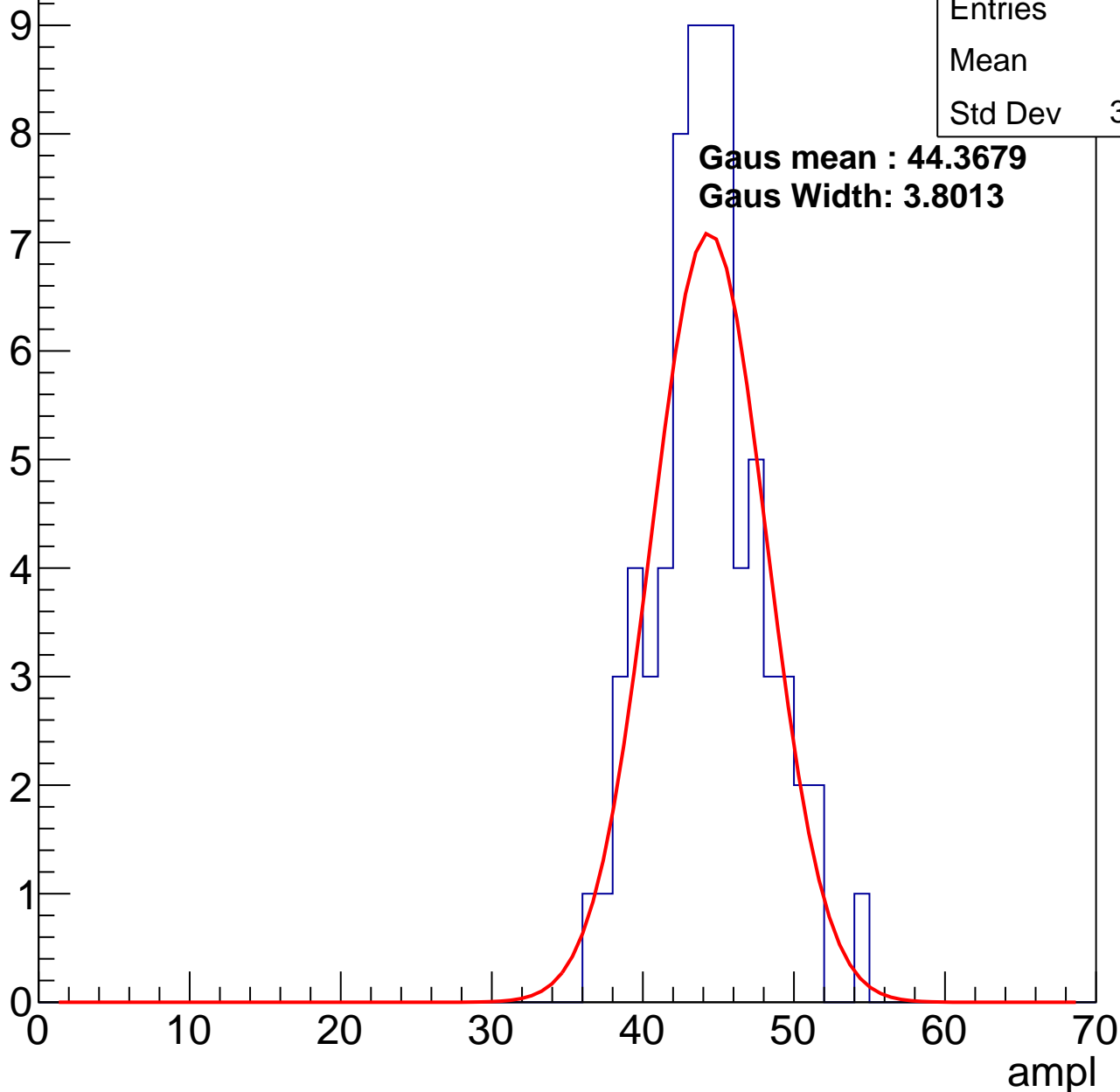
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	71
Mean	43.9
Std Dev	3.577

**Gaus mean : 44.3679**

**Gaus Width: 3.8013**

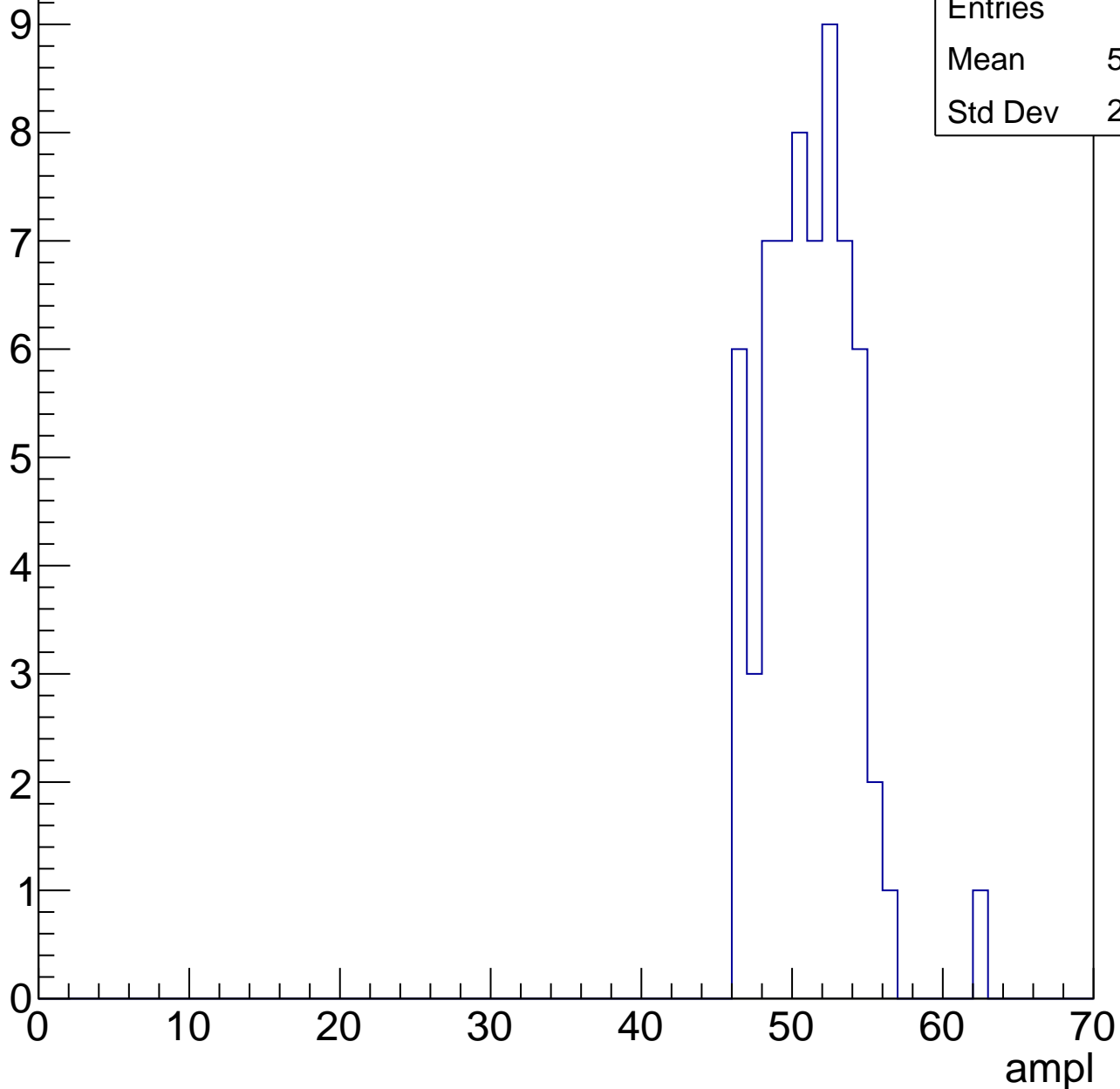


# B1L101S, U19-ch111, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	50.69
Std Dev	2.957

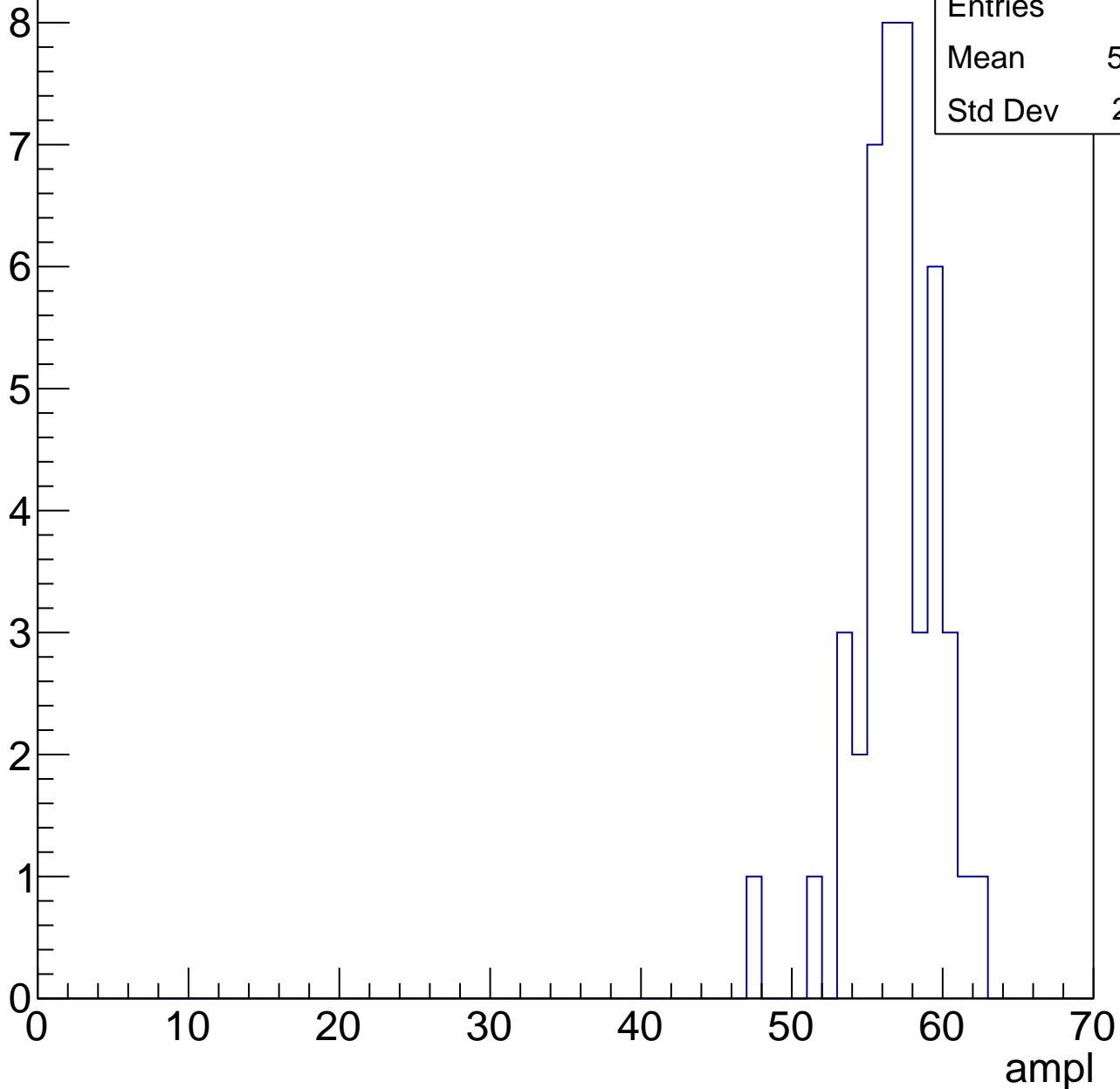


# B1L101S, U19-ch111, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	44
Mean	56.48
Std Dev	2.701

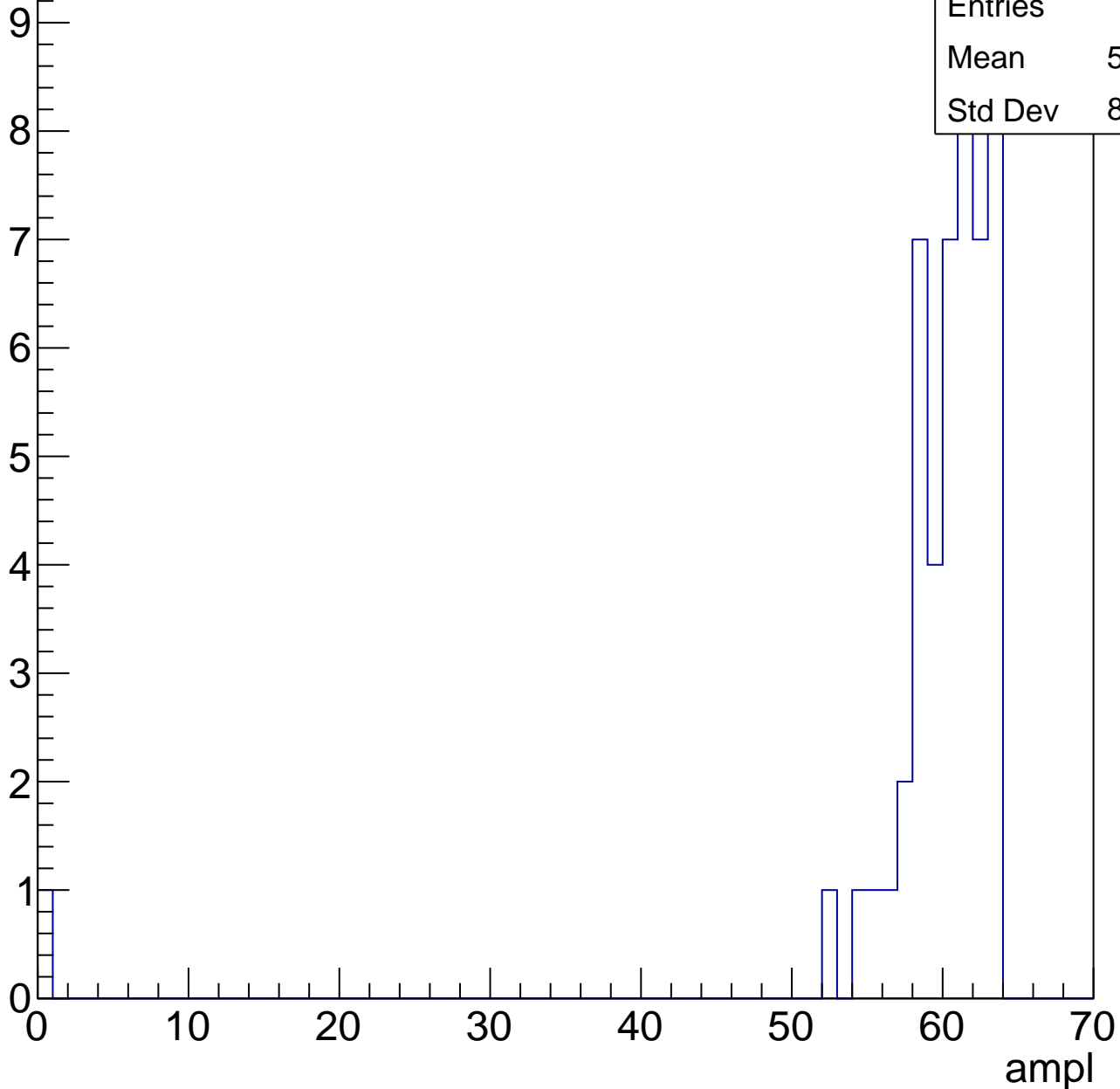


# B1L101S, U19-ch111, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	50
Mean	58.86
Std Dev	8.768



# B1L101S, U19-ch111, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U19-ch111, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L101S, U19-ch112, adc0

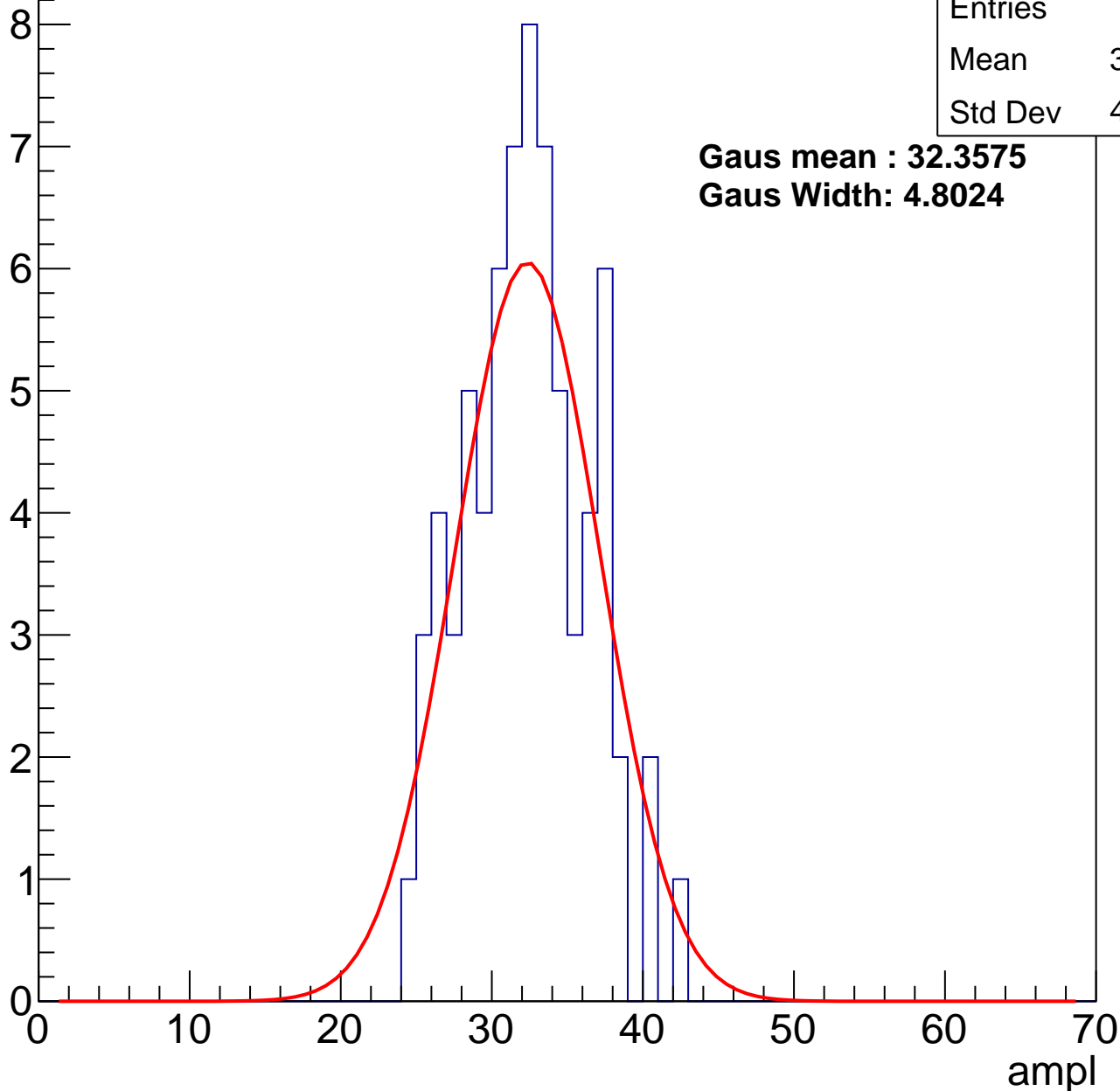
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	71
Mean	31.87
Std Dev	4.014

**Gaus mean : 32.3575**

**Gaus Width: 4.8024**



# B1L101S, U19-ch112, adc1

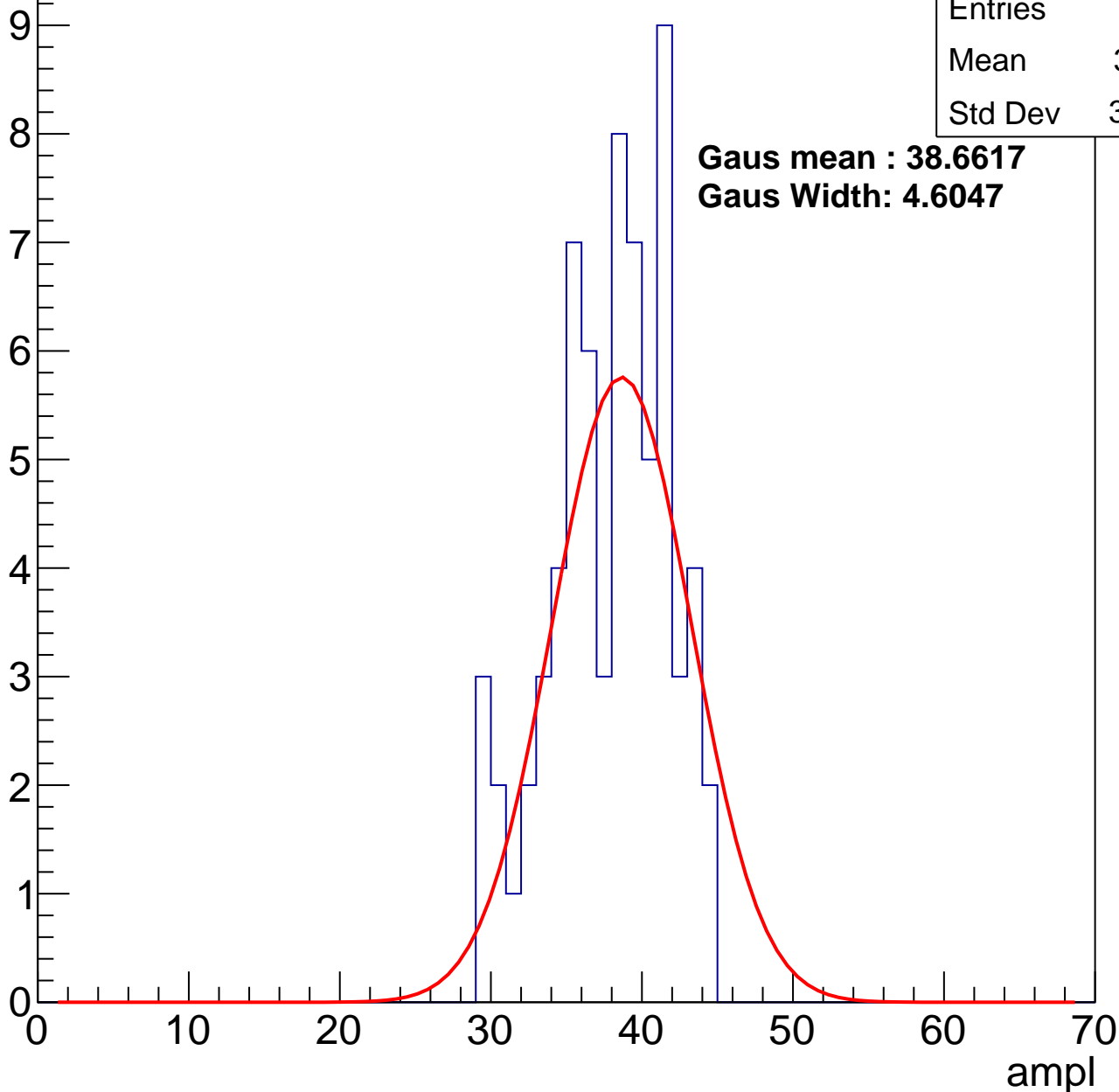
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	37.41
Std Dev	3.854

**Gaus mean : 38.6617**

**Gaus Width: 4.6047**



# B1L101S, U19-ch112, adc2

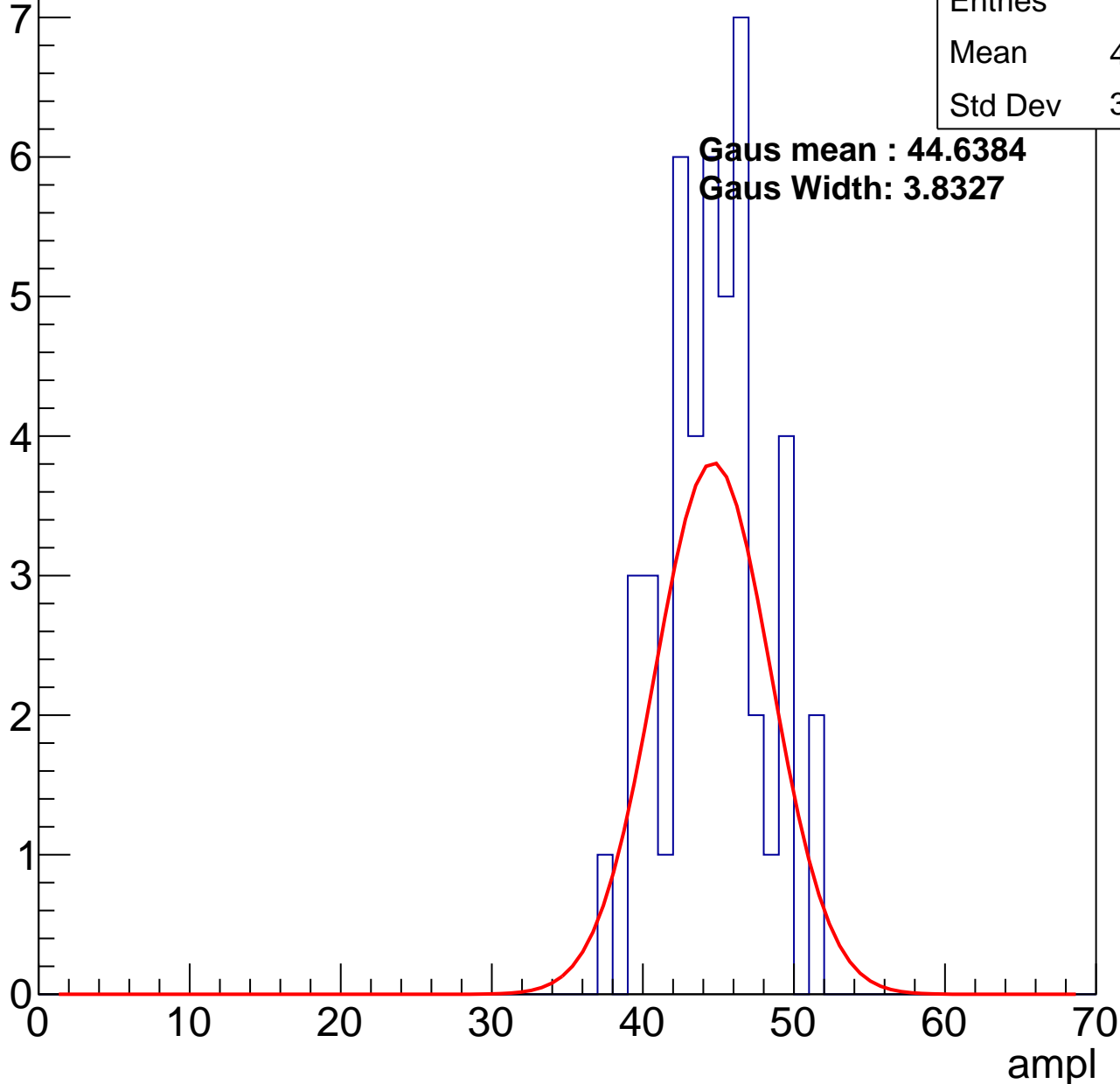
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	45
Mean	44.22
Std Dev	3.238

**Gaus mean : 44.6384**

**Gaus Width: 3.8327**

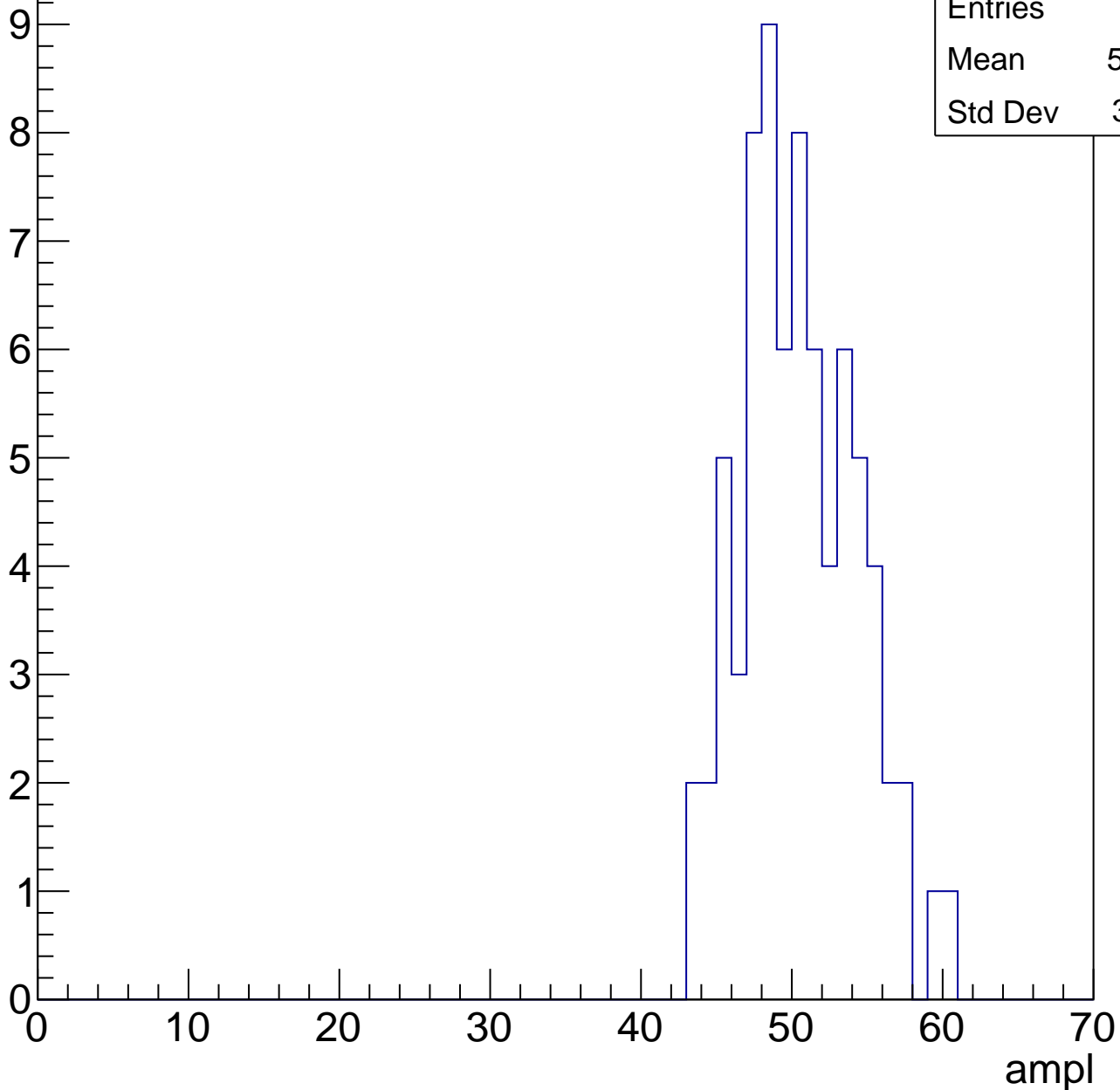


# B1L101S, U19-ch112, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

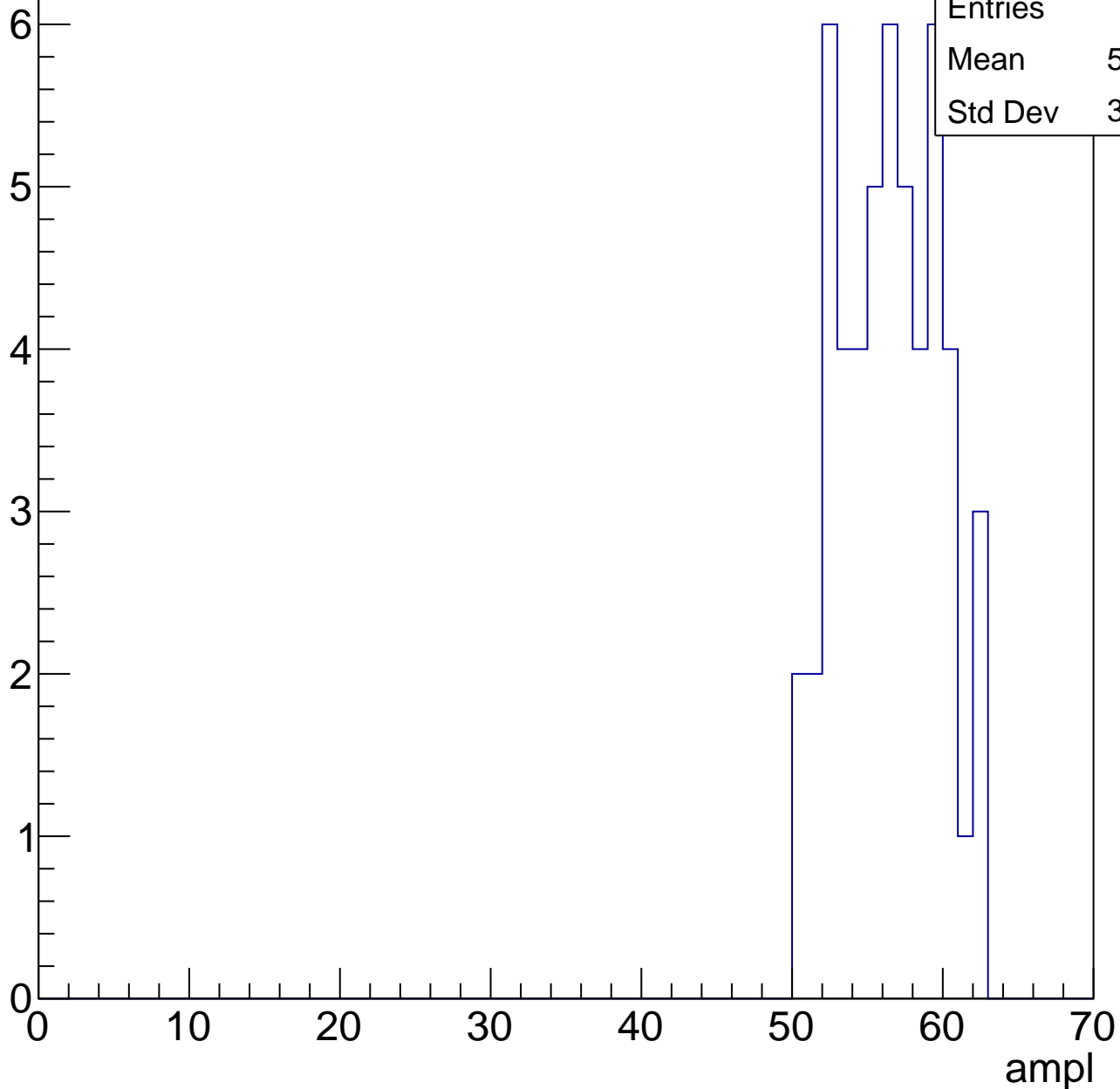
Entries	74
Mean	50.08
Std Dev	3.791



# B1L101S, U19-ch112, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



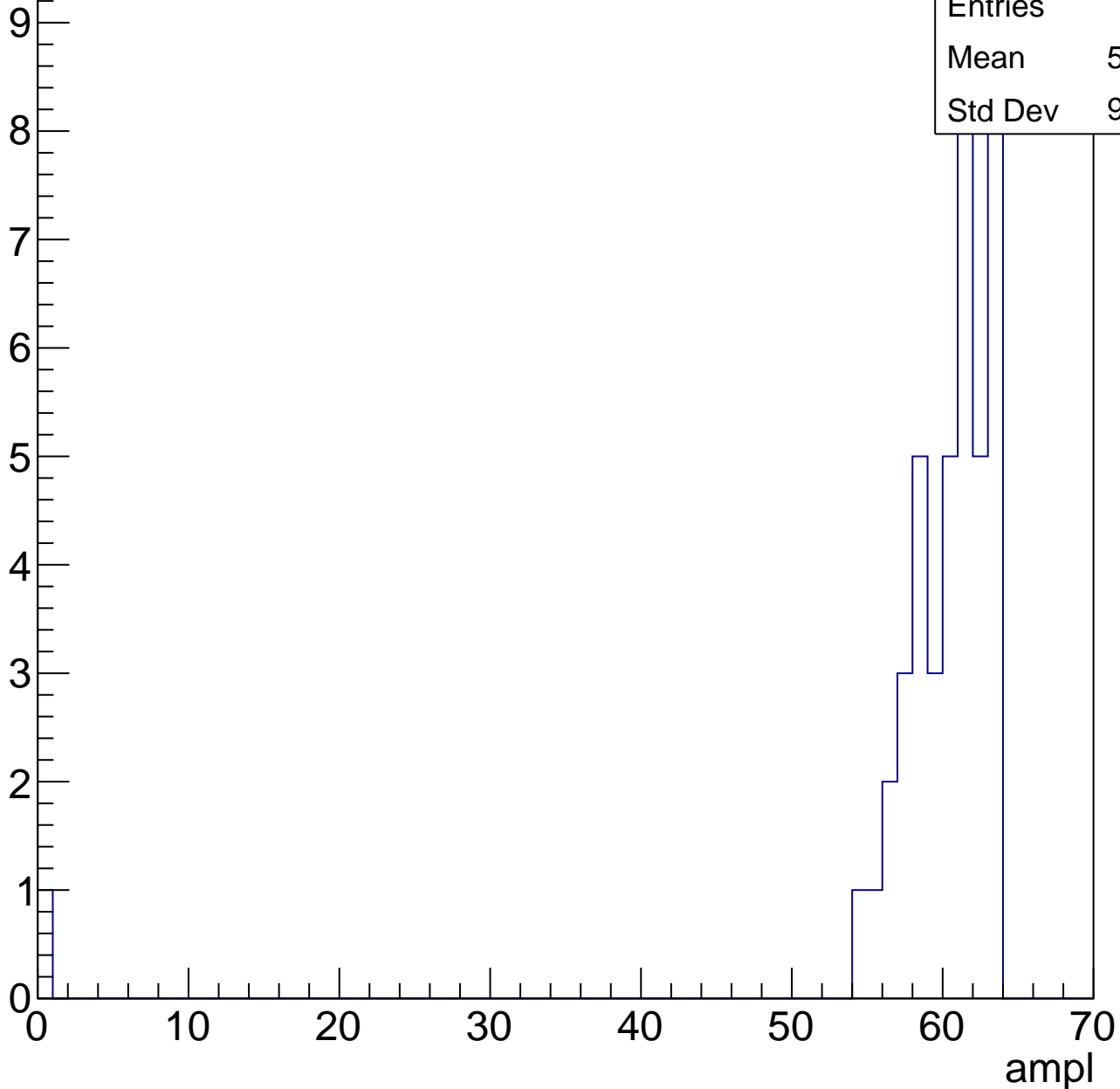
Entries	52
Mean	55.98
Std Dev	3.243

# B1L101S, U19-ch112, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

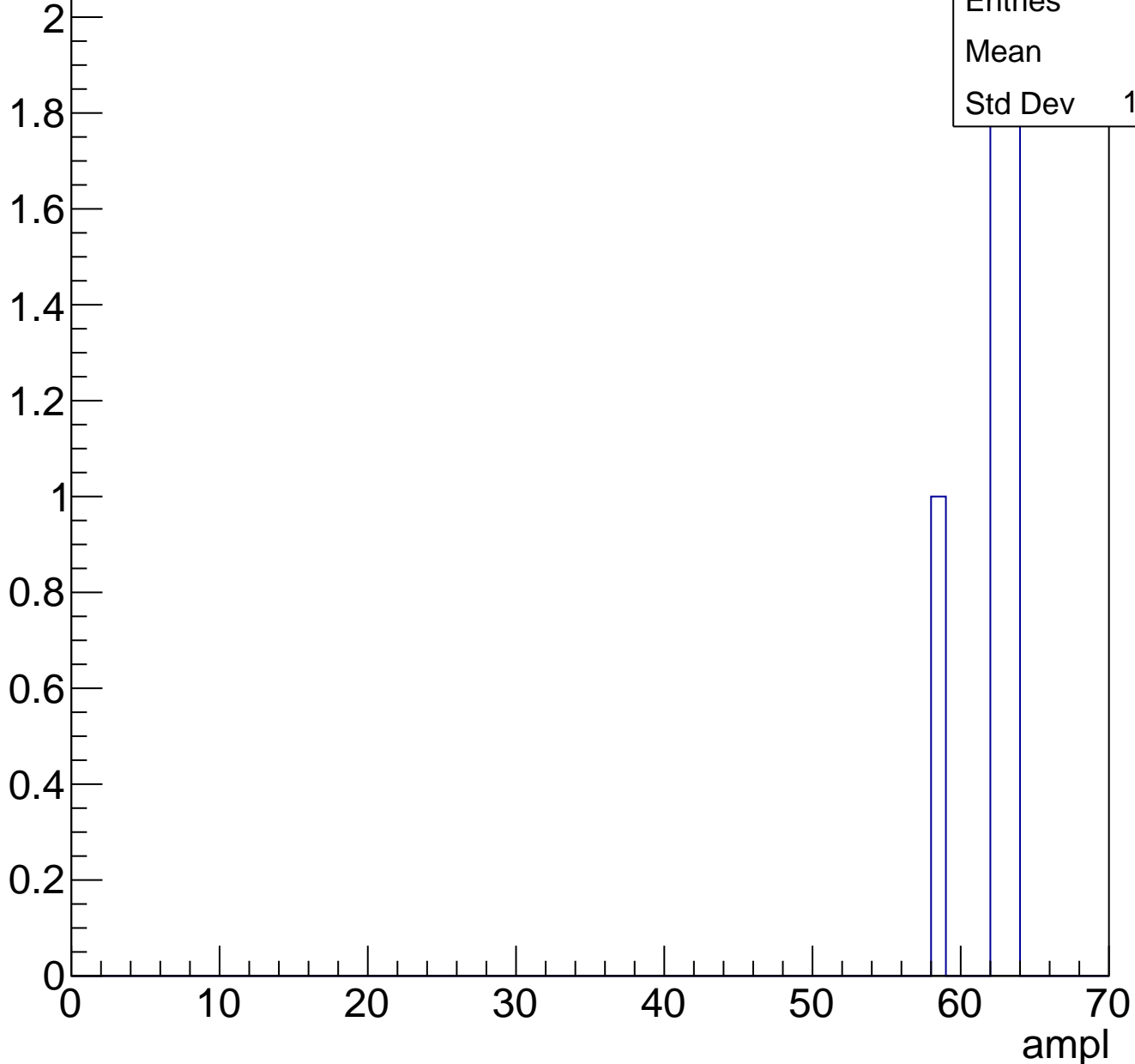
Entries	43
Mean	58.65
Std Dev	9.358



# B1L101S, U19-ch112, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

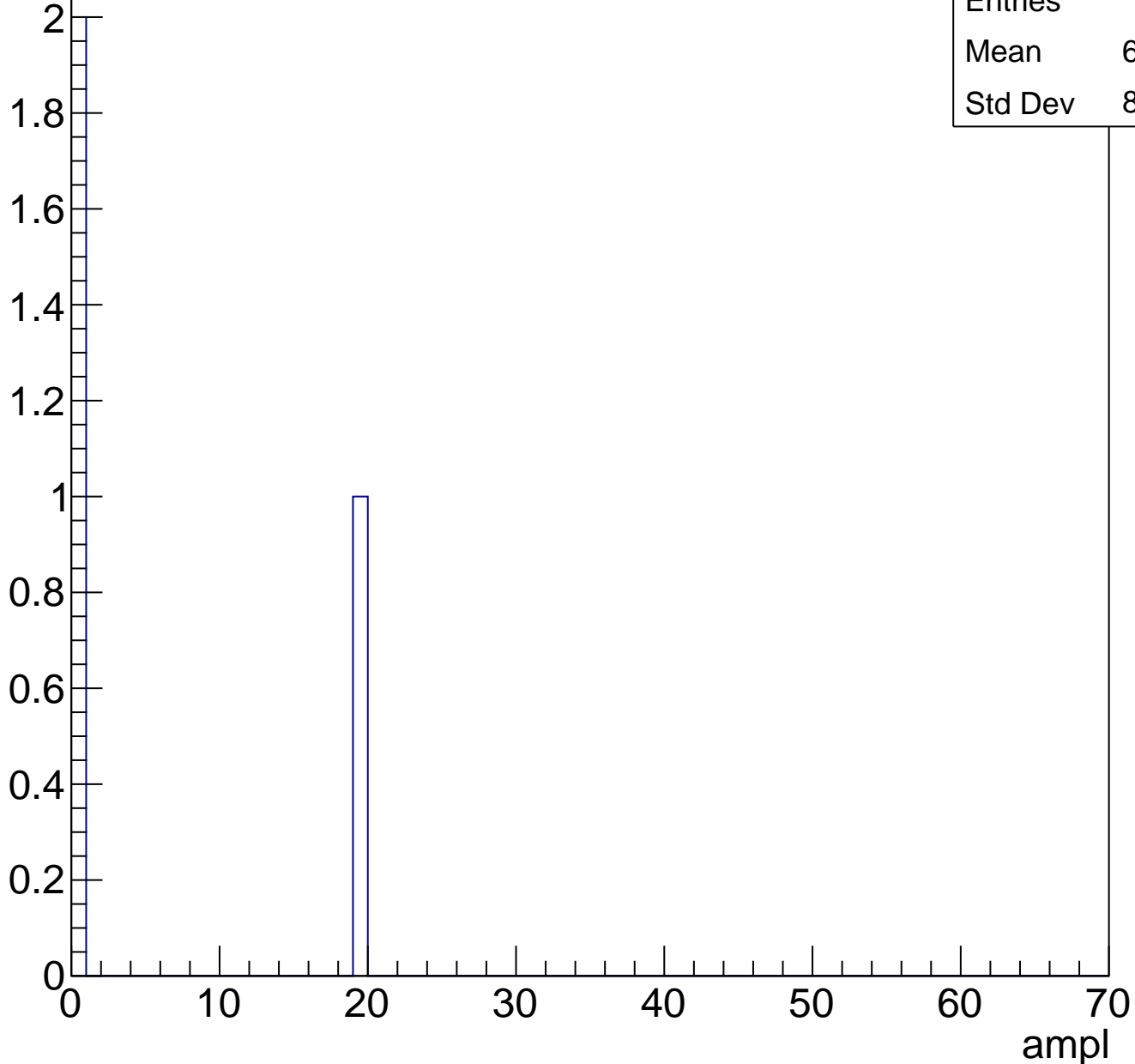




# B1L101S, U19-ch112, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	3
Mean	6.333
Std Dev	8.957

# B1L101S, U19-ch113, adc0

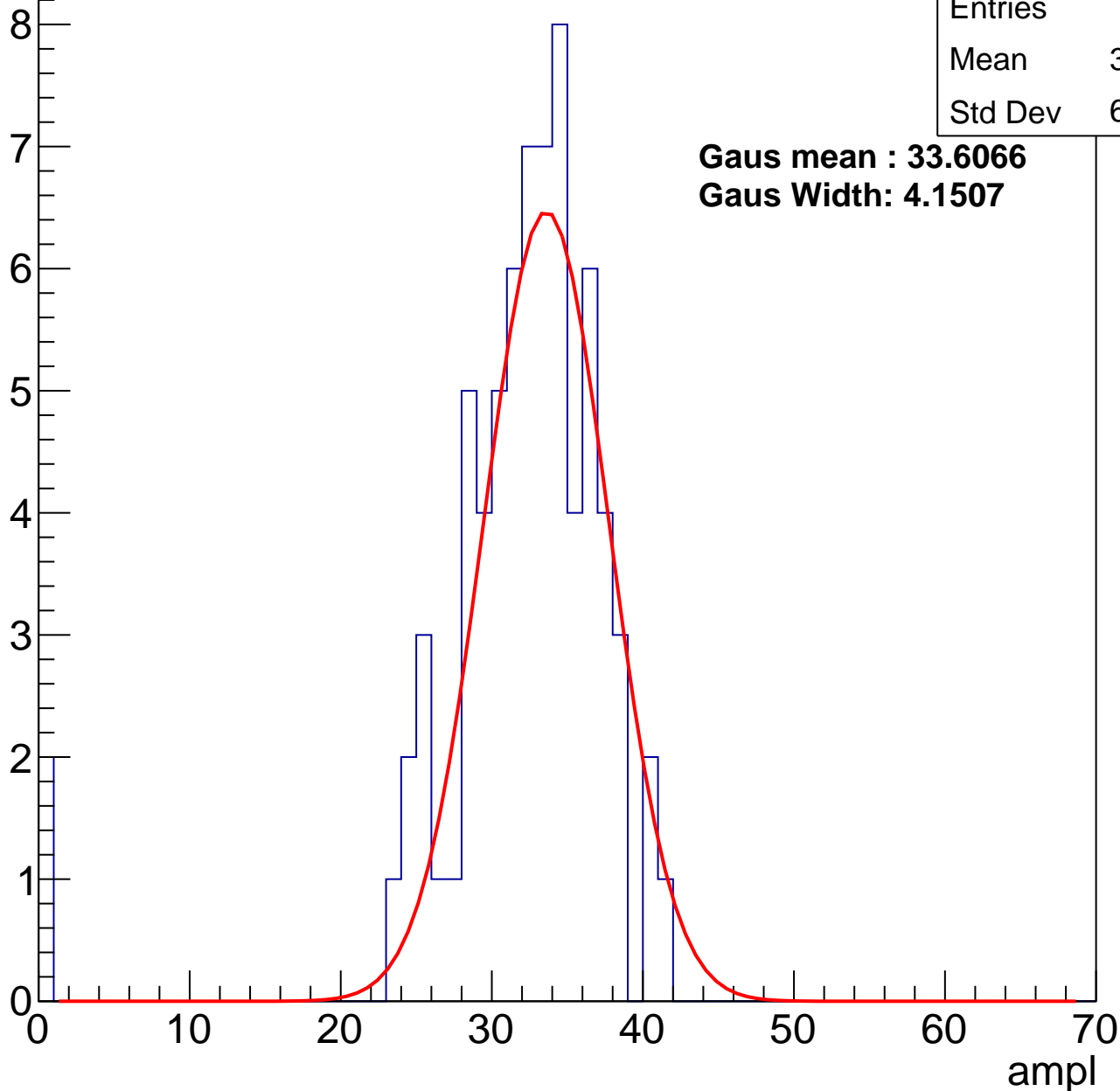
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	72
Mean	31.35
Std Dev	6.629

**Gaus mean : 33.6066**

**Gaus Width: 4.1507**



# B1L101S, U19-ch113, adc1

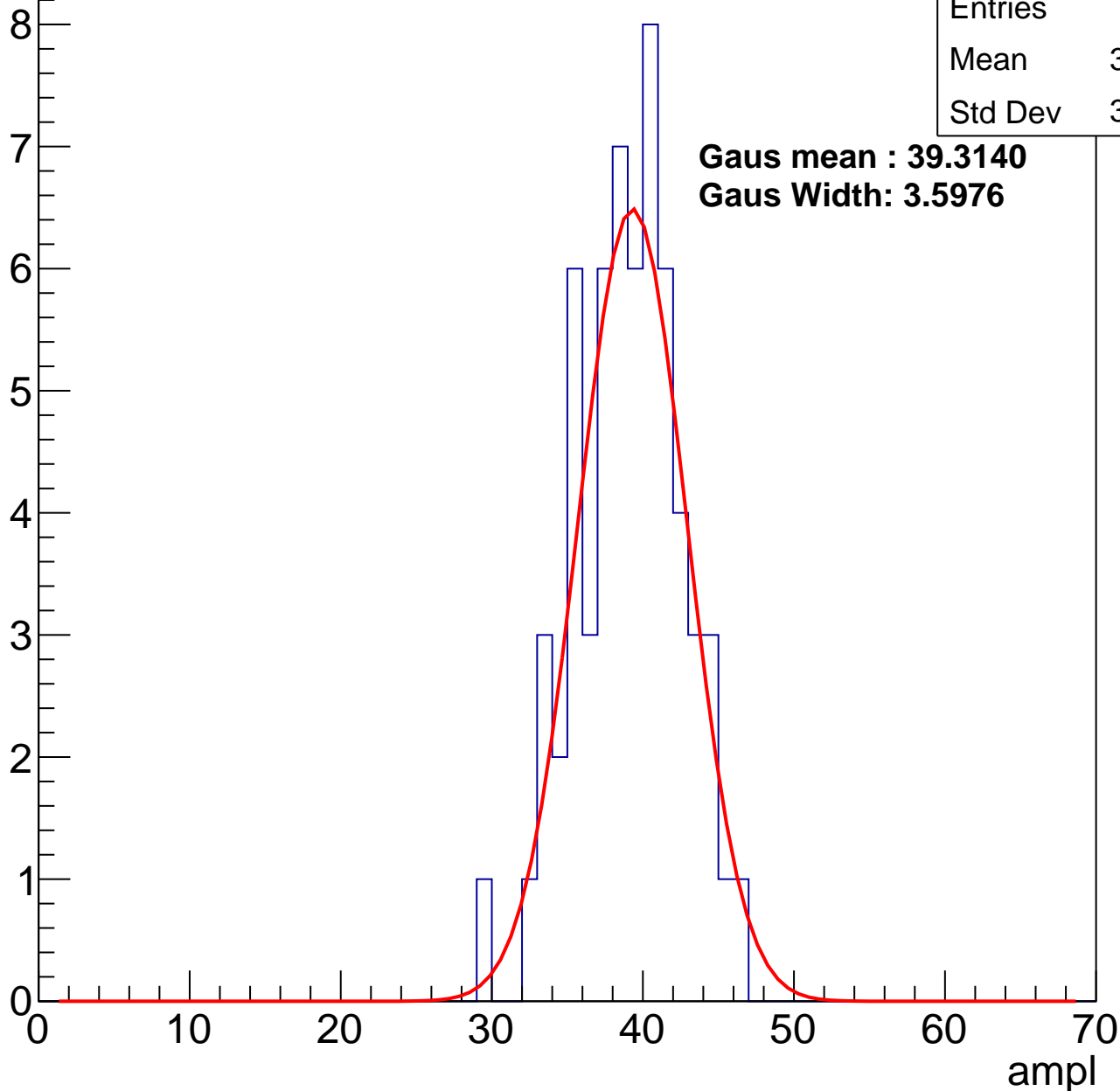
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	38.59
Std Dev	3.452

**Gaus mean : 39.3140**

**Gaus Width: 3.5976**



# B1L101S, U19-ch113, adc2

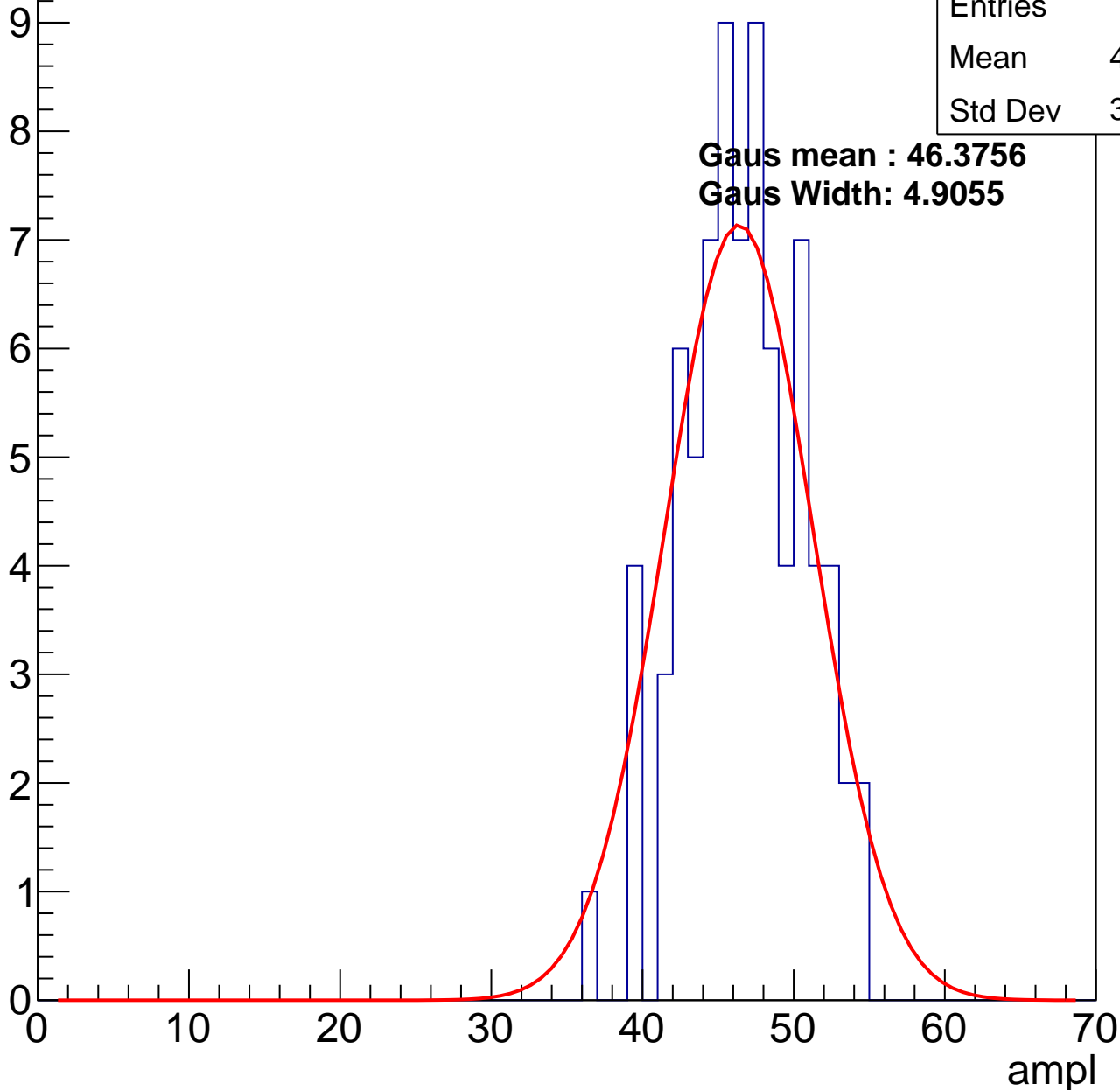
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	80
Mean	46.25
Std Dev	3.865

**Gaus mean : 46.3756**

**Gaus Width: 4.9055**

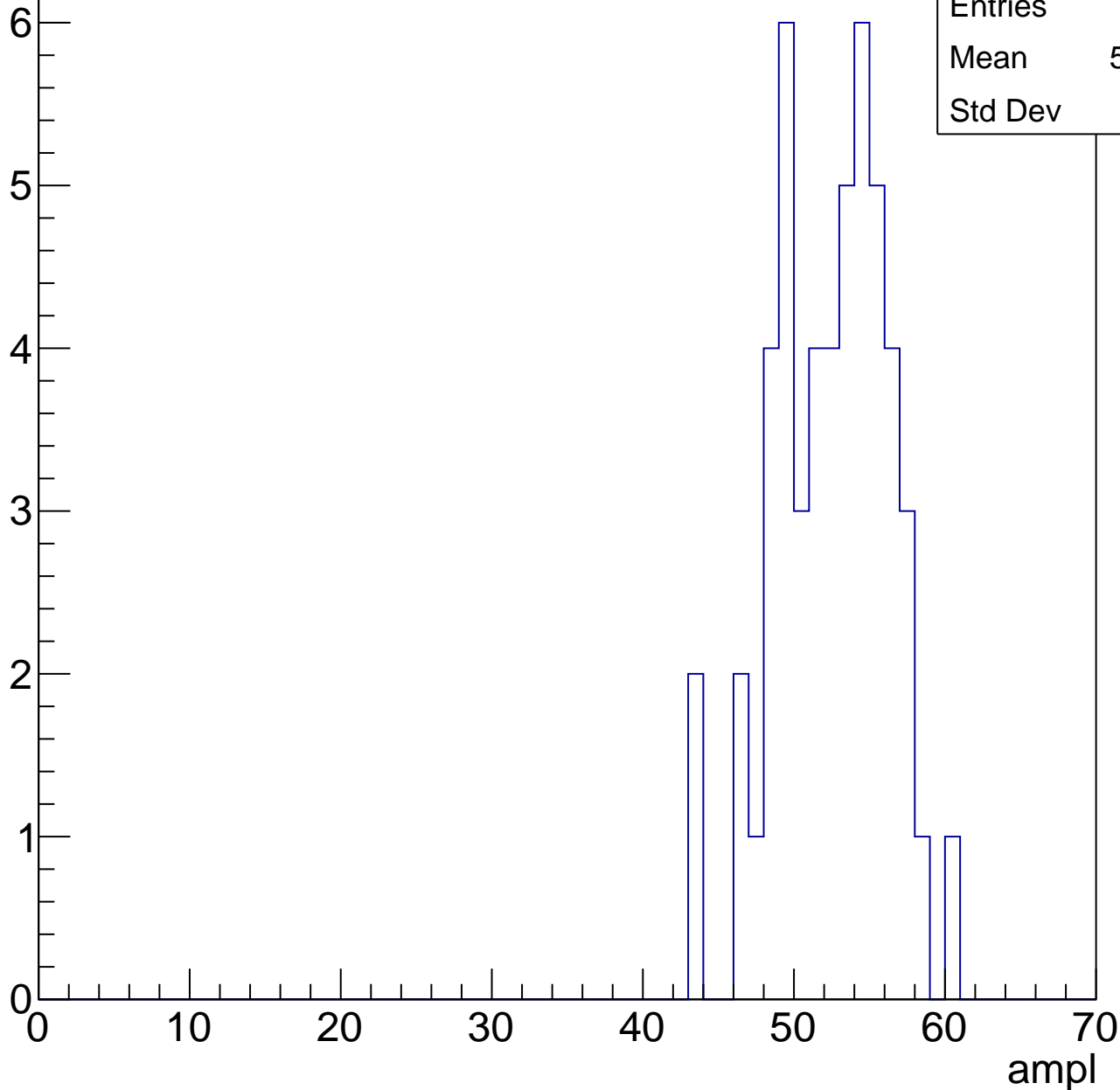


# B1L101S, U19-ch113, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	51
Mean	51.96
Std Dev	3.72

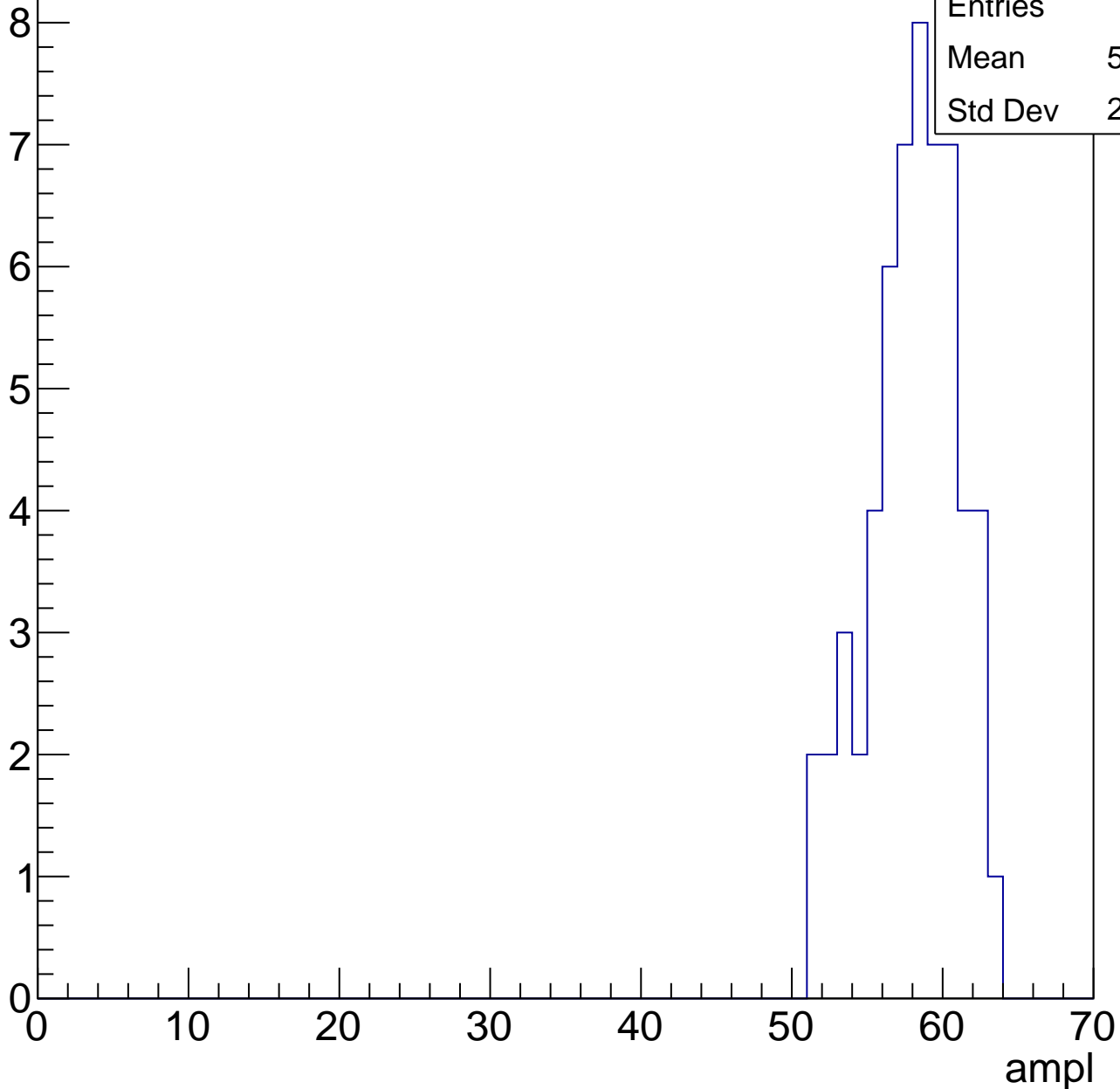


# B1L101S, U19-ch113, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	57
Mean	57.54
Std Dev	2.938

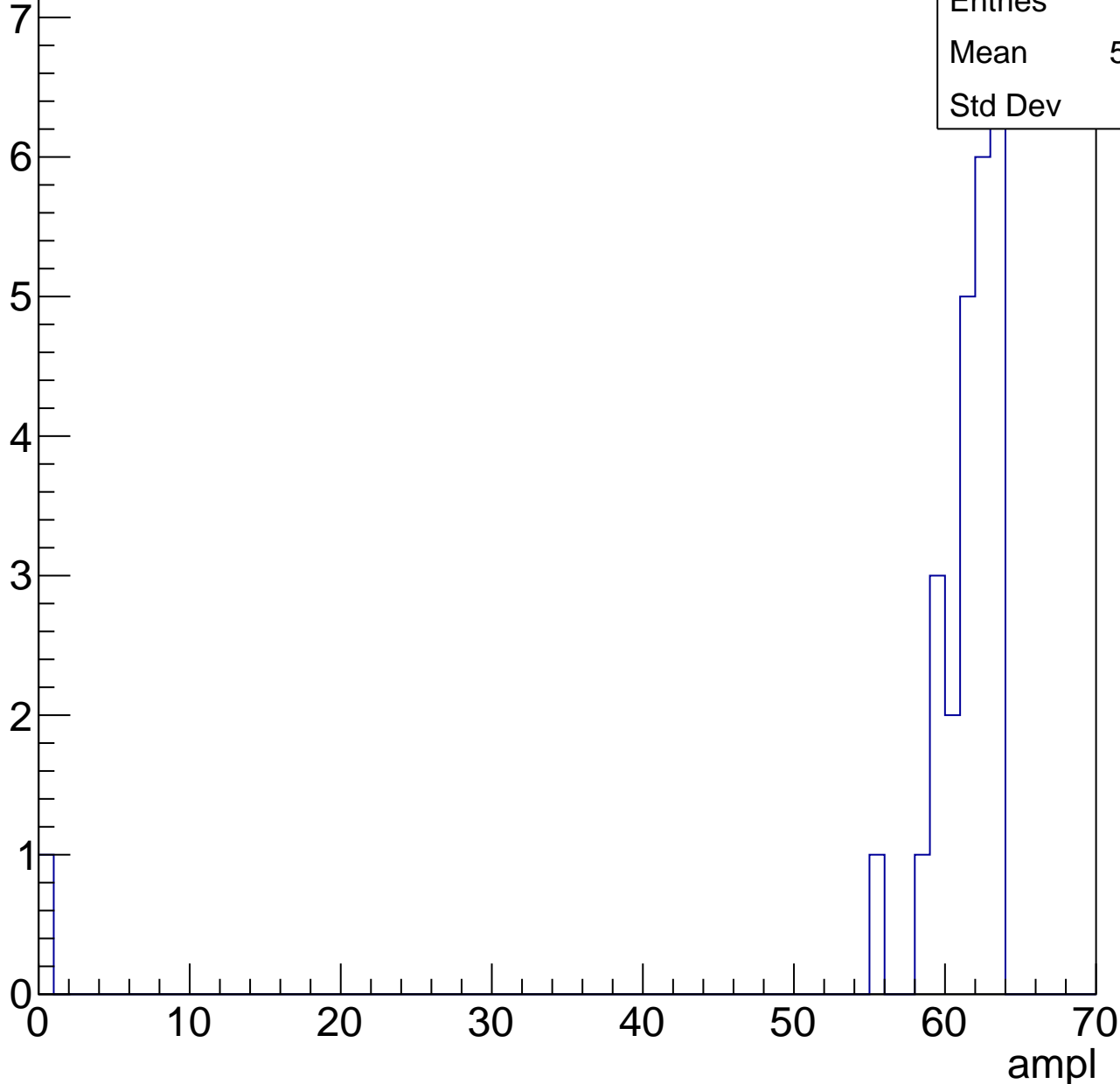


# B1L101S, U19-ch113, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	26
Mean	58.77
Std Dev	11.9



# B1L101S, U19-ch113, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U19-ch113, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U19-ch114, adc0

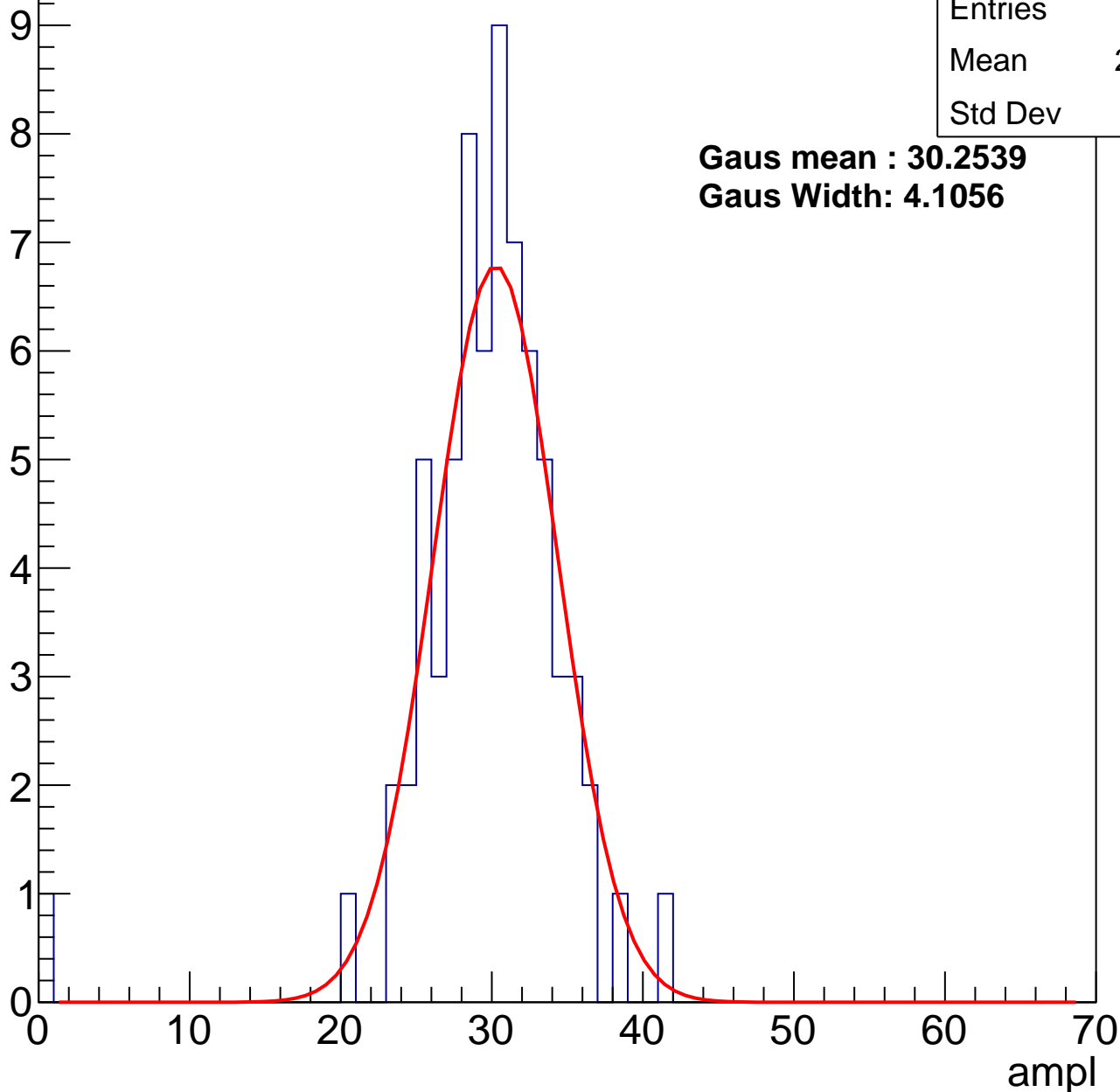
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	29.31
Std Dev	5.14

**Gaus mean : 30.2539**

**Gaus Width: 4.1056**



# B1L101S, U19-ch114, adc1

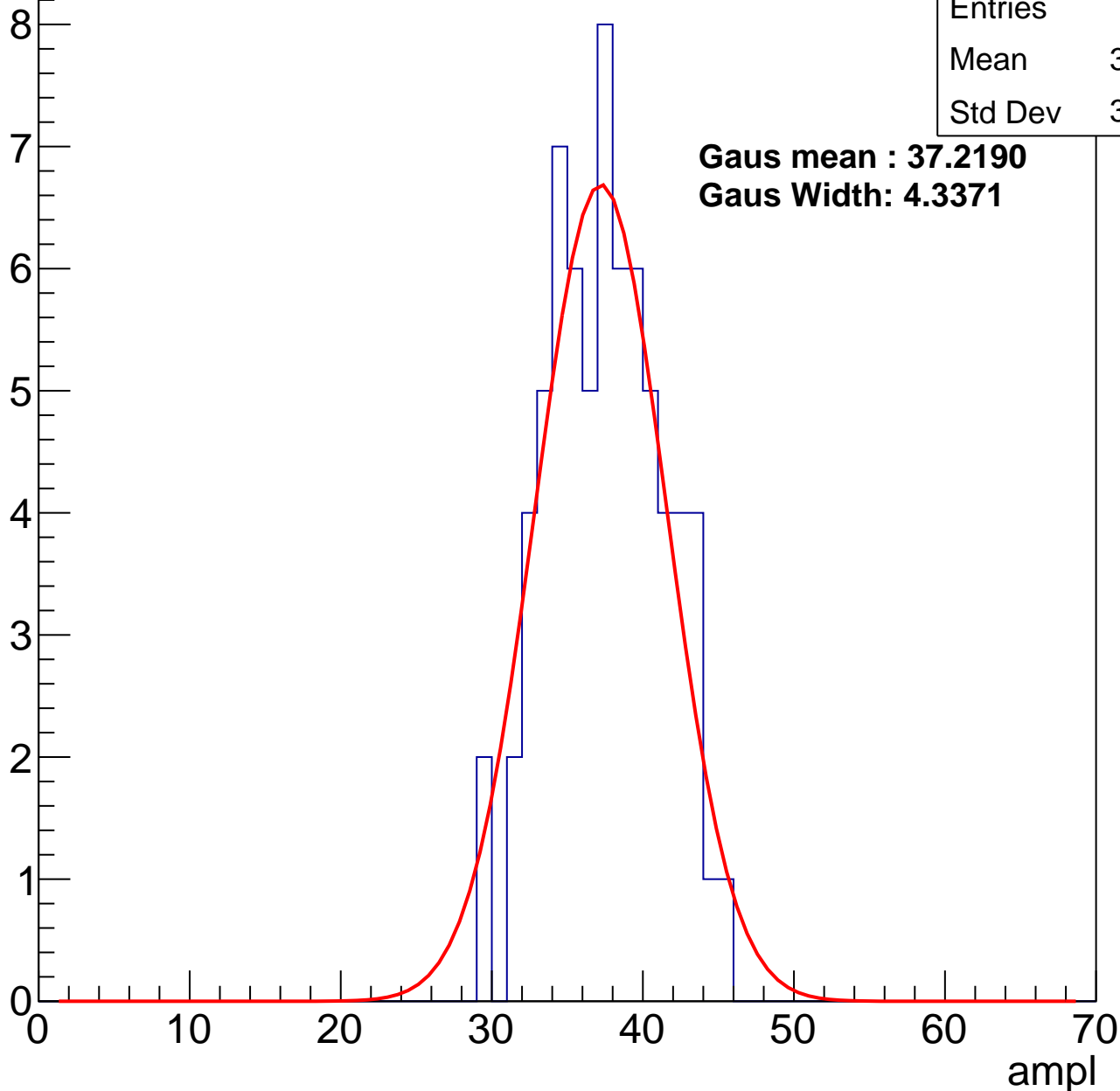
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	37.03
Std Dev	3.719

**Gaus mean : 37.2190**

**Gaus Width: 4.3371**



# B1L101S, U19-ch114, adc2

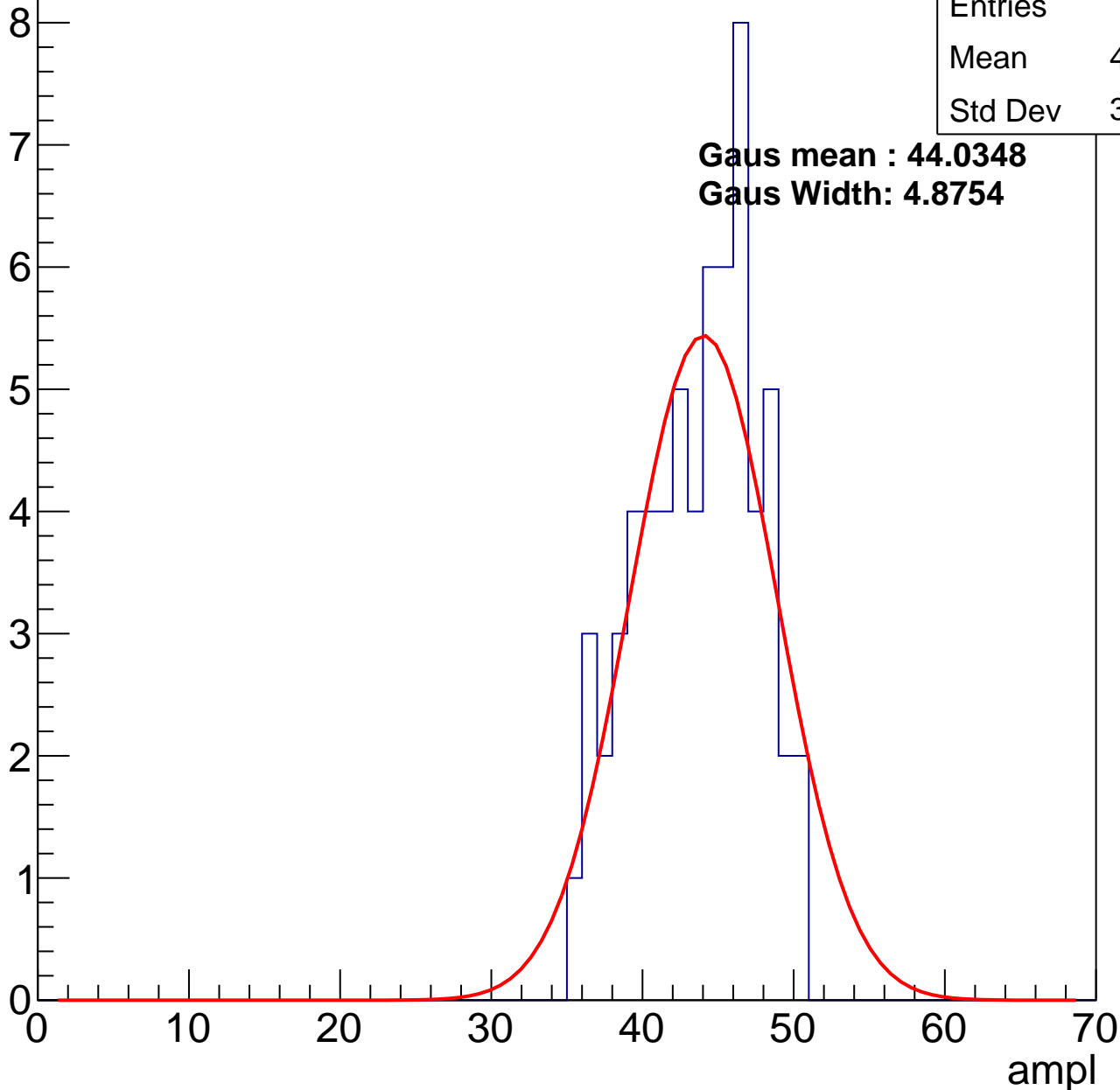
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	43.19
Std Dev	3.858

**Gaus mean : 44.0348**

**Gaus Width: 4.8754**

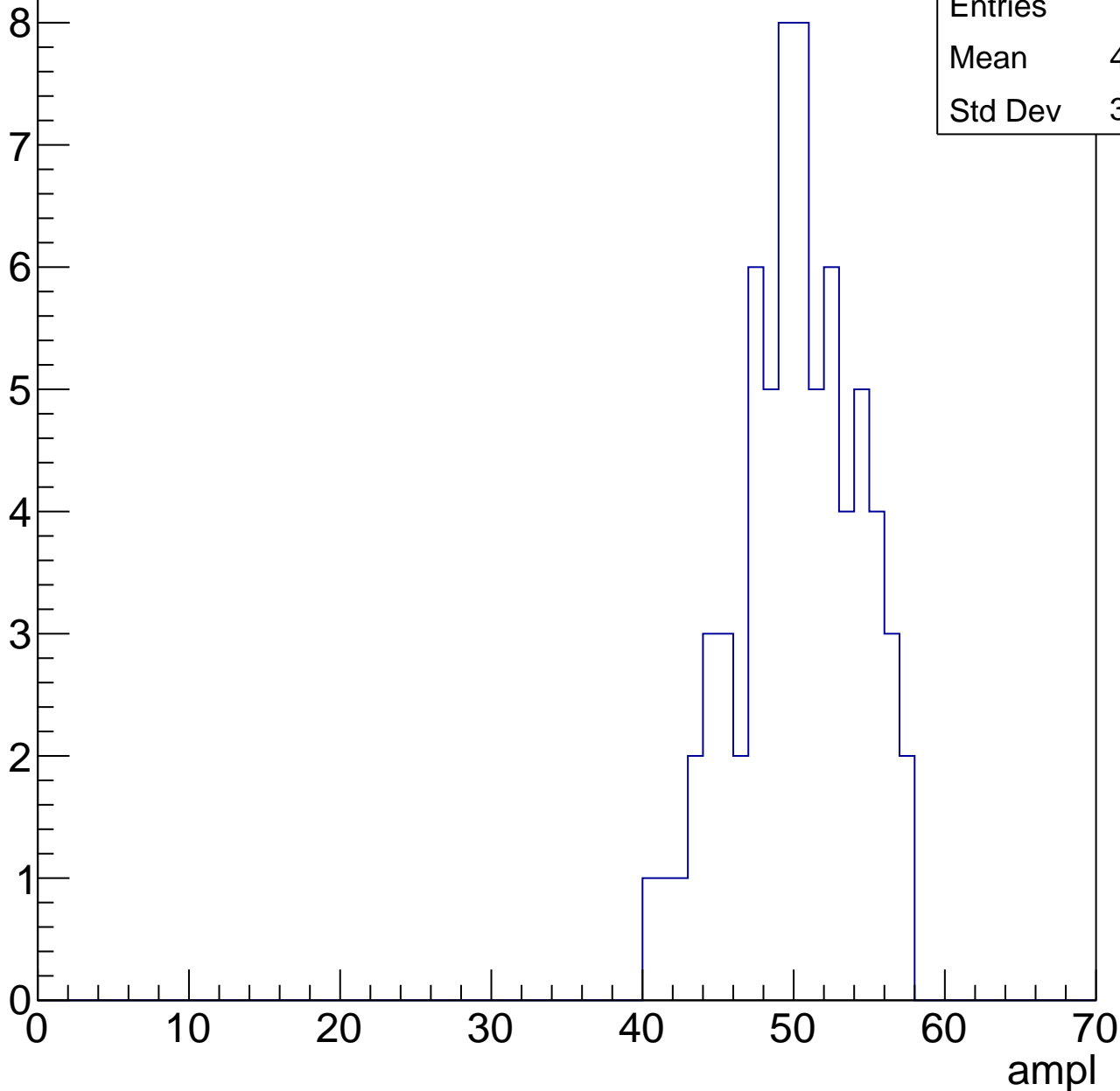


# B1L101S, U19-ch114, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

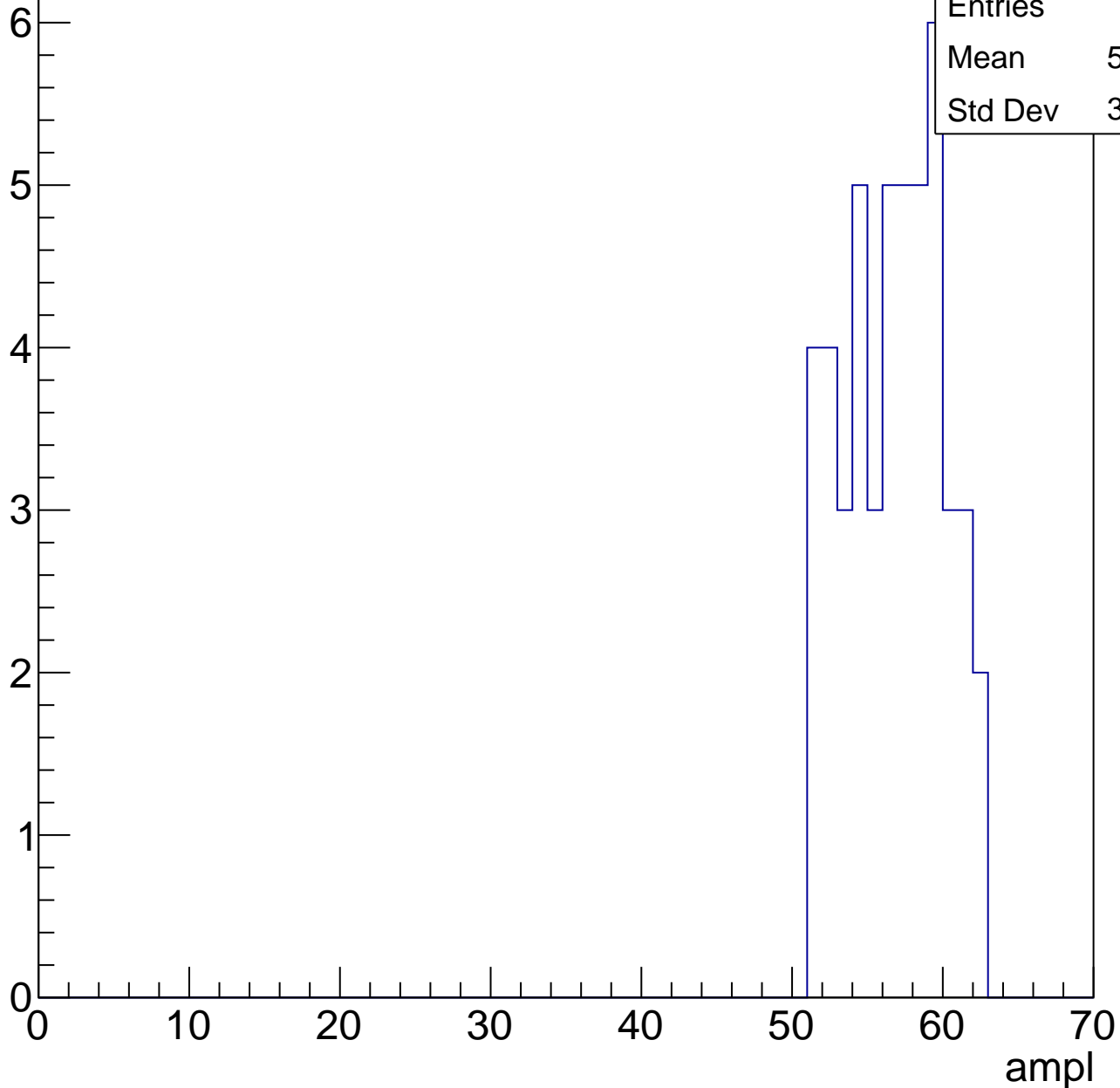
Entries	69
Mean	49.75
Std Dev	3.969



# B1L101S, U19-ch114, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

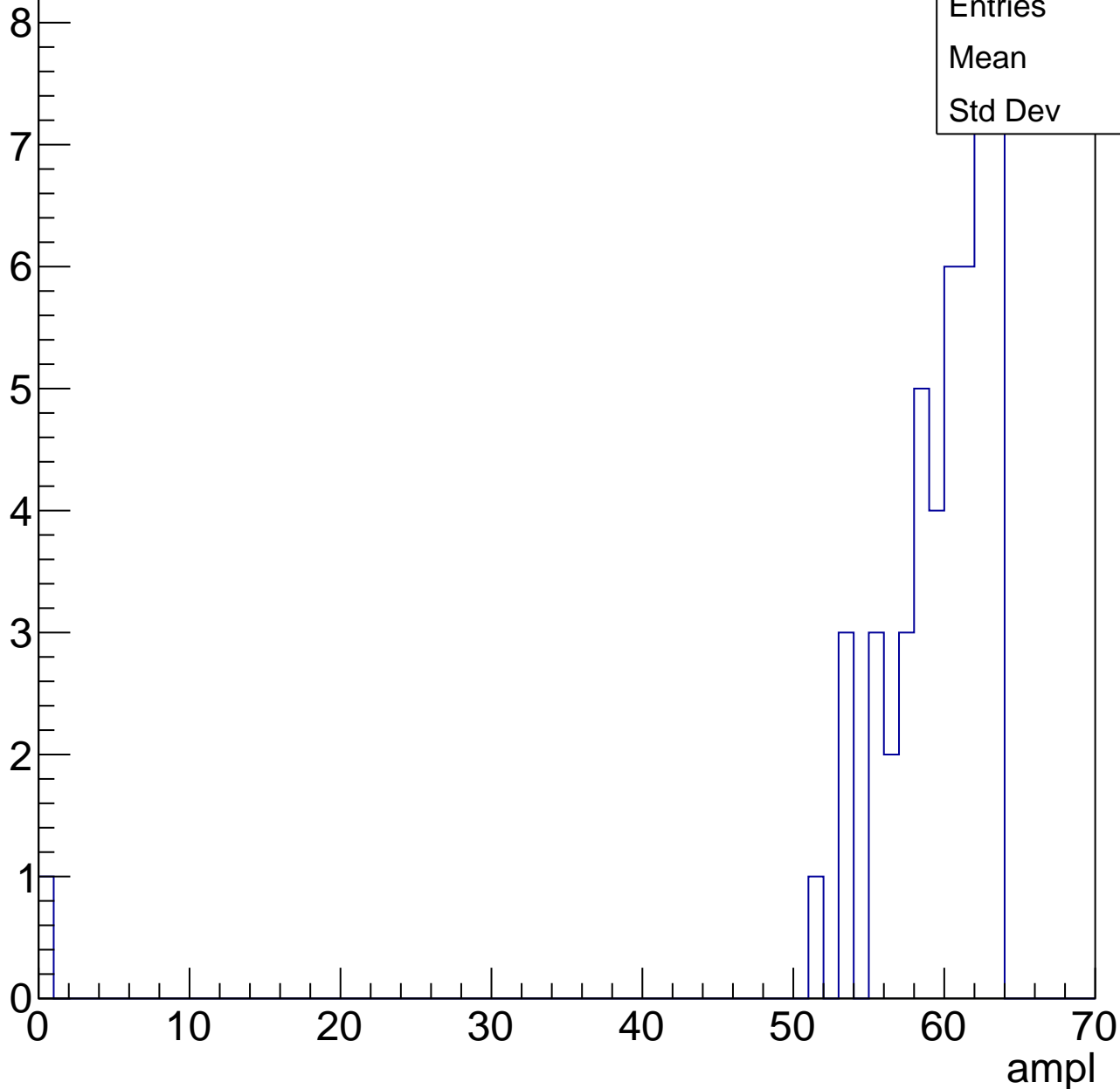


# B1L101S, U19-ch114, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	50
Mean	58.2
Std Dev	8.87



# B1L101S, U19-ch114, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U19-ch114, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U19-ch115, adc0

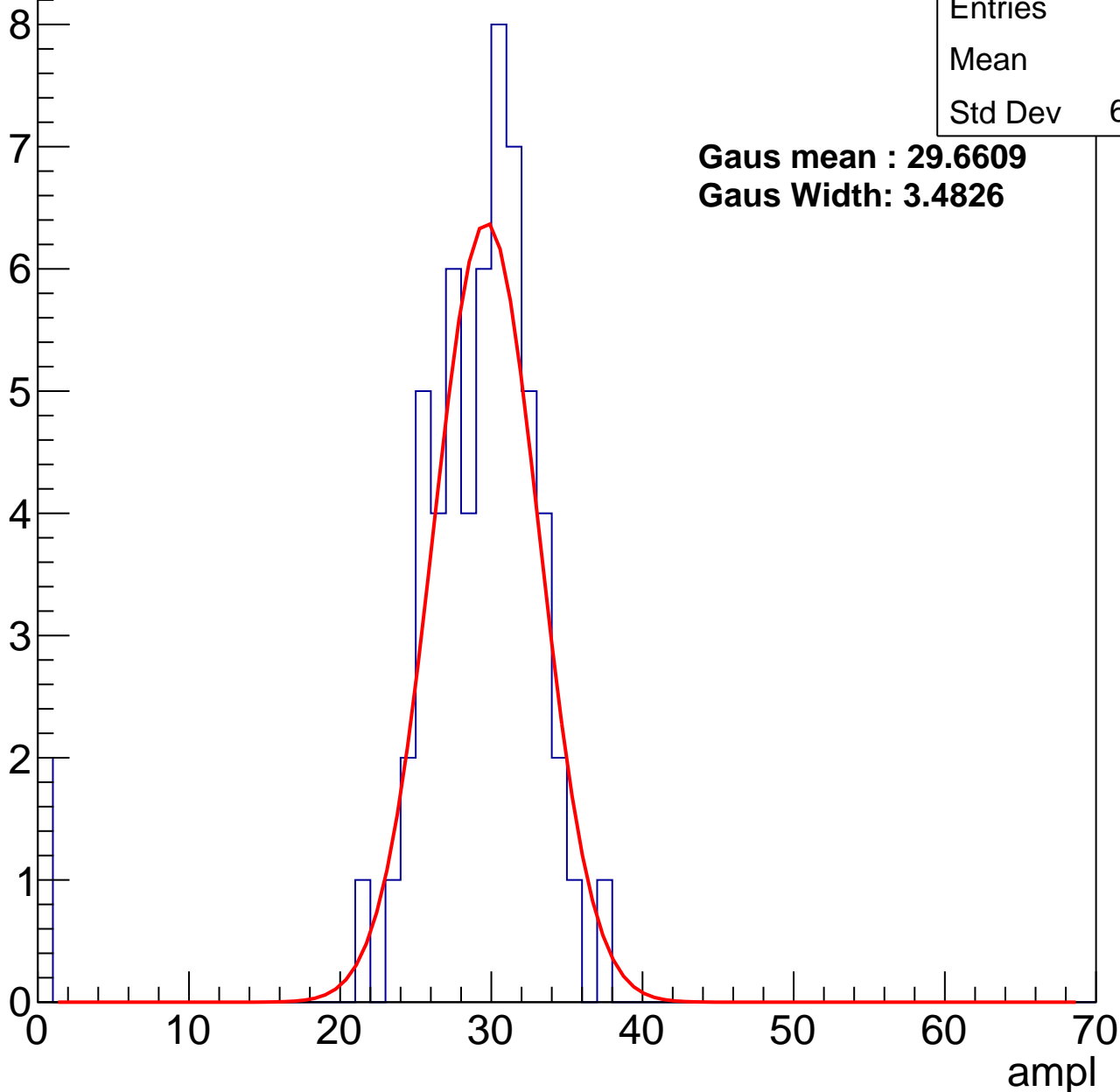
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	59
Mean	28.1
Std Dev	6.139

**Gaus mean : 29.6609**

**Gaus Width: 3.4826**



# B1L101S, U19-ch115, adc1

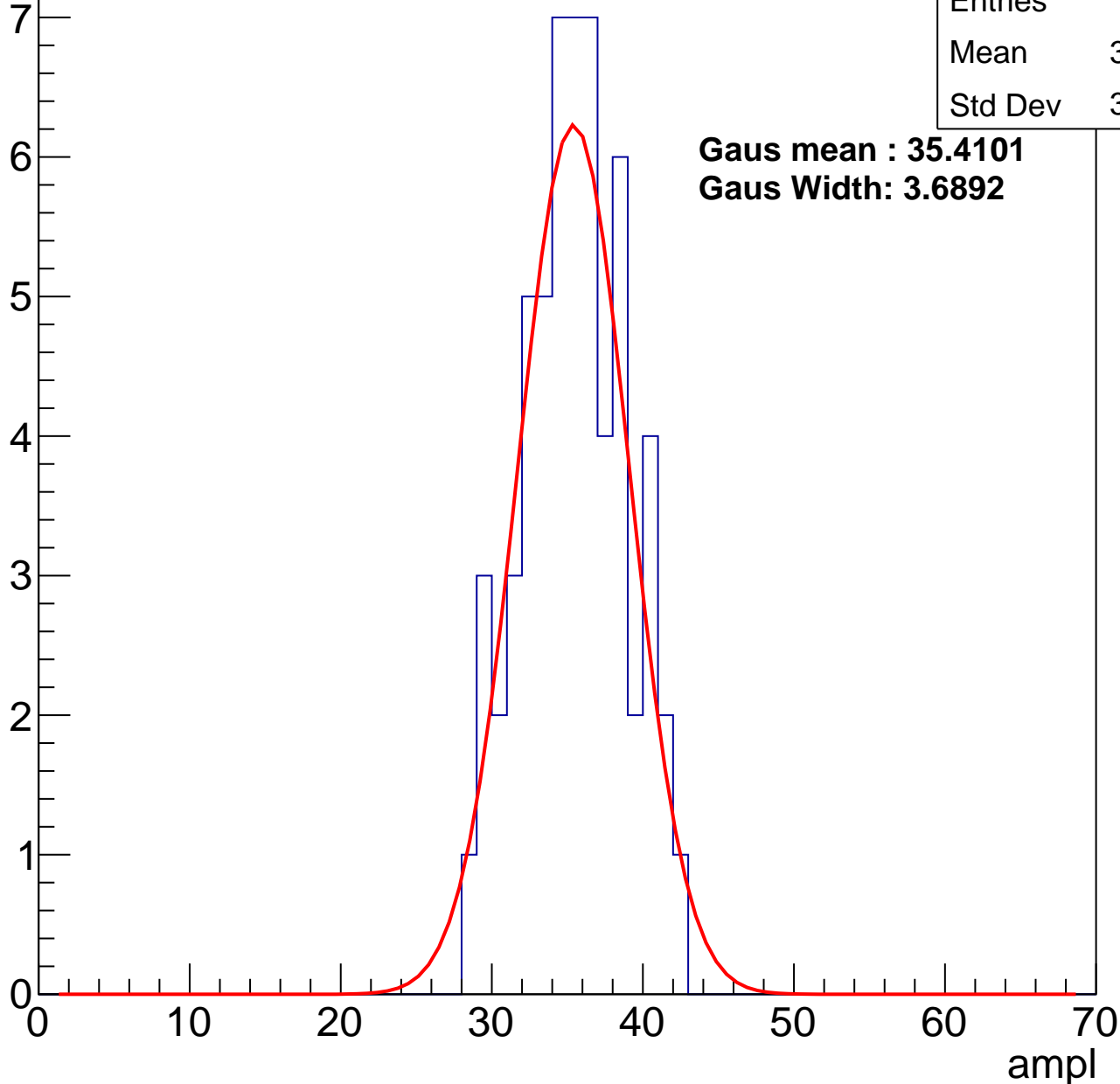
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	59
Mean	35.02
Std Dev	3.337

**Gaus mean : 35.4101**

**Gaus Width: 3.6892**



# B1L101S, U19-ch115, adc2

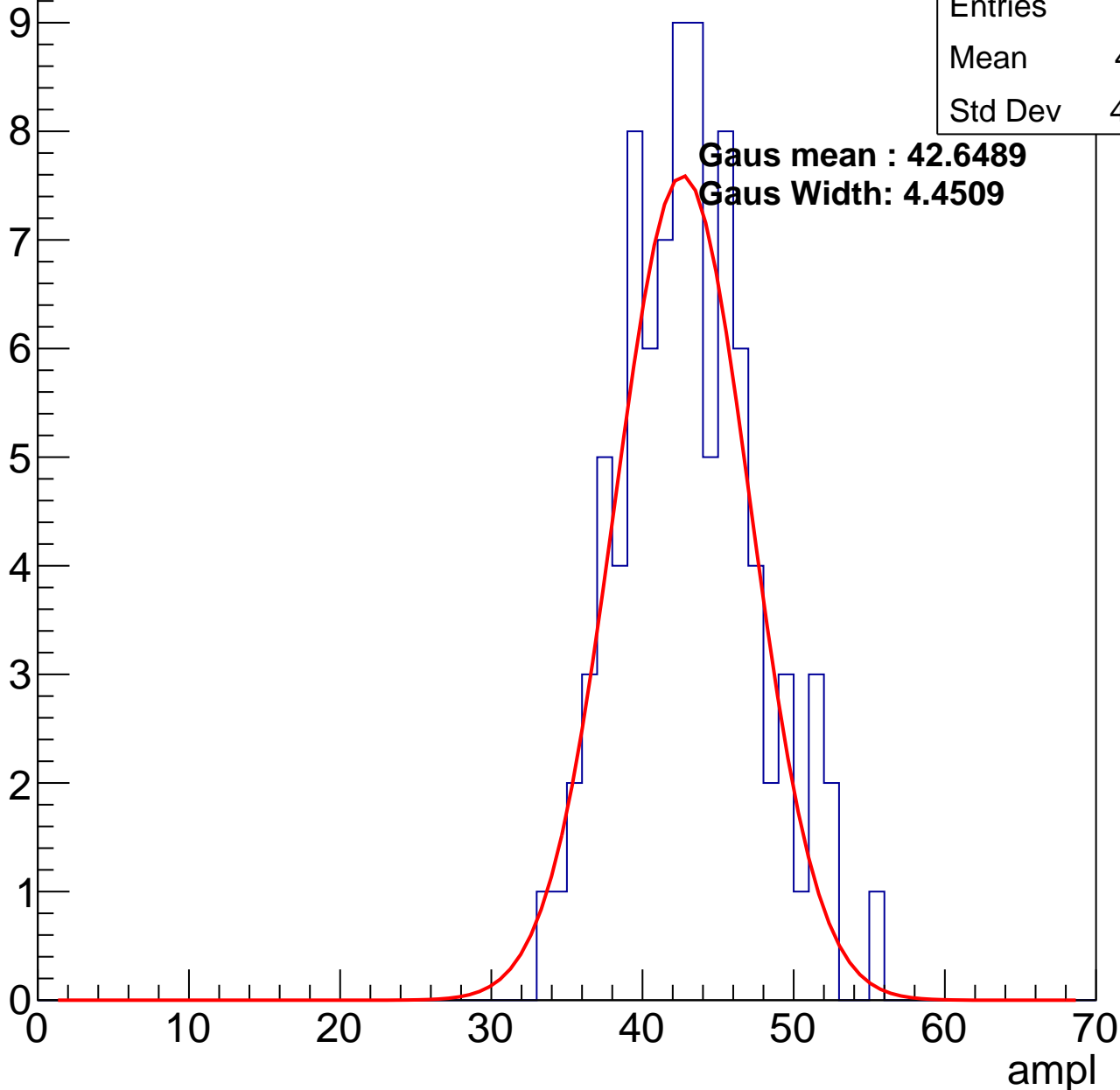
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	90
Mean	42.61
Std Dev	4.474

**Gaus mean : 42.6489**

**Gaus Width: 4.4509**

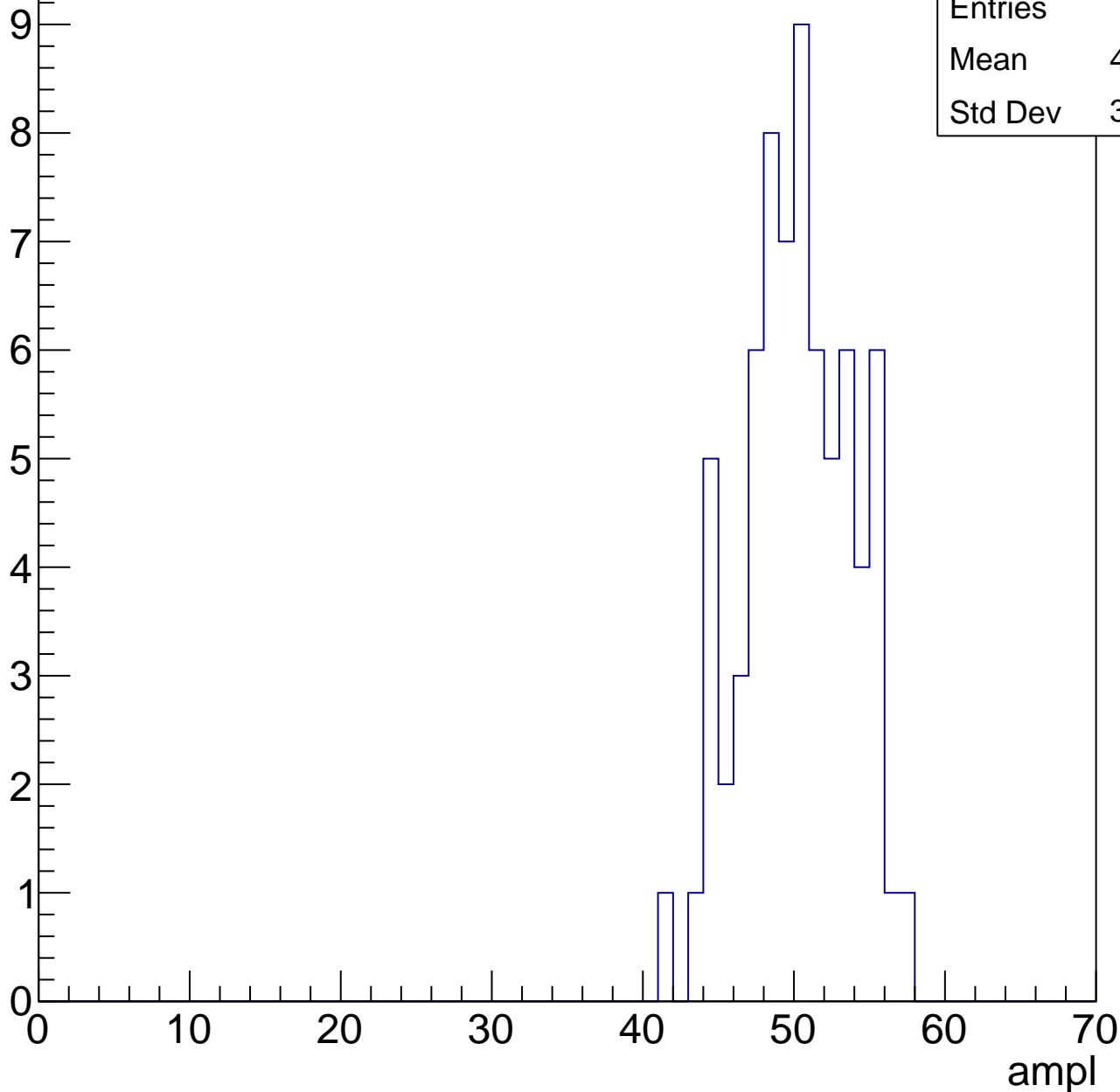


# B1L101S, U19-ch115, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	71
Mean	49.77
Std Dev	3.513

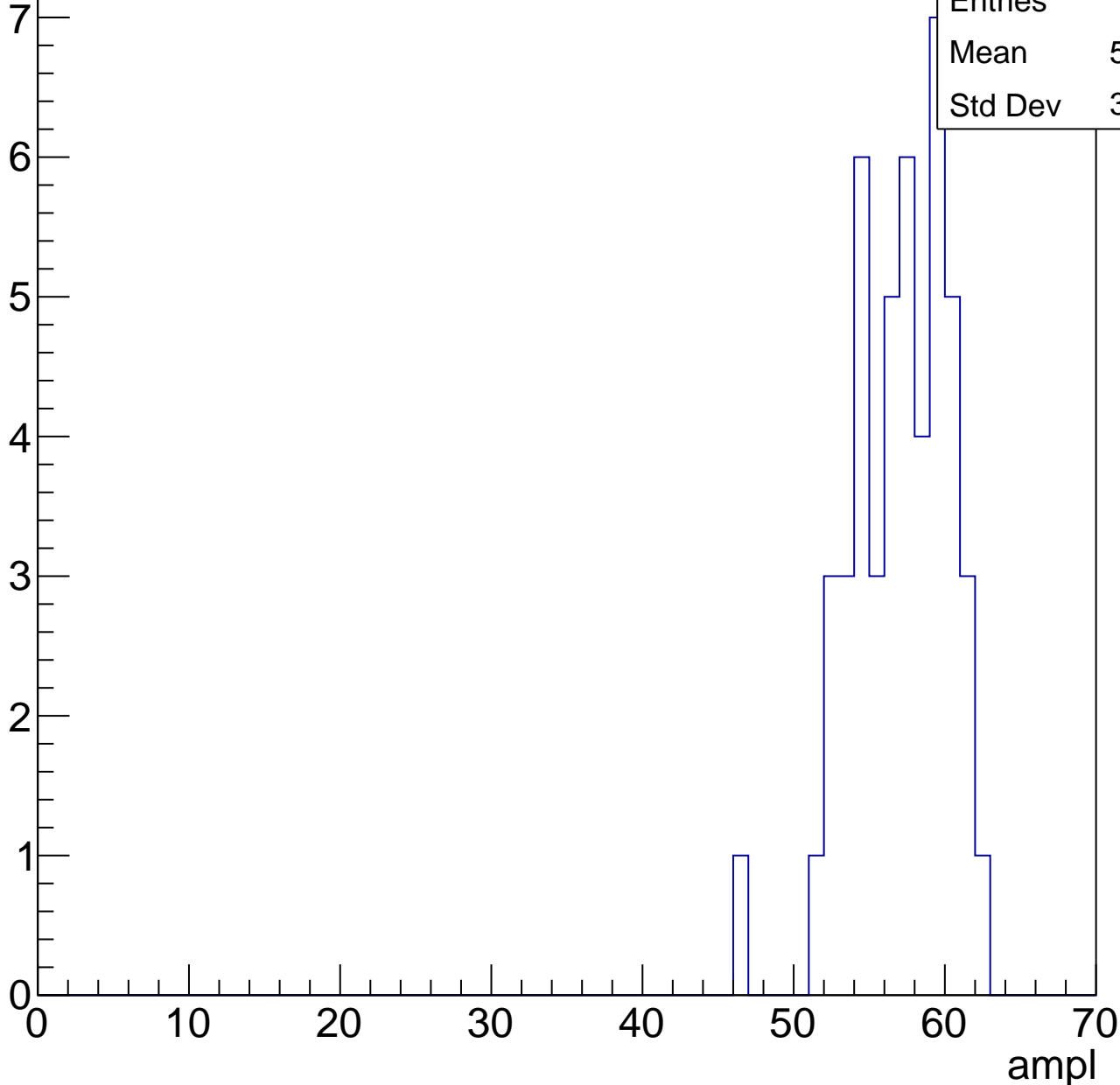


# B1L101S, U19-ch115, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	48
Mean	56.52
Std Dev	3.195

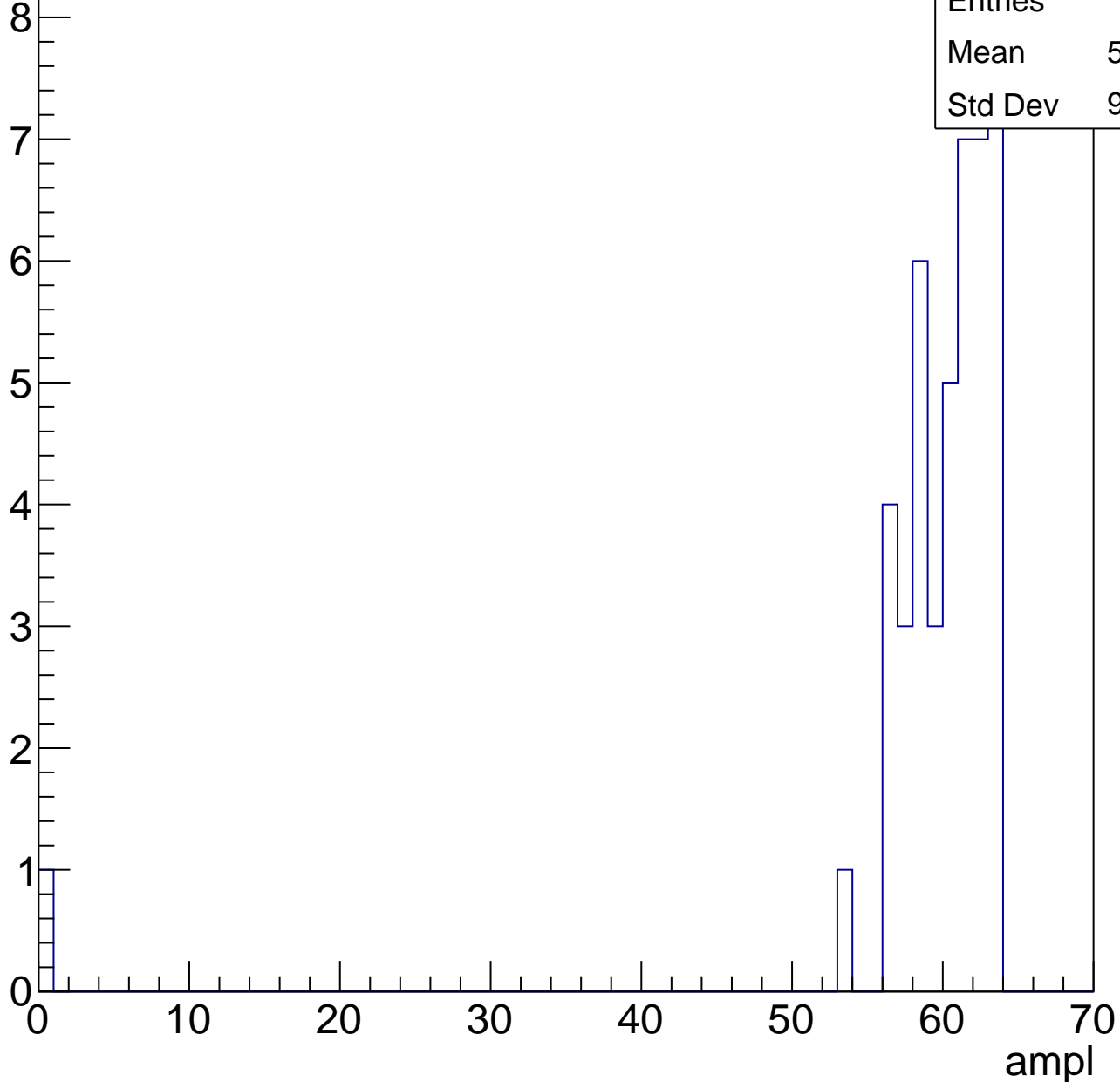


# B1L101S, U19-ch115, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	45
Mean	58.62
Std Dev	9.176



# B1L101S, U19-ch115, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	4
Mean	62.5
Std Dev	0.5

0 10 20 30 40 50 60 70

ampl



# B1L101S, U19-ch115, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U19-ch116, adc0

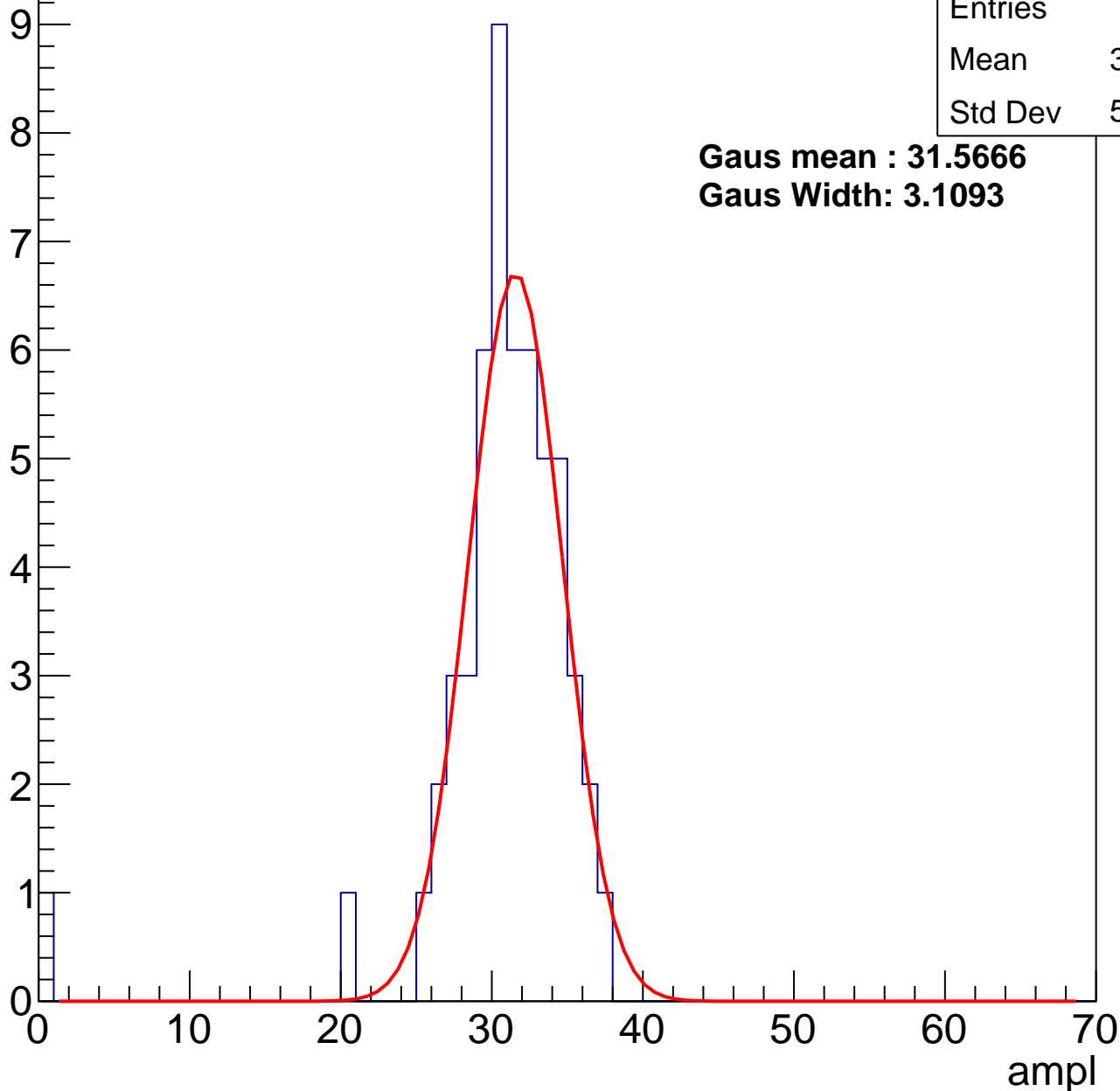
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	54
Mean	30.24
Std Dev	5.182

**Gaus mean : 31.5666**

**Gaus Width: 3.1093**



# B1L101S, U19-ch116, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

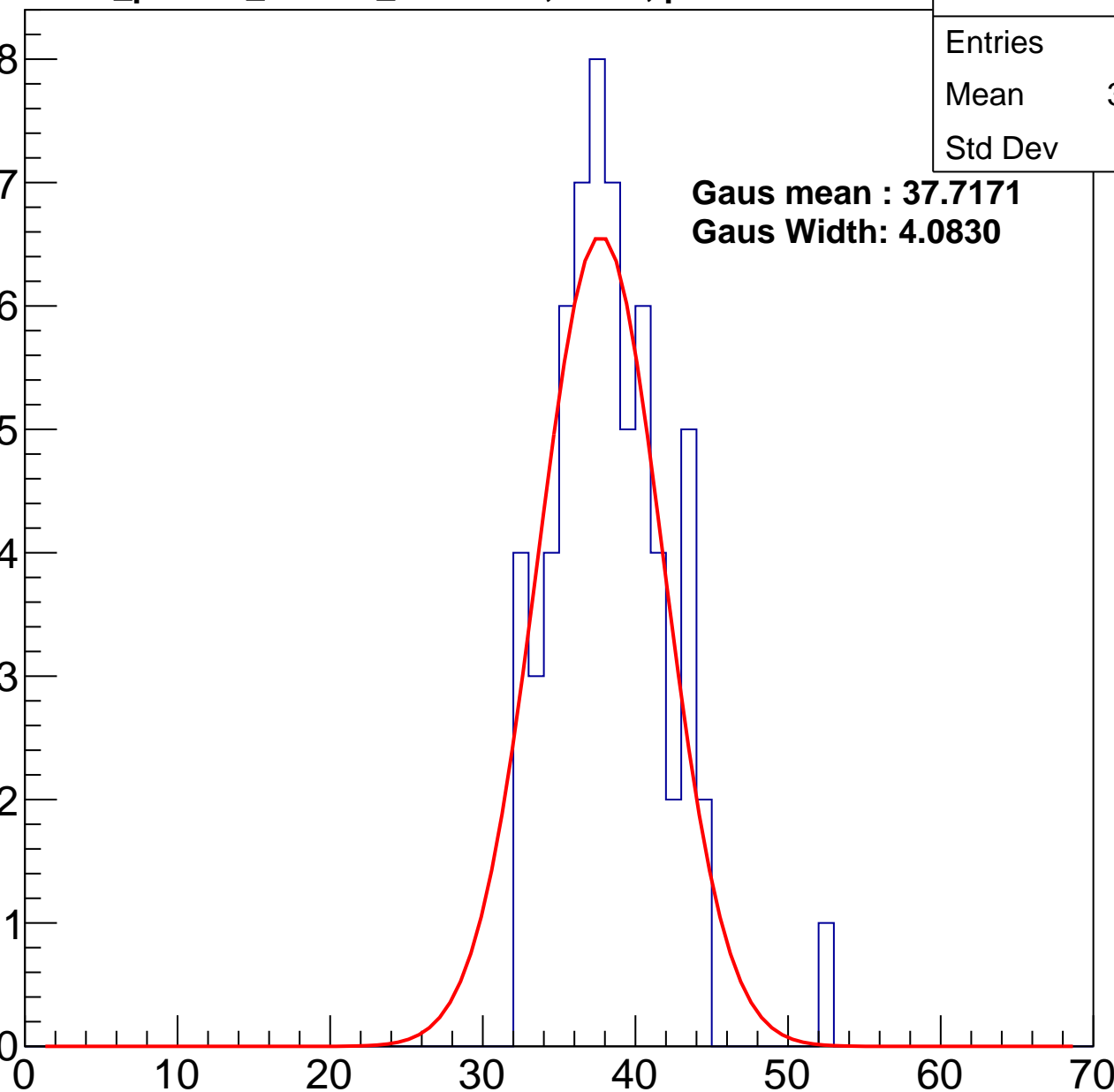
Entries	64
Mean	37.89
Std Dev	3.67

**Gaus mean : 37.7171**

**Gaus Width: 4.0830**

0  
1  
2  
3  
4  
5  
6  
7  
8

ampl



# B1L101S, U19-ch116, adc2

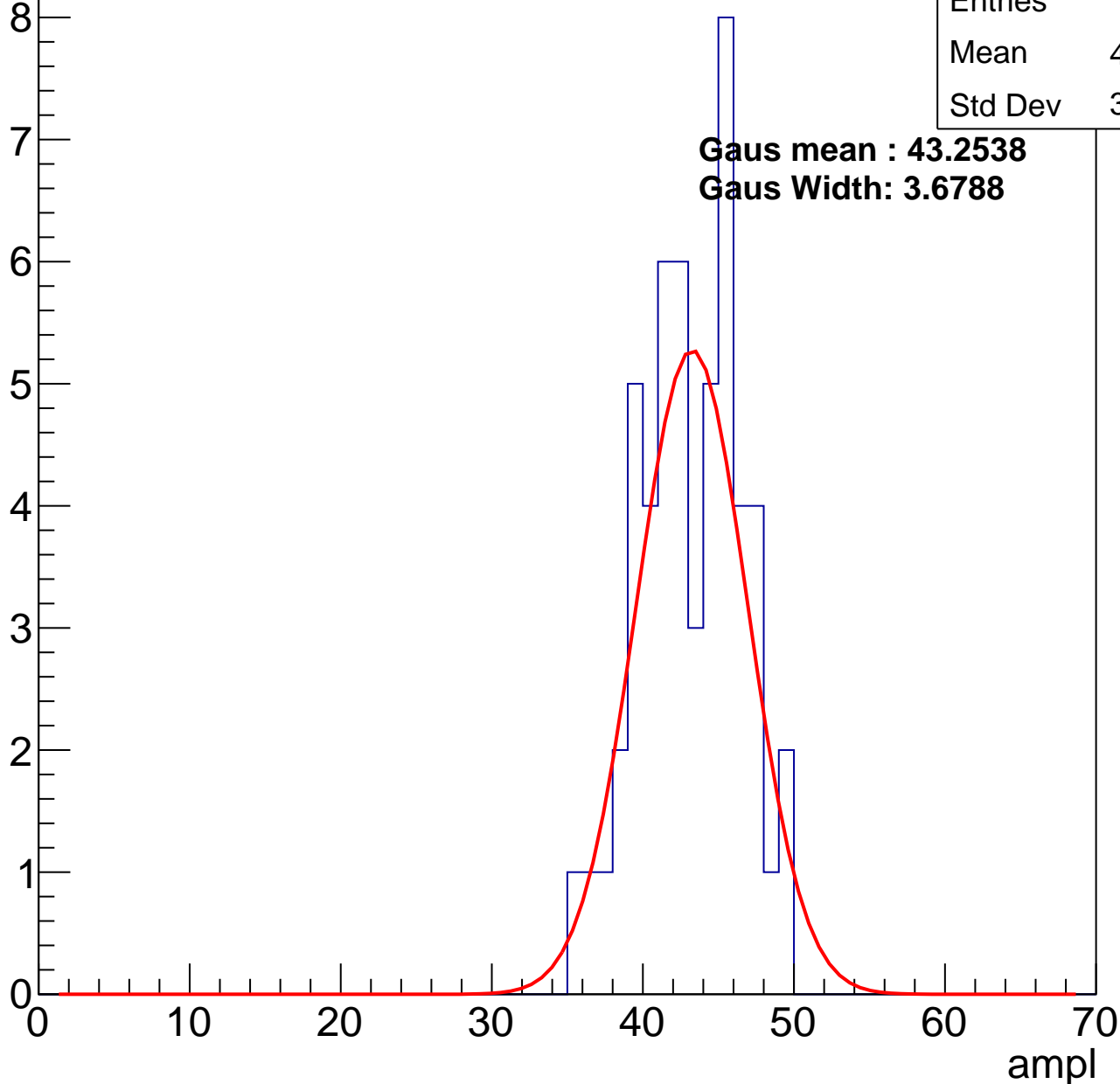
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	53
Mean	42.72
Std Dev	3.293

**Gaus mean : 43.2538**

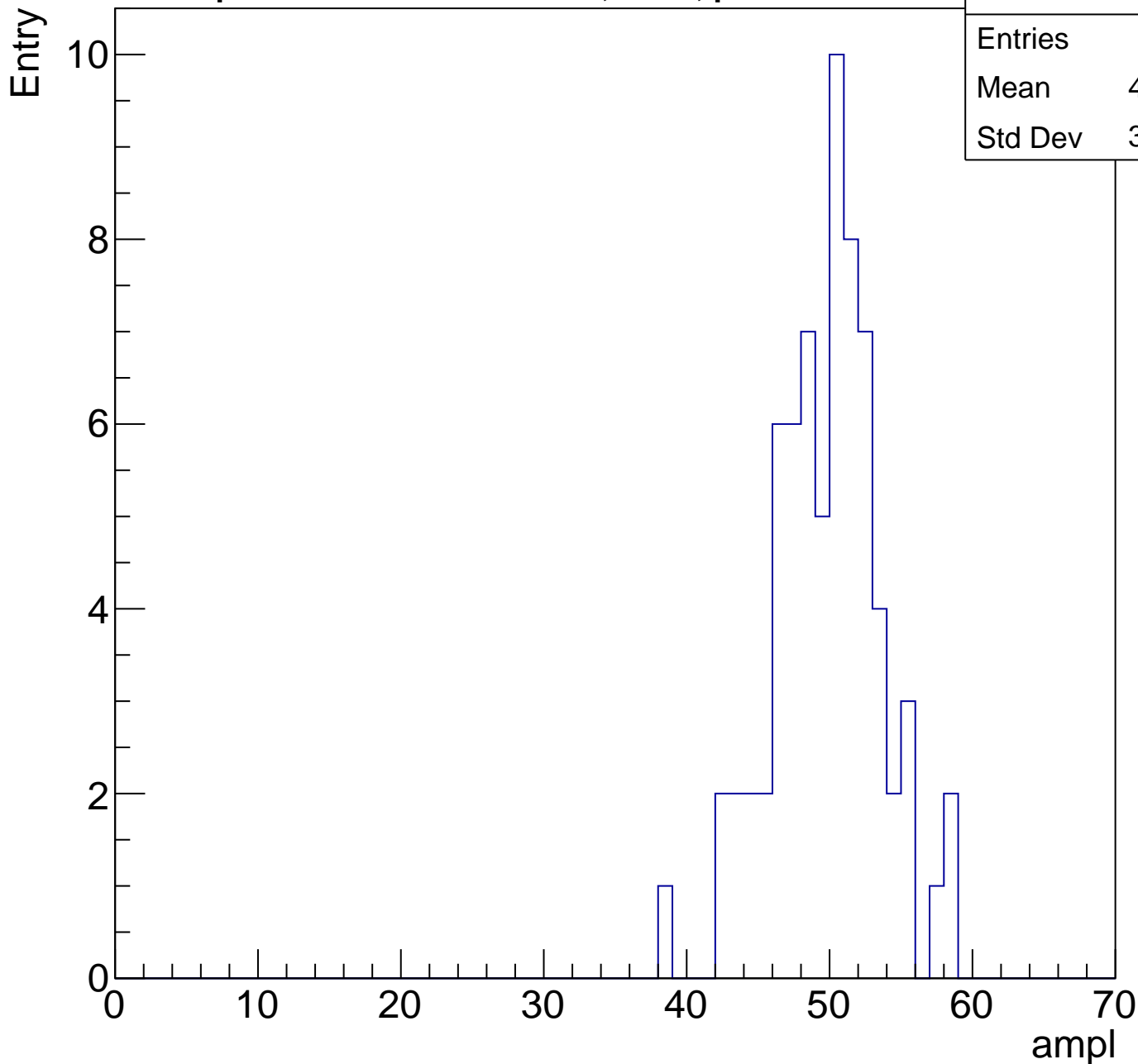
**Gaus Width: 3.6788**



# B1L101S, U19-ch116, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	70
Mean	49.36
Std Dev	3.784



# B1L101S, U19-ch116, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	73
Mean	55.95
Std Dev	3.781

Entry

10

8

6

4

2

0

0

10

20

30

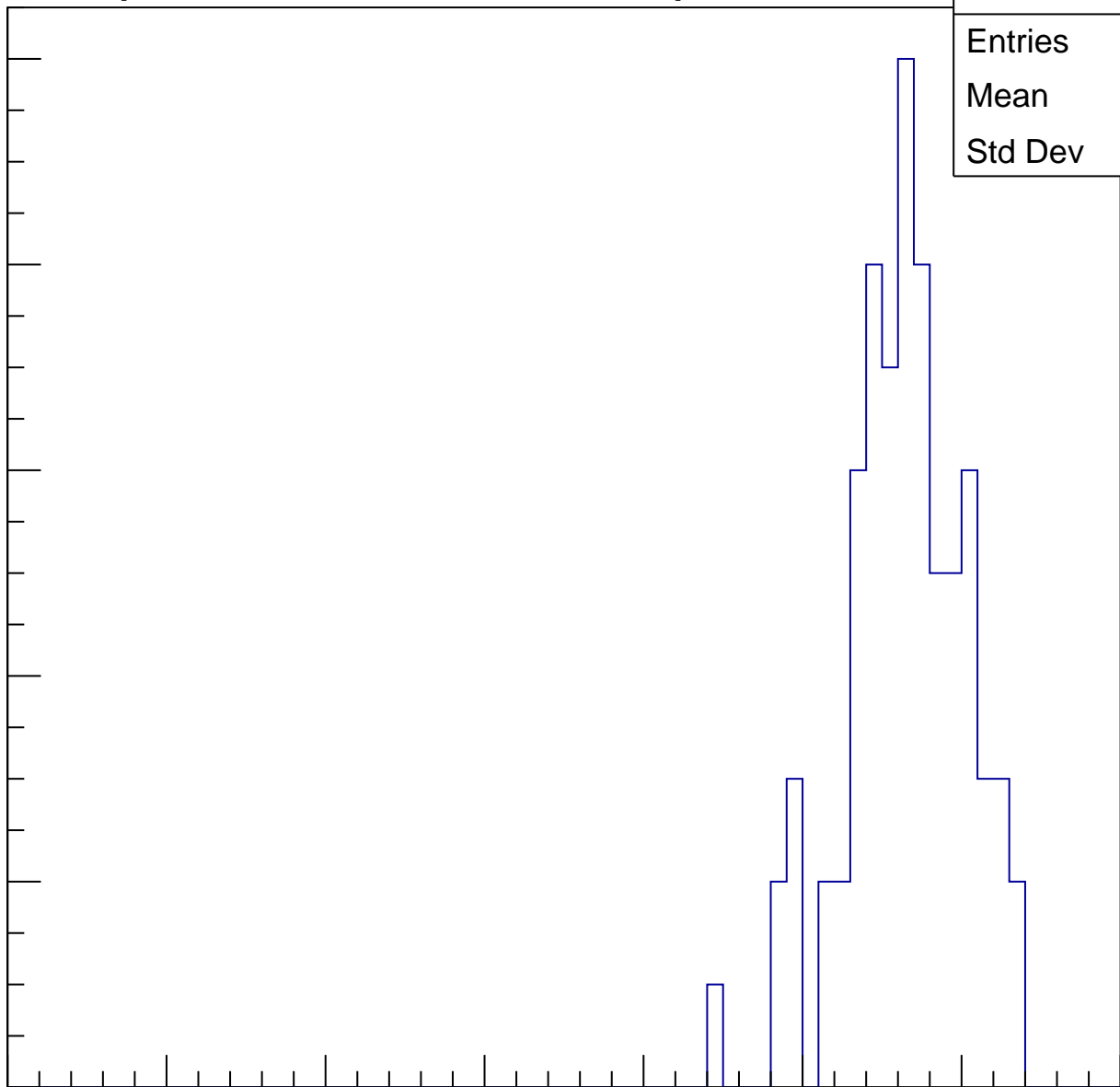
40

50

60

70

ampl

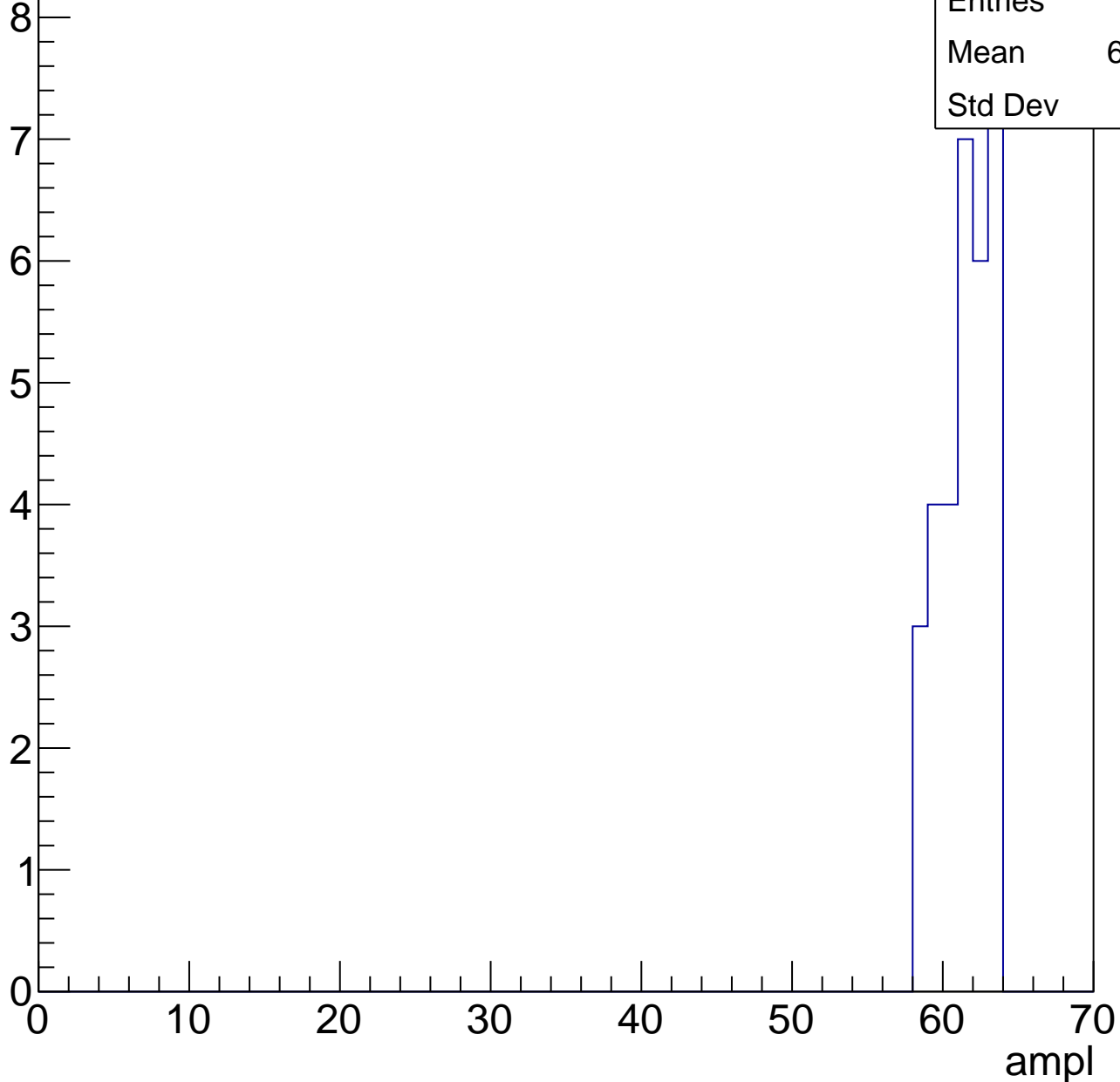


# B1L101S, U19-ch116, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

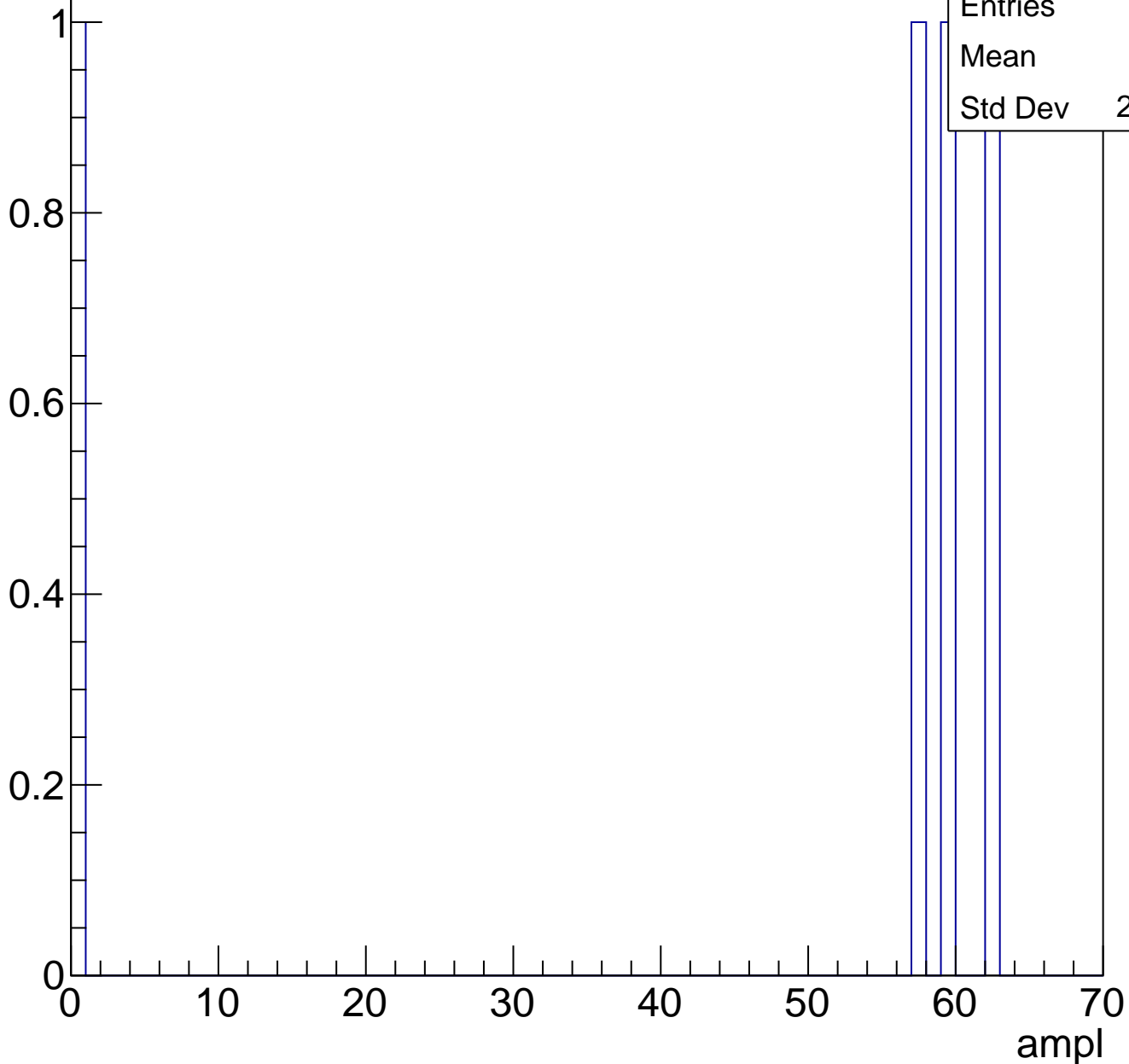
Entries	32
Mean	61.03
Std Dev	1.63



# B1L101S, U19-ch116, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U19-ch116, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L101S, U19-ch117, adc0

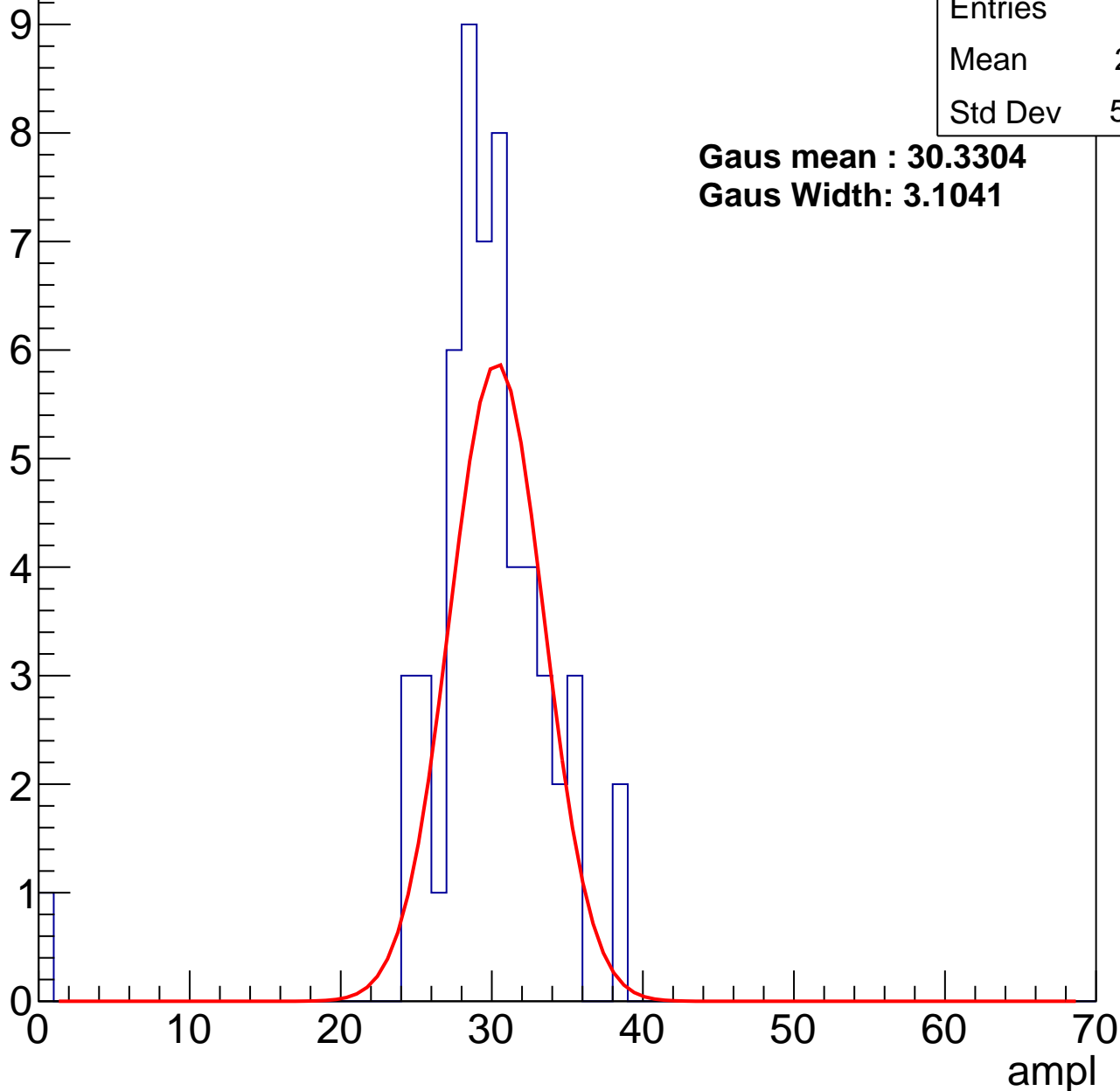
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	56
Mean	29.11
Std Dev	5.059

**Gaus mean : 30.3304**

**Gaus Width: 3.1041**



# B1L101S, U19-ch117, adc1

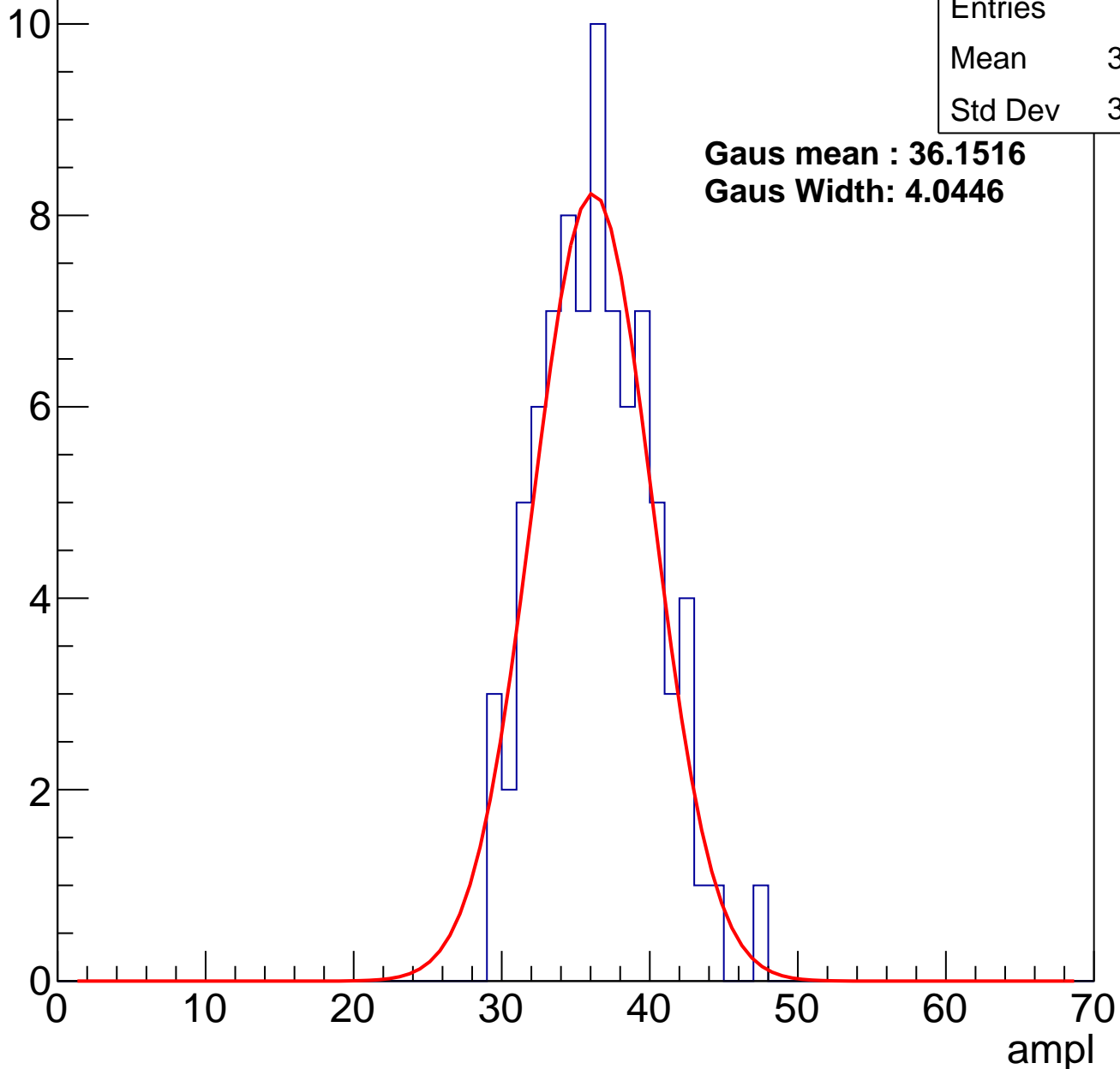
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	83
Mean	35.99
Std Dev	3.753

**Gaus mean : 36.1516**

**Gaus Width: 4.0446**

Entry



# B1L101S, U19-ch117, adc2

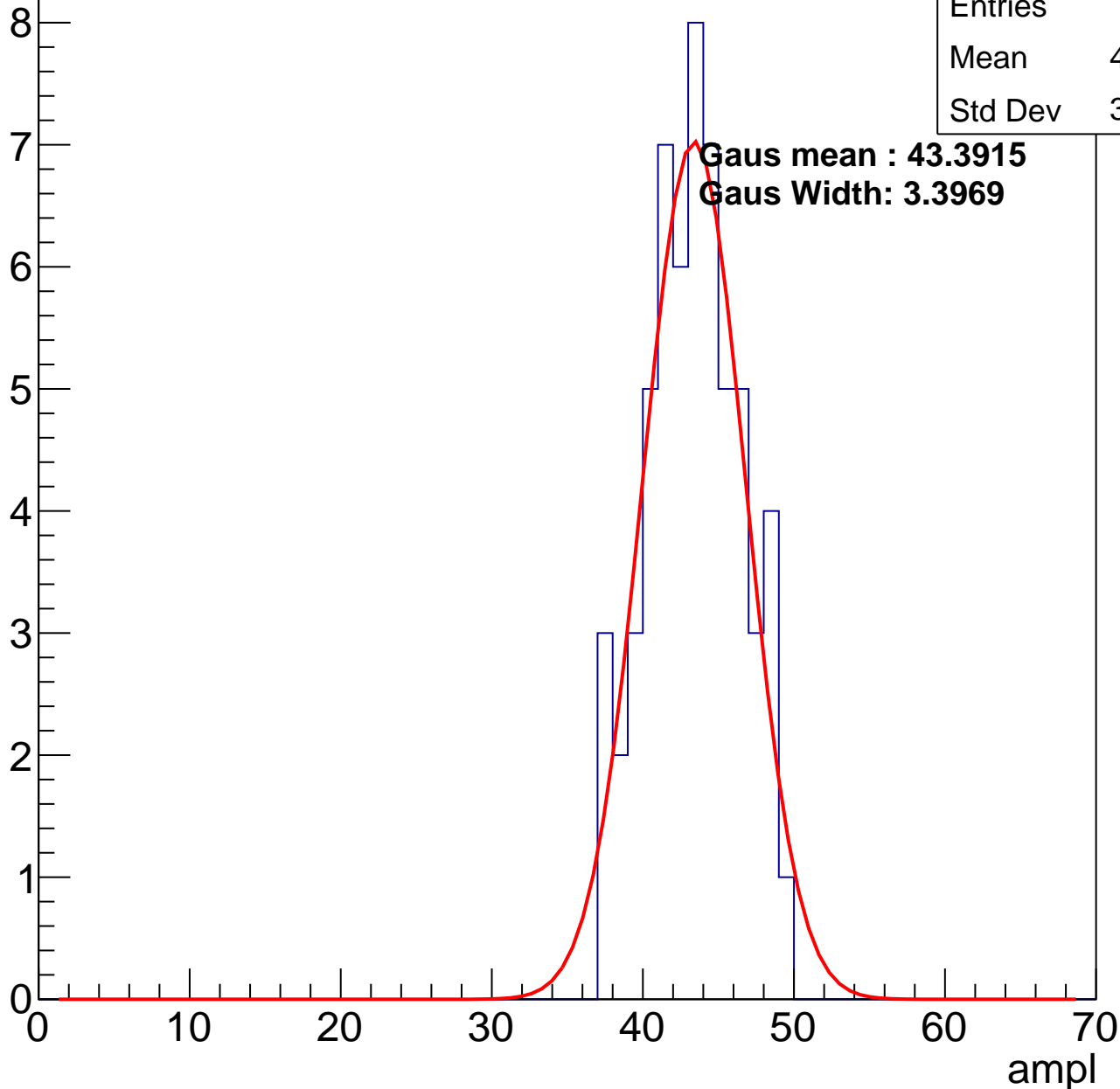
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	59
Mean	42.92
Std Dev	3.027

**Gaus mean : 43.3915**

**Gaus Width: 3.3969**

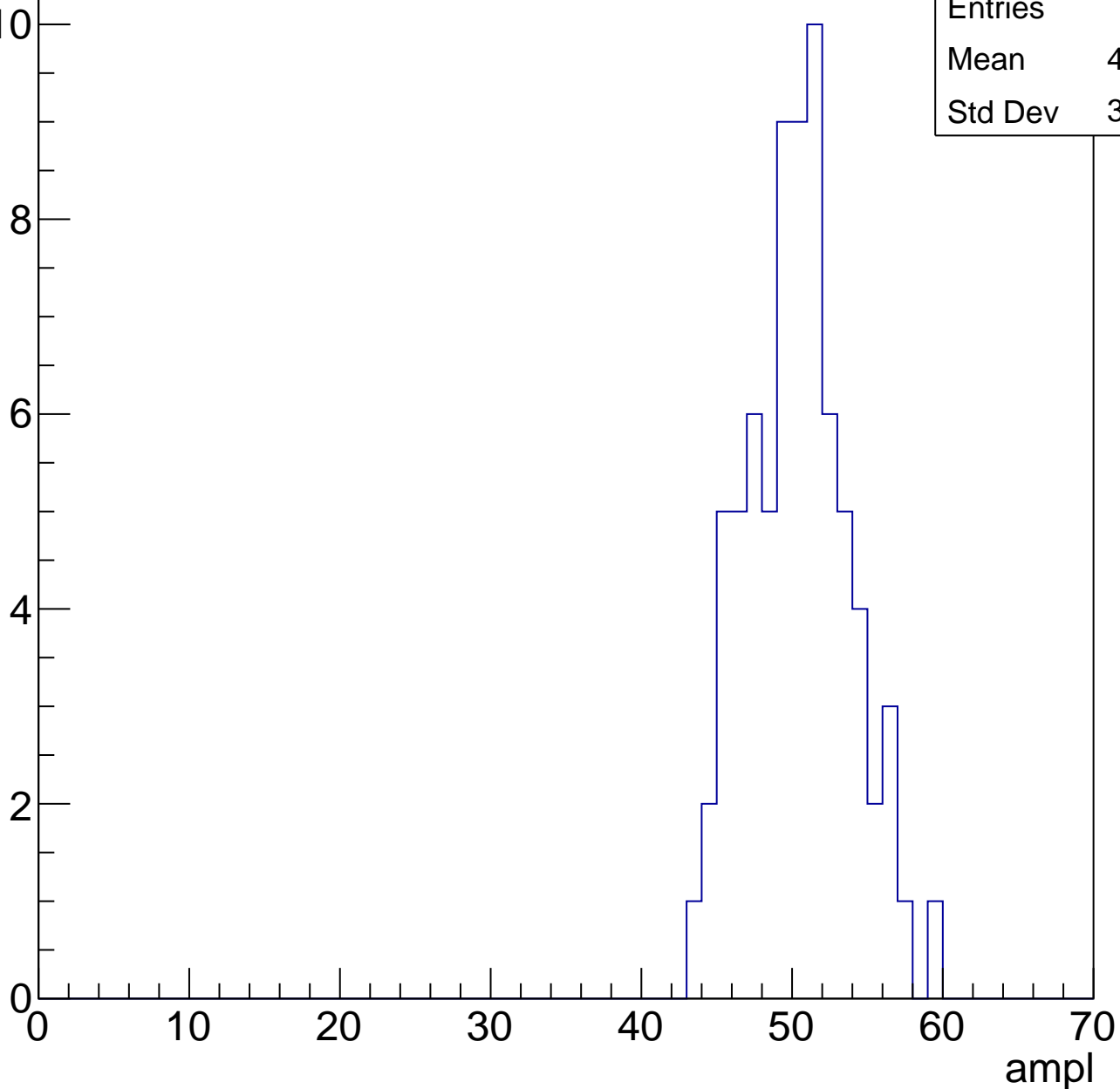


# B1L101S, U19-ch117, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	74
Mean	49.95
Std Dev	3.369

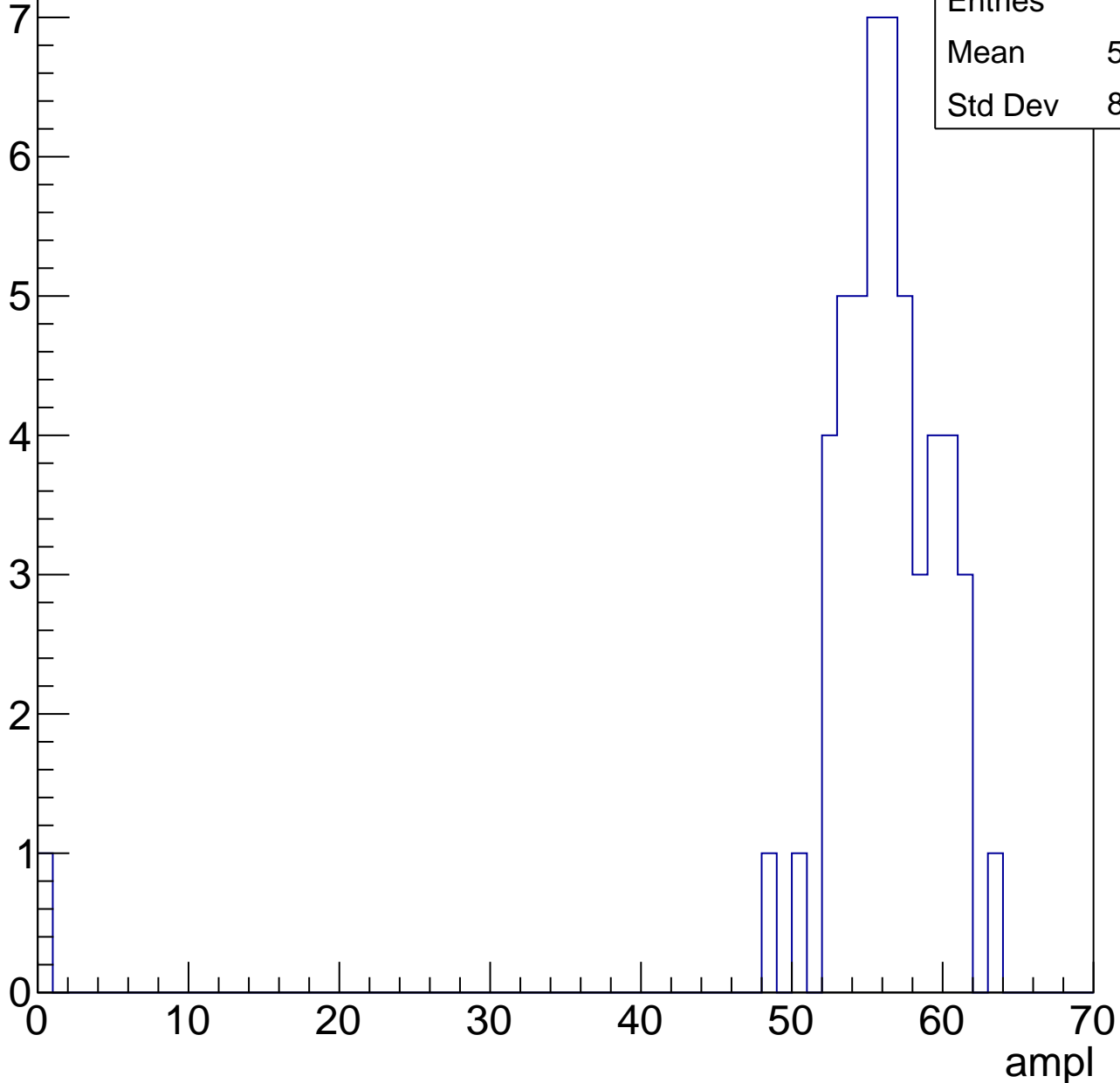


# B1L101S, U19-ch117, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	51
Mean	54.88
Std Dev	8.342

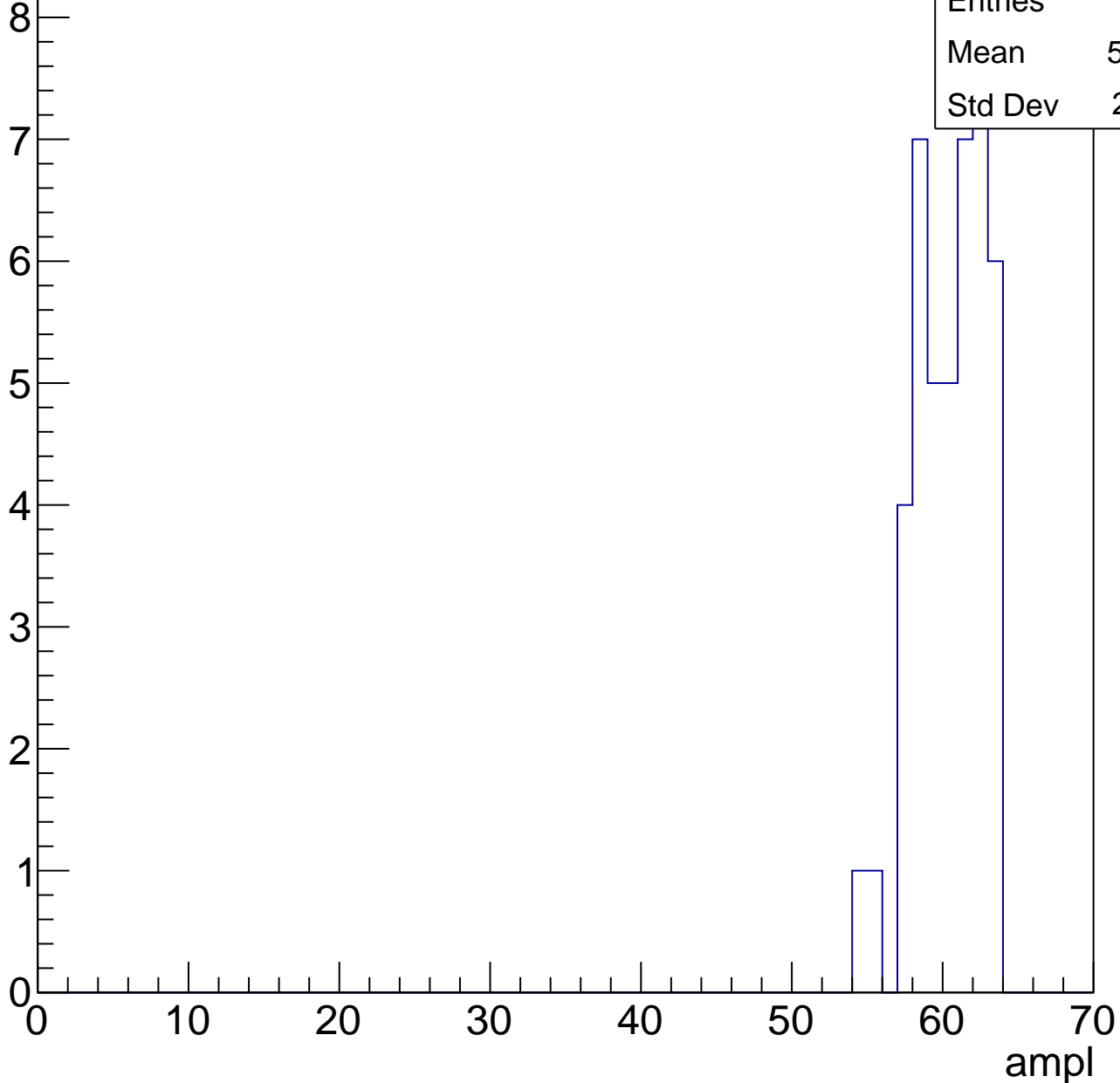


# B1L101S, U19-ch117, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

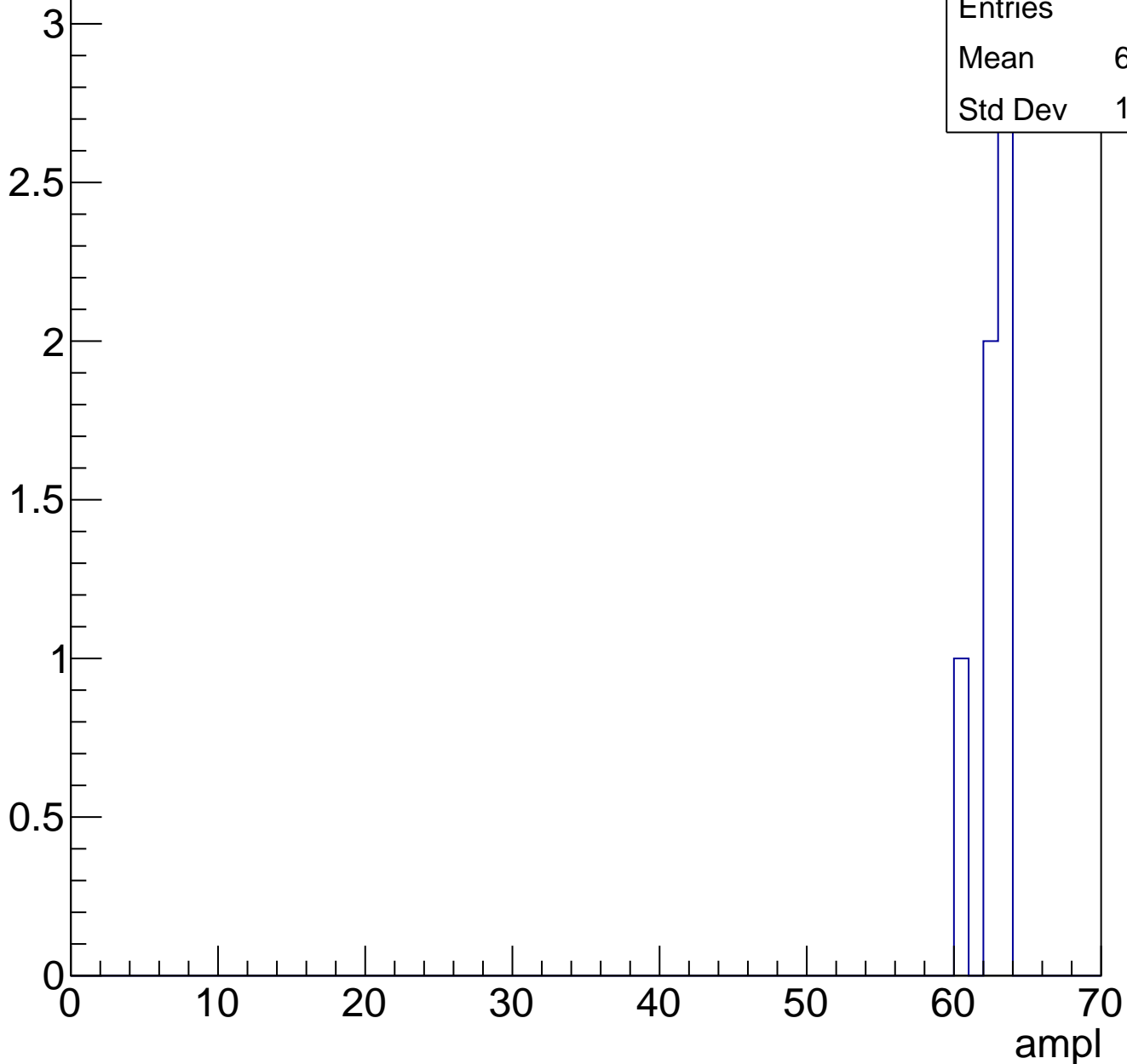
Entries	44
Mean	59.98
Std Dev	2.251



# B1L101S, U19-ch117, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U19-ch117, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U19-ch118, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	83
Mean	27.45
Std Dev	4.936

**Gaus mean : 28.1916**

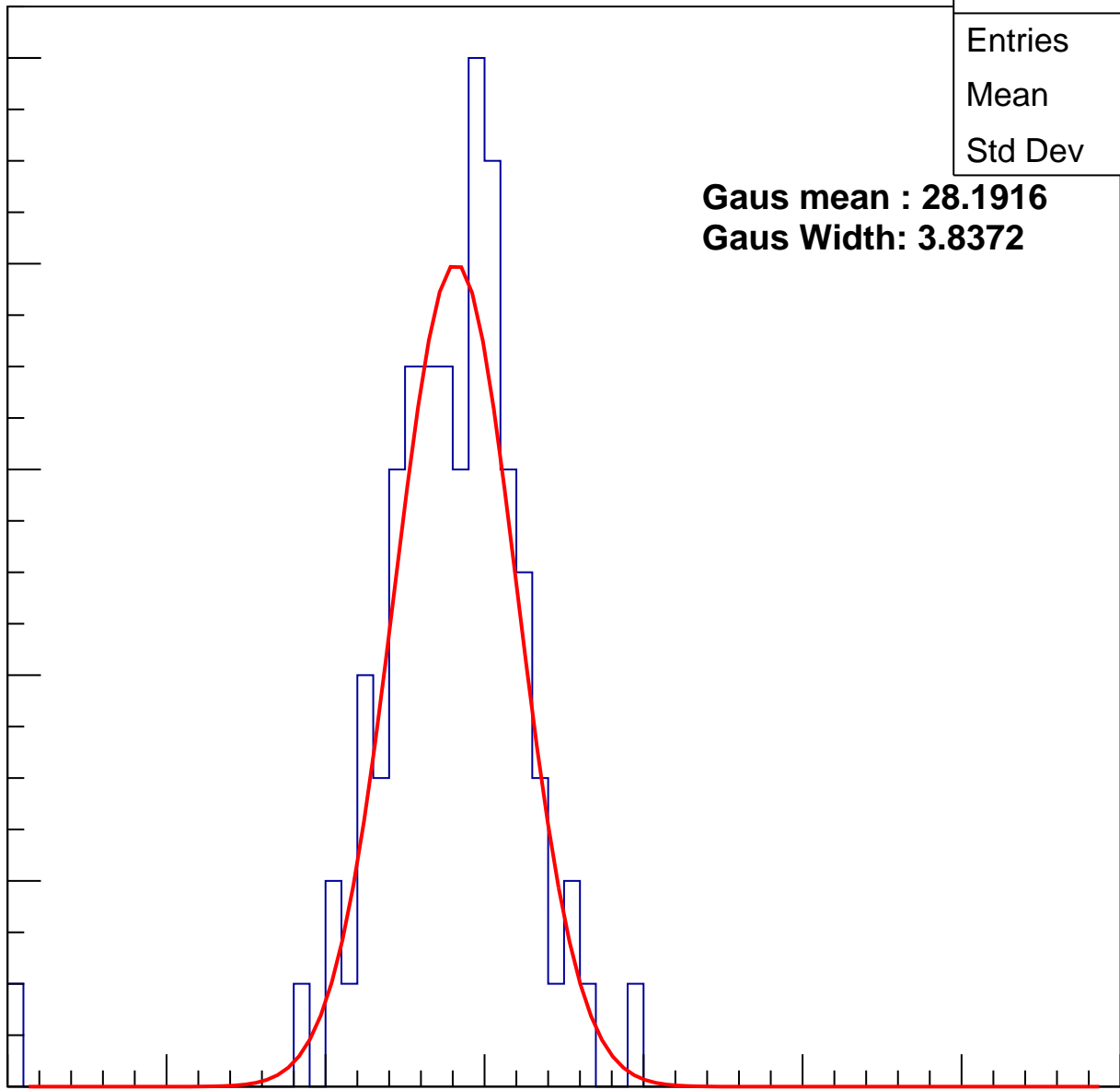
**Gaus Width: 3.8372**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U19-ch118, adc1

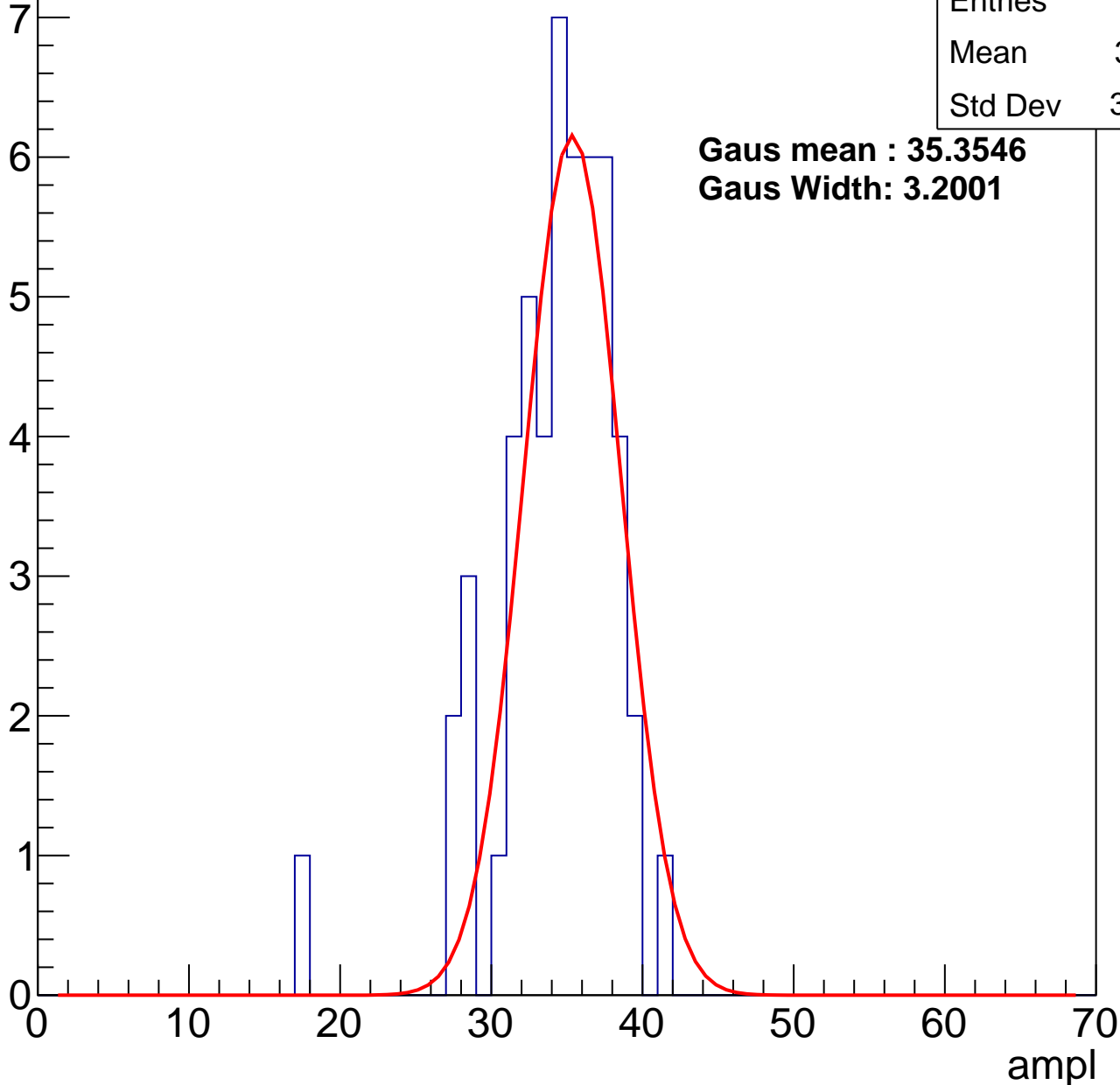
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	52
Mean	33.81
Std Dev	3.962

**Gaus mean : 35.3546**

**Gaus Width: 3.2001**



# B1L101S, U19-ch118, adc2

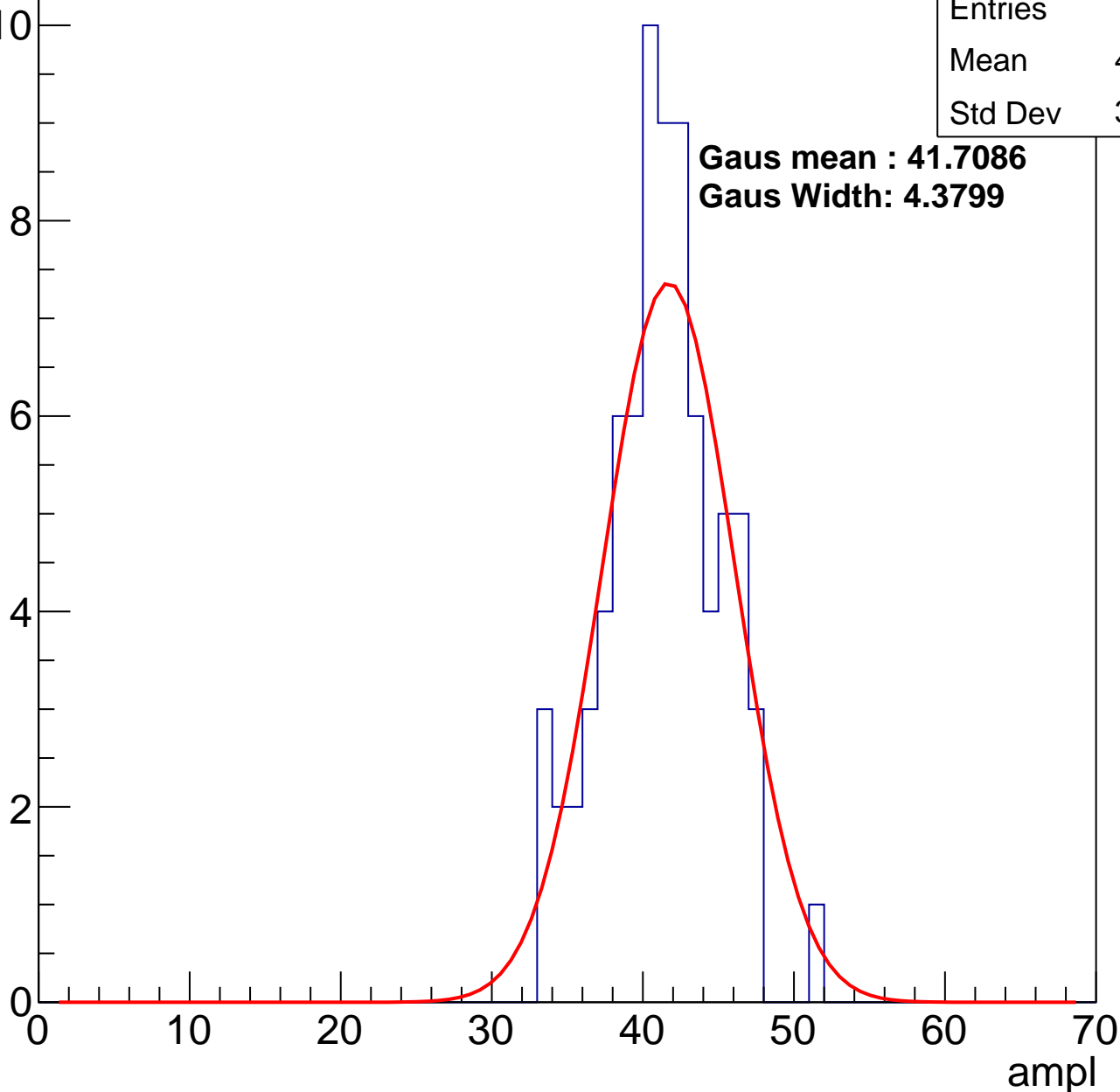
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	78
Mean	40.81
Std Dev	3.701

**Gaus mean : 41.7086**

**Gaus Width: 4.3799**

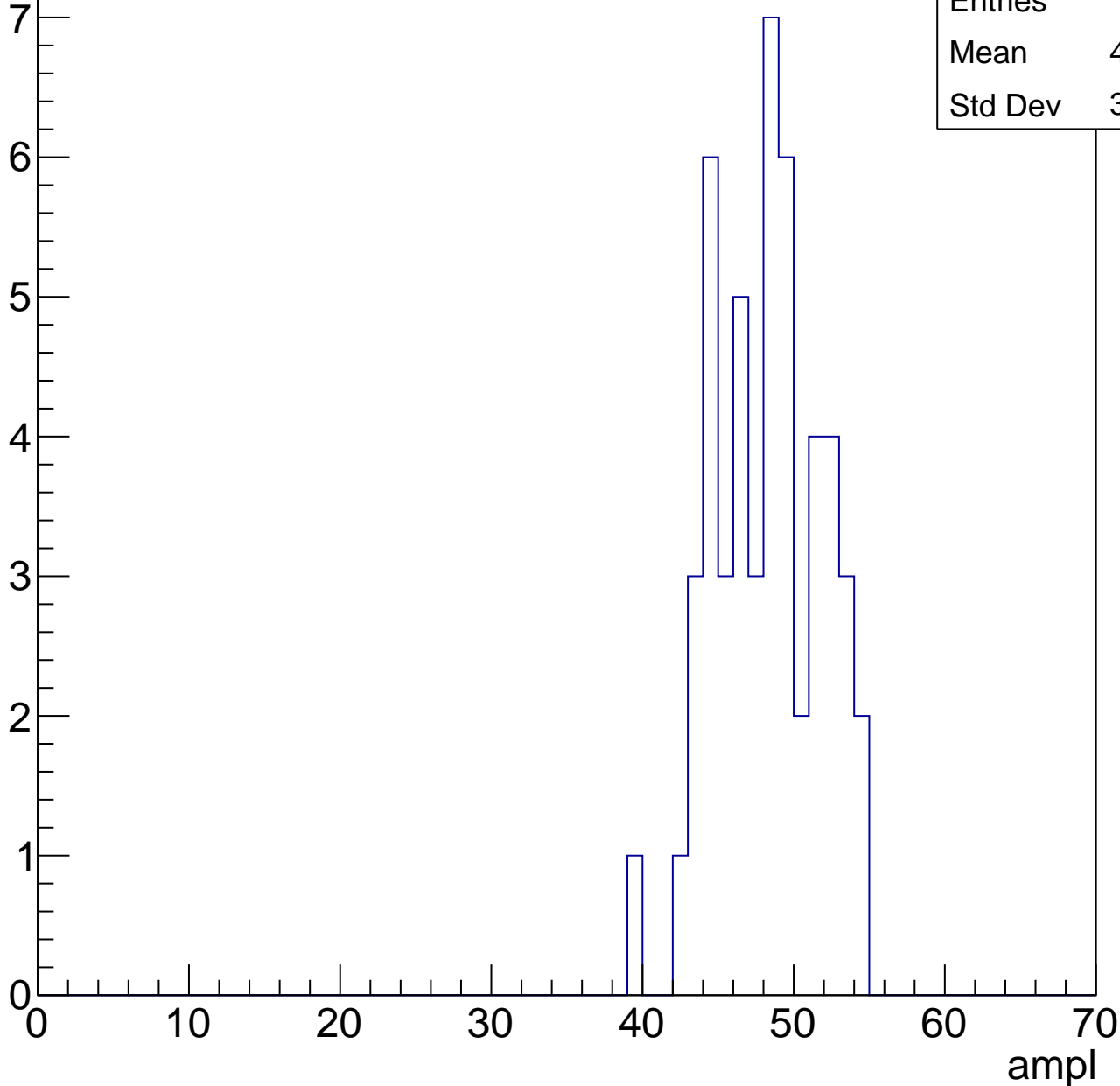


# B1L101S, U19-ch118, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	50
Mean	47.78
Std Dev	3.454

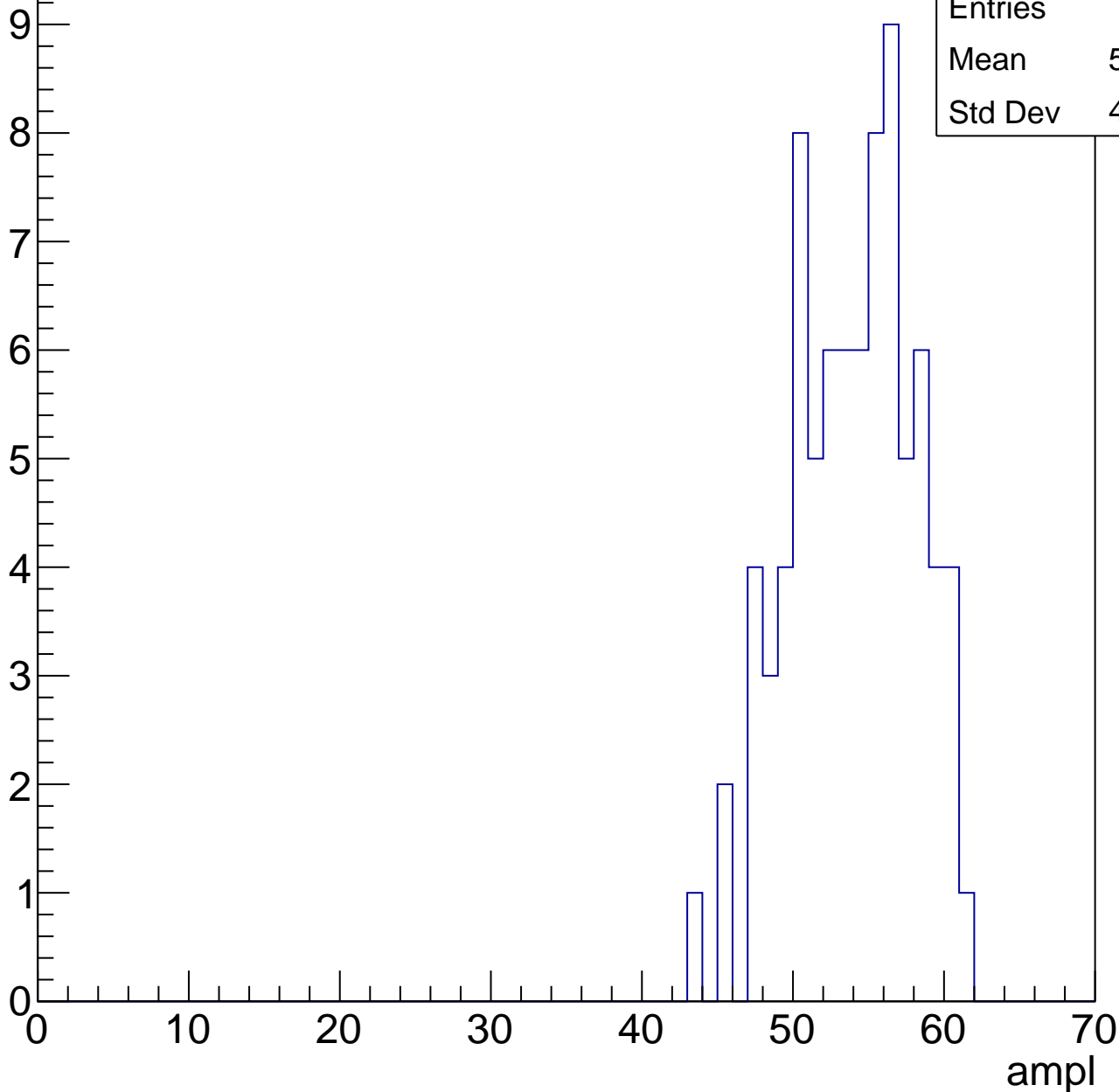


# B1L101S, U19-ch118, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	82
Mean	53.46
Std Dev	4.049

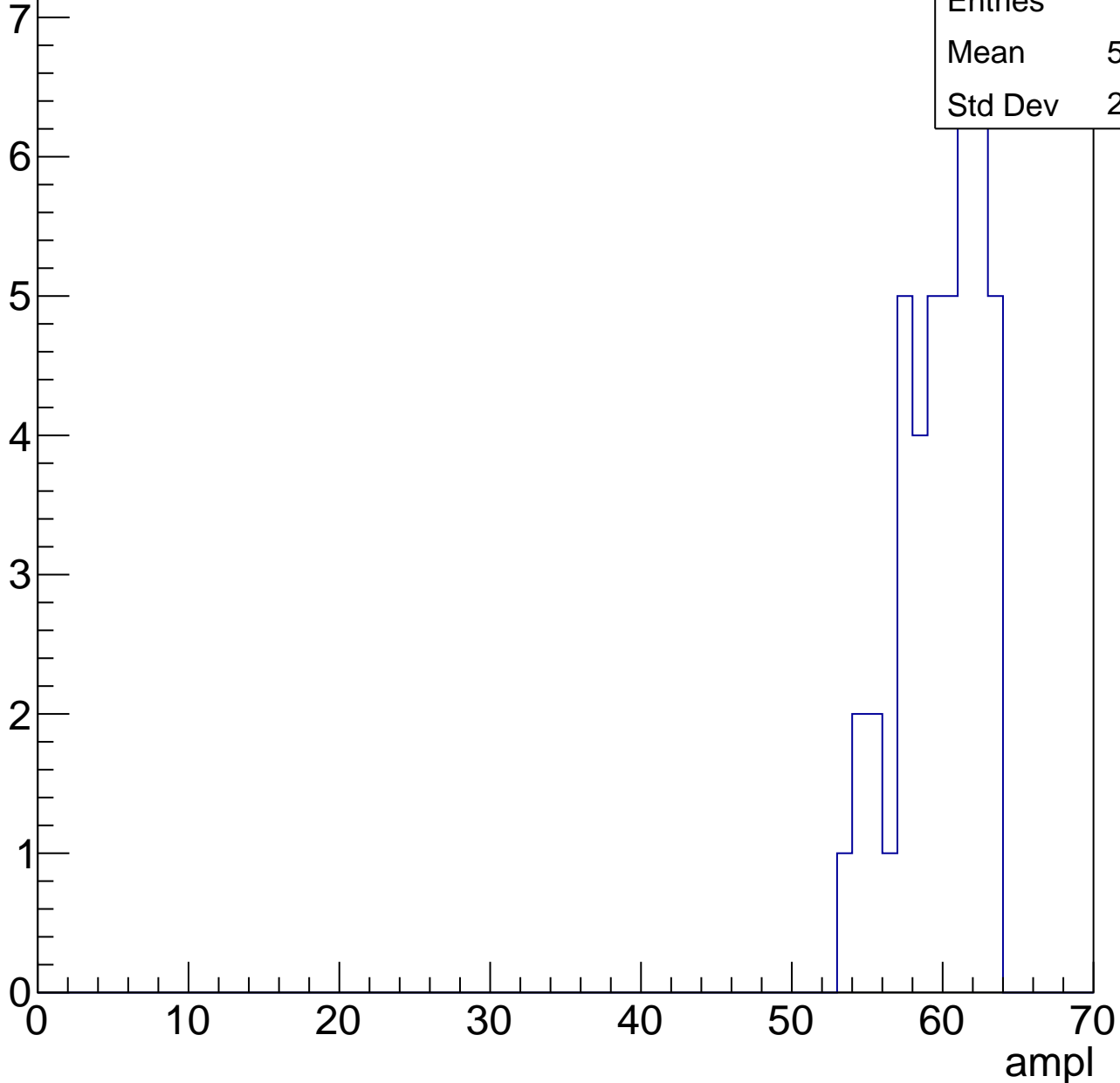


# B1L101S, U19-ch118, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

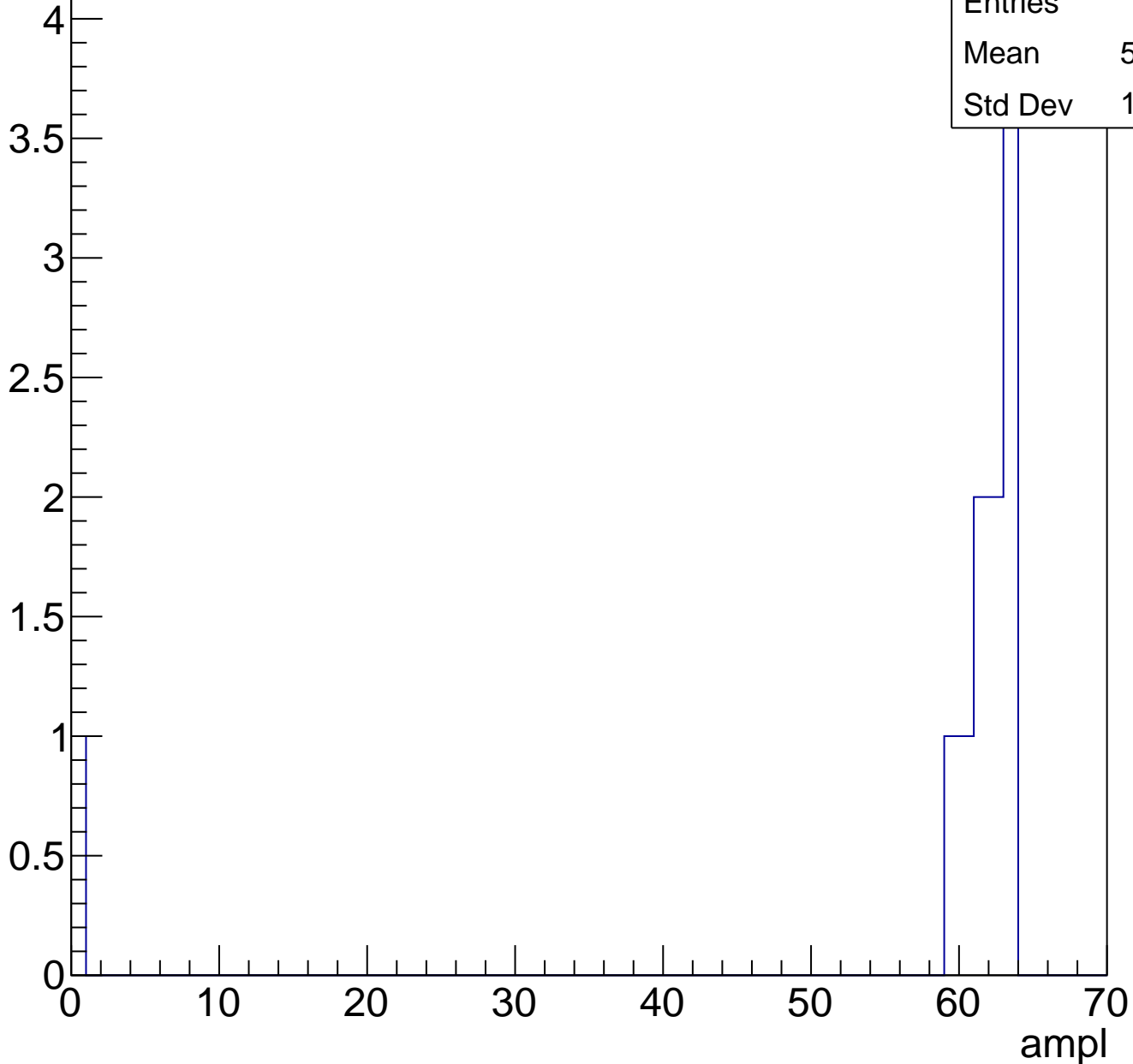
Entries	44
Mean	59.43
Std Dev	2.692



# B1L101S, U19-ch118, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U19-ch118, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U19-ch119, adc0

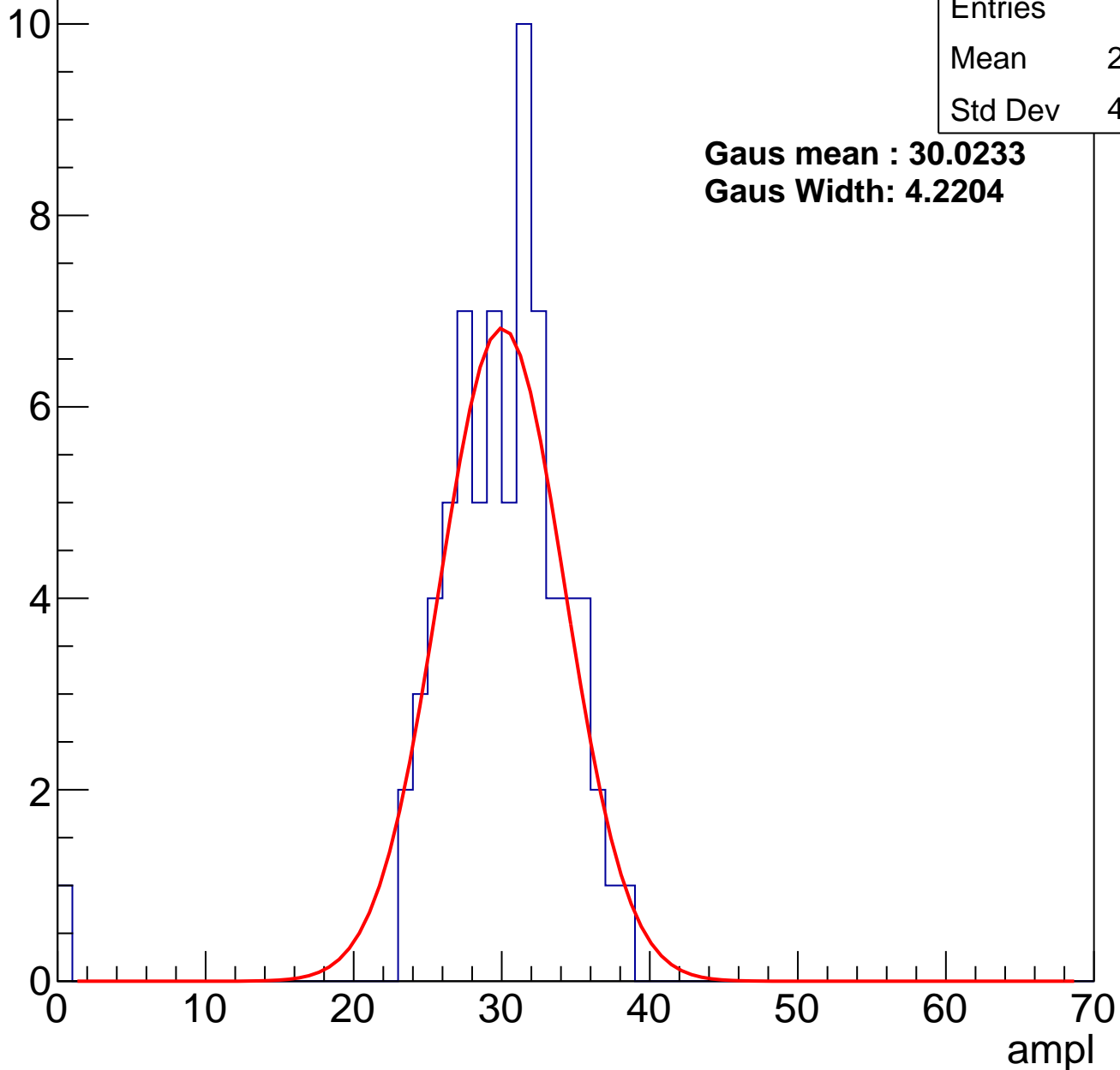
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	72
Mean	29.43
Std Dev	4.966

**Gaus mean : 30.0233**

**Gaus Width: 4.2204**

Entry



# B1L101S, U19-ch119, adc1

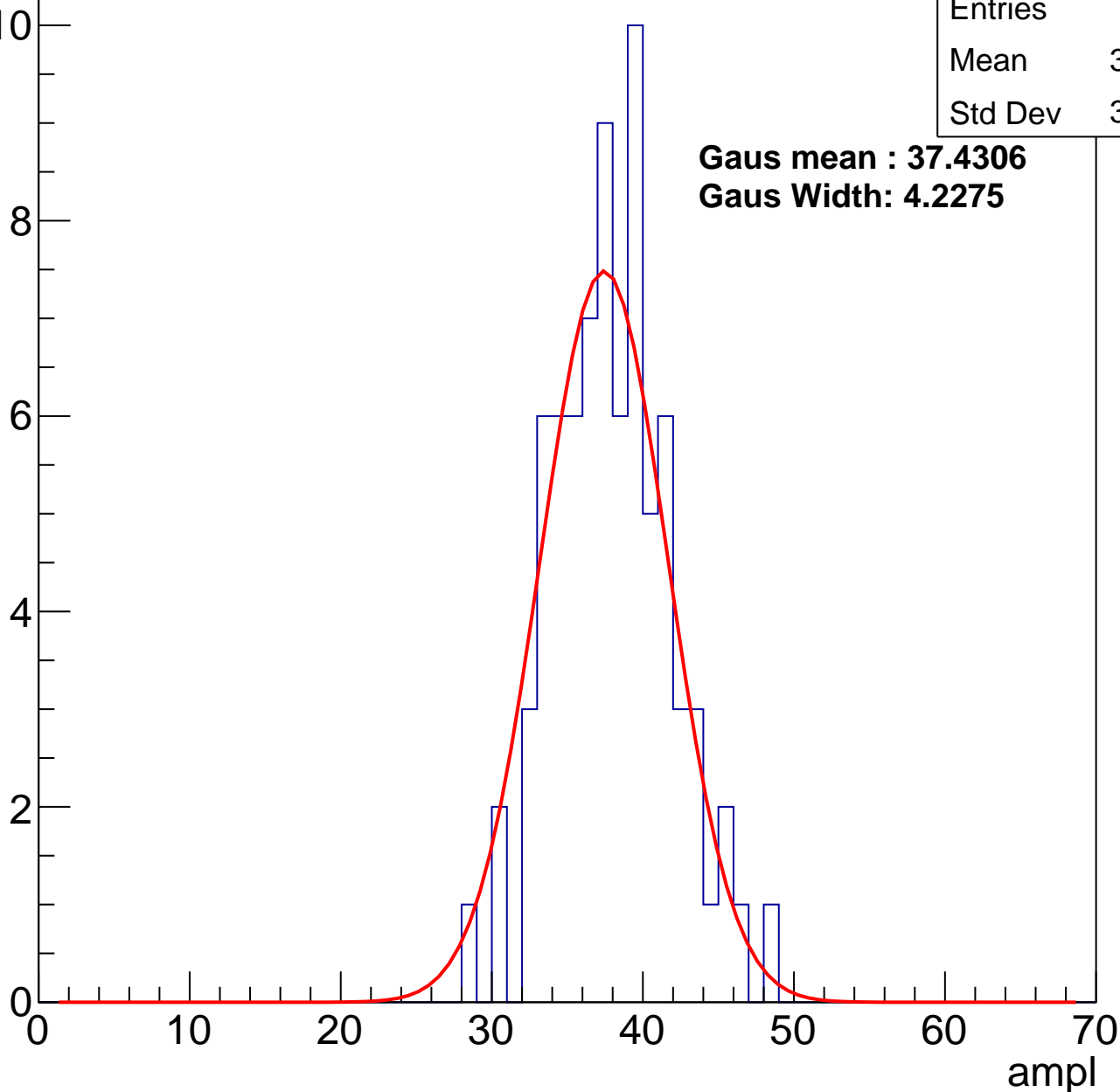
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	78
Mean	37.54
Std Dev	3.859

**Gaus mean : 37.4306**

**Gaus Width: 4.2275**

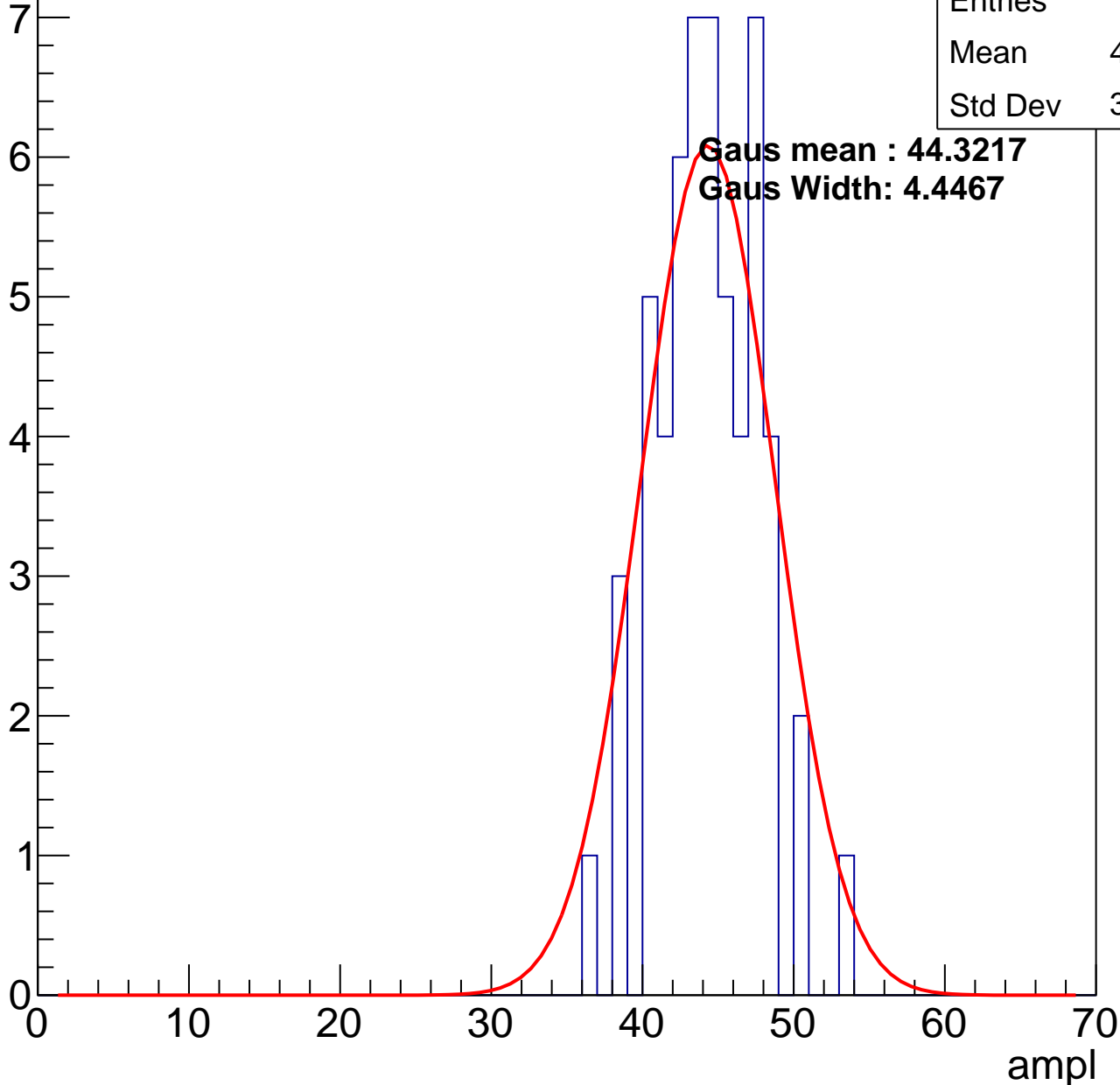


# B1L101S, U19-ch119, adc2

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	56
Mean	43.89
Std Dev	3.326

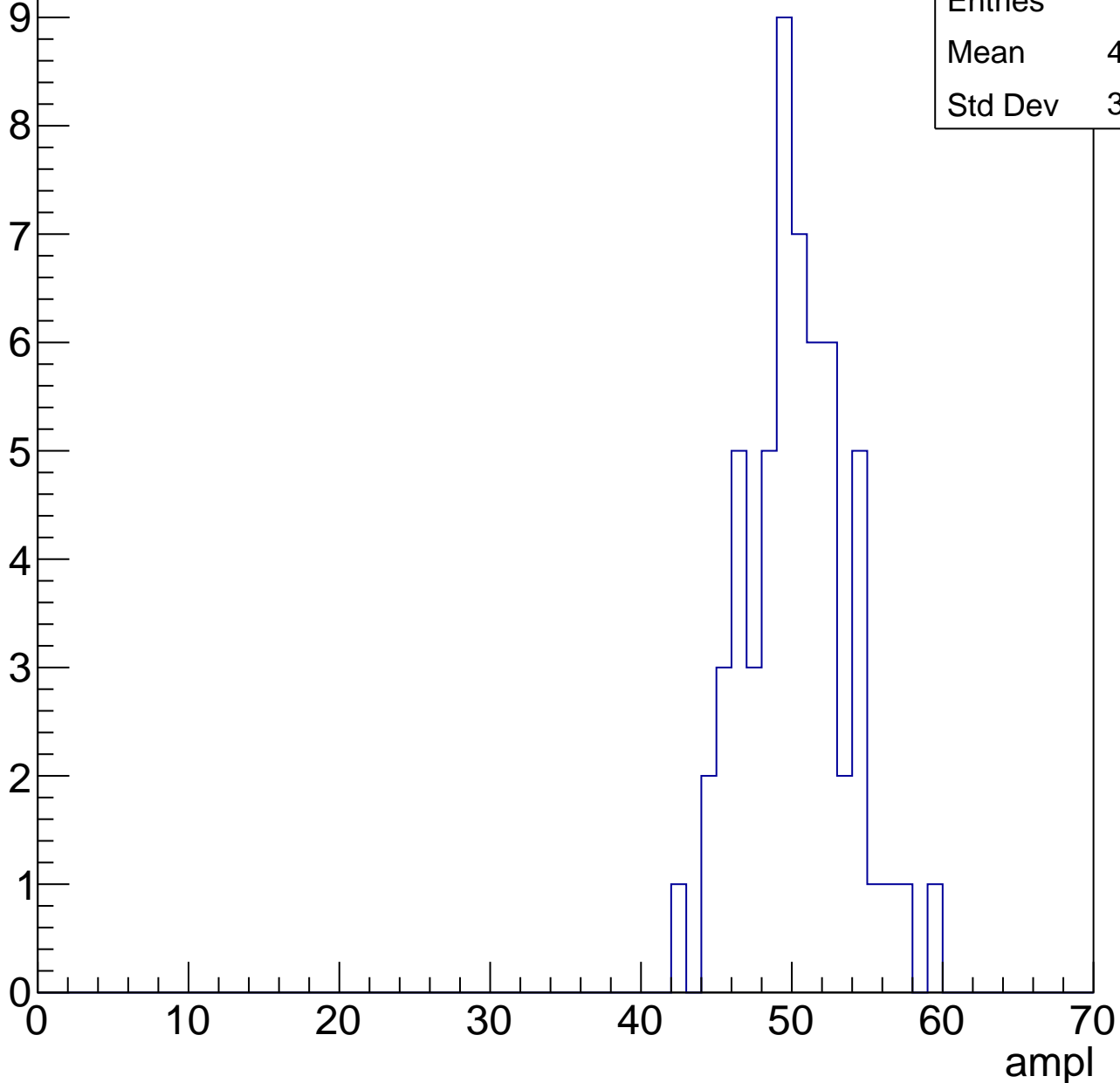


# B1L101S, U19-ch119, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	58
Mean	49.79
Std Dev	3.382

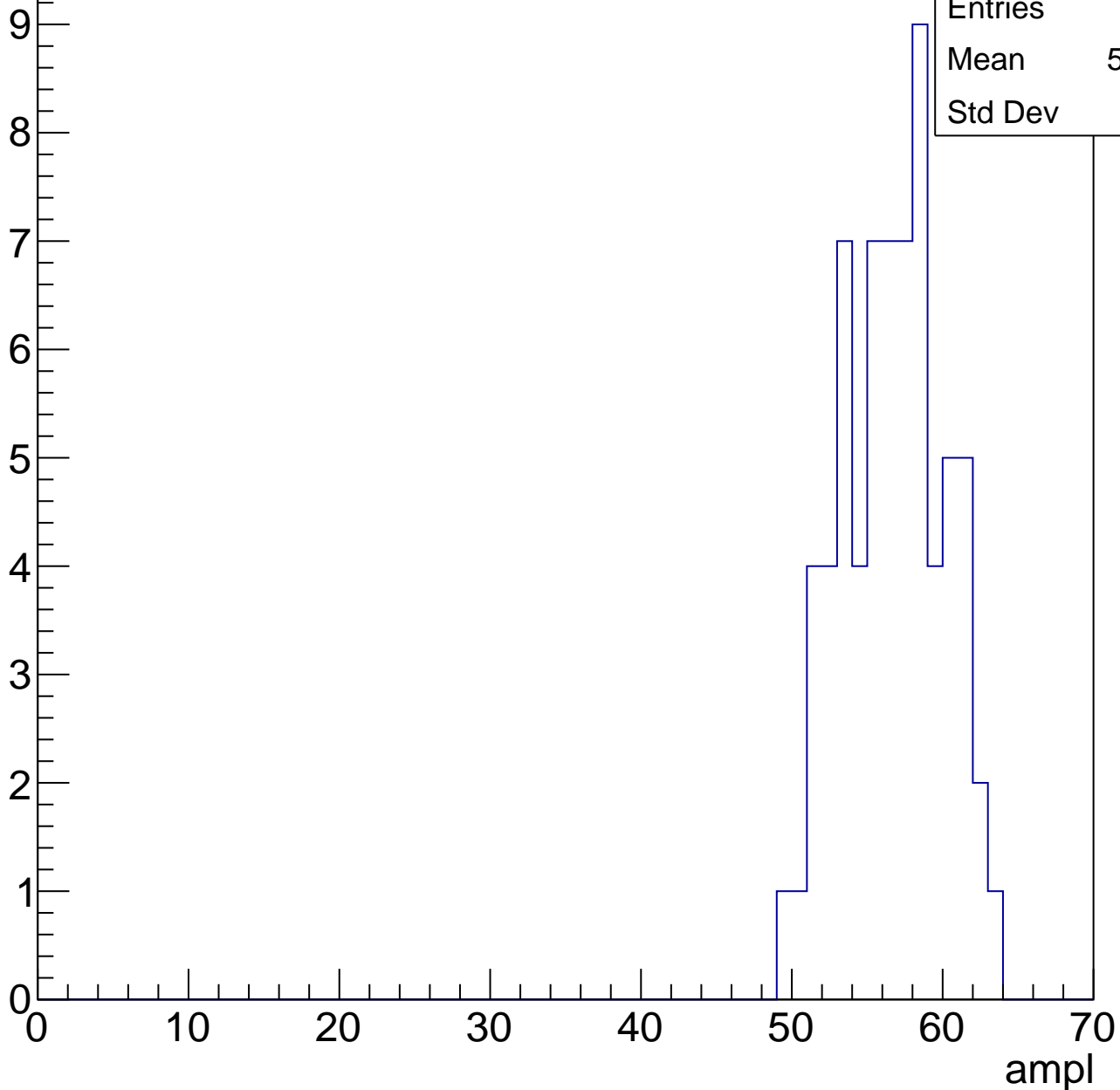


# B1L101S, U19-ch119, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	56.24
Std Dev	3.29

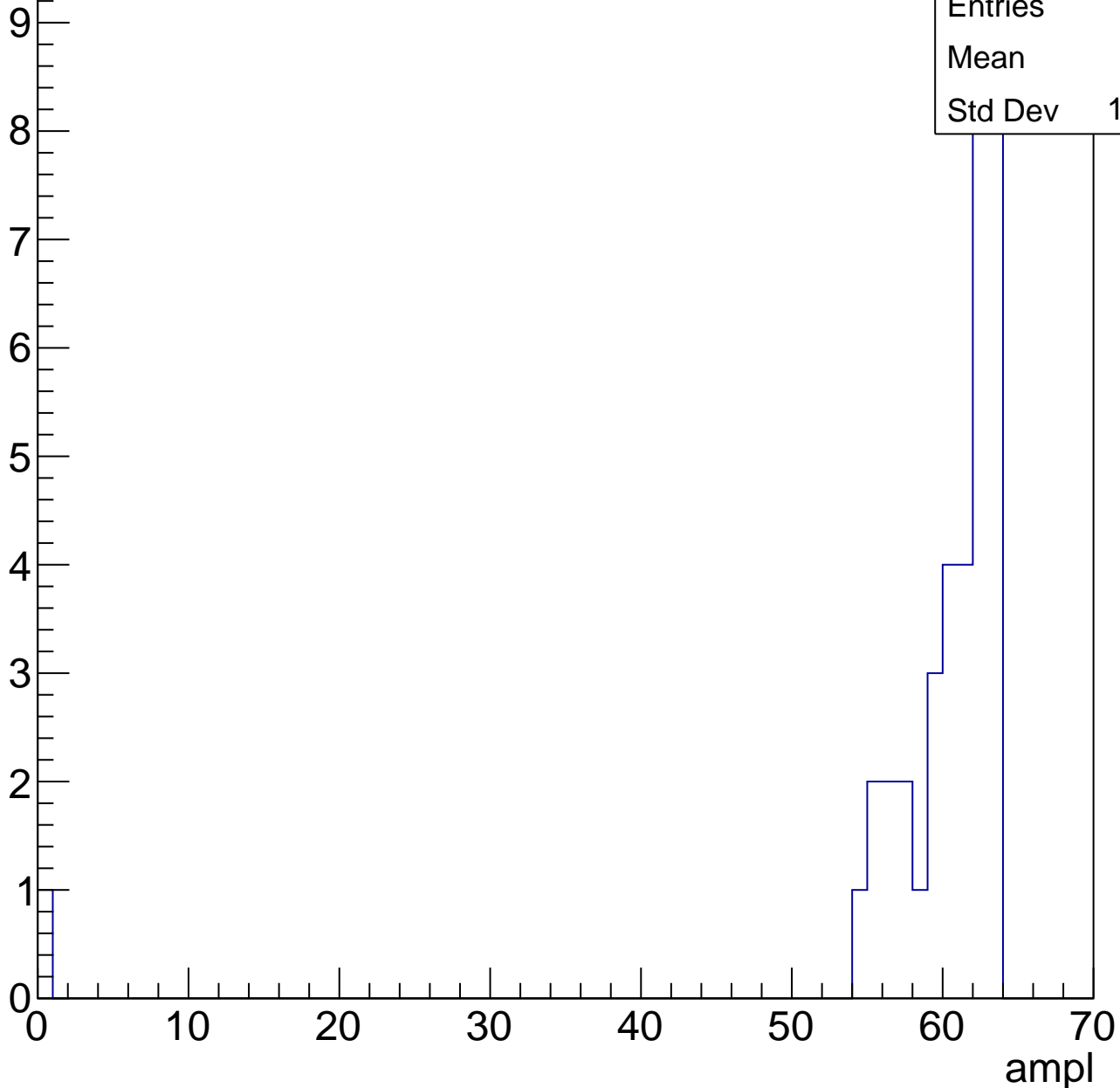


# B1L101S, U19-ch119, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	37
Mean	58.7
Std Dev	10.13



# B1L101S, U19-ch119, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

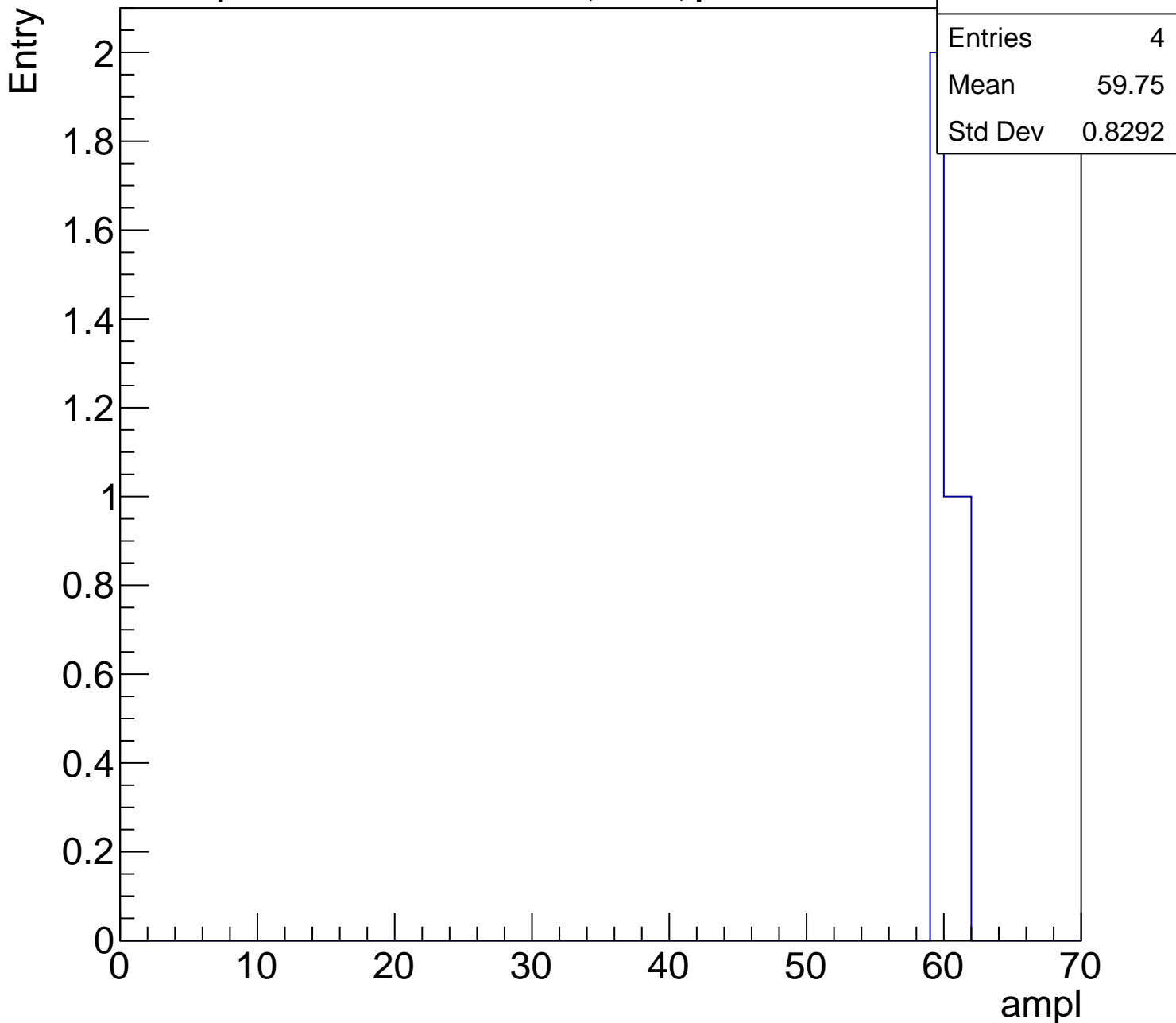
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	4
Mean	59.75
Std Dev	0.8292

0 10 20 30 40 50 60 70

ampl

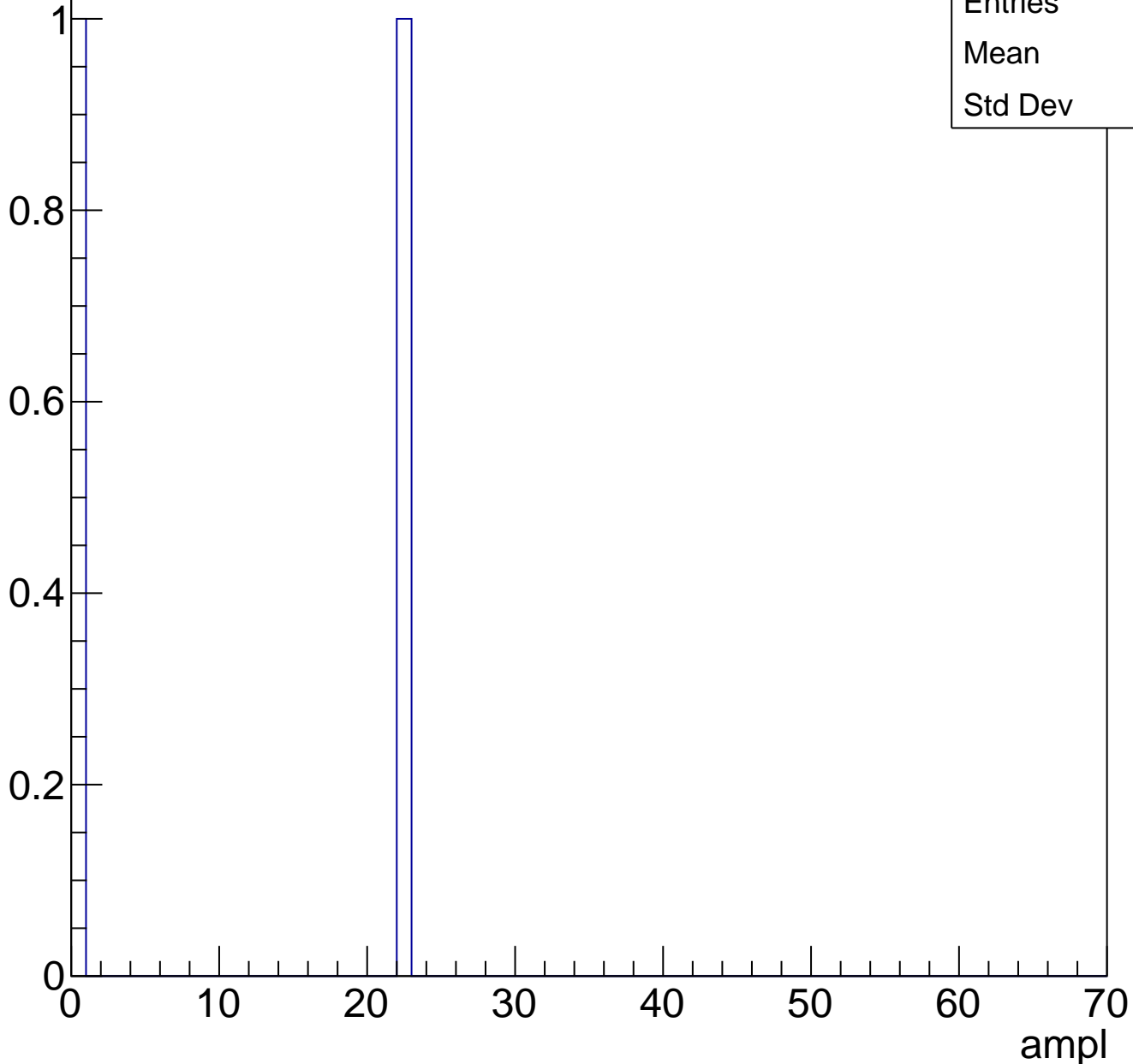




# B1L101S, U19-ch119, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	2
Mean	11
Std Dev	11

# B1L101S, U19-ch120, adc0

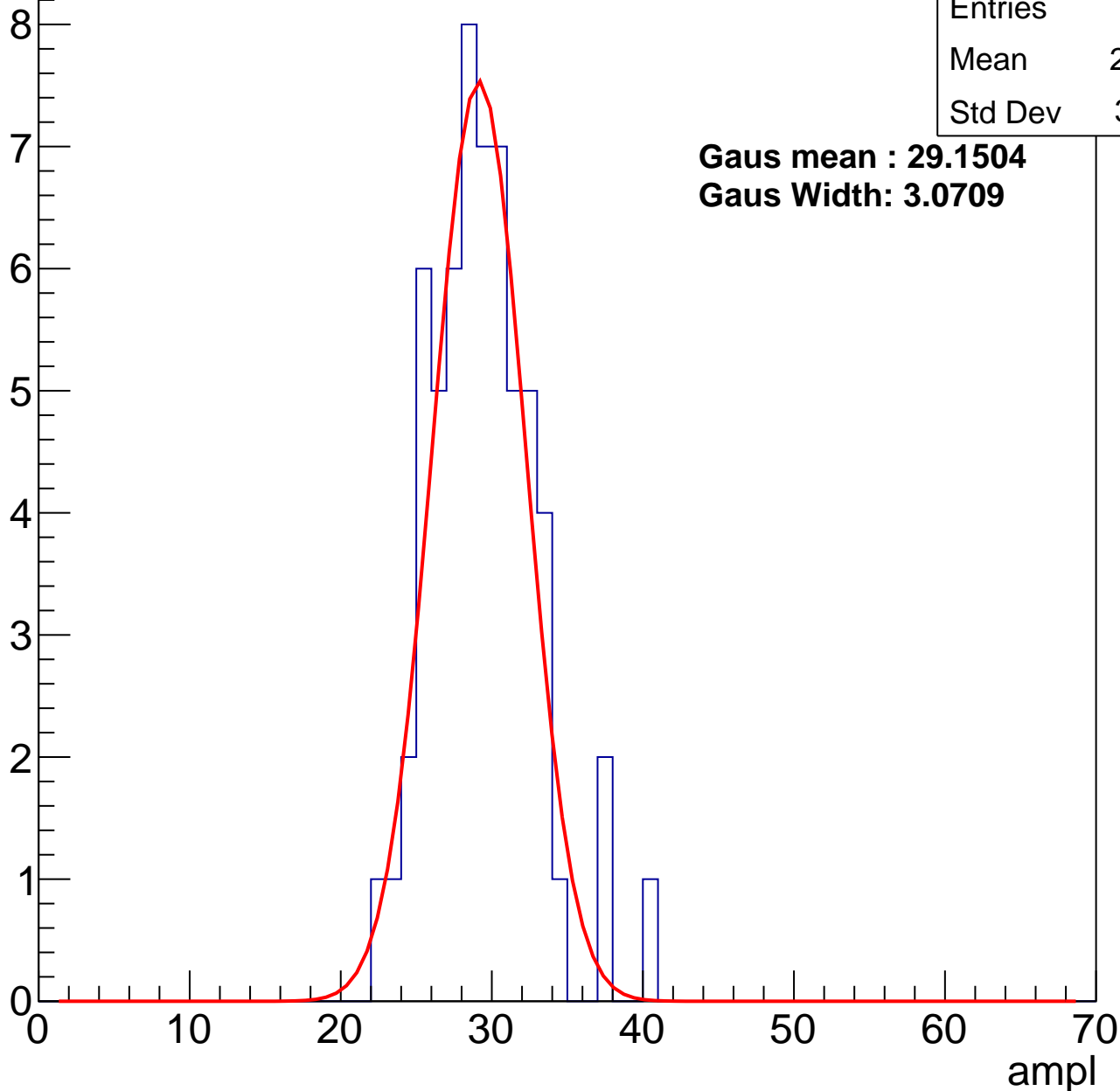
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	28.97
Std Dev	3.431

**Gaus mean : 29.1504**

**Gaus Width: 3.0709**



# B1L101S, U19-ch120, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	68
Mean	35.69
Std Dev	3.578

**Gaus mean : 36.1095**

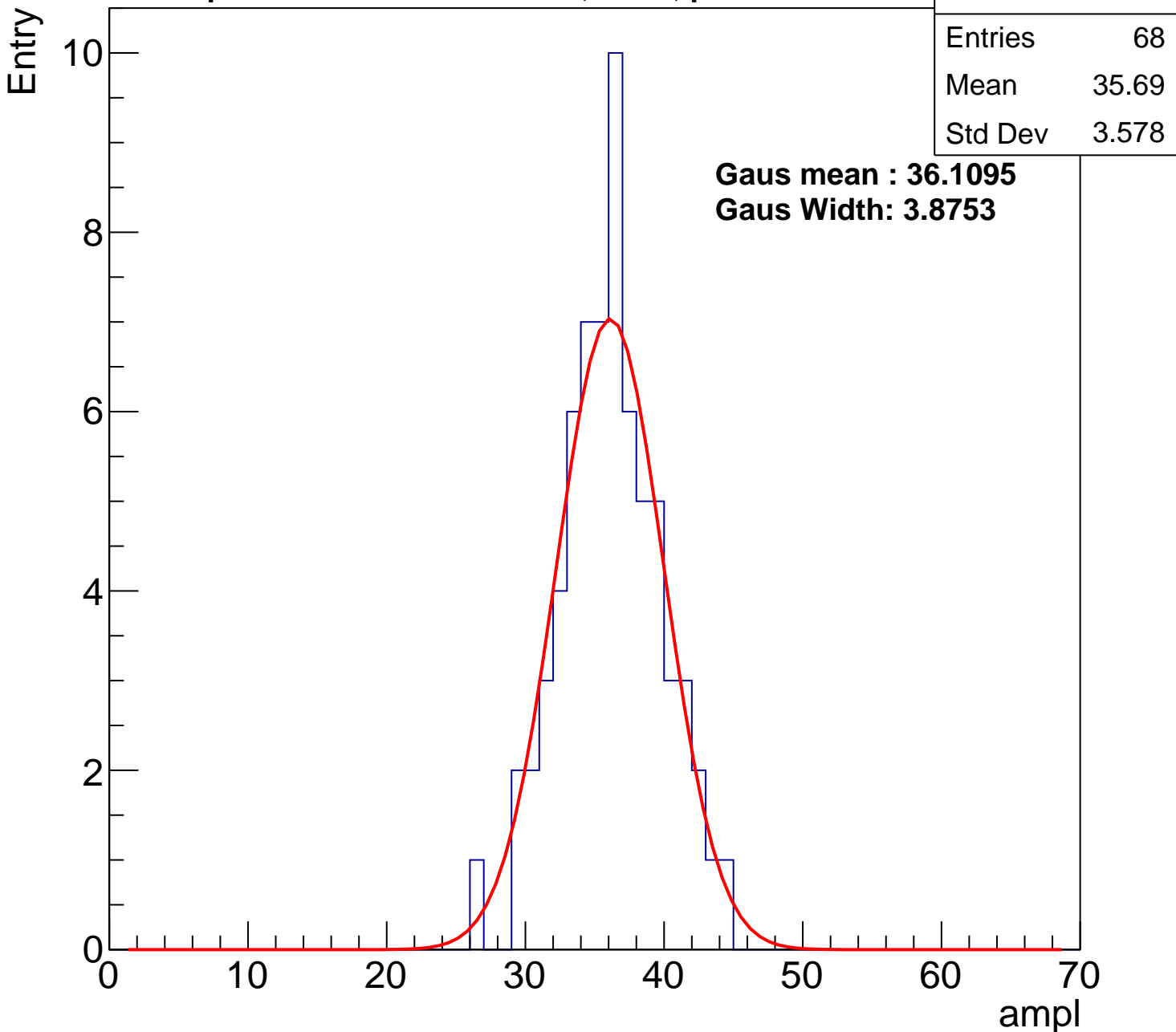
**Gaus Width: 3.8753**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U19-ch120, adc2

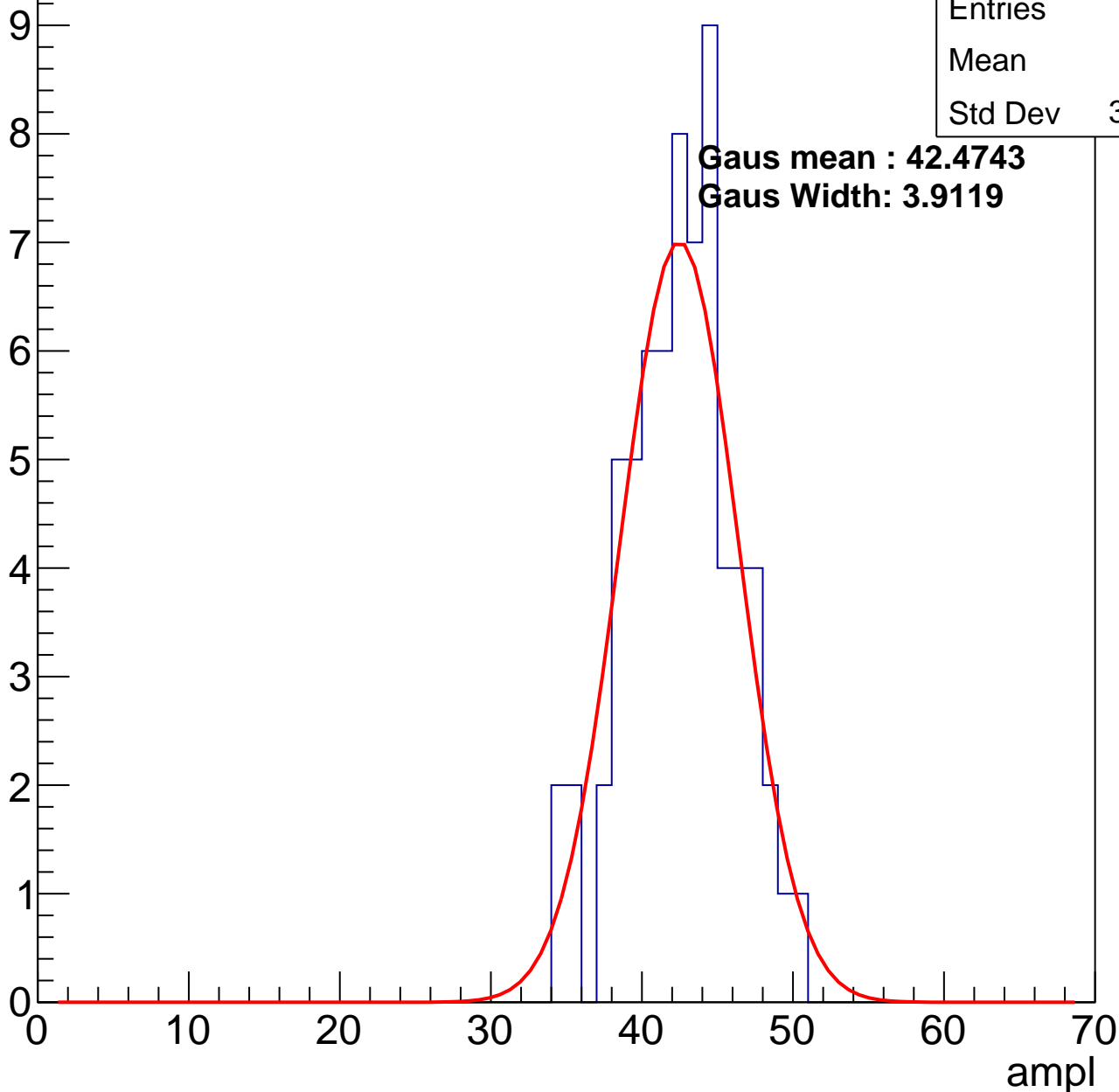
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	42.1
Std Dev	3.553

**Gaus mean : 42.4743**

**Gaus Width: 3.9119**

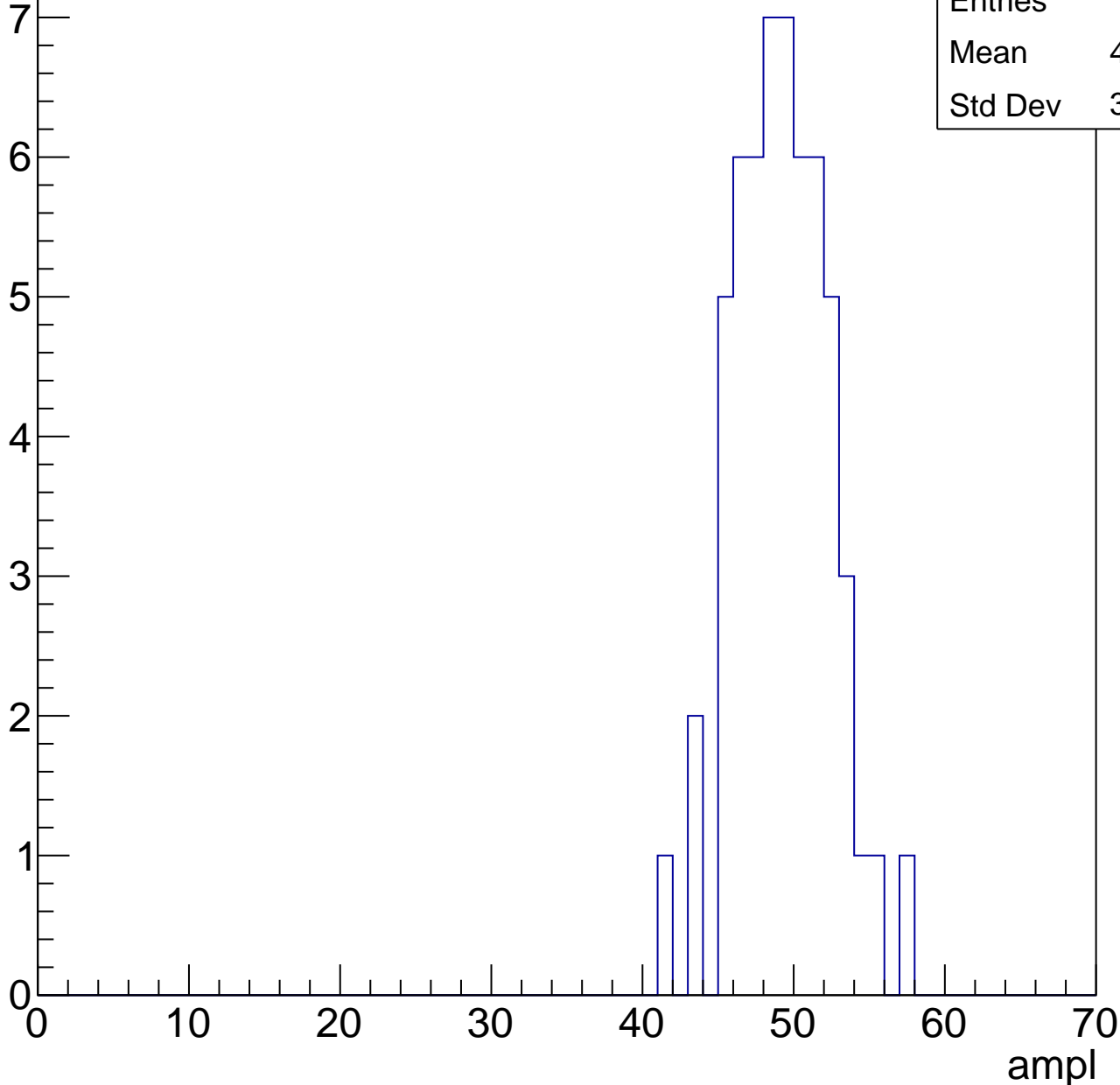


# B1L101S, U19-ch120, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	57
Mean	48.77
Std Dev	3.095

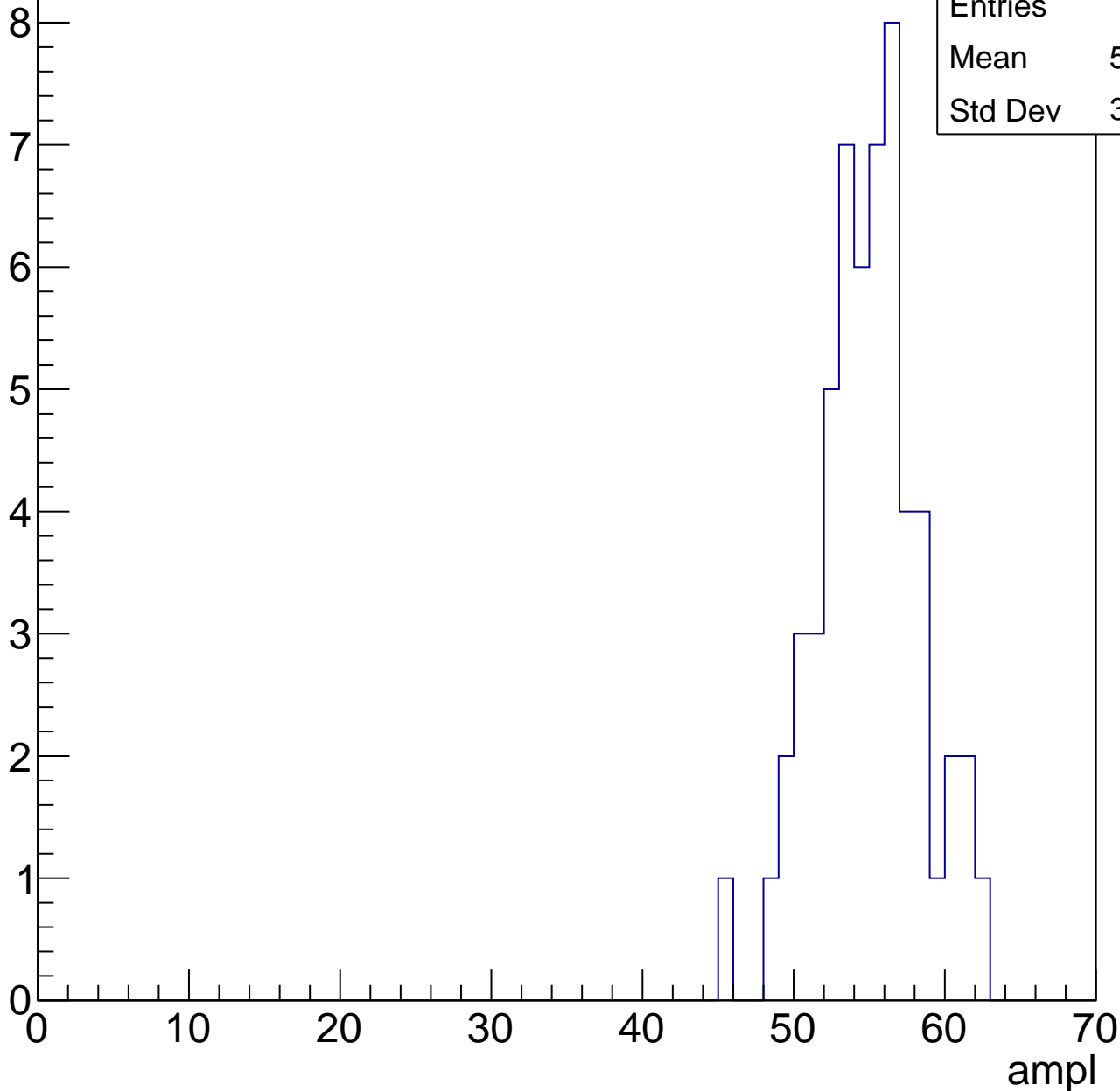


# B1L101S, U19-ch120, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	57
Mean	54.47
Std Dev	3.388

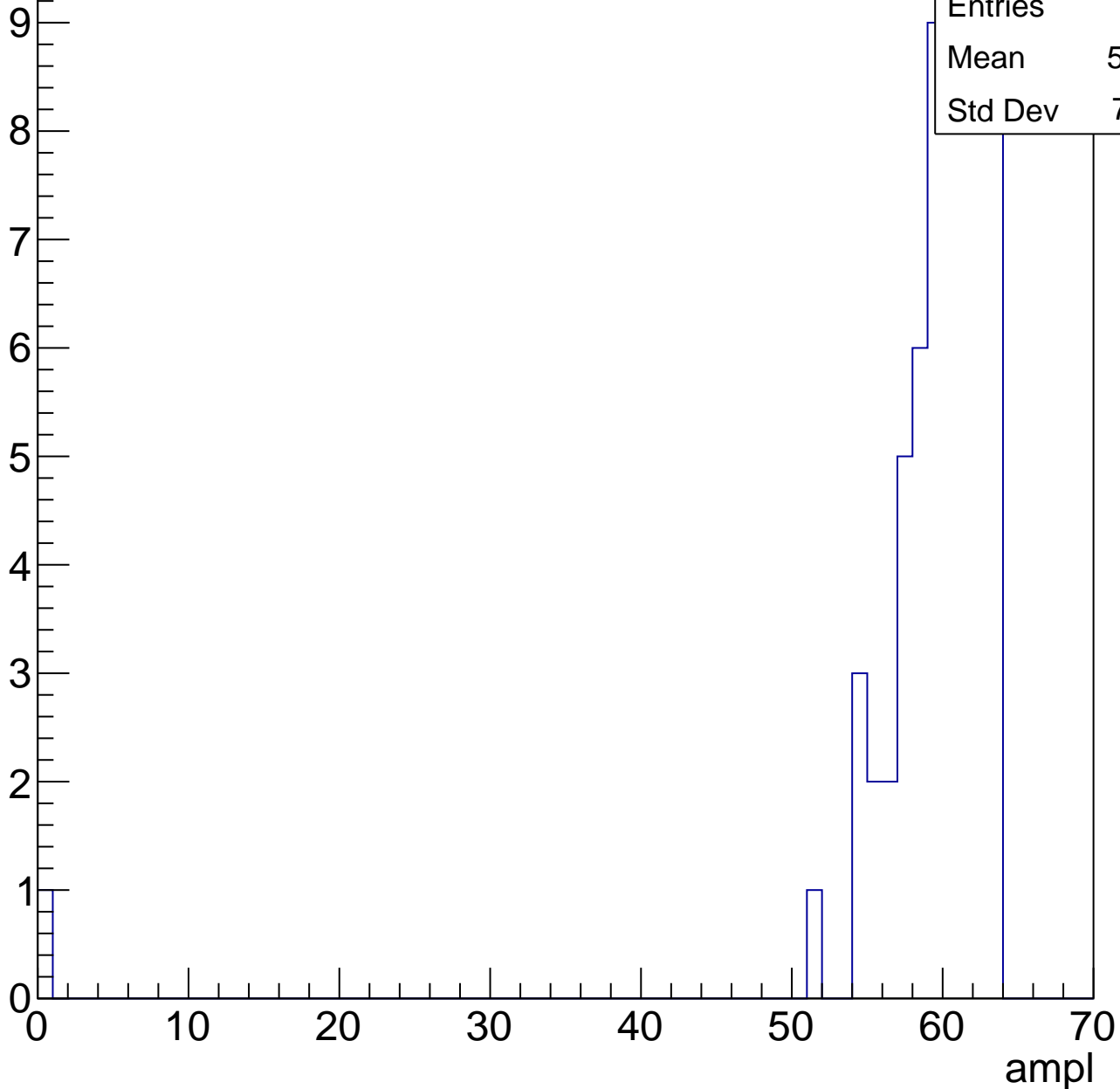


# B1L101S, U19-ch120, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	58.55
Std Dev	7.971



# B1L101S, U19-ch120, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

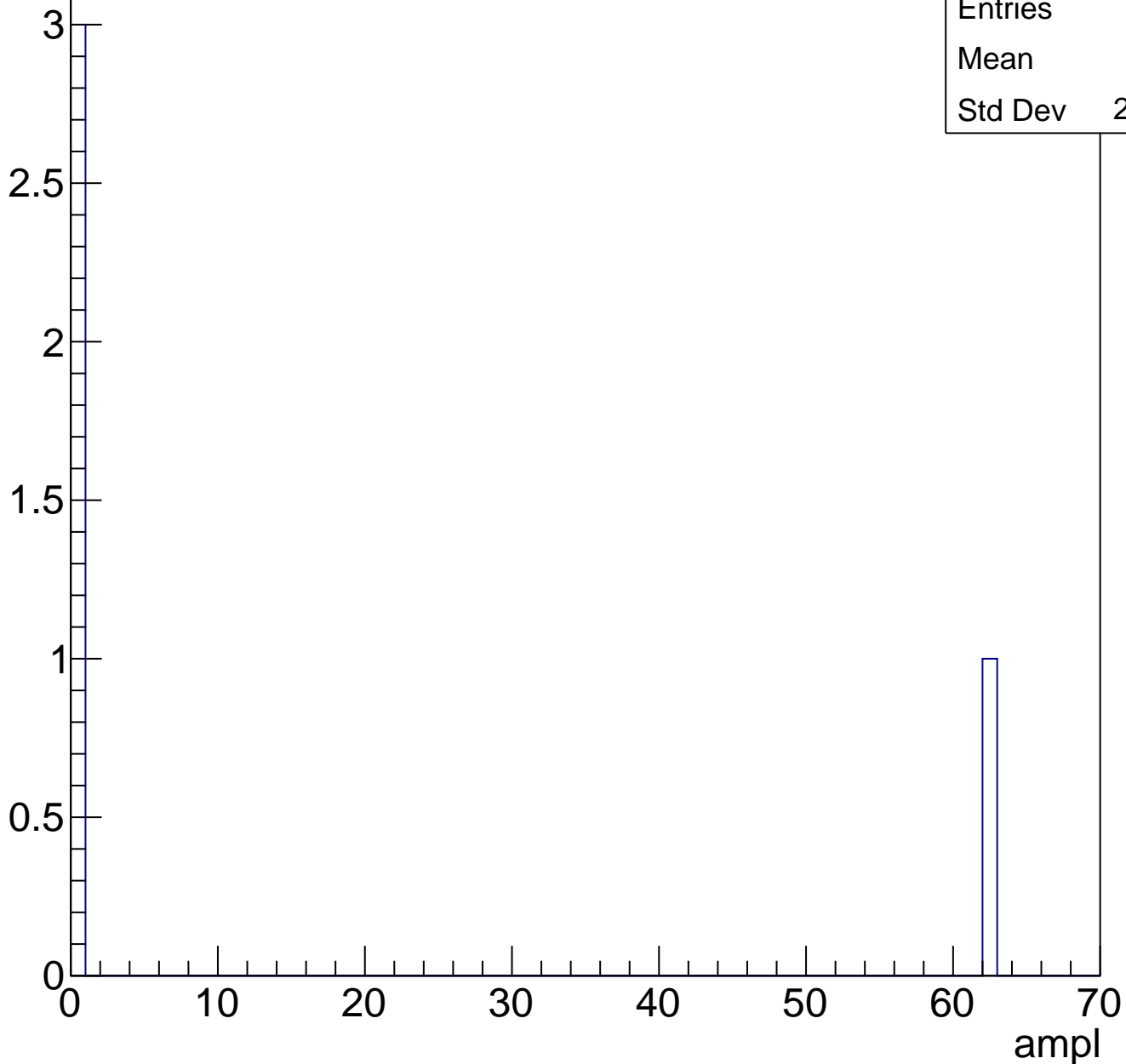




# B1L101S, U19-ch120, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U19-ch121, adc0

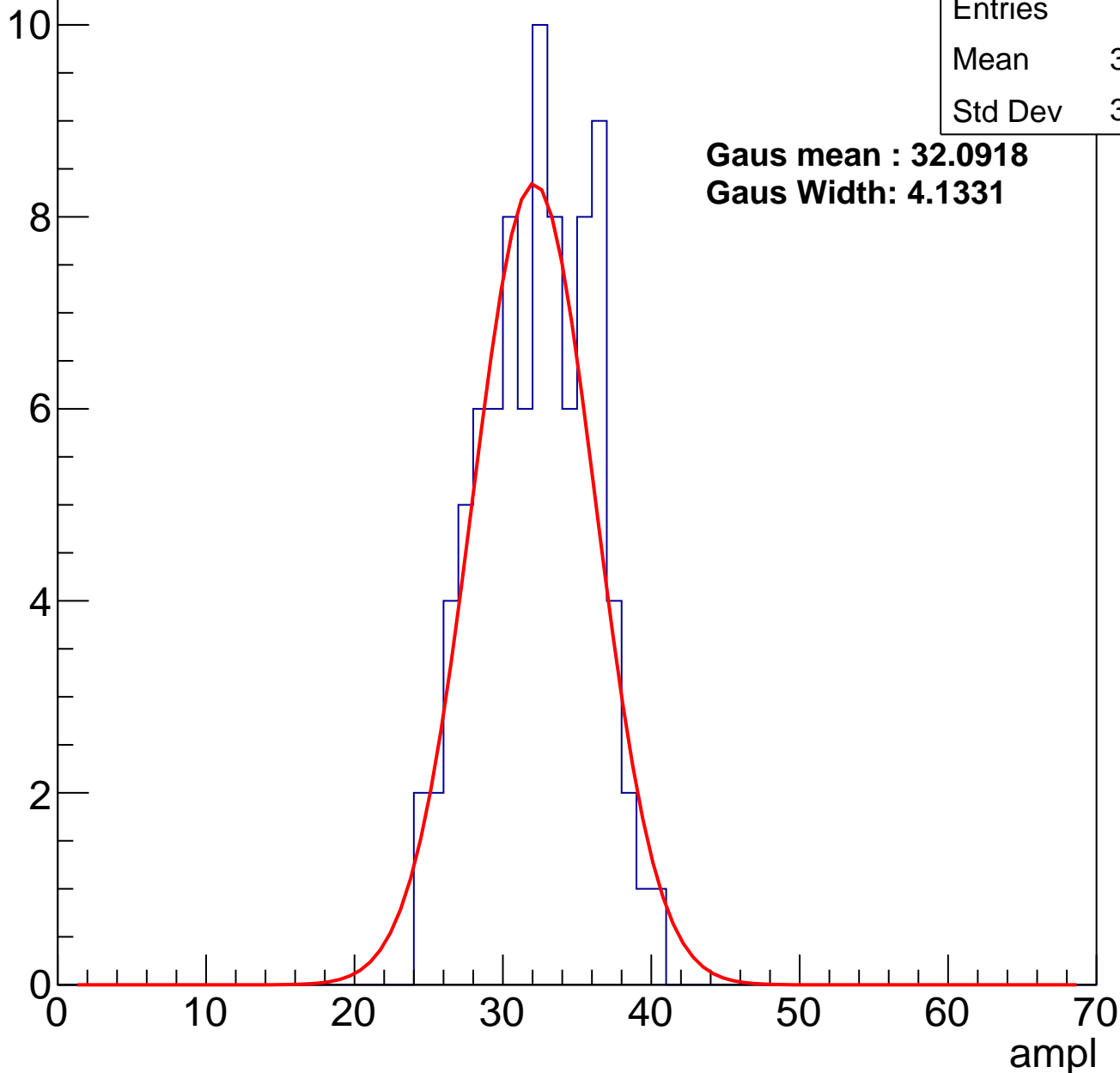
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	88
Mean	31.82
Std Dev	3.713

**Gaus mean : 32.0918**

**Gaus Width: 4.1331**

Entry



# B1L101S, U19-ch121, adc1

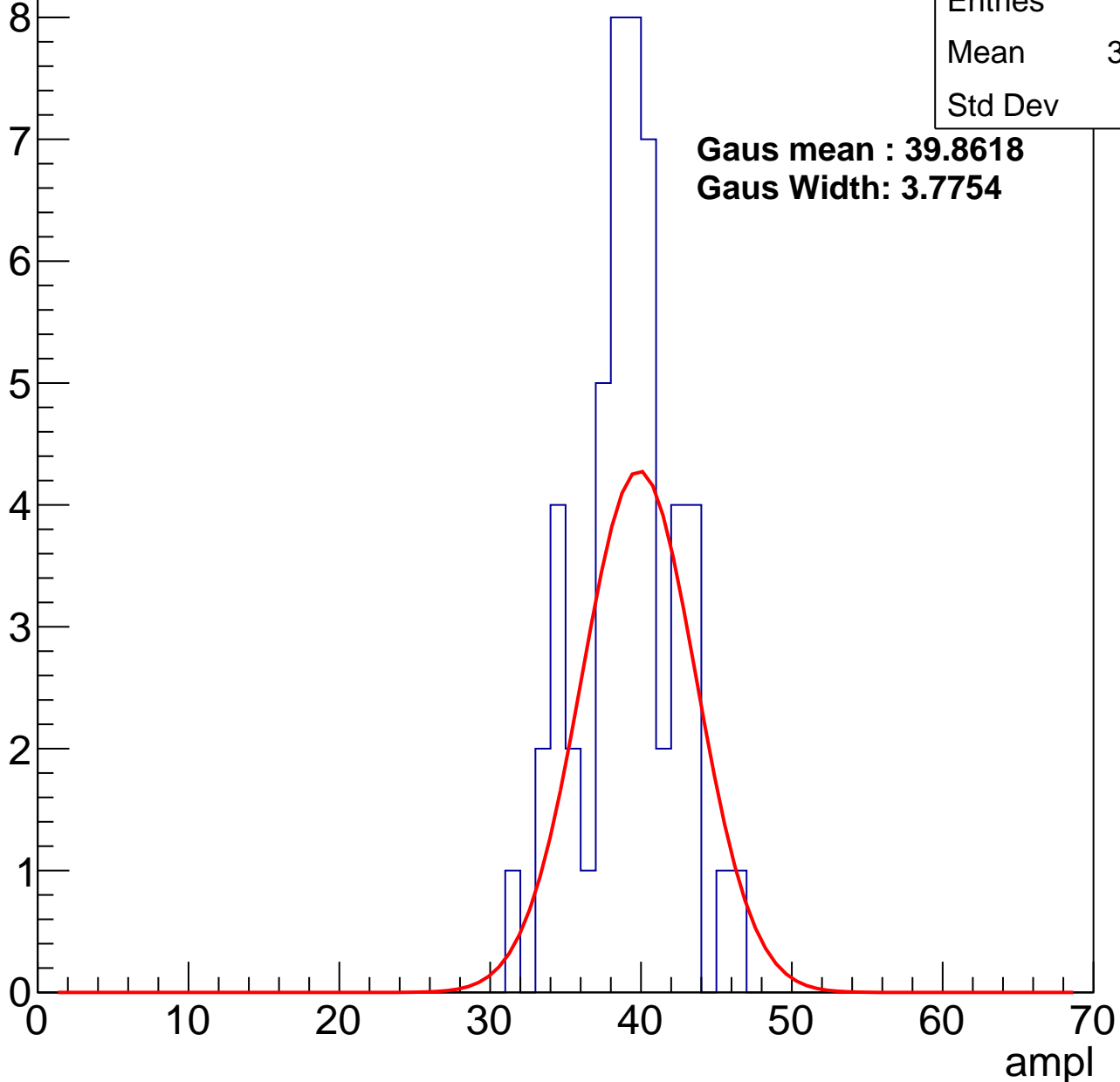
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	50
Mean	38.66
Std Dev	3.16

**Gaus mean : 39.8618**

**Gaus Width: 3.7754**



# B1L101S, U19-ch121, adc2

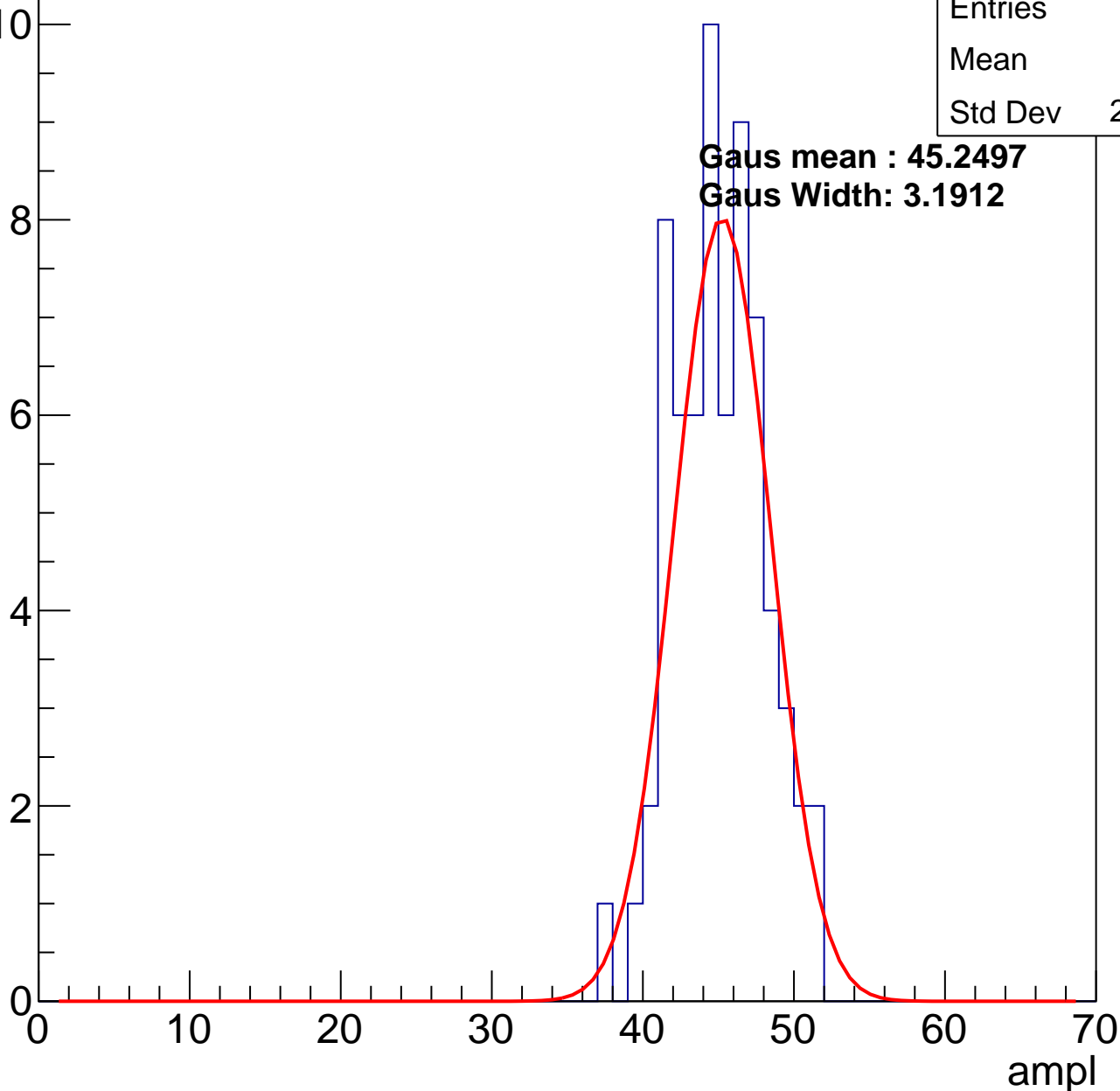
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	67
Mean	44.6
Std Dev	2.988

**Gaus mean : 45.2497**

**Gaus Width: 3.1912**

Entry

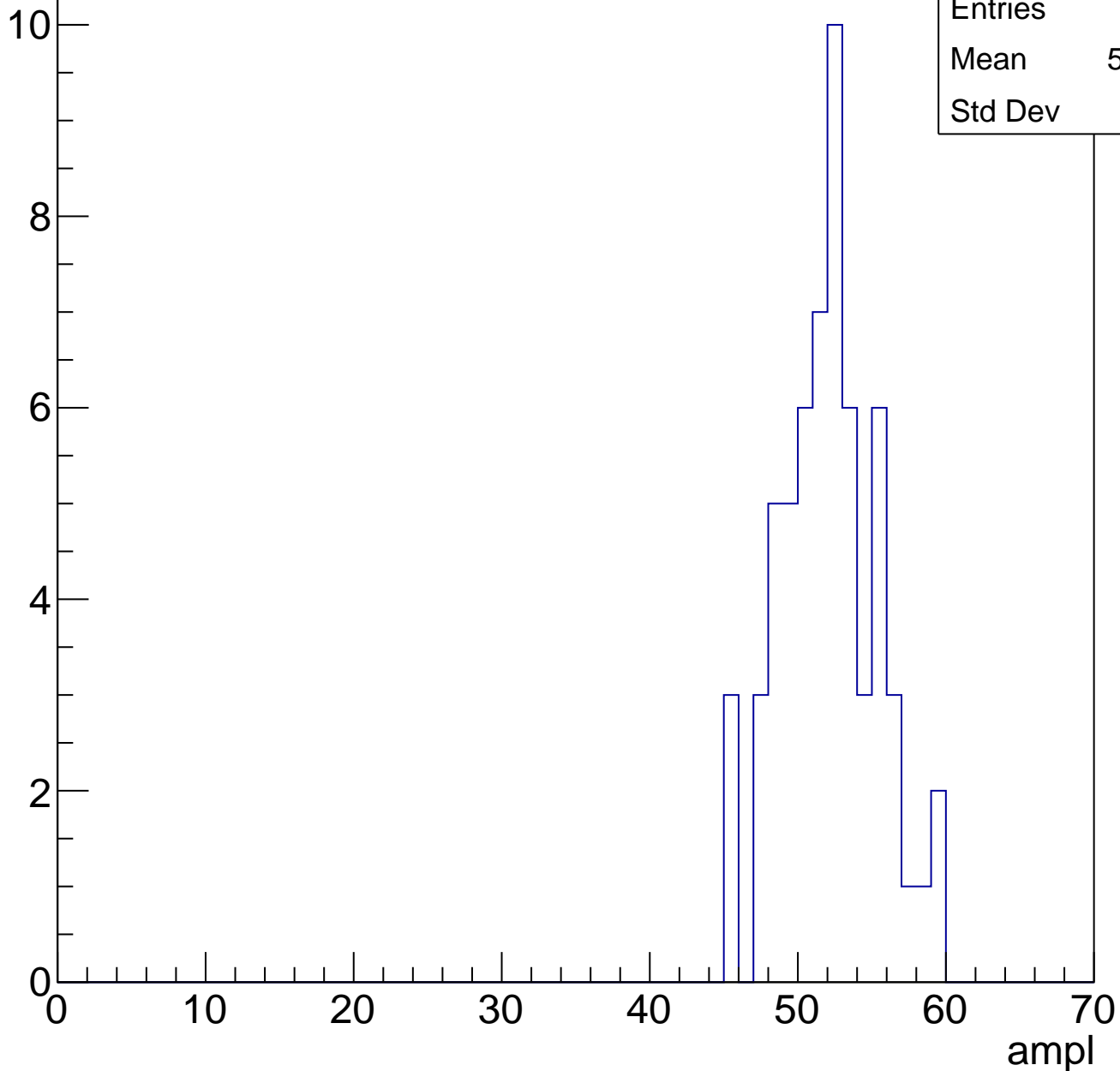


# B1L101S, U19-ch121, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	51.62
Std Dev	3.26

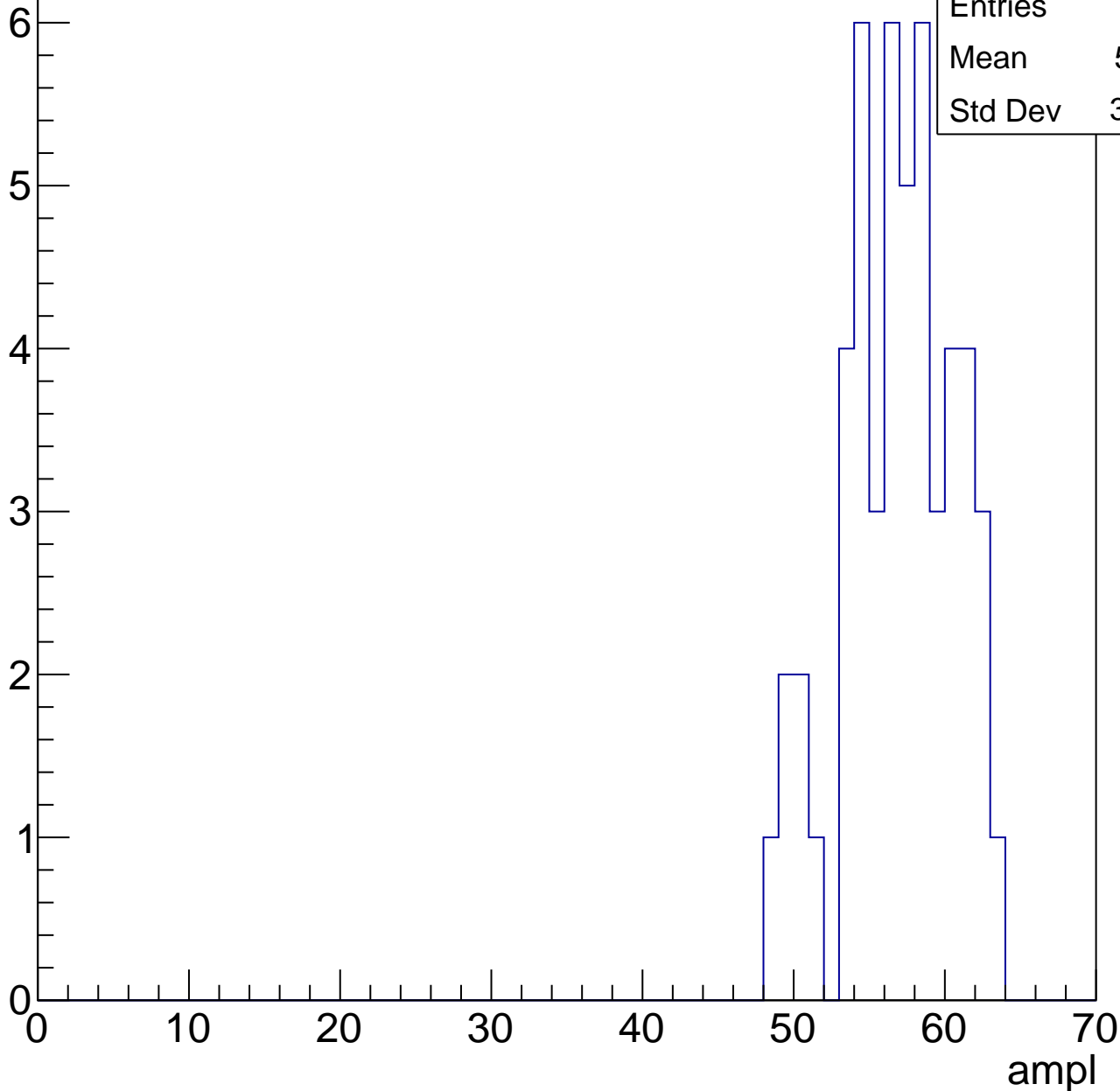


# B1L101S, U19-ch121, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	51
Mean	56.41
Std Dev	3.679

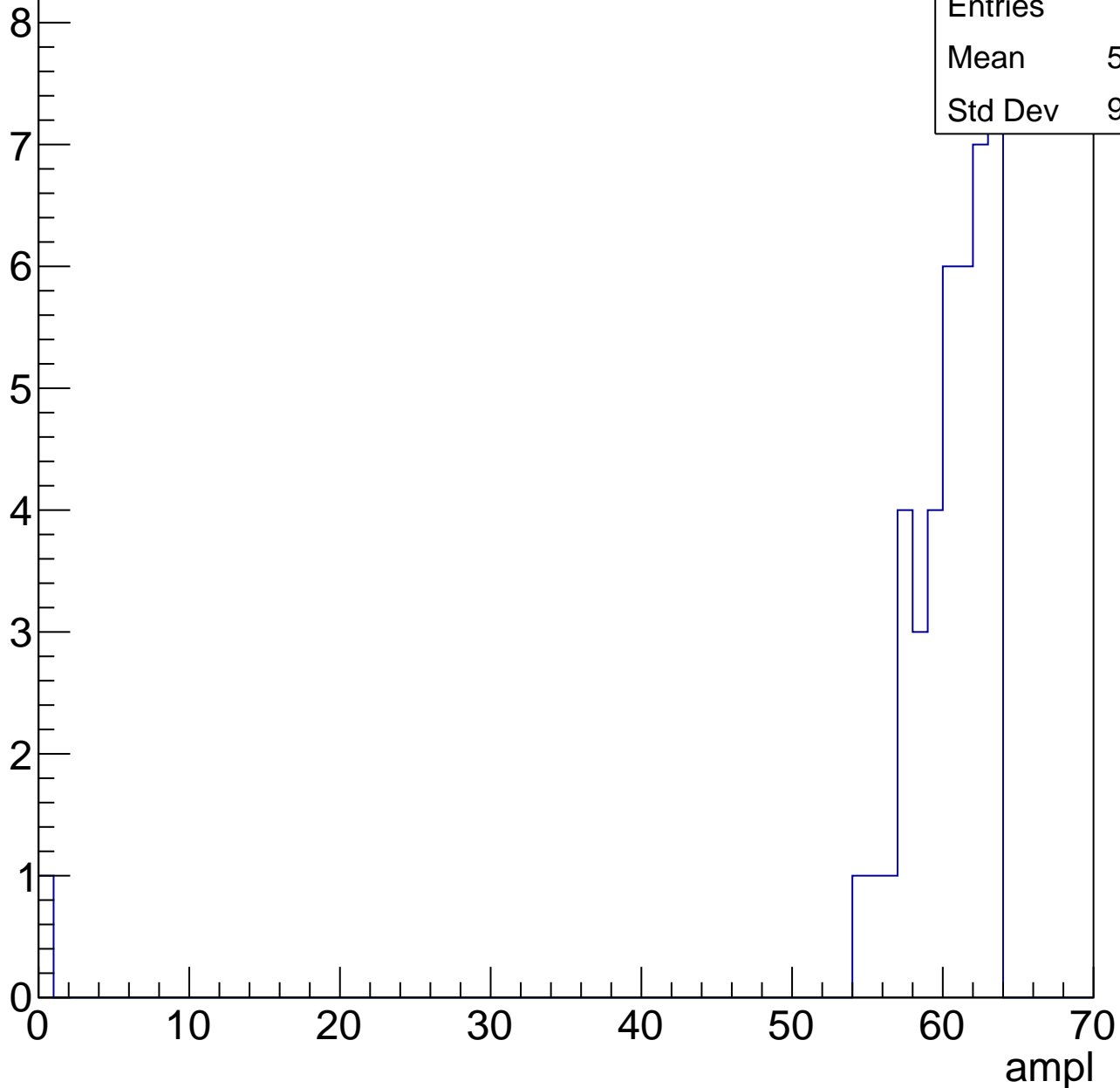


# B1L101S, U19-ch121, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	42
Mean	58.74
Std Dev	9.472



# B1L101S, U19-ch121, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U19-ch121, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U19-ch122, adc0

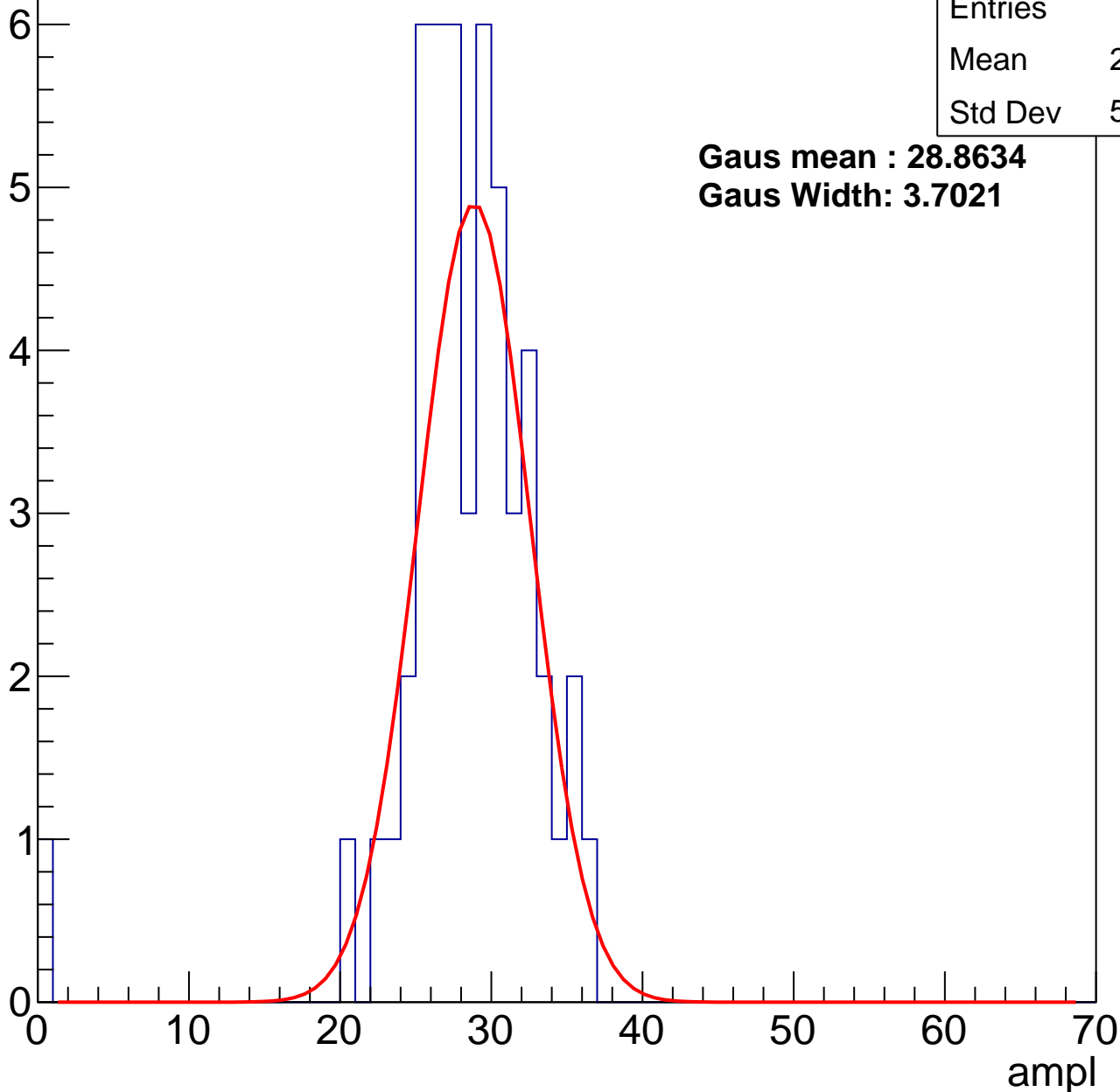
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	51
Mean	27.76
Std Dev	5.215

**Gaus mean : 28.8634**

**Gaus Width: 3.7021**



# B1L101S, U19-ch122, adc1

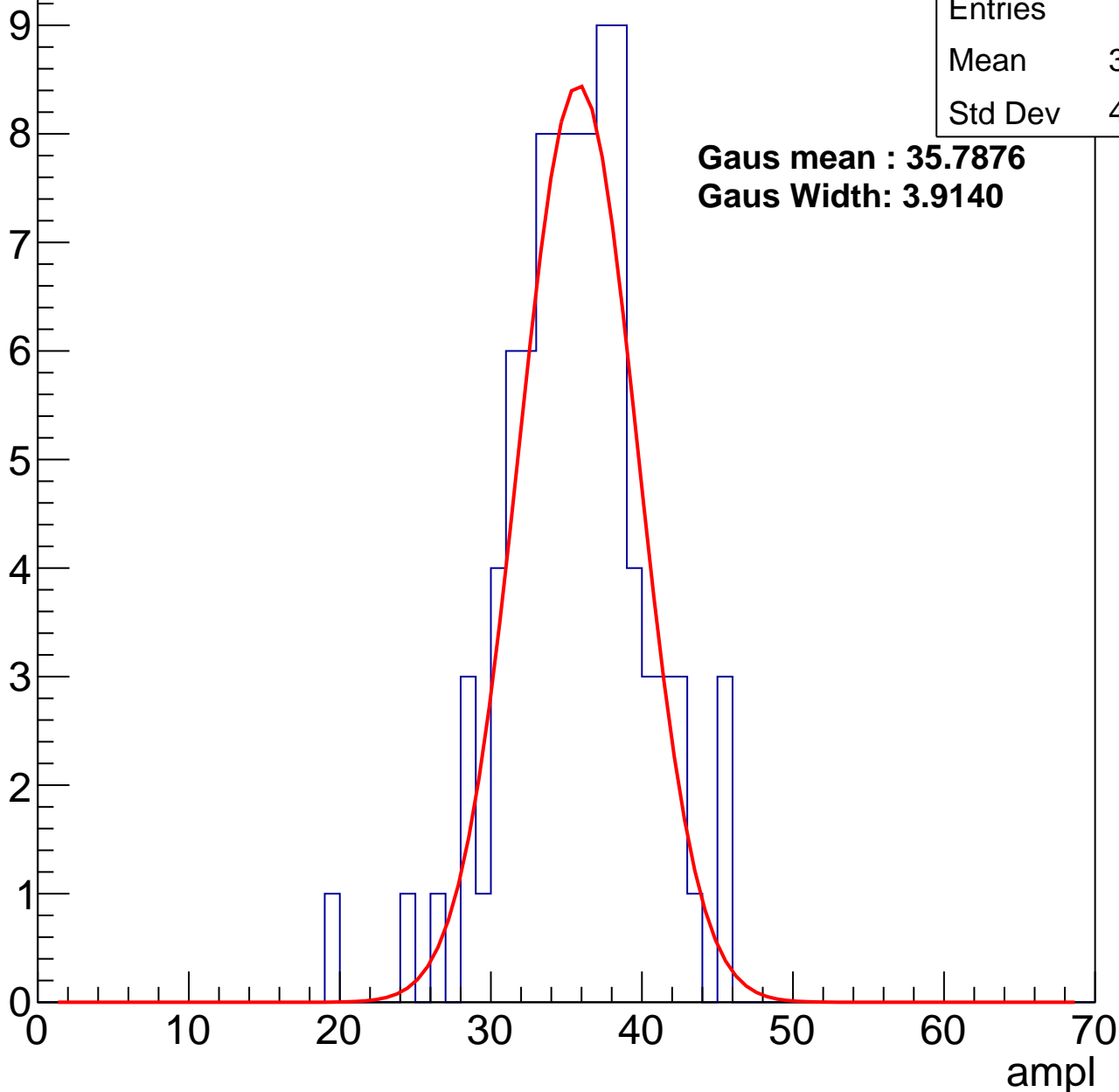
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	90
Mean	35.13
Std Dev	4.488

**Gaus mean : 35.7876**

**Gaus Width: 3.9140**



# B1L101S, U19-ch122, adc2

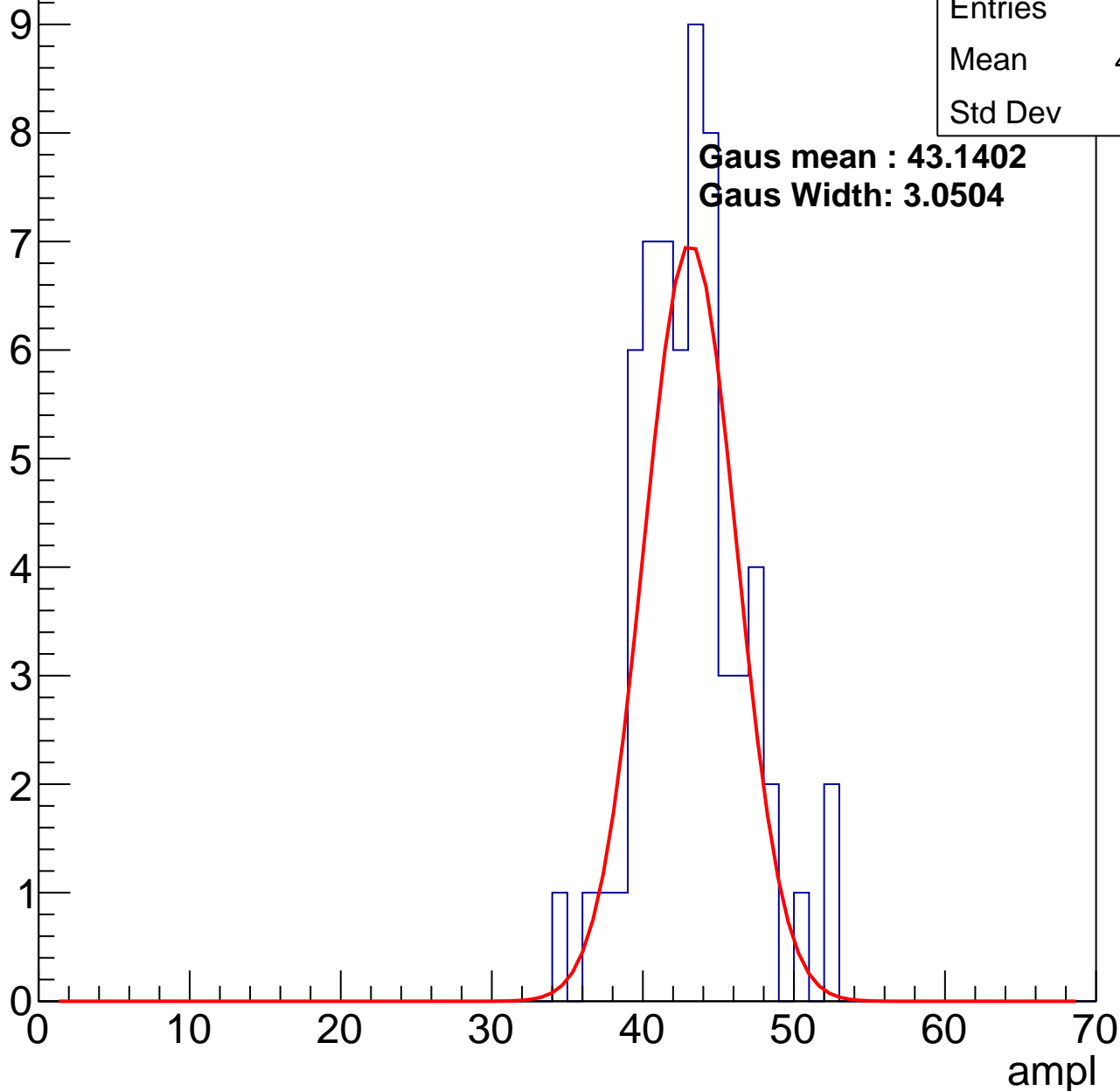
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	42.71
Std Dev	3.48

**Gaus mean : 43.1402**

**Gaus Width: 3.0504**

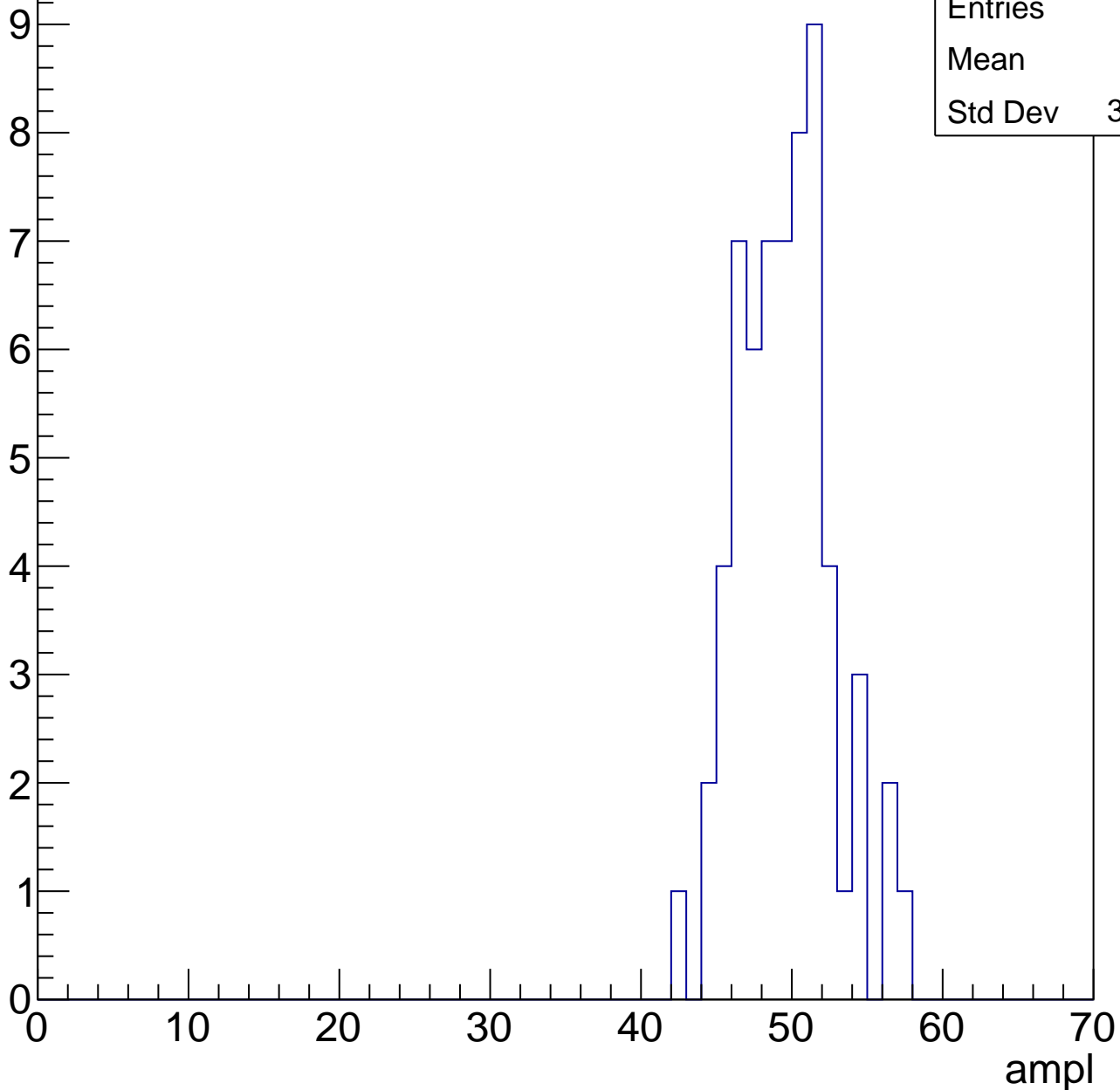


# B1L101S, U19-ch122, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	49.1
Std Dev	3.083

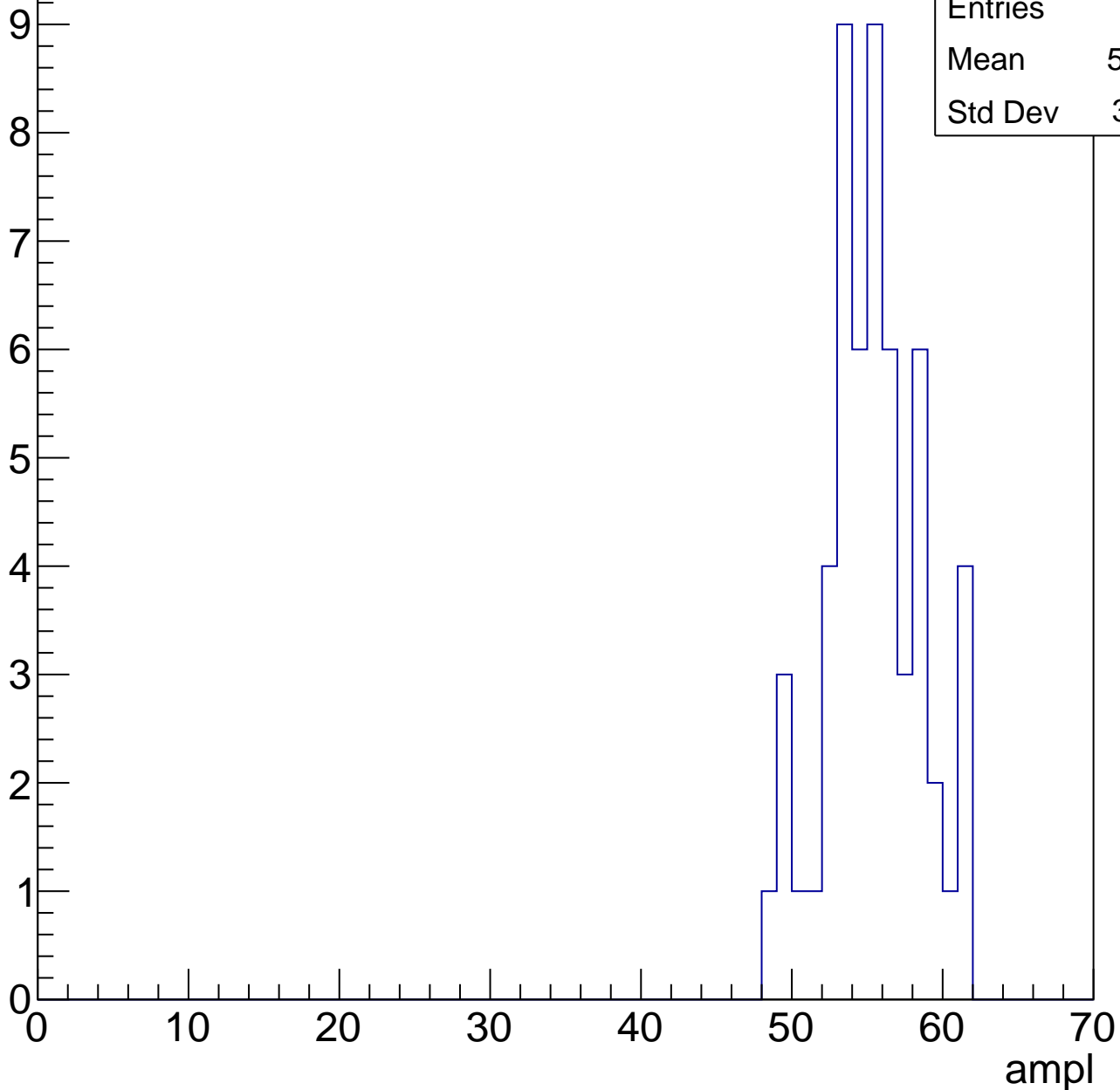


# B1L101S, U19-ch122, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	56
Mean	54.95
Std Dev	3.131

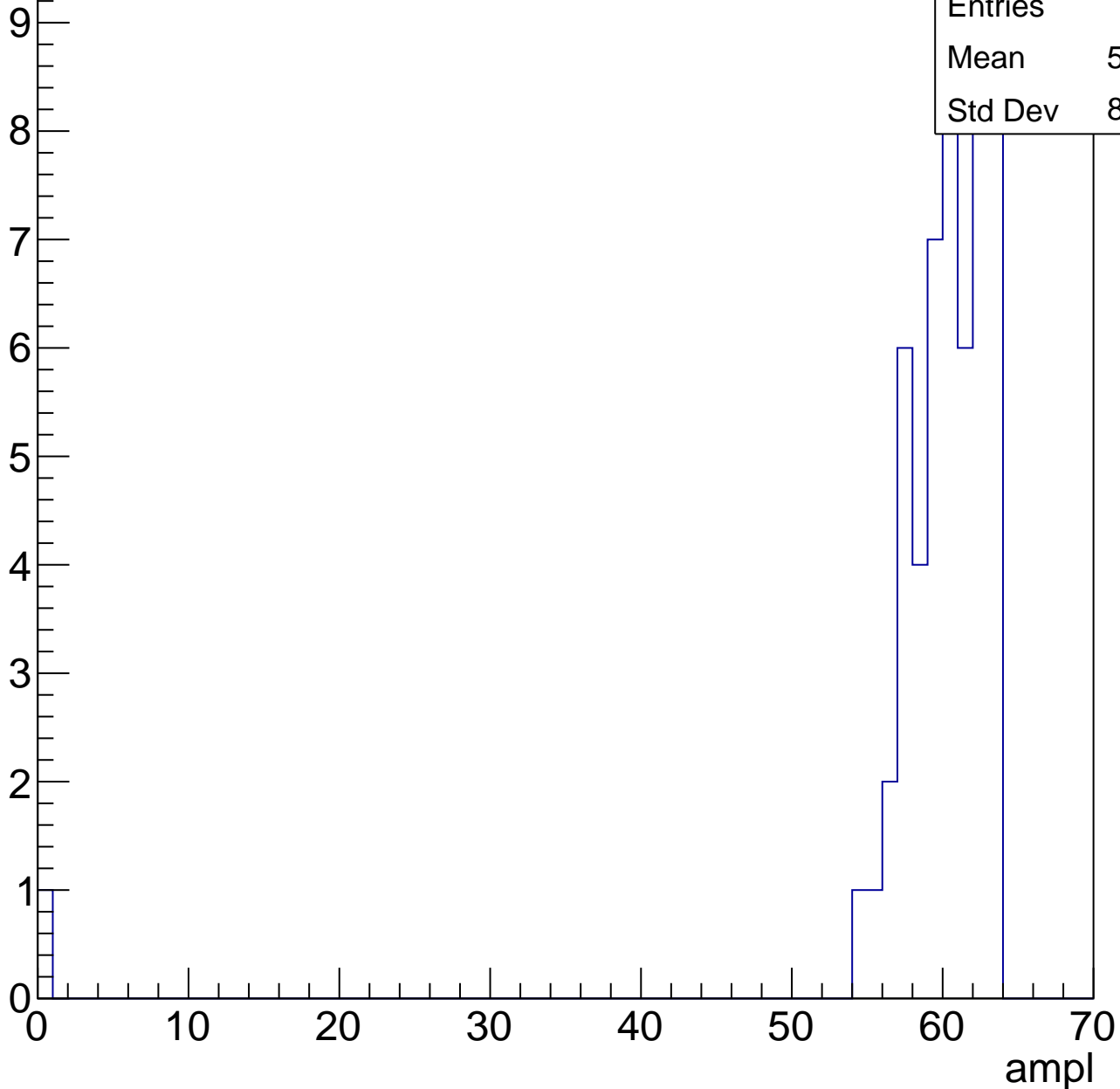


# B1L101S, U19-ch122, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

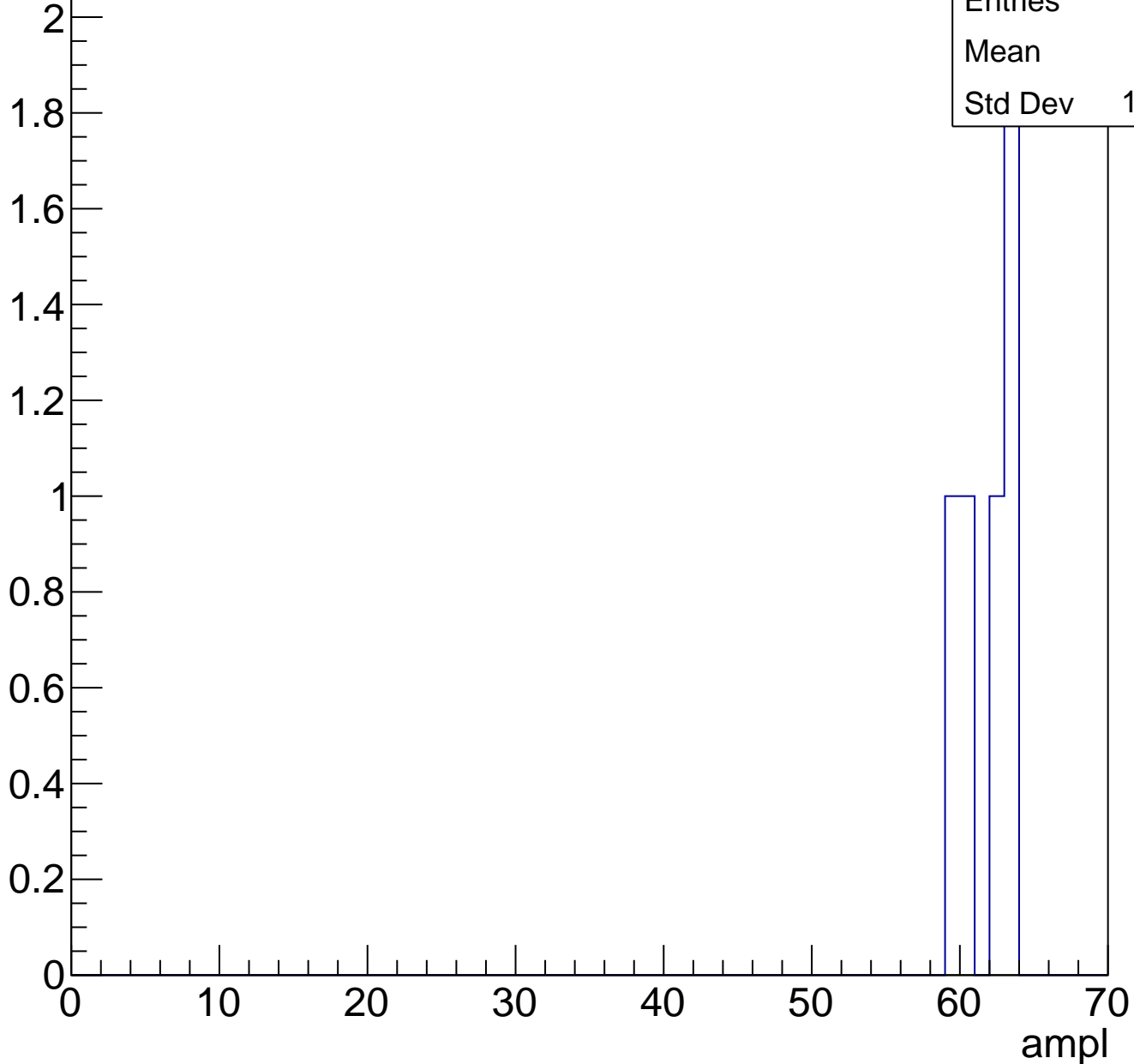
Entries	53
Mean	58.79
Std Dev	8.475



# B1L101S, U19-ch122, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U19-ch122, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U19-ch123, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	57
Mean	30.09
Std Dev	3.425

**Gaus mean : 31.1978**

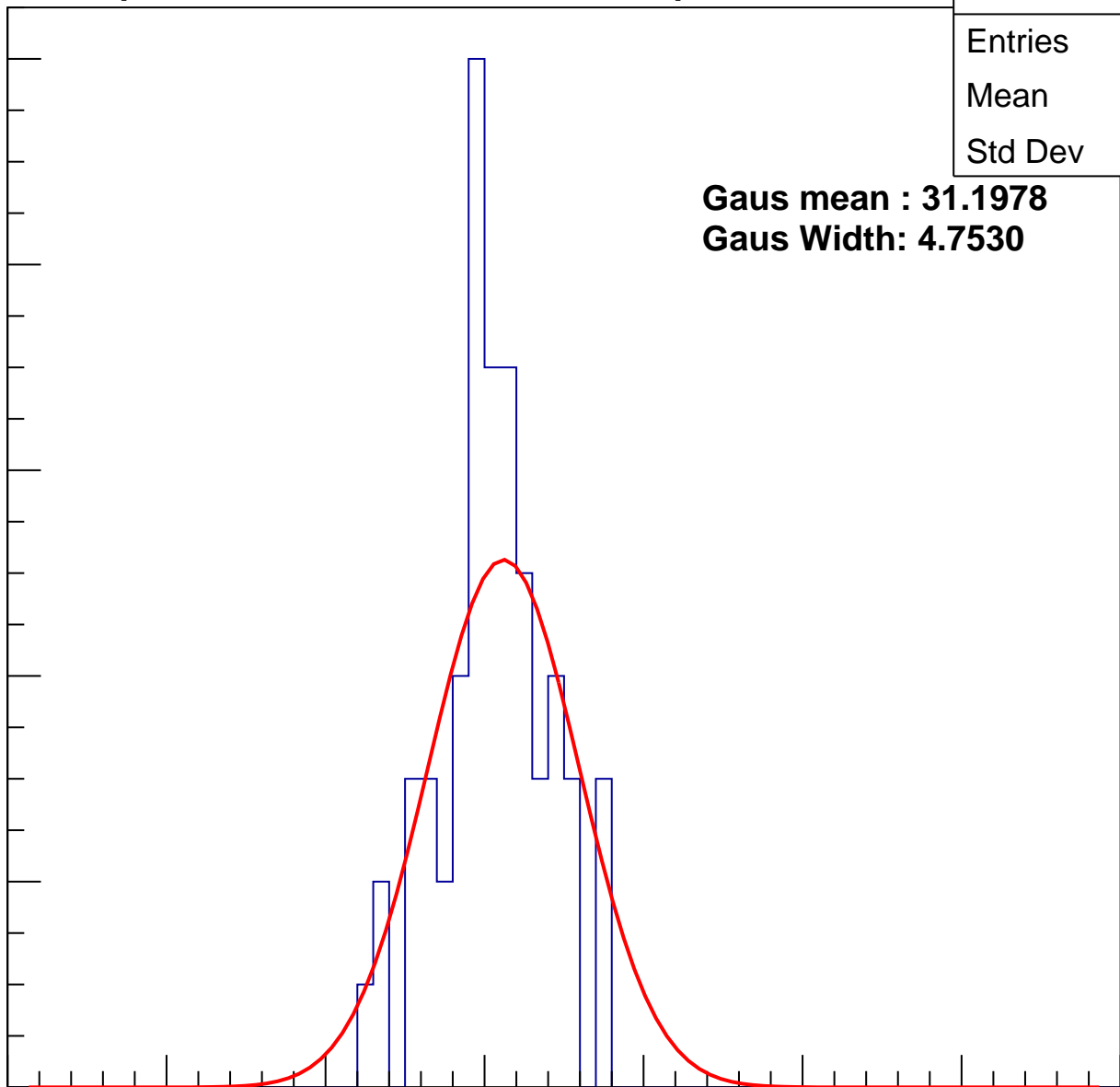
**Gaus Width: 4.7530**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U19-ch123, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	76
Mean	36.38
Std Dev	3.453

**Gaus mean : 36.6755**

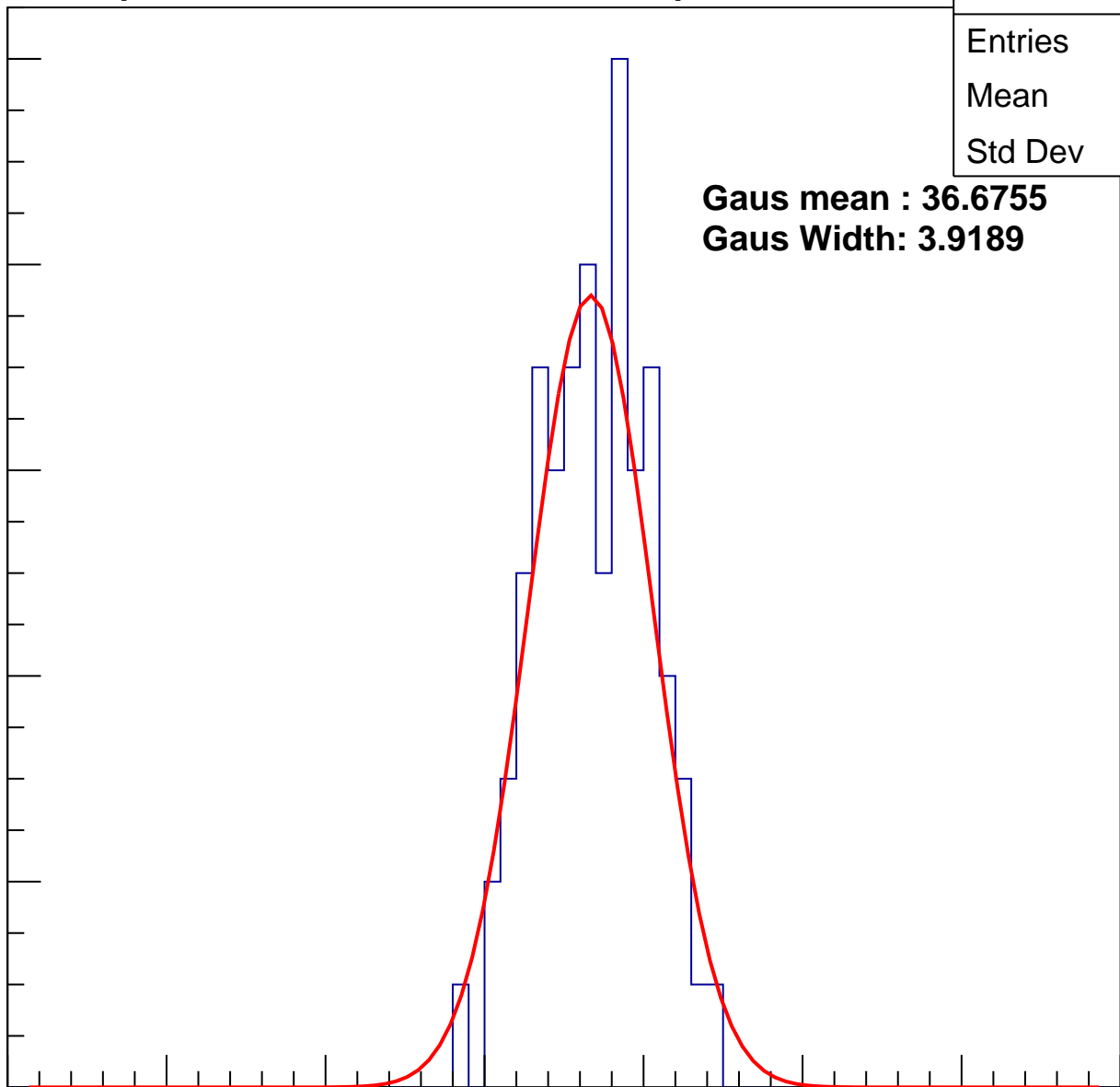
**Gaus Width: 3.9189**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U19-ch123, adc2

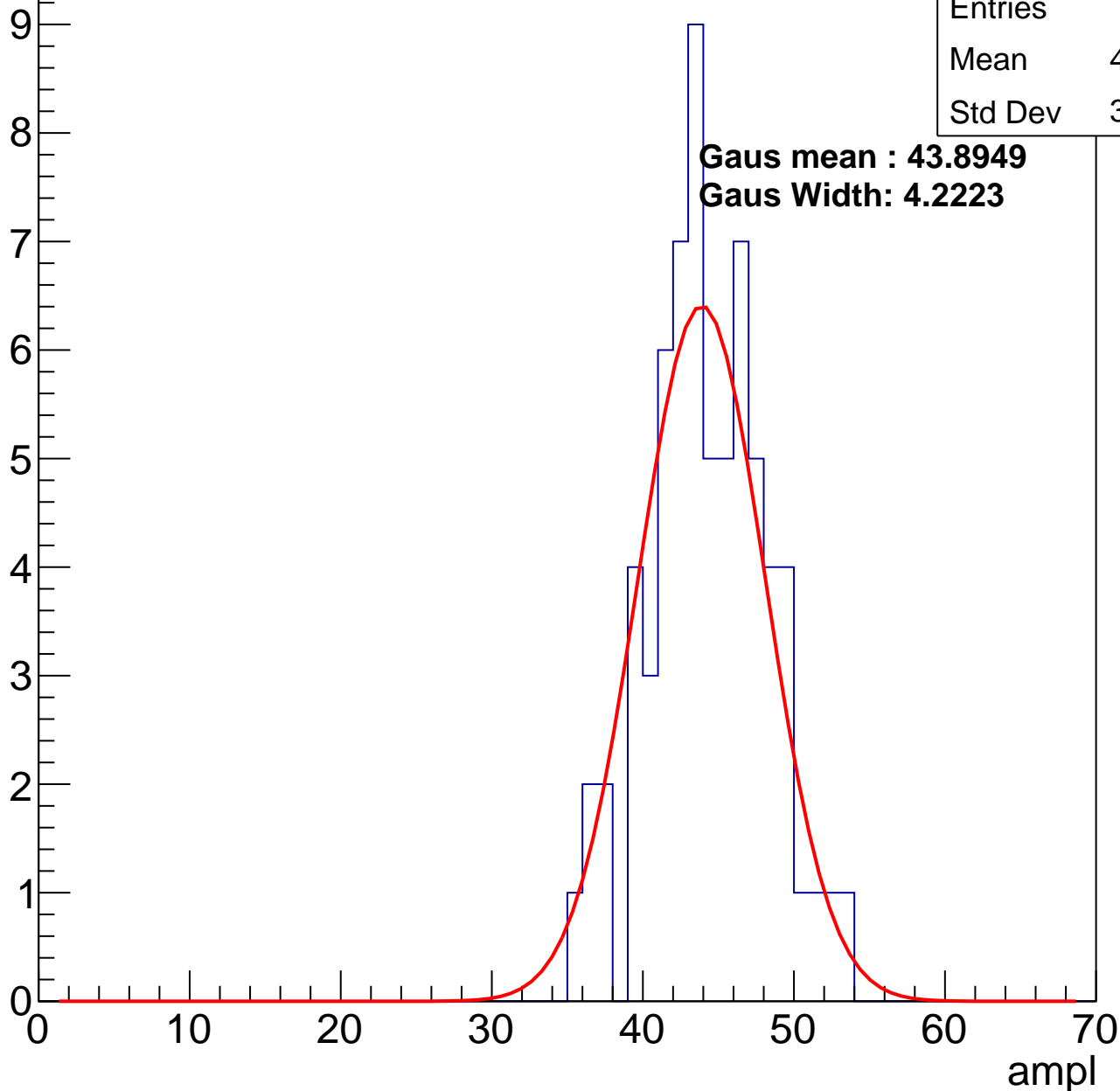
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	43.82
Std Dev	3.865

**Gaus mean : 43.8949**

**Gaus Width: 4.2223**

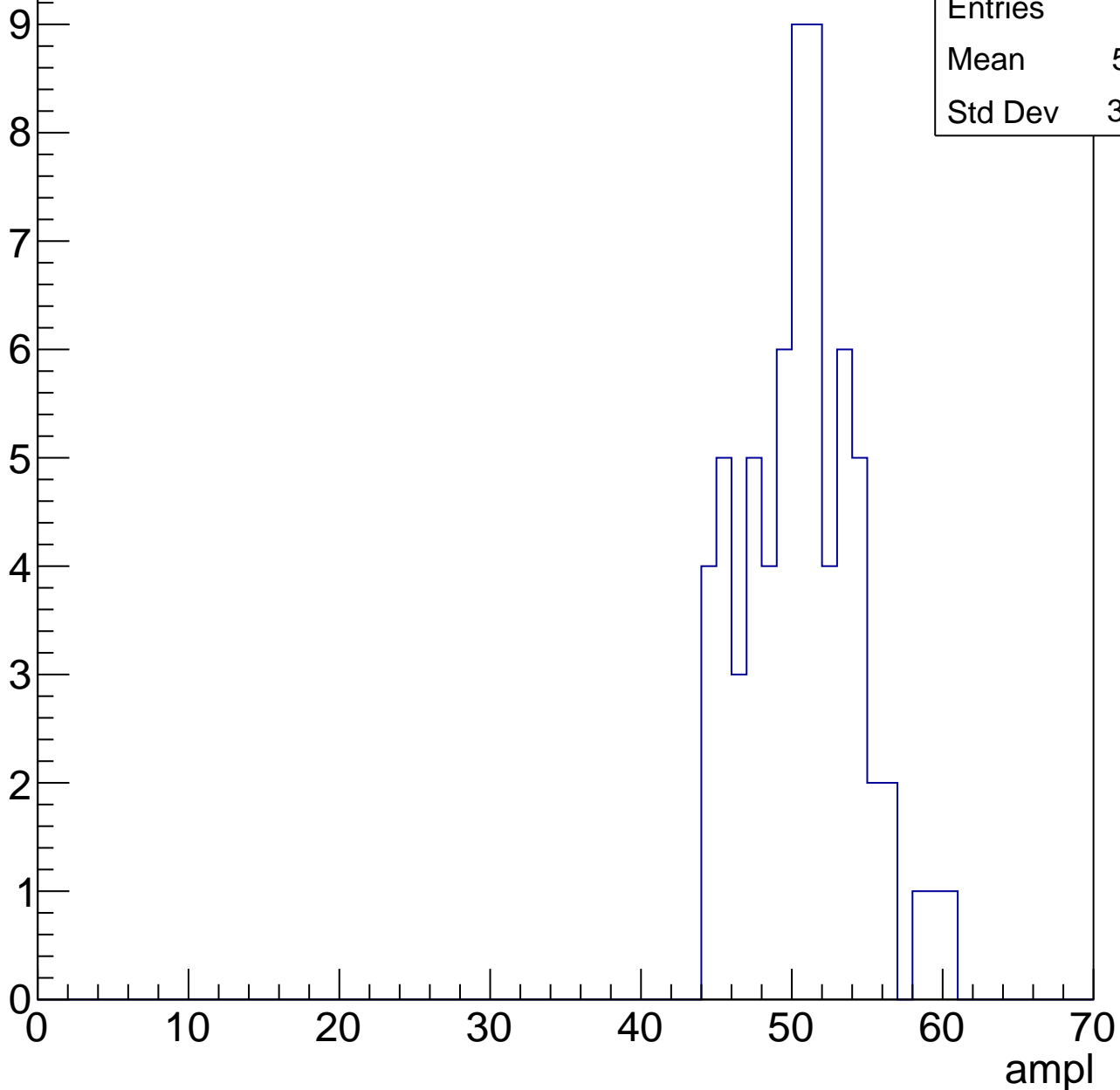


# B1L101S, U19-ch123, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

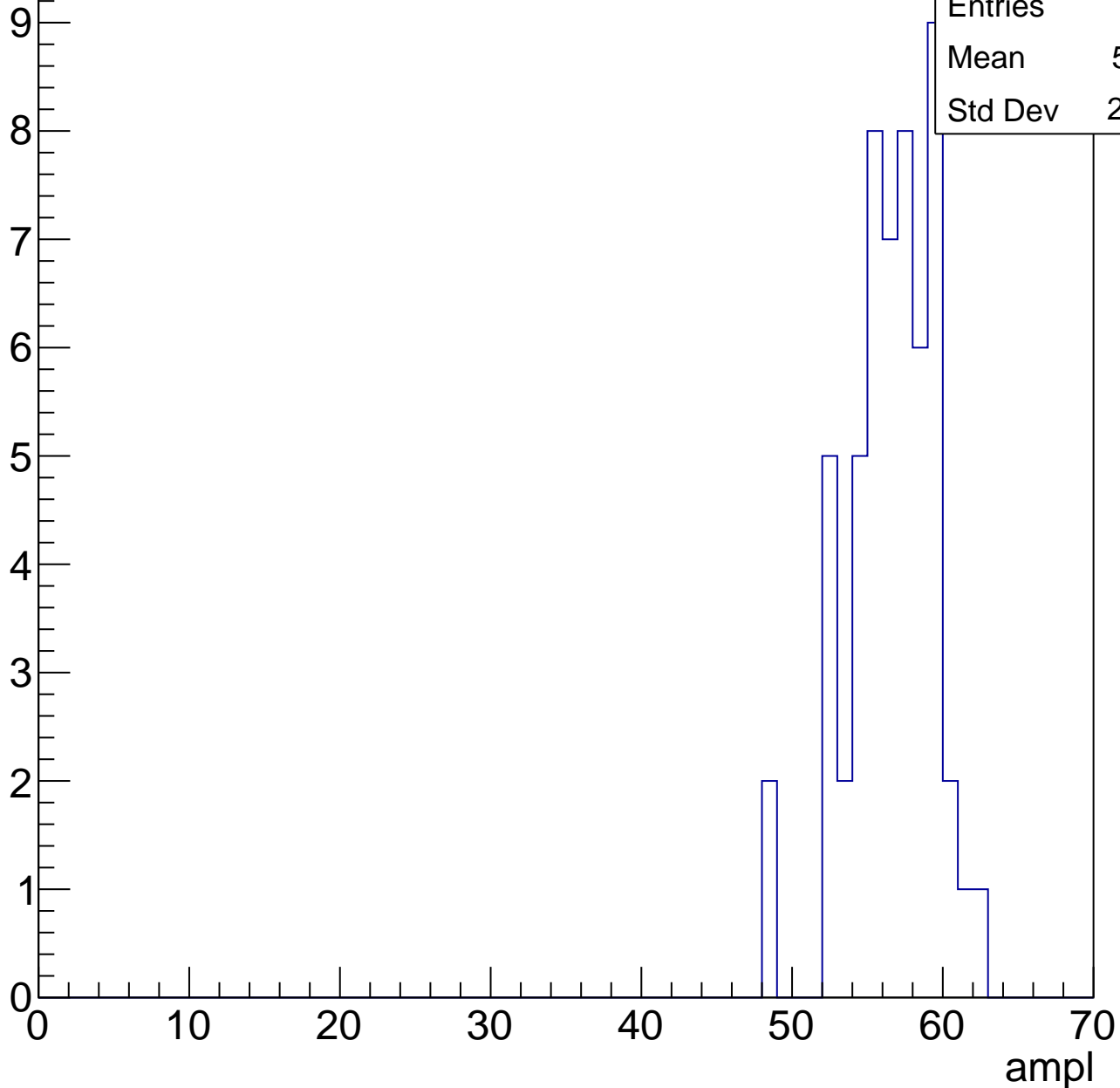
Entries	67
Mean	50.21
Std Dev	3.679



# B1L101S, U19-ch123, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

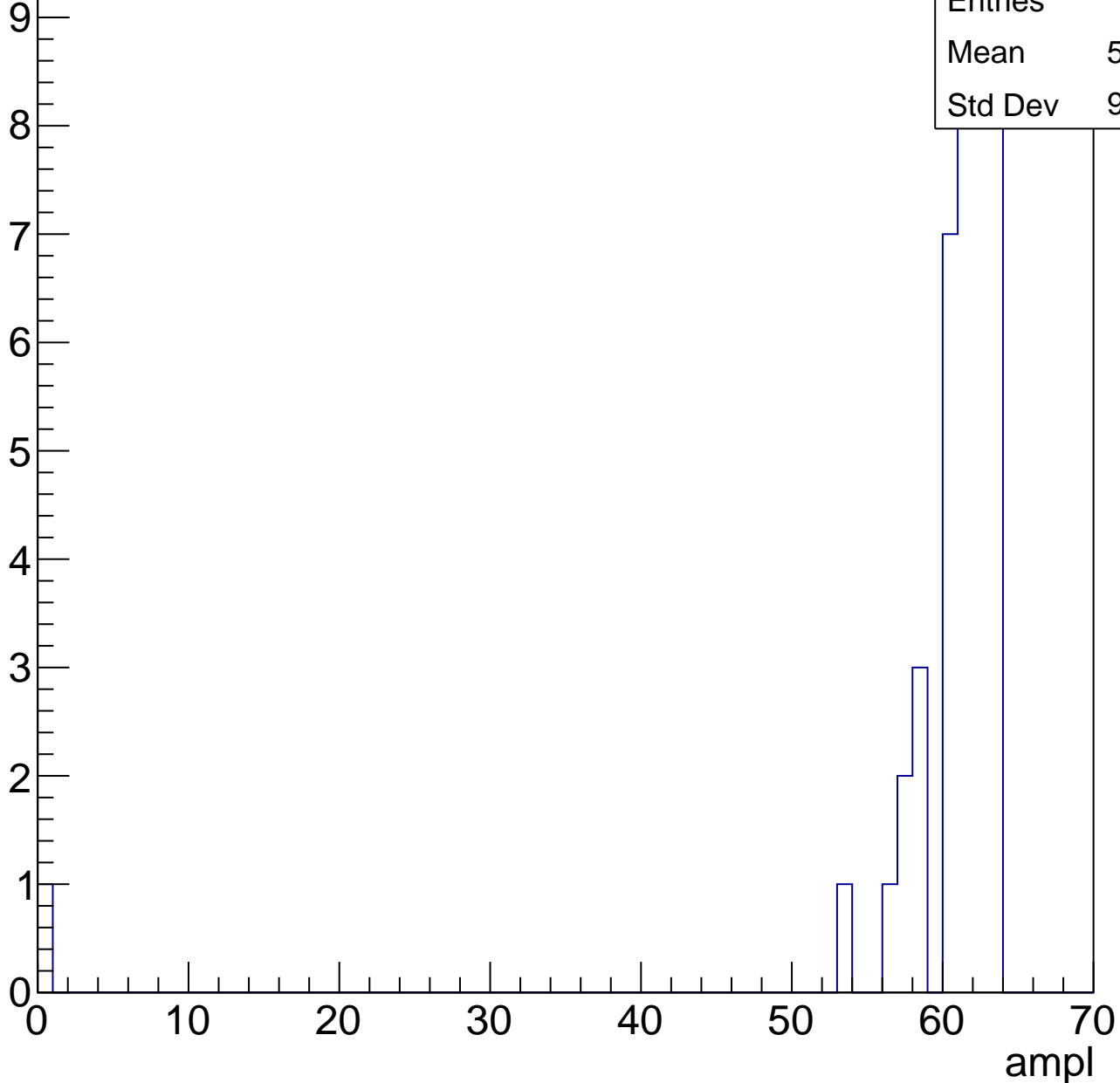


# B1L101S, U19-ch123, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	41
Mean	59.27
Std Dev	9.625



# B1L101S, U19-ch123, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

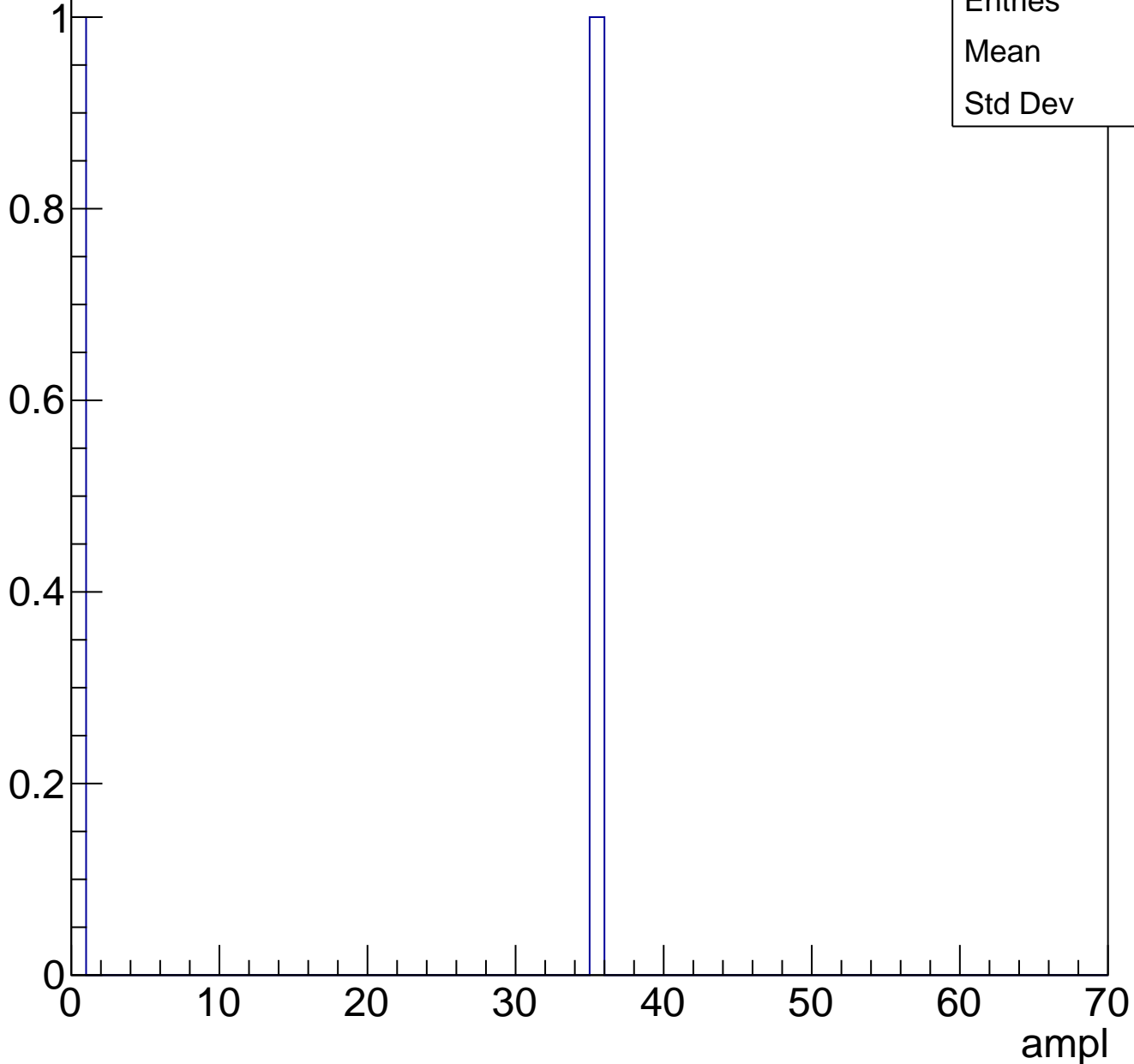




# B1L101S, U19-ch123, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U19-ch124, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	68
Mean	28.46
Std Dev	6.035

**Gaus mean : 29.5142**

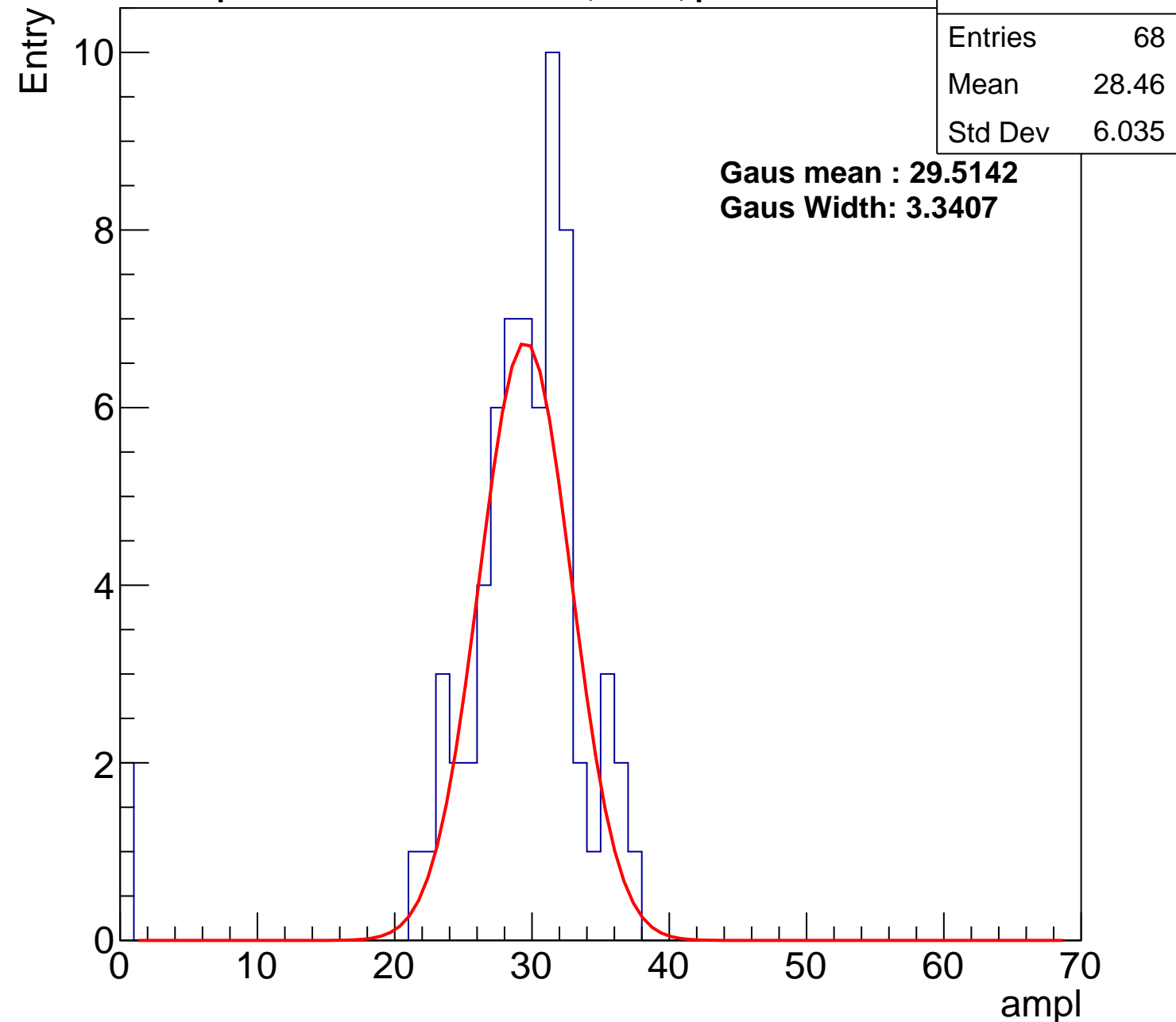
**Gaus Width: 3.3407**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U19-ch124, adc1

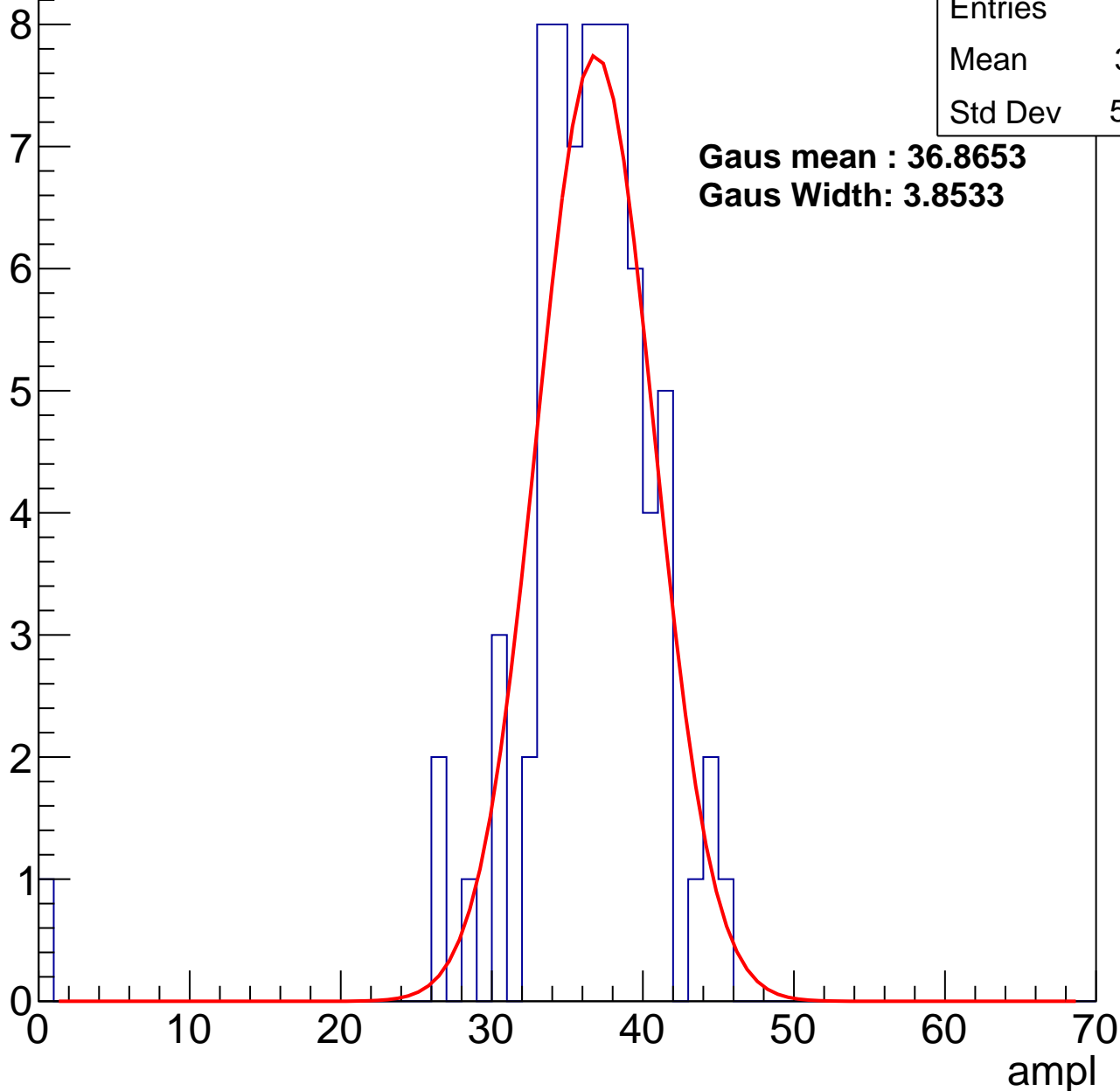
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	75
Mean	35.71
Std Dev	5.592

**Gaus mean : 36.8653**

**Gaus Width: 3.8533**



# B1L101S, U19-ch124, adc2

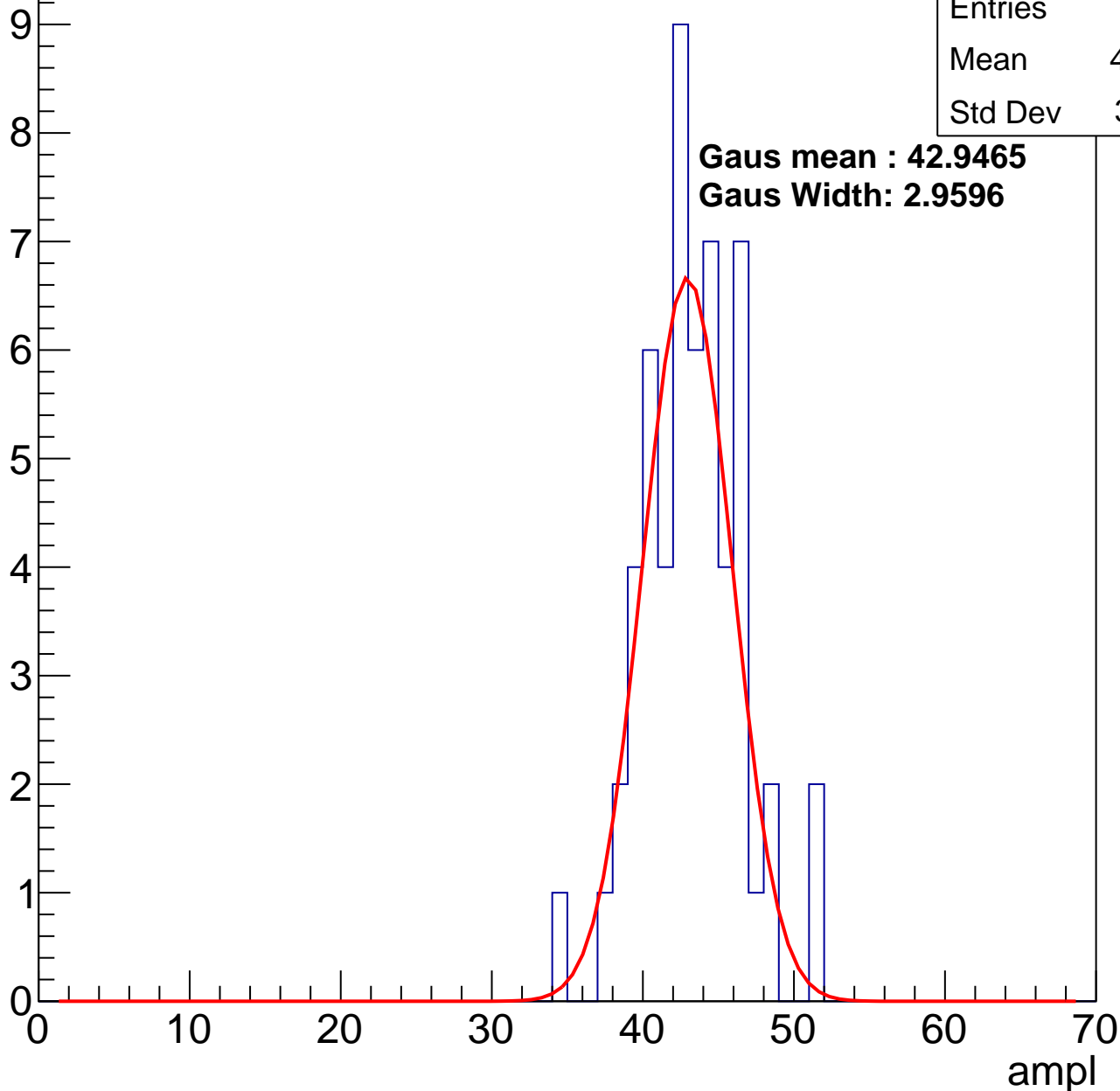
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	56
Mean	42.82
Std Dev	3.241

**Gaus mean : 42.9465**

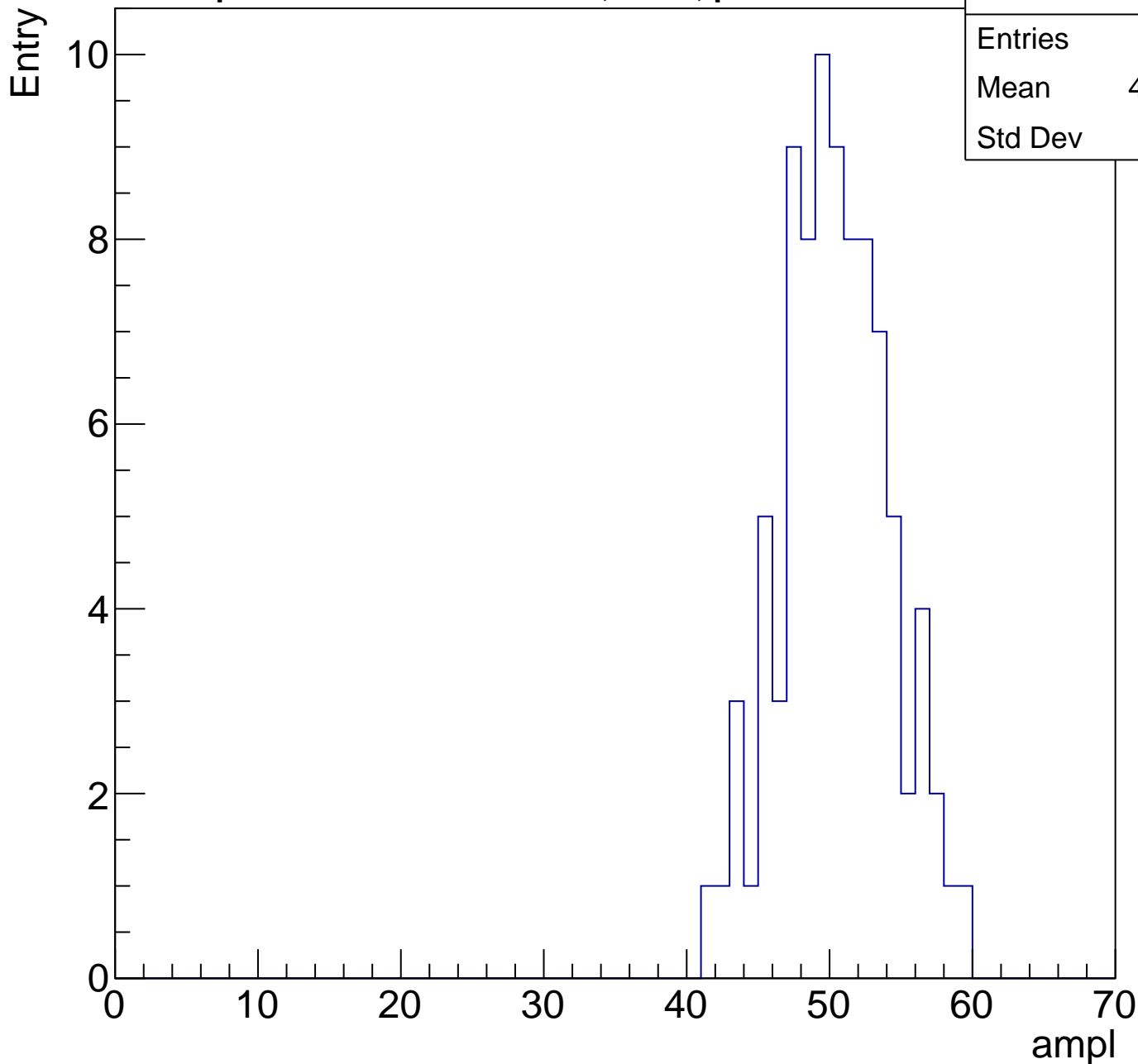
**Gaus Width: 2.9596**



# B1L101S, U19-ch124, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	88
Mean	49.95
Std Dev	3.76

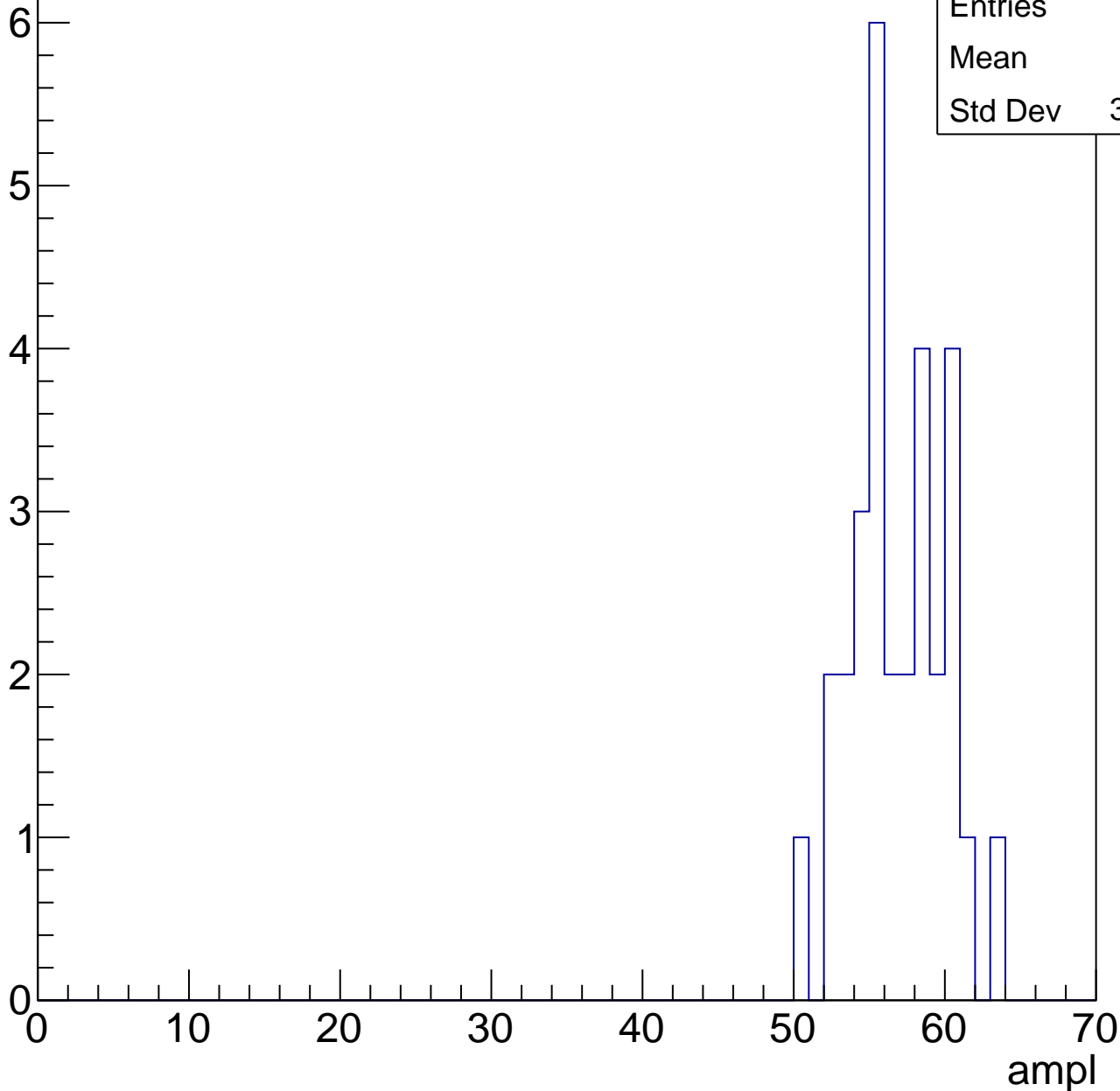


# B1L101S, U19-ch124, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	30
Mean	56.4
Std Dev	3.018

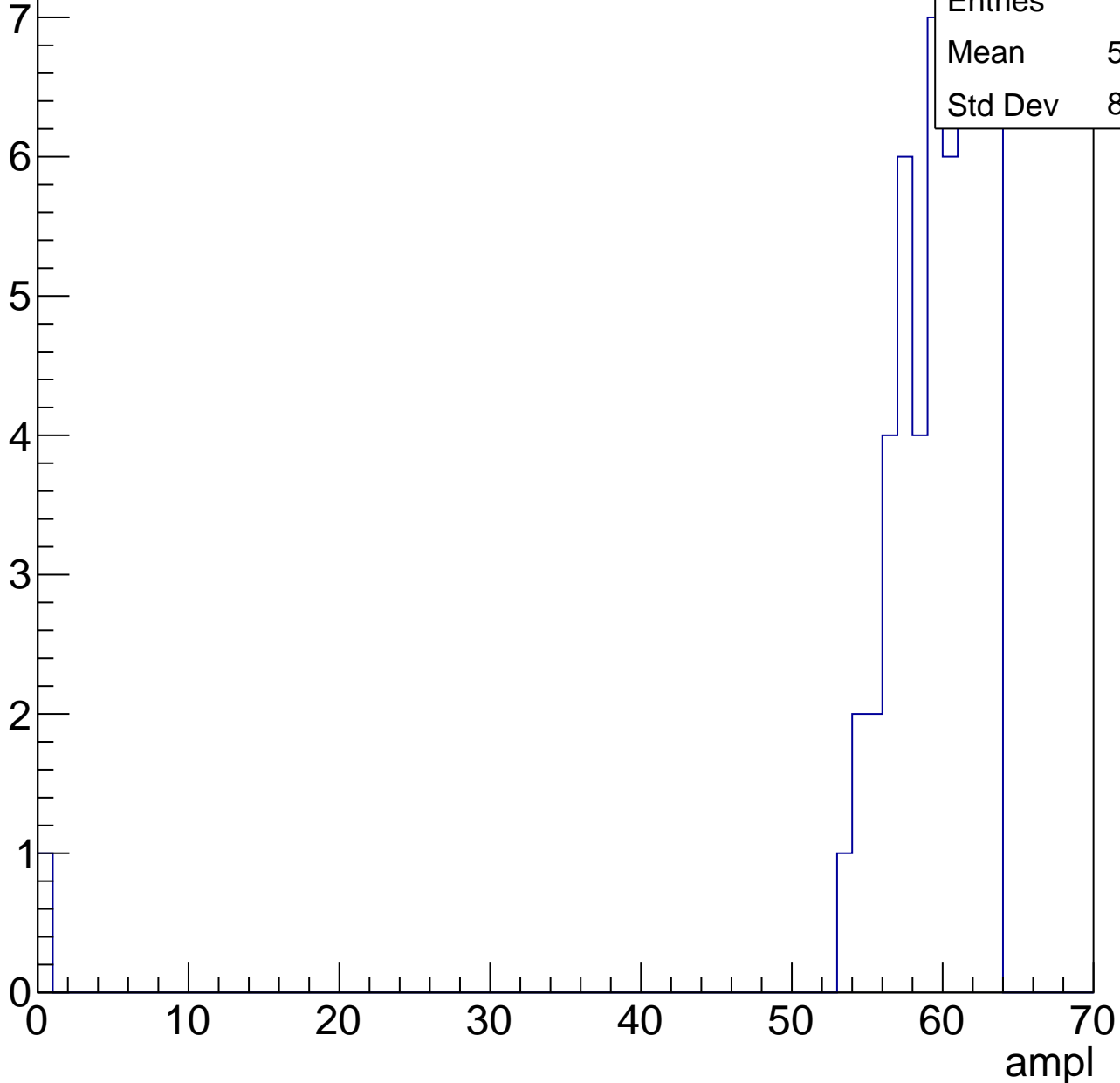


# B1L101S, U19-ch124, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

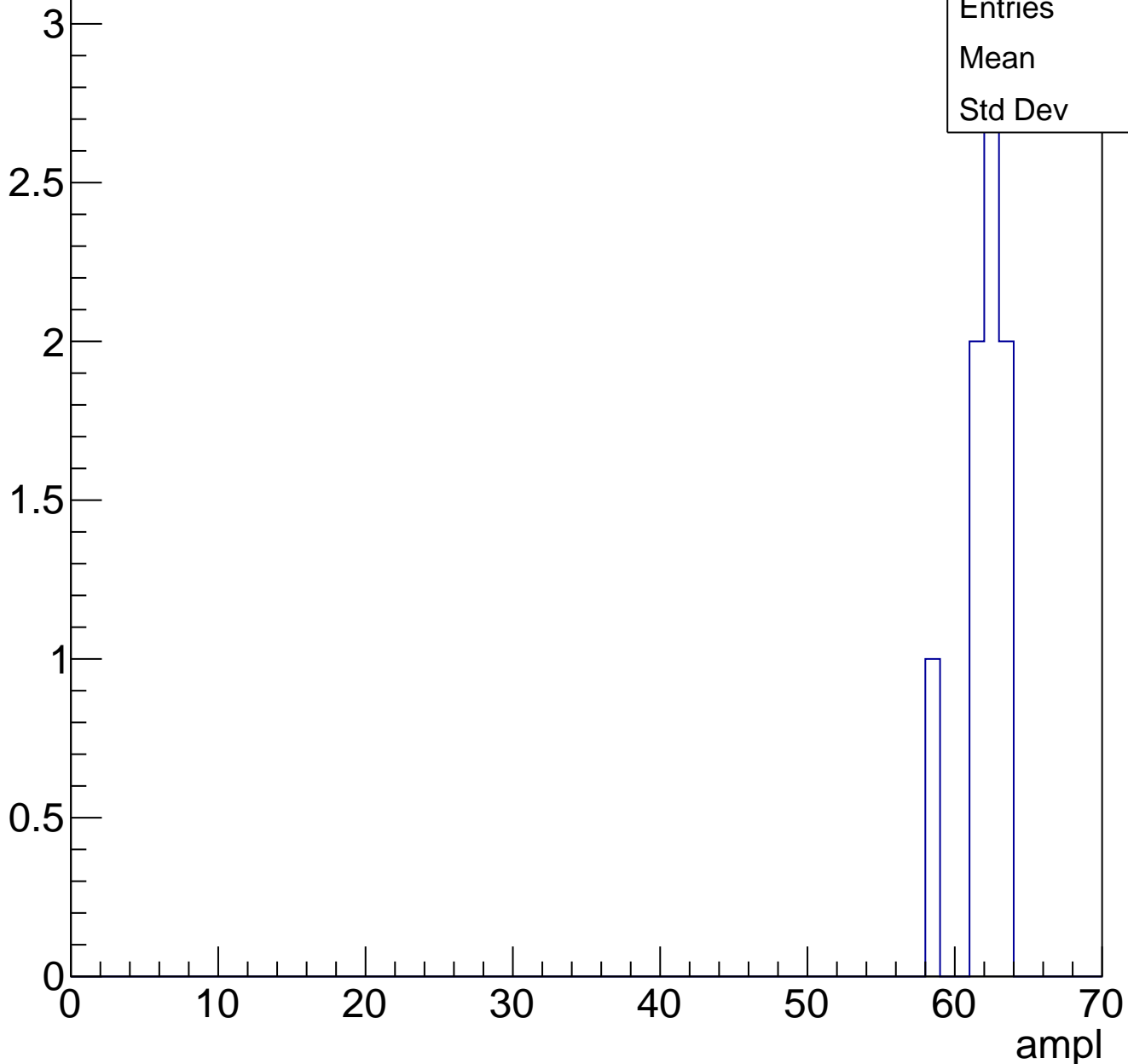
Entries	54
Mean	58.22
Std Dev	8.432



# B1L101S, U19-ch124, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U19-ch124, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U19-ch125, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	73
Mean	30.48
Std Dev	3.315

**Gaus mean : 30.7063**

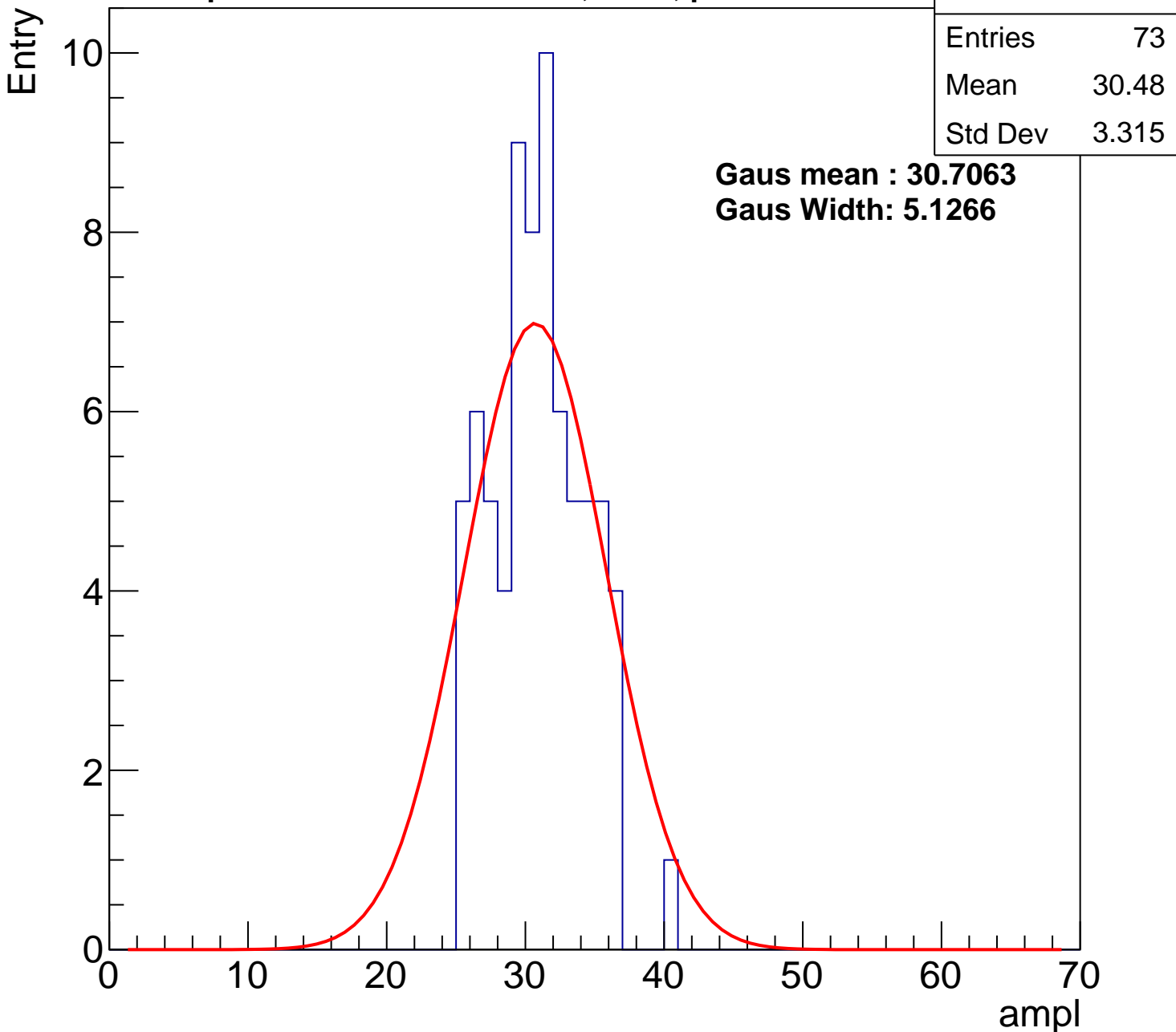
**Gaus Width: 5.1266**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U19-ch125, adc1

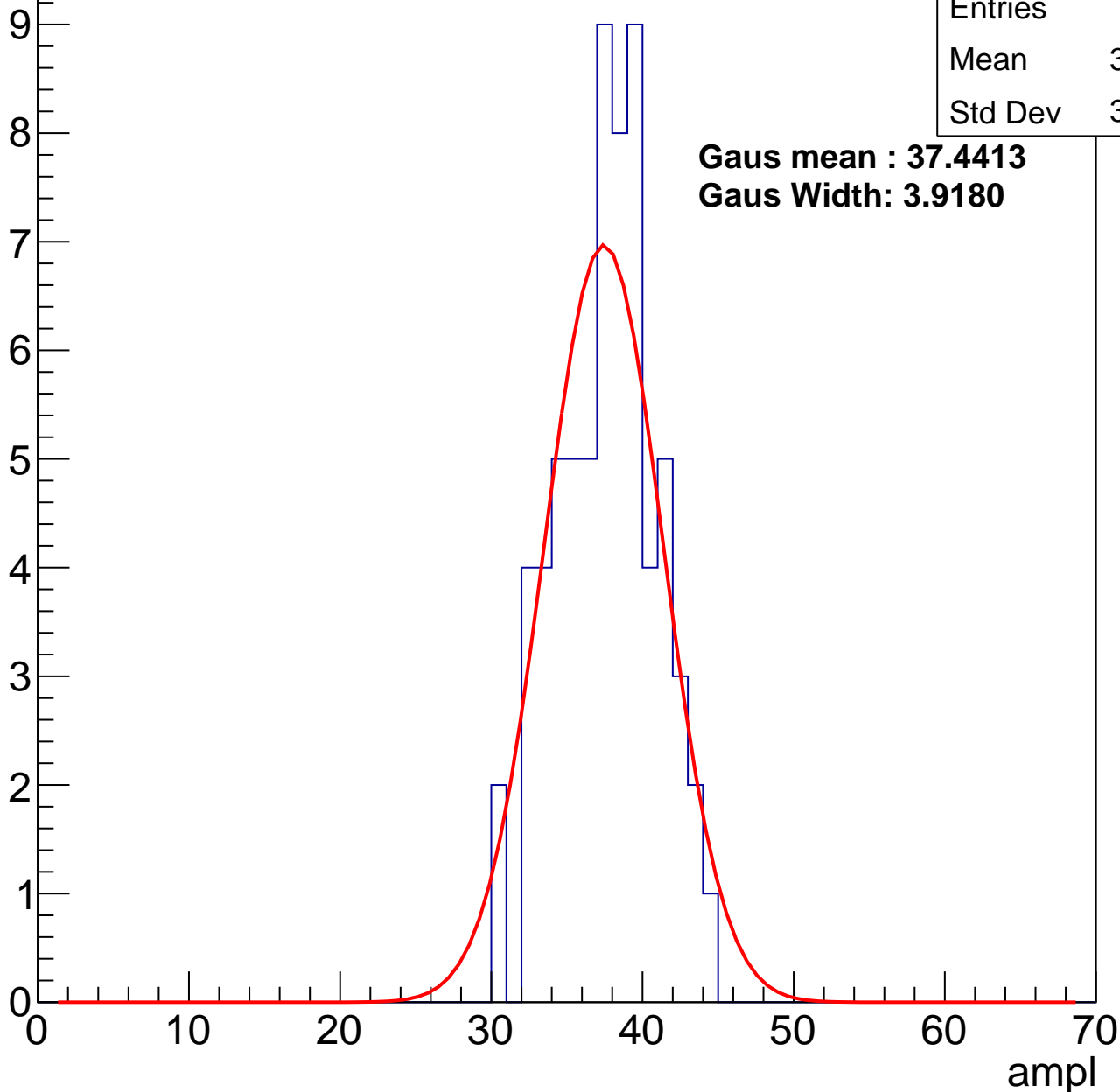
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	66
Mean	37.18
Std Dev	3.224

**Gaus mean : 37.4413**

**Gaus Width: 3.9180**



# B1L101S, U19-ch125, adc2

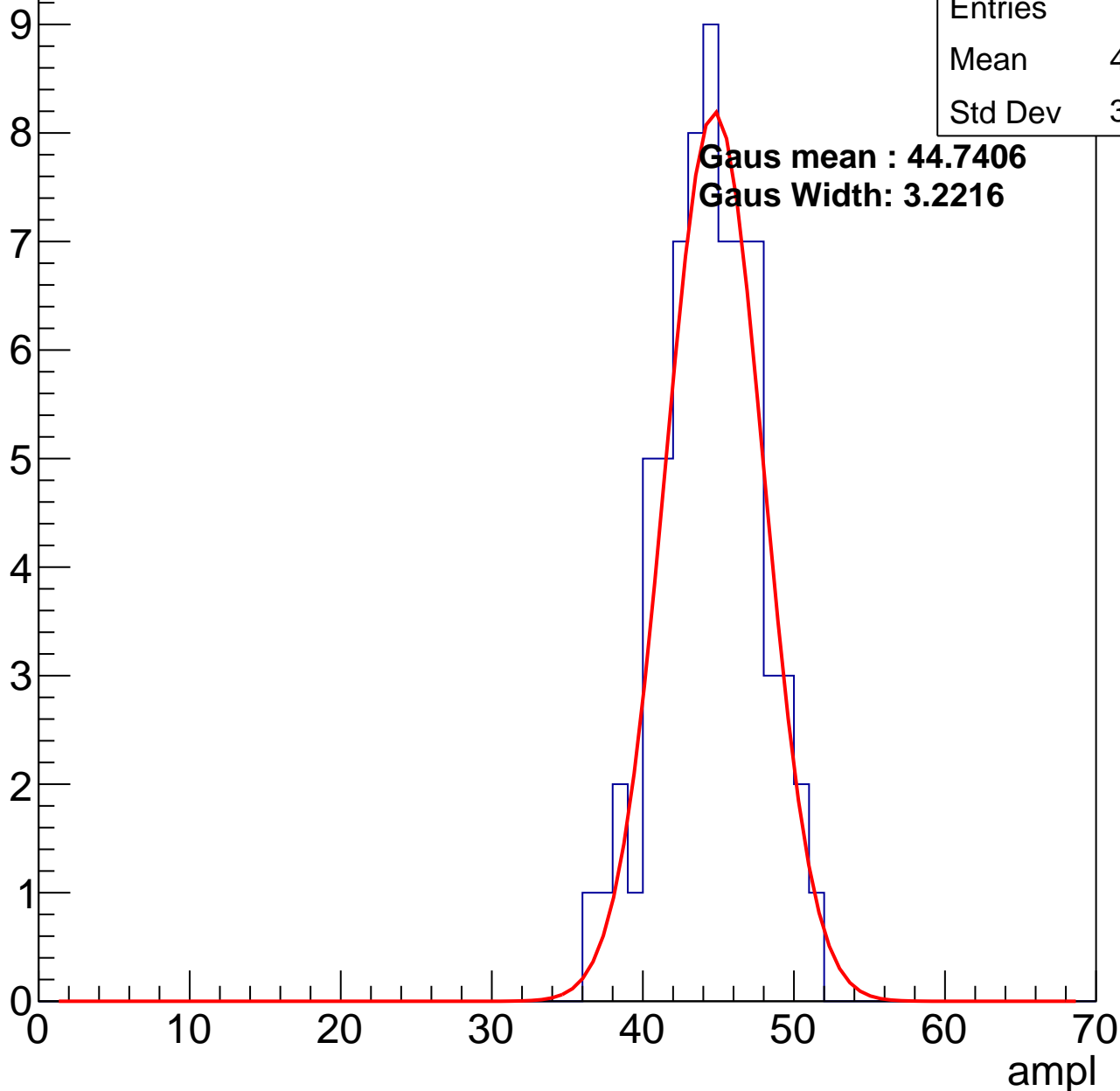
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	43.99
Std Dev	3.215

**Gaus mean : 44.7406**

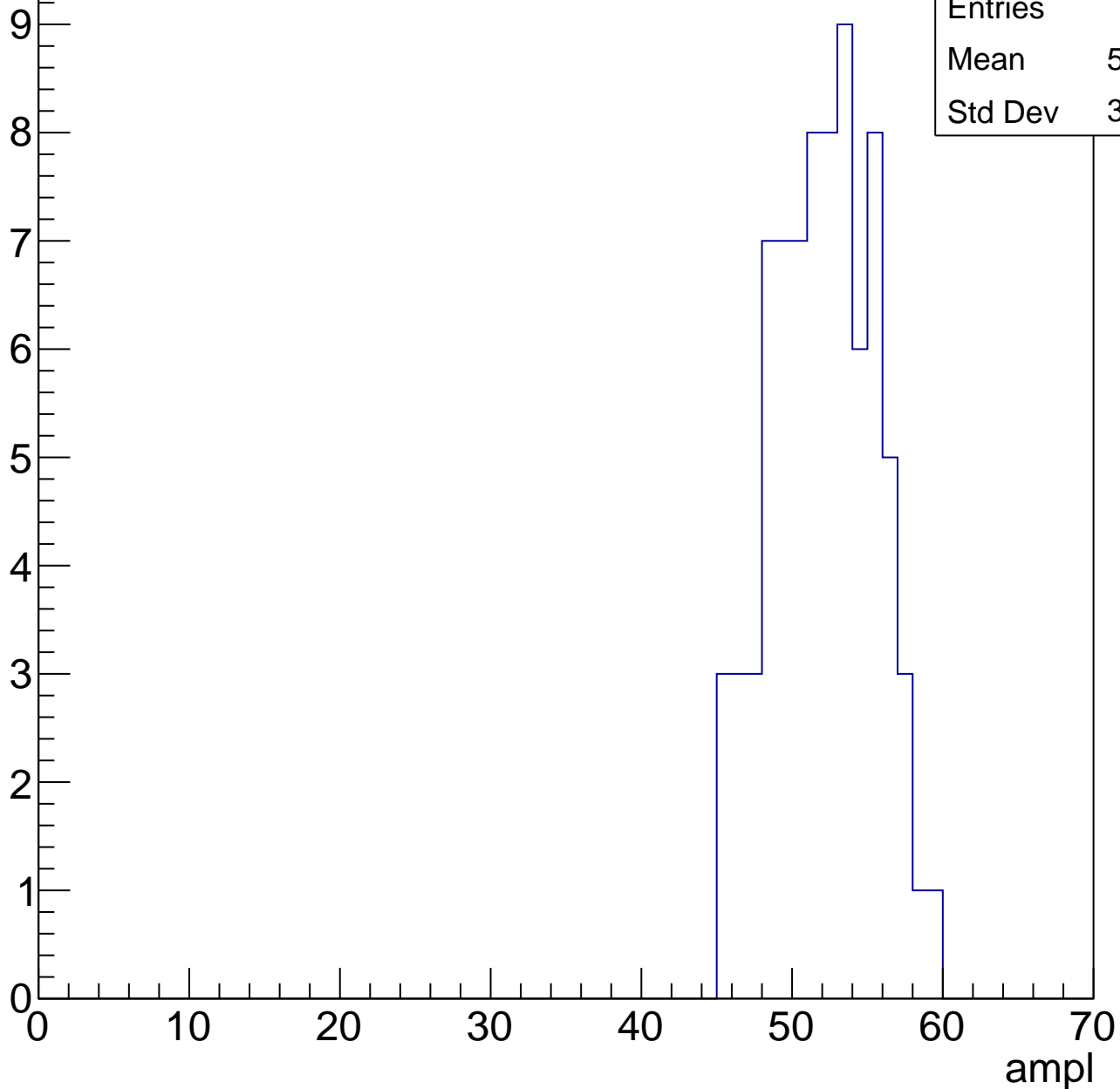
**Gaus Width: 3.2216**



# B1L101S, U19-ch125, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

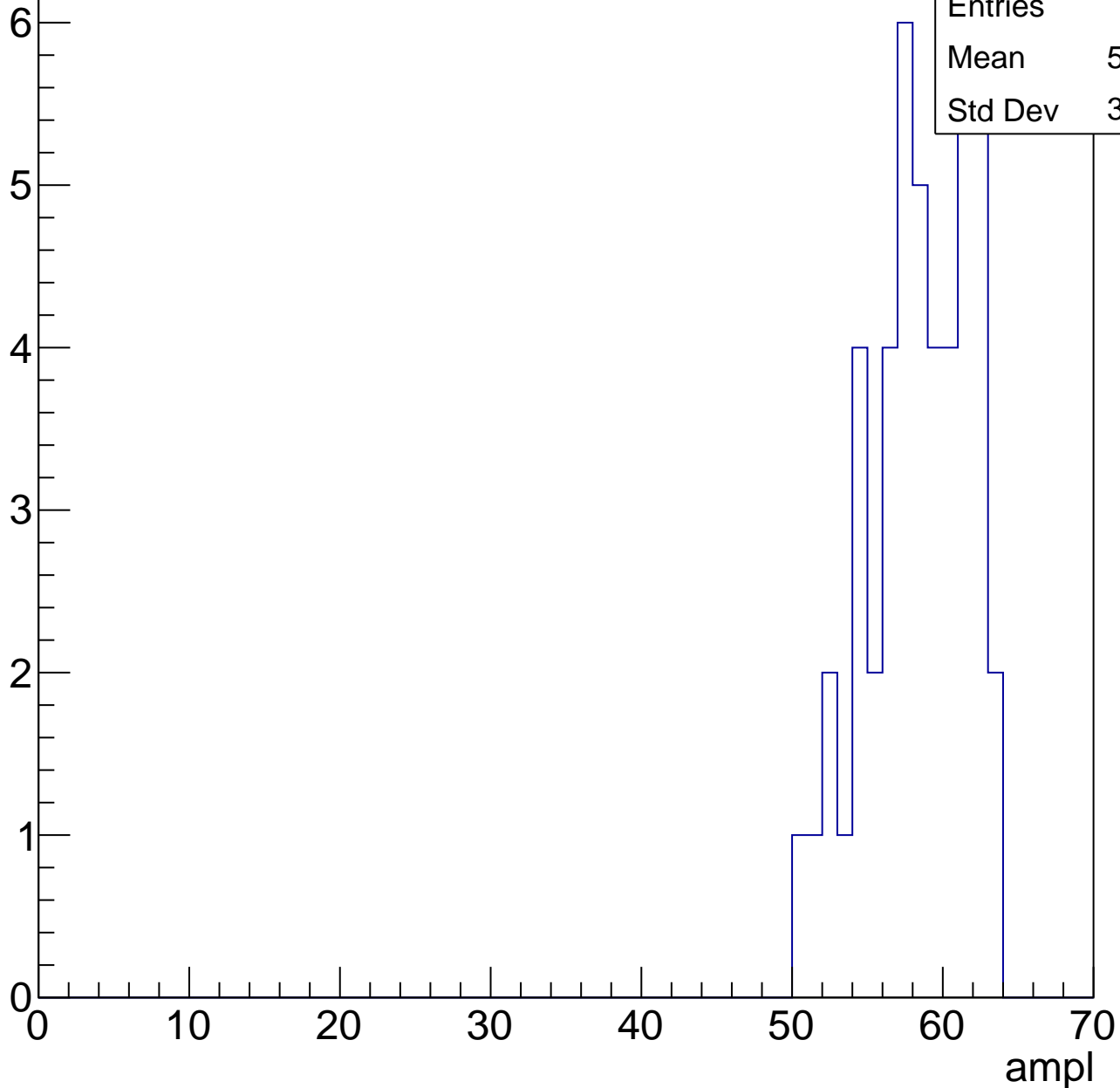
Entry



# B1L101S, U19-ch125, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U19-ch125, adc5

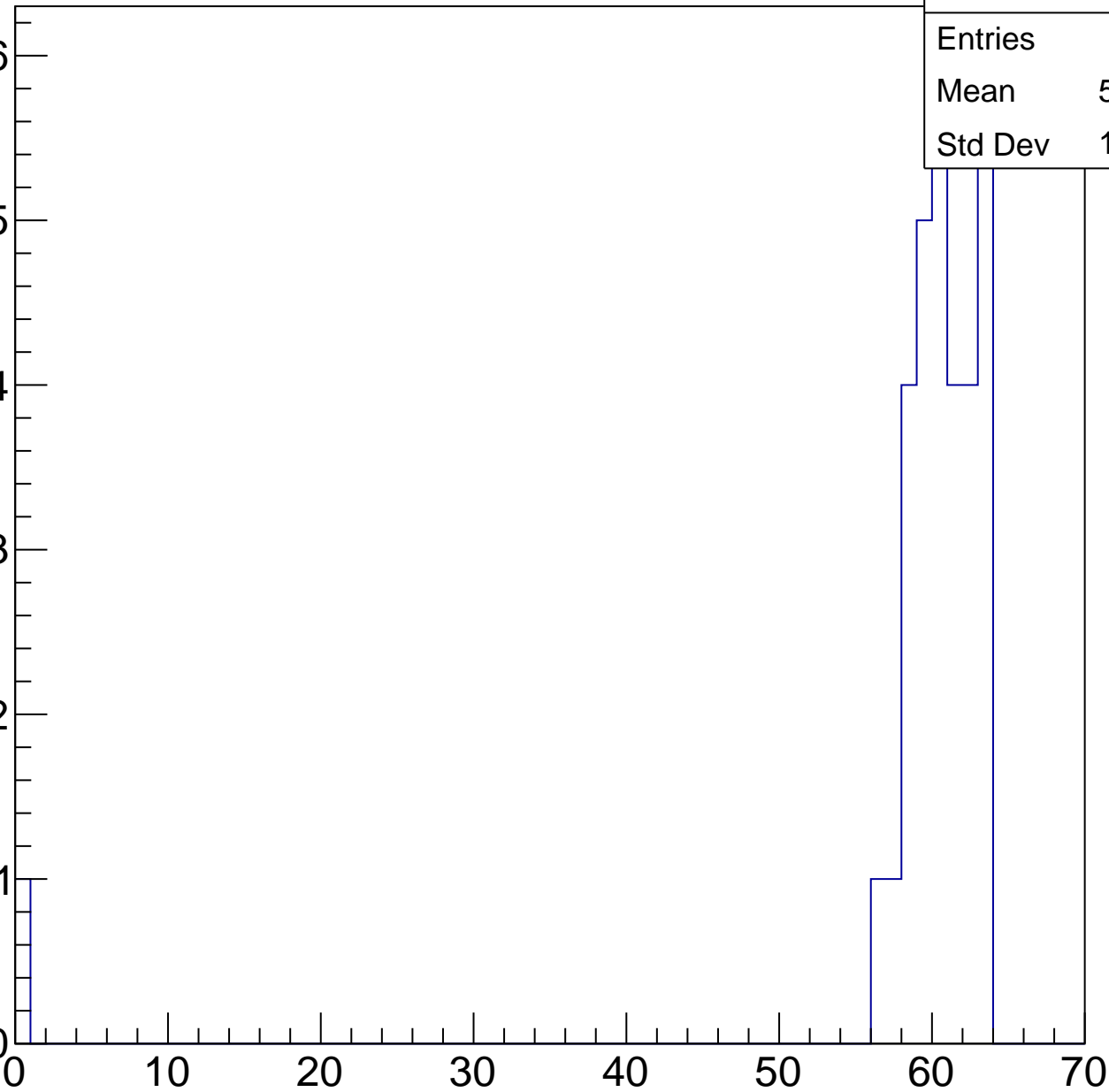
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

6  
5  
4  
3  
2  
1  
0

Entries	32
Mean	58.44
Std Dev	10.67

ampl



# B1L101S, U19-ch125, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	2
Mean	63
Std Dev	0

0 10 20 30 40 50 60 70

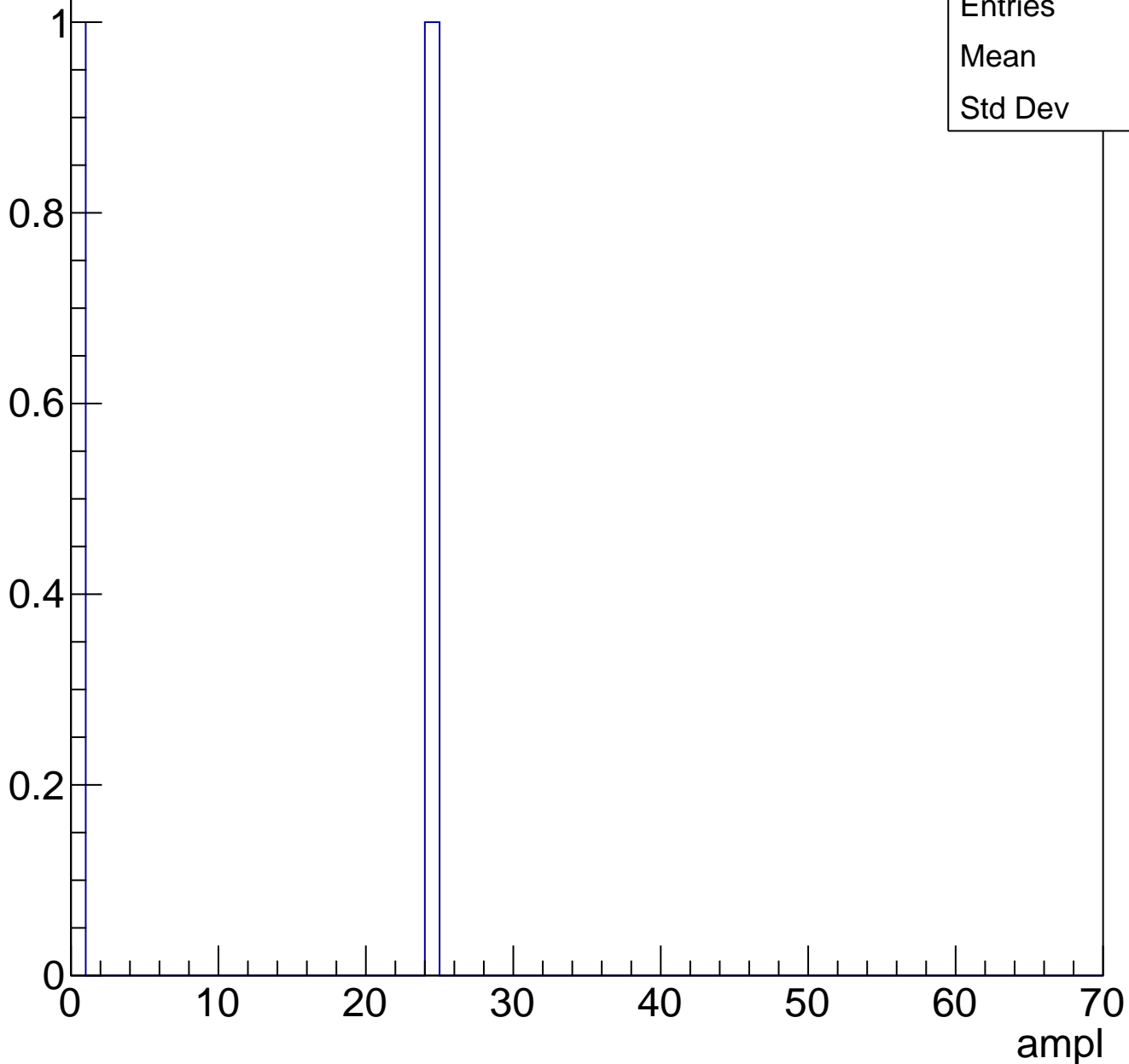
ampl



# B1L101S, U19-ch125, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U19-ch126, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	83
Mean	27.7
Std Dev	7.918

**Gaus mean : 28.8769**

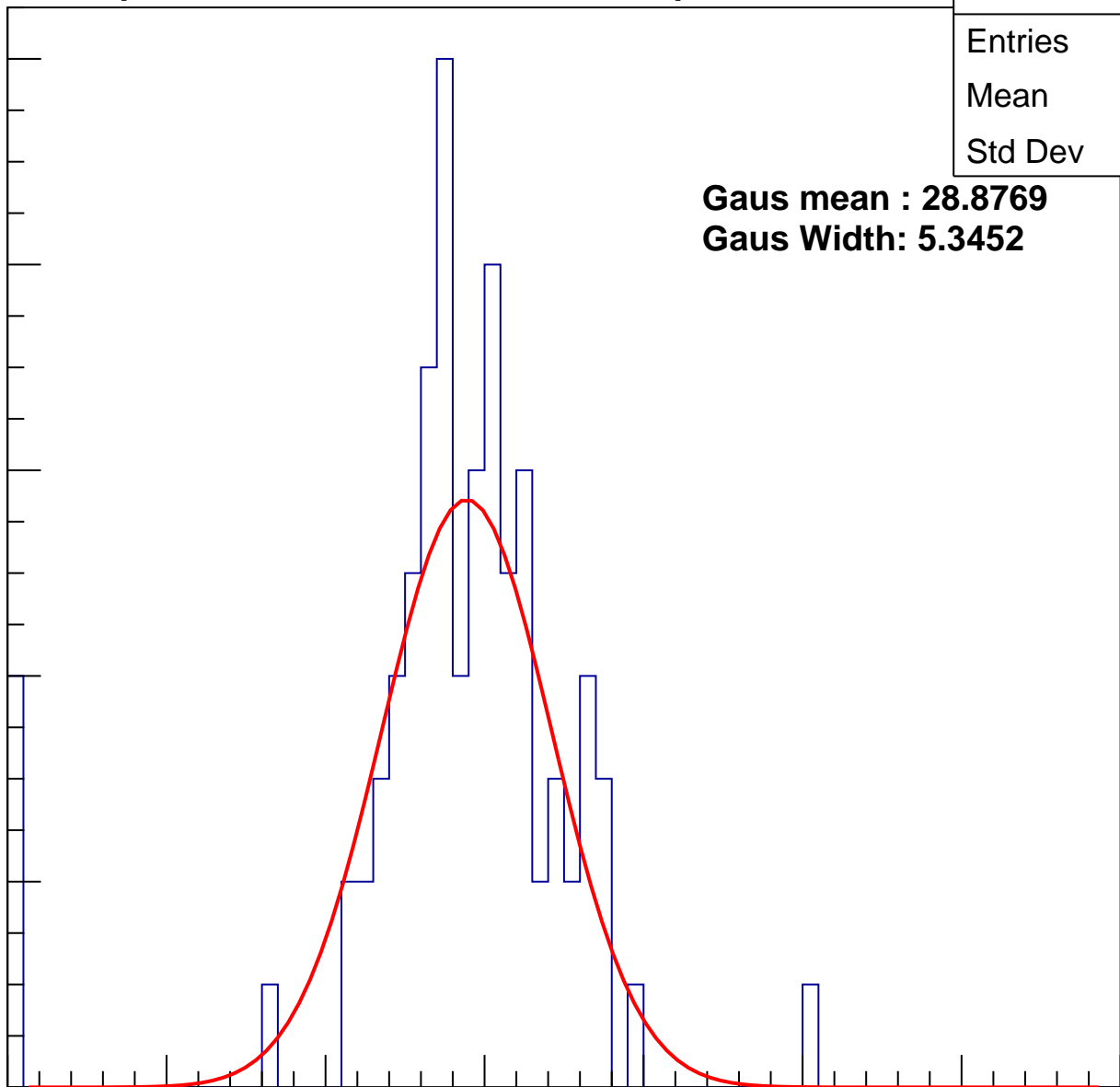
**Gaus Width: 5.3452**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U19-ch126, adc1

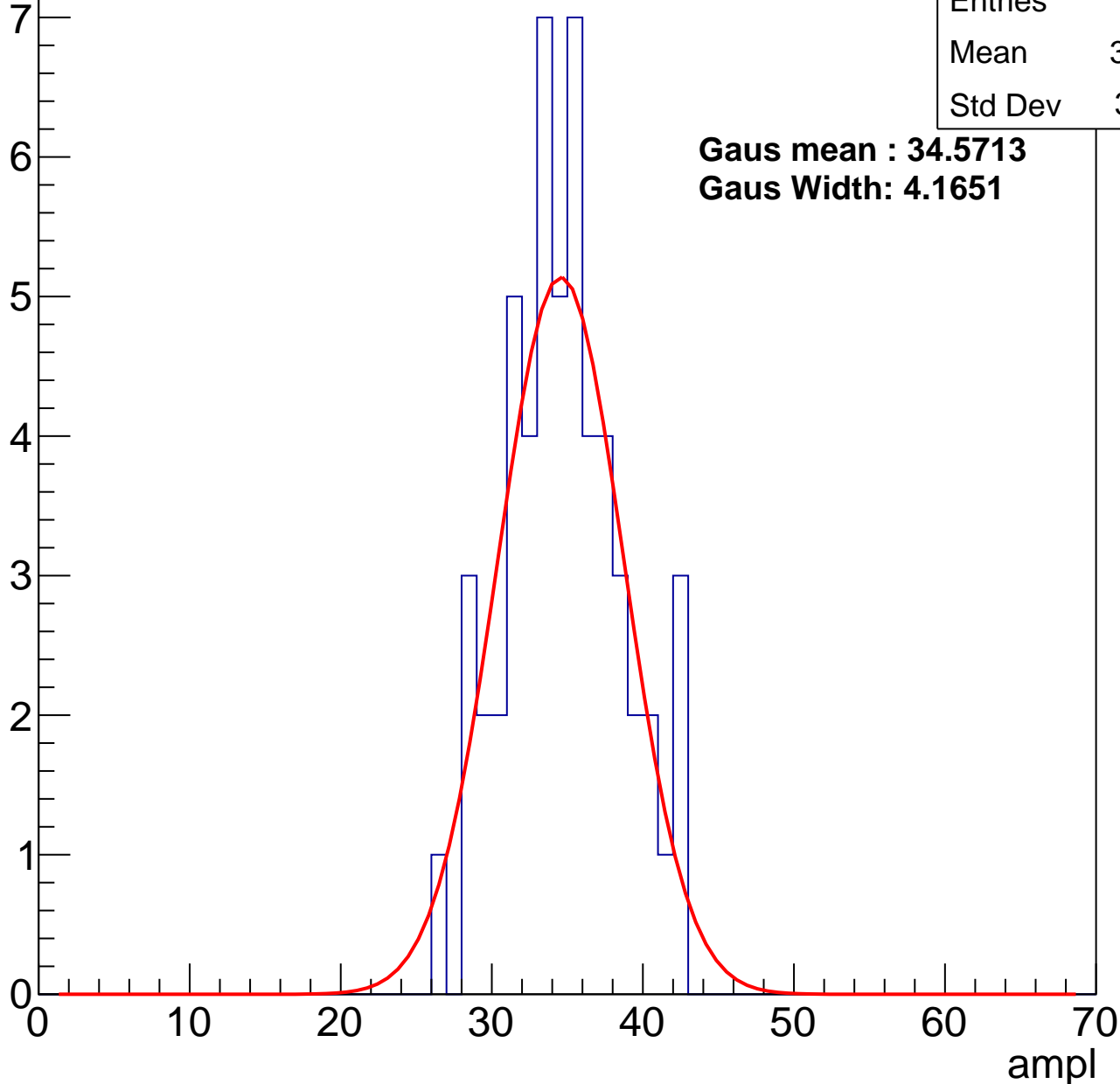
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	55
Mean	34.33
Std Dev	3.781

**Gaus mean : 34.5713**

**Gaus Width: 4.1651**



# B1L101S, U19-ch126, adc2

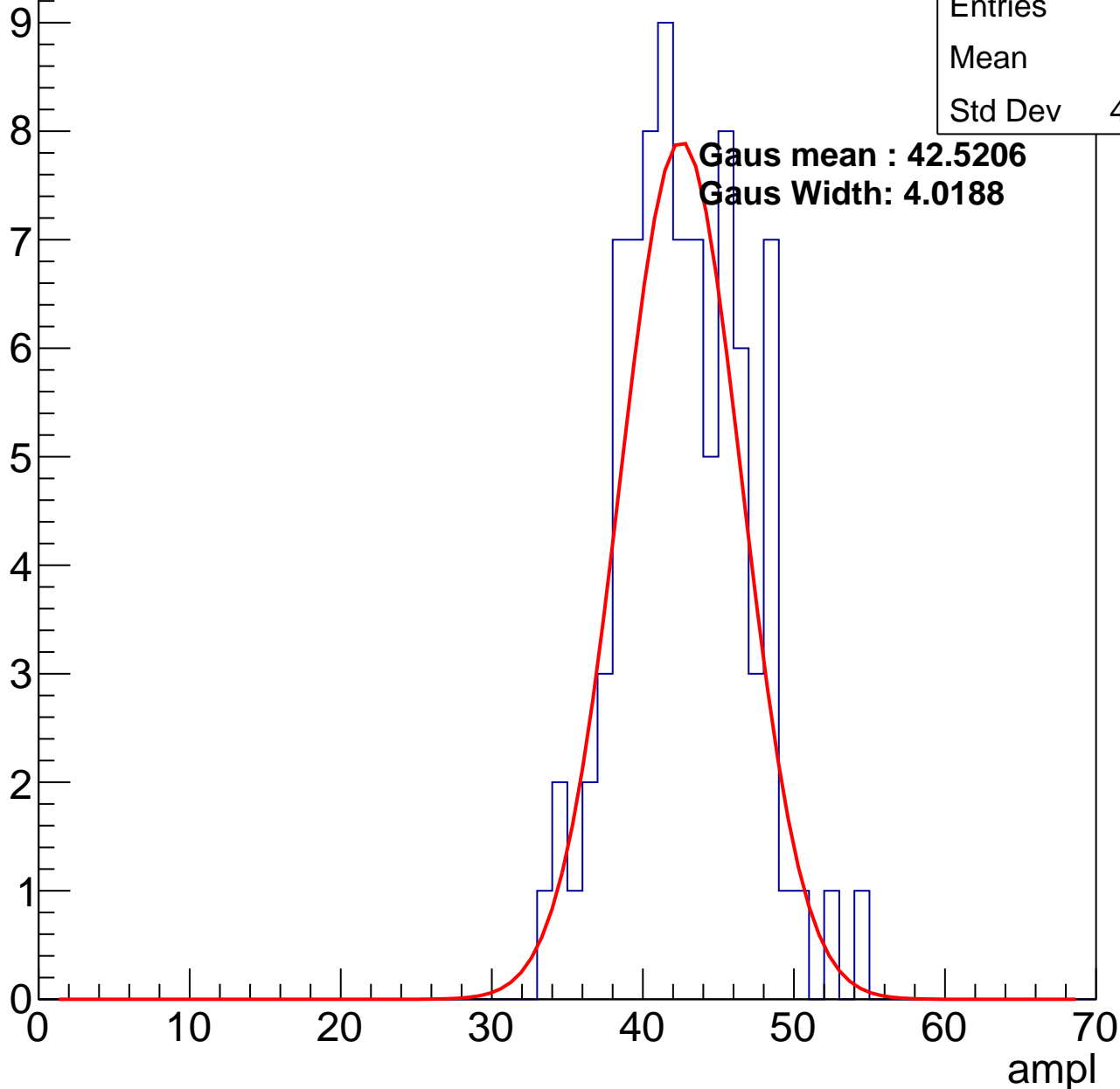
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	87
Mean	42.3
Std Dev	4.142

**Gaus mean : 42.5206**

**Gaus Width: 4.0188**

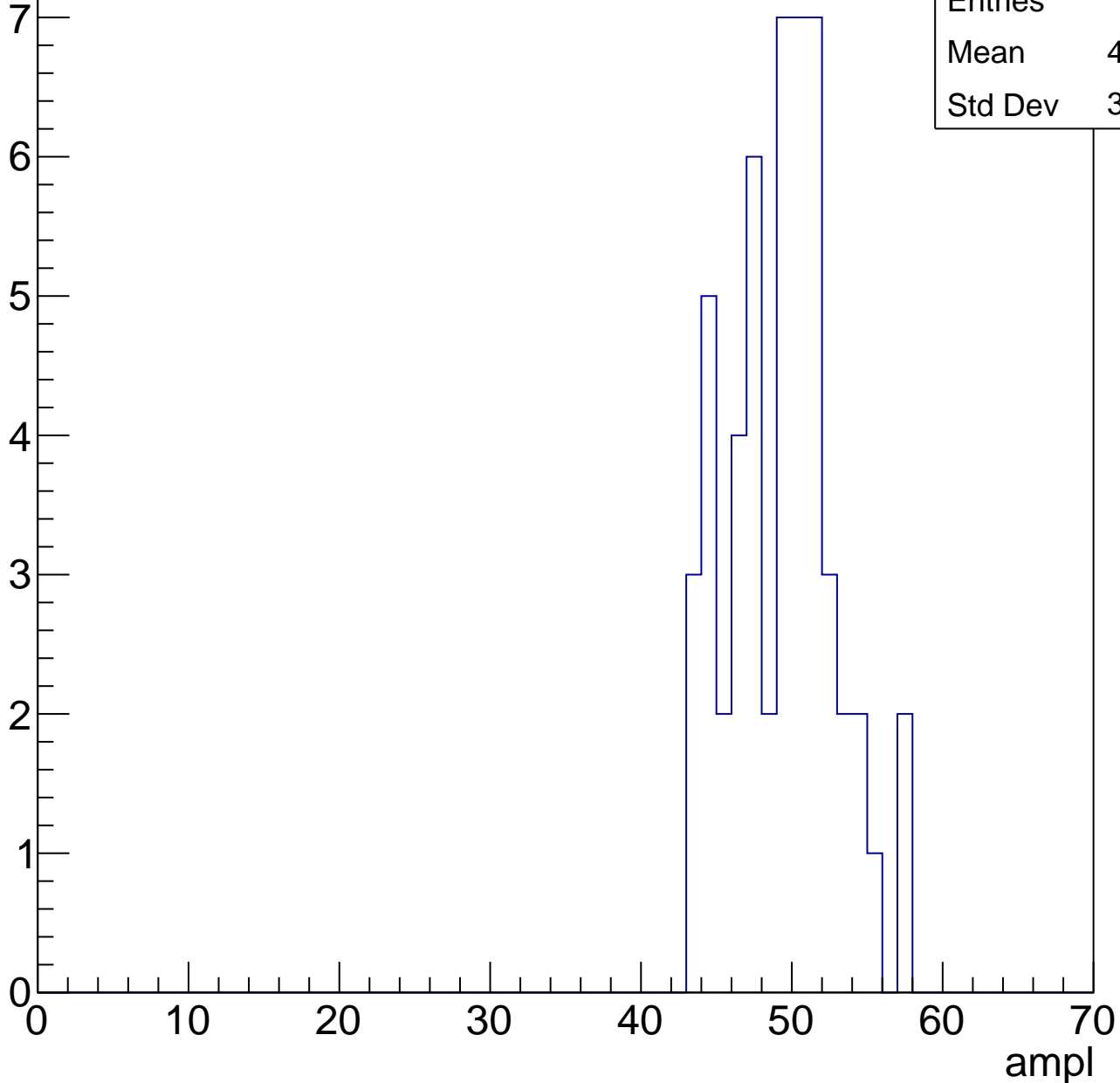


# B1L101S, U19-ch126, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	53
Mean	48.87
Std Dev	3.459

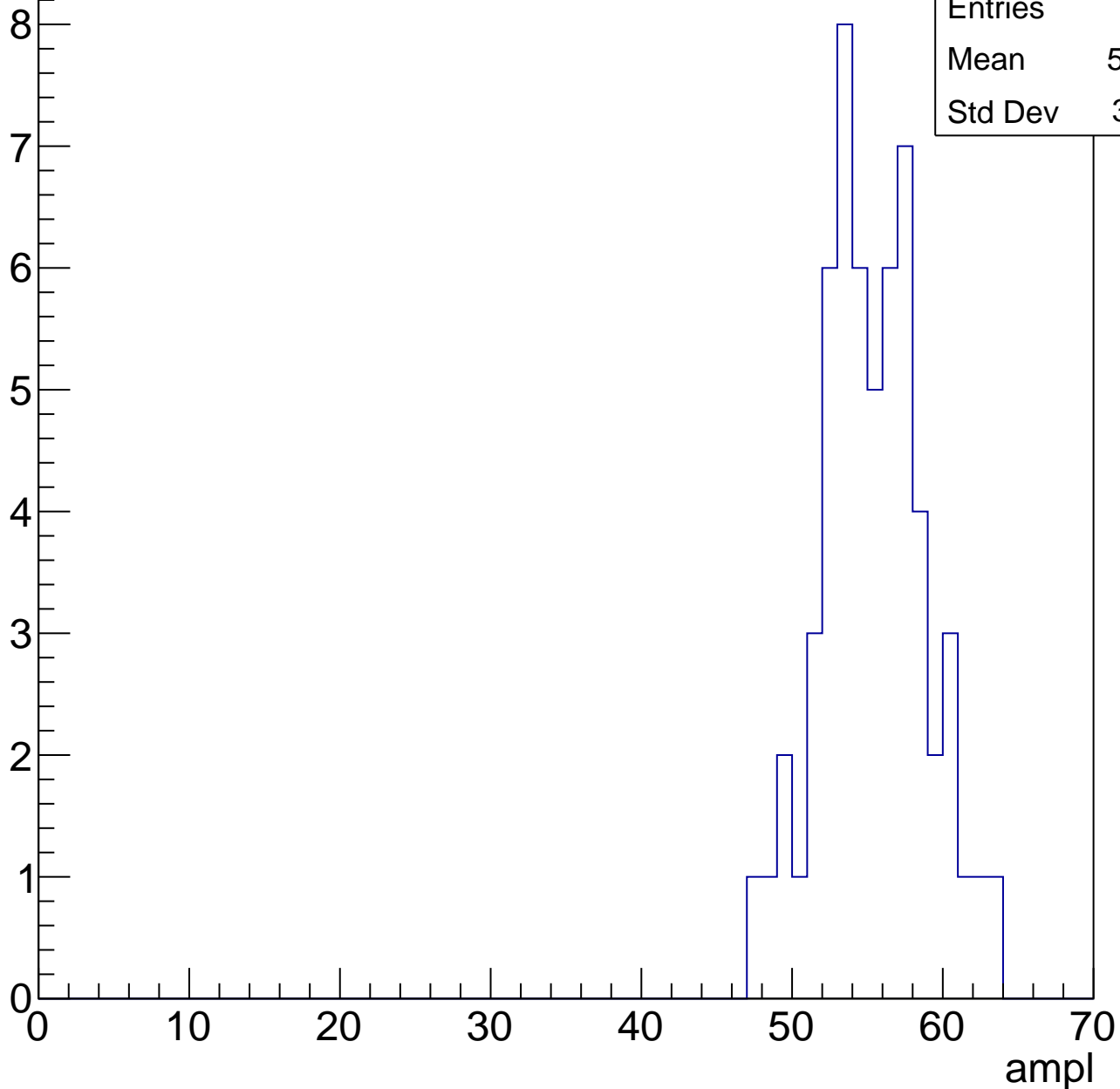


# B1L101S, U19-ch126, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	58
Mean	54.86
Std Dev	3.411

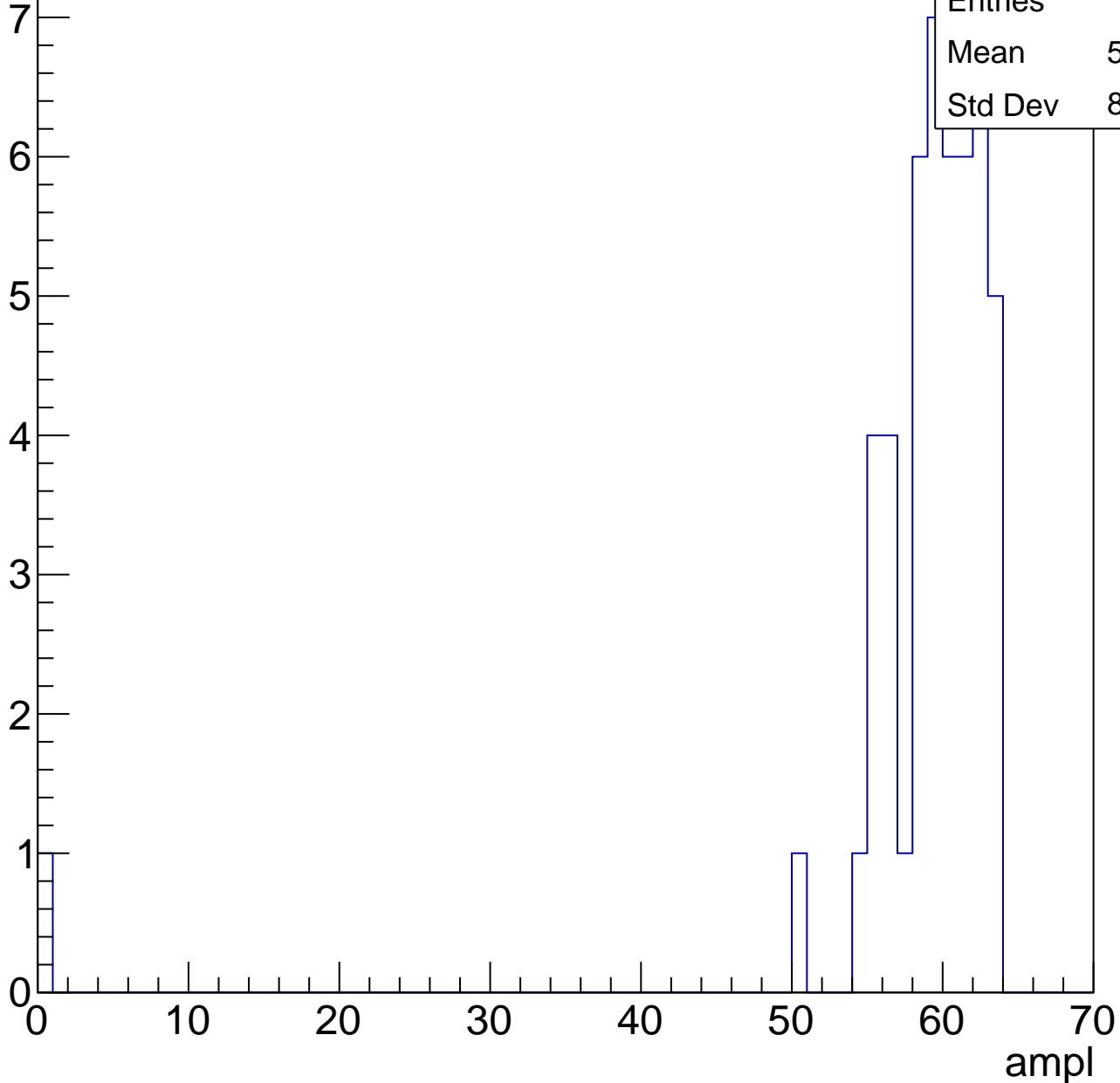


# B1L101S, U19-ch126, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

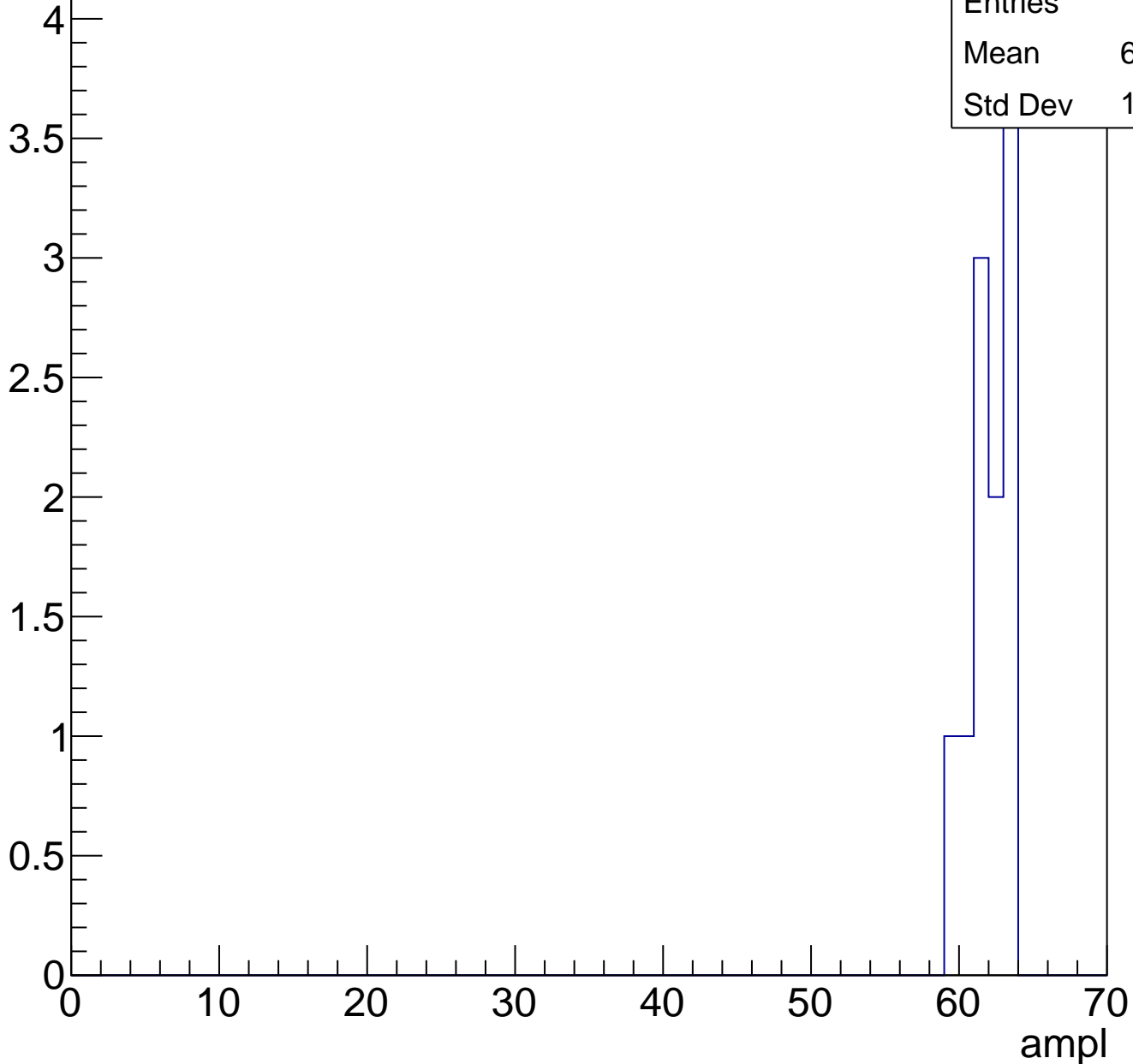
Entries	49
Mean	57.98
Std Dev	8.828



# B1L101S, U19-ch126, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U19-ch126, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U19-ch127, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	83
Mean	30.07
Std Dev	5.02

**Gaus mean : 31.0243**

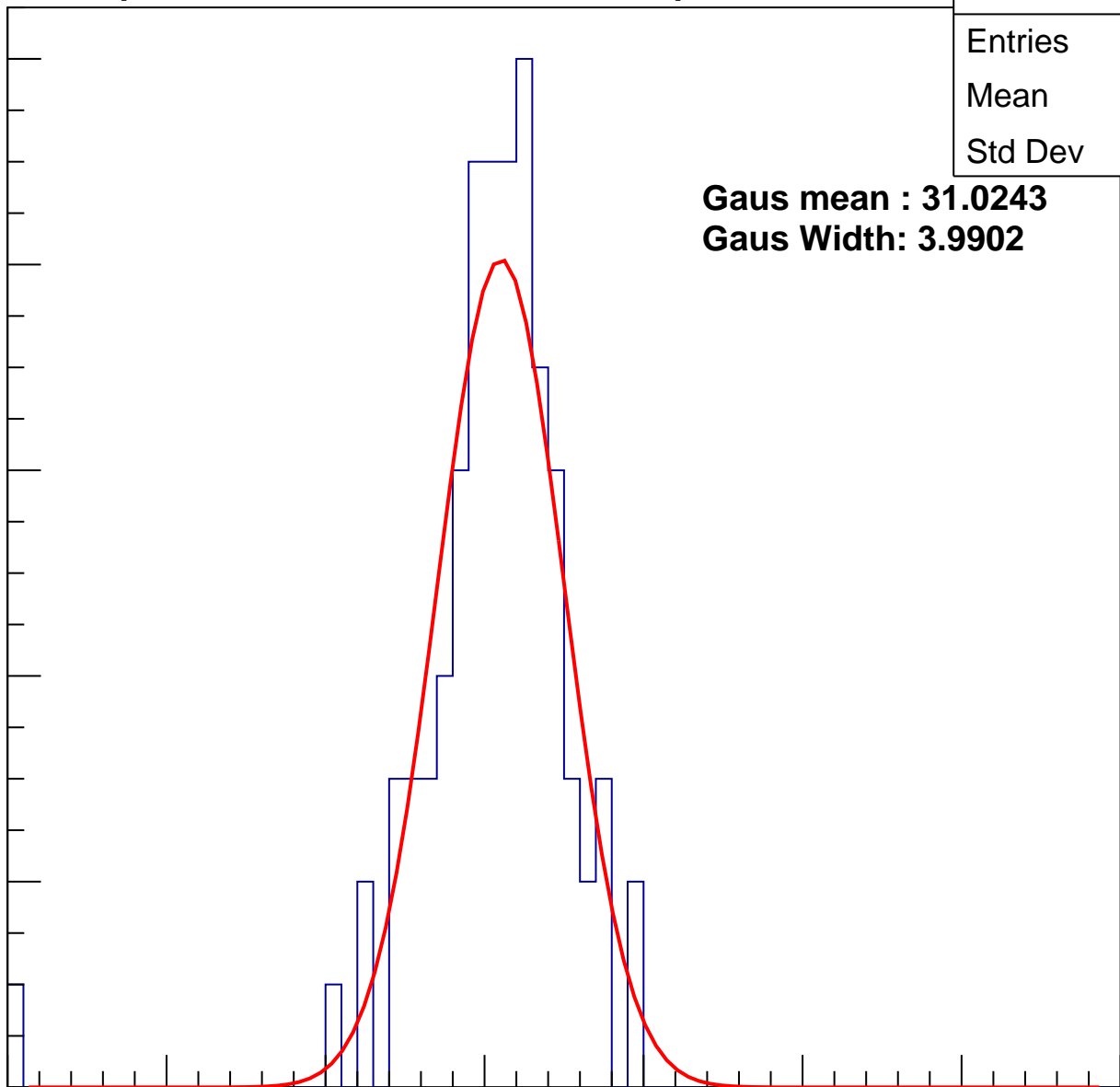
**Gaus Width: 3.9902**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U19-ch127, adc1

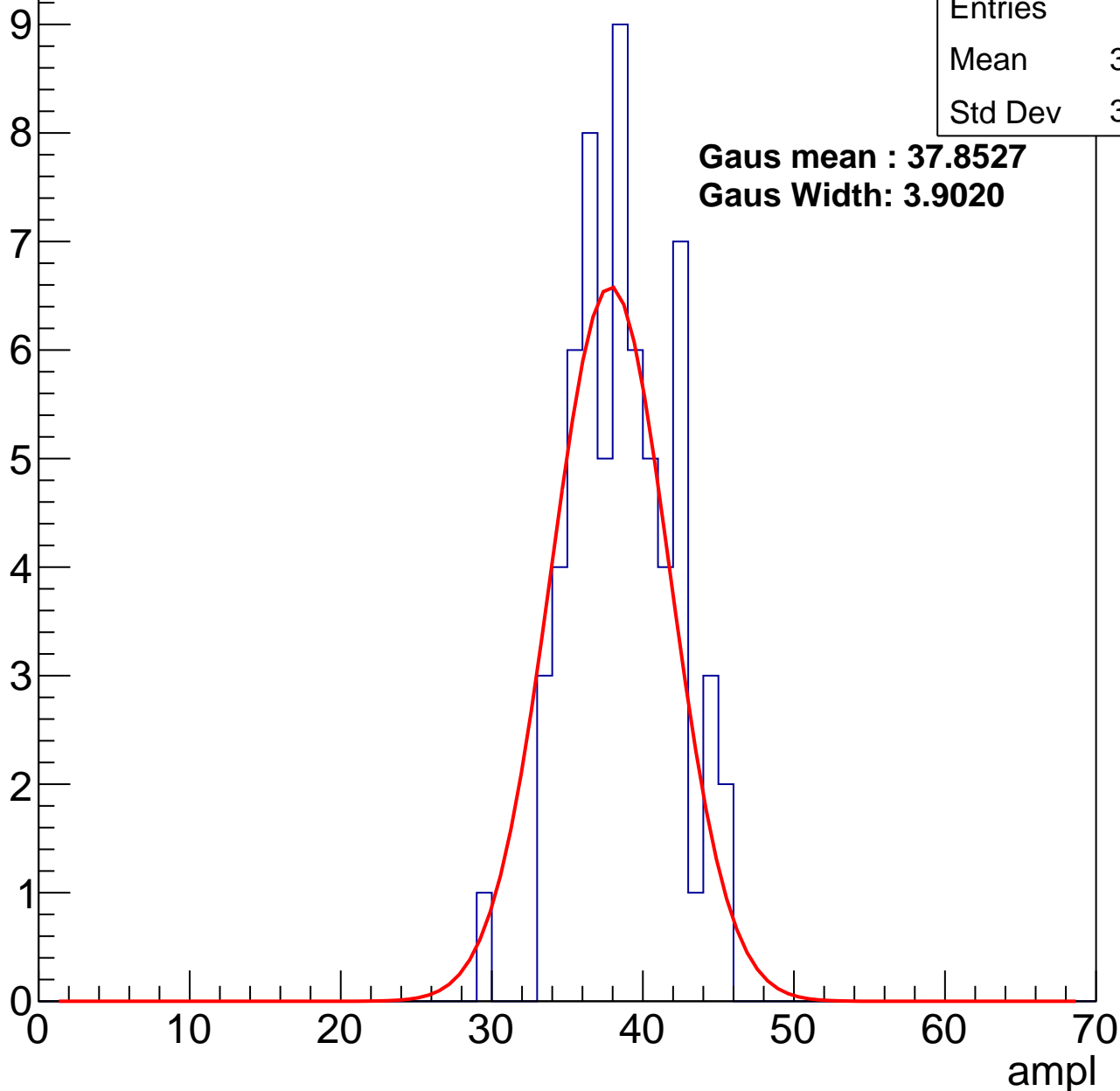
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	38.22
Std Dev	3.338

**Gaus mean : 37.8527**

**Gaus Width: 3.9020**



# B1L101S, U19-ch127, adc2

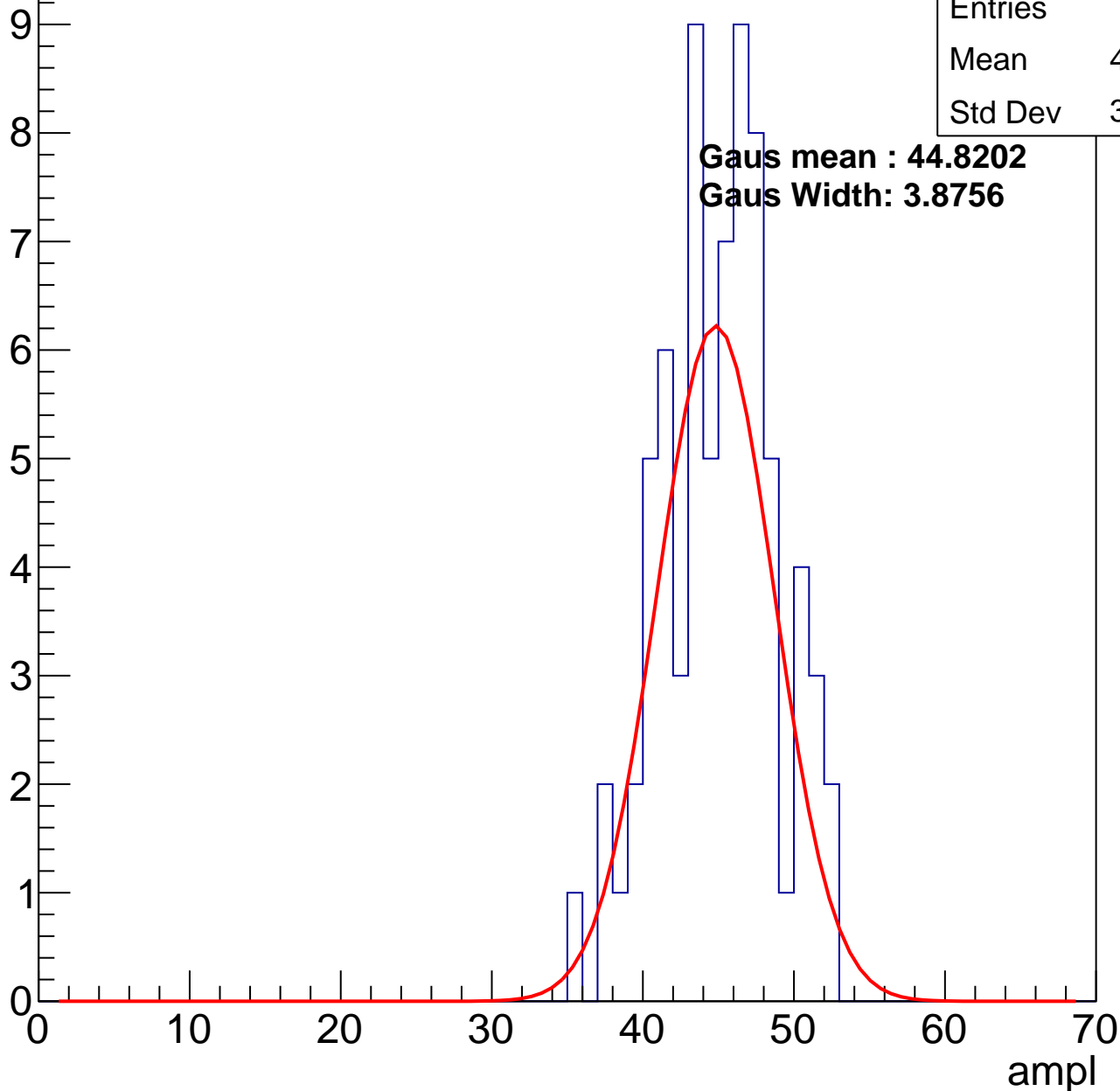
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	73
Mean	44.59
Std Dev	3.763

**Gaus mean : 44.8202**

**Gaus Width: 3.8756**

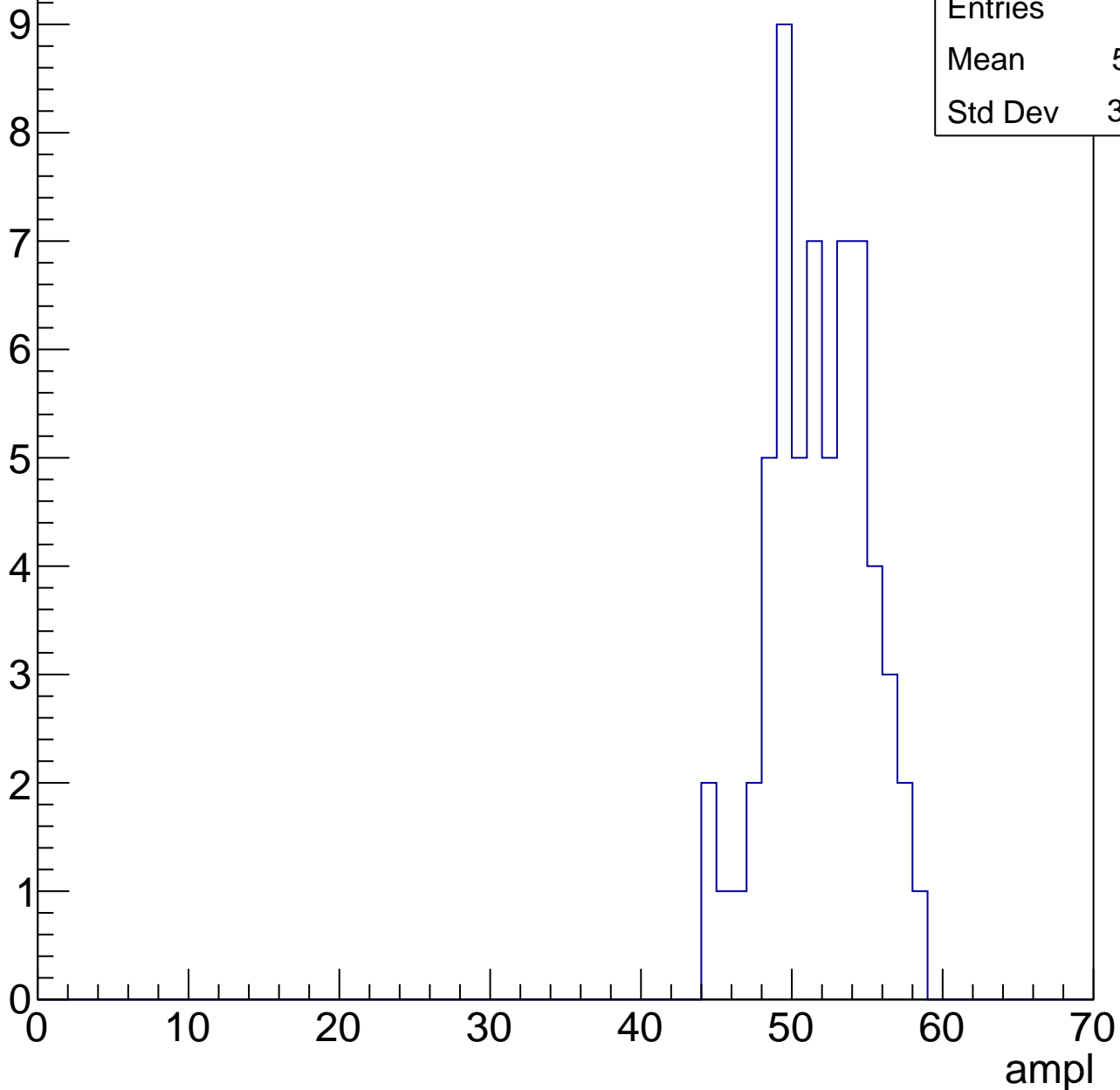


# B1L101S, U19-ch127, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	51.31
Std Dev	3.206

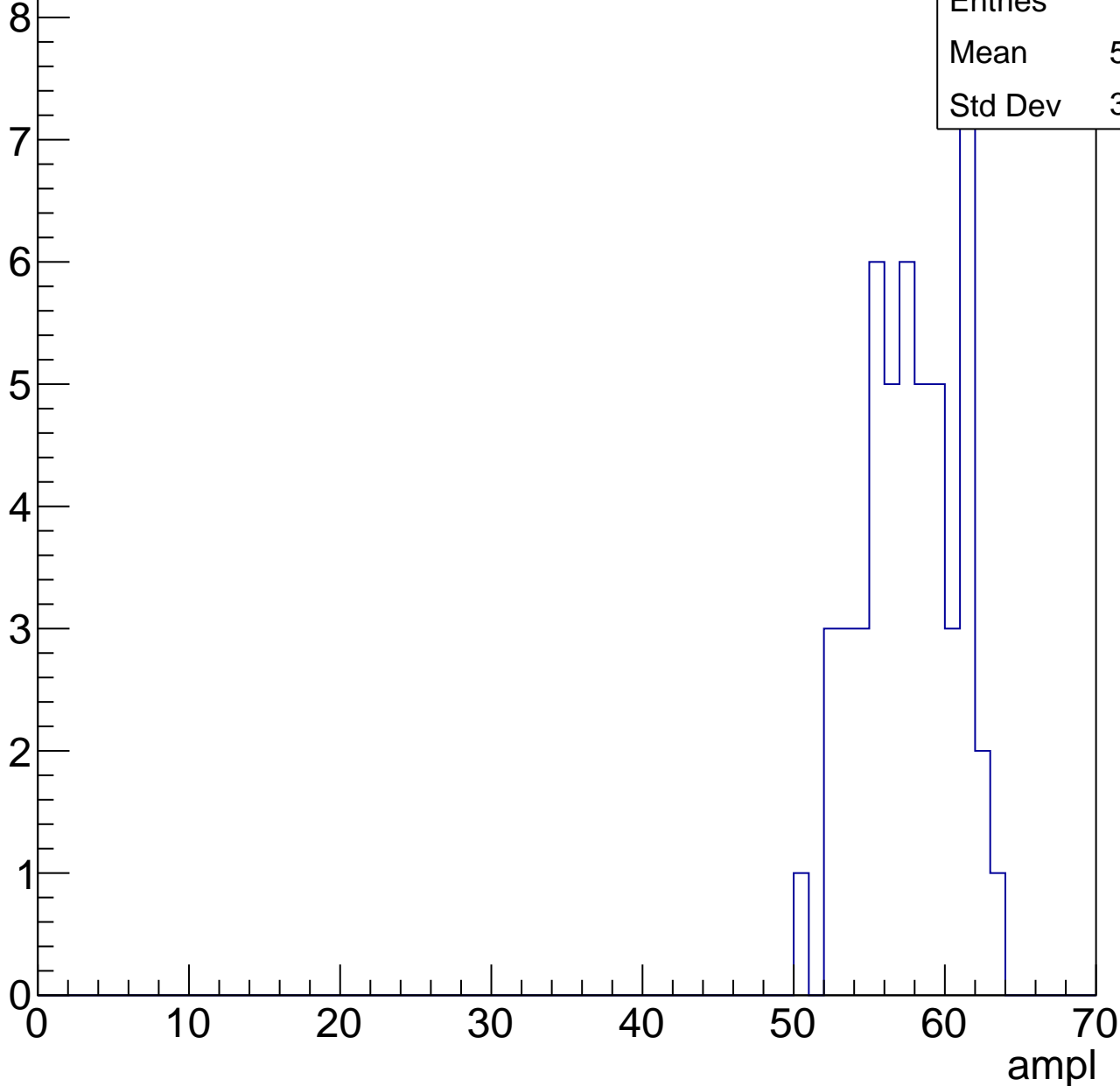


# B1L101S, U19-ch127, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

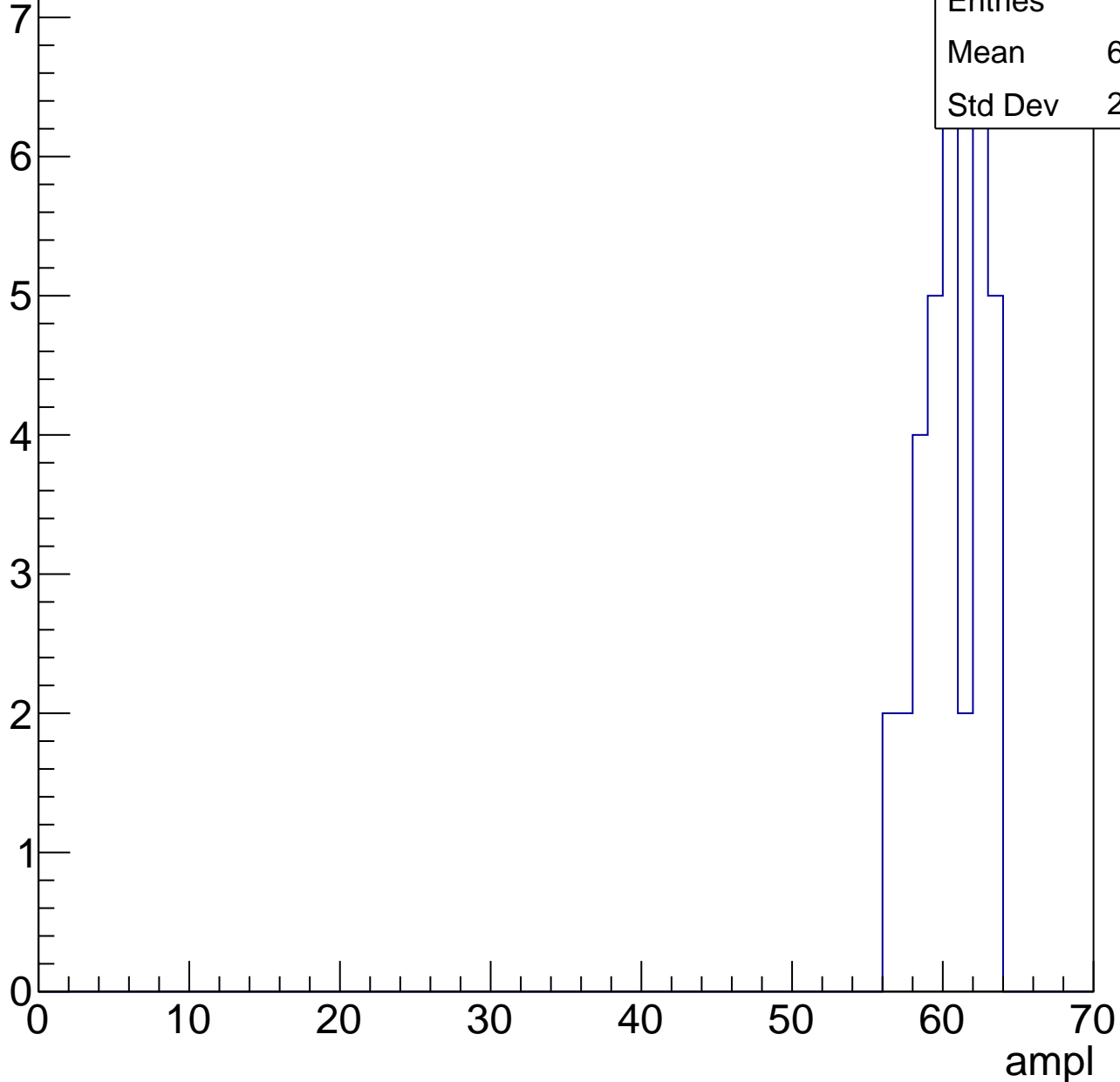
Entries	51
Mean	57.24
Std Dev	3.103



# B1L101S, U19-ch127, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

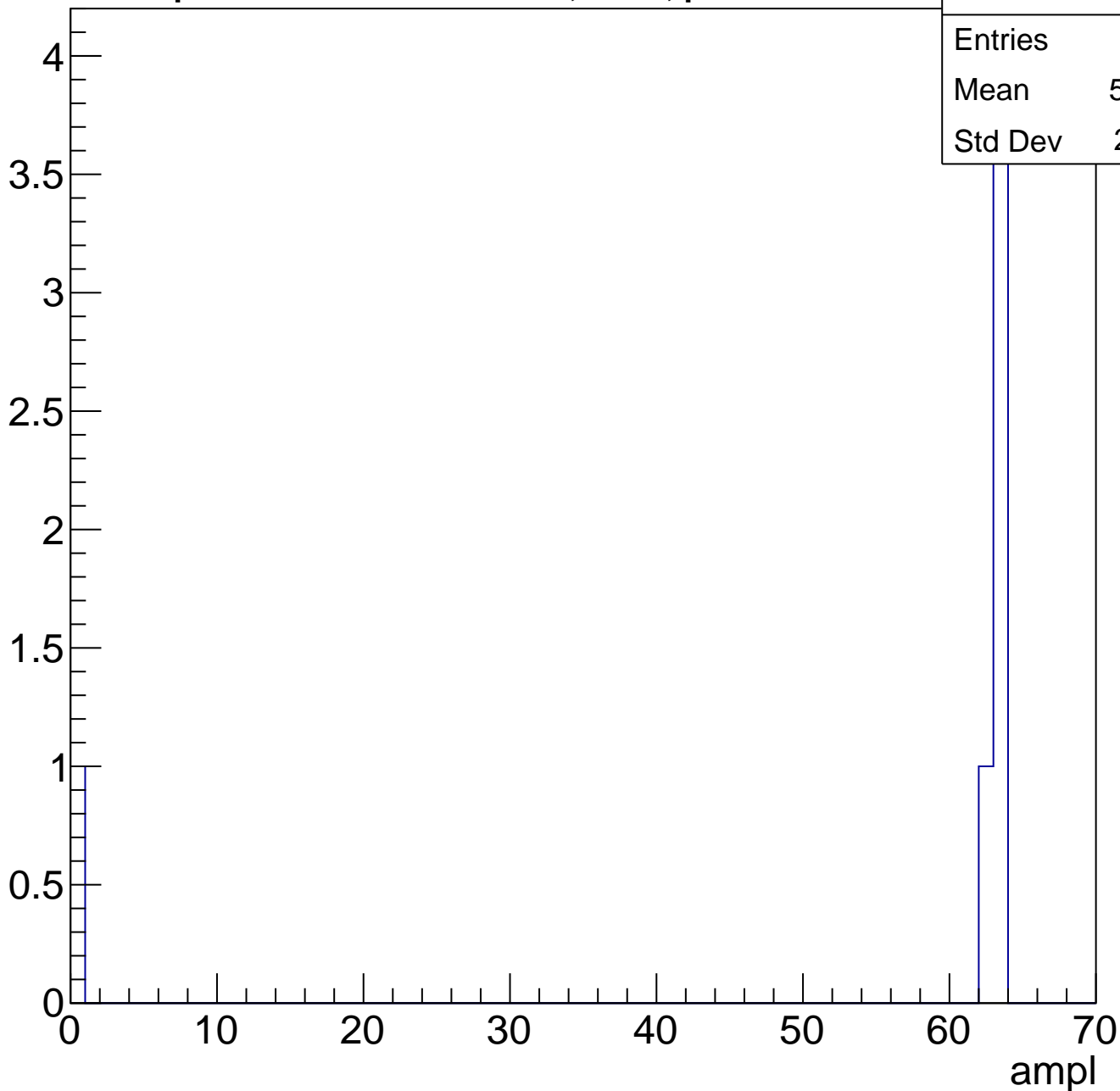


Entries	34
Mean	60.12
Std Dev	2.069

# B1L101S, U19-ch127, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U19-ch127, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U19-ch127, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

